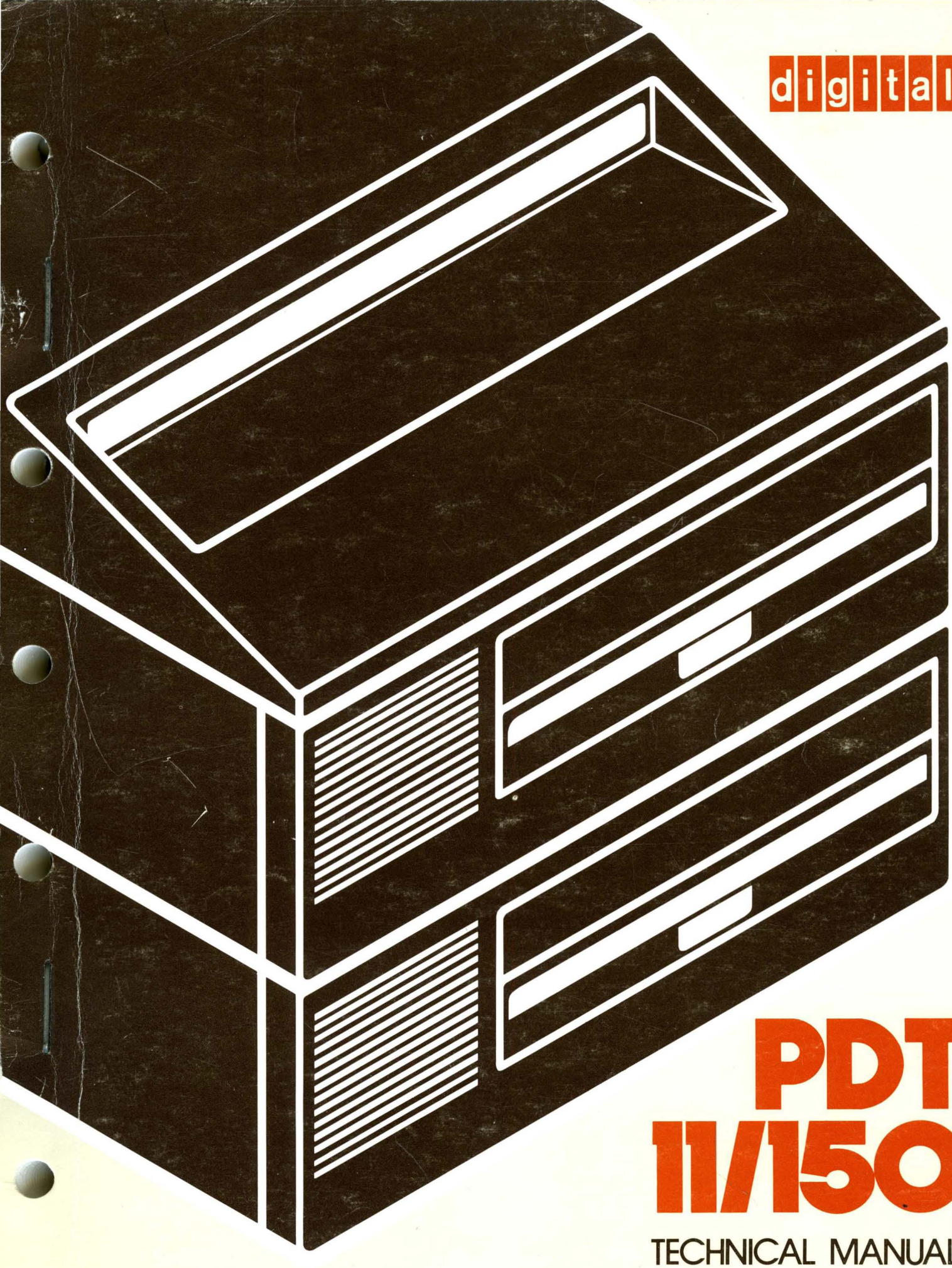
digital



PDT 11/150

TECHNICAL MANUAL

EK-PT150-TM-001

PDT-11/150
TECHNICAL MANUAL

digital equipment corporation • marlboro, massachusetts

1st Edition, April 1980

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

CONTENTS (Cont)

CONTENTS (Cont)

CONTENTS (Cont)

FIGURES

FIGURES (Cont)

FIGURES (Cont)

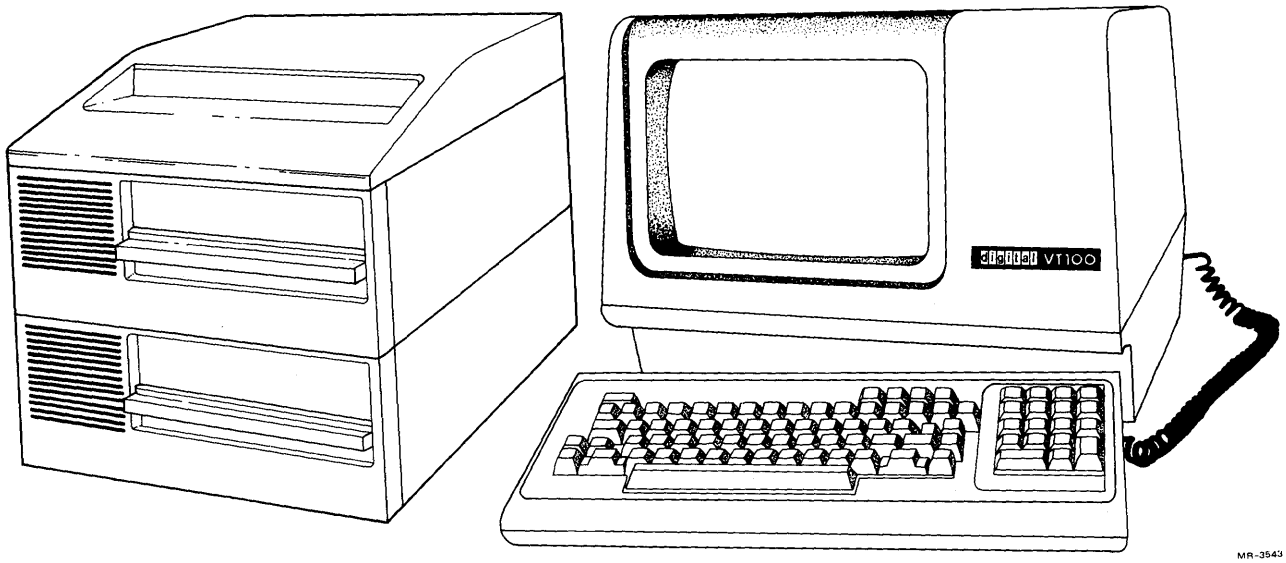
FIGURES (Cont)

TABLES

TABLES (Cont)

PDT-11/150 DUAL DISK
DRIVE UNIT

VT100 CONSOLE TERMINAL



MR-3543

PREFACE

The PDT-11/150 is an LSI-11 microprocessor-based unit that contains one (or two) flexible (floppy) disk drive(s) for program loading and data storage. The unit is available with one of several console devices, each forming a complete programmable system.

This manual defines these systems and provides the technical information required to install them, monitor their performance, and isolate the malfunctions that may occur in each. Also included are general and detailed descriptions of the operation of the modules and assemblies.

Chapter 1 provides a general description of a PDT-11/150 system containing an operator's console and terminals. Also discussed are the features and capabilities of the system and the equipment specifications and options available.

Chapter 2 shows how to install the unit, connect the peripheral devices and initiate the internal self-test program.

Chapter 3 describes the functions of the operator controls and indicators, the loading of the flexible disk into the disk drive, the initiation of the self-test program, and the loading of the system programs contained on the flexible disk.

Chapter 4 provides a general description of the functional operation of the entire unit and detailed descriptions of the operations of each module and assembly.

Chapter 5 contains detailed information on initiating the diagnostic program (on disk) and evaluating its performance. Also discussed are the removal, replacement and repair of assemblies and modules, and disk drive adjustments.

Chapter 6 describes the hardware characteristics of the PDT-11/150 and includes the addresses assigned to the internal registers, detailed descriptions of the register bit functions, and programming considerations.

Appendix A lists the PDT-11/150 component parts and their part numbers.

Appendix B is a glossary of terms and notation used in this manual.

CHAPTER 1
INTRODUCTION

The PDT-11/150 is a small, user-programmable, intelligent terminal that contains a dual flexible (floppy) disk drive assembly for program loading and data storage. The basic unit can communicate with a console terminal, a modem, and a line printer. With the addition of the Cluster EIA (Electronic Industries Association) option, three additional terminals can be connected to operate with the PDT-11/150.

All terminals and devices transfer serial data that conforms to the requirements of EIA standard RS-232-C.

The PDT-11/150 is available with 16K- or 30K-word resident RAM and can be programmed using the standard LSI-11 microprocessor instruction set. Programs can be developed by using a PDP-11/V03 hardware system (or equivalent) running under the RT-11/V3B software operating system.

1.1 TYPICAL SYSTEM CONFIGURATIONS

Figure 1-1 shows a typical PDT-11/150 hardware system with the maximum number of terminals and devices attached. The Standard EIA Converter enables data transfer rates of up to 9.6K baud for the console and line printer terminal. The communications modem operates asynchronously or synchronously with Bell 103, 113, 202, 212 data sets (or equivalents) in full- or half-duplex operation.

The Cluster EIA converter provides the additional interfaces and connectors required to attach three character printers or video display units (VDUs). The maximum data transfer rates of these terminals is 2.4K baud.

The data transfer rates to and from the devices and terminals depend on the applications program or operating system and the number and types of peripheral units connected to the PDT-11/150. Refer to Paragraph 6.2 for detailed information on data transfer rates.

Model Designations

The PDT-11/150 is available with or without a console terminal and is wired to operate with either 50 Hz or 60 Hz ac input power. Any of the options listed in Table 1-1 may also be included.

The model designation specifies the system and unit configurtains of the PDT-11/150 delivered. The designation is stamped on a metallic label attached to the rear panel of the unit. Figure 1-2 describes the model designations and the equipment and options included.

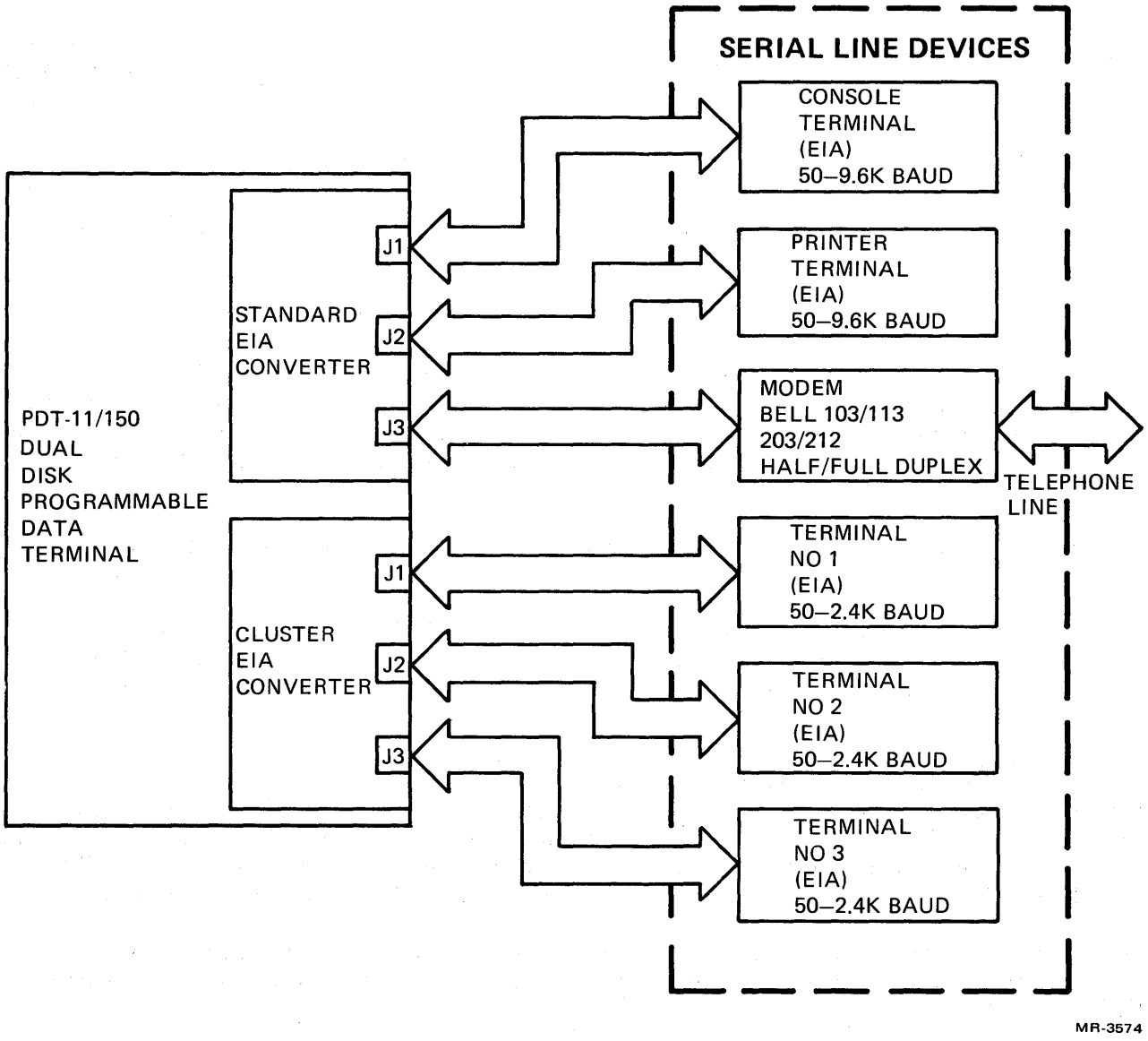
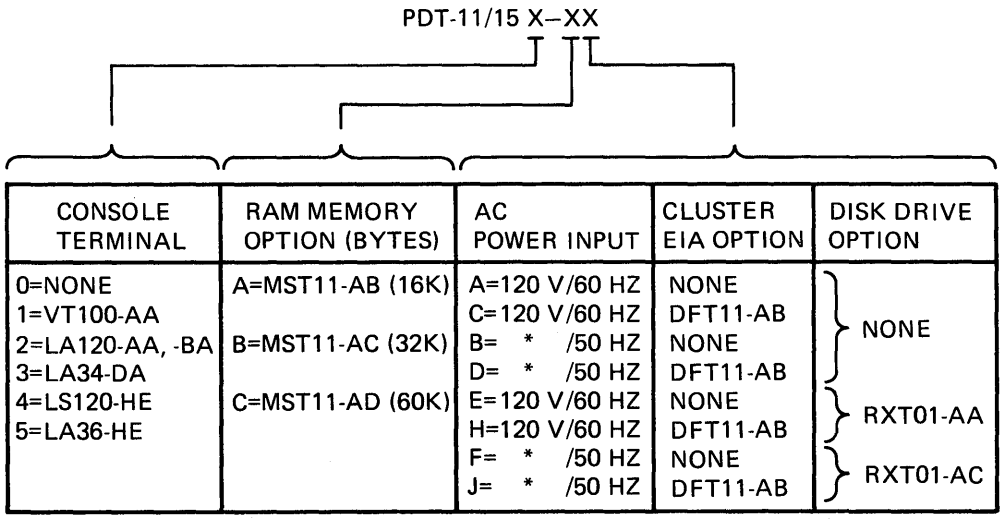


Figure 1-1 Typical PDT-11/150 Flexible (Floppy) Disk Operating System



* AVAILABLE IN THE FOLLOWING VOLTAGE RATINGS: 90–120 VAC, 100–132 VAC, 180–240 VAC, 200–264 VAC

EXAMPLE: PDT-11/151-BH INCLUDES THE FOLLOWING

- VT100-AA CONSOLE TERMINAL
- MST11-AC OPTION (32K BYTES OF RAM)
- 120 V/60 HZ AC POWER INPUT
- DFT11-AB OPTION (THREE EIA TERMINAL INTERFACES)
- RXT01-AA OPTION (SECOND DISK DRIVE)

MR-2330

Figure 1-2 PDT-11/150 Model Designations

Table 1-1 PDT-11/150 Available Hardware Options

Option No.	Description
RXT01-AA	60 Hz disk drive assembly, includes enclosure, rear panel, front bezel, and cable extender (70-15989)
RXT01-AC	50 Hz disk drive assembly, includes enclosure, rear panel, front bezel, and cable extender (70-15989)
DFT11-AB*	Standard EIA converter module (includes flat cable)
MST11-AB** MST11-AC MST11-AD	RAM module/16K bytes RAM module/32K bytes RAM module/60K bytes These three modules include a diagnostic ROM IC that contains the bootstrap loader program.
KDT11-AA*	Intelligence module with ROM program
DLT11*	Peripheral module with USARTs for standard EIA terminals
RXT11*	Disk controller module with ROM program

* Included with all PDT-11/150 models
** MST11-XX are factory-installable only

1.2 EQUIPMENT AND MEDIA SPECIFICATIONS

Table 1-2 lists the mechanical, electrical and environmental specifications for the PDT-11/150 units. Detailed specifications for the console terminal, printers and communications modem operating with the system can be obtained from the appropriate vendor or from a local DIGITAL sales office.

Table 1-3 lists the pertinent specifications for the flexible disk media.

Engineering Specifications – Table 1-4 lists the documents of engineering specifications relating to the PDT-11/150.

1.3 RELATED PUBLICATIONS

Table 1-5 lists the manuals and quides that contain information related to the PDT-11/150 units. This information is available to DIGITAL personnel in hard copy and microfiche, and to customers in hard copy only.

Table 1-2 PDT-11/150 Equipment Specifications

Characteristics	Description
Mechanical	
Overall Dimensions	
Single Disk Unit	51.0 cm (20.08 in) length × 33.02 cm (13.0 in) width × 20.9 cm (8.23 in) height
Dual Disk Unit	51.0 cm (20.08 in) length × 33.02 cm (13.0 in) width × 34.8 cm (13.42 in) height
Weight	
Unpackaged	Single disk unit: 15 kg (33 lb) Dual disk unit: 20.8 kg (46 lb)
Packaged	Single disk unit: 18.1 kg (40 lb) Dual disk unit: 24.9 kg (55 lb)
Environmental	
Temperature	
Operating	15° C to 32° C (59° to 90° F) ambient (Temperature is derated 1.8° C/1000 m or 1° F/1000 ft for altitude.)
Maximum gradient	11° C/hr (20° F/hr)
Nonoperating	-35° C to +60° C (-30° F to 140° F)
Humidity	
Operating	Maximum wet bulb: 25° C (77° F) Minimum dew point: 2° C (36° F) Relative humidity: 20% to 80%
Nonoperating	5% to 95% relative humidity (noncondensing)
System Reliability	Disk Life: 3 million revolutions per track with head loaded. The head contacts 5 tracks when loaded. Seek error rate: 1 in 10^6 seeks Soft read error rate: 1 in 10^9 bits read Hard read error rate: 1 in 10^{12} bits read **NOTE** **The above error rates only apply to media that are properly cared for. Seek errors and soft read errors are usually attributable to random effects in the head/media interface, due to electrical noise, dirt, or dust. Both are defined as "soft" errors if the error is recoverable in ten additional tries or less. "Hard" errors cannot be recovered. Seek error retries should be preceded by an initialize or restore command.**

Table 1-2 PDT-11/150 Equipment Specifications (Cont.)

Characteristics	Description
	To ensure the integrity of the information stored on the disk, the disks should not be in the disk drives when the ac power is initially applied to the unit. The disks should be removed from the disk drives before the ac power is removed from the unit.
Drive Performance	
Data transfer rate (disk to RAM module)	32 μs/16-bit word (nominal)
Track-to-track-move	10 ms/track maximum
Head settle time	20 ms maximum
Rotational speed	360 r/min ± 2.5%; 166 ms/rev (nominal)
Recording surfaces per disk	1
Tracks per disk	77 (0–76) or ($0–114_8$)
Sectors per track	26 (1–26) or ($1–32_8$)
Recording technique	Double frequency
Bit density	3200 bits/in at inner track
Track density	48 tracks/in
Average access*	488 ms
ac Power Requirements	
115 V/60 Hz Input	Single disk drive: 2.5 A Dual disk drive: 3.0 A
90–130 V/50 Hz Input	Single disk drive: 2.5 A Dual disk drive: 3.0 A
180–264 V/50 Hz	Single disk drive: 1.5 A Dual disk drive: 2.0 A
Device Signals	All device signals are serial line and compatible with EIA standard RS-232-C. (Refer to Tables 2-4 and 2-5 for signal requirements.)

* **Seek Settle Rotate Total**

(77 tks/2) × 10 ms + 20 ms + (166 ms/2) = 488 ms

Table 1-3 Flexible Disk Specifications

Specifications	Description
Description	Mylar based, oxide-coated disk
Dimensions	
Disk	19.8 cm (7.8 in) diameter
Jacket	20.26 cm (7.94 in) square
Recording Format	Single-side, industry-compatible according to IBM 3740 floppy disk format, 77 data/address tracks
Operating	
Temperature/Humidity	Media temperature must be within PDT-11/150 operating temperature and humidity range before use.
Storage	
Temperature	–35° C (–30° F) to 52° C (125° F)
Relative Humidity	10% to 80% (noncondensing)
Magnetic field	Exposure to a magnetic field strength of 50 oersteds or greater may result in loss of data.

Table 1-4 PDT-11/150 Engineering Specifications

Document No.	Title
A-SP-KDT11-0-2	TIM Module Specification (PDT-11/150)
A-SP-MST11-0-2	RAM Daughter Module Specification (PDT-11/150)
A-SP-DLT11-0-2	Peripheral Daughter Module Specification (PDT-11/150)
A-SP-DFT11-0-2	I/O Interconnect Module Specification (PDT-11/150)
A-SP-H7833-0-2	Power Supply Specification, H7833 (PDT-11/150)
A-SP-RXT11-0-2	Floppy R/W-Controller Module Specification (PDT-11/150)
A-SP-RX01-0-2	Floppy Disk Drive Specification

Table 1-5 PDT-11/150 Publications

Document No.	Title	Form
EK-PT150-IN	PDT-11/150 Installation Guide	Hard Copy
EK-PT150-J1	PDT-11/150 Mini Maintenance Hardware Guide	Hard Copy
EK-PT150-TM	PDT-11/150 Technical Manual	Hard Copy/ Microfiche
EK-PT150-UG	PDT-11/150 User Guide	Hard Copy/ Microfiche
EK-11150-IP	PDT-11/150 Programmable Data Terminal*	Hard Copy/ Microfiche
EK-13077-IP	70-13077 Flexible Disk Drive*	Hard Copy/ Microfiche

* Illustrated Parts Breakdown (IPB)

1.3.1 Ordering Information for DIGITAL Personnel

Additional copies of this document and hard copies of this document listed in Table 1-5 may be obtained from:

Digital Equipment Corporation
444 Whitney Street
Northboro, Massachusetts 01532
ATTN: Printing and Circulation Services (NR2/M15)
Customer Services Section

Microfiched documents are available from:

Digital Equipment Corporation
Micropublishing Group
BU/E46
Bedford Research Park
Crosby Drive
Bedford, Mass. 01730

1.3.2 Ordering Information for Customers

Purchase orders for supplies and accessories should be forwarded to:

Digital Equipment Corporation
Accessories and Supplies Group
Cotton Road
Nashua, New Hampshire 03060

Contact your local sales office or call DIGITAL Direct Catalog Sales toll-free (800) 258-1710 from 8:30 a.m. to 5:00 p.m. eastern standard time (U.S. customers only). Customers in New Hampshire, Alaska and Hawaii should dial (603) 884-6660. Terms and conditions include net 30 days and f.o.b.

DIGITAL plant. Freight charges will be prepaid by DIGITAL and added to the invoice. The minimum order is $35.00 (does not apply when full payment is submitted with an order). Checks and money orders should be made out to Digital Equipment Corporation.

1.4 TECHNICAL REFERENCE MATERIAL

The PDT-11/150 includes several functional IC (integrated circuit) elements which are described in detail in vendor-supplied documentation or in DIGITAL specifications. Table 1-6 lists the vendors' items and reference documentation. Table 1-7 lists the DIGITAL Specification numbers for the LSI-11 Microprocessor IC set.

Table 1-8 lists the circuit schematics (CSs) for the PDT-11/150 unit. These schematics contain the detailed wiring information of the modules and are available as part of the Field Maintenance print set. The Field Maintenance print set consists of mechanical and electrical drawings of the unit and is available at the address of the Accessories and Supplies Group listed in Paragraph 1.3.2. The ordering number is MP00720.

Table 1-6 Vendor IC Reference Documentation

Component	Document
8085A 8-bit microprocessor 8155 RAM/I/O timer 8259-5 programmable interrupt controller 3245 quad TTL to MOS driver 2104A (4K × 1-bit) dynamic RAM 2117-3 (16K × 1-bit) dynamic RAM 2616E 16K (2K × 8) ROM (also 8316E)	Intel Component Data Catalog
FD1771-1 floppy disk formatter/controller	Western Digital MOS/LSI Devices Product Catalog
8136 (DM8136) 6-bit unified bus comparator	National Semiconductor TTL Data Book
1414 (MG14146) dual- differential comparator	Motorola Linear Integrated Circuits Data Book

Table 1-6 Vendor IC Reference Documentation (Cont.)

Component	Document
MC1488L quad line drivers MC1489 quad line receivers	Signetics Digital Linear MOS Data Book
2651 programmable communications interface	Signetics Bipolar MOS Microprocessor Data Manual
75107 dual line receiver	National Memory Data Book
NE556 precision timing* LM393 differential comparator LM301 operational amplifiers (DEC301) 7812-04 (US 7812) positive voltage regulator 7805 (ua7805) positive voltage regulator 733 (ua733) differential video amplifier	Texas Instruments The Linear Control Circuits Data Book for Design Engineers (First Edition)
74LS138 3 to 8 line decoder/multiplexer 74LS 141 BCD-to-decimal decoder/driver 74LS151 1 of 8 data selector/multiplexer 74LS157 quad 2 to 1 line data selector/multiplexer 74LS158 (inverted data output LS157) 74LS161 synchronous 4-bit counter	Texas Instruments The TTL Data Book for Design Engineers

*NE556 is a dual NE555, which is described in the data book.

Table 1-6 Vendor IC Reference Documentation (Cont.)

Component	Document
74LS174 hex D-type flip-flop	
74LS175 quad D-type flip-flop	
74LS197 binary counter	
74LS244 octal buffers/line drivers and receivers	
74LS245 octal bus tranceivers	
74LS373 octal D-type latches	
74LS374 octal D-type flip-flops	
74LS393 dual 4-bit binary counters	
747497 synchronous 6-bit binary rate multiplier	
747406 hex inverter buffer/drivers	

Table 1-7 DIGITAL LSI-11 Microprocessor IC Specifications

LSI-11 IC	Specification No.
Control ROM 1 (microm)	23003B5
Control ROM 2 (microm)	23001B5
Processor Control	23002C4
Processor data	2111549-01

Table 1-8 PDT-11/150 Circuit Schematics

Drawing No.	Title
CS 5413271 (Sheets 1–9)	TIM Intelligence Module
CS 5413275 (Sheets 1–3)	MST11 TIM RAM Module
CS 5413269 (Sheets 1 and 2)	TIM Peripheral Module
CS 5413267	EIA Level Converter for TIM
CS 5413427	EIA/Connector Cluster Option
CS 5413343	H7833 Power Supply Module
CS 5413273 (Sheets 1–6)	RX36 Floppy Controller

CHAPTER 2
UNPACKING/INSTALLATION

The PDT-11/150 programmable data terminal is a free-standing, self-enclosed unit that can be placed on a desk or table. The console device, modem, printer, and terminals that operate with the unit are attached by cables to its rear panel. The devices can be located adjacent to the unit or at a remote location.

PDT-11/150 units are packaged in reinforced cartons and protected by side cushions and a protective cover. The *PDT-11/150 Installation Guide*, EK-PT150-IN, is included with the unit. All remaining publications ordered are supplied in a separate container.

This chapter explains how to unpack the PDT-11/150 and supporting documents, and how to inspect the contents and connect the units with their associated devices.

2.1 UNPACKING AND INSPECTION

Figure 2-1 shows how to unpack a dual drive unit. The single drive unit is packaged similarly.

1. Remove the unpacking procedure diagram attached to the outside of the PDT-11/150 container.

2. Remove the PDT-11/150 unit according to the procedures on the diagram.

CAUTION

Do not lift the unit by grasping the front door handles of the disk drive assembly.

3. Visually inspect the unit for any physical damage.

NOTE

If there is damage, notify a local DIGITAL sales office.

4. Open all other cartons supplied and remove their contents.

5. Using the packing lists attached to each carton, inspect the contents of each to ensure that all items listed are supplied.

6. Connect the female end of the ac power cord to the recessed male connector on the rear panel of the unit.

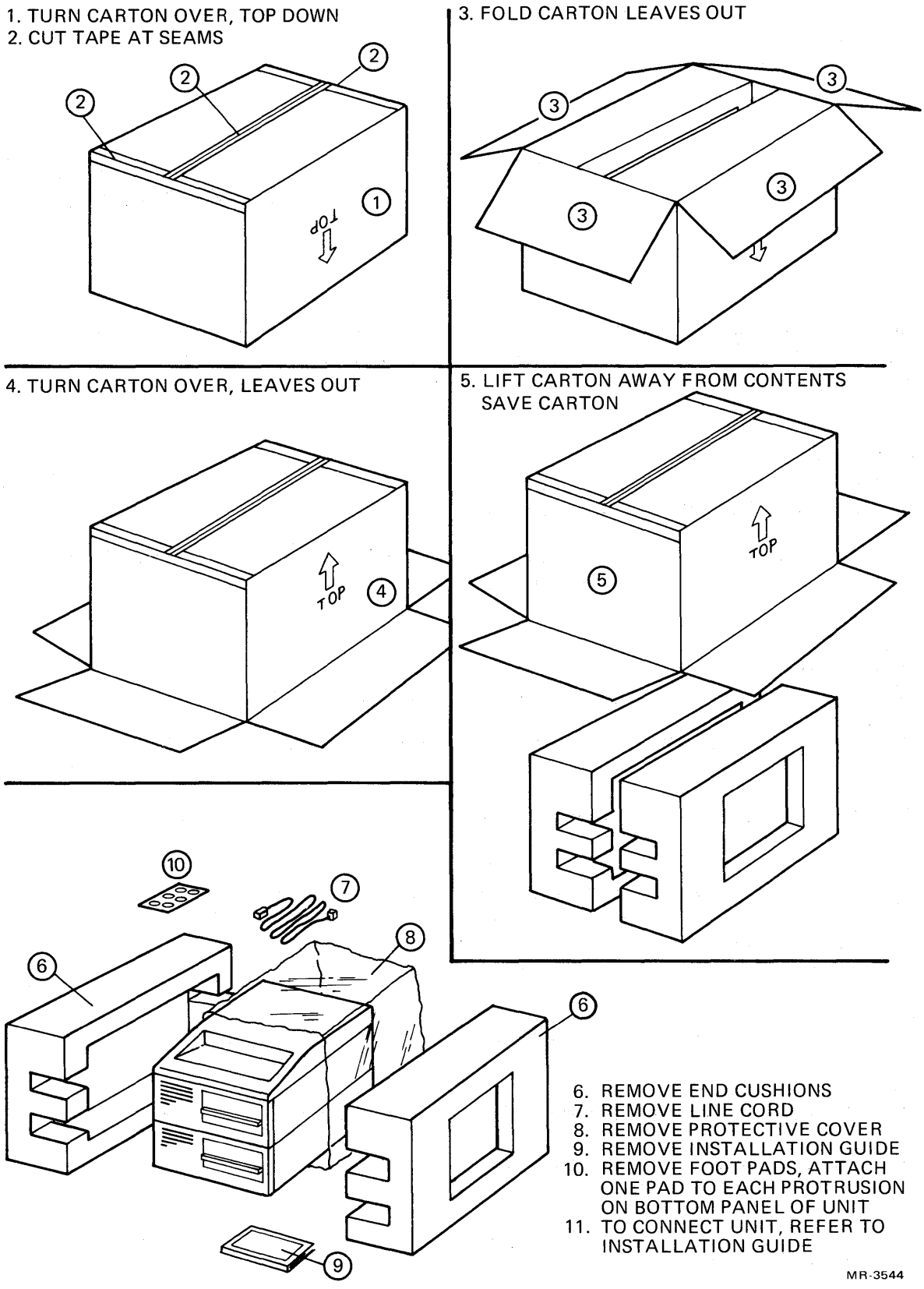


Figure 2-1 PDT-11/150 Unpacking Procedure

CAUTION

PDT-11/150 units are available to operate with several variations of the ac input power. Check the voltage and frequency listed on the metallic label on the rear panel of the unit to ensure that the power supplied at the site is compatible with the unit's requirements.

2.2 SITE PREPARATION AND CONNECTIONS

Figure 2-2 shows the overall dimensions of the single and dual disk drive units. In a single disk drive unit, the disk drive is designated Disk Drive 0. In a dual disk drive unit, Disk Drive 0 is located above Disk Drive 1. Adequate clearance is required at the front of the unit to monitor the indicators on the front panel and to allow the insertion and removal of a disk. The rear of the unit should also be clear for easy access to the ac power switch and mode switch and to permit the free circulation of air through the fan (also located on the rear panel). The signal and power cables that attach to the connectors on the rear panel should be unobstructed and without sharp bends.

NOTE

To prevent the accumulation of film and foreign matter on the disk and disk drive components, the PDT-11/150 should be operated in locations free of dust or industrial contaminants.

2.2.1 AC Power Requirements

Table 2-1 lists the voltage, frequency and current ratings of the PDT-11/150 models. Each unit is shipped with the appropriate ac power cable (also listed). Additional cable lengths are available on request. A separate ac power outlet is required for connection of the PDT-11/150 power cord and console terminal power cord. The main ac line to the outlet can be fused at 10 A or greater.

NOTE

Do not connect appliances or office equipment to the same ac circuits that supply power to the PDT-11/150 unit or associated console and terminals.

To connect the ac power, perform the following precedures:

1. Set the ac power switch on the rear panel to the OFF (0) position.
2. Connect the male end of the line cord to the ac outlet.
3. Connect the female end of the line cord to the rear panel of the PDT-11/150 unit.

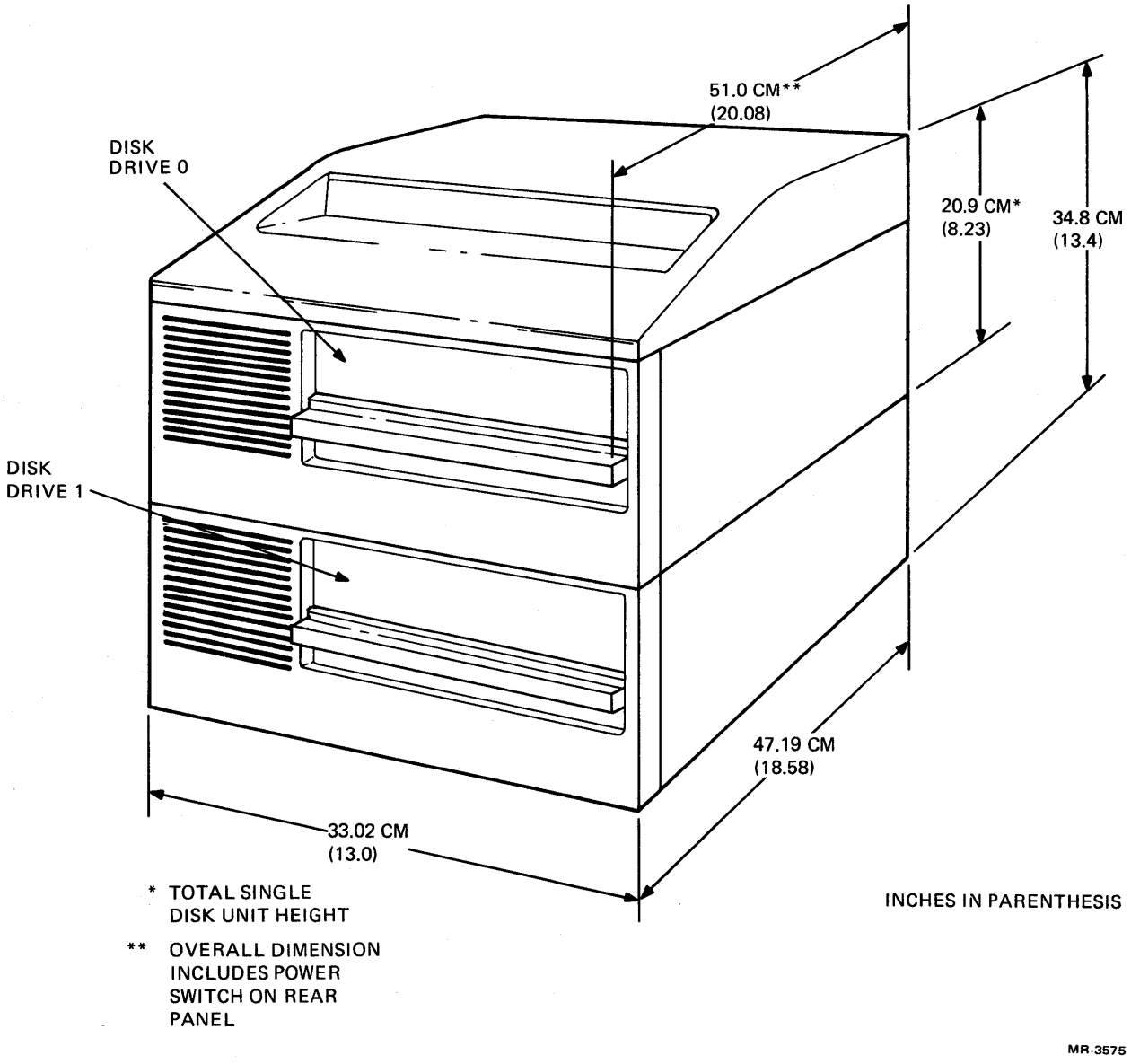


Figure 2-2 PDT-11/150 Single and Dual Disk Unit Dimensions

Table 2-1 AC Power Requirements

Model No.	Voltage (ac)	Line Current	ac Cable No.*
PDT-11/150-AA, -AC -BA, -BC, -CA, CC (single disk drives)	100–125 V/60 Hz	2.5 A	1700083-09 (125 V ac)
PDT-11/150-AE, -AH, (dual disk drives)	100–125 V/60 Hz	3.0 A	170083-10 (250 V ac)
PDT-11/150-AB, -AD, -BB, -BD, -CB, -CD (single disk drives)	90–130 V/50 Hz 100–130 V/50 Hz	2.5A	
	180–240 V/50 Hz 200–264 V/50 Hz	1.5 A	
PDT-11/150-AF, -AJ, -BF, -BJ, -CF, -CJ (dual disk drives)	90–130 V/50 Hz 100–130 V/50 Hz	3.0 A	
	180–240 V/50 Hz 200–264 V/50 Hz	1.5 A	

* Cable lengths are 1.90 m (6.25 ft).
Cable 170083-09 required for Japan.
Cable 170083-10 required for Europe.

2.2.2 Serial Line Cable Connectors

Three 25-pin serial line connectors are mounted on the rear panel of the PDT-11/150 and an additional three 25-pin connectors are optional as shown in Figure 2-3. All cables from the devices attach to these connectors through compatible 25-pin RS232-type plugs. Table 2-2 lists the rear panel assignments and connector designations. The connector type used at the other end of a cable depends on the device. Cable assemblies are normally included with the terminals; however, additional cables of various lengths are available from DIGITAL.

Some of the typical cable assembly types are listed in Table 2-3 and can be ordered by contacting a local DIGITAL sales office.

2.2.2.1 EIA Connector Pin Assignments – Figure 2-3 shows the contact numbering of the EIA connectors on the rear panel. The modem connector (J3) of the Standard EIA connectors is male and all other connectors on both the Standard EIA and Cluster EIA options are female. The signal/pin assignments for the standard connectors are listed in Table 2-4 and those for the cluster connectors are listed in Table 2-5. These signals are pin-compatible with equipment conforming to RS-232-C specifications, but not all the signals defined by RS-232-C are required by the PDT-11/150.

2.2.2.2 Serial Line Cable Lengths – The maximum length of the serial line cables that connect from the PDT-11/150 to the terminals is 15.24 meters (50 feet).

2.3 SERIAL LINE DATA CHARACTERISTICS

The baud rate and character parameters of the serial line data transferred between the devices and terminals and the PDT-11/150 must be compatible. Refer to Chapter 5 for the initial data conditions and for the data parameter programming information.

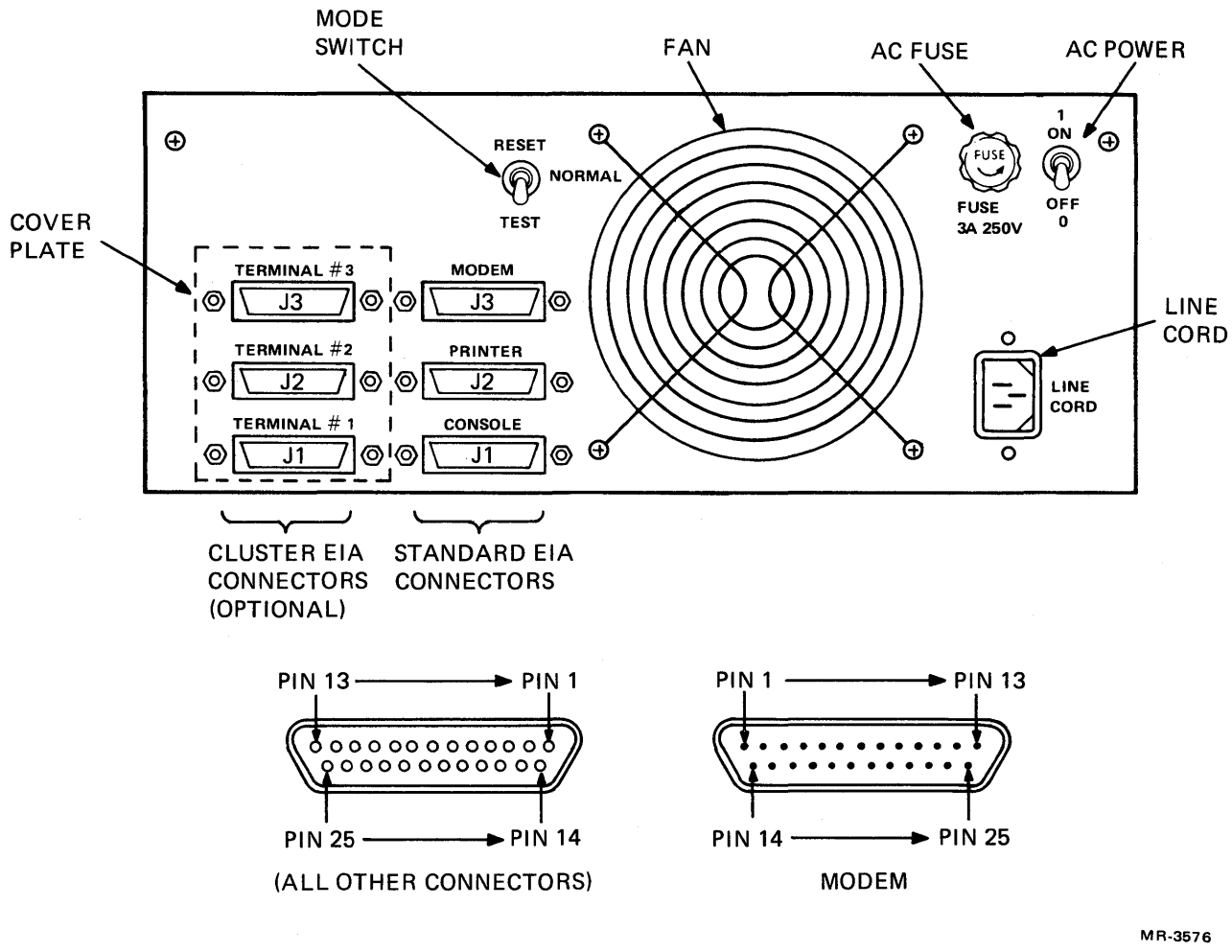


Figure 2-3 Rear Panel Assembly, Component and Connector Locations

Table 2-2 Rear Panel Device Connector Assignments
EIA Connections

Standard	Cluster
Modem (J3)	Terminal 3 (J3)
Printer (J2)	Terminal 2 (J2)
Console (J1)	Terminal 1 (J1)

Table 2-3 Available Device Cable Assemblies

Cable No.	Cable Length	Connector	Cable Type	Connector
BC05C-25	7.62 m/25 ft	H856*	Round 25 conductor	RS-232 (male)
BC05C-50	15.24 m/50 ft	H856*		RS-232 (male)
BC05D-10	3.04 m/10 ft	RS-232 (male)		RS-232 (female)
BC05D-25	7.62 m/25 ft	RS-232 (male)		RS-232 (female)
BC22A	3.04 and 7.62 m/ 10 and 25 ft	RS-232 (female)	Round 6 conductor (including shield)	RS-232 (female)
BC22B	3.04 and 7.62 m/ 10 and 25 ft	RS-232 (male)	Round 14 conductor (including shield)	RS-232 (female)

* H856 is a 40-contact female connector

Table 2-4 Standard EIA Connector Signals

Connector Pin	Signal Designation	Device
J1 (female)		*Console Terminal*
		DIGITAL-type:
2	Term Xmit Data	LA34 DECwriter IV
3	Term RCV Data	LA36 DECwriter II
20	Term RDY	VT50 DECscope
1	Chassis GND	VT100 video terminal
7	Signal GND	LA120 DECwriter III
		LS120 DECwriter III
		VT52 DECscope
J2 (female)		*Printer Terminal*
		DIGITAL-type:
2	LP Xmit Data	LA35 DECwriter II
3	LP RCV Data	LA36 DECwriter II
20	LP RDY	LA180 DECprinter
1	Chassis GND	LA34 DECwriter II
7	Signal GND	LA120 DECwriter III
		LS120 DECwriter III
J3 (male)		*Modem*
		Bell System type:
2	Modem RCV Data	103, 113, 202, 212,
3	Modem Xmit Data	or equivalent
12	SEC Carrier Detect	
5	PRI CTS	
22	Ring Indicator	
8	Carrier Dectect	
6	Data Set RDY	
11	SEC RTS	
4	PRI RTS	
20	DTR	
17	SYN CLK R	
15	SYN CLK T	
1	Chassis GND	
7	Signal GND	

Table 2-5 Cluster EIA Option Connector Signals

Connector Pin	Signal Designation	Device
J1 (female)		*Printer/Video Terminal*
		DIGITAL-type:
2	Term 1 Xmit Data	LA36 DECwriter II
3	Term 1 RCV Data	VT50 DECscope
20	Term 1 RDY	VT52 DECscope
7	Signal IN (GND)	LA34 DECwriter IV
1	Chassis IN (GND)	VT100
		LA120 DECwriter III
		LS120 DECwriter III
J2 (female)		
2	Term 2 Xmit Data	
3	Term 2 RCV Data	Same as J1 terminal
20	Term 2 RDY	
7	Signal IN (GND)	
1	Chassis IN (GND)	
J3 (female)		
2	Term 3 Xmit Data	
3	Term 3 RCV Data	Same as J1 terminal
20	Term 3 RDY	
7	Signal IN (GND)	
1	Chassis IN (GND)	

CHAPTER 3
OPERATING PROCEDURES

This chapter provides detailed operator information, including the function of the switches and indicators, the procedure used to load a disk into a disk drive, and the procedure used to initiate the self-test diagnostic program. This diagnostic program should be performed periodically to check that the unit is operating properly. If a malfunction is indicated during the performance of the self-test, refer to Chapter 5 for the servicing information.

3.1 SWITCHES AND INDICATORS

The front panel indicators and the switches on the rear panel provide the controls used during the self-test programs. The console terminal display and keyboard are also used in conjunction with the controls and indicators.

3.1.1 Front Panel Indicators

The front panel is located at the front of the unit on the top cover. Figure 3-1 shows the four indicators and Table 3-1 lists and describes the function of each.

3.1.2 Rear Panel Switches and Components

The panel mounted at the rear of disk drive 0 contains the ac power switch, fuse, receptacle, fan, and mode switch. Table 3-2 lists the functions of the switches and fuse. Refer to Paragraph 2.2.2 for a description of the 25-pin connectors and the associated devices.

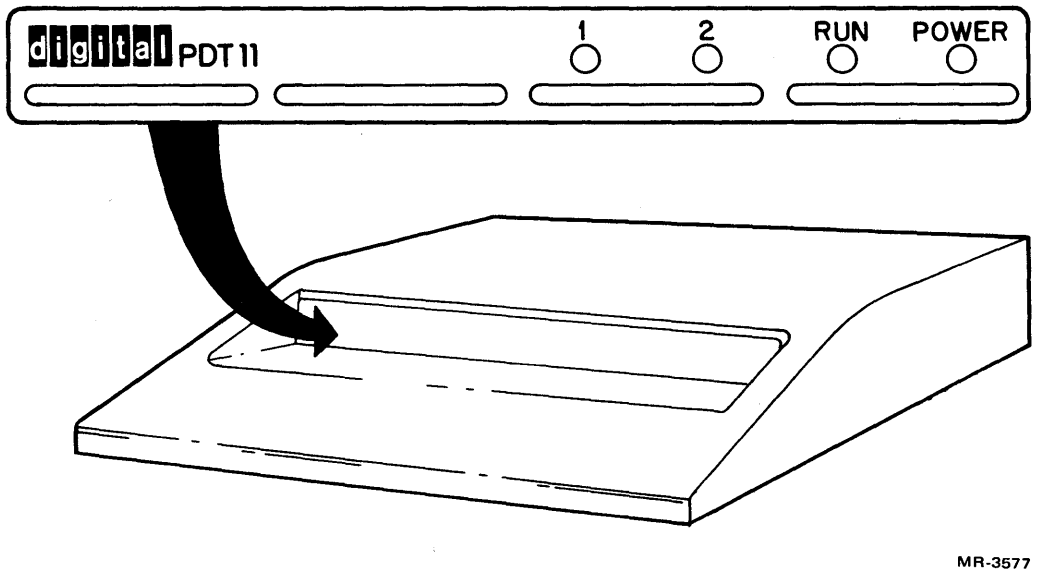


Figure 3-1 Front Panel Indicators

Table 3-1 Front Panel Indicators

Designation	Description
1	Lights to indicate a system error when in the self-test mode. During programmed operation, this indicator can be controlled by the user.
2	Lights to indicate that the system is waiting for an autobaud response from the console terminal; occurs when ac power is applied to the unit or when the mode switch is momentarily set to the RESET position and released during either program operation (NORMAL) or self-test mode. The autobaud function can be disabled by switch S1-1 (Table 3-4). During programmed operation, it can also be controlled by user program.
RUN	Lights to indicate that the LSI-11 microprocessor is executing instructions.
POWER	Lights to indicate that the +5 V dc is present in the unit.

Table 3-2 Rear Panel Switches and Fuse

Item	Function
ac power (toggle switch)	Up position ON (1) – applies ac power to the PDT-11/150.
Fuse 3 A 250 V	ac power fuse
Mode (toggle switch)	Three positions:
RESET	Up position (momentary) – Initializes the PDT-11/150 system by clearing registers and logic.
NORMAL	Center position (latch) – Allows normal program operation of the PDT-11/150.
TEST	Down position (latch) – Initiates diagnostic testing of the PDT-11/150 system and allows the BREAK key detection from the console terminal keyboard.

3.1.3 Function Switch

The PDT-11/150 contains an internal switch pack S1 used to select specific conditions both during program operations and during test functions. The switch pack is mounted on the Peripheral module and can only be accessed by removing the top cover of the unit. When the unit is shipped, the switches are set to the positions shown in Table 3-3. Table 3-4 lists and describes all five switch functions. To remove the top cover assembly, perform the procedure in Paragraph 5.3.1.1. Figure 5-27 shows the location of the function switch.

Table 3-3 Function Switch Positions During Self-Test

Switch No.	Position	Function
1	OFF	Console terminal autobaud enabled
2	ON	Line time clock interrupt disabled
3	OFF	Dynamic RAM refresh enabled
4	ON	Self-test function of mode switch enabled
5	OFF	Manufacture mode disabled

Table 3-4 Function Switch Selections

Switch No.	Function
1 Auto Baud	OFF position – Enables the autobaud function, which allows the PDT-11/150 to monitor the baud rate of the console terminal and select the same baud rate for the console terminal interface. During normal, maintenance (refer to switch no. 5), and test mode, when LED no. 2 lights on the indicator panel the operator is required to press the @ key of the console keyboard two consecutive times. When the baud rate is established, the LED no. 2 light will go off. ON position – The PDT-11/150 defaults to a console baud rate of 9600. In either the ON or OFF position, the PDT-11/150 assumes the transmit/receive character to be eight bits, no parity, and one stop bit (two stop bits for the 110 baud rate only).
2 Line Time Clock	OFF position – Enables the internal line time clock to generate an event program interrupt every 16.6 ms to the LSI-11 microprocessor. When performing the system exerciser program, this switch must be in the OFF position. ON position – Disables the line time clock to inhibit the event program interrupt.
3 Dynamic Memory Refresh	OFF position – Enables the LSI-11 dynamic RAM memory to be refreshed every 1.0 ms. ON position – Disables the dynamic RAM memory function.
4 Test Mode	OFF position – Prevents the self-test mode from being selected by the mode switch on the rear panel of the PDT-11/150. (Refer to Table 3-2). ON position – Allows the self-test mode to be selected by the mode switch on the rear panel.
5 Manufacture Mode	OFF position – Disables the manufacture mode, requiring operator response from the console keyboard during performance of the self-test functions. (Refer to Paragraph 3.3.2). ON position – Enables the manufacture mode, which eliminates the requirements of operator response from the console keyboard during the performance of the self-test functions.

3.2 DISK HANDLING AND STORAGE

The flexible disk used to store data and programs in the PDT-11/150 is shown in Figure 3-2. The oxide-coated disk is enclosed in a square plastic envelope. Precautions must be taken when handling and storing disks to prevent the loss of data or the creation of erroneous data and to ensure maximum operating life. The following practices are recommended.

1. To avoid touching the oxide surface of a disk, handle the disk by the envelope.
2. Write all disk identification on a label before affixing the label to a disk's envelope.
3. Do not apply solutions or chemicals to a disk's surface or its envelope.
4. Do not attach clips or rubber bands to disk envelopes.
5. Do not place heavy objects on a disk.
6. Do not subject disks to sharp objects or magnetic fields.
7. Do not use disks that are bent or mutiliated.
8. Do not remove the oxide-coated disk from its envelope.
9. Store disks in a box or contaminant-free enclosure.
10. Do not expose disks to direct sunlight or excessive heat.

Insertion and Removal of a Disk – Perform the following procedures to load and remove a disk from the disk drive. Refer to Figure 3-2.

CAUTION

Do not install or remove a disk when the disk drive is performing read or write operations. Withdraw all disks from the disk drives before applying the ac power to the unit or removing the ac power from the unit.

1. With the disk drive cover closed, grasp the center of the disk cover handle and press the release lever. The cover is spring-activated and will rise to the open position when the latch is released.

2. Hold the disk in the position shown with the read/write head aperture closest to the disk drive opening.

NOTE

The index hole aperture must be located left side the disk center's line as shown. If the hole is on the opposite side, turn the disk over.

3. Insert the disk fully into the disk drive opening.

4. Press down on the top of the cover handle until the cover closes and remains in the latched position.

5. To remove the disk, perform step 1, slide the disk gently from the drive unit and close the cover as described in step 4.

3.3 TEST PROCEDURES

The following procedures are used to initiate the self-test diagnostic programs stored within ROM memory of the PDT-11/150. These procedures verify the correct operation of the disk drive and logical components within the unit. When the diagnostic tests have been successfully completed, the PDT-11/150 system exerciser program (CVKDAB0), contained on disk, may be initiated to further evaluate the performance of the unit. Refer to Chapter 5 for information related to the system exerciser.

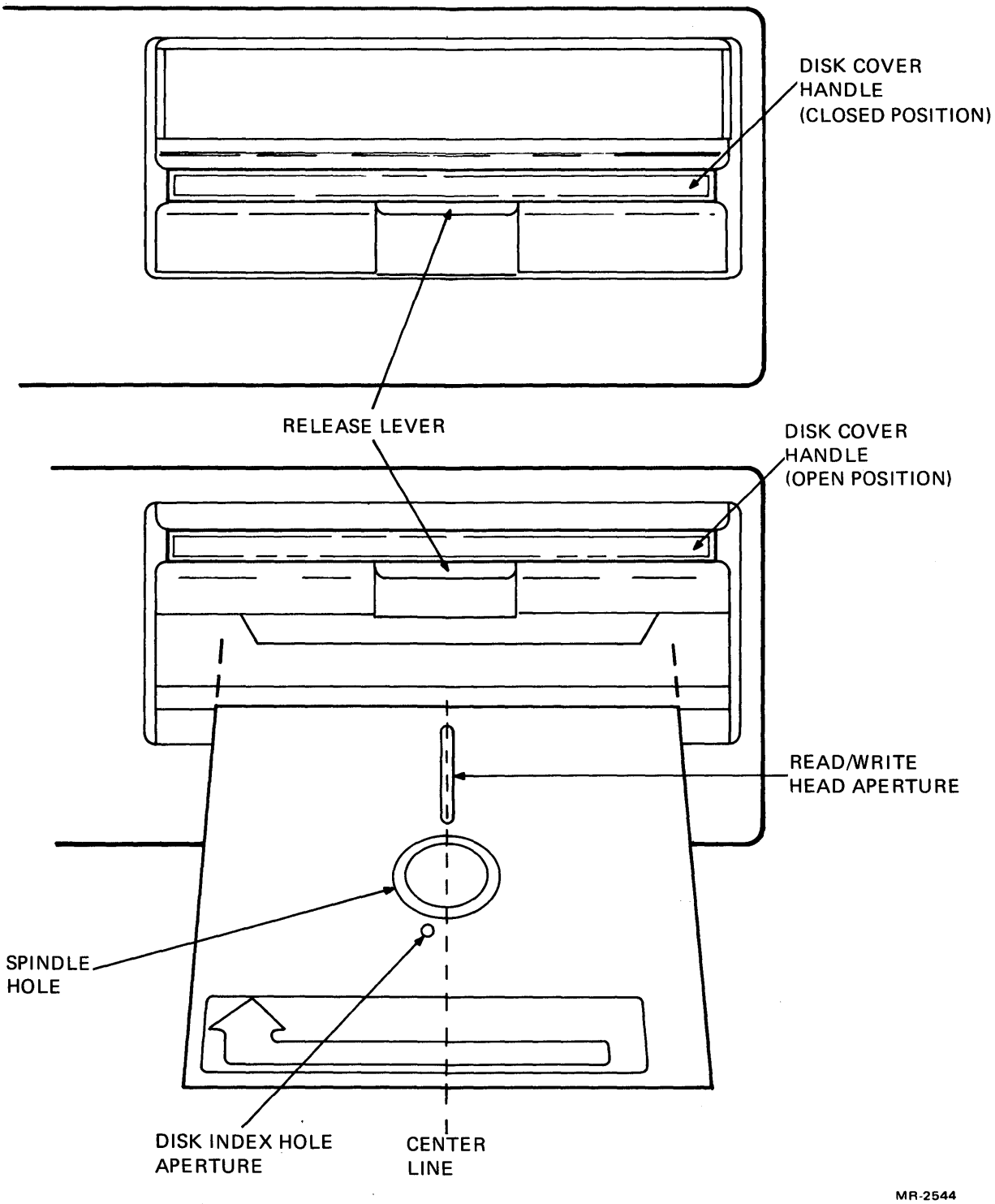


Figure 3-2 Loading the Disk into the Disk Drive

3.3.1 Preliminary Setup

Prior to initiating the self-test procedure, ensure that the following conditions exist.

1. The ac power cord is connected.
2. The console device and terminals are connected to the PDT-11/150 and to the ac power (see Paragraph 2.2.2).
3. The function switches are set to the positions indicated in Table 3-3.
4. The ac power switch (see Figure 2-3) on the rear panel of the unit is in the OFF (0) position.
5. The mode switch (see Figure 2-3) on the rear panel is in the TEST position (down).
6. No blank or programmed disks are installed in the drive(s).

3.3.2 Optional Loopback Connector

The self-test procedures and system exerciser program includes the facility for testing serial data transfers through the standard EIA connectors (except the console) and the Cluster EIA connectors. The loopback connector assembly is available as an option (DEC No. 7016464) and must be attached to the connectors on the rear panel as shown in Figure 3-3. Remove all terminal cable connectors on the rear panel except the console terminal connector if the loopback test function is desired.

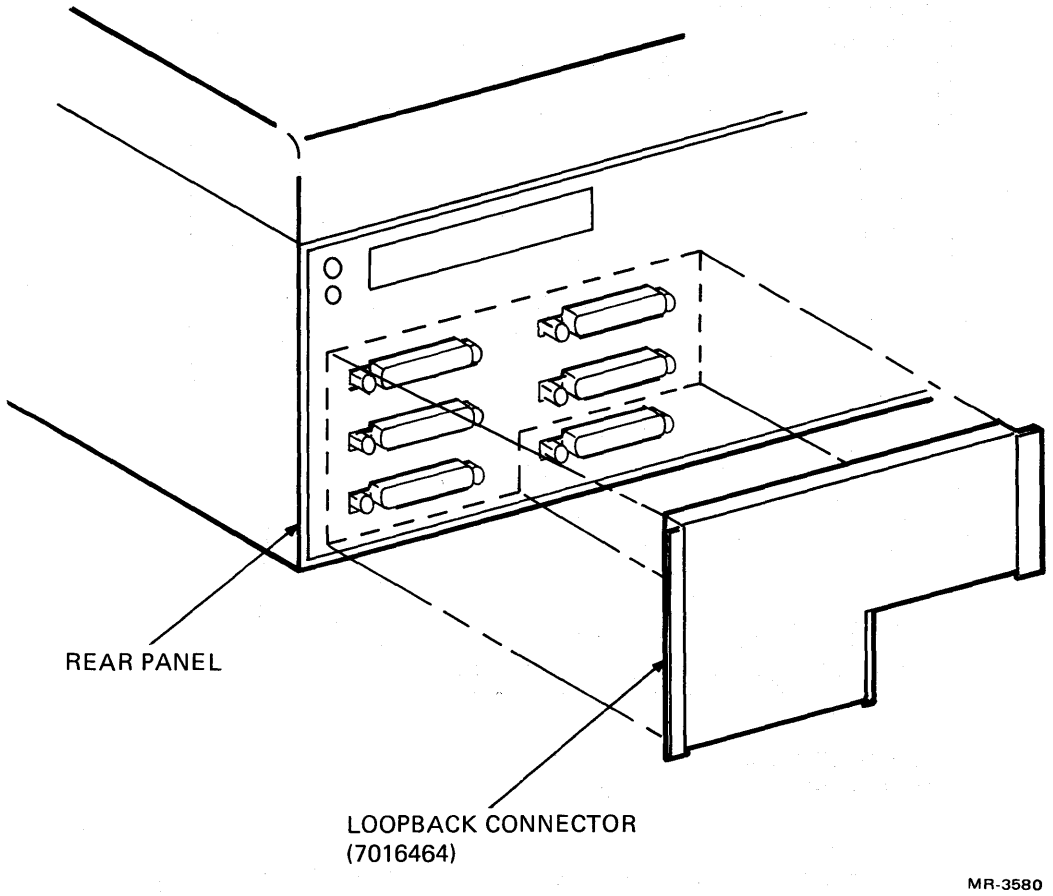


Figure 3-3 Loopback Connector Installation

3.3.3 Self-Test Procedures

Perform the following procedures in the sequence indicated. If a failure is detected during the performance of this test, one or more of the following events will take place.

1. The error indicators (1) on the front panel will light.
2. An improper response to the test procedure will occur.
3. No response will occur when a response is indicated by the test procedure.

If the self-test diagnostic does not run successfully during the initial test, repeat the procedure a minimum of three times. The function switches must be set to the positions indicated in Table 3-3.

1. Set the ac power switch to the ON (1) position.

NOTE

All indicators on the front panel, except the RUN indicator, will light initially when the ac power is applied. This confirms that the indicators are operative.

2. The power indicator on the front panel will remain lighted.

3. When the (2) indicator on the front panel remains lighted, press the @ symbol key on the console terminal keyboard twice. If there is no response, press the @ symbol key again.

NOTE

Some terminal keyboards may require that the SHIFT key be pressed when typing the two @ symbols.

4. The (2) indicator will be extinguished. This procedure establishes the baud rate of the PDT-11/150 to be compatible with the console terminal. The console terminal will respond by displaying the following message:

   SCRATCH FLOPPY INSTALLED?

5. Open the front cover of disk drive 0 and insert a scratch disk. Refer to Paragraph 3.2.1 for disk insertion. In a dual drive unit, insert a scratch disk in each drive.

NOTE

Scratch disks are preformatted blank disks or disks with data no longer required.

6. Type **Y** on the console terminal when the disks are properly installed. This indicates a "yes" to the question.

NOTE

This initiates the read/write test of the disk. The disk controller module will write and read information from selected tracks. In a dual disk drive unit, disk 0 will be exercised first, followed by disk 1. Allow approximately two minutes for the complete disk test.

7. If **N** is typed to indicate "no," the disk drive exercise part of the self-test will not be performed. The console terminal will respond by displaying the following message:

   EIA LOOPBACK TEST?

8. To run the EIA loopback test, the loopback connector assembly must be installed on the rear panel (see Paragraph 3.3.2). Disconnect all terminal cable connectors from the rear panel except for the console terminal connector and attach the loopback connector. Type **Y** indicating "yes" on the console keyboard after the connector is attached. Type **N** indicating "no" if the loopback test is not desired.

9. After successful completion of this test, the console terminal will respond by displaying the following message:

   XXXXXX (the six digits can be of any value)
   @

10. To initiate the LSI-11 microprocessor test and RAM module test, set the mode switch to the RESET position and release to the NORMAL position.

11. When the (2) indicator on the front panel remains lighted, press the @ symbol key on the console terminal twice.

NOTE
Some terminal keyboards may require that the SHIFT key be pressed when typing the @ symbols.

12. The (2) light will be extinguished and the RUN indicator will light. After a short delay, the following message will be displayed on the console terminal.

   NO BOOT ON VOLUME
   TYPE START UNIT NUMBER (0 OR 1):

13. The PDT-11/150 has successfully completed the self-test diagnostic. If it is desired that a program disk or system exerciser disk be loaded, remove the scratch disk and insert the appropriate programmed disk into drive 0 or 1.

NOTE
In a dual disk drive unit, the programmed disk may be inserted into either drive 0 or 1 and the scratch disk previously inserted can remain installed in the other disk drive.

3.3.4 Loading a System Program

A program disk can be initially loaded into the PDT-11/150 by the following procedures.

1. Check to ensure that no disks are installed in the disk drive(s).

2. Set the mode switch on the rear panel to the NORMAL position (center).

3. Apply power to the console device.

4. Set the power switch on the rear panel to the ON (1) position.

NOTE
All indicators on the front panel, except the RUN indicator, will light momentarily when the ac power is applied. This confirms that those indicators are operative.

5. The POWER indicator will remain lighted and the (2) indicator will again light.

6. Insert the program disk in disk drive 0. In a dual disk unit, disk drive 0 is located above disk drive 1.

7. If the application program requires data storage on disk drive 1, insert a preformatted scratch disk into disk drive 1 of the dual drive unit.

8. Press the @ symbol on the console device twice.

NOTE
Some consoles may require that the SHIFT key be pressed while typing the @ symbols.

9. The console will display the program title and contents for user selection.

3.3.5 Changing a System Program

If the PDT-11/150 is presently operating and the program disk must be changed, perform the following procedures.

1. Remove the disk in disk drive 0 and insert the program disk to be loaded.

2. Set the mode switch momentarily to the RESET position and release to NORMAL position.

3. When the (2) indicator on the front panel lights, press the @ symbol key on the console keyboard twice. If there is no response, press the @ symbol key again.

NOTE
Some consoles may require that the SHIFT key be pressed while typing the @ symbols.

4. The console will display the program title and contents for user selection.

CHAPTER 4
TECHNICAL DESCRIPTION

This chapter contains a technical description of the overall operation of the PDT-11/150 and detailed descriptions of the logic and signal flows of the modules, disk drives and power supply. References are made to the information contained in the DIGITAL *Microcomputer Processor Handbook 1978–79* and to the *Intel M65-85*[TM] *User's Manual*. The circuit schematics for the modules and power supply are referenced in this chapter and listed in Table 1-8.

4.1 GENERAL OPERATION

Figure 4-1 is a simplified diagram that shows the main functional elements of the PDT-11/150 and their relationships to each other. The main system consists of the following.

1. Intelligence module (KDT11)
2. RAM module (MST11)
3. Peripheral module (DLT11)
4. Standard EIA module (DFT11-AA)
5. Cluster EIA module (optional) (DFT11-AB)
6. Disk drive 0 assembly (RX01)
7. Disk drive 1 assembly (optional) (RX01)
8. Power supply assembly (H7833)
9. Disk Controller module (RXT11)

4.1.1 Intelligence Module (KDT11)

The Intelligence module (KDT11) is the main controlling element within the PDT-11/150; it communicates with the RAM module, Disk Controller module and Peripheral Module. The Intelligence module contains the LSI-11 16-bit microprocessor, which consists of four 40-pin integrated circuits. The LSI-11 is the user-programmable processor and operates similarly to the DIGITAL PDP-11 series of processors. This microprocessor contains the Octal Debugging Technique (ODT) program stored in ROM. ODT provides the user access to internal registers and RAM locations.

An 8-bit I/O microprocessor is also included on the module to simulate the standard I/O device interface normally used with the LSI-11 microprocessor system. The I/O microprocessor operates with firmware stored within a 6K × 8-bit ROM and uses a 256 × 8-bit RAM as a scratch pad memory. Communication between the I/O microprocessor and the LSI-11 is through the Inter-Processor Link (IPL) circuits.

Five LED indicators are mounted on the module and are used during the self-test mode to indicate the octal number of the test being performed.

[TM] MCS-85 is a trademark of the Intel Corporation.

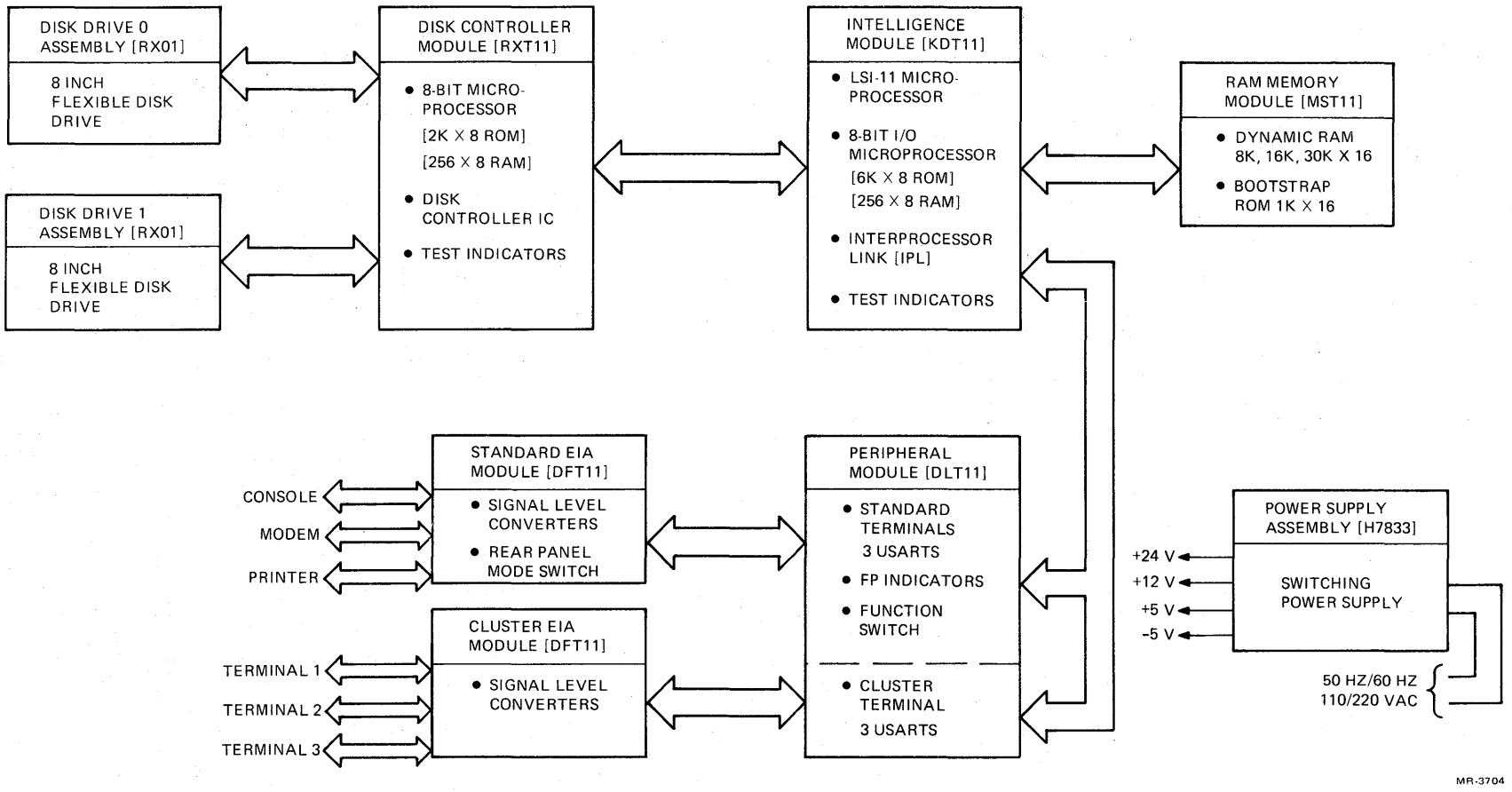


Figure 4-1 PDT-11/150, Simplified Block Diagram

4.1.2 RAM Module (MST11)

The memory module (MST11) contains 8K, 16K or 30K 16-bit words of dynamic MOS RAM for storage of the operating system software or user application programs. The module also includes a 1K × 16-bit ROM that contains a bootstrap loader program for loading the operating or application program from a disk into the RAM. The RAM and ROM are resident memories for the LSI-11 microprocessor on the Intelligence module. The RAM is refreshed every 1.0 ms under control of the LSI-11.

4.1.3 Peripheral Module (DLT11)

The Peripheral module (DLT11) contains three universal synchronous/asynchronous, receiver/transmitter (USARTs) integrated circuits. The USARTs convert the parallel data from the PDT-11/150 to serial data for transmission to the I/O devices, and serial data to parallel data for transmission to the PDT-11/150. The USARTs also contain status registers that are accessible by the 8085 microprocessor on the Intelligence module and control registers that allow program selection of the USART parameters. One USART is used for the console terminal, one for the communication modem and one for the line printer.

Three additional USARTs are installed on the module when the Cluster EIA option is added to the PDT-11/150 unit. The Cluster EIA option will support three additional I/O devices. The Peripheral module communicates with the I/O devices through the level converters on the Standard EIA and Cluster EIA modules.

The module also contains the front panel indicator lights and a 5-section function switch that permits the selection of the internal test and control functions.

4.1.4 Standard and Cluster EIA Modules (DFT11)

The Standard and Cluster EIA modules (DFT11) provide the converters necessary to make the signal levels between the PDT-11/150 and the peripheral devices compatible. Mounted on each module are three 25-pin connectors, one for each I/O device cable. The Standard EIA module also contains the rear panel mode switch used to select normal, reset and test mode operations.

4.1.5 Disk Controller Module (RXT11)

The Disk Controller module (RXT11) contains the digital and analog circuits required to read or write on the flexible 8-inch disks used. The module contains an 8085 8-bit controller microprocessor which is programmed by the microcode stored in a 2K × 8-bit ROM. Data to be written or read on a disk is stored within a 256 × 8-bit RAM used as a data buffer. The formatting of disk data is performed under the control of the FD 1771 disk controller IC, which senses and selects the read/write head position and locates the track and sectors of a disk where the data will be read or written. The disk data formats are compatible with an IBM 3740 data entry system. The module also contains four LED indicators which are used during the self-test mode of the PDT-11/150 to specify the octal number of the test being performed.

4.1.6 Disk Drive Assembly (RXT01)

The disk drive 0 and disk drive 1 assemblies provide the mechanical and electrical components necessary to read or write on the 8-inch flexible disk. The assembly consists of a disk drive motor to rotate the disk, a read/write head and head positioning motor, and electrical sensors to determine the head position in relation to track and sector information on a disk. A head load solenoid raises and lowers the read/write head from the surface of the disk. The disk is inserted into the disk drive by releasing the cover on the front of the assembly.

4.1.7 Power Supply Assembly (H7833)

The H7833 power supply assembly provides +24 V, +12 V, +5 V and −5 V regulated dc voltages to the modules and disk drives of the PDT-11/150 unit. The power supply operates on the switching principle and receives an input line ac voltage of 115 V RMS or 230 V RMS at a frequency range of 47 to 63 Hz.

4.2 PDT-11/150 BUS STRUCTURE

The PDT-11/150 contains several busses that are used to transfer data, address, and control information between the logic circuits on the modules and between the modules themselves. Figure 4-2 (Sheets 1–3) shows the busses used and the distribution of the bus lines to the functional elements.

The LSI-11 microprocessor on the Intelligence module uses the WMIB 00–21 L bus for information transfers between the logic circuits associated with the LSI-11. Refer to the DIGITAL *Microcomputer Processor Handbook 1978–79* for a description of the microinstruction bus. The LSI-11 microprocessor communicates with both the Inter-Processor Link (IPL) on the same module and with the RAM and ROM on the RAM module through the WDAL bus. The first four lines are buffered by the LSI-11 bus drivers and become lines BWDAL 00 H–03 H. These lines and WDAL 04 H–15 H are distributed to the IPL and address register on the Intelligence module and to the RAM, ROM and memory buffer register of the RAM module. All data to and from the LSI-11 microprocessor and RAM passes through these lines. The IPL converts the 16-bit information from the LSI-11 into two 8-bit bytes for the I/O microprocessor (on lines BAD 0 H–7 H) and the two 8-bit bytes into 16 bits of information for the LSI-11.

The address register stores only the address information from the LSI-11 on the BWDAL and WDAL lines. The output of the address register is on the ADR 00 H–15 H lines. The address information on lines ADR 00 H–15 H is distributed to the RAM module. The information on lines ADR 01 H–12 H is decoded by the row/column multiplexer and lines ADR 12–15 H are used to select the memory bank of the dynamic RAM. The ADR 01 H–10 H lines also provide address information to select locations in the bootstrap ROM. The RAM module includes an internal bus M 00 H–15 H used to transfer data between the dynamic RAM and the memory data buffer.

The ADR bus also connects to the I/O device address decoders (on the Intelligence module) which will generate an interrupt request to the 8085 microprocessor when an I/O device or disk drive is addressed.

The low byte of the address information from the I/O microprocessor and the 8-bit data to and from the I/O microprocessor are transferred through lines AD 0 H–7 H. The high byte of the address information is transferred on lines A 8 H–15 H. Lines AD 0 H–7 H are distributed to the I/O port and RAM IC, and provide data, status and address information between the I/O microprocessor and the I/O port and RAM IC. The A 0 H–5 H lines are also decoded by the indicator register to control the LED indicators during self-test operations. The low byte data address lines A 0 H–7 H are buffered by the bus transceivers, which control the data and address transfer direction. The bus transceivers also connect to the HDBAD 0 H–7 H lines, which transfer address information to the I/O devices and disk drives and data and status information to and from the I/O devices and drives. The HDBAD bus connects to another buffer consisting of the bus transceivers.

The low bit address information from the 8085 I/O microprocessor is transferred through both 8-bit bus transceivers and is latched into the low byte address register. The A 0 H–7 H output of the low byte address register and the A 8 H–15 H output from the 8085 are used to select locations within the 6K × 8-bit ROM. The address lines A 0 H and A 11 H–15 H are also decoded by the memory and I/O device select logic to enable one of several discrete lines, which select ROM banks, I/O devices, disk drives and other special functions.

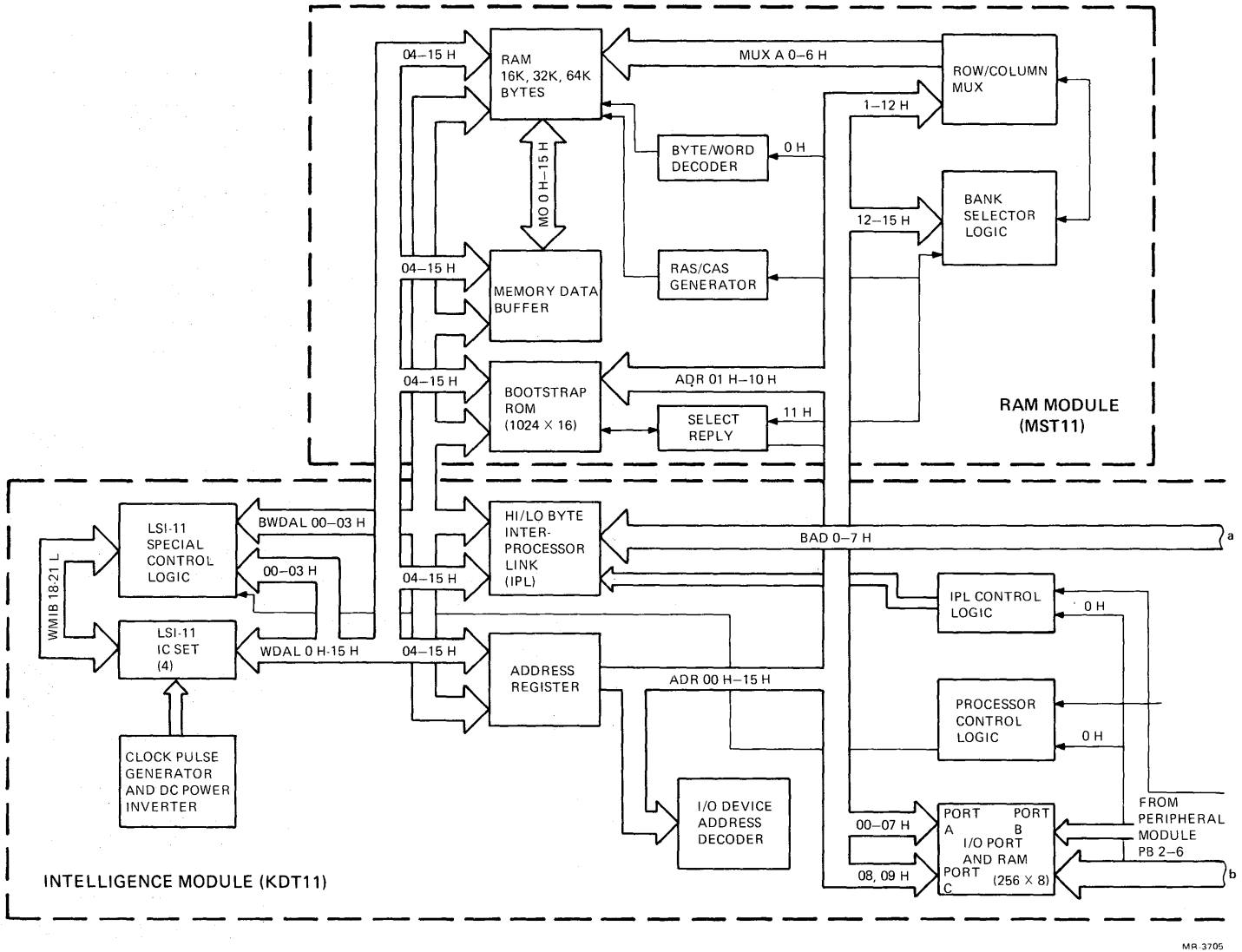


Figure 4-2 PDT-11/150 Bus Structure (Sheet 1 of 3)

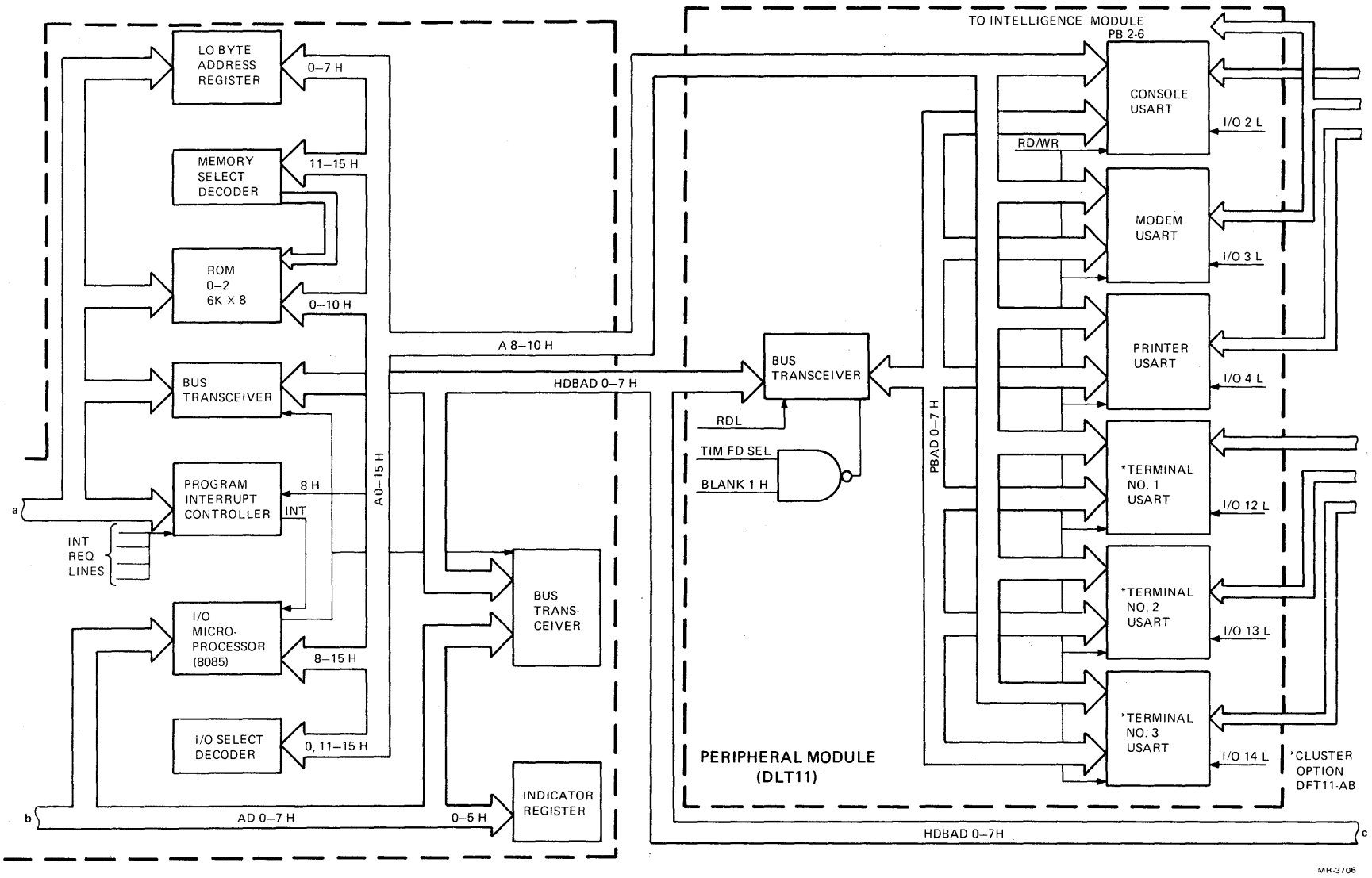


Figure 4-2 PDT-11/150 Bus Structure (Sheet 2 of 3)

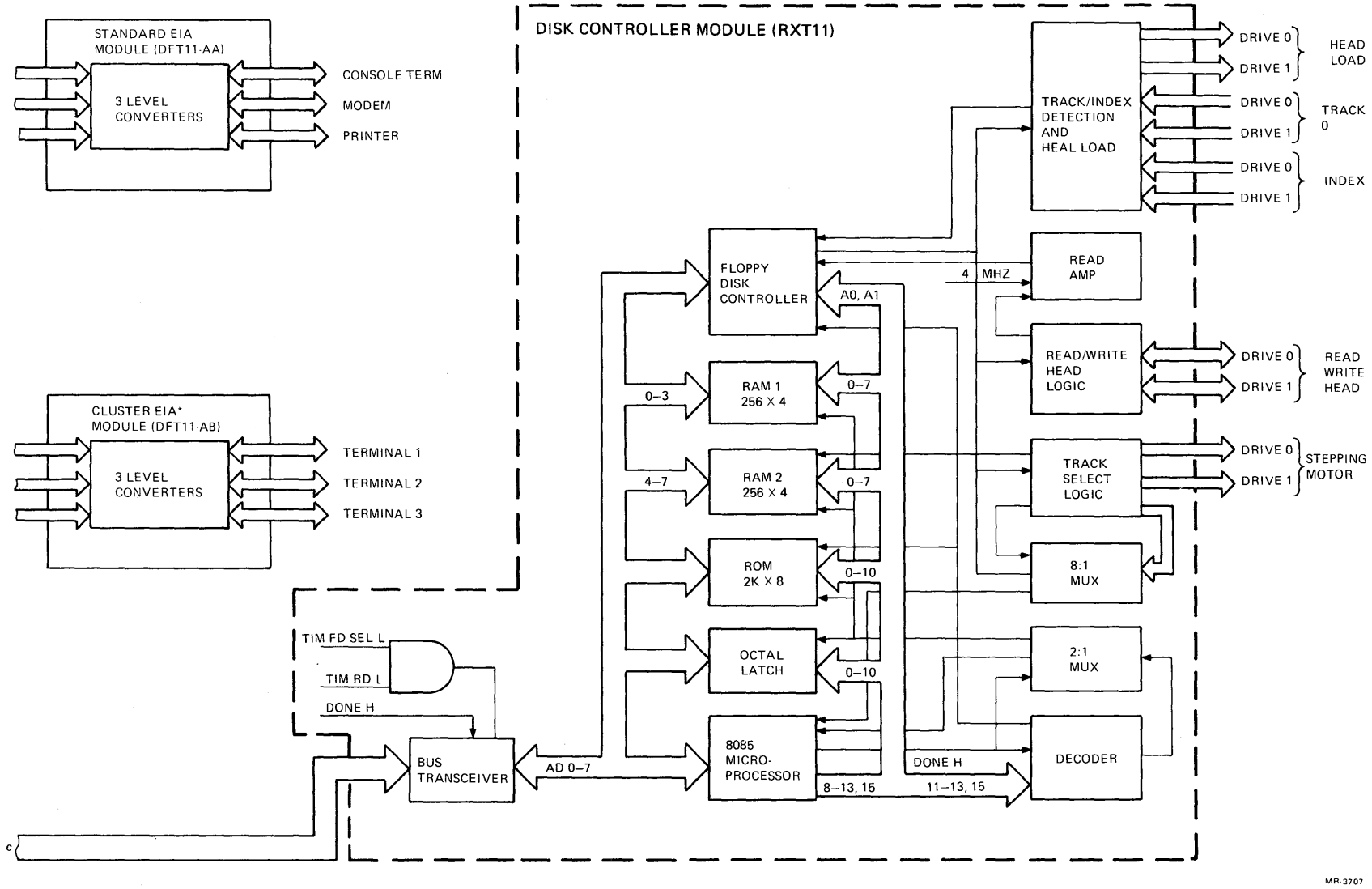


Figure 4-2 PDT-11/150 Bus Structure (Sheet 3 of 3)

Address lines A 8 H–10 H are distributed to the Peripheral module and used to select read or write operations and internal registers within the addressed USARTs. Data status and address information is transferred to and from the Peripheral module and Disk Controller module through the HDBAD bus. The transfer's direction is controlled by the bus drivers on each module. The bus drivers on the Peripheral module are connected to the PBAD 0 H–7 H lines, which are distributed to each of the USARTs. The bus transceivers of the Disk Controller module are connected to the low byte data/address bus lines from the 8085 microprocessor. These lines also transfer data and status information internally to the RAM 1, RAM 2, ROM and to the disk controller IC. Address information from the 8085 is latched into an 8-bit register and distributed internally on lines A 0–7 to the same elements as those to which the AD 0–7 lines are distributed.

4.3 SIGNAL DISTRIBUTION

Figure 4-3 shows the distribution of signals and busses among the individual modules of the PDT-11/150 unit. Refer to Paragraph 4-10 for the signals and voltages transferred between the Disk Controller module and the disk drive 0 and 1 assembly. Refer to Paragraph 4.8 for the signals transferred between the Standard EIA and Cluster EIA modules and the peripheral devices.

4.4 SYSTEM OPERATION

The LSI-11 16-bit microprocessor contained in the PDT-11/150 is programmed using the standard LSI-11 instruction set. The PDT-11/150 also contains an 8085 I/O microprocessor used to control the I/O data transfers to and from the peripheral devices and the internal disk drives. Figure 4-2 (Sheets 1–3) shows the main functional elements of the modules in the PDT-11/150 unit.

4.4.1 Power-Up Functions

When ac power is initially applied or when the mode switch on the rear panel is momentarily placed in the RESET position, the 8085 I/O microprocessor assumes control of all operations. At power-up time, the 8085 initializes, senses the mode and function switch selections, preselects the baud rates of the console modem and terminal USARTs, and initializes other elements in the system related to the 8085. The 8085 programs are stored in the 6K × 8-bit ROM and the I/O microprocessor has access to a 256 × 8-bit scratch pad RAM in the 8155 I/O port and RAM IC. During power-up the 8085 initializes the stack pointer of the RAM and the 8259 interrupt controller IC. It also clears the system flags and presets the interval timer in the 8155 for a 16.6 ms interval. The modem and printer USARTs on the Peripheral module are also preset by the 8085 to a baud rate of 1200. If the Cluster EIA module is included in the unit, each of the terminal USARTs is preset to a baud rate of 300.

When the autobaud function is enabled by switch S1-1 on the Peripheral module, the 8085 will determine the baud rate of the console and set the parameters of the console USART to the corresponding value. If the autobaud function is disabled, the 8085 will preset the console USART to a 9600 baud rate.

If the Line Time Clock (LTC) is enabled by switch S1-2 on the Peripheral module, the 8085 will enable an event interrupt to the LSI-11 microprocessor to occur every 16.6 ms.

The 8085 also provides an initialize signal to the Disk Controller module to allow the 8085 controller microprocessor to prepare for data transfers. When the normal mode is selected by the mode switch on the rear panel, the 8085 will then disable the interrupts to the LSI-11 and allow it to begin its power-up sequence.

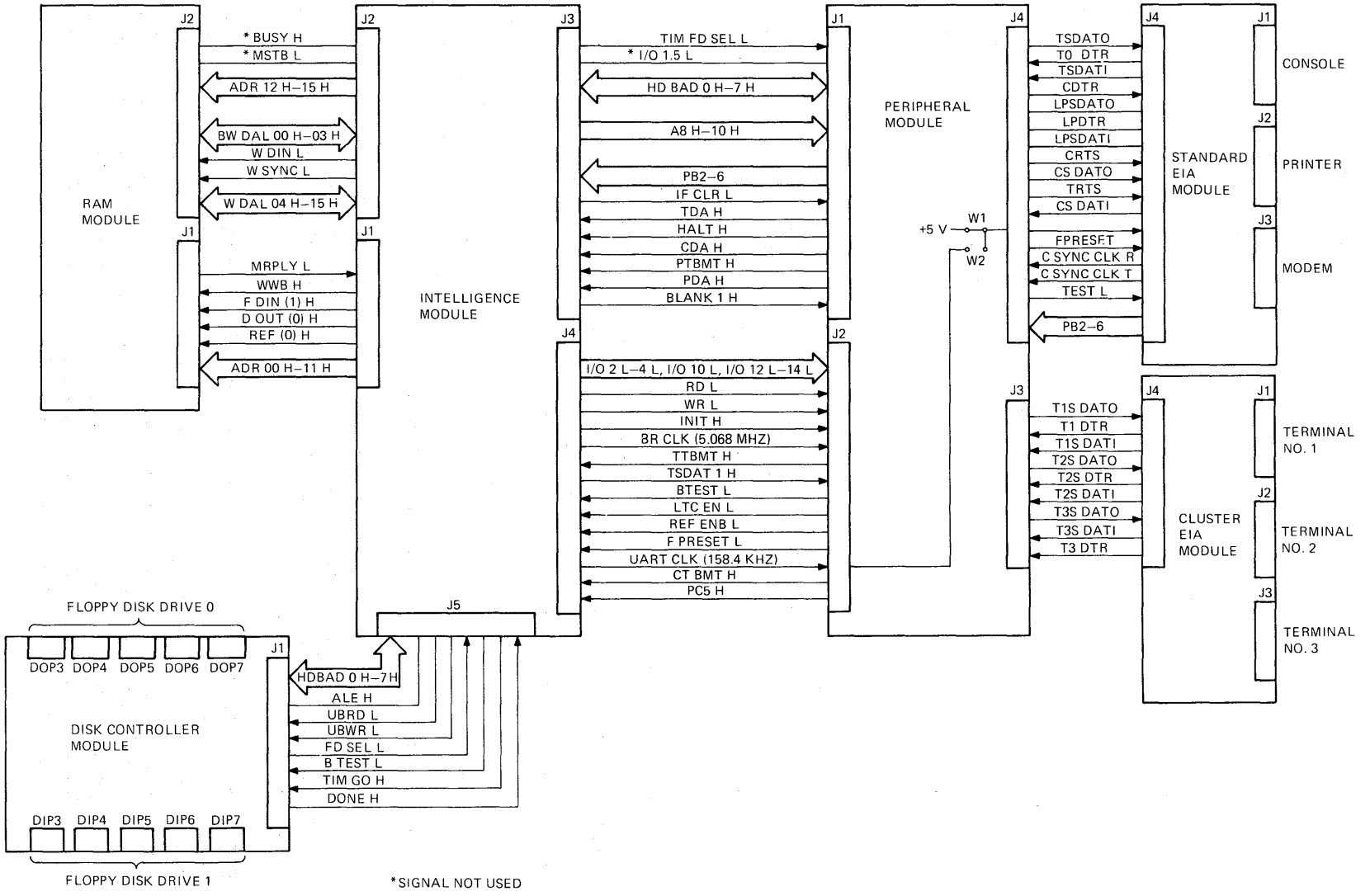


Figure 4-3 PDT-11/150 Internal Signal Distribution

When the mode switch is in the TEST position, the 8085 will perform a self-test of the I/O processor circuits, and a non-media test of the Disk Controller module. It also will allow an EIA loopback test to be selected by an operator and a disk controller test to be selected to read and write on specific tracks of a scratch disk installed in the drive. Upon completion of the self-test, the 8085 will also enable the operation of the LSI-11 in the same manner as it would in the normal mode. During the test mode, LED indicators on the Intelligence module and Disk Controller module will light to indicate the test program sequences; these will remain lighted when a failure occurs. These indications are used to specify malfunctions of cables and modules within the PDT-11/150 unit.

During the power-up cycle, the LSI-11 microprocessor will first initiate a Fast-Data-In cycle to check the condition of the power-up signal from the 8085 and to determine if the self-test mode has been selected by the mode switch. When the normal mode has been selected, the LSI-11 will then access location 173000 in the 1K × 16-bit ROM on the RAM module and perform a memory/instruction test to verify the operation of the microprocessor and memory. If an error is detected during this test, the LSI-11 will print out on the operator's console the memory address where the error occurred. If no errors are detected in the normal mode, the LSI-11 will then attempt to load the program stored on a disk in disk drive 0.

4.4.2 I/O Microprocessor Control

The 8085 I/O microprocessor determines the status of the peripheral devices by periodically checking the status of the I/O device control and status registers (CSRs) or by detecting an interrupt request from the device. The device polling routines are accurately controlled by the timer located in the 8155 I/O port and RAM IC. All peripheral devices, ROM and internal registers are selected by activating unique select lines in conjunction with the various addresses on the 8085 address bus. All data transfers between the 8085 and the LSI-11 are made through the Inter-Processor Link (IPL).

4.4.3 Data Transfer Operations

Data transfers are initiated when the LSI-11 places an address on the LSI-11 data/address bus and activates an input or output operation. Address values below 176000 are decoded to select memory locations in RAM or register and memory locations in the ROM of the LSI-11 IC set. Addresses above 176000 are assigned to peripheral device or disk controller registers and require I/O microprocessor intervention. All valid addresses issued by the LSI-11 require a reply signal to the LSI-11 from the addressed memory or register location. If no reply is received within the specified interval of 1.6 ms, the LSI-11 will time out and then perform a Fast-Data-In cycle to determine if the time-out error was a result of an ac power-up condition, a reset instruction, or a reply not received. The LSI-11 will then either halt operations or jump to a specified routine in RAM.

Addresses issued to an I/O device are decoded by logic and generate one of three interrupt requests to the 8085 I/O microprocessor. One interrupt request is produced from any I/O device address except the disk controller data register. The remaining two interrupts indicate either a read or write command to the disk controller data register.

The interrupt reguests are received by the 8259 interrupt controller and result in a program interrupt of the 8085 I/O microprocessor. The 8085 initiates a routine to determine the device location by examining the low address bits from the LSI-11 through the 8155 I/O port and RAM IC. The 8155 also receives information that specifies read or write and word or byte operations from the LSI-11. The 8085 locates the appropriate device handler routine (stored in the 6K × 8-bit ROM) that is required to service the specific device addressed. Address information from the 8085 is decoded to generate discrete I/O select, memory and disk controller signals, which are used to enable ROM memory locations and I/O devices and to select other functions within the unit.

The LSI-11 communicates with the selected I/O device using four types of transfer operations: Read, Write, Read-Modify-Write and Interrupt Acknowledge.

The read operation, initiated by a read command, transfers information from the addressed memory location or register to the LSI-11. The operation begins with the transfer of a 16-bit address from the LSI-11. Data is transferred to the processor registers from RAM or the device by an input byte or input word instruction. The input byte instruction allows the selection of the upper or lower byte of information.

The write operation is initiated by the write command, which transfers information from the LSI-11 to the addressed memory location or device registers. The operation begins with the transfer of the 16-bit address from the LSI-11. Data is transferred from the LSI-11 processor registers to the RAM or device register by an 8-bit output byte or a 16-bit output word instruction.

The read-modify-write operation performs both a read and write transaction with the memory location or addressed device. It is initiated by a read operation, which transfers a 16-bit address from the LSI-11. The data is transferred from the device to the LSI-11 microprocessor. The sequence is continued with a write operation, which transfers the modified information to the location previously addressed. The information transferred can be either a 16-bit word or 8-bit byte.

The interrupt acknowledge operation allows information to be read from a device register or written to a device register from the LSI-11 using an interrupt polling routine in the 8085. The LSI-11 monitors the interrupt request line from the 8085 and provides an interrupt acknowledge signal to the 8085. The 8085 then transfers a vector address to the LSI-11 through the IPL, which locates the device handler routine stored in the RAM module.

4.4.4 LSI-11 Resident Memory

The RAM module provides 8K (8,192), 16K (16,384) or 30K (30,7620) 16-bit locations as resident memory for the LSI-11 microprocessor, and contains the LSI-11 instruction codes for the PDT-11/150 object program or customer programs. The RAM module also includes a 1K × 16-bit ROM that contains the LSI-11 instruction and memory test and the bootstrap loader program used to load a program contained on the flexible disk. The memory address from the LSI-11 is received on the RAM module address bus and is used to select one of two memory banks and a row and column within the bank. Data to be read from the addressed memory location in RAM is strobed into the memory data buffer and read by the LSI-11. During write operations, data from the LSI-11 data address bus is loaded directly into the addressed memory location.

The bootstrap ROM is enabled by an address from the LSI-11 in the range of 170000 to 173776.

The RAM memory is dynamic and is refreshed every 1.0 ms by microcoded refresh cycles from the LSI-11 microprocessor.

When a ROM or RAM memory address is received, a reply signal is generated by the RAM module to inform the LSI-11 that data has been received or is ready for transmission.

4.4.5 Peripheral Device Interface

The data for all peripheral devices is transferred through the programmable USARTs located on the Peripheral module. Three USARTs are included with all PDT-11/150 models and an additional three can be added as an option. The USARTs convert the serial line data from the level converters to parallel data for the PDT-11/150 and parallel data from the PDT-11/150 to serial line data for the level converters. Each of the USARTs are enabled by a unique select line from an 8085 I/O microprocessor address decoder.

The control and status registers within a USART are selected by three address lines from the 8085.

A bank of five DIP switches is mounted on the module and permits the selection of specific functions, including: console autobaud, LTC interrupts, manufacturing mode, RAM refresh, and self-test mode. The printer USART may also be programmed to light the front panel indicators 1 and 2, located on the Peripheral module.

4.4.6 EIA/TTL Level Converters

The EIA/TTL level converters convert the serial line data signal levels that are transferred between the USARTs on the Peripheral module and the peripheral devices. The signal levels transferred to and from the USARTs are TTL-compatible and the signal levels to and from the peripheral devices are EIA-compatible and defined by the RS-232-C standard. The EIA input levels from the devices are -15 V to +15 V maximum and the EIA output levels to the devices are -5 V to +12 V maximum.

4.4.7 Disk Controller

The Disk Controller module contains an 8085 microprocessor, a 256 × 8-bit RAM, and a 2K × 8-bit ROM. The 8085 is used to control the initialize functions, to initiate the self-test operations and to sequence and control the data transfers between the 8085 microprocessor on the Intelligence module and the flexible disks. All data formatting and track and sector locating is performed under control of the FD1771-1 disk controller IC.

When ac power is applied to the PDT-11/150 and the normal mode of operation has been selected, the 8085 controller microprocessor performs an initialize routine that sets up the stack pointer in RAM and enables the interrupt request system associated with the module. When the power-up sequence is completed, the 8085 will enter the halt state and interrupt the I/O microprocessor to indicate that it is ready for a transfer.

When data is to be written on a disk, or read from a disk, the 8085 I/O microprocessor on the Intelligence module will recognize the halt condition of the 8085 on the disk controller module and will load the control and status information into reserved locations of the disk controller RAM. This RAM contains 256 × 8-bit locations. If a write operation is specified, the 8085 I/O microprocessor will also load the data to be written on disk in the same RAM. After the appropriate locations are loaded, the 8085 I/O microprocessor will initiate an interrupt to the disk controller 8085, specifying a vector address for a handler routine stored in ROM. This routine allows the 8085 to access the locations in RAM where the control and status information from the 8085 I/O microprocessor is stored. The 8085 will then activate the FD1771-1 controller IC and initiate the desired operation.

The disk controller 8085 specifies the read or write operation and selects either disk drive 1 or disk drive 0, and enables the associated stepper motor, read/write heads, head load solenoids, and index hole and track 0 detectors.

The FD1771-1 controller IC provides the stepper motor pulses and the write and erase information to the write head, and monitors the data received by the read heads. It also receives track 0 and index hole information to determine the required head position and to synchronize the reading and writing of information on the disk.

The disk controller ROM also contains the diagnostic self-test program to check the operation of the disk controller module and to verify the reading and writing of data on selected disk tracks. During the self-test, the state of a four-bit binary counter is displayed by LED indicators to provide a visual indication of the test operation when an error is detected.

4.5 INTELLIGENCE MODULE FUNCTIONS (DWG. NO. 5413271)

Figure 4-4 (Sheets 1–3) are signal flow diagrams of the Intelligence module showing the functional elements and controlling signals.

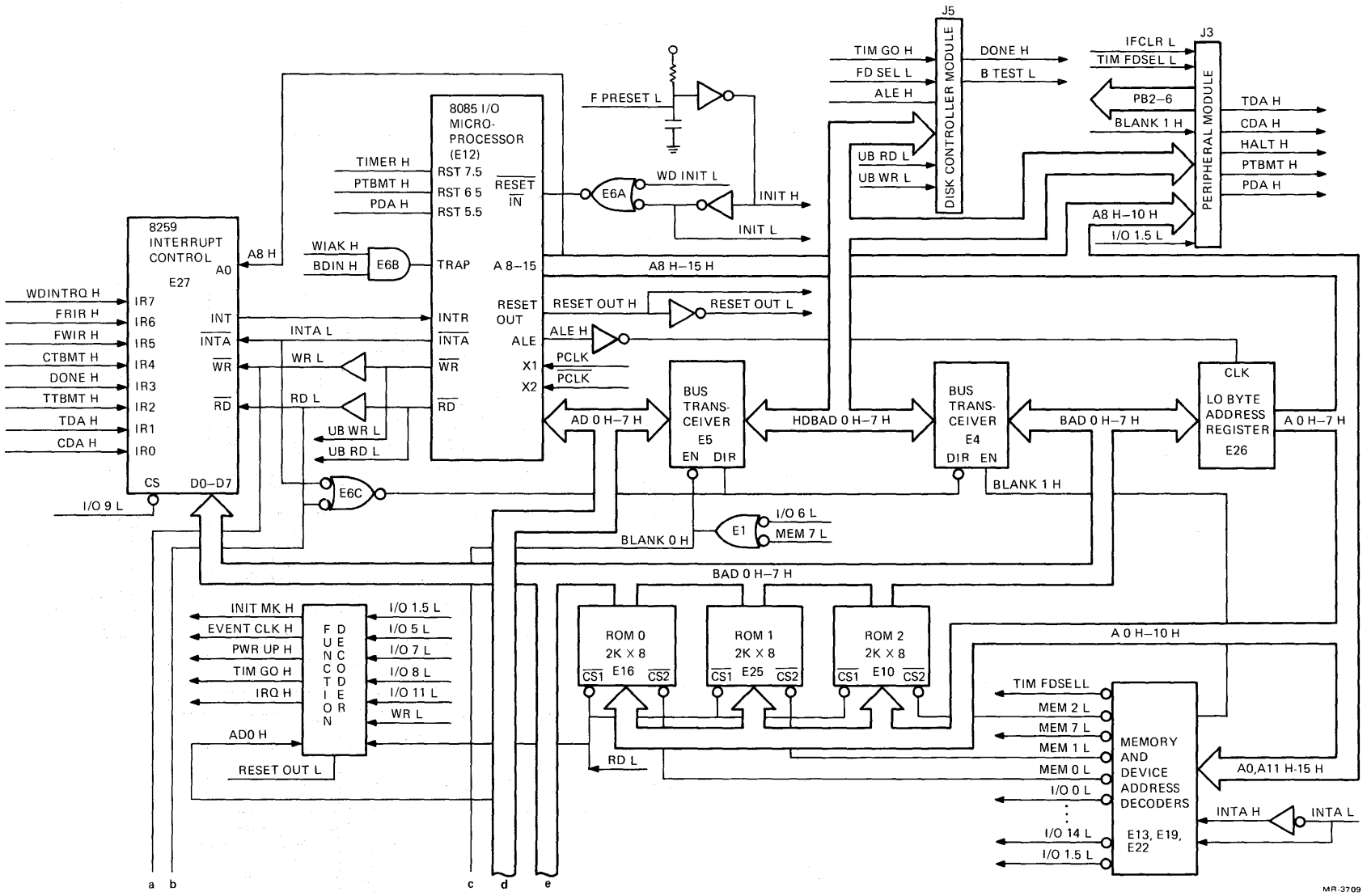


Figure 4-4 Intelligence Module, Simplified Function Diagram
(Sheet 1 of 3)

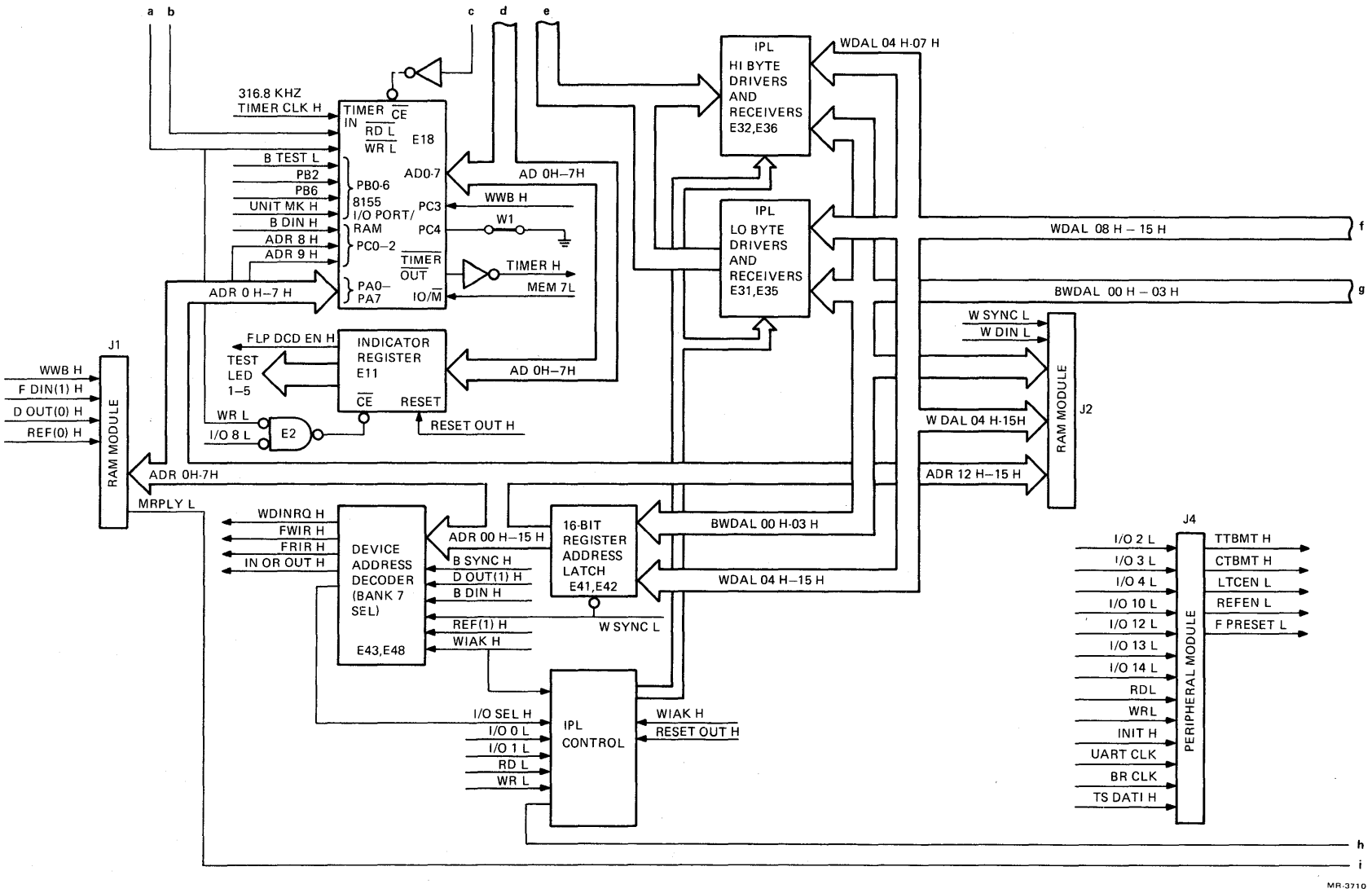


Figure 4-4 Intelligence Module, Simplified Function Diagram
(Sheet 2 of 3)

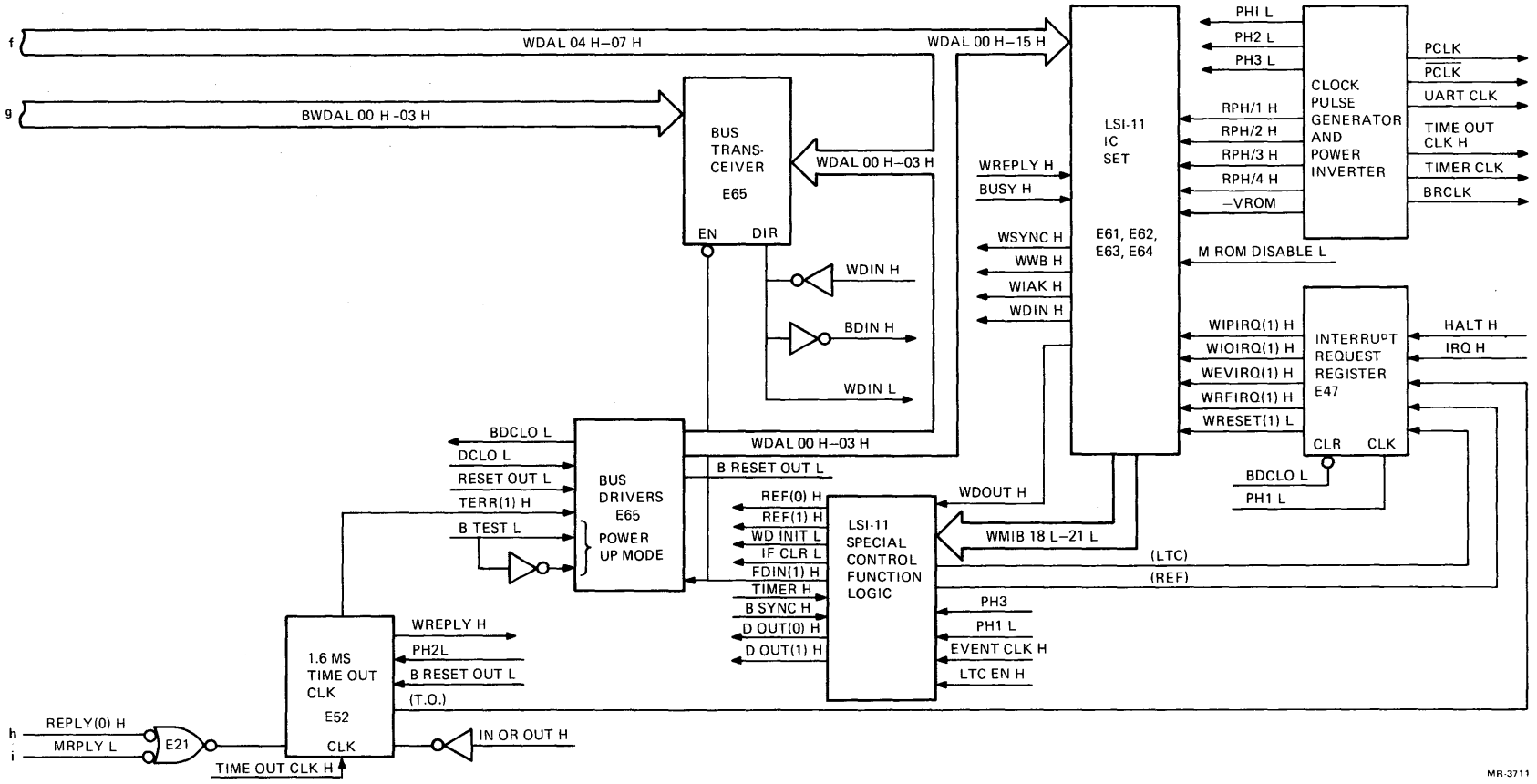


Figure 4-4 Intelligence Module, Simplified Signal Diagram
(Sheet 3 of 3)

4.5.1 8085 I/O Microprocessor and Associated Logic

The 8085 I/O microprocessor E12, the 8259 interrupt controller E27, and the 8155 I/O port and RAM E18 are the main elements used to control the transfer of information between the I/O devices and the LSI-11 microprocessor. The device handler routines for each I/O device are contained in the 2K × 8-bit ROM 0, ROM 1, and ROM 2. Refer to the *Intel MCS-85™ User's Manual* for detailed information on the operation of these elements.

The 8085 receives 6.0825 MHz input clock pulses, PCLK and $\overline{\text{PCLK}}$ from the clock pulse generator for the LSI-11 microprocessor. The internal operating frequency of the 8085 is one-half of the input frequency. During write operations, the WR output from the 8085 indicates that data is available on lines AD 0 H–7 H. During read operations the RD output indicates that the AD 0 H–7 H lines are ready to receive data. The ALE H signal is used to latch the low byte of the address information into the low-byte address register E26.

4.5.1.1 8085 I/O Transfers – Data and low-byte address information is transferred between the 8085 and associated logic through lines AD 0 H–7 H. These lines are buffered by the bidirectional bus transceiver E5 to become the HDBAD 0 H–7 H lines, which communicate with the I/O devices through the Peripheral module, and with the disk drives through the Disk Controller module. The HDBAD 0 H–7 H lines are also buffered by the bidirectional bus transceiver E4 to become the BAD 0 H–7 H lines. These lines provide the information to the low-byte address register E26 and the information is latched into the register by the inverted address latch signal ALE H from the 8085. The BAD 0 H–7 H lines also transfer information from the addressed locations of ROM0, ROM1 and ROM2 and to and from the LSI-11 microprocessor through the drivers and receivers of the Inter-Processor Link (IPL) logic.

The bus transceiver E5 is enabled by a decoded I/O 6 L or MEM 7 L signal from the memory and device address decoders. Bus transceiver E4 is enabled by the decoded BLANK 1 H signal. The direction of transfer of E4 and E6 is controlled by the RD L signal or the INTA L signal from the 8085. The RD L output is low whenever the 8085 requests a read operation, and the INTA L output is low when an interrupt request to 8085 has been acknowledged. Either output will cause the information to be transferred to the 8085.

The ROM0, ROM1 and ROM2 are enabled by the decoded MEM 0 L, MEM 1 L and MEM 2 L outputs of the memory and device address decoders. The addressed information from the memory is transferred to the HDBAD 0 H–7 H lines by the low RD L signal from the 8085.

4.5.1.2 Interrupt and Priority Assignments – The 8085 I/O microprocessor receives five separate interrupts to inputs TRAP, RST 5.5, RST 6.5, RST 7.5 and INTR as shown on Figure 4-4 (Sheet 1). All vector interrupts are fixed except INTR, which is variable. The TRAP interrupt request has the highest priority and is generated as a result of the high interrupt acknowledge signal WIAK H and input request signal WDIN H, both from the LSI-11 microprocessor. The WIAK H signal becomes high in response to an interrupt request from the 8085 I/O microprocessor and the WDIN H signal becomes high when the LSI-11 initiates an input request. The RST 7.5 is next in priority status and is generated by the TIMER H signal from the 8155. This interrupt allows the 8085 to check periodically the I/O device status registers to determine if servicing is required.

When the printer terminal USART is ready to transmit data, an interrupt request is generated at the RST 6.5 input; when the printer terminal is ready to receive data, an interrupt request is generated at the RST 5.5 input. The lowest priority input is INTR, which is generated as a result of any of the interrupt requests received by the 8259 Interrupt Controller IC. The interrupt request priority level at the 8259, and the associated devices producing the requests are listed in Table 4-1.

Table 4-1 8259 Interrupt and Priority Assignments

Input	Priority Level	Signal	Interrupt Request
IRO	1	CDA H	Modem USART Receiver ready (RXRDY)
IR1	2	TDA H	Console USART Receiver ready (RXRDY)
IR2	3	TTBMT	Console USART Transmitter ready (TXRDY)
IR3	4	DONE H	Disk Controller 8085 in halt state
IR4	5	CTBMT	Modem USART Transmitter ready (TXRDY)
IR5	6	FWIR H	Decoded LSI-11 address Write on disk
IR6	7	FRIR H	Decoded LSI-11 address Read from disk
IR7	8	WDINTRQ H	Decoded LSI-11 address (all I/O devices except disk drives)

4.5.1.3 8155 I/O Port and RAM IC Functions – The 8155 I/O port and RAM (E18) is shown in Figure 4-4 (Sheet 2) contain three I/O ports, a 2K × 8-bit static RAM, and a programmable 14-bit counter. Data and address information is transferred between the 8155 and the 8085 I/O microprocessor through the low-byte lines AD0 H–7 H shown in Figure 4-4 (Sheet 1). The 8155 is enabled by decoding one of two addresses on lines A 11–A 15 from the 8085 at the memory and device address decoder.

A low MEM 7 L or low I/O 6 L output of the decoder is gated at E1 to generate a high BLANK 0 H signal, which disables the bus transceiver E5, and is inverted to enable the 8155. The MEM 7 L signal is also connected to the 8155 IO/M input; when the signal is low, the 2K × 8-bit static RAM will be selected. When the I/O 6 L is decoded, MEM 7 L will be high and one of the three I/O ports of the 8155 can be selected by the internal CS register.

The I/O port A of the 8155 (PA 0–7) is used to monitor the eight bits of the address information on lines ADR 00 H–ADR 07 H, and port C (PC 0 and PC 1) monitors lines ADR 08 H ADR 09 H. When an interrupt request from the LSI-11 microprocessor occurs for an I/O peripheral device other than a disk drive, the 8085 will read the address information from the 8155 to determine the specific device register addressed by the LSI-11. The 8085 will then access the device handler routine in the ROM used to service the device. The I/O port B (PB 0–PB 6) and I/O port C (PC 2–PC 4) are accessed by the 8085 during program I/O operations to provide status conditions. I/O port B receives the BTEST L signal, which indicates normal program operation or self-test mode of operation, PB 2 through PB 6 inputs which are control signals from the modem, and the INIT MK H signal which is set by the 8085 when a power-up or manual reset reset occurs. The PC3 input of I/O port C receives the WWB H signal from

the LSI-11 which specifies a word or byte transaction and the PC 4 input, when not grounded by jumper W1, indicates that the Cluster controller option is installed in the PDT-11/150. The PC 2 input receives the B DIN H signal from the LSI-11 to specify a read or write operation at the register addressed by the LSI-11.

The 8155 also receives signals RD L and WR L from the 8085 and a TIMER CLK input of 316.8 KHz from the LSI-11 clock pulse generator.

4.5.1.4 Test Indicator Register – The test indicator register E11 stores the address information from the 8085 on lines AD 0 H–5 H to control the five LED indicators and to generate the FLD DCD EN L signal. The five LED indicators light to specify the octal number of the test being performed during the self-test mode. The FLD DCD EN L signal enables the decoding of the LSI-11 address to generate a read or write disk interrupt to the 8085 I/O microprocessor. The information is stored in the register by a low-to-high transition of the WR L signal from the 8085 or by a low-to-high transition of the I/O 8 L output from the device address decoder. LINE AD 0 H, when high (1), sets the flip-flop in the register to generate a high FLD DCD EN H signal. Lines AD 1 H–AD 5 H, when high (1), set the flip-flop registers to light LED 1 through LED 5. The E11 register is cleared by the RESET OUT L signal from the 8085.

4.5.1.5 8085 Memory and I/O Select Address Decoding – The address information from the 8085 is decoded as shown on Figure 4-5 to produce I/O select and memory select signals on unique select lines distributed throughout the PDT-11/150 logic. The information on address lines A 11 H–15 H is decoded to produce a low select signal on line MEM 0 L, MEM 1 L, MEM 2 L or MEM 7 L. The MEM 0 L–2 L signals are used to enable one of three ROM banks of the 8085. The MEM 7 L signal enables the 8155 I/O port and RAM IC to read or write in RAM. Table 4-2 lists each of the functions enabled by the memory select decoder addresses. Address lines A 0 H and A 11 H–15 H are decoded to produce I/O select signals I/O 0 L–I/O 14 L, I/O 1.5 L, and TIM FWD SEL L. Most of the memory I/O select signals are gated with the read (RD L) or write (WR L) signals from the 8085 and enable specific elements within the PDT-11/150. Table 4-3 lists the specific functions selected by the device select decoder address.

Table 4-2 8085 Memory Select Decoding

Memory Address					8085 Signal			Decoded Output	Function Selected
A15	A14	A13	A12	A11	INTA L	RD L	WR L		
L	L	H	H	H	H			MEM 7 L	Enable 8155 I/O port and RAM
L	L	L	H	L	H	L	X	MEM 2 L	Read ROM 2
L	L	L	L	H	H	L	X	MEM 1 L	Read ROM 1
L	L	L	L	L	H	L	X	MEM 0 L	Read ROM 0

X = H or L

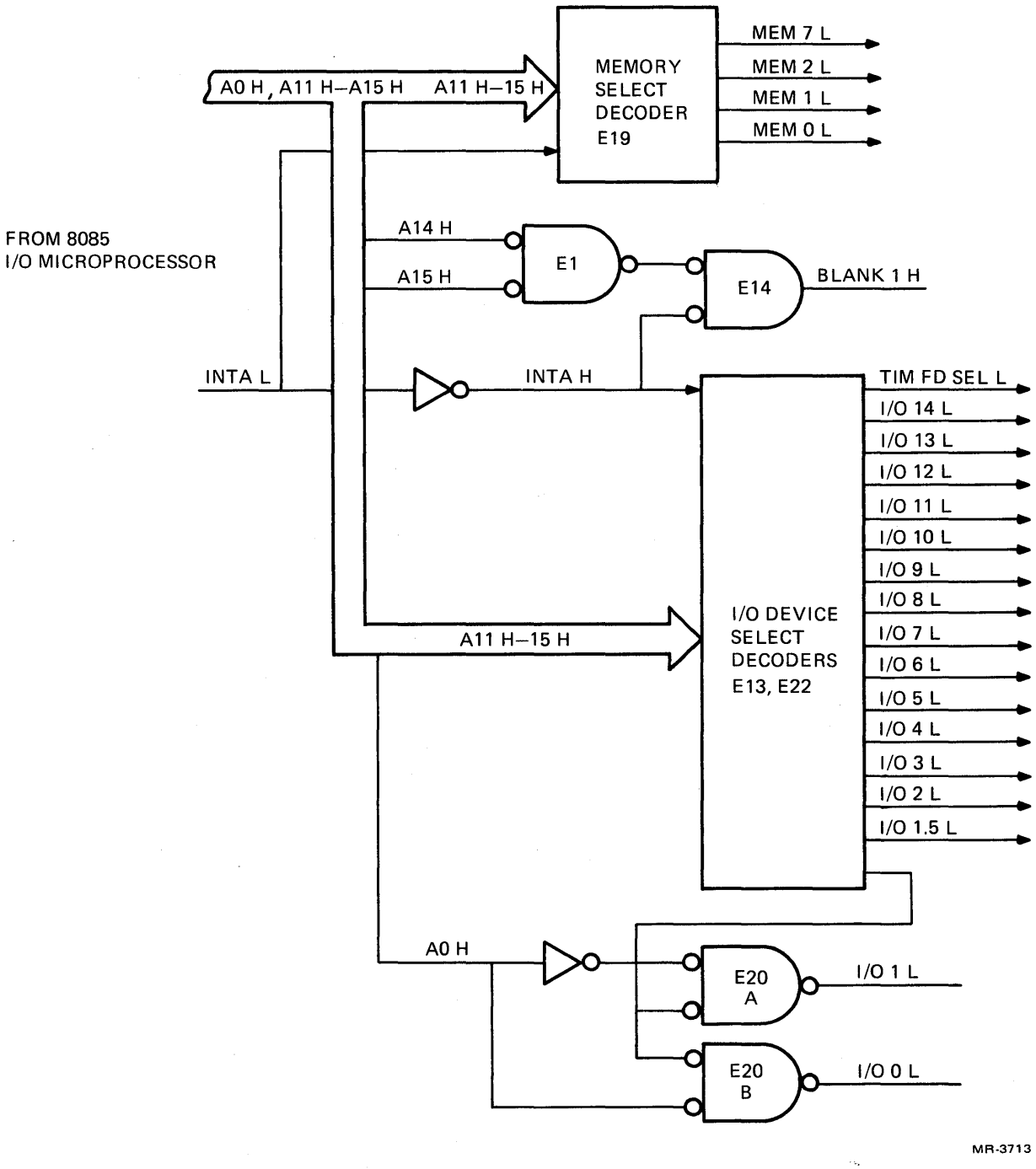


Figure 4-5 8085 I/O Microprocessor, Memory and Device Select Logic, Simplified Diagram

Table 4-3 8085 I/O Device Select Decoding

Memory Address						8085 Signal			Decoded Output	Function Selected
A0	A15	A14	A13	A12	A11	INTA L	RD L	WR L		
X	L	L	X	X	X	H	X	X	BLANK 1 H	8085 bus transceiver
X	H	H	H	H	H	H	X	X	TIM FD SEL L	Enable disk controller
X	H	H	H	H	L	H	L	L	I/O 14 L	Enable terminal 3 USART
X	H	H	H	H	L	H	L	L	I/O 13 L	Enable terminal 2 USART
X	H	H	H	H	L	H	L	L	I/O 12 L	Enable terminal 1 USART
X	H	H	L	H	L	H	L	X	I/O 11 L	LSI-11 interrupt request (IRQ)
X	H	H	H	L	H	H			I/O 10 L	Not used
X	H	L	L	H	H	H	X	X	I/O 9 L	Enable 8259 interrupt controller
X	H	L	L	H	L	H	L	X	I/O 8 L	Power-up and mode switch reset
X	H	L	H	H	H	H	X	L	I/O 7 L	Enable event interrupt to LSI-11
X	H	L	H	H	L	H	X	X	I/O 6 L	Enable 8155 I/O port and RAM
X	H	L	H	L	H	H	X	L	I/O 5 L	Interrupt to disk controller 8085
X	H	H	L	H	H	H	L	L	I/O 4 L	Enable line printer USART
X	H	H	L	L	H	H	L	L	I/O 3 L	Enable modem USART
X	H	H	L	L	L	H	L	L	I/O 2 L	Enable console USART
X	H	L	L	L	H	H	X	L	I/O 1.5 L	8085 set INIT MK H
H	H	L	L	L	L	H	L	X	I/O 1 L	IPL receive low byte
H	H	L	L	L	L	H	X	L	I/O 1 L	IPL clock low byte out
L	H	L	L	L	L	H	L	X	I/O 0 L	IPL receive high byte
L	H	L	L	L	L	H	X	L	I/O 0 L	IPL clock high byte out

X = H or L

4.5.1.6 Power-Up and Manual Reset – Figure 4-6 is a simplified diagram of the circuits used to reset the 8085 I/O microprocessor and associated logic. When ac power is initially applied or when the mode switch on the rear panel is set to the RESET position, the RC network consisting of R2 and C1 will hold the RESET IN input to the 8085 at a low level for 100 ms. This delay permits the 8085 to initialize internal registers and counters and to disable the internal interrupt request functions.

The low output of the RC network is inverted to a high INIT H level, which clears the timer clock E38 and disables the generation of the TIMER CLK H and TIME OUT CLK H output pulses. The TIMER CLK H line provides the basic timing pulses to the counter/timer in the 8155 I/O port and RAM E18. The TIMER OUT output of the counter/timer will also be disabled and, therefore, no TIMER H pulses will occur to cause an interrupt request at the RST 7.5 input to the 8085. The TIMER H line also connects to the flip-flop E39A, which will remain cleared until the TIMER H pulses occur. The (1) output of E39 generates a refresh pulse that causes an interrupt to the LSI-11 and results in a RAM module refresh cycle.

The TIME OUT CLK H line provides the basic timing pulses to the 1.6 ms Time-Out (T.O.) counter E52. With the input pulses inhibited, no count will occur and the Z output of the counter will be held low. This output provides the reset signal to the LSI-11 microprocessor through the interrupt request register E47, and the LSI-11 will remain in a reset condition.

The high INIT H signal is inverted to a low INIT L signal, which presets flip-flops E29 and E39A. The low DCLO L output of E39A is buffered to become a low BDCLO L signal, which clears flip-flop E39B, clears the interrupt request register E47 and clears flip-flop E46. Flip-flop E46 is normally controlled by the LSI-11 program to cause a reset condition of the 8085 microprocessor.

After a 100 ms delay, the level from the RC network will become high, the INIT H signal will become low and the timer clock E38 will be enabled. The INIT L signal will become high, removing the low RESET IN level to the 8055 I/O microprocessor. The 8085 I/O microprocessor will perform a power-up sequence, which requests an autobaud from the console, initializes the disk controller logic, and initializes the terminal USARTs on the Peripheral module to the default condition.

During the power-up sequence, the 8085 produces an address on lines A 11–15 which is decoded by E13 to generate a low I/O 8 L signal. This signal is gated at E3 with a low RD L signal and results in a high PWR UP H signal to flip-flop E39A. The PWR UP H signal clears flip-flop E39A and its DCLO L output becomes high. The resulting high BDCLO L output allows flip-flop E39B to be clocked by the TIMER H pulses and allows interrupt requests to be latched into the interrupt request register E47. The high BDCLO L signal enables flip-flop E46 to be controlled by the D3 and D6 outputs of the LSI-11 decoder E49. This allows the LSI-11 to reset the 8085 I/O microprocessor by program. The BDCLO L signal is also gated with the high D5 output of E49 at gate E21. The high output of E21 is gated with the high TERR (1) H signal from the Y output of the T.O. counter E52 and produces a low signal to the U/C input of E52. The low input will clear an internal flip-flop and result in a low TERR (1) H signal from the Y output. The TERR (1) H signal, when high, indicates to the LSI-11 that a timeout error has occurred. With the TIME OUT CLK H pulses enabled, the T.O. counter E52 will initiate the count and the Z output will become high to remove the reset condition from the LSI-11 microprocessor.

During the power-up sequence of the 8085 I/O microprocessor, address lines A 11–15 are also decoded by E13 to produce a low I/O 1.5 L signal. This signal is gated with a low WR L signal from the 8085 and the high output will clear flip-flop E29. The INIT MK H signal from E29 is an input to the 8155 I/O port and RAM E18, and is monitored by the 8085 during program operations. During normal operations, the INIT MH H signal is high whenever an ac power-up or manual reset has occurred, and low for a program reset instruction from the 8085. The AD 0 H line from the 8085, however, can control the INIT MK H signal by program.

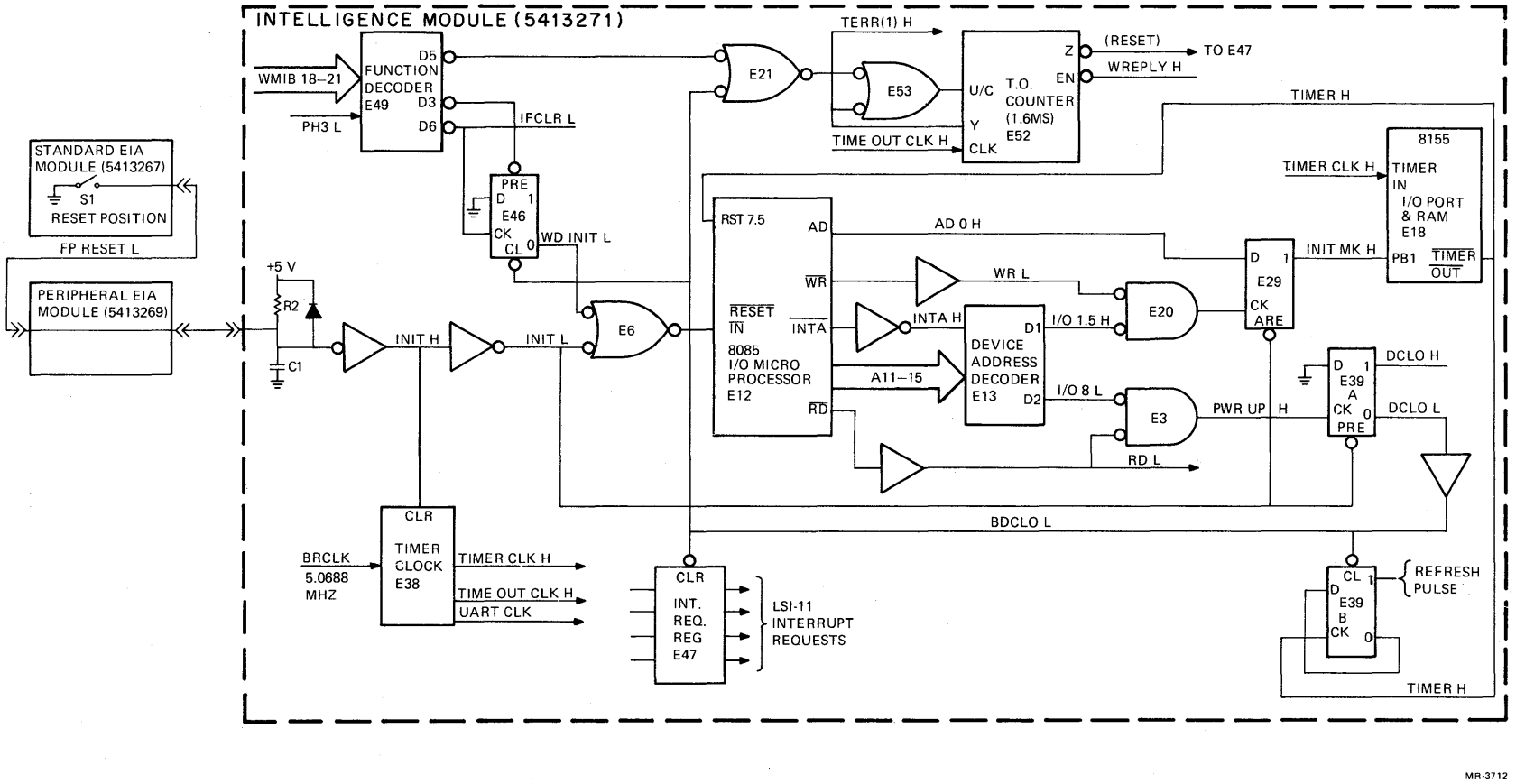


Figure 4-6 Power-up and Manual Reset, Simplified Diagram

4.5.2 Inter-Processor Link (IPL) and Control Logic

Figure 4-7 is a simplified diagram of the Inter-Processor Link (IPL) and shows the logic and signals used for control. The IPL converts the 16 bits of information on the LSI-11 bus into two 8-bit bytes for the 8085 microprocessor. It also stores two 8-bit bytes from the 8085 and transfers them to the LSI-11 bus as a 16-bit word. The IPL consists of a low-byte register and drivers and a high-byte register and drivers. During data transfers to the LSI-11, the first 8-bit byte on lines BAD 0 H–7 H is clocked into the high-byte register by the CLK HB OUT L signal. The second 8-bit byte is clocked into the low-byte register by the CLK LB OUT L signal, and the IPL DRIVE (1) signal gates the low and high bytes onto the WDAL 04 H–15 H and BWDAL 00 H–03 H lines of the bus.

During data transfers from the LSI-11 microprocessor, the information on lines WDAL 08 H–15 H is strobed onto lines BAD 0 H–7 H through the high-byte drivers by the RCV HB L signal. The information on lines BWDAL 00 H–03 H and WDAL 04 H–07 H is strobed onto lines BAD 0 H–7 H through the low-byte register by the RCVLB L signal.

The 8085 I/O microprocessor controls the direction of the IPL's operation. During write commands from the 8085, the WR L signal at E9D will be low and gated with a low I/O 0 L signal from the select decoder. The resulting low CLK HB OUT L signal will clock the information on the BAD 0 H–7 H lines to the WDAL 0 H–15 H lines through the high-byte register E36.

A high WIAK H or I/O SEL H signal will produce a low output at gate E3. Signal WIAK H is generated by the LSI-11 to acknowledge an interrupt request from the 8085 and the I/O SEL H signal indicates that the address from the LSI-11 was decoded as an I/O device address. The low output of E3 is gated with a low RESET OUT H signal from the 8085 at E9A. The output of E9A and the low I/O 1 L signal from the select decoder will produce a high output of gate E14. This output is inverted and applied as an input to gate E9B, which also receives the low WR L signal. The resulting CLK LB OUT L signal will clock the information on the BAD 0 H–7 H bus through the low-byte register E35 to the BWDAL 0 H–3 H and WDAL 04 H–07 H lines.

The outputs of registers E35 and E36 are initially enabled by the low IPL DRIVE (1) L output of flip-flop E15A. Before the control signals are received, the output of gate E9A is high. This signal is inverted and holds flip-flop E15A in a clear condition. After the write data transaction has been completed, the low-to-high transition of the WR L signal and the high D input will set flip-flop E15A. The high IPL DRIVE (1) L signal will disable the output of registers E35 and E36.

During a read operation, the RD L signal from the 8085 is low and is gated at E9C with the low decoded select signal I/O 0 L. The resulting low RCV HB L output of E9C will transfer the information on lines WDAL 08 H–15 H to the BAD 0 H–7 H bus through the high-byte driver E32. The inverted RD L signal is gated at E1 with the high output of gate E14. The low RCV LB L output of gate E1 transfers the information on lines BWDAL 00 H–03 H and WDAL 04 H–07 H to the BAD 0 H–7 H bus.

4.5.3 LSI-11 Microprocessor and Associated Logic

The LSI-11 microprocessor located on the Intelligence module consists of four, 40-pin integrated circuits. Figure 4-8 is a simplified block diagram that shows the processor data IC, processor controller IC and the two microinstruction ROM ICs. Refer to the M7270 module described in the DIGITAL *Microcomputer Processors Handbook 1978–79* for a general description of the LSI-11 functions. The LSI-11 ICs communicate with each other through the WMIB 00 L–21 L bus. Bus lines WMIB 18 L–21 L also connect to the special control function logic that generates signals for the RAM refresh cycle, the fast DIN cycle, and lights the RUN indicator on the front panel of the unit.

Timing and synchronization of the LSI-11 circuits and related logic are controlled by the four phase outputs of the clock pulse generator. The clock pulse generator also provides timing signals for the 8085 microprocessor and the counter in the 8155 I/O port and RAM IC.

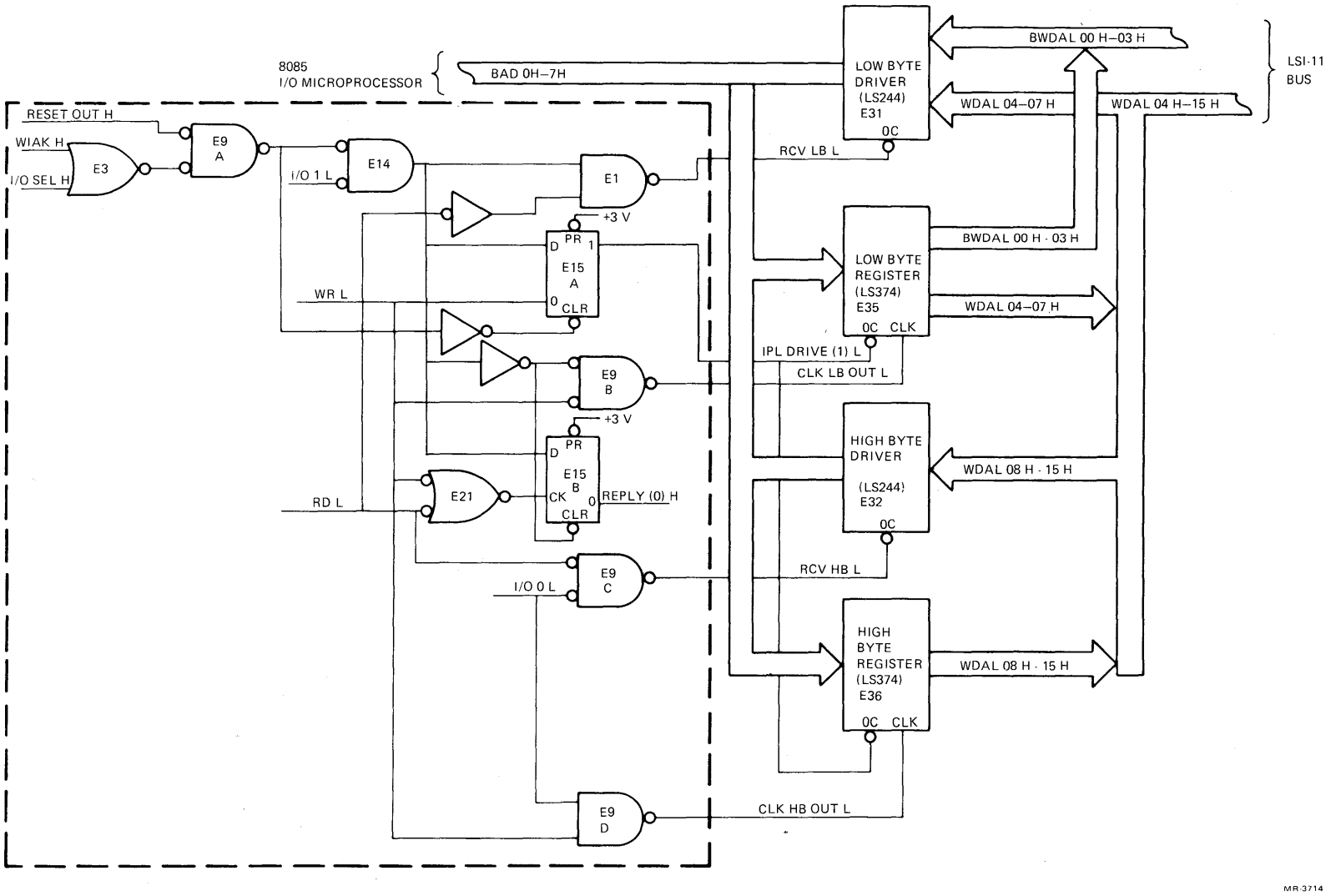


Figure 4-7 IPL and Control Logic, Simplified Diagram

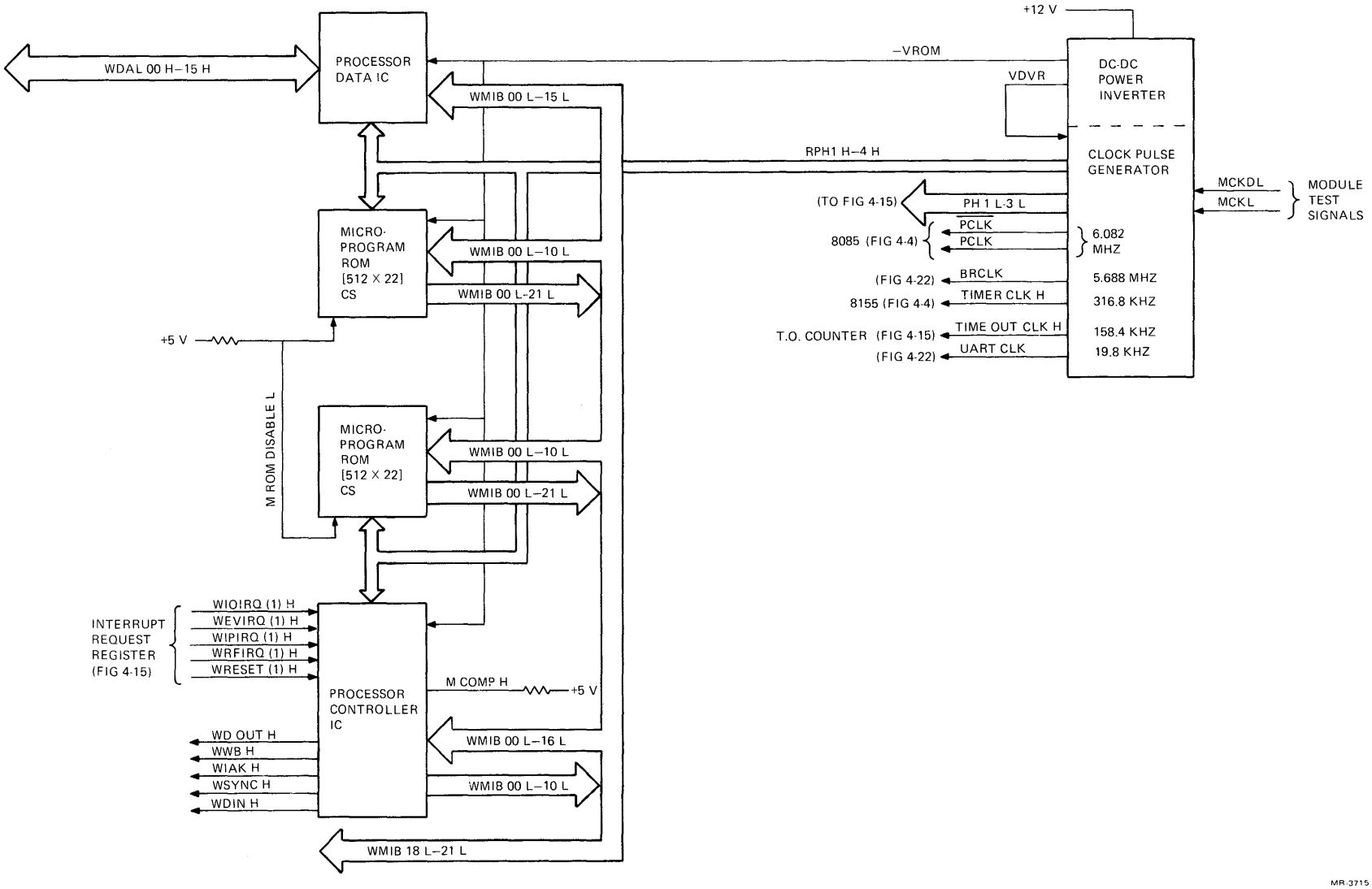


Figure 4-8 LSI-11 Microprocessor, Simplified Block Diagram

The LSI-11 processor controller IC receives five separate interrupt request lines from the interrupt request register. These lines enable the LSI-11 program to branch for specific request inputs. This IC also provides most of the control signals for the associated logic.

4.5.3.1 Clock Pulse Generator and Power Inverter – Figure 4-9 is a simplified diagram of the clock pulse generator and power inverters which provide the system timing and synchronization signals. The basic frequency is produced by a 30.413 MHz crystal-controlled oscillator which is gated into a four-state decoder. The maintenance clock gates allow external test signals to be used when performing tests and maintenance using a module tester. The four-state decoder generates the four phase signals RPH 1 L through RPH 4 L. Signals PH 1 through PH 3 are used by the LSI-11 special control function logic. The four-state decoder also provides a 10.1367 MHz output to the dc-dc power inverter, which generates a +13.4 V (VDVR) voltage source for the drivers and delay circuit and a -3.9 V (-VROM) bias voltage for the LSI-11 IC set.

The driver and delay circuits receive phase signals, PH 1 L through PH 4 L, and produce four nonoverlapping signals RPH 11 H through RPH 4 H, which are used for the timing of the main states of the LSI-11 IC set. The +5 V voltage regulator ensures a stable voltage for the delay circuits. A divide-by-three output of the four-state decoder is applied to the divide-by-two counter, resulting in a BRCLK (5.0688 MHz) signal used to time the baud-rate generator of the USARTs on the Peripheral module. The BRCLK signal is also applied to a dual divide-by-sixteen counter. The output of the first divide-by-sixteen counter is the TIMER CLK H (316.8 KHz) signal and is used for the basic timing of the interval timer in the 8155 IC. The same output is divided by two to generate the TIMER OUT CLK H (158.4 KHz) frequency, which clocks the time out counter for the LSI-11 microprocessor. This output is divided by eight and used to time the USARTs in the PDT-11/110 and PDT-11/130 system units, which also use the KDT11-AA Intelligence module. The dual divide-by-sixteen counter is cleared by the INIT H signal during power-up or when reset by the switch on the rear panel.

The 30.413 MHz output of the maintenance clock gate is divided by five to generate the (6.0825 MHz) PCLK and $\overline{\text{PCLK}}$ signals used as the input frequency of the 8085 microprocessor.

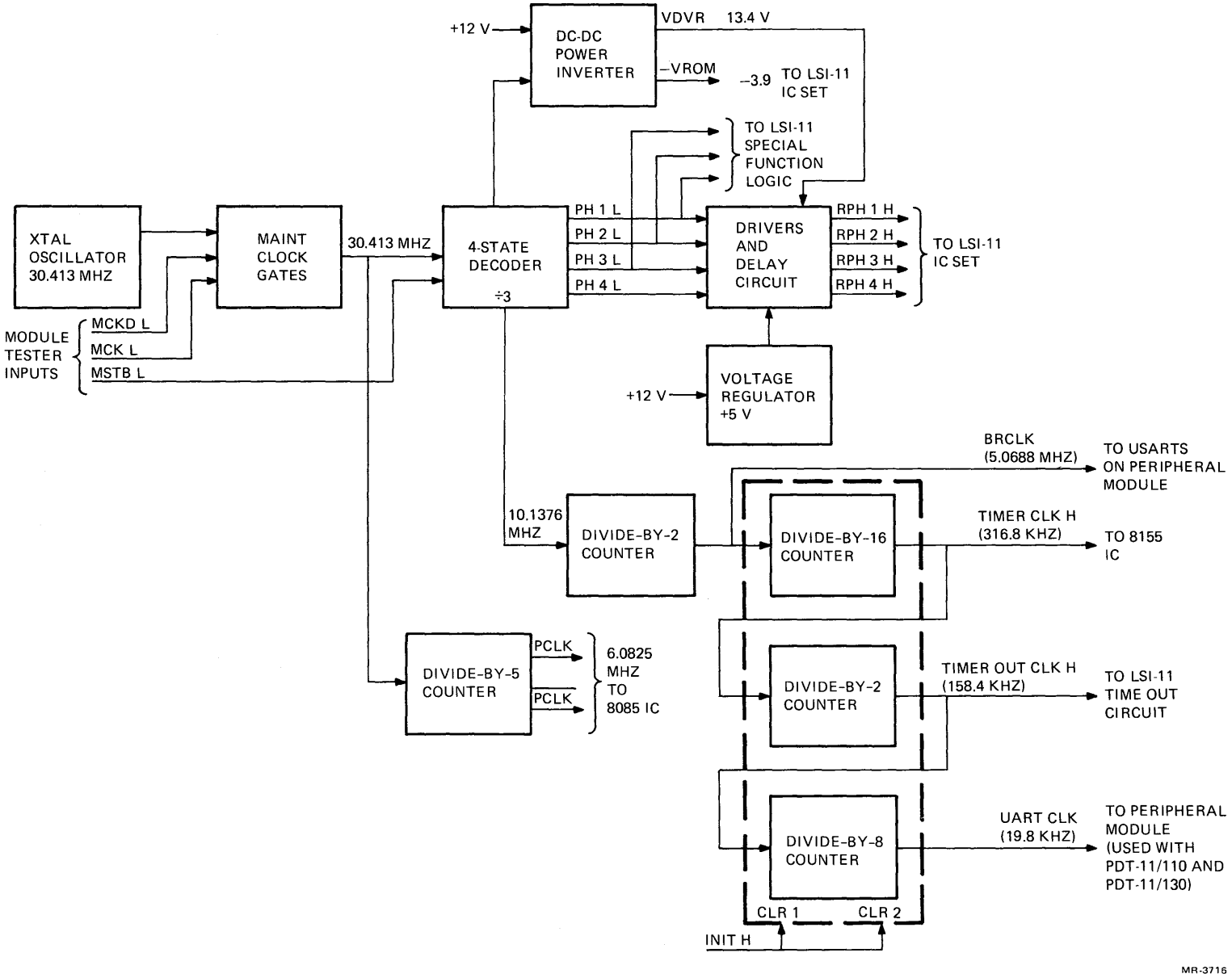


Figure 4-9 Clock Pulse Generator and Power Inverter, Simplified Block Diagram

4.5.3.2 LSI-11 I/O Transfer Sequence – Each LSI-11 microprocessor I/O instruction requires one or more transfer operations. The sequences are identical when transferring instructions or data to or from RAM or when transferring data, control or status information to or from an I/O device or disk controller. The four sequences used are read (input transfer), write (output transfer), read-modify-write (input and output), and interrupt acknowledge read (vector input).

Figure 4-10 (Sheets 1 and 2) shows the timing sequence of the data and control signals required during each type of transfer. The RPH 01–04 segments at the top of each diagram are the four phase inputs RPH 1 H-4 H developed by the clock pulse generator. The completion of these four phases constitutes one LSI-11 processor cycle.

1. Write Word or Byte – The write word or byte is an output operation that transfers information from the LSI-11 to the addressed location. Figure 4-11 shows the sequence of events that occur during the program output transfer.

   The operation is initiated when the LSI-11 transfers a 16-bit address to the WDAL 00 H–15 H bus followed by a high WSYNC H level. The WSYNC H level is inverted to WSYNC L and is used to latch the address information into the 16-bit address register E41 and E42 (see Figure 4-4, Sheet 2).

   During the next cycle the data is transferred from the LSI-11 to the WDAL 00 H–15 H bus and the WD OUT H signal becomes high when the data is available on the bus. The WD OUT H level is latched into flip-flop E33 during PH 1 L time and produces the IN OR OUT H and D OUT (0) H signals from the device address decoder (also shown in Figure 4-4, Sheet 2). The WD OUT (0) H signal specifies a write operation to the RAM module and is used in the generation of the disk controller FWIR H interrupt signal. The IN OR OUT H signal clears the T.O. counter E52 (see Figure 4-4, Sheet 3).

   When the WWB H signal is high, a byte transfer is specified and the byte information will appear on the upper and lower halves of the WDAL 00 H–15 H lines. The WWB H signal is monitored by the 8155 I/O port and RAM E18 (see Figure 4-4, Sheet 2) during I/O transfers to peripheral devices. If a word is specified by the WWB H signal, the entire 16-bit word appears on the WDAL 00 H–15 H bus. The WREPLY H signal is generated in response to signal conditions from the 8085 I/O microprocessor E12 and the device address decoder and in response to signals produced by the RAM module. If the WREPLY H signal does not occur within 1.6 ms after WD OUT H becomes high, the LSI-11 will terminate the cycle and trap through location 4, which is the timeout error vector address.

2. Read Word or Byte – The read word or byte is an input operation that transfers information from the addressed location to the LSI-11. Figure 4-12 shows the sequence of events that occur during the program input transfer.

   The WDIN H signal indicates to the device or memory that an input operation is requested. The WDIN H level becomes high when the address information is removed from the bus. The WDIN H signal is inverted to WDIN L, which controls the bus transceiver E65 during the fast-data-in cycle of the LSI-11 (see Figure 4-4, Sheet 3). The WDIN L signal is also inverted to become BDIN H, which is monitored by the 8155 I/O port and RAM E18 (see Figure 4-4, Sheet 2) to specify a data transfer from the addressed I/O device to the LSI-11. During the read operations, the LSI-11 determines the selection of the upper byte, lower byte, or byte specified by the low-order bit of the address.

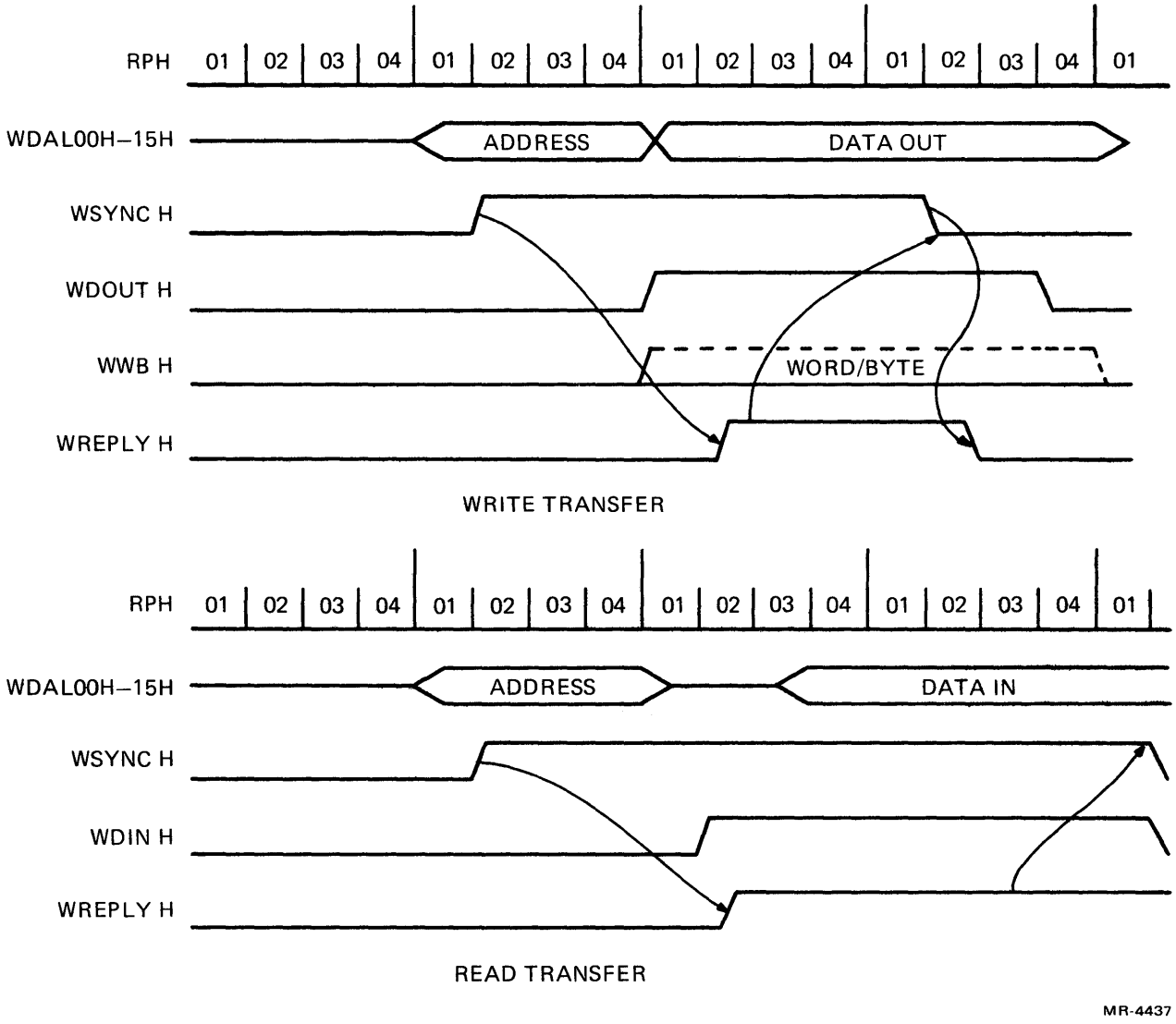


Figure 4-10 LSI-11 Microprocessor, I/O Transfer Timing
(Sheet 1 of 2)

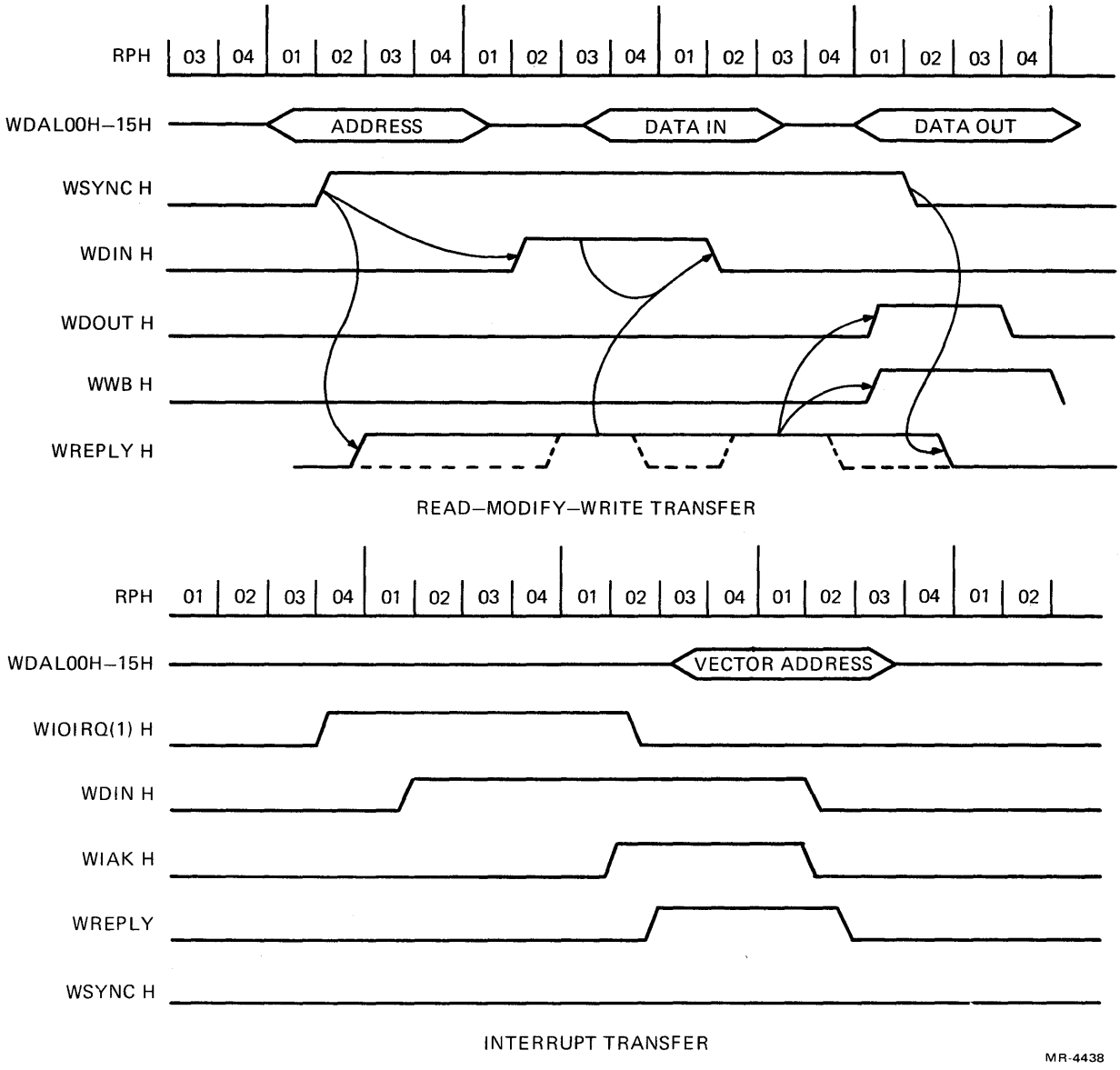


Figure 4-10 LSI-11 Microprocessor, I/O Transfer Timing
(Sheet 2 of 2)

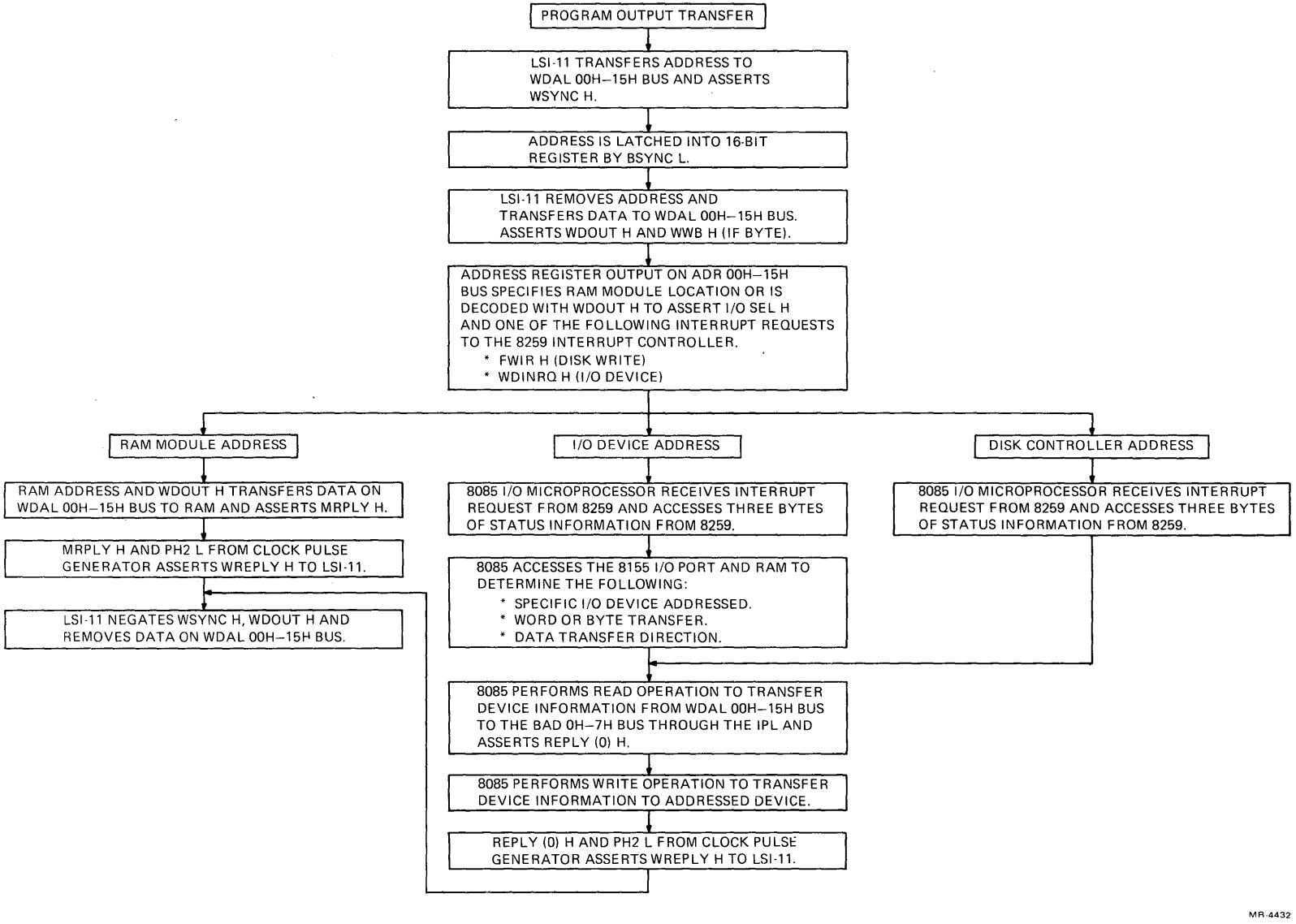


Figure 4-11 Output Transfer Events

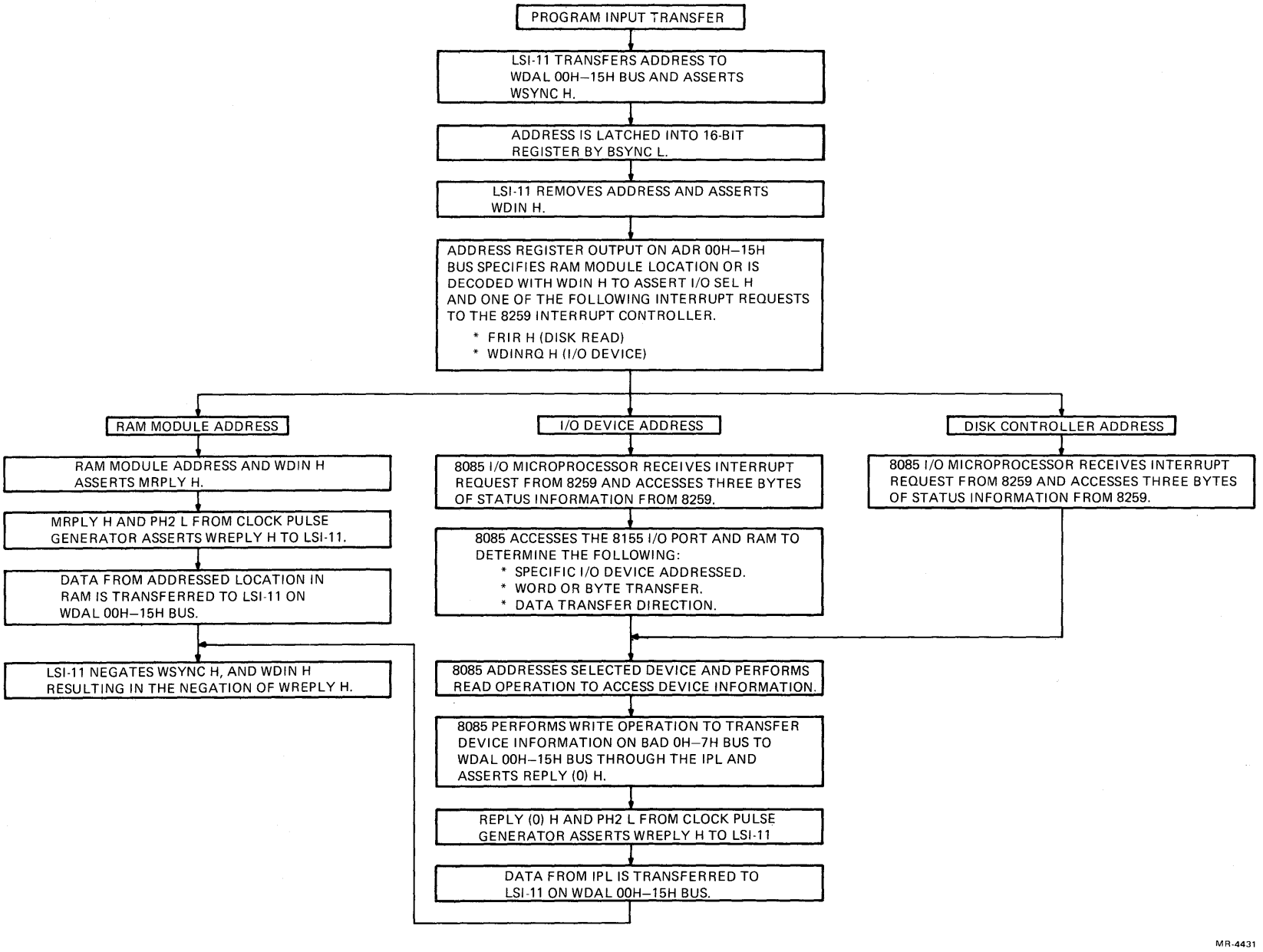


Figure 4-12 Input Transfer Events

3. Read-Modify-Write – This operation causes an input and output transfer to occur successively. The sequence of the transfer is the same as shown in Figures 4-11 and 4-12.

   Information is transferred from the addressed device to the LSI-11 and vice versa. The WSYNC H signal holds the address in the 16-bit address register for the entire sequence. The WDIN H signal becomes high before the data is transferred and the WD OUT H signal becomes high after the data appears on the WDAL 00 H–15 H bus. The WWB H will become high when a byte transfer is specified during the write cycle. The WREPLY H signal is generated in the same manner as described in the read or write operations.

4. Read Interrupt Acknowledge – This operation occurs as a result of an LSI-11 interrupt request generated by the 8085 I/O microprocessor; it transfers a vector address to the LSI-11 on the WDAL 00 H–15 H bus from the 8085. Figure 4-13 shows the sequence of events that occur during the interrupt acknowledge operation. The 8085 sends an IRQ H interrupt request to the LSI-11 (see Figure 4-4, Sheet 3). This occurs when the disk controller or I/O device is requesting service. When interrupted, the LSI-11 will access the vector address of the device routine from the WDAL 00 H–15 H bus. The LSI-11 will cause the WSYNC H signal to become high prior to the vector address input and the WIAK H interrupt acknowledge signal will be in sequence with the WSYNC H signal. The WREPLY H signal will occur as a result of the signals from the 8085 I/O microprocessor and the WIAK H output.

   After receiving the vector address the LSI-11 it will service the requesting device by performing the required read or write operations as specified by the device routines.

4.5.3.3 LSI-11 I/O Device Address Decoding – Figure 4-14 is a simplified diagram of the logic used to decode the device address information from the LSI-11 microprocessor and to generate interrupt requests to the 8085. The address decode logic produces an interrupt request for all valid I/O device addresses above 176XXX. The 8085 I/O microprocessor determines if the address is valid by reading address bits ADR 0 H–7 H through the 8155 I/O port and RAM E18.

The address information on lines BWDAL 00 H–03 H and WDAL 04 H–15 H from the LSI-11 is loaded into the 16-bit register E41 and E42 by the WSYNC L signal from the LSI-11, and is transferred to lines ADR 00 H–15 H. The address information on lines ADR 04 H–09 H is decoded by the 6-bit decoder E43. With the strobe input grounded, an address of XX116X will produce a high output to E30B. The address information on lines ADR 10 H–15 H is decoded by the 6-bit decoder E48 and the output will become high on a high-to-low transition of the BSYNC H signal. The BSYNC H input, a buffered WSYNC H signal, will occur for all I/O transfers of the LSI-11 except for the vector input transfer, which occurs during an interrupt request to the LSI-11. Address lines ADR 01 H and ADR 03 H are gated at E30A with the FLP DCD EN H signal from the indicator register E11. The FLP DCD EN H signal will become high when the indicator register is loaded and bit AD 0 H from the 8085 is high. With all inputs high, the output of gate E30A will be high. This output is gated with the high output of the 6-bit decoder E43 and with the inverted address bit ADR 02 H. The output of E30B will become high when an address of XX1172 is decoded, which specifies a read or write operation to the Disk Controller module.

During an input or output transfer of the LSI-11 microprocessor, the DOUT (1) H or BDIN H signal at E20 will generate the high IN OR OUT H signal. This signal is gated at E30C with the decoded address signal 176XXX from the 6-bit decoder E48. The E48 output will be high for all decoded addresses of the I/O device registers and Disk Controller module registers. The output of gate E30C is enabled by a low WSYNC L signal and a low REF (1) H signal to gate E14. The WSYNC L signal, the inverted WSYNC H signal from the LSI-11, will occur for all I/O transfers of the LSI-11 except the vector input transfer during an interrupt request.

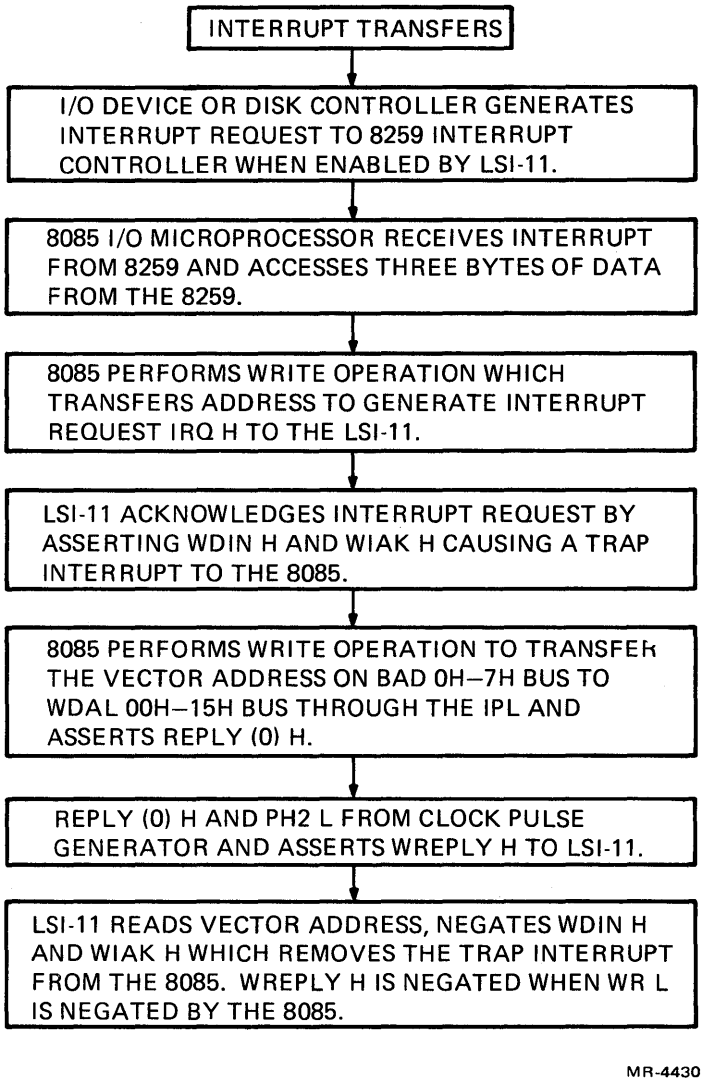


Figure 4-13 Interrupt Transfer Events

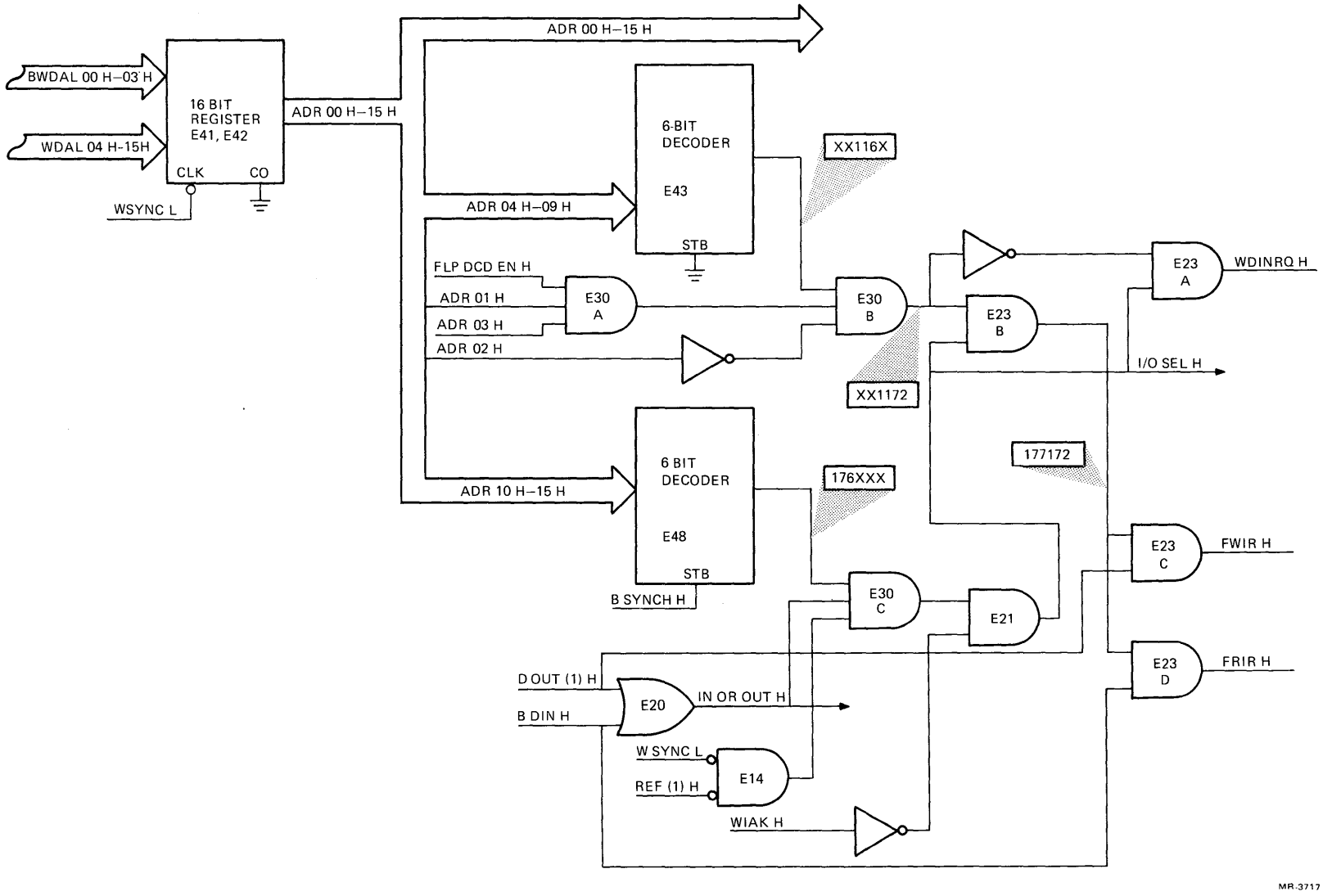


Figure 4-14 LSI-11 I/O Device Address Decoding Logic, Simplified Diagram

The high REF (1) H signal prevents an I/O device address from being decoded during the RAM refresh cycle. The output of gate E30C is applied with an inverted WIAK H signal at gate E21 to produce the I/O SEL H output, which specifies a decoded address to any external I/O device or to an internal disk drive. The I/O SEL H signal is applied as an input to gate E23B with the decoded XX1172 address; this produces an output of 177172, which is the address of the data buffer in the disk controller. During output operations from the LSI-11, the 177172 output and DOUT (1) H at gate E23C will generate the high FWIR H signal, indicating an interrupt request to the 8085 for a write to the disk controller data buffer. During input operations, the BDIN H signal and the 177172 output to gate E23D will result in a high FRIR H signal specifying an interrupt request to the 8085 for a read from the data buffer in the disk controller. All other decoded I/O addresses will cause a high WDINRQ H output from gate E23A, which is a general interrupt to the 8085 I/O microprocessor.

4.5.3.4 Function Control, Fast-Data-In and Interrupt Request Logic – Figure 4-15 shows the logic that develops the control functions, the reset and interrupt requests, and the conditions monitored by the fast-data-in (DIN) cycle of the LSI-11 microprocessor.

The microinstruction bus lines WMIB 18 L–21 L from the LSI-11 are decoded during the PH 3 L interval to enable one of the six outputs of the function decoder E49. Table 4-4 lists the bus inputs and the function of the outputs.

The interrupt requests and reset level to the LSI-11 are transferred from the interrupt request register E47 during the PH1 interval of the clock pulse generator. When ac power is applied to the PDT-11/150, or the mode switch is set to the reset position, the low INIT L level will preset flip-flop E39A. The low DCLO L output is buffered to become BDCLO L, and clears both the flip-flop E39B and the interrupt request register E47. The low R1 (1) output of the E47, the WRESET(1) L signal to the LSI-11, will hold the microprocessor in the reset condition. The BDCLO L signal is also applied to gate E21A and the resulting low output is an input to gate E53. The high output of E53 is applied to the write/cascade U/C input of the timeout (T.O.) counter E52, which will reset the TERR (1) H output to a low level.

Flip-flop E39A will be cleared during a read operation of the 8085 I/O microprocessor when an address is decoded to generate a low I/O 8 L input to gate E3A. When the RD L input at E3A becomes low, the low-to-high transition at the output will clear E39A, and the BDCLO L output will become high to allow an interrupt request to be clocked into the interrupt register E47.

The 1.6 MA T.O. counter is clocked by the 19.8 KHz pulse inputs from the clock pulse generator (see Figure 4-7). The Z output of the counter will be low during the count and will become high for the duration of the 64th count. The counter is cleared by the high IN OR OUT H signal from the IPL logic; this will occur whenever the LSI-11 issues a high WD OUT H or WDIN H signal.

During normal operation, the low RESET OUT L signal from the 8085 will preset flip-flop E46A. The low WREPLY H output of E46A enables counter E52. When a high IN OR OUT H signal occurs, the counter will be cleared to zero and the count will start. The count will continue until flip-flop E46A is cleared by a low MRPLY L from the RAM module or by a low REPLY (0) H signal from the IPC logic. These signals indicate that the address issued by the LSI-11 is valid and has been received. Flip-flop E46A is clocked during the PH2 L interval of the clock pulse generator.

If a reply signal to gate E21B does not occur with the 1.6 MA interval of the T.O. counter E52, a high TERR (1) H signal will be generated from the Y output. The Z output of E52 will become low and result in a low WRESET (1) L pulse to the LSI-11 from the interrupt register E47. The LSI-11 will initiate a fast DIN cycle to determine if the PDT-11/150 is in the self-test or normal operating mode and if a timeout error has occurred.

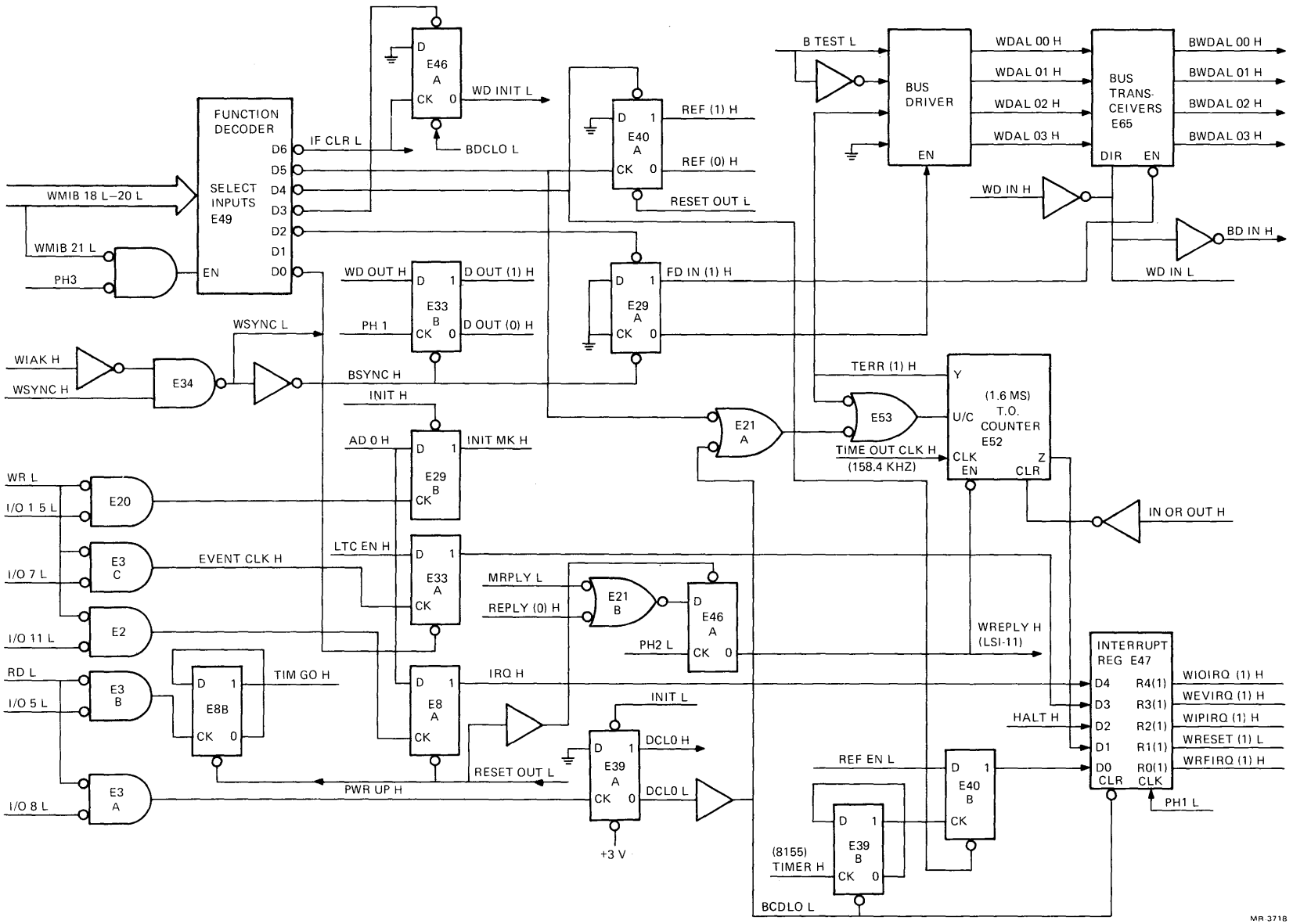


Figure 4-15 Function Control, Fast DIN and Interrupt Request Logic

Table 4-4 Function Decoder Outputs

WMIB				Decoded Output (L)	Description
21	20	19	18		
0	0	0	0	D0	Clears the line time clock (LTC) interrupt request flip-flop. Set by WRL and I/O 7 L from the 8085 when enabled by the LTC EN H signal from S1-1 on the Peripheral module.
0	0	0	1	D1	Not used.
0	0	1	0	D2	Sets a flip-flop that generates the FDIN (1) H signal, which is used to transfer the information on lines WDAL 00 H–03 H to the LSI-11 during the fast-data-in cycle. The LSI-11 monitors the BTEST L signal from the mode switch and the TERR (1) H signal from the T.O. counter to determine if a jump should occur to location 173000 or the μ ODT location.
0	0	1	1	D3	Presets the flip-flop that generates the WD INIT L signal, which causes a program reset to the 8085 I/O microprocessor.
0	1	1	0	D4	Presets the flip-flop that generates the REF (1) H signal and clears the flip-flop that enables the refresh pulses from the 8155 TIMER H to generate an LSI-11 interrupt. REF (1) H prevents LSI-11 device address decoding during the RAM refresh cycle and REF (0) H informs the RAM module that a refresh cycle is occurring.
0	1	0	1	D5	Clears the flip-flop that generates the REF (1) H signal as described in D4; also used to clear the T.O. counter during refresh cycles.
0	1	1	0	D6	Clears the flip-flop that generates the WD INIT L signal (refer to D3); also used to light the RUN indicator on the front panel. This output will occur on every memory access.
0	1	1	1	D7	Not used.
1	X	X	X		No operation.

X = high or low

The LSI-11 initiates the fast DIN cycle by issuing an address on the WMIB 18 L–21 L lines to the function decoder E49, which causes the D2 output to become low. This signal presets flip-flop E29A, and the low 0 output of E29A will enable the bus driver E56. The BTEST L input to a bus driver is applied directly to the WDAL 00 H line, inverted and then applied to the WDAL 01 H line. The BTEST L signal is from the mode switch on the rear panel and is low when the self-test mode has been selected. The TERR (1) H output from the T.O. counter is coupled to line WDAL 02 H and will be high after the T.O. counter has completed its count. The information on the WDAL 00 H–03 H lines is transferred through the bus transceiver E65 when enabled by a low FDIN (1) H from flip-flop E29A. Flip-flop E29A is cleared when the WSYNC H signal from the LSI-11 becomes low or when the interrupt acknowledge signal WIAK H becomes high as a result of an interrupt acknowledge. The WDIN H signal from the LSI-11 is inverted to WDIN L and selects the transfer direction of bus transceiver E65.

During a read operation of the 8085 I/O microprocessor, the low RD L signal and the low I/O 5 L output from the device decoder are gated at E3B, and the low-to-high output of E3B will set flip-flop E8, producing a high TIM GO H signal. This signal provides an interrupt request to the 8085 controller microprocessor on the Disk Controller module. At the end of the transaction, the RESET OUT L from the 8085 I/O microprocessor will clear flip-flop E8.

During write operations of the 8085 I/O microprocessor, the low WR L signal is gated at E20, E3C and E2. When a low I/O 1.5 L signal occurs, the low-to-high transition at the output of gate E20 will clock flip-flop E29B. This flip-flop is initially preset by the low INIT H signal when ac power is applied to the unit or when the mode switch is set to the RESET position. When the AD 0 H bus bit from the 8085 is low, flip-flop E29B will be cleared. The INIT MK H output of E29B connects to port B of the 8155 I/O port and RAM to specify a power-up or reset condition.

The low I/O 7 L output is gated with a low WR L at gate E3B, and the low-to-high EVENT CLK H output will set flip flop E33A when the LTC EN H signal is high. The LTC EN H signal is controlled by switch S1-2 on the Peripheral module. When LTC EN H is high, flip-flop E33B will be set to provide a high signal of the D3 input to the interrupt register E47. At the PH1 interval of the clock generator, the WEVIRQ (1) H signal will cause an event interrupt request to the LSI-11 microprocessor. This interrupt will occur, when enabled by S1-2, every 16.66 ms and will result in the incrementing of a counter every 16.66 ms. Flip-flop E33B is cleared by the LSI-11 with a low D0 output of the function decoder E49.

The low decoded output I/O 11 L is gated at E2 with a low WR L signal from the 8085 to set or clear flip-flop E8, depending on the level of the AD 0 H bus bit from the 8085 I/O microprocessor.

The high IRQ H output of E8, transferred to the D4 input of the interrupt register E47, results in a high WIOIRQ (1) H interrupt signal to the LSI-11. This will cause an I/O transfer to occur to or from the addressed memory or device location. When the 8085 I/O microprocessor detects a null character in the console terminal USART on the Peripheral module, a high HALT H signal to E47 will be generated by the DTR output of the USART. This occurs only when the self-test mode has been selected. The HALT H input will cause a WIPIRQ (1) H interrupt request to the LSI-11. The HALT H input will become high when the 8085 I/O microprocessor detects a null character in the console USART on the Peripheral module during the self-test mode of operation.

Flip-flop E33B is set during the clock generator pulse PH1 by a high WD OUT H signal from the LSI-11 microprocessor. This signal occurs during an output transfer and E33B generates a high DOUT (1) H (to the I/O device address decoders), which is used to generate a disk write interrupt to the 8259 interrupt control IC E27. The low DOUT (0) H signal, transferred to the RAM module, enables the data on the bus to be written into the addressed RAM locations. Flip-flop E33B is cleared when the WSYNC H signal from the LSI-11 becomes low or when the WIAK H signal from the LSI-11 becomes high during an interrupt acknowledge transfer.

The 8085 I/O microprocessor can be reset by program from the LSI-11. This occurs when the D3 output of the function decoder E49 becomes low and presets flip-flop E46B. The low WD INIT L signal is gated into the RESET IN input of the 8085. Flip-flop E46B is cleared by the BDCLO L input or by program when the D6 output of the function decoder has a low-to-high transition.

The RAM refresh cycle is controlled by the LSI-11 by a low D4 output of the function decoder E49, which presets flip-flop E40A and clears flip-flop E40B. The high REF (1) H signal from E40A prevents the generation of a high I/O SEL H signal from the I/O device decoder logic.

The low REF (0) H output of E40A is inverted on the RAM module and used to clock the toggle flip-flop, which selects 64 rows of the RAM.

The RAM refresh cycle is initiated by the TIMER H input to flip-flop E39B. This signal is a series of pulses from the 8155 internal clock, which will toggle flip-flop E39 B at a 500 μs rate. The low-to-high transition of the (1) output of E39B will set flip-flop E40B when the REF EN L input is high. This signal is controlled by switch S1-3 on the Peripheral module; when the switch is open, flip-flop E40B is enabled by a high level. When the switch is closed, the REF EN L signal will be low, which will prevent E40B from being set. The (1) output of E40B connects to the D0 input of the interrupt register E47. When the (1) output is high, a high WRFIRQ (1) H interrupt will occur at the LSI-11 to initiate the refresh interrupt cycle every 1.0 ms. When the refresh cycle is complete, the low DH output of function decoder E49 will clear flip-flop E40B with the next low-to-high transition of flip-flop E39B.

4.6 RAM MODULE FUNCTIONS (DWG. NO. 5413275)

The dynamic RAM module is the resident memory of the LSI-11 microprocessor. Figure 4-16 (Sheets 1 and 2) is a simplified diagram showing the function, control signals and logical elements of the RAM modules. The RAM provides storage for data and for the user's operating program or the RT11 operating system programs. The RAM is composed of 4K × 1-bit or 16K × 1-bit integrated circuits, depending on the memory module configuration.

The module includes a 1K × 16-bit ROM that contains the microcode for the bootstrap loader program. This program is used to load into RAM memory the operating system program contained on the flexible disk. The bank select decoder logic receives address information and decodes the information to select one of two banks within RAM or to select the bootstrap ROM. The row and column select logic controls the address information transfers to RAM.

Special logic is included on the module both to generate a reply signal when a valid memory address is recognized and to allow the information in the dynamic RAM to be refreshed periodically.

Data is transferred from RAM to the LSI-11 through the memory data buffer on the RAM module.

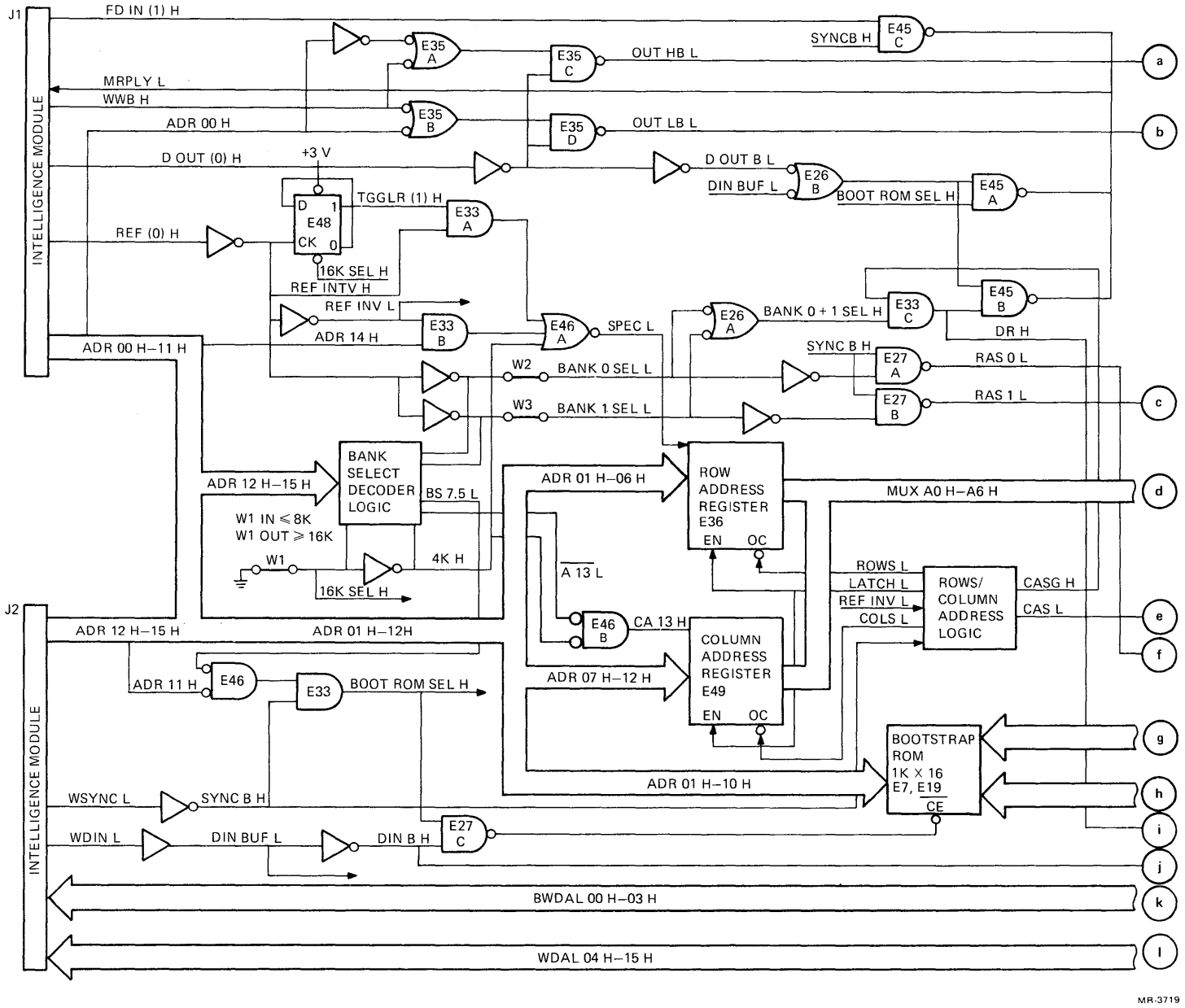


Figure 4-16 RAM Module, Simplified Function Diagram
(Sheet 1 of 2)

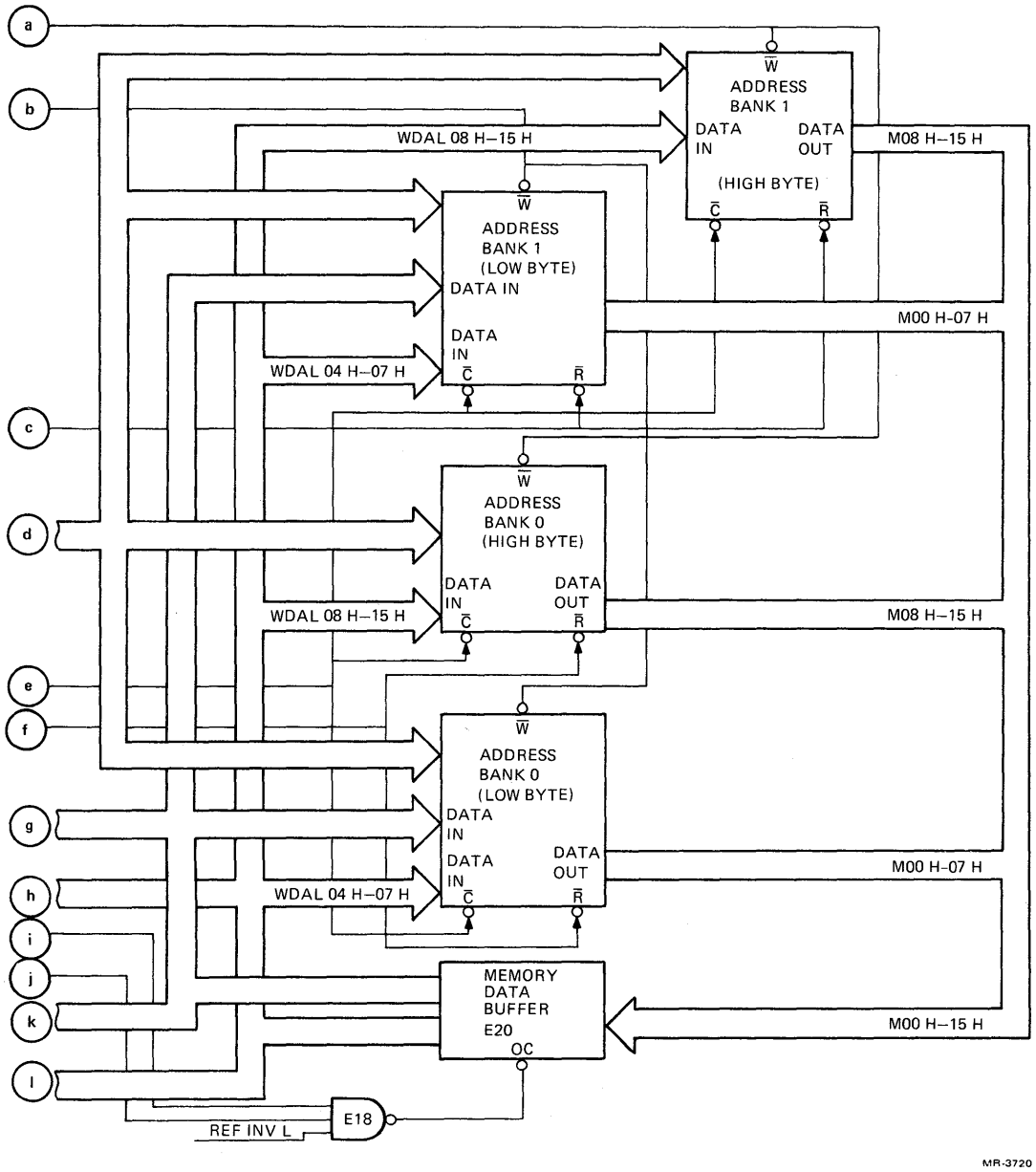


Figure 4-16 RAM Module, Simplified Function Diagram
(Sheet 2 of 2)

4.6.1 RAM Matrix Configurations

Figure 4-17 shows the three RAM matrix configurations available. The MST11-AB module consists of 32 (4K × 1-bit) ICs, with 16 ICs located in bank 0 and 16 ICs in bank 1. The MST11-AC module uses bank 0 only and contains 16 (16K × 1-bit) ICs. The MST11-AD has 32 (16K × 1 bit) ICs, with 16 ICs in bank 0 and 16 ICs in bank 1. During write operations, each location in a bank is addressable as an 8-bit high byte, an 8-bit low byte or a 16-bit word.

Table 4-5 lists the RAM modules available and the jumper lead configuration related to each memory matrix. Refer to Paragraph 5.4.3 for the physical location of the ICs and the jumper leads on the RAM module.

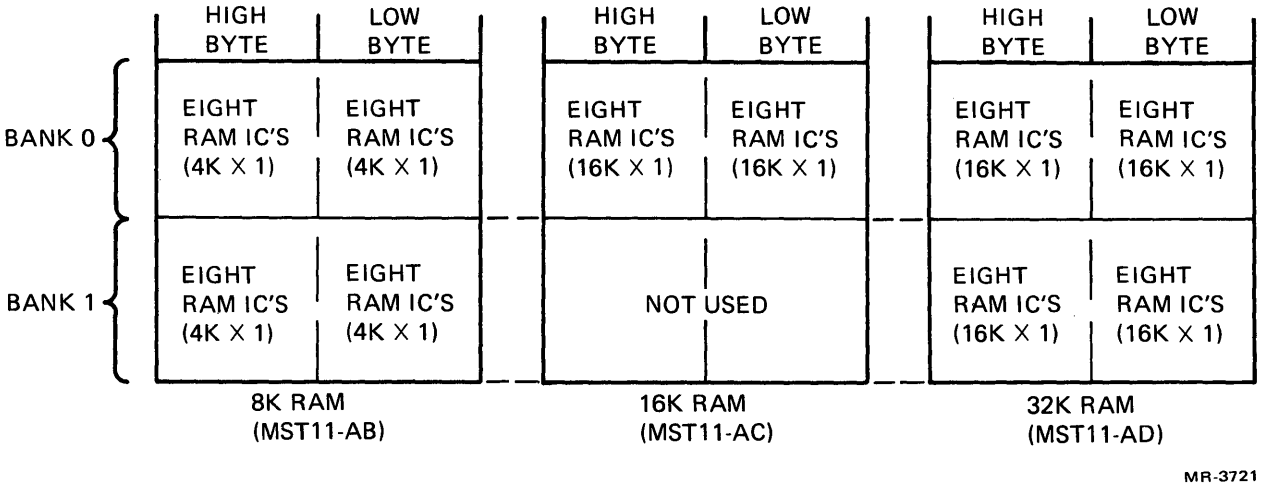


Figure 4-17 RAM Module, Memory Matrix Configurations

Table 4-5 RAM Module Designations and Jumper Configurations

RAM Module Designation	Words (16 bits)	Total ICs	Banks Used	Jumpers Installed W1	W2	W3
MST11-AB	8192	32 (4K × 1)	Bank 0 and Bank 1	IN	IN	IN
MST11-AC	16384	16 (16K × 1)	Bank 0	OUT	IN	OUT
MST11-AD	32768	32 (16K × 1)	Bank 0 and Bank 1	OUT	IN	IN

4.6.2 Address Bus Distribution

Memory address information from the LSI-11 is distributed on address lines ADR 00 H–15 H to select the locations within the dynamic RAM and bootstrap ROM. Address lines ADR 01 H–06 H are latched into the 7-bit row register E36 and address lines ADR 07 H–12 H are latched into the column register E49 by the LATCH L signal. This signal is produced by the WSYNC H output from the LSI-11 microprocessor. Register E39 also receives the SPEC L signal, which controls the selection of the upper 64 rows. Register E49 receives the CA 13 H signal to control the selection of the upper 64 columns when the 16K × 1-bit RAMs are installed on the module. During the refresh cycle, the SPEC L signal alternately selects the low and high 64 rows of RAM. The output of the row register E36 is multiplexed onto the MUX A 0 H–A 7 11 lines by the ROW L signal and the output of the column register E49 is multiplexed onto the same lines by the COLS L signal.

Address lines ADR 01 H–10 H are used to select locations within ROM. The addresses allocated in ROM are from locations 170000 to 173776. All addresses above this range are assigned to the peripheral devices and disk controller registers. The bootstrap ROM is enabled by the BOOT ROM SEL H signal generated during an input operation from the LSI-11 microprocessor. Address bit ADR 11 is monitored for a low condition, when the bank select decoder recognizes an address above 170000, and produces the BS 7.5 L signal.

Figure 4-18 shows the format of the address word used to select locations within the RAM and ROM. The address decoding is performed in conjunction with the configuration of the jumper leads W1 through W3 to select the desired memory bank.

4.6.3 Bank Select Decoder Logic

Figure 4-19 is a diagram of the bank select decoder logic used to select one or two memory banks of the RAM or to enable the bootstrap ROM. The installation of the jumper leads for each memory matrix is listed in Table 4-5.

In an 8K-word memory, sixteen 4K × 1-bit ICs are located in bank 0 and sixteen 4K × 1-bit ICs are in bank 1. Jumper leads W1, W2 and W3 are installed. Bank 0 is selected when address lines ADR 12 H–15 H are low. The output of gate E6A will be low and all inputs to gate E18 will be low. The high BS 7.5 L output is applied to gate E17B and to a gating circuit shown in Figure 4-16 (Sheet 1) that inhibits the selection of the bootstrap ROM E7 and E19. All inputs to gate E17B will be high to produce a high input to gate E32D. With jumper W1 installed, the 4K H signal to gate E32D will also be high, resulting in a low BANK 0 SEL L signal through jumper W2. This signal is inverted and gated with the SYNC B H signal at gate E27A to generate a low RAS 0 L signal. The RAS 0 L signal is used to latch the information on the MUX A 0 H–A 6 H bus into the internal row address registers of the bank 0 ICs and to enable the decoding of the row information.

Bank 1 is selected when address line ADR 13 is high and lines ADR 14 H and 15 H are low. The output of gate E6A be low and the B5 7.5 L output of gate E18 will remain high. With the high ADR 13 H line, all inputs to gate E17A will be high. Gate E17B will be disabled by the A13L input. The high output of E17A is gated at E32C with the high 4K H level to produce a low BANK 1 SEL L signal through jumper lead W3. The BANK 1 SEL L signal is inverted and gated with the SYNC B H signal to generate a low RAS 1 L output. This signal latches the information on the MUX A 0 H–A 6 H bus into the internal row address registers of the bank 1 ICs and enables the decoding of the row information. Refer to Figure 4-16 (Sheet 2).

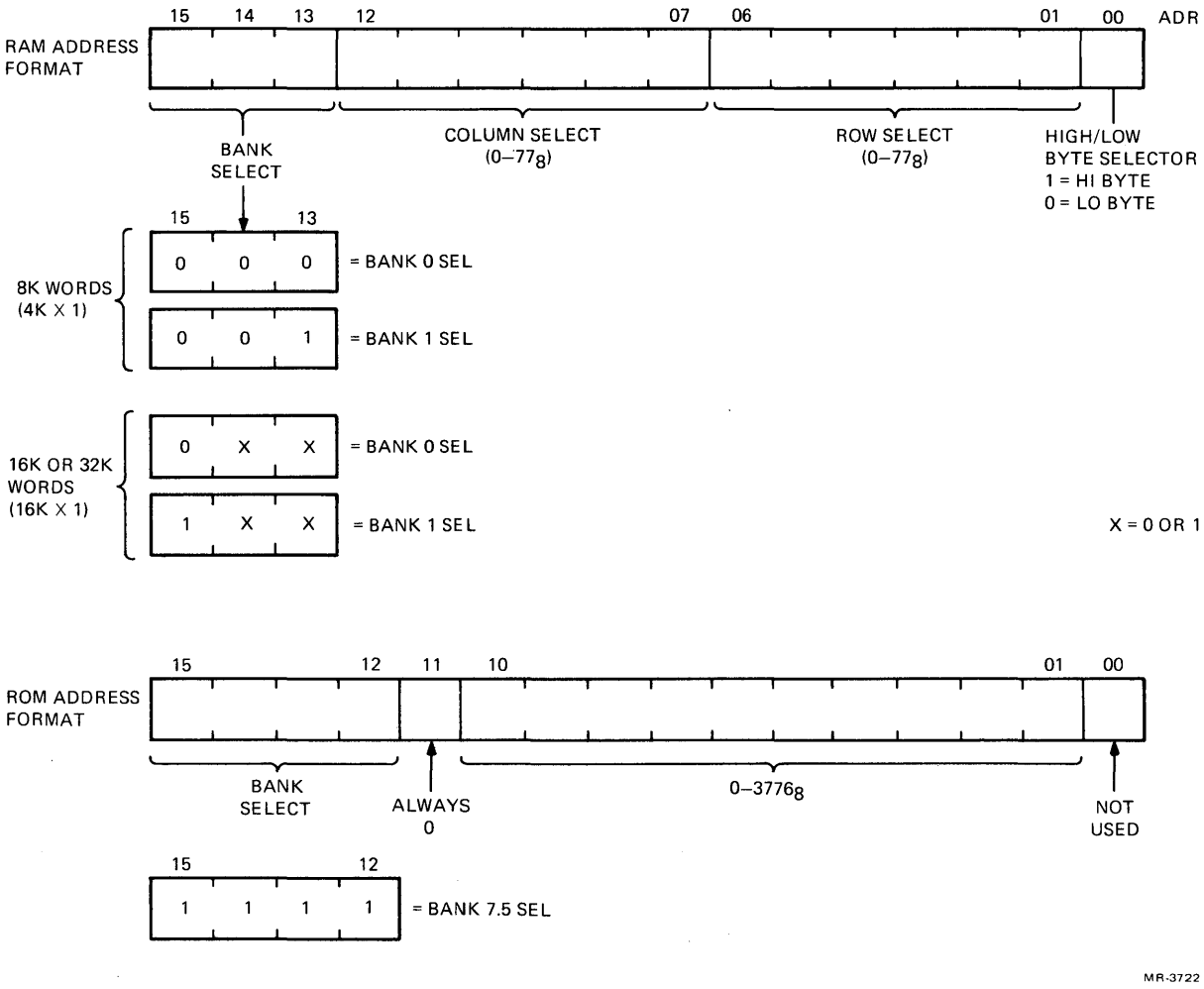


Figure 4-18 Memory Address Word Formats

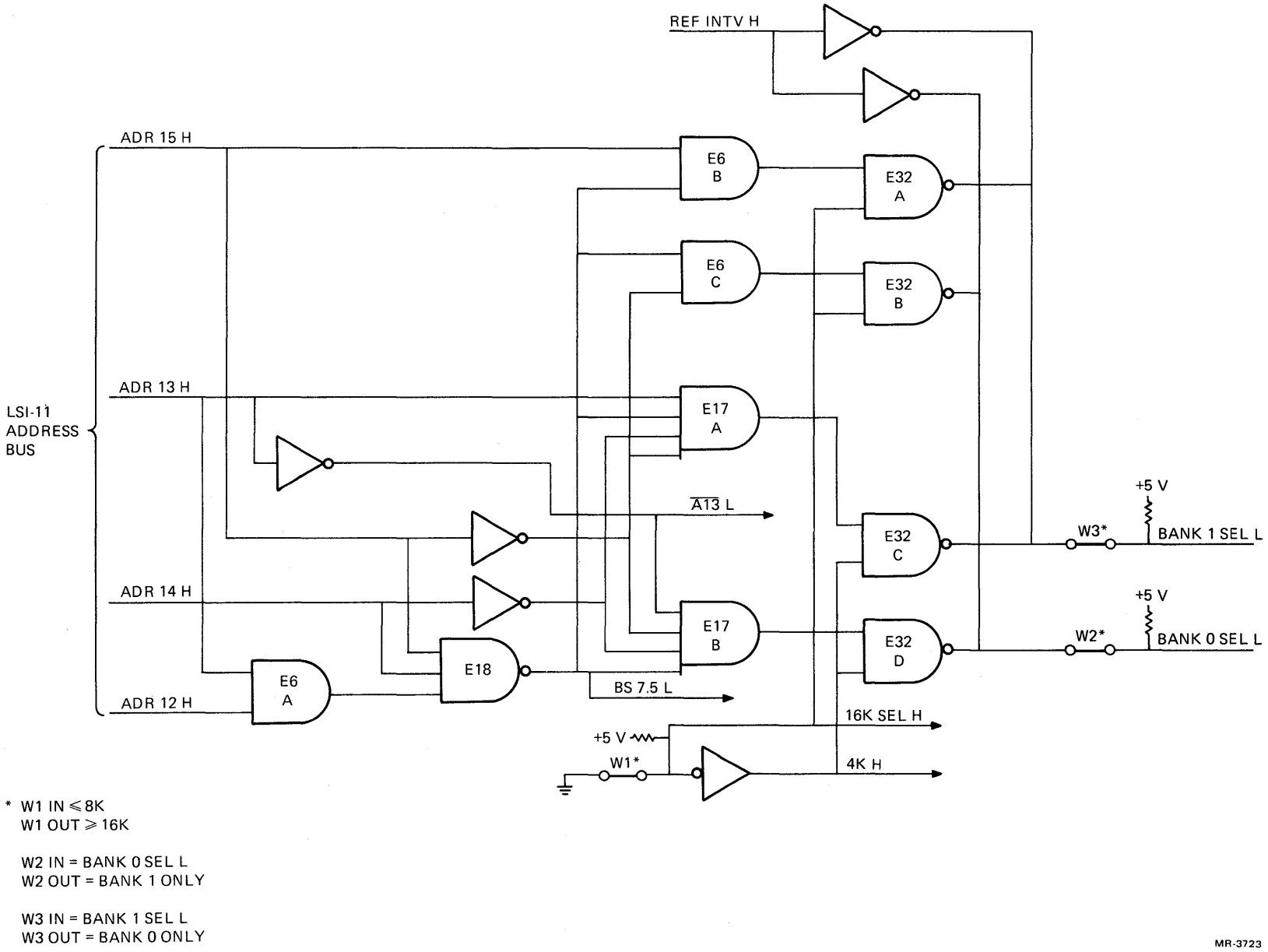


Figure 4-19 Bank Select Decoder Logic

A 16K-word memory is composed of sixteen 16K × 1-bit ICs in bank 0; therefore, only jumper lead W2 is installed. To select bank 0, address bit ADR 15 H is set low and inverted to a high input at gate E6C. The BS 7.5 L output of gate E18 is held high by the low ADR 15 H input. The BS 7.5 L output is applied to gate E6C, resulting in a high input to gate E32B. Jumper lead W1 is not installed; therefore, the 16K SEL H level to gate E32B is also high and results in a low BANK 0 SEL L signal through jumper W2. This selects the bank 0 rows in a manner similar to that described for the 8K-word memory. With jumper lead W3 not installed, the BANK 1 SEL L signal will be held high to disable the selection of the bank 1 ICs.

In a 32K-word memory, bank 0 and bank 1 are both required and jumper leads W2 and W3 are installed. Bank 0 is selected in a manner similar to that in the 16K-word memory and bank 1 is selected when address bit ADR 15 H becomes high. The high ADR 15 H line and the high BS 7.5 L signal are gated at E6B to produce a low output to gate E32A. Jumper W1 is not installed and the output of gate E32A produces the low BANK 1 SEL L signal through jumper lead W3. This results in the row address information on the MUX A 0 H–A 6 H bus to be transferred to the bank 1 ICs.

The ROM ICs E7 and E19 are enabled when address lines ADR 12 H–15 H are all high. Lines ADR 12 H and ADR 13 H are decoded by gate E6A to produce a high output. All three inputs to gate E18 will be high and the BS 7.5 L signal will be low; this inhibits the selection of bank 0 and bank 1. The BS 7.5 L output is gated with a low ADR 11 H signal (see Figure 4-16, Sheet 1) to produce a high output. This signal and the high SYNC B H signal will produce a high BOOT ROM SEL H output. During input commands from the LSI-11, a high DIN B H signal and the BOOT ROM SEL H signal will enable the information in bootstrap ROM to be transferred to the LSI-11.

4.6.4 Row/Column and Address Multiplexer Control Logic

Figure 4-20 shows the logic used to generate the row and column strobe signals and the signals that transfer the address information to the MUX A 0 H–A 6 H bus. This logic includes the time delays required to properly sequence the address information into the RAM.

Figure 4-21 is the timing diagram of the control signals. The address information from the LSI-11 is present on the ADR lines before the WSYNC L signal becomes low. The WSYNC H signal from the LSI-11 is gated with the WIAK H signal on the Intelligence module to become WSYNC L. The WSYNC L signal is inverted to SYNC B H. When the WSYNC L signal occurs, the information on lines ADR 01 H–06 H and the SPEC L input are latched into the row address register E36 and the information on lines ADR 07 H–12 H and the CA 13 H input are latched into the column address register E49 by the negative transition of the LATCH L signal. Because the ROWS L signal is initially low, the row address information will be transferred to the MUX A 0 H–A 6 H bus. The COLS L signal is initially high and prevents the column address transfer. The SYNC B H signal is also gated at E27A and E27B with the BANK 0 SEL L and BANK 1 SEL L signals to load the row address information into bank 0 and bank 1, respectively.

The LATCH L signal is inverted and applied to the RC network, which consists of capacitor C3 and resistors R16 and R17. The RC network connects to the (+) input of amplifier E29A and the (–) input of amplifier E29B. The remaining input to each amplifier is biased by a positive voltage. When the LATCH L signal becomes low, capacitor C3 will begin to charge to the positive voltage and E25 B will provide a low output after 80 ns. This output is inverted to produce a high ROWS L signal which inhibits the output of the rows register E36.

The ROWS L output is gated at E18 with a high SYNC B H and a REF INV L signal to produce a low COLS L output to the column address register E49. The COLS L signal transfers the high address information to the MUX A 0 H–A 6 H bus.

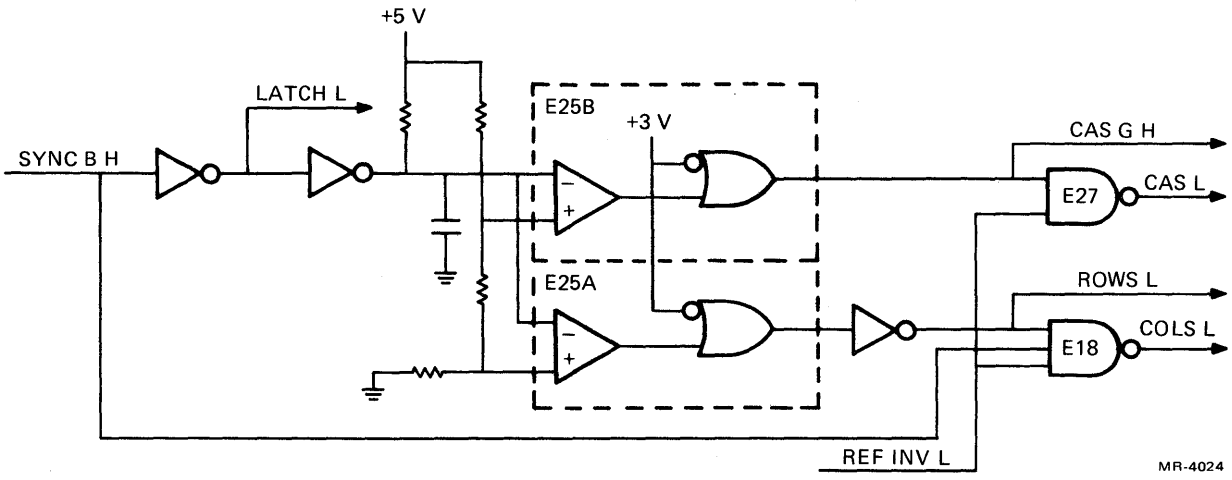


Figure 4-20 Row/Column and Address Multiplexer, Control Logic

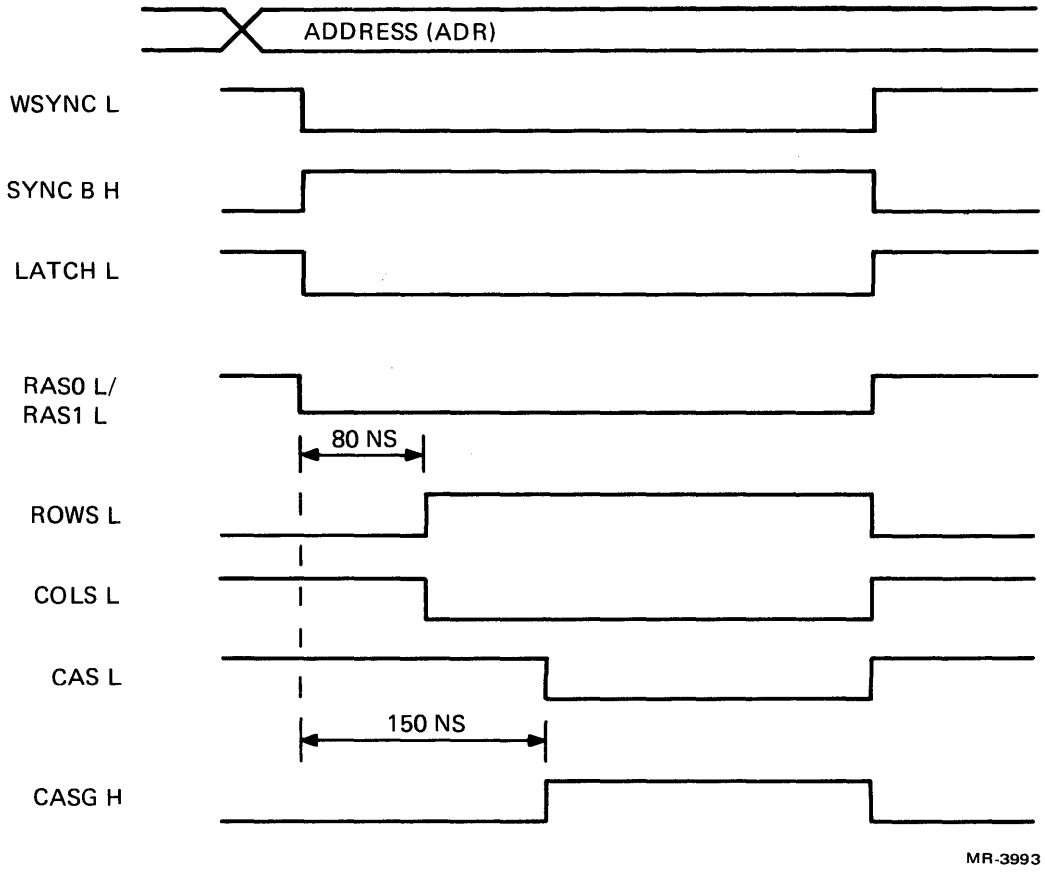


Figure 4-21 Row/Column and Address Multiplexer, Timing Diagram

After 150 ns, the CAS G H output of E25A will become high and gated with the BANK 0 + 1 SEL H input at gate E33C (see Figure 4-16, Sheet 1). The high DR H output of E33C is gated into E45B with the high output of E26 B to produce the low MRPLY L output, which is a reply to the LSI-11 microprocessor. The DIN BUF L input to gate E26B is the inverted WDIN H output of the LSI-11 microprocessor. The DOUT (0) H signal to gate E26B is generated by the WDOUT H signal from the LSI-11.

The high CASG H output of E25A is gated at E27 with a high REF INV L signal from the refresh logic to produce a low CAS L output. This signal strobes the column address information into the internal column registers of this RAM.

When the 4K × 1-bit RAM ICs are contained on the module, the seventh address bit, specified by the SPEC L input to the row address register E36, and the CA 13 H input to the column address register E49 are not required for the selection of the 64 columns and 64 rows in the RAM. The seventh address bit is held low by the 4K H high input to the gate that generates the SPEC L and CA 13 H signals.

When the RAM module contains 16K × 1-bit RAM ICs, jumper lead W1 is not installed, the 4K H output will be low, and the 16K SEL H signal will be high. With the 4K H output low, the CA 13 H output depends on the address bit ADR 13 H and the SPEC L output depends on the address bit ADR 14 H. This permits 128 rows and 128 columns to be addressed by the seven MUX bus lines.

4.6.5 RAM Refresh Logic

The dynamic RAM locations are refreshed a minimum of once every 2.0 ms to prevent the loss of data. The refresh cycle is initiated and controlled by the LSI-11 microprocessor, which will sequentially address 64 rows. When a row is addressed, the data information is recirculated and restored within the addressed row. When the 16K × 1-bit ICs are installed on the module, two refresh cycles are required to restore the data in 128 rows. Sixty-four rows are refreshed during the first 1.0 ms interval and 64 rows are refreshed during the second 1.0 ms interval.

When the refresh cycle is initiated, the REF (0) H signal will become low and the low-to-high transition will set flip-flop E38 (see Figure 4-16, Sheet 1) to produce a high TGGLR (1) H output. This signal is gated at E33A with the high REF INTV H input, which results in a low SPEC L output of E46A. The low SPEC L signal will enable the selection of the first 64 rows of RAM. When the next refresh cycle occurs flip-flop E38 will be cleared and the output of E33A will become low. The output of E33B will also be low due to the low REF INV L input and the 4K H signal will be low whenever 16K × 1-bit ICs are installed. With all inputs low, the SPEC L output of E46 will be high, allowing the addressing of the next 64 rows of RAM. When the 4K × 1-bit RAM ICs are used, the flip-flop E38 is held disabled by the low 16K SEL H line.

During the refresh cycle, bank 0 and bank 1 are selected by the inverted REF (0) H signal through jumper leads W2 and W3. The BANK 0 SEL L and BANK 1 SEL L outputs are gated with the BSYNC H signal to generate RAS 0 L and RAS 1 L, as during the read/write mode.

4.6.6 RAM Read or Write Operations

During write operations, the data to be written into the addressed location in RAM is on the BWDAL 00 H–03 H and WDAL 04 H–15 H bus. The DOUT (0) H signal from the Intelligence module is low when the LSI-11 requests an output transfer. The low DOUT (0) H signal is inverted and applied as an input to gates E35C and E35D. When a word transfer is specified, signal WWB H from the LSI-11 will be low at gates E35A and E35B. The high outputs are gated into E35C and E35D to produce a low OUT HB L signal and a OUT LB L signal. The OUT HB L signal will write the eight bits of information on the WDAL 07 H–15 H lines into the low byte RAM and the OUT LB L signal will write the eight bits of information on the BWDAL 00 H–03 H and WDAL 04 H–06 H into the high-byte RAM.

When signal WWB H is high, a byte transfer is specified and address bit ADR 00 H determines whether the information is a low or high byte. When ADR 00 H is high, the output of gate E35A will be high, resulting in a low OUT HB L signal. When ADR 00 H is low, the output of gate E35B will be high, with a low OUT LB L signal being the result.

During read operations, the DOUT (0) H signal from the Intelligence module will be high. When inverted, this signal will disable gates E35C and E35D, resulting in a high OUT HB L and OUT LB L signal. When the W inputs to the RAM ICs are high, the data from any addressed location within RAM will be loaded onto the M0 00 H–07 H or MO 08 H–15 H bus by the row and column strobes. This information is present at the memory data buffer E20 and is transferred to the BWDAL 00 H–03 H and WDAL 04 H–15 H bus by the DIN B H signal when a bank 0 or 1 has been selected and the refresh cycle has not been selected. The data buffer output is enabled by a low output of gate E18.

4.6.7 Reply Logic

The MRPLY L signal informs the LSI-11 that a valid memory address has been decoded. When the LSI-11 requests a fast-data-in cycle, the FD IN (1) H input to the RAM module (see Figure 4-16, Sheet 1) will become high and gated at E45C with the high SYNC B H signal to produce the low MRPLY L output. This low output is also produced by an input or output request from the LSI-11 when a bank 0 or 1 address has been selected in RAM or when the ROM is addressed. During a write instruction to RAM, the low DOUT (0) H signal becomes a low DOUT B L signal to gate E26B. The high output of E26B is gated at E45A with a high BOOT ROM SEL H signal to generate a low MRPLY L output. The BOOT ROM SEL H signal is high when a ROM address is decoded.

When bank 0 or 1 has been decoded, the BANK 0 + 1 SEL H output of gate E26A will be high and gated at E33C with a high CASG H signal from the row column select logic. The high DR H output of E33C is gated at E45B with the output signal from gate E26E to generate in a low MRPLY L output.

4.7 PERIPHERAL MODULE FUNCTIONS (DWG. NO. 5413269)

The Peripheral module provides the interface circuits required to transform the parallel information from the Intelligence module into serial information for transmission to the peripheral devices. During receive operations the serial data from the peripheral devices is transformed to parallel data. The module also contains the function switch (S1) used to select special functions, and the LED indicators, which are visible through the indicator panel on the front of the PDT-11/150.

Figure 4-22, a simplified diagram of the Peripheral module, shows the main functional elements, bus routing and control signals.

The module includes three programmable universal synchronous/asynchronous receiver transmitter (USART) ICs; three USARTs are included with the Cluster EIA option (DFT11-AB) and can be inserted into the 28-pin sockets provided on the module. Detailed information on the USARTs is contained in the *Signetics Bipolar/MOS Microprocessor Data Manual.*

Two 24-pin IC connector sockets are mounted on the edge of the module. A flat cable assembly attaches to connector J4 and transfers the signals between the console, modem, and printer USARTs and the level converters on the Standard EIA module. When the DFT11-AB option is installed, a flat cable assembly, included with the option, attaches to connector J3 and transfers the signals between the terminal no. 1, terminal no. 2 and terminal no. 3 USARTs and the level converters on the Cluster EIA module. Connector J5 is not installed on the module.

4.7.1 Information Transfers

Data, status and command information is transferred between the USARTs and the Intelligence module through the bus transceiver E13. The HD BAD 0–7 bus lines connect to the Intelligence module through the stacking connector J1. The PBAD 0–7 bus lines connect to the data input and output on each USART. The E13 bus transceiver is enabled by a low BLANK 1 H and a TIM FD SEL L signal from the I/O address decoder (see Figure 4-5). The RD L signal from the 8085 I/O microprocessor controls the transfer direction of the information through E18. During a read operation, a low RD L signal will cause the information on the PBAD 0–7 bus to be transferred to the HDBAD 0 H–7 H bus. During a write operation, the RD L signal will be high and the information will be transferred from the HDBAD 0 H–7 H bus to the PBAD 0 H–7 H bus.

Each of the USARTs has internal registers that are accessed during read and write operations to transfer data, status and control information. Address lines A 8 H–10 H from the 8085 I/O microprocessor at connector J2 select the register and specify a read or write transfer. The register and addressing information is listed in Table 4-6. Address line A 10 H specifies a read or write operation to the register selected.

Six I/O select lines from the I/O select decoder on the Intelligence module (see Figure 4-5) are used to enable the six USARTs. The USARTs are enabled by a low CE input, which occurs when the 8085 I/O microprocessor issues a read or write command. The low RD L or WR L input is gated at E3B to produce a low RD/WD L output, which is distributed to the enable gates of each USART. Signal I/O 2 L is gated at E7C to enable the printer USART E9. When the Cluster option is installed, signal I/O 12 L is gated at E8H to enable the terminal no. 1 USART E2; signal I/O 13 L is gated at E8B to enable the terminal no. 2 USART; and signal I/O 14 L is gated at E8C to enable the terminal no. 3 USART E10.

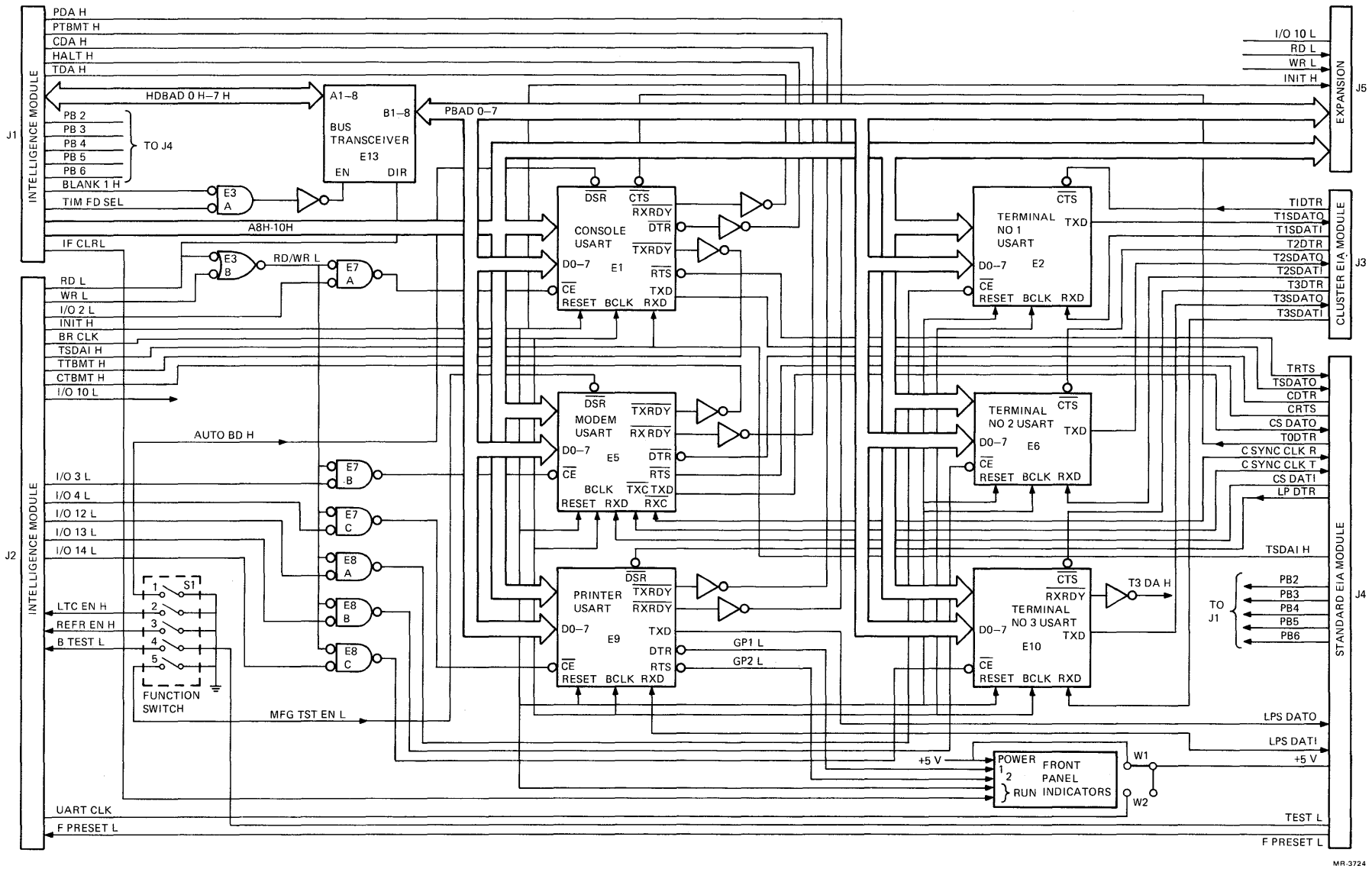


Figure 4-22 Peripheral Module, Simplified Function Diagram

Table 4-6 USART Register Addressing

Address Line A10	A9	A8	Function
L	L	L	Read receive holding register
H	L	L	Write transmit holding register
L	L	H	Read status register
H	L	H	Write SYN1, SYN2 or DLE register
L	H	L	Read mode register 1 and 2
H	H	L	Write mode register 1 and 2
L	H	H	Read command register
H	H	H	Write command register

L = low level
H = high level

One of two jumper leads, W1 or W2, is installed on the Peripheral module, depending on the module's use. On the PDT-11/150 series units, jumper lead W1 is installed and W2 is removed. This configuration supplies + 5 V dc to the Standard EIA module through a flat cable assembly. On the PDT-11/110 and PDT-11/130 series units, jumper lead W2 is installed and jumper W1 is removed. This provides a 158.4 KHz square wave signal (UART CLK) to the VT100.

4.7.2 Standard Device USARTs

The standard device USARTs are the console, E1, the modem E5, and the printer E9. The DSR input to the console USART is connected to the function switch S1-1. When the switch is open (OFF), the high input to DSR will allow the baud rate of the console terminal to be monitored under program control and the control register in the console USART to be programmed to accept the console terminal baud rate automatically. When switch S1-1 is closed (ON), the autobaud function is disabled by the low (ground) DTR input to E1.

The DTR input to the modem USART connects to the function switch S1-5. When the switch is closed (ON), the low DTR input selects the manufacturing mode of operation, which allows the external testing of the PDT-11/150 unit without operator response from the console terminal. When the switch is open (OFF), the manufacturing mode is disabled.

The DTR and RTS outputs of the printer USART are programmable, through the internal registers, to light the (1) and (2) indicators appearing on the front panel of the PDT-11/150 unit.

Table 4-7 lists the signals for the console USART and their functions, Table 4-8 for those of the modem USART, and Table 4-9 for those of the printer USART.

Table 4-7 Console USART Signals

USART Signal	PDT-11/150 Signal	Function
BCLK	BRCLK	A 5.0688 MHz square wave input from the clock pulse generator on the Intelligence module. Connects to USART baud rate generator clock.
RESET	INIT H	A master reset input from the Intelligence module to clear all USART registers when ac power is applied to the PDT-11/150, or when the mode switch is set to the RESET position.
$\overline{CE}$	L = enable	Chip enable – Input to enable the console USART when I/O 2 L occurs during a read or write operation.
D0–D7	PBAD 0–7	Bidirectional data bus for parallel transfer with the Intelligence module.
A0–A1	A8 H, A9 H	Register address – Input to select the USART internal registers (see Table 4-6).
$\overline{R}/W$	A10 H	Read or write selection (see Table 4-6).
$\overline{DSR}$	AUTO BAUD H	Data Set Ready – Input from function switch S1-1. Complement appears in USART status register SR7. Monitored under program control to determine if autobaud function has been selected.
$\overline{DTR}$	HALT H	Data terminal ready – Output that is the complement of the USART command register bit CR1. Programmed to cause an interrupt request to the LSI-11 on the Intelligence module.
$\overline{RTS}$	TRTS	Request to send – Output that is the complement of USART command register bit CR5. Indicates to the terminal that USART has data for transmission.
RXD	TSDATI H	Receive data – Serial data input from the terminal to USART and to the SID input of the 8085 I/O microprocessor. Used by the 8085 to determine the baud rate of data transmission during the autobaud function.
$\overline{RXRDY}$	TDA H	Receive ready – Output that is complement of the USART status register bit SR1. Causes an interrupt request to the 8085 I/O microprocessor where the USART data holding register is ready for transmission to the Intelligence module.
$\overline{TXRDY}$	TTBMT H	Transmit ready – Output that is the complement of the USART status register bit SR0. Causes an interrupt request to the 8085 I/O microprocessor when the USART transmit data holding register is ready to accept data.
$\overline{CTS}$	T0DTR	Clear to send – Input from the terminal indicating that the terminal is ready to receive data.
TXD	TSDATO	Transmit data – Serial data output to the console terminal.

Table 4-8 Modem USART Signals

USART Signal	PDT-11/150 Signal	Function
BCLK	BRCLK	A 5.0688 MHz square wave input from the clock pulse generator on the Intelligence module. Connects to USART baud rate generator clock.
RESET	INIT H	A master reset input from the Intelligence module to clear all USART registers when ac power is applied to the PDT-11/150.
$\overline{CE}$	L = enable	Chip enable – Input to enable the console USART when I/O 3 L occurs during a read or write operation.
D0–D7	PBAD 0–7	Bidirectional data bus for parallel transfer with the Intelligence module.
A0–A1	A8 H,A9 H	Register address – Input to select the internal registers of the USARTS (see Table 4-6).
$\overline{R}$/W	A10 H	Read or write select (see Table 4-6).
$\overline{DSR}$	MFG TST EN L	Data set ready – Input from function switch S1-5. The complement appears in USART status register SR7. Monitored under program control to determine if the manufacturing test function is enabled.
DTR	CDTR	Data terminal ready – Output that is the complement of the USART command register bit CR1. Controlled by program to indicate to the modem that the PDT-11/150 is ready for communication.
$\overline{RTS}$	CRTS	Request to send – Output that is the complement of USART command register bit CR5. Controlled by program to indicate to the modem that the USART has data for transmission.
RXD	CSDATI	Receive data – Serial data input from modem to USART.
$\overline{RXRDY}$	CDA H	Receive ready – Output that is complement of USART status register bit SR1. Causes an interrupt request to the 8085 I/O microprocessor when the USART data holding register is ready for transmission to the Intelligence module.
$\overline{TXRDY}$	CTBMT H	Transmit ready – Output that is the complement of the USART status register bit SR0. Causes an interrupt request to the 8085 I/O microprocessor when the USART transmit data holding register is ready to accept data.
TXD	CS DATO	Transmit data – Serial data output to the console terminal.
$\overline{RXC}$	CSYNC CLK R	Receiver clock – Input to USART to control the rate at which the characters are to be received as programmed by the USART mode register.
$\overline{TXC}$	CSYNC CLK T	Transmit clock – Input to USART to control the rate at which the characters are transmitted as programmed by the USART mode register.

Table 4-9 Printer USART Signals

USART Signal	PDT-11/150 Signal	Function
BCLK	BRCLK	A 5.0688 MHz square wave input from the clock pulse generator on the Intelligence module. Connects to USART baud rate generator clock.
RESET	INIT H	A master reset input from the Intelligence module to clear all USART registers when ac power is applied to the PDT-11/150.
$\overline{CE}$	L = enable	Chip enable – Input to enable the console USART when I/O 4 L occurs during a read or write operation.
D0–D7	PBAD 0–7	Bidirectional data bus for parallel transfer with the Intelligence module.
A0–A1	A8 H, 9H	Register address – Input to select the USART internal registers (see Table 4-6).
$\overline{R}$/W	A10 H	Read or write select (see Table 4-6).
$\overline{DSR}$	LP DTR	Data Set Ready – Input from the line printer to indicate that the printer is ready to receive data.
$\overline{DTR}$	GP1 L	Data Terminal Ready – Output that is the complement of the USART command register bit CR1. Controlled by program to cause the (1) indicator on the front panel to light.
$\overline{RTS}$	GP2 L	Request to send – Output that is the complement of USART command register bit CR5. Controlled by program to cause the (2) indicator on the front panel to light.
RXD	LPS DATI	Receive Data – Serial data input from terminal to USART.
$\overline{RXRDY}$	PDA H	Receive Ready – Output that is the complement of USART status register bit SR1. Causes an interrupt request to the 8085 I/O microprocessor when the USART data holding register is ready for transmission to the Intelligence module.
$\overline{TXRDY}$	PTBMT H	Transmit Ready – Output that is the complement of the USART status register bit SR0. Causes an interrupt request to the 8085 I/O microprocessor when the USART transmit data holding register is ready to accept data.
TXD	LPS DATO	Transmit Data – Serial data output to the line printer terminal.

4.7.3 Optional Device USARTs

Three device USARTs are included with the DFT11-AA Cluster EIA option and can be installed on the Peripheral module to allow the PDT-11/150 to operate with three additional terminals. The terminal no. 1 USART E2, terminal no. 2 USART E6, and terminal no. 3 USART E10 connect to the peripheral devices through the connectors on the Cluster EIA module. These USARTs are programmed in a similar manner to the console USART. Table 4-10 lists and defines the signals used with the terminal no. 1, terminal no. 2 and terminal no. 3 USARTs.

Table 4-10 USART Signals for Terminals No. 1 – No. 3

USART Signal	PDT-11/150 Signal	Function
BCLK	BRCLK	A 5.0688 MHz square wave input from the clock pulse generator on the Intelligence module. Connects to the USART baud rate generator clock.
RESET	INIT H	A master reset input from the Intelligence module to clear all USART registers when ac power is applied to the PDT-11/150.
$\overline{CE}$	L = enable	Chip enable – Input to enable the console USART when I/O 12 L (terminal 1), I/O 13 L (terminal 2) or I/O 14 L (terminal 3) occurs during a read or write operation.
D0–D7	PBAD 0–7	Bidirectional data bus for parallel transfer with the Intelligence module.
A0–A1	A8 H, A9 H	Register address – Input to select the USART internal registers (see Table 4-6).
R/W	A10 H	Read or write selector (see Table 4-6).
RXD	T1SDATI T2SDATI T3SDATI	Receive data – Serial data input from terminal to USART.
TXD	T1SDATO T2SDATO T3SDATO	Transmit data – Serial data output from USART to terminal.
$\overline{CTS}$	T1DTR T2DTR T3DTR	Clear to send – Input from the teminal indicating that the terminal is ready to receive data.

4.7.4 Front Panel Indicators

Figure 4-23 is a simplified diagram of the logic and signals used to control the front panel indicators on the Peripheral module. These indicators are mounted on the edge of the module and are displayed through the transparent bezel of the indicator panel.

The GP1 L and GP2 L outputs from the printer USART are used to control the (1) and (2) indicators as shown. During the self-test mode, the lights indicate the performance of specific functions, and during normal operation they can be controlled by the user program. A low output on the GP1 L line will light the (1) indicator and a low output on the GP2 L will light the (2) indicator.

The RUN indicator is lighted by the IF CLR L signal from the LSI-11 special function logic on the Intelligence module. When the LSI-11 is performing read or write operations, the high-to-low transition of the IF CLR L signal will trigger the one-shot multivibrator E14 at a rate causing the indicator to appear continually lighted. The high INIT H signal clears E14 when ac power is applied to the PDT-11/150 unit.

The POWER indicator, connected between +5 V dc and ground, will light whenever the +5 V dc is present in the unit.

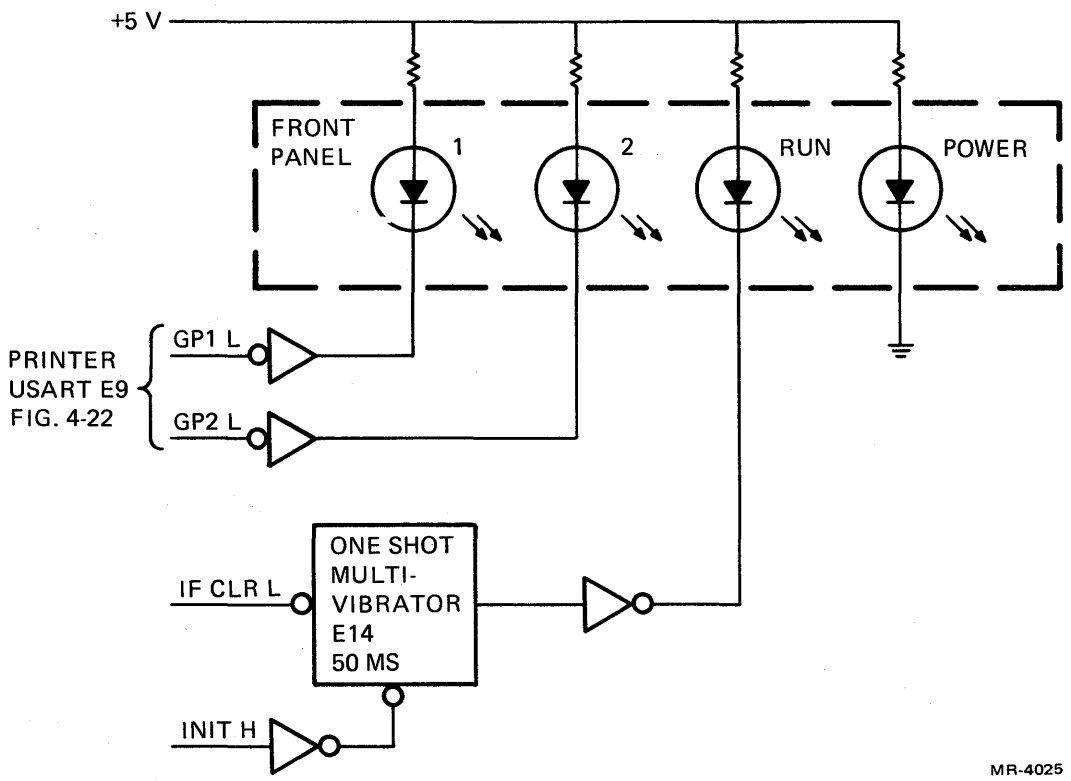


Figure 4-23 Front Panel Indicator Logic, Simplified Diagram

4.7.5 Function Switch Selections

The function switch S1 is shown in Figure 4-22, with its positions and their functions listed in Table 4-11. Refer to Chapter 6 for the program effects of the switch positions. In the closed position, all switch banks are connected to ground except switch bank S1-4.

4.8 EIA/TTL LEVEL CONVERTERS

The Standard EIA module and the Cluster EIA module include the circuits necessary to convert the level of the signals transferred between the PDT-11/150 and the external peripheral devices. The PDT-11/150 operates with TTL/DTL-compatible levels and the devices communicate with signal levels that are EIA-compatible, according to the specifications included in the Electronic Industries Association's *EIA Standard, RS-232-C.* Refer to this specification for detailed signal requirements for interfacing data terminal equipment to data communications equipment.

Each of the modules contain a series of line drivers and receivers that perform the signal conversions. The EIA input levels from a device to the receivers range from –15 V to +15 V maximum, and the EIA output levels range from –5 V to +12 V. All TTL levels are approximately 0 V to +3 V.

Also mounted on each module are three 22-pin connectors to which the device cables can be attached.

Table 4-11 Function Switch (S1) Signals

Switch Bank	Signal	Function
S1-1	AUTO BD H	ON – Provides a low level to the DSR input of the console USART to disable the autobaud function. OFF – Enables the autobaud function.
S1-2	LTC EN H	ON – Provides a low level to the function logic of the LSI-11 microprocessor to disable the event interrupt request WEV-IRQ (1) H. OFF – Enables the event interrupt request to the LSI-11.
S1-3	REFR EN H	ON – Provides a low level to the function logic of the LSI-11 to disable the refresh interrupt request WRFIRQ (1) H. OFF – Enables the refresh interrupt request.
S1-4	BTEST L	ON – Allows the S1 mode switch on the Standard EIA module (rear panel) to select the test mode of operation. OFF – Prevents the test mode from being selected.
S1-5	MFG TST EN L	ON – Provides a low level to the DSR input of the modem USART to enable the manufacturing test function. OFF – Disables the manufacturing test function.

4.8.1 Standard EIA Module Functions (DWG. NO. 5413267)

Figure 4-24, a simplified diagram of the Standard EIA module, shows the signals and their direction of transfer. Connectors J1, J2 and J3 are 25-pin cable connectors for the device cable, and connector J4 is a 24-pin IC connector for the flat cable assembly G2 that connects to the Peripheral module. Also mounted on the module is the mode switch S1, which is used to select the self-test mode (TEST position), the normal program operating mode (NORMAL position) and the reset function (RESET position). When the switch is set to the TEST position, the signal ground will be present on the TEST L line; this line connects to switch S1-4 on the Peripheral module. When the switch is closed, a low BTEST L signal will appear at the 8155 I/O port and RAM on the Intelligence module.

When switch S1 is in the momentary RESET position, the signal ground will be present on the FPRESET L line. This signal is transferred through the Peripheral module to the RC network, which controls the RESET IN level to the 8085 I/O microprocessor.

Table 4-12 lists and defines the interface signals for the console, modem and printer terminals.

Table 4-12 Standard EIA Module Interface Signals

Device Signal Name	25-Pin Connector	PDT-11/150 Signal	24-Pin IC Connector	Description
Console				
TERM RCV DATA	J1-3	TS DATO	J4-1	Output - The EIA serial data to the console.
TERM XMIT DATA	J1-2	TS DATI	J4-3	Input - The EIA serial data from the console.
TERM RDY	J1-20	T DTR	J4-2	Input - The status of the data-terminal-ready indicator from the console.
Chassis GND	J1-1	SIGNAL GND	J4-12	Chassis and logic ground.
Signal GND	J1-7			
Printer				
LP RCV DATA	J2-3	LPS DATO	J4-5	Output - The EIA serial data to the printer.
LP XMIT DATA	J2-2	LPS DATI	J4-7	Input - The EIA serial data from the printer.
LP RDY	J2-20	LP DTR	J4-6	Input - The status of data-terminal-ready indicator from the printer.

Table 4-12 Standard EIA Module Interface Signals (Cont.)

Device Signal Name	25-Pin Connector	PDT-11/150 Signal	24-Pin IC Connector	Description
Chassis GND	J2-1	SIGNAL	J4-12	Chassis and logic ground.
Signal GND	J2-7	GND		
Modem				
MODEM RCV DATA	J3-2	CS DATO	J4-9	Output - The EIA serial data to the modem.
MODEM XMIT DATA	J3-3	CS DATI	J4-11	Input - The EIA serial data from the modem.
SEC CARRIER DETECT	J3-12	PB2	J4-13	Input - The status of the secondary-carrier-detect indicator from the modem.
DATA SET RDY	J3-6	PB3	J4-14	Input - The status of the data-set-ready indicator from the modem.
CARRIER DETECT	J3-8	PB4	J4-15	Input - The status of the carrier-detect indicator from the modem.
PRI CTS	J3-5	PB5	J4-16	Input - The status of the primary clear-to-send indicator from the modem.
RING	J3-22	PB6	J4-17	Input - The status of the ring indicator from the modem.
SEC RTS	J3-11	TRTS	J4-10	Output - The secondary request-to-send signal to the modem.
PRI RTS	J3-4	CRTS	J4-8	Output - The request-to-send signal to the modem.

Table 4-12 Standard EIA Module Interface Signals (Cont.)

Device Signal Name	25-Pin Connector	PDT-11/150 Signal	24-Pin IC Connector	Description
DTR	J3-6	CDTR	J4-4	Output – The data-terminal-ready signal to the modem.
SYNC CLK R	J3-17	CSYNC CLK R	J4-21	Input – The receiver clock pulses for synchronous modem communications.
SYNC CLK T	J3-15	CSYNC CLK T	J4-19	Input – The transmitter clock pulses for synchronous modem communications.
Chassis GND	J3-1	SIGNAL	J4-12	Chassis and logic ground.
Signal GND	J3-7	GND		

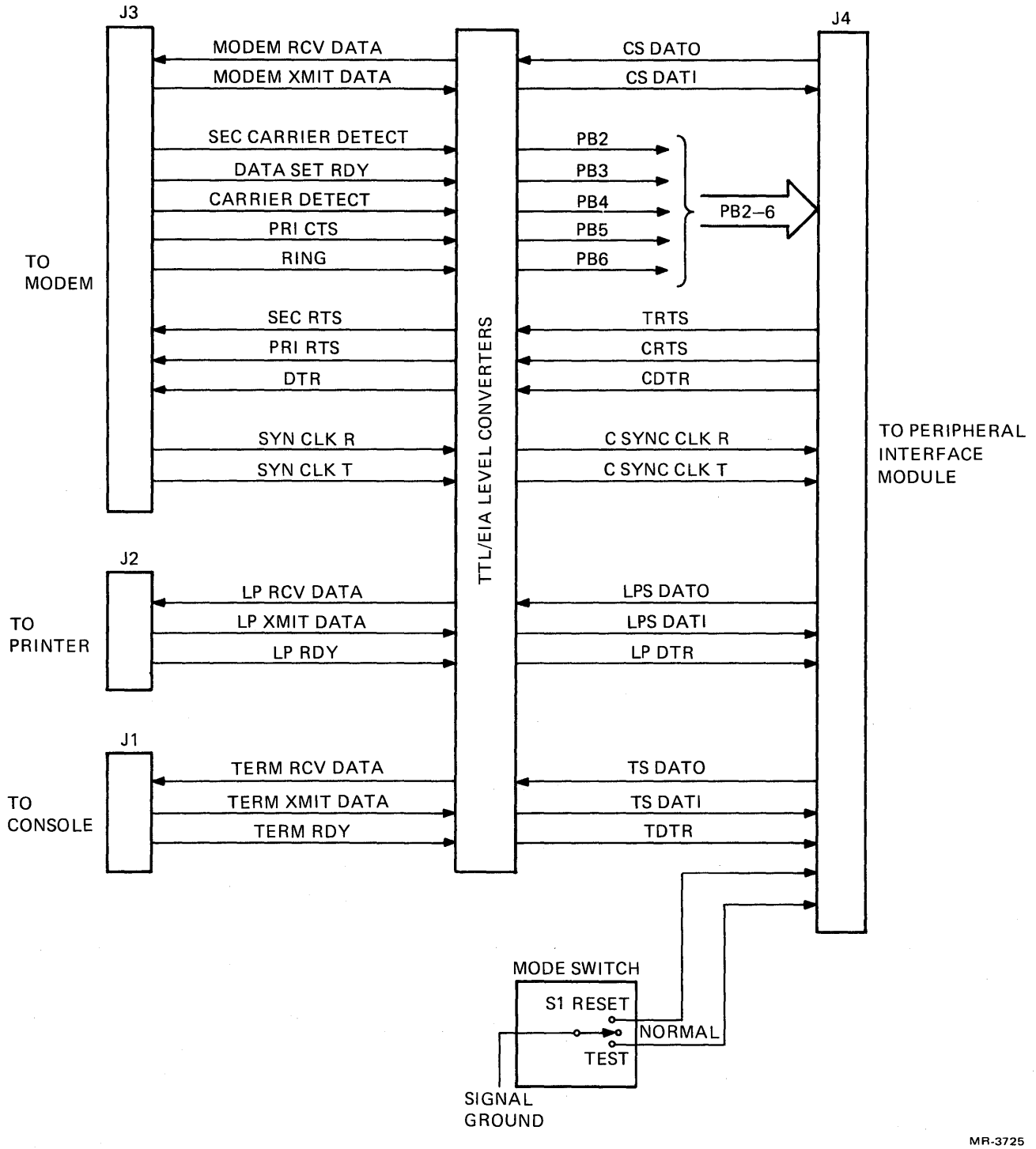


Figure 4-24 Standard EIA Module, Simplified Diagram

4.8.2 Cluster EIA Module Functions (DWG. NO. 5413427)

Figure 4-25, a simplified diagram of the Cluster EIA module, shows the interface signals and their direction of transfer. This module is included with the DFT11-AB option. Connectors J1, J2 and J3 are 25-pin cable connectors for the device cables, and connector J4 is a 24-pin IC connector for the flat cable assembly G3 that connects to the Peripheral module.

Table 4-13 lists and defines the interface signals for the terminal no. 1, terminal no. 2 and terminal no. 3 devices that connect to the module.

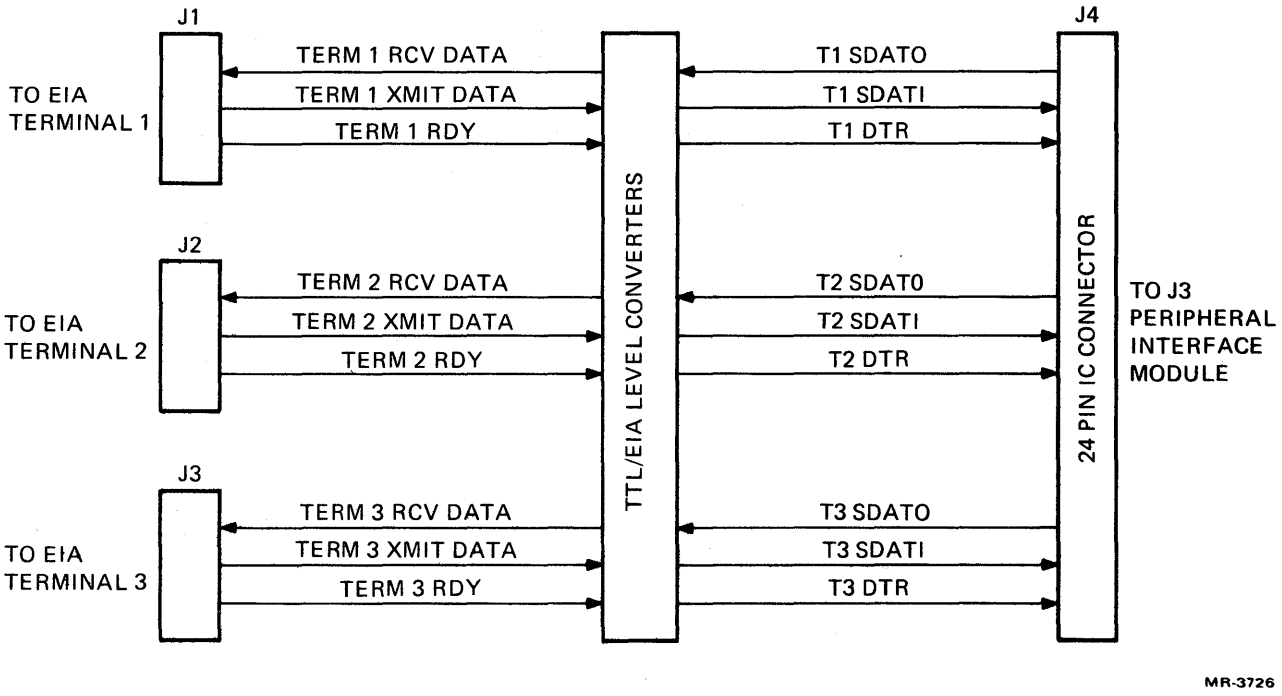


Figure 4-25 Cluster EIA Module, Simplified Diagram

Table 4-13 Cluster EIA Module Interface Signals

Device Signal Name	25-Pin Connector	PDT-11/150 Signal	24-Pin IC Connector	Description
Terminal No. 1				
TERM 1 RCV DATA	J1-3	T1 SDATO	J4-1	Output – The EIA serial data to terminal no. 1
TERM 1 XMIT DATA	J1-2	T1 SDATI	J4-3	Input – The EIA serial data from terminal no. 1.
TERM 1 RDY	J1-20	T1 DTR	J4-2	Input – The status of the data-terminal-ready indicator from terminal no. 1.

Table 4-13 Cluster EIA Module Interface Signals (Cont.)

Device Signal Name	25-Pin Connector	PDT-11/150 Signal	24-Pin IC Connector	Description
Chassis GND	J1-1	SIGNAL	J4-18	Chassis and logic ground.
Signal GND	J1-7	GND		
Terminal No. 2				
TERM 2 RCV DATA	J2-3	T2 SDATO	J4-5	Output - The EIA serial data to terminal no. 2.
TERM 2 XMIT DATA	J2-2	T2 SDATI	J4-7	Input - The EIA serial data from terminal no. 2.
TERM 2 RDY	J2-20	T2 DTR	J4-6	Input - The status of the data-terminal-ready indicator from terminal no. 2.
Chassis GND	J2-1	SIGNAL	J4-18	Chassis and logic ground.
Signal GND	J2-7	GND		
Terminal No. 3				
TERM 3 RCV DATA	J3-3	T3 SDATO	J4-9	Output - The EIA serial data to terminal no. 3.
TERM 3 XMIT DATA	J3-2	T3 SDATI	J4-11	Input - The EIA serial data from terminal no. 3.
TERM 3 RDY	J3-20	T3 DTR	J4-23	Input - The status of the data-terminal-ready indicator from terminal no. 1.
Chassis GND	J3-1	SIGNAL	J4-18	Chassis and logic ground.
Signal GND	J3-7	GND		

4.9 FLEXIBLE DISK DESCRIPTION

The flexible disk is the medium used in the disk drives to load program information and store data. The disk is composed of a mylar base coated with oxide on both sides and enclosed in a plastic envelope. Figure 4-26 shows the disk in its envelope and identifies important characteristics of the medium.

At the center of the disk is the drive spindle hole. When the disk is inserted into the drive, a centering cone presses the disk against the spindle and causes the disk to rotate with the spindle. An aperture in both sides of the disk envelope permits the read/write head to make physical contact with the oxide surface of the disk. An index hole, also in both sides of the plastic envelope, is aligned with a single hole through the disk. When the disk is rotating, the position of the hole is sensed and used for synchronization when reading or writing information on a track. The outside track of the disk is identified as track 00 and the innermost track is track 76.

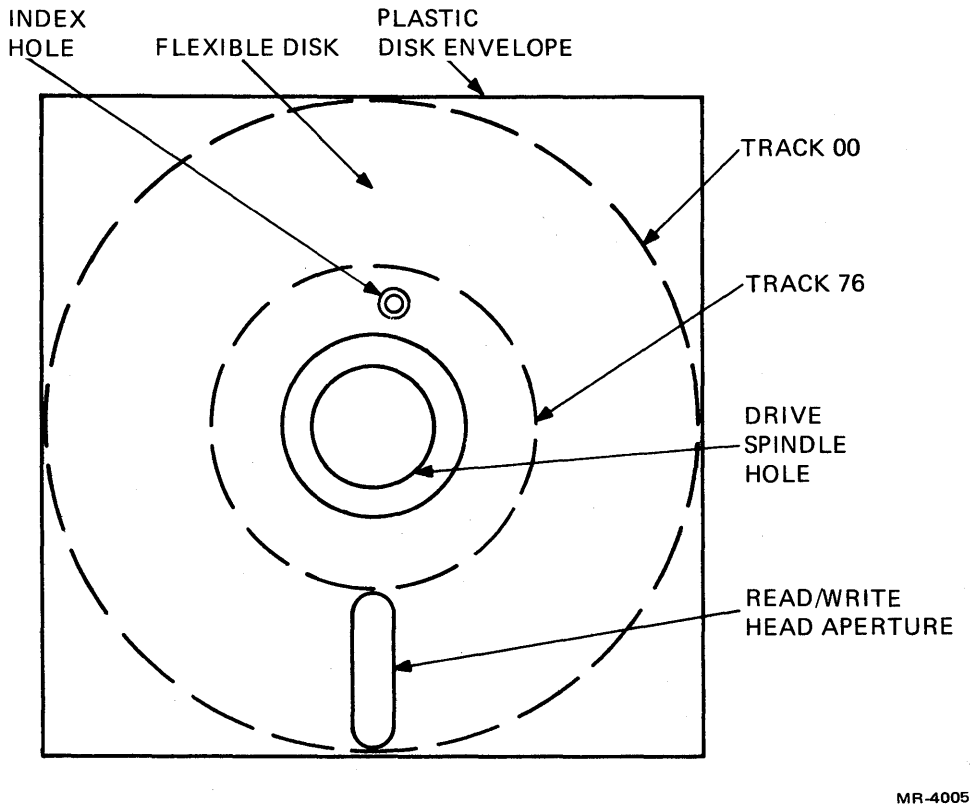


Figure 4-26 Flexible Disk and Envelope

4.9.1 Recording Format

The flexible disk is prerecorded on one side using the IBM 3740 compatible format consisting of 77 tracks and 26 sectors per track. Each sector can contain a maximum of 128, 8-bit bytes of serially recorded data. The data is recorded as single density and double frequency (FM). Figure 4-27 shows the format of a track and sector and identifies the contents of each sector. Each sector contains a header field and a data field.

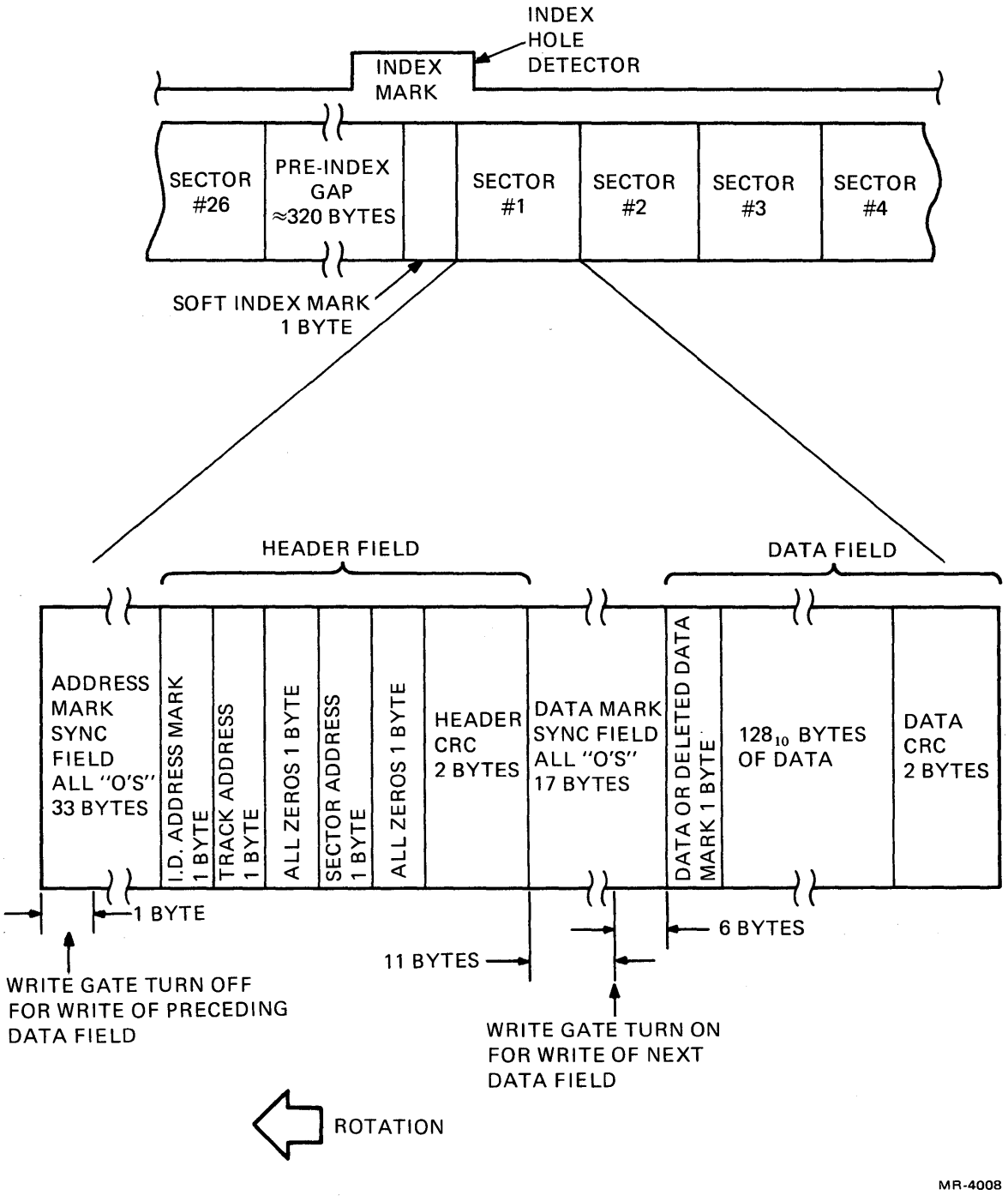


Figure 4-27 Flexible Disk, Track and Sector Information

4.9.1.1 Header Field – The header field consists of seven bytes of information preceded by 33 bytes of all zeros. The header field contains the following information.

1. ID Address Mark – One byte of flux reversals which identifies the beginning of the header field.

2. Track Address – One byte which is the absolute binary track address ($0–114_8$).

3. Byte Separator – One byte of all zeros.

4. Sector Address – One byte which is the absolute binary sector address identifying the sector's position on the track.

5. Byte Separator – One byte of all zeros.

6. Header CRC – Two bytes representing the Cyclic Redundancy Check (CRC) character calculated using the information from the first five header bytes.

4.9.1.2 Data Field – The data field consists of 131 bytes of information preceded by 17 bytes of all zeros. The data field contains the following information.

1. Data or Deleted Data Address Marks – One byte of flux reversals which identifies the beginning of the data field.

2. Data – 128 bytes of recorded data.

3. Data CRC – Two bytes representing the Cyclic Redundancy Check (CRC) character calculated from the information contained in the first 129 data field bytes.

4.9.2 Recording Method

The method used to record track and sector information and data on the flexible disks is defined as double frequency modulated (FM) encoding. When a "one" is to be recorded, it is written between flux changes caused by a fixed clock frequency.

4.9.2.1 Data Recording Patterns – Figure 4-28 shows the recording patterns for writing "ones" and "zeros" on the disk surface. A fixed clock frequency normally causes a flux reversal to occur every 4.0 μs. If a "one" is to be written, an additional flux change will occur between the flux reversals caused by the clock. When a "zero" is to be written, no flux change will occur between clock transitions. The number of flux reversals is therefore the same as that caused by the clock pulses when all "zeros" are written, and twice the number when all "ones" are written.

4.9.2.2 Data and Address Mark Recording – Four address identification marks are preformatted on the disk to indicate the type of information that will follow. Each mark is an 8-bit byte recognized by the pattern which has missing flux reversals that are normally produced by the clock pulses. Figure 4-29 shows the address mark patterns and indicates the code identification. The last three bits specify the type of information that will follow the address mark.

The deleted data or data mark precedes the 128 bytes of data information stored on each sector. The deleted data code will indicate to the operating system that the data which follows is required or invalid. The data code specifies that valid data will follow.

The soft index mark precedes sector 1 and indicates that the 26 sectors will follow. The address ID mark precedes the track and sector address information located in the header field of each sector.

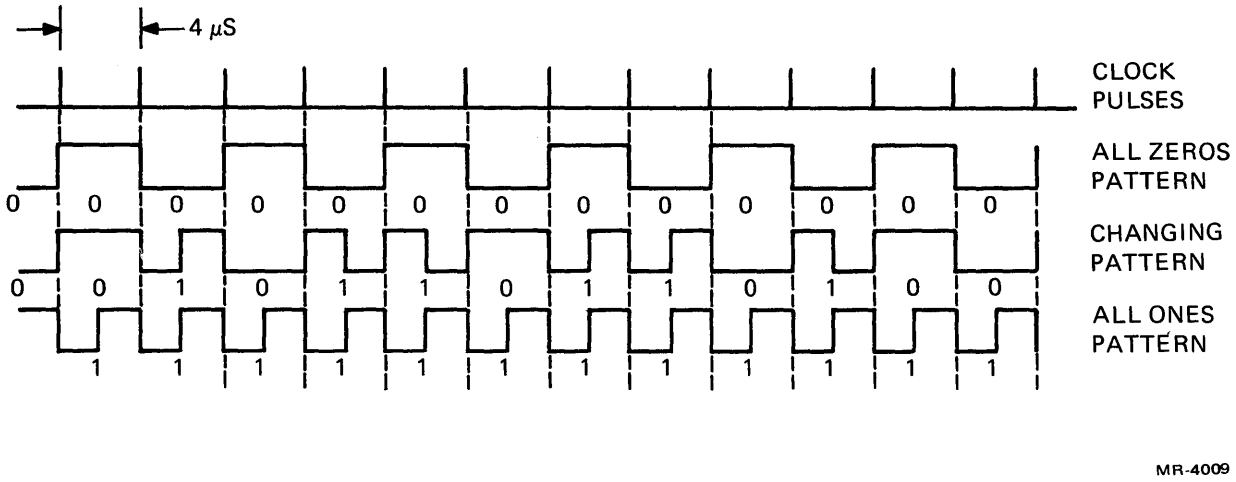
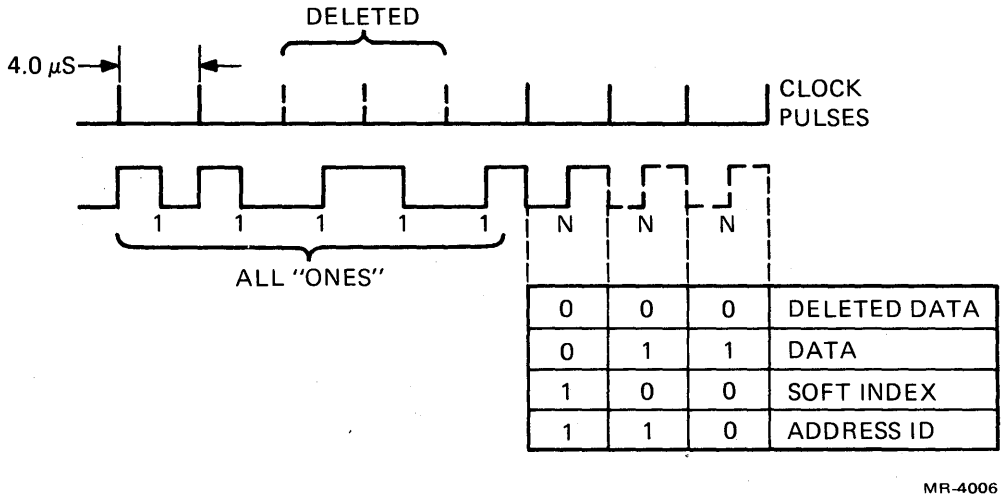


Figure 4-28 Double Frequency (FM) Data Recording Pattern



0	0	0	DELETED DATA
0	1	1	DATA
1	0	0	SOFT INDEX
1	1	0	ADDRESS ID

Figure 4-29 Double Frequency (FM) Address Mark Pattern

4.9.2.3 Synchronization Fields – Synchronization fields, groups of bytes that contain all zeros, provide synchronization to compensate for fluctuations of the disk drive motor. A sync field precedes the header field and data field of each sector.

4.10 DISK CONTROLLER MODULE FUNCTIONS (DWG. NO. 5413273)

Figure 4-30 (Sheets 1 and 2), a simplified diagram of the Disk Controller module, shows the main functional elements, the internal bus routing and the control signals of the module. The Disk Controller module contains an 8085 controller microprocessor which sequences and controls the information transfers within the module. The 8085 operates with an 8316E, (2K × 8-bit ROM) and two 2101A-2 (256 × 4-bit RAMs). The ROM contains the control programs and the RAMs provide storage for data and commands. For detailed functional information related to the 8085 microprocessor, 8316E ROM and 2101A-2 RAM, refer to the *Intel MCS-85*™ *User's Manual* and the current Intel data catalog.

The FD1771 disk controller IC processes the read/write information and controls the operation of the disk drive units. Detailed functional operation of the FD1771 disk controller IC is contained in the data sheet for the Western Digital FD1771 A/B-01 Floppy Disk Formatter/Controller.

Two types of the Disk Controller module are presently in operation in PDT-11/150 units. One module is designated revision K, the other, revision L. The revision designation is contained on both the component side of the module and in the title block of and the circuit schematics (CS). The signal mnemonics assigned to the revision L series drawings are preceded by an F (X) indicator, where (X) specifies the sheet number of the drawing set where the signal was originated.

The location designations of the ICs are contained within some of the function blocks in the diagrams. Location designations not in parentheses are for the revision K module and those in parentheses are for the revision L module.

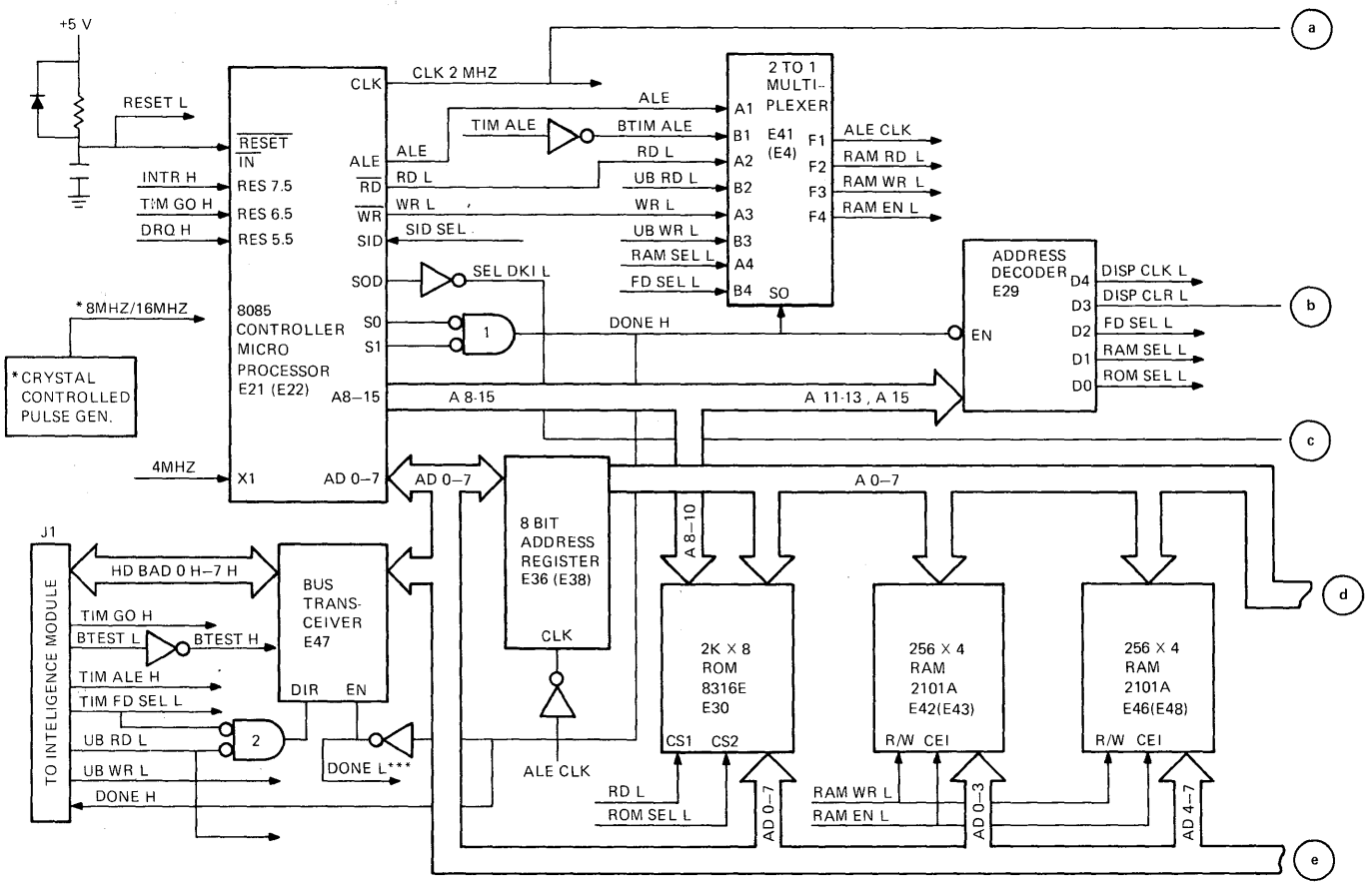
4.10.1 8085 Controller Microprocessor

The internal clock generator of the 8085 microprocessor E21 (E22) is controlled by a 4 MHz square wave connected to the × 1 input. On the revision K series module, the input frequency is developed from an 8 MHz crystal-controlled oscillator; on the revision L module, the oscillator frequency is 16 MHz. The input frequency to the 8085 is internally divided by two and the 8085 provides a CLK 2 MHz output to both the binary counter circuit and the FD1771 disk controller IC.

The 8085 receives interrupt requests on the RST 7.5, RST 6.5 and RST 5.5 inputs. Table 4-14 lists the input signals and interrupt functions.

Control signals from the 8085 microprocessor or from the Intelligence module are switched by the 2-to-1 multiplexer E41 (E4) under control of the 8085. The multiplexer outputs are used to select read and write operations of the RAM and to latch the address information into the 8-bit address register. The 2-to-1 multiplexer is switched by the DONE H signal. When the 8085 is executing instructions, the S0 and S1 outputs will produce a low DONE H signal and the 2-to-1 multiplexer inputs will be selected from the 8085 controller microprocessor. When the 8085 is in the halt state, the DONE H output will be high and the 2-to-1 multiplexer will select the signals from the Intelligence module on connector J1.

Data and address information from the Intelligence module or from the 8085 controller microprocessor are transferred over the AD 0–7 bus lines. The low-byte address information is latched into the address register E36 (E38) by the ALE CLK output of the 2-to-1 multiplexer. The A 0–7 address information is transferred from the address register to the 8316E ROM E30, the 2101A-2 RAM E42 (E43) and the 2101A RAM E46 (E48). The high address bits from the 8085 are transferred over the bus lines A 8–15. Lines A 8–10 provide the additional address information for the 8316E ROM and lines A 11–13 and A 15 are distributed to the address decoder E29 to select one of five control outputs. Table 4-15 lists the address configuration for each of the functions of the address decoders.



* 8MHZ FOR REVISION K MODULE
16 MHZ FOR REVISION L MODULE

***USED ON REVISION L MODULE ONLY

LOCATIONS IN PARENTHESIS ARE FOR REVISION L MODULE. ALL OTHER LOCATIONS ARE FOR REVISION K MODULE.

LOCATION	REVISION	
LOGIC	K	L
GATE 1	E35A	E37A
2	E35B	E37B
3	E20A	E6A
4	E20B	E21
5	E35C	E37C
6	E35D	E9A

Figure 4-30 Disk Controller Module, Simplified Function Diagram
(Sheet 1 of 2)

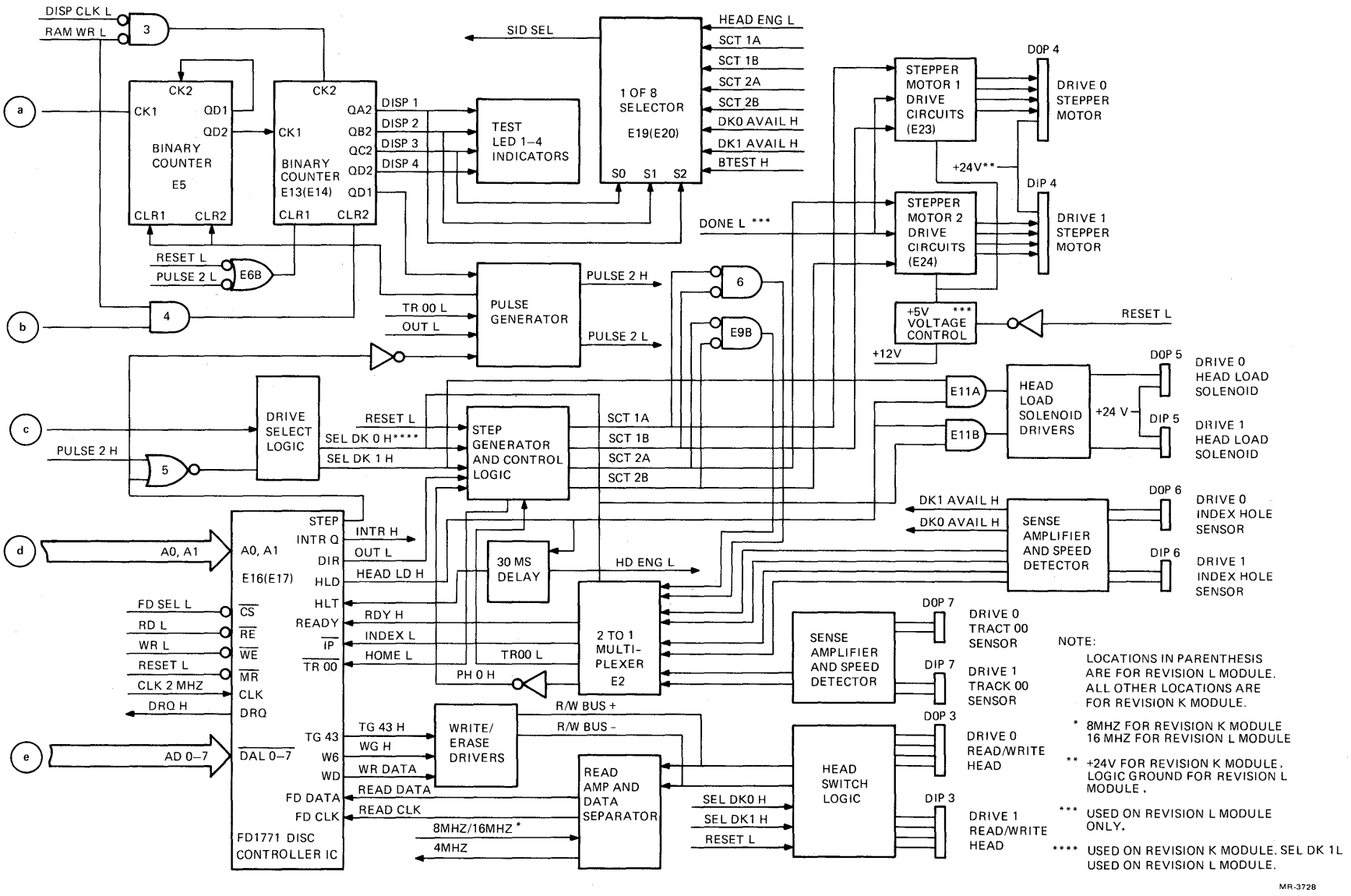


Figure 4-30 Disk Controller Module, Simplified Function Diagram
(Sheet 2 of 2)

Table 4-14 8085 Controller Microprocessor Interrupt Request

Interrupt Input	Signals	Function
RST 7.5	INTR H	From the FD1771 IC to indicate the termination of a previous command.
RST 6.5	TIM GO H	From the function decoder on the Intelligence module to inform the 8085 to execute the previously loaded command.
RST 5.5	DRQ H	From the FD1771 IC to indicate that it contains a byte of data during a read operation or requires a byte of data during a write operation.

Table 4-15 8085 Controller Microprocessor Address Decoding

Address				Output	
All	A12	A13	A15	Signal	Function
L	L	L	L	ROM SEL L	Enables the ROM for read operations.
H	L	L	L	RAM SEL L	Enables the RAM for read or write operations.
L	H	L	L	FD SEL L	Enables the operation of the FD1771 disk controller.
H	H	L	L	DISP CLR L	Allows the WR L signal to clear the 4-bit binary counter which generates the display pulses during the self-test functions.
L	L	H	L	DISP CLK L	Allows the WR L signal to clock the 4-bit binary counter to generate the display pulses during the self-test mode. During normal operation the DISP CLR C and DISP CLK L signals are used to monitor the head load timing and determine if one or two disk drive assemblies are contained in the unit.

The SID SEL signal to the SID input of the 8085 is monitored during the power-up sequence to determine if the self-test mode was selected. This signal is the output from the 1-of-8 selector E19 (E20) and during the self-test mode the selector senses the functions being performed by the Disk Controller module. The 1-of-8 selector is sequenced to select one of the eight inputs by the output of a 4-bit binary counter E13 (E14). The operation of the counter is controlled by the decoding of specific addresses from the 8085 at address decoder E29.

4.10.1.1 Power-Up and Initialize Functions – When ac power is applied to the PDT-11/150 unit, the RESET L signal to the RESET IN input of the 8085 will be held low by the RC delay circuit until the +5 V is present. The low RESET L signal clears the instruction register and program counter within the 8085 and also resets the internal status flip-flops. The signal is an input to gate E6B, which is used to clear the step generator logic and the binary counter E13 (E14). The RESET L signal is a master reset to the FD1771 IC and clears the internal command register.

During the power-up sequence, the 8085 controller microprocessor performs an initialize routine that loads the starting address of the stack location of the RAM into the stack pointer register of the 8085. The routine also checks the 1-of-8 selector E19 (E20) to determine whether the unit is in self-test mode or normal mode of operation. If the normal mode is indicated, the 8085 will set the internal interrupt enable flip-flops and enter the halt state upon completion of the initialize routine. In the self-test mode, the 8085 will perform a two-phase diagnostic test and then halt.

When the halt condition exists, the S0 and S1 outputs of the 8085 will be low, resulting in a high DONE H signal at the output of gate 1. This signal will disable the address decoder E29, enable the bus transceiver E47, and inform the 8085 I/O microprocessor on the Intelligence module that the Disk Controller module is ready to receive instructions.

The 2-to-1 multiplexer E41 (E4) enables the 8085 I/O microprocessor or the 8085 controller microprocessor to read from or write into the 256 × 4-RAM ICs on the Disk Controller module. The high DONE H signal selects the input control signals from the Intelligence module through the B inputs of the 2-to-1 multiplexer. The A inputs receive control signals from the 8085 controller microprocessor and are selected by a low DONE H signal. The outputs of the 2-to-1 multiplexer are used to enable the reading or writing of information into the 2101A RAMs and to load the RAM address information into the 8-bit address register E36 (E38).

The low TIM FD SEL L signal at connector J1 is generated by the I/O select logic on the Intelligence module. This signal, transferred through the 2-to-1 multiplexer E41 (E4), produces a low RAM EN L signal which selects both of the 256 × 4-RAM ICs. The TIM FD SEL L is gated with the low UB RD L signal at gate 2 to select the direction of data transfers through the bus transceiver. A high output from gate 2 will connect the HDBAD 0 H–7 H bus lines to the AD 0–7 bus lines allowing the Intelligence module to read from selected locations in RAM. A low output at gate 2 will allow a transfer in the opposite direction during a write command.

The RAM contains a data buffer consisting of 128 bytes. All data to be written onto or read from the disk is stored in this buffer. Other locations in RAM are reserved for track and sector information, commands and status. During normal program operation, the 8085 I/O microprocessor writes or reads the track and sector information and the command status is written by the 8085 controller microprocessor.

4.10.1.2 Read or Write Operations – All read or write operations on a disk are initiated by the command information from the Intelligence module. After the commands and data are loaded into the 2101A-2 RAM ICs, the high TIM GO H signal at connector J1 from the function decoder of the Intelligence module will cause an interrupt to occur at the RST 6.5 input of the 8085 controller microprocessor. The 8085 performs a vectored interrupt to read the command information stored in the RAM and perform the specified operation. During this operation, the DONE H signal will be low, which will enable the address decoder E29, select the 8085 control information from the 2-to-1 multiplexer E41 (E4), disable the bus transceiver E47, and inform the Intelligence module that the 8085 controller is performing the designated operation.

4.10.2 Disk Drive Selections

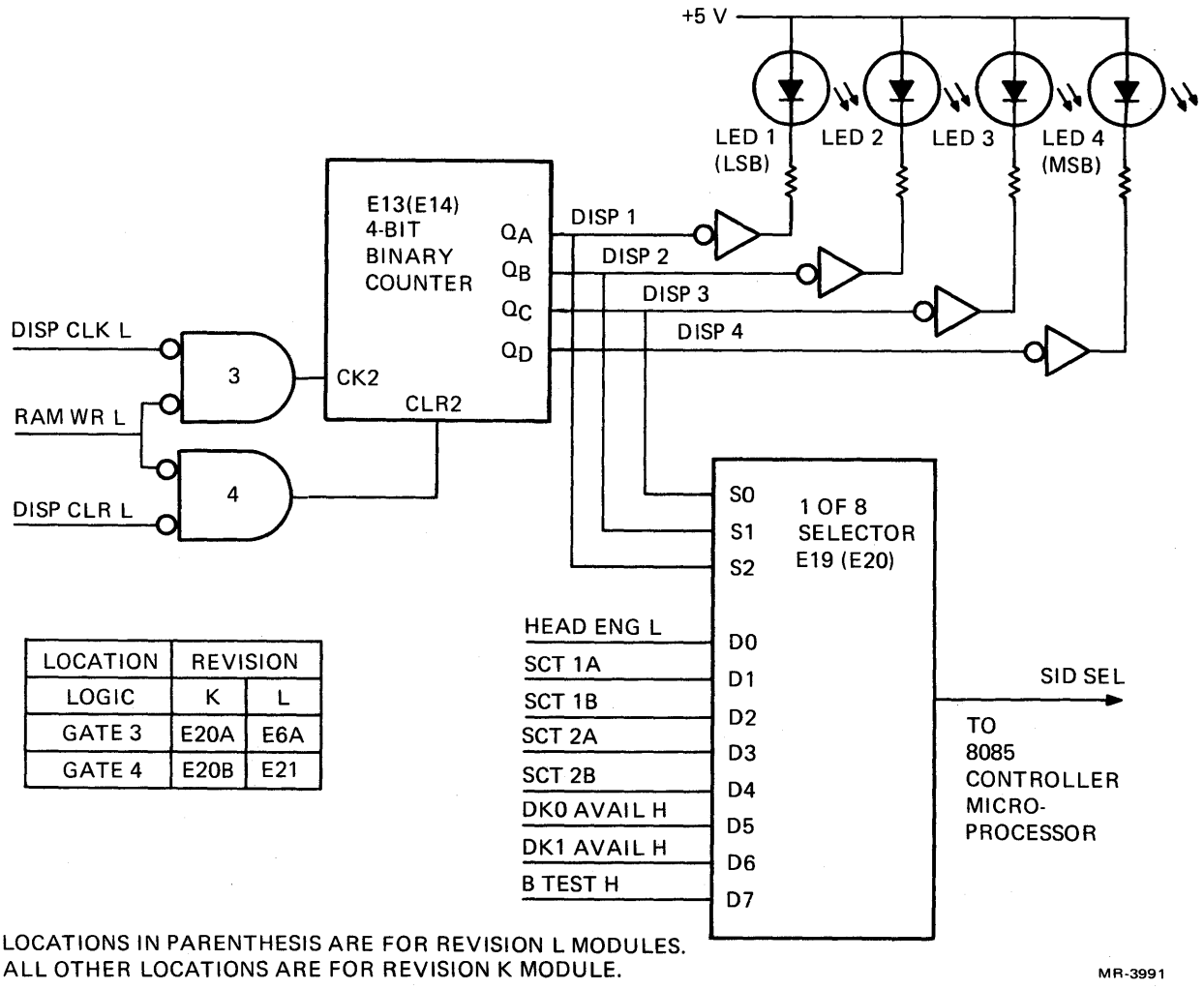
The selection of disk drive 0 or disk drive 1 is performed by the 8085 controller microprocessor as shown in Figure 4-27. The SOD output of the 8085 is inverted to generate the SEL DK1 L signal, which is distributed to the drive select logic. The SEL DK1 L output is low to select disk drive 1 and high to select disk drive 0. The drive select logic provides a SEL DK0 H output (which is the same signal as SEL DK1 L) and an inverted SEL DK1 L signal (which is SEL DK1 H). These signals are used to enable the required stepper motor control circuit, to energize the head load solenoid, and to

select the proper input of the index hole and track 00 detectors through the 2-to-1 multiplexer E2. During information transfers with the disk, the SEL DK0 H signal (used on the revision K module) and the SEL DK1 H signal (used on the revision L module) select the read/write head of disk drive 0 or disk drive 1.

4.10.3 Self-Test Function Select and Indicator Logic

Figure 4-31 is a simplified diagram of the logic used to monitor the disk controller functions during the self-test diagnostics and to display the octal code of the test being performed. The 4-bit binary counter E13 (E14) is controlled by the self-test program stored in ROM. The 8085 controller microprocessor address lines are decoded by E29 to generate the DISP CLK L and DISP CLR L signals. The low DISP CLR L signal is gated with the low RAM WR L signal from the 8085 at gate 4 to clear counter E13 (E14). The low DISP CLK L signal is gated with a low RAM WR L signal at gate 3 to clock the counter. Each clock input will be counted and the counter outputs used both to control the LED indicators and to select one of the eight inputs to the 1-of-8 selector E19 (E20). The SID SEL output of selector E19 (E20) is monitored by the 8085 at the SID input to determine if the function requested during the self-test has occurred.

Table 4-16 lists the E13 (E20) counter outputs and the resulting selector signal and octal display codes.



LOCATION	REVISION	
LOGIC	K	L
GATE 3	E20A	E6A
GATE 4	E20B	E21

Figure 4-31 Self-Test Function Select and Display, Simplified Diagram

Table 4-16 Self-Test Function Select and Octal Code

Counter E13 (E14) Output QA	QB	QC	QD	Output Signal	LED Octal Code
L	L	L	L	HD ENG L	0
H	L	L	L	SCT 1A	1
L	H	L	L	SCT 1B	2
H	H	L	L	SCT 2A	3
L	L	H	L	SCT 2B	4
H	L	H	L	DK0 AVAIL H	5
L	H	H	L	DK1 AVAIL H	6
H	H	H	L	BTEST H	7
L	L	L	H	HD ENG L	10
H	L	L	H	SCT 1A	11
L	H	L	H	SCT 1B	12
H	H	L	H	SCT 2A	13
L	L	H	H	SCT 2B	14
H	L	H	H	DK0 AVAIL H	15
L	H	H	H	DK1 AVAIL H	16
H	H	H	H	BTEST H	17

H = high level
L = low level

4.10.4 Head Load Control and Track/Index Hole Detection

Figure 4-32 is a simplified diagram of the circuits that detect the presence of the index hole and the location of track 00 of the disk in disk drive 0. It also includes the circuit that controls the solenoid. The circuit shown is for disk drive 0; however, a similar circuit on the Disk Controller module provides the same functions for disk drive 1.

When solenoid L1 is energized, a pressure pad forces the surface of the disk onto the read/write head. When a read or write operation is to occur, the FD1771 transfers a high HEAD LD H signal to gates E11A and E11B. When disk drive 0 is selected, a high SEL DK0 H input (for the revision K module) or a high SEL DK1 L signal (for revision L module) to gate E11B will cause transistor Q15 to conduct and energize the head load solenoid L1. When disk drive 1 is selected, a high SEL DK1 H signal at gate E11A will activate the head load circuit of disk drive 1.

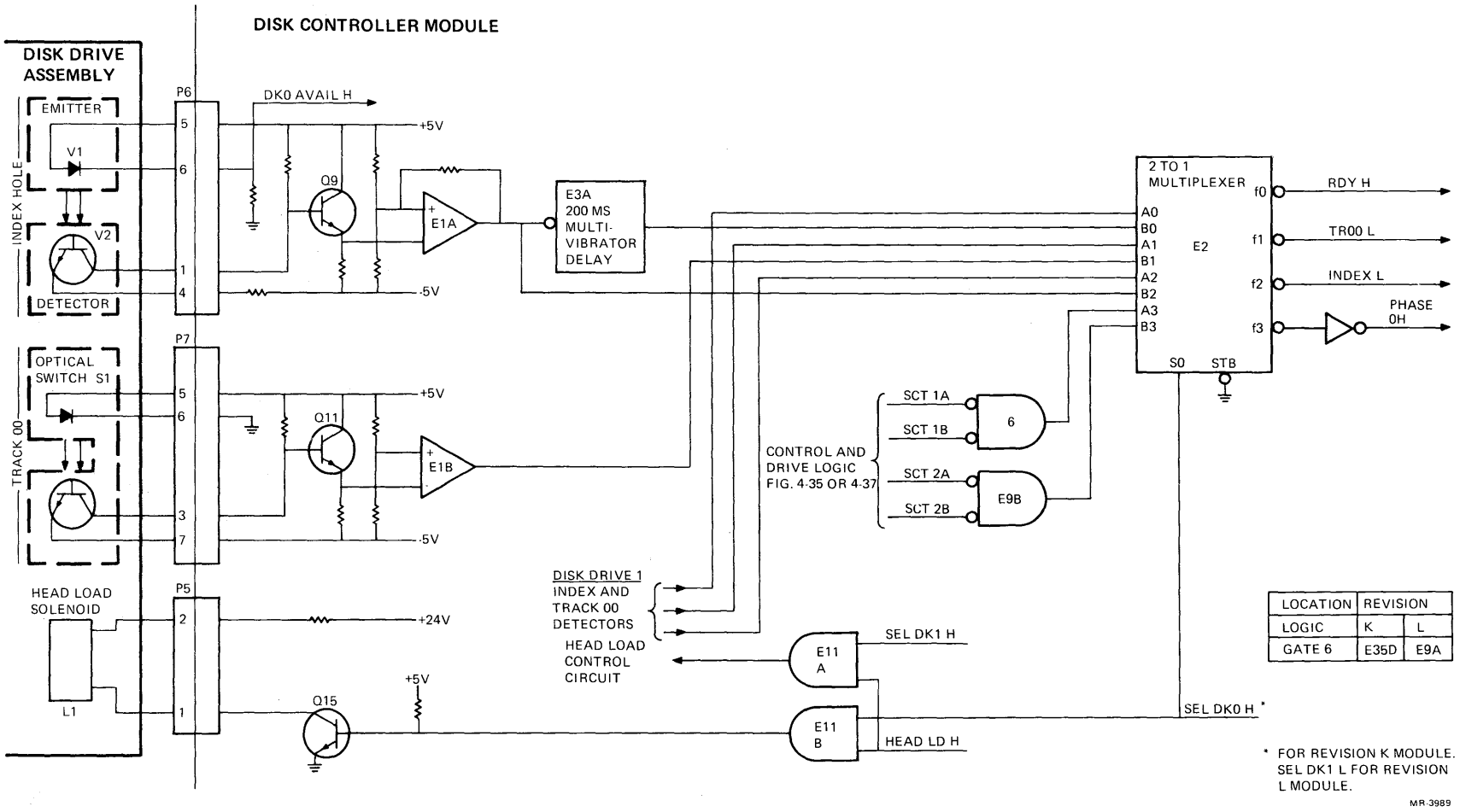


Figure 4-32 Head Load Control and Track and Index Hole Detection

The SEL DK0 H or SEL DK1 L signal is also used to control the outputs of the 2-to-1 multiplexer E2. When SEL DK0 H is high, the B inputs from the disk drive 0 circuits will be selected; when the signal is low, the A inputs from the disk drive 1 circuits will be selected.

The LED emitter V1 and detector V2 sense the position of the index hole in the disk when the disk is rotating and generate a pulse when the hole is detected, using it as a starting reference. Refer to Figure 4-26 for the physical location of the index hole in the disk surface, and Figure 5-46 for the location of the index hole detector V2 and emitter V1 on the disk drive assembly.

When the index hole is not aligned with emitter V1, detector V2 is not conducting but the +5 V on the base of transistor Q9 will cause it to conduct. The emitter of Q9 is connected to the negative input of amplifier E1A and the +5 V will prevent the output of E1A from triggering E3A, the 200 ms multivibrator delay. When the index hole is sensed, the light emitted from V1 will cause detector V2 to conduct. The base of transistor Q9 will become negative and Q9 will stop conducting, causing the emitter to become more negative than the bias voltage on the positive (+) input to E1A. The negative transition of the output of E1A will trigger E3A, which will produce a low pulse to the 2-to-1 multiplexer at input B0. When the disk is rotating at normal operating speed, the time of one revolution is approximately 166 ms and the E3A multivibrator will remain in the triggered condition. The E3A output will remain at a low level, which results in a high RDY H signal at the F0 output of E2. When the rotating speed of the disk is less than required, the output of E3A will become high after 200 ms to produce a low RDY H signal. This signal is monitored by the FD1771 disk controller to prevent a read or write operation when the disk is not up to speed.

The output of E1A provides a pulse to E2 at B2 which is sampled as an INDEX L signal by the FD1771 to indicate the detection of the of the index hole's transition.

The DK0 AVAIL H signal indicates whether a disk drive 0 assembly is physically installed in the PDT-11/150 unit. A similar signal DK1 AVAIL H is also generated by the disk drive 1 circuit. When the drive assembly is present, the conduction of V1 will produce either a high DK0 AVAIL H signal or DK1 AVAIL H signal. If the drive assembly is not installed, the signal will be low. The output is monitored by the 8085 controller microprocessor through the 1-of-8 selector E19 (E20) shown in Figure 4-30, Sheet 2.

Optical switch S1 is used to indicate that the read/write head is located over track 00 of the disk. Refer to Figure 4-26 for the physical location of track 00 on the disk surface, and Figure 5-46 for the location of optical switch S1 in the disk drive assembly.

When the read/write head is not positioned over track 00, the arm on the head carriage will not interrupt the light. The light from the LED will be detected and transistor Q11 will conduct. The emitter of Q11, which is connected to the negative input of amplifier E1B, will become more positive than the voltage at the positive input. The high output of E1B, sensed at the B1 input of the 2-to-1 multiplexer, produces a high TR 00 L signal. This indicates that the head is not over track 00. When the stepper motor positions the head over track 00, an arm attached to the head carriage will interrupt the light from switch S1. Transistor Q11 will stop conducting and the output of amplifier E1B will be low level, resulting in a low TR 00 L signal. The TR 00 L signal is connected to the stepper motor control logic.

The SCT1A and SCT1B inputs to gate 6 and the SCT2A and SCT2B inputs to gate E9B are generated by the stepper motor control logic for disk drive 0 and disk drive 1, respectively. When the phase 0 winding of the stepper motor is energized, both inputs to each gate will be low and a high level will be present on the A3 and B3 inputs of the 2-to-1 multiplexer E2. The F3 output of E2 is inverted to produce a high PHASE 0 H signal. This signal is applied to the TR 00 input of the FD1771 to insure that the track 00 indication is valid before the FD1771 issues an OUT L signal.

4.10.5 Stepper Motor Direction and Control Logic

The stepper motor shaft is attached to a lead screw as shown in Figure 5-50. The read/write head on the head carriage of the disk drive assembly is moved over the desired track on the flexible disk by the rotation of the 4-phase, variable reluctance stepper motor. The motor shaft rotates 15° for each pulse applied to stator windings. To move the head from one track to an adjacent track, the motor shaft must rotate 30°; therefore, two step pulses are required.

To control the stepper motor, the FD1771 generates two outputs, OUT L and STEP, as shown in Figure 4-30, Sheet 2. The OUT L signal from the DIR output of the FD1771 controls the motor shaft's direction of rotation; the STEP output is a pulse generated by the FD1771 for each required track-to-track transition of the head. If the head is required to move toward track 00, which is located at the outer edge of the flexible disk, the OUT L signal will be low. If the direction required is toward track 76, the innermost track of the disk, the OUT L signal will be high.

The second pulse required for each track-to-track transition is generated by a counter delay circuit consisting of a divide-by-256 counter, a divide-by-16 counter, a gating circuit and a one-shot pulse generator.

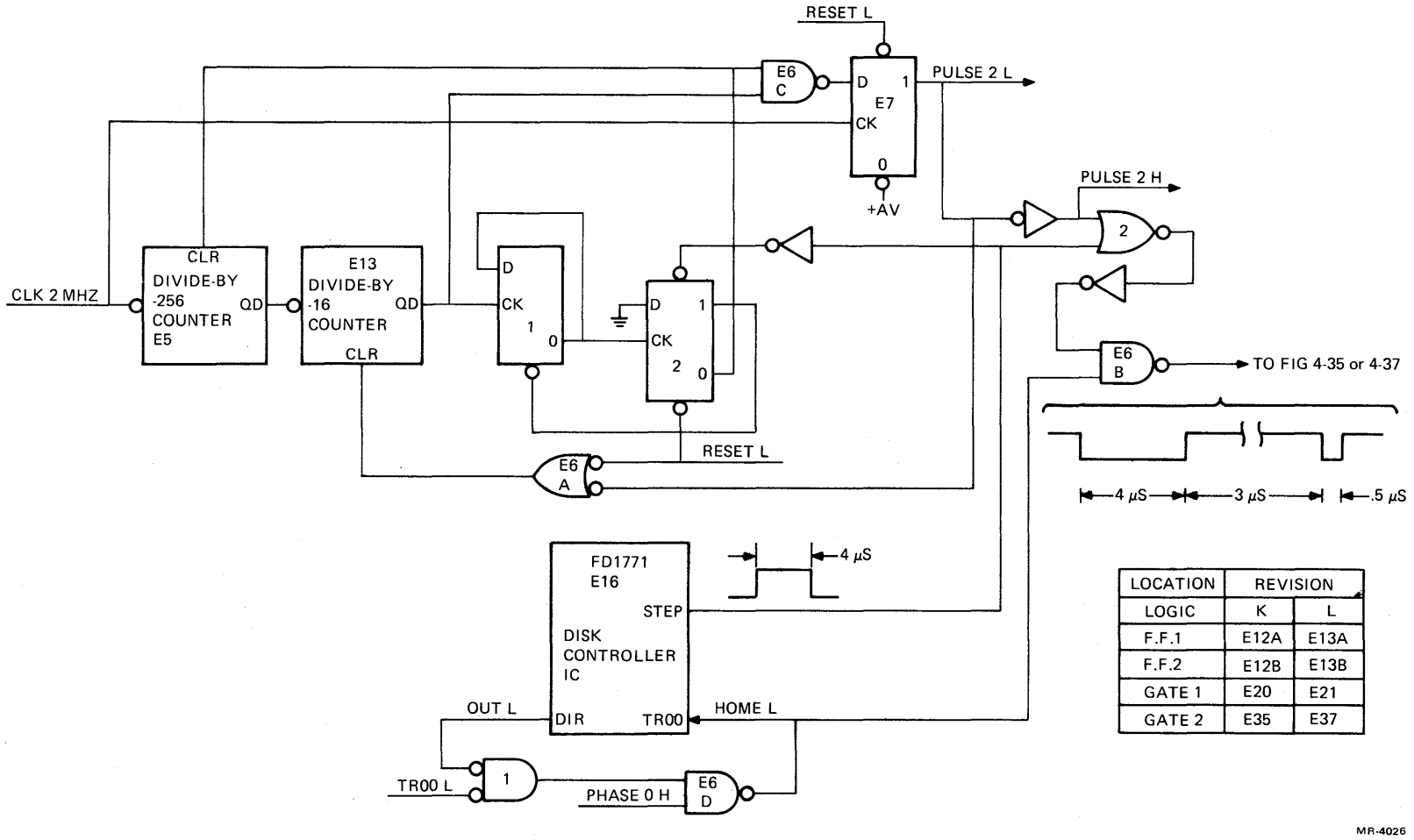
4.10.5.1 Stepper Motor Pulse Generation – Figure 4-33 is a simplified diagram of the logic used to generate the stepper motor pulses, and Figure 4-34 shows the timing sequence of the signals. When the ac power is applied to the PDT-11/150, the low RESET L signal will preset flip-flop E7, clear flip-flop 2 and clear the divide-by-16 counter E13 through gate E6A. The high (0) output of flip-flop 2 will clear the divide-by-256 counter E5 and the low (1) output will clear flip-flop 1.

The high PULSE 2 L output of flip-flop E7 is inverted and becomes a low PULSE 2 H signal to gate 2. The STEP output of the FD1771, also applied to gate 2, will also be low until a read/write head movement is decoded by the FD1771. The high output of gate 2 is inverted to produce a low input to gate E6B. The output of gate E6B will initially be held at a high level.

When a read/write head movement is to occur, the FD1771 generates a 4 μs pulse at the STEP output which is applied to gate 2. The output of the gate is inverted and produces a positive-going pulse on the input of gate E6B. When the HOME L signal from gate E6A is high, the 4 μs pulse will be transferred through gate E6B to become a negative-going pulse at the output. This is the first stepper motor pulse.

The HOME L signal will be low when a track 00 indication is detected, when the direction of the read/write head motion indicated by the FD1771 is toward track 00, and when the phase 0 winding of the stepper motor is energized. Refer to Figure 4-32 for the generation of the TR 00 L and PHASE 0 H signals. The low OUT L signal from the DIR output of the FD1771 is gated with a low TR 00 L signal at gate 1 to produce a high signal at the input of gate E6C. The high PHASE 0 H signal, also at E6C, will produce a low HOME L output, which is monitored at the TR 00 input at the FD1771. This indicates to the FD1771 that track 00 has been reached and the low HOME L signal will inhibit gate E6B and prevent any additional step pulses from causing stepper motor rotation.

The step pulse from the FD1771 is also inverted and used to preset flip-flop 2. The low (0) output of flip-flop 2 enables the divide-by-256 counter E5, which will start counting the CLK 2 MHz input pulses. The high (1) output of flip-flop 2 will allow flip-flop 1 to be clocked. After 128 μs, the high-to-low transition of the QD output of E5 will start the count of the divide-by-16 counter E13. After eight high-to-low transitions of E5 (1024 μs), the QD output of E13 will become high and will set flip-flop 1.



LOCATION	REVISION	
LOGIC	K	L
F.F.1	E12A	E13A
F.F.2	E12B	E13B
GATE 1	E20	E21
GATE 2	E35	E37

Figure 4-33 Step Generator Circuit, Simplified Diagram

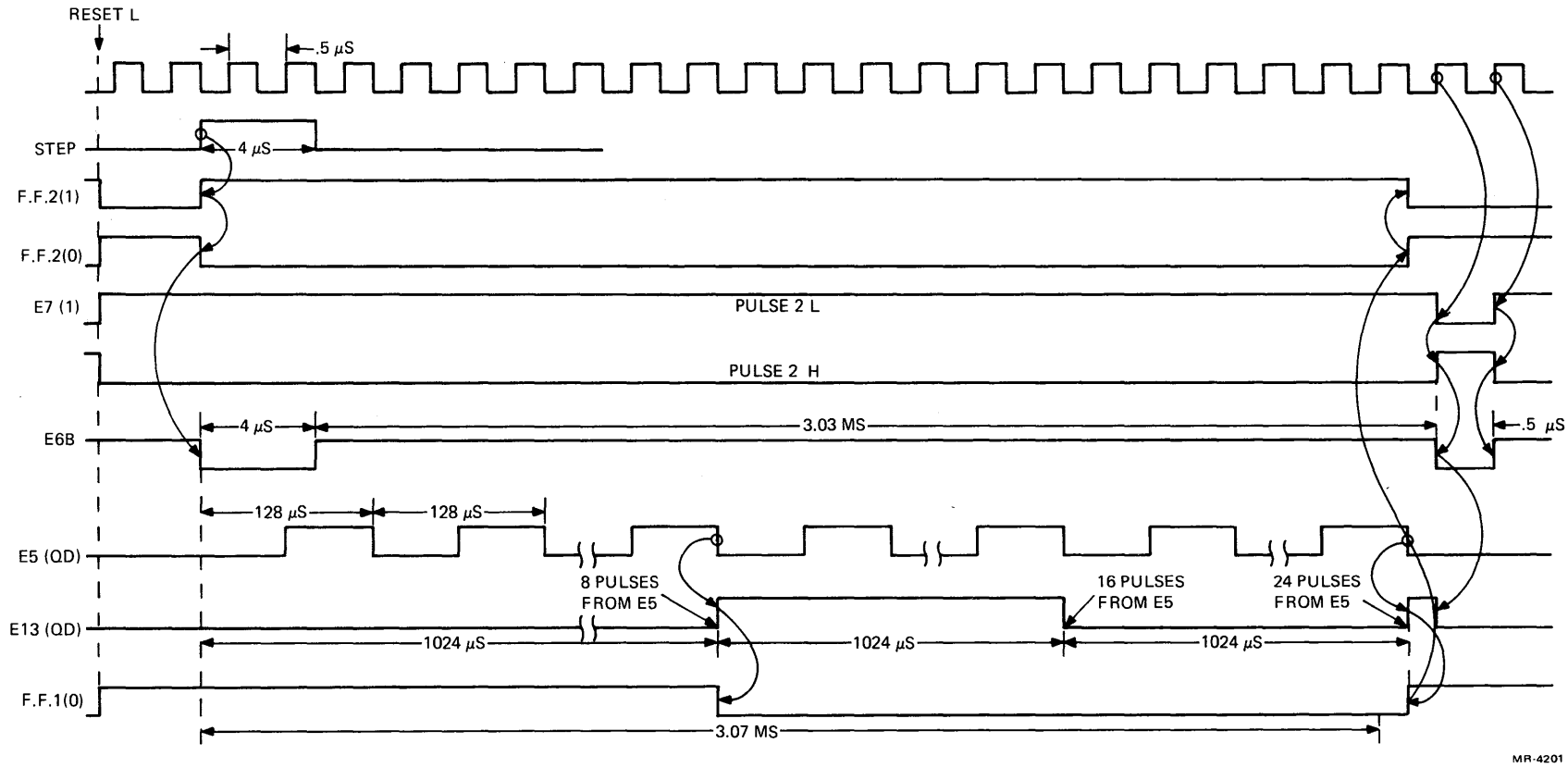


Figure 4-34 Step Generator Circuit, Timing Diagram

The next low-to-high transition of E13 will occur after 16 high-to-low transitions of E5 (2048 μs), and will clear flip-flop 1. The low-to-high transition of the (0) output of flip-flop 1 will clear flip-flop 2 and the high (0) output of flip-flop 2 will enable gate E6D. The high QD output of counter E13 is also applied to gate E6D, causing a low level at the D input of flip-flop E7. Flip-flop E7 will be cleared by the next low-to-high transition of the CLK 2 MHz pulse, which is connected to the clock (CK) input. The PULSE 2 L output signal from E7 will become low and gated through E6A to clear counter E13.

The low QD output of E13 will disable gate E6D and cause the D input of the flip-flop E7 to become high. The next low-to-high transition of the CLK 2 MHz pulse will set flip-flop E7 and cause the PULSE 2 L to become high for .5 μs. The PULSE 2 H signal is inverted and gated through E6B to produce the second pulse required by the stepper motor. When the next 4 μs step pulse occurs at the STEP output of the FD1771, the entire sequence will be repeated; after a 3 ms delay, the next .5 μs pulse will be generated.

4.10.5.2 Stepper Motor Control and Drive Circuits – Two versions of the stepper motor control and drive circuits are in use in PDT-11/150 units. One version is contained on Disk Controller module 5413273 revision K and the other on Disk Controller module 5413273 revision L. Figure 4-35 is a simplified diagram of the revision K circuit. The stepper motor pulses from the pulse generator (see Figure 4-33) are applied to the stepper motor drive logic (see Figure 4-35). The circuit shown in Figure 4-35 is for the disk drive 0 stepper motor B1. A similar circuit is used to control the stepper motor of disk drive 1.

When ac power is applied to the unit, the low RESET L input will clear flip-flops E17A and E17B. The high (0) outputs of each flip-flop are gated at E22A to produce a high input to the base of transistor Q1, causing it to conduct. The current from the +24 at pin 2 of connector D0P4/P4 V dc will conduct through the phase 0 winding of motor B1, through PIN 1 of the connector, and through the Q1 transitor to ground. One of the foour phase windings will always be grounded, depending on the state of the stepper counter.

Figure 4-36 is the timing sequence diagram for the stepper motor control and drive circuits. When the position of the read/write head is to be changed, the stepper motor pulses occur at gates E39A and E39B. When disk drive 0 is selected, the SEL DK1 L signal from the 8085 controller microprocessor is high; when disk drive 1 is selected, the SEL DK1 L signal is low. The high SEL DK1 L signal is inverted to enable gate E39A and allows the first step pulse to set the E17A flip-flop. This results in a high SCT 1A signal to gate E22B, which is also connected to the high (0) output of flip-flop E17B. Transistor Q1 will stop conducting and transistor Q2 will conduct through the phase 1 winding of the stepper motor B1. The motor shaft will rotate 15° from its previous position.

If the the head is required to move toward track 00, the OUT L signal from the FD1771 IC will be low. This signal disables gate E18A and is inverted to enable gate E18B. The low (0) output of flip-flop E17A is gated through E18 B inverted by E18C to provide a high signal on the J and K inputs of E17B. When the next step pulse occurs, flip-flop E17A will be cleared and flip-flop E17B will be set. The high SCT 1B output of flip-flop E17B is gated at E22C with the high (0) output of flip-flop E17A. Transistor Q3 will conduct and current will flow through the phase 2 winding of stepper motor B1, moving the motor shaft 15° for the total of 30° required for each track-to-track change.

If the movement of the head is required to change toward track 76, the OUT L signal from the FD1771 will be high and gate E18A will be enabled. If transistor Q2 is initially conducting when the direction change occurs, the first step pulse will clear the E17A flip-flop and produce a low SCT 1A signal. The low signal is transferred through gate E18A and inverted to a high signal at the J and K inputs of E17B. When the next step pulse occurs, flip-flop E17B will become set to generate a high signal on both inputs of gate E22D. Transistor Q4 will conduct and current will flow through the phase 3 winding, the motor shaft will rotate 15° in the opposite direction. Subsequent pulses will cause transistors Q3, Q2 and Q1 to conduct (in that order).

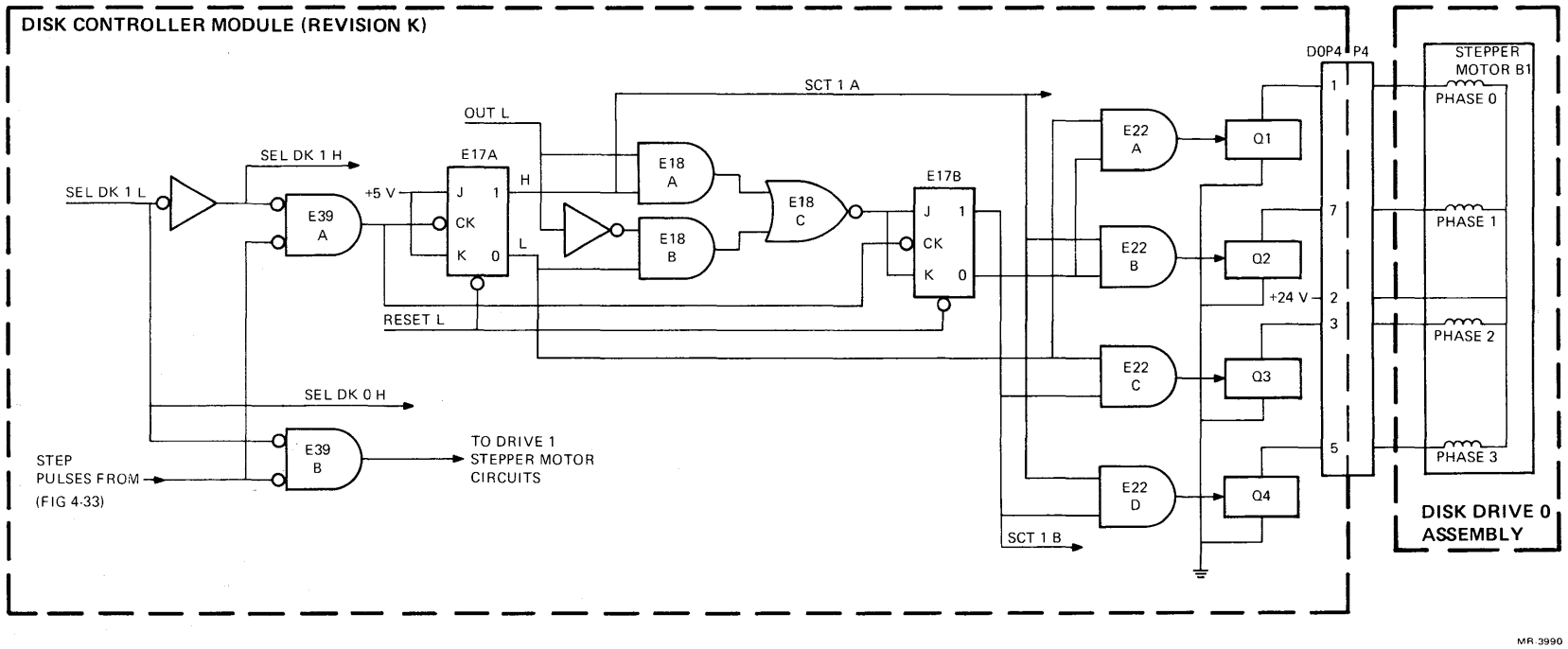


Figure 4-35 Stepper Motor Control and Drive Logic (Revision K), Simplified Diagram

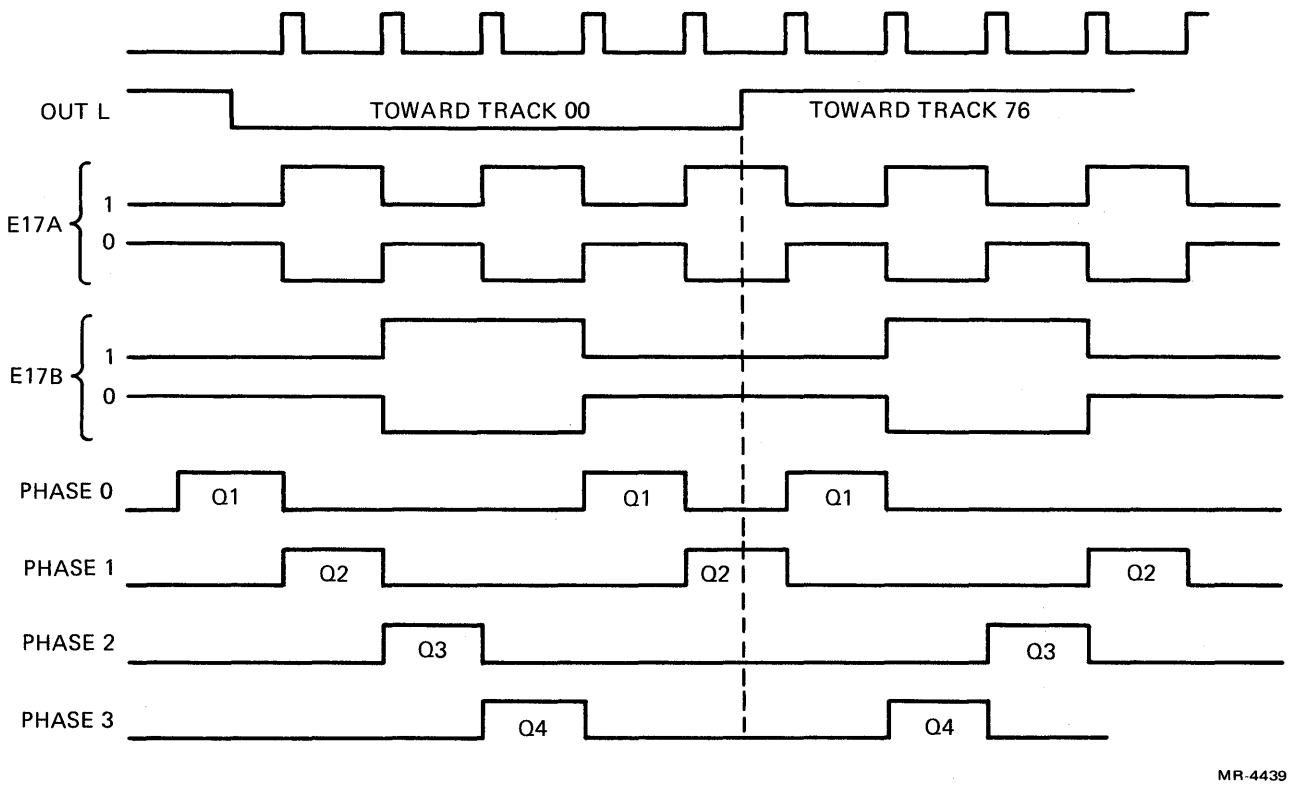


Figure 4-36 Stepper Motor Control and Drive Logic, Timing Diagram

Figure 4-37 is a simplified diagram of the stepper motor control and drive logic on the revision L module. This circuit operates in a manner similar to that of the revision K circuit described above. The output gating circuit of the stepper motor control logic consists of a decoder/driver E23, which controls the conduction of four Darlington transistor circuits, Q1 through Q4.

The input Vcc voltage to E23 is derived from the circuit consisting of the +12 V dc, a series resistor and zener diode D36. The FI RESET L signal is held low by an RC network when the ac voltage is initially applied. When the FI RESET L becomes high, the level is inverted to become F7 RESET H, which allows transistor Q24 to conduct, and the F7 MAG 5VH (+5 V dc) is applied to E23. This delay prevents the energizing of a stepper motor winding until the dc voltages are at their required levels.

When the 8085 controller microprocessor is not in the halt state, the F2 DONE L level will be high. This level is inverted to a low F7 STEP DIS H level and is connected to the C and D inputs of the decoder/driver E23 and E24. The (1) output of flip-flop E17A, the F3 SCT 1A signal, connects to input A of E23; the (1) output of flip-flop E17B, the F3 SCT 1B signal, connects to the B input of E23. Table 4-17 shows the relationship of the input levels to the outputs of E23. When an output is "off," it is an open circuit to ground; when it is "on," it becomes grounded.

When a decoder/driver E23 output is grounded, the input level to a Darlington transistor will become low and the transistor will conduct. The emitter of the output transistor is connected to the +24 V. When the transistor conducts, the appropriate stepper motor phase winding is energized through connectors D0P4/P4. The ground return for all phase windings is also through pin 2 of the same connector.

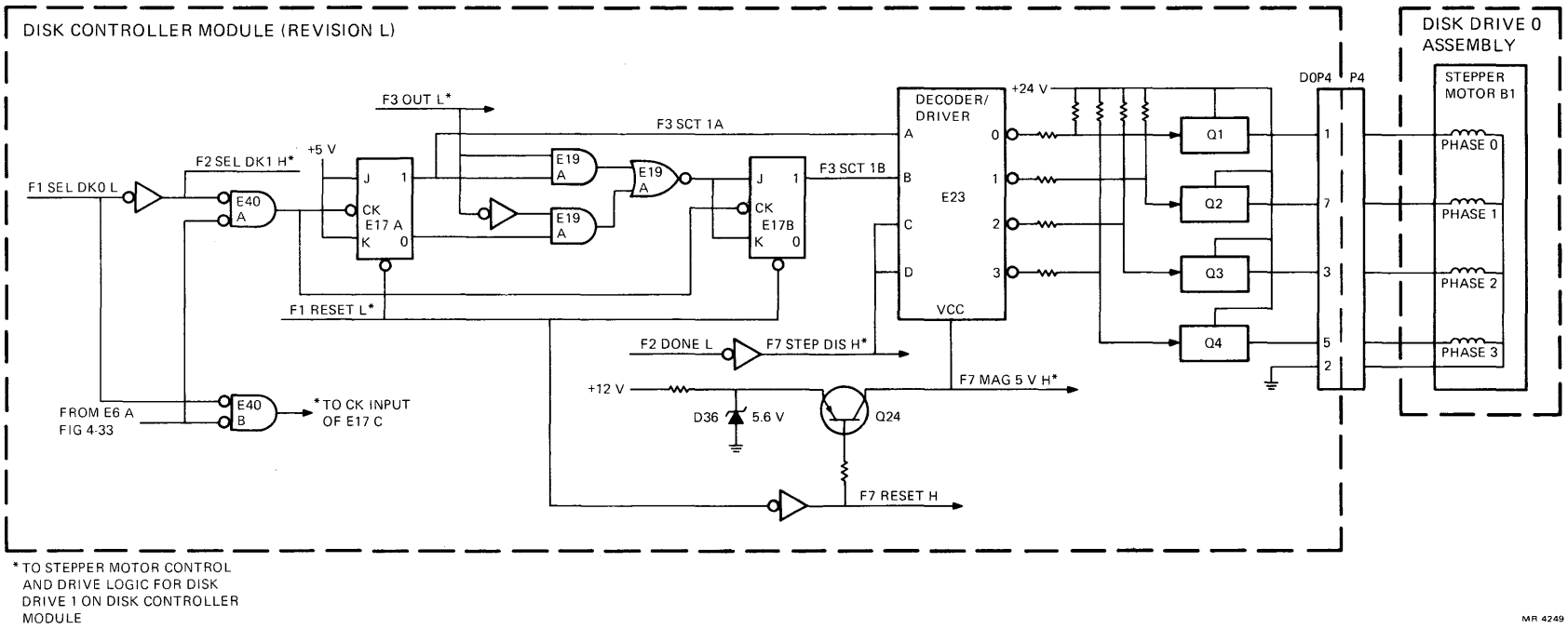


Figure 4-37 Stepper Motor Control and Drive Logic (Revision L), Simplified Diagram

Table 4-17 E23 Decoder/Driver Functions

Inputs				Output (ON)
D	C	B	A	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
H	H	X	X	None (all open)

X = L or H

4.10.6 FD1771 Disk Controller IC and Associated Logic

The FD1771 (see Figure 4-30, Sheet 2) is the disk controller IC that receives control, address and data information from the 8085 and provides the data and control information to the selected disk drive. The address information from the 8085 controller microprocessor is transferred through the address register E36 (E38) on bus lines A 0 and A 1. These lines select one of five internal registers of the FD1771, depending upon a read or write operation. Table 4-18 lists the internal registers selected by the address lines when the write enable WE or read enable RE inputs to the FD1771 are selected.

Track and sector address information and data are transferred to and from the FD1771 through the AD 0–7 bus lines under control of the 8085 controller microprocessor.

The chip select CS input to the FD1771 is controlled by the FD SEL L signal from the address decoder E29. When the CE input is low the FD1771 is enabled and communication between the 8085 controller microprocessor can occur.

The master reset MR input to the FD1771 is connected to the RESET L signal which is initially low level when ac power is applied, becoming high level after a delay. The low signal clears the internal command register and resets the circuits within the FD1771.

The clock (CLK) input provides the timing reference for the internal operations of the FD1771. The input is connected to the CLK 2 MHz square wave output from the 8085 controller microprocessor.

The data request DRQ output from the FD1771 produces an interrupt request to the 8085 on the DRQ H line. When the FD1771 data register contains assembled data during a read operation or when the data register is empty during write operations, the DRQ H line will become high to request service from the 8085.

4.10.6.1 Disk Write Operations – Data to be written on the disk is transferred from the 8085 as an 8-bit byte and loaded into the data register of the FD1771. The data is then shifted serially from the WD output of the FD1771, through the WD DATA line, to the read/write head circuits shown in Figure 4-38. The circuits shown in Figure 4-38 are for disk drive 0; however, similar circuits on the Disk Controller module provide the same functions for disk drive 1.

Table 4-18 FD1771 Register Selection

Address Line A0	Address Line A1	FD1771 Input*	FD1771 Register
L	L	RE	Status
L	L	WE	Command
L	H	WE or RE	Track
H	L	WE or RE	Sector
H	H	WE or RE	Data

L = low level
H = high level

* RE = read = low
WE = write = low

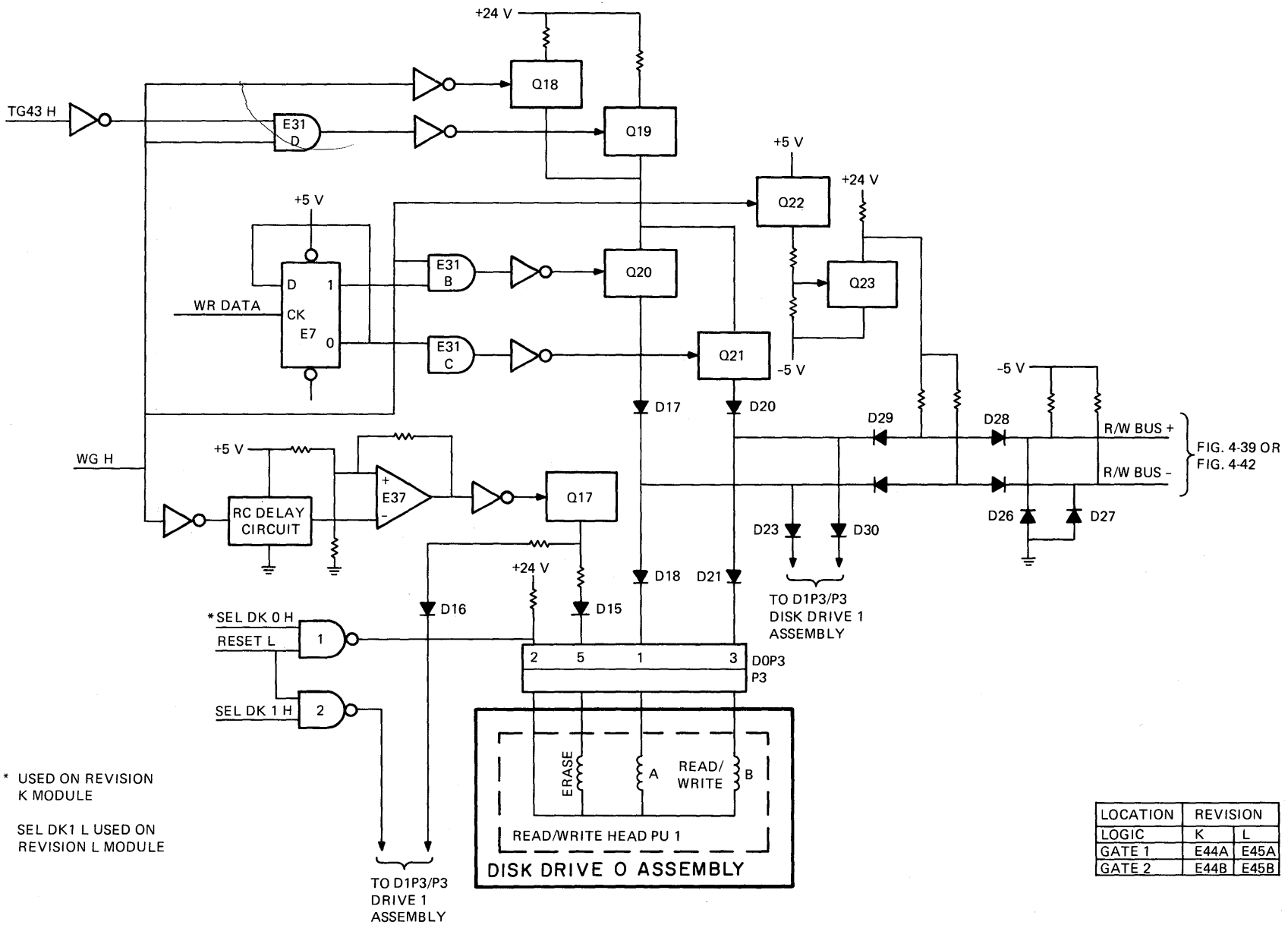
The read/write head of disk drive 0 is initially disabled by the +24 V, which connects to pin 2 of connector P3. This is the common return for the read/write and erase coils of read/write head PU1.

When disk drive 0 is selected, the high SEL DK0 H input and the high RESET L input to gate E44A will cause a low output at connector P3, pin 2, and enable the read/write head operation. When writing is to occur, the WG H signal from the FD1771 will become high and inverted, thus allowing transistor Q18 to conduct. Input signal TG43 H from the FD1771 will be low level when any track between 00 and 43 has been selected and high level for selecting tracks 44 to 76. A low TG43 H level is inverted and gated at E31A with the high WG H signal. The high output of E31A is inverted, allowing transistor Q19 to conduct.

When the WG H signal initially becomes high, it is inverted and causes the capacitor in the RC delay circuit to begin discharging from +5 V toward ground. Approximately 224 μs after the WG H signal becomes high, the output of amplifier E37 will become high. This signal is inverted, causing transistor Q17 to conduct. Current will flow through Q17 through the diode and erase coil of the read/write head. The erase coil is used to remove the residual flux changes that may have occurred in the spaces between the tracks on a disk. The 225 ns delay is the time required to allow the area on the disk where the write head current started to be positioned over the erase head.

When a sector has been completely filled with data, the WG H signal will become low and the capacitor in the delay circuit will begin to charge to the +5 V level. Amplifier E37 will hold transistor Q17 in conduction for approximately 523 μs after the WG H signal becomes low.

The WR DATA input to flip-flop E7 is composed of positive-going clock pulses, with the data information spaced between each pulse as shown in Figure 4-28. The positive transition of each pulse at the CK input will change the state of the E7 outputs, each of which is connected to a gate. The other input to each gate will be the WG H signal, which will be high when the writing is to occur. When flip-flop E7 is set, the high (1) output will produce a high output of gate E31B, which is inverted to allow transistor Q20 to conduct. Read/write head coil A will be energized through connector pin 1 of connector D0P3/P3 by the current through transistors Q18, Q19 (which are presently activated) through Q20 and diodes D17 and D18. When flip-flop E7 is cleared, read/write head coil B will be energized through pin 3 of connector D0P3/P3 by the conduction of transistor Q21 and diodes D20 and D21.



LOCATION	REVISION	
LOGIC	K	L
GATE 1	E44A	E45A
GATE 2	E44B	E45B

Figure 4-38 Read/Write Head and Control Circuits, Simplified Diagram

When the TG43 H signal is high, indicating track 44 or greater has been addressed, the output of gate E31A becomes low and inverted to prevent transistor Q19 from conducting. Transistors Q18 and Q19 are in parallel; therefore, the current through coil A or B of the read/write head is reduced when transistor Q19 is not conducting. This decreases the magnitude of the flux transitions on the shorter track lengths, which have the highest bit density.

During write operations, the high WG H signal is inverted to cause transistor Q22 to conduct. The collector of transistor Q22 will become negative and cause transistor Q23 to conduct. The collector of transistor Q23 is connected to -5 V, and the -5 V from the output of transistor Q23 will back bias diodes D24 and D29 and prevent the write currents from affecting the R/W BUS+ and R/W BUS- lines.

Diodes D16, D23 and D30 provide the current to the erase coil, and to coils A and B of the read/write head in disk drive 1 assembly when this assembly selected by the SEL DK1 H input to gate 2.

4.10.6.2 Disk Read Operations - During read operations, the write circuits shown in Figure 4-38 are disabled by a low WG H signal. Transistors Q20 and Q21 are therefore not conducting, and no write current is present in either coil A or B of the read/write head. Transistors Q22 and Q23 are also not conducting and the output of Q23 is a positive voltage, which produces a forward bias on diodes D24 and D29. The read current through D24 passes through coil A and the current through D29 passes through coil B of the read/write head. The flux transitions recorded on the tracks of a disk are sensed by both coils A and B and superimposed on the dc current levels through the coils. Diodes D25 and D28 are also biased in the forward direction by the positive voltage from the output of transistor Q23. The flux changes are transferred through the diodes to the R/W BUS+ and R/W BUS- lines.

Two versions of the read amplifier and data separator circuits are used in PDT-11/150 units. Disk Controller module 5413271 revision K contains a data separator circuit which is clocked by an 8 MHz input, and Disk Controller module 5413271 revision L contains a data separator circuit which is clocked by a 16 MHz input.

Figure 4-39 is a simplified diagram of the read amplifier and data separator circuits on the revision K module. The R/W BUS+ and R/W BUS- lines connect to the input of E43, which amplifies the detected signals. The output of E43 connects to a low-pass filter that removes the noise and high frequency components contained on the information from the read/write head. The output of amplifier E38 is applied to a differentiator circuit which shifts the peaks of the detected data by 90° to become zero crossings.

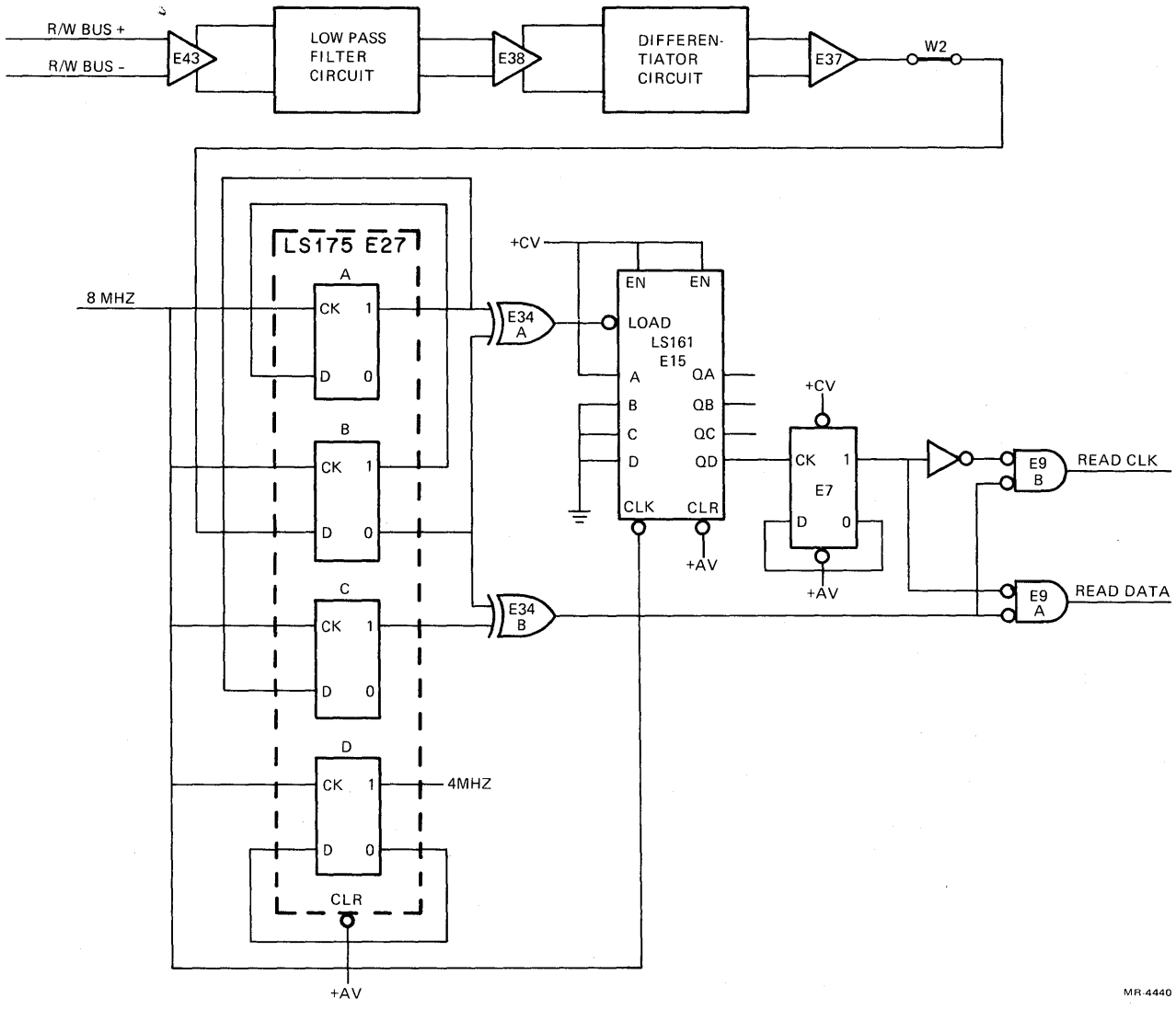


Figure 4-39 Read Amplifier and Data Separator Circuit (Revision K), Simplified Diagram

Figure 4-40 shows the read amplifier and differentiator outputs and their relationship to the recorded data on the disk. The output of E37 is a TTL-compatible signal and its transitions are directly related to the recorded information.

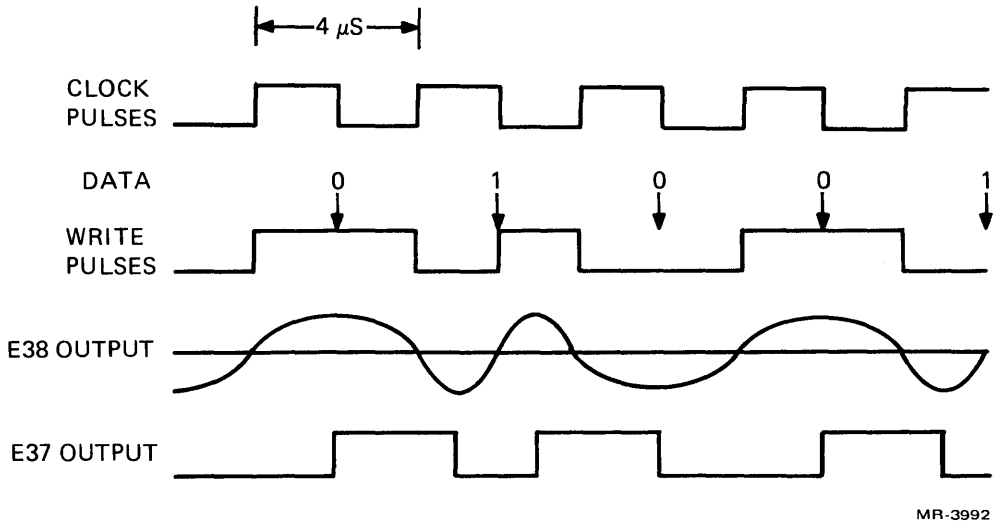


Figure 4-40 Read Amplifier and Differentiator Circuit (Revision K), Timing Diagram

The output of amplifier E37 is transferred through jumper lead W2 to the D input of flip-flop E27B of the data separator circuit. Figure 4-41 is the timing diagram for the 8 MHz data separator circuit. Flip-flops E27A, B, C and D are all clocked by the 8 MHz input pulses. If the data level to the D input of E27B was previously low for a period of more than 400 ns or four positive transitions of the clock pulses, flip-flops E27B, A, and C will be cleared. The output of gate E34A will be high and will be present on the LOAD input of counter E15. The output of gate E34B will also be high to disable gates E9B and E9A, resulting in a low READ CLK and READ DATA output.

When a flux transition is detected on the disk, due to either a clock pulse or data = 1, the D input to flip-flop E27B will become high and the next positive transition of the 8 MHz clock input will set E27B. The low (0) output of E27B is gated with the low (1) output of E27A, resulting in a high-to-low transition at the output of E34A. This signal will load a preset count of binary 1 into counter E15, and the counter will start the count of the positive transitions of the 8 MHz pulse inputs.

The low (0) output of flip-flop E27B is also gated at E34B with the low (1) output of flip-flop E27C, causing the output of E34B to become low. This signal is applied to gates E9A and E9B. With flip-flop E7 cleared, the low (1) output of E7 will allow the signal from gate E34B to produce a positive output of E9B.

The (1) output of flip-flop E27B connects to the D input of flip-flop E27A. When E27B was set, the high level on the D input allowed E27A to be set by the next low-to-high transition of the 8 MHz clock pulse. The high (1) output of E27A will cause the output of E34A to become high and will also provide a high level to the D input of flip-flop E27C. The next positive transition of the 8 MHz pulse will set flip-flop E27C and the high (1) output of E27C will cause the output of E34B to become high. The output pulse duration from E34A is .125 μs, and .250 μs from E34B.

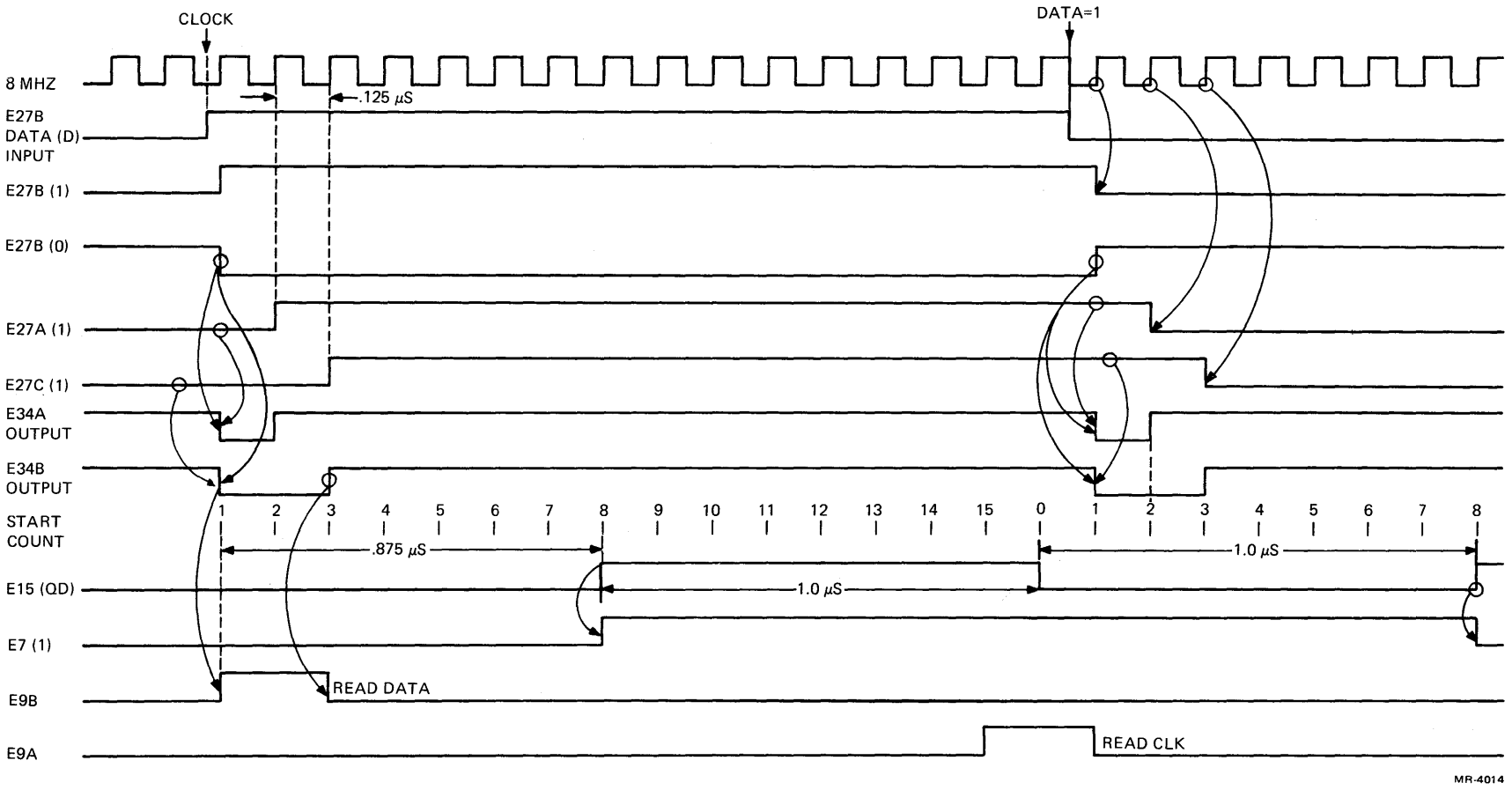


Figure 4-41 Data Separator Circuit (Revision K), Timing Diagram

The binary count of E15 that was initiated by the low output of E34A will cause the QD output of E15 to become high at the binary count of eight. The low-to-high transition of QD will set flip-flop E7. The high (1) output of E7 is inverted and enables gate E9B. Flip-flop E7 will remain set until the next low-to-high transition of the QD output of E15, which will occur again at a binary count of eight.

If the next data or clock transition occurs at the D input of E27B within a 2.875 μs duration after the first transition, gate E9A will be held enabled by flip-flop E7 and the output pulse of E34B will produce a positive (READ DATA) output at E9A.

Each data or clock transition will generate a .25 μs pulse output from either E9A or E9B. If a second transition occurs within 2.875 μs of the first, the .250 μs pulse will occur at the gate output opposite to that where the first pulse occurred. If the second transition occurs after the 2.875 μs interval, the output will occur at the same output as the first pulse.

Figure 4-42 is a simplified diagram of the read amplifier circuits and data separator logic on the revision L module. Figure 4-43 shows the relationship of the signals in the read amplifier circuits to the recorded data.

The information from the read/write head connects to amplifier E46 through the R/W BUS+ and R/W BUS– lines. The output of E46 is applied to a low-pass filter network that removes noise and high frequency components from the read head. The output of the filter is applied to a differentiator circuit that phase shifts the information so that the detected signals result in a zero crossing at the input of amplifier E44. The output of E44 is amplified by E39 to provide the TTL-compatible signals with level changes directly related to the clock and data information read from the disk. The output of E39 is transferred through to jumper lead W1 on the F5 RAW DATA H line to the data separator circuit.

The data separator circuit receives the data transitions and separates the information into either clock pulses or data pulses, depending on the time interval between pulses. The data separator circuit is clocked by the F1 16 MHz square wave signal, which controls the input flip-flops of E36 and the 8-bit binary counter consisting of E26 and E16.

Figure 4-44 (Sheets 1 and 2) shows the relationship of the signals in the circuit to the 16 MHz clock inputs.

When ac power is applied to the unit, the F1 RESET L signal will be initially held low by the RC network shown in Figure 4-30, Sheet 1. The low F1 RESET L level (see Figure 4-42) will clear the E36 flip-flops and the 8-bit binary counter.

When a low-to-high data transition occurs on the F5 RAW DATA H input to flip-flop E3A1, the flip-flop will be set on the next positive transition of the 16 MHz clock pulse. The high (1) output of E36A is applied to the D input of flip-flop E36B, which will be set on the next positive transition of the 16 MHz clock pulse. The high (1) output of E36B is applied to the D input of flip-flop E36C, which will also be set on the next positive transition of the 16 MHz clock pulse. The high (1) output of E36C connects to the D input of E36D and to gate E34A. Initially, the (1) output of E36D is low and the signal is inverted and applied with the high (1) output from flip-flop E36C at gate E34A. This produces a low F5 TRX L signal from gate E34A that will remain low until flip-flop E36D is set by the next positive transition of the 16 MHz clock. The F5 TRX L signal will become low whenever a transition occurs on the F5 RAW DATA H line. The low output on F5 TRX L will cause one of four counts to be entered into the 8-bit binary counter and will clear flip-flop E36E on the positive transition of the 16 MHz clock. Flip-flop E36E is normally held in the set condition by the high F5 TRXL level. The (1) output of E36E connects to a 225 ns pulse generator E7. When signal F5E H goes low, it will trigger E7 and produce a low 225 ns pulse output. This pulse will be gated through gate E9A or E9B, depending on the state of the QB output of the binary counter E16. The QB output is the F5 WINDOW H signal.

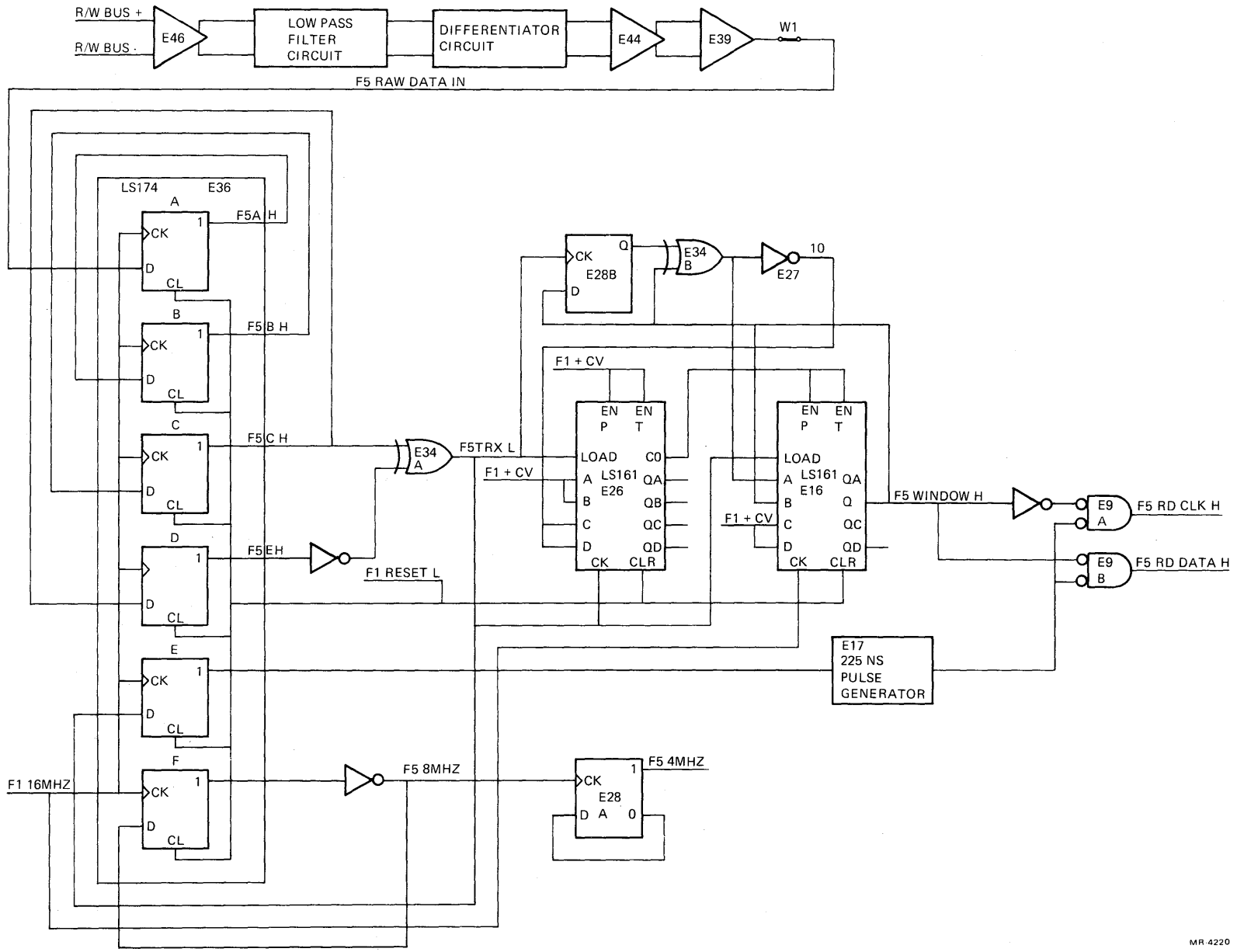


Figure 4-42 Read Amplifier and Data Separator Circuit (Revision L), Simplified Diagram

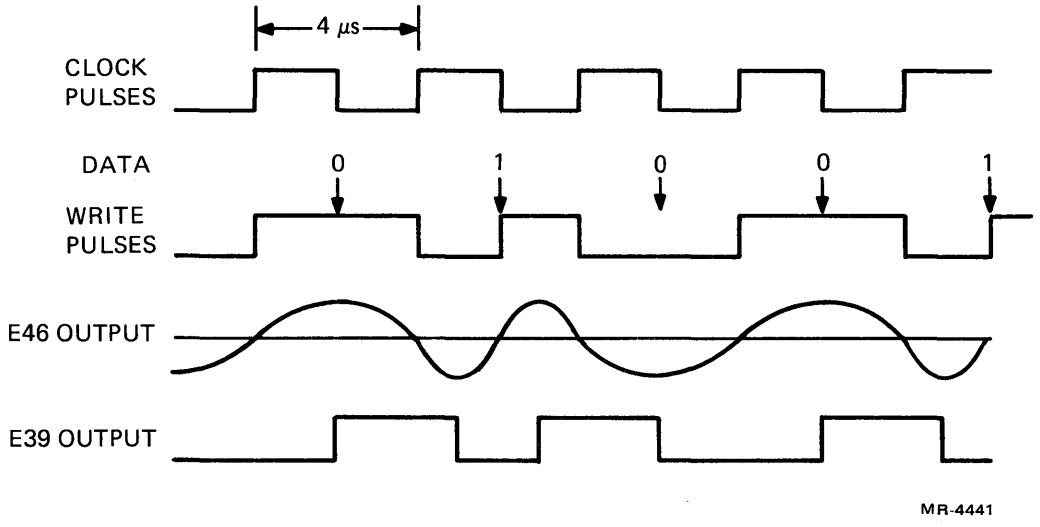


Figure 4-43 Read Amplifier and Differentiator Circuit (Revision K), Timing Diagram

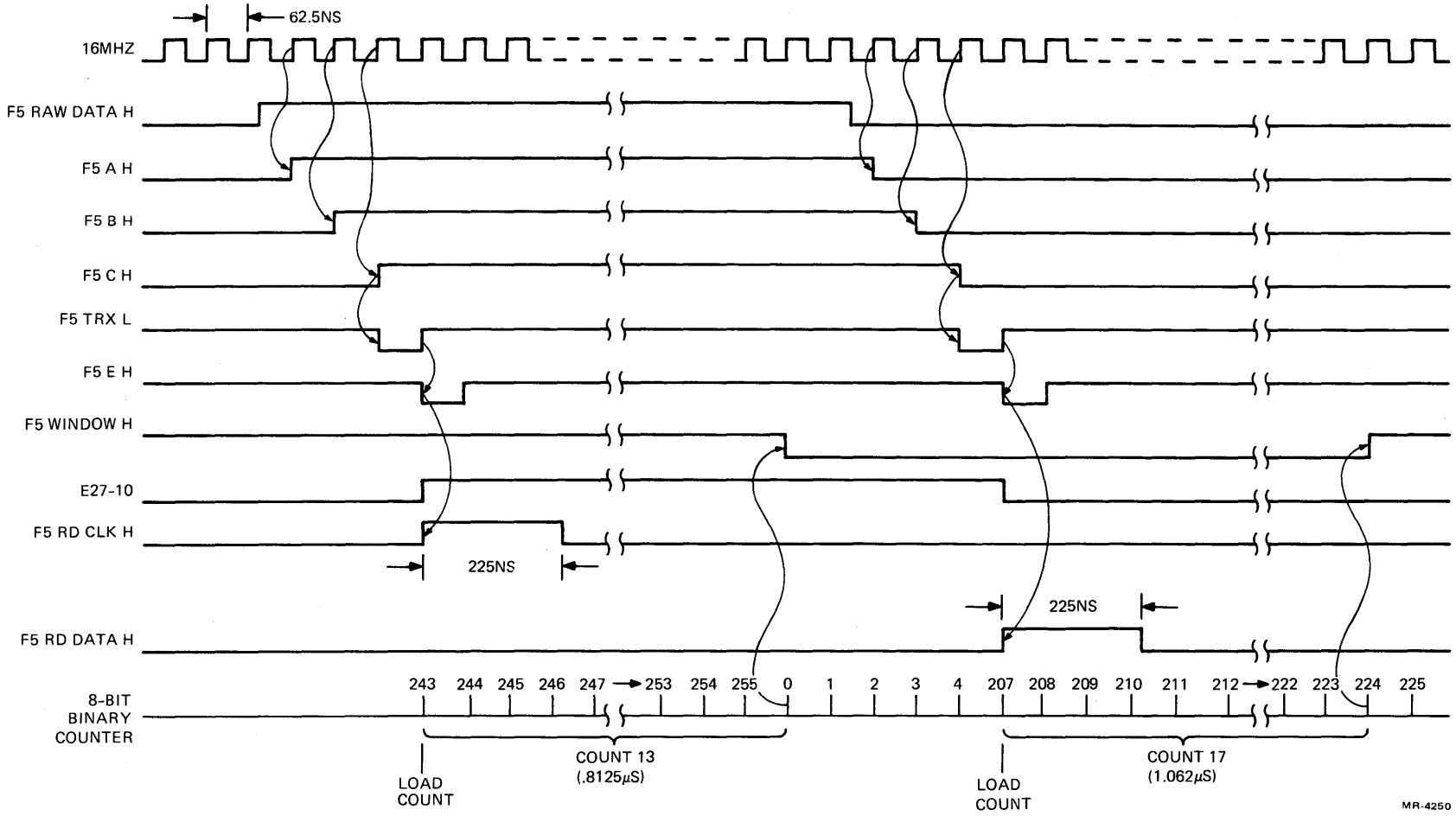


Figure 4-44 Data Separator Circuit (Revision L), Timing Diagram
(Sheet 1 of 2)

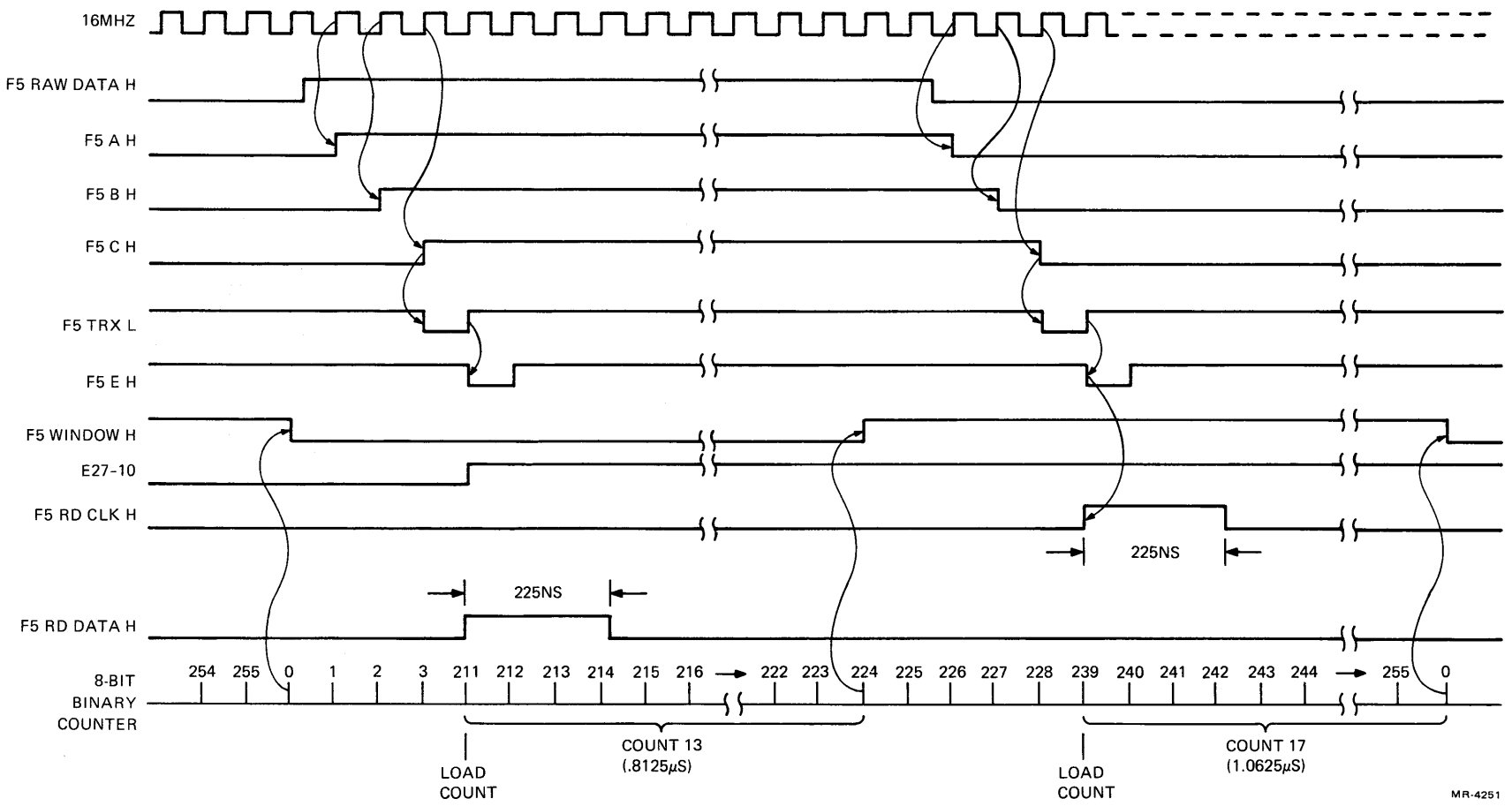


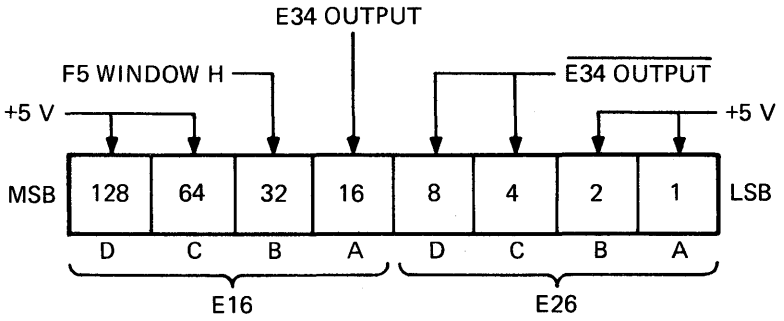
Figure 4-44 Data Separator Circuit (Revision L), Timing Diagram
(Sheet 2 of 2)

The low-to-high transition of the F5 TRX L signal will also load the state of the F5 WINDOW H signal into flip-flop E28A.

When the F5 RAW DATA H becomes low due to a detected transition, flip-flops E36A, E36B, E36C and E36D will be cleared by the 16 MHz clock pulses in a manner similar to that described previously, and a low F5 TRX L pulse will again be generated. A 225 ns pulse will occur at the output of gate E9A or gate E9B, and one of four counts will be entered into the binary counter.

Figure 4-45 shows the binary configuration of the 8-bit counter and the four counts that can be entered. The binary counter will free-run under control of the 16 MHz clock, through a total count of decimal 256. Inputs A and B of E26 and inputs C and D of E16 connect to F1 + C V and are always entered as (1). Input B of E16 connects to the F5 WINDOW H signal. Input A of E16 connects to the output of gate E34A and inputs C and D of E26 are connected to the inverted output of E34A. The decimal counts that can be entered are 211, 243, 207 and 239. When counts 211 or 243 are entered, thirteen 16 MHz clock pulses are required to change the state of the QB output of E16. When counts 207 or 239 are entered, seventeen 16 MHz clock pulses are required to change the QB output level of E16. If no count is entered, the QB output signal F5 WINDOW H, will change states every thirty-two 16 MHz clock pulses.

Figure 4-46 shows the time related to the 13-count and 17-count intervals. The minimum delay interval between the data transition on F5 RAW DATA H and the start of the count is .1875 μs, or three 16 MHz clock pulses; the maximum delay interval is .250 μs, or four 16 MHz clock pulses. The value of the count to be entered is a function of the existing level of the F5 WINDOW H signal when the load pulse occurs, and the level of the F5 WINDOW H signal when the previous load pulse occurred. Flip-flop E28A stores the level at each load pulse on F5 TRX L.



BINARY COUNTER

	LOAD VALUE	E16				E26			
		QD	QC	QB	QA	QD	QC	QB	QN
COUNT 13	211	1	1	0	1	0	0	1	1
	243	1	1	1	1	0	0	1	1
COUNT 17	207	1	1	0	0	1	1	1	1
	239	1	1	1	0	1	1	1	1

MR-4252

Figure 4-45 8-Bit Binary Counter Configuration and Load Counts

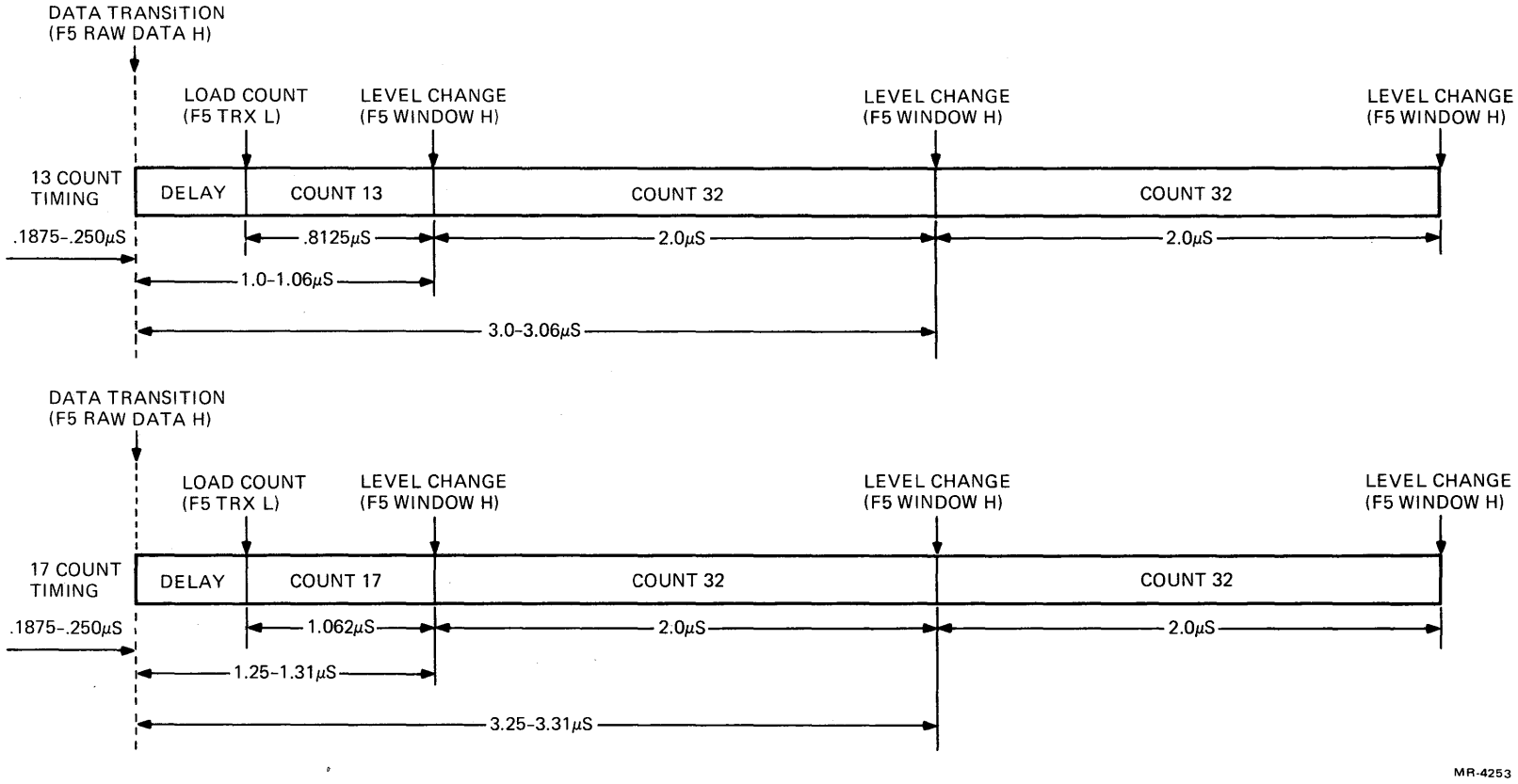


Figure 4-46 13- and 17-Count Intervals, Timing Diagrams

When the counter is loaded, the decimal count is always selected so that the level of the F5 WINDOW H signal will be the same as its level prior to the load pulse. This is caused by the F5 WINDOW H signal connected to the B input of E16. If the F5 WINDOW H signal is low, either count 211 or 207 will be entered; if the F5 WINDOW H signal is high, either count 243 or 239 will be entered.

The selection of the 13-count interval or 17-count interval depends on both the F5 WINDOW H level previously stored in flip-flop E28A and the current value of the F5 WINDOW H level. A 17-count interval will be selected if the level of the F5 WINDOW H signal is the same as the value stored at the (1) output of flip-flop E28 by the previous load pulse. If the level of the F5 WINDOW H signal is different from the value stored, a 13-count interval will be entered into the counter. The time of the 13 count interval is .8125 μs and the time of the 17-count interval is 1.062 μs. The total time from the data transition to a change in the F5 WINDOW H level will be either 1.0–1.06 μs for a 13-count interval, or 1.25–1.31 μs for a 17-count interval. The F5 WINDOW H signal controls the outputs of gates E9A and E9B; therefore, a 17-count interval will hold the F5 WINDOW H signal at its existing level for .250 μs longer than the 13-count interval will. At the end of either count interval, the F5 WINDOW H will change and remain at that level for a 32-count interval, or 2.0 μs, after which it will again change. A high F5 WINDOW H level enables gate E9A and a low level enables gate E9B. If the second data transition occurs within the first 32-count interval, the F5 WINDOW H level will be different when each of the transitions occurs, and a 13-count interval will be selected. This effectively decreases the time until the F5 WINDOW H level changes. If the second data transition occurs after the first 32-count interval, the F5 WINDOW H level will be the same when each data transition occurs, and the 17-count interval will be selected.

When successive clock pulses are read from the disk at a normal rate of 4.0 μs, a 17-count will continually be entered into the counter, allowing more time to detect the next pulse. When the information read from the disk is alternating clock pulses and data = 1 transitions at a normal rate of 2.0 μs, a 13-count interval will continually be entered into the counter and will decrease the time allowed to detect the next pulse.

The F1 16 MHz input from the crystal-controlled pulse generator is divided by two by flip-flop E36B to become a F5 8 MHZ clock, and again by flip-flop E28 to become a F5 4 MHZ clock used as an input to the 8085 controller microprocessor.

4.11 H7833 POWER SUPPLY MODULE (DWG. NO. 5413343)

The H7833 power supply module provides the dc voltages required by the PDT-11/150. Figure 4-47 is a simplified diagram that shows the main functional elements of the H7833 power supply. The input voltage is passed through the M EI filter FL1 at the rear panel assembly and distributed to the supply by a cable assembly. The H7833 operates from the following inputs.

Voltage	Frequency
90–128 V RMS	
180–256 V RMS	47–63 Hz

The selection of the input ac voltage range is made by the slide switch S1 mounted on the printed circuit board. In the 115 V position, the input rectifier circuit is connected in a voltage double configuration. In the 230 V position, the input rectifier circuit is connected in a full-wave bridge configuration. The output of the rectifier circuits supply the high voltage to operate the switching and snubber circuits which control the conduction of the high frequency transformer T1.

The 115 V or 230 V ac input voltage is connected to the +12 V startup power supply. This supply generates +12 V dc used to power the 20 MHz oscillator, pulse width modulator, error amplifier and associated control circuit functions.

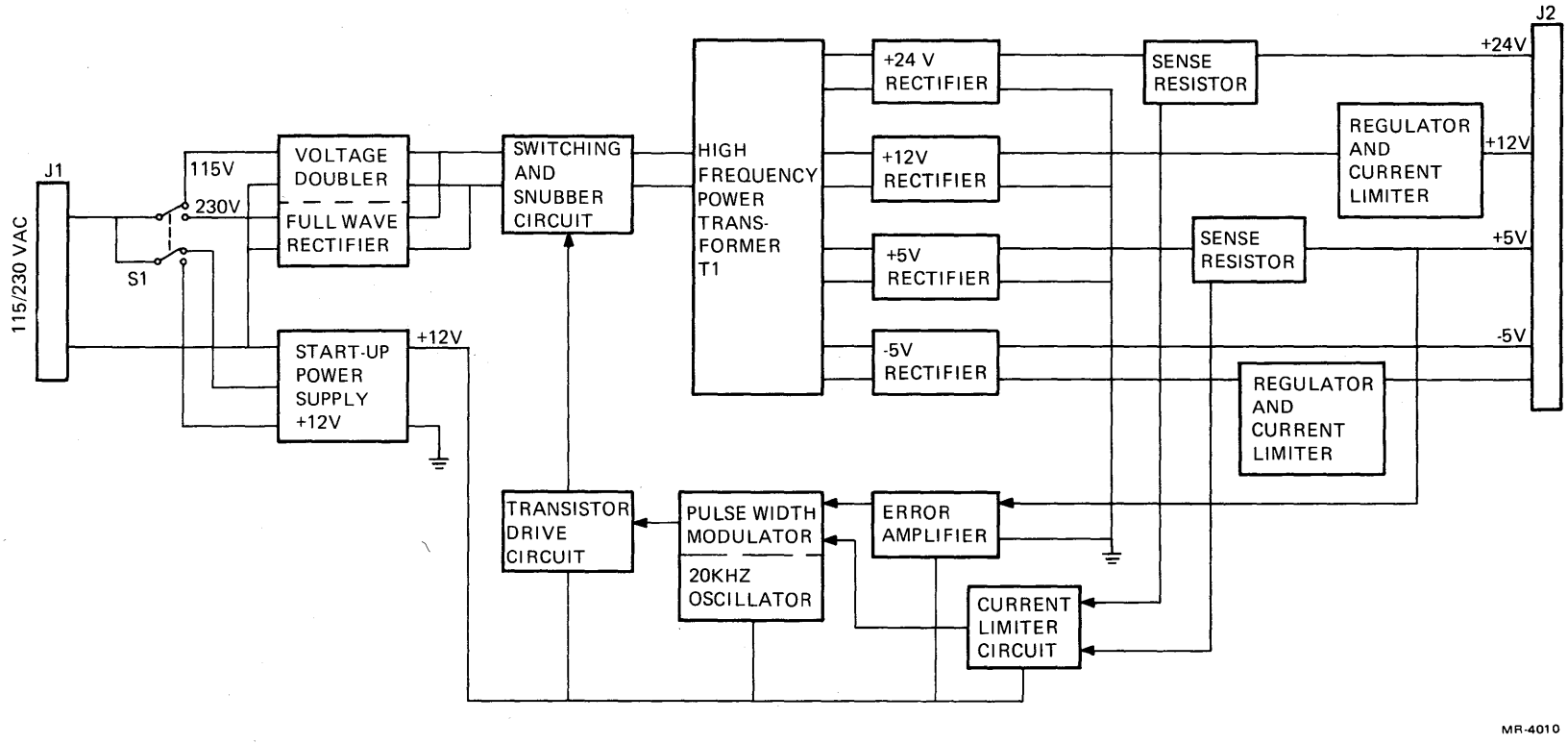


Figure 4-47 H7833 Power Supply, Simplified Block Diagram

The output of the 20 KHz oscillator is connected to the pulse width modulator circuit, which is used to control the conduction of the transistor in the transistor drive circuit. This transistor is switched at the 20 KHz rate to generate the high frequency required by transformer T1.

The outputs of transformer T1 are rectified to supply the following maximum dc voltages:

+5 V at 5.6 A
+12 V at 1.6 A
+24 V at 2.0 A
-5 V at 270 mA

The +5 V dc and +24 V dc outputs are current-regulated by a sense resistor and a current-limiting circuit. This circuit monitors the voltage developed across the resistors and develops an output voltage that is related to the current changes through the sense resistors. The pulse width modulator circuit varies the width of the pulses supplied to the transistor drive circuit according to the voltage developed by the current-limiting circuit.

The +5 V dc output is monitored by the error amplifier circuit, which is also connected to the pulse width modulator circuit. Changes in the +5 V dc will also vary the width of the pulse to the transistor drive circuit, thereby changing the +5 V dc level. The +12 V dc and -5 V dc are regulated and controlled by the current-limiting circuit.

4.11.1 Input ac Voltage Circuits

Figures 4-48 and 4-49 show the input circuit configurations for the 115 V ac and 230 V ac selections, respectively. The 115 V position of switch S1 is selected for the 90–128 V RMS input voltage range and the 230 V switch position is selected for the 180–256 V RMS input voltage range.

4.11.1.1 115 V ac Voltage Doubler Circuit – Figure 4-48 shows the voltage doubler circuit selected by switch S1. On the first half of the input cycle, with the voltage on connector P1-1 more positive than that on P1-3, diode D22 will conduct and capacitor C3 will be charged with the polarity shown.

On the second half of the input cycle, the voltage on connector P1-3 will be more positive than that on P1-1 and diode D23 will conduct. Capacitor C2 will be charged with the polarity indicated. The voltage across the A and B lines of the circuit will be the total of the voltage across capacitors C22 and C23, or approximately twice the RMS input voltage. Thermistor R1 limits the amount of input current during the warmup period of the power supply.

The 115 V position of switch S1-B supplies the input ac power to one-half of the primary winding of the startup transformer T3. This transformer is part of the +12 V dc supply used to provide power to the elements internal to the power supply.

4.11.1.2 230 V ac Full Wave Rectifier Circuit – When switch S1 is in the 230 V position, as shown in Figure 4-49, the input circuit is configured as a full-wave rectifier. On the first half of the input cycle, when the voltage on connector P1-1 is more positive than that on P1-3, diodes D24 and D22 will conduct and capacitors C2 and C3 will be charged with the voltage polarity as shown. During the next half of the input cycle, the voltage on connector P1-3 will be more positive than that on P1-1. Diodes D23 and D25 will conduct and capacitors C2 and C3 will again be charged with the same voltage polarity as during the first half of the cycle. The output voltage at lines A and B will be approximately equal to the RMS of the input voltage. Thermistors R1 and R2 limit the amount of input current during the warmup period of the power supply.

The input ac voltage will also be applied across both primary windings of transformer T1 through switch S1-B.

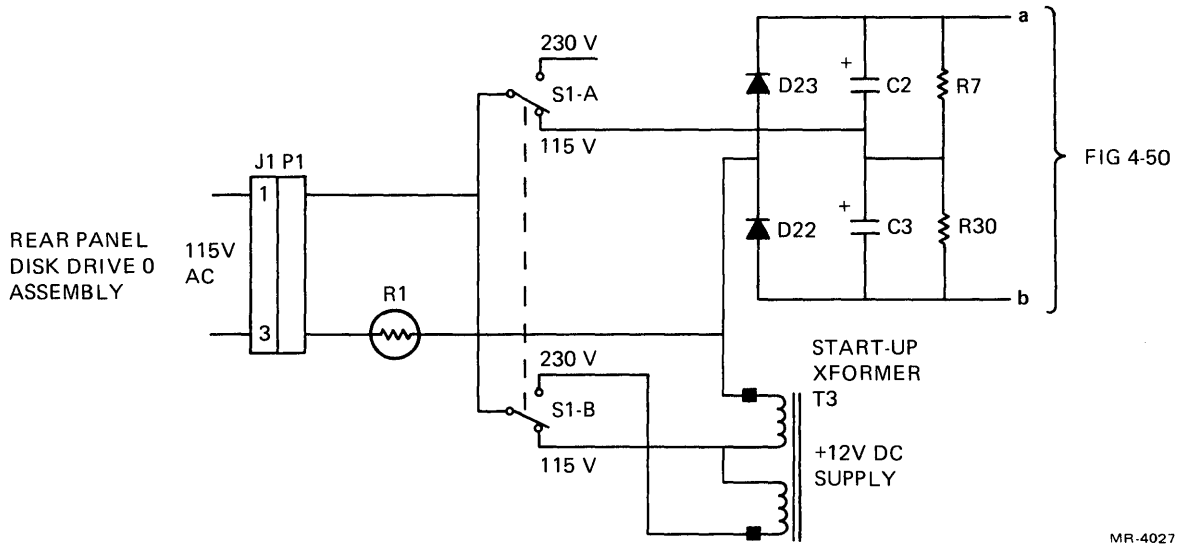


Figure 4-48 115 V ac, Voltage Doubler Circuit, Simplified Diagram

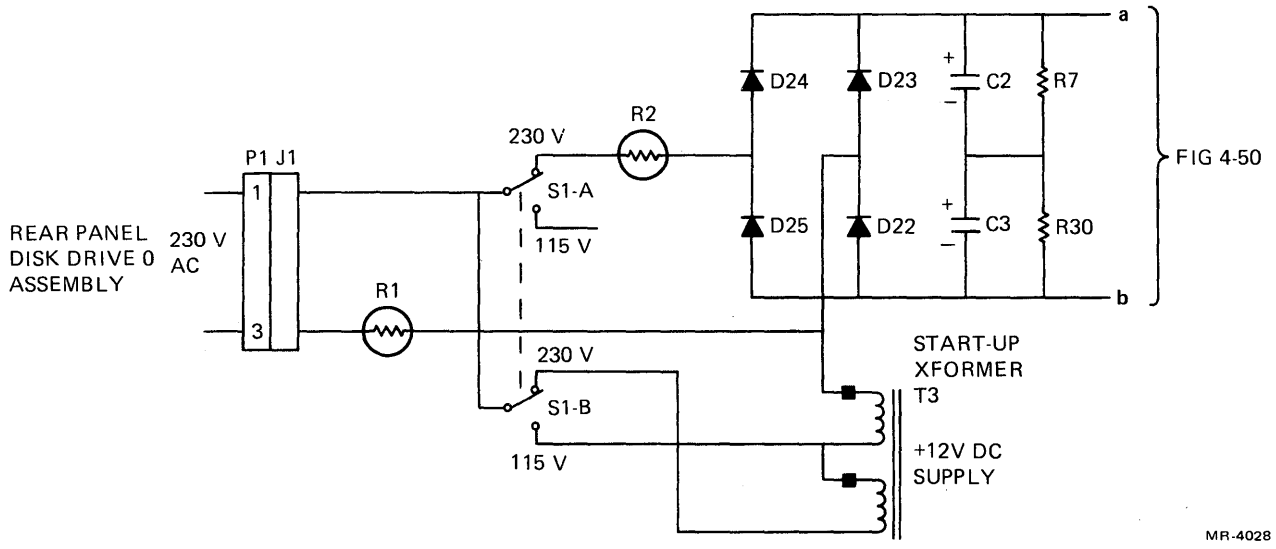


Figure 4-49 230 V ac, Full Wave Rectifier Circuit, Simplified Diagram

4.11.2 Flyback Inverter Circuit

The A and B lines from the input voltage circuits described in Paragraph 4.11.1 supply the dc voltage to the flyback inverter circuit shown in Figure 4-50. This circuit consists of a high voltage transformer T1, and a transistor drive circuit consisting of transistors Q1, Q2, and a coupling transformer T2. The flyback inverter circuit converts the dc voltage at the primary winding of transformer T1 to a 20 KHz ac voltage. The outputs of the four secondary windings of T1 are rectified and regulated to provide the dc voltage requirements of the PDT-11/150. The regulation of the output voltages is controlled by the conduction time of transistor Q1, which is switched by the coupling circuit at the 20 KHz rate. When transistor Q2 is conducting, transistor Q1 is not conducting. The conduction of Q2 is controlled by the output of the pulse width modulator in the control circuit. The rectified output of the +5 V dc from the power supply is sensed by the control circuit to adjust the conduction duration of transistor Q2.

When transistor Q1 is conducting, the current through the primary winding of T1 induces a current in the secondary windings, which reverse biases the rectifier diodes. When transistor Q1 is disabled, the collapsing magnetic field of the primary winding of T1 reverses the voltage polarity of the secondary windings and the rectifier diodes will conduct. When the base of transistor Q2 is high, current from the internal +12 V dc supply will flow through diode D10, resistor R14, the primary winding of T2, and through Q2 to ground. The voltage induced in the secondary winding A of T2 will use diode D1 to conduct and prevent a forward bias on transistor Q1. When the base of Q2 becomes low, transistor Q2 will stop conducting and the induced voltage in the primary winding of T2 will be reversed. The base of transistor Q1 will then become more positive than the emitter due to the induced voltage in the secondary winding A, and Q2 will conduct. The current through Q2 will induce a voltage in the secondary winding B, which aids the forward bias developed by the secondary winding A. The current through the secondary windings of T2 will also induce a current in the primary winding of T2. When transistor Q2 starts conducting again, capacitor C8 will discharge through the primary winding of T2 and induce a current in the secondary winding B. This causes a reverse current to flow from the emitter to the base of Q1, which aids in stopping the conduction of Q1.

Components R8, C1 and D12 in the primary circuit of transformer T1 control the rate at which the collector voltage of transistor Q1 will rise; components R10, D40, and D11 limit the maximum voltage at the collector of transistor Q1. Components C8, R13, D14, D6 and D15 comprise a circuit that aids stopping the conduction of transistor Q1.

4.11.3 Control Circuit

Figure 4-51 shows the control circuit, which consists of a 5 V reference voltage, an error amplifier, a current limiter circuit, a 20 KHz clock pulse oscillator and a pulse width modulator. The 20 KHz oscillator and the pulse width modulator are contained in an NE556 IC element E1. Refer to the *Signetics Digital Linear MOS Data Book* for detailed information on the NE556.

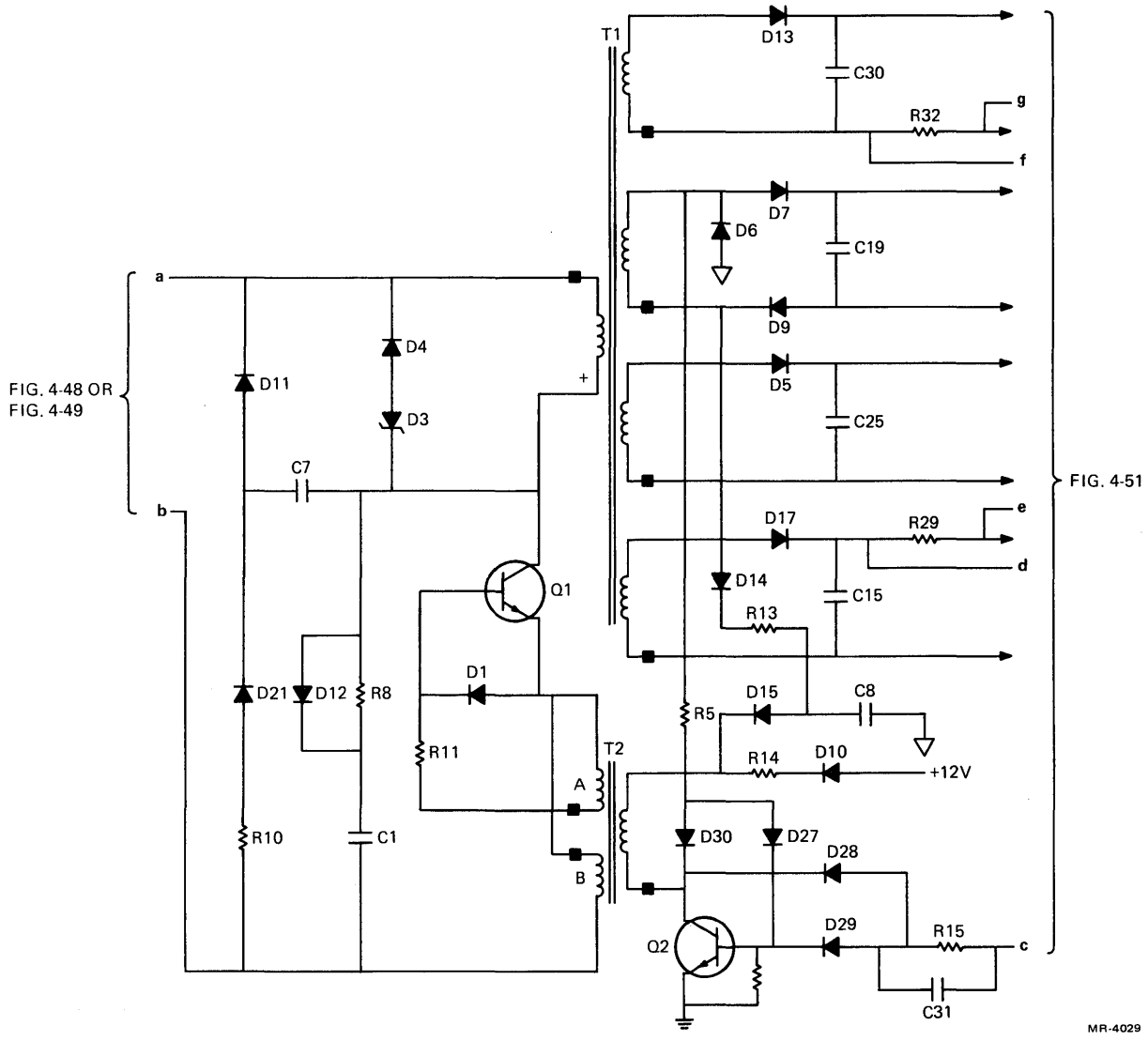


Figure 4-50 Flyback Inverter Circuit, Simplified Diagram

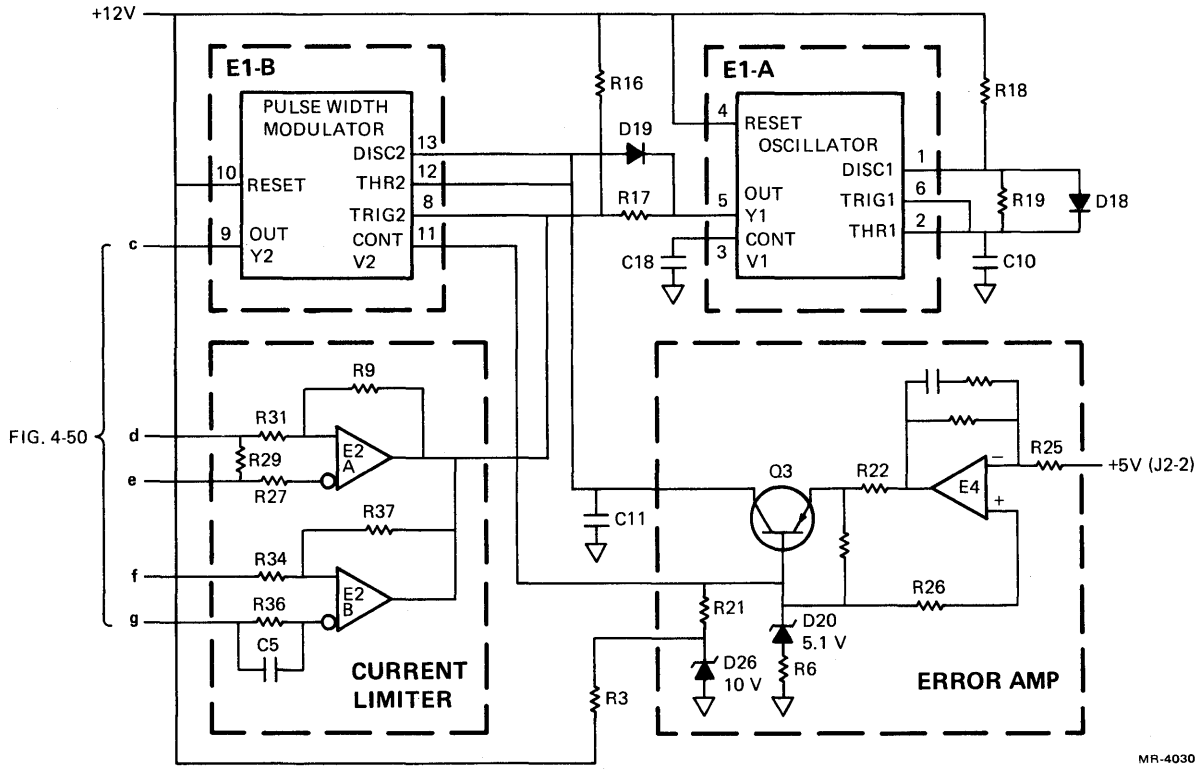


Figure 4-51 Output Control Circuit, Simplified Diagram

4.11.3.1 Oscillator and Pulse Width Modulator – The E1A oscillator circuit generates a rectangular pulse output every 50 μs. Figure 4-52 shows the timing of the signals related to the control circuits. The oscillator timing is controlled by resistor R18 and capacitor C10 for the duration that the output is high, and by R19 and C10 for the duration that the output is low. The output pulses from the OUT (Y1) terminal of E1A are transferred through R17 to the TRIG2 input of the pulse width modulator E1B. When the output of the oscillator is low, the output OUT (Y2) of the pulse width modulator is held high. The high output at point A of Figure 4-51 will cause transistor Q2 to conduct. The timing capacitor C11 of the pulse width modulator E1B is prevented from charging by the forward bias on the diode D19. When the output of the oscillator becomes high, capacitor C11 will become charged from the voltage controlled current source of the error amplifier circuit. The base of transistor Q3 and the CONT V2 input to the pulse width modulator E1B are connected to the 5.1 V reference diode D20. When the charge on capacitor C11 is 5.1 V, the output OUT (Y2) of E1-B will become low, and transistor Q2 (see Figure 4-51) will stop conducting, which will cause transistor Q1 to conduct. When the oscillator output becomes low again, the output of the pulse width modulator will become high, and capacitor C11 will be discharged. The width of the pulse to transistor Q2 is determined by the charge time of capacitor C11 during the time the oscillator pulse is high. As the charge time of C11 decreases, the duration of the output pulse to Q2 increases.

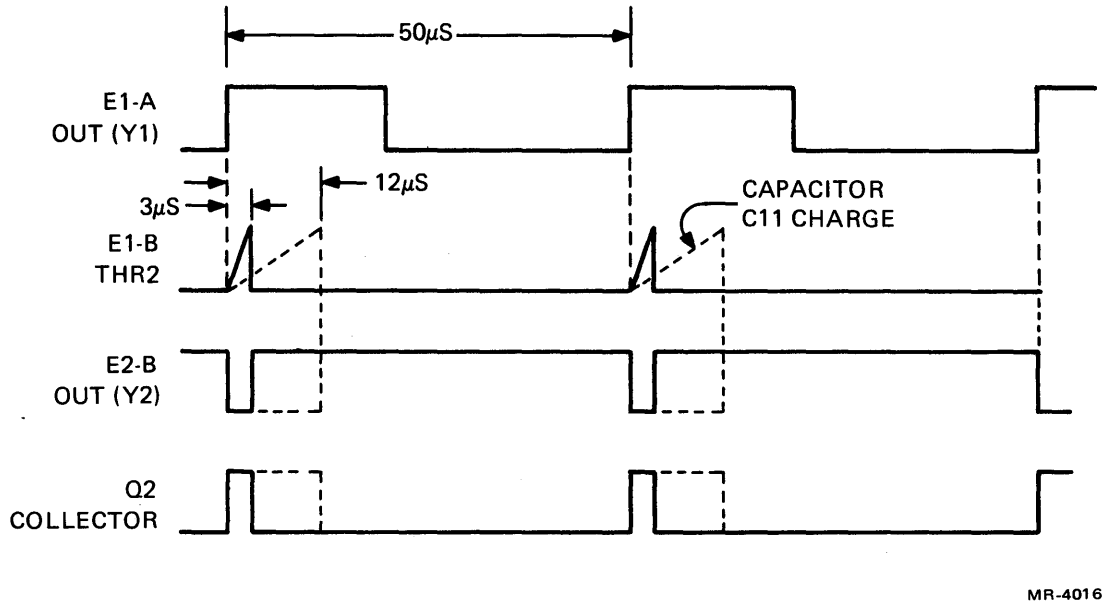


Figure 4-52 Control Circuit, Timing Diagram

4.11.3.2 Error Amplifier Circuit – Figure 4-51 shows the error amplifier circuit of the power supply. This circuit monitors the +5 V dc output of the supply and controls the conduction time of the high voltage transformer. The negative input to comparator E4 is connected through R25 to the +5 V dc at connector J2-2. The positive input is connected to the 5 V reference diode D20. When the +5 V dc increases in voltage, the different voltages at the inputs at comparator E4 will produce a lower voltage at the output of E4. During the charge time of capacitor C11, the lower emitter voltage of Q3 will increase the time of the charge on C11 to reach +5 V. This results in an extension of the time that transistor Q1 is not conducting, which reduces the +5 V dc voltage at the output of the supply. When the +5 V dc decreases, the voltage at the emitter of Q3 will increase and the charge time of capacitor C11 will decrease. This will cause the conduction time of Q1 to increase and raise the +5 V dc output voltage.

4.11.3.3 Current Limiter Circuit – The current limiter circuit, shown in Figure 4-51, prevents an external short on the +5 V dc and +24 V dc outputs from causing damage to the supply.

Comparator E2A monitors the voltage developed across series resistor R29 and comparator E2B monitors the voltage developed across series resistor R32. The output of each comparator is connected to the TRIG2 input of the pulse width modulator E1-5 and is normally high. When excessive current occurs through the sense resistors, the voltage across the comparator input will increase and cause the comparator outputs to become low. The output of the pulse width modulator will become high, which will prevent transistor Q1 from conducting and will disable the output voltages of the supply.

When the current through the sense resistors returns to the normal limit, the comparator outputs will again become high to allow the pulse width modulation output to control the conduction of transistor Q1.

CHAPTER 5
SERVICE

This chapter provides the detailed information required to evaluate the performance of the PDT-11/150 and to determine the cause of a failure when one occurs. Also included are the procedures for removal and replacement of the modules, cables and assemblies within the unit.

5.1 PERFORMANCE TESTS AND FAULT ANALYSIS

Table 5-1 is a fault isolation chart that lists the symptoms and probable causes of failures indicated on the front panel or the console terminal display during normal program operations. The self-test diagnostic programs and the system exerciser programs can be performed to further isolate equipment malfunctions.

The self-test diagnostic programs are permanently stored as microcode in the ROMs of the Intelligence module, the RAM module, and the Disk Controller module. With the test mode selected by the switch on the rear panel and ac power applied, the diagnostic program of the Intelligence module and Disk Controller module are simultaneously initiated and automatically sequence through the individual test of the program. When a fault occurs the "1" LED indicator on the front panel will light. When the error is detected, the specific test being performed is displayed by groups of LED indicators located internally on the Intelligence module and Disk Controller module. When an error is detected during the LSI-11 microprocessor and RAM module test, an address is displayed on the console terminal, indicating the location of the specific test being performed when the error occurred.

More complete testing of the PDT-11/150 may also be initiated through the use of the exerciser program (stored on a flexible disk), which contains a comprehensive test operation for the TIM group and disk units.

The TIM group assembly consists of the Intelligence module, the RAM module and the Perpiheral module.

NOTE

The PDT-11/150 system exerciser disk (CVKDAB0) can be ordered through your local DIGITAL sales office. The ordering designations are as follows:

Flexible Disk and Listing - ZJV03-RY
Flexible Disk only - ZJV03-PY
Listing only - ZJV03-RZ

Table 5-1 PDT-11/150 Fault Isolation Chart

Symptoms	Probable Cause	Corrective Action	Reference
		Power Failure Indications	
No response when the power switch is set to the ON position (fan not operative and front panel indicators not lighted).	1. Ac power cord not connected.	Check ac power cord connections at rear panel and at ac power outlet.	1. Fig. 2-3
	2. No power at ac outlet.	Check main power fuse at distribution panel and replace.	
	3. Defective ac power cord.	Replace cord.	3. Appendix A
	4. Internal ac power distribution harness defective.	Repair or replace harness.	4. Para. 5.3.2
No response when the power switch is set to the ON position (fan operative and front panel indicators not lighted).	1. Rear panel fuse.	Replace fuse.	1. Fig. 2-3
	2. Defective ac power distribution to power supply.	Repair or replace harness or cable.	2. Para. 5.2.2
	3. Defective dc power supply.	Replace power supply.	3. Para. 5.3.11
	4. Defective dc power distribution.	Replace cable or connectors.	4. Para. 5.2.3

Table 5-1 PDT-11/150 Fault Isolation Chart (Cont.)

Symptoms	Probable Cause	Corrective Action	Reference
		Front Panel or Console Failure Indications	
During normal operation, a detected error causes front panel indicators 1 or 2 to light. *or* During normal operation, an error indication is displayed on the console terminal. *or* During normal operation, an improper response or no response occurs during communication between the console terminal and the PDT-11/150 unit.	Hardware or software malfunction.	Perform self-test diagnostic program and system exerciser program to isolate cause of failure. Check disk drive failure indications.	Fig. 3-1; Para. 3.3 and Para. 5.1
		Disk Drive Failure Indications	
Disk drive 0 or 1 spindle not rotating.	1. Drive belt broken or not in position.	Replace drive belt.	1. Para. 5.5.2
	2. No ac power to disk drive unit.	Repair or replace ac power harness.	2. Para. 5.5.2
	3. Defective drive motor.	Replace disk drive assembly.	3. Para. 5.3.1.2

5.1.1 LED Indicator Locations

Figure 5-1 shows the location of the five LED indicators on the Intelligence module and the four LED indicators on the Disk Controller module. The front panel indicators mounted at the edge of the Peripheral module are also identified. To view the indicators, remove the top cover assembly, following the procedures in Paragraph 5.3, and raise the TIM group assembly by performing steps 4, 5, and 6 of Paragraph 5.3.4.1.

5.1.2 Fault Isolation Procedures

Figure 5-2 (Sheets 1–3), a flow chart showing the sequence of the self-test programs, identifies each of the tests being performed. This chart is used with Tables 5-2 through 5-5 to identify easily the test number displayed by the LED indicators on the Intelligence module and Disk Controller module, or to identify an address displayed on the console terminal during the LSI-11 microprocessor and RAM module test.

The tests performed in Figure 5-2 (Sheets 1–3) are enclosed in blocks. The number at the top right-hand corner of each block indicates the table that contains a more detailed description of the test. These tables include the octal code test number displayed by the LED indicators and the probable hardware cause of the failure. An "X" entered in the LED indicator columns of Tables 5-2 through 5-5 specifies a lighted condition of the lamp.

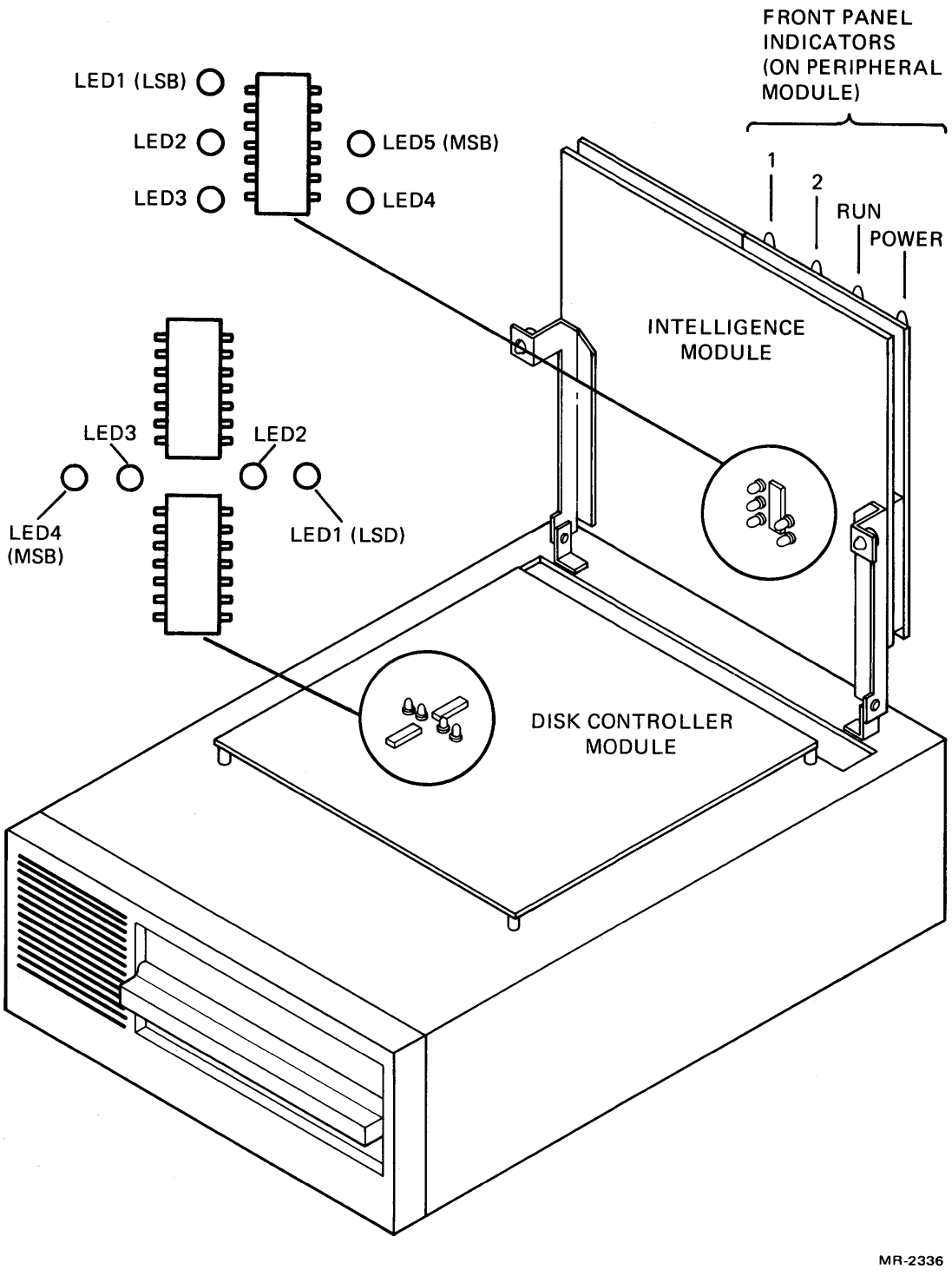


Figure 5-1 Self-Test LED Indicator Locations

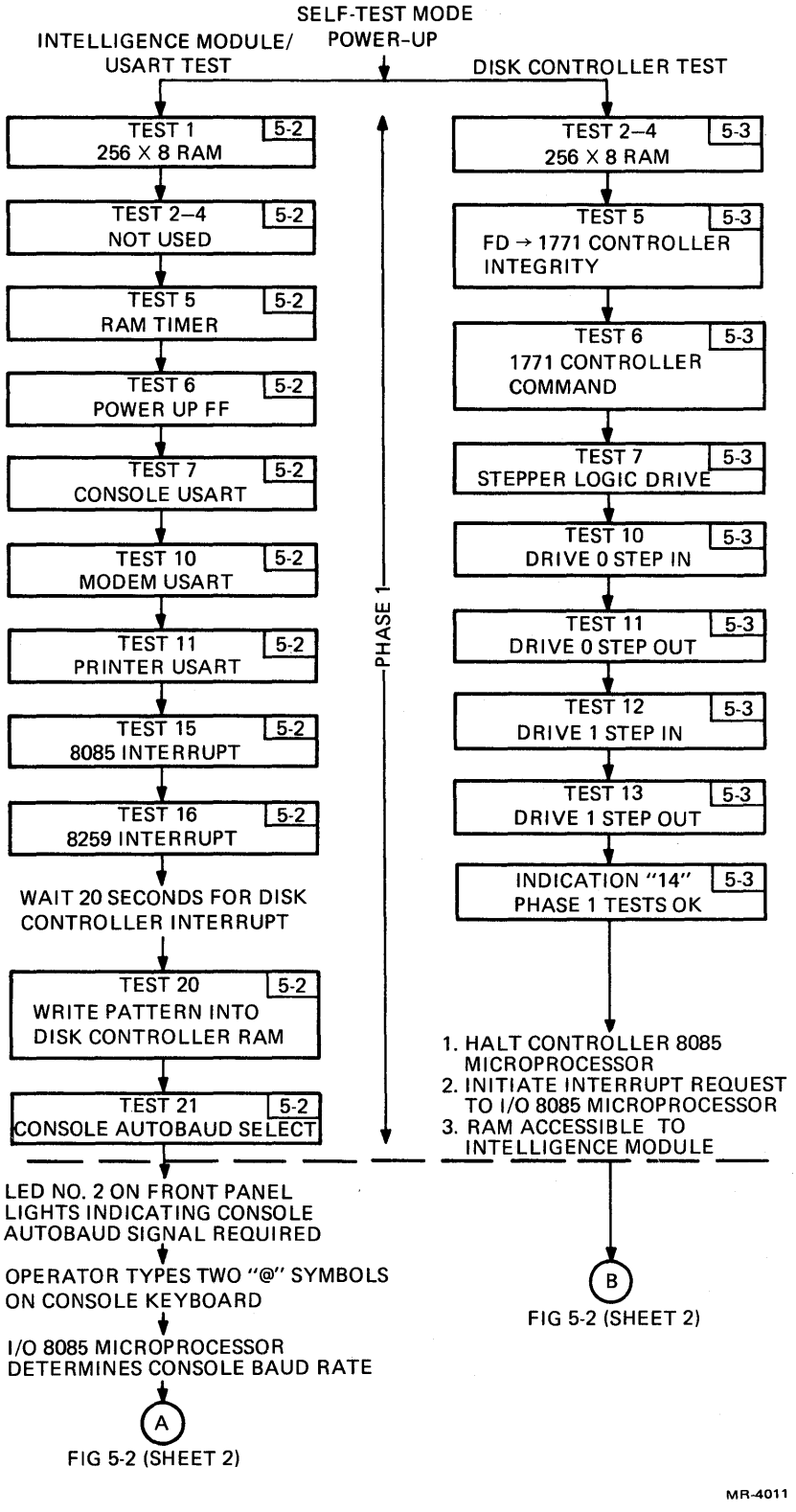


Figure 5-2 Self-Test Sequence Chart (Sheet 1 of 3)

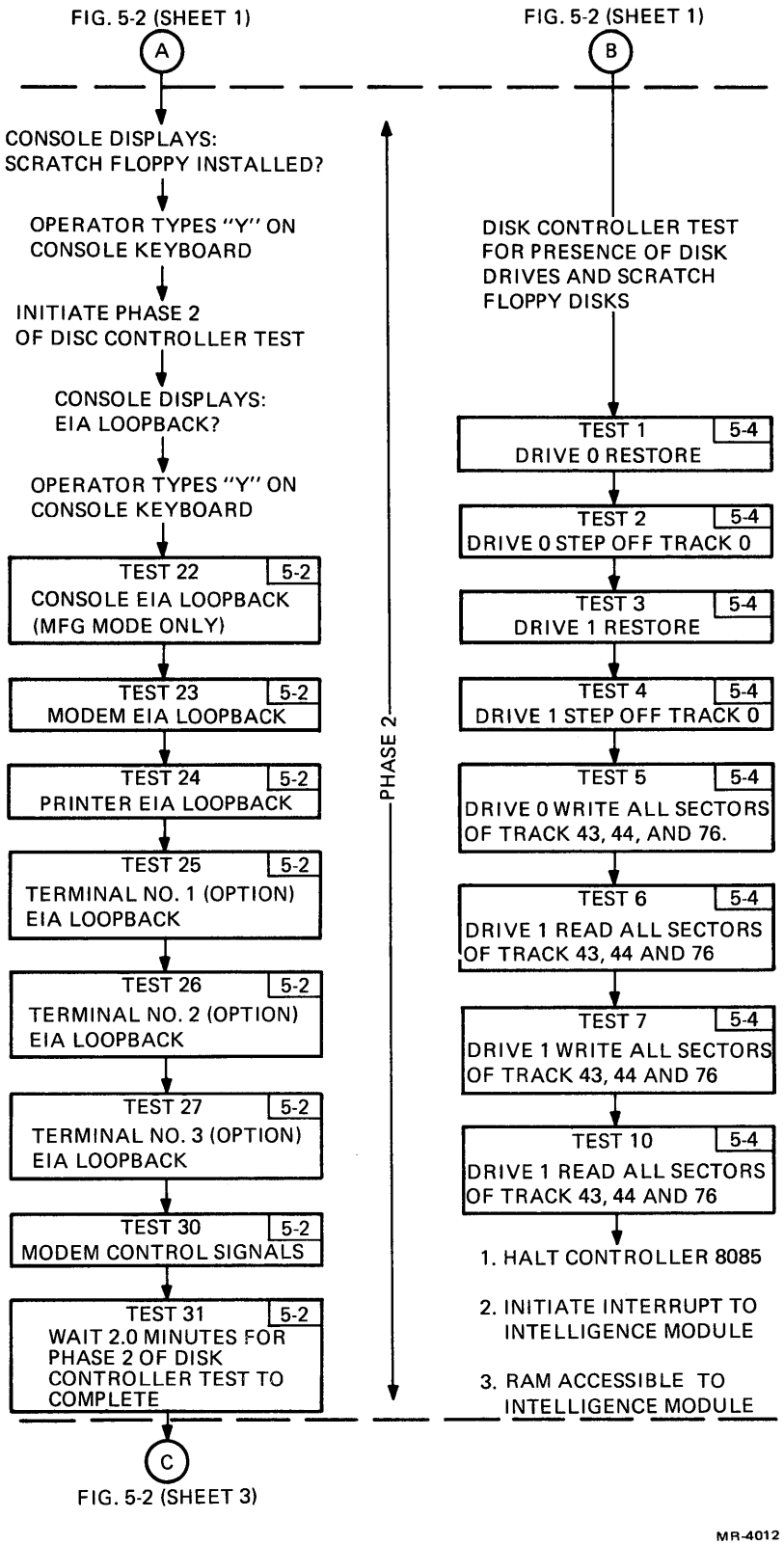


Figure 5-2 Self-Test Sequence Chart (Sheet 2 of 3)

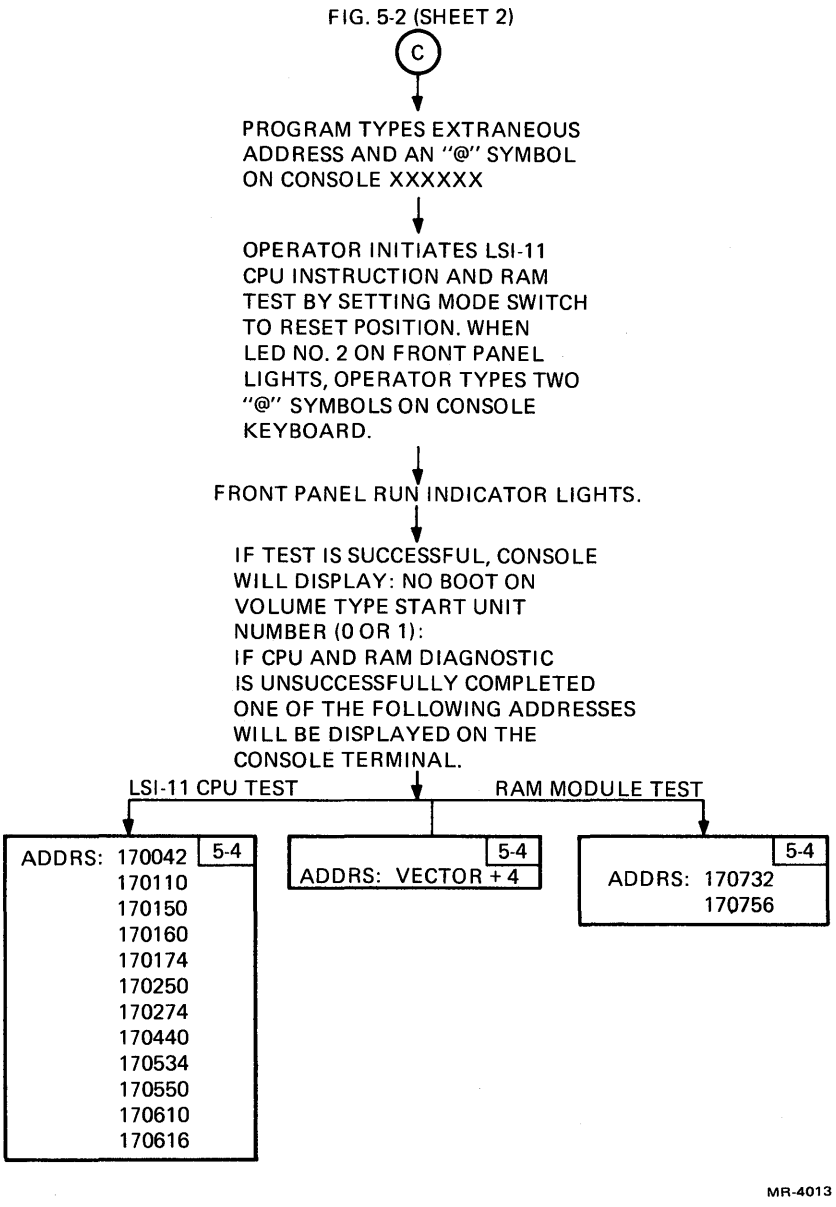


Figure 5-2 Self-Test Sequence Chart (Sheet 3 of 3)

Table 5-2 TIM Group Assembly Fault Indications

LED Indicators					Octal Code	Probable Cause	Correction	Test Description	Reference
5	4	3	2	1	Test				
				X	01	Intelligence module.	Replace module.	Verifies the integrity of the data written into and read from the 256, 8-bit locations of the 8155 IC on the Intelligence module.	Para. 5.3.7
					02–04			Not Used.	
		X		X	05	Intelligence module.	Replace module.	Verifies the operation of the timer in the 8155 IC on the Intelligence module.	Para. 5.3.7
		X	X		06	Intelligence module.	Replace module.	Verifies the operation of the power-up flip-flop on the Intelligence module.	Para. 5.3.7
		X	X	X	07	1. Intelligence module. 2. Peripheral module. 3. Module stacking connector P1 or P2.	Replace module or connector.	Verifies the performances of the console USART on the Peripheral module in the internal loopback mode at 19.2K baud. Controlled by the 8085 I/O microprocessor on the Intelligence module.	1. Para. 5.3.7 2. Para. 5.3.6 3. Para. 5.3.7
	X				10	1. Intelligence module. 2. Peripheral module. 3. Module stacking connector P1 or P2.	Replace module or connector.	Verifies the performance of the communications USART on the Peripheral module in the internal loopback mode at 19.2K baud. Controlled by the 8085 I/O microprocessor on the Intelligence module.	1. Para. 5.3.7 2. Para. 5.3.6 3. Para. 5.3.7

Table 5-2 TIM Group Assembly Fault Indications (Cont.)

LED Indicators					Octal Code	Probable Cause	Correction	Test Description	Reference
5	4	3	2	1	Test				
	X			X	11	1. Intelligence module. 2. Peripheral module. 3. Module stacking connector P1 or P2.	Replace module or connector.	Verifies the performance of the printer USART on the Peripheral module in the internal loopback mode at 19.2K baud. Controlled by the 8085 I/O microprocessor on the Intelligence module.	1. Para. 5.3.7 2. Para. 5.3.6 3. Para. 5.3.7
	X		X		12	1. Intelligence module. 2. Peripheral module. 3. Module stacking connector P1 or P2.	Replace module or connector.	Verifies the performance of the terminal No. 1 USART (optional) on the Peripheral module in the internal loopback mode at 19.2K baud. Controlled by the 8085 I/O microprocessor on the Intelligence module.	1. Para. 5.3.7 2. Para. 5.3.6 3. Para. 5.3.7
	X		X	X	13	1. Intelligence module. 2. Peripheral module. 3. Module stacking connector P1 or P2.	Replace module or connector.	Verifies the performance of the terminal No. 2 USART (optional) on the Peripheral module in the internal loopback mode at 19.2K baud.	1. Para. 5.3.7 2. Para. 5.3.6 3. Para. 5.3.7
	X	X			14	1. Intelligence module. 2. Peripheral module. 3. Module stacking connector P1 or P2.	Replace module or connector.	Verifies the performance of the terminal No. 3 USART (optional) on the Peripheral module in the internal loopback mode at 19.2K baud.	1. Para. 5.3.7 2. Para. 5.3.6 3. Para. 5.3.7

Table 5-2 TIM Group Assembly Fault Indications (Cont.)

LED Indicators					Octal Code	Probable Cause	Correction	Test Description	Reference
5	4	3	2	1	Test				
	X	X		X	15	1. Intelligence module. 2. Peripheral module. 3. Module stacking connector P1 or P2.	Replace module or connector.	Verifies the operation of the 8085 I/O microprocessor interrupt structure on the Intelligence module. Program interrupt requests are from the printer terminal USART on the Peripheral module and from the internal timer in the 8155 I/O port and RAM IC on the Intelligence module.	1. Para. 5.3.7 2. Para. 5.3.6 3. Para. 5.3.7
	X	X	X		16	1. Intelligence module. 2. Peripheral module. 3. Module stacking connector P1 or P2.	Replace module or connector.	Verifies the ability of the 8259 programmable interrupt IC to generate a program interrupt request to the 8085 I/O microprocessor on the Intelligence module.	1. Para. 5.3.7 2. Para. 5.3.6 3. Para. 5.3.7
	X	X	X	X	17	1. Disk Controller module. 2. Cable G1.	Replace a defective module or cable.	Verifies that an interrupt request from the Disk Controller module occurs at the completion of phase 1 of the disk drive diagnostic. The disk drive(s) should not be active (head searching). If active, refer to Table 5-3 for fault indications of Disk Controller module or disk drive.	1. Para. 5.3.10 2. Figure 5-22

Table 5-2 TIM Group Assembly Fault Indications (Cont.)

LED Indicators					Octal Code	Probable Cause	Correction	Test Description	Reference
5	4	3	2	1	Test				
X					20	1. Disk Controller module. 2. Cable G1.	Replace module or cable.	Verifies the integrity of data written into and read from the two 256 X 4 RAM ICs on the Disk Controller module. The data is written and read by the 8085 I/O microprocessor on the Intelligence module.	1. Para. 5.3.10 2. Figure 5-22
X				X	21	Requests autobauding.	Type two "@" symbols on the console keyboard if autobaud is desired.	Indicates the successful completion of all tests in phase 1. The PDT-11/150 is waiting to be autobauded. Front panel indicator "2" is lighted and Test 12 is indicated by the LEDs on the Disk Controller module (Table 5-3).	Para. 3.3.3; Figure 3-1
						1. Console terminal or terminal cable. 2. Cable G2. 3. Standard EIA module. 4. Intelligence module. 5. Module stacking connector P1 or P2.	Replace module, cable, or connector.	The two "@" symbols were typed and the front panel indicator "2" remains lighted. Test 12 remains displayed on the Disk Controller module. Front panel error "1" LED is not lighted. This test indicates the unsuccessful request for autobaud due to faulty console terminal, interconnecting cables, Standard EIA module or Intelligence module.	1. Para. 2.2.2 2. Figure 5-20 3. Para. 5.3.8 4. Para. 5.3.7 5. Para. 5.3.7

Table 5-2 TIM Group Assembly Fault Indications (Cont.)

LED Indicators					Octal Code	Probable Cause	Correction	Test Description	Reference
5	4	3	2	1	Test				
X			X		22			Test 22 can only be performed when the manufacturing mode is selected by the ON position of switch S1-5 on the Peripheral module (Table 3-4) and the manufacturing loopback connector is installed on the rear panel. This test verifies that data can be transmitted and received through the 25-pin EIA console terminal connector J1 on the rear panel.	
X			X	X	23	A Y (yes) was typed in answer to the EIA LOOPBACK TEST? question displayed on the console, and the loopback connector was not installed. *or*	Install loopback connector.	Verifies that data can be transmitted and received through the modem connector J2 on the rear panel.	
						1. Standard EIA module. 2. Cable G2. 3. Peripheral module. 4. Loopback connector module.	Replace module or cable.	Verifies that data can be transmitted and received through the modem connector on the rear panel. The following conditions are required: 1. The loopback connector is properly installed;	1. Para. 5.3.8 2. Figure 5-20 3. Para. 5.3.6 4. Para. 3.3.2

Table 5-2 TIM Group Assembly Fault Indications (Cont.)

LED Indicators					Octal Code	Probable Cause	Correction	Test Description	Reference
5	4	3	2	1	Test				
								2. The manufacturing mode switch S1-5 is in the OFF position (Table 3-4); 3. A Y (yes) was typed in answer to the EIA LOOPBACK TEST? question displayed on the console.	
X		X			24	1. Standard EIA module. 2. Cable G2. 3. Peripheral module. 4. Loopback connector module.	Replace module or cable.	Similar to Test 23 except for the printer connector J3 on the rear panel.	1. Para. 5.3.8 2. Figure 5-20 3. Para. 5.3.6 4. Para. 3.3.2
X		X		X	25	1. Cluster EIA module. 2. Cable G3. 3. Peripheral module. 4. Loopback connector module.	Replace module or cable.	Similar to Test 23 except for the Terminal 1 connector J1 of the Cluster option (DFT11-AB) on the rear panel.	1. Para. 5.3.9 2. Figure 5-20 3. Para. 5.3.6 4. Para. 3.3.2
X		X	X		26	1. Cluster EIA module. 2. Cable G3. 3. Peripheral module. 4. Loopback connector module.	Replace module or cable.	Similar to Test 23 except for the Terminal 2 connector J2 of the Cluster option (DFT11-AB) on the rear panel.	1. Para. 5.3.9 2. Figure 5-20 3. Para. 5.3.6 4. Para. 3.3.2

Table 5-2 TIM Group Assembly Fault Indications (Cont.)

LED Indicators					Octal Code	Probable Cause	Correction	Test Description	Reference
5	4	3	2	1	Test				
X		X	X	X	27	1. Cluster EIA module. 2. Cable G2. 3. Peripheral module. 4. Loopback connector module.	Replace module or cable.	Similar to Test 23 except for the Terminal 3 connector J3 of the Cluster option (DFT11-AB) on the rear panel.	1. Para. 5.3.9 2. Figure 5-20 3. Para. 5.3.6 4. Para. 3.3.2
X	X				30	1. Standard EIA module. 2. Cable G2. 3. Peripheral module. 4. Intelligence module.	Replace module or cable.	Verifies that the control signals from the modem are sensed at the 8155 I/O IC on the Intelligence module. Refer to Test 23 for conditions required.	1. Para. 5.3.8 2. Figure 5-20 3. Para. 5.3.6 4. Para. 5.3.7
X	X			X	31			Verifies that the second pass of the disk drive diagnostic was successfully completed. If an error is indicated, refer to Table 5-4 for the possible fault indicators on the Disk Controller module test phase 2.	

Table 5-3 Disk Controller Module Fault Indications (Phase 1)

LED Indicators				Octal Code	Probable Cause	Correction	Test Description	Reference
4	3	2	1	Test				
			X	01			Not Used.	
		X		02	Disk Controller module.	Replace module.	Verifies the integrity of the data written into and read from the four MSBs of the RAM IC on the Disk Controller module.	Para. 5.3.10
		X	X	03	Disk Controller module.	Replace module.	Same as Test 02 for the four LSBs of the RAM IC.	Para. 5.3.10
	X			04	Disk Controller module.	Replace module.	Continuation of Tests 2 and 3 of the RAM IC.	Para. 5.3.10
	X		X	05	Disk Controller module.	Replace module.	Verifies the integrity of the registers in the FD1771 disk controller IC on the Disk Controller module.	Para. 5.3.10
	X	X		06	Disk Controller module.	Replace module.	Verifies the ability of the FD1771 disk controller IC on the Disk Controller module to process commands.	Para. 5.3.10
	X	X	X	07	Disk Controller module.	Replace module.	Verifies that the proper control counters for the stepper motors are selected for disk drives 0 and 1, and that the counters change state with a step command.	Para. 5.3.10
X				10	Disk Controller module.	Replace module.	Verifies that the step logic for disk drive 0 performs a step-in function.	Para. 5.3.10

Table 5-3 Disk Controller Module Fault Indications (Phase 1) (Cont.)

LED Indicators				Octal Code	Probable Cause	Correction	Test Description	Reference
4	3	2	1	Test				
X			X	11	Disk Controller module.	Replace module.	Verifies that the step logic for disk drive 0 performs a step-out function.	Para. 5.3.10
X		X		12	Disk Controller module.	Replace module.	Same as step 10 except for disk drive 1.	Para. 5.3.10
X		X	X	13	Disk Controller module.	Replace module.	Same as step 11 except for disk drive 1.	Para. 5.3.10

Table 5-4 Disk Controller Module Fault Indications (Phase 2)

LED Indicators				Octal Code	Probable Cause	Correction	Test Description	Reference
4	3	2	1	Test				
			X	01	1. Disk drive 0 assembly. 2. Disk controller module.	Replace defective drive 0 or module.	Verifies the position of the disk drive 0 head after a restore command is issued.	1. Para. 5.3.12 2. Para. 5.3.10
		X		02	Same as Test 01.	Same as Test 01.	Verifies the position of the disk drive 0 head after a step off track 0 command is issued.	Same as Test 01
		X	X	03	1. Disk drive 1 assembly. 2. Disk Controller module.	Replace defective drive 1 or module.	Verifies the position of the disk drive 1 head after a restore command is issued. Test 03 is not executed if drive 1 is not included.	1. Para. 5.3.13 2. Para. 5.3.10

Table 5-4 Disk Controller Module Fault Indications (Phase 2) (Cont.)

LED Indications				Octal Code	Probable Cause	Correction	Test Description	Reference
4	3	2	1	Test				
	X			04	Same as Test 03.	Same as Test 03.	Verifies the position of the disk drive 1 head after a step off track 0 command is issued. Test 04 is not executed if drive 1 is not present.	Same as Test 03.
	X		X	05	1. Disk drive 0 assembly. 2. Disk Controller module. 3. Scratch disk not installed.	Replace defective drive 0 or module. Install scratch disk.	Writes on all sectors of tracks 44 and 76 on the scratch disk. An error will be indicated if the header field that precedes the sector is not identified.	1. Para. 5.3.12 2. Para. 5.3.10 3. Para. 3.2
	X	X		06	Same as Test 05.	Same as Test 05.	Reads all sectors of tracks 43, 44, and 76 on the scratch disk. An error will be indicated if the header field is not identified, if the data written and read is different, or if a CRC error is detected.	Same as Test 05.
	X	X	X	07	1. Disk drive 1 assembly. 2. Disk Controller module. 3. Disk not installed. 4. Defective disk.	Repair or replace defective drive, cable, or module. Install scratch disk. Replace scratch disk.	Writes on all sectors of tracks 43, 44, and 76 on the scratch disk. An error will be indicated if the header field that precedes each sector is not identified.	1. Para. 5.3.13 2. Para. 5.3.10 3. Para. 3.2
X				10	Same as Test 07.	Same as Test 07.	Reads all sectors of tracks 43, 44, and 76 on the scratch disk. An error will be indicated.	Same as Test 07

Table 5-5 LSI-11 Microprocessor and RAM Module Fault Indications

Indications	Probable Cause	Correction	Test Description	Reference
The following addresses are displayed on the console terminal.				
170046			Test 1; tests single word operand instructions with destination mode zero.	
170110			Test 2; tests single byte operand instructions with destination mode zero.	
170150	Intelligence module (LSI-11)	Replace module.	Test 3; tests double word operand instructions with destination mode zero, and all source modes.	Para. 5.3.7
170160			Test 4; tests the jump instruction, destination modes 1, 3, and 6.	
170174			Test 4; tests the jump instruction, destination modes 1, 3, and 6.	
170250			Test 5; tests TST and TSTB instructions, destination modes 1, 2, 4 and 6.	
170274			Test 6; tests double byte operand instructions with destination mode zero, and source modes 1, 2 and 4.	

Table 5-5 LSI-11 Microprocessor and RAM Module Fault Indications (Cont.)

Indications	Probable Cause	Correction	Test Description	Reference
170440			Test 7; tests word instructions with destination modes not zero. Tests the MOV instruction with destination modes 1, 2, 3 and 4. All destination modes are checked with a variety of instructions.	
170534	1. Intelligence module. 2. RAM module. 3. Stacking connector P1 or P2.	Replace module or connector.	Test 8; tests byte instructions with destination modes not zero.	1. Para. 5.3.7 2. Para. 5.3.5 3. Para. 5.3.7
170550			Test 9; tests the JSR instruction. This error is an "RTS R3" failing to return.	
170610				
170616				
If any of the preceding addresses are displayed, initiate the RAM memory test by typing 170616G on the console terminal.			If a halt occurs during the RAM memory test at either of the locations that follow, a failure of the RAM module is indicated.	

Table 5-5 LSI-11 Microprocessor and RAM Module Fault Indications (Cont.)

Indications	Probable Cause	Correction	Test Description	Reference
170732	RAM module.	Replace module.	Memory test; reads, writes and verifies memory. This is a memory address error. All memory is written with its address and then read back and verified. Expected data is in R3, bad data is pointed to by the address in R2. Type **P** to continue memory test.	Para. 5.3.5
170756			Memory test; reads, writes, and verifies memory. This is a data storage error. All memory is filled with zeros, the A-1 is sequenced through memory and checked. Expected data is in R3, bad data is pointed to by the address in R2. Type **P** to continue memory test.	Para. 5.3.5
Vector address 0–500 + 4	Intelligence module.	Replace module.	During the diagnostic, vectors from 0–500 are filled with .+2 HALT A spurious interrupt or trap can cause a halt with PC = VECTOR + 4 displayed.	Para. 5.3.7

5.1.3 Loading the System Exerciser Program

To continue the diagnostic testing of the unit, perform the following procedures immediately after the successful completion of the self-test.

NOTE

Before performing the system exerciser program, switch S1-2 (see Table 3-3) must be set to the OFF position to enable the line time clock.

1. Insert the PDT-11/150 system exerciser disk (CVKDAC) into disk drive 0 or 1.

2. On the console keyboard, type the number of the disk drive where the disk is located (0 or 1).

3. The program will be entered and the console will display the identification of the disk program as follows.

   CVKDAC PDT-11/150 SYSTEM EXERCISER

   SWR = 000000 NEW =

4. Select from Table 5-6 the switch register SWR functions desired and add the content values for each function.

Table 5-6 Switch Register (SWR) Functions

Content	Function
100000	Halt on error
20000	Inhibit error typeouts
10000	Enable performance reports
2000	Bell on error

5. Enter the sum of the content values on the console keyboard and press the RETURN key. If the current value (000000) is desired, press only the RETURN key.

NOTE

The content value of 10000 must be entered to permit a display of the status of each test being performed.

Example:

To select performance reports and bell on error, add the following values.

Enable performance reports	10000	
Bell on error	2000	
	012000	Content sum

6. The console terminal will then display a message similar to the following.

   DEVM = 000017 NEW =

7. The device map (DEVM) options allow the selection of the system exerciser tests to be compatible with user requirements and system configuration. Select the tests desired from Table 5-7 by adding the content values.

   a. A content value of DEVM = 000000 will exercise all configurations in external loopback mode.

   b. Any content sum having the two least significant octal digits less than 17 requires installation of the loopback connector assembly on the rear panel (see Paragraph 3.3.2).

      DEVM = XXXX16 (or less)

   c. The console connector will not be tested.

      Example:

      A single disk drive unit has devices attached to all standard EIA connectors and one terminal attached to the cluster terminal no. 1 connector. Perform all tests on external loopback.

Delete	Cluster terminal no. 3 test	40000
Delete	Cluster terminal no. 2 test	20000
Delete	Disk drive 1 test	1000
	Content sum	061000

8. Remove all device cables (except the console cable) from the rear panel and install the loopback connector.

9. Enter the sum of the content values on the console terminal keyboard and press the RETURN key. If no value is entered and the RETURN key is pressed, the group 2 options (internal loopback) will be selected by the current value of DEVM = 000017.

10. The console will display a message similar to the following.

```
30K MEMORY PRESENT
PRINTER NOT PRESENT

INSERT SCRATCH DISKS, TYPE 'P' FOR NORMAL TESTING
'240G' FOR NORMAL RESTARTS
'250G' TO COPY SYS EXERCISER DISK
'260G' FOR COMPATABILITY PASS 1: WRITE
'270G' FOR COMPATABILITY PASS 2: READ
003706
XXXXXX
@
```

11. Remove the system exerciser disk from disk drive 0 and insert a scratch disk into the drive(s) to be tested.

Table 5-7 Device Map (DEVM) Options

Group	Contents	Function
1	000000	Selects the following tests: External loopback for all three cluster terminals External loopback for standard terminals (modem and printer) Asynchronous and synchronous testing of the modem Disk drive 0 and 1 Internal clock
	100000	Delete printer test
	40000	Delete cluster terminal no. 3 test
	20000	Delete cluster terminal no. 2 test
	10000	Delete cluster terminal no. 1 test
	4000	Delete ASYNC modem test
	2000	Delete SYNC modem test
	1000	Delete disk drive 1 test
	400	Delete drive 0 test
	200	Delete clock test
	100	Cluster option not present
2	10	Internal loopback for modem USART
	4	Internal loopback for cluster terminal no. 1 USART
	2	Internal loopback for cluster terminal no. 2 USART
	1	Internal loopback for cluster terminal no. 3 USART

12. To start the normal program, type **P** on the console terminal keyboard. The exerciser will begin testing and the results of each test will be displayed on the console terminal. At the end of each pass, the console will display a message similar to the following.

```
END PASS #      1          TOTAL ERRORS:              0
                           TOTAL SOFT ERRORS:         0

                           TOTAL ERRORS THIS PASS:    0
                           SOFT ERRORS THIS PASS:     0
```

13. Allow approximately 1/2 hour for the entire test to be completed. If an error is encountered during the test and a halt on error function has been selected in step 4, type **240G** to restart the program after the last error.

NOTE
Some terminals may require that the SHIFT key be pressed while typing G.

14. To continue the test from where the error was detected, type **P** on the console keyboard.

15. To alter the content of the SWR while the exerciser program is operating, press CTRL key while typing **G**.

16. The program will halt and the console will display the current SWR value.

```
SWR = XXXXXX NEW =
(XXXXXX = previous value selected)
```

17. Enter the new SWR content value as described in step 5 or press the RETURN key to retain the current content value. The program will resume when RETURN is pressed.

18. To alter the content of the DEVM while the exerciser program is operating, press CTRL key while typing **G**.

19. The program will halt and the console will display the current SWR value.

```
SWR = 012000 NEW =
(XXXXXX = previous value selected)
```

20. To continue, press CTRL key while typing **C**.

21. The console will display the current DEVM value.

```
DEVM = XXXXXX NEW =
(XXXXXX = previous value selected)
```

22. Enter the new DEVM content value as described in step 9. When the RETURN key is pressed the program will resume.

5.1.4 Exerciser Compatibility Test

The system exerciser program includes a test to verify that data written on a disk by one disk drive can be read by another disk drive. In a dual disk drive unit the disks can be exchanged between drives. In a single drive unit, disks may be exchanged between units.

1. The compatibility test is selected at step 10 of the system exerciser test (see Paragraph 5.1.3) by typing **260G**.

   NOTE
   Some terminals may require that the SHIFT key be pressed while typing G.

   Data will be written on all tracks of disk drive 0 and 1 if both disk drives are selected by the DEVM (step 9 of Paragraph 5.1.3).

2. At the end of pass 1 the console will print the following message. Allow approximately 1/2 hour for the entire pass to be completed.

   ```
   END PASS #      1          TOTAL ERRORS:              0
                              TOTAL SOFT ERRORS:         0

                              TOTAL ERRORS THIS PASS:    0
                              SOFT ERRORS THIS PASS:     0

   COMPATABILITY PASS 1 (WRITE) DONE
   DO 'P' FOR PASS 2 (READ)
   010236
   ```

3. If the disks are exchanged between drive 0 and 1 of the same PDT-11/150 unit, type **P** on the console to initiate pass 2.

4. The console will display a message similar to the following.

   ```
   END PASS #      2          TOTAL ERRORS:              0
                              TOTAL SOFT ERRORS:         0

                              TOTAL ERRORS THIS PASS:    0
                              SOFT ERRORS THIS PASS:     0
   ```

5. If the disks are exchanged between drives in different PDT-11/150 units, each unit must have completed the self-test and system exerciser programs to step 10 of Paragraph 5.1.3. Type **240G** on the console of the unit where the disk will be tested.

6. The console will display a message similar to the message in step 4.

5.1.5 Copying the System Exerciser Disk

The PDT-11/150 system exerciser disk program can be duplicated on a scratch disk by performing the following procedures.

1. The copy utility is selected at step 10 of Paragraph 5.1.3 by typing **250G**.

2. The console will display the message

   COPY DX0 TO DX1
   INSERT SCRATCH FLOPPY IN DX1. TYPE "P" TO PROCEED

3. Insert the scratch disk into disk drive 1 (DX1).

4. Type **P** on the console keyboard.

   NOTE
   Allow approximately 1.5 minutes for transfer.

5. The console will display the message

   DONE . . . TYPE "P" TO DO AGAIN OR 240G FOR NORMAL TESTING

6. To reproduce another system exerciser disk, remove the disk in disk drive 1 (DX1) and replace it with another scratch disk.

7. Type **P** on the console keyboard.

8. To return to the system exerciser program, type **240G** on the console keyboard after receiving the message in step 5.

5.1.6 Loading a System Program

A program disk can be initially loaded into the PDT-11/150 by the following procedures.

1. Check to ensure that no disks are installed in the disk drive(s).

2. Set the mode switch on the rear panel to the NORMAL position (center).

3. Apply power to the console device.

4. Set the power switch on the rear panel to the ON (1) position.

   NOTE
   All indicators on the front panel, except the RUN indicator, will light momentarily when the ac power is applied. This confirms that those indicators are operative.

5. The POWER indicator will remain lighted and the (2) indicator will light again.

6. Insert the program disk into disk drive 0. In a dual disk unit, disk drive 0 is located above disk drive 1.

7. If the application program requires data storage on disk drive 1, insert a preformatted scratch disk into disk drive 1 of the dual drive unit.

8. Press the @ symbol twice on the console device.

NOTE
Some consoles may require that the SHIFT key be pressed while typing the @ symbols.

9. The console will display the program title and contents for user selection.

5.1.7 Changing a System Program

If the PDT-11/150 is presently operating and the program disk must be changed for some reason, perform the following procedures.

1. Remove the disk in disk drive 0 and insert the program disk to be loaded.

2. Set the mode switch to the RESET position and release (momentarily) to NORMAL position.

3. When the (2) indicator on the front panel lights, press the @ symbol key on the console keyboard twice.

NOTE
Some consoles may require that the SHIFT key be pressed while typing the @ symbols.

4. The console will display the program title and contents for user selection.

5.2 POWER DISTRIBUTION

This section includes the procedures for checking the ac power supplied to the unit and the dc power distributed internally to the modules and disk drive assemblies. Before removing or replacing a module or assembly indicated to be the cause of a test failure, check the ac and dc voltages to ensure that the required voltages exist and are of the proper value.

5.2.1 Internal Cable and Connector Locations

Figure 5-3 shows the locations of the cables and connectors within the PDT-11/150. The cable assemblies attached to the rear panel are included with the 60 Hz units. Figure 5-4 shows the difference in the cable wiring for the 50 Hz units. All 50 Hz units include the T1 autotransformer mounted on the power supply slide plate.

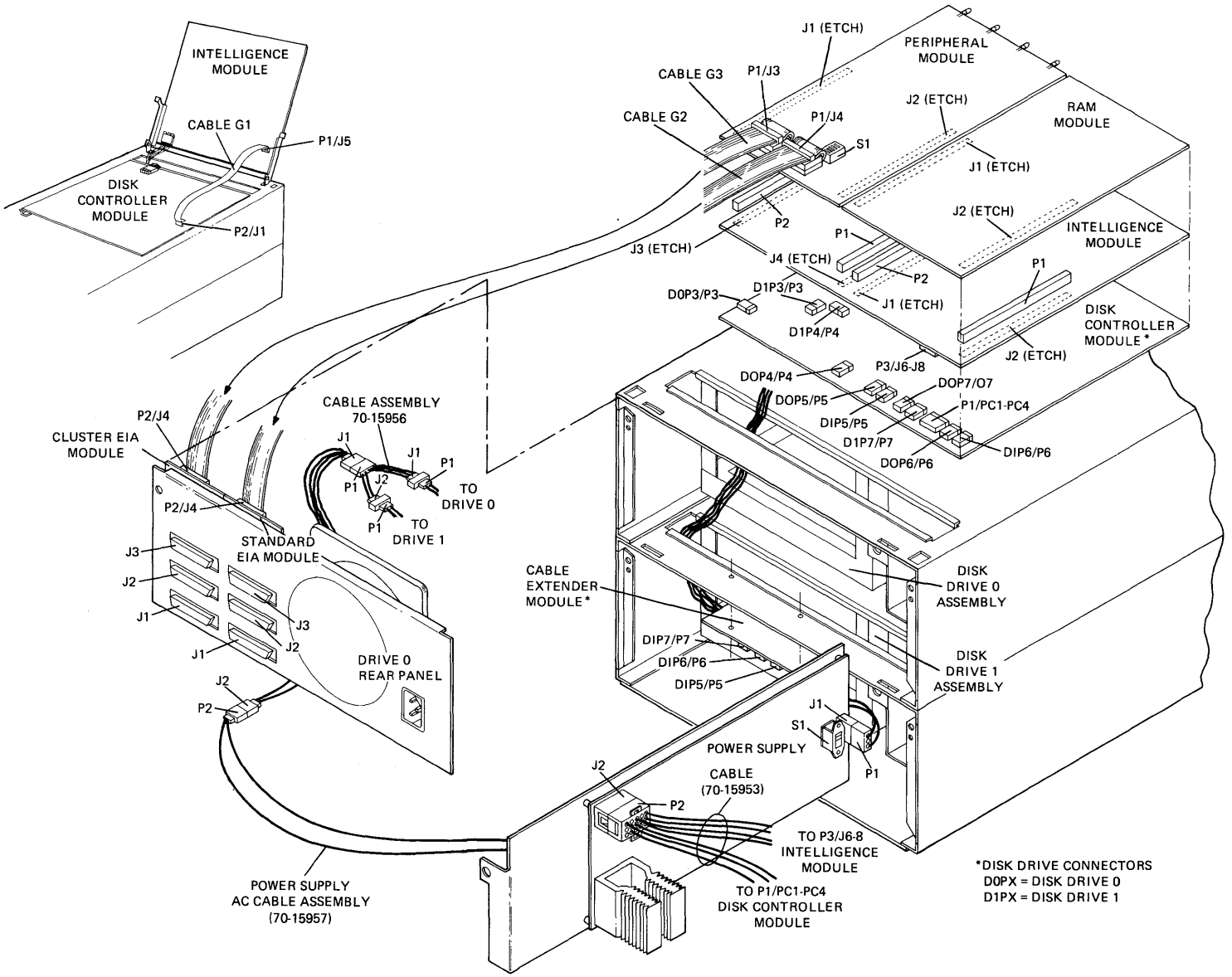


Figure 5-3 PDT-11/150 Internal Cables and Connectors

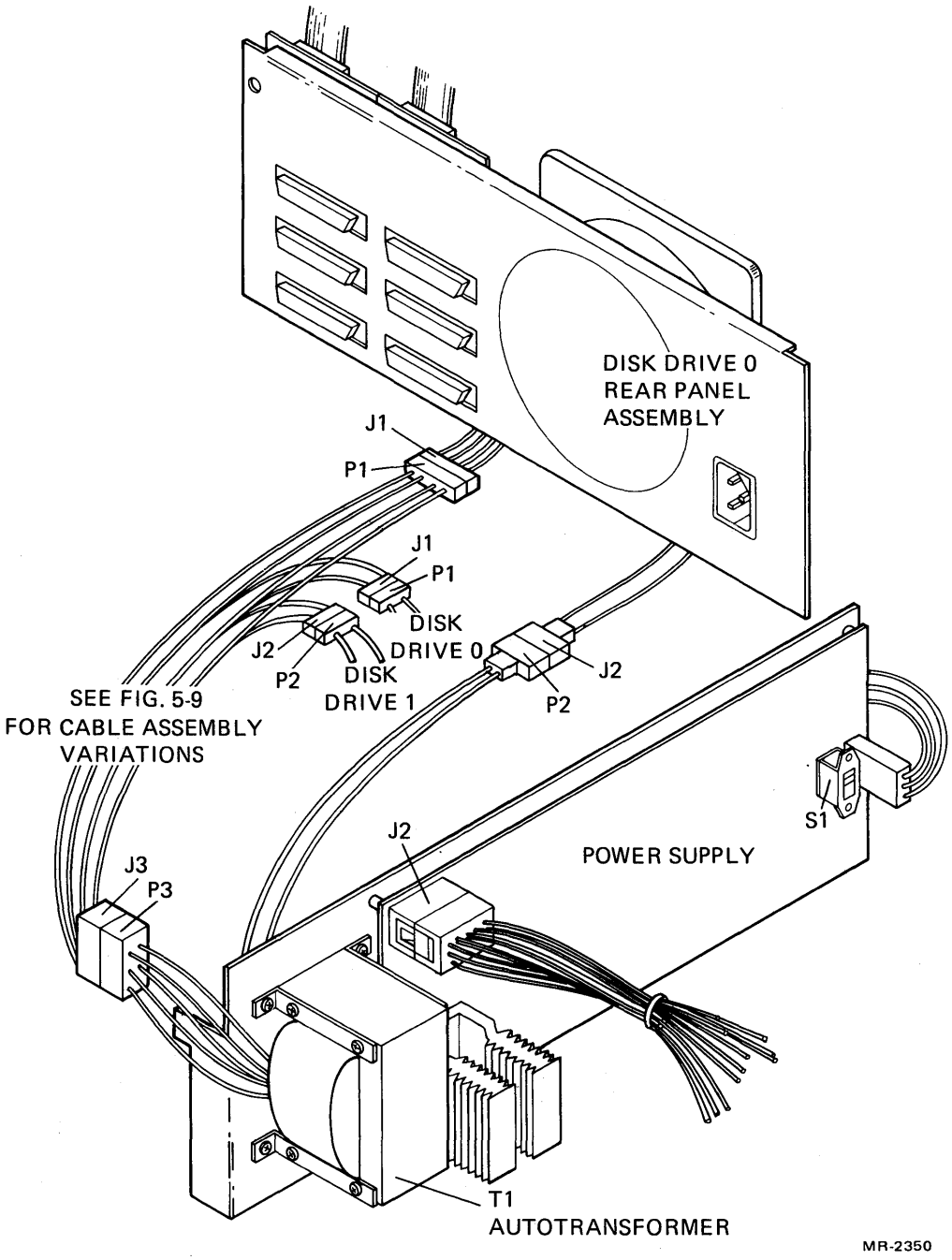


Figure 5-4 Internal ac Cables and Connectors, 50 Hz Units

5.2.2 Initial ac Power Checks

To ensure that the ac power is applied to the unit, perform the following.

1. Check to ensure the ac power cord plugs are properly installed in the ac power outlet on the rear panel of the disk drive 0 enclosure. (See Figure 2-3.)

2. Set the ac power ON(1)/OFF(0) switch on the rear panel to the up (ON) position.

3. Check to ensure that the fan on the rear panel of the unit is operating.

4. If the fan is inoperative, test the main ac power at the power outlet where the unit power cord is connected.

5. If ac power is not present at the outlet, check the power distribution outlet in the area.

6. If ac power is present at the outlet, disconnect the power cord from the rear panel of the unit and remove the rear panel assembly using the procedures described in Paragraph 5.3.2.2.

7. Check the continuity of the wiring on the rear panel.

Figure 5-5 (Sheets 1 and 2) is the ac and dc power distribution diagram for the 115V, 60 Hz dual disk drive units. Figure 5-6 shows the rear panel connector pin locations and Figure 5-7 shows the connector pin locations for the cable assembly (no. 7015957) which distributes the ac from the rear panel assembly to the power supply. Figure 5-8 shows the ac power distribution from the rear panel assembly for the 50 Hz units. Four different cable assemblies can be attached to the T1 autotransformer, depending on the input ac voltage supplied. Figure 5-9 (Sheets 1 and 2) identifies the cables for the voltage ranges and shows the pin locations of the connector cables. Figure 5-10 shows the connector pin location of the ac cable which is attached to the drive vector E1 of the disk drive assemblies.

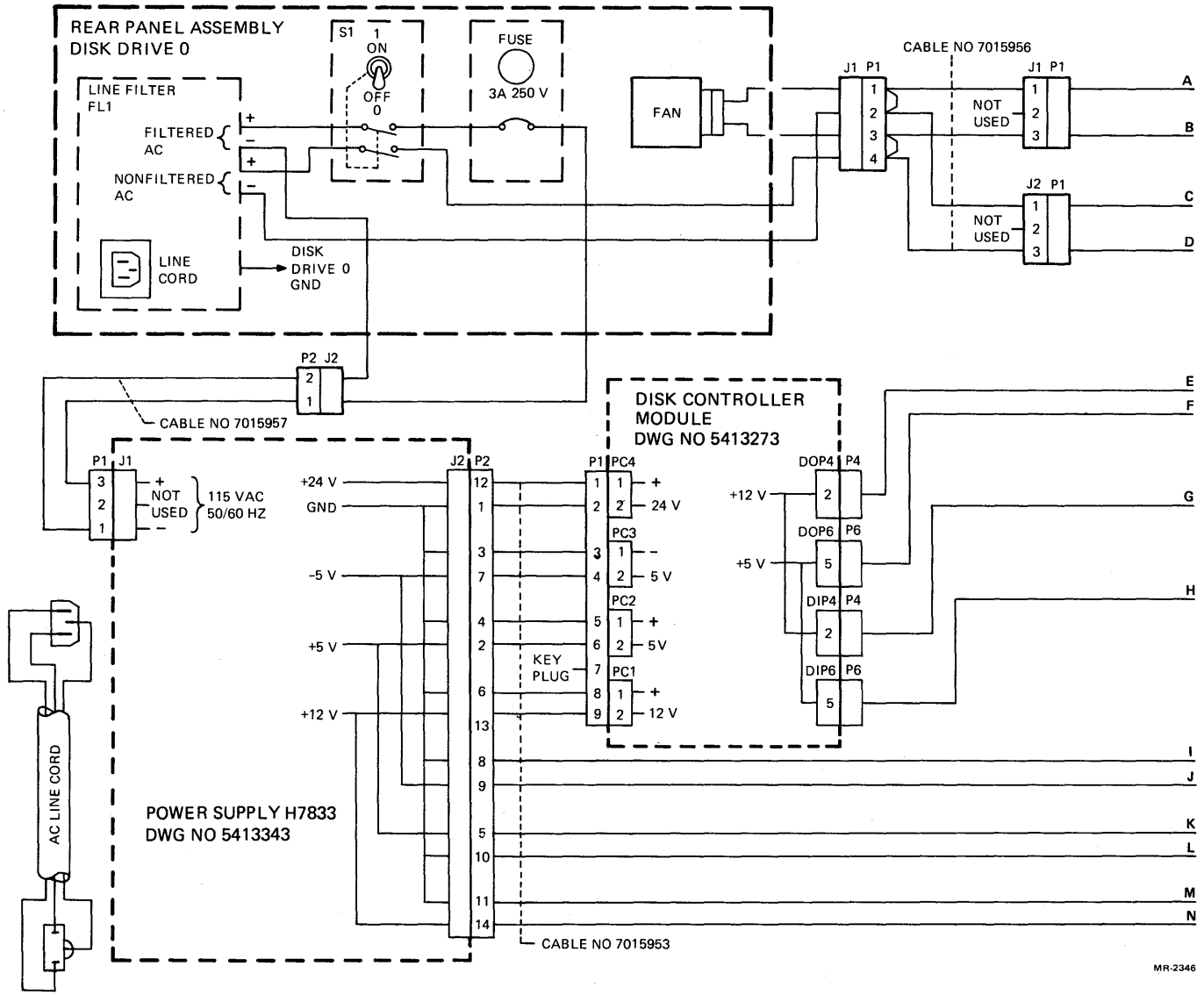


Figure 5-5 AC/DC Power Distribution, 60 Hz Units
(Sheet 1 of 2)

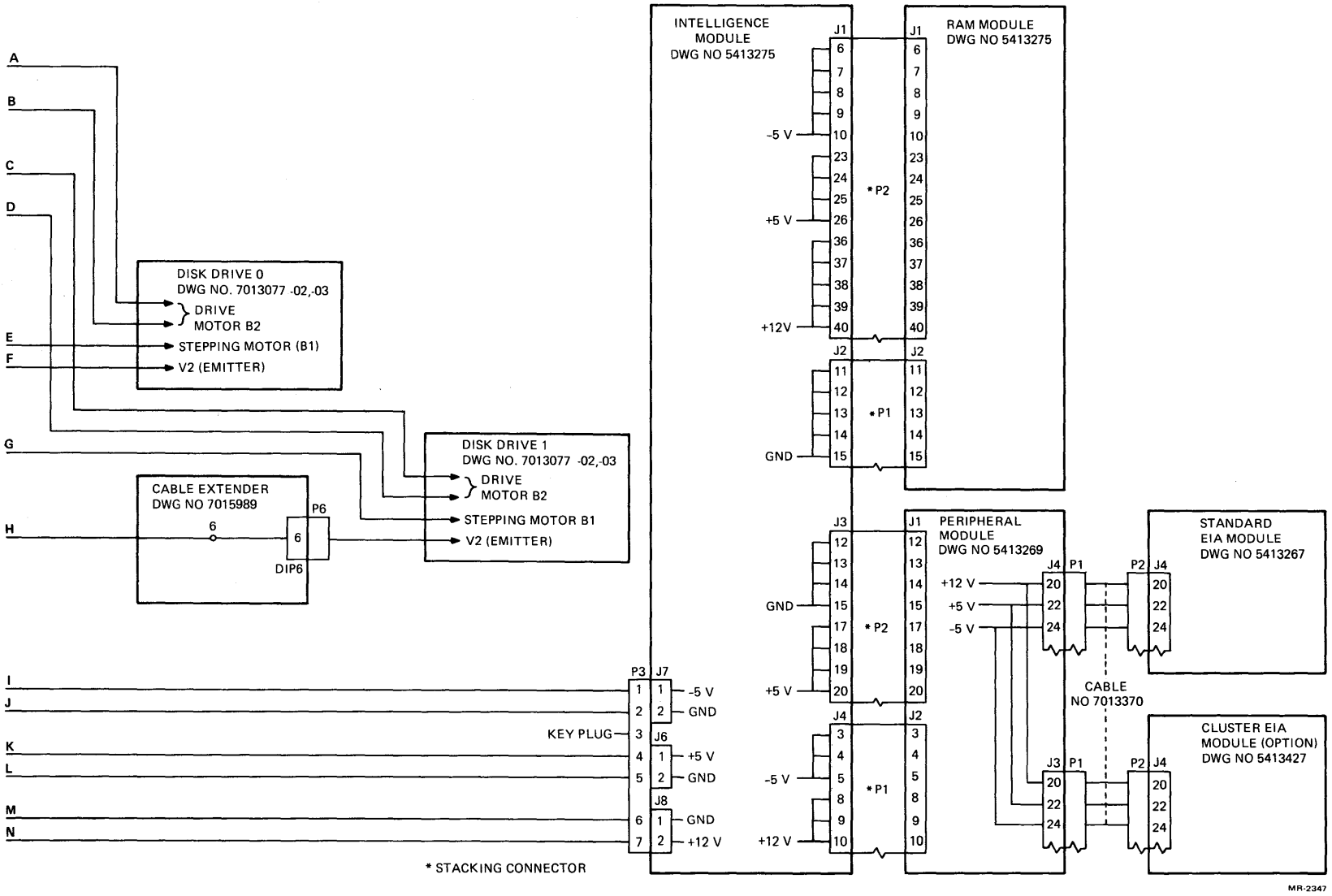


Figure 5-5 AC/DC Power Distribution, 60 Hz Units
(Sheet 2 of 2)

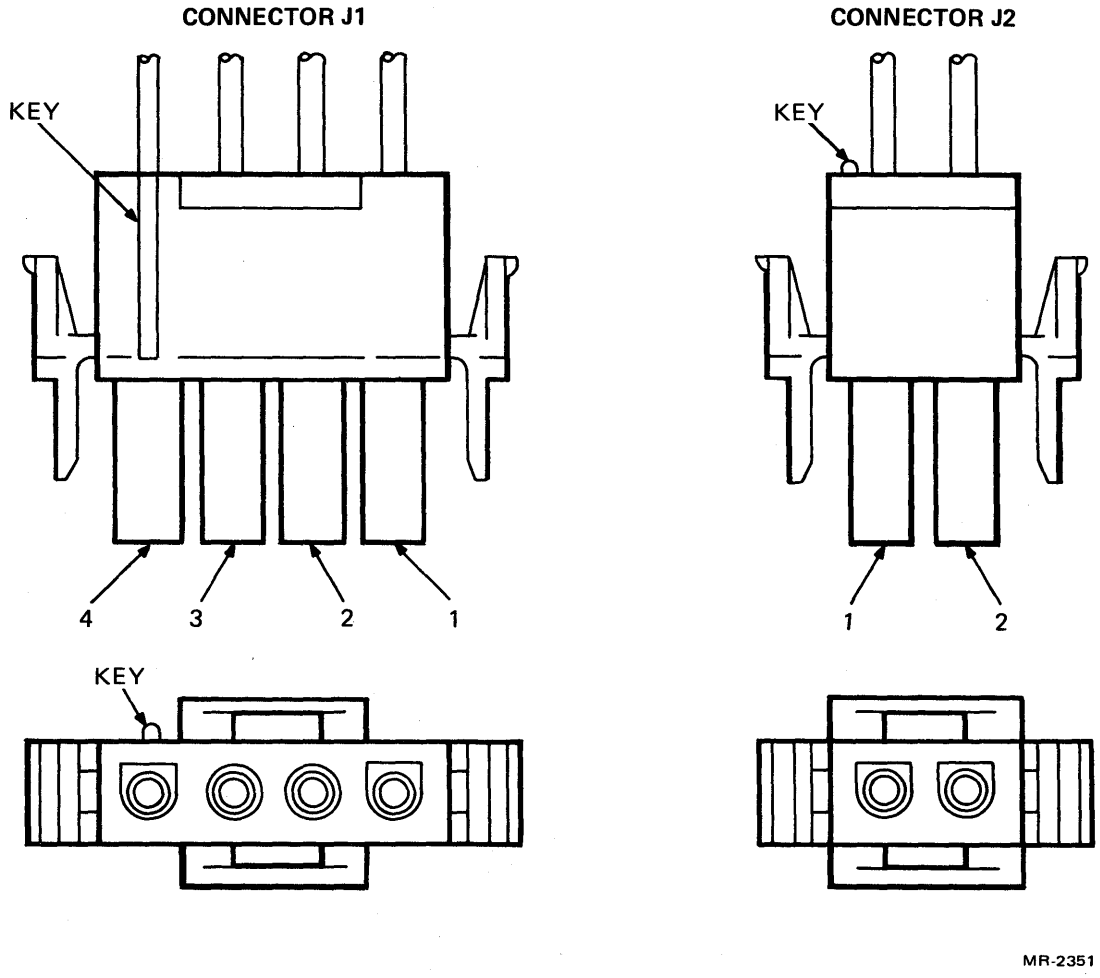


Figure 5-6 Rear Panel Assembly, ac Cable Pin Locations

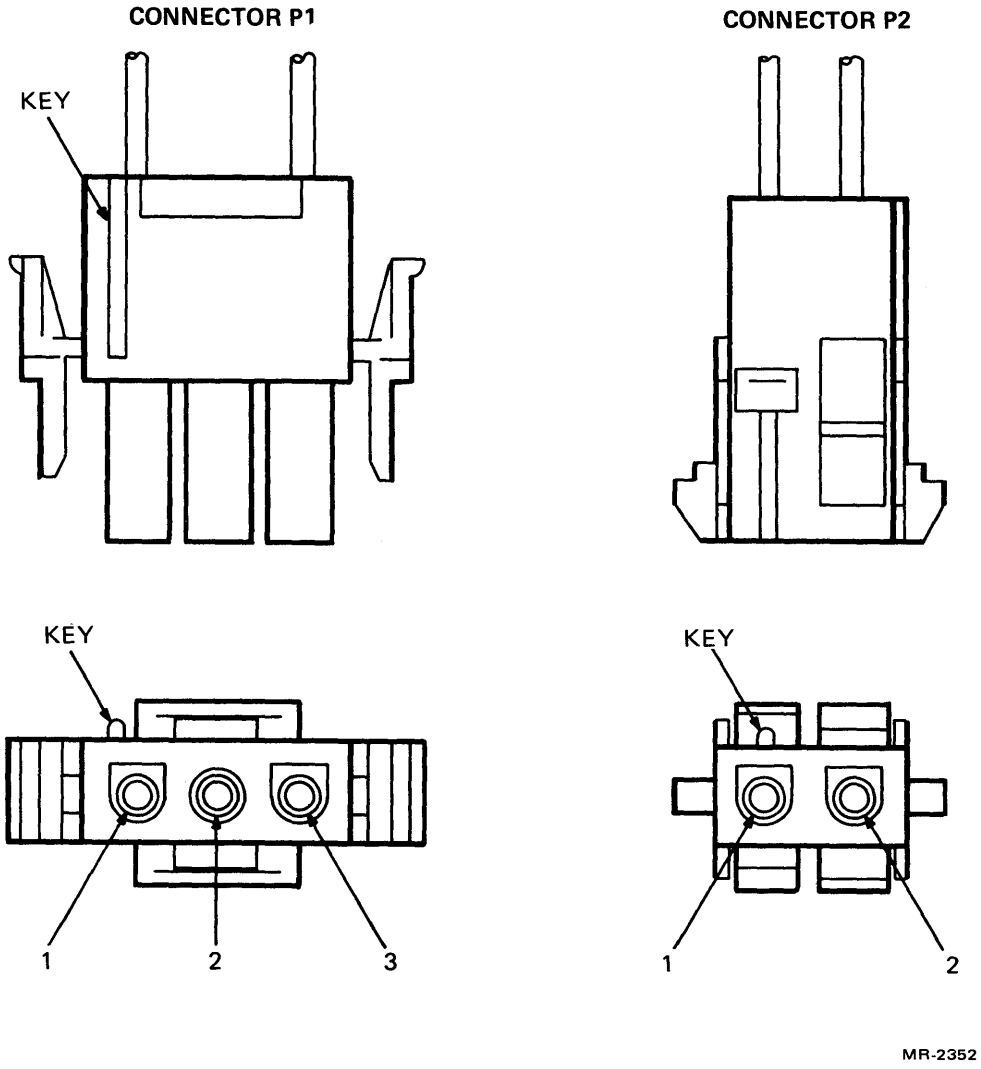


Figure 5-7 Power Supply ac Cable, Connector Pin Locations

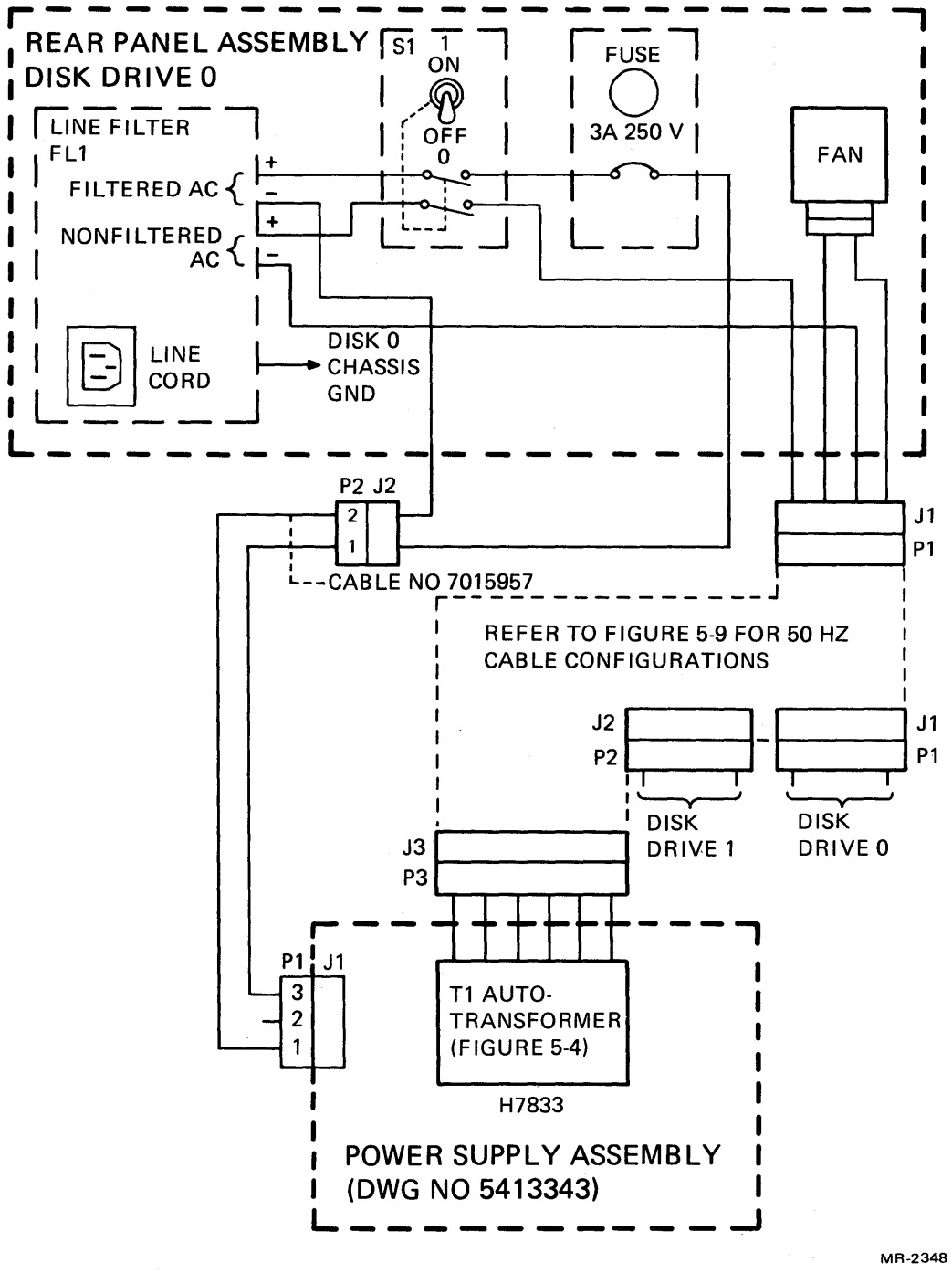


Figure 5-8 AC Power Distribution, 50 Hz Units

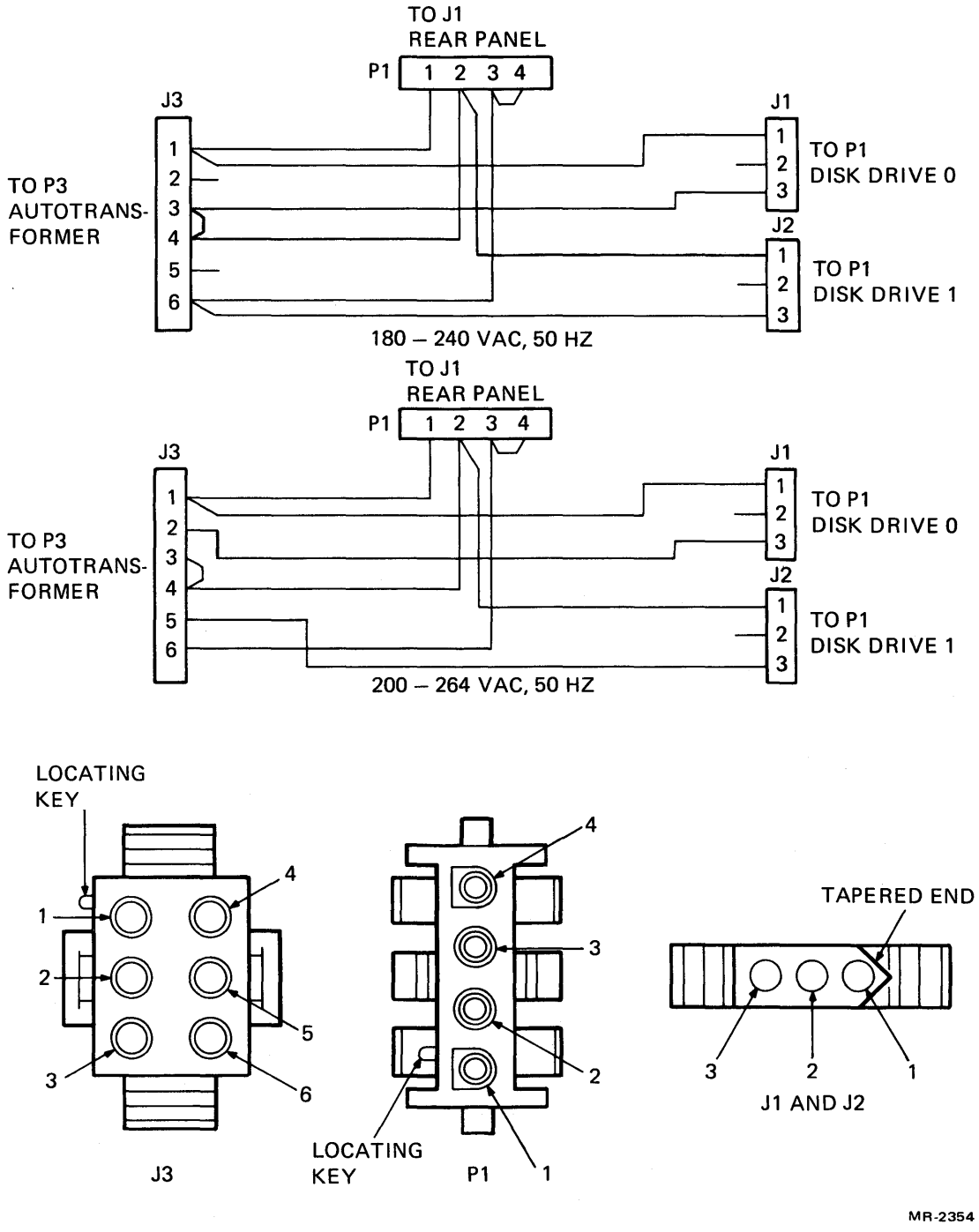


Figure 5-9 50 Hz Internal Cable Configurations (Sheet 1 of 2)

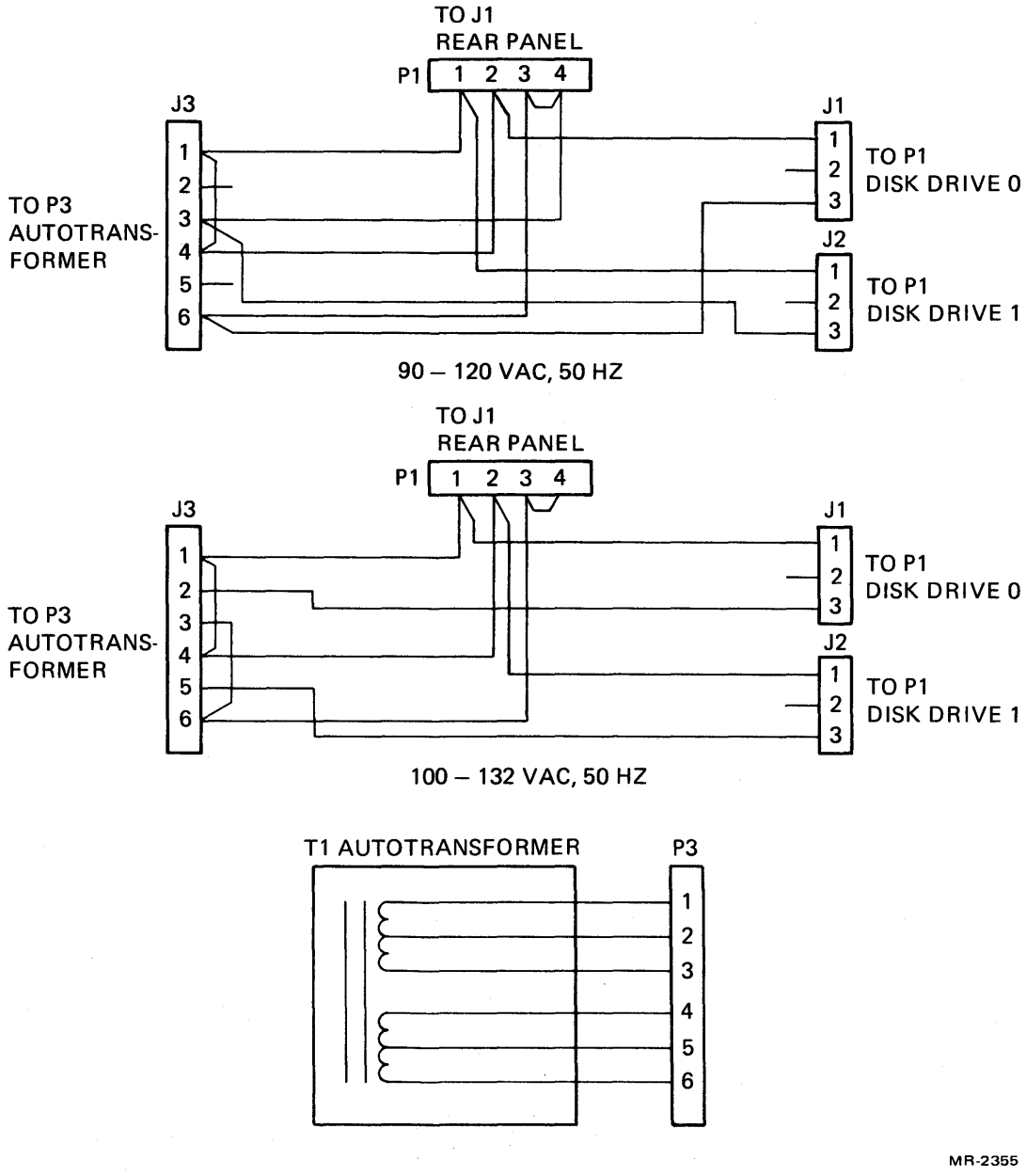


Figure 5-9 50 Hz Internal Cable Configurations (Sheet 2 of 2)

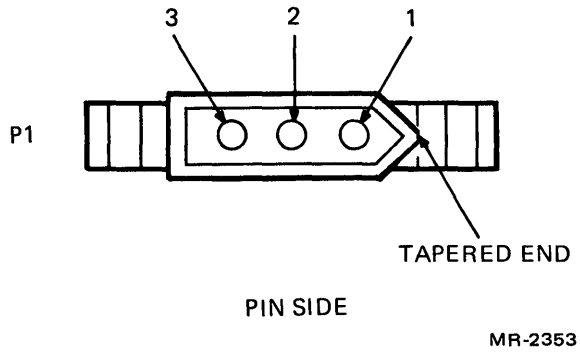


Figure 5-10 Disk Drive Assembly, ac Cable Connector Pin Locations

5.2.3 Initial dc Power Checks

To ensure that the dc power is properly distributed throughout the unit, perform the following procedures.

1. Check to ensure that the ac power is applied as described in Paragraph 5.2.2.
2. Check for a lighted POWER indicator on the front panel of the unit (See Figure 3-1).

NOTE
The POWER indicator monitors the +5 V distributed internally.

3. If the power indicator does not light, disconnect the power cord from the rear panel assembly and remove the rear panel assembly as described in Paragraph 5.3.2.1.
4. Reconnect the ac power cord to the rear panel and check to ensure that ac power is present at connector J2 of the ac cable to the power supply. Refer to Figure 5-4 for location of the J2/P2 connectors.
5. If ac power is present at J2, remove the top cover of the unit as described in Paragraph 5.3.1.1 and raise the TIM group assembly as described in steps 4, 5 and 6 of Paragraph 5.3.4.1.
6. Remove the power connector P1 from PC1–PC4 as shown in Figure 5-23.
7. Test the dc voltages on the P1 connector as shown in Figure 5-13.

NOTE
All the dc voltages produced by the power supply are distributed through connector P1.

8. If the dc voltages are correct, the cause for failure is proably on the Peripheral module.

9. If the dc voltages are not present or not of the correct value, remove the power supply assembly as described in Paragraph 5.3.11.

10. Connect the ac power cable connectors P2/J2 and apply ac power from the rear panel.

11. Test the dc voltages present on connector J2 of the power supply assembly (see Figure 5-11).

12. If the dc voltages are not present or not of the correct value, replace the power supply assembly using the procedures described in Paragraph 5.3.11.

DC Power Distribution

Figure 5-11 shows the power supply connector pin locations and voltages, and Figure 5-12 shows the connector pin locations of the dc power distribution cable (no. 7015953) which attaches to power supply connector J2. This cable assembly distributes power to the Disk Controller module and Intelligence module. The connector pin locations on each of these modules is shown in Figures 5-13 and 5-14, respectively.

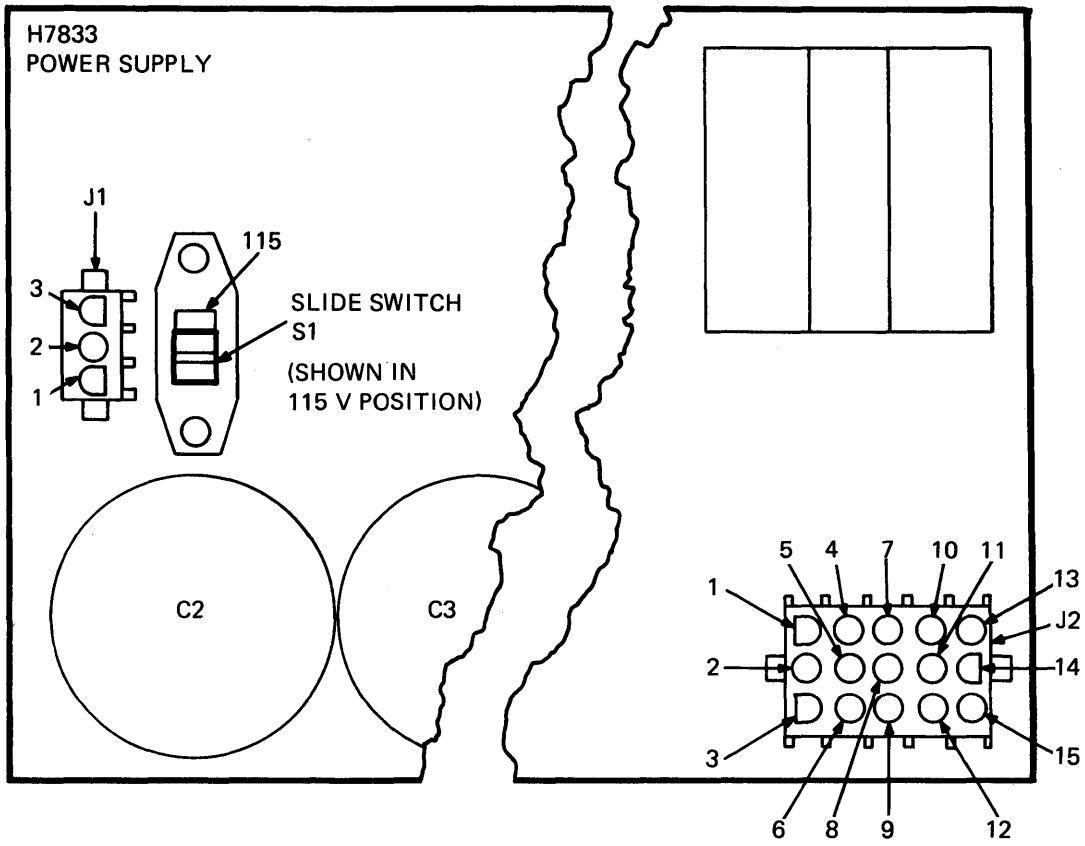
The dc power for the RAM module and the Peripheral module is distributed through the stacking connectors from the Intelligence module. Figure 5-15 shows the stacking connector pin locations and voltage for the RAM module, as does Figure 5-16 for the Peripheral module. Figure 5-16 also shows the pin locations and voltage for connectors J3 and J4, which connect by flat cable to the Cluster EIA module and Standard EIA module.

The dc power is supplied to the Standard EIA module by the flat cable assembly G2 and to the Cluster EIA module by flat cable assembly G3. Figure 5-17 shows the pin locations and voltage to connector J4 of each module.

The Disk Controller module supplies +5 V and +12 V to the disk drive 0 and 1 assemblies through connectors DOP4, DOP6, DIP4, and DIP6.

Refer to Figure 5-13 for the location of the connectors on the module, pin identification and dc voltages. The +5 V dc and other signals to disk drive 1 are distributed through the cable extender module mounted below the disk drive 1 enclosure.

Figure 5-18 shows the location of the cable extender module, the wiring diagram and the locations. This module is included only in the PDT-11/150 dual disk drive units.



H7833 POWER SUPPLY POWER CONNECTORS			
AC INPUT (J1)		DC OUTPUT (J2)	
PIN	POWER	PIN	POWER
1	115 V (-AC)	1	GND
2	NOT USED	4	GND
3	115 V (+AC)	2	+5 V
		5	+5 V
		3	+5 V (GND)
		6	+5 V (GND)
		7	-5 V
		8	-5 V
		9	+24 V (GND)
		10	+12 V (GND)
		11	+12 V (GND)
		12	+24 V
		13	+12 V
		14	+12 V
		15	NOT USED

MR-2357

Figure 5-11 Power Supply, Connector Pins and Voltage

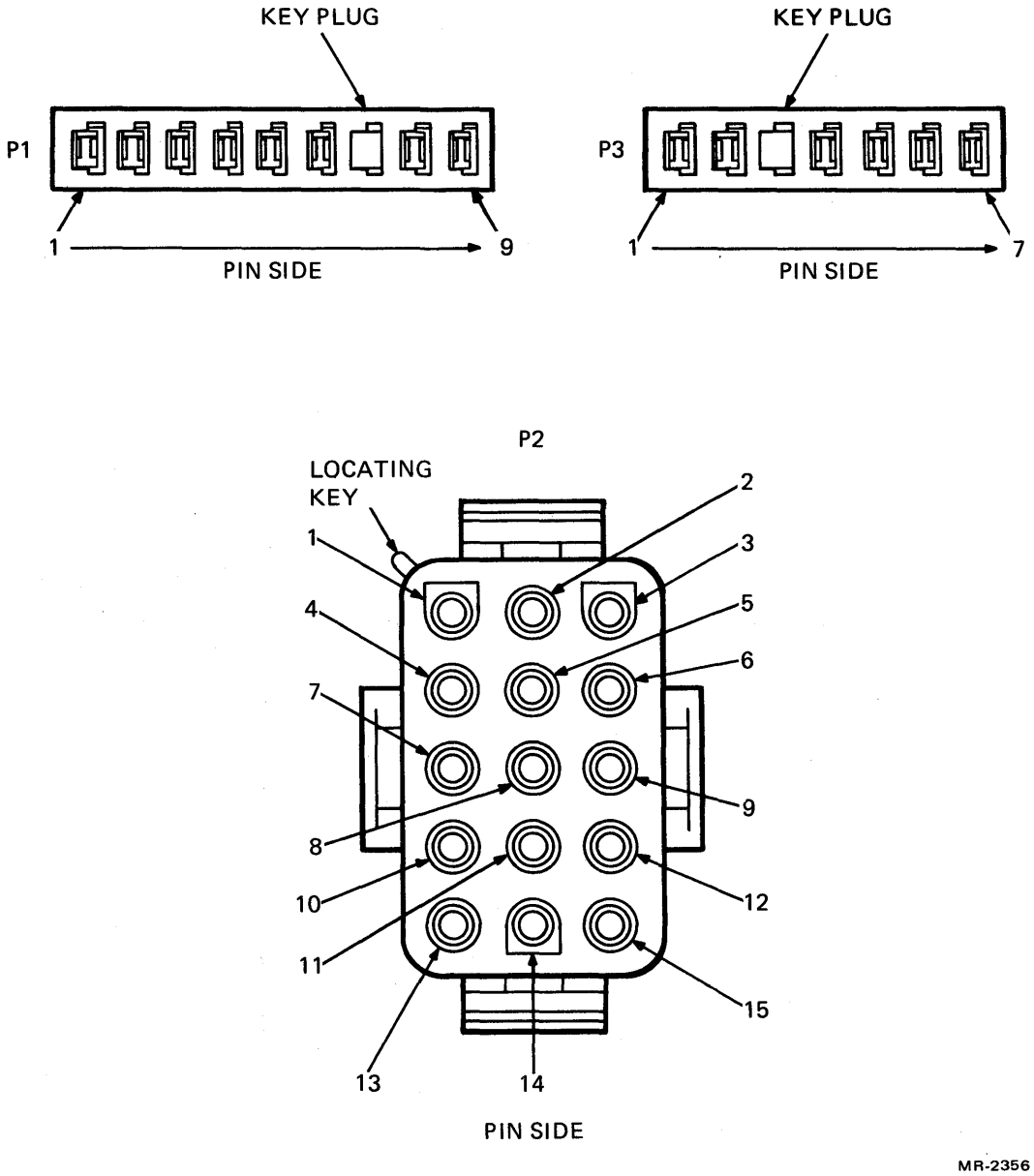
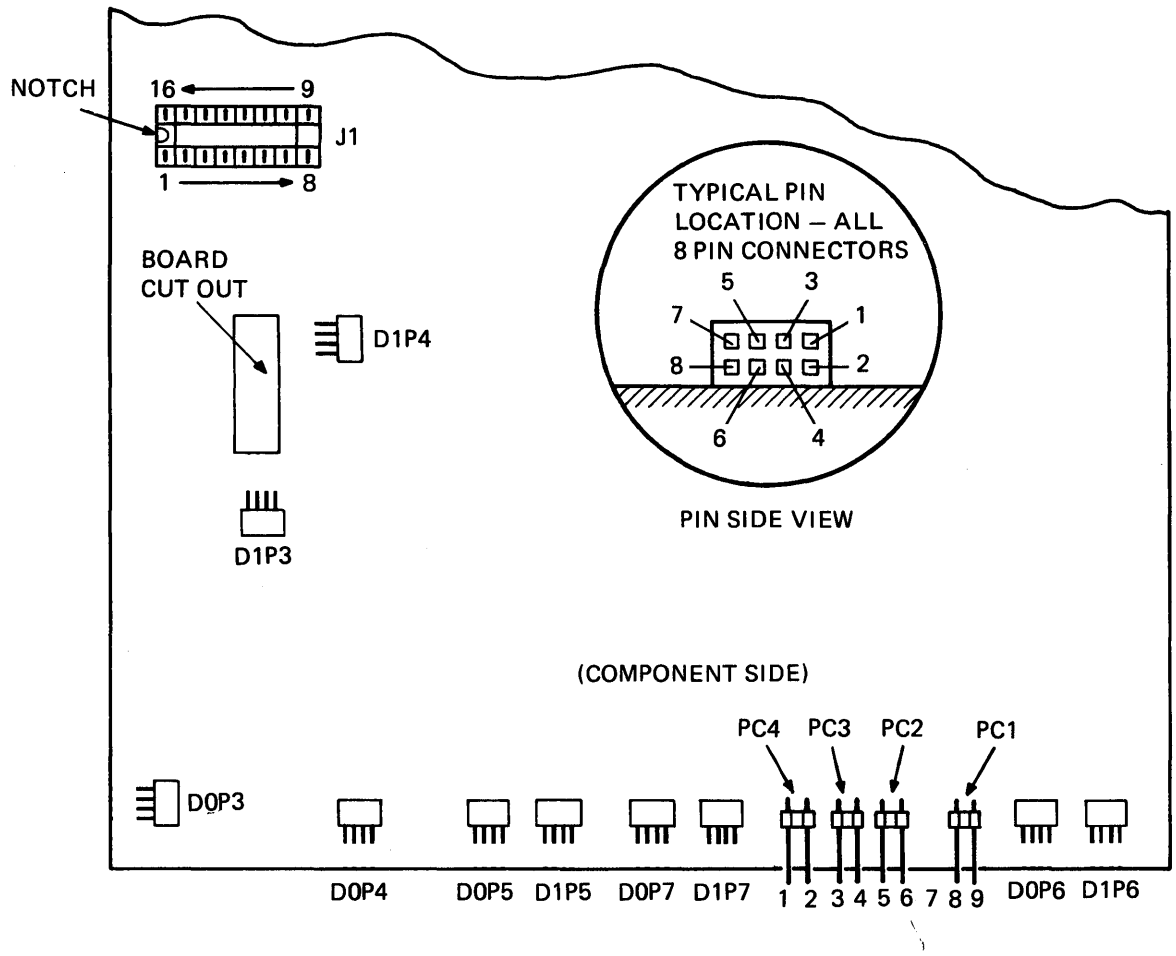


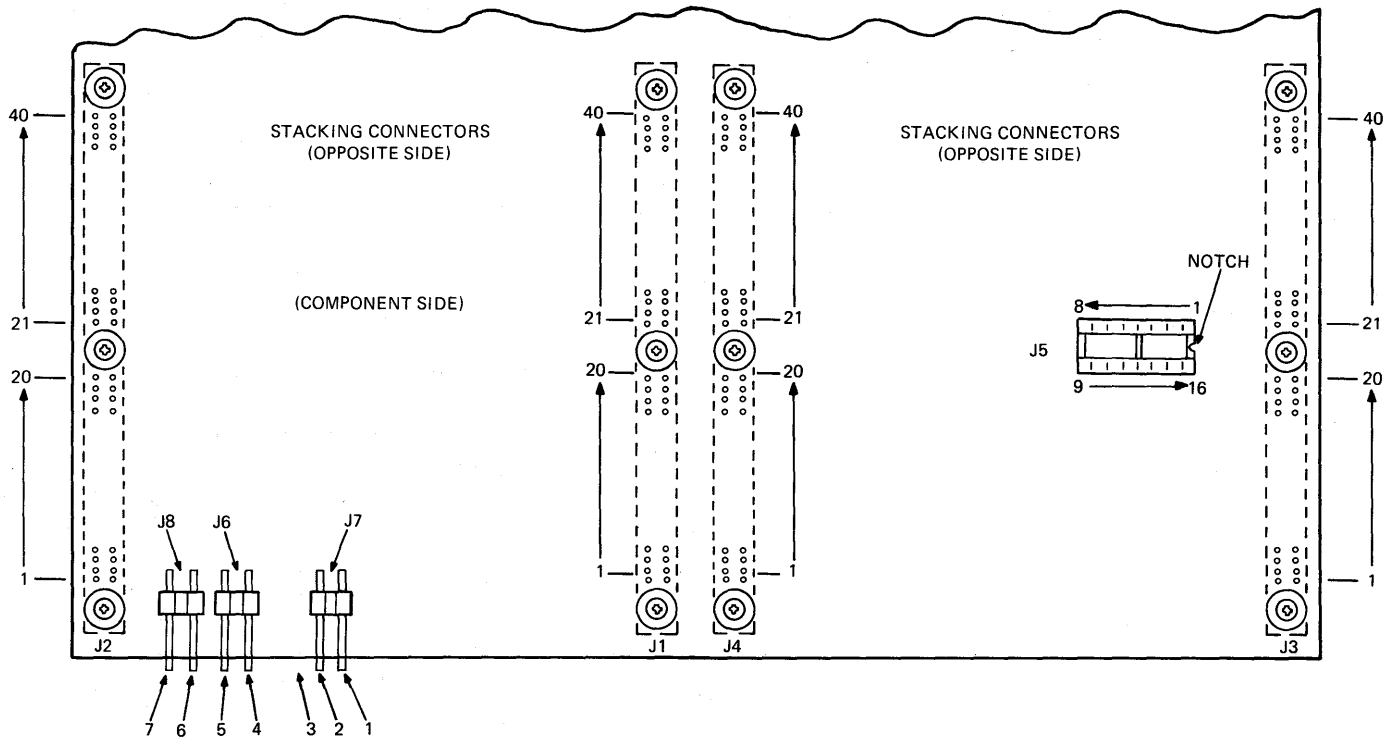
Figure 5-12 DC Power Distribution Cable, Connector Pin Locations



DISK CONTROLLER MODULE CONNECTIONS					
CONNECTOR	PIN	VOLTAGE	CONNECTOR	PIN	VOLTAGE
PC4	1 2	+24 V +24 V GND	D0P4	2	+12 V
PC3	3 4	-5 V GND -5 V	D1P4	2	
PC2	5 6	+5 V GND +5 V	D0P6	5	+5 V
	7	NOT USED	D1P6	5	
PC1	8 9	+12 V GND +12 V			

MR-2363

Figure 5-13 Disk Controller Module, Connector Pins and dc Voltages

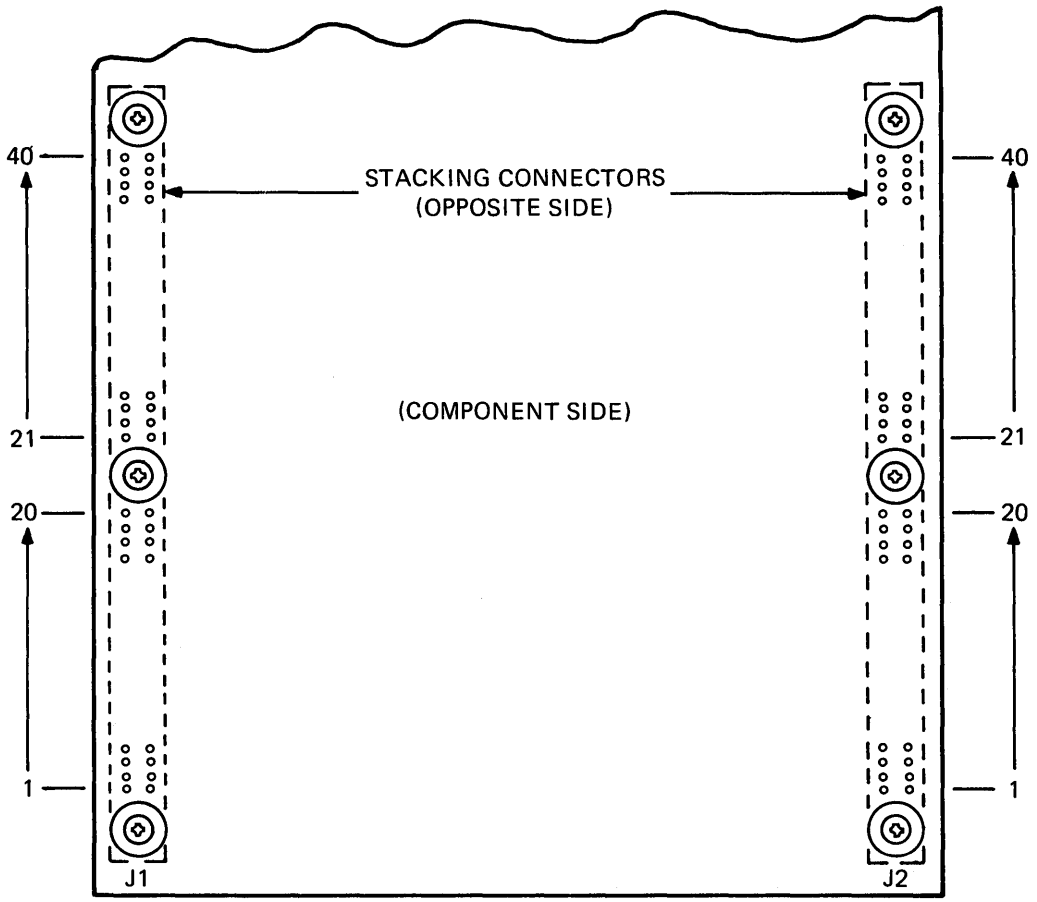


INTELLIGENCE MODULE CONNECTIONS					
CONNECTOR	PIN	VOLTAGE	CONNECTOR	PIN	VOLTAGE
J1	6	-5 V	J1	36	+12 V
	7			37	
	8			38	
	9			39	
	10			40	
	23	+5 V	J2	11	GND
	24			12	
	25			13	
	26			14	
				15	

INTELLIGENCE MODULE CONNECTIONS					
CONNECTOR	PIN	VOLTAGE	CONNECTOR	PIN	VOLTAGE
J3	12	GND	J4	3	-5 V
	13			4	
	14			5	
	15		J7	1	-5 V
	17	-5 V		2	-5 V GND
	18			3	NOT USED
	19		J6	4	+5 V
	20			5	+5 V GND
J4	8	+12 V	J8	6	+12 V GND
	9			7	+12 V
	10				

MR-4001

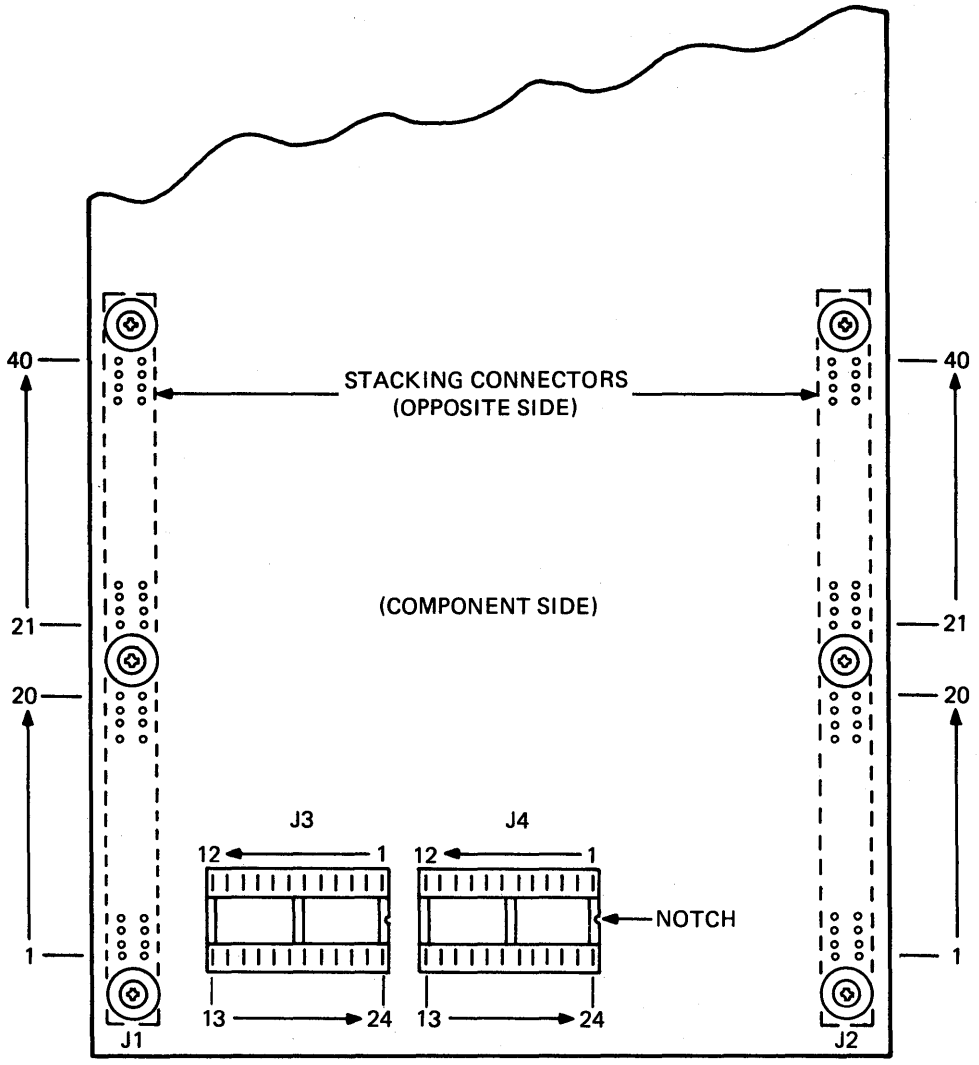
Figure 5-14 Intelligence Module, Connector Pins and dc Voltages



RAM MODULE POWER CONNECTIONS					
CONNECTOR	PIN	VOLTAGE	CONNECTOR	PIN	VOLTAGE
J1	6	-5 V	J1	36	+12 V
	7			37	
	8			38	
	9			39	
	10			40	
	23	+5 V	J2	11	GND
	24			12	
	25			13	
	26			14	
				15	

MR-2359

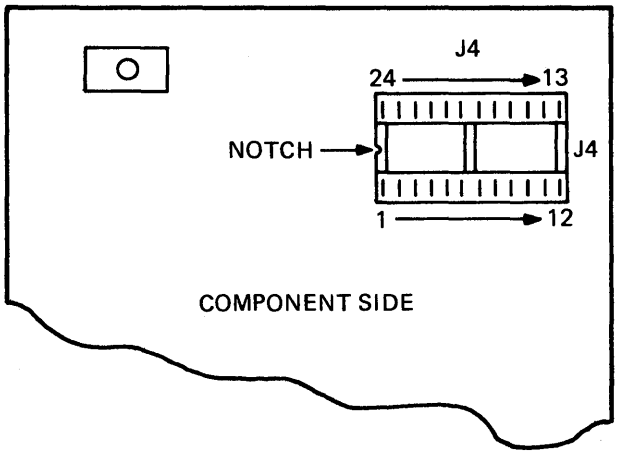
Figure 5-15 RAM Module, Connector Pins and dc Voltages



PERIPHERAL MODULE POWER CONNECTIONS					
CONNECTOR	PIN	VOLTAGE	CONNECTOR	PIN	VOLTAGE
J1	12, 13, 14, 15	GND	J2	3, 4, 5	-5 V
	17, 18, 19, 20	+5 V		8, 9, 10	+12 V
			J3 AND J4	20	+12 V
				22	+5 V
				24	-5 V

MR-2358

Figure 5-16 Peripheral Module, Connector Pins and dc Voltages



EIA MODULE POWER CONNECTIONS		
CONNECTOR	PIN	VOLTAGE
J4	20	+12 V
	22	-5 V
	24	+5 V

MR-2360

Figure 5-17 Standard EIA and Cluster EIA Modules, Connector Pins and dc Voltages

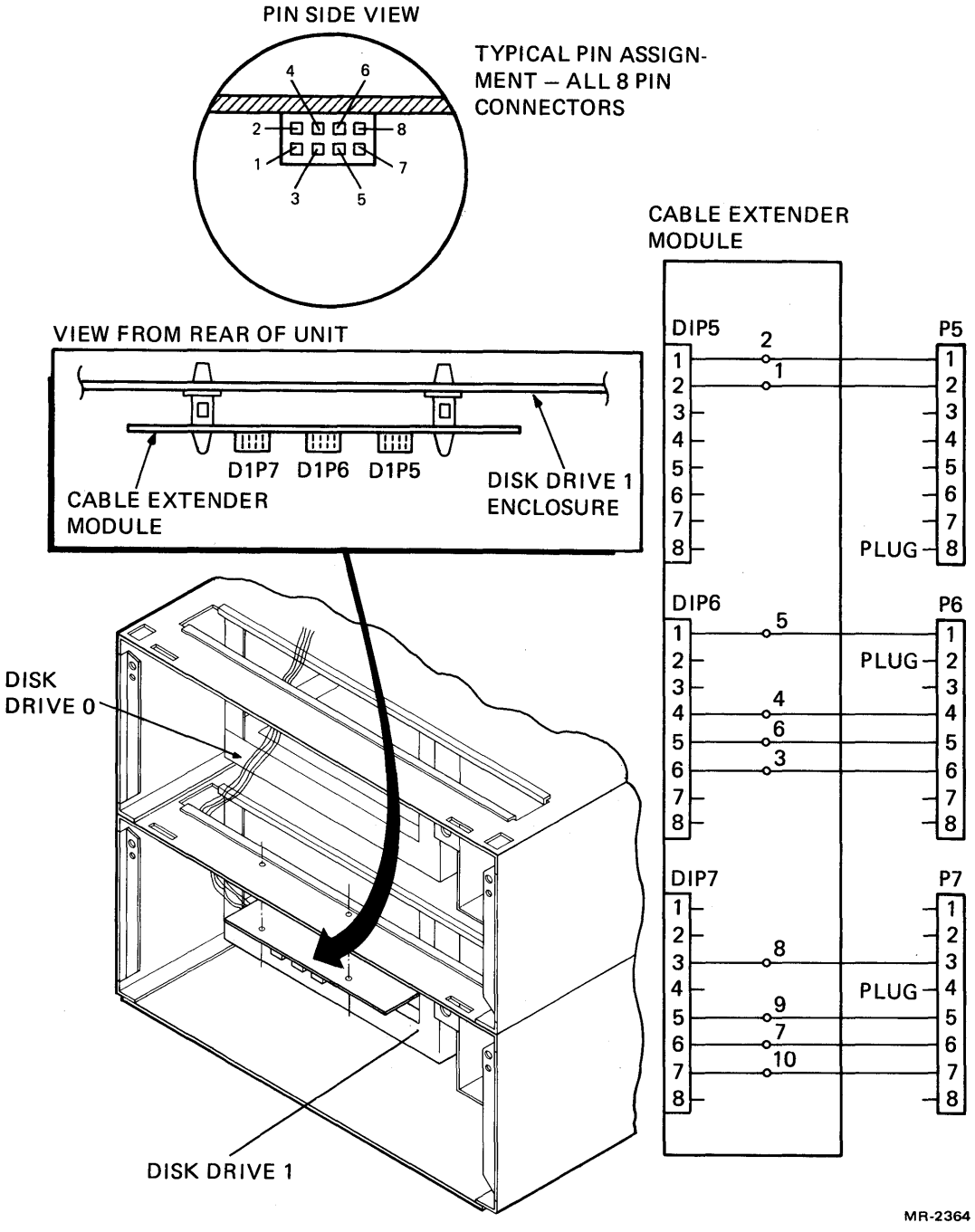


Figure 5-18 Cable Extender, Module Location and Connections

5.3 REMOVAL AND REPLACEMENT PROCEDURES

The following procedures are used to remove and replace the modules, cables and assemblies within the PDT-11/150 unit. Figure 5-19, a removal sequence diagram, identifies the removable items and indicates the sequence of removal.

5.3.1 Top Cover Assembly

The top cover assembly is located on the top of the unit and contains the front panel indicator bezel. To remove and replace the top cover, perform the following procedures.

5.3.1.1 Top Cover Removal

1. Disconnect the ac power cord from the recessed receptacle on the rear panel of the disk drive 0 enclosure (see Figure 5-20).

2. Remove and retain the two (6-32) screws and flat washers behind the access holes located at the top left and right side of the rear panel.

3. Gently slide the top cover assembly toward the front of the unit approximately 1.29 cm (0.5 in) to disengage the cover from the slotted tabs on the enclosure. Lift the cover vertically and remove.

5.3.1.2 Top Cover Replacement

1. Gently place the top cover assembly on the disk drive 0 enclosure so that the front of the cover extends over the front of the disk drive 0 enclosure by approximately 1.29 cm (0.5 in).

2. Slide the top cover toward the rear of the unit to engage the slotted tabs.

   Replace the two (6-32) screws and flat washers removed in step 2 of Paragraph 5.3.1.1.

5.3.2 Rear Panel Assembly, Disk Drive 0 Enclosure

The rear panel assembly is located at the rear of the disk drive 0 enclosure and contains the fan, the device connectors, and the ac power and mode switch.

5.3.2.1 Rear Panel Assembly Removal

1. Disconnect the ac power cord from the recessed receptacle on the rear panel. (See Figure 5-20.)

2. Disconnect any device cables attached to the rear panel.

NOTE

The device cable connectors may be secured to the rear panel by two (4-40) screws located on each side of the connector.

3. Remove and retain the two (8-32) screws used to secure the rear panel to the enclosure.

4. Allow the top edge of the panel to pivot away from the top edge of the enclosure.

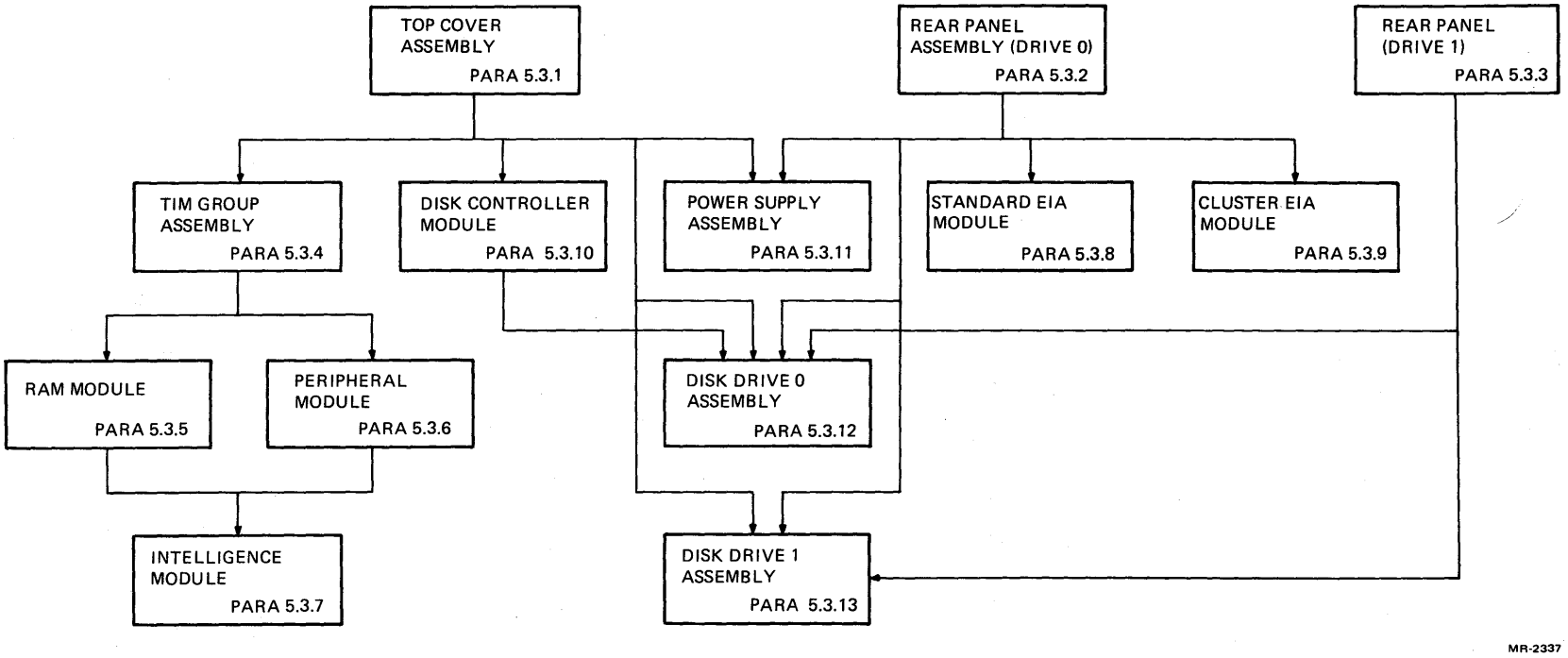


Figure 5-19 PDT-11/150 Removal and Replacement Reference Chart

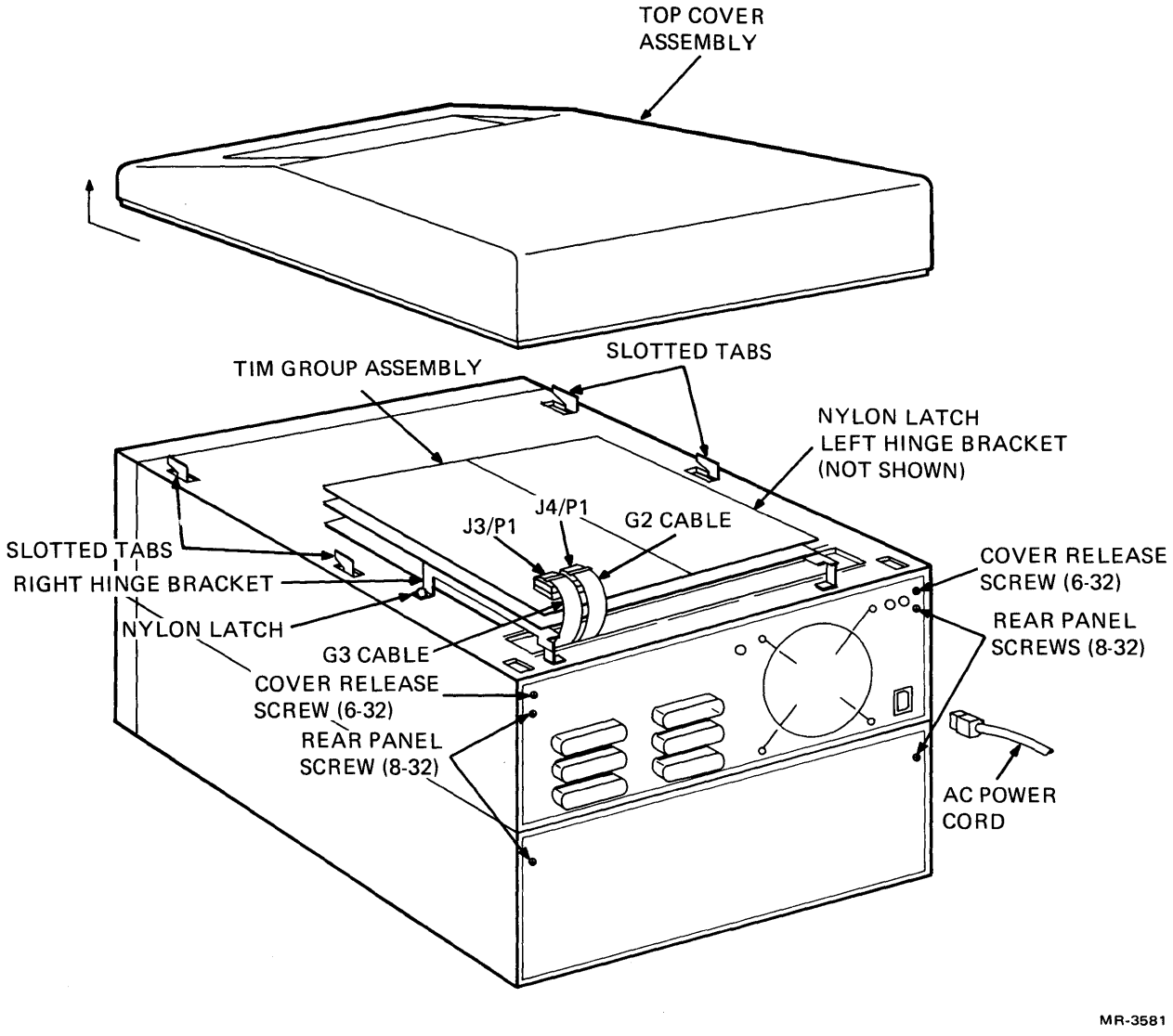


Figure 5-20 Top Cover and TIM Group Assembly, Removal and Replacement

5. Disconnect the flat cable connector P2 from the socket J4 on the Standard EIA module.

NOTE

To prevent damage to the cable or cable connector, alternately insert a screwdriver blade into the slot at each end of the connector and carefully twist the blade to separate the connector from the module socket.

6. If the Cluster EIA module is included on the rear panel, disconnect the flat cable connector P2 from J4 as described in step 5.

7. Lift the panel vertically to disengage the two tabs on the bottom edge of the panel from the slots in the enclosure. (See Figure 5-21.)

8. Disconnect the ac power cable from the rear panel to the power supply by separating P2 from J2.

9. Disconnect the ac power cable from the rear panel to disk drives 0 and 1 by separating connectors J1 and P1.

10. Disconnect the rear panel ground lead by removing the (6-32) screw that secures the ground lead lug to the filter FL1.

11. Remove the rear panel.

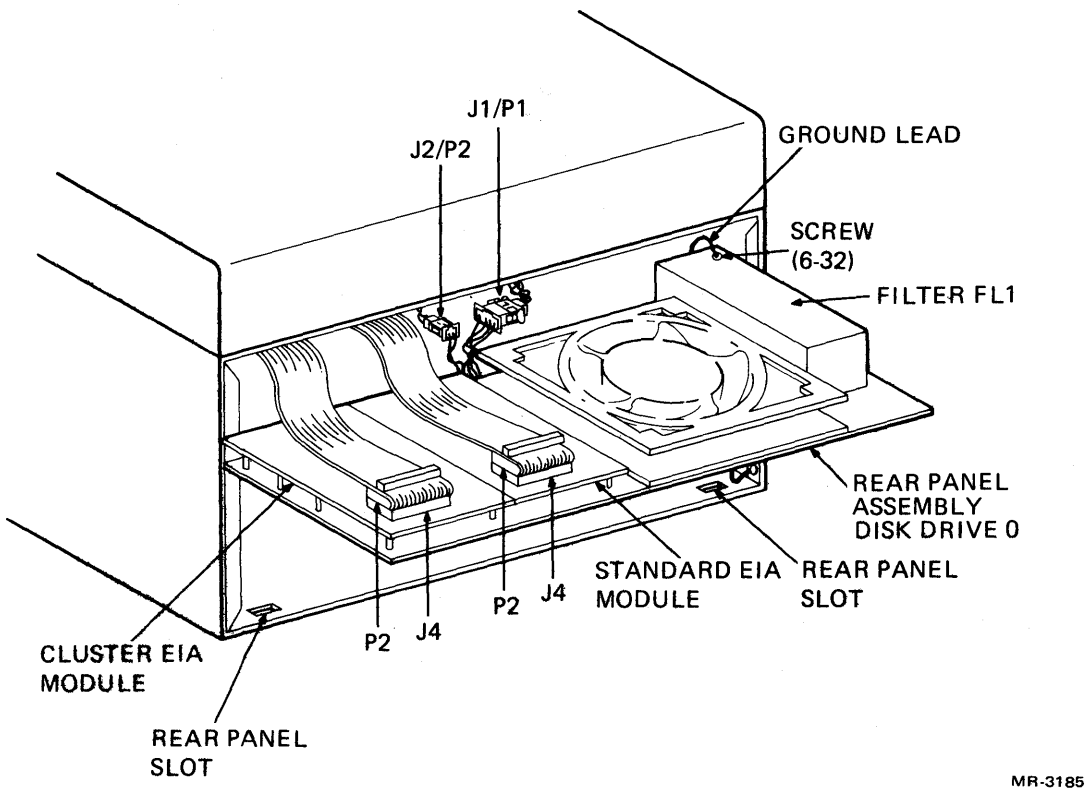


Figure 5-21 Rear Panel Assembly, Removal and Replacement

5.3.2.2 Rear Panel Assembly Replacement

1. Connect the rear panel ground lead removed in step 10 of Paragraph 5.3.2.1.

2. Connect the ac power cable connectors removed in steps 8 and 9 of Paragraph 5.3.2.1.

3. Connect the flat cable connectors removed in steps 5 and 6 of Paragraph 5.3.2.1.

NOTE
Check to ensure all pins of the flat cable connector are straight and evenly spaced before inserting it into the socket. Carefully press the connectors together. Do not allow the cable to twist between connectors.

4. Insert the tabs located on the bottom of the rear panel assembly into the appropriate slots of the disk drive 0 enclosure.

NOTE
Before setting the rear panel into position, check to ensure that the ac power leads are routed away from the signal cables.

5. Replace the two (8-32) rear panel screws removed in step 3 of Paragraph 5.3.2.1.

   Replace the ac power cable removed in step 1 of Paragraph 5.3.2.1.

5.3.3 Rear Panel, Disk Drive 1 Enclosure

The rear panel is located at the rear of the disk drive 1 enclosure and permits access to the cable extender module. To remove and replace the rear panel, perform the following procedures.

5.3.3.1 Rear Panel Removal

1. Remove and retain the two (8-32) screws used to secure the rear panel to the disk drive 1 enclosure (see Figure 5-20).

2. Allow the top edge of the rear panel to pivot away from the housing and lift the panel vertically to disengage the two tabs on the bottom edge of the panel from the slots in the enclosure.

5.3.3.2 Rear Panel Replacement

1. Insert the tabs located on the bottom of the rear panel into the appropriate slots of the disk drive 1 enclosure.

2. Replace the two (8-32) screws removed in step 1 of Paragraph 5.3.3.1.

5.3.4 TIM Group Assembly

The TIM group assembly is located under the top cover and consists of the Intelligence module, RAM module and Peripheral module. To remove and replace the assembly, perform the following procedures.

5.3.4.1 TIM Group Assembly Removal

1. Remove the top cover assembly as described in Paragraph 5.3.1.

2. Disconnect the G2 flat cable connector P1 from the socket J4 on the Peripheral module (see Figure 5-20).

> **NOTE**
> **To prevent damage to the cable or cable connector, alternately insert a screwdriver blade into the slot at each end of the connector and carefully twist the blade to separate the connector from the module socket.**

3. Disconnect the G3 flat cable connector P1 (if included) from the socket J3 on the Peripheral module. See NOTE in step 2.

4. Pull up to release the nylon latches in the module hinge brackets located on the left and right sides of the TIM group assembly.

5. Raise the front of the TIM group assembly until the assembly remains in the vertical position (see Figure 5-22).

6. Carefully slide the slot of the RFI shield away from the cable G1 and fold the shield to the position shown.

7. Disconnect the G1 ribbon cable connector P1 from the socket J5 on the Intelligence module. See NOTE in step 2.

8. Disconnect the power supply cable connector P3 from connectors J6, J7, and J8 on the Intelligence module.

9. Remove and retain the (8-32) screws used to secure the left and right hinge brackets to the top of the disk drive 0 enclosure.

10. Remove the TIM group assembly.

5.3.4.2 TIM Group Assembly Replacement

1. Place the TIM group assembly in its normal mounting position over the Disk Controller module and press the nylon latches released in step 4 of Paragraph 5.3.4.1.

2. Replace the two (8-32) screws removed in step 9 of Paragraph 5.3.4.1.

3. Release the nylon latches and raise the TIM group assembly as described in steps 4 and 5 of Paragraph 5.3.4.1.

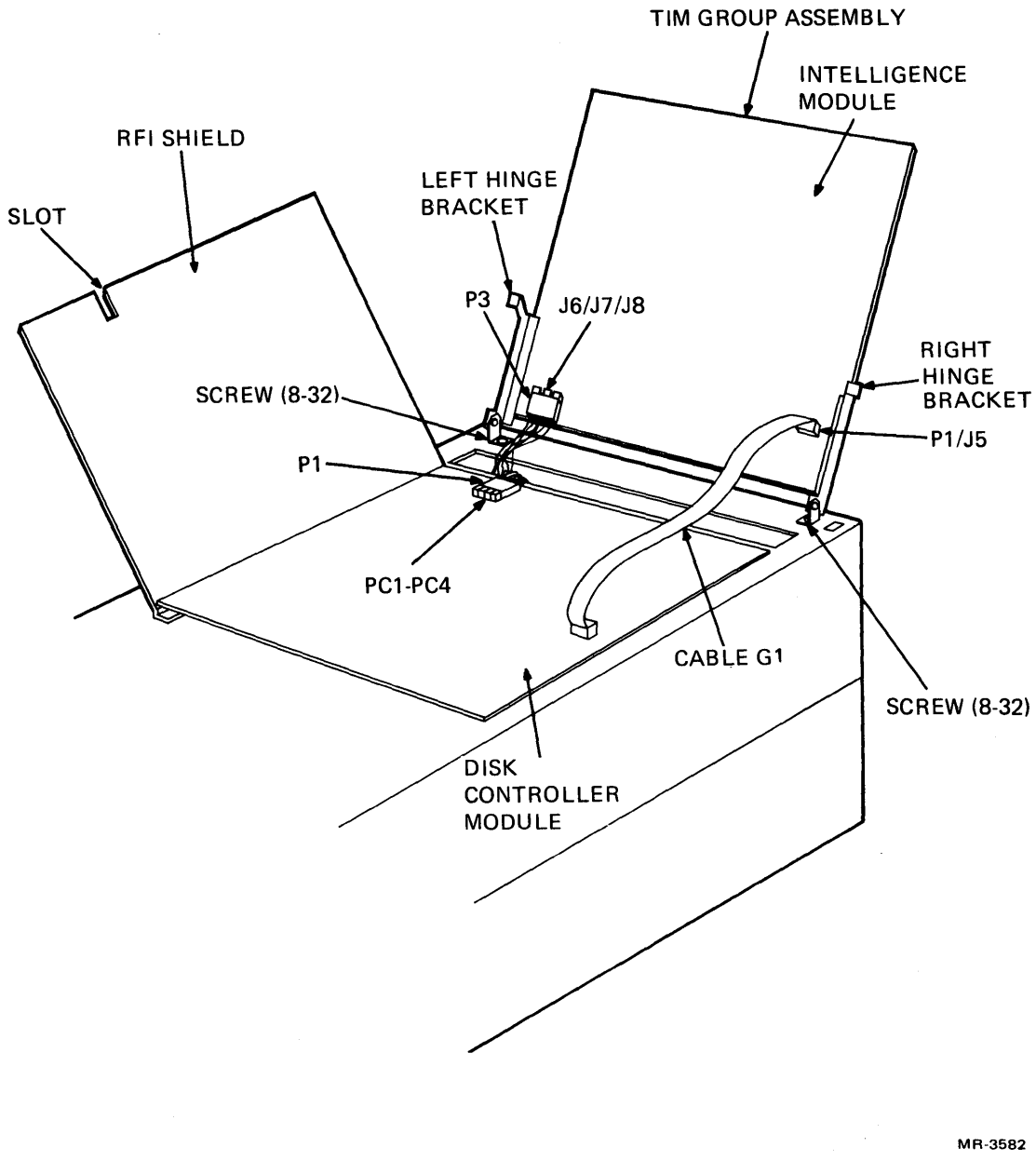


Figure 5-22 TIM Group Assembly Connections

4. Connect the G1 cable connector P1 removed in step 7 of Paragraph 5.3.4.1.

NOTE

Check to ensure that all pins of this flat cable connector are straight and evenly spaced before inserting it into the socket. Carefully press the connectors together. Do not allow the cable to twist between connectors.

5. Fold the RFI shield down over the disk controller module and carefully slide the cable into the slot of the shield.

6. Connect the power supply cable connector P3 removed in step 8 of Paragraph 5.3.4.1.

7. Lower the front of the TIM group assembly to the normal position and press the nylon latches released in step 4 of Paragraph 5.3.4.1 to secure the assembly to the disk drive 0 enclosure.

NOTE

The G1 cable should be routed toward the front of the unit so that the fold in the cable will be close to the POWER indicator of the Peripheral module when the TIM assembly is latched.

5.3.5 RAM Module

The RAM module, part of the TIM group assembly, contains the LSI-11 RAM ICs and the bootstrap loader ROM ICs. To remove and replace the module, perform the following procedures.

5.3.5.1 RAM Module Removal

1. Remove the top cover assembly as described in Paragraph 5.3.1.

2. Remove the TIM group assembly as described in Paragraph 5.3.4.1.

3. Gently place the TIM assembly on a clean, flat surface with the component side of the Intelligence module facing up.

4. Remove and retain the two (4-40) kepnuts used to secure the left hinge bracket to the TIM assembly. Remove the hinge bracket (see Figure 5-23).

5. Turn over the TIM assembly so that the component side of the RAM module is facing up.

6. Remove and retain the (4-40) nylon screw located at the front edge of the RAM module. This screw is mounted into a standoff between the two boards.

7. Remove and retain the two (4-40) 1-inch screws and four (4-40) 7/8-inch screws that are inserted through the two stacking connectors P1 and P2 and into the nutplates.

8. Remove and retain the four insulating strips, two connector clamps and two connector nutplates.

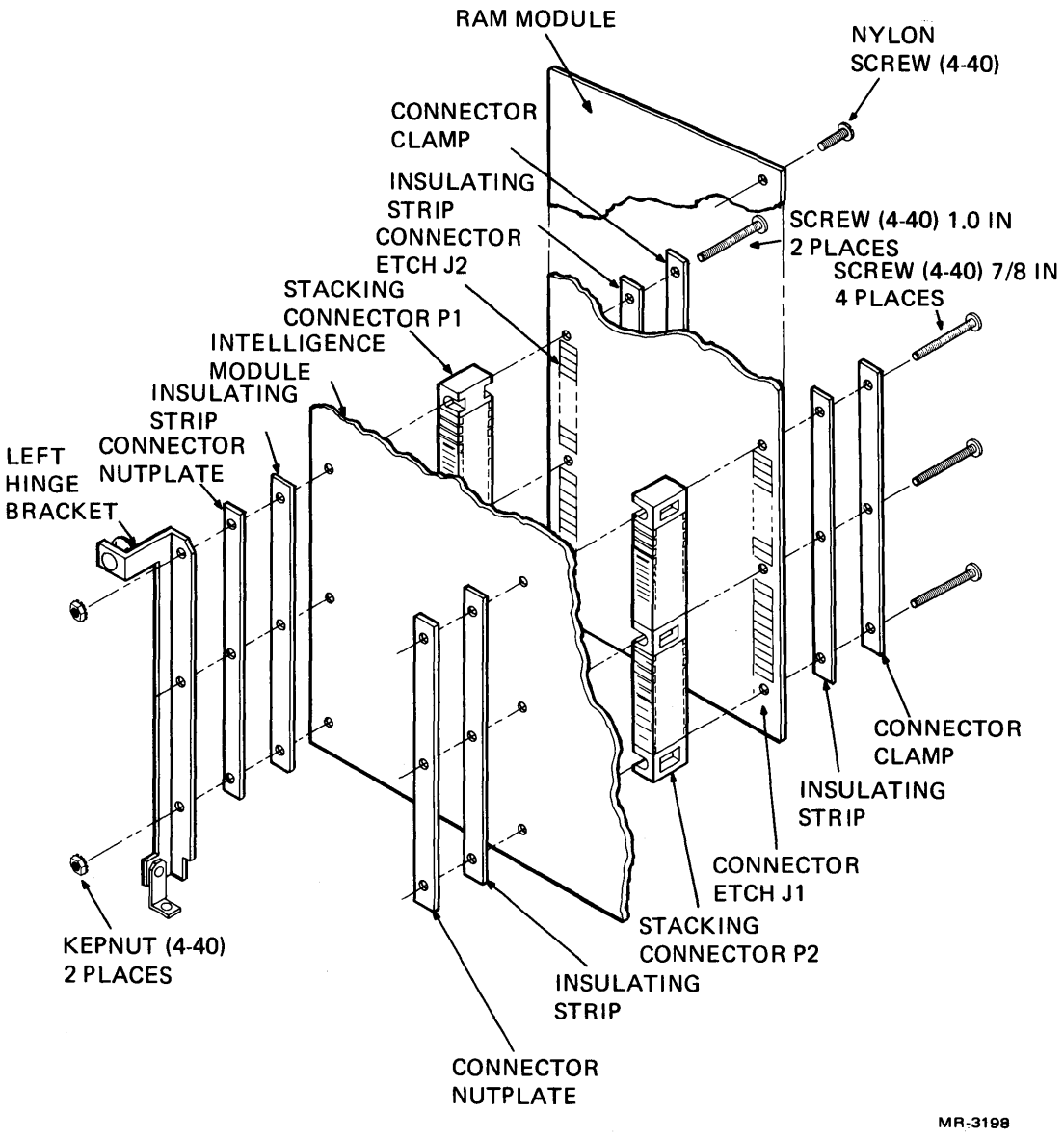


Figure 5-23 RAM Module, Removal and Replacement

9. Lift the RAM module away from the TIM assembly and retain the two stacking connectors P1 and P.

NOTE
Handle the stacking connectors carefully to prevent damage to the connector contacts.

5.3.5.2 RAM Module ROM IC Installation – The bootstrap ROM 0 and ROM 1 ICs used in the RAM module are sensitive to static electricity. When the ROM ICs from the module previously removed are to be used in the replacement module, perform the following procedures.

1. Remove ROM 0 and ROM 1 by inserting a screwdriver blade into the slot at each end of the socket and carefully twist the blade to separate the ICs from the mounting socket (see Figure 5-24).

2. Grasp the body of the IC at the sides adjacent to the pins.

3. Inspect the pins to ensure that they are properly aligned, parallel and at a 90° angle with the body of the IC (see Figure 5-25).

4. If any pins are not parallel, straighten each pin using needlenose pliers, making contact with only one pin at a time.

SOCKET	IC DEC NO.
E7	23032F3
E19	23033F3

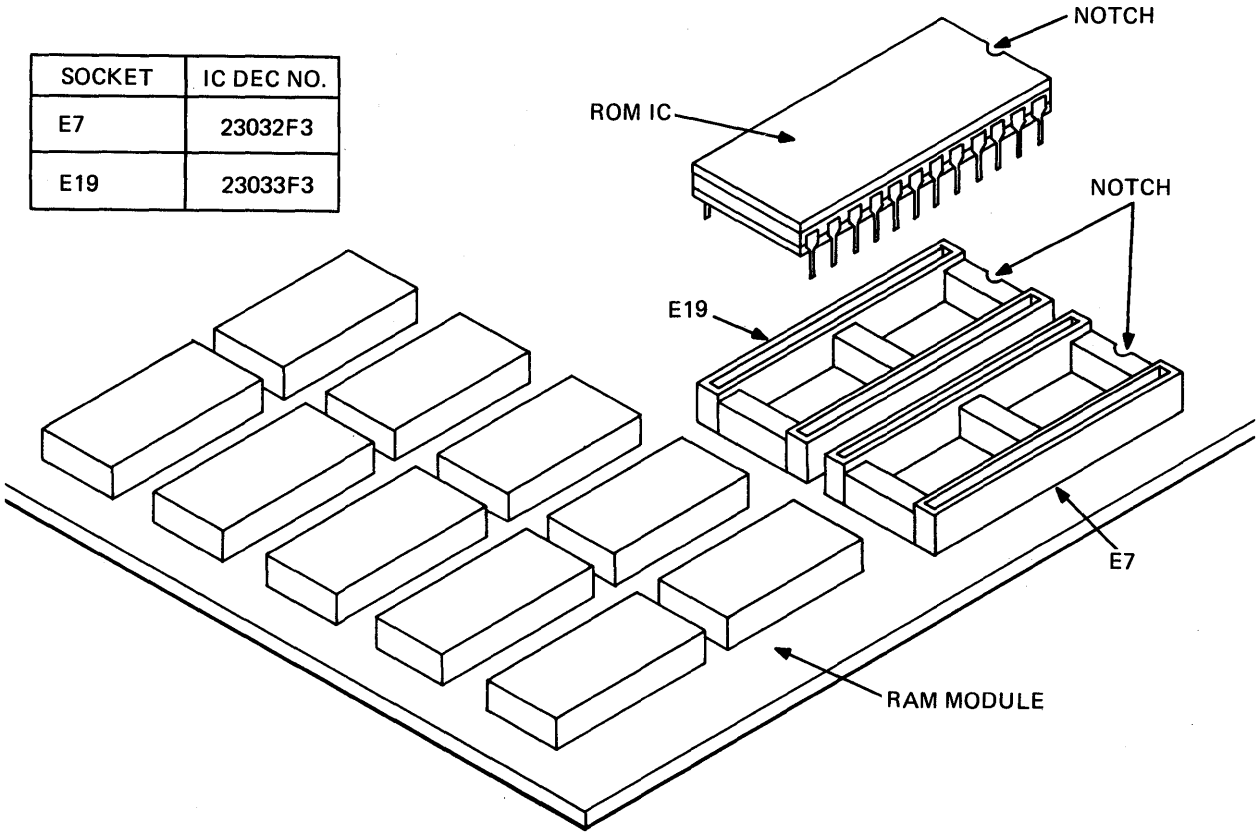


Figure 5-24 RAM Module, ROM IC Removal and Replacement

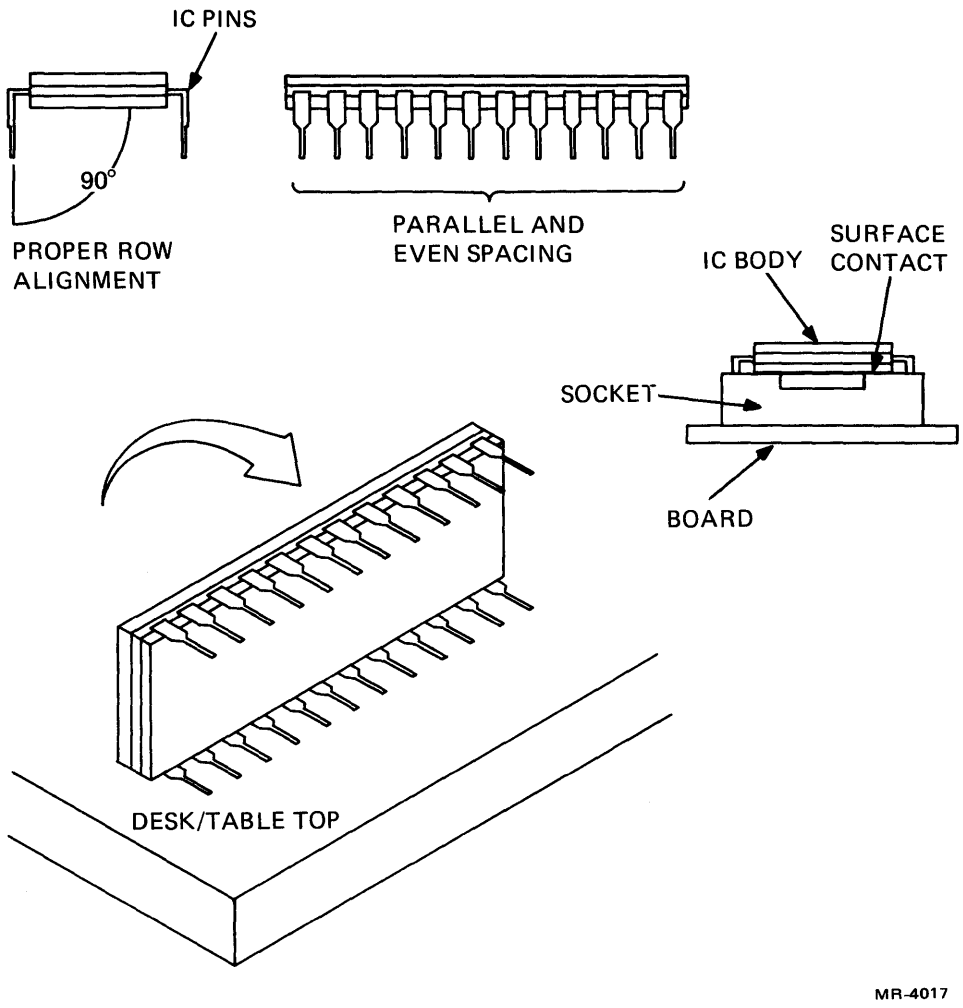


Figure 5-25 ROM IC, Pin Alignment and Mounting

5. If a row of pins is not at the proper angle, gently press the pins against a desk or table top until all pins in the row are aligned.

6. Locate the notch at the end of the IC body and at the end of the IC socket mounted on the module.

7. With the notches positioned at the same end, carefully insert the pins into the socket slots. Insert the IC evenly into the socket by pressing on the top surface of the body.

CAUTION

If excessive resistance occurs, remove the IC and check the pin alignment again.

When properly installed, the body of the IC should make contact with the inner edges of the socket.

When installing new ROM ICs in the replacement RAM module, perform the following procedure. The ROM ICs are supplied separately and are shipped with the pins inserted into conductive foam.

8. Unpack the ROMs but do not remove them from the conductive foam.

9. Gently press the conductive foam against the surface of the module.

10. Remove the ROMs from the conductive foam by grasping the body of each IC at the sides adjacent to the pins.

11. Perform steps 3 through 7.

5.3.5.3 RAM Module Replacement

1. Install the ROM ICs on the RAM module (see Paragraph 5.3.5.2).

2. Insert the 1-inch (4-40) screw shown in Figure 5-23 through the end hole in the connector clamp and insulating strip, and through the corresponding hole in the RAM module.

3. Slide the stacking connector P1 onto the screw and insert the screw through the corresponding hole in the Intelligence module.

CAUTION

The stacking connector pins must be clean and properly aligned before installation with the module. Inspect the connector pins and replace the connector if necessary. Before assembling, carefully clean the connector pins and the module connector etch using denatured alcohol.

4. Slide the insulating strip onto the screw, align the end of the screw with the corresponding threaded hole in the nutplate, and tighten the screw with fingers.

5. Insert the remaining screw and the 7/8-inch (4-40) screw through the corresponding holes and into the nutplate. The 7/8-inch screw is inserted through the center hole of connector P1.

6. Perform steps 2 through 5, inserting the three 7/8-inch (4-40) screws into the opposite side of the RAM module and into stacking connector P2.

7. Align the RAM module with the Intelligence module and tighten all six (4-40) screws using a screwdriver.

NOTE
Use an adequate amount of torque on the (4-40) screws to ensure proper pressure of the stacking connector contacts onto the module etch.

8. Replace the (4-40) nylon screw removed in step 6 of Paragraph 5.3.5.1.

9. Place the left hinge bracket removed in step 4 of Paragraph 5.3.5.1 over the screw threads and replace the two (4-40) kepnuts. Tighten with a nut driver.

10. Remount the TIM group assembly as described in Paragraph 5.3.4.2.

5.3.6 Peripheral Module

The Peripheral module, part of the TIM group assembly, contains three IC sockets in which the USART ICs are installed when the Cluster EIA option is included. The module also contains two jumper lead locations. Perform the following procedures to remove or replace the module.

5.3.6.1 Peripheral Module Removal

1. Remove the top cover assembly as described in Paragraph 5.3.1.

2. Remove the TIM group assembly as described in Paragraph 5.3.4.1.

3. Gently place the TIM assembly on a clean, flat surface with the component side of the Intelligence module facing up.

4. Remove and retain the two (4-40) kepnuts used to secure the right hinge bracket to the TIM group assembly. Remove the hinge bracket (see Figure 5-26).

5. Turn over the TIM assembly so that the component side of the Peripheral module is facing up.

6. Remove and retain the two (4-40) nylon screws located at the front edge of the Peripheral module. These screws are mounted into the standoffs between the boards.

7. Remove and retain the two 1-inch (4-40) and four 7/8-inch (4-40) screws that are inserted through the two stacking connectors P1 and P2 and into the connector nutplates.

8. Remove and retain the four insulating strips, two connector clamps and two connector nutplates.

9. Lift the Peripheral module away from the TIM assembly and retain the two stacking connectors P1 and P2.

NOTE
Handle the stacking connectors carefully to prevent damage to the connector contacts.

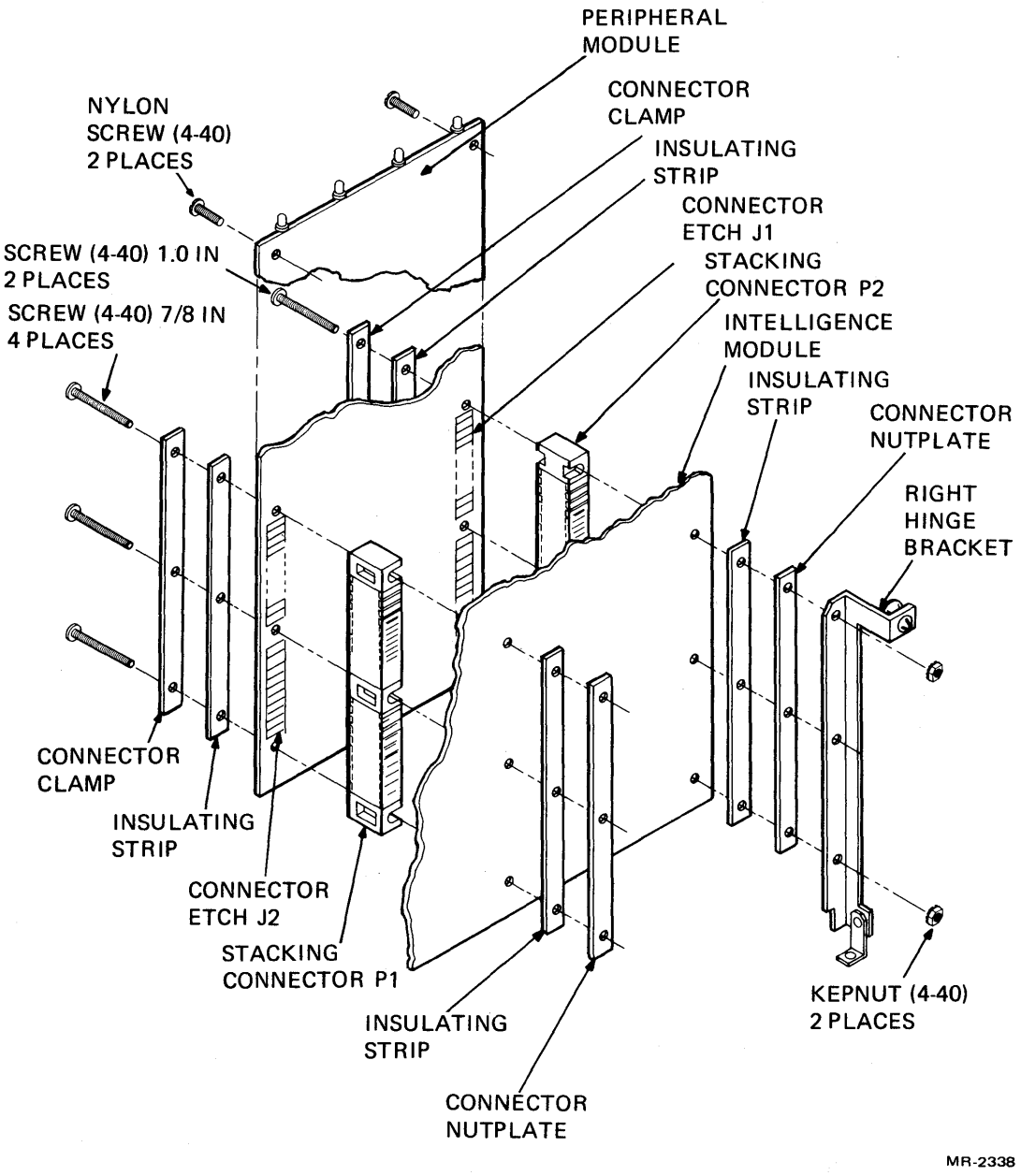


Figure 5-26 Peripheral Module, Removal and Replacement

5.3.6.2 Peripheral Module USART IC Installation - When the Cluster EIA option (DFT11-AB) is included in the PDT-11/150 unit, three USART ICs are mounted in the IC sockets on the Peripheral module. The USART ICs from the module previously removed can be inserted into the IC sockets on the replacement module. To remove or replace the the ICs, perform the following procedure.

1. Remove the USARTs by inserting a screwdriver blade into the slot at each end of the socket. Carefully twist the blade to separate the IC from the socket (see Figure 5-27).

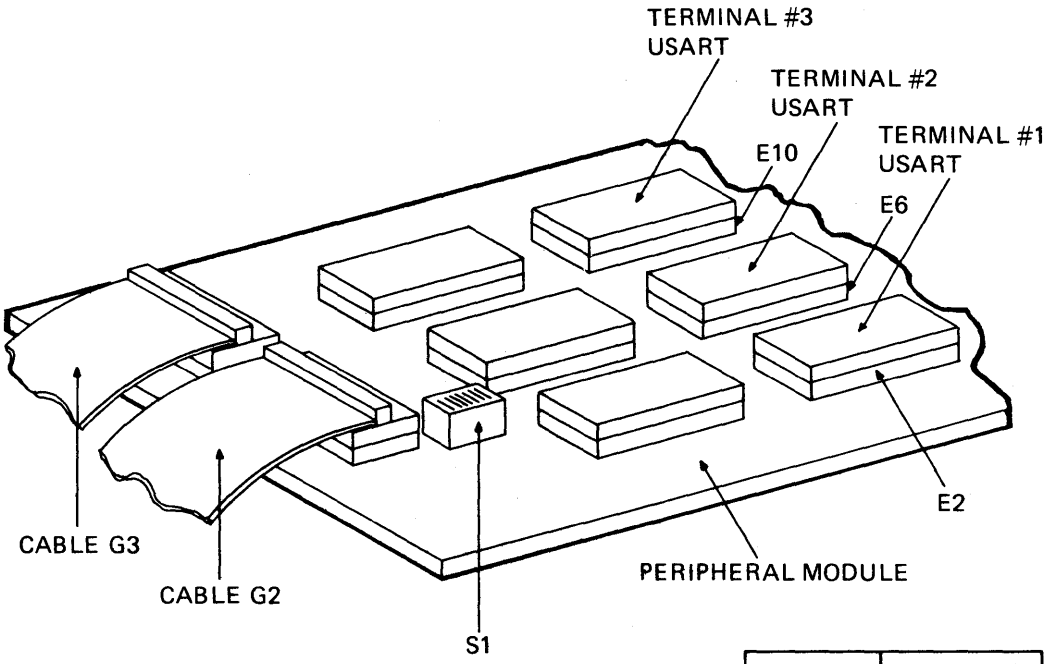
2. Inspect the pins to ensure that they are properly aligned, parallel and at a 90° angle with the body of the IC (see Figure 5-25).

3. If any pins are not parallel, straighten them using needlenose pliers, making contact with only one pin at a time.

4. If a row of pins is not at the proper angle, gently press the pins against a desk or table top until all pins in the row are aligned.

5. Locate the notch at the end of the IC body and at the end of the IC socket mounted on the module.

6. With the notches positioned at the same end, carefully insert the pins into the socket slots.



SOCKET	IC DEC NO.
E2 E6 E10	2115103

MR-3186

Figure 5-27 Peripheral Module, USART Locations

7. Insert the IC evenly into the socket by pressing on the top surface of the body.

CAUTION
If excessive resistance occurs, remove the IC and check the pin alignment again.

When properly installed, the body of the IC should make contact with the inner edges of the socket.

5.3.6.3 Jumper Lead Installation – The Peripheral module contains two jumper lead locations, W1 and W2, as shown in Figure 5-28. When replacing the module in the PDT-11/150 unit, a jumper lead must be installed in position W1 and removed from position W2.

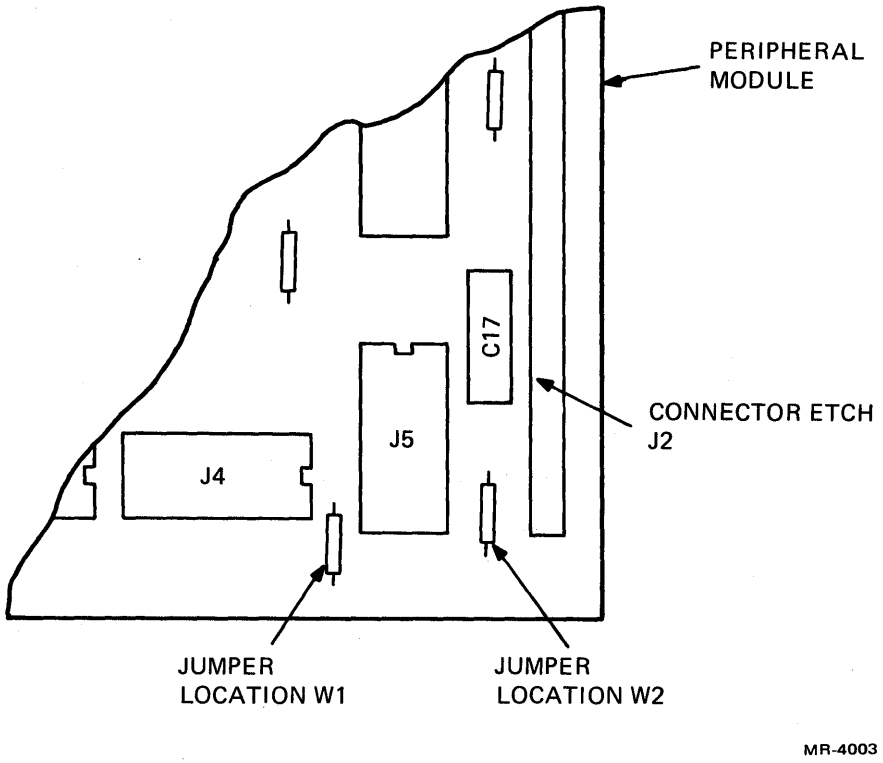


Figure 5-28 Peripheral Module, Jumper Lead Locations

5.3.6.4 Peripheral Module Replacement

1. Insert one 1-inch (4-40) screw (shown in Figure 5-26) through the end hole in the connector clamp and insulating strip, and through the corresponding hole in the RAM module.

2. Slide the stacking connector P1 onto the screw and insert the screw through the corresponding hole in the Intelligence module.

CAUTION

The stacking connector pins must be clean and properly aligned before installation with the module. Inspect the connector pins and replace the connector if necessary. Before assembling, carefully clean the connector pins and the module connector etch using denatured alcohol.

3. Slide the insulating strip onto the screw, align the end of the screw with the corresponding threaded hole in the nutplate, and tighten the screw with fingers.

4. Insert the remaining screw and the 7/8-inch (4-40) screw through the corresponding holes and into the nutplate. The 7/8-inch screw is inserted through the center hole of connector P2.

5. Perform steps 2 through 5, inserting the three 7/8-inch (4-40) screws on the opposite side of the RAM module and into stacking connector P1.

6. Align the Peripheral module with the Intelligence module and tighten all six (4-40) screws using a screwdriver.

NOTE

Use an adequate amount of torque on the (4-40) screws to ensure proper pressure of the stacking connector contacts onto the module etch.

7. Replace the two (4-40) nylon screws removed in step 6 of Paragraph 5.3.6.1.

8. Place the right hinge bracket removed in step 4 of Paragraph 5.3.6.1 over the screw threads and replace the two (4-40) kepnuts. Tighten using a nutdriver.

9. Remount the TIM group assembly as described in Paragraph 5.3.4.2.

5.3.7 Intelligence Module

The Intelligence module, part of the TIM group assembly, contains two removable ROMs and a jumper lead location used when the Cluster EIA option is installed.

5.3.7.1 Intelligence Module Removal

1. Remove the top cover assembly as described in Paragraph 5.3.1.1.
2. Remove the TIM assembly as described in Paragraph 5.3.4.1.
3. Remove the RAM module as described in Paragraph 5.3.5.1.
4. Remove the Peripheral module as described in Paragraph 5.3.6.1.

5.3.7.2 ROM IC Installation – The ROM ICs used in the Intelligence module are sensitive to static electricity. When the ROM ICs from the module previously removed are to be used in the replacement module, perform the following procedures.

1. Remove ROM 0, ROM 1 and ROM 2 by inserting a screwdriver blade into the slot at each end of the socket. Carefully twist the blade to separate the ICs from the mounting socket (see Figure 5-29).

2. Grasp the body of the IC at the sides adjacent to the pins.

3. Inspect the pins to ensure that they are properly aligned, parallel and at a 90° angle with the body of the IC (see Figure 5-25).

4. If any pins are not parallel, straighten each pin using needlenose pliers, making contact with only one pin at a time.

5. If a row of pins is not at the proper angle, gently press the pins against a desk or table top until all pins in the row are aligned.

6. Locate the notch at the end of the IC body and at the end of the IC socket mounted on the module.

7. With the notches positioned at the same end, carefully insert the pins into the socket slots. Insert the IC evenly into the socket by pressing on the top surface of the body.

CAUTION

If excessive resistance occurs, remove the IC and check the pin alignment. When properly installed, the body of the IC should make contact with the inner edges of the socket.

When installing new ROM ICs in the replacement module, perform the following procedure. The ROM ICs are supplied separately and are shipped with the pins inserted into conductive foam.

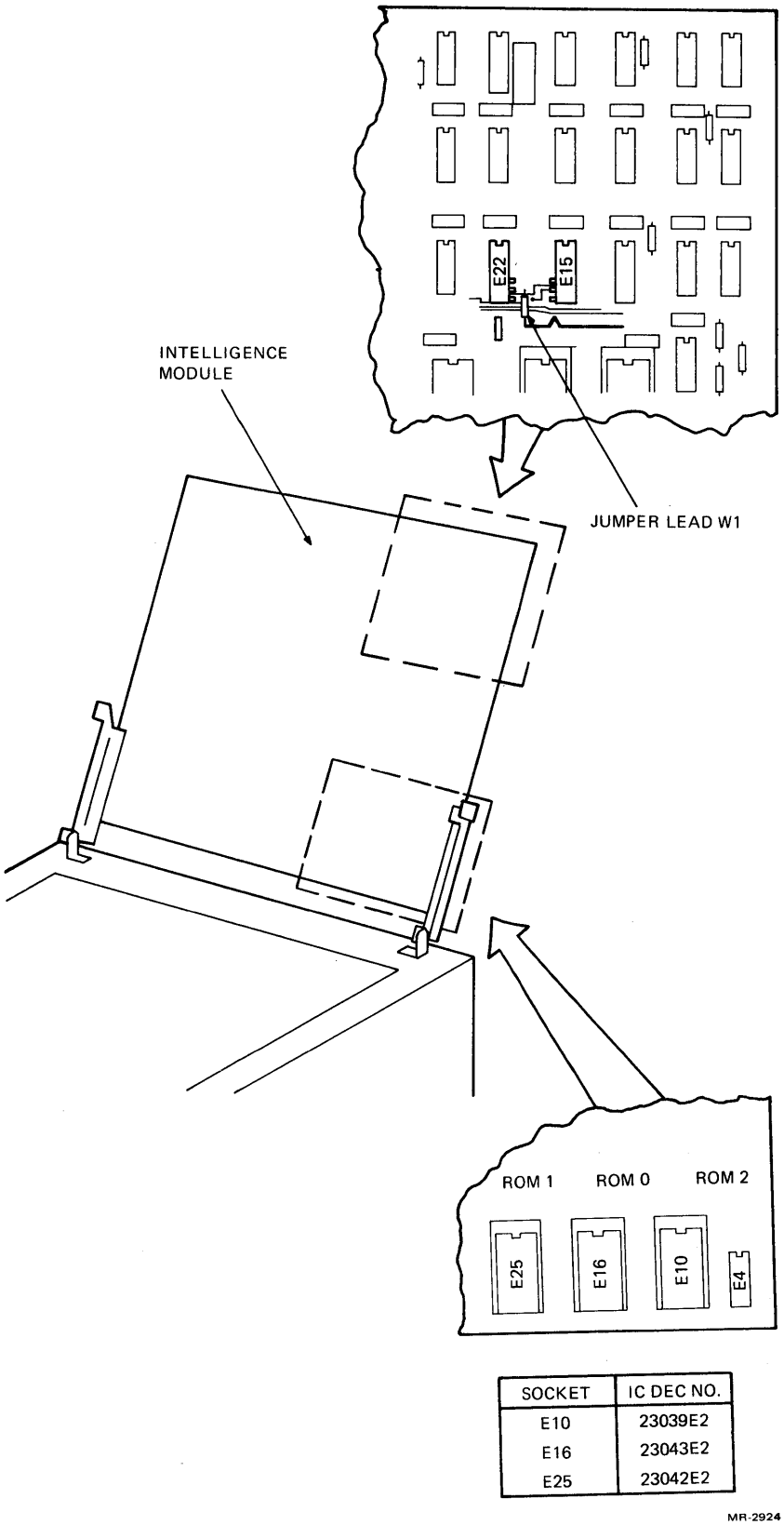
8. Unpack the ROMs but do not remove them from the conductive foam.

9. Gently press the conductive foam against the surface of the module.

10. Remove the ROMs from the conductive foam by grasping the body of each IC at the sides adjacent to the pins.

11. Perform steps 3 through 7.

5.3.7.3 Jumper Lead Installation – Jumper lead W1 must be removed from the module when the PDT-11/150 includes the DFT11-AB Cluster EIA option and installed if the option is not included (see Figure 5-29).



SOCKET	IC DEC NO.
E10	23039E2
E16	23043E2
E25	23042E2

Figure 5-29 Intelligence Module,
ROM IC and Jumper Lead Locations

5.3.7.4 Intelligence Module Installation

1. Replace the Peripheral module as described in Paragraph 5.3.6.4.
2. Replace the RAM module as described in Paragraph 5.3.5.3.
3. Replace the TIM group assembly as described in Paragraph 5.3.4.2.
4. Replace the top cover assembly as described in Paragraph 5.3.1.2.

5.3.8 Standard EIA Module

The Standard EIA module is mounted on the inside of the rear panel of the disk drive 0 enclosure. To remove and replace the module, perform the following procedures.

5.3.8.1 Standard EIA Module Removal

1. Remove the rear panel assembly as described in Paragraph 5.3.3.1.

2. From the outside of the rear panel, remove and retain the six (4-40) hex-head screws and associated washers used to secure the three 25-pin connectors to the rear panel (see Figure 5-30).

3. On the inside of the rear panel, remove and retain the (6-32) kepnut used to secure the module to the ground stud.

4. Remove the module from the rear panel.

5. Remove the ground lead, and remove and retain the 1.27 cm (0.5 in) hex-spacer on the ground stud.

5.3.8.2 Standard EIA Module Replacement

1. Place the hex-spacer and ground lead lug over the (6-32) ground stud.

2. Place the Standard EIA module over the ground stud and allow the mode switch S1 and 25-pin connectors on the module to protrude through the slots in the rear panel.

3. Replace the (6-32) kepnut removed in step 3 of Paragraph 5.3.8.1. Do not tighten.

4. Replace the six washers and six (4-40) hex-head screws removed in step 2 of Paragraph 5.3.8.1.

5. Tighten all nuts and screws.

6. Replace the rear panel assembly as described in Paragraph 5.3.2.2.

5.3.9 Cluster EIA Module

The Cluster EIA module is mounted on the inside of the rear panel assembly of the disk drive 0 enclosure when the DFT11-AB option is installed in the PDT-11/150 unit. To remove or replace the module, perform the following procedures.

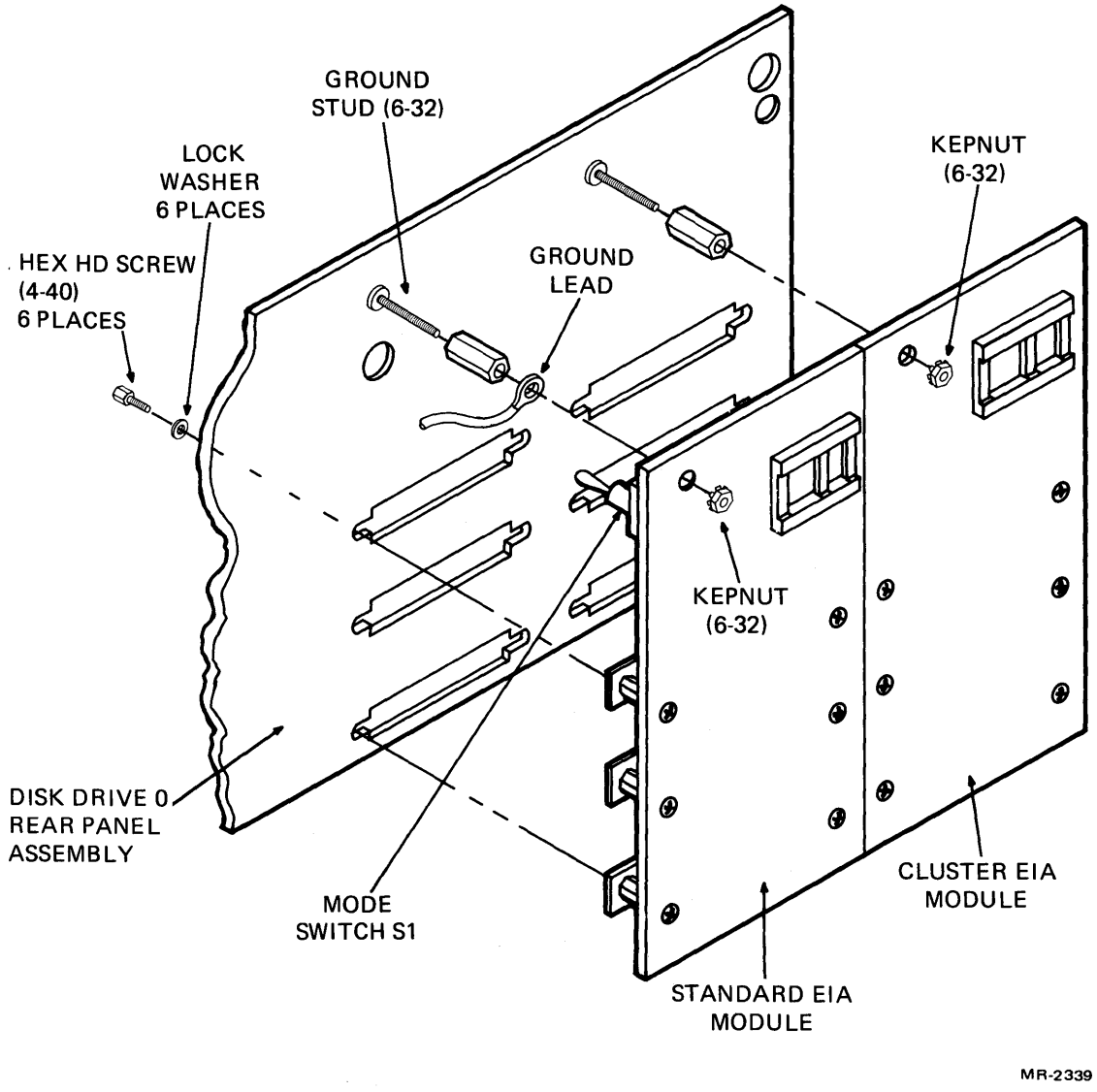


Figure 5-30 Standard EIA and Cluster EIA Modules, Removal and Replacement

5.3.9.1 Cluster EIA Module Removal

1. Remove the rear panel assembly as described in Paragraph 5.3.3.1.

2. From the outside of the rear panel, remove and retain the six (4-40) hex-head screws and associated washers used to secure the three 25-pin connectors to the rear panel. (See Figure 5-30.)

3. On the inside of the rear panel, remove and retain the (6-32) kepnut used to secure the module to the ground stud.

4. Remove the module from the rear panel.

5. Remove and retain the 1.27 cm (0.5 in) hex-spacer on the ground stud.

5.3.9.2 Cluster EIA Module Replacement – If the mounting of the Cluster EIA module is part of the DFT11-AB option installation, refer to the *PDT-11/150 User Guide* (Document No. EK-PT150-UG) for option installation information.

1. Place the hex-spacer over the (6-32) ground stud (see Figure 5-30).

2. Place the Cluster EIA module over the ground stud and allow the 25-pin connectors on the module to protrude through the slots in the rear panel.

3. Replace the (6-32) kepnut removed in step 3 of Paragraph 5.3.9.1. Do not tighten.

4. Replace the six washers and six (4-40) hex-head screws removed in step 2 of Paragraph 5.3.9.1.

5. Tighten the (6-32) kepnut and hex-head screws.

6. Replace the rear panel assembly as described in Paragraph 5.3.2.2.

5.3.10 Disk Controller Module

The Disk Controller module is mounted on the top surface of the disk drive 0 enclosure, and directly beneath the TIM assembly. To remove or replace the module, perform the following procedures.

5.3.10.1 Disk Controller Module Removal

1. Remove the top cover assembly as described in Paragraph 5.3.1.1.

2. Release the left and right hinge brackets by pulling up on the nylon latches (see Figure 5-20).

3. Raise the TIM group assembly to the vertical position (see Figure 5-22).

4. Slide the RFI shield slot away from flat cable G1 and open the shield to the position shown.

5. Disconnect the G1 flat cable connector P2 from connector J1 on the Disk Controller module.

NOTE

Insert a screwdriver tip into the slot at each end of the connector and gently twist the blade to separate the plug from the connector.

6. Disconnect the power supply cable connector P1 from connectors PC1 through PC4 on the Disk Controller module.

7. Disconnect disk drive 0 cable connectors P3 through P7 from module connectors D0P3 through D0P7 (see Figure 5-31).

8. In a dual disk drive unit, disconnect disk drive 1 cable connectors P3 through P7 from module connectors D1P3 through D1P7.

9. Release the Disk Controller module, carefully compressing the tabs on the nylon standoffs used to secure the module to the top of the disk drive 0 enclosure. When the tabs are compressed, raise the module to release it from the standoff.

10. After the module is released from the standoffs, carefully route connectors P3 and P4 (if included) through the slot in the module and remove the module.

5.3.10.2 Disk Controller ROM IC Installation – The Disk Controller module contains a ROM IC that is removable and can be inserted into the socket of the replacement module. The ROM IC is sensitive to static electricity and must be handled with care. To remove and replace the ROM IC, perform the following procedures.

1. Remove the ROM IC by inserting a screwdriver blade into the slot at each end of the socket and carefully twist the blade to separate the IC from the mounting socket (see Figure 5-32).

2. Grasp the body of the IC at the sides adjacent to the pins.

3. Inspect the pins to ensure that they are properly aligned, parallel and at a 90° angle with the body of the IC (see Figure 5-25).

4. If any pins are not parallel, straighten each pin using needlenose pliers, making contact with only one pin at a time.

5. If a row of pins is not at the proper angle, gently press the pins against a desk or table top until all pins in the row are aligned.

6. Locate the notch at the end of the IC body and at the end of the IC socket mounted on the module.

7. With the notches positioned at the same end, carefully insert the pins into the socket slots.

   Insert the IC evenly into the socket by pressing on the top surface of the body.

CAUTION
If excessive resistance occurs, remove the IC and check the pin alignment again.

When properly installed, the body of the IC should make contact with the inner edges of the socket.

When installing a new ROM IC in the replacement module, perform the following procedure. The ROM IC is supplied separately and shipped with the pins inserted into conductive foam.

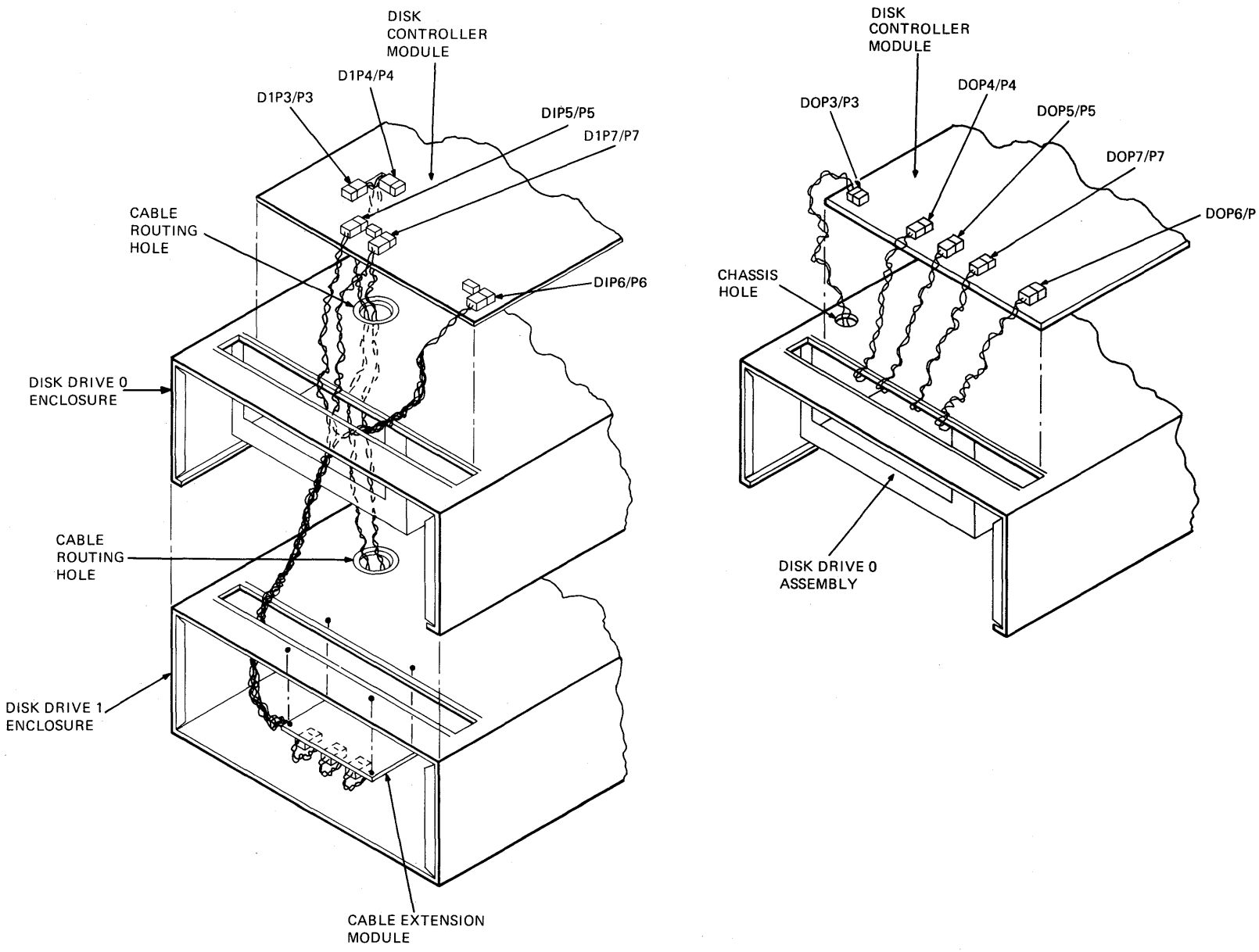


Figure 5-31 Disk Drive Cable Routing

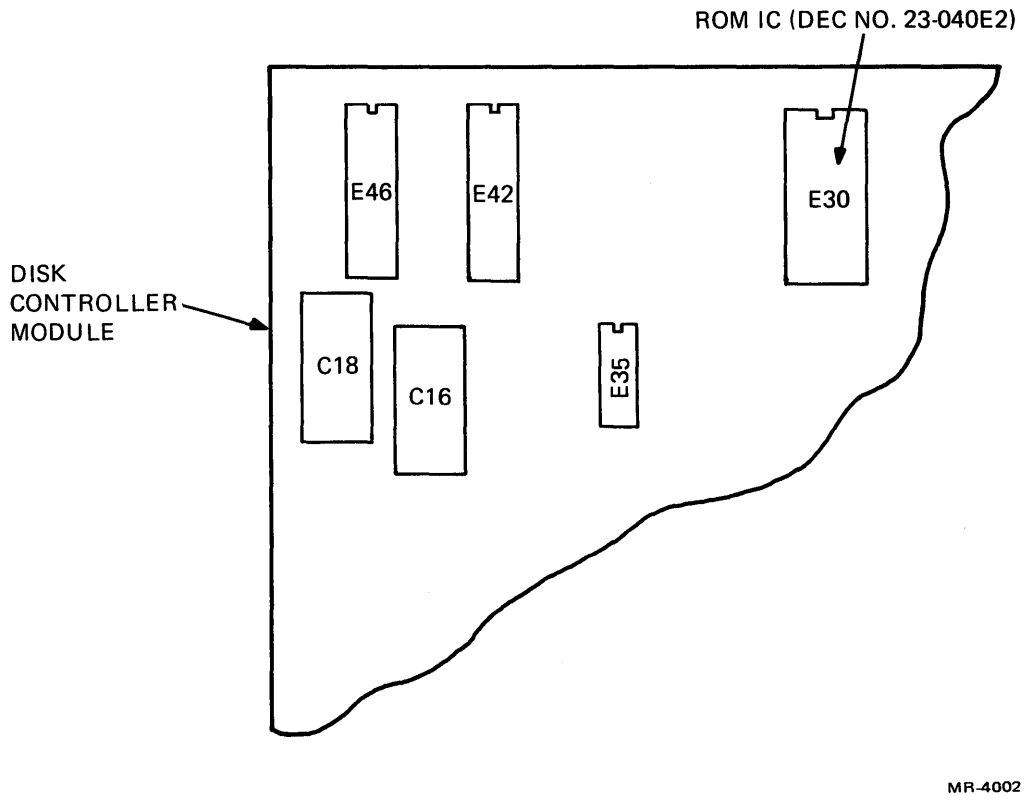


Figure 5-32 Disk Controller Module, ROM IC Location

8. Unpack the ROMs but do not remove them from the conductive foam.

9. Gently press the conductive foam against the surface of the module.

10. Remove the ROMs from the conductive foam by grasping the body of each IC at the sides adjacent to the pins.

11. Perform steps 3 through 7.

5.3.10.3 Disk Controller Module Replacement

1. Place the Disk Controller module over the disk drive 0 enclosure with the slot in the module positioned over the cable routing hole. (See Figure 5-31.)

2. Route connectors P3 and P4 from disk drive 1 (if included) through the slot in the module.

3. Position the module so that the mounting holes in the module are located directly over the nylon standoffs mounted on the top surface of the disk drive 0 enclosure.

4. Press the module so that each nylon standoff protrudes through the mounting holes, and the compression tabs of the standoffs securely hold the module.

5. Connect P3 through P7 removed in step 8 of Paragraph 5.3.10.1.

6. Connect P3 through P7 removed in step 7 of Paragraph 5.3.10.1.

7. Connect P1 removed in step 6 of Paragraph 5.3.10.1.

8. Connect the G1 flat cable connection P2 removed in step 5 of Paragraph 5.3.10.1.

9. Fold the RFI shield down over the Disk Controller module and carefully slide the cable into the slot of the shield.

NOTE

The G1 cable should be routed toward the front of the unit so that the fold in the cable will be close to the POWER indicator of the Peripheral module when the TIM assembly is latched.

10. Lower the front of the TIM group assembly to the normal position and press the nylon latches perviously released in step 2 of Paragraph 5.3.10.1.

11. Replace the top cover assembly as described in Paragraph 5.3.1.2.

5.3.11 Power Supply Assembly

The power supply assembly is located on the left side of the disk drive 0 enclosure. To remove and replace the power supply assembly and power supply module, perform the following procedures.

5.3.11.1 Power Supply Assembly Removal

1. Remove the top cover as described in Paragraph 5.3.1.1.
2. Pull up on the nylon latch in the left and right hinge brackets to release the TIM assembly (see Figure 5-20).
3. Raise the TIM assembly to the vertical position (see Figure 5-22).
4. Slide the RFI shield slot away from flat cable G1 and open the shield to the position shown.
5. Disconnect the power supply cable connector P3 from connectors J6, J7, and J8 on the Intelligence module.
6. Disconnect the power supply cable connector P1 from connectors PC1 through PC4 of the Disk Controller module.
7. Route the power supply cable connectors P1 and P3 down through the slot in the top of the disk drive 0 enclosure at the rear.
8. Remove the rear panel assembly of the disk drive 0 enclosure as described in Paragraph 5.3.2.1.
9. Remove the (8-32) screw that secures the ground lead to the power supply assembly (see Figure 5-33).
10. Release the power supply assembly by removing the (8-32) screw that holds the slide plate to the center support of the disk drive 0 enclosure.
11. Pull the power supply assembly toward the rear of the unit and remove.

5.3.11.2 Power Supply Module Installation

The power supply module of the power supply assembly is removable and can be replaced when required. To remove and replace the module perform the following procedures.

1. Disconnect connector P2 from J2 of the power supply module and remove the cable assembly.
2. Disconnect connector P1 from J1 (see Figure 5-34).
3. Remove and retain the four (6-32) screws, metal washers, and nylon washers used to secure the power supply module to the slide plate.
4. Remove and retain the ground (6-32) screw and metal washer.
5. Remove the power supply module.
   To replace the module, perform the removal procedures in the reverse order.

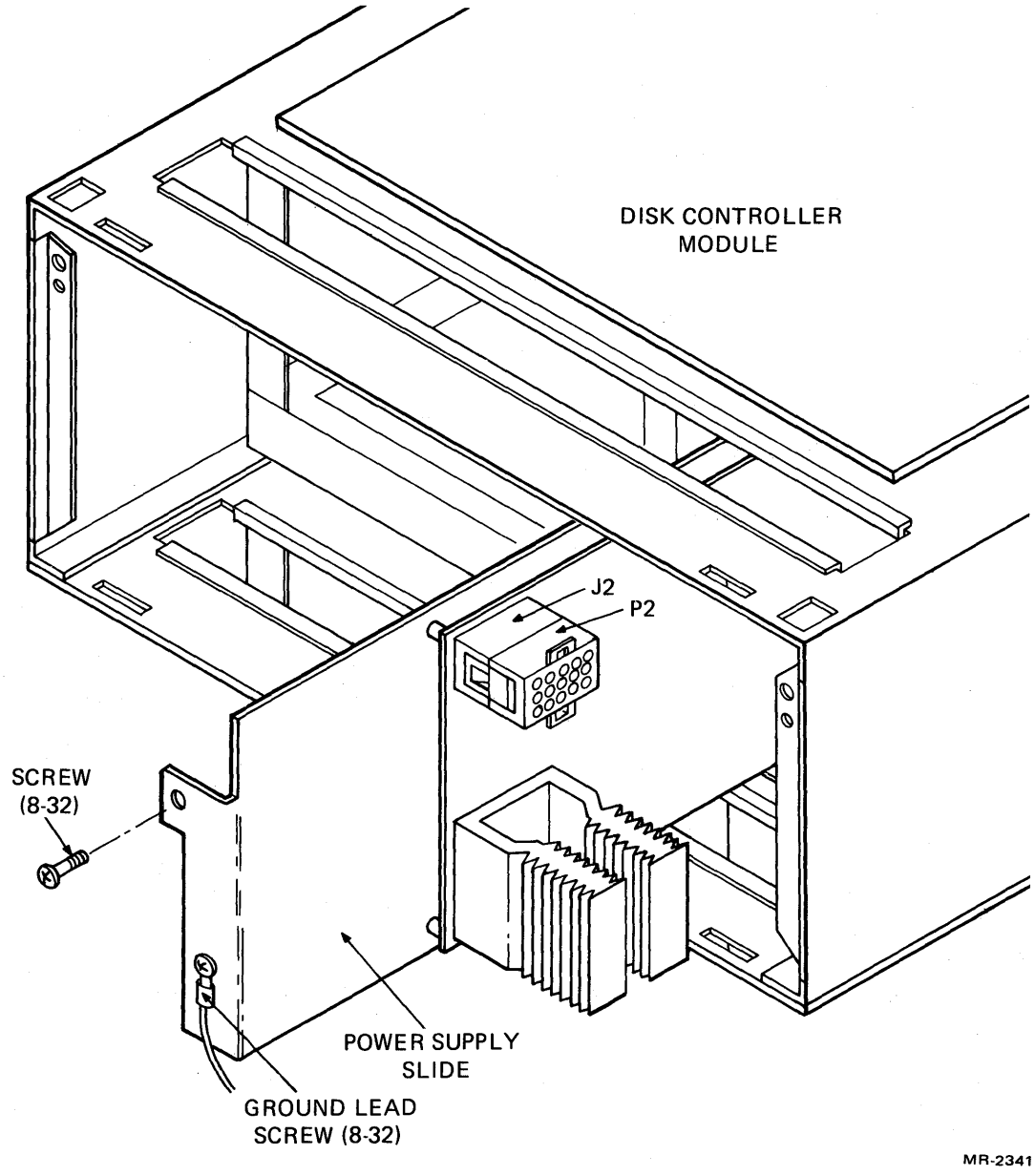


Figure 5-33 Power Supply Assembly, Removal and Replacement

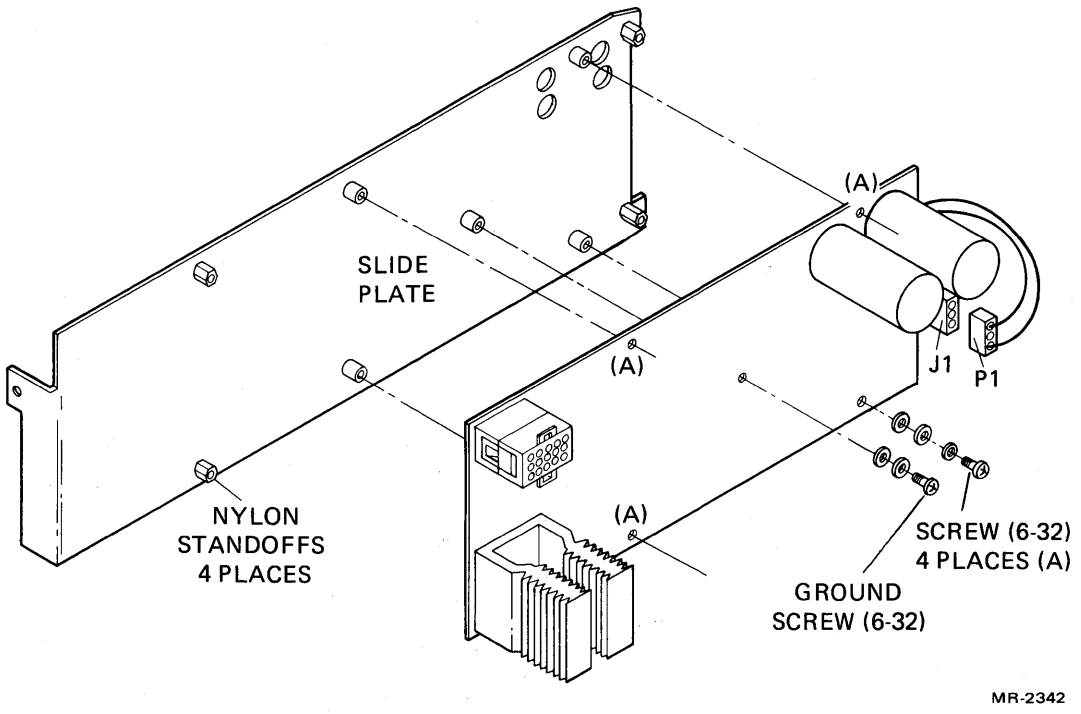


Figure 5-34 Power Supply Module, Removal and Replacement

5.3.11.3 Power Supply Assembly Installation

1. Slide the power supply assembly into the slots provided in the disk drive 0 enclosure. (See Figure 5-33.)

2. Feed the dc power supply cable connectors P1 and P3 up through the slot in the top of the disk drive 0 enclosure and insert them into the connectors as described in steps 5 and 6 of Parargraph 5.3.11.1.

3. Replace the (8-32) screw removed in step 10 of Paragraph 5.3.11.1.

4. Replace the (8-32) screw removed in step 9 of Paragraph 5.3.11.1.

5. Replace the rear panel assembly of disk drive 0 as described in Paragraph 5.3.2.2.

6. Lower the front of the TIM group assembly to the normal position and press the nylon latches previously released in step 2 of Paragraph 5.3.11.1.

7. Replace the top cover assembly as described in Paragraph 5.3.1.2.

5.3.12 Disk Drive 0 Assembly

The disk drive 0 assembly is mounted on the right side of the disk drive 0 enclosure and is removed from the front of the unit. To remove or replace the assembly, perform the following procedures.

5.3.12.1 Disk Drive 0 Assembly Removal

1. Remove the top cover assembly as described in Paragraph 5.3.1.1.

2. Remove the rear panel assembly of the disk drive 0 enclosure as described in Paragraph 5.3.2.1.

3. Remove the rear panel of the disk drive 1 enclosure as described in Paragraph 5.3.3.1.

4. Remove the Disk Controller module as described in Paragraph 5.3.10.1.

5. Route the disk drive 1 cable connectors P3 and P4 down through the hole in the top of the disk drive 0 enclosure and the disk drive 1 enclosure. (See Figure 5-31.)

NOTE
These two cables are routed through the disk drive 0 chassis and must be removed.

6. Disconnect the ground lead that attaches to the rear of disk drive 0 by removing the (6-32) screw. (See Figure 5-35.)

7. Disconnect the ac power cable to disk drive 0 by separating connector J1 from P1.

8. Remove and retain the six (6-32) screws, lockwashers and flat washers used to secure the disk drive 0 assembly to the top of the enclosure. (See Figure 5-36.)

9. Check to ensure all disk drive 0 cables are free, and carefully slide the drive assembly and front bezel forward and clear of the enclosure.

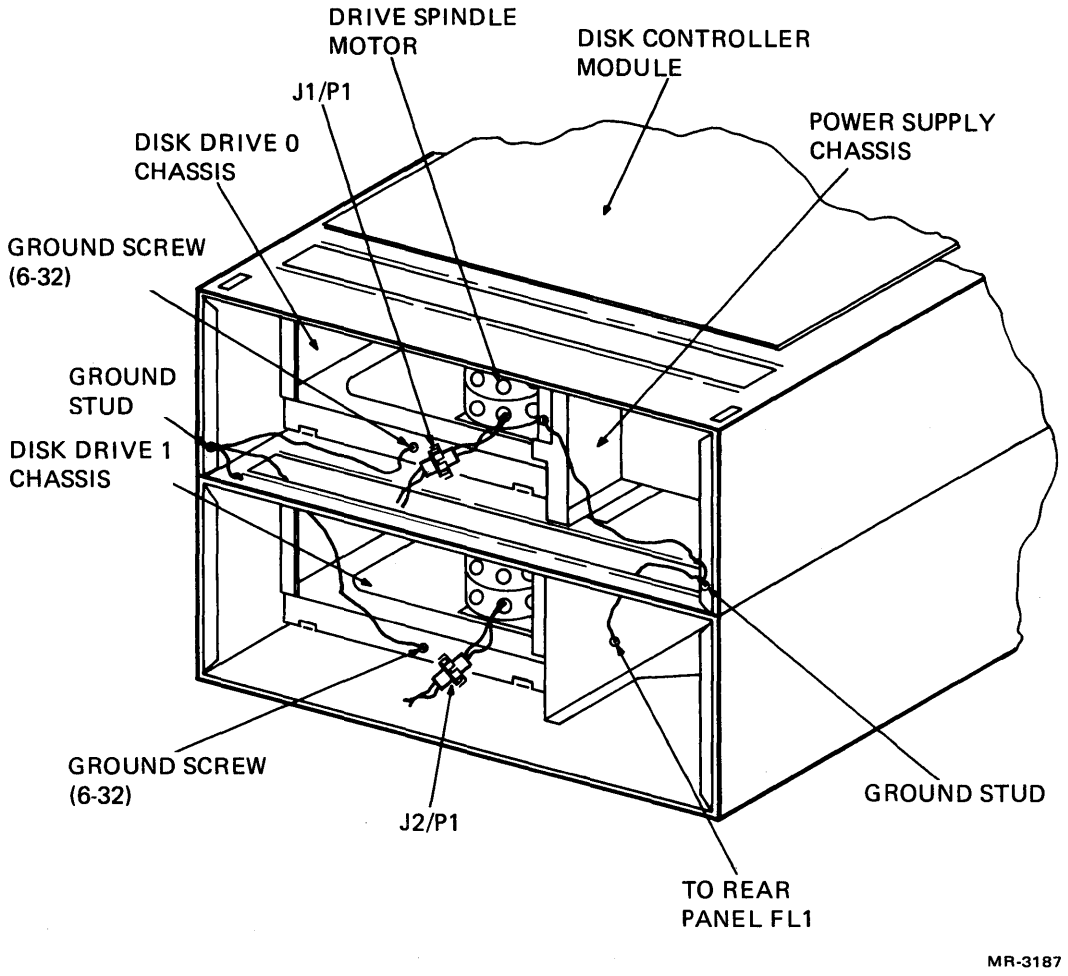


Figure 5-35 Disk Drive Ground Lead and ac Cable Connections

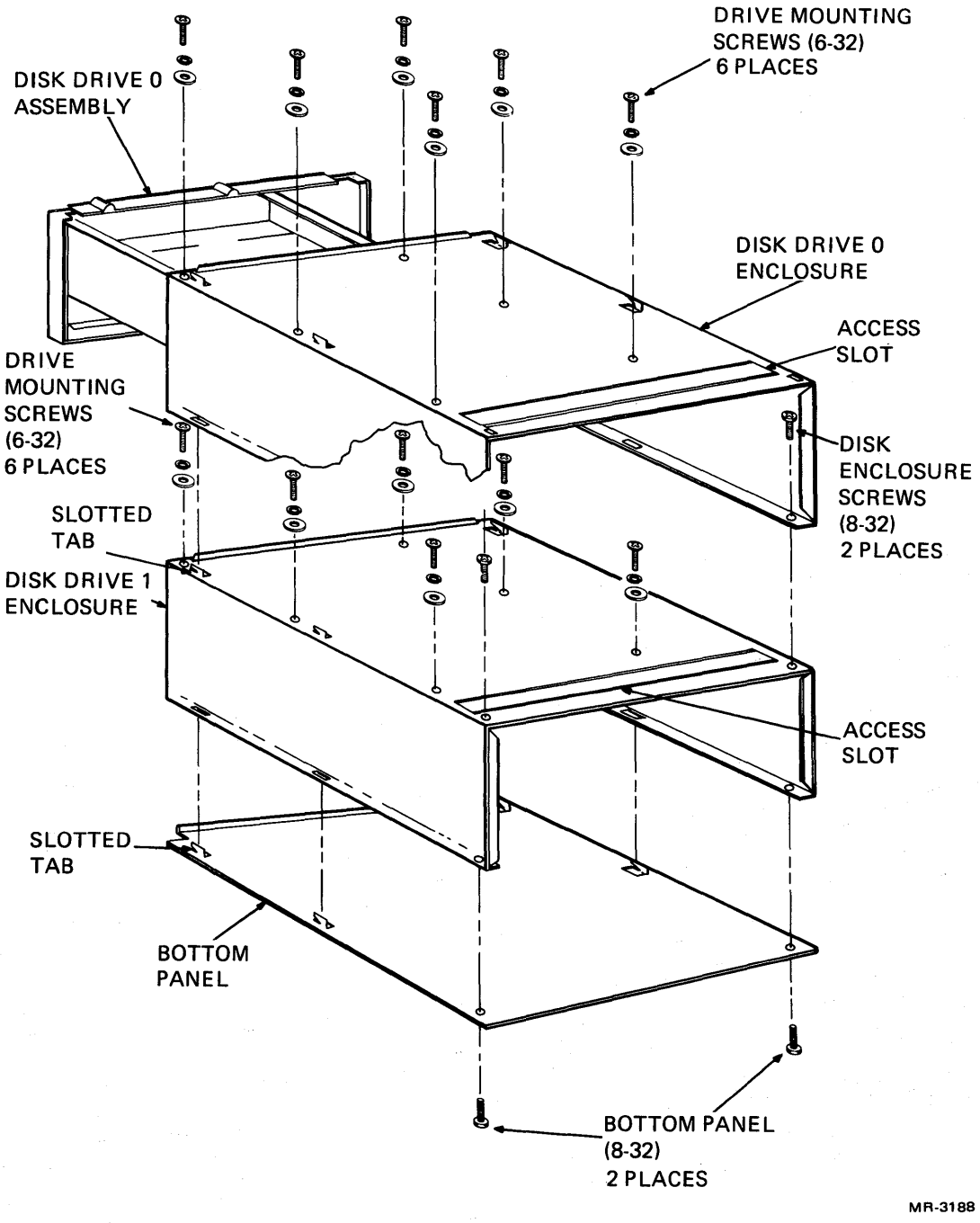


Figure 5-36 Disk Drive and Enclosure Mounting

10. Remove and retain the two metal clips used to secure the top of the bezel to the disk drive 0 assembly. (See Figure 5-37.)

11. Remove and retain the two (6-32) screws, metal washers and kepnuts used to secure the bottom of the disk drive 0 bezel to the disk drive 0 assembly, and remove the bezel.

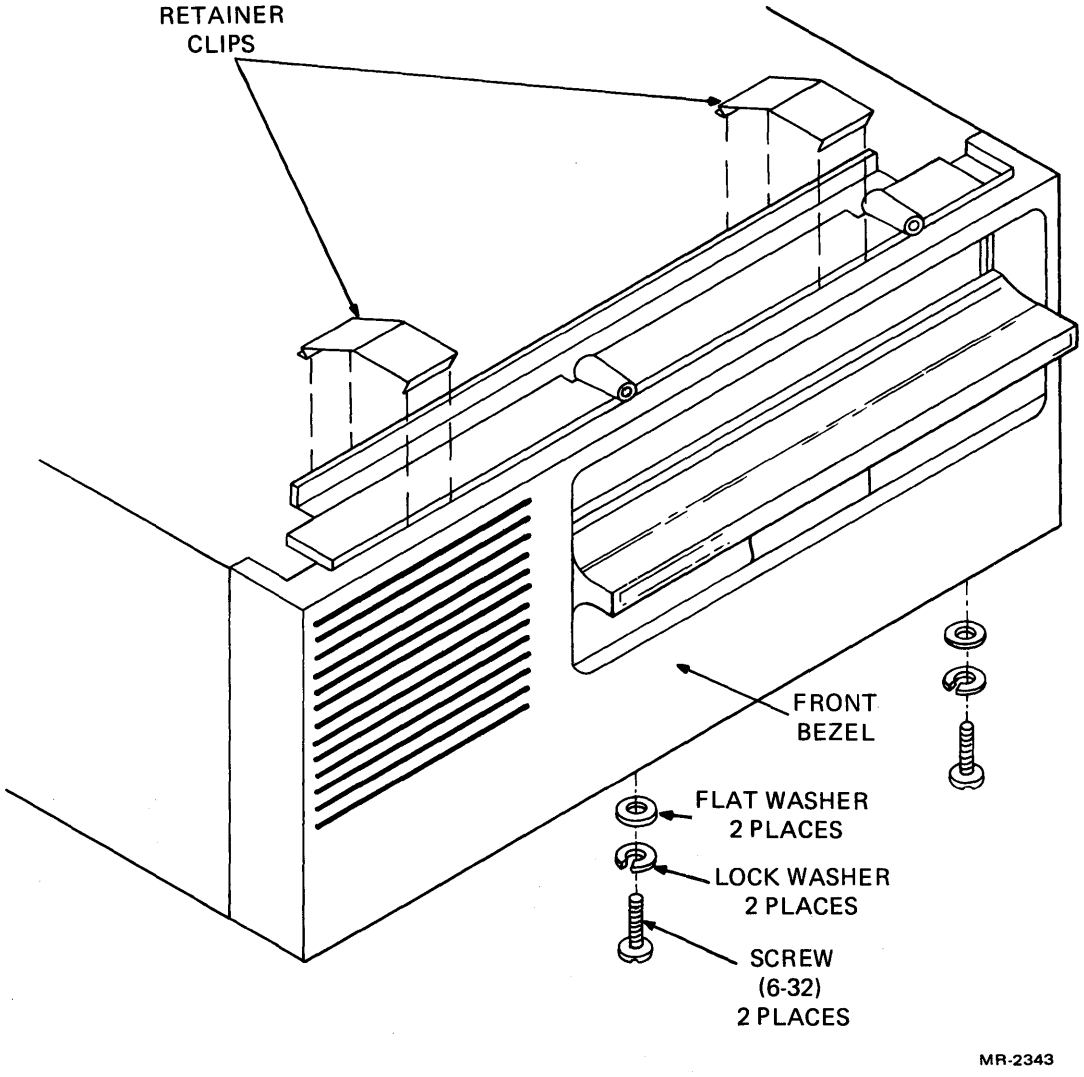


Figure 5-37 Front Bezel, Removal and Replacement

5.3.12.2 Disk Drive 0 Assembly Replacement

1. Mount the bezel to the disk drive 0 assembly using the metal clips and hardware removed in steps 10 and 11 of Paragraph 5.3.12.1.

2. Insert the rear of the disk drive 0 assembly into the enclosure until the six tapped holes in the top edges of the drive chassis are properly aligned with the holes in the enclosure.

3. Replace the mounting hardware removed in step 8 of Paragraph 5.3.12.1.

NOTE
From the rear of the enclosure, hold the disk drive 0 assembly against the top surface of the enclosure before inserting hardware.

4. Connect J1 to P1 on the ac power cable removed in step 7 of Paragraph 5.3.12.1.

5. Route the disk drive 1 cable connectors through the hole in the top of the disk drive 1 enclosure, through the chassis of the disk 0 drive assembly and through the hole in the top of the disk drive 0 enclosure. (See Figure 5-31.)

6. Connect the ground lead removed in step 6 of Paragraph 5.3.12.1.

7. Replace the Disk Controller module as described in Paragraph 5.3.10.2.

8. Replace the rear panel of the disk drive 1 enclosure as described in Paragraph 5.3.3.2.

9. Replace the rear panel assembly of the drive 0 enclosure as described in Paragraph 5.3.2.2.

10. Replace the top cover assembly as described in Paragraph 5.3.1.2.

5.3.13 Disk Drive 1 Assembly

The disk drive 1 assembly is mounted on the right side of the disk drive 1 enclosure and is removed from the front of the unit. To remove or replace the assembly, perform the following procedures.

5.3.13.1 Disk Drive 1 Assembly Removal

1. Remove the top cover assembly as described in Paragraph 5.3.1.1.

2. Remove the rear panel assembly of the disk drive 0 housing as described in Paragraph 5.3.2.1.

3. Remove the rear panel of the drive 1 housing as described in Paragraph 5.3.3.1.

4. Release the left and right hinge brackets of the TIM assembly by pulling up on the nylon latches. (See Figure 5-20.)

5. Raise the TIM assembly to the vertical position. (See Figure 5-22.)

6. Slide the RFI shield slot away from the G1 cable assembly and open the shield to the position shown.

7. Disconnect the disk drive 1 cable connectors P3 and P4 from the Disk Controller module connectors D1P3 and D1P4. (See Figure 5-31.)

8. Release the Disk Controller module from the top of the disk drive 0 enclosure by carefully compressing the nylon standoff tabs while gently lifting the module.

9. Route the P3 and P4 cable connectors down through the slot in the module, through the hole in disk drive 0 enclosure, through the disk drive 0 chassis, and through the hole in the disk drive 1 enclosure.

10. Disconnect the disk drive 0 cable connectors P5, P6, and P7 from the cable extender module located below an access slot at the rear of the drive 1 enclosure.

11. Disconnect the ac power cable to disk drive 1 by separating connector J2 from P1. (See Figure 5-35.)

12. Disconnect the ground lead attached to the disk drive 0 chassis by removing and retaining the (6-32) screw.

13. Using a long shank screwdriver, remove and retain the two (8-32) disk enclosure screws and washers located toward the rear and at each side of the disk drive 0 enclosure. (See Figure 5-36.)

14. Slide the disk drive 0 enclosure forward approximately 1.27 cm (0.5 in) and carefully lift the disk drive 0 enclosure to separate it from the slotted tabs in the disk drive 1 enclosure.

15. Remove and retain the six (6-32) screws, lockwashers, and flat washers used to secure the disk drive 1 assembly to the top of the disk drive 1 enclosure.

16. Check to ensure that all disk drive 1 cables are clear, then carefully slide the disk drive 1 assembly and bezel toward the front of the enclosure and remove.

17. Remove and retain the two metal clips used to secure the top edge of the bezel to the front of the disk drive 1 chassis. (See Figure 5-37.)

18. Remove and retain the two (6-32) screws, metal washers, and kepnuts used to secure the bottom edge of the bezel to the front of the disk drive 1 chassis.

5.3.13.2 Disk Drive 1 Assembly Replacement

1. Mount the bezel to the disk drive 1 assembly using the metal clips and hardware removed in steps 17 and 18 of Paragraph 5.3.13.1.

2. Insert the rear of drive 1 into the enclosure until the six tapped holes in the top edges of the disk drive 1 chassis are properly aligned with the hole in the enclosure.

3. Replace the mounting hardware removed in step 15 of Paragraph 5.3.13.1. Ensure that all cables are properly routed and free from obstructions.

NOTE

From the rear of the enclosure, hold the disk drive 1 chassis against the top surface of the enclosure before inserting the hardware.

4. Position the disk drive 0 enclosure over the drive 1 enclosure so that the tabs in the disk drive 1 enclosure are inserted through the slots in the disk drive 0 enclosure. (See Figure 5-36.)

5. Slide the disk drive 0 enclosure toward the rear of the disk drive 1 enclosure until the tabs engage and the enclosures are properly aligned.

6. Replace the hardware removed in step 13 of Paragraph 5.3.13.1.

7. Route the disk drive 1 cable connectors P3 and P4 through the hole in the disk drive 1 enclosure, through the disk drive 0 chassis, through the hole in the disk drive 0 enclosure and through the slot in the Disk Controller module. (See Figure 5-31.)

8. Press the Disk Controller module down over each standoff until all tabs on the standoffs are firmly engaged.

9. Connect cable connectors P3 and P4 removed in step 7 of Paragraph 5.3.13.1.

10. Connect cable connectors P5, P6 and P7 removed in step 10 of Paragraph 5.3.13.1.

11. Connect J2 to P1 on the ac power cable removed in step 11 of Paragraph 5.3.13.1.

12. Connect the ground lead removed in step 12 of Paragraph 5.3.13.1.

13. Replace the rear panel of the disk drive 1 enclosure as described in Paragraph 5.3.3.2.

14. Check to ensure that all signal cables are routed away from the ac power cables and replace the rear panel assembly of the disk drive 0 enclosure as described in Paragraph 5.3.2.2.

15. Replace the top cover assembly as described in Paragraph 5.3.1.2.

5.4 MODULE AND ASSEMBLY COMPONENT LOCATIONS AND SIGNALS

This paragraph contains the component location diagrams of the logic modules contained in the PDT-11/150 unit. The module diagrams are sectioned into areas to facilitate the location of functions. Also included for each module are tables that describe the signals to the module connectors.

5.4.1 Removable Module ICs

Some of the ICs on the modules are installed in sockets and can be removed and replaced when suspected to be the cause of a failure. Table 5-8 lists the removable ICs and provides the DIGITAL replacement part number or the manufacturer's designations.

5.4.2 Intelligence Module, Functional Layout and Signals

Figure 5-38 shows the IC locations and functional areas on the Intelligence module, and Tables 5-9 through 5-13 list and define the interfacing signals on the etch connectors and cable connector. Refer to Figure 5-14 for the connector pin locations.

5.4.3 RAM Module, Functional Layout and Signals

Figure 5-39 shows the IC locations and functional areas on the RAM module. The module shown is the MST-AB (16K) or MST-AD (60K), each of which contains 32 RAM ICs. Tables 5-14 and 5-15 list and define the interfacing signals on the etch connectors. Refer to Figure 5-15 for the connector pin locations.

5.4.4 Peripheral Module, Functional Layout and Signals

Figure 5-40 shows the IC locations and functional areas on the Peripheral module, and Tables 5-16 through 5-19 list and define the interfacing signals on the etch and cable connectors. The module shown contains the three USARTs for the Cluster EIA option DFT11-AB. Refer to Figure 5-16 for the location of the etch and cable connector pins.

5.4.5 Standard EIA Module, Functional Layout and Signals

Figure 5-41 shows the IC locations and functional areas on the Standard EIA module. Table 5-20 lists and defines the signals on connector J4. Refer to Table 4-12 for the device signals on the 25-pin EIA connectors. Refer to Figure 5-17 for the connector pin locations of J4, and Figure 2-3 for the 25-pin device connectors.

5.4.6 Cluster EIA Module, Functional Layout and Signals

Figure 5-42 shows the IC locations and functional areas on the Cluster EIA module. Table 5-21 lists and defines the signals on connector J4. Refer to Table 4-13 for the 25-pin device connector signals. Refer to Figure 5-17 for the connector pin locations of J4, and Figure 2-3 for the 25-pin device cable connectors.

5.4.7 Disk Controller Module, Functional Layout and Signals

Figure 5-43 shows the IC locations and functional areas on the Disk Controller module, revision K, and Figure 5-44 shows the IC locations and functional areas on the revision L module. Table 5-22 lists and defines the signals on connector J1. Refer to Figure 5-15 for the J1 connector pin locations.

5.4.8 Power Supply Module, Component Layout

Figure 5-45 shows the component layout of the H7833 power supply module. Refer to "DC Power Distribution" below Paragraph 5.2.3 for the input ac voltage to the module and the output dc voltages.

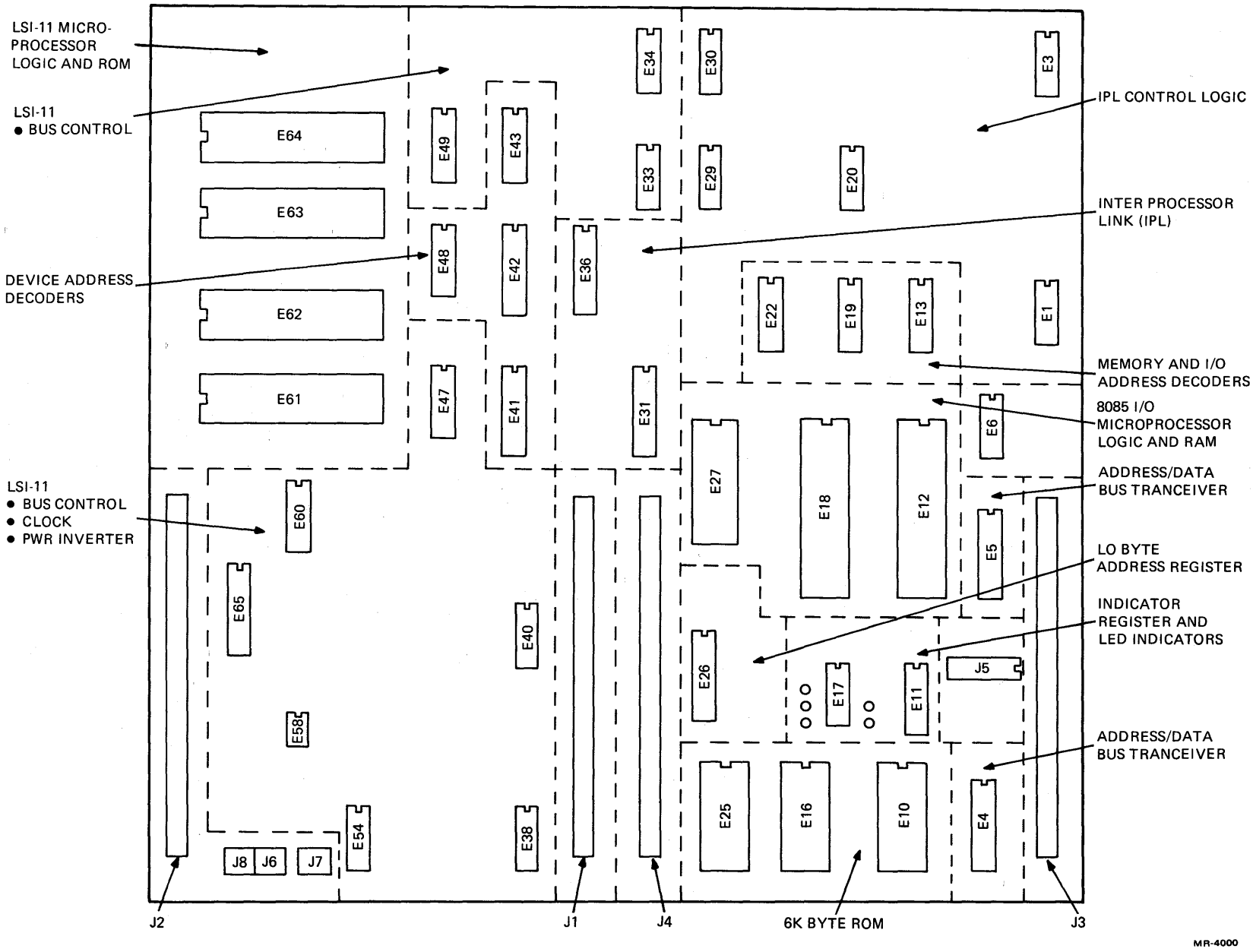


Figure 5-38 Intelligence Module, Functional Layout

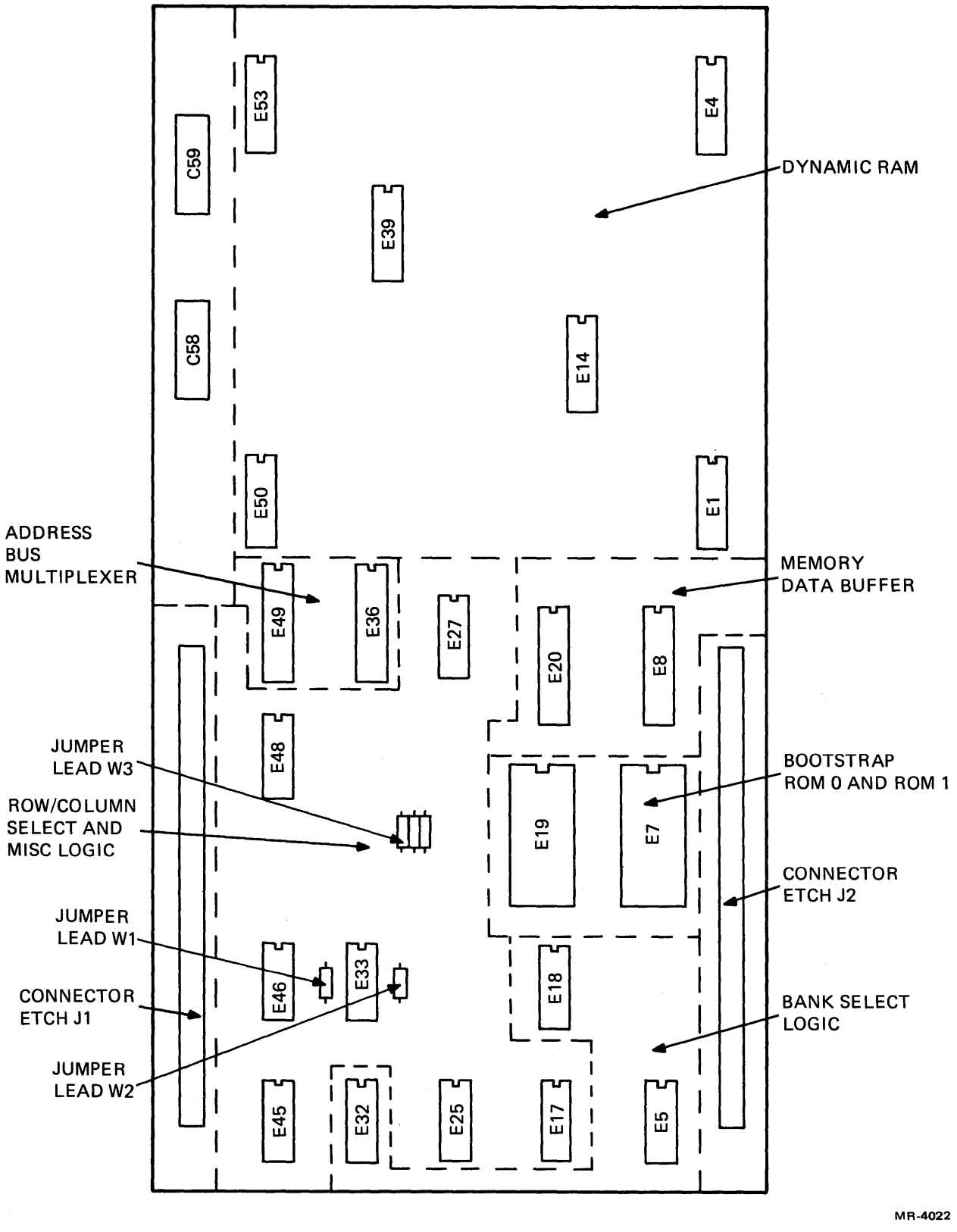


Figure 5-39 RAM Module, Functional Layout

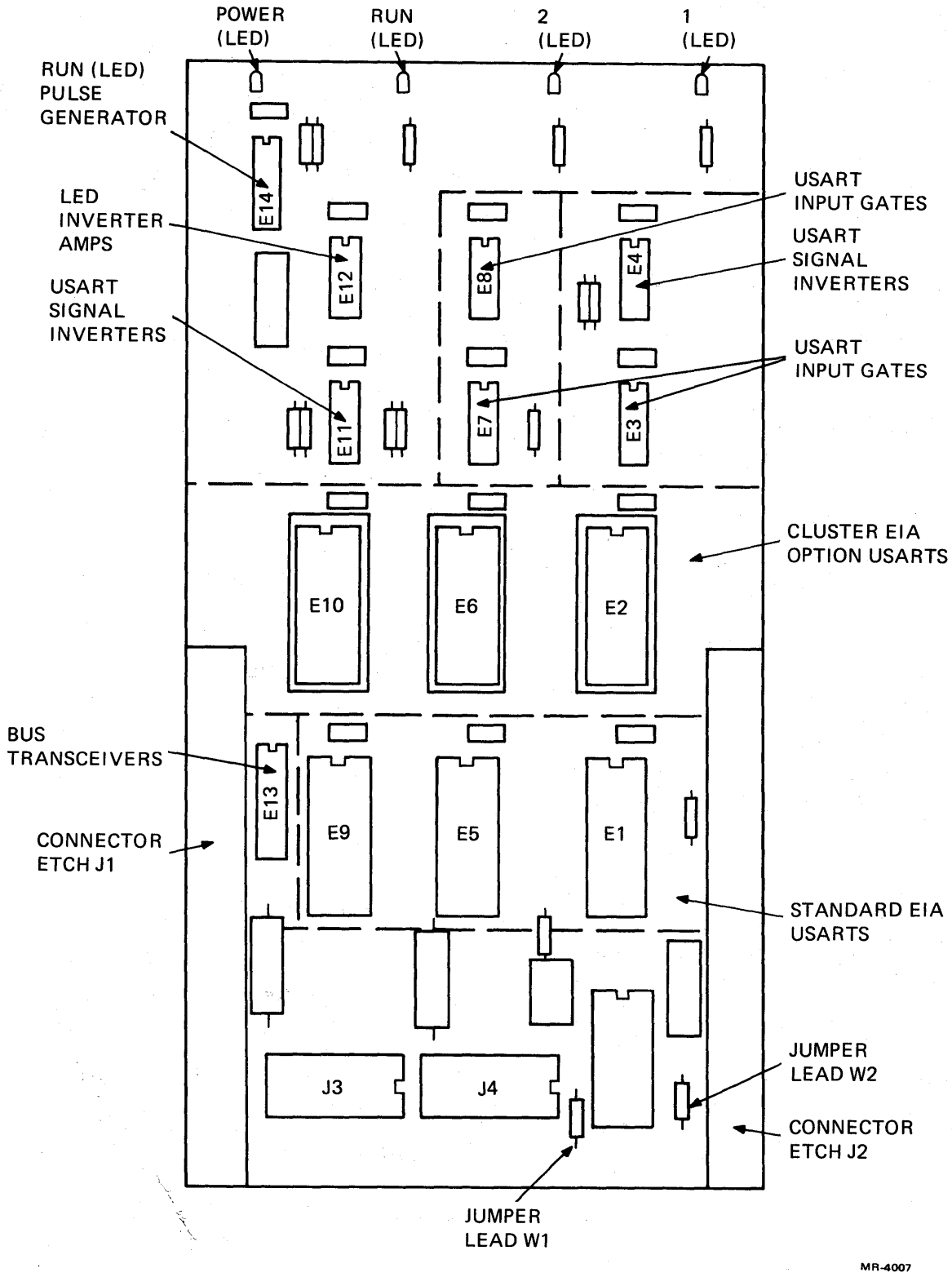


Figure 5-40 Peripheral Module, Functional Layout

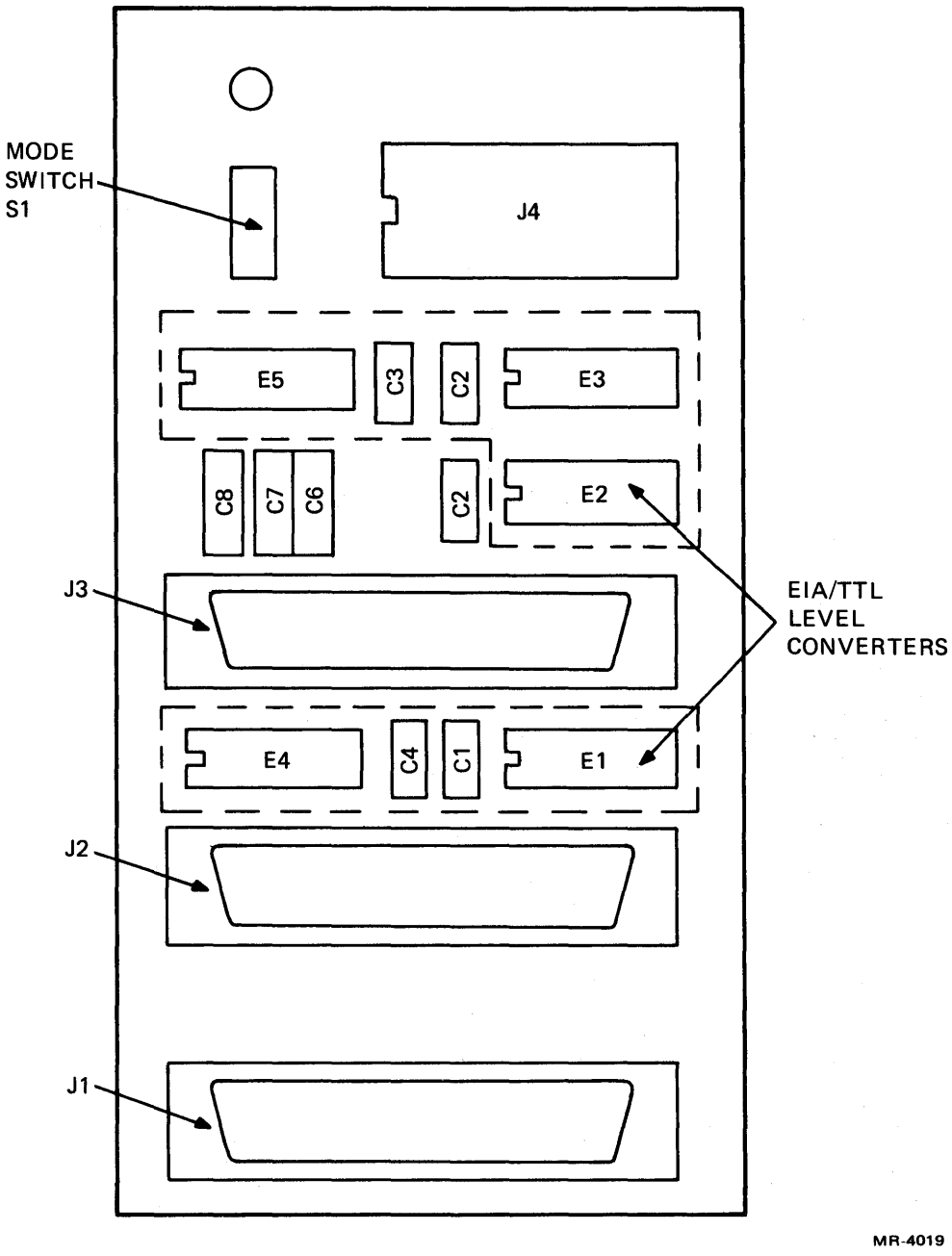


Figure 5-41 Standard EIA Module, Functional Layout

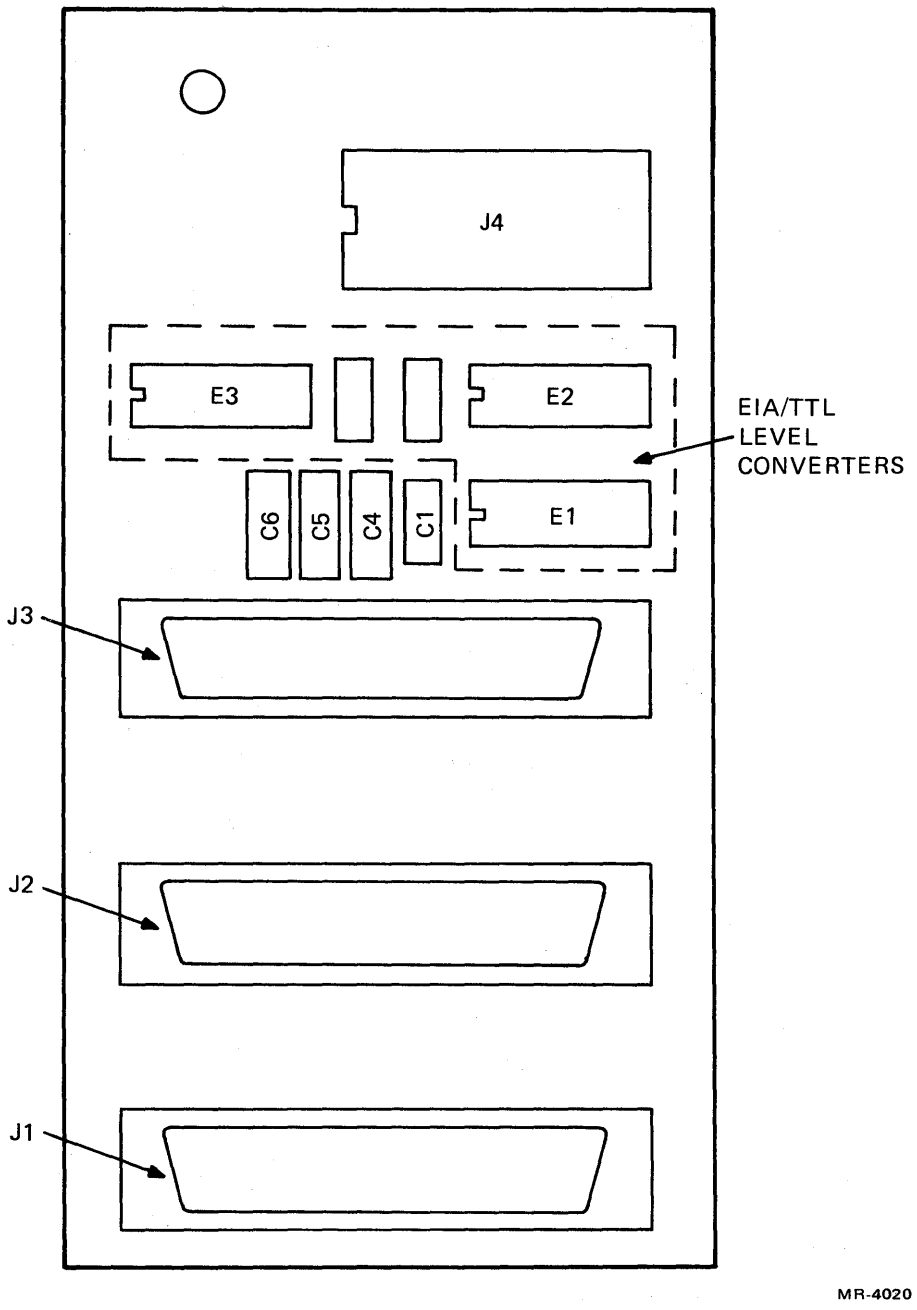


Figure 5-42 Cluster EIA Module, Functional Layout

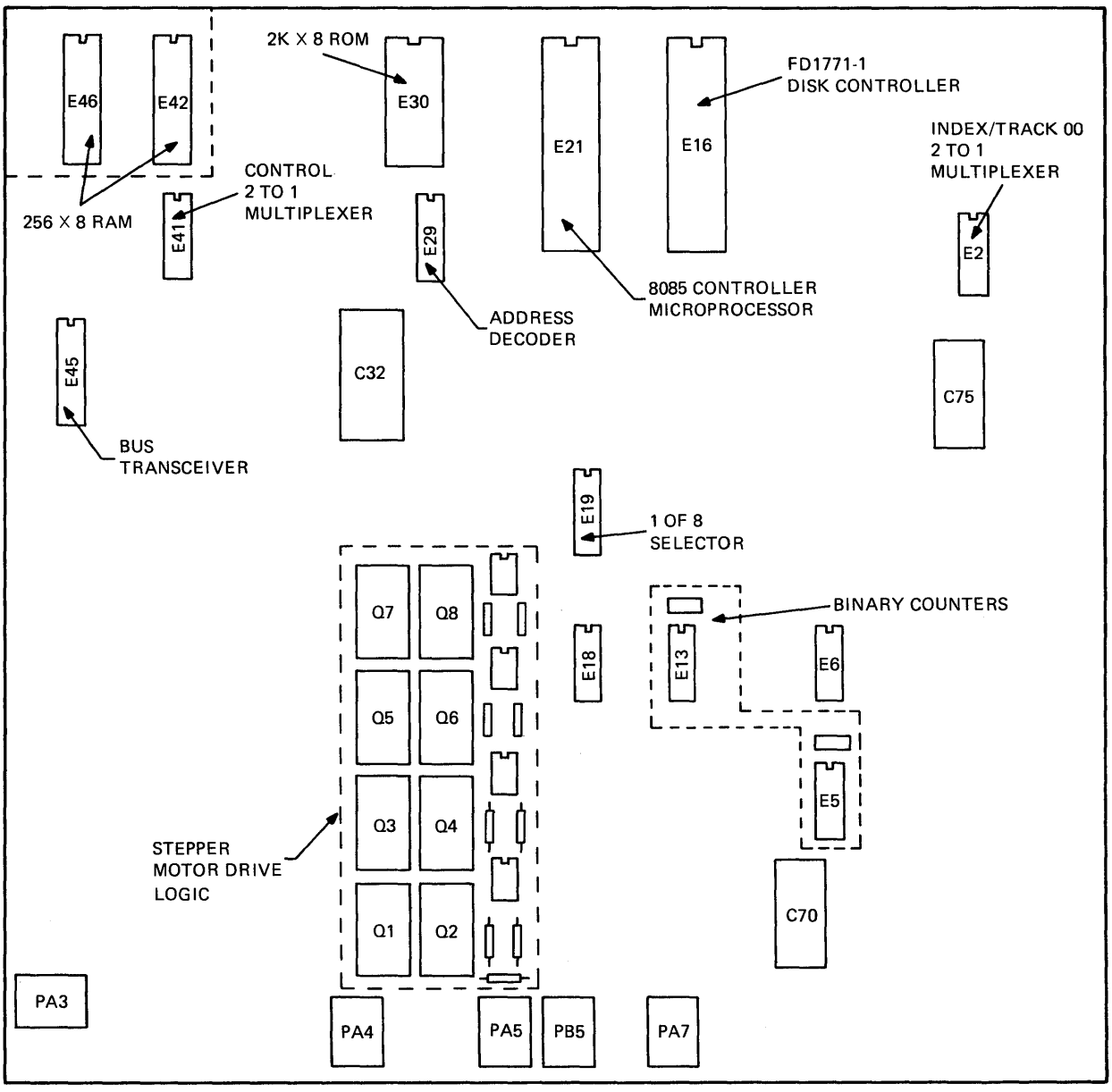


Figure 5-43 Disk Controller Module (Revision K), Functional Layout

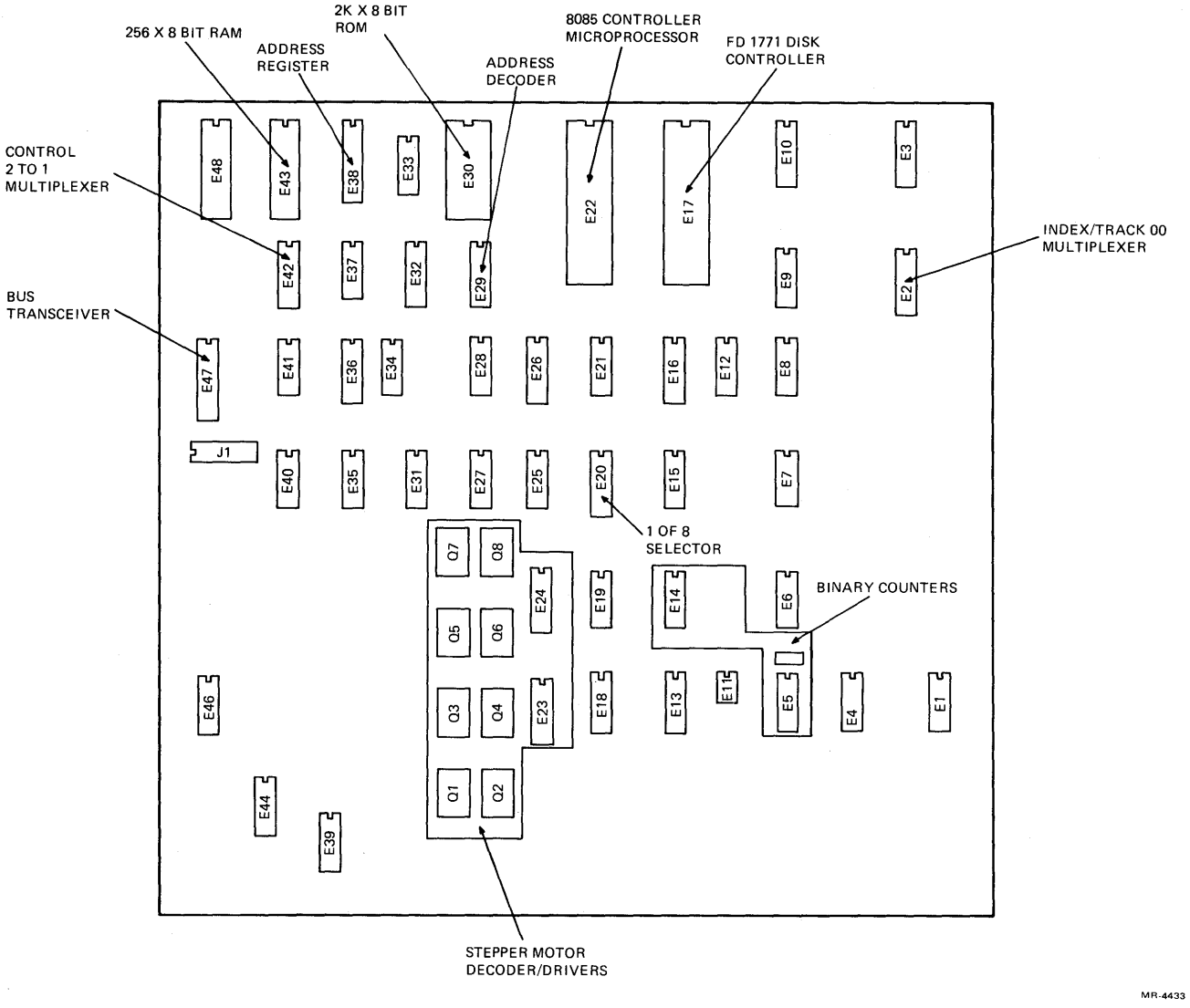


Figure 5-44 Disk Controller Module (Revision L), Functional Layout

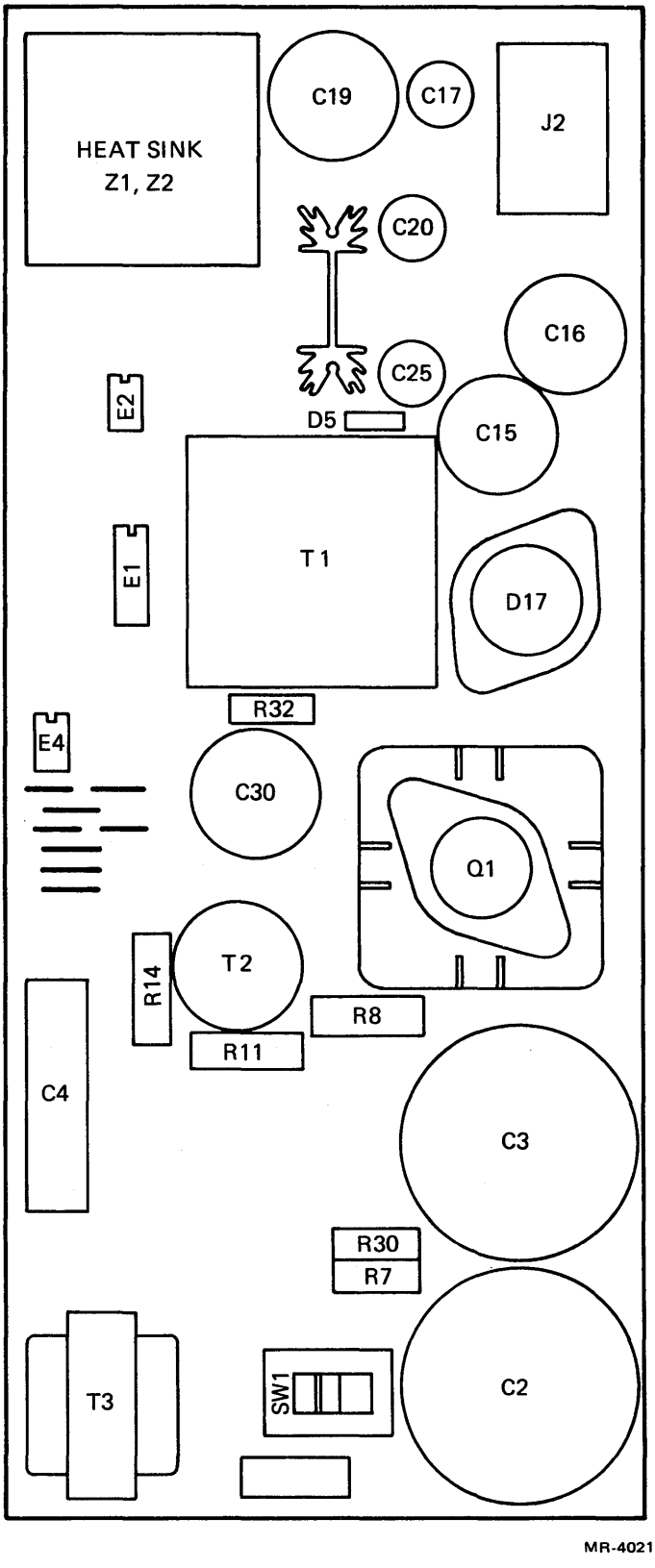


Figure 5-45 Power Supply Module, Component Locations

Table 5-8 Removable Module ICs

Module	Location	Description	DEC Part No.
Intelligence			
I/O Micro-processor	E10	ROM2	23-039E2
	E25	ROM1	23-042E2
	E16	ROM10	23-043E2
	E12	8085*	21-14963-00
	E18	8155*	21-14964-00
LS1-11 Micro-processor	E61	Data	21-1549-01
	E62	Control	23-002C4-00
	E63	Microm 0	23-001B5-00
	E64	Microm 1	23-002B5-00
RAM			
low byte	E7	ROM0	23-032F3
high byte	E19	ROM1	23-033F3
Peripheral			
Terminal No 1	E2		
Terminal No 2	E6	2651 USART**	21-15103
Terminal No 3	E10		
Disk Controller			
Disk Controller	E16 (E17)	FD1771-1	21-15105
Control Microprocessor	E21 (E22)	8085*	21-14963-00
ROM	E30	8316E*	23-040E2-00

Note: Locations in parentheses are for the revision L module.

* Intel type
** Signetics type

Table 5-9 Intelligence Module J1 Connector Signals

Pin	Signal	Description
1		Not used.
2		Not used.
3	FDIN (1) H	A reply to LSI-11 when a fast-data-in cycle is requested.
4	WWB H	Specifies a write byte to RAM memory.
5	MRPLY H	Generated by the RAM module in reply to a valid RAM address.
6		-5 V
7		-5 V
8		-5 V
9		-5 V
10		-5 V
11		Not used.
12	ADR 11 H	See pins 27-34.
13		Not used.
14		Not used.
15	ADR 10 H	See pins 27-34.
16	ADR 09 H	See pins 27-34.
17	ADR 00 H	See pins 27-34.
18		Not used.
19		Not used.
20	DOUT (0) H	Indicates to the RAM module that a write operation is in process and data is available.
21		Not used.
22	REF (0) H	Indicates to the RAM module that the refresh cycle is in process.
23		+5 V
24		+5 V
25		+5 V
26		+5 V
27	ADR 03 H	Latched address information to RAM modules.
28	ADR 02 H	
29	ADR 01 H	
30	ADR 04 H	
31	ADR 03 H	
32	ADR 06 H	
33	ADR 08 H	
34	ADR 07 H	
35		Not used.
36		+12 V
37		+12 V
38		+12 V
39		+12 V
40		+12 V

Table 5-10 Intelligence Module J2 Connector Signals

Pin	Signal	Description
1	WSYNC L	Indicates to the RAM module that the address is available.
2		Not used.
3	ADR 15 H	See pins 27–34, Table 5-9.
4	ADR 14 H	See pins 27–34, Table 5-9.
5	ADR 13 H	See pins 27–34, Table 5-9.
6		Not used.
7		Not used.
8		Not used.
9		Not used.
10		Not used.
11		Logic ground.
12		Logic ground.
13		Logic ground.
14		Logic ground.
15		Logic ground.
16		Not used.
17		Not used.
18		Not used.
19		Not used.
20	WDIN L	Indicates to the RAM module that the LSI-11 is ready to accept data.
21		Not used.
22	ADR 12 H	See pins 27–34, Table 5-9.
23		Not used.
24		Not used.
25	BWDAL 00 H	Additionally buffered address and data information to the RAM module.
26	BWDAL 01 H	Additionally buffered address and data information to the RAM module.
27	BWDAL 02 H	Additionally buffered address and data information to the RAM module.
28	BWDAL 03 H	Additionally buffered address and data information to the RAM module.
29	WDAL 04 H	} Buffered address and data information to the RAM module.
30	WDAL 05 H	
31	WDAL 06 H	
32	WDAL 07 H	
33	WDAL 08 H	
34	WDAL 09 H	
35	WDAL 10 H	
36	WDAL 11 H	
37	WDAL 12 H	
38	WDAL 13 H	
39	WDAL 14 H	
40	WDAL 15 H	

Table 5-11 Intelligence Module J3 Connector Signals

Pin	Signal	Description
1	PB6	The modem ring signal from the Peripheral module.
2	PB2	The modem secondary carrier-detect signal.
3	PB3	The modem data-set-ready signal from the Peripheral module.
4	PB4	The modem carrier-detect signal from the Peripheral module.
5	PB5	The modem primary clear-to-send signal from the Peripheral module.
6		Not used.
7	BLANK 1 H	Selects transfer director of the data bus.
8		Not used.
9		Not used.
10		Not used.
11		Not used.
12		Not used.
13		Logic ground.
14		Logic ground.
15		Logic ground.
16		Logic ground.
17		+5 V
18		+5 V
19		+5 V
20		+5 V
21	HDBAD 0 H	See pins 27–32.
22	HDBAD 1 H	See pins 27–32.
23	TIM FD SEL L	Selects transfer director of the data bus.
24	A 10 H	Address bits used to select the USART register on the Peripheral module.

Table 5-11 Intelligence Module J3 Connector Signals (Cont.)

Pin	Signal	Description
25	A 8 H	Address bits used to select the USART register on the Peripheral module.
26	A 9 H	Address bits used to select the USART register on the Peripheral module.
27	HDBAD7 H	Bidirectional data bus between the Peripheral module and Intelligence module.
28	HDBAD6 H	Bidirectional data bus between the Peripheral module and Intelligence module.
29	HDBAD5 H	Bidirectional data bus between the Peripheral module and Intelligence module.
30	HDBAD4 H	Bidirectional data bus between the Peripheral module and Intelligence module.
31	HDBAD3 H	Bidirectional data bus between the Peripheral module and Intelligence module.
32	HDBAD2 H	Bidirectional data bus between the Peripheral module and Intelligence module.
33		Not used.
34		Not used.
35	PDA H	Indicates the status of the receiver data holding register of the printer USART.
36	PTBMT H	Indicates the status of the transmit data holding register of the printer USART.
37	CDA H	Indicates the status of the receiver data holding register of the modem USART.
38	HALT H	Console data-terminal-ready signal.
39	TDA H	Indicates the status of the receiver holding register of the console USART.
40	IF CLR L	Controls the RUN indicator on the Peripheral module.

Table 5-12 Intelligence Module J4 Connector Signals

Pin	Signal	Description
1	FPRESET L	Reset signal from the S1 mode switch on the Standard EIA module.
2	REF EN L	RAM refresh signal from function switch S1-3 on the Peripheral module.
3		-5 V
4		-5 V
5		-5 V
6	LTC EN L	Line time clock enable signal from function switch S1-2 on the Peripheral module.
7	I/O 10 L	Not used.
8		+12 V
9		+12 V
10		+12 V
11	BTEST L	Indicates the self-test status of mode switch S1 through function switch S1-4 on the Peripheral module.
12		Not used.
13		Not used.
14		Not used.
15		Not used.
16	TS DAT 1 H	Not used.
17		Not used.
18	UART CLK	19.8K Hz square wave signal to the W2 jumper on the Peripheral module.
19		Not used.
20		Not used.
21		Not used.
22		Not used.
23	BRCLK	5.0688 MHz square wave to USARTs on the Peripheral module.

Table 5-12 Intelligence Module J4 Connector Signals (Cont.)

Pin	Signal	Description
24	INIT H	Reset signal to the Peripheral module when ac power is applied or a reset is selected on the mode switch.
25		Not used.
26		Not used.
27		Not used.
28		Not used.
29		Not used.
30	I/O 3 L	Enables the modem USART on the Peripheral module.
31	I/O 4 L	Enables the printer USART on the Peripheral module.
32	I/O 2 L	Enables the console USART on the Peripheral module.
33	WR L	Write signal from the 8085 I/O microprocessor.
34	RD L	Read signal from the 8085 I/O microprocessor.
35	I/O 13 L	Enables terminal no. 1 USART on the Peripheral module.
36	I/O 14 L	Enables terminal no. 3 USART on the Peripheral module.
37	I/O 12 L	Enables terminal no. 2 USART on the Peripheral module.
38		Not used.
39	CTBMT H	Transmit data holding register of the modem USART.
40	TTBMT H	Indicates the status of the transmit data holding register of the console USART.

Table 5-13 Intelligence Module J5 Connector Signals

Pin	Signal	Description
1	TIM GO H	Interrupt request to the 8085 controller microprocessor.
2	HD BAD3 H	Bidirectional data bus between the Disk Controller module and the Intelligence module.
3	HD BAD5 H	Bidirectional data bus between the Disk Controller module and the Intelligence module.
4	HD BAD7 H	Bidirectional data bus between the Disk Controller module and the Intelligence module.
5	HD BAD1 H	Bidirectional data bus between the Disk Controller module and the Intelligence module.
6	UB RD L	Read command from the 8085 I/O microprocessor.
7	UB WR L	Write command from the 8085 I/O microprocessor.
8	DONE H	Halt condition of the 8085 controller microprocessor.
9		Logic ground.
10	TIM FD SEL L	Memory select input from the Intelligence module.
11	HD BAD O H	See pins 2–5.
12	HD BAD 2 H	See pins 2–5.
13	HD BAD 6 H	See pins 2–5.
14	HD BAD 4 L	See pins 2–5.
15	TIM ALE H	Address latch from the 8085 I/O microprocessor.
16	BTEST L	Indicates the self-test status of mode switch S1 through function switch S1-4.

Table 5-14 RAM Module J1 Connector Signals

Pin	Signal	Description
1		Not used.
2		Not used.
3	FDIN(1)H	Provides a reply to the LSI-11 when a fast-data-in cycle is requested.
4	WWB H	Specifies a word or byte to RAM memory.
5	MRPLY H	Generated by the RAM module in reply to a valid RAM address.
6		-5 V
7		-5 V
8		-5 V
9		-5 V
10		-5 V
11		-5 V
12	ADR 11 H	See pins 27–34.
13		Not used.
14		Not used.
15	ADR 10 H	See pins 27–34.
16	ADR 09 H	See pins 27–34.
17	ADR 00 H	See pins 27–34.
18		Not used.
19		Not used.
20	DOUT (0) H	Indicates to the RAM module that a write operation is in process and data is available.

Table 5-14 RAM Module J1 Connector Signals (Cont.)

Pin	Signal	Description
21		Not used.
22	REF (0) H	Indicates to the RAM module that the refresh cycle is in process.
23		+5 V
24		+5 V
25		+5 V
26		+5 V
27	ADR 03 H	Latched address information to the RAM module.
28	ADR 02 H	
29	ADR 01 H	
30	ADR 04 H	
31	ADR 03 H	
32	ADR 06 H	
33	ADR 06 H	
34	ADR 07 H	
35		Not used.
36		+12 V
37		+12 V
38		+12 V
39		+12 V
40		+12 V

Table 5-15 RAM Module J2 Connector Signals

Pin	Signal	Description
1	WSYNC L	Indicates to RAM the module that an address is available.
2		Not used.
3	ADR 15 H	See pins 27–34, Table 5-14.
4	ADR 14 H	See pins 27–34, Table 5-14.
5	ADR 13 H	See pins 27–34, Table 5-14.
6		Not used.
7		Not used.
8		Not used.
9		Not used.
10		Not used.
11		Logic ground.
12		Logic ground.
13		Logic ground.
14		Logic ground.
15		Logic ground.
16		Not used.
17		Not used.
18		Not used.
19		Not used.
20	WDIN L	Indicates to the RAM module that the LSI-11 is ready to accept data.
21		Not used.
22	ADR 12 H	See pins 27–34, Table 5-14.
23		Not used.
24		Not used.
25	BWDAL 00 H	Additionally buffered address and data information to the RAM module.
26	BWDAL 01 H	Additionally buffered address and data information to the RAM module.
27	BWDAL 02 H	Additionally buffered address and data information to the RAM module.
28	BWDAL 03 H	Additionally buffered address and data information to the RAM module.
29	WDAL 04 H	Buffered address and data information to the RAM module.
30	WDAL 05 H	
31	WDAL 06 H	
32	WDAL 07 H	
33	WDAL 08 H	
34	WDAL 09 H	
35	WDAL 10 H	
36	WDAL 11 H	
37	WDAL 12 H	
38	WDAL 13 H	
39	WDAL 14 H	
40	WDAL 154 H	

Table 5-16 Peripheral Module J1 Connector Signals

Pin	Signal	Description
1	PB6	The modem ring signal from the Peripheral module.
2	PB2	The modem secondary carrier-detect signal from the Peripheral module.
3	PB3	The modem data-set-ready signal from the Peripheral module.
4	PB4	The modem carrier-detect signal from the Peripheral module.
5	PB5	The modem primary clear-to-send from the Peripheral module.
6		Not used.
7	BLANK 1 H	Selects transfer director of the data bus.
8		Not used.
9		Not used.
10		Not used.
11		Not used.
12		Not used.
13		Logic ground.
14		Logic ground.
15		Logic ground.
16		Logic ground.
17		+5 V
18		+5 V
19		+5 V
20		+5 V
21	HDBAD 0 H	See pins 27–32.
22	HDBAD 1 H	See pins 27–32.
23	TIM FD SEL L	Selects transfer director of the data bus.
24	A 10 H	Address bits used to select the USART register on the Peripheral module.
25	A 8 H	Address bits used to select the USART register on the Peripheral module.

Table 5-16 Peripheral Module J1 Connector Signals (Cont.)

Pin	Signal	Description
26	A 9 H	Address bits used to select the USART register on the Peripheral module.
27	HDBAD 7 H	Bidirectional data bus between the Peripheral module and Intelligence module.
28	HDBAD 6 H	Bidirectional data bus between the Peripheral module and Intelligence module.
29	HDBAD 5 H	Bidirectional data bus between the Peripheral module and Intelligence module.
30	HDBAD 4 H	Bidirectional data bus between the Peripheral module and Intelligence module.
31	HDBAD 3 H	Bidirectional data bus between the Peripheral module and Intelligence module.
32	HDBAD 2 H	Bidirectional data bus between the Peripheral module and Intelligence module.
33		Not used.
34		Not used.
35	PDA H	Indicates the status of the receiver data holding register of the printer USART.
36	PTBMT H	Indicates the status of the transmit data holding register of the printer USART.
37	CDA H	Indicates the status of the receiver data holding register of the modem USART.
38	HALT H	Console data-terminal-ready signal.
39	TDA H	Indicates the status of the receiver holding register of the console USART.
40	IFCLR L	Control-the RUN indicator on the Peripheral module.

Table 5-17 Peripheral Module J2 Connector Signals

Pin	Signal	Description
1	FPRESET L	Reset signal from the S1 mode switch on the Standard EIA module.
2	REF EN L	RAM refresh signal from function switch S1-3 on the Peripheral module.
3		-5 V
4		-5 V
5		-5 V
6	LT CEN L	Line time clock enable signal from function switch S1-2 on the Peripheral module.
7	I/O 10 L	Not used.
8		+12 V
9		+12 V
10		+12 V
11	BTEST 6	Indicates the self-test status of mode switch S1 through function switch S1-4.
12		Not used.
13		Not used.
14		Not used.
15		Not used.
16	TSTDAT1 H	Not used.
17		Not used.
18	UART CLK	19.8 KHz square wave signal to the W2 jumper on the Peripheral module.
19		Not used.

Table 5-17 Peripheral Module J2 Connector Signals (Cont.)

Pin	Signal	Description
20		Not used.
21		Not used.
22		Not used.
23	BRCLK	5.06 MHz square wave to the USARTs on the Peripheral module.
24	INIT H	Reset signal to the Peripheral module when ac power is applied or a reset is selected on the mode switch.
25		Not used.
26		Not used.
27		Not used.
28		Not used.
29		Not used.
30	I/O 3 L	Enables the modem USART on the Peripheral module.
31	I/O 4 L	Enables the printer USART on the Peripheral module.
32	I/O 2 L	Enables the console USART on the Peripheral module.
33	WR L	Write signal from the 8085 I/O microprocessor.
34	RD L	Read signal from the 8085 I/O microprocessor.
35	I/O 13 L	Enables terminal no. 1 USART on the Peripheral module.
36	I/O 14 L	Enables terminal no. 3 USART on the Peripheral module.
37	I/O 12 L	Enables terminal no. 2 USART on the Peripheral module.
38		Not used.
39	CTBMT H	Transmit data holding register of the modem USART.
40	TTBMT H	Indicates the status of the transmit data holding register of the console USART.

Table 5-18 Peripheral Module J3 Connector Signals

Pin	Signal	Description
1	T1SDATO	Serial data output to terminal no. 1 from the terminal no. 1 USART.
2	T1DTR	Status input of clear-to-send from terminal no. 1.
3	T1SDATI	Serial data input to the terminal no. 1 USART from terminal no. 1.
4		Not used.
5	T2SDATO	Serial data output to terminal no. 2 from the terminal no. 2 USART.
6	T2DTR	Status input of clear-to-send from terminal no. 2.
7	T25DATI	Serial data input to the terminal no. 2 USART from terminal no. 2.
8		Not used.
9	T2SDATO	Serial data output to terminal no. 3 from the terminal no. 3 USART.
10		Not used.
11	T2SDATI	Serial data input to the terminal no. 3 USART from terminal no. 3.
12		Not used.
13		Not used.
14		Not used.
15		Not used.
16		Not used.
17		Not used.
18		Logic ground.
19		Not used.
20		+12 V
21		Not used.
22		-5 V
23	T3DTR	Status input of clear-to-send from terminal no. 3.
24		+5 V

Table 5-19 Peripheral Module J4 Connector Signals

Pin	Signal	Description
1	TSDATO	Serial data output from the console USART.
2	T0DTR	Indicates the status of the clear-to-send from the console terminal.
3	TSDATI	Serial data input to the console USART from the console terminal.
4	CDTR	Output indicating USART ready status.
5	LPSDATO	Serial data output from the printer USART.
6	LPSDTR	Input from the printer indicating the terminal is ready.
7	LPSDATI	Serial data input from the printer terminal.
8	CRTS	Request-to-send output from the modem USART.
9	CSDATO	Serial data output from the modem USART.
10	TRTS	Request-to-send output from the console USART.
11	CSDATI	Serial data input to the modem USART.
12		Logic ground.
13	PB2	Secondary carrier-detect signal from the modem.
14	PB3	Data-set-ready signal from the modem.
15	PB4	Carrier-detect signal from the modem.
16	PB5	Primary clear-to-send signal from the modem.
17	PB6	Ring signal from the modem.
18	TESTL	Self-test signal from the mode switch S1.
19	CSYNC CLK T	Input from the modem for synchronous transmit communication.
20		+12 V
21	CSYNC CLK R	Input from the modem for synchronous receive communications.
22		-5 V
23	FPRESET L	Reset signal from the S1 mode switch on the Standard EIA module.
24	UART CLK	19.8K Hz through jumper W1 or +5 V through jumper W2 to the Standard EIA module.

Table 5-20 Standard EIA Module J4 Connector Signals

Pin	Signal	Description
1	TSDATO	Serial data output from the console USART.
2	T0DTR	Indicates the status of the clear-to-send from the console terminal.
3	TSDATI	Serial data input to the console USART from the console terminal.
4	CDTR	Output indicating USART ready status.
5	LPSDATO	Serial data output from the printer USART.
6	LPSDTR	Input from the printer indicating the terminal is ready.
7	LPSDATI	Serial data input from the printer terminal.
8	CRTS	Request-to-send output from the modem USART.
9	CSDATO	Serial data output from the modem USART.
10	TRTS	Request-to-send output from the console USART.
11	CSDATI	Serial data input to the modem USART.
12		Logic ground.
13	PB2	Secondary carrier-detect signal from the modem.
14	PB3	Data-set-ready signal from the modem.
15	PB4	Carrier-detect signal from the modem.
16	PB5	Primary clear-to-send signal from the modem.
17	PB6	Ring signal from the modem.
18	TESTL	Self-test signal from the mode switch S1.
19	CSYNC CLK T	Input from the modem for synchronous transmit communication.
20		+12 V
21	CSYNC CLK R	Input from the modem for synchronous receive communications.
22		-5 V
23	FPRESET L	Reset signal from the S1 mode switch on the Standard EIA module.
24	UART CLK	19.8 KHz through jumper W1 or +5 V through jumper W2 to the Standard EIA module.

Table 5-21 Cluster EIA Module J4 Connector Signals

Pin	Signal	Description
1	T1SDATO	Serial data output to terminal no. 1 from the terminal no. 1 USART.
2	T1DTR	Status input of clear-to-send from terminal no. 1.
3	T1SDATI	Serial data input to the terminal no. 1 USART from terminal no. 1.
4		Not used.
5	T2SDATO	Serial data output to terminal no. 2 from the terminal no. 2 USART.
6	T2DTR	Status input of clear-to-send from terminal no. 2.
7	T25DATI	Serial data input to the terminal no. 2 USART from terminal no. 2.
8		Not used.
9	T2SDATO	Serial data output to terminal no. 3 from the terminal no. 3 USART.
10		Not used.
11	T2SDATI	Serial data input to the terminal no. 3 USART from terminal no. 3.
12		Not used.
13		Not used.
14		Not used.
15		Not used.
16		Not used.
17		Not used.
18		Logic ground.
19		Not used.
20		+12 V
21		Not used.
22		-5 V
23	T3DTR	Status input of clear-to-send from terminal no. 3.
24		+5 V

Table 5-22 Disk Controller Module J1 Connector Signals

Pin	Signal	Description
1	TIM GO H	Interrupt request to the 8085 controller microprocessor.
2	HDBAD 3 H	Bidirectional data bus between the Disk Controller module and the Intelligence Module.
3	HDBAD 5 H	Bidirectional data bus between the Disk Controller module and the Intelligence Module.
4	HDBAD 7 H	Bidirectional data bus between the Disk Controller module and the Intelligence Module.
5	HDBAD 1 H	Bidirectional data bus between the Disk Controller module and the Intelligence Module.
6	UB RD L	Read command from the 8085 I/O microprocessor.
7	UB WR L	Write command from the 8085 I/O microprocessor.
8	DONE H	Halt condition of the 8085 controller microprocessor.
9		Logic ground.
10	TIM FD SEL L	Memory select input from the Intelligence module.
11	HDBAD O H	See pins 2–5.
12	HDBAD 2 H	See pins 2–5.
13	HDBAD 6 H	See pins 2–5.
14	HDBAD 4 L	See pins 2–5.
15	TIM ALE H	Address latch from the 8085 I/O microprocessor.
16	BTEST L	Indicates the self-test status of mode switch S1 through function switch S1-4.

5.5 DISK DRIVE ASSEMBLY, FUNCTIONS AND ADJUSTMENTS

The main mechanical and electrical components of the disk drive assembly are shown in Figure 5-46. Figure 5-47 is the internal wiring diagram of the assembly.

5.5.1 Mechanical Functions

The disk drive assembly consists of four mechanical functions:

1. Spindle rotation,
2. Flexible disk spindle engagement,
3. Read/Write head positioning,
4. Read/Write head loading.

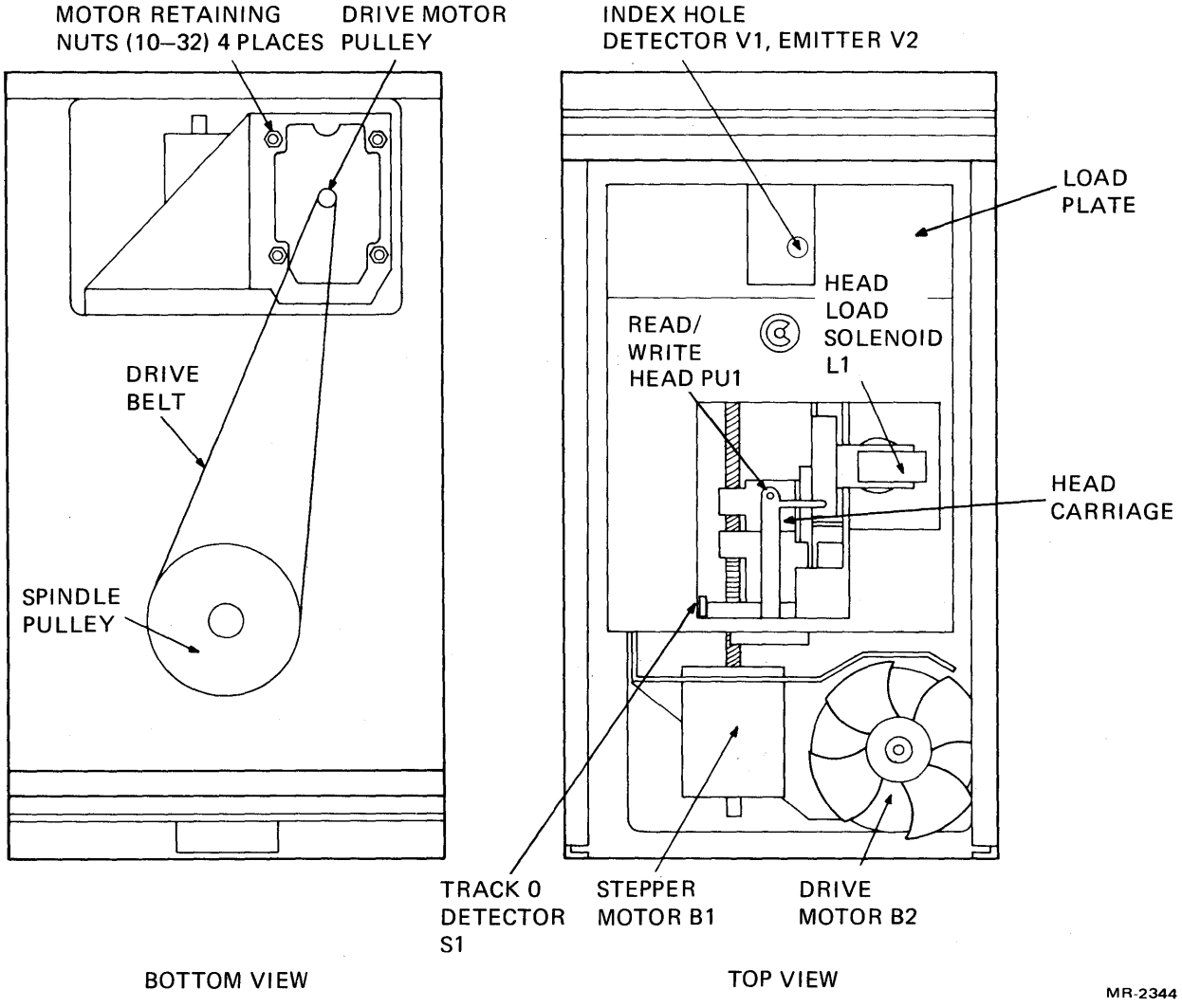


Figure 5-46 Disk Drive Assembly, Component Locations

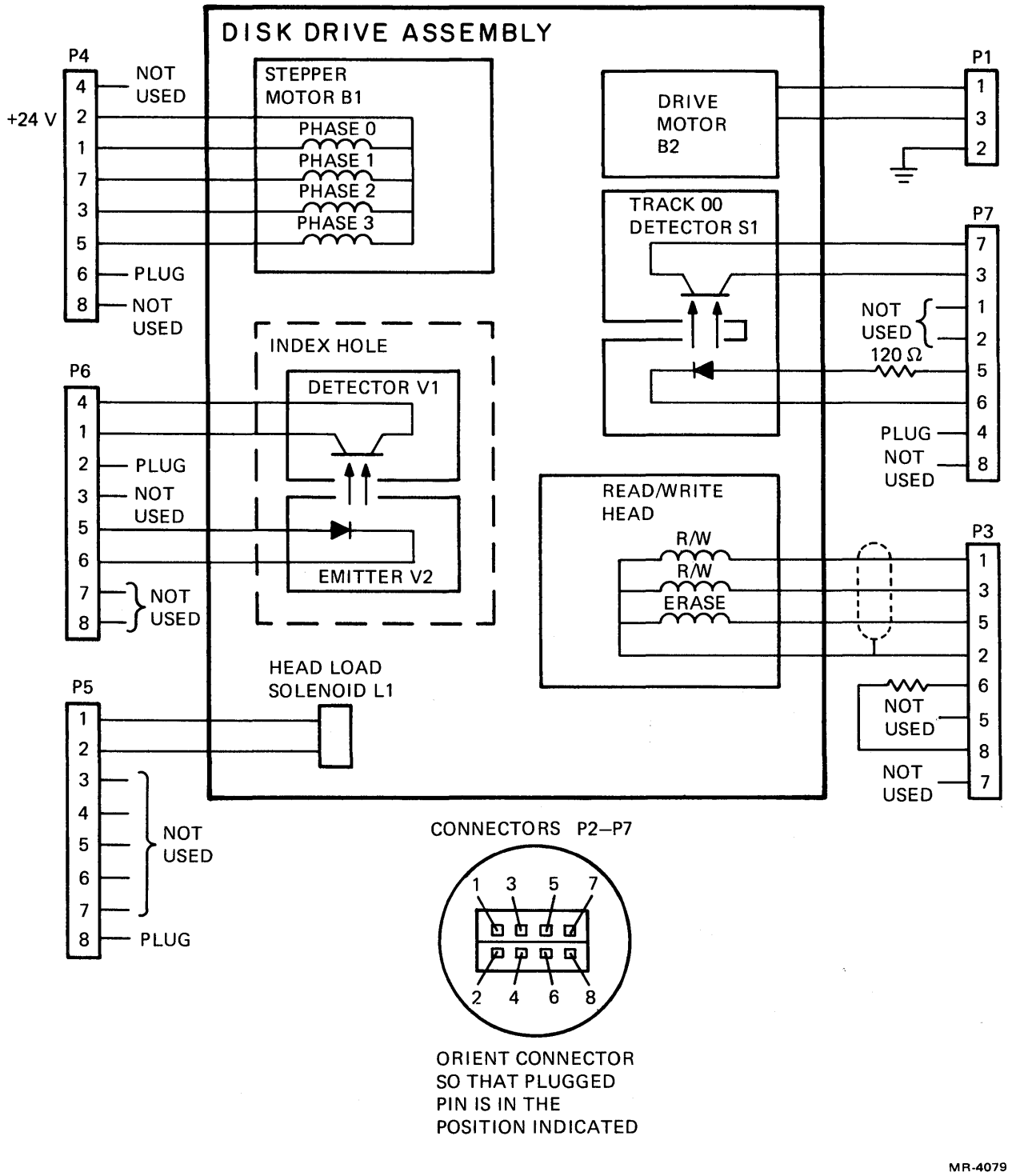


Figure 5-47 Disk Drive Assembly, Wiring Diagram

5.5.1.1 Spindle Rotation Mechanism – Figure 5-48 shows the drive mechanism that rotates the spindle pulley. The spindle motor operates with 115 V ac, 50 Hz or 60 Hz input power. Attached to one end of the motor shaft is a fan blade that provides cooling for the spindle motor. Mounted on the opposite end of the motor shaft is the drive motor pulley which is coupled to the spindle pulley through the drive belt. The spindle pulley rotates at 360 r/min.

5.5.1.2 Flexible Disk Spindle Engagement – Figure 5-49 shows the mechanism that engages the flexible disk and causes the disk to rotate with the spindle pulley. When the front cover of the disk drive unit is released to the open position, the load plate is raised and the centering cone is separated from the spindle drive hub. When a flexible disk is inserted into the disk drive assembly and the cover is closed, the load plate and centering cone expander are lowered, and the centering cone is inserted into the center hole in the flexible disk. The centering cone presses the edge of the flexible disk hole against the spindle drive hub. The pressure of the expander spring on the centering cone expander causes the tapered end of the expander to press outward against the edge of the flexible disk hole. This maintains the proper disk alignment within the drive mechanism. The expander spring also assures the proper pressure to prevent the flexible disk from slipping during rotation.

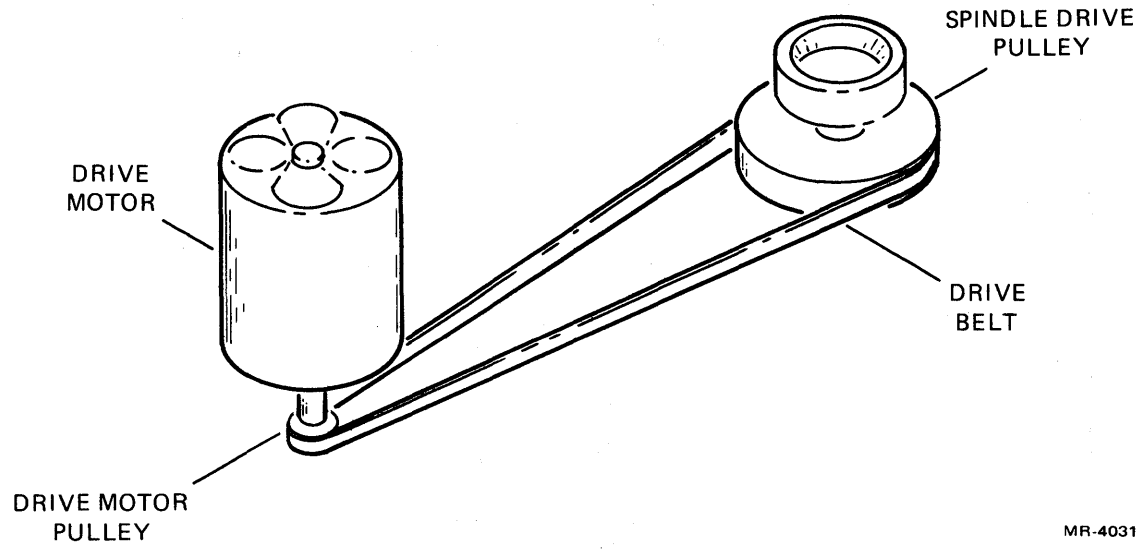


Figure 5-48 Spindle Rotation Mechanism

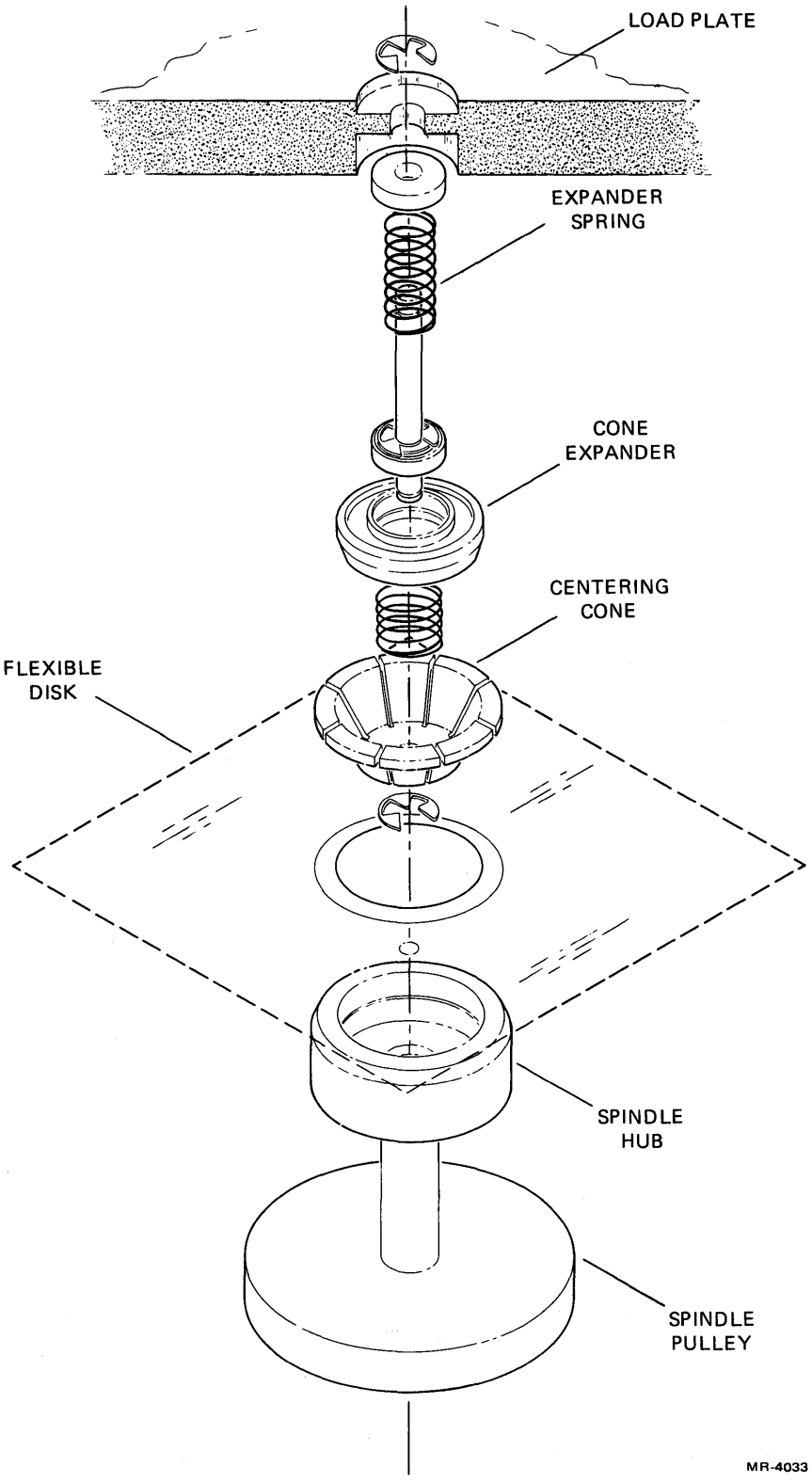


Figure 5-49 Centering Cone and Spindle Drive Components

5.5.1.3 Read/Write Head Positioning – Figure 5-50 shows the read/write head positioning mechanism that moves the read/write head on the head carriage over the selected track of the flexible disk. The head carriage is moved by the rotation of the lead screw attached to the stepper motor shaft. The motor rotation is bidirectional. As the stepper motor is pulsed by the drive circuits, the rotation of the shaft moves the head carriage toward or away from the center of the disk.

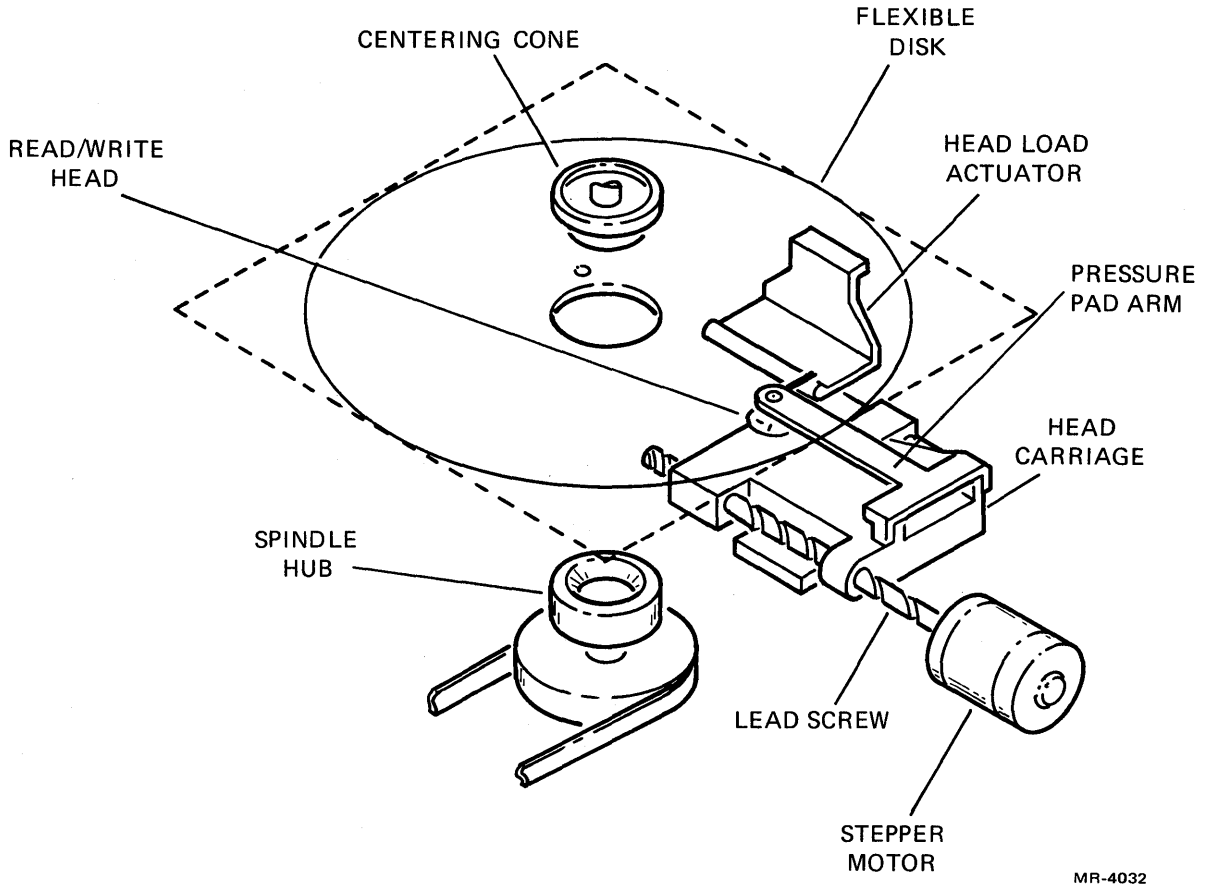


Figure 5-50 Read/Write Head Positioning Mechanism

5.5.1.4 Head Load Solenoid and Actuator – The head load solenoid (see Figure 5-46) and the head load actuator (see Figure 5-50) are attached to the load plate of the disk drive assembly. When the front cover is in the raised position, the head load actuator holds the pressure pad arm on the head carriage away from the surface of the disk. When the cover is closed, the pressure pad arm is lowered to an operating position slightly above the disk surface. The head load actuator is attached to the head load solenoid.

When the solenoid is energized, the head load actuator releases the spring-actuated pressure pad arm and allows the pad at the end of the arm to press the flexible disk surface against the read/write head. When the solenoid is de-energized, the head load actuator raises the pressure pad arm and removes the pressure pad from the flexible disk surface.

5.5.1.5 Track 00 and Index Hole Detectors – The locations of the track 00 detector S1 and the index hole detector V1 are shown in Figure 5-46. The track 00 detector senses the position of a tab attached to the head carriage. When the read/write head on the head carriage approaches track 00 (located on the outer edge of the disk), the tab of the head carriage interrupts the light sensed by detector S1 and indicates to the logic that the read/write head is in position over track 00.

The index hole emitter V2 is mounted to the load plate of the disk drive assembly and the detector V1 is mounted to the base plate. When the front cover of the disk drive assembly is in the operating position, the light from V1 is detected by V2 when the index hole in the flexible disk is between V1 and V2. This occurs once every revolution of the flexible disk and provides a strobe to the logic circuits on the Disk Controller module.

5.5.2 Drive Belt and Pulley Alignment

Perform the following procedures to replace an existing drive belt or to install a new belt.

1. Using a 3/16-inch allen wrench, loosen the (6-32) screw that secures the spindle motor pulley to the drive motor shaft as shown in Figure 5-51.

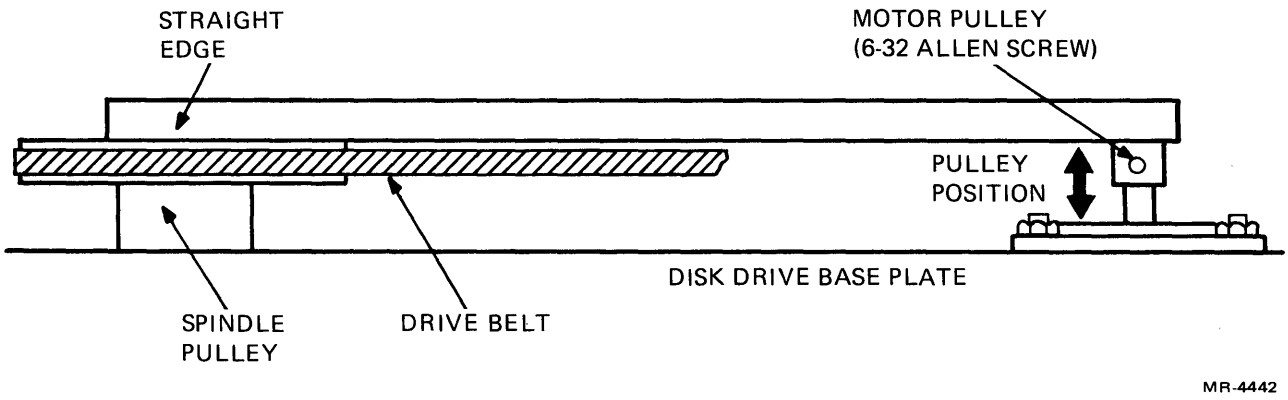


Figure 5-51 Pulley Alignment

2. Place one end of a metal straightedge on the surface of the spindle pulley and vertically align the spindle motor pulley on the motor shaft until the surface of the pulley makes contact with the opposite end of the straightedge.

3. Tighten the (6-32) screw with the 3/16-inch allen wrench.

4. Release the four (10-32) motor retaining nuts so that the motor shaft can be moved toward or away from the spindle pulley.

5. Insert the spacer gauge (part no. 93-06353-02 for 60 Hz, or 93-06353-03 for 50 Hz) between the crowns of the motor pulley and spindle pulley.

6. Reposition the motor until the ends of the spacer gauge are in contact with the crown of each pulley.

7. Tighten the four (10-32) motor retaining screws.

8. Install the drive belt (part no. 12-14005-00 for 60 Hz, or 12-14005-01 for 50 Hz) around the drive pulley and partially around the spindle pulley.

9. Rotate the spindle pulley until the belt is fed around the pulley and is firmly held in place.

10. Rotate the spindle pulley a few turns to center the belt on the crowns of the pulleys.

5.5.3 Disk Drive Assembly, 60 Hz to 50 Hz Conversion

The disk drive assemblies can be converted from operation with 60 Hz to 50 Hz input ac power by the removal and replacement of the motor pulley and drive belt. To convert the assembly to 50 Hz, perform the following procedure.

1. Remove the existing motor pulley by performing step 1 of Paragraph 5.5.2.
2. Replace the 60 Hz motor pulley with the 50 Hz pulley, part no. 74-18534-00.
3. Perform steps 2 through 9 of Paragraph 5.5.2.

CHAPTER 6
PROGRAMMING INFORMATION

This chapter describes the hardware characteristics of the PDT-11/150 and includes the addresses assigned to the internal registers, detailed descriptions of the register bit functions, and programming considerations.

User programs for the PDT-11/150 system can be developed using a DIGITAL PDP-11V03 microprocessor system or equivalent PDP-11 system. The PDP-11V03 contains an RXV11 dual flexible disk drive, and programs can be generated on a flexible disk for loading into the PDT-11/150.

The RT-11V3 operating software is used with the PDP-11 hardware to develop realtime application programs for the PDT-11/150, as shown in Figure 6-1. Refer to the DIGITAL *Microcomputer Processor Handbook 1978–79* for a description of the PDP-11V03 hardware and RT-11 operating system.

6.1 SYSTEM CHARACTERISTICS

The PDT-11/150 is an LSI-11 microprocessor-based system that is programmed using the same instruction set as the PDP-11V03. The memory assignments for the I/O page and user area are similar to standard PDP-11 systems with equivalent memory size. I/O page access time is approximately 90 μs. Any instruction addressed to the I/O page to write a byte of information will cause a dual transfer (read/write) and double the access time to 180 μs. For detailed hardware and software information relating to the LSI-11 microprocessor, refer to the DIGITAL *Microprocessor Processor Handbook 1978–79.*

The PDT-11/150 includes a parameter control register used to enable software control of the serial line devices. The system communicates externally with a maximum of six serial line devices and internally with a maximum of two flexible disks.

Each serial line device is interfaced to the PDT-11/150 through a USART and EIA level converter. Data is transferred using programmed I/O instructions or through interrupt device routines.

When transmitting data to a device using the interrupt routines, the interrupt enable bit of the CSR associated with the device must be set prior to the transfer of data to the USART. To end the data transmission, the interrupt enable bit must be cleared prior to the last data word transferred.

Console ODT (Octal Debugging Technique) commands are executed by the LSI-11 processor when the processor is in the HALT mode. These commands allow the operator to examine and alter the contents of memory and register locations through the console terminal. The halt condition is entered by pressing the BREAK key on the console keyboard when the mode switch on the rear panel is in the TEST position. If pressing the BREAK key does not cause the processor to enter the HALT mode, press the BREAK key again.

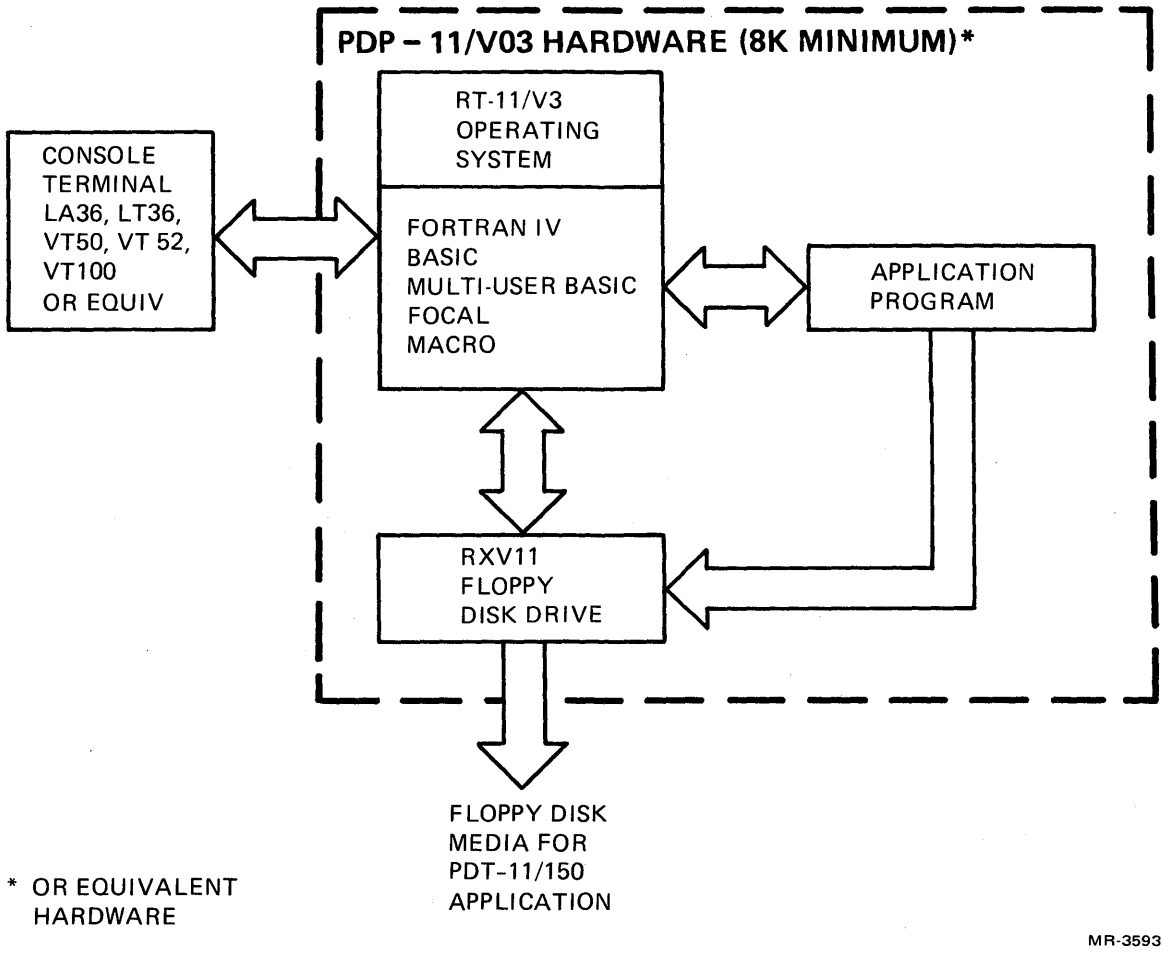


Figure 6-1 PDT-11/150 Program Development System

6.2 PERIPHERAL DEVICE COMMUNICATION

The PDT-11/150 is capable of communicating with the peripheral devices in a full-duplex transmission mode. In full-duplex mode, serial data characters can be simultaneously and independently transmitted and received. The actual operating baud rate of each device depends upon the transmission mode, the number and types of devices used with the system, and the operating or application system programs. The maximum baud rates must also be considered when using devices capable of transmitting continuous serial streams of characters of stored information from special function keys or from buffered data storage.

The maximum baud rate for each peripheral device is listed in Table 6-1.

Table 6-1 Maximum Device Baud Rate

Device	Baud Rate
Console	9600
Modem	2400 (synchronous) 4800 (asynchronous)
Printer (Line)	9600
Terminal 1	2400
2	2400
3	2400

6.2.1 Console Device

The operator's console keyboard provides for direct communication between the user and the software system. The maximum console baud rate is 9600 baud for data transfers using the standard ASCII keyboard characters. Some consoles include special function keys (cursor control, answerback functions, etc.) that, when pressed, cause a serial stream of continuous data. When these functions are required, the console baud rate should be reduced to a maximum of 4800 to prevent the loss of data during the receive transmissions.

6.2.2 Communications Modem

The communications modem can be operated synchronously at a maximum baud rate of 2400. During asynchronous transfers, the baud rate can be increased to 4800 maximum.

6.2.3 Line Printer Terminal

The printer terminal is capable of operating with the system at a maximum rate of 9600 baud.

6.2.4 Cluster Option Terminals

The cluster EIA interface permits the operation of three additional terminal devices, each at a maximum data transfer rate of 2400 baud. Each terminal can include a keyboard with the standard ASCII character set. When the terminal contains buffered data storage or special function keys, as described in Paragraph 6.2.1, the baud rate should be reduced to a maximum of 2000.

6.2.5 Power-Up and Manual Reset Conditions

When ac power is applied to the PDT-11/150 unit, or when the mode switch on the rear panel is momentarily set to the RESET position, the parameters listed in Table 6-2 will be preselected for the serial line interfaces and line time clock (LTC).

The baud rate and parameters of the console interface may be changed by selecting different parameters under program control when power is initially applied. Refer to Paragraph 6.3.1.

If the console autobaud function is selected (see Table 3-4), the character parameters of the console device must be set prior to establishing the baud rate to 8-bit length (one start bit, one stop bit and no parity).

Table 6-2 Preselected Device Parameters

Device Interface	Baud Rate	Character Parameters
Console	9600*	8-bit length including one start bit and one stop bit. Baud rates of 110 require two stop bits.
Modem	1200 (asynchronous mode)	
Printer	1200 No parity	
Cluster Terminal 1 Terminal 2 Terminal 3	300	
Line Time Clock (LTC)**	The INT ENB (bit 06) of the TCSR is set to 1. Refer to Table 5-23.	

* Autobaud function disabled (see Table 3-4).
** LTC enabled (see Table 3-4).

6.2.6 Programmed Reset Instruction (Initialize)

If a reset instruction is issued during programmed operation, all device registers will be reset and any operation in process will be terminated. If the INT ENB (bit 06) of the LTC was previously cleared, the reset instruction will set the bit to 1. If the synchronous mode was selected for the modem interface, the reset will cause the interface to default to the asynchronous mode.

6.3 DEVICE AND INTERRUPT VECTOR ADDRESS ASSIGNMENTS

Each of the registers associated with the device interfaces, disk drives, and the line time clock have specific device addresses assigned. In addition, all interfaces that have the capability to generate a programmed interrupt request have unique vector address assignments to locations in RAM memory, where the device service routines are stored. All device and vector addresses are fixed and may not be altered by the user. Figure 6-2 shows the relationship of the control and buffer registers within the PDT-11/150.

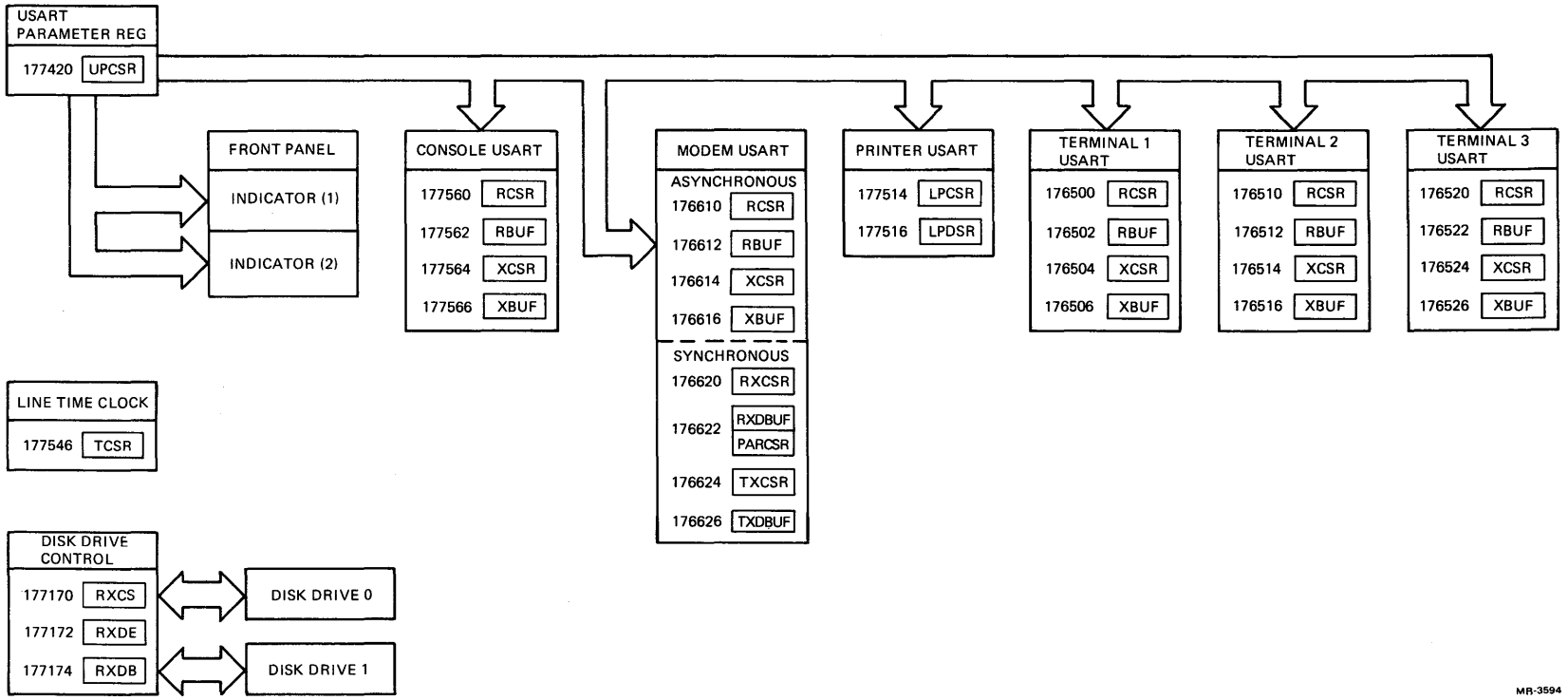


Figure 6-2 PDT-11/150 Device Register Address Assignments

6.3.1 USART Parameter Control Register Address

The USART parameter control register (UPCSR) is used to select the operating parameters of the standard USART interfaces and the optional USART interfaces. The standard devices are the console, modem and printer. The optional devices are terminals 1, 2 and 3. The register also enables the user to control the 1 and 2 indicator lamps on the front panel of the unit. When operating synchronously with a modem on the communications interface, an additional parameter control/status register (PARCSR) is also used for selecting operating parameters. The following address is assigned to the USART parameter register.

USART PARAMETER 177420
REGISTER ADDRESS

6.3.2 Standard Terminal Addresses

Table 6-3 lists the device and interrupt vector address assignments for the I/O registers associated with each of the three standard devices that operate with the PDT-11/150. The address assignments cannot be changed.

6.3.3 Optional (Cluster) Terminal Addresses

Table 6-4 lists the device and interrupt vector address assignments for the I/O registers associated with each of the three additional terminals. Terminals operate with the PDT-11/150 when option DFT11-AB is installed.

6.3.4 Disk Drive Addresses

Table 6-5 lists the address assignments of the registers and interrupt vector for the single or dual disk unit. The RXCS register information specifies either disk drive 0 or 1.

6.3.5 Line Time Clock Addresses

Table 6-6 lists the device and interrupt vector address assignments for the line time clock within the PDT-11/150.

Table 6-3 Standard Device and Vector Addresses

Device Type	Address	
	Register	Interrupt Vector
CONSOLE TERMINAL		
Receiver Control/ Status Register (RCSR)	177560	Receive 000060 Transmit 000064
Receiver Data Buffer Register (RBUF)	177562	
Transmitter Control/ Status Register (XCSR)	177564	
Transmitter Data Buffer Register (XBUF)	177566	
ASYNCHRONOUS COMMUNICATIONS MODEM		
Receiver Control/ Status Register (RCSR)	176610	Receive 000330 Transmit 000334
Receiver Data Buffer (RBUF)	176612	
Transmitter Control/ Status Register (XCSR)	176614	
Transmitter Data Buffer (SBUF)	176616	
SYNCHRONOUS COMMUNICATIONS MODEM		
Receiver Control/ Status Register (RXCSR)	176620	Receive 000340 Transmit 000344
Receiver Data Buffer (RXDBUF)	176622	
Parameter Control/ Status Register (PARCSR)	176622	
Transmitter Control/ Status Register (TXCSR)	176624	
Transmitter Data Buffer (TXDBUF)	176626	
PRINTER		
Control/Status Register (LPCSR)	177514	Transmit 000200
Receiver Data Buffer (LPDSR)	177516	

Table 6-4 Optional (Cluster) Terminals, Device and Vector Addresses

Device Type	Address	
	Register	Interrupt Vector
TERMINAL NO. 1		
Receiver Control/ Status Register (RCSR)	176500	Receive 000300 Transmit 000304
Receiver Data Buffer (RBUF)	176502	
Transmitter Control/ Status Register (XCSR)	176504	
Transmitter Data Buffer (XBUF)	176506	
TERMINAL NO. 2		
Receiver Control/ Status Register (RCSR)	176510	Receive 000310 Transmit 000314
Receiver Data Buffer (RBUF)	176512	
Transmitter Control/ Status Register (XCSR)	176514	
Transmitter Data Buffer (XBUF)	176516	
TERMINAL NO. 3		
Receiver Control/ Status Register (RCSR)	176520	Receive 000320 Transmit 000324
Receiver Data Buffer (RBUF)	176522	
Transmitter Control/ Status Register (XCSR)	176524	
Transmitter Data Buffer (XBUF)	176526	

Table 6-5 Disk Drive, Device and Vector Addresses

Device Type	Address	
	Register	Interrupt Vector
Receiver Control/ Status Register (RXCS)	177170	
Data Buffer Register (RXDE)	177172	
Used as data and error/ status register for the following two functions:		000264
RX Data Buffer (RXDB) RX Error and Status (RXSA)		
RX Track/Sector Register (RXSA)	177174	

Table 6-6 Line Time Clock, Device and Vector Address

Device Type	Address	
	Register	Interrupt Vector
Line Time Clock	177546	000100

6.4 STANDARD TERMINAL REGISTER FORMATS

The following paragraphs describe the content and function of the registers associated with each of the three standard terminal interfaces.

6.4.1 USART Parameter Register

The operating parameters of the devices connected to the standard interface or optional (cluster) interface and the user lights (1) and (2) on the front panel can be selected and modified by the USART parameter register. The interface for each device is initialized at power-up time and must be programmed for operating conditions after initialization if different conditions are required. Figure 6-3 shows the word format and Table 6-7 describes the function of the bits. This register is write-only and must be programmed as a full 16-bit word.

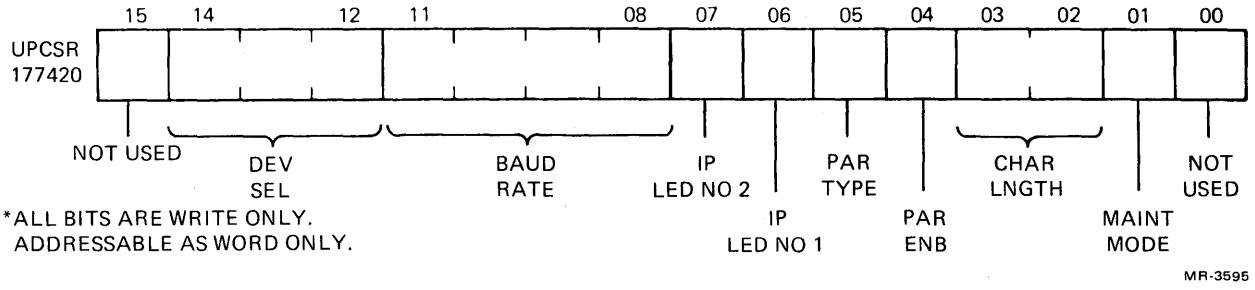


Figure 6-3 USART Parameter Control Register UPCSR Format

Table 6-7 USART Parameter Register Bit Descriptions

Bit	Name	Description
15	Not Used	
14–12	DEV SEL	Device Select – Selects one of the six standard or optional device interfaces for parameter information as follows:
11–08	BAUD RATE	Baud Rate – Selects the desired baud rate for the interface selected as follows:

Bits 14	13	12	Interface Selected
0	0	0	Cluster terminal no. 1 (option)
0	0	1	Console terminal
0	1	0	Printer terminal
0	1	1	Communications (modem)
1	0	0	Selects user lights on indicator panel
1	0	1	Cluster terminal no. 2 (option)
1	1	0	Cluster terminal no. 3 (option)

Baud Rate	Bits 11	10	09	08	Baud Rate	Bits 11	10	09	08
50	0	0	0	0	1800	1	0	0	0
75	0	0	0	1	2000	1	0	0	1
110*	0	0	1	0	2400	1	0	1	0
134.5	0	0	1	1	3600	1	0	1	1
150	0	1	0	0	4800	1	1	0	0
300	0	1	0	1	7200	1	1	0	1
600	0	1	1	0	9600	1	1	1	0
1200	0	1	1	1	19200	1	1	1	1

Table 6-7 USART Parameter Register Bit Descriptions (Cont.)

Bit	Name	Description
07	LED No. 2	Indicator Panel – Set to light the "2" LED on the PDT-11/150 indicator panel.
06	LED No. 1	Indicator Panel – Set to light the "1" LED on the PDT-11/150 indicator panel.
05	PAR TYPE	Parity Type – Selects odd or even parity when enabled by PARENB (bit 04) as follows: 1 = even parity 0 = odd parity
04	PAR ENB	Parity Enable – Enables or disables the parity check function as follows: 1 = enable parity 0 = disable parity
03–02	CHAR LNTH	Character Length – Selects the number of bits in each character transferred as follows:
01	MAINT MODE	Maintenance Mode – Set to 1 to select the maintenance mode. Used during diagnostic programs to loop back cluster option interface data and communications interface data from the standard interface.
00	Not Used	

Bits 03	Bits 02	Character Length (Bits)
0	0	5
0	1	6
1	0	7
1	1	8

*Baud rate 110 assumes two stop bits.

6.4.2 Console Device Interface

Program information and status and control information are transferred between the user and the PDT-11/150 system using the console device and interface. Four registers are associated with the interface. The content and format of the registers are shown in Figure 6-4 and described in the following paragraphs.

6.4.2.1 Receiver Control/Status Register (RCSR) – The RCSR provides control and status information for data transferred from the console device to the PDT-11/150. Table 6-8 describes the functions of the bits of the RCSR.

Table 6-8 Console Interface, Receiver Register Bit Descriptions

Bit	Name	Description
15–08	Not Used	RCSR Receiver Control/Status Register.
07	RCVR DONE	Receiver Done – A read-only bit set when an incoming character is available in the RCVR data register (RBUF). If the RCVR INT ENB (bit 06) is set, an interrupt request will be generated. Cleared by the INIT signal or when the RBUF is read.
06	RCVR INT ENB	Receiver Interrupt Enable – A read/write bit set by program to allow the RCVR DONE (bit 07) to generate an interrupt request. Cleared by the INIT signal or under program control.
05–00	Not Used	
15–08	Not Used	RBUF (Receiver Data Buffer).
07–00	RCVD DATA	Received Data – Read-only bits comprising the last character assembled by the USART from the console. If the specified character length is less than eight bits, the character will appear right-justified with the low-order bit in bit 00. The unused high-order bits of the word will contain (0).

6.4.2.2 Receiver Data Buffer (RBUF) – The RBUF stores the data characters received by the PDT-11/150 from the console device. Table 6-8 lists and defines the functions of the bits in the RBUF.

6.4.2.3 Transmitter Control/Status Register (XCSR) – The XCSR provides control and status information during information transfers from the PDT-11/150 to the console device. See Table 6-9.

6.4.2.4 Transmitter Data Buffer (XBUF) – The XBUF stores the data characters for transmission to the console from the PDT-11/150. Table 6-9 lists the bit assignments and describes their functions.

6.4.3 Communications Interface (Modem)

The communications (modem) interface in the PDT-11/150 transmits and receives standard EIA levels from a Bell 103, 113, 202, or 212 data set or equivalent device. The communications interface is programmable to operate with synchronous and asynchronous data transmissions in either a half- or full-duplex mode.

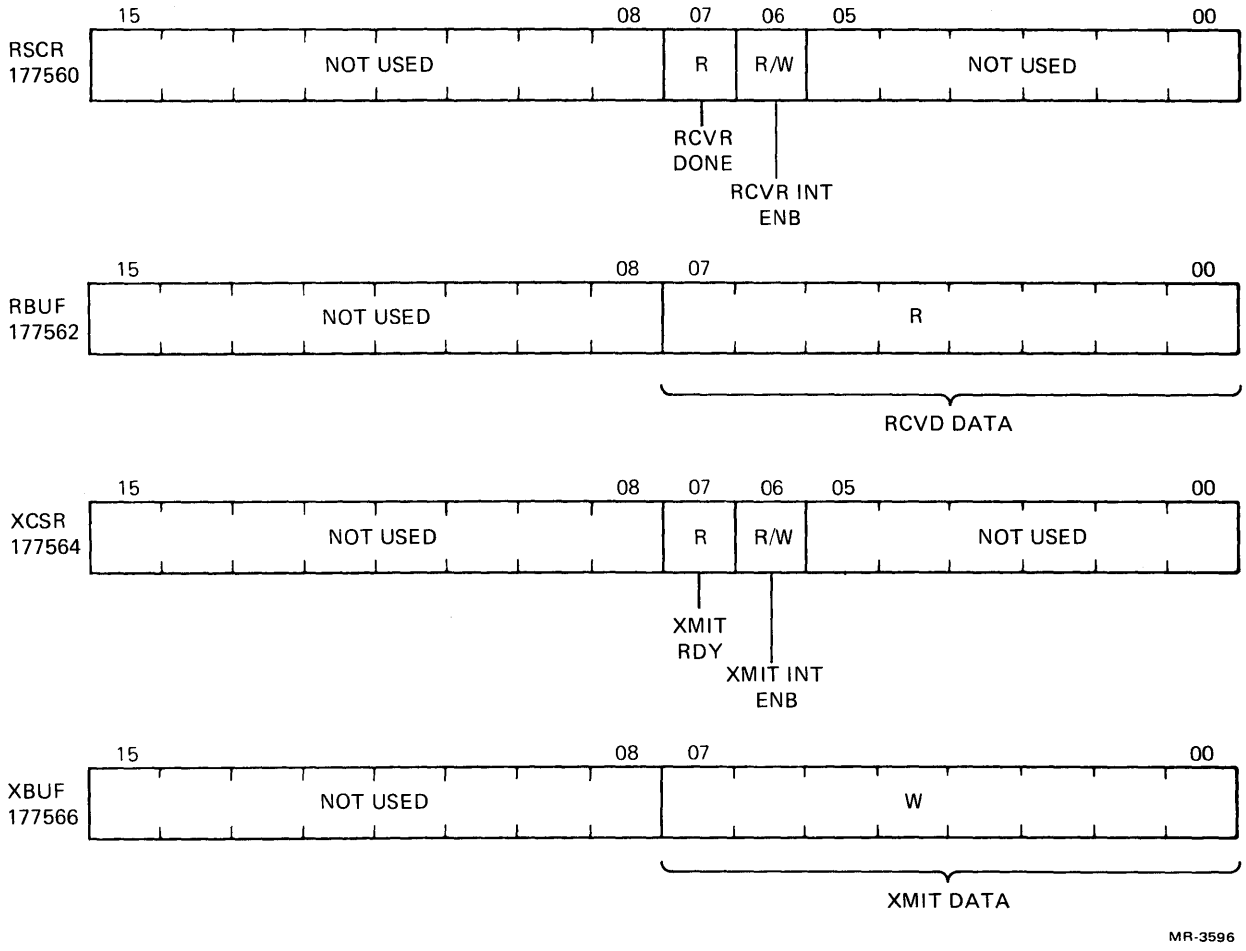


Figure 6-4 Console Terminal Interface Register Formats

Table 6-9 Console Interface, Transmitter Register Bit Descriptions

Bit	Name	Description
15–08	Not Used	XCSR (Transmitter Control/Status Register).
07	XMIT RDY	Transmitter Ready – A read-only bit set when the transmit buffer is ready to accept a character. Also set by the INIT signal. If the XMIT INT ENB (bit 06) is set, an interrupt request will be generated. Cleared when a character is loaded into the XBUF.
06	XMIT INT ENB	Transmitter Interrupt Enable – A read/write bit set by program to allow the XMIT RDY (bit 07) to generate an interrupt request. Cleared by the INIT signal or under program control.
05–00	Not Used	
15–08	Not Used	XBUF (Transmitter Data Buffer).
07–00	XMIT DATA	Transmit Data – Write-only bits comprising the data character to be transmitted serially to the console. If the specified character length is less than eight bits, the character must be right-justified with the low-order bit in bit 00 position when loaded.

Figure 6-5 indicates the methods used to select the synchronous or asynchronous transfers. When the PDT-11/150 system is initialized, the asynchronous mode is preselected with the parameters indicated on the diagram. To modify the parameter information in the asynchronous mode, follow the procedures on the left branch of the diagram. The synchronous transmission mode is selected by followingthe procedures indicated on the right branch of the diagram. Refer to the appropriate tables for parameter definitions.

To determine if the receiver has been synchronized when the synchronous mode is selected, the user should monitor the RCVR DONE (bit 07) of the RXCSR. This bit only becomes asserted (1) when synchronization has been attained. If the STRIP SYNC (bit 08) of the RXCSR is asserted, the RCVR DONE will indicate the receipt of a valid data character. The RCVR DONE bit will not be asserted when the sync character is recognized. If the STRIP SYNC is not asserted, the RCVR DONE (bit 07) will indicate the receipt of either a sync character or data character.

When selecting the asynchronous mode by the parameter register after the synchronous mode was previously selected, the contents of the asynchronous register RCSR (176610) should be monitored to detect the possibility of a false framing error.

CAUTION

A programmed reset instruction from the microprocessor will cause the interface to change from the synchronous mode to the asynchronous mode and clear all flags.

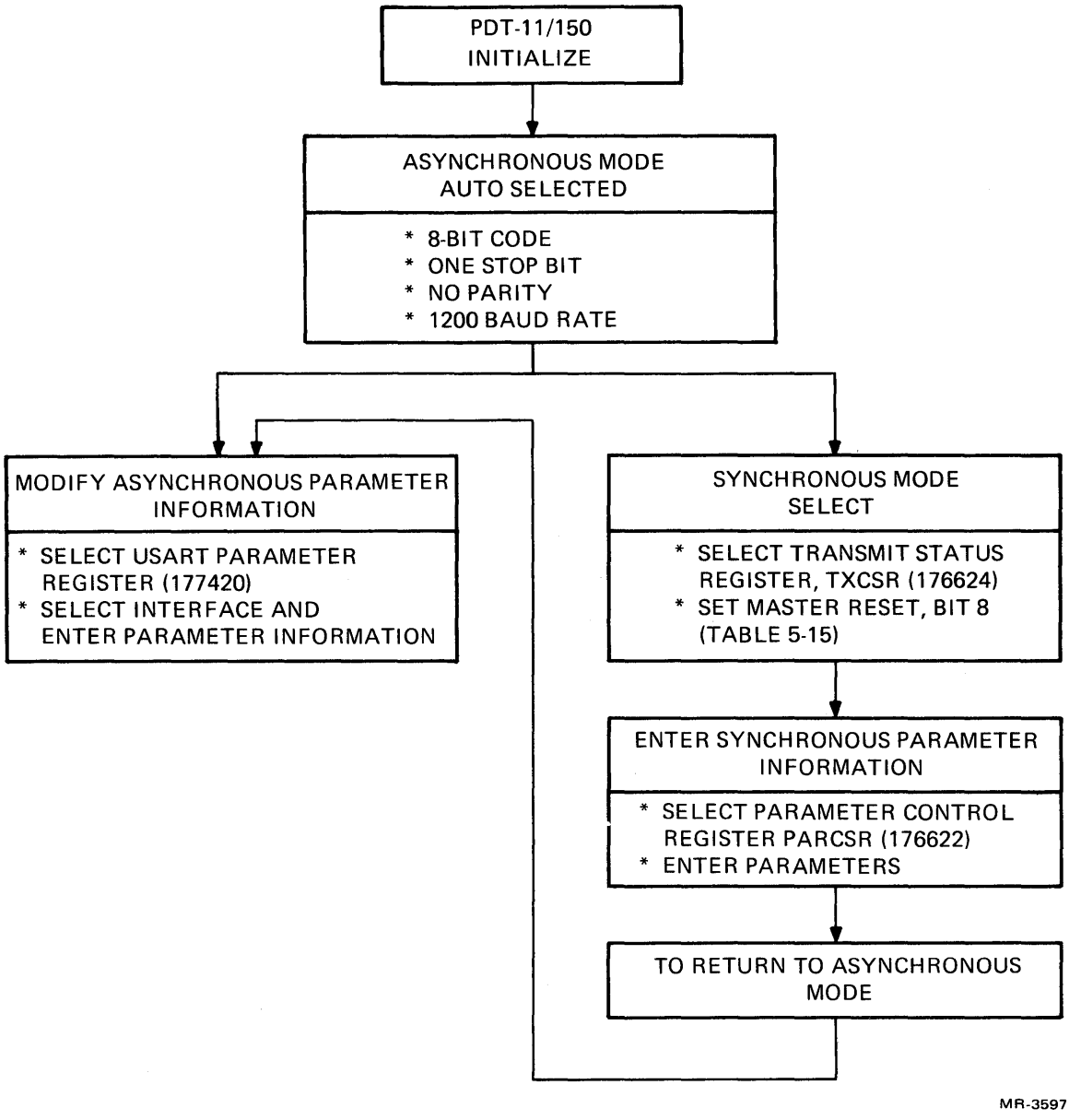


Figure 6-5 Communication Interface, Asynchronous/Synchronous Select

NOTE

When clearing an interrupt enable bit (INT ENB), first set the processor to its highest priority (processor status word PSW bit 7 = 1). After the interrupt enable bit is cleared, the processor may be returned to its normal priority (PSW bit 7 = 0).

EXAMPLE PROGRAM:

```
MTPS #200
BIC #100, CSR
MTPS #0
EXIT
```

6.4.4 Asynchronous Modem Interface

Four registers are associated with the asynchronous communications. Two registers provide data control and status information during the receive functions, and two registers provide this information during transmit functions. In addition, the USART parameter register can be programmed to modify the parameter information. Figure 6-6 shows the bit formats for each of the registers associated with the interface. The asynchronous communications interface is designed to be compatible with the DIGITAL LSI-11 microprocessor, DLV11-E asynchronous serial line interface as described in the DIGITAL *Memories and Peripherals Handbook 1978–79*.

6.4.4.1 Asynchronous Receiver Control/Status Register (RCSR) – The RCSR provides control and status information during all operations. Table 6-10 lists and defines the function of each bit.

6.4.4.2 Asynchronous Receiver Data Buffer (RBUF) – The RBUF register stores the data bits received from the line and indicates any error conditions associated with the data received. Table 6-11 lists and describes the bit functions.

6.4.4.3 Asynchronous Transmitter Control/Status Register (XCSR) – The XCSR provides control and status information during transmit operations. Table 6-12 describes the function of each bit in the register.

6.4.4.4 Asynchronous Transmitter Data Buffer (XBUF) – The XBUF stores the data information for transmission to the line. The bit functions are described in Table 6-13.

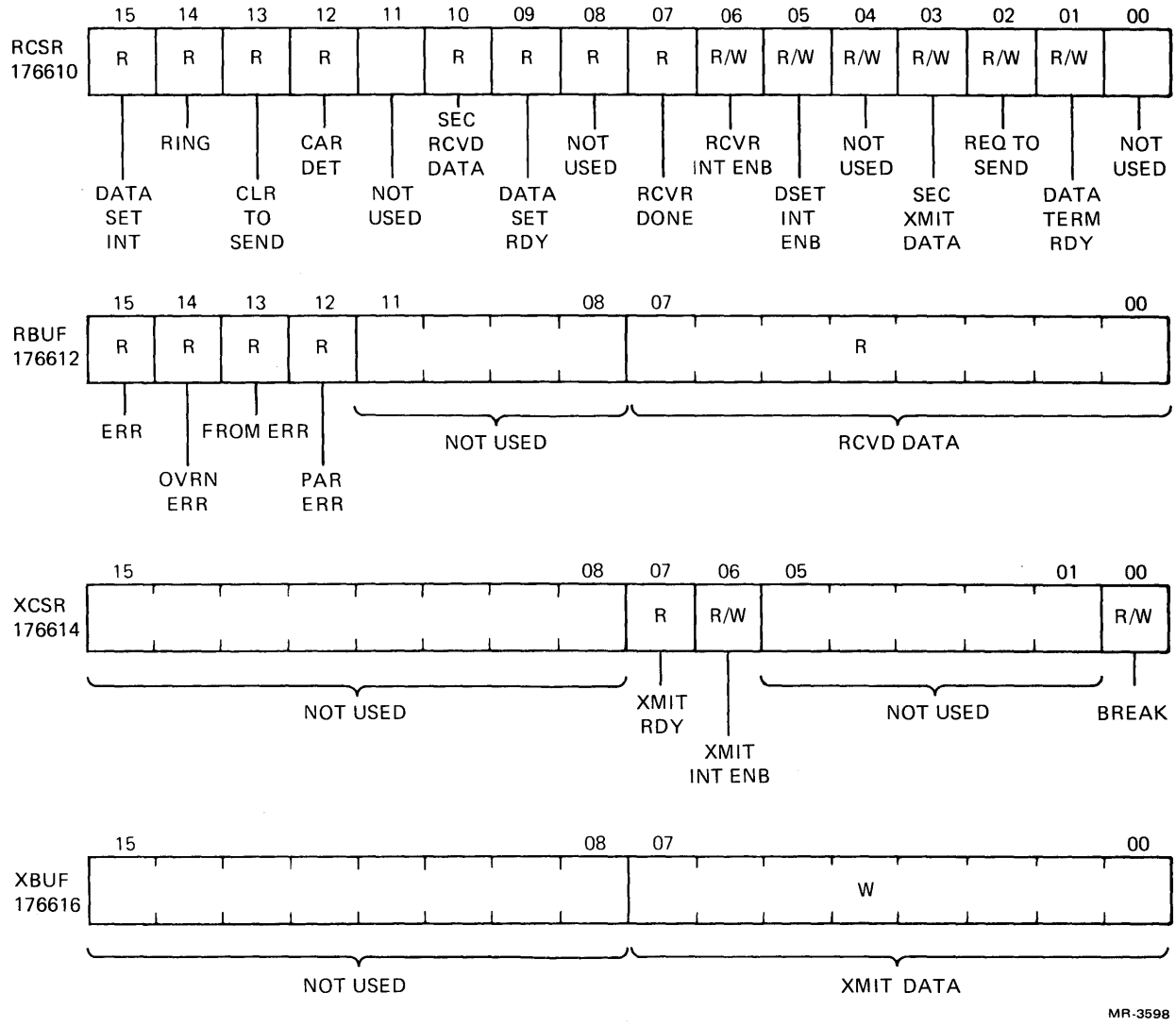


Figure 6-6 Asynchronous Communications Interface Register Formats

Table 6-10 Asynchronous Communication, RCSR Bit Descriptions

Bit	Name	Description
15	DATA SET CHNG	Data Set Change – A read-only bit that initiates an interrupt sequence, provided the DAT SET INT ENB bit (05) is also set. Set whenever CAR DET, CLR TO SEND, DATA SET READY, or SEC REC changes state in a 0-to-1 or 1-to-0 transition. Also set when Ring changes from 0 to 1. Cleared by the INIT signal or by reading the RCSR.
14	RING	Ring – A read-only bit; when set, indicates that a RINGING signal is being received from the data set. The RINGING signal is an EIA control with a cycle time of two seconds on and four seconds off.
13	CLR TO SEND	Clear to Send – A read-only bit. The state of this bit depends on the state of the clear-to-send signal from the data set. When set, indicates an ON condition; when clear, indicates an OFF condition.
12	CAR DET	Carrier Detect – A read-only bit set when the data carrier is received. When clear, indicates either the end of the current transmission activity or an error condition.
11	Not Used	
10	SEC REC	Secondary Received or Supervisory Received Data – A read-only bit that provides a receive capability for the reverse channel of a remote station. A space (approx. 10 V) is a 1. (A transmit capability is provided by bit 03.)
09	DATA SET READY	Data Set Ready – A program read-only bit that is a direct reflection of the Data Set Ready (or interlock) lead emanating from the modem. When asserted, this line indicates that the modem is powered up and not in the test, talk, or dial mode. Any transition of this bit will cause the Data Set Change bit to be asserted.

Table 6-10 Asynchronous Communication, RCSR Bit Descriptions (Cont.)

Bit	Name	Description
08	Not Used	
07	RCVR DONE	Receiver Done – A read-only bit set when an entire character has been received and is ready for transfer to the LSI-11. When set, it initiates an interrupt sequence, provided RCVT INT ENB (bit 06) is also set. Cleared whenever the receiver buffer (RBUF) is addressed and by the INIT signal.
06	RCVR INT ENB	Receiver Interrupt Enable – A read/write bit. When set, it allows an interrupt sequence to start when the DONE (bit 07) is set. Cleared by the INIT signal.
05	DSET INT ENB	Data Set Interrupt Enable – A read/write bit. When set, it allows an interrupt sequence to start when the DATA SET INT (bit 15) is set. Cleared by the INIT signal.
04	Not Used	
03	SEC XMIT	Secondary Transmit or Supervisory Transmitted Data – A read/write bit that provides a transmit capability for a reverse channel of a remote station. When set, it transmits a space (approx. 10 V). (A receive capability is provided by bit 10.) Cleared by the INIT signal.
02	REQ TO SEND	Request to Send – A read/write bit used to control the transmitted data of the data set. Cleared by the INIT signal.
01	DTR	Data Terminal Ready – A read/write bit. When set, it permits the connection of the communications channel in the data set. When clear, it disconnects the interface from the channel. Cleared by the INIT signal.
00	Not Used	

Table 6-11 Asynchronous Communications, RBUF Bit Descriptions

Bit	Name	Description
15	ERROR	Error – A read-only bit that indicates an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13 and 12, respectively). Whenever one of these bits is set, it causes ERROR to set. This bit is not connected to the interrupt logic. Cleared when the error producing the condition is removed. If a byte of data is read and no new data character is received, the error indication is cleared. Cleared by the INIT signal.
14	OR ERR	Overrun Error – A read-only bit; when set, it indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character. Cleared by the INIT signal.
13	FR ERR	Framing Error – A read-only bit; when set, it indicates that the character that was read had no valid STOP bit. Cleared by the INIT signal.
12	P ERR	Parity Error – A read-only bit; when set, it indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected.
11–08	Not Used	
07–00	RCVD DATA	Received Data Bits – Read-only bits that represent the character received from the modem. If less than eight bits are selected, the buffer is right-justified into the least significant bit positions. The higher unused bit or bits are read as zeros. Not cleared by the INIT signal. If parity is selected at the UPCSR (PAR ENB bit = 1) for characters less than eight bits, the parity will be appended to the next bit position from the highest-order bit of the character. No parity is present when an 8-bit character is used. When the character is read, RCVR DONE (bit 07) of the RCSR is cleared.

Table 6-12 Asynchronous Communications, XCSR Bit Assignments

Bit	Name	Description
15–08	Not Used	
07	XMIT READY	Transmit Ready – A read-only bit set when the transmitter buffer is ready to accept a character. This condition initiates an interrupt sequence when XMIT INT ENB (bit 06) is set. Also set by the INIT signal.
06	XMIT INT ENB	Transmit Interrupt Enable – A read/write bit; when set, it allows an interrupt sequence to start when XMIT READY, bit 07, is set.
05–01	Not Used	
00	BREAK	Break – A read/write bit; when set by program, it transmits a continuous space character to the external device. Cleared by the INIT signal. The duration of the space character transmission must be controlled by the program using software timers.

Table 6-13 Asynchronous Communications, XBUF Bit Descriptions

Bit	Name	Description
15–08	Not Used	
07–00	XMIT DATA CHAR	Transmit Data Character – Write-only bits that comprise the data character for transfer to the modem. If the character is less than eight bits, it must be loaded right-justified at the least significant bit.

6.4.5 Synchronous Modem Interface

The synchronous mode of the communications interface is selected as described in Paragraph 6.4.3. Two registers are associated with the receive operation of the USART and two registers are associated with the transmit operations. Figure 6-7 shows the formats for each of the four registers. In addition, a parameter control register, specifically for the synchronous mode, is programmable to specify the transmission characteristics.

Certain programming procedures are required to terminate the transmission of data when operating full- or half-duplex in the synchronous mode.

For full-duplex transmission, perform the following procedures.

1. Load the last character to be transmitted into the TXDBUF (176626) in response to the assertion of the XMIT DONE (bit 07) of the TXCSR (176624).

2. Clear the send (BIT 04) of the TXCSR (176624) in response to the assertion of the next XMIT DONE (bit 07) of the TXCSR. This will cause the XMIT DONE (bit 07) and DATA NOT AVAIL (bit 15) to remain asserted after the last character is serialized.

For half-duplex transmission, perform the following procedures.

1. Load all "ones" into the TXDBUF (1776626) in response to the assertion of XMIT DONE (bit 07) of the TXCSR (176624). At this time, the previous data character is being serialized.

2. Clear the SEND (bit 04) of the TXCSR (176624) in response to the assertion of the next XMIT DONE (bit 07) of the TXCSR. The last data character has been transmitted when XMIT DONE is set to (1).

3. Clear the REQ TO SEND (bit 02) of the RXCSR (176620). One or more of the "ones" bits loaded into the TXDBUF at step 1 will be transmitted before the SEND (bit 04) of the TXCSR (176624) is cleared.

6.4.5.1 Parameter Control Register (PARCSR) – Figure 6-8 shows the word format of the PARCSR and Table 6-14 lists the bit assignments.

6.4.5.2 Synchronous Receiver Control/Status Register (RXCSR) – The RXCSR is programmed and monitored during receive data operations. The register is addressable as a word or byte and contains control and status information from the modem. Table 6-15 lists and defines the function of each bit.

6.4.5.3 Synchronous Receiver Data Buffer (RXDBUF) – The RXDBUF stores the character received from the modem and indicates error conditions associated with the received data. Table 6-16 lists and describes the functions of the RXDBUF bits.

6.4.5.4 Synchronous Transmitter Control and Status Register (TXCSR) – The TXCSR is programmed and monitored to provide control and status operations. Table 6-17 describes the function of each bit.

6.4.5.5 Synchronous Transmitter Data Buffer (TXDBUF) – The TXDBUF contains eight bits of data to be transmitted serially to the modem and is addressable as a word or byte to an even address only. The remaining eight bits in the word are not used. Table 6-18 describes the character formats for the eight data bits.

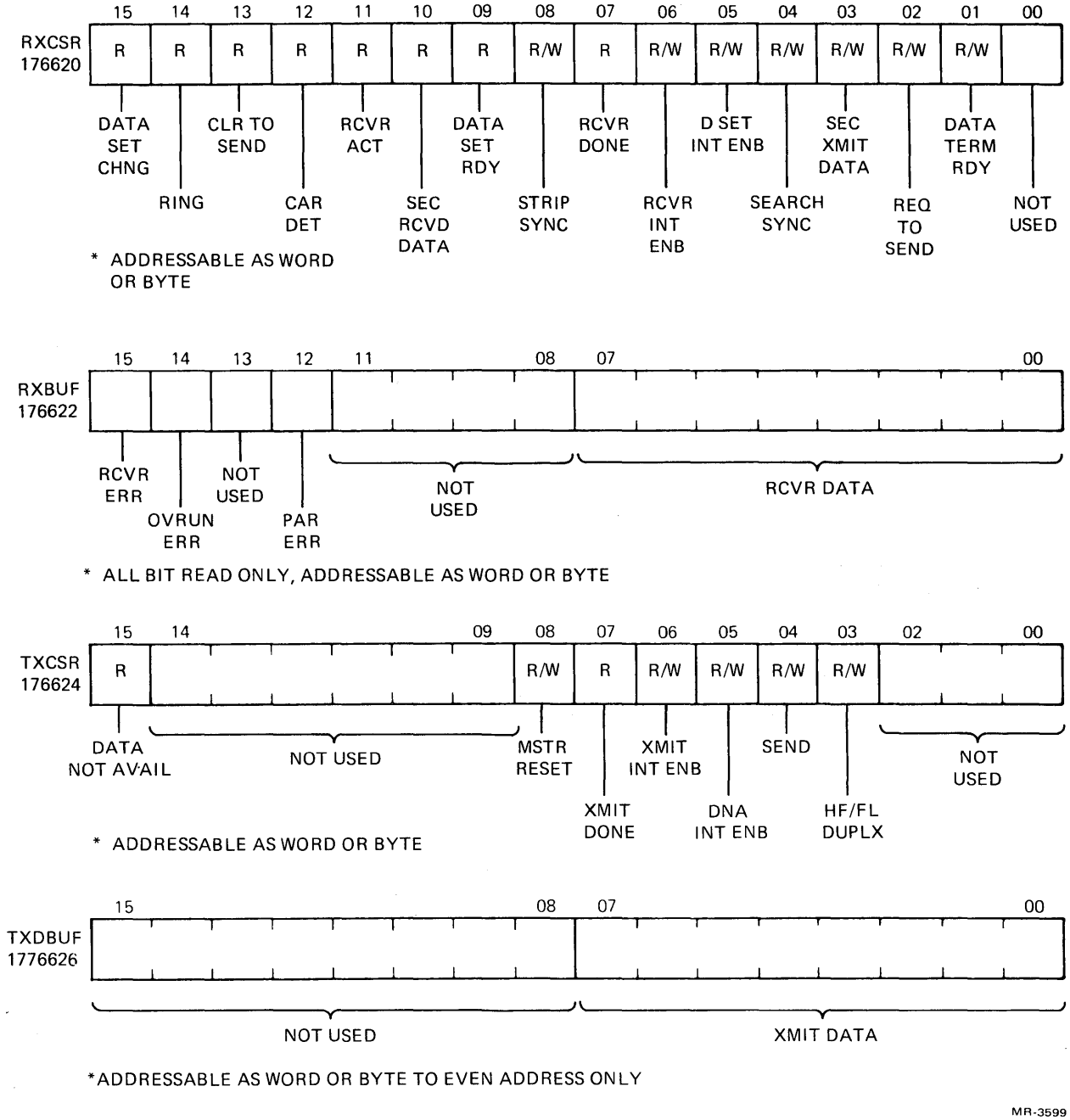


Figure 6-7 Synchronous Communications Interface Register Formats

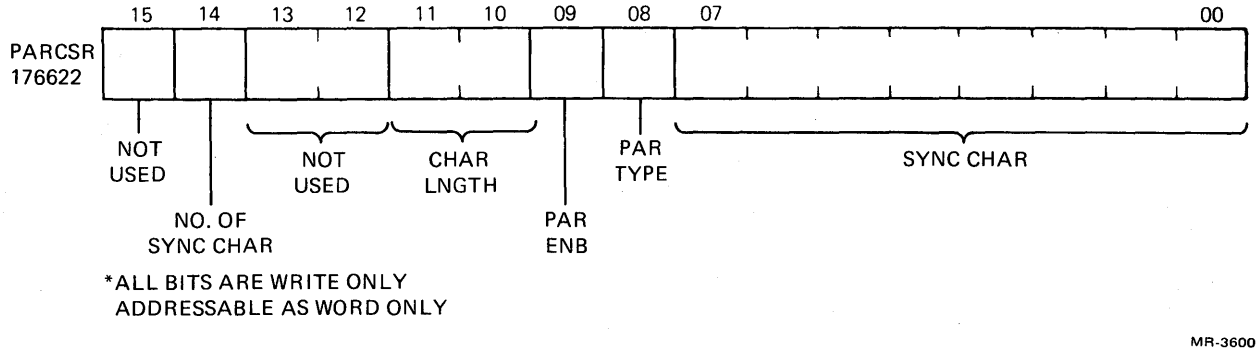


Figure 6-8 Synchronous Communications Parameter Control Register Format

Table 6-14 Parameter Control Register, PARCSR Bit Descriptions

Bit	Name	Description
15	Not Used	
14	NO SYNC CHAR	Number of Sync Characters – A write-only bit that selects either one or two sync characters; it must be received for successfully synchronization as follows: 1 – selects two sync characters 0 – selects one sync character
13–12	Not Used	
11, 10	CHAR LENGTH	Character Length – Write-only bits that select the number of bits associated with each character as follows:

Bits 11	Bits 10	Character Length
0	0	5
0	1	6
1	0	7
1	1	8

09	PAR ENB	Parity Enable – Enables or disables the parity check function as specified by PAR TYPE (bit 08) as follows: 1 = enable parity generation 0 = disable parity generation
08	PAR TYPE	Parity Type – Program write-only bit used to select odd or even parity generation when enabled by PARENB (bit 09) as follows: 1 = even parity 0 = odd parity Parity is added to transmitted characters and a parity check is performed on received characters.
07–00	SYNC CHAR	Sync Character – Program write-only; used for character synchronization prior to transmitting a serial character stream. Character format and number of characters transmitted depends on the command mode. Refer to modem information. Sync character will be all 1s after master reset. Character length is right-justified from bit 00.

Table 6-15 Synchronous Communications, RXCSR Bit Descriptions

Bit	Name	Description
15	DATA SET CHNG	Data Set Change – A read-only bit set to indicate a level transition on one of the following modem lines: Ring Clear to Send Carrier Secondary Received Data Data Set Ready If D SET INT ENB (bit 05) is set, the level transition will cause an interrupt request by the receiver. Cleared by the INIT signal or when the RXCSR is read.
14	RING	Ring Indicator – A read-only bit set to indicate that a ring signal is being received from the modem.
13	CLR TO SEND	Clear to Send – A program read-only bit set to indicate that the modem is ready to receive data from the interface.
12	CAR DET	Carrier Detect – A program read-only bit set by the modem whenever an acceptable carrier is on the communications line.
11	RCVR ACT	Receiver Active – A program read-only bit set when the selected number of continuous sync characters (either one or two) from the modem has been received. Cleared by the INIT signal.
10	SEC RCV DATA	Secondary Received Data – A program read-only bit that reflects the state of the Secondary Received Data line from the modem. Any transition on the line will also assert DATA SET CHANGE (bit 15). Supervisory data can be received over this line when operating with some modems. As a control line, it can also be used to acknowledge a message.
09	DATA SET RDY	Data Set Ready – A program read-only bit that reflects the state of the Data Set Ready line from the modem. When asserted, the line indicates that the modem is powered up and is not in the test, talk, or dial mode. Any transition on the line will also assert the DATA SET CHANGE (bit 15).
08	SRIP SYNC	Strip Sync – A program read/write bit; when set, it prevents the receive characters which match the contents of the sync register from causing an RCVR interrupt, provided no errors are detected in the RXDBUF. Cleared by the INIT signal.

Table 6-15 Synchronous Communications, RXCSR Bit Descriptions (Cont.)

Bit	Name	Description
07	RCVR DONE	Receiver Done – A program read-only bit normally set when a character is transferred into the receive buffer. If the character received is a sync character and the STRIP SYNC (bit 08) and RCVR ACT (bit 11) are set, the RCVR DONE bit will not be asserted. Cleared by reading the RXBUF or by the INIT signal.
06	RCVR INT ENB	Receiver Interrupt Enable – A program read/write bit; when set, it allows a receiver interrupt request to be generated, provided RCVR DONE (bit 07) is set. Cleared by the INIT signal.
05	D SET INT ENB	Data Set Interrupt Enable – A program read/write bit; when set, it allows a receiver interrupt request to be generated, provided the D SET CHANGE (bit 15) is asserted. Cleared by the INIT signal.
04	SEARCH SYNC	Search Sync – A program read/write bit; when set, it enables the comparison of the received data with the sync code stored in the sync register. After the selected number of sync characters are detected, the RCVR ACT (bit 11) is asserted. Cleared by the INIT signal.
03	SEC XMIT DATA	Secondary Transmit Data – A program read/write bit that indicates the status of the secondary transmit line of the modem. Supervisory data can be transmitted on this line with certain modems. It also can be used to acknowledge a message. Cleared by the INIT signal.
02	REQ TO SEND	Request to Send – A program read/write bit; when set, it causes the Request to Send line to the modem to be asserted. This line is asserted prior to transmitting serial data to the modem. Cleared by the INIT signal.
01	DATA TERM RDY	Data Terminal Ready – A program read/write bit; when set, it causes the Data Terminal Ready line to the modem to be asserted. During Autodial and manual call origination, asserting the line maintains the established call. For Autoanswer, it allows handshaking in response to a ring signal. Cleared by the INIT signal.
00	Not Used	

Table 6-16 Synchronous Communications, RXDBUF Bit Descriptions

Bit	Name	Description
15	RCVR ERR	Receiver Error – A program read bit set when either or both the PAR ERR (bit 12) and OVRN ERR (bit 14) are set. Cleared when both the PAR ERR and OVRN ERR bits are cleared.
14	OVRN ERR	Overrun Error – A program read bit, set to indicate a data overrun in the receiver. When the RCVR DONE (bit 07) of the RXCSR is set, the processor must read the RXBUF within a specified time or the overrun error will occur. The time specified is as follows: Ts = (1/baud rate) × bits/character Cleared by the INIT signal or when the RXDBUF low byte is read.
13	Not Used	
12	PAR ERR	Parity Error – A program read bit; if parity detection is enabled, it is set when the parity of the received character is different from the parity selected by PAR TYPE (bit 08) of the PARCSR. A detected parity error will also set RCVR ERR (bit 15). Cleared by the INIT signal or when the RXDBUF low byte is read.
11–08	Not Used	
07–00	RCVR DATA CHAR	Receiver Data Character – Program read bits that represent the data character from the modem and are stored in the RXDBUF. The character can be five to eight bits in length and is always right-justified. Parity, if selected, always appears after the MSB except for an 8-bit character, where no parity will be indicated. Cleared by reading the low byte of RXDBUF, which also clears RCVR DONE (bit 07) of the RXCSR.

Table 6-17 Synchronous Communications, TXCSR Bit Assignments

Bit	Name	Description
15	DATA NOT AVAIL	Data Not Available – A program read bit set to indicate that a character has been transmitted from the sync register to the modem. A sync character is transmitted if a new character is not loaded into the TXDBUF within a specified time after the XMIT DONE (bit 07) is set. The time interval is as follows. Ts = (1/baud rate) × (bits/character – 1/2 bit time) If the DNA INT ENB (bit 05) is set when DATA NOT AVAIL is asserted, a transmitter interrupt request will be generated. Cleared by the INIT signal or when a character is transmitted.
14–09	Not Used	
08	MSTR RESET	Master Reset – A program read/write bit; when set, it causes the receiver and transmitter to enter an idle state. The transmitter idle state results in the following: 1. Internal timing is reset. 2. Transmitter sync register is set to all ones. 3. All bits of the TXCSR are cleared. The receiver state results in the following: 1. Internal timing is reset. 2. The following RXCSR bits are cleared. **Bit Name** 15 DATA SET CHANGE 11 RCVR ACT 08 STRIP SYNC 07 RCVR DONE 06 RCVR INT ENB 05 D SET INT ENB 04 SEARCH SYNC 03 SEC XMIT DATA 02 REQ TO SEND 01 DATA TERM RDY
07	XMIT DONE	Transmitter Done – A program read bit set to indicate that the TXDBUF is ready to receive a data character. If the XMIT INT ENB (bit 06) is set when XMIT DONE is asserted, a transmitter interrupt request is generated. Cleared by the INIT signal or when the TXDBUF receives a character.

Table 6-17 Synchronous Communications, TXCSR Bit Assignments (Cont.)

Bit	Name	Description
06	XMIT INT ENB	Transmitter Interrupt Enable – A program read/write bit set to allow a transmitter interrupt request to be generated when the XMIT DONE (bit 07) is asserted. Cleared by the INIT signal.
05	DNA INT ENB	Data Not Available Interrupt Enable – A program read/write bit set to allow a transmitter interrupt request to be generated when DATA NOT AVAIL (bit 15) is asserted. Cleared by the INIT signal.
04	SEND	Send – A program read/write bit set to enable data transfer from the transmitter. The SEND bit must be asserted for the entire message otherwise, only the current character will be transferred and the transmitter will enter the idle state. Cleared by the INIT signal.
03	HF/FL DUPLEX	Half- or Full-Duplex – A read/write bit used to select half- or full-duplex transmission. 1 = half duplex 0 = full duplex The receiver will be disabled if the SEND (bit 04) is asserted during half-duplex operation.
02–00	Not Used	

Table 6-18 Synchronous Communications, TXDBUF Bit Assignments

Bit	Name	Description
15–08	Not Used	
07–00	XMIT DATA CHAR	Transmit Data Character – Program write bits that represent the data character stored in the TXBUF for transfer to the modem. Character length is from five to eight bits and right-justified at bit 00. The INIT signal sets all ones in the TXDBUF.

6.4.6 Printer Terminal Interface

The printer terminal interface transfers EIA-compatible serial line data to the printer unit at a maximum rate of 9600 baud. To prevent the loss of data when the printer buffer is full, an XOFF ASCII command is issued by the printer to stop the data transfers. The XON ASCII command indicates that the printer buffer can accept additional data.

When the interface is initialized, the following data parameters are selected. However, the parameters can be modified through the USART parameter register as described in Paragraph 6.3.1.

DATA WORD PARAMETERS - 8-bit, one start bit, one stop bit, no parity, 1200 baud.

Figure 6-9 shows the bit formats for the printer terminal interface registers.

6.4.6.1 Printer Control/Status Register (LPCSR) - Table 6-19 lists and defines the functions of the bits in the LPCSR.

6.4.6.2 Printer Data Buffer (LPDSR) - Table 6-20 lists and defines the functions of the bits in the LPDSR.

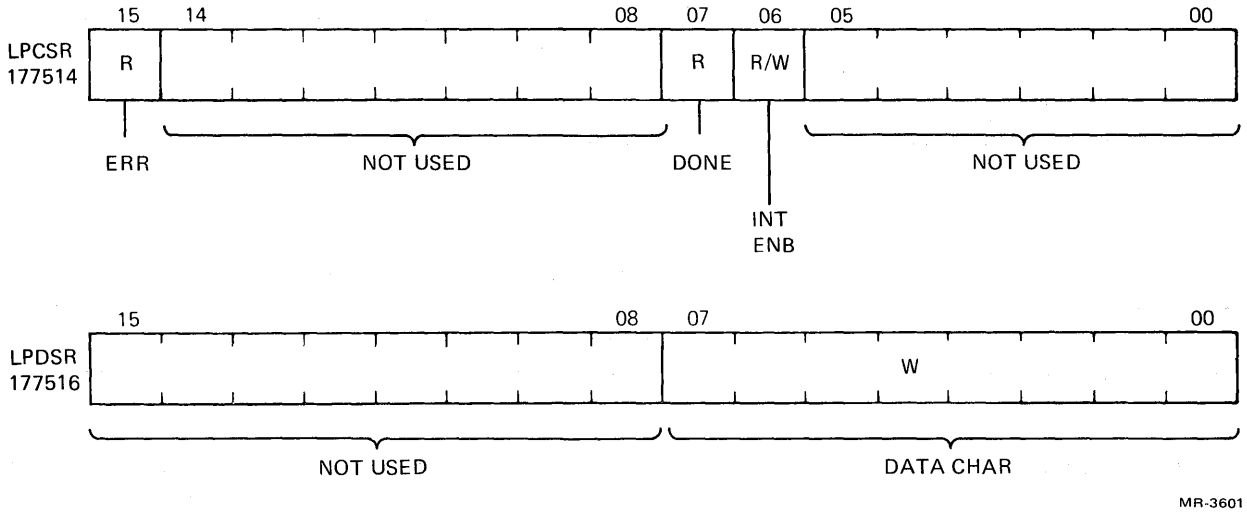


Figure 6-9 Printer Terminal Interface Register Formats

Table 6-19 Printer Interface, LPCSR Bit Descriptions

Bit	Name	Description
15	ERR	Error – A read-only bit set when the Data Terminal Ready line from the printer is negated. This condition occurs when the printer terminal paper is depleted or the printer is not powered-up. Cleared when the condition is corrected or when power is applied.
14–08	Not Used	
07	DONE	Done – A read-only bit set when the printer is ready to accept a character. An interrupt request will be generated, provided the INT ENB (bit 06) is set. The DONE bit is set by the INIT signal and cleared by loading a character into the data register (LPDSR).
06	INT ENB	Interrupt Enable – A read/write bit set or cleared under software control. When set, an interrupt request will be generated provided DONE (bit 07) is set. Cleared by the INIT signal.
05–00	Not Used	

Table 6-20 Printer Interface, LPDSR Bit Descriptions

Bit	Name	Description
15–08	Not Used	
07–00	DATA CHAR	Data Character – Write-only bits that represent the data character to be transferred to the printer. Bit 07 is the most significant bit of the 8-bit character.

6.5 OPTIONAL TERMINAL REGISTER WORD FORMATS

The cluster option enables the PDT-11/150 to operate with three additional serial line devices. The interface parameters are selected by the USART parameter register as described in Paragraph 6.3.1. The register formats are identical to the console terminal described in Paragraph 6.4.2.

6.6 DISK DRIVE REGISTER FORMATS

Software control of the disk drive is through three registers available on the disk controller interface: the command and status register (RXCS); the data buffer register (RXDB); and the track and sector address register (RXSA). These registers can be read or loaded by programs using instructions referring to the register device addresses. The interface also contains a read/write data buffer that can contain 64 16-bit words of disk data.

Read and write data transfers require two operations. When writing on a disk, the program is required to transfer data to the data buffer through the RXDB. When the buffer is full, a write sector command is issued through the RXCS and the data is written on the disk.

During a read operation, the data is first read into the buffer from the disk and then read from the buffer through the RXDB. At the completion of a function, the RXDB will contain the current error and status (RXES) of the function selected.

The RXSA that contains the track and sector addresses is loaded prior to issuing a read or write command.

Figure 6-10 shows the bit assignments for the registers described in the following paragraphs.

6.6.1 Drive Control/Status Register (RXCS)

Table 6-21 provides a description of each bit in the RXCS. The information in the RXCS initiates and selects the functions of the drives, indicates errors, and selects one of the two drives on a dual drive unit.

Function Select Codes - The FUNC SEL (bits 03–01) are used to select any of the eight functions associated with each drive. Detailed information of each function follows.

Fill Buffer (000)

The fill buffer function is used to load the interface buffer with 64 16-bit words of data from the microprocessor memory. After loading, the contents of the buffer can be written onto a disk by a write sector function (010) or returned to the microprocessor by an empty buffer function (001). DONE (bit 07) is cleared at the start of the function and set when all 64 words are stored.

NOTE

To prevent loss of data, only 16-bit words, not 8-bit bytes, can be transferred during a fill buffer command. The DONE (bit 07) will not be set at the completion of the transfer when less than 64 words are loaded.

The UNIT SEL (bit 04) is not required for this function because no data transfer to a drive is specified.

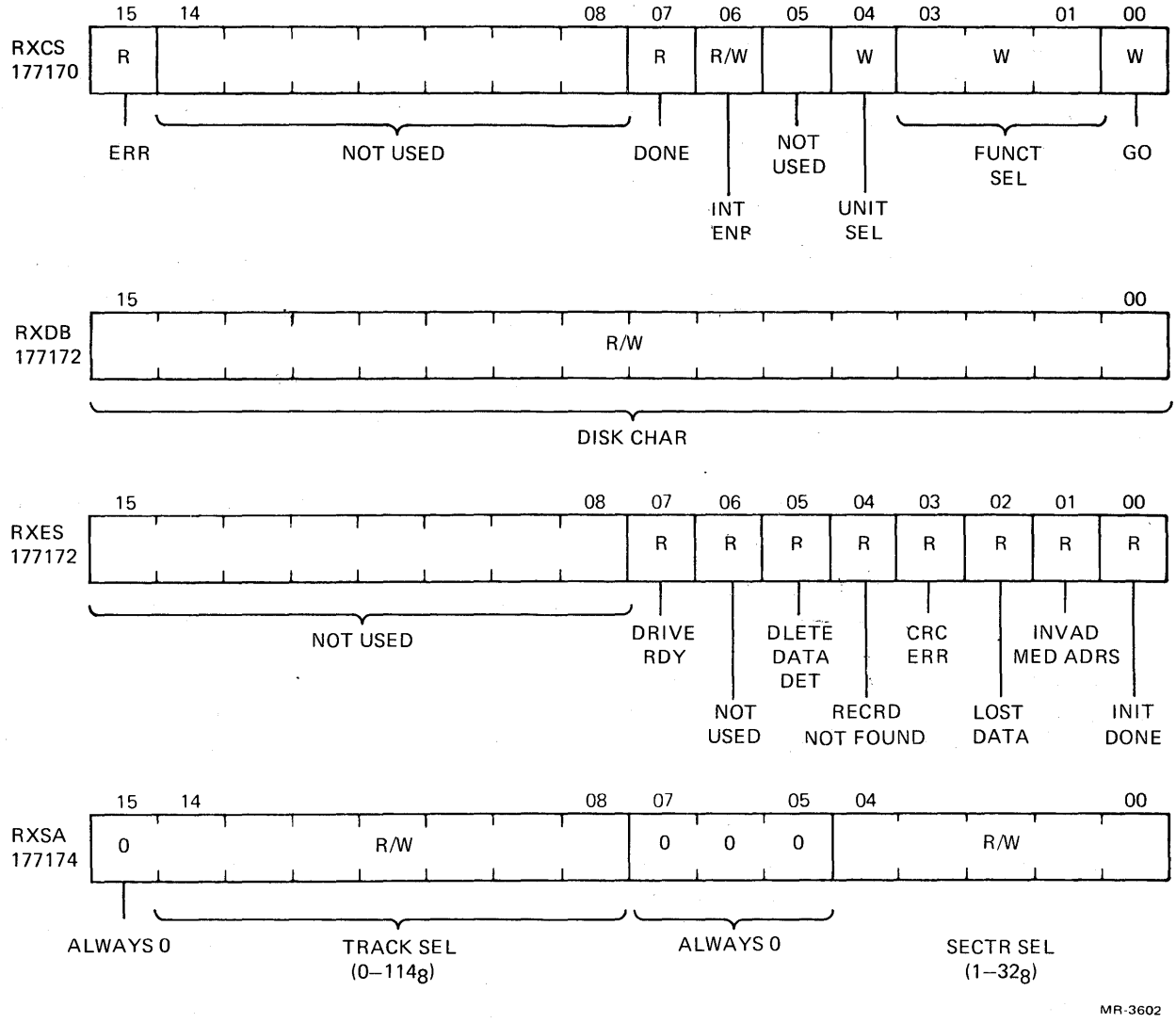


Figure 6-10 Disk Drive Interface Register Formats

Table 6-21 Disk Controller, RXCS Bit Descriptions

Bit	Name	Description
15	ERR	Error – A read-only bit set to indicate that an error has occurred during an attempt to execute a command. Cleared by the initiation of a new command and by the INIT signal.
14–08	Not Used	
07	DONE	Done – A read-only bit set to indicate the completion of a function. When set, it results in an interrupt request, provided the INT ENB (bit 06) is set.
06	INT ENB	Interrupt Enable – A read/write bit set by the program to enable an interrupt request when the disk drive has completed an operation (DONE bit set). Cleared by the INIT signal.
05	Not Used	
04	UNIT SEL	Unit Select – A read/write bit used to select disk drive 0 or 1. In a PDT-11/150 single drive unit, the drive is always 0. 0 = disk drive 0 1 = disk drive 1
03–01	FUNC SEL	Function Select – Three write-only bits used to select the operation associated with the selected drive as follows: **Code Function** 000 Fill buffer 001 Empty buffer 010 Write sector 011 Read sector 100 Initialize 101 Read status 110 Write deleted data sector 111 Restore
00	GO	Go – A write-only bit; when set, it initiates a command selected by bits 01–03 to the drive selected by bit 4.

Empty Buffer (001)
The empty buffer function transfers to the microprocessor 64 words of data that were previously loaded by a read sector (011), initialize (100) or fill buffer (000) function. DONE (bit 07) is cleared at the start of the command and set when all 64 words have been transferred.

NOTE
This function does not destroy the contents of the interface buffer.

Write Sector (010)
The write sector command will write the 64 words of data stored in the interface buffer onto the disk sector specified by the track and sector address of the RXSA. The track and sector address must be issued prior to this command. Following the data information, a 16-bit CRC (Cyclic Redundancy Check) character will be written within the sector.

The initiation of this command clears all the status bits in the RXES register.

DONE (bit 07) is cleared at the start of the function and set at the completion of the operation.

If the specified sector has not been located within two revolutions of disk, ERR (bit 15) and DONE (bit 07) will be set and a program interrupt will be requested if INT ENB (bit 06) has been previously set.

NOTE
A write sector command issued after a power interruption of the PDT-11/150 may result in the recording of random data onto the disk from the buffer.

Read Sector (011)
The read sector command causes 64 16-bit words of data from a specified sector on the disk to be read and loaded into the interface buffer. The track and sector address information of the RXSA must be issued prior to this instruction. The initiation of this command clears all the status bits in the RXES register. DONE (bit 07) is cleared at the start of the function and set at the completion of the operation.

If the specified sector or track has not been located within two revolutions of the disk, ERR (bit 15) and DONE (bit 07) will be set and a program interrupt will be requested if the INT ENB (bit 06) was previously set.

If a deleted data address mark is detected after the sector is located, the interface will set DEL DATA DET (bit 05) of RXES and ERR (bit 15) and DONE (bit 07) of the RXCS. A program interrupt will be generated at completion, provided INT ENB (bit 06) was previously set. The contents of the RXES status register will then be available by reading the RXDB.

As data is loaded into the interface buffer, a CRC is computed, based on the information in the data field, and compared with the 16-bit CRC character recorded on disk. If the two CRC characters are different, a read error is detected and CRC ERR (bit 03) of the RXES is set, and ERR (bit 15) and DONE (bit 07) of RXCS are set. A program interrupt will be requested at completion, provided the INT ENB (bit 06) was previously set. The contents of the RXES status register will then be available by reading the RXDB.

Initialize (100)
The initialize command clears the registers and buffers within the disk drive interface and performs a restore, followed by a read operation at sector 1, track 1, of drive 0. In a dual, disk drive unit, a restore operation will be performed on both drive 0 and drive 1 prior to reading data at drive 0. At the start of the command, DONE (bit 07) will be cleared. At the end of the command, bit 07 will be set. Upon completion of a successful initialize operation, the ERR (bit 15) of the RXCS and all RXES status bits will be cleared, except for DR RDY (bit 07) and INIT DONE (00), which will be set.

CAUTION

During power-up, an initialize command is automatically issued, and no programmed command can be issued until DONE (bit 07) is set, indicating the initialize operation has been completed.

Read Status (101)
The read status command assembles the current status of the selected drive in the RXES for transfer to the program through the RXDB. At the start of the operation, DONE (bit 07) RXCS is cleared. The DR RDY (bit 07) of the RXES will reflect the status of the drive selected by UNIT SEL (bit 04) of the RXCS at the time the command was issued. At the completion of the operation, DONE (bit 07) will be set and an interrupt request will be generated, provided the INT ENB (bit 06) was previously set. The contents of the RXDB can then be sampled to obtain the RXES.

Write Sector with Deleted Data (110)
This command initiates an operation similar to the write sector (010) command except that a deleted data address mark, instead of a standard data address mark, precedes the data field.

Restore (111)
The restore command moves the read/write head of the selected drive over track 0. At the completion of the command, DONE (bit 07) is set, and an interrupt request is generated, provided the INT ENB (bit 06) has been previously set.

6.6.2 Disk Controller Data Buffer Register (RXDB)
The RXDB provides a general-purpose data path between the disk drives and the interface. All data information to and from the disk is transferred through this register. The register also contains the current error and status conditions for the disk specified at the completion of a disk function (RXES).

CAUTION

Either data or status information may be present in this register; therefore, violation of the protocol in the manipulation of this register may result in loss of data.

Figure 6-10 shows the RXDB register format during data transfers and Table 6-22 describes the functions of the bits.

Table 6-22 Disk Controller, RXDB Bit Descriptions

Bit	Name	Description
15–00	DISK CHAR	Disk Character – A 16-bit word that reflects the disk serial information read or to be written on the disk. All information to and from the disk is transferred through the RXDB as word transfers only.

Figure 6-10 shows the RXES error and status information format at the completion of a function, and Table 6-23 describes the functions of each bit.

Table 6-23 Disk Controller, RXES Bit Descriptions

Bit	Name	Description
15–08	Not Used	
07	DR RDY	Drive Ready – A ready-only bit set when the following conditions exist: 1. Selected drive is present. 2. Selected drive has power. 3. Selected drive has disk properly installed with door closed and has reached operating speed. If a function FUNC SEL (bits 03–01 of RXCS) is issued prior to the above conditions, ERR (bit 15) and DONE (bit 07) of the RXCS will be asserted. DR RDY bit is valid only when retrieved during a read status function or at completion of an initialize command the status of drive 0 is indicated.
06	Not Used	
05	DEL DATA DET	Deleted Data Detected – A read-only bit set to indicate that the identification mark preceding the data field was decoded as a deleted mark during a data recovery function.
04	REC NOT FND	Record Not Found – A read-only bit set to indicate that the specified track and sector were not located within two revolutions of the disk during a write or read operation. This condition results in ERR (bit 15) and DONE (bit 07) of the RXCS being set.
03	CRC ERR	Cycle Redundancy Check Error – A read-only bit set to indicate that a cycle redundancy check error was detected as the information was retrieved from a data field on the disk. This condition results in ERR (bit 15) and DONE (bit 07) of the RXCS being set.
02	LOST DATA	Lost Data – A read-only bit set to indicate that the disk controller failed to respond to a data request in one byte time. This condition sets ERR (bit 15) and DONE (bit 07) of the RXCS.
01	INV MED ADRS	Invalid Media Address – A read-only bit set to indicate that either the track or sector address was not within the range of valid addresses. This condition sets ERR (bit 15) and DONE (bit 07) of the RXCS.
00	INIT DONE	Initialize Done – A read-only bit set at the completion of the initialize routine.

6.6.3 Disk Controller Track and Sector Register (RXSA)

The RXSA is programmed with the appropriate track and sector address information indicating where the data is to be written on or read from the disk. Table 6-24 describes the formats for each address.

6.7 LINE TIME CLOCK (LTC)

The line time clock provides a realtime indication to the program at 16.6 ms intervals. The line time clock initiates an interrupt request every 16.6 ms, provided the INT ENB (bit 06) of the TCSR (shown in Figure 6-11) is set. A program reset instruction from the microprocessor will enable the LTC by setting the INT ENB bit. Table 6-25 defines the bits associated with the TCSR. The LTC can be disabled by the function switch S1-2 on the Peripheral module. Refer to Table 3-4 for the S1 switch settings.

Table 6-24 Disk Controller, RXSA Bit Descriptions

Bit	Name	Description
15	Always 0	
14–08	TRK SEL	Track Select – Seven read/write bits used to select one of the 77 tracks ($0–114_8$) on the disk for the read or write function selected.
07–05	Always 0	
04–00	SECT SEL	Sector Select – Five read/write bits used to select one of the 26 sectors ($1–32_8$) of each track on a disk for the read or write function selected.

Table 6-25 Line Time Clock Control/Status Register (TCSR)

Bit	Name	Description
15–07	Not Used	
06	INT ENB	Interrupt Enable – Set by the program to allow an interrupt request to be generated every 16.66 ms. Set by the INIT signal.
05–00	Not Used	

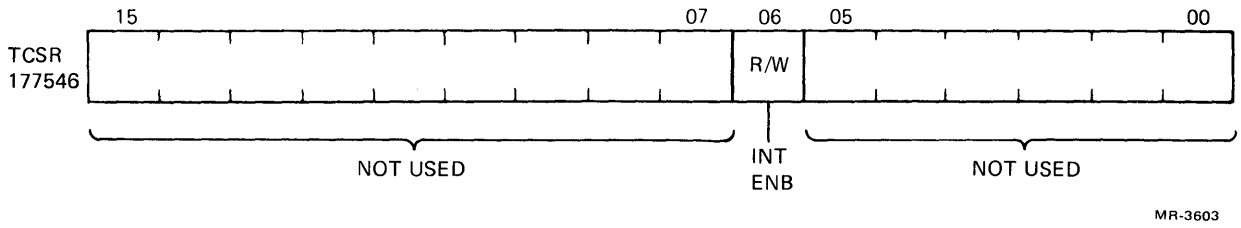


Figure 6-11 Line Time Clock (TCSR) Format

APPENDIX A
PDT-11/150 COMPONENT PART LIST

DIGITAL Part No.	Description
	Cable Assemblies
17-00083-09	ac power cord (120 V)
17-00083-10	ac power cord (220 V) USA
17-0083-02	ac power cord (220 V) Europe
70-08612-OM	16-conductor cable assembly
70-13370-OH	24-conductor cable assembly
70-15989-00	Extender cable assembly (disk drive 1)
70-15957-00	ac cable assembly (power supply)
70-15956-00	ac cable assembly (disk drives 60 Hz, 120 V)
70-16370-00	ac cable assembly (50 Hz, 90-120 V)
70-16371-00	ac cable assembly (50 Hz, 100-132 V)
70-16372-00	ac cable assembly (50 Hz, 180-240 V)
70-16363-00	ac cable assembly (50 Hz, 200-264 V)
70-15953-00	dc cable assembly
	Miscellaneous Hardware
90-09670-00	Nylon standoff (power supply)
90-09747-01	Nylon standoff (disk controller module)
90-10055	Nylon latch plunger
90-10056	Nylon latch grommet
70-15970-00	RH hinge bracket
70-15970-01	LH hinge bracket
90-09903	Rubber feet
	TIM Group
54-13271	Intelligence module W/O ROM IC
54-13273	Disk Controller module
54-13269	Peripheral module
54-13275-AA	8K RAM module W/O ROM IC
54-13275-BA	16K RAM module W/O ROM IC
54-13275-CA	32K RAM module W/O ROM IC
23-043E2	Controller ROM 0 for 54-13271
23-042E2	Controller ROM 1 for 54-13271
23-039E2	Controller ROM 2 for 54-13271
23-032F3	Bootstrap ROM 0 for 54-13275-AA, -BA, -CA
23-033F3	Bootstrap ROM 1 for 54-13275-AA, -BA, -CA
12-15230	Module stacking connector

EIA Converter Modules

54-13267	Standard EIA Converter module
54-13427	Cluster EIA Converter module W/USARTs

Rear Panel Components

12-13185	Fan
12-15232	Power switch
12-15492	EMI line filter
12-12893	Fuse holder

Power Supply

54-13343	Power supply module
16-15567	Autotransformer (50 Hz)

Disk Drive

70-13077-02	Disk drive assembly (60 Hz)
12-14005-00	Spindle drive belt (60 Hz)
12-14005-01	Spindle drive belt (50 Hz)
74-18534-00	Spindle pulley (50 Hz)

Enclosure

12-15476	Top cover assembly
12-15475	Front bezel assembly
74-20980	Rear panel, drive 0
74-20981	Rear panel, drive 1
74-20984	Disk drive enclosure
74-21086	Bottom cover panel

Accessories

36-12408	Preformatted flexible disks
93-06353-02	Drive belt spacer gauge (60 Hz disk drive)
93-06353-03	Drive belt spacer gauge (50 Hz disk drive)
74-16464	EIA loopback connector

APPENDIX B
GLOSSARY AND NOTATION

Auto Baud – A program-controlled function that sets the baud rate of the console USART to be compatible with the console terminal.

Bank 0 or Bank 1 – A sectioned area of RAM memory on the RAM module consisting of a group of ICs.

Bootstrap ROM – A ROM on the RAM module that contains the bootstrap loader program.

Break key – A key on the peripheral device keyboard that halts the program operation of the LSI-11 microprocessor.

Cluster EIA module – A printed circuit board that contains the EIA/TTL level converters and 25-pin connectors for terminals no. 1, no. 2, and no. 3.

Data Field – The area of a track on the flexible disk where the data information is recorded.

DEVM (Device Map) – A listing of options used to specify the tests to be performed during the system exerciser program.

Disk Controller module – A printed circuit board that contains the 8085 controller microprocessor and provides an interface to the disk drives.

EIA (Electronic Industries Association) – A standard (RS-232-C) which defines the signals used between data terminal equipment and data communications equipment.

Exerciser Compatibility test – A test performed to verify that the information written on a flexible disk in one disk drive can be read by another disk drive.

Fast DIN cycle – A fast data input cycle of the LSI-11 microprocessor used to monitor special functions within the PDT-11/150.

Function switch – A bank of five switches on the peripheral module used to enable or disable specific PDT-11/150 functions.

Index hole – A hole in the flexible disk used to indicate the speed of rotation and to synchronize the recording and reading of data on the disk.

Intelligence module – A printed circuit board that contains the LSI-11 microprocessor IC set and the 8085 I/O microprocessor.

Loopback connector – An optional device that attaches to the device connectors on the rear panel of the PDT-11/150 when performing the loopback test.

Loopback test – A test that transmits and receives data for validation through the USART registers or through the loopback connector.

LPCSR (Line Printer Control/Status Register) – A 16-bit register used to select control functions and to indicate the status of the printer during transient operations of the line printer.

LPDSR (Line Printer Data Buffer Register) – A 16-bit register that stores the data to be transmitted to the line printer.

LSI-11 – A 16-bit microprocessor consisting of four 40-pin ICs on the Intelligence module.

LTC (Line Time Clock) – A frequency standard that causes a realtime event interrupt of the LSI-11 microprocessor to occur every 16.6 ms.

Mode switch – A three-position switch on the rear panel used to select normal operation, the self-test program, or to reset the PDT-11/150.

ODT (Octal Debugging Technique) – A program that allows the operator access from the console keyboard to internal registers.

PARCSR (Parameter Control/Status Register) – A 16-bit USART register used to select the operating parameters for the transfer of data to and from the modem during the synchronous mode of operation.

PASS – The completion of a sequence of program tests.

PDT-11V03 – An LSI-11 microprocessor based system that contains two flexible disk drives.

Performance tests – A series of tests used to evaluate the performance of the PDT-11/150.

Peripheral module – A printed circuit board that contains the USARTs ICs for standard and optional devices.

RAM module – A printed circuit board that contains the resident RAM and the bootstrap ROM for the LSI-11 microprocessor.

RBUF (Receiver Data Buffer) – A 16-bit USART register that receives the data character to be printed or displayed by a device.

RCSR (Receiver Control/Status Register) – A 16-bit USART register used to select control functions or to indicate the status of a device.

RT-11V3 – A realtime operating system used for program development and on-line applications.

RXCS (Disk Drive Control/Status Register) – A 16-bit register on the Disk Controller module.

RXCSR (Receiver Control/Status Register) – A 16-bit USART register used during synchronous modem operations to select control functions and indicate the status of the receiver. Used to select control functions or to indicate the status of the disk drives.

RXDB/RXES (Disk Drive Data Buffer) – A 16-bit general purpose USART register used to select control functions or to store data from a device during receive operations.

RXDBUF (Receiver Data Buffer Register) – A 16-bit USART register used during synchronous modem operations to store the data received from the modem.

RXSA (Track and Sector Register) – A 16-bit register in the Disk Controller module used to select the location of the data to be written or read from the flexible disk.

Scratch Floppy – A preformatted flexible disk that contains no data or data no longer required.

Self-Test – A diagnostic program stored in ROM that functionally tests the operation of the PDT-11/150.

Standard EIA module – A printed circuit board that contains the level converters and connectors for the console, modem, and line printer devices.

System Exerciser (CVKDAB) – A sequence of programs available on flexible disk and used to test functionally the operation of the PDT-11/150.

System Program – Any of a series of stored programs that, when entered into the PDT-11/150, will perform specific functions.

SWR (Switch Register) – A register used to control the output indications when the system exerciser programs are being performed.

TIM Group Assembly – A group of three printed circuit boards consisting of the Intelligence module, the RAM module and the Peripheral module.

TXCSR (Transmitter Control/Status Register) – A 16-bit register used during synchronous modem operations to select control functions and to indicate the status of the transmitter.

TXDBUF (Transmitter Data Buffer Register) – A 16-bit register used during synchronous modem operations to store the data to be transmitted to the modem.

UPCSR (USART Parameter Control/Status Register) – A 16-bit register used to select the operating parameters of the USARTs that interface to the Standard EIA and Cluster EIA devices.

XCSR (Transmitter Control/Status Register) – A 16-bit USART register used to select control functions or to indicate the status of the transmitter section of the USART.

XBUS (Transmitter Data Buffer) – A 16-bit USART register used to store the data for transmission to the device.

INDEX

INDEX

PDT-11/150 Technical Manual
EK-PT150-TM-001

Reader's Comments

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults or errors have you found in the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

☐ Please send me the current copy of the *Technical Documentation Catalog*, which contains information on the remainder of DIGITAL's technical documentation.

Name _____ Street _____

Title _____ City _____

Company _____ State/Country _____

Department _____ Zip _____

Additional copies of this document are available from:

Digital Equipment Corporation
Accessories and Supplies Group
Cotton Road
Nashua, NH 03060

Attention: Documentation Products
Telephone 1-800-258-1710

Order No. EK-PT150-TM

Fold Here

Do Not Tear — Fold Here and Staple

digital

No Postage
Necessary
if Mailed in the
United States

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 33 MAYNARD, MA.

POSTAGE WILL BE PAID BY ADDRESSEE

Digital Equipment Corporation
Educational Services Development and Publishing
200 Forest Street (MR1-2/T17)
Marlboro, MA 01752