MASTER

digital

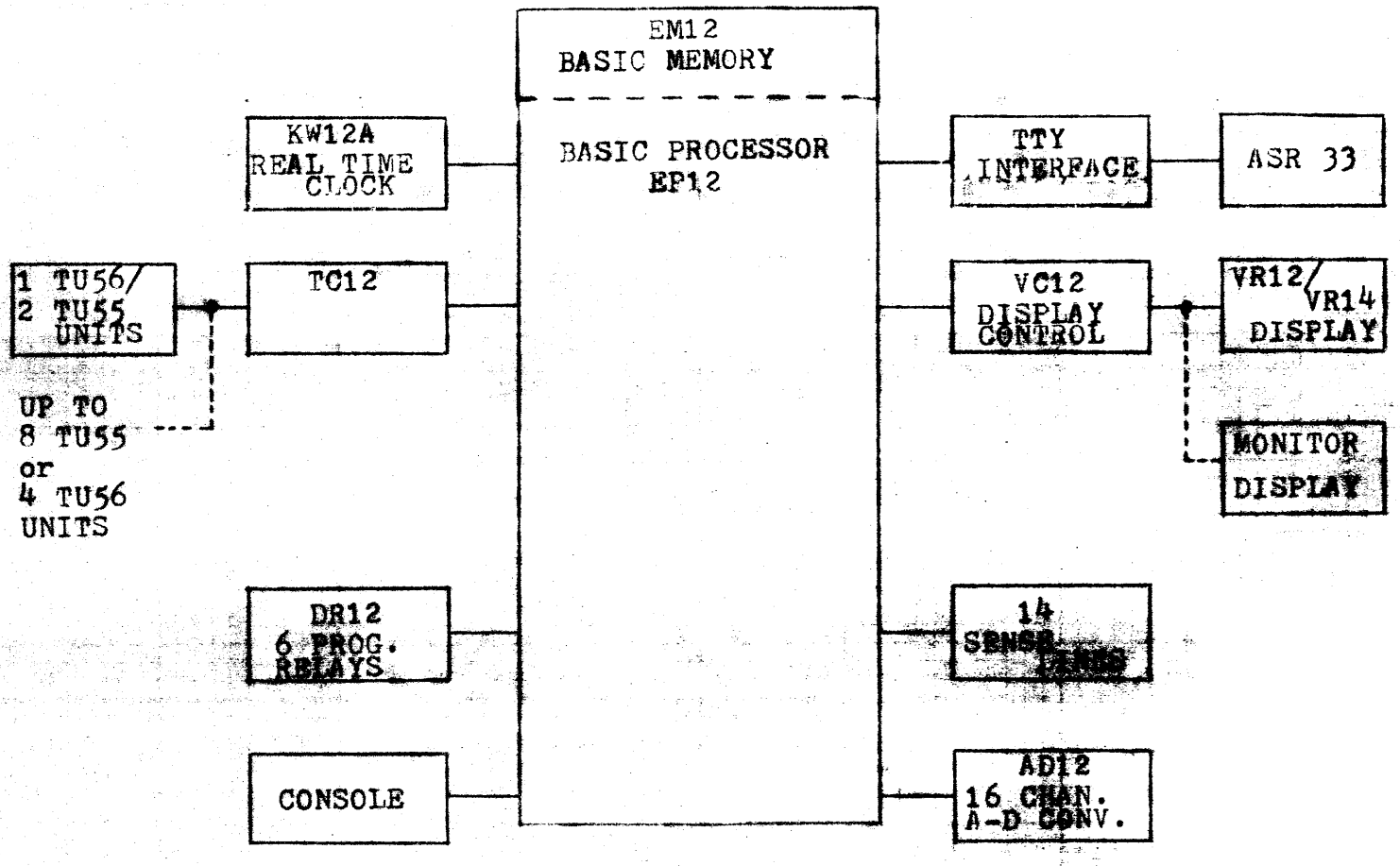
PDP 12
STUDENT HANDOUTS

PDP 12
STUDENT HANDOUTS

INDEX TO HANDOUTS

Index to Handouts -2

47. Linc Tape Block Diagram
48. PDP-12 Linc Tape Flow Diagram
49. Linc Tape
50. PDP-12 Linc Tape Format
51. Block Mark
52. Reading Block Mark (Fwd-Rev)
53. Writing on Tape
54. Linc Tape Reader-Writer Control
55. Functional Block Diagram
56. KW-12 Front Panel
57. KW-12 System
58. KW-12 Block Diagram
59. KW-12 Input Channel
60. Timing Format
61. Documentation Format
62. " "
63. " "
64. " "
65. " "
66. Mark " Tape, Copy " Tape, Print " Dial Index " Exercise
67. " " " " "
68. " " " " "
69. Dial Block Diagram
70. Linc Tape Overall Format
71. Interrupt Next Priority



PDP-12A SYSTEM BLOCK DIAGRAM

PDP-12 KEY IO PRESET

Key IO Preset kicks off manual timing if run = 0

1.

	CST	IO	PRESET	
a.		0 ⟶	IOT PAUSE	CPT
b.		0 ⟶	INTERNAL PAUSE	CPT
c.		-	CPT IO PRESET	CPT
d.		0 ⟶	DO F/F	CST
e.		1	ENABLE MEM	CST
f.		0 ⟶	FILL STEP	CST
g.		0 ⟶	AUTO	CST
h.		0 ⟶	MFTS1·MFTS2	CST
i.		0 ⟶	STEP EX	
j.		0 ⟶	FLOW	
k.		0 ⟶	LINK	FLK
l.		-	LOAD AC	RCL
m.		-	IO PRESET L	IOC
n.		-	IO PRESET	MPG
o.		-	MEM EXT N PRESET	MPG
p.		0 ⟶	RELAY	

2.

a. $\overline{\text{CPT SET TS1}}$ ⟶ 1 ⟶ CYCLE DONE (CPT)
b. 1 ⟶ TS1 (CPT)
c. 0 ⟶ TS2 — 5 (CPT)
d. 0 ⟶ RECYCLE SYNC (CPT)
e. 0 ⟶ T5 RECYCLE (CPT)
f. 1 ⟶ MEM IDLE (CPT)

3. $\overline{\text{CST KEY CONT}}$ · MFTP1

a. 0 ⟶ H (SKH)
b. 0 ⟶ SKIP (SKH)

4. IOC TO PRESET

c. 0 ⟶ ADDRESS ACCEPTED (IOC)
d. 0 ⟶ WC OVERFLOW (IOC)
e. 0 ⟶ INT ENABLE (IOC)
f. 0 ⟶ IOP FF 1-2-4 (IOC)

0 ⟶ INT DLY (IOC)

5. MPG IO PRESET

a. 0 ⟶ SF 9 (MPG)
b. SET IF to 2(8)
c. 0 ⟶ INT INHIBIT (MPG)
d. SET DF to 3(8)
e. SET IB to 2(8)

EIGHT BASIC INSTRUCTIONS

0 ——————→ 5

MEMORY REFERENCE INSTRUCTIONS MRI's

AND TAD ISZ DCA JMP JMS
0XXX 1XXX 2XXX 3XXX 4XXX 5XXX

IS MB 3 = 1 OR 0
IS MB 4 = 1 OR 0
IS MB 5 = 1 OR 0
} 2ND OCTAL DIGIT ANALOGY 0-7

MB 3 (0) = DIRECT
MB 3 (1) = INDIRECT
MB 4 (0) = PAGE ZERO
MB 4 (1) = CURRENT PAGE
MB 5 (0) = < 100 LOCATIONS
MB 5 (1) = ≥ 100 LOCATIONS

TRUTH TABLE

OCTAL	BINARY	ANALOGY
0	000	DIR, Pg. Z, <100
1	001	DIR, Pg. Z, ≥100
2	010	DIR, CUR. Pg., <100
3	011	DIR, CUR. Pg., ≥100
4	100	IND, Pg. Z, <100
5	101	IND, Pg. Z, ≥100
6	110	IND, CUR. Pg., <100
7	111	IND, CUR. Pg., ≥100

6

IN/OUT TRANSFER IOT's

IOT's FOR TRANSFER OF DATA INTO OR OUT OF COMPUTER

→ IN → OUT

KS_F KC_C KR_S KR_B TS_F TC_F TP_C TL_S

IS MB 9 (1) = IOP 4
IS MB 10 (1) = IOP 2
IS MB 11 (1) = IOP 1

GENERAL IOP USES

IOP 1 – SKIP
IOP 2 – CLEAR
IOP 4 – READ OR LOAD

7

OPERATE GROUPS OPR

GROUP I → GROUP II → GROUP III ARITHMETIC GROUP (OPTIONAL)

DECISION GROUP

CLEAR AC | SKIP | OSR | HLT

SMA SZA SNL
SPA SNA SZL

EFFECT IS ON THE AC & L

CLEAR
AC L

COMPLEMENT
AC L

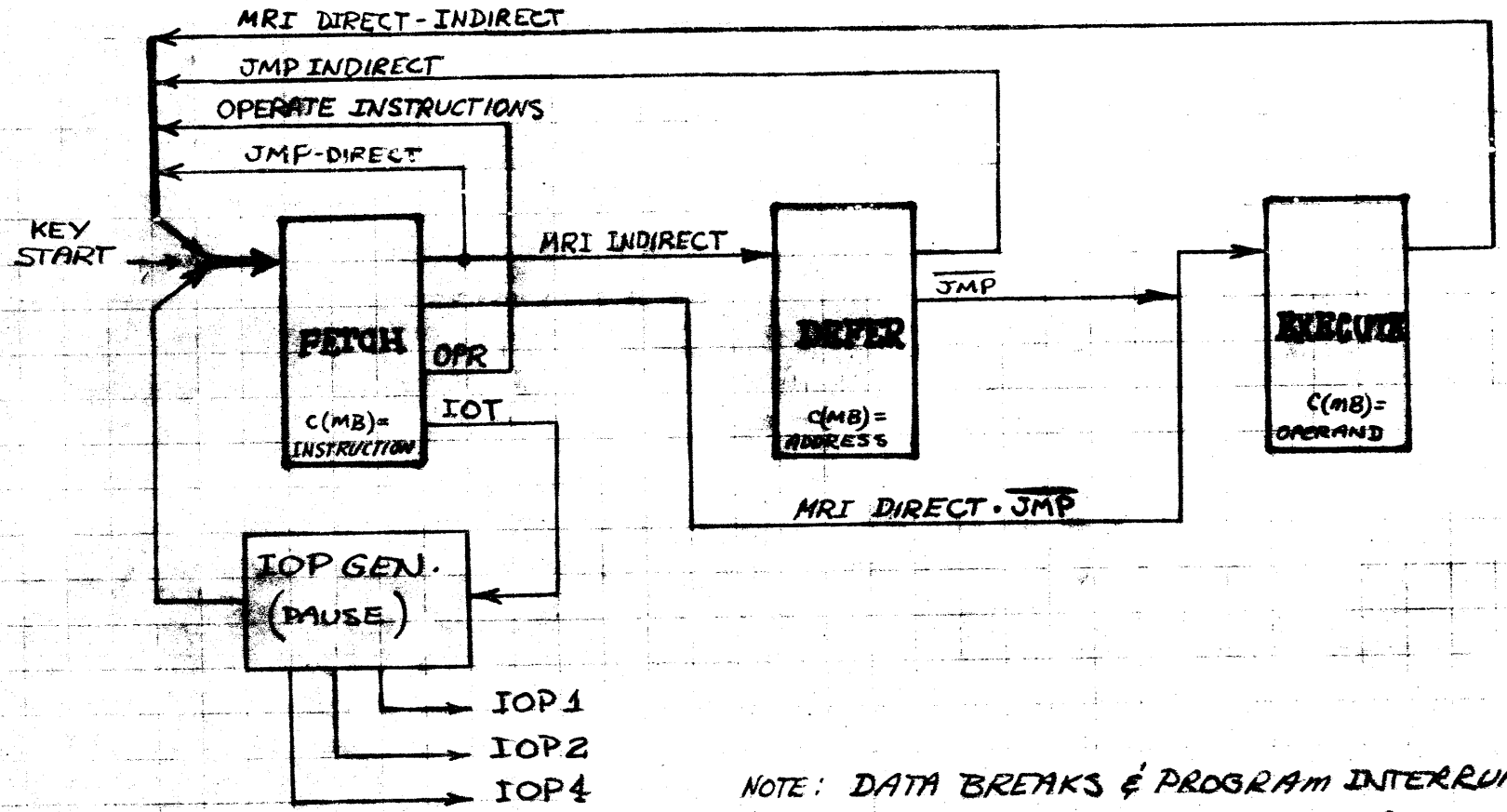
IAC

ROTATE
RIGHT 1 2
LEFT 1 2

MEMORY BUFFER
0 1 2 3 4 5 6 7 8 9 10 1

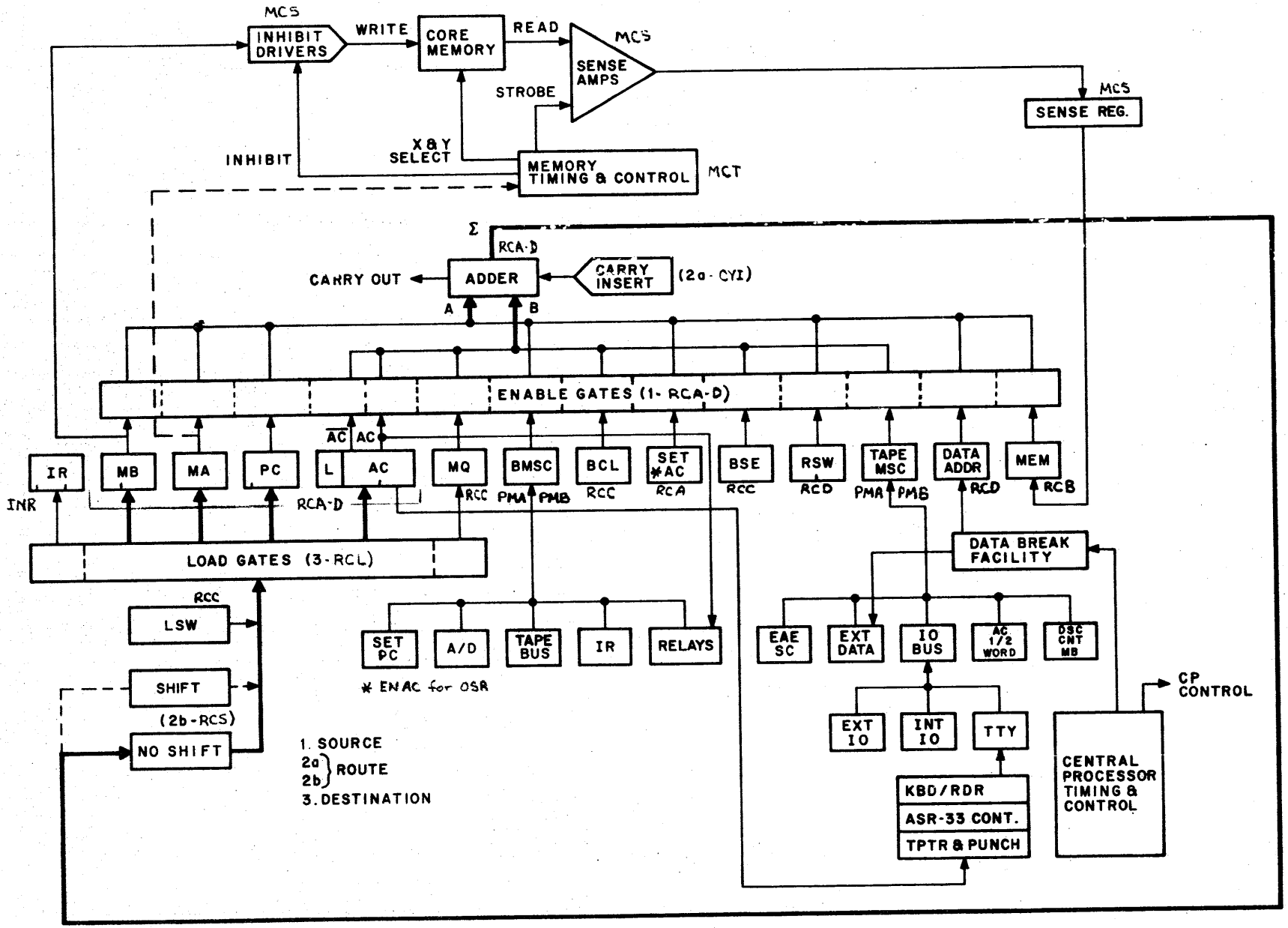
0 GP I
1 GP II
1 GP III

MAJOR STATE FLOW DIAGRAM

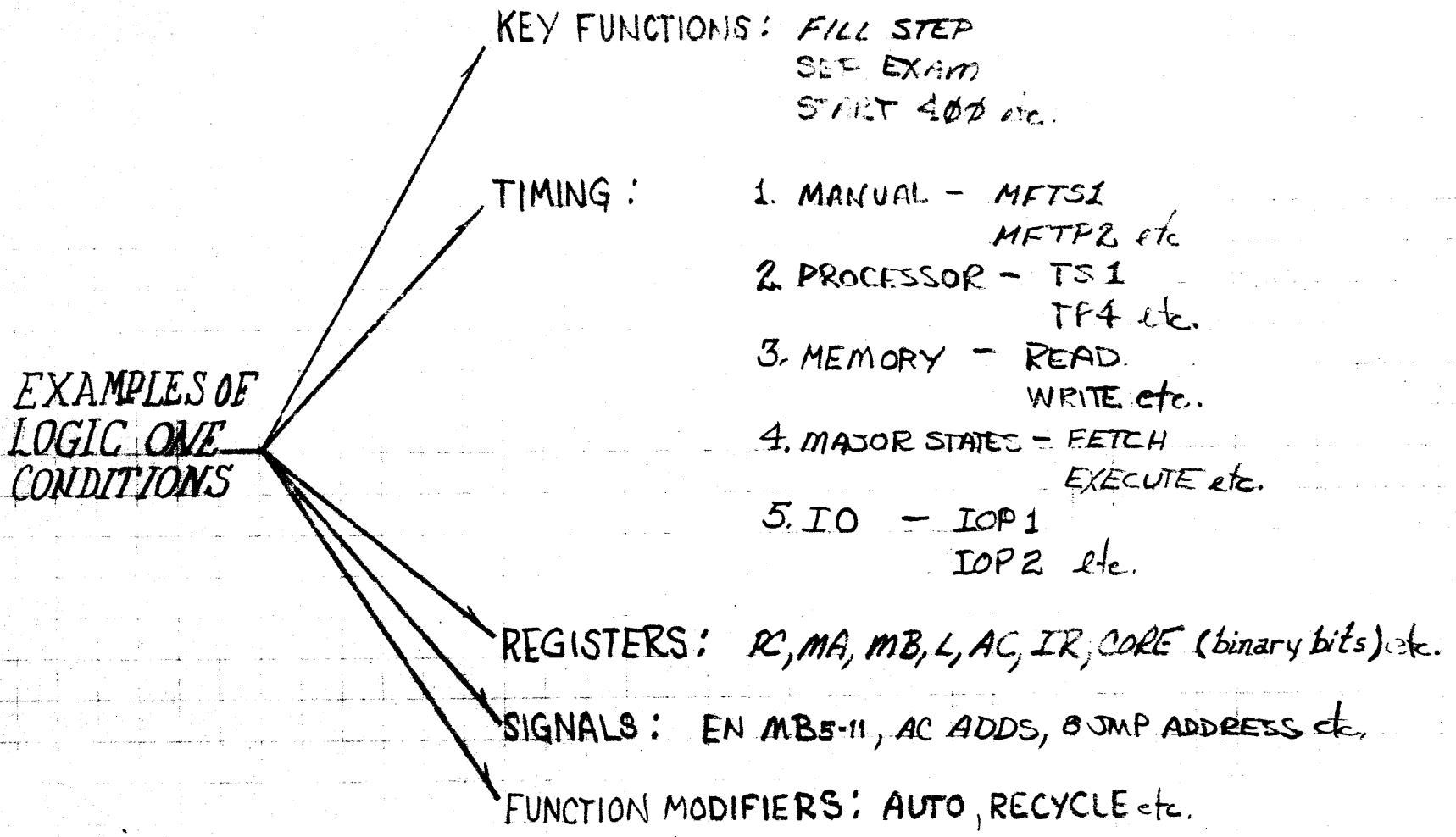


NOTE: DATA BREAKS & PROGRAM INTERRUPTS HAVE BEEN EXCLUDED FOR SIMPLICITY

PDP-12 DATA FLOW

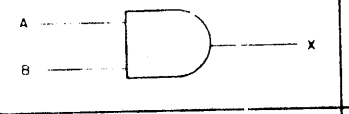
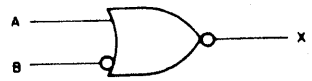
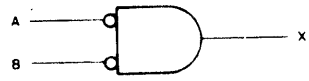
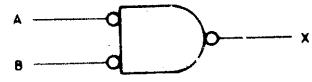
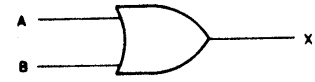
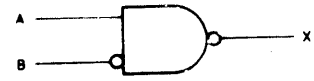
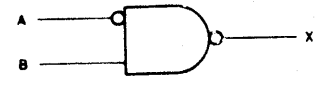
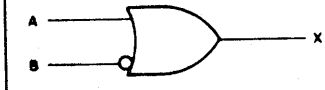
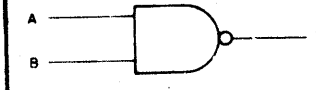
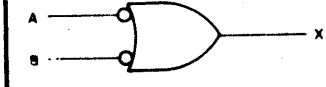


IS IT A LOGIC ONE OR ZERO ?



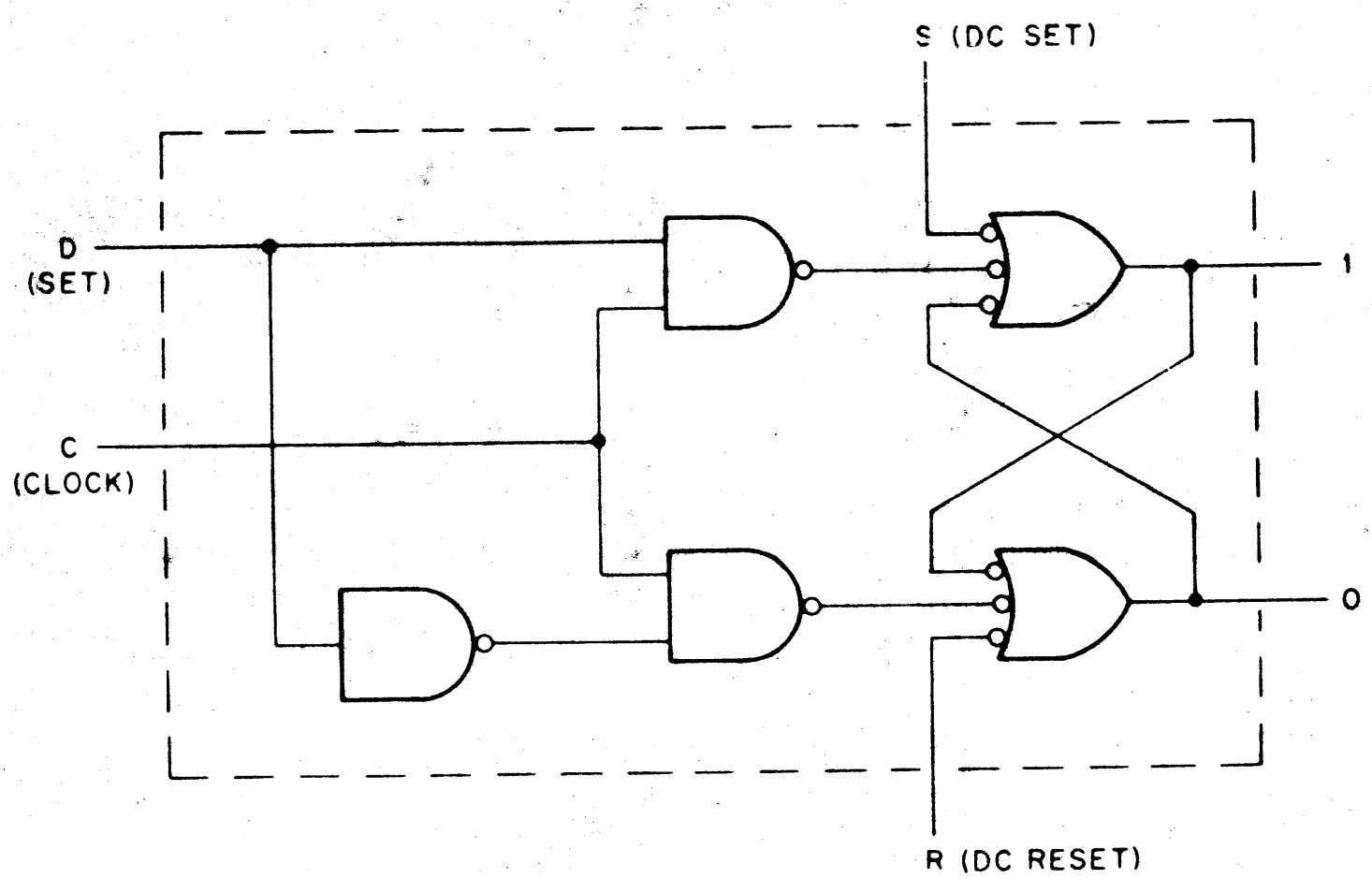
A LOGIC ONE IS A CONDITION THAT IS ACTIVE, TRUE, HAPPENING AND IS NOT NECESSARILY ANY PERTICULAR LOGIC LEVEL ie, DEC USES DUAL POLARITY DUAL DEFINED LOGIC. THEREFORE, A POLARITY INDICATOR IS REQUIRED IN ADDITION TO THE LOGIC CONDITION NAMED. CONVERSELY, A LOGIC ZERO WOULD BE AN INACTIVE, FALSE OR NEGATED CONDITION AND THE POLARITY INDICATED WOULD BE INCORRECT UNLESS INDICATED TO BE A NOT CONDITION.

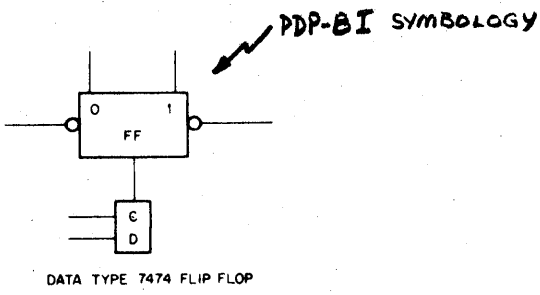
The following table of combinations illustrates the applications and functions of two variables and equivalents.

AND	OR	TABLE OF COMBINATIONS A	B	X
		H	H	H
		H	L	L
		L	H	L
		L	L	L
		H	H	L
		H	L	L
		L	H	H
		L	L	L
		H	H	L
		H	L	H
		L	H	L
		L	L	L
		H	H	L
		H	L	L
		L	H	L
		L	L	H
		H	H	H
		H	L	H
		L	H	H
		L	L	L
		H	H	H
		H	L	L
		L	H	H
		L	L	H
		H	H	H
		H	L	H
		L	H	L
		L	L	H
		H	H	L
		H	L	H
		L	H	H
		L	L	H

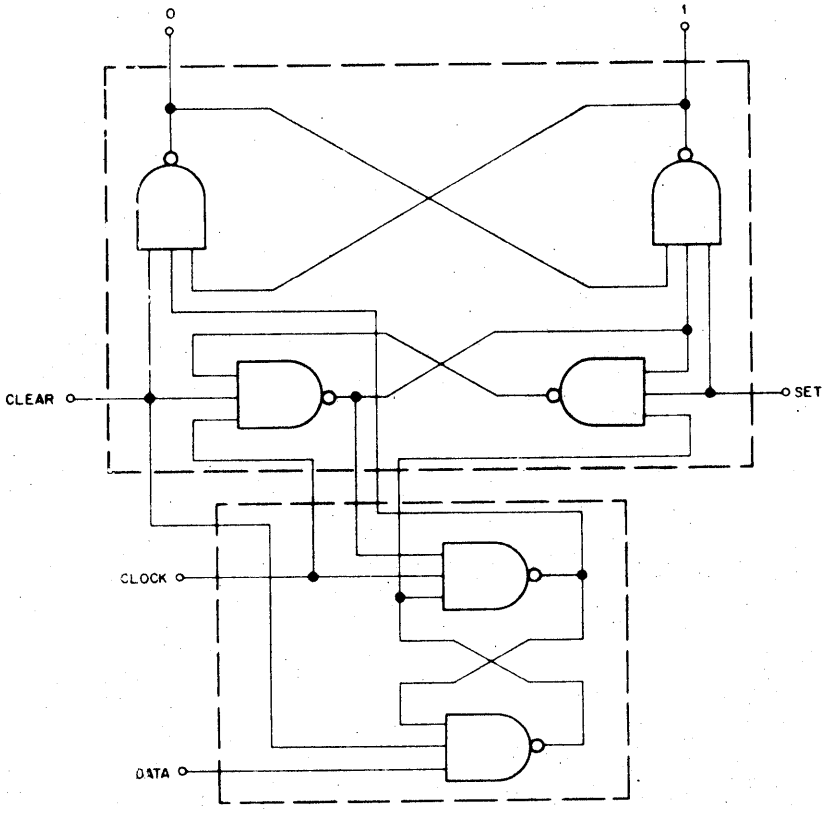
Logic Functions

SIMPLIFIED D-TYPE FLIP-FLOP

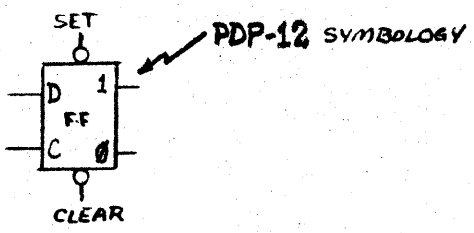


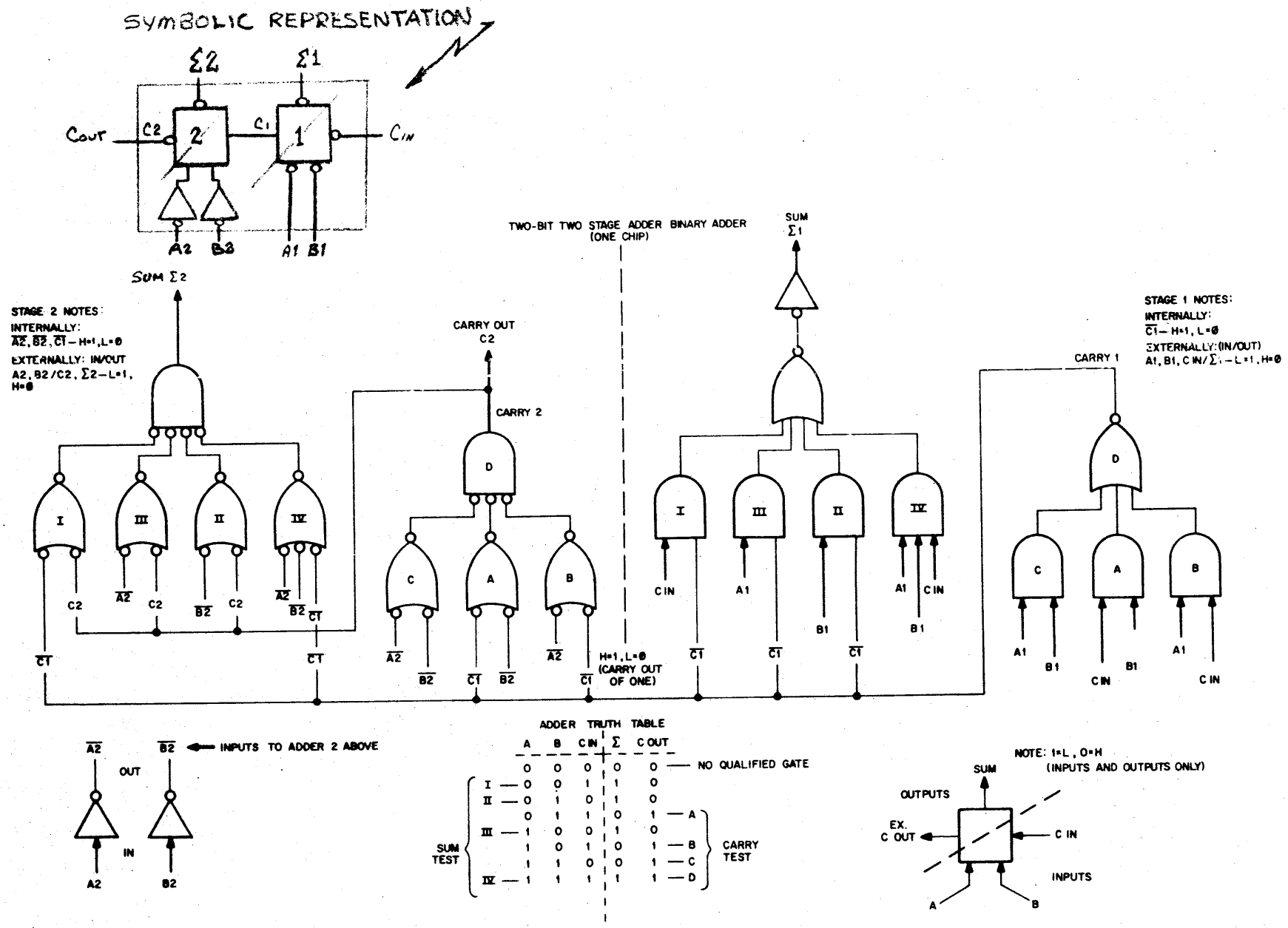


DATA TYPE 7474 FLIP FLOP



Data Type 7474 Flip-flop



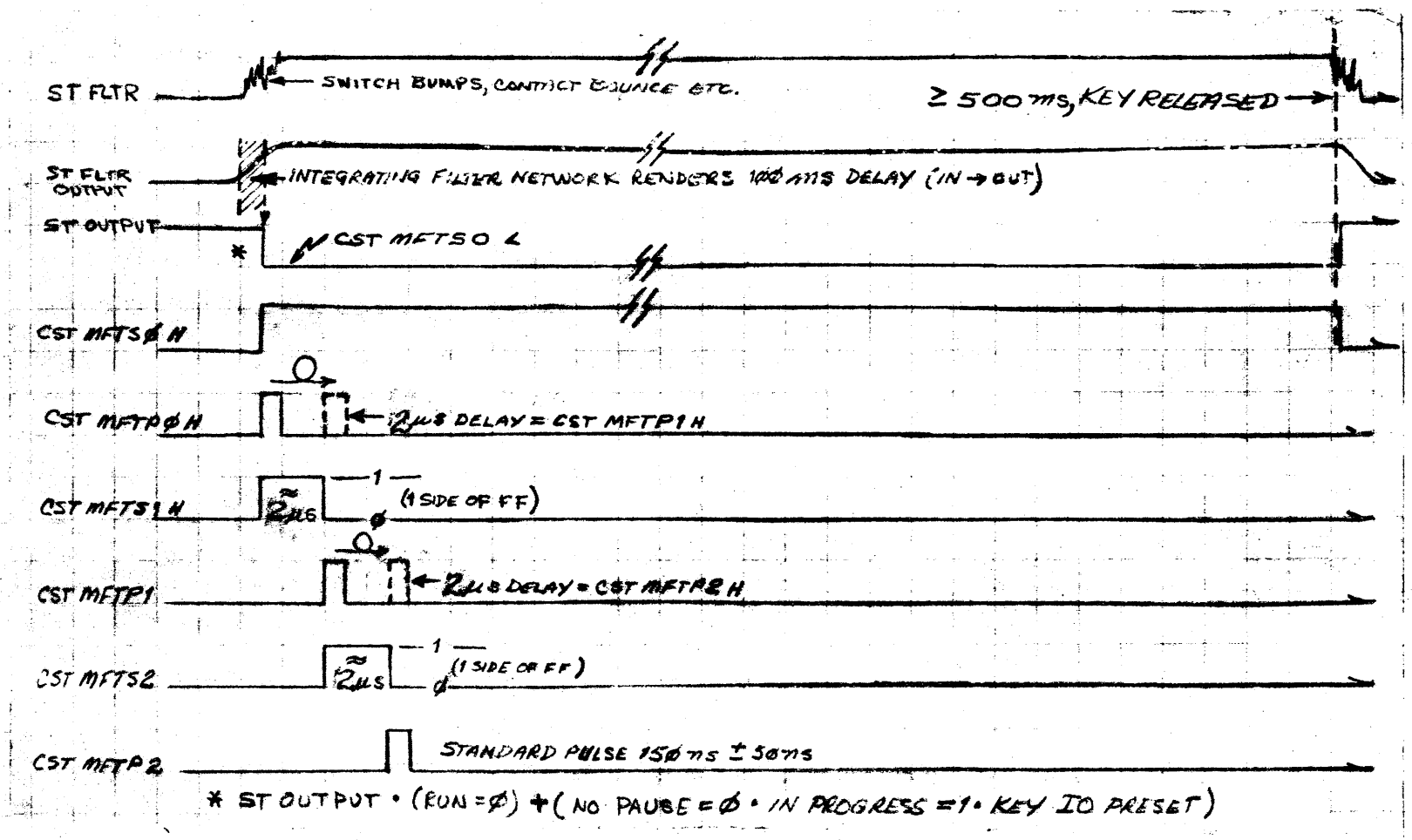


Two-Bit Two Stage Adder-Binary

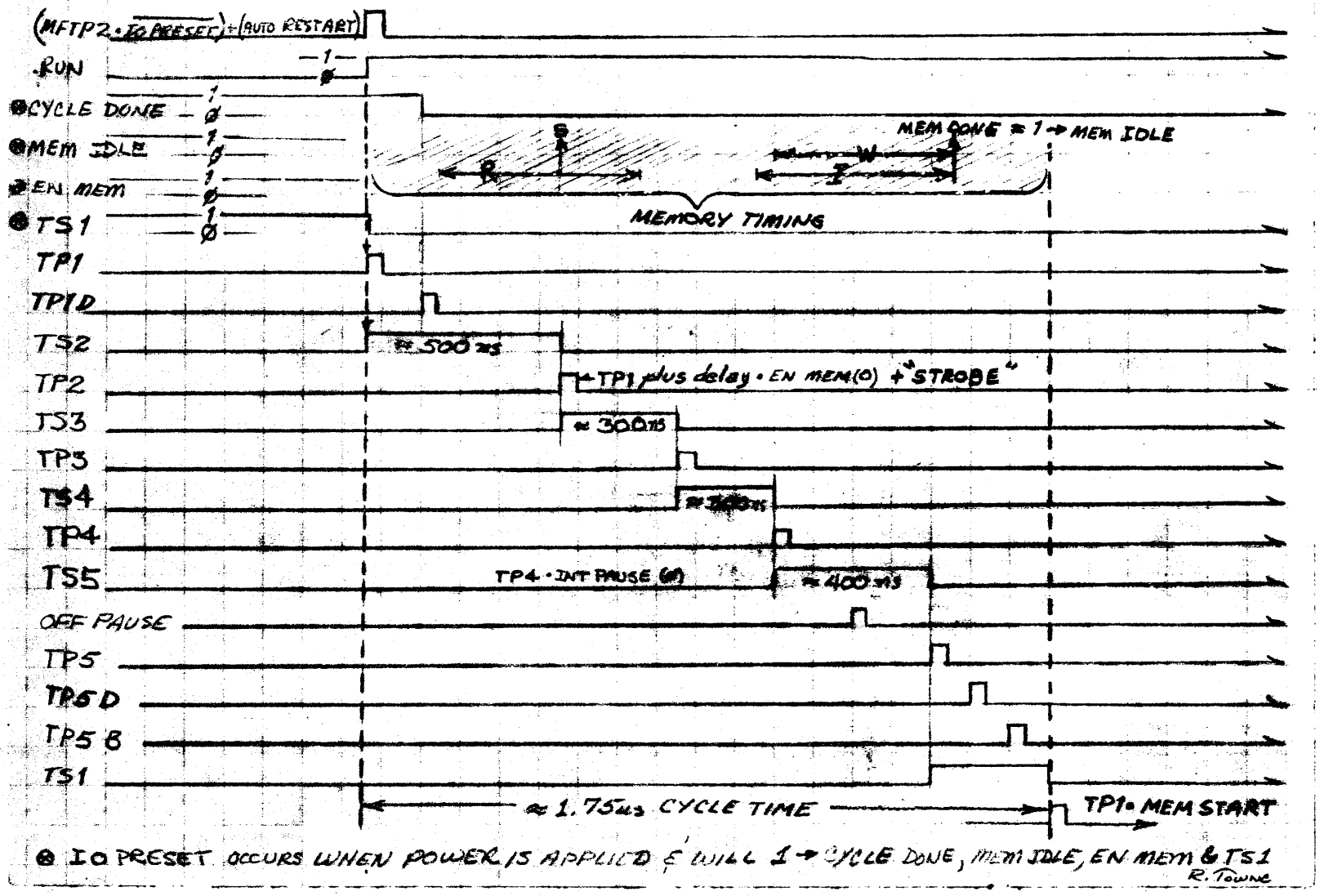
(One Chip)

ENGINEERING DRAWINGS

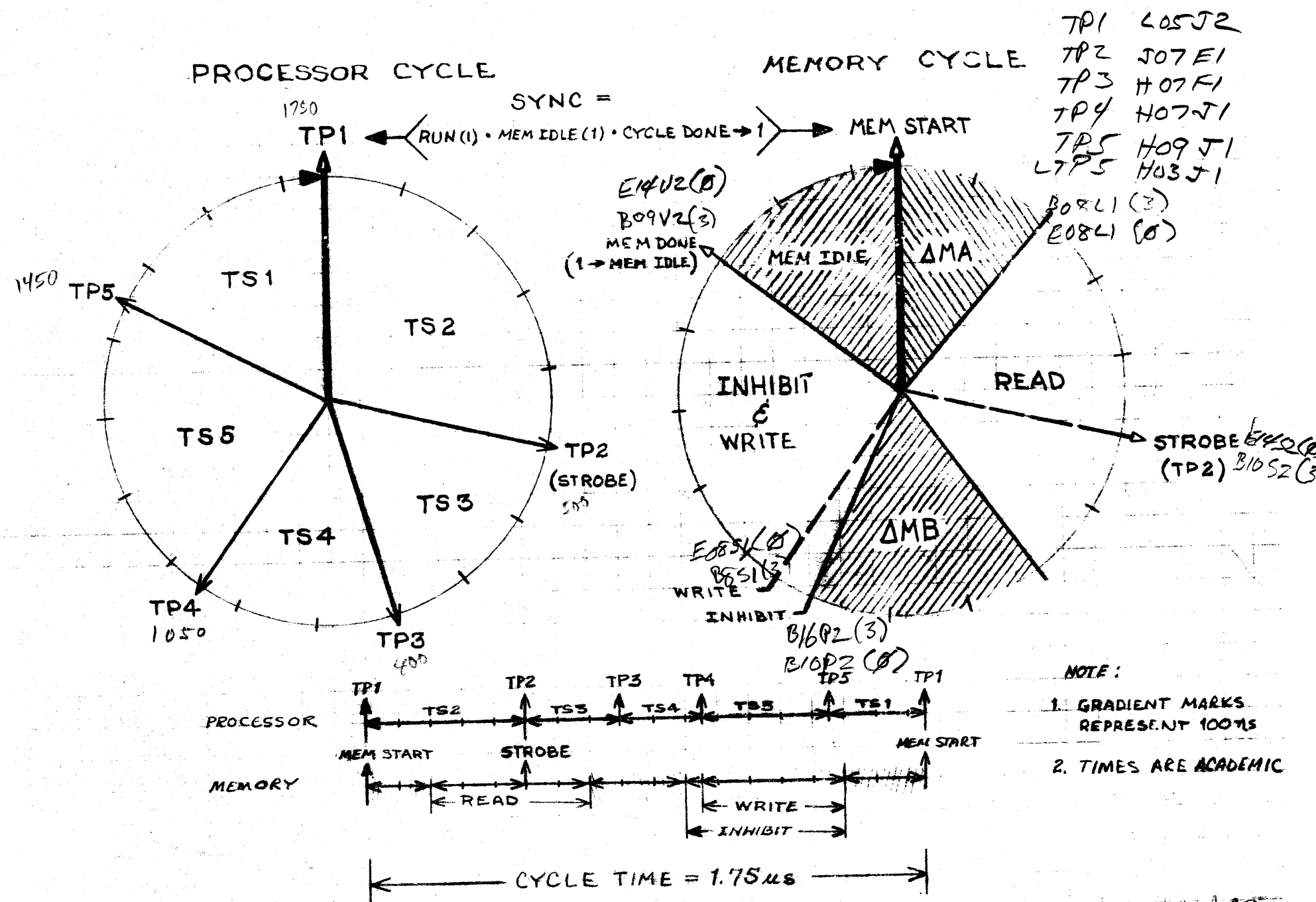
KEY OPERATIONS TIMING

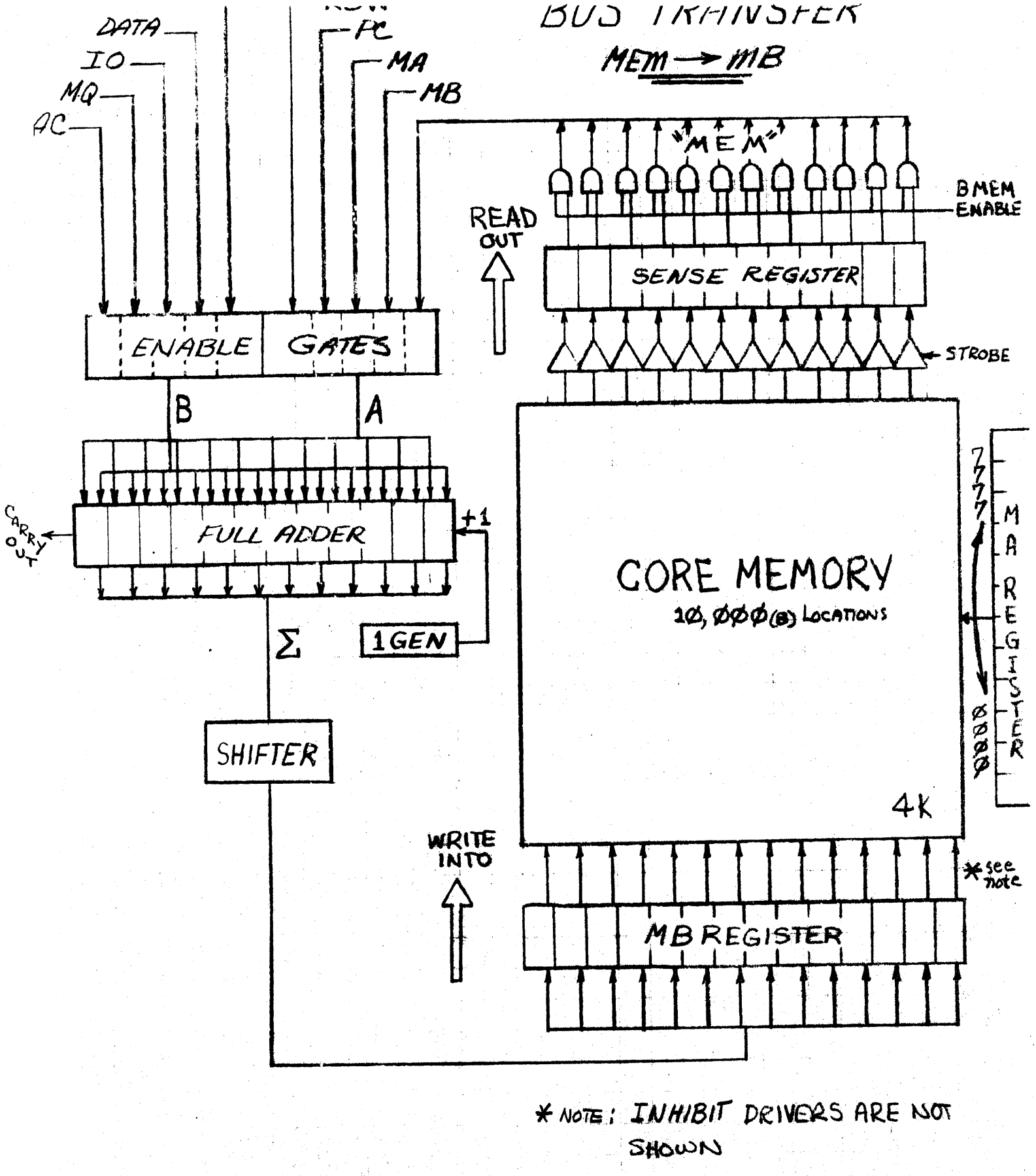


CENTRAL PROCESSOR-TIMING & RUN



CYCLE TIME

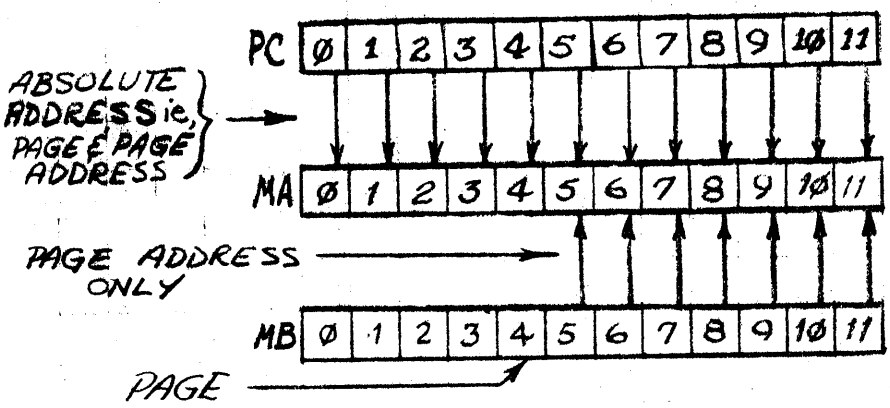

PROCESSOR CYCLE
SYNC =
RUN (1) • MEM IDLE (1) • CYCLE DONE → 1
TP1
TP2 (STROBE)
TP3
TP4
TP5
TS1
TS2
TS3
TS4
TS5
1750
1450
1050
400
MEMORY CYCLE
MEM START
MEM IDLE
ΔMA
READ
STROBE (TP2)
INHIBIT & WRITE
ΔMB
WRITE
INHIBIT
E14V2(Ø)
B09V2(3)
MEM DONE (1 → MEM IDLE)
B08L1(3)
E08L1(Ø)
E08S1(Ø)
B08S1(3)
B16P2(3)
B10P2(Ø)
TP1 L05J2
TP2 J07E1
TP3 H07F1
TP4 H07J1
TP5 H09J1
TP5 H03J1
PROCESSOR
MEMORY
TS2
TS3
TS4
TS5
TS1
MEM START
STROBE
READ
WRITE
INHIBIT
CYCLE TIME = 1.75 μs
NOTE:
1. GRADIENT MARKS REPRESENT 100 ns
2. TIMES ARE ACADEMIC

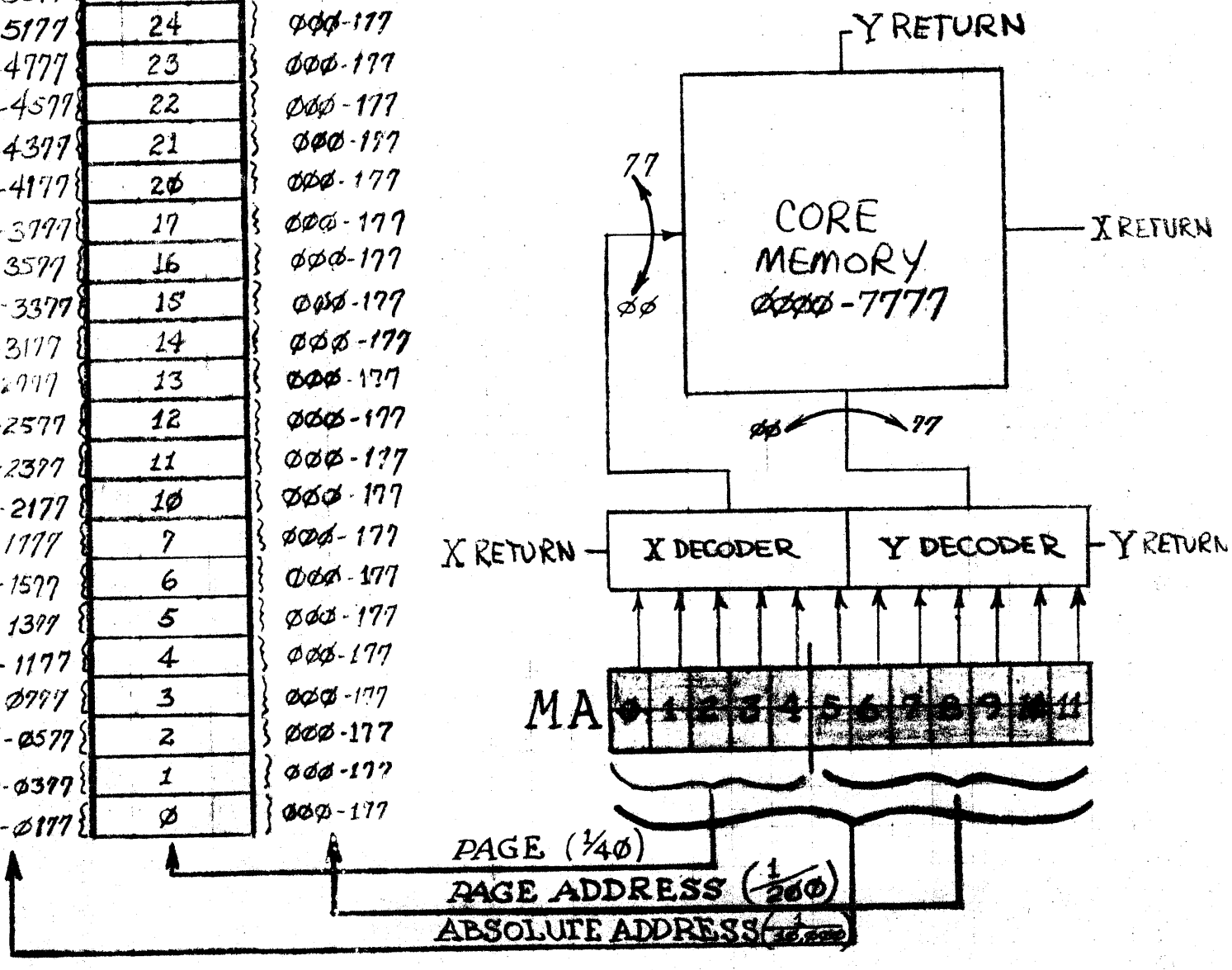


* NOTE: INHIBIT DRIVERS ARE NOT SHOWN

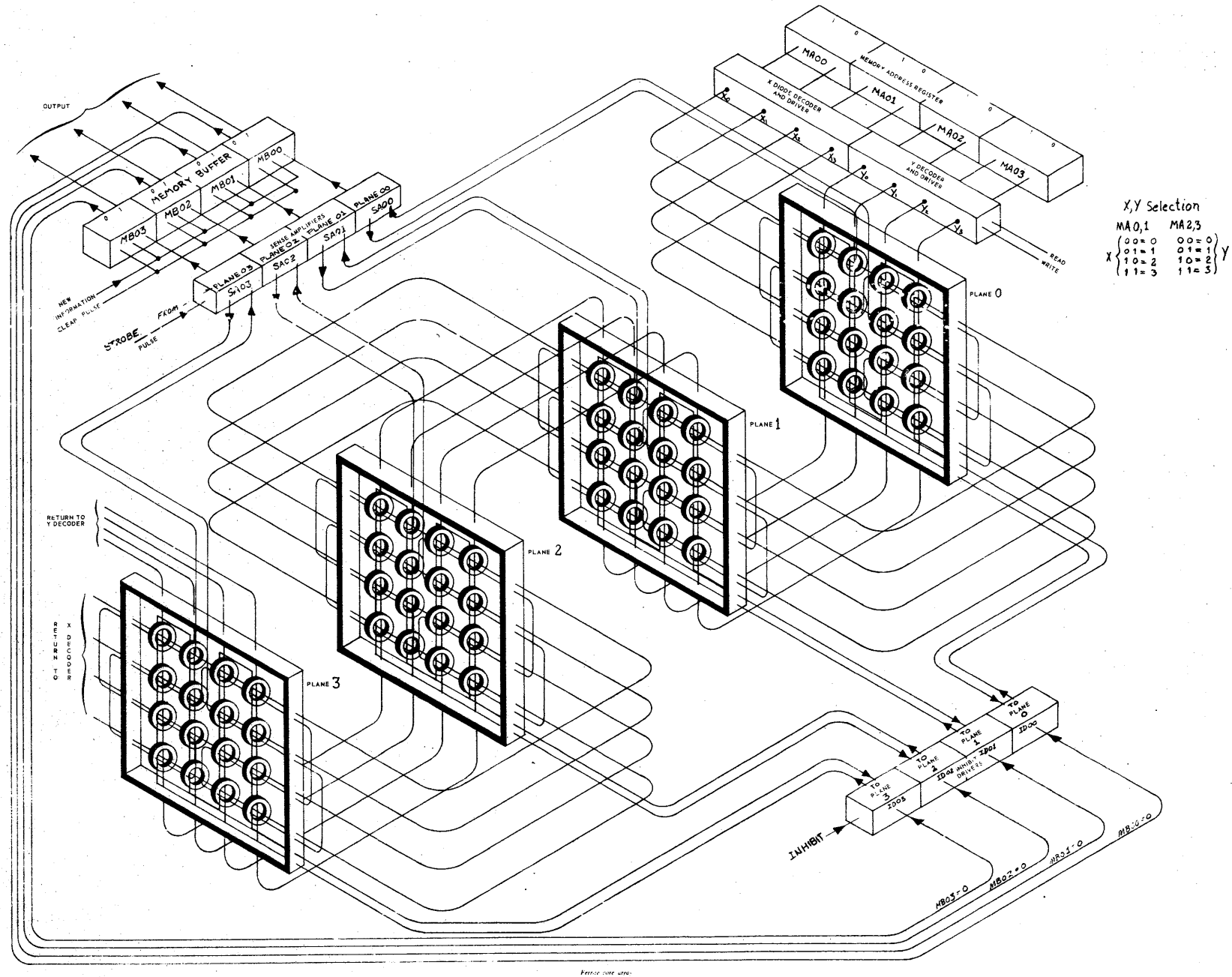
MEMORY ADDRESSING

ADDRESS	PAGE	ADDRESS
7600 - 7777	37	000 - 177
7400 - 7577	36	000 - 177
[illegible] - 7377	35	000 - 177
7000 - 7177	34	000 - 177
6600 - 6777	33	000 - 177
6400 - 6577	32	000 - 177
6200 - 6377	31	000 - 177
6000 - 6177	30	000 - 177
5600 - 5777	27	000 - 177
5400 - 5577	26	000 - 177
5200 - 5377	25	000 - 177
5000 - 5177	24	000 - 177
4600 - 4777	23	000 - 177
4400 - 4577	22	000 - 177
4200 - 4377	21	000 - 177
4000 - 4177	20	000 - 177
3600 - 3777	17	000 - 177
3400 - 3577	16	000 - 177
3200 - 3377	15	000 - 177
[illegible] - 3177	14	000 - 177
[illegible] - [illegible]	13	000 - 177
2400 - 2577	12	000 - 177
2200 - 2377	11	000 - 177
2000 - 2177	10	000 - 177
1600 - 1777	7	000 - 177
1400 - 1577	6	000 - 177
1200 - 1377	5	000 - 177
1000 - 1177	4	000 - 177
0600 - 0777	3	000 - 177
0400 - 0577	2	000 - 177
0200 - 0377	1	000 - 177
0000 - 0177	0	000 - 177





THE MA REGISTER ALWAYS CONTAINS THE ABSOLUTE ADDRESS FOR THE CURRENT MEMORY REFERENCE.

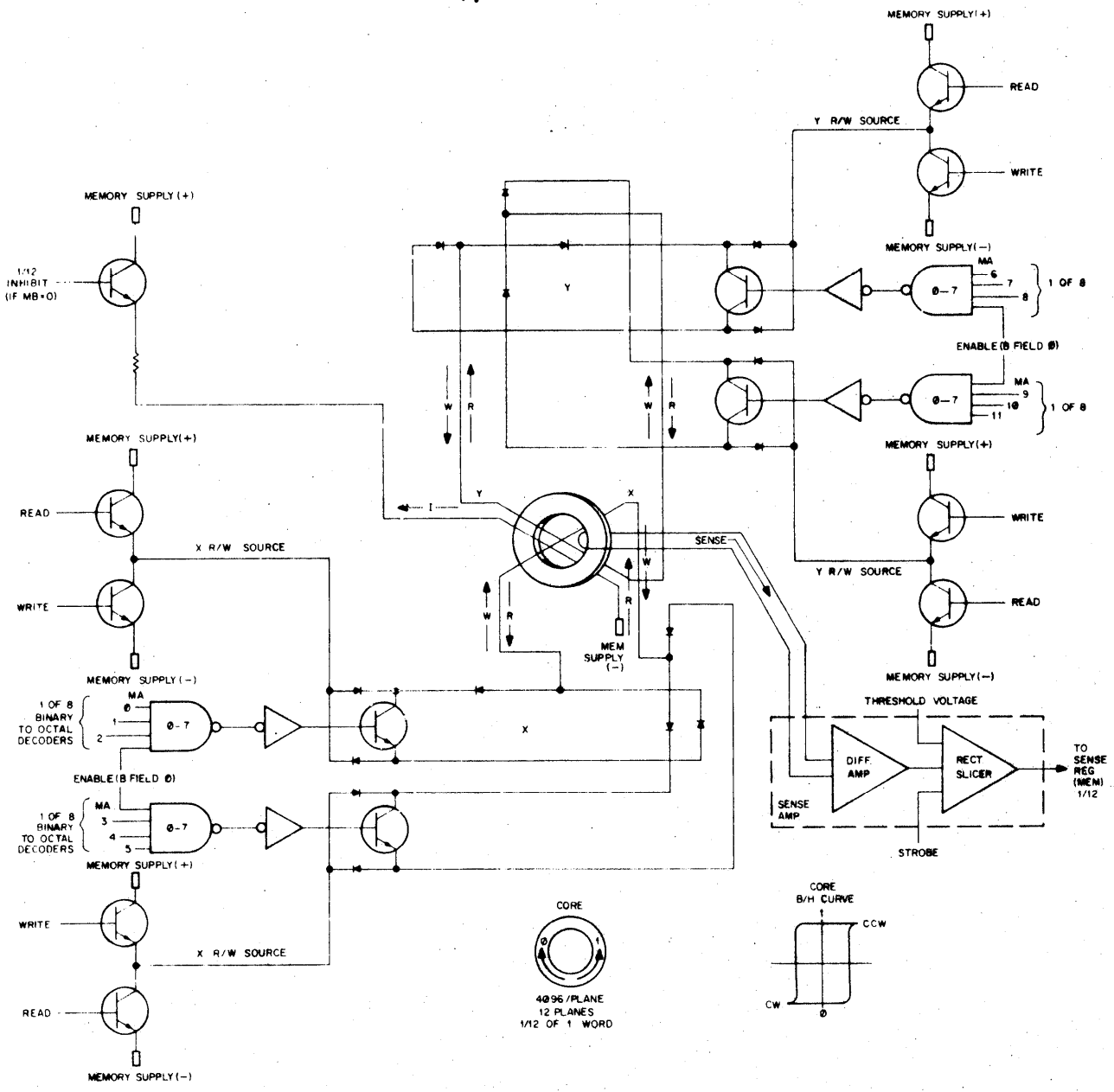


X,Y Selection

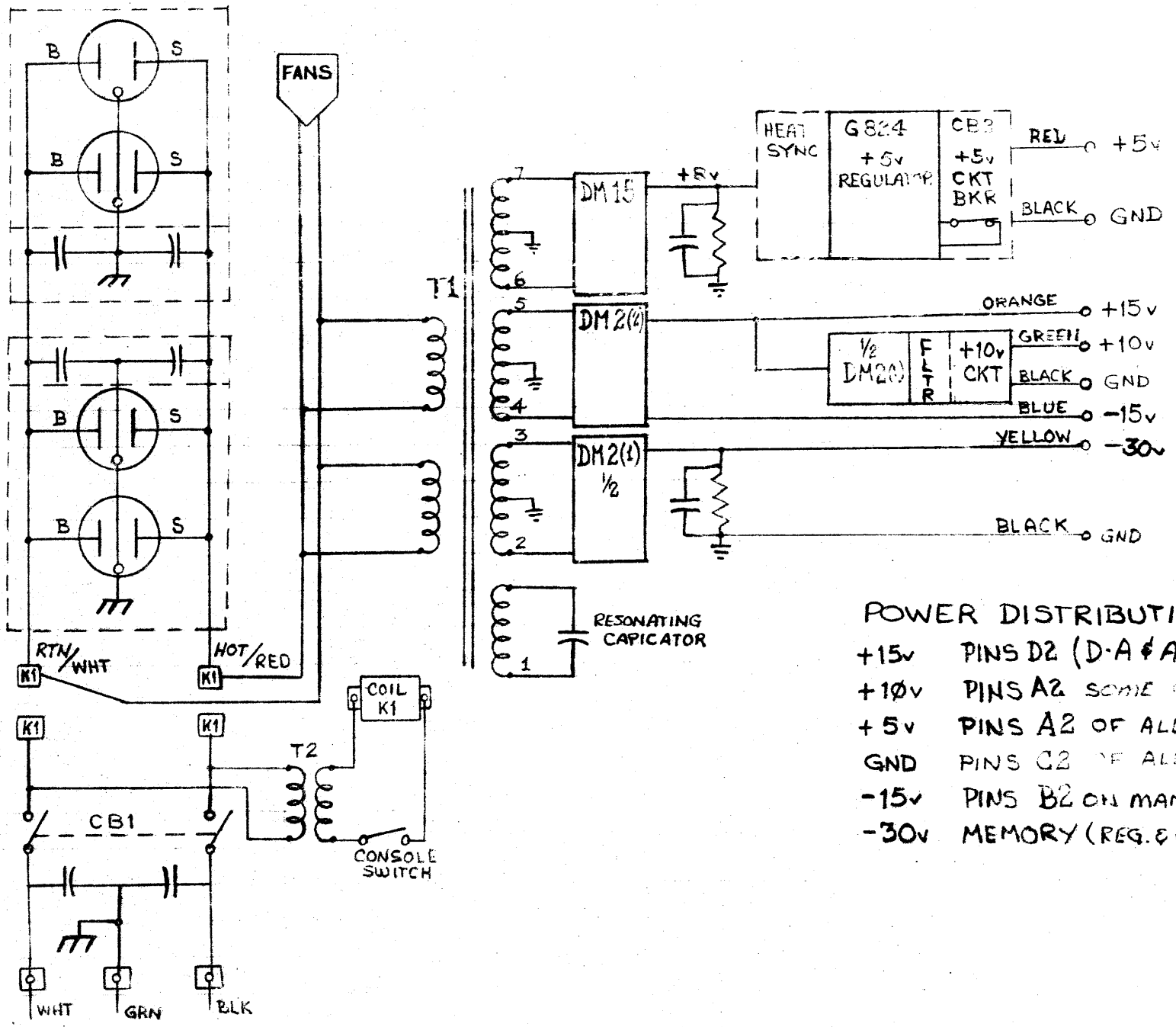
MA0,1	MA2,3	
00 = 0	00 = 0	Y
01 = 1	01 = 1	
10 = 2	10 = 2	
11 = 3	11 = 3	

X

ADDRESS SELECTION



POWER SUPPLY 724 (60 HZ)



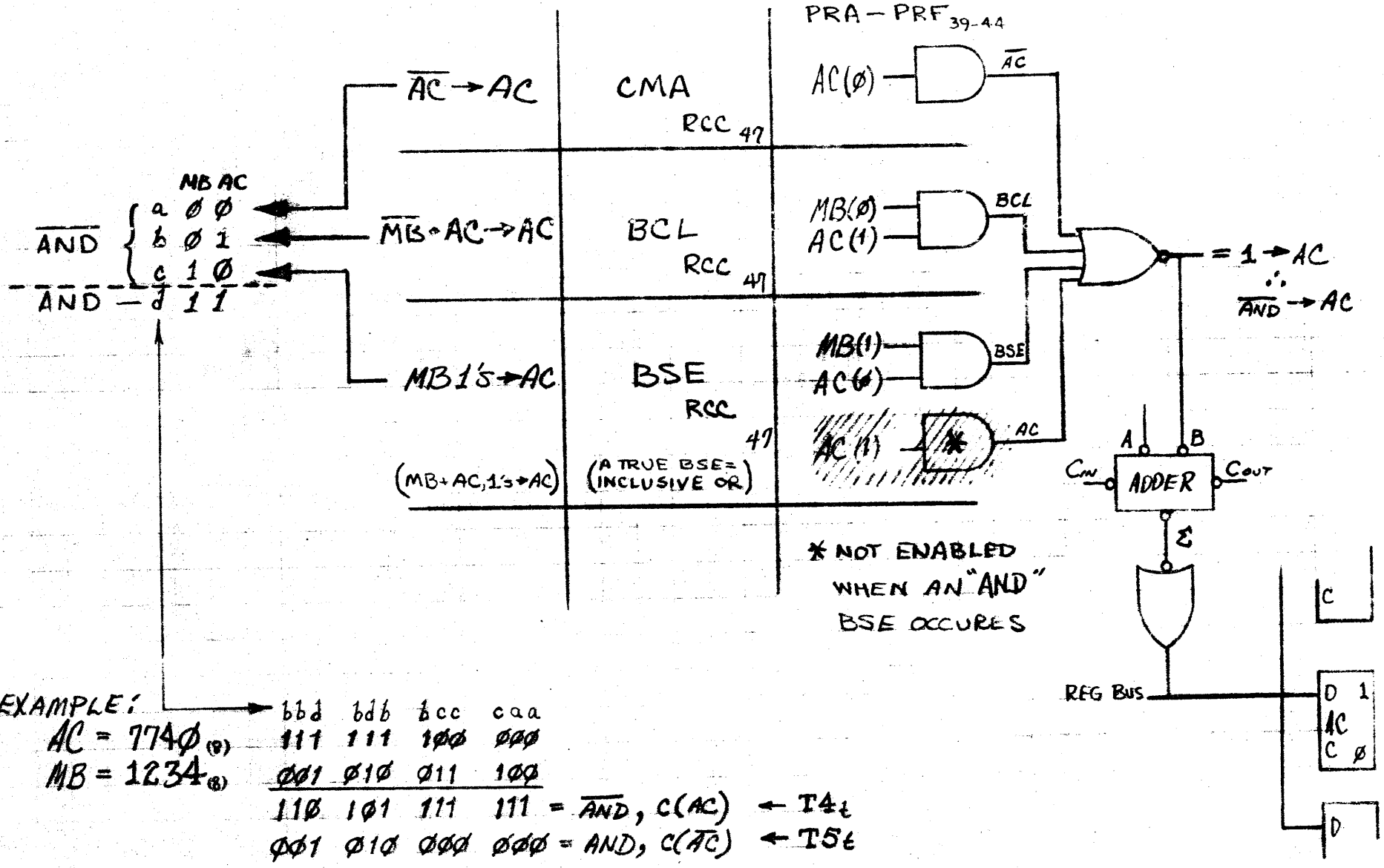
NOTE: see diagram

1. POWER WIRING & SIGNAL CABLES PDP12-Ø-3
2. POWER SUPPLY 724-Ø-1

POWER DISTRIBUTION:

+15v	PINS D2 (D-A & A-D, SCHMIT TRIG., PANEL LIGHTS
+10v	PINS A2 SOME CASES (R SERIES LOGIC & TUS
+5v	PINS A2 OF ALL LOGIC ROWS
GND	PINS C2 OF ALL LOGIC ROWS (F2, HQ GND)
-15v	PINS B2 ON MANY MODULES (TU55)
-30v	MEMORY (REG. & CONT., G-826) & TTY

"AND" INSTRUCTION LOGIC



EXAMPLE:

AC = 774Ø (8)
MB = 1234 (8)

bbd	bdb	bcc	caa	
111	111	1ØØ	ØØØ	
ØØ1	Ø1Ø	Ø11	1ØØ	
11Ø	1Ø1	111	111	= $\overline{AND}$, C(AC) ← $T4_t$
ØØ1	Ø1Ø	ØØØ	ØØØ	= AND, C($\overline{AC}$) ← $T5_t$

LINC MODE INSTRUCTIONS

SUBGROUP

FULL ADDRESS

ADD 2000
STC 4000
JMP 6000

INDEX (BETA)

LDA 1000
STA 1040
ADA 1100
ADM 1140
LAM 1200
MUL 1240
LDH 1300
STH 1300

SHD 1400
SAE 1440
SRO 1500
BCL 1540
BSE 1600
BCO 1640
NO INST 2 1700–1737 } T(32)
DSC 1740

NON-INDEX

MSC 00XX

HLT 0000
AXO 0001
PDP 0002
TAC 0003
ESF 0004
QAC 0005
DJR 0006
CLR 0011
ATR 0014
RTA 0015
NOP 0016
COM 0017
XOA 0021
TMA 0023
SFA 0024

SET 0040
SAM 0100
DIS 0140
XSK 0200
} (ALPHA)
ROL 0240
ROR 0300
SCR 0340
SXLn040n (Ø-13₈)
SNS 044n (Ø-5)
AZE 0450
APO 0451
LZE 0452
KST 0415
FLO 0454
QLZ 0455
IBZ 0453
SKP 0456
STD 0416
TWC 0417

LOPR 05XX

0501–0515 } T(15)
IOB 0500
RSW 0516
0521–0535 } T(15)
LSW 0517

NO INST 1 0540
0540–0571 } T(32)

LMB (LIF) 0600
UMB (LDF) 0640
MTP 07XX
RDE 0702
RDC 0700
RCG 0701
WRI 0706
WRC 0704
WRG 0705
CHK 0707
MTB 0703
} could be trapped

EXC 0740–0777 } T(32)

NOTE: T = Trap Codes

LINC 8 "CODE" ORIENTED FORMAT

LINC MODE

Mnemonic	Code	Operation	Direct	Indirect
		Miscellaneous		
HLT	0000	halt	3	
ZTA†	0005	Z to A$_{i-1}$ (11 bits) i equals 1 to 11	3	
ENI*†	0010	enable interrupt	N/A	
CLR	0011	clear accumulator, link, and Z register	3	
ATR	0014	(A$_6$–A$_{11}$) → R register	3	
RTA	0015	R register → (A$_6$–A$_{11}$)	3	
NOP	0016	no operation	3	
COM	0017	C(A) → C(A)	3	
SET	0040	C(p+1) → β register (or indirect)	4.5	6
SAM	0100	sample analog	19.5	
DIS	0140	display (dot)	18	
XSK	0200	skip on 1777	4.5	
		Shift		
		if i = 1 include LINK bit		
ROL	0240	rotate left	3-13.5	
ROR	0300	rotate right also shift right into Z register	3-13.5	
SCR	0340	scale right also shift right into Z register	3-13.5	
		Skip		
SXL	0400	skip if external level is −3	3	
KST	0415	skip if key has been struck	3	
SNS	0440	skip if sense switch is up	3	
PIN*†	0446	pause interrupt	N/A	
SKP	0440	skip unconditionally	3	
AZE	0450	skip if accumulator zero	3	
APO	0451	skip if accumulator positive	3	
LZE	0452	skip if link zero	3	
IBZ	0453	skip if between tape blocks	3	
FLO†	0454	skip if add overflow flag is set	3	
ZZZ†	0455	skip if bit 11 of Z register is 0	3	
		i=0 skip if condition met i=1 skip if condition not met		
		Operate		
PDP†	0513	transfer to PDP-8 programming at location contained in LINC A register		
TYP†	0514	TYPE the ASC ii character in the LINC A register on the teleprinter		
KBD	0515	read keyboard into accumulator	<200	
RSW	0516	read right switch register into accumulator	<200	
LSW	0517	read left switch register into accumulator	<200	

* Classic LINC only †Not defined in LAP 4

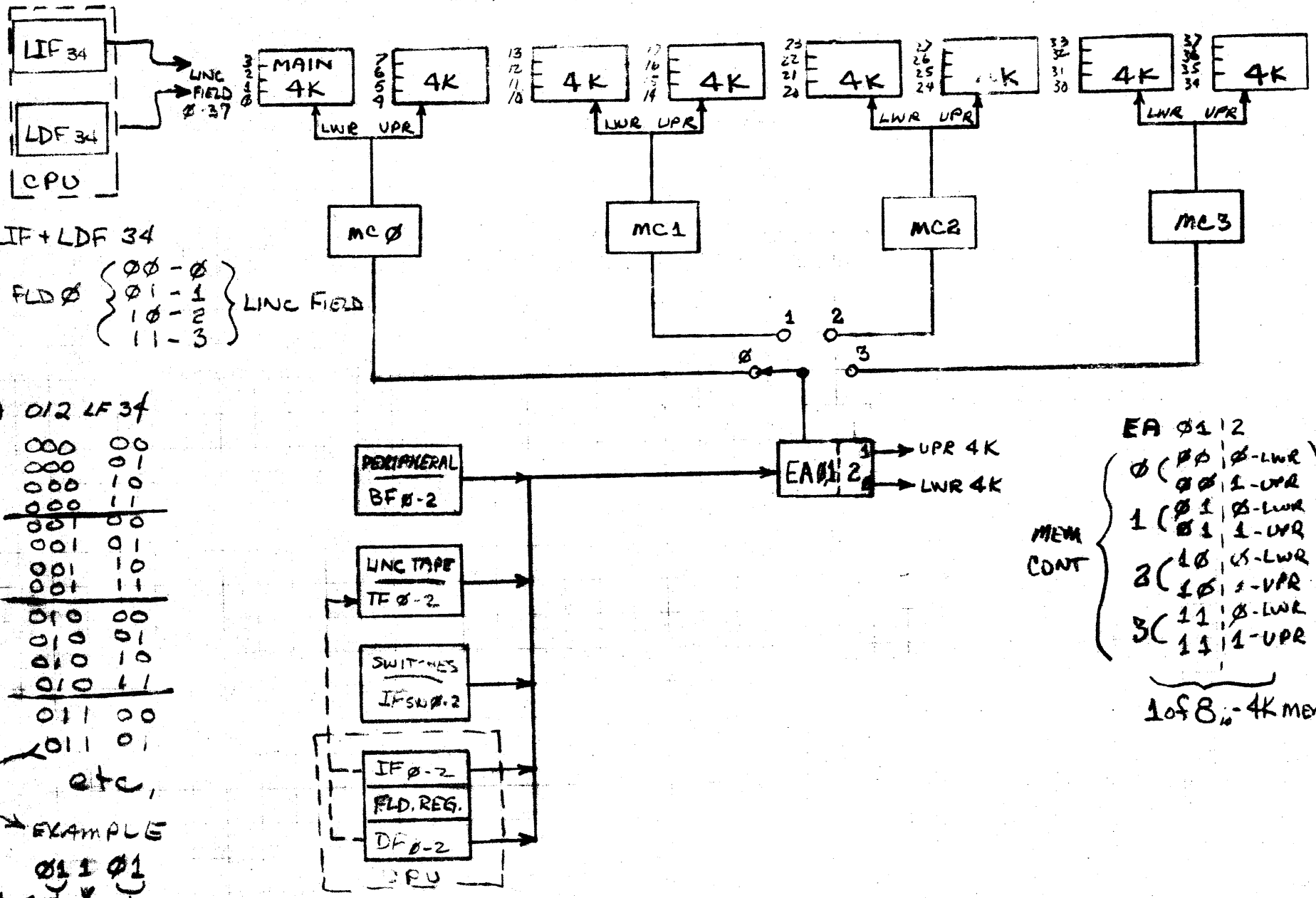
Mnemonic	Code	Operation	Direct	Indirect
		Memory Bank		
LMB †	0600	change contents of lower memory bank selector	3	
UMB †	0640	change contents of upper memory bank selector	3	
		Magnetic Tape (MTP)		
RDC	0700	read and check one block		
RCG	0701	read and check n consecutive blocks		
RDE	0702	read one block into memory		
MTB	0703	move tape toward designated block	(times depend on tape position)	
WRC	0704	write and check one block		
WCG	0705	write and check n consecutive blocks		
WRI	0706	write one block		
CHK	0707	check one block		
		i=0 stop tape after instruction i=1 leave tape in motion after instruction		
		Mode Change		
EXC †	0740	transfer to PDP-8 program control	<120 depends on PROGOFOP	
		Arithmetic		
LDA	1000	load accumulator	3	4.5
STA	1040	store contents of accumulator	4.5	6
ADA	1100	add to contents of accumulator	3	4.5
ADM	1140	add to contents of memory register	6	7.5
LAM	1200	add contents of link and accumulator to contents of memory register	6	7.5
MUL	1240	multiply	33	34.5
		Half Word Operations		
LDH	1300	transfer half word from memory into the right half of accumulator	3	4.5
STH	1340	transfer the half word from the right side of accumulator register into the designated half of a memory register	4.5	6
SHD	1400	skip if the half word in accumulator register and the memory register differ	4.5	6

†Not defined in LAP 4

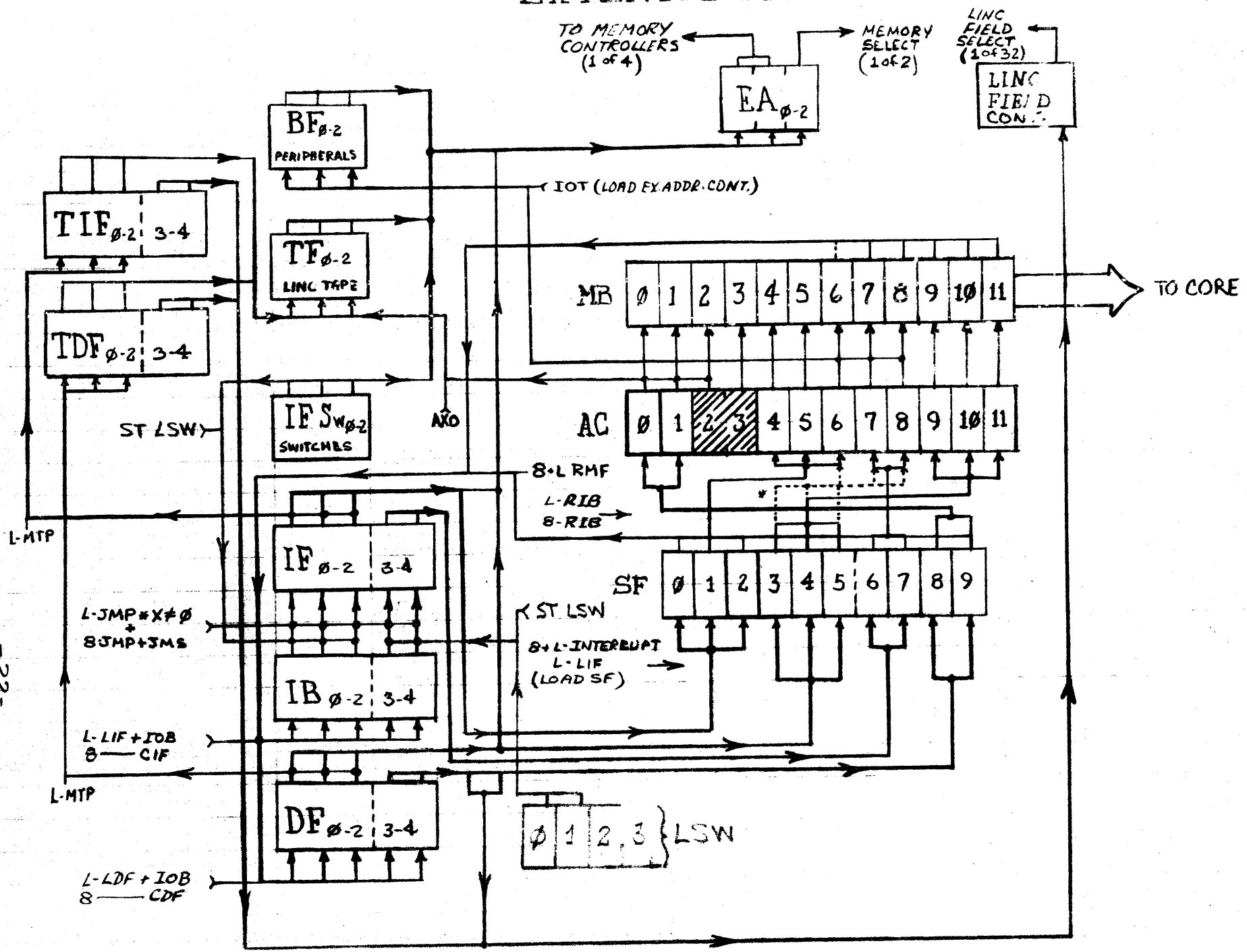
Mnemonic	Code	Operation	Direct	Indirect
		Memory Reference Operations		
SAE	1440	skip if the contents of the accumulator equal the contents of the designated memory register	4.5	6
SRO	1500	skip if the right-most bit in the designated memory register is 0; after testing, rotate the contents one place to the right	4.5	6
BCL	1540	for each bit position of memory register Y that contains a 1, clear the corresponding bit position of the accumulator (logical AND)	3	4.5
BSE	1600	for each bit position of memory register Y that contains a 1, set the corresponding bit position of the accumulator (inclusive OR)	4.5	6
BCO	1640	for each bit position of memory register Y that contains a 1, complement the corresponding bit position of the accumulator (exclusive OR)	3	4.5
		Character Display		
DSC	1740	display the character stored in the designated memory register	75-140	
		Full Address		
ADD	2000	add the contents of the designated memory register to accumulator	3	
STC	4000	store the contents of accumulator in the designated memory register then clear accumulator	3	
JMP	6000	jump to another designated memory register for the next instruction	3 (1.5 if to location 0)	

Index Class Addressing
- i=0, β=0 operand address is in p+1
- i=0, β≠0 operand address is in β register
- i=1, β=0 operand is in next location
- i=1, β≠0 operand address (less 1) in β register when execution starts (auto indexing)

EA - EXTENDED ADDRESS CONTROL

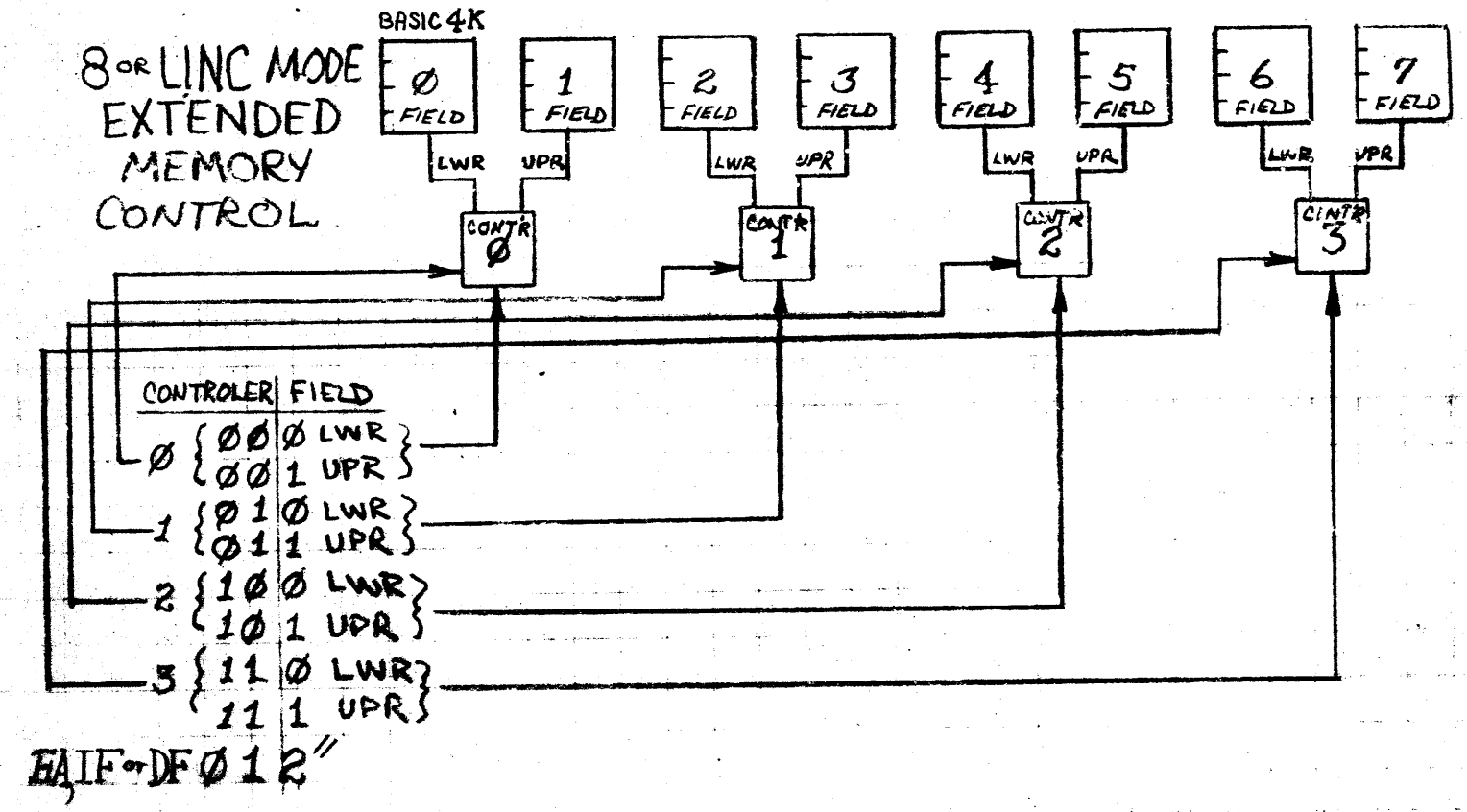


EXTENDED MEMORY BLOCK DIAGRAM

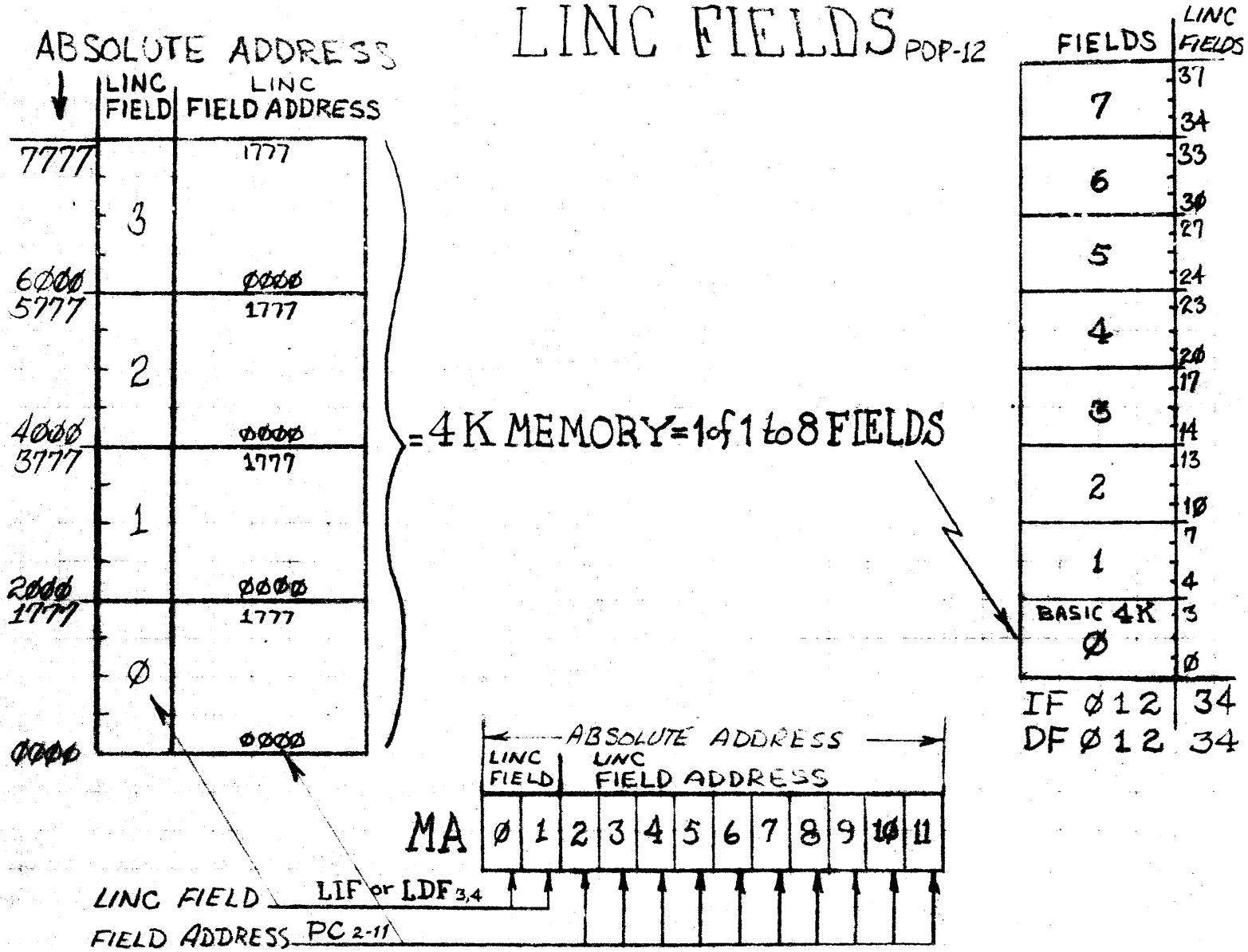


* NOTE: DOTTED LINE REPRESENTS AN 8-MODE DEVIATION

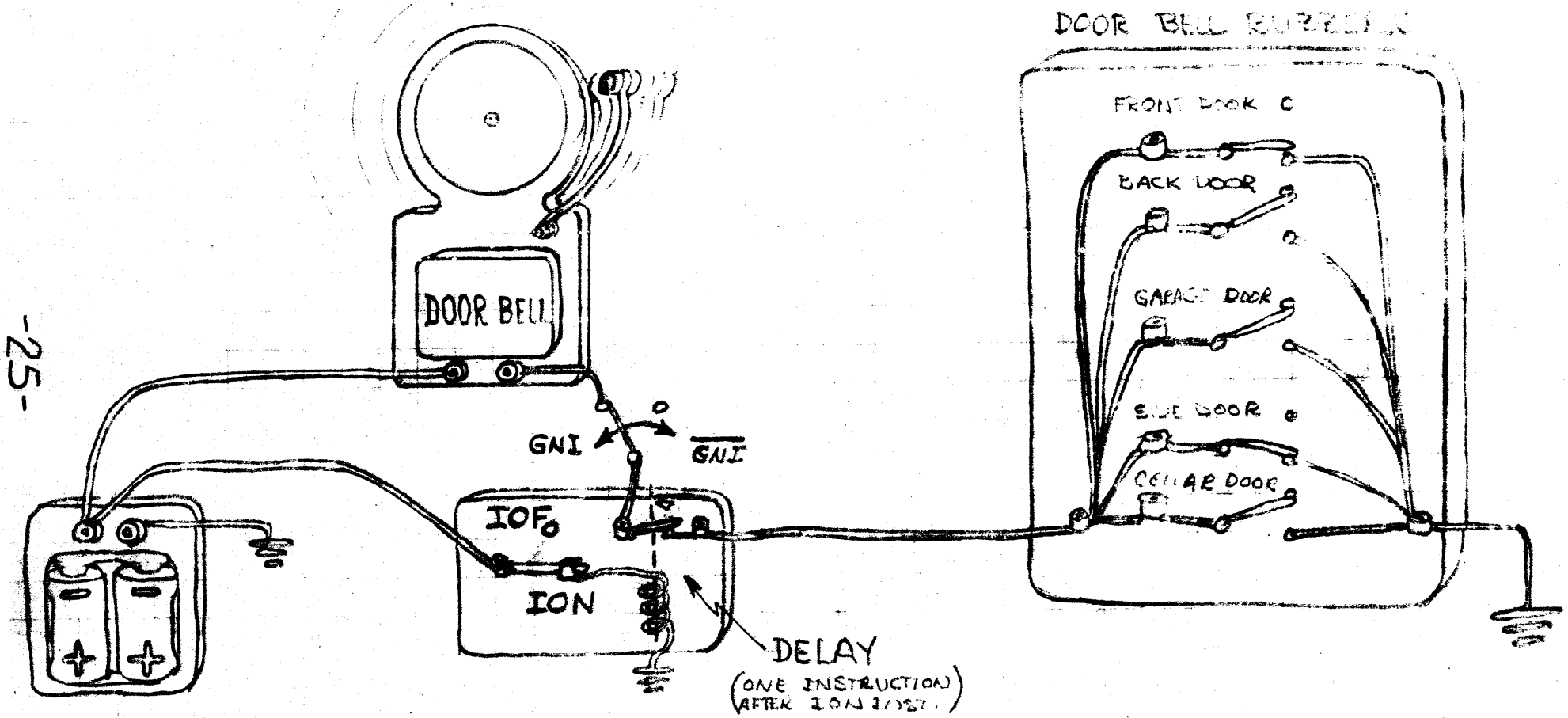
EXTENDED MEMORY CONTROL



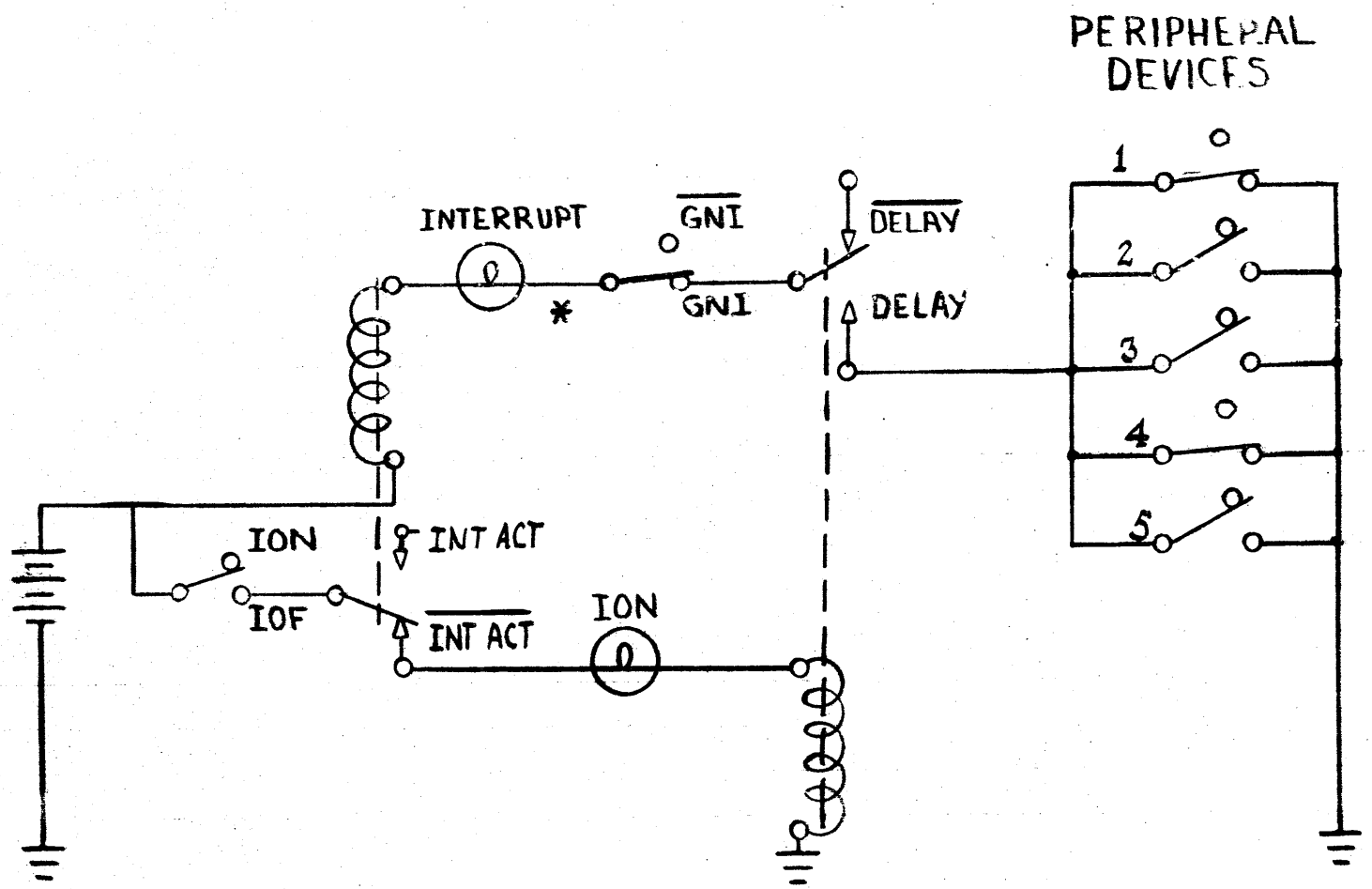
LINC FIELDS PDP-12



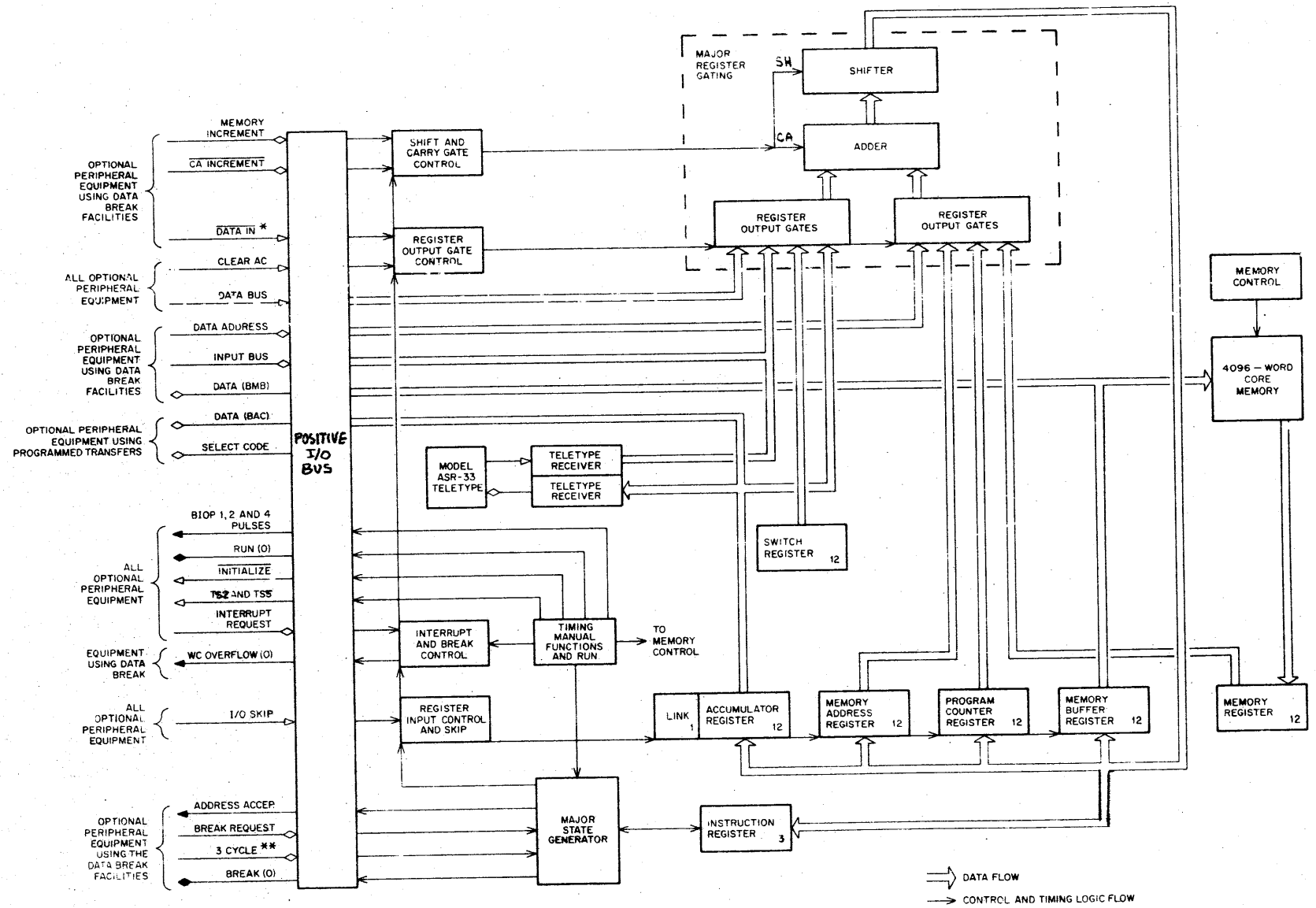
INTERRUPT CONCEPT



INTERRUPT CHAIN



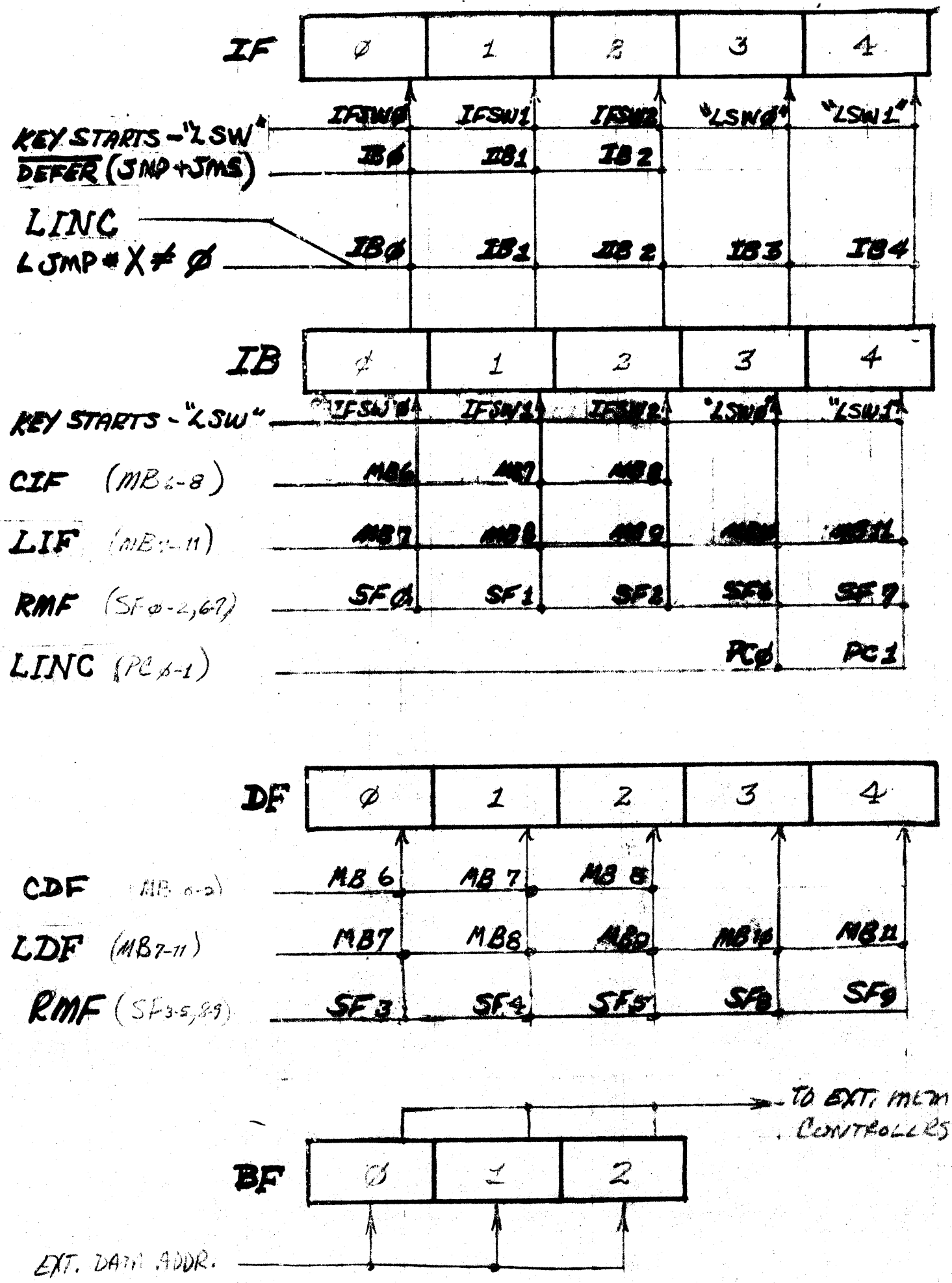
* MODE CHANGE (PDP + LINC) OR INTERRUPT INHIBIT WILL INHIBIT INTERRUPT ACKNOWLE



* TRANSFER DIRECTION IS INTO THE PDP-8/I WHEN -3 VOLTS, OUT OF PDP-8/I WHEN GROUND.

** DATA BREAK REQUEST IS FOR THREE-CYCLE BREAK WHEN GROUND OR ONE-CYCLE BREAK WHEN -3 VOLTS.

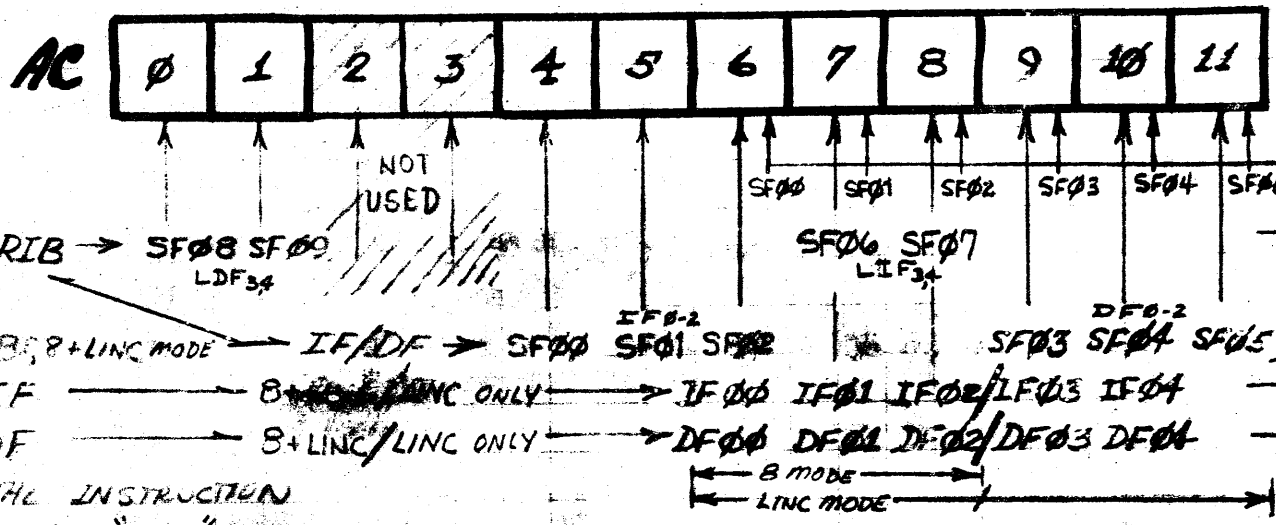
INTERFACE DIAGRAM


IF
0
1
2
3
4
IFSW0
IFSW1
IFSW2
"LSW0"
"LSW1"
KEY STARTS - "LSW"
DEFER (JMP + JMS)
IB0
IB1
IB2
LINC
LJMP * X ≠ 0
IB0
IB1
IB2
IB3
IB4
IB
0
1
2
3
4
IFSW0
IFSW1
IFSW2
"LSW0"
"LSW1"
KEY STARTS - "LSW"
CIF (MB 6-8)
MB6
MB7
MB8
LIF (MB 7-11)
MB7
MB8
MB9
MB10
MB11
RMF (SF 0-2, 6-7)
SF0
SF1
SF2
SF6
SF7
LINC (PC 0-1)
PC0
PC1
DF
0
1
2
3
4
CDF (MB 6-8)
MB 6
MB 7
MB 8
LDF (MB 7-11)
MB7
MB8
MB9
MB10
MB11
RMF (SF 3-5, 8-9)
SF3
SF4
SF5
SF8
SF9
TO EXT. MEM. CONTROLLERS
BF
0
1
2
EXT. DATA ADDR.

RK

EM REGISTER CONTROL (2 of 2)

ACCUMULATOR REG.



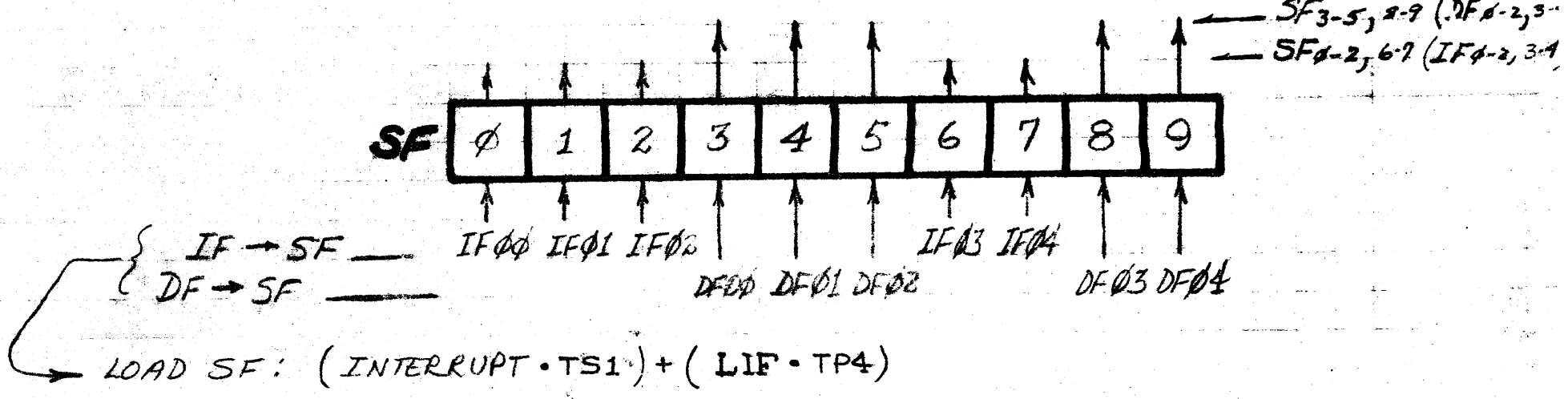
MNEMONIC CODE
IOB 0541
RIB 6234

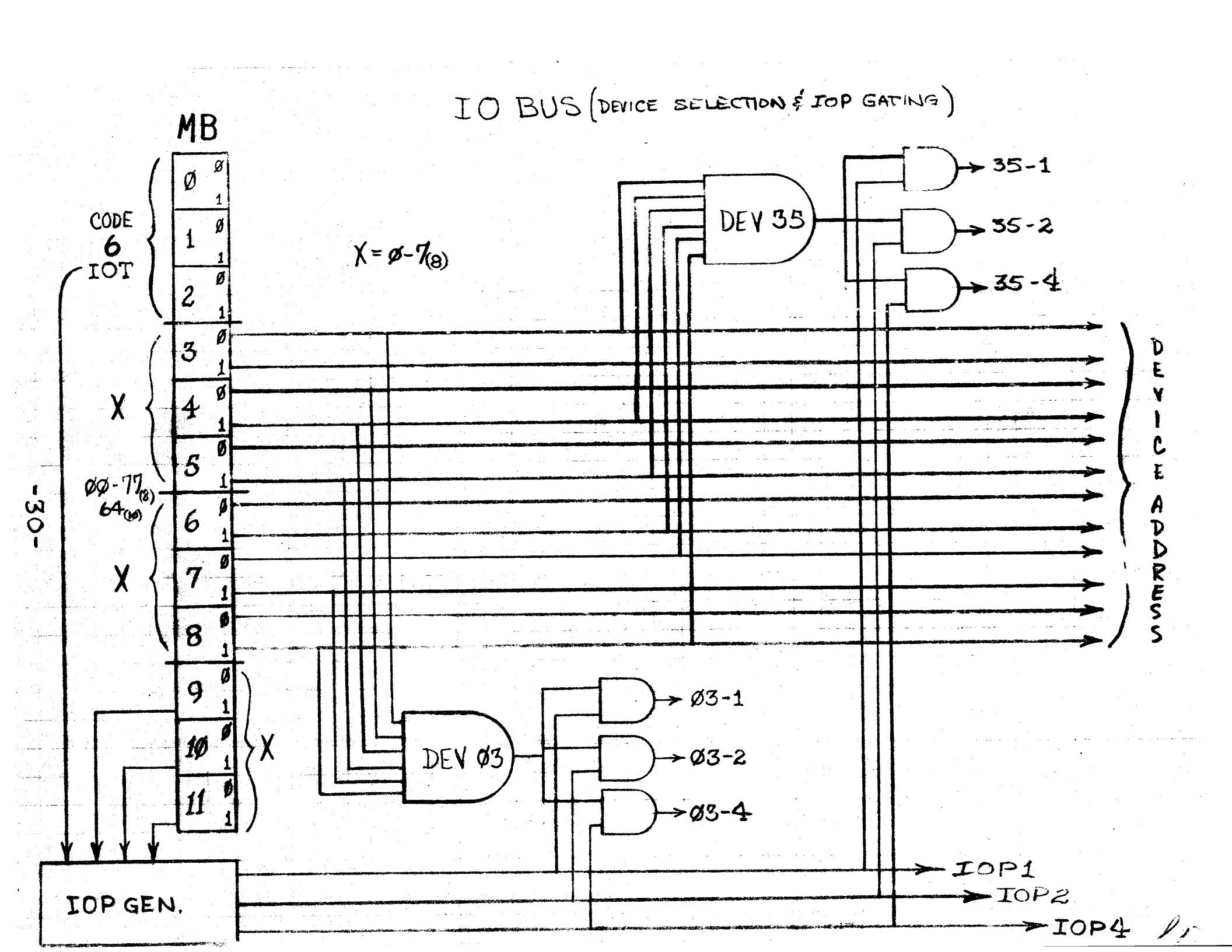
IF IN PDP-12 MODE THE INSTRUCTION MUST BE PRECEEDED BY AN "IOB" INSTRUCTION

DRAWING SEQUENCE = MEA (INT IO BUS) → IOA (IO BUS) → PMA (B MSC) → PRA (PROC. REG'S)

-29-

SAVE FIELD REG.




IO BUS (DEVICE SELECTION & IOP GATING)
MB
CODE
6
IOT
X
X
X
00-77(8)
64(10)
X = 0-7(8)
DEV 35
35-1
35-2
35-4
DEV 03
03-1
03-2
03-4
DEVICE ADDRESS
IOP GEN.
IOP1
IOP2
IOP4
-30-

TTY DISTRIBUTOR

603X = KEYBOARD READER — TTY — READ — COMPUTER

604X = TELEPRINTER PUNCH — TTY — LOAD — COMPUTER

CHARACTERISTICS:

603X, 604X } X-IOP 1 (SKIP) + IOP 2 (CLEAR) + IOP4 (TRANSFER ie READ/LOAD)

DISTRIBUTER REVOLUTION = 100ms

1 CHARACTER / 100 ms

10 CHARACTERS / SECOND

600 CHARACTERS / MINUTE ~ 5 CHAR / WORD = 120 WORDS / MIN

OUTPUT: (ASCII CODE)

1 START BIT – 8 CHARACTER BITS – 2 STOP BITS

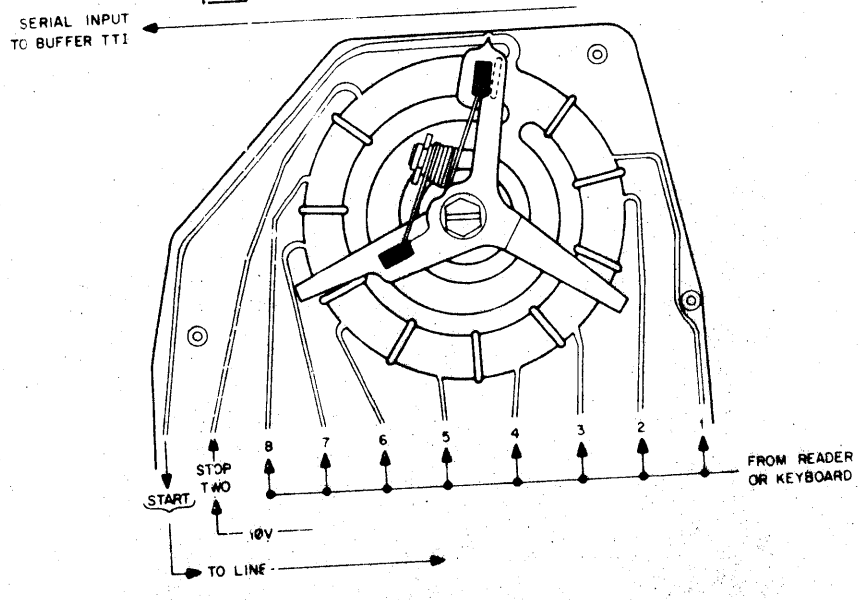
@ 9.09 ms / BIT = 99.99 ms

OUTPUT IS TO "LINE" & THE 1st BIT TRANSMITTED IS "START"

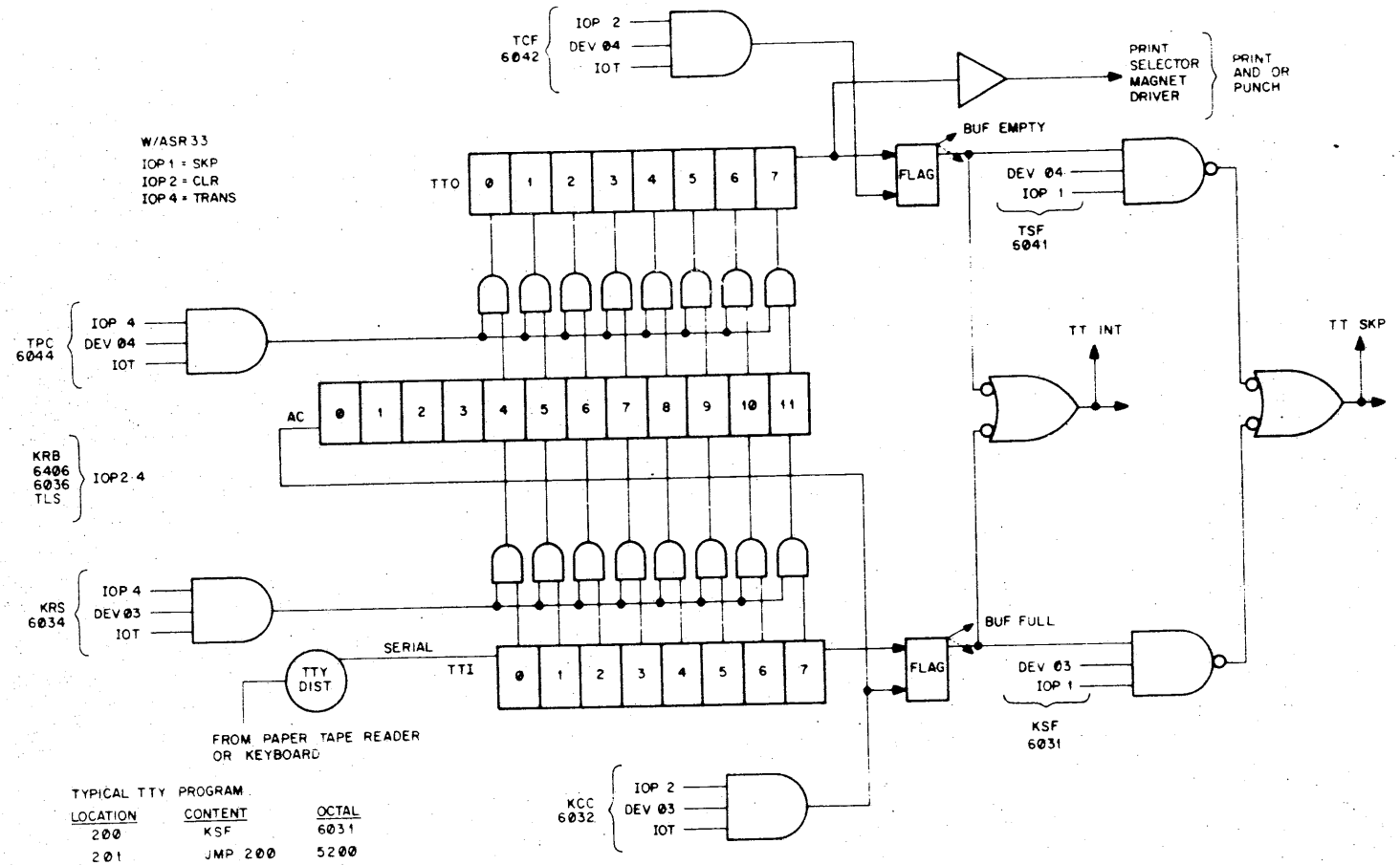
"1" IS A MARK, "0" IS A SPACE

START	1	0	0	0	0	0	1	1	STOP STOP

A = 301 (ASCII CHARACTER)

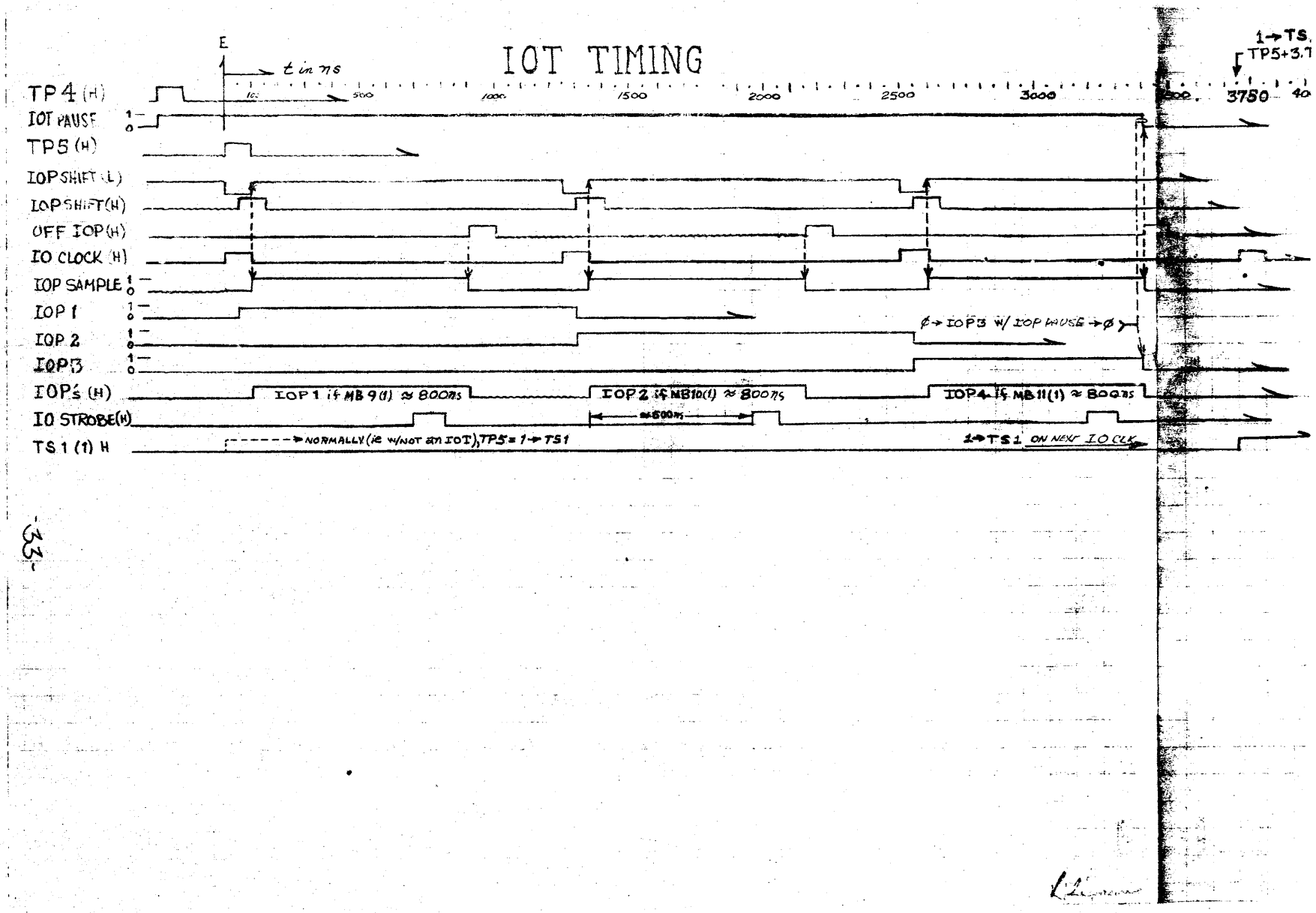


TTY BLOCK DIAGRAM

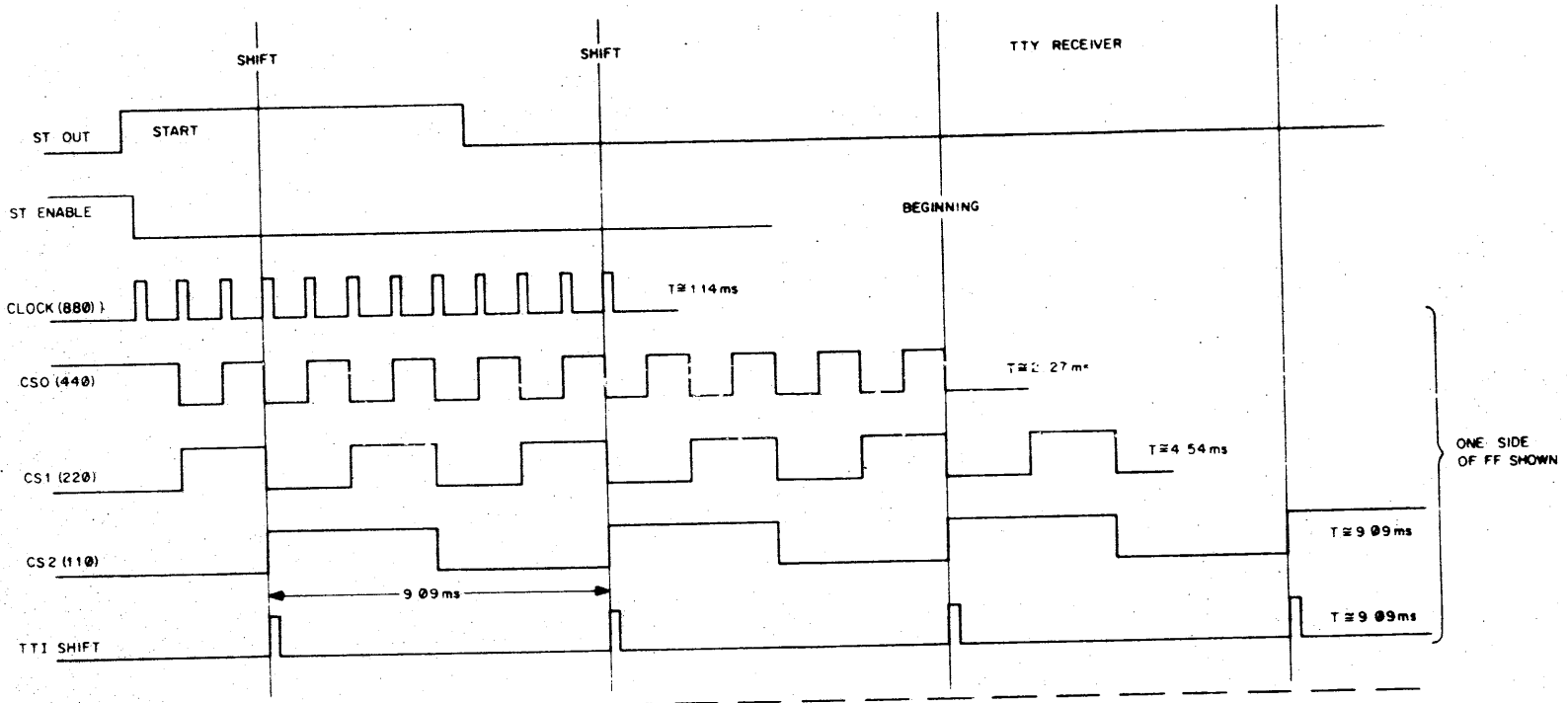


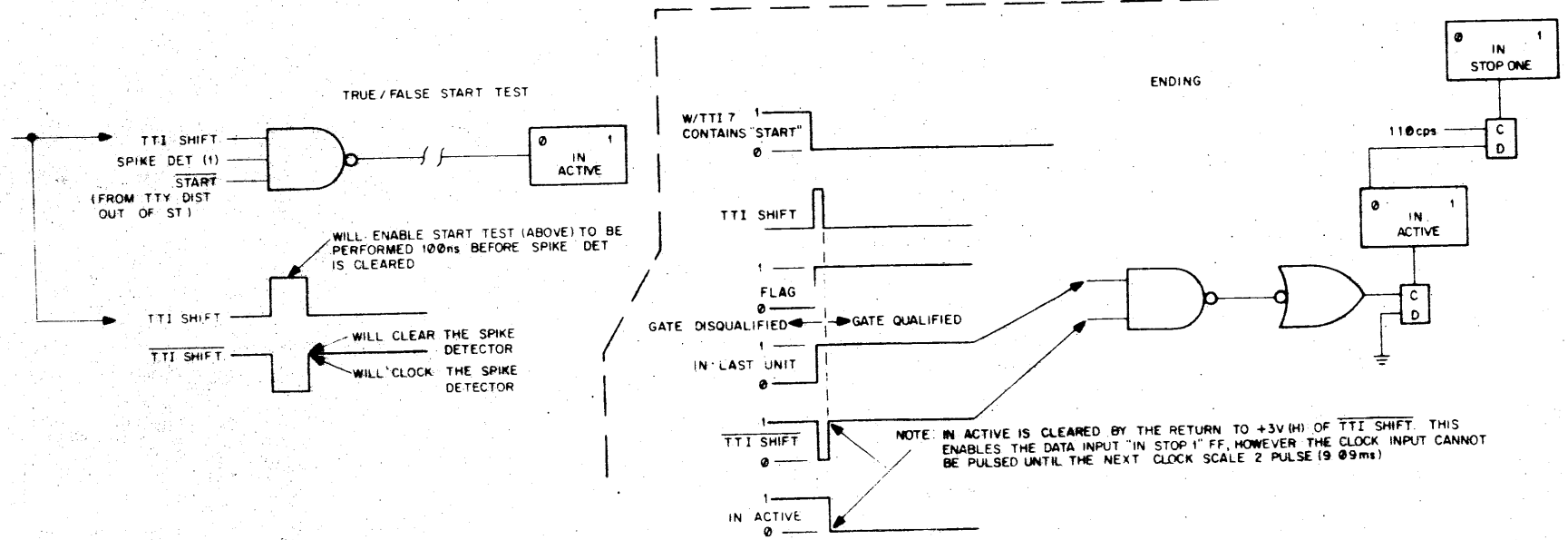
TYPICAL TTY PROGRAM

LOCATION	CONTENT	OCTAL
200	KSF	6031
201	JMP 200	5200
202	KRB	6036
203	TSF	6041
204	JMP 203	5203
205	TLS	6046
206	DCAI10	3410
207	JMP 200	5200


IOT TIMING
E
t in ns
TP4 (H)
IOT PAUSE
TP5 (H)
IOP SHIFT (L)
IOP SHIFT (H)
OFF IOP (H)
IO CLOCK (H)
IOP SAMPLE
IOP 1
IOP 2
IOP 3
IOP's (H)
IO STROBE (H)
TS 1 (1) H
500
1000
1500
2000
2500
3000
3750
1→TS
TP5+3.7
Ø→IOP3 W/ IOP HOUSE→Ø
IOP 1 if MB 9 (1) ≈ 800ns
IOP 2 if MB10 (1) ≈ 800ns
IOP4 if MB11 (1) ≈ 800ns
≈500ns
NORMALLY (ie W/NOT an IOT), TP5 = 1→TS1
1→TS1 ON NEXT IO CLK

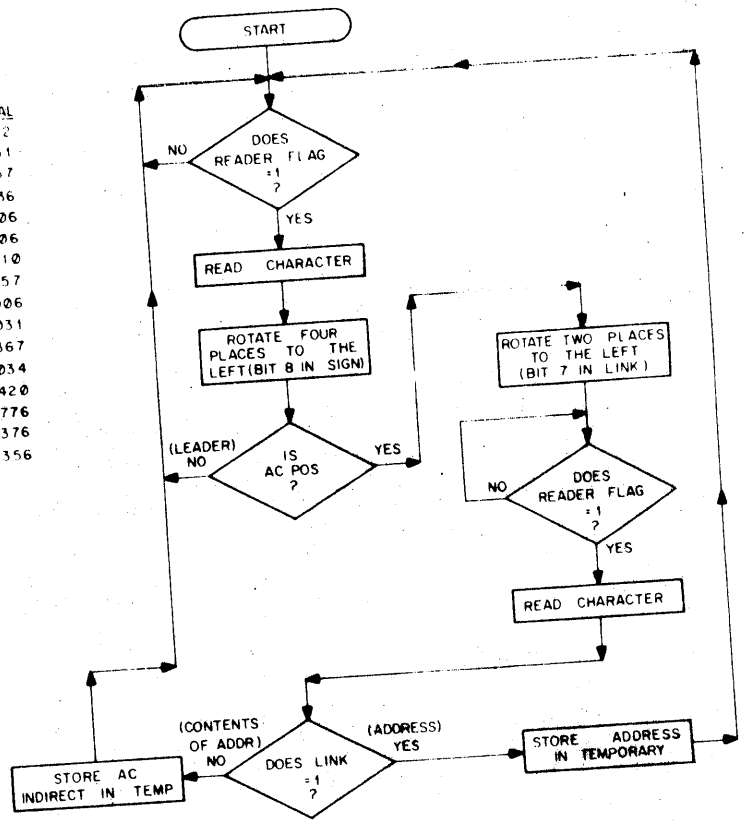
TTY CONTROL LOGIC



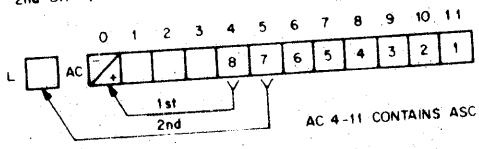


RIM

LOCATION	CONTENT	OCTAL
7756	KCC	6032
7757	KSF	6031
7760	JMP 7757	5357
7761	KRB	6036
7762	CLL, RTL	7106
7763	RTL	7006
7764	SPA	7510
7765	JMP 7757	5357
7766	RTL	7006
7767	KSF	6031
7770	JMP 7767	5367
7771	KRS	6034
7772	SNL	7420
7773	DCAI7776	3776
7774	DCA 7776	3376
7775	JMP 7756	5356
7776	0000	

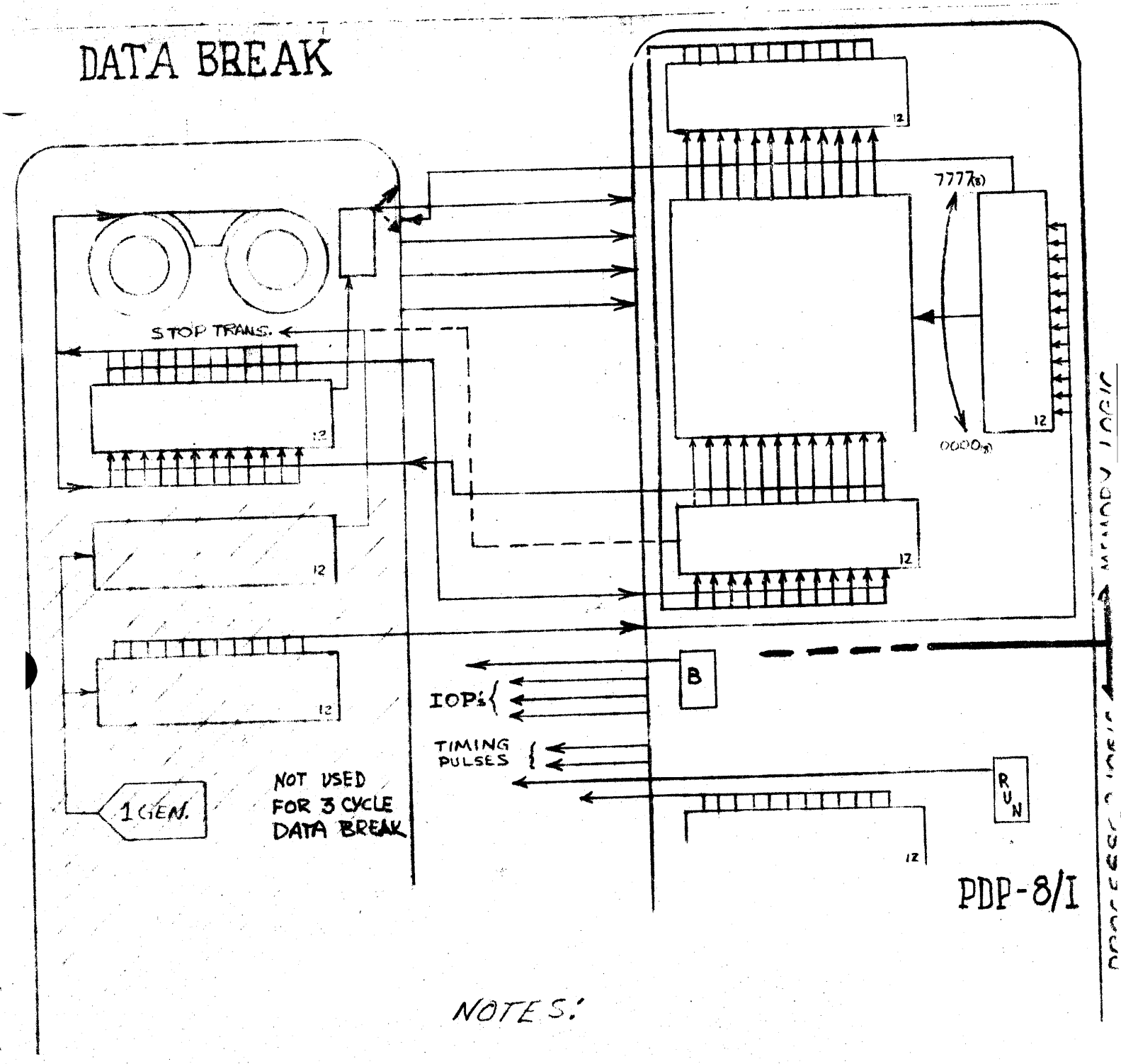


1st BIT 8, SIGN BIT CHECK IS FOR LEADER – TRAILER
2nd BIT 7, IN LINK CHECK DETERMINE: IF A ONE = ADDRESS
IF A ZERO = DATA



AC 4-11 CONTAINS ASC II CODED CHARACTER

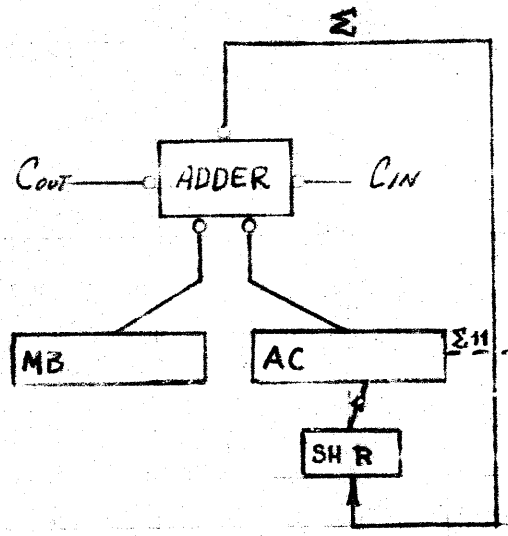
DATA BREAK



NOTES:

MULTIPLY

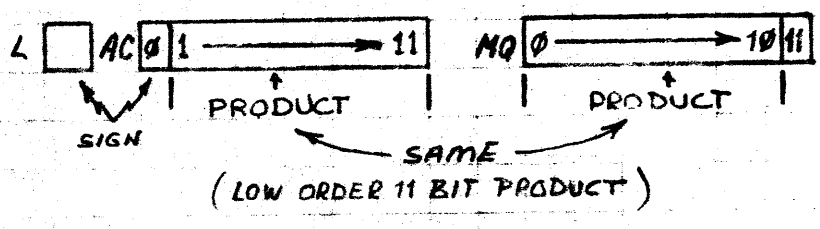
(1) MULTIPLY FLOW



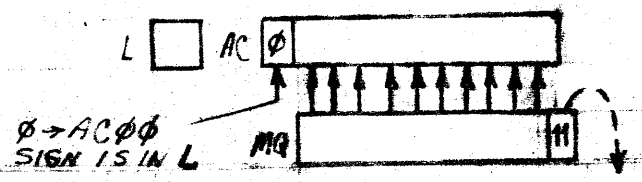
Σ: IF MQ 11 = Ø
Ø + AC → AC_{N-1}
IF MQ 11 = 1
MB + AC → AC_{N-1}
(N-1 = RAR, SCR 1)

Σ11: ΣLSB → MQ MSB

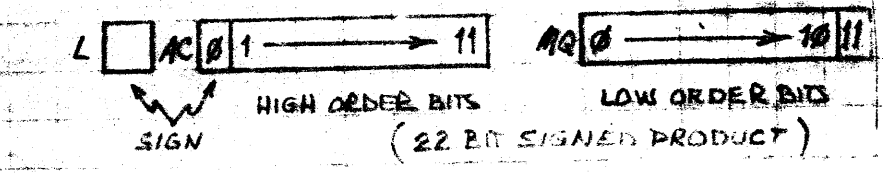
(2a) INTEGER MULTIPLY H = Ø



MQ → AC, LSB TRANSFER



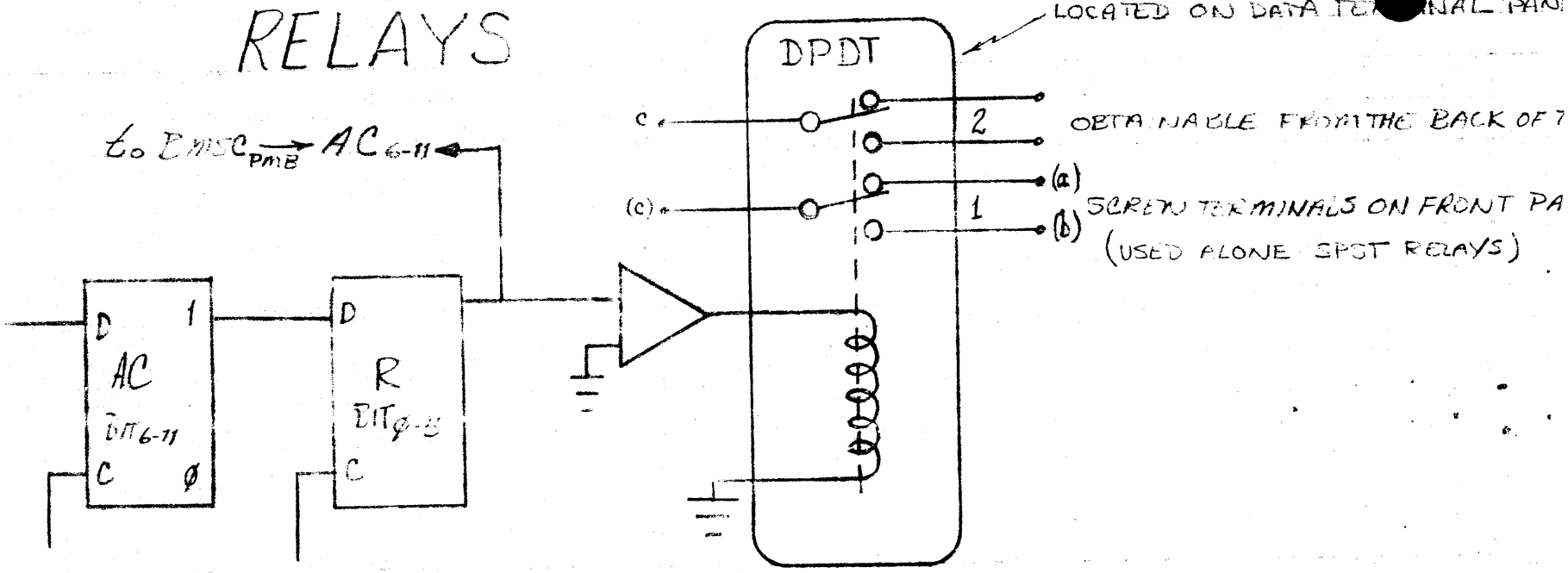
(2b) FRACTIONAL MULTIPLY H = 1



(3.) PROBLEM: $23 \times 15_{(8)} = Ø367_{(8)}$

MULTIPLICAND MB	AC	MULTIPLIER MQ		
001 101	000 000	010 01	1	← TESTED BIT TO DETERMINE NEXT TYPE OF ADD → see (1)
	001 101			ADD - MB + AC → AC
	000 110	101 00	1	SHIFT
	010 011			ADD - MB + AC → AC
	001 001	110 10	0	SHIFT
	001 001			ADD - Ø + AC → AC
	000 100	111 01	0	SHIFT
	000 100			ADD - Ø + AC → AC
	000 010	011 10	1	SHIFT
	001 111			ADD - MB + AC → AC
	000 111	101 11	0	SHIFT
	000 111			ADD - Ø + AC → AC
001 101	000 011	110 11	1	SHIFT
	Ø 3	6 7	(8)	
	MSH	LSH		

RELAYS



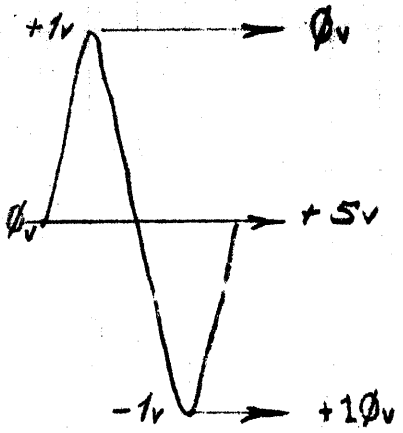
AC bit		RELAY
6	⟷	Ø
7	⟷	1
8	⟷	2
9	⟷	3
10	⟷	4
11	⟷	5
RIA	⟷	ATR

(a)	(c) COMMON	(b)
○	○	○
○	○	○
○	○	○
○	○	○
○	○	○
○	○	○

SCREEN TERMINALS

A-D CONVERTER

A 214 PRE AMP INPUT | A 404 SAM & HLD OUTPUT



CONVERTER	
2^9	5v
2^8	2.5v
2^7	1.25v
2^6	Ø.625v
2^5	Ø.3125v
2^4	Ø.15625v
2^3	Ø.ØØ78125v
2^2	Ø.ØØ39Ø625v
2^1	Ø.ØØ1953125v
$2^Ø$	Ø.ØØØ976562Sv

TRANSFER

YAD AD2(1) H = 1→AC Ø, 1→AC1, 1→AC2 (NOT COMPLEMENTED)

" AD3(1) H = Ø→AC3 (COMPLEMENT)

" AD4(1) H = Ø→AC4

" AD5(1) H = Ø→AC5

" AD6(1) H = Ø→AC6

" AD7(1) H = Ø→AC7

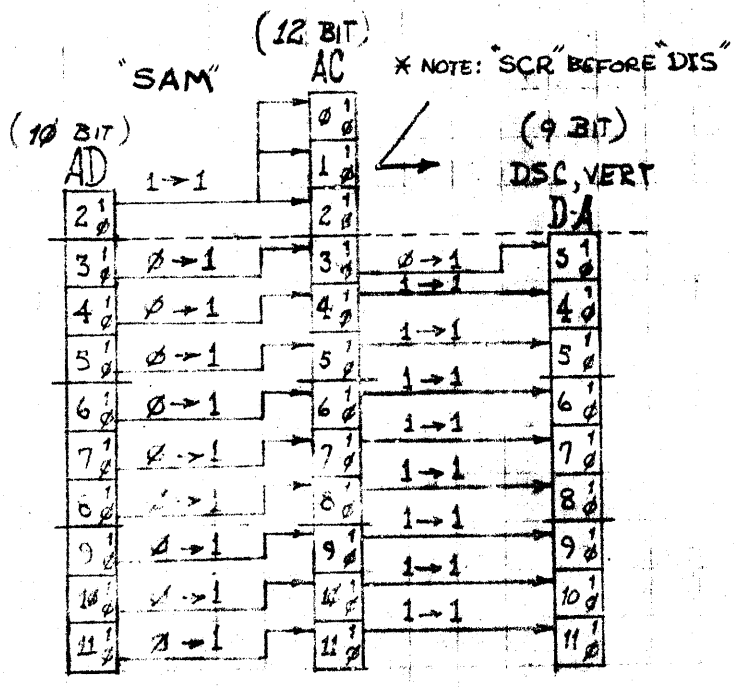
" AD8(1) H = Ø→AC8

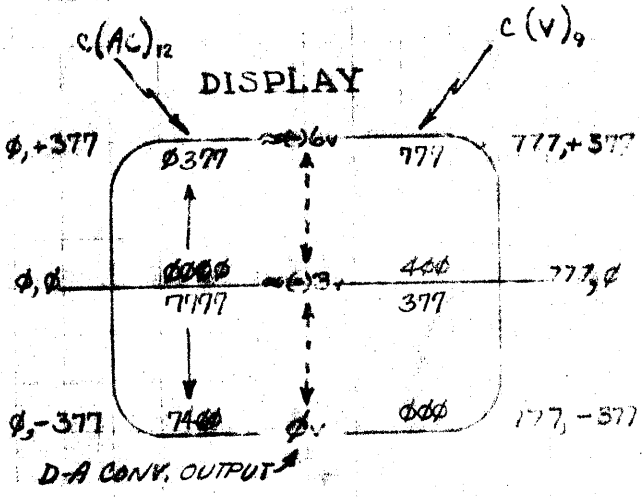
" AD9(1) H = Ø→AC9

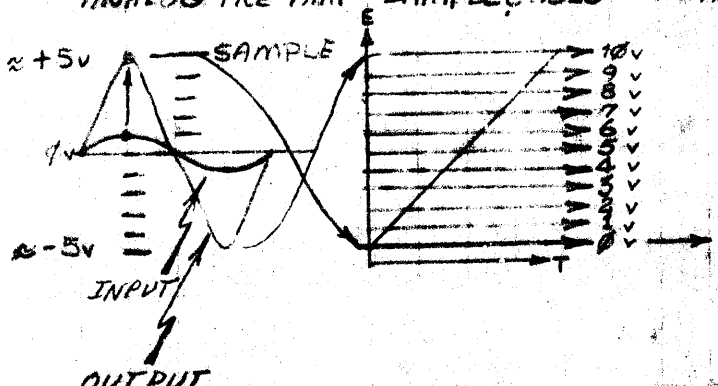
" AD10(1) H = Ø→AC10

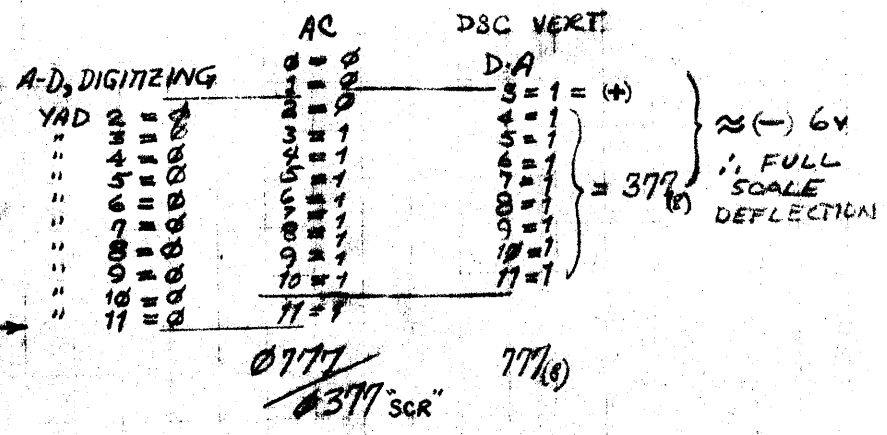
" AD11(1) H = Ø→AC11

CONVERSION IS ACCOMPLISHED THROUGH SUCCESSIVE APPROXIMATIONS

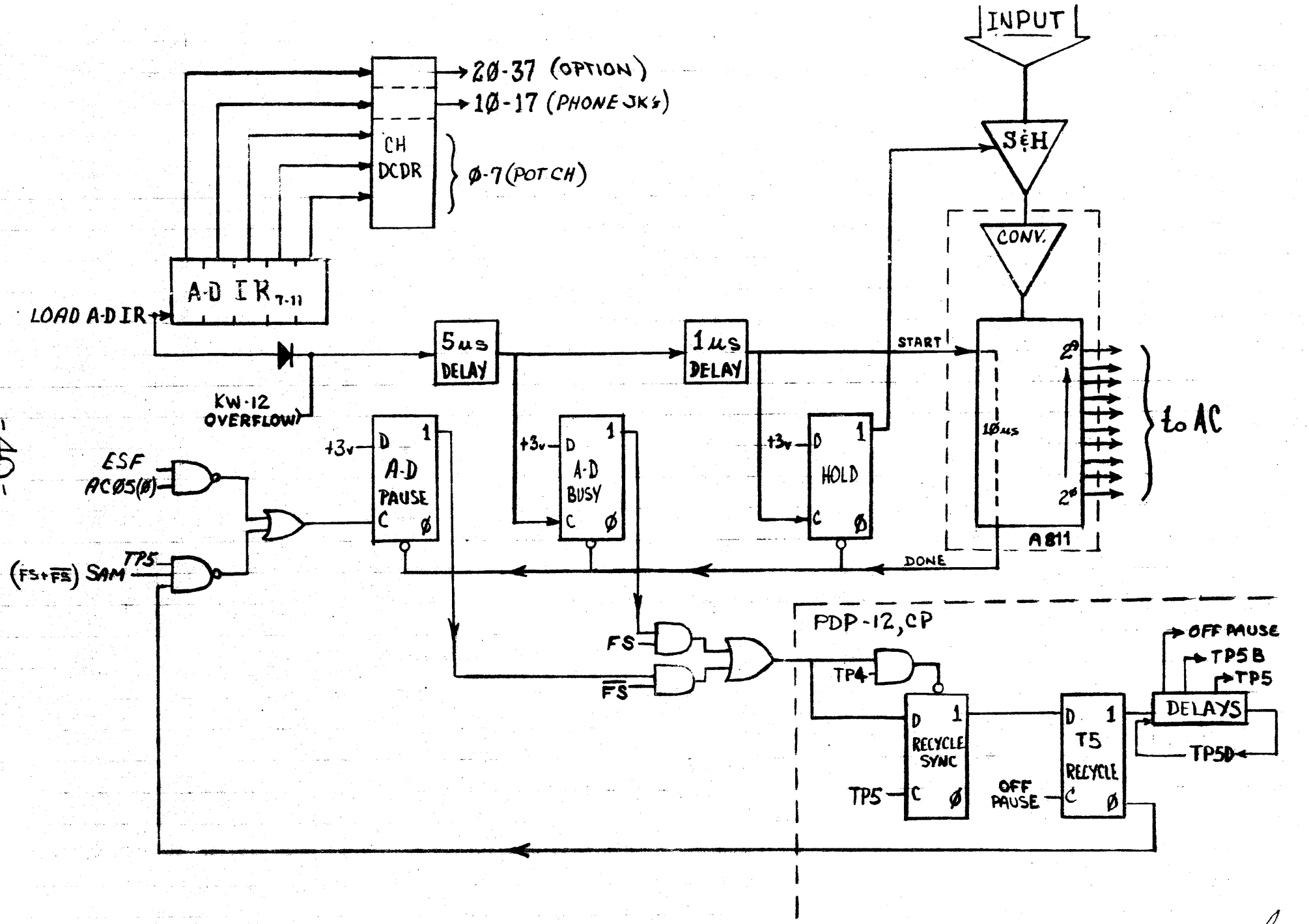


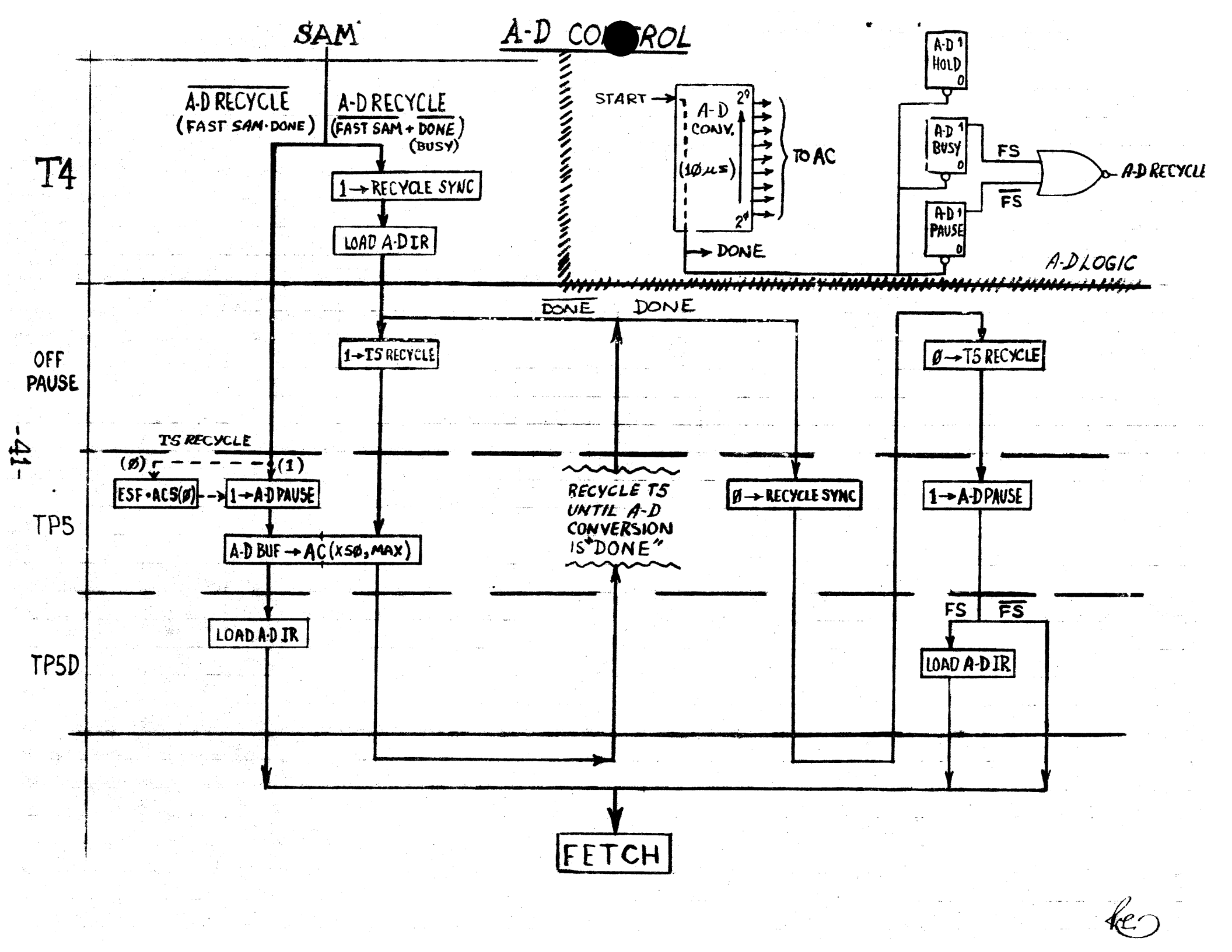




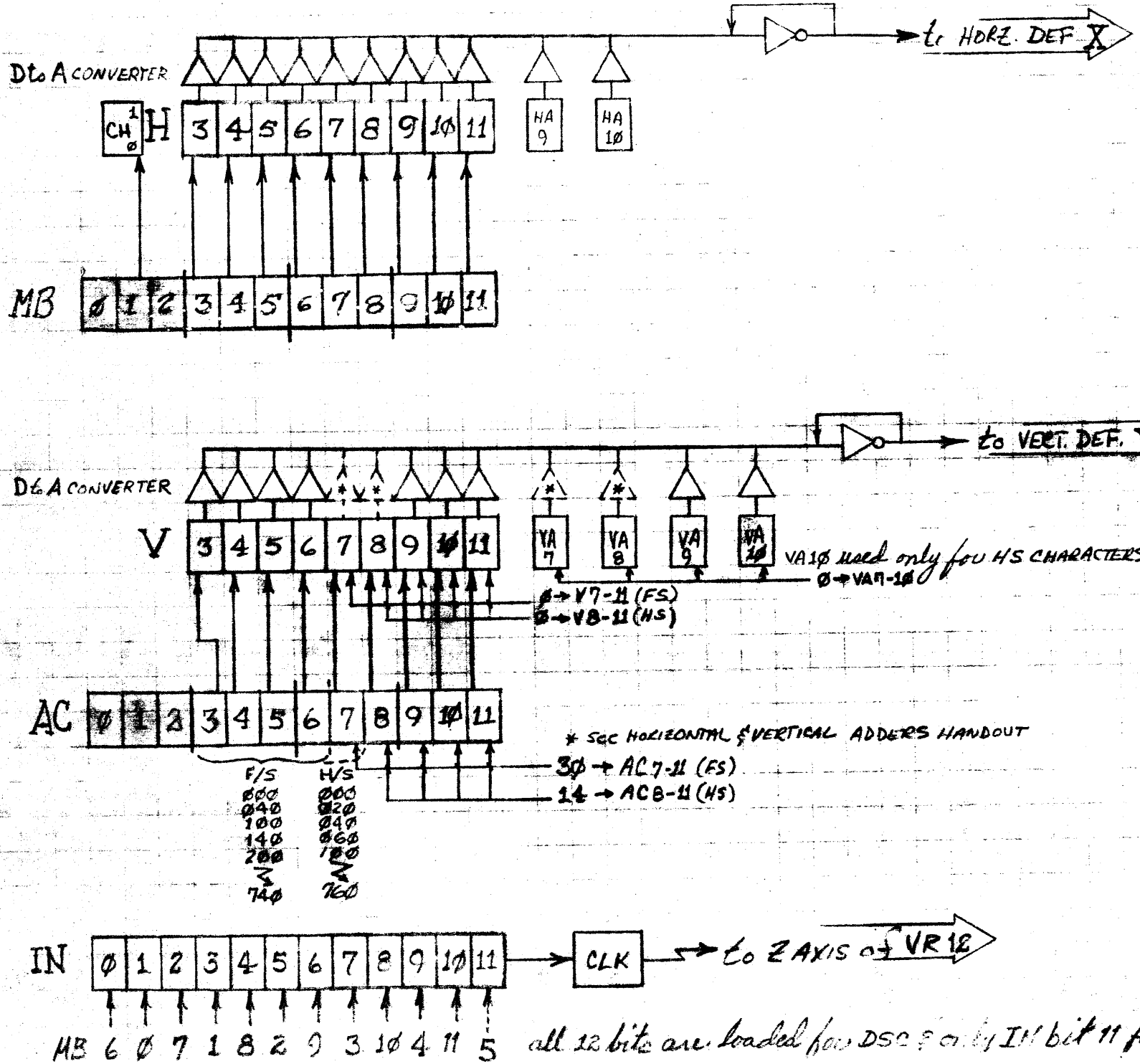


A-D BLOCK DIAGRAM

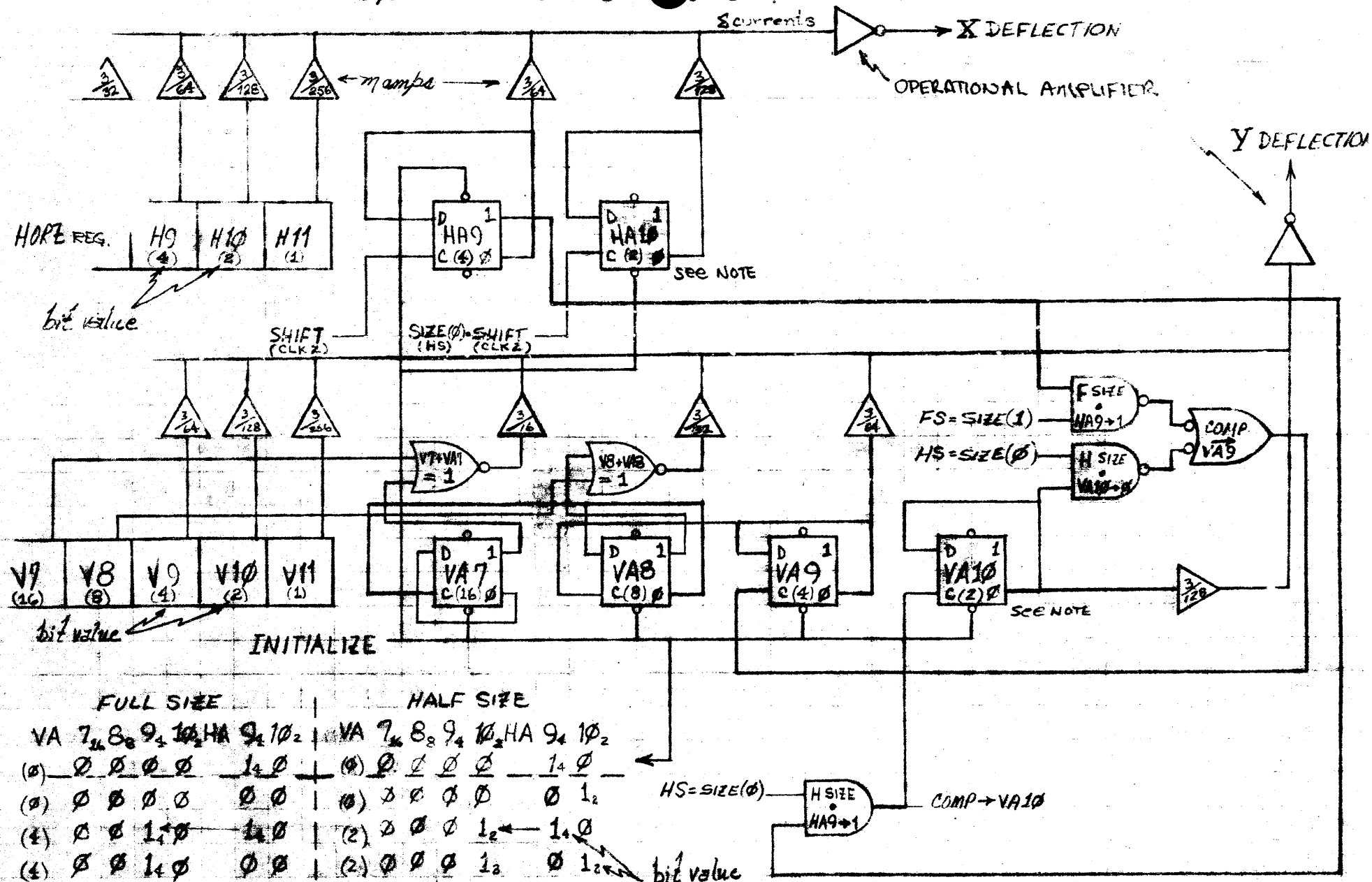



SAM
A-D CONTROL
A-D RECYCLE
(FAST SAM·DONE)
A-D RECYCLE
(FAST SAM + DONE)
(BUSY)
T4
1→RECYCLE SYNC
LOAD A-D IR
START
A-D CONV. (10μs)
2⁹
2⁰
TO AC
DONE
A-D 1 HOLD 0
A-D 1 BUSY 0
A-D 1 PAUSE 0
FS
FS
A-D RECYCLE
A-D LOGIC
DONE
DONE
OFF PAUSE
1→TS RECYCLE
Ø→T5 RECYCLE
TS RECYCLE
(Ø)
(1)
ESF·ACS(Ø)
1→A-D PAUSE
TP5
A-D BUF→AC (xSØ, MAX)
RECYCLE T5 UNTIL A-D CONVERSION IS "DONE"
Ø→RECYCLE SYNC
1→A-D PAUSE
FS
FS
LOAD A-D IR
TP5D
LOAD A-D IR
FETCH

VERTICAL, HORIZONTAL, INTENSITY LOADING



D/A HORIZONTAL & VERTICAL ADDERS



FULL SIZE							HALF SIZE						
	VA 7_{64}	8_{32}	9_{16}	10_8	HA 9_4	10_2		VA 7_{64}	8_{32}	9_{16}	10_8	HA 9_4	10_2
(Ø)	Ø	Ø	Ø	Ø	1_4	Ø	(Ø)	Ø	Ø	Ø	Ø	1_4	Ø
(Ø)	Ø	Ø	Ø	Ø	Ø	Ø	(Ø)	Ø	Ø	Ø	Ø	Ø	1_2
(1)	Ø	Ø	1_{16}←Ø		1_4	Ø	(2)	Ø	Ø	Ø	1_2 ←	1_4	Ø
(4)	Ø	Ø	1_4	Ø	Ø	Ø	(2)	Ø	Ø	Ø	1_8	Ø	1_2
(8)	Ø	1_{32}←Ø	←Ø		1_4	Ø	(4)	Ø	Ø	1_{16}←Ø	←	1_4	Ø
(8)	Ø	1_8	Ø	Ø	Ø	Ø	(4)	Ø	Ø	1_4	Ø	Ø	1_2
(12)	Ø	1_8	1_{16}←Ø		1_4	Ø	(6)	Ø	Ø	1_4	1_2 ←	1_4	Ø
(12)	Ø	1_8	1_4	Ø	Ø	Ø	(6)	Ø	Ø	1_4	1_2	Ø	1_2
(16)	1_{64}←Ø	←Ø	←Ø		1_4	Ø	(8)	Ø	1_{32}←Ø	←Ø	←	1_4	Ø

bit value

← COMPLEMENTS W/VA 8 → Ø

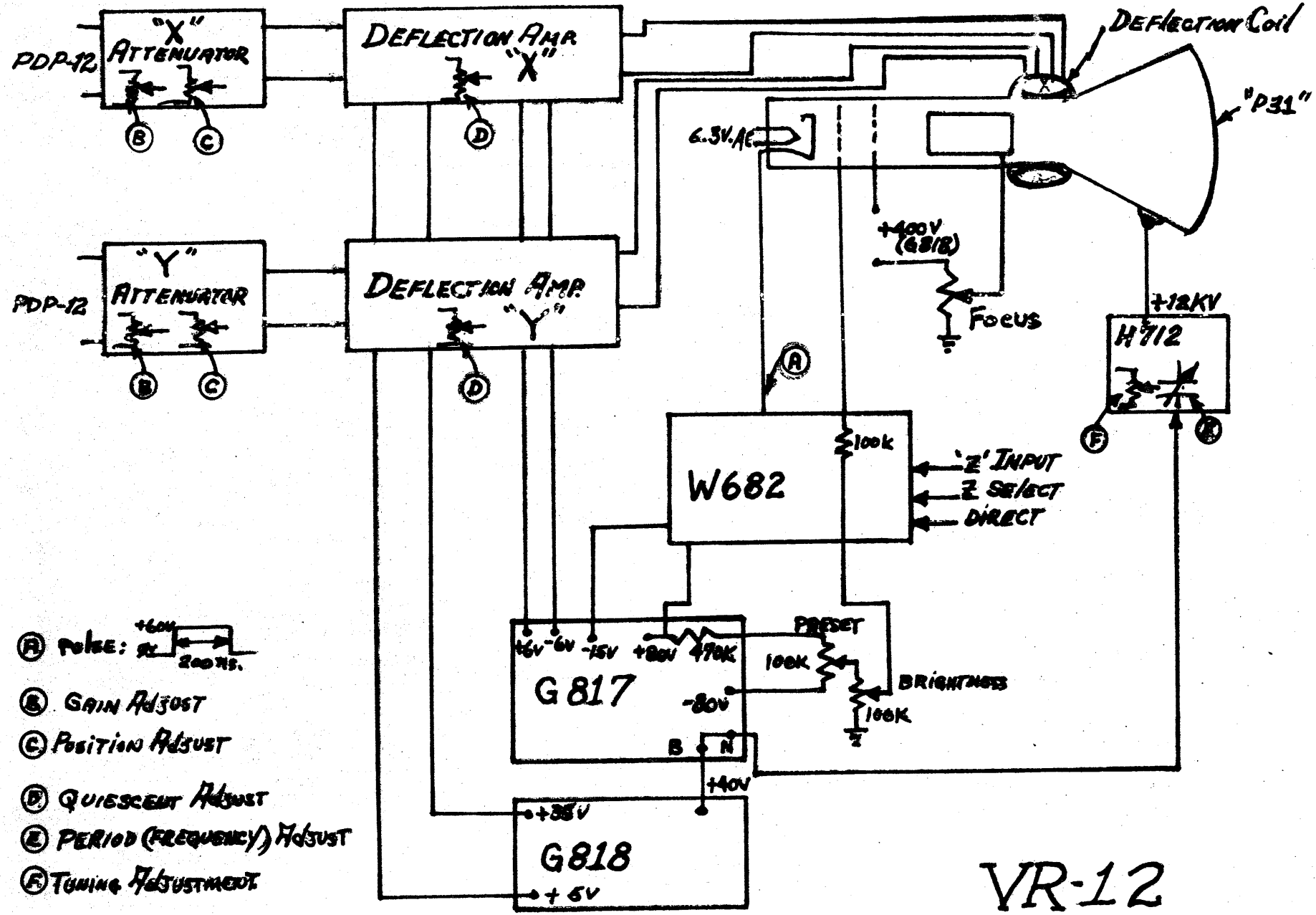
NOTE: VA & HA 1Ø are only used (a) on HALF SIZE characters

(b) CLOCK 1 = INTENSIFY
2 = SHIFT

DISPLAY CHARACTER TABLE

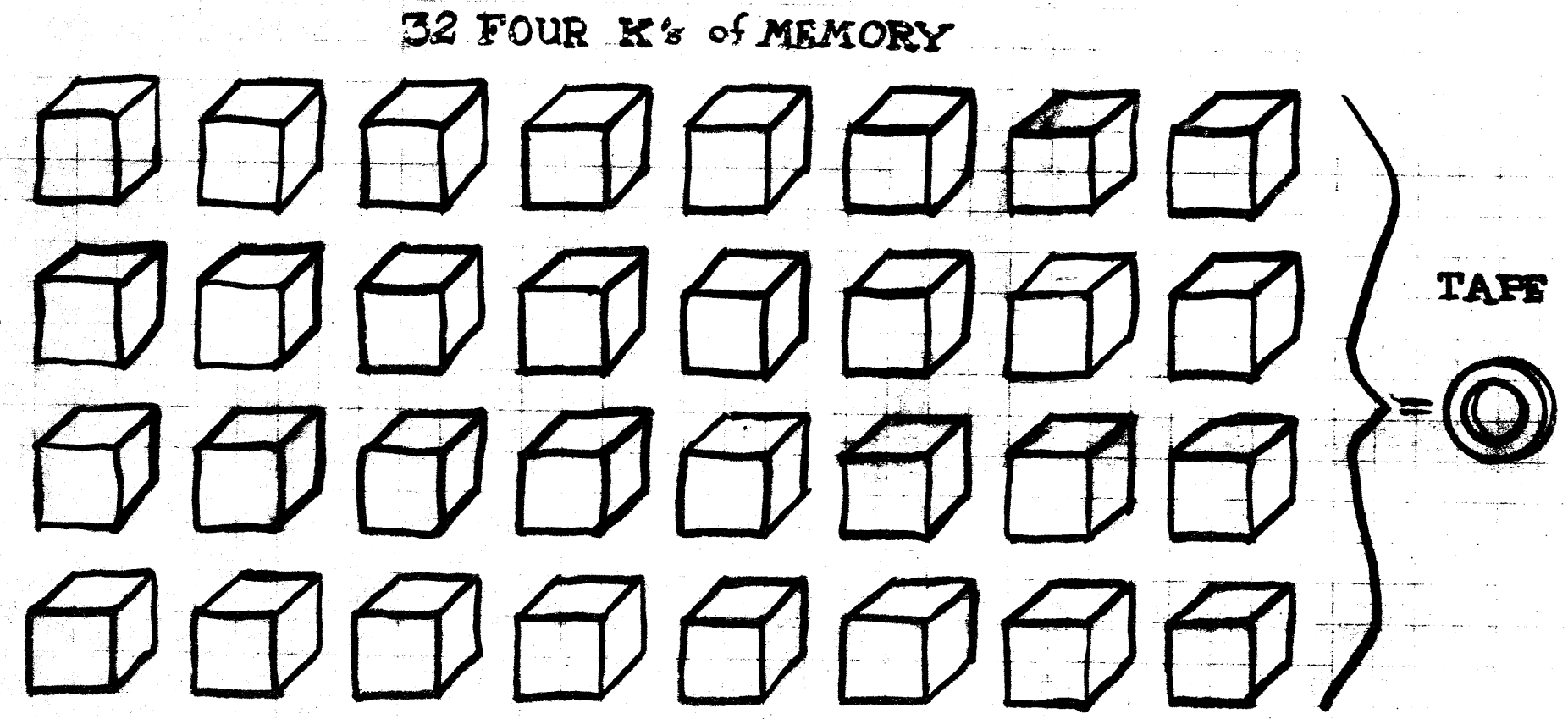
0	4136	A	4477	U	0177
	3641		7744		7701
1	2101	B	5177	V	0176
	0177		2651		7402
2	4523	C	4136	W	0677
	2151		2241		7701
3	4122	D	4177	X	1463
	2651		3641		6314
4	2414	E	4577	Y	0770
	0477		4145		7007
5	5172	F	4477	Z	4543
	0651		4044		6151
6	1506	G	4136	=	1212
	4225		2645		1212
7	4443	H	1077	u	0107
	6050		7710		0107
8	5126	I	7741	,	0500
	2651		0041		0006
9	5120	J	4142	.	0001
	3651		4076		0000
EOL	0000	K	1077	⊟	4577
	0000		4324		7745
del	0000	L	0177	[	4177
	0000		0301		0000
SPACE	0000	M	3077		
	0000		7730		
i	0101	N	3077		
	0126		7706		
p	3700	O	4177		
	3424		7741		
-	0404	P	4477		
	0404		3044		
+	0404	Q	4276		
	0437		0376		
|	0000	R	4477		
	0077		3146		
#	3614	S	5121		
	1436		4651		
CASE	0000	T	4040		
	0000		4077		

VR-12 BLOCK DIAGRAM



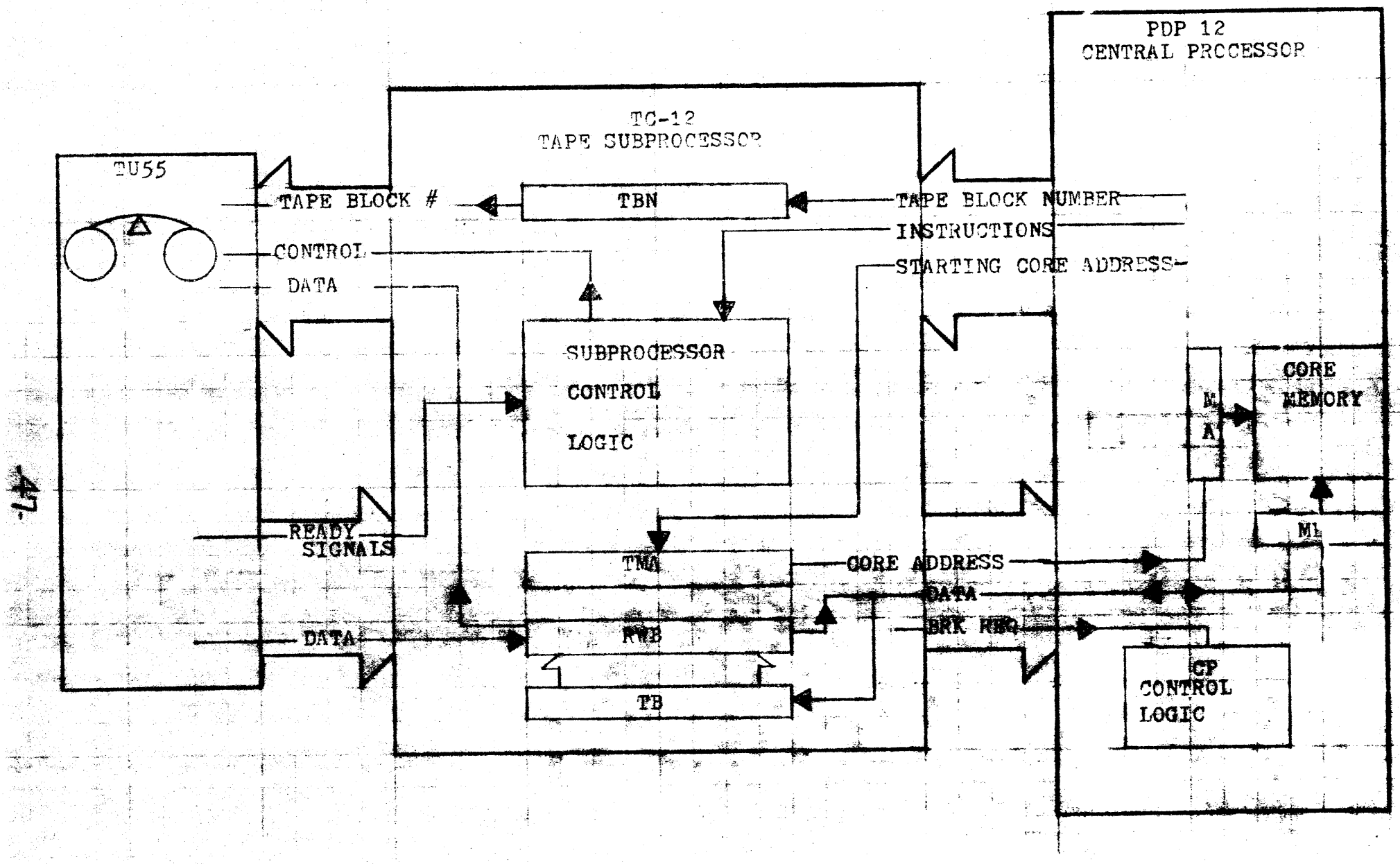
VR-12

CORE MEMORY STORAGE VRS TAPE STORAGE



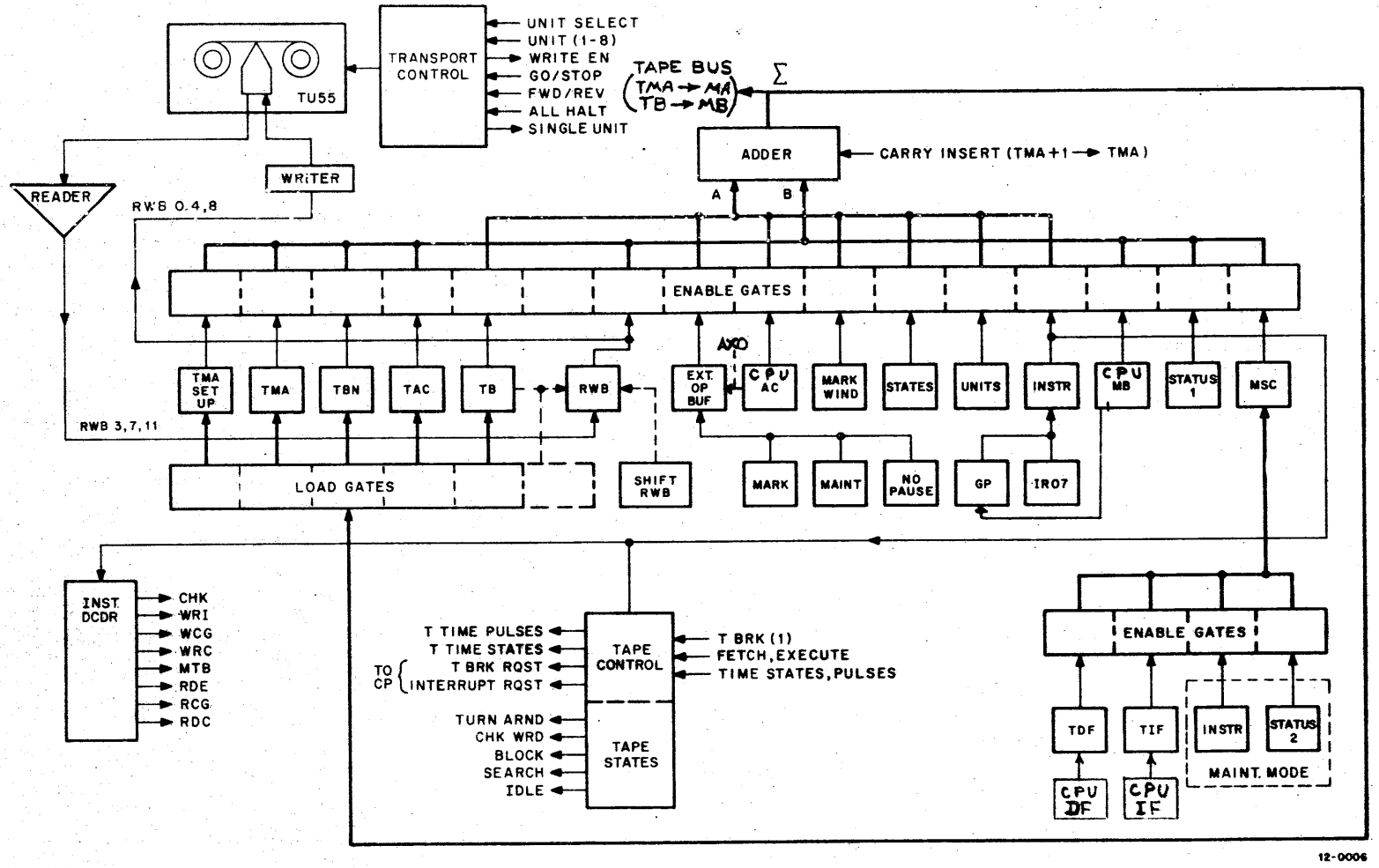
4096 WORDS — 12 BIT WORDS

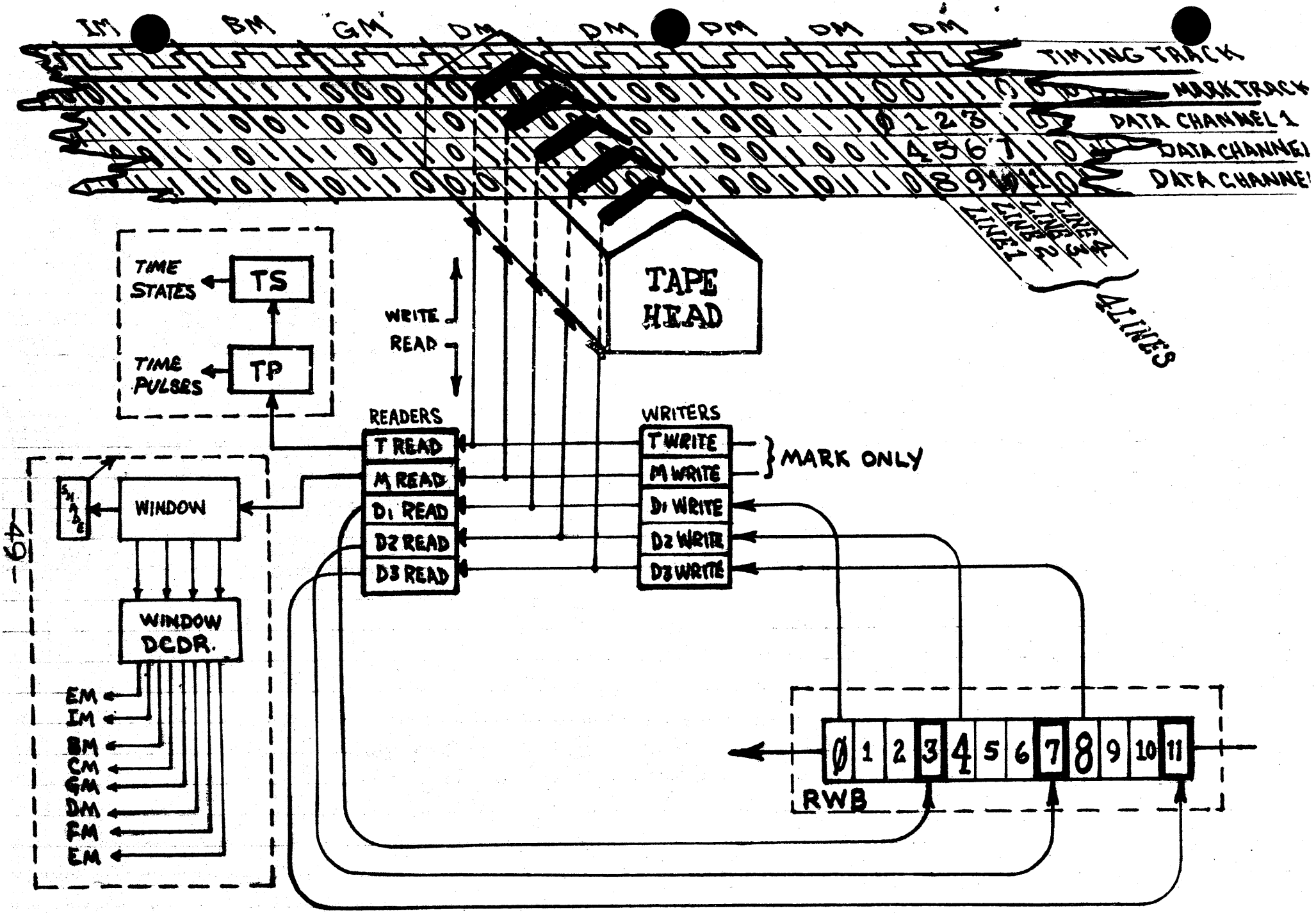
131,072 WORDS
512 BLOCKS
256 WORDS
12 BIT WORDS



LINCTAPE BLOCK DIAGRAM

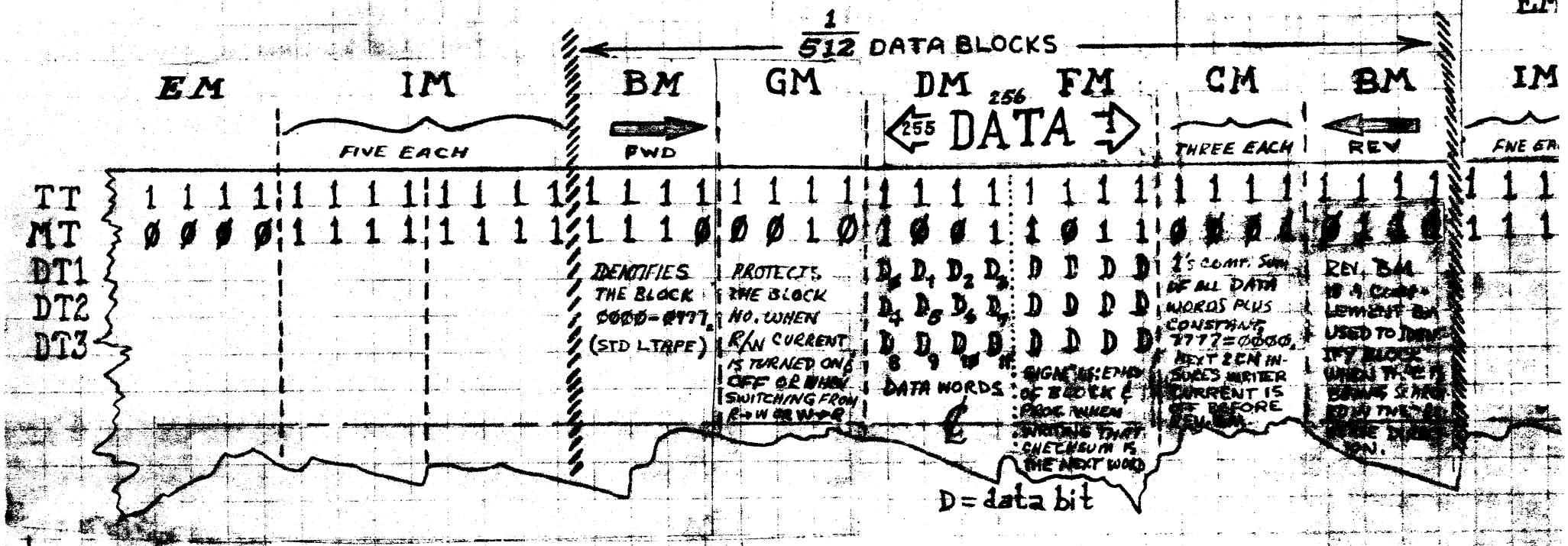
PDP-12 LINC TAPE FLOW DIAGRAM




IM
BM
GM
DM
DM
DM
DM
DM
TIMING TRACK
MARK TRACK
DATA CHANNEL 1
DATA CHANNEL
DATA CHANNEL
0 1 2 3
4 5 6 7
8 9 10 11
LINE 1
LINE 2
LINE 3
LINE 4
4 LINES
TAPE HEAD
WRITE
READ
TIME STATES
TS
TIME PULSES
TP
READERS
T READ
M READ
D1 READ
D2 READ
D3 READ
WRITERS
T WRITE
M WRITE
D1 WRITE
D2 WRITE
D3 WRITE
MARK ONLY
WINDOW
WINDOW DCDR.
EM
IM
BM
CM
GM
DM
FM
EM
0 1 2 3 4 5 6 7 8 9 10 11
RWB

LINC TAPE

PDP 12 LINCTAPE FORMAT

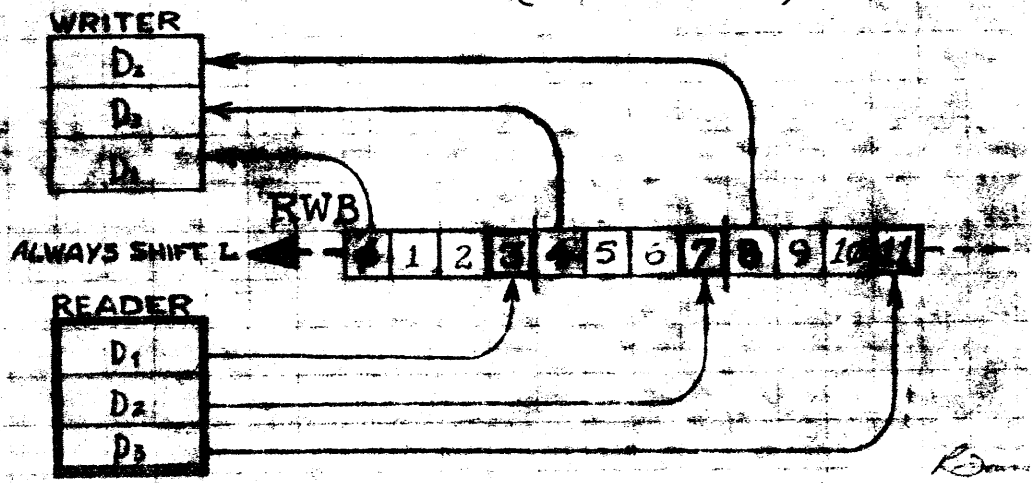


-50-

NOTE:

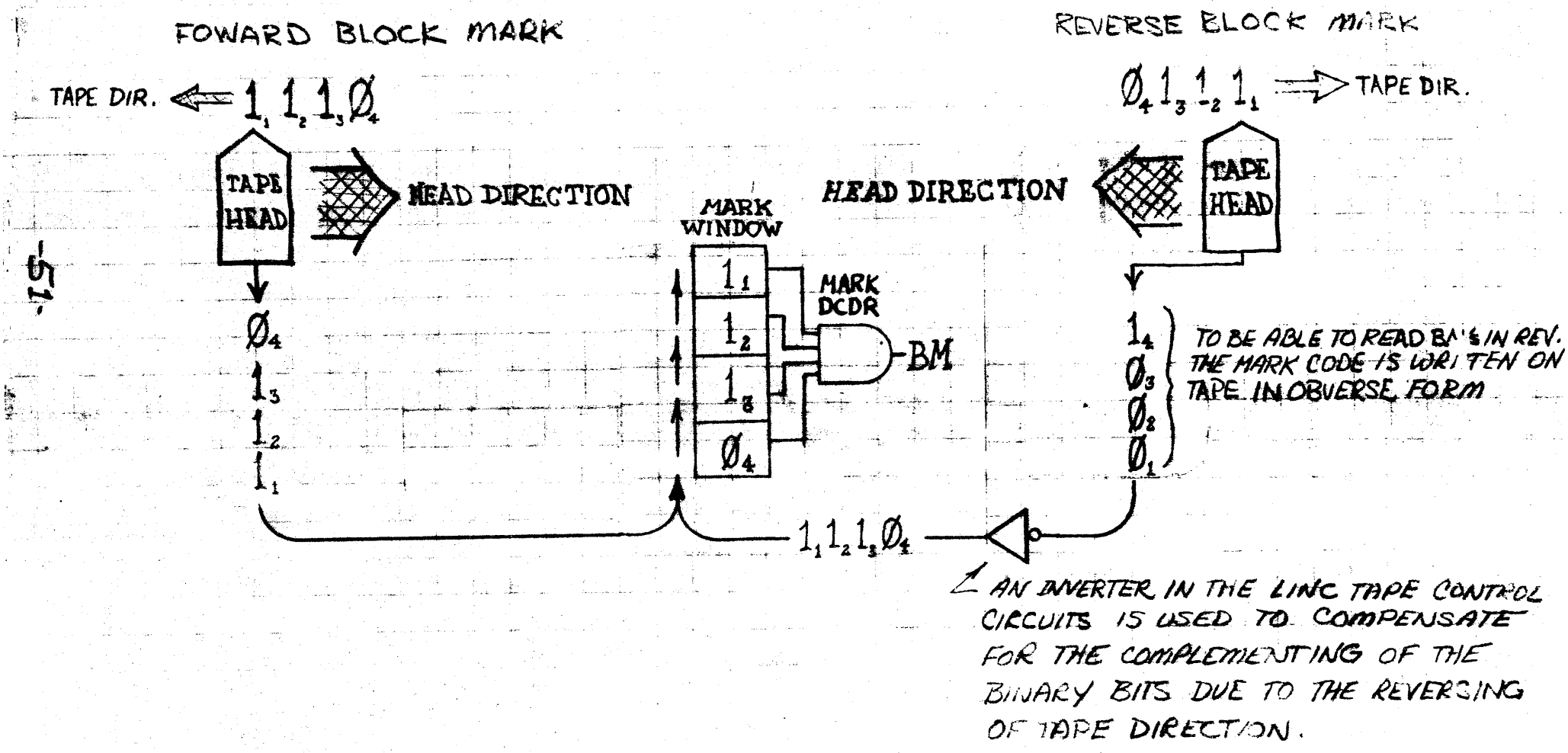
1. ONLY READ AND WRITE DATA IN THE FOWARD DIRECTION/ CAN READ BLOCK NUMBERS IN EITHER DIRECTION (FOWARD OR REVERSE).
2. MARK AND DATA TRACKS ARE WRITTEN AND ARE READ IN BINARY FORM (ie 1=1 & Ø=Ø) THE CHECK SUM IS WRITTEN IN COMPLEMENT FORM (ie 1=Ø & Ø=1) BY PHASE.

(1) BM = BLOCK MARK
(3) CM = CHECK MARK
(255) DM = DATA MARK
EM = END MARK
(1) FM = FINAL MARK
(1) GM = GUARD MARK
(5) IM = INTERBLOCK MARK
MT = MARK TRACK
TT = TIMING TRACK

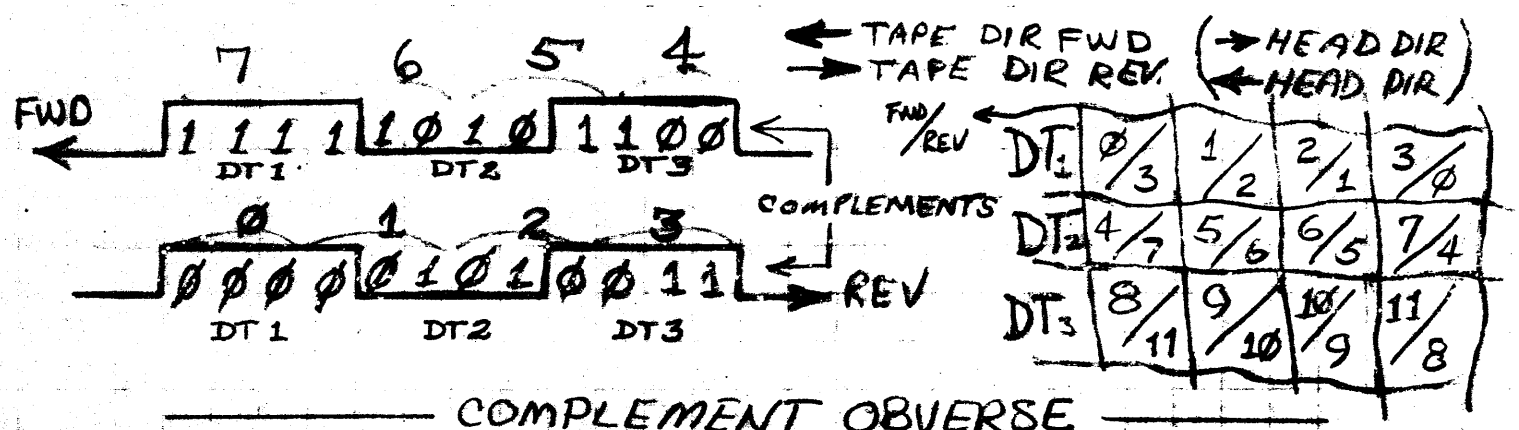


BLOCK MARK

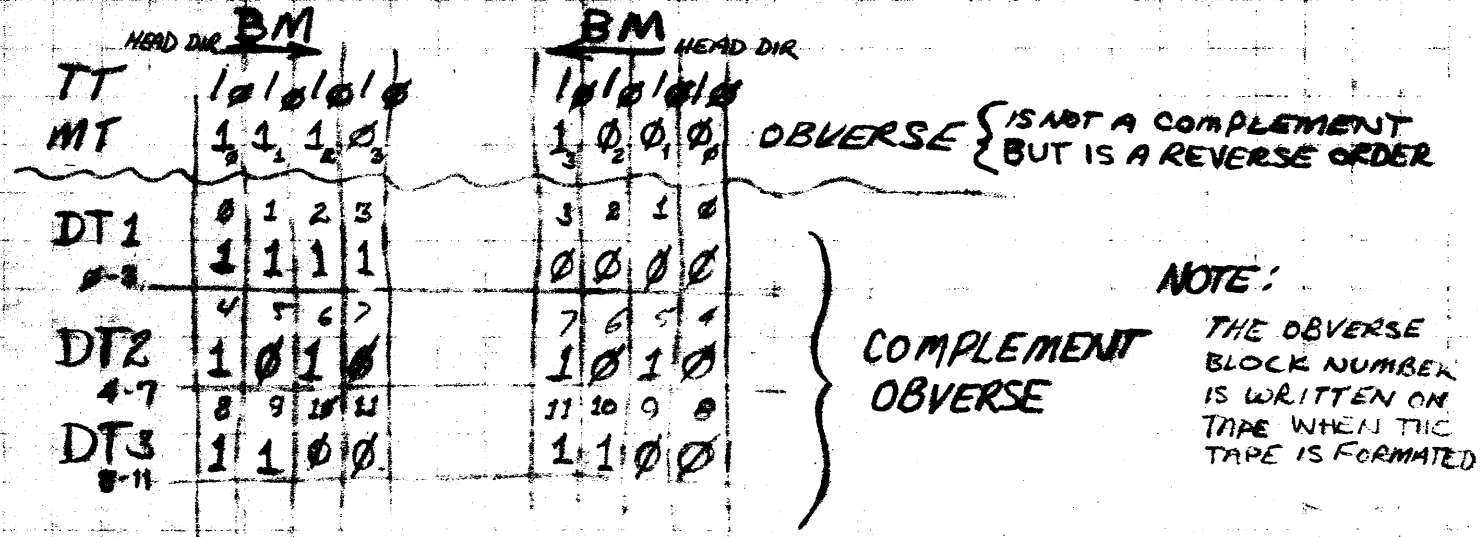
BM - BLOCK MARK = 1 1 1 Ø



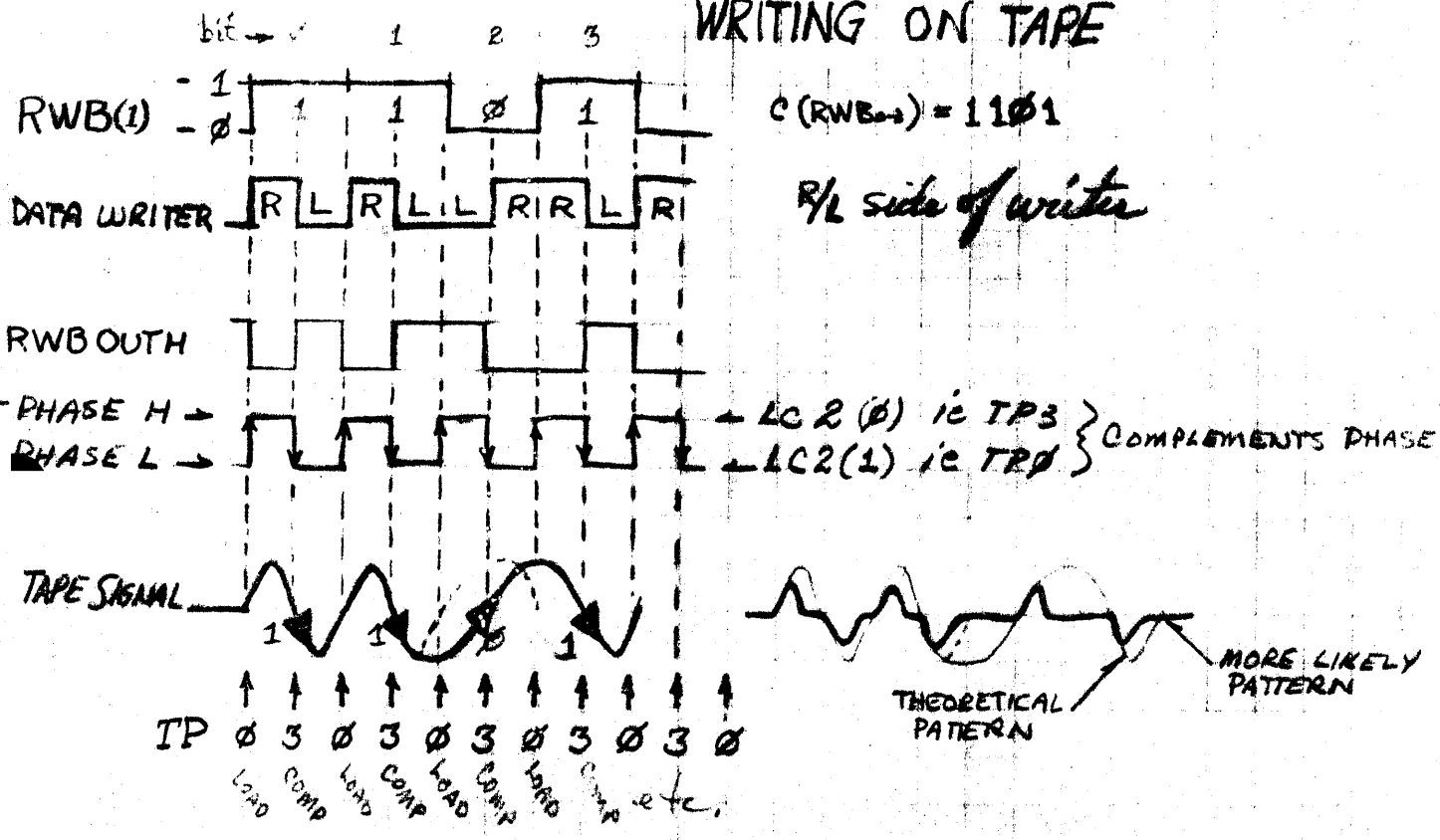
READING BLOCK MARKS (FWD - REV)



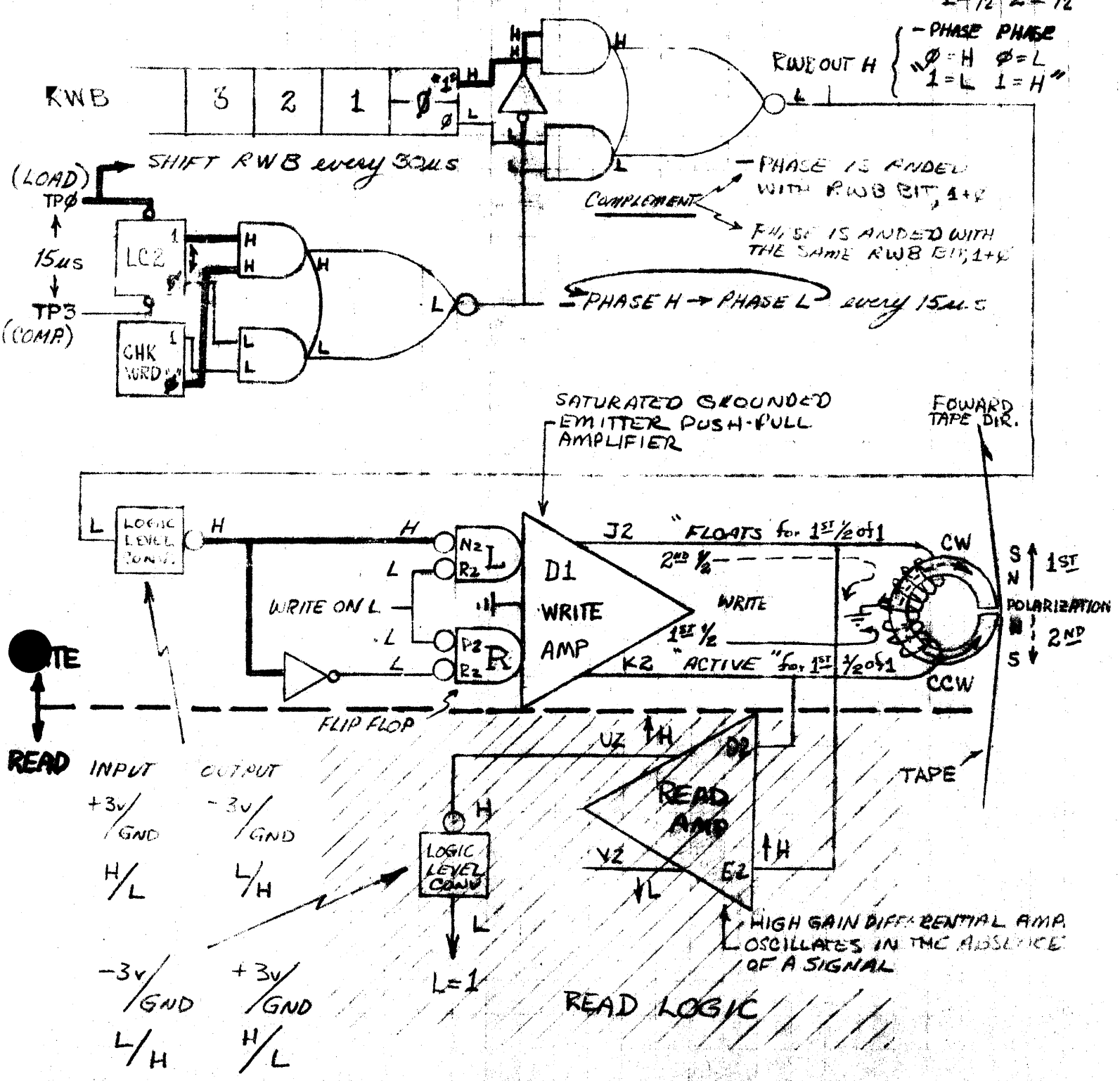
COMPLEMENT OBVERSE



WRITING ON TAPE

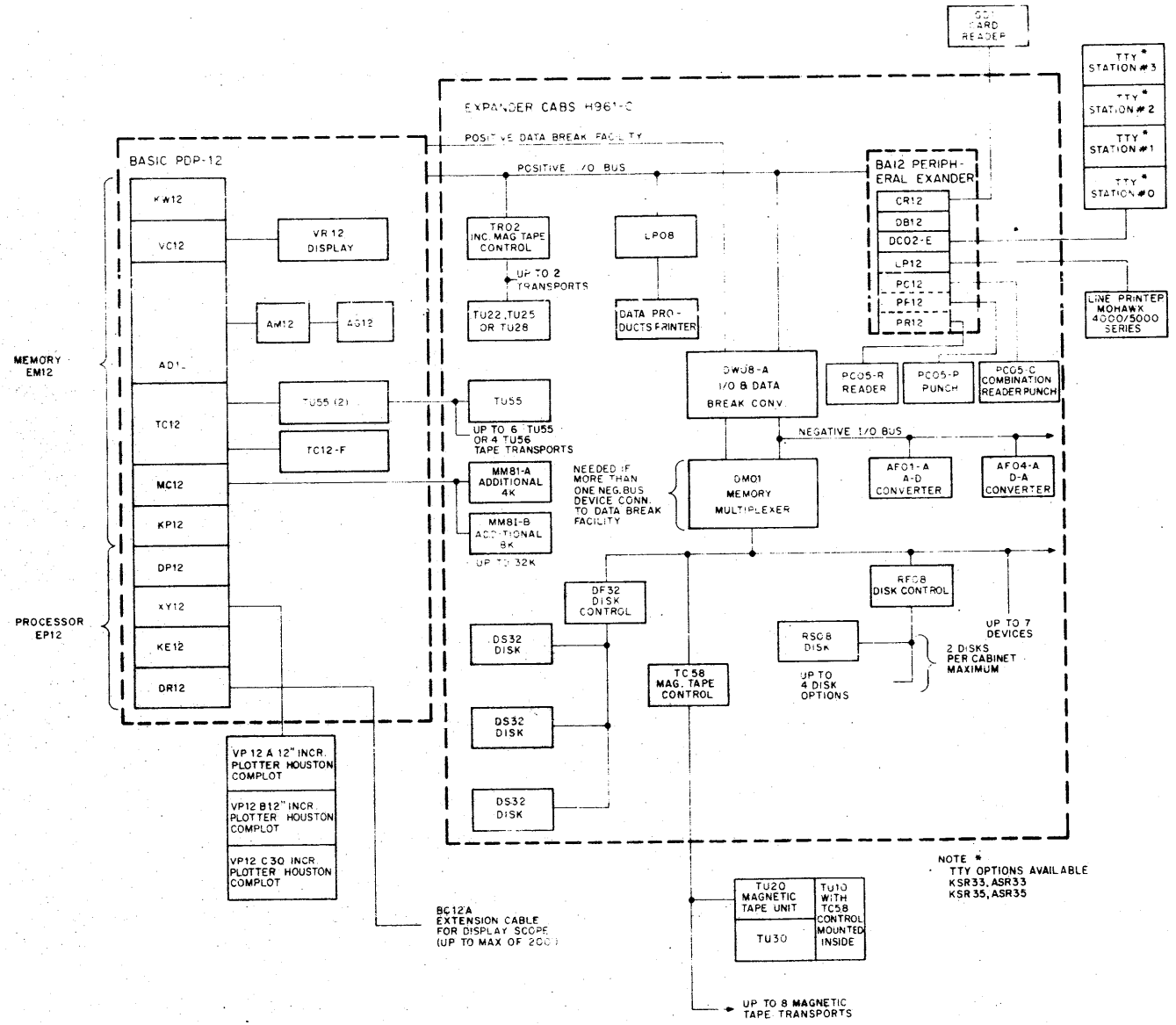


LINC TAPE READER-WRITER & CONTROL

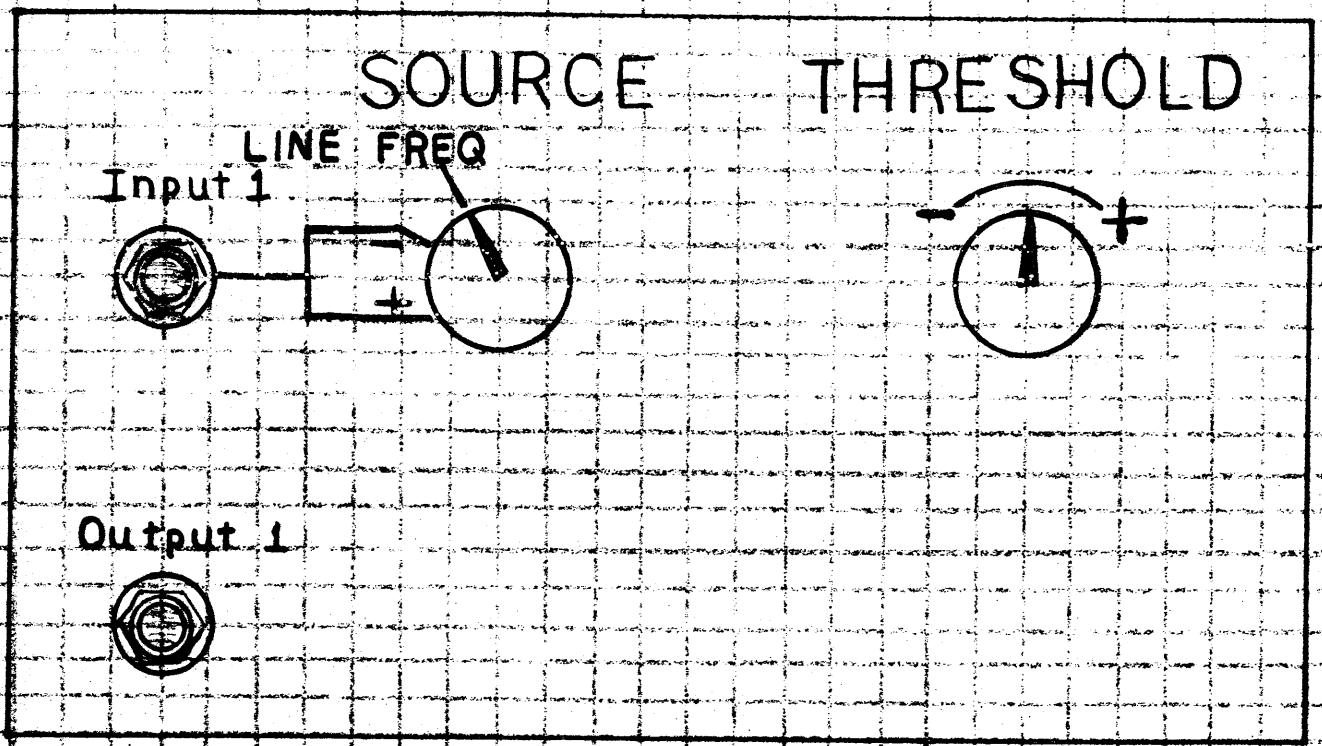


NOTE: POLARITIES SHOWN ON GATES ARE TRUE WHEN THE RWB IS LOADED & LC 2 (Ø) ie, TPØ (ALSO, NOT IN THE CHECK WORD MAJOR STATE). THE RESULT IS ANDED WITH (IN THE EXAMPLE) RWB ØØ (CONSIDER A 1). AT TP3, LC 2 WILL COMPLEMENT ∴ LC 2 → Ø, PHASE ∴ → H AND THE INPUT TO THE WRITER COMPLEMENTS, CHANGING POLARIZATION ON TAPE FROM S → N Ø N → S

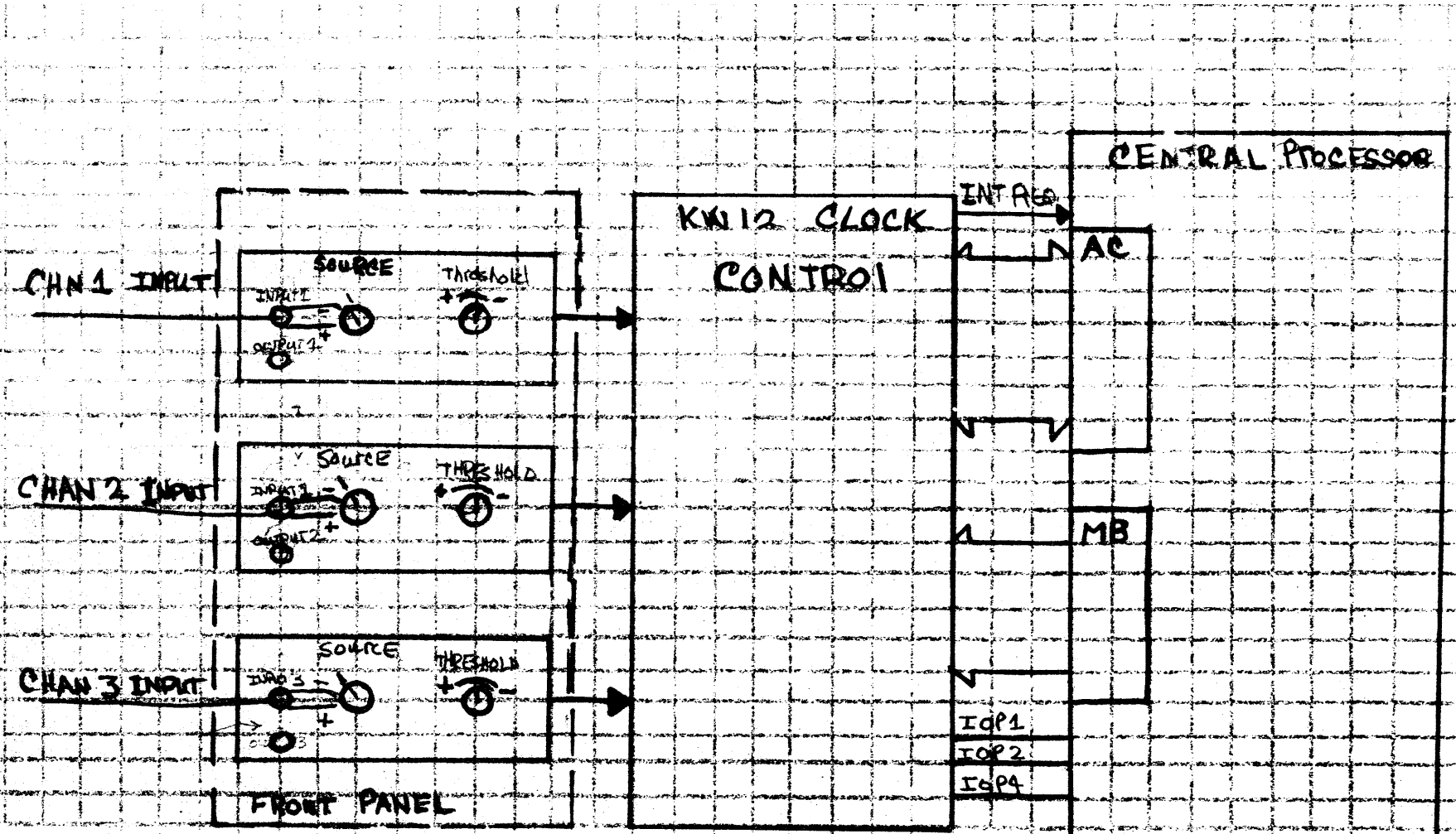
Towne



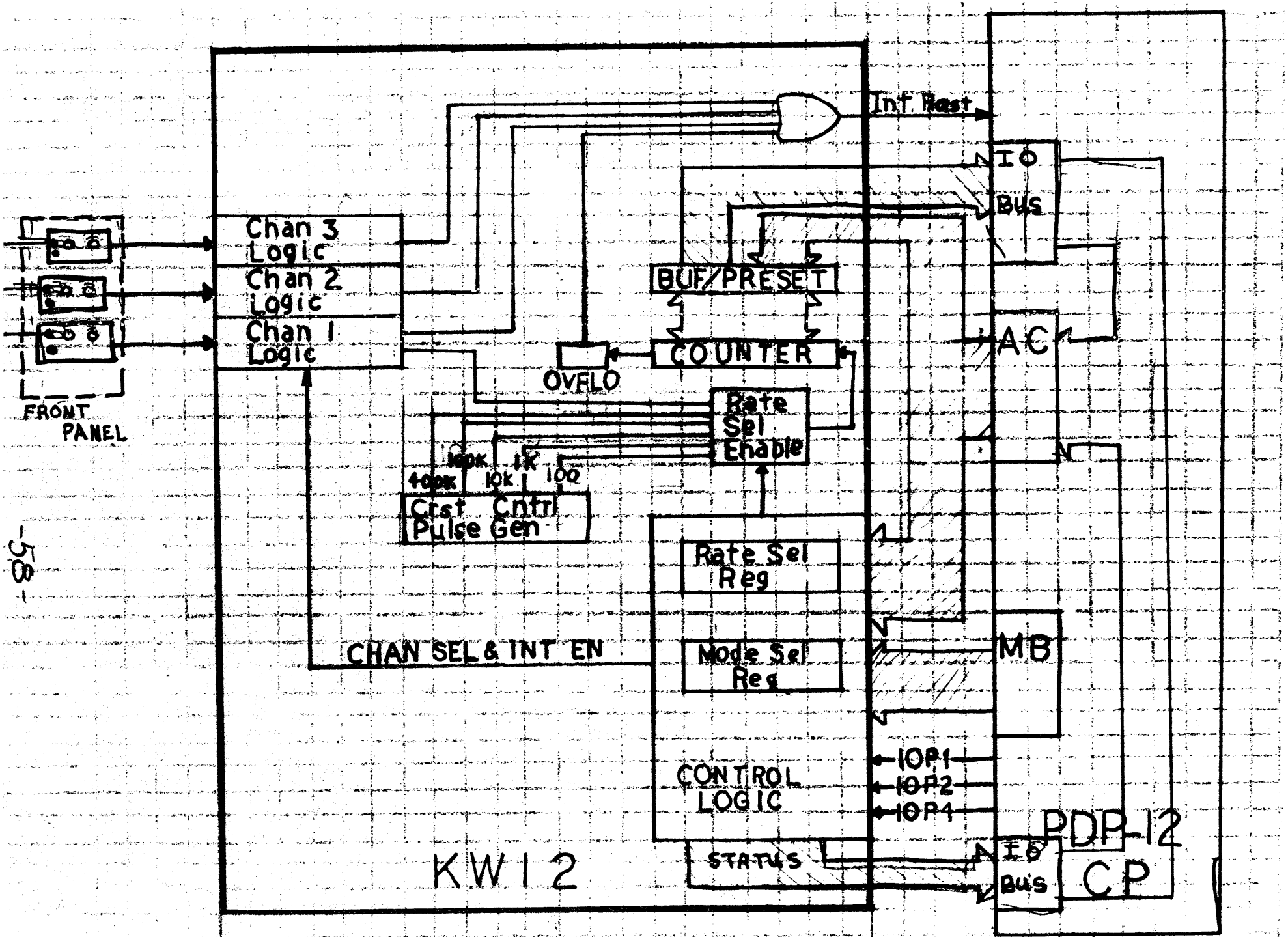
PDP-12 Functional Block Diagram



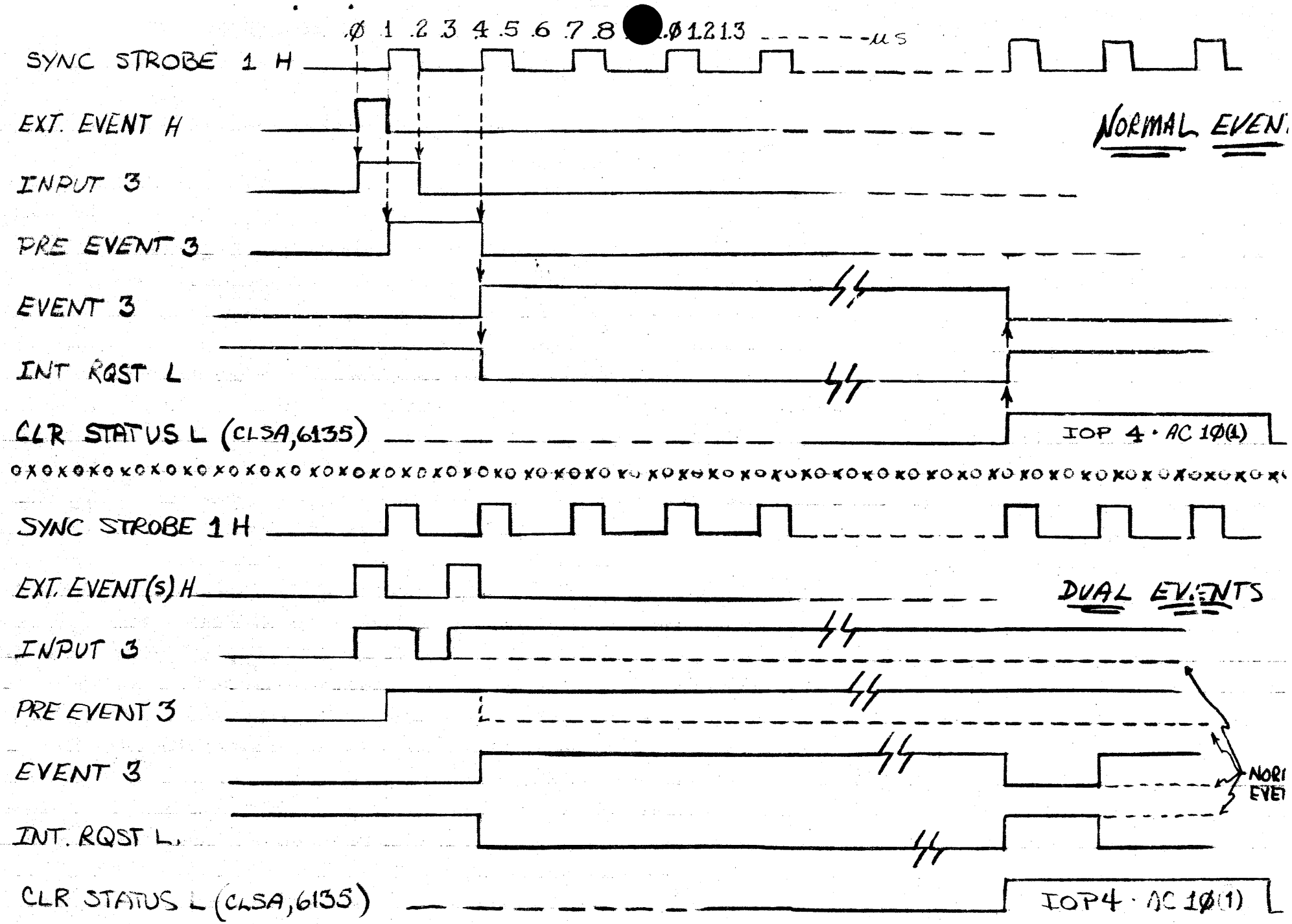
KW12
FRONT PANEL


CENTRAL PROCESSOR
KW12 CLOCK
CONTROL
INT ACK
AC
MB
IOP1
IOP2
IOP4
CHN 1 INPUT
CHAN 2 INPUT
CHAN 3 INPUT
SOURCE
THRESHOLD
FRONT PANEL

KW 12 SYSTEM



KW12 BLOCK DIAGRAM



KW12 - INPUT CHANNEL

TIMING FORMAT

SIGNAL NAME	FETCH					DEFER					EXECUTE				
	T2	T3	T4	T5	T1	T2	T3	T4	T5	T1	T2	T3	T4	T5	T1

DOCUMENTATION FORMAT

PC	MA	MEM	MB	IR	L	AC	CYCLE	INST	TIME
									T
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0001							T2/S
									T3
									T4
									T5 W
									T1
		0002							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0003							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0002							T2/S
									T3
									T4
									T5 W
									T1

DOCUMENTATION FORMAT

PC	MA	MEM	MB	IR	L	AC	CYCLE	INST	TIME
									T
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0001							T2/S
									T3
									T4
									T5 W
									T1
		0002							T2/S
									T3
									T4
									T5 W
									T1
		0003							T2/S
									T3
									T4
									T5 W
									T1
		0004							T2/S
									T3
									T4
									T5 W
									T1
		0005							T2/S
									T3
									T4
									T5 W
									T1

DOCUMENTATION FORMAT

PC	MA	MEM	MB	IR	L	AC	CYCLE	INST	TIME
									T
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0002							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0001							T2/S
									T3
									T4
									T5 W
									T1
		0002							T2/S
									T3
									T4
									T5 W
									T1

DOCUMENTATION FORMAT

PC	MA	MEM	MB	IR	L	AC	CYCLE	INST	TIME
									T
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0002							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1

DOCUMENTATION FORMAT

PC	MA	MEM	MB	IR	L AC	CYCLE	INST	TIME
								T
		0000						T2/S
								T3
								T4
								T5 W
								T1
		0000						T2/S
								T3
								T4
								T5 W
								T1
		0000						T2/S
								T3
								T4
								T5 W
								T1
		0000						T2/S
								T3
								T4
								T5 W
								T1
		0000						T2/S
								T3
								T4
								T5 W
								T1
		0000						T2/S
								T3
								T4
								T5 W
								T1
		0000						T2/S
								T3
								T4
								T5 W
								T1

MARK TAPE, COPY TAPE, PRINT DIAL INDEX EXERCISE

NOTE: See references to paragraphs (ex. 5, 2) on pp. (ex. 1-5) in the LA 6 DIAL Manual

Initial Starting Procedure

1. Place dial tape on top unit.
   Select unit Ø (8) on TU55 transport.

2. Mount another tape on the lower transport.
   Select unit 1.

   NOTE: A. This is only required for commands AS, LI, QL, and SB (See 1.8 commands).
   B. This is also required when using the Mark 12 program.
   C. If this is a new DECtape rather than Linc tape, it must be placed on the left hub and an empty spool on the right hub. The left spool must now be wound on the right using "LOCAL" and "→ (AW)".

3. Set switches on both tape units to "REMOTE" and set unit Ø (8) to "Write Enable".

4. Set the Mode Switch to "LINC" mode and press "IO PRESET" to preset Linc IF 2 and Linc DF to 3.

5. Set "LSW" to Ø7Ø1 and "RSW" to 73ØØ.

   NOTE: Depressing switch on the panel side (of the switch) is a Ø and on the operator side equals a 1.
   If tape comes off the spool, you didn't wind enought of it. Turn "REMOTE" switch "OFF", rewind spool with leader and switch to "REMOTE" again.

6. Press to "DO" switch (memory is initialized by tapes).

7. When tape motion stops, press "START 2Ø" (starting address of Dial)

Dial Program Selection

1. Turn A-D knobs 3 (Cursor Control) and 7 (Line Control) fully CW (See 2.Ø)

2. Using the keyboard, type Linefeed (→ , ▟) "cursor" appears at the lower left of DISPLAY) DX RETURN (↵) to obtain the Dial Index (See 5.4)

3. To view the entire index use the following keys:

KEY	ACTION
1	Forward one frame
2	Forward one line
Q	Backward one frame
W	Backward one line

4. When the MARK 12 program listing is found, perform the following steps using the keyboard.

   A. Strike Key "RETURN and LINE FEED"
      1. Return gets you back to DIAL
      2. Line Feed stations the cursor in the lower left of Display

   B. Type
      1. "LO" (load)
      2. "SPACE" (␣)
      3. "MARK12" (w/no space)
      4. "COMMA" (,)
      5. "Ø"
      6. "RETURN" (↵) MARK12 instructions should be seen on the display.

      Refer to MARK 12 program listing (Program Library)

5. Follow the instructions on the Display.

Returning to DIAL

1. Using the keyboard, type:

   A. "2"
   B. "LINE FEED"

   NOTE: Depending on programs used (other than MARK12) there are numerous ways to remove the current display, typing:

      1. "RETURN" (clears the screen - back to DIAL)
      2. "CONTROL D" (at the same time, gets DIAL back)
      3. "CONTROL P" (together, gets you back to PIP)

Copy Tape

1. "LINE FEED" - cursor moves to lower left.

2. Type "DX & RETURN" (returns Index)

3. Locate PIP (peripheral interchange program) in the Index

4. "RETURN" back to DIAL

5. "LINEFEED" cursor lower left

NOTE: Do not use LO for PIP - has an auto loader type PIP & RETURN.

6. Select "A" (auxilliary options) and "RETURN"

NOTE: At this point tape to be duplicated should be to transport Ø (8)

7. Select "D" (duplicate) and "RETURN"

NOTE: Duplication begins
Observe tape instruction register on the PDP-12 Panel

Tape Inst Reg.
a. 000 702 RDE-Unit Ø (8)
b. 000 706 WRI
c. 000 707 CHK-Unit 1

8. "CONTROL D" together - back to DIAL

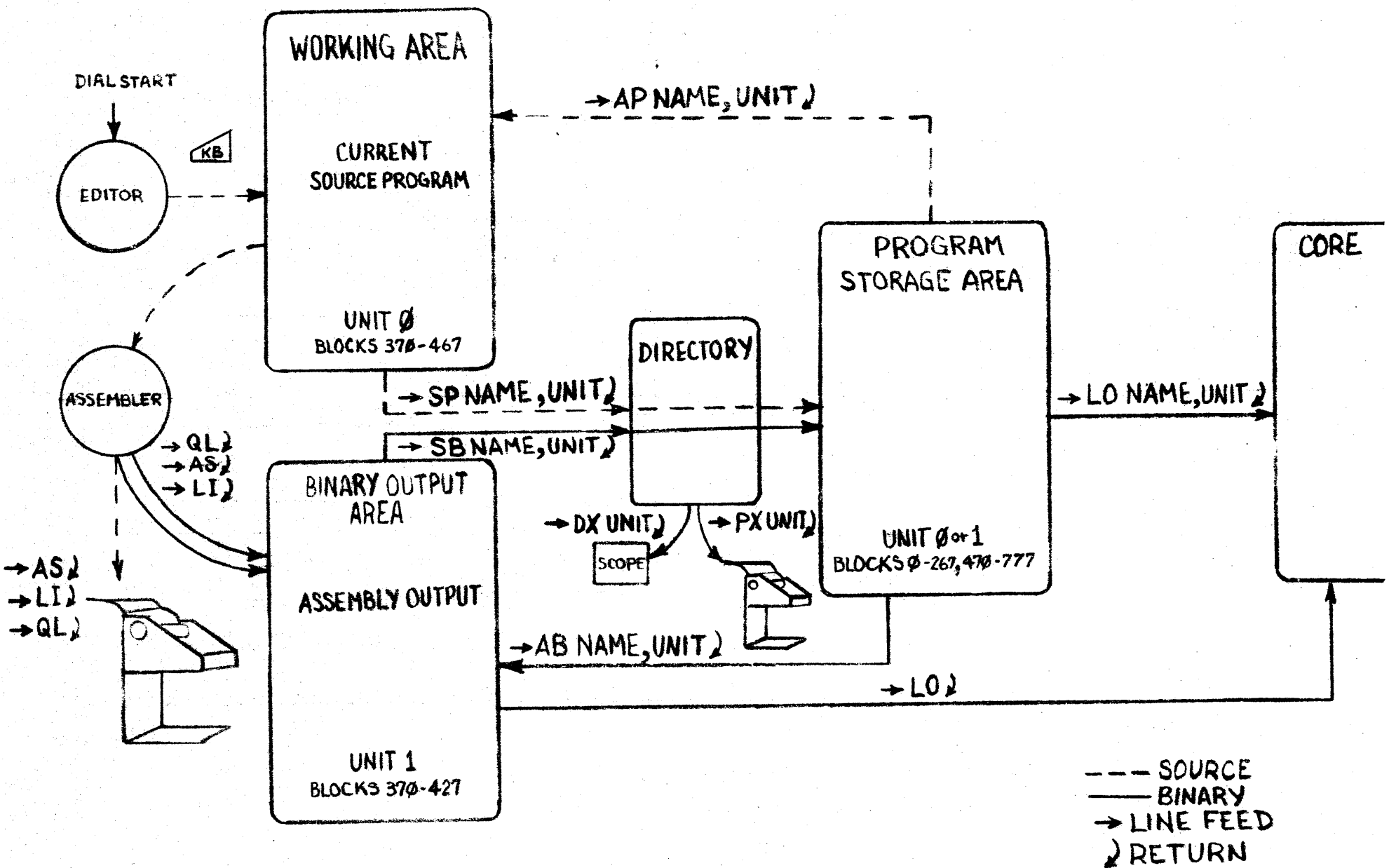
9. Linefeed - cursor lower left.

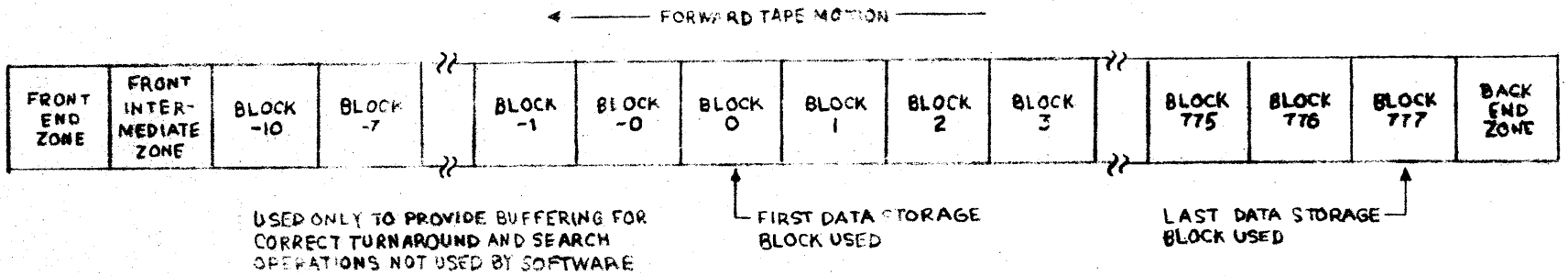
Print Index

1. Linefeed print index unit return (See 5.5)

→ PX (,unit) ↵
Printout occurs

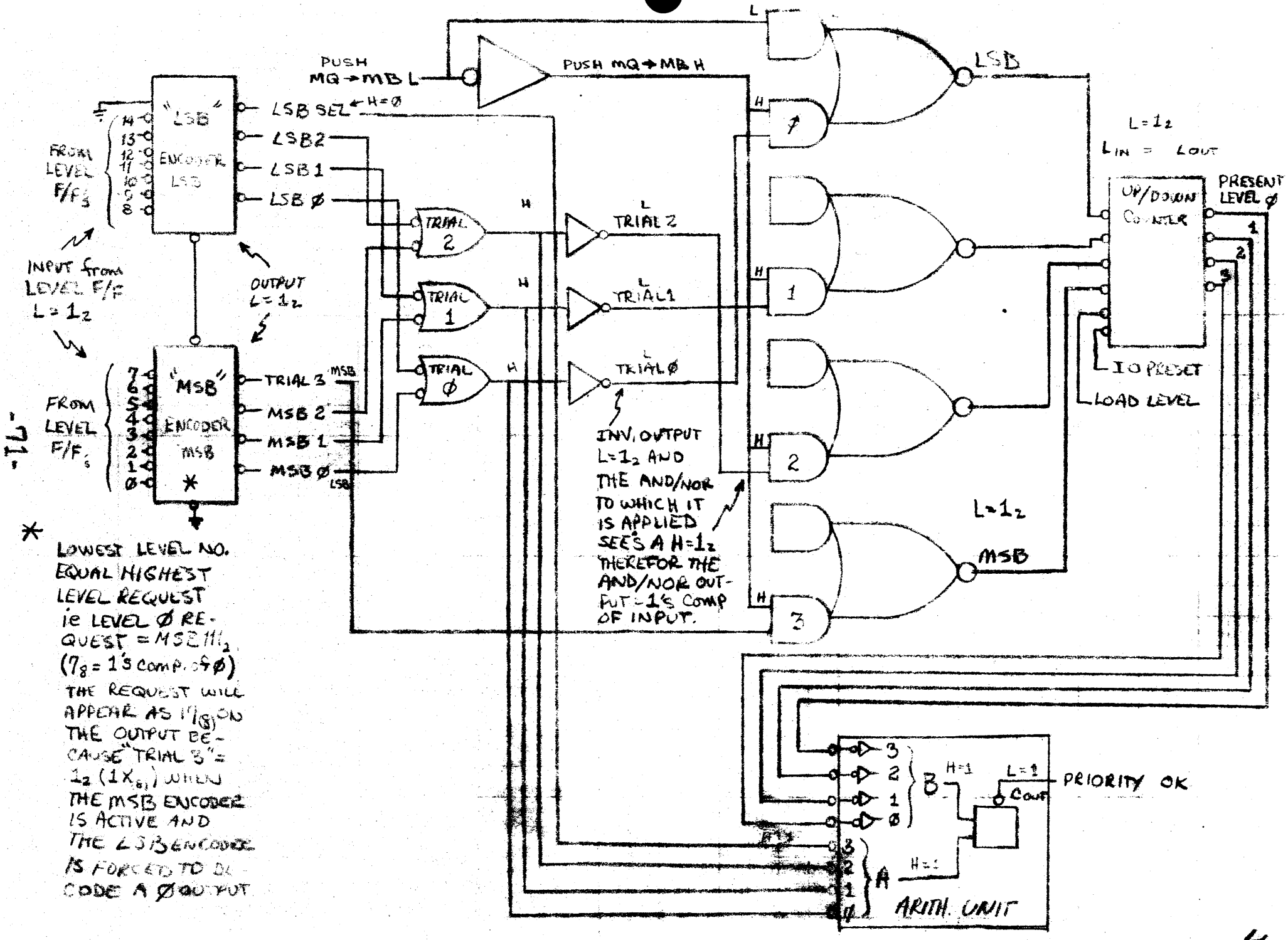
DIAL BLOCK DIAGRAM





LINC TAPE OVERALL FORMAT

INTERRUPT LEVEL PRIORITY



* LOWEST LEVEL NO. EQUAL HIGHEST LEVEL REQUEST ie LEVEL Ø REQUEST = MSB 111_2 (7_8 = 1's COMP. OF Ø) THE REQUEST WILL APPEAR AS $17_{(8)}$ ON THE OUTPUT BECAUSE "TRIAL 3" = 1_2 ($1X_{8_1}$) WHEN THE MSB ENCODER IS ACTIVE AND THE LSB ENCODER IS FORCED TO DO CODE A Ø OUTPUT