DEC-14-HGZA-D (I)

pdp14

MAINTENANCE MANUAL VOLUME I

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Printing March 1970

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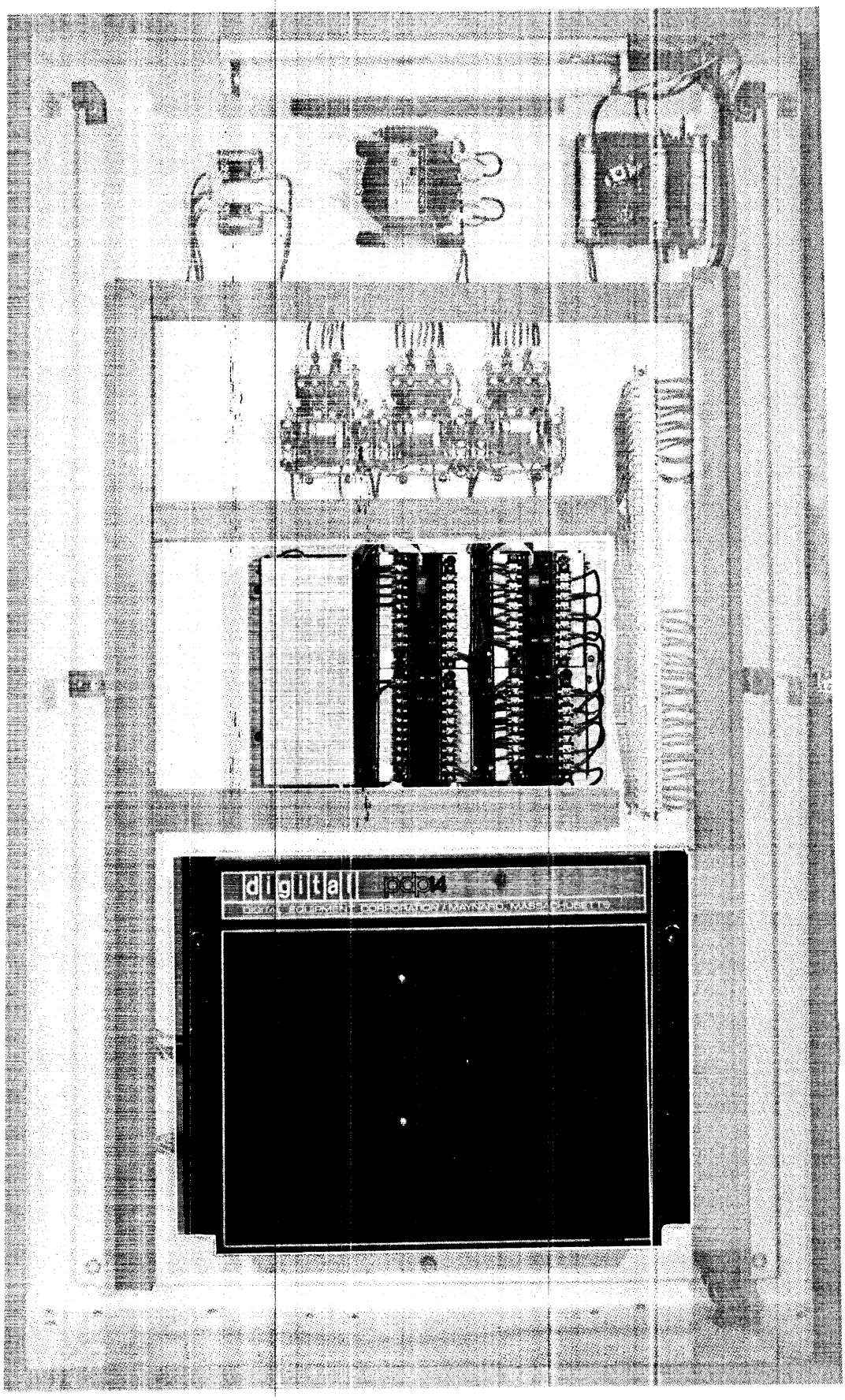


PDP-14 Controller

CHAPTER 1
GENERAL

1.1 PDP-14 SYSTEM

The PDP-14 System is designed to replace relay control systems in industrial and other applications using AC control power. Control relay wiring is replaced by a control program stored in Read Only Memory (ROM) modules located in the PDP-14 mainframe assembly (see Figure 1-1).

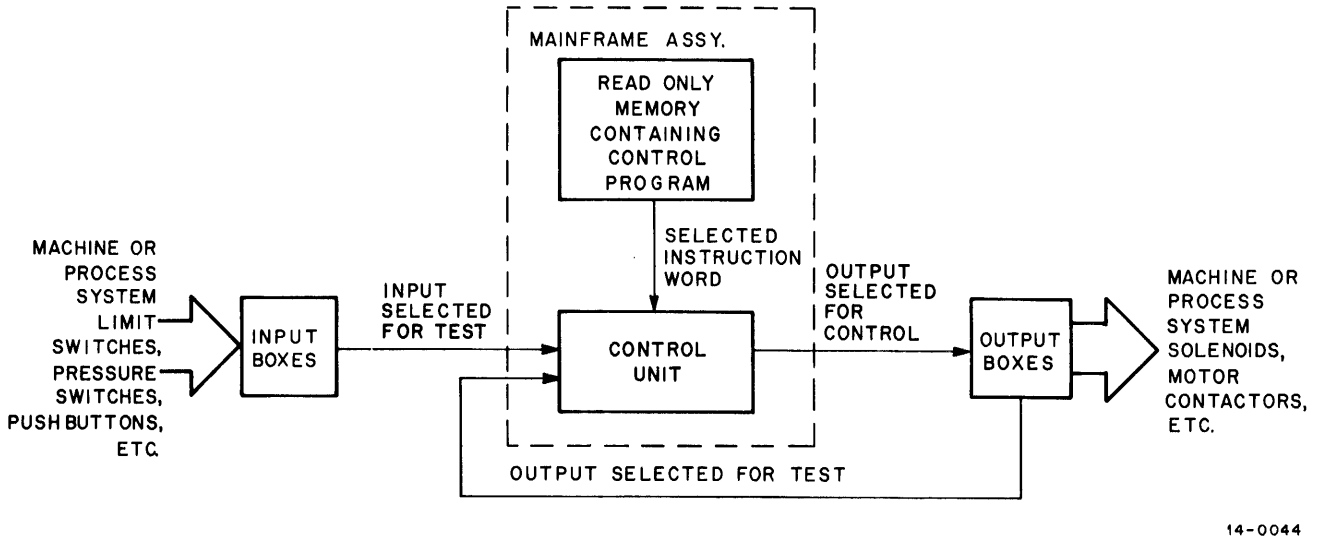


Figure 1-1 PDP-14 Controller, Simplified Functional Diagram

To accomplish its purpose, the PDP-14 tests the status (on or off) of machine or process system limit switches, pressure switches, push buttons, etc, and its own outputs. The PDP-14 compares these conditions, one at a time, with information from the control program within the ROM. The results of these comparisons cause outputs associated with these conditions to be turned on or off.

The basic operation sequence is as follows: first, the control unit obtains an instruction from the control program contained within the ROM (Fetch major state); second, the control unit performs the operation specified by the instruction (Execute major state).

The control program instructions take three basic forms.

a. Test Instructions - These instructions cause the control unit to test an input or output, specified in the instruction, to determine whether that input or output is on or off.

b. Decision-Making Instructions - These instructions are used to determine the future action of the program through the use of conditional jumps performed on the basis of test instruction results. These program jumps lead to additional test instructions and, eventually, to turning a particular output on or off.

c. Control Instructions - These instructions cause the control unit to turn on or off an output specified by the instruction. Additional instructions are used to facilitate transfer of information between the PDP-14 System and an external computer, and to perform internal "bookkeeping" functions.

The PDP-14 User's Manual (DEC-14-GGZA-D) provides detailed programming and installation information, which is beyond the scope of this Maintenance Manual.

1.2 MAINTENANCE LEVELS

Two distinct PDP-14 maintenance levels are presented in this manual. Both levels provide fault isolation and correction procedures; no preventive maintenance is required.

1.2.1 On-Line

Chapter 2 presents maintenance procedures to be performed without disconnecting the PDP-14 from the machine or process system. This material is presented in a step-by-step format in order that the maintenance electrician can rapidly isolate and correct the fault by simply substituting modules, in the rare event the fault is within the PDP-14 Controller.

Although Paragraph 2.3.7 describes a method of fault isolation and correction using only module substitution, it is recommended that the maintenance programs and a test computer be utilized to assist in fault isolation. The test computer (Digital Equipment Corporation, PDP-8/I, PDP-8/L, or PDP-12) can also be used for generation of new control programs as required to meet changes in the machine or process system. A complete package of programs is provided with each PDP-14.

1.2.2 Off-Line

Chapter 4 provides techniques and information required to repair defective modules or other PDP-14 components. The defective module or other components must be removed to a location suitable for repair of relatively delicate

electronic equipment. In addition, personnel performing these procedures must be familiar with digital equipment hardware, electronic and logic schematic diagrams, and electronic equipment repair techniques. These personnel must also thoroughly understand the operation of PDP-14 circuits. To assist in this, Chapter 3 consists of a complete discussion of PDP-14 circuits oriented toward the technician with a good understanding of basic electronic and digital circuits.

Volume II of this manual contains a complete set of engineering physical (parts location) drawings and electrical schematic diagrams of PDP-14 modules to be used with Chapter 4 in fault isolation and repair of defective modules. The techniques in Chapter 4 require a test computer and maintenance programs, in addition to standard electronic test equipment.

1.3 TEST EQUIPMENT AND SPARES

Table 1-1 lists the test equipment required (but not supplied) for the two levels of maintenance. Table 1-2 is a list of recommended spare modules.

Table 1-1
Maintenance Test Equipment

Equipment Description	On-Line Maintenance	Off-Line Maintenance
Test Computer: Digital Equipment Corp. PDP-8/I, PDP-8/L, or PDP-12	Optional (recommended)	Required
Teleprinter: Teletype Corp. 33ASR	Optional (recommended)	Required
Test Computer Interface Pkg.: DA14-I (for PDP-8/I), DA14-L (for PDP-8/L or PDP-12).	Optional (recommended)	Required
Oscilloscope: Bandwidth Min. 5 mHz, Min. Gain 1 V/cm, external trigger or dual trace	Not used	Required
Volt/Ohm Meter: 1,000 ohms/volt	Not used	Optional
Module Extender: Digital Equipment Corp. Type W982	Not used	Required (four)

Table 1-2
Module Spares

Type (one each)	Description	Usage
M740	Instruction Decoder and Register Control	Control Unit
M741	Major States and Timing	Control Unit
M742	PDP-14 Switch and Power Control	Control Unit
M743	K Interface Control	Control Unit
M744	Register Compare Circuit	Control Unit
M745*	PDP-14 to PDP-8/L, -8/I Interface	Control Unit
M746	Bus Register	Control Unit
M747	Incrementing Bus Register	Control Unit
G922	ROM Braid Board	Control Unit
G923	ROM Sense Amplifier	Control Unit
G924	ROM Selection	Control Unit
M921*	Device Code Select Jumper Board	Control Unit
M106*	Dot NOR Gates	Control Unit
K578	AC Inputs	I-Boxes
K614	Isolated AC Switch	O-Boxes
K302**	Two Timers	A-Boxes
K272***	Retentive Memory	A-Boxes
K207	Flip-Flop	O-, S-, and A-Boxes
K161	Binary-to-Octal Decoder	I-, O-, S-, and A-Boxes
K135	Inverters	I-, O-, S-, and A-Boxes
BC14A	Cable	I-, O-, S-, and A-Boxes

*Required only for external computer interface.
**Required only if accessory box time delays are used.
***Required only if accessory box retentive memories are used.

CHAPTER 2

ON-LINE MAINTENANCE

2.1 GENERAL

The PDP-14 Controller requires no periodic maintenance. Maintenance consists of fault isolation and repair in the event of a machine or process system malfunction. Though the PDP-14 Controller is seldom the cause of the malfunction, the neon lamps on the PDP-14 input and output boxes are very useful tools for determining whether the problem is in the machine or process system (and where within the machine or process system) or within the PDP-14 System.

The machine or process system is defined as the machine, or group of machines, under the control of a PDP-14 Controller. The machine or process system includes all control solenoids, limit switches, etc, and all control wiring between these elements and the PDP-14 input and output box terminals.

On-line repair consists of two major steps, which must be performed in sequence:

Step	Procedure
1	Fault isolation to wiring and components outside the PDP-14 Controller or to PDP-14 Controller components; and
2	Localization and repair of the machine or process system wiring or component (limit switch, pushbutton, solenoid, motor contactor, etc), or localization and repair of the PDP-14 Controller by substitution of plug-in components.

Paragraph 2.2 describes the techniques to follow in order to make maximum use of the PDP-14 lamps in locating a defective component outside the PDP-14 Controller.

If it is determined from following the procedures of Paragraph 2.2 that the trouble is definitely within the PDP-14, Paragraph 2.3 contains step-by-step procedures to locate the defective PDP-14 component. On-line repair of the PDP-14 is limited to substituting a properly functioning component (module) for the defective component. If the trouble is determined to be within the PDP-14 Control Unit mainframe but cannot be isolated using the procedures described in Paragraph 2.3, the mainframe must be removed from the NEMA enclosure and sent to a test area where specially trained personnel and electronic test equipment are available to perform detailed troubleshooting and repair procedures.

2.2 MACHINE OR PROCESS SYSTEM FAULT ISOLATION

The techniques described under this heading isolate the malfunction to a machine or process system component (AC control wiring, limit switches, pushbuttons, solenoids, motor contactors, etc), or to the PDP-14 system (input and output boxes, and control unit modules).

2.2.1 Fault Isolation Technique

The machine or process system malfunction is usually apparent at one or more machine stations, or may be indicated by fault indicator lamps on the operator's console. In either case, the machine or process system circuits associated with the fault should be checked, using the neon lamps on the PDP-14 input and output boxes.

If the neon lamps on the PDP-14 input and output boxes disagree with the actual status of the machine, the trouble is not in the PDP-14. Thus, if a carriage reaches the end of its travel and depresses a normally-open limit switch operating lever but the associated input box lamp does not light, the trouble must be in the limit switch or in the wiring to the PDP-14 input box terminal adjacent to the lamp.

If a motor is not running, but the PDP-14 output box lamp corresponding to the contactor for that motor is lighted, the trouble is not in the PDP-14. The trouble is in the AC wiring from the output box to the contactor, within the contactor, in the high power wiring to the motor, or within the motor itself.

However, if the motor fails to run when the carriage activates the limit switch, and the input box lamp associated with the limit switch is lighted but the output box lamp associated with the motor contactor is not lighted, then there is a malfunction within the PDP-14. In other words, if the combination of input box lights, as observed, does not produce the correct output lamp response, the procedures in Paragraph 2.3 must be followed to isolate the trouble to a PDP-14 input or output box or control unit module.

2.2.2 NEMA Enclosure Input and Output Tables

To assist in locating the input box lamps associated with a particular control function, a list is posted inside the NEMA enclosure door to identify each input box terminal. A sample of the input table format is presented in Figure 2-1.

A similar table lists the output box terminals and the conditions required to turn each output on. A sample of the output table format is presented in Figure 2-2.

NOTE

There is usually an interlock on the NEMA enclosure door. This interlock must be defeated in order to observe output box lamps.

Input Box Terminal Assignments

Input Box and Terminal Number	Input Device Identification	Functional Description of Active State	Input Device X Number
A8	UNCLAMP Pushbutton, 10PB	Applies power to input terminal when pressed.	X10
A16	Head Retracted Limit Switch, 4LS	Applies power to input terminal when machine head is fully retracted.	X20
A14	Clamps In Limit Switch, 1LS	Limit switch applies power to input terminal when clamp is engaged.	X16
A17	Clamps Out Limit Switch, 5LS	Limit switch removes power from input terminal when clamp is released.	X21

Figure 2-1 NEMA Enclosure Input Box Terminal Assignment Table With Sample Entries

Output Box Terminal Assignments

Output Device Identification	Output Device Control Equation X=Input Terminal, Y=Output Terminal, +=OR, *=AND, /=NOT	Output Device Y Number
Red AUTOMATIC Console Lamp, 2LT	;1. 2LT=3PB*(4PB+2LT)*/3LT Y0 = X0*(X1 + Y0)*/Y1	Y0
Amber MANUAL Console Lamp, 3LT	;2. 3LT=3PB*(5PB+3LT) Y1 = X0*(X2 + Y1)	Y1
Machine Head FULL DEPTH Amber Console Lamp, 5LT	;9. 5LT = (3LS*/4LS)+(1LS*2LS*5LT) Y2 = (X16*/X17)+(X15 * Y2)	Y2
Release Clamp Solenoid B	;14. SOLB = 4LS*3LT*10PB+[(1LS*2LS*5LT+SOLB)*/5LS*/6LS*2LT] Y5 = X17*Y1 * X7 +[(X15 * Y2+ Y5)* /X20 *Y0]	Y5

Figure 2-2 NEMA Enclosure Output Box Terminal Assignment Table With Sample Entries

The input and output box terminals are numbered in octal from top to bottom starting with the lamp in the top left corner then down the right row of lamps (0_8 through 37_8 for input boxes, 0_8 through 17_8 for output boxes).

The right-hand column of the Output Box Terminal Assignment Table defines the conditions required to turn a particular output ON. These conditions are stated in Boolean algebra, which is simply a shorthand method of describing the conditions necessary to turn on the output box terminal. The slash symbol (/) is used to indicate negation of a signal; e.g., /X17 means NOT X17.

When the asterisk symbol (*) appears between two terminal designators, the conditions on either side of the asterisk MUST be present in order to satisfy that portion of the statement. Thus

X16*/X17

means that the lamp associated with input terminal X16 must be on, and the lamp associated with input terminal X17 must be off in order to turn the output terminal ON.

When the plus symbol (+) appears between two terminal designators, either one or the other condition flanking the plus symbol (or both) must be present in order to satisfy that portion of the statement. Thus

X16+/X17

means that the lamp associated with input terminal X16 must be on, or the lamp associated with input terminal X17 must be off (or both conditions) in order to turn the dependent output ON.

Parentheses are used to combine a group of conditions to be considered a SINGLE condition in relation to other conditions outside the parentheses. Thus the Boolean statement

X16*(/X17+X15)

means that either the lamp associated with input terminal X17 be off, or the lamp associated with input terminal X15 be on; and, in addition to this requirement, the lamp associated with input terminal X16 must be on.

Several sets of parentheses, nested one within the other, may be used in a single Boolean equation. Always check lamps starting with those outside any parentheses, then check those within the innermost sets of parentheses--noting whether or not the relationship within a single set of parentheses is satisfied before going to the next wider set of parentheses. In this way it can be determined if the combination of lamps, as observed, should cause the associated output lamp to light. Thus

X16* ((/X17 + Y13) * X15)

means the lamp associated with input terminal X17 must be off, or the lamp associated with output terminal Y13 must be on, or both. If one of these three possibilities is observed on the lamps, then, additionally, the lamp associated with input terminal X15 must be on. If the conditions described thus far are observed in some form, then the lamp associated with input terminal X16 must also be on in order for the output lamp and circuit controlled by this relationship to be turned on.

NOTE

Whenever groups of parentheses are encountered, always work from the innermost sets, then consider the contents of the innermost sets as single conditions to be considered in relation to the other conditions bracketed by the next wider set of parentheses.

2.2.3 System Troubleshooting Example #1, Control Input Device Malfunction

As an example of the system troubleshooting procedure, assume that an automatic transfer line machining engine blocks is stopped by a malfunction. A visual check of the line reveals that the left-hand clamp holding the blocks under a particular machining head is still clamped, even though the engine block at that station has already been machined and the clamp should have released. The trouble is therefore associated with the clamp and its control circuitry.

The NEMA enclosure housing the PDP-14 is opened (the interlock must be defeated) and the solenoid controlling the clamp release is located in the output box terminal assignment table inside the NEMA enclosure door (see sample entries in Figure 2-2). The PDP-14 Output Box and terminal number associated with the clamp release solenoid are noted, and the lamp associated with that terminal is observed.

The lamp associated with the clamp solenoid is not lighted. This does not mean that the PDP-14 has malfunctioned. It simply means that the trouble is apparently not in the clamp release solenoid or the control wiring between the output box and the solenoid.

It is now necessary to return to the output box terminal assignment table and compare the conditions required to turn on output box terminal Y6 with the existing state of the input and output box lamps. It is observed that the lamp associated with input terminal X20 is not lighted. As this condition is necessary in order to activate output terminal Y6, it can now be assumed that the trouble is definitely not in the PDP-14 system, but must be in the outside circuit associated with input terminal X20.

The input box terminal assignment table is now consulted, and it is found that input terminal X20 is connected to limit switch 4LS, which should be ON when the machine head is fully retracted (see sample entries in Figure 2-1). The machine head is observed to be fully retracted; therefore, the trouble must be in the limit switch or its associated wiring. A check of the limit switch reveals that it has, in fact, failed. Replacing the switch puts the line back in production again.

2.2.4 System Troubleshooting Example #2, Control Output Device Malfunction

The same machine system malfunction described in Paragraph 2.2.3 is observed. This time the lamp associated with output terminal Y6 is lighted. The trouble is not in the PDP-14 System, but must be in the solenoid, in the wiring between the output box and the solenoid, or in the machinery between the solenoid and the clamp. Examination reveals that a defective hydraulic valve, controlled by the solenoid, prevented release of the clamp. The valve is replaced and the line put back in production.

2.2.5 System Troubleshooting Example #3, PDP-14 System Malfunction

The same machine system malfunction described in Paragraph 2.2.3 is observed. This time the lamp associated with output terminal Y6 is not lighted, but all the conditions required to activate output terminal Y6 are present. The trouble must be assumed to be in the PDP-14 System.

NOTE

Each PDP-14 Output Box terminal is fused. If it is suspected that an output load has exceeded five amperes, the output circuit should be repaired to remedy the overcurrent condition (shorted wiring, solenoid winding, etc), and the output box fuse associated with that terminal should be checked. If the output box fuse is blown, the lamp associated with that output will not light.

If the trouble is in the PDP-14 system, the procedures in Paragraph 2.3 must be followed to isolate the trouble to a control unit module or to an input or output box.

2.3 PDP-14 SYSTEM FAULT ISOLATION

The procedures under this heading should not be performed until the procedures described in Paragraph 2.2 have been performed and the trouble has been definitely isolated to the PDP-14 System. The test computer procedures in Paragraphs 2.3.1 through 2.3.6 must be performed in sequence, the one exception being that the procedure in Paragraph 2.3.4 may be performed first if it is suspected that an output box fuse has been blown because of a control output short or other circuit overload conditions.

If an external computer is not available for fault isolation, Paragraph 2.3.7 describes a few simple substitution techniques which may be used to isolate the defective PDP-14 System module.

2.3.1 PDP-14 Control Unit and Storage Box Checkout Procedure

CAUTION

PDP-14 and/or test computer circuits may be damaged if modules or connectors are inserted or removed with power ON.

Step	Procedure
1	Remove PDP-14 control unit shield cover.
2	Connect test computer (PDP-8/I or PDP-8/L) system power cable to convenience outlet on PDP-14 control unit switch panel.
3	Place PDP-14 Control Unit and Test Computer Panel Switches in OFF position.
4	Connect three control cables between the test computer and the PDP-14 control unit as follows:

From PDP-14 Location	To Test Computer		
	PDP-8/I Location	PDP-8/L Location (4K) (8K)	PDP-12 Location
A19	J05 & J06	D34 B34	N16
A20	J03 & J04	D35 B35	N15
B20	J01 & J02	D36 B36	N14

5 Disconnect all Input (I) Box, Storage (S) Box, Accessory (A) Box, and Output (O) Box cables from PDP-14 control unit mainframe.

NOTE

These connectors should be labeled with the I or O box letter designator or mainframe location designator to facilitate replacement when testing is completed.

6 Insert all storage box (S-Box) cable connectors into adjacent PDP-14 mainframe output box locations (see Figure 2-3). Always insert full S-Box cable connectors first, making certain that cables leaving the top of the S-Boxes are connected to mainframe row C connectors and cables leaving the bottom of the S-Boxes are connected to the mainframe row D connectors.

NOTE

Any number of "full" S-Boxes can be checked at one time, but only one half S-Box can be checked at one time, and its cable connector must be inserted into the last sequential mainframe output box connector (this will always be in row C). If additional half S-Boxes must be checked, the first half S-Box tested must be disconnected at the mainframe, the next half S-Box cable connected, and the entire test cycle repeated.

7 Place PDP-14 control unit and test computer power switches in ON position.

8 Place PDP-14 START/STOP switch momentarily in STOP position.

9 Set test computer SWITCH REGISTER to 7777_8. The correct switch configuration for this is

111 111 111 111

10 Press the LOAD ADDRESS switch on test computer.

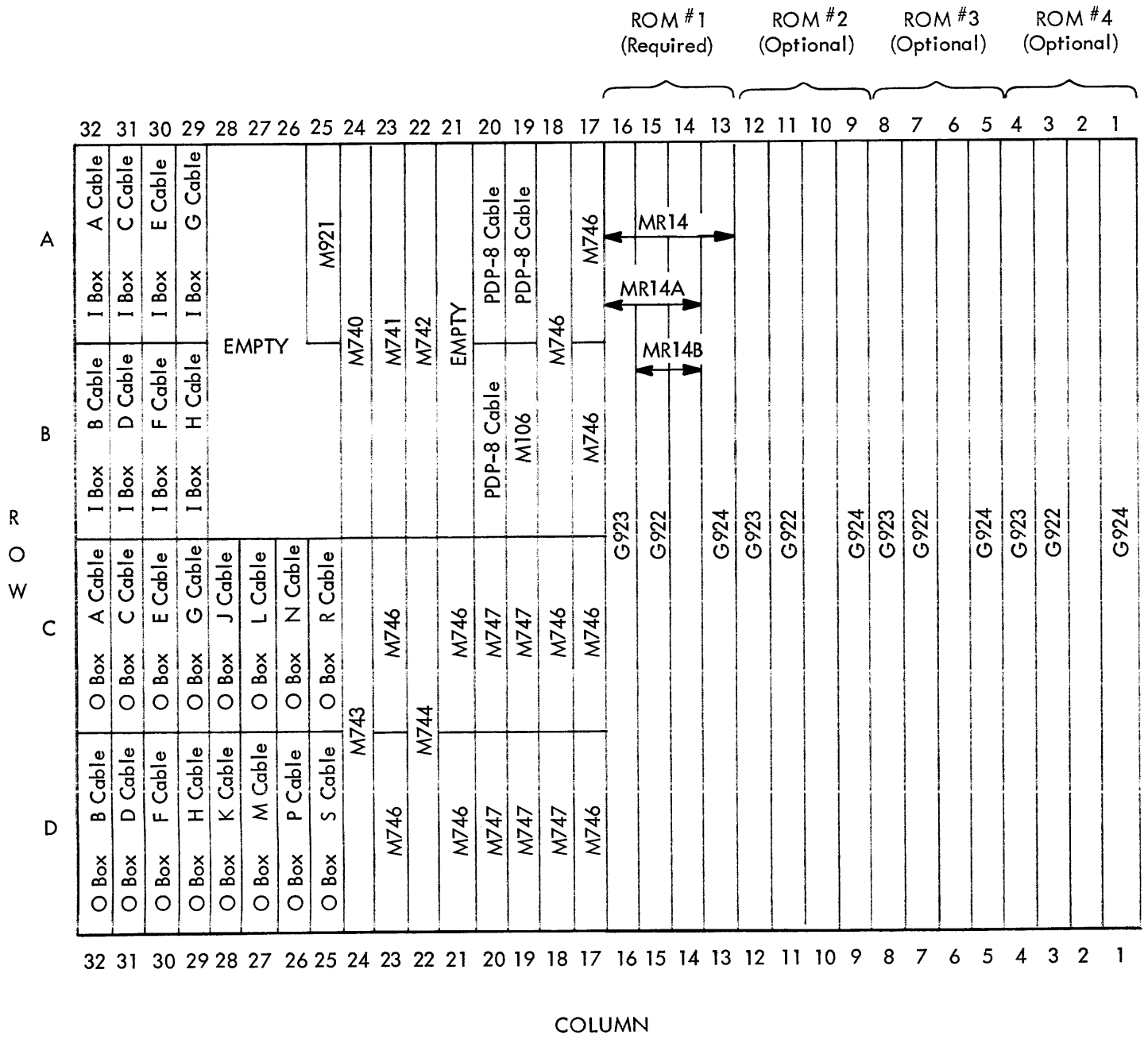


Figure 2-3 Mainframe Module and Cable Connector Map, Front View

NOTES:

1. Maximum Mainframe Configuration Shown.
2. O Box Letter Designators "I", "O", and "Q" are not used to Prevent Confusion With Numbers "1" and "0".

Step	Procedure
11	Load the TEST-14 paper tape into the test computer teleprinter paper-tape reader as follows: a. Set the reader START/STOP/FREE switch to the FREE position. b. Release the cover guard by means of the latch at the right and open cover. c. Insert the leader (start) end of the punched tape from the rear over the reader sprocket wheel so that the small holes in the tape engage the sprocket teeth and there are 3 holes spaces on the tape to the left of the sprocket wheel. The leader portion of tape has a single row of large holes and a single row of small holes. d. Close reader cover.
12	Place paper-tape reader START/STOP/FREE switch to START position.
13	Press test computer START switch momentarily. Tape should now move through reader until it is completely read and only the trailing portion remains in the reader.
	NOTE If tape stops before it has been completely read, place tape leader in reader and press test computer CONT switch momentarily.
14	Remove the trailing portion of the TEST-14 paper tape from the reader by releasing the cover guard with the latch and opening the reader cover. Lift the tape off the sprocket wheel.
15	Enter the number 200_8 on test computer console SWITCH REGISTER. The correct switch configuration for this is 000 010 000 000
16	Press the LOAD ADDRESS switch on test computer console.
17	Enter the following configuration in the SWITCH REGISTER switches: 000 000 000 000 if PDP-14 control unit module positions C20 and D20 are empty, or enter 000 000 100 000 if PDP-14 control unit module positions C20 and D20 contain modules.
18	Press the START switch on test computer console. Program will type HOW MANY-I-BOXES?
19	Respond to this question by typing the number zero. 0 then press the carriage return (RETURN) key.

Step	Procedure
19 (Cont)	NOTE Do not type the letter "o". This character is not recognized by the test program. Program will type HOW MANY 0-BOXES?
20	Respond to this question by typing the number zero. 0 Then press the RETURN key. The program will type HOW MANY HALF S-BOXES?
21	Respond to this question by typing the number of S-Box connectors inserted in succeeding output box connector locations, then press RETURN key. NOTE Do not type the letter "I". This character is not recognized by the test program. The test program will now start and run automatically. If the program types PASS 1 COMPLETE the PDP-14 has been tested and found to be operating properly. In this case, the problem can be assumed to be in an Input or Output box or in the machine control program; proceed to Paragraph 2.4. If the program types anything else, proceed to the following step. NOTE If the test program types PDP-14 STOPPED, substitute PDP-14 control unit modules at locations AB23 (M741) and AB22 (M742). If the test program types PDP-14 HUNG, or if the test computer RUN lamp goes out, substitute PDP-14 control unit modules at locations AB23 (M741) and AB18 (M745).
22	If the test program detects a malfunction in the PDP-14 control unit, the program will identify the problem area by typing a two-letter error code flanked by asterisks. The module locations referenced by each two-letter error code are identified in Table 2-1. Module types are presented in parentheses following the module locations (a module map is presented in Figure 2-3). Substitute the module at the first location listed for a particular error code in Table 2-1.
23	Press test computer STOP switch. Enter 201_8 in switch register. The correct switch configuration for this is 000 010 000 001

Table 2-1
Test Program Error Code/Module Location Cross Reference

Error Code Typed	Module Location/ (Type)	Error Code Typed	Module Location/ (Type)
AA	AB18 (M745) A17 (M746) B17 (M746) C17 (M746) D17 (M746) C18 (M746) D18 (M746) AB23 (M741) AB24 (M740) C23 (M746) D23 (M746)	**AJ**	AB24 (M740) C23 (M746) D23 (M746)
		AK	Same as **AJ**
		AL	Same as **AJ**
		AM	Same as **AJ**
		AN	Same as **AJ**
		AO	Same as **AJ**
AB	C19 (M747) D19 (M747) C18 (M746) D18 (M746) AB24 (M740) C23 (M746) D23 (M746)	**AP**	Same as **AJ**
		AQ	Same as **AJ**
		AR	AB23 (M741) AB24 (M740) C23 (M746) D23 (M746)
AC	C21 (M746) D21 (M746) C18 (M746) D18 (M746) AB24 (M740) C23 (M746) D23 (M746)	**AS**	AB23 (M741) CD22 (M744) AB24 (M740) C23 (M746) D23 (M746)
		AT	Same as **AJ**
		AU	Same as **AJ**
AD	C20 (M747) D20 (M747) C18 (M746) D18 (M746) AB24 (M740) C23 (M746) D23 (M746)	**AV**	Same as **AJ**
		AW	CD22 (M744) AB24 (M740) C23 (M746) D23 (M746)
		AX	Same as **AJ**
AE	Same as **AB**	**AY**	Same as **AJ**
AF	Same as **AD**	**AZ**	Same as **AJ**
AG	Same as **AB**	**BA**	Same as **AJ**
AH	Same as **AD**	**BB**	Same as **AJ**
AI	AB18 (M745) AB23 (M741) C19 (M747) D19 (M747) C18 (M746) D18 (M746) AB24 (M740) C23 (M746) D23 (M746)	**BC**	Same as **AJ**
		BD	Same as **AJ**
		BE	Same as **AJ**
		BF	Same as **AJ**
		BG	Same as **AJ**

Table 2-1 (Cont)
Test Program Error Code/Module Location Cross Reference

Error Code Typed	Module Location/ (Type)
BH	CD24 (M743) S Box † AB22 (M742) AB23 (M741) AB24 (M740) C23 (M746) D23 (M746)
BI	Same as **BH**
BJ	CD24 (M743) AB24 (M740) C23 (M746) D23 (M746)
BK	Same as **BJ**
BL	Same as **BH**
BM	AB22 (M742) CD24 (M743) AB24 (M740) C23 (M746) D23 (M746)
BN	Same as **BH**
BO	AB23 (M741) AB24 (M740) C23 (M746) D23 (M746)
BP	Same as **BO**
BQ	Same as **BH**
BR	Same as **BO**
BS	Same as **BH**
BT	Same as **BO**
BU	Same as **BO**
BV	Same as **BJ**
BW	Same as **BO**
BX	Same as **BH**
BY	Same as **BH**
BZ	Same as **BJ**
CA	Same as **BJ**
CB	Same as **BH**
CC	Same as **BH**
CD	AB18 (M745) AB24 (M740) C23 (M746) D23 (M746)
CE	C19 (M747) D19 (M747) AB22 (M742) AB24 (M740) C23 (M746) D23 (M746)

†Refer to Paragraph 2.3.2.

Step	Procedure
24	Press the LOAD ADDRESS switch on test computer console. Test program will now be repeated without typing questions. If the same error code is typed as was typed during the previous test pass, substitute the module at the next location listed for that error code in Table 2-1. Continue to repeat this step until program types PASS COMPLETE (regardless of pass number). The module just substituted is defective and should be returned to the proper facility for repair.
25	If all modules have been substituted and the same error code is again typed, or if the program types something other than a two-letter error code flanked by asterisks, the control unit mainframe must be repaired off line, using information provided in Chapters 3 and 4 of this manual.
26	If the control unit and S-Boxes are functioning properly, proceed to Paragraph 2.3.2 to check the PDP-14 Program Storage modules.

2.3.2 PDP-14 Storage Box Fault Isolation Procedure

The storage boxes are checked by the test computer during the procedure described in Paragraph 2.3.1 above. If error code **BH** (or any of the codes listed subsequently in Table 2-1 which refer to **BH**) is typed by the test computer, the control unit module at location CD24 should first be substituted.

If, upon repeating the test program, the same error code is printed, the following procedure should be performed to check out the suspected storage box:

Step	Procedure
1	Note the leftmost 4-digit number associated with the error code.
2	Locate this number in Table 2-2. (The numbers are listed in sets of 4.)
3	Note the mainframe location designator directly above the group of numbers in Table 2-2 which contains the printed number.
4	Observe the S-Box connector inserted at this mainframe location. This connector should identify the S-Box with which it is associated.
5	Turn test computer and PDP-14 system OFF.
	CAUTION Failure to shut down test computer and PDP-14 System before removing or inserting modules can damage PDP-14 System components.
6	Remove the cover from the S-Box identified in step 4 by loosening eight 5/16 hex head screws which secure the cover to the S-Box shell.
7	Referring again to Table 2-2, substitute the module at the S-Box locations listed in the right-hand column, directly across from the group of numbers in the Table containing the number printed by the program (see Figure 2-4). Turn PDP-14 and test computer ON, and repeat the test (Paragraph 2.3.1) from step 16 until the defective module is located.

Table 2-2
Test Program Address/S-Box Module Location Cross Reference Table

	NOTE: In order for this table to be valid, all S-Box cables must be inserted in sequence in the mainframe O-Box locations. Upper S-Box cables must be inserted in mainframe row C and lower S-Box cables must be inserted in mainframe row D.								Replace S-Box Module at Location/ (Type)
	Upper S-Box Cable connected to Mainframe Module Location (see Figure 2-3)								
	C32	C31	C30	C29	C28	C27	C26	C25	
Leftmost 4-digit number typed by program	0000-0003	0040-0043	0100-0103	0140-0143	0200-0203	0240-0243	0300-0303	0340-0343	A4(K207) B3(K161) A2(K135)
	0004-0007	0044-0047	0104-0107	0144-0147	0204-0207	0244-0247	0304-0307	0344-0347	B4(K207) B3(K161) A2(K135)
	0010-0013	0050-0053	0110-0113	0150-0153	0210-0213	0250-0253	0310-0313	0350-0353	A1(K207) B2(K161) A2(K135)
	0014-0017	0054-0057	0114-0117	0154-0157	0214-0217	0254-0257	0314-0317	0354-0357	B1(K207) B2(K161) A2(K135)
	Lower S-Box Cable connected to Mainframe Module Location (see Figure 2-3)								
	D32	D31	D30	D29	D28	D27	D26	D25	
Leftmost 4-digit number typed by program	0020-0023	0060-0063	0120-0123	0160-0163	0220-0223	0260-0263	0320-0323	0360-0363	C4(K207) C3(K161) D2(K135)
	0024-0027	0064-0067	0124-0127	0164-0167	0224-0227	0264-0267	0324-0327	0364-0367	D4(K207) C3(K161) D2(K135)
	0030-0033	0070-0073	0130-0133	0170-0173	0230-0233	0270-0273	0330-0333	0370-0373	C1(K207) C2(K161) D2(K135)
	0034-0037	0074-0077	0134-0137	0174-0177	0234-0237	0274-0277	0334-0337	0374-0376	D1(K207) C2(K161) D2(K135)

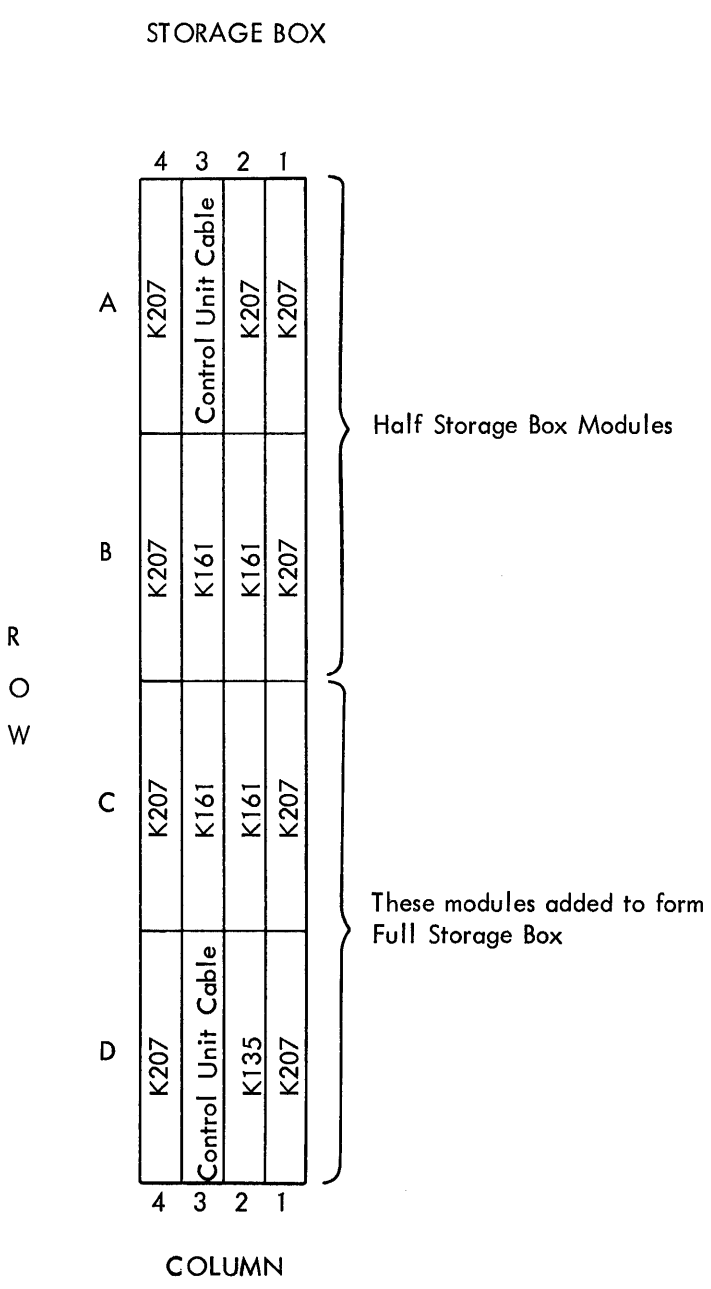


Figure 2-4 Storage Box Module and Cable Connector Map, Front View

Step	Procedure
8	If the fault is not isolated, return to Table 2-1 and substitute the remaining control unit modules listed for the **BH** error code.
9	If the above procedure fails to isolate a defective module, turn all power off, remove all modules from the S-Box, and remove the S-Box connector panel by loosening six Phillips head screws slightly and sliding the panel from beneath the screw heads.
10	Substitute a properly functioning connector panel and replace all modules (see Figure 2-4).

2.3.3 PDP-14 Read Only Memory Checkout Procedure

The control program for the machine system is stored within the PDP-14 Control Unit in Read Only Memory (ROM) modules (see Figure 2-3). Assuming that the PDP-14 and the test computer are already interconnected and that power is ON in both machines, the ROM modules are checked by the following procedure.

NOTE

The PDP-14 Control Unit must be tested and found to be working properly, using the procedure in Paragraph 2.3.1, before testing the ROMs with this procedure.

Step	Procedure
1	Place PDP-14 START/STOP switch momentarily in STOP position.
2	Set test computer SWITCH REGISTER to 7777_8. The switch configuration for this is 111 111 111 111
3	Press the LOAD ADDRESS switch on test computer.
4	Load the VER-14 paper tape into the test computer teleprinter paper tape reader as follows: a. Set the reader START/STOP/FREE switch to the FREE position. b. Release the cover guard by means of the latch at the right and open cover. c. Insert the punched tape leader from the rear over the reader sprocket wheel so that the small holes in the tape engage the sprocket teeth and there are 3 hole spaces on the tape to the left of the sprocket wheel. d. Close reader cover.
5	Place paper tape reader START/STOP/FREE switch to START position.
6	Press test computer START switch momentarily. Tape should now move through reader until completely read and only trailing portion remains in reader.

NOTE

If tape stops before it has been completely read, place tape leader in reader and press test computer CONT switch momentarily. If tape cannot be read, refer to Chapter 4 of this manual to reload the BIN tape.

Step	Procedure
7	Remove the trailing portion of the VER-14 paper tape from the reader by releasing the cover guard with the latch and opening the reader cover. Lift the tape off the sprocket wheel.
8	Load the LOAD-14 paper tape into the test computer teleprinter paper tape reader using the procedure described in Step 4, above.
9	Place the paper tape reader START/STOP/FREE switch to START position.
10	Press the test computer START switch momentarily. The tape should now move through reader until it is completely read and only the trailing portion remains in reader.

NOTE

If the tape stops before it has been completely read, place the tape leader in reader and press the test computer CONT switch momentarily. If the tape cannot be read, refer to Chapter 4 of this manual to reload the BIN tape.

11	Remove the trailing portion of the LOAD-14 paper tape from the reader by releasing the cover guard, using the latch at the right, and opening the reader cover. Lift the tape off the sprocket wheel.
12	Load the PDP-14 program tape into the test computer teleprinter paper tape reader using the procedure described in Step 4, above. The fan-fold paper tape containing the control program is divided into sections containing the ROM program for each of the ROM modules used in a particular installation. The leader punching identifies the ROM module program contained in that segment of the tape as follows: leader for ROM #1, one row of large holes; leader for ROM #2, two rows of large holes; leader for ROM #3, three rows of large holes; and leader for ROM #4, four rows of large holes. To test a particular ROM, locate the appropriate leader in the fan-fold paper tape and insert this leader in the paper tape reader.
13	Enter 7400$_8$ in test computer SWITCH REGISTER switches. The correct switch configuration for this is 111 100 000 000
14	Press the test computer LOAD ADDRESS switch momentarily.
15	Press the test computer START switch momentarily. The PDP-14 program tape should now move through the paper tape reader until it is completely read and only the trailing portion remains in the reader.

NOTE

If the tape stops before the ROM segment has been completely read, place the tape leader in the reader again and press the test computer CONT switch momentarily.

16	Set the test computer SWITCH REGISTER to 6000$_8$. The correct switch configuration for this is 110 000 000 000
17	Momentarily press the test computer LOAD ADDRESS switch.

Step	Procedure
18	Set the test computer SWITCH REGISTER for the ROM module to be tested. This information is set into the two leftmost switches of the register as follows: ROM #1; set switches to 00. ROM #2; set switches to 01. ROM #3; set switches to 10. ROM #4; set switches to 11. Set the remainder of SWITCH REGISTER switches to 0. NOTE The SWITCH REGISTER setting must agree with the PDP-14 program tape read into the test computer in Step 12, above.
19	Momentarily press the test computer START switch.
20	Momentarily move the PDP-14 START/STOP switch to START position. The VER-14 test program will now run. If the ROM module under test is functioning properly, the teleprinter bell will ring in approximately one minute. If the program types anything, the ROM module is defective, and must be replaced by a ROM module containing the same PDP-14 program. Do not remove defective module yet.
21	Momentarily press the PDP-14 and test computer STOP switches.
22	If the ROM module just tested was not defective and if there are additional ROM modules which have not been tested, return to Step 12 and repeat this procedure from that point until a defective ROM is located or until all ROM modules have been tested.
23	If a defective ROM module is discovered, place the PDP-14 and test computer power switches OFF before removing ROM assemblies. CAUTION Insertion or removal of modules or connectors with power applied can damage PDP-14 circuits.
24	Each ROM consists of a G924 module and an assembly consisting of a G922 module and a G923 module. Substitute the G924 module first, and then repeat the VER-14 program. If the ROM under test continues to malfunction, remove the MR14A assembly, consisting of the G922 and G923 modules. Separate the two modules by placing the aluminum keeper plate of the G922 module down and removing the 15 screws which secure the G923 module to the G922 module. Lift the G923 module straight up from the G922 module. Substitute a spare G923 module, replace the 15 screws, replace the assembly in the control unit, and repeat VER-14. If VER-14 indicates an error, the new wiring should be checked for mistakes. CAUTION The ferrite transformer cores exposed during this procedure are delicate. Do not attempt to bend or otherwise apply force to them. Be particularly careful when tightening the 15 screws.

Step	Procedure
24 (Cont)	NOTE The G922 module which holds the wire braid containing the control program contains no active electronics and is therefore not subject to malfunctions.
25	If a spare ROM module is substituted for a defective module, repeat this procedure from Step 19.
26	Turn Power Switches OFF, remove test cables from PDP-14 mainframe, and reconnect all Input and Output box cables.
27	If all ROM modules are functioning properly, proceed to Paragraph 2.3.4 to check PDP-14 input and output boxes.

2.3.4 PDP-14 Output Box Fault Isolation Procedure

If the trouble has been isolated to the PDP-14 System, but the preceding test computer checkout procedures indicate that both the PDP-14 Control Unit and the control program ROM modules are functioning properly, then the malfunction must be in an input or output box.

If only a single output fails to perform properly, the trouble is probably in that output box. Each output box contains four output modules (K614) and seven associated modules (see Figure 2-5). To check the suspected output terminal, only the output module containing that terminal and its associated modules need be substituted by performing the following steps:

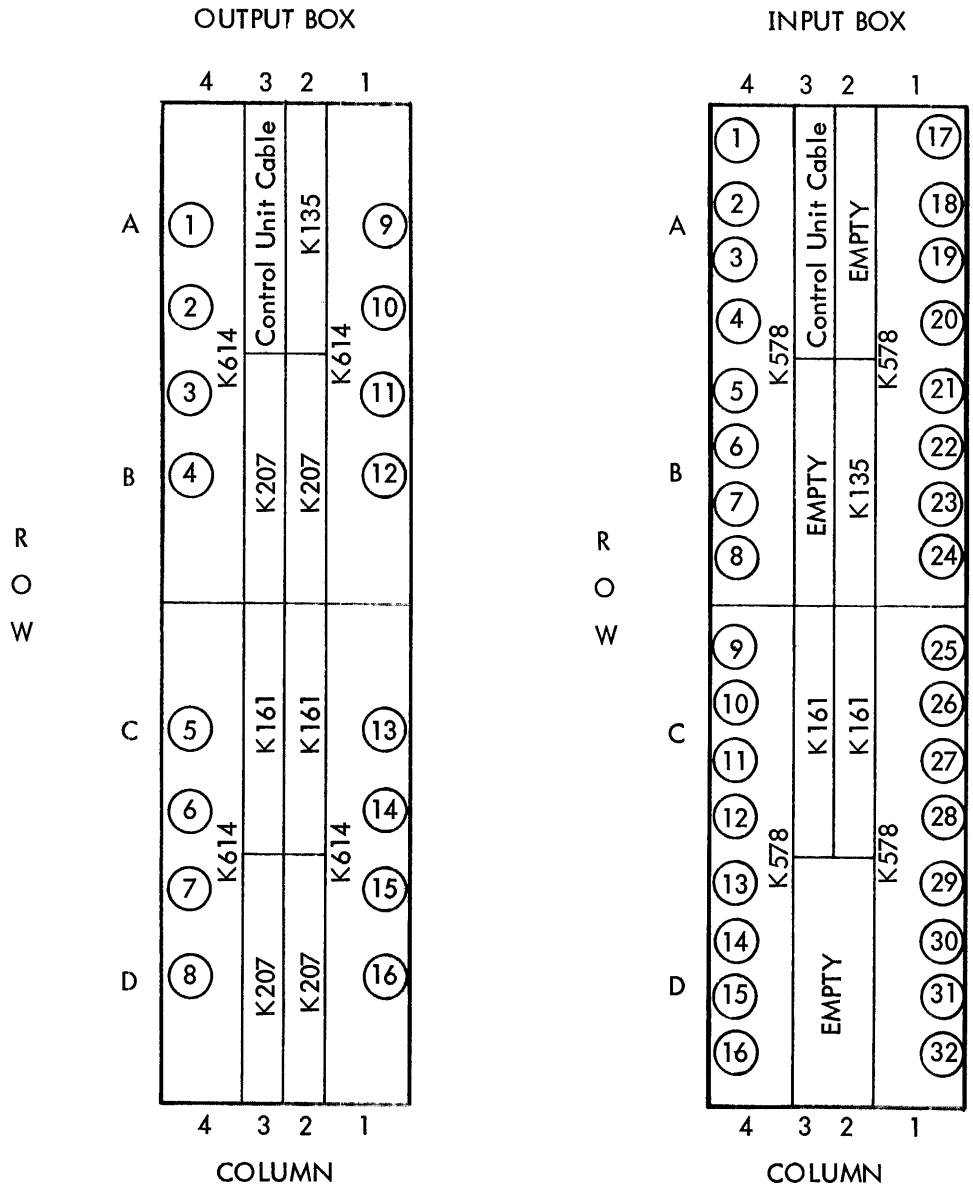
WARNING

Remove all power within the NEMA enclosure before proceeding. If the power is on, dangerous voltages are exposed during the following steps.

Step	Procedure
1	Remove the clear plastic protective cover from the output box by loosening four captive thumbscrews.
2	Remove the AC wiring from the terminals of the suspected output module (K614).
3	Remove the suspected output module by loosening the two 5/16" clamp screws holding the module to the output box shell, and substitute a properly functioning K614 module.
4	Connect the AC control wiring to the substitute output module terminals.
5	Replace the clear plastic protective cover.
6	Turn NEMA enclosure power ON.

NOTE

If the enclosure door is equipped with a power interlock, this interlock must be defeated in order to supply the output boxes and PDP-14 with power.



NOTE

Circled Numbers Represent Neon Lamps and Associated Screw Terminals for AC Control Lines.

Figure 2-5 Input and Output Boxes Module and Cable Connector Maps, Front View

Step	Procedure
7	Place the PDP-14 POWER switch in ON position and allow a few seconds for the power supply output voltage to stabilize.
8	Momentarily place the PDP-14 START/STOP switch in START position.
9	If the output box terminal now functions properly, return the defective output module to the proper facility for repair. If the terminal still malfunctions, proceed to step 10.
10	Place the PDP-14 POWER switch in OFF position, turn all NEMA enclosure power off, and refer to Table 2-3 to continue substitution of output box modules related to the malfunctioning output box terminal (see Figure 2-5 for module locations).

WARNING

Hazardous voltages are present on input and output box terminals. Always turn NEMA enclosure power OFF before removing clear plastic protective covers from boxes.

Table 2-3
Output Box Fault Isolation

Defective Output Terminal Number	Substitute Modules at These Locations One at a Time in Order Listed
1 2 3 4	AB4 (K614) C3 (K161) B3 (K207)
5 6 7 8	CD4 (K614) C3 (K161) D3 (K207)
9 10 11 12	AB1 (K614) C2 (K161) B2 (K207)
13 14 15 16	CD1 (K614) C2 (K161) D2 (K207)
(ALL)	A2 (K135)

Step	Procedure
11	If the preceding steps do not isolate a defective module, the trouble may be in an associated input box (the control unit and ROM modules having already been tested and eliminated as possible causes of the malfunction). However, the output box terminal assignment listing inside the NEMA enclosure door should be carefully examined to determine if the conditions necessary to control the malfunctioning output terminal are also used to control other output box terminals. In this way, it should be possible to eliminate most of the conditions that must be checked, using the procedure below for input box fault isolation.

Step	Procedure
12	If the above steps fail to isolate the trouble within the output box, and a check of the boxes associated with control conditions for the malfunctioning output terminal fails to isolate the trouble, the output box connector panel must be substituted by removing all AC control wiring, the cable to the PDP-14 Control Unit, and all output box modules. Then remove the six Phillips-head screws securing the connector panel to the output box frame.
13	Substitute a properly functioning connector panel by securing it to the output box frame with six Phillips-head screws, then replace all output box modules (see Figure 2-5), as well as the AC control wiring and the cable to the PDP-14 Control Unit.

2.3.5 PDP-14 Input Box Fault Isolation Procedure

If several output box circuits are malfunctioning, and these output circuits share a single input box control condition according to the output box terminal assignment listing in the NEMA enclosure door, then the defective component is probably in the input box circuits associated with the suspected input box terminal. The procedure would then be as described below.

An input box circuit should also be checked if it is a condition required by only one output, and that output is malfunctioning. If the output box circuits associated with the malfunctioning output terminal have been found to be functioning properly using the procedure in Paragraph 2.3.4, then the input box circuits associated with the suspected terminal should be checked.

WARNING

Remove all power within the NEMA enclosure, including power to PDP-14 input box AC control circuits, before processing. If power is on, dangerous voltages are exposed on the input box terminals during the following procedure.

Step	Procedure
1	Remove the clear plastic protective cover from the input box by loosening the four captive thumbscrews that pass through the cover.
2	Remove the AC wiring from the terminals of the suspected input module (K578).
3	Remove the suspected input module by loosening the two 5/16" clamp screws holding the module to the input box shell, and substitute a properly functioning K578 module.
4	Connect the AC control wiring to the substitute input module terminals.
5	Replace the clear plastic protective cover.

Step	Procedure
6	Turn NEMA enclosure and all control input power ON.

NOTE

If enclosure door is equipped with a power interlock, this interlock must be defeated in order to supply output boxes and PDP-14 with power.

7	Place the PDP-14 POWER switch in ON position.
8	Momentarily place the PDP-14 START/STOP switch in START position.
9	If the affected output box terminals now function properly, return the defective input module to the proper facility for repair. If the terminals still malfunction, proceed to Step 10.
10	Place the PDP-14 POWER switch in OFF position, turn all NEMA enclosure power off, including power to the input box control AC circuits, and refer to Table 2-4 to continue substitution of input box modules related to the suspected input box terminal. A module location map is presented in Figure 2-5 to assist in locating the modules listed in Table 2-4.

Table 2-4
Input Box Fault Isolation

Defective Input Terminal Number	Substitute Modules at These Locations One At a Time in Order Listed
1 5 2 6 3 7 4 8	AB4 (K578) C3 (K161)
9 13 10 14 11 15 12 16	CD4 (K578) C2 (K161)
17 21 18 22 19 23 20 24	AB1 (K578) C3 (K161)
25 29 26 30 27 31 28 32	CD1 (K578) C2 (K161)
(ALL)	B2 (K135)

WARNING

Hazardous voltages are present on input and output box terminals. Always turn NEMA enclosure power OFF before removing clear plastic protective covers from boxes.

Step	Procedure
11	If the preceding steps fail to isolate a defective input box module, the input box connector panel must be substituted by removing all AC control wiring, the cable to the PDP-14 control unit, and all input box modules. Then remove six Phillips-head screws securing the connector panel to the input box frame.
12	Substitute a properly functioning connector panel by securing it to the input box frame with six Phillips-head screws, then replace all input box modules (see Figure 2-5), the AC control wiring, and the cable to the PDP-14 Control Unit.
13	If the preceding steps have failed to isolate the defective component and an accessory box (A-Box) is used in the PDP-14 System, proceed to Paragraph 2.3.6.

2.3.6 PDP-14 Accessory Box Fault Isolation Procedure

Accessory boxes (A-Boxes) contain time delay and latching relay modules. Checkout using the test computer consists of the following procedure.

NOTE

The PDP-14 Control Unit must be tested and found to be working properly, using the procedure in Paragraph 2.3.1, before testing accessory boxes in this manner.

Assuming that the PDP-14 and the test computer are already interconnected and that power is ON in both machines, the A-boxes are tested as follows:

Step	Procedure
1	Place PDP-14 START/STOP switch momentarily in STOP position.
2	Set test computer SWITCH REGISTER to 7777_8. The correct switch configuration for this is 111 111 111 111
3	Press the LOAD ADDRESS switch on test computer.
4	Load the ABE-14 paper tape into the test computer teleprinter paper-tape reader as follows: a. Set the reader START/STOP/FREE switch to the FREE position. b. Release the cover guard by means of the latch at the right and open cover. c. Insert the leader (start) end of the punched tape from the rear over the reader sprocket wheel so that the small holes in the tape engage the sprocket teeth and there are three hole spaces on the tape to the left of the sprocket wheel. The leader portion of the tape has a single row of large holes and a single row of small holes. d. Close the reader cover.
5	Place paper-tape reader START/STOP/FREE switch to START position.

Step	Procedure
6	Press test computer START switch momentarily. Tape should now move through reader until completely read and only trailing portion remains in reader.

NOTE

If tape stops before it has been completely read, place tape leader in reader and press test computer CONT switch momentarily.

7	Remove the trailing portion of the ABE-14 paper tape from the reader by releasing the cover guard with the latch and opening the reader cover. Lift the tape off the sprocket wheel.
8	Enter the number 200_8 on test computer console SWITCH REGISTER. The correct switch configuration for this is 000 010 000 000
9	Press the LOAD ADDRESS switch on the test computer console.
10	Enter the following configuration in the SWITCH REGISTER switches: 000 000 000 000
11	Press the START switch on the test computer console. Program will type A-BOX IS CONNECTED TO SLOT
12	Complete this statement by typing the letter designator of the box according to the control unit O-box cable connector designator to which the accessory box is connected (see Figure 2-3). Do not type the alphanumeric (row and column) identification within the control unit. After typing the single letter, press the carriage return key.

NOTE

Only one accessory box can be tested during one ABE-14 pass. This procedure must be repeated beginning with Step 8 if additional A-boxes are used.

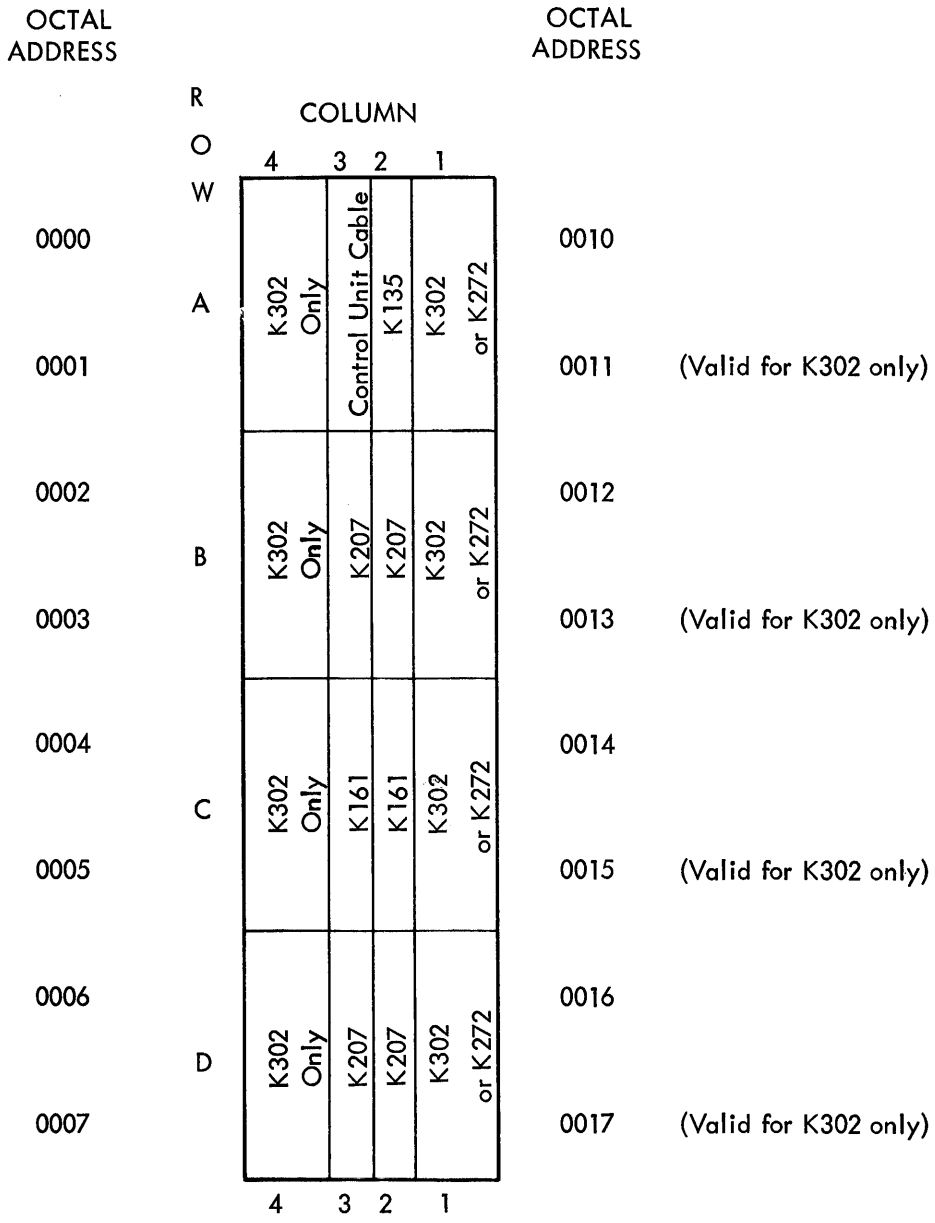
ABE-14 program will type

```
IDENTIFY THE HARDWARE ASSOCIATED WITH EACH ADDRESS BY TYPING:
T FOR TIMER, M FOR RETENTIVE MEMORY, ALL ELSE EMPTY
0000
```

NOTE

Retentive memory modules (K272) may only be inserted in accessory box locations A1, B1, C1, and D1. Each K272 module contains only one addressable latching relay. This relay can only be addressed by the even octal address shown for that A-box location position in Figure 2-6. If a K272 module is inserted in location A1, the response to the ABE-14 query 0010 should be M followed by a carriage return. The response to the ABE-14 query 011 should be only the carriage return. This note applies to K272 modules located at B1, C1, and D1 for ABE-14 queries 0012 and 0013, 0014 and 0015, and 0016 and 0017 respectively.

Step	Procedure
13	Respond to this query by typing a T if a K302 module is located at this position within the accessory box (see Figure 2-6). Accessory box modules may be observed by removing the cover. If no module is inserted in the accessory box position corresponding to 0000, type nothing.
14	Press the carriage return key. ABE-14 program will type 0001
15	Respond to this query as described for 0000 in Step 13 of this procedure. Follow this response by pressing the carriage return key as described in Step 14 of this procedure.
16	Respond to queries 0002 through 0017 as described in Steps 13 through 15 of this procedure. When query 0017 has been answered and the carriage return key pressed, the test program will be performed. If K272 modules are tested, the program will type POWER-DOWN
17	Respond to this print-out by placing the PDP-14 ON/OFF switch momentarily in OFF position, then back to ON position. The program will type POWER-DOWN up to four times, depending on the number of K272 modules inserted in the A-box. The response is always as described above in this step.
18	If the accessory box is functioning correctly, the test computer teleprinter bell will ring to indicate the end of the test program. If an error is detected, the program will type a two-letter error code corresponding to the defective module or group of modules within the accessory box. NOTE ABE-14 types the delay measured for K302 modules. This figure must be compared with system documentation to determine if the delay is correct. This delay may be adjusted using procedures described in Chapter 4. Refer to Tables 2-5 and 2-6 to substitute the appropriate Accessory Box modules.
19	If the preceding steps fail to isolate the fault, substitute a properly functioning connector panel by removing the cable to the control unit and all accessory box modules. Then remove the six Phillips-head screws securing the connector panel to the accessory box frame. Substitute a properly functioning connector panel by securing it to the accessory box frame with the six Phillips-head screws. Then replace all accessory box modules (see Figure 2-6) and the cable to the control unit.



NOTES:

1. K302 is designated T in ABE-14 test program
   K272 is designated M in ABE-14 test program
2. Any K302 or K272 module position may be left empty if not required.

Figure 2-6 Accessory Box Module and Cable Connector Map, Front View

Table 2-5
Accessory Box Module/ABE-14 Error Code Cross Reference

ABE-14 Error Code	Accessory Box Module Type (Refer to Table 2-6 for module location based on 4-digit address printed with error code)
BL **BN** **BQ** **BX** **BY** **CB**	K207, K161, K135
CF **CG**	K302
CH	K272, K302, K207, K161, K135

Table 2-6
Accessory Box Module Location/Address Cross Reference

Octal Address	K302 (T) Location	K272 (M) Location	K207 Location	K161 Location	K135 Location
0000	A4	--			
0001	A4	--			
0002	B4	--	B3		
0003	B4	--			
0004	C4	--		C3	
0005	C4	--	D3		
0006	D4	--			
0007	D4	--			
0010	A1	A1			A2
0011	A1	--			
0012	B1	B1	B2		
0013	B1	--			
0014	C1	C1		C2	
0015	C1	--			
0016	D1	D1	D2		
0017	D1	--			

2.3.7 Fault Isolation Without Test Computer

If a test computer is not available and the fault has been definitely isolated to the PDP-14 System, a few simple substitutions based on the symptoms observed may isolate and correct the fault.

a. If all output box lamps are off and PDP-14 power is on, substitute control unit modules at AB22 (M742) then at AB23 (M741).

CAUTION

Always turn PDP-14 power OFF before substituting modules to avoid possible damage to PDP-14 circuits.

b. If a single output terminal fails to turn on under any condition, substitute for the fuse associated with that terminal in the K614 module containing the terminal in question. This is accomplished by removing the K614 module from the output box and removing the fuse (located behind finned heat sinks) using right-angle needle-nose pliers. The fuses are not soldered to the circuit board.

c. If some of the control outputs (output box lamps) come on when PDP-14 power is turned on but the machine or process system fails to perform properly, substitute modules at the following locations in the PDP-14 control unit one at a time and in the order listed:

CAUTION

Always turn PDP-14 power OFF before substituting modules to avoid possible damage to PDP-14 circuits.

C18 (M746)	Memory Buffer Register
D18 (M746)	Memory Buffer Register
C23 (M746)	Instruction Register
D23 (M746)	Instruction Register
AB24 (M740)	Instruction Decoder
C19 (M747)	Program Counter #1
D19 (M747)	Program Counter #1
C21 (M746)	Program Counter #2
D21 (M746)	Program Counter #2

NOTE

Because modules are substituted one at a time, only one spare module of each type is required. These modules are: M740, M741, M742, M746, M747. Module types M743, M744, and M745 are used primarily when the PDP-14 System is connected to an external computer.

If the above suggestions do not isolate and correct the PDP-14 System malfunction, an input box or accessory box circuit may be faulty. In this case, the PDP-14 System should be taken off line for more detailed fault isolation procedures.

CHAPTER 3
THEORY OF OPERATION

3.1 GENERAL

See Paragraph 1.1 for a description of the PDP-14 System General Philosophy. Additional information of this nature is also contained in the PDP-14 User's Manual.

The control program is organized so that all the conditions required to turn a particular output on or off are listed in a set of control data words. Control logic circuitry compares each program-specified function condition with the actual state of that function, testing each function state against its specified condition until a logical decision to turn the output on or off can be made.

This process is repeated for up to 255 controllable output functions (see Figure 3-1). Then the entire program is again performed automatically. Thus, a given set of conditions for a particular output is examined repeatedly, at a rate depending on length of memory. Typical examination rates are:

1K of memory	15 milliseconds
2K of memory	30 milliseconds
3K of memory	45 milliseconds
4K of memory	60 milliseconds

Up to 256 machine system control inputs (limit switches, pushbuttons, etc) may be utilized as control conditions. In order to increase the flexibility of the PDP-14 System, three additional functions are available: time delays, retentive memories, and storage flip-flops. The delay timers and retentive memories are contained in accessory boxes; the storage flip-flops are contained in storage boxes. Full storage boxes contain 32 flip-flops; half storage boxes contain 16 flip-flops.

The storage flip-flops, timers, and retentive memories (latching relays) are all controlled in the same manner as output boxes which control the machine system directly.

In addition to 256 input conditions, the PDP-14 control logic can test the state of every output condition, every storage flip-flop condition, every latching relay condition, and the output state of all time delays.

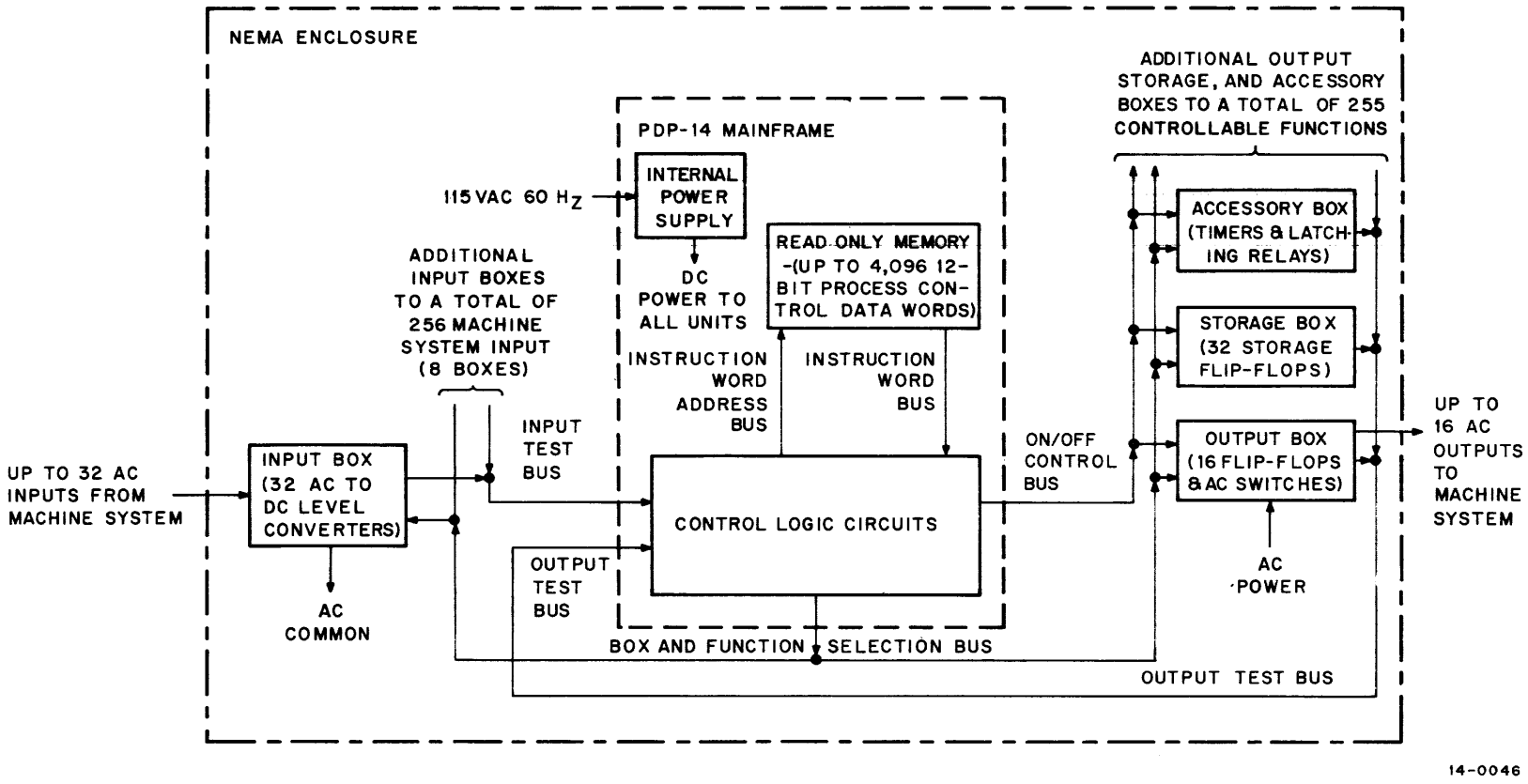


Figure 3-1 PDP-14 Controller, Simplified Block Diagram

NOTE

Storage and accessory boxes are accessed by control logic circuits as outputs. The number of outputs available for machine control is diminished as the number of accessory and storage boxes is increased.

Figure 3-1 illustrates only internal mode operation. In this mode, system operation is controlled solely by the control program stored in the PDP-14 Read Only Memory. However, the entire system may be monitored and controlled by one of several general purpose computers; or, information may be transferred between this system and another PDP-14 System controlling associated machine systems. When the control program is contained in an associated general purpose computer, the PDP-14 said to be operating in external mode.

Paragraph 3.2 provides an overall functional description of the PDP-14 system as operated in internal mode, and includes a description of the basic instruction set.

Paragraph 3.3 describes in detail nonstandard logic hardware including operation of the "test flop" (test flag), the basic functional element of the PDP-14 system, and its associated conditional jump circuits.

Paragraph 3.4 describes computer interface operations and logic circuits, including external computer instructions affecting PDP-14 System operations and PDP-14 interface circuits required for external computer control.

Throughout this chapter, reference will be made to detailed block diagrams (block schematics) and module schematic diagrams (circuit schematics) contained in Volume II of this manual. These figures will be referenced by a Roman numeral two (II) followed by a dash and the figure number in volume II (e.g., II-12).

3.2 SYSTEM FUNCTIONAL DESCRIPTION

A detailed block diagram of the PDP-14 System is presented in Figure 3-2. The paragraphs under this heading describe the major functional blocks shown and their normal functional relationships during internal mode operation. A brief description of the hardware required for computer interface operation is provided, but detailed information on external mode operation is presented in Paragraph 3.4.

3.2.1 Internal Mode Instruction Set

There are two major classes of instruction words in the PDP-14 instruction set (Table 3-1). Class instructions are used to access a specific input, output, storage, or accessory box terminal either to test the current state of that terminal or function, or, in the case of output, storage, and accessory boxes, to set or clear the selected function or terminal. Basic instruction word formats are presented in Figure 3-3.

Class II instructions control the internal operations of control logic circuits. This class of instructions includes those that perform program jumps. A jump instruction transfers control to a different part of memory.

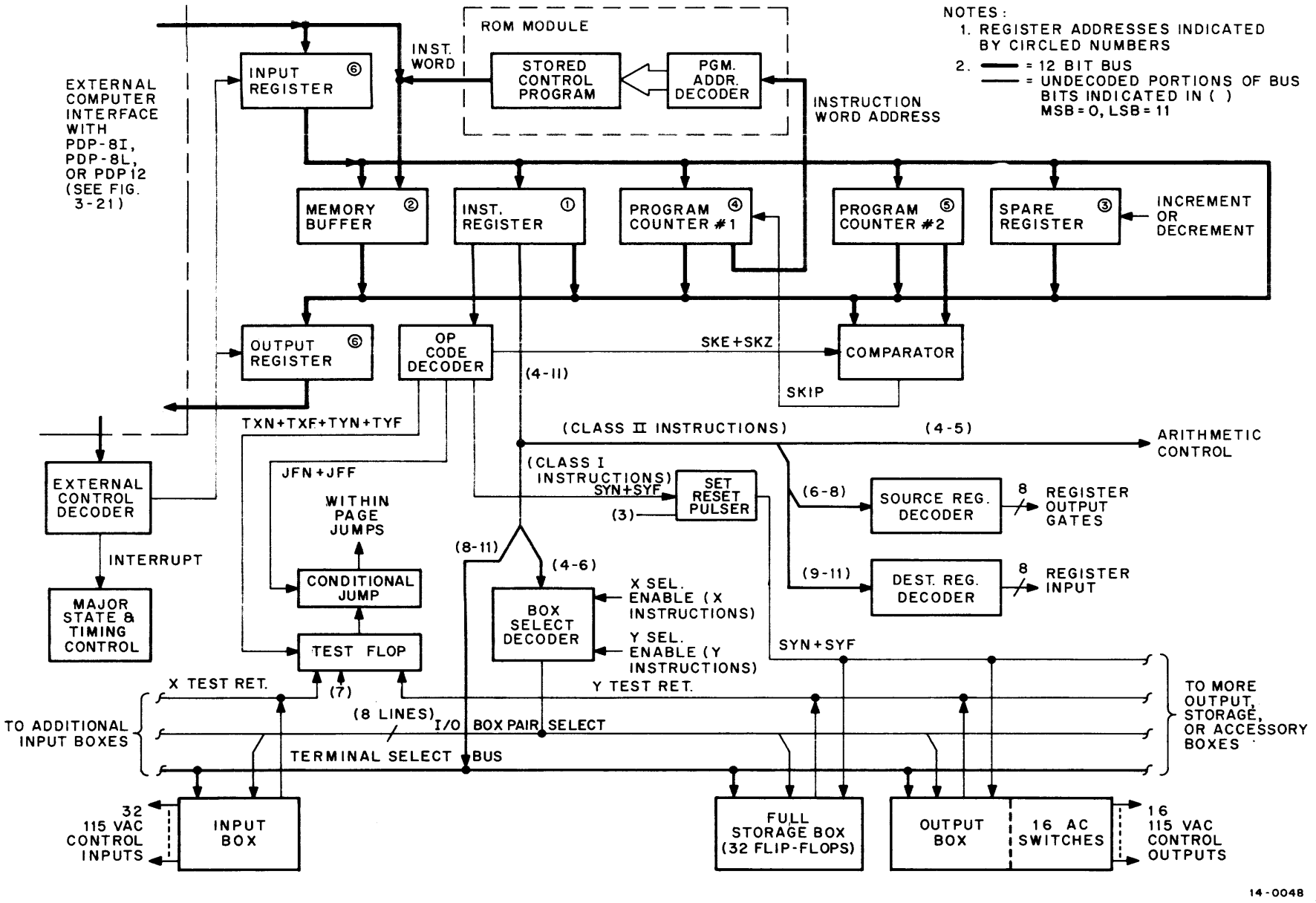


Figure 3-2 PDP-14 Controller, Detailed Block Diagram

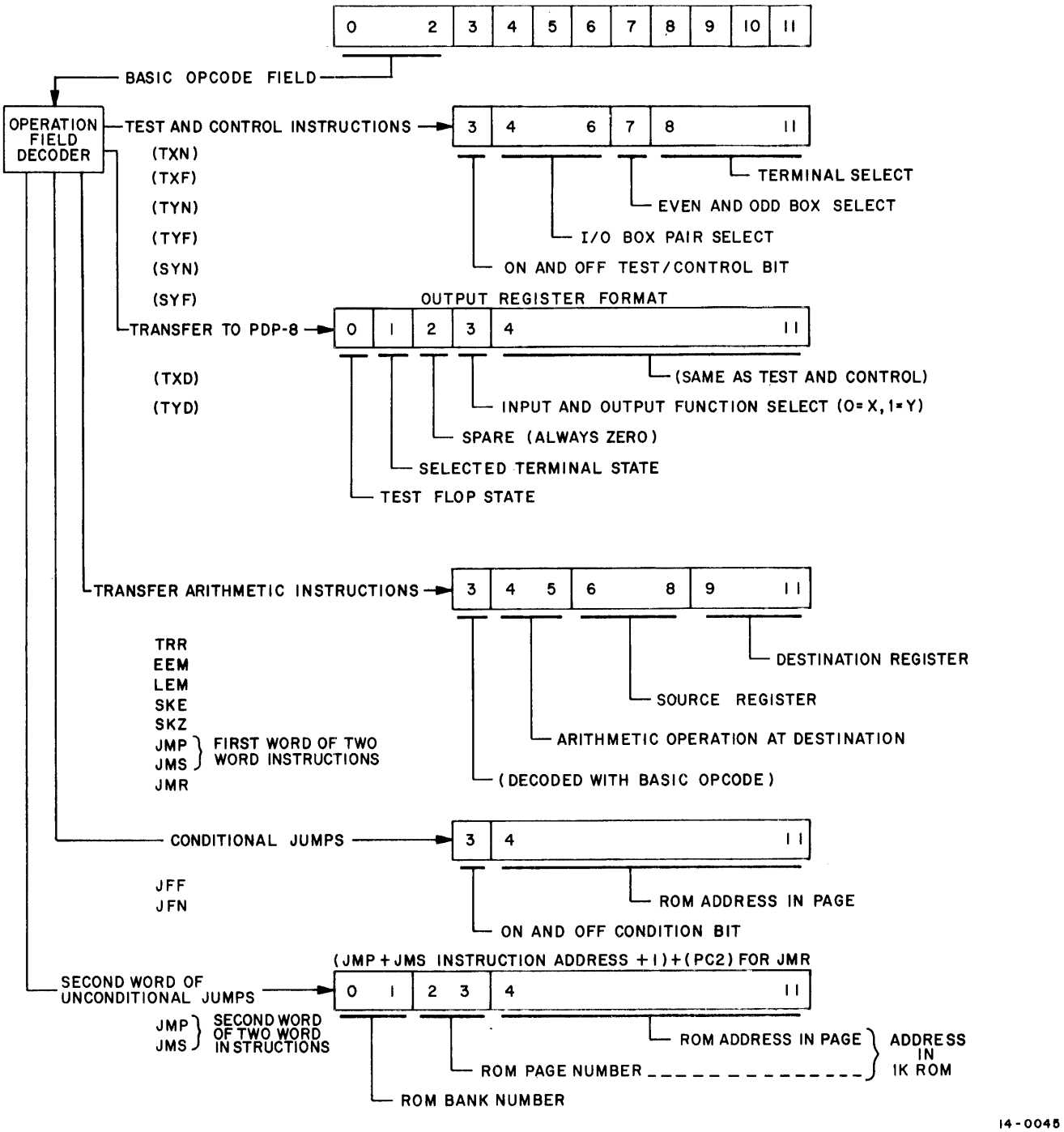


Figure 3-3 Instruction Word Formats

Table 3-1
PDP-14 Internal Mode Instruction Set

Assembly Language Mnemonic	Op Code Field MSB (Bit 0) ↓	Definition
TXN	010 1	Set test flop if specified input is ON.
TXF	010 0	Set test flop if specified input is OFF.
TYN	001 1	Set test flop if specified output terminal, storage flip-flop, latching relay, or timing circuit output is ON.
TYF	001 0	Set test flop if specified output terminal, storage flip-flop, latching relay, or timing circuit output is OFF.
SYN	011 1	Set ON specified output terminal, storage flip-flop, latching relay, or start delay timer.
SYF	011 0	Set OFF specified output terminal, storage flip-flop, latching relay, or clear delay timer.
CLR	011 011 111 111 (3377_8)	Sets OFF all output terminals, storage flip-flops, and clears delay timers when address $377_8(256_{10})$ is specified. For this reason, only 255_{10} controllable output functions are available.
JFN	110 1	If test flop is set (ON), jump to relative address specified by bits 4-11 of JFN instruction word and reset test flop. If test flop is reset (OFF), jump is not performed, and next sequential instruction is executed.
JFF	110 0	If test flop is reset (OFF), jump to relative address specified by bits 4-11 of JFF instruction word. If test flop is set, jump is not performed but test flop is reset, and next sequential instruction is executed.
JMP	100 010 010 100 (4224_8 +$NNNN_8$)	Unconditional jump to instruction word located at the address ($NNNN_8$) specified in the next sequential memory address (two-word instruction).
JMS	100 110 100 101 (4645_8)	Unconditional jump to subroutine instruction word located at the address specified in the next sequential memory address (two-word instruction). Return address to resume primary routine is stored, minus 1, in PC2 for use by JMR instruction at end of subroutine.
JMR	000 011 101 100 (0354_8)	Unconditional return jump from subroutine to primary routine address stored by JMS instruction in PC2, plus one. Used at completion of all subroutines.
TXD	111 0	Provides state of selected input terminal and current state of test flop to external monitoring computer.
TYD	111 1	Provides state of selected output terminal and current state of test flop to external monitoring computer.
TRM	100 010 010 110 (4226_8 + $NNNN_8$)	TRM is a two-word instruction which transfers the next sequential ROM word to the PDP-14 Output Register for use by a monitoring external computer. No restrictions are placed on the contents of the transferred word.

Table 3-1 (Cont)
PDP-14 Internal Mode Instruction Set

Assembly Language Mnemonic	Op Code Field MSB (Bit 0) ↓	Definition
SKP	000 011 100 100 (0344_8)	Skip the next sequential ROM instruction. The instruction following the skipped instruction is executed (the second sequential instruction following the SKP instruction).
SKE	110 111 XXX 100 ($67X4_8$)	Causes PC1 to skip the next sequential ROM memory address if the PDP-14 register specified by the X-field is equal to the contents of PC2.
SKZ	110 011 XXX 100 ($63X4_8$)	Causes PC1 to skip the next sequential ROM memory address if the PDP-14 register specified by the X-field is equal to zero.

There are two types of program jumps employed in the PDP-14 system. Unconditional jumps (JMS, JMP, JMR) are made whenever the Jump instruction is encountered in the control program. Basic to the operation of the PDP-14, however, are two conditional jump instructions. In a conditional jump (JFF, JFN), the jump to a specified control program address is performed if and only if some condition is satisfied. In the PDP-14, the two conditional jump instructions are performed if and only if the state of the test flop agrees with the condition specified for the test flop in the conditional jump instruction.

Also included in Class II are those instructions which transfer data between pairs of registers within the PDP-14. Each register and counter is identified in Figure 3-2 by a circled number corresponding to the octal number decoded to access that register or counter. If the counter specified in the instruction is capable of basic arithmetic operations (incrementing, decrementing), the arithmetic operation is also defined in the instruction.

The basic instruction Op Code (operation code) is contained in the most significant four bits (bits 0-3) of all words except the second word of two-word instructions where these bits specify the ROM "page" in which the instruction word specified by the remaining bits is located. The op code decoder sets up the controls required to execute the instruction specified in bits 0-3 of the instruction word.

With the exception of the two-word instructions, the remaining bits of the instruction word form the effective address; that is, the address of the input or output, or internal registers affected by the instructions. Bits 4-11 are decoded in Class I instructions to select an input or output (X or Y) function, bits 4-7 being decoded by the box select decoder to select half the inputs of a particular input box and all the outputs of an output box. Bits 8-11 are bused to all input storage and accessory output boxes, but only the box enabled by the box select decoder is permitted to complete the selection process by decoding bits 8-11. Bits 4-11 always select both an input and an output function. The final selection process is determined by the basic Class I Op Code. If the

instruction code mnemonic contains an X, only the selected input is accessed. If the code contains a Y, only the selected output or function is accessed for monitoring or control.

Class II instructions employ the same four-bit Op Code (bits 0-3). The remaining bits of the instruction word define which register or counter is to be the source of the data transfer, and which register or counter is to be the destination, as well as what arithmetic operation is to be performed on the data by the destination register.

NOTE

The terms "register" and "counter" are not used in the strict sense of the terms. PC2 is not a counter, it is a gated flip-flop register. The Spare Register is capable of basic arithmetic operations with bits 6-11 (incrementing, decrementing).

Instruction word bits 6-8 define the source register, and bits 9-11 define the destination register. The octal code designations of the various registers are indicated by a circled number within each register or counter of Figure 3-2. There is no register or counter corresponding to 0_8 (000_2). This empty register designator is called the "dummy" register. Table 3-2 summarizes the registers and counters within the PDP-14, their capabilities, and major uses.

Table 3-2
PDP-14 Register and Counters

Name	Source/ Destination Code	Major Use	Capabilities
Dummy (No Register)	000 (source only)	No operation	As source, provides all ones to destination
Instruction Register	001	Stores instruction word for execution	Flip-flop register storage only
Memory Buffer	010	Stores word read from ROM	Flip-flop register storage only
Spare Register	011	Utility counter, return address storage for nested subroutines	Increment, decrement, transfer
Program Counter #1	100	Stores address of next ROM instruction	Increment, decrement, transfer
Program Counter #2	101	Stores return address during subroutines	Flip-flop register storage only
Input Register	110 (source only)	Flip-flop buffer from data transfer from external computer to PDP-14	Only as stated under major use
Output Register	110 (destination only)	Flip-flop buffer for data transfer to external computer from PDP-14	Only as stated under major use
(No Register)	111 (destination)	Halt	Only as stated under major use

If the destination counter or register is capable of performing the operation listed, bits 4 and 5 of Class II instructions specify the arithmetic operation as follows:

Bits 4	5	Arithmetic Operation
0	0	Transfer
0	1	Transfer, decrement by one
1	0	Transfer
1	1	Transfer, increment by one

3.2.2 Cycle Control and Data Transfer

In addition to the registers and counters described in the preceding paragraph, a method of transfer between selected source and destination registers and counters is required. This is accomplished by a single 12-bit data transfer bus. When a particular register or counter is selected as the source of a data transfer, output gates from that register to the data transfer bus are enabled. The selected destination register or counter is also enabled. The destination register is either (1) force loaded as a simple flip-flop register, or (2) is used to combine the data held in the source register with the contents already in the destination counter as described above in Paragraph 3.2.1.

Registers and counters not selected as the destination in a Class II instruction are unaffected by the data present on the data transfer bus. If source register code 000_2 is selected, the data bus is left floating; that is, every bit (wire) of the bus will be at a logic one potential. The selected destination register will therefore be loaded with all ones (if an increment is also performed, the register is cleared).

In Figure 3-2, all possible sources for a particular register or counter are shown entering the register box from the top. Only one source is active at a particular time. Likewise, all possible destinations are shown leaving the register box from the bottom, but only one destination is active (the transfer bus being considered as one destination for the source register).

To complete a functional description of the PDP-14, it is necessary to mention the major states in which the instruction words are obtained and performed. During the Fetch state, an instruction word is obtained from the ROM (or from an external computer). During the Execute state, the instruction word obtained during the Fetch state is decoded and executed. The PDP-14 contains only these two major states.

Within each major state, additional timing pulses and time delays are required to properly synchronize the transfer of data and permit data to stabilize from the ROM and external computer lines.

The two major states and cycle timing are discussed in detail in Paragraphs 3.3.2 and 3.3.3.

3.2.3 External Computer Interface and Skip Comparator

In order for an external computer to be interfaced with the PDP-14, a special external control decoder is provided. This decoder is under control of the external computer; upon decoding an interrupt signal from the external computer, the decoder will stop the PDP-14 internal timing at the appropriate point in the PDP-14 cycle and synchronize the PDP-14 with the external computer. A signal ("flag") is also produced by the PDP-14 whenever the output register is loaded with data for an external computer.

Data transfer between the PDP-14 system and an external computer is accomplished via the input and output registers. In addition, PDP-14 instructions from the external computer during an interrupt or during external mode operation are loaded directly into the memory buffer register (via the memory port). The ROM memory modules are disabled during interrupts and when PDP-14 instructions are received from an external computer.

The skip comparator is employed primarily as a diagnostic tool. It is used to test the contents of a specified source register against the contents of PC2 when an SKE (skip if equal) instruction is executed, or to test the contents of a specified source register for all bits equal to zero when an SKZ (skip if zero) instruction is executed. If the specified skip condition is satisfied, the instruction immediately following the skip instruction is skipped and the second sequential instruction is fetched and executed.

3.3 DETAILED CIRCUIT DESCRIPTIONS

The circuit schematics presented in Volume II of this manual consist of standard electronic and MIL-STD-806 logic symbols. An important exception, however, is a special symbol used for gated flip-flops. This symbol and its equivalent logic circuit is shown in Figure 3-4. When the clock level is high, the state of the flip-flop cannot be changed from the data input or output terminals.

3.3.1 Test Flop and Conditional Jumps

The input, output, storage, or accessory condition to be tested is selected by the address field of Class I instructions (see Figure 3-3). The return from test condition is compared with the state of bit 3 of a TXN, TXF, TYN, or TYF instruction in the test comparator (Figures II-2 and 3-5).

If the selected condition is the same state as the state of bit 3 of the test instruction word, the "test true" output of the test comparator sets the test flop at the end of the execute major state. A loop from the set output of the test flop to the OR gate data input to the test flop ensures that no subsequent test will have any affect upon the test flop once it is set.

The Jump comparator (see Figure 3-5) is enabled for JFN or JFF instructions. The jump comparator tests the state of the test flop against the requirements of the conditional instruction to enable setting the "JF OK" flip-flop.

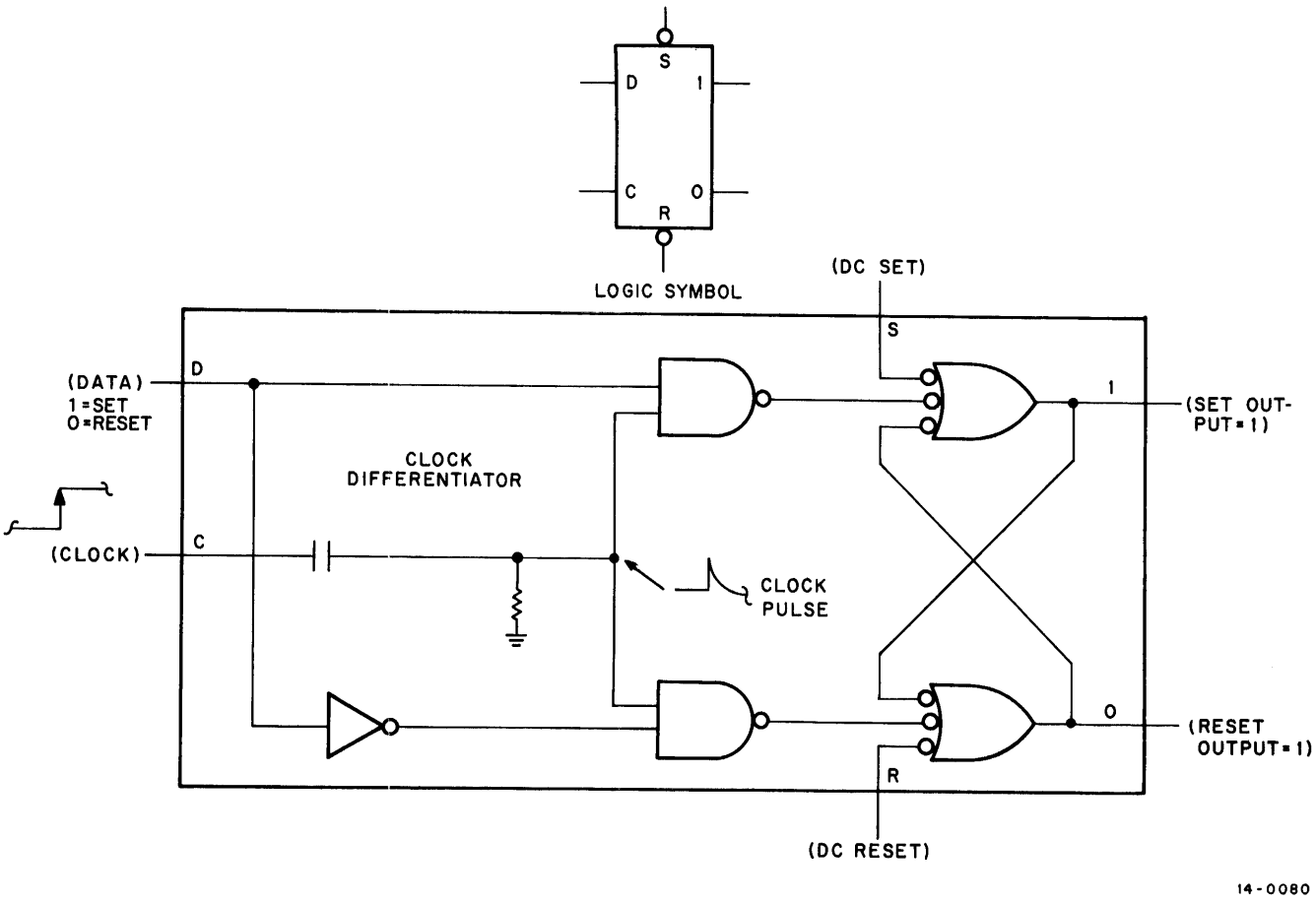


Figure 3-4 Gated Flip-Flop and Equivalent Logic Circuit

The conditional jump instructions also employ bit 3 of the instruction as the test condition. A JFN instruction has bit 3 of the instruction word set. Therefore, the jump comparator will set the JF OK flip-flop only if the test flop is set. A JFF instruction includes bit 3 in the reset state; therefore, the test flop must be in the reset state for the JF OK flip-flop to be set.

The test flop is reset by a JFF or JFN instruction, regardless of whether or not the conditions required for the conditional jump are met. In fact, the JFF and JFN instructions are the only instructions which will reset the test flop, and they will always reset it. If the jump comparator enables setting the JF OK flip-flop, the ROM memory page address specified in bits 4-11 of the JFN or JFF instruction is enabled; a transfer of this address is then made to PC1.

NOTE

Because the final output from the jump comparator to the JF OK flip-flop is inverted, the set output of the JF OK flip-flop is the "0" output of the flip-flop symbol.

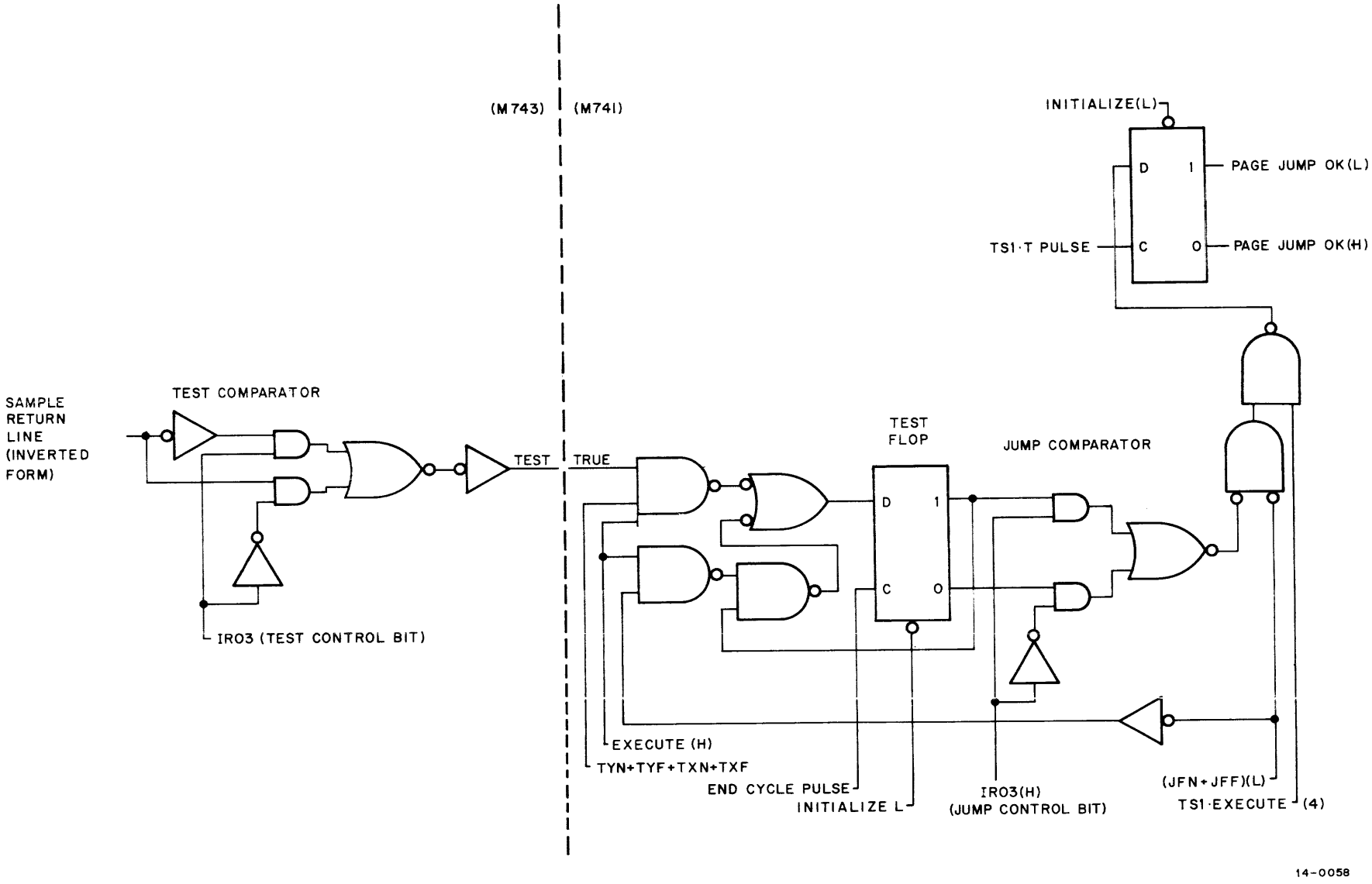


Figure 3-5 Test Flop and Associated Circuits, Simplified Logic Diagram

The jump is called a page jump because only a partial ROM address can be held in bits 4-11 of the conditional jump instruction word. An unrestricted jump to any address within the ROM requires all instruction word bits (Bits 0-11). Address bits 0-3 are therefore called the "page" selection field and bits 4-11 specify the location within a page containing the instruction word. The unconditional jumps (JMP, JMS, and JMR) provide the entire address field so that page restrictions do not apply.

The conditional jumps will always be made to an address within the page specified by bits 0-3 of PC1 at the time the jump is performed. Data input to the JF OK flip-flop is enabled by the timing pulse, but data is available only during time state 1 of an execute cycle. Thus, the JF OK flip-flop can only be set during time state 1 of an execute cycle if the conditional jump condition is satisfied.

If the JF OK flip-flop is set during time state 1, bits 4-11 of the instruction register are gated to PC1 bits 4-11 during time state 2. The address contained in the conditional jump instruction will now be read, and the instruction at that address supplied to the instruction register for execution. This address is in the control program "page" specified by the original contents of bits 0-3 of PC1.

If the JF OK flip-flop is not set during a conditional jump instruction execution, the test flop is cleared and the next sequential instruction (PC)+1 is read and executed. The conditional jump is not performed if the JF OK flip-flop is not set.

3.3.2 Major States

Figure 3-6 illustrates the two major states, fetch and execute, of the PDP-14 control unit. These two states are indicated at the top of the flow chart. The timing states are indicated down the left side of the chart. The fetch state is invariable and is always used to obtain a new instruction word from ROM (or an external computer) to be executed during the following execute major state. Major state and timing cycle relationships are shown in Figure 3-7. These circuits are shown in block diagram form in Figure II-2.

3.3.2.1 Fetch - The fetch major state during internal mode operation is invariable, it always places an instruction word into the instruction register and increments PC1 in preparation to read the next sequential word from ROM (whether this word will in fact be read depends on what happens during the following execute major state).

However, during the pause cycle at the beginning of the fetch major state, an interrupt flag set by an external computer will be honored by the PDP-14. When this flag is honored, the memory buffer is loaded from the input data bus instead of from the ROM. During time state 1, the contents of the memory buffer are transferred to the instruction register. This is the only method an external computer has to interrupt the PDP-14 system. Unless the instruction gated into the memory buffer during an interrupt is an EEM (enter external mode) instruction,

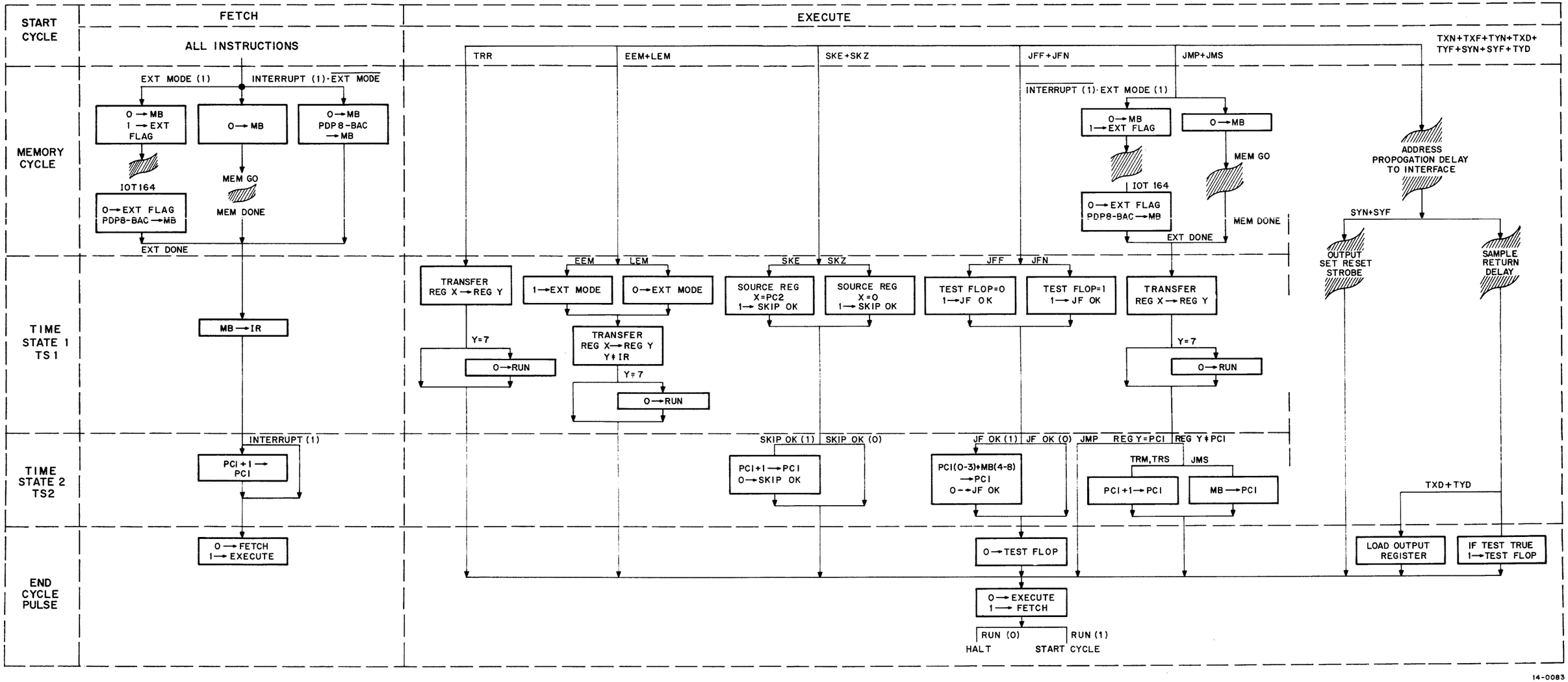


Figure 3-6 PDP-14 Controller, Flow Diagram

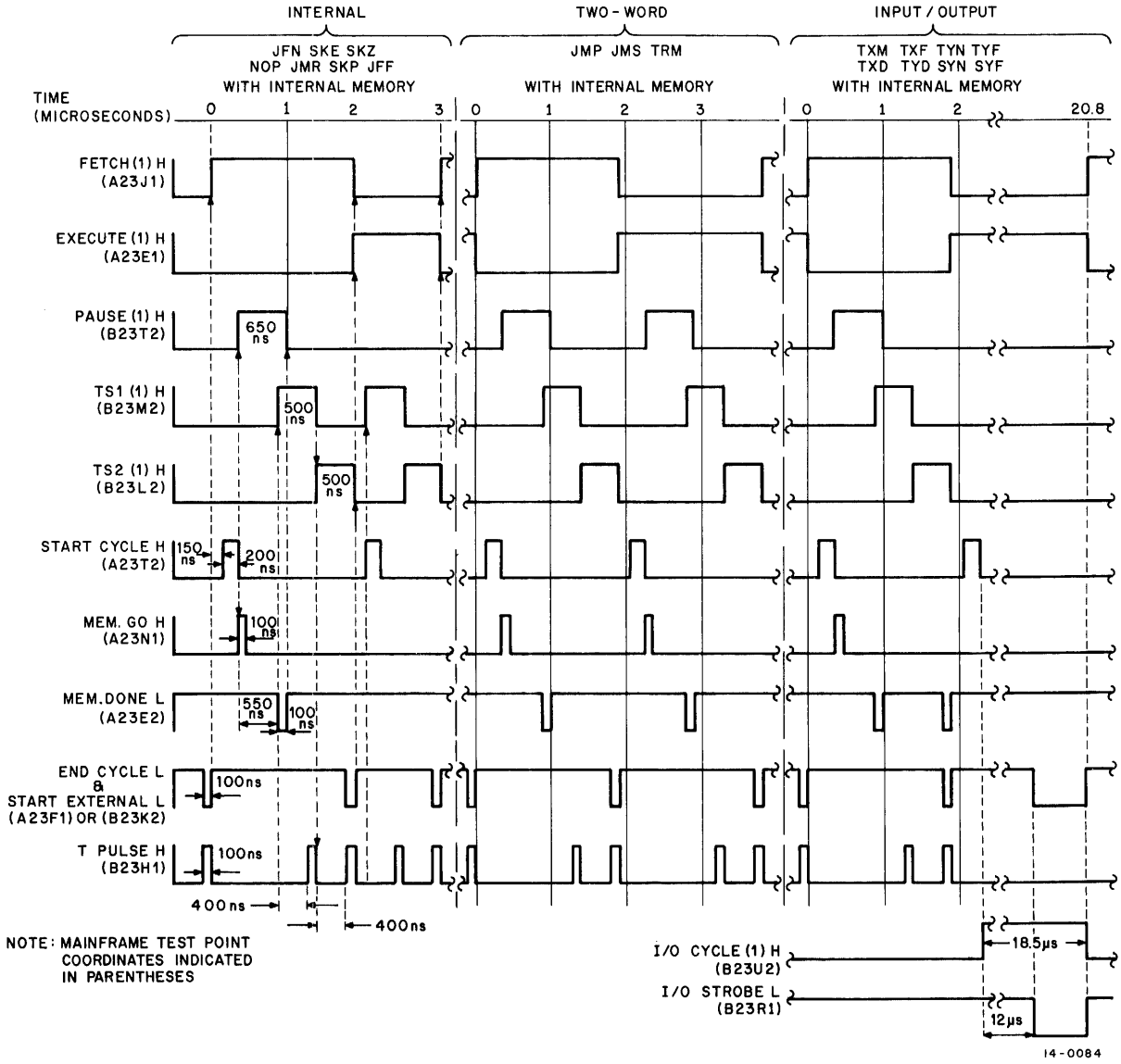


Figure 3-7 Control Logic Timing Diagram

the interrupt will result in only a "cycle steal" operation; that is, the instruction specified by the external computer will be performed but control will then revert to the PDP-14 ROM program, picking up at the instruction following the last ROM program instruction executed.

If, during an interrupt, the external computer places an EEM instruction on the input data bus, the external mode flag is set and all subsequent instructions must come over the input data bus until the external computer initiates a LEM (leave external mode) instruction. To execute this instruction, the PDP-14 resets the external mode flag and resumes the ROM program at the address currently stored in PC1. Unless specifically programmed into the external program, this address will not be the next sequential ROM instruction following the last ROM instruction executed.

The fetch/execute control flip-flop is set to the fetch state when the PDP-14 is initialized in order to obtain the first instruction word from the ROM or external computer (see Figure 3-8).

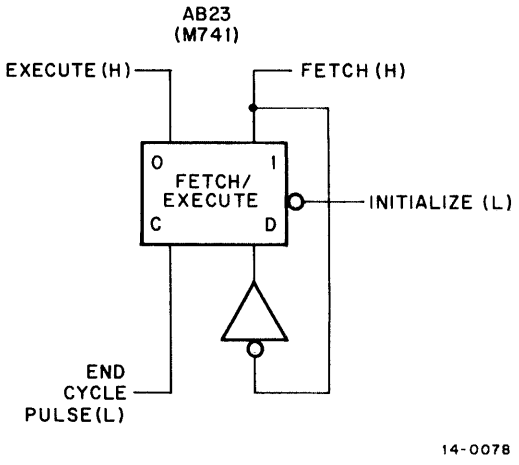


Figure 3-8 Fetch/Execute Major States Toggle

3.3.2.2 Execute - The fetch/execute control flip-flop is toggled to the execute state by the fetch major state end cycle pulse (see Figure 3-8). Three types of execute cycles exist, as shown in Figure 3-7.

If an internal instruction is decoded during the fetch cycle, no pause cycle (involving ROM or external computer) is required. If a two-word type instruction (JMP, JMS, TRM) is decoded, a pause cycle is required during the execute major state. This pause cycle is in addition to the two time states required for an internal instruction execution. Execution of instructions involving input or output functions (input boxes, output boxes, storage boxes, or accessory boxes) do not require either a pause cycle or the two time state cycles.

3.3.3 Timing Cycle

As described in Paragraph 3.3.2, the timing cycle for the fetch major state is fixed while the timing cycle for Execute may be one of three sequences (see Figure 3-7). The discussions under this heading describe the start, pause, input/output, time states, and end pulse timing. These circuits are shown in block diagram form in Figure II-2.

3.3.3.1 Start Cycle - A start cycle pulse is initiated by an end pulse or by an external start pulse (see Figure 3-9). The start pulse generator produces a negative-going pulse to the base of the start cycle delay transistor. The negative-going pulse on the base of this NPN transistor turns the transistor off, permitting the charge of the anode of the start cycle delay capacitor to rise. When this charge reaches the threshold of the input gate of the start pulse generator, the start pulse is initiated.

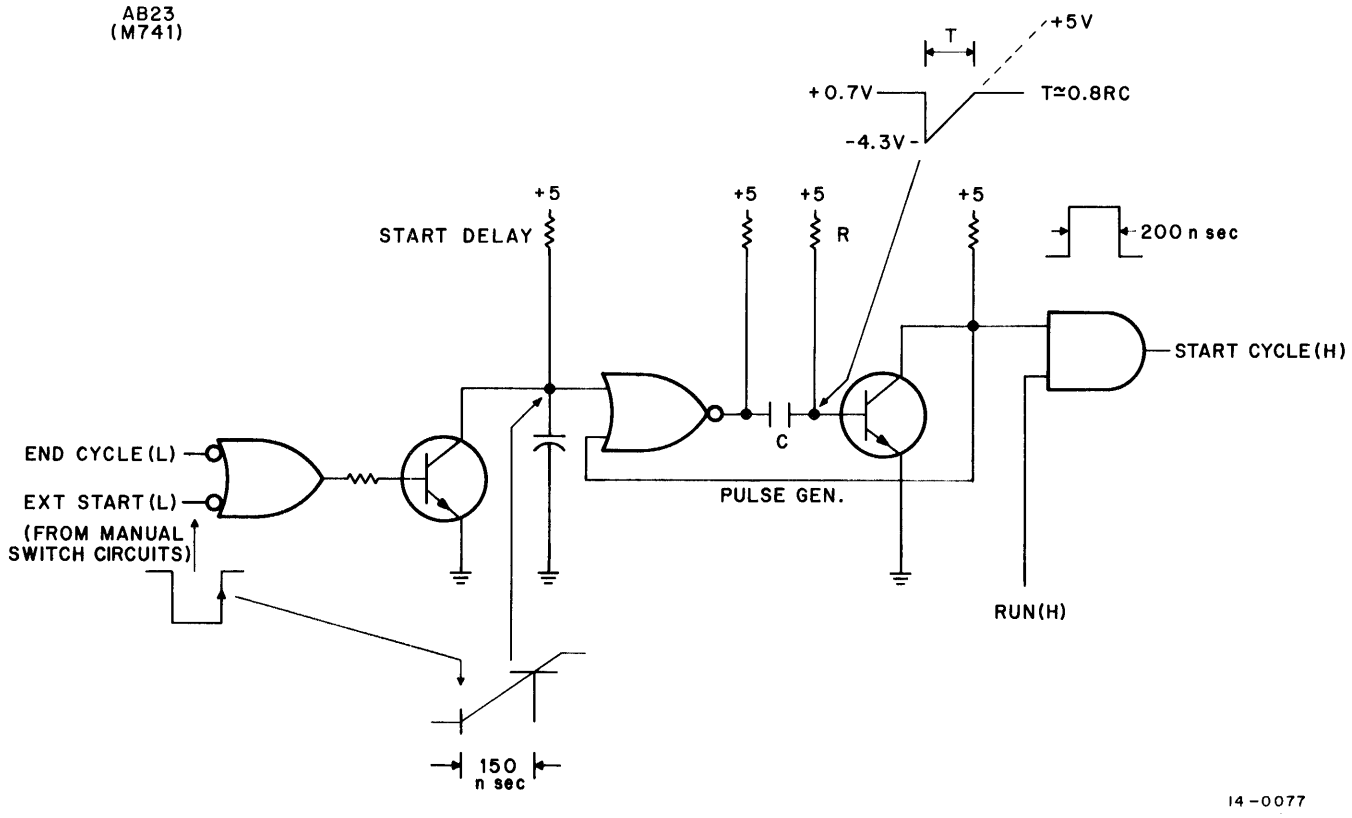


Figure 3-9 Start Cycle Control, Simplified Logic Diagram

The start cycle pulse is terminated by a loop from the output of the start pulse generator to its input. When the charge on the start pulse generator capacitor is bled through the resistor to ground, the output of the start pulse generator inverter goes high, turning on the transistor which in turn terminates the start cycle pulse. As long as the RUN flip-flop is set, the start cycle pulse generator output gate is enabled.

3.3.3.2 Pause Cycle (Memory and External Control) - The Pause control flip-flop (Figure 3-10) is set if a JMP or JMS instruction is decoded during an execute major state or if the fetch major state flip-flop is set. The pause flip-flop clock is triggered by the positive edge of the start cycle pulse or by the memory done or external done pulses.

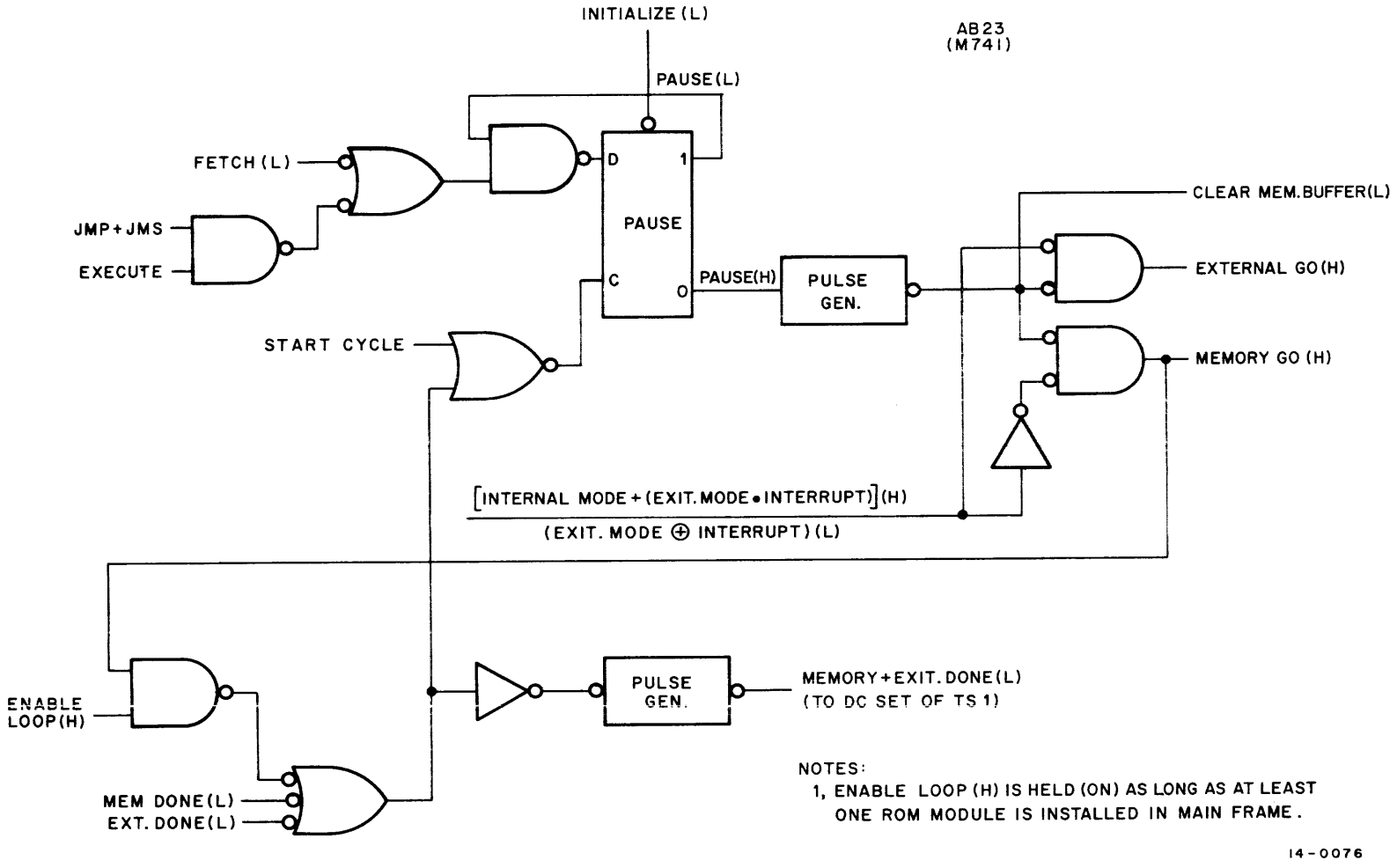


Figure 3-10 Pause Cycle Control, Simplified Logic Diagram

A loop from the pause (L) output of the Pause flip-flop to the data input gate disables that gate so that when the memory done or external done pulse occurs the flip-flop will be reset. Setting the Pause flip-flop triggers a pulse generator, the output of which clears the memory buffer and initiates a ROM read cycle, if in internal mode, or requests a new instruction from an external computer if in external mode or if an external interrupt occurs. Note that if an interrupt instruction (TRM) occurs while the PDP-14 is in external mode, the pause circuit will initiate a ROM read cycle during the execute major state. This feature is useful in checking the ROM program from an external computer. A loop from the memory go (H) gate output to the enable loop gate prevents the PDP-14 timing from "hanging" in the pause cycle if there are no ROM modules installed in the mainframe.

NOTE

Timing cycle will hang if ROM modules are installed in other than sequential locations, beginning at ROM 1.

This situation may occur during maintenance when the PDP-14 is being operated from an external computer. This loop ensures that the PDP-14 is running (no operation instruction cycles) and can therefore be controlled from an external computer. An external computer cannot interrupt the PDP-14 if the PDP-14 is not running, thus no external instructions can be performed if the PDP-14 is hung.

The output of the enable loop gate is combined in an OR gate with the memory done and external done lines. The output of this OR gate supplies the clock pulse to reset the pause flip-flop and sets time state 1 (TS1) flip-flop to continue the major state cycle.

3.3.3.3 Input/Output (I, O, S, and A Boxes) - The I/O cycle flip-flop is clocked by the leading edge of the start cycle pulse (see Figure 3-11). The data input is controlled by a NAND gate, which is satisfied if an Input/Output type instruction (TXN+TXF+TXD+TYD+TYN+TYF+SYN+SYF) is decoded during the execute major state. An address decode delay circuit is employed to permit the address selection process to be completed before the strobe I/O pulse is initiated. This delay must compensate for propagation to and decoding of the low order address bits within the selected box.

A subsequent data return delay circuit compensates for the data returned from the selected box address before producing the I/O done pulse. The I/O done pulse or initialization resets the I/O cycle flip-flop. The I/O done pulse also initiates the end cycle control circuit (the two time states are not required during I/O instruction execution).

The strobe pulse is used with SYN or SYF instructions to gate set or reset data onto the control buses to the selected output, storage, or accessory box function addressed. The I/O done pulse delays the end cycle pulse sufficiently to allow data to stabilize on data return bus before the end cycle pulse clocks test results on that data into the test flop. The delayed end cycle pulse also clocks the loading of the output register during TXD and TYD instructions.

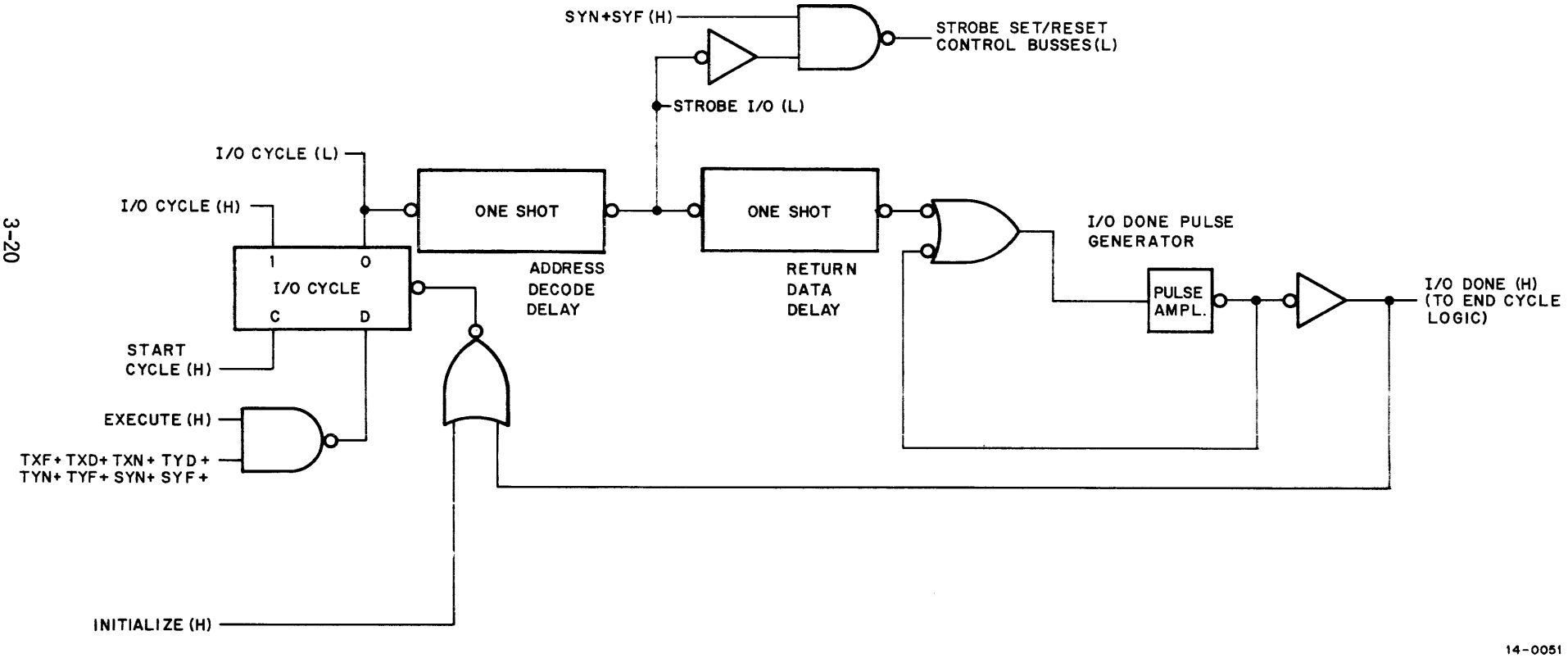


Figure 3-11 I/O Cycle Control, Simplified Logic Diagram

3.3.3.4 Time States, Timing Pulse, and End Cycle Circuits - The two time state flip-flops, TS1 and TS2, control data transfer within the mainframe (see Figure 3-12). Both flip-flops are reset during initialization.

During the fetch major state, the TS1 flip-flop is set (DC set input) by the memory done pulse from the ROM module, or by an external done pulse from an external computer if an interrupt or external mode instruction occurred during the initial pause cycle of the fetch state.

During the execute major state, the TS1 flip-flop is set (data input) if TS2 is reset and so long as the decoded instruction is not an input/output or two-word instruction. The clock is provided for this condition by the trailing edge of the start cycle pulse.

Upon being set, TS1 initiates a timing pulse delay. The timing pulse generator is triggered at the end of this delay. The timing pulse clocks both time state flip-flops. The data input to the TS2 control flip-flop is the set output of the TS1 flip-flop. Therefore the TS2 flip-flop is set when the timing pulse occurs.

Time state two has its own timing pulse delay circuit. Two delay circuits are required because one could not recover rapidly enough following the reset of time state one to be of any use as a time state two delay (time state two follows time state one at the same clock time). At the end of the TS2 flip-flop is reset because TS1 was previously reset. The existence of the timing pulse while TS2 is set also produces the end cycle pulse (the time state flip-flops are clocked on the trailing edge of the timing pulse, the end cycle pulse begins on the leading edge). As the time states are not used for input/output instructions, the end pulse is also produced by the I/O done pulse.

The end cycle pulse clocks execute and fetch major state control flip-flops, test flop operations, and output register loading for TXD and TYD instructions.

3.3.4 Manual Control and Power Detection Circuits

Initialization is accomplished automatically by its power detection circuits, or by the STOP/START switch. When PDP-14 internal power is first switched on, the collector output of the power up sense circuit is held low because of the on bias maintained on its base through a capacitor, the other side of which is connected to the +5 volt power bus (Figure II-1 and 3-13). The output of the transistor is connected to the start (L) bus. When this bus is low, the capacitor in the input circuit to the Schmitt trigger is shorted and the initialize line is active to ensure that all control flip-flops are reset, all output, storage and accessory flip-flops are reset, and that the memory buffer and instruction registers are cleared. The run flip-flop is also reset by the initialize line.

When the +5 volt bus voltage ceases to rise, the charge on the capacitor bleeds down rapidly, permitting the power up sense transistor to turn off. The start (L) line level goes high as a result of the transistor being turned

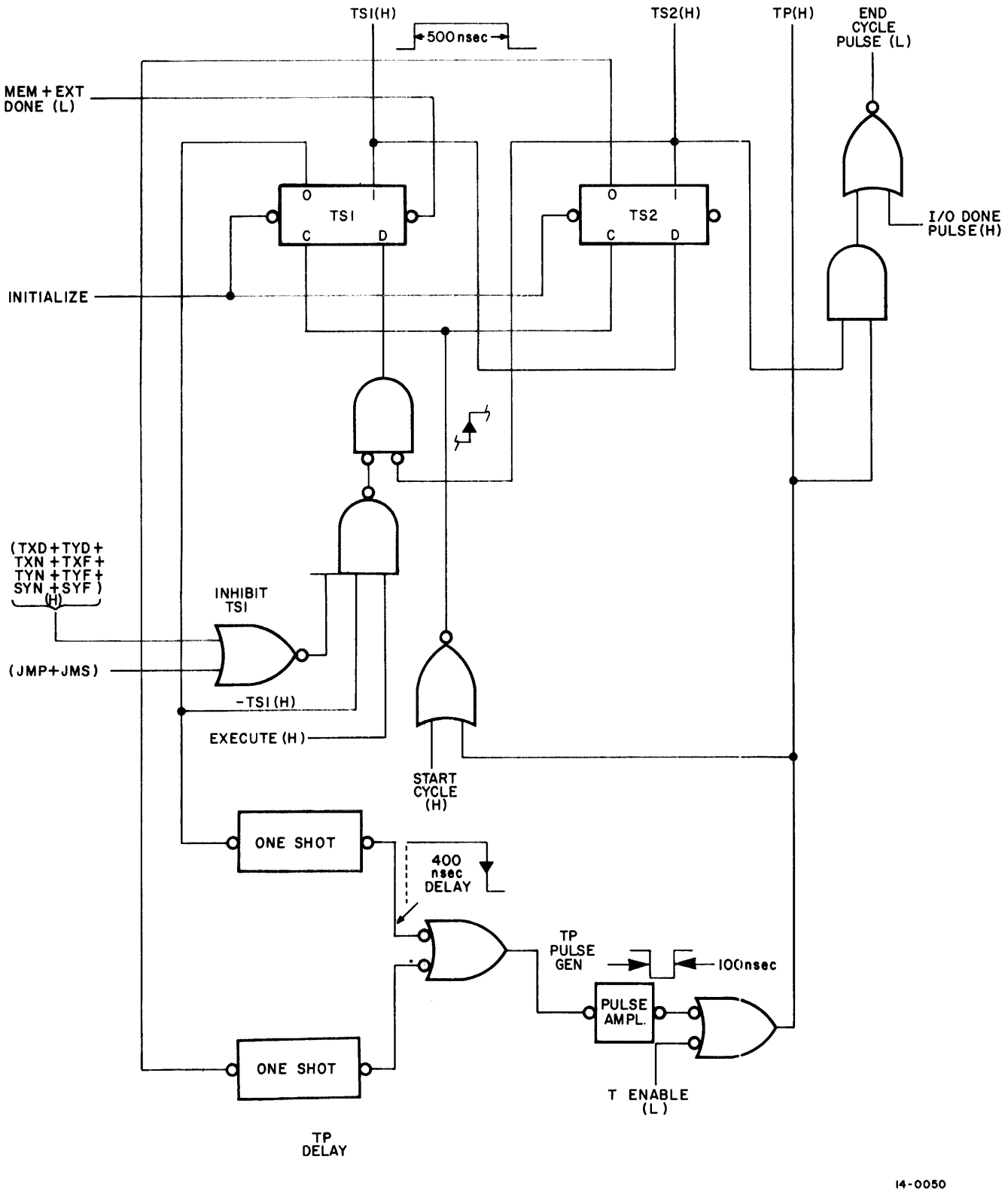


Figure 3-12 TS1, TS2, End Cycle Pulse, and Timing Pulse Generators, Simplified Logic Diagram

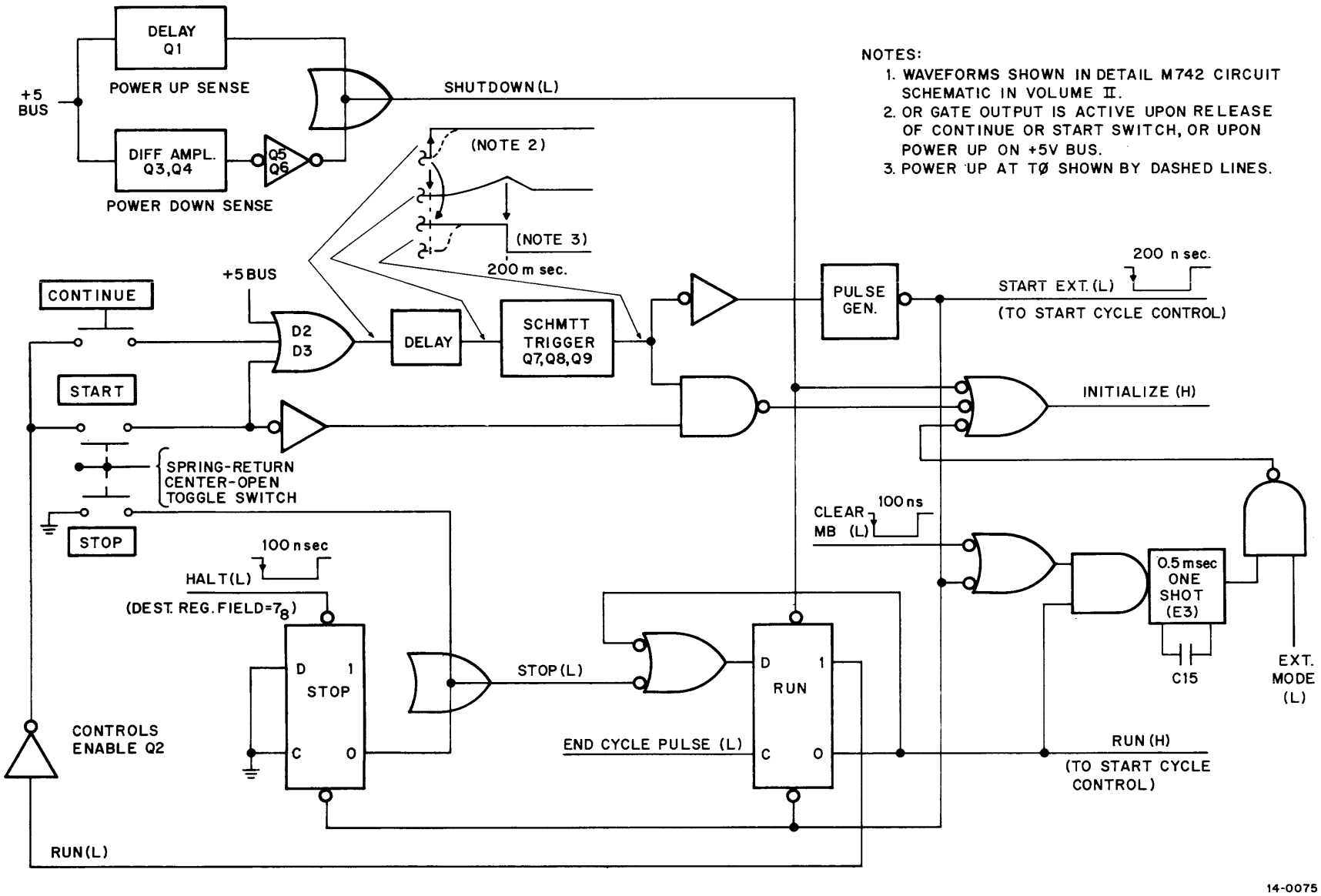


Figure 3-13 Manual Controls and Power Sense Circuits, Simplified Logic Diagram

off. This terminates the initialize signal and releases the capacitor in the input circuit of the Schmitt trigger. Voltage now rises at the input to the Schmitt trigger. When this voltage reaches approximately +2.8 volts, the Schmitt trigger fires through a pulse amplifier, producing a 200 ns pulse which sets the run flip-flop (DC set).

In order to shut down the machine system in a predictable manner when PDP-14 power is removed (accidently or deliberately), a power down sense circuit monitors the +5 volt internal power bus. A differential amplifier constantly compares this bus against a precision voltage divider reference. When the voltage monitored at the differential amplifier input voltage divider falls below this voltage, the initialize line is activated which resets the run flip-flop, all control flip-flops, and all output, storage, and accessory box flip-flops. Sufficient power is available in the power supply filters and within individual module +5-volt bus filter capacitors to permit completion of this operation, even though primary power has been completely removed at the power supply.

3.3.4.2 Manual Controls - When moved to the STOP position momentarily, the STOP/START control push-button resets the run flip-flop at the trailing edge of the end cycle pulse. An AND gate loop from the set output to the data input of the run flip-flop prevents unintentional setting of the run flip-flop when the STOP button is released. Once reset, the run flip-flop can only be set by the Schmitt trigger and external start pulse generator via the DC set input to the flip-flop.

NOTE

For M742 printed circuit revisions C or higher, the STOP position of the START/STOP switch resets output, storage, or accessory box control flip-flops. It only stops PDP-14 activity at the end of the instruction being fetched or executed when the button was pushed in systems containing M742 modules prior to revision C.

Resetting the run flip-flop enables the START and CONTINUE controls by turning on the switch transistor to provide a ground return for the manual switches through the transistor emitter-collector circuit.

With the run flip-flop reset, pressing the CONTINUE switch momentarily will, upon releasing the button, activate the Schmitt trigger and external start pulse generator, which sets the run flip-flop. The program now resumes at the point where it was stopped. The CONTINUE switch does not produce an initialize signal.

With the run flip-flop reset, placing the START/STOP switch momentarily in the START position will produce an initialize signal while the switch is pressed; then, upon release of the switch, it will activate the Schmitt trigger and external start pulse generator to set the run flip-flop. The program is started at ROM address 0000_8, with all output, storage, and accessory box flip-flops reset (retentive memory latching relays are not affected).

The run flip-flop can also be reset when the PDP-14 is operated in external mode. This halt is executed when 7_8 is decoded by the destination register decoder from instruction word bits 9-11. The pulse produced as a result of this decoder output line and the timing pulse during time state 1 is ORed with the initialize line at the DC reset input of the RUN flip-flop.

NOTE

JMP, JMS, EEM, LEM, and all TRR instructions enable the destination register. The halt is performed whenever this register contains 7_8. Instructions of this nature in the ROM program will cause the PDP-14 to "hang" (Stop running). The destination register field should never contain 7_8 in a ROM instruction word.

3.3.5 Read Only Memory (ROM) Circuits

Four Read Only Memory (ROM) modules may be inserted in the PDP-14 mainframe. Each module contains up to $1,024_{10}$ 12-bit control program instruction words. A simplified logic diagram of one ROM module and the module selection scheme is presented in Figures II-20 and 3-14.

3.3.5.1 Instruction Word Selection - The maximum number of instruction word addresses in the PDP-14 is $4,096_{10}$. This is the maximum number that can be contained (in binary) in program counter #1. Every ROM address is obtained from this counter which always holds the complete 12-bit address.

The most significant two bits of the address specify the ROM module containing the instruction word. These two bits are decoded by a ROM module decoder located at mainframe location AB22 (M742 module). ROM modules must be installed in adjacent locations in the mainframe, or the PDP-14 will hang. If no ROM modules are installed, the PDP-14 will execute NOP instructions.

Program Counter bits 2-5 are decoded to select one of 16 matrix transistor rows. Bits 6-8 are decoded to select one of 8 matrix transistor columns via eight current switch transistors. Each transistor in the matrix is connected to one of 128 programmable drive wires. Each drive wire is routed through 8 of 12 sense transformers, so the selection process is completed by decoding the least significant address bits (bits 9-11) to select one set of 12 sense amplifiers corresponding to one instruction word.

3.3.5.2 Timing Circuits - A ROM cycle is initiated by a "mem go" pulse from the pause cycle control circuit (Figure 3-15). The mem go pulse is gated into only the ROM module selected by bits 0 and 1 of program counter #1. Within that module, the mem go triggers the current switch pulse generator which turns on the current switch transistor selected by bits 6-8 of program counter #1. This completes the emitter return path to 16 matrix transistors. The base of one of the 16 transistors has already been selected by program counter bits 2-5; the delay to allow the decoding propagation to take place was produced by the start cycle control circuits before the mem go pulse was transmitted.

In order to prevent drive wire switching transients from being detected by the sense amplifiers, a strobe delay circuit is also triggered by the mem go pulse. The trailing edge of the strobe delay triggers the strobe pulse

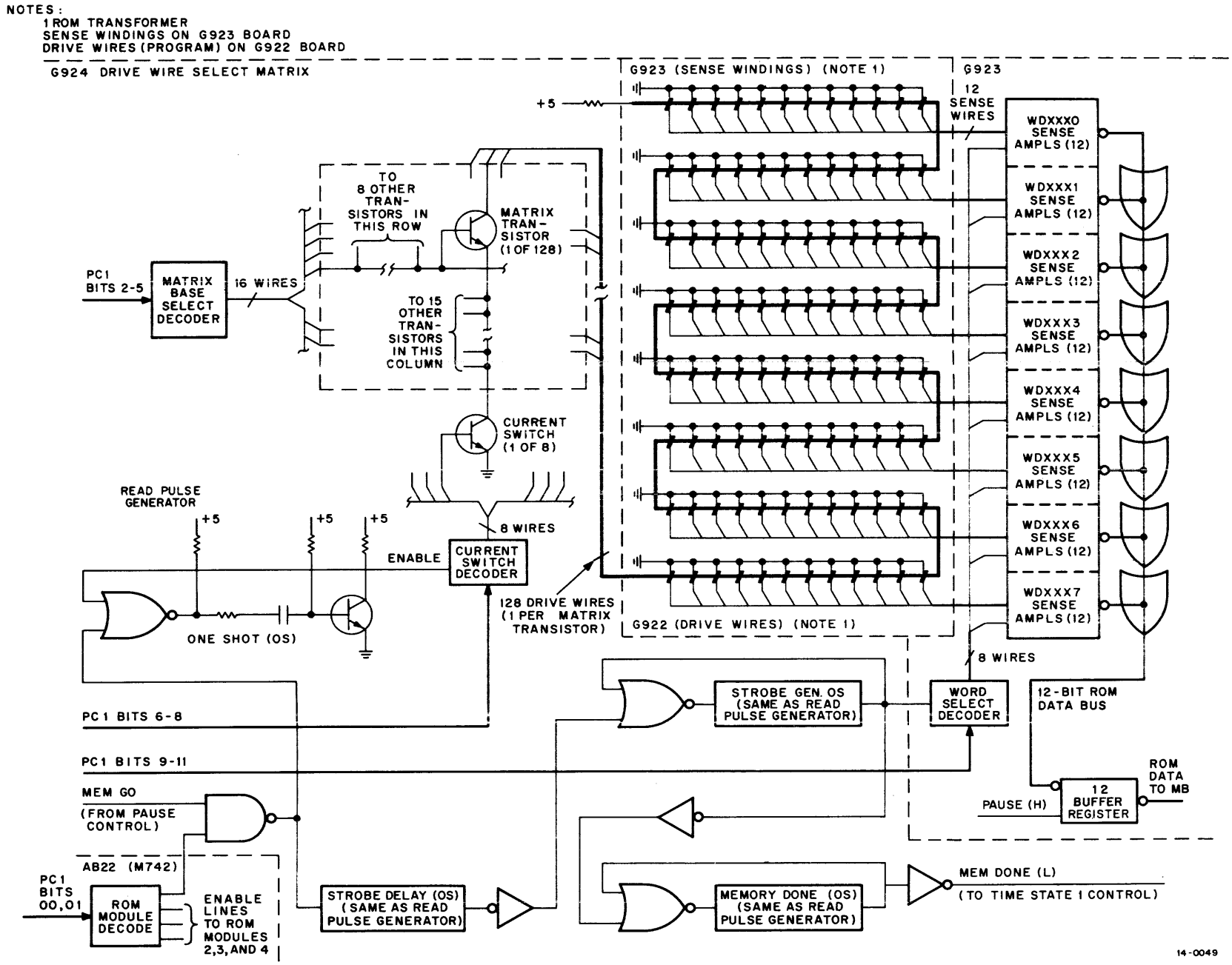


Figure 3-14 Read Only Memory (ROM), Simplified Logic Diagram

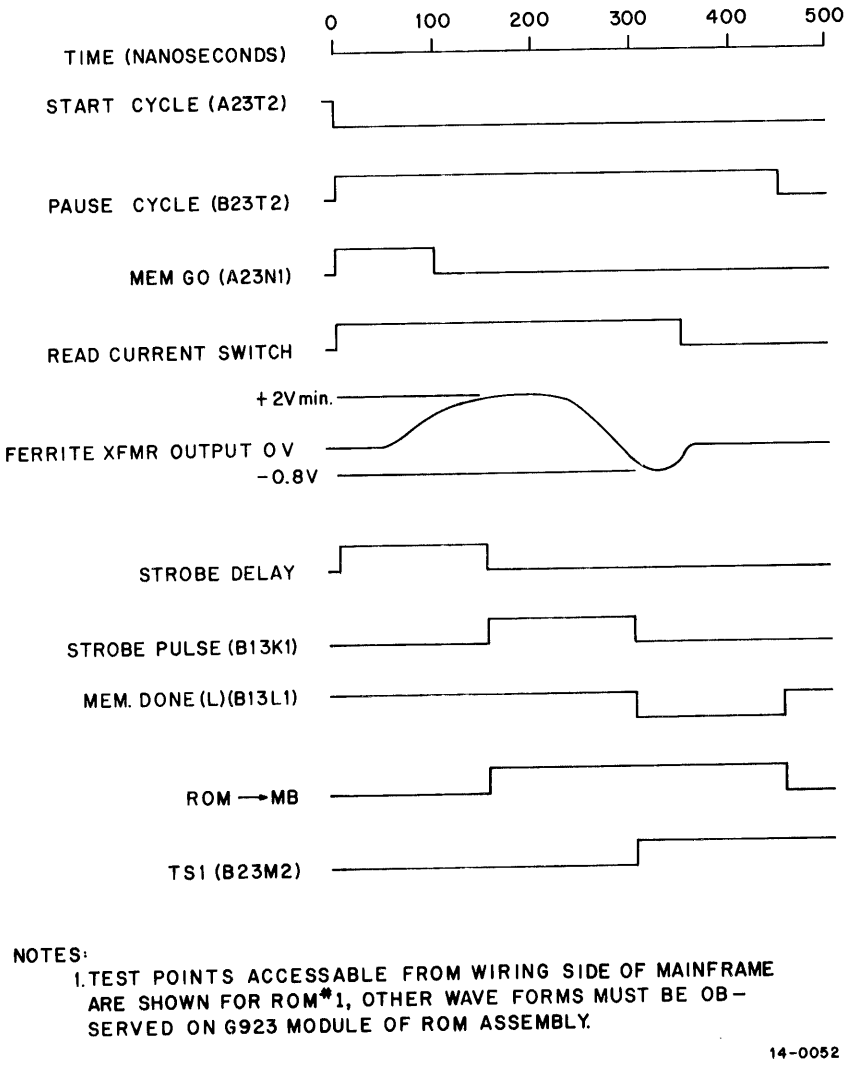


Figure 3-15 ROM Timing Diagram

generator. The strobe pulse enables the group of 12 sense amplifiers selected by bits 9-11 of program counter #1. A "mem done" pulse is triggered by the trailing edge of the strobe pulse. The leading edge of this pulse initiates time state 1, and the trailing edge resets the pause flip-flop. During the overlapping period, ROM data is gated into the memory buffer register.

3.3.5.3 Data Sense Circuits - There are 96 two-part ferrite sense transformers in each ROM module. These are arranged in rows of twelve transformers each, corresponding to the 12 data bits of a control program instruction word. Each of the 128 drive wires threads eight sets of sense transformers, so each drive wire actually holds eight words. The correct word is obtained by selecting the set of sense amplifiers according to the contents of the least significant bits (9-11) of program counter #1.

Each bit of the control program data is stored by routine the drive wire through a sense transformer, if the bit is a "1", or around the transformer, if the bit is a zero. The pattern of one drive wire through or around each of the 96 sense transformers defines the control program data in eight adjacent ROM addresses.

Figure 3-16 illustrates the method used to obtain one bit of the selected data word and place it on the bus to the memory buffer register. If the drive wire selected in the transistor matrix passes through the sense transformer, a positive-going pulse is induced in the secondary, or sense, winding of the transformer. The sense amplifier is not enabled by the strobe pulse, however, until after switching transients caused by placing current on the selected drive wire have settled. These transients are quite short compared to the transformer-induced current in the sense winding.

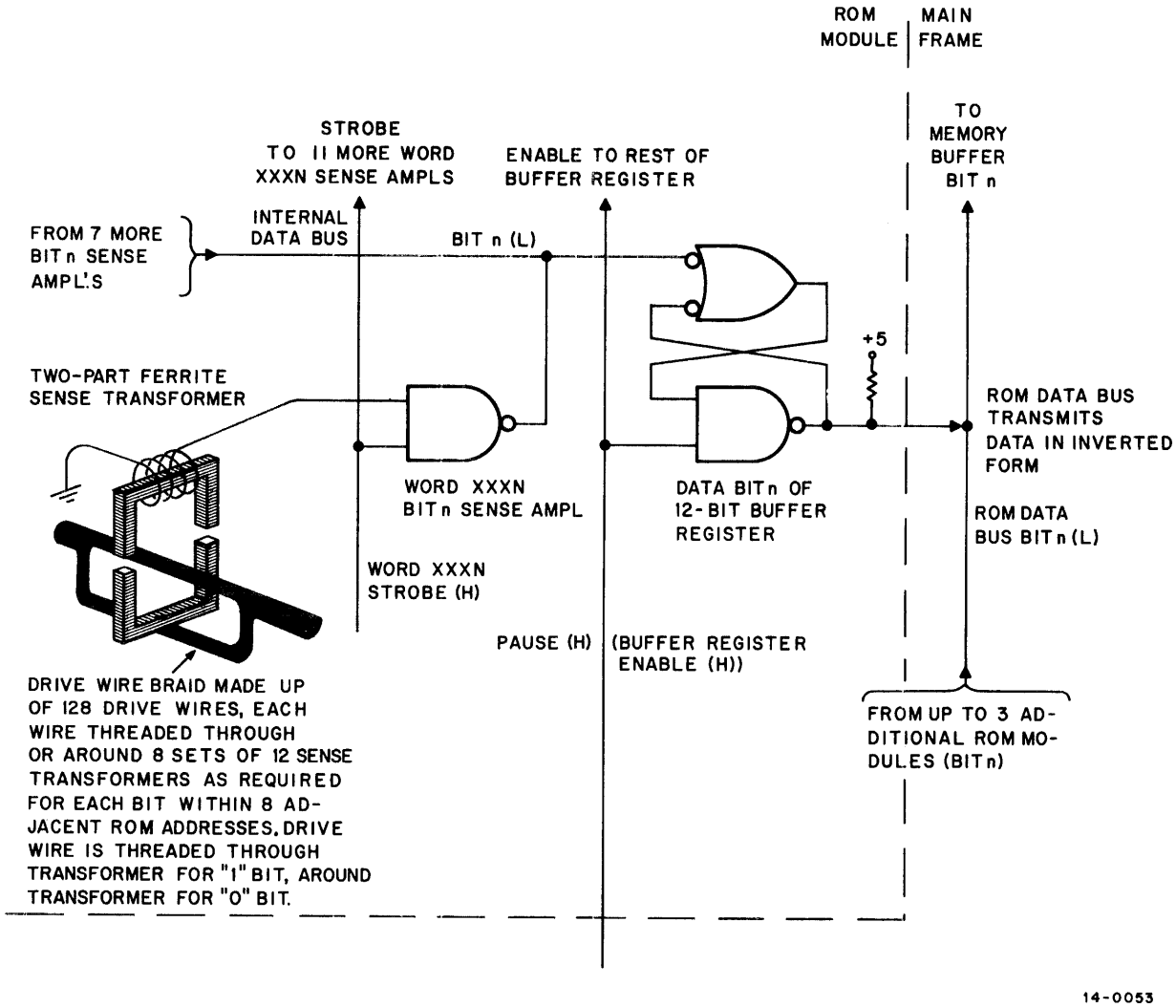


Figure 3-16 ROM Data Sense Circuits, Simplified Logic Diagram

If the selected drive wire passes through the sense transformer, the output of the sense amplifier (shown as a NAND gate) is active. This active low overrides the seven other bit n sense amplifiers in the seven word sets which were not selected by bits 9-11 of PC1.

The bit n storage flip-flop, which was enabled by the leading edge of the pause cycle, is set if the selected sense amplifier is active. Once the flip-flop is set, it will remain set until the trailing edge of the pause cycle; thus the flip-flop stores the bit n data and holds the data on the memory buffer register bus until the data can stabilize in the bit n flip-flop of the memory buffer register. Data is in inverted form ("1" = low) on the memory buffer bus.

3.3.6 Input Box Circuits

A block diagram of input box circuits is presented in Figure II-37. A simplified diagram of input box circuits and input terminal selection is presented in Figures II-56 and 3-17. The input box containing the desired terminal is selected by decoding instruction register bits 4-6. Within the input box, instruction register bit 8 is used to select one of two binary (12 bits 9-11) to eight-line decoders in combination with the box select line. Each of the eight decoder output wires enables a pair of input detectors. One of the pair is connected to the "sample return #1" line, and the other is connected to the "sample return #2" line. The outputs of the unselected input detector circuits are held low by their selection lines. If either of the selected terminals is active, the sample return line to which it is attached is permitted to go low by the enabling lines from the decoder.

Instruction bit 7 is used to select the sample return line carrying data from the terminal of the pair selected by instruction register bits 8-11.

The terminal selection process thus far described is simultaneously carried out to select a corresponding Y function (output, storage, or accessory box terminal or function). Therefore, the final selection of an input box terminal is restricted to those instructions which specify an X (input box) address. These instructions are TXN, TXF, and TXD.

There are 32 identical input detector circuits in each input box. One such circuit is shown in Figure 3-17. The control input from the external machine system is returned to AC ground through the primary of an isolation transformer. A neon lamp is also connected across the input to provide a visual indication that the control line is on. A diode detector, voltage divider, and filter capacitor develop the DC logic levels required within PDP-14 circuits.

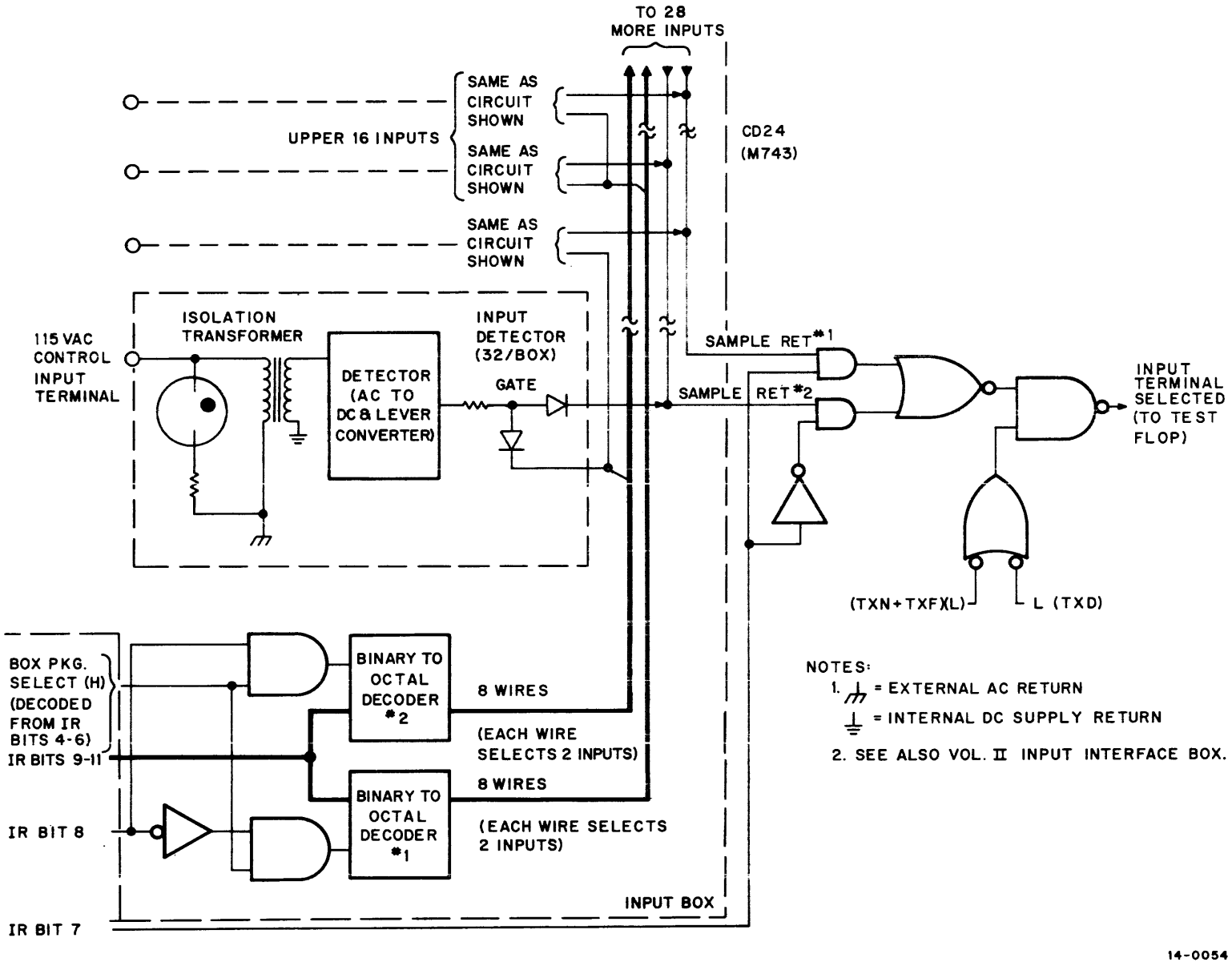


Figure 3-17 Input Box Circuits, Simplified Logic Diagram

3.3.7 Output Box Circuits

A block diagram of output box circuits is presented in Figure II-40. A simplified diagram of output box circuits and output terminal selection is presented in Figures II-57 and 3-18. The output box containing the desired terminal is selected by decoding instruction register bits 4-6. Within the output box, instruction register bit 8 is used to select one of two binary (instruction register bits 9-11) to eight line decoders in combination with the box select line. Each of the eight decoder output wires enables a single control flip-flop.

There are 16 control flip-flops in each output box. Each control flip-flop drives a single TRIAC (solid-state AC switch) circuit, which, in turn, drives the external machine system device (Figure 3-19). The TRIAC circuit is transformer-isolated from PDP-14 system circuits.

As the terminal selection has been carried out at the same time for input box terminals, the final selection of an output box terminal is restricted to those instructions which specify a Y (output box) address. In addition, the operation code field of the output instruction specifies whether the selected output control flip-flop is to be set, reset, or tested. To test an output terminal, a return line is provided and the state of the selected control flip-flop is gated via this line to the test comparator in exactly the same manner an input terminal is tested.

3.3.8 Storage Box Circuits

A block diagram of storage box circuits is presented in Figure II-48. Storage box circuits are identical to output box circuits, except that the TRIAC (K614) circuit associated with every output box control flip-flop is deleted. The storage box flip-flops perform a temporary storage function, but they are addressed, set, reset, and tested in exactly the manner output box flip-flops are handled.

However, because the output box TRIAC circuits are not required, 32 storage flip-flops may be located in one box. This is not significant electrically because an additional cable is simply run from a second mainframe output box connector to a second connector on the 32 flip-flop storage box (BF14-F). Half-storage boxes (BD14-H) are also employed, having only 16 flip-flop storage elements and a single interface cable to the PDP-14 mainframe.

3.3.9 Accessory Box Circuits

A block diagram of accessory box circuits is presented in Figure II-43. Accessory boxes may have two types of circuits: delay circuits that change state at a specified time following initialization (timers), and mercury latching relays that do not change state when power is removed from the PDP-14 system (Retentive Memory). Like the storage box flip-flops, these functions are for PDP-14 internal use and are addressed, set, reset, initialized (in the case of time delay circuits) as though they were output terminals (Y addresses). The supporting electronics for the timer and retentive memory modules are identical to those used in output boxes.

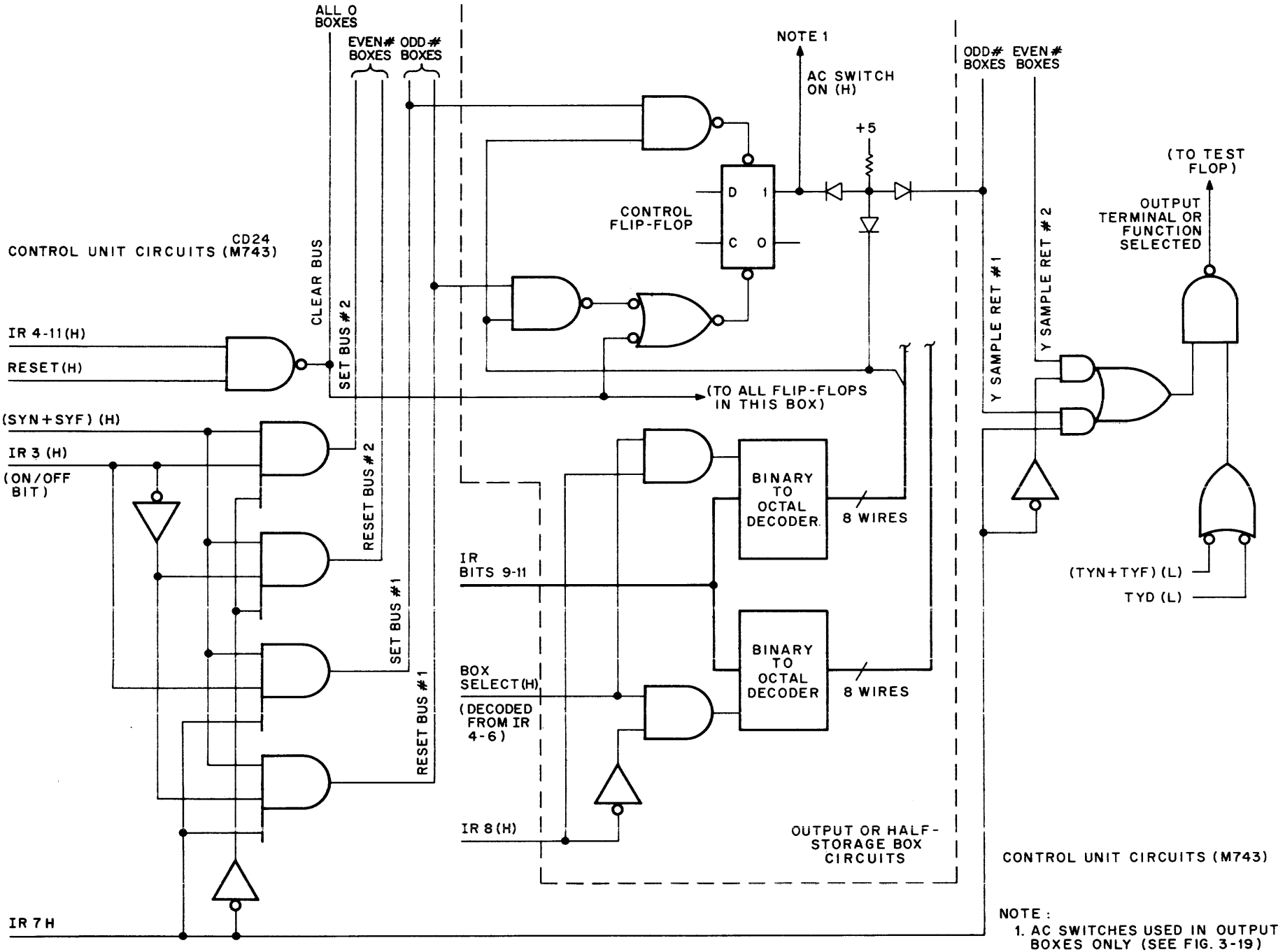


Figure 3-18 Output and Storage Box Circuits, Simplified Logic Diagram

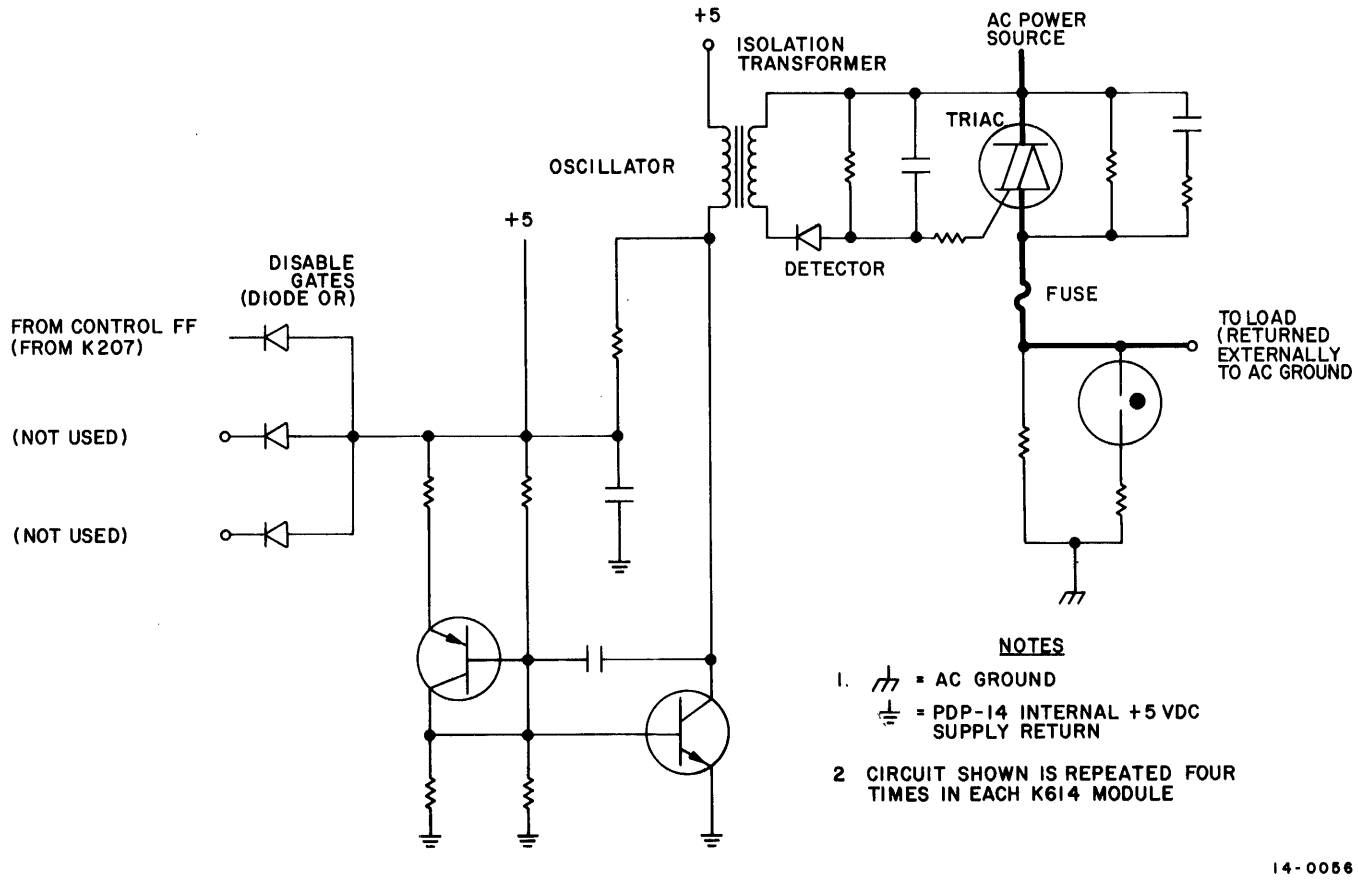


Figure 3-19 Output Box AC Control Circuit, Simplified Schematic Diagram

3.3.9.1 Retentive Memory - Each accessory box can contain up to four retentive memory modules. These modules must be installed in the option slots at the right side of the accessory box, as viewed from the front. This is necessary in order to keep the mercury-wetted latching relay on each module in an upright position.

As each retentive module contains only one relay, that relay is addressed by the even number octal address applicable to that module location within the accessory box.

The retentive modules are used to store machine or process system status in the event power is removed from the PDP-14. It should be remembered that all output control and storage flip-flops are reset as part of the initialization process when power is first applied to the PDP-14 (via an automatic SYF377 instruction). This initial reset does not affect the state of retentive memory relays. Therefore, the states of these relays can be tested by the PDP-14 to determine critical machine or process system conditions as they existed when the shutdown occurred.

3.3.9.2 Timers - Each accesory box can contain up to 16 timers: two timers to each of eight timer modules. The option slots at the right side of the accessory box can be used for timer or retentive memory modules.

Each timer circuit (two per module) offers three time delay range options determined by the selection of a capacitor for an R/C delay circuit. Vernier timing within the selected range is provided by a screw-adjusted potentiometer, which forms part of the resistance in the R/C circuit (see Figure 3-20). The delay circuit is controlled by a flip-flop in the associated K207 module in the same manner described for output box switches. The delay is initiated when the flip-flop is set. This turns the input inverter, Q1, off. Q3, which had been holding the charge on the delay R/C, is now turned off. The charge on the delay capacitor begins to bleed through the resistance portion of the delay R/C until the voltage on the base of Q5 falls below the reference voltage present on the emitter of that transistor. Q5 now begins to conduct, turning on Q6. A feedback resistor between the collector of Q6 and the base of Q5 produces a sharp transition at the end of the delay time, as both Q5 and Q6 saturate. Q6 emitter current is now provided via the Q5 emitter-base junction, even after the charge in the delay R/C capacitor has been completely bled. Q6 turns on Q9, which turns bus driver Q13 off. The collector of Q13 now supplies a logic 1 (high) to the sample return bus when the delay is tested by the control unit.

It should be noted that the control flip-flop must be maintained in set state until the delay has timed out. If this flip-flop is reset before the charge on the delay R/C has drained, Q3 will be turned on and the charge will be immediately restored.

Note also that the control flip-flop must be turned off before again using the delay, in order that the charge on the delay R/C capacitor be restored. Resetting the control flip-flop produces an almost immediate logic 0 (low) at the delay circuit output.

3.4 EXTERNAL COMPUTER INTERFACE

Provision has been made in the PDP-14 to permit data transfer between it and an external computer. The external computer may be one of the following: PDP-8/I; PDP-8/L; or PDP-12. Instructions TRM, TXD, and TYD may be contained within the ROM control program to make available to the external computers the state (on or off) of the test flop and the state of a particular input level or output control flip-flop (whether the flip-flop is in an output box or storage box, or the state of the time delay or latching relay within an accessory box). Block diagrams of the interface circuits for PDP-8/I and PDP-8/L external computers are presented in Figures II-29 and II-30, respectively.

An external computer may also assume complete control of the PDP-14 system, either by initiating an interrupt ("cycle steal") instruction which delays the execution of the next ROM instruction for the time required to perform the instruction transferred during the interrupt; or by transmitting an EEM (Enter External Mode) instruction while the PDP-14 is interrupted.

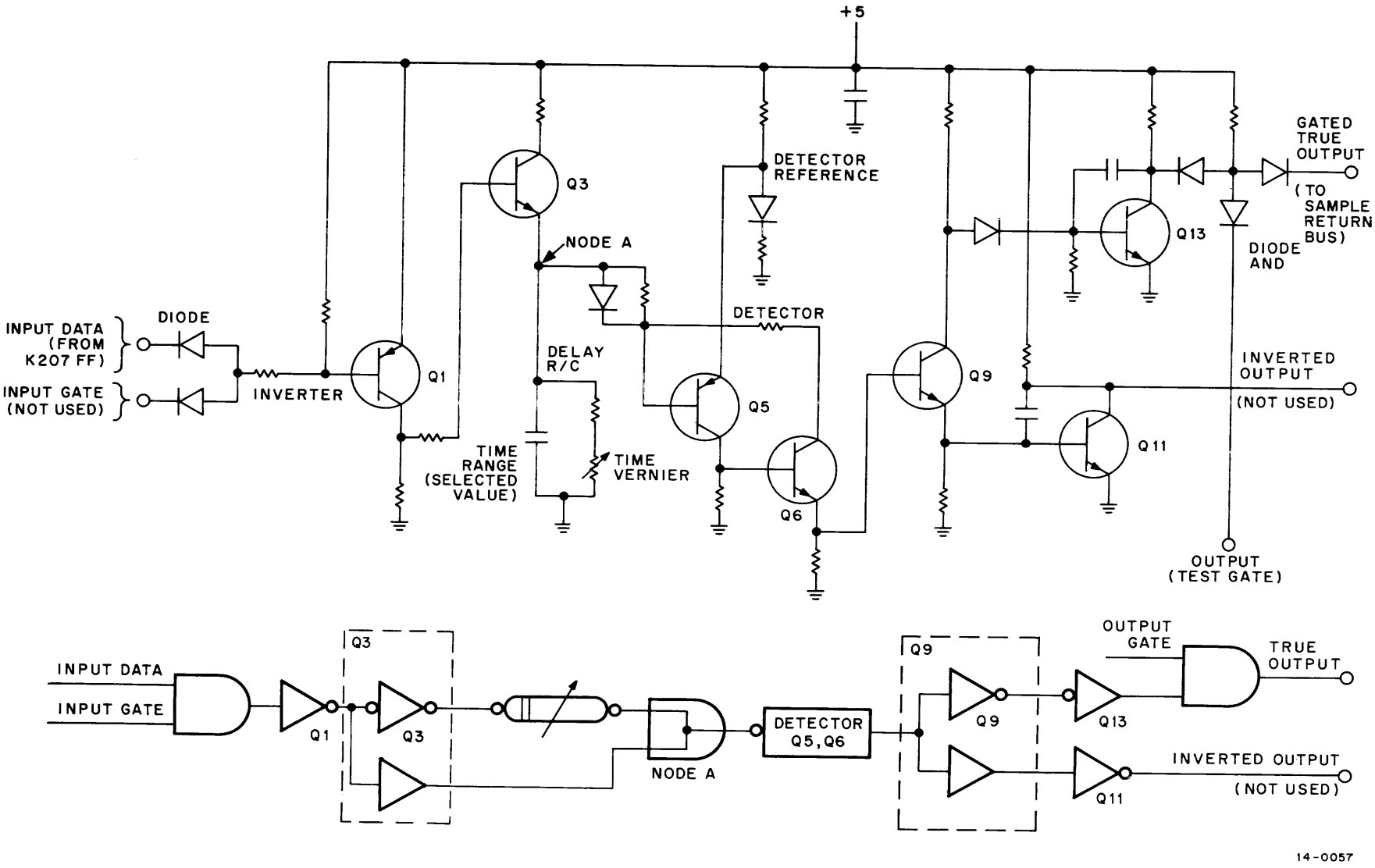


Figure 3-20 Timer Module, Time Delay Circuit, Simplified Schematic Diagram, and Equivalent Logic Diagram

After the PDP-14 executes an EEM instruction, all PDP-14 operations are under the control of the external computer until a LEM (Leave External Mode) instruction occurs.

NOTE

An interrupt by an external computer does not affect the execution of the ROM program unless so directed, because the contents of program counter #1 are not affected. However, if the interrupt contains an EEM instruction, all subsequent LDE instructions will cause PC1 to be incremented as they are executed (GNI does not increment). Hence the return address for the next sequential ROM instruction must be stored by the interrupting external computer program.

3.4.1 External Control Instruction Set

In order to control the PDP-14 from an external computer, a special decoder is provided on the M745 module at PDP-14 mainframe location AB18. First, when the most significant three bits (0-2) contain 6_8 (110_2), the external computer word is an IOT (In/Out Transfer) instruction as decoded by the external computer. This decoder monitors bits 3-11 of the external computer memory buffer. Bits 3-8 of the instruction define the device (in this case the PDP-14) and bits 9-11 (plus the IOP bits) define the PDP-14 operation to be performed.

The external control decoder within the PDP-14 is actually enabled by both 16_8 and 17_8 device codes, and the least significant bit of the device code field (bit 8) is used to double the number of control instructions, which would otherwise be restricted to a total of eight (the maximum that can be specified by bits 9-11 alone). The IOT instructions affecting PDP-14 operation are described in Table 3-3.

Table 3-3
External Control (IOT) Instruction Set

Assembly Language Mnemonic	Instruction Field	Definition
GNI	110 001 110 101 (6165_8)	Sets PDP-14 interrupt flag and clears the PDP-14 external flag. Contents of external computer accumulator is transferred to PDP-14 memory buffer instead of ROM word during PDP-14 fetch major state. PC1 is not incremented during the interrupt unless so directed. External flag is set. NOTE If a GNI instruction is used to supply the TRM instruction while the PDP-14 is in external mode, the contents of the ROM address specified by the contents of the PDP-14 PC1 will be transferred to the output register for subsequent transfer to the external computer.

Table 3-3 (Cont)
External Control (IOT) Instruction Set

Assembly Language Mnemonic	Instruction Field	Definition
LDE	110 001 110 100 (6164_8)	Load the PDP-14 memory buffer from the external computer accumulator while the PDP-14 is in EXTERNAL mode. The PDP-14 program counter is incremented each time this instruction is executed. While executing the instruction loaded into its memory buffer, the PDP-14 external flag is reset. The PDP-14 sets the external flag upon completion of execution to enable the external computer to introduce another instruction (or the second part of a two word instruction).
CEF	110 001 110 111 (6167_8)	Clear the PDP-14 external flag.
CLF	110 001 111 010 (6172_8)	Clear the PDP-14 output flag. This flag is set by the PDP-14 whenever data is placed in the output register for transfer to the external computer. This instruction permits the external computer to clear the flag without accepting the data held in the PDP-14 output register (see ROR instruction, below). The external computer accumulator is also cleared.
LIR	110 001 110 010 (6162_8)	Loads the PDP-14 input register from the external computer accumulator. Utilization of this data within the PDP-14 requires a PDP-14 input to XXX transfer instruction (e.g., input to PC1).
ROR	110 001 111 110 (6176_8)	Transfers the contents of the PDP-14 output register to the external computer accumulator and clear the PDP-14 output flag (set by the PDP-14 when data was placed in the output register). The output flag from the PDP-14 must be honored by the external computer with an ROR instruction before the PDP-14 places new data in the output register or the original data will be lost.
SEF	110 001 110 001 (6161_8)	Causes the external computer to skip its next sequential instruction if the PDP-14 external flag is set.
SOF	110 001 111 001 (6171_8)	Causes external computer to skip its next sequential instruction if the PDP-14 output flag is set.
STF	110 001 111 011 (6173_8)	Causes external computer to skip its next sequential instruction if the PDP-14 test flop is set.
SCR	110 001 111 101 (6175_8)	Causes external computer to skip its next sequential instruction if the PDP-14 is running (run flip-flop set).

3.4.2 External Mode Instruction Set

The instructions described in Table 3-4 are for use in the external computer interfaced with the PDP-14. Once control of the PDP-14 has been transferred from the ROM program to an external computer by an external computer interrupt (GNI) instruction, all of the internal instructions listed in Table 3-1 may be supplied by the external computer program, as well as those described in Table 3-4.

Table 3-4
External Mode Instruction Set

Assembly Language Mnemonic	Op Code Field	Definition
EEM	000 110 000 000 (0600_8)	This instruction must be contained in the external computer accumulator when an external computer GNI instruction is performed if the external computer is to assume control of the PDP-14. This instruction sets the PDP-14 external mode flip-flop during the execute major state, which in turn sets the external flag during the following fetch major state.
EES	000 110 100 101 (0645_8)	This instruction performs the same function as the EEM instruction described above. In addition, however, the contents of PC1 are stored in PC2 in order that a subsequent LER instruction encountered in the external computer program can return the PDP-14 to the ROM program instruction, following the last ROM instruction executed before the interrupt transferring program control to the external computer. NOTE Obviously, the external computer program must not contain instructions affecting the contents of the PDP-14 PC2.
LEM	000 100 000 000 (0400_8)	This external computer instruction returns the PDP-14 to internal control by resetting the external mode flip-flop during the execute major state which in turn prevents setting the external flag. The point at which the PDP-14 picks up the ROM program is determined by the current contents of the PC1.
LER	000 110 101 110 (0656_8)	This instruction performs the same function as the LEM instruction described above. In addition, however, the contents of PC2, which were transferred from PC1 at the beginning of the external mode operation by an EES instruction, are transferred back into PC1 in order that the ROM program be resumed at the point it was interrupted.

Table 3-4 (Cont)
External Mode Instruction Set

Assembly Language Mnemonic	Op Code Field	Definition
TRM	100 010 010 110 (4226_8)	If TRM is the instruction transferred by a GNI instruction, the contents of the ROM address contained in PC1 will be transferred to the external computer (see GNI instruction).
TRS	100 010 010 101 (4225_8)	Transfers the contents of the address specified by the following 12-bit word from the PDP-14 memory buffer to PC2. As PC2 is used to hold the return address from subroutines (or return address stored by an EES), this instruction may be used to change the return address while the PDP-14 is in external mode.

3.4.3 External Computer Interface Circuits

External Computer Interface Circuits are diagrammed in Figure 3-21. Bits 3-8 of the external computer buffered memory bus are routed to the device field decoder. If this field contains 16_8 or 17_8, bits 9-11 of the same bus are gated into the external control (IOT) decoder. Bits 9-11 are used within the external computer to select three input/output timing pulses (IOP): bit 9 gates out IOP 1, bit 10 gates out IOP 2, and bit 11 gates out IOP 3. Any one or all three of these pulses may be gated out on the IOP bus, depending on the configuration of bits 9-11 from the external computer memory. However, the external control decoder within the PDP-14 uses only the IOP appropriate to the function to be performed, based on bits 9-11 of the BMB (and bit 8, which essentially doubles the number of external control functions that can be decoded within the PDP-14).

NOTE

Refer to Chapter 12 in the DIGITAL Small Computer handbook (1970 Edition) for complete description of the Computer Interface and associated circuits.

The external control decoder permits the external computer to interrupt the PDP-14 program or to modify its own program by selecting conditional skips based on the status of the PDP-14. The selected skip condition is monitored within the PDP-14 skip condition detector. There are four PDP-14 conditions which may be selected by the external computer program to cause a skip within that program: PDP-14 external flag set; PDP-14 run flip-flop set; PDP-14 test flop set; and PDP-14 output flag set. If the selected condition exists, the skip pulse (timed by IOP 1) is sent back to the external computer program counter over a single skip control line.

Two other control discretes are routed from the PDP-14 to the external computer. The interrupt request line informs the external computer that data is available in the PDP-14 output register for transfer to the external computer (output flag), or that the PDP-14 is ready to receive data or an instruction from the external computer (external flag). The external computer accumulator register is also cleared by the external control decoder in preparation to receive data from the PDP-14 output register. This clear pulse is strobed by IOP 2 in order that the accumulator be cleared before the contents of the output register are gated onto the output bus by IOP 4.

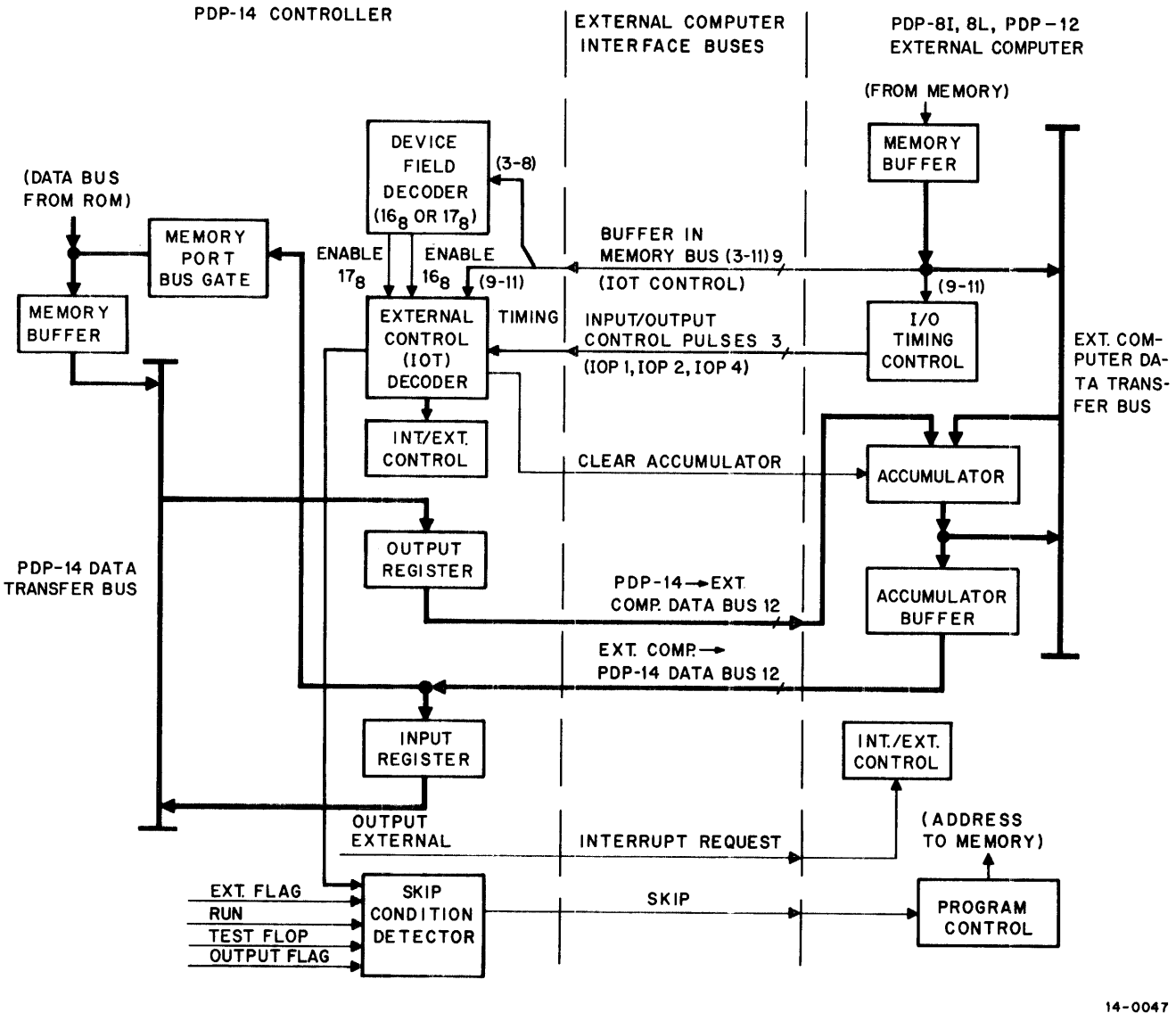


Figure 3-21 External Computer Interface, Detailed Block Diagram

The remaining two interface buses are data transfer buses. The output bus transfers the contents of the PDP-14 12-bit output register to the external computer accumulator (during ROR instructions). The input bus transfers data from the external computer accumulator buffer register to the PDP-14 memory buffer, if the word is a PDP-14 instruction, or to the PDP-14 input register, if the word consists of data to be operated on by a PDP-14 instruction.

3.4.4 Interrupt and External Mode Control Circuits

Figure 3-22 diagrams the logic circuits associated with the interrupt, interrupt sync, and external mode flip-flops. When an IOT 165 (GNI) instruction from the external computer is decoded, the clock input to the

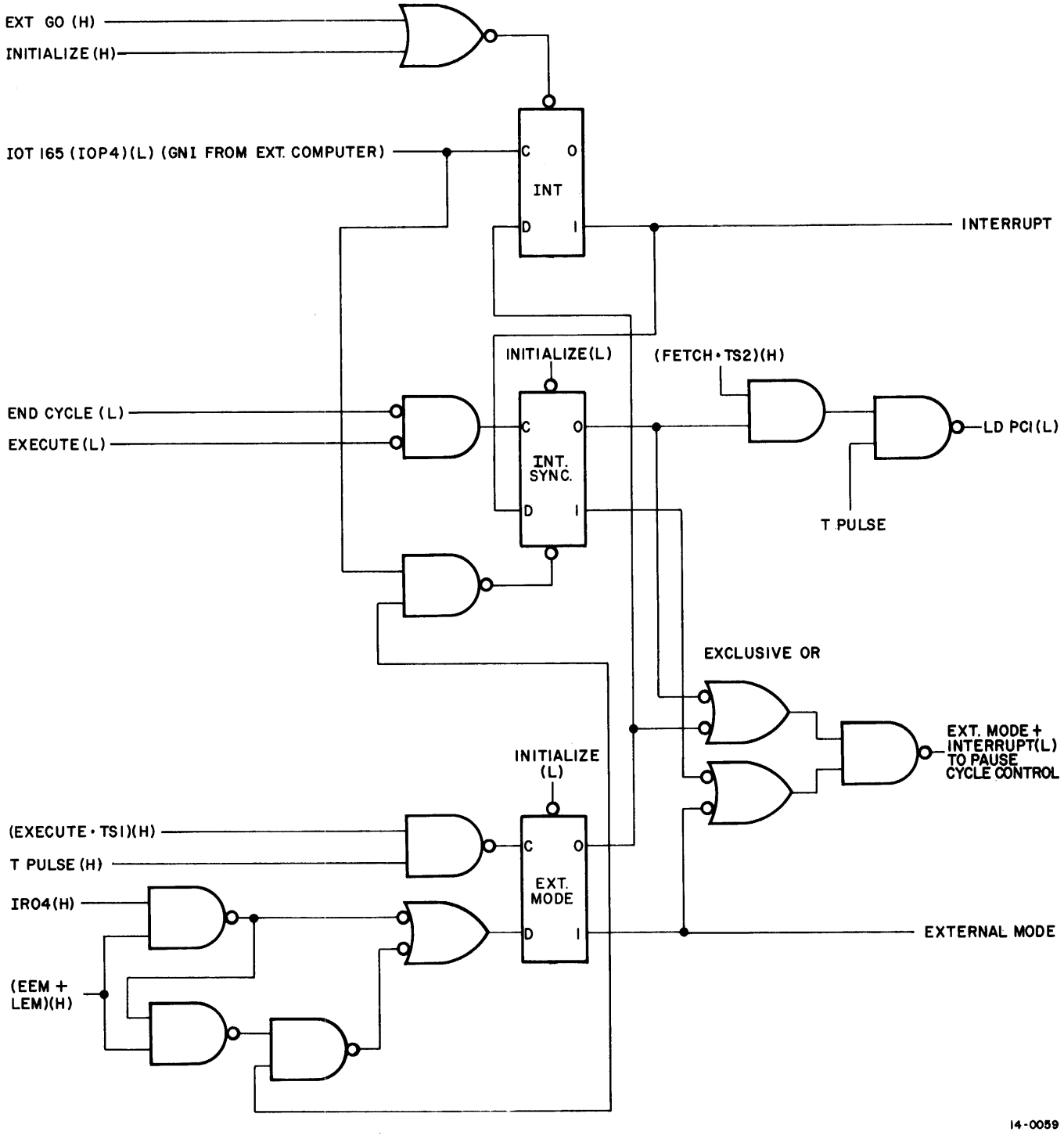


Figure 3-22 Interrupt and External Mode Controls, Simplified Logic Diagram

interrupt flip-flop is supplied a negative-going IOP 4 pulse. If the external mode flip-flop has not been previously set, the interrupt flip-flop is set at the trailing edge of the IOP 4 pulse.

The interrupt sync flip-flop is subsequently set, inhibiting the normal increment of program counter #1. Thus, program counter #1 will resume the PDP-14 internal ROM program at the next sequential instruction. In addition, setting the interrupt sync flip-flop causes the data on the input bus from the external computer accumulator to be gated into the PDP-14 memory buffer register. During internal mode operation, the PDP-14 memory buffer register is loaded from the ROM.

If a GNI is encountered while the external mode flip-flop is set, an exclusive OR produces the same pause control output as internal mode operation. Thus, placing a GNI in the external computer program after placing the PDP-14 in external mode enables reading sequential ROM address without having to place the PDP-14 back in internal mode operation.

The external mode flip-flop is controlled from the instruction register decoder. Instruction register bit 4 is set during an EEM instruction that sets the external mode flip-flop during the trailing edge of the timing pulse of TS 1 of the execute major state.

Figure 3-23 diagrams the external flag and output flag control circuits. The external flag is set upon completion of a GNI instruction from the external computer. This generates an interrupt request to the external computer, in order to obtain the data to be gated into the PDP-14 memory buffer. The external flag flip-flop is clocked by the clearing of the interrupt sync flip-flop, and, in the absence of either DC flip-flop control conditions, will cause the external flag flip-flop to be set.

The output flag is set from within the PDP-14 whenever data is available in the output register for transfer to the external computer. Setting either flag will cause an external computer interrupt request. The output flag is reset by a CLF or ROR instruction from the external computer (the data input is strapped as a zero).

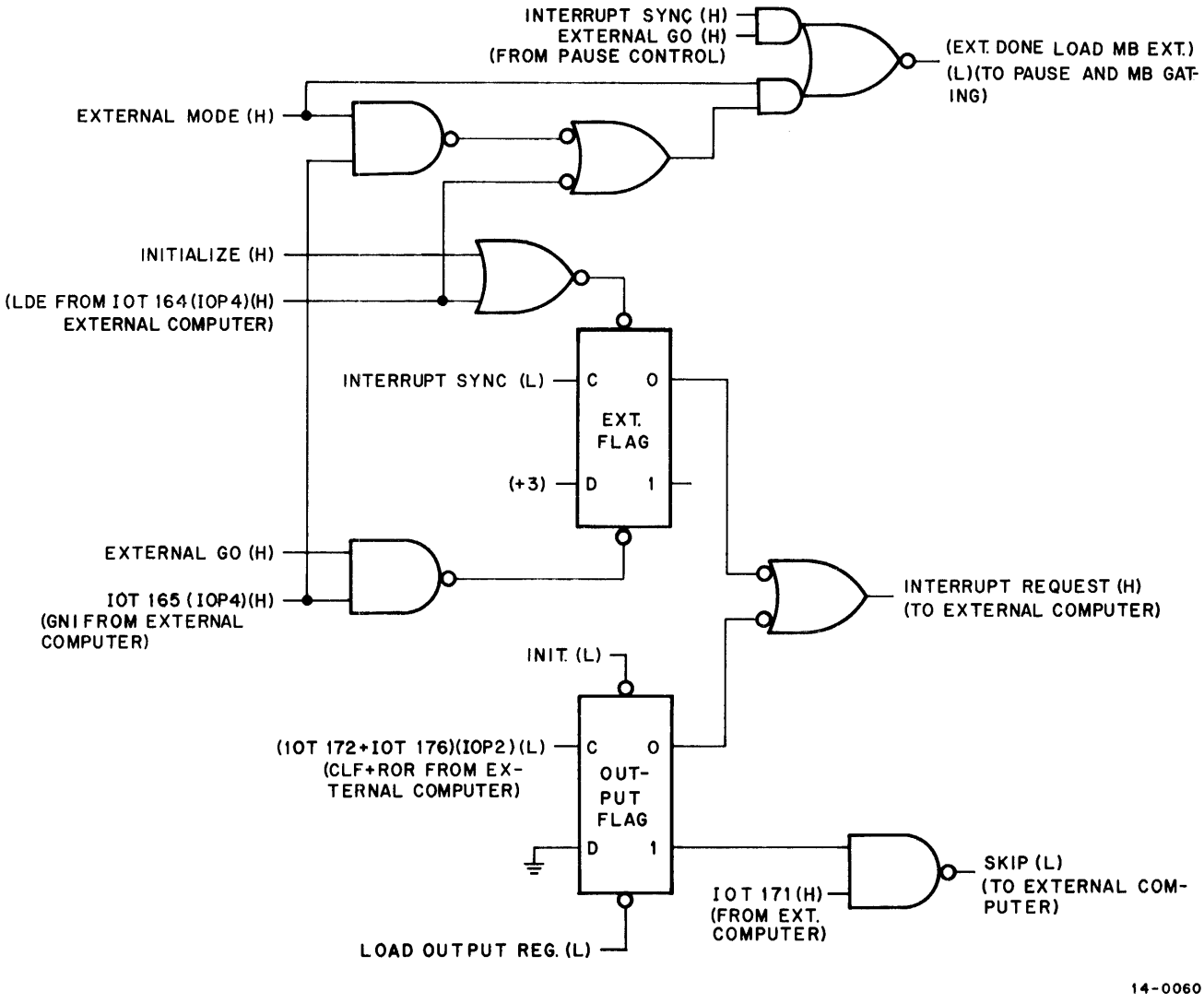


Figure 3-23 External and Output Flags, Simplified Logic Diagram

CHAPTER 4
OFF-LINE MAINTENANCE

4.1 GENERAL

The procedures described in this chapter cover detailed fault isolation of the PDP-14 using standard digital equipment test procedures. These procedures should be used in the unusual event that the procedures of Chapter 2 fail to correct the fault, or to repair defective modules that have been removed from an on-line PDP-14.

The same programs and test computer employed in Chapter 2 are used here. However, the use of program loops is explained to permit the faulty PDP-14 circuitry to be examined with a dual-trace oscilloscope. In addition, more detailed explanations of the test program error printouts are supplied to permit maximum use of this material in fault isolation.

In order to make effective use of this chapter, it is necessary to be completely familiar with PDP-14 operation. This information is presented in Chapter 3. Volume II of this manual consists of a complete set of PDP-14 engineering drawings: block diagrams, module circuit schematics, and module component location drawings. The module component location drawings and module schematics are located on facing pages in order to facilitate probing the circuit and replacing defective module components.

All troubleshooting described in this chapter consists of dynamic tests; that is, the PDP-14 must be running and the module or modules in question must be connected to the PDP-14 mainframe via module extenders, which permit the modules to be probed while they are active. Refer to Figure 3-7 for timing and major state test points.

NOTE

The procedure for connecting the test computer to the PDP-14 is described in steps one through six of Paragraph 2.3.1. This procedure must be performed before selecting the appropriate test procedure from the following paragraphs.

4.2 COMPONENT FAULT ISOLATION PROCEDURES

Select the procedure under this heading corresponding to the major PDP-14 system component in question (control unit, input box, output box, etc.). A PDP-14 control unit must be used in all procedures. If other than control unit circuits are to be checked, the control unit must be functioning properly.

4.2.1 Control Unit Procedure

Step	Procedure

1 Perform the Test-14 procedure described in Paragraph 2.3.1 through Step 22. (Steps 1 through 6 should have already been performed.)

2 The error printouts associated with the error codes take the following basic forms:

a.
```
**AA**      BASIC GATING AND INTERFACE TESTSX
            OLD       GOOD      BAD
INPUT       ----      0002      0000
INPUT       ----      0003      0001
INPUT       ----      0006      0004
```

In the example shown above, the error designator is "AA". The operator can go to the module call table and look up "AA" or he can analyze the rest of the message. The tests being performed involved some of the basic gating of the PDP-14 and the PDP-8I/8L to PDP-14 Interface module. The failing register was the "Input Register" (or possibly the "Output Register", as it is impossible to tell at this point in the testing scheme). Since the old contents of the register are not important, there is no entry in that column. The GOOD Column lists the data entered by the test program. The BAD Column lists the incorrect register contents. Analysis of the typeouts indicate a problem with the gating of bit 10.

b.
```
**AQ**      0334      (JMR)     TEST
            OLD       GOOD      BAD
SPARE       3642      3642      3600
PC1         0000      3643      3600
```

It is possible that more than one register can be affected in a test. In the example shown above, gating between the "Spare Register" and "PC1" was being tested. Since the data in the "Spare Register" was destroyed, both registers contained the wrong numbers when the test was completed. The number following the error code is the PDP-14 instruction.

c.
```
**BH** SYF 377 LEFT ON OUTPUT OR TEST FLOP ALWAYS SET BY TYN 0000
**BH** SYF 377 LEFT ON OUTPUT OR TEST FLOP ALWAYS SET BY TYN 0001
**BH** SYF 377 LEFT ON OUTPUT OR TEST FLOP ALWAYS SET BY TYN 0002
**BH** SYF 377 LEFT ON OUTPUT OR TEST FLOP ALWAYS SET BY TYN 0002
```

The above example indicates a problem in the I/O section of the PDP-14. The operator can refer to the module call for error "BH" after reading this message, or he can further analyze the message if he desires to 'scope' the error. In this test, he would scope the "SYF 377" instruction and the "TYN" class of instruction to check pulse generation, addressing, gating, decoding, etc, in the PDP-14 processor and in the I-Box affected. The 4-digit number at the far right identifies the terminal selected by the program.

d.
```
**CB** XXXX TURNED OFF BY SYF YYYY
**CC** XXXX TURNED ON BY SYN YYYY
```

The Y terminal specified by the second 4-digit number has incorrectly affected the Y terminal identified by the first 4-digit number.

e.
```
**BS** TEST FLOP NOT SET BY TXF XXXX
**BX** TEST FLOP NOT SET BY TYN XXXX
**BV** TEST FLOP SET BY TXN XXXX
**BY** TEST FLOP SET BY TYF XXXX
**BZ** TEST FLOP NOT SET BY TXN XXXX
**CA** TEST FLOP SET BY TXF XXXX
```

Step	Procedure
2 (cont)	In these error codes, the terminal specified by the 4-digit number typed in the code has produced an incorrect response by the test flop.

f. PDP-14 STOPPED
PDP-14 HUNG

There are a few PDP-14 errors which the program cannot diagnose, although they are detectable. Two of these are shown above. If the PDP-14 stops, the above printout will occur and the PDP-8 will stop. If stoppage of PDP-14 causes other errors, depressing PDP-8 "CONTINUE", after depressing PDP-14 "CONTINUE" may provide more information about the error. Refer to Paragraph 4.2.4 for additional troubleshooting suggestions for these and similar problems.

3 After use of the information presented in Step 2 of this procedure to isolate the problem to a particular input or output function, a program loop may be initiated by setting test computer SWITCH REGISTER bit 1 and momentarily pressing the test computer CONTINUE button. Using the appropriate drawings in Volume II of this manual and Figure 4-1, the oscilloscope can now be used to isolate the problem to a single component, or at worst, to a few components on a module.

4 Repair should be accomplished using techniques described in Paragraph 4.3.

5 The test program should be run again after repairs have been made to make certain the fault has been corrected, before returning the module or the entire control unit to its operating station.

4.2.2 ROM Assembly Procedure

NOTE

The PDP-14 control unit used in conjunction with the following procedure must be capable of passing TEST-14.

Step	Procedure
1	Perform the VER-14 procedure described in Paragraph 2.3.3, Steps 1 through 20.
2	The error printouts associated with the error codes take the following basic forms:

a. SEQUENTIAL ADDRESS TEST

ADDR	GOOD	BAD
0470	7777	0000
0471	5777	0000
0472	7777	0000
0473	7777	0000
0474	7777	0000
0475	6777	0000
0476	7777	0000
0477	7777	0000

In this test, every address in the selected ROM assembly is read in sequence and the contents of each address is compared with the correct data held in the test computer. In the above printout, eight sequential addresses read from ROM (the "BAD" column) contain zeros. These addresses should contain the data shown in the GOOD column. The ROM matrix transistor

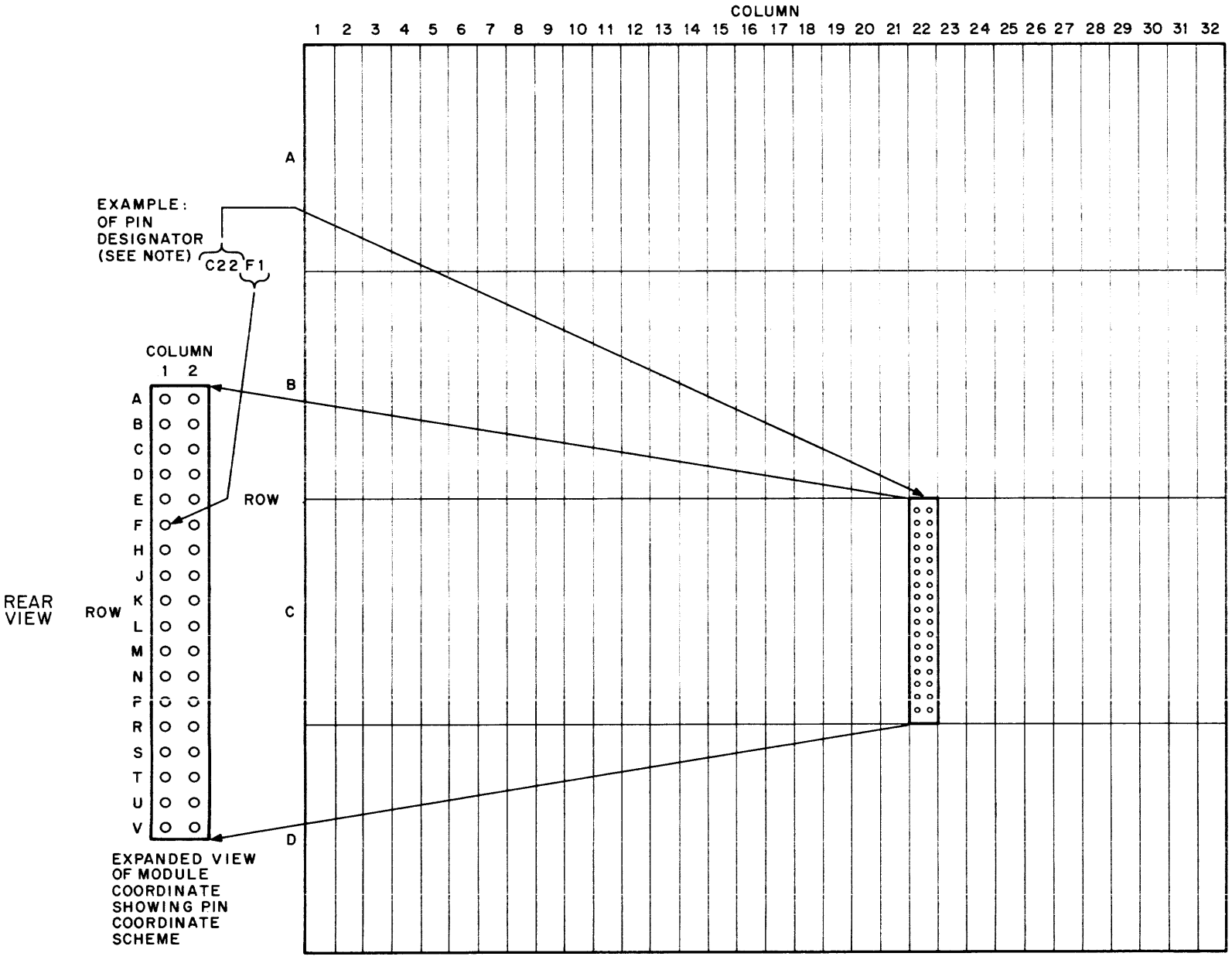


Figure 4-1 Control Unit Mainframe Wirewrap Panel, Rear View, Showing Pin Coordinate Scheme

Step	Procedure
2 (Cont)	associated with the most significant three octal address digits (047_) is suspected as it provides the read current for these eight addresses. If the error is unique, the problem is probably in ROM program. If the error occurs only every eighth word, and affects all bits of those words, the problem is probably in the decoder associated with the least significant bit of the address which selects the sense amplifier groups. If only one bit of every eighth word is faulty, a single sense amplifier is defective. If one bit of every word is affected, the problem is in the ROM data bus or ROM data register . If the fault is of a cyclical nature, occurring at regular intervals greater than every eighth word, the problem is in the matrix base select decoder or read current switch decoder, or one of the read current switches (see Figure 3-14). If all active address within a ROM read "BAD", the trouble may be in the timing circuits within the ROM or within the ROM selection circuit of the control unit (which decodes address bits 0 and 1). b. RANDOM ADDRESS TEST ADDR GOOD BAD 0061 7777 5777 0071 7777 5777 0101 7777 5777 0111 7777 5777 0121 7777 5777 0131 7777 5777 0141 2525 0525 0171 6666 4666 0261 7777 5777 0271 7777 5777 0361 7777 5777 The error indicated in the above example affects data bit 1 as read from the ROM and is therefore a ROM sense amplifier problem. Program looping cannot be set up for random address-tests, this test is for sense amplifier noise immunity and the problem area is defined by the printout. c. PDP-14 HUNG PDP-14 STOPPED Assuming the control unit circuits to be functioning properly, these VER-14 printouts can only be caused by a timing malfunction in the selected ROM assembly.
3	A sequential error will automatically place VER-14 in a program loop. Using the appropriate drawings in Volume II of this manual and Figure 3-15 (ROM Timing), an oscilloscope can be used to isolate the problem to a single component, or at worst, to a few components on a module.
4	Repair should be accomplished using techniques described in Paragraph 4.3.
5	VER-14 should be run again after repairs have been made to ensure that the fault has been corrected, before returning the ROM assembly or the entire control unit to its operating station.

4.2.3 Accessory Box Procedure

Step	Procedure
1	Perform the ABE-14 procedure described in Paragraph 2.3.6, Steps 1 through 18.
2	The error printouts associated with the error codes take the following basic forms:

a. `OUTPUT XXXX SET ON IN ABOUT YYYY MILLISECONDS`

Although this is not strictly an error output, it can be used to determine if the timer specified by address xxxx changes state in the corrected period of time. The actual delay (~±10%) is indicated by yyyy in milliseconds.

If it is desired to adjust a particular time delay, set switch register bit 3 on the test computer before the program completes the printout for the timer. The program will now loop, permitting the time adjust screw (Trimpot clear handle) on the timer module in the accessory box to be adjusted as required as the program types out the new times.

b. `**CH** TIME OUT ERROR OUTPUT XXXX.`

If the timer specified by address xxxx does not change state in approximately 61.5 seconds, this error code is generated by ABE-14. (Under special conditions, the correct delay may in fact be longer than this.)

c.
```
**BX** TEST FLOP NOT SET BY TYN XXXX
**BQ** TEST FLOP SET BY TYN XXXX
**BN** STATUS ERROR TYD XXXX
**BL** TEST FLOP NOT SET BY TYF XXXX
**BY** TEST FLOP SET BY TYF XXXX
```

All of these codes describe an incorrect test flop response to the state of the accessory box function identified by XXXX.

d.
```
**CB** OUTPUT XXXX NOT TURNED OFF BY SYF
**CB** OUTPUT XXXX TURNED OFF BY SYF
```

The accessory box function identified by XXXX has not responded correctly to the SYF instruction.

e.
```
**CF** ZERO LOST IN POWER SHUT-DOWN BY RM XXXX
**CG** ONE LOST IN POWER SHUT-DOWN BY RM XXXX
```

The retentive memory (RM) module specified by octal address XXXX has failed to function properly.

f.
```
PDP-14 HUNG
PDP-14 STOPPED
```

These errors should not occur if TEST-14 can be run successfully.

Step	Procedure
3	After using the information presented in Step 2 of this procedure to isolate the problem to a particular accessory box module (see Table 2-5 and Figure 2-6), a program loop may be initiated by setting the test computer SWITCH REGISTER bit 1 and momentarily pressing the test computer CONTINUE button. Using a module extender, an oscilloscope can now be used to isolate the problem to a single component, or, at worst, to a few components on the module.
4	Repair should be accomplished using techniques described in Paragraph 4.3.
5	ABE-14 should be run again after repairs have been made to make certain the fault has been corrected before returning the module or the entire control unit to its operating station.

4.2.4 Hints and Kinks

The following paragraphs may help isolate many problems, particularly those in which the test software cannot be used.

If TEST-14 prints "PDP-14 HUNG", the trouble is probably due to the loss of a timing pulse. If this occurs, shut down power and remove ROM modules, shut down external computer, and then turn PDP-14 power on. Observe the fetch/execute flip-flop to determine if the PDP-14 is running. The PDP-14 should execute NOPs (no operation). Execution of NOP exercises all basic timing except Input/Output, IOT, JMS, and TRM instructions.

If basic timing cannot be observed, substitute the M741 module. If timing still cannot be observed, substitute the M742 module.

If some or all input or output instructions fail, input/output timing may be at fault. In this case substitute the M741 module. If this does not correct the problem, substitute the M743 module.

If the PDP-14 is capable of executing NOPs but some instructions are not executed, the instruction decoder may not be functioning properly. Replace the M740 module.

If a JFF or JFN failure occurs, replace: 1) M740; 2) the MB register modules; and, finally 3) PC1 modules.

If the external computer accumulator contains 0600_8, determine that PDP-14 timing is functioning.

If TEST-14 will not run, substitute first the M741 module. If TEST-14 still will not run, substitute the M740 module.

If TEST-14 prints "PDP-14 HUNG" when executing a Skip-On-Run instruction, substitute the M742 module in the PDP-14.

If the PDP-14 functions correctly when operating independently, but malfunctions when interfaced with an external computer, replace the M745 module in the PDP-14.

4.3 MODULE REPAIR TECHNIQUES

When soldering semiconductor devices (transistors, diodes, rectifiers, or integrated circuits) which may be damaged by heat, physical shock, or excessive electrical current, take the following special precautions:

a. Use a heat sink, such as a pair of pliers to grip the lead between the joint and device being soldered.

b. Use a 6V iron with an isolation transformer. Use the smallest iron adequate for the work. Use of an iron without an isolation transformer may result in excessive voltages presented at the iron tip.

c. Perform the soldering operation in the shortest possible time to prevent damage to the component and delamination of the module etched wiring.

d. ICs may be easily removed by using a solder-sucker to remove all excessive solder from contacts and then, by straightening the leads, lifting the IC from its terminal points. If it is not desirable to save the defective IC for test purposes, then the terminals may be cut at the IC body and each terminal removed from the board individually.

CAUTION

Never attempt to remove solder from terminal points by heating and rapping module against another surface. This practice can result in module or component damage. Always remove solder by the use of a solder-sucking tool.

When removing any part of the equipment for repair and replacement, make sure that all leads or wires which are unsoldered or otherwise disconnected are legibly tagged or marked for identification with their respective terminals. Replace defective component only with parts of equal or better quality and equal tolerance.

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or device lines. When repair has been completed, remove all excess flux by washing junctions with a solvent such as trichlorethylene. Be very careful not to expose painted or plastic surfaces to this solvent.