INSTRUCTION MANUAL

TYPE 164
MAGNETIC CORE
MEMORY SYSTEM

PDP-6

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

DEC-06-H1BA-D

TYPE 164 MAGNETIC CORE MEMORY SYSTEM

INSTRUCTION MANUAL

December 1967

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

CONTENTS

CONTENTS (cont)

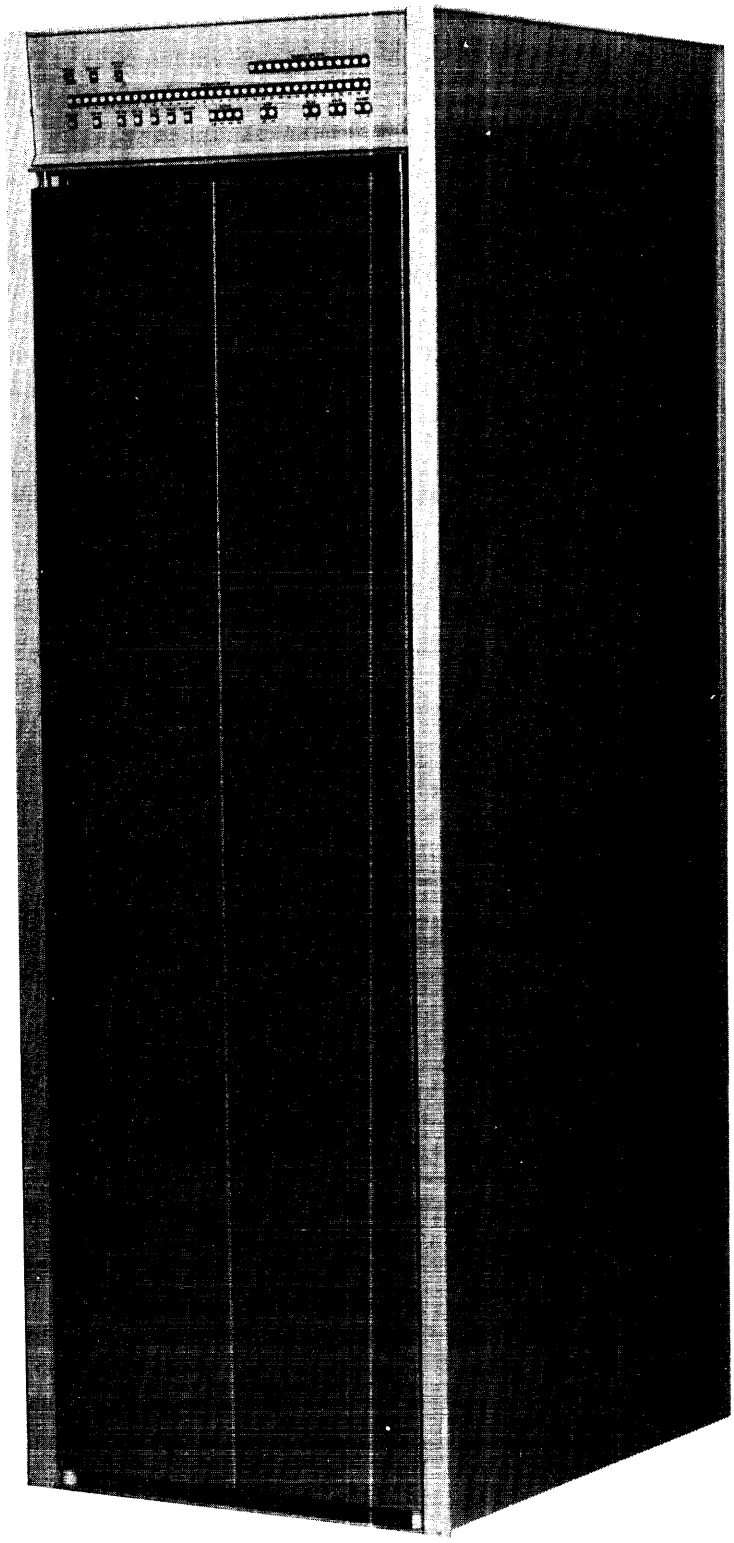
CHAPTER 4
SPECIAL MEMORY MODULES

CHAPTER 5
MAINTENANCE

ILLUSTRATIONS (cont)

TABLES

TYPE 164 MAGNETIC CORE MEMORY SYSTEM



Type 164 Magnetic Core Memory System

CHAPTER 1
INTRODUCTION AND DESCRIPTION

Type 164 Magnetic Core Memory System (Frontispiece), manufactured by Digital Equipment Corporation, stores standard PDP-6* 36-bit words, and can accommodate a parity bit if required. This memory performs with either a single- or multiple-processor configuration. In addition, a system configuration can incorporate several of these memories. A single memory can accommodate up to four processors and includes priority logic to control processor access. All memories for use with a single processor are connected to the processor-memory bus, and each memory can be connected through to as many as four processor-memory buses. The standard Type 164 Memory stores 16,384 words.

1.1 PURPOSE AND SCOPE

This manual provides initial instruction in the use of the Type 164 Memory System. Information suitable for maintenance of the system sufficient for use by personnel with experience in servicing similar types of equipment also is included.

This document is one of several associated with the PDP-6 computer. For complete and comprehensive coverage of areas not included in this manual, the operator should refer to the list of documents under Paragraph 1.3.

1.2 SYSTEM REQUIREMENTS AND CHARACTERISTICS

Table 1-1 lists the system requirements.

Table 1-1
System Requirements

Access time from processor	Single processor 850 ns ± 50 Multiple processors 950 ns ± 50
Total cycle time of memory	1.65 μs
Input ac voltage	105-125 at 60 c/s 220-250 at 50 c/s
Current	Nominal 11A Surge 16A
Power dissipation	995W
VA	1265

*PDP is a registered trademark of Digital Equipment Corporation

Table 1-1 (cont)
System Requirements

Heat dissipation	3396 Btu/hr
Temperature range (Operating)	70° to 85° F
Humidity range	30% to 80%

1.2.1 Access Time

Total cycle time for the core memory is 1.65 μs, but this time is not a factor in system operating speed unless calls to the same memory are so frequent that processor time is lost in waiting, in which case memories should be interleaved. The total time required for access by the processor is of importance when considering system operating speed. This time is dependent both on the speed of the memory and the time required by the memory subroutine in the processor. In Table 1-2, all times are in nanoseconds. The time in memory is the actual time consumed within the memory for read access and write access (the time from the appearance of the request signal at the memory until acknowledgement or the read restart is generated). (See Chapter 4.) The access time is the total access time for the Arithmetic Processor Type 166 and is the interval between the pulse which requests memory access subroutine and the return pulse which restarts the waiting sequence. The times are given below for a call without relocation or stopping on parity errors, with a bus length of 10 ft. For each additional foot of cable, add 3 ns; when a core address is relocated, an additional 100 ns is required; for parity checking with error stop, add 100 ns to the read-access time for core.

Table 1-2
Access Times

	Time in Memory (ns)	Type 166 (Exec Mode) Access Time (ns)
Core Memory		
Read access	Single processor 500±50 Multiple processors 600±50	Single processor 850±50 Multiple processors 950±50
Write access	Single processor 100±50 Multiple processors 200±50	Single processor 500±50 Multiple processor 550±50

NOTE: Add 150 ns to read and write access time when Type 166 Arithmetic Processor is in the user mode.

For read/write access, the time required for the first memory call is the time given for read. No time is required within the memory for the second call because it is already waiting for data and the write restart, and no response is expected of it. (See Chapter 4.) The time required for the call in the processor is the time required to send the restart and terminate the subroutine.

1.2.2 Physical Description

The Type 164 Memory System is housed in a single standard 19-in. DEC cabinet. Figure 1-1 shows the major equipment layout within the cabinet, and Table 1-3 presents the major physical characteristics. Inside the doors at the rear of the rack is an inner plenum door on which are mounted the required power supplies and power control panels.

Table 1-3
Physical Characteristics

Dimensions	
Width:	22-1/4 in.
Depth:	27-1/16 in.
Height:	69-1/8 in.
Service Clearance	
Front:	8-3/4 in.
Rear:	14-7/8 in.
Weight	
	560 lb

The figures listed in Table 1-3 are for memories that stand alone. Whenever a memory is added to a frame containing either a processor or another memory, the width is decreased by 2 in. Clearance required for the double doors is 9 in., and for the rear plenum doors, 15 in.

Intake fans at the middle protion of the rack cool the top and bottom logic modules by blowing filtered air between them. Additional fans mounted on the plenum door cool ambient temperature of the bay.

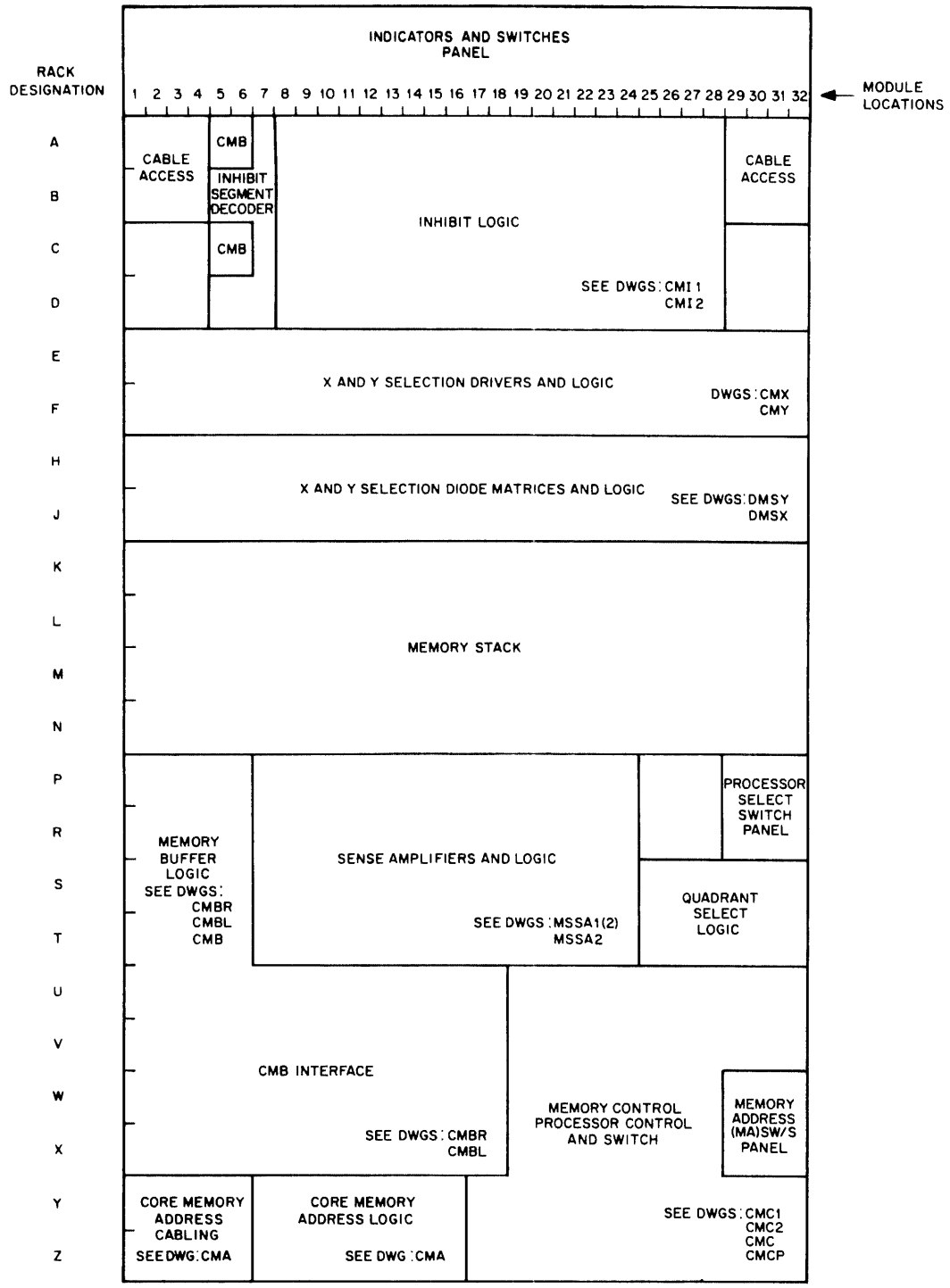


Figure 1-1 Type 164 Memory System, Equipment Layout

1.3 REFERENCE DOCUMENTS

The listing of Table 1-4 itemizes the standard documentation provided for use with the PDP-6 system. Other documents may be furnished if they are applicable to customer requirements.

Table 1-4
Hardware and Software Documentation

Central Processor Type 166 Maintenance Manual, F67	Instruction and servicing information.
PDP-6 Users Handbook, F65	Programmers manual for PDP-6 system.
Module Catalog, C105	Complete data concerning modules and module circuits used in the PDP-6 system.
PDP-6 Program Library	Detailed description, listings and tapes.
PDP-6 Software Documents	Includes software system manuals such as FORTRAN, DDT debugging, etc.

1.4 REFERENCE CONVENTIONS

The Digital Equipment Corporation engineering drawing conventions and instruction manual referencing should be understood at this point. A study of the reference conventions in this paragraph and Chapter 6 will save considerable time and preserve thought continuity while reading the text that follows. Any reference to figure numbers or table numbers indicates that the illustration or table is located in text. For example, Figure 3-1 is located Chapter 3 and is the first illustration in that Chapter.

All engineering drawings have a full drawing number. These drawings are included in Chapter 6. In text, references to engineering drawings are abbreviated. For example:

Full drawing no. D-164-0-SBD

- D — Drawing original size
- 164-0 — Drawing set identifier and no. in set
- SBD — Mnemonic identifier

For this number, the first reference in text is 164-0-SBD; all subsequent references are -SBD.

To locate a specific signal or function, the origin of the signal on a specific drawing is stated in one of two conventions.

1. "The OGN pulse developed at PA (D23, SBD)..., where PA is the module type."
   D23 is the physical location of the module by rack and module slot, and
   SBD is the specific drawing on which the reference can be found.
2. "The CLR pulse is generated at module PA (SBD:C4)..., where PA is module type."
   SBD is the drawing, and
   C4 is the coordinate location on the drawing for the module.

CHAPTER 2
INSTALLATION AND INDICATORS

2.1 SYSTEM CABLING

2.1.1 Power Cabling

The standard power cables supplied with the 164 Memory System are 25 ft long and 11/16 in. in diameter and permanently wired to the unit. These cables have a Hubbel Twist-loc plug number 34-3331, rated at 115V, 30A. Thus, the primary power source must have a 115V, 30A Hubbel Twist-loc flush receptable part number 34-3333 or equivalent.

2.1.2 Bus Cable Requirements

The central processor and memory system are interconnected by eight 9-conductor coaxial cables. Four of these have two DEC 10350 female connectors (two 9-conductor cables per 10350) on one end, and four DEC W028 connectors on the other as shown on Dwg. D-164-0-CCD, sheet 1. The other four cables have DEC 10360 male connectors at one end and four DEC W028 connectors on the other end of each cable, as shown on Dwg. D-164-0-CCD, sheet 2.

The signals transmitted over these cables are listed in Table 2-1.

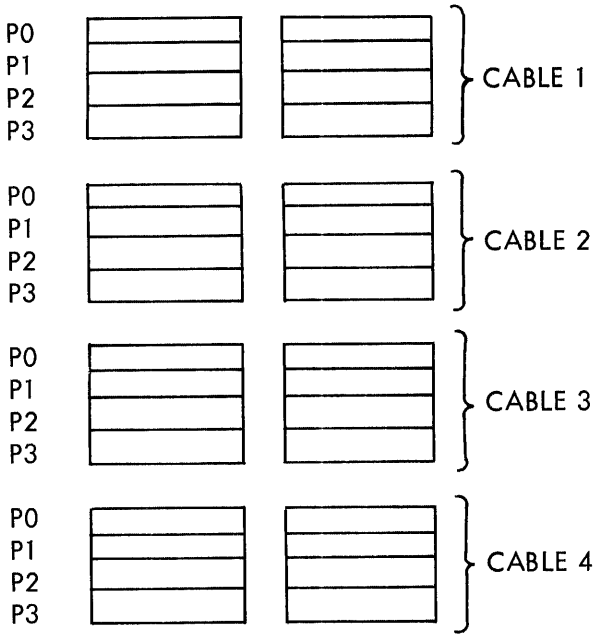
Table 2-1
PDP-6 Memory Bus Interface

PDP-6 PROCESSOR END					164 Memory End	
Pin	DEC 10360 Memory Cable No. 1	DEC 10360 Memory Cable No. 2	DEC 10350 Memory Cable No. 3	DEC 10350 Memory Cable No. 4	DEC * W028 Pin No.	
A	Gnd	Gnd	Gnd	Gnd		
B	ADDR ACK →	MA 22 (1) ◆→	MB 0 (1) →	MB 18 (1) →	D	
C	RD RS →	MA 23 (1) ◆→	MB 1 (1) →	MB 19 (1) →	E	
D	WR RS →	MA 24 (1) ◆→	MB 2 (1) →	MB 20 (1) →	H	
E	PAR (1) →	MA 25 (1) ◆→	MB 3 (1) →	MB 21 (1) →	K	First
F	RQ CYCLE ◆→	MA 26 (1) ◆→	MB 4 (1) →	MB 22 (1) →	M	W028
H	Spare	MA 27 (1) ◆→	MB 5 (1) →	MB 23 (1) →	P	Connector
J	Gnd	Gnd	Gnd	Gnd		
K	MA 18 (1) ◇→	MA 28 (1) ◆→	MB 6 (1) →	MB 24 (1) →	S	
L	MA 18 (0) ◇→	MA 29 (1) ◆→	MB 7 (1) →	MB 25 (1) →	T	
M	MA 19 (1) ◇→	MA 30 (1) ◆→	MB 8 (1) →	MB 26 (1) →	V	

Table 2-1 (cont)
PDP-6 Memory Bus Interface

PDP-6 PROCESSOR END					164 Memory End	
Pin	DEC 10360 Memory Cable No. 1	DEC 10360 Memory Cable No. 2	DEC 10350 Memory Cable No. 3	DEC 10350 Memory Cable No. 4	DEC * W028 Pin No.	
N	MA 19 (0) ◇—	MA 31 (1) ◆—	MB 9 (1) →	MB 27 (1) →	D	
P	MA 20 (1) ◇—	MA 32 (1) ◆—	MB 10 (1) →	MB 28 (1) →	E	
R	MA 20 (0) ◇—	MA 33 (1) ◆—	MB 11 (1) →	MB 29 (1) →	H	
S	Gnd	Gnd	Gnd	Gnd		Second W028 Connector
T	MA 21 (1) ◇—	MA 34 (1) ◆—	MB 12 (1) →	MB 30 (1) →	K	
U	MA 21 (0)	MA 35 (1) ◆—	MB 13 (1) →	MB 31 (1) →	M	
V	MA 22 (1)	MC RD RQ ◆—	MB 14 (1) →	MB 32 (1) →	P	
W	MA 22 (0)	MC WR RQ ◆—	MB 15 (1) →	MB 33 (1) →	S	
X	MA 22-	Spare	MB 16 (1) →	MB 34 (1) →	T	
Y	31=0 ◇—	Spare	MB 17 (1) →	MB 35 (1) →	V	
Z	Gnd	Gnd	Gnd	Gnd		

(SOURCE 2L5) (SOURCE 2L20) (SOURCE 2E25) (SOURCE 2J25)



*NOTE: Each DEC 10350 and DEC 10360 connector and cable is terminated to two DEC W028 connectors. (Refer to BUS CABLE REQUIREMENTS Paragraph 2.1.2.)

2.1.3 Inter-Memory Cabling

Interconnection between Type 164 Memory to another Type 164 Memory is accomplished by eight 9-conductor coaxial cables with DEC W028 connectors on each end.

2.1.4 Margin Check and Remote Power Cable

Each system is supplied with a margin check and remote power turn-on cable which plugs into the power connector bracket between the Type 164 Memory and processors. (See Dwg. IA-B-7405423-0-0).

2.1.5 Termination Requirements

Each 164 Memory System on the end of a bus should be supplied with eight DEC W028 connectors with handles. These should be ordered separately. Each W028 will have nine 100 ohms, 1/4W, 5% or 10% wired-in terminators to ground. (Refer to Dwg. IA-B-5403930-0-0.)

2.1.6 Pressurized Cabinets

A 164 Memory System which is to be connected mechanically to a unit that contains system type modules, must have a side panel installed so that pressurization can be maintained in the unit with system modules. Cable access through the side panel is 8 in. x 4 in. These side panels are not necessary when two Type 164 Memories are connected together. These panels should be ordered separately (Part No. 74-05415 and Dwg. D-MD-7405415-0-0).

2.1.7 Cable Access

If the Type 164 Memory is remotely located, cable access is through the bottom of the cabinet.

If the Type 164 Memory is connected mechanically to another Type 164 unit or non-system type module unit, cable access is through the side or bottom of the cabinet.

If the Type 164 Memory is connected mechanically to a system type module unit, cable access is through the side panel as explained under pressurized cabinets.

2.1.8 Cooling

All modules will have styrofoam strips 1/8 in. x 2-1/4 in. x 16 in. between handles. These must remain in place to insure that modules are not damaged by excessive heat.

2.1.9 Multiprocessor Input Module Requirement

10 each - W102 per additional processor input

1 each - B684 per additional processor input

8 each - W028 (cable terminator) per additional processor input if Type 164 Memory unit is at the end of the bus.

2.2 INDICATOR PANEL AND SWITCHES

The indicator panel (Figure 2-1) contains the POWER, RESTART, and SINGLE STEP switches and register flip-flop indicator lights that illustrate system conditions for memory address and memory buffer plus control conditions.

A processor selection switch and restart switch are mounted on the rack as shown in Figure 2-2. Table 2-2 lists the system switches and functions.

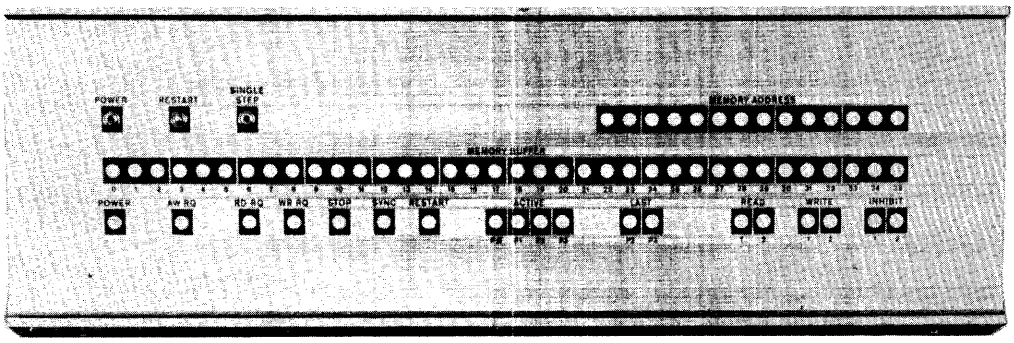


Figure 2-1 The Indicator Panel

Table 2-2
System Controls

Switch	Location	Function
POWER	Indicator Panel	Primary power for memory
RESTART	Indicator Panel	To restart memory cycle manually
SINGLE STEP	Indicator Panel	Allows one-step operation for maintenance under control of RESTART switch
PROCESSOR SELECTION	S6 Front of Cabinet	Manual selection of a single processor or multi-processor operation
RESTART	S5 Front of Cabinet	Manual restart

Table 2-2 (cont)
System Controls

Switch	Location	Function
SEL/DES PO	S23 Front of Cabinet	Manual selection or deselection of individual processors
SEL/DES P1	S24 Front of Cabinet	
SEL/DES P2	S25 Front of Cabinet	
SEL/DES P3	S26 Front of Cabinet	
PO NORM/INTL	S1 Front of Cabinet	Select normal or interleaving memory operation (more than one) (Type 164 Memory)
P1 NORM/INTL	S2 Front of Cabinet	
P2 NORM/INTL	S3 Front of Cabinet	
P3 NORM/INTL	S4 Front of Cabinet	
MA 18 0-1 P0, P1, P2, P3	S7, S8, S9, S10	Select code
MA 19 0-1 P0, P1, P2, P3	S11, S12, S13, S14	
MA 20 0-1 P0, P1, P2, P3	S15, S16, S17, S18	
MA 21 0-1 P0, P1, P2, P3	S19, S20, S21, S22	

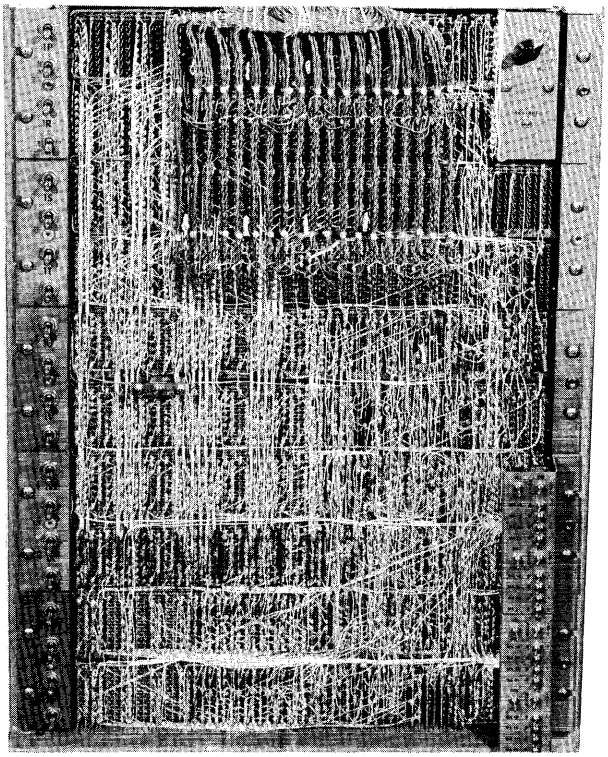


Figure 2-2 System Switches

2.3 OPERATION

A standard panel (Figure 2-1) is installed on all memories, although some of the indicators may not be used. The controls and indicators are primarily for maintenance; most of the lights change too rapidly to be significant when the computer is running normally. On the upper left of the panel are two toggles and a pushbutton. Memory power can come on only when the POWER switch is up, so this switch is usually left on at all times so that the memory comes on when power is applied to the computer system. The POWER light at the lower left turns on immediately when power is applied. If the SINGLE STEP switch is up, the memory stops with the STOP light on at the end of every cycle; it can be restarted by pressing the RESTART button.

Following a stop, the memory appears to the processor to be nonexistent when the next access is requested. Therefore, to use single-step mode at the memory, the operator should latch on the MEMORY STOP key at the processor console so that he may single-step the processor by memory subroutine-calls or turn on the DISABLE MEMORY switch so that the processor stops whenever the memory does not respond to a request for access. If a malfunction causes the memory to hang up with the STOP light off, it can be restarted by pressing RESTART while holding on the stop override button. This button is located behind the double doors on the front of the bay.

2.3.1 Core Memory Indicators

If the AW RQ light on a core memory remains on while the computer is running, the particular memory is not currently in use. One of the LAST lights may also stay on during operation. This light indicates which of processors 2 and 3 was the last to have access. The remaining indicators display useful information only when the memory has stopped (during maintenance procedures) or the computer has stopped. MEMORY ADDRESS indicates the location within the memory to which the last access was made; MEMORY BUFFER displays the word read or written, but all the lights are off following the read portion of a read-write cycle. When a memory cycle starts, the AW RQ light goes off, and one of the four ACTIVE lights goes on, indicating which processor gained access. The RD RQ and WR RQ lights indicate whether there is a read request, a write request, or both. At the end of the read portion of the memory cycle, the SYNC light goes on, and if new data is to be written, the RESTART light goes on when the processor sends the write restart. The READ, WRITE, and INHIBIT lights represent the drive currents applied to the cores, and they can be on at the completion of a cycle only if a malfunction occurs.

If the memory is stopped independently of the processor, the ACTIVE lights will be out, STOP will be on, and the remaining lights will reflect the cycle just performed. On an instruction stop, or the stop following an examine or deposit from the processor console, the AW RQ light will be on, indicating that the memory is free and awaiting a request; ACTIVE will be off; and the other lights will reflect last

cycle. On a memory stop at the processor (i.e., a stop following the completion of a memory subroutine), the lights reflect the type of stop. If the stop follows the read part of a read/write access, the memory is at the middle of its cycle, so AW RQ will be off; one of the ACTIVE lights will be on; and RESTART will not yet be on. For any other type of memory stop, the lights are the same as for an instruction stop.

The remaining controls are located behind the double doors. The operator selects normal or interleave operation by using the toggle switch mounted on a bracket and listed in Table 2-2. In normal operation, the switch is in the NC position and the memory responds to a block of 16K consecutive addresses. To interleave the locations in a pair of memories, are interleaved, the MEMORY ADDRESS lights still indicate the internal location to which access was made. Bit 35 at the memory now corresponds to bit 21 at the processor, and processor bit 35 determines memory module selection. This exchange must be considered when working with the memories from the processor console.

Power supplies are mounted on the rack plenum door. The red light on the power supply is on whenever the ac line is plugged in. Beside the light are the ac circuit berakers.

Switching S1 to LOCAL turns on memory power; with the switch in REMOTE, memory power goes on and off with system power which is controlled from the control panel POWER switch.

CHAPTER 3
SYSTEM DESCRIPTION

All core memories associated with a central processor are connected to the processor memory bus. Also, each memory can be connected to up to four memory buses (four processors). A core memory responds to a request for access over any associated processor memory bus and includes within its logic a priority network that determines which processor shall have access. In addition to standard 36-bit word storage, the core memory also accommodates a parity bit when the Type 169 Parity Option is installed.

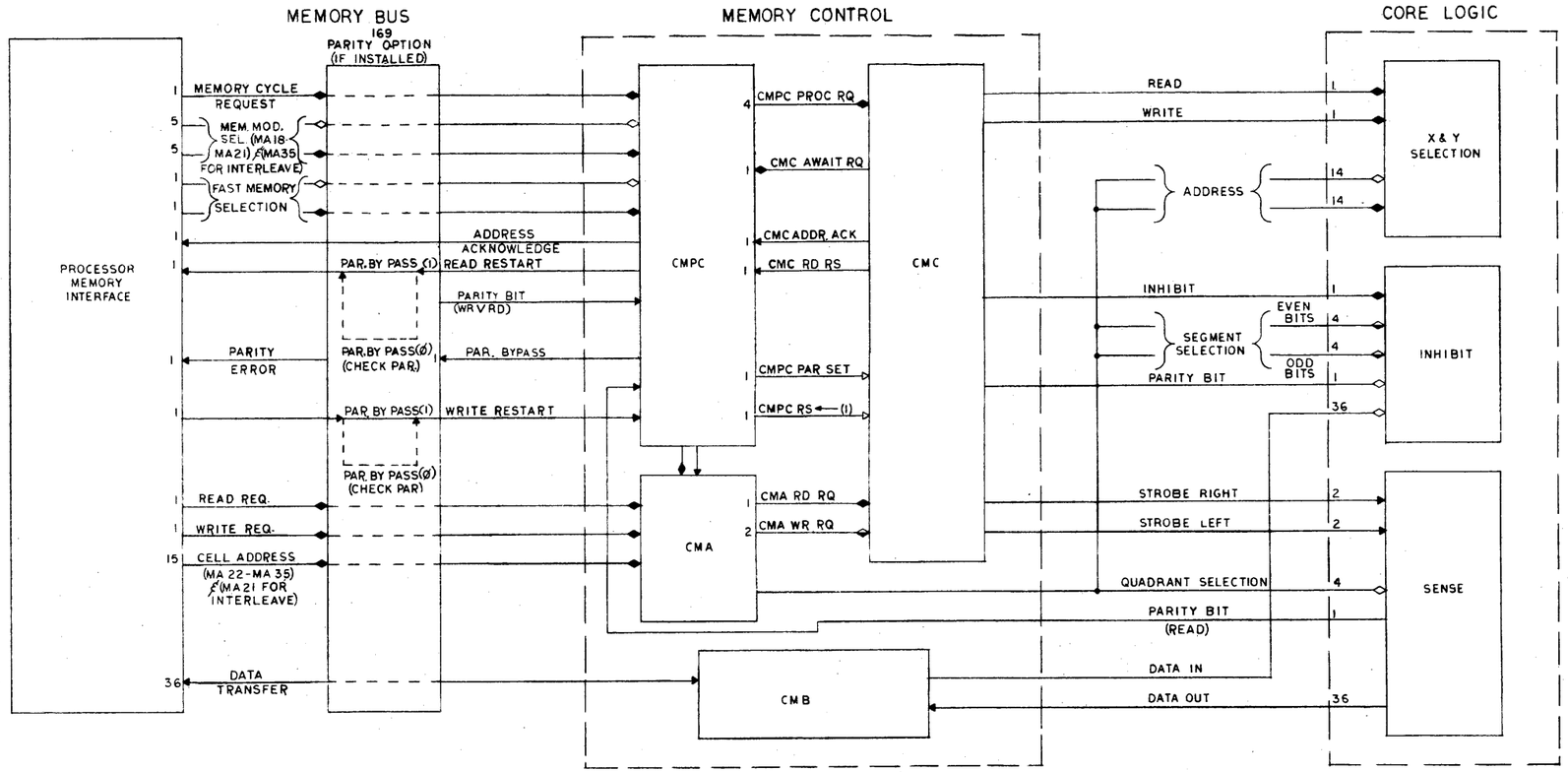
A processor may request three types of access to memory: read, in which the memory subroutine (in the processor) retrieves a word from memory; write, in which the subroutine sends a word to memory to be stored; read/pause/write, in which the processor combines two memory subroutine calls into one memory-access, the first to retrieve a word, the second to store a new one.

A single processor can select any location out of 262,144 using an 18-bit address. A 16K memory module is selected by the 4 MSBs of the address, and the remaining 14 bits select a location within that memory. The address of each memory is prewired within its interface with the memory bus.

In systems with added memory modules, interleaving memory addresses between two modules can be selected to reduce processor waiting time. The two core memories are n and n+1 where n is even. Consecutive addresses supplied by the processor switch access back and forth between modules. Interleaving is accomplished by throwing a switch that makes jumper changes in the module involved. These changes substitute address bit 35 for bit 21 in the selection of memory and substitute 21 for 35 in the address of a location within the selected memory. In the first 16K block, all even addresses address the even locations in the first memory, and all odd addresses address the even locations in the second module. In the second 16K block, all even addresses address odd locations in first module, and all odd addresses address odd locations in the second module. In this way, the processor cycles can overlap memory cycles; that is, after addressing the first module, the processor does not need to wait for completion of the memory cycle in module one and can go on to address the second module.

3.1 DISCUSSION OF SYSTEM BLOCK DIAGRAM

As shown in Figure 3-1, system block diagram, pulses transfer data between the processor(s) and memory over 36 data lines. (See Table 2-2.) With a parity option included, a pulse line carries the parity bit between the memory and the parity logic. The processor provides 14 levels (MA22-35) as the address and 2 levels as read and write request signals. Memory module selection and interleaving are selected by five level times, MA18-21 and MA35, respectively.



NOTE:
DOTTED LINES REPRESENT FUNCTIONAL SIGNALS
WITHIN THE 169 PARITY OPTION

Figure 3-1 System Block Diagram

In return to processor requests, the memory control logic provides an ADDRESS ACKNOWLEDGE pulse which initiates processor functions to execute the requested access (read or write).

For read access, the processor sends a READ REQ (request), and the memory control responds by sending an ADDRESS ACKNOWLEDGE pulse. Then data and a READ RESTART trigger completion of the access routine. For write access, the processor sends the WRITE REQUEST SIGNAL. When the memory controls return ADDRESS ACKNOWLEDGE, the processor sends data and a WRITE RESTART pulse to memory control. For read/write access, the processor sends both READ and WRITE requests at the beginning of the first memory subroutine. After acknowledgment, data and READ RESTART trigger completion of the read portion of the access, then the WRITE RESTART is generated at the processor to complete the write portion of the cycle. In the memory, the cycle stops after completing the read part to await the WRITE RESTART and new data (READ/PAUSE/WRITE).

The memory control section sends the acknowledge signal and, simultaneously, loads the address and request signals from the selected bus into the address register (CMA) and read and write request flip-flops. The outputs of CMA are applied to the core logic to select the proper address in the core stack. In read access, the processor waits during the read portion of the memory cycle until the memory strobes the sense-amplifier outputs, sending data into the CMB and over the bus. For read access, data is retained in the CMB.

After returning the READ RESTART and disconnecting itself from the bus (so that the processor can use another memory), the active memory completes its cycle, writing the word in CMB back into the same location. For write access, acknowledgment causes the processor to send the WRITE RESTART and data immediately. Memory control gates the data into CMB and disconnects from the bus. The memory then performs its complete cycle, first readingto clear the location and then writing the CMB information into it. For read/write access, the memory begins by performing the same function as in read access. The processor completes its first memory subroutine upon receiving the data, but the memory does not disconnect; instead it completes only the read portion of its cycle, and then pauses with a gate open to allow data from the bus into CMB. When the processor makes the second call, it sends the data and the write restart. The memory then disconnects and continues with the write portion of its cycle, writing the new data into the cleared location.

The processor selection portion (CMPC) of memory control decodes bits 18 through 21 to determine when this memory is being addressed. For interleave operation, bit 21 is substituted for 35 at CMA and 35 for 21 in CMPC. In addition, the CMPC receives signals from S6, the processor selection switch for manual selection of up to four processors, P0, P1, P2 or P3, and for automatic operation of all four processors through the MULTI position of S6.

To select a single location within the stack, CMA provides a 14-bit address; two 7-bit halves are decoded separately to select individual X- and Y-windings.

The stack is also divided into four quadrants with four sense windings per plane (every X- and Y-winding crosses two quadrants). The most significant bits for both halves of the address (bits 22 and 29) determine which quadrant (Q0, 1, 2, 3) contains the addressed location. Sense amplifiers detect the sense windings from only the selected quadrant. Separate strobe pulses are applied to sense amplifiers for load reasons and due to the characteristics of the stack, the strobe for bits 9 through 17 and 18 through 26 is delayed 20 ns as compared to bits 0 through 8 and 27 through 35. The delaying process is achieved by the addition of two inverters.

WRITE and 14 ADDRESS bits (7 bits for X and 7 for Y) accomplish X- and Y-selection for data input to the core stack. INHIBIT and four lines of SEGMENT SELECTION provide the current for switching the cores of the selected address in accordance with the 36 data inputs.

3.1.1 Central Processor/Memory Interface

Up to four CPs can address a single memory module and/or a single CP can address up to four memory modules. Within a memory module, the CMC logic contains a priority system to control multiprocessor access to the memory. The processor sends bits 18 through 21 and ~ FM as the code for a module, and each module recognizes its own code.

In the processor, the interface that connects with the memory bus includes:

Memory address register (MA)
Memory buffer (MB)
User mode registers (PR and RLR)
Memory indicator register (MI)
Control logic for the memory subroutine.

Flow and control for the memory subroutine for the processor is shown in Dwg. FD-D-167-0-FD contained in the Type 166 Central Processor Maintenance Manual.

3.1.2 Memory Control (Prints CMPC, CMC1, CMC2 (1 of 2), CMA, CMB, CMBR)

The basic memory control scheme is shown in Figure 3-2 and consists of the major logic elements as follows.

Processor control logic (CMPC)
Memory control logic (CMC)
Memory address logic (CMA)
Memory buffer logic (CMB).

The CMPC logic receives from the processor MA bits 18, 19 and 20 which carry the code of the processor requesting access, and bits 21 and 35 for interleaving. The processor priority logic provides a processor request signal (P0RQ, P1RQ, etc.) to set the proper flip-flop in the CMC logic. These flip-flops and/or settings of a processor selection switch initiate address acknowledge and read restart signals to the processor, and control gating of memory address bits to the X- and Y-selection inhibit and sense logic.

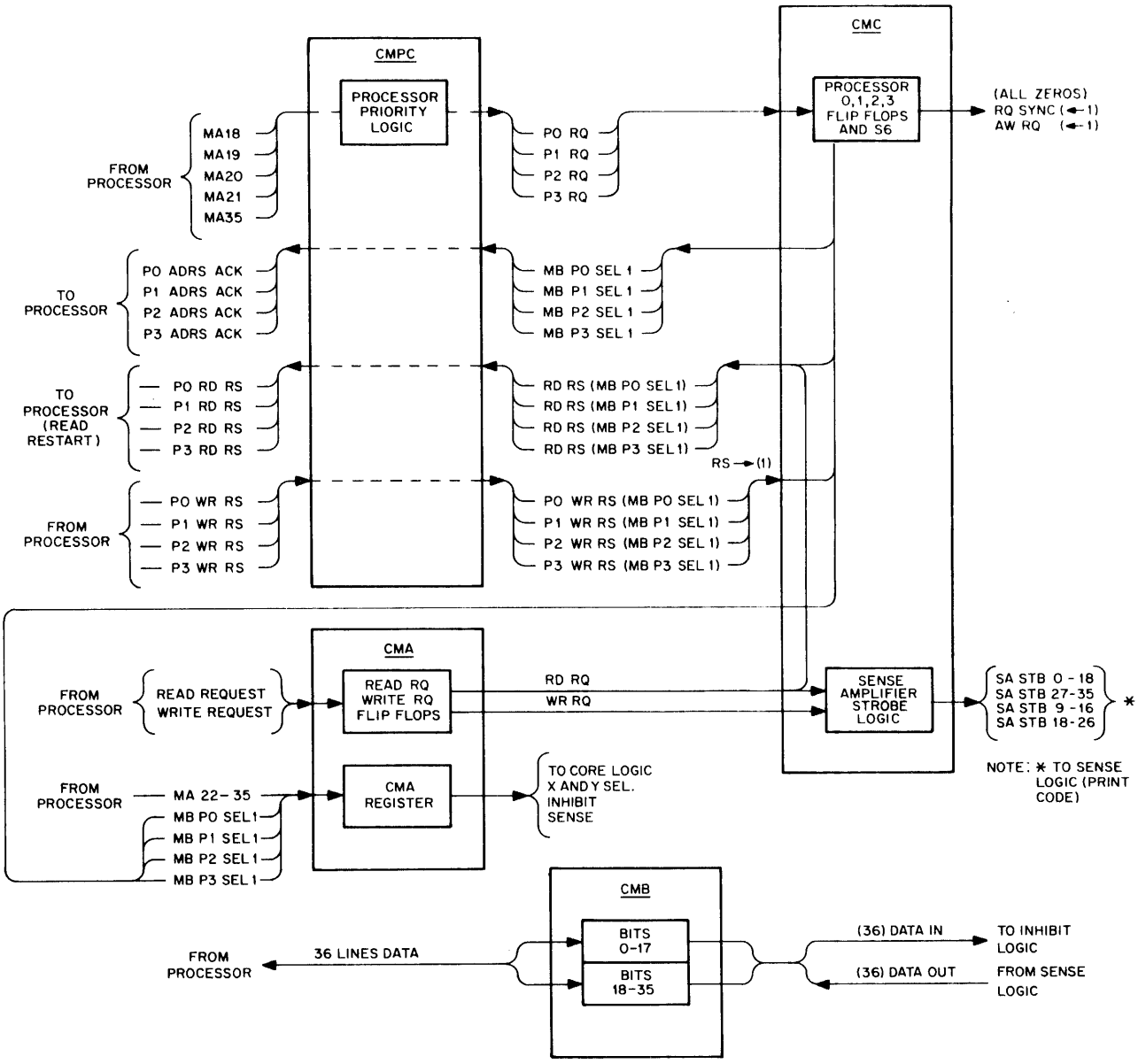


Figure 3-2 Memory Control Block Diagram

The CMA receives read and write request signals to drive the sense amplifier strobe logic in the CMA logic. The outputs of this logic provide strobe signals for all word bits 0 through 35 plus parity for the sense logic.

The CMB logic receives 36 data lines from the processor bus for execution of a write command and 36 bits from the sense logic for execution of a read command as indicated earlier.

In CMB, information is strobed in from or out to only that bus which connects the processor selected by the processor priority logic in CMPC. Bits 22 through 35 are provided for normal mode. Interleaving is under switch control (S10 on CMPC logic) to substitute bit 21 for 35.

3.1.3 Detail Control Logic (Prints CMPC, CMC1, CMC2 (2 sheets), CMA, CMB, CMBR)

3.1.3.1 Data In and Out - The first three logic drawings for memory control show the 14-bit address register on BS-D-164-0-CMA and the 36-bit data buffer on BS-D-164-0-CMBR and CMBL. On all three drawings, input connections from all four possible processor/memory buses are shown. Data is strobed in from or out to only the processor/memory bus that is selected by the memory control logic; that is, either CMC P0, P1, P2 or P3 SEL.

The read and write request flip-flops are shown on CMA location B7, 8. Either or both of these control flip-flops is set at the beginning of the memory cycle by the READ REQUEST or WRITE REQUEST signal from the processor. The flip-flop output enables gates for sensing, clearing CMB, and starting the write portion of read access. The MA PO SEL, etc., signals are enabled by manual selection at S6 on Dwg. CMC2 (Sheet 2), or by the active flip-flop in multiprocessor mode.

CMBR and CMBL show the left and right halves of the core memory buffer CMB. The (CMC) CMB CLR pulse is generated at the beginning of every cycle by T1B. T1B was generated by RQ SYNC flip-flop set state which is controlled by T0 pulse, generated by any processor request for access and CMC SP (single processor mode), or by CMC RQ SYNC (⟶ 1) (for multiprocessor mode) on Dwg. CMC2 (Sheet 1).

CMB CLR is also generated again in the same cycle of a READ/WRITE. This is done 300 ns after T2 along with the gating of READ and WRITE RQ on a (1). This will clear the CMB prior to sending of new data to be written into memory.

There are two logically equivalent gating levels for each processor/memory bus. One gates the output pulses from the core bank sense amplifiers onto the bus; the other gates pulses from the bus into the CMB register. In this structure and in a read access, pulses from the sense amplifiers at the first level of gating are applied to the bus and to the second level gating for regeneration of data. During write access, data from the bus passes through the second level gating into the CMB register . (Drawing CMB shows the buffers through which the CMB outputs are applied to the core logic (to sense and inhibit lines.)

3.1.3.2 Memory Access Control Logic - The sequence of events and timing of memory access is described in Paragraph 3.3 and Figure 3-11. Here, the memory access control logic is described. This logic is shown on Dwg. CMPC, CMC1, and CMC2 (Sheets 1 and 2).

Drawing CMPC shows the control connections between the memory and the processor/memory buses. The left-hand half of each bus connecting module (1W31, 1X31, 1Y31, 1Z31, etc.) determines whether the memory is being addressed by decoding address bits according to switch selected connections. For interleaving, bit 35 can be switch-selected to replace bit 21. These signals are ANDed with two

control inputs: the processor request signal (P0RQ, P1RQ, P2RQ or P3RQ) from the processor shown at the right center of the drawing; and the AWAIT RQ(1) from the await request flip-flop on Dwg. CMC2 (Sheet 1). The processor request signal initiates an access to memory, a CMC AW RQ(1) enables the gate to allow the CMPC PQ RQ, etc., whenever a processor request arrives over the bus.

The four processor request signals are ORed in 1V28 as shown on Dwg. CMC1 (Core Memory Control Timing) to provide T0 and thus trigger the time chain.

The four CMPC processor request signals are also applied to the processor selection logic on CMC2 (Sheet 2). They serve as set inputs to the processor active flip-flops (PQ ACT, etc.) to determine which processor will have access for the current memory cycle. During a cycle, only one active flip-flop is set and it generates a pair of selection levels (CMC MB PO SEL, etc.) that are inputs to the two-level gating structure on CMBR and CMBL, thereby controlling data transfers over the bus. These signals are also enabling inputs to control gating on the right-hand side of CMPC to control transfer of address acknowledge signals at T1 time (Figure 3-11, Timing Chart), read restart signals (CMC RD RS), and write restart signals from the memory and processor to the bus.

On Dwg. CMC2 (Sheet 2), the processor priority logic controls processor access. If P0 requests access (the highest priority), P0 ACT is set and the other three flip-flops are held reset. If no P0 request is present and P1 requests access, P1 ACT becomes set and P2 and P3 are held reset. This order does not hold true for the last two flip-flops; if it did, processor 3 might never gain access. To avoid this, the last processor flip-flop (LAST PROC) is connected to remember which of P2 or P3 had last access. (The gating is enabled by the T2 timing pulse.) Thus, whenever P2 and P3 request access simultaneously, and neither P0 or P1 request access, the current cycle is given to whichever processor has gone without access the longer time. This is accomplished because simultaneous access requests of P2 and P3 complement the flip-flop. The LAST PROC flip-flop outputs are each applied to a gate at the reset side of each flip-flop. The other input to these two gates are the set sides of the flip-flops (i.e., P3ACT (1) is applied to the gate at the reset input to P2 ACT flip-flop and the converse of this). Thus a P3 RQ and P2 LAST (1) resets P2 ACT and allows P3 access. Conversely, a P2 request and P3 LAST (1) allows P2 access.

If only one CMPC processor request signal is present, when the memory becomes free, the corresponding active flip-flop is set and all others are left clear. When there are conflicting requests, the nets below the flip-flops determine priority. Every processor requesting access tries to set its active flip-flop by grounding its unbuffered 1 output. But the highest priority flip-flop that is set grounds the 0 sides of the others. This situation becomes stablized when the first pulse in the timing chain T0 clears the AWAIT RQ flip-flop (1V30, CMC2 (Sheet 1)) negating all processor request signals so that the indeterminate flip-flops become clear. Thus only one flip-flop is set.

The flip-flop that remains 1 generates the selection levels which connect CMBR and L logic to the selected bus, and gates control signals shown at the right in CMPC. Thus the address acknowledge and the read restart are sent back to the selected processor, the write restart from that processor is received, and the address strobe jam pulse, generated by the timing chain, loads CMA from the selected bus.

If a priority option is installed on a bus, the parity bit in or out passes through the right-most circuit on CMPC. In reading, the parity sense amplifier signal accompanies the data out; in writing, the parity bit accompanies the delayed write restart following the data.

3.1.3.3 Control Flip-Flops - Figure 3-3 illustrates basic sequencing of control flip-flops shown on engineering drawings CMC1 and CMC2 (Sheets 1 and 2). The three flip-flops READ, WRITE, and INH control the read, write, and inhibit drivers in the core logic. All these flip-flops are initially cleared by PWR CLR.

The READ flip-flop is triggered by the T1A pulse from the timing chain. The control is arranged to reset READ 450 ns after T1A. INHIBIT is set by T3 and WRITE by T4; then, T5 resets all three and sets AWAIT REQUEST on Dwg. CMC2 (Sheet 1). At this time, the memory becomes again free. READ (1) is on 450 ns, WRITE (1) is on 500 ns, and INHIBIT (1) is on 550 ns. CMC RQ SYNC flip-flop and CMC CYCLE DONE flip-flop on Dwg. CMC1 are used as synchronizing flip-flops. The RQ SYNC flip-flop monitors the priority network to see whether a processor request has been generated. This is done in two modes of operation. The first mode being SINGLE PROCESSOR MODE on which T0 which was generated by a processor request will set the RQ SYNC flip-flop. Second being MULTIPROCESSOR MODE in which T0 again is used, but is delayed by 100 ns (the time allowed for the priority network to deselect and settle down) and regenerated as RQ SYNC (⟶1) pulse which set RQ SYNC flip-flop.

The CYCLE DONE flip-flop monitors the timing control of the memory at the time the timing cycle has been completed. CMC T6 will set the CYCLE DONE flip-flop to a one provided that the CMC STOP flip-flop has not been set (this STOP FF is set by a switch or T2 on the indicator panel for single cycle operation) at the completion of a memory cycle.

When both RQ SYNC and CYCLE DONE flip-flop are set, the timing chain will be initiated starting with T1A, T1B, and MA JAM. These flip-flops are both cleared at T2 time and are also cleared by power clear pulse.

On Dwg. CMC2 (Sheet 1), the AWAIT RQ flip-flop is set at T5 or AW RQ (⟶1) from 1X26H. AW RQ (⟶1) pulse is an automatic setting of the AW RQ flip-flop in the event of a lower priority being first selected then deselected by noise on a higher priority bus line in which case all the active flip-flops would be left in the zero state, and the AW RQ FF being clear by T0 developed by the lower priority being selected first. This case is rare, but gives the priority network a second chance to

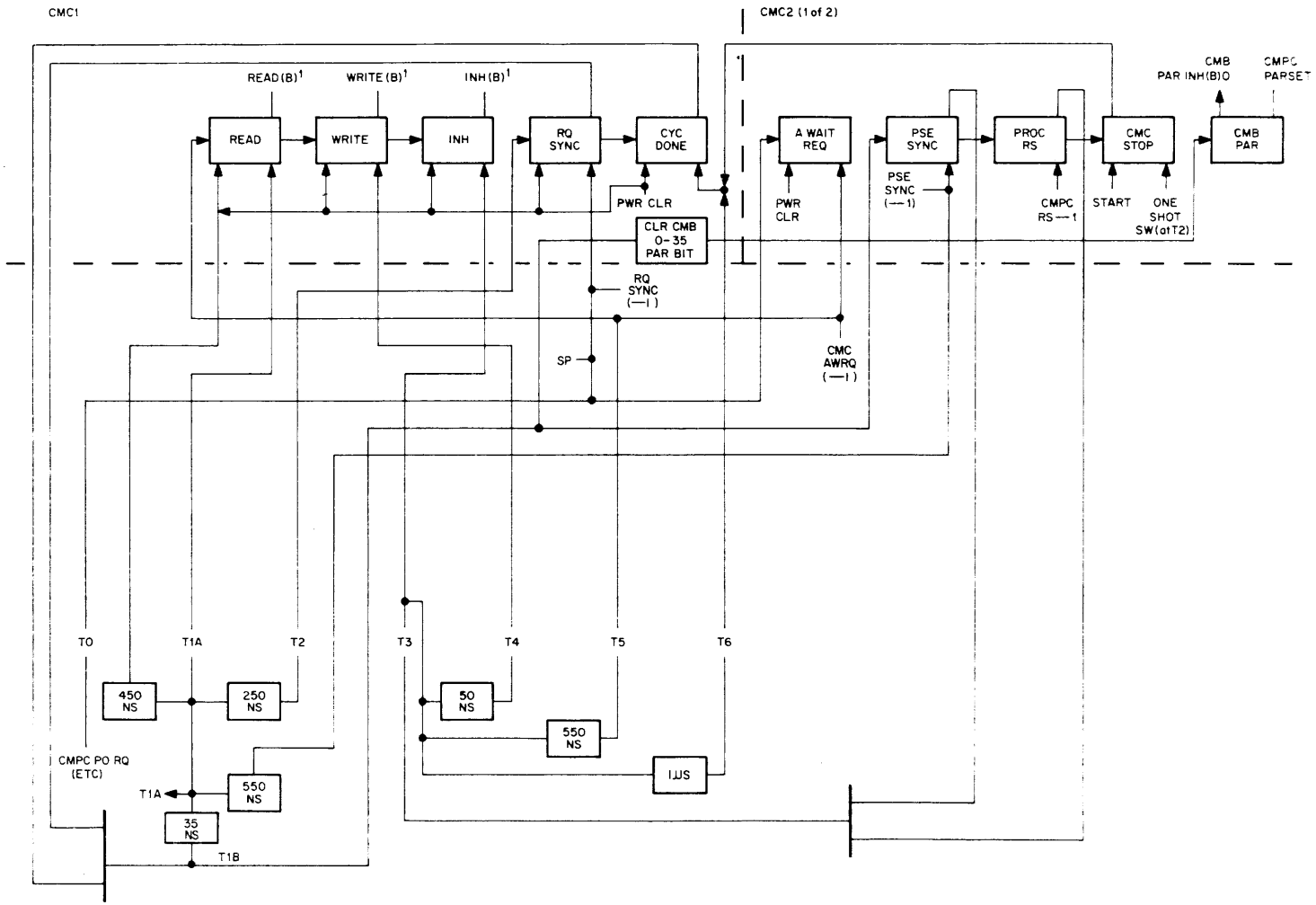


Figure 3-3 Control Flip-Flops

see what processor desires access. AWAIT RQ (1) indicates that the memory is free. The PSE SYNC flip-flop is set by the control signal PSE SYNC (⟶1), and functions to synchronize the write part of the cycle. PSE SYNC flip-flop is a synchronizing flip-flop which monitors the completion of the read protion of a cycle in either READ ACCESS, WRITE ACCESS or READ/WRITE. It is generated 100 ns after clearing the READ flip-flop. In the READ ACCESS, PSE SYNC is ANDed with WR RQ (1) to generate T3 which starts the write portion of the cycle. In the WRITE ACCESS, and READ/WRITE MODE PSE SYNC is ANDed with PROC RS to generate T3, which starts again the write portion of the cycle. The PROC RS flip-flop, through the RS ⟶1 signal from CMPC, receives the restart signal from the processor. The STOP flip-flop is controlled by a single step switch which allows T2 to set it.

3.1.3.4 Single Step Operation - If the CMC STOP flip-flop on Dwg. CMC2 (Sheet 1) is a ONE by T2 in a single operation selected by the SINGLE STEP switch, the timing chain stops at T6. To restart, the operator must push the RESTART button shown on CMC1 to generate the CMC RESTART pulse. This pulse provides CMC START and thus CMC STATE CLR. CMC START provides T6 to set up the CYCLE DONE flip-flop for a new memory access, and T5 to set AW RQ flip-flop.

3.1.4 Core Logic

The core logic consists of X- and Y-selection, inhibit logic, and sense logic. The core stack consists of 37 planes for 36 data bits and one parity. A simplified core stack arrangement is shown in Figure 3-4.

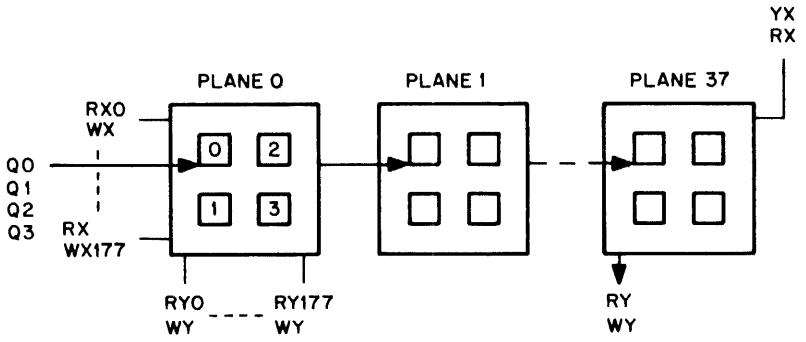


Figure 3-4 Simplified Core Stack Arrangement

Through all planes, the memory is divided into four quadrants for sensing and four segments for inhibiting. Figure 3-5 shows the addressing bit assignments for the memory.

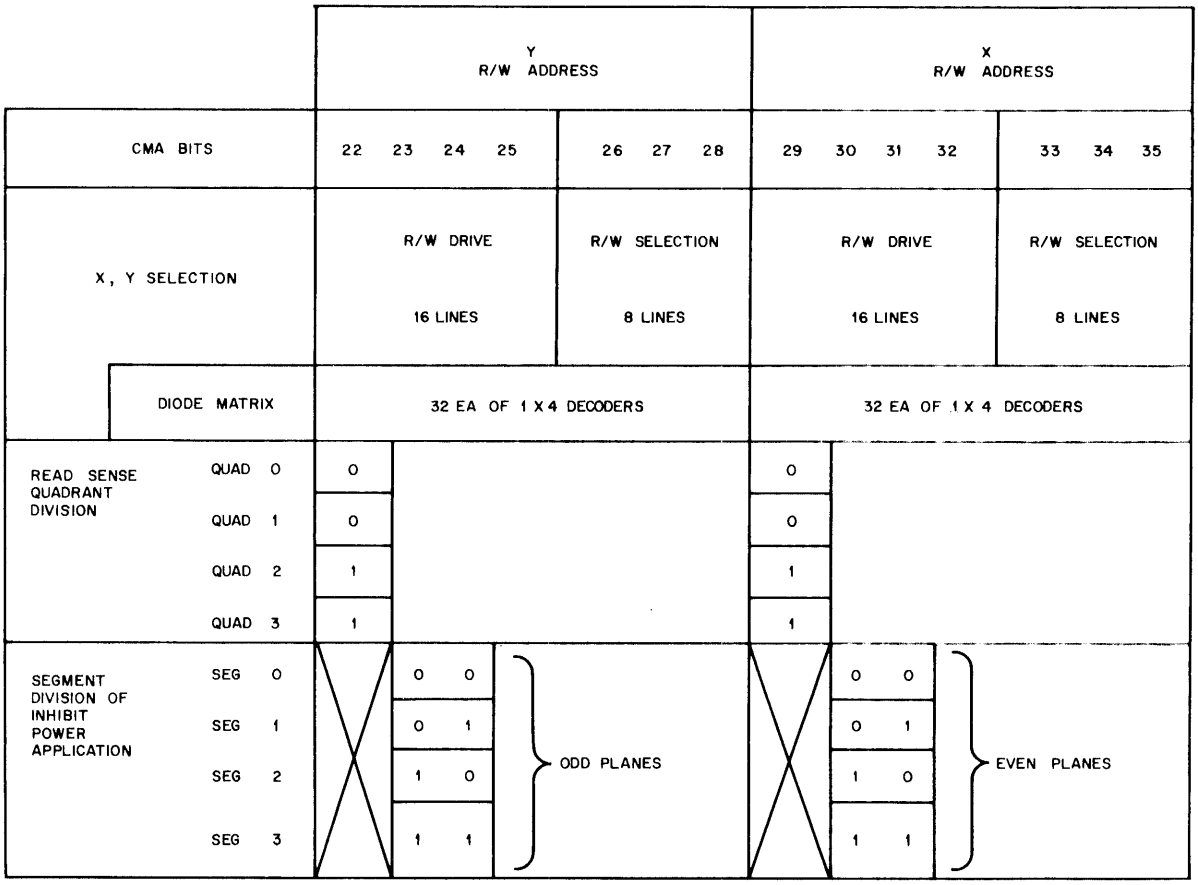


Figure 3-5 Core Memory Type 164 Addressing Bit Assignments

In a read cycle, X- and Y-selection is controlled by the 14 CMA bits shown and sense quadrant selection by the 22 and 29 bits, inhibit segment selection by 23 and 24 for odd bits and 30 and 31 for even bits. By this arrangement, any address can generate a proper sense quadrant selection signal and inhibit segment selection level. In this way, when an address is called only sufficient drive current is required to drive the selected sense quadrant and inhibit segment.

3.1.4.1 X- and Y-Selection Logic - The details of the logic are contained on drawings CMX, CMY, DMSX, and DSMY. The schemes for selection are the same for both X and Y; therefore, only the X selection is described and shown in the simplified diagram Figure 3-6.

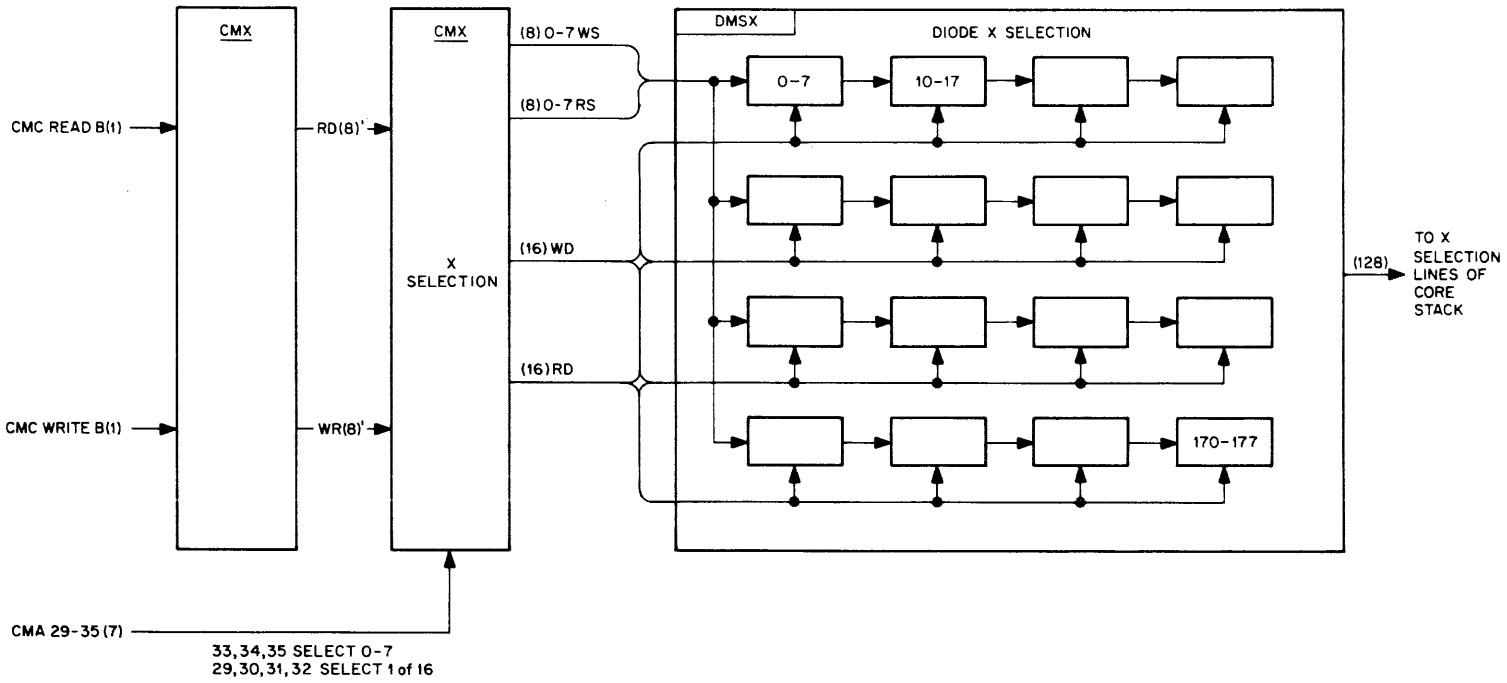


Figure 3-6 X-Selection Logic

The READ and WRITE flip-flops of CMC provide the enabling signals to the X selection logic which receives address bits 29 through 35. The outputs are 1 of 8 write or read lines that provide a single line into one of the 16 octal group circuits of the diode matrix, and 1 of 16 lines selects the proper octal group. The Y selection is accomplished in the same way. Bits 33, 34, and 35 select the 0 to 7 count within each octal group; bits 29, 30, 31 and 32 select 1 of 16 separate octal groups. The output of the diode matrix is 1 of 128 X-selection lines to the core stack.

3.1.4.2 Inhibit Logic - Inhibit logic details are contained on drawings CMI-1 and CMI-2. The simplified scheme is shown in Figure 3-7.

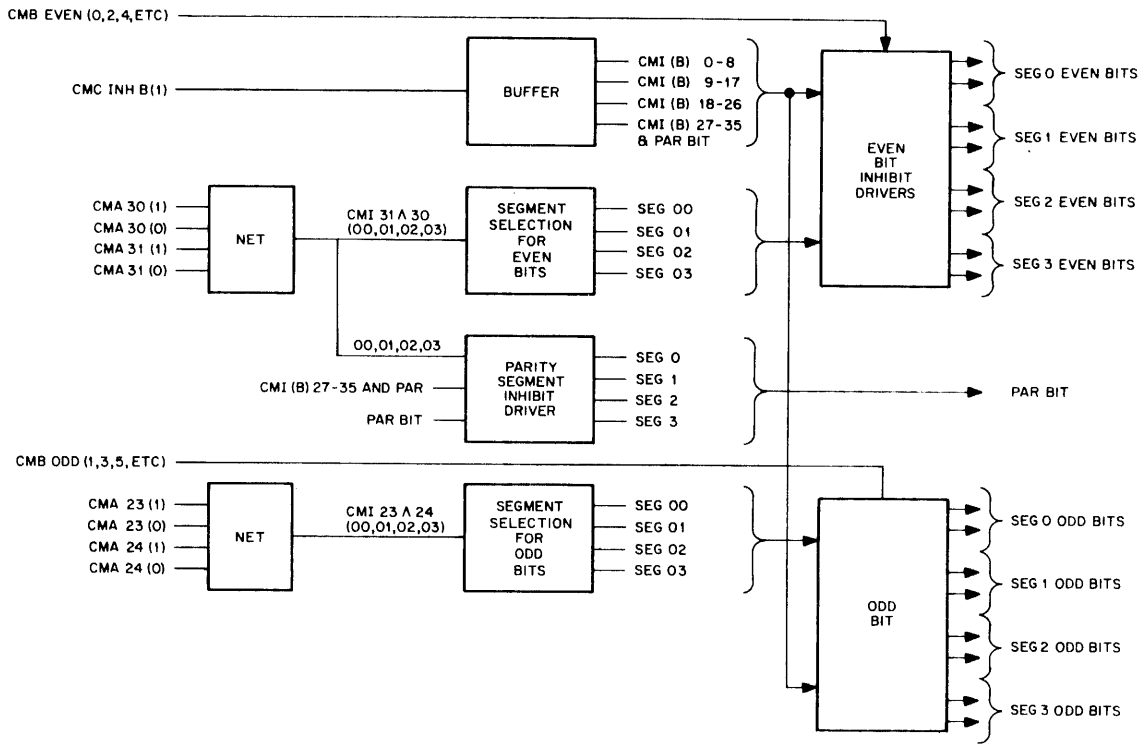


Figure 3-7 Inhibit Logic

The nets determine which segment contains the addressed location by decoding address bits 23 and 24 for odd bits and 30 and 31 for even bits. The inhibit driver for a plane provides an output pair for each of four segments. Inhibit current flows only for the duration of the inhibit signal from memory control, and only through drivers corresponding to CMB 0s at the CMB bit inputs. Thus, during a write cycle, 1s are written into all cores of the addressed location except into those planes which receive inhibit current.

Figure 3-8 shows the winding configuration for four segment inhibit winding for a 16K memory Type 164 System.

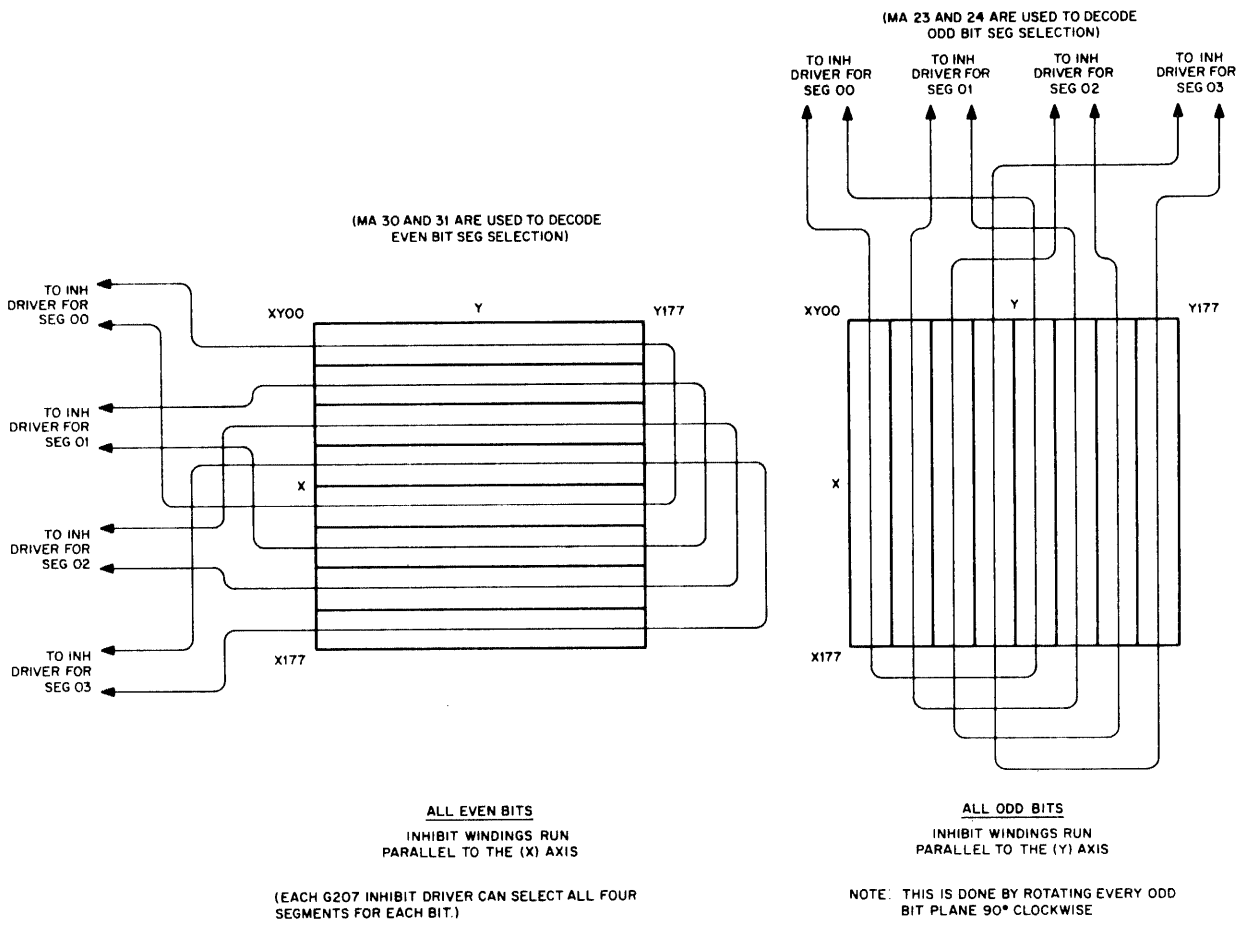


Figure 3-8 A Segment Inhibit Winding for 16K - 164 System

3.1.4.3 Sense Logic - Details of the sense logic are contained on MSSA1, (Sheets 1 and 2) and MSSA2. Figure 3-9 is a simplified diagram of the sense logic.

For read-sense quadrant selection, bits 22 and 29 are decoded. These are the MSB's of the X- and Y-addresses. The decoding circuits provide four signals for each quadrant to drive the sense amplifiers. Strobe inputs provide timing control. As in the inhibit scheme, the sense logic provides one pair of sense lines for each quadrant.

Figure 3-10 shows the winding configuration for four-quadrant sense winding for a 16K memory Type 164 System.

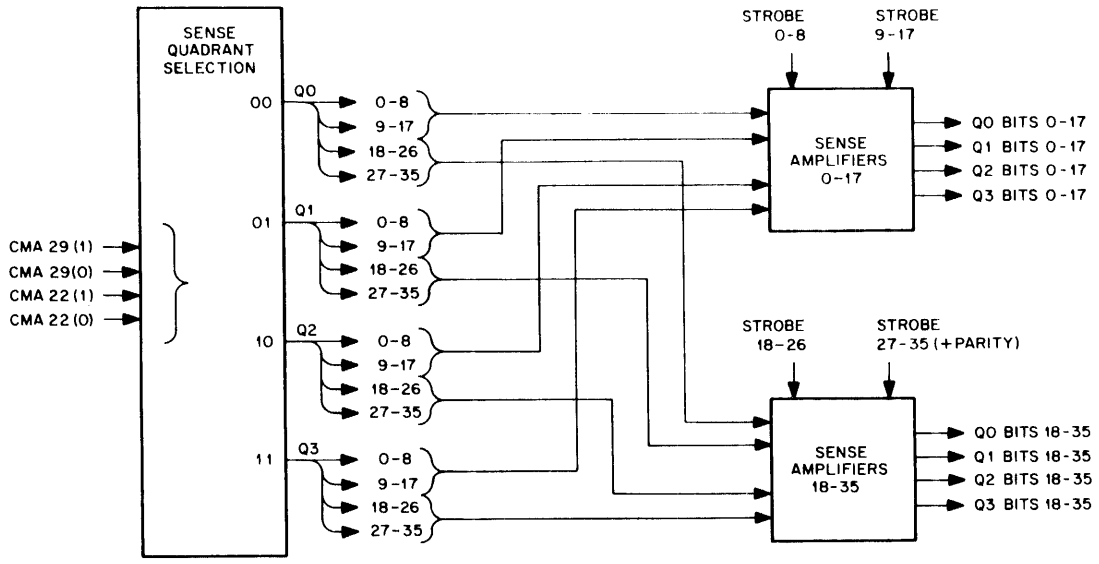


Figure 3-9 Sense Logic

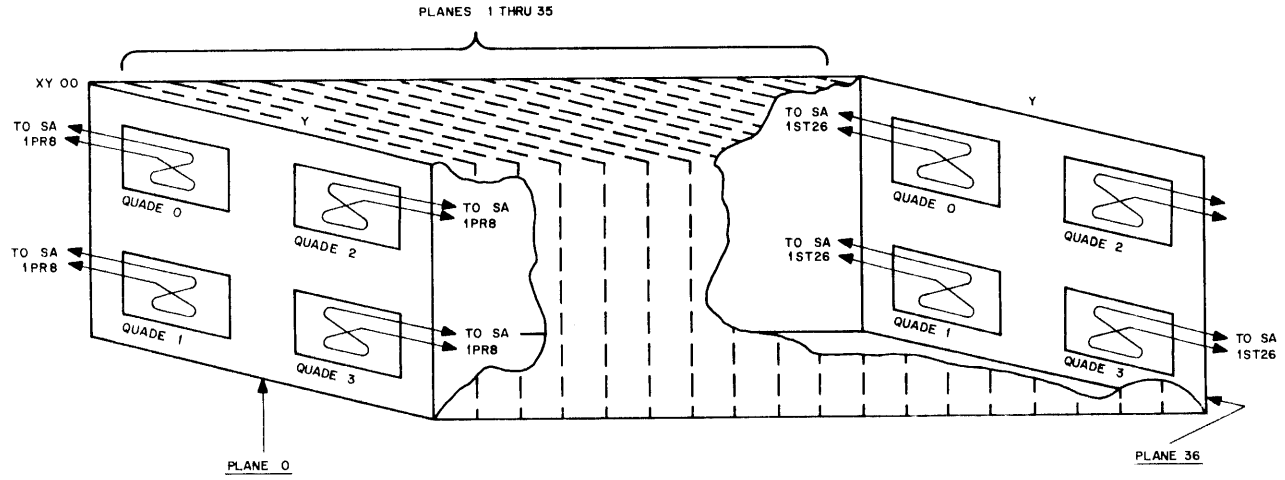


Figure 3-10 Four Quadrant Sense Windings for 16K - 164 System

3.2 TIMING

The memory system timing chain and associated logic are shown on Dwg. CMC1. Figure 3-11 briefly summarizes generation of the timing chain pulses.

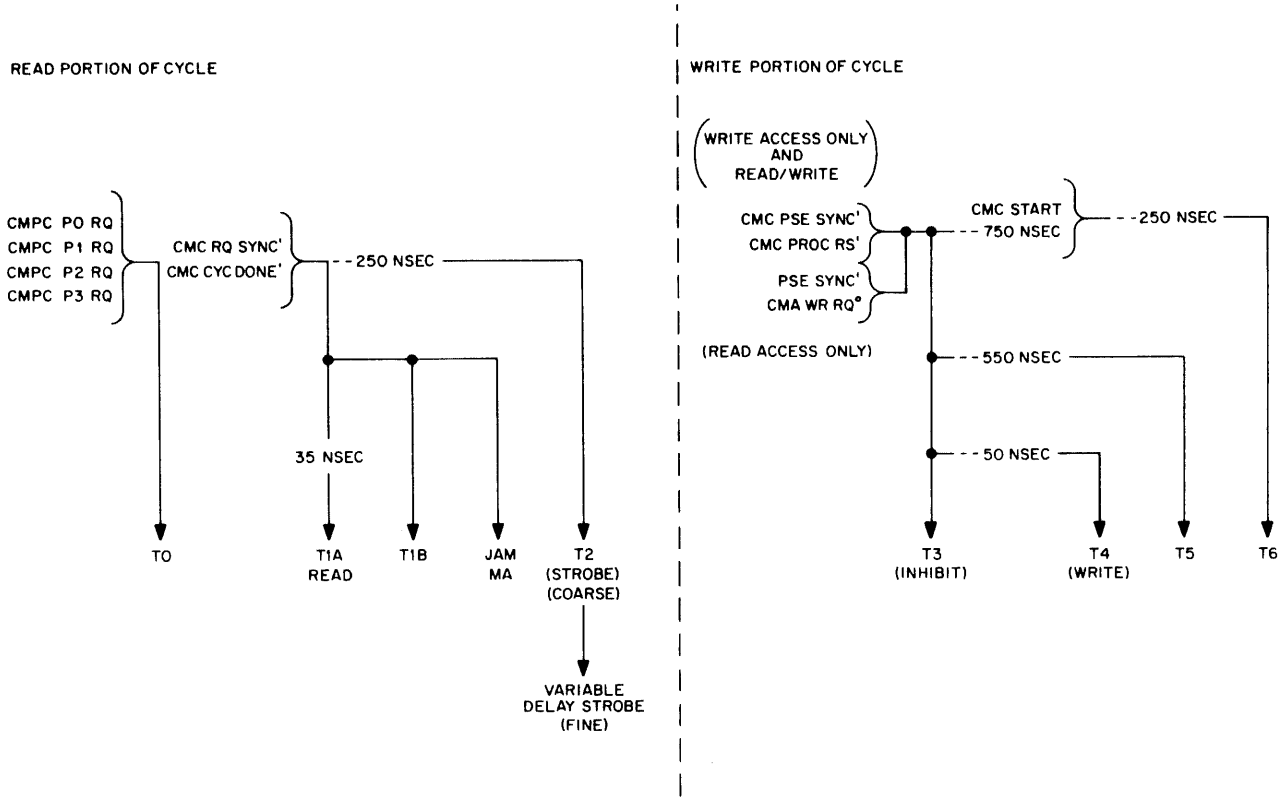


Figure 3-11 Timing Chart

Any CMPC processor request signal triggers the chain by generating T0. The T0 pulse sets the RQ SYNC flip-flop which generates T1A to provide JAM CMA 22 through 29 and JAM CMA 30 through 35 to set the address into CMA. This same flow generates CMB CLR 0 through 35 and the PAR BIT signal to clear CMB at the start of the cycle.

At this time, the processor priority logic on Dwg. CMC2 (Sheet 2) selects the processor that has priority for access.

If access is for write, the processor upon receiving ADDRESS ACKNOWLEDGE immediately loads CMB and returns the WRITE RESTART signal to CMPC. The processor generates a restart strobe RS < (1) which sets the PROC RS flip-flop on Dwg. CMC2 (Sheet 1). Because the memory at this point has the information for writing during the second part of the cycle, the PROC RS flip-flop transition triggers the STATE CLR signal on CMC1 to clear the active flip-flops on CMC2 (Sheet 2). PROC RS flip-flop is also ANDed with PSE SYNC flip-flop which initiates T3, the write portion. In this way, the memory is effectively disconnected from the processor and can then finish the write process while the processor is free to address another memory bank.

If access is for read, T1A occurs 35 ns after T1B and turns on the read signal to the core logic by setting the READ flip-flop on CMC1. Signal T1B on drawing CMPC enables the logic to send the ADDRESS ACKNOWLEDGE pulse back to the processor that has access. Then, 250 ns after T1A (READ), T2 (STROBE) occurs and triggers strobes for the sense amplifiers at the proper time during the read interval.

The logic at the right of CMC1 shows T2 connected to a variable delay to generate RD RS, and the strobe signals SA STB 0-8, 9-17, 18-26, and 27-35. While information is strobed from the sense amplifiers into CMB and out over the bus, the RD RS signal goes to CMPC for return to the processor.

In restoring the information the CMC WR RQ flip-flop is ANDed with PSE SYNC flip-flop to initiate T3 the write portion. T3 also is gated with WR RQ on a 0 to develop a state clear the active flip-flop, and thus disconnect the bus from memory to processor. No WR RS signal is initiated during a read access only. Again the memory will go on and write leaving the processor free to address another memory bank.

The READ/WRITE is much the same as a read access except for the following: The condition of CMA RD RQ (1) and CMA WR RQ (1) is true. This enables a second CMB CLR pulse to be generated 300 ns after T2 so that the CMB register will be cleared when it is ready to accept new information for the write portion of a READ/WRITE CYCLE. A WR RS pulse is sent back to the memory to set the PROC RS flip-flop which is gated with PSE SYNC flip-flop to generated T3 which is the start of the write portion. The PROC RS flip-flop also generates a state CLR pulse to clear the active flip-flop and again disconnect the bus and leave the processor free to access another memory bank.

In the second part of the cycle, the word CMB, whether supplied by the processor or read from memory during the first part, is written in the addressed location. T3 starts the inhibit level by setting the INH flip-flop on CMC1. Then, 30 ns later, T4 sets the WRITE flip-flop to provide the WRITE(B) 1 level. At 500 ns after T4, T5 is generated to terminate the write cycle by resetting the WRITE and INH flip-flops, and setting the AWAIT RQ flip-flop on CMC2 (Sheet 1) to indicate that the memory is again available for a processor request. T6 or CMC STOP B (0) provides the CMC CYC DONE (1) to set the CYC DONE flip-flop.

3.3 POWER SUPPLIES AND CONTROLS

The remaining logic to be discussed is associated with memory power turn on and power failure. Connections to the power control relay Type 836 are shown on Dwg. 164-0-CMC2 (Sheet 1). The PSOK signal generated from the 739D power supply, and W505 (low voltage detector) which indicates when power levels are satisfactory for operation, are shown on Dwg. 164-0-CMC1.

The PSOK logic level is an input to the 200 ms leakout delay (IUV32). The 0 output of this delay supplies the input to pin V of the start delay (IUV31). This type of delay is triggered by a transition to ground at pin V (delay period does not begin until the pulse at V disappears). Thus when the power comes on, both delays come on in the 1 state.

At turn-on time, power voltage changes are slow so that the 1 output of the upper delay that triggers the power start through PA at IU30-U is slow. To prevent premature processor access, the 1 output of the lower delay held asserted by PSOK, holds CMC AW RQ in the 0 state and thus prevents any processor from gaining access.

When the start delay (1UV31) times out (100 ms), its 0 output supplies a power clear level that holds off the core-control flip-flops.

When power becomes satisfactory (PSOK), the period of the lockout delay (200 ms) begins. At its completion, it drops the request lockout ($\not 0$ AWAIT RQ), and its 0 output sets and holds the start delay (100 μs). The transition in this generates the START signal and enables T5, which sets the AWAIT RQ flip-flop to indicate that the memory is available to the bus, and T6 which sets CYC DONE flip-flop (1).

When the memory is operating, the lockout delay (IUV32) is off and its 0 output holds the start delay on to insure continuous operation. If power levels become unsatisfactory, PSOK is negated, triggering the lockout delay and allowing the start delay to begin. During this period, the current memory cycle is completed. After this delay times out, the 0 output power-clear level inhibits further operation.

Each memory has a pair of power controls, Types 836 and 834, shown on Dwg. CMC2 (Sheet 1). The Type 836 Power Control contains a diode gate that receives the -15V turnon signals supplied from the power terminal. The output of the gate goes through the power switch on the control panel and back to the 836 to energize a relay that turns on the Type 834 Power Control. The Type 834 Power Control receives the local ac line voltage and provides this to the system power supplies.

Power supply Type 728 provides +10 and -15 Vdc and Type 778 Power Supply also provides -15 Vdc for the memory logic and the core memory control. Power Supplies 739 provide voltage for circuits associated with the driving of the core bank.

CHAPTER 4
SPECIAL MEMORY MODULES

This chapter explains the seven special memory modules used in the Type 164 Magnetic Core Memory System. These modules are analogue in nature and are not explained in the standard logic handbook. To aid the maintenance personnel with troubleshooting, a brief functional description of each module that indicates the input and output signals is provided. A block diagram of each module is also provided.

4.1 G005 SENSE AMPLIFIER

This double-height module detects the ONE and ZERO outputs from coincident-current core memory systems. Each module has the capability of sensing one of four fields. The field being sensed is selected by holding the appropriate preamplifier field select gate at the -3 Vdc level and the other three field select gates are deselected with a -6 Vdc level. Refer to Figure 4-1 for the following functional description.

To obtain optimum operation, each preamplifier has a balance potentiometer that is used to adjust the preamplifiers output within ±200 mV of balance. The outputs of the four preamplifiers are connected in parallel to a common amplifier. From the common amplifier, the output signal is applied to a rectifying slicer and the resultant signal from the slicer is used to enable a DCD gate. When the selected core output is a ONE, the DCD gate is enabled and the pulse amplifier is gated by the 40 ns strobe pulse. The pulse amplifier generates a 100 ns output pulse.

A G008 Master Slice Control determines the operating current of the preamplifier and the common amplifier and also the slice level for the rectifying slicer.

Inputs

Preamplifier:	Accepts a signal up to a 50 mV from the sense lines.
Strobe:	A 40 ns negative pulse that draws 1 mA at -3 Vdc and negligible current at ground.
Field Select:	SELECT: A -3V level that draws approximately 5 mA due to the transient effect of the memory stack capacitance.
	DESELECT: A -6V level that draws approximately 10 mA.
First Stage (Clamp Level):	Operates at 3.8 Vdc with respect to +15 Vdc and draws 0.7 mA.
Second Stage (Clamp Level):	Operates at 8.0 Vdc with respect to +15 Vdc and draws 0.3 mA.
Slice Level:	Operates at a dc level between 5.5V to 5.9V with respect to +10 Vdc and draws 0.4 mA.

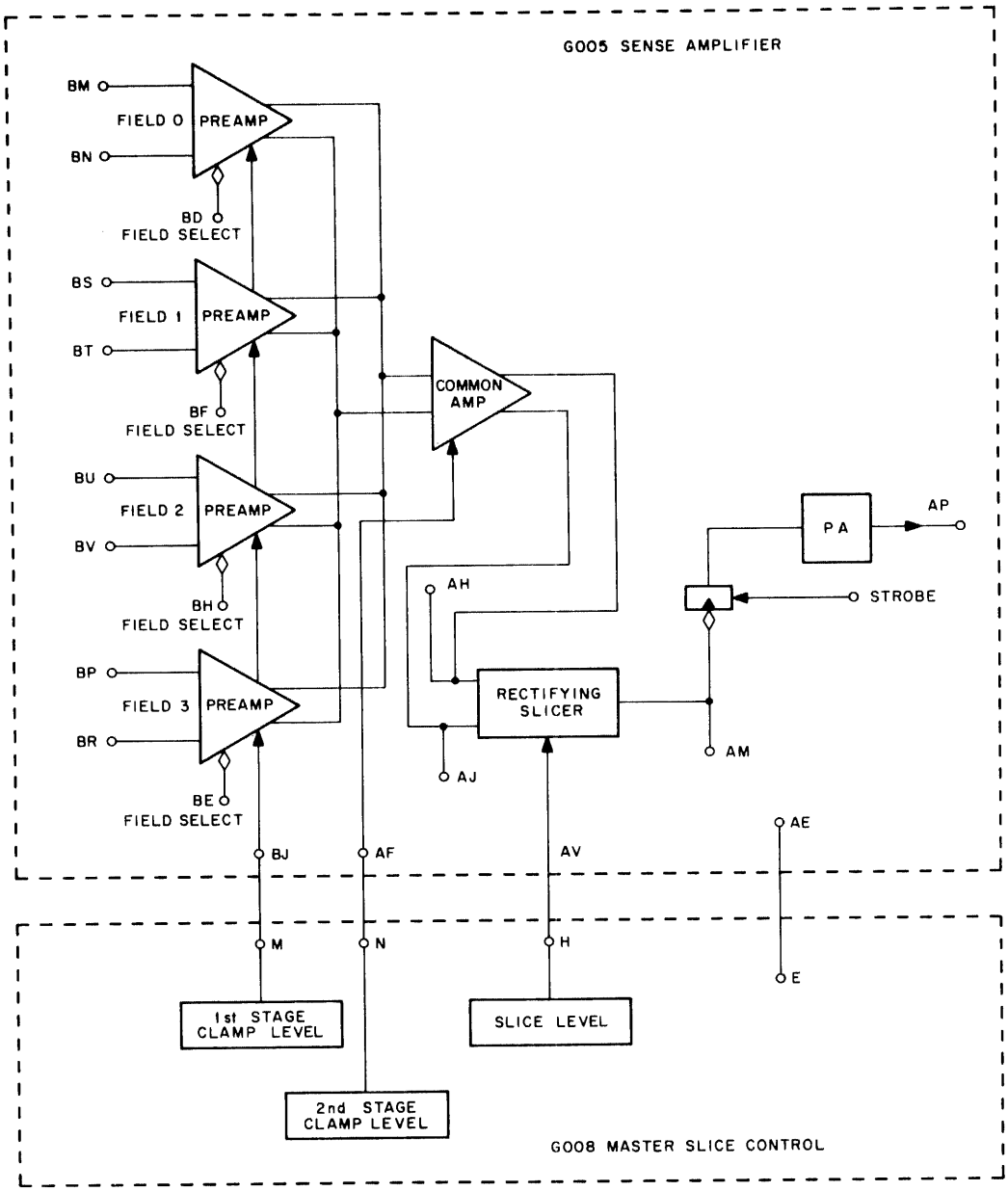


Figure 4-1 G005 Sense Amplifier

Output

Amplifier:	Overall amplifier gain between 65 and 85, measured single - ended at the outputs AJ or AH.
Rectifying Slicer:	Output capable of driving 1.0 mA at ground level and 8.5 mA at -3 Vdc.
Pulse Amplifier:	A 100 ns 3V negative pulse capable of driving 10, 2-mA diode gates. A negative pulse out is a ONE.

4.2 G008 MASTER SLICE CONTROL

This module supplies the first stage clamp level, the second stage clamp level, and the slice level required by the G005 Sense Amplifier. Refer to Figure 4-2 for the module block diagram. Each circuit consists of a zener diode network with silicone diodes for temperature compensation. Emitter follower stages provide current driving capability and low-impedance outputs.

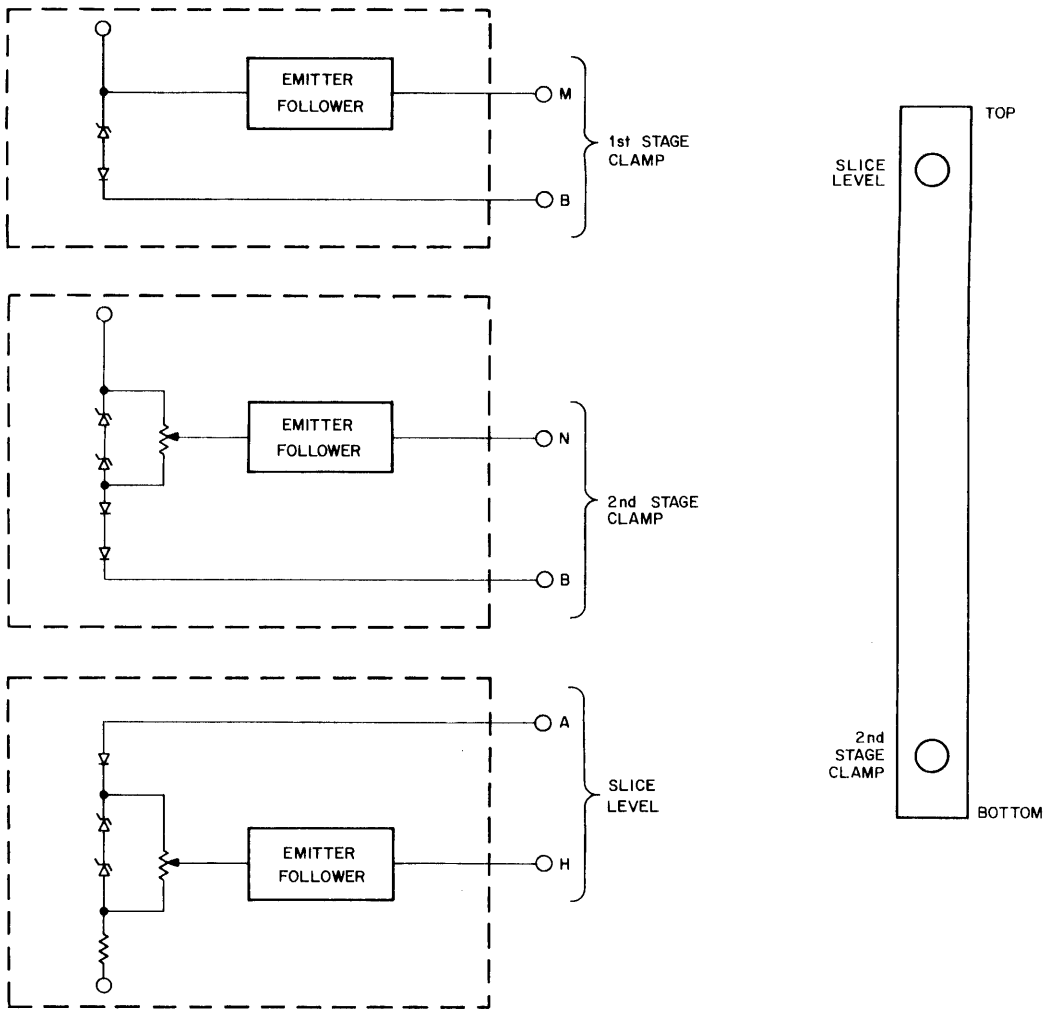


Figure 4-2 Master Slice Control

Output

First Stage (Clamp Level): 3.9 Vdc with respect to -15 Vdc

Second Stage (Clamp Level): Variable between +0.6 and +13 Vdc with respect to -15 Vdc.

Slice Level: Variable between 0 and -11.6 Vdc with respect to +10 Vdc.

4.3 G010 SENSE AMPLIFIER SELECTOR

This module contains two noninverting driver circuits. Using standard input levels, each drive circuit can drive a large number of base loads and diode loads with levels of -3V and -6V. Refer to Figure 4-3 for the module block diagram.

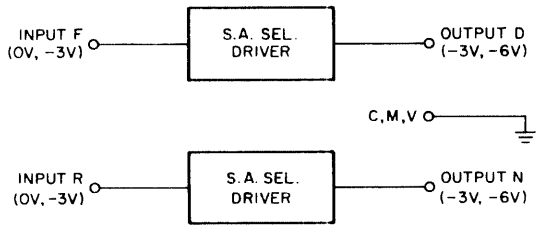


Figure 4-3 Sense Amplifier Selector

Input: Standard DEC logic levels are used; 2 mA of base load are used when the input is -3 Vdc.

Output: A -3 Vdc level occurs when the input level is at ground; a -6 Vdc level occurs when the input level is at -3 Vdc. These levels can drive ±40 mA at 10 Mc. Drive delay is approximately 40 ns.

4.4 G206 MEMORY SELECTOR

This module is used as a selector switch in the read/write matrix of coincident current memories. Refer to Figure 4-4 for the following functional description. Each module contains two read gates and two write gates. Due to the decoding, only one read gate and one write gate may be enabled at one time. Although this module is primarily intended for four-bit decoding, it may be used for three-bit decoding by grounding pin AK.

Input: Standard DEC -3 Vdc levels are used for turn on. The decoding gates and the LSB gate draw one unit of base current. The read or write gates draw two units of base current.

Output: Each output can drive 425 mA for 500 ns at a PRF of 1 MHz. The following specifications refer to the output waveform.

Maximum delay for output fall: 80 ns

Maximum delay for output rise: 50 ns

Minimum cycle time: 1.3 μs

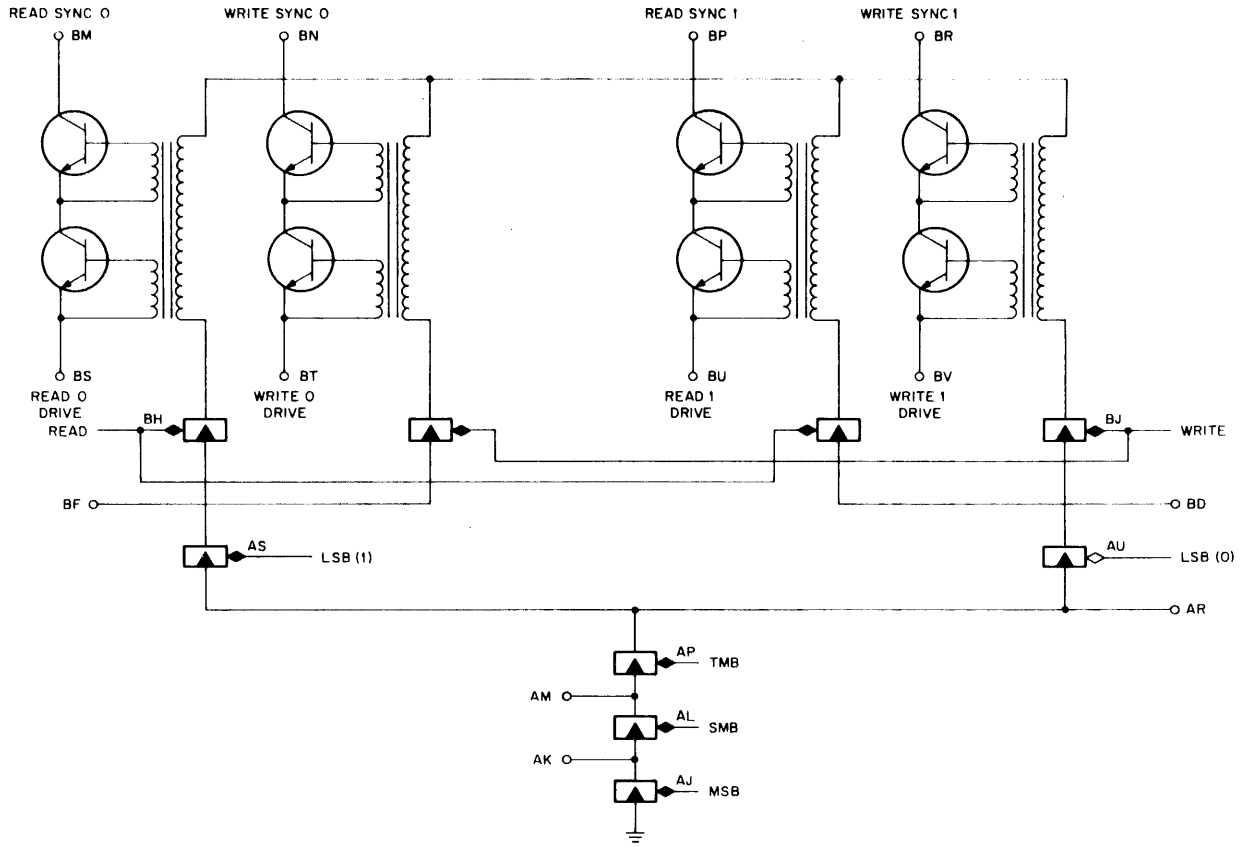


Figure 4-4 G206 Memory Selector

4.5 G207 INHIBIT DRIVE

This module is used to drive the inhibit winding of magnetic core memory planes. Refer to Figure 4-5 for the following functional description. Each module contains four identical gated circuits. A balun (1/1 balanced trap) at the output is used to obtain balanced drive. The switched current is determined by the inhibit resistor.

Input: Standard DEC -3 Vdc levels are used for turn on. The quadrant selection gates draw two units of base current and the MB gate-input draws three units of base current. Each of the inhibit gate inputs draws 1 unit of base current.

Output: Each output can drive 350 mA for 600 ns at a PRF of 750 KHz. The following specifications refer to the output pulse.

Maximum delay for output fall: 60 ns

Maximum delay for output rise: 60 ns

Minimum cycle time: 1.3 μs

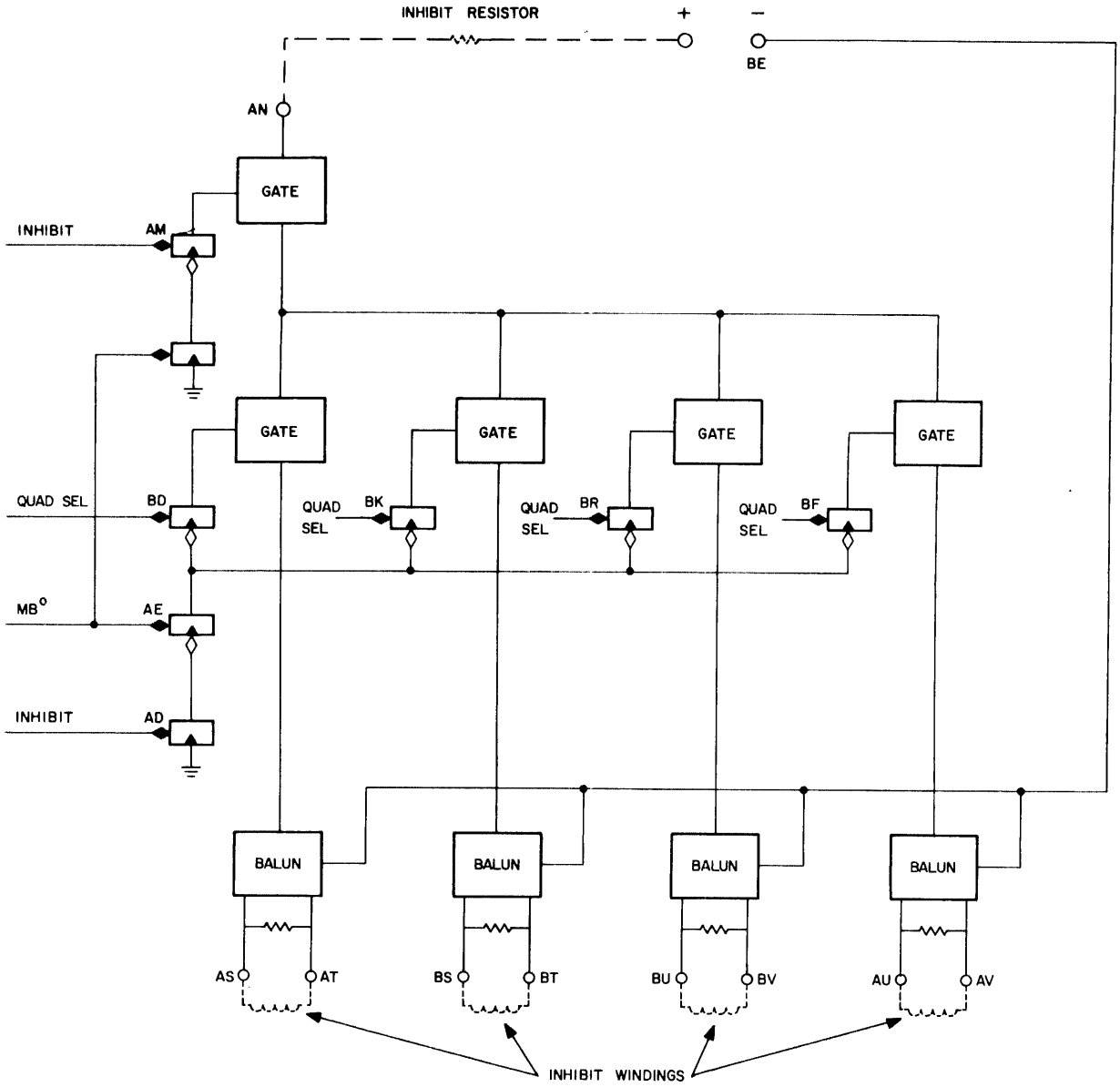


Figure 4-5 Inhibit Drive

4.6 G212 MEMORY COMMON DRIVE

This double height module is used as a common drive in the read/write matrix of coincident current memories. Refer to Figure 4-6 for the following functional description. Each module contains two read gates and two write gates but the decoding gate enables only one read gate and one write gate at a time. The decoding circuit is used to decode a 4-bit address. Clamping diodes are connected to terminals AE and AF to limit transients, and compensating resistors are connected to terminals BE and BK to bias the diode balun matrix.

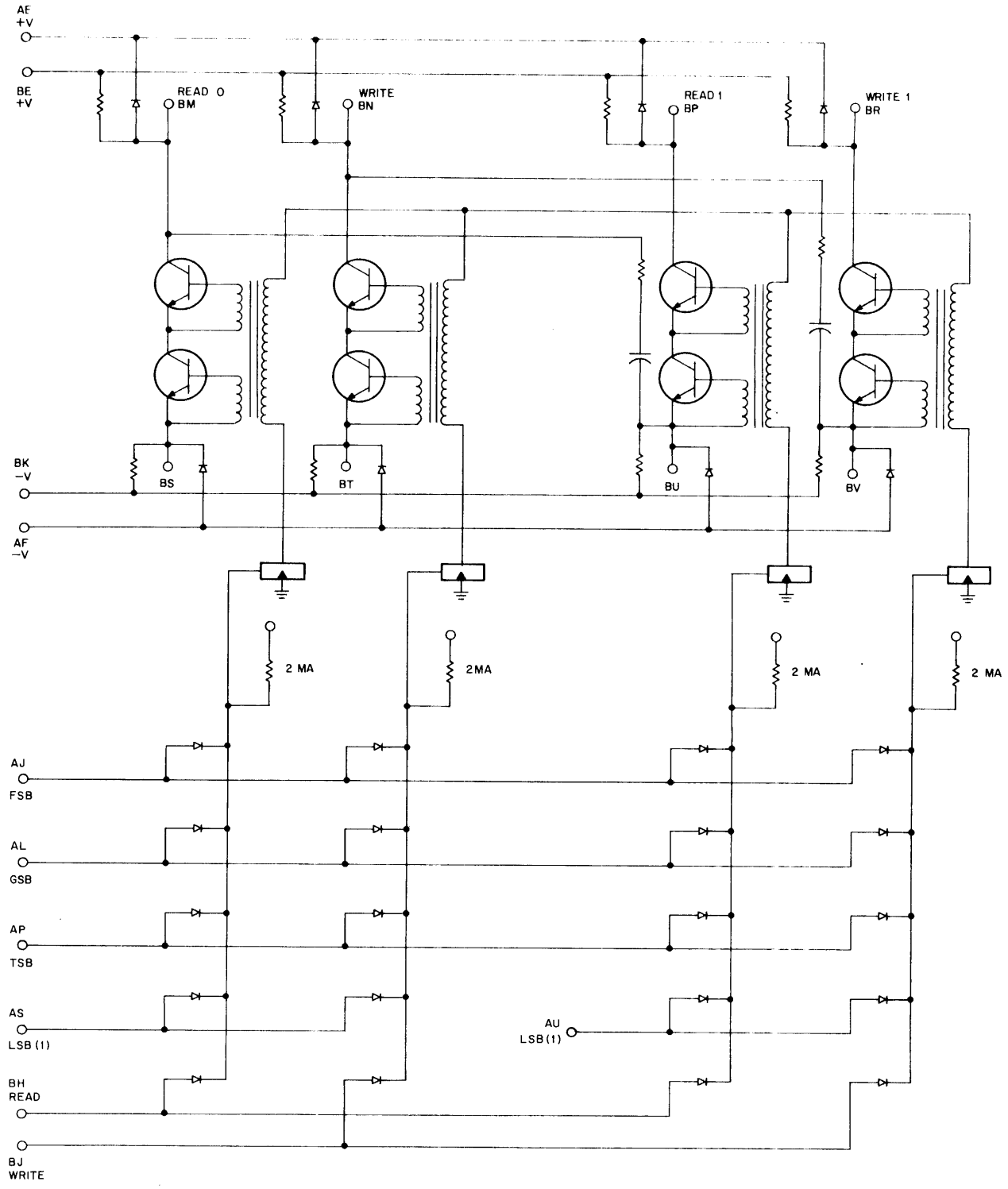


Figure 4-6 Memory Common Drive

Input: Standard DEC -3 Vdc levels are used for turn on. All input gates draw 2 mA of current at ground.

Output: Each output can drive 425 mA for 600 ns at a PRF of 750 KHz. The following specifications refer to the output waveform.

Maximum TTT of output fall: 150 ns

Maximum TTT of output rise: 100 ns

Minimum cycle time: 1.5 μs

4.7 G604 MEMORY SELECTOR MATRIX

This module is used to select the read or write windings of a coincident current memory. Refer to Figure 4-7 for the following functional description. There are four diode-balun networks on each module. Each diode-balun network provides a current path through one winding for read and the reverse current path for write. A balun transformer is used to provide balanced drive.

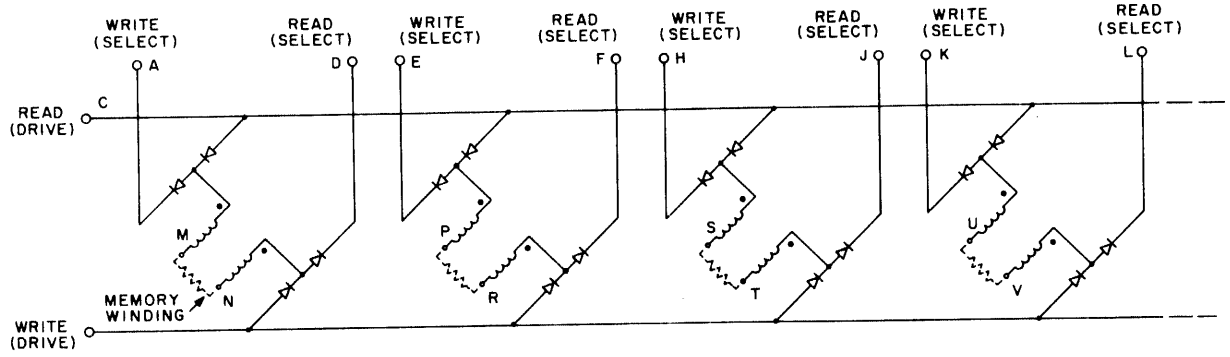


Figure 4-7 Memory Selector Matrix

Input: A 425 mA current for 500 ns at a PRF of 1 MHz. The output pulse from a G206 module.

Output: Each output can drive 425 mA for 500 ns at a PRF of 1 MHz. The following specifications refer to the output waveform.

Maximum TTT output fall: $\leq$ 130 ns

Maximum TTT output rise: $\leq$ 85 ns

CHAPTER 5
MAINTENANCE

Preventive and corrective maintenance at the system level are discussed in this chapter. Since the memory must operate with a Type 166, Arithmetic Processor the discussions presented here, should be used with a full knowledge of the processor and in conjunction with the descriptions in Chapter 9 of the Type 166 Arithmetic Processor Maintenance Manual. Many memory maintenance procedures such as MAINDEC programs use the processor.

The following equipment, with that listed in Chapter 9 of the Type 166 Maintenance Manual, is required to support testing of the Type 164 Memory.

Oscilloscope current probe	Hewlett Packard 1110A or equivalent, calibrated to 1 mV per mA
Dual-channel oscilloscope preamplifier	Tektronix Model CA or equivalent; must have algebraic-add facility.

5.1 MAINDEC DESCRIPTIONS

There are six basic MAINDEC programs fo use in trouble shooting the memory system; all use the processor to exercise either fast or core memory. Each consists of a program tape and a write-up in the 6-MD-DEC reference manual. As an introduction to the MAINDEC write-ups, see Chapter 9 of the Type 166 Processor manual. Always consult the program write-ups for information on start addresses, address modification, or details of program operation. MAINDECS for the memories are as follows.

MAINDEC 603-1 Low-End Address Test - This address test checks registers for unique contents.

MAINDEC 603-2 High-End Address Test - This program, which is loaded into the top of memory (highest available addresses), checks each location for unique contents by loading it with its own address.

MAINDEC 613 Core Data Test - This MAINDEC tests all locations from 40 up, except the top 27, which are occupied by the program. Each time the test word, originally supplied by the DATA switches, is read in and out, the contents of core are tested for accuracy; then the test word is rotated once and the same location is tested again. After 36 rotations the address is indexed and the next location is tested in the same manner. Installations having the two core memories can use this program

most efficiently by modifying its address limits so that the program is contained in one memory while the other is tested completely. The program is then immune to marginal checking or trouble shooting procedures on the memory under test.

MAINDEC 622A High Speed Checkerboard Test - This program, in the presence of a noise-producing data pattern, tests the Type 164 Memory for read-out errors. The program has several options, one of which allows the worst case noise to be generated for any memory or interleaved configuration currently produced. This test should be used to verify correct operation of the memory sense amplifier and inhibit drivers.

MAINDEC 691 Automatic Block Transfer Test - This test detects and diagnoses malfunctions occurring in the block transfer instruction. When run with data switches 19-35 down, it serves as a relocation test for adders and the memory address register. It calculates and prints the time every four or five minutes thereby providing a time record of the program run. The program is executed in the user mode. With data switches 19-35 down, the block transfer buffer size and relocation are generated by random numbers; otherwise, they are controlled by the data switches. The block transfer effective address is a function of the buffer size and the "from" and "to" addresses.

MAINDEC 693 Time Sharing Instruction Test - This test runs Parts 1, 2, 4 and 5 of the PDP-6 instruction tests in the user mode to test the time sharing hardware while concurrently testing the instruction set of the PDP-6.

5.2 PREVENTIVE MAINTENANCE PROCEDURE

Preventive maintenance consists of performing specific procedures at scheduled times, using maintenance programs, marginal checks, and other electrical and mechanical checks, including cleaning and inspections.

5.2.1 Daily Operator Maintenance

Check that all cooling fans are running and cooling air flows freely through the filters.

Run the following MAINDEC programs with no margins; log all error halts, and note the cause, if known. Refer to each MAINDEC program write-up for proper operation.

MAINDEC 603-2 High-End Address Test

MAINDEC 603-1 Low-End Address Test

MAINDEC 613 Core Data Test

MAINDEC 622A High-Speed Checkerboard Test

MAINDEC 691 Automatic Block Transfer Test

MAINDEC 693 T/S Main Test

Replace any noncritical components such as indicators, etc. Note any replacement in the log.

5.2.2 Weekly

Using MAINDEC 622A High-Speed Checkerboard, take moderate margin voltage ±5V on sense amplifier panels 1P and 1S 10V line. Log all error halts, noting cause, if known.

5.2.3 Every Two Weeks

Change lower fan filter for memory stack.

5.2.4 Every 1000 Hours

Run the following MAINDEC programs taking margins in the following panels as shown below. Refer to each MAINDEC program write-up for proper operation.

MAINDEC 603-2 High-End Address Test

MAINDEC 603-1 Low-End Address Test

MAINDEC 613 Core Data Test

MAINDEC 622A High-Speed Checkerboard Test

MAINDEC 691 Automatic Block Transfer Test

MAINDEC 693 T/S Main Test

(+10V margins are taken in the following panels, in groups as shown.)

1A through 1F	(Inhibit and R/W)
1P and 1S	(Sense amplifiers)
1R, 1T, 1U, 1V	
1W, 1X	(MB and control)
1Y and 1Z	(MA and control)

(-15V margins are taken in the following panels, in groups and separately as shown.)

1A through 1F	(Inhibit and R/W)
1P and 1S	(Sense amplifiers)
1R	(MB)
1T	(MB)
1U	(Control and interface)
1V	(Control and interface)

1W	(Control and interface)
1X	(Control and interface)
1Y and 1Z	(MA and control)

NOTE: Log all margins on preventative maintenance voltage charts, form #SA-1, dated 5/25/64.

Change and clean all air filters.

5.3 CORRECTIVE MAINTENANCE

The Type 166 manual contains a general discussion of troubleshooting and repair for DEC logic, with a corrective maintenance procedure assigned, to make most efficient use of field engineering time. It is essential that this material be understood.

5.3.1 Power Supply Checks

Before troubleshooting, always check the power supplies for proper voltage output and ripple content as shown in Table 5-1.

Table 5-1
Power Supply Outputs

Measurement Terminals	Nominal Output Voltage (70 F)	Permissible Range	**Permissible Peak-to-Peak Ripple
	Type 728		
Orange (+), Black (-)	10	9.5 to 11.0	0.7V
Blue (-), Black (+)	-15	-14.5 to -16.0	0.7V
	Type 739		
(Jones Strip)			
2(+), 1(-) - Inhibit -	53*	52 to 55	250 mV
4(+), 3(-) - R/W -	65*	63 to 65	250 mV
	Type 778		
Blue (-), Red (+)	-15	14.5 to 16.5	0.7V
Blue (-), Red (±)			

(*) Exact voltage dependent on stack temperature.
(**) 20% more ripple on 50-cycle types.

The Type 728 and 778 Supplies are not adjustable, therefore, if output or ripple is not within the tolerance specified, the supplies should be considered defective and replaced. The Type 739 Supply is adjustable; but, if outputs are outside tolerance, do not attempt to restore the voltages given above without first checking the core drive currents. If all supply outputs are within tolerance, continue logic troubleshooting procedures.

5.3.2 MAINDEC Testing

The most efficient method of troubleshooting a memory is by tracing signals with an oscilloscope. To set up repetitive, predictable behavior, deposit test routines derived from a MAINDEC into a memory other than the one under test, so that even the most severe malfunctions in the latter do not affect the testing routine. After diagnostics have categorized a malfunction, a small part of the memory logic can be operated repetitively by using the processor EXAMINE or DEPOSIT key with the REPEAT switch ON and the speed controls set to the desired repetition rate. These keys make requests only for read or write access, but read/write access can be requested from the computer console by executing an appropriate instruction, preferably the slowest (e.g., subtract in memory mode).

For apparent malfunctions in memory, examine the processor for faults by checking for the presence of signals on the bus without distrubing it; to do this, wheel the scope down to the last memory where the probe can be attached to the bus without distrubing it. Alternatively, there are many points in the processor wiring where memory return signals or their derivatives appear; signal tracing in that area can determine whether the memory sends back the appropriate responses. When troubleshooting, always turn the DISABLE MEMORY switch at the processor ON so that it will hang up whenever it cannot gain access.

5.3.3 Marginal Checking

Nearly all core memory malfunctions are discovered during marginal check process. As margins are increased from nominal bias values, a single bit generally fails first; such failure may be random or systemic. Check for randomness of failure by increasing margins still further: whenever a very slight increase produces errors in several additional bits, the first error can be considered random. Errors occurring at margin levels substantially below those at which most bits are not random; instead, they signify some systemic malfunction that must be corrected. The remainder of this chapter correlates symptoms to their most probable causative malfunctions, assuming that the malfunction is isolated within a single 16K memory. When errors are truly random, but occur at unsatisfactory margins, the adjustment procedure detailed in the following section should be performed to improved marginal

operation before continuing troubleshooting. When margins for properly operating circuits are wide enough, nonrandom malfunctions are more easily detected. Nonrandom errors always occur in specific data patterns.

5.4 ACCESS MALFUNCTIONS

All access troubles a single symptom; either the processor or the memory hangs up. The fault is always a lack of communication between the two, or a signal ambiguity caused by noise or internal memory control malfunction. With the DISABLE MEMORY switch ON, the system will wait after an access failure, allowing examination of the indicators. If the memory AW RQ indicator is OFF, the memory has failed to complete its cycle. If AW RQ is ON, the hang up is at the processor, which has not received the read restart or address acknowledgment over the bus. These pulses turn off indicators at the top of bay 1 at the processor. If the MC RD indicator is lit, the processor failed to receive the read restart during a read or read/write access. If MC RQ is ON, the address acknowledgment was missing. If either system is confined to a single processor in a multiprocessor system, the fault is almost certainly in the CMPC bus associated with it.

5.5 TROUBLESHOOTING GUIDE FOR MEMORY TYPE 164

5.5.1 Memory Does Not Recognize a Processor Request

Check to make sure that all switches on the memory are in the proper position for memory module address and named processor. Check the CMPC (Core Memory Processor Control) cables for bad connections, or for misalignment. Scope for proper memory module address signals.

5.5.2 Memory Hangs-up With AWAIT REQUEST Zero

A possible cause is multiple selection due to noisy module address lines from the computer. If there are negative-going transients on the module address lines after MC REQUEST has appeared on the bus, one memory may not be completely selected; that is, the active flip-flop in that memory may not get set to 1. If this occurs, then no addressing information and no READ or WRITE REQUEST will get strobed into the memory. T0, will probably have been generated, and will clear the AWAIT REQUEST flip-flop, but that is as far as it will go. The next time the computer tries to reference the memory, the memory will not be available so the non existent memory flag will be set.

Another cause may be the READ-RESTART or ADDRESS ACKNOWLEDGE not getting back to the processor on a READ. If the ACKNOWLEDGE does not get back to the CP on a WRITE, the memory will also hang with AWAIT REQUEST zero. On READ/PAUSE/WRITE the memory will hang

with AWAIT REQUEST zero if the RESTART does not get back, and on either a READ/PAUSE/WRITE or a WRITE, the memory will also hang if the WRITE RESTART does not get from the processor to the memory. The best way of determining which of these things is happening is simply to understand the exact interchange of signals between the memory and the CP, for each type of memory cycle.

The following malfunctions also could cause problems: the failure of the REQUEST SYNC flip-flop to be set to L by either T0 in the single processor mode or REQUEST SYNC in the multi processor mode; the failure of the PSE SYNC flip-flop to set, thus preventing T3 from being generated; the failure of T5 to set the AWAIT REQUEST flip-flop to 1; a noisy W505 in the 739 Power Supply causing transients on the PSOK line; or the self-triggering R303 hangs AW RQ FF to 0.

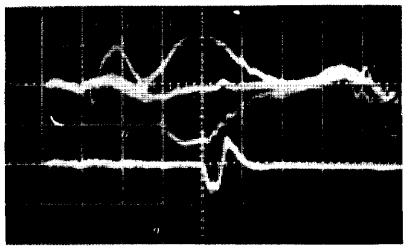
5.6 FULL-WORD FAILURES

Check the pattern of locations that exhibit full-word failures to determine whether they are limited to one or two quadrants or occur throughout a memory. Pickup errors throughout a single quadrant indicate trouble in the sense quadrant selection; check memory address bits 22 and 29 and trace the decoder outputs through. Full-word drop errors in two quadrants indicate that CMABB22 or 29 does not govern quadrant selection in the sense amplifiers; check these levels. Errors affecting the full word in all locations cannot be due to malfunction in the core logic; troubleshooting should thus concentrate on the power supply, memory control, or selection logic. If the power supply outputs are within the tolerances specified at the beginning of this section, malfunction in the supply is doubtful. In general, supply malfunctions can be distinguished from control malfunctions by taking margins on the control panels; poor marginal operation here is due to control-logic faults, since power supply adjustments affect only the sense amplifier margins.

For all types of full-word faults, begin by checking the address logic. Errors in the transfer of addresses from MA in the processor or malfunction in CMA bits or their buffers cause duplication of addressing; a given core location is selected by more than one MA configuration. Thus the same information is read twice, once erroneously, causing data errors in the checkerboard or BTL program (block transfer). If the system is dropping bits, check the logic for transfers into CMB; compare the CMB and processor MB indicators to check data transmission over the bus; check the memory strobe generating logic. For pickup errors check the timing and duration of the inhibit level, and check the CMB clear logic. When the memory exhibits generally poor margins and is both picking up and dropping bits, check the timing of the read and write levels. If necessary, replace the delay lines (W301) to restore this timing requirement.

5.7 SINGLE-BIT FAILURES

A single-bit error that affects only one address results from a single core whose characteristics have drifted out of specifications. Since every memory is checked out thoroughly before shipment, it can be assumed that the cores are not malfunctioning unless they have been subjected to extreme punishment. A single-bit pickup error throughout memory can be caused by a chort or other low impedance path between an X or Y winding and a sense winding, but this is easily recognized by checking the sense preamplifier outputs. Each sense amplifier has test points on the wiring panel for checking internal waveforms. The waveforms at the test point is the differential output of the selected preamp and is shown in Figure 5-1.

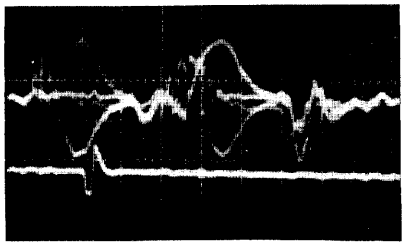


Single ended core read output in reference to strobe.

Time: 100 ns/cm

Core output: 2 volts/cm

Strobe: 5 volts/cm



Single ended core read/write output in reference to strobe.

Time: 200 ns/cm

Core output: 2 volts/cm

Strobe: 5 volts/cm

Figure 5-1 Sense Amplifier Waveforms

For a 1, these show a half-sinusoid pulse of either polarity, approximately 350 to 400 MS long at its base, base, and superimposed on noise that occurs at the beginning and end of the read and write current waveforms. For a 0, only the noise is present; absence of the half-sinusoid indicates that the selected core has not changed state.

To check the slice waveform, an oscilloscope is connected to pin AM on the G005 modules. The oscilloscope should show a sense amplifier slice waveform, quiescent at + .05V, which falls to -3.5V whenever the preamp waveform has sufficient amplitude. Consequently, the level is +.05V for a 0 and -3.5V approximately 200 to 300 ns for a 1. Figure 5-2 shows the sense and slice waveforms for both 1 and 0 core outputs. Both of the above single-bit faults require replacement of the entire stock.

Single ended core with relationship to slice.

Time: 100 ns/cm
2 volts/cm

Figure 5-2 Sense Amplifier Slice Waveform

A single-bit pickup error throughout memory can also be caused by a faulty inhibit-driver output section or an open inhibit winding; a drop error similarly confined results from a faulty quadrant sense-amplifier preamps or an open sense line.

Failures in this class turn up initially with a single bit failing at a particular address. Then the problem is to determine whether the failure was due to a faulty bit or a faulty address. To make this determination, some test programs should be run; memory address tests, which sometimes will show up multiple addressing which checkerboard won't; checkerboard with sense amp margins; and block transfer tests.

While running checkerboard, vary sense amp margins until a particular bit begins to fail, then continue to move the voltage and see if the addresses on which the bit fails seem to stay concentrated on a single or a very small group of addresses and if other bits begin to fail quickly as the margin is increased. If they do, then the failure probably is an address failure and not a bit failure. If, however, the failure sticks to a single bit until the margins reach the normal failing points, then the failure is almost certain to be in the sense amplifier or inhibit rather than an address failure.

On the other hand, if many bits and large numbers of consecutive addresses fail, something common to the entire memory system is probably at fault, such as drivers, selectors, power supplies, address register, quadrant selection, segment selection for inhibit, if even or odd bits are dropping or picking up.

In the case of a bit failure, first try changing the sense amplifier and inhibit driver card for that bit.

5.8 ADDRESS FAILURES

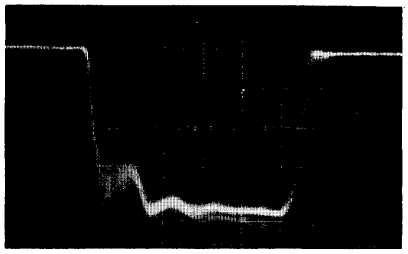
If the failure is always on one and only one address, until margins are varied up to the normal failure points, the failure must be in the stack. With a multiple address failure, the trouble is usually a balun card, G604 or G206. The fault may lie on a balun card other than the one pointed to by the address decoding points, beacuse these cards are connected in a matrix. All the cards on both selection axes should be checked by substitution.

If sense amp margins have no effect on a failure which looks like a bit failure, the failure is usually occurring in the MB flip-flop or the W102 board. If it is a single bit failure occurring only in every address of a single quadrant (determined by address bits 22 and 29) then there is most probably a wire broken; there are four sets of inhibit windings and four sets of sense amp windings to each module.

An open diode on a balun card will be pointed to by failures one every address on that selection line. A shorted or leaky diode will not be pointed to directly, as the address affected will probably appear to be all right and other addresses will appear to be failing. Be sure that you obtain a complete table of every address that fails, far enough into memory to obtain a pattern. This clue will enable you to pinpoint a particular G206 or balun (G604) failure and can be done, quickly and easily, using the checkerboard to inhibit address lines, or by halting on error and pressing CONTINUE. If the errors occur every fourth address or every 1000th address on the Y lines, exercise extreme caution. The error may only be in a single address, but it may be propagated throughout memory because the process by which the program loads the pattern. Address test may help here, but simple deposit examine may also be helpful.

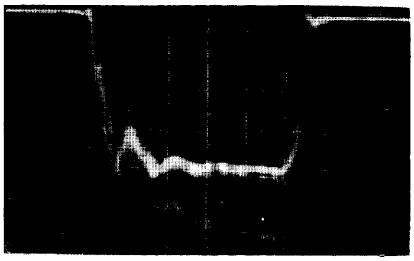
If the address failure pattern is random rather than patterned, there is a chance that the memory common driver G212 may be bad; or, if the failure has occurred throughout the entire word, then it probably is a control failure; i.e. the timing is off or there is a power supply problem. In this case, the bits may not be scattered evenly through the word. It might also be an address bit problem since the MAs are used to feed the G206. If this is the case, expect the failures to show up readily when that bit is inhibited on the checkerboard test.

The best way to test for problems on any of the modules, that have been mentioned so far, is by substitution. A good point at which to start checking bit multi-address failures is to take a current probe and check all the read and write currents while cycling through checkerboard using the test stubs provided for. Open circuits, either in the drivers or selector, will show up as complete absence of current. Photographs provided in Figure 5-3 show waveforms for some typical patterns. These are read and write current waveforms, sense amplifier waveforms and inhibit current waveforms. Generally speaking, the sense amplifier outputs, when looked at differentially, should be approximately 4V peak-to-peak.



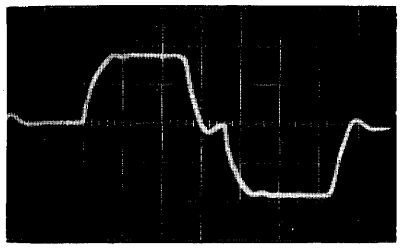
X read select current measured between pins 1F04S and 1F06M white bus.

Time: 100 ma/cm
100 ns/cm



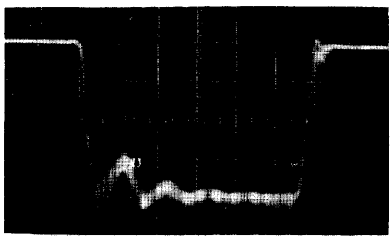
X read drive current measured between pins 1F06U and 1F09M white bus.

Time: 100 ma/cm
100 ns/cm



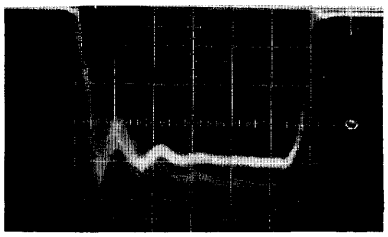
X read-write total current through the stack

Time: 200 ma/cm
200 ns/cm



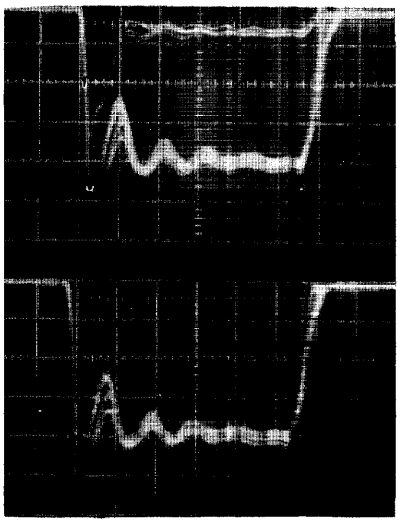
X write select current measured between pins 1F04V and 1F06N brown bus.

Time: 100 ma/cm
100 ns/cm



X write drive current measured between pins 1F06V and 1F09R brown bus.

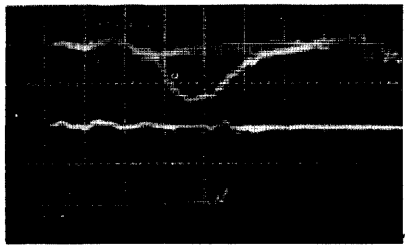
Time: 100 ma/cm
100 ns/cm



Open address on X write drive current.

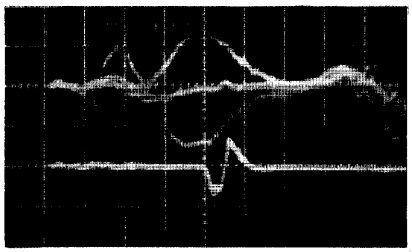
Normal X write drive current

Figure 5-3 Type 164 Memory System Waveforms (Sheet 1 of 2)



Single ended core with relationship to slice.

Time: 100 ns/cm
2 volts/cm



Single ended core read output in reference to strobe.

Time: 100 ns/cm

Core output: 2 volts/cm

Strobe: 5 volts/cm

Single ended core read/write output in reference to strobe.

Time: 200 ns/cm

Core output: 2 volts/cm

Strobe: 5 volts/cm

Total inhibit current with relationship to total read/write current.

Time: 200 ma/cm
200 ns/cm

Total inhibit current measured from the resistor panel reference, with time pulse 3.

Time: 200 ns/cm
100 ma/cm

Time Pulse 3: 2 volts/cm

Figure 5-3 Type 164 Memory System Waveforms (Sheet 2 of 2)

5.9 TUNE-UP PROCEDURE

This procedure should only have to be followed, if the stack or power supply regulator cards have been replaced or if someone has misadjusted all the knobs on the power supply; under no circumstances should the balance pots on the sense amplifier cards be touched out in the field.

On the back of the power supply, there is a label giving read-write voltage, inhibit voltage, slice voltage, first and second stage clamp voltages; the memory was set to these when voltages left the plant. A good starting point when reregulating is to set the voltages to these values. Inhibit voltage should be 52-55V, read-write voltage should be 63-65V, and slice should be set at +5.5 to 5.9V at pin AV of the sense amplifiers. The read-write should never be over 70V or below 60V; the inhibit should never be above 60 or below 50V. If these limits are exceeded, the memory simply will run with errors; no damage will be done.

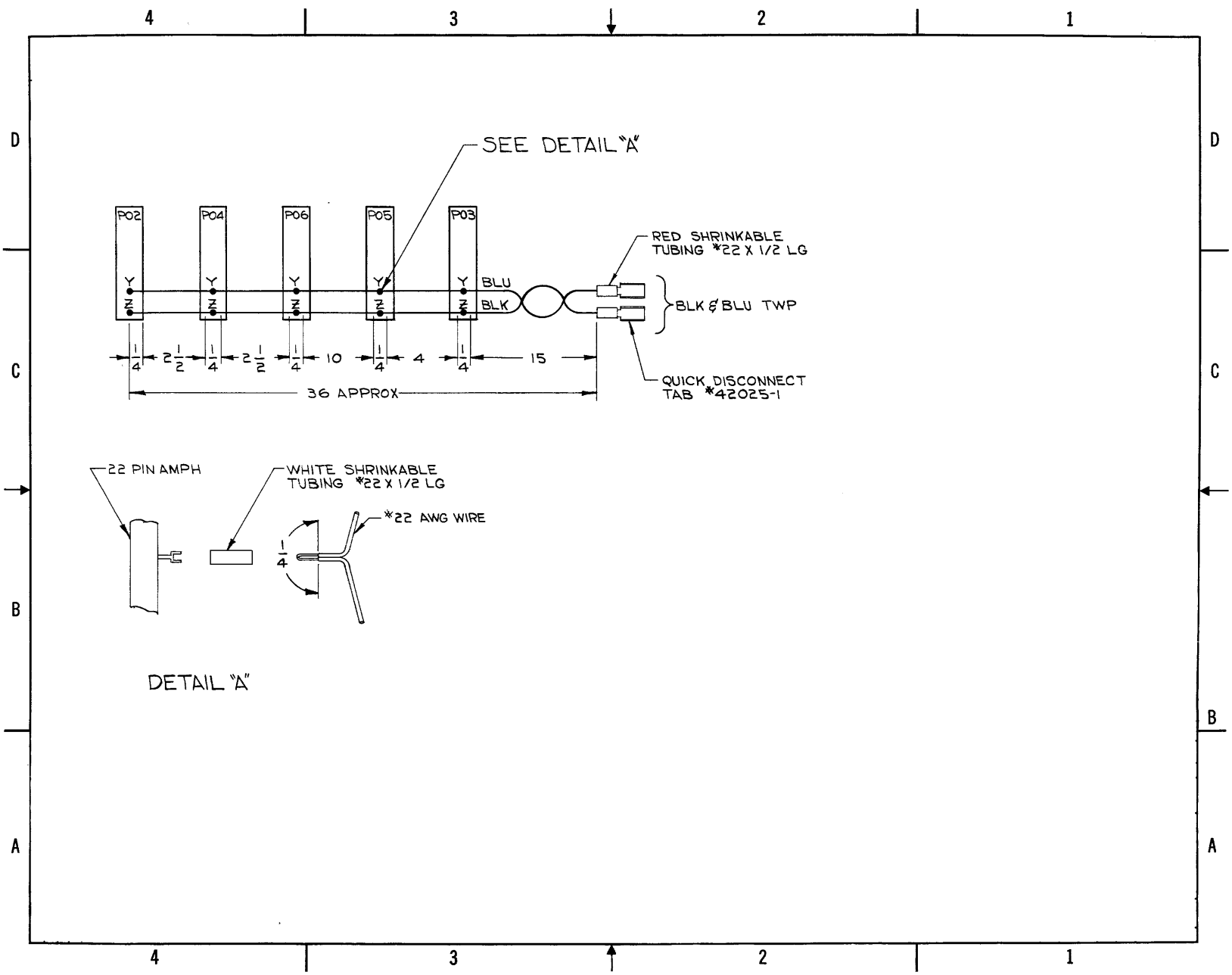
When the voltages are set as described, start moving the sense amp margins using checkerboard. Adjust the read-write voltage for maximum positive margin, and the inhibit voltage for maximum negative margin. Don't worry if the margins are not balanced as long as failure points can be detected on both ends. If failure points cannot be detected, adjust the slice voltage to move the margins so that failure points can be detected and continue tuning. The last thing to be done is adjusting the slice for balanced positive and negative margins. Remember that by using this procedure margins are being optimized for a checkerboard pattern; other patterns will have different margins. Next, look at the slice output pin AM on any sense amp, while simultaneously looking at strobe. Strobe should be about in the middle of the sliced output; if it is offset, the margin range will be too narrow.

CHAPTER 6
ENGINEERING DRAWINGS

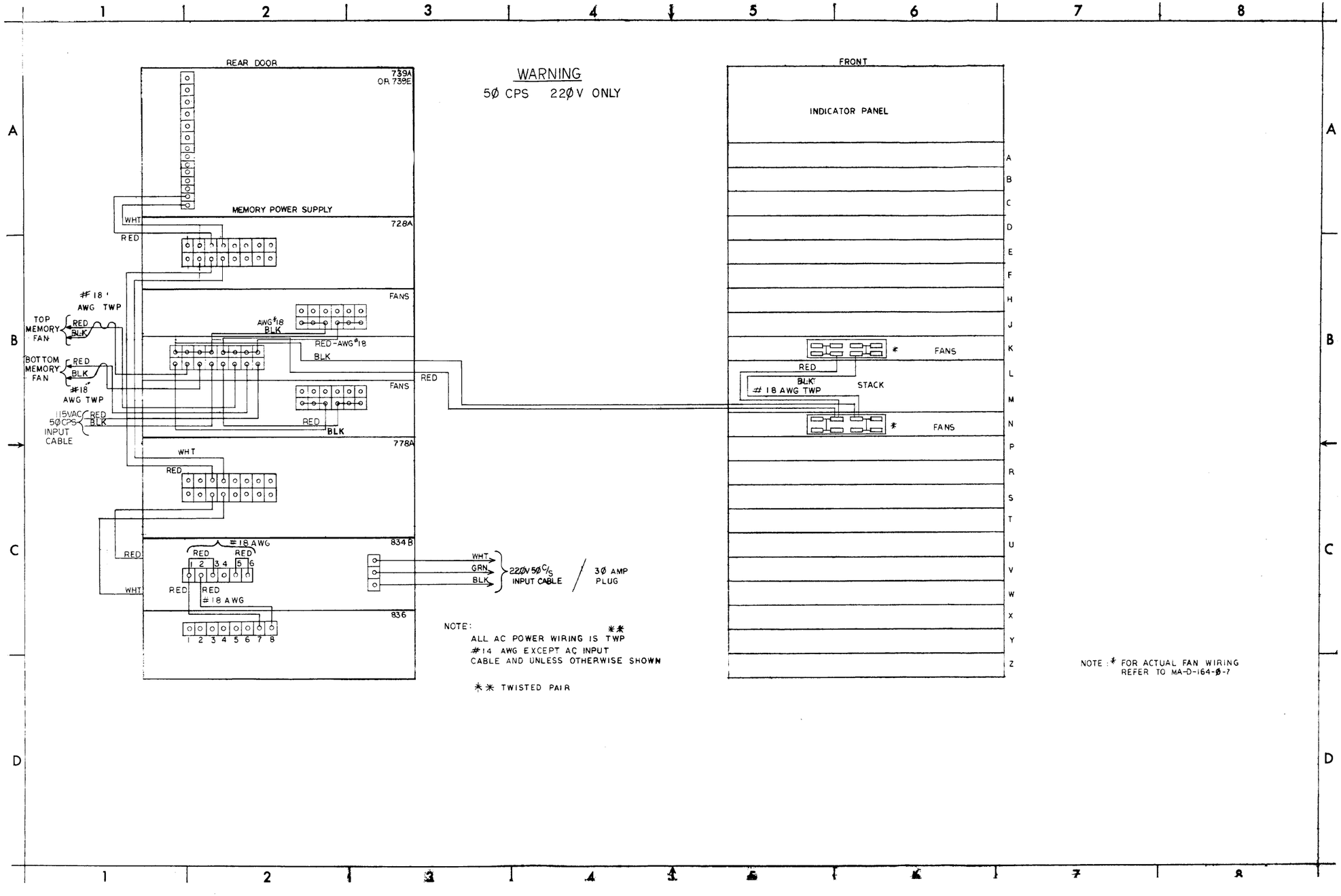
This chapter contains copies of all of the engineering drawings and replacement schematics necessary to understand and maintain the Type 164 Memory System. The engineering drawings in this chapter are in addition to the complete set of full-size drawings supplied with each system; should any discrepancy exist between the drawings in this manual and those supplied with the equipment, assume the drawings supplied with the equipment are correct. The drawings supplied should be used by maintenance personnel when working on the memory, because they show variations peculiar to an individual installation. Replacement schematics are furnished for test and maintenance purposes. The circuits on these drawings are proprietary in nature and should be treated accordingly.

The engineering drawings* appear in the order listed below.

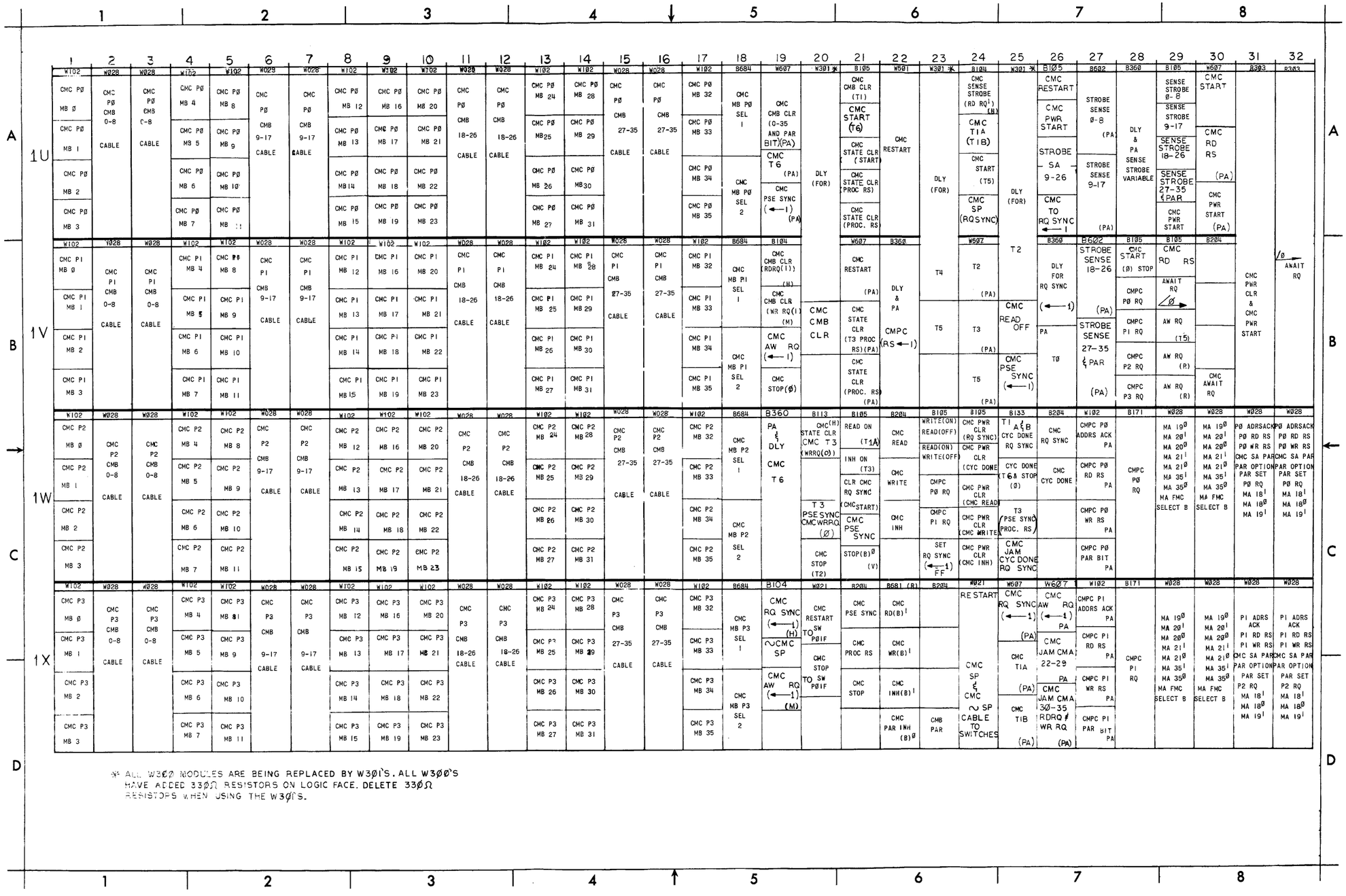
*Standard DEC drawing terminology is used in the drawings contained in this chapter. For an explanation of DEC logic, symbology, and information on the drawings, the reader can refer to Chapter 4 of this manual and Appendix 1 of the Arithmetic Processor 166 Instruction Manual, F-67 (166).



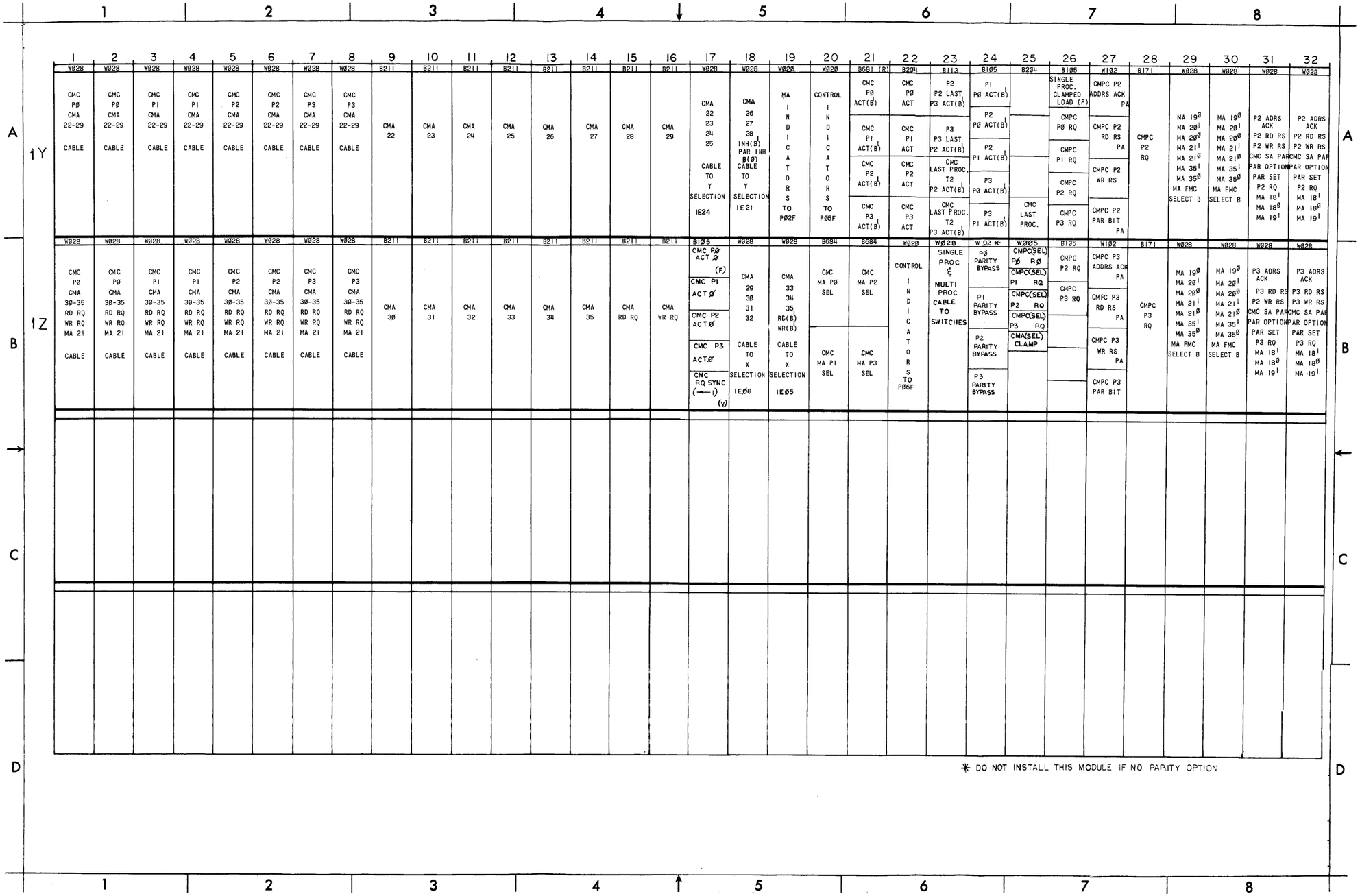
PW-C-164-0-IPW Indicator Power Wiring



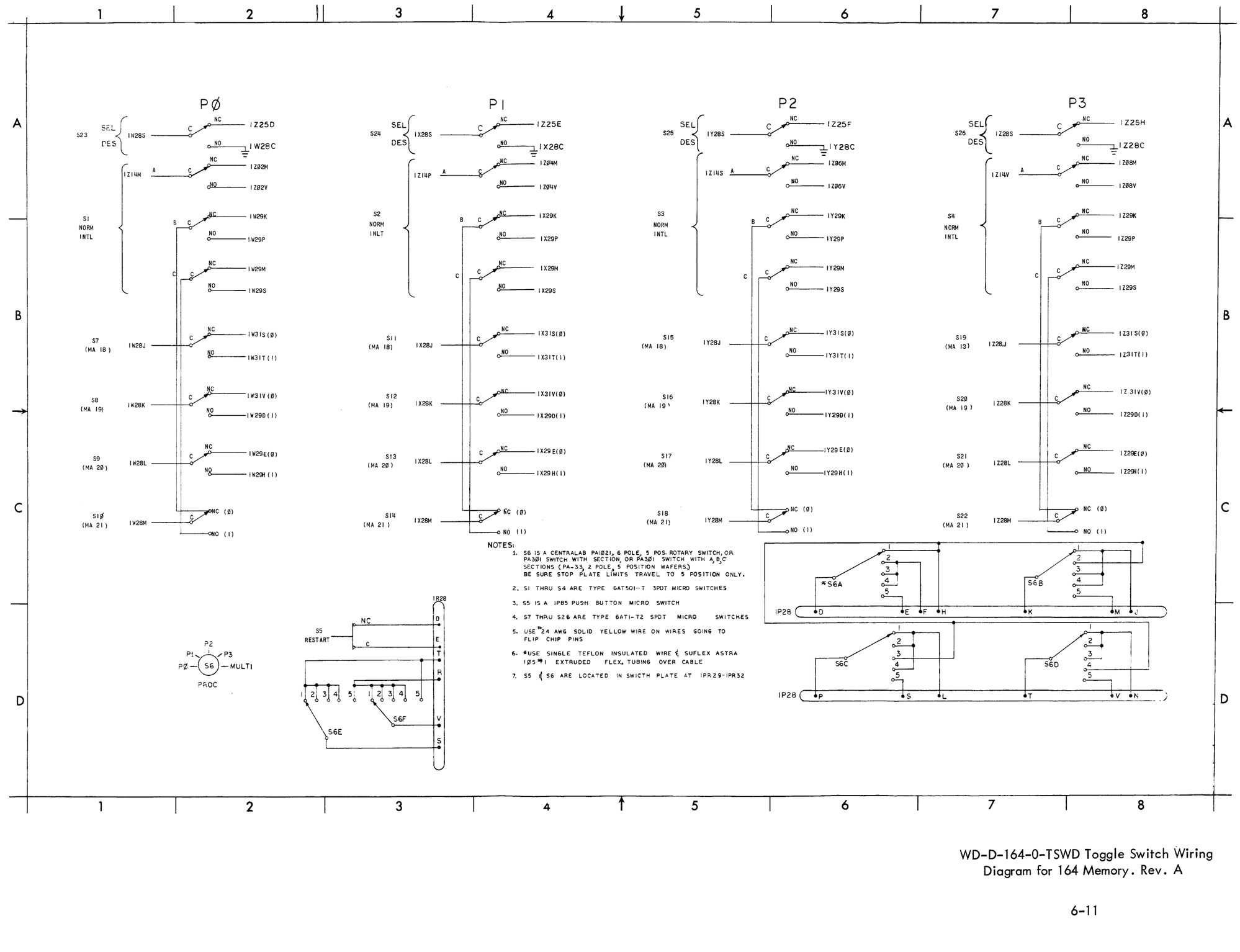
PW-D-164-0-50ACPW AC Power Wiring



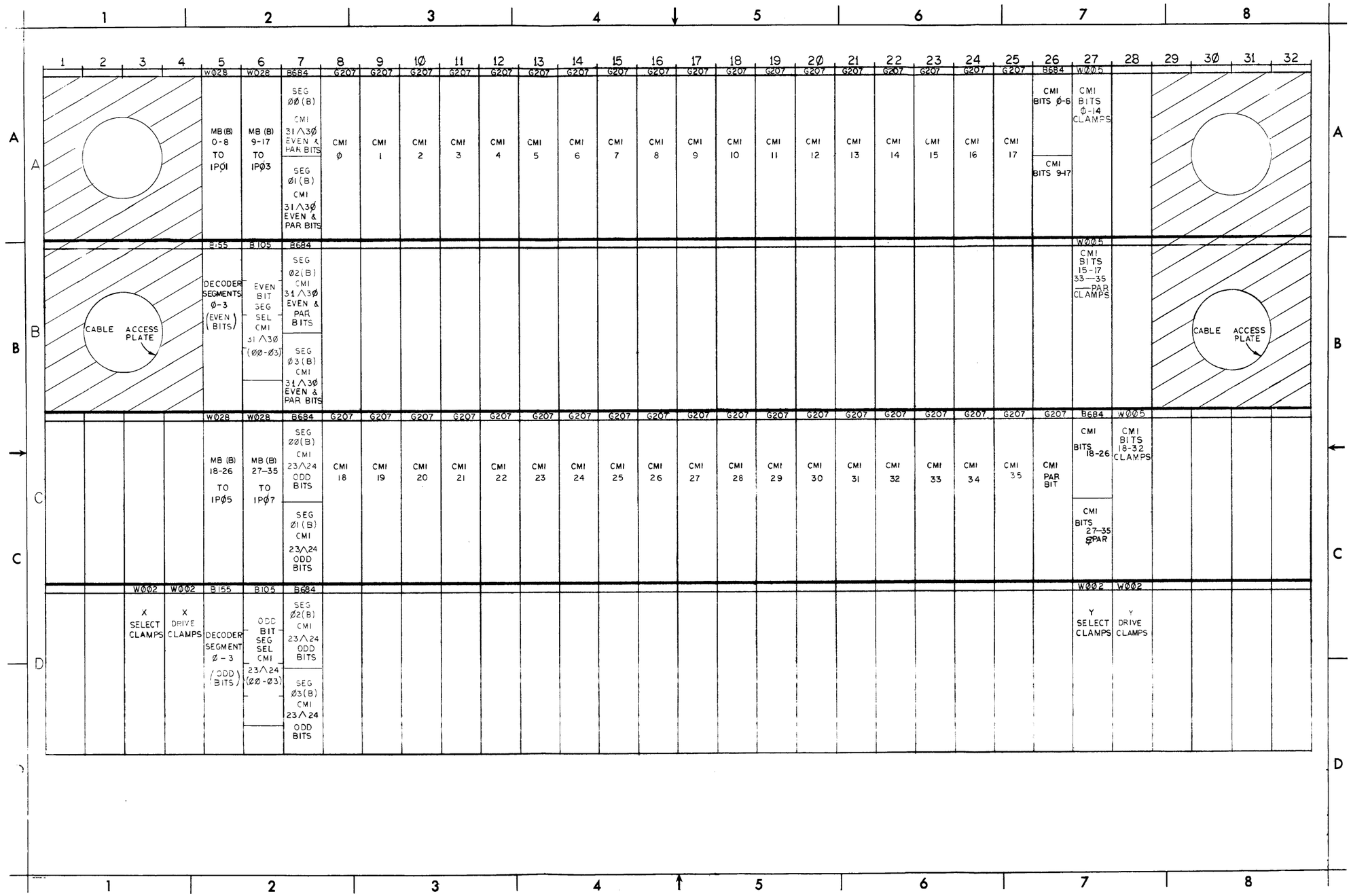
UML-D-164-0-11 Utilization Module List Control and Interface (Part 1). Rev. C



UML-D-164-0-11 Utilization Module List Control and Interface (Part 2). Rev. C



WD-D-164-0-TSWD Toggle Switch Wiring Diagram for 164 Memory. Rev. A

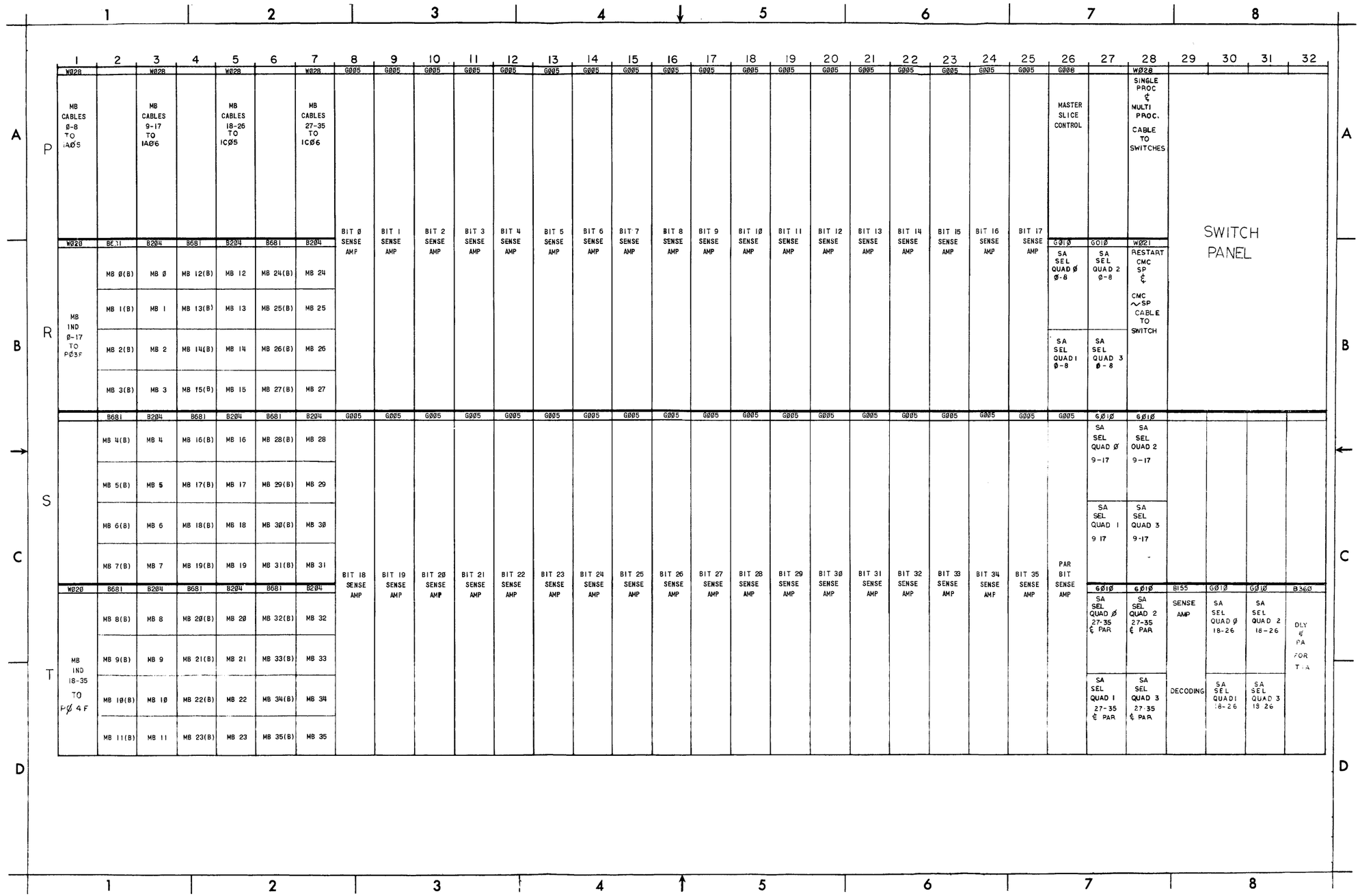


UML-D-164-0-UML-1 Utilization Module
List Inhibit

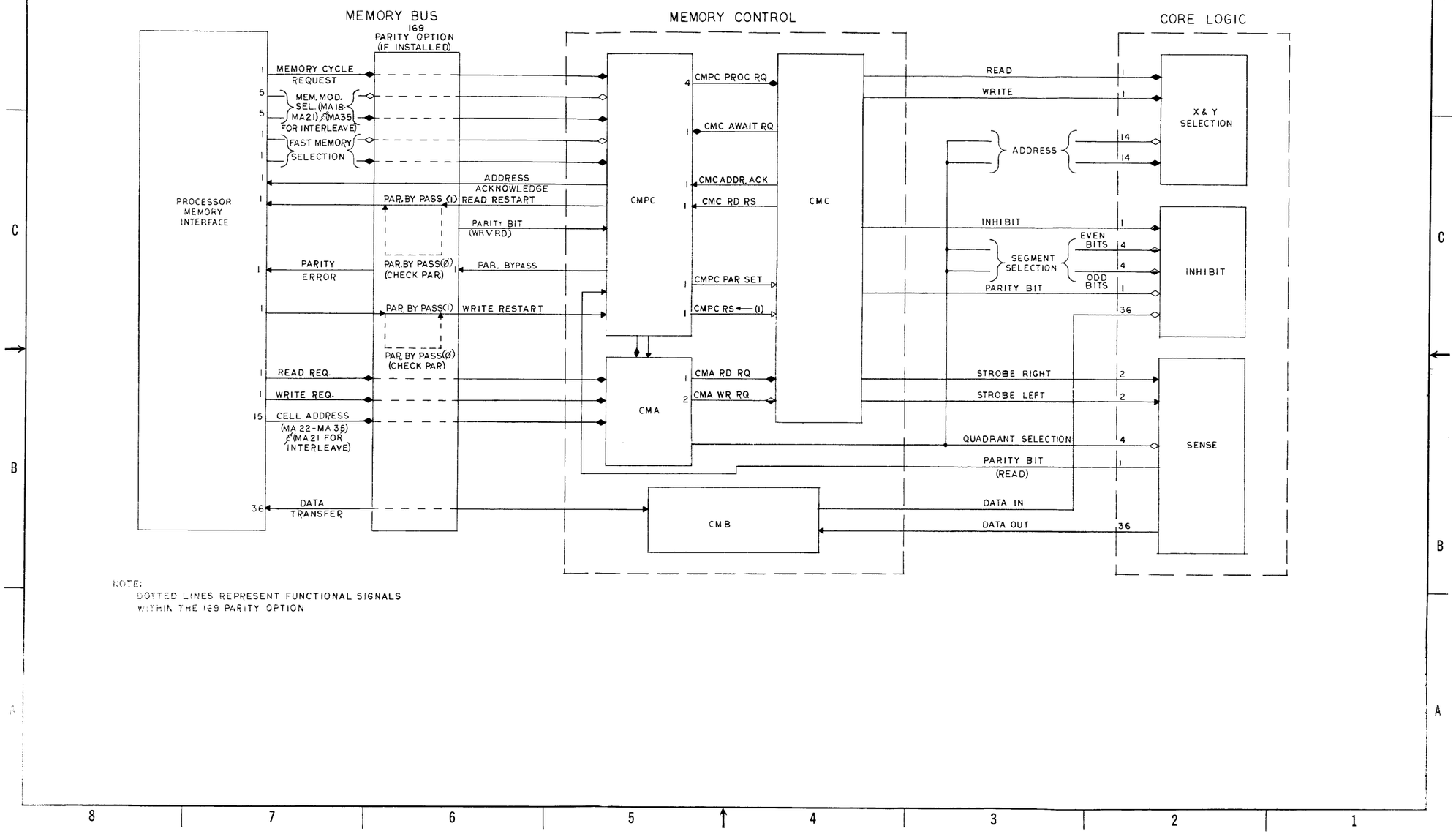
DOUBLE MODULE

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
G206	G206	G206	G206	W028	G212		W028	G206	G206	G206	G206	G206	G206	G206	G206	G206	G206	G206	G206	W028	G212		W028	G206	G206	G206	G206	G206	G206	G206	G206
ADDR Ø 1 XS	ADDR 2 3 XS	ADDR 4 5 XS	ADDR 6 7 XS	MAB S 33 34 35 RD(B)(1) WR(B)(1) TO 1Z19	X -R/W FUSE SWITCH X +R/W FUSE SWITCH		MAB S 29 30 31 32 FOR X SEL TO 1Z18 B684 RD B(1) X WR B(1) X	ADDR Ø-7 1Ø-17 XD	ADDR 2Ø-27 3Ø-37 XD	ADDR 4Ø-47 5Ø-57 XD	ADDR 6Ø-67 7Ø-77 XD	ADDR 1ØØ-1Ø7 11Ø-117 XD	ADDR 12Ø-127 13Ø-137 XD	ADDR 14Ø-147 15Ø-157 XD	ADDR 16Ø-167 17Ø-177 XD	ADDR Ø 1 YS	ADDR 2 3 YS	ADDR 4 5 YS	ADDR 6 7 YS	MAB S 26 27 28 INH(B)1 PARINH(B) TO 1Y18 Ø	Y -R/W FUSE SWITCH Y +R/W FUSE SWITCH		MAB S 22 23 24 25 FOR Y SEL. TO 1Y17 B684 RD B(1) Y WR B(1) Y	ADDR Ø-7 1Ø-17 YD	ADDR 2Ø-27 3Ø-37 YD	ADDR 4Ø-47 5Ø-57 YD	ADDR 6Ø-67 7Ø-77 YD	ADDR 1ØØ-1Ø7 11Ø-117 YD	ADDR 12Ø-127 13Ø-137 YD	ADDR 14Ø-147 15Ø-157 YD	ADDR 16Ø-167 17Ø-177 YD
G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604
ADDR Ø-3 X-SEL.	ADDR 1Ø-13 X SEL.	ADDR 2Ø-23 X SEL.	ADDR 3Ø-33 X SEL.	ADDR 4Ø-43 X SEL.	ADDR 5Ø-53 X SEL.	ADDR 6Ø-63 X SEL.	ADDR 7Ø-73 X SEL.	ADDR 1ØØ-1Ø3 X SEL.	ADDR 11Ø-1Ø3 X SEL.	ADDR 12Ø-123 X SEL	ADDR 13Ø-133 X SEL	ADDR 14Ø-143 X SEL	ADDR 15Ø-153 X SEL	ADDR 16Ø-163 X SEL	ADDR 17Ø-173 X SEL	ADDR Ø-3 Y SEL	ADDR 1Ø-13 Y SEL	ADDR 2Ø-23 Y SEL	ADDR 3Ø-33 Y SEL	ADDR 4Ø-43 Y SEL	ADDR 5Ø-53 Y SEL	ADDR 6Ø-63 Y SEL	ADDR 7Ø-73 Y SEL	ADDR 1ØØ-1Ø3 Y SEL	ADDR 11Ø-113 Y SEL	ADDR 12Ø-123 Y SEL	ADDR 13Ø-133 Y SEL	ADDR 14Ø-143 Y SEL	ADDR 15Ø-153 Y SEL	ADDR 16Ø-163 Y SEL	ADDR 17Ø-173 Y SEL
G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604	G604
ADDR 4 7 X SEL	ADDR 14-17 X SEL	ADDR 24-27 X SEL	ADDR 34-37 X SEL	ADDR 44-47 X SEL	ADDR 54-57 X SEL	ADDR 64-67 X SEL	ADDR 74-77 X SEL	ADDR 1Ø4-1Ø7 X SEL	ADDR 114-117 X SEL	ADDR 124-127 X SEL	ADDR 134-137 X SEL	ADDR 144-147 X SEL	ADDR 154-157 X SEL	ADDR 164-167 X SEL	ADDR 174-177 X SEL	ADDR 4-7 Y SEL	ADDR 14-17 Y SEL	ADDR 24-27 Y SEL	ADDR 34-37 Y SEL	ADDR 44-47 Y SEL	ADDP 54-57 Y SEL	ADDR 64-67 Y SEL	ADDR 74-77 Y SEL	ADDR 1Ø4-1Ø7 Y SEL	ADDR 114-117 Y SEL	ADDR 124-127 Y SEL	ADDR 134-137 Y SEL	ADDR 144-147 Y SEL	ADDR 154-157 Y SEL	ADDR 164-167 Y SEL	ADDR 174-177 Y SEL

UML-D-164-0-UML-2 Utilization Module List
Memory Selector and Diode Matrices. Rev. A

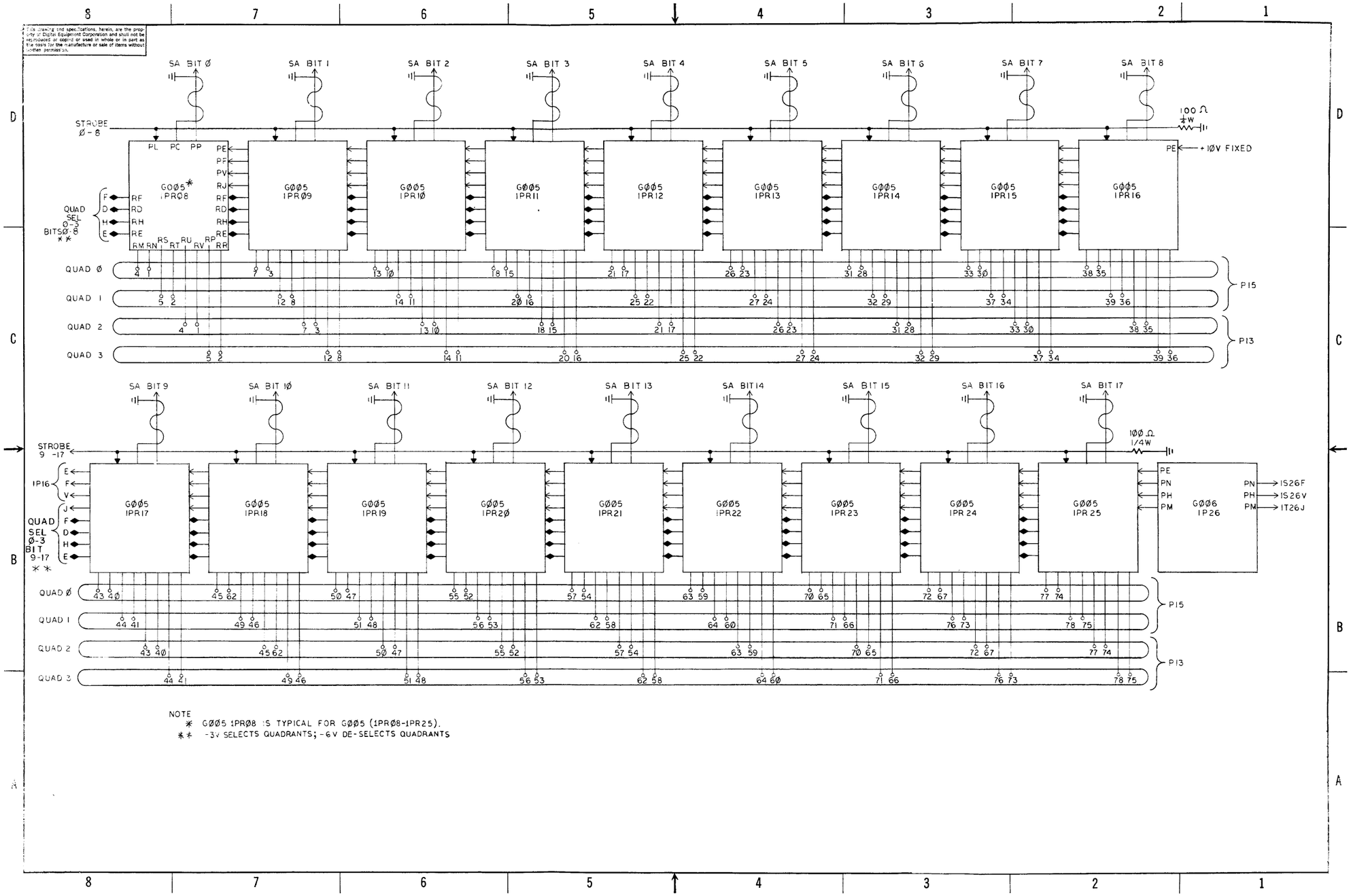


UML-D-164-0-3 Utilization Module List Sense Amps and MBs 164 Memory System. Rev. A

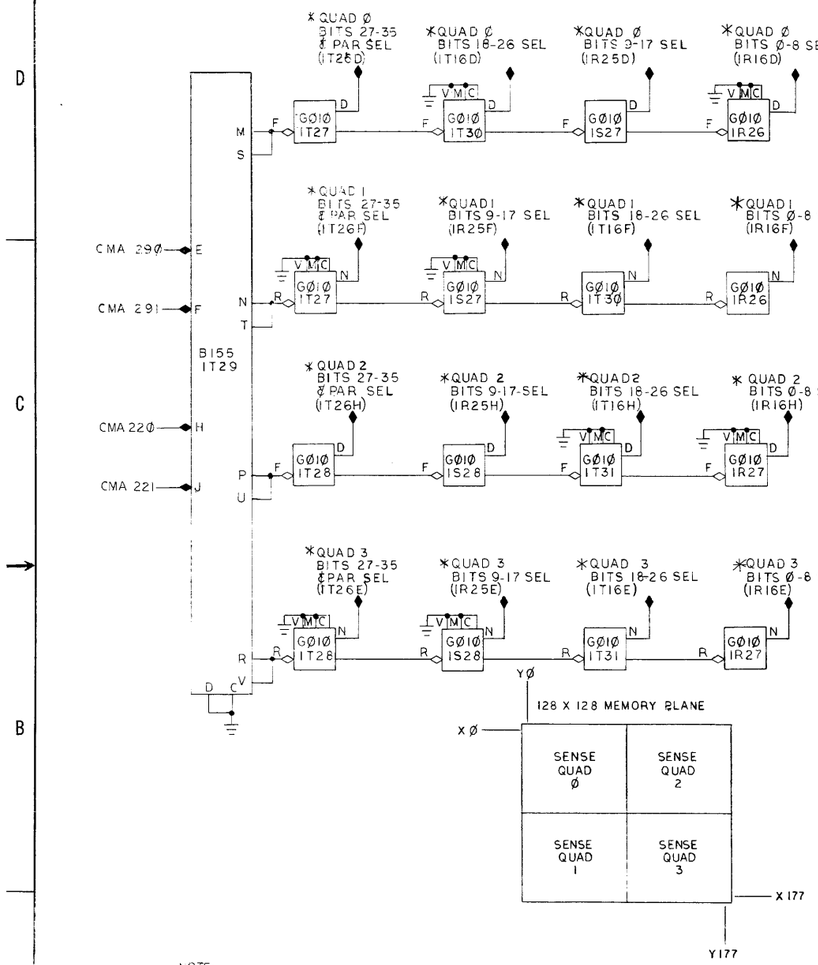


NOTE:
DOTTED LINES REPRESENT FUNCTIONAL SIGNALS
WITHIN THE 169 PARITY OPTION

SD-D-164-0-SBD System Block Diagram

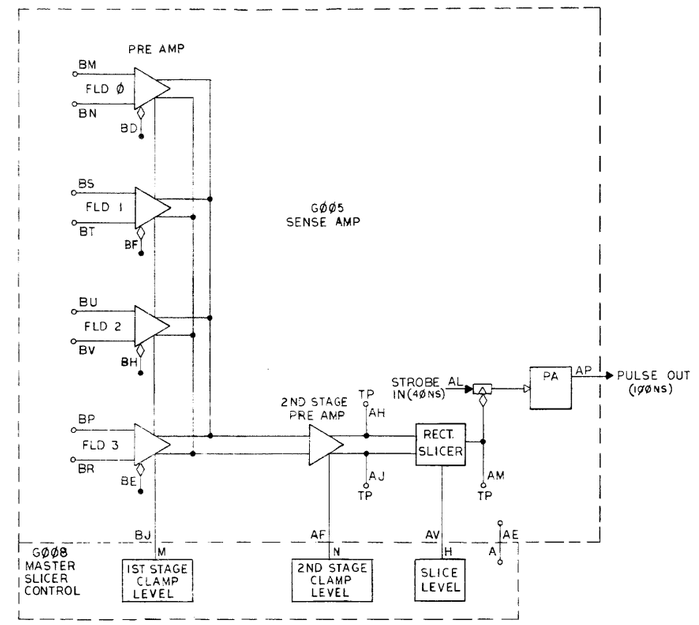


NOTE
* G005 1PRØ8 IS TYPICAL FOR GØØ5 (1PRØ8-1PR25).
** -3V SELECTS QUADRANTS; -6V DE-SELECTS QUADRANTS



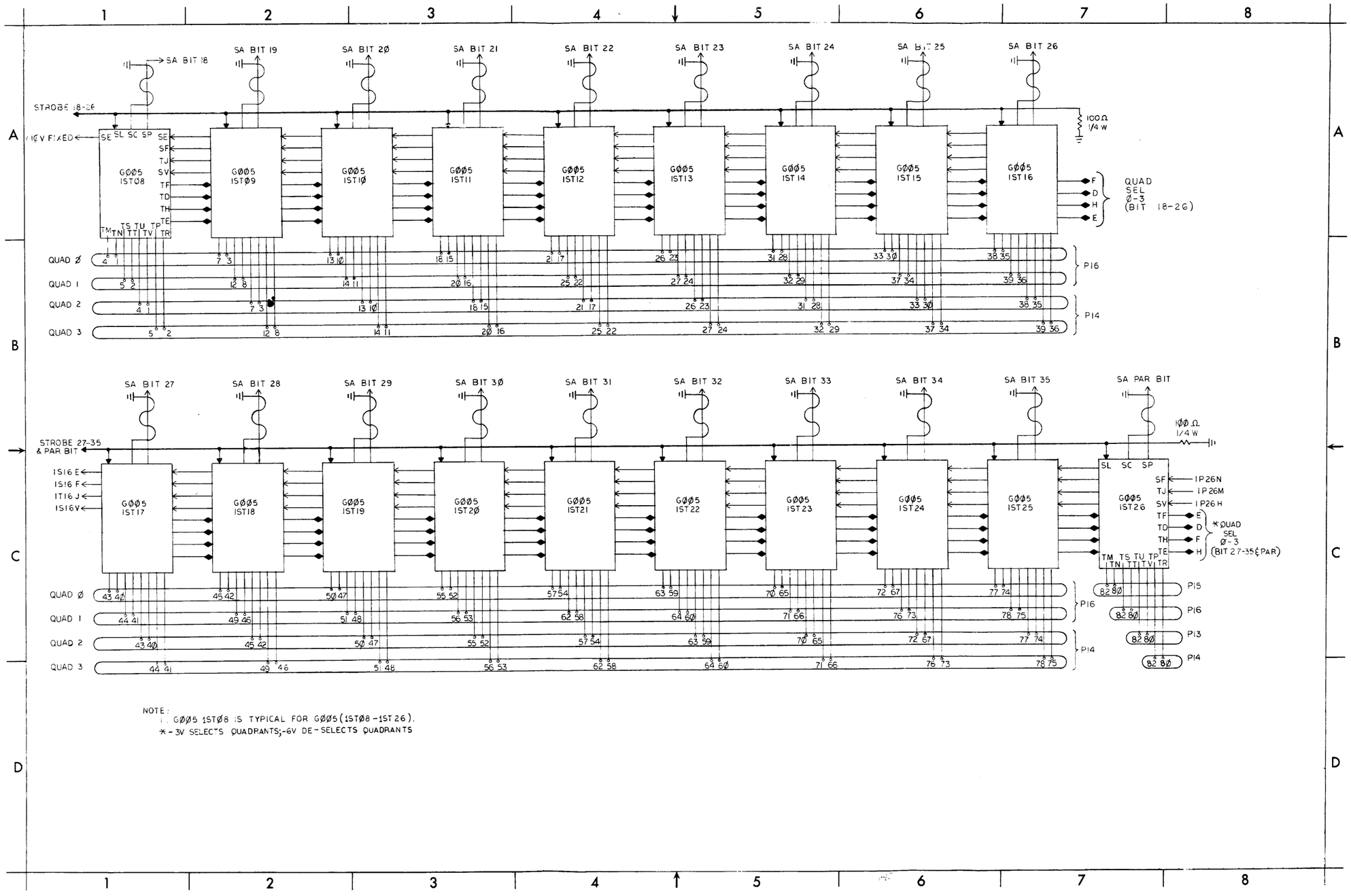
NOTE:

* QUAD SEL. LEVELS ARE -3V
DESELECT LEVELS ARE -6V.



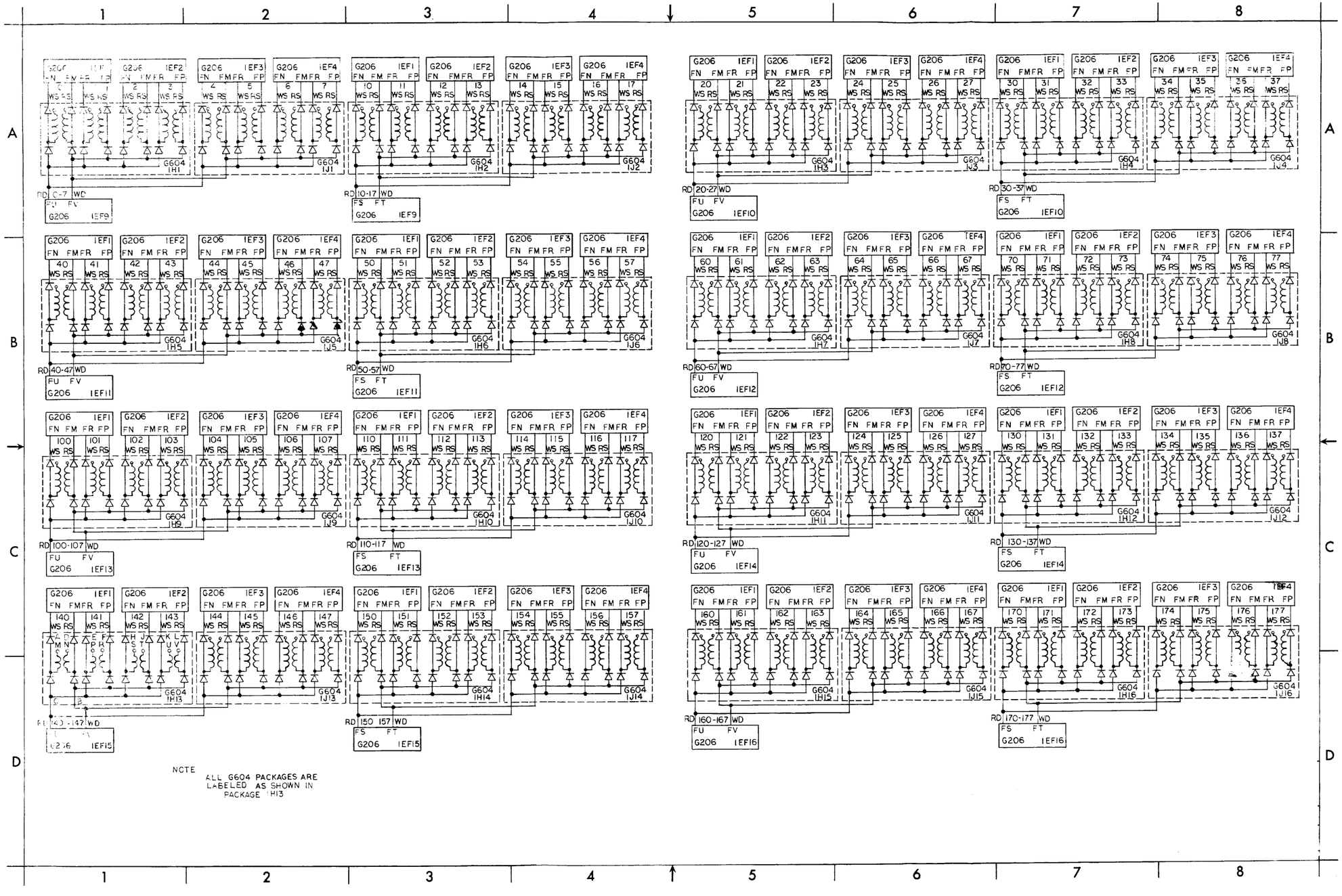
MASTER SLICER CONTROL MEASUREMENTS

	REFERENCE	MEASURE BETWEEN PINS		
*1 STAGE CLAMP	-15V	IP26B	IP26M	3.7V TO 4.0V (FIXED)
*2 STAGE CLAMP	-15V	IP26B	IP26N	8.0V
SLICE LEVEL	+10V	IP26A	IP26H	5.5V TO 5.9V



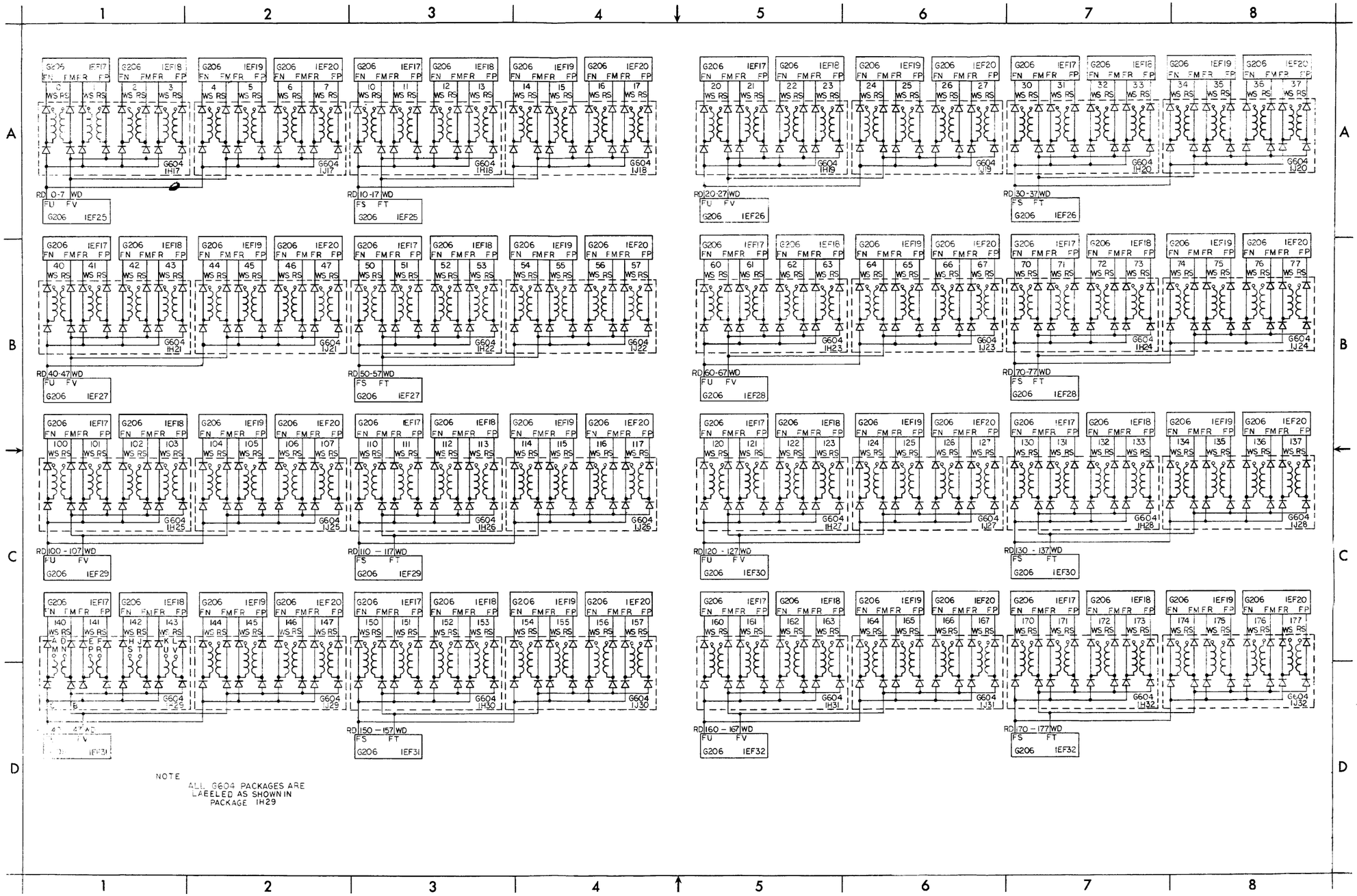
NOTE:
1. GØØ5 1STØ8 IS TYPICAL FOR GØØ5 (1STØ8 - 1ST26).
* - 3V SELECTS QUADRANTS; -6V DE-SELECTS QUADRANTS

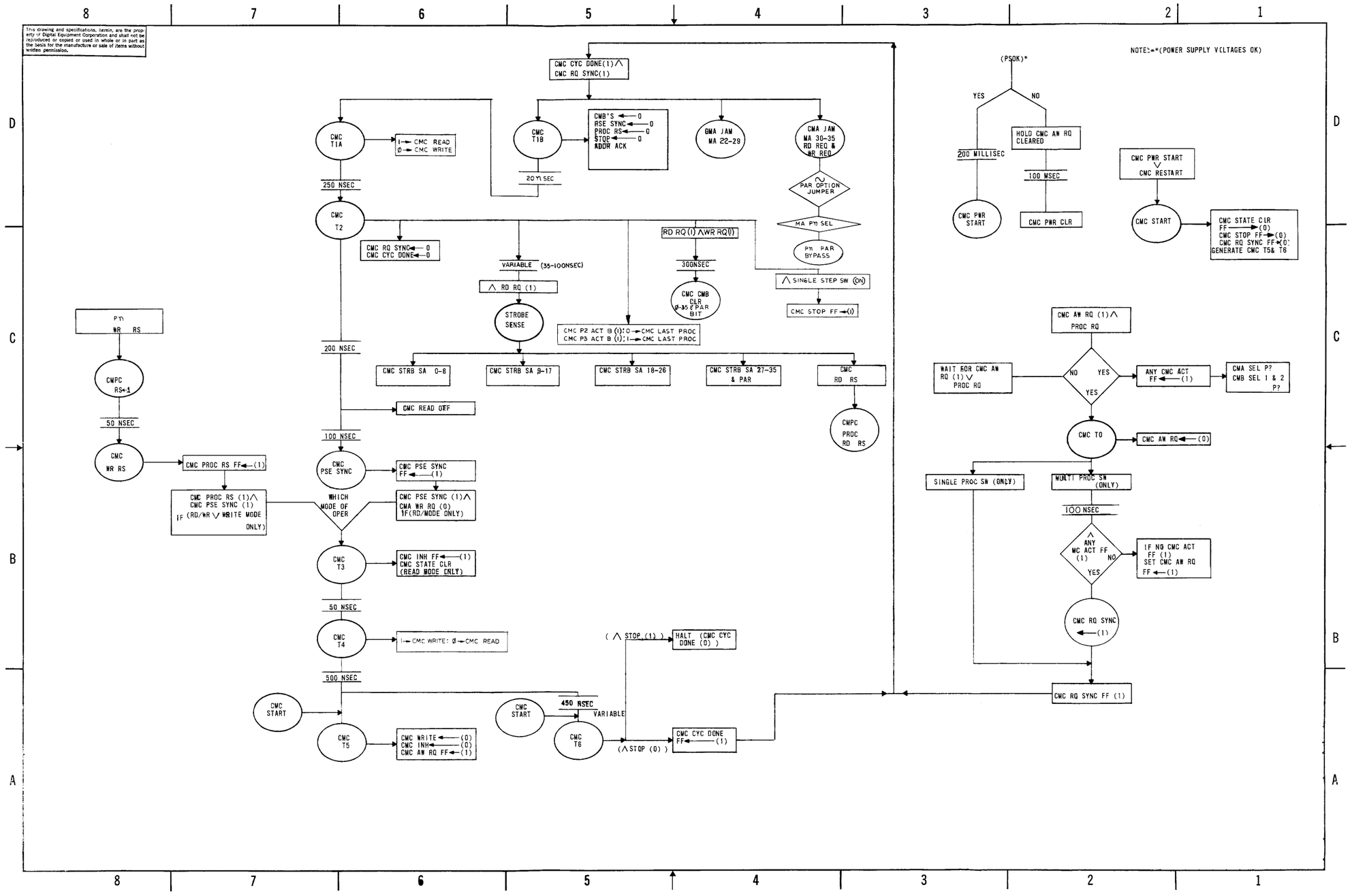
BS-D-164-0-MSSA-2 Sense Amplifier Bits 18-35 and Parity Bit

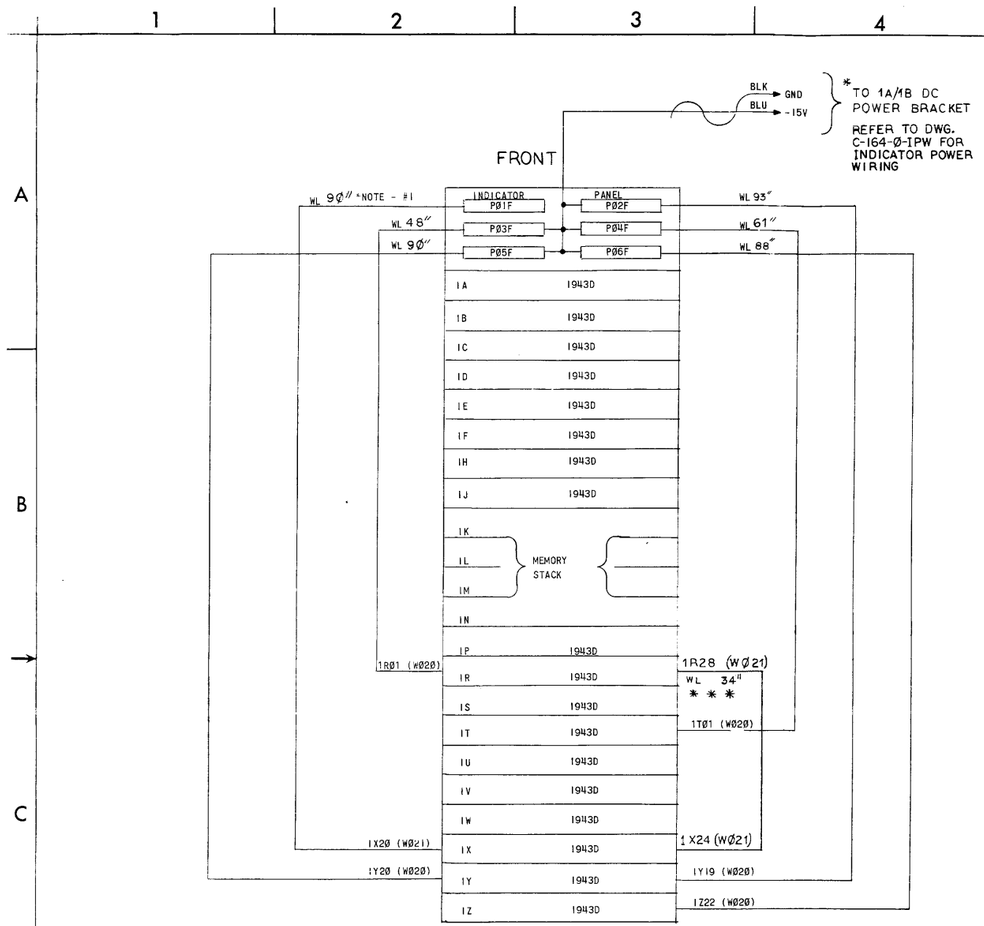


NOTE

ALL G604 PACKAGES ARE LABELED AS SHOWN IN PACKAGE IH13


1
2
3
4
5
6
7
8
A
B
C
D
G206 1EF17 FN FM FR FP
G206 1EF18 FN FM FR FP
G206 1EF19 FN FM FR FP
G206 1EF20 FN FM FR FP
WS RS
G604 1H17
G604 1J17
G604 1H18
G604 1J18
G604 1H19
G604 1J19
G604 1H20
G604 1J20
G604 1H21
G604 1J21
G604 1H22
G604 1J22
G604 1H23
G604 1J23
G604 1H24
G604 1J24
G604 1H25
G604 1J25
G604 1H26
G604 1J26
G604 1H27
G604 1J27
G604 1H28
G604 1J28
G604 1H29
G604 1J29
G604 1H30
G604 1J30
G604 1H31
G604 1J31
G604 1H32
G604 1J32
RD 0-7 WD
RD 10-17 WD
RD 20-27 WD
RD 30-37 WD
RD 40-47 WD
RD 50-57 WD
RD 60-67 WD
RD 70-77 WD
RD 100-107 WD
RD 110 — 117 WD
RD 120-127 WD
RD 130-137 WD
RD 150 — 157 WD
RD 160 — 167 WD
RD 170 — 177 WD
FU FV
FS FT
G206 1EF25
G206 1EF26
G206 1EF27
G206 1EF28
G206 1EF29
G206 1EF30
G206 1EF31
G206 1EF32
NOTE
ALL G604 PACKAGES ARE LABELED AS SHOWN IN PACKAGE 1H29





NOTES:

* 1. P01F IS A 12 PIN AMPHENOL FEMALE PLUG USING SINGLE TEFLON INSULATED WIRES TO W021 (REFER TO NOTE #5.)

2. P02F THRU P06F ARE 22 PIN AMPHENOL FEMALE PLUGS USING SINGLE TEFLON INSULATED WIRES TO W020. (REFER TO NOTE #5)

3. WL - WIRE LENGTH

4. A. PIN Z OF P02F THRU P06F ARE BUSSED TOGETHER BY TWP (BLK).

   B. PIN Y OF P02F THRU P06F ARE BUSSED TOGETHER BY TWP (BLU).

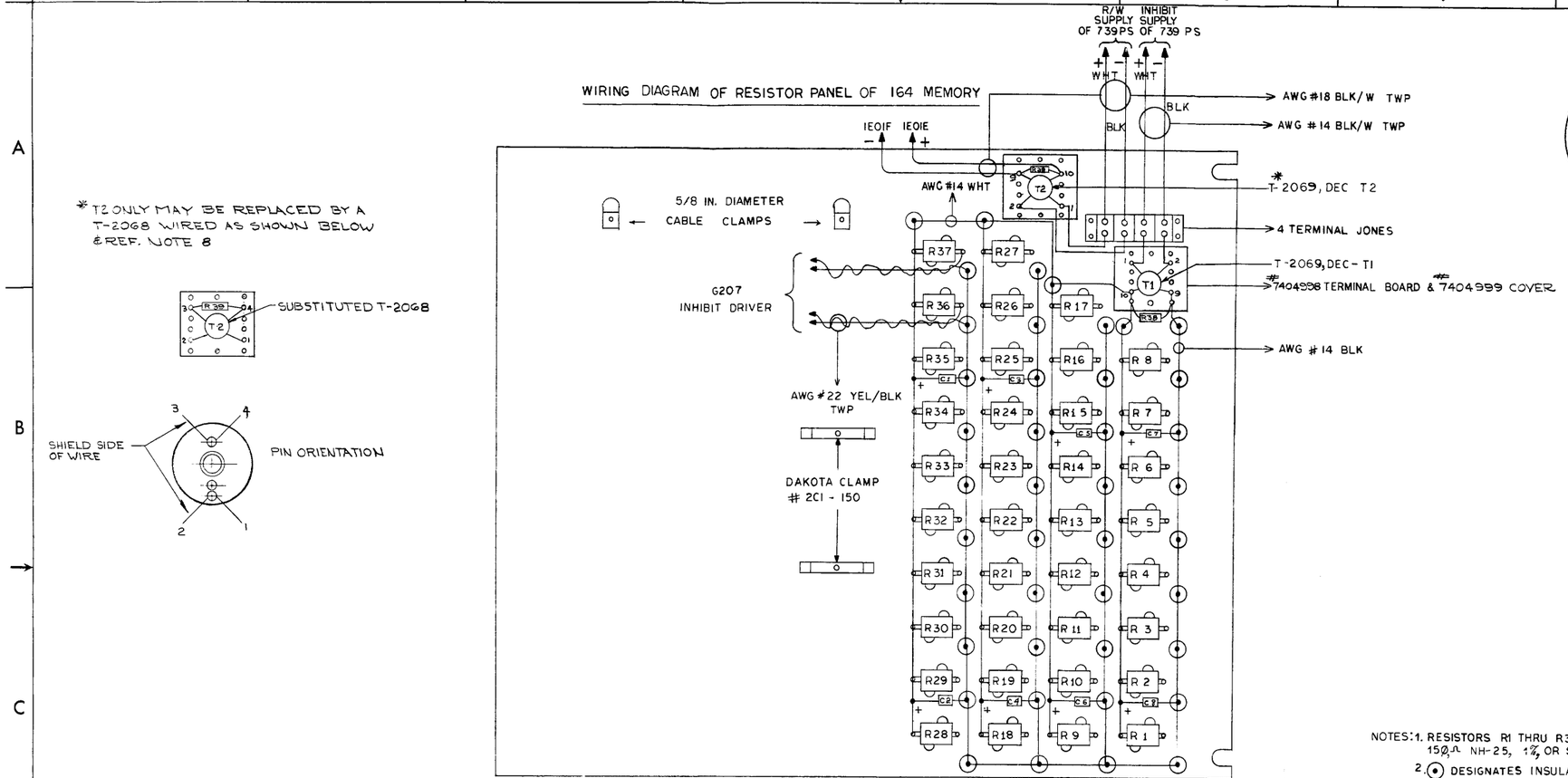
   C. WIRE TWP BLU/BLK FROM P05F TO POWER CONNECTOR BRACKET.

** 5. USE SUFLEX ASTRA 105 #1 EXTRUDED FLEX TUBING.

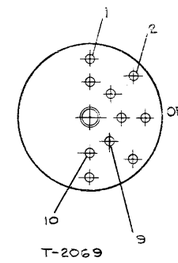
*** 6. USE SINGLE TEFLON INSULATED WIRES PER NOTE 5

CD-D-164-0-ICD Indicator Switch
Cable Diagram. Rev. A

WIRING DIAGRAM OF RESISTOR PANEL OF 164 MEMORY

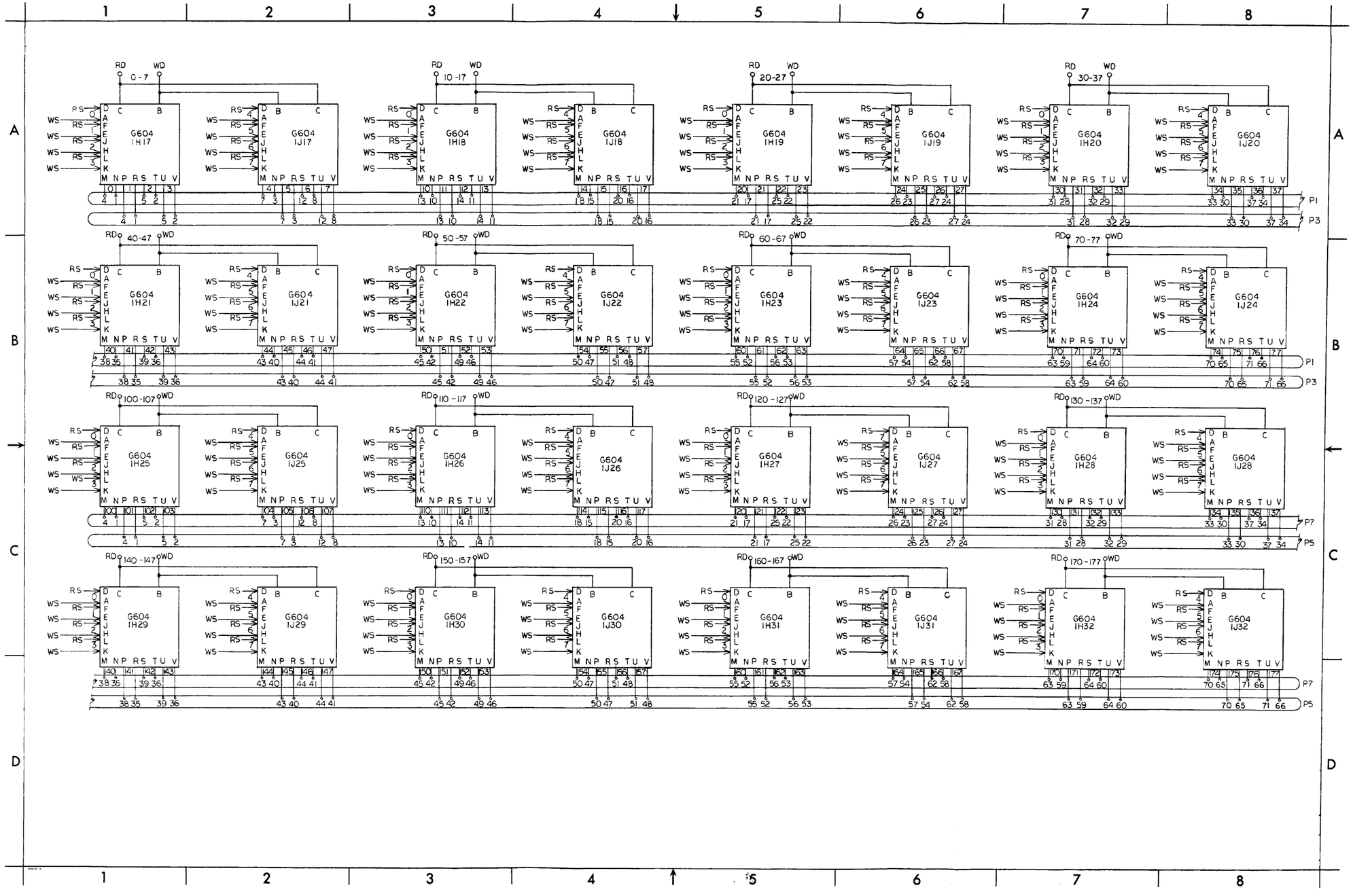


* T2 ONLY MAY BE REPLACED BY A T-2068 WIRED AS SHOWN BELOW & REF. NOTE 8

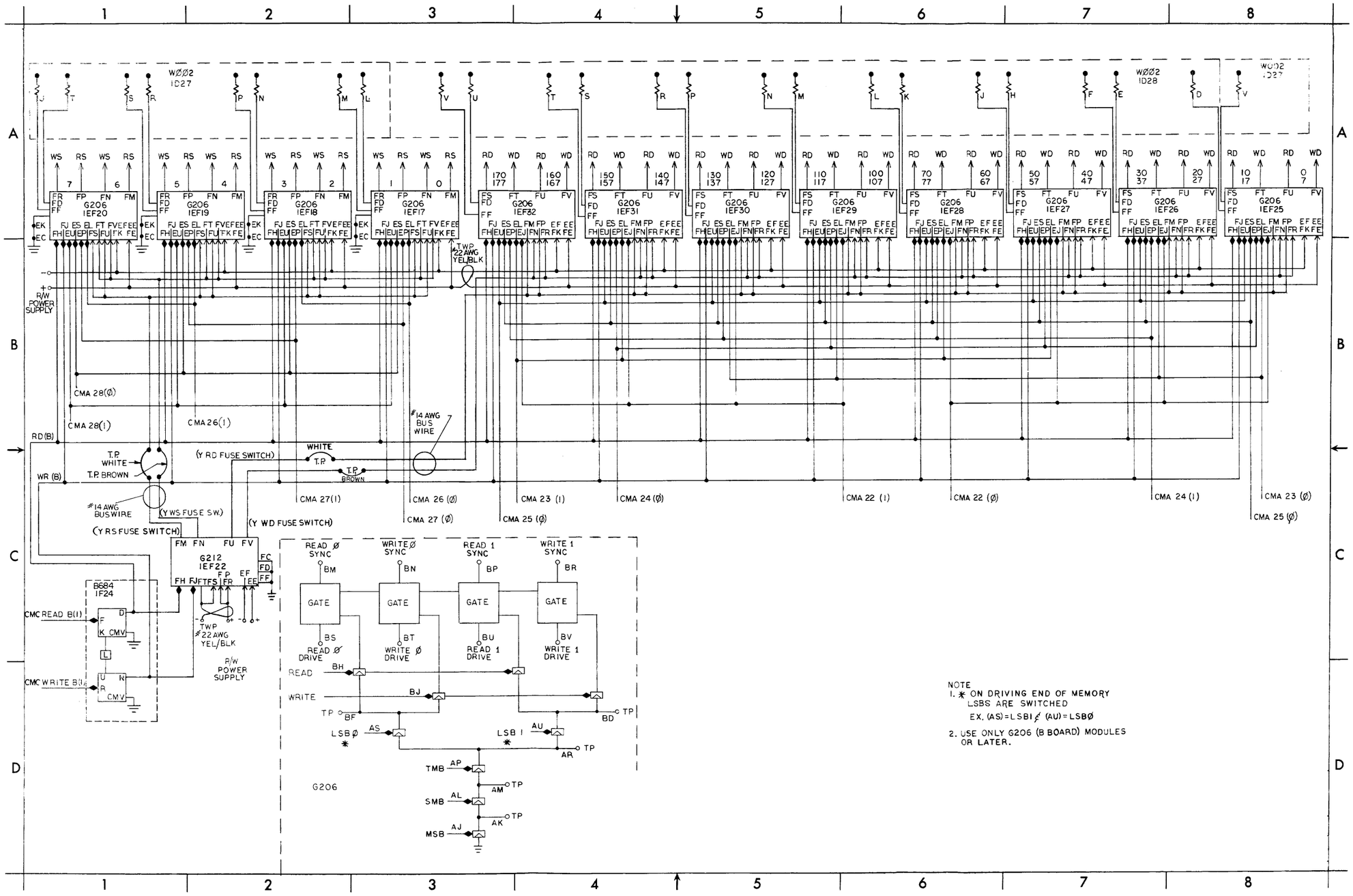


NOTES:
1. RESISTORS R1 THRU R37 ARE DALE 150Ω NH-25, 1%, OR SAGE 3225 NM, 150Ω, 1%.
2. ⊙ DESIGNATES INSULATED SPADE STANDOFF * 4-40 THD, WINCHESTER #753
3. ALL CAPACITORS ARE 1 μF, 150V, WITH INSULATION PLACED OVER LEADS.
4. YEL/BLK TWISTED PAIRS TO APPROPRIATE INHIBIT DRIVERS FROM ALL RESISTORS
5. USE SILICON GREASE WHEN MOUNTING 150Ω RESISTORS
6. R38 & R39 ARE OHMITE 6000Ω 10W RES
7. FOR ASSEMBLY REFER TO MAD-D-164-0-4
8. COVER LEADS #2 AND #3 ON T2 WITH #16 AWG BLK INSULATION.

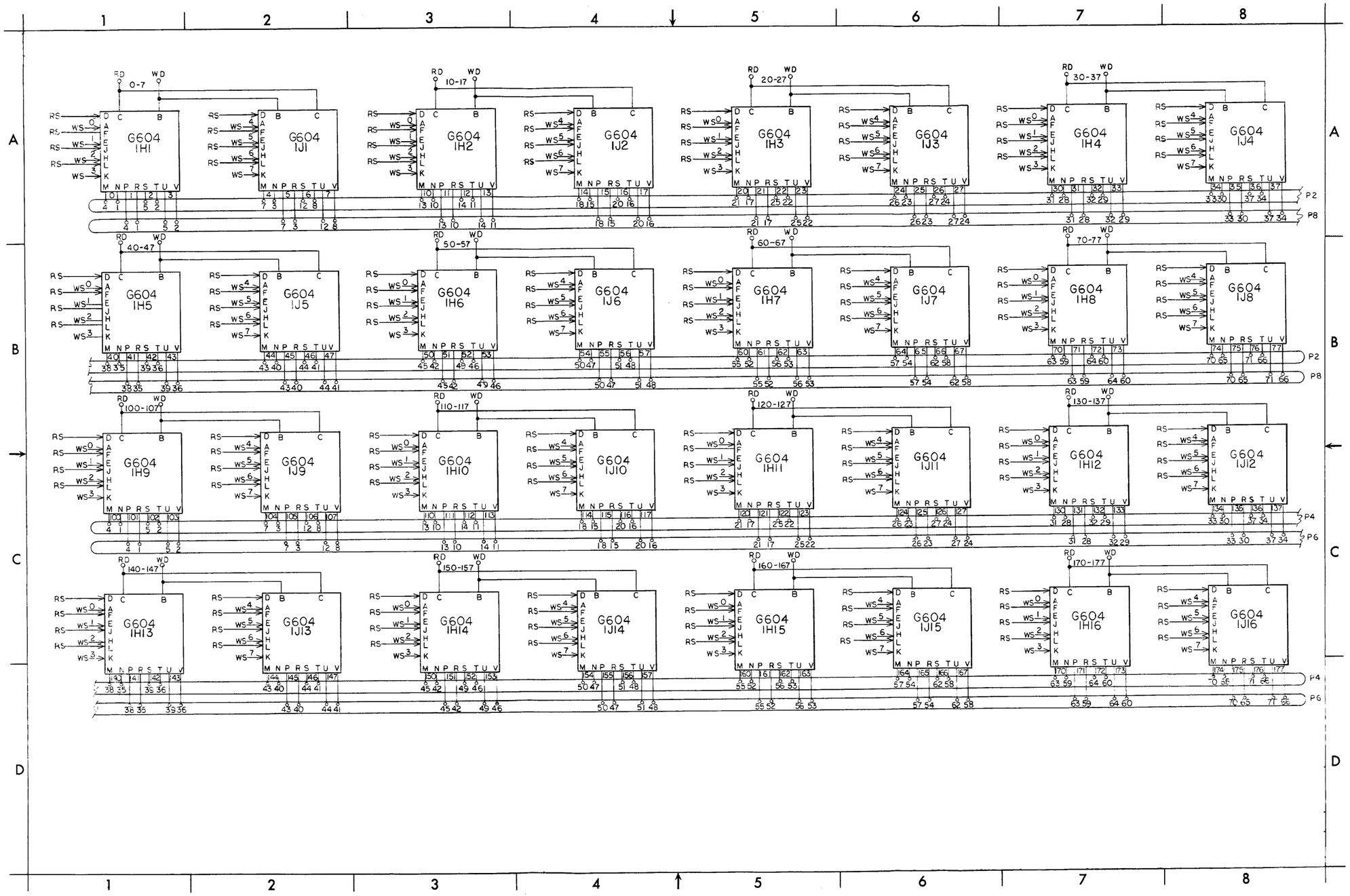
WD-D-164-0-IRP Inhibit Resistor Panel
164 Memory. Rev. A



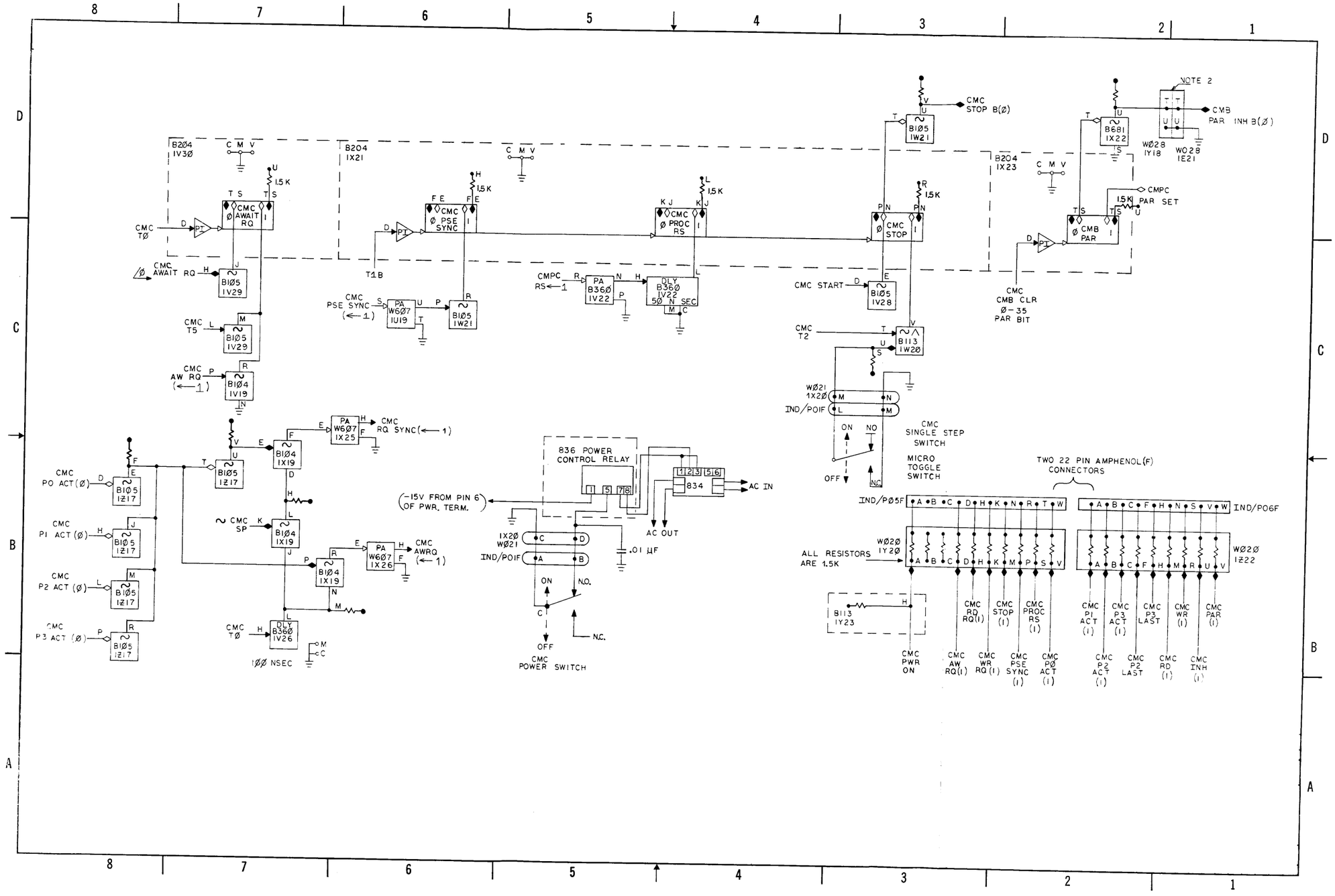
BS-D-164-0-DMSY Diode Matrix
Y-Selection



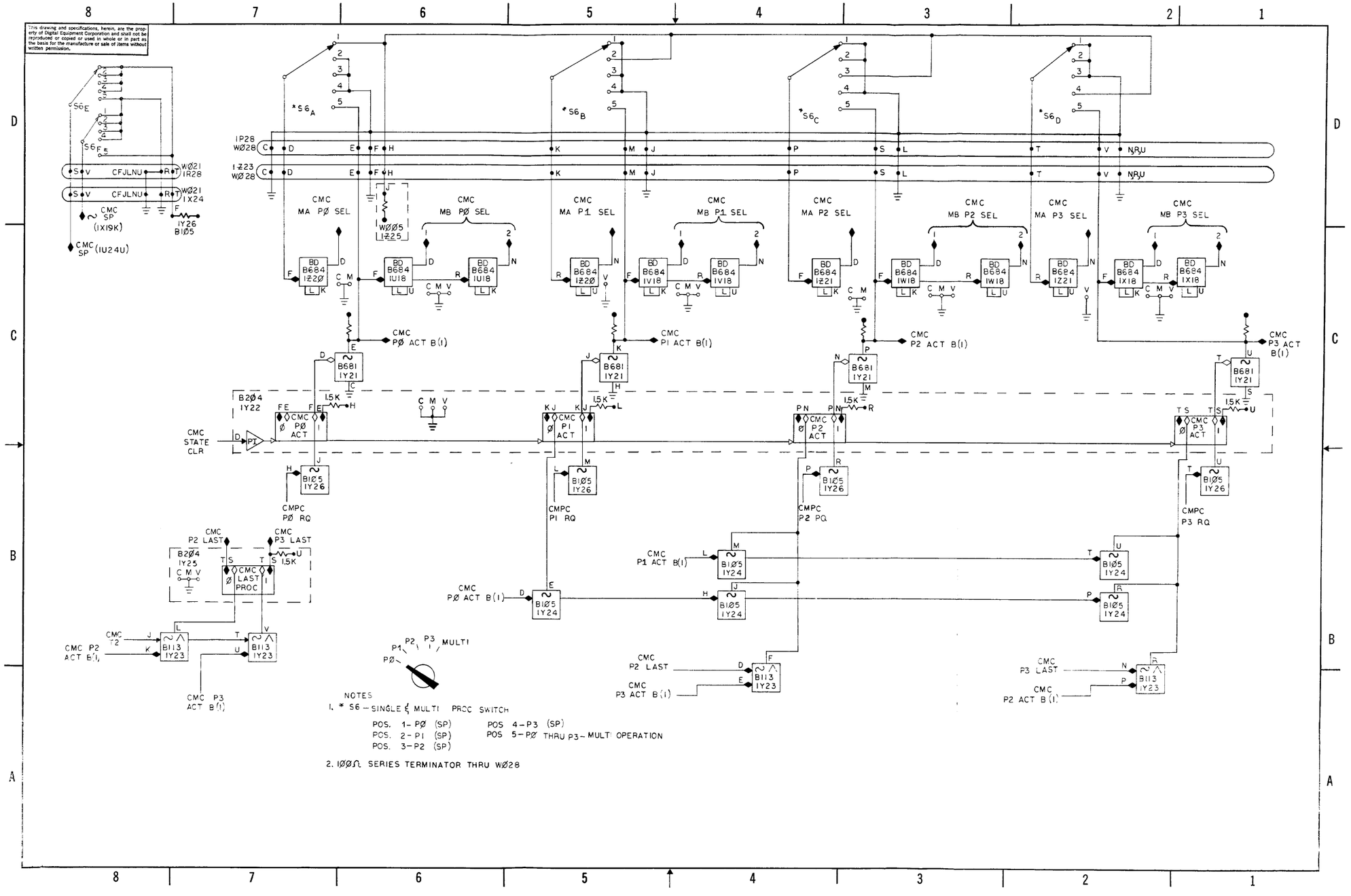
BS-D-164-0-CMY Core Memory Y-Selection
Bits 0-35 and Parity Bit. Rev. A



BS-D-164-0-DMSX Diode Matrix
X-Selection



BS-D-164-0-CMC2 Memory Control (Part 1). Rev. B

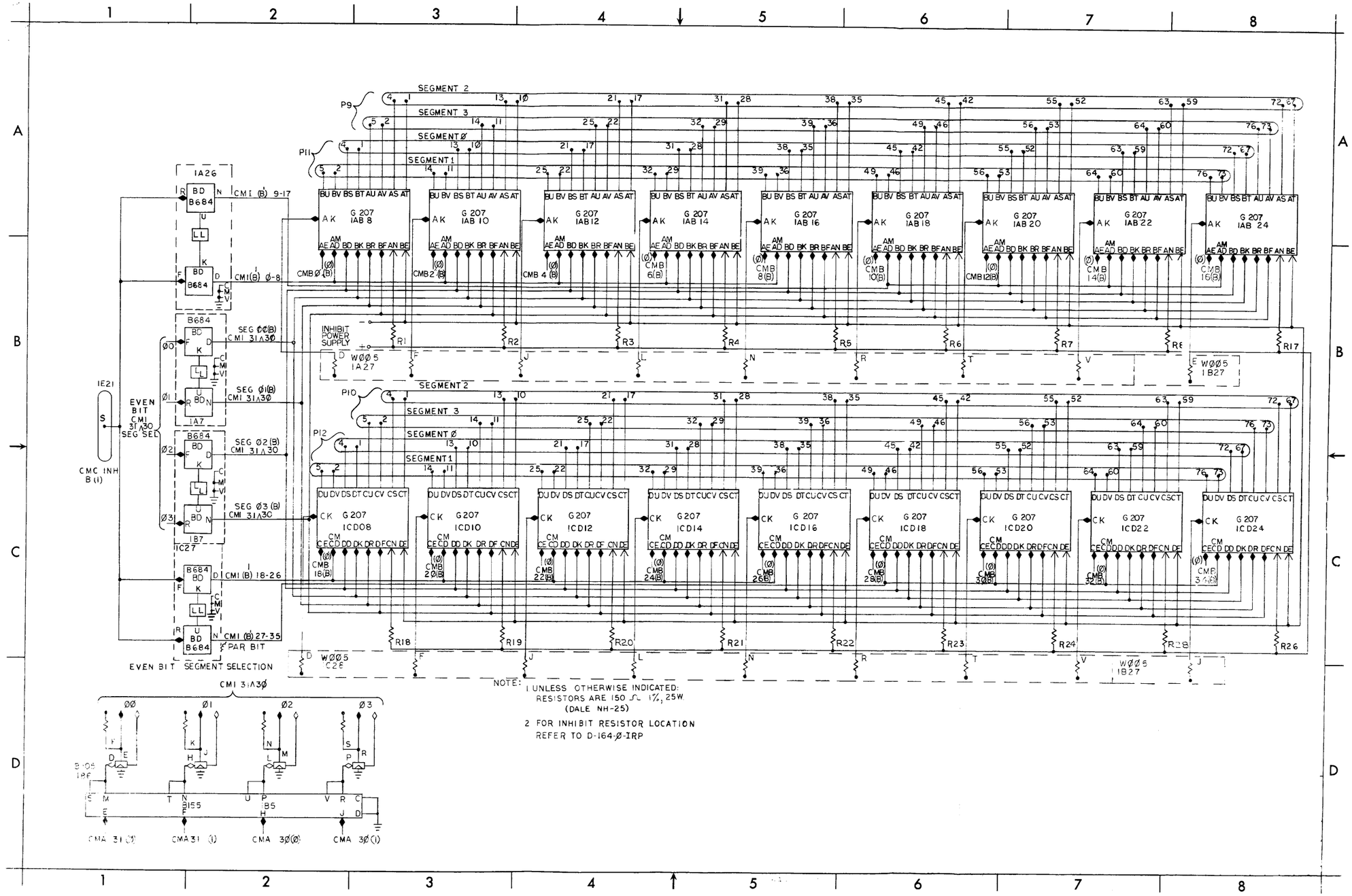


NOTES

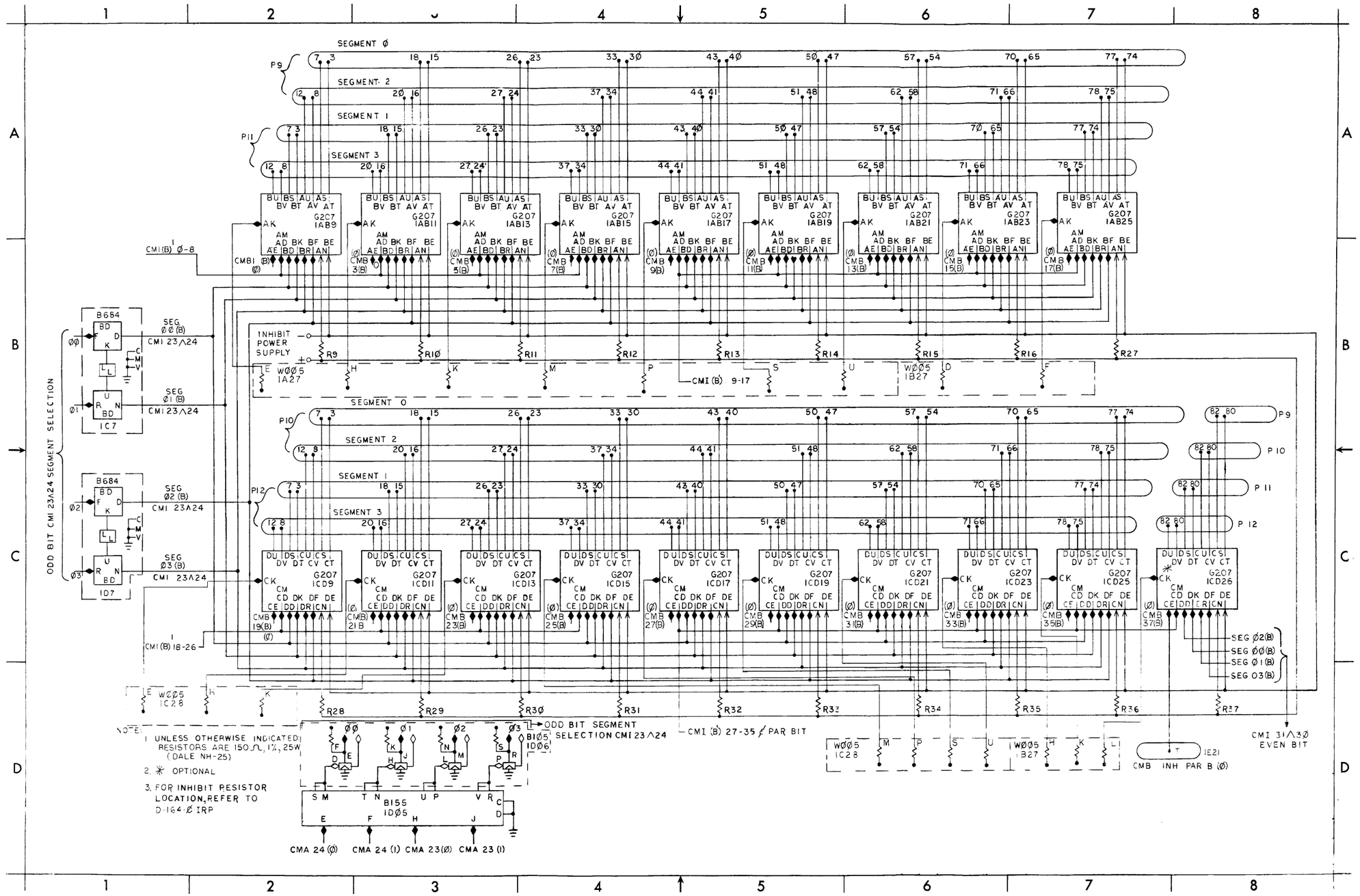
1. * S6 – SINGLE & MULTI PROC SWITCH

POS. 1 – PØ (SP)
POS. 2 – P1 (SP)
POS. 3 – P2 (SP)
POS 4 – P3 (SP)
POS 5 – PØ THRU P3 – MULTI OPERATION

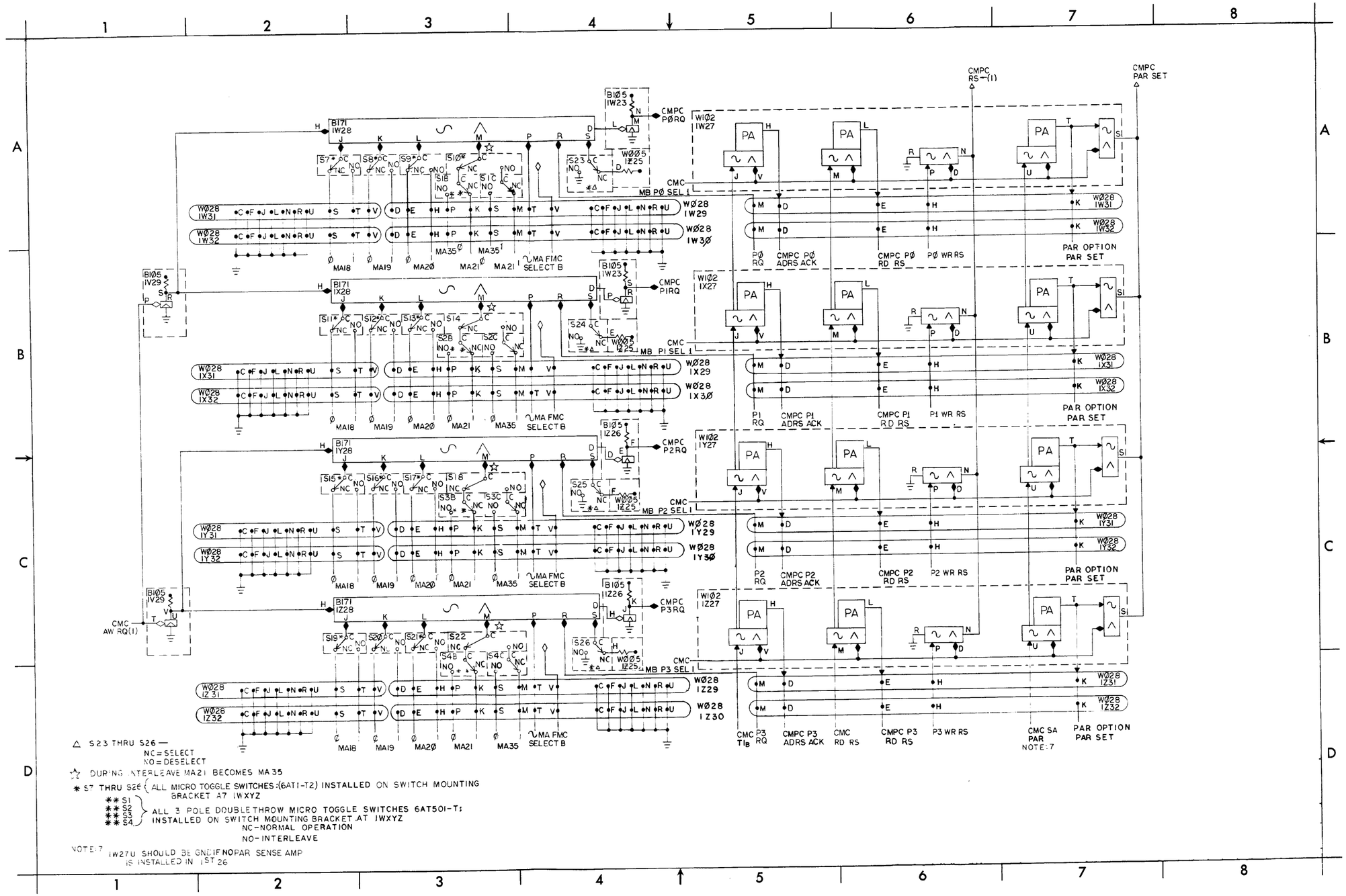
2. 1ØØΩ SERIES TERMINATOR THRU WØ28

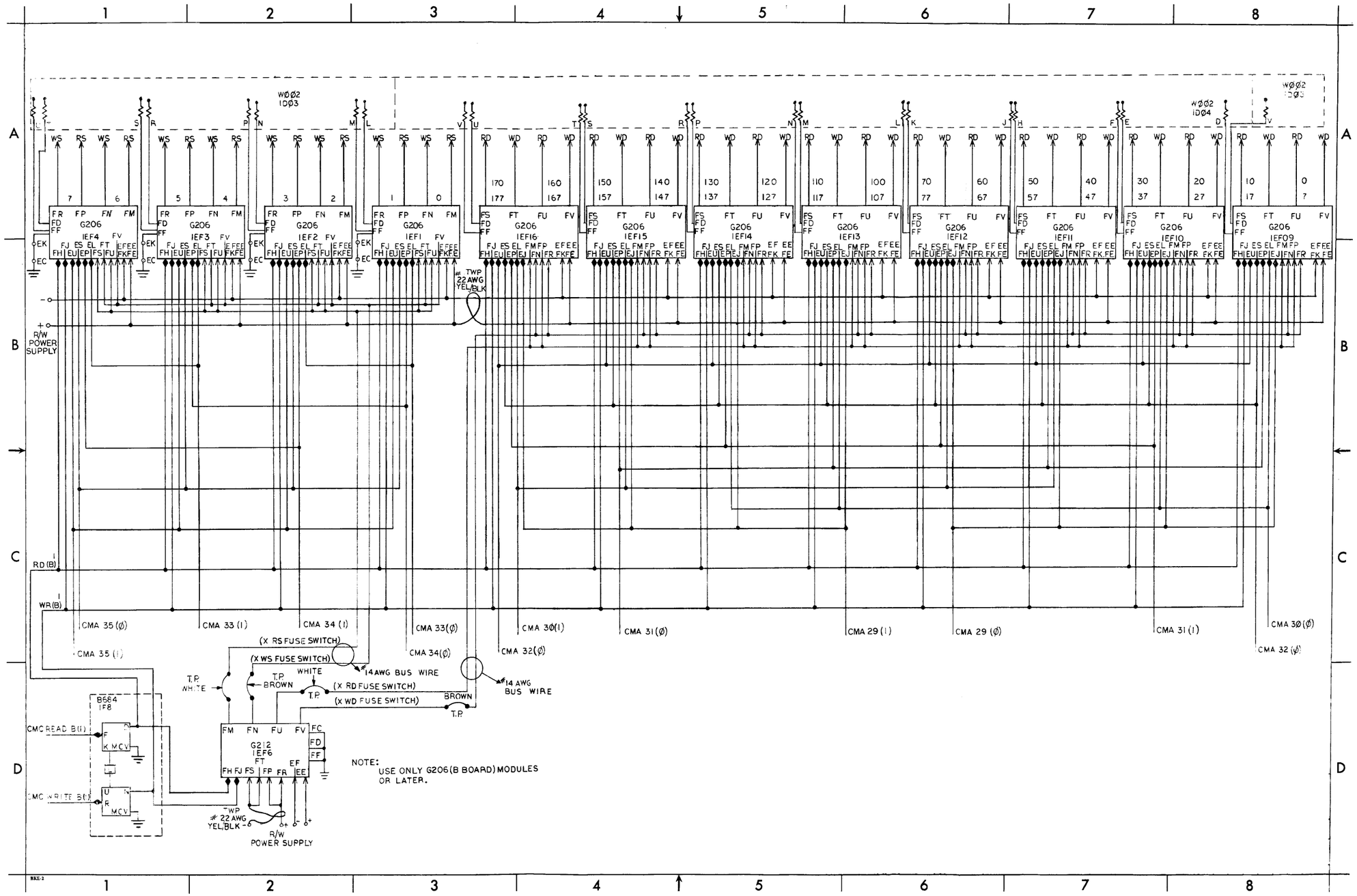


BS-D-164-0-CMI-1 CMI Inhibit Even Bits
Rev. A

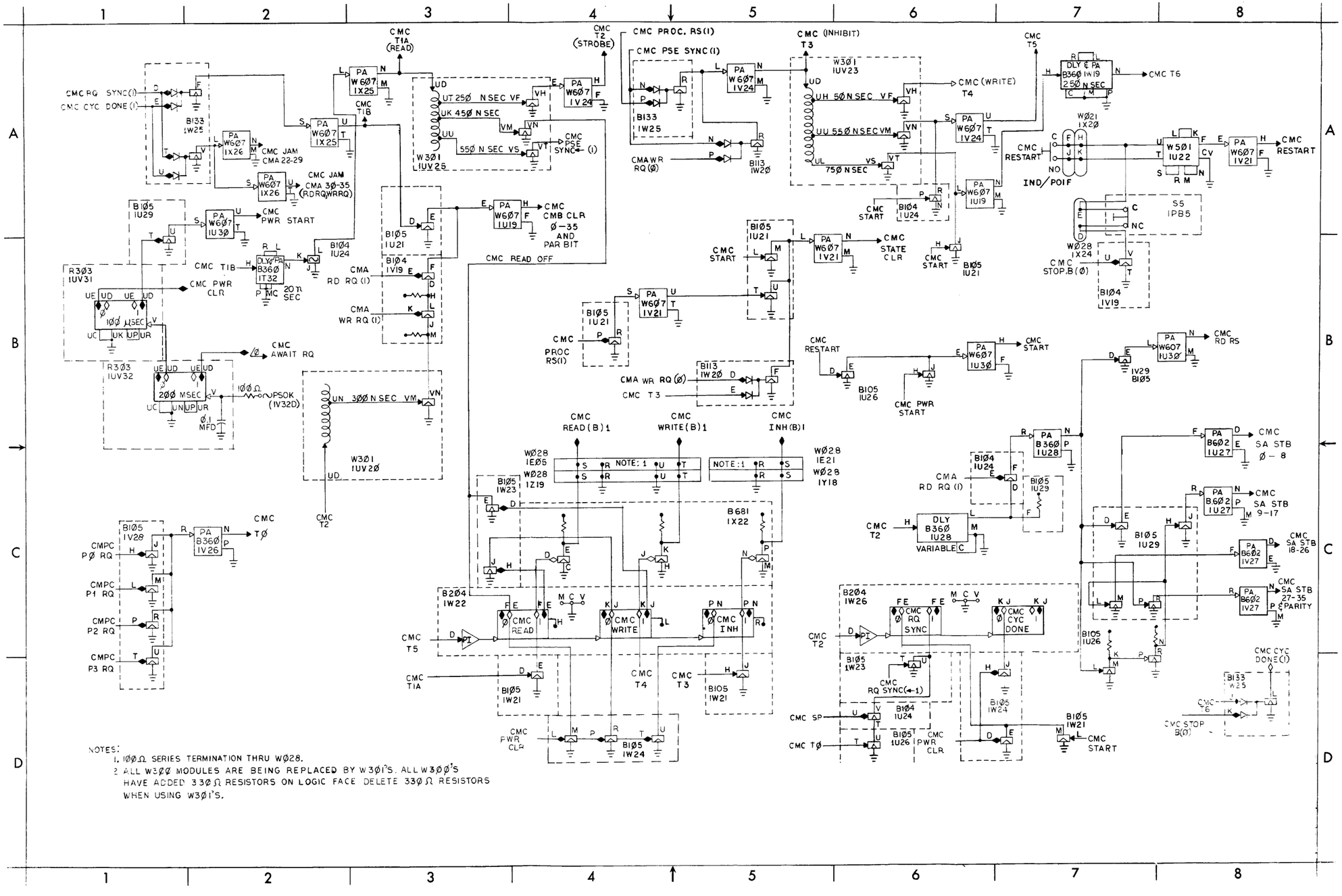


BS-D-164-0-CMI-2 CMI Inhibit Odd Bits and Parity Bits

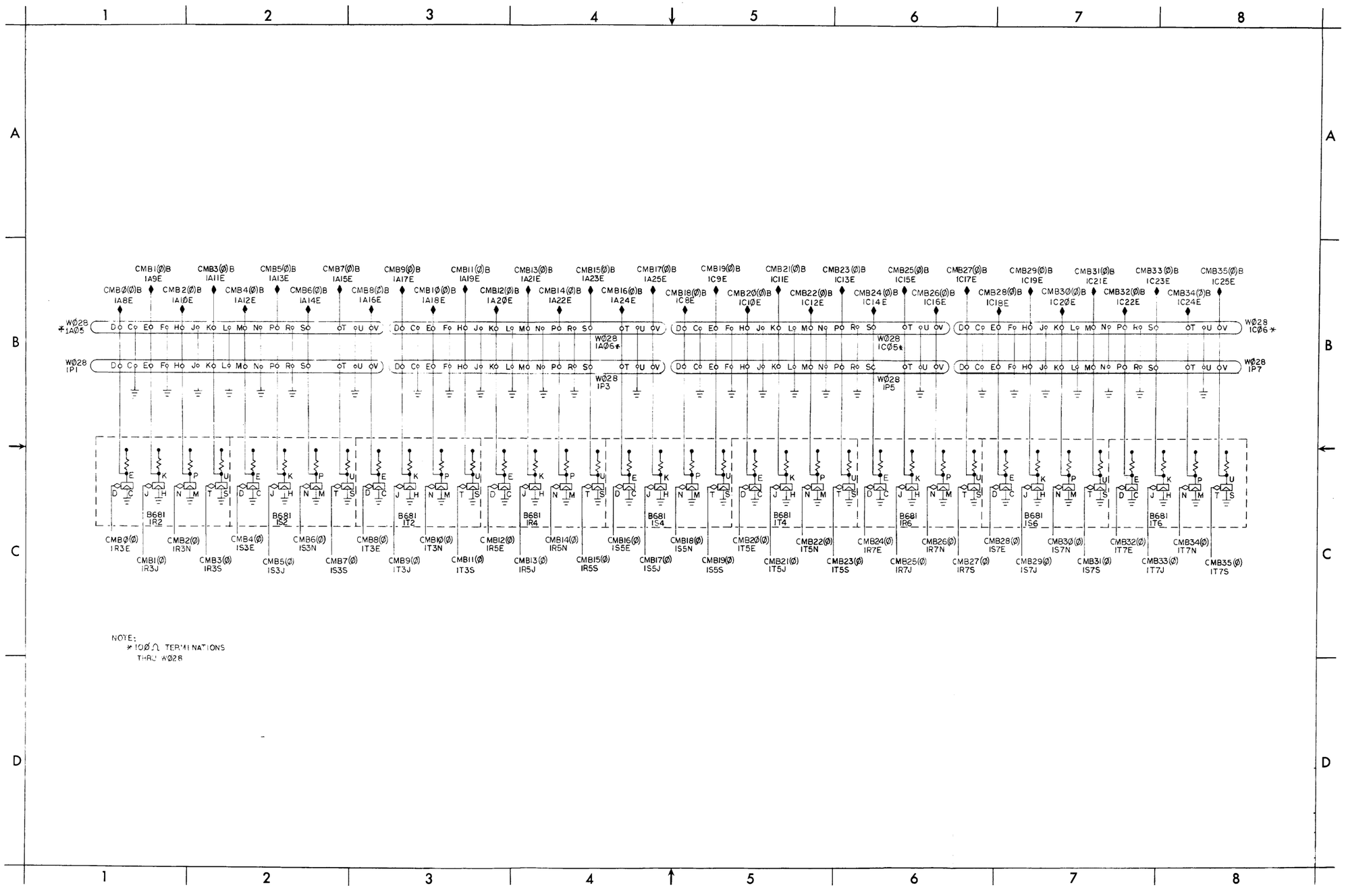

CMPC PØ RQ
CMPC PI RQ
CMPC P2 RQ
CMPC P3 RQ
CMC AW RQ(1)
MA FMC SELECT B
MA18
MA19
MA20
MA21
MA35
CMPC RS-(1)
CMPC PAR SET
CMC MB PØ SEL
CMC MB PI SEL
CMC MB P2 SEL
CMC MB P3 SEL
PØ RQ
CMPC PØ ADRS ACK
CMPC PØ RD RS
PØ WR RS
PI RQ
CMPC PI ADRS ACK
CMPC PI RD RS
PI WR RS
P2 RQ
CMPC P2 ADRS ACK
CMPC P2 RD RS
P2 WR RS
CMC P3 TIB RQ
CMPC P3 ADRS ACK
CMC RD RS
CMPC P3 RD RS
P3 WR RS
CMC SA PAR NOTE:7
PAR OPTION PAR SET
△ S23 THRU S26 — NC=SELECT NO=DESELECT
☆ DURING INTERLEAVE MA21 BECOMES MA35
* S7 THRU S26 { ALL MICRO TOGGLE SWITCHES:(6ATI-T2) INSTALLED ON SWITCH MOUNTING BRACKET A7 IWXYZ
** S1, S2, S3, S4 } ALL 3 POLE DOUBLE THROW MICRO TOGGLE SWITCHES 6AT501-T; INSTALLED ON SWITCH MOUNTING BRACKET AT IWXYZ
NC-NORMAL OPERATION
NO-INTERLEAVE
NOTE:7 IW27U SHOULD BE GND IF NOPAR SENSE AMP IS INSTALLED IN IST 26



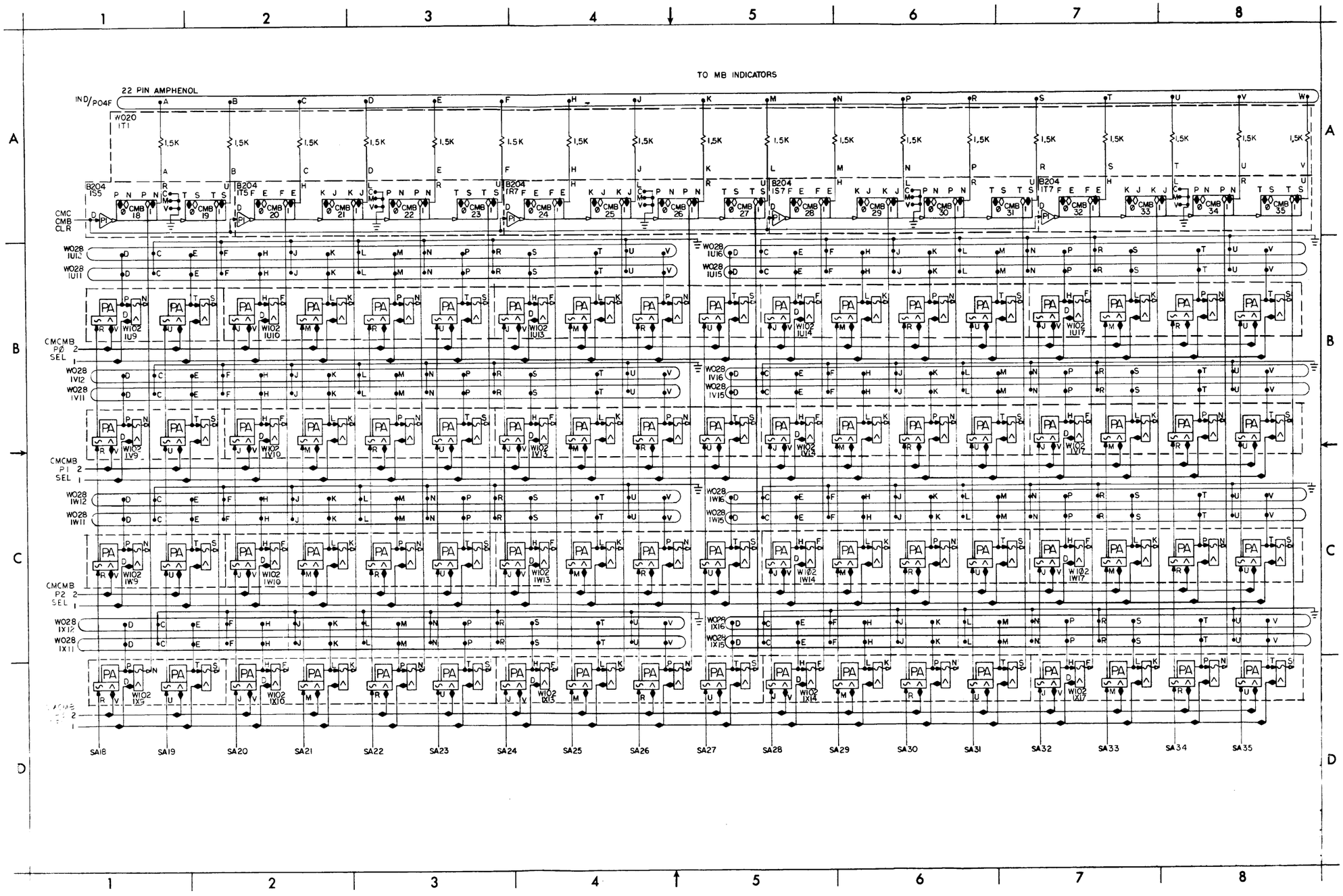
BS-D-164-0-CMX Core Memory X-Selection
0-35 and Parity Bit. Rev. A



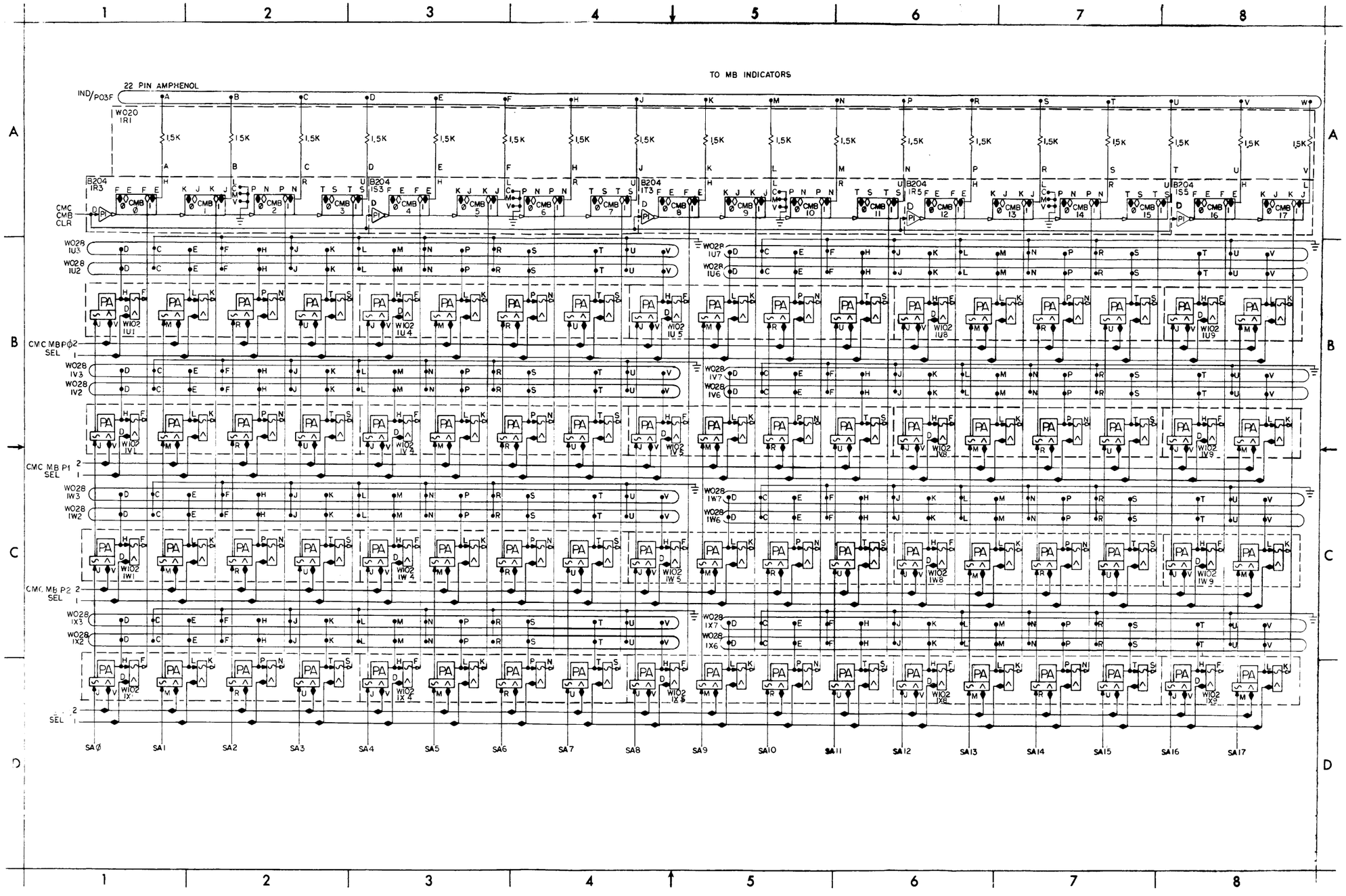
NOTES:
1. 100Ω SERIES TERMINATION THRU W028.
2. ALL W3ØØ MODULES ARE BEING REPLACED BY W3Ø1'S. ALL W3ØØ'S HAVE ADDED 330Ω RESISTORS ON LOGIC FACE DELETE 330Ω RESISTORS WHEN USING W3Ø1'S.



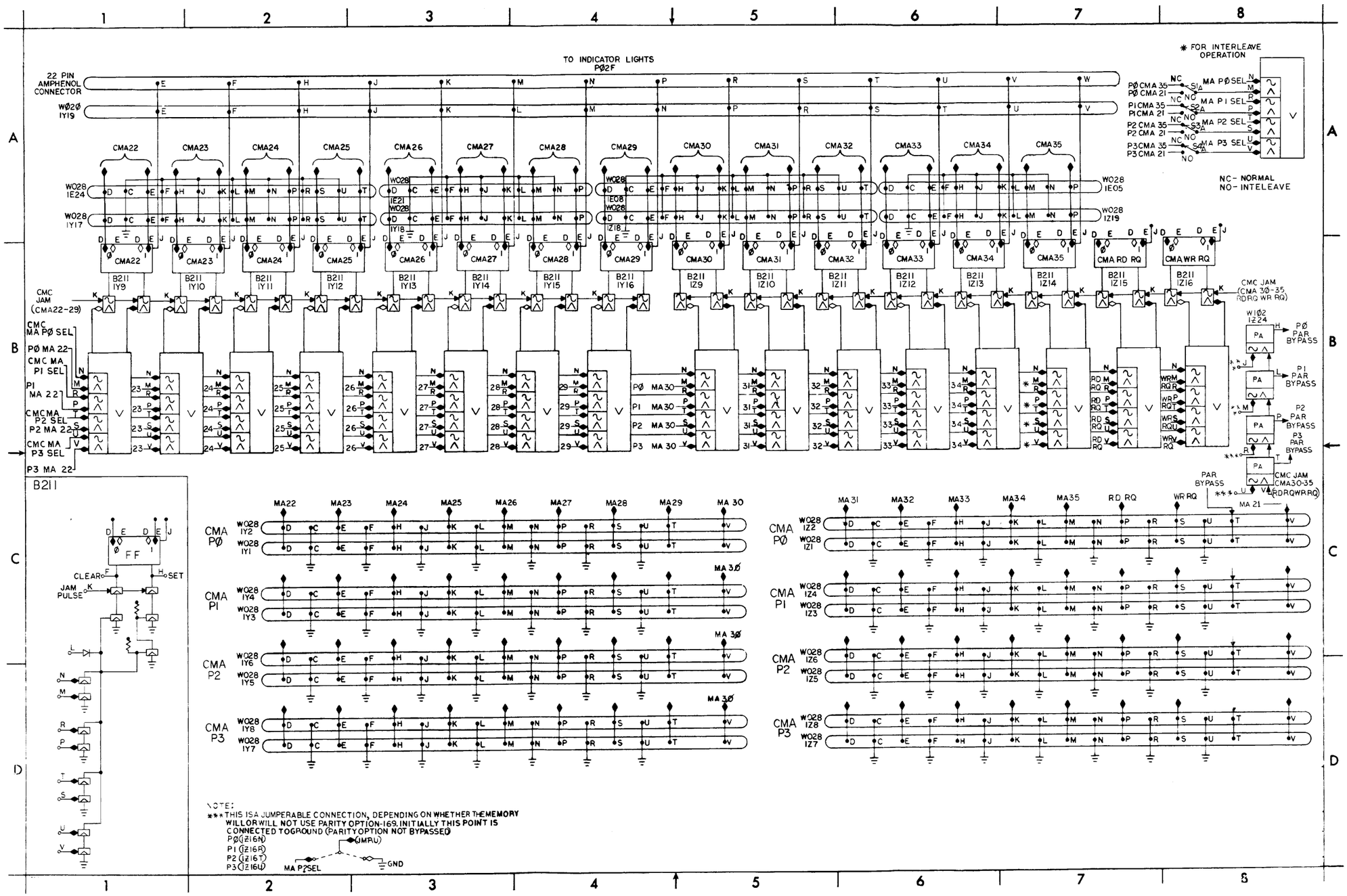
NOTE:
*IOØΩ TERMINATIONS THRU WØ28



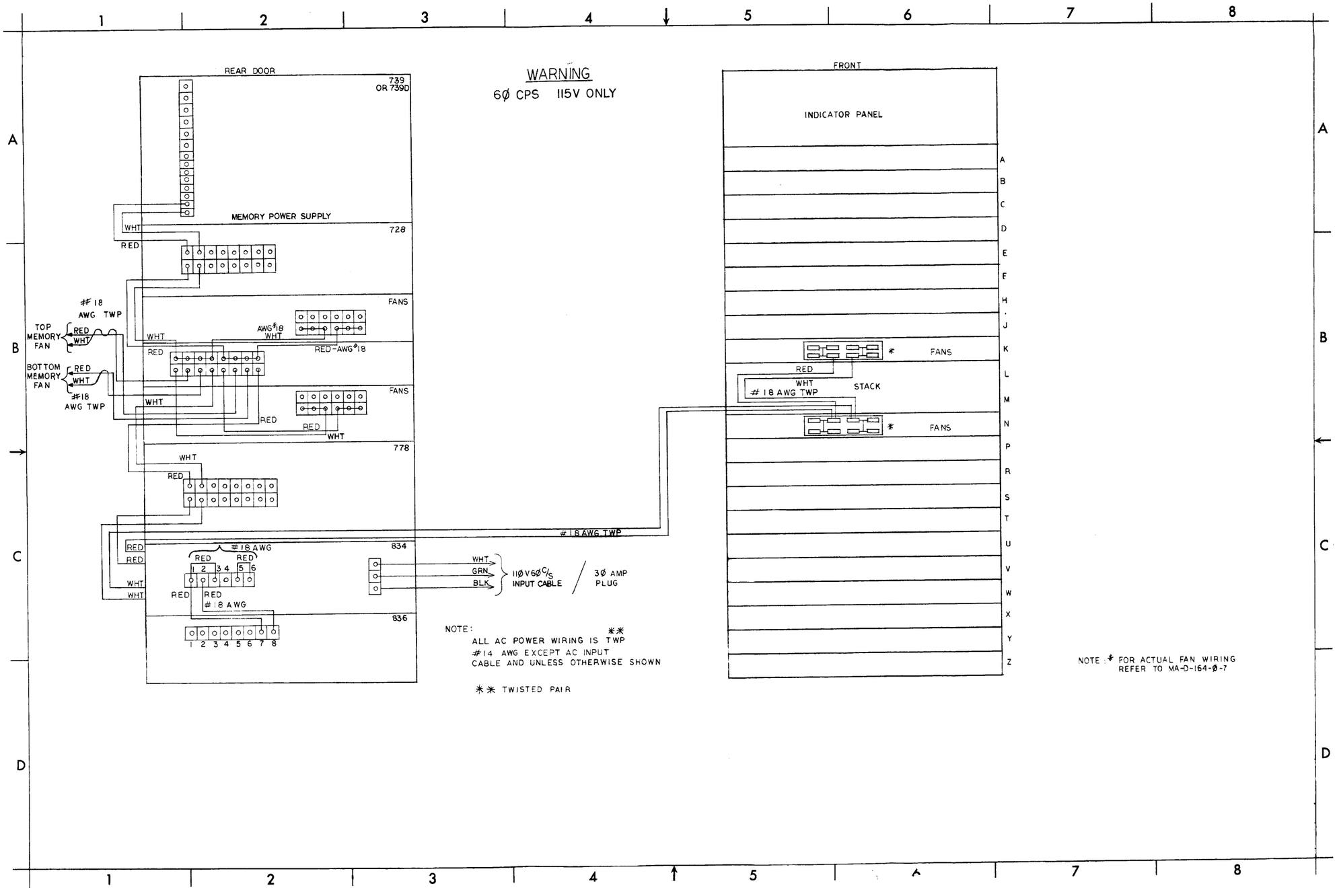
BS-D-164-0-CMBR Core Memory Buffer
18-35 Type 164



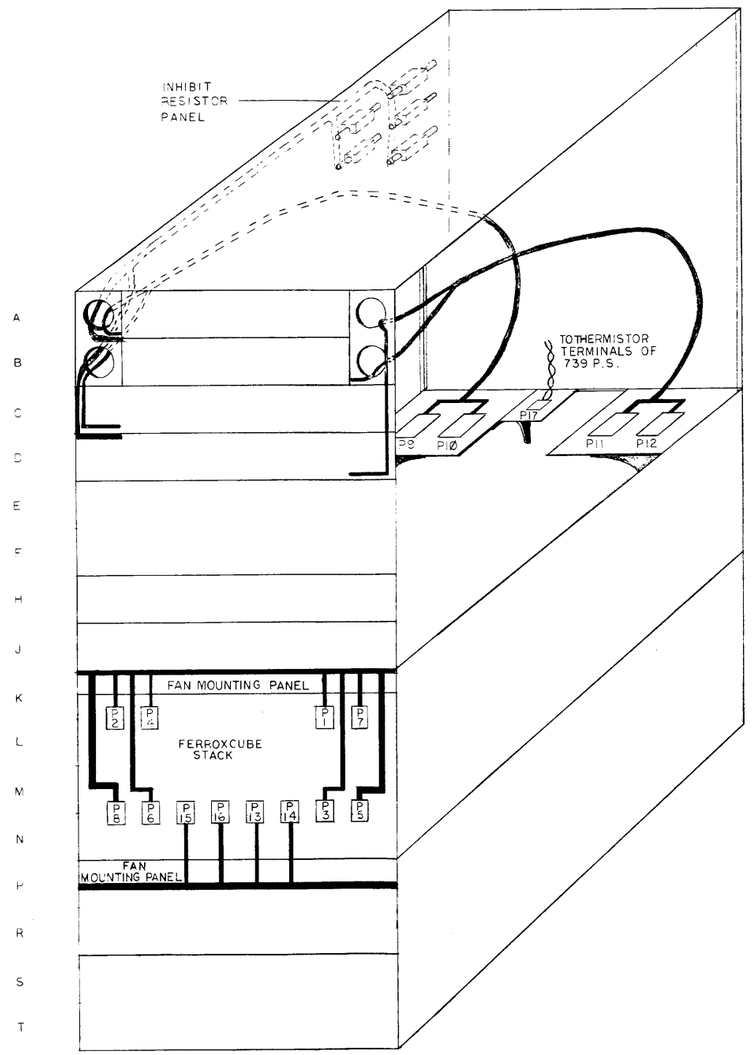
BS-D-164-0-CMBL Core Memory Buffer
0-17 Type 164



BS-D-164-0-CMA CMA. Rev. A



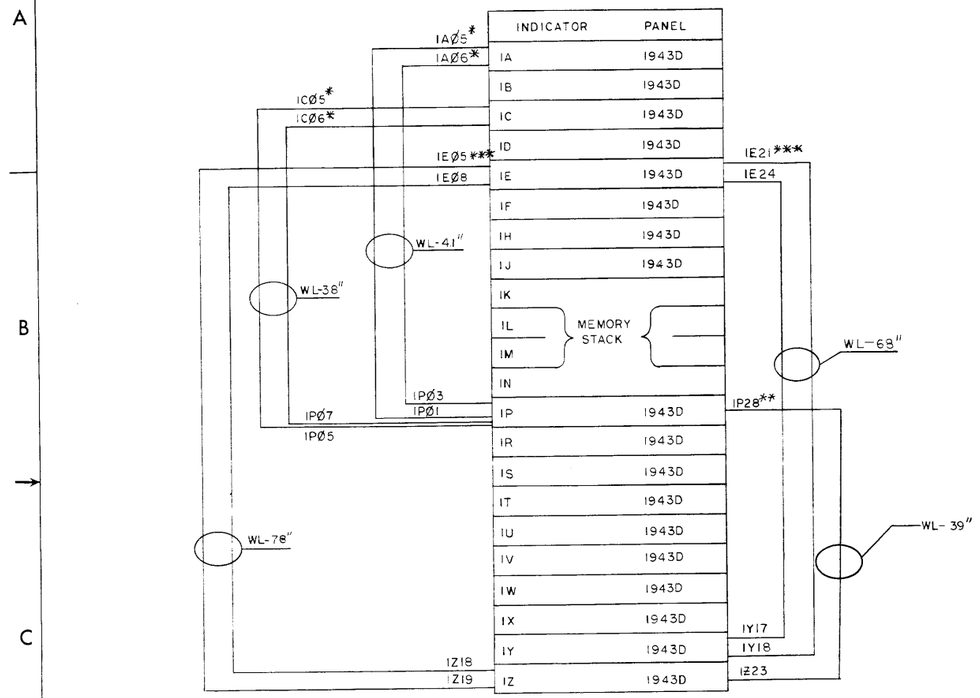
PW-D-164-0-ACPW AC Power Wiring. Rev. A



CABLE LENGTHS			CABLE LISTS	
FROM	TO	42 IN	DWG NO.	CODE
IHJ	P1		A-164-Ø-CBLS-9	CL
IHJ	P2		A-164-Ø-CBLS-10	CL
IHJ	P3		A-164-Ø-CBLS-11	CL
IHJ	P4		A-164-Ø-CBLS-12	CL
IHJ	P5		A-164-Ø-CBLS-13	CL
IHJ	P6		A-164-Ø-CBLS-14	CL
IHJ	P7		A-164-Ø-CBLS-15	CL
IHJ	P8	42 IN	A-164-Ø-CBLS-16	CL
IA	P9	72 IN	A-164-Ø-CBLS-6	CL
IB	P10		A-164-Ø-CBLS-5	CL
IC	P11		A-164-Ø-CBLS-4	CL
ID	P12	72 IN	A-164-Ø-CBLS-3	CL
IT	P13	48 IN	A-164-Ø-CBLS-17	CL
IT	P14		A-164-Ø-CBLS-18	CL
IR	P15		A-164-Ø-CBLS-7	CL
IR	P16	48 IN	A-164-Ø-CBLS-8	CL
IA	RES	66 IN	A-164-Ø-12	CL
IC	RES	66 IN	A-164-Ø-13	CL
739 PS.	P17	36 IN	A-164-Ø-21	CL

NOTES
1. P1 THRU P16 ARE 75 PIN BURNDY CONNECTORS # MS75R-124
2. P17 IS A 14 PIN BURNDY CONNECTOR # MS14R-1

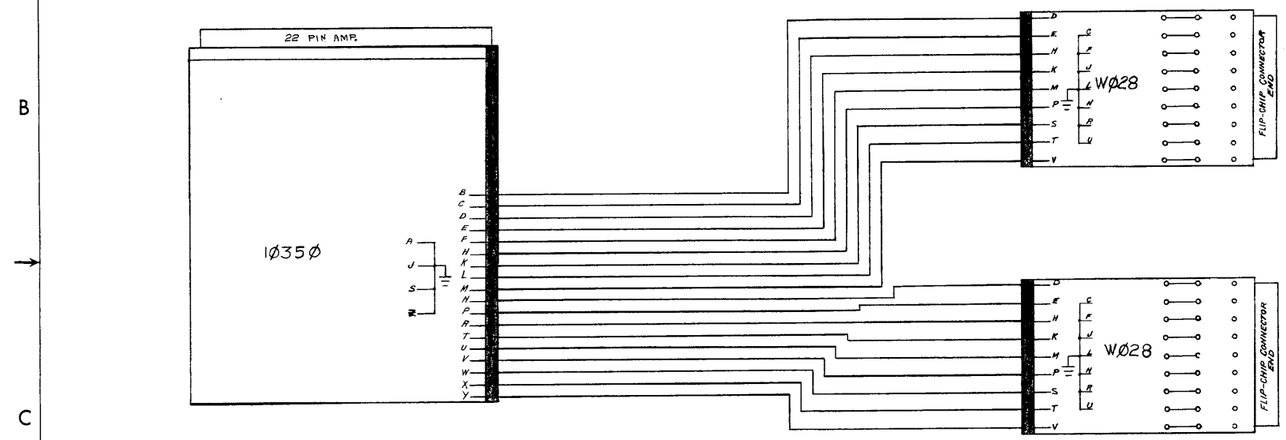
CD-D-164-0-CD Cable Diagram Core Memory
164 (Part 1). Rev. A



NOTE:

1. WL-WIRE LENGTH
2. * — DESIGNATES END OF CABLE WHICH HAS SERIES TERMINATION OF ØØΩ, 1/4W 10% RESISTORS
3. ** — SAME AS NOTE 2 EXCEPT PIN E, M, S, V ONLY WILL HAVE SERIES TERMINATION OF 100Ω $\frac{1}{4}$W RESISTORS & THE OTHER PINS WILL BE JUMPERS.
4. *** — SAME AS NOTE 2 EXCEPT PIN S, T ONLY WILL HAVE SERIES TERMINATIONS OF 100Ω, 1/4W RESISTORS & THE OTHER PINS WILL BE JUMPERS.

CD-D-164-0-CD Cable Diagram Core Memory
164 (Part 2). Rev. A

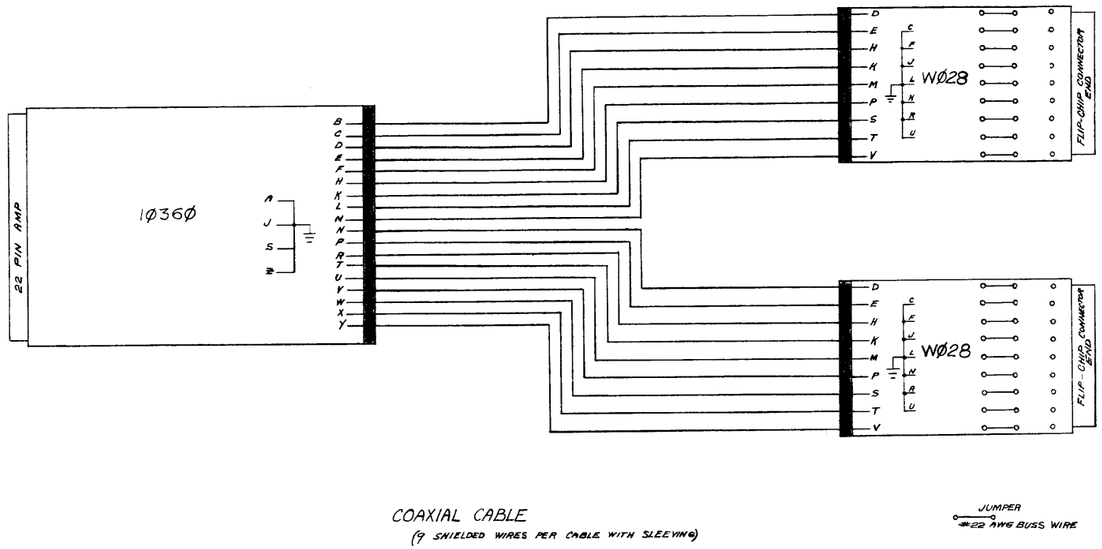


COAXIAL CABLE
(9 SHIELDED WIRES PER CABLE WITH SLEEVING)

*FOR USE BETWEEN:
TYPE 164 AND C.P.
TYPE 164 TO TYPE 163C
TYPE 164 AND MEMORY EXERCISER

CABLE LENGTH WILL BE SPECIFIED WHEN ORDERED

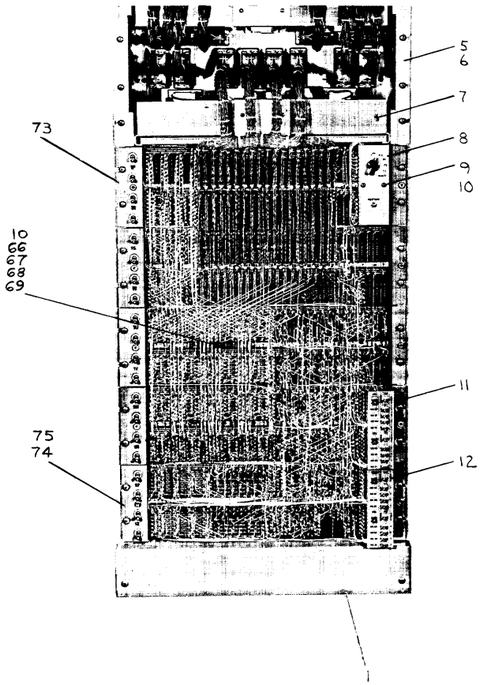
CD-D-164-0-CCD Coaxial Cable
Diagram (Part 1)

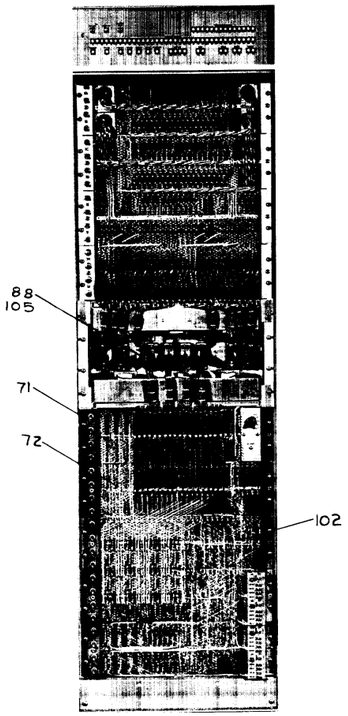


* FOR USE BETWEEN:
TYPE 164 AND C.P.
TYPE 164 TO TYPE 163C
TYPE 164 AND MEMORY EXERCISER

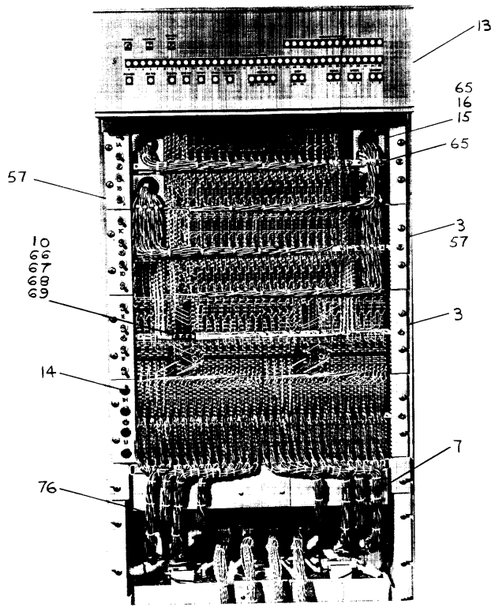
CABLE LENGTH WILL BE SPECIFIED WHEN ORDERED

CD-D-164-0-CCD Coaxial Cable Diagram (Part 2)



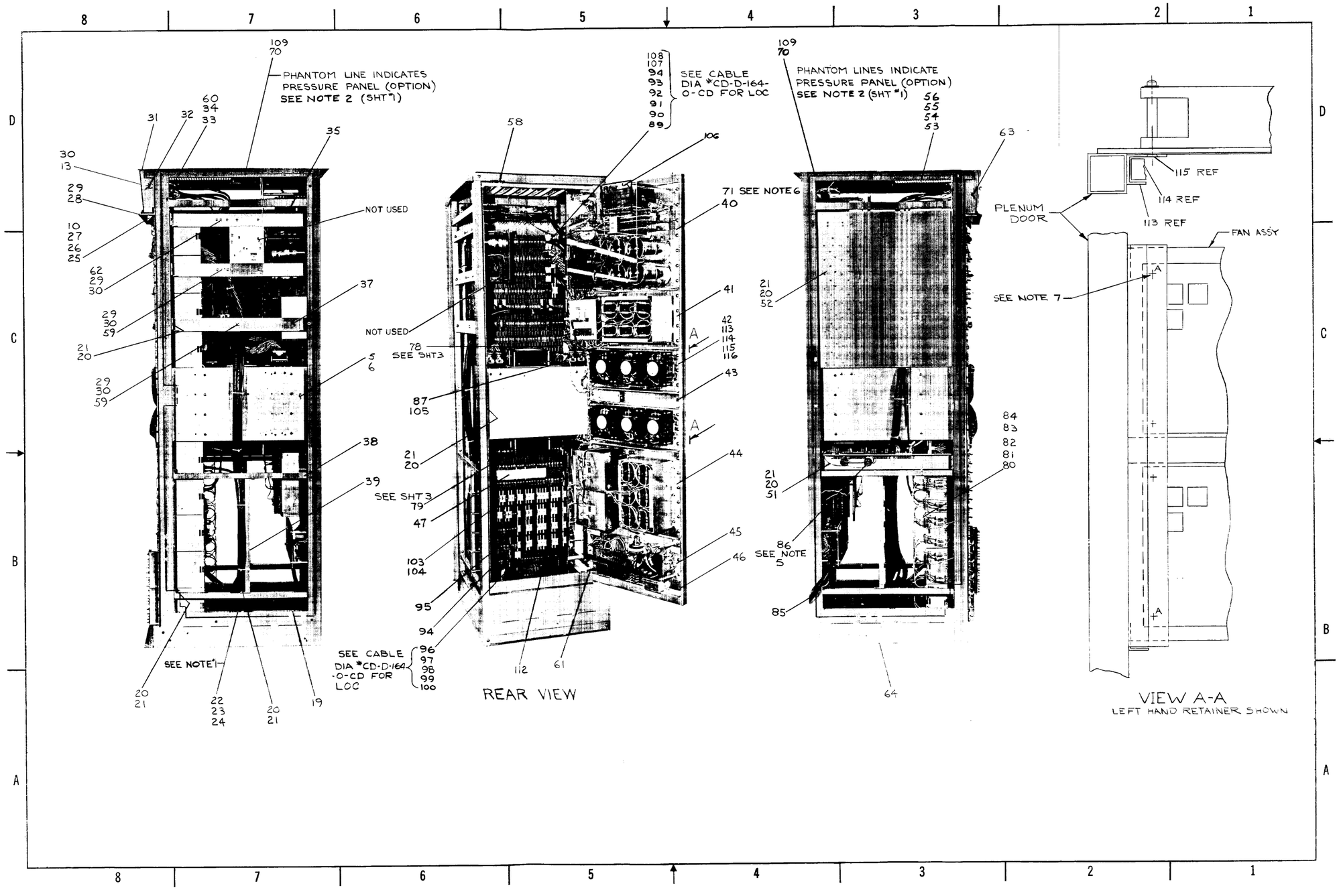


FRONT VIEW WITH DOORS
AND END PANELS REMOVED

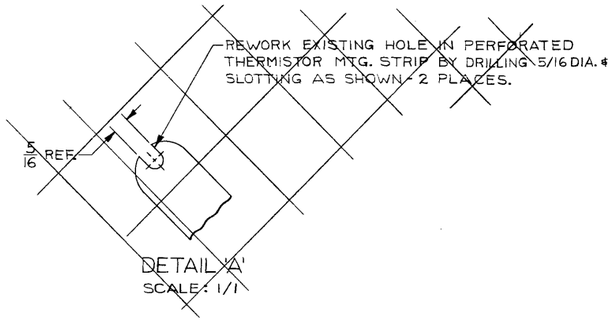


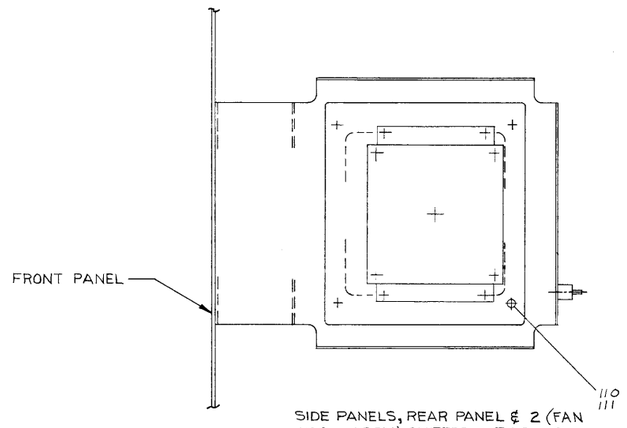
NOTES:

1. DRILL THRU .332 DIA HOLES IN CABINET FRAME, THRU SKID DWG NO. MD-D-0142, & INSTALL PART NO. 22, 23 & 24
2. IF #70 (PRESSURE PANEL) IS USED, YOU MAY BY USING 2 HOLES AT TOP OF CAB. FOR RIVET (109) IN PLACE. DRILL REMAINING HOLES #20 (161) DRILL USING PANEL AS TEMPLATE & POP RIVET (109), IN PLACE.
3. ~~IF #70 PRESSURE PANEL IS USED PART TO HAVE 5/32 HOLES CSK .82" TO .86 DIA FOR #6-32 X 1/4 LG. FLAT HEAD SCREWS (MAKE SURE HOLES ARE CSK ON CORRECT SIDE) WHICH DEPENDS ON WHETHER LEFT OR RIGHT SIDE MTG IS REQD.~~
4. #101 (164 BUS TERMINATOR, DWG NO. B-IA-5403930) NOT SHOWN ON THIS ASSEMBLY. LOC TO BE SPECIFIED BY PROJ ENG.
5. LENGTH OF CABLE TO BE SPEC BY PROJ ENG.
6. LABEL TO BE PLACED IN THIS LOCATION WHICH READS "THIS UNIT REQ A G800D BOARD."
7. REMOVE 4 "A" SCREWS, 2 LEFT SIDE, 2 RIGHT SIDE, & ASSEMBLE ITEMS #113 & 116 USING FLT H'D SCREWS ITEM #115 TO REPLACE "A" SCREWS.

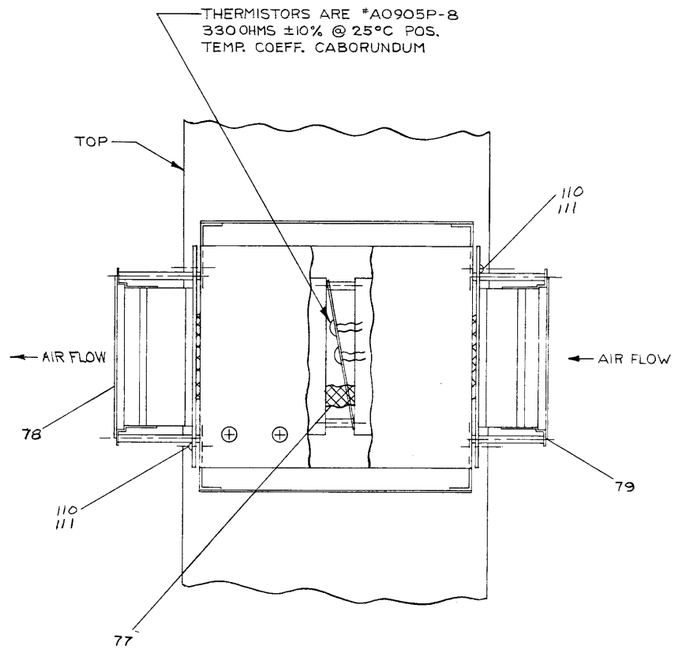


D-UA-164-0-1 Core Memory Type 164 (Part 2). Rev. J





SIDE PANELS, REAR PANEL & 2 (FAN HSG. ASSY.) OMITTED IN THIS VIEW.



NOTES:

1. THIS DWG WAS FORMERLY CALLED 164 MEMORY REWORK. DWG # D-AD-164-0-15, BUT HAS BEEN MADE SHT 3 OF 164 ASSY.

* 739A POWER SUPPLY MODIFICATIONS FOR TYPE 164 MEMORY

REFER TO MA-D-739-0-1

WIRE CHANGES

CHANGE	LOCATION	COLOR & SIZE	LOCATION
DELETE	D1 & D4 CATHODE	RED AWG 14	C1 (+)
DELETE	D1 & D4 CATHODE	RED AWG 18	PIN AD OF R/W G800
ADD	PIN AD OF R/W G800	RED AWG 18	C4 (+)
ADD	D1 & D4 CATHODE	BLUE AWG 14	TERM. # TO JONES STRIP)
ADD	C1 (+)	YELLOW AWG 14	TERM. # 4 JONES STRIP)
ADD	PIN AS OF R/W G800	WHT AWG 22	PIN BK OF R/W G800
ADD	PIN AS OF INH G800	WHT AWG 22	PIN BK OF INH G800

TRANS. TAP CHANGES (T1 57144 TRANS. ONLY) **	
FROM TAP	TO TAP
15	20
11	25

NOTE: INSTALL G800-D BOARDS IF PRIOR BOARDS ARE PREVIOUSLY IN

COMPONENT CHANGES ON FLIP CHIP MOUNTING BLOCK

CHANGE	LOCATION	COMPONENT	LOCATION
DELETE	PIN BM OF R/W G800	R9-1,62K, $\frac{1}{8}$W, 1%, MF	PIN BN OF R/W G800
ADD	PIN BM OF R/W G800	R9-2K, $\frac{1}{8}$W, 1%, MF	PIN BN OF R/W G800
DELETE	PIN BM OF INH G800	R10-1,62K, $\frac{1}{8}$W, 1% MF	PIN BN OF INH G800
ADD.	PIN BM OF INH G800	R10-2K, $\frac{1}{8}$W, 1% MF	PIN BN OF INH G800
DELETE	PIN AE OF R/W G800	R3-909Ω, $\frac{1}{8}$W, 1% MF	PIN AC OF R/W G800
ADD	PIN AE OF R/W G800	R3-3,3K, $\frac{1}{4}$W, 5%	PIN AC OF R/W G800

* NOTE: THESE CHANGES APPLY ONLY TO 739A POWER SUPPLIES AND NO CHANGES ARE NECESSARY ON 739E'S.

** THIS CHANGE ALSO APPLIES TO 739E POWER SUPPLIES ALREADY USED IN THE FIELD

✳ 739 POWER SUPPLY MODIFICATIONS FOR TYPE 164 MEMORY

REFER TO MA-D-739-0-1

WIRE CHANGES

CHANGE	LOCATION	COLOR & SIZE	LOCATION
DELETE	D1 & D4 CATHODE	RED AWG 14	C1 (+)
DELETE	D1 & D4 CATHODE	RED AWG 18	PIN AD OF R/W G800
ADD	PIN AD OF R/W G800	RED AWG 18	C4 (+)
ADD	D1 & D4 CATHODE	BLUE AWG 14	TERM # 10 (JONES STRIP)
ADD	C1 (+)	YELLOW AWG 14	TERM # 4 (JONES STRIP)
ADD	PIN AS OF R/W G800	WHT AWG 22	PIN BK OF R/W G800
ADD	PIN AS OF INH G800	WHT AWG 22	PIN BK OF INH G800

TRANS FROM TAP	TAP CHANGES TO TAP
3	17
6	11

(T 157109 TRANS. ONLY) ✳✳

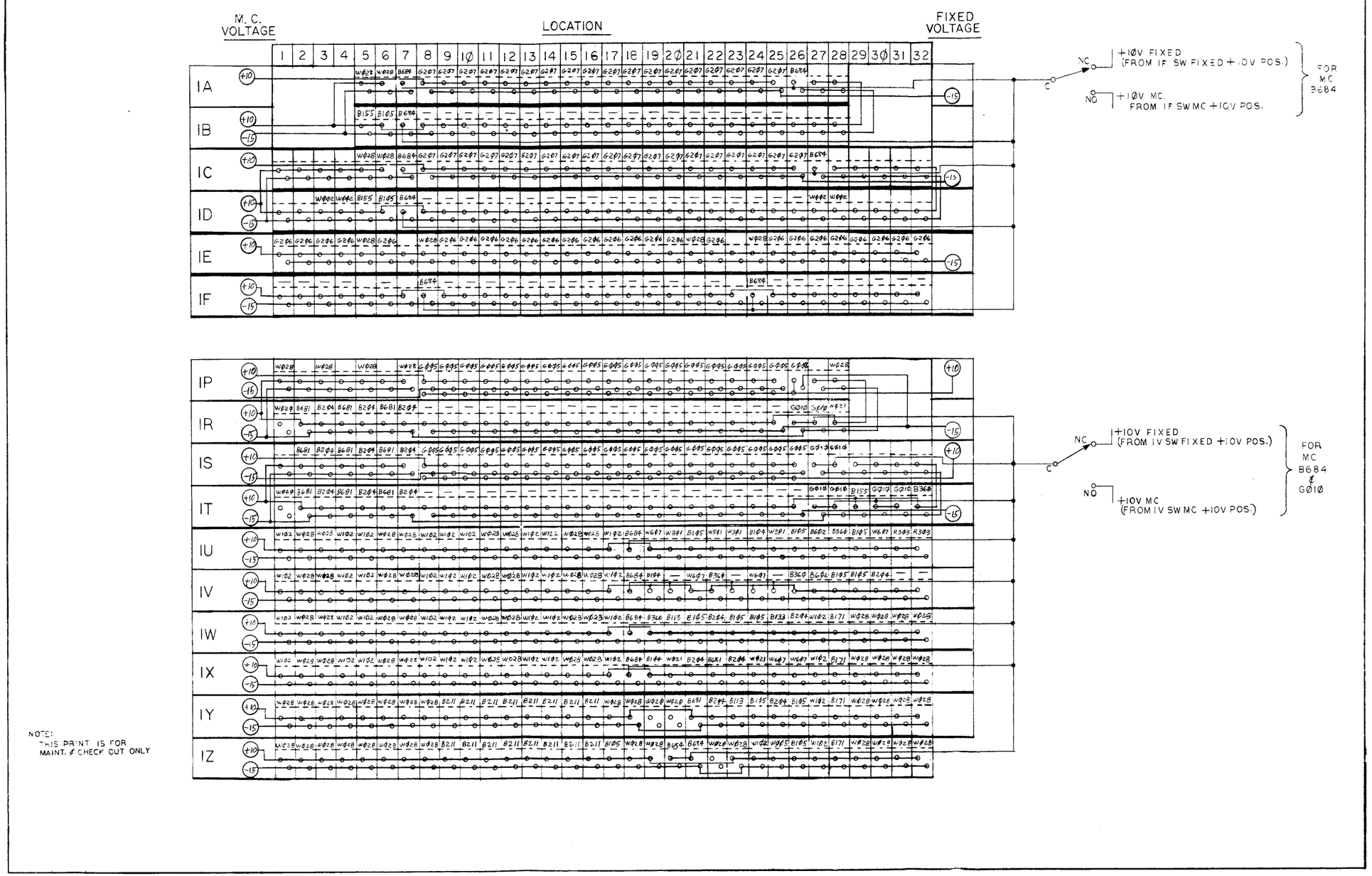
NOTE: INSTALL G800-D BOARDS IF PRIOR BOARDS ARE PREVIOUSLY IN

COMPONENT CHANGES ON FLIP CHIP MOUNTING BLOCK

CHANGE	LOCATION	COMPONENT	LOCATION
DELETE	PIN BM OF R/W G800	R9-1,62K, $\frac{1}{8}$W, 1% MF	PIN BN OF R/W G800
ADD	PIN BM OF R/W G800	R9— 2K, $\frac{1}{8}$W, 1% MF	PIN BN OF R/W G800
DELETE	PIN BM OF INH G800	R10-1,62K $\frac{1}{8}$W, 1% MF	PIN BN OF INH G800
ADD	PIN BM OF INH G800	R10— 2K, $\frac{1}{8}$W, 1% MF	PIN BN OF INH G800
DELETE	PIN AE OF R/W G800	R3-909Ω, $\frac{1}{8}$W, 1% MF	PIN AC OF R/W G800
ADD	PIN AE OF R/W G800	R3-3,3K, $\frac{1}{4}$W, 5%	PIN AC OF R/W G800

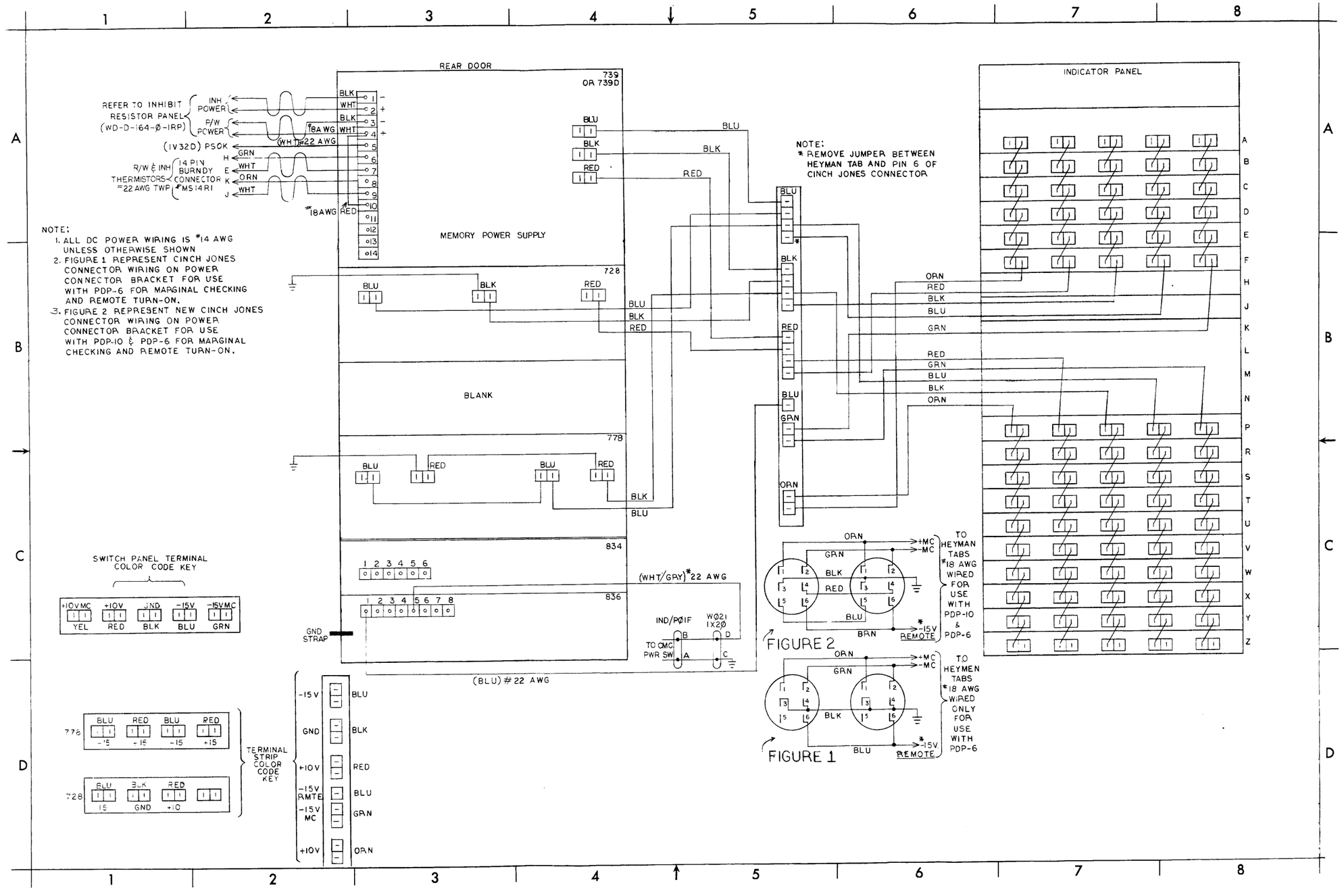
✳ NOTE: THESE CHANGES APPLY ONLY TO 739 POWER SUPPLIES AND NO CHANGES ARE NECESSARY ON 739D'S

✳✳ THIS CHANGE ALSO APPLIES TO 739D POWER SUPPLIES ALREADY USED IN THE FIELD

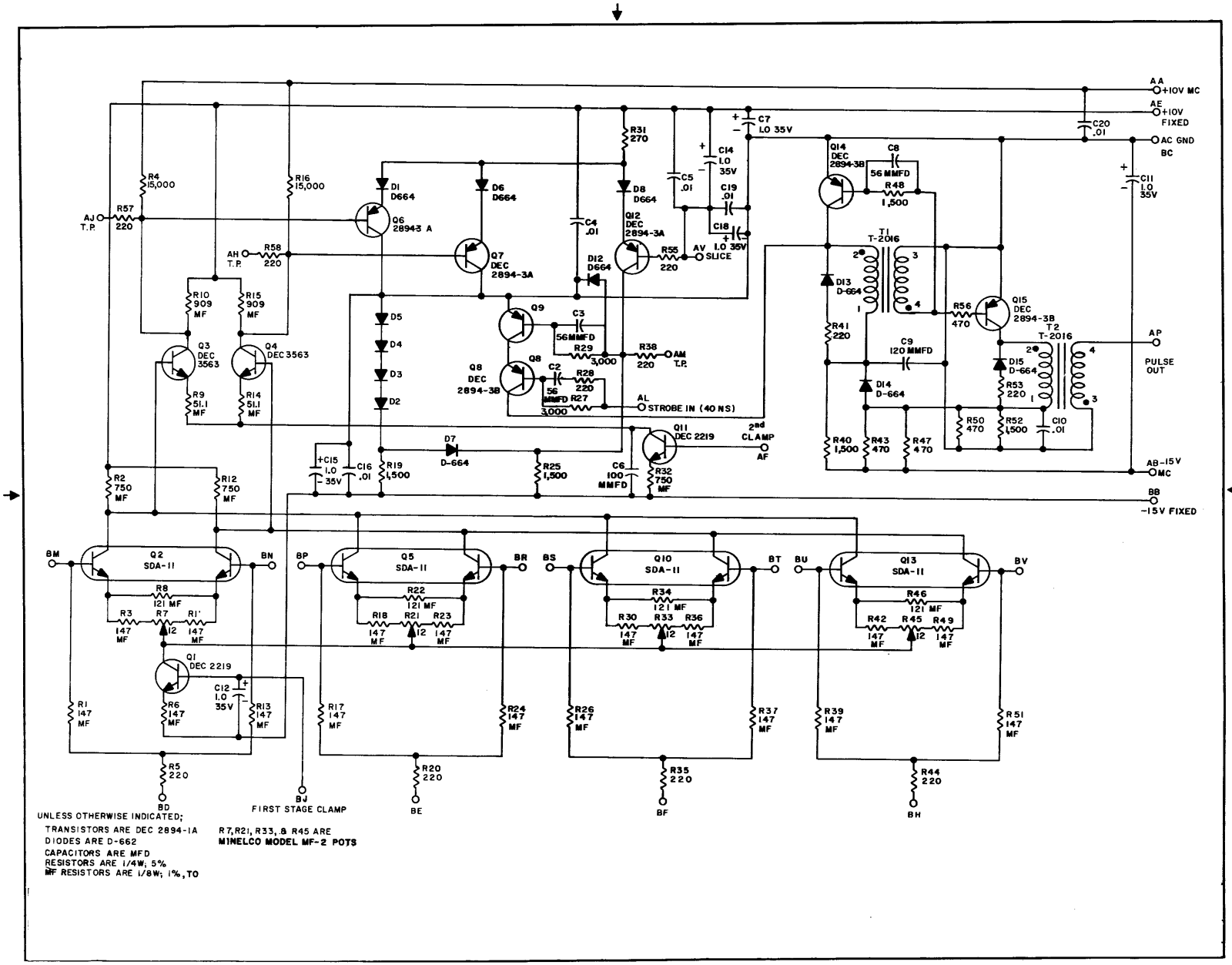


NOTE:
THIS PRINT IS FOR MAINT. & CHECK OUT ONLY

CD-D-164-0-MCR Margin Check Routine with Module Location. Rev. C



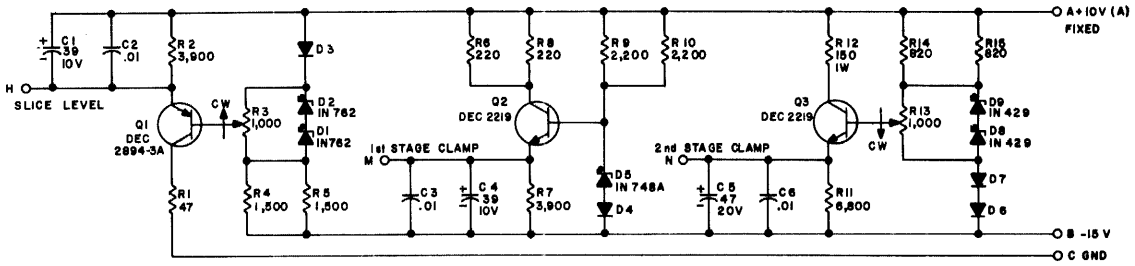
PW-D-164-0-DCPW DC Wiring for Type 164 Memory System. Rev. B



UNLESS OTHERWISE INDICATED;
TRANSISTORS ARE DEC 2894-1A
DIODES ARE D-662
CAPACITORS ARE MFD
RESISTORS ARE 1/4W, 5%
MF RESISTORS ARE 1/8W; 1%, TO

R7, R21, R33, & R45 ARE MINELCO MODEL MF-2 POTS

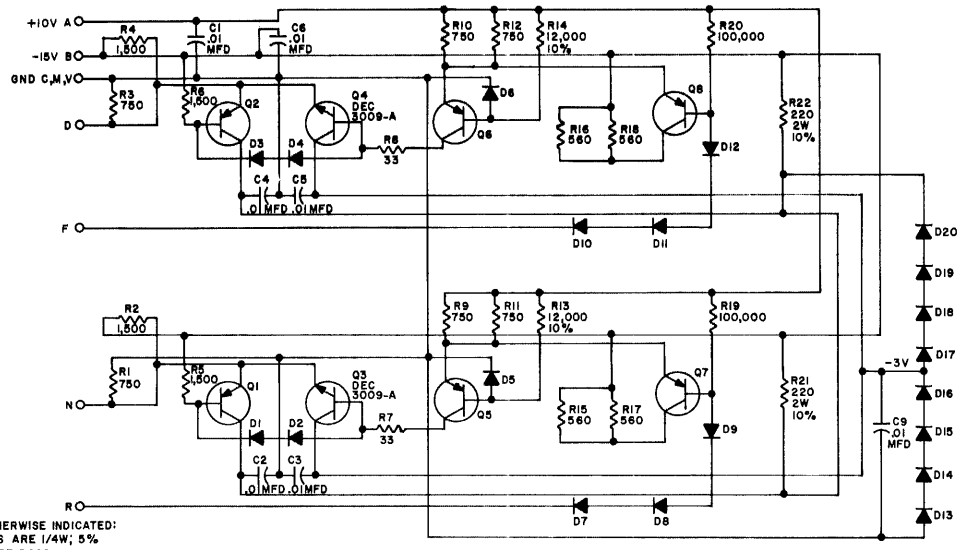
CS-C-G005-0-1 4 Input DC Sense Amplifier, G005. Rev. L



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W,5%
CAPACITORS ARE MFD
DIODES ARE D-662
R3 & R13 ARE A #275P

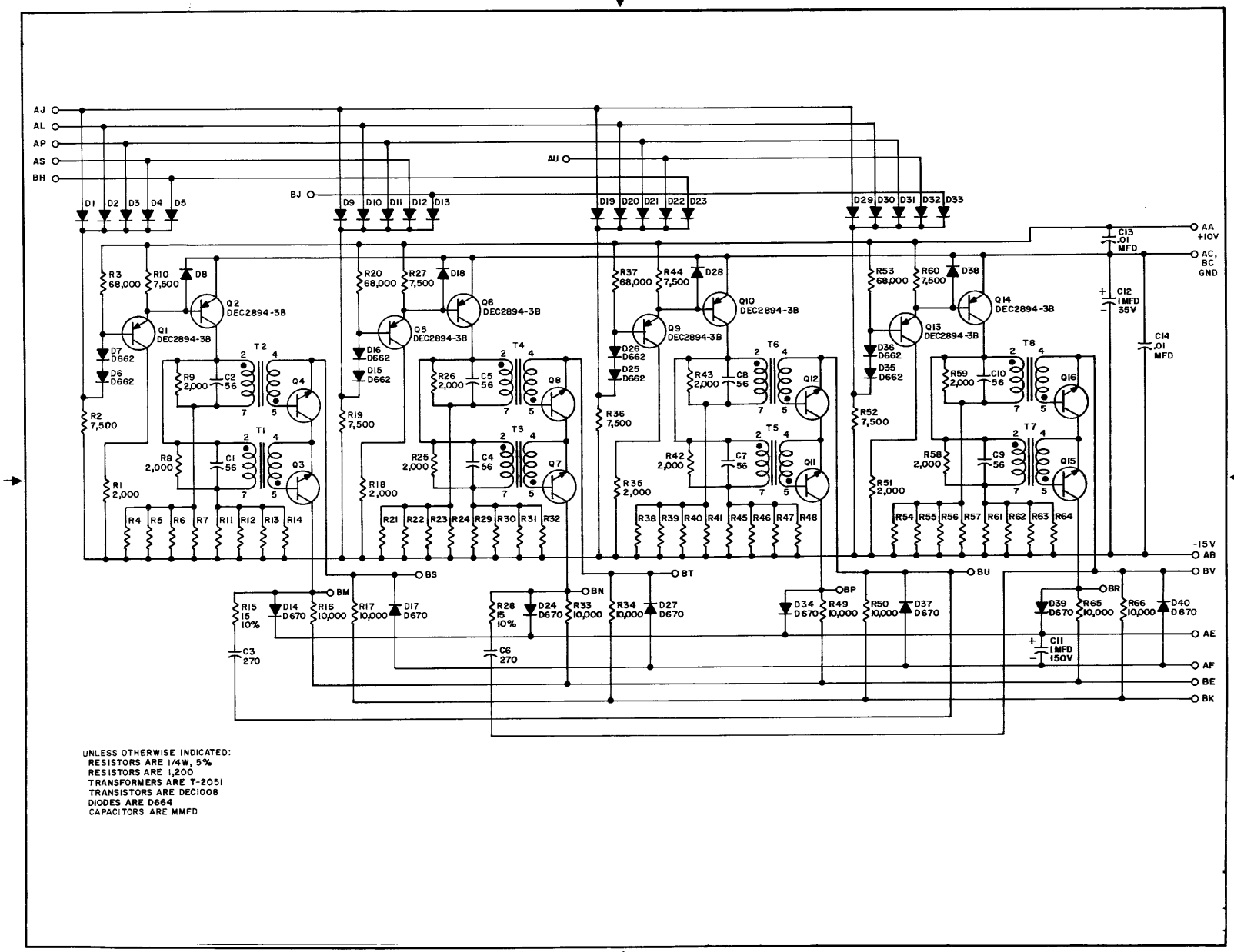
NOTES: * IN429 6.2V 5%
** IN762 6.5V 250mw 5%

CS-C-G008-0-1 Master Slice,
G008. Rev. C

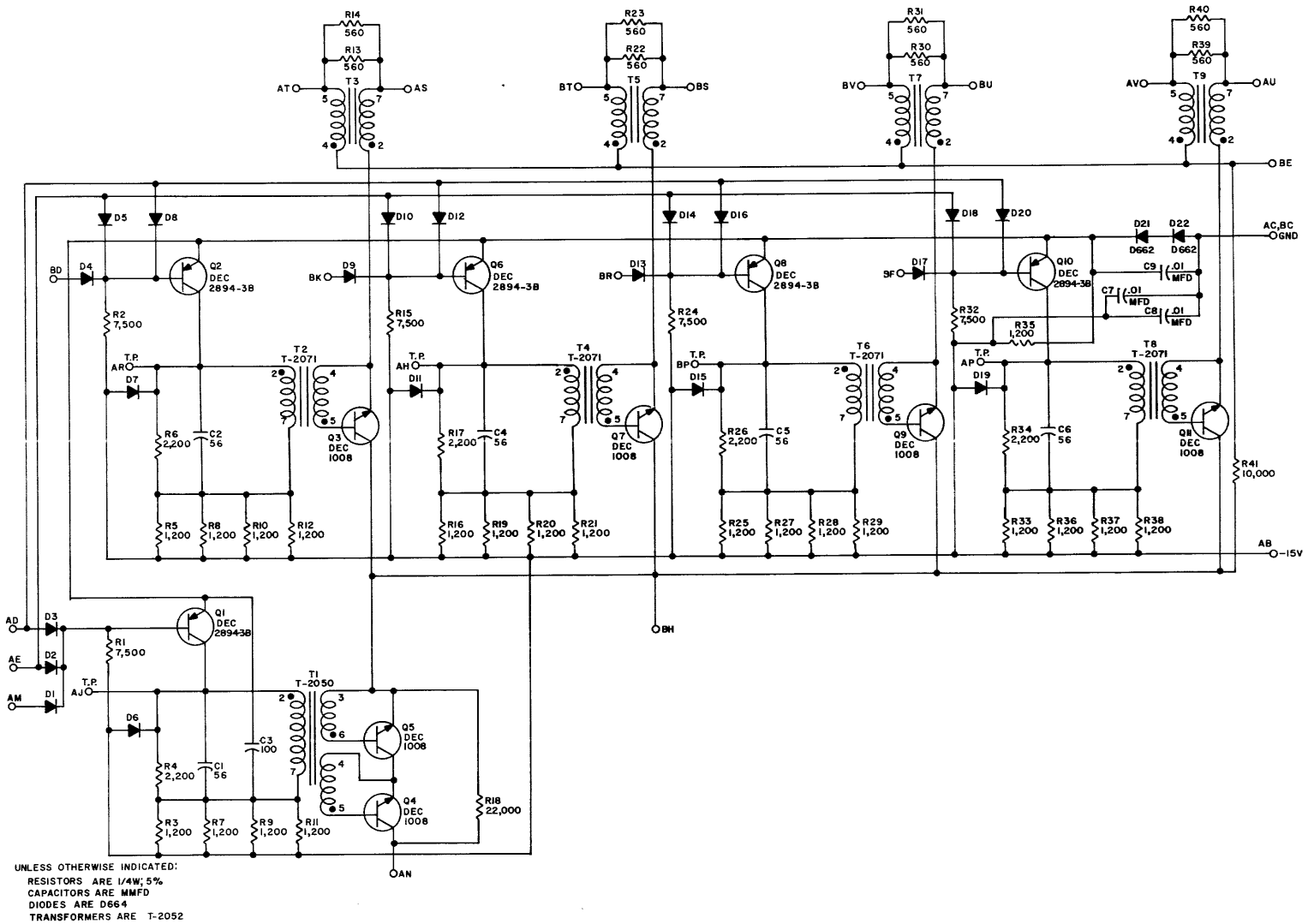


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D662
TRANSISTORS ARE DEC 2894-3A

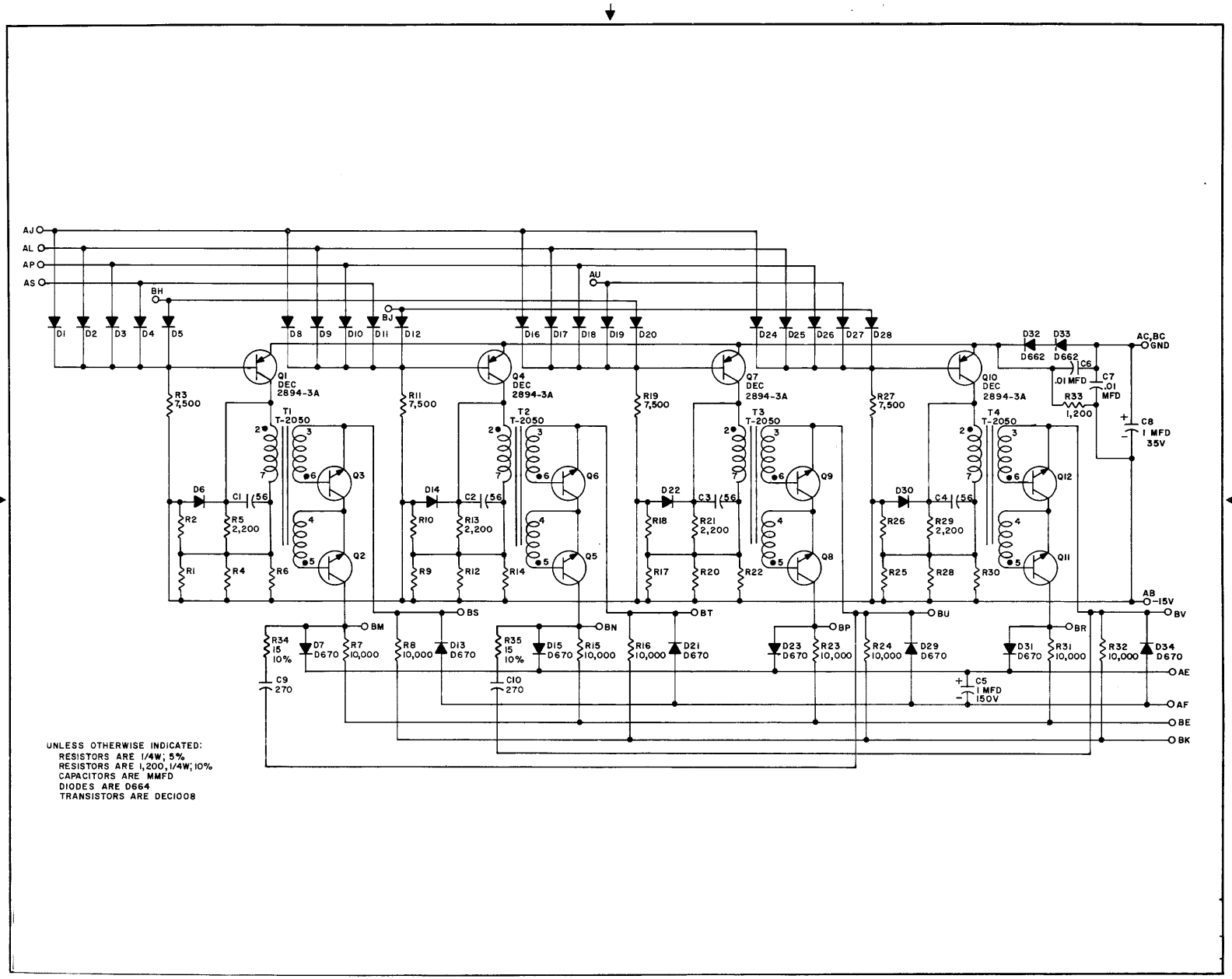
CS-B-G010-0-1 Sense Amplifier
Selector, G010. Rev. A



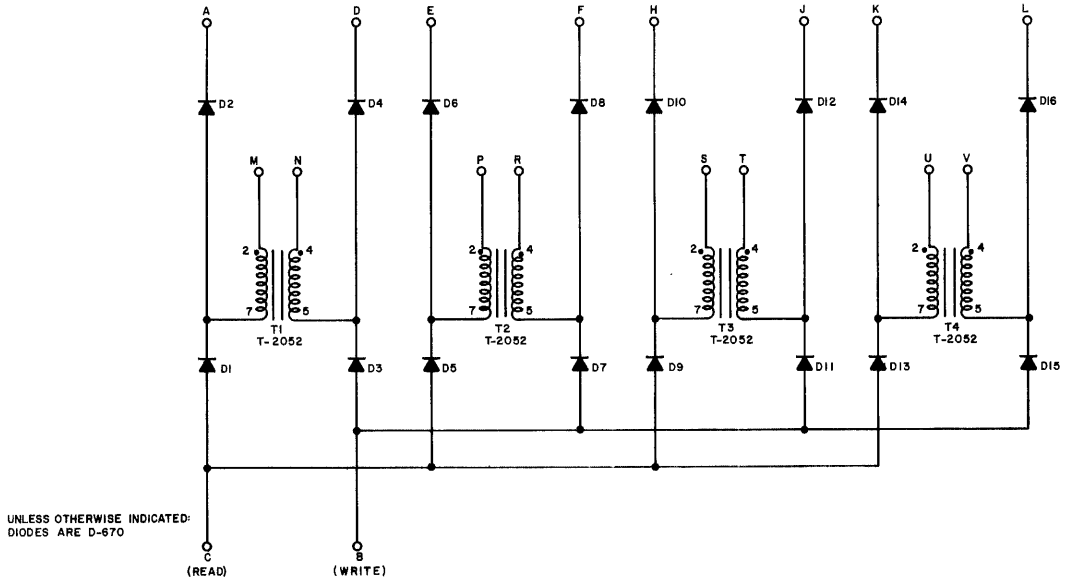
CS-C-G206-0-1 Memory Selector,
G206. Rev. C



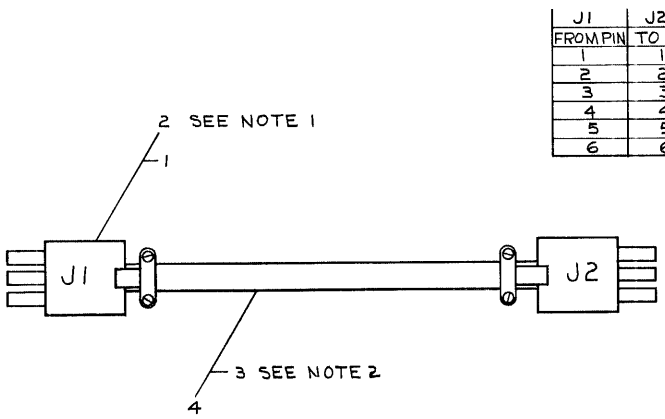
CS-C-G207-0-1 Inhibit Driver, G207. Rev. D



CS-C-G212-0-1 Memory Common Driver, G212



CS-B-G604 Memory Selector Matrix, G604



J1 FROM PIN	J2 TO PIN
1	1
2	2
3	3
4	4
5	5
6	6

NOTES

1. COVER SOLDER PIN CONNECTIONS WITH *2 (HY SHRINK TUBING.)
2. LENGTH WILL BE 4 FT. LONG.
3. TO BE USED FOR ADJACENT 164 OR MB10B MEMORY SYSTEMS.

QTY.	DESCRIPTION	PART NO.	ITEM NO.
AS REQD	TUBING EXTR SUFLEX ASTRA 105 #1		4
6	18 AWG STRANDED TEFLON WIRE (WHITE)		3
12	HY SHRINK TUBING #14 x 1/2 LG (RED)		2
2	PLUG #34-P-308-CCT CINCH JONES	34-P-308-CCT	1

PARTS LIST

IA-B-7405423-0-0 Marginal Check and Remote Control Cables for Installation Only. Rev. A

APPENDIX A
TYPE 169 PARITY OPTION

The Type 169 Parity Option is connected across the PDP-6 memory bus (MBUS). It is used to check the parity of each data word transferred between the central processor and the memory. In the write cycle, the parity of each data word being transferred to memory is checked. If the parity of the data word is even, a parity bit is generated and is routed to memory along with the data word. The data word including the parity bit is stored in memory with odd parity.

When a data word is transferred out of memory during a read cycle, the data word is checked for odd parity. If an even parity condition is located, an error condition exists. The parity option detects the error condition and reacts according to the selected operating mode.

The parity option will not check the data word parity or generate a parity bit when a fast memory control is referenced or when a memory plane returns a bypass signal.

A1 INSTALLATION

To install the parity option, the MBUS cable connectors from the central processor are disconnected at the memory and the cables are inserted into the parity option, according to Table A-1. Record the memory slot number from which the cables were removed in Table A-1. Then, install the supplied jumper cables between the parity option and the memory according to Table A-1.

Table A-1
Cable Installation

Processor End	Parity Option End	Parity Option End	Memory End
2L5 (DEC 10360)	1A1 (W028)	1A2 (W028)	
	1B1 (W028)	1B2 (W028)	
2L24 (DEC 10360)	1C1 (W028)	1C2 (W028)	
	1D1 (W028)	1D2 (W028)	
2E25 (DEC 10350)	1A31 (W028)	1A32 (W028)	
	1B31 (W028)	1B32 (W028)	

Table A-1 (cont)
Cable Installation

Processor End	Parity Option End	Parity Option End	Memory End
2J25 (DEC 10350	1C31 (W028) 1D31 (W028)	1C32 (W028) 1D32 (W028)	

A2 CONTROLS AND INDICATORS

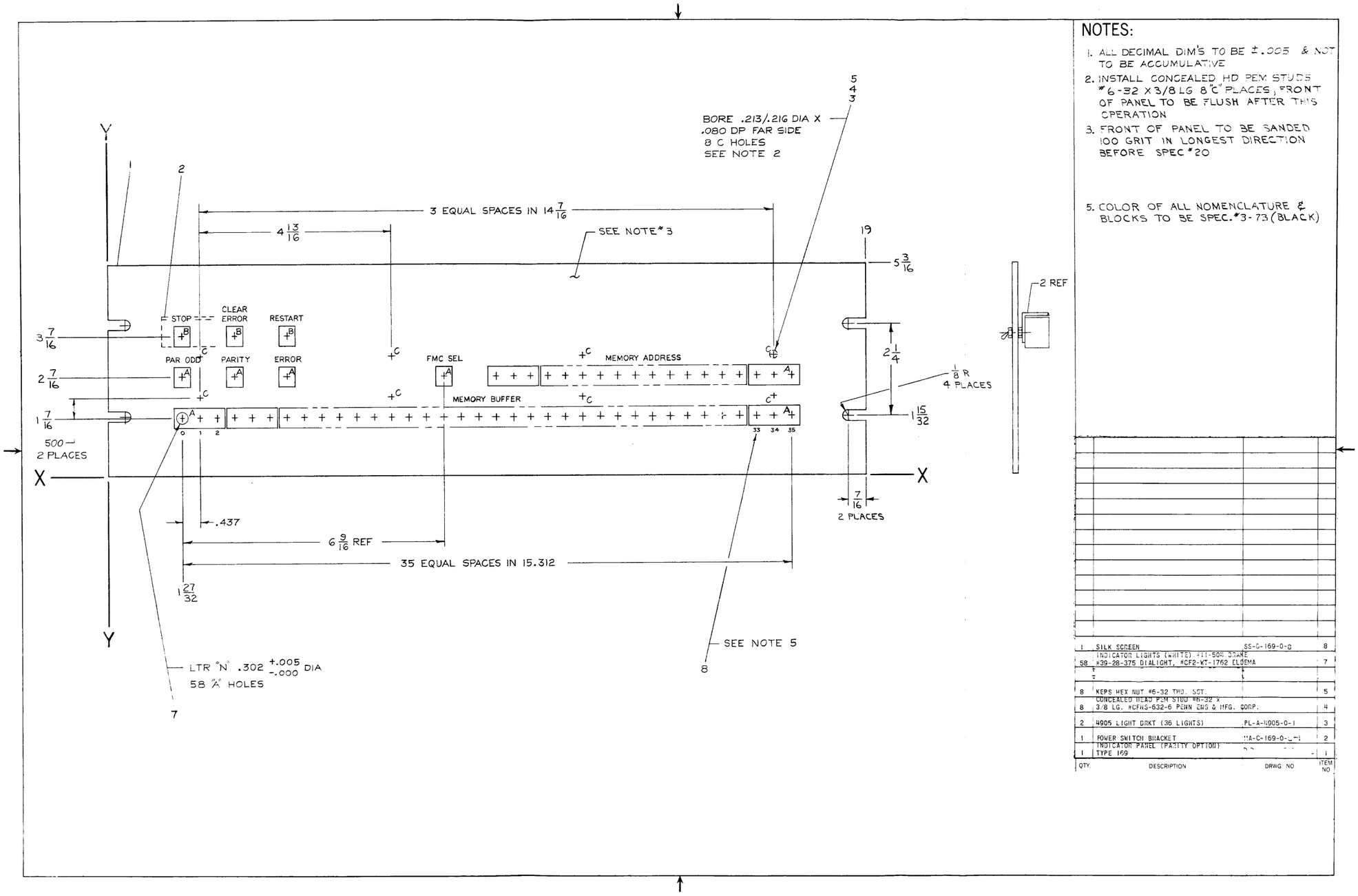
The controls and indicators for the parity option are contained on the indicator panel. Figure A-1 shows the indicator panel and Table A-2 contains a brief description of the function of each.

Table A-2
Controls and Indicators

Number	Nomenclature	Type	Function
1	STOP	Micro toggle switch	Selects Normal or Stop-on-Error operating mode.
2	PAR ODD	Indicator	Indicates odd parity
3	CLEAR ERROR	Push button switch	Clears PAR ERR flip-flop
4	PARITY	Indicator	Indicates the presence of a parity bit.
5	RESTART	Push button switch	Clears PAR ERR flip-flop, clears ERROR stop flip-flop, clears Memory Buffer flip-flops and generates RDRS signal.
6	ERROR	Indicator	Indicates a parity error
7	FMC SEL	Indicators	Indicates when a fast memory control is selected.
8	MEMORY BUFFER	36 Indicators	Displays the data word being transferred
9	MEMORY ADDRESS	18 Indicators	Displays the memory address being referenced.

A3 THEORY OF OPERATION

In this section, the circuit operation of the parity option during the write cycle, read cycle, and the read/pause/write cycle is discussed. When only a zone number is referenced, refer to drawing BS-D-169-0-POC. The other references in the text will refer to the drawing number containing the circuits under discussion.



NOTES:

1. ALL DECIMAL DIM'S TO BE ±.005 & NOT TO BE ACCUMULATIVE
2. INSTALL CONCEALED HD PEM STUDS #6-32 X 3/8 LG 8 "C" PLACES, FRONT OF PANEL TO BE FLUSH AFTER THIS OPERATION
3. FRONT OF PANEL TO BE SANDED 100 GRIT IN LONGEST DIRECTION BEFORE SPEC #20
5. COLOR OF ALL NOMENCLATURE & BLOCKS TO BE SPEC.#3-73 (BLACK)

QTY.	DESCRIPTION	DRWG. NO	ITEM NO
1	SILK SCREEN	SS-C-169-0-0	8
58	INDICATOR LIGHTS (WHITE) #II-60W SNAKE #39-28-375 DIALIGHT, #CF2-WT-1762 CLOEMA		7
8	KEPS HEX NUT #6-32 THD. SST.		5
8	CONCEALED HEAD PEM STUD #6-32 x 3/8 LG. #CFHS-632-6 PENN ENG & MFG. CORP.		4
2	4905 LIGHT DRKT (36 LIGHTS)	PL-A-4905-0-1	3
1	POWER SWITCH BRACKET	MA-C-169-0-[illegible]-1	2
1	INDICATOR PANEL (PARITY OPTION) TYPE 169		1

Figure A1 Indicator Panel (Parity Option) Type 169

A3.1 Write Cycle

When the central processor requests a write cycle, the PMA 18 through PMA 35 flip-flops (drawing BS-D-169-0-POMA) are cleared by the CLR PAR MEM ADRS signal (zone A2) which is generated from the PROC RQ signal (zone A1). After a 100-ns delay, the STRB PAR MEM ADRS signal (zone A3) is generated and the PMA flip-flops are set equal to the address presently being referenced.

In addition, at the start of the write cycle, the PAR MB 0 through PAR MB 35 flip-flops (drawing BS-D-169-0-POMB) and the parity flip-flop (zone A7) are cleared by the CLR PAR MEM BUF signal (zone B8) which is generated from the PROC RQ signal (zone B7). Then, the PAR MB flip-flops are connected to the parity option circuit (drawing BS-E-169-0-PO).

In the parity option circuit, the 1 and 0 sides of each PAR MB flip-flops are connected to a parity checking circuit. When odd parity is detected, the desired condition, no parity bit is generated. If even parity is detected, the WR RS (write restart) signal (zone B7), which signifies the end of the central processor write-access time, is ANDed with the PAR EVEN signal. The resultant signal, PAR BIT (zone B7), is transferred via the MBUS and stored in the parity plane of the memory.

A3.2 Read Cycle

When the central processor requests a read cycle, the PMA 18 through PMA 35 flip-flops are cleared and set equal to the address presently being referenced. At the same time, the parity flip-flop and the PAR MB 0 through PAR MB 35 flip-flops are cleared and a data word is placed on the MBUS. If the data word being transferred to the central processor via the MBUS contains a parity bit, the PAR BIT signal (zone B7) is ANDed with the PAR EVEN level and the resultant signal is used to set the parity flip-flop.

After the PAR MB flip-flops are cleared, they are set equal to the data word being transferred to the central processor. The output lines from the PAR MB flip-flops are routed to the parity option circuit along with the output lines from the parity flip-flop. In the parity option circuit, the parity of the data word, including the parity bit, is checked. Since the combination of the data word and the parity bit was stored in the memory with odd parity, the data word being transferred should cause the PAR ODD levels from the parity option circuit to be in the true condition. If an odd number of bits are lost from the data word during transfer, an error condition exists. When an error condition does exist, the generation of the RDRS signal to the central processor (zone B4), which signifies the end of the central processor read access time, is dependent upon the selected operating mode and is explained in Section A3.3.

The RDRS signal (zone B1) from the memory is used to start a 200 ns delay. The resultant signal from the delay is ANDed with the PAR EVEN level. If an error condition does exist, the resultant signal is used to generate the PAR ERROR signal which is routed to the central processor for further action and is used to set the PAR ERR flip-flop (zone A3).

A3.3 Read/Pause/Write Cycle

In this cycle, the read portion of the cycle is performed in an identical fashion as the read cycle explained above. The write portion of this cycle is performed in a slightly different fashion. The main difference between the write portion of the read/pause/write cycle and the write cycle is the way in which the PAR MB flip-flops are cleared. It is recalled that the PROC RQ signal was used at the start of the write cycle to generate the CLR PAR MEM BUF signal. In this cycle, the PROC RQ signal is generated at the start of the read portion and is not present at the start of the write portion. To generate the CLR PAR MEM BUF signal before the write portion of this cycle, the RD RS (read restart) signal starts a 200 ns delay and the resultant signal from the delay causes the CLR PAR MEM BUF signal to be generated, just prior to the write portion of the cycle. The CLR PAR MEM BUF signal clears the PAR MB flip-flops and the parity flip-flop.

A3.4 Operating Modes

The parity option can be operated in a normal mode or a stop-on-error mode. Either mode can be selected with S1 (zone D4 and C5) on the indicator panel. Differences between the two modes are explained below. In this section, circuit operation, when a fast memory control is selected and when the parity option is placed in by-pass, is also explained.

A3.4.1 Stop-on-Error Mode - This mode has no effect on the write cycle. During a read cycle, the RD RS signal (zone C2) from the memory is gated with the output from the parity option circuit and the STOP MODE signal. If an even parity exists, an error condition, the RD RS signal (zone C4) to the central processor is inhibited. At the same time, the PAR ERR, and the ERROR STOP flip-flops are set and the PAR ERROR (zone B3) signal is routed to the central processor. When this occurs, the transfer operation is stopped. The address being referenced and the data word are displayed on the indicator panel. To resume operation, the RESTART pushbutton (S3-zone C1) on the indicator panel is depressed. If the ERROR STOP (1) signal is true, the RESTART pushbutton sends a RD RS pulse to the central processor which restarts the processor. The RESTART pushbutton also starts a 100 ns delay which clears the ERROR STOP flip-flop.

A3.4.2 Normal Mode - In this mode, the write cycle is not affected. During a read cycle, the RD RS signal is returned to the central processor without a delay except for the logic delay. If an error condition does exist, the PAR ERR flip-flop is set and the PAR ERROR signal is returned to the central processor for further action. Normal operation continues without an interruption.

A3.4.3 Fast Memory Control Operation - When a fast memory control is selected, parity of the transfer is not checked and the parity option circuit operation is not affected.

A3.4.4 BYPASS Operation - When the parity plane in the memory is used for storing information other than parity information or when the parity bit is not in the stack the parity option must be bypassed. A jumper is inserted in the memory, when parity is not used, to generate the PAR BYPASS signal that sets the PAR BYPASS flip-flop. The information is then transferred without checking parity.

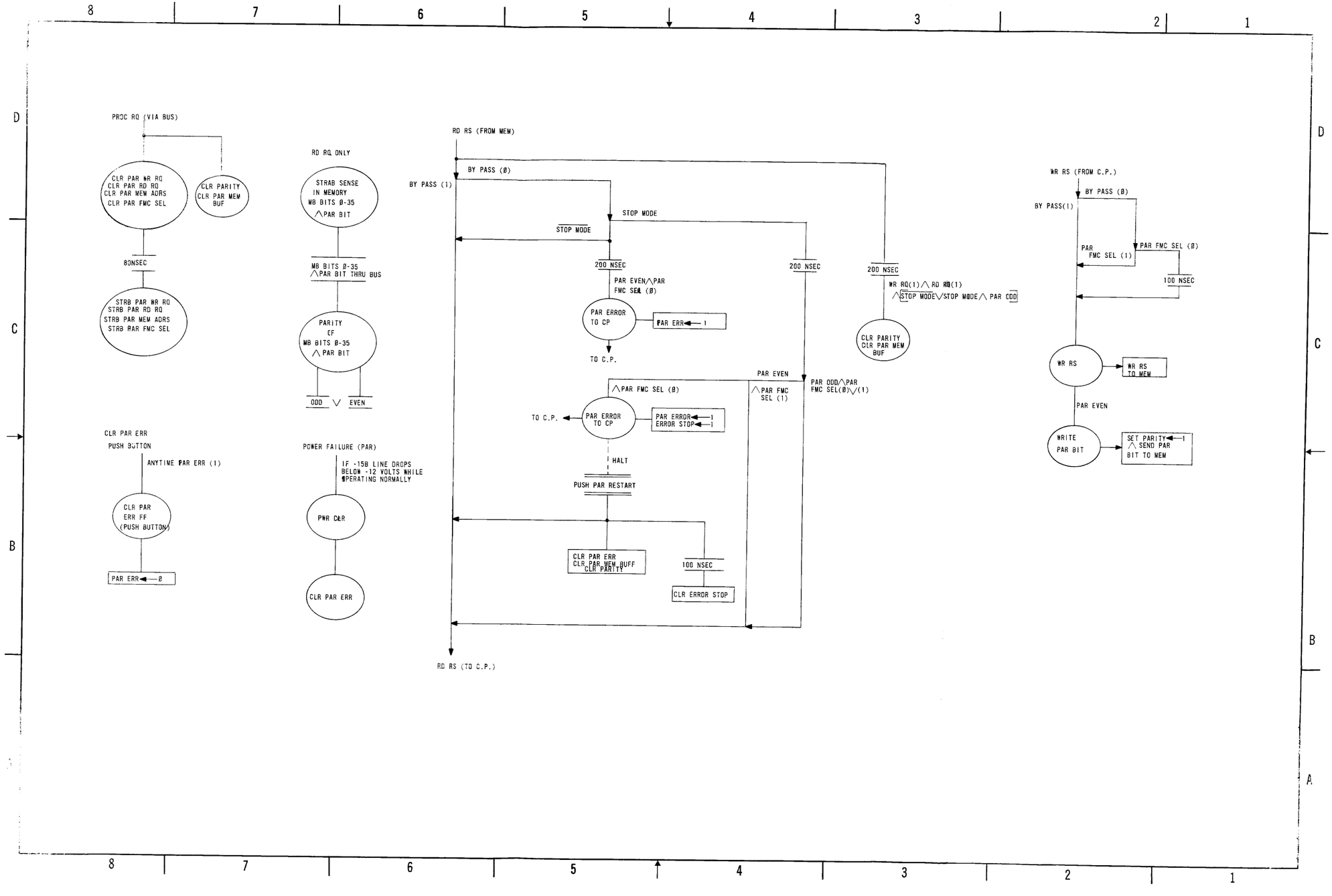
A4 ENGINEERING DRAWINGS

This section contains reduced copies of the engineering drawings required for understanding and maintaining the Type 169 Parity Option. The drawings are in addition to a complete set of full-size drawings supplied with each system. Should any discrepance exist between the drawings in this manual and those supplied with the equipment, assume the full-size drawings are correct.

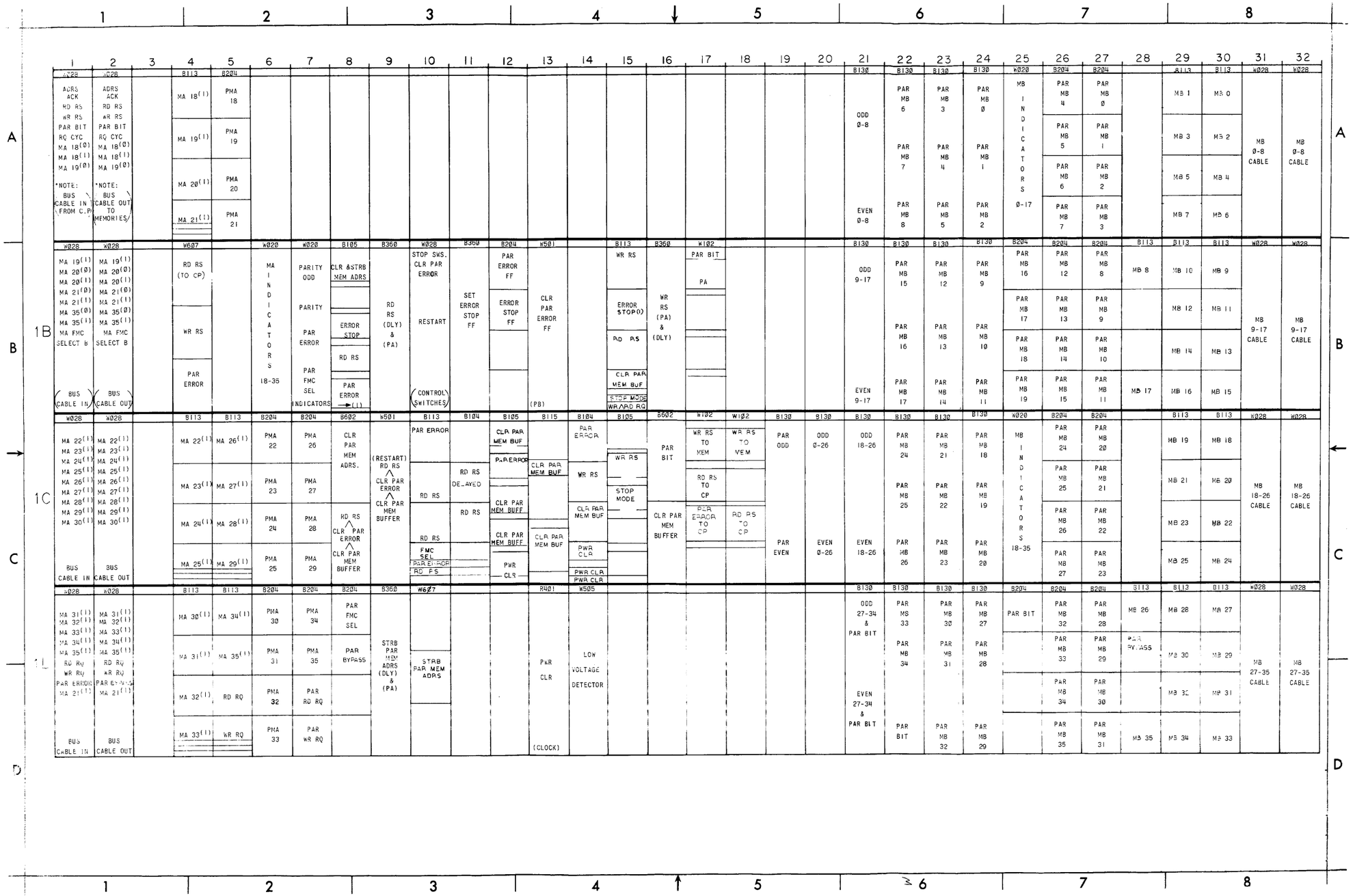
Standard DEC drawing terminology is used in the drawing contained in this appendix. For an explanation of DEC logic symbology and information on the drawings, the reader can refer to Appendix 1 of the Arithmetic Processor 166 Instruction Manual, F-67 (166).

Type 169 Parity Option Engineering Drawings

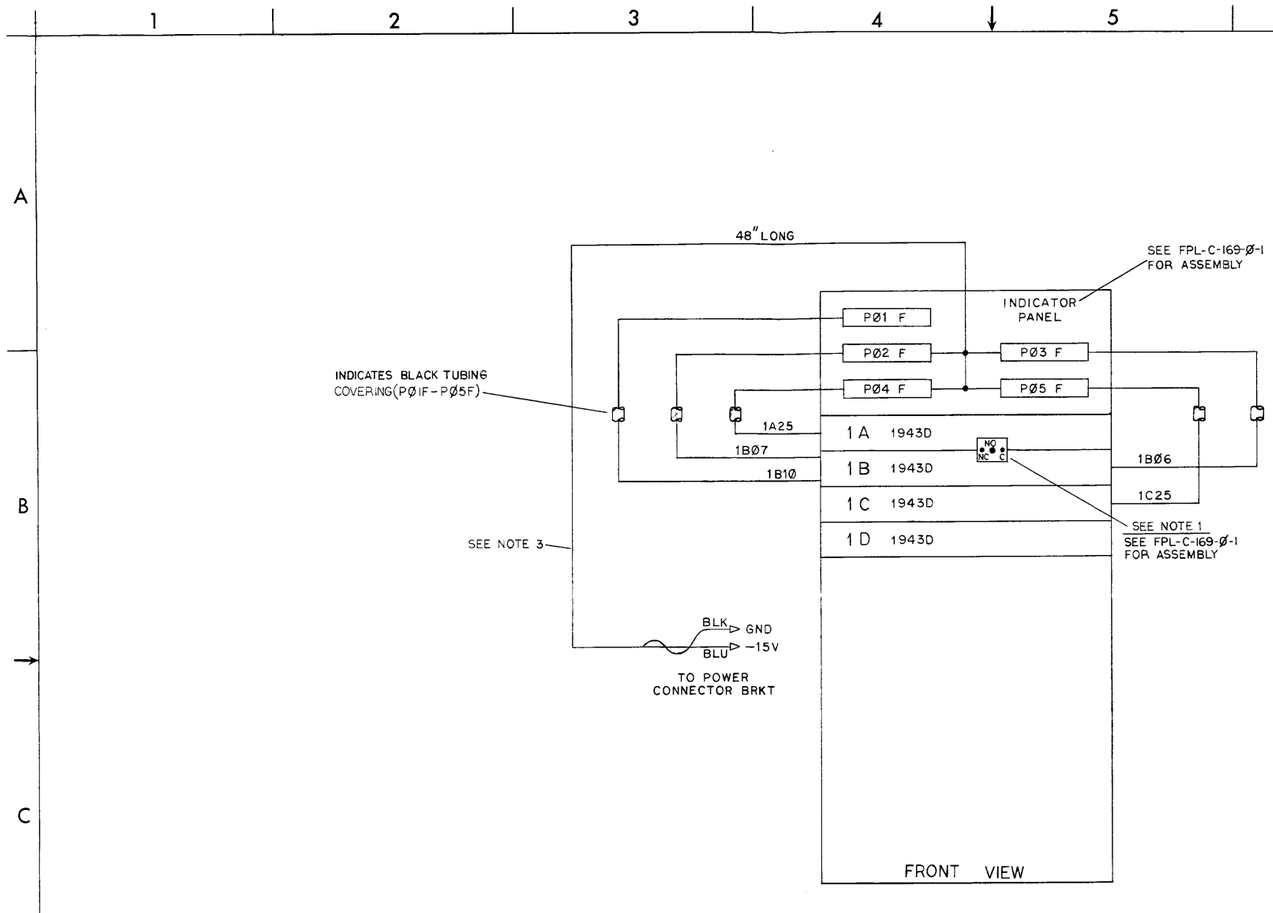
BS-E-169-0-PO
BS-D-169-0-POMA
BS-D-169-0-POMB (2 sheets)
BS-D-169-0-POC
PW-D-169-0-PW
SD-D-169-0-SBD
CD-D-169-0-WLCD
UML-D-169-0-UML
FD-D-169-0-5
MAD-D-169-0-8



D-FD-169-0-5 Memory Parity Option
Type 169. Rev. A



UML-D-169-0-UML Memory Parity Option
UML. Rev. A



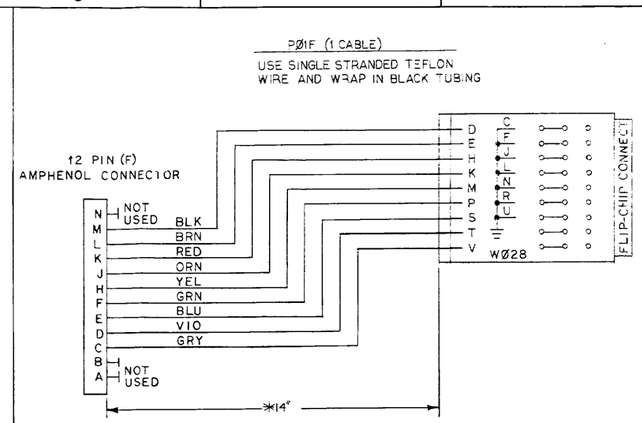
NOTES

1. MICRO TOGGLE SWITCH (FOR MAINTENANCE PARITY ERROR CHECK) SPDT MOUNT ON BRACKET ABOVE 1B13 & 1B16

2. A. PØ1F IS A 12 PIN AMPHENOL FEMALE PLUG

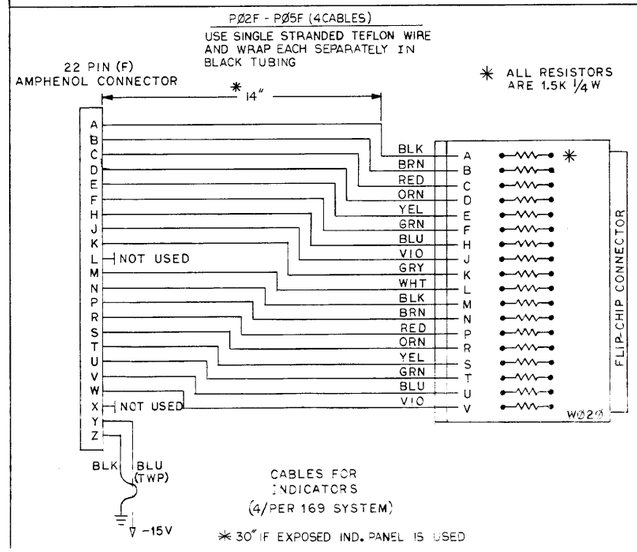
   B. PØ2F THRU PØ5F ARE 22 PIN AMPHENOL FEMALE PLUGS.

3. A. PIN Z OF PØ2F THRU PØ5F ARE BUSSED TOGETHER BY TWP BLK
   B. PIN Y OF PØ2F THRU PØ5F ARE BUSSED TOGETHER BY TWP BLU
   C. WIRE TWP BLU/BLK FROM PØ4F TO POWER CONNECTOR BRKT



CABLE FOR CONTROL SWITCHES
(1/PER 169 SYSTEM)

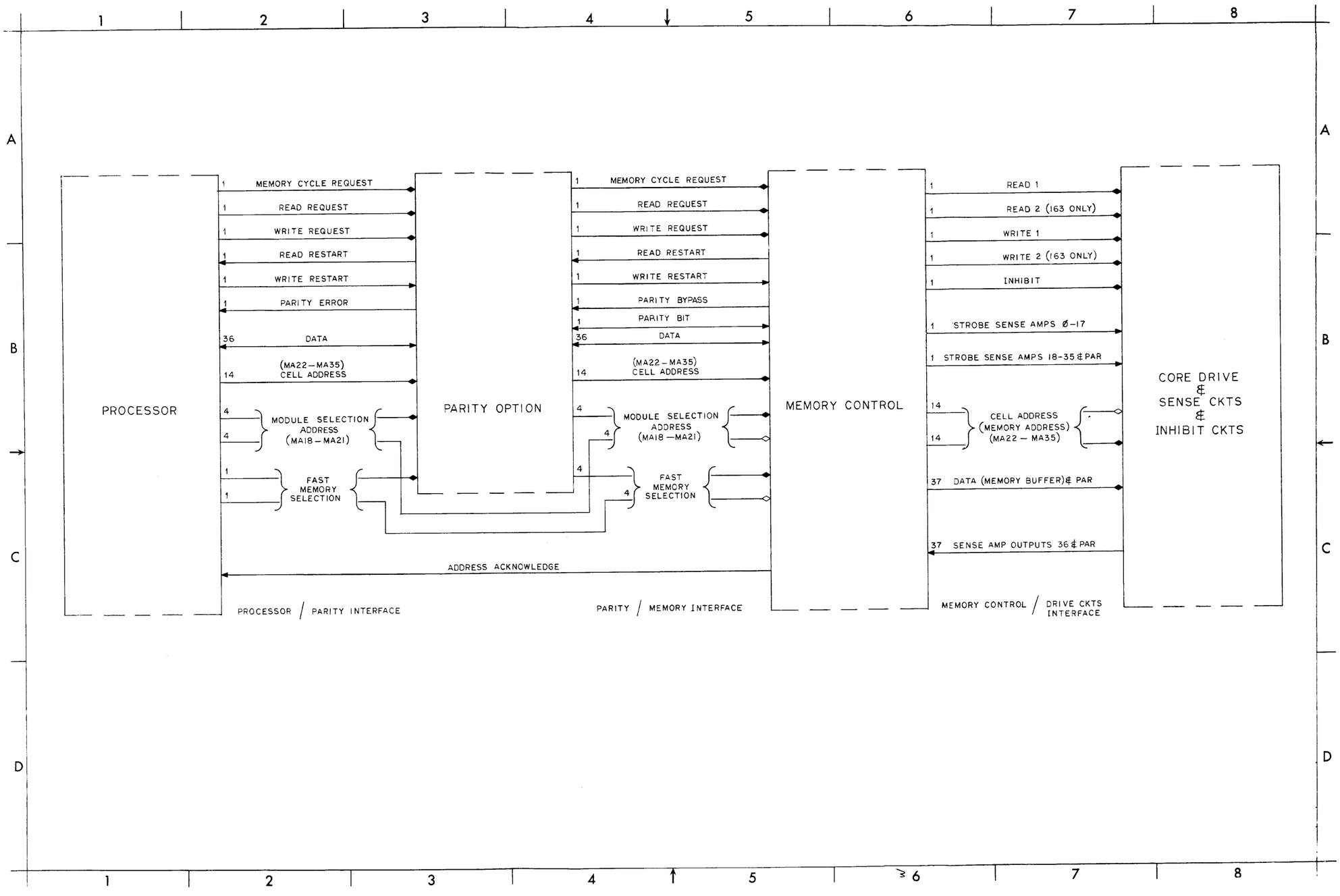
* 30" IF EXPOSED IND. PANEL IS USED



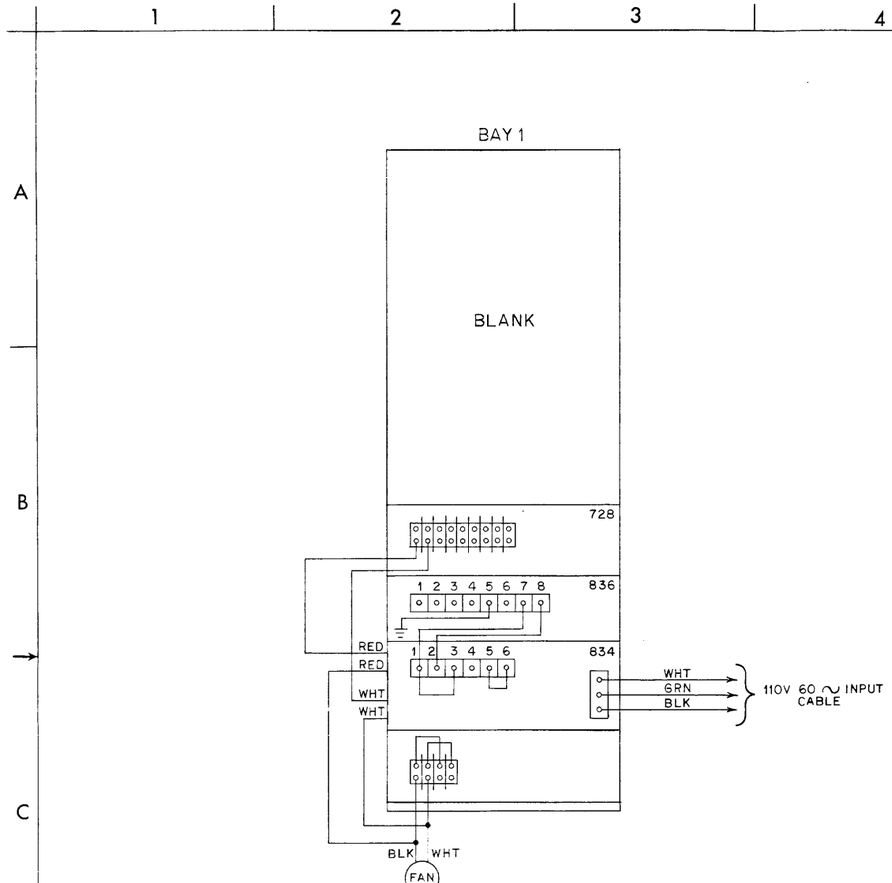
CABLES FOR INDICATORS
(4/PER 169 SYSTEM)

* 30" IF EXPOSED IND. PANEL IS USED

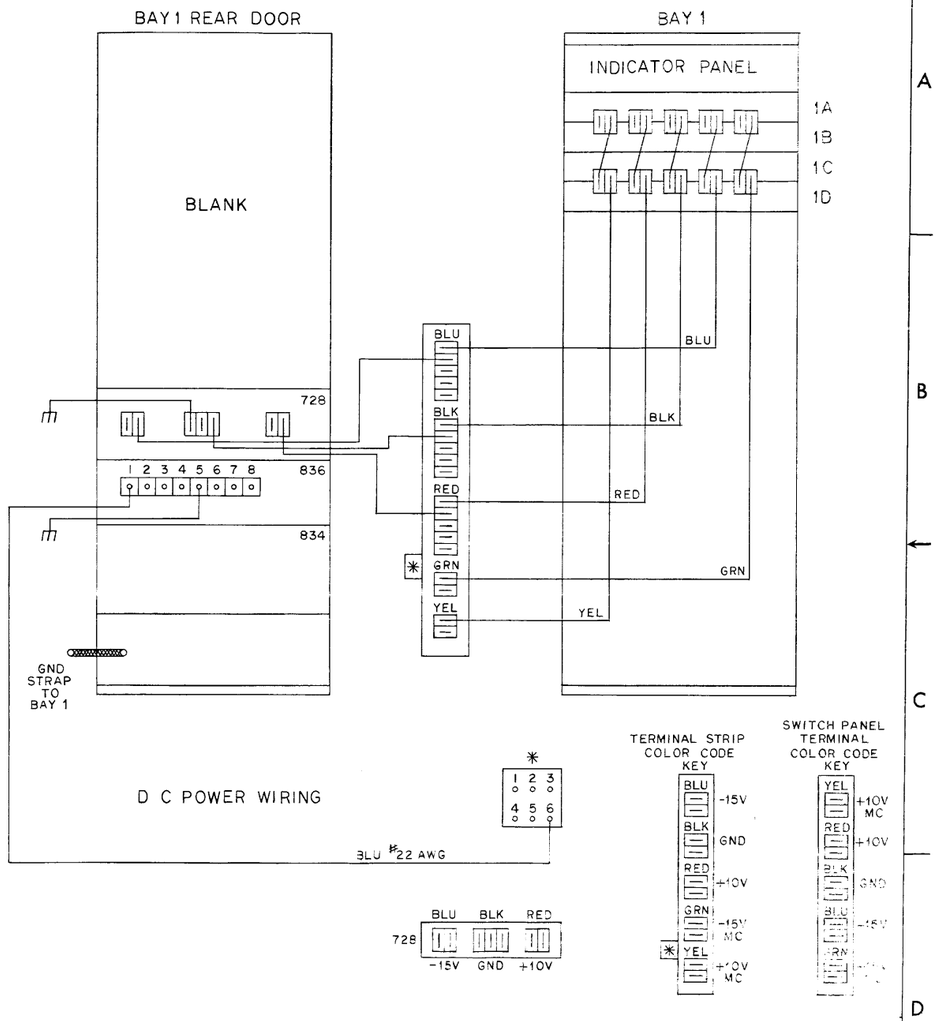
CD-D-169-0-WLCD Indicator & Switches
Cable Diagram Type 169 Parity Option
Rev. A



SD-D-169-0-SBD Type 169 Parity Option
System Block Diagram. Rev. A

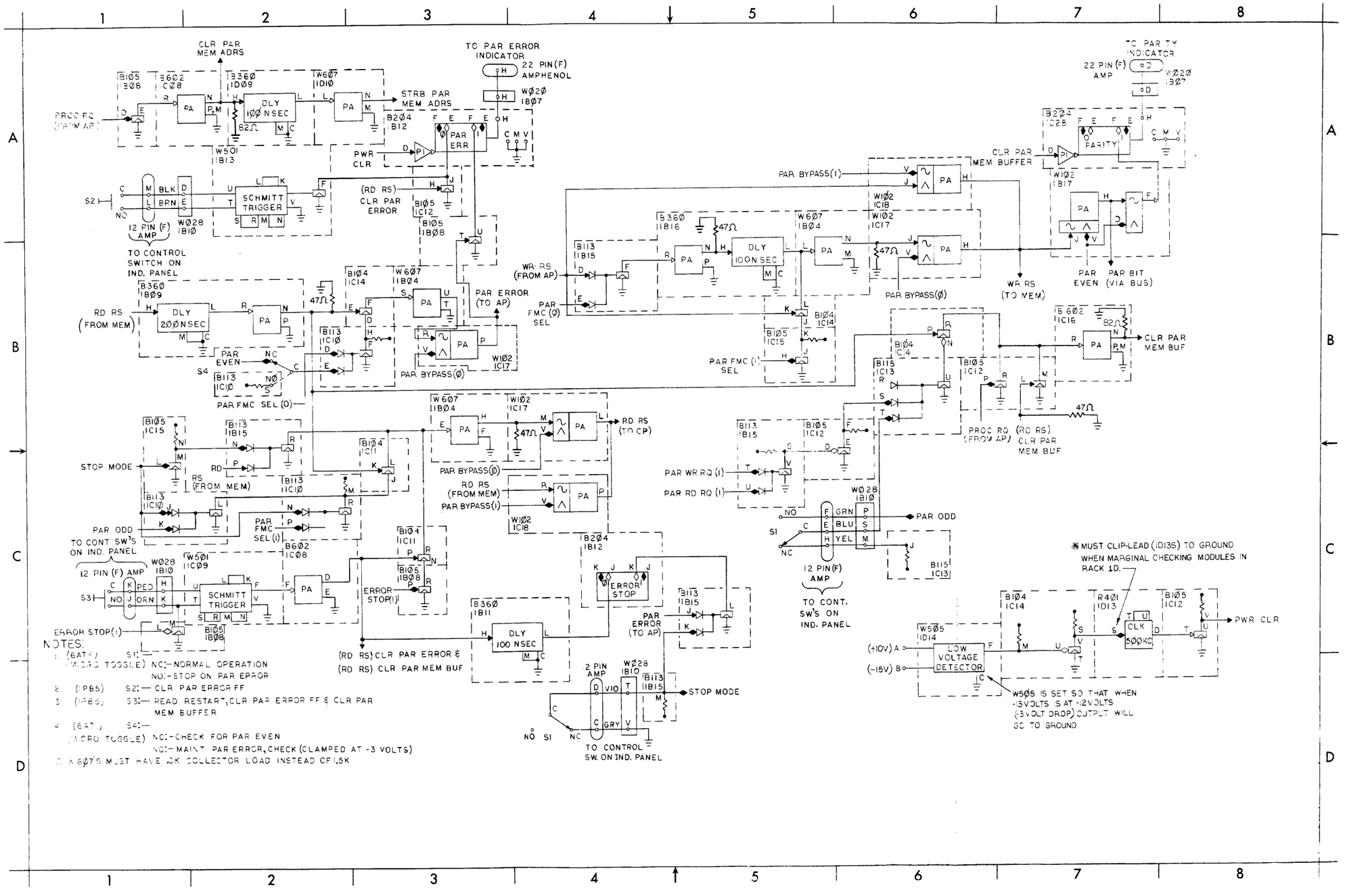


*A-C POWER WIRING



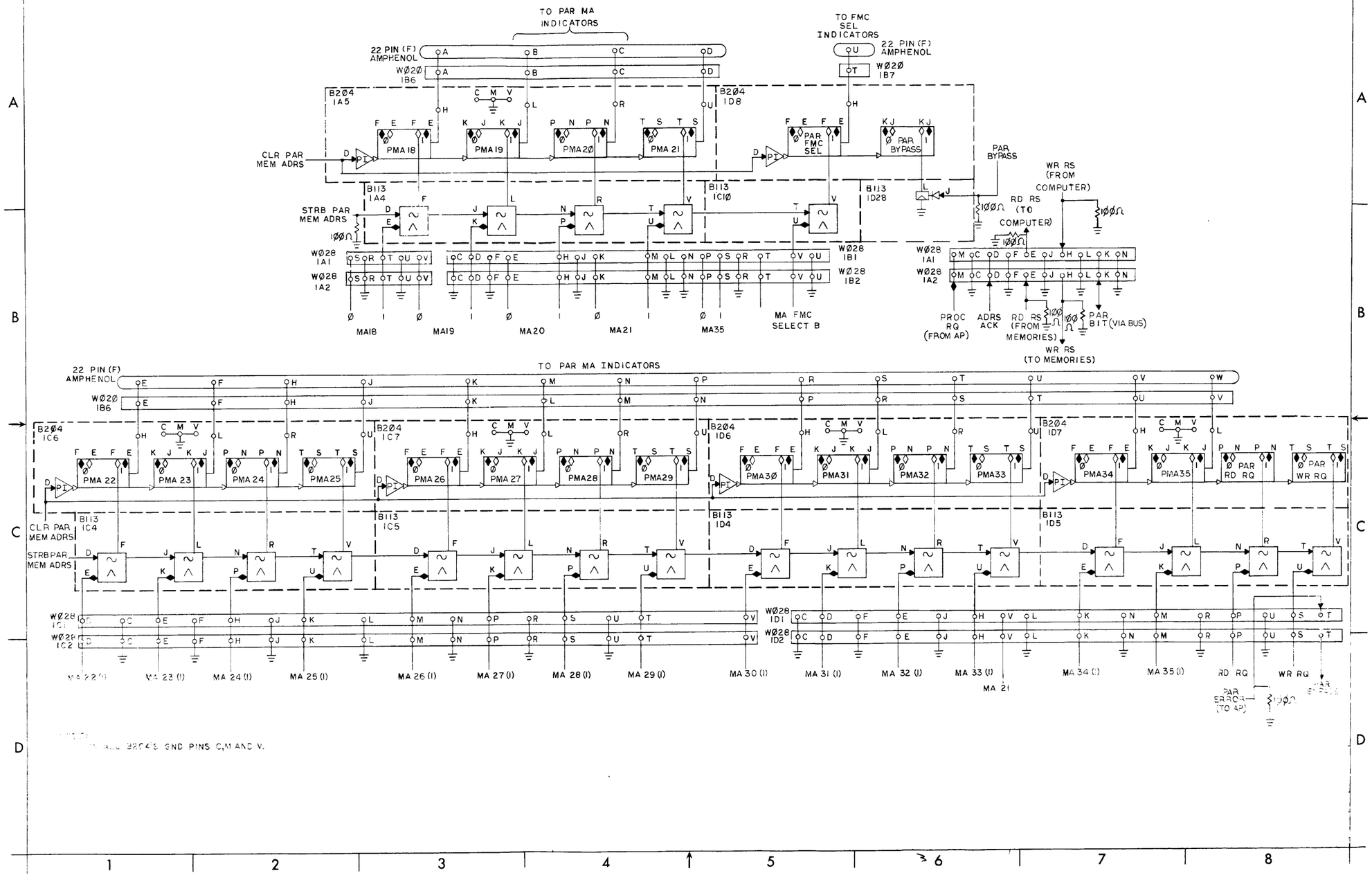
D C POWER WIRING

PW-D-169-0-PW AC-DC Wiring
Type 169 Parity Option

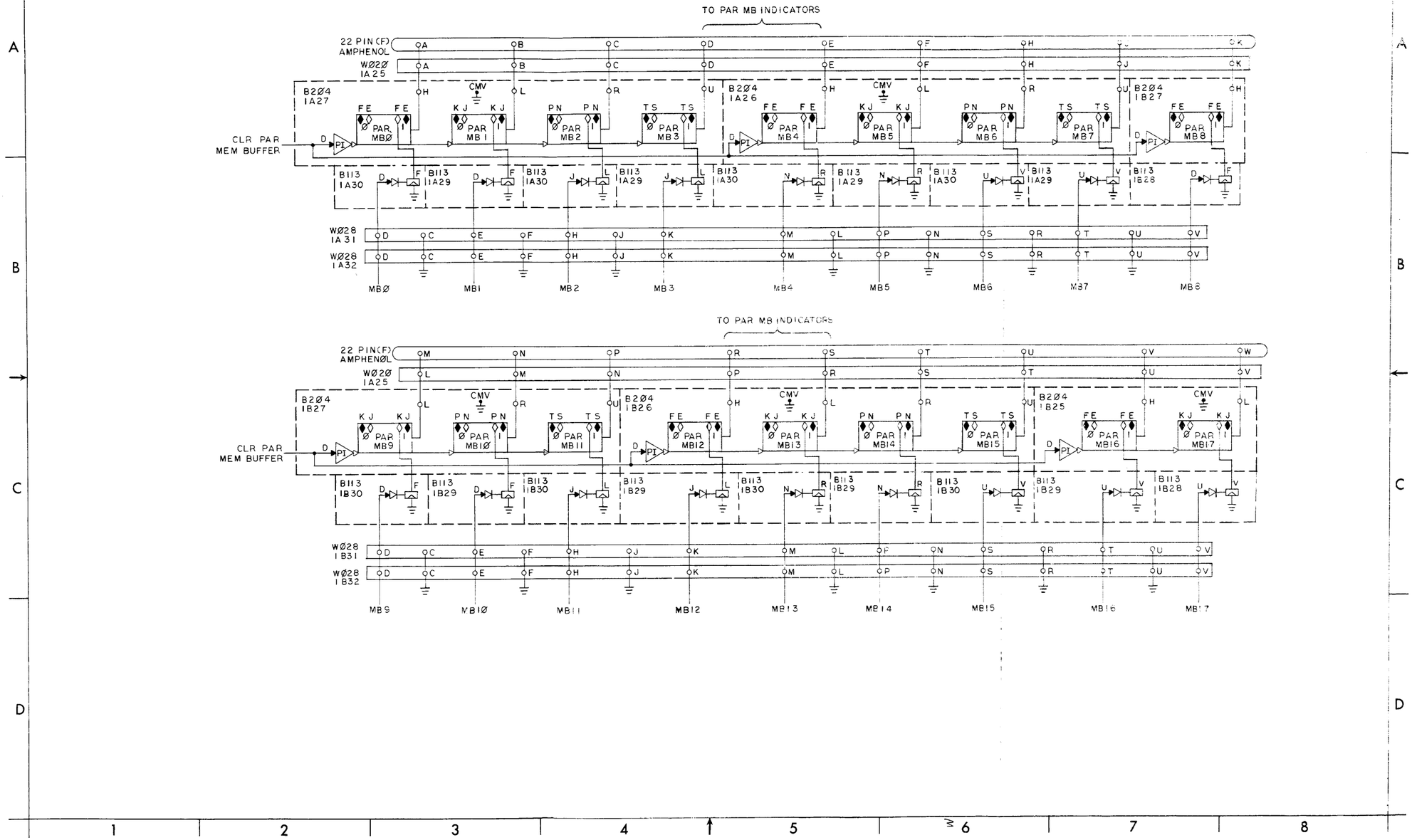


NOTES:

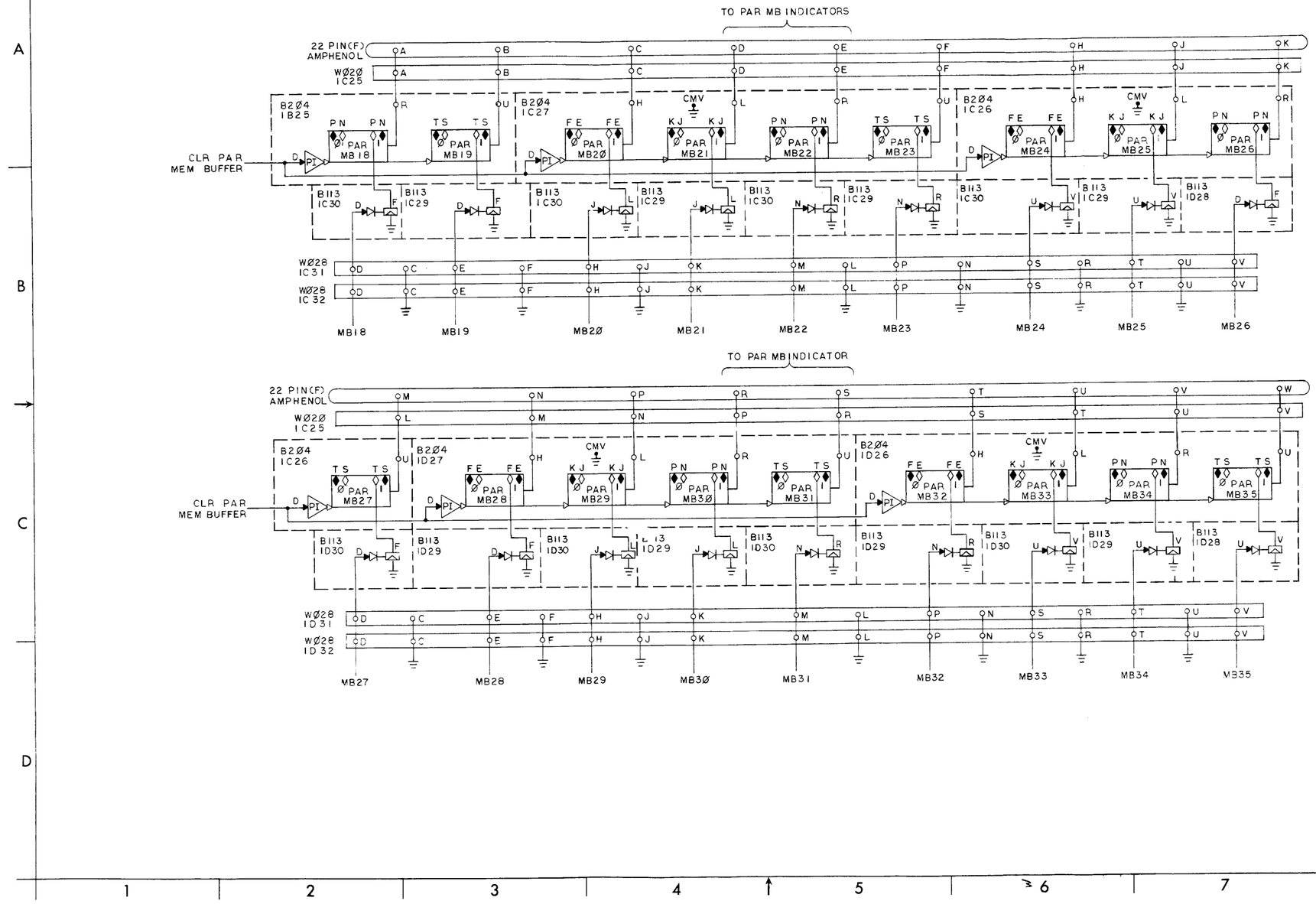
1. (6AT4) S1: (MICRO TOGGLE) NC:—NORMAL OPERATION
   NO:—STOP ON PAR ERROR
2. (1PB6) S2:— CLR PAR ERROR FF
3. (1PB6) S3:— READ RESTART; CLR PAR ERROR FF & CLR PAR MEM BUFFER
4. (6AT4) S4:— (MICRO TOGGLE) NC:—CHECK FOR PAR EVEN
   NO:—MAINT. PAR ERROR CHECK (CLAMPED AT -3 VOLTS)
5. A8Ø78 MUST HAVE 2K COLLECTOR LOAD INSTEAD OF 1.5K



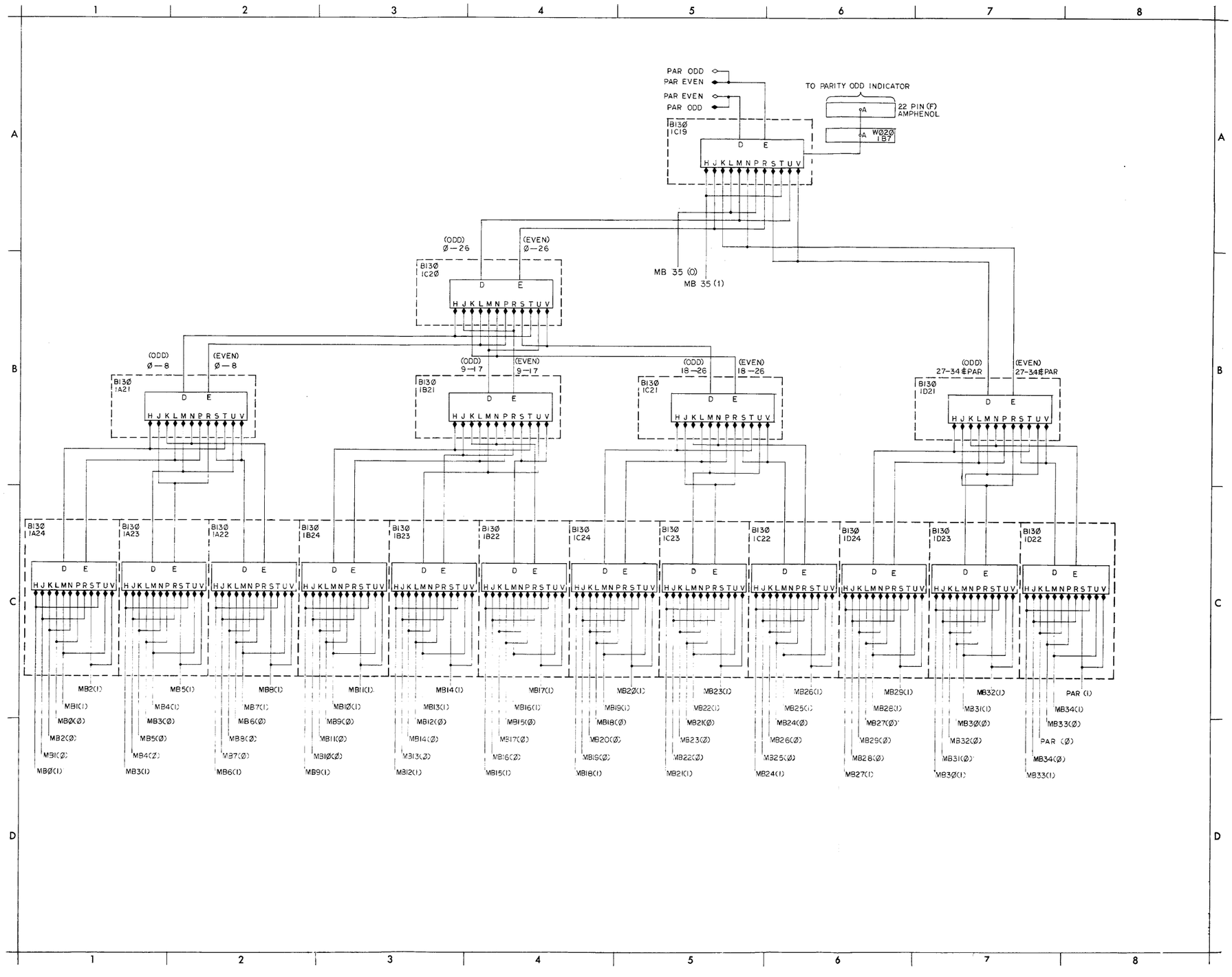
BS-D-169-0-POMA Memory Address Parity
Option Type 169. Rev. A

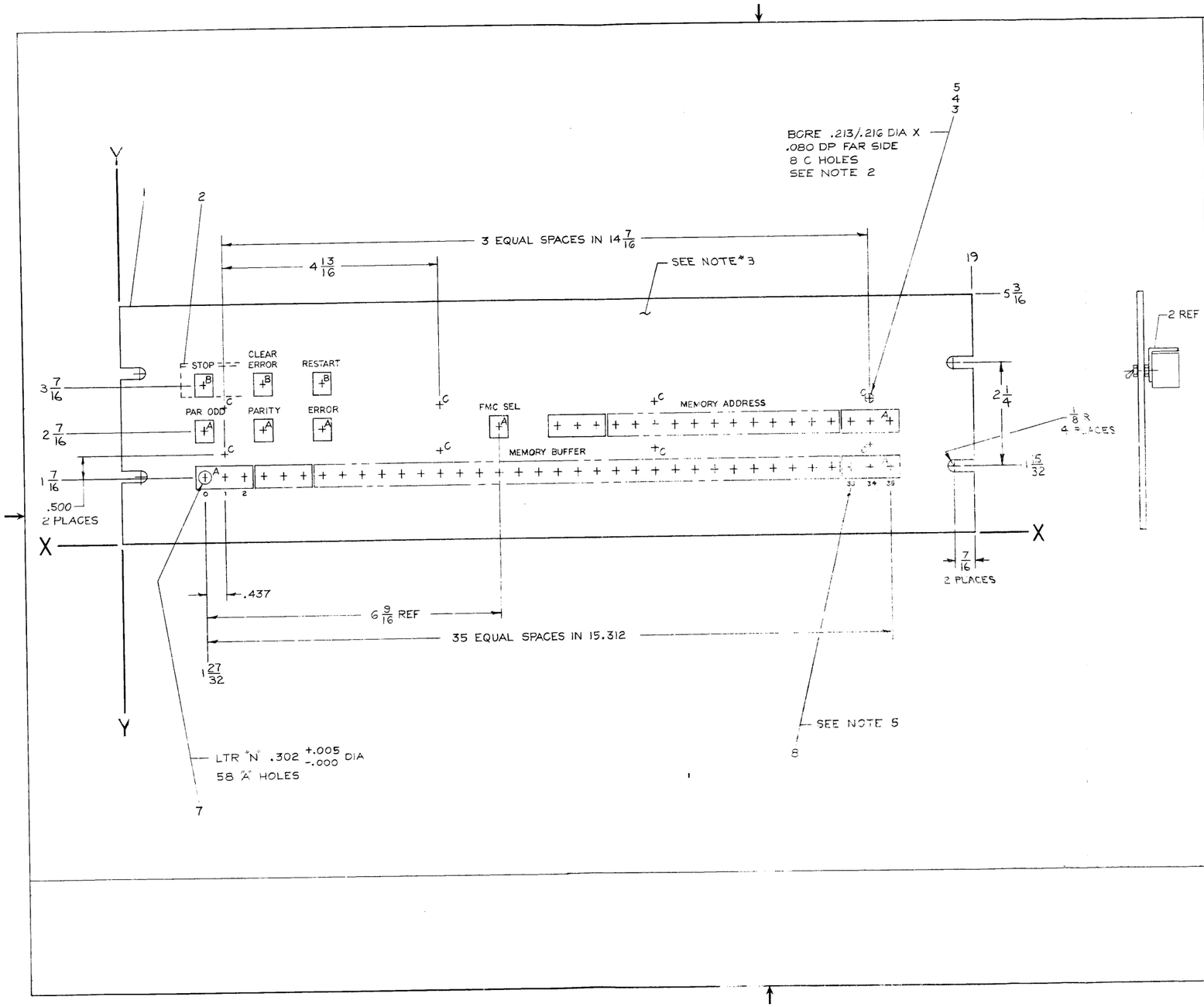


BS-D-169-0-POMB PAR MB Bits 0-17 Memory Parity Option Type 169. Rev. A



BS-D-169-0-POMB PAR MB Bits 18-35 Memory Parity Option Type 169. Rev. A


PAR ODD
PAR EVEN
PAR EVEN
PAR ODD
TO PARITY ODD INDICATOR
22 PIN (F) AMPHENOL
W020 187
BI3Ø IC19
D E
H J K L M N P R S T U V
MB 35 (Ø)
MB 35 (1)
(ODD) Ø—26
(EVEN) Ø—26
BI3Ø IC2Ø
(ODD) Ø—8
(EVEN) Ø—8
BI3Ø IA21
(ODD) 9—17
(EVEN) 9—17
BI3Ø IB21
(ODD) 18—26
(EVEN) 18—26
BI3Ø IC21
(ODD) 27-34 ¢PAR
(EVEN) 27-34 ¢PAR
BI3Ø ID21
BI3Ø IA24
BI3Ø IA23
BI3Ø IA22
BI3Ø IB24
BI3Ø IB23
BI3Ø IB22
BI3Ø IC24
BI3Ø IC23
BI3Ø IC22
BI3Ø ID24
BI3Ø ID23
BI3Ø ID22
MB2(1)
MB1(1)
MBØ(Ø)
MB2(Ø)
MB1(Ø)
MBØ(1)
MB5(1)
MB4(1)
MB3(Ø)
MB5(Ø)
MB4(Ø)
MB3(1)
MB8(1)
MB7(1)
MB6(Ø)
MB8(Ø)
MB7(Ø)
MB6(1)
MB11(1)
MB10(1)
MB9(Ø)
MB11(Ø)
MB10(Ø)
MB9(1)
MB14(1)
MB13(1)
MB12(Ø)
MB14(Ø)
MB13(Ø)
MB12(1)
MB17(1)
MB16(1)
MB15(Ø)
MB17(Ø)
MB16(Ø)
MB15(1)
MB20(1)
MB19(1)
MB18(Ø)
MB20(Ø)
MB19(Ø)
MB18(1)
MB23(1)
MB22(1)
MB21(Ø)
MB23(Ø)
MB22(Ø)
MB21(1)
MB26(1)
MB25(1)
MB24(Ø)
MB26(Ø)
MB25(Ø)
MB24(1)
MB29(1)
MB28(1)
MB27(Ø)
MB29(Ø)
MB28(Ø)
MB27(1)
MB32(1)
MB31(1)
MB30(Ø)
MB32(Ø)
MB31(Ø)
MB30(1)
PAR (1)
MB34(1)
MB33(Ø)
PAR (Ø)
MB34(Ø)
MB33(1)



NOTES:

1. ALL DECIMAL D.M'S TO BE ±.005 & NOT TO BE ACCUMULATIVE
2. INSTALL CONCEALED HD PEM STUDS #6-32 X 3/8 LG 8 "C" PLACES, FRONT OF PANEL TO BE FLUSH AFTER THIS OPERATION
3. FRONT OF PANEL TO BE SANDED 100 GRIT IN LONGEST DIRECTION BEFORE SPEC *20
5. COLOR OF ALL NOMENCLATURE & BLOCKS TO BE SPEC.*3-73 (BLACK)

QTY.	DESCRIPTION	DRWG. NO.	ITEM NO.
1	SILK SCREEN	SS-D-169-0-8	8
59	INDICATOR LIGHTS (WHITE) *11-807 DRAKE #39 28-175 DIALIGHT, #CF2-WT-1762 ELDEMA		7
8	KEPS HEX NUT #6-32 THD. DOT.		5
8	CONCEALED HEAD PEM STUD #6-32 x 3/8 LG. #CFHS-632-6 PENN ENG & MFG. CORP.		4
2	4905 LIGHT DRKT (36 LIGHTS)	PL-A-4905-0-1	3
1	POWER SWITCH BRACKET	MA-C-169-0-[illegible]	2
1	INDICATOR PANEL (PARITY OPTION) TYPE 169	[illegible]	1

MAD-D-169-0-8 Indicator Panel (Parity Option) Type 169

digital

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

Printed in U.S.A.