INTERSIL

IM6102 Memory Extension/ DMA Controller/ Interval Timer (MEDIC)

FEATURES

- **Provides Extended Memory Address to 32K Words**
- **Simultaneous DMA — Provides Simultaneous DMA Channel that Uses DX Bus During Second Half of a Cycle to Access Memory**
- **DMA Channel Can be Used for Dynamic RAM Refresh**
- **12-Bit Programmable Interval Timer**
- **Direct Interface with IM6100 Microprocessor Via Bidirectional DX Bus and Handshake Lines**
- **Hardware Reset**
- **28 Different I/O Instructions**

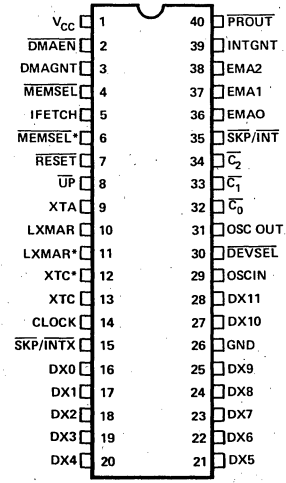
GENERAL DESCRIPTION

The IM6102 is a multi-function peripheral controller chip incorporating functions such as memory extension, direct memory access control, and a programmable real time clock.

The IM6102 provides necessary control to address up to 32K words of memory, and its DMA channel can be used with Dynamic RAM Components for "transparent refresh". The programmable real time clock is 12-bit long, and its output frequency can be programmed for 5 decades.

It features a high degree of system integration, putting into one chip all the functions which are normally available in three or more LSI circuits. As a result of this large integration, the user can design and produce a compact microcomputer with minicomputer performance.

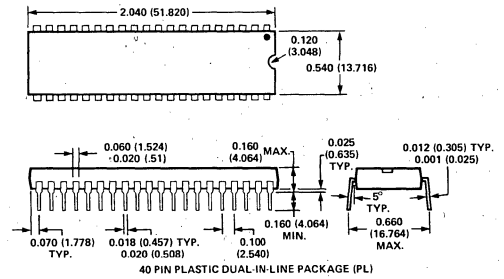
PIN CONFIGURATION



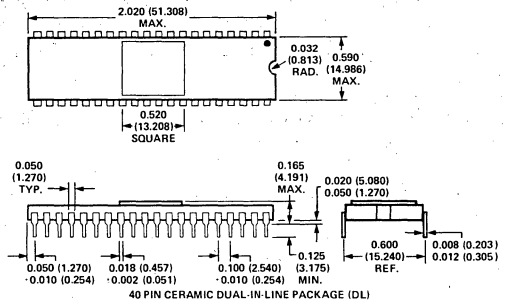
ORDERING INFORMATION

ORDER CODE	IM6102-1	IM6102A	IM6102
PLASTIC PKG.	IM6102-1IPL	IM6102-AIPL	IM6102-IPL
CERAMIC PKG	IM6102-1IDL	IM6102-AIDL	—
MILITARY TEMP.	IM6102-1MDL	IM6102-AMDL	—
MILITARY TEMP. WITH 883B	IM6102-1 MDL/883B	IM6102-AMDL/ 883B	—

PACKAGE DIMENSIONS

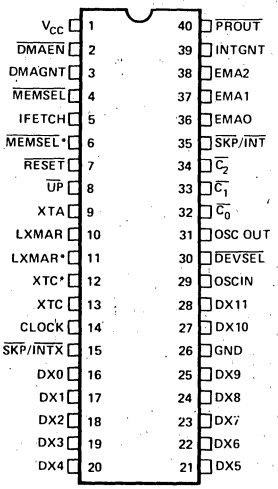


40 PIN PLASTIC DUAL-IN-LINE PACKAGE (PL)



40 PIN CERAMIC DUAL-IN-LINE PACKAGE (DL)

NOTE: DIMENSIONS IN PARENTHESIS ARE METRIC



IM6102 FUNCTIONAL PIN DESCRIPTION

Pin Number	Symbol	Input/ Output	Description
1	V_{CC}		Supply voltage
2	$\overline{DMAEN}$	I	Enable the IM6102 DMA channel to transfer data
3	DMAGNT	I	Direct memory access grant from CPU
4	$\overline{MEMSEL}$	I	Memory select for read or write from CPU
5	IFETCH	I	CPU flag indicating instruction fetch cycle
6	$\overline{MEMSEL}^*$	O	Memory select generated by the IM6102
7	$\overline{RESET}$	I	Asynchronous reset will clear Instruction Field to 0_8, disable all interrupts, initialize DMA port to READ/REFRESH, initialize timer to "stop", "divide by 2^{12} mode" and "enable divide counters"
8	$\overline{UP}$	O	User pulse (read or write)
9	XTA	I	CPU external minor cycle timing signal
10	LXMAR	I	A falling edge of LXMAR pulse from CPU will load external memory address register
11	LXMAR*	O	LXMAR generated by the IM6102
12	XTC*	O	XTC generated by the IM6102
13	XTC	I	CPU external minor cycle timing signal
14	CLOCK	I	Oscillator OUT pulses from CPU for timing the IM6102 DMA transfers.
15	$\overline{SKP}/\overline{INTX}$	I	Multiplexed SKP/INT line from lower priority devices
16	DX0	I/O	Most significant bit of the 12-bit multiplexed address and data I/O bus
17	DX1	I/O	See pin 16-DX0
18	DX2	I/O	See pin 16-DX0
19	DX3	I/O	See pin 16-DX0
20	DX4	I/O	See pin 16-DX0
21	DX5	I/O	See pin 16-DX0
22	DX6	I/O	See pin 16-DX0
23	DX7	I/O	See pin 16-DX0
24	DX8	I/O	See pin 16-DX0
25	DX9	I/O	See pin 16-DX0
26	GND	I/O	Power Supply
27	DX10	I/O	See pin 16-DX0
28	DX11	I/O	See pin 16-DX0
29	OSCIN	I	Crystal input for timer oscillator
30	$\overline{DEVSEL}$	I	Device select for read or write from CPU
31	OSC OUT	O	See pin 29
32	$\overline{C_0}$	O	Control lines to CPU determining type of peripheral data transfer
33	$\overline{C_1}$	O	See pin 32-C_0
34	$\overline{C_2}$	O	See pin 32-C_0
35	$\overline{SKP}/\overline{INT}$	O	Multiplexed SKP/INT input to the CPU
36	EMAO	O	Extended memory address field (most significant bit)
37	EMA1	O	Extended memory address field
38	EMA2	O	Extended memory address field
39	INTGNT	I	CPU interrupt grant
40	$\overline{PROUT}$	O	Priority out for vectored interrupt

NOTE: All DX lines are bidirectional with three-state outputs: Pins 6, 8, 11, 12, 35, 40 have active pullups; pins 32, 33, 34 have open drain outputs; pin 15 has a resistive input pullup; all inputs are protected with resistors and clamp diodes.

ARCHITECTURE

The IM6102 is composed of three distinct functions:

a) A DMA port that uses the bus during the second half of a cycle to read, write, or refresh memory. The DMA port logic includes a word count register WC, a current address register CA, an extended current address register ECA, and a DMA status register.

b) An extended memory address controller that augments the 12-bit addresses generated by the IM6100 microprocessor by supplying a 3-bit address field that may be decoded to select one of eight 4096 word memory fields. The memory extension controller logic consists of an instruction field register IF, a data field register DF, an instruction buffer register IB, and a save field register SF.

c) A realtime clock whose mode and time base rate may be programmed by the user. The clock logic includes a clock enable register CE, a clock buffer register CB, a clock counter register CC, and a time base multiplexer.

A block diagram of the IM6102 is shown in Figure 1.

The IM6102 registers are summarized as follows:

A. Simultaneous DMA Channel (Figure 3)

CURRENT ADDRESS (CA) REGISTER

This register is a 12-bit presettable binary counter. At the beginning of a SDMA transfer, the current address must be set to the first location to be accessed. The content of the CA register is incremented by 1 after a SDMA transfer, and the incremented value is used as the address of the memory location with which the next transfer will be performed.

EXTENDED CURRENT ADDRESS (ECA) REGISTER

This is a 3-bit presettable binary counter and if the carry enable bit of the DMA status register is set, the 12-bit CA register and the 3 ECA bits are treated as one 15-bit register with the ECA bits most significant. If memory field 7 (all 3 bits at logic one) is selected, the ECA cannot increment, but will wrap around in field 7 and an F7 error (F7E) will occur. The Interrupt Enable bit IE in SR11 must be set to enable F7E interrupts. If enabled the F7E will request an interrupt. If the carry enable bit CE in SR9 is not set, the ECA is not incremented when CA goes from 7777_8 to 0000_8.

WORD COUNT (WC) REGISTER

A 12-bit presettable binary counter is used as a word counter. At the beginning of a SDMA transfer, the two's complement of the number of 12-bit words to be transferred must be loaded into the WC. If enabled this will initiate the SDMA operation. The WC register is incremented by 1 after a SDMA transfer. If this value becomes zero, word count overflow has occurred and if the IE bit in SR11 is set, interrupts are enabled and an interrupt is requested. Unless instructed to be in the continuous run mode, a WC overflow inhibits further transfers. The WOF is set when the MSB of the WC register makes a "1" to "0" transition.

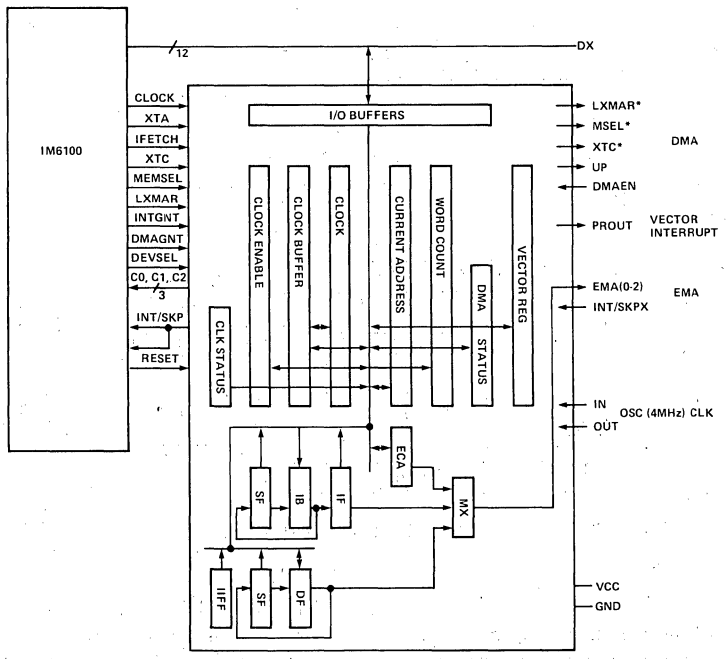


FIGURE 1: IM6102 MEMORY EXTENSION/DMA/INTERVAL TIMER CONTROLLER (MEDIC)

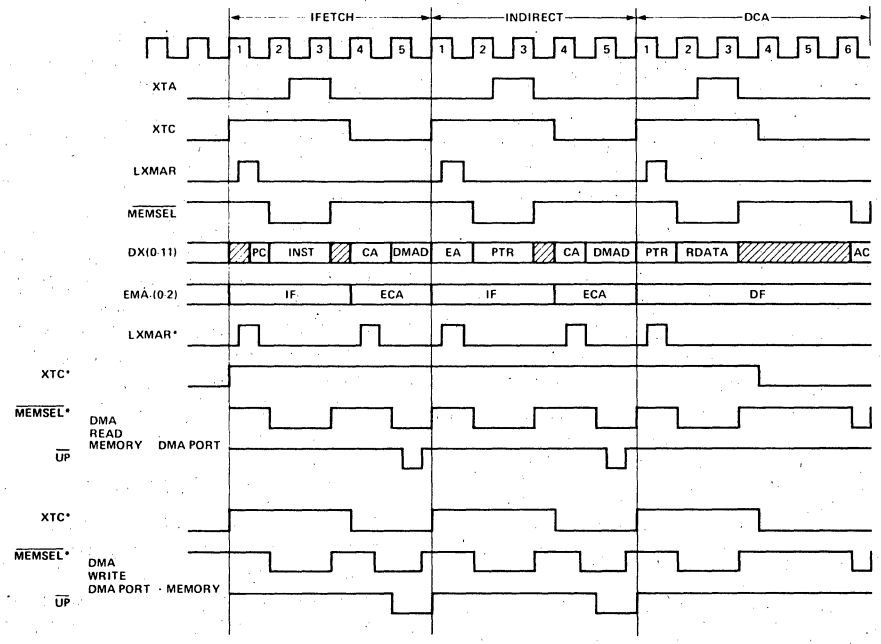


FIGURE 2: MEDIC TIMING FOR DCA I

DMA Status Register

This register consists of 5 control bits and 2 flag bits for the SDMA feature. For a description refer to the register bit assignments.

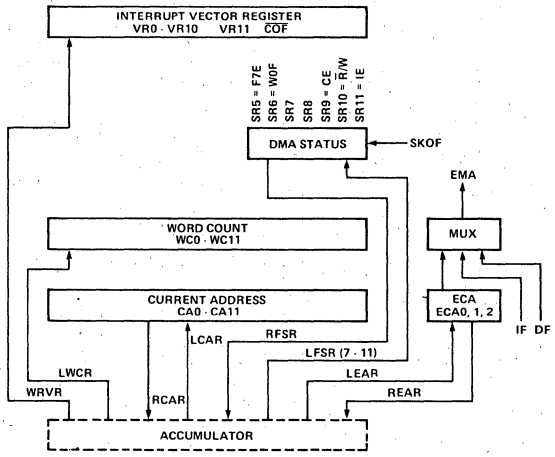


FIGURE 3: SDMA REGISTERS

OPERATION

The IM6102 SDMA channel augments the throughput of the IM6100 during DMA operations by transferring data between memory and peripheral devices simultaneously with normal processor bus usage. In other words, no memory cycles are "stolen" from the processor; but the DMA address and data are transferred on the bus during periods that the DX bus is inactive.

TABLE 3 SDMA INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
LCAR	6205_8	LOAD CURRENT ADDRESS REGISTER (CA) The contents of the AC replace the contents of the CA and the AC is cleared. DMA sequencing is stopped.
RCAR	6215_8	READ CURRENT ADDRESS REGISTER Description: Contents of CA transferred to AC.
LWCR	6225_8	LOAD WORD COUNT REGISTER (WC) Description: Contents of AC are transferred to the WORD COUNT REGISTER, the AC is cleared WORD COUNT OVERFLOW (WOF) is cleared and DMA operation started.
LEAR	$62N6_8$	LOAD IMMEDIATE TO EXTENDED CURRENT ADDRESS REGISTER (ECA) Description: Field N of the IOT instruction is transferred to the Extended current address register.
REAR	6235_8	READ EXTENDED CA Description: Extended current address register contents OR'd into bits 6, 7, 8, of AC.
LFSR	6245_8	LOAD DMA FLAGS and STATUS REGISTER Description: AC bits 7-11 are transferred to the DMA STATUS REGISTER and the AC is cleared.
RFSR	6255_8	READ DMA FLAGS and STATUS REGISTER Description: DMA Flags and Status Register bits are OR transferred into AC bits 5-11 and Field 7 wraparound error (F7E) is cleared.
SKOF	6265_8	SKIP ON OVERFLOW INTERRUPT Description: The PC is incremented by 1 if a word count register overflow interrupt condition is present causing next instruction to be skipped.
WRVR	6275_8	WRITE VECTOR REGISTER Description: AC bits 0-10 are transferred to the Vector Register and the AC is cleared.
CAF	6007_8	CLEAR ALL FLAGS–clears F7E and WOF (and also COF), Clock enable and clock buffer. The DMA process is initiated if the status register is not set to the "stop" mode.

TABLE 4 DMA FLAGS AND STATUS REGISTER BIT ASSIGNMENTS

0	1	2	3	4	5	6	7	8	9	10	11
*	*	*	*	*	F7E	WOF	SR7	SR8	CE	$\overline{R}$/W	IE

where* – don't care for write and zero for read.

F7E Field 7 wrap around carry error; cleared by CAF, RFSR and RESET

WOF Logic one indicates word counter overflow; clear by CAF, LWCR and RESET

CE Carry enable from CA(0-11) to ECA; cleared by RESET

$\overline{R}$/W Logic one indicates DMA write (Port to Memory transfer). Cleared (DMA Read) by RESET

IE Enable interrupt when WC overflows or Field 7 error occurs; cleared by RESET

SR7, 8
- 00 Refresh mode; WC is frozen, no UP, DMAEN is don't care
- 01 Normal mode; DMAEN(H) freezes WC CA and no UP if WC has not overflowed; stop if WC overflows
- 10 Burst mode; DMAEN(H) freezes WC, CA and no UP if WC has not overflowed; refresh condition if WC overflows
- 11 Stops DMA

DMA MODES

$SR_7 = SR_8 = 0$ REFRESH MODE

This is the mode to which the 6102 reverts on RESET. The word count register clock input is disabled, the user pulse (DMA data strobe) is suppressed and the DMAEN input is ignored. However, provided valid DMA transfer conditions are met in a particular memory cycle, the DMA sequencer will be started, appropriate timing signals will be generated and the current address register will be clocked. Thus DMA read accesses will be performed continually with an essentially free-running current address register. Read accesses will refresh dynamic memory. No WOF is possible but an F7E is possible if bit SR9 is set, enabling a carry from the current address register to the extended current address register.

$SR_7 = 0; SR_8 = 1$ NORMAL MODE

This mode is used for normal SDMA operations with static memory. The following instruction sequence can be used:

```
CLA      /Clear AC
TAD CA   /Get starting address
LCAR     /Load into current address register and
          clear AC
```

```
TAD SR   /Get DMA status Register Constant
LFSR     /Change status (from refresh to normal
         for example)
TAD WC   /Get two's complement of block length
LWCR     /Load word count register and start
         DMA TRANSFERS
```

Note that LWCR will start the sequencer so it should be the last instruction in the initialization sequence. The ECA register and vector register could also have been initialized in this sequence.

The SDMA sequencer samples DMAEN on the rising edge of every XTA and latches the condition of the enable line. If DMAEN is low, the sequencer is enabled, external timing signals XTC*, MSEL*, UP, LXMAR* are generated, the WC and CA registers are clocked. If DMAEN is high, at XTA (↑) time, the signal is sampled and latched and if the WC has not overflowed, the WC and CA registers are frozen, UP is suppressed. If the WOF condition comes up, the SDMA operation stops, regardless of DMAEN level.

The DMAEN and UP signals provide a simple interlocked handshaking method for transferring data one or more characters at a time (entire blocks) concurrently with processor operations on the bus. Of course, at all times, independent of DMAEN, the SDMA sequencer can proceed only if other bus usage conditions for DMA operations are met (not IOTA, IAUTOI, DCA, JMS, IJMS, ISZ, DMAGNT, or access of location X0000$_8$),

NOTE: IAUTOI is an indirect cycle of any autoindexed instruction; IJMS is indirect cycle of JMS. An autoindexed JMP* instruction may not be executed when the DMA mode is active.

$SR_7 = 1; SR_8 = 0$ BURST MODE

This mode is the same as the normal mode except when the word count register overflows. When this happens, the SDMA sequencer will set the WOF flag and revert to the refresh mode (ignoring DMAEN, freezing WC and suppressing UP). This mode is used when SDMA operations and dynamic memory refresh must be concurrently performed. The system designer must control the block lengths to be transferred, the refresh interval, and memory system design according to the application and performance desired.

$SR_7 = 1; SR_8 = 1$ STOP MODE

In this mode, no SDMA operations will take place. Naturally, cycle stealing DMA is still possible, and indeed may be used in any of the modes but the designer must be aware that cycle stealing may adversely affect dynamic memory refresh intervals. LWCR and LFSR may be executed in either order to change mode and start DMA.

B. Extended Memory Address Control

Figure 4 shows the EMA registers in more detail along with the register transfers caused by various instructions. The EMA function of the IM6102 is program compatible with the DEC PDP-8/E KM8-E Memory Extension option. The purpose of the EMA function is to extend the effective addressing space of the system from 4K to 32K words. To perform this function, the EXTENDED MEMORY CONTROLLER maintains a 3-bit extended address which is decoded by the memory modules to select 1 of 8 memory fields each containing 4096 words of storage. These 4K fields start with FIELD 0 and progress to FIELD 7 when 32K of memory is used. All software communication with the controller is via programmed IOT instructions for which a summary is included in Table 1.

Figure 4 shows two 3-bit field registers: the Instruction Field, which acts as an extension to the Instruction and directly obtained operand addresses and the Data Field, which augments indirectly obtained operand addresses. The program can, therefore, use one field for instructions and address pointers and another field for data. The selection between Instruction and Data Fields is signalled by the DATAF signal generated by the IM6100. A discussion of the various registers follows.

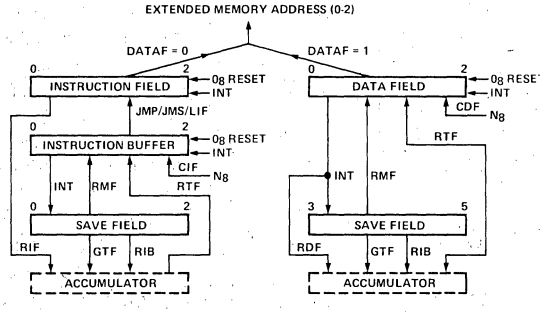


FIGURE 4: EMA REGISTERS

INSTRUCTION FIELD REGISTER (IF)

The IF is a 3-bit register that serves as an extension of the Program Counter (PC). The IF, however, is not incremented when the PC goes from 7777$_8$ to 0000$_8$. The contents of the IF determine the field from which all instructions are taken. Operands for all directly addressed memory reference instructions also come from the Instruction Field. The indirect pointer for all indirectly addressed memory reference instructions reside in the Instruction Field. The IF is cleared to 0$_8$ and the IM6100 Program Counter is set to 7777$_8$ by RESET.

DATA FIELD REGISTER (DF)

The DF is a 3-bit register which determines the memory field from which operands are fetched in indirectly addressed AND, TAD, ISZ or DCA instructions. However, the branch address for indirectly addressed JMS or JMP instructions is obtained from the Instruction Field. The Data Field register may be modified under program control. The DF is set to O_8, on reset.

INSTRUCTION BUFFER REGISTER (IB)

The IB is a 3-bit register which serves as an input buffer for the Instruction Field (IF) register. All programmed modifications of the IF register are made through the IB

register. The transfer from IB to IF takes place at the beginning of the execute phase of the "next" JMP or JMS instruction or immediately upon execution of an LIF instruction. Using this feature, a program segment can execute an instruction to modify the IF and then "exit" the program segment before the actual modification of the IF takes place. If instructions could change the IF directly, it would be impossible to execute the "next" sequential instruction, followed by a Change IF instruction. The IB to IF transfer is inhibited if the JMP/JMS instruction is fetched from control panel memory, which is restricted to 4K, but the LIF instruction is used here to provide the ability to load the IF register from the IB register. This allows the control panel routines to be executed transparently while the IB and IF differ and also yields a method for the panel to extract or alter the status of the primary EMA registers. The IB is set to 0_8, on reset. The IB to IF transfer takes place during the second cycle of a JMP/JMS instruction when XTC makes a falling (↓) transition.

SAVE FIELD REGISTER (SF)

The SF is a 6-bit register in which the IB and DF registers are saved during an Interrupt Grant. When an Interrupt occurs, the contents of IB and DF are automatically stored in SF (0-2) and SF (3-5), respectively, and the IF, IB and DF registers are cleared. The INTGNT (Interrupt Grant) cycle stores the "current" Program Counter (PC) in location 0000_8 of Memory Field 0_8 and the CPU resumes operation in location 0001_8 of Memory Field 0_8. The Instruction Field and Data Field of the program segment being executed by the CPU before the interrupt was acknowledged are available in the SF register.

INTERRUPT INHIBIT FLIP-FLOP

The INTREQ (Interrupt Request) line to the IM6100 must be "gated" by the Interrupt Inhibit Flip-Flop so that, when the Instruction Field is changed under program control, all interrupts are disabled until a JMP or JMS instruction is executed. Since the actual modification of the Instruction Field takes place only after the "next" JMP/JMS, this inhibition of the INTREQ's ensures that the program sequence resumes operation in the "new" memory field before an Interrupt Request is granted.

Since Interrupt Requests are asynchronous in nature, a situation may arise in which an INTREQ is generated when the IF and IB bits are different. The Interrupt Inhibit FF guarantees the structural integrity of the program segment. The IIF is cleared on reset.

TABLE 5 EMA INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
GTF	6004_8	GET FLAGS Operation: AC (0) ← LINK AC (2) ← INTREQ Line AC (3) ← INT INHIBIT FF AC (4) ← INT ENABLE FF AC (6-11) ← SF (0-5) Description: LINK, INTREQ and INT ENABLE FF are internal to the CPU. The INT INHIBIT FF and SF are in the MEDIC.
RTF	6005_8	RETURN FLAGS Operation: LINK ← AC (0) IB ← AC (6-8) DF ← AC (9-11) Description: LINK is restored. All AC bits are available externally during IOTA T6 to restore other flag bits. The internal Interrupt System is enabled. However, the Interrupt Inhibit FF is made active until the "next" JMS/JMP/LIF. The IB is transferred to IF after the "next" JMS/JMP/LIF.
CDF	$62N1_8$	CHANGE DATA FIELD Operation: DF ← N_8 Description: Change DF register to N (0_8-7_8).

TABLE 5, Continued

MNEMONIC	OCTAL CODE	OPERATION
CIF	$62N2_8$	CHANGE INSTRUCTION FIELD Operation: IB ← N_8 Description: Change IB to N (0_8-7_8). Transfer IB to IF after the "next" JMP/JMS/LIF. The Interrupt Inhibit FF is active until the "next" JMP/JMS/LIF.
CDF, CIF	$62N3_8$	CHANGE DF, IF Operation: DF ← N_8 IB ← N_8 Description: Combination of CDF and CIF.
RDF	6214_8	READ DATA FIELD Operation: AC (6-8) ← AC (6-8) + DF Description: OR's the contents of DF into bits 6-8 of the AC. All other bits are unaffected.
RIF	6224_8	READ INSTRUCTION FIELD Operation: AC (6-8) ← AC (6-8) + IF Description: OR's the contents of IF into bits 6-8 of the AC. All other bits of the AC are unaffected.
RIB	6234_8	READ INTERRUPT BUFFER READ SAVE FIELD Operation: AC (6-11) ← AC (6-11) + SF Description: OR's the contents of SF into bits 6-11 of the AC. All other bits are unaffected.
RMF	6244_8	RESTORE MEMORY FIELD Operation: IB ← SF (0-2) DF ← SF (3-5) Description: The SF register saves the contents of the IB and DF when an interrupt occurs. This command is used to restore IB and DF when "exiting" from the interrupt service routine in another field. Transfer IB to IF after the next JMP/JMS/LIF. The Interrupt Inhibit Flip-Flop is active until the next JMP/JMS/LIF.
LIF	6254_8	LOAD INSTRUCTION FIELD Operation: IF ← IB Description: Transfer IB to IF and clear the Interrupt Inhibit FF

+: "OR"
●: "AND"
←: "IS REPLACED BY"

OPERAND FETCHING

Instructions are accessed from the currently assigned Instruction Field. For indirect AND, TAD, ISZ or DCA instructions, the operand address refers first to the Instruction Field to obtain an Effective Address which in turn refers to a location in the currently addressed Data Field. All instructions and operands are obtained from the field designated by the IF, except for indirectly addressed operands, which are specified by the DF.

Thus, DF is active only in the Execute phase of an AND, TAD, ISZ or DCA when it is directly preceded by an Indirect phase.

ADDRESS MODE	IF	DF	AND, TAD, ISZ or DCA
Direct	m	n	Operand in field m
Indirect	m	n	Absolute address of operand in field m; operand in field n

Each field of extended memory contains eight auto-index registers in addresses 10 through 17. For example, assume that a program in field 2 is running (IF = 2) and using operands in field 1 (DF = 1) when the instruction TAD I 10 is fetched. The indirect autoindex cycle is entered, and the contents of location 10 in field 2 are read, incremented, and rewritten. If address 10 in field 2 originally contained 0546, it now contains 0547. In the execute cycle, the operand is fetched from location 0547 of field 1.

Program control is transferred between memory fields by the CIF instruction. The instruction does not change the instruction field directly, as this would make it impossible to execute the next sequential instruction; instead, it loads the new instruction field in the IB for automatic transfer into the IF when either a JMP or JMS instruction is executed. The DF is unaffected by the JMP and JMS instructions.

The 12-bit program counter is set in the normal manner and, because the IF is an extension on the most significant end of the PC, the program sequence resumes in the new memory field following a JMP or JMS. Entry into a program interrupt is inhibited after the CIF instruction until a JMP or JMS is executed.

NOTE: The IF is not incremented if the PC goes from 7777_8 to 0000_8. This feature protects the user from accidentally entering a nonexistent field.

To call a subroutine that is out of the current field, the data field register is set to indicate the field of the calling JMS, which establishes the location of the operands as well as the identity of the return field. The instruction field is set to the field of the starting address of the subroutine. The following sequence returns program control to the main program from a subroutine that is out of the current field.

```
/PROGRAM OPERATIONS IN MEMORY FIELD 2
/INSTRUCTION FIELD = 2; DATA FIELD = 2
/CALL A SUBROUTINE IN MEMORY FIELD 1
/INDICATE CALLING FIELD LOCATION BY THE
/CONTENTS OF THE DATA FIELD
        CIF  10         /CHANGE TO INSTRUCTION
                        /FIELD 1 = 6212
        JMS I SUBRP     /SUBRP = ENTRY ADDRESS
        CDF  20         /RESTORE DATA FIELD
         .
         .
         .
SUBRP,  SUBR            /POINTER
```

FIELD 2
FIELD 1

```
                        /CALLED SUBROUTINE,
                        /LOCATION IN FIELD 1
SUBR,   0               /RETURN ADDRESS
                        /STORED HERE
        CLA
        RDF             /READ DATA FIELD INTO AC
        TAD RETURN      /CONTENTS OF THE AC =
                        /6202 + DATA FIELD BITS
        DCA EXIT        /STORE CIF N INSTRUCTION
         .              /NOW CHANGE DATA FIELD
         .              /IF DESIRED
         .
EXIT,   0               /A CIF INSTRUCTION
        JMP I SUBR      /RETURN TO CALLING
                        /PROGRAM
RETURN, CIF             /USED TO FORM CIF N
                        /INSTRUCTION
```

When a program interrupt occurs, the current instruction and data field numbers are automatically stored in the 6-bit save field register, then the IF and DF are cleared. The 12-bit program counter is stored in location 0000_8 of field 0_8 and program control advances to location 0001_8 of field 0_8. At the end of the program interrupt subroutine, the RMF instruction restores the IF and DF from the contents of the SF. Alternatively, the GTF and RTF instructions may be used to handle the Save Field and Link information. The following instruction sequence at the end of the program interrupt subroutine continues the interrupted program after the interrupt has been processed:

```
         .
         .
         .
         .
        CLA
        TAD AC          /RESTORE AC
        RMF             /LOAD IB AND DF FROM SF
        ION             /TURN ON INTERRUPT
                        /SYSTEM
        JMP I 0         /RESTORE PC WITH
                        /CONTENTS OF LOCATION
                        /0000₈ AND LOAD
                        /IF FROM IB
```

IM6100 control panel memory programs, if used must be careful in the manner that EMA register data is manipulated. Control panel interrupt requests bypass the device interrupt enable flip flop, and indeed, are granted even by a halted CPU. The interrupts from a control panel may occur at any time, and in particular when the IB and IF registers do not contain the same data. The EMA logic inhibits IB to IF transfers in control panel memory so that panel routines may execute transparently (in particular, JMP/JMS instructions). The panel routines may alter the IF by executing the LIF instruction.

Users should also note that the GTF and RIB instructions read the SF register, and only the RIF instruction reads the IF register. Note also that the SF saves the IB register rather than the IF during an interrupt. However, interrupts are inhibited until the IF and IB registers are the same.

The memory extension controller that we have discussed in this section shows three important design considerations involved in extending memory addressing space. The first is the concept of having separate instruction and data fields for program flexibility. The second is the importance of double buffering the instruction field register to maintain structural integrity of programs and the third is the provision for saving the current field status upon interrupts and disabling interrupts until a change of instruction field has been completely executed.

C. Programmable Real Time Clock

The programmable real time clock offers the 6100 user a number of ways to accurately measure and count intervals in order to implement real time data acquisition and data processing systems.

The crystal used should have the following characteristics:

$R_S \leqslant 150$ ohms

C_M = 3-30 mpF (10^{-15}F)

C_O = 10-50 pF

Static capacitance should be around 5pF; for the greatest stability, C_O should be around 12pF and the oscillator is parallel resonant.

TABLE 6 CLOCK ENABLE REGISTER BIT ASSIGNMENTS

0	1	2	3	4	5	6	7	8	9	10	11
EN0	*	EN2	EN3	EN4	EN5	*	EN7	*	*	*	*

* Don't care for write and zero for read.

Where EN0 – When set to 1, enables clock overflow (COF flag) to cause an interrupt. Cleared by RESET, CAF.

EN2 – When reset to a 0-counter runs at selected rate. Overflow occurs every 4096 (2^{12}) counts.COF flag remains set until cleared by IOT 6135 (CLSA), CAF, RESET.

When set to a 1-counter runs at selected rate. If the COF flag is cleared, overflow causes clock buffer to be transferred to the clock counter which continues to run. COF flag remains set until cleared with IOT 6135 (CLSA). Also cleared by RESET, CAF.

EN3, 4, 5 – Assuming 2 MHz crystal oscillator cleared by RESET, CAF.

Bits 3,4,5	Octal	Interval Between Pulses	Frequency
000	0	Stop	0
001	1	Stop	0
010	2	20 msec	50 Hz
011	3	2 msec	500 Hz
100	4	200 μsec	5 KHz
101	5	20 μsec	50 KHz
110	6	2 μsec	500 KHz
111	7	Stop	0

EN7 – Inhibits clock prescaler when set to 1 cleared by RESET, CAF. EN3-5 and EN7 should not be changed simultaneously.

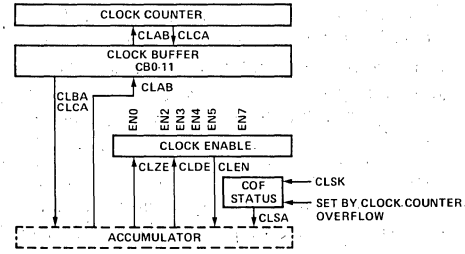


FIGURE 5 RTC REGISTERS

A discussion of the Real Time Clock registers as shown in Fig. 5 follows:

CLOCK ENABLE REGISTER

This register controls the mode of counting, whether clock interrupts are allowed, and the rate of the time base of the clock. For a description refer to the register bit assignments.

CLOCK BUFFER REGISTER (CB)

This 12-bit register stores data being transferred from the AC to the clock counter, or from the clock counter to the AC. It also permits presetting of the clock counter.

CLOCK COUNTER REGISTER (CC)

This register is a 12-bit binary counter that may load the clock buffer or be loaded from it. It is driven by a 2 MHz crystal oscillator with the proper predivision set by the time base selection. When an overflow occurs and if bit 0 of the clock enable register is a logic one, an interrupt is requested. If bit 2 is also 1, overflow causes the clock buffer to be transferred automatically into the clock counter.

TIME BASE MULTIPLEXER

The multiplexer provides count pulses to the clock counter according to the rate set by the clock enable register. Use of other than a 2 MHz crystal for the clock will result in proportionately different time bases.

CLOCK OVERFLOW FLAG

This flag is set by a clock counter overflow. It is cleared by CAF, CLSA and RESET. Its complement provides LSB (VR11) of interrupt vector. If ENO of clock enable counter is set, COF can cause an interrupt request. The COF is set when the MSB of the counter makes a "1" to "0" transition.

TABLE 7 RTC INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
CLZE	6130_8	CLEAR ENABLE REGISTER PER AC Description: Clears the bits in the clock enable register corresponding to those bits set in the AC. The AC is not changed.
CLSK	6131_8	SKIP ON CLOCK INTERRUPT Description: Causes the program counter to be incremented by one if clock interrupt conditions exists, so that the next sequential instruction is skipped.
CLOE	6132_8	SET ENABLE REGISTER PER AC Description: Sets the bits in the clock enable register corresponding to those bits set in the AC. The AC is not changed.
CLAB	6133_8	TRANSFER AC TO CLOCK BUFFER Description: Causes the contents of the AC to be transferred to the Clock Buffer, then causes the contents of the Clock Buffer to be transferred to the Clock Counter. The AC is not changed.
CLEN	6134_8	READ CLOCK STATUS Description: Interrogates the clock overflow status flip flop by clearing AC, then transferring clock status into AC bit 0. COF is cleared.
CLSA	6135_8	READ CLOCK STATUS Description: Interrogates the clock overflow status flip flop by clearing AC, then transferring clock status into AC bit 0. COF is cleared.
CLBA	6136_8	READ CLOCK BUFFER Description: Clears the AC, then transfers the contents of the Clock Buffer into the AC.
CLCA	6137_8	READ CLOCK COUNTER Description: Clears the AC, transfers the contents of the Clock Counter to the Clock Buffer, then transfers the contents of the Clock Buffer into the AC. If EN7 is set to 1 (clock prescaler is inhibited), the CLCA instruction increments the prescaler input by one. If the clock is in the "stop" mode but EN7 is not inhibited, the prescaler will not be clocked by the CLCA instruction.
CAF	6007_8	CLEAR ALL FLAGS Description: Clears COF flag (and also F7E, WOF flags), clock enable and clock buffer registers.

SYSTEM CONSIDERATIONS

The IM6102 is the highest priority device in a priority interrupt scheme. It provides an active low signal on pin 40, POUT, to signal the next lower priority device in the chain (thus, a high level on POUT indicates that the 6102 is not requesting an interrupt) via its "priority-in", PRIN, input.

The IM6102 when requesting an interrupt activates the SKP/INT line low on pin 35 and the POUT line low on pin 40 if its interrupt inhibit flip-flop is not set.

The IOT instructions used by the IM6102 preclude the use of certain device addresses when the system uses IM6101 PIEs. The addresses that may not be used are those given by bits 3 through 7 of the IOT instructions that are used with the IM6102. These addresses are 00101, 01000, 01001, 01010, 01011 corresponding to IOT instructions 612X, 613X, 620X, 621X, 622X, 623X, 624X, 625X, 626X and 627X.

The IM6102 does not generate DMAREQ signals to the 6100 because of its simultaneous use of the DX bus. It monitors the DMAGNT signal in order to place the EMA 0, 1, 2 lines on pins 36, 37, 38 in a high impedance state while DMAGNT is high.

If the application requires other peripherals requiring direct memory access on a cycle stealing basis, for example, bus contention problems will be resolved by the IM6102 as it monitors the DMAGNT line and gets off the bus (by placing all lines in the high impedance state) when DMAGNT is active.

If interrupts are enabled and a request is pending, during the first INTGNT cycle, the IM6102 will detect the referencing of location 0000_8 by the IM6100 in order to save the PC and will suspend simultaneous DMA during that cycle. The logic will in fact suspend simultaneous DMA in any cycle that location 0000_8 is referenced, either in main memory or control panel memory.

This makes it possible to disable automatic interrupt vectoring by grounding the INTGNT line to the IM6102. This will not affect the generation of INTREQ so the IM6100 will have to poll peripheral devices (skip on flag instructions) to determine the interrupting source.

Grounding INTGNT is not possible in extended memory applications since the INTGNT signal is used to save the Instruction Buffer and Data Field Register and clear the IF, IB and DF registers. (All peripheral device interrupt service routines have their entry point at location 0001_8 of Memory Field 0_8).

If no interrupt requests are pending in the 6102 (COF, F7E or WOF) from the DMA or RTC functions, the IM6102 interrupt request flip-flop is clear and POUT, the priority out signal, is high, enabling interrupt requests downstream in the priority chain. In the event that interrupts are enabled (DMA status bit SR11 is set and/or clock enable bit ENO is set) and an interrupting condition occurs (F7E, WOF, COF), the POUT signal goes low asynchronously disabling interrupt vectors downstream.

If the Interrupt Inhibit Flip-Flop is not set, the SKP/INT line is driven low by the interrupt request. If the IIFF is set, the SKP/INT line stays high until the IIFF is cleared (by RESET or an IB to IF transfer) at which time SKP/INT may be driven low. Skip requests will always propagate independently of IIFF during IOTA •$\overline{\text{DEVSEL}}$• XTC.

Interrupt requests from devices downstream of the IM6102 must also be channeled via the IM6102 in order that the IIFF may condition the request timing. The IM6102 provides a built in pull-up on the SKP/INTX line coming in from devices downstream in the priority chain. At 5v, the pull-up looks like a 10K resistor; at 10V, it looks like 5K.

The execution of any IOT instruction will reset INTGNT to a low level at the end of IOTA time. This IOT instruction will be the first instruction in the interrupt service routine after saving status. If hardware vectoring is being used, any IOT instruction when INTGNT is high will cause the IM6102 to place a vector address on the bus if it requested an interrupt and pull the C1 and C2 lines low, thus placing the vector in PC and forcing a branch to the service routine. If the C2 line is left unconnected, the vector address will not be forced into the PC, but will be OR'ed into the AC. The interrupt service routine would have to execute a CLA after its first IOT instruction in order to clear the AC. Note that the LSB of the vector address is determined by the complement of the COF flag and that a DMA interrupt service routine must distinguish between the two possible interrupting conditions, a word count overflow or a field 7 wrap-around error. The programmer may read the DMA status register with an RFSR instruction and also test the WOF flag with a skip instruction, SKOF. The COF flag may also be tested with the CLSK skip instruction. The flag may be read (and cleared) with the CLSA instruction. The skip instructions cause the SKP/INT line to go low during IOTA • XTC time if the flag being tested is set. At all other times, the SKP/INT line carries interrupt requests as modified by the IM6102 interrupt inhibit logic. The flags must always be explicitly cleared by the interrupt service routine.

The DMA transfer rate depends on the program. The minimum rate would be obtained if the processor was executing an autoindexed DCA or an indirect JMS (even if non-autoindexed, DMA is suppressed during indirect phase of JMS). Continuously executing these instructions would cause DMA transfers to occur only every third memory cycle (IFETCH). The maximum rate could be obtained by executing a JMP• loop (JMP to itself); data would be transferred on every cycle and the interrupt routine entered when word count overflows could bump the return address out of the loop.

In dynamic memory systems it should be noted that the MEMSEL* signal narrows when the mode changes from write to refresh (burst mode). RESET signals may need to be limited in duration to prevent loss of memory data in dynamic memory systems.

The accuracy of the clock counter in the programmable real time clock section of the IM6102 is as follows:

CASE 1: Counter running; CC loaded from AC via CB using instruction CLAB (IOT 6133) accuracy is 0 to +1 count.

CASE 2: CC loaded from CB automatically on overflow; the accuracy of counting is then only dependent on accuracy of oscillator.

IM6102 users who do not need all the capabilities of the device may improve systems performance by not using some of the features. To do this properly, certain pins on the device will become unused. The following table summarizes what may be done with certain pins when using only part of the IM6102 functions. All unlisted pins must be used when implementing any of the three basic features.

PIN NUMBER	PIN NAME	RTC ONLY	SDMA ONLY	EMC ONLY	EMC & DYNAMIC REFRESH
2	DMAEN	GND	USED	GND	GND
3	DMAGNT	USED	USED	USED	USED
6	MEMSEL*	N/C	USED	N/C	USED
8	UP	N/C	USED	N/C	N/C
11	LXMAR*	N/C	USED	N/C	USED
12	XTC*	N/C	USED	N/C	USED
15	SKP/INTX	VCC	VCC	USED	USED
29	OSCIN	USED	GND	GND	GND
31	OSC OUT	USED	N/C	N/C	N/C
34	C2	USED	USED	N/C	N/C
36	EMAO	N/C	N/C	USED	USED
37	EMA 1	N/C	N/C	USED	USED
38	EMA 2	N/C	N/C	USED	USED
40	PROUT	USED	USED	N/C	N/C

TABLE 1 SUMMARY OF IM6102 INSTRUCTIONS

MNEMONIC	OCTAL CODE	I/O CONTROL LINES			OPERATION
		C0	C1	C2	
GTF	6004	0	0	1	① Get flags, INT INH FF → AC(3), SF (0-5) → AC(6-11)
RTF	6005	1	1	1	② Return flags, AC(6-8) → IB, AC(9-11) → DF
CDF	62N1	1	1	1	Change Data Field, N → DF
CIF	62N2	1	1	1	Change IF, N → IB
CDF, CIF	62N3	1	1	1	Combination of CDF, CIF
RDF	6214	1	0	1	Read DF, DF + AC(6-8) → AC(6-8)
RIF	6224	1	0	1	Read IF, IF + AC(6-8) →AC(6-8)
RIB	6234	1	0	1	Read Save Field, SF + AC(6-11) → AC(6-11)
RMF	6244	1	1	1	Restore Mem. Field, SF(0-2) →IB, SF(3-5) → DF
LIF	6254	1	1	1	Load IF, IB → IF
CLZE	6130	1	1	1	Clear Clock Enable Register if corresponding AC bit is set AC not changed
CLSK	6131	1	1	1	Skip on Clock Overflow Interrupt condition
CLOE	6132	1	1	1	Set Clock Enable Register if corresponding AC bit is set AC not changed
CLAB	6133	1	1	1	AC → Clock Buffer; Clock Buffer → Clock Counter; AC not changed
CLEN	6134	0	0	1	Clock Enable Register → AC
CLSA	6135	0	0	1	COF → AC(0), Clear COF Status bit
CLBA	6136	0	0	1	Clock Buffer → AC
CLCA	6137	0	0	1	Clock Counter → Clock Buffer; Clock Buffer → AC
LCAR	6205	0	1	1	AC → Current Address Register, 0 → AC
RCAR	6215	0	0	1	Current Address Register → AC
LWCR	6225	0	1	1	AC → Word Count Register, Start DMA, 0 → AC; clears word count overflow (WOF)
LEAR	62N6	1	1	1	N → Extended Current Address Register (ECA)
REAR	6235	1	0	1	Read ECA, ECA + AC(6-8) → AC(6-8)
LFSR	6245	0	1	1	AC(7-11) → Status Register, 0 → AC
RFSR	6255	1	0	1	DMA Status Register + AC(5-11) → AC(5-11); clears Field 7 Wraparound error (F7E)
SKOF	6265	1	1	1	Skip on Word Count Overflow
WRVR	6275	0	1	1	AC(0-10) → Vector Register, 0 → AC
CAF	6007	1	1	1	③ Clear all flags (F7E, W0F, COF) Clear clock Enable register, clock buffer

NOTES:

1. The internal flags of the IM6100 are defined as follows: LINK → AC (0), INTREQ → AC (2) and INTERRUPT ENABLE FF → AC (4).
2. When RTF is executed, the LINK is restored from AC (0) and the Interrupt System is enabled after the next sequential instruction is executed. The Interrupt Inhibit FF is set preventing interrupts until the next JMP, JMS or LIF instruction is executed.
3. A hardware RESET clears F7E, W0F, 11FF and COF. The IF and DF are cleared to 0_8. The DMA status register is cleared. (Read; refresh; disable F7E and W0F interrupts; no carry from CA0 to ECA2). The clock Enable register is cleared (Disable COF interrupt; disable clock buffer to clock counter transfer on COF; disable counter). Counter/buffer is cleared.

TABLE 2 SUMMARY OF IM6102 REGISTER BIT ASSIGNMENTS

	DX0	DX1	DX2	DX3	DX4	DX5	DX6	DX7	DX8	DX9	DX10	DX11
Current Address	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11
Extended Current Address							ECA0	ECA1	ECA2			
Word Count	WC0	WC1	WC2	WC3	WC4	WC5	WC6	WC7	WC8	WC9	WC10	WC11
DMA Status (1)						SR5	SR6	SR7	SR8	SR9	SR10	SR11
Interrupt Vector (2)	VR0	VR1	VR2	VR3	VR4	VR5	VR6	VR7	VR8	VR9	VR10	VR11
RIF Instruction (3)							IF0	IF1	IF2			
RTF, CIF Instruction							IB0	IB1	IB2			
GTF, RIB Instruction				IIFF(4)			SF0	SF1	SF2	SF3	SF4	SF5
CDF, RDF Instruction							DF0	DF1	DF2			
RTF Instruction										DF0	DF1	DF2
Clock Enable (5)	EN0		EN2	EN3	EN4	EN5		EN7				
Clock Buffer	CB0	CB1	CB2	CB3	CB4	CB5	CB6	CB7	CB8	CB9	CB10	CB11
Clock Overflow (6)	COF											

(1) DMA STATUS

SR5 Set if Field 7 wraparound carry error — F7E; cleared by CAF, RFSR (at IOTA · $\overline{XTC}$ time), RESET } READ ONLY BITS

SR6 Set if DMA Word Counter Overflow — W0F; cleared by CAF, LWCR, RESET } READ ONLY BITS

SR7 Mode Bit 7 } ; Cleared by RESET (REFRESH MODE)

SR8 Mode Bit 8 } See below

SR9 Carry enable from CA0-11 to ECA2 if set — CE

SR10 DMA Write if set

SR11 Enable F7E or W0F interrupt if set — IE

(2) VR0-VR10 loaded from AC. VR11 is equivalent to $\overline{COF}$

(3) IF — Instruction Field; cleared to 0_8 by RESET AND INTGNT

(4) IIFF — Interrupt Inhibit Flip-Flop; set whenever IB ≠ IF; (CIF, CDF/CIF, RMF, RTF) cleared by RESET and IB → IF transfer

(5) EN0 — Enable Clock Overflow (COF) interrupt; cleared (interrupt disable) by RESET, CAF

EN2 — When set causes clock buffer to be transferred to clock counter on COF.
Counter runs at selected rate; COF remains set until cleared with CLSA.
When cleared to 0, counter runs at selected rate, overflow occurs every 2^{12} counts and COF remains set. EN2 is cleared by RESET, CAF

EN3, EN4, EN5 — Select interval between pulses. Cleared to 000 by RESET (counter disabled), CAF See below.

EN7 — Inhibits clock prescaler when set. Cleared by RESET, CAF

(6) COF — Clock Overflow status bit; cleared by CAF, RESET and CLSA; complement provides LSB of interrupt vector.

SR 7, 8	00	Refresh mode; WC is frozen, no UP, DMAEN don't care
	01	Normal mode; DMAEN(H) freezes WC, CA and no UP if WC has not overflowed; stop if WC overflows
	10	Burst mode; DMAEN (H) freezes WC, CA and no UP if WC has not overflowed; reverts to refresh mode if WC overflows.
	11	Stops SDMA

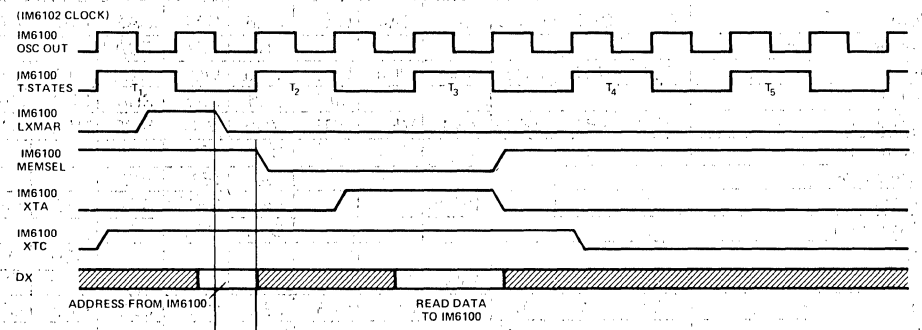
EN 3, 4,5	with	2 MHz clock
000		STOP
001		STOP
010		20 ms interval
011		2 ms interval
100		200 μs interval
101		20 μs interval
110		2 μs interval
111		STOP

NOTES:

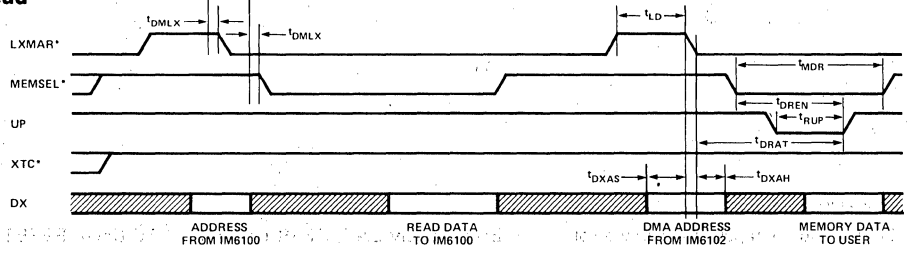
1. Bits SR 7 and 8 do not change when the DMA controller stops or reverts to refresh mode as a result of WC overflow.
2. The "overflow" status is defined as set when the most significant bit of a counter makes a "1" to "0" transition.

SDMA OPERATIONS TIMING

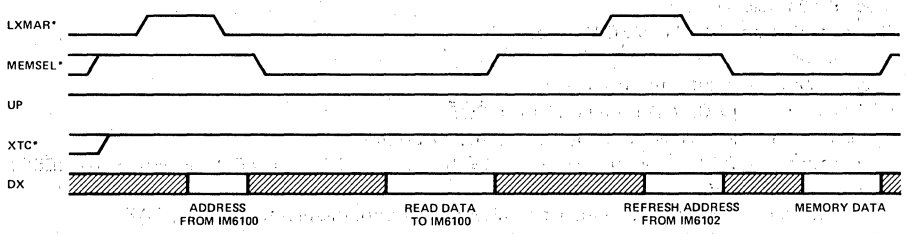
A. IM6100 Signals



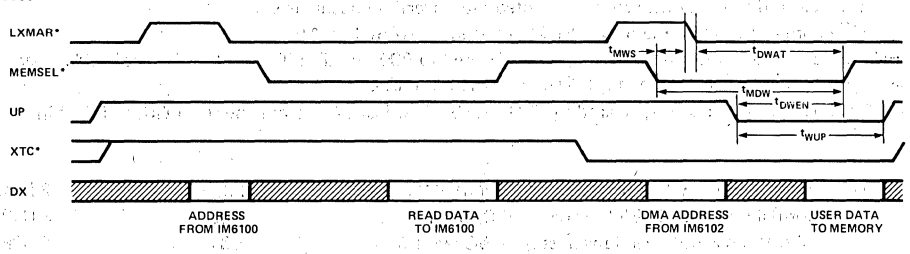
B. DMA Read



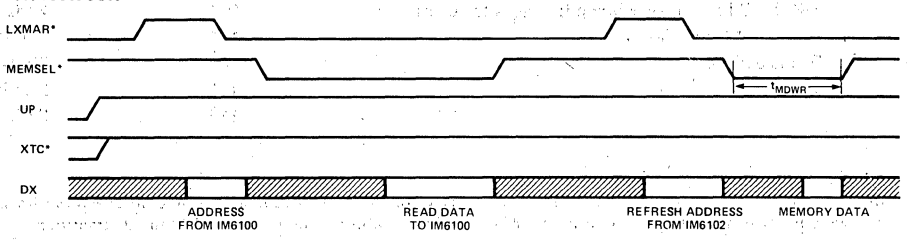
C. DMA Read/Refresh



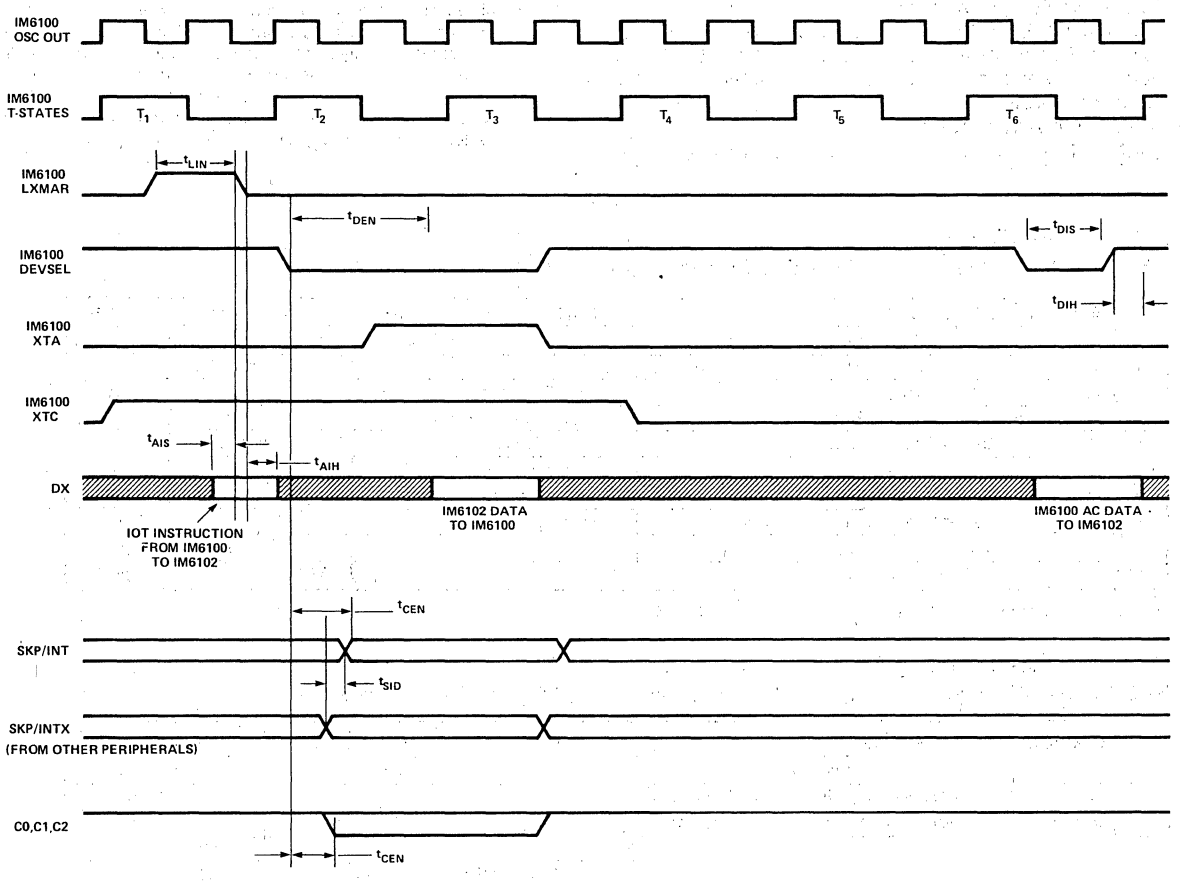
D. DMA Write



E. DMA Write/Refresh



TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6102A ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... +4.0V to +11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	µA
4	V_{OH}	Output Voltage High[2]	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OL}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	µA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}			900	µA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 5.71MHz			4.0	mA
9	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
10	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, C_L = 50pF, T_A = -40°C to +85°C, f_C = 5.71MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{LIN}	LXMAR Pulse Width IN	125			ns
2	t_{AIS}	Address Setup Time IN: DX-LXMAR (↓)	50			ns
3	t_{AIH}	Address Hold Time IN: LXMAR(↓)-DX	50			ns
4	t_{DEN}	Data Output Enable Time: DEVSEL(↓)-DX			240	ns
5	t_{CEN}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			240	ns
6	t_{DIS}	Data Input Setup Time: DX-DEVSEL(↑)	50			ns
7	T_{DIH}	Data Input Hold Time: DEVSEL(↑)-DX	50			ns
8	t_{RST}	RESET Input Pulse Width	250			ns
9	t_{SID}	SKP/INTX to SKP/INT Propagation Delay			100	ns
10	t_{DMLX}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			100	ns
11	t_{DEM}	Enable/Disable Time from DMAGNT to EMA Lines			50	ns
12	t_{MDR}	MEMSEL* Pulse Width READ	300			ns
13	t_{MDW}	MEMSEL* Pulse Width WRITE	380			ns
14	t_{MDWR}	MEMSEL* Pulse Width WRITE/REFSH	240			ns
15	t_{LD}	LXMAR* Pulse Width	150			ns
16	t_{DRAT}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	300			ns
17	t_{DXAS}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	150			ns
18	t_{DXAH}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	55			ns
19	t_{DREN}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	210			ns
20	t_{RUP}	UP Pulse Width DMA READ	150			ns
21	t_{DWAT}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	300			ns
22	t_{DWEN}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	210			ns
23	t_{MWS}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	50			ns
24	t_{DMS}	DMAEN Setup Time Wrt XTA (↑)	50			ns
25	t_{DMH}	DMAEN Hold Time Wrt XTA (↑)	50			ns
26	t_{WUP}	UP Pulse Width DMA WRITE	300			ns

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6102-1I ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... +4.0V to +7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	µA
4	V_{OH}	Output Voltage High[2]	I_{OH} = -0.2mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			GND+0.01	V
6	I_{OL}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	µA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}			800	µA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 3.33MHz			2.0	mA
9	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
10	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: 5.0V ± 10%, C_L = 50pF, T_A = -40°C to +85°C, f_C = 3.33MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{LIN}	LXMAR Pulse Width IN	250			ns
2	t_{AIS}	Address Setup Time IN: DX-LXMAR (↓)	70			ns
3	t_{AIH}	Address Hold Time IN: LXMAR(↓)-DX	100			ns
4	t_{DEN}	Data Output Enable Time: DEVSEL(↓)-DX			350	ns
5	t_{CEN}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			350	ns
6	t_{DIS}	Data Input Setup Time: DX-DEVSEL(↑)	100			ns
7	T_{DIH}	Data Input Hold Time: DEVSEL(↑)-DX	100			ns
8	t_{RST}	RESET Input Pulse Width	500			ns
9	t_{SID}	SKP/INTX to SKP/INT Propagation Delay			120	ns
10	t_{DMLX}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			120	ns
11	t_{DEM}	Enable/Disable Time from DMAGNT to EMA Lines			80	ns
12	t_{MDR}	MEMSEL* Pulse Width READ	550			ns
13	t_{MDW}	MEMSEL* Pulse Width WRITE	700			ns
14	t_{MDWR}	MEMSEL* Pulse Width WRITE/REFSH	400			ns
15	t_{LD}	LXMAR* Pulse Width	260			ns
16	t_{DRAT}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	85			ns
17	t_{DXAS}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	125			ns
18	t_{DXAH}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	125			ns
19	t_{DREN}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	400			ns
20	t_{RUP}	UP Pulse Width DMA READ	260			ns
21	t_{DWAT}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	550			ns
22	t_{DWEN}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	400			ns
23	t_{MWS}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	100			ns
24	t_{DMS}	DMAEN Setup Time Wrt XTA (↑)	100			ns
25	t_{DMH}	DMAEN Hold Time Wrt XTA (↑)	100			ns
26	t_{WUP}	UP Pulse Width DMA WRITE	550			ns

INTERSIL

IM6102

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6102 ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... +4.0V to +7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	$GND \le V_{IN} \le V_{CC}$	-1.0		1.0	µA
4	V_{OH}	Output Voltage High [2]	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OL}	Output Leakage	$GND \le V_{OUT} \le V_{CC}$	-1.0		1.0	µA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}		1.0	800	µA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 2.5MHz			1.8	mA
9	C_{IN}	Input Capacitance [1]			7.0	8.0	pF
10	C_O	Output Capacitance [1]			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: 5.0V ± 10%, C_L = 50pF, T_A = -40°C to +85°C, f_C = 2.5MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{LIN}	LXMAR Pulse Width IN	300			ns
2	t_{AIS}	Address Setup Time IN: DX-LXMAR (↓)	80			ns
3	t_{AIH}	Address Hold Time IN: LXMAR(↓)-DX	120			ns
4	t_{DEN}	Data Output Enable Time: DEVSEL(↓)-DX			400	ns
5	t_{CEN}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			400	ns
6	t_{DIS}	Data Input Setup Time: DX-DEVSEL(↑)	100			ns
7	T_{DIH}	Data Input Hold Time: DEVSEL(↑)-DX	100			ns
8	t_{RST}	RESET Input Pulse Width	500			ns
9	t_{SID}	SKP/INTX to SKP/INT Propagation Delay			150	ns
10	t_{DMLX}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			150	ns
11	t_{DEM}	Enable/Disable Time from DMAGNT to EMA Lines			100	ns
12	t_{MDR}	MEMSEL* Pulse Width READ	750			ns
13	t_{MDW}	MEMSEL* Pulse Width WRITE	950			ns
14	t_{MDWR}	MEMSEL* Pulse Width WRITE/REFSH	550			ns
15	t_{LD}	LXMAR* Pulse Width	350			ns
16	t_{DRAT}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	750			ns
17	t_{DXAS}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	120			ns
18	t_{DXAH}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	175			ns
19	t_{DREN}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	550			ns
20	t_{RUP}	UP Pulse Width DMA READ	350			ns
21	t_{DWAT}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	750			ns
22	t_{DWEN}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	550			ns
23	t_{MWS}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	100			ns
24	t_{DMS}	DMAEN Setup Time Wrt XTA (↑)	100			ns
25	t_{DMH}	DMAEN Hold Time Wrt XTA (↑)	100			ns
26	t_{WUP}	UP Pulse Width DMA WRITE	750			ns

IM6102AM (Military)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Military IM6102AM ..... -55°C to +125°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... +4.0V to +11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	$GND \leq V_{IN} \leq V_{CC}$	-1.0		1.0	µA
4	V_{OH}	Output Voltage High[2]	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OL}	Output Leakage	$GND \leq V_{OUT} \leq V_{CC}$	-1.0		1.0	µA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}			900	µA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 5.0MHz			4.0	mA
9	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
10	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, C_L = 50pF, T_A = -55°C to +125°C, f_C = 5.0MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{LIN}	LXMAR Pulse Width IN	135			ns
2	t_{AIS}	Address Setup Time IN: DX-LXMAR (↓)	60			ns
3	t_{AIH}	Address Hold Time IN: LXMAR(↓)-DX	60			ns
4	t_{DEN}	Data Output Enable Time: DEVSEL(↓)-DX			260	ns
5	t_{CEN}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			260	ns
6	t_{DIS}	Data Input Setup Time: DX-DEVSEL(↑)	60			ns
7	T_{DIH}	Data Input Hold Time: DEVSEL(↑)-DX	60			ns
8	t_{RST}	RESET Input Pulse Width	250			ns
9	t_{SID}	SKP/INTX to SKP/INT Propagation Delay			120	ns
10	t_{DMLX}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			120	ns
11	t_{DEM}	Enable/Disable Time from DMAGNT to EMA Lines			60	ns
12	t_{MDR}	MEMSEL* Pulse Width READ	375			ns
13	t_{MDW}	MEMSEL* Pulse Width WRITE	475			ns
14	t_{MDWR}	MEMSEL* Pulse Width WRITE/REFSH	275			ns
15	t_{LD}	LXMAR* Pulse Width	175			ns
16	t_{DRAT}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	375			ns
17	t_{DXAS}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	70			ns
18	t_{DXAH}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	70			ns
19	t_{DREN}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	275			ns
20	t_{RUP}	UP Pulse Width DMA READ	175			ns
21	t_{DWAT}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	375			ns
22	t_{DWEN}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	275			ns
23	t_{MWS}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	50			ns
24	t_{DMS}	DMAEN Setup Time Wrt XTA (↑)	50			ns
25	t_{DMH}	DMAEN Hold Time Wrt XTA (↑)	50			ns
26	t_{WUP}	UP Pulse Width DMA WRITE	375			ns

IM6102-1M (Military)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Military IM6102-1M ..... -55°C to +125°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... +4.0V to +7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = -55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC} -2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	$GND \le V_{IN} \le V_{CC}$	-1.0		1.0	µA
4	V_{OH}	Output Voltage High[2]	I_{OH} = 0mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			0.45	V
6	I_{OL}	Output Leakage	$GND \le V_{OUT} \le V_{CC}$	-1.0		1.0	µA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}			800	µA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 2.5MHz			2.0	mA
9	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
10	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C, f_C = 2.5MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{LIN}	LXMAR Pulse Width IN	300			ns
2	t_{AIS}	Address Setup Time IN: DX-LXMAR↓	80			ns
3	t_{AIH}	Address Hold Time IN: LXMAR↓-DX	120			ns
4	t_{DEN}	Data Output Enable Time: DEVSEL↓-DX			400	ns
5	t_{CEN}	Controls Output Enable Time: DEVSEL↓-lines C0,C1,C2,S/I			400	ns
6	t_{DIS}	Data Input Setup Time: DX-DEVSEL↑	100			ns
7	T_{DIH}	Data Input Hold Time: DEVSEL↑-DX	100			ns
8	t_{RST}	RESET Input Pulse Width	500			ns
9	t_{SID}	SKP/INTX to SKP/INT Propagation Delay			130	ns
10	t_{DMLX}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			130	ns
11	t_{DEM}	Enable/Disable Time from DMAGNT to EMA Lines			100	ns
12	t_{MDR}	MEMSEL* Pulse Width READ	750			ns
13	t_{MDW}	MEMSEL* Pulse Width WRITE	950			ns
14	t_{MDWR}	MEMSEL* Pulse Width WRITE/REFSH	550			ns
15	t_{LD}	LXMAR* Pulse Width	350			ns
16	t_{DRAT}	DMA READ Access Time: LXMAR*↓-UP↑	750			ns
17	t_{DXAS}	DX & EMA Address Setup Time Wrt LXMAR*↓	120			ns
18	t_{DXAH}	DX & EMA Address Hold Time Wrt LXMAR*↓	175			ns
19	t_{DREN}	DMA READ Enable Time: MEMSEL*↓-UP↓	550			ns
20	t_{RUP}	UP Pulse Width DMA READ	350			ns
21	t_{DWAT}	DMA WRITE Access Time: LXMAR*↓-MEMSEL*↑	750			ns
22	t_{DWEN}	DMA WRITE Enable Time: UP↓-MEMSEL*↑	550			ns
23	t_{MWS}	MEMSEL* Setup Time DMA WRITE MEMSEL*↓-LXMAR*↓	100			ns
24	t_{DMS}	DMAEN Setup Time Wrt XTA↑	100			ns
25	t_{DMH}	DMAEN Hold Time Wrt XTA↑	100			ns
26	t_{WUP}	UP Pulse Width DMA WRITE	750			ns

APPLICATION

IM6100-IM6102 Interface in a Buffered System.