INSTRUCTION MANUAL

34H
OSCILLOSCOPE
DISPLAY

PDP-9

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

34H

OSCILLOSCOPE

DISPLAY

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ILLUSTRATIONS

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1. INTRODUCTION

The Type 34H Oscilloscope Display is a two-axis digital-to-analog converter and intensifying circuit which displays points on the screen of a cathode ray tube. This manual contains installation, operation, programming, and maintenance information for the 34H Display manufactured by Digital Equipment Corporation, Maynard, Massachusetts.

1.1 Related Documentation

Table 1 lists other publications containing information pertaining to the 34H or related equipment.

Table 1
Reference Documents

Title	Doc. No.	Contents
Digital Logic Handbook	C-105	Specification and description of most FLIP CHIP modules.
PDP-9 User Handbook	F-95	Operation and programming information for the PDP-9.
PDP-9 Maintenance Manual Volumes I and II	F-97	Operation and maintenance information for the PDP-9, including engineering drawings.

2. INSTALLATION

The oscilloscope is supplied in a cabinet-mounted configuration. It mounts in a standard 19-in. rack adjacent to the central processor. Unless otherwise specified, it is placed in the top right-hand position as viewed from the front of the console.

The display logic modules are located in the lower right-hand portion of the I/O logic in the processor rack (Drawing MU-KD09-A-14, sheet 2). Cabling to the oscilloscope consists of control for the x-axis, y-axis, intensity, and the light pen option. Cable connections are shown on Drawing UA-34H-0-0.

2.1 Power

There are no additional power supplies required for the display logic. All logic power is obtained from the basic PDP-9 system. Oscilloscope power is determined by the type of scope and the system power used.

3.   PROGRAMMING

Table 2 lists the IOT commands that are assigned to the 34H Display.

Table 2
IOT Commands

Mnemonic Code	Octal Code	Description
DSF	700501	Skip if display (light pen) flag is a 1.
DXC	700502	Clear x-coordinate buffer
DXL	700506	Load the x-coordinate buffer with I/O Bus 8-17.
DXS	700546	Load the x-coordinate buffer and display the point specified by the XB and YB.
DYC	700602	Clear the y-coordinate buffer.
DYL	700606	Load the y-coordinate buffer with I/O bus 8-17.
DYS	700646	Load the y-coordinate buffer and display the point specified by the YB and XB.
DLB	700704	Load the brightness register from I/O Bus 16-17.

3.1   Display Examples

The displays shown in Figures 1, 2, and 3 may be observed by inserting the corresponding program into the processor.
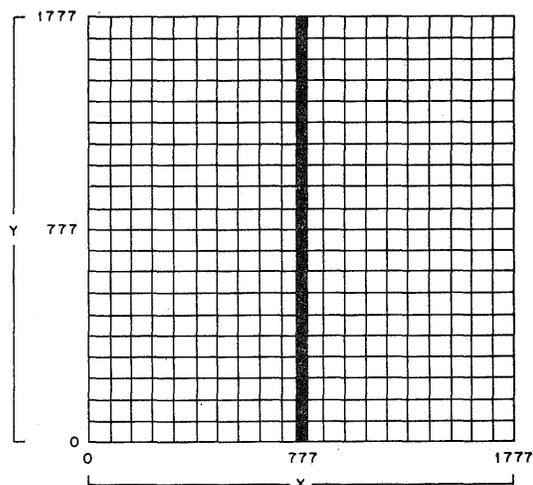
a.   Vertical Line

Figure 1   Vertical Line Display

2

0	LAW	777	Establishes x-position of line
1	DXS	700546	
2	DZM	100	
3	LAC	100	
4	ISZ	100	
5	DYS	700646	
6	SAD	101	Number in location 101 establishes length of line (101/1777).
7	JMP 2		
10	JMP 3		

b. Horizontal Line
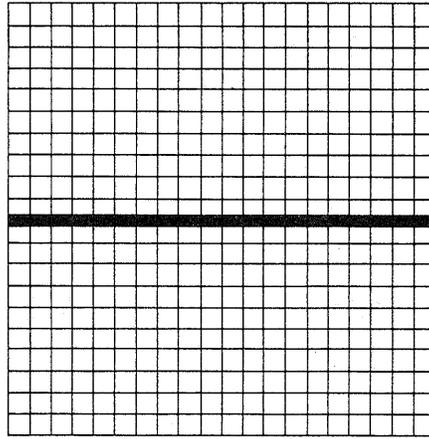
Figure 2 Horizontal Line Display

				X	Y
1000	0	LAW	777	760777	
	1	DYS	700646	700646	700546
	2	DZM	100	140100	
	3	LAC	100	200100	
	4	ISZ	100	440100	
	5	DXS	700546	700546	700646
	6	SAD	101	540101	LOAD 101 MED
	7	JMP 2		601002	17778
	10	JMP 3		601003	

3
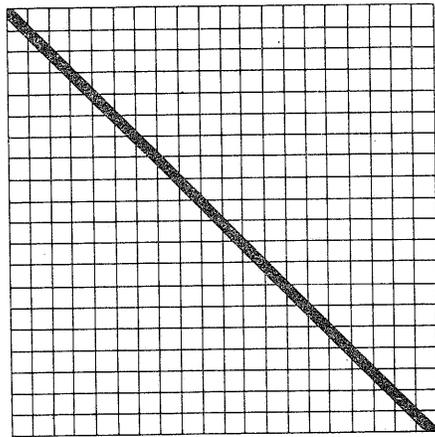
c. Diagonal Line

Figure 3   Diagonal Line Display

0	DZM	100	
1	LAC	100	
2	ISZ	100	
3	DYS	700646	The slope of the line may be reversed by interchanging the DYS and DXS instruction sequence.
4	DXS	700546	
5	JMP 1		

4.   THEORY OF OPERATION

A simplified block diagram of the 34H Display is shown in Figure 4. The 34H consists of an x-axis (XB) and y-axis (YB) buffer, a brightness register (BR), and an IOT decoder.

The Type 34H Display points on the face of an oscilloscope CRT. Each point is located by its x- and y-coordinate, in a 1024-by-1024-point array whose origin is in the lower left-hand corner of the CRT screen. The x- and y-coordinates are determined by two 10-bit buffers whose inputs are bits 8-17 of the DEC PDP-9 computer accumulator. The binary data in these buffers is converted to an analog (-10 to 0V) deflection signal.

A 2-bit brightness register (bits 16 and 17 of the AC) determines the intensity of the point being displayed. The intensity scale is as follows.

Intensity Level	BR Contents
No display	0
Dimmest	1
Average	2
Brightest	3

4

16-17

IOT 0704   BR, 01

3

IOP 1, 2, 4   DELAYS

DSO-5   IOT 0504
                          0604
                                    INTENSITY

0502
IOT 050X

IO BUS   8-17   XB

1024 ADDRESSES

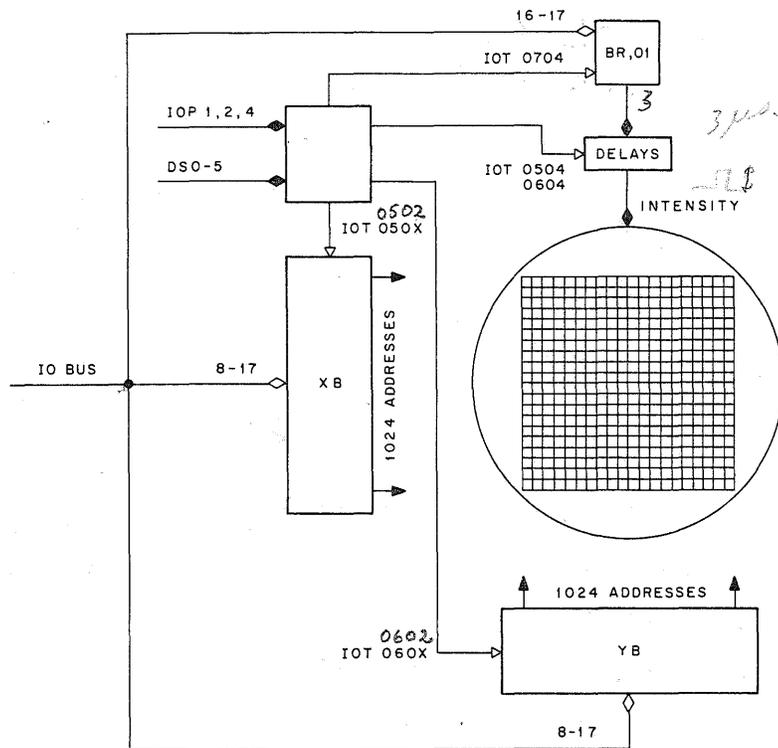1024 ADDRESSES

0602
IOT 060X   YB

8-17

Figure 4   Simplified Block Diagram, 34H Display

The XB and YB are loaded separately and may be loaded without intensifying the CRT. The usual procedures is to load one buffer, load the second buffer and then display the point. The Type 34H requires 10 µs to display a point. Points can be plotted at approximately a 30 kHz rate.

A 6-bit device selection address code (0X EN and DS 3-5) from the PDP-9 is combined with timing levels (IOP 1, 2, and 4) to generate the in-out transfer commands (IOT) which control operation of the display logic. The functions of the IOT commands that are generated are explained in Section 3 of the manual.

4.1   Logic Operation

Logic control of the 34H Display as it relates to the PDP-9 computer is shown on Drawing D-BS-34H-0-1, sheets 1 and 2.

4.1.1   Processor Turn-On - During processor turn-on, IO PWR CLR POS pulses are generated, clearing the brightness register (BR) and light pen flag (34 LP FLG) flip-flops (Drawing D-BS-34H-0-1,

sheet 1). With BR cleared, there is no display on the CRT screen. In the cleared state, the 34 LP FLG prevents program interrupt and skip commands from being generated. IO PWR CLR POS is also generated by the CAF (clear all flags) instruction.

4.1.2   IOT Generation - IOT commands assigned to 34H Display (Section 3) are decoded from the device selection bits (OX EN and DS 3-5) and timing levels (IOP 1, 2, and 4) transmitted from the processor (Drawing D-BS-34H-0-1, sheet 2). These IOTs clear and load the coordinate buffers, load the BR, and control the intensity delay circuit.

4.1.3   Coordinate Buffers - The x- and y-coordinate buffers (XB and YB) contain 10 flip-flops each (sheet 1). There are 1024 (2^{10}) possible locations obtainable from each buffer. The buffers are cleared at event time 2 (IOP2) of the processor timing cycle. Address data, I/O Bus 8-17, is loaded into the buffers at event time 3 (IOP4).

The normal addressing procedure, after the buffers are cleared, is to issue a load command for one buffer followed by a load and display command for the second buffer. Outputs from the XB and YB are fed to digital-to-analog converters. Analog voltages from the converters are fed to the deflection circuits of the oscilloscope. These voltages (one from each buffer) vary in 1024 discrete levels with a voltage swing from 0V to -10V. The D/A output will be 0V (most positive) when all the buffer flip-flops are in the 1 state. It will be -10V (most negative) when all the flip-flops, except the least significant bit, are in the 0 state.

4.1.4   Intensity Display - The brightness intensity of the point being displayed is determined by the contents of the brightness register (BR) and the intensity delay register. Initially the BR is cleared by the IO PWR CLR POS pulse setting it to the 0 state. I/O Bus 16 and 17, which specify the level of brightness desired, are gated in at event time 3 by IOT 0704. The BR outputs are then combined at the delay register input gates. A 1-μs delay, controlled by IOT 0504, 0604, and sub-device bit SD 0 P, gates the BR outputs into the desired delay. Maximum brightness is produced by the 3-μs delay, average brightness by the 0.8-μs delay, and minimum brightness by the 0.4-μs delay. An intensity amplifier accepts the brightness level chosen and transmits it to the oscilloscope CRT. It also generates the light pen strobe level (LP STB).

The intensity amplifier (W681, H36, sheet 1) is capable of delivering either a positive or negative output "intensity" level to the CRT. If the user desires grid blanking, the output connection to the scope would be as shown (pin N). For cathode blanking, the intensity level output is taken from pin R of the intensity amplifier.

4.1.5   Light Pen Operation - A photomultiplier light pen may be used by the 34H to communicate with a computer program. The light pen detects a point of light on the CRT screen and transmits it to the display control circuits (sheet 1). The light pen output (LP OUT) and light pen strobe (LP STB) trigger the light pen flag flip-flop (34 LP FLG) setting it to the 1 state. LP STB is generated by the intensity amplifier and is of the same duration as the intensity signal. The output of the light pen flag flip-flop is combined with other pulses and levels to generate skip or interrupt requests to the computer (sheet 2).

The use of the light pen must be considered for the type of scope being used. If a high persistent scope is used, care must be taken that the intensity of the last point displayed has decayed sufficiently to allow valid light pen hits to be acknowledged.

4.1.6   API and Program Interrupt Requests - Device initiated data transfers, from the display control logic, are made possible by program interrupt break requests. Interrupt requests are initiated when the light pen has sensed a spot on the CRT screen. An interrupt request, depending on the type required, is then sent to the processor. After priority status has been determined, the processor sends a grant level to the display logic which responds with the interrupt break address location. The computer performs the instruction in this location, then returns to the main program.

Automatic priority interrupt (API) and program interrupt request (PROG INT RQ) logic is shown on Drawing D-BS-34H-0-1, sheets 1 and 2. When the light pen senses a spot on the CRT screen, it generates a level (LP OUT) which is combined with the light pen strobe (LP STB) level from the intensity amplifier to trigger the light pen flag flip-flop (34 LP FLG). The 34 LP FLG, now set to the 1 state, is combined with IO SYNC SP (B), setting the REQ flip-flop in the W104 module, sheet 2. API 2 RQ is generated from REQ and sent to the processor priority determination logic. If there is no higher priority device in use, the processor sends the grant level (API 2 GR (1)) to the display logic. This level triggers the ENA flip-flop in the W104, gating IO ADDR 12, 14, and 15 onto the I/O bus. This address specifies the API break location, and the processor executes the instruction in this location. Usually, this instruction puts the processor into a device service routine, then returns to the main program.

Program interrupt request (PROG INT RQ) are initiated in the same manner as API. The 34 LP FLG is set to 1 upon receipt of LP OUT and LP STB. 34 LP FLG (1) and DPY API RQ (1) are combined to generate PROG INT RQ (sheet 1), putting the processor into the priority determination routine. At IOP 1 time the display logic generates INT SKP RQ BUS at which time the processor enters the device service routine. Upon completion of the device service routine, the processor returns to the main program.

When the API option is included in the system, DPY API RQ (1) is generated in the W104 module (sheet 2). Under this condition, DPY API RQ (1) is generated by IO SYNC SP (B) and 34 LP FLG (1). The additional timing insures that API has higher priority than program interrupt.

5.   MAINTENANCE

5.1   Preventive Maintenance

The general preventive maintenance procedures in the PDP-9 Maintenance Manual (DEC Doc. F-97) also apply to the display control logic.

5.2   Power Supply Checks

As there are no separate supplies required for the display control logic, power supply checks for the DEC Type 709 Power Supply, in the processor, should be made as described in the PDP-9 Maintenance Manual (Chapter 4).

5.3   Margin Checks

Marginal checking of the display logic is performed by utilizing the marginal check panel at the front of the processor and the marginal check switches at the rear of the processor as described in the PDP-9 Maintenance Manual (F-97), Figures 2-2 and 4-1. Figure 2-2 explains the functions of the marginal check panel, and marginal checking is described in Paragraphs 4.4 and 4.6.1 of the PDP-9 Maintenance Manual.

MC switch 09, on the switch panel, is selected for applying margins to the display logic. Specifications for the display logic are as follows.

Supply Voltage	Margins
+10V	-4V, +5V
-15V	±2.5V

5.4   Oscilloscope Maintenance

For information on maintenance and troubleshooting procedures, refer to the documentation provided by the manufacturer of the oscilloscope. The basic 34H Oscilloscope Display Unit utilizes a Tektronix RM-503 Oscilloscope; however, other models may be used.

5.5   Display Diagnostic

Display Diagnostic (PDP-9, 30D, 34H, 370), MAINDEC-9A-D6AB-D, is a program which facilitates the calibration, check out, and diagnosis of a display, such as the 34H, with or without a light pen (370) on a PDP-9 computer. With this program, the digital-to-analog resistor ladder networks may be calibrated, the display may be checked for linearity, flyback, hysteresis and scope burn. The light pen may be checked for flag function (with and without interrupt and API) and field of view. All errors are visual except the light pen flag tests.

Incorrect display indications, such as distortion or non-linear traces, may result from faulty digital-to-analog converter modules (A601 and A604), the input flip-flops to the DAC or the -10V reference supply modules (A704). Distortion appearing in vertical lines may be caused by a change in voltage from the -10V reference. In this case a substitute module should be inserted in its place as these modules are factory aligned.

Faulty flip-flop outputs can be observed with an oscilloscope while programs, such as those shown in Paragraph 3 are run. Interchanging similar DAC's should reveal suspected modules. The specifications for these three types of modules are included in the DEC Logic Handbook (C-105).

5.6   Engineering Drawing List

The following is a list of DEC drawings that pertain to the Type 34H Oscilloscope Display, but they are not supplied with this manual.

Drawing No.	Rev.	No. Pages	Title
A-ML-34H-0	F	1	Display Control (Option)
A-PL-KD09-A-0	A	1	I/O Assembly (KD09A)
A-PL-KD09-A-14	AC	2	Module Parts List
A-PL-34H-0-0	-	1	Display Control Type 34H
A-PL-34H-0-2	-	1	Module Parts List 34H-0 Option
C-VA-34H-0-0	-	1	Display Control Type 34H
D-BS-34H-0-1	E	2	Display Control
D-MU-KD09-A-14	AC	2	PDP-9 IO Module List

5.7   MODULE LIST

Module No.	No. Req.	Description
A601	6	3-bit DAC
A604	2	2-bit DAC
A704	1	10V Precision Power Supply
R002	1	Diode Cluster
R111	5	Diode Cluster
R302	2	Delay (One shot)
S107	1	Inverter
S202	1	Dual Flip-Flop
S203	7	Triple Flip-Flop
S603	1	Pulse Amplifier
W681	1	Scope Intensifier

6.   GLOSSARY OF TERMS

API 2 RQ	Priority interrupt levels sent to processor when light pen flag is a 1.
BR	Brightness register flip-flop.
DS	Device selection line from PDP-9
INTENSITY	Output level from intensity delay register
INT SKP RQ BUS	Forces I/O skip in the PDP-9
IO ADDR 12,14,15	Determines API break address.
IO BUS	Input bus from PDP-9
IOP 1, 2, 4	Event time 1, 2, and 3 respectively from PDP-9
IO PWR CLR	Clear pulse from PDP-9
IO SYNC SP	Generated during power-on or power-off and the CAF (clear all flags) instruction.
IOT	Decoded in-out transfer command
PROG INT RQ	Program interrupt request to PDP-9.
LP FLG	Light pen flag level
LP STB	Light pen strobe level
SD	Sub device bit from PDP-9
0X EN	Level generated when MB 6, 7, 8 (DS 0, 1, 2) are zero during an IOT

05 SEL
06 SEL   Level generated when device selection bits equal 5, 6, or 7.
07 SEL

34 LP FLG   Light pen flip-flop