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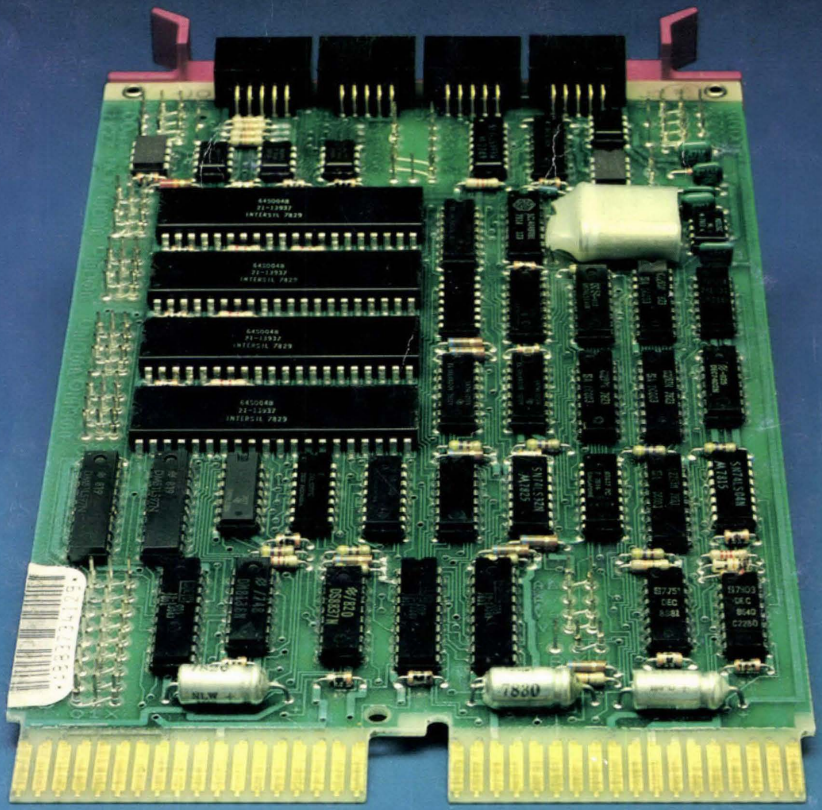

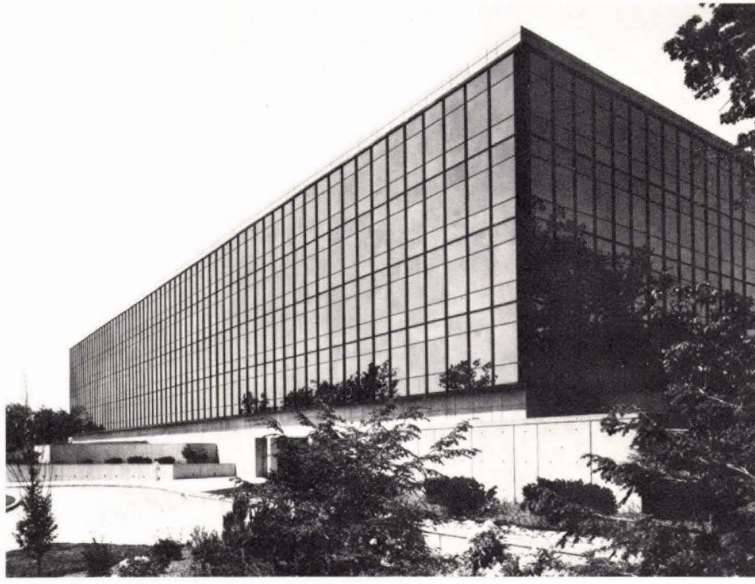

DIGITAL facility, Marlboro, Massachusetts

CORPORATE PROFILE

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part 1
introduction

INTRODUCTION

GENERAL

This handbook is a reference guide for the interface and peripheral hardware options that can be installed on the LSI-11 bus. It includes descriptions, specifications, configuration information, programming information as applicable to the options, and functional theory. Because the hardware options described in this handbook are designed to interface with a processor via the LSI-11 bus, the user should be familiar with the contents of the appropriate processor handbook.

The handbook is organized into two parts. Part 1 contains general information about microcomputer interfaces; Part 2 contains description of the interface options in alphanumeric sequence.

Digital Equipment Corporation designs and manufactures the options described in this handbook. The general design criterion was to provide maximum system throughput for options when installed on the LSI-11 bus. LSI-11 bus-compatible processors, interfaces, and peripherals are designed to work together, providing a broad spectrum of system-compatible hardware options. The memory and peripheral devices can be used with various LSI-11 bus configuration; the system can later be expanded or modified to meet new system requirements. This hardware flexibility, when coupled with DIGITAL software and support, provides a single source for all present and future microcomputer processing needs.

LSI-11 FAMILY CHARACTERISTICS

LSI-11 bus systems include various processors, memory and peripheral device options, and software. Some of the characteristics of the LSI-11 bus systems are:

- Low-cost powerful components for integration into any small- or medium-sized computer system.
- Direct addressing of all memory locations and peripheral device registers.
- Efficient processing of 8-bit bytes (characters) without the need to rotate, swap, or mask.
- Asynchronous bus operation that allows system components to run at their highest possible speed; replacement with faster devices means faster operation without other hardware or software changes.
- A module component design that provides ease and flexibility in configuring systems.

INTRODUCTION

- Inherent direct memory access capabilities for high data rate devices.
- A bus structure that provides position-dependent priority for peripheral device interfaces connected to the I/O bus.
- Vectored interrupts that allow service routine entry without device polling.

Processors

The processor is connected to the LSI-11 bus (backplane) as a subsystem that executes programs and arbitrates usage of the LSI-11 bus for peripherals. It contains multiple, high-speed, general-purpose registers that can be used as accumulators, address pointers, index registers, and other specialized functions. The processor can perform data transfers directly between peripheral input/output (I/O) devices and memory without disturbing the processor registers. Data transfers include both 16-bit word and 8-bit byte data.

LSI-11 Bus

System components, including the processor, memory, and peripherals, are interconnected and communicate with each other via the LSI-11 bus. The form of communication is the same for all devices on the bus; instructions that communicate with memory can communicate with peripheral devices. Each device, including memory locations and peripheral device registers, is assigned an individual byte or word address on the LSI-11 bus.

The LSI-11 bus supports 18-bit addresses. However, processors and peripherals having a 16-bit addressing capability are completely PDP-11 hardware- and software-compatible within the 16-bit limitation. By PDP-11 convention, all peripheral device addresses are located within the upper 4K address space in the system, whether 16-bit or 18-bit addresses are used. This 4K address space is called the I/O page or "bank 7."

Whenever the I/O page is addressed, the processor must assert the BBS7 L bus signal. All peripheral devices use this signal line during addressing rather than decoding address bits <15:13> or <17:13>. An active (asserted) BBS7 L signal will always indicate an address in the I/O page, enabling peripheral device addressing.

Peripheral device addresses within the I/O page are decoded by each peripheral device. Each peripheral device will include one or more "device register(s)." These registers can be accessed under program

control in exactly the same manner as memory locations. Unique addresses within the I/O page are encoded on address bits <12:00>.

NOTE

Address bits, for the purpose of this discussion, are logical states present on LSI-11 bus signal lines BDAL <17:00> L during the addressing portion of a bus cycle.

Refer to the appropriate processor handbook for a complete description of bus transactions, including bus cycles, addressing, etc.

Device Registers

All peripheral devices are defined by one or more device registers that are addressed as part of the main memory. These registers are generally designated control and status registers.

Control and status registers (CSRs) contain all the necessary information to establish communications with the device. Some devices will require fewer than 16 status bits, while other devices could require more than 16 bits and therefore will require additional registers. The bits of the CSR have predetermined assigned functions. Typical bit functions include interrupt enable, error, done or ready, and enabled.

Data buffer registers (DBRs) are for temporarily storing data to be transferred into and out of the processor. The number and type of data registers is a function of the individual peripheral device requirements.

Interrupts

Interrupts allow devices to obtain processor service when they are "ready" for service, or "done" with a specific operation. The interrupt structure allows the processor to execute other programs while one or more peripherals are "busy." When a peripheral requires service it requests an interrupt. The processor completes execution of the present instruction, saves PC and PS words on the stack, and acknowledges the interrupt. The highest priority peripheral device currently requesting interrupt service responds by inputting its interrupt vector address to the processor. The processor uses this vector address as a pointer to two memory locations containing the PC (starting address) and PS for the peripheral device interrupt service routine. Program control is transferred from the interrupted program to the routine associated with the requesting peripheral device. Note that no device polling is required, since the interrupt vector is unique for that

device. Once the device service routine execution has been completed, control is returned either to the previously interrupted program or to another peripheral device requesting interrupt service.

Memory Address

Memory addresses are generally limited to the address space other than the I/O page. However, the I/O page can contain read-only memory (ROM) for disk bootstraps, paper tape loaders, diagnostics, etc. or read/write memory for DMA buffers. The system designer must use care in assigning memory addresses within the I/O page to avoid conflicts with peripheral device addresses used for actual system hardware, or addresses that system software may attempt to access for peripheral devices not actually installed in the system. See Appendix A for the standard assignments of the addresses in the I/O page.

SPECIFICATIONS

All the LSI-11 bus modules will operate under the following conditions:

Temperature	5° to 60° C (41° to 140° F)
Humidity	10 to 95% (no condensation)

When operating at the maximum outlet temperature (60° C or 140° F), adequate air flow must be maintained to control the inlet to outlet temperature rise across the modules to 5° C (9° F) maximum. The air flow should be directed to flow across the modules.

All the individual module specifications are included in the detailed descriptions of the peripheral or option. A summary of the module characteristics is provided in Table 2; these characteristics are defined as follows:

1. The option designation is the alphanumerical code assigned to the option.
2. The module number is the number assigned to the interface modules that are connected to the LSI-11 bus. This number is printed on the module handle and can be used as a quick reference to determine what specific options are installed in any system. The module numbers are listed numerically in Table 3 so that the user can identify the options installed by using the module numbers.
3. The module description identifies the category of the option.
4. The power requirements specify the power by the option when connected to the bus backplane. These requirements are used to determine the total power supply loading within a single system.

5. The bus loads for ac and dc loading are provided so that the user can calculate the total ac and dc loading for any system.
6. The interface modules are standarized as either a double or a quad and all are extended length. The double size module is 13.2 cm (5.2 in.) high, 22.8 cm (8.9 in.) long, and 1.27 cm (0.5 in.) wide. The quad size module is 26.5 cm (10.5 in.) high, 22.8 cm (8.9 in.) long, and 1.27 cm (0.5 in.) wide (Figure 1).

DESCRIPTION OF OPTION CATEGORIES

The LSI-11 bus peripherals and options are classified into general categories that pertain to their performance and function. This listing indicates the wide span of equipment capability available to the user

Interface Options

AAV11-A — The AAV11-A is a 4-channel, 12-bit digital-to-analog converter module that includes control and interfacing circuits. It has four D/A converters, a dc-dc converter that provides power to the analog circuits, and a precision voltage reference. Each channel has its own holding register that can be addressed separately and provides 12 bits of resolution. Bits 0, 1, 2, and 3 of the fourth holding register are brought out to the I/O connector so that they can be used as a 4-bit digital output register.

ADV11-A — The ADV11-A is a 12-bit successive approximation analog-to-digital converter that samples analog data at specified rates and stores the digital equivalent value for processing. The multiplexer can accommodate up to 16 single-ended or 8 quasi-differential inputs. The converter uses a patented auto-zeroing design that measures the sampled data with respect to its own offset and therefore cancels out its own offset error.

External event inputs can originate at the user's equipment or from the Schmitt trigger output of the KWV11-A clock. Three reference signals are provided for self-testing any channel input. These signals consist of two dc levels and one bipolar triangular waveform. This output can be used with DIGITAL diagnostic software to produce a data base for extremely precise analog linearity testing.

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DRV11

The DRV11 is a parallel interface module that is used to interconnect the LSI-11 bus with general-purpose, parallel line TTL or DTL devices. It allows program-controlled data transfers at rates up to 40K words per second and uses LSI-11 bus interface and control logic to generate interrupts and process vector handling. The data are handled by 16 diode-clamped input lines and 16 latched output lines. There are two 40-pin connectors on the module for user interface applications.

DRV11-B

The DRV11-B is an interface module that uses direct memory access (DMA) to transfer data directly between the system memory and an I/O device. The interface is programmed by the processor to move variable length blocks of 8- or 16-bit data words to or from specified locations in the system memory. Once programmed, there is no processor intervention required. The module can transfer up to 250K 16-bit words per second in the single-cycle mode and up to 500K 16-bit words per second in the burst mode. It also allows read-modify-restore operations.

DRV11-J

Sixty-four input/output data lines are now available on a double-height module for the LSI-11/2, LSI-11/23, PDP-11/03, and PDP-11/23. The DRV11-J also includes an advanced interrupt structure with bit interruptability up to 16 lines, programmable interrupt vectors, and program selection of fixed or rotating interrupt priority within the DRV11-J. The DRV11-J's bit interrupts for real-time response make it especially useful for sensor I/O applications. It can also be used as a general-purpose interface to custom devices, and two DRV11-Js can be connected back-to-back as a link between two LSI-11 buses.

DRV11-P

The DRV11-P is a foundation wire-wrap interface module with a 40-pin I/O connector. Approximately 25 percent of the module is occupied by bus transceivers, interrupt vector generation logic, device comparator logic, protocol logic, and interrupt logic. The remaining 75 percent is for user applications; this portion has plated-through holes for securing

ICs and wire-wrap pins for interconnecting the user's curcuits. The plated-through holes can accept 6-, 8-, 14-, 18-, 20-, 22-, 24-, and 40-pin dual-in-line integrated circuits or discrete components.

IBV11-A — The IBV11-A is an interface module that interconnects the LSI-11 bus with the instrument bus described in IEEE standard 488 1975, "Digital Interface for Programmable Instrumentation." The IBV11-A makes a processor-controlled programmable instrument system possible. The module can accommodate up to 15 IEEE-488 devices and is PDP-11 software-compatible.

KWV11-A — The KWV11-A is a programmable real-time clock/counter that provides a means of determining time intervals or counting events. It can be used to generate interrupts to the processor at predetermined intervals or establish timing between input and output events. It can also initialize the ADV11-A analog-to-digital converter by a clock counter overflow or by firing a Schmitt trigger. The clock counter has a resolution of 16 bits and can be driven by any one of five crystal-controlled frequencies (100 Hz to 1 MHz), from a line frequency input, or from a Schmitt trigger fired by an external input. The module can operate in any of four programmable modes: single interval, repeated interval, external event timing, and external event timing from zero base.

Communications Options

DLV11 — The DLV11 is a serial line unit (SLU) that interfaces with asynchronous serial I/O devices. The module has jumper-selectable baud rates (50-9600) and serial word format that includes the number of stop bits, number of data bits, and even, odd, or no parity bit. The DLV11 can support 20 mA current loop interfaces or EIA "data leads only" interfaces.

DLV11-E — The DLV11-E is an asynchronous line interface module that interconnects the LSI-11 bus to standard serial communications lines. The module receives serial data, converts it to parallel data, and

transfers it to the LSI-11 bus. Also, it accepts parallel data from the LSI-11 bus, converts it to serial data, and transmits it to the peripheral device. The module has jumper-selectable or software-selectable baud rates (50-19,200), and jumper-selectable data bit formats. The DLV11-E offers full modem control for EIA/CCITT interfaces.

DLV11-F

The DLV11-F is an asynchronous line interface module that interconnects the LSI-11 bus to several types of standard serial communications lines. The module receives serial data, converts it to parallel data, and transfers it to the LSI-11 bus. It also accepts parallel data from the LSI-11 bus, converts it to serial data, and transmits it to the peripheral device. The module has jumper-selectable or software-selectable baud rates (50-19,200) and jumper-selectable data bits. The DLV11-F supports either 20 mA current loop or EIA standard lines, but does not include modem control.

DLV11-J

The DLV11-J contains four independent asynchronous serial line channels used to interface peripheral devices to the LSI-11 bus. Each channel transmits and receives data from the peripheral device over EIA data leads (lines that do not use a control line). The module can be used with 20 mA current loop devices if a DLV11-KA adapter is used. The DLV11-J has jumper-selectable baud rates from 150 to 39.4 K baud.

DUV11

The DUV11 synchronous line interface module establishes a data communication line between the LSI-11 bus and a Bell 201 synchronous modem or equivalent. The module is fully programmable with respect to sync characters, character length (to to 8 bits), and parity selection. The receiver logic accepts serial data for the LSI-11 bus. The transmitter logic converts the parallel LSI-11 bus data into serial data for the transmission line. The interface logic converts the TTL logic levels to the EIA voltage levels required by the Bell 201 modems and also controls the modem for half-duplex or full-duplex operation.

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DZV11

The DZV11 is an asynchronous multiplexer interface module that interconnects the LSI-11 bus with up to four asynchronous serial data communications channels. The module provides EIA interface voltage levels and data set control to permit dial-up (auto-answer) options with full-duplex modems such as Bell models 103, 113, 212, or equivalent. The DZV11 does not support half-duplex operations or the secondary transmit and receive operations available in some modems such as Bell 202. The DZV11 has applications in data concentration and collection systems where front-end systems interface to a host computer and for use in a cluster controller for terminal applications.

Expansion Memories (For detailed memory descriptions, see the Microcomputer Processor Handbook)

MMV11-A

The MMV11-A is a 4K × 16-bit core memory option that provides nonvolatile read/write storage. The memory can be configured by bank addressing switches. The module is limited to LSI-11 bus backplanes that contain the LSI-11 bus in both the A/B bus and the C/D slots.

MRV11-AA

The MRV11-AA is a read-only memory module on which the user can install fusible link, programmable, read-only memory (PROM) chips or masked read-only memory (ROM) chips. The user selects the address space of the memory by configuring removable jumper wires.

MRV11-BA

The MRV11-BA is a read-only memory module that uses ultraviolet (UV) erasable, programmable, read-only memory (EPROM) integrated circuits. The module also contains a 256 × 16-bit random access memory (RAM) that can be used as a "scratchpad" or "stack" by the system software.

MRV11-C

The MRV11-C is a flexible, high-density ROM module used with the LSI-11 bus. The module contains sixteen 24-pin sockets which accept a variety of user-supplied ROM chips. It will accept masked ROMS, fusible link PROMs, and ultraviolet erasable

PROMs. It accepts several densities of ROM chips up to and including 4K × 8 chips. Using these high-density chips gives the module a total capacity of 64K bytes. The contents of the module can be accessed in one of two ways—either directly or window-mapped. Direct access provides total random access to all ROM locations on the module. Window-mapping provides two 2K-byte windows in memory address space to access 2K-byte segments of the ROM array. The segments that are viewed through each window can be varied under program control.

MSV11-B — The MSV11-B is a 4K × 16-bit dynamic MOS read/write memory module. The user can select the memory addresses of the module by configuring removable jumpers. The memory refresh must be controlled by external bus signals.

MSV11-CD — The MSV11-CD is a 16K × 16-bit dynamic MOS read/write memory module. Refresh is automatically performed by the module but it can be disabled if the user wishes to use the LSI-11 bus refresh signals. This memory module can be configured to operate in the battery backup mode. The user can configure the memory addresses by selecting switch settings.

MSV11-D,-E — The MSV11-D module has either 8K, 16K, or 32K × 16 bits of MOS memory. The MSV11-E is the same as the MSV11-D except that it has an 18-bit word that generates and detects byte parity for each word. The modules have an on-board memory refresh and perform the necessary LSI-11 bus cycles. The memory addressing is selectable by the user by configuring switch settings. The module can use a battery backup system to preserve data when primary power is lost.

MXV11-A — The MXV11-A is a dual height multifunction option module for the LSI-11, LSI-11/2 or LSI-11/23. It contains a read/write memory, provisions for read-only memory, two asynchronous serial line interfaces and a 60 Hz clock signal derived from a crystal oscillator. Read/write memory is supplied with either 8K or 32K bytes (4K or 16K words). Two 24-pin sockets are

provided for +5 V read-only memories. 1K × 8, 2K × 8, or 4K × 8 ROMS may be used. The sockets may also be used for 256 words of bootstrap code. The two asynchronous serial lines transmit and receive EIA-423 signal levels from 150 baud to 38.4K baud. 20 mA active or passive current loop operation at 110 baud may be obtained with the DLV11-KA EIA to 20 mA converter option. The serial lines will not support the reader run function of the DLV11-KA option. The serial lines provide error indicator bits for overrun error, frame error, and parity error, but do not have modem controls. Serial line 1 may be configured to respond to a break signal. The serial lines have signal level interrupt logic and should be placed after multi-level devices on an LSI-11/23 system. Serial line 1 may be used as a console port, or, along with serial line 0, may be used with any of several standard types of serial communication devices. The 60 Hz clock signal can be selected by a wirewrap jumper to provide line-time clock interrupts on the bus.

Peripherals

LAV11

The LAV11 option consists of an LA180 DECprinter, an interface module, and a BC11S-25 interface cable. The interface module provides interconnection between the LA180 DECprinter and the LSI-11 bus. The module outputs ASCII characters to the printer and monitors various printer operations that require operator control.

LPV11

The LPV11 printer option consists of an interface module, an interface cable, and either an LP05 or LA180 line printer. The interface module provides programmed control of data transfers and provides printer strobe signals appropriate for either printer. The LA180 DECprinter is a high-speed printer that prints 180 characters per second and the LP05 printer can print 240 or 300 lines per minute, depending on which model is selected.

RKV11-D

The RKV11-D option consists of an RK05 disk drive controller, an LSI-11 bus interface module, and an RK05J disk drive. The RK05 disk drive controller can be used with up to eight RK05J disk drive units to form a mass memory storage system that contains up to 21M bytes of storage. The RKV11-D system is block-oriented but is capable of transferring from 1 to 2^{16} consecutive data words without reinitiation or processor intervention. The data transfers occur from the RKV11-D to the system memory by direct memory access (DMA) and operate at maximum bus bandwidth. The system can use either RK05J or RK05F disk drives and the controller can be mounted in a standard 48.3 cm (19 in.) cabinet.

RLV11

The RLV11 option interfaces the LSI-11 bus with an RL01 disk drive controller and an RL01 disk drive assembly. The controller can only be used in an H9273-A type backplane which incorporates an LSI-11 bus in slots A and B, with an interboard bus in slots C and D. The controller can interface up to four RL01 disk drives for a complete system of 21M bytes of storage. The RL01 disk drive is a random access, mass storage system that stores data in fixed length blocks on a preformatted disk cartridge. Each drive can store up to 5.24 million bytes and the complete system can store up to 21 million bytes. The RLV11 transfers data using direct memory access (DMA) techniques; this allows data transfers without processor intervention and at bus bandwidth speed.

RXV11

The RXV11 option consists of an interface module, cable assembly, and either a single or dual drive RX01 floppy disk. This option is a random access mass storage device that stores data in fixed-length blocks on a preformatted flexible diskette. Each diskette can store and retrieve up to 256K, 8-bit bytes of data. The RXV11 system is rack mountable in the standard 48.3 cm (19 in.) cabinet.

RXV21

The RXV21 floppy disk option is a random access mass memory device that stores data in fixed-length blocks on a preformatted, flexible diskette. Each

diskette can store and retrieve up to 512K 8-bit bytes of data. The RXV21 system is rack-mountable and consists of an interface module, an interface cable, and either a single or dual RX02 floppy disk drive. The interface module converts the RX02 I/O bus to the LSI-11 bus structure. It controls the RX02 interrupts to the processor, decodes device addresses for register selection, and handles the data interchange between the RX02 and the processor via DMA transfers. Power for the interface module is supplied by the LSI-11 bus.

TU58

The TU58 is a low-cost intelligent mass memory device that offers random access to block-formatted data on pocket-size cartridge media. It is ideal as a small computer systems device, as inexpensive archive mass storage, or as a software update distribution medium. A dual drive TU58 offers 512 Kb of storage space, making it one of the lowest cost complete mass storage subsystems available. For mounting flexibility, the TU58 is offered both as a component level subsystem and as a fully powered 5½" rack-mount subsystem.

VK170-CA

The VK170 module forms an integral part of a terminal. The module accepts serial ASCII encoded data to be stored in a refresh memory to generate a display for a video monitor. The VK170 also accepts parallel data from a keyboard (on strobe demand) to generate serial ASCII output. The VK170 is an extended-length, double-height, single-width board. Mounting holes are provided for stand-off mounting via handle rivets and two holes located near the module fingers.

INTRODUCTION

Backplanes

The four backplane options available for the LSI-11 bus are presented in the following paragraphs.

H9270	A 4 × 4 (four rows of four slots each) backplane with card guide assembly. LSI-11 bus in rows A-B and C-D. Accepts 8 double-height modules or 4 quad-height modules or combinations of both.
H9273-A	A 9 × 4 (nine rows of four slots each) backplane with card guide assembly. LSI-11 bus in rows A-B only. Special interconnect bus in rows C-D.A ccepts double-height or quad-height modules.
H9281	A 2-slot backplane available in 4-, 8-, or 12-slot options. Accepts double-height modules only.
DDV11-B	A 9 × 6 (nine rows of six slots each) backplane. LSI-11 bus in rows A-B and C-D. Rows E-F are unbussed except for +5V and ground. Accepts 18 double-height or 9 quad-height modules or combinations of both.

Enclosures

H909-C	A 13.3 cm (5.25 in.) high, 48.3 cm (19 in.) wide enclosure which can be mounted in a 48.3 cm (19 in.) rack or as a stand-alone. Accommodates the DDV11-B backplane or a 9 × 6 system mounting unit or houses non-standard mounting arrangement. Includes cooling fan, cord guide, cable restraints, front bezel, and connector block.
BA11-M	A 8.9 cm (3.5 in.) high , 48.3 cm (19 in.) wide expansion box which can be mounted in 48.3 cm (19 in.) rack. Includes H9270 backplane, H780 power supply, blank front panel or bezel, and cooling fan.
BA11-N	A 13.2 cm (5.19 in.) high, 48.3 cm (19 in.) wide mounting box which can be mounted in a 48.3 cm (19 in.) rack. Includes H9273-A backplane, H786 power supply, H403-A ac input panel, blank front panel or bezel, and cooling fan.

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BA11-VA — The BA11-VA is a small form-factor package providing mounting space and power for four LSI-11/2 or LSI-11/23 family modules. This package, plus the high functionality of DIGITAL's microcomputer products, allows LSI-11 microcomputer applications to be implemented within a space smaller than that required for many 8-bit systems.

Cabinets

H984-B — A low-profile cabinet with four casters. Provides mounting space for standard 48.3 cm (19 in.) panels and enclosures in rack at front or rear. Includes distribution panel (115 Vac, 230 Vac)

H9800-A — A low-profile system desk with casters. Provides mounting space for standard 48.3 cm (19 in.) panels and enclosures. Includes distribution panel (115 Vac, 230 Vac)

Power Supplies

H780 — Provides +5V ±4%, 18 A (max) and +12V ± 3%, 3.5 A (max) at 110 Vac and features line-time clock, and power-fail/automatic restart. Available primary power of 115 or 230 Vac and with or without master and slave console.

Cables and Connectors

Various preassembled cables in different lengths are available for use with interface and communications options. See Appendix C for commonly used cables.

Wire-Wrappable Modules

W9500 Series: LSI-11 Bus-Compatible Wire-Wrappable Modules (W9511, W9512, W9514 AND W9515) — The LSI-11 bus-compatible wire-wrappable modules consist of quad-height and double-height modules. Two LSI-11 bus-compatible modules are available without DIP sockets.

W9511 — Quad-height, extended-length, single-width module with extractor handle. No DIP sockets included. One 40-pin male cable connector premounted on board and space for additional 40-pin connector provided.

	Power and ground connections are V—AA2, BA2, CA2, DA2 GND—AT1, BT1, CT1, DT1, AC2, BC2, CC2, DC2
W9514	Same as W9511 except with 58 pre-mounted DIP sockets. Power and ground connections are the same as W9511
W9512	Double-height, extended-length, single-width module with Flip-Chip handle. No DIP sockets included. One 40-pin male connector premounted on board. Power and ground connections are GND—AT1, BT1,AC2, BC2
W9515	Same as W9512 except with 25 pre-mounted DIP sockets. Power and ground connections are the same as W9512

Integrated Circuits

DCK11-AA, -AC	The DCK11-AA and -AC CHIPKITs provide the logic necessary for a program transfer interface to the LSI-11 bus. The DCK11-AA kit contains one DC003 Interrupt Chip, one DC004 Protocol Chip, and four DC005 Transceiver/Address Decoder/Vector Select Chips. The DCK11-AC kit contains previous chips plus one W9512 double-height, extended length, high-density wire-wrappable module and one BC07D-10 ten-foot, 40-connector plug-in cable.
DCK11-AB, -AD	The DCK11-AB and -AD CHIPKITs provide the logic necessary for a Direct Memory Access (DMA) interface to the LSI-11 bus. The DCK11-AB. The DCK11-AB kit contains one DC003 Interrupt Chip, one DC004 Protocol Chip, four DC005 Transceiver/Address Decoder/Vector Select Chips, two DC006 Word Count/Bus Address Chips, and one DC010 DMA Control Chip. The DCK11-AD kit contains the previous chips plus one W9512 double-height, extended-length, high-density wire-wrappa-

ble module and one BC07D-10 ten-foot, 40-connector plug-in cable. DMA applications use the same chips as program control interfaces, plus two DC006s for word or byte address counters and a DC010 DMA bus control IC.

Miscellaneous Options

BDV11

The BDV11 module has 2K words of read-only memory (ROM) that contains diagnostic and bootstrap programs. These programs are user-selectable by setting dip switches. The diagnostic programs will test the processor, the memory, and the user's console. The bootstrap programs can boot most LSI-11 peripheral devices. The module also has 120-ohm bus terminator circuits.

The user can add up to 16K of read-only memory (ROM) and up to 2K words of erasable programmable ROM (EPROM) on the module. This 18K words of additional memory can be used with no increase in the amount of I/O address space.

KPV11-A, -B, -C

The KPV11-A module generates power-up and power-down sequences, monitors for a power-fail condition, and generates the line-time clock (LTC) function. The KPV11-B is the same as the "A" except that it provides 120-ohm termination circuits. The KPV11-C is the same as the "A" except that it provides 220-ohm termination circuits. The module can be installed on any backplane or remotely installed via an optional cable.

REV11-A, -C

The REV11-C module has a bootstrap ROM and direct memory access (DMA) refresh circuits. The REV11-A is identical to the REV11-C except it has additional 120-ohm termination circuits.

TEV11

The TEV11 is a bus terminator module that provides 120-ohm bus termination circuits.

Table 1 Module Specifications

Option Desig.	Module No(s).	Description	Power Requirements + 5V ±5%	Power Requirements + 12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
AAV11-A	A6001	4-channel, 12-bit D/A converter	1.5 A	0.4 A	1.9	1	Quad
ADV11-A	A012	16-channel, 12-bit A/D converter	2.0 A	0.45 A	3.25	1	Quad
BDV11	M8012	Bootstrap, terminator, diagnostic	1.6 A	0.07 A	2.0	1	Quad
DDV11-B		6 × 9 backplane			6.4	0	
DLV11	M7940	Asynchronous serial line interface	1.0 A	0.18 A	2.5	1	Double
DLV11-E	M8017	Asynchronous line interface	1.0 A	0.18 A	1.6	1	Double
DLV11-F	M8028	Asynchronous line interface	1.0 A	0.18A	2.2	1	Double
DLV11-J	M8043	4 asynchronous serial interfaces	1.0 A	0.25 A	1	1	Double

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 1 Module Specifications

Option Desig.	Module No(s).	Description	Power Requirements + 5V ±5%	Power Requirements + 12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
DRV11	M7941	Parallel line unit interface	0.9 A	-	1.4	1	Double
DRV11-B	M7950	DMA interface	1.9 A	-	3.3	1	Quad
DRV11-J	M8049	64-line parallel I/O	1.6A	1.8A	2.0	1	Double
DRV11-P	M7948	Foundation module	1.0 A + user logic	-	2.1	1	Quad
DUV11	M7951	Synchronous serial line interface	0.86 A	0.32	1.00	1	Quad
DZV11	M7957	Asynchronous line interface	1.15 A	0.39 A	3.95	1	Quad
H9270		4 X 4 backplane			5.1	0	
H9273		4 X 9 backplane			2.6	0	
H9281A		2 X 4 backplane			1.3	0	
H9281B		2 X 8 backplane			2.4	0	

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 1 Module Specifications

Option Desig.	Module No(s).	Description	Power Requirements + 5V ±5%	Power Requirements + 12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
H9281C		2 × 12 backplane			3.6	0	
IBV11-A	M7954	Instrument bus interface	0.8 A	—	1.9	1	Double
KD11-F	M7264	LSI-11 CPU with 4K RAM	1.8A	0.8A	2.4	1	Quad
KD11-H	M7264-YA	LSI-11 CPU without RAM	1.6A	0.25A	2.4	1	Quad
KD11-HA	M7270	LSI-11/2 CPU	1.0A	0.22A	1.7	1	Double
KDF-11	M8186	LSI-11/23 CPU	2.0A	0.2A	2.0	1	Double
KPV11-A	M8016	Power-fail/line-time clock	0.56 A	—	1.63	1	Double
KPV11-B	M8016-YB	Power-fail/line-time clock/120 Ω bus terminator	0.56 A	—	1.63	1	Double

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 1 Module Specifications

Option Desig.	Module No(s).	Description	Power Requirements + 5V ±5%	Power Requirements + 12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
KPV11-C	M8016-YC	Power-fail/line-time clock/220 Ω bus terminator	0.56 A	—	1.63	1	Double
KUV-11	M8018	WCS module	3.0A			1	Quad
KWV11-A	M7952	Programmable real-time clock	1.75A	0.01A	3.4	1	Quad
LAV11	M7949	LA180 line printer interface	0.8 A	—	1.8	1	Double
LPV11	M8027	LA180/LP05 printer interface	0.8 A	—	1.4	1	Double
MMV11-A	G653	4K X 16 core memory		1.91	1	2	Quads
		(standby current)	3.0 A	0.2 A			
		(operating current)	7.0 A	0.6 A			
MRV11-AA	M7942	4K X 16 read-only memory (less PROM integrated circuits)	0.4 AA	—	1.8	1	Double

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 1 Module Specifications

Option Desig.	Module No(s).	Description	Power Requirements + 5V ±5%	+ 12V ±3%	Bus Loads* AC(Max)	DC	Size
		(with 32 512 X 4 PROM integrated circuts) (MRV11-AC)	2.8 A				
MRV11-BA	M8021	UV PROM-RAM (less PROM integrated circuits)	0.58 A	0.34 A	2.8	1	Double
		(with 8 1K X 8 PROM integrated circuits) (MRV11-BC)	0.62 A	0.5 A			
MRV11-C	M8048	PROM/ROM module	0.8A		2.0	1	Double
MSV11-B	M7944	4K X 16 read/write MOS memory	0.6 A	0.54 A	1.9	1	Double
MSV11-CD	M7955-YD	16K X 16 read/write MOS memory	1.1 A	0.54 A	2.3	1	Quad

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 1 Module Specifications

Option Desig.	Module No(s).	Description	Power Requirements + 5V ±5%	Power Requirements + 12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
MSV11-D	M8044	4K/16K/32K MOS memory	1.7 A	0.34 A	2.0	1	Double
MSV11-E	M8045	4K/16K/32K MOS memory	2.0 A	0.41 A	2.0	1	Double
MXV11-A	M8047	Multifunction module	1.2A	0.1A	2.0	2	Double
REV11-A	M9400-YA	120 Ω terminator, DMA refresh, bootstrap ROM	1.6 A	—	2.2	1	Double
REV11-C	M9400-YC	DMA refresh, bootstrap	1.6 A	—	2.2	1	Double
RKV11-D	M7269	LSI-11 Bus control for RKV11-D	1.8 A	—	1.9	1	Double
RLV11	M8013 M8014	RL01 disk drive	6.5 A	1.0 A	3.2	1	2 Quads

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 1 Module Specifications

Option Desig.	Module No(s).	Description	Power Requirements + 5V ±5%	Power Requirements + 12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
RXV11	M7946	RX01 interface	1.5 A	—	1.8	1	Double
RXV21	N8029	Double density floppy interface	1.1A		2.0	1	Doublel
TEV11	M9400-YB	120 Ω terminator	0.5 A	—	0	0	Double
TU58		Serial/cartridge cassette	0.75 Appr.	1.2A max			
VK170	CAM7142	Serial video module	1.2A	0.15			Double

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

INTRODUCTION

CONFIGURATION

The LSI-11 bus permits a unified addressing structure in which control/status and data registers for peripheral devices are directly addressed as memory locations. All operations on these registers, such as transferring informaton to or from them or manipulating data within them, are performed by normal memory address instructions. The use of memory address instructions on peripheral device registers greatly increases the flexibility of input/output communications.

Addresses

All the options except memories have at least one control and status register and may have several data registers. Each register is assigned an address through which the option can communicate with the processor. The upper 4K of memory address space is reserved for the processor and external input/output (I/O) registers. The user can select any address (Appendix A) in the range of 160000 through 177776 and assign it to the option interface module. The modules are configured to the desired address by selecting dip switches, connecting or disconnecting wire-wrap pins, or installing or removing wired jumpers on the module.

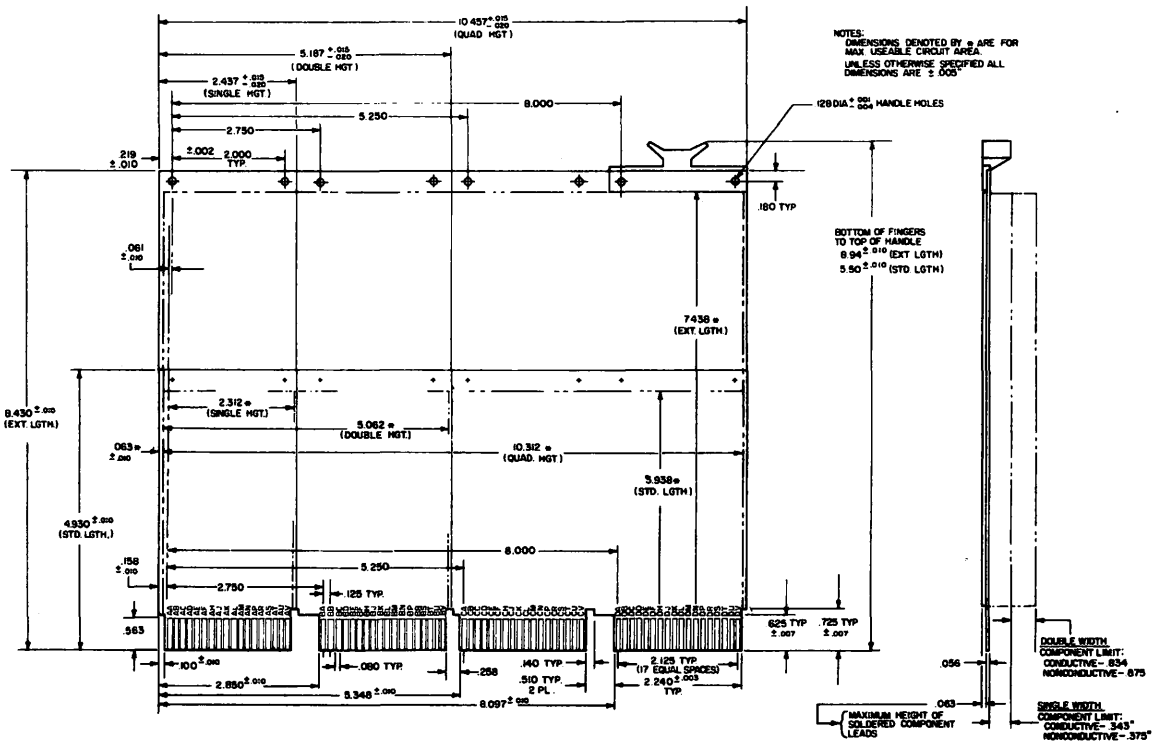


Figure 1 Module Dimensions

Control and Status Registers

The general form for the control and status registers, shown in Figure 2, does not necessarily apply to every device, but is presented as a guide.

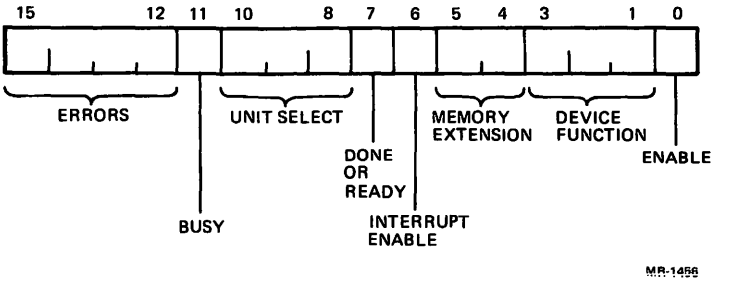


Figure 2 Control and Status Registers

Many devices require less than 16 status bits. Other devices will require more than 16 and therefore will require additional status and control registers.

The bits in the control and status registers are generally assigned as described below.

Typical Control and Status Register

Bit: 15-12 **Name:** Errors
Function: Generally there is an individual bit associated with a specific error. When more bits are required for errors, they can be obtained by expanding the error section in the word or by using another status word. Generally bit 15 is the inclusive-OR of all other error bits (if there is more than one). Most devices will have "hard" error conditions which will cause an interrupt if bit 6 is set. Some may also have "soft" errors (warning types) which do not cause immediate interrupts.

Bit: 11 **Name:** Busy
Function: Set to indicate that a device operation is being performed.

Bit: 10-8 **Name:** Unit Select
Function: Some peripheral systems have more than one device per control. For example, a disk system can have multiple surfaces per control and an analog-to-digital converter can have multiple channels. The unit bits select the proper surface or channel.

Bit: 7 **Name:** Done or Ready
Function: The register can contain a done bit, a ready bit or a done-busy pair of bits, depending on the device. These bits are set and cleared by the peripheral device, but may be queried by the program to determine the availability of the device.

Bit: 6 **Name:** Interrupt Enable
Function: Set by the program to allow an interrupt to occur as a result of a function done or error condition.

Bit: 5-4 **Name:** Memory Extension
Function: Allows devices to use a full 18 bits to specify addresses on the bus.

Bit: 3-1 **Name:** Device Function Bits
Function: Specifies the operation that a device is to perform.

Bit: 0 **Name:** Enable
Function: Set to enable the device to perform an operation.

Data Buffer Registers
The data buffer register is used for temporarily storing data to be transferred into or out of the computer. The number and type of data registers is a function of the device.

Interrupts
Interrupts are requests, made by peripheral devices, which cause the processor to temporarily suspend its present (background) program execution to service the requesting device. Each device that is capable of requesting an interrupt must have a user-supplied service routine that is automatically entered when the processor acknowledges the interrupt request. After completing the service routine execution, program control is returned to the interrupted program. This type of operation is especially useful for the slower peripheral devices.

A device can interrupt the processor only when interrupts are enabled and services interrupts only when the appropriate PSW bits are cleared. Device priority is highest for devices electrically closest to the processor along the bus. Any device that can interrupt the processor can also interrupt the service routine execution of a lower priority device if the processor's priority is set during the execution; hence, interrupt nesting to any level is possible with this interrupt structure. Each device normally contains a control/status register (CSR), which includes an interrupt enable bit. A program must set this bit before an interrupt can be generated by the device.

Interrupt Vectors

An interrupt vector associated with each device is hard-wired into the devices's interface/control logic. This vector is an address pointer that is transmitted to the processor duing the interrupt acknowledge sequence, allowing automatic entry into the service routine without device polling. The user can select an interrupt vector from the range of 000 to 777 for any interrupting options. The module can be configured to the desired interrupt vector by either selecting dip switches, connecting or disconnecting wire-wrap pins, or installing or removing wired jumpers on the module.

part 2

the interfaces

AAV11-A

AAV11-A 4-CHANNEL 12-BIT D/A CONVERTER

GENERAL

The AAV11-A is a 4-channel, digital-to-analog converter module that includes control and interfacing circuits. It has four D/A converters, a dc-dc converter that provides power to the analog circuits, and a precision voltage reference. Each channel has its own holding register that can be addressed separately and provides 12 bits of resolution. These registers can be written and read, using either word or byte format. In addition, bits 0, 1, 2, and 3 of the fourth holding register are brought out to the I/O connector so they can be used as a 4-bit digital output register.

FEATURES

- Four 12-bit digital input channels, binary encoded for either unipolar mode or bipolar mode.
- Jumper-selected output ranges and modes:
  Bipolar mode ±2.56 V, ±5.12 V, ±10.24 V
  Unipolar mode 0 to +5.12 V, 0 to +10.24 V
- One part in 4096 resolution
- 5V/μs slew rate
- ±5 mA drive capability per converter

SPECIFICATIONS

Identification	A6001
Size	Quad
Power	+5.0 Vdc ±5% at 1.5 A +12.0 Vdc ±3% at 0.4 A
Bus loads	
AC	1.9
DC	1.0
Resolution	12-bits (1 part in 4096)
Number of D/A converters	4
Digital input	12-bits (binary encoded for unipolar mode; offset binary encoded for bipolar mode)
Digital storage	Read/write, word or byte operable, single buffered

AAV11-A

Output voltage range (jumper selected)	±2.56 V, ±5.12 V, ±10.24 V bipolar, 0 V to +5.12 V, 0 V to +10.24 V unipolar
Gain accuracy	Adjustable (factory set for bipolar ±5.12 V)
Gain temperature coefficient	10 PPM per °C, max.
Offset temperature coefficient	20 PPM of full scale range per °C, max.
Linearity	±½ LSB max, non-linearity
Differential linearity	±½ LSB, monotonic
Output impedance	1 ohm max.
Drive capability	±6 mA max. per converter
Slewing speed	5 V/μs
Rise and settling time (to 0.1% of final value)	4 μs (8 μs wth 5000 pF load in parallel with 1 kΩ

DESCRIPTION

General

The function of the AAV11-A module is to convert digital data input to an analog dc voltage output that is representative of the input. This is accomplished by the bus interface, the control logic, and the D/A converter functions as shown in Figure 1.

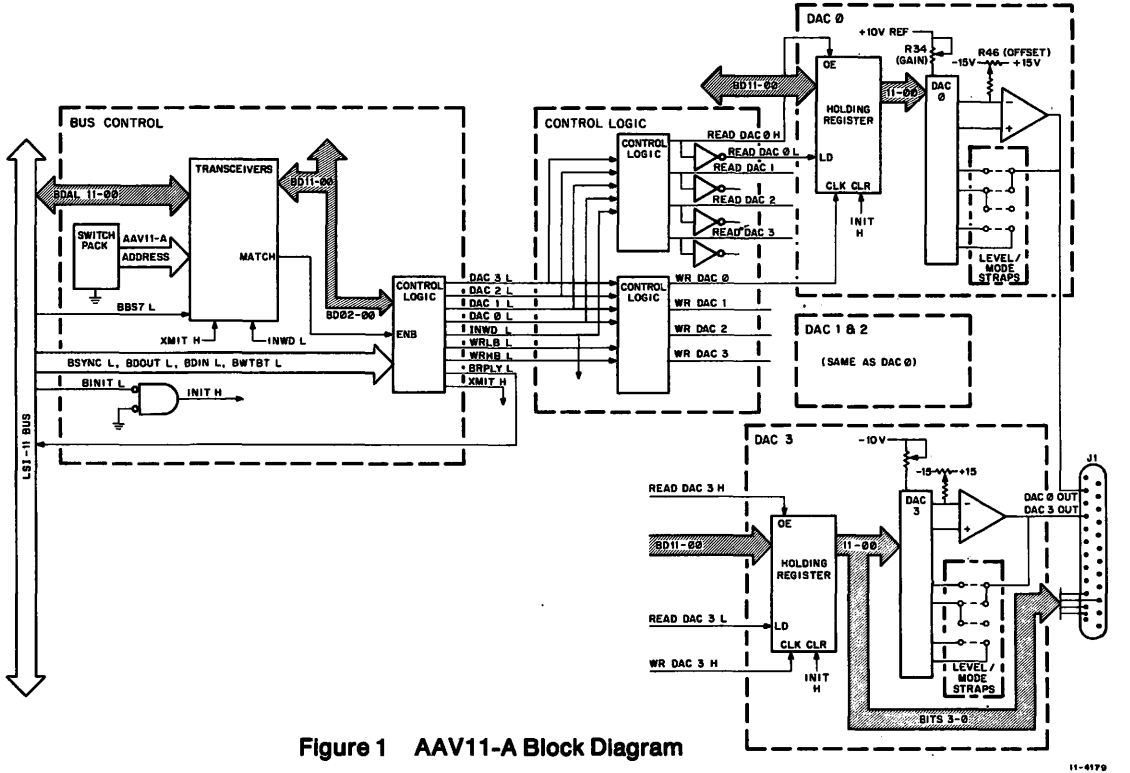


Figure 1 AAV11-A Block Diagram

Bus Interface

The logic associated with the bus interface section maintains proper communications protocol between the processor LSI-11 bus and the AAV11-A. This logic generates and monitors the bus signals involved during data transfers between the processor and the AAV11-A, permitting the AAV11-A to recognize when it is being addressed by the processor (address defined by setting on the address switch pack) to accept input data from the processor, and to output data to the processor.

Control Logic

The AAV11-A has no control/status register. The four digital-to-analog converters continually generate voltages at their outputs that reflect whatever digital values have most recently been written into their respective holding registers. The role of the control logic is to make the necessary discriminations between requests to change the state of the holding registers (i.e., to *write* into the holding registers), and requests to put the holding register contents onto the BD lines where they can be picked up through the transceivers by the processor.

DACs 0, 1, and 2

Digital-to-analog conversion functions are performed in each of the four AAV11-A channels by identical circuits:

- a holding register which stores the digital value output by the processor
- a digital-to-analog converter (DAC) proper which generates a current that is a function of the holding register value and of the mode/level jumper conditions
- an amplifier that translates the current into a proportional voltage, provides a low output impedance for the channel, and permits adjustment of signal offset

DAC 3

DAC 3 is identical to DACs 0, 1, and 2 except that holding register bits 0-3 are routed to the I/O connector as well as to the DAC. This arrangement permits these bits to be routed to external equipment that requires binary control signals at programmable intervals. Control data in these bit positions affects any 12-bit D/A conversion that they coincide with, but since they involve the least significant bits of the word, the worst-case error is less than 0.5 percent. Consequently, DAC 3 can be used as a 12-bit DAC or as an 8-bit DAC plus four output bits for CRT Intensify, Store, Non-Store, Erase, etc.

CONFIGURATION

General

This section describes how the user can configure the module to function within his system by setting dip switches (Figure 2) to obtain the desired device address. The voltage range for each D/A converter (DAC 0—DAC 3) can be configured independently by installing or removing the designated jumpers (Figure 2) associated with a specific D/A converter. This section also describes how to connect external devices to the module. The standard factory addresses for the registers are listed in Table 1.

Table 1 Standard Addresses

Register	Mnemonic	Address
Holding 0	DAC 0	170440
Holding 1	DAC 1	170442
Holding 2	DAC 2	170444
Holding 3	DAC 3	170446

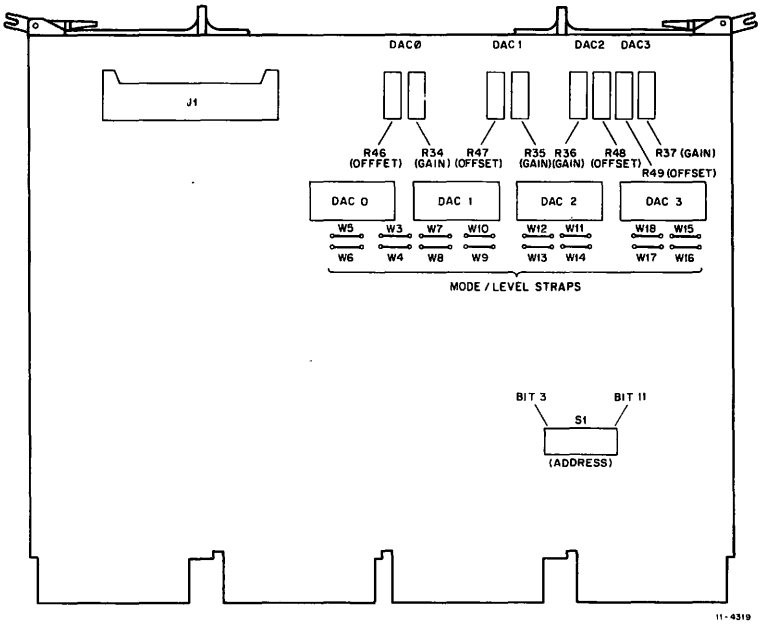


Figure 2 AAV11-A Connectors, Switches, and Jumpers

Device Registers

The device registers can be configured to respond to any address within the range 170000 to 177777. Each register address does not have to be individually set. The DAC 0 register address is selectable and the last digit will be zero. The remaining registers will use addresses 17XXX2, 17XXX4, and 17XXX6 for DAC 1, DAC 2, and DAC 3 registers, respectively. The factory-configured device address is 170440 as shown in Figure 3. The word formats for the DAC registers are described in Table 2. Note that all device registers are always a sequence of four consecutive even locations. There is no vector used for this module.

D/A Converter Range and Mode

The range and mode (bipolar or unipolar) voltages can be selected by the user inserting or removing jumpers as shown in Figure 2. Four jumpers are associated with each D/A converter. The module is facto-

ry-configured for −5.12 to +5.12 V bipolar operation. The jumper configuations for the bipolar mode ranges are shown in Table 3; the unipolar ranges are shown in Table 4.

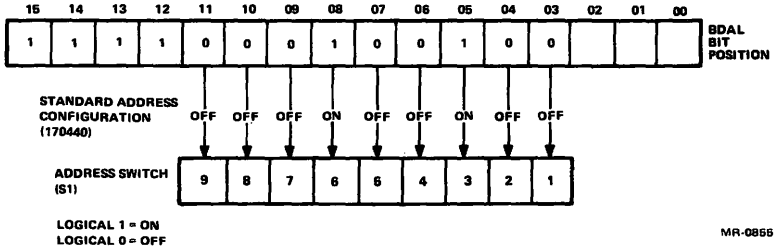


Figure 3 Address Selection

Table 2 DAC Word Formats

Bit	DAC 0, DAC 1, DAC 2	DAC 3
15-12	Not used	Not used
11	Binary 11	Binary 11
10	Binary 10	Binary 10
9	Binary 9	Binary 9
8	Binary 8	Binary 8
7	Binary 7	Binary 7
6	Binary 6	Binary 5
5	Binary 5	Binary 5
4	Binary 4	Binary 4
3	Binary 3	Binary 3/Control 3
2	Binary 2	Binary 2/Control 2
1	Binary 1	Binary 1/Control 1
0	Binary 0	Binary 0/Control 0

Table 3 Jumper Configurations for Bipolar Operation

	±2.56 V	±5.12 V	±10.24 V
DAC 1			
W3	IN	IN	OUT
W4	OUT	OUT	IN
W5	IN	OUT	OUT
W6	IN	IN	IN
DAC 2			
W7	IN	IN	OUT
W8	OUT	OUT	IN
W9	IN	OUT	OUT
W10	IN	IN	IN
DAC 3			
W11	IN	IN	OUT
W12	OUT	OUT	IN
W13	IN	OUT	OUT
W14	IN	IN	IN
DAC 4			
W15	IN	IN	OUT
W16	OUT	OUT	IN
W17	IN	OUT	OUT
W18	IN	IN	IN

Table 4 Jumper Configurations for Unipolar Operation

	0 V—+5.12 V	0 V—+10.24 V
DAC 1		
W3	IN	IN
W4	OUT	OUT
W5	IN	OUT
W6	OUT	OUT
DAC 2		
W7	IN	IN
W8	OUT	OUT
W9	IN	OUT
W10	OUT	OUT
DAC 3		
W11	IN	IN
W12	OUT	OUT
W13	IN	OUT
W14	OUT	OUT
DAC 4		
W15	IN	IN
W16	OUT	OUT
W17	IN	OUT
W18	OUT	OUT

J1 Output Connections

Analog output devices such as oscilloscopes may be either grounded or floating. If the oscilloscope is grounded, either through its power plug or through contact between its chassis and a grounded cabinet, the oscilloscope ground should not be connected to any of the AAV11-A ground pins. Doing so may result in a ground loop which will adversely affect oscilloscope control results as well as ADV11-A operation (if used). If the oscilloscope is floating, its ground should be con-

nected to the AAV11-A logic ground, J1 pins L, N, R, or T. Note that the foregoing assumes that the LSI-11 power suppy ground is connected to power line (earth) ground. If continuity checks reveal no such connection, attach a length of 12-gauge wire between the power supply ground and a convenient point associated with earth ground.

Oscilloscope X and Y inputs may be either differential or single-ended. Differential inputs should be driven as in Figure 4.

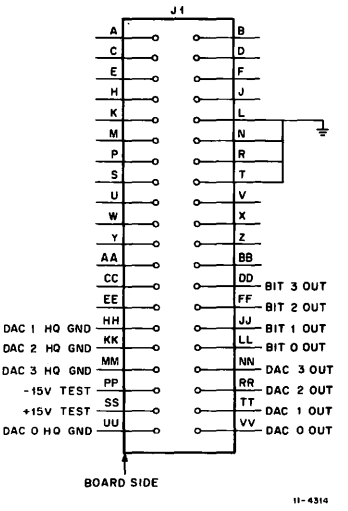


Figure 4 Connection to Oscilloscope with Differential Input

When oscilloscopes with single-ended inputs are involved, the AAV11-A analog grounds (pins UU and HH) are not used. The return path for X and Y signal currents is through ground for a grounded oscilloscope or through logic ground (pins L, N, R, or T) for a floating oscilloscope. Since the grounded, single-ended oscilloscope receives an input voltage which is the sum of the AAV11-A output and the ground difference voltage between the oscilloscope and the AAV11-A, noise and line frequency errors may be minimized by plugging the oscilloscope into an ac socket as close as possible to the LSI-11 system. Running single-ended oscilloscopes in a floating configuration will eliminate noise

and line frequency errors which are due to ground voltage differences.

The effect of magnetic coupling into the oscilloscope input lines can be minimized for a differential-input oscilloscope by running the AAV11-A output and its return line in a twisted pair. No benefit is derived from a twisted pair with a single-ended oscilloscope input.

The effect of electrostatic coupling into the oscilloscope input lines can be minimized by shielding the input lines from AAV11-A to the oscilloscope. The shield should be connected to ground at one end only. Grounding the shield at both ends may result in a ground loop which will adversely affect oscilloscope control results and any ADV11-A A/D operations (if used).

Careful selection of cabling is essential. The D/A outputs are capable of driving a maximum of 5000 pF. Output impedance is 1 ohm. Output current limit is 5 mA.

Optional Equipment

Figure 5 illustrates the H854 40-pin connector pin assignments for user outputs. These pins may be connected to the optional H322 distribution panel for convenient user access via an optional BCO8R cable. The optional BCO4Z is available for applications which require an unterminated cable. One end is terminated with an H856 connector that mates with the H854 connector on the AAV11-A module. The other end is an unterminated ribbon cable. The BCO4Z cable is available in lengths of 3.05 m (10 ft), 4.5 m (15 ft), and 7.6 m (25 ft).

PROGRAMMING

All four DAC holding registers are automatically set to zero on system initialization. This produces −5.12 V at the DAC outputs when the mode/level jumpers are connected as delivered from the factory. Any holding register value remains in effect until changed by the processor in response to a program instruction. Coding to the D/A converters is offset binary for bipolar operation and straight binary for unipolar operation. Offset binary defines 0 as maximum negative voltage, midpoint (i.e., 4000_8 for the 12-bit AAV11-A) as 0 V, and all 1s (7777_8) as maximum positive voltage. These relationships are illustrated in Table 5.

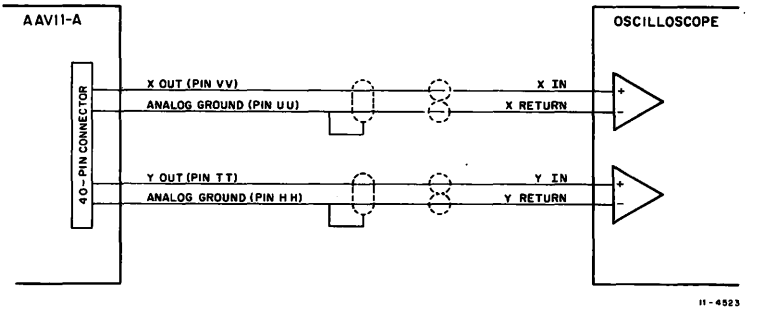


Figure 5 J1 Connector Pin Assignments

Table 5 AAV11-A Digital-to-Analog Conversions*

Input Code (octal)	Bipolar ±2.56 V (volts)	Bipolar ±5.12 V (volts)	Bipolar ±10.24 V (volts)	Unipolar 0 V to +5.12 V (volts)	Unipolar 0 V to +10.24 V (volts)
0000	−2.56	−5.12	−10.24	+0.0	+0.0
0001	−2.55875	−5.1175	−10.235	+0.00125	+0.025
3777**	−0.00125	−0.0025	−0.005	+2.55875	+5.1175
4000	0.0	0.0	0.0	+2.56	+5.12
4001	+0.00125	+0.0025	+0.005	+2.56125	+5.1225
7777	+2.55875	+5.1175	+10.235	+5.11875	+10.2375

* Offset binary for bipolar, straight binary for unipolar operating modes. Conversions may be made between 2's complement signed binary and offset binary numbers by subtracting 4000_8 from the 2's complement number (or adding 4000_8 to the offset binary number) and using only the low-order 12 bits of the result.

** Note that in all ranges, actual maximum positive voltage output is 1 LSB less than nominal maximum positive output.

ADV11-A ANALOG TO DIGITAL CONVERTER

GENERAL

The ADV11-A is a 12-bit successive approximation analog-to-digital converter that samples analog data at specified rates and stores the digital equivalent value for processing. A multiplexer section can accommodate up to 16 single-ended or 8 quasi-differential inputs. The converter section uses a patented auto-zeroing design that measures the sample data with respect to its own circuitry offset and therefore cancels out its own offset error.

A/D conversions are initiated by program command, clock overflow, or external events. The program control is determined by the control and status register (CSR). The clock overflow command is supplied by the KWV11-A option. External event inputs can originate at the user's equipment or from the Schmitt trigger output on the KWV11-A clock. The digital data output is routed through a buffer register to the bus, from which it can be transferred into memory. This buffer optimizes the throughput rate of the converter.

Three reference signals are provided for self-testing on any channel input: two dc levels and one bipolar triangular waveform. This output can be used with DIGITAL diagnostic software to produce a data base for extremely thorough and precise analog linearity testing.

FEATURES

- 16-channel multiplexer
- Sample-and-hold functions
- Auto-zeroing technique
- Buffered data output
- Self-testing features

SPECIFICATIONS

Identification	A012
Type	Quad
Power	+5 Vdc ±5% at 2.0 A +12 Vdc ±3% at 450 mA
Bus Loads	
AC	3.25
DC	1

ADV11-A

Inputs	
Analog input protection	Fusible resistor guaranteed to open at ±85 V within 6.25 seconds. Guaranteed not to open from −25 V to +20 V at the input. Overload affects no components other than the fusible resistor on the overloaded channel; no other channels are affected.
Logic input protection	Fusible resistor guaranteed to open at ±25 V within 6.25 seconds. Guaranteed not to open from −4 V to +9 V at the input.
Analog input full scale range (FSR)	10.24 V bipolar (−5.12 V to +5.12 V)
Analog input dynamic resistance (Vin ≤ 5.12 V)	100 MΩ minimum
Analog input bias current (Vin ≤ 5.12 V)	50 nA, maximum
Logic input voltages	Low = 0.0 to +0.7 V High = +2 V to +5 V
Logic input currents	Low = −6.8 mA at 0 V High = +1.3 mA at +5 V
Logic input rise/fall time	400 ns maximum
Coding	
A/D Converter	
Resolution	12 bits, binary weighted (2.5 mV nominal)
Format	Parallel offset binary, right justified
	Input Voltage +FS-1 LSB 0 −FS
	Output Code 7777 4000 0

ADV11-A

	(FS = 5.12 V; 1 LSB = 2.5 mV)
Vernier D/A	
Resolution	8 bits, binary weighted
Format	Offset binary encoded
	Input Code 377 200 0 **Approximate Offset Voltage** +2.5 A/D LSB (+6.4 mV) 0 −2.5 A/D LSB (−6.4 mV)
Performance	
Gain error	Adjustable to zero
Offset error	Adjustable to zero
Differential linearity	No skipped states; no states wider than 2 LSB. 99% of state widths ±½ LSB
Integral linearity	±1 LSB, maximum non-linearity (referenced to end points)
Temperature coefficients	Gain = 6 PPM per °C Linearity = 2 PPM of full-scale range per °C Offset = 7.5 PPM of full-scale range per °C
Noise	Module = 0.4 LSB rms; 2 LSB peak System = 0.5 LSB rms; 2 LSB peak
Warm-up time	5 minutes, maximum
Timing	
External start	Low level pulse, 50 ns minimum to 10 μs maximum; conversion starts on leading edge

Synchronization	0 to T
Conversion time	16 T (T = Clock period = 2 μs)
Transition interval (reacquisition interval between end of conversion or channel change and start of new conversion)	9 μs

Test Signals

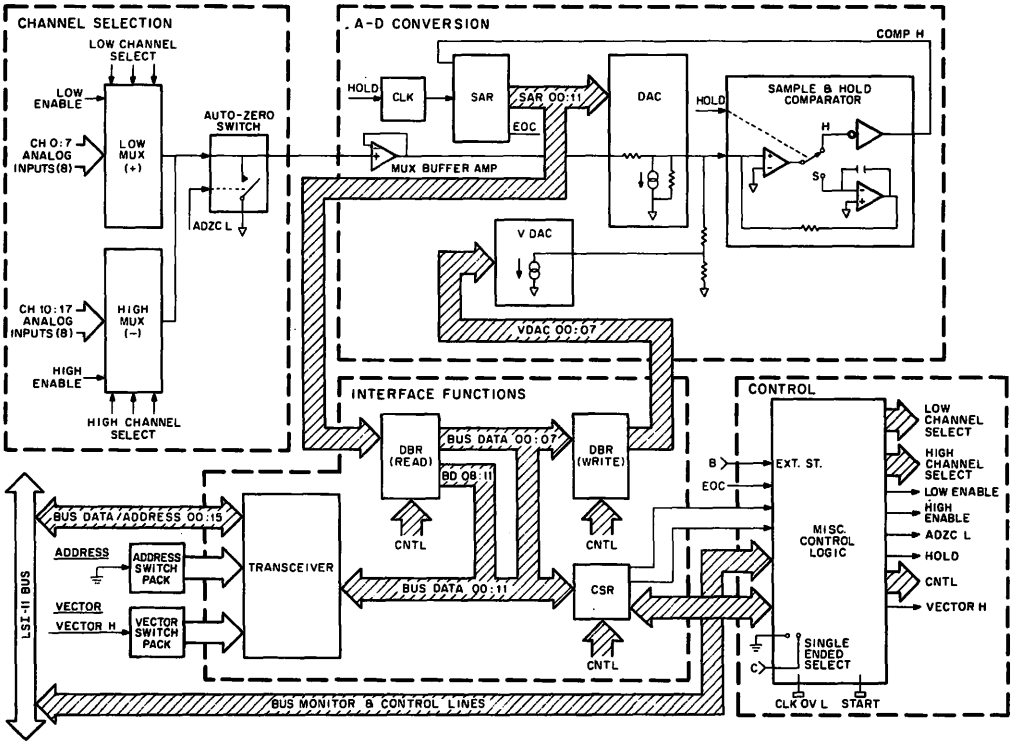
The ADV11-A provides three output voltages for test purposes:

1. Positive dc level, +4.4 V (±15%)
2. Negative dc level, −4.4 V (±15%)
3. Triangular wave, 15 Hz nominal (±15%)

DESCRIPTION

General

The function of the ADV11-A module is to convert analog input data to a 12-bit digital word that is representative of the input. This is done by the channel selection, control logic, A/D converter, and bus interface functions as shown in Figure 1.



11-4165

Figure 1 ADV11-A Functional Block Diagram

Channel Selection

Channel selection is accomplished under program control by two 8-channel multiplexers and is a function of the data asserted in bits 8 through 11 of the control/status register (CSR). Each of the 16 analog input channels is routed to the single output channel through a MOS field-effect transistor which acts as a normally open switch. During the sample interval, the data pattern in CSR bits 8 through 11 selects one of these transistors and causes it to change from a condition of nearly infinite resistance (1 GΩ or more) to one of very low resistance (1000 Ω or less). Since in the selected state the transistor conducts current within the ±5.12 V limits equally well in both directions, it now functions as a closed switch, effectively routing to the output line whatever analog signal is connected to its input.

A/D Conversion

A/D conversion can be initiated in three ways: under program control, on overflow from the KWV11-A real-time clock, or on external input. When a conversion is completed or the control program writes a multiplexer address into the CSR, the control logic initiates the transition interval, a delay of about 9 μs to allow the multiplexer adequate selection and settling time and to permit a valid representation of the signal level to be established in the sample circuit. If no A/D start signal has occurred by the time the transition interval has elapsed, the sample circuit merely follows the signal transmitted to it through the selected multiplexer channel and waits for an A/D start signal. When an A/D start signal occurs—or at the end of the transition interval if A/D start was previously generated by the writing of the CSR GO bit—the sample-and-hold circuits are switched to hold, sustaining the sampled level for the next step. The multiplexer output is then set to its hold condition, i.e., to ground if the single-ended (SE) input is set low for single-ended measurement, or to the second differential input (return line) if the SE input is not set low. Note that if an external or clock start signal occurs during the transition interval, conversion starts immediately, without waiting for the transition interval to be completed. Bit 15 of the CSR (A/D Error) is set, however, and an interrupt is generated if Bit 14 (Error Interrupt Enable) is set—alerting the program that conversions are occurring too fast and are consequently liable to be in error.

Under normal conditions, it is not until the transition interval is complete that the measurement process is begun. The successive approximation register (SAR) is cycled through 13 states by the clock. In the first state, its output code involves only the most significant bit (MSB) of the 12-bit SAR word. This output code causes the feedback digital-

to-analog converter to generate an output equivalent to that produced by the hold circuits in response to a sample voltage of 0. The digital-to-analog converter output is summed with that produced by the hold circuits and with that coming from the grounded multiplexer output (single-ended mode) or from the second differential input (quasi-differential mode). If the current from the summing mode is negative, the first approximation was too low, and the comparator signals the SAR to maintain the state of bit 11 and repeat the process with bit 10. If the current from the summing mode is positive, the first approximation is too high, and the SAR changes the state of bit 11 before cycling to the second approximation. This process continues until all 12 bits in the word have been set, tested, and if necessary, changed. The 13th state (end of conversion, or EOC) indicates that the measurement is complete and that the SAR now contains an offset binary equivalent of the sampled voltage and may therefore be transferred to the processor. EOC causes the sample-and-hold circuits to return to the sample mode and to reset the SAR, preventing further SAR activity until the occurrence of the next hold condition.

Note that because the reference point against which the sample voltage is compared is at the output of the multiplexer itself rather than internal to the sample-and-hold circuits, all offset voltages generated by the intervening circuits are common to both sample-and-hold conditions and are therefore cancelled out of any measurement. In single-ended mode, grounding the multiplexer output (and thereby establishing this reference point) is identified as auto-zeroing the converter.

Bus Interface

In addition to stopping the SAR clock and re-establishing the sample mode, the end-of-conversion signal also initiates the process that causes the SAR data to be transferred to the processor. Since this operation takes a finite amount of time which would interfere with subsequent measuring operations, the SAR data is first transferred to a holding device, the data buffer register (DBR) where it will remain until the processor can be notified to read the conversion data for processing. In the meantime, the channel selection and A/D conversion circuits can begin the next measurement as dictated by control/status register (CSR) bit conditions controlled by the processor.

Included in the ADV11-A interface is an extension of the DBR designed to accept 8-bit write information from the bus data/address lines. This buffer permits programmed setting of the vernier DAC. Also included are transceivers that connect the bidirectional bus data lines to the LSI-11 bus data/address lines. Associated with these transceiv-

ers are switches that let device and vector addresses be assigned to any given ADV11-A.

Control Logic

As the above discussion suggests, a large number of signals must be precisely orchestrated each time the ADV11-A executes a conversion. The control logic contains an assortment of gates, latches, read-only memories, and timing circuits designed to ensure that 1) multiplexer channels are properly selected, 2) sample durations are of adequate length, 3) conversions are not initiated during uncompleted previous conversions. In general, the user need not attend to any but the most elementary details of the conversion process, e.g., making necessary connections to the system and writing control programs that make appropriate use of the CSR.

CONFIGURATION

General

This section describes how the user can configure the module to function within his system by setting dip switches S1 and S2 (Figure 2) to obtain the desired device address and interrupt vector as described in Table 1. When a jumper wire is inserted between the lugs, the single-ended inputs (16 channels) are selected. When the wire is removed, quasi-differential inputs are selected.

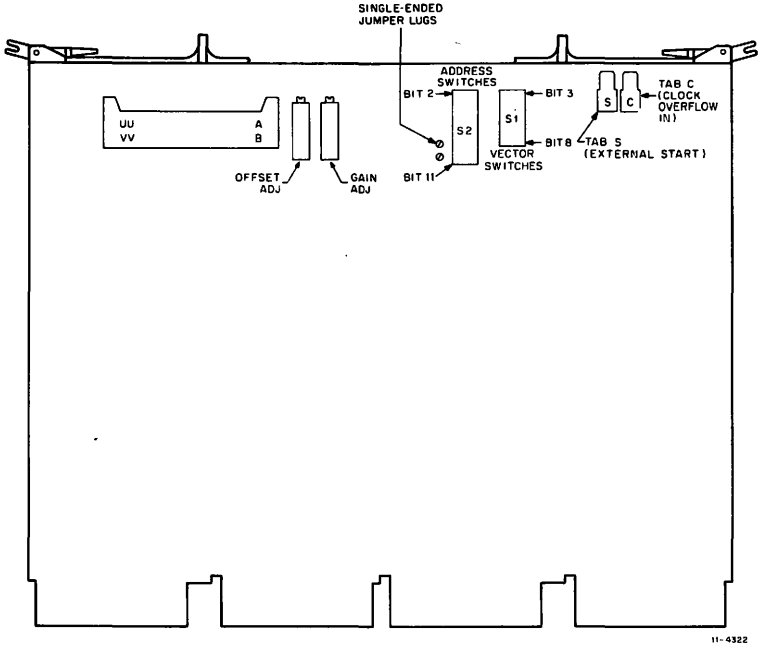


Figure 2 ADV11-A Connectors and Switches

Table 1 Standard Assignments

Description	Mnemonic	First Module Address	Second Module Address
Registers			
Control and Status	CSR	170400	170420
Data Buffer	DBR	170402	170422
Interrupt Vectors			
Conversion Complete		400	410
Error		404	414

Registers

The control and status register (CSR) address can be selected in the range of 170000 to 177774 by using the S2 dip switch as shown in Figure 3. Switch S2 is factory-set at 170400, which is the recommended address as illustrated in Figure 3. The functions of the CSR bits are shown in Figure 4 and detailed in Table 2.

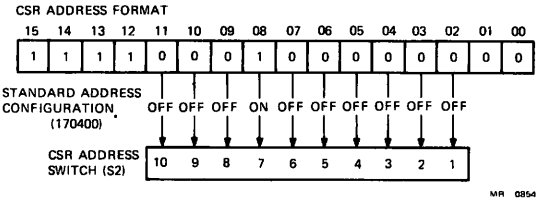


Figure 3 CSR Switch-Selectable Address

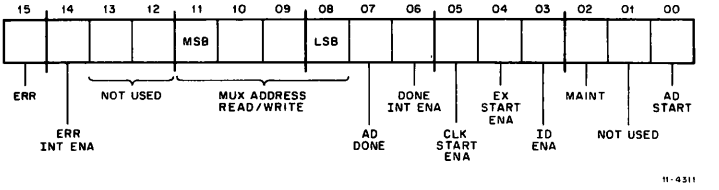


Figure 4 CSR Bit Format

Table 2 CSR Bit Functions

Bit	Description
15	A/D Error (Read/Write)—The A/D Error bit may be program set or cleared and is cleared by asserting BINIT L. It is set by any of the following conditions: 1. Attempting an external or clock start during the transition interval. 2. Attempting any start during a conversion in progress. 3. Failing to read the result of a previous conversion before the end of the current conversion.
14	Error Interrupt Enable (Read/Write)—When set, enables a program interrupt upon an error condition (A/D Error). Interrupt is generated whenever bits 14 and 15 are set, regardless of which was set first.
13-12	Not used.
11-8	Multiplexer Address (Read/Write)—Contains the number of the current analog input channel being addressed.
7	A/D Done (Read)—Set at the completion of a conversion when the data buffer is updated. Cleared when the data buffer is read by asserting BINIT L. If enabled, interrupts are requested simultaneously by both bits 7 and 15; bit 7 has the higher priority.
6	Done Interrupt Enable (Read/Write)—When set, enables a program interrupt at the completion of a conversion (A/D Done). Interrupt is generated when bit 7 and bit 6 are both set regardless of sequence.
5	Clock Start Enable (Read/Write)—When set, enables conversions to be initiated by an overflow from the clock option.
4	External Start Enable (Read/Write)—When set, enables conversions to be initiated by an external signal or through a Schmitt trigger from the clock option.

Table 2 CSR Bit Functions (Cont)

Bit	Description
3	ID Enable (Read/Write)—When set, causes bit 12 of the data buffer register to be loaded to 1 at the end of any conversion.
2	Maintenance (Read/Write)—When set, loads all bits of the converted data output equal to multiplexer address LSB (bit 8) at the completion of the next conversion. Cleared by asserting BINIT L. Used for all 0s and all 1s = test of A/D conversion logic.
1	Not used
0	A/D Start (Read/Write)—Initiates a conversion when set. Cleared at the completion of the conversion and by asserting BINIT L.

The data buffer register (DBR) address will be the next even address following the selected CSR address. This address has two separate DBR registers: one read-only and the other write-only. The functions of the register bits are shown in Figure 5 and described in Table 3.

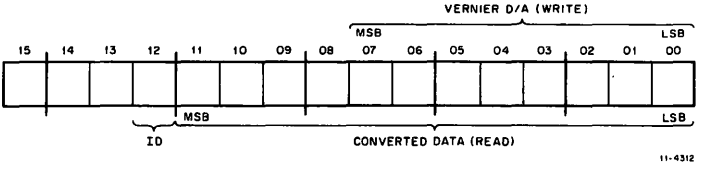


Figure 5 DBR Bit Format

Table 3 DBR Bit Functions

Bit	Function
Read-Only	
15-13	Not used. Should read as 0.
12	ID—When ID Enable (bit 3) of the CSR has been set, DBR bit 12 will be set to 1 at the end of the conversion.
11-0	Converted Data—These bits contain the results of the last A/D conversion.
Write-Only	
15-8	Not used.
7-0	Vernier D/A—These bits provide a programmed offset to the converted value (scaled 1 D/A LSB = 1/50 A/D LSB). The hardware initializes this value to 200_8 (mid-range). Values greater than 200_8 make this input voltage appear more positive.

Vector Interrupt

The A/D conversion complete interrupt vector is set by dip switch S1 (Figure 2). Any address in the range of 000_8 to 777_8 can be selected by the user. The switch is factory-configured for 400_8, the recommended vector, as shown in Figure 6. The error interrupt vector will be four words higher than the A/D conversion complete interrupt vector.

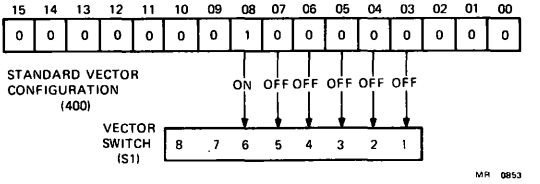


Figure 6 Interrupt Vector

Mode Control

The ADV11-A is equipped with the jumper lugs (Figure 2) that permit changing the operating mode from quasi-differential (no connection) to single-ended (jumper installed). The single-ended mode can also be selected by connecting H854 connector pin C to logic ground. This alternative is provided to permit convenient external mode selection in installations that require frequent alteration between one mode and the other.

Analog Input Interfacing

Single-Ended Mode — Single-ended analog input signals for the ADV11-A may be of two types, grounded and floating. A grounded input is one whose level is referenced to the ground of the instrument that is producing it, as illustrated in Figure 7. Since the instrument may be located at a distance from the computer, there may be some voltage difference between the instrument ground and the computer ground. The voltage seen by the ADV11-A will be the sum of the undesired ground difference voltage and the desired instrument signal voltage. In cases where such differences are encountered, they can be minimized by plugging the instrument into an ac outlet as close as possible to that providing power to the computer. Do *not* run a wire from user's ground to the ADV11-A analog ground. Such a wire can cause ground loop currents which affect results not only on the input channel in question, but also on other channels.

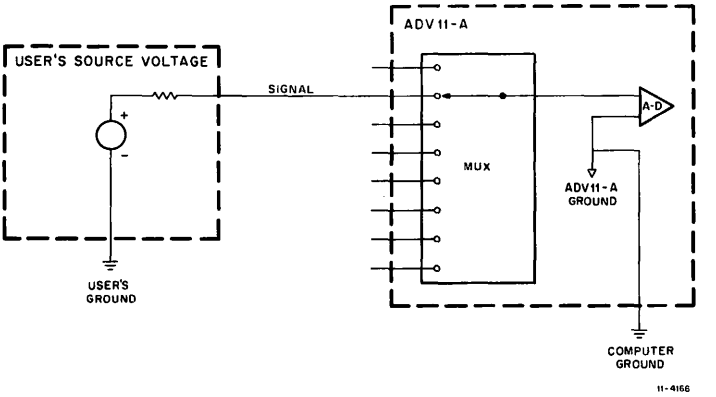


Figure 7 Single-Ended Input Referenced to User's Ground

A floating input is one whose signal voltage is developed with respect to a point not connected to ground, as illustrated in Figure 8. The identifying characteristic of a floating source is that connecting the signal return to the ADV11-A ground does not result in a current path between the ADV11-A ground and the instrument ground.

Note that the return of a floating input must be connected to one of the ADV11-A's analog ground terminals. Ground points may be shared among channels, as illustrated by the battery-powered sources in the figure.

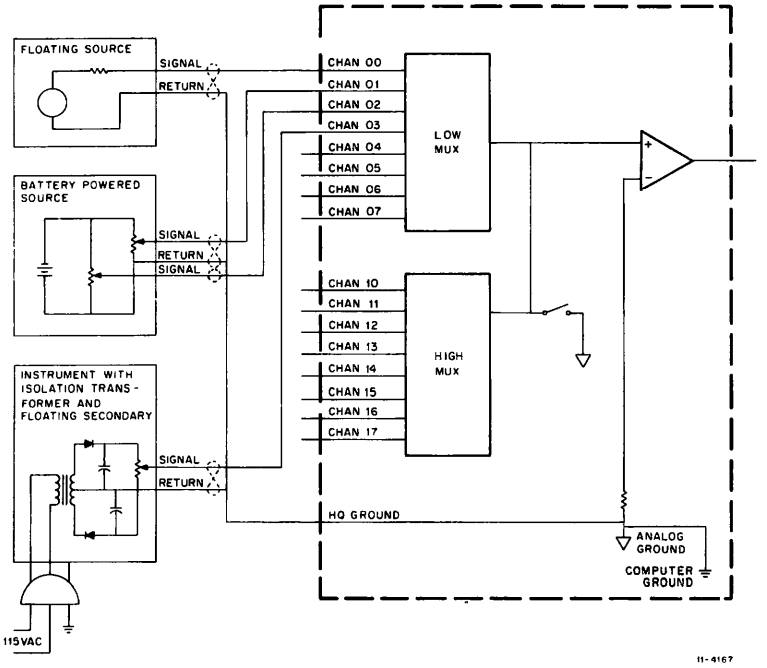


Figure 8 Floating ADV11-A Input Signals

Quasi-Differential Mode — The "quasi" prefix in "quasi-differential" can best be explained by reviewing a true differential operation. A true differential input involves two signal lines connected to a differential amplifier so that the output of the device is a function of the instantaneous *difference* between the voltages on the two signal lines. One advantage of such a configuration is illustrated in Figure 9.

Figure 9A assumes a single-ended generating device that produces a signal, V_s with respect to its ground and is situated sufficiently far enough away from the receiving device for a significant noise voltage, V_n, to be developed in the power distribution ground lines. The result is that, at any given instant, the differential amplifier in the receiving device sees both the signal voltage and the noise voltage. Its output, V_o, is a function of $V_s + V_n$ and is in error with respect to V_s alone.

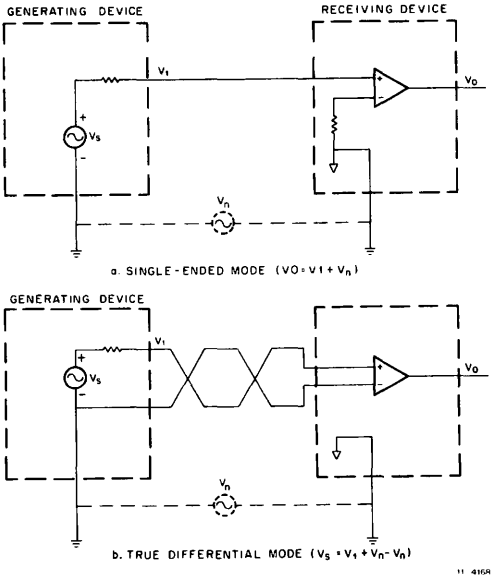


Figure 9 Single-Ended vs. True Differential Input Modes

Figure 9B illustrates the same device connected in true differential mode. The same noise voltage exists in the power distribution ground system, except the generating device ground is connected directly to the negative input of the receiving differential amplifier. Because the instantaneous noise voltage is common to both the + and − inputs, it is cancelled out of the final amplifier output. V_0 now provides a valid representation of V_S alone.

Figure 10 illustrates the ADV11-A operating in the quasi-differential mode.

The major contrast between true differential operation as described above and the operation of the ADV11-A in differential mode is that in the latter, the two sides of the signal are not simultaneously input to a differential amplifier. Rather, their difference is established by a sequential operation that first samples the voltage at one of the two inputs and then, holding this value fixed, in effect subtracts it from the

voltage at the second input. For near dc conditions, this procedure produces a result like that of true differential operation (i.e., the output is a function of the difference between the two input voltages, and common mode voltages are cancelled out).

Because of a significant time lapse, however, between taking the sample and completing the final approximation, a possibility for error is introduced by the ADV11-A that increases as a function of common mode signal frequency. The result is that the common mode rejection ratio, while essentially infinite at dc, rolls off for ac signals, and is about 40 dB at 60 Hz line frequency. Also, because the holding action of the sample-and-hold circuit is, in effect, only on the first (non-inverting, signal) input, but not on the second (inverting, return) input, the voltage rate of change on the second input should be kept below 25 mV/rms. This is the slope that results in a quarter-LSB change during the conversion interval. Such a rate of change corresponds to 125 mV peak-to-peak at 60 Hz line frequency. This dynamic response difference between the two inputs requires distinguishing the ADV11-A's differential mode from true differential operation. Hence the term "quasi-differential."

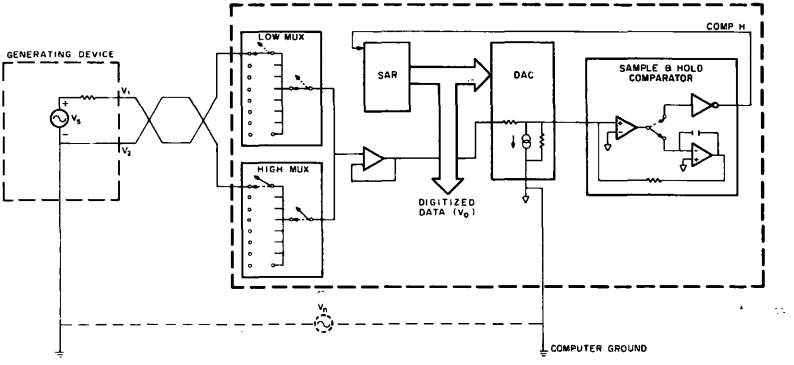


Figure 10 ADV11-A Quasi-differential Mode

Installation Precautions
As a preliminary step, confirm that the computer power supply ground is connected to power line (earth) ground. If continuity checks reveal no such connection, attach a length of 12-gauge wire between the power supply ground and a convenient point associated with earth ground.

Twisted Pair Input Lines — The effects of magnetic coupling on the input signals may be reduced for floating single-ended or differential inputs by twisting the signal and return lines in the input cable. If the inductive pickup voltages of the two leads match, the net effect seen at the ADV11-A input is zero. Use of twisted pairs has no effect with a single-ended non-floating signal (referenced to ground at the instrument end).

Shielded Input Lines — The effects of electrostatic coupling on the input signals may be reduced by shielding the signal wires. This is especially important if the instrument or transducer has high source impedance. To prevent the shield from carrying current and thus developing ground loop voltages within the ADV11-A, connect it to ground at the instrument end only.

Allowing for Input Settling with High Source Impedance — All solid-state multiplexers inject a small amount of charge into their input lines when changing channels. This causes a transient error voltage that is discharged by the source impedance of the input signal. The ADV11-A has this characteristic, and also injects a small charge into the selected input line at the end of each conversion when the auto-zero switch is turned off. After any channel change and after any conversion, the ADV11-A's control allows a 9-μs interval (identified as the transition interval) during which conversions cannot start without generating error conditions. Normally, this is sufficient time for the input transient to settle out.

More time may be needed, however, when the multiplexer is switching into an input channel with high source impedance, particularly when large amounts of shunt capacitance exist in the interconnecting cables. Avoid products with source impedance/cable shunt capacitance greater than 1 μs whenever conversions are to be made at maximum rate with less than ½ LSB error. This means that cable shunt capacitance for a 1000 Ω source should not exceed 1000 pF ($10^3 \times 10^{-9} = 10^{-6}$), that shunt capacitance for a 100 Ω source should not exceed 0.01 μF ($10^2 \times 10^{-8} = 10^{-6}$), etc. Assuming twisted pair cable capacitance of 50 pF/foot, these constraints translate into a maximum

run of 20 feet from a 1000 Ω souce, 200 feet from a 100 Ω source, etc. Note that these values are consistent with good practice for avoiding noise pickup in long cable runs. Note also that settling errors can be eliminated by increasing the time between conversions or incorporating a software delay between channel changes and program start commands.

Connections

Figure 11 illustrates the location of user connectors and switches on the component side of the ADV11-A board.

Analog input signals are input to the ADV11-A through the 40-pin connector. Pin assignments for the connector are shown in Figure 11. The proper H856-to-H856 cable is the BCO8R; The proper H856 to prepared open-ended cable is the BCO4Z.

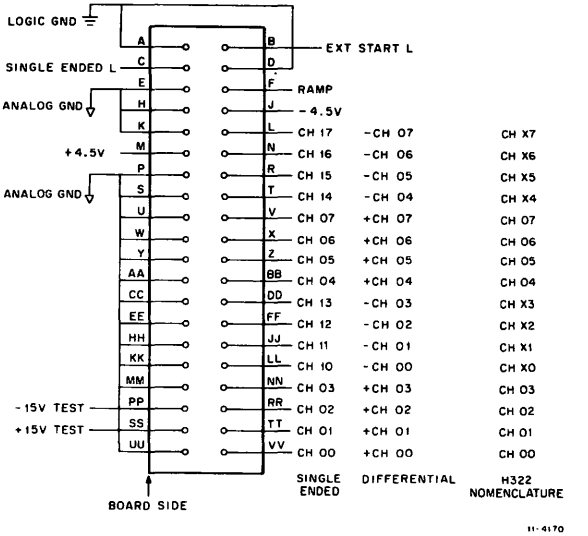


Figure 11 ADV11-A 40-Pin Connector Pin Assignments

Distribution Panel — Figure 12 shows an H322 distribution panel that is connected on the rear to the ADV11-A Berg connector and on the front provides easily identifiable and conveniently accessible barrier

strip connections for user apparatus. Each H322 accommodates two ADV11-As or one ADV11-A and one other single-connector device. Note that the H323-B potentiometer box may *not* be used with the ADV11-A.

External and Clock Starts — The external start signal line, pin B of the 40-pin connector or TAB S (Figures 2 and 11), is a TTL-compatible input that presents five unit loads (8.0 mA) to any driving output. Conversions start on the high-to-low transitions of this signal.

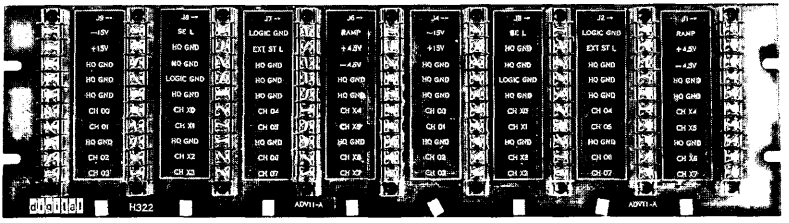


Figure 12 H322 Distribution Panel

In most cases, the external start signal will be produced by a grounded (non-floating) pulse generator or logic circuitry located in a grounded instrument. The return path for the external start signal will be through the power line ground system. For this reason, ground differences between source and computer should be minimized to prevent spurious start pulses due to ground noise. In no case should a separate return line be run between grounded source and the computer ground. Only with floating devices should return lines be run between source logic ground and logic ground pins on the ADV11-A 40-pin connector. External devices that require buffering can be interfaced to the ADV11-A through Schmitt trigger 1 of the KWV11-A clock (STI). Connection is made by means of a DEC 70-10771 type jumper to TAB S (Figure 2) of the ADV11-A.

Conversions that must be initiated by time intervals or on every nth external event may be triggered from the KWV11-A through a DEC 70-

10771 type jumper connected from the clock output tab (CLK) to the ADV11-A clock overflow tab (C).

PROGRAMMING

The following programming example reads 100_8 A/D conversions from channel 0 into locations 4000_8—4176_8 and halts.

```
START:  CLR     @ADSR           ;CLEAR A/D STATUS REGISTER
        MOV     #4000,R0        ;SET UP FIRST ADDRESS
        INC     @ADSR           ;START A/D CONVERSION
LOOP:   TSTB    @ADSR           ;CHECK DONE FLAG
        BPL     LOOP            ;WAIT UNTIL FLAG SET
        INC     @ADSR           ;START NEXT CONVERSION*
        MOV     @ADBR,(R0)+     ;PLACE CONVERTED VALUE
                                ;FROM A/D BUFFER INTO MEMORY
                                ;LOCATION AND SET UP NEXT
                                ;LOCATION FOR TRANSFER*
        CMP     R0,#4200        ;CHECK IF 100 CONVERSIONS
                                ;HAVE BEEN DONE
        BNE     LOOP            ;NO, GET NEXT CONVERSION
        HALT                    ;DONE
ADSR:   170400                  ;A/D STATUS REGISTER ADDRESS
ADBR:   170402                  ;A/D BUFFER REGISTER ADDRESS
        .END    START
```

* Starting a subsequent conversion before moving data from a previous conversion is recommended only with systems equipped with non-processor memory refresh. Without this capability, data will be lost occasionally by CPU memory refresh intervening between the INC and MOV commands. In general, non-processor memory refresh is essential to realizing the full potential of the ADV11-A.

BA11-M

BA11-M EXPANSION BOX

GENERAL

The BA11-M expansion box provides a convenient means for expanding LSI-11 bus systems. Each expansion box includes an H9270 LSI-11 bus-structured backplane and an H780 power supply system mounted in an enclosure with a blank front panel.

The BA11-M is shown in Figure 1. Mechanical and mounting details are shown in Figures 2 and 3.

FEATURES

- Provides power and cooling for LSI-11 Bus options
- Accepts quad or double height modules
- Eight double-height (four quad) LSI-11 Bus slots available for options
- LSI-11 Bus power sequencing signals provided by the power supply
- LSI-11 Bus line frequency clock signal provided by power supply
- LSI-11 Bus backplane compatible with LSI-11, LSI-11/2 and LSI-11/23 processors, memories, and interface modules
- Rack-mountable in standard RETMA 19" wide rack
- UC listed; CSA certified

SPECIFICATIONS

Dimensions (including bezel)	
Width	48.3 cm (19 in)
Height	8.9 cm (3.5 in)
Depth	
Without mounting brackets	34.3 cm (13.5 in)
With mounting brackets	38.1 cm (15.0 in)
Shipping Weight	18.1 kg (40 lb)
Operating temperature*	5° to 50° C (41° to 122° F)
Operating humidity	10% to 95% with a maximum wet bulb temperature of 32° C (90° F) and a minimum dew point of 2° C (36° F)

* The maximum allowable operating temperature is based on operation at sea level, i.e., at 760 mmHg (29.92 inHg); maximum allowable operating temperature will be reduced by a factor of 1.8° C/1000 m (1.0° F/1000 ft) for operation at higher altitude sites.

BA11-M

AC input power	100-127 Vrms, 50 ±1 Hz or 60 ±1 Hz, 400 W maximum, or 200-254 Vrms, 50 ±1 Hz or 60 ±1 Hz, 400 W maximum
DC output power	+5 Vdc ±3%, 0-18 A load (static and dynamic) +12 Vdc ±3%, 0-3.5 A load (static and dynamic) Maximum output power: 120 W (total)
Recommended circuit breaker rating	15 A and 115 Vac or at 230 Vac

DESCRIPTION

The BA11-M is a rack-mounted enclosure that provides power and cooling for eight double (four quad) LSI-11 Bus module slots. It accepts either double or quad size modules. Modules are accessible from the front of the box. A cable area is provided for routing I/O cables from the modules to the rear of the box where a cable clamp allows cables to be strain-relieved before leaving the box. An AC ON/OFF switch and line cord are located at the rear of the box. Two of the eight slots for double size modules are normally used for cabling and termination, which leaves six bus slots available for options. Note that multi-board options that require the special backplane interconnection on connections card D (i.e., RLV11) are not accommodated by this expansion box. The BA11-M is available in two line voltage variations: 115V and 230V. Each version accommodates either 60 Hz or 450 Hz line frequency.

CONFIGURATION

When installing an expansion box to expand from a single to a dual backplane system, the BCV1B bus expansion option and TEV11 bus terminator option (or equivalent) must be used. Install the BCV1B modules and cables as shown in Figure 4. The terminator must be installed in the option location in the last box. When installing the BCV1B cable set, disregard any "This side up" labels that may be on the BC05L cables. Ensure that the red line on each cable is toward the center of both modules and that J1 on each board is connected to J1 on the second board and similarly J2 on both boards. Ensure that the cables have no twists. Carefully fold excess cable as shown in Figure

4. Figure 5 illustrates proper installation of the BCV1B and TEV11 options.

When expanding from a second to a third backplane, the BCV1A bus expansion option is required, in addition to the items required for expansion to the second backplane.

NOTE

BCV1A and BCV1B cables must differ in length by 121.92 cm (4 ft) (minimum).

The completed installation for a 3-backplane system using the BCV1A option is shown in Figure 5. In addition to this option, the BCV1B option is required to connect the first backplane to the second backplane; a 120 Ω bus termination is required in the last option slot in the third backplane.

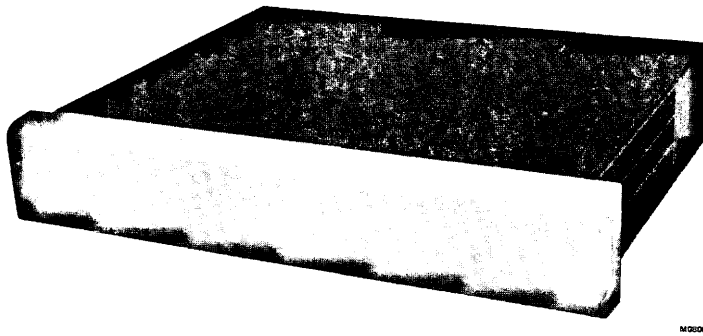


Figure 1 BA11-M Expansion Box

BA11-M

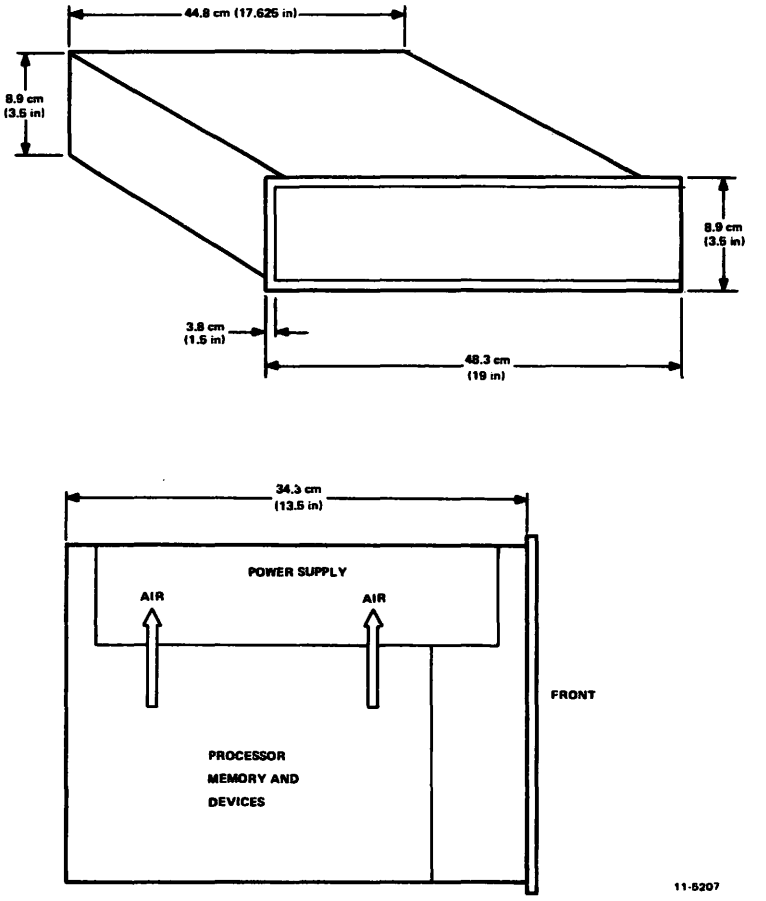


Figure 2 BA11-M Assembly Unit

BA11-M

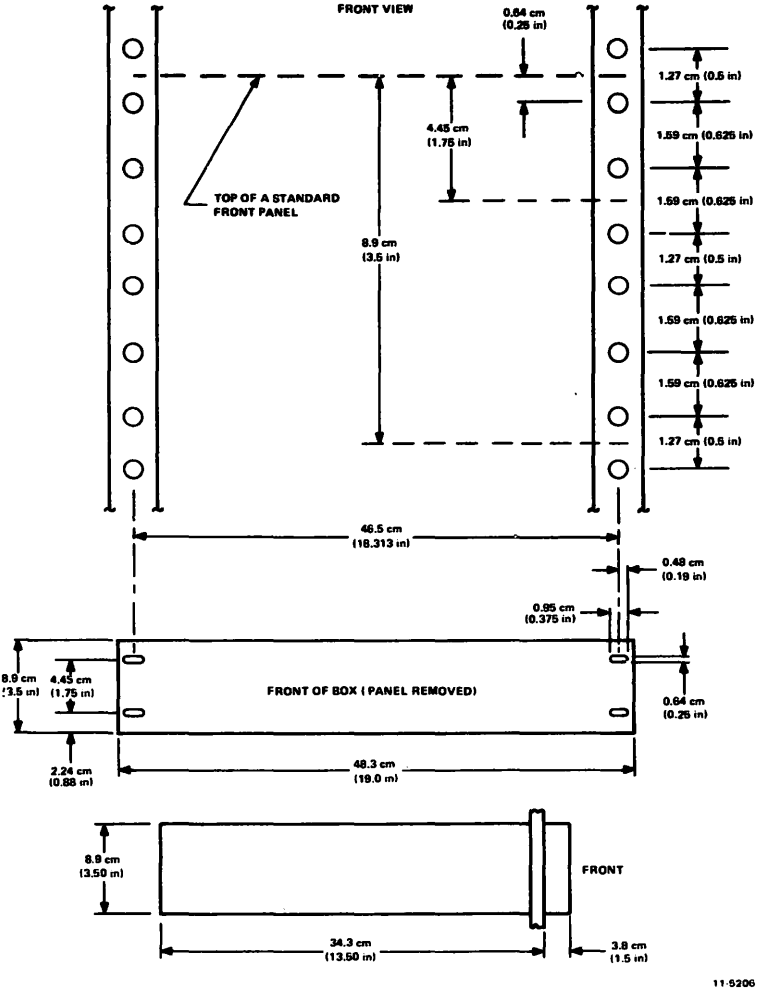


Figure 3 BA11-M Cabinet Mounting

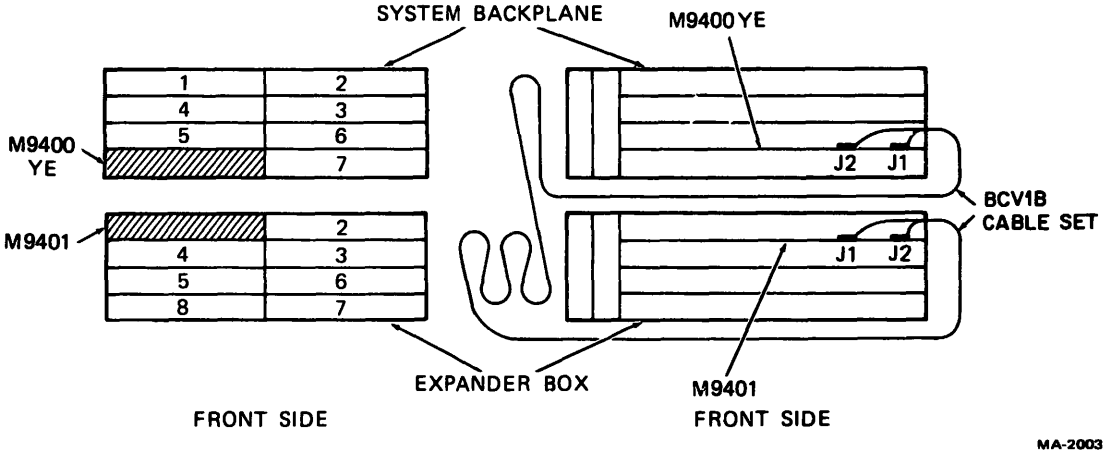
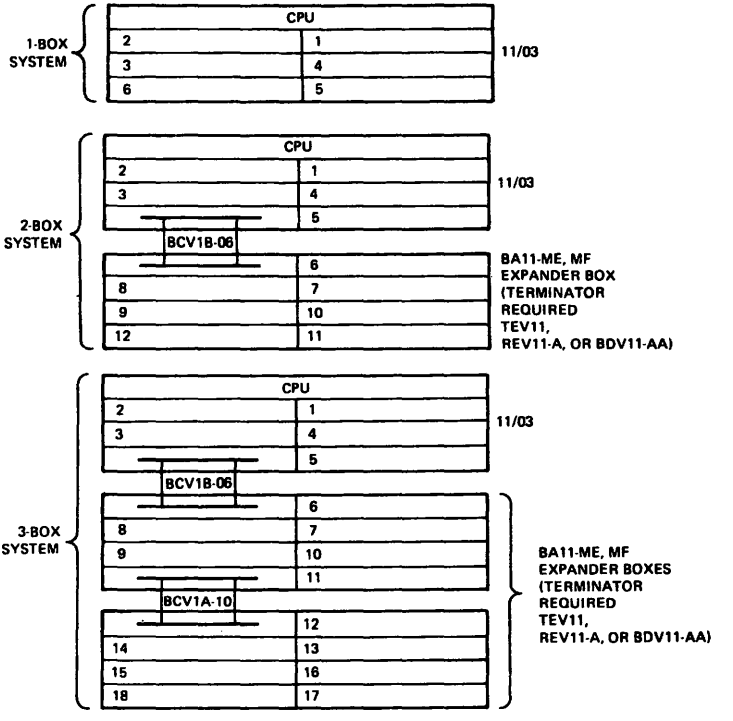


Figure 4 BA11-M Expansion Box Interconnections (two-backplane system)



NOTES

1. INCLUDED IN BCV1B BUS EXPANSION OPTION. (CABLES ARE AVAILABLE IN 2, 4, 6, OR 12 FT LENGTHS.)
2. INCLUDED IN BCV1A BUS EXPANSION OPTION. (CABLES ARE AVAILABLE IN 2, 4, 6, OR 12 FT LENGTHS.)
3. INCLUDED IN TEV11 BUS TERMINATOR OPTION.
4. THE LSI-11 BUS IN RESTRICTED TO 15 OPTIONS, MAXIMUM. THESE OPTION SLOTS WOULD ONLY BE USED WHEN PREVIOUS OPTION(S) OCCUPY MORE THAN 1 OPTION LOCATION.
5. BCV1A AND BCV1B EXPANSION CABLES MUST DIFFER IN LENGTH BY 4 FT (MIN).

MA-2000

Figure 5 BCV1A Installation

BA11-N

BA11-N MOUNTING BOX

GENERAL

The BA11-N mounting box is designed to be used as a mounting box or as an expander box for an LSI-11 bus-based system. Each mounting box (Figure 1) includes an H9273 backplane assembly, an H786 power supply, and an H403-A ac input panel mounted in an enclosure with a blank front panel (BA11-NE, NF) or bezel assembly (PDP-11/03-LC, LD).

FEATURES

- Nine slots for double or quad size modules
- Powerful and reliable 240-watt switching power supply, which is both voltage- and frequency-independent
- Module cooling
- Designed to meet small system applications
- Modular design for ease of servicing
- LSI-11 bus power sequencing signals provided by power supply
- Line frequency signal provided by power supply
- Unique backplane interconnection for custom multi-board options
- LSI-11 bus backplane-compatible with LSI-11, LSI-11/2 and LSI-11/23 processors, memories, and interface modules
- Rack-mountable in standard RETMA 19" wide rack
- UL listed, CSA certified and complies with VDE and IEC requirements

SPECIFICATIONS

Tables 1 and 2 show BA11-NE and BA11-NF mounting box specifications, including the H786 power supply.

Dimensions (including bezel)	
Width	48.3 cm (19 in)
Height	13.2 cm (5.19 in)
Depth	
Without mounting brackets	57.8 cm (22.7 in)
With mounting brackets	67.96 cm (26.75 in)
Weight (without modules)	20 kg (44 lb)

BA11-N

Operating temperatures*	5° to 50° C (41° to 122° F)
Operating humidity	10% to 95%, with a maximum wet bulb temperature of 32° C (90° F) and a minimum dew point of 2° C (36° F)
Input voltage	
BA11-NE	115 Vac
BA11-NF	230 Vac
Input current**	
BA11-NE	12 A max
BA11-NF	6 A max
Circuit breaker rating	15 A at 115 Vac or 230 Vac

* The maximum allowable operating temperature is based on operation at sea level, i.e., at 760 mmHg (29.92 inHg); maximum allowable operating temperature will be reduced by a factor of 1.8° C/1000 m (1.0° F/1000 ft) for operation at higher altitude sites.

** Input current consists of that used by the BA11-N, itself, plus whatever current is supplied via the convenience ac outlet (J3) to an expander box; the total current must be less than the maximum specified.

DESCRIPTION

The H9273 backplane assembly consists of a backplane, a card frame assembly, and two cooling fans. The H9273 9-slot backplane assembly will accept nine LSI-11 bus double-height or quad-height modules (except for MMV11-A 4K × 16 core memory modules). The PDP-11/03-LC and the BA11-NE operate on 115 V and the PDP-11/03-LD and the BA11-NF operate on 230 V. Mechanical and mounting details are shown in Figure 2.

BA11-N

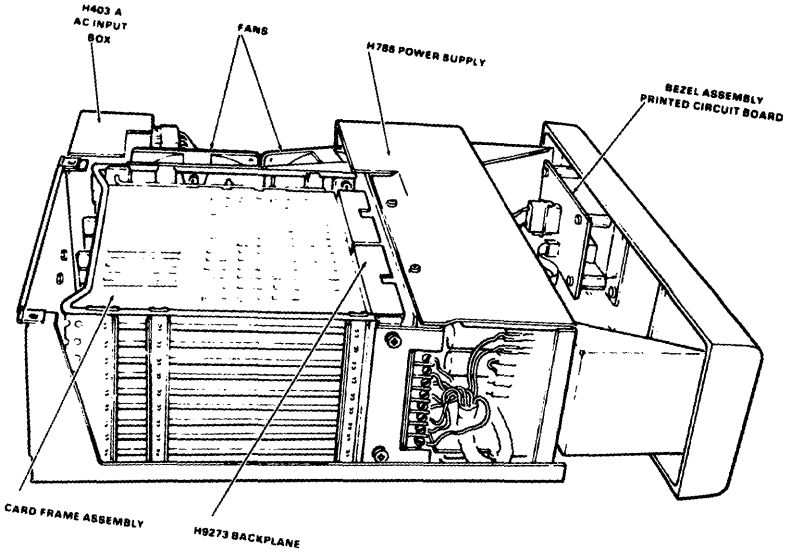
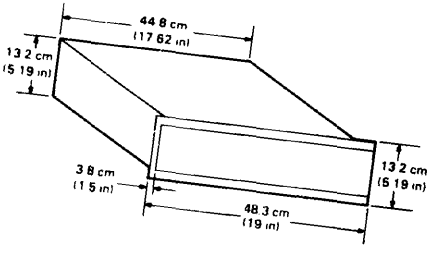


Figure 1 BA11-N Major Assemblies



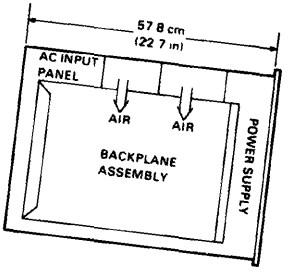


Figure 2 BA11-NE and BA11-NF Assembly Unit

The ac input box, power supply, and H9273 logic assembly are attached to the logic box base. The power supply assembly is hinged to the base and can be swung open to expose the internal components; with little effort, the entire assembly can be removed from the base and replaced. LSI-11 bus modules are inserted in the backplane from the rear of the box through an access door that is equipped with strain reliefs for LSI-11 bus and communications cables.

When the unit is to be mounted in an equipment rack, the logic box cover is attached to the rack with mounting hardware. The logic box base slides into the mounted cover and a spring-button assembly engages to prevent the base from being accidentally pulled out of the cover.

Table 1

Item	Specification
Current rating	5.5 A at 115 Vrms 2.7 A at 230 Vrms
Inrush current	100 A peak, for ½ cycle at 128 Vrms or 256 Vrms
Apparent power	630 VA
Power factor	The ratio of input power to apparent power shall be greater than 0.6 at full load and low input voltage
Output power	+5 Vdc ±250 mV at 22 A (A minimum of 2 A of +5 Vdc power must be drawn to ensure that the +12 Vdc supply regulates properly) +12 Vdc ±600 mV at 11 A
Power-up/power-down characteristics	
Static performance	
Power-up	BDCOK H goes high; 75 Vac BPOK H goes high; 90 Vac
Power-down	BPOK H goes low; 80 Vac BDCOK H goes low; 75 Vac

Table 1 BA11-N Power Supply Specifications (Cont)

Item	Specification
Dynamic performance	
Power-up	3 msec (min) from dc power within specification or to BDCOK H asserted 70 msec (min) from BDCOK H asserted to BPOK H asserted
Power-down	4 msec (min) from ac power off to BPOK H negated 4 msec (min) from BPOK H negated to BDCOK H negated 5 μsec (min) from BDCOK H negated to dc power as of specifications

CONFIGURATION

The procedure for mounting the BA11-N mounting box in an equipment rack is presented below.

Installing the Logic Box Cover — The logic box cover is mounted in the equipment rack as shown in Figure 3.

1. When the unit is shipped, the logic box cover is held to the base by four screws (these are used only in non-rack-mounted applications), and a single shipping screw, which, for safety, must be in place whenever the unit is moved or shipped. First, remove the four screws that attach the cover to the base. Then open the rear door and remove the shipping screw.
2. A safety locking device is found on the right side of the unit (when looking at the front). This device, a spring-button assembly, is attached to the side of the ac input box. When the unit is closed, the button on this assembly fits into the rear hole of two holes in the right side of the cover. This mechanical interlock can be overridden by pushing the button in from the outside of the cover while, at the same time, pulling the logic box base to get the button past the hole. The base can then be pulled out of the cover to its extended position; at this position, the button pops into the front of the two holes, preventing the base from being inadvertently pulled entirely out of the cover. Open the base to the extended position and then release the button from the front hole. Slowly

pull the base entirely out of the cover and set the base out of the way.

3. Attach the Tinnerman nuts to the cabinet uprights in eight places.
4. Mount the cover to the front cabinet uprights using four pan head screws (10-32 X 0.62 lg) and four No. 8 lockwashers.
5. Attach the two support brackets to the cover using four Phillips pan head screws (8.32 X 0.38 lg) and four No. 8 lockwashers.
6. Attach the support brackets to the rear cabinet uprights using four Phillips pan head screws (10-32 X 0.62 lg) and four No. 10 flat washers.
7. Slide the unit into the cover. It will be held in place by the spring-button assembly. To slide the unit forward again it will be necessary to release this spring button.
8. If the system is to be moved or shipped, the shipping screw must be replaced.

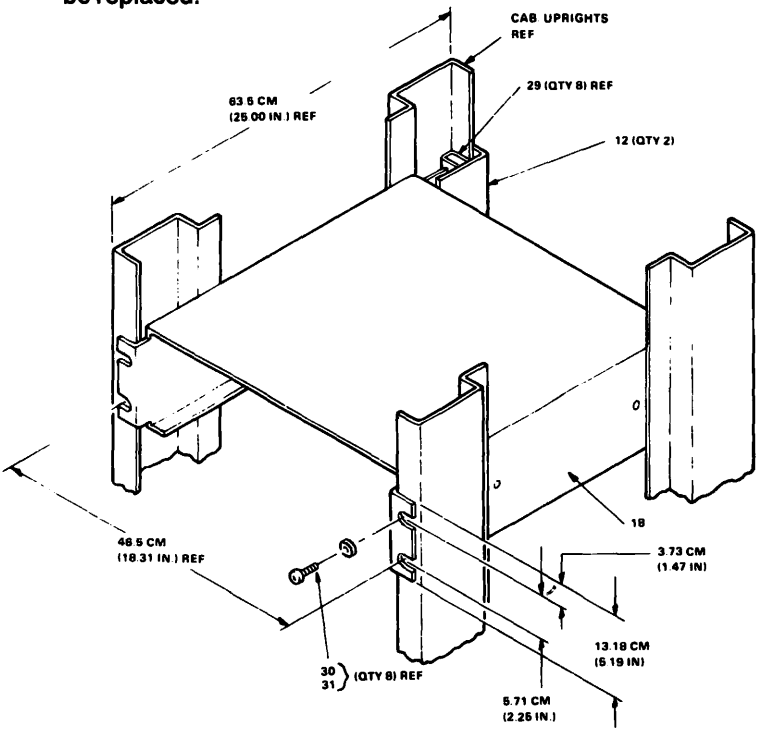


Figure 3 BA11-NE and BA11-NF Cover Mounting Dimensions

Installing the Logic Box Base in the Cover — Set the rear of the logic box base on the support flanges of the cover and slide the base in until the spring-button assembly engages in the extended position. Take care not to pinch the cables while sliding the base in. Release the spring-button and push the base all the way in until it engages in the closed position. Take the following steps to complete the installation.

NOTE

The base being installed is either the main base, i.e., the one containing the CPU, or an expander base (two expander boxes can be added). Modify the following instructions to suit the kind of base you are installing, e.g., if there is a blank front panel, skip the first half of step 1.

1. Put the AUX switch in the front panel in the OFF position; put the ON/OFF switch on the ac input box in the OFF position.
2. When the AUX switch on the front panel is in the ON position, the two wires of the power controller cable are common. Connect the free end of the cable to the input circuit of the power controller so that the AUX switch controls the application of primary power to the controller. Keep the AUX switch in the OFF position.
3. Loosen the cable strain reliefs and open the rear door of the box to install the LSI-11 bus expansion cable assemblies. Two cable assemblies are used. Table 3 describes the assemblies and tells where to insert the assembly modules. (Figure 4 illustrates module placement.) When inserting the modules, make sure the connectors are on top.
4. Close the rear door; bring the bus cables out under the left strain relief and the communcations cables out under the right strain relief. Adjust the strain reliefs so that the cables are held firmly but are not pinched or crushed. Secure the strain reliefs and the rear door. Make sure the cables will not bind when the base is pulled out to the extended position.

Table 2 LSI-11 Bus Expansion Cable Assemblies

Assembly	Assembly Composition	Insert Modules In
BCV1B-XX	Two BC05L-XX cables	
	One M9400-YE module	Slots A and B of the first open row after all other LSI-11 bus options have been installed in the main box.
	One M9401 module	Slots A and B of row 1 of expander box 1
BCV1A-XX	Two BC05L-XX cables	
	One M9400-YD module	Slots A and B of the first open row after all other LSI-11 bus options have been installed in expander box 1
	One M9401 module	Slots A and B of row 1 of expander box 2

NOTE

"-X" in the cable assembly number denotes length, which can be 60.96, 121.92, 182.88, or 304.80 cm (2, 4, 6, or 10 ft). (Each cable of an assembly is the same length.) When both assemblies are used in a system (boxes), the lengths must differ by 121.92 cm (4 ft). To facilitate servicing, the BCV1B cables should be 182.88 cm (6 ft) long, while the BCV1A cables should be 304.80 cm (10 ft) long.

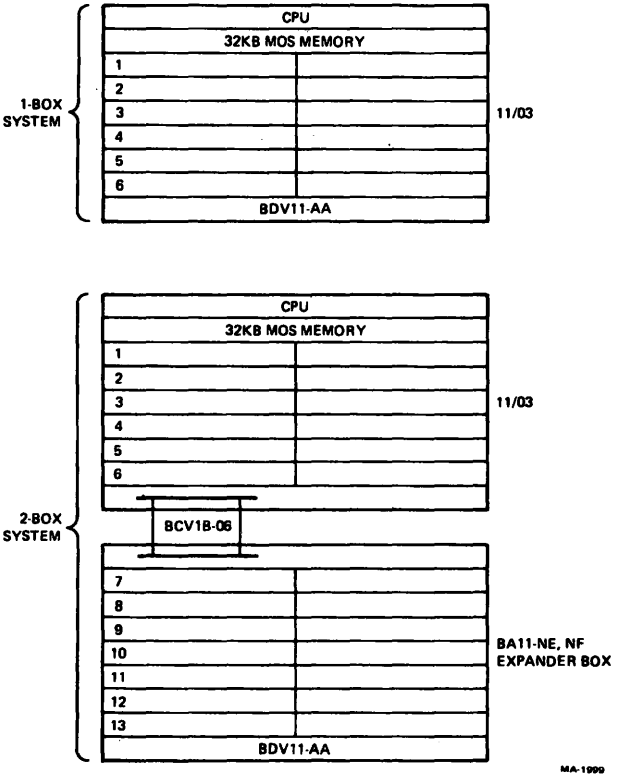


Figure 4 Configuring Large Box

BA11-VA MOUNTING CHASSIS/POWER SUPPLY

GENERAL

The BA11-VA is a small form-factor package providing mounting space and power for four LSI-11/2 or LSI-11/23 family modules. This package, plus the high functionality of DIGITAL's microcomputer products, allows LSI-11 microcomputer applications to be implemented within a space smaller than that required for many 8-bit systems.

FEATURES

- Four slots for double 5.2 in. × 8.9 in. (13.2cm × 22.8cm) height modules.
- LSI-11 bus backplane compatible with the LSI-11/2 and LSI-11/23 processors, memories, and interface modules.
- Power and cooling for modules.
- DC power indicator.
- Mounting hardware for table-top or fixed-position usage.
- Off/On switch located at the rear of the unit.
- External connection to let users add a remote restart switch.
- UL listed, CSA certified, and complies with VDE and IEC requirements.

SPECIFICATIONS

Mechanical	
Capacity	4 dual LSI-11 bus modules
Size	11.7 in. × 13.38 in. × 3.62 in. (29.71cm × 33.98cm × 9.19cm)
Weight	10 lbs (4.5kg)
Mounting	4 rubber feet for table-top use and 4 metal brackets for fixed position mounting (installed by user)
Environmental	
Operating Temperature	5°C (41°F) to 5°C (122°F)
Relative Humidity	10% to 95% (non-condensing)
Power	
Output	5.6 amps at +5V max 1.6 amps at +12V max

BA11-VA

Input Voltage	115Vac-50/60Hz or +230V-50/60Hz (selectable by user)
Current	3.0 amps at 115V (maximum) 1.5 amps at 230V (maximum)
Power Cord	6 ft. 3 in. (1.9m) for 115 Vac to be used with a NEMA 5-15P wall socket. User supplies cord for other power requirements.
External Connectors	
Optional Power Outlet	Plug type (user-supplied) for use with the power outlet: 3-pin AMP™ plug—Part #1-480700-0 AMP contact pins—Part # 350547-3
Remote Restart	Plug type (user-supplied) for use with the remote restart outlet: 2-pin AMP plug—Part #1-480698-0. AMP contact pins—Part # 350547-3
Model Number	BA11-VA—LSI-11 Bus mounting chassis and power supply

DESCRIPTION

The BA11-VA is designed as a low-cost mounting enclosure for a wide range of mounting configurations. Two types of mounting hardware let the BA11-VA be used as a table-top unit or be attached to a flat surface in any plane.

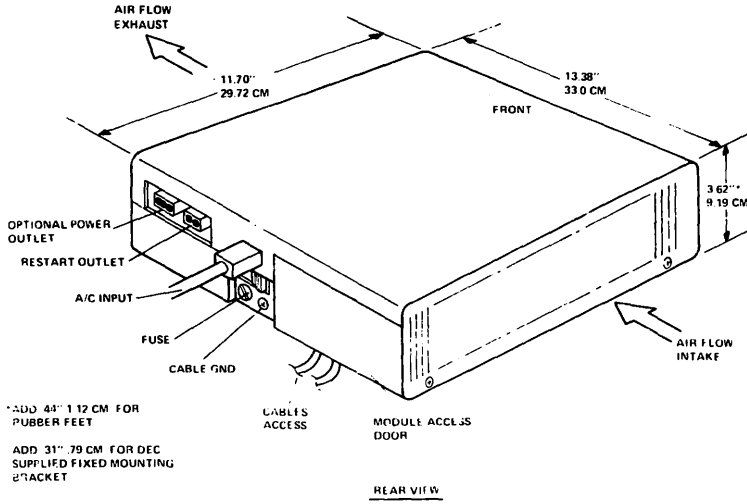
The BA11-VA does not generate a signal for use as a line-time clock in the processor module. If this function is required, the MXV11 multi-function module, which includes a 60Hz clock, should be used. If power-fail capability is needed, external hardware is required.

For applications where the mounting of the BA11-VA prevents easy user access to the chassis, the capability is provided for adding an external restart switch. A simple, single pole/single throw switch can be located up to 10 feet from the box and connected using a standard connector. Momentary closure of this switch causes the processor to go to the user-selected power-up mode for the system.

The power supply has more capacity than normally used by the four LSI-11 bus modules that can be mounted in the chassis. Therefore, a

connector is supplied to let this power be used for other electronic equipment located in the same area as the computer.

The BA11-VA power supply can be configured through selector switches to operate throughout the world. The product is UL listed, CSA certified, and complies with VDE and IEC requirements.



BDV11

BDV11 DIAGNOSTIC, BOOTSTRAP, TERMINATOR

GENERAL

The BDV11 module has 2K words of read-only memory (ROM) that contains both diagnostic programs and bootstrap programs. These programs are user-selectable by setting dip switches. The diagnostic programs test the processor, the memory, and the user's console. The bootstrap programs are used to boot a number of LSI-11-compatible peripherals. The module also contains 120-ohm bus terminator circuits.

Space is available on the module to allow the user to add up to 2K words of erasable programmable ROM (EPROM) and up to 16K words of read-only memory (ROM).

A HALT/ENABLE switch allows the user to start and stop the processor and a RESTART switch enables the user to reboot the system. The module also has four programmable light-emitting diodes (LEDs) that indicate a failure in a program and monitor the tests in progress. All the switches and indicators are edge-mounted on the module for easy access.

NOTE

There are two versions of the BDV11 module: revisions 0 and A. The revision 0 module was produced in limited quantities and does not incorporate all the characteristics of revision A. The differences between these modules are listed at the end of this section.

FEATURES

- Programmed ROMs with bootstraps for RXV11, RXV21, RLV11, and RKV11 disk options
- DECnet bootstraps for DLV11-E, DLV11-F, and DUV11 serial line units
- Capable of booting a system automatically with no operator intervention
- Can automatically load and start a 16K word program from ROM/EPROM to RAM
- 12-bit readable configuration register
- 16-bit read/write maintenance register

BDV11

- Software-controllable line-time clock (LTC)
- Power OK monitor, green LED
- 4-bit LED programmable display
- RESTART and HALT switches
- 120-ohm bus terminator

SPECIFICATIONS

Identification	M8012
Type	Quad
Power	+5 Vdc ±5% at 1.6 A +12 Vdc ±3% at 0.07 A
Bus Loads	
AC	2
DC	1

DESCRIPTION

General

The functions of the BDV11 are shown in Figure 1. The transciever and control functions control the transfer of data between the bus and the BDV11. The ROM address function decodes the address data from the bus and uses the socket selection and ROM address functions to access the memory located on the BDV11. The ROM address function is also used to transfer data into the data selection function. Then data is placed on the LSI-11 bus by the control and transciever functions. The data for the read/write registers are also transferred in and out by using the transceiver and control functions. The BDV11 uses power-up, BVENT, and display functions for monitoring program operations.

Transceiver

The transceiver logic monitors the LSI-11 bus BDAL lines for the address of a BDV11 register or the address of a ROM location. When a register or a ROM has been addressed, the transceiver logic gates the address onto the BDV11 DAL lines. If a register was addressed, the transceiver logic generates the address match signal that activates the control logic. If a ROM address was generated, then the DAL lines transfer the address to the ROM address selection logic. The transceiver logic is also used to transfer data from the DAL lines to the LSI-11 bus BDAL lines. When the transceiver receives XMIT H, the data can be from either a register or ROM address.

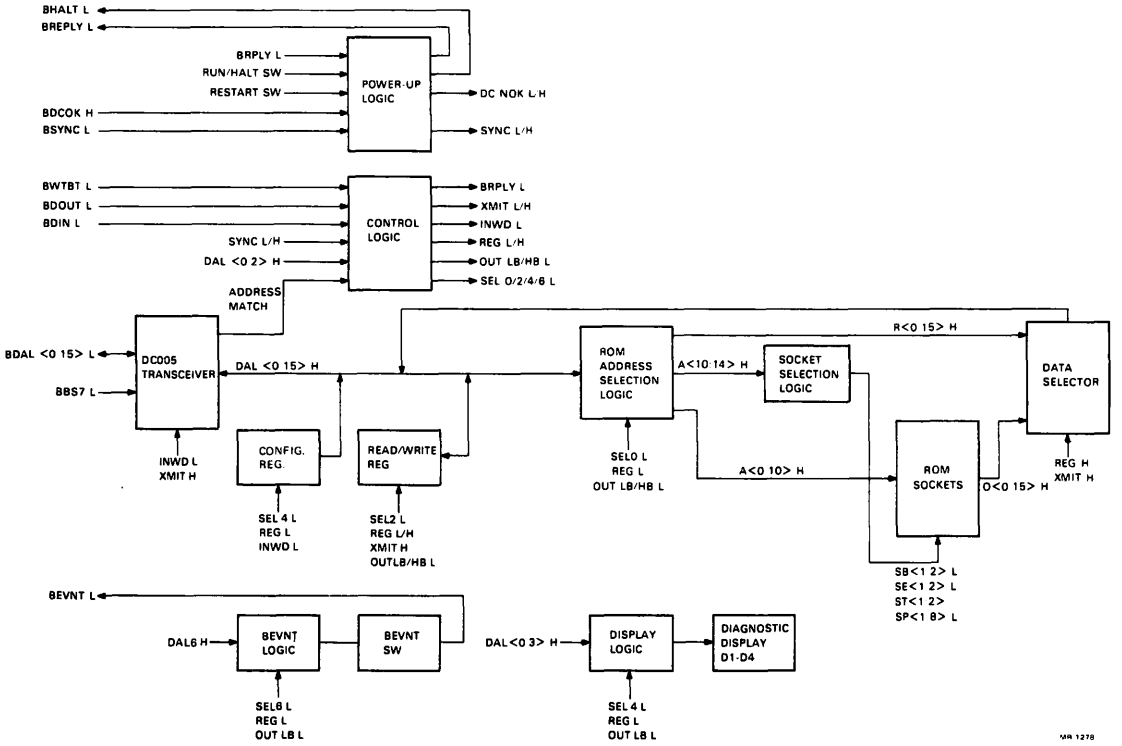


Figure 1 BDV11 Block Diagram

Control

The control logic consists of a DC004 protocol chip (Chapter 5) and an 82523 PROM. The control logic is enabled by the address match signal from the transceiver logic. The PROM monitors some of the DAL lines and the address match signal and generates an enable signal for the DC004 chip whenever any of the assigned bus addresses (173000 to 173777) is placed on the BDAL lines. The DC004 chip generates all the protocol signals used with the LSI-11 bus to allow data transfers. The control logic also generates the control signals for the read/write register's ROM address selection and the ROM socket selection logic. The bus control signals are defined in the appropriate processor handbook.

Read/Write Registers

The read/write register logic consists of two 8-bit universal shift registers. When the registers are being read, the control logic asserts XMIT H and the information on the DAL lines is the data within the shift registers. When the registers are to be written into, the XMIT signal is negated and the registers are placed into a load condition. The registers are clocked and the information on the DAL lines is loaded into the registers as data. The registers are cleared when power is turned on or when the system is booted.

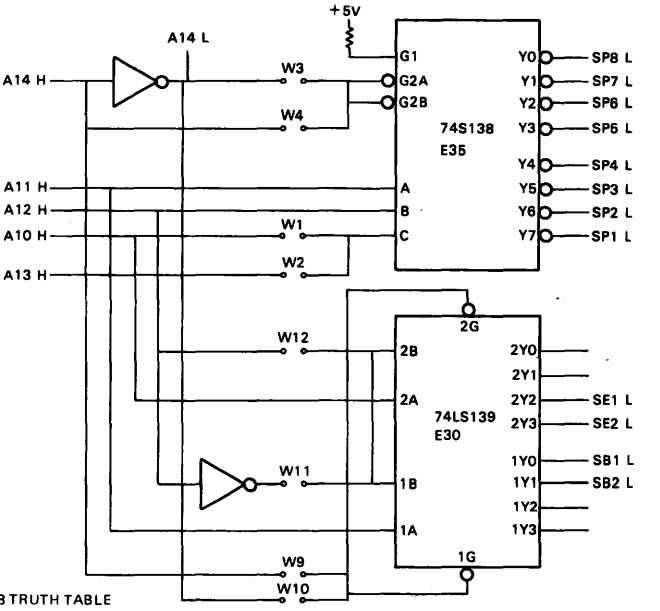
ROM Address Selection

The ROM address selection logic uses the contents of the PCR register and the LSI-11 bus address to determine the address of the BDV11 ROM locations. Each ROM has 2048_{10} addresses available. The logic selects the high byte of the PCR register if bit 8 of the LSI-11 bus is one and selects the low byte if bit 8 is a zero. The selected byte is shifted to the right one bit and used as the high byte of the BDV11 address. The low byte of the LSI-11 bus address is shifted one bit to the right and used as the low byte of the BDV11 address. The complete BDV11 ROM address is formatted by using a combination of the high and low bytes generated. Table 10 is a listing of how the PCR contents and the LSI-11 bus addresses are used to generate ROM addresses.

Socket Selection

The socket (or ROM) selection logic (Figure 2) consists of two decoders (E30 and E35) that provide the outputs used to select the high byte and low byte sockets. The user can program A10 H and A14 H inputs to these decoders by selecting jumper wires W1-W4 and W9-W12 to determine the configuration designation described in Table 2. The

SB1 L and SB2 L outputs are used to select the 4K of diagnostic/bootstrap DIGITAL programs. The SE1 L and SE2 L outputs are used to select the 2K words of user PROM. The SP1 L to SP8 L outputs are used to select the additional 16K words of user ROM.



74S138 TRUTH TABLE

G1	G2	C	B	A	OUT LOW
H	L	L	L	L	Y0 (SP8 L)
		L	L	H	Y1 (SP7 L)
		L	H	L	Y2 (SP6 L)
		L	H	H	Y3 (SP5 L)
		H	L	L	Y4 (SP4 L)
		H	L	H	Y5 (SP3 L)
		H	H	L	Y6 (SP2 L)
		H	H	H	Y7 (SP1 L)

74LS139 TRUTH TABLE (EACH HALF)

G	B	A	OUT LOW
L	L	L	YO(SB1 L)
	L	H	Y1 (SB2 L)
	H	L	Y2 (SE1 L)
	H	H	Y3 (SE2 L)

MA 1348

Figure 2 Socket Selection Logic

ROM Address

The ROM address logic uses the socket select logic outputs and address lines A0 to A10 to select the desired address. The diagnostic/bootstrap ROMs are enabled by SB1 L and SB2 L and are addressed by A0 to A10. The user EPROMs are enabled by SE1 L and SE2 L and are addressed by A0 to A9. The user ROM sockets are enabled by SP1 L to SP8 L and addressed by A0 to A9. The output data from the ROMs is sent to the data selector logic.

Data Selector

The data selector receives data from the ROMs and the registers of the BDV11. This data is stored until the outputs are enabled by XMIT. The data is then gated to the DAL0-15 bus lines where it is transferred to the LSI-11 bus by the transceiver and control logic.

Display

The display logic consists of four flip-flops and four LEDs. The contents of the display register (address 177524) are gated into the flip-flops and the outputs light the display LED indicators. The pattern of the display indicates to the user the type of program error when a failure occurs.

Power-up

The power-up logic includes the ENABLE/HALT switch and the RESTART switch. In normal operation, the ENABLE/HALT switch is in the ENABLE position. When the switch is placed in the HALT position, the bus signal BHALT L is asserted. The processor enters the halt mode and responds to the console ODT commands. To resume processor operation, the user must set the switch to ENABLE and enter a "P" command from the console.

The RESTART switch must be cycled to reboot the system. When the switch is cycled, a capacitor is charged to disable the bus BDCOK H signal and DCNOK L is asserted to initialize the BDV11 registers. When the capacitor discharges, the BDCOK H signal is enabled, the processor carries out a power-up sequence, and normal operation is resumed.

BVENT

The BVENT logic uses a switch located in E21 that lets the user control the LTC function. When the switch is open, the bus BVENT L signal can be controlled by the LTC signal generated in the LSI-11 bus power supply. When the switch is closed, the BVENT L signal can be controlled by the program.

CONFIGURATION

General

The BDV11 is factory-configured (Group A in Table 2) by DIGITAL to let the user expand the diagnostic and bootstrap programs by adding 2K words of EPROM and 16K words of ROM/EPROM memory. The user can modify the configuration for his own software requirements. Thirteen jumper wires are located on the module as shown in Figure 3 and identified in Table 1. Eight are used for selecting sockets, and five are used to accommodate various types of memory chips. The switches used to select programs are listed in the Programming section below.

Socket Selection

The socket selection logic is controlled by jumpers W1-W4 and W9-W12, which can be configured in seven different ways, as shown in Table 2. Group A assigns the PCR pages and socket selections. Groups B-G let the user choose where to begin program execution, such as having the processor execute instructions directly from a system ROM or EPROM when power is turned ON, rather than from the diagnostic/bootstrap ROM.

Table 1 Selectable Jumpers

Jumper	Function
W1	Socket selection
W2	Socket selection
W3	Socket selection
W4	Socket selection
W5	Chip selection
W6	Chip selection
W7	Chip selection
W8	Chip selection
W9	Socket selection
W10	Socket selection
W11	Socket selection
W12	Socket selection
W13	Chip selection

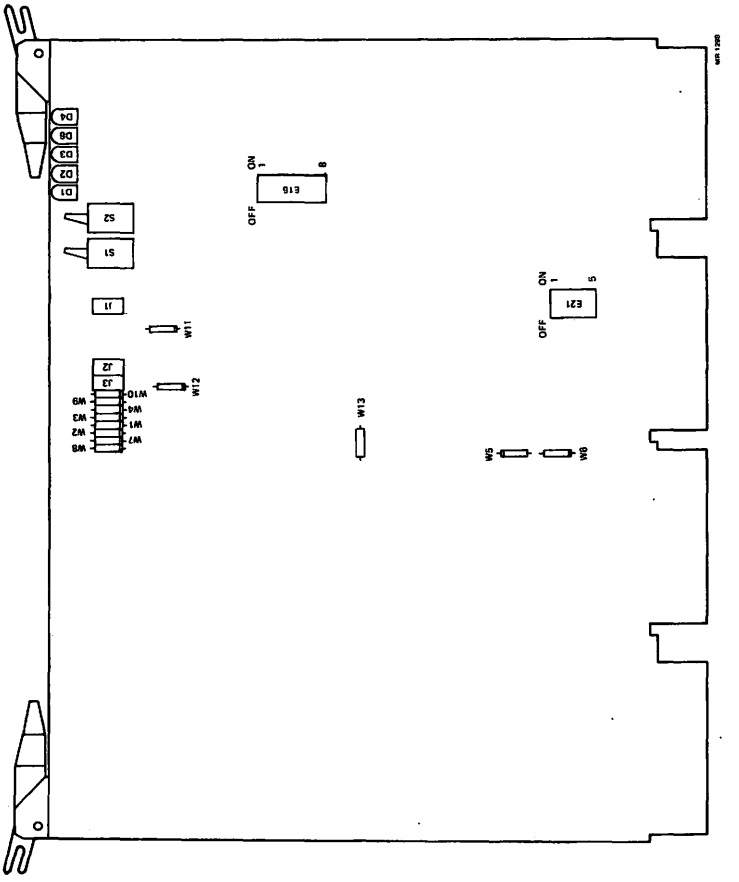


Figure 3 BDV11 Switch and Jumper Locations

Table 2 Memory Configuration

High Byte Socket	Low Byte Socket	Configuration Designation	ROM Address	PCR Page	Selection Signal
4K Diagnostic/Bootstrap (DIGITAL)					
E53	E48	A	0-2K	0-17	SB1 L
(2)	(1)	B	4K-6K	40-57	SB1 L
		C	16K-18K	200-217	SB1 L
		D	20K-22K	240-257	SB1 L
E58	E44	A	2K-14K	20-37	SB2 L
(4)	(3)	B	6K-8K	60-77	SB2 L
		C	18K-20K	220-237	SB2 L
		D	22K-24K	260-277	SB2 L
2K User EPROM					
E57	E40	A	4K-5K	40-47	SE1 L
(3)	(1)	B	0-1K	0-7	SE1 L
		C	20K-21K	240-247	SE1 L
		D	16K-17K	200-207	SE1 L
E52	E36	A	5K-6K	50-57	SE2 L
(4)	(2)	B	1K-2K	10-17	SE2 L
		C	21K-22K	250-257	SE2 L
		D	17K-18K	210-217	SE2 L

Table 2 Memory Configuration (Cont)

High Byte Socket	Low Byte Socket	Configuration Designation	ROM Address	PCR Page	Selection Signal
16K User ROM					
E54	E49	A	16K-18K	200-217	SP8 L
(2)	(1)	E	16K-17K	200-207	SP8 L
		F	0-2K	0-17	SP8 L
		G	0-1K	0-7	SP8 L
E59	E45	A	18K-20K	220-237	SP7 L
(4)	(3)	E	18K-19K	220-227	SP7 L
		F	2K-4K	20-37	SP7 L
		G	2K-3K	20-27	SP7 L
E60	E41	A	20K-22K	240-257	SP6 L
(6)	(5)	E	18K-19K	240-247	SP6 L
		F	4K-6K	40-57	SP6 L
		G	4K-5K	40-47	SP6 L
E55	E37	A	22K-24K	260-277	SP5 L
(8)	(7)	E	22K-23K	260-267	SP5 L
		F	6K-8K	60-77	SP5 L
		G	6K-7K	60-67	SP5 L

Table 2 Memory Configuration

High Byte Socket	Low Byte Socket	Configuration Designation	ROM Address	PCR Page	Selection Signal
16K User ROM (cont)					
E51	E38	A	24K-26K	300-317	SP4 L
(10)	(9)	E	17K-18K	210-217	SP4 L
		F	8K-10K	100-117	SP4 L
		G	1K-2K	10-17	SP4 L
E47	E42	A	26K-28K	320-337	SP3 L
(12)	(11)	E	19K-20K	230-237	SP3 L
		F	10K-12K	120-137	SP3 L
		G	3K-4K	30-37	SP3 L
E43	E46	A	28K-30K	340-357	SP2 L
(14)	(13)	E	21K-22K	250-257	SP2 L
		F	12K-14K	140-157	SP2 L
		G	5K-6K	50-57	SP2 L
E39	E50	A	30K-32K	360-377	SP1 L
(16)	(15)	E	23K-24K	270-277	SP1 L
		F	14K-16K	160-177	SP1 L
		G	7K-8K	70-77	SP1 L

NOTE

The parenthetical numbers in the socket colums indicate the order for installing each ROM.

Memory Configuration

The user can change the configuration of the BDV11 memory structure by using socket selection jumpers W1-W4 and W9-W12; the standard configuration is designated "A" in Table 2. This table also indicates the installation order for the PROM/ROM chips. The B, C, D, E, F, and G configurations show as alternate ways the user can map the ROM memory. Details about selecting a configuration using the socket selection jumpers are shown below.

Configuration	Socket Selection Jumpers*							
Designation	**W1**	**W2**	**W3**	**W4**	**W9**	**W10**	**W11**	**W12**
A	R	I	I	R	I	R	R	I
B	X	X	X	X	I	R	I	R
C	X	X	X	X	R	I	R	I
D	X	X	X	X	R	I	I	R
E	I	R	I	R	X	X	X	X
F	R	I	R	I	X	X	X	X
G	I	R	R	I	X	X	X	X

* I = Installed, R = Removed, X = Irrelevant

Chip Selection

The system ROM sockets can be occupied by either 2K ROMs or 1K ROMs. The ROM socket logic uses jumpers W5-W8 and W13 to select the type of ROM that can be used on the BDV11. Table 3 shows jumper configurations and the type of ROM or PROM used with these configurations.

Control Registers

The BDV11 module has five hardware registers that are software-addressable. These registers are assigned individual addresses that *cannot be changed or modified.* The registers are described in the following paragraphs; their designations and addresses are listed in Table 4.

Page Control Register (PCR) — This register is word- or byte-addressable and can be read or written. The PCR is a 16-bit register that consists of two 8-bit bytes. The low byte consists of bits 0-7 and the high byte consists of bits 8-15. When the low byte of the PCR is equal to page 6, then bus addresses 173000-173777 accesses the 128 ROM locations in the block 1400-1577. When a bus address falls in this range, the logic considers only the low byte of the PCR. However, if the bus address is in the range 173400-173777, only the high byte of the PCR is used to select the ROM location.

Table 3 Chip Selection Jumpers

	Jumpers Inserted[1]				
ROM Type	**W5**	**W6**	**W7**	**W8**	**W13**
2708[2]	R	I	R	I	R
2716[3]	R	R	I	R	I
8316E[4]	I	R	I	R	R
8316E[5]	R	R	I	R	I

NOTES

1. I = Inserted; R = Removed.
2. CB2 and DB2 must be supplied with external −5 V power.
3. Use only +5 Vdc type components.
4. Chip select signals must be programmed as follows:

CS1	CS2	CS3
LOW	LOW	LOW

5. Chip select signals must be programmed as follows:

CS1	CS2	CS3
LOW	LOW	HIGH

Table 4 Standard Assignments

Register	Read/ Write	Size	Address
Page Control	R/W	16 bits	177520
Read/Write	R/W	16 bits	177522
Configuration*	R	12 bits	177524
Display*	W	4 bits	177524
BEVNT*	W	1 bit	177546

* Dual-purpose register.

Table 5 relates the PCR contents to the PCR page for pages 0-17. If the PCR is loaded with data 000400, the PCR low byte contains data 000, while the high byte contains data 001. The PCR bytes can be loaded separately. To select ROM locations 1600-1777, for instance, one need only load the PCR high byte with page 7; thus, the high byte contains 007, while the low byte can contain anything. Table 6 lists the PCR contents for the remaining PCR pages.

Read/Write Register — This register is used as a maintenance register for the diagnostic programs. The register is cleared when power is turned on or when the RESTART switch is activated.

Configuration Register — This 12-bit read-only register is used to select for execution diagnostics or bootstrap programs for maintenance and system configuration. Bits 0-11 of the register are set by switches E15-1 through E15-8 and E21-1 through E21-4. These switches are associated with BDAL(0:11)L, when an individual switch is closed (on), the corresponding BDAL signal is low (1).

Display Register — This 4-bit register is used for program control of the diagnostic LED display. When bits 0-3 of the register are set, then the corresponding LEDs are off. The register is cleared by turning power ON or by activating the RESTART switch.

Table 5 PCR Contents/Page Relationship, Pages 0-17

PCR Page	PCR Contents	PCR High Byte (Bits 15-8)	PCR Low Byte (Bits 7-0)
0			
1	000400	001	000
2			
3	001402	003	002
4			
5	002404	005	004
6			
7	003406	007	006
10			
11	004410	011	010
12			
13	005412	013	012
14			
15	006414	015	014
16			
17	007416	017	016

Table 6 Pages 20-57, 200-377

Page	Contents	Page	Contents
20,21	010420	260,261	130660
22,23	011422	262,263	131662
24,25	012424	264,265	132664
26,27	013426	266,267	133666
30,31	014430	270,271	134670
32,33	015432	272,273	135672
34,35	016434	274,275	136674
36,37	017436	276,277	137676
40,41	020440	300,301	140700
42,43	021442	302,303	141702

Table 6 Pages 20-57, 200-377 (Cont)

Page	Contents	Page	Contents
44,45	022444	304,305	142704
46,47	023446	306,307	143706
50,51	024450	310,311	144710
52,53	025452	312,313	145712
54,55	026454	314,315	146714
56,57	027456	316,317	147716
200,201	100600	320,321	150720
202,203	101602	322,323	151722
204,205	102604	324,325	152724
206,207	103606	326,327	153726
210,211	104610	330,331	154730
212,213	105612	332,333	155732
214,215	106614	334,335	156734
216,217	107616	336,337	157736
220,221	110620	340,341	160740
222,223	111622	342,343	161742
224,225	112624	344,345	162744
226,227	113626	346,347	163746
230,231	114630	350,351	164750
232,233	115632	352,353	165752
234,235	116634	354,355	166754
236,237	117636	356,357	167756
240,241	120640	360,361	170760
242,243	121642	362,363	171762
244,245	122644	364,365	172764
246,247	123646	366,367	173766
250,251	124650	370,371	174770
252,253	125652	372,373	175772
254,255	126654	374,375	176774
256,257	127656	376,377	177776

BEVNT Register — Setting bit 6 (100_8) removes the clamp from BEVNT, thus enabling the line-time clock. Under program control, the user can clamp the BEVNT line low (thus stopping the line-time clock). Opening the BEVNT switch disconnects this function. The register is cleared (disabling the line-time clock) when the power is turned ON or when the RESTART switch is activated.

PROGRAMMING

General

The BDV11 contains dip switches that let the user select diagnostic and bootstrap programs for execution. Four LEDs indicate when a program fails. A green LED monitors the +12 Vdc and +5 Vdc and is lit when power is ON. A HALT/ENABLE switch and a RESTART switch let the user start and stop the processor. The switches and LEDs are shown in Figure 4.

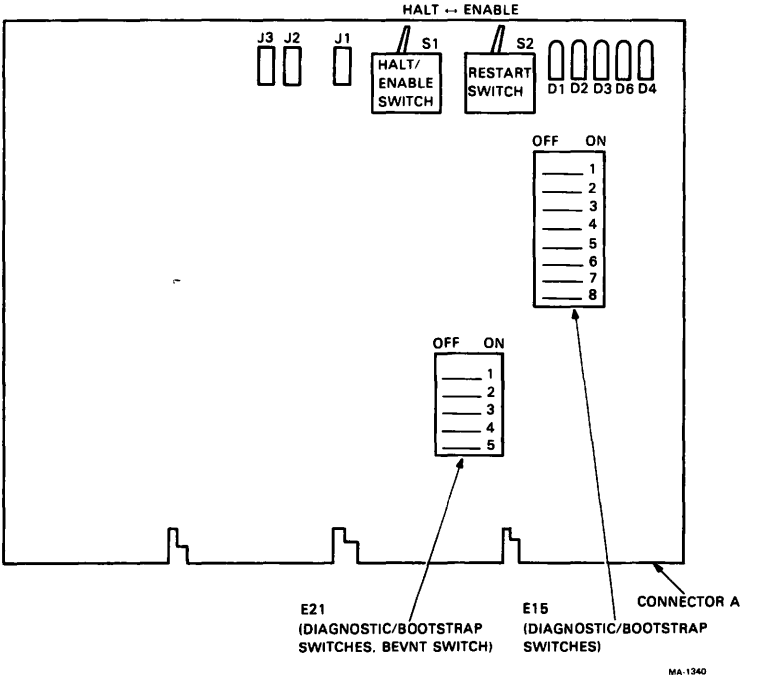


Figure 4 BDV11 Switches and Indicators

Diagnostic/Bootstrap Switches

Dip switch units E15 and E21 let the user select diagnostic programs and/or a bootstrap program. Switches A1-A8 represent switches 1-8

of E15, and switches B1-B4 represent switches 1-4 of E21. The programs selected by these switches are listed below. These 12 switches make up the configuration register that can be read at address 177524.

Switches A1-A4 are defined as follows:

A1	ON	Execute CPU test upon power-up or restart.
A2	ON	Execute memory test upon power-up or restart.
A3	ON	DECnet boot—A4, 5, 6, and 7 are arguments.
A4	ON	Console test and dialogue (A3 OFF).
A4	OFF	Turnkey boot dispatched by switch setting (A3 OFF).

DECnet boot arguments are:

Boot*	A4	A5	A6	A7
DUV11	ON	OFF	OFF	OFF
DLV11-E	OFF	ON	OFF	OFF
DLV11-F	OFF	ON	OFF	ON

All boots other than the DECnet boots above are controlled by the bit patterns in switches A5 through A8 and B1 (shown in Table 7) or, if the console test is selected, by mnemonic and unit number. The console test prompts with

```
xx
START?
```

where xx is the decimal multiple of 1024 words of RAM found in the system when sized from 0 up in 1024-word increments. The first word of each 1024-word segment is read and then written back into itself.

Allowed responses are a 2-character mnemonic with a 1-digit octal unit number or one of two special single character mnemonics. The response must be followed by a RETURN. The special single-character mnemonics are:

Y	Use switch settings to determine boot device
N	Halt—enter microcode ODT

* DLV11-E CSR = 175610; DLV11-F CSR = 176500; DUV11 CSR = 160040 if no devices from 160010 to 160036.

Table 7 Diagnostic/Boostrap Switch Selection

Mnemonic	A5	A6	A7	A8	B1	Program Selected[1]
	0	0	0	0	0	
	0	0	0	0	1	Loop on test
DKn; n<8	0	0	0	1	0	RKV11 Boot
	0	0	0	1	1	
DLn; n<4	0	0	1	0	0	RLV11 Boot
	0	0	1	0	1	
	0	0	1	1	0	
	0	0	1	1	1	
DXn; n<2	0	1	0	0	0	RXV11 Boot
	0	1	0	0	1	
	0	1	0	1	0	
	0	1	0	1	1	
DYn; n<2	0	1	1	0	0	RXV21 Boot
	0	1	1	0	1	
	0	1	1	1	0	
	0	1	1	1	1	
	1	0	0	0	0	ROM Boot[2]
	1	0	0	0	1	
	1	0	0	1	0	
	1	0	0	1	1	
	1	0	1	0	0	
	1	0	1	0	1	
	1	0	1	1	0	
	1	0	1	1	1	
	1	1	0	0	0	
	1	1	0	0	1	
	1	1	0	1	0	
	1	1	0	1	1	
	1	1	1	0	0	
	1	1	1	0	1	
	1	1	1	1	0	
	1	1	1	1	1	

On = 1
Off = 0

1. All unused patterns or mnemonics will default to ROM boot if switch B2, B3, or B4 is on.
2. The ROM boot uses switches B2, B3, and B4 to dispatch as follows:

B2	B3	B4	ROM
1	X	X	Extended diagnostic
0	1	X	2708
0	0	1	Program ROM

where X = Irrevelant

If an unrecognized mnemonic or switch setting (A5 through B1) is encountered, B2, B3, and B4 are checked for the presence of additional ROM. If present, the ROM boot is invoked. The mnemonic's first character is placed in the high byte location of 2. Both characters are converted to uppercase with bit 7 cleared. Location 0 is loaded with the binary unit number. If an unrecognized switch setting is encountered instead, a copy of the switches is placed in location 2 with bit 15 set.

If no additional ROM exists, the switch-checking routine will halt or the mnemonic routine will reprompt.

The above features let the user implement additional features or boots in additional ROMs without changing to the base ROMs. If the additional ROM encounters an unrecognized mnemonic, it should load address 173000 into the PC, which will restart the BDV11 base ROM and reprompt.

Diagnostic Lights

When a failure occurs in a diagnostic test or in a bootstrap program, the diagnostic light display indicates the area of the failure as shown in Table 8. A failure causes the error to be indicated by the display and an error halt instruction is carried out by the processor. When entering the halt mode, the processor outputs the PC address at the time of the error on the console terminal. (The actual error address is one word less than the terminal printout.) In the halt mode, the processor responds to console ODT commands and the operator can troubleshoot the error. Table 9 lists the possible address and the cause of some errors.

BEVNT L Switch

Contact 5 of dip-socket switch E21 is the BEVNT L switch. When the switch is off (open), the LSI-11 bus BEVNT L signal can be controlled by the power supply-generated LTC signal. When the switch is on (closed), the LTC function is program-controlled, i.e., a single-bit, write-only register in the logic (address 177546, bit 6) clamps BEVNT L low when the register is cleared. (The register is automatically cleared when the power is turned on or when the RESTART switch is cycled.)

Power OK LED

This green LED is lit when the +12 Vdc supply voltage is greater than +10 V and the +5 Vdc supply voltage is greater than +4 V for normal operating conditions. The +12 Vdc voltage and the +5 Vdc voltage can be measured at the tip jacks as indicated below. (Both J2 and J3 have a 560-ohm resistor in series to prevent damage from a short circuit; use at least a 20,000 ohm/V meter to measure the voltage.)

Jack	Color	Voltage
J1	Black	Ground
J2	Red	+5 Vdc
J3	Purple	+12 Vdc

HALT/ENABLE Switch

When this switch is in the ENABLE position, the processor can operate program control. If the switch is placed in the HALT position, the processor enters the halt mode and responds to console ODT commands. While in the halt mode, the processor can execute single instructions for system maintenance. Program control is reestablished by returning the switch to the ENABLE position and entering a "P" command at the console terminal (providing the contents of register R7 were not changed). Refer to the appropriate processor handbook for a description of console ODT command usage.

Table 8 Diagnostic LED Error Display (D1-D4)*

D4 Bit 3	D3 Bit 2	D2 Bit 1	D1 Bit 0	Comments* (Type of Error)
On	On	On	On	System hung; halt switch on or power-up mode wrong.
Off	Off	Off	On	CPU, fault, or configuration error.
Off	Off	On	Off	Memory error; R1 points to bad location.
Off	Off	On	On	Console SLU will not transmit.
Off	On	Off	Off	Waiting for response from operator.
Off	On	Off	On	Load device fault.
Off	On	On	Off	Secondary boot incorrect (location 0 not a NOP).
Off	On	On	On	DECnet waiting for response from host.
On	Off	Off	Off	DECnet; received done flag set.
On	Off	Off	On	DECnet; message received.
On	Off	On	Off	ROM bootstrap error.

* The light pattern indicates the corresponding test is in progress or failed. Some tests retry (DECnet) and others will halt the CPU (CPU, memory, non-DECnet boots).

Table 9 List of Error Halts

Address of Error	Cause of Error
173 022	Memory error 1. Write address into itself.
173 040	SLU switch selection incorrect. Error in switches.
173 046	SLU error. CSR address for selected device. Check CSR for selected device in floating CSR address area.

Table 9 List of Error Halts (Cont)

Address of Error	Cause of Error
173 050	CP1 error. R0 contains address of error.
173 052	Memory error 2. Data test failed.
173 106	Memory error 3. Write and read bytes failed.
173 202	ROM loader error. Checksum on data block.
173 240	CP4 error. R0 contains address of error.
173 366	ROM loader error. Checksum on address block.
173 402	ROM loader error. Jump address is odd.
173 532	RL device error.
173 634	CPU error 3. R0 points to cause of error.
173 642	In console terminal test, a "no" typed.
173 656	RK device error.
173 656	Switch mode halt. Match was not made with switches.
173 670	Console terminal test. No done flag.
173 706	CPU error 2. R0 points to cause of error.
173 712	RX device error.

RESTART Switch

When the RESTART switch is cycled, i.e., moved from one side to the other and back, the CPU automatically carries out a power-up sequence. Thus, for maintenance purposes, the system can be rebooted at any time.

Addressing ROM on the BDV11 module

A block of 256 LSI-11 bus addresses is reserved to address the ROM locations on the BDV11 module. This block resides in the upper 4K address bank (28K-32K), which is normally used for peripheral-device addressing, and consists of byte addresses 173000-173776.

All 2048 locations in a selected 2K ROM (or 1024 locations in a 1K ROM) can be addressed by just these 256 bus addresses. The logic includes a page control register (PCR) at bus address 177520; the contents of this read/write register determine which specific ROM location is accessed when one of the 256 bus addresses is placed on the BDAL lines. The PCR is loaded with "page" information, i.e., the PCR contents point to 1 of 16 (or 1 of 8) 128-word pages in the selected ROM (16 pages × 128 words = 2048 words). For example, if the PCR contents represent pages 0 and 1, then bus addresses 173000-173776 access ROM locations 0000-0377; if the PCR contents represent pages 10 and 11, then bus addresses 173000-173776 access ROM locations 2000-2377. Table 10 relates bus addresses, PCR pages, and ROM locations.

At the top of each column of PCR pages in Table 10 appear two circuit component designations; column 1, for example, is headed by E53/E48. These designations represent the ROMs and EPROMs that one might find on a BDV11 module. For instance, the BDV11 is supplied with 2K words of diagnostic ROM. The ROM inserted in socket XE53 supplies the high byte (bits 8-15) of these 2K words, while the ROM inserted in socket XE48 supplies the low byte (bits 0-7). To access the BDV11 diagnostic ROM locations, the user must load the PCR with the pages in column 1; thus, when 12 and 13, for example, are loaded into the PCR, diagnostic ROM locations 2400-2777 can be addressed by the LSI-11 BDAL signals. Another variation of the BDV11 could have 1K-word EPROMs inserted in sockets XE57—XE40 (E57 supplies the high byte, while E40 supplies the low byte). To access these EPROM locations, the user would load the PCR with pages in column 3; thus, with 44 and 45 in the PCR, EPROM locations 1000-1377 are accessible.

Table 10 BDV11 Bus Address/PCR Pages

ROM Location Bus Address Accessed	PCR Pages E53/ E48	E58/ E44	E57/ E40	E52/ E36	E54/ E49	E59/ E45	E60/ E41	E55/ E37	E51/ E38	E47/ E42	E43/ E46	E39/ E50
173000-173376 0000-0177	0	20	40	50	200	220	240	260	300	320	340	360
173400-173777 0200-0377	1	21	41	51	201	221	241	261	301	321	341	361
173000-173376 0400-0577	2	22	42	52	202	222	242	262	302	322	342	362
173400-173777 0600-0777	3	23	43	53	203	223	243	263	303	323	343	363
173000-173376 1000-1177	4	24	44	54	204	224	244	264	304	324	344	364
173400-173777 1200-1377	5	25	45	55	205	225	245	265	305	325	345	365
173000-173376 1400-1577	6	26	46	56	206	226	246	266	306	326	346	366
173400-173777 1600-1777	7	27	47	57	207	227	247	267	307	327	347	367

Table 10 BDV11 Bus Address/PCR Pages (Cont)

ROM Location Bus Address Accessed	PCR Pages E53/ E48	E58/ E44	E57/ E40	E52/ E36	E54/ E49	E59/ E45	E60/ E41	E55/ E37	E51/ E38	E47/ E42	E43/ E46	E39/ E50
173000-173376 2000-2177	10	30			210	230	250	270	310	330	350	370
173400-173777 2200-2377	11	31			211	231	251	271	311	331	351	371
173000-173376 2400-2577	12	32			212	232	252	272	312	332	352	372
173400-173777 2600-2777	13	33			213	233	253	273	313	333	353	373
173000-173376 3000-3177	14	34			214	234	254	274	314	334	354	374
173400-173777 3200-3377	15	35			215	235	255	275	315	335	355	375
173000-173376 3400-3577	16	36			216	236	256	276	316	336	356	376
173400-173777 3600-3777	17	37			217	237	257	277	317	337	357	377

As Table 10 implies, the PCR pages are assigned to specific module ROM sockets. Furthermore, the sockets are assigned specific kinds of ROMs, as Table 11 indicates, e.g., the diagnostic/bootstrap ROM can occupy only sockets XE53 and XE48. Thus, a specific ROM can be addressed only when the PCR contains the page or pages assigned to the socket that the ROM occupies. For example, if 2K-word ROMs are inserted in sockets E39 and E50, they can be addressed only when the PCR contains pages 360-377. The page/socket assignments indicated in Table 10 apply to the BDV11 module shipped by DIGITAL. There are eight locations on the BDV11 printed circuit board in which jumpers are inserted selectively to achieve these assignments. The user can change the factory arrangement of these jumpers to cause the CPU to execute instructions directly from a ROM or EPROM of the user's choice when power is turned on, rather than from the diagnostic ROMs.

Table 11 Functions of ROM Sockets

Sockets	ROM Function	Sockets	ROM Function
XE53/XE48	2K Diagnostic/Bootstrap	XE47/XE42	2K System ROM
XE58/XE44	2K Diagnostic/ Bootstrap (reserved for DIGITAL)	XE51/XE38	2K System ROM
XE57/XE40	1K EPROM	XE55/XE37	2K System ROM
XE52/XE36	1K EPROM	XE60/XE41	2K System ROM
XE39/XE50	2K System ROM	XE59/XE45	2K System ROM
XE43/XE46	2K System ROM	XE54/XE49	2K System ROM

Loading ROM into RAM

A utility is provided in the BDV11 firmware which loads user programs from ROM to RAM at specified (and possibly scattered) addresses and transfers control to a specified address. This allows a programmer to write a program (to be stored in ROM) without knowing the BDV11 mapping hardware or having to "ROMize" the program. This utility loads the DIGITAL-reserved space, the 2K EPROM, or the 16K ROM/EPROM areas. The utility uses the four highest words of RAM (<30K) as scratch space.

The format is a modified version of absolute loader paper tape format. The standard format consists of sequential blocks, organized by byte, as follows:

1 BYTE	This indicates start of block.
0 BYTE	Required.
BCL	Low-order eight bits of byte count.
BCH	High-order eight bits of byte count.
ADL	Low-order eight bits of load address.
ADH	High-order eight bits of load address.
DATA	Sequential bytes of data.
CKB	Checksum byte.

These frames are repeated as required until a starting address block is encountered. This is indicated by a byte count of six, which is too short to allow a data field. The load address of this block is used as the starting address.

The format skips every 255th and 256th location in the ROM pattern. These locations are filled with checking information which allows DIGITAL diagnostics to determine whether the ROMs are good and inserted in the correct socket.

The ROMs should be inserted as indicated by the ROM address chart. The user program may be patched by changing only the last ROM of a set and by adding a new data block(s) before the starting address block. This block will overlay previously loaded data.

Executing ROMs in the I/O Page

ROMs may be executed in the I/O page provided their starting address is between 173016 and 173376. The next page lists a program which executes in the I/O page. It uses the ROM loader but supplies only a starting address block. It must start in the window between 173000 and 173376 since the ROM boot is executing out of the other window. It is the programmer's responsibility to properly map the upper window and then manage all remapping.

DCK11-AA, -AC PROGRAM TRANSFER INTERFACE

GENERAL

The DCK11-AA and -AC CHIPKITs provide the logic necessary for a program transfer interface to the LSI-11 bus.

The DCK11-AA kit contains:

1-DC003 Interrupt Chip
1-DC004 Protocol Chip
4-DC005 Transceiver/Address Decoder/Vector Select Chips

The DCK11-AC kit contains the above chips plus:

1-W9512 double-height, extended-length, high-density wire-wrappable module
1-BC07D-10 ten-foot, 40-conductor plug-in cable

Figure 1 shows a schematic of the program control CHIPKIT part of a user's interface.

FEATURES

DC003 Interrupt Logic IC Features

- Two interrupts (A & B) per DC003
- Interrupt enable flip-flop on the IC
- Enable flip-flop outputs available to the user
- Interrupts initially disabled by BUS INIT
- VECTOR output to the DC005s to gate the Interrupt Vector address directly onto the LSI-11 bus
- Interrupt B generates the second LSB of vector address directly (VECRQST B H)
- BUS INIT buffered and made available to the user (INITO L)
- Contains logic for LSI-11 bus "daisy-chained" interrupts

DC004 Protocol Logic IC Features

- Device selection features
  - Four register select lines (SEL 6 L, SEL 4 L, SEL 2 L, SEL 0 L)
  - High and low byte output select lines (OUTHB L, OUTLB L)
  - Input select line (INWD L)
  - Enable input from higher level decode (ENB H)
- Bus functions
  - Bus reply generated for device addresses and for interrupts (BRPLY L)
  - Ability to vary bus reply response by adding an RC network provided (RXCX H)

DC005 Bus Transceiver IC Features

- Four bits per IC
- Three bits of address selection logic included on the chip
- LSI-11 bus drivers and receivers
  - Drivers—open collector with 70 mA sink capability.
  - Receiver—65 μA input loading. (BUS 0-3L)
- Internal 3-state bus drivers and receivers
  - Drivers—20 mA sink
  - Receivers—standard TTL (DAT 0-3 H)
- Address selection
  - Enable input for use with a higher level decoded input (MENB L)
  - Address bits may be excluded from comparison by tying them to VCC (JA(3:1)L)
- Interrupt Vector
  - Vector address bits "ORed" directly onto LSI-11 bus (JV(3:1)H)

SPECIFICATIONS

For complete Electrical Specifications refer to EJ 17475. A summary of the more important specifications follow the pin/signal descriptions for individual ICs.

DC003 Pin/Signal Descriptions

Pin	Signal	Description
1	VECTOR H	Interrupt Vector Gating. This signal should be used to gate the appropriate vector address onto the bus and to form the bus signal called BRPLY L. **Type:** TTL-OUTPUT
2	VECRQSTB H	Vector Request "B." When asserted, indicates RQST "B" service vector address is required. When unasserted, indicates RQST "A" service vector address is required. VECTOR H is the gating signal for the entire vector address; VECRQSTB H is normally bit 2 of the vector address. **Type:** TTL-OUTPUT

DC003 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
3	BDIN L	Bus Data In. This signal, generated by the processor BDIN, always precedes a BIAK signal. **Type:** BUS-INPUT
4	INITO L	Initialize Out. This is the buffered BINIT L signal used in the device interface for general initialization. **Type:** OPEN COLLECTOR WITH 1K PULL UP - OUTPUT
5	BINIT L	Bus Initialize. When asserted, this signal brings all driven lines to their unasserted state (except INITO L). **Type:** BUS-INPUT
6	BIAKO L	Bus Interrupt Acknowledge (Out). This signal is the daisy-chained signal that is passed by all devices not requesting interrupt service (see BIAKI L). Once passed by a device, it must remain passed until a new BIAKI L is generated. **Type:** BUS-OUTPUT
7	BIAKI L	Bus Interrupt Acknowledge (In). This signal is the processor's response to BIRQ L true. This signal is daisy-chained such that the first requesting device blocks the signal propagation while non-requesting devices pass the signal on as BIAKO L to the next device in the chain. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device. **Type:** BUS-INPUT
8	BIRQ L	Bus Interrupt Request. This signal is generated when this device needs to interrupt the processor. The request is generated by a false to true transition of the RQST signal along with the associated true interrupt enable signal. The request is removed after the acceptance of the BDIN L signal and on the leading edge of the BIAKI L signal or the removal of the associated request signal. **Type:** BUS-OUTPUT

DC003 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
10 17	RQSTB H RQSTA H	Device Interrupt Request. When asserted with the enable flip-flop set, will cause the assertion of BIRQ L on the bus. This signal line normally remains asserted until the request is serviced. **Type:** BUS-INPUT
11 16	ENBST H ENAST H	Interrupt Enable Status. This signal indicates the state of the interrupt enable internal flip-flop which is controlled by the signal ENX (where X is either A or B) DATA H, and the ENX (where X is either A or B) CLK H clock line. **Type:** TTL-OUTPUT
12 15	ENBDATA H ENADATA H	Interrupt Enable Data. The level on this line, in conjunction with the ENX (where X is either A or B) CLK H signal, determines the state of the internal interrupt enable flip-flop. The output of this flip-flop is monitored by the ENX (where X is either A or B) ST H signal.**Type:** TTL-INPUT
13 14	ENBCLK H ENACLK H	Interrupt Enable Clock. When asserted (on the positive edge), interrupt enable flip-flop assumes the state of the ENX (where X is either A or B) DATA H, signal line. **Type:** TTL-INPUT

Summary of Electrical Specifications for DC003

Ambient Temperatures	0°C to 70°C
TTL Input	
High-level input current	50 μA max. I_{IH}(V=2.7V)
Low-level input current $I_{IL}(V_I=0.5V)$	−.55 mA max.
Exceptions	Pins 12 & 15 ENX DATA H I_{IH} = 100 μA max. I_{IL} = −2.0 mA max.

TTL Outputs

High-level output voltage V_{OH} (I_O = −1 mA max.)	2.7V min.
Low-level output voltage V_{OL} (I_O = 20 mA max.)	0.5V max.

Bus (Hi Z) Input and (open collector) outputs.

Bus Inputs

High-level input current I_{IH} (V_I = 3.8V)	40μA max.
Low-level input current I_{IL} (V_I = 0V)	−10μA max.

Bus Outputs

Low-level output voltage V_{LO} (I_{sink} = 70 mA max.)	0.8V max.

DC004 Pin/Signal Descriptions

Pin	Signal	Description
1	VECTOR H	Vector. This input causes BRPLY L to be generated through the delay circuit. Independent of BSYNC L and ENB H. **Type:** TTL-INPUT
2 3 4	BDAL2 L BDAL1 L BDAL0 L	Bus Data Address Lines. These signals are latched at the assert edge of BSYNC L. Lines 2 and 1 are decoded for the select outputs; line 0 is used for byte selection. **Type:** BUS-INPUTS
5	BWTBT L	Bus Write/Byte. While the BDOUT L input is asserted, this signal indicates a byte or word operation: asserted = byte, unasserted = word. Decoded with BDOUT L and latched BDAL0 L to form OUTLB L and OUTHB L. **Type:** BUS-INPUT

DC004 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
6	BSYNC L	Bus Synchronize. At the assert edge of this signal, address information is trapped in four latches. While unasserted, disables all outputs except the vector term of BRPLY L. **Type:** BUS-INPUT
7	BDIN L	Bus Data In. This is a strobing signal to effect a data input transaction. Generates INWD L and BRPLY L through the delay circuit and INWD L. **Type:** BUS-INPUT
8	BRPLY L	Bus Reply. This signal is generated through an RC delay by VECTOR H, or BDIN L, or BDOUT L and the AND of BSYNC L and latched ENB H. **Type:** BUS-OUTPUT
9	BDOUT L	Bus Data Out. This is a strobing signal to effect a data output transaction. Decoded with BWTBT L and BDAL0 to form OUTLB L and OUTHB L. Generates BRPLY L through the delay circuit. **Type:** BUS-INPUT
11	INWD L	In Word. Used to gate (read) data from a selected register onto the data bus. Enabled by BSYNC L and strobed by BDIN L. **Type:** TTL-OUTPUT
12 13	OUTLB L OUTHB L	Out Low Byte. Out High Byte. Used to load (write) data into the lower, higher, or both bytes of a selected register. Enabled by BSYNC L and decode of BWTBT L and latched BDAL0 L, and strobed by BDOUT L. **Type:** TTL-OUTPUT
14 15 16 17	SEL0 L SEL2 L SEL4 L SEL6 L	Select Lines. One of these four signals is true as a function of BDAL2 L and BDAL1 L if ENB H is asserted at the asserted edge of BSYNC L. They indicate that a word register has been selected for a data transaction. These signals never become asserted except at the assertion of BSYNC L (then only

DC004 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
		if ENB H is asserted at that time) and once asserted, are not unasserted until BSYNC L becomes unasserted. **Type:** TTL-OUTPUT
18	RXCX H	External Resistor Capacitor Node. This node is provided to vary the delay between the BDIN L, BDOUT L, or VECTOR H inputs and BRPLY L output. The external resistor should be tied to V_{CC} and the capacitor to ground. As an output, it is the logical inversion of BRPLY L. **Type:** OPEN-COLLECTOR OUTPUT
19	ENB H	Enable. This signal is latched at the asserted edge of BSYNC L and is used to enable the select outputs and the address term of BRPLY L. **Type:** TTL-INPUT WITH 850Ω PULL UP

Summary of Electrical Specifications for DC004

Ambient Temperatures	0°C to 70°C
TTL Inputs	
High level input current	
I_{IH} (V_I = 2.7V)	50 μA max.
Low level input current	
I_{IL} (V_I = 0.5V)	−.70 mA max.
Exceptions	Pin 19 ENB H I_{IH} = −3.85 mA max. I_{IL} = −8.0 mA max.
TTL Outputs	
High Level output voltage	
V_{OH} (I_O = −1 mA)	2.7V min.
Low level output voltage	
V_{OL} (I_O = 20 mA)	0.5V max.
Bus (Hi-Z) Inputs and (Open Collector) Outputs	
Bus inputs	

High level input current I_{IH} (V_I = 3.8V)	40 μA max.
Low level input current I_{IL} (V_I = 0V)	−10 μA max.
Bus Outputs Low level output voltage V_{LO} (I_{sink} = 70 mA)	0.8V max.

DC005 Pin/Signal Descriptions

Pin	Signal	Description
	BUS(3:0) L	
12	BUS0 L	Bus Data. This set of four lines constitutes
11	BUS1 L	the bus side of the transceiver. Open collec-
9	BUS2 L	tor outputs; high-impedance inputs. Low=
8	BUS3 L	1. **Type:** BUS-INPUT/OUTPUT
	DAT(3:0) H	
18	DAT0 H	Peripheral Device Data. These four tri-state
17	DAT1 H	lines carry the inverted received data from
7	DAT2 H	BUS (3:0) when the transceiver is in the re-
6	DAT3 H	ceive mode. When in transmit data mode, the data carried on these lines are passed inverted to BUS (3:0). When in the disabled mode, these lines go open (HI-Z). High = 1. **Type:** TTL-INPUTS
	JV(3:1) H	Vector Jumpers. These inputs, with internal
14	JV1 H	pull-down resistors, directly drive BUS
15	JV2 H	(3:1). A low or open on the jumper pin will
16	JV3 H	cause an open condition on the corres- ponding bus pin if XMIT H is low. A high will cause a one (low) to be transmitted on the bus pin. Note that BUS0 L is not controlled by any jumper input. **TYPE:** TTL-INPUT WITH PULL DOWN
13	MENB L	Match Enable. A low on this line will enable the Match output. A high will force MATCH low, overriding the MATCH circuit. **TYPE:** BUS-INPUT

DC005 Pin/Signal Descriptions (Cont)

Pin	Signal	Descriptions
3	MATCH H	Address Match. When BUS (3:1) match with the state of JA (3:1) and MENB L is low, this output is open; otherwise it is low. **TYPE:** BUS-OUTPUT
	JA(3:1) L	Address Jumpers. A strap to ground on these inputs will allow a match to occur with a 1 (low) on the corresponding BUS line; an open will allow a match with a 0 (high); a strap to V_{CC} will disconnect the corresponding address bit from the comparison. **TYPE:** TERNARY-INPUT (SEE TEXT)
1	JA1 L	
2	JA2 L	
19	JA3 L	
5	XMIT H	Control Inputs. These lines control the operation of the transceiver as follows:
4	REC H	

REC	XMIT	
0	0	DISABLE:BUS,DAT open
0	1	XMIT DATA:DAT→BUS
1	0	RECEIVE:BUS→DAT
1	1	RECEIVE:BUS→DAT

To avoid 3-state signal overlap conditions, an internal circuit delays the change of modes between XMIT DATA and RECEIVE mode and delays 3-state drivers on the DAT lines from enabling. This action is independent of the DISABLE mode.

Summary of Electrical Specifications for DC005

Ambient Temperatures	0°C to 70°C
TTL Inputs	
High level input current I_{IH} (V_I = 2.7V)	—
REC H Pin 4	100 μA max.
XMIT H Pin 5	50 μA max.
Low level input current I_{IL} (V_I = 0.5V)	—

REC H Pin 4	−2.2 mA max.
XMIT H Pin 5	−1.1 mA max.

TTL Outputs

High Level output voltage V_{OH} (I_O = −1 MA)	3.65V min.
Low level output voltage V_{OL} (I_O = 20 mA)	0.5V max.

Bus (HI-Z) Inputs and (Open Collector) Outputs

Bus inputs

High level input current I_{IH} (V_I = 3.8V)	65 μA max.
Low level input current I_{IL} (V_I = 0.5V)	−10 μA max.

Bus Outputs

Low level output voltage V_{LO} (I_{sink} = 70 mA)	0.8V max.

DESCRIPTION

PROGRAM CONTROL CHIPKIT APPLICATION

In Figure 1, the transceivers (four DC005s) provide data lines D0 through D15 to reflect the state of the bus lines BDAL 0-15, when REC H is asserted, and to drive the BDAL lines when XMIT is asserted. Address and interrupt vector information for interrupt request and device selection is also provided by the DC005. The device address is set up using input lines A3 through A12, while the interrupt vector address is set up using input lines V3 through V8.

When the address lines (JA inputs on DC005s) match the state of the associated BDAL lines, the MATCH output will float high such that all DC005s will let ENB H on the DC004 be asserted, thus enabling the DC004 to look for proper synchronizing signals from the bus. Once these synchronizing signals (BDIN, BDOUT, BSYNC, and BWTBT) are present, the DC004 generates the control signals (INWD, OUTHB, OUTLB, and SEL 0, 2, 4, 6) for the user's device.

The protocol logic (DC004) functions as a register selector to provide

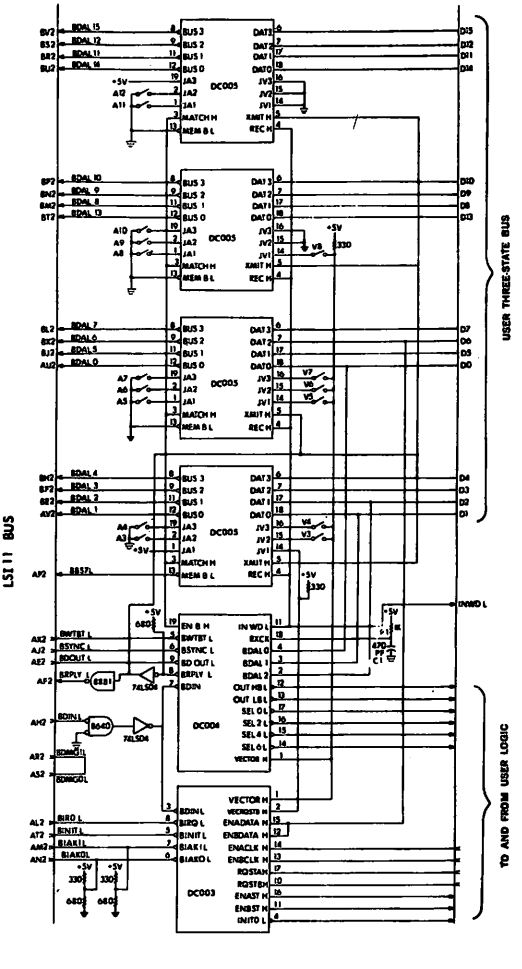
the signals necessary to control data flow into and out of the user's registers. When the proper device address has been decoded by the device address comparator (all DC005s), the MATCH outputs let the ENBH input go high, thus enabling the DC004 protocol logic. Address bits D01 H and D02 H are decoded by the protocol logic, producing one of the SEL outputs, while bit D0 and BWTBT are decoded for output word/byte selection (OUTHB L, OUTLB L). The device select line (SEL 0, 2, 4, 6) and word/byte select lines (INWD L, OUTHB L, OUTLB L) are used by the user's logic. Each SEL output is used to select one of four user's registers, and the word/byte lines are used to determine the type of transfer (word or byte) to or from these registers.

Either BDIN L or BDOUT L, depending on the type of bus cycle, will initiate a delay whose value is dependent on the time constant of the RC network connected to pin RXCX H of the DC004. The end of this delay will initiate a reply to the CPU indicating that the address has been received.

The interrupt logic (DC003) performs an interrupt transaction. Two channels (A and B) are provided for generating two interrupt requests, with channel A having the highest priority. The interrupt enable flip-flop within the interrupt logic must first be set when the user's device is to interrupt the LSI-11. This is accomplished by asserting (logic H) the ENX DATA* line and then clocking the enabled flip-flop by asserting the ENX CLK* line. With the interrupt enable flip-flop set, the user's device may then make an interrupt request by asserting (logic H) RQSTX*. When RQST is asserted and the interrupt enable flip-flop is set, the interrupt logic asserts BIRQ L to the bus which initiates the bus "handshake" operation. This operation terminates with the generation of the vector address by the DC005 under the control of the DC003, and it's signals VECTOR H and VECRQSTB H.

The interrupt logic available to the user indicates the status of the interrupt logic enable flip-flops. Each line is asserted (logic H) when the appropriate interrupt enable flip-flop is set. These status lines can function as part of the user's control status register (CSR). The VECRQSTB H line is asserted (logic H) when the device connected to channel B has been granted use of the bus for interrupt vector transfer operation. When VECRQSTB H is unasserted (logic L), the user's device connected to channel A of the interrupt logic has been granted use of the bus. The INITO L output from the interrupt logic can be used to initialize the user's logic.

* X may be either A or B depending on which half of the interrupt logic is being enabled.



NOTE:

CLOSE SWITCH FOR ONE
OPEN SWITCH FOR ZERO

Figure 1 DCK11 Bus Interface Typical Application

DC003 Interrupt Logic (DEC #19-12730-00)

The interrupt chip is an 18-pin, 0.762 cm center × 2.349 cm long (max) (0.3 in. center × 0.925 in. long) dual-in-line-package (DIP) device that provides the circuits to perform an interrupt transaction in a computer system that uses a daisy-chain type of arbitration scheme. The device is used in peripheral interfaces to provide two interrupt channels labeled "A" and "B," with the A section at a higher priority than the B section. Bus signals use high-impedance input circuits or high-current open collector outputs, which allow the device to directly attach to the computer system bus. Maximum current required from the V_{CC} supply is 140 mA.

Figure 2 is a simplified logic diagram of the DC003 IC. Table 1 describes the signals and pins of the DC003 by pin and signal name.

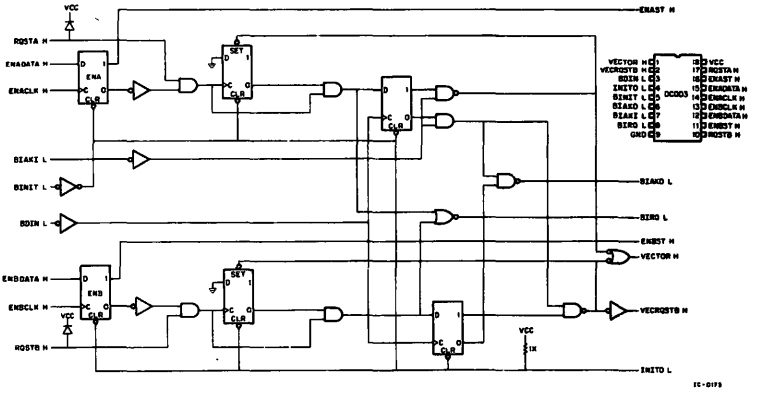


Figure 2 DC003 Simplified Logic Diagram

DC004 Protocol Logic (DEC #19-12729-00)

The protocol chip is in a 20-pin 0.762 cm center × 2.74 cm long (0.3 in. center × 1.08 in. long) DIP device that functions as a register selector, providing the signals to control the data flow into and out of up to four word registers (eight bytes). Bus signals can directly attach to the device because receivers and drivers are provided on the chip. However, the DC004 is now ordinarily used with the user's three-state bus to limit Bus loading. An RC delay circuit is provided to slow the response of the peripheral interface to data transfer requests. The circuit is designed such that if tight tolerance is not required, then only an external 1K ±20 percent resistor is necessary. External RCs can be added to vary the delay. Maximum current required from the V_{CC} supply is 120 mA.

Figure 3 is a simplified logic diagram of the DC004 IC. Signals and pin definitions for the DC004 are presented in Table 2.

NOTE

The pin names shown in this diagram are for the situation where the DC004 is connected to the internal 3-state bus of the DC005s, not connected directly to the LSI-11 bus.

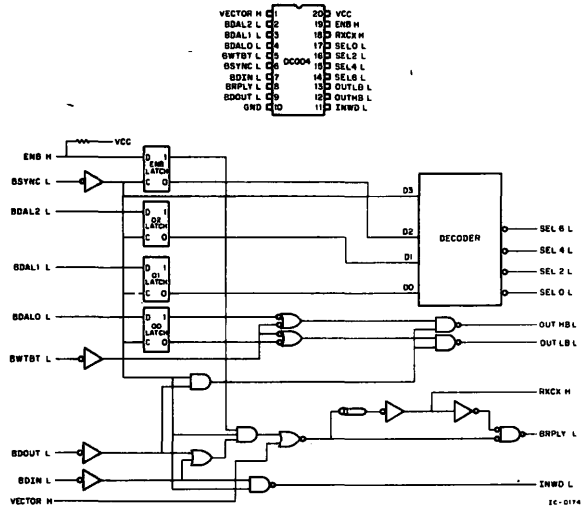


Figure 3 DC004 Simplified Logic Diagram

DC005 Transceiver Logic (DEC #19-13040)

The 4-bit transceiver is a 20-pin, 0.762 cm center × 2.74 cm long (0.3 in. center × 1.08 in. long) DIP, low-power Schottky device; its primary use is in peripheral device interfaces to function as a bidirectional buffer between a data bus and peripheral device logic bus. It also includes a comparison circuit for device address selection and a constant generator for interrupt vector address generation. The bus I/O port provides high-impedance inputs and high drive (70 mA) open collector outputs to allow direct connection to a computer data bus structure. On the peripheral device side, a bidirectional port is also provided, with standard TTL inputs and 20 mA, tri-state drivers. Data on this port are the logical inversion of the data on the bus side.

Three address "jumper" inputs are used to compare against three bus inputs to generate the signal MATCH. The MATCH output is open collector, which allows the output of several transceivers to be wire-ANDed to form a composite address match signal. The address jumpers can also be put into a third logical state that disables jumpers for "don't care" address bits. In addition to the three address jumper inputs, a fourth high-impedance input line is used to enable/disable the MATCH output.

Three vector jumper inputs are used to generate a constant that can be passed to the computer bus. The three inputs directly drive three of the bus lines, overriding the action of the control lines.

Two control signals are decoded to give three optional states: receive data, transmit data, and disable.

Maximum current required from the V_{CC} supply is 120 mA.

Figure 4 is a simplified logic diagram of the DC005 IC. Signal and pin definitions for the DC005 are presented in Table 3.

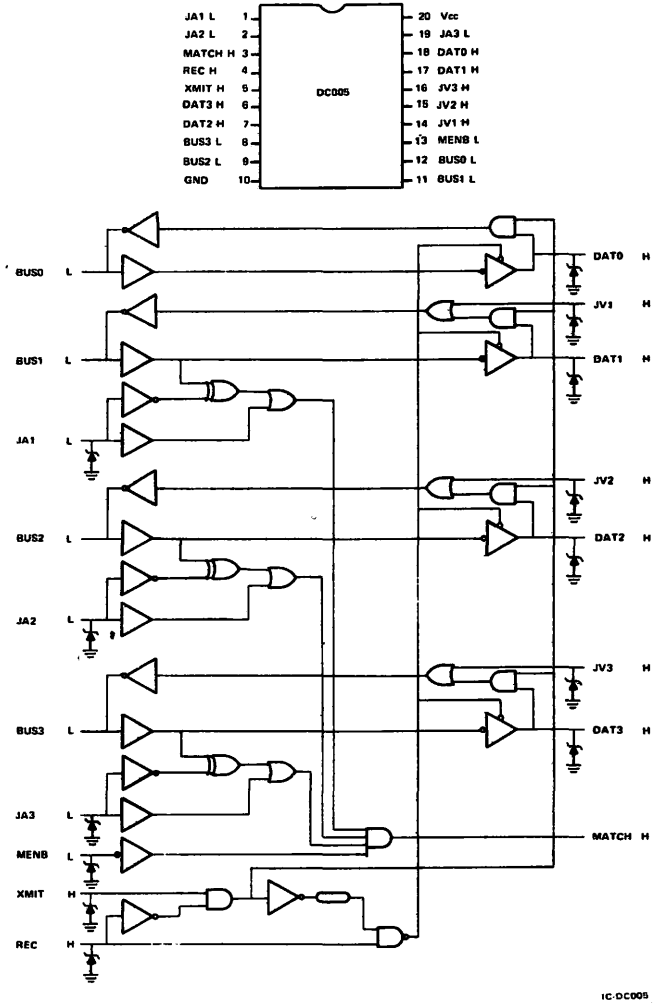


Figure 4 DC005 Simplified Logic Diagram

CONFIGURATION

The drawings on the following pages show sample circuits that may be helpful in applying the CHIPKITS.

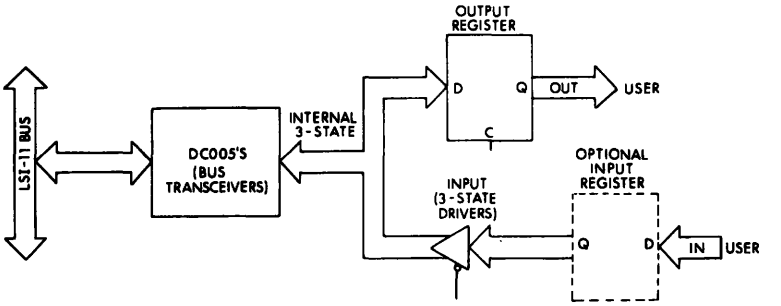


Figure 5 Data Path Flow Diagram

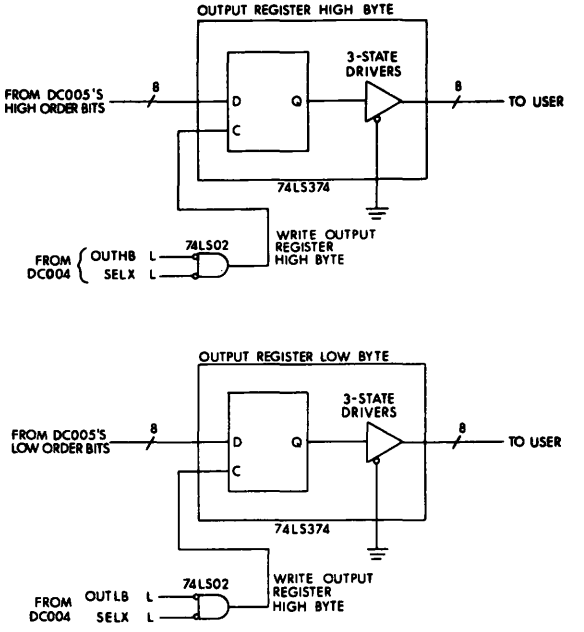


Figure 6 Example of Output Register

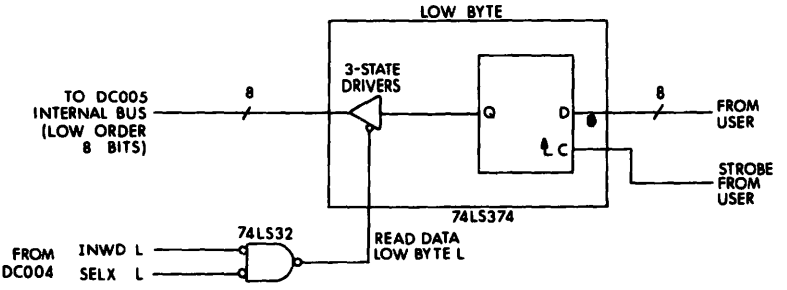


Figure 7. Example of Input Register (BYTE)

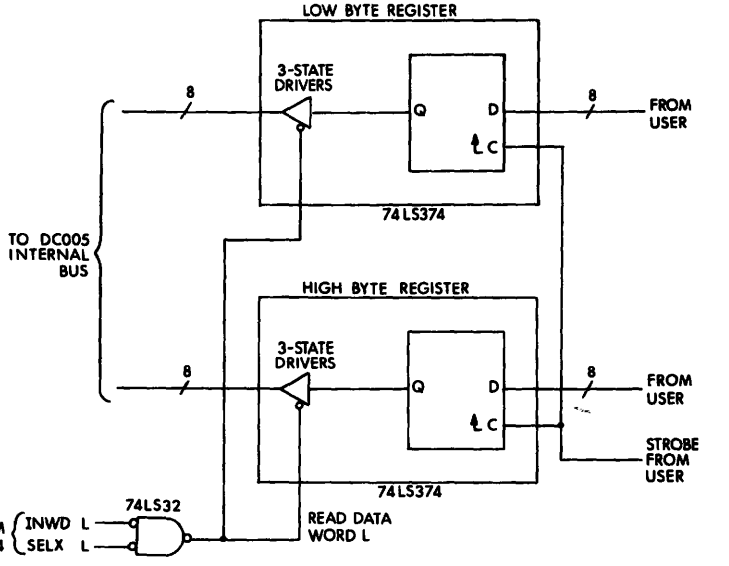


Figure 8 Example of Input Register (WORD)

This example is the interrupt enable bit for interrupt A which connects to bit 6 of the example CSR.

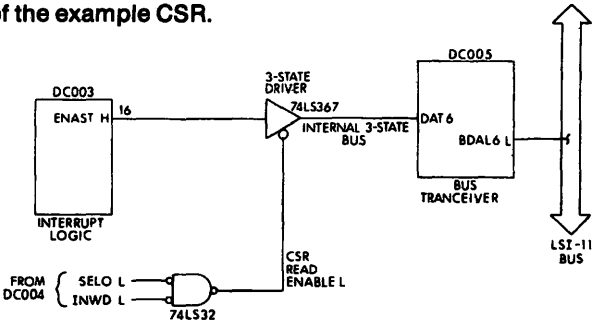
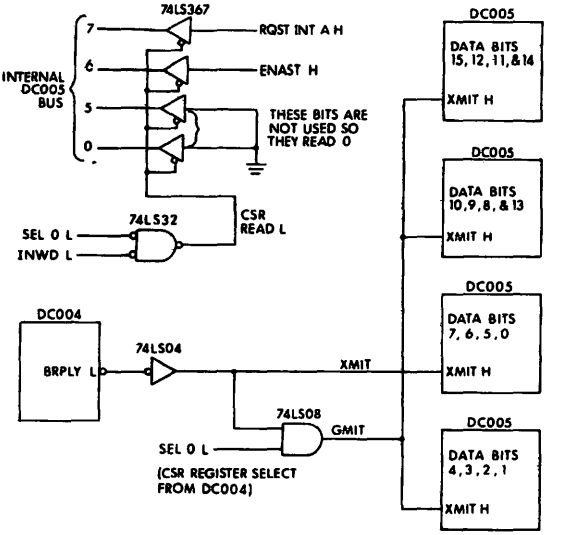


Figure 9 Typical CSR Bit



WHEN THE CSR IS READ (SEL 0 L = 0) THE SIGNAL GMIT WILL BE 0 CAUSING THE UNUSED DC005 BITS TO BE READ AS ZEROS. (HIGH ON BDAL LINES) FOR ANY OTHER REGISTER GMIT = XMIT.

Figure 10 Sample Circuit to Cause Unused CSR Bits to be Read as Zeros

This example is the A interrupt request and a DATA READY status bit (bit 7 of the CSR).

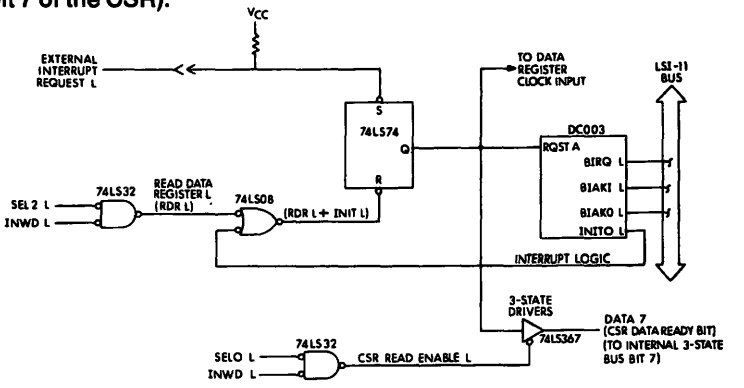


Figure 11 Typical Interrupt Request

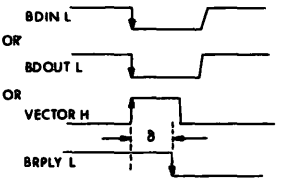
BUS REPLY DELAY TIMES

Bus Reply delays as a function of RC values connected to pin 18 (RXCX H) of the DC004.

k1. RX = 1KΩ 5%
CX = 0
Delay ~ 50 ns from falling edge of BDIN L, or BDOUT L, or rising edge of VECTOR H to BRPLY L falling edge.

2. RX = 1KΩ 5%
CX = 470 pf 5%
Delay as described in item 1 above ~ 200 ns.

3. RX = 10KΩ 5%
CX = 1000 pf 5%
Delay as described above ~ 3.2 μsec



WHERE δ = DELAY DESCRIBED IN ITEMS 1-3

Figure 12

DCK11-AB, -AD

DCK11-AB, -AD DIRECT MEMORY ACCESS INTERFACE

GENERAL

The DCK11-AB and -AD CHIPKITs provide the logic necessary for a Direct Memory Access (DMA) interface to the LSI-11 bus.

The DCK11-AB kit contains:

1-DC003 Interrupt Chip
1-DC004 Protocol Chip
4-DC005 Transceiver/Address Decoder/Vector Select Chips
2-DC006 Word Count/Bus Address Chips
1-DC010 DMA Control Chip

The DCK11-AD kit contains the above chips plus:
1-W9512 double-height, extended-length, high-density wire-wrappable module
1-BC07D-10 ten-foot, 40-conductor plug-in cable

Figure 1 shows a typical interconnection of DMA CHIPKIT components, in block diagram form.

DMA applications use the same chips as program control interfaces, plus two DC006s for word or byte address counters and a DC010 DMA bus control IC.

DC006 Word and Address Counter IC Features

- Two 8-bit counters on each IC
- 16-bit address and word counters available in two ICs cascaded
- Input and output share pins on the 3-state bus
- Read and write control logic located on the IC
- Maximum count decoded and brought out for user

DC010 DMA Logic Features

- Uses an external 8 MHz clock to generate LSI-11 bus signals for DIN, DOUT, SYNC, and SACK
- Inputs allow selection of cycle type (DATI, DATO, DATIO)
- Interfaces with DMA daisy-chain signals
- Allows an external RC network to force a variable wait before the next bus request is made (TMOUT H)
- An input which allows a maximum of four transfers before the bus is released, when enabled (CNT4 H)

DCK11-AB, -AD

SPECIFICATIONS

This section contains a summary of the most important specifications for DC006 and DC010. See the previous section DCK11-AA, -AC for a summary of specifications for DC003, DC004, and DC005.

DC006 Pin/Signal Descriptions

Pin	Signal	Description
6	CNT1A	Count A Counter by 1 (TTL input). This signal controls the least significant bit of the A counter. When CNT1A is low, the A counter increments by one. When high, the LSB is prevented from toggling, hence the counter increments by two. When two counters are cascaded, CNT1A on the high-order counter should be grounded.
3	CLK-A	Clock A Counter (TTL input). This clock signal increments the A counter on its negative edge. The counter is incremented by one or two, depending on CNT1A. CNT1A and LD must be stable while CLK-A is high.
16	CLK-C	Clock C Counter (TTL input). This clock signal increments the C counter by one on its negative edge. LD must be stable while CLK-C is high.
2	S-A	Select A Counter (TTL input). This signal allows the selection of the A counter according to the truth tables.

DC006 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
19	S-C	Select C Counter (TTL Input). This signal allows the selection of the A counter according to the truth tables.
4	RD-A	Read A Counter (TTl Input). This signal allows the selection of the A counter according to the truth tables.
5	RD-	Read (TTL Input). This signal allows the read operation to take place according to the truth tables.
18	LD	Load (TTL Input). When this signal goes through a high-to-low transition, the load operation is allowed to take place according to the truth tables. No data changes permitted while LD is low.
7-9 11-15	D/F (7:0)	Data Bus (Bidirectional, 3-State Outputs/TTL Inputs). These eight bidirectional lines are used to carry data in and out of the selected counter.
1	MAX-A	Maximum A Count(TTL Output). This signal is generated by ANDing CLK-A and the maximum count condition of counter A (count 376 when counting by 2 or count 377 when counting by 1).
17	MAX-C	Maximum C Count (TTL Output). This signal is generated by ANDing CLK-C and the maximum count conditions of counter C (count 377).

Summary of Electrical Specifications for DC006

Ambient Temperatures	0° to 70°
TTL Inputs	
High level input current I_{IH} (V_I = 2.7V)	55 μA max.
Low level input current I_{IL} (V_I = 0.5V)	−1.7 mA max.
TTL Outputs	
High level output voltage V_{OH} (I_O = −1 mA)	2.7V min.
Low level output voltage V_{OL} (I_O = 20 mA)	0.5V max.

DC010 Pin/Signal Descriptions

Pin	Signal	Description
1	REQ H	Request (TTL Input). A high on this signal initiates the bus request transaction. A low allows the termination of bus mastership to take place.
13	BDMGI L	DMA Grant Input (Hi-Z Input). A low on this signal allows bus mastership to be established if a bus request was pending (REQ = high); otherwise, this signal is delayed and output as BDMGO L.
16	CNT4 H	Count Four Input (TTL Input). A high on this signal allows a maximum of four transfers to take place before giving up bus mastership. A low disables this feature and an unlimited transfer will take place as long as REQ is high. If left open, this pin will assume a high state.

DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
14	TMOUT H	Time-Out (TTL Input/Open Collector Output). This I/O pin is low while MASTER ENA is high. It goes into high impedence when MASTER ENA is low. When driven low it prevents the assertion of BDMR; when driven high it allows the assertion of BDMR to take place if BDMR has been negated due to the 4-maximum transfer condition. An RC network may be used on this pin to delay the assertion of BDMR.
3	DATIN L	Data In (TTL Input). This signal allows the selection of the type of transfers to take place according to the truth table.
2	DATIO L	Data IN/Out (TTL Input). This signal allows the selection of the type of transfer to take place according to the truth table. During a DATIO transfer, this signal must be toggled in order to allow the completion of the output portion of the I/O transfer. If left open, this pin will assume a high state.
12	RSYNC H	Receive Synchronize (TTL Input). This signal allows the device to become master according to the following relationship:

DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
		RSYNC L · RPLY H· MASTER ENA = MASTER
17	CLK L	Clock (TTL Input). This clock signal used to generate all transfer timing sequences.
15	RPLY H	Reply (TTL Input). This signal is used to enable or disable the clock signal. This signal also allows the device to become master according to the following relationship:
		RSYNC L · RPLY H · MASTER ENA = MASTER
19	INIT L	Initialize (TTL Input). This signal is used to initialize the chip to the state where REQ is needed to start a bus reqest transaction. When INIT is low, the following signals are negated: BDMR L, MASTER H, DATEN L, ADREN H, SYNC H, DIN H, DOUT H.
11	BDMR L	DMA Request (Open Collector Output). A low on this signal indicates that the device is requesting bus mastership. This output may be tied directly to the bus.
9	MASTER H	Master (TTL Output). A high on this signal indicates that the device has bus mastership and a transfer sequence is in progress.

DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
8	BDMGO L	DMA Grant Output (Open Collector Output). This signal is the delayed version of BDMGI if no request is pending; otherwise, it is not asserted. This output may be tied directly to the bus.
7	TSYNC H	Transmit Synchronize (TTL Output). This signal is asserted by the device to indicate that a transfer is in progress.
18	DATEN L	Data Enable (TTL Output). This signal is asserted to indicate that data may be placed on the bus.
4	ADREN H	Address Enable (TTL Output). This signal is asserted to indicate that an address may be placed on the bus.
6	DIN H	Data In (TTL Output). This signal is asserted to indicate that the bus master device is ready to accept data.
5	DOUT H	Data Out (TTL Output). This signal is asserted to indicate that the bus master device has output valid data.

Summary of Electrical Specifications for DC010

Ambient Temperatures 0°C to 70°C

TTL Inputs

High level input current 300 μA max.
I_{IH} (V_I = 2.7V)

Low level input current I_{IL} (V_I = 0.5V)	−2.0 mA max.

TTL Outputs

High Level output voltage V_{OH} (I_O = −1 mA)	2.7V min.
Low level output voltage V_{OL} (I_O = 8 mA)	0.5V max.

Bus (HI - Z) Inputs and (Open Collector) Outputs

Bus Inputs

High level input current I_{IH} (V_I = 3.8V)	65 μA max.
Low level input current I_{IL} (V_I = 0.5V)	−10 μA max.

Bus Outputs

Low level output voltage V_{LO} (I_{sink} = 70 mA)	0.8V max.

DESCRIPTION

DMA CHIPKIT Application

Figure 1 shows how four DC005 transceivers are used to handle the first 16 BDAL lines (BDAL 0-BDAL 15) from the LSI-11 bus and to provide the interface to the internal 3-state bus. The transceivers are enabled to receive data from the LSI-11 bus when the REC H line is driven high. Similarly, the transceivers transmit data to the LSI-11 bus when the XMIT H line is driven high. Normally, the DC005s are in the receive state (REC H line asserted) and allow the transceivers to monitor the LSI-11 bus for device addresses.

Device address and vector switch inputs to the transceivers provide convenient address and vector selection.

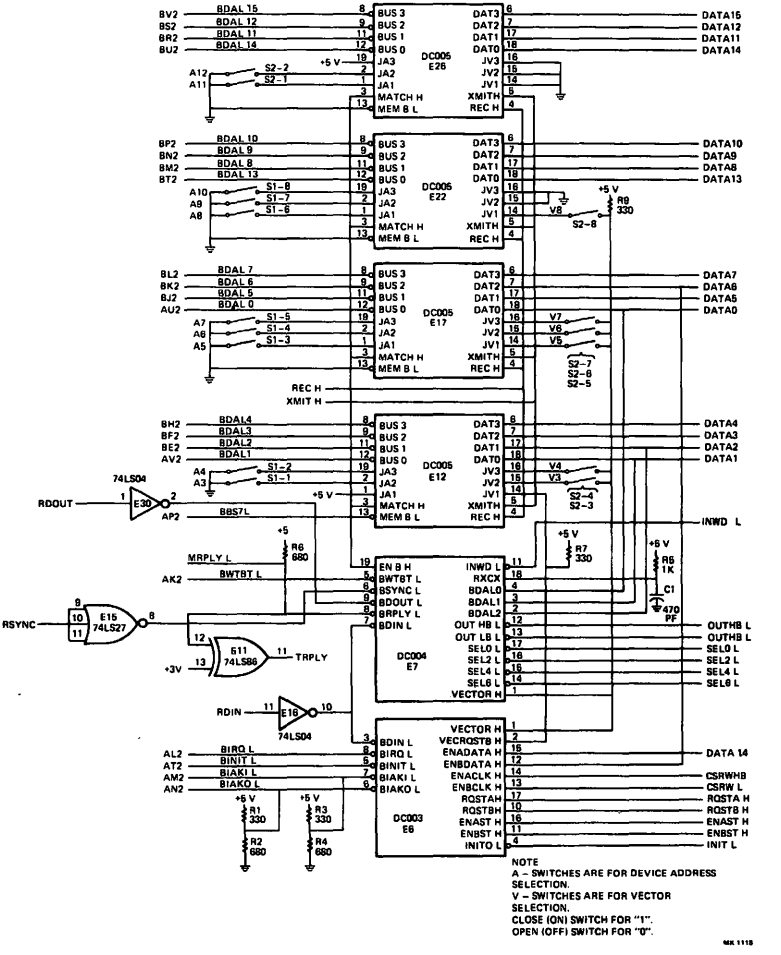


Figure 1 Typical DMA CHIPKIT Application

Switches A3 through A12 are the device address selection switches and switches V3 through V8 are for vector selection. Switches are ON

(closed) for a 1 bit and are OFF (open) for a 0 bit. The addressable registers are:

Register	Bank 7 Octal Address
Bus Address Register	1XXXX0
Word Count Register	1XXXX2
Control/Status Register	1XXXX4
Output Buffers	1XXXX6

The user selects a base address for the bus address register and sets the device address selection switches to decode this address. The remaining register addresses are then properly decoded as sequential addresses beyond the bus address register (Figures 2 and 3).

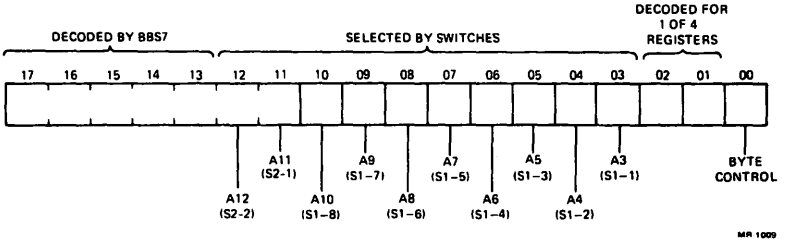


Figure 2 Device Address Select Format

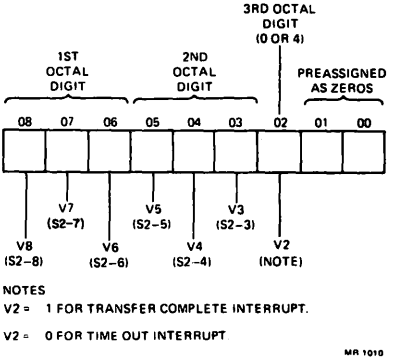


Figure 3 Interrupt Vector Select Format

The DC004 is the internal register selector. This integrated circuit monitors BDAL lines 0, 1, and 2 to determine which register address has been placed on the LSI-11 bus. The states of BDOUT and BDIN are also monitored to determine the type of transfer (DATO or DATI). When an address for an internal register is placed on the LSI-11 bus, one of the SEL outputs from the DC004 is driven low. This selects that particular register for the transfer (into or out of the master device) is determined by the state of the OUTHB L, OUTLB L, or INWD L lines. Internal register selection is summarized as follows:

Control Line	Select	Register
INWD L (Read)	SEL 0 L	Bus Address Register
INWD L (Read)	SEL 2 L	Word Count Register
OUTHB L (Write High Byte)	SEL 0 L	Bus Address Register
OUTHB L (Write High Byte)	SEL 2 L	Word Count Register
OUTLB L (Write Low Byte)	SEL 0 L	Bus Address Register
OUTLB L (Write Low Byte)	SEL 2 L	Word Count Register
INWD L (Read)	SEL 4 L	Control/Status Register
OUTHB L and MRPLY L (Write CSR High Byte)	SEL 4 L	Control/Status Register
OUTLB L and MRPLY L (Write CSR Low Byte)	SEL 4 L	Control/Status Register
OUTHB L and MRPLY L (Write High Byte)	SEL 6 L	Output Buffer
OUTLB L and MRPLY L (Write Low Byte)	SEL 6 L	Output Buffer

Note that MRPLY L is the BRPLY L output of the DC004 and is used along with OUTHB L and OUTLB L to write either the high or low byte in the control/status register or the output buffers. Write byte selection for the bus address register and the word count register is controlled only by the OUTHB L and OUTLB L lines. Words can be written to the control/status register or the output buffer registers by driving both OUTHB L and OUTLB L to the low state at the same time.

The DC004 integrated circuit was designed to operate directly from the LSI-11 bus. However, since the introduction of the DC005, the DC004 is usually interfaced to the LSI-11 bus through the DC005. Bus signals (BDAL lines) passing through the DC005 are inverted. Therefore, BDAL 0, 1, and 2 signals applied to the DC004 are inverted. Because of this inversion, it is necessary to change the nomenclature

on pins 12 through 17 on the DC004. The difference in nomenclature between DC004s operated directly from the LSI-11 bus and through a DC005 are as follows:

From Bus (Non-Inverted BDAL 0,1,2)		From DC005 (Inverted BDAL 0,1,2)	
Pin	**Signal**	**Pin**	**Signal**
12	OUTLB L	12	OUTHB L
13	OUTHB L	13	OUTLB L
14	SEL 0 L	14	SEL 6 L
15	SEL 2 L	15	SEL 4 L
16	SEL 4 L	16	SEL 2 L
17	SEL 6 L	17	SEL 0 L

It is recommended that when a DC005 is used, the DC004 be interfaced to the LSI-11 bus through the DC005 to avoid unnecessary bus loading.

The DC003 IC performs an interrupt transaction that uses the daisy-chain type arbitration scheme to assign priorities to peripheral devices. The DC003 has two channels (A and B) for generating two interrupt requests. Channel A has higher priority than channel B. If a user's device wants control of the LSI-11 bus, the interrupt enable flip-flop within the DC003 must be set. This is accomplished by asserting (logic 1) the ENX* DATA line to the DC003 (writing bit 14 or bit 6 to a one) and then clocking the enable flip-flop by asserting (logic 1) RQST. RQST must be held asserted until the interrupt is serviced. When the RQST is asserted and the interrupt enable flip-flop is set, the DC003 asserts (logic 0) BIRQ L, thus making a bus request. When the request is granted, the processor asserts (logic 0) BDIN L. This causes the DC003 to assert (logic 1) VECTOR H, which is applied to the DC005. VECTOR H at the DC005 causes the device vector to be placed on the BDAL lines to the processor. Interrupts are produced for bus time-outs (CSR bits 15 and 14) and at the completion of a block transfer (CSR bits 7 and 6).

* X may be either A or B.

DMA Application

Figure 4 shows the DMA control (DC010), the word count/bus address registers (both DC006), the output buffers (both 74LS273s), and the input drivers (74LS367s).

The DC010 performs handshaking operations required to request and gain control of the LSI-11 bus for DMA data transfers. After becoming bus master, the DC010 produces the signals necessary to perform a DIN or DOUT bus cycle as specified by the control lines. An 8-MHz free-running clock is provided by E21. This clock is used by the DC010 to generate all transfer timing sequences. The actual clock frequency is not critical and can be any frequency up to 8.3 MHz, provided it is symmetrical. An RC time constant provided by resistor R14 and capacitor C2 provides a delay for the reassertion of BDMR to the LSI-11 bus. This allows other direct memory access devices to obtain the bus during the time the CNT4 logic releases the bus and re-requests the bus.

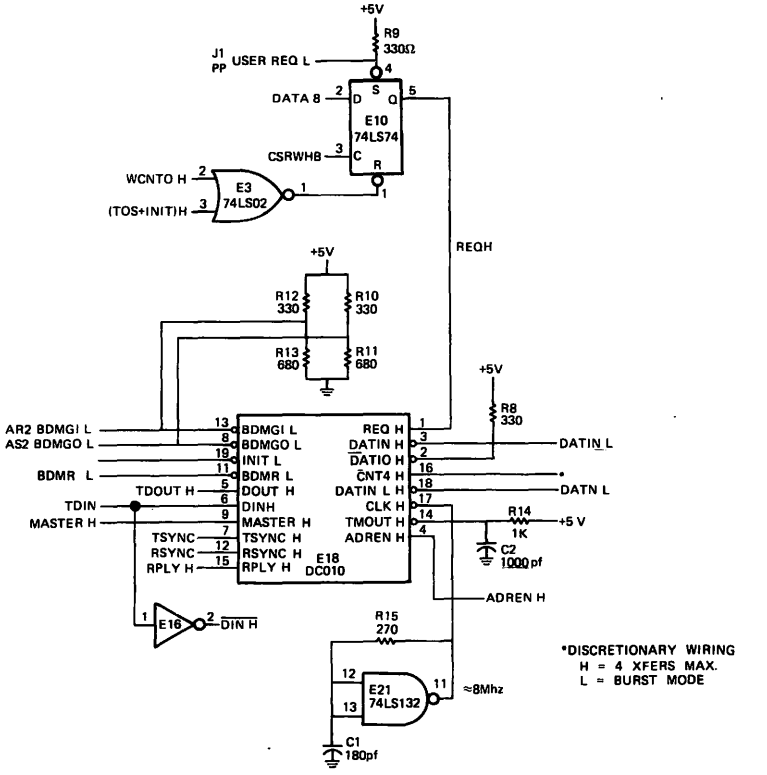


Figure 4 Typical Application (DC006, DC010, Output Delay, and Input Drives)
(Sheet 1 of 2)

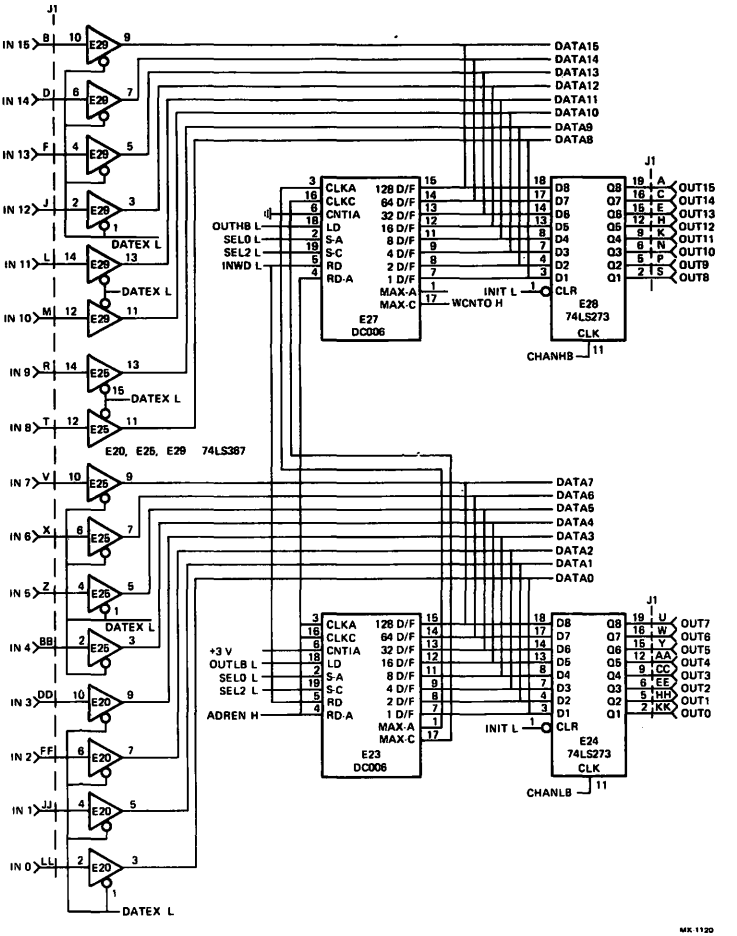


Figure 4 Typical Application (DC006, DC010, Output Delay, and Input Drives)
(Sheet 2 of 2)

User devices initiate bus requests by driving the set input of the request flip-flop (E10) low. This asserts REQ to the DC010 and generates BDMR L to the LSI-11 bus. When the DC010 becomes bus master, it asserts ADREN H to the DC006 bus address registers. ADREN H allows the bus address registers to place the address of the slave (memory) onto the internal bus and, via the DC005 transceivers, onto the LSI-11 bus. The request flip-flop (E10) remains set until the DC006 word count overfows to zero (WCNT0). WCNT0 then resets the request flip-flop.

Two DC006 word count/bus address register ICs are used to provide 16 bits each of word count and bus address. The least significant bits of the word count and bus address register and register C is the word count register. Both registers can be read or written under program control from the LSI-11 bus. Registers are selected by:

• Read bus address register	SEL 0 L INWD L
• Write high byte of bus address register	SEL 0 L OUTHB L
• Write low byte of bus address register	SEL 0 L OUTLB L
• Read word count register	SEL 2 L INWD L
• Write high byte of word count register	SEL 2 L OUTHB L
• Write low byte of word count register	SEL 2 L OUTLB L

The bus address register is incremented by two for word transfers. To accomplish the increment by two, the CNT1A input to the most significant DC006 (E23) must be high, and the CNT1A input to the most significant DC006 (E27) must be grounded. Clocking for DC006 E23 is provided by the transition of the ADREN H line from the DC010. When bus address register DC006 E23 overflows, MAX-A goes high, thus clocking the DC006 E27 bus address register.

The word count register is incremented by one each time a word is transferred. Initially, the word count register is loaded under program control, with the 2's complement of the number of words to be transferred. As words are transferred, the word count register is incremented toward zero. When DC006 E23 overflows, MAX-C goes high. MAX-C clocks the DC006 E27 word count register until DC006 E27 overflows. When E27 overflows, WCNT0 H is generated; WCNT0 H then resets the request flip-flop (E10), thus terminating data transfers.

During DMA data transactions input data from the DATI bus cycle is placed on the internal 3-state bus via the DC005 transceivers and is applied to he 74LS273 (E28 and E24) output buffers. These buffers are then clocked by CHANHB and CHANLB, thus placing the data on the 16 OUT lines to the user's device.

For output data transfers (DATO), the user's device places data on the 16 IN lines to the 74LS367 3-state drivers. The drivers are enabled by DATEX L, which is asserted during a DATO cycle. The data passes through the drivers, is applied to the internal 3-state bus and, via the DC005 transceivers, to the LSI-11 bus.

Miscellaneous Logic

Miscellaneous logic is shown in Figure 5. This logic includes CSR, output buffer and input driver control, non-existent address time-out, DC005 transceiver receive/transmit control, the control/status register (CSR), additional transceivers (8641s), and the "B" request flip-flop.

The CSR, output buffers, and input driver control receive INWD L, OUTHB L, OUTLB L, SEL 4 L, SEL 6 L, DATN H, and DIN H. These signals are gated to produce enable signals for the CSR, the output buffers, and the input drivers. CSR RD is produced by INWD L and SEL 4 L to enable the CSR data (DATA 5 through DATA 14) (Figure 5, sheet 1) to pass through the 74LS367 3-state drivers and onto the LSI-11 bus via the DC005 transceivers. OUTHB L, OUTLB L, SEL 4 L, and MRPLY L produce either CSRWHB L or CSRWLB L for writing bit 6 of the CSR (74LS74 E10 on Figure 3, sheet 1), or for clocking the "B" request flip-flop. DATEX L enables the 74LS367 3-state input drivers (Figure 5, sheet 1) during an "input" cycle. The CHANHB and CHANLB signals clock the 74LS273 output buffers during an "output" cycle. When bytes are transferred, OUTHB L, MRPLY L and SEL 6 L enable the high byte (CHANHB L asserted), while OUTLB L, MRPLY and SEL 6 L enable the low byte (CHANLB L). Both bytes are simultaneously transferred (word transfer) when DIN H is negated.

The non-existent address time-out provides a 10 μs time-out in the event that a non-existent address is requested on the LSI-11 bus during a DMA operation. This prevents hanging-up the LS-11 bus for periods longer than 10 μs. When the DC010 becomes bus master, ADREN H is asserted and cocks the 10 μs one-shot (E8). Normally RPLY L from the LSI-11 bus goes low and the one-shot is cleared. However, if RPLY L is high (no response from slave), the one-shot times out and cocks the 74LS74 flip-flop (E9). The flip-flop is set, generating (TOS + INIT) L; this signal is applied to the DC010 (Figure 4, sheet 1) clearing the internal synchronization circuit and releasing the LSI-11 bus. The signal (TOS + INIT) H resets the request flip-flop (E10). The 74LS74 flip-flop (E9) can be set and reset with CSRW HB and DATA 15 (CSR bus time-out). This flip-flop is automatically reset during power-up.

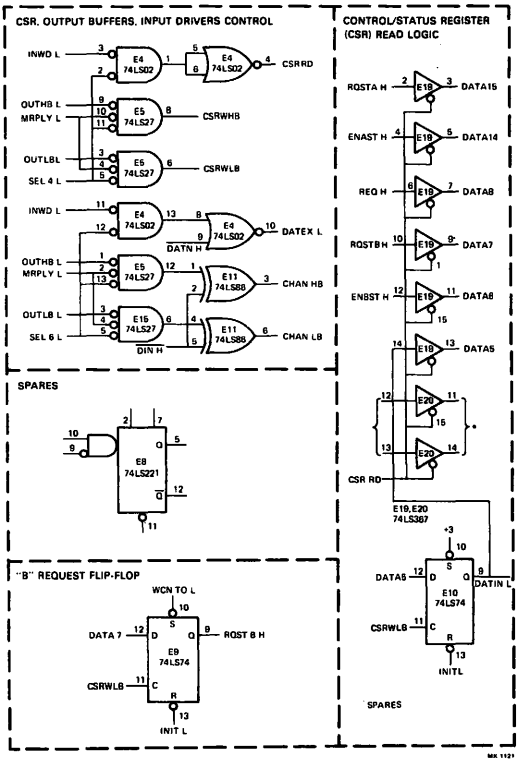


Figure 5 Typical Application (Miscellaneous Logic) (Sheet 1 of 3)

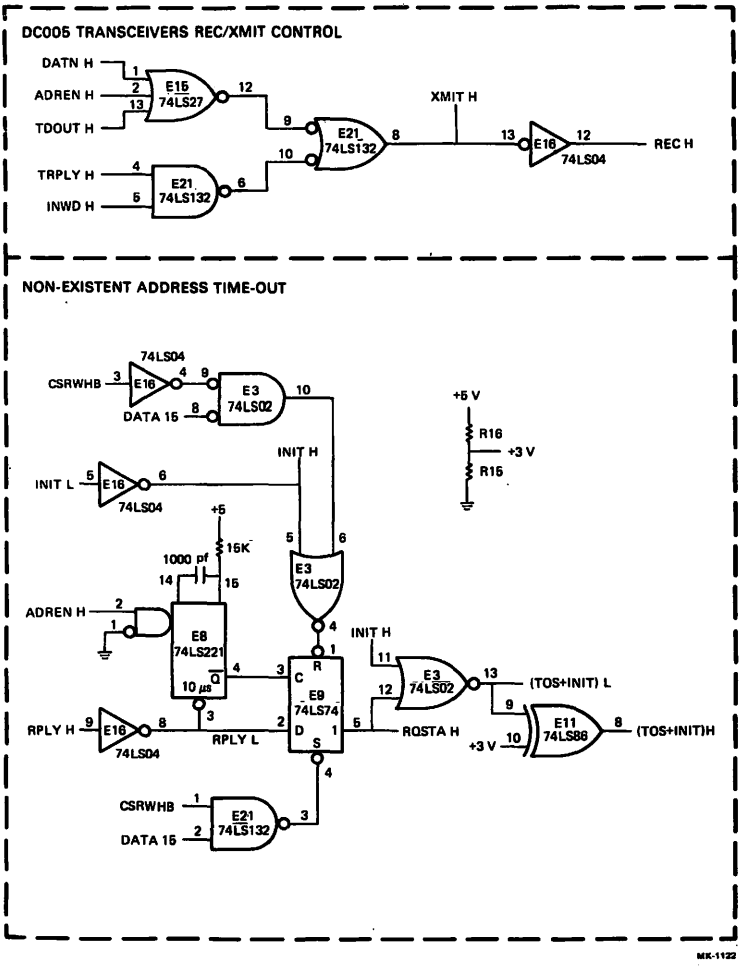


Figure 5 Typical Application (Miscellaneous Logic)
(Sheet 2 of 3)

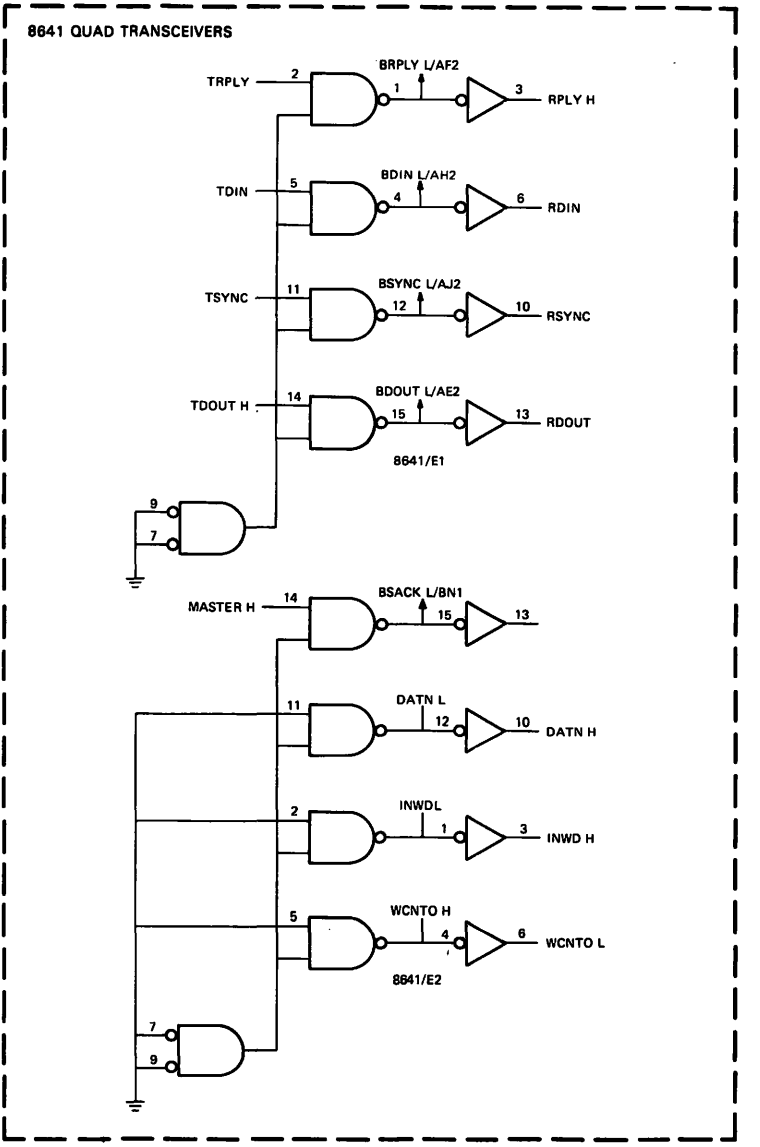


Figure 5 Typical Application (Miscellaneous Logic) (Sheet 3 of 3)

The DC005 transceiver receive/transmit control determines the state of the DC005 tranceivers. Normally, the transceivers are in the receive state to accept device addresses from the LSI-11 bus. When REC H is asserted (high), XMIT is negated (low). XMIT is asserted (high) when transferring data to the LSI-11 bus (TDOUT, DATEN, and ADREN are high; TRPLY, INWD are low). REC is asserted (high) when receiving data from the LSI-11 bus (TDOUT, DATEN, and ADREN are low; TRPLY, INWD are high).

The control/status register (CSR) (Figure 5, sheet 1) has six active bits and is a read/write register comprised of 74LS367 3-state drivers and flip-flops which are part of other logic circuits shown in Figure 3, sheet 1, and Figure 5, sheet 2. Figure 6 shows the CSR format. The CSR bits are described in Table 1.

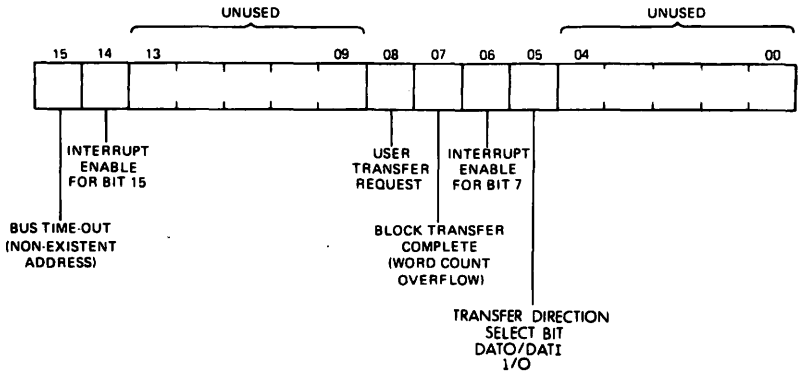


Figure 6 Control/Status Register (CSR) Format

The quad transceivers (8641) shown in Figure 3 sheet 3, supplement the DC005 transceivers for interfacing to the LSI-11 bus. In this particular application, the 8641s are permanently enabled by grounding pins 7 and 9.

CSR Bit Descriptions

Bit	Name	Description
00	Unused	
01		
02		
03		
04		
05	DATO/DATI	When set to a 1, indicates a DATO cycle; when set to a 0, indicates DATI bus cycle.
06	Interrupt enable for bit 7	This bit must be set (1) to enable the word count overflow interrupt at the end of a block transfer. When set to 0, the interrupt is inhibited.
07	Block transfer complete	This bit sets (1) when the word count register overflows, providing bit 06 is set.
08	User transfer request	The user's device must set (1) this bit to make a bus request and transfer data. User REQ L (J1-PP) must be driven low (0) to set bit 08. This bit is always read as a zero. This is an example for test purposes.
09	Unused	
10		
11		
12		
13		
14	Interrupt enable for bit 15	This bit must be set (1) to enable the bus time-out interrupt. When set to a 0, the interrupt is inhibited.
15	Bus time-out	This bit sets (1) when a slave on the LSI-11 bus does not respond with BRPLY within 10 μs after being addressed. Bit 14 must be set (1) to enable the bus time-out interrupt.

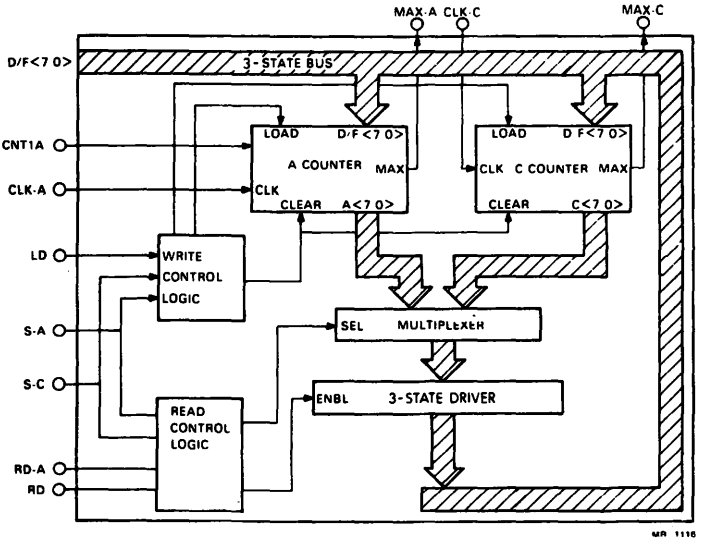


Figure 7 DC006 Simplified Block Diagram

DC006 WORD COUNT/BUS ADDRESS LOGIC (DEC #19-14035)

The word count/bus address (WC/BA) chip is a 20-pin, 0.762 cm center x 2.74 cm long (0.3 in. center x 1.08 in. long) DIP, low-power Schottky device. Its primary use is in DMA peripheral device interfaces. This IC is designed to connect to the 3-state side of theDC005 transceiver. The DC006 has two 8-bit binary up-counters, one for the word (byte) count and another for bus address. Two DC006 ICs may e cascaded to increase register implementation.

The chip is controlled by the address latch protocol chip (DC004), the DMA chip (DC010), and a minimum of ancillary logic. Both counters may be cleared simultaneously. Each counter is separately loaded by LD and the corresponding select line from the protocol chip. Each counter is incremented separately. The WC counter (word byte counter) is always incremented by one; the A counter (bus address) may be incremented by one or two for byte or word addressing, respectively.

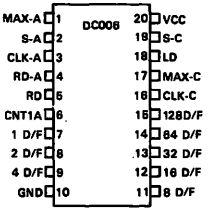
Data from the DC006 IC is placed on the 3-state bus via internal 3-state drivers. Each counter is separately read by RD and the corresponding select line.

Figure 7 is a block diagram of the DC006 IC while Figure 8 illustrates a simplified logic diagram. The DC006 pin/signal description is presented in Table 2.

TRUTH TABLES
WHERE: L = TTL LOW
H = TTL HIGH
X = DON'T CARE
Z = HIGH IMPEDANCE
↓ = HIGH TO LOW TRANSITION

READ CONTROL

INPUTS				OUTPUTS
LD – H		S-A	S-C	D/F<7:0>
RD-A	RD			
L	L	L	L	CLEAR A&C AND READ C
L	L	L	H	A<7:0>
L	L	H	L	C<7:0>
L	L	H	H	Z
L	H	X	X	Z
H	L	L	L	CLEAR A&C AND READ A
H	L	L	H	A<7:0>
H	L	H	L	A<7:0>
H	L	H	H	A<7:0>
H	H	L	L	CLEAR A&C AND READ A
H	H	L	H	A<7:0>
H	H	H	L	A<7:0>
H	H	H	H	A<7:0>



WRITE CONTROL

INPUTS			FUNCTION
RD - A = L, RD = H			
LD	S-A	S-C	
↓	L	L	*ILLEGAL
↓	L	H	LOAD A<7:0>
↓	H	L	LOAD C<7:0>
X	H	H	WC/BA NOT SELECTED
H	L	L	CLEAR BOTH COUNTERS
H	L	H	LOADING DISABLED
H	H	L	LOADING DISABLED

*ILLEGAL CONDITION BECAUSE A LOAD OPERATION AND A CLEAR OPERATION IS ATTEMPTED SIMULTANEOUSLY. RESULT OF THIS OPERATION IS TO CLEAR BOTH COUNTERS.

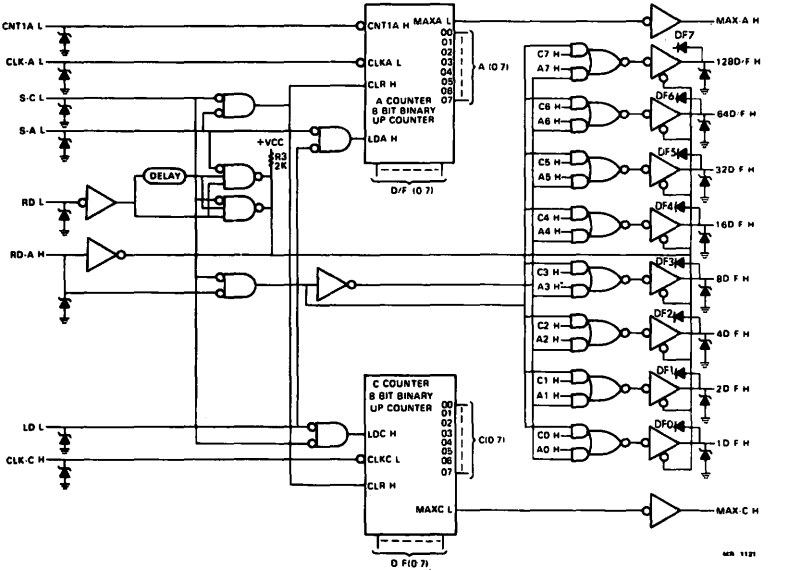


Figure 8 DC006 Simplified Logic Diagram

DC010 DIRECT MEMORY ACCESS LOGIC (DEC #19-14038)

The Direct Memory Access (DMA) chip is a 20-pin, 0.762 cm center × 2.74 cm long (0.3 in. center × 1.08 in. long) DIP, low-power Schottky device for primary use in DMA peripheral device interfaces using the LSI-11 bus.

This device provides the logic to perform the handshaking operations required to request and to gain control of the system bus. Once bus mastership has been established, the DC010 generates the required signals to perform a DATI, DATO, or DATIO transfer as specified by control lines to the chip. The DC010 IC has a control line that will allow multiple transfers or only four transfers to take place before giving up bus mastership.

Figure 9 is a simplified logic diagram of the DC010 IC. The logic symbols and truth table are presented in Figure 10. Table 3 describes the signals and pins of the DC010 by pin and signal name.

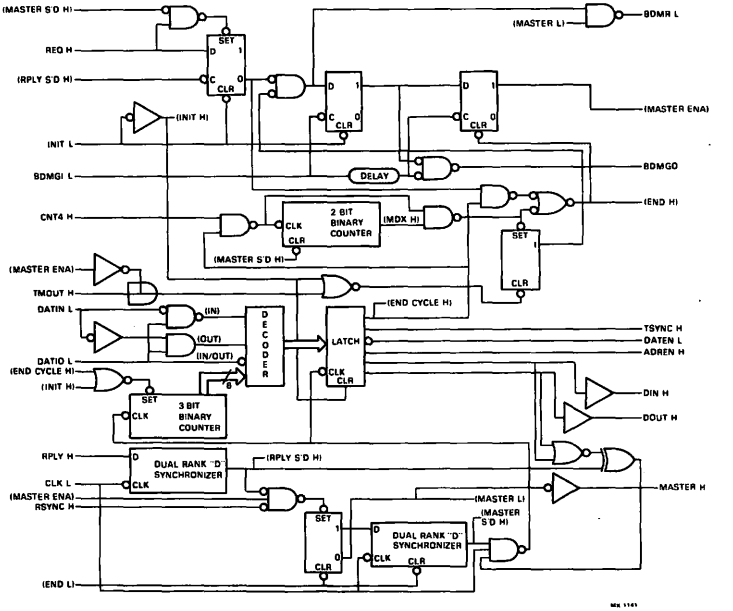
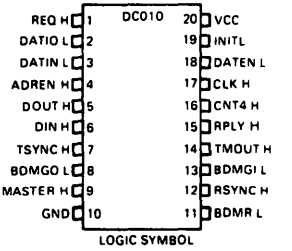


Figure 9 DC010 Simplified Logic Diagram



LOGIC SYMBOL

TRUTH TABLE

WHERE L = TTL LOW
H = TTL HIGH
X = DON'T CARE

INPUTS		TRANSFER TYPE
DATIN	DATIO	
X	L	DATIO
L	H	DATI
H	H	DATO

Figure 10 DC010 Logic Symbol/Truth Table

DDV11-B Backplane

GENERAL

The DDV11-B is an optional LSI-11 bus expansion backplane for use when additional logic space is required. The DDV11-B is a 9 × 6, 54-slot backplane with a 9 × 4 slot section (18 individual double-height or 9 quad-height module slots) prebused specifically for LSI-11 bus signal, power, and ground connections. The remaining 9 × 2 slot section is provided with +5 Vdc, GND, and −12 Vdc power connections only; this leaves the remaining pins free for use with any special double-height logic modules to be used in conjunction with the LSI-11 family of modules and bus requirements.

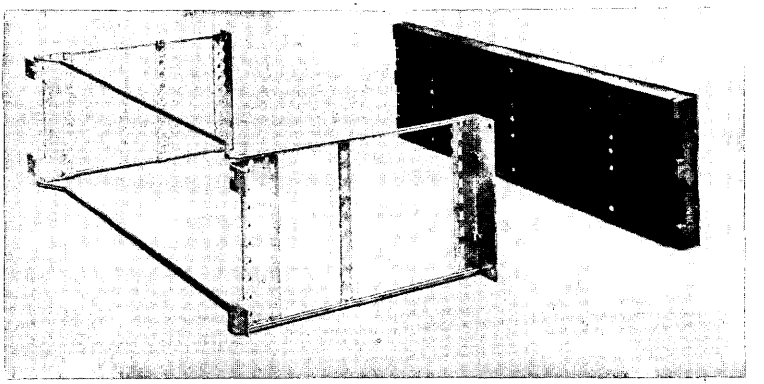
DESCRIPTION

The DDV11-B consists of an H034 system unit mounting frame, six H863, and three H8030 connector blocks, and the etched board bus structure necessary for signal routing. The etched board completely overlays the entire pin side of all connector blocks and is recessed sufficiently to allow wire-wrapping on those same pins with 30 AWG wire.

An optional card cage, type H0341, is also available to provide protection against physical damage to modules and to serve as a card guide. The card cage completely surrounds the slot side of the system unit and is shown in Figure 1. The DDV11-B can be mounted in the H909-C enclosure.

NOTE

The H909-C includes the H0341 card guide.



7920 - 26W - AO168

Figure 1 DDV11-B with H0341 Card Assembly

DDV11-B

CONFIGURATION

Module Slot Assignments

Figure 2 shows the slot location assignments of the DDV11-B. Rows A, B, C, and D are dedicated to the LSI-11 bus. Any module which conforms to the LSI-11 bus specifications may be used in this portion of the DDV11-B. The position numbers indicate the bus grant wiring scheme with respect to the processor module. The bus grant signals propagate through the slot locations in the position order shown in Figure 2 until they reach the requesting device. Any unused slots must be jumpered to provide bus grant signal continuity or it is recommended that unused locations occur only in the highest position numbered locations.

Rows E and F contain the 18 user-defined slots with power and ground connections provided.

Equipment Supplied

The DDV11-B option consists of the following items:

Six H863 connector blocks
Three H8030 connector blocks
Etched board bus structure

Installation

The DDV11-B can be mounted on panels or chassis using standard hardware. The overall dimensions of the unit are shown in Figure 3. The H034 mounting frame of the DDV11-B is provided with tapped holes and clearance holes to enable the attachment of the system unit.

H0341 Card Assembly Mounting

The card assembly provides nylon guides which help to guide and support the modules installed in the system unit. The H0341 card assembly is supplied with the hardware necessary to mount to the H034 mounting frame. Figure 4 shows the method of assembly. Two screws (item 2) and two washers (item 1) are inserted through the clearance holes of the PC board and H034 mounting frame and into the two threaded inserts on each bracket of the card assembly.

DDV11-B

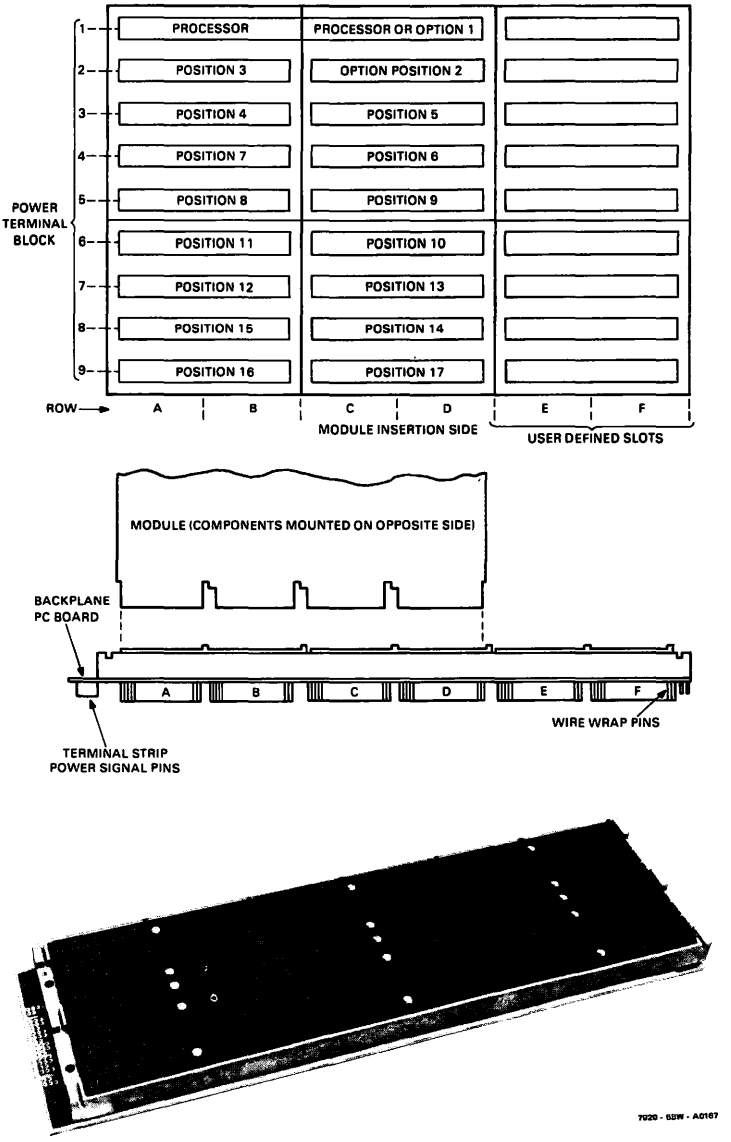


Figure 2 DDV11-B Module Installation and Slot Assignments

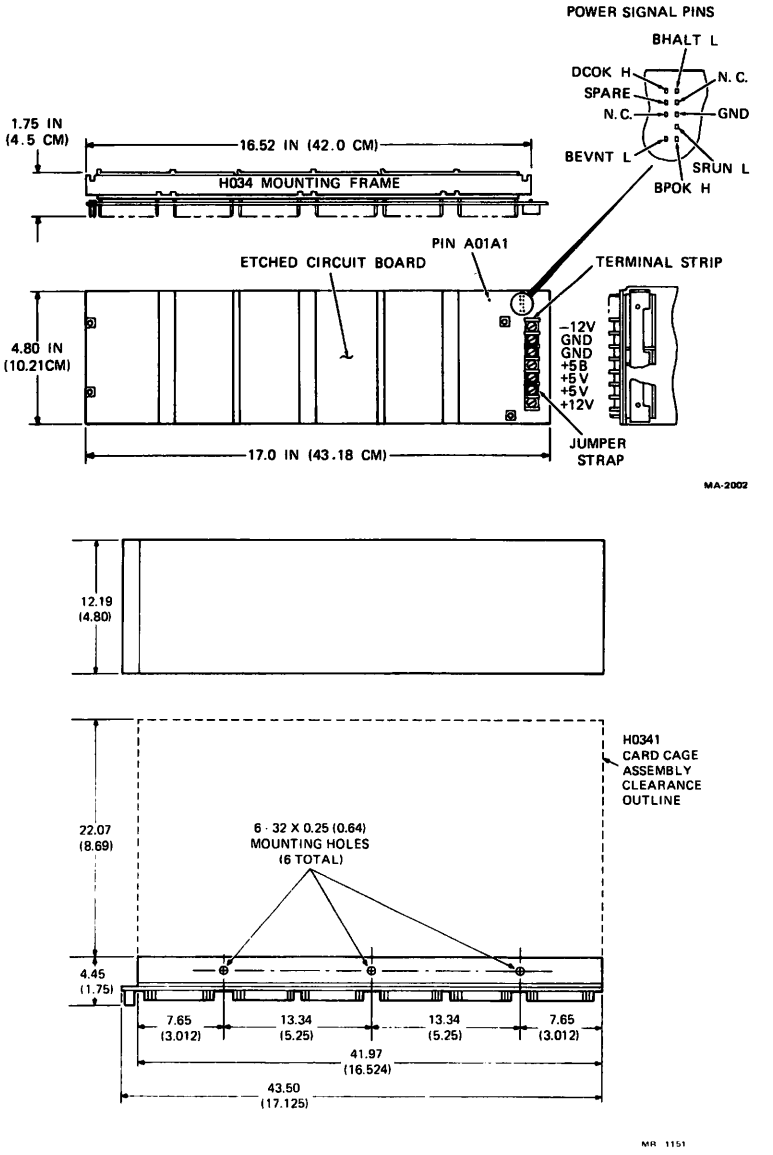


Figure 3 DDV11-B Power Wiring and Dimensions

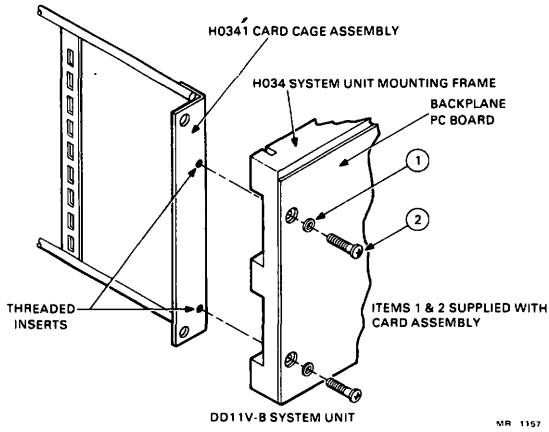


Figure 4 H0341 Card Assembly Installation

DC Power and Power Signal Connections

DC power is supplied to the modules in the DDV11-B through the backplane PC board. The power and ground leads from the external source connect to the 7-position terminal board mounted on the edge of the PC board as shown in Figure 3. Any suitable connector terminals, solder or crimp style, may be attached to the power supply leads and inserted under the terminal strip screws. A jumper tab is mounted between the two +5 V screws and between the two ground (GND) screws on the terminal board. The total current capability of the DDV11-B and the wire size required are as follows:

Terminal		Current (Max)	Wire Size (AWG)
+12 V		20 A	14
+5 V	Jumped	40 A	14
+5 V			
+5 B		20 A	
GND	Jumped	40 A	14
GND			
−12 V		20 A	

Figure 5 identifies the power signal pins which are located at the opposite end of the backplane PC board from the power terminal strip. A mating female connector (DIGITAL P/N 12-11206-02 or 3M P/N 3473-3) can be inserted over the pins and used to connect the external signals to the backplane.

Backplane Pin Assignments

Table 1 lists the backplane pin assignments for the LSI-11 bus signals and dc power and ground connections on the DDV11-B backplane.

Table 1 DDV11-B Backplane Pin Assignments

Side Row	2 A&C	1 A&C	2 B&D	1 B&D	2 E	1 E	2 F	1 F
A	+5V	BSPARE1	+5V	BDCOK H	+5V	BLANK	+5V	BLANK
B	−12V	BSPARE2	−12V	BPOK H	−12V	BLANK	−12V	BLANK
C	GND	BDAL 17 L	GND	SSPARE 4	GND	BLANK	GND	BLANK
D	+12V	BDAL 16 L	+12V	SSPARE 5	BLANK	BLANK	BLANK	BLANK
E	BDOUT L	SSPARE1	BDAL2 L	SSPARE 6	BLANK	BLANK	BLANK	BLANK
F	BRLPY L	SSPARE2	BDAL3 L	SSPARE 7	BLANK	BLANK	BLANK	BLANK
H	BDIN L	SSPARE3	BDAL4 L	SSPARE 8	BLANK	BLANK	BLANK	BLANK
J	BSYNC L	GND	BDAL5 L	GND	BLANK	BLANK	BLANK	BLANK
K	BWTBT L	MSPAREA	BDAL6 L	MSPARE B	BLANK	BLANK	BLANK	BLANK
L	BIRQ L	MSPAREA	BDAL7 L	MSPARE B	BLANK	BLANK	BLANK	BLANK
M	BIAK I L	GND	BDAL8 L	GND	BLANK	BLANK	BLANK	BLANK
N	BIAK O L	BDMR L	BDAL9 L	BSACK L	BLANK	BLANK	BLANK	BLANK
P	BBS 7 L	BHALT L	BDAL10 L	BSPARE 6	BLANK	BLANK	BLANK	BLANK
R	BDMG 1 L	BREF L	BDAL11 L	BEVNT L	BLANK	BLANK	BLANK	BLANK
S	BDMG 0 L	PSPARE3	BDAL12 L	PSPARE 4	BLANK	BLANK	BLANK	BLANK
T	BINIT L	GND	BDAL13 L	GND	BLANK	GND	BLANK	GND
U	BDAL 0 L	+12B	BDAL14 L	PSPARE 2	BLANK	BLANK	BLANK	BLANK
V	BDAL 1 L	+5B	BDAL15 L	+5	BLANK	BLANK	BLANK	BLANK

DLV11 SERIAL LINE UNIT

SPECIFICATIONS

Identification	M7940
Size	Double
Power	+5.0 Vdc ± 5% at 1.0 A (1.6 A max) +12.0 Vdc ± 3% at 0.18 A (0.25 A max)
Bus loads	
AC	2.5
DC	1.0

CONFIGURATION

General

The user can select the register address, parity, number of data bits, number of stop bits, baud rate, and type of serial interface. The descriptions of the registers and their standard factory addresses are listed in Table 1. Available jumpers are shown in Figure 1 and their applications are listed in Table 2.

Table 1 Standard Addresses

Register	Mnemonic	Console	Second Module
Receiver control status	RCSR	177560	176500
Receiver data buffer	RBUF	177562	176502
Transmit control/status	XCSR	177564	176504
Transmit data buffer	XBUF	177566	176506
Standard vectors	RCSR	060	300
	XCSR	064	304

DLV11

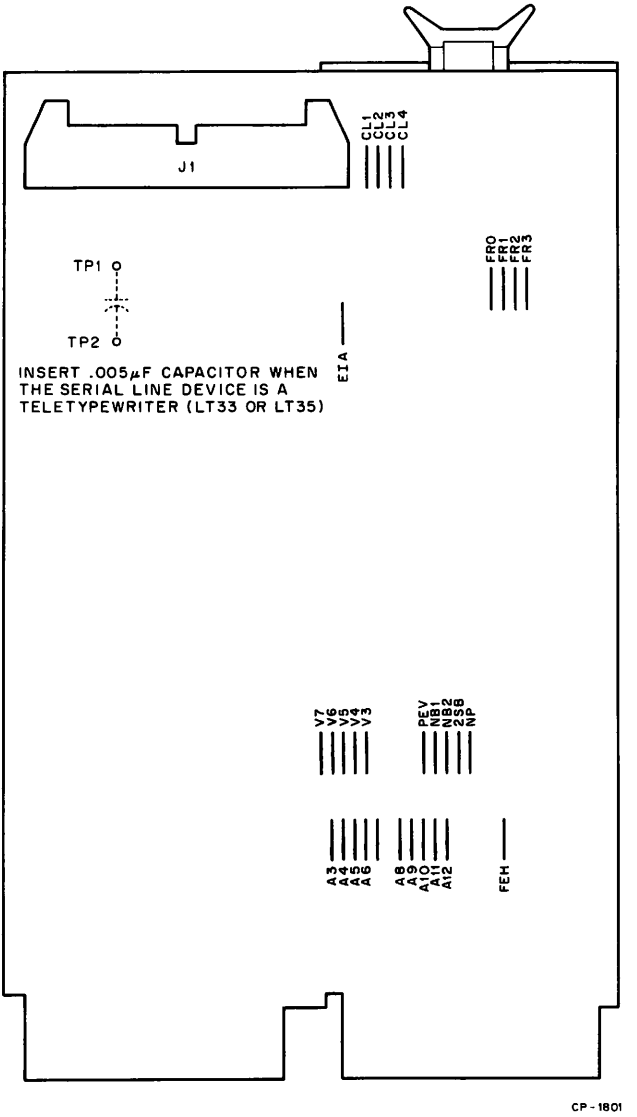


Figure 1 DLV11 Jumper Locations

Table 2 DLV11 SLU Factory Jumper Configuration

Jumper Designation	Jumper State*	Function Implemented
A3	I	This arrangement of jumpers A3 through A12 implements the octal device address 17756X, which is the assigned address for the console device SLU. The least significant digit is hardwired on the module to address the four SLU device registers as follows: X = 0, RCSR address X = 2, Receive data register address X = 4, XCSR address X = 6, Transmit data register address
A4	R	
A5	R	
A6	R	
A7	I	
A8	R	
A9	R	
A10	R	
A11	R	
A12	R	
V3	I	This jumper arrangement implements the interrupt vector: 60 for received data and 64 for transmitted data.
V4	R	
V5	R	
V6	I	
V7	I	
NP	R	No parity
2SB	R	Two stop bits
NB2	R	Eight data bits
NB1	R	
PEV	R	Even parity if NP installed
FEH	I	Halt on framing error
EIA	I	12 V EIA operation enabled
FR0	R	
FR1	R	110 baud rate selected
FR2	R	
FR3	R	
CL1	I	20 mA current loop active receiver and transmitter selected
CL2	I	
CL3	I	Jumpered with 180 ohm resistors
CL4	I	

* R = removed, I = installed

Addresses

Addresses for the DLV11 can range from 160000_8 through $17777X_8$. The least significant three bits (only bits 1 and 2 are used; bit 0 is ignored) address the desired register in the DLV11, as described in Table 1.

Address bits 3 through 12 are jumper-selected as shown in Figure 2.

Since each DLV11 module has four registers, each requires four addresses. Addresses 177560-177566 are reserved for the DLV11 used with the console peripheral device. Additional DLV11 modules should be assigned addresses from 176500 through 176670, allowing up to 30 additional DLV11 modules to be addressed.

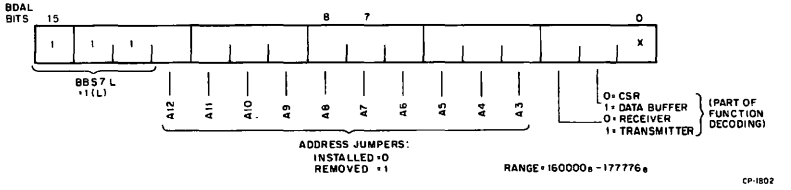


Figure 2 CSR Address Selection

Word Format

The word format for the Receiver Control/Status Register (RCSR) is detailed in Figure 3 and is described in Table 3.

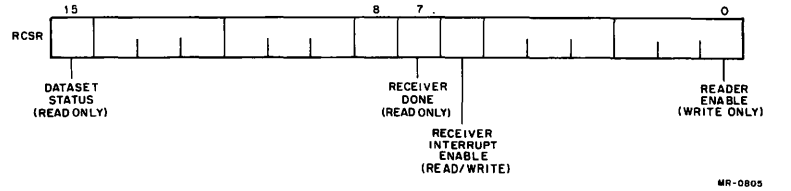


Figure 3 Receiver Control/Status Register (RCSR)

Table 3 RCSR Word Format

Bit	Function
15	Dataset Status — Set when CARRIER or CLEAR TO SEND and DATA SET READY signals are asserted by an EIA device. Read-only bit.
14-8	Not used. Read as 0.
7	Receiver Done — Set when an entire character has been received and is ready for input to the processor. This bit is automatically cleared when RBUF is addressed or when the BDCOK H signal goes false (low). A receiver interrupt is enabled by the DLV11 when this bit is set and receiver interrupt is enabled (bit 6 is also set). Read-only bit.
6	Interrupt Enable — Set under program control to generate a receiver interrupt request when a character is ready for input to the processor (bit 7 is set). Cleared under program control or by the BINIT signal. Read/write bit.
5-1	Not used. Read as 0.
0	Reader Enable — Set by program control to advance the paper tape reader on a teletypewriter device to input a new character. Automatically cleared by the new character's start bit. Write-only bit.

The receiver data buffer register (RBUF) word format is shown in Figure 4 and described in Table 4.

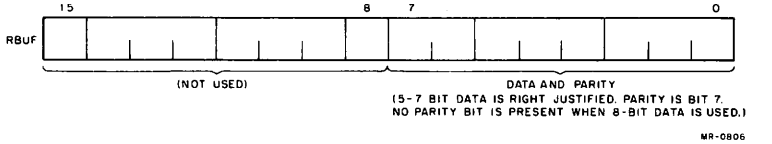


Figure 4 Receiver Data Buffer Register (RBUF)

Table 4 RBUF Word Format

Bit	Function
15-8	Not used. Read as 0.
7-0	Contains five to eight data bits in a right-justified format. MSB is the optional parity bit. Read-only bits.

The transmit control/status register (XCSR) word format is shown in Figure 5 and described in Table 5.

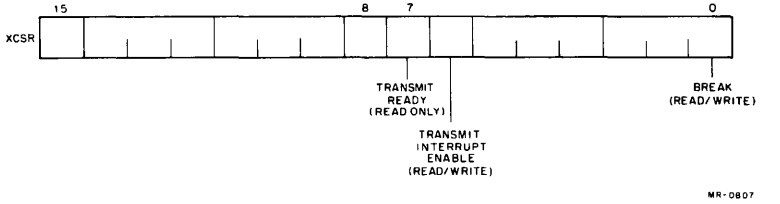


Figure 5 Transmitter Control/Status Register (XCSR)

Table 5 XCSR Word Format

Bit	Function
15-8	Not used. Read as 0.
7	Transmit Ready — Set when XBUF is empty and can accept another character for transmission. It is also set during the power-up sequence by the BDCOK H signal. Automatically cleared when XBUF is loaded. When transmitter interrupt is enabled (bit 6 also set), an interrupt request is asserted by the DLV11 when this bit is set. Read-only bit.
6	Interrupt Enable — Set under program control to generate a transmitter interrupt request when the DLV11 is ready to accept a character for

Table 5 XCSR Word Format (Cont)

Bit	Function
	transmission. Reset under program control or by the BINIT signal. Read/write bit.
5-1	Not used. Read as 0.
0	Break — Set or reset under program control. When set, a continuous space level is transmitted. BINIT resets this bit. Read/write bit.

The transmit data buffer register (XBUF) word format is shown in Figure 6 and described in Table 6.

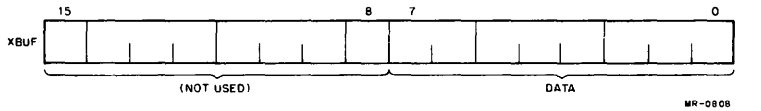


Figure 6 Transmitter Data Buffer Register (XBUF)

Table 6 XBUF Word Format

Bit	Function
15-8	Not used.
7-0	Contains five to eight right-justified data bits. Loaded under program control for serial transmission to a device. Write-only bits.

Interrupt Vectors

Vectors can range from 0 through $37X_8$. Vectors 60 and 64 are reserved for the console peripheral device. Additional DLV11 modules should be assigned vectors following any DRV11 modules installed in

the system starting at 300. Vector bits 3 through 7 are selectable by the user to form the address as described in Figure 7. The factory configuration will set the receiver interrupt vector for 060 and the transmitter interrupt vector will be set at 064.

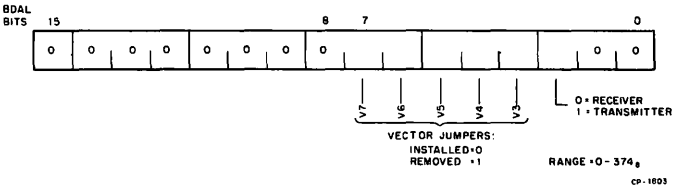


Figure 7 Interrupt Vector

UART Operation

The UART operation is programmed by using jumpers NP, 2SB, NB1, NB2, and PEV as shown below.

Number of Data Bits

	NB1	NB2
5	Installed	Installed
6	Removed	Installed
7	Installed	Removed
8	Removed	Removed

Number of Stop Bits Transmitted

2SB installed = One stop bit
2SB removed = Two stop bits

Parity Transmitted

NP removed = No parity bit
NP and PEV installed = Odd parity
NP installed and PEV removed = Even parity

Baud Rate Selection

Baud rate is programmed via jumpers FR0 through FR3 as shown in Table 7.

Table 7 Baud Rate Selection

Baud Rate	FR3	FR2	FR1	FR0
50	I	I	R	I
75	I	I	R	R
110	R	R	R	R
134.5	I	R	I	I
150	R	R	R	I
200	I	R	I	R
300	R	R	I	R
600	I	R	R	I
1200	R	I	R	R
1800	R	I	R	I
2400	I	R	R	R
2400	R	R	I	I
4800	R	I	I	R
9600	R	I	I	I
External (via pin BH1)	I	I	I	X

NOTE:
I = Installed X = Irrelevant R = Removed

EIA Interface

EIA drivers are enabled when jumper EIA is installed. This jumper applies −12V to the EIA driver chip. It should be removed during 20 mA current loop operation.

20 mA Current Loop Interface

Jumpers CL1 through CL4 are associated with 20 mA current loop interface operation. Remove or install CL1 and CL4 jumpers and CL2 and CL3 180 ohm resistors for the desired function as described below.

The active current loop jumper configuration is shown in Figures 8 and 9.

Transmit: CL4 jumper installed
CL3 resistor installed

Receive: CL1 jumper installed
CL2 resistor installed

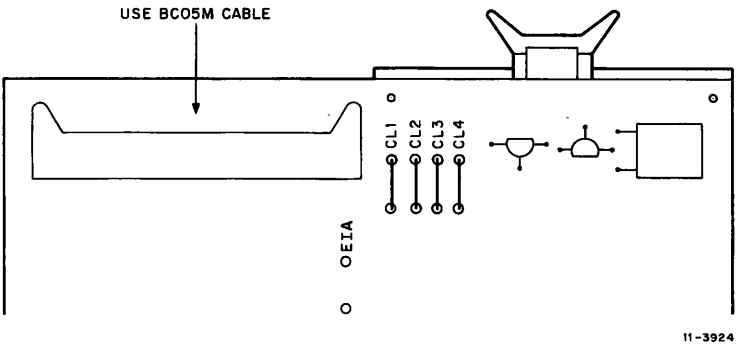


Figure 8 20 mA Active Current Loop Jumper Configuration

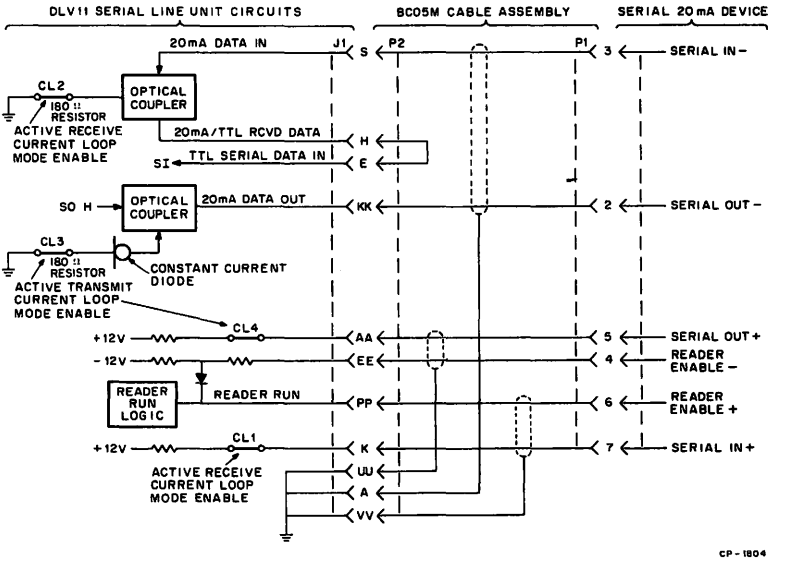


Figure 9 Active 20 mA Current Loop Interface

The passive current loop jumper configuration is shown in Figures 10 and 11.

Transmit: CL4 jumper removed
CL3 resistor removed

Receive: CL1 jumper removed
CL2 resistor removed

The DLV11 is supplied with jumpers CL1 through CL4 wired for the active transmit, active receive mode (Figure 9). When in this mode, serial current limiting to 23 mA is provided by resistors (one each for transmit and receive functions) connected to the +12V source. Note that when module power is removed, the 20 mA transmit optical coupler closes the serial loop (active or passive mode). When the DLV11 is used in the passive 20 mA mode (Figure 11), the serial device must produce the 20 mA current. Current limiting must be provided for transmit and receive currents in the serial device.

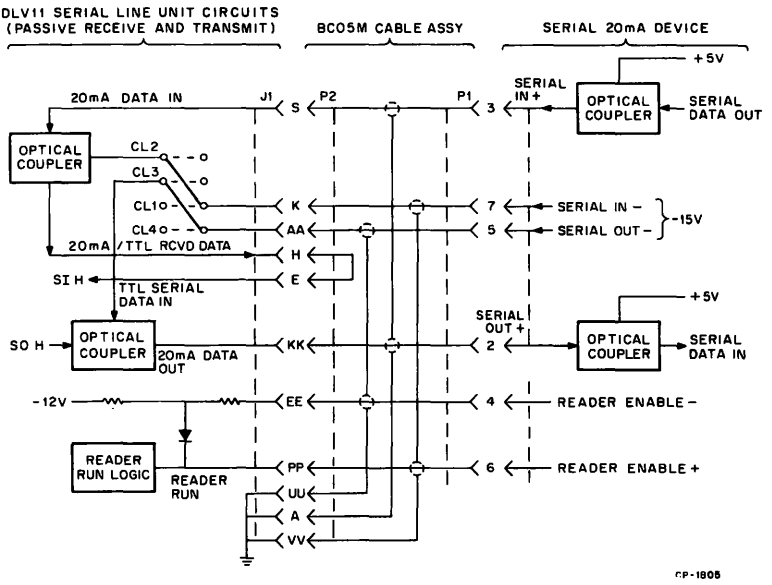


Figure 10 Passive 20 mA Current Loop Interface

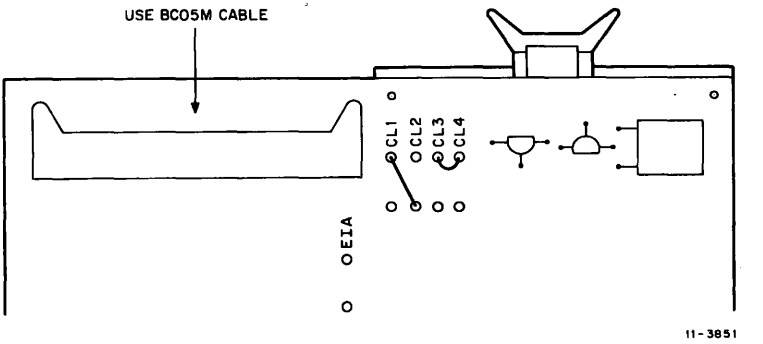


Figure 11 20 mA Passive Current Loop Jumper Configuration

Framing Error Halt

A framing error halt allows entry to console microcode directly from the console device by pressing the BREAK key, producing a framing error. A framing error occurs when the received character has no valid stop bit. This error condition is detected by the UART. FEH is factory-

installed, causing the assertion of BHALT L when the framing error is detected. The processor then executes console microcode.

Installation

Prior to installing the DLV11 on the backplane, first establish the desired priority level to determine the backplane slot in which the module will be installed. Then, check that jumpers are removed or installed as described for your application. Connection to the peripheral device is via an optional data interface cable. Cables are listed below.

Application	Cable Type*
EIA Interface	BC01V-X or BC05C-X Modem Cable
20 mA Current Loop	BC05M-X Cable Assembly

* The -X in the cable number denotes length in feet, as follows: -1, -6, -10, -20, -25. For example, a 10-ft EIA interface cable would be ordered as BC05C-10.

Interfacing with 20 mA Current Loop Devices

When interfacing with 20 mA current loop devices, the BC05M cable assembly provides the correct connections to the 40-pin connector on the DLV11. The peripheral device end of the cable is terminated with a Mate-'N'-Lok connector.

The complete interface circuit provided by the BC05M cable and the associated DLV11 jumpers is shown in Figure 10.

NOTE

When the DLV11 is used with teletypewriter devices, a 0.005 μF capacitor must be installed between split lugs TP1 and TP2.

After configuring the module jumpers and installing the proper interface cable, the DLV11 can be installed in the backplane.

Interfacing with EIA-Compatible Devices

When interfacing with EIA devices, the BC01V or BC05C modem cable provides the correct connection to the 40-pin connector on the DLV11. The peripheral device end of the cable is terminated with a Cinch DB25P connector that is pin-compatible with Bell 103 or 113 modems. Connector pinning and signal levels conform to EIA specification RS-232C. The complete EIA interface circuit is shown in Figure 12; jumpers are shown in Figure 13.

OPTIONAL HARDWARE

Cables

BC05M	20 mA; H856 to Mate-'N'-Lok female
BC05C	EIA; H856 to Cinch 25-pin male.

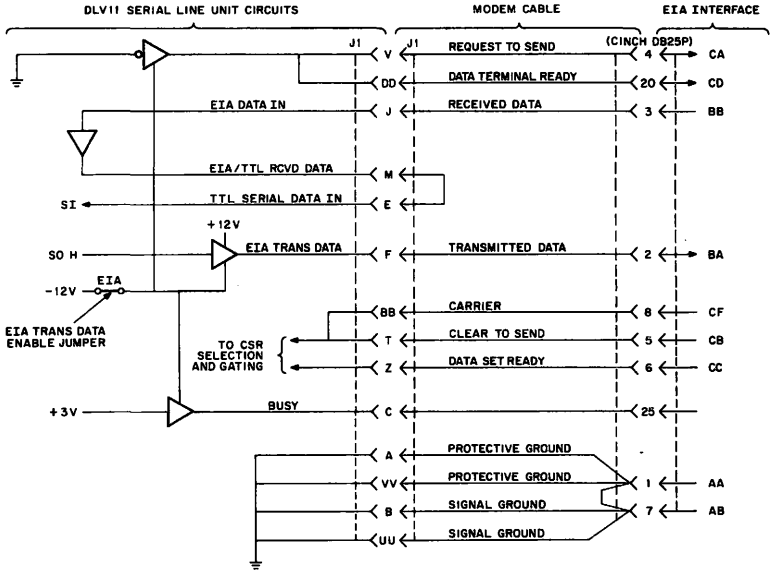


Figure 12 EIA Interface

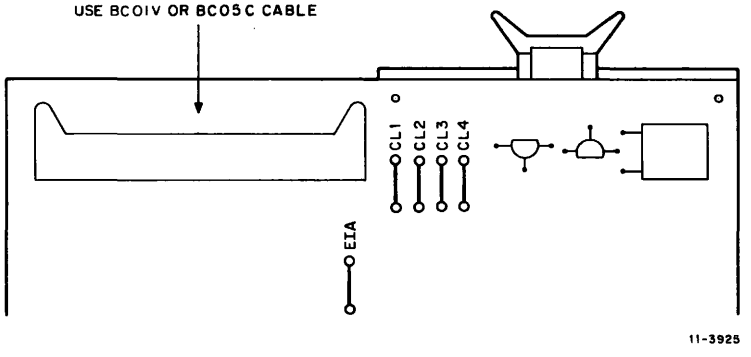


Figure 13 EIA Jumper Configuration

DLV11

Connectors

H856	To module
Cinch DB25S	To BC05C
Mate-'N'-Lok (male)	12-09340-01 connector
Mate-'N'-Lok (male)	12-09378-01 contacts
Mate-'N'-Lok (female)	12-09340-00 connector
Mate-'N'-Lok (female)	12-09379-01 contacts

Miscellaneous

BC05F	20 mA extension cable (Mate-'N'-Lok to Mate-'N'-Lok)
BC03P	Null modem Cable (female Cinch to female Cinch)
H312A	Null modem

DLV11-E

DLV11-E ASYNCHRONOUS LINE INTERFACE

GENERAL

The DLV11-E is an asynchronous line interface module that interfaces the LSI-11 bus to any of several types of serial communications lines. The module receives serial data from peripheral devices, assembles it into parallel data, and transfers it to the LSI-11 bus. It accepts data from the LSI-11 bus, converts it into serial data, and transmits it to the peripheral devices. The DLV11-E offers full modem control and EIA-type interface.

FEATURES

- Jumper- or program-selectable, crystal-controlled baud rates: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, and 19,200. Split transmit and receive baud rates are possible.
- Provisions for user-supplied external clock inputs for baud rate control.
- Jumper-selectable data bit formats.
- LSI-11 bus interface and control logic for interrupt processing and vectored addressing of interrupt service routines.
- Full modem control (Bell 103, 113, 202C, 202D, and 212-compatible).

SPECIFICATIONS

Identification	M8017
Size	Double
Power	+5.0 Vdc ±5% at 1.0A +12.0 Vdc ±3% at 0.18 A
Bus loads	
AC	1.6
DC	1.0

DLV11-E

DESCRIPTION

General

Major functions contained on the DLV11-E are shown in Figure 1. Communications between the processor and the DLV11-E are executed via programmed I/O operations or interrupt-driven routines.

Bus Interface

The bus interface circuit signal lines consist of data moving between the LSI-11 bus and the module's internal tri-state bus. It decodes the device address and produces an address match (MATCH H) signal and it places interrupt vectors on the LSI-11 bus. The bus interface receives from the LSI-11 bus unless it is switched to transmit to the LSI-11 bus. The interrupt logic can cause the bus interface to transmit either a transmitter or receiver interrupt vector and the I/O control logic can cause the bus interface to transmit to or receive data from the LSI-11 bus.

The bus interface receives LSI-11 bus lines BDAL00 L through BDAL15 L and places them on the module's tri-state bus. If BBS7 L is asserted, the circuit decodes BDAL03 L through BDAL12 L and asserts MATCH H. Jumpers A3-A12 are configured to allow the option to respond to specific device register addresses. Jumpers V3-V8 select the options' interrupt vector.

I/O Control Logic

When the I/O control logic receives MATCH H from the bus interface, it decodes tri-state bus lines DAT00 H through DAT02 H and selects the addressed device register. The I/O control logic exchanges bus control signals with the processor to perform input and output data transfers.

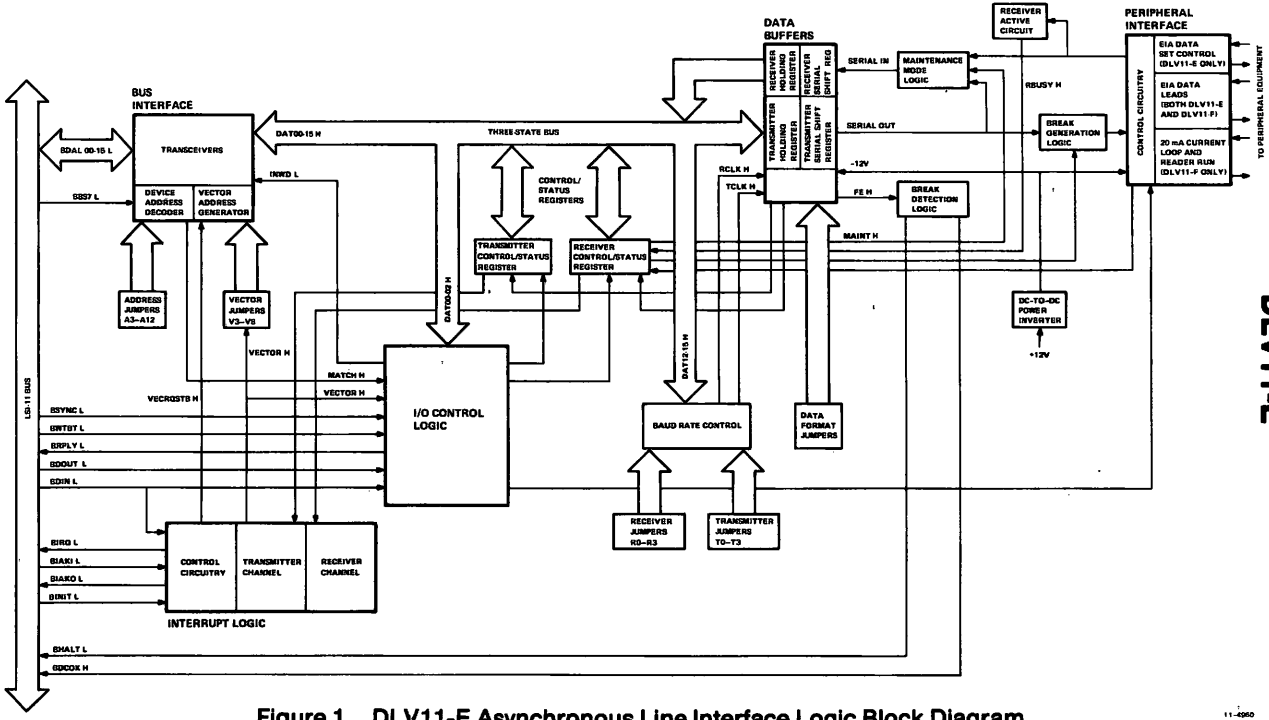


Figure 1 DLV11-E Asynchronous Line Interface Logic Block Diagram

11-4960

During an interrupt transaction, VECTOR H from the interrupt logic causes the circuit to assert BRPLY L in response to BDIN L. During data transactions, the I/O control logic asserts INWD L to switch the bus interface transceivers from receiving to transmitting.

Control/Status Registers

The receiver control/status register (RCSR) and the transmitter control/status register (XCSR) are enabled by selection signals from the I/O control logic. The CSRs are byte addressable for reading status bits or writing control bits.

Data Buffers

The receiver buffer (RBUF) and transmitter buffer (XBUF) provide double-buffering, in that one byte of data can be held while another byte is entering or exiting. This allows asynchronous, full-duplex operation. Data is handled in the low byte of the registers. The buffer control circuitry places receiver buffer error flag bits in the high byte of the RBUF. It also sends a status bit to the RCSR and a framing error bit (FE H) to the break logic.

Receiver Active Circuit

This circuit monitors the received serial data line and sets a status bit (RCVR ACT) as soon as the RBUF begins receiving data. It clears the bit when a character of data has been received.

Interrupt Logic

The DLV11-E can generate transmitter interrupts. If the XBUF is ready to serialize another character of data and the transmitter interrupt enable bit is set in the XCSR, the interrupt logic requests to interrupt the processor (by asserting BIRQ L.) If the processor acknowledges via the BIAKI/BIAKO daisy-chain, the interrupt logic asserts VECTOR H and VECRQSTB H. These signals cause the bus interface to place the transmitter function interrupt vector address on the LSI-11 bus.

The module also can request a receiver interrupt if the RBUF has received a character and the receiver interrupt bit is set in the RESR. When the interrupt request is acknowledged, the interrupt logic asserts VECTOR H. VECTOR H causes the bus interface circuit to place the receiver function interrupt vector on the LSI-11 bus. (VECRQSTB H is used only for a transmitter interrupt.)

The DLV11-E also generates a receiver interrupt as a result of data set status. If the data set interrupt enable bit is set in the RCSR, a receiver interrupt will result from a change of state on any of the modem control lines (ring, clear to send, carrier, or secondary received data).

The interrupt acknowledge daisy-chain (BIAKI/BIAKO) passes through both the receiver and transmitter sections of the interrupt logic. It goes through the receiver section first, thereby giving the receiver channel priority over the transmitter channel.

Baud Rate Control

The baud rate control establishes the speed at which the data buffers handle serial data. It produces clock signals by dividing a crystal oscillator frequency by an amount selected by jumpers or the program. The circuit can be jumpered to generate either independent transmitter and receiver clocks (split speed operation) or a common clock (common speed operation).

When the programmable baud rate enable bit is set in the XCSR, the baud rate control decodes tri-state bus lines DAT12 H through DAT15 H. These bits control the receive baud rate in split speed operation and both transmit and receive baud rate in common speed operation. When programmable baud rate is not enabled, the baud rates are controlled by jumpers. In split speed operation, jumpers R0-R3 control the receive baud rate and jumpers T0-T3 control the transmit baud rate. In common speed operation, R0-R3 control both baud rates.

The circuit also has provisions for a user-supplied external clock.

Break Logic

A break signal is a continuous spacing condition on the serial data line. If the break bit is set in the XCSR, the module will transmit a break signal to the peripheral device (normally another processor). If the module receives a break signal from the peripheral device (normally a console device), the RBUF control circuitry interprets the absence of stop bits as a framing error. The circuit can be jumpered to ignore the framing error, to place the processor in the halt mode, or to cause the processor to reboot. The break logic asserts BHALT L to halt the processor. It negates BDCOK H to reboot.

Maintenance Mode Logic

The modules can check out their data paths up to (but not including) the peripheral interface circuit by looping the XBUF's serial output back to the RBUF'S serial input. Data from the LSI-11 bus still goes to the peripheral device, but no data is received from the peripheral in this maintenance mode. The program can compare received (looped) data with transmitted data to check for errors. The maintenance mode is entered by setting the maintenance bit in the XCSR.

Signal Peripheral Interface

This circuit converts the module's TTL levels to EIA standard levels for modem control. It receives ring, carrier, clear to send, and secondary received data from the data set. It transmits data terminal ready, request to send, force busy, and secondary transmitted data to the data set. (Request to send and force busy are jumper-selectable.) If data set interrupts are enabled, a change in state on any of the received control lines initiates a receiver interrupt. Data is received on the received data line and transmitted on the transmitted data line. Handshake sequences are under program control.

DC-to-DC Power Inverter

The power inverter uses the +12V from the backplane to produce −12V for the peripheral interface and data buffer circuitry. It consists of an oscillator, rectifier, inductive charge pump, and a zener regulator.

CONFIGURATION

General

The following paragraphs describe how the user can configure the module to function within his system. The user can select the register addresses, interrupt vectors, data format, baud rate, and interface mode. The descriptions of the registers and their standard factory addresses are listed in Table 1. The jumpers used on this module consist of wire-wrap pins to which the connections are made; their locations are shown in Figures 2 and 3. A complete listing of the jumpers and a description of their functions are contained in Table 2.

Addresses for the DLV11-E can range from 160000 through 177770_8. The least significant three bits (only bits 1 and 2 are used; bit 0 is ignored) address the desired registers in the module, as described in Table 1. Address bits 3 through 12 are jumper-selected as illustrated in Figure 3.

Since each module has four registers, each requires four addresses. Addresses 177560—177566 are reserved for the module used with the console peripheral device. Additional modules should be assigned addresses from 175610 through 176176, allowing up to 30 additional DLV11-E modules to be addressed.

Table 1 Standard Assignments

Description	Mnemonic	Console Module	Second Module
Register			
Receiver Control/Status	RCSR	177560	175610
Receiver Data Buffer	RBUF	177562	175612
Transmit Control/Status	XCSR	177564	175614
Transmit Data Buffer	XBUF	177566	175616
Interrupts			
Receiver		60	300
Transmitter		64	304

DLV11-E

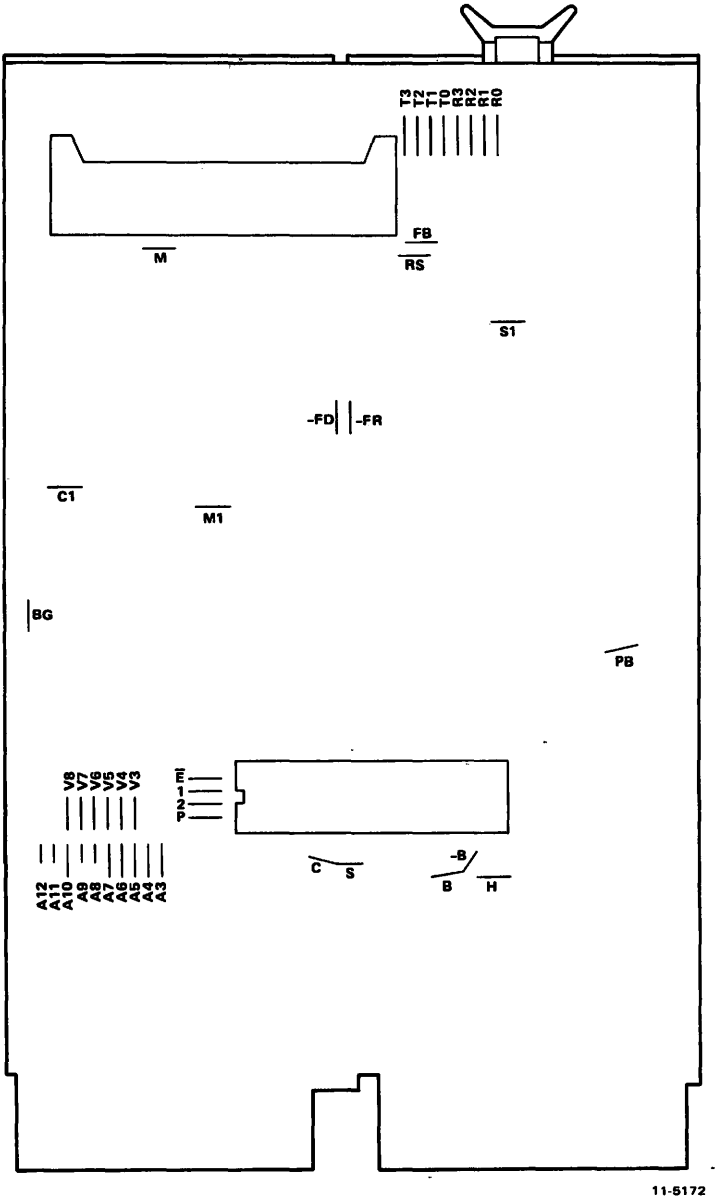


Figure 2 DLV11-E Jumper Locations

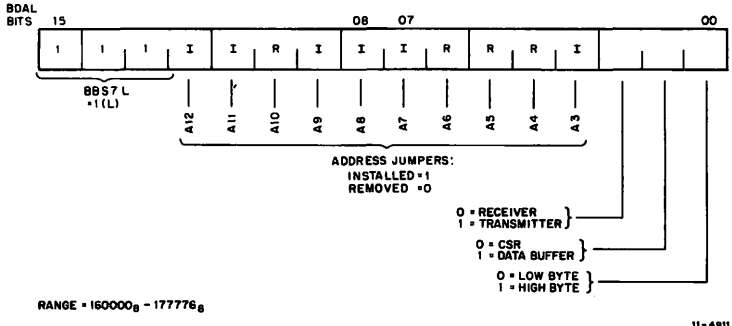


Figure 3 DLV11-E Addressing

Table 2 DLV11-E Jumper Definitions

NOTE

Jumpers are inserted to enable the function they control except for those jumpers which indicate negation (such as "−B" and "E"). Negated jumpers are removed to enable the functions they control.

Jumper	Function
A3-A12	These jumpers correspond to bits 3 through 12 of the address word. When inserted, they will cause the bus interface to check for a true condition on the corresponding address bit.
V3-V8	Used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding vector bit on the LSI-11 bus.
R0-R3	Receiver and transmitter baud rate select jumpers during common speed operation. Receiver-only baud rate select jumpers during split speed operation as defined in Table 3.
T0-T3	Transmitter baud rate select jumpers during split speed operation. Both receiver and transmitter baud rate if maintenance mode is entered during split speed operation as defined in Table 3.

BG	Jumper is inserted to enable break generation.
P	Jumper is inserted for operation with parity.
E	Removed for even parity; inserted for odd parity.
1, 2	These jumpers select the desired number of data bits, as defined in Table 4.
PB	Jumper is inserted to enable the programmable baud rate capability.
C, C1	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted.)
S, S1	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.)
H	This jumper is inserted to assert BHALT L when a framing error is received, except when the maintenance bit is set. This places the processor in the halt mode.
B, −B	Jumper B is inserted to negate BDCOK H when a break signal or framing error is received, except when the maintenance bit is set. This causes the processor to reboot. (Jumper −B must be removed when B is inserted.)
−FD	Jumper is removed to force data terminal ready signal on.
−FR	Jumper is removed to force request to send signal on.
RS	This jumper is inserted to enable normal transmission of the request to send signal.
FB	Inserted to enable transmission of the force busy signal (for Bell model 103E data sets).
M, M1	These are test jumpers used during the manufacture of the module. They are not defined for field use.

Interrupt Vectors

The interrupt vectors are selected by using jumpers V3 to V8. The standard configuration is shown in Figure 4 and Table 1. The vectors can range from 001 through 774. Note that vectors 60 and 64 are reserved for the console device. Additional DLV11-E modules should be assigned vectors following any DRV11 parallel interface modules installed in the system that start at address 300.

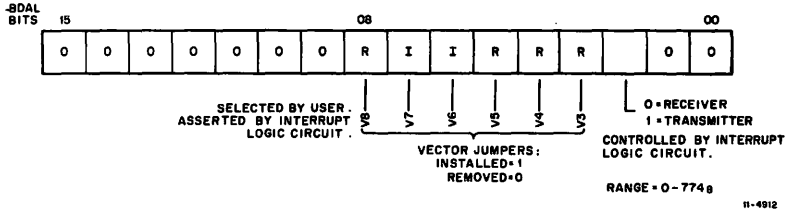


Figure 4 DLV11-E Interrupt Vector

Baud Rate Selection

The DLV11-E allows the user to configure jumpers T0-T3 and R0-R3 for the transmit baud rate and the receiver baud rate as shown in Table 3.

Data Bit Selection

The number of data bits being transmitted or received by the DLV11-E is user-selectable by installing or removing jumpers 1 and 2. The specific number of data bits as controlled by the configuration of jumpers 1 and 2 is shown in Table 4.

Factory Configuration

The user can reconfigure any of the jumpers to make the module meet his requirements. The factory configuration as shipped is shown in Table 5 to help the user determine if any changes are required.

Registers

The word format for the DLV11-E CSR is shown in Figure 5 and its functions are described in Table 6.

Table 3 DLV11-E Baud Rate Selection

Program Control / Receive Jumpers / Transmit Jumpers / Baud Rate	Bit 15 R3 T3	Bit 14 R2 T2	Bit 13 R1 T1	Bit 12 R0 T0	Bit 11*
50	I	I	I	I	
75	I	I	I	R	
110	I	I	R	I	
134.5	I	I	R	R	
150	I	R	I	I	
300	I	R	I	R	
600	I	R	R	I	
1200	I	R	R	R	
1800	R	I	I	I	
2000	R	I	I	R	
2400	R	I	R	I	
3600	R	I	R	R	
4800	R	R	I	I	
7200	R	R	I	R	
9600	R	R	R	I	
19200	R	R	R	R	

I = jumper inserted = program bit cleared.
R = jumper removed = program bit set.

* Bit 11 of the XCSR (write-only bit) must be set in order to select a new baud rate under program control. Also, jumper PB must be inserted to enable baud rate selection under program control.

Table 4 DLV11-E Data Bit Selection

Jumpers 2	1	Number of Data Bits
I	I	5
I	R	6
R	I	7
R	R	8

Table 5 DLV11-E Factory Jumper Configuration

Jumper Designation	Jumper State	Function Implemented
A3	I	Jumpers A3 through A12 implement device address 17561X. The least significant octal digit is hardwired on the module to address the four device registers as follows:
A4	R	
A5	R	
A6	R	
A7	I	
A8	I	X = 0 RCSR
A9	I	X = 2 RBUF
A10	R	X = 4 XCSR
A11	I	X = 6 XBUF
A12	I	
V3	R	This jumper selection implements interrupt vector address 300_8 for receiver interrupts and 304_8 for transmitter interrupts.
V4	R	
V5	R	
V6	I	
V7	I	
V8	R	
R0	I	This module is configured to receive at 110 baud.
R1	R	
R2	I	
R3	I	

T0	I	The transmitter is configured for 9600
T1	R	baud if split speed operation is used.
T2	R	
T3	R	
BG	I	Break generation is enabled
P	R	Parity bit is disabled.
E	R	Parity type is not applicable when P is removed
1	R	Operation with eight data bits per char-
2	R	acter
PB	R	Programmable baud rate function disabled.
C	I	Common speed operation enabled.
C1	I	
S	R	Split speed operation disabled.
S1	R	
H	R	Halt on framing error disabled.
B	R	Boot on framing error disabled.
−B	I	
FD	I	The data terminal ready signal is not forced continuously true.
RS	I	The circuitry controlling the request to send signal is enabled.
FB	R	The force busy signal is disabled.
EF	R	Error flags are enabled.
MT	R	Maintenance bit is disabled.
M	R	Factory test jumpers. Not defined for
M1	R	field use.

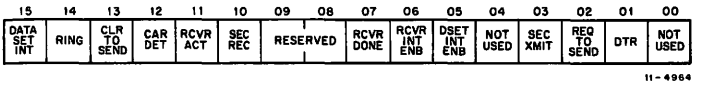


Figure 5 DLV11-E RCSR Register Word Format

Table 6 DLV11-E RCSR Bit Assignments

Bit: 15 **Name:** DATA SET INT
Description: (Data Set Interrupt)
This bit initiates an interrupt sequence provided the DSET INT ENB (bit 5) is also set.

This bit is set whenever CAR DET, CLR TO SEND, or SEC REC changes state, i.e., on a 0 to 1 or 1 to 0 transition of any one of these bits. It is also set when RING changes from 0 to 1.
Cleared by INIT or by reading the RCSR. Because reading the register clears the bit, it is, in effect, a "read-once" bit.

Bit: 14 **Name:** RING
Description: When set, indicates that a ringing signal is being received from the data set. Note that the ringing signal is not a level but an EIA control with a duty cycle of 2 seconds ON and 4 seconds OFF.
Read-only bit.

Bit: 13 **Name:** CLR TO SEND
Description: (Clear to Send)
This state of this bit is dependent on the state of the clear to send signal from the data set. When set, this bit indicates an ON condition; when clear, it indicates an OFF condition.
Read-only bit.

Bit: 12 **Name:** CAR DET
Description: (Carrier Detect)
This bit is set when the data carrier is received. When clear, it indicates either the end of the current transmission activity or an error condition.
Read-only bit.

Bit: 11 **Name:** RCVR ACT
Description: (Receiver Active)
When set, this bit indicates that the DLV11-E's receiver is active. The bit is set at the center of the start bit, which is the beginning of the input serial data from the device, and is cleared by the leading edge of RDONE H.
Read-only bit; cleared by INIT or by RDONE H (bit 7).

Bit: 10 **Name:** SEC REC
Description: (Secondary Received or Supervisory Received Data)
This bit provides a receive capability for the reverse channel of a remote station. A space (+6V) is read as a 1. (A transmit capability is provided by bit 3.)
Read-only bit.

Bit: 9-8 **Name:** Not Used
Description: Reserved for future use.

Bit: 7 **Name:** RCVR DONE
Description: (Receiver Done)
This bit is set when an entire character has been received and is ready for transfer to the processor. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 6) is also set.

Cleared whenever the receiver buffer (RBUF) is addressed. Also cleared by INIT.

Read-only bit.

Bit: 6 **Name:** RCVR INT ENB
Description: (Receiver Interrupt Enable)
When set, allows an interrupt sequence to start when RCVR DONE (bit 7) sets.

Read/write bit; cleared by INIT.
(See Note 1.)

Bit: 5 **Name:** DSET INT ENB
Description: (Data Set Interrupt Enable)
When set, allows an interrupt sequence to start when DATA SET INT (bit 15) sets.

Read/write bit; cleared by INIT.
(See Note 1.)

Bit: 4 **Name:** Not Used
Description: Reserved for future use.

Bit: 3 **Name:** SEC XMIT
Description: (Secondary Transmitted or Supervisory Transmitted Data)
This bit provides a transmit capability for a reverse channel of a remote station. When set, transmits a space (approx. +11.5V). (A receive capability is provided by bit 10.)

Read/write bit; cleared by INIT.

Bit: 2 **Name:** REQ TO SEND
Description: (Request to Send)
A control lead to the data set which is required for transmission. A jumper on the DLV11-E ties this bit to REQ TO SEND or force busy in the data set.

Read/write bit; cleared by INIT.

Bit: 1 **Name:** DTR
Description: (Data Terminal Ready)
A control lead for the data set communication channel. When set, permits connection to the channel. When clear, disconnects the interface from the channel.

Read/write bit; must be cleared by the program; is not cleared by INIT. (See Note 2.)

NOTES

1. When clearing an interrupt enable bit, first set the appropriate processor status bit = 1. After the interrupt enable bit at the module is cleared, the processor may be returned to its normal priority.
2. The state of this bit is not defined after power-up.
3. INIT = LSI-11 bus BINIT signal assertion.

The word format for the DLV11-E RBUF register is shown in Figure 6 and its functions are described in Table 7.

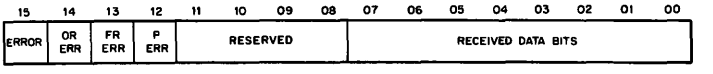


Figure 6 DLV11-E RBUF Register Word Format

Table 7 DLV11-E RBUF Bit Assignments

Bit: 15 **Name:** ERROR
Description: (Error)
Used to indicate that an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13, and 12, respectively). Whenever one of these bits is set, it causes error to set. This bit is not connected to the interrupt logic.

Read-only bit; cleared by removing the error-producing condition.

NOTE

Error indications remain present until the next character is received, at which time the error bits are updated. INIT clears the error bits.

Bit: 14 **Name:** OR ERR
Description: (Overrun Error)
When set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character.

Read-only bit. Cleared by INIT.

Bit: 13 **Name:** FR ERR
Description: (Framing Error)
When set, indicates that the character that was read had no valid stop bit.

Read-only bit. Cleared by INIT.

Bit: 12 **Name:** P ERR
Description: (Parity Error)
When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected.

Read-only bit. Cleared by INIT.

Bit: 11-8 **Name:** Not Used
Description: Reserved for future use.

Bit: 7-0 **Name:** RECEIVED DATA
Description: Holds the character just read. If less than eight bits are selected, then the buffer is right-justified into the least significant bit positions. In this case, the unused bits are read as 0s.

Read-only bits; not cleared by INIT.

NOTE

INIT = LSI-11 bus BINIT signal assertion.

The word format for the DLV11-E XCSR register is shown in Figure 7 and its functions are described in Table 8.

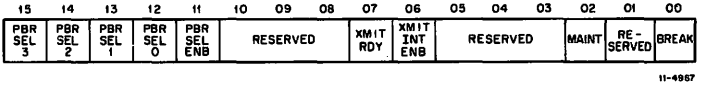


Figure 7 DLV11-E XCSR Register Word Format

Table 8 DLV11-E XCSR Bit Assignments

Bit: 15-12 **Name:** PBR SEL
Description: (Programmable Baud Rate Select)
When set, these bits choose a baud rate from 50-9600 baud. See Table 3.

Write-only bits.

Bit: 11 **Name:** PBR ENB
Description: (Programmable Baud Rate Enable)
This bit must be set in order to select a new baud rate inciated by bits 12 to 15.

Write-only bits.

Bit: 10-8 **Name:** Not Used
Description: Reserved for future use.

Bit: 7 **Name:** XMIT RDY
Description: (Transmitter Ready)
This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT ENB (bit 6) is also set.

Bit: 6 **Name:** XMIT INT ENB
Description: (Transmitter Interrupt Enable)
When set, allows an interrupt sequence to start when XMIT RDY (bit 7) is set.

Read/write bits; cleared by INIT.
(See Note.)

Bit: 5-3 **Name:** Not Used
Description: Reserved for future use.

Bit: 2 **Name:** MAINT
Description: Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed when common speed operation is enabled.

Read/write bit; cleared by INIT.

Bit: 1 **Name:** Not Used.
Description: Reserved for future use.

Bit: 0 **Name:** BREAK
Description: When set, transmits a continuous space to the external device.

Read/write bit; cleared by INIT.

NOTE

When clearing an interrupt enable bit, first set the appropriate processor status word bit = 1. After the interrupt enable bit at the module is cleared, the processor may be returned its normal priority.

The word format for the DLV11-E XBUF register is shown in Figure 8 and its functions are described in Table 9.

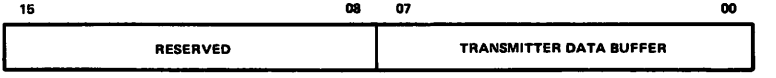


Figure 8 DLV11-E XBUF Register Word Format

Table 9 DLV11-E XBUF Bit Assignments

Bit: 15-8 **Name:** Not Used
Description: Not defined. Not necessarily read as 0s.

Bit: 7-0 **Name:** TRANSMITTER DATA BUFFER
Description: Holds the character to be transferred to the external device. If less than eight bits are used, the character must be loaded so that it is right-justified into the least significant bits.

Write-only bits. Not necessarily read as 0s.

Installation

Prior to installing the DLV11-E on the backplane, first establish the desired priority level to determine the backplane slot in which the module will be installed. Then, check that module configuration jumpers are configured as required for your application. Connection to the peripheral device is via an optional BC05C-X* modem cable for EIA interface applications.

The BC05C cable provides the correct connection to the 40-pin connector on the DLV11-E. The peripheral device end of the cable is terminated with a Cinch DB25P connector that is pin-compatible with Bell 103, 113, 202C, 202D, and 212 modems. Connector pinning and signal levels conform to EIA specification RS-232C. The EIA interface circuit is shown in Figure 9; jumpers are shown in Figure 2.

*X= Length in feet. Standard length is 25 feet.

DLV11-E

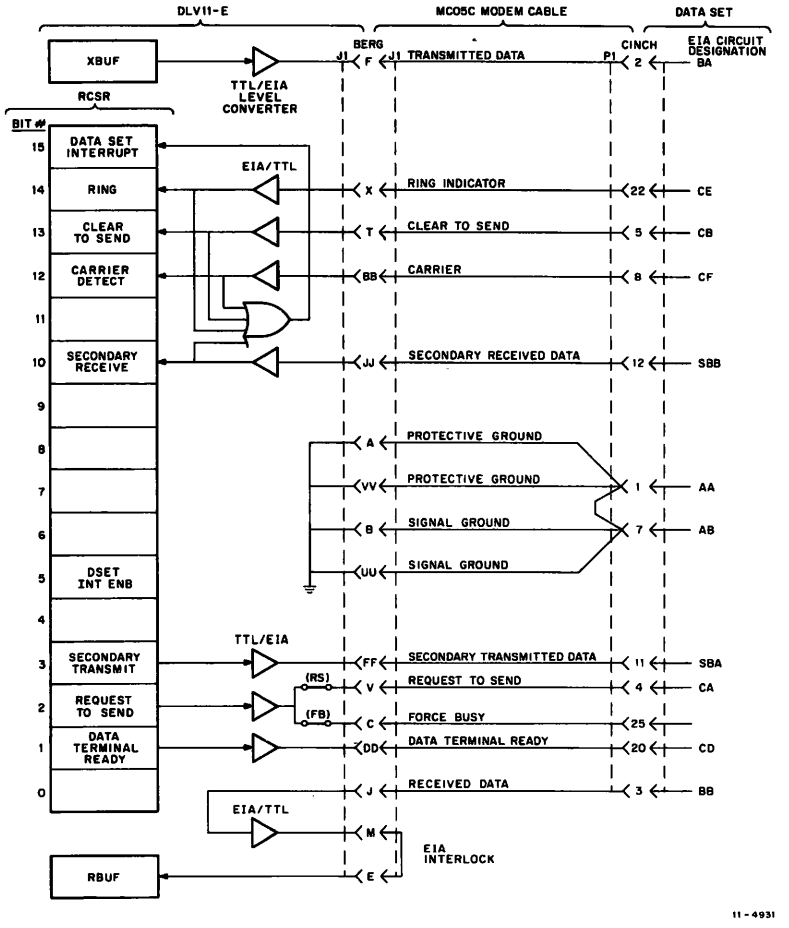


Figure 9 DLV11-E Peripheral Interface Signal Flow

DLV11-F ASYNCHRONOUS LINE INTERFACE

GENERAL

The DLV11-F asynchronous line interface module interfaces the LSI-11 bus to any of several standard types of serial communications lines. The module receives serial data from peripheral devices, assembles it into parallel data, and transfers it to the LSI-11 bus. It accepts data from the LSI-11 bus, converts it into serial data, and transmits it to the peripheral devices. The DLV11-F supports either 20 mA current loop or EIA-standard lines, but does not include modem control.

FEATURES

- Jumper- or program-selectable, crystal-controlled baud rates: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, and 19,200. Split transmit and receive baud rates are possible.
- Provisions for user-supplied external clock inputs for baud rate control.
- Jumper-selectable data bit formats.
- LSI-11 bus interface and control logic for interrupt processing and vectored addressing of interrupt service routines.
- Control, status, and data buffer registers directly accessible via processor instructions.
- Support for "data leads only" modem (Bell type 103, 113).
- Generation of reader run signal for use with ASR-type terminals (when equipped with reader run relay).

SPECIFICATIONS

Identification	M8028
Size	Double
Power	+5.0 Vdc ±5% at 1.0 A +12.0 Vdc ±3% at 0.18 A
Bus loads	
AC	2.2
DC	1.0

DESCRIPTION

General

Major functions of the DLV11-F are shown in Figure 1. Communications between the processor and the DLV11 are executed via programmed I/O operations or interrupt-driven routines.

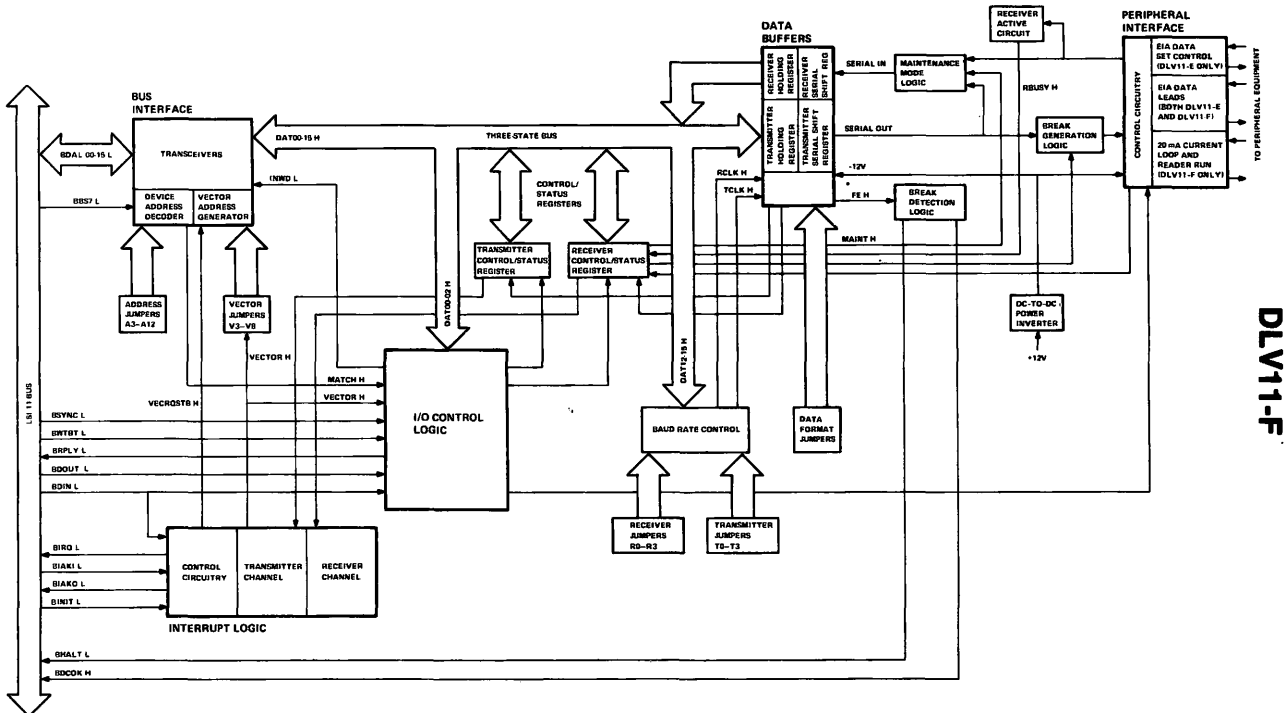


Figure 1 DLV11-F Asynchronous Line Interface Logic Block Diagram

Bus Interface

The bus interface circuit signal levels consist of data moving between the LSI-11 bus and the module's internal tri-state bus. The interface decodes the device address and produces an address match (MATCH H) signal, and places interrupt vectors on the LSI-11 bus. The interface receives from the LSI-11 bus unless it is switched to transmit to the LSI-11 bus. The interrupt logic can cause the bus interface to transmit either a transmitter or a receiver interrupt vector; the I/O control logic can cause the interface to transmit or receive data to or from the LSI-11 bus.

The interface receives LSI-11 bus lines BDAL00 L through BDAL15 L and places them on the module's tri-state bus. If BBS7 L is asserted, the circuit decodes BDAL03 L through BDAL12 L and asserts MATCH H. Jumpers A3-A12 are configured to let the option respond to specific device register addresses. Jumpers V3-V8 select the option's interrupt vector.

I/O Control Logic

When the I/O control logic receives MATCH H from the bus interface, it decodes tri-state bus lines DAT00 H through DAT02 H and selects the addressed device register. The I/O control logic exchanges bus control signals with the processor to perform input and output data transfers. During an interrupt transaction, VECTOR H from the interrupt logic causes the circuit to assert BRPLY L in response to BDIN L. During data transactions, the I/O control logic asserts INWD L to switch the bus interface transceivers from receiving to transmitting.

Control/Status Registers

The receiver control/status register (RCSR) and the transmitter control/status register (XCSR) are enabled by selection signals from the I/O control logic. The CSRs are byte addressable for reading status bits or writing control bits.

Data Buffers

The receiver buffer (RBUF) and transmitter buffer (XBUF) provide double-buffering in that one byte of data can be held while another byte is entering or exiting. This allows asynchronous, full duplex operation. Data is handled in the low byte of the registers. The buffer control circuitry places receiver buffer error flag bits in the high byte of the RBUF. If also sends a status bit to the RCSR and a framing error bit (FE H) to the break logic.

Receiver Active Circuit
This circuit monitors the received serial data line and sets a status bit (RCVR ACT) as soon as the RBUF begins receiving data. It clears the bit when a full character of data has been received.

Interrupt Logic
The DLV11-F can generate transmitter interrupts. If the XBUF is ready to serialize another character of data and the transmitter interrupt enable bit is set in the XCSR, the interrupt logic requests to interrupt the processor (by asserting BIRQ L). If the processor acknowledges via the BIAKI/BIAKO daisy-chain, the interrupt logic asserts VECTOR H and VECRQSTB H. These signals cause the bus interface to place the transmitter function interrupt vector address on the LSI-11 bus.

The module also can request a receiver interrupt if the RBUF has received a character and the receiver interrupt bit is set in the RCSR. When the interrupt request is acknowledged, the interrupt logic asserts VECTOR H. VECTOR H causes the bus interface circuit to place the receiver function interrupt vector address on the LSI-11 bus. (VECRQSTB H is used only for a transmitter interrupt.)

The interrupt acknowledge daisy-chain (BIAKI/BIAKO) passes through both the receiver and transmitter sections of the interrupt logic. It goes through the receiver section first, thereby giving the receiver channel priority over the transmitter channel.

Baud Rate Control
The baud rate control establishes the speed at which the data buffers handle serial data. It produces clock signals by dividing a crystal oscillator frequency by an amount selected by jumpers or by the program. The circuit can be jumpered to generate either independent transmitter and receiver clocks (split speed operation) or a common clock (common speed operation).

When the programmable baud rate enable bit is set in the XCSR, the baud rate control decodes tri-state bus lines DAT12 H through DAT15 H. These bits control the receive baud rate in split speed operation and both transmit and receive baud rate in common speed operation. When programmable baud rate is not enabled, the baud rates are controlled by jumpers. In split speed operation, jumpers R0-R3 control the receive baud rate and jumpers T0-T3 control the transmit baud rate. In common speed operation, R0-R3 control both baud rates.

The circuit has provisions for a user-supplied external clock.

Break Logic

A break signal is a continuous spacing condition on the serial data line. If the break bit is set in the XCSR, the module will transmit a break signal to the peripheral device (normally another processor). If the module receives a break signal from the peripheral device (normally a console device), the RBUF control circuitry interprets the absence of stop bits as a framing error. The circuit can be jumpered to ignore the framing error, to place the processor in the halt mode, or to cause the processor to reboot. The break logic asserts BHALT L to halt the processor. It negates BDCOK H to reboot.

Maintenance Mode Logic

The modules can check out their data paths up to (but not including) the peripheral interface circuit by looping the XBUF's serial output back to the RBUF's serial input. Data from the LSI-11 bus still goes to the peripheral device, but no data is received from the peripheral in this maintenance mode. The program can compare received (looped) data with transmitted data to check for errors. The maintenance mode is entered by setting the maintenance bit in the XCSR.

Peripheral Interface

This circuit can be jumpered to support either EIA-level data leads (no modem control) or 20 mA current loop modes. When interfacing EIA-level data leads ("data leads only" operation), request to send, force busy, and data terminal ready are continuously true by separate EIA drivers. No modem control signals are received.

In the current loop mode of operation, the circuit uses optical isolators to interface TTL to 20 mA current loops. This operation is jumper-selectable for either active or passive operation of the transmitter and receiver circuitry.

The peripheral interface also produces a reader run current to advance the paper tape reader on a peripheral equipped with a reader run relay. This is controlled by the reader enable bit in the DLV11-F's RCSR.

DC-to-DC Power Inverter

The power inverter uses the +12V from the backplane to produce −12V for the peripheral interface and data buffer circuitry. It consists of an oscillator, rectifier, inductive charge pump, and a zener regulator.

DLV11-F

CONFIGURATION

General

The following paragraphs describe how the user can configure the module to function within his system. The user can select the register addresses, interrupt vectors, data format, baud rate, and interface mode. The registers and their standard factory addresses are listed in Table 1. The jumpers used on this module consist of wire-wrap pins to which the connections are made; their locations are shown in Figure 2. A complete listing of the jumpers and a description of their functions are listed in Table 2.

Addresses

Addresses for the DLV11-F can range from 160000_8 through 177770_8. The least significant three bits (only bits 1 and 2 are used; bit 0 is ignored) address the desired registers in the module, as shown in Table 1. Address bits 3 through 12 are jumper-selected as shown in Figure 3.

Since each module has four registers, each requires four addresses. Addresses 177560—177566 are reserved for the module used with the console peripheral device. Additional modules should be assigned addresses from 176500 through 176670, allowing up to 30 additional DLV11-F modules to be addressed.

Interrupt Vectors

The interrupt vectors are selected by using jumpers V3 to V8. The standard configuration is shown in Figure 4 and Table 1. The vectors can range from 001 through 774_8. Note that vectors 60_8 and 64_8 are reserved for the console device. Additional DLV11-F modules should be assigned vectors following any DRV11 peripheral interface module installed in the system that starts at address 300_8.

Table 1 Standard Assignments

Description	Mnemonic	Console Module	Second Module
Register			
Receiver Control/Status	RCSR	177560	176500
Receiver Data Buffer	RBUF	177562	176502
Transmit Control/Status	XCSR	177564	176504
Transmit Data Buffer	XBUF	177566	176506
Interrupts			
Receiver		60	300
Transmitter		64	304

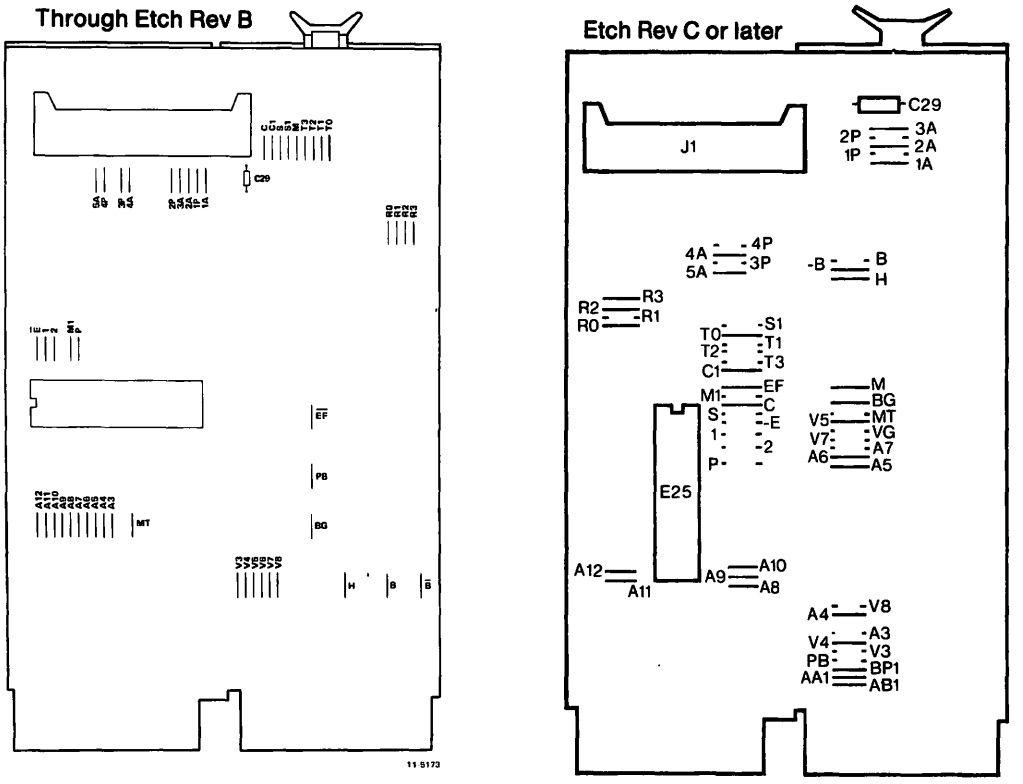


Figure 2 DLV11-F Jumper Locations

Table 2 DLV11-F Jumper Definitions

NOTE

Jumpers are inserted to enable the function they control except for those jumpers which indicate negation (such as "−B" and "E"). Negated jumpers are removed to enable the functions they control.

Jumper	Function
A3-A12	These jumpers correspond to bits 3 through 12 of the address word. When inserted, they cause the bus interface to check for a true condition on the corresponding address bit.
V3-V8	Used to generate the vector during an interrupt transaction. Each inserted jumper asserts the corresponding vector bit on the LSI-11 bus.
R0-R3	Receiver and transmitter baud rate select jumpers during common speed operation.
	Receiver-only baud rate select jumpers during split speed operation, as defined in Table 3.
T0-T3	Transmitter baud rate select jumpers during split speed operation.
	Both receiver and transmitter baud rate if maintenance mode is entered during split speed operation, as defined in Table 3.
BG	Jumper is inserted to enable break generation.
P	Jumper is inserted for operation with parity.
E	Receiver checks for appropriate parity and transmitter inserts appropriate parity.
1, 2	These jumpers select the desired number of data bits, as defined in Table 4.
PB	Jumper is inserted to enable the programmable baud rate capability.
C, C1	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted.)

S, S1	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.)
H	This jumper is inserted to assert BHALT L when a framing error is received, except when the maintenance bit is set. This places the processor in the halt mode.
B, −B	Jumper B is inserted to negate BDCOK H when a break signal or framing error is received, except when the maintenance bit is set. This causes the processor to reboot. (Jumper −B must be removed when B is inserted.)
1A, 2A, 3A	These three jumpers are inserted to make the 20 mA current loop receiver active. (Jumpers 1P and 2P must be removed when 1A, 2A, and 3A are inserted.)
1P, 2P	These jumpers are inserted to make the 20 mA current loop receiver passive. (Jumpers 1A, 2A, and 3A must be removed when 1P and 2P are installed.)
4A, 5A	Inserted to make the 20 mA current loop transmitter active. (Jumpers 3P and 4P must be removed when 4A and 5A are inserted.)
3P, 4P	Inserted to make the 20 mA current loop transmitter passive. (Jumpers 4A and 5A must be removed when 3P and 4P are inserted.)
EF	Jumper is removed to enable the error flags to be read in the high byte of the receiver buffer.
M, M1	These are test jumpers used during the manufacture of the module. They are not defined for field use.

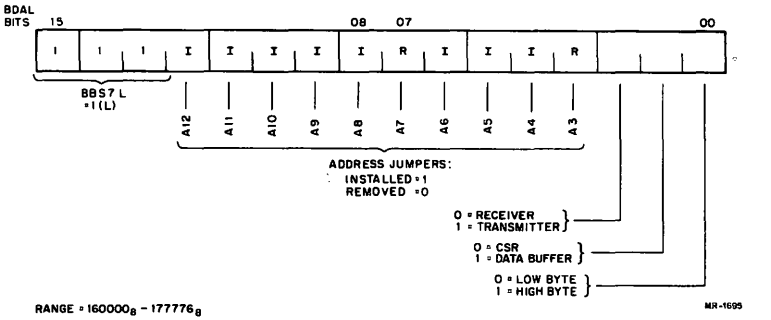


Figure 3 DLV11-F Addressing

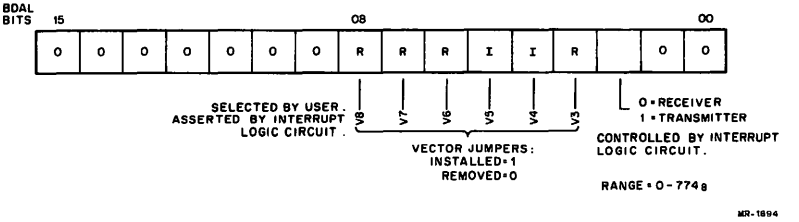


Figure 4 DLV11-F Interrupt Vectors

Baud Rate Selection

The DLV11-F allows the user to configure jumpers T0-T3 and R0-R3 for the transmit baud rate and the receiver baud rate as shown in Table 3.

Data Bit Selection

The number of data bits transmitted or received by the DLV11-F is user-selectable by installing or removing jumpers 1 and 2. The specific number of data bits as controlled by the configuration of jumpers 1 and 2 is shown in Table 4.

Table 3 DLV11-F Baud Rate Selection

Program Control Receive Jumpers Transmit Jumpers	Bit 15 R3 T3	Bit 14 R2 T2	Bit 13 R1 T1	Bit 12 R0 T0	Bit 11* Baud Rate
	I	I	I	I	50
	I	I	I	R	75
	I	I	R	I	110**
	I	I	R	R	134.5
	I	R	I	I	150
	I	R	I	R	300
	I	R	R	I	600
	I	R	R	R	1200
	R	I	I	I	1800
	R	I	I	R	2000
	R	I	R	I	2400
	R	I	R	R	3600
	R	R	I	I	4800
	R	R	I	R	7200
	R	R	R	I	9600
	R	R	R	R	19200

I = Jumper inserted = program bit cleared
R = Jumper removed = program bit set

* Bit 11 of the XCSR (write-only bit) must be set in order to select a new baud rate under program control. Also, jumper PB must be inserted to enable baud rate selection under program control.

** When configured for 110 baud, the UART is set for two stop bits.

Table 4 DLV11-F Data Bit Selection

Jumpers		Number of Data Bits
2	1	
I	I	5
I	R	6
R	I	7
R	R	8

Factory Configuration

The user can reconfigure any of the jumpers to make the module meet his requirements. The factory configuration, as shipped, is shown in Table 5 to assist the user in determining what changes are needed.

Table 5 DLV11-F Factory Jumper Configuration

Jumper Designation	Jumper State	Function Implemented
A3	R	Jumpers A3 through A12 implement device address 17756X. The least significant octal digit is hardwired on the module to address the four device registers as follows: X = 0 RCSR X = 2 RBUF X = 4 XCSR X = 6 XBUF
A4	I	
A5	I	
A6	I	
A7	R	
A8	I	
A9	I	
A10	I	
A11	I	
A12	I	
V3	R	This jumper selection implements interrupt vector 60_8 for receiver interrupts and 64_8 for transmitter interrupts.
V4	I	
V5	I	
V6	R	
V7	R	
V8	R	
R0	I	The module is configured to receive at 110-baud.
R1	R	
R2	I	
R3	I	
T0	I	The transmitter is configured for 9600 baud if split speed operation is used.
T1	R	
T2	R	
T3	R	
BG	I	Break generation is enabled.

P	R	Parity bit is disabled.
E	R	Parity type is not applicable when P is removed
1	R	Operation with eight data bits per character.
2	R	
PB	R	Programmable baud rate function disabled.
C	I	Common speed operation enabled.
C1	I	
S	R	Split speed operation disabled.
S1	R	
H	I	Halt on framing error enabled.
B	R	Boot on framing error disabled.
−B	I	
1A	I	The 20 mA current loop receiver is configured as an active receiver.
2A	I	
3A	I	
1P	R	
2P	R	
4A	I	The 20 mA current loop transmitter is configured for active operation.
5A	I	
3P	R	
4P	R	
EF	I	Error flags are disabled.
MT	R	Maintenance bit disabled.
M	R	Factory test jumpers. Not defined for field use.
M1	R	

Registers

The word format for the DLV11-F RCSR is shown in Figure 5 and functionally described in Table 6.

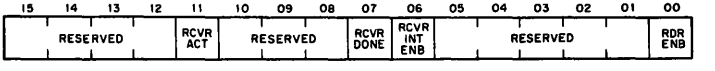


Figure 5 DLV11-F RCSR Word Format

Table 6 DLV11-F RCSR Bit Assignments

Bit: 15-12 **Name:** Not used
Description: Reserved for future use.

Bit: 11 **Name:** RCVR ACT
Description: (Receiver Active)
When set, this bit indicates that the DLV11-F interface receiver is active. The bit is set at the center of the start bit, which is the beginning of the input serial data from the device and is cleared by the leading edge of RDONE H.

Read-only bit; cleared by INIT or by RCVR DONE (bit 7).

Bit: 10-8 **Name:** Not used
Description: Reserved for future use.

Bit: 7 **Name:** RCVR DONE
Description: (Receiver Done)
This bit is set when an entire character has been received and is ready for transfer to the processor. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 6) is also set.

Read-only bit.

Bit: 6 **Name:** RCVR INT ENB
Description: (Receiver Interrupt Enable)
When set, allows an interrupt sequence to start when RCVR DONE (bit 7) sets.

Read/write bit; cleared by INIT.

Bit: 5-1 **Name:** Not used
Description: Reserved for future use.

Bit: 0 **Name:** RDR ENB
Description: (Reader Enable)
When set, this bit advances the paper tape reader in DIGITAL-modified TTY units (LT33-C, LT35-A, C) and clears the RCVR DONE bit (bit 7).

This bit is cleared at the middle of the start bit, which is the beginning of the serial input from an external device. Also cleared by INIT.

Write-only bit.

NOTE

INIT = LSI-11 bus BINIT signal assertion.

The word format for the DLV11-F RBUF register is shown in Figure 6 and functionally described in Table 7.

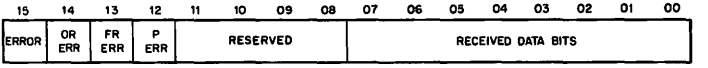


Figure 6 DLV11-F RBUF Word Format

Table 7 DLV11-F RBUF Bit Assignments

Bit: 15 **Name:** ERROR
Description: Used to indicate that an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13, and 12, respectively). Whenever one of these bits is set, it causes bit 15 to set. This bit is not connected to the interrupt logic.

Read-only bit; cleared by removing the error-producing condition.

NOTE

Error indications remain present until the next character is received, at which time the error bits are updated. INIT clears the error bits.

Bit: 14 **Name:** OR ERR
Description: (Overrun Error)
When set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character.

Read-only bit. Cleared by INIT.

Bit: 13 **Name:** FR ERR
Description: (Framing Error)
When set, indicates that the character that was read had no valid stop bit.

Read-only bit. Cleared by INIT.

Bit: 12 **Name:** P ERR
Description: (Parity Error)
When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected.

Read-only bit. Cleared by INIT.

Bit: 11-8 **Name:** Not used
Description: Reserved for future use.

Bit: 7-0 **Name:** RECEIVED DATA BITS
Description: Holds the character just read. If less than eight bits are

selected, then the buffer is right-justified into the least significant bit positions. In this case, the higher unused bit or bits are read as 0s.

Read-only bits; not cleared by INIT.

NOTE

INIT = LSI-11 bus BINIT signal assertion.

The word format for the DLV11-F XCSR register is shown in Figure 7 and functionally described in Table 8.

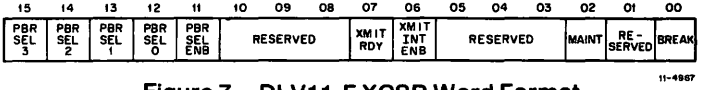


Figure 7 DLV11-F XCSR Word Format

Table 8 DLV11-F XCSR Bit Assignments

Bit: 15-12 **Name:** PBR SEL
Description: (Programmable Baud Rate Enable)
When set, these bits choose a baud rate from 50-9600 baud. See Table 3.

Write-only bits.

Bit: 11 **Name:** PBR ENB
Description: (Programmable Baud Rate Enable)
This bit must be set in order to select a new baud rate indicated by bits 12 to 15.

Write-only bits.

Bit: 10-8 **Name:** Not used
Description: Reserved for future use.

Bit: 7 **Name:** XMIT RDY
Description: (Transmitter Ready)
This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT ENB (bit 6) is also set.

Bit: 6 **Name:** XMIT INT ENB
Description: (Transmitter Interrupt Enable)
When set, allows an interrupt sequence to start when XMIT RDY (bit 7) is set.

Read/write bit; cleared by INIT. (See Note.)

Bit: 5-3 **Name:** Not used
Description: Reserved for future use.

Bit: 2 **Name:** MAINT
Description: Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed when common speed operation is enabled.

Read/write bit; cleared by INIT.

Bit: 1 **Name:** Not used
Description: Reserved for future use.

Bit: 0 **Name:** BREAK
Description: When set, transmits a continuous space to the external device.

Read/write bit; cleared by INIT.

NOTE

When clearing an interrupt enable bit, first set the appropriate processor status word bit = 1. After the interrupt enable bit at the module is cleared, the processor may be returned to its normal priority.

The word format for the DLV11-F XBUF register is shown in Figure 8 and functionally described in Table 9.

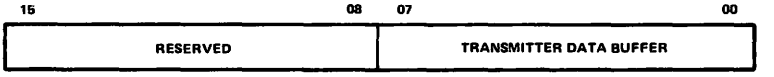


Figure 8 DLV11-F XBUF Word Format

Table 9 DLV11-F XBUF Bit Assignments

Bit: 15-8 **Name:** Not Used
Description: Not defined. Not necessarily read as 0s.

Bit: 7-0 **Name:** TRANSMITTER DATA BUFFER
Description: Holds the character to be transferred to the external device. If fewer than eight bits are used, the character must be loaded so it is right-justified into the least significant bits.

Write-only bits. Not necessarily read as 0s.

DLV11-F

Installation

Before installing the DLV11-F on the backplane, first establish the desired priority level to determine in which backplane slot to install the module. Then ensure that the module configuration jumpers are configured correctly for your application. Connection to the peripheral device is via an optional data interface cable. Cables are listed below.

Application	Cable Type*
EIA Interface	BC01V-X or BC05C-X Modem Cable
20 mA Current Loop	BC05M-X Cable Assembly

Interfacing EIA-Compatible Devices

The DLV11-F supports only the data leads of EIA-compatible devices. It uses a BC05C modem cable to interface devices such as the Teletype® Model 37 Teletypewriter and the Bell Data Set Model 103 (in auto mode). The DLV11-F's EIA "data leads only" interface circuit is shown in Figure 9 and the jumpers are shown in Figure 1.

---

* X = Length in feet. Standard length is 25 feet.

® Teletype is a registered trademark of Teletype Corporation.

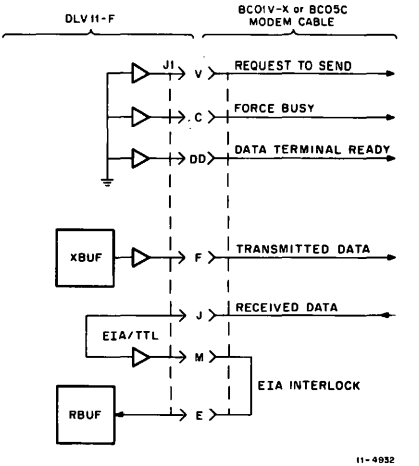


Figure 9 EIA Data Leads Only Interface

Interfacing 20 mA Current Loop Devices with the DLV11-F

When interfacing with 20 mA current loop devices, the BC05M cable assembly provides the correct connections to the 40-pin connector on the DLV11-F. The peripheral device end of the cable is terminated with

a Mate-N-Lok connector that is pin-compatible with all DIGITAL 20 mA serial interface terminals.

The interface circuits provided by the BC05M cable and the associated DLV11-F jumpers are shown in Figures 9, 10 and 11.

NOTE

When the DLV11-F is used with teletypewriter devices, a 0.005μF capacitor must be installed (see Figure 1).

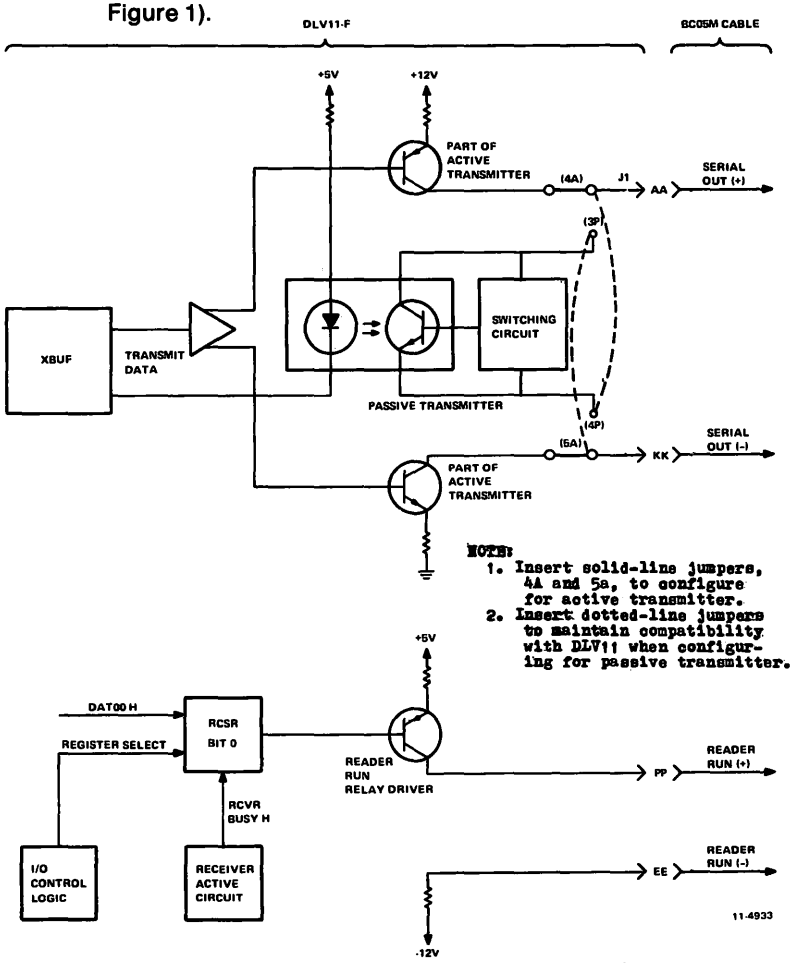


Figure 10 20 mA Transmitter and Reader Run Circuits

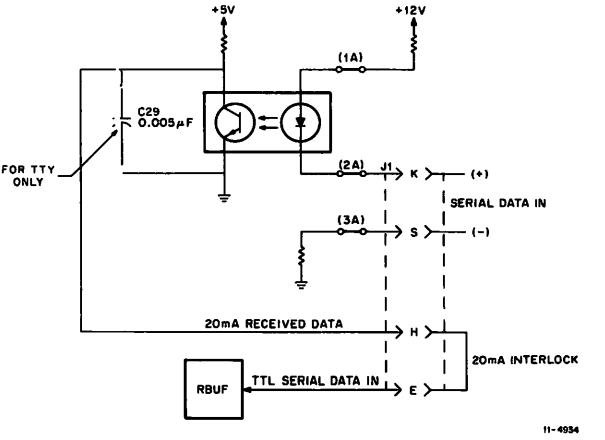


Figure 11 Active Receive 20 mA Current Loop

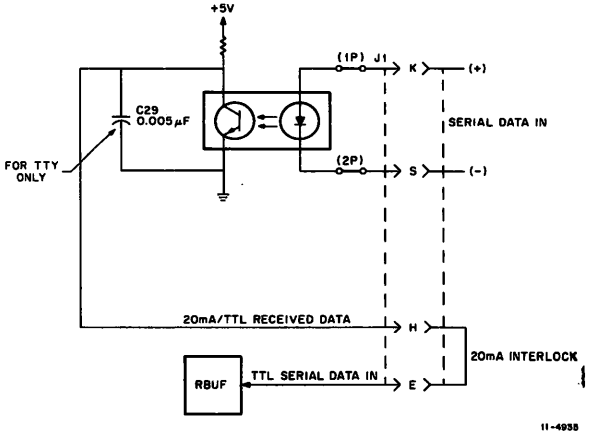


Figure 12 Passive Receive 20 mA Current Loop

DLV11-J FOUR ASYNCHRONOUS SERIAL INTERFACES

GENERAL

The DLV11-J is a 4-channel asynchronous serial line unit used to interface peripheral equipment to an LSI-11 bus. The interface transmits and receives data from the peripheral device over Electronics Industry Association (EIA) "data leads only" lines which do not use control lines. The module can be used with 20 mA current loop devices (with "reader-run" capabilities) when the DLV11-KA option is installed. With a DLV11-J interface, the processor can communicate with a local terminal such as a console teleprinter, a remote terminal via data sets and private line, or another local or remote processor.

FEATURES

- Four independent, full-duplex, asynchronous serial line interfaces to the LSI-11 bus on one double-height module.
- Each channel independently configured for:
  1. EIA RS-232C, RS-422, RS-423
  2. Baud Rates: 150, 300, 600, 1200, 2400, 4800, 9600, 19.2K, 38.4K and external
  3. Variable character format:
     7 or 8 data bits;
     1 or 2 stop bits;
     odd, even or no parity
  4. Support for data leads only: MODEMS (Bell type: 103, 113)
- One channel configurable as computer console device interface, including halt or boot on received break.
- 8.9 in. × 5.2 in. (22.8cm × 13.2cm) module
- 20 mA current loop and 110 baud capability optionally added using the EIA to 20 mA converter (DLV11-KA).
- The DLV11-KA provides: (Figure 1)
  1. Single line EIA to 20 mA converter unit and 3 ft. (.91m) cable for connection to DLV11-J.
  2. A program-controlled, reader advance function for DIGITAL-modified ASR33 teletypes.
  3. A 110 baud rate generator.
  4. Choice of active or passive operation.
  5. Operation up to 9600 baud.
  6. Cable drive capability up to 4000 feet.

DLV11-J

SPECIFICATIONS

Identification	M8043
Size	Double
Power	+5 V ±5% at 1.0 A +12 V ±3% at 0.25 A
Bus Loading	
AC	1
DC	1

DESCRIPTION

General

The DLV11-J module is designed to interface peripheral devices that transmit and receive asynchronous serial data over EIA-compatible data lines or 20 mA current loops to the parallel LSI-11 bus. When configured, the module transmits and receives the specified EIA signal levels on the receive and transmit data lines of the cable. Also, the module constantly asserts the data-terminal-ready signal.

When configured for 20 mA current loop operation (DLV11-KA option installed), the DLV11-J can support devices which contain program-controlled paper tape readers (such as DIGITAL's LT33 Teletypewriters or the ASR33 Teletypewriter with the LT33 modification kit.)

During operation, the module is required to convert data from parallel to serial and serial to parallel. To accomplish this, a universal asynchronous receiver/transmitter (UART) is employed. When performing this conversion, the UART must also alter the speed and character format for the data (to meet user-selected parameters). In addition, the UART creates error bits to allow the programmer to check data transmission for errors. A block diagram of the DLV11-J module is shown in Figure 1.

UART Operation

The DLV11-J module is equipped with four universal asynchronous receiver/transmitters, one for each channel. The UART chip is capable of parallel data transfers with the computer and serial data transfers with the peripheral device. User-selectable jumpers determine the character format used during transmission. The jumpers select:

7 or 8 data bits
1 or 2 stop bits
Parity or no parity
Even or odd parity

The receiver section performs serial-to-parallel conversion of data which will always appear right-justified in the receive data buffer. The start, stop, and parity bits are removed and error flags appended to the transmission as it enters the receive buffer. The error flags, when set, will not interrupt operation, but they are available to the programmer when reading the RBUF.

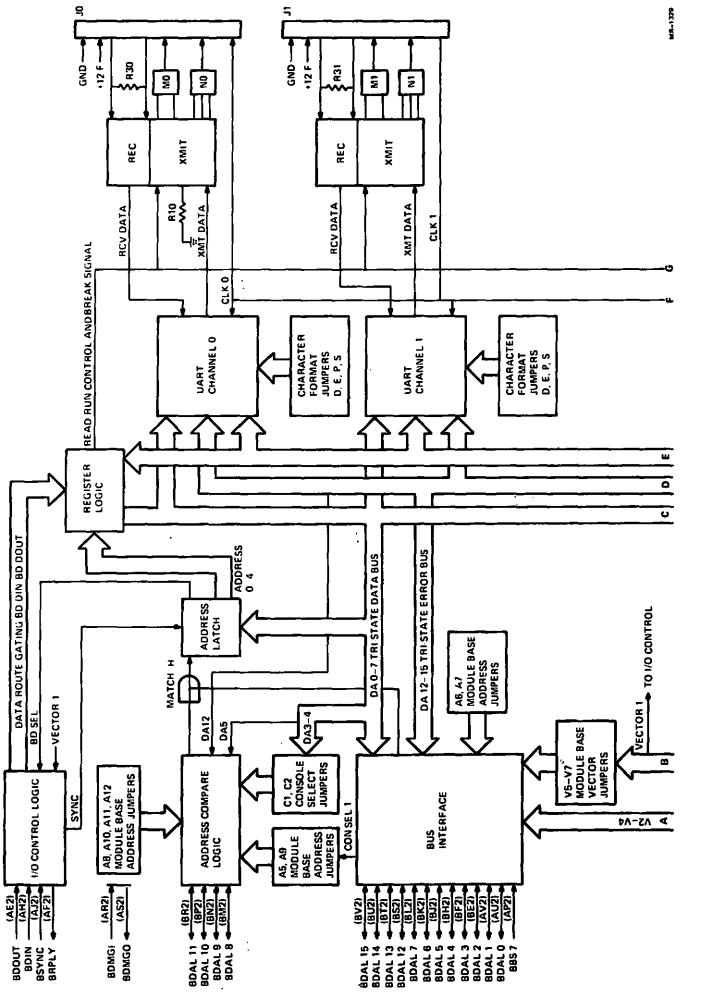


Figure 1 DLV11-J Block Diagram (Sheet 1 of 2)

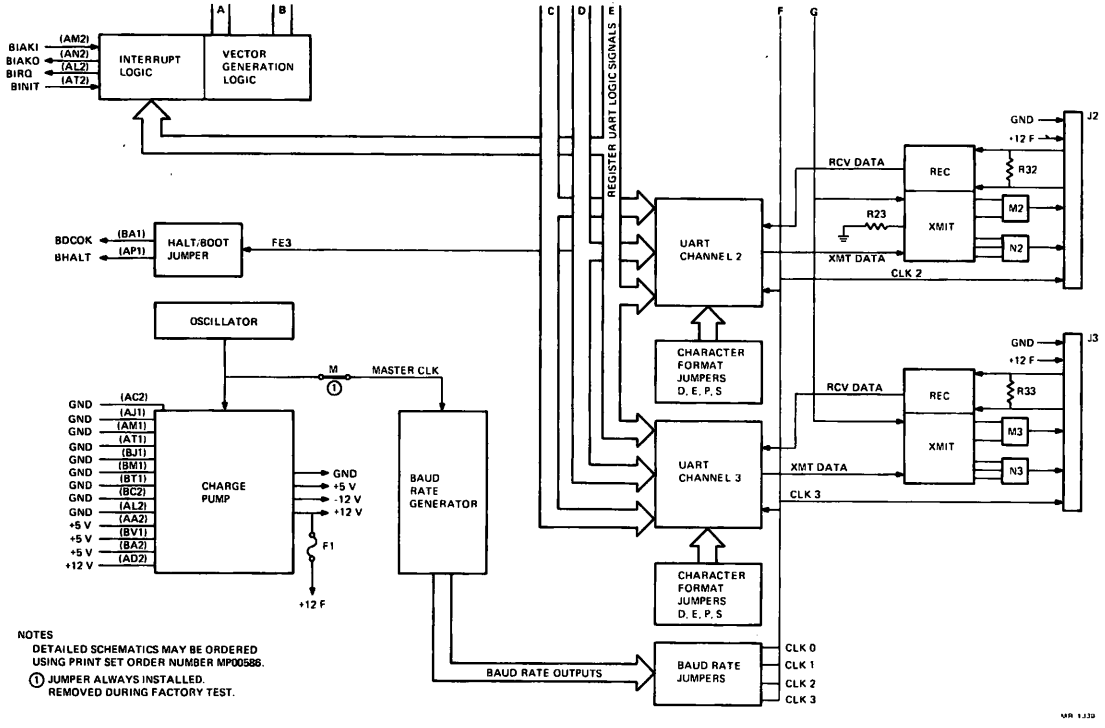


Figure 1 DLV11-J Block Diagram (Sheet 2 of 2)

The transmitter performs parallel to serial conversion of data provided by the LSI-11 bus. The character length, stop bit code, parity, and baud rate are identical to the receiver section of the SLU channel. The transmitter, however, appends the proper start, stop, and parity bits to the data before transmission.

Baud Rate Generator

The baud rate control circuit generates clock signals that control the speed at which the receive buffer (RBUF) and the transmit buffer (XBUF) move serial data. The circuit provides a command clock to both buffers of the channel.

The speed at which a channel will operate is configured by the selection of wire-wrap jumpers which supply the desired baud rate clock. The clock is developed by a crystal-controlled oscillator driving a frequency division chip. The outputs of the frequency division chip are connected to wire-wrap posts which may be selected when configuring the channel(s). If more than one channel is used for a particular baud rate, the clock may be daisy-chained between channels.

When 110 baud operation is desired, the DLV11-KA option must be used. This option provides the 110 clock to the channel via the peripheral device cable; no baud rate jumper may be configured on the module for the 110 baud channel.

I/O Control Logic

The I/O control logic directs data transfers between the computer and the DLV11-J module. The logic monitors the LSI-11 bus control lines to determine the type of data transfer to be executed (from the LSI-11 bus to the register logic for an output operation or from the register logic to the LSI-11 bus for an input operation). The following LSI-11 bus control lines are monitored by the I/O control logic during the operation:

BSYNC	Bus Synchronized. Set when valid address has been placed on LSI-11 bus.
BDIN	Bus Data Input. Set when processor is ready to receive input data.
BDOUT	Bus Data Output. Set when processor is ready to transmit output data.

The module asserts the BRPLY (reply from module) bus control line when the data transfer has been completed.

During operation, the module receives the BSYNC signal indicating an address has been placed onto the LSI-11 bus. The I/O control logic gates this address into the address latch of the module with a SYNC H gating signal. If the address received is a bus device address on the DLV11-J, the address latch sends a BD SEL signal to the I/O control logic (indicating a valid address has been received). The control logic may now develop the proper gating signals (BDOUT/BDIN) to move the data to its proper destination. When the data transfer is complete, the module signals the processor via the BRPLY control line.

Address Latch

The address latch is used to hold the channel address (0-3), the device register address (RCSR, RBUF, XCSR, or XBUF), and the high-low byte indicator of the pending operation. When the program addresses the DLV11-J module, address bits 0-4 are presented to the address latch by the bus interface circuit over the internal tri-state data bus. Simultaneously, the address compare circuit and the bus interface circuit supply the address latch with the MATCH H signal and are gated into the latch under the control of the I/O control logic circuit (SYNC H signal). The address latch now holds the address and a board select signal (BD SEL 1) to be used by the I/O control/register logic during the completion of the desired operation.

Address Compare Circuit

The address compare circuit tests the user-configured base address of the module (wire-wrap jumpers A5, A8-12) against the LSI-11 bus input (BDAL 5, 8-12 L). If the addresses are same, the address compare circuit generates a portion of the MATCH H signal. (The remainder of MATCH H is supplied by the bus interface.) The MATCH H signal is used by the address latch circuit when creating the BD SEL H signal required by the I/O control logic during data transfers.

When channel 3 is configured as a console device interface, the bus interface logic tests for a proper console device address on the LSI-11 bus. If the address received by the bus interface is a proper console address, the CON SEL 1 H signal is generated. This signal is transmitted from the bus interface to the address compare circuit to force console address recognition.

Bus Interface

The module contains bus drivers and receivers which interface directly with the LSI-11 bus. This allows data movement between the LSI-11 bus and the module's internal tri-state bus. These drivers also have

the ability to transmit vector addresses received from the interrupt vector generation logic onto the LSI-11 bus.

If the LSI-11 bus holds an address within the I/O page, the BBS7 L signal line is asserted. This will cause the bus interface circuit of the DLV11-J to test the BDAL 6-7 L lines against the user-configured wire-wrap pins (A6-7) when the addresses and the same MATCH H signal are allowed to be asserted to the address latch. Since this is a "wired-AND," the MATCH H signal from the address compare signal must also be asserted. The MATCH H signal is required by the address latch to allow I/O data transfers. If channel 3 has been selected as a console device interface (jumpers C1 and C2 installed between wire-wrap posts X and 1), the bus interface performs a match operation between the LSI-11 bus lines (BDAL 3-5) and an internal address which is enabled by console select jumper C1. If the addresses agree, a CON SEL 1 H signal is produced for the address compare circuit which will force a console address recognition.

Interrupt and Vector Generation Logic

When a peripheral device interfaced to a DLV11-J needs service, the module can, if enabled, interrupt the computer program and vector to a service routine. The interrupt logic can initiate two types of interrupts: a receiver interrupt and a transmitter interrupt. These interrupts are handled through separate receiver and transmitter channels.

For an interrupt transaction to occur, the program must set the interrupt enable bit (bit 6) in the control/status register (CSR). Next, the interrupt logic must recognize a condition requiring service (indicated by the setting of bit 7 within the CSR) and then assert the interrupt request line (BIRQ L) on the LSI-11 bus. When the interrupt is acknowledged by the processor, the interrupt logic creates an input to the module's vector generation circuit which reflects the channel needing service (0, 1, 2, or 3) and the type of service needed (receive or transmit). The vector generation logic creates a vector function address which may be modified by the user-configured "base vector" address jumpers (V5-7). This modified address is output to the LSI-11 bus by the bus interface circuit, thus causing the processor to jump to the proper peripheral device service routine.

A receiver interrupt request is initiated when the receive buffer (RBUF) has received and assembled a character of data and is ready to transfer it to the processor. A transmitter interrupt is initiated when the transmitter buffer holding register (XBUF) is empty and is ready for another data input from the processor. The interrupt logic is also used

to initialize the DLV11-J module. On a system power-up sequence, the processor creates BINIT L on the LSI-11 bus which is converted by the interrupt logic into INITO H. This signal is distributed on the module to initialize the four UARTs and the interrupt status registers (held within the interrupt logic).

Control/Status Registers

The control/status registers (CSRs) consist of a series of latches, data selectors, and gating circuitry. During data transactions, the I/O control logic enables the XCSR or RCSR to either latch in control bits or gate out status bits.

The RCSR uses only three bits during operation:

Receiver done (bit 7), set by RBUF
Receiver interrupt enable (bit 6), set by program
Reader enable (bit 0), set by program

All bits except the reader enable bit may be read by the program.

The XCSR uses three bits during operation:

Transmitter ready (bit 7), set by XBUF
Transmitter interrupt enable (bit 6), set by program
Break (bit 0), set by program and used only with the DLV11-KA option.

All bits may be read by the program.

Break Logic

During normal operation, the UART checks each received character for the proper number of stop bits. It does this by testing for a marking condition at the appropriate bit time. If it finds a spacing condition instead, it sets the framing error (FE) flag. The BREAK signal is a continuous spacing condition, and is interpreted by the UART as a data character that is missing its stop bit(s). The UART, therefore, responds to the BREAK signal by asserting FE H. If the channel 3 break response jumper is installed from X to B, FE H will negate control line BDCOK H; BDCOK H indicates to the processor that dc power is "OK." When FE H negates this signal, it causes the computer to restart at the bootstrap (provided proper processor power-up mode is selected).

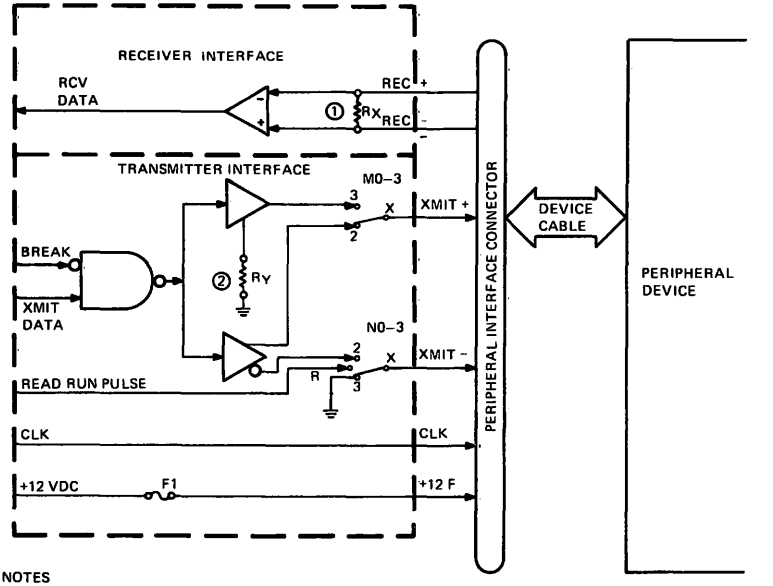
If the break jumper is installed from X to H, the computer will not "boot" on a framing error, but FE H will negate control line BHALT L. This causes the computer to halt when a framing error is received.

CAUTION

If the system is using MOS memory, data may be lost when BDCOK is negated because this action interrupts the memory refresh cycle. If the jumper is not installed, the module will not take action.

Peripheral Interface

Each SLU channel of the DLV11-J module can be independently configured for line signal compatibility with EIA RS-232C and RS-423, RS-422, or 20 mA current loop operation (Figure 2). Each of the four interfaces may be configured to support 20 mA current loop devices with the addition of the DLV11-KA option. When installed, the peripheral interface supplies all power supply voltages needed by this option. If the 20 mA device contains a paper tape reader that can be program-controlled (such as DIGITAL's LT33 or an ASR33 Teletypewriter with LT33 modification kit), the interface can be configured to advance the reader one character at a time.



NOTES

① RX IS INSTALLED WHEN CHANNEL IS CONFIGURED FOR EIA RS-422 OPERATION (100 Ω, 1/4 W NON-WIRE WOUND)
R30 - CHANNEL 0
R31 - CHANNEL 1
R32 - CHANNEL 2
R33 - CHANNEL 3

② RY IS CHOSEN FOR PROPER SLEW RATE WHEN CHANNEL IS CONFIGURED FOR EIA RS-232C/RS-423 OPERATION
R10 SETS SLEW RATE FOR CHANNELS 0 AND 1
R23 SETS SLEW RATE FOR CHANNELS 2 AND 3

MR 1297

Figure 2 Typical Peripheral Interface

DC-to-DC Power Converter

The power converter produces −12 Vdc and +5 Vdc from the LSI-11 power supply voltage of +12 Vdc. These voltages are produced to power all chips on the DLV11-J module and to supply the DLV11-KA 20 mA option. The power converter circuit consists of crystal-controlled oscillator which drives a charge pump. The charge pump during operation supplies the desired power supply output voltage.

CONFIGURATION

General

The DLV11-J device and vector addressing, serial word formats, baud rates, interface, type, etc. are selected by installing and/or removing jumpers. Wire-wrap posts are provided on the module for this purpose. The module is factory-configured and ready to use in most user applications. However, if a system requires different device register addresses and interrupt vectors or operations, the module may be reconfigured. The DLV11-J module is factory-configured for the following operations:

- Base address = 176500
- Base vector address = 300
- Channel 3 enabled as the console device (device addresses 177560-177566 and vector addresses 60 and 64).
- Channel 3 halt on break enabled
- Baud rates (transmit and receive are identical):
  Channels 0,1 and 2 = 9.6K baud
  Channel 3 = 300 baud
- Data/parity/stop bit format (all channels):
  Eight data bits
  One stop bit
  No parity
- Serial line signal interface levels (all channels) compatible with both EIA RS-232C and RS-423, simultaneously (slew rate = 2 μs)

Figure 3 gives jumper and pad locations on the DLV11-J module and Table 1 gives a summary of the module's factory configuration.

DLV11-J

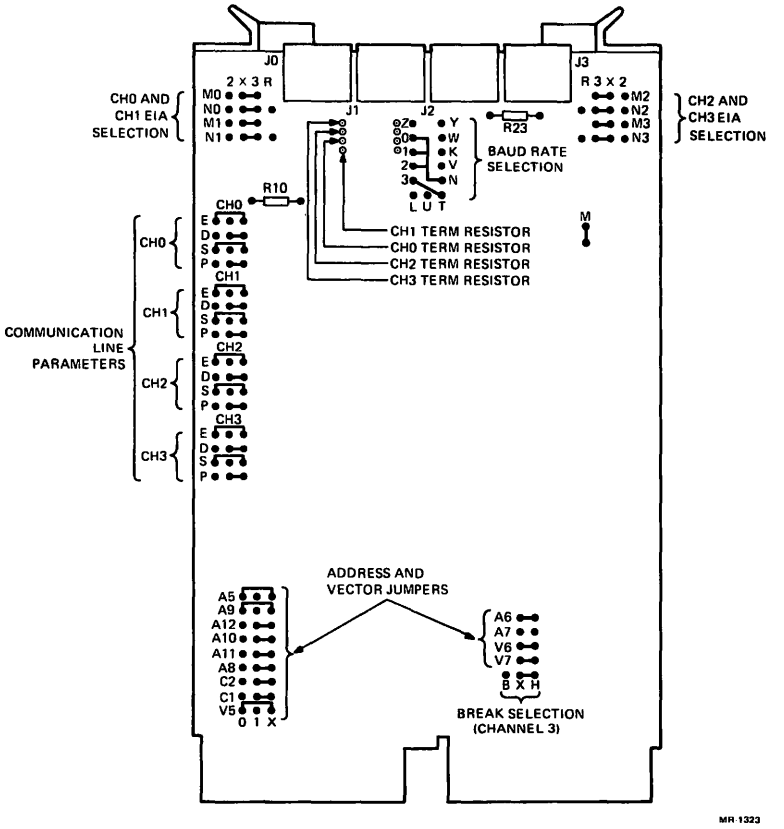


Figure 3 DLV11-J Jumper Locations

Table 1 Factory Jumper Configuration

Label	Standard Configuration	Function Implemented
A12 A11 A10 A9 A8 A7 A6 A5	X to 1 X to 1 X to 1 X to 0 X to 1 R I X to 0	This arrangement of jumpers A5-A12 implements the octal base device address 1765XX, which is the assigned address for channel 0 RCSR. The least significant digit is decoded on the module during operation to address one of four SLU device registers as follows: X = 0, RCSR X = 2, RBUF X = 4, XCSR X = 6, XBUF
C1 C2	X to 1 X to 1	These jumpers are used to enable channel 3 for console operation. Base address must be 176500 (factory-configured), 176540, or 177500 for the console.
(Break response)	X to H	This jumper determines channel 3 break response. The board is configured for halt (console emulator mode) on break condition.
V7 V6 V5	I I X to 0*	This arrangement of jumpers V5-V7 implements the octal "base" vector of 300 with channel 3 at 60 and 64.
E D S P	X to 0 X to 1 X to 0 X to 1	Odd parity 8 data bits 1 stop bit Parity inhibited These jumpers determine the word format used by the channel. All channels are configured the same at the factory.

Table 1 Factory Jumper Configuration (Cont)

Label	Standard Configuration	Function Implemented
0	0 to N	9.6K baud
1	1 to N	9.6K baud
2	2 to N	9.6K baud
3	3 to T	300 baud These jumpers determine the baud rate of the serial line channel for same baud rate daisy-chain wire-wraps.
NO-3 MO-3	X to 3 X to 3	These jumpers determine the EIA standard compatibility of the channel. All channels are set at the factory to be compatible to both EIA RS-423 and RS-232C simultaneously.
R10	22KΩ	Channels 0 and 1, slew rate of 2 μs (used when configured for EIA RS-423/RS-232C)
R23	22KΩ	Channels 2 and 3, slew rate of 2 μs (used when configured for EIA RS-423/RS232C)

* See Interrupt Vector Format figure.

Device Registers— The DLV11-J contains 16 device registers that can be individually addressed by the program. The four device registers provided for each of the SLU channels (0 through 3) are:

Receive Control/Status Registers (RCSR)
Receive Buffer (RBUF)
Transmit Control/Status Register (XCSR)
Transmit Buffer (XBUF)

Wire-wrap jumpers are configured to establish the base address (BA) for the module. This base address is the channel 0 RCSR address. The device address format is shown in Figure 4. The remaining device addresses follow through 16 (total) contiguous word addresses; however, it is possible to independently dedicate the last four addresses (channel 3) to a console device. When configured for console device operation, the channel's device register addresses will be 177560-

177566. For console operation, the board's base address must be one of the following:

176500 (factory-configured)
176540
177500

The floating address configurations are listed in Table 2 and the factory or standard configuration addresses are listed in Table 3.

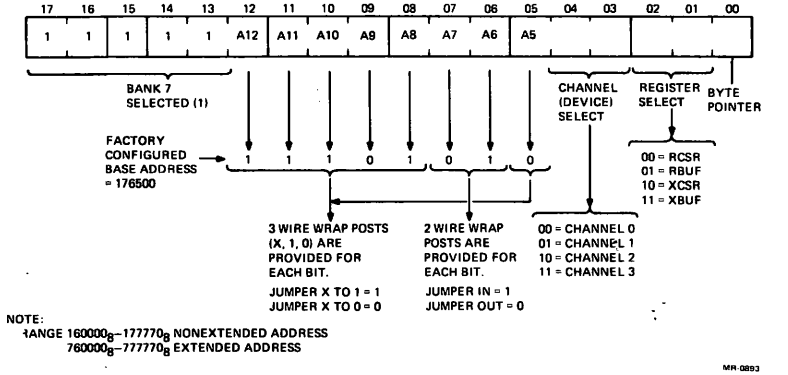


Figure 4 Channel 0 RCSR Address Format

Table 2 Address Assignments (with Console Selected)

Address	Device Register	Associated Vector
	Channel 0	
Module Base Address (BA)	RCSR	Module Base Vector (BV)
BA+2	RBUF	
BA+4	XCSR	BV+4
BA+6	XBUF	
	Channel 1	
BA+10	RCSR	BV+10
BA+12	RBUF	
BA+14	XCSR	BV+14
BA+16	XBUF	

Table 2 Address Assignments (with Console Selected) (Cont)

Address	Device Register	Associated Vector	
		Channel 2	
BA+20	RCSR	BV+20	
BA+22	RBUF		
BA+24	XCSR	BV+24	
BA+26	XBUF		
		Channel 3*	
177560	RCSR		
177562	RBUF	60	Console
177564	XCSR		Selected
177566	XBUF	64	

* Channel 3 is used as a console device.

Table 3 Factory or Standard Addresses

Address	Register	Vector	
176500	RCSR		
176502	RBUF	300	
176504	XCSR		Channel 0
176506	XBUF	304	
176510	RCSR		
176512	RBUF	310	
176514	XCSR		Channel 1
176516	XBUF	314	
176520	RCSR		
176522	RBUF	320	
176524	XCSR		Channel 2
176526	XBUF	324	
177560	RCSR		
177562	RBUF	60	
177564	XCSR		Channel 3
177566	XBUF	64	

Four word formats, one for each device register within a channel, are shown in Figure 5 and described in Table 4. These word formats are typical of all channels on the DLV11-J module.

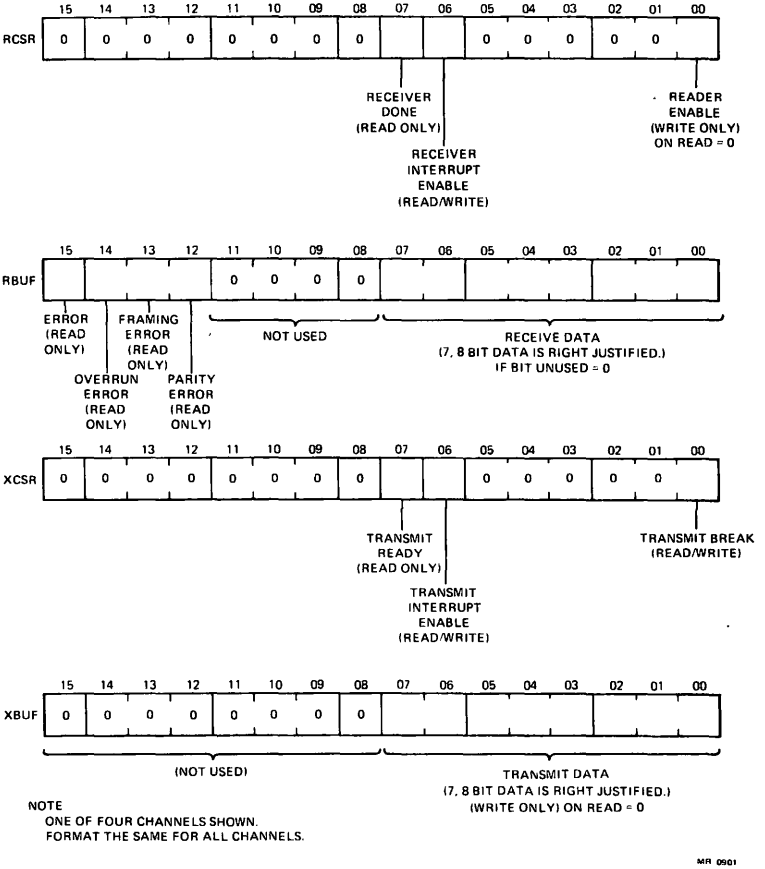


Figure 5 DLV11-J Device Register Formats

Table 4 DLV11-J Word Formats

Receiver Control/Status Register

Bit: 8-15
Description: Not used. Read as 0.

Bit: 7
Description: Receiver Done. Set when an entire character has been received and is ready for input to the processor. This bit is automatically cleared when RBUF is read, when BINIT L signal goes true (low), or when reader enable bit is set. Read-only bit.

If Receiver Interrupt (bit 6) is set, the setting of Receiver Done starts an interrupt sequence.

Bit: 6
Description: Receive Interrupt Enable. Set under program control when it is desired to generate a receiver interrupt request (when a character is ready for input to the processor signified by bit 7 being set). Cleared under program control or by the BINIT signal. Read/write bit.

Bit: 1-5
Description: Not used. Read as 0.

Bit: 0
Description: Reader Enable. Setting this bit advances the paper tape reader on an LT33 terminal one character at a time. Setting of this bit clears Receiver Done (bit 7). Write-only bit.

The DLV11-KA 20 mA current loop option is required for operation of this bit.

Receiver Buffer

Bit: 15
Description: Channel Error Status. Logical OR of bits 14, 13, and 12. Read-only bit.

Bit: 14
Description: Overrun Error. When set, indicates that the reading of the previously received character was not completed (receiver done not cleared) prior to receiving a new character.

Cleared by BINIT signal. Read-only bit.

NOTE

When "back-to-back" characters are received, one full character time is allowed from the time instant receiver done (bit 7) is set to the occurrence of an overrun error.

Bit: 13
Description: Framing Error. When set, indicates that the character read had no valid stop bit.

Cleared by BINIT signal. Read-only bit.

Bit: 12
Description: Parity Error. When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no-parity operation is configured for the channel. Read-only bit.

NOTE

Error bits remain valid until the next character is received, at which time the error bits are updated.

Bit: 8-11
Description: Not used. Read as 0.

Bit: 0-7
Description: Data bits. Contains seven or eight data bits in a right-justified format. Bit 7 = 0 when 7 data bits are enabled. Read-only bits.

Transmitter Control/Status Register

Bit: 8-15
Description: Not used. Read as 0.

Bit: 7
Description: Transmit Ready. Set when XBUF is empty and can accept another character for transmission. It is also set by INIT during the power-up sequence or during a reset instruction. Read-only bit.

If Transmitter Interrupt Enable (bit 6) is set, the setting of Transmit Ready will start an interrupt sequence.

Bit: 6
Description: Transmit Interrupt Enable. Set under program control when it is desired to generate a transmitter interrupt request (when transmitter is ready to accept a character for transmission).

The bit is cleared under program control, during power-up sequence, or reset instruction. Read/write bit.

Bit: 1-5
Description: Not used. Read as 0.

Bit: 0
Description: Transmit Break. Set or reset under program control. When set, a continuous space level is transmitted. However, transmit done and transmit interrupt can still operate, allowing software timing of break. When not set, normal character transmission can occur.

Cleared by BINIT. Read/write bit.

Transmit Buffer

Bit: 8-15
Description: Not used. Read as 0.

Bit: 0-7
Description: Data bits. Contains seven or eight right-justified data bits. Loaded under program control for serial transmission.

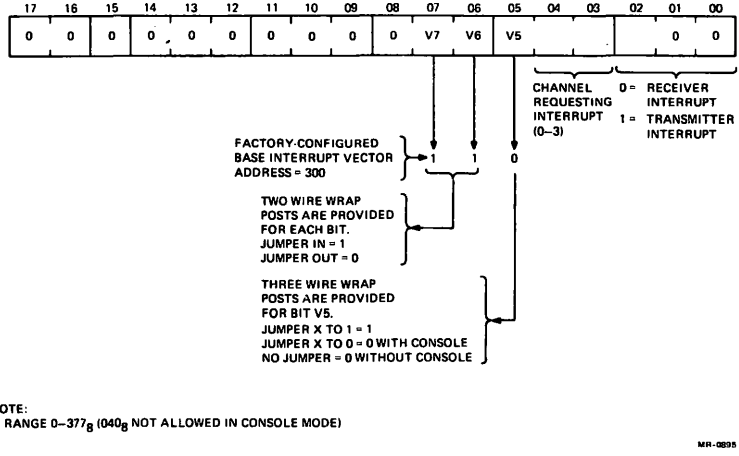
Interrupt Vectors

Two interrupt vectors are provided for each of the four SLU channels (eight vectors total). The procedure for configuring the vectors is similar to that used when configuring the base device register address; the configured base vector is the channel 0 receiver interrupt vector. Each interrupt vector references two word locations in memory (the Program Counter address and the Processor Status Word). Hence, sequential vectors appear in increments of four.

The module is factory-configured with an interrupt vector base of 300. However, it is also configured for channel 3 operation as the console device; thus, channel 3 will automatically have interrupt vectors of 60 and 64. The vector format is shown in Figure 6 and a summary of vector jumper configurations is provided in Table 5. Table 6 gives a list of the factory-configured vector assignments.

Interrupt priority within the DLV11-J module is structured as follows:

Interrupt Priority	Requesting Function
1 (highest)	Channel 0, receiver
2	Channel 1, receiver
3	Channel 2, receiver
4	Channel 3, receiver
5	Channel 0, transmitter
6	Channel 1, transmitter
7	Channel 2, transmitter
8 (lowest)	Channel 3, transmitter



NOTE:
RANGE $0–377_8$ (040_8 NOT ALLOWED IN CONSOLE MODE)

MR-0895

Figure 6 Interrupt Vector Format

Table 5 Summary of Vector Jumper Configurations

Label	Logical 1	Logical 0
V7	Jumper installed.	Jumper removed.
V6	Jumper installed.	Jumper removed.
V5	Jumper installed from wire-wrap post X to 1.	Console not selected: jumper removed Console selected: jumper installed from wire-wrap post X to 0.

Table 6 Vector Assignments (with Console Selected) (Factory Configured)

Standard Address	Interrupt Vector
300 [Module Base Vector (BV)]	Channel 0, Receiver
304 (BV+4)	Channel 0, Transmitter
310 (BV+10)	Channel 1, Receiver
314 (BV+14)	Channel 1, Transmitter
320 (BV+20)	Channel 2, Receiver
324 (BV+24)	Channel 2, Transmitter
60	Channel 3, Receiver
64 Console Selected	Channel 3, Transmitter

NOTES

1. Module is factory-configured for channel 3 as a console device.
2. All addresses are in octal notation.

Character Formats

Each of the four channels may be independently configured for various character formats. When a character format is configured (by wire-wrap jumpers) for a channel, both the transmitter and receiver will use the same format. The character may contain:

7 or 8 data bits
1 or 2 stop bits
Parity or no parity
Even or odd parity

Configuration instructions for determining the character formats of each channel are shown in Table 7.

Baud Rates

Each channel can be configured for baud rates ranging from 150 to 38,400 bits per second. One baud rate clock input wire-wrap pin is provided for each channel (0 through 3). Both the transmitter and receiver for a given channel must operate at the same baud rate; split baud rate operation cannot be configured. Configure baud rates by connecting a jumper from the appropriate baud rate generator output wire-wrap pin to the clock input pin of the channel. One jumper is

required for each channel. When configuring the same baud rate for more than one channel, the wire-wrap pins may be daisy-chained. Table 8 lists the possible baud rates for each channel and their associated labels.

Table 7 Character Format Jumpers

Label	Channel Parameter	Wire-wrap X to 0	Connection X to 1	Comments
D	No. of data bits	7 bits	8 bits	LSB transmitted first
S	No. of stop bits	1 bit	2 bits	
P	Parity inhibit	Parity generation and detection enabled	Parity bit deleted; parity error = 0	
E*	Even parity enabled	Odd parity expected	Even parity expected	Only when P = 0

* Jumper must be installed to 0 or 1 even if no parity is selected.

Table 8 Baud Rate Generator Outputs

Wire-Wrap Pin Label	Baud Rate (Bits/Second)
U	150
T	300
V	600
W	1,200
Y	2,400
L	4,800
N	9,600
K	19,200
Z	38,400

When using the DLV11-KA option, 110 bits/sec operation is possible. A 110 baud rate clock generator circuit on the option will supply the DLV11-J module with the proper clock; no baud rate jumper is configured on the module for the desired channel.

Console Device Selection

Channel 3 of the DLV11-J module may be independently dedicated for console device operation. To accomplish this, the console select jumpers must be properly configured. Table 9 gives channel 3 configuration instructions. When configured for console operation, the device addresses are 177560-177566 and the interrupt vectors are 60 and 64.

Table 9 Summary of Console Selection Jumper Configurations

Label	Console Selected	Console Not Selected
C1	Install jumper from wire-wrap pins X to 1.	Install jumper from wire-wrap pins X to 0.
C2	Install jumper from wire-wrap pins X to 1.	Install jumper from wire-wrap pins X to 0.

Break Response

Channel 3 may be configured to either bootstrap, halt (console emulator mode), or have no response to a receive break condition. A bootstrap operation upon a receive break condition will cause the processor to execute the bootstrap program starting at the memory location defined by the power-up mode jumpers of the processor. A halt operation upon a receive break condition will cause the processor to halt and the console octal debugging technique (ODT) microcode to be invoked. Configuration instructions are given in Table 10.

Table 10 Channel 3 Break Operation Jumper Summary

Break Operation Response	Jumper Connection
Boot*	Install jumper between wire-wraps X to B.
Halt	Install jumper between wire-wrap pins X to H.
No Response	No jumper installed.

* Do not send continual breaks to a system so configured, as it will cause continued reinitializing of any device on the bus.

Peripheral Interface Configuration

Each of the channels can be independently configured for serial line signal compatibility with EIA RS-423 (simultaneously RS-232C), RS-422, or 20 mA current loop devices. When using 20 mA current loop devices, the DLV11-KA option is required. Configuration instructions for each of the standards are listed in Table 11. Table 12 is used when configuring EIA RS-423 (RS-232C compatible) slew rates. Use this table in conjunction with Table 11.

Table 11 Summary of Serial Channel Signal Level Configurations

Serial Channel Signal Level Modifiers	EIA RS-422	EIA RS-232C and RS-423	20 mA Current Loop (Using DLV11-KA)
M0-3 Jumper	Connect wire-wrap pins X and 2.	Connect wire-wrap pins X and 3.	Connect wire-wrap pins X and 3.
N0-3 Jumper	Connect wire-wrap pins X and 2	Connect wire-wrap pins X and 3.	Connect wire-wrap pins X and R for program-controlled paper tape reader.
Termination Resistor (one per channel)	Install a 100Ω, 1/4 W, non-wire wound, fusible resistor.		
Wave-Shaping Resistor (one per channel pair; channel pair 0 and 1; 2 and 3)		Install resistor from Table 12 (1/4 W non-wire wound).	
Fuse F1			Install 2.0 A Pico fuse

Table 12 EIA RS-423 and RS-232C Slew Rate Resistor Values

Baud Rate	R10 or R23
38.4 K	22 KΩ
19.2 K	51 KΩ
9.6 K	120 KΩ
4.8 K	200 KΩ
2.4 K	430 KΩ
1.2 K	820 KΩ
600	1 MΩ
300	1 MΩ
150	1 MΩ
110	1 MΩ

Cabling

Following are listed cables currently available that will mate with the 2X5 pin Amp connector on the DLV11-J, as well as some pointers and part numbers for constructing a cable.

DIGITAL cables for the DLV11-J:

BC20N-05	5' EIA RS-232C null modem cable to directly interface with an EIA RS-232C terminal (2X5 pin Amp female to RS-232C female; see Figure 8).
BC21B-05	5' EIA RS-232C modem cable to interface with modems and acoustic couplers (2X5 pin Amp female to RS-232C male; see Figure 7).
BC20M-50	50' EIA RS-422 or RS-423 cable for high-speed transmission (19.2K baud) between two DLV11-Js (2X5 pin Amp female to 2X5 pin Amp female).
DLV11-KA	20 mA current loop converter option for the DLV11-J. Comes with an EIA cable (BC21A-03) which connects the DLV11-KB converter box to the DLV11-J. The option mates with standard DIGITAL 20 mA cabling using the 8-pin Mate-'N'-Lock connector.

DLV11-J

When designing a cable for the DLV11-J, here are several points to consider:

1. The receivers on the DLV11-J have differential inputs. Therefore, when designing an RS-232C or RS-423 cable, RECEIVE DATA (pin 7 on the 2X5 pin Amp connector) must be tied to signal ground (pins 2, 5, or 9) in order to maintain proper EIA levels. RS-422 is balanced and uses both RECEIVE DATA+ and RECEIVE DATA —.
2. To directly connect to a local EIA RS-232C terminal, it is necessary to use a null modem. To design the null modem into the cable, one must switch RECEIVE DATA (pin 2) with TRANSMITTED DATA (pin 3) on the RS-232C male connector as shown in Figure 8.
3. To mate to the 2X5 pin connector block, the following parts are needed:

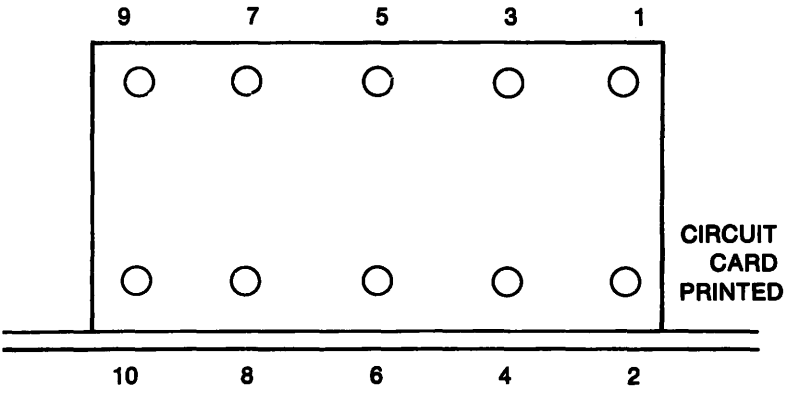
Cable Receptacle	AMP PN 87133-5 DEC PN 12-14268-02
Locking Clip Contacts	AMP PN 87124-1 DEC PN 12-14267-00
Key Pin (pin 6)	AMP PN 87179-1 DEC PN 12-15418-00

4. The pin out on the 2X5 pin connector block on the DLV11-J is as follows:

Pin #	Signal
1	UART clock in or out (16 X baud rate; CMOS)
2	Signal ground
3	TRANSMIT DATA+
4	TRANSMIT DATA−

Note: For EIA RS-423, this line is grounded. For DLV11-KA 20 mA option, this line is the reader enable pulse.

5	Signal ground
6	Indexing key—no pin
7	RECEIVE DATA−
8	RECEIVE DATA+
9	Signal ground
10	When F1 is installed for the DLV11-KA, +12V is supplied through a fuse to this pin



2X5 PIN CONNECTOR BLOCK (Viewed from Edge of Card)

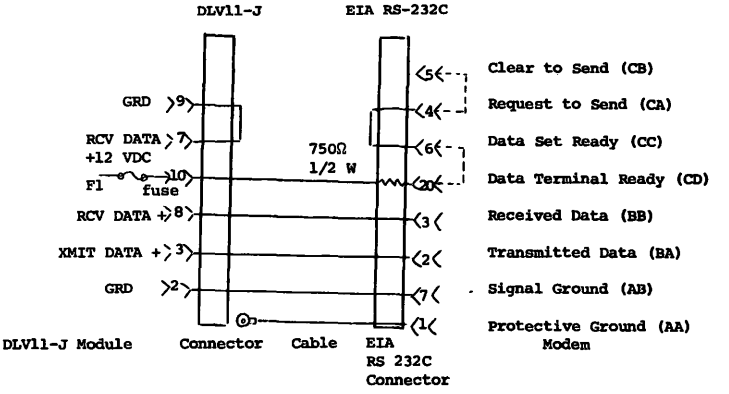


Figure 7 BC21B-05 Modem Cable

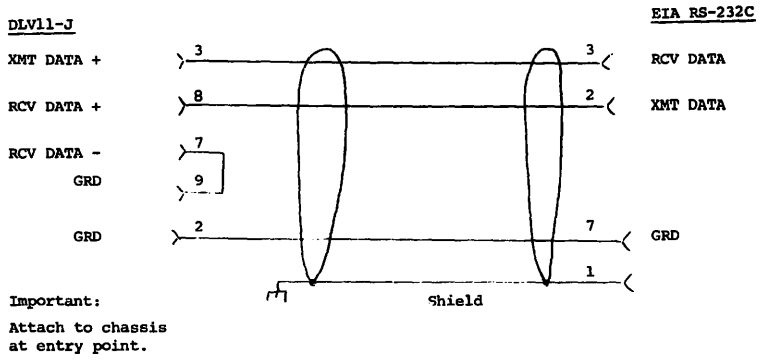


Figure 8 BC20N-05 "Null Modem" Cable

PROGRAMMING

The DLV11-J contains a bank of sixteen (16) contiguous registers that may be positioned from 160000_8 to 177777_8 in address space by wire wrap jumpers. Four registers are provided for each of the four SLU channels.

The format of these registers is shown in Figure 1.

Similarly, the DLV11-J has a bank of eight contiguous interrupt vectors that may be positioned in vector space from 000_8 to 377_8 by jumpers. Two vectors (receive and transmit) are provided for each of the four channels.

NOTE

One channel may be separately configured as the computer console device ($177560\text{-}6_8$, vectors 60 and 64) provided the module base address is 176500_8, 176540_8 or 177500_8.

To software, the DLV11-J appears to be four independent serial line units similar to four single-channel DLV11s.

DLV11-KA

DLV11-KA EIA TO 20 MA CONVERTER

GENERAL

The DLV11-KA option consists of the DLV11-KB EIA-to-20 mA converter unit and a BC21A-03 EIA interface cable. This option is designed to allow 20 mA current loop capability to be added to a standard RS-232 EIA serial line unit interface module, such as the DLV11-J. The DLV11-KB is a small enclosed box with two connectors, one (2 × 5 pin Berg) for the EIA/TTL signals from the interface module and the other (standard DIGITAL 20 mA connector 8-pin Mate-N-Lok) for the 20 mA signals to 20 mA peripherals using standard DIGITAL 20 mA cabling.

FEATURES

- EIA RS-232 to 20 mA converter (XMT data)
- 20 mA to EIA RS-232 converter (RCVR data)
- A program-controlled, one character at a time reader advance function for DIGITAL-modified ASR-33 Teletypes
- A 110 baud rate generator
- Optical isolation
- Choice of active or passive operation
- Operates up to 9600 baud rate
- Drive capability up to 4000 feet of cable

* Teletype is a registered trademark of Teletype Corporation.

SPECIFICATIONS

Size: 13.3cm (5.25 in.) long
11.4cm (4.5 in.) wide
2.64cm (1.04 in.) high

Power: +12.0 Vdc ±5% at 0.275 A max

20 mA Transmitter

Switch is passive and optically isolated and goes to "mark" state when power is turned off (passive mode).

	Minimum	Typical	Maximum
Open circuit voltage (of circuit being driven)	8.0V	-	40V
Voltage drop marking	0.5V	-	2.0V

Spacing current	0.4 mA	-	1.8 mA
Marking current	20 mA	-	80 mA
Rise and fall time	2 μs	6 μs	10 μs
Waveform distortion	0 μs	7 μs	15 μs
Constant current sink (active mode)	20 mA	24 mA	28 mA

When the transmitter is active, the maximum cable loop resistance plus receiver equivalent resistance (at 20 mA) is 600 ohms.

20 mA Receiver

Receiver is passive and optically isolated.

	Minimum	Typical	Maximum
Voltage drop marking	0.4V	1.35V	2.4V
Spacing current	0.0 mA	-	6 mA
Marking current	16 mA	-	80 mA
Waveform distortion	0 μs	7 μs	15 μs
Constant current load (active mode)	20 mA	24 mA	28 mA

When the receiver is active, the maximum cable loop resistance plus transmitter equivalent resistance (at 20 mA) is 600 ohms.

Temperature

Storage temperature range:	−40° C to 66° C (−40° F to 151° F) Before operating a module which is at a temperature beyond the operating range, that module must first be brought to an environment within the operating range and then allowed to stabilize for a reasonable length of time (five or more minutes, depending on air circulation).
Operating temperature range:	5° C to 60° C (41° F to 140° F) Derate the maximum operating temperaure by 0.5° C (1° F) for each 1000 feet of altitude above 8000 feet.

Relative Humidity:	10% to 95%, noncondensing
Altitude:	Up to 50,000 feet (90 mm mercury)
Environment:	Air must be noncaustic

DESCRIPTION

The DLV11-KA contains the following functional circuits (Figure 1): EIA-to-20 mA converter, 20 mA-to-EIA converter, reader run, 110 baud rate generator, current sources and current sinks, a +5 Vdc generator and a −12 Vdc charge pump. These circuits are selected by the user to operate in a desired configuration.

EIA-to-20 mA

The circuit accepts a standard EIA RS-232 signal to an EIA receiver and then provides optical isolation before it activates a passive 20 mA switch. When the EIA input is in the "mark" condition (less than −3V), the switch is on. When the EIA input is in the "space" condition (greater than +3V), the switch is off. The user can select passive or active operation by using jumpers as described in the Configuration section. The current source is provided by a 180 ohm resistor connected to the +12 Vdc and the current sink is provided by a 24 mA current-limited load to −12 Vdc.

20 mA-to-EIA

The circuit receives a 20 mA signal in a passive 20 mA detector. The signal is optically isolated and then generates a standard EIA RS-232 output. With the 20 mA current signal flowing into the 20 mA detector, the EIA output is in the "mark" state (less than −3V). With the 20 mA current off, the EIA output is in the "space" state (greater than +3 V). The current source is provided by a 180 ohm resistor connected to the +12 Vdc and the current sink is provided by a 24 mA current-limited load to −12 Vdc. When using this circuit with an ASR-33 Teletype, the user should install the noise suppression capacitor.

Reader Run

The reader run circuit receives a TTL pulse to set a flip-flop. This flip-flop enables the relay drive circuit that drives the reader run relay in a DIGITAL-modified ASR-33 Teletype. The Teletype reader will advance to the next character and initiate its transmission down the line. A delay circuit is used to reset the flip-flop in the middle of the start bit and therefore disable the reader run circuits. When the first character has been received, the flip-flop may again be set to advance to the next character for its transmission. When used with the DLV11-J inter-

face module, the circuit allows only one character to be transmitted by the Teletype each time a 1 is written into the reader enable bit of the RCS register.

NOTE

For proper operation of Teletype ASR-33 with DIGITAL-supplied paper tape software, the SLU should be configured for eight data bits, two stop bits, and no parity. The Teletype models can be LT33-DC, LT33-DD, LT33-DE, or an ASR-33 Teletype with the LT33-MB modification kit installed.

110 Baud Rate Generator

A 614.4 kHz crystal oscillator frequency is divided by 352 (by 11 and 32) to produce a 110 baud UART clock at 1760 Hz (16 × 110). This signal is sent back to the SLU module through the BC21A-03 cable.

+5 Vdc Generator

The +5 Vdc voltage is generated by a zener diode that drops the +12 Vdc power to +5 Vdc and is for internal use only.

−12 Vdc Charge Pump

The −12 Vdc charge pump uses the output of the 614.4 kHz crystal-controlled clock that is amplified and then rectified to produce the −12 Vdc reference voltage.

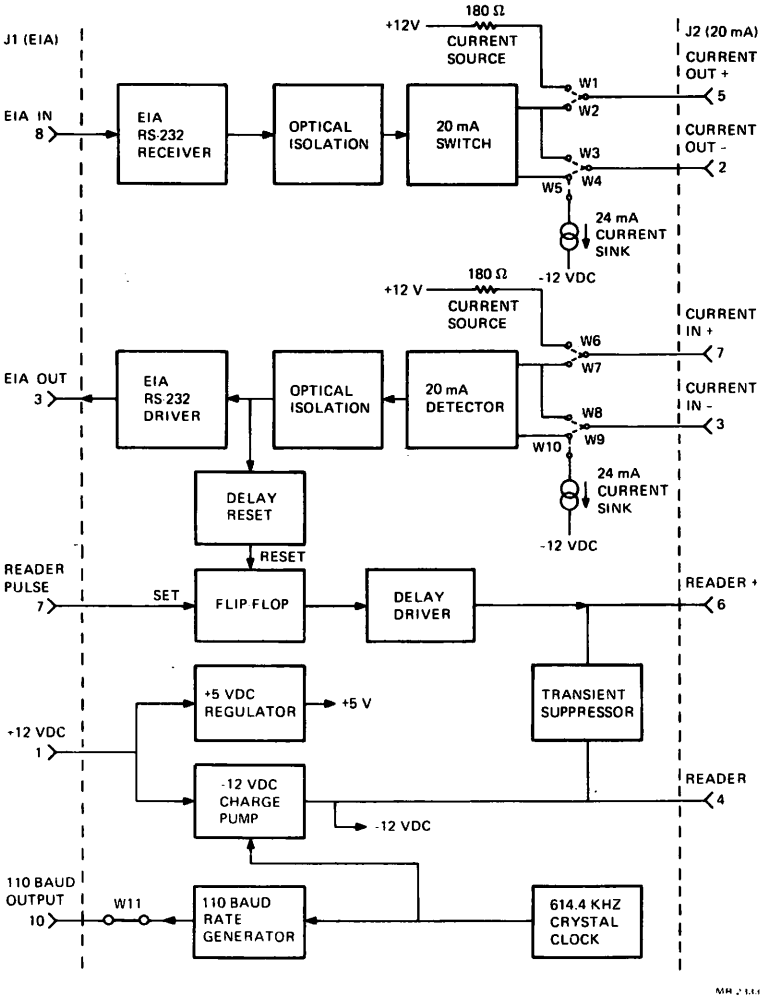


Figure 1 DLV11-KA Functional Block Diagram

DLV11-KA

CONFIGURATION

The DLV11-KA requires the configuration of eleven jumper wire connections and one capacitor connection. The locations of these jumpers are shown in Figure 2 and their functions are listed in Table 1.

Current Loop Definition

In simplest terms, the current in a circuit loop which extends from the sender to the receiver is switched on and off to represent some particular format for serial transmission of binary data. Besides the actual current path (wire), the following other three functions are required in every current loop:

1. Current source 2. Switch 3. Current detector

The switch has to be located in the transmitter, and the current detector has to be located in the receiver. However, the current source may be located in either the sender or receiver. The function that includes the current source is designated active and the one without it passive. Only one passive and one active function are allowed in a current loop: never two active or two passive functions (Figure 3). In order to minimize ground differential noise coupling into data leads, the transmitter and receiver at one end of the line should be either both active or both passive, not mixed. Also, it is usually better to configure the computer (master computer) as active and the terminal (slave computer) as passive.

110 Baud Rate Generator

This circuit provides a 16 × 110 (1760 Hz), TTL level, crystal-controlled clock to be sent back to the serial line unit module in order to add 110 baud rate capability to the module. A solderable jumper (W11) is provided in order to select or deselect this function.

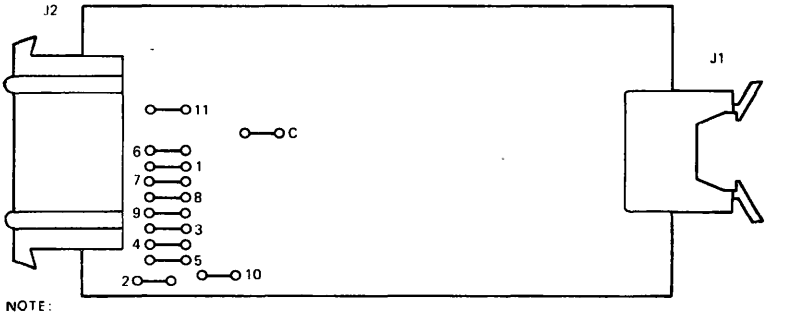


Figure 2 DLV11-KA Jumper Locations

Table 1 DLV11-KA Jumper Configurations

Function	Jumper In	Jumper Out
Passive 20 mA Receiver	W7, W9	W6, W8, W10
Active 20 mA Receiver*	W6, W8, W10	W7, W9
Passive 20 mA Transmitter	W2, W4	W1, W3, W5
Active 20 mA Transmitter*	W1, W3, W5	W2, W4
110 Baud Enabled*	W11	-
110 Baud Disabled	-	W11
Noise Suppression	-	-

* Factory configuration.

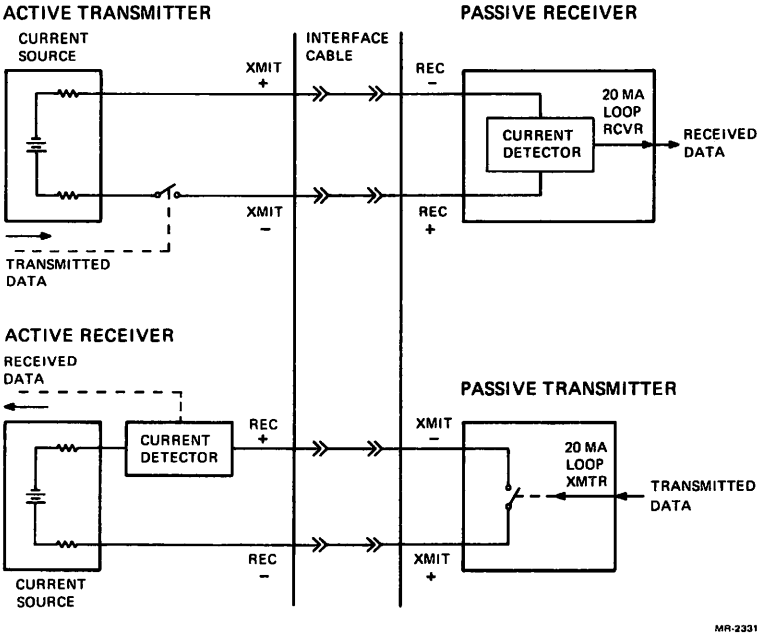


Figure 3 Standard Current Loop Interface

Noise Suppression Capacitor

The DLV11-KA can be used with a DIGITAL-modified ASR-33 Teletype and requires the user to install a 0.047 μF capacitor for noise suppression. This capacitor is installed across the position designated "C" as shown in Figure 2.

Installation

The DLV11-KA option can be installed in a system that requires conversion from EIA RS-232 standard to a 20 mA current loop. The DLV11-KA option consists of a DLV11-KB converter box and a BC21A-03 interface cable as shown in Figure 4. The BC21A-03 is a 0.9 m (3 ft.) cable that interconnects the DLV11-KB to a EIA SLU interface module. The smaller connector (2 × 5 pin) connects to the SLU module and the larger connector (2 × 7 pin) connects to the DLV11-KB box. Keying is provided on both connectors, and cable retention is provided by locking pins on the SLU connector. To disengage, pull back on the connector shell and the connector will slide free. However, if the cable is pulled, the locking pins will hold the connector firmly in place. A BC05F-XX cable can be used to connect the DLV11-KB converter box to DIGITAL 20 mA terminals including the DIGITAL-modified ASR-33 Teletype. External mounting dimensions for the DLV11-KB box are shown in Figure 5.

Cabling

Cables other than the DIGITAL BC05F-XX can be used when installing the DLV11-KA option. However, any other cable must conform to the following parameters in order to meet the baud rate versus cable length specification described in Table 2.

1. Resistance—not more than 30 ohms/1000 ft. (not less than 22 AWG)
2. Capacitance to ground—not more than 50 pF/ft.
3. Capacitance wire-to-wire—not more than 35 pF/ft.

The BC05F-XX cable meets the above requirements. If the user desires to use shielded cable, the shield should be grounded to the chassis at entry point and not to the DLV11-KB converter box. The user can fabricate custom cables for the 20 mA interface by using DIGITAL connectors and pins.

Baud Rate

The DLV11-KA option will operate up to a maximum of 9600 baud, provided that the interface module can accommodate these rates.

However, the maximum operational baud rate is also limited by the length of cable. Table 2 provides maximum recommended cable lengths for the specific baud rates. These recommendations are conservative and will yield satisfactory operation for almost all applications. Exceeding these guidelines should be done only after reviewing the DLV11-KA specifications, the severity of the operating environment, and the error rate that can be tolerated.

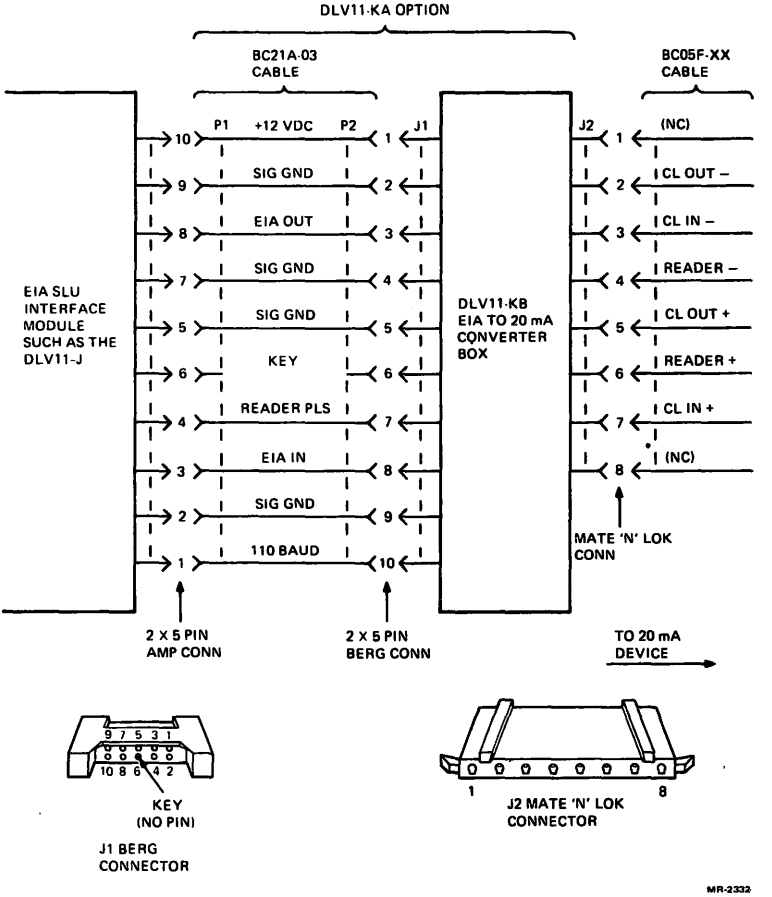


Figure 4 DLV11-KA Typical Installation

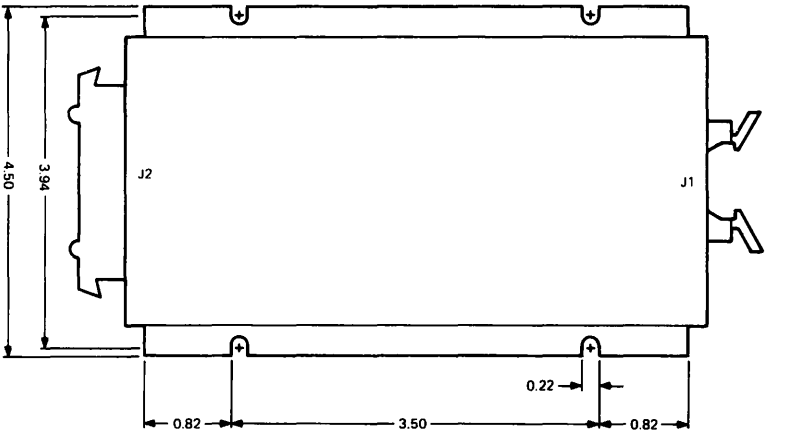


Figure 5 DLV11-KA Mounting Dimensions

Table 2 Baud Rate vs. Cable Length

Baud Rate	Max Cable Length
9600	30 m (100 ft.)
4800	76 m (250 ft.)
2400	152 m (500 ft.)
1200	305 m (1000 ft.)
600	610 m (2000 ft.)
300	1220 m (4000 ft.)
110	1220 m (4000 ft.)

DRV11 PARALLEL LINE UNIT

GENERAL

The DRV11 is a general-purpose interface unit used for connecting parallel line TTL or DTL devices to the LSI-11 bus over up to 7.6 m (25 ft) of cable. It permits program-controlled data transfers at rates up to 40K words per second and provides LSI-11 bus interface and control logic for interrupt processing and vector generation. Data is handled by 16 diode-clamped input lines and 16 latched output lines. The device address is user-assigned and control/status registers (CSR) and data registers are compatible with PDP-11 software routines.

FEATURES

- 16 diode-clamped data input lines
- 16 latched output lines
- 16-bit word or 8-bit byte programmed data transfers
- User-assigned device address decoding
- LSI-11 bus interface and control logic for interrupt processing and vector generation
- Interrupt priority determined by electrical position along the LSI-11 bus
- Control/status registers (CSR) and data registers that are compatible with PDP-11 software routines
- Four control lines to the peripheral device for NEW DATA RDY, DATA TRANS, REQ A, and REQ B
- Logic-compatible with TTL and DTL devices
- Program-controlled data transfer rate of 40K words per second (maximum)

SPECIFICATIONS

Identification	M7941
Size	Double
Power	5.0 Vdc ±5% at 0.9 A
Bus Loads	
AC	1.4
DC	1.0

DESCRIPTION

General

Major functions contained on the DRV11 module are shown in Figure 1. Communications between the processor and the DRV11 are execut-

ed via programmed I/O operations or interrupt-driven routines.

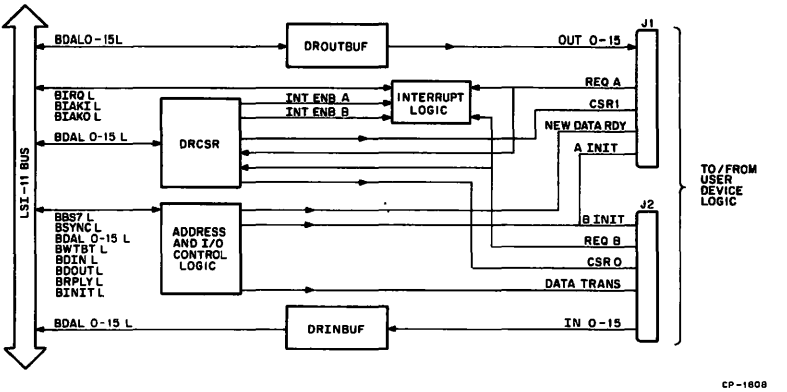


Figure 1 DRV11 Parallel Line Unit

The DRV11 is capable of storing one 16-bit output word or two 8-bit output bytes in DROUTBUF. The stored data (OUT0-15 H) is routed to the user's device via an optional I/O cable connected to J1. Any programmed operation that loads a byte or a word in DROUTBUF causes a NEW DATA RDY H signal to be generated, informing the user's device of the operation.

Input data (DRINBUF) is gated onto the BDAL bus during a DATI bus cycle. All 16 bits are placed on the bus simultaneously; however, when the processor is involved in an 8-bit byte operation, it uses only the high or low byte. When the data is taken by the processor, a DATA TRANS H pulse is sent to the user's device to inform the device of the transfer.

Addressing

When addressing a peripheral device interface such as the DRV11, the processor places an address on BDAL0-15 L, which is received and distributed as BRD0-15 H in the DRV11. The address is in the upper 4K (28-32K) address space. On the leading edge of BSYNC L, the address decoder decodes the address selected by jumpers A3-A12 and sets the device selected flip-flop (not shown); the active flip-flop output is the ME signal, which enables function selection and I/O control logic operation. At the same time, function selection logic stores address bits BRD0-2.

NOTE

When addressed, the DRV11 always responds to either BDIN L or BDOUT L by asserting BRPLY L (L = assertion).

Function Selection

Function selection and I/O control logic monitors the ME signal and bus signals BDIN L, BDOUT L, and BWTBT L. It responds by generating appropriate select signals which control internal data gating. NEW DATA RDY H or DATA TRANS H output signals for the user's device, and the BRPLY L bus signal which informs the processor that the DRV11 has responded to the programmed I/O operation. Since the DRV11 appears to the processor as three addressable registers (DRCSR, DROUTBUF, and DRINBUF) that can be involved in either word or byte transfers, the three low-order address bits stored during the addressing portion of the bus cycle are used for function selection. The select signals relative to I/O bus control signals and address bits 0-2 are listed in Table 1.

Function selection is performed by a ROM located at E15 on the DRV11. The inputs to this ROM consist of the address bits and other LSI-11 bus signals as shown at the top of Table 1. This table shows the functions performed by the ROM outputs for a specific input condition. For example, when the output buffer is addressed by the processor, the last octal digit is decoded by the ROM to provide the SEL2IN L and the RPLY L signals. The RPLY L signal is delayed and becomes the BRPLY L signal. The SEL2IN L signal is used by the DRV11 logic to enable the contents of the output buffer register to be placed on the data lines of the LSI-11 bus so that the processor can read the data.

NEW DATA READY H is active for the duration of BDOUT L when in a DROUTBUF write operation. This signal is normally active for 350 ns. However, by adding an optional capacitor in the BRPLY L portion of the circuit, the leading edge of BRPLY is delayed, effectively increasing the duration of the NEW DATA RDY H pulse; adding the capacitor also increases the DATA TRANS H pulse width by approximately the same amount.

DATA TRANS H is active for the duration of BDIN L when in a DRINBUF read operation. This signal is normally active for 1150 ns. The time, however, can be extended by adding the optional capacitor to the BRPLY L portion of the circuit as previously described.

Table 1 DRV11 Device Function Decoding

Programmed Operation	Stored Device Addr. Bits 0-2	BWTBT L During Data Transfer	BDIN L	BDOUT L	Bus Cycle Type	Select Signals
	0	0	H	L	DATO	
Write DRCSR	0	1	H	L	DATOB	SEL0OUT I
Read DRCSR	0	0	L	H	DATI or DATIO	SEL0IN L
Write DROUTBUF Word	2	0	H	L	DATO	SEL2OUT (W + HB) L, SEL2OUT (W + LB) L, and NEW DATA READY H
Low Byte	2	1	H	L	DATOB	SEL2OUT (W + LB) L and NEW DATA READY H
High Byte	3	1	H	L	DATOB	SEL2OUT (W + HB) L and NEW DATA READY H
Read DROUTBUF	2	0	L	H	DATI or DATIO	SEL2IN L
Read DRINBUF	4	0	L	H	DATI	SEL4IN L and DATA TRANS H

Read Data Multiplexer

The read data multiplexer selects the proper data and places them on the BDAL bus when the processor inputs DRCSR, DROUTBUF or interrupt vectors; DRINBUF contents are gated onto the bus separately. The select signals (previously described) and VECTOR H, produced by the interrupt logic, control read data selection.

DRCSR Functions

The control/status register (DRCSR) has separate functions. Four of the six significant DRCSR bits can be involved in either write or read operations. The remaining two bits, 7 and 15, are read-only bits that are controlled by the external device via the REQ A H and REQ B H signals, respectively. The four read/write bits are stored in the 4-bit CSR latch. They represent CSR0 and CSR1 (DRCSR bits 0 and 1, respectively), which can be used to simulate interrupt requests when used with an optional maintenance cable. INT ENB A and INT ENB B (bits 6 and 5, respectively) enable interrupt logic operation. Note that CSR0 and CSR1 are available to the user's device for any user application.

DRINBUF Input Data Transfer

DRINBUF is an addressable 16-bit read-only register that receives data from the user's device for transmission to the LSI-11 bus. Data to be read are provided by the user's device on the IN0-15 H signal lines. Since the input buffer consists of gating logic rather than a flip-slop register, the user's device must hold the data on the lines until the data input transaction has been completed.

The input data are read during a DATI sequence while bus drivers are enabled by the SEL4IN L signal. The DATA TRANS pulse that is sent to the user's device by the function select logic informs the device of the transaction. Input data can be removed on the trailing edge of this pulse.

DROUTBUF Output Data Transfer

DROUTBUF comprises two 8-bit latches, enabling either 16-bit word or 8-bit byte output transfers. Two SEL2 signals function as clock signals for the latches. When in a DATO bus cycle, both signals clock data from the internal BRD0-15 H bus into the latches. However, when in a DATOB cycle, only one signal clocks data into an 8-bit latch, as determined by address bit 0 previously stored during the addressing portion of the bus cycle.

The NEW DATA RDY H pulse generated by the function select logic is sent to the user's device to inform the device of the data transaction. The data can be input to the device on the trailing edge of this pulse.

Interrupts

The DRV11 contains LSI-11 bus-compatible interrupt logic that allows the user's device to generate interrupt requests. Two independent interrupt request signals (REQ A H and REQ B H) are capable of requesting processor service via separate interrupt vectors. In addition, DRCSR contains two interrupt enable bits (INT EN A and INT EN B, bits 6 and 5, respectively), which independently enable or disable interrupt requests. REQ A and REQ B status can be read by the processor in DRCSR bits 7 and 15, respectively. Since separate interrupt vectors are provided for each request, one of the requests could be used to imply that device data is ready for input and the remaining request could be used to imply that the device is ready to accept new data.

An interrupt sequence is generated when a DRCSR INT EN bit (A or B) is set and its respective REQ signal is asserted by the device. The processor responds (if its PS bit 7 is not set) by asserting BDIN L; this enables the device requesting the interrupt to place its vector on the BDAL bus when the interrupt request is acknowledged. The processor then asserts BIAKO L, acknowledging the interrupt request. The DRV11 receives BIAKI L and the interrupt logic generates VECTOR H, which gates the jumper-addressed vector information through the read data multiplexer and bus drivers and onto the LSI-11 bus. The processor then proceeds to service the interrupt request.

Maintenance Mode

The maintenance mode allows the user to check DRV11 operation by installing an optional BC08R cable between connectors J1 and J2. This maintenance cable allows the contents of the output buffer DROUTBUF to be read during a DRINBUF DATI bus cycle. In addition, interrupts can be simulated by using DRCSR bits CSR0 and CSR1. CSR1 is routed via the cable directly to rhe REQ B H input and CSR0 is routed to the REQ A H input. By setting or clearing INT EN A, INT EN B, and CSR0 and CSR1 bits in the DRCSR register, a maintenance program can test the interrupt facility.

Initialization

BINIT L is received by a bus driver, inverted, and distributed to DRV11 logic to initialize the device interface. The buffered initialize signal is

available to the user's device via the AINIT H and BINIT H signal lines. DRV11 logic functions cleared by the BINIT signal include DROUTBUF, DRCSR (bits 0, 1, 5, and 6), and interrupt logic.

CONFIGURATION

The following paragraphs describe how the user can configure the module by inserting or removing jumpers (Figure 2) so that it will function within his system. The jumpers, listed in Table 2, indicate the factory configuration when shipped.

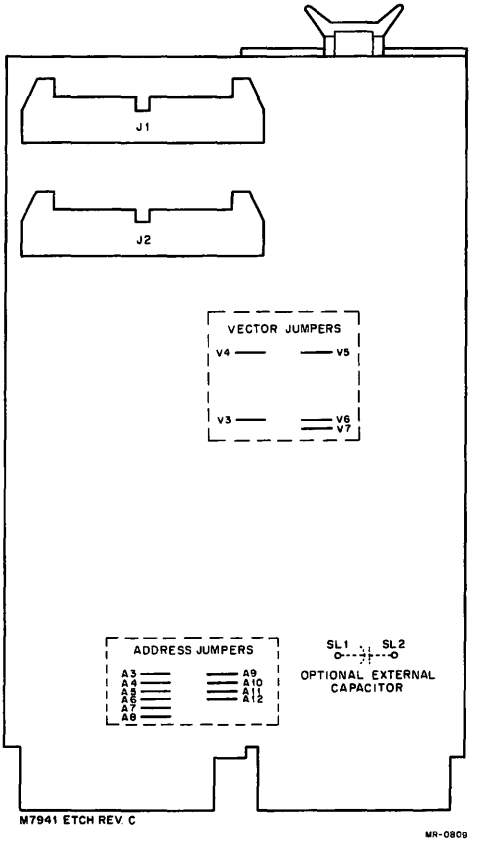


Figure 2 DRV11 Jumper Locations

Table 2 DRV11 PLU Factory Jumper Configuration

Jumper Designation	Jumper State	Function Implemented
A3	R	This arrangement of jumpers A3 through A12 assigns the device address 16777X to the PLU. This address is the starting address of a reserved block in memory bank 7 which is recommeded for user device address assignments. The least significant digit X is hardwired on the module to implement the three PLU device addresses as follows: X = 0 DRCSR address X = 2 Output buffer address X = 4 Input buffer address
A4	R	
A5	R	
A6	R	
A7	R	
A8	R	
A9	R	
A10	R	
A11	R	
A12	I	
V3	I	This factory-installed jumper configuration implements the two interrupt vector addresses 300 and 304 for use as defined by application requirements.
V4	I	
V5	I	
V6	R	
V7	R	

* R = Removed, I = Installed

Device Address

Addresses for the DRV11 can range from 16000X through 17777X. The three least significant bits are predetermined for the other DRV11 registers as shown in Table 3 and Figure 3. Addresses within 177560 to 177566 are reserved for the console device and should not be used for the DRV11.

Table 3 Standard Assignements

Description	Mnemonic	Read/ Write	First Module Address	Second Module Address
Register				
Control and Status	DRCSR	R/W	167770	167760
Output Buffer	DROUTBUF	R/W	167772	167762
Input Buffer	DRINBUF	R	167774	167764
Interrupt				
Request A	REQ A	—	300	310
Request B	REQ B	—	304	314

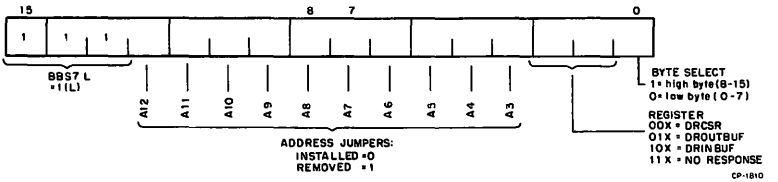


Figure 3 DRV11 Device Address Selection

Jumpers for bits 3 through 12 are installed or removed to produce the 16-bit address word shown in Figure 3. The appropriate jumpers are removed to produce logical 1 bits, and installed to produce logical 0 bits.

Vectors

The two vectors are selected within the range of 000 to 374 by using jumpers V3 to V7. Vector bits 3 through 7 are selected by the user to form the vector as described in Figure 4. The factory configuration sets the interrupt vector for 300 as shown in Table 3 and Figure 4.

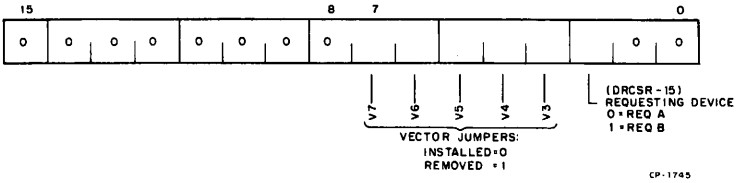


Figure 4 DRV11 Interrupt Vector

Registers

The word format for the control and status register (DRCSR) is shown in Figure 5 and described in Table 4.

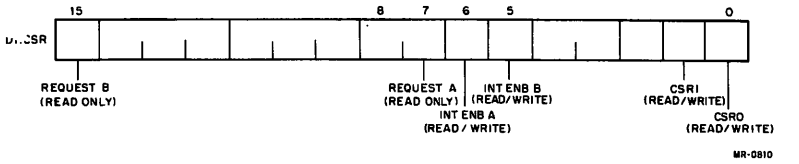


Figure 5 DRCSR Word Format

Table 4 DRCSR Word Formats

Bit: 15 **Name:** Request B.

Function: This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program.

When used as an interrupt request, it is asserted by the external device and initiates an interrupt provided the INT ENB B bit (bit 5) is also set. When used as a flag, this bit can be read by the program to monitor external device status.

When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 (bit 1). This permits checking interface operation by loading a 0 or 1 into CSR1 and then verifying that Request B is the same value.

Read-only bit. Cleared by INIT when in maintenance mode.

Bit: 14-8 **Name:** Not used.
Function: Read as 0.

Bit: 7 **Name:** Request A.
Function: Performs the same function as Request B (bit 15) except that an interrupt is generated only if INT ENB A (bit 6) is also set.

When the maintenance cable is used, the state of Request A is identical to that of CSR0 (bit 0).

Read-only bit. Cleared by INIT when in maintenance mode.

Bit: 6 **Name:** INT ENB A.
Function: Interrupt enable bit. When set, allows an interrupt request to be generated, provided Request A (bit 7) becomes set.

Bit: 5 **Name:** INT ENB B.
Function: Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided Request B (bit 15) becomes set.

Bit: 4-2 **Name:** Not used.
Function: Read as 0.

Bit: 1 **Name:** CSR1.
Function: This bit can be loaded or read (under program control) and can be used for a user-defined command to the device (appears only on connector number 1).

When the maintenance cable is used, setting or clearing this it causes an identical state in bit 15 (request B). This permits checking operation of bit 15 which cannot be loaded by the program.

Can be loaded or read by the program (read/write bit). Cleared by INIT.

Bit: 0 **Name:** CSR0.
Function: Performs the same functions as CSR1 (bit 1) but appears only on connector number 2.

When the maintenance cable is used, the state of this bit controls the state of bit 7 (Request A).

Read/write bit; cleared by INIT

The word format for the transmit output buffer (DROUTBUF) is shown in Figure 6 and defined in Table 5.

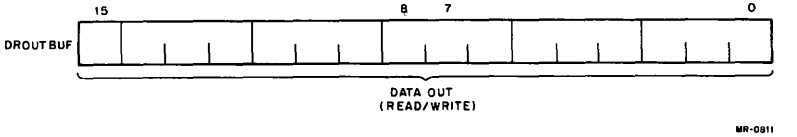


Figure 6 DROUTBUF Word Format

Table 5 DROUTBUF Word Format

Bit: 15-0 **Name:** Output Data Buffer.
Function: Contains a full 16-bit word or one or two 8-bit bytes; high byte = 15-8; low byte = 7-0.

Loading is accomplished under a program-controlled DATO or DATOB bus cycle. It can be read under a program-controlled DATI cycle.

The word format for the receiver input buffer (DRINBUF) is shown in Figure 7 and defined in Table 6.

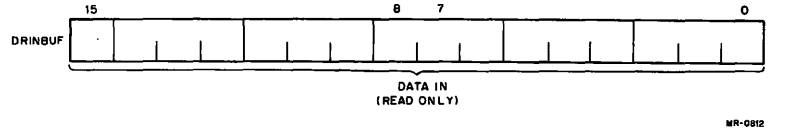


Figure 7 DRINBUF Word Format

Table 6 DRINBUF Word Format

Bit: 15-0 **Name:** Input Data Buffer.
Function: Contains a full 16-bit word or one or two 8-bits bytes. The entire 16-bit word is read under a program-controlled DATI bus cycle.

Installation

Prior to installing the DRV11 on the backplane, first establish the desired priority level for the backplane slot installaton. Check that proper device address vector jumpers are installed. The DRV11 can then be installed on the backplane. Connection to the user's device is via optional cables.

Interfacing to the User's Device

Interfacing the DRV11 to the user's device is via the two board-mounted H854 40-pin male connectors. Pins are located as shown in Figure 8. Signal pin assignments for input interface J2 (connector number 2) and output interface J1 (connector number 1) are listed in Table 7. Optional cables and connectors for use with the DRV11 include:

BC08R-01—Maintenance cable; 40-conductor flat with H856 connectors on each end.

*BC07D-X**—Signal cable; two 20-conductor ribbon cables with a single H856 connector on one end; remaining end is terminated by the user. Available in lengths of 3, 4.6, and 7.6 m (10, 15, and 25 ft).

* The -X in the cable number denotes length in feet, -10, -12, -20. For example, a 10-ft BC07D cable would be ordered as BC07D-10.

*BC04Z-X**—Flat 40-conductor signal cable with a single H856 connector on one end; remaining end is terminated by the user. Available in lengths of 3, 4.6, and 7.6 m (10, 15, and 25 ft).

*BCV11-X**—Flat, 40-conductor, twisted pair cable with a single H856 connector on one end. The remaining end is connected by the user. Available in lengths of 1.5, 3, 4.6, 6.1, and 7.6 m (5, 10, 15, 20, and 25 ft).

H856—Socket, 40-pin female, for user-fabricated cables.

When using the BC07D cable, connect the free end of the ribbon cables using the wiring data contained in Table 8.

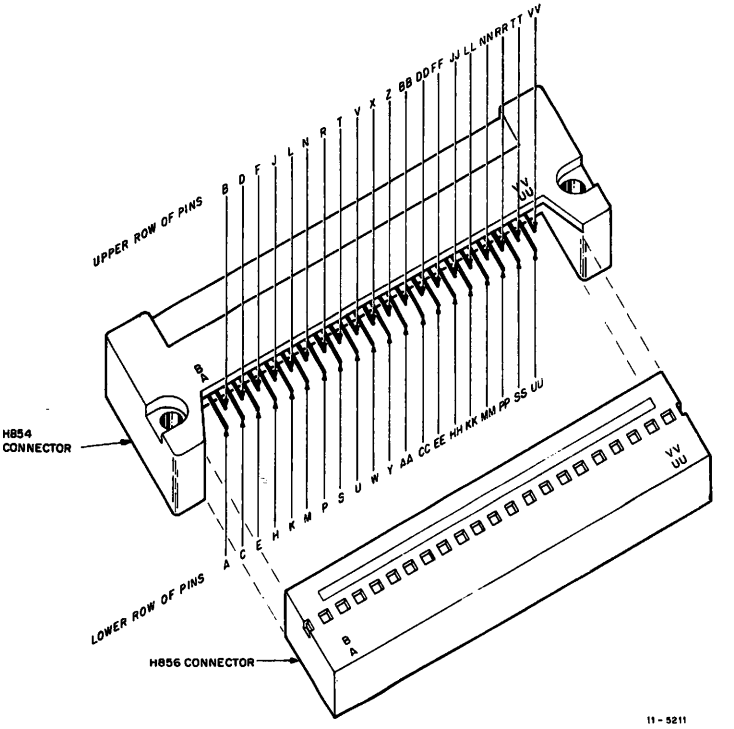


Figure 8 J1 or J2 Connector Pin Locations

* The -X in the cable number denotes length in feet, -10, -12, -20. For example, a 10-ft BC07D cable would be ordered as BC07D-10.

DRV11

Table 7 DRV11 Input and Output Signal Pins

Inputs			Outputs		
Signal	**Connector**	**Pin**	**Signal**	**Connector**	**Pin**
IN00	J2	TT	OUT00	J1	C
IN01	J2	LL	OUT01	J1	K
IN02	J2	H, E	OUT02	J1	NN
IN03	J2	BB	OUT03	J1	U
IN04	J2	KK	OUT04	J1	L
IN05	J2	HH	OUT05	J1	N
IN06	J2	EE	OUT06	J1	R
IN07	J2	CC	OUT07	J1	T
IN08	J2	Z	OUT08	J1	W
IN09	J2	Y	OUT09	J1	X
IN10	J2	W	OUT10	J1	Z
IN11	J2	V	OUT11	J1	AA
IN12	J2	U	OUT12	J1	BB
IN13	J2	P	OUT13	J1	FF
IN14	J2	N	OUT14	J1	HH
IN15	J2	M	OUT15	J1	JJ
REQ B	J2	S	REQ A	J1	LL
DATA TRANS	J2	C	NEW DATA RDY	J1	VV
CSR0	J2	K	CSR1	J1	DD
INIT	J2	RR, NN	INIT	J1	P

Table 8 BC07D Signal Cable Connections

Cable 1 (connector pins B-VV)				Cable 2 (connector pins A-UU)		
Wire Color	**Pins**	**J1 Signal**	**J2 Signal**	**Pins**	**J1 Signal**	**J2 Signal**
blk	B	open	open	A	open	open
brn	D	open	open	C	OUT00	DATA TRANS
red	F	open	open	E	open	IN02

Table 8 BC07D Signal Cable Connections (Cont)

Cable 1 (connector pins B-VV)				Cable 2 (connector pins A-UU)		
Wire Color	Pins	J1 Signal	J2 Signal	Pins	J1 Signal	J2 Signal
orn	J	GND	GND	H	open	IN02
yel	L	OUT04	GND	K	OUT01	CSR0
grn	N	OUT05	IN14	M	GND	IN15
blu	R	OUT06	GND	P	INIT	IN13
vio	T	OUT07	GND	S	GND	REQ B
gry	V	GND	IN11	U	OUT03	IN12
wht	X	OUT09	GND	W	OUT08	IN10
blk	Z	OUT10	IN08	Y	GND	IN09
brn	BB	OUT12	IN03	AA	OUT11	GND
red	DD	CSR1	GND	CC	GND	IN07
orn	FF	OUT13	open	EE	GND	IN06
yel	JJ	OUT15	GND	HH	OUT14	IN05
grn	LL	REQ A	IN01	KK	GND	IN04
blu	NN	OUT02	INIT	MM	GND	GND
vio	RR	OUT02	INIT	PP	GND	GND
gry	TT	open	IN00	SS	GND	GND
wht	VV	NEW DATA RDY	open	UU	GND	GND

Table 9 BC08R Maintenance Cable Signal Connection

J2		J1	
Pin	**Name**	**Pin**	**Name**
VV	OPEN	A	OPEN
UU	GND	B	OPEN
TT	IN00	C	OUT00
SS	GND	D	OPEN
RR	INIT H	E	OPEN
PP	GND	F	OPEN
NN	INIT	HH	OPEN
MM	GND	J	GND
LL	IN01	K	OUT01
KK	IN04	L	OUT04
JJ	GND	M	GND
HH	IN05	N	OUT05
FF	OPEN	P	INIT H
EE	IN06	R	OUT06
DD	GND	S	GND
CC	IN07	T	OUT07
BB	IN03	U	OUT03
AA	GND	V	GND
Z	IN08	W	OUT08
Y	IN09	X	OUT09
X	GND	Y	GND
W	IN10	Z	OUT10
V	IN11	AA	OUT11
U	IN12	BB	OUT12
T	GND	CC	GND
S	REQ B	DD	CSR1
R	GND	EE	GND
P	IN13	FF	OUT13
N	IN14	HH	OUT14
M	IN15	JJ	OUT15
L	GND	KK	GND
K	CSR0	LL	REQ A
J	GND	MM	GND

Table 9 BC08R Maintenance Cable Signal Connection (Cont)

J2		J1	
Pin	**Name**	**Pin**	**Name**
H	IN02	NN	OUT02
F	OPEN	PP	GND
E	IN02	RR	OUT02
D	OPEN	SS	GND
C	DATA TRANS	TT	OPEN
B	OPEN	UU	GND
A	OPEN	VV	NEW DATA RDY

Output Data Interface

The output interface is the 16-bit buffer (DROUTBUF). It can be either loaded or read under program control. When loaded by a DATO or DATOB bus cycle, the NEW DATA RDY H pulse is generated to inform the user's device of the data transfer. The trailing edge of this positive-going pulse should be used to strobe the data into the user's device in order to allow data to settle on the interface cable. The system initialize signal (BINIT L) will clear DROUTBUF.

All output signals are TTL levels capable of driving eight unit loads except for the following:

New Data Ready = 10 unit loads
Data Transmitted = 30 unit loads
INIT (Initialize) = 10 units per connector

Input Data Interface

The input interface is the 16-bit DRINBUF read-only register, made up of gated bus drivers that transfer data from the user's device onto the LSI-11 bus under program control. DRINBUF is not capable of storing data; hence the user must keep input data on the IN lines until read by the processor. When read, the DRV11 generates a positive-going DATA TRANS H pulse which informs the user's device that the data has been accepted. The trailing edge of the pulse indicates that the input transfer has been completed.

All input signals are one standard TTL unit load; inputs are protected by diode clamps to ground and +5 V.

Request Flags

Two signal lines (REQ A H and REQ B H) can be asserted by the user's device as flags in the DRCSR word. REQ B is available via connector number 2, and it can be read in DRCSR bit 15. REQ A is available via connector number 1, and it can be read in DRCSR bit 7. Two DRCSR interrupt enable bits, INT ENB A (bit 6) and INT ENB B (bit 5), allow automatic generation of an interrupt request when their respective REQ A or REQ B signals are asserted. Interrupt enable bits can be set or reset under program control.

In a typical application, REQ A and REQ B are generated by request flip-flops in the user's device. The user's request flip-flop must be set when servicing is required and must be cleared by the trailing edge of NEW DATA RDY or DATA TRANS when the appropriate data transaction has been completed.

This timing is shown in Figure 9. The logic required by the user to implement this is shown in Figure 10. The logic consists of a flip-flop that is set by the User Request pulse, which indicates that the user's device is requesting a transfer. The flip-flop is reset by the trailing edge of the NEW DATA RDY signal or the DATA TRANS signal.

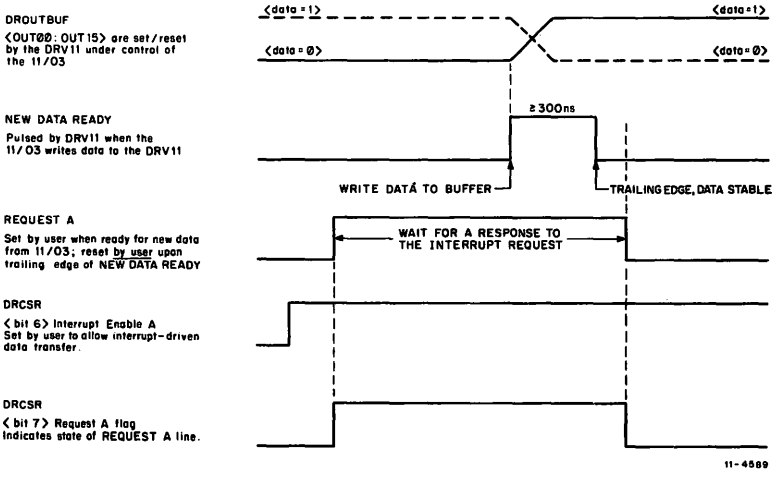


Figure 9 DRV11 Interface Signal Sequence

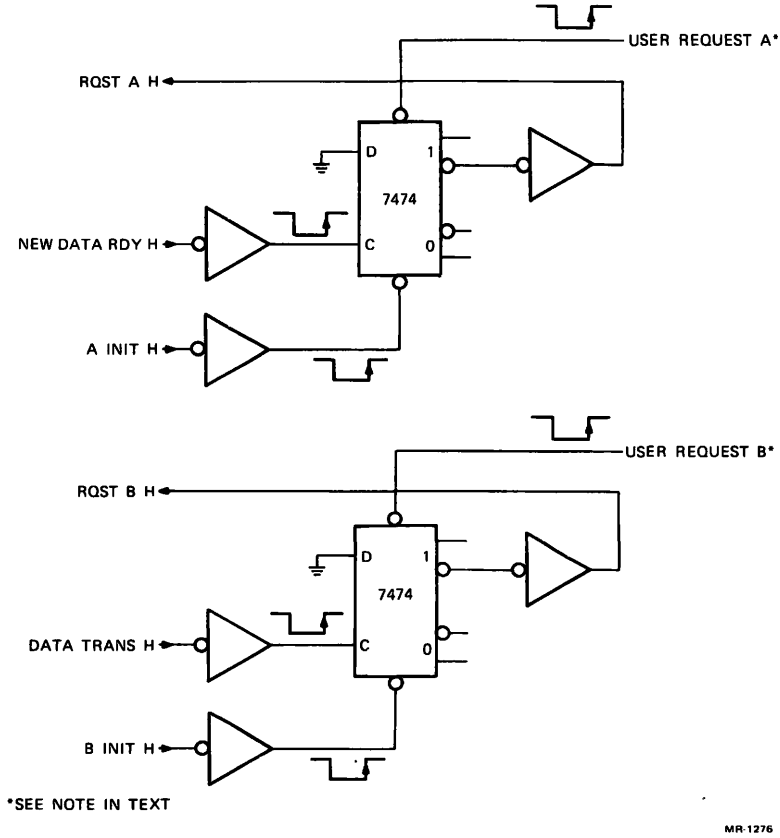


Figure 10 User Request Logic

NOTE

The User Request signal must return to the "high" state prior to the occurrence of the trailing edge of NEW DATA RDY or DATA TRANS. The leading edge of NEW DATA RDY or DATA TRANS can be used for this purpose. In most applications, a pulse on the User Request Line of less than 10 μs is adequate.

Initialization

The BINIT L processor-generated initialize signal is applied to DRV11 circuits for interface logic initialization. It is also available to the user's circuits via connectors J1 and J2 as follows:

Connector/Pin	Signal
J1/P	AINIT H
J2/RR	BINIT H
J2/NN	BINIT H

An active BINIT L signal will clear DROUTBUF data, DRCSR bits 6, 5, 1, 0, bits 16 and 7 (when the maintenance cable is connected), and interrupt request and interrupt acknowledge flip-flops.

NEW DATA RDY and DATA TRANS Pulse Width Modification

An optional capacitor can be added by the user to the DRV11 module to extend the pulse width of both the NEW DATA RDY and DATA TRANS pulse widths. The capacitor can be added in the location shown in Figure 2 to produce the approximate pulse widths listed below.

Optional External	Approximate Pulse Width (ns)	
Capacitance (F)	NEW DATA RDY	DATA TRANS
None	350	1150
0.0047	750	1550
0.01	1550	2400
0.02	2330	3200
0.03	3150	3900

BC08R Maintenance Cable

When using the optional BC08R maintenance cable, the connections listed in Table 9 are provided. Cable connectors P1 and P2 are connected to DRV11 connectors J1 and J2, respectively. Note that CSR0 (J2-K), which can be set or reset under program control, is routed to the REQ A input (J1-LL); similarly, CSR1 (J1-DD) is routed to REQ B (J2-S). Hence, a maintenance program can output data to DROUTBUF and read the same data via the cable and DRINBUF. DRCSR bits 0 (CSR0) and 1 (CSR1) can be used to simulate REQ A and REQ B signals, respectively. If the appropriate INT ENB bit (DRCSR bits 5 or 6) is set, the simulated signal will generate an interrupt request. Note that the BC08R cable must incorporate a half-twist when connected to J1 and J2.

DRV11-B DMA INTERFACE

GENERAL

The DRV11-B is a general purpose direct memory access (DMA) interface used to transfer data directly between tthe LSI-11 system memory and an I/O device. The interface is programmed by the processor to move variable length blocks of 8- or 16-bit data words to or from specified locations in memory by means of the LSI-11 bus. Once programmed, no processor intervention is required. The DRV11-B can transfer up to 250K 16-bit words per second in single cycle mode and up to 500K 16-bit words per second in burst mode. The control structure also allows read-modify-restore operations.

FEATURES

- Buffered input/output data
- Data transfer rate of up to 500K 16-bit words per second
- Tranfer of up to 32K 16-bit words
- Compatible with LSI-11 bus
- 16-bit CSR available for control and status functions
- Two 40-pin I/O connectors mounted on module for interface with user's hardware
- Switch-selectable device address and interrupt vector

SPECIFICATIONS

Identification	M7950
Size	Quad
Power	+5 Vdc ±5% at 1.9 A
Bus Loads	
AC	3.3
DC	1

DESCRIPTION

General

Basic functions that make up the DRV11-A are shown in Figure 9. The following paragraphs describe the DRV11-B registers, the bus operations required for DMA transfers and the DMA transfer timing.

DRV11-B Registers
The DRV11-B contains five registers:

Word Count Register (WCR)
Bus Address Register (BAR)
Control/Status Register (CSR)
Output Data Buffer Register (ODBR)
Input Data Buffer Register (IDBR)

Word Count Register (WCR) — The WCR is a 16-bit read/write register that controls the number of transfers. This register is loaded (under program control) with the 2's complement of the number of words to be transferred. At the end of each transfer, the word count register is incremented. When the contents of the WCR are incremented to zero, transfers are terminated. READY is set, and if enabled, an interrupt is requested. The WCR is word-addressable only.

Bus Address Register (BAR) — The BAR is a 15-bit read/write register. This register is loaded (under program control) with a bus address (not including the address bit 0) which specifies the location to or from which data is to be transferred. The BAR is incremented acros 32K memory boundaries via the extended address feature of the DRV11-B. Systems with only 16 address bits will "wrap-around" to location zero when the extended address bits are incremented. The BAR is word-addressable only.

Control/Status Register — The CSR is a 16-bit register used to control the function and monitor the status of the interface. Bit 0 is a write-only bit and always reads as zero. Bits 1-6 and bits 8 and 12 are read/write bits; bits 7, 8-11 and 13-15 are read-only bits. Bit 14 can be written to a zero. Bits 4 and 5 are the extended addressing bits. The CSR is both byte- and word-addressable.

Input and Output Data Buffer Regisers (DBRs) — The two DBRs are 16-bit registers. The input DBR is a read-only register and the output DBR is a write-only register. Data is loaded into the input DBR by the user's device and subsequently transferred into memory under DMA control by the DRV11-A , or under program control by the processor. Conversely, data is written into the output DBR from memory under DMA control by the DRV11-B, or under program control by the processor, and read by the user's device. The input and output DBRs interface to the user's device by means of two separate 40-pin I/O connectors. These connectors may be cabled together (for maintenance purposes) to function as a read/write register. The input and output DBRs share the same bus address and are byte- and word-addressable.

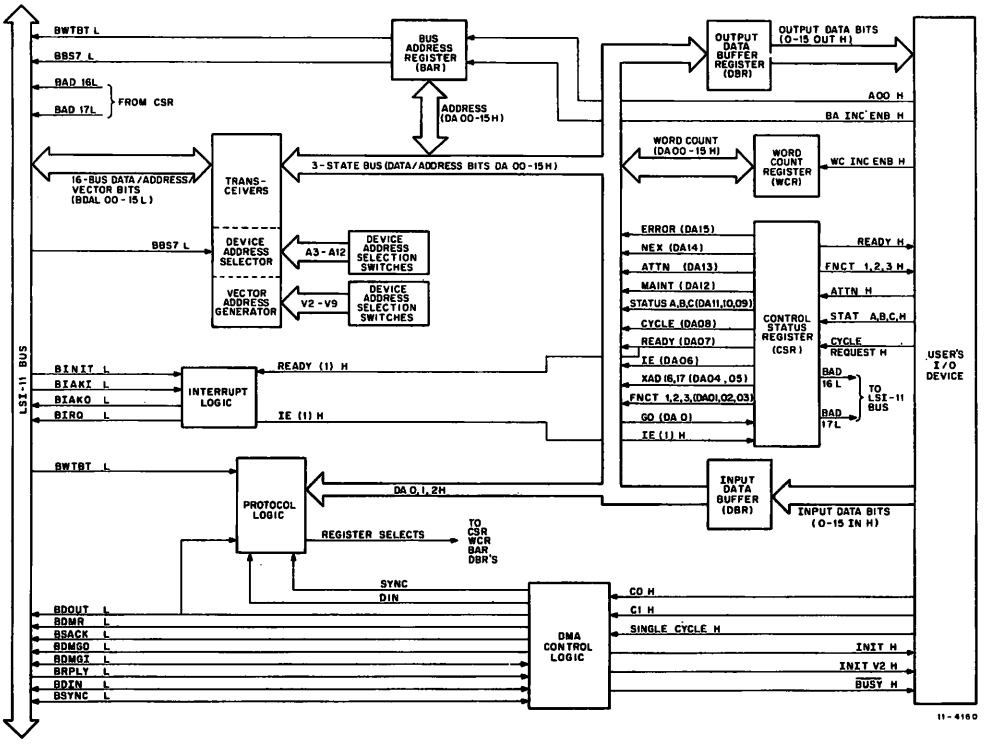


Figure 1 DRV11-B Logic Block Diagram

User's I/O Device to System Memory Transfer (DATO or DATOB)
Data transfers from the user's I/O device to the memory are DMA transfers. Figure 10 illustrates the data flow for a DMA DATO or DATOB cycle. Referring to Figure 9, DMA transfers are initialized under program control by loading the DRV11-B WCR (in 2's complement) with a count equal to the number of words to be transferred; loading the BAR with the starting memory address for word storage; and setting the CSR for transfers.

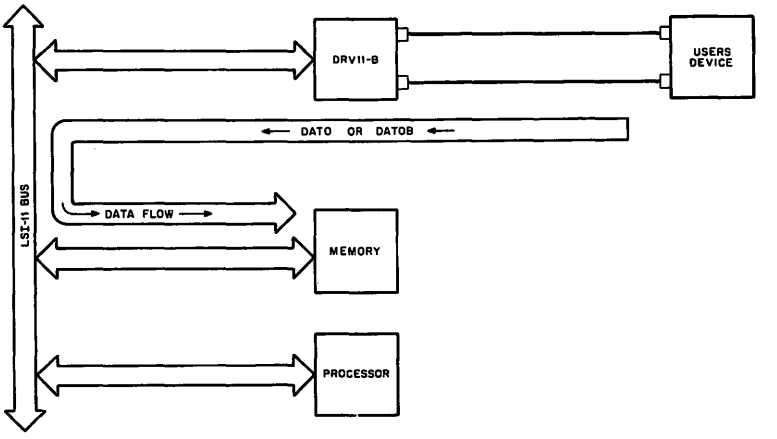


Figure 2 DMA DATO/DATOB Data Flow Diagram

When the GO bit of the CSR is written to a "one," READY goes low, the user's I/O device conditions the A00, BA INC ENB, WC INC ENB, ATTN, SINGLE CYCLE (high for normal DMA transfers), and the C0, C1 (Table 6) lines, and then asserts CYCLE REQUEST. The input data bits and the control bits (C0, C1 and SINGLE CYCLE) are latched into the respective DRV11-B registers. CYCLE REQUEST sets CYCLE and causes the DRV11-B to assert BDMR, which makes an LSI-11 bus request and causes BUSY to go low. In response to BDMR, the processor asserts BDMGO which is received as BDMGI. The DRV11-B becomes bus master and asserts BSACK and negates BDMR. The processor then terminates the bus grant sequence by negating BDMGO.

When the DRV11-B becomes bus master, a DATI or DATIO bus cycle is performed (a DATI is described). The DRV11-B places the address of the memory location from which the first word is taken on the BDAL

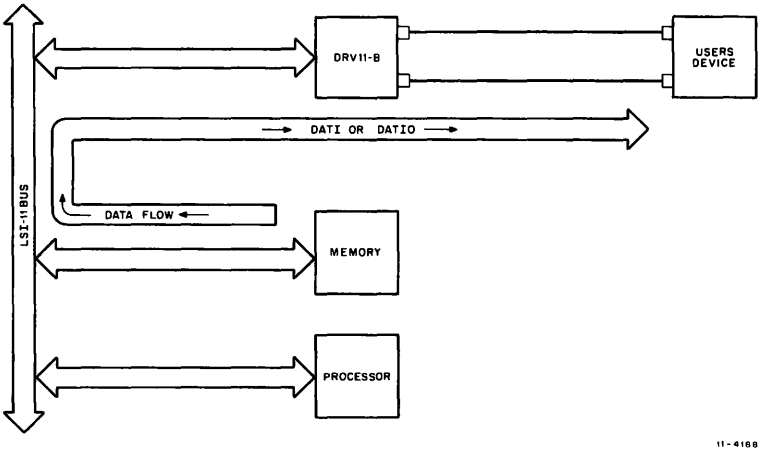


Figure 3 DMA DATIO/DATI Data Flow Diagram

lines and asserts BSYNC. Memory decodes and latches the address. The DRV11-B then removes the address from the BDAL lines and asserts BDIN. Input data is now placed on the BDAL lines by the memory and the memory asserts BRPLY. The input data is accepted by the DRV11-B and BDIN is negated. Memory negates BRPLY and the DRV11-B negates BSACK and BSYNC to terminate the bus cycle and release the bus. The output data bits for the user's I/O device are stored in the DRV11-B output data buffer register. These bits can be read by the user's device at the low-to-high transition of BUSY.

At the end of the first transfer, the DRV11-B WCR and BAR are incremented, BUSY goes high and READY remains low. The user's device can initiate another DATI or DATIO cycle by again setting CYCLE REQUEST. DMA transfers to the user's device can continue until the WCR increments to zero and causes an interrupt request to be generated.

DMA Transfers

The DRV11-B interface is designed for DMA transfers which the user can accomplish in several ways. DMA transfers are always set up by the processor when it loads the BAR and WCR and sets the READY bit. The user then has the option of initiating transfers either by program control (setting the GO bit in the CSR) or by the user device asserting CYCLE REQUEST for 1 μs minimum.

Type of I/O to be Performed — The user has the option of selecting DATI, DATO, DATOB, or DATIO bus cycles by asserting C0 and C1 per Table 6. Note that if byte transfers are being performed, the byte address bit (A00) must be manipulated by the user. (Refer to the section entitled "Word or Byte Transfers.")

Burst Mode vs. Single Cycle DMA — Single cycle DMA allows the asynchronous transfer of data to or from the user's device. Each time the user's device is ready for a transfer, the user asserts CYCLE REQUEST for 1 μs. A DMA cycle is requested from the LSI-11 bus, and when the bus is granted to the DRV11-B, the BUSY line is asserted to inform the user that a data transfer is underway. The user must set up input data when CYCLE REQUEST is asserted, and hold it valid until the next assertion of CYCLE REQUEST. The user must strobe output data out of the DRV11-B on the rising edge of BUSY. The data will be valid 250 ns minimum before the rising edge of BUSY. (Figures 12 and 13 are detailed timing diagrams.)

Burst mode DMA allows synchronous transfer of data between a user's device and the DRV11-B. Once a DMA sequence is started (either by the user or by the processor), data will be transferred at a synchronous rate of 500K words per second. One data word will be transferred every 2 μs. The user must strobe data out of the DRV11-B into the user's device on the rising edge of BUSY. The data to be transferred to the DRV11-B must be set up when the READY line goes low (for the first data transfer) or on the rising edge of BUSY (for subsequent data transfers). (Figures 14 and 15 are detailed timing diagrams.)

Word or Byte Transfers — The DRV11-B can transfer words or bytes to memory. Transfers from memory are always on a word basis; if only one byte is required, the unused bytes are disregarded. To transfer data on a byte basis to memory, the following operations must be performed:

1. A00 must be manipulated by the user to address the proper byte in memory.
2. The byte to be transferred to memory must be input in its proper position in the input word, i.e., if A00 is 1, the byte to be input must be on the input lines IN 8 H through IN 15 H (high byte being transferred).
3. WC INC EN H and BA INC EN H must be asserted during the write cycle of the first byte of each word to inhibit the BAR and WCR from incrementing.

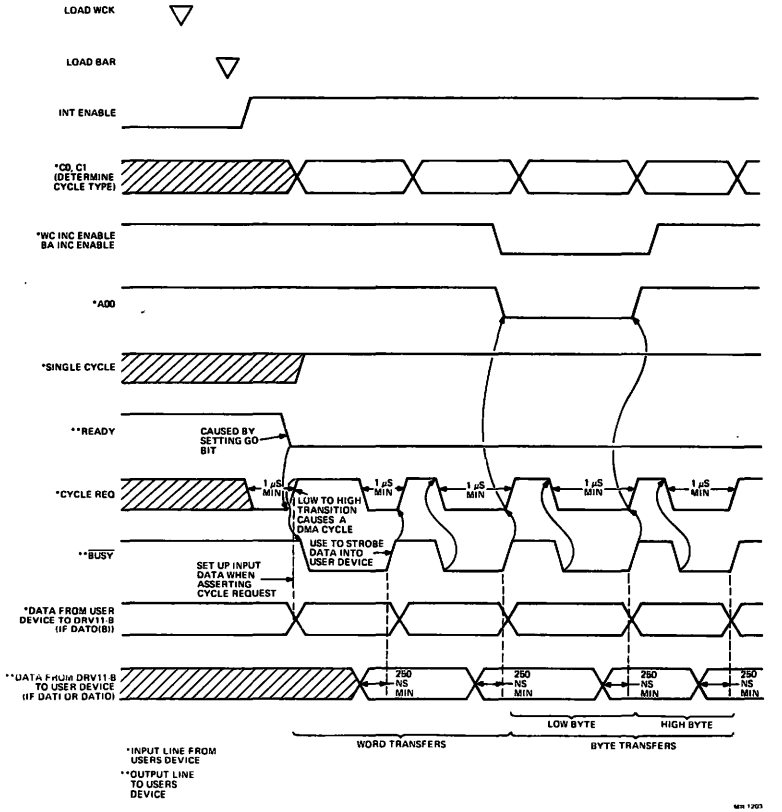


Figure 4 DRV11-B Timing: Single Cycle, Asynchronous, User-Initiated

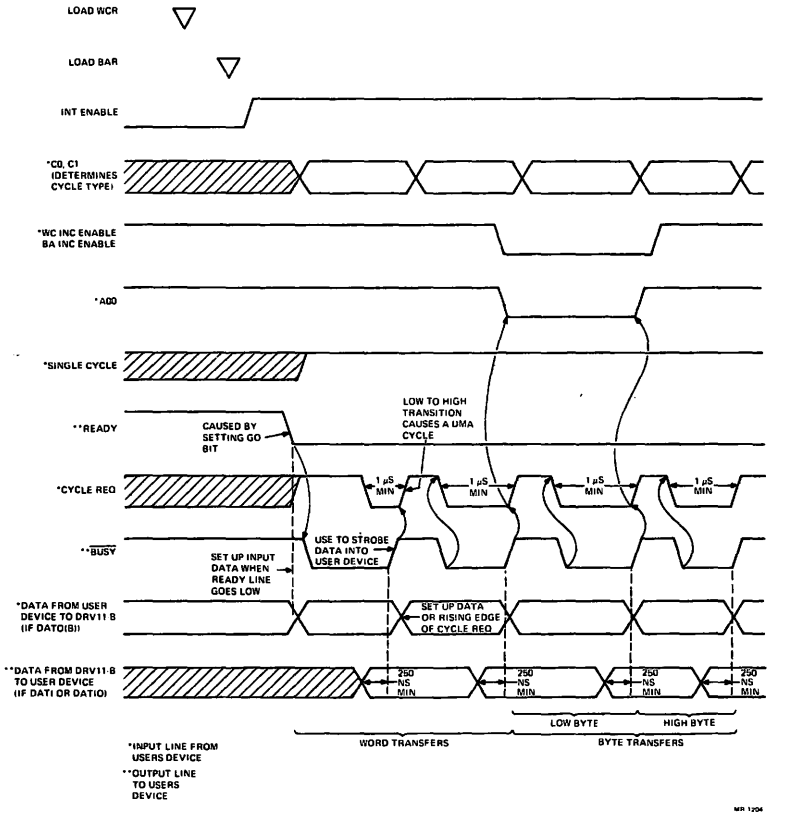


Figure 5 DRV11-B Timing: Single Cycle, Asynchronous, Program-Initiated

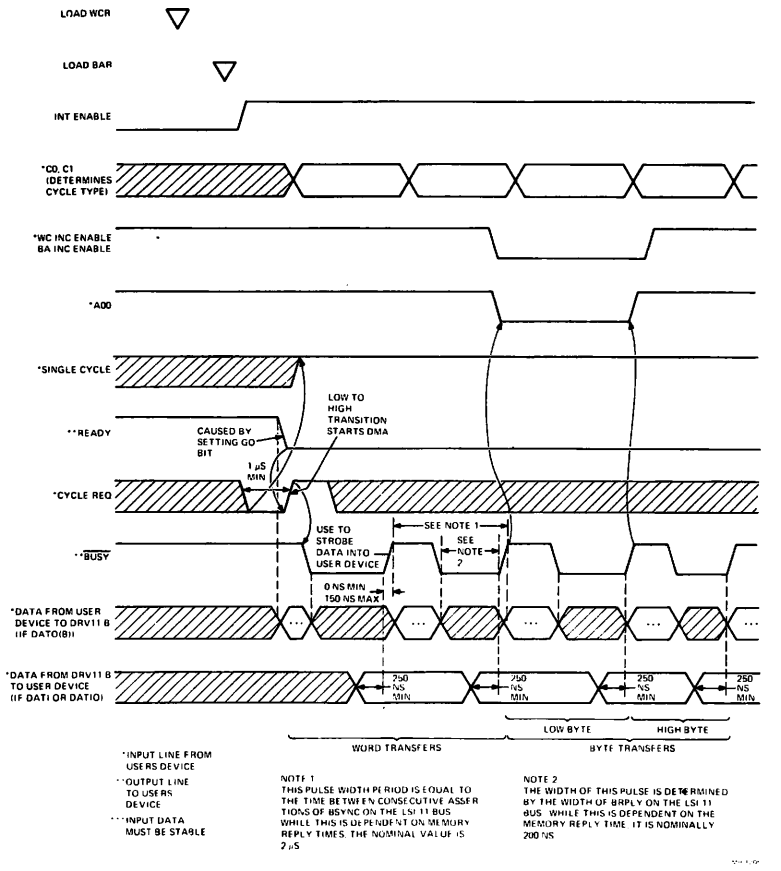


Figure 6 DRV11-B Timing: Burst Mode, User-Initiated

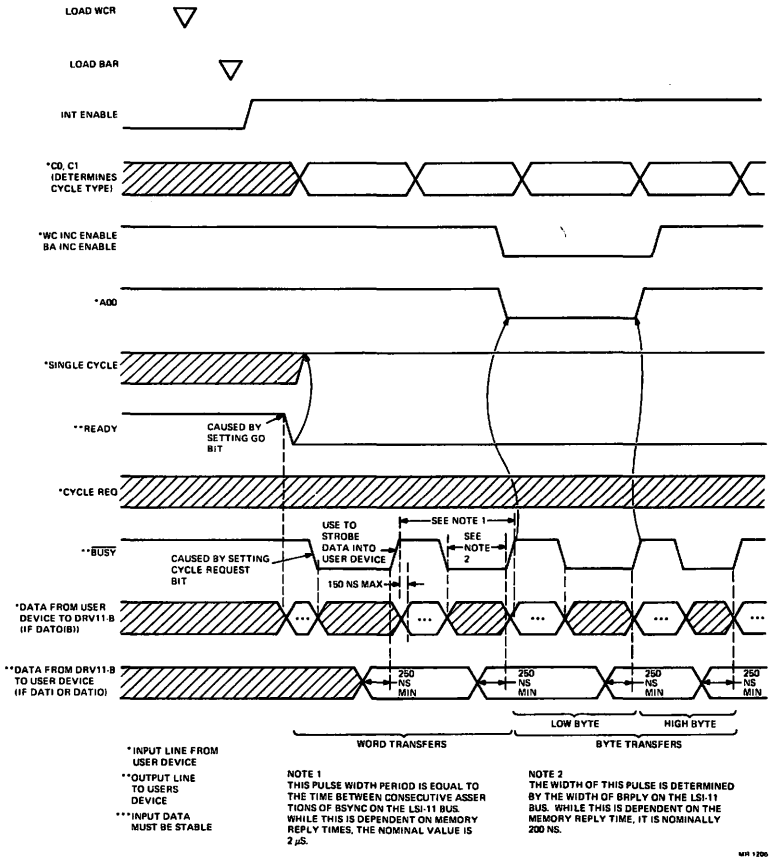


Figure 7 DRV11-B Timing: Burst Mode, Program Initiated

Miscellaneous Signals — Four sets of signals exist to perform handshaking and status exchange between the processor and the user's device. They are:

STATUS A, B, C—These three TTL lines are used to input status to the DRV11-B from the user's device.

FUNCT 1, 2, 3—These three TTL lines are used to output status from the DRV11-B to the user's device.

INIT, INIT V2—INIT is asserted when the LSI-11 bus INIT signal is asserted. INIT V2 is asserted either when the LSI-11 bus INIT is asserted or when FUNCT 2 is a 1.

ATTN—ATTN terminates a DMA transfer. This sets the READY bit and causes an interrupt (if the interrupt enable bit has been set).

DRV11-B

CONFIGURATION

General

The interface consists of five registers (Table 1): word count register (WCR), bus address register (BAR), control/status register (CSR), input data buffer register (IDBR), and output data buffer register (ODBR). The module also includes bus transceivers and logic for interrupt requests, address control and protocol, and DMA requests.

Table 1 Standard Addresses

Description	Mnemonic	Read/ Write	Address
Register			
Word Count	WCR	R/W	172410
Bus Address	BAR	R/W	172412
Control/Status	CSR	R/W	172414
Input Data Buffer	IDBR	R	172416
Output Data Buffer	ODBR	W	172416
Interrupt			
Interrupt Vector	—	—	124

The DRV11-B contains two switch packs, one to assign an appropriate device address to the DMA interface and one to select an interrupt vector.

The address of both the DRV11-B interface and the interrupt vector is selected by the position of the switches in switch pack S2 and S1, respectively. The location of the switches on the module is shown in Figure 1. The switches are set to the OFF position (open) to select a zero bit and the ON position (closed) to select a one.

Device Address Format

The DRV11-B decodes four addresses, one for each of the registers listed:

Register	Octal Address
WCR	1XXXX0
BAR	1XXXX2
CSR	1XXXX4
DBR	1XXXX6

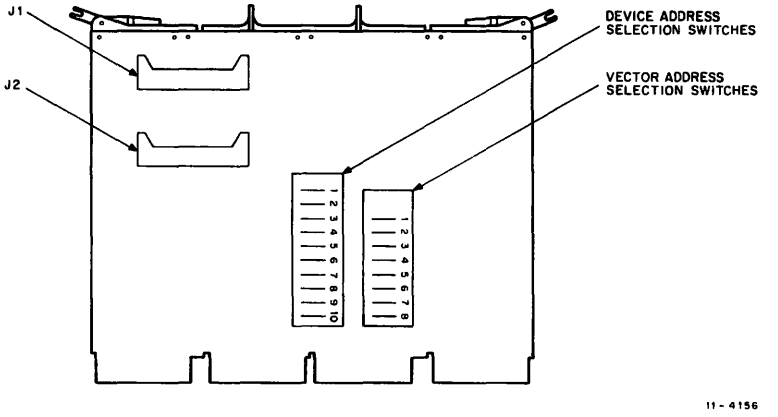


Figure 8 DRV11-B Connector and Switch Locations

Normally, the addresses assigned to the DMA start at 772410_8 and progress upward. Switches S2-1 through S2-10 select the base address as indicated by the X portion of the octal code; the individual registers are decoded by the DMA interface. The relationship between the address format and the switches is shown in Figure 2.

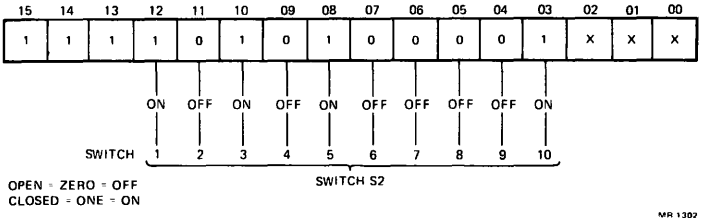


Figure 9 Device Address Switch S2 Selection

Interrupt Vector Selection

The interrupt vectors for the LSI-11 systems are allocated from $0\text{-}774_8$. The recommended vector assigned to the DRV11-B is 124_8. Switches S1-1 through S1-8 are used to select the vector. The relationship between the switches and the vector format is shown in Figure 3.

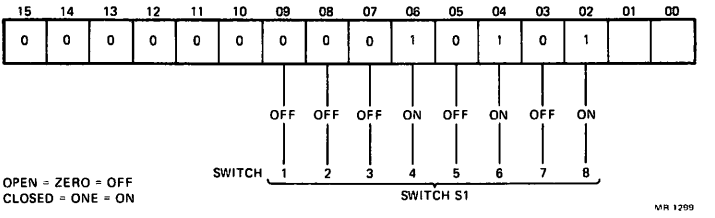


Figure 10 Interrupt Vector Switch S1 Selection

Registers

Each of the five registers can be addressed by the processor. The IDBR and ODBR are assigned the same address and are read-only and write-only, respectively.

Word Count Register (WCR) — The WCR (Figure 4) is a 16-bit read/write counter which is loaded by the program with the 2's complement of the number of words or bytes to be transferred at one time between memory and the I/O device. At the end of each transfer, the WCR is incremented. When the count becomes zero (all 16 bits = 0), the DMA generates an interrupt request. The contents of the WCR can be monitored by the processor program.

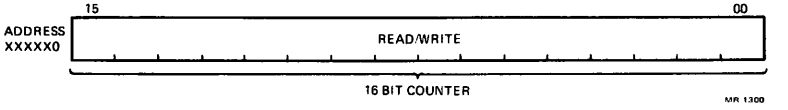


Figure 11 Word Count Register

Bus Address Register (BAR) — The BAR (Figure 5) is a 16-bit read/write register used to generate the bus address which specifies the location to or from which data is to be transferred. The register is incremented after each transfer. It will increment across 32K boundary lines via the extended address bits in the control/status register. Bus address bit 0 is driven by the user device.

Control and Status Register (CSR) — The CSR (Figure 6) contains 16 bits of information used to control the function and monitor the status of the DMA transfers. The information in the CSR can be modified or read by the processor program in either 8-bit bytes or 16-bit words. Table 2 lists and defines each of the 16 bits.

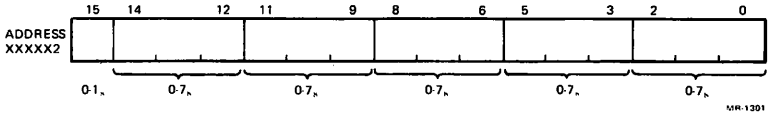


Figure 12 Bus Address Register

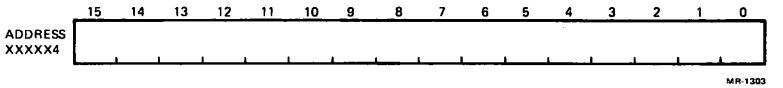


Figure 13 Control/Status Register

Table 2 DRV11-B Control/Status Register Bit Description

Bit: 15 **Name:** Error
Description: (Read-only)
Indicates a special condition
NEX (bit 14)
ATTN (bit 13)

Sets READY (bit 7) and causes interrupt if IE (bit 6) is set.

Cleared by removing the special condition.
NEX is cleared by writing to zero.
ATTN is cleared by the user device.

Bit: 14 **Name:** NEX
Description: (Read/Write zero)
Nonexistent memory indicates that as bus master, the DRV11-B did not recieve BRPLY or that a DATIO cycle was not completed.

Sets error (bit 15).

Cleared by INIT or by writing to zero.

Bit: 13 **Name:** ATTN
Description: (Read-only)
Indicates the state of the ATTN user signal.

Sets error (bit 15).

Bit: 12 **Name:** MAINT
Description: (Read/Write)
Maintenance bit used with diagnostic program.

Bit: 11 **Name:** STAT A
Description: (Read-only)
Device status bit that indicates the state of the DSTAT A, B, and C, user signals.

Set and cleared by user control only.

Bit: 10 **Name:** STAT B
Description: (Read-only)
Device status bit that indicates the state of the DSTAT A, B, and C user signals.

Set and cleared by user control only.

Bit: 9 **Name:** STAT C
Description: (Read-only)
Device status bit that indicates the state of the DSTAT A, B, and C user signals.

Set and cleared by user control only.

Bit: 8 **Name:** CYCL
Description: (Read/Write)
Cycle is used to prime a DMA bus cycle.

Bit: 7 **Name:** READY
Description: (Read-only)
Indicates that the DRV11-B is able to accept a new command. Requests an interrupt if IE (bit 6) is set.

Set by INIT.

Bit: 6 **Name:** IE
Description: (Read/Write)
Enables interrupts to occur when READY (bit 7) is set.

Cleared by INIT.

Bit: 5 **Name:** XAD 17
Description: (Read/Write)
Extended access bit 17; cleared by INIT.

Bit: 4 **Name:** XAD 16
Description: (Read/Write)
Extended address bit 16; cleared by INIT.

Bit: 3 **Name:** FNCT 3
Description: (Read/Write)
One of three bits made available to the user device. User defined.
Cleared by INIT.

Bit: 2 **Name:** FNCT 2
Description: (Read/Write)
One of three bits made available to the user device. User defined.

Cleared by INIT.

Bit: 1 **Name:** FNCT 1
Description: (Read/Write)
One of three bits made available to the user device. User defined.

Cleared by INIT.

Bit: 0 **Name:** GO
Description: (Write-only)
Causes "NOT READY" to be sent to the user device indicating a command has been issued. Clears READY (bit 7). Enables DMA transfers.

Input Data Buffer Register (IDBR) — The IDBR (Figure 7) is used for read-only operations. Data is loaded into the register by the user's device. The data may be read from the IDBR as a 16-bit word, an 8-bit high byte or an 8-bit low byte. Transfers are usually via DATO or DATOB DMA bus cycles. The register input connects to J2 mounted on the module.

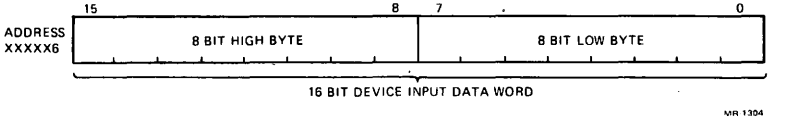


Figure 14 Input Data Buffer Register

Output Data Buffer Register (ODBR) — The ODBR (Figure 8) is used during write-only operations. Data from the LSI-11 bus is loaded into the register under program control and read from the register by the user's device. The register can be loaded with a 16-bit data word or with an 8-bit high byte or an 8-bit low byte. Transfers are usually via DATI or DATIO DMA bus cycles. The output of the register connects to J1 on the module.

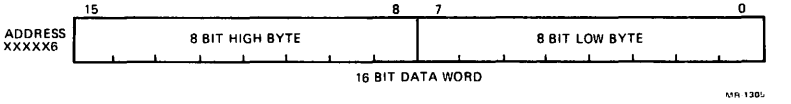


Figure 15 Output Data Buffer

PROGRAMMING

General

The DRV11-B interface operates as both a slave and a master device. Prior to becoming bus master, all data transfers out (DATO) or data transfers in (DATI) are in respect to the processor. Once the DRV11-B is granted bus mastership by the processor, all data transfers are in respect to the DRV11-B.

DMA operation is initialized under program control by loading the WCR with the 2's complement of the number of words to be transferred, loading the BAR with the first address to or from which data is to be transferred, or loading the CSR with the desired function bits. After the interface is initialized, data transfers ae under control of the DMA logic.

Program Control Transfers

Data transfers may be performed under program control by addressing the IDBR or ODBR and reading or writing data.

DMA Control Transfers

DMA input (DATI) or output (DATO) data transfers occur when the processor clears READY. For a DATO cycle (DRV11-B to memory transfer), the user's I/O device presets the control bits [word count increment enable (WC INC ENB), bus address increment enable (BA INC ENB), C1, C0, A00, and ATTN], and asserts CYCLE REQUEST to gain use of the LSI-11 bus. When CYCLE REQUEST is asserted, input data is latched into the input DBR, the control bits are latched into the DRV11-B DMA control and BUS goes low. A DATI cycle—memory to DRV11-B transfer—is handled in a similar manner, except that the output data is latched into the output DBR at the end of the bus cycle.

When the DRV11-B becomes bus master, a DATO or DATI cycle is performed directly to or from the memory location specified by the BAR. At the end of each cycle, the WCR and BAR are incremented and BUSY goes high while READY remains low. A second DATO or DATI cycle is performed when the user's I/O device again asserts CYCLE REQUEST. DMA transfers will continue until the WCR increments to zero, at which time READY goes high and the DRV11-B generates an interrupt (if interrupt enable is set) to the processor.

If burst mode is selected (SINGLE CYCLE low), only one CYCLE REQUEST is required for the complete transfer of the specified number of data words.

Device Cables and Signals

Data, status, and control signals are transferred between the user's

I/O device and DMA by an input and an output cable assembly. The input cable attaches to connector J2 and the output cable attaches to connector J1. Tables 3 and 4 list the connector pin and designations for each signal. Table 5 lists several recommended cable assemblies that are available from DIGITAL in the lengths indicated. The H856 female connector mates with either J1 or J2 on the DRV11-B. To order cable assemblies in lengths not listed, contact a DIGITAL sales office. Cables up to 15.2 m (50 ft) maximum may be used.

Table 3 DRV11-B Input Connector Signals

J2* Connector Pin	Signal Name	Unit Loads
B	BUSY H	10 (drive)
D	ATTN H	1
F	A00 H	1
J	BA INC ENB H	1
K, L	FNCT 3 H	10 (drive)
N	C0 H	1
R	FNCT 2 H	10 (drive)
T	C1 H	1
V	FNCT 1 H	10 (drive)
DD	08 IN H	
FF	09 IN H	
JJ	10 IN H	
LL	11 IN H	
NN	12 IN H	
RR	13 IN H	
TT	14 IN H	
VV	15 IN H	
CC	07 IN H	
EE	06 IN H	
HH	05 IN H	1
KK	04 IN H	
MM	03 IN H	
PP	02 IN H	
SS	01 IN H	
UU	00 IN H	

* All remaining pins connect in common to logic ground by board etch.

Table 4 DRV11-B Output Connector Signals

J1* Connector Pin	Signal Name	Unit Loads
B	CYCLE REQUEST H	1
D	INIT V2 H	10 (drive)
F	READY H	10 (drive)
J	WC INC ENB H	1
K	SINGLE CYCLE H	1
L	STATUS A	1
N	INIT H	10 (drive)
R	STATUS B	1
T, V	STATUS C	1
DD	08 OUT H	
FF	09 OUT H	
JJ	10 OUT H	
LL	11 OUT H	
NN	12 OUT H	
RR	13 OUT H	
TT	14 OUT H	
VV	15 OUT H	
CC	07 OUT H	
EE	06 OUT H	10 (drive)
HH	05 OUT H	
KK	04 OUT H	
MM	03 OUT H	
PP	02 OUT H	
SS	01 OUT H	
UU	00 OUT H	

* All remaining pins connect in common to the logic ground by board etch.

Table 5 Recommended Cable Assemblies

Cable No.	Connectors	Type	Standard Lengths (ft)
BC07D-XX	H856 to open end	ribbon	2,20 conductor
10, 15, 15			
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25, 50
BC04Z-XX	H856 to open end		Shielded flat
6, 10, 15, 25, 50			

Table 6 DRV11-B Interface Connector Signals

Mnemonic	Description
00 OUT — 15 OUT	16 TTL data output lines from the DRV11-B. One = high
00IN — 15 IN	16 TTL data input lines from the user's device. One = high
STATUS A, B, C	Three TTL status input lines from the user's device. The function of these lines is defined by the user.
FUNCT 1, 2, 3	Three TTL output lines to the user's device. The function of these lines is defined by the user.
INIT	One TTL output line; used to initialized the user's device.
INIT V2	One TTL output line; present when INIT is asserted or when FUNCT 2 is written to a one. Used for interprocessor buffer applications.
A00	One TTL input line from the user's device. This line is normally high for word transfers. During byte transfers this line controls address bit 00.

Table 6 DRV11-B Interface Connector Signals

Mnemonic	Description
BUSY	One TTL output line to the user's device. BUSY is low when the DRV11-B DMA control logic is requesting control of the LSI-11 bus or when a DMA cycle is in progress. A low-to-high transition indicates end of cycle.
READY	One TTL output line to the user's device. When the READY line goes low, DMA transfers may be initiated by the user's device.
C0, C1	Two TTL input lines from the user's device. These lines control the LSI-11 bus cycle for DMA transfers. C0, C1 codes for the four (4) possible bus cycles as listed below: **Bus Cycle C0 C1** DATI 0 0 DATIO 1 0 DATO 0 1 DATOB 1 1
SINGLE CYCLE	One TTL input line from the user's device. This line is internally pulled high for normal DMA transfers. For burst mode operation, SINGLE CYCLE is driven low by the user's device. **CAUTION:** When SINGLE CYCLE is driven low, total system operation is affected because the LSI-11 bus becomes dedicated to the DMA device and other devices cannot use the bus.
WC INC ENB	One TTL input line from the user's device. This line is normally high to enable incrementing the DRV11-B word counter. Low inhibits incrementing.
BA INC ENB	One TTL input line from the user's device. This line is normally high to enable incrementing the bus address counter. Low inhibits incrementing.

Table 6 DRV11-B Interface Connector Signals (Cont)

Mnemonic	Description
CYCLE REQUEST	One TTL input line from the user's device. A low-to-high transition of this line initiates a DMA request.
ATTN	One TTL input line from the user's device. This line is driven high to terminate DMA transfers, to set READY, and to request an interrupt if the interrupt enable bit is set.

As bus master, the DRV11-B performs a DATO or DATOB bus cycle by placing the memory address on BDAL lines, asserting BWTBT, and then asserting BSYNC. The memory decodes the address, then the DRV11-B removes the address from the BDAL lines, negates BWTBT (BWTBT will remain active for a DATOB), places the user's input data on the BDAL lines and asserts BDOUT. Memory receives the data and asserts BRPLY. In response to BRPLY, the DRV11-B negates BDOUT and then removes the user's input data from the BDAL lines. Memory now negates BRPLY, the bus cycle is terminated, and the bus released when the DRV11-B negates BSACK and BSYNC.

At the end of the first transfer, the DRV11-B WCR and BAR are incremented, BUSY goes high, and READY remains low. With BUSY high and READY low, the user's I/O device can initiate another DATO or DATOB cycle by again asserting CYCLE REQUEST.If the interrupt enable is set, DMA transfers can continue until the WCR increments to zero and generates an interrupt request.When the WCR increments to zero, READY goes high, and the DRV11-B generates an interrupt request (if the interrupt circuits are enabled). The processor responds to the interrupt request (BIRQ) by asserting BDIN followed by BIAKI (interrupt acknowledge). BIAKI is received by the DRV11-B and in response places a vector address on the BDAL lines, asserts BRPLY, and negates BIRQ. The processor receives the vector address and negates BDIN and BIAKI. The DRV11-B now negates BRPLY, while the processor exits from the main program and enters a service program for the DRV11-B via the vector address.

Interrupt requests from the DRV11-B occur for the following conditions:

1. When the WCR increments to zero—this is a normal interrupt at the end of a designated number of transfers.

2. When the user's I/O device asserts ATTN—this is a special condition interrupt which may be defined by the user to override the WCR.
3. When a nonexistent memory location is addressed by the DRV11-B—this special condition interrupt is produced when no BRPLY is received from the memory.

System Memory to User's Device Transfers (DATIO or DATI)

DMA transfers from the memory to the user's I/O device occur in a manner similar to that described for user's I/O device to memory transfers. Figure 11 illustrates the data flow for a DMA DATIO or DATI cycle. Under program control, the DRV11-B WCR (Figure 9) is loaded with a count equal to the number of transfers, while the BAR is loaded with the starting address from which the first word will come; the CSR is set for transfers.

With the CSR set, READY goes low and the user's I/O device conditions the C0, C1 lines (Table 6) for a DATI or a DATIO, conditions the WC INC ENB, BA INC ENB, ATTN, SINGLE CYCLE (high for normal DMA transfers) signals, and asserts CYCLE REQUEST.

DRV11-J

HIGH DENSITY PARALLEL INTERFACE

GENERAL

Sixty-four input/output data lines are now available on a double-height module for the LSI-11/2, LSI-11/23, PDP-11/03, and PDP-11/23. The DRV11-J also includes an advanced interrupt structure with bit interruptability up to 16 lines, programmable interrupt vectors, and program selection of fixed or rotating interrupt priority within the DRV11-J.

The DRV11-J's bit interrupts for real-time response make it especially useful for sensor I/O applications. It can also be used as a general-purpose interface to custom devices, and two DRV11-Js can be connected back-to-back as a link between two LSI-11 buses.

FEATURES

- 64 tri-state bidirectional input/output lines organized as four 16-bit ports, A through D.
- Data line direction selectable under program control for each 16-bit port.
- Transitions on each of the 16 lines of Port A can generate unique interrupt vectors (bit interrupts). This means high-priority inputs get serviced by the CPU much faster.
- Transitions on the USER RPLY lines of each port can generate unique interrupt vectors (I/O interrupts). This means less processor overhead. By selecting this feature, bit interrupts are reduced to 12.
- Double-height module: 22.8cm × 13.2cm (8.9 in. × 5.2 in.)
- Drive up to 25 feet of shielded cable, 6 feet of unshielded flat or round cable.
- Four external control lines per port: USER RDY, USER RPLY, DRV11-J RDY, and DRV11-J RPLY.
- Interrupt vectors (fixed or rotating priority) are set under program control. This eliminates the need for jumper-defined vectors.
- Latched outputs, PNP-Schmitt-trigger inputs.

SPECIFICATIONS

Identification M8049

Power

+5V±5% 1.6A typical, 1.8A maximum

Bus Loading:

2 ac loads, 1 dc load

Data Buffer Tri-State Outputs:
V_{OL} = 0.5V @ I_{OL} = 8 mA
V_{OL} = 0.4V @ I_{OL} = 4 mA
V_{OH} = 2.4V @ I_{OH} = −2.6 mA

Data Buffer Inputs:
I_{IL} = −0.2 mA @ V_{IL} = 0.4V
I_{IH} = 20 μA @ V_{IH} = 2.7V

Protocol Signal Tri-State Outputs:
V_{OL} = 0.55V @ I_{OL} = 64 mA
V_{OH} = 2.4V @ I_{OH} = −15 mA

Protocol Signal Inputs:
Termination: 120 ohms
I_{IL} = −2.7 mA @ V_{IL} = .5V
I_{IH} = 80 μA @ V_{IH} = 2.7V

Environmental:
Storage temperature: −40°C to +60°C
Operating temperature: +5°C to +60°C
Adequate airflow must limit the inlet to outlet temperature rise to 10°C (5°C if inlet air is 55°C).

NOTE

Derate maximum operating temperature by 1.8°C for each 1000 meters of altitude above sea level.

Humidity: 10% to 90%, non-condensing

Size
Double-height module:
13.2cm (5.2in.) wide
22.8cm (8.9in.) long

Cabling:
BC05W-xx—Shielded cable with 50-pin connectors at both ends. Available in 3.0 and 7.5 meter (10 and 25 foot) lengths.

DESCRIPTION
Detailed information about the DRV11-J is supplied with the module.

DRV11-J

PROGRAMMING

The DRV11-J is programmed through eight contiguous directly addressable registers, which may be positioned to start from 760000_8 through 777760_8 in address space by stake pin jumpers. There are four Control Status Registers and four Data Buffers.

The Registers are:

Control Status Register A	(CSRA)	$7XXXX0_8$
Data Buffer Register A	(DBRA)	$7XXXX2_8$
Control Status Register B	(CSRB)	$7XXXX4_8$
Data Buffer Register B	(DBRB)	$7XXXX6_8$
Control Status Register C	(CSRC)	$7XXX10_8$
Data Buffer Register C	(DBRC)	$7XXX12_8$
Control Status Register D	(CSRD)	$7XXX14_8$
Data Buffer Register D	(DBRD)	$7XXX16_8$

XXXX is jumper-selectable between 6000_8 to 7776_8 in a modulus of 16 and factory-set to 6416_8 (CSRA = 764160_8).

The format of these registers is shown in Figure 1.

Unlike other LSI-11 interface modules, the DRV11-J uses two sets of eight internal registers to control interrupts. The first set of registers is controlled through CSRA and CSRB and is responsible for interrupts generated in bits 0-7 of Port A. The second set of registers is controlled through CSRC and CSRD and is responsible for either bits 8-15 of Port A or, when I/O interrupts are selected, the four USER RPLY lines and bits 8-11 of Port A (see Figure 1).

IRR	Interrupt Request Register
ISR	Interrupt Service Register
IMR	Interrupt Mask Register
ACR	Auto Clear Register
—	Status Register
—	Mode Register
—	Command Register
—	Byte Count
—	Vector Address Memory

Interrupt vectors are stored in Vector Address Memory. Vector addresses can be set from 0 to 1774_8 and must be loaded on power-up. To provide for dynamic changing of interrupt subroutines, vectors are programmable. Four vectors are available for each of the sixteen interrupts.

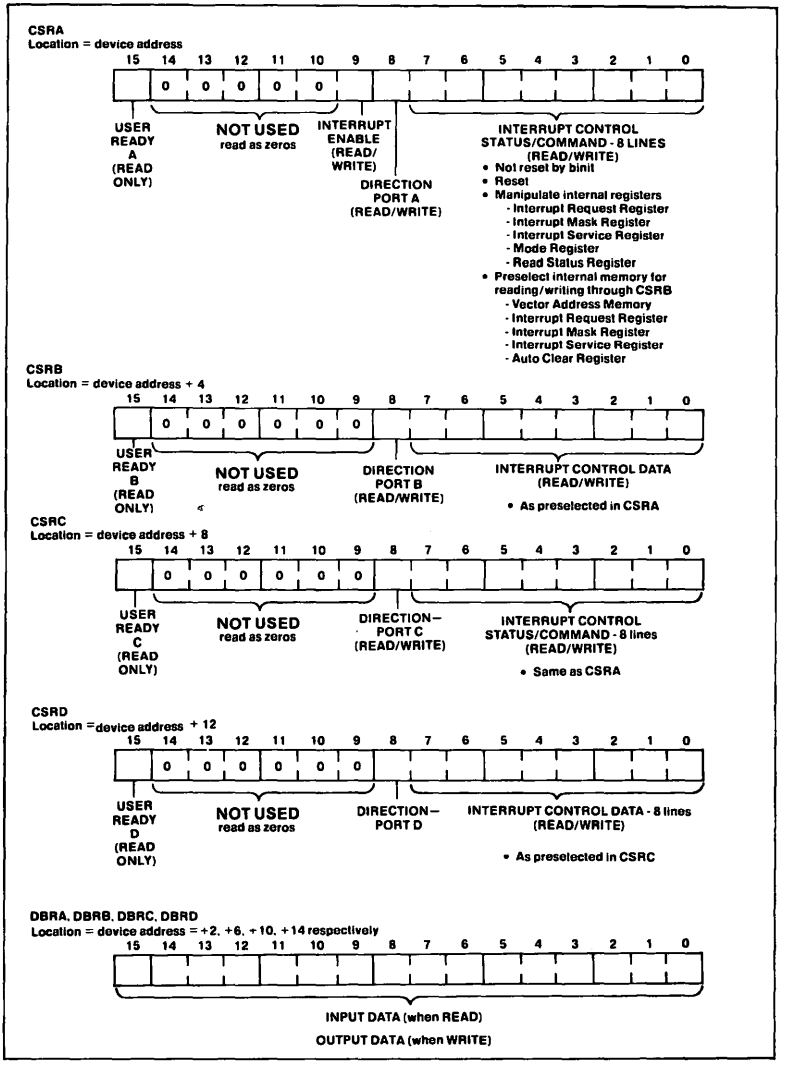


Figure 1 Register Format

DRV11-P

DRV11-P LSI-11 BUS FOUNDATION MODULE

GENERAL

The DRV11-P is an LSI-11 bus-compatible foundation wire-wrap interface module. Approximately one-quarter of the module is occupied by bus transceivers, interrupt vector generator logic, and a 40-pin I/O connector. The remaining three-quarters of the module is for user application and has plated-through holes to accept ICs and wire-wrap pins (WP) for interconnecting the user's circuits. The plated-through holes can accept 6-, 8-, 14-, 16-, 18-, 20-, 22-, 24-, and 40-pin dual-in-line ICs or IC sockets in various mounting areas of the module, or discrete components can be inserted into the plated-though holes. The DRV11-P can be inserted into any one of the available interface option locations of any LSI-11 bus.

FEATURES

- An easy-to-use foundation module for custom interface applications.
- Factory-installed LSI-11 bus-compatible interface circuits.
- Device and interrupt vector that can be configured by the user.
- Compact—occupies only two device locations on the bus.
- Can accommodate up to 50 integrated circuits making up the user's device logic.
- Wire-wrap pins are provided for all signals.
- All user control signal lines are TTL-compatible.

SPECIFICATIONS

Identification	M7948
Size	Quad
Power	5.0 Vdc ±5% at 1.0 A
Bus Loads	
AC	2.1
DC	1 (plus user's logic)

DESCRIPTION

General

The DRV11-P contains 16 bus transceivers, device selection and interrupt vector generation logic, interrupt control, and control and status register functions. The device data inputs and outputs of the bus

transceivers and the device control signals are made available to the user to complement control of up to four 16-bit registers.

Address Selection Logic

The address selection logic consists of a device address comparator and the protocol control logic. Up to four discrete addresses are made available with the existing logic on the DRV11-P and can be assigned to data registers, status and control registers, or word counters. By adding additional ICs, the user can increase the total number of addresses available. The main address of the DRV11-P is selected by monitoring the BBS7 bus line and decoding address information D03-D12 from the bus. The main device address is assigned by the configuration of jumper leads (A03-A08) attached to wire-wrap pins. When the selected and input bus addresses are the same, the device address comparator provides an ENB H level to the protocol control logic. The protocol control logic receives bus signals and address bits D01 and D02 to assert one of the four available output lines: SEL DEV 0L, SEL DEV 2L, SEL DEV 4L, and SEL DEV 6L. In addition, the protocol control logic provides output signals to specify word or byte transfers.

Table 1 lists and defines the function of the control signals required or available for the user logic.

Table 1 DRV11-P Protocol Control Logic Signals

Signal	Function
SEL DEV 0 L SEL DEV 2 L SEL DEV 4 L SEL DEV 6 L	Select device 0 through 4. One of four lines asserted by decoding the device address and available to select one of four user word registers.
OUT LB L OUT HB L	Out low byte, out high byte. Used to load (write) data into low byte (8 bits) or high byte (8 bits) or both bytes (16 bits) of the selected word register.
IN WD L	In word. Used to gate (read) data from the selected word register to the bus.

The format for the device address selection is shown in Figure 2. A logical 1 is specified when no jumper lead is installed between the appropriate wire-wrap pin from A3-A12. A logical 0 is specified when a jumper lead is installed.

Interrupt Control Logic

The interrupt control provides the circuits necessary to allow a program interrupt transaction between the bus and device. Two interrupt channels (A and B) are available to the user, with channel A assigned to the highest priority. Table 2 lists and defines the user-available signals associated with the interrupt control logic.

Table 2 DRV11-P Interrupt Control Logic Signals

Signal	Function
RQST A H	Interrupt Request A. Asserted by device logic and sets the channel A interrupt request flip-flop when the channel A interrupt enable flip-flop is set.
ENB DATA A H	Interrupt Enable A Data. Asserted by device logic and sets the channel A interrupt enable flip-flop when the ENB CLK A signal is asserted.
ENB CLK A	Interrupt Enable A Clock. Asserted by device logic to cause the channel A interrupt enable flip-flop to be set when ENB DATA A signal is asserted.
ENB A ST H	Interrupt Enable A Status. Indicates the status of the channel A interrupt enable flip-flop.
RQST B H	Interrupt Request B. Same as RQST A H signal except controls channel B interrupts.
ENB DATA B H	Interrupt Enable B Data. Same as ENB DATA A H signal except controls channel B interrupts.
ENB CLK B	Interrupt Enable B Clock. Same as ENB CLK A signal except controls channel B interrupts.
ENB B ST H	Interrupt Enable B Status. Same as ENB A ST H except controls channel B interrupts.
VECTOR H	Interrupt Vector Gate. Used by device logic to gate vector address onto the bus and to generate BRPLY signal.
VEC RQST H	Vector Request. Asserted by device logic to specify that channel A vector address is required; negated to specify channel B vector address is required.
INIT O L	Initialize Out. Buffered BINIT L signal from bus used for general initialization.

Device Address Comparator

The device address comparator (Figure 1, sheet 1) receives address bits D03 H-D12 H from the bus transceivers and compares these bits to the device address assignment bits (A03-A12) wired by the user on the DRV11-P module. If the two addresses compare, an ENB H signal is applied to the protocol logic. The device address comparator logic is designed around two type 8136 ICs. The user's device address is selected by means of wire-wrap pins. Wire-wrapping a device address pin to a ground pin makes that device address bit a zero. Device address bits which are to be ones are left unwrapped. These bits will be pulled up to +5V (one state) via resistors on the module.

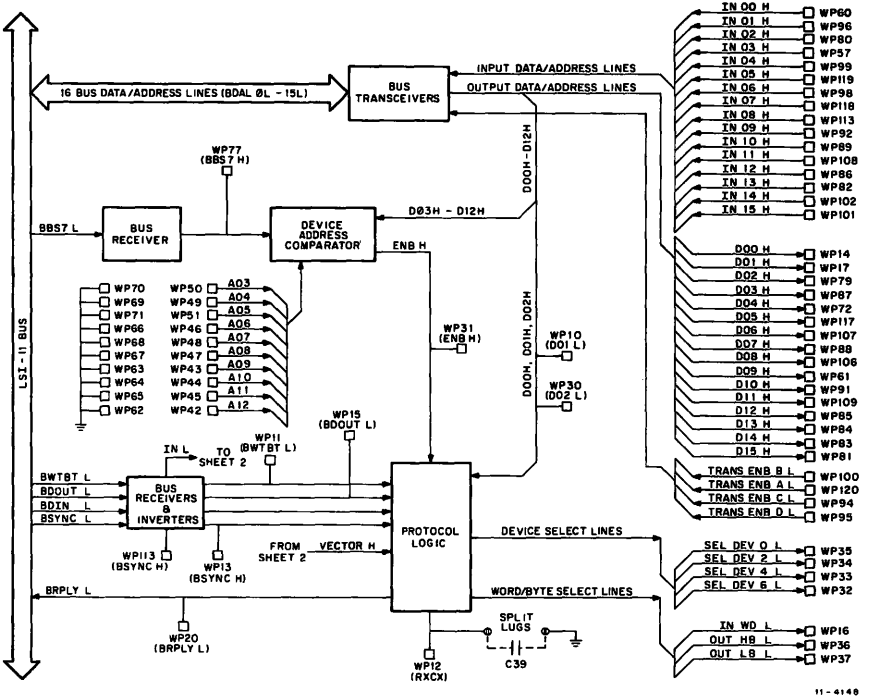


Figure 1 DRV11-P Block Diagram (Sheet 1 of 2)

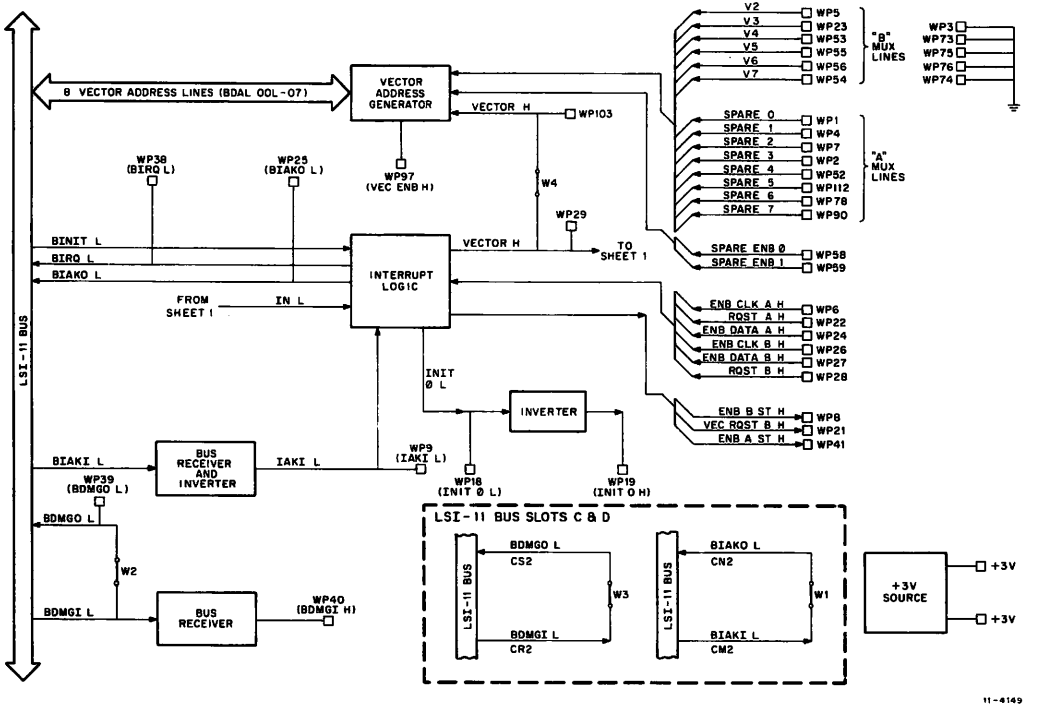


Figure 1 DRV11-P Block Diagram (Sheet 2 of 2)

Bus Transceivers

Referring to Figure 1, sheet 1, data output lines D00 through D15 reflect the state of the bus DBAL lines and will contain address and data information for any bus transfer, regardless of the device involved. Output data are usually clocked into a register for use by the interface or a peripheral since the length of time that the data are available on the bus during the bus cycle is very short. The device address comparator and the protocol logic determine if the data currently on the D00-D15 lines are intended for the DRV11-P.

Input data present at the IN00-IN15 lines will be applied to the bus when the TRANS ENB A, B, C, and D lines are asserted low. These lines are asserted by the protocol logic to gate data onto the bus at the proper time during a bus cycle when the data are addressed by the processor. The SEL DEV and IN WD lines would be driven by the protocol logic to select a user's register. The bus transceivers consist of four type 8641 ICs.

Protocol Logic

The protocol logic (Figure 1, sheet 1) functions as a register selector, providing the signals necessary to control data flow into and out of up to four user registers (eight bytes). Designed around a special DIGITAL IC (DC004), the protocol logic operates as follows: when the proper device address has been decoded by the device address comparator, ENB H goes high, and is applied to a latch in the protocol logic. Address bits D01 H and D02 H are decoded by the protocol logic, producing one of the SEL DEV outputs, while bit D00 H and BWTBT are decoded for output word/byte selection (OUT HB L, OUT LB L). The device select lines (SEL DEV 0L, 2L, 4L, 6L) and word/byte select lines (IN WD L, OUT HB L, OUT LB L) are for user application and are available at wire-wrap pins (WP). Table 3 lists and defines the wire-wrap pins associated with the protocol logic. Generally, each DEV SEL output is used to select one of four user's registers, and the word/byte lines are used to determine the type of transfer (word or byte) to or from these registers. The active state of the user's lines from the protocol logic is a low assertion and the lines are TTL-compatible. The DEV SEL lines can sink up to 20 mA. Split lugs are provided on the DRV11-P to accommodate C37. This capacitor may be installed by the user to vary the delay between BDIN L, BDOUT L, and VECTOR H inputs and the BRPLY output.

The BRPLY L signal is normally issued within 85 ns (max.) of receiving either BDIN L or BDOUT L, depending on the bus cycle. If the user's interface requires more time before ending the bus cycle, the BRPLY L

signal can be delayed up to a maximum of 10 μs by adding capacitor C37 across the split lugs in the BRPLY delay circuit.

The BRPLY L signal is also issued as the result of a signal on the VECTOR H input. This is used when transmitting the vector during an interrupt sequence.

Interrupt Logic

The interrupt logic (Figure 1, sheet 2) performs an interrupt transaction that uses the daisy-chain type arbitration scheme to assign priorities to peripheral devices. The DRV11-P interrupt logic has two channels (A and B) for generating two interrupt requests. Channel A has higher priority than channel B. If a user's device wants control of the LSI-11 bus, the interrupt enable flip-flop within the interrupt logic must first be set. This is accomplished by asserting (logical 1) the ENB DATA line and then clocking the enable flip-flop by asserting (positive transition) the ENB CLK line. With the interrupt enable flip-flop set, the user's device may then make a bus request by asserting (logical 1) RQST. When RQST is asserted, and if the interrupt enable flip-flop is set, the interrupt logic asserts (logical 0) BIRQ L, thus making a bus request. When the request is granted, the processor asserts (logical 0) BDIN L (Figure 1, sheet 1), which is applied to the interrupt logic as IN L (Figure 1, sheet 2). IN L causes the interrupt logic to assert (logical 1) VECTOR H, which is applied to the vector generator. A vector is thus placed on the LSI-11 bus to indicate the starting address of the service routine for the user's device which made the bus request.

As mentioned previously, two interrupt request channels (A and B) are contained within the interrupt logic. These channels can be used to service two user devices. However, because channel A has a higher priority than channel B, fast peripheral devices which cannot recover data if not serviced promptly should use channel A.

There are three status lines from the DRV11-P interrupt logic available to the user. These are: ENB B ST H, ENB A ST H, and VEC RQST B H. ENB B ST H and ENB A ST H indicate the status of the interrupt logic interrupt enable flip-flops. Each line is asserted (logical 1) when the appropriate enable flip-flop is set. The VEC RQST B line is asserted (logical 1) when the user's device connected to channel B has been granted use of the bus. When VEC RQST B is unasserted (logical 0), the user's device connected to channel A of the interrupt logic has been granted use of the bus. These status lines can function as part of the user's control and status register (CSR), which can be constructed on the DRV11-P module. Additionally, the INIT 0 and INIT 0 H outputs from the interrupt logic can be used to initialize the user's logic.

Interrupt Vector Generator

The interrupt vector generator (Figure 1, sheet 2) produces a vector which points to a location in memory containing the address of a service routine for the user's device-requesting interrupt service. The interrupt vector is selected by the user by means of wire-wrap pins on the DRV11-P. Vector bits V3 through V7 are hard-wired by the user for either logical 1s or 0s. Wire-wrapping an interrupt vector pin to a ground pin makes that vector bit a 0. Vector bits which are to be 1s are left unwrapped. These bits will be pulled up to +5V ("one" state) via resistors on the DRV11-P. When VECTOR H from the interrupt logic goes high (logical 1), eight vector bits are gated onto the LSI-11 bus. It should be noted that the user can generally select the state of only six of the eight vector bits. The remaining bits, V00 and V01, are preset by the DRV11-P vector generator. With this arrangement, the user can select an interrupt vector in the normal user range of 0 to 374_8. However, by adding one gate to the interrupt vector generator encode logic, the user can accommodate nine bits in the vector and thus extend the interrupt to 774_8.

The interrupt vector generator is primarily designed around two type 74157 multiplexer ICs. Each 74157 has two separate 4-bit inputs which are multiplexed. Thus, both 74157s can accommodate two 8-bit bytes, one of which is used for vector generation. This leaves one spare 8-bit input for user application. The spare input can be used to gate onto the bus the lower byte of the user's CSR on the DRV11-P. The data on the spare input can be gated to the LSI-11 bus by driving both SPARE ENB 0 and SPARE ENB 1 inputs low (logical 0). This is best accomplished by using one of the SEL DEV lines from the protocol logic (Figure 1, sheet 1) along with the IN WD line. The actual use of the spare inputs is at the user's discretion, but SPARE ENB 0 and SPARE ENB 1 should not be permanently held low as this could affect the interrupt vector. If not used, these inputs should be connected to the +3V source.

Interrupt Vector Selection

As manufactured, the DRV11-P can generate vectors in the range from 0-374_8. However, by adding one gate to the DRV11-P vector generation logic, the user can extend the vector to 774_8. The user selects the interrupt vector by means of wire-wrap pins on the DRV11-P module.

Figure 4 shows the vector select format and presents the wire-wrap pin-to-bit relationship for vector selection. Bits to be decoded as zero

bits in the interrupt vector are wire-wrapped to ground wire-wrap pins. Bits to be decoded as one bits are left unwrapped, as these bits are pulled up to the one state.

It is recommended that WP5 (vector bit 2) be wrapped to WP21 (VEC RQST B H). This will automatically decode the least significant bit of the interrupt vector as a 0 or a 4. When the VECTOR H signal is issued as a result of the B half of the interrupt logic becoming bus master, the VEC RQST B H (WP5) signal is also issued, changing bit 2 of the interrupt vector, thus presenting a different vector for interrupt B.

The VEC RQST B H line can be thought of as a one-bit code indicating which half of the interrupt logic is bus master. When bit 2 of the interrupt vector is a zero, the A half is bus master; a one indicates that the B half is master.

Bus Receivers

All LSI-11 bus data and control lines are fully buffered on the DRV11-P module. Buffering for the data and address lines (BDAL) is accomplished by the bus transceivers. Bus control lines (BWTBT, BDOUT, BDIN, BSYNC, BBSY, BIAKI, and BDMGI) are buffered on the DRV11-P with type 8640 bus receivers. These receivers are high-impedance receivers with the following input levels:

High = 1.7 V min.
Low = 1.3 V max.

The receivers have standard TTL-compatible outputs which are made available (for most bus signals) to the user by means of wire-wrap pins.

+3V Source

There are two +3V wire-wrap pins on the DRV11-P module. These pins provide a source of +3V for pulling up unused TTL inputs. Each +3V source is capable of driving up to 13 TTL unit loads. The +3V sources are derived from resistor dividers placed across the +5V logic source.

Wire-Wrap Pins

There are 112 user I/O lines and 122 wire-wrap pins (not counting the 40 pins for the I/O connector and the 70 pins for C and D module fingers) for user applications. The locations and functions of these pins are described in detail in Table 5.

CONFIGURATION

General

The DRV11-P (Figure 2) is a versatile wire-wrap module that contains interface logic for operation with the LSI-11 bus and provides adequate board area for mounting and connecting integrated circuits (ICs) or discrete components. Because the bus interface logic is included, the module can be efficiently configured by the user to satisfy a variety of device interface logic applications.

A 40-pin connector mounted at the board edge connects to a device through several cable assembly types available from DIGITAL.

Except for the bus interface connections, all signals and voltages are terminated to wire-wrap pins for user connections. The bus control logic is provided with wire-wrap test points for monitoring the internal signals. The test points are spaced at 0.254 cm (0.1 in.) between pins to let 40-pin connectors, be inserted over the wire-wrap pins for automated test functions.

Approximately two-thirds of the surface area on the module consists of plated-through holes, each connected to a wire-wrap pin. The user can mount three different types of dual-in-line ICs or a variety of discrete components into the holes and connect the proper voltages and signals by wire-wrapping leads on the board.

Device Address Selection

The DRV11-P will respond to up to four consecutive addresses in the bank 7 area (addresses between 160000_8 and 177776_8). The register addresses are sequential by even numbers and are as follows.

Register	BBS7	Octal Address
1	1	16XXX0
2	1	16XXX2
3	1	16XXX4
4	1	16XXX6

The user selects a base ending in zero for assignment to the first register by means of wire-wrap pins on the DRV11-P module. The module decodes this base address and the remaining register addresses are then properly decoded by the DRV11-P as they are received from the LSI-11 bus.

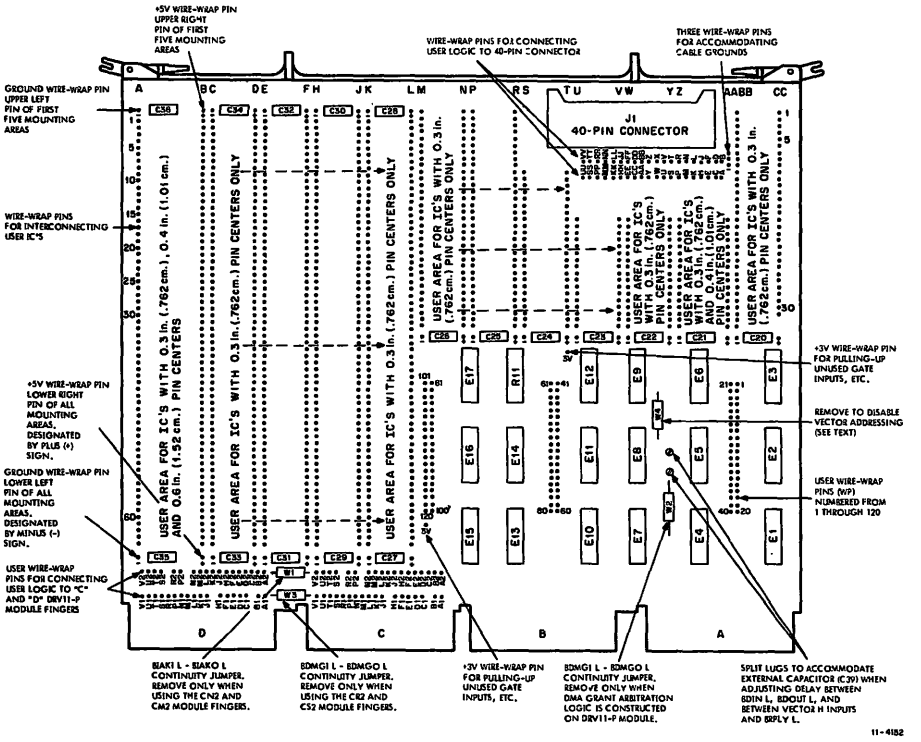


Figure 2 DRV11-P Component Mounting Locations

Figure 3 shows the address select format and presents the wire-wrap pin-to-bit relationship for device address selection. Bits to be decoded as 0 bits in the base address are wire-wrapped to ground wire-wrap pins (WP). Bits to be decoded as 1 bits are left unwrapped as these bits are pulled up to the 1 state.

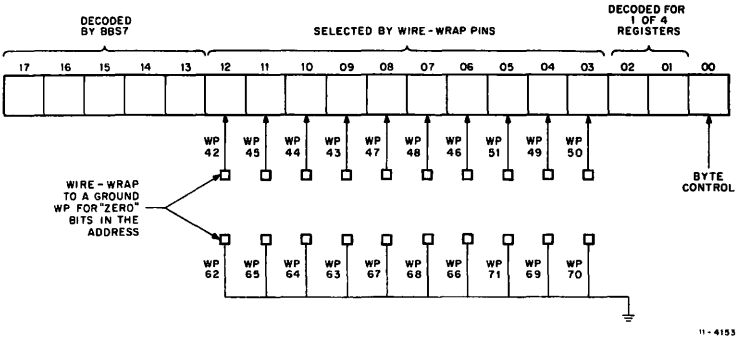


Figure 3 DRV11-P Device Address Select Format

Interrupt Vector Logic — The interrupt vector logic is used in conjunction with the interrupt control logic to generate a vector on bus lines BDAL 00 L-BDAL 07 L. The interrupt vector is specified by the user and selected by installing jumper leads between wire-wrap pins on the M7948 module. The vectors available are from 0 to 374_8. The vector range can be increased from 0 to 774_8 with additional logic and wiring.

When the VECTOR H signal is asserted as a result of a device interrupt request, the interrupt vector is placed on the bus lines.

Wire-wrap pins V3 through V7 are used to assign the vector bits. A jumper lead installed selects a logical 0 address bit for its associated line and no lead selects a logical 1 address bit according to the format in Figure 4.

Bit BDAL 02 L can be connected to the device interrupt request RQST A signal to specify a separate vector address for channel A and channel B.

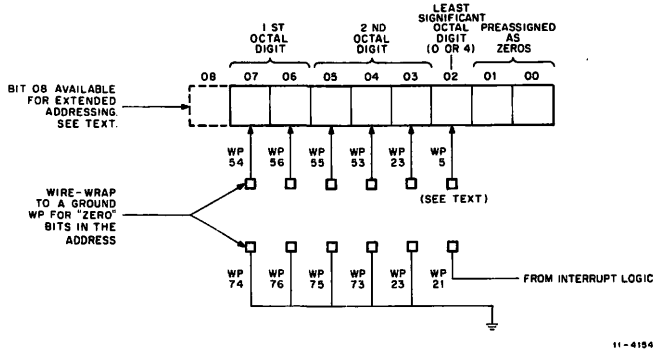


Figure 4 DRV11-P Vector Selection

Status and control information can be multiplexed through the same logic used to generate the vector address. Up to eight status and control bits can be assigned by the user and transferred to bus lines BDAL 00 L-BDAL 07 L. The information can be gated onto the bus lines using a select level generated by the address decoding logic.

Component Mounting Area

General — Twelve vertical areas (A-L) are available on the M7948 module for mounting integrated circuits or discrete components as shown on Figure 2. Each area has a double row of wire-wrap pins that connect to an associated plated-through hole located at 0.254 cm (0.1 in.) vertical spacing. Area A is for multi-use and is capable of accepting ICs with pin centers at 0.762 cm (0.3 in.), 1.01 cm (0.4 in.), or 1.52 cm (0.6 in.). Area K will also accept ICs with pin centers at 0.762 cm or 1.01 cm. All remaining areas will accept only ICs with pin centers at 0.762 cm.

Table 3 lists the total number of ICs with 0.762 cm spacing that can be mounted in the user areas A through L of the module.

Table 3 DRV11-P IC Mounting Area

IC Type	Total Number
14-pin	60
16-pin	52
18-pin	44
20-pin	44

Connector Wire Wrap Pins — The 36 contact pins in rows C and D at the edge of the module connect to a double row of wire-wrap pins. These two rows are made available to the user for connecting signals and voltages from the backplane to the user-installed logic circuits. The following pins of rows C and D are normally dedicated to +5V and GND.

The user can connect the power to the IC or components using the row C and row D wire-wrap pins.

+5V	CA2, DA2
GND	CJ1, CM1, CT1
	DJ1, DM1, DT1
	CC2, DD2

Device Signals — Input and output data and status and control signals can be transferred between the device and the DRV11-P module using any one of several cable assemblies listed in Table 4 and available from DIGITAL. One end of each cable is terminated with a 40-pin female connector which mates with the 40-pin male connector J1 mounted on the M7948 module. The pins of J1 connect to the user-installed logic through a series of wire-wrap pins.

Table 4 Recommended Cable Assemblies

Cable No.	Connectors	Type	Length (XX)
BC07A-XX	H856 to open end	20-twisted pair	10, 15, 25
BC07D-XX	H856 to open end	2, 20-conductor ribbon	10, 15, 25
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12 20, 25, 50, 75, 100
BC04Z-XX	H856 to open end	Shielded flat	6, 10, 15, 25, 50

User Pin Selection

The DRV11-P provides many wire-wrap pins for the user to select that will assist him in determining his configuration. These pins and their functions are listed in Table 5.

Table 5 User Wire-Wrap Pins

Wire-Wrap Pin: WP1 **Mnemonic:** SPARE 0
Function: Spare input to the vector address multiplexer. This input can be used to read part of a control/status register.

Wire-Wrap Pin: WP2 **Mnemonic:** SPARE 3
Function: See WP1.

Wire-Wrap Pin: WP3 **Mnemonic:**
Function: Ground for vector address bit V3. See WP23.

Wire-Wrap Pin: WP4 **Mnemonic:** SPARE 1
Function: See WP1.

Wire-Wrap Pin: WP5 **Mnemonic:** V2
Function: Vector address bit 2.

Wire-Wrap Pin: WP6 **Mnemonic:** ENB CLK A H
Function: ENB CLK A H is the clock input to the enable A flip-flop of the A interrupt logic. When ENB CLK A H goes high, ENB DATA A is clocked into the enable A flip-flop.

Wire-Wrap Pin: WP7 **Mnemonic:** SPARE 2
Function: See WP1.

Wire-Wrap Pin: WP8 **Mnemonic:** ENB B ST H
Function: ENB B ST H is the status output from the enable B flip-flop of the B interrupt logic. When ENB B ST H is high, the enable B flip-flop is set.

Wire-Wrap Pin: WP9 **Mnemonic:** IAKI L
Function: Test point for the BIAKI bus signal. BIAKI L is the processor's response to BIRQ L and is daisy-chained such that the first requesting device blocks the signal propagation. Non-requesting devices pass the signal on as BIAKO L. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device.

Wire-Wrap Pin: WP10 **Mnemonic:** D01 L
Function: Test point for data/address bit 1. Useful when testing the protocol logic. D01 is latched in the protocol logic at the asserted edge of BSYNC L. D01 and D02 are decoded to produce the SEL DEV outputs.

Wire-Wrap Pin: WP11 **Mnemonic:** BWTBT L
Function: Test point for the BWTBT bus signal; while BDOUT L is asserted, BWTBT L indicates a byte or word operation: BWTBT L asserted indicates byte operation; BWTBT L unasserted

indicates word operation. BWTBT L decoded with BDOUT L and BDAL 0 L forms OUT LB L or OUT HB L.

Wire-Wrap Pin: WP12 **Mnemonic:** $R_X C_X$
Function: Test point for monitoring the delay of BRPLY.

Wire-Wrap Pin: WP13 **Mnemonic:** BSYNC H
Function: Test point for the BSYNC L bus signal. BSYNC L indicates that the address is valid. At the assertion of BSYNC L, address information is trapped in four latches. While unasserted, disables all outputs except the vector term of BRPLY L. BSYNC L is held throughout the entire bus cycle.

Wire-Wrap Pin: WP14 **Mnemonic:** D00 H
Function: One of 16 data or address lines from the transceivers for user applications. Address bit 0 is used for byte selection: 0 = low byte; 1 = high byte.

Wire-Wrap Pin: WP15 **Mnemonic:** BDOUT L
Function: Test point for the BDOUT L bus signal. BDOUT L is a strobe signal to effect a data output transaction. BDOUT L is decoded with BWTBT L and BDAL0 to form OUT LB L and OUT HB L. BDOUT L also causes BRPLY L to be issued through the delay circuit.

Wire-Wrap Pin: WP16 **Mnemonic:** IN WD L
Function: In word (IN WD) is used to gate input data from a selected register onto the LSI-11 bus. Enabled by BSYNC L and strobed by BDIN L.

Wire-Wrap Pin: WP17 **Mnemonic:** D01 H
Function: One of 16 data or address lines from the transceivers for user applications.

Wire-Wrap Pin: WP18 **Mnemonic:** INIT 0 L
Function: An initialize signal (asserted low) for user applications.

Wire-Wrap Pin: WP19 **Mnemonic:** INIT 0 H
Function: An initialize signal (asserted high) for user applications.

Wire-Wrap Pin: WP20 **Mnemonic:** BRPLY L
Function: Test point for the BRPLY L bus signal. BRPLY L is generated by VECTOR H (vector term) or by BSYNC and ENB in combination with either BDIN L or DBOUT L. Capacitor C37 can be added by the user to extend the delay.

Wire-Wrap Pin: WP21 **Mnemonic:** VEC RQST B H
Function: Used to distinguish whether device A or device B is making a request. VECT RQST B H is asserted for device B requests and unasserted for device A requests.

Wire-Wrap Pin: WP22 **Mnemonic:** RQST A H
Function: When RQST A H is asserted, the bus request flip-flop is enabled, and BIRQ L becomes asserted if the interrupt enable flip-flop is set.

Wire-Wrap Pin: WP23 **Mnemonic:** V3
Function: Vector address bit 3. WP23 is used to select the state of vector address bit 3. When not wrapped to a ground pin, vector address bit 3 is a 1. When wrapped to WP3, vector address bit 3 is a 0.

Wire-Wrap Pin: WP24 **Mnemonic:** ENB DATA A H
Function: Interrupt enable A data line. The level on this line, in conjunction with the ENB CLK A H (see WP6) line, determines the state of the A interrupt enable flip-flop within the interrupt logic.

Wire-Wrap Pin: WP25 **Mnemonic:** BIAKO L
Function: Test point for the BIAKO L bus signal. BIAKO L is the daisy-chained signal that is passed by all devices not requesting interrupt service (see WP9).

Wire-Wrap Pin: WP26 **Mnemonic:** ENB CLK B H
Function: ENB CLK B H is the clock input to the enable B flip-flop of the B interrupt logic. When ENB CLK B H goes high, ENB DATA B is clocked into the enable B flip-flop.

Wire-Wrap Pin: WP27 **Mnemonic:** ENB DATA B H
Function: Interrupt enable B data line. The level on this line, in conjunction with the ENB CLK B H (see WP26) lines, determines the state of the B interrupt enable flip-flop within the interrupt logic.

Wire-Wrap Pin: WP28 **Mnemonic:** RQST B H
Function: When RQST B H is asserted, the bus request flip-flop for device B in the interrupt logic is enabled, and BIRQ L becomes asserted if the interrupt enable flip-flop is set.

Wire-Wrap Pin: WP29 **Mnemonic:** VECTOR H
Function: Test point for VECTOR H. This signal causes BRPLY L (vector term) to be generated through a delay independent of BSYNC L and ENB H. VECTOR H also gates the vector address onto the LSI-11 bus via the vector address generator.

Wire-Wrap Pin: WP30 **Mnemonic:** D02 L
Function: Test point for data/address bit 2. Useful when testing the protocol logic. D02 is latched at the asserted edge of BSYNC L. D02 and D01 are decoded to produce the SEL DEV outputs.

Wire-Wrap Pin: WP31 **Mnemonic:** ENB H
Function: Test point for ENB H. This signal is the result of a compare between the device address on the LSI-11 bus and the device address established by the user. When the addresses compare, ENB H is asserted and sent to the protocol logic.

Wire-Wrap Pin: WP32 **Mnemonic:** SEL DEV 6 L
Function: One of four select signals that is true as a function of BDAL1 L and BDAL2 L if ENB H (see WP31) is asserted at the asserted edge of BSYNC L. The four select signals indicate that a user's register has been selected for a data transaction. The select signals remain asserted until BSYNC L becomes unasserted.

Wire-Wrap Pin: WP33 **Mnemonic:** SEL DEV 4 L
Function: See WP32.

Wire-Wrap Pin: WP34 **Mnemonic:** SEL DEV 2 L
Function: See WP32.

Wire-Wrap Pin: WP35 **Mnemonic:** SEL DEV 0 L
Function: See WP32.

Wire-Wrap Pin: WP36 **Mnemonic:** OUT LB L
Function: Out low byte is used to load (write) data into the low byte of a selected user register. See WP37.

Wire-Wrap Pin: WP37 **Mnemonic:** OUT HB L
Function: Out high byte is used to load (write) data into the high byte of a selected user register. If used with OUT LB L, the higher, lower, or both bytes can be written. OUT HB L is enabled by BSYNC L and the decode of BWTBT L and BDAL0 L, and strobed by BDOUT L.

Wire-Wrap Pin: WP38 **Mnemonic:** BIRQ L
Function: Test point for the BIRQ L bus signal. This signal is asserted by a device needing interrupt service.

Wire-Wrap Pin: WP39 **Mnemonic:** BDMGO L
Function: This signal is generated by DMA devices as a result of arbitrating the BDMGI L line. Jumper W2 must be removed if the DRV11-P is to be used for DMA service.

Wire-Wrap Pin: WP40 **Mnemonic:** BDMGI H
Function: Used as a source for the BDMGI signal to drive the user's DMA request arbitration logic. See WP39.

Wire-Wrap Pin: WP41 **Mnemonic:** ENB A ST H
Function: ENB A ST H is the status output from the enable A flip-flop of the A interrupt logic. When ENB A ST H is high, the enable A flip-flop is set.

Wire-Wrap Pin: WP42 **Mnemonic:** A12
Function: Used to select the user's device address along with WP45, 44, 43, 47, 48, 46, 51, 49, 50. When not wrapped to a ground pin, the particular device address bit will be a 1. When wrapped to a ground pin (WP62 for bit A12), the particular bit will be a 0.

Wire-Wrap Pin: WP43 **Mnemonic:** A09
Function: User's device address bit 9. The associated ground pin is WP63. See WP42.

Wire-Wrap Pin: WP44 **Mnemonic:** A10
Function: User's device address bit 10. The associated ground pin is WP64. See WP42.

Wire-Wrap Pin: WP45 **Mnemonic:** A11
Function: User's device address bit 11. The associated ground pin is WP65. See WP42.

Wire-Wrap Pin: WP46 **Mnemonic:** A06
Function: User's device address bit 6. The associated ground pin is WP66. See WP42.

Wire-Wrap Pin: WP47 **Mnemonic:** A08
Function: User's device address bit 8. The associated ground pin is WP67. See WP42.

Wire-Wrap Pin: WP48 **Mnemonic:** A07
Function: User's device address bit 7. The associated ground pin is WP68. See WP42.

Wire-Wrap Pin: WP49 **Mnemonic:** A04
Function: User's device address bit 4. The associated ground pin is WP69. See WP42.

Wire-Wrap Pin: WP50 **Mnemonic:** A03
Function: User's device address bit 3. The associated ground pin is WP70. See WP42.

Wire-Wrap Pin: WP51 **Mnemonic:** A05
Function: User's device address bit 5. The associated ground pin is WP71. See WP42.

Wire-Wrap Pin: WP52 **Mnemonic:** SPARE 4
Function: See WP1.

Wire-Wrap Pin: WP53 **Mnemonic:** V4
Function: Vector address bit 3. The associated ground pin is WP73. See WP23.

Wire-Wrap Pin: WP54 **Mnemonic:** V7
Function: Vector address bit 7. The associated ground pin is WP74. See WP23.

Wire-Wrap Pin: WP55 **Mnemonic:** V5
Function: Vector address bit 5. The associated ground pin is WP75. See WP23.

Wire-Wrap Pin: WP56 **Mnemonic:** V6
Function: Vector address bit 6. The associated ground pin is WP76. See WP23.

Wire-Wrap Pin: WP57 **Mnemonic:** IN03 H
Function: One of 16 data or address lines to the transceivers for user applications.

Wire-Wrap Pin: WP58 **Mnemonic:** SPARE ENB 0
Function: SPARE ENB 0 and SPARE ENB 1 (WP59) both must be driven low to write data from SPARE inputs 0 through 7 to the LSI-11 bus via the transceiver. For 8-bit input applications, SPARE ENB 0 could be driven by one of the SEL DEV lines, while SPARE ENB 1 could be driven by IN WD L.

Wire-Wrap Pin: WP59 **Mnemonic:** SPARE ENB 1
Function: See WP58.

Wire-Wrap Pin: WP60 **Mnemonic:** IN00 H
Function: See WP57.

Wire-Wrap Pin: WP61 **Mnemonic:** D09 H
Function: See WP17.

Wire-Wrap Pin: WP62 **Mnemonic:**
Function: Ground for user's device address bit A12. See WP42.

Wire-Wrap Pin: WP63 **Mnemonic:**
Function: Ground for user's device address bit A09. See WP42.

Wire-Wrap Pin: WP64 **Mnemonic:**
Function: Ground for user's device address bit A10. See WP42.

Wire-Wrap Pin: WP65 **Mnemonic:**
Function: Ground for user's device address bit A11. See WP42.

Wire-Wrap Pin: WP66 **Mnemonic:**
Function: Ground for user's device address bit A06. See WP42.

Wire-Wrap Pin: WP67 **Mnemonic:**
Function: Ground for user's device address bit A08. See WP42.

Wire-Wrap Pin: WP68 **Mnemonic:**
Function: Ground for user's device address bit A07. See WP42.

Wire-Wrap Pin: WP69 **Mnemonic:**
Function: Ground for user's device address bit A04. See WP42.

Wire-Wrap Pin: WP70 **Mnemonic:**
Function: Ground for user's device address bit A03. See WP42.

Wire-Wrap Pin: WP71 **Mnemonic:**
Function: Ground for user's device address bit A05. See WP42.

Wire-Wrap Pin: WP72 **Mnemonic:** D04 H
Function: See WP17.

Wire-Wrap Pin: WP73 **Mnemonic:**
Function: Ground for vector address bit V4. See WP23.

Wire-Wrap Pin: WP74 **Mnemonic:**
Function: Ground for vector address bit V5. See WP23.

Wire-Wrap Pin: WP75 **Mnemonic:**
Function: Ground for vector address bit V6. See WP23.

Wire-Wrap Pin: WP76 **Mnemonic:**
Function: Ground for vector address bit V7. See WP23.

Wire-Wrap Pin: WP77 **Mnemonic:** BBS7 H
Function: Test point for the bank 7 select (BBS7) bus signal. This line is asserted by the bus master when an address in the upper bank is placed on the LSI-11 bus.

Wire-Wrap Pin: WP78 **Mnemonic:** SPARE 6
Function: See WP1.

Wire-Wrap Pin: WP79 **Mnemonic:** D02 H
Function: See WP17.

Wire-Wrap Pin: WP80 **Mnemonic:** IN 02 H
Function: See WP57.

Wire-Wrap Pin: WP81 **Mnemonic:** D15 H
Function: See WP17.

Wire-Wrap Pin: WP82 **Mnemonic:** IN 13 H
Function: See WP57.

Wire-Wrap Pin: WP83 **Mnemonic:** D14 H
Function: See WP17.

Wire-Wrap Pin: WP84 **Mnemonic:** D13 H
Function: See WP17.

Wire-Wrap Pin: WP85 **Mnemonic:** D12 H
Function: See WP17.

Wire-Wrap Pin: WP86 **Mnemonic:** IN 12 H
Function: See WP57.

Wire-Wrap Pin: WP87 **Mnemonic:** D03 H
Function: See WP17.

Wire-Wrap Pin: WP88 **Mnemonic:** D07 H
Function: See WP17.

Wire-Wrap Pin: WP89 **Mnemonic:** IN 10 H
Function: See WP57.

Wire-Wrap Pin: WP90 **Mnemonic:** SPARE 7
Function: See WP1.

Wire-Wrap Pin: WP91 **Mnemonic:** D10 H
Function: See WP17.

Wire-Wrap Pin: WP92 **Mnemonic:** IN 09 H
Function: See WP57.

Wire-Wrap Pin: WP93 **Mnemonic:**
Function: Not used.

Wire-Wrap Pin: WP94 **Mnemonic:** TRANS ENB C L
Function: Enables user's data to be placed onto the LSI-11 bus. Both TRANS ENB C and A (WP94 and WP120) and TRANS

ENB D and B (WP95 and WP100) must be driven low prior to the processor's read data time.

Wire-Wrap Pin: WP95 **Mnemonic:** TRANS ENB D L
Function: See WP94.

Wire-Wrap Pin: WP96 **Mnemonic:** IN 01 H
Function: See WP57.

Wire-Wrap Pin: WP97 **Mnemonic:** VEC ENB H
Function: Test point for VEC ENB H. This signal gates the vector to the LSI-11 bus, provided that jumper W4 has not been removed. WP97 can be used as the source for VEC ENB H when adding an additional gate to the DRV11-P for vector expansion up to 774_8.

Wire-Wrap Pin: WP98 **Mnemonic:** IN 06 H
Function: See WP57.

Wire-Wrap Pin: WP99 **Mnemonic:** IN 04 H
Function: See WP57.

Wire-Wrap Pin: WP100 **Mnemonic:** TRANS ENB B L
Function: See WP94.

Wire-Wrap Pin: WP101 **Mnemonic:** IN 15 H
Function: See WP57.

Wire-Wrap Pin: WP102 **Mnemonic:** IN 14 H
Function: See WP57.

Wire-Wrap Pin: WP103 **Mnemonic:**
Function: Used to pull up the VEC ENB H line when jumper W4 is removed.

Wire-Wrap Pin: WP104 **Mnemonic:**
Function: Not used.

Wire-Wrap Pin: WP105 **Mnemonic:**
Function: Not used.

Wire-Wrap Pin: WP106 **Mnemonic:** D08 H
Function: See WP17.

Wire-Wrap Pin: WP107 **Mnemonic:** D06 H
Function: See WP17.

Wire-Wrap Pin: WP108 **Mnemonic:** IN 11 H
Function: See WP57.

Wire-Wrap Pin: WP109 **Mnemonic:** D11 H
Function: See WP17.

Wire-Wrap Pin: WP110 **Mnemonic:**
Function: Not used.

Wire-Wrap Pin: WP111 **Mnemonic:**
Function: Not used.

Wire-Wrap Pin: WP112 **Mnemonic:** SPARE 5
Function: See WP1.

Wire-Wrap Pin: WP113 **Mnemonic:** IN 08 H
Function: See WP57.

Wire-Wrap Pin: WP114 **Mnemonic:**
Function: Not used.

Wire-Wrap Pin: WP115 **Mnemonic:** BSYNC H
Function: Test point for BSYNC H. At the asserted edge of this signal, address information is trapped in four latches. BSYNC H is the inversion of BSYNC L. See WP13.

Wire-Wrap Pin: WP116 **Mnemonic:**
Function: Not used.

Wire-Wrap Pin: WP117 **Mnemonic:** D05 H
Function: See WP17.

Wire-Wrap Pin: WP118 **Mnemonic:** IN 07 H
Function: See WP57.

Wire-Wrap Pin: WP119 **Mnemonic:** IN 05 H
Function: See WP57.

Wire-Wrap Pin: WP120 **Mnemonic:** TRANS ENB A L
Function: See WP94.

Wire-Wrap Pin: +3V **Mnemonic:**
Function: There are two +3V source wire-wrap pins on the DRV11-P. Each +3V source can drive up to 13 TTL unit loads. These sources can be used for pulling up unused TTL inputs.

DUV11 LINE INTERFACE

GENERAL

The DUV11 line interface is a buffered, program-controlled, single-line communications interface device which is used to establish a data communications line between any LSI-11 bus and a Bell 201 synchronous modem or the equivalent. The module is fully programmable with respect to sync characters, character length (5 to 8 bits), and parity selection. The DUV11 provides serial-to-parallel and parallel-to-serial data communications, buffers TTL-to-EIA voltage levels and EIA-to-TTL voltage levels, and controls the modem for half- or full-duplex operation.

FEATURES

- Interfaces synchronous and isochronous communications data
- Supports bisynchronous communications data
- Interface signals meet EIA RS-232C standard
- Operates in full-duplex or half-duplex modes
- Maximum baud rate is 19.2K baud
- Uses variable length characters (5, 6, 7, or 8 bits plus parity)
- Generates odd or even parity bits that are transmitted with the data character to the modem
- Verifies received character parity
- Inhibits transmitter output for maintenance purposes
- Provides control signals to the modem and monitors the modem status lines
- Establishes synchronization prior to receiving data
- Generates program interrupt requests

SPECIFICATIONS

Identification	M7951
Size	Quad
Power	+5 Vdc ±5% at 0.86A +12 Vdc ±3% at 0.32A
Bus Loads	
AC	1
DC	1

DUV11

DESCRIPTION

General

The DUV11 interface module comprises six functions that control the data flow between an LSI-11 bus and a Bell 201 modem or the equivalent. The major functions, shown in Figure 1, are address comparator/command decoder, data multiplexer, modem interface logic, receiver logic, transmitter logic, and interrupt control logic. The address comparator provides addressable access to the LSI-11 bus and the command decoder receives its control from the LSI-11 bus via the address comparator and direct connections. The data multiplexer receives status data from the modem interface logic, the receiver logic, and the transmitter logic. It also controls the data and status information to the transceivers which is output to the LSI-11 bus. The modem interface logic converts the TTL logic levels to the EIA voltage levels required by the Bell 201 modem. It also contains the transmit data line to the modem and the serial data input line and has access to the modem control signals. The receiver logic accepts the EIA serial input and converts it into parallel data for the LSI-11 bus. The transmitter logic converts the parallel LSI-11 bus data into serial data for transmission over the communications lines. The interrupt control logic enables the DUV11 module to become bus master over the LSI-11 bus by generating a program interrupt to an interrupt address vector.

Address Comparator

The address comparator logic is made up of the bus transceivers and address/vector rocker switches. The rocker switches are set before operating the DUV11. When the processor addresses the DUV11, the bus transceivers compare the preset address with the address on the LSI-11 bus (BDAL 00 through 15). If they compare, the MATCH signal is asserted, which enables the command decoder (DC004 chip). Information then received at the transceivers is passed from the LSI-11 bus to the QDL bus (QDL 00 through 15) under control of the command decoder. Signal INWDB H enables the transceivers to receive data from the Q bus and place that data onto the QDL bus. This signal originates from the Q bus as BDIN L, which is driven to become DIN L. DIN L is applied to the command decoder and is output at INWD L when MATCH is asserted by the address comparator. INWD L is then gated to become INWDB L. Similarly, the signals SEL 0 L, SEL 2 L, and SEL 4 L, which are functions of QDL 00, QDL 01, and QDL 02 when MATCH is asserted to the command decoder, are gated to become EN QDL TO BDAL. This signal enables data from the QDL bus which is applied to the transceivers to pass on to the LSI-11 bus.

During an interrupt sequence, the address comparator circuitry provides passage of the preset interrupt vector address to the LSI-11 bus.

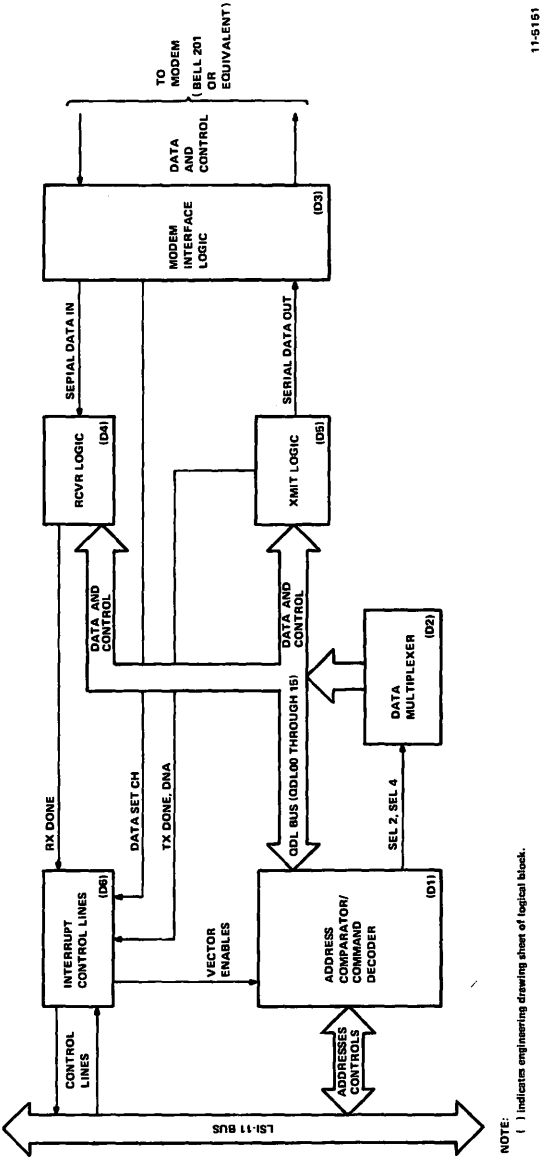


Figure 1 DUV11 Logic Block Diagram

Command Decoder (DC004)
The command decoder logic controls the flow of data into the status registers within the DUV11 and the passage of status information and data back out to the CPU.

The signals that enable the registers of the DUV11, such as LD PARCSR, LD TXDBUF, etc., are generated by gating the outputs of the command decoder. This logic receives bits 0 through 2 from the QDL bus. When the address comparator outputs MATCH, these bus bits cause the command decoder logic to output the proper select signal. For example, if the control logic selector asserts SEL 6 L along with OUTLB L, the resultant gated output is LD TXDBUF (1) L, which causes the transmitter data buffer to load parallel data from the QDL bus.

Data Multiplexer
The data multiplexer controls the passage of DUV11 status signals and data to the bus transceivers for output to the CPU. Two signals, SEL 2 L and SEL 4 L, enable the selection of status signals and data which will pass on to the QDL bus.

Modem Interface Logic
The modem interface logic contains level converters to change the logic level signals to the operating voltage levels of the Bell 201 modem. All logic signals ranging from 2.4V to 3.5V are converted to +6V. All ground (0V) logic signals are converted to −6V.

Receiver Control Logic
The receiver circuitry contains the synchronous/asynchronous receiver chip (SAR) and its supportive logic. Within the SAR, serial data received from the modem are converted to parallel data for output to the QDL bus. Parameter data are supplied via the QDL bus. PARCSR (1) L loads this data into the SAR. Having stored these parameters, the receiver detects the serial received character, accomplishes synchronization, frames the received character, detects errors, raises the RX DONE flag, and holds the framed character (for program reading) until the next character is framed.

Once the RCVR logic is enabled, it operates as programmed. The SCH SYNC input enables the RCVR logic. The contents of the PARCSR determine:

1. Mode of operation (internal synchronous, external synchronous, or isochronous)
2. Length of character to be framed (5, 6, 7, or 8 bits plus parity)

3. Parity (enabled or disabled)
4. Parity sense (odd or even)
5. Sync character configuration

The method of achieving synchronization is the principal difference between the modes of operation.

1. In the internal synchronous mode, two contiguous sync characters must be recognized by the RCVR logic to achieve synchronization. Once synchronization is achieved, the RCVR starts framing on the very next character bit. The received characters must arrive at the RCVR in a continuous serial bit stream or synchronization will be lost.
2. The external synchronous mode is designed for use with communication equipment which accomplishes synchronization external to the DUV11 interface. The external synchronization logic prohibits RCVR operation by inhibiting the assertion of SCH SYNC until synchronization with the XMTR has been achieved. When external synchronization is achieved, SCH SYNC asserts, forcing the RCVR logic to the synchronized state. The RCVR then starts framing immediately, beginning with the next character bit.
3. In the isochronous mode, each received character is preceded by a start bit and succeeded by a stop bit, which serves to synchronize the RCVR. In this mode, the receiver simply does not start framing until it recognizes a start bit. It then frames the character following the start bit and looks for a stop bit. If a stop bit is not detected, the character received is considered invalid, flagged as such, and held for reading by the program. Hence, in the isochronous mode, characters need not be preceded by sync characters and need not arrive contiguously at the RCVR.

The strip synchronization character (STRIP SYNC) input determines whether received sync characters are to be permitted to set the RX DONE flag. If STRIP SYNC is asserted, all sync characters are discarded provided no errors are detected.

Transmitter Control Logic

The transmitter circuitry contains the synchronous/asynchronous transmitter chip (SAT) and its supportive logic. The SAT accepts parallel characters from the program, raises the TX DONE flag to request the next character, and serially outputs the current character to the modem. Before the transmitter operation can begin, the transmitter logic must be initialized and the PARCSR and TXCSR registers programmed.

The high-order bits from the QDL bus are loaded into the XCSR when signal LD TXCSR HB H is asserted. The low-order bits are loaded into the TXCSR when LD TXCSR LB H is asserted. The signal LD PARCSR (1) L asserted enables parameter data into the SAT.

The signal SEND (1) H enables the transmitter logic. Once the transmitter is enabled, it operates as programmed. The contents of the PARCSR determine:

1. Mode of operation (synchronous or isochronous)
2. Length of character to be transmitted (5, 6, 7, or 8 bits plus parity)
3. Parity (enabled or disabled)
4. Parity sense (odd or even)
5. Sync character configuration (used as fill character in synchronous mode)

There are distinct differences between the two modes of operation:

1. In the synchronous mode, the XMTR receives a parallel transmit character from the program, generates parity if programmed, serially outputs the character plus parity to the modem, and raises the TX DONE flag to request the next character. If the program fails to provide the next character before transmission of the current character is complete, the XMTR outputs fill characters to maintain continuous transmission until another data character is provided. Whenever a fill character is transmitted, the data not available (DNA) flag is raised to notify the program of fill character transmission.

2. In the isochronous mode, the XMTR receives a parallel transmit character from the program, generates parity if programmed, outputs a start bit, serially outputs the character plus parity, outputs a stop bit, and raises the TX DONE flag to request the next character. However, in the isochronous mode, if the program fails to provide the next character before transmission of the current character is complete, the XMTR simply pauses until the next character is provided. Hence, the DNA flag is never used in the isochronous mode.

The break input inhibits the XMTR output. Whenever the TXCSR break bit is set, the break input to the XMTR logic asserts and inhibits the XMTR output. This input enables the program to inhibit the XMTR output, while inputting data directly to the RCVR via the RCVR input select logic in the internal and external loop maintenance modes.

Interrupt Control Logic

The interrupt control logic consists of two DC003 chips and associated driving circuitry. When the interrupt control logic receives either RXDONE (1) H, TXDONE (1) H, DATA SET CH (1) H, or DNA H with their associated interrupt enable signal, it generates BIRQ L (interrupt request) to the processor. The processor responds with BIAKI L (interrupt acknowledge in), which searches the logic for the originator of the interrupt. If the interrupt was not originated at the DUV11, the signal BIAKO L (interrupt acknowledge out) is passed through with no action taken. If the DUV11 had originated the request, EN VEC TO BUS H is asserted and, depending on the particular interrupt, EN UPPER VEC H may also be asserted. This signal asserted then causes the addressing logic to load, onto the LSI-11 bus, the contents of the preset vector address rocker switches. The processor will then perform the preprogrammed subroutine for that interrupt vector address.

Clear Logic

The clear logic generates clear (CLR) and optional clear (OPT CLR), which initialize all DUV11 logic. The INIT signal or MSTRST asserted will activate the clear signals. INIT is a function of BINIT, which is received by the interface whenever the computer activates the GO function, the processor executes a reset instruction, or the power-fail sequence occurs. The clear logic outputs are asserted as long as the BINIT signal remains low. MSTRST is program-controlled and is generated by setting bit 8 of the TXCSR. When bit 8 of the TXCSR is set and LD TXCSR HB goes low, a 3 μs one-shot asserts MSTRST and the clear signals remain active for the duration of the one-shot.

The OPT CLR output resets RXCSR bits 1, 2, and 3 and thereby clears the control lines to the modem. By not selecting SW1 option switch, OPT CLR is disabled, allowing the DUV11 to be cleared without having to repeat the handshaking sequence. BRPLY is also inhibited as long as CLR is asserted.

Clock Control Logic

The clock control logic decodes the maintenance mode select bits and assigns the transmitter and receiver clocks. There are three possible clock sources: the modem, the programmable SS CLK (single step clock), and the system test clock. If the normal operating mode is decoded, the modem clocks are selected. MS00 (0) H is asserted, enabling the modem clock inputs (TRS CLK, and REC CLK). If the internal loop or external loop maintenance mode is decoded, the SS CLK is selected. This program-controlled clock can be operated very

slowly to facilitate troubleshooting. In the internal loop mode, MS00 (1) H is asserted, enabling SS CLK (1) H. In the external loop mode, MS01 (1) H and MS00 (0) H are asserted, enabling SS CLK (0) H, TRS CLK, and REC CLK. SS CLK (0) H drives CLK EXT, which is routed to the modem test connector, looped back and applied to the TRS CLK and REC CLK inputs. If the system test mode is decoded, the system test clock is selected. This output provides an asynchronous clocking source for the system test mode. MS01 (1) H and MS00 (0) H are asserted, enabling the internal system test clock to drive the transmitter and receiver. In this mode, the modem clock inputs (TRS CLK and REC CLK) are inhibited. When the DUV11 is transmitting in the half-duplex mode, REC CLK is inhibited. HALF DUP (0) L and SEND (0) L go high in this condition, inhibiting REC CLK from reaching the receiver.

+12 to −12 Power Converter

Circuitry is provided to produce −12 Vdc for use by the EIA drivers, the SAT, and the SAR chips. A 600 kHz clock is used to switch +12V into a capacitor network to produce approximately −20V unregulated. This unregulated voltage is then regulated to −12V at the output of two twin zener diode networks. The zeners keep the −12V to within ±5%.

Maintenance Indicators

Indicators in the form of light-emitting diodes are provided to display data lines and modem control states for maintenance purposes. Any of the following lines asserted will cause its respective LED to illuminate: RING H, CLR TO SEND H, DATA SET RDY H, CARRIER H, SERIAL DATA OUT H, and SERIAL DATA IN H.

DUV11

CONFIGURATION

General

The following paragraphs describe how the user can configure the module for his own system. This module contains switches to select the device address, vector interrupt, and special control functions. The descriptions of the registers and their standard factory addresses are listed in Table 1 and described below.

Table 1 DUV11 Factory Address Assignments

Register	Mnemonic	Read/ Write	DUV11 Address
Receiver Status	RXCSR	R/W	160010
Receiver Data Buffer*	RXDBUF	R	160013
Parameter Status*	PARCSR	W	160012
Transmitter Status	TXCSR	R/W	160014
Transmitter Data Buffer	TXDBUF	W	160016
Interrupt Vector	DONE	—	440

* Dual-purpose read or write register.

Device Address

The LSI-11 bus address and interrupt vector addresses, which are selectable, must be determined prior to operating the DUV11. The bus address (also referred to as the device address) is controlled by switches contained in the two switch banks E38 and E39 (Figure 2), located in the address comparator logic. The position of these switches determines the required address state (1 or 0) of bus address bits 12-3. If a switch is set to ON, the switch contacts are closed and an address state of 1 is required on the related address bit to the address of the DUV11. Hence, electrically, the DUV11 can have any device address within the range of 160000 to 177777. However, DIGITAL software requires that the device address fall within the floating address range of 160010 to 163776. The device address is set to 160010 at the factory to facilitate manufacturing testing. The switch positions for address selection are described in Table 1 and Figure 3.

NOTE

If a device address is selected which falls outside the floating address range, the software must be modified accordingly.

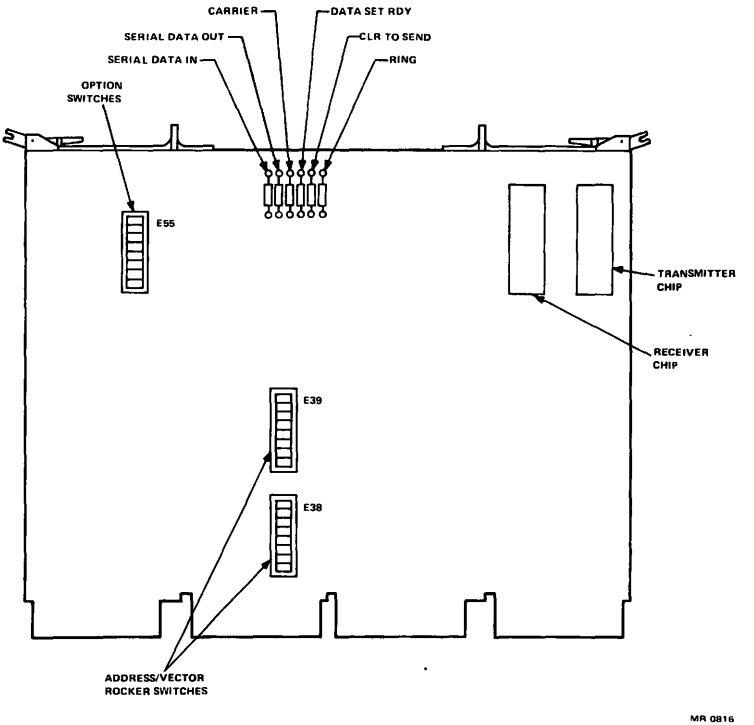


Figure 2 DUV11 (M7951) Major Components

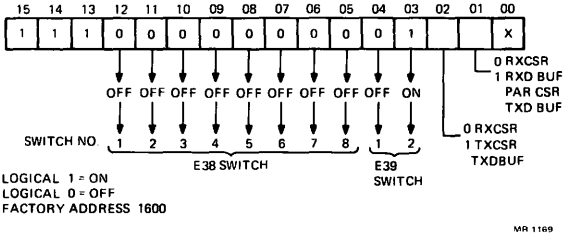


Figure 3 Device Address Selection

Interrupt Vector

The interrupt vector is also floating and is set to 440 at the factory to facilitate factory testing. If it is necessary to change the vector, simply change the six vector select switches contained in switch bank E39 (Figure 2) as required. These switches control vector bits 8-3; therefore, vectors can be generated in the range 000 to 774. However, the software requires that the vector fall within the floating range of 300 to 777. The switch settings for vector selection are shown in Figure 4.

NOTE

If a vector is selected which falls outside the floating address range, the software must be modified accordingly.

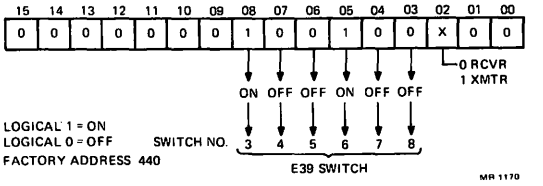


Figure 4 Interrupt Vector Selection

Option Switches

The DUV11 can select optional control functions that are used during operation by using switches S1 through S8 of E55. The detailed operation of these switches is listed in Table 2.

Table 2 Switch Assignments

Switch No.*	Function
SW1	Optional Clear—Switch ON enables CLR OPT, which is used to clear RXCSR bits 3, 2 and 1.
SW2	Secondary Transmit—Switch ON enables secondary data channel between the modem and DUV11.

*All switches are located on component reference designation E55.

Table 2 Switch Assignments (Cont)

Switch No.*	Function
SW3	Secondary Receive—Switch ON enables secondary data channel between the modem and DUV11.
SW4	Sync Characters—Switch ON enables the receiver to synchronize internally upon receiving one sync character. The normal condition of receiving two sync characters exists when SW4 is off.
SW5	Special Feature—Switch ON allows external clock to be internally generated; used when a modem is not being utilized.
SW6	Special Feature—Optional feature is switched ON for program control of data rate selection.
SW7	Maintenance Clock—Switch ON enables the clock that is used for maintenance purposes only.
SW8	Not used.

* All switches are located on component reference designation E55.

Optional Equipment

Mating Connector	H836
Cable	BC05C-XX

Registers

The RXCSR is a read/write register that controls the RCVR (receiver) portion of the interface, communicates interface status, requests, and supervisory data to the modem, and monitors status and supervisory data inputs from the modem.

The word format for the RXCSR is shown in Figure 5 and described in Table 3.

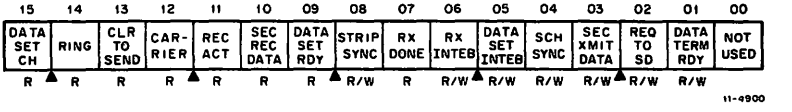


Figure 5 RXCSR Word Format

Table 3 RXCSR Word Format

Bit: 15 **Name:** DAT SET CH
Description: (Data Set Change)
When set, this bit indicates a modem status change.

This bit is set by a transition of any of the following lines:

- Ring
- Clear to Send
- Carrier
- Secondary Received Data
- Data Set Ready

If bit 5 of this register is set, the setting of this bit will cause a RCVR interrupt.

Read-only bit; cleared by INIT, master reset, and the DTI SEL 0 (RXCSR read strobe).

Bit: 14 **Name:** RING
Description: (Ring)
This bit reflects the state of the modem ring line. When set, this bit indicates that a ring signal is being received from the modem. Read-only bit.

Bit: 13 **Name:** CLR TO SD
Description: (Clear to Send)
This bit reflects the state of the clear to send line from the modem. When set, this bit indicates that the modem is ready to accept data from the interface for transmission. Read-only bit.

Bit: 12 **Name:** CARRIER
Description: (Carrier)
This bit reflects the state of the modem carrier. When set, this bit indicates the carrier is up. Read-only bit.

Bit: 11 **Name:** REC ACT
Description: (Receiver Active)
When the internal synchronous mode is selected, this bit is set when the proper number of contiguous sync characters (either 1 or 2, normally set for 2) have been received. If external synchronous or isochronous mode is selected, this bit follows the state of the search sync bit (bit 4 of this register).

Read-only; cleared by INIT, master reset, and SCH SYNC (1) H (search sync) making 1 to 0 transition.

Bit: 10 **Name:** SEC RCV DAT
Description: (Secondary Recieve Data)
This bit reflects the state of the secondary receive data line from the modem. This bit provides a receive channel for supervisory data from the modem to the processor. Read-only bit.

Bit: 9 **Name:** DAT SET RDY
Description: (Data Set Ready)
This bit reflects the state of the data set ready line from the modem. When set, this bit indicates that the modem is powered up and ready. Read-only bit.

Bit: 8 **Name:** STRIP SYNC
Description: (Strip Sync)
This bit determines whether sync characters received from the modem are to be presented to the program for reading. When this bit is set, receive characters that match the contents of the sync register do not cause RCVR interrupt, provided no errors are detected, i.e., bit 15 of the RXDBUF is clear.

Read/write bit; cleared by INIT and master reset.

Bit: 7 **Name:** RX DONE
Description: (Receiver Done)
This bit is set when synchronization has been achieved and a character has been loaded into the RXDBUF, provided the STRIP SYNC bit is not set. If the STRIP SYNC bit is set and the received character is a sync character without errors, i.e., bit 15 of the RXDBUF is clear, this bit will not be set.

When set, this bit will cause a RCVR interrupt request provided bit 6 of this register is set.

Read-only bit; cleared by INIT, master reset, and the DTI SEL 2 (RXDBUF read strobe).

Bit: 6 **Name:** RX INT EB
Description: (Receiver Interrupt Enable)
When set, allows a RCVR interrupt request to be generated when the RX DONE bit is set.

Read/write bit; cleared by INIT and master reset.

Bit: 5 **Name:** DAT SET INT EB
Description: (Data Set Interrupt Enable)
When set, allows a RCVR interrupt request to be generated when the DAT SET CH bit is set.

Bit: 4 **Name:** SCH SYNC
Description: (Search Sync)
When set in the internal synchronous mode, enables the RCVR synchronization logic and causes the RCVR to start comparing incoming data bits to the contents of the sync register in an attempt to recognize a sync character.

When set in the isochronous mode, enables the RX DONE flag generation logic.

When set in the external synchronous mode, enables the RX DONE flag generation logic and causes the RCVR to start framing incoming characters.

Read/write bit; cleared by INIT and master reset.

Bit: 3 **Name:** SEC XMIT
Description: (Secondary Transmit Data)
This bit reflects the state of the secondary transmit data line to the modem. This bit provides a transmit channel for supervisory data from the processor to the modem.

Read/write bit: cleared by INIT and master reset.

Bit: 2 **Name:** REQ TO SD
Description: (Request to Send)
When set, this bit causes the request to send line to the modem to be asserted. The request to send line is a control lead to the modem. This line must be asserted before the interface can transmit data to the modem.

Read/write bit; optionally cleared by INIT and master reset.

Bit: 1 **Name:** DATA TERM RDY
Description: (Data Terminal Ready)
When set, this bit indicates the interface is powered up, programmed, and ready to receive data from the modem.

Setting this bit causes the data terminal ready line to the modem to be asserted. The data terminal ready line is a control lead for the modem communication channel. When asserted, it permits the interface to be connected to the channel.

Read/write bit; optionally cleared by INIT and master reset.

The receiver data buffer (RXDBUF) and the parameter status register (PARCSR) have the same address location, but RXDBUF is a read-only register and PARCSR is a write-only register. The RXDBUF regis-

ter detects interface RCVR status flags and RCVR parallel data outputs. Its word format is shown in Figure 6 and described in Table 4. The PARCSR register establishes the overall operating parameters of the DUV11, i.e., the mode of operation (synchronous or isochronous), word length (5, 6, 7, or 8 bits plus parity), parity (enabled or disabled), parity sense (odd or even), and sync character configuration. Its word format is shown in Figure 7 and described in Table 5.

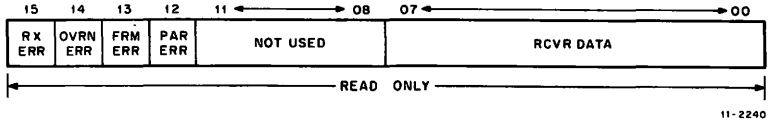


Figure 6 RXDBUF Word Format

Table 4 RXDBUF Word Format

Bit: 15 **Name:** RX ERR
Description: (Receive Error)
This bit is set whenever one of the three receiver error bits is set (logical OR of bits 14, 13 and 12).

Read-only bit, cleared only when bits 14, 13, and 12 are cleared.

Bit: 14 **Name:** OVRN ERR
Description: (Overrun Error)
When set, this bit indicates that the processor has failed to service the RX DONE flag within the time required to load another character into the RXDBUF, i.e, (1/baud rate) × (bits per character) seconds. Hence, the previous character was overwritten (lost). This condition indicates the loss of at least one character.

Read-only bit; cleared by INIT, master reset, and DTI SEL 2 (RXDBUF read strobe).

Bit: 13 **Name:** FRM ERR
Description: (Framing Error)
When set, indicates that character received was not followed by a valid stop bit. This error only occurs in the isochronous mode of operation.

Read-only bit; cleared by INIT, master reset, and DTI SEL 2.

Bit: 12 **Name:** PAR ERR
Description: (Parity Error)
When set, indicates that the parity of the received character does not agree with the parity programmed (odd or even). If parity is not programmed, this bit is always cleared.

Read-only bit; cleared by INIT, master reset and DTI SEL 2.

Bit: 7-0 **Name:** RCVR DATA
Description: (Receiver Data)
This register holds the received character for transfer to the program. The buffer is right-justified for 5, 6, 7 or 8 bits. If parity is received, it is also loaded into the buffer at the next vacant higher order bit position. Therefore, if a 5-bit character plus parity is framed by the RCVR, the parity bit would be loaded into bit position 5 in the RXDBUF and presented to the program for reading. If an 8-bit character plus parity is framed, the parity bit would not be presented to the program for reading.

Read-only buffer; cannot be cleared; INIT or master reset sets the buffer to all 1s. Reading the RDXBUF causes the RX DONE bit in the RXCSR to clear.

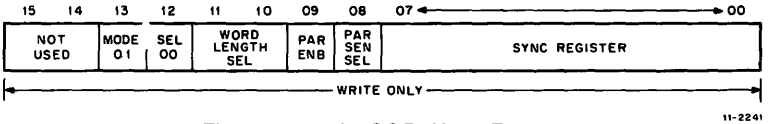


Figure 7 PARCSR Word Format

Table 5 PARCSR Word Format

Bit: 13-12 **Name:** MODE SEL
Description: (Mode Select)
These bits control the mode of operation. Modes are selected as follows:

Mode	Bit 13	Bit 12
Internal Synchronous	1	1
External Synchronous	1	0
Isochronous	0	0
Illegal (not used)	0	1

Write-only bits.

Bit: 11-10 **Name:** WORD LEN SEL
Description: (Word Length Select)
These bits control the length of characters received and transmitted by interface. Word length (not including parity) is selected as follows:

Bits/Char	Bit 11	Bit 10
5	0	0
6	0	1
7	1	0
8	1	1

Write-only bits.

Bit: 9 **Name:** PAR ENB
Description: (Parity Enable)
If this bit is set, parity for each character will be generated by the XMTR and checked by the RCVR. If character length is less than eight bits, the parity bit for received data is loaded into the RXDBUF for reading by the program. If bad parity is detected at the RCVR, the parity error flag is set (bit 12 of the RXDBUF).

Write-only bit.

Bit: 8 **Name:** PAR SEN SEL
Description: (Parity Sense Select)
When the parity enable bit (bit 9 of this register) is set, the sense of the parity (odd or even) is controlled by this bit. When this bit is set, even parity is generated by the XMTR and checked for by the RCVR. (The program does not have to provide a parity bit to the XMTR.) When this bit is cleared, odd parity is generated and checked.

Write-only bit.

Bit: 7-0 **Name:** Sync Register
Description: This register contains the sync character. The sync character is used by the RCVR to detect received sync characters and thereby achieve synchronization.

The sync character is used as a fill character by the XMTR when operating in the synchronous mode. Fill characters are transmitted when the program fails to provide characters to the XMTR fast enough to maintain continuous transmission i.e, (1/baud rate) × (bits per character) seconds − ½ (bit time).

The transmitter status register (TXCSR) is a read/write register that controls the XMTR (transmitter) portion of the interface, controls the resetting and initialization of the interface, and controls and monitors the maintenance mode operation of the interface.

The TXCSR word format is shown in Figure 8 and described in Table 6.

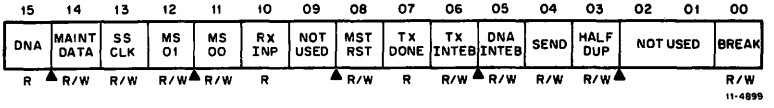


Figure 8 TXCSR Word Format

Table 6 TXCSR Word Format

Bit: 15 **Name:** DNA
Description: (Data Not Available)
This bit is set by the XMTR when a fill character is transmitted. This applies only to the synchronous mode of operation and is caused by late program response to a TX DONE interrupt request.

The processor response to TX DONE must be within (1/baud rate) × (bits per character) seconds − ½(bit time). If not, the fill character is transmitted.

If bit 5 of this register is set, setting this bit causes an XMTR interrupt request.

Read-only bit; cleared by INIT, master reset, and DTI SEL 4 (TXCSR read strobe).

Bit: 14 **Name:** MAINT DATA
Description: (Maintenance Data)
This bit is used in the internal loop and external loop maintenance modes by the diagnostic program to simulate serial input to the RCVR.

Read/write bit; cleared by INIT or master reset.

Bit: 13 **Name:** SS CLK
Description: (Single Step Maintenance Clock)
This bit is used in the internal loop and external loop maintenance modes by the diagnostic program to simulate XMTR and RCVR clocks.

Read/write bit; cleared by INIT or master reset.

Bit: 12-11 **Name:** MS01/MS00
Description: (Maintenance Mode Select 01 and 00)
These bits are used to select the normal mode of operation or one of three maintenance modes. Modes are selected as follows:

Mode	Bit 12	Bit 11
Normal	0	0
Internal Maintenance Loop	0	1
External Maintenance Loop	1	0
System Test	1	1

Read/write bits; cleared by INIT and master reset.

Bit: 10 **Name:** RX INP
Description: (Receiver Input)
This bit monitors the RCVR input to the internal loop and external loop maintenance modes.

Read-only bit.

Bit: 9 **Name:** MSTRST
Description: (Master Reset)
This bit is used to generate a CLR (clear) pulse, which initializes the registers and the XMTR and RCVR and inhibits the BRPLY L (bus reply) signal. This bit remains at a (1) for only 3 μs after being set.

Read/write bit.

Bit: 7 **Name:** TX DONE
Description: (Transmitter Done)
This bit is set by INIT and master reset and when the first bit of the character contained in the XMTR register is placed on the XMTR output line. If bit 6 of this register is set when this bit is set, an XMTR interrupt request is generated.

Read-only bit; cleared by LD TXDBUF (TXDBUF load strobe).

Bit: 6 **Name:** TX INT EB
Description: (Transmitter Interrupt Enable)
When set, this bit allows a XMTR interrupt request to be generated by the TX DONE bit.

Read/write bit; cleared by INIT and master reset.

Bit: 5 **Name:** DNA INT EB
Description: (Data Not Available Interrupt Enable)
When set, this bit allows an XMTR interrupt request to be generated by the DNA bit.

Read/write bit; cleared by INIT and master reset.

Bit: 4 **Name:** SEND
Description: (Send)
When set, this bit enables the XMTR and transmission will start when a character is loaded into the TXDBUF. This bit must remain set until the entire message is transmitted. If not, transmission of the character currently in the XMTR register is completed and the XMTR will enter the idle state.

Read/write bit; cleared by INIT and master reset.

Bit: 3 **Name:** HALF DUP
Description: (Half-Duplex)
When this bit is set, operation will be in the half-duplex mode. In this mode, the RCVR is disabled whenever bit 4 of this register is set.

Read/write bit; cleared by INIT and master reset.

Bit: 0 **Name:** BREAK
Description: (Break)
When this bit is set, the serial XMTR output D5 SERIAL DATA OUT H is held in the space (constant low) condition; otherwise, operation is normal. This bit is used by the diagnostic program in the internal loop or external loop maintenance modes to inhibit the XMTR output while inputting data to the RCVR via bit 14 of this register.

Read/write bit; cleared by INIT and master reset.

The transmitter data buffer (TXDBUF) is a write-only register that provides parallel data to the interface XMTR for serial transmission to the modem. The word format for the TXDBUF is shown in Figure 9 and described in Table 7.

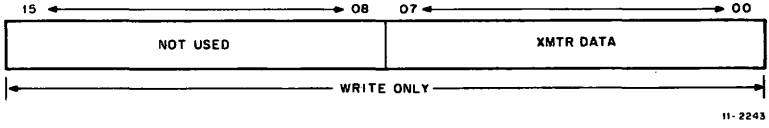


Figure 9 TXDBUF Word Format

Table 7 TXDBUF Word Format

Bit: 7-0 **Name:** XMTR DATA
Description: (Transmitter Data)
This register is loaded by the program with the character to be transmitted. Character length is from 5 to 8 bits. The character is right-justified. If a parity bit is enabled, it is generated by the interface.

Write-only bits; an INIT or master reset places all 1s in this register.

DZV11 ASYCHRONOUS MULTIPLEXER

GENERAL

The DZV11 is an asynchronous multiplexer interface module that interconnects the LSI-11 bus with up to four asynchronous serial data communications channels. The module provides EIA interface levels and enough data set control to permit dial-up (auto-answer) operation with modems using full-duplex operations such as Bell models 103, 113, 212, or equivalent. The DZV11 does not support half-duplex operations such as remote operation over private lines for full-duplex point-to-point or full-duplex multipoint as a control (master) station. The DZV11-B includes a BC11U cable assembly for interconnection to the communication devices.

The DZV11-B interface consists of the M7957 module, a BC11U-25 interface cable, and two accessory test connectors (H329 and H325). The H329 connector permits a staggered loopback. The H325 connector is used with the BC11U cable to provide the single-line loopback.

FEATURES

- Selectable baud rates of 50 to 9600
- Character length of 5, 6, 7, or 8-bits
- Stop bits, 1 or 2, for 6-, 7-, and 8-bit characters
- Stop bits, 1 or 1.5, for 5-bit characters
- Parity generation and detection for odd, even, and no parity
- Transmitter and receiver interrupts
- Generates and detects break signals

SPECIFICATIONS

Identification	M7957
Size	Quad
Power	+5 Vdc ±5% at 1.15 A +12 Vdc ±3% at 0.40 A
Bus loads	
AC	3.95
DC	1
Performance	Interface signals meet EIA standard RS-232C

DESCRIPTION

General

The DZV11 module transmits communication data from the LSI-11 bus, through the interface, to the transmitter data register in the UARTs. There they are converted from parallel data to serial data and sent to the EIA transmitters. The transmitters convert the serial data from TTL levels to EIA levels and send them to the communication line. A functional diagram of the module is shown in Figure 1.

Data coming in from the communication lines are converted from EIA to TTL by the EIA receivers, then from serial to parallel by the UARTs. The parallel data leaves the UART receiver buffers and are stored in the silo buffer. From there it is transferred via multiplexers to the bus interface. The bus interface places the data on the LSI-11 bus.

The interrupt logic requests interrupt service when a transmitter is empty and when the silo buffer has either 1 or 16 characters of received data, as selected by the program.

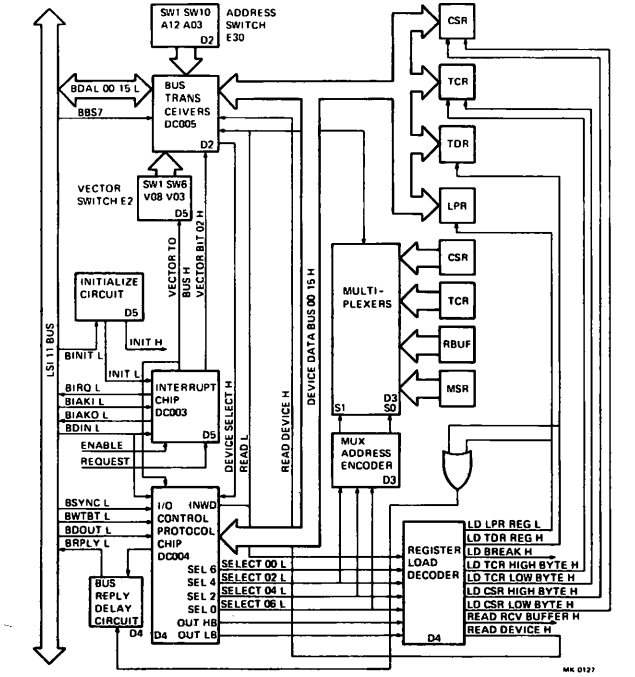


Figure 1 Bus Interface, I/O Control, and Interrupt Logic

The transmitter control determines which of the four possible lines is to be used, and controls the loading of the data.

The receiver control scans the receiver status and controls the loading and unloading of the silo.

The speed and format control generates clock signals for the UARTs. Under program control, it selects baud rate and stop bit, parity bit, and character length parameters.

The break logic inhibits output data to create a break signal. The four lines operate independently and under program control.

The maintenance mode data selector provides the capability of switching the data outputs and the data inputs. This is used to verify module operation.

Interrupt Logic

Most of the logic for interrupts is contained in a single DC003 interrrupt chip. The chip contains two interrupt channels: one for receiver interrupts and one for transmitter interrupts. The circuit generates a receiver interrupt either when the RBUF has one character ready for the computer (receiver-done interrupt) or when the silo buffer has 16 characters ready (silo-alarm interrupt.)

The receiver-done interrupt is enabled by setting CSR bit 6. The silo-alarm interrupt is enabled by setting bit 12. Setting bit 12, however, inhibits the receiver-done signal from the RBUF. Therefore, receiver-done interrupts do not occur when silo-alarm interrupts are enabled.

The circuit generates a transmitter interrupt when the transmitter data register is empty and ready for another data output from the computer. The transmitter-ready interrupt is enabled by setting CSR bit 14.

A silo-alarm interrupt can be distinguished from a receiver-done interrupt by checking the corresponding bits in the CSR when entering a service routine.

EIA Receivers

The DZV11 receives three modem signals for each of the four communication lines it interfaces. Carrier-detect, ring-indicator, and received-data are received and converted from EIA levels to TTL levels. The carrier and ring signals go to the modem status register. The received-data signals go the RBUF (in the UARTs).

EIA Transmitters

The DZV11 can control up to three modem control signals for each of the four communication lines it interfaces. Control bits from the trans-

mitter control register are converted from TTL levels to EIA levels to drive modem control lines. For each line there is a single control bit that is always connected to data-terminal-ready. These signals may be jumpered to also control request-to-send. If this is done, they may then be further jumpered to control forced-busy (for Bell model 013E and 113B modems with the forced-busy option).

Data to be transmitted from the computer to the lines move from the transmitter data buffer to the EIA transmitters, where they are converted from TTL levels to EIA levels and placed on the lines.

UARTs

The DZV11 uses four universal asynchronous receiver/transmitter (UART) chips, one for each of the four communication lines. Each UART performs part of the functions of the receiver buffer (RBUF), transmitter data register (TDR), and line parameter register (LPR) for the channel under its control. The RBUF takes serial data received by the EIA receivers, strips off the start, stop, and parity bits, converts them to parallel data, and places them on the device data bus. The TDR takes parallel data from the device data bus, appends start, stop, and parity bits, converts them to serial data, and sends them to the EIA transmitter. The LPR controls the speed, parity, and number of stop bits that the RBUF and TDR use.

Setting Line Parameters — The low byte of the LPR is contained inside the UARTs, and controls the data format. The high byte is contained in the baud rate generator circuits and controls the speed at which data is transmitted and received.

When the computer addresses the LPR, the I/O control logic generates a load pulse. The load pulse enables LPR bits 0 and 1 to strobe the selected UART and baud rate generator. Bits 3 through 7 are latched into the UART to select the data format. Bits 8 through 11 are latched into the baud rate generator to select the speed. Bit 12 enables the receiver clock signal to reach the UART.

UART Receiver Operation — Serial data coming in from the EIA receiver are applied to the receiver section of the selected UART. The UART samples the serial input at the receiver clock rate (16 times the data bit rate). The line is in a continuous marking state when idle. When a start bit arrives, the UART detects the mark-to-space transition. It samples the line again at the time corresponding to the middle of the start bit. If the line is marking, the UART logic assumes that the first sample was noise, and resumes sampling. If it finds that the line is still spacing, however, the logic assumes it is receiving a start bit, and

enters the data entry mode. In this mode the UART shifts the data serially into an internal register. If parity is enabled, the UART checks the total of the received data bits plus the parity bit. (It checks for an even total if even parity has been selected, and an odd total if odd parity has been selected.) A parity error causes the UART to set the parity error flag bit in the high byte of the RBUF word.

The UART checks the stop bit to see if it is marking. If the line is spacing instead, the UART sets the framing-error flag bit. If the line is marking, the UART logic assumes there is a valid stop bit.

About half-way through the stop bit time, the UART transfers the received-character data, the parity-error bit, and the framing-error bit from the serial shift register to the holding register. At this time it asserts the data-available signal to the receiver-control logic. If the previous character has not yet been serviced by the receiver-control logic, the UART sets the overrun-error flag bit to indicate that the previous character was lost.

The receiver control loads the contents of the RBUF (data and status) into the silo buffer for subsequent transfer to the computer. The receiver-control circut determines when and what type of receiver interrupt to request.

UART Transmitter Operation — During idle time, the UART transmits a continuous marking signal and holds the transmitter ready signal (TBMT) asserted. The transmitter control circuitry uses this signal to determine when to initiate a transmitter interrupt request.

When the computer has data to transmit to a communication line, it uses a DATO or DATOB sequence to address the TDR and place the data on the bus lines. The low byte of the TDR word is loaded into a holding register in the UART. When the data enters the holding register, the UART negates TBMT. It then transfers the data in parallel from the holding register to a serial shift register and reasserts TBMT. In the serial shift register, the UART attaches start, stop, and parity bits, as set by the LPR. The assembled character is then shifted serially out to the EIA transmitter.

Because the transmitter, like the receiver, is double-buffered, it can be loading in a second character before the first one moves out.

Break Bits

The transmission and reception of break bits are closely related to the transmission and reception of data. A break signal is a continous spacing condition on the serial data line. When a UART receives a

break signal, it interprets the continuous space as a character that is missing a stop bit. Therefore, it sets the framing-error flag. The program then determines how a framing error is handled.

A break signal may be transmitted by interrupting the flow of serial data leaving the UART. The high byte of the TDR may be thought of as a break register. It contains one break bit for each of the four communication channels. Setting one of these bits will inhibit the flow of data from the UART transmitter to the EIA transmitter, thereby causing a break to be transmitted on the communication line.

Speed and Format Control

The circuits controlling speed and format include the line parameter register, two dual-baud-rate generator chips, an oscillator, and two addressable latches.

When the LSI-11 bus writes a word out to the LPR, the following events occur.

1. During address time the bus interface and I/O control circuitry decode the address and produce a load pulse, LD LPR REGISTER L.
2. During data time, the load pulse enables two addressable latches to be addressed by bits 0 through 2. One latch routes the state of bit 12 to a gate that inhibits or enables the receiver clock to the selected UART. For a receive operation the clock is enabled; for a transmit operation it is inhibited.

   The other latch applies an enabling signal (CONTROL STROBE H) to both the UART and the baud-rate generator chip section that controls the communication line selected by bits 0 through 2.
3. Bits 3 through 7 are strobed into the selected UART to select the number of data bits, the number of stop bits, and odd, even, or no parity.
4. Bits 8 through 11 are strobed into the selected baud-rate generator chip to control the amount by which the 5 MHz oscillator is divided to produce the UART clock signal.

Thus, the line parameter register is formed by the latches located in the UARTs, baud-rate generators, and addressable latches.

Receiver Control

Receiver Scanner — The receiver scanner circuit samples the states of the data available signals from the UARTs. When it detects a true condition, it generates a load pulse to transfer the received data from

the UART to the silo buffer. The sequence in which the receiver-data-available (DA) flags are scanned and the characters loaded into the silo buffer is controlled by a 4-phase timing sequencer and a group of multiplexers, demultiplexers, and counters.

The sequencer produces four timing signals. The signal times are designated Phase 1 through Phase 4.

During Phase 1, a signal toggles the address generator to increment by one count. The two least significant bits of the counter are used as a 2-bit address code, designated RCV SCAN LEAD A and RCV SCAN LEAD B. These two signals address a multiplexer. The multiplexer selects the data-available-line from the UART corresponding to the address code and applies it to a gate. The other input to the gate is a ready signal from the silo buffer. This signal is asserted when the silo is ready to load data.

If the data-available signal is set and the silo buffer is ready, the gate asserts SILO LOAD REQUEST H. The load request is applied to the load-silo flip-flop.

RCV SCAN LEAD A and RCV SCAN LEAD B also address a demultiplexer. The demultiplexer places an enabling signal (RCV DATA ENABLE) on the line to the UART addressed by the scan leads. This is the same UART that is having its DA line sampled. The RCV DATA ENABLE signal enables the UART to place the contents of the receiver holding register on the lines to the silo buffer (RD1 through RD8).

During Phase 2, the sequencer clocks the load-silo flip-flop. If SILO LOAD REQUEST H is true, the flip-flop sets. When the flip-flop sets, one output goes to the silo buffer as LOAD SILO H and strobes received data from the UART into the silo buffer. At the same time the data enter, status information is also loaded into the silo. Framing-error, overrun-error, and parity-error bits from the selected UART are routed via multiplexers into the silo. The states of RCV SCAN LEAD A and RCV SCAN LEAD B are loaded into the silo to indicate from which communication line the received character came.

LOAD SILO H also goes to a latch in the sequencer. From there it passes through a demultiplexer and asserts RESET DA to the selected UART. RESET DA clears the data available flag in the UART so that another character may be received.

At the beginning of Phase 4 time, the transition out of Phase 3 clocks the silo counter. The silo counter increments by one count to keep a tally of the number of times the silo buffer has been loaded.

Phase 4 re-establishes the initial conditions of the scanner circuit for the next scan cycle.

Silo Buffer — The silo buffer comprises four 4 × 64-bit 3341 serial memory chips. The chips are arranged as a 16-bit long, 64-word deep first-in first-out memory. Data is entered in the "top" of the memory as described in the previous section. The in-ready signal means there is a vacancy in the top word of the memory. Similarly, the out-ready signal indicates there is a word in the "bottom" of the silo waiting to be shifted out.

The buffer stores full RBUF words. Received character data is stored in the low byte, and receiver data in the high byte. The buffer shifts data in when it receives LOAD SILO H from the load-silo flip-flop, and it shifts data out when it receives UNLOAD SILO H from the unload control.

Data is shifted out as a result of either a receiver-done interrupt or a silo-alarm interrupt. The presence of an output-ready signal from each of the four chips asserts RECEIVER DONE H to the interrupt logic. If the receiver-done interrupt enable bit is set, the interrupt logic will assert the interrupt request signal to the CPU.

If the silo-alarm interrupt enable bit is set, RECEIVER DONE H is inhibited at the interrupt logic. In this case, a receiver interrupt is not requested until the silo buffer has 16 characters ready. Setting silo-alarm-enable allows the silo counter to increment each time the silo is loaded. On the 16th count, the silo counter overflows, and the carry-out signal sets the silo-alarm flip-flop. The flip-flop in turn asserts SILO ALARM H to the interrupt logic.

When the interrupt request is acknowledged, the silo is unloaded. The unloading sequence is the same for both types of receiver interrupts. It proceeds as follows:

1. When data reaches the bottom of the silo, the out-ready signals are gated together to produce RECEIVER DONE H.
2. RECEIVER DONE H is applied to a latch. When a CPU input transaction (DATI) addresses the RBUF, READ RCV BUFFER H latches the state of RECEIVER DONE H.
3. The output of the latch is VALID DATA H. This signal conditions one input of a one-shot.
4. The trailing edge of READ RCV BUFFER H triggers the one-shot, which generates UNLOAD SILO H.

5. UNLOAD SILO H causes the silo buffer to shift out an RBUF word (character and status data). The word is transferred via a multiplexer to the device data bus. From there the bus transceivers place it on the LSI-11 bus. VALID DATA H is applied to the multiplexer along with the output of the silo buffer, where it becomes bit 15 of the RBUF word.

Transmitter Control

The transmitter control circuit checks the transmitter control register to determine which lines are enabled. It checks the UARTs to determine which are ready to transmit, and it enables the UART controlling the highest priority line to load data from the CPU.

The sequence begins with the master scan enable signal from the CSR. MASTER SCAN ENBL H triggers a 350 ns one-shot. The leading edge of the one-shot output clocks a 4-bit latch. A true bit in the latch indicates that the corresponding line is enabled and that the transmitter buffer empty flag is set for the UART controlling that line. Outputs from the latch are applied to a priority encoder. The priority encoder generates a 2-bit code to represent the communication line number. When more than one channel is ready at the same time, the code always indicates the one having the highest priority. (Line 3 has the highest priority; line 0, the lowest.) This code addresses two multiplexers in the transmitter control circuit, and also goes to CSR bits 8 and 9. CSR bits TLINE A and TLINE B tell the program on which line the next character will be transmitted. The priority encoder also applies a ready signal to the transmitter ready flip-flop when any of the bits in the latch are true.

The trailing edge of the 350 ns one-shot output performs two functions:

1. The zero (false) output checks the transmitter ready flip-flop. Assuming a line-enable bit is set and a TBMT signal is true, the transmitter-ready flip-flop asserts TRANSMITTER READY H to the interrupt logic and the CSR. If enabled, a transmitter-interrupt request will be initiated.

   The transmitter-ready flip-flop also disables the gate controlling the input to the 350 ns one-shot. This inhibits further clocking until the line can be serviced. At the same time, the signal enables the contents of the line-enable latch to enter a multiplexer.
2. The second function of the trailing edge of the 350 ns one-shot is to trigger a 100 ns one-shot. The output of the 100 ns one-shot

disables the input to the 350 ns one-shot. The 350 ns one-shot is inhibited to prevent losing the latched-in line number.

The assertion of TRANSMITTER READY H ultimately results in the CPU performing a DATOB to load data into the TDR. During address time, the I/O control asserts load pulse LD TDR REGISTER H. LOAD IN PROGRESS L from the I/O control strobes LD TDR REGISTER H into a demultiplexer. The demultiplexer output is a transmitter-holding-register load pulse (THRL). It is routed to the UART that controls the line addressed by the priority encoder. This enables the UART transmitter to load character data from the device data bus during data time.

When LD TDR REGISTER H returns to the negated state, the trailing edge triggers a 100 ns one-shot. The output of the one-shot clears the transmitter ready flip-flop. It also disables the gate controlling the input to the 350 ns one-shot. The 350 ns one-shot is inhibited in order to allow the UART sufficient time to drop its transmitter-buffer-empty flag before the circuit starts another scan cycle.

When the program is finished sending a message, it clears the line-enable bit in the TCR. This occurs after enable-bit-TMBT signals have already been latched in and TRANSMITTER READY H has not asserted. It is therefore necessary to prevent the scanner from locking up on a line for which there is no data. This is accomplished by clearing the transmitter-ready flip-flop if it is set for a line which is no longer enabled. The states of the line-enable bits from the TCR are applied to a multiplexer. The bit corresponding to the line addressed by the priority encoder is passed to a pulse-forming circuit. If the bit is in the clear state, a 50 ns pulse is formed. This pulse clears the transmitter-ready flip-flop, thereby negating TRANSMITTER READY H and allowing the 350 ns one-shot to fire for the next transmitter scan cycle.

Maintenance Mode

The DZV11 can be switched to receive the data that it is transmitting. The four serial data lines leaving the UARTs are applied to both a data selector and the EIA transmitter. The data selector controls the inputs to the UART receivers. During normal operation, data from the EIA receivers is routed through the data selector to the UART receivers. In the maintenance mode, the data selector ignores the inputs from the EIA receivers. Instead, it routes the output data to the UART receivers. This internal "wrap around" feature is enabled by setting the maintenance bit in the CSR. Setting CSR bit 3 asserts MAINTENANCE H, which switches the data selector.

Power Supplies

In addition to the +12V and +5V available on the LSI-11 bus, the DZV11 also requires +3V, −9V, and −12V. The +3V source is a voltage divider. The negative voltages are produced by two capacitive-charge pump circuits.

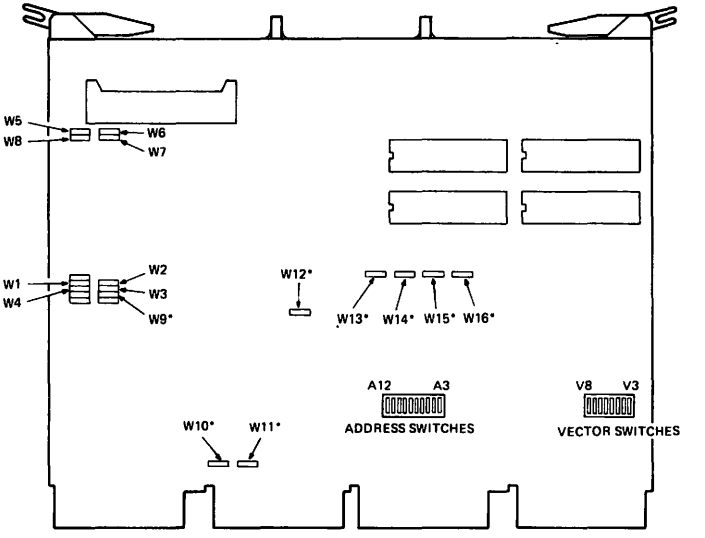
Each of the two charge pumps uses the following scheme:

1. An oscillator running at approximately 500 kHz switches a pair of drivers on and off.
2. The outputs of the drivers are capacitively coupled to a rectifier.
3. The negative-going output of the rectifier builds up a charge on a capacitor.
4. The charge is zener-regulated back to the required negative voltage.

CONFIGURATION

General

The software control of the DZV11 is performed by six device registers. These registers are assigned addresses and can be read or loaded by the program. DIGITAL software requires that the device addresses be within the range of 760000 to 777777. The M7957 module utilizes the floating address space that starts at 760010 and extends to 764000. The control and status register (CSR) is assigned the basic address by setting the rocker switches of E30 on the module as shown in Figure 2. The correlation between the bit assignments and the switches is detailed in Figure 3. The remaining register addresses will sequentially follow the basic address as shown in Table 1. A basic address is preset at the factory; if the user requires a different address, the switches allow him to change the addresses to comply with his system. The interrupt vector is also programmable and can be used with DIGITAL software, provided that the address is within 300 to 777. The switches of E2 on the module (Figure 1) allow the user to select an interrupt vector to function within his system. The correlation between the bit assignments and the switches is detailed in Figure 4.



*NOTES:

JUMPERS W9, W12, W13, W14, W15, AND W16 ARE REMOVED ONLY FOR MANUFACTURING TESTS. THEY SHOULD NOT BE REMOVED IN THE FIELD.

JUMPERS W10 AND W11 MUST REMAIN INSTALLED WHEN THE MODULE IS USED IN A BACKPLANE THAT SUPPLIES LSI-11 BUS SIGNALS TO THE C AND D CONNECTORS OF THE DZV11 (SUCH AS THE H9270). WHEN THE MODULE IS USED IN A BACKPLANE THAT INTERCONNECTS THE C AND D SECTIONS TO AN ADJACENT MODULE, JUMPERS W10 AND W11 MUST BE REMOVED.

MK-0064

Figure 2 M7957 Module

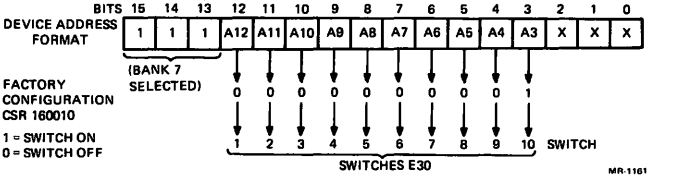


Figure 3 DZV11 CSR Address Bits

Table 1 DZV11 Register Address Assignments

Register	Mnemonic	Address*	Read/ Write
Control and Status	CSR	76XXX0	R/W
Receiver Buffer	RBUF	76XXX2	R
Line Parameter	LPR	76XXX2	W
Transmitter Control	TCR	76XXX4	R/W
Modem Status	MSR	76XXX6	R
Transmit Data	TDR	76XXX6	W

* XXX = Selected in accordance with floating device address scheme. Dual-purpose register.

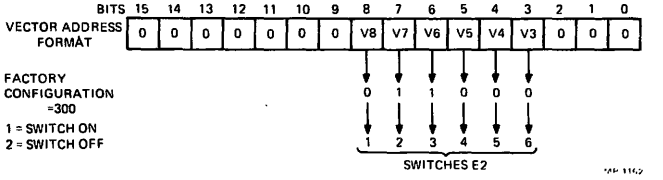


Figure 4 DZV11 Vector Bits

Jumpers

Modem Control — There are eight jumpers (W1-W8) used for modem control. Jumpers W1 and W4 connect data terminal ready (DTR) to request to send (RTS). This allows the DZV11 to assert both DTR and RTS when using a modem that requires the control of RTS. These jumpers must be installed to run the external cable and test diagnostic programs. Jumpers W5 through W8 connect the forced-busy leads to the request-to-send leads. When these jumpers are installed, the assertion of an RTS signal places an ON or busy signal on the corresponding forced busy lead. Forced busy jumpers W5-W8 are normally removed unless they are required for the modem. These modem control jumpers are listed in Table 2.

Table 2 Modem Control Jumper Configuration

Jumper	Connection	Line
W1	DTR to RTS	3
W2	DTR to RTS	2
W3	DTR to RTS	1
W4	DTR to RTS	0
W5	RTS to FB	3
W6	RTS to FB	2
W7	RTS to FB	1
W8	RTS to FB	0

Bus Signals — Jumpers W10 and W11 must remain installed when the module is used in a backplane that supplies bus signals to C and D connectors such as the H9270. When the module is in a backplane that uses the C-D interconnect scheme (such as the H9273), the jumpers W10 and W11 must be removed.

Testing — Jumpers W9 and W12 through W16 are removed for manufacturing test purposes only. These jumpers should not be removed by the user.

Device Registers — All software control of the DZV11 is performed by six device registers. Each register is assigned a bus address that can be read or loaded. The following paragraphs define the bits within a register and their specific function to the operation of the DZV11. Bits that are designated as "not used" and "write-only" are always read as 0 and attempts to load these bits will have no effect on the operation.

Control and Status Register — The control and status register (CSR) is a byte- and word-addressable register. All bits in the CSR are cleared by an occurrence of BINIT or by setting device master clear (CSR 4). The format is shown in Figure 5 and the bit assignments are listed in Table 3.

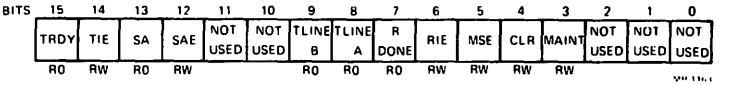


Figure 5 CSR Bit Assignments

Table 3 CSR Bit Assignments

Bit: 0-2 **Name:** Not Used
Description:

Bit: 3 **Name:** Maintenance
Description: This bit, when set, loops all the transmitter's serial output leads to the corresponding receiver's serial input leads on a TTL basis. While operating in maintenance mode, the EIA received data leads are disabled. Normal operating mode is assumed when this bit is cleared. This bit is a read/write bit.

Bit: 4 **Name:** Master Clear
Description: When written to a one, generates "initialize" within the DZV11. A readback of the CSR with this bit set indicates initialize in progress within the device. This bit is self-clearing. All registers, silos, and UARTs are cleared with the following exceptions:

1. Only bit 15 of the receiver buffer register (valid data) is cleared; the remaining bits 0 through 14 are not.
2. The high byte of the transmitter control register is not cleared by master clear.
3. The modem status register is not cleared by master clear.

Bit: 5 **Name:** Master Scan Enable
Description: This read/write bit must be set to permit the receiver and transmitter control sections to begin scanning. When cleared, Transmitter Ready (CSR bit 15) will be inhibited from setting and the received character buffers (silos) will be cleared.

Bit: 6 **Name:** Receiver Interrupt Enable
Description: This bit, when set, permits the setting of CSR bits 7 and 13 to generate a receiver interrupt request. This bit is a read/write bit.

Bit: 7 **Name:** Receiver Done
Description: This is a read-only bit that will set when a character appears at the output of the FIFO buffer. To operate in interrupt per character mode, CSR bit 6 must be set and CSR bit 12 must be

cleared. With CSR bits 6 and 12 cleared, character flag mode would be indicated. Receiver done will clear when the receiver buffer register (RBUF) is read or when Master Scan Enable (CSR bit 5) is cleared. If the FIFO buffer contains an additional character, the receiver done flag will stay cleared a minimum of 1 μs before presenting that character.

Bit: 8-9 **Name:** Transmitter Line Number

Description: These read-only bits indicate the line number whose transmit buffer requires servicing. These bits are valid only when Transmitter Ready (CSR bit 15) is set and will be cleared when Master Scan Enable is cleared. Bit 8 is the least significant bit.

Bit: 10-11 **Name:** Not used

Description:

Bit: 12 **Name:** Silo Alarm Enable

Description: This is a read/write bit; when set, enables the silo alarm counter to keep count of the number of characters stored in the FIFO buffer. The counter will be cleared when the Silo Alarm Enable bit is cleared. Conditioning of this bit must occur prior to any character reception.

Bit: 13 **Name:** Silo Alarm

Description: This is a read-only bit set by the hardware after 16 characters have been entered into the FIFO buffer. Silo Alarm will be held cleared when Silo Alarm Enable (CSR bit 12) is cleared. This bit will be reset by a read to the receiver buffer register and will not set until 16 additional characters are entered into the buffer. If Receiver Interrupt Enable (CSR bit 6) is set, the occurrence of Silo Alarm will generate a receiver interrupt request. Reception with CSR bit 6 cleared permits flag mode operation of the silo alarm bit.

Bit: 14 **Name:** Transmitter Interrupt Enable

Description: This bit must be set for Transmitter Ready to generate an interrupt. It is a read/write bit.

Bit: 15 **Name:** Transmitter Ready

Description: This bit is read-only and is set by the hardware. This bit will set when the transmitter clock stops on a line whose transmit buffer may be loaded with another character and whose associated TCR bit is set. The transmitter line number, specified in CSR bits 8 and 9, is only valid when Transmitter Ready is set. Transmitter Ready will be cleared by any of the following conditions:

1. Master Scan Enable cleared
2. When the associated TCR bit is cleared for the line number pointed to in CSR bits 8 and 9

3. At the conclusion of the load instructions of the transmit data register (low byte only).

If additional transmit lines require service, Transmitter Ready will reappear within 1.4 μs from the completion of the transmit data register load instruction. The occurrence of Transmitter Ready with Transmitter Interrupt Enable set will generate a transmitter interrupt request.

Receiver Buffer — The receiver buffer (RBUF) is a 16-bit read-only register which contains the received character at the output of the FIFO buffer. A read of the register causes the character entry to be extracted from the buffer and all other entries to bubble down to the lowest unoccupied location. Only the valid data bit (RBUF bit 15) is cleared by BINIT or by setting device master clear (CSR bit 4). Bits 0-14 are not affected. The bit assignments for the RBUF register are listed in Table 4 and the format is shown in Figure 6.

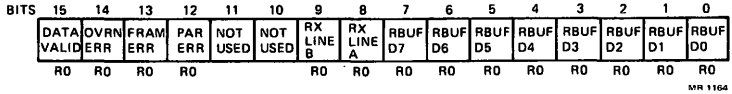


Figure 6 Receiver Buffer Bit Assignments

Table 4 RBUF Bit Assignments

Bit: 0-7 **Name:** Received Character
Description: These bits contain the received character, right-justified. The least significant bit is bit 0. Unused bits are 0. The parity bit is not shown.

Bit: 8-9 **Name:** Received Character Line Number
Description: These bits contain the line number on which the character was received. Bit 8 is the least significant bit.

Bit: 10-11 **Name:** Not used
Description:

Bit: 12 **Name:** Parity Error
Description: This bit is set if the sense of the parity of the received character does not agree with that designated for that line.

Bit: 13 **Name:** Framing Error
Description: This bit is set if the received character did not have a stop bit present at the proper time. This bit is usually interpreted as indicating the reception of a break.

Bit: 14 **Name:** Overrun Error
Description: This bit is set if the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer on that line.

Bit: 15 **Name:** Valid Data
Description: This bit, when set, indicates that the data presented in bits 0-14 is valid. This bit permits the use of a character-handling program that takes characters from the FIFO buffer until there are no more available. This is done by reading this register and checking bit 15 until the program obtains a word for which bit 15 is zero.

Line Parameter Register — The line parameter register (LPR) controls the operating parameters associated with each line in the DZV11. The LPR is a word-addressable, write-only register. The line parameters for all lines must be reloaded following an occurrence of either BINIT or device master clear. Table 5 lists bit assignments and the format is shown in Figure 7.

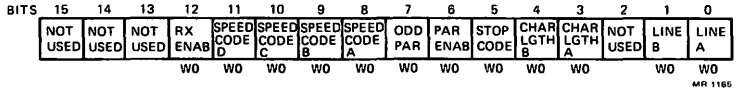


Figure 7 Line Parameter Register Bit Assignments

Table 5 LPR Bit Assignments

Bit: 0-1 **Name:** Parameter Line Number
Description: These bits specify the line number for which the parameter information (bits 3 through 12) is to apply. Bit 0 is the least significant bit.

This bit must always be written as a 0 when specifying the parameter line number. Writing this bit as a 1 will extend the parameter line number field into nonexistent lines. Parameters for lines 0 through 3 will not be affected.

Bit: 2 **Name:** Not used
Description:

Bit: 3-4 **Name:** Character Length

Description: These bits are set to receive and transmit characters of the length (excluding parity) shown below.

4	3	
0	0	5-bit
0	1	6-bit
1	0	7-bit
1	1	8-bit

Bit: 5 **Name:** Stop Code
Description: This bit sets the stop code length (0 = 1-unit stop, 1 = 2-unit stop, or 1.5-unit stop if a 5-bit character is used).

Bit: 6 **Name:** Parity Enable
Description: If this bit is set, characters transmitted on the line have an appropriate parity bit affixed; characters received on the line have their parity checked.

Bit: 7 **Name:** Odd Parity
Description: If this bit and bit 6 are set, characters of odd parity are generated on the line and incoming characters are expected to have odd parity. If this bit is not set but bit 6 is set, characters of even parity are generated on the line and incoming characters are expected to have even parity. If bit 6 is not set, the setting of this bit is immaterial.

Bit: 8-11 **Name:** Speed Code
Description: The state of these bits determines the operating speed for the transmitter and receiver of the selected line.

11	10	9	8	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	0	1	9600
1	1	1	1	Invalid

Bit: 12 **Name:** Receiver Enable
Description: This bit must be set before the UART receiver logic can assemble characters from the serial input line. This bit will be cleared following a BINIT or device master clear.

Bit: 13-15 **Name:** Not used
Description:

Transmitter Control Register — The transmitter control register (TCR) is a byte- and word-addressable register. The low byte of the TCR contains the transmitter control bits which must be set to initiate transmission on a line. Each TCR bit position corresponds to a line number. For example, TCR bit 0 corresponds to line 0, bit 1 to line 1, etc. Setting a TCR bit causes the transmitter scanner clock to stop if the UART for this line has a transmit buffer empty condition. An interrupt will then be generated if transmitter interrupt enable is set. The scanner clock will restart when either the transmit data register is loaded with a character or the TCR bit is cleared for the line on which the clock has stopped. TCR bits must only be cleared when the scanner is not running. The format is shown in Figure 8.

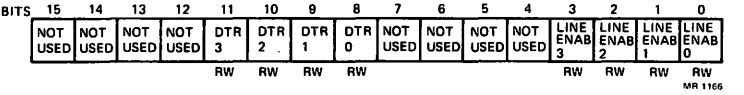


Figure 8 Transmitter Control Register Bit Assignments

The TCR bits are represented in bits 0 through 3. These bits are read/write and cleared by BINIT or device master clear. Bits 4 through 7 are unused and read as zero.

The high byte of the TCR contains the writable modem control lead, Data Terminal Ready (DTR). Bit designations are as follows.

Bit	Name
8	DTR Line 0
9	DTR Line 1
10	DTR Line 2
1	DTR Line 3
12-15	Unused. Read as zero

Assertion of a data terminal ready bit puts an ON condition on the appropriate modem circuit for that line. Data terminal bits are read/write and cleared only by BINIT. Jumpers have been provided to

allow the request to send circuits to be asserted with data terminal ready assertions.

Modem Status Register — The modem status register (MSR) is a 16-bit read-only register. A read to this register results in the status of the readable modem control leads, ring and carrier. The ON condition of a modem control lead is interpreted as a logical 1. Bits 4 through 7 and 12 through 15 are unused and read as a zero. Remaining bit designations are shown in Figure 9 and explained below.

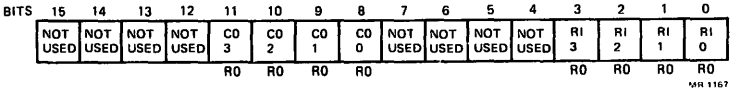


Figure 9 Modem Status Register Bit Assignments

Bit	Name
0	Ring Line 0
1	Ring Line 1
2	Ring Line 2
3	Ring Line 3
4-7	Unused. Read as zero.
8	Carrier Line 0
9	Carrier Line 1
10	Carrier Line 2
11	Carrier Line 3
12-15	Unused. Read as zero.

Transmit Data Register — The transmit data register (TDR) is a byte- and word-addressable, write-only register. Characters for transmission are loaded into the low byte. TDR bit 0 is the least significant bit. Loading of a character should occur only when Transmitter Ready (CSR bit 15) is set. The character that is loaded into this register is directed to the line defined in CSR bits 8 and 9. The high byte of the transmit data register is designated as the break control register. The bit designations are shown in Figure 10.

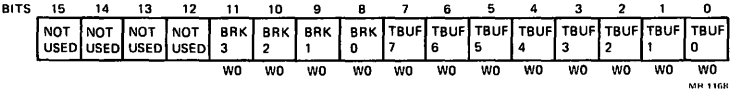


Figure 10 Transmit Data Register Bit Assignments

Each of the four multiplexer lines has a corresponding break bit for that line. TDR bit 8 represents the break bit for line 0, TDR bit 9 for line 1, etc. TDR bits 12 through 15 are unused. Setting a break bit will force that line's output to space. This condition will remain until cleared by the program. This register is cleared by BINIT or device master clear. The break control register can be used regardless of the state of the device maintenance bit (CSR bit 3).

PROGRAMMING

The DZV11 has several programming features that allow control of baud rate, character length, stop bits, parity, and interrupts. This section discusses the application of these controls to achieve the desired operating parameters.

Baud Rate

Selection of the desired transmission and reception speed is controlled by the conditions of bits 8-11 of the LPR. The baud rate for each line is the same for both the transmitter and receiver. The receiver clock is turned on and off by setting and clearing bit 12 in the LPR for the selected line.

Character Length

The selection of one of the four available character lengths is controlled by bits 3 and 4 of the LPR. The bit conditions for bits 4 and 3, respectively, are as follows: 00 (5-level), 01 (6-level), 10 (7-level), and 11 (8-level). For character lengths of 5, 6, and 7, the high-order bits of the received character are forced to zero.

Stop Bits

The length of the stop bits in a serial character is determined by bits 5 of the LPR. If bit 5 is a zero, the stop length is one unit; bit 5 set to a one selects a 2-unit stop unless the 5-level character length (bits 3 and 4 at zero) is selected, in which case the stop bit length is 1.5 units.

Parity

The parity option is selected by bit 6 of the LPR. Parity is enabled on transmission and reception by setting bit 6 to a one. Bit 7 of the LPR allows selection of even or odd parity, and bit 6 must be set for bit 7 to be significant. The parity bit is generated and checked by hardware and does not appear in the RBUF or TBUF. The parity error (bit 12, RBUF) flag is set when the received character has a parity error.

Interrupts

The Receiver Interrupt Enable (RIE) and Silo Alarm Enable (SAE) bits in the CSR control the circumstances upon which the DZV11 receiver interrupts the processor.

If RIE and SAE are both clear, the DZV11 receiver will not interrupt the processor. In this case, the program must periodcally check for the availability of data in the silo and empty the silo when data is present. If the program operates off a clock, it should check for characters in the silo at least as often as the time it takes for the silo to fill, allowing a safety factor to cover processor response delays and time to empty the silo. The RDONE bit in the CSR will set when a character is available in the silo. The program can periodically check this bit with a TSTB or BIT instruction. When RDONE is set, the program should empty the silo.

If RIE is set and SAE is clear, the DZV11 will interrupt the processor to the DZV11 receiver vector address when RDONE is set, indicating the presence of a character at the bottom of the silo. The interrupt service routine can obtain the character by performing a MOV instruction from the RBUF. If the program then dismisses the interrupt, the DZV11 will interrupt when another character is available (which may be immediately is additional characters were placed in the silo while the interrupt was being serviced.) Alternatively, the interrupt service routine may respond to the interrupt by emptying the silo before dismissing the interrupt.

If RIE and SAE are both set, the DZV11 will interrupt the processor to the DZV11 receiver vector when the Silo Alarm (SA) bit in the CSR is set. The SA bit will be set when 16 characters have been placed in the silo since the last time the program has accessed the RBUF. Accessing the RBUF will clear the SA bit and the associated counter. The program should follow the procedure described to empty the silo completely in response to a silo alarm interrupt. This will ensure that any characters placed in the silo while it is being emptied are processed by the program.

NOTE

If the program processes only 16 entries in response to each silo alarm interrupt, characters coming in while interrupts are being processed will build up without being counted by the silo alarm circuit and the silo may eventually overflow without the alarm being issued.

If the silo alarm interrupt is used, the program will not be interrupted if fewer than 16 characters are received. In order to respond to short messages during periods of moderate activity, the program should periodically empty the silo. The scanning period will depend on the required responsiveness to received characters. While the program is emptying the silo, it should ensure that DZV11 receiver interrupts are inhibited. This should be done by raising the LSI-11 processor priority. The silo alarm interrupt feature can significantly reduce the processor overhead required by the DZV11 receiver by eliminating the need to enter and exit an interrupt service routine each time a character is received.

The Transmitter Interrupt Enable (TIE) bit controls transmitter interrupts to the processor. If enabled, the DZV11 will interrupt the processor at the DZV11 transmitter interrupt vector when the transmitter ready (TRDY) bit in the CSR is set, indicating that the DZV11 is ready to accept a character to be transmitted.

Emptying the Silo

The program can empty the silo by repeatedly performing MOV instructions from the RBUF to temporary storage. Each MOV instruction will copy the bottom character in the silo so it will not be lost and will clear out the bottom of the silo, allowing the next character to move down for access by a subsequent MOV instruction. The program can determine when it has emptied the silo by testing the DATA VALID bit in each word moved out of the RBUF. A zero value indicates that the silo has been emptied. The test can be performed conveniently by branching on the condition code following each MOV instruction. The TST or BIT instruction must not access the RBUF because these instructions will cause the next entry in the silo to move down without saving the current bottom character. Furthermore, following a MOV from the RBUF, the next character in the silo will not be available for at least one μs. Therefore, on fast CPUs, the program must use sufficient instructions or NOPs to ensure that successive MOVs from the RBUF are separated by a minimum of one μs. This will prevent a false indication of an empty silo.

Transmitting a Character

The program controls the DZV11 transmitter through four registers on the QBUS: the control and status register (CSR), the line parameter register (LPR), the transmit control register (TCR), and the transmit data register (TDR).

Following DZV11 initialization, the program must use the LPR to specify the speed and character format for each line to be used and must set the Master Scan Enable (MSE) bit in the CSR. The program should set the Transmitter Interrupt Enable (TIE) bit in the CSR if it wants the DZV11 transmitter to operate on a program interrupt basis.

The TCR is used to enable and disable transmission on each line. One bit in this register is associated with each line. The program can set and clear bits by using MOV, MOVB, BIS, BISB, BIC, and BICB instructions. (If word instructions are used, the line enable bits and the DTR bit are simultaneously accessed.)

The DZV11 transmitter is controlled by a scanner which is constantly looking for an enabled line (line enable bit set) which has an empty UART transmitter buffer. When the scanner finds such a line, it loads the number of the line into the 2-bit transmit line number (TLINE) field of the CSR and sets the TRDY bit, interrupting the processor if the TIE bit is set. The program can clear the TRDY bit by moving a character for the indicated line into the TBUF or by clearing the line enable bit. Clearing the TRDY bit frees the scanner to resume its search for lines needing service.

To initiate transmission on an idle line, the program should set the TCR bit for that line and wait for the scanner to request service on the line, as indicated by the scanner loading the number of the line into TLINE and setting TRDY. The program should then load the character to be transmitted into the TBUF by using a MOVB instruction. If interrupts are to be used, a convenient way of starting up a line is to set the TCR bit in the main program and let the normal transmitter interrupt routine load the character into the TBUF.

NOTE

The scanner may find a different line needing service before it finds the line being started up. This will occur if other lines request service before the scanner can find the line being started. The program must always check the TLINE field of the CSR when responding to TRDY to ensure it loads characters for the correct line. Assuming the program services lines are requested by the scanner, the scanner will eventually find the line being started. If several lines require service, the scanner will request service in priority order as determined by line number. Line 3 has the highest priority and line 0 the lowest.

To continue transmission on a line, the program should load the next character to be transmitted into the TBUF each time the scanner requests service for the line as indicated by TLINE and TRDY.

To terminate transmission on a line, the program loads the last character normally and waits for the scanner to request an additional character for the line. The program clears the Line Enable bit at this time instead of loading the TBUF.

The normal rest condition of the transmitted data lead of any line is the 1 state. The break bits are used to apply a continuous 0 signal to the line. One bit in the TDR is associated with each line. The line will remain in this condition as long as the bit remains set. The program should use a MOVB instruction to access the BRK bits. If the program continues to load characters for a line after setting the break bit, transmitter operation will appear normal to the program despite the fact that no characters can be transmitted while the line is in the continuous 0 sending state. The program may use this facility for sending precisely timed 0 signals by setting the break bit and using Transmit Ready interrupts as a timer.

It should be remembered that each line in the DZV11 is double buffered. The program must not set the BRK bit too soon or the two data characters preceding the break may not be transmitted. The program must also ensure that the line returns to the 1 state at the end of the 0 sending period before transmitting any additional data characters. The following procedure will accomplish this. When the scanner requests service the first time after the program has loaded the last data character, the program should load an all-zero character. When the scanner requests service the second time, the program should set the BRK bit for the line. At the end of the zero sending period, the program should load an all-zero character to be transmitted. When the scanner requests service, indicating this character has begun transmission, the program should clear the BRK bit and load the next data character.

Data Set Control

The program may sense the state of the carrier and ring indicator signals for each data set and may control the state of the data terminal ready signal to each data set. The program uses two registers to access the DZV11 data set control logic. *There are no hardware interlocks between the data set control logic and the receiver and transmitter logic.* Any required coordination should be done under program control.

The Data Terminal Ready (DTR) bits in the TCR are read/write bits. Setting or clearing a bit in this register will turn the appropriate DTR signal on or off. The program may access this register with word or byte instructions. (If word instructions are used, the DTR and line enable bits will be simultaneously accessed.) The DTR bits are cleared by the INIT signal on the QBUS but are not cleared if the program clears the DZV11 by setting the CLR bit of the CSR.

The carrier (CO) and ring (RI) bits in the MSR are read-only bits. The program can determine the current state of the carrier signal for a line by examining the appropriate bit in the MSR. It can determine the current state of the ring signal by examining the appropriate bit of the ring register. The program can examine these registers separately by using MOVB or BITB instructions or can examine them as a single 16-bit register by using MOV or BIT instructions. The DZV11 data set control logic does not interrupt the processor when a carrier or ring signal changes state. The program should periodically sample these registers to determine the current status. Sampling at a high rate is not necessary.

Device Address Assignments

The device address assigned to the DZV11 resides in the floating address space according to appendix A. This address space ranges from 160010_8 to 163776_8. Each DZV11 requires increments of 10_8 address locations and the first option should be configured with an address of 160010_8. The initial configured address assumes that the system consists of only DZV11s in the floating address field. If the DUV11 option is also configured in the floating address field, assign the DZV11 an address which establishes a gap of 10_8 address locations between the last DUV11 and the first DZV11. For example: If the system consisted of one DUV11 located at 160010_8, the DZV11 should be configured with an address of 160030_8.

Interrupt Vector Address Assignments

The DZV11 device vector address is selected from the floating vector space according to appendix A. This space ranges from address 300_8 to address 776_8. Each DZV11 requires increments of 10_8 address locations for its two contiguous interrupt vectors. If the DZV11 is the only option in the floating vector area, configure it for a vector of 300_8. If there are options other than the DZV11 residing in the floating vector area, other configuration rules must be applied. When configuring the device vector, only the first vector address must be considered. The first vector, or base vector, must start on a zero boundary.

A zero boundary is one which has the three least significant bits equal to zero. The second vector is controlled by the first vector and data bit 2. Data bit 2 is generated by the M7957 hardware.

Any option ahead of DZV11 in the floating vector space which is not in the configuration should not occupy any vector space gap. For example, if only one DZV11 is in the system, the vector for the DZV11 should be 300.

Each DZV11 requires two interrupt vectors, one for the transmitter section and one for the receiver section. If simultaneous interrupt requests were generated from each section, the receiver section would have priority in placing its vector onto the LSI-11 bus. A receiver interrupt to address XX0 will be generated from having either a Receiver Done (CSR 7) or Silo Alarm (CSR 13) occurrence. A transmitter interrupt to address XX4 will be generated by Transmitter Ready (CSR 15). Additional prerequisites for generating interrupts are that the individual interrupt enable bits (CSR 6 and CSR 14) be set. The recommended method of clearing interrupt enable bits is first to raise the processor status word to level 4, next to clear these interrupt enable bits, and then to lower the Processor Status Word to zero. Using this method prevents false interrupts from being generated.

H780 POWER SUPPLY

GENERAL

Six H780 power supply options are available for use in system applicatons. The six models provide for a choice of input voltage (115 Vac or 230 Vac, nominal), and master console, slave console, or no console.

All models are used for supplying dc operating voltages to an LSI-11 bus backplane. In addition, each model generates a proper power-up/power-down sequence of BDCOK H and BPOK H LSI-11 bus signals. Master console-equipped and slave console-equipped models can be interconnected to allow control of both supplies from the master console.

FEATURES

- +5V ±3%, 18 A (maximum) and +12V ±3%, 3.5 A (maximum); combined dc power must not exceed 110 W.
- Overcurrent/short-circuit protection—Output voltages return to normal after removal of overload or short. Current limited to approximately 1.2 times the required maximum rating.
- Overvoltage protection—+5V limited to +6.3V (approximately); +12V limited to +15V (approximately).
- Line-time clock—A bus-compatible signal is generated by the power supply for the event (line-time clock) interrupt input to the processor. This signal is either 50 or 60 Hz, depending on primary power line frequency input to the power supply.
- Power-fail/automatic restart—Fault detection and status circuits monitor ac and dc voltages and generate bus-compatible BPOK H and BDCOK H signals (respectively) to inform the LSI-11 bus modules of power supply status.
- Fans—Built-in fans provide cooling for the power supply and modules contained in the system backplane.

SPECIFICATIONS

Input voltage (Continuously—see Note 1)
100-127 Vac (H780-C, -H, -K)
200-254 Vac (H780-D, -J, -L)

Temporary Line Dips Allowed
100% of voltage, 20 msec max

AC Inrush Current
70 A at 127V, 60 Hz (8.33 msec)
25 A at 254V, 50 Hz (10 msec)

Input Power (fans included)
340 W at full load max
290 W at full load typical

EMI (Emission and Susceptibility)
Per DEC STD 102.7 and VDE N-12 Limits

Input Protection
H780-C, -H, -K (100-127 Vac) fast blow, 5 A fuse
H780-D, -J, -L (200-254 Vac) fast blow, 2.5 A fuse

Hi-Pot
2 kV for 60 seconds from input to output, or input to chassis

Output Power (combinations not to exceed 110 W)
+5V, 1.5 A-18 A
+12V, 0.25 A-3.5 A

Maximum DC Current under Fault Conditions
+5V bus = 28 A
+12V bus = 9.5 A

+5V Output	
Total Regulation	5V ±3%
Line Regulation	±0.5%
Load Regulation	±1.0%
Stability	0.1%/1000 hours
Thermal Drift	0.025%/°C (See Note 2)
Ripple	150 mV p-p (1% for f <3 kHz)
Dynamic Load Regulation	±1.2% di/dt = 0.5 A μs delta I = 5 A
Noise	1 % peak at f > 100 kHz (noise is super-imposed on ripple)
Interaction due to +12V	±0.05%
+12V Output	
Total Regulation	12V ±3%
Line Regulation	±0.25%
Load Regulation	±0.5%
Stability	0.1%/1000 hours (See Thermal Drift Note 2) 0.025%/°C above 25°C

Ripple	350 mVp-p (1% for f <3 kHz)
Dynamic Load Regulation	±0.8% di/dt = 0.5 A μsec f<500 Hz delta I = 3 A
Noise	1 % peak at f > 100 kHz (noise is super-imposed on ripple)
Interaction due to +5V	±0.02%

Overvoltage Protection

+5V	6.3V nominal 5.65V min 6.8V max
+12V	15V nominal 13.6V min 16.5V max

Adjustments

+5V Output	4.05V-6.8V Guarantee Range 4.55-5.65V
+12V Output	10.6V-16.5V Guarantee range 11.7-13.6V

Controls

Rear Panel	AC ON/OFF switch
Front Console	DC ON/OFF switch HALT/ENABLE switch
(Master only)	LC ON/OFF switch
Console Indicators	DC ON RUN (Master) SPARE (Master only)

Backplane Signals

BPOK H	
BDCOK H	
BEVNT L	Transmitted
BHALT L	
SHRUN L	Received (Master only)

Mechanical

Cooling

Two self-contained fans provide 0.7140 m^3/min (30 ft^3/min) air flow.

H780

Size
13.97 cm w × 8.43 cm h × 37.15 cm l
(5-1/2 in w × 3-1/3 in h × 14-5/8 in l)

Weight
5.90 kg (13 lb)

Environmental

Temperature

Ambient	5° to 50° C (41° to 122° F)
Storage	−40° to +70° C (−40° to +158° F)

Humidity
90% maximum without condensation

NOTES

1. Operation from ac lines below 100V may cause the power supply to overheat because of decreased air flow from the cooling fans.
2. These parameters apply after 5 minutes of warmup and are measured with an averaging meter at the processor backplane terminal block under system loading.

DESCRIPTION

General

Six H780 power supply options are available for use in LSI-11 bus systems. Individual model numbers determine combinations of 115 or 230 Vac (nominal) primary power and selection of master console, slave console, or no console. Models are listed below.

H780 Model No.	Input Power	Console Description	Figure
H780-C	115V	None	1
H780-D	230V	None	1
H780-H	115V	Master	2
H780-J	230V	Master	2
H780-K	115V	Slave	3
H780-L	230V	Slave	3

The H780 master console contains RUN and DC ON indicators for monitoring the processor states, as well as DC ON/DC OFF, LTC ON/OFF, and ENABLE/HALT switches for controlling the processor. The slave console contains only a DC ON indicator for monitoring the status of the slave power supply.

In addition to producing dc operating voltages (+5V, 18 A and +12V, 3.5 A) for system components, the H780 power supply automatically sequences BPOK and BDCOK bus signals for proper power-up/power-down operation. The power supply can be used as a stand-alone unit or it can be used with a backplane. Built-in cooling fans provide forced air cooling for the H780, and, when mounted to an H9270 backplane, also provide cooling for the system modules mounted in the backplane. High-frequency, low-voltage switching regulators and a multiplexing scheme provide control of overcurrent, overvoltage, slow voltage buildup, low line voltage, and short-circuit protection.

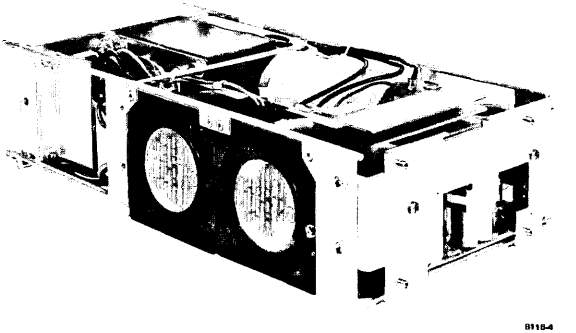


Figure 1 H780-C and -D Power Supplies

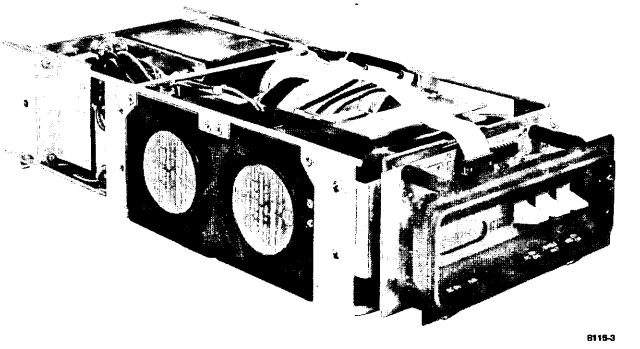


Figure 2 H780-H and -J Power Supplies

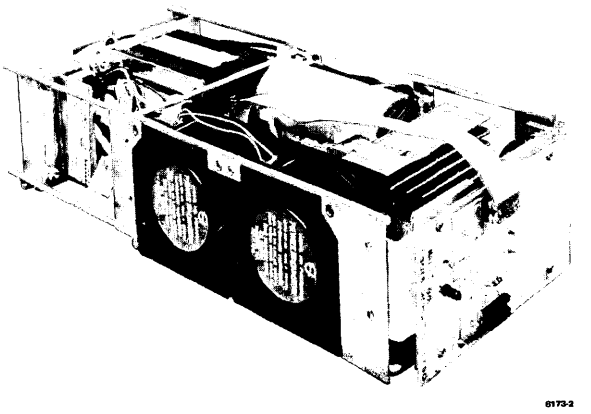


Figure 3 H780-K and -L Power Supplies

Figure 4 is a block diagram of the H780 power supply. AC line voltage is applied to the two cooling fans and to the power transformer. The transformer has dual primary windings to meet U.S. and European power requirements. A single secondary winding generates a stepped-down ac voltage which is rectified and filtered to produce 26 Vdc (nominal) unregulated. The unregulated 26 Vdc is applied to two 3-terminal regulators which produce −15V and +5V for the H780 internal circuits. Unregulated 26 Vdc is also applied to +5V and +12V high-frequency, high-efficiency switching regulators. The outputs of the +5V and +12V switching regulators supply operating power to the backplane. Each switching regulator circuit is designed for good frequency stability, high noise rejection levels, and excellent load and line regulation. An L-C output filter and a fast-recovery diode are used in each switching regulator circuit. The +5V switching regulator operates at a frequency from 7 kHz to 12 kHz, while the +12V switching regulator operates from 8 kHz to 14 kHz. Both switching regulator circuits are protected from overvoltage, overcurrent, and short-circuit outputs. In addition, failsafe short-circuit startup is provided, along with protection against a short between the +5V and +12V outputs. Logic signal generation circuits within the H780 provide for proper power sequencing of the processor, as well as the generation of the line-time clock (BEVNT L) and power supply status signals. H780-H and -J options are supplied with a console which contains RUN and DC ON indicators for monitoring the processor and power supply

states, as well as DC ON/DC OFF, LTC ON/OFF, and ENABLE/HALT switches for controlling the system. The H780-K and -L options have a console which contains only a DC ON indicator. H780-C and -D options have no console panel.

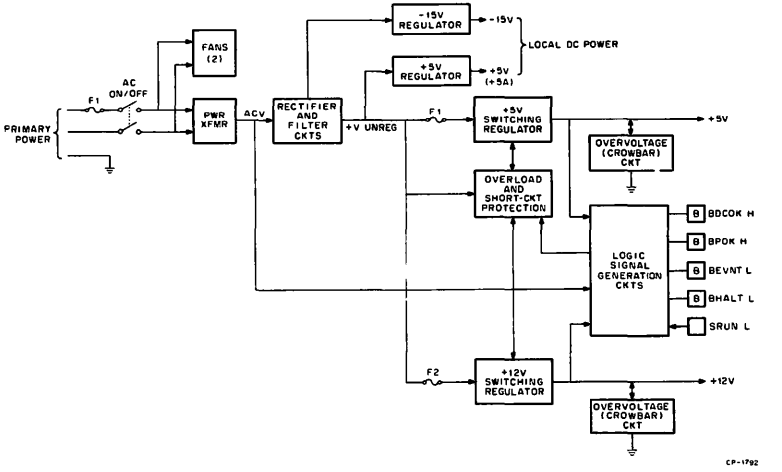


Figure 4 H780 Power Supply Block Diagram

Unregulated Voltage and Local Power Circuits — Unregulated voltage and local power circuits provide operating dc power for power supply logic and control circuits, and dc power for the +5V and +12V regulator circuits. These circuits are shown in Figure 5. AC power is supplied to the H780 via an ac input plug and cable. A toggle switch mounted on the rear of the H780 applies ac power to the power supply. Normally, this switch remains in the ON position, allowing ac power to be controlled by power distribution and control circuits external to the H780. Primary circuit overload protection is provided by a fuse mounted on the rear of the H780.

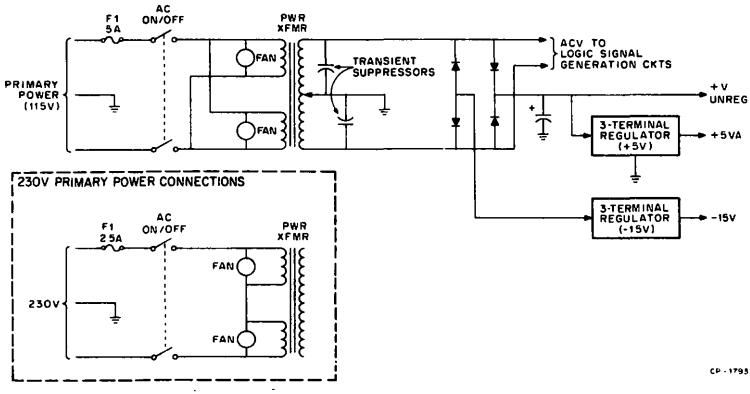


Figure 5 Unregulated Voltage and Local DC Power Circuits

Primary power circuits are factory-wired for 115 Vac (H780-C, -H, -K) or 230 Vac (H780-D, -J, -L) operation. Power transformer primary windings and the two fans operate directly from the switched ac power.

A single center-tapped secondary winding supplies power for regulator circuits and internal circuit operation. Conventional full-wave rectifiers and a −15V, 3-terminal regulator IC provide regulated voltage for internal distribution. The rectifiers also provide unregulated +30V (+V UNREG) for internal distribution and regulator operation. A 3-terminal regulator integrated circuit provides 5V +5 A power for H780 logic and control circuits. The +5V and +12V regulators use the same V UNREG voltage for regulation and distribution to the processor modules. AC voltage from one side of the transformer secondary is also routed to the line-time clock (LTC) circuit, which generates a BEVNT L bus signal for a line-time clock processor interrupt. When used with a 60 Hz line frequency, the interrupt occurs at 16.667 msec intervals; a 50 Hz line frequency will produce interrupts at 20 msec intervals.

+5V and +12V Switching Regulator Circuits — Both +5V and +12V regulator circuits receive the +V UNREG input power. The +5V and +12V regulator circuits are identical except for component values. Hence, only the basic +5V regulator is described in detail.

The basic regulator is a switching regulator which operates at approximately 10 kHz. The main controlling element is a 3-terminal regulator which operates at approximately the regulated output voltage level. Basic regulator circuits are shown in Figure 6. Note that the ground terminal of the 3-terminal regulator is connected to a circuit that allows adjustment of the terminal voltage over a −0.7V to +1.5V range. Hence, the 3-terminal regulator output in the +5V regulator circuit can range from 4.3V to 6.8V (approx).

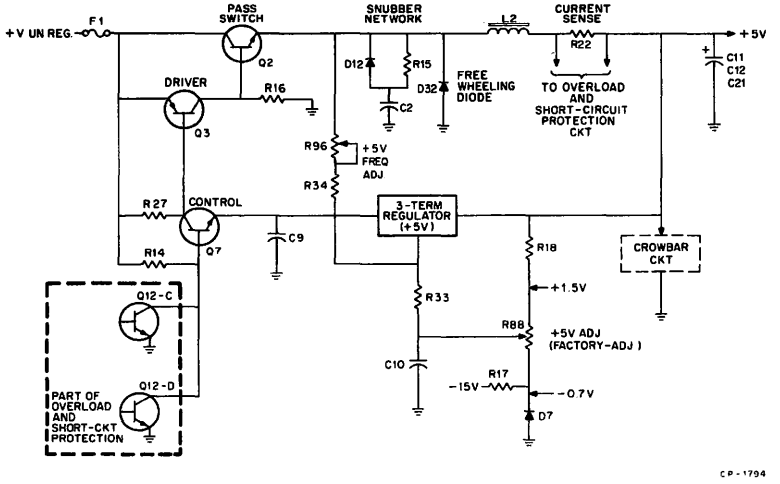


Figure 6 Basic Regulator Circuit

Normal switching regulator operation is accomplished when the control transistor is turned on. Forward-bias for the control transistor is supplied via R14. It is turned off only during fault conditions (overcurrent or shorted output voltage) or when the input ac line voltage is below specifications. Its emitter supplies unregulated voltage to the 3-terminal regulator. At less than 50 mA regulator output current (approximately), the 3-terminal regulator supplies the output voltage. However, as load current through the 3-terminal regulator is increased beyond this value, the voltage drop across R27 and forward-biases the driver transistor. The pass switch transistor then turns on and applies the +V UNREG to L2. The output capacitor then charges toward the

+5V value, current limited by the inductance of L2. When the output voltage rises to the 3-terminal regulator regulation voltage, the 3-terminal regulator turns off; current through R27 stops, and the driver transistor is not forward-biased. Hence, the driver and pass switch transistors cut off. The energy stored in L2 continues to charge the capacitor bank slightly beyond the designed output voltage via the free-wheeling diode and the current sense resistor. Once the inductor's stored energy is spent, the load discharges the output capacitor until the output voltage drops below the 3-terminal regulator's regulation voltage. At that point, current through R27 increases and turns on the driver and pass switch transistors, and the cycle repeats. Note that as the load is increased, the pass switch must remain on longer in order to charge the output capacitor to the regulated voltage value. This process repeats at a 7-12 kHz rate, producing the switching regulator operation.

Switching losses in the pass switch transistor are minimized by the snubber network. This network operates during the "off" switching transient (as the pass switch is biased-off) by controlling the rate of increasing collector to emitter voltage as collector current decreases.

The control transistor is turned off during a fault condition by overload and short-circuit protection circuits. When a fault condition is detected, the control transistor's base voltage drops to nearly 0V, causing it to cut off. When cut off, operating voltage is removed from the 3-terminal regulator and R27 current is 0, disabling the switching regulator circuit.

Overload and Short-Circuit Protection Circuits — Each H780 dc output is overload and short-circuit protected. When in an overload condition, excessive power supply current is sensed, causing both switching regulators to go off and then cycle on and off at a low-frequency rate (approximately 7.5 Hz) until the overload is removed. Each time the power supply cycles on, the circuit checks for the overload condition. If the load current returns to normal, the 10 kHz switching regulator operation resumes.

Overcurrent sensing circuits for +5 and +12 Vdc outputs are identical except for component values. A 5V power supply overcurrent condition results in an increased voltage drop across the current sense resistor (Figure 7), forward-biasing the current sense transistor. (During normal operation, this transistor is not forward-biased.) Current sense transistor collector (Q8) voltage then drops from near +V UNREG to the +5V regulator output value; this voltage, which is less than

the +13.8V reference applied to current limit comparator's inverting input, is diode-coupled to the comparator's non-inverting input, causing the comparator's output to go low; the diode coupling provides an OR logic function for both the +5V and +12V overcurrent fault conditions. The comparator's low output signal triggers the 50 μsec one-shot, whose OVERCURRENT L pulse output triggers the 135 msec one-shot and sets the Current Limit flip-flop. The OVERCURRENT L pulse is also ORed with the POWER OFF L signal, turning on the +5V and +12V hold-off transistors. Both switching regulators are then disabled. The high 135 msec one-shot output pulse is ANDed with the Current Limit flip-flop output, turning on +5V and +12V extended hold-off transistors. Hold-off signals remain in this state and inhibit switching regulator operation for the 135 msec pulse duration. At the end of this time, the 135 msec one-shot resets, terminating the delayed hold-off signals, and triggers the 2 msec one-shot. Its active low output resets the Current Limit flip-flop and clears the 135 msec one-shot for 2 msec, allowing the regulator pass switch transistors to operate for 2 msec (minimum). At the end of this time, the 135 msec one-shot is again enabled (the clear input goes high) and a new overcurrent cycle is enabled. If the overload is removed, normal operation resumes; otherwise, the overload causes a new overload condition to occur and the cycle repeats, as described above.

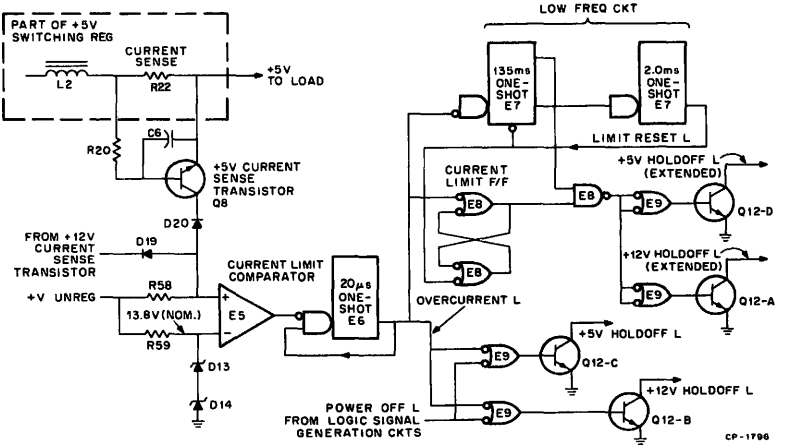


Figure 7 Overload and Short-Circuit Protection Circuits

Switching regulator operation is suspended when the operator places the DC ON/OFF switch in the OFF position. Logic signal generation circuits respond by immediately asserting BPOK H low to initiate a processor power-fail sequence. After a 5-10 msec "pseudo delay," POWER OFF L is asserted low. This low signal is wire-ORed with OVERCURRENT L, inhibiting the switching regulator operation, and dc power is removed from the backplane.

+5 V and +12 V Crowbar Circuits – Crowbar circuits are connected across both +5 V and +12 V power supply outputs for overvoltage protection. An overvoltage condition could occur if +12 V and +5 V outputs shorted together, or if a driver or switch transistor becomes shorted. When shorted to a higher voltage source, the crowbar fires, shorting the supply voltage that is protected to ground (dc return). In this condition, the overload and short-circuit protection circuits respond by limiting the duty cycle of the switch transistor until the overvoltage source is removed. However, when the overvoltage is caused by a shorted driver or switch transistor, short-circuit protection is ineffective, and the excessive current caused by the crowbar circuit firing will blow the regulator's fuse (F1 for +5 V or F2 for +12 V).

The crowbar circuit for the +5 V output is shown in Figure 8. It comprises a 5.6 zener diode D9, diode D8, programmable unijunction transistor Q9 and silicon-controlled rectifier Q15. Q15, R19, D8, and D9 supply the 6.1 Vdc (approx) crowbar reference (threshold) voltage to the gate of Q9 via R21. Q9 is normally off and its cathode supplies a 0 V gate input to Q15. An overvoltage will present a significantly higher voltage to the anode of Q9 (connected directly to +5 V) than to its gate (clamped by D8 and D9 to approximately 6.1 V). This triggers Q9 and its cathode voltage rises to the anode potential. Q15 then fires and shorts (crowbars) the supply output. The circuit remains in this condition until the overvoltage is removed (Q15 current goes to zero) and either the power supply switch transistor is off, due to short-circuit protection, or the regulator's dc fuse opens. Capacitor C7 decouples the gate of Q7 to prevent noise on +5 V from activating the crowbar.

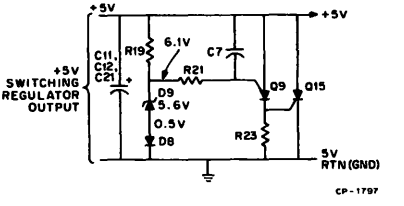


Figure 8 Crowbar Circuit

The +12 V crowbar circuit functions in a similar manner. However, the unijunction gate reference voltage for this power supply is approximately 13.5 V.

Logic Signal Generation Circuits – Logic signal generation circuits produce LSI-11 bus signals for power-normal/power-fail and line-time clock interrupt functions and processor Run-Enable/Halt mode. The RUN indicator circuit monitors the SRUN L backplane (nonbused) signal and provides an active display when the processor is in the Run mode. BPOK H and BDCOK H indicate power status. When both are high, power to the LSI-11 bus is normal and no power-fail condition is pending. However, if primary power goes abnormally low (or is removed) for more than 16.5 ms, BPOK H goes low and initiates a power-fail processor interrupt. If the power-fail condition continues for more than an additional 4 ms, a "pseudo delay" circuit causes BDCOK H to go low. The circuit also causes the overload and short-circuit protection circuit to inhibit +5 V and +12 V control transistors; normal output voltages are available for 50 μs (minimum) after BDCOK H goes low (depending on the loading of the dc output voltages). The DC ON/OFF switch simulates an AC ON/OFF operation by turning switching regulators on or off without turning system primary power off. A normal power-up/power-down sequence is produced by this circuit. The line-time clock circuit produces a processor interrupt at the power line frequency (either 50 or 60 Hz). The circuit simply asserts the BEVNT L line at the line frequency.

DC voltage monitor circuits respond to both +5 V and +12 V power supply outputs. A +2.5 V reference at the voltage comparator's noninverting input is established by +5 A and a voltage divider comprised of R25 and R3, as shown in Figure 9. Voltages are sensed at the anodes of diodes D17 and D35.

The sensed voltage to the voltage comparator's inverting input is normally 5 V, causing the comparator's output to go low. The low signal forward-biases DC ON panel indicator driver transistor Q10, producing a DC ON indication, and reverse-biases the BDCOK H FET bus driver Q6. As a result, Q6 cuts off, and its source voltage rises to +5 V, producing the active BDCOK H signal.

When either (or both) power supply output is 0 V, the voltage at the voltage comparator's inverting input is less than the +2.5 V reference. Hence, the comparator's output goes high, turning off the DC ON indicator and allowing Q6 to conduct. Q6 asserts the BDCOK H signal low, indicating that a dc power-fail condition exists. When normal power is restored, as during the power-up sequence, C37 charges via R50. When the C37 voltage exceeds the +2.5 V reference, the comparator's output then goes low (normal).

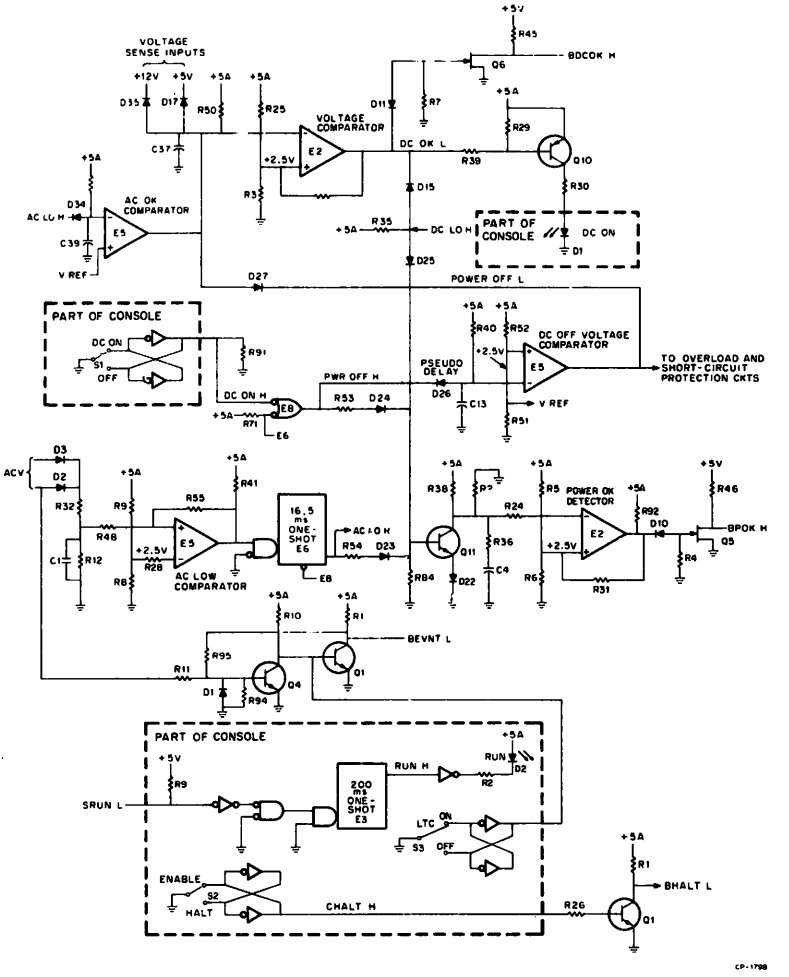


Figure 9 Logic Signal Generation Circuits

AC voltage monitor circuits include an ac low comparator, a 16.5 ms delay, and a BPOK H bus driver circuit, which is enabled only when BDCOK H is in the active (dc voltage normal) state. Rectifiers D2 and D3 produce positive-going dc voltage pulses at twice the ac line frequency. R32, R12, and C1 produce nominal +3.9 V (peak) normal line voltage

pulses which are coupled to the noninverting input of the ac low comparator via R48. R8 and R9 produce a +2.5 V reference for the comparator's inverting input. The comparator's normal output is a series of pulses occurring at twice the ac power line frequency. Each positive-going leading edge retriggers the 16.5 ms one-shot, keeping it in the set state. The 16.5 ms one-shot output is diode-ORed with DCOK L via diodes D25 and D23 and PWR OFF H via D24. Normally, the three signals are low and Q11 remains cut off. In this condition, C4 charges to +3.125 V via R36 and R38. This signal is then applied to the power OK comparator's inverting input via R24. Since the noninverting input is referenced to +2.5 V by voltage divider R5 and R6, the comparator's output goes low, biasing off FET Q5. Q5's source voltage then rises toward +5 V via R46, producing the active BPOK H signal. Power-up/power-down sequence timing is shown in Figure 10.

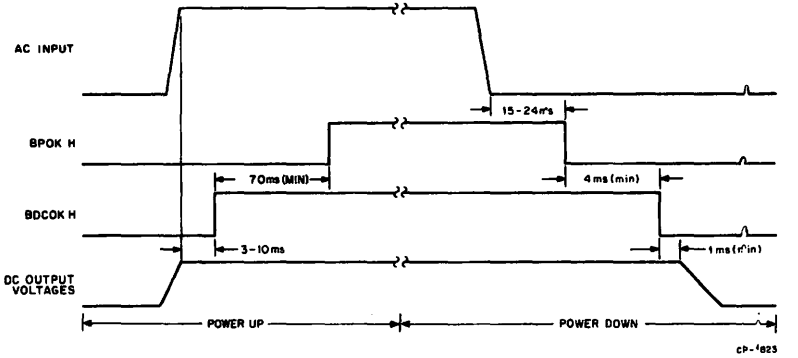


Figure 10 Power-Up/Power-Down Sequence

A power failure is first detected when the pulsating dc voltage at the ac low comparator's noninverting input is less than +2.5 V (peak). The comparator's output then remains low, allowing the 16.5 ms one-shot to go out of the retrigger mode. The one-shot resets 16.5 ms after the leading edge of the last valid ac voltage alternation; the 16.5 ms delay is equivalent to a full line cycle (two-alternate) failure. The high one-shot output is then coupled via D23 to the base of Q11, forward-biasing it.

Q11 conducts and rapidly discharges C4; R36 limits peak discharge current.

The low voltage thus produced is less than the +2.5 V reference at the power OK comparator's input, and its output goes high. Q5 then conducts and asserts the BPOK H signal low (power fail). The AC LO H

signal produced by the 16.5 ms one-shot is coupled via D34 to C39 on the inverting input of AC OK comparator E5. When C39's voltage rises above 2.5 V, the comparator's output goes low, turning off the DC ON indicator, negating BDCOK via the dc voltage monitor circuit, and turning off the regulator circuits by asserting POWER OFF L via D27.

When normal power is restored, the 16.5 ms one-shot returns to the retrigger (set) mode. AC LO H goes low and enables the dc voltage monitor and regulator circuits. The low AC LO H signal also removes forward bias from the base of Q11, cutting it off. Its collector voltage then rises as C4 charges at a relatively slow rate. R38 controls the charging rate of C4 and ensures that ac voltage and dc output voltages are normal for approximately 100 ms (70 ms minimum) before BPOK H goes high.

The DC ON/OFF switch simulates a power failure when it is placed in the OFF position. Cross-coupled inverters provide switch debounce protect on and a low (false) DC ON H signal is produced. This signal is inverted to produce a high PWR OFF H signal that is coupled via D26 to the "pseudo delay" circuit, causing a power-fail sequence to occur, and to Q11 via R53 and D24, causing BPOK H to go low (power-fail indication). After a 5–10 ms (approx) "pseudo delay," C13's voltage rises above the dc off voltage comparator's +2.5 V reference (noninverting) input. The comparator's output goes low, asserting POWER OFF L low and turning off the switching regulators. When the DC ON/OFF switch is returned to the ON position, PWR OFF H goes low, rapidly discharging C13. POWER OFF L then goes high and switching regulator operation resumes. Approximately 100 ms later, BPOK H goes high and normal processor operation is enabled. DC ON/OFF circuit timing is shown in Figure 11.

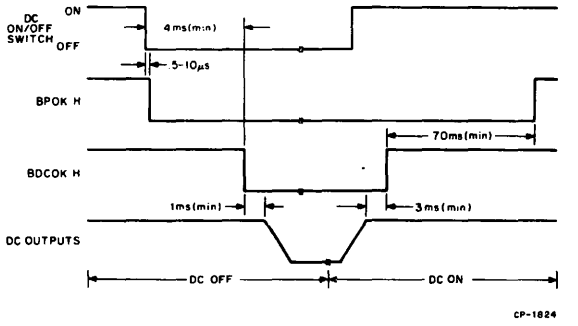


Figure 11 DC ON/OFF Circuit Timing

BEVNT L is the bused EVENT line which is normally used for line-time clock interrupts. Q4 is cut off and Q1 is forward-biased during negative alternations of the ac line, producing low-active BEVNT L signals. D1 clips negative alternations and limits Q4's reverse-bias to emitter voltage. The LTC ON/OFF switch must be in the ON position for BEVNT L signal generation. When the LTC function is not desired, the LTC switch is set to the OFF position; CSPARE2 goes low. Q1 remains cut off, and BEVNT L remains passive (high).

The RUN indicator is illuminated whenever the processor is executing programs. SRUN L, a nonbused backplane signal, is a series of pulses which occur at 3–5 μs intervals whenever the processor is in the Run mode. The pulses trigger a 200 ms one-shot on each SRUN L pulse leading edge, keeping it in the retrigger mode. Its high RUN H output signal is then inverted, producing a low signal that turns on the RUN indicator. When the processor is in the Halt mode, SRUN L pulses cease and the 200 ms one-shot resets after the 200 ms delay. The RUN indicator turns off, indicating the Halt mode.

The HALT/ENABLE switch allows the operator to manually assert the BHALT L signal low, causing the processor to execute console ODT microcode. When in the ENABLE position, BHALT L is not asserted, and the Run mode is enabled. Cross-coupled inverters provide a switch debounce function.

H780-C, -D, -H, -J, -K, -L Installation

Installation of an H780 power supply consists of inspecting the unit, connecting a suitable dc power cord, setting up the +5 and +12 Vdc outputs, and connecting the power supply to the system.

Differences Between 115 Vac and 230 Vac Power Supplies – The main differences between the 115 Vac H780 power supplies (H780-C, -H, and -K) and the 230 Vac H780 power supplies (H780-D, -J, and -L) are the ac input jumper configuration on the power supply terminal block (TB1), the fuse rating (115 Vac supplies are equipped with a 5 A fast-blow fuse; the 230 Vac supplies have a 2.5 A fast-blow fuse), and the power line RFI filter which is used only on the 230 Vac supplies. Power supplies factory-wired for 115 Vac operation (H780-C, -H, and -K) can be rewired for 230 Vac operation by reconfiguring the jumpers on TB1. However, European users of 115 Vac supplies should not rewire the H780-C, -H or -K for 230 Vac operation as these supplies will not meet the EMI requirements of VDE N-12. On the other hand, the 230 Vac supplies (H780-D, -J, and -L) can be rewired for 115 Vac and used in European countries as well as the U.S. AC wiring configurations for the H780 power supplies.

Space Requirements – The H780 power supply occupies a space 13.97 cm wide X 8.43 cm high X 37.15 cm long (5-1/2 in wide X 3-1/3 in high X 14-5/8 in long). Space should be available to the rear of the supply to gain access to the AC ON/OFF toggle switch. H780-H, -J, -K and -L options should be installed to allow for unobstructed viewing and use of the power supply console.

Input Power Requirements – The user's ac power source must be capable of providing 340 W (full load) of ac power at 50 ± 1 Hz or 60 ± 1 Hz. No ac power cord is supplied with the H780 options; it is the user's responsibility to provide the proper line cord and ac plug for his particular application.

Cable Requirements – Three interface cables are supplied with the H780 options to connect the H780 console to the power supply and to connect the H780 to the system backplane:

Cable	Digital Part No.
DC output cable (connects dc to backplane)	70-11584-0-0
Power supply status cable (logic cable) (connects logic signals to backplane)	70-11411-0K-0
Power supply console cable (connects console to H780)	70-08612-0M-0

Refer to the BA11-N description for multiple backplane interconnection information.

In addition, if the user is controlling an H780 slave power supply (H780-K or -L) from an H780 master (H780-H or -J), the interface cable between the master and slave is the user's responsibility. This cable can be constructed from 12-conductor ribbon cable and two 16-pin, IC-type male connectors (3M part number 3416). The master/slave cable can be ordered from the nearest Digital Equipment Corporation Sales Office Cable lengths and part numbers are listed in Table 1.

Installation Procedure – After unpacking the H780 from the shipping container, inspect the unit and report any damage to the nearest Digital Equipment Corporation Sales Office. Inspect for the following:

1. Damage to the chassis or printed circuit boards

Table 1 Master/Slave Interface Cables

Length	DIGITAL Part No.
10.2 cm (4 in)	70-08612-0D
15 cm (6 in)	70-08612-0F
22.9 cm (9 in)	70-08612-0K
27.5 cm (11 in)	70-08612-0M
35.6 cm (14 in)	70-08612-1B
45.7 cm (18 in)	70-08612-1F
124 cm (49 in)	70-08612-4A
61.0 cm (2 ft)	70-08612-02
1.83 m (6 ft)	70-08612-6A
3.05 m (10 ft)	70-08612-10

2. Loose or broken components

3. Damage to the console on the H780-H, -J, -K, or -L

4. Free rotation of the blades on the cooling fans

5. Proper amperage fuse (2.5 A fast-blow for H780-D, -J, and -L; 5 A fast-blow for H780-C, -H, and -K)

6. Proper seating of the fuse

7. Proper seating of the console cable connectors (H780-H, -J, -K, and -L)

8. The presence of the shield covering the terminal block at the rear of the H780.

Connecting AC Line Cord – The H780 power supplies are equipped with a terminal block (Figure 12) at the rear. Jumpers on this terminal block configure the supply for 115 Vac or 230 Vac operation while two of the terminal block screws provide a means of connecting ac input power to the H780. A suitable length of No. 16 AWG, 3-conductor, stranded power cord is to be connected to the terminal block as shown in Figure 12 (for H780-C, -H, and -K supplies), or Figure 14 (for H780-D, -J, and -L supplies). The jumpers shown in Figures 13 and 14 are factory-installed. However, the jumper configuration can be altered by the user to change the ac input from 115 V to 230 V for the H780-C, -H, and -K, or from 230 V to 115 V for the H780-D, -J, and -L. European users are advised not to operate an H780-C, -H, or -K power supply on a 230 Vac line as these supplies are not

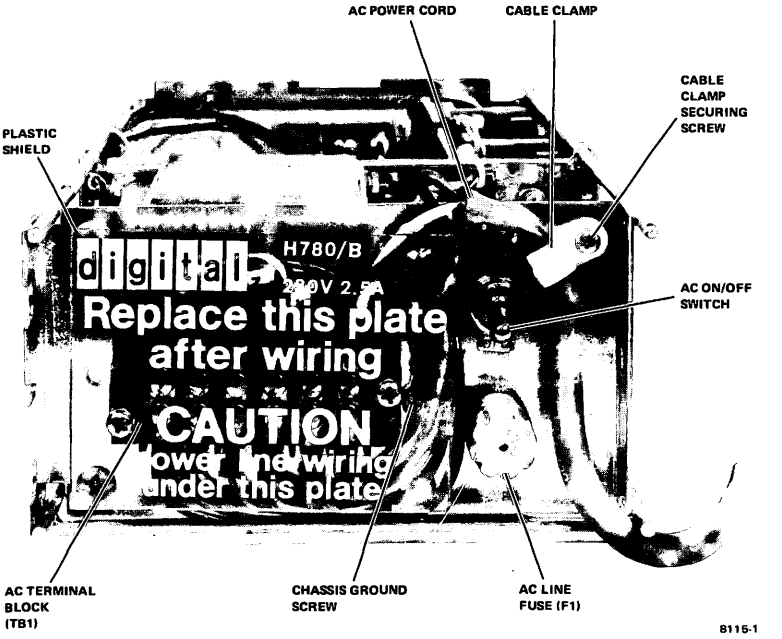


Figure 12 AC Terminal Block at Rear of H780

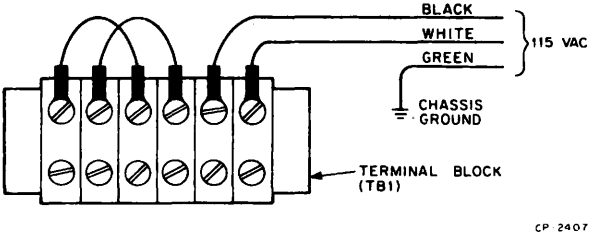


Figure 13 H780-C, -H, and -K (115 Vac) AC Terminal Block Wiring Configuration

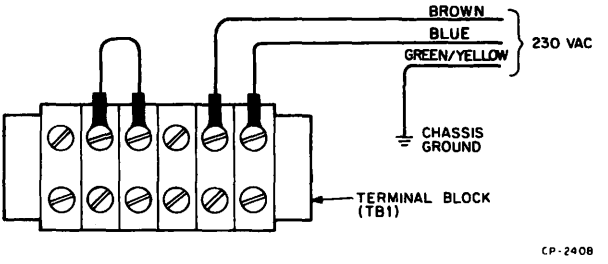


Figure 14 H780-D, -J, and -L (230 Vac) AC Terminal Block Wiring Configuration

equipped with a RFI line filter. When installing the ac line cord, remove the plastic shield covering the terminal block (Figure 12). Terminals should be crimped or soldered to the power cord wires. Connect the ac phase wires to the terminal block (Figures 13 and 14) and connect the ac ground wire to the H780 chassis using the Phillips head screw to the right of the terminal block (Figure 12). This screw also provides a ground for the RFI filter in the H780-D, -J, and -L supplies by means of a green/yellow wire. Make sure this wire is reconnected to ground when replacing the screw. Be sure to replace the plastic shield over the terminal block after completing the wiring. Route the power cord to the top of the H780 chassis and secure it to the chassis with a suitable strain relief, as shown in Figure 12 . The upper right screw at the rear of the H780 chassis can be used to anchor a cable clamp. The free end of the power cord should be terminated with a connector which is suitable for the user's requirements.

H780-C and H780-D Stand-Alone Operation – If an H780-C or -D power supply is to be used as a stand-alone supply, a 510 Ω, 1/4 W resistor must be installed between J2-2 and J2-9 on the power supply printed circuit board (Figure 15). The 510 Ω resistor provides a pull-up level to an internal power supply gate, thus enabling the +5 V and +12 V outputs. This resistor is not required for the H780-K or -L slave supplies, nor is the resistor required for the H780-H and -J supplies. The resistor can be installed by bending its leads and inserting them into socket J2, or by soldering the resistor across pins 2 and 9 of a 16-pin DIP, IC-type male connector. Pinning for the J2 enable plug is shown in Figure 16 .

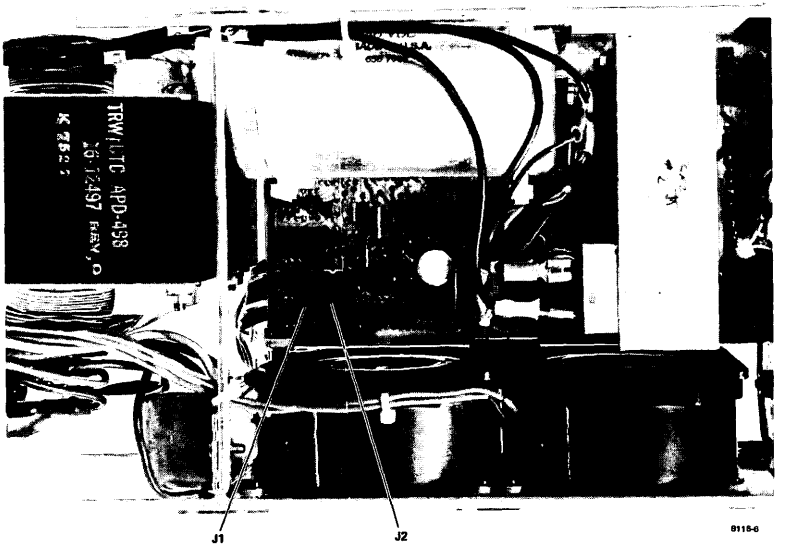


Figure 15 Locations of J1 and J2 on Power Supply Board

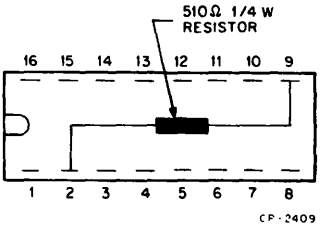


Figure 16 H780-C and -D Enable Plug

Initial Power Turn-On – Before connecting the dc output of the H780 to a system, verify the dc output voltages by performing the following procedure.

1. If the H780 is a slave supply (or an H780-C, -D), either connect cable J2 REMOTE of the slave H780 (or J2 on the power supply PC board of H780-C, -D) to the J2 REMOTE connector on the H780 master supply or install a 510 Ω 1/4 W resistor into the slave.

2. Connect the H780 to a suitable ac power source.

3. Set the H780 AC ON/OFF switch (Figure 12) to ON. The fans in the H780 should operate.

4. On H780-H and -J options, set the console DC ON/OFF switch (Figure 25) to ON. The DC ON indicator should light. (For master-slave operation, the DC ON/OFF switch and DC ON indicator are located on the user's master supply. The DC ON indicator on the slave should also light.)

5. Using a DVM, measure the +5 and +12 Vdc outputs at J4 (Figures 20 and 21) on the H780 PC board (side 2). The +5 V output should not be greater than +5.15 V and the +12 V output should not exceed +12.36 V.

6. Set the master console DC ON/OFF switch to the OFF position.

7. Set the AC ON/OFF switch to the OFF position.

8. Unplug the ac power cord and connect the H780 system.

Mounting an H780 to an H9270 Backplane – The H780 power supply is designed to be mounted to the LSI-11 H9270 backplane. Four holes on the left side of the H780 are equipped with No. 8-32 threaded bosses (Figure 17). These holes mate with four holes in the right side of the H9270 backplane frame. Four No. 8-32 X 1/2 inch screws are inserted through the H9270 backplane holes and are threaded into the H780 power supply. The H9270 backplane and the H780 power supply thus become one assembly (Figure 18). Figure 17 shows the location of the four mounting holes in the H780. The two screws securing the front-chassis partition must be removed. These screws are to be replaced with longer screws (1/2 in) when attaching the H780 to the H9270.

Connecting an H780 to an H9270 Backplane – The H780 power supply is connected to the H9270 by means of two cables. These cables are supplied with the H780. One of these cables is a 25.4 cm (10 in) logic signal cable (DIGITAL part number 70-11411-0K-0), which connects from J1 on the power supply board (Figure 15) to connector pins on the H9270 printed circuit board (Figure 19). Either end of this cable can be connected to the power supply or the backplane. The other cable is a 30.5 cm (12 in) dc output cable (part number 70-11584-0-0). This cable is terminated at one end with a keyed, 12-pin connector which mates with J4 on side 2 of the H780 power supply board. Figure 20 shows the location of J4; Figure 21 shows J4 pinning. The remaining end of the dc output cable is terminated with a 6-lug connector strip which is connected to the H9270 backplane terminal block,

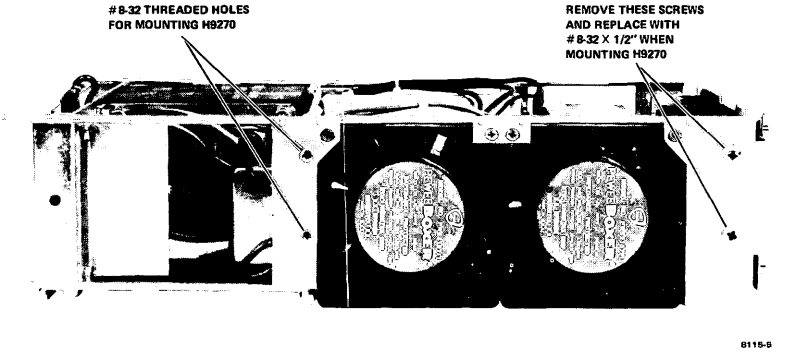


Figure 17 Left Side of H780 Showing H9270 Mounting Holes

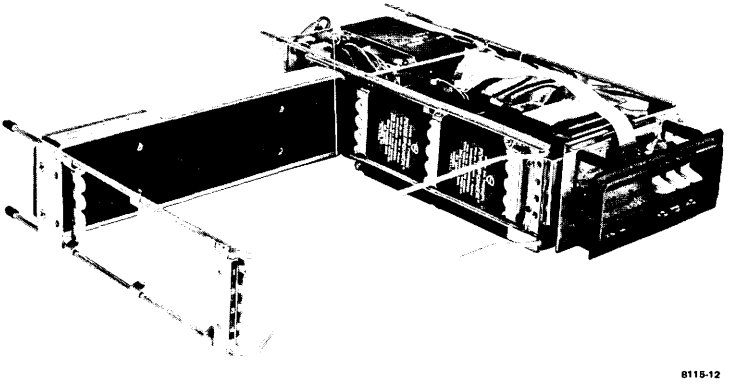


Figure 18 H780 Mounted to H9270 Backplane

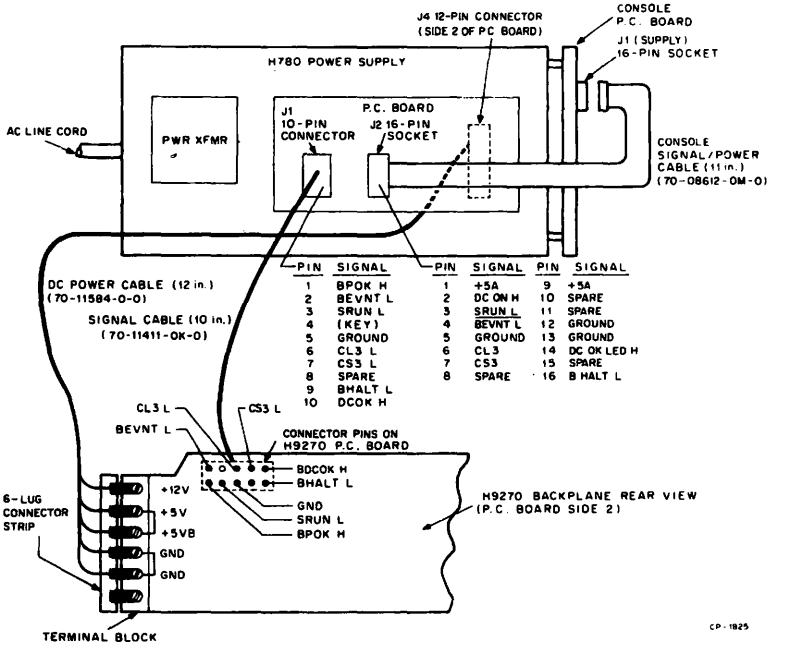


Figure 19 H780 to H9270 Backplane Connections

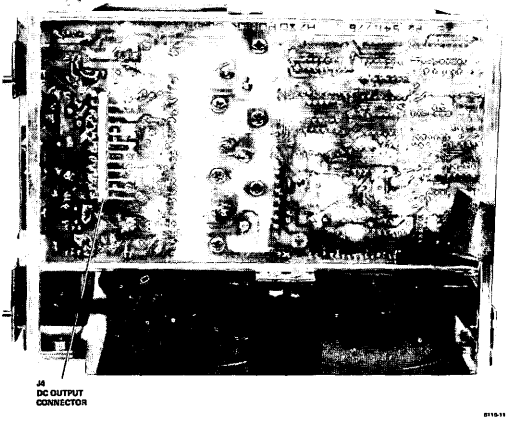


Figure 20 Location of H780 DC Output Connector (J4)

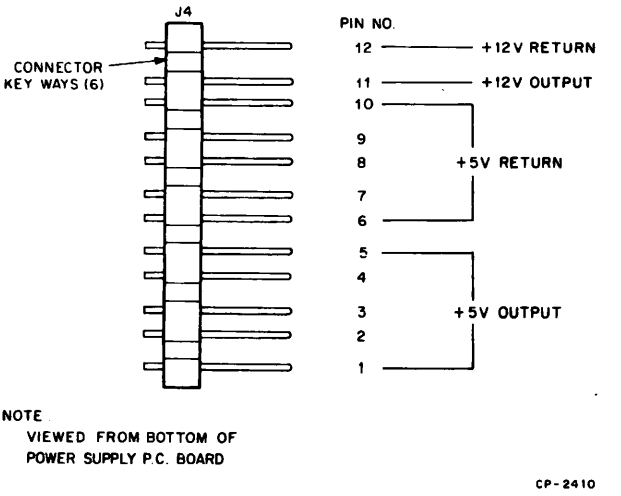


Figure 21 Pinning for H780 DC Output Connector (J4)

as shown in Figure 19. When connecting the 6-lug connector strip to the H9270 backplane, make sure that the spade lug connectors are facing up. Figure 22 shows the dc output cable connected to J4 of the H780. The H780 logic signal and dc output cables are routed toward the rear of the power supply and exit from the supply chassis next to the H9270 backplane terminal block.

H780-H, -J, -K, and -L power supplies have a console that is attached to the H780 and connected to the supply by means of a console signal/power cable (part number 70-08612-0M-0). This cable is factory-installed from J2 on the power supply board (Figure 15) to J1 on the console PC board (Figures 19 and 23).

H780 Master-Slave Connection – An H780-H or -J power supply can be used as a master supply to control an H780-K or -L slave supply. This master-slave arrangement allows the user to power up/power down system expander backplane logic from the master supply console. The slave supply is connected to the master supply by means of the J2 (REMOTE) connector on the master supply console printed circuit board, and J2 (REMOTE) or J3 on the slave power supply console printed circuit board. The interconnecting cable is the user's responsibility. Two 16-pin, IC-type male connectors and a suitable length of 16-conductor cable (preferably ribbon type) can be used to construct the interconnecting cable.

Figure 23 shows the console printed circuit boards and the locations of the J1 (SUPPLY), J2 (REMOTE), and J3 connectors. J1 is always connected to J2 of the power supply printed circuit board (Figure 19) by the console signal/power cable (part number 70-08612-0M-0) which is factory-installed. Pinning for J2 (REMOTE) on the console printed circuit board is shown in Figure 24. Pinning for J2 on the power supply printed circuit board is indicated in Figure 19.

Connector J3 (Figure 23) provides the means of interconnecting boxes in a multiple backplane system. This connector parallels connector J2, so a user can connect J2 on the slave BA11-M to J2 on the master PDP11/03 using the cable supplied with the first BA11-M expansion box, and can connect J3 on the first slave BA11-M to J2 on the second slave BA11-M using the cable supplied with the second BA11-M.

The slave console boards in the early model power supplies did not contain connector J3. Therefore, a single cable containing three DIP plugs (BC03Y-16) should be purchased to interconnect boxes in a multiple backplane system. Each DIP plug is inserted into connector J2 on each box.

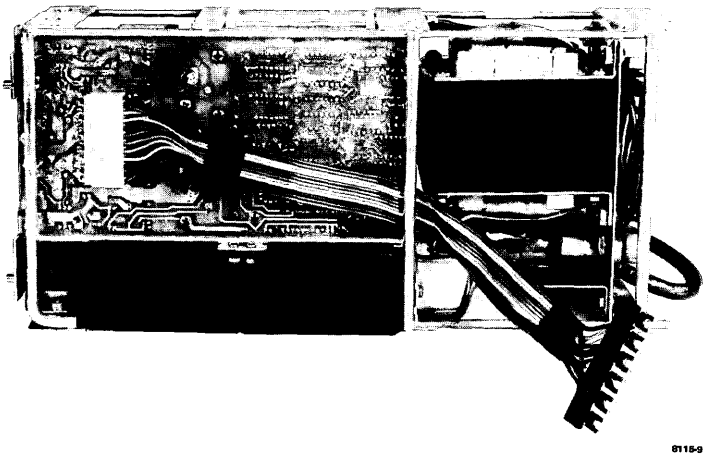
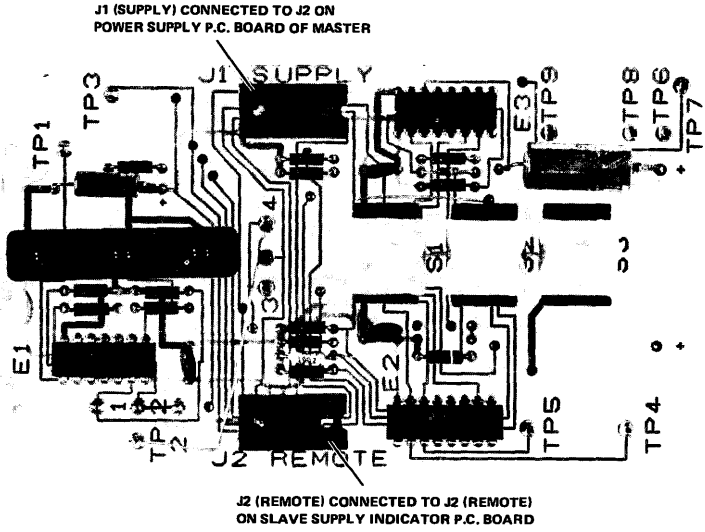
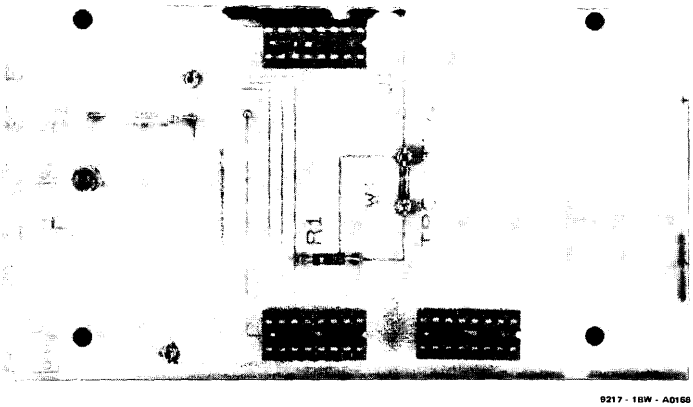


Figure 22 H780 DC Output Connector (J4) with Mating DC Output Cable (70-11584-0-0)



a. H780-H and -J (Master)

8115-2



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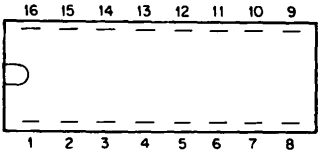
b. H780-K and -L (Slave)

Figure 23 H780 Master-Slave Connections



J2 (REMOTE)

PIN	SIGNAL	PIN	SIGNAL
1	NO CONNECTION	9	NO CONNECTION
2	DC ON H	10	SPARE 3
3	NO CONNECTION	11	SPARE 4
4	SPARE 2	12	SPARE 5
5	GROUND	13	GROUND
6	CL3 L	14	DC OK H
7	CS3 L	15	SPARE 6
8	SPARE 1	16	NO CONNECTION

CP-2411

Figure 24 Pinning for J2 (REMOTE) on Console Printed Circuit Board

Console Controls and Indicators – The H780-H or -J master console has three LED indicators and three 2-position toggle switches. One of the LED indicators is a spare indicator. Circuitry to drive this indicator is included on the console printed circuit board for user application. The console on the H780-K and -L slave supplies has only one LED indicator, DC ON. Figure 25 shows the H780 console controls and indicators; they are described in Table 2 . Additionally, the rear panel of the H780 contains an AC ON/OFF toggle switch and an ac line fuse (Figure 12).

+12 V and +5 V Adjustment Procedure – The H780 power supply is factory-adjusted to produce +12 V and +5 V outputs within the operating tolerance of the system. The adjustment procedures presented allow the user to trim the dc outputs of the H780 to meet his particular needs. One adjustment is provided for the +12 V output, while two adjustments (one for the output voltage and one for the switching regulator frequency) are provided for the +5 V. Figure 26 shows the location of the adjustments. A DVM, an oscilloscope, and a small screwdriver are required. Power supply loading is provided by the LSI-11 bus or processor.

Table 2 H780 Controls and Indicators

Control/ Indicator	Type	Function
DC ON	LED indicator	Illuminates when the DC ON/OFF toggle switch is set to ON and proper dc output voltages are being produced by the H780. If either the +5 or +12 V output from the H780 is faulty, the DC ON indicator will not illuminate. This is the only indicator on the H780-K and -L slave supplies.
RUN	LED indicator	Illuminates when the processor is in the run state (see ENABLE/HALT).
SPARE	LED indicator	Not used by the H780 or processor. The H780 contains circuitry for driving this indicator for user applications.
DC ON/OFF	Two-position toggle switch	When set to ON, enables the dc outputs of the H780. The DC ON indicator will illuminate if the H780 dc output voltages are of proper values. If a slave supply is connected to a master, the slave DC ON indicator will light if the slave dc output voltages are of proper value. When set to OFF, the dc outputs from the H780 are disabled and the DC ON indicator is extinguished. If a slave supply is connected to a master, the slave DC ON indicator will also extinguish.

Table 2 H780 Controls and Indicators (Cont)

Control/ Indicator	Type	Function
ENABLE/HALT	Two-position toggle switch	When set to ENABLE, the B HALT L line from the H780 to the processor is not asserted and the processor is in the Run mode (RUN indicator illuminated). When set to HALT, the B HALT L line is asserted, allowing the processor to execute console ODT microcode (RUN indicator extinguished).
LTC ON/OFF	Two-position toggle switch	When set to ON, enables the generation of the line-time clock (LTC) BEVNT L signal by the H780. When set to OFF, disables the H780 line time clock.
AC ON/OFF (rear panel)	Two-position toggle switch	When set to ON, applies ac power to the H780. When set to OFF, removes ac power from the H780.
FUSE (rear panel)	5 A or 2.5 A fast-blow	Protects H780 from excessive current. H780-C, -H, and -K use a 5 A fuse, H780-D, -J, and -L use a 2.5 A fuse.

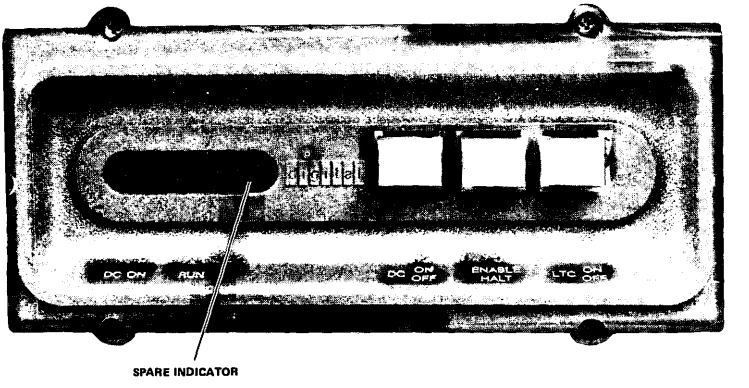


Figure 25 Console Controls and Indicators

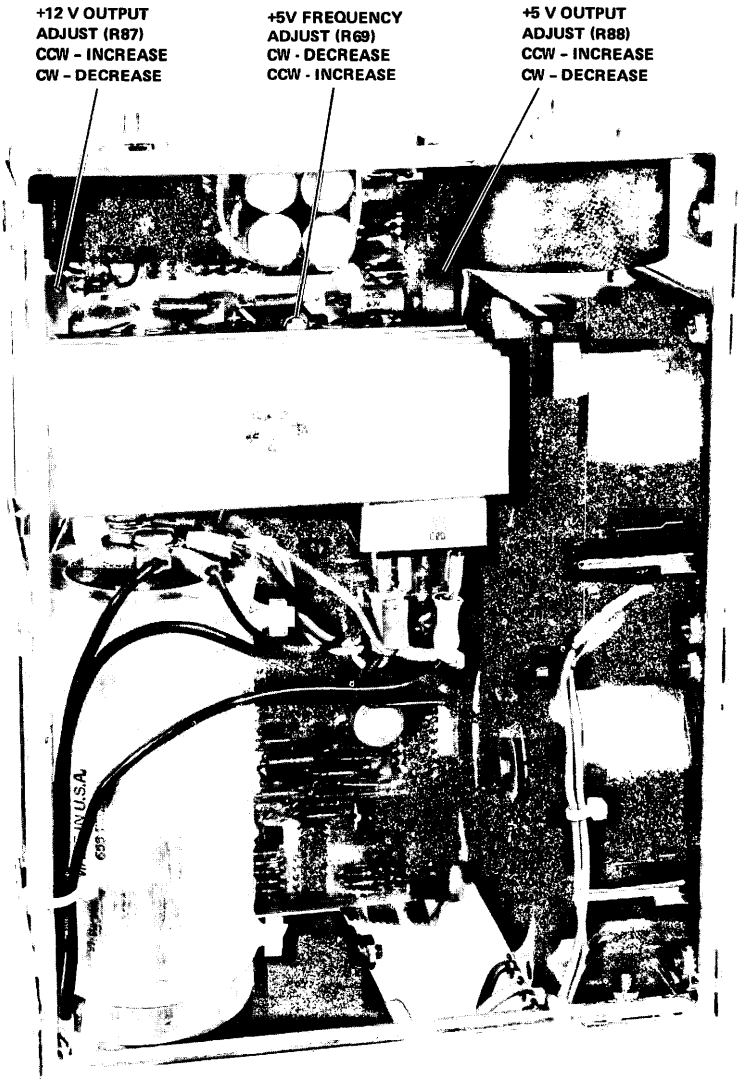


Figure 26 Locations of H780 Adjustments

+12 V Adjustment – Perform the following procedure when adjusting the +12 Vdc output.

1. Apply power to the system and allow a 5-minute warmup period.
2. Using a DVM, measure the +12 V output at the system backplane terminal block (Figure 19).
3. Using a small screwdriver, adjust R87 (Figure 26) until the DVM indicates +12.0 V (+11.64 V to +12.36 V acceptable range). Turning R87 clockwise decreases the +12 V output, while turning counterclockwise increases the output.

NOTE

If R87 is turned too far counterclockwise, the +12 V output will crowbar and drop to approximately 0 V. This will occur between +13.0 V and +16.5 V. Do not allow the supply to crowbar as this may blow the internal fuse (F1) protecting the +12 V regulator.

4. Using an oscilloscope, measure the ripple on the +12 V output at the backplane terminal block. The ripple should not be greater than 350 mV peak-to-peak.
5. Using an oscilloscope, measure the amplitude and frequency of the ripple on the +12 V output at the backplane terminal block. The ripple should not be greater than 350 mV peak-to-peak with a period from 65–140 μs. If the ripple period is not within 80–140 μs, adjust R37 to +12 V.

+5 V Adjustment – Perform the following procedure when adjusting the +5 Vdc output.

1. Apply power to the system and allow a 5-minute warmup period.
2. Using a DVM, measure the +5 V output at the system backplane terminal block (Figure 4-50).
3. Using a small screwdriver, adjust R88 (Figure 26) until the DVM indicates +5.0 V (+4.85 V to +5.15 V acceptable range). Turning R88 clockwise decreases the +5 V output, while turning counterclockwise increases the output.

NOTE

If R88 is turned too far counterclockwise, the +5 V output will crowbar and drop to approximately 0 V. This will occur between +5.6 V and +6.8 V. Do not allow the supply to crowbar as this may blow the internal fuse (F2) protecting the +5 V regulator.

4. Using an oscilloscope, measure the amplitude and frequency of the ripple on the +5 V output at the backplane terminal block. The ripple should not be greater than 150 mV peak-to-peak with a period from 80–140 μs. If the ripple period is not within 80–140 μs, adjust R96 (Figure 26). Turning R96 clockwise decreases the ripple period, while turning counterclockwise increases the period. After adjusting the ripple period, recheck the +5 V output (steps 2 and 3).

H909-C

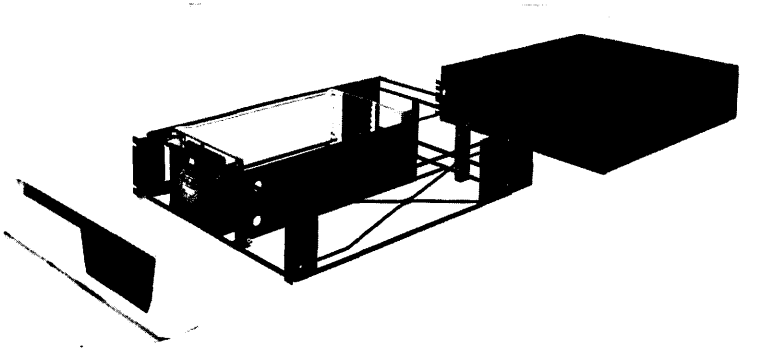
H909-C GENERAL PURPOSE LOGIC ENCLOSURE

GENERAL

The H909-C is one of the three basic enclosures available: the H909-C enclosure, the BA11-M expansion box and the BA11-N mounting box.

SPECIFICATIONS

Width	48.25 cm (19 in.)
Height	13.33 cm (5.25 in.)
Depth	62.86 cm (24.75 in.) 70.48 cm (27.50 in.) including bezel
Weight	27.21 kg (60 lb.)
Mounting Space for Power Supplies	12.7 cm × 15.8 cm × 50.8 cm (5 in. × 6.25 in. × 20 in.)



7920-48W-A0168

Figure 1 H909-C Enclosure

H909-C

DESCRIPTION

The H909-C is a general purpose logic box designed to accommodate the DDV11-B backplane or any one of several different standard logic subsystems (Figure 1). In addition, with the use of compatible logic frames and connector blocks, it can house custom-configured subassemblies. The box features a distinctive front panel that can be drilled for lights and switches as desired by the user. A fan is provided for cooling capability and ample room is reserved for power supply installation.

CONFIGURATION

A detailed description of each, including application and configuration information, is presented in the following table. The various options available are listed below.

Options	Voltage (V)	Bezel*	Includes	Mounting
H909-C	—	No	Fan and H0341 card guide	—
PDP-11/03-XA	115	Yes	X=E: KD11-F	BA11-MC or BA11-MD
PDP-11/03-XB	230	Yes	X=K: KD11-R	BA11-MC or BA11-MD
PDP-11/03-LC	115	Yes	KD11-R and BDV11-A	BA11-NC or BA11-ND
PDP-11/03-LD	230	Yes	KD11-R and BDV11-A	BA11-NC or BA11-ND
BA11-ME	115	No	Cable to daisy chain	
BA11-MF	230	No	Power supply	
BA11-NE	115	No		
BA11-NF	230	No		

* Including switches

H984 SERIES CABINETS

GENERAL

H984 series is one of two types of low-profile cabinets available: the H984 series and the H9800-A. The H984-BA (115 Vac) and the H984-BB (230 Vac) are low-profile cabinets equipped with a walnut-grained, plastic laminate top surface and four ball-type casters mounted on a supporting frame for ease of positioning on solid or carpeted surfaces. The cabinets are a light gray steel enclosure trimmed in flat black to make them compatible with the decor of the modern office or laboratory.

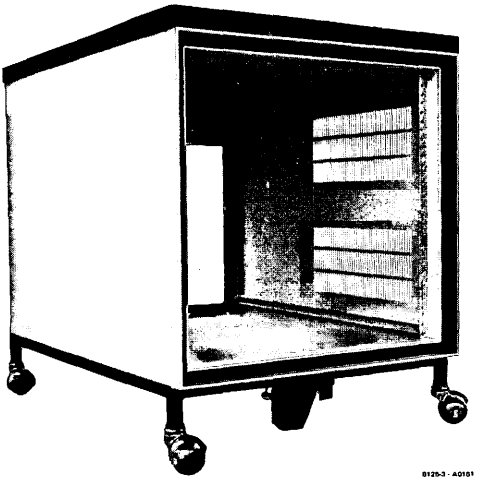


Figure 1 H984 Series Cabinet

SPECIFICATIONS

Dimensions	59.7 cm (23.50 in)
Width	71.3 cm (28.06 in)
Depth	54.6 cm (21.50 in)
Height	
Module enclosure	Standard 48.3 cm (19 in) EIA
Mounting space	59.7 cm (23.50 in)
Usable height	61.7 cm (24.28 in)
Usable depth	44.6 cm (17.56 in)
Color	Walnut-grained top surface, light gray side panels, chrome and flat black trim

H984

Description	Part No.	Shipping Weight
Low-Profile Cabinet (115 Vac)	H984-BA	31.8 kg (70 lb)
Low-Profile Cabinet (230 Vac)	H984-BB	31.8 kg (70 lb)
Optional Hardware		
Blower Fan (115 Vac)	70-12438-0	3.6 kg (8 lb)
Blower Fan (230 Vac)	70-12438-1	3.6 kg (8 lb)
Blank Connector Panel (back)	74-17440	2.3 kg (5 lb)
Louvered Cover Panel (front)	12-11474-0	0.45 kg (1 lb)
Blank Metal Cover (front)	H950-NC	1.8 kg (4 lb)
Connector Panel Frame (back)	74-16743	
Connector Panel Assembly (back)	70-12871	

DESCRIPTION

Each H984 provides mounting space for standard 48.3 cm (19 in.) panels or racks at both the front and rear of the unit. Two vertical angles at the front and rear opening of the enclosure contain pre-drilled holes at EIA spacing. The angles can be laterally positioned within the cabinet to adjust for mounting units with varying depths. Both sides of the steel enclosure contain ventilation ports to allow cooling of the internal components.

A service leg with caster is located beneath the center of the unit and can be easily extended and retracted. The service leg provides stability to the cabinet when slide-mounted chassis are withdrawn from the front of the cabinet. When not in use, the leg retracts into the channel.

A 115 Vac power distribution panel is supplied with the cabinet and is mounted at the top of the rear opening of the cabinet. The panel can be easily repostioned to accomodate internal chassis when required.

Optional Equipment

Fan Panel Assembly — A fan panel assembly with two enclosed rotary fans is available as an option and provides additional cooling for the electrical components in the cabinet. The assembly is prewired with a cord and male connector which can be inserted into one of the outlets on the power control panel (part of the H984 cabinet). The fan assembly is available for 115 Vac or 230 Vac. The panel is supplied with hardware for mounting.

Black Plastic Front Cover — A flat black, plastic louvered cover panel, 4.45 cm (1.75 in) high, can be used to complete the covering at the

front of the H984. The panel slots allow increased air flow through the cabinet.

Blank Connector Panel — The blank connector panel is designed to completely enclose the rear opening of the H984 when the blower fan assembly option is included. This provides a surface for mounting interface cable connectors or cable openings. The panel is supplied with hardware for mounting.

Blank Metal Panel — A light gray blank metal cover panel, 8.9 cm (3.5 in) high, can be ordered to complete the covering at the front of the cabinet. The color is the same as the PDP-11/03 front panel and H984 cabinet.

Connector Panel Assembly — A hinged connector, preformed for mounting up to eight cable connectors, encloses the remainder of the H984 rear opening when the fan assembly is included.

H9270 BACKPLANE

GENERAL

The H9270 consists of an 8-slot backplane with a card guide assembly. This backplane is designed to accept up to eight double-height modules (including processor), four quad modules, or a combination of quad and double-height modules. When used for bus expansion in multiple backplane systems, the H9270 provides space for up to six option modules, plus the required expansion cable connector module(s) and/or terminator module.

DESCRIPTION

Mounting the Backplane

Mounting dimensions and possible methods of mounting the H9270 backplane (in any of three planes) are shown in Figure 1. Option positions are shown in Figure 2. Slot numbers indicate device interrupt and DMA priority in LSI-11 bus systems. The lowest numbered positions receive the highest priority.

DC Power Connections

Voltage and Current Requirements — A power supply for a single H9270 backplane LSI-11 system should have the following capacity:

+5V ±5% load; 0-18 A static/dynamic
+12V ±3% load; 1-2.5 A static/dynamic
+5 ripple; less than 1% of nominal voltage
+12 ripple; less than 150 mV p-p (frequency 5 kHz)

NOTE

Regulation at the H9270 backplane must be maintained to the specifications listed above

The H780 power supply option provides sufficient dc power and generates the required bus signals. Installation details are included in the H780 power supply description.

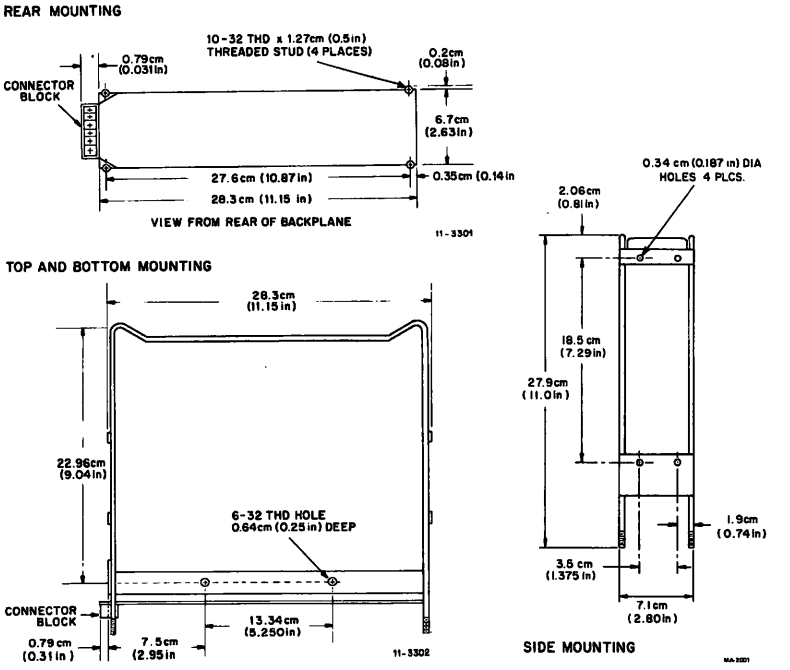


Figure 1 Backplane Mounting

VIEW FROM MODULE SIDE OF BACKPLANE

PROCESSOR (HIGHEST PRIORITY LOCATION)	PROCESSOR OR OPTION 1	1
OPTION 3	OPTION 2	2
OPTION 4	OPTION 5	3
OPTION 7 (LOWEST PRIORITY LOCATION)	OPTION 6	4

PREFERRED LOCATION FOR MMV11-A CORE MEMORY

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Figure 2 H9270 Option Positions

A power supply for a DDV11-B, or a multiple-backplane system using H9270 backplanes, should have the same voltage regulation and ripple specification as listed for the single H9270 backplane. However, it will be necessary to calculate the actual power requirements, based on individual power requirements for modules used in the system.

Backplane Power Connections — If the H780 power supply option is not used, perform the following steps to connect power to the H9270 backplane (Figure 3).

1. Select wire size. (14 gauge is recommended.) Consider load current and distance between the power supply and backplane.
2. For a standard system, connect the applicable wires to the H9270 connector block per Table 1.

   For battery backup, remove the jumper between +5V and +5B and connect the applicable wires to the H9270 connector block.
3. Connect the ground terminals at the power source.
4. It is recommended that the backplane frame/casting be electrically connected to the system/power supply ground.

The signal connections to the H9270 backplane are shown in Figure 4.

Table 1 H9270 Backplane Standard Power Connections

Power Source (From)		H9270 Connector Block (To)
+12V	+12V	
+5V	+5V	Factory
	+5B	Connected
GND	GND	Factory
GND	GND	Connected
−12V	−12V	This voltage is not required. The connection is available for custom interfaces.

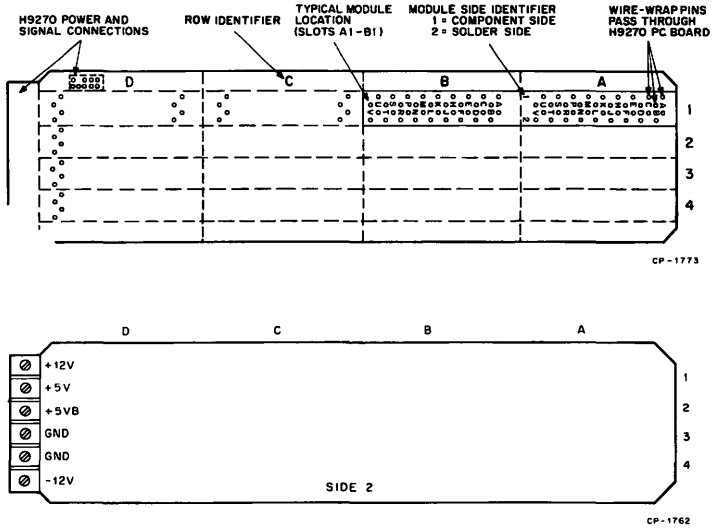


Figure 3 H9270 Backplane Terminal Block (Pin Side View Shown)

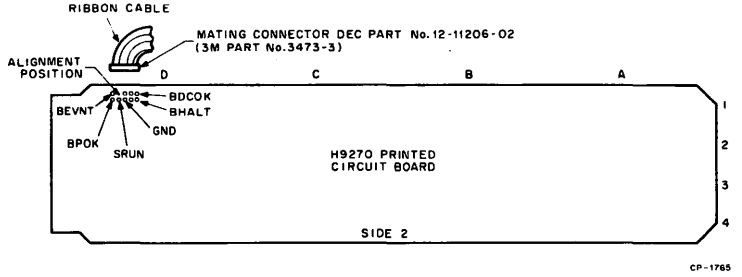


Figure 4 H9270 Backplane Signal Connections (Pin Side View Shown)

CONFIGURATION

Backplane and Module Configuration

LSI-11 bus systems can be classified as either single-backplane or multiple-backplane systems. The electrical characteristics of each system are different; hence, two sets of rules have been devised and must be observed. These rules have their basis in bus loading and power consumption.

Single Backplane Configuration Rules

1. The LSI-11 bus can support up to 20 ac loads, if unterminated at the end.
2. The terminated bus can support up to 35 ac loads.
3. The bus can support up to 20 dc loads.
4. The amount of current drawn from each power supply should be 70 percent or less of the maximum rated output of the supply.

Multiple Backplane Configuration Rules

1. No more than three backplanes can be connected together.
2. Each backplane can have no more than 20 ac loads.
3. The total number of dc loads cannot be more than 20.
4. Both ends of the termination line must be terminated with 120 ohms, i.e., the first backplane must have an impedance of 120 ohms, and the last backplane must have a termination of 120 ohms.
5. The cable connecting the first two backplanes (i.e., the main box and expander box 1) must be at least 60.96 cm (2 ft.) long. (A 182.88 cm (6 ft.) cable is recommended for ease of installation.)
6. The cable connecting the backplane of expander box 1 to the backplane of expander box 2 must be at least 121.92 cm (4 ft.) longer or shorter than the cable connecting the main box and expander box 1 (a 304.80 cm (10 ft.) cable is recommended for ease of installation).
7. The combined length of both cables in a 3-backplane system cannot exceed 487.68 cm (16 ft.).
8. The interbackplane cables must have a characteristic impedance of 120 ohms.
9. The amount of current drawn from each power supply should be 70 percent or less of the maximum output of the supply.

To configure an LSI-11 bus system, take the following steps:

1. Choose the type of memory (MOS, PROM or combination) required for the specific application.
2. Select the CPU and memory combination most suited for the application.
3. Select additional memory, interface, and peripheral options.
4. Count the total number of module positions.
5. Count the total number of bus positions.
6. Choose a backplane configuration that satisfies both the module position requirement, the bus position requirement, and also provides sufficient expansion space.
7. Enter the option names in the backplane positions of the selected configuration.

H9273-A BACKPLANE

GENERAL

The H9273-A backplane logic assembly consists of a 9 × 4 backplane (nine rows of four slots) and a card frame assembly.

DESCRIPTION

The H9273-A backplane logic assembly is shown in Figure 1. Power and signals are supplied to the backplane to conncectors J7 and J8. These connectors are shown in Figures 1, 2 and 3. Connectors J9 (GND) and J10 (−12V) are also shown in Figure 2.

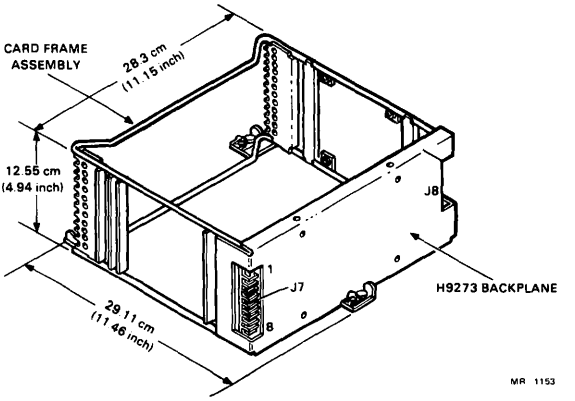


Figure 1 H9273-A Backplane Logic Assembly

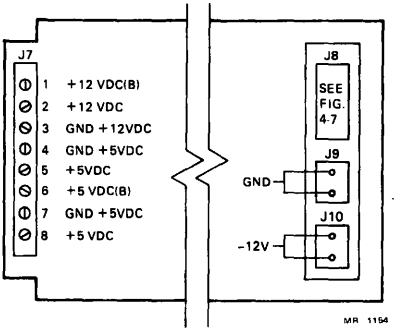


Figure 2 H9273-A Power Connections

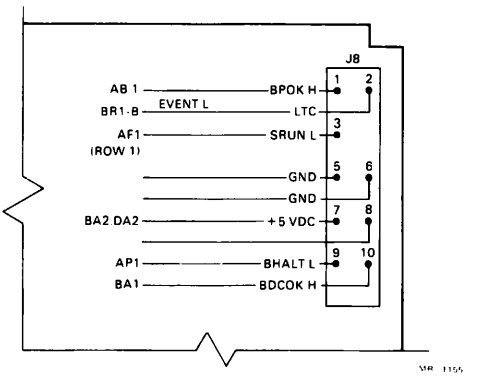


Figure 3 H9273-A Signal Connections

The H9273-A backplane is designed to accept both double-height and quad-height modules with the exception of the MMV11-A core memory module. The backplane structure is unique in that it provides two distinct buses: the LSI-11 bus signals (slots A and B) and the CD bus (slots C and D). The connectors that make up this backplane are arranged in nine rows (Figure 4). Each connector has two slots, each of which contains 36 pins, 18 on either side of the slot.

The connectors designated "Connector 1" in Figure 4 are wired according to the LSI-11 bus specifications. Slots A and B carry the LSI-11 bus signals and are termed the LSI-11 bus slots. The connectors designated "Connector 2" are wired for +5 V and ground, and have no connections to the LSI-11 bus; instead, C- and D-slot pins on side 2 of each row are connected to the C- and D-slot pins on side 1 in the next lower row. Details of the CD interconnection scheme are depicted in Figure 5.

CONFIGURATION

The H9273-A backplane logic assembly is designed to mount into a BA11-N mounting box or equivalent. Refer to the BA11-N mounting box description for more information.

NOTE

Connector block pins do not extend beyond the H9273-A printed circuit etch card, thus eliminating the possibility of backplane wire-wrapping.

Three jumpers (W1, W2, and W3) are shown in Figure 4. Jumper W1 enables the line-time clock when inserted and disables it when removed.

NOTE

Only one BA11-N mounting box in any system may have the line-time clock enabled.

When inserted, jumpers W2 and W3 allow the LSI-11 quad-height CPU to run in row 1. Jumpers W2 and W3 are removed when the backplane is used as an expansion backplane in a system.

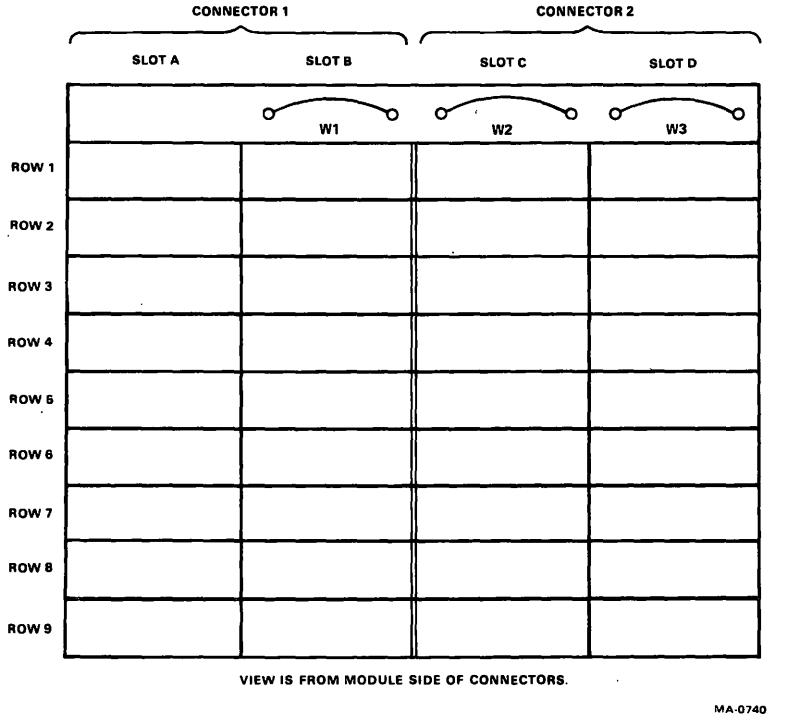
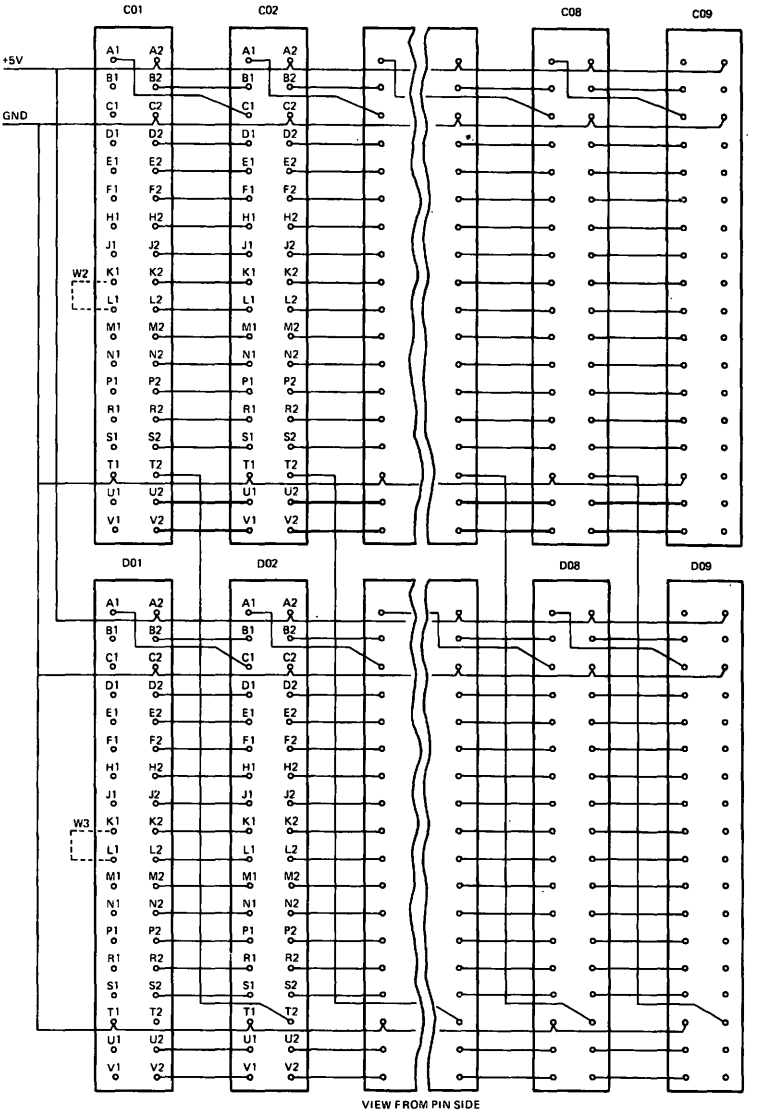


Figure 4 H9273-A Backplane Connectors



FEATURES:

- ALL PINS A1 CONNECT TO PINS C1 IN THE NEXT LOWEST SLOT.
- ALL PINS A2 CONNECT TO +5 VOLTS.
- ALL PINS T2 OF SLOT C ARE CONNECTED TO PIN T2 OF SLOT D IN THE NEXT LOWER SLOT.
- ALL PINS C2 AND PINS T1 ARE GROUND
- JUMPER W2 IS CONNECTED ACROSS PINS K1 AND L1 IN SLOT C ONLY.
- JUMPER W3 IS CONNECTED ACROSS PINS K1 AND L1 IN SLOT D ONLY.

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Figure 5 C-D Bus Interconnection Scheme

H9281 BACKPLANE

GENERAL

The H9281 backplane is designed to accept double-height modules only. Six options of the H9281 backplane let the user configure compact LSI-11 bus systems that most efficiently use available system space.

DESCRIPTION

The H9281 2-slot backplane is available in the following six options:

Backplane Option Designation	Description
H9281-AA	4-module backplane
H9281-AB	8-module backplane
H9281-AC	12-module backplane
H9281-BA	4-module backplane and card cage assembly
H9281-BB	8-module backplane and card cage assembly
H9281-BC	12-module backplane and card cage assembly

The following list presents quad-height options that are too large to be installed in an H9281 backplane.

Backplane Option Designation	Module Number	Description
AAV11-A	A6001	4-channel 12-bit D/A converter
ADV11-A	A0121	16-channel 12-bit A/D converter
DRV11-B	M7950	DMA interface
DUV11-A	M7951	Line interface
DZV11-A	M7957	Asynchronous multiplexer
KWV11-A	M7952	Programmable line-time clock
MMV11-A	H223, G653	Core memory
MSV11-CD	M7955-YD	16K MOS memory
RLV11	M8013 M8014	RL01 controller
BDV11	M8012	Bootstrap, terminator

CONFIGURATION

Mounting dimensions for H9281 backplanes are shown in Figures 1 and 2. The H9281 backplanes can be mounted in any plane. The enclosure in which the backplane is mounted, available system space, and cooling air flow will determine an acceptable backplane position in a particular system.

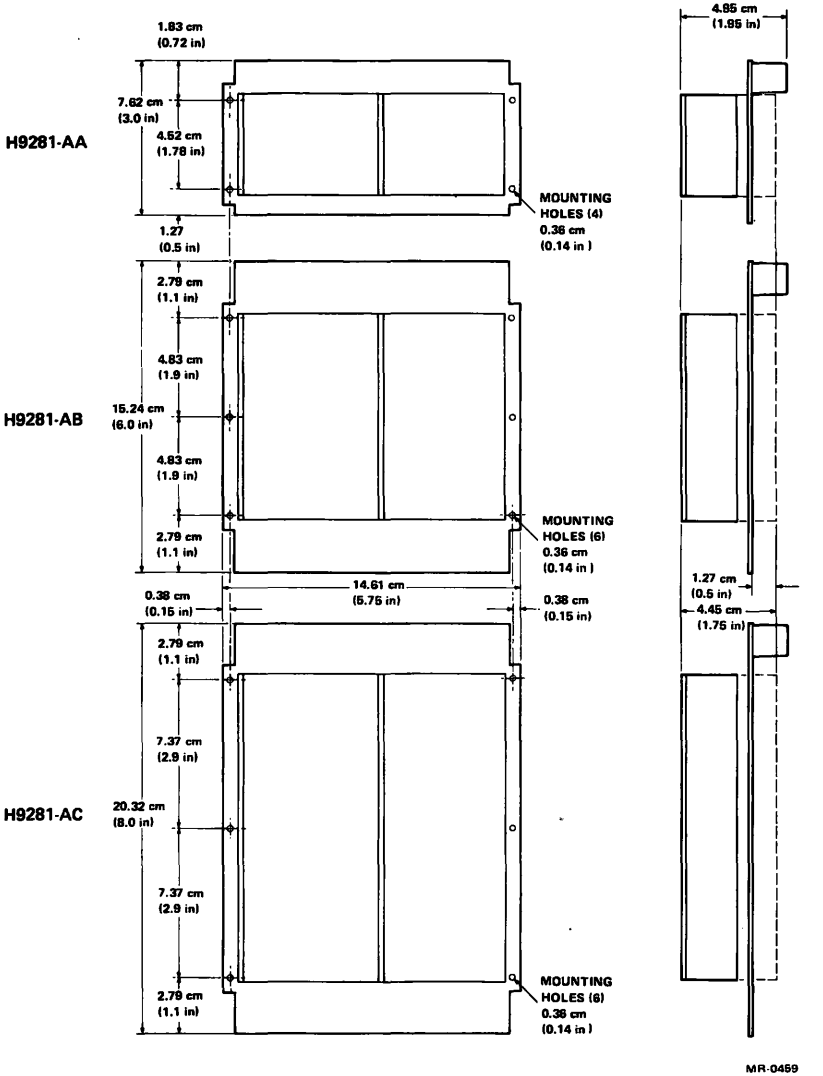

Figure 1 H9281-AA,-AB,-AC Mounting Dimensions

MODEL	MOUNTING DIMENSION A	ASSEMBLY LENGTH B
H9281-BA	6.86 cm (2.7 in)	7.62 cm (3.0 in)
H9281-BB	11.94 cm (4.7 in)	15.24 cm (6.0 in)
H9281-BC	17.02 cm (6.7 in)	20.32 cm (8.0 in)

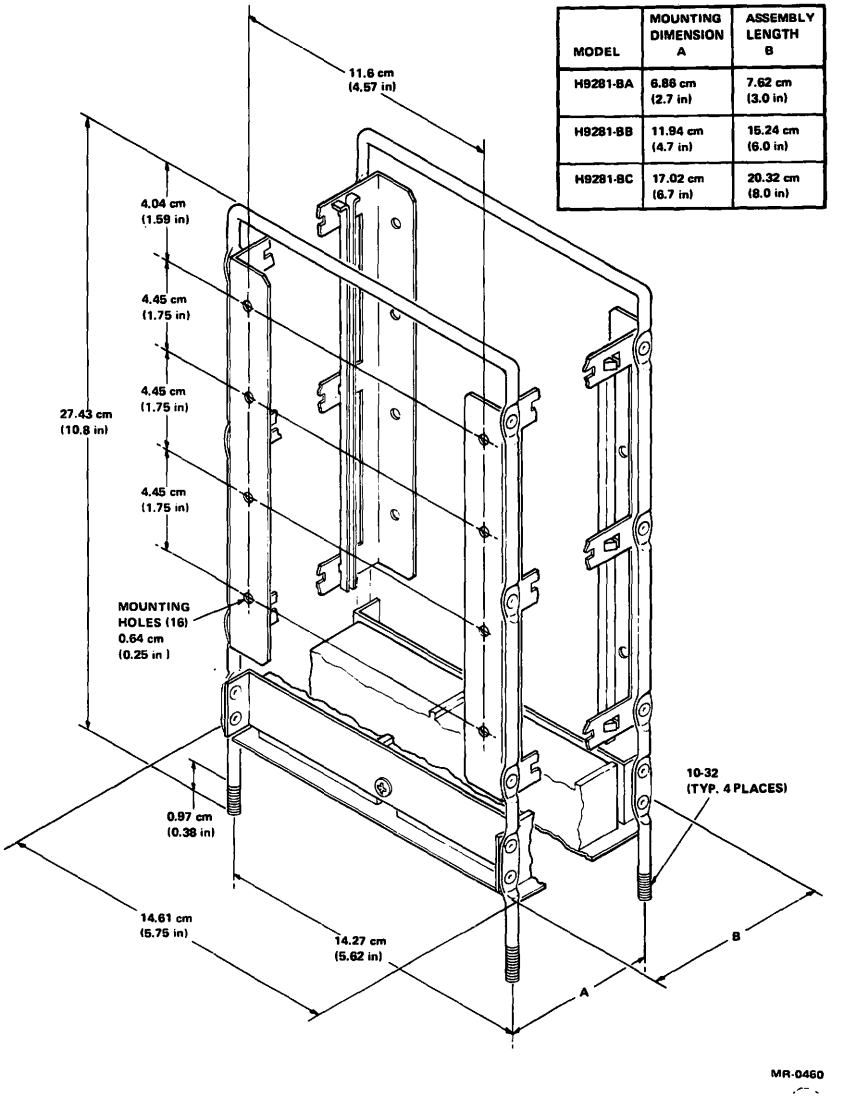

Figure 2 H9281-BA,-BB,-BC Mounting Dimensions

Connecting System Power

Seven screw terminals are provided on the slot 1 end of the backplane for power connections. Connect system power (and optional battery backup power) as shown in Figure 3. Power wiring should be done with a wire gauge appropriate for the total power requirements for options installed in the backplane. The recommended wire size for H9281-AC and -BC backplanes is 12 gauge. 14 gauge is sufficient for the other H9281 models.

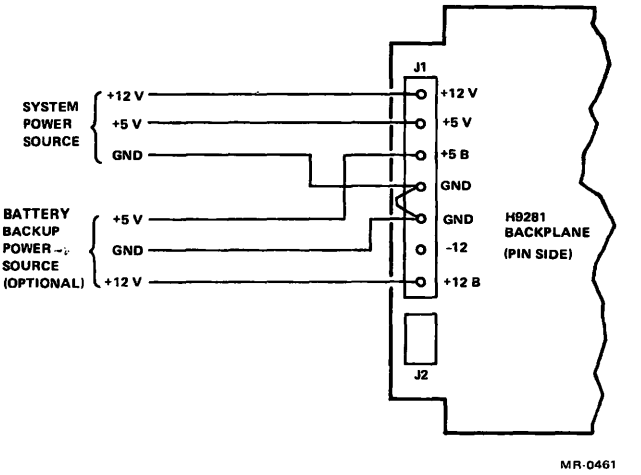

Figure 3 H9281 Power Connections

Select a power supply that will meet LSI-11 system power specifications and supply sufficient current for the options in the system. The H780 power supply is recommended.

Connecting Externally Generated Bus Signals

Externally generated bus signals can be connected to the H9281 backpanel via connector J2. These signals include power sequence signals BPOK H, BDCOK H, BHALT L and BEVNT L. In addition, the processor-generated SRUN L signal is available via J2 for driving a RUN indicator circuit. J2 connector pins are fully compatible with the H780 model series power supply or the KPV11-A power-fail/line-time clock. Signal connector J2 pinning and signal names are identified in Figure 4.

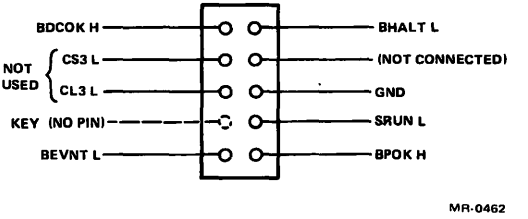

Figure 4 H9281 Signal Connections (J2)

Device Priority

All LSI-11 bus backplanes are priority structured. Daisy-chained grant signals for DMA and interrupt requests propagate away from the processor from the first (highest priority device) to successively lower priority devices. Processor module locations and device (option) priorities are shown in Figure 5.

Bus Terminations

Backplane models H9281-AB, -BB, -AC, and -BC include 120 Ω bus termination resistors at the electrical end of the bus; therefore, it is not necessary to install a separate 120 Ω bus terminator module in these backplanes.

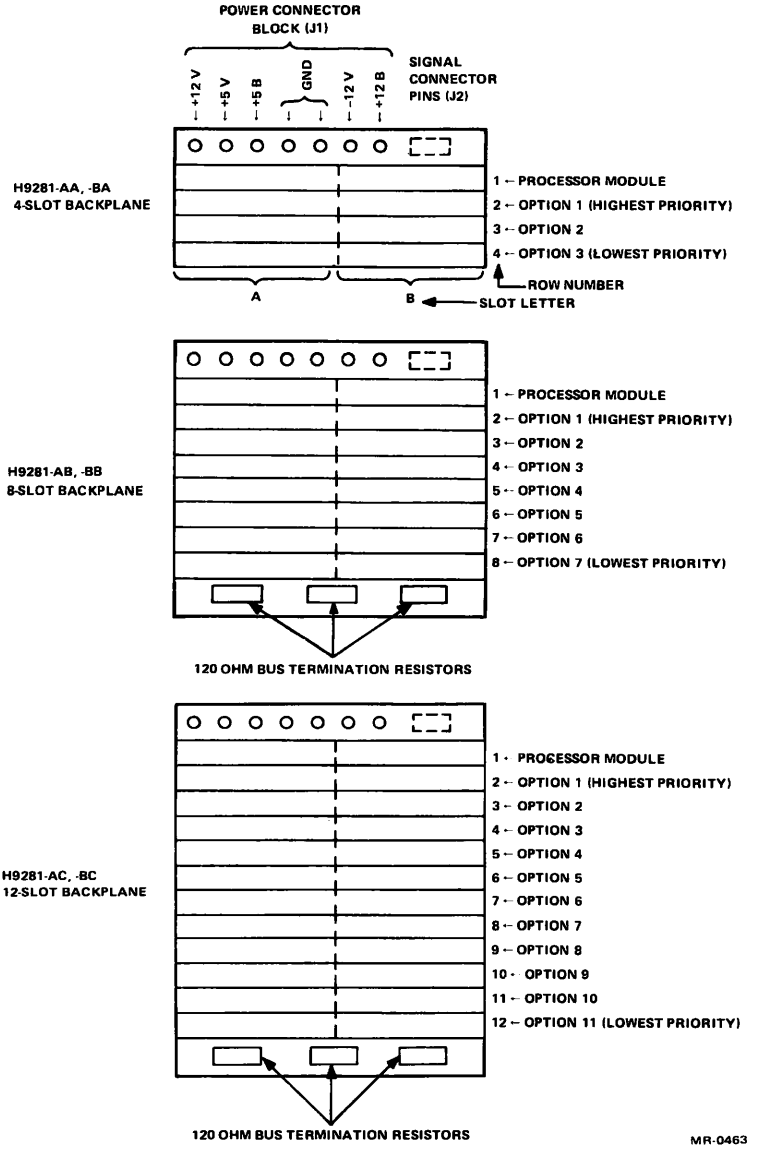

Figure 5 H9281 Option and Connector Locations (Module Side)

H9800-A

H9800-A CABINET

GENERAL

The H9800-A is a low-profile systems desk equipped with a walnut-grained plastic laminate top and color-coordinated to fit into modern office decor. The unit is equipped with six ball casters as standard equipment for easy positioning on carpeted surfaces. Also included is a 115 Vac power distribution panel.

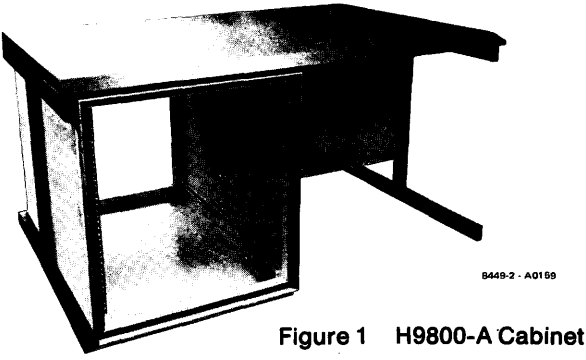

Figure 1 H9800-A Cabinet

SPECIFICATIONS

Dimensions	
Width	121.92 cm (48 in.)
Depth	81.28 cm (32 in.)
Height	70.1 cm (27.6 in.)
Shipping weight	45.36 kg (100 lb.)
Module enclosure	Standard 48.3 cm (19 in.) EIA
Mounting space	
Usable height	53.3 cm (21 in.)
Usable depth (variable)	73.7 cm (29 in.)
Color	Walnut-grained top surface, beige side panels, chrome trim

DESCRIPTION

The H9800-A is constructed of quality materials including a top constructed of 24.9 kg (55 lb.) particle board with a dark-walnut plastic laminate. The "module" itself is constructed of 11 and 18 gauge steel with a maximum loading capacity of 181.44 kg (400 lb.).

H9800-A

The H9800-A consists of a left-mounted rack enclosure offering 53.3 cm (21 in.) of usable height and 73.7 cm (29 in.) of usable depth in a standard 48.3 cm (19 in.) EIA mount format. The right side offers knee space, a modesty panel, and a convenient work surface ideal for using terminals or typewriters.

IBV11-A INSTRUMENT BUS INTERFACE

GENERAL

The IBV11-A is an option that interfaces the LSI-11 bus with the instrument bus as described in IEEE Standard 488-1975, "Digital Interface for Programmable Instrumentation." An IBV11-A can be installed in any LSI-11 system. The IBV11-A consists of an M7954 interface module and a BN11A-04 cable for connecting the first instrument. Additional instruments may be connected using a BN01A cable.

The IBV11-A makes an LSI-11 based programmable instrument system possible.

FEATURES

- PDP-11 software-compatible
- 40-Kbyte/sec maximum transfer capability of hardware
- Board-mounted, user-configured switches allow easy device (register address) and interrupt vector address selection
- Software support available under FORTRAN IV
- 5-Kbyte/sec transfer rate under FORTRAN
- System hardware-compatible with the LSI-11 component system
- Instrument bus compatible with the IEEE 488-1975 standard
- The module supports cable lengths up to 20 m (65.6 ft) total
- 15 devices (maximum) can connect to the bus

SPECIFICATIONS

Identification	M7954
Size	Double
Power	+5.0 Vdc ±5% at 0.8 A
Bus Loads	
AC	1.8
DC	1

The IBV11-A, *when connected to the LSI-11,* will meet the following subsets of IEEE Standard 488-1975:

SH1	SR1	C1
AH1	RL1	C2
TS	PP2	C3
TE5	DC1	C4
LE3		

This module is designed to be the only controller on the IEEE bus. Therefore, it will not respond to another controller on the bus that issues either a parallel poll configure command or a parallel poll control signal.

DESCRIPTION

General

The functional logic blocks that make up the IBV11-A are shown in Figure 1. LSI-11 software controls and communicates with the IBV11-A via programmed I/O transfers and interrupts. Programmed I/O transfers are made possible by assigning unique device addresses (also called "bus addresses") to the IBS and IBD registers.

LSI-11 Bus Interface

LSI-11 bus address selection, interrupt vector address generation, and bus data driver/receiver (transceiver) functions are provided by transceiver integrated circuits (DC005). Each integrated circuit provides the interface for four BDAL bus lines; thus, four transceivers comprise the 16-line BDAL (0:15) L LSI-11 bus interface.

Bit 1 of the least significant octal digit (BDAL 0) selects the IBS or IBD register. This is a byte pointer and it is significant for DATOB and DATIOB bus cycles only. Register address selection is actually performed in the LSI-11 bus protocol and register selection circuit (DC004); the receiver integrated circuit (DC005) simply routes the received low-order three address bits [DA (2:0)] to that function.

All I/O transfers over the LSI-11 bus are done according to a strict protocol. One bus protocol integrated circuit (DC004) performs both this function and the register address selection previously discussed. When an active ADDRESS MATCH signal is present and BSYNC L signal is asserted, the bus protocol integrated circuit is enabled to complete its register selection function. BWTBT L, BDOUT L, and BDIN L bus signals are decoded in the integrated circuit, as appropriate, to produce the LOAD IBS LOW BYTE, SELECT IBS, LOAD IBD LOW BYTE, and RECEIVE internal control signals from the IBV11-A logic functions. The integrated circuit also asserts BRPLY L as required during the I/O sequence to complete the programmed transfer.

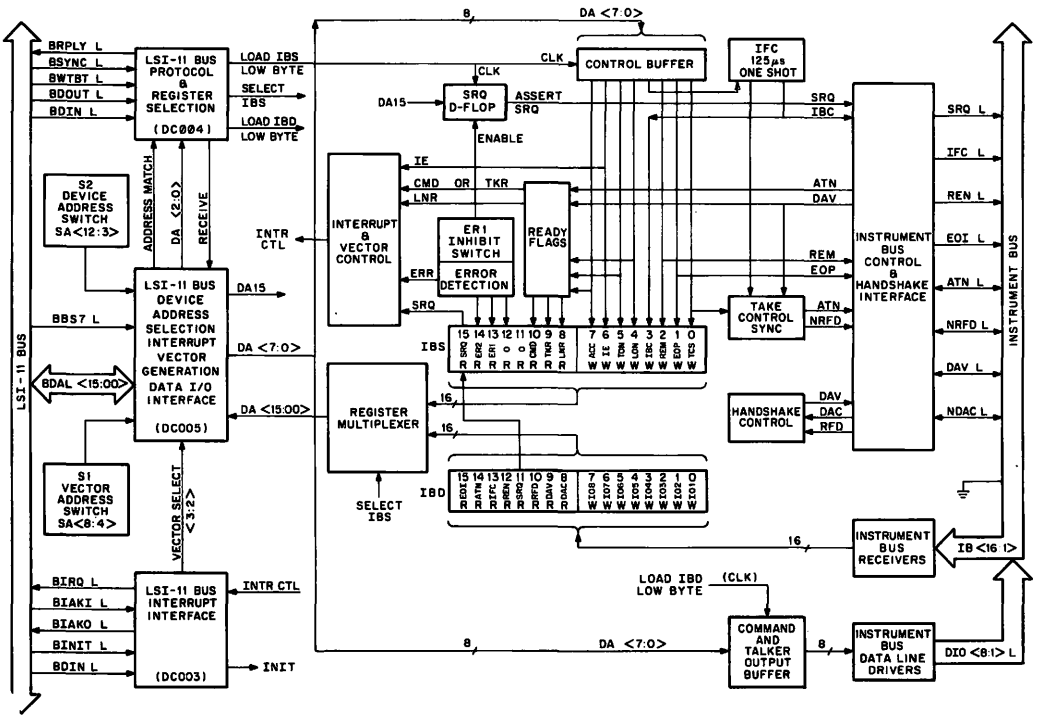

Figure 1 IBV11-A Functional Block Diagram

Interrupts are generated by one interrupt integrated circuit (DC003). Four interrupt vectors can be generated by this bus interrupt interface function. A 5-bit vector switch allows the user to select the interrupt vector for the IBV11-A module. The IBV11-A base interrupt vector is factory-configured for 420. The base interrupt vector can range from 300 to 760; however, the vector interrupt must not conflict with other bus devices, or with those interrupts reserved for system vectors.

Interrupt Vector	Interrupt Source
000420	Error
000424	Service request
000430	Command and talker
000434	Listener

These interrupt vectors allow the IBV11-A to generate interrupts that can most efficiently be serviced by four separate service routines.

Interrupt and vector control logic on the IBV11-A module generates the INTR CTL signals that initiate the interrupts. Inputs for this logic function include the interrupt enable (IE) bit (stored in the control buffer), command or talker (CMD or TKR) and listener (LNR) ready flags, error (ERR) status from the error detection logic, and the device service request (instrument bus control signal).

Instrument Bus Control

The control buffer is an 8-bit register that functions as the low byte of the IBS register. Bits stored in this register control generation of interrupts, instrument bus clear, and instrument bus control and status logic. Setting the IBC bit actually triggers a one-shot producing a 125 μs pulse that clears the instrument bus. Take control sync and handshake control logic function together with instrument bus control and handshake interface logic to communicate with instruments on the bus according to instrument bus protocol. Output transactions with the low byte of the IBD register result in data being stored in the 8-bit command and talker output buffer. Instrument bus line drivers gate this byte onto the instrument bus when the IBV11-A is an active talker, or when it is an active controller.

Instrument Bus Interface

The IBV11-A interfaces with the instrument bus via four integrated circuits, type MC3441. These integrated circuits are bus transceivers, each containing four bus drivers, four bus receivers, and bus terminations that comply with instrument bus specifications.

CONFIGURATION

General

The IBV11-A option can be installed in any LSI-11 bus to interface various instruments via an "interrupt bus." The instrument bus is defined in the IEEE Standard 488-1975, "Digital Interface for Programmable Instrumentation." Any instruments designed to interface with the bus defined in that standard can be interfaced to the LSI-11 system via the IBV11-A.

The following paragraphs contain only the basic information necessary for configuring device register addresses and vector interrupts, general installation and interface to the instrument bus, and basic programming (e.g., device register functions).

Device Address

Device address switches provide a convenient means for the user to configure the IBV11-A's register addresses. Only switches corresponding to BDAL lines (3:12) are provided. By PDP-11 convention, the upper 4K address space (bank 7) is normally reserved for peripheral devices, such as the IBV11-A. The processor module asserts BBS7 L whenever a bank 7 address [BDAL (13:15) L is asserted] is placed on the bus. Thus, BBS7 L must be asserted to enable an "address match" output from the address selection function. Any address ranging from 16000X to 17777X can be configured that does not conflict with other device addresses within the system; the X in the address represents register and byte selection within the module.

Each IBV11-A module is factory-configured for a standard device register address (160150) and interrupt vector (420). Switches S1 (interrupt vector) and S2 (device register address) configure the module. A summary of register addressing and interrupt vectors is provided in Figures 2 and 3. Observe that the IBD register address is always the IBS address plus 2. Similarly, only the error interrupt vector is configured. The remaining three vectors are permanently assigned sequential addresses in address increments of four as shown in Table 1.

Table 1 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address
Registers			
Control/Status	IBS	R/W	160150
Data	IBD	R/W	160152
Vectors			
Error	ER2, ER1		420
Service	SRQ		424
Command and Talker	CMD, TKR		430
Listener	LNR		434

Switches S1 and S2 are located on the IBV11-A module as shown in Figure 4. S1 and S2 are switch assemblies, each containing several individual switches. The individual switches indicated in Figures 2 and 3 are clearly marked on the S1 and S2 assemblies. The ON and OFF positions are also clearly marked.

Interrupt Vectors

The IBV11-A is capable of generating four separate interrupt requests; each have separate interrupt vectors and normally would have separate service routines. Interrupts can be requested only when the IBS IE (interrupt enable) bit is set. Interrupt requests are priority structured in the IBV11-A. A summary of the four types is provided below.

Priority	Vector	Associated IBS Bit	Cause of Interrupt
Highest	000XNN00	ER2, ER1	Error condition.
Second highest	000XNN04	SRQ	A device connected to the instrument bus is requesting service.
Third highest	000XNN10	TKR, CMD	The IBV11-A is an active talker and is ready for the processor to output a byte to the low byte of the IBD register. (The IBV11-A will normally then transmit the

			byte over the installation bus to the active listener(s).)
Lowest	000XNN14	LNR	The IBV11-A is an active listener and has a data byte to be read by the processor.

NOTES

1. X = User-configured interrupt vector octal digit.
2. N = User-configured interrupt vector binary bits.
3. Associated IBS bits shown, when set, produce interrupt requests if the IE bit is set.

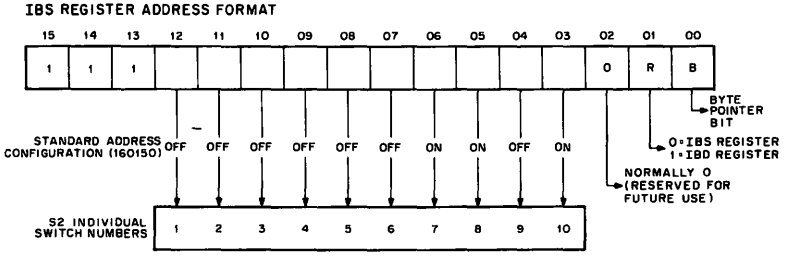

Figure 2 Register Addresses

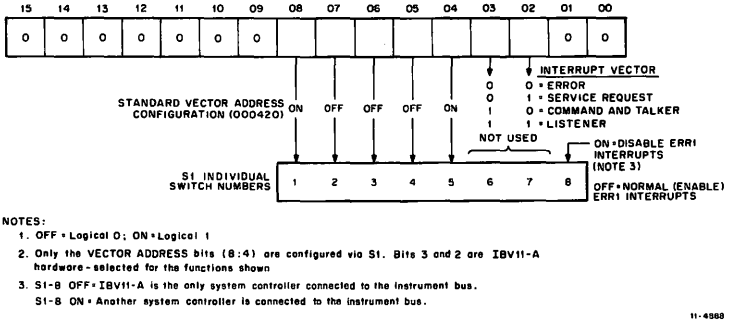

Figure 3 Interrupt Vector

IBV11-A

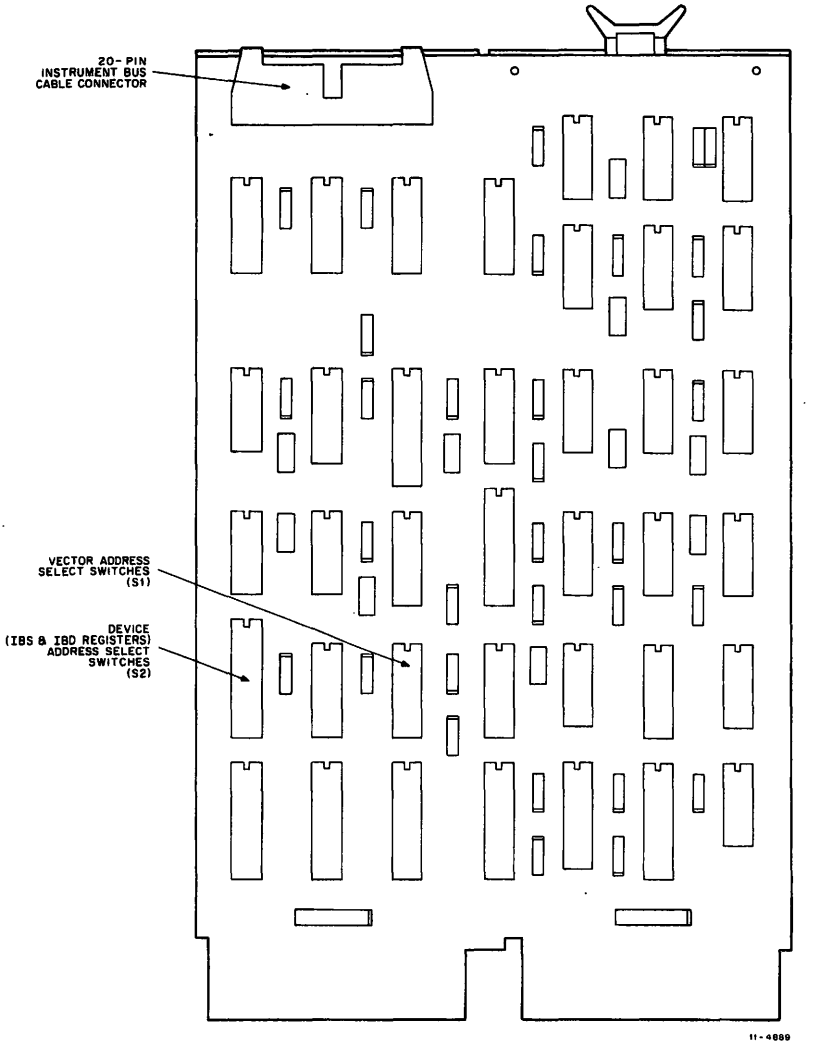

Figure 4 IBV11-A Module Switch Locations

Interrupt	Interrupt Vector
Error	"n" (configured vector)
Service	n + 4
Command and Talker	$n + 10_8$
Listener	$n + 14_8$

Preferred value range for "n" = $300 \leq n \leq 760$

Registers

The IBV11-A communicates with devices connected to the instrument bus under the control of the program being executed. All communication between the processor and the IBV11-A is via the instrument bus status (IBS) and instrument bus data (IBD) registers. The programmer must be aware of the functional significance of each bit in both registers before any programs can be written that will control specific devices on the instrument bus. In addition, the programmer must establish instrument (device) addresses, and conform to the programming rules specified for each instrument connected to the instrument bus. See Figure 5 for a description of the IEEE bus.

The instrument bus status (IBS) register is similar in function to other device control/status register (CSRs). The instrument bus data (IBD) register is a 16-bit register that contains eight read/write data bits in the low byte and eight read-only bits in the high byte. The eight read-only bits allow the program to read the logical state of the control and management signals of the instrument bus.

The IBS register provides the means for controlling the instrument bus control and management signals, and IBV11-A functions relative to the LSI-11 bus. The low byte of the IBD register, on the other hand, is used for passing commands to devices connected to the bus, and for transmitting and receiving data between the processor and talker and listener devices. In addition, the high byte of the IBD register allows for processor monitoring of all instrument bus signal (control) lines. IBS and IBD registers are shown in Figure 6 and described in Tables 2 and 3.

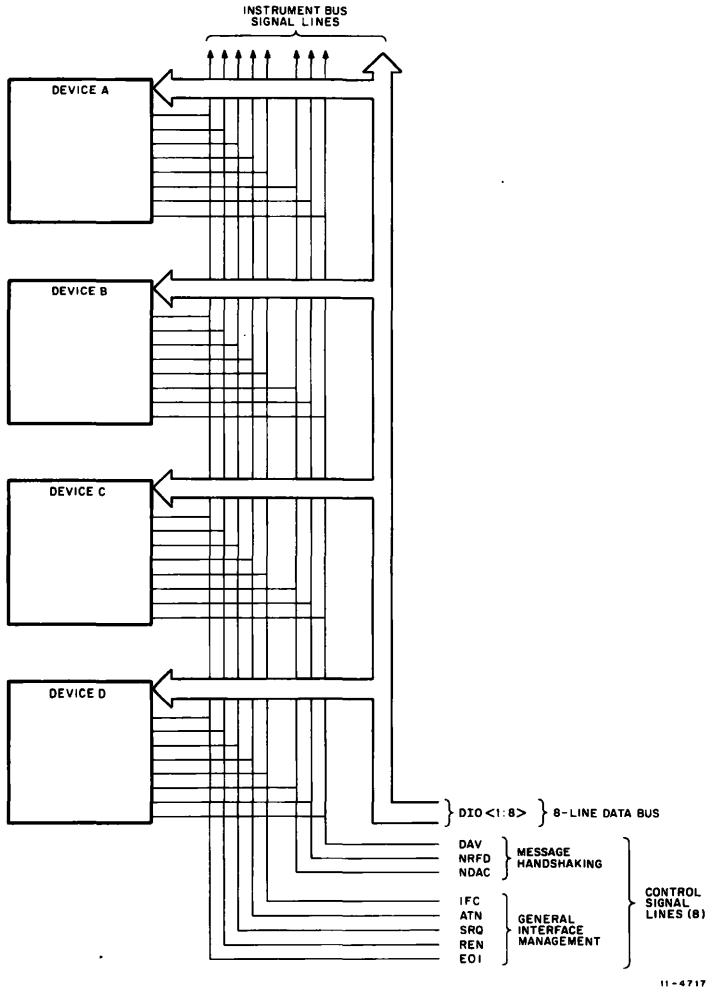

Figure 5 Instrument Bus Signal Lines

INSTRUMENT BUS STATUS (IBS)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SRQ	ER2	ER1	NOT USED	NOT USED	CMD	TKR	LNR	ACC	IE	TON	LON	IBC	REM	EOP	TCS

INSTRUMENT BUS DATA (IBD)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
EOI	ATN	IFC	REN	SRQ	RFD	DAV	DAC	I08	I07	I06	I05	I04	I03	I02	I01

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Figure 6 Register Word Format

Table 2 Instrument Bus Status Word Format

Bit: 15 **Name:** SRQ
Description: (Service Request)
Monitors the state of the instrument bus service request line at all times. Set when the IB SRQ line is low. Will cause an interrupt when both SRQ and the interrupt enable bits are set. When the ER1-inhibit switch is set, this bit will be written by any type of instruction that writes into the IBS. Read/write.

Bit: 14 **Name:** ER2
Description: (Error 2)
Asserted if the IB reports that DAC is true when the IBV11-A tries to send a data or command byte. This condition will exist when there is no active listener or command acceptor on the IB. An ERR interrupt occurs when both the ER2 and the interrupt enable bits are set. Cleared by clearing both TON the TCS. Read-only.

Bit: 13 **Name:** ER1
Description: (Error 1)
Unless inhibited by the ER1-inhibit switch, this bit is asserted whenever a conflict occurs between the IB ATN, IFC, or REN lines and their IBV11-A control hardware, i.e., if one or more of these control lines is asserted when it should not be asserted or not asserted when it should be asserted. When asserted, the IBV11-A will not assert the ATN line even though the TCS bit remains set. An ERR interrupt occurs when both the ER1 and the interrupt enable bits are set. This condition can be cleared only by clearing the cause. Read-only.

Bit: 12 **Name:** Not used
Description: Always read as a zero. Read-only.

Bit: 11 **Name:** Not used
Description: Always read as a zero. Read-only.

Bit: 10 **Name:** CMD
Description: (Command Done)
Set when the IBV11-A is ready to send a command byte; set by a successsful TCS to indicate that ATN was asserted and the first command byte may be issued. Also set by DAC when a command has been completely accepted. A CMD/TKR interrupt occurs when both the CMD and the interrupt enable bits are set. This bit is cleared by INIT, received IFC, writing a command into the IBD low byte, or by turning TCS off. Read-only.

Bit: 9 **Name:** TKR
Description: (Talker Ready)
Set when the IBV11-A is ready to send a data byte; set when TON is on while TCS is turned off, or by DAC when TON is on. A CMD/TKR interrupt occurs when both the TKR and the interrupt enable bits are set. Cleared by INIT, received IFC, writing a data byte into the IBD low byte, or by turning TON off or TCS on. Read-only.

Bit: 8 **Name:** LNR
Description: (Listener Ready)
Set when the IBV11-A has a data or command byte ready for reading from the IBD low byte; set by DAV when LON is on. An LNR interrupt occurs when both the LNR and the interrupt enable bits are set. Cleared by reading the IBD low byte if ACC is off or by clearing the IBD low byte if ACC is on. Also cleared when LON is turned off and by INIT or received IFC. Read-only.

Bit: 7 **Name:** ACC
Description: (Accept Data)
Set and cleared under program control. When clear, reading the IBD will automatically clear the LNR and assert DAC. When set, the programmer must write 0 to the IBD low byte in order to clear the LNR bit and assert DAC. When the TCS, LON, and TON bits are all off (clear), setting this bit will assert NRFD. Cleared by INIT or received IFC. Read/write.

Bit: 6 **Name:** IE
Description: (Interrupt Enable)
Set and cleared under program control to enable and disable all interrupts. Cleared by INIT. Read/write.
Bit: 5 **Name:** TON
Description: (Talker On)
Set and cleared under program control to enable and disable the talker function. Cleared by INIT or received IFC. Read/write.

Bit: 4 **Name:** LON
Description: (Listener On)
Set and cleared under program control to enable and disable the listener function. Cleared by INIT or received IFC. Read/write.

Bit: 3 **Name:** IBC
Description: (Interface Bus Clear)
Set under program control to cause the IFC line to be asserted for about 125 μsec. TCS will automatically be asserted at the end of IBC (out-going IFC). Cleared by INIT. Read/write.

Bit: 2 **Name:** REM
Description: (Remote On)
Set and cleared under program control to assert and unassert the REN line. Cleared by INIT or received IFC. Read/write.

Bit: 1 **Name:** EOP
Description: (End of Poll)
Set and cleared under program control to assert and unassert the E01 line. Cleared by INIT or received IFC. Read/write.

Bit: 0 **Name:** TCS
Description: (Take Control Synchronously)
Set and cleared under program control to take control synchronously, or to unassert ATN. Setting TCS will cause NRFD to be asserted for at least 500 ns before DAV is checked. ATN is then asserted when DAV is unasserted; NRFD is unasserted and CMD is set no sooner than 500 ns after ATN is asserted. Cleared by INIT or received IFC. Read/write.

Table 3 Instrument Bus Data Word Format

Bit: 15 **Name:** EOI
Function: (End or Identify)
Monitors the IB EOI line at all times. Set when the IB EOI line is low. Read-only.

Bit: 14 **Name:** ATN
Function: (Attention)
Monitors the IB ATN line at all times. Set when the IB ATN line is low. Read-only.

Bit: 13 **Name:** IFC
Function: (Interface Clear)
Monitors the IB IFC line at all times. Set when the IB IFC line is low. Read-only.

Bit: 12 **Name:** REN
Function: (Remote Enable)
Monitors the IB REN line at all times. Set when the IB REN line is low. Read-only.

Bit: 11 **Name:** SRQ
Function: (Service Request)
Monitors the state of the instrument bus service request line at all times. Set when the IB SRQ line is low. Will cause an interrupt when both SRQ and the interrupt enable bits are set. Read-only.

Bit: 10 **Name:** RFD
Function: (Ready for Data)
Monitors the IB NRFD line at all times. Set when the IB NRFD line is high. Read-only.

Bit: 9 **Name:** DAV
Function: (Data Valid)
Monitors the IB DAV line at all times. Set when the IB DAV line is low. Read-only.

Bit: 8 **Name:** DAC
Function: (Data Accepted)
Monitors the IB NDAC line at all times. Set when the IB NDAC line is high. Read-only.

Bit: 7-0 **Name:** DIO8-DIO1
Function: IB Data I/O lines
Reading the IBD low byte picks up unlatched data directly from the IB DIO lines. Data on the IB DIO lines may change if the LNR bit is not set. Generally, the only reason to read the DIO lines when LNR is not set is when a parallel poll response is expected. Writing data to the IB DIO lines is permitted when TON is set and DAV is clear, or when TCS and ATN are set and DAV is clear. Otherwise, writing into the IBD low byte will have no effect on the DIO lines but will set DAC if both ACC and LNR are set. Read/write.

The data and command output buffer is cleared by INIT or received IFC.

Connecting the External Equipment
Connection from the IBV11-A to the first device on the instrument bus is via a type BN11A cable (supplied with the M7954 module), as shown in Figure 7. One end is terminated with a 20-pin connector that mates with the 20-pin connector on the IBV11-A module; the other end is terminated with a 24-pin "double-ended" connector that conforms to

the IEEE 488 1975 standard; the cable can be connected to any device conforming to that standard. The double-ended connector contains a male 24-pin and a female 24-pin connector in the same connector housing. This allows for "linear" and "star" connections to instruments connected to the instrument bus, as shown in Figure 8. One BN11A is included in the IBV11-A option.

The linear arrangement shown in the figure includes five devices (or instruments), A through E. There is no particular significance to the sequence shown, or the electrical position along the instrument bus. Unlike the LSI-11 bus, the position along the bus does not structure device priority in the system.

The star arrangement shown in the figure allows five devices to be connected by stacking instrument cable connectors on the BN11A's double-ended connector. Double-ended connectors on instrument bus cables will normally include captive locking screws on each connector assembly (two each), allowing stacked connectors to be secured together in a single assembly.

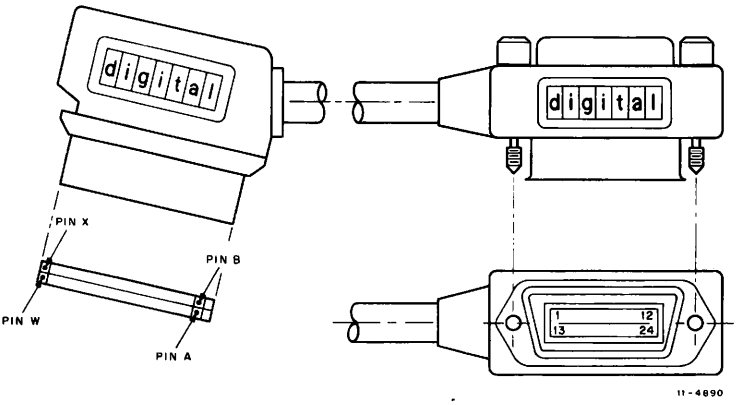

Figure 7 BN11A Instrument Bus Cable

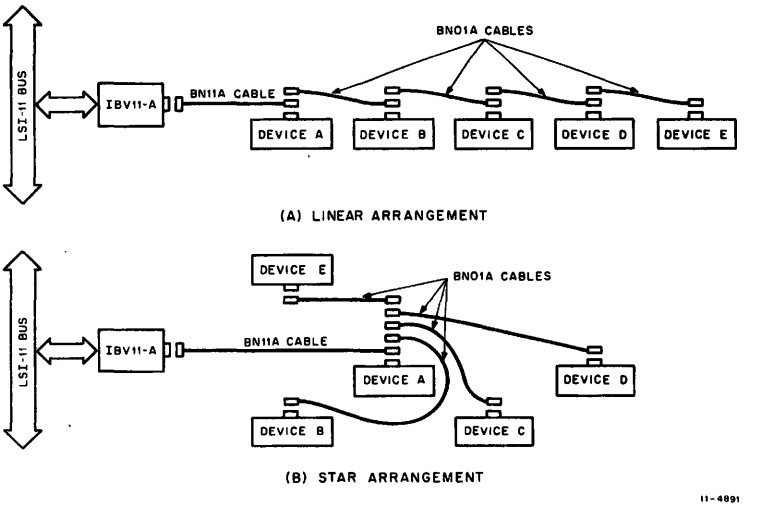

Figure 8 Linear and Star Configurations

The BN11A cable connector pin signal assignments are listed in Table 4 for each connector. One BN11A cable is required for each IBV11-A module in a system.

Optional Cables

1. Connect M7954 module to first instrument:

BN11A-02	2 m (78.7 in.)
BN11A-04	4 m (157.5 in.)

2. Connect instrument to instrument:

BN01A-01	1 m (39.4 in.)
BN01A-02	2 m (78.7 in.)
BN01A-04	4m (157.5 in.)

Table 4 BN11A Connector Pin Assignments

IBV11-A Connector Pin	Signal Name	Instrument Bus Connector Pin
U	DIO1	1
S	DIO2	1
P	DIO3	3
M	DIO4	4
R	EOI	5
T	DAV	6
V	NRFD	7
X	NDAC	8
B	IFC	9
J	SRQ	10
F	ATN	11
W	(SHIELD)	12
K	DIO5	13
H	DIO6	14
E	DIO7	15
C	DIO8	16
D	REN	17
	GND (DAV GND)	18
N	GND (NRFD GND)	19
	GND (NDAC GND)	20
A	GND (IFC GND)	21
	GND (SRQ GND)	22
L	GND (ATN GND)	23
W	GND (LOGIC)	24

PROGRAMMING

Example 1—IBV11-A to Listener Device

This programming example illustrates how the IBV11-A communicates with a listener device. Standard device and vector addresses are used, as shown in Figures 2 and 3. Once the program is started, and after pointers have been initialized and the IBV11-A has taken control synchronously, it communicates with the IBV11-A via an interrupt-driven service routine. No "background" program is used; the program simply waits until another interrupt occurs.

Communication with the listener device includes the transmission of two command bytes (read as words from a message buffer), followed by 24 message bytes that program device functions. After all message bytes have been transmitted, the program halts (displays HALT PC address = 1066).

A program flowchart for this example is shown in Figure 9; a symbolic listing is shown in Figure 10.

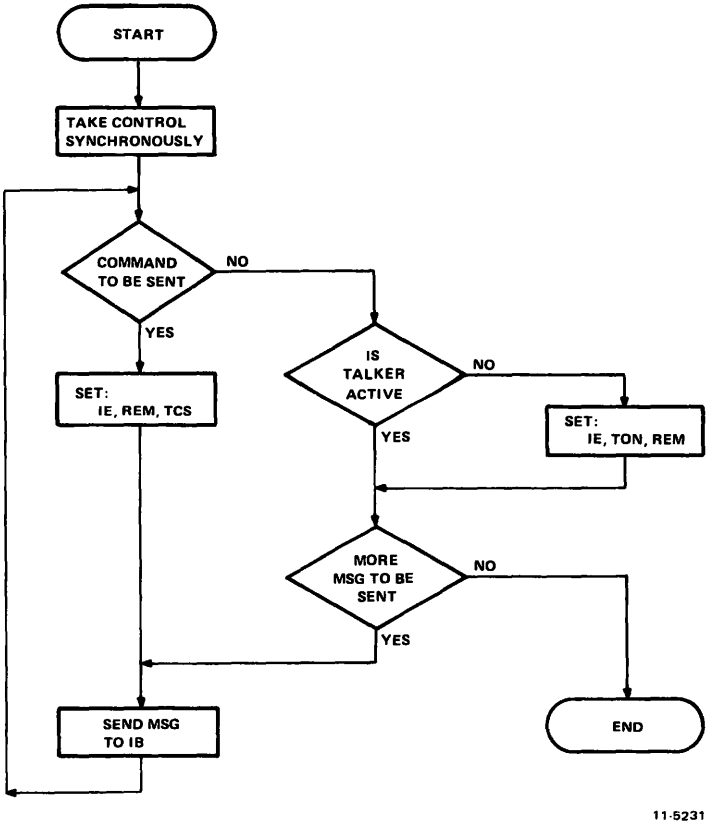

Figure 9 Communicating with a Listener Device (Program Flowchart)

```
ADDRESS   OCTAL CODE      ASSEMBLER SYNTAX      COMMENTS

000430    001020                                ; INTR RETURN ADDRESS
000432    000200                                ; PSW

001000    012706    START: MOV #500,R6          ; SET UP STACK POINTER
001002    000500
001004    012700           MOV #2000,R0         ; R0 IS MSG BUFFER ADDRESS
001006    002000
001010    012737           MOV #110,160150      ; TAKE CONTROL
001012    000110                                ; SYNCHRONOUSLY TO BECOME
001014    160150                                ; CONTROLLER-IN-CHARGE

001016    000777    WAIT:  BR .                 ; WAIT FOR INTERRUPT
001020    020027           CMP R0,#2004         ; MORE COMMANDS TO BE SENT?
001022    002004
001024    100006           BPL 20$              ; IF NO,GO TO 20$
001026    012737           MOV #105,160150      ; IF YES,SET IE,REM,AND
001030    000105                                ; TCS BITS OF IBS REG TO
001032    160150                                ; ACTIVATE CONTROLLER
001034    012037    SEND:  MOV (R0)+,160152     ; SEND MSG TO IB
001036    160152
001040    000002           RTI                  ; RETURN TO WAIT--FOR
                                                ; MSG TO BE ACCEPTED
001042    020027    20$:   CMP R0,#2004         ; IS TALKER ACTIVE?
001044    002004
001046    003003           BGT 30$              ; IF YES,GO TO 30$
001050    012737           MOV #144,160150      ; OTHERWISE SET IE,TON
001052    000144                                ; AND REM BITS OF IBS REG
001054    160150                                ; TO ACTIVATE TALKER
001056    020027    30$:   CMP R0,#2064         ; HAD ALL MSG BEEN SENT?
001060    002064
001062    100364           BMI SEND             ; IF NO,GO SEND ANOTHER MSG
001064    000000           HALT                 ; OTHERWISE STOP
```

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Figure 10 Communicating with a Listener Device (Program Listing)

Example 2—IBV11-A to Talker Device

This programming example illustrates how the IBV11-A communicates with a talker device. As in example 1, this programming example assumes standard IBV11-A device and interrupt vector addresses. Communication between the instrument and the LSI-11 system is via IBV11-A interrupt-driven service routines. No background program is used; the program simply waits until another interrupt occurs.

Communication with the instrument involves first transmitting the content of the command message buffer, in a manner similar to the program operation described for example 1, followed by accepting instrument output data and storing it in a received data buffer. The content of the command message buffer typically includes first activating the device via its listener address, followed by setting up range mode, operating parameters for the instrument, an execute command, and finally, activating the device as an active talker via its talker address. Once the device has received the command message buffer data, it performs the programmed measurements (or the function, depending on the instrument) and returns data to the LSI-11 system via the IBV11-A. Note that during this portion of program operation, the IBV11-A functions as an active listener on the instrument bus. Once all measurements have been stored by the program, the program halts with a displayed PC address = 1102.

A program flowchart for this example is shown in Figure 11 and a symbolic program listing is shown in Figure 12.

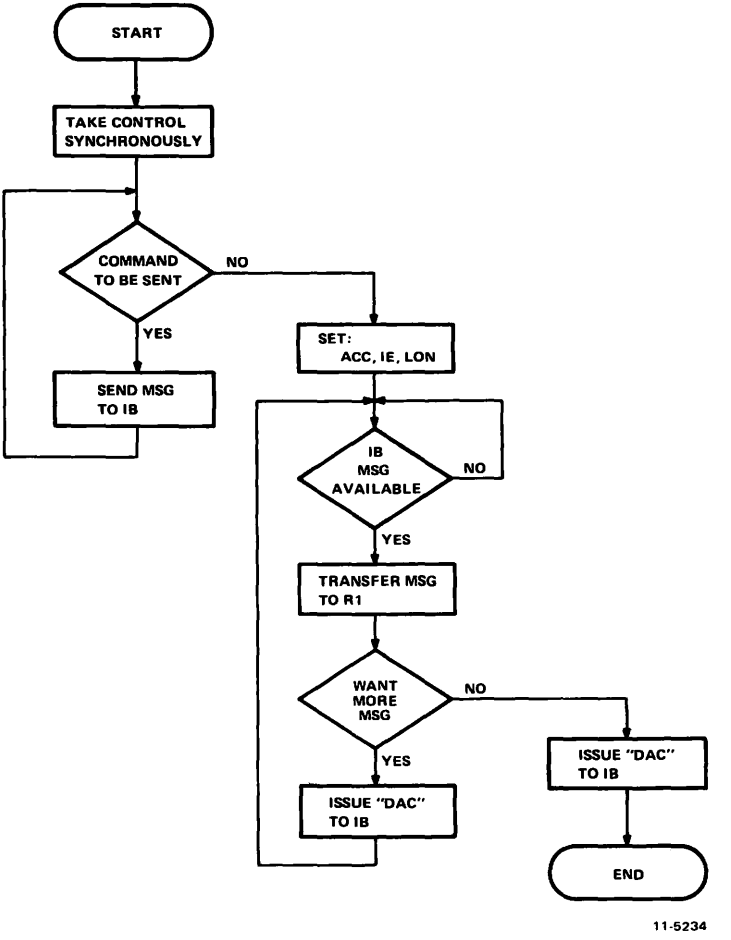


Figure 11 Communicating with a Talker Device (Program Flowchart)

```
ADDRESS CODE    ASSEMBLER SYNTAX          COMMENTS

000430  001024                            ; COMMAND/TALKER INTR
                                          ; RETURN ADDRESS
000432  000200                            ; PSW
000434  001056                            ; LISTENER RETURN ADDRESS
000436  000200                            ; PSW

001000  012706  START:  MOV #500,R6        ; SET UP STACK
001002  000500
001004  012700          MOV #2000,R0      ; IBV11-A MSG BUFFER
001006  002000
001010  012701          MOV #2500,R1      ; BUFF FOR RECEIVED MSG
001012  002500
001014  012737          MOV #110,160150 ; TAKE CONTROL SYNCHRONOUSLY
001016  000110                            ; TO BECOME CONTROLLER-
001020  160150                            ; IN-CHARGE,C-I-C
001022  000777  WAIT:   BR .              ; WAIT--FOR INTERRUPT
001024  012737          MOV #105,160150 ; PREPARE TO SEND
001026  000105                            ; COMMAND MESSAGES
001030  160150
001032  022700          CMP #2024,R0      ; HAD ALL COMMANDS
001034  002024                            ; BEEN SENT?
001036  001404          BEQ 20$           ; IF YES,GO TO 20$
001040  012037          MOV (R0)+,160152; OTHERWISE SEND MSG
001042  160152
001044  000002          RTI               ; RETURN TO WAIT--FOR
                                          ; MSG TO BE ACCEPTED
001046  012737  20$:    MOV #320,160150 ; IBV11-A SWITCHES FROM
001050  000320                            ; CONTROLLER TO LISTENER
001052  160150
001054  000002          RTI               ; RETURN TO WAIT--
                                          ; FOR DMM MSG
001056  013721          MOV 160152,(R1)+; SAVE THE RECEIVED
001060  160152                            ; MSG IN R1
001062  022701          CMP #2540,R1      ; HAD 20 (OCTAL) MSG
001064  002540                            ; BEEN ACCEPTED?
001066  001403          BEQ 30$           ; IF YES,GO TO 30$
001070  005037          CLR 160152        ; OTHERWISE ISSUE DAC
001072  160152
001074  000002          RTI               ; RETURN TO WAIT--FOR
                                          ; ANOTHER DMM MSG
001076  005037  30$:    CLR 160152        ; ISSUE DAC TO IB
001100  000000          HALT              ; STOP,20 MSG RECEIVED
```

11-5235

Figure 12 Communicating with a Talker Device (Program Listing)

KPV11-A,-B,-C
POWER-FAIL/LINE-TIME
CLOCK/TERMINATOR

GENERAL

The KPV11 is an LSI-11 power-fail/line-time clock (LTC) generator. Three versions of the KPV11 are available: KPV11-A, which has only power-fail and LTC functions; KPV11-B, which has 120 Ω bus terminations in addition to the power-fail and LTC; and KPV11-C, which is similar to the KPV11-B, but has 220 Ω bus terminations. The KPV11 is compatible with all LSI-11 component systems and LSI-11 backplane options. It is designed for installation into any LSI-11 bus-structured backplane or remote installation (not installed into a backplane) via an optional cable which connects the KPV11 to the LSI-11 backplane. In order to use the KPV11-B or KPV11-C as bus terminators, they must be installed in the LSI-11 backplane. An optional console panel and bezel are available for manual control of the LTC and the display of dc power on/off status and the processor run/halt state.

FEATURES

- Automatic generation of BPOK and BDCOK power-up/power-down signal sequence
- Automatic program restoration and starting when used with nonvolatile memory and appropriate software routines
- Line-time clock time reference provided by a signal source (user-supplied) other than the power line
- KPV11-B and KPV11-C provide bus termination when plugged into an LSI-11 backplane
- Can be installed into the LSI-11 backplane or mounted remotely. An optional cable (DIGITAL part no. 70-12754) connects the KPV11 to the LSI-11 backplane
- Expandable with the 54-11808 console panel option

KPV11-A, -B, -C

SPECIFICATIONS

Identification	M8016 (KPV11-A) M8016-YB (KPV11-B) M8016-YC (KPV11-C)
Size	Double
Power	+5 Vdc ±5% at 560 mA
System DC	
DC Sensing Inputs	+5 Vdc ±5% at 0.11 mA +12 Vdc ±3% at 0.82 mA
AC Line Monitor Input	24 Vac ±10% at 200 mA with grounded center tap (Figure 4)
Bus Loads	
AC	1.6
DC	1.0
Options	
54-11808	Console Panel (PC assembly)
70-11656	Console Bezel
70-12754	Remote Signal Cable (for remote mounting of KPV11)
70-086120	Console Signal/Power Cable (for connecting optional console panel to the KPV11)

DESCRIPTION

General

The KPV11-A provides two main functions—power signal sequence circuits and programmable line-time clock circuits. The KPV11-B and KPV11-C have, in addition, bus termination circuits, 120 Ω for the KPV11-B and 220 Ω for the KPV11-C. All KPV11 modules have an interface for the optional console panel. Figure 1 illustrates the basic KPV11 functions.

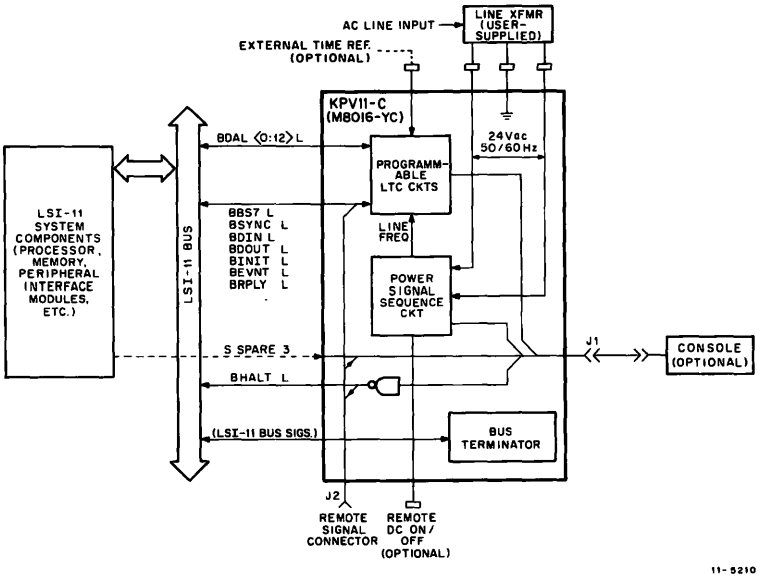


Figure 1 KPV11 Functional Block Diagram

Power Signal Sequence Circuits

The power signal sequence circuits generate the proper LSI-11 bus power sequencing signals (BPOK H and BDCOK H) for the processor power-up/power-down sequence and line-time clock interrupts at the power line frequency. Figure 2 illustrates the KPV11 power signal sequence timing.

Power signal sequence circuits are shown in Figure 12. Operating power for these circuits is obtained from the 24 Vac, 50 Hz or 60 Hz input at the two ac terminals and GND. Conventional full-wave rectifiers produce +17V and −17V operating voltages for the ac line monitor Schmitt trigger (Q1 and Q2) and a 5V, 3-terminal regulator; the regulator +5V is distributed throughout the power signal sequence circuit for operating power.

Power-Up — During the power-up sequence, ac voltage from the transformer secondary is applied to a Schmitt trigger circuit (Q1 and Q2). The Schmitt trigger squares the ac sine-wave and drives level converter Q3. Q3's output is a TTL-compatible signal. The square wave signal is applied to two 10 ms (nominal) one-shots (and the LTC circuits). One one-shot triggers on the positive-going transition of the square wave signal and the other triggers on the negative-going transition. The one-shot outputs are ORed, producing a high (normal) output at gate E6-13. Normally, one or the other one-shot will be in the set state. If a transition of the square wave signal is not followed by a transition of the opposite polarity within 20 ms, both one-shots will time out and the logic signal at E6-13 will go low; this is a power-fail condition.

During a power-up sequence, voltage sense +5V and +12V (remote sense), or +5V and +12V (LSI-11 backplane voltages) inputs rise to voltage levels that cause voltage comparators A and B to produce high outputs. The comparator outputs are connected and applied to one input of gate A. The remaining input of gate A is enabled by the normally high gate E6-13 signal, which is applied (but not delayed) via the 3 ms delay circuit. Gate A's output goes high. This signal is then delayed 17 ms and inverted, producing a low signal which is applied to the non-inverting input of comparator C and gate C. Comparator C's output goes low, turning off Q4 and producing an active BDCOK H signal 17 ms (minimum) after ac power is applied.

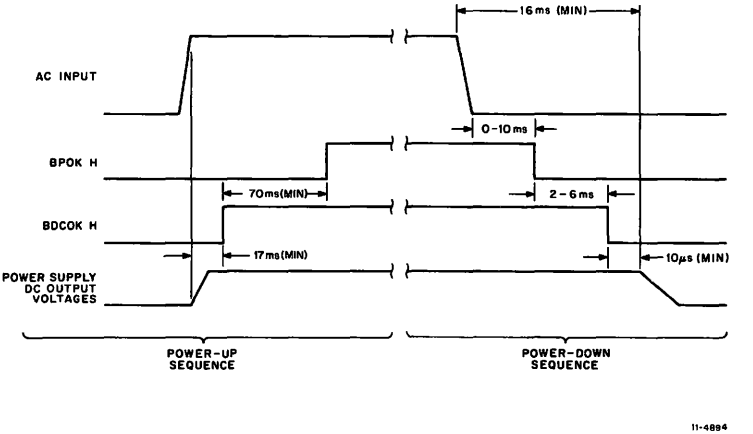


Figure 2 Power Signal Sequence Timing

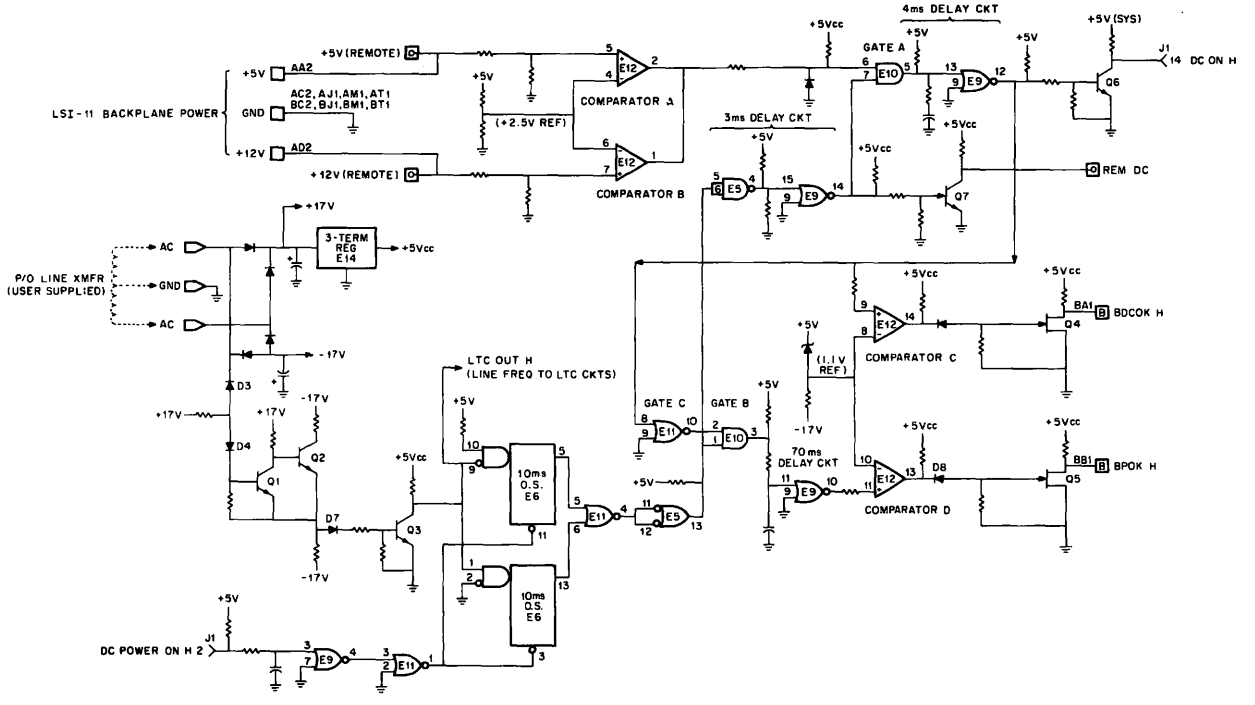


Figure 3 Power Signal Sequence Circuits

Gate C's output goes high, enabling gate B. The remaining gate B input is enabled by the high gate E6-13 output signal. Gate B's high output signal is delayed 70 ms and inverted, producing a low signal (E10-10) which is applied to the non-inverting input of comparator D. Comparator D's output signal goes low, turning off Q5, and producing the active BPOK H signal 70 ms after the active BDCOK H signal. With both signals in the active (high) state, normal system operation can proceed.

Power-Down — When an ac power failure occurs, the trigger pulses to the one-shots cease, and both one-shots time out. Gate E6-13 goes low, inhibiting gate B, and initiating the 3 ms delay. (E6-4 signal voltage starts to rise from the logical low state). Gate B's output goes low; this low signal is inverted, but not delayed, by the 70 ms delay circuit, and the resulting high signal is applied to the non-inverting input of comparator D. Comparator D's output goes high, turning on Q5, and negating BPOK H. Meanwhile, the 3 ms delay circuit, after the 3 ms delay, produces a low signal at E10-14. A low signal inhibits gate A, causing its output signal to go low. The low signal is inverted (but not delayed) by the 17 ms delay circuit, and applied to the non-inverting input of comparator C. Comparator C's output goes high, turning on Q4 and negating the BDCOK H signal 3 ms after BPOK H becomes negated. Q6 monitors the 17 ms delay circuit output and produces the DC ON H signal for the remote console panel display. When dc voltages are normal, E10-12 goes low; Q6 cuts off and DC ON H goes high. When dc voltages are not present, E10-12 goes high; Q6 turns on and negates DC ON H.

When the remote console panel is connected to the KPV11, the DC ON/OFF switch can simulate a power line failure and control the user's power supply. The simulated power line failure occurs when a low DC POWER ON H occurs (DC OFF switch position). This low signal produces a low signal that clears both one-shots, and the simulated power failure results.

Remote control of the user's power supply is made possible via the REMOTE DC ON/OFF etched pad. The signal present at this point is the 3 ms delay circuit signal (E10-14) inverted by Q7. Thus, when normal line voltage is sensed and the remote console panel DC ON/OFF switch is not in the OFF position, this signal goes low, activating a control circuit in the user's power supply that turns dc voltages on. When this signal is high—a result of power-fail or placing the remote console panel DC ON/OFF switch in the OFF position—the user's power supply dc output voltages should turn off.

Programmable Line-Time Clock (LTC) Circuits

Programmable line-time clock functions are shown in Figure 4. Jumpers allow selection of line frequency or external time base operation,

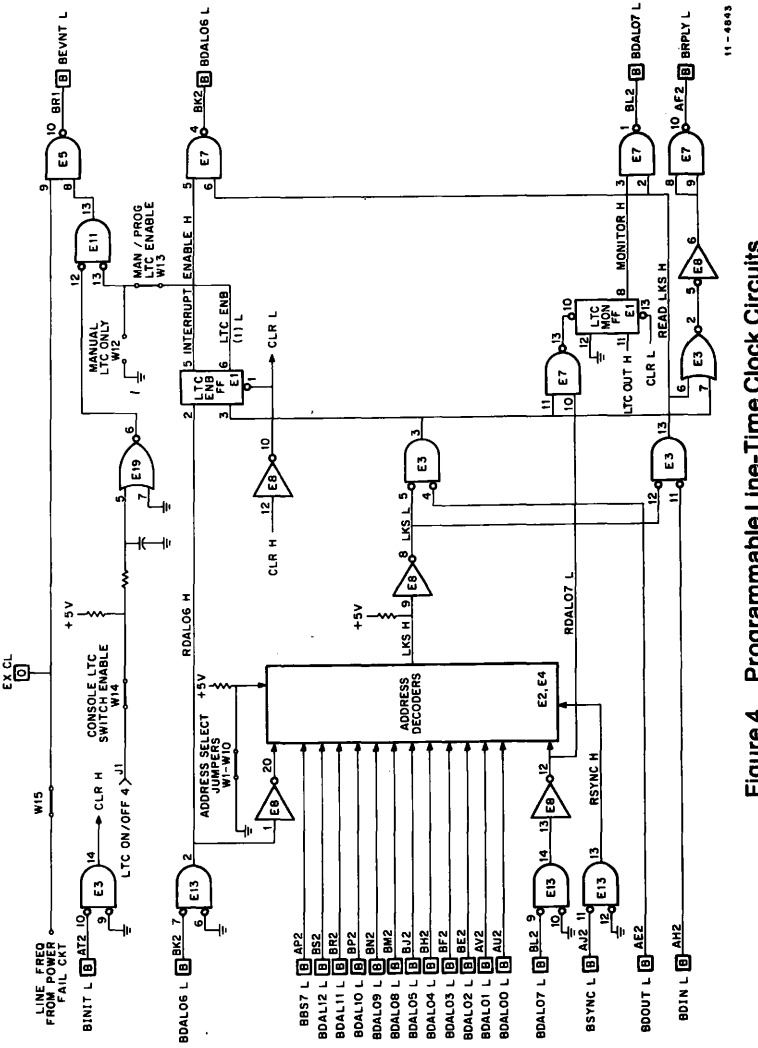


Figure 4 Programmable Line-Time Clock Circuits

console LTC ON/OFF switch enable/disable, and manual/-programmable operation. Additional jumpers (W1-W10) select the device address for the LKS register. Jumpers are factory-configured as shown in Figure 8.

Program access to the LKS register is via the address configured by jumpers W1-W10. The processor first places the KPV11 LKS register address on BDAL (00:15) L and asserts BBS7 L. Note that BBS7 L is asserted only during an addressing operation when BDAL (13:15) L are asserted; hence, the address decoders receive only BDAL (00:12) L and BBS7 L. Device selection occurs on the leading edge of BSYNC L. If the address input matches the jumpered address, LKS H goes high (true), and remains true for the duration of the LSI-11 bus cycle.

Two flip-flops comprise the two significant bits of the LKS register. Bit 6 is produced by the LTC enable flip-flop. Similarly, bit 7 is produced by the LTC monitor flip-flop.

During a programmed write operation (DATO, DATOB, or the write portion of DATIO, or DATIOB bus cycle), LKS L (LKS H inverted) and BDOUT L are ANDed to produce an active (high) WRITE LKS H signal. The leading edge of LKS H clocks the logical state of BDAL06 H into the LTC ENB flip-flop, enabling or disabling LTC interrupts. The LTC MON flip-flop, however, can be preset only during the write cycle. Note that the LTC MON flip-flop, when preset, is read as a logical 0 via the flip-flop's Q output; when the flip-flop is reset, it is read as a logical 1. BDAL07 L (0 = high) is ANDed with WRITE LKS H, producing a low signal that presets the flip-flop; MONITOR H then goes low.

Normally, the LTC ON/OFF input to E10-5 is passive (high), producing a low at E10-6 that enables AND gate input E13-12. When interrupts are enabled, LTC ENB (1) L enables E13-11 and E13-13 goes high. This signal then enables one input of the BEVNT L bus driver. The remaining bus driver input is the LTC H signal. Thus, when LTC H goes high, BEVNT L goes low, and the LTC interrupt request is presented to the processor.

The leading edge of LTC H also clocks the LTC MON flip-flop to the reset state, and MONITOR H goes true (high). MONITOR H conditions one input of the BDAL07 H bus driver. During a read cycle, DATI (or the read portion of the DATIO cycle), LKS L, and BDIN L are gated to produce an active (high) READ LKS H signal. READ LKS H enables both BDAL07 L and BDAL06 L bus drivers, gating the monitor and interrupt enable status bits onto the LSI-11 bus.

During both programmed read and write bus cycles, the KPV11 must

respond by asserting BRPLY L. READ LKS L and WRITE LKS L are ORed and applied to the BRPLY L to produce the appropriate device response according to LSI-11 bus protocol.

The optional console panel includes the LTC ON/OFF switch. When placed in the OFF position, J1-4 is low; E10-6 goes high, inhibiting E13-12 and LTC interrupt requests are disabled. The function can be disabled by removing W14.

When manual-only LTC operation is desired, W13 is removed and W12 is installed. E13-11 is continuously enabled and LTC interrupt requests can be disabled via the console panel LTC ON/OFF switch; W14 must be installed for this operation.

Bus Terminations

The KPV11-C provides 120 Ω bus termination, while the KPV11-B has 220 Ω bus terminations. Each bus signal line termination includes two resistors as shown in Figure 5. Termination resistors are contained in 16-pin dual-in-line packages that are physically identical to integrated circuit packages. Each package contains 14 terminations. Daisy-chained grant signals are jumpered but are not terminated. BIAKI L is jumpered to BIAKO L and BDMGI L is jumpered to BDMGO L.

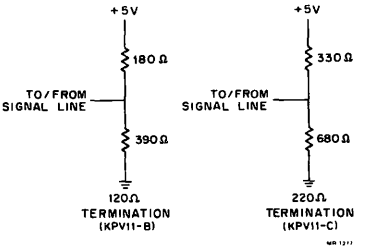


Figure 5 KPV11-B and KPV11-C Bus Terminations

Console Panel Interface

The option console panel interfaces with the system via the KPV11 module as shown in Figure 6. The DC ON indicator (D1) is driven directly by the DC ON H driver (Q6) in the power signal sequence circuit.

The RUN indicator is driven by the processor-generated SRUN L signal pulse. The 200 ms one-shot receives a continuous series of trigger pulses, when the processor is in the "run" (program execution) state,

that keeps the one-shot in the retriggered state. When in this state, the one-shot produces a high signal that turns the RUN indicator (D2) via the LED driver. When the processor is halted, the 200 ms one-shot times out, and the RUN indicator extinguishes.

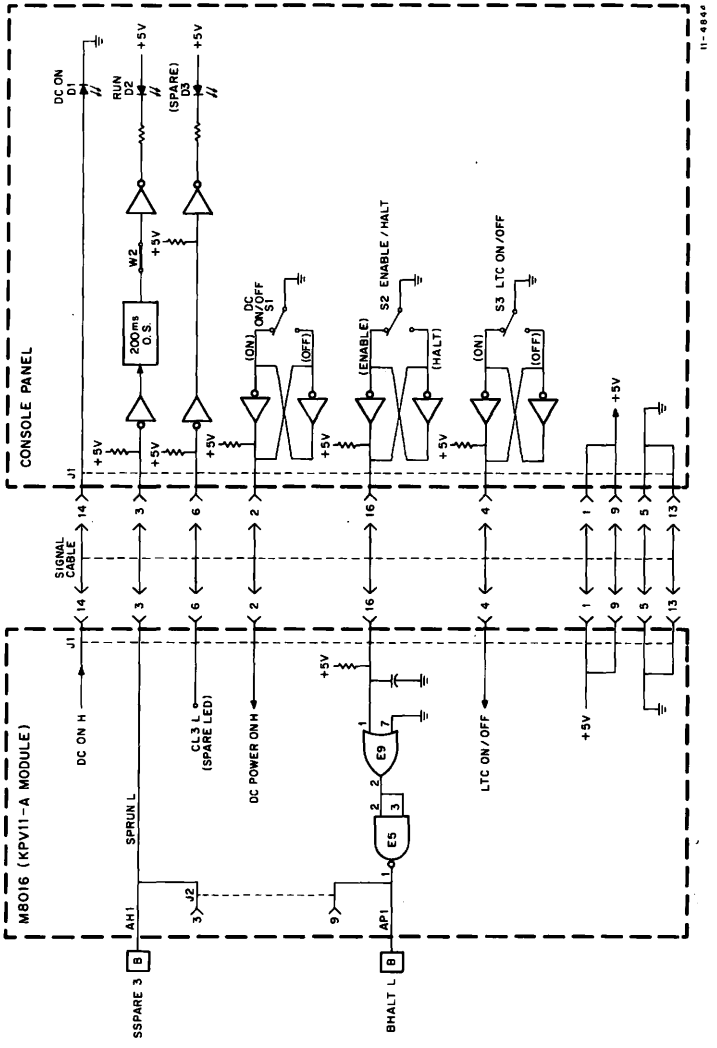


Figure 6 Console Panel Interface

The three console switches each include a "debounce" circuit composed of cross-coupled inverters. DC ON/OFF and LTC ON/OFF functions are used as previously described for power signal sequence and programmable line-time clock circuits, respectively.

The ENABLE/HALT switch enables the run mode (by not asserting BHALT L) or halts the processor; when halted, console ODT microcode operation is invoked. An R-C filter and BHALT L bus driver circuit on the KPV11 module interface this function to the LSI-11 bus.

CONFIGURATION

General

The KPV11 can be installed into any LSI-11 system backplane or into a remote installation (not installed in a backplane). All KPV11 installations require a user-supplied, 24 Vac, center-tapped transformer capable of supplying at least 0.2 A. Remote KPV11 installations also require the optional remote signal cable (part no. 70-12754). Users requiring manual control of the LTC and desiring the display of dc power on/off status and processor run/halt status need the optional console panel, console bezel, and console signal/power cable. Mounting hardware for the console panel and remote installation must be provided by the user.

Configuring LTC Jumpers

LTC jumpers are located on the KPV11 module as shown in Figure 7 and are factory-configured for programmable operation with the LKS (line clock status) register at address (177546) as shown in Figure 8. Normally, it will not be necessary to reconfigure LTC jumpers; however, it is possible to alter LTC operation as listed in Table 1 and the LKS device address as shown in Figure 8 and listed in Table 2.

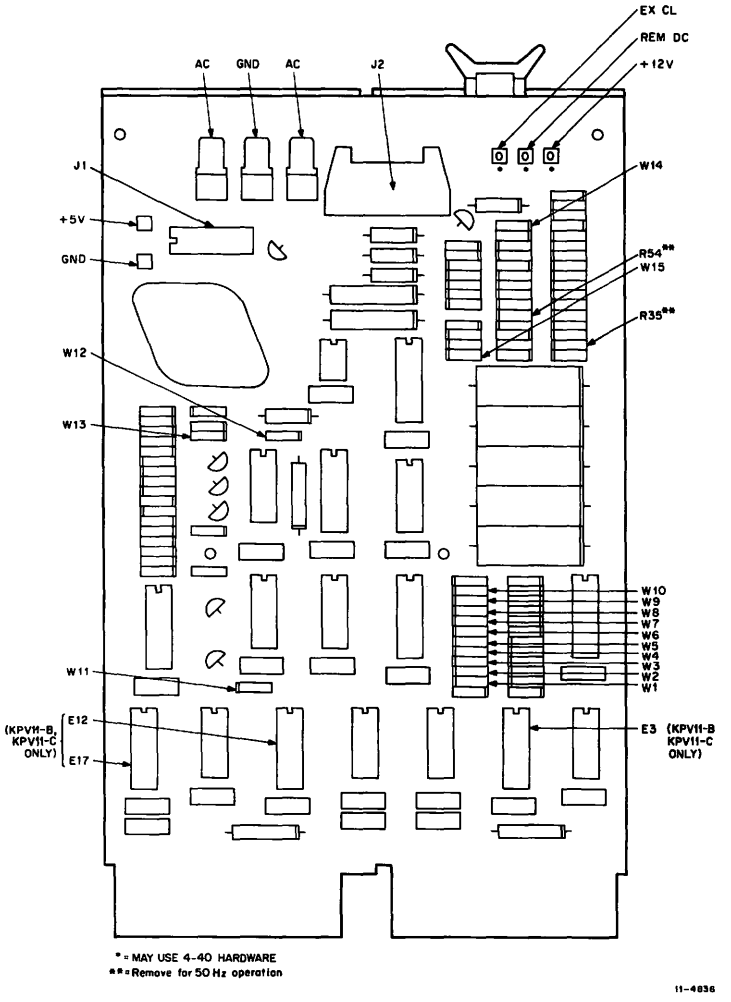


Figure 7 Jumper, Connector, Resistor, and Pad Locations

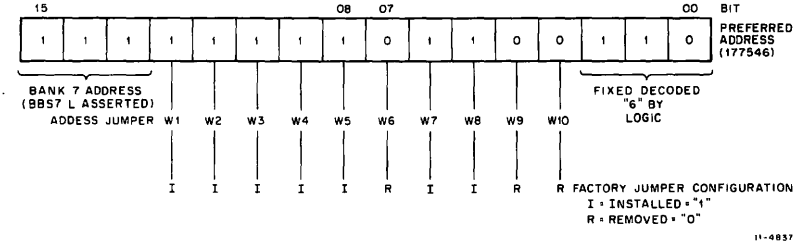


Figure 8 Device Address (LKS Register) Jumpers

Table 1 LTC Jumpers

Jumper	Installed	Removed
W12	Enable manual control or continuous LTC interrupt request operation. Do no install when W13 is installed.	*Disable continuous or manual operation.
W13	*LTC interrupt requests can be enabled and disabled by program. Do not install when W12 is installed.	LTC interrupt requests cannot be program controlled.
W14	*Console (optional) LTC ON/OFF switch enabled.	Console LTC ON/OFF switch disabled.
W15	*LTC signal occurs at the power line frequency.	LTC frequency is determined by an external source via EXT TIME REF etched pad on module.

* Factory-jumpered configuration

Table 2 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address
Register			
Line Clock Status	LKS	R/W	177546
Vector			
None			

Installation in the LSI-11 Backplane

The KPV11 module can be installed in any LSI-11 backplane. The KPV11 may be inserted into any option location when not used as a terminator. This option does not require the use of the daisy-chained grant signals (BIAK L and BDMG L) and is not priority dependent on device position in the backplane.

When used as a terminator (KPV11-B and KPV11-C), the module is inserted after the last module in the last backplane.

When the optional console panel is used with the terminator option and the RUN indicator is desired, the following must be performed.

- Insert the KPV11 module in the last option location in the backplane system.
- Connect a wire on the backplane from pin CH1 or AH1 on the KPV11 module to the SRUN L signal on the processor module. The wire must not exceed the length of the LSI-11 bus. This signal is located on pin AH1 of the processor.

Remote Installation

The KPV11 option can be mounted in a remote location (not installed in a backplane), as desired. Mounting holes are provided in the module for this purpose. Mounting details (mechanical) are shown in Figure 9.

NOTE

Program control of the LTC function and bus termination is not possible when remote installation is used. Hoever, manual control of the LTC function is available via the optional console panel.

Electrical connection between the KPV11 option and the LSI-11 bus is made via a 10-pin connector (J1) on the KPV11 and a 10-pin connector on the backplane (H9270 or DDV11-B) in which the processor is

installed. The optional signal cable (part no. 70-12754) provides the electrical connection between the two 10-pin connectors.

The +5 Vdc and +12 Vdc voltage sense input must be provided by the user when the KPV11 option is not installed in an LSI-11 backplane. Etched pads are provided on the KPV11 module for this purpose and

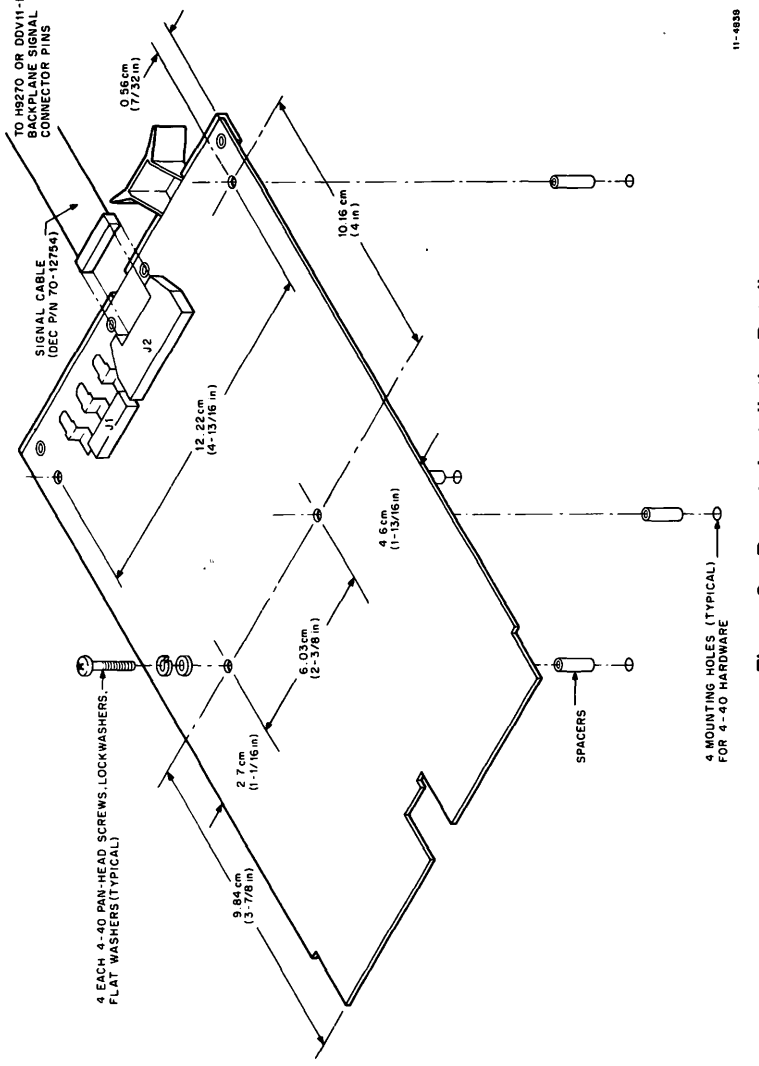


Figure 9 Remote Installation Details

are located as shown in Figure 7. Connect the +5V, +12V and GND pads to the respective LSI-11 backplane power terminals.

If the optional console panel is to be used and the RUN indicator function is desired, a wire must be installed between the SRUN L pin (pin 3) on the 10-pin connector on the backplane and the processor module pin AH1. A wire is normally factory-installed for this purpose on all backplanes except DDV11-B backplanes.

Power Sense Connections

Three tabs on the KPV11 are provided for connecting the option to a 24 Vac, center-tapped transformer. This 50 or 60 Hz input voltage produces the required dc operating voltages for the option, provides the 50 or 60 Hz reference for the LTC function, and is the power-fail monitor signal for the power signal sequence circuit. This voltage must be supplied by the user. A transformer can be connected as shown in Figure 7 for this purpose. When the KPV11 is used with a 50 Hz input voltage, resistors R35 and R54 must be removed for proper power-fail time to compensate for the change in frequency. The location of these resistors is shown in Figure 10.

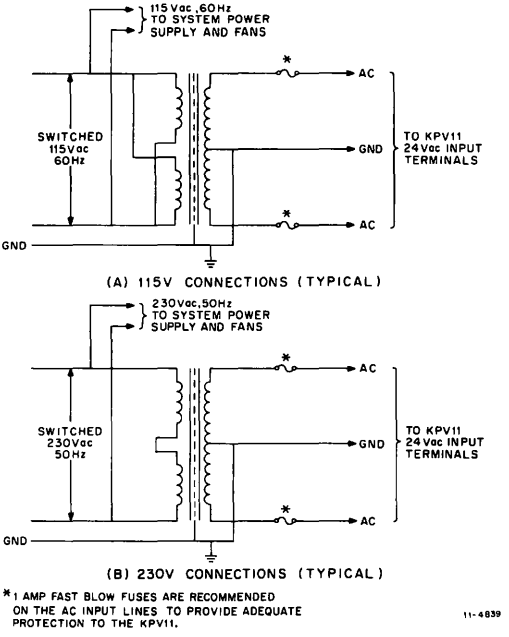


Figure 10 Power Line Monitor Transformer Installation

Installing Console Panel

The optional console panel can be mounted as shown in Figure 11. Electrical connections between the KPV11 and the console panel are made via 16-pin dual-in-line integrated circuit sockets located on each assembly. The electrical connection between the sockets is made using a signal/power cable (part no. 70-08612-OD).

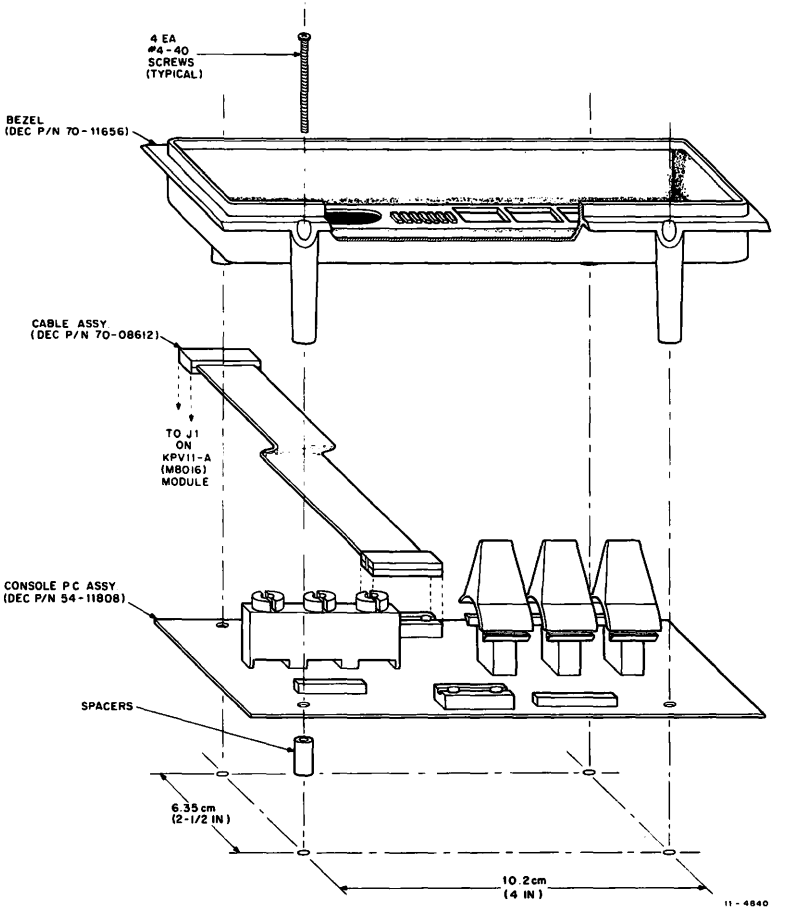


Figure 11 Console Panel Installation

In addition to the LTC ON/OFF and RUN/ENABLE switch functions, the console panel includes a DC ON/OFF switch. This switch, when in the OFF position, disables BDCOK H and BPOK H signal generation. If desired, this switch can also control the DC ON/OFF state of the user's power supply. This function is enabled by connecting the REMOTE DC ON/OFF and GND etched pads on the KPV11 module to an appropriate control circuit in the power supply. The signal thus produced is TTL-compatible and is capable of sinking 16 mA signal current in its logical low (DC ON) state. The logical high state is the DC OFF condition.

Using an External Reference

The KPV11 normally uses the 50 or 60 Hz input (via the three power tabs on the module) for LTC signal generation. However, an external frequency source may be used for producing LTC signals at frequencies other than the power line frequency. An etched pad is provided for this purpose on the KPV11 module. First, cut or remove jumper W15; this jumper and the external clock (EX CL) pad are located as shown in Figure 7. Then, connect the external frequency source to the EX CL and GND pads. The frequency source must be TTL logic-compatible; the KPV11 presents three TTL loads to the source.

Console Operation

The console panel option controls and indicators are shown in Figure 12 and described in Table 3.

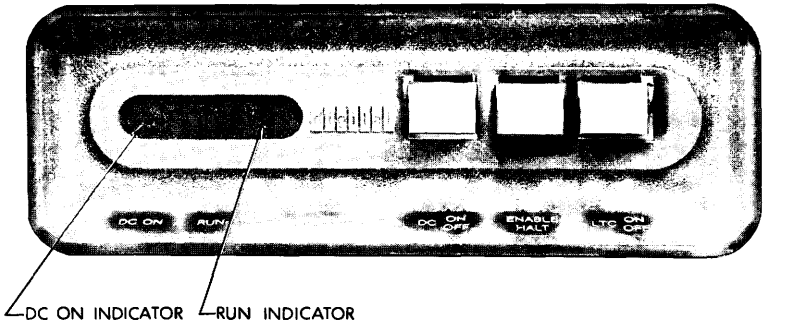


Figure 12 Console Panel Controls and Indicators
(P/N 54-11808 and 70-11656 shown)

Table 3 Console Panel Controls and Indicators

Control Indicator	Type	Function
DC ON	LED Indicator	Illuminates when the DC ON/OFF toggle switch is set to ON and proper dc output voltages are being produced by the user's power supply and sensed by the KPV11 option. If either the +5V or +12V output from the power supply is faulty, the DC ON indicator will not illuminate.
RUN	LED Indicator	Illuminates when the processor is in the run state (see ENABLE/HALT).
Spare	LED Indicator	
DC ON/OFF	Two-position Toggle Switch	When set to ON, enables dc outputs of the user's power supply (if connected to this function—see instructions for installing the console panel). The DC ON indicator will illuminate if the dc output voltages are of proper values. When set to OFF, the power supply dc out-

Table 3 Console Panel Controls and Indicators (Cont)

Control Indicator	Type	Function
		puts are disabled and the DC ON indicator is extinguished.
ENABLE/HALT	Two-position Toggle Switch	When set to ENABLE, the BHALT L line to the processor is not asserted and the processor is in the run-enable mode (RUN indicator is illuminated only when the processor is executing a program).
		When set to HALT, the BHALT L line is asserted. The processor halts program execution and executes console ODT microcode. The RUN indicator is extinguished.
LTC ON/OFF	Two-position Toggle Switch	When set to ON, enables KPV11 option generation of LTC interrupts. When set to OFF, disables LTC interrupts (W14 must be installed).

PROGRAMMING

Power-down and Power-up Routines — Power-down and power-up routine examples for systems using core memory are provided in Figures 13 and 14. The power-down routine shown provides an orderly power-down sequence of the system and saves the contents of the general-purpose registers along with the stack pointer and the Processor Status Word. Other device registers which the user desires save

during power-down can be included through the use of the MOV @ NAME–(SP) instruction.

The power-down routine is entered via the routine's starting address ($PWRDN) in interrupt vector location 24; location 26 should contain 200_8 to disable device interrupts during the power down sequence. The first MOV instruction temporarily replaces the power-down vector address with the address of a HALT instruction ($HLT). This prevents an erroneous power-up attempt during the power-down routine execution. A sequence of MOV instructions then saves register contents on the stack. The second from the last MOV instruction, however, saves the SP in location $SAVR6, which is dedicated by the program for this purpose. It is the last register saved by the routine. The starting address ($PWRUP) for the power-up routine is then written into location 24, replacing the temporary $HLT address. Finally, the program halts and the power-down sequence is completed.

```
$PWRDN:     MOV    #$HLT,@ #24       ;DISABLE FALSE
                                     ;RESTART SEQUENCE
            MOV    R0,—(SP)          ;PUSH R0 ON STACK
            MOV    R1,—(SP)          ;PUSH R1 ON STACK
            MOV    R2,—(SP)          ;PUSH R2 ON STACK
            MOV    R3,—(SP)          ;PUSH R3 ON STACK
            MOV    R4,—(SP)          ;PUSH R4 ON STACK
            MOV    R5,—(SP)          ;PUSH R5 ON STACK
            MOV    @NAME,—(SP)       ;SAVE ANY
                   .                 ;NECESSARY DEVICE
                   .                 ;REGISTERS
                   .
                   .
                   .
            MOV    SP,$SAVR6         ;SAVE SP
            MOV    #$PWRUP,@#24      ;SET POWER-UP
                                     ;VECTOR
$HLT:       HALT                     ;POWER-DOWN
                                     ;SEQUENCE
                                     ;DONE, READY FOR
                                     ;POWER-UP
                                     ;SEQUENCE
$SAVR6:     WORD 0                   ;SP SAVED HERE
```

Figure 13 Power-Down Routine Programming Example

```
$PWRUP:     MOV    #$ILLUP,@#24  ;SET FOR FAST DOWN
            MOV    $SAVR6,SP     ;GET SP
            MOV    (SP)+,@NAME   ;RESTORE ANY DEVICE
                   .             ;REGISTERS SAVED
                   .
                   .
                   .
            MOV    (SP)+,R5      ;POP STACK INTO R5
            MOV    (SP)+,R4      ;POP STACK INTO R4
            MOV    (SP)+,R3      ;POP STACK INTO R3
            MOV    (SP)+,R2      ;POP STACK INTO R2
            MOV    (SP)+,R1      ;POP STACK INTO R1
            MOV    (SP)+,R0      ;POP STACK INTO R0
            MOV    #$PWRDN,@#24  ;SET UP THE POWER-
                                 ;DOWN VECTOR
            TYPE                 ;REPORT THE POWER
                                 ;FAILURE
$PWRMG:     WORD   $POWER        ;POWER FAIL MESSAGE
            RTI                  ;POINTER
$ILLUP:     HALT                 ;THE POWER-UP
                                 ;SEQUENCE WAS
                                 ;STARTED
            BR     .2            ;BEFORE THE POWER-
                                 ;DOWN
                                 ;WAS COMPLETE
$POWER:     .ASCII <15><12>"POWER"
```

Figure 14 Power-Up Routine Programming Example

When power is restored, the power-up routine is entered via the routine's starting address ($PWRUP) in interrupt vector location 24. The power-up routine shown in Figure 14 uses the $HLT and $SAVR6 locations shown in the power-down routine for disabling false power-down sequences and restoring the stack pointer, respectively. The first two MOV instructions reference those locations. A sequence of MOV instructions that follow restore device and processor registers, respectively. The last MOV instruction writes the starting address ($PWRDN) for the power-fail routine in location 24, replacing the temporary $HLT address. Finally, the RTI instruction pops the PC and PS of the program where the power-down sequence occurs from the stack and normal program execution is restored.

Programming the LTC — The LTC function normally divides time into 16-2/3 ms or 20 ms intervals determined by the line frequency source (60 Hz or 50 Hz, respectively). It is possible to disable the line frequency source and use an external frequency source (user-supplied). The program communicates with the LTC function via the LKS register (Figure 15) contained in the KPV11 logic circuits. The LKS register's device address is normally configured to 177546 for system software compatibility.

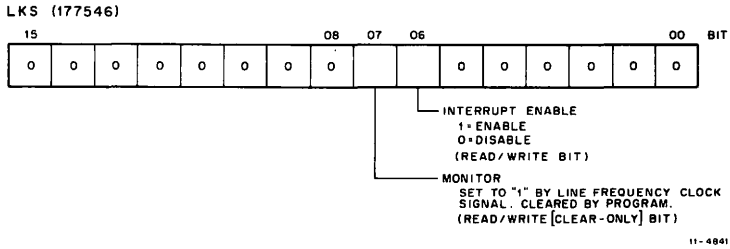


Figure 15 Line-Time Clock Status Register (LKS)

LTC interrupts, when enabled (LKS bit 6 = 1), occur as an interrupt request (bus low assertion) on the BEVNT L signal line. This causes the processor to execute a service routine via vector address 100. Memory location 100 must contain the PC (starting address) for the LTC service routine; similarly, memory location 102 must contain the PS (processor status word) for the service routine. As with all "external" interrupts, the processor will recognize the LTC interrupt request only when current PS bit 7 is cleared. When PS bit 7 = 1, external interrupts, including the LTC interrupt, are ignored. The LTC interrupt has highest priority of all external interrupts and does not require a vector address bus transfer. An interrupt request via the BEVNT L bus signal line, as previously stated, always results in access to the service routine via vector address 100.

The KPV11 is factory-configured for programmable operation as described above. If the user's hardware configuration also includes the optional console panel, the operator can disable or enable the LTC function by setting the LTC ON/OFF switch to the desired position. When set to the OFF position, the LC switch overrides program control and LTC operation is disabled. W14 must be installed for this function.

KWV11-A PROGRAMMABLE REAL-TIME CLOCK

GENERAL

The KWV11-A is a programmable clock/counter that provides a variety of means for determining time intervals or counting events. It can be used to generate interrupts to the processor at predetermined intervals, or to synchronize the processor ratios between input and output events. It can also be used to start the ADV11-A analog-to-digital converter either by clock counter overflow or by the firing of a Schmitt trigger.

The clock counter has a resolution of 16 bits and can be driven from any of five internal crystal-controlled frequencies (100 Hz to 1 MHz), from a line frequency input or from a Schmitt trigger fired by an external input. The KWV11-A can be operated in any of four programmable modes: single interval, repeated interval, external event timing, and external event timing from zero base.

The KWV11-A includes two Schmitt triggers, each with integral slope and level controls. The Schmitt triggers permit the user to start the clock, initiate A/D conversions, or generate program interrupts in response to external events.

FEATURES

- Resolution of 16 bits
- Can be driven by an external input or from any of five internal frequencies
- Four programmable modes
- Slope and reference signal level selection switches
- Can be used to start the ADV11-A analog-to-digital converter.

SPECIFICATIONS

Identification	M7952
Size	Quad
Power	+5 Vdc ±5% at 1.75 A +12 Vdc ±3% at 0.01 A
Bus Loads	
AC	3.4
DC	1
Operational	
Clock	
Accuracy	0.01%
Range	Base frequency (10 MHz) divided into five selectable rates (1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz); line frequency; Schmitt trigger 1 input

KWV11-A

Input Signals	
ST1 IN (Schmitt Trigger 1 Input)	
Input Range m(maximum limits)	−3V to +30V
Assertion Level	Depends upon position of slope reference selector switch and level control; triggering range = −12 V to +12V
Origin	User device
Response Time	Depends on input waveform and amplitude; typically 600 ns with TTL logic input
Hysteresis	Approximately 0.5V, positive and negative
Characteristics	Single-ended input; 100 KΩ impedance to ground
ST2 IN (Schmitt Trigger 2 Input)	
Same description as ST1 IN	
Output Signals	
CLK OV (Clock Overflow)	Low
Asserted Level	User device or ADV11-A
Destination	Approximately 500 ns
Duration	TTL open-collector driver with 470 Ω pull-up to +5V
Characteristics	Maximum source current from output through load to ground when output is high (≥2.4V): 5 mA
	Maximum sink current from external source voltage through load to output when output is low (≤0.8V): 8 mA
ST1 Out (Schmitt Trigger 1 Output)	
Same description as CLK OV	
ST2 Out (Schmitt Trigger 2 Output)	
Same description as CLK OV	

DESCRIPTION

General

Functions making up the KWV11-A are shown in Figure 1.

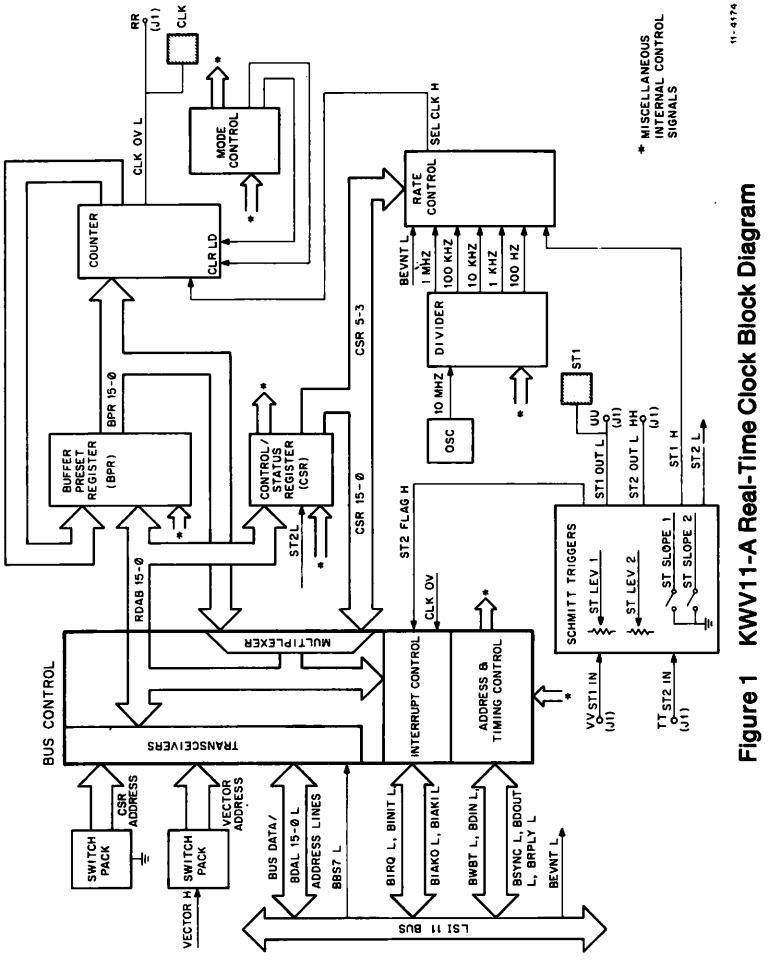


Figure 1 KWV11-A Real-Time Clock Block Diagram

The logic associated with the bus control block maintains proper communications protocol between the processor bus and the KWV11-A. This logic generates and monitors the bus signals involved during interrupts and data transfers between the processor and the KWV11-A. It permits the KWV11-A to recognize when it is being addressed by the processor (address defined by the address switch pack), to prescribe the location in memory pointing to the starting addresses of interrupt service routines (by means of the vector switch pack), to input control data from the processor, and to output data to the processor.

Interrupts can be enabled for both counter overflow and operation of ST2. Since each of these conditions raises a flag bit in the control/status register, and since separate interrupt vectors exist for each condition, the conditions may be distinguished either by vectors or by testing flag bits.

Control/Status Register

The control/status register (CSR) provides a means for the processor to control the operating of the KWV11-A and to derive information about its operation condition. Bits are provided for enabling interrupts, mode selection, maintenance operations, starting the counter, and overflow and Schmitt trigger event monitoring.

Mode Control

Logic circuitry associated with the mode control block permits KWV11-A operation in four different modes as specified by bits 2-1 of the CSR.

Mode 0 (Single Interval) — When the GO bit is set in this mode either by the processor or by a Schmitt trigger 2 event, the counter is loaded from the buffer/preset register (which has previously been loaded with the 2's complement of the number of counts desired before overflow). Once loaded, the counter will increment at the selected rate until it overflows. Overflow clears the GO bit, sets the Overflow flag, and interrupts the processor if that function has been enabled. If interrupt has not been enabled, the KWV11-A waits for processor intervention.

Mode 1 (Repeated Interval) — When the GO bit is set in this mode, the counter is loaded from the buffer/preset register (BPR) and is then incremented to overflow as for mode 0. In mode 1, however, overflow does not clear the GO bit; instead, it causes the counter to be reloaded from the BPR, raises the Overflow flag, initiates an interrupt sequence if the CSR Interrupt on Overflow bit is set, and causes the count to be continued with no loss of data.

Mode 2 (External Event Timing) — When the GO bit is set in this mode, the counter is set to 0 and then incremented at the selected rate as long as the GO bit remains set. An external signal to Schmitt trigger 2 (ST2) causes the current contents of the counter to be loaded into the BPR while the counter continues to run. At the same time, the ST2 flag is set and, if Interrupt 2 is enabled, an interrupt is generated, thus permitting the program to read the value held in the BPR.

The counter continues to run after the ST2 event and also continues to run after overflow. Interrupt on Overflow may be enabled to alert the program to the overflow condition.

Mode 3 (External Event Timing from Zero Base) — Operation in mode 3 is identical to that in mode 2 except that the counter is zeroed each time an ST2 event loads its contents into the BPR.

Flag Overrun — In all modes, if a second overflow occurs before the Overflow flag is reset (i.e., before a prior event is serviced by the processor), or if ST2 fires when the ST2 flag is already set, the Flag Overrun bit is set.

Oscillator, Divider, Rate Control Chain

The circuitry associated with these blocks provides the time base that is fed to the counter. The KWV11-A permits eight clock conditions to be specified by bits 5-3 of the CSR: STOP, 1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz, an external time base applied to ST1, and line frequency (50 or 60 Hz) picked up from bus line BEVNT. External periodic or aperiodic pulses may be applied to ST1 and counted.

Buffer/Preset and Counter Registers

The buffer/preset register is a word-oriented, 16-bit read/write register that can be loaded either under program control or from the counter. In modes 2 and 3, the firing of ST2 causes the BPR to be loaded with the contents of the counter. The BPR cannot be loaded by the program in these modes as long as the GO bit is set.

The counter is a 16-bit internal register accessible only by way of the BPR; in modes 2 and 3 it can be read indirectly through the BPR.

Schmitt Triggers

Both Schmitt triggers are equipped with switches to permit selecting slope direction (+ or −) and threshold reference level (TTL or −12V to +12V continously variable). Each Schmitt trigger is also equipped with a screwdriver-operated potentiometer to permit setting the variable threshold level. Switch pack and potentiometer terminals are all

brought to multiple connector J1 to permit attachment of external user-provided slope and level controls.

The two Schmitt triggers are used in somewhat different ways.

ST1 — Performs as an external time base input or external input for aperiodic signals to be counted. Outputs both to ST1 Faston connector to provide external start signals to ADV11-A and, through rate control circuitry, to permit selection as input to the counter. Maximum frequency varies as a function of input waveform.

ST2 — When the ST2 GO Enable bit is set, firing ST2 in any mode sets the GO bit and initiates counter action, causes the ST2 flag to be asserted, and generates an interrupt if that function is enabled. When the GO bit is set in modes 2 and 3, firing ST2 causes the buffer/preset register to be loaded from the counter, the ST2 flag to be set, and an interrupt to be generated if enabled.

CONFIGURATION

The following paragraphs describe the procedure for device and interrupt vector address selection, slope and reference level selection, user connections, and programming. (Refer to the ADV11-A when using the KWV11-A with that module.)

Device Address Selection

The KWV11-A contains two device registers that can be addressed by the processor. These registers are the control/status register (CSR) and buffer/preset register (BPR). The BPR's address is always equal to the CSR address plus two. Thus, only the CSR address is configured by the user, as shown in Table 1.

Table 1 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address
Register			
Control/Status	CSR	R/W	170420
Buffer/Preset	BPR	R/W	170422
Interrupts			
Clock Overflow	CLK OV	—	440
Schmitt Trigger 2	ST2	—	444

Switch pack S1 (Figure 2) contains 10 switches; each corresponds to an address bit as shown in Figure 3. The ON positions select a logical 1 bit address; similarly, the OFF positions select logical 0s. The CSR address can be configured for any address ranging from 17000 to 17777r, with the least significant octal digit configured for 0 or 4. The recommended KWV11-A CSR address is 170420; S1 is shown configured for this address in Figure 2. Note that the BPR address, based on the recommended CSR address, is 170422.

Interrupt Vector Selection

The KWV11-A can interrupt the processor for clock overflow and Schmitt trigger 2 (ST2) services. Thus, two interrupt vectors are produced by the KWV11-A. Switch pack S3 (Figure 4) selects the vector for the clock overflow interrupts; the ST2 interrupt vector is always equal to the clock overflow interrupt vector plus four. S3 contains seven switches (one not used) that correspond to vector bits (03:08), as shown in Figure 4. Configure the desired clock overflow interrupt vector shown in the figure. The recommended address is 000440.

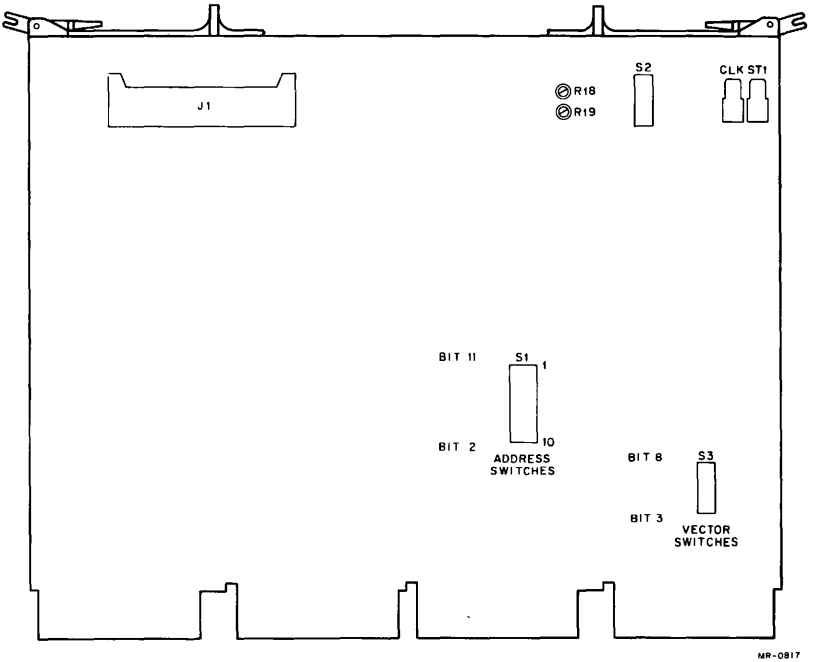


Figure 2 KWV11-A Connectors, Switches, and Controls

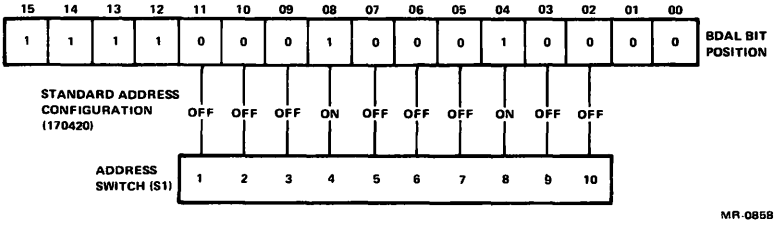


Figure 3 KWV11-A CSR Address Switches

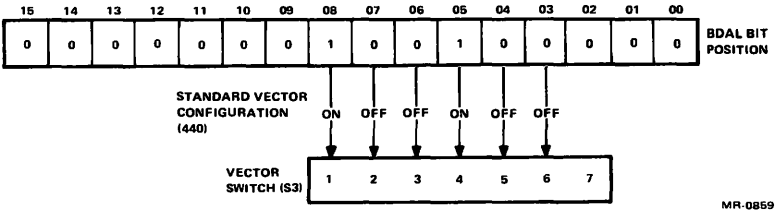


Figure 4 KWV11-A Vector Address Switches

Slope and Reference Level Selection

Slope and reference level switches and controls are shown in Figures 2 and 5. Two reference modes are selectable for each Schmitt trigger—one that picks a fixed level appropriate to TTL logic, and one that picks a variable level that permits setting the ST threshold to any point between −12V and +12V.

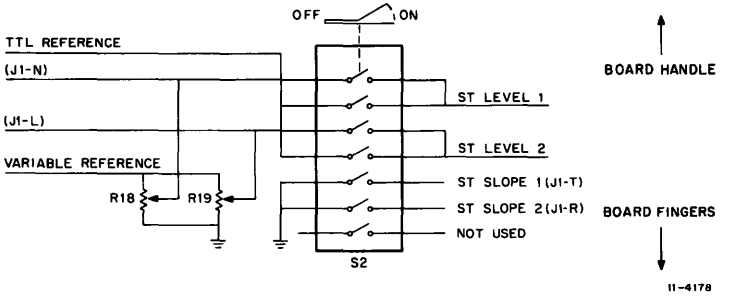


Figure 5 KWV11-A Slope/Reference Level Selector Switches and Controls

Slope selection is accomplished by separate switches for ST1 and ST2, respectively. When the related switch is on, the firing point effectively occurs on the positive slope of the input waveform. When the switch is off, the firing point occurs on the negative slope. R18 or R19 is used to set the level of the reference. Typical slope selection is shown in Figure 6.

NOTE

Users should take care that both TTL and variable switches for either Schmitt trigger are not on simultaneously. This condition will not damage components, but produces unpredictable reference levels. Note also that if no signal is connected to a Schmitt trigger input, both threshold switches for that ST should be open for noise immunity. Alternatively, ST1 IN and ST2 IN can be grounded externally.

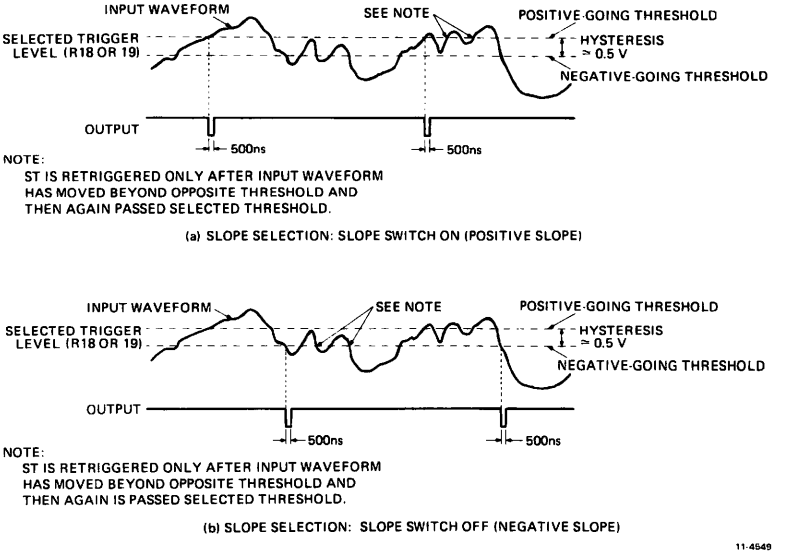


Figure 6 KWV11-A Slope Selection

Register Format

CSR Bit Assignments — CSR bit assignments are identified in Figure 7 and defined in Table 2.

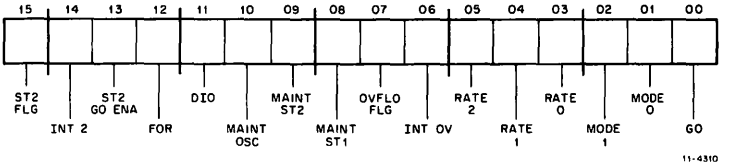


Figure 7 CSR Bit Assignments

Table 2 KWV11-A CSR Bit Definitions

Bit/CSR Name	Set By/Cleared By	Remarks
15/ST2 Flag Read/write to 0	Set by the firing of Schmitt trigger 2 or the setting of the MAINT ST2 bit in any mode while the GO bit or the ST2 Go Enable bit is set. Cleared under program control. Also cleared at the "1"-going transition of the GO bit unless the ST2 Go Enable bit has previously been set.	Must be cleared after servicing an ST2 interrupt to enable further interrupts. When cleared, any pending ST2 interrupt request will be cancelled. If enabled interrupts are requested at the same time by bits 7 and 15, bit 7 has the higher priority.
14/INT 2 (Interrupt on ST2) Read/write	Set, and cleared under program control.	When set, the assertion of ST2 Flag will cause an interrupt. If set while ST2 Flag is set, an interrupt is initiated. When cleared, any pending ST2 interrupt request will be cancelled.

Table 2 KWV11-A CSR Bit Definitions (Cont)

Bit/CSR Name	Set By/Cleared By	Remarks
13/ST2 Go Enable Read/write	Set and cleared under program control. Also cleared at the "1"-going transition of the GO bit.	When set, the assertion of ST2 flag will set the GO bit and clear the ST2 Go Enable bit.
12/FOR (Flag Overrun) Read/write	Set when an overflow occurs and the Overflow flag is still set from a previous occurrence, or when ST2 fires and the ST2 flag is already set. Cleared under program control and at the "1"-going transition of the GO bit.	This bit provides the programmer with an indication that the hardware is being asked to operate at a speed higher than is compatible with the software.
11/DIO (Disable Internal Oscillator) Read/write	Set and cleared under program control.	For maintenance purposes, this bit inhibits the internal crystal oscillator from incrementing the clock counter. Used in conjunction with bit 10.
10/MAINT OSC Write-only	Set under program control. Clearing is not required. Always read as a 0.	Setting this bit simulates the firing of Schmitt trigger 2. All functions initiated by ST2 can be exercised under program control by using this bit.
9/MAINT ST2 Write-only	Set under program control. Clearing is not required. Always read as a 0.	Setting this bit simulates the firing of Schmitt trigger 2. All functions initiated by ST2 can be exercised under program control by using this bit.

Table 2 KWV11-A CSR Bit Definitions (Cont)

Bit/CSR Name	Set By/Cleared By	Remarks
8/MAINT ST1 Write-only	Set under program control. Clearing is not required. Always read as a 0.	Setting this bit simulates the firing of ST1. All functions initiated by ST1 can be exercised under program control by using this bit.
7/OVFLO FLAG Read/write to 0	Set each time the counter overflows. Cleared under program control and at the "1"-going transition of the GO bit.	If bit 6 is set, bit 7 will initiate an interrupt. Bit 7 must be cleared after the interrupt has been serviced to enable further overflow interrupts. If cleared while an overflow interrupt request to the processor is pending, the request is cancelled. If enabled interrupts are requested at the same time by bits 7 and 15, bit 7 has the higher priority.
6/INTOV (Interrupt on Overflow) Read/write	Set and cleared under program control.	When this bit is set, the assertion of OVFLO FLAG will generate an interrupt. Interrupt is also generated if bit 6 is set while OVFLO FLAG is set. If cleared while an overflow interrupt request to the processor is pending, the request is cancelled.

Table 2 KWV11-A CSR Bit Definitions (Cont)

Bit/CSR Name	Set By/Cleared By	Remarks
5-3/RATE Read/write	Set and cleared under program control.	These bits select clock counting rate or source. **5 4 3 Rate** 0 0 0 STOP 0 0 1 1 MHz 0 1 0 100 kHz 0 1 1 10 kHz 1 0 0 1 kHz 1 0 1 100 Hz 1 1 0 ST1 1 1 1 Line (50/60 Hz)
2-1/MODE Read/write	Set and cleared under program control.	**Function 2 1** Mode 0: 0 0 Mode 1: 0 1 Mode 2: 1 0 Mode 3: 1 1
0/GO Read/write	Set and cleared under program control. Also cleared when the counter overflows in mode 0.	Setting this bit initiates counter action as determined by the rate and mode bits. In modes 1, 2, and 3 it remains set until cleared. In mode 0 it clears itself when counter overflow occurs. Clearing bit 0 clears and inhibits the counter.

Buffer/Preset Register (BPR) — The BPR is a 16-bit, word-oriented, read/write register. Any attempt to write a byte into this register will result in a whole word being written. In modes 0 and 1, the program may load it with the 2's complement of the number of counts desired before overflow. In modes 2 and 3, it permits indirect reading of the clock counter.

Normal Control Sequences — Mode 0 (Single Interval)
Control code for operation in mode 0 must support the following sequence:

1. The control program writes the desired count (2's complement) into the BPR.
2. The program writes the control code into the control/status register as indicated in Table 3.
3. If the GO bit is set high, KWV11-A responds by loading the 16-bit counter from the BPR and enabling the counter; if the GO bit is set low and the ST2 Go Enable bit is set high, KWV11-A waits for an ST2 event, then sets the GO bit and loads and enables the counter.
4. The counter increments until overflow, then halts (GO bit is cleared).
5. KWV11-A raises the Overflow flag and issues an interrupt if the CSR INT OV bit is set; if the interrupt is not enabled, KWV11-A waits for program intervention.
6. The program responds to the interrupt or intervenes in consequence of other criteria (e.g., testing the Overflow flag or the A/D Done flag if overflow was used to start an A/D conversion). The program reads the CSR, clears the Overflow flag, and if no counting or mode changes are required, sets the GO bit or the ST2 GO ENABLE bit to re-enter the sequence at step 3.

Table 3 CSR Bit Settings for Mode 0, Single Interval

Bit No.	CSR Name	Bit Condition as Written by Processor	Remarks
15	ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of GO bit assertion except when ST2 GO ENA has previously been set.
14	INT 2	x	Set to 1 by program if interrupt on ST2 event is desired.

Table 3 CSR Bit Settings for Mode 0, Single Interval (Cont)

Bit No.	CSR Name	Bit Condition as Written by Processor	Remarks
13	ST2 GO ENA	x	Set to 1 by program if GO is to be set by external signal to ST2. Cleared by leading edge of GO bit assertion.
12	FOR	(0)	Will be set to 1 by counter overflow. Always cleared by leading edge of GO bit assertion.
11	DIO	0	
10	MAINT OSC	0	
9	MAINT ST2	0	
8	MAINT ST1	0	
7	OVFLO FLG	(0)	
6	INT OV	x	Set to 1 by program for interrupt on counter overflow.
5	RATE 2	x	
4	RATE 1	x	See Table 2.
3	RATE 0	x	
2	MODE 1	0	Set by program to 0.
1	MODE 0	0	Set by program to 0.
0	GO	x	Set by program to 1 unless ST2 GO ENA is set; remains 1 until written to 0 by program. Cleared when counter overflows.

X = 0 or 1, depending on user requirements.
(0) = Automatically cleared by GO bit assertion.

Mode 1 (Repeated Interval)
Control code for operation in mode 1 must support the following sequence:

1. The control program writes the desired count (2's complement) into the BPR.
2. The program writes the control code into the CSR as indicated in Table 4.
3. If the GO bit is set high, KWV11-A responds by loading the 16-bit counter from the BPR and enabling the counter; if the GO bit is set low and the ST2 GO ENABLE bit is set high, KWV11-A waits for ST2 event, then sets the GO bit and loads and enables the counter.
4. The counter increments until overflow.
5. KWV11-A reloads the counter from the BPR, re-enables the counter, raises the Overflow flag in the CSR, and issues an interrupt to the processor if interrupt is enabled.
6. If a second overflow occurs before the first is serviced (i.e., if Overflow flag is still high when next overflow occurs), the KWV11-A Flag Overrun (FOR) bit in the CSR is set high to alert the program that data has been lost.
7. The program responds to the interrupt or intervenes in consequence of other criteria. The program reads the CSR, clears the Overflow flag, and if no counting or mode changes are required, sets the GO bit or the ST2 Go Enable bit to re-enter the sequence at step 3.

Table 4 CSR Bit Settings for Mode 1, Repeated Interval

Bit No.	CSR Name	Bit Condition as Written by Processor	Remarks
15	ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of GO bit assertion except when ST2 GO ENA has previously been set.
14	INT 2	x	Set to 1 by program if interrupt on ST2 event is desired.

Table 4 CSR Bit Settings for Mode 1, Repeated Interval (Cont)

Bit No.	CSR Name	Bit Condition as Written by Processor	Remarks
13	ST2 GO ENA	x	Set to 1 by program if GO is to be set by external signal to ST2. Cleared by leading edge of GO bit assertion.
12	FOR	(0)	Will be set to 1 by counter overflow. Always cleared by leading edge of GO bit assertion.
11	DIO	0	
10	MAINT OSC	0	
9	MAINT ST2	0	
8	MAINT ST1	0	
7	OVFLO FLG	(0)	
6	INT OV	x	Set to 1 by program for interrupt on counter overflow.
5	RATE 2	x	
4	RATE 1	x	See Table 2.
3	RATE 0	x	
2	MODE 1	0	Set by program to 1.
1	MODE 0	1	
0	GO	x	Same as for Mode 0, except that bit is not cleared when counter overflows.

X = 0 or 1, depending on user requirements.
(0) = Automatically cleared by GO bit assertion.

Mode 2 (External Event Timing)

Control code for operation in mode 2 must support the following sequence:

1. The program writes the control code into the CSR as indicated in Table 5.
2. KWV11-A responds by incrementing the counter (cleared when

the GO bit was cleared) at the selected rate until the GO bit is set to 0.

3. ST2 pulse loads the current counter contents into the BPR, sets the ST2 flag, and generates an interrupt if INT 2 is enabled.
4. Overflow sets OVFLO FLG high and, if INT OV bit is high, generates an interrupt.
5. The counter continues to increment until the processor sets the GO bit to 0.

Normally, the program enables the INT 2 and/or INT OV bits, permitting the processor to synchronize its operations with the external ST2 events and prevent loss of data by reinitializing the process after step 4.

Table 5 CSR Bit Settings for Mode 2, External Event Timing

Bit No.	CSR Name	Bit Condition as Written by Processor	Remarks
15	ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of GO bit assertion except when ST2 GO ENA has previously been set.
14	INT 2	x	Set to 1 by program if interrupt on ST2 event is desired.
13	ST2 GO ENA	x	Set to 1 by program if GO is to be set by external signal to ST2. Cleared by leading edge of GO bit assertion.
12	FOR	(0)	
11	DIO	0	
10	MAINT OSC	0	
9	MAINT ST2	0	
8	MAINT ST1	0	

Table 5 CSR Bit Settings for Mode 2, External Event Timing (Cont)

Bit No.	CSR Name	Bit Condition as Written by Processor	Remarks
7	OVFLO FLG	(0)	Will be set to 1 by counter overflow. Always cleared by leading edge of GO bit assertion.
6	INT OV	x	Set to 1 by program for interrupt on counter overflow.
5	RATE 2	x	
4	RATE 1	x	See Table 2.
3	RATE 0	x	
2	MODE 1	1	Set by program to 2.
1	MODE 0	0	
0	GO	x	Set by program to 1 unless ST2 GO ENA is set; remains 1 until written to 0 by program. Cleared when counter overflows.

X = 0 or 1, depending on user requirements.
(0) = Automatically cleared by GO bit assertion.

Mode 3 (External Event Timing from Zero Base)
Operation is identical to that in mode 2 except that the counter is cleared after the ST2 pulse. The counter continues to increment until the GO bit is set to 0.

Note that the interval between two ST2 events may be measured directly in mode 2 or 3 with processor assistance if the CSR ST2 Go Enable and interrupt 2 bits are set before the first event and the GO bit is left clear. Under these conditions, the first ST2 event will set the GO bit (and thus start the counting process) and simultaneously issue an interrupt. If the interrupt service routine now clears the ST2 flag bit, the next ST2 event will cause the BPR to be loaded from the counter in the normal mode 2 fashion. The choice of mode 2 or mode 3 for such

measurements will depend on whether or not an on-going accumulation of time after the second event is required by the application. If such an accumulation is necessary, mode 2 is appropriate since the counter is not cleared after ST2 events.

User Connections

A 40-pin type 854 connector (J1) is provided on the KWV11-A for user connections as shown in Figure 8. This connector will mate with an H856 connector. External user-supplied slope and level controls can be interfaced via this connector as shown in Figure 9. J1 can be connected to the optional H322 distribution panel for convenient user access, via an optional BC08R cable.

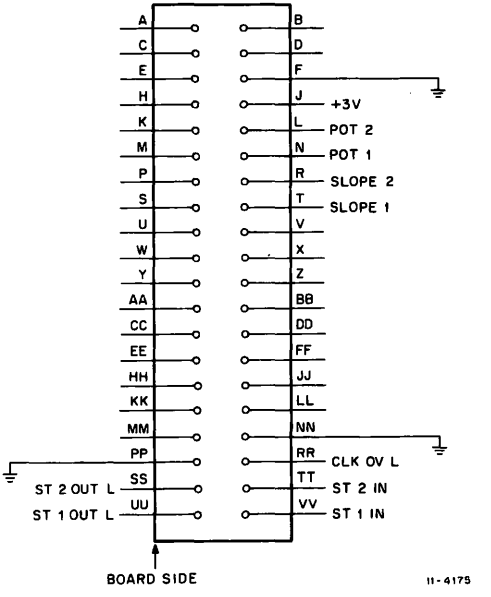
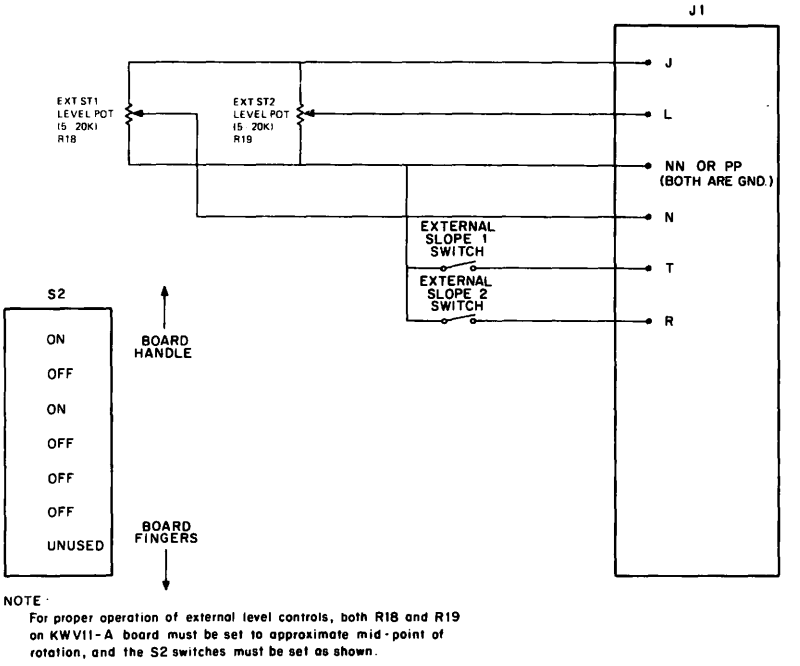


Figure 8 J1 40-Pin Connector Pin Assignments



NOTE:
For proper operation of external level controls, both R18 and R19 on KWV11-A board must be set to approximate mid-point of rotation, and the S2 switches must be set as shown.

Figure 9 Connecting External User-Supplied Slope and Level Controls

In addition, two tabs (CLK and ST1) are located on the module as shown in Figure 2. These tabs are electrically connected to J1 pins RR (CLK OV L) and UU (ST1 OUT L); the tabs may be used to connect the KWV11-A functions to ADV11-A TAB S (external start) and TAB C (clock overflow), respectively, in an ADV11-A. Optional jumpers (DEC part no. 70-10771) are available for this purpose.

PROGRAMMING

Record the point in double-precision timeframe for each S12 event following GO. The program makes use of a 32-bit counter, the low-order bits of which are taken directly from the KWV11-A (KWBPR) and the high-order bits of which are taken from a software counter (HICNT) that is incremented with each KWBPR overflow.

```
                MTPS    #0                      ;CLEAR PSW
                MOV     #ST2SRV, @ST2VEC        ;LOAD ST2 VECTOR
                                                ;ADDR
                MOV     #200,@ST2PSW            ;SET UP PSW FOR ST2
                                                ;INTERRUPT (DISABLE
                                                ;ALL SUBSEQUENT
                                                ;INTERRUPTS)
                MOV     #OVSRV, @OVVEC          ;LOAD OV VECTOR
                                                ;ADDR
                MOV     #200,@OVPSW             ;SET UP PSW FOR OV
                                                ;INTERRUPT (DISABLE
                                                ;ALL SUBSEQUENT
                                                ;INTERRUPTS)
                 .
                 .
                MOV     #BUFFER, R0             ;SET UP POINTER TO
                                                ;BEGINNING OF
                                                ;BUFFER AREA
CLKGO:          MOV     #40115,@KWCSR           ;DEPOSIT 1MHZ, MODE 2,
                                                ;INT OV EN, INT ST2 EN,
                                                ;AND GO INTO KWCSR
COUNT:          WAIT                            ;FOR INTERRUPT
                                                ;BY OVFLO OR ST2
                BIT     #100000,@KWCSR          ;IS FOR BIT SET?
                BEQ     COUNT                   ;NO, CONTINUE
                JMP     FORSRV                  ;YES, SERVICE FLAG
                                                ;OVERRUN CONDITION
OVSRV:          BIT     #100000,@KWCSR          ;IS ST2 FLAG SET?
                BEQ     2$                      ;NO, CONTINUE
                TST     @KWBPR                  ;DID ST2 OCCUR BEFORE OV?
                BPL     2$                      ;NO, BRANCH
                MOV     HICNT,(R0)+             ;YES, SERVICE ST2 FIRST
                MOV     @KWBPR,(R0)+
                BIC     #100000,@KWCSR          ;ACKNOWLEDGE ST2
                                                ;OCCURRENCE
```

LAV11 PRINTER OPTION

SPECIFICATIONS

Identification	M7949
Size	Double
Power	+5 V ±5% at 0.8 A
Bus Loads	
AC	1.8
DC	1

CONFIGURATION

The LAV11 interface module is shipped from the factory with jumpers and switches configured for standard (Digital Equipment Corporation software-compatible) device and interrupt vector assignments. It is normally not necessary for the user to configure the address or vector switches unless special device addresses or interrupt vectors are desired. The factory-installed jumpers and switches are shown in Figure 1. The jumpers can be removed by carefully cutting each end close to the printed circuit board. Table 1 lists the special jumpers and the associated function they control when the jumper is installed on the interface.

LAV11

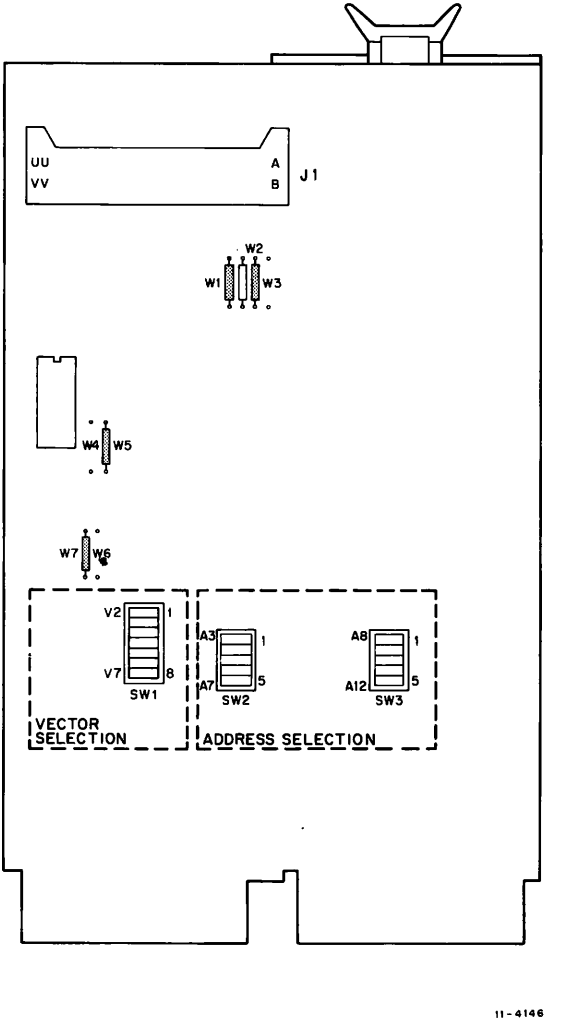


Figure 1 LAV11 Switch and Jumper Locations

Table 1 Special Jumpers

Jumper	Shipped Condition*	Function if Inserted
W1	I	Transmit parity on line
W2	I	+5 Vdc sense from LA180
W3	R	+5 Vdc sense from LAV11
W4	R	DEMAND is asserted low
W5	I	DEMAND is asserted high
W6	R	P STROBE is asserted low
W7	I	P STROBE is asserted high

* I = inserted, R = removed

Device Address

The device address is selected by setting switches 1 to 5 in switch banks 2 and 3 to the standard address (Table 2). The LAV11 has a factory-set standard address of 177514 for the device control/status register. The data buffer register (DBR) is always set at the next address following the CSR address. The standard address for the DSR is 177516. If more than one LAV11 option is installed in the system, or if special device addresses are desired, set the switches (one for each CSR address bit) as directed in Figure 2.

Interrupt Vector

The interrupt vector is selected by setting switches 1 through 8 in the switch bank to the standard vector. The LAV11 module has a factory-set standard interrupt vector of 200_8. If more than one LAV11 option is installed in the system or if a special interrupt vector is desired, set the switches (one for each vector address bit) as directed in Figure 3.

Table 2 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address	Second Module Address
Registers				
Control/Status	LPCSR	R/W	177514	(Use floating
Data Buffer	LPDSR	R/W	177516	address space)
Interrupt				
Done or Error	—	—	200	(Use floating vector space)

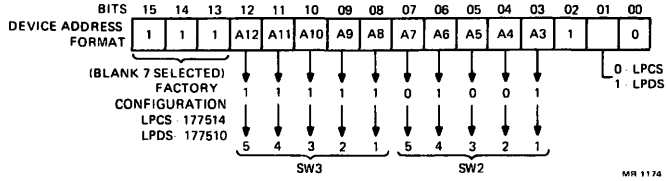


Figure 2 LAV11 Device Address Format

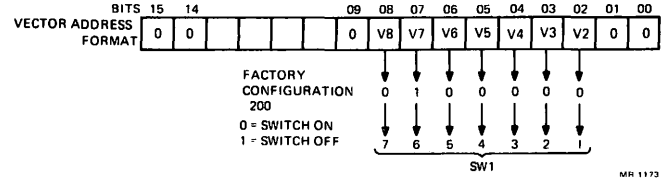


Figure 3 LAV11 Interrupt Vector Format

Parity(W1)
This jumper will allow a parity bit to be transmitted to the LA180 when inserted. Removing the jumper will disable the parity bit.

+5 Vdc Sense (W2, W3)
These jumpers allow the user to sense 5 Vdc from either the LA180 printer or the LAV11 interface. To sense the 5 Vdc from the LA180, leave W2 installed and remove W3. To sense 5 Vdc from the interface module, leave W3 installed and remove W2. Under no condition should both jumpers be installed or removed.

Demand (W4, W5)
These jumpers allow the user to assert INTERNAL DEMAND from the LA180 on either a low level (zero) or a high level (one). For a low level, the user will leave W4 installed and remove W5. For a high level, the user will leave W5 installed and remove W4. Under no condition should both jumpers be installed or removed.

P Strobe (W6, W7)
These jumpers allow the user to assert P STROBE on either a low level (zero) or a high level (one). For a low level, the user will leave W6 installed and remove W7. For a high level, the user will leave W7 installed and remove W6. Under no condition should both jumpers be installed or removed.

LA180 to LAV11 Interface Cable

The only acceptable cable for use between the LA180 and the LAV11 is the BC11S. The cable end labeled P2 must be attached to the LA180. The end labeled P1 must be attached to the LAV11.

LA180 Modifications

Jumper W6 must be inserted on the LA180 logic board (54-11023). This insures +5 Vdc sense to the LAV11. Failure to insert this jumper will result in a continued error condition in the LAV11 LACS buffer.

Device Registers

All software control of the LAV11 is performed by means of two device registers. Each register has been assigned a bus address and can be read or loaded (with the exceptions noted) using any instruction that refers to those addresses.

The following discussion presents the bit assignments within the two device registers. Bits referenced as "unused" and "write-only" are always read as zeros. Loading "unused" and "read-only" bits has no effect on those bits.

Control and Status Register (CSR) — The address of the CSR is 177514 and the register data contains the control and status of the system. The data bit assignments are shown in Figure 4; the bit assignments are described in Table 3.

Data Buffer Register (DBR) — The address of the DBR is 177516 and the register contains the data being processed by the system. The data bit assignments on the register are shown in Figure 5; the bit assignments are described in Table 4.

Interrupt Servicing

Both the error and done bits are enabled by the same CSR bit (interrupt enable). When granted, the interrupt occurs using the vector block at location 200_8 (interrupt vector is limited to location 777_8). These bits do not occur in the set condition simultaneously. When servicing an interrupt, therefore, the routine must check the state of error and done in the CSR (bits 15 and 7) to determine which of the two flags caused the interrupt. Because the LAV11 is normally connected to the LSI-11 bus BIRQ L line, servicing the LAV11-originated interrupt request depends upon its closeness to the processor via the daisy-chain network.

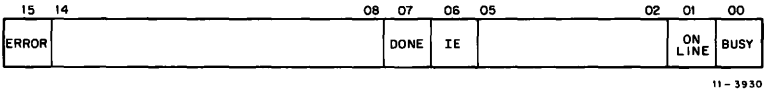


Figure 4 LAV11 CSR Bit Assignments

Table 3 LAV11 CSR Bit Definitions

Bit: 15 **Name:** Error
Description: The error bit is asserted when an error condition (i.e., torn or no paper) exists in the LA180. This is a read-only bit which is reset only by manual correction of the error condition.

Bit: 14-8 **Name:** Unused

Bit: 7 **Name:** Done
Description: The done bit is asserted when the printer is ready to accept another character. This is a read-only bit set by INIT. The done bit is cleared by loading the LADB register. An interrupt sequence is started if IE (interrupt enable, bit 6) is also set.

Bit: 6 **Name:** Interrupt Enable
Description: The interrupt enable bit is set or cleared (read or write bit) under program control. It is cleared by the INIT signal on the LSI-11 bus. (INIT is caused by a programmed reset instruction, a console start function, or a power-up or power-down condition.) When IE is set, an interrupt sequence is started if either error or done is also set.

Bit: 5-2 **Name:** Unused
Bit: 1 **Name:** On-line
Description: The on-line bit is asserted when the LA180 printer (only) is on-line. It is a read-only bit.

Bit: 0 **Name:** Busy
Description: The busy bit is asserted when the LA180 printer (only) is performing a print or paper advance operation.

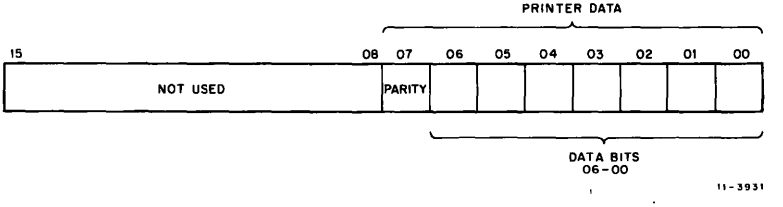


Figure 5 LAV11 DBR Bit Assignments

Table 4 LAV11 DBR Bit Definitions

Bit: 15-8 **Name:** Unused

Bit: 7 **Name:** Parity
Description: The parity bit is loaded with the data word if the parity jumper is installed. It is a write-only bit.

Bit: 6-0 **Name:** Data
Description: The data character comprises seven bits, bit 6 being most significant. This buffered 7-bit character will be transferred to the LA180. These bits are all write-only bits.

LPV11 PRINTER OPTION

GENERAL

The LPV11 printer option is a high-speed line printer system for use with an LSI-11 system. The system consists of an LPV11 interface module, an interface cable, and a line printer (either an LP05 or LA180). The LPV11 interface module functions that are used with an LP05 or LA180 line printer are similar; however, the printer strobe signals required for each printer are different. The specific interface cable allows the interface module to detect which printer it is interfacing to, and automatically supplies the correct timing signals for the specific type of printer. The interface module is program-controlled to transfer data from an LSI-11 bus to the line printer. There are 12 option numbers that define the type of printer and four primary power (line) voltages. Printer types include the LA180 DECprinter and two LP05 line printer models (uppercase letters only, and both uppercase and lowercase letters). These models and their interface cables are defined in Table 1.

Table 1 LPV11 Option Model Numbers

Option No. (Model)	Interface Cable*	Primary Power	Model	Printer Description
LPV11-PA	BC11S-25	115V, 60Hz	LA180-PA	180 char/sec printer, 132 column, upper- and lowercase letters
LPV11-PB	BC11S-25	230V, 60Hz	LA180-PB	
LPV11-PC	BC11S-25	115V, 50Hz	LA180-PC	
LPV11-PD	BC11S-25	230V, 50Hz	LA180-PD	
LPV11-VA	70-11212-25	115V, 60Hz	LP05-VA	300 line/min printer,132 column, uppercase letters only
LPV11-VB	70-11212-25	230V, 60Hz	LP05-VB	
LPV11-VC	70-11212-25	115V, 50Hz	LP05-VC	
LPV11-VD	70-11212-25	230V, 50Hz	LP05-VD	
LPV11-WA	70-11212-25	115V, 60Hz	LP05-WA	240 line/min printer, 132 column upper-and lower-case letters
LPV11-WB	70-11212-25	230V, 60Hz	LP05-WB	
LPV11-WC	70-11212-25	115V, 50Hz	LP05-WC	
LPV11-WD	70-11212-25	230V, 50Hz	LP05-WD	

* 7.62 m (25 ft) interface cable is supplied with each option.

LPV11

FEATURES

- Models available for 115 or 230 Vac operation at either 50 or 60Hz
- Line printers available with 132-column upper- and lowercase letters, or uppercase only
- Line printers available with speeds of 180 characters per second (LA180), or 300 or 240 lines per minute (LP05)
- Interface module and interface cable supplied.

SPECIFICATIONS

Module	
Identification	M8027
Size	Double
Power	+5V ±5% at 0.8 A
Bus Loads	
AC	1.4
DC	1
Interface Cable	
Type	BC11S-25 or 70-11212-25, depending on LPV11 model (see Table 1)
Length	7.62 m (25 ft) maximum
LP05 Line Printer	
Power	115 Vac ±10% 50/60 Hz ±3 Hz or 230 Vac ±10% 50/60 Hz ±3 Hz 700 W
Printable Characters	
64-Character set	!"#$%&'()*+,->/0123456789:;<=>?@ ABCDEFGHIJKLMNOPQRS TUVWXYZ[\]↑_
96-Character set	All of the above plus a through z: ~
Type	Open Gothic print
Size	Typically 0.024 cm (0.095 in.) high; 0.065 cm (0.025 in.) wide

LPV11

Code Format	ASCII
Characters per line	132
Character drum speed	64-character drum: 1200 r/min 96-character drum: 800 r/min
Printer Characteristics	
Format	Top-of-form control; single line advance with automatic perforation step-over, and carriage return. Automatic vertical format control is optional.
Paper-Feed	One pair of pin-feed tractors for 1.27 cm (½ in.) hole center, edge-punched paper.
Paper Slew Speed	50.8 cm (20 in.) per second
Print Area	33.53 cm (13.2 in.) wide, left justified
Character Spacing (horizontal)	0.254 ±0.0127 cm (0.1 ±0.005 in.) between centers; maximum possible accumulative error for normal spacing is 0.0254 cm (0.-01 in.) per 80- or 132-character line.
Line Spacing	0.424 ±0.025 cm (0.167 ±0.01 in.) at 6 lines per inch; 0.3175 cm (0.125 in.) at 8 lines per inch. Each character within ±0.254 cm (0.1 in.) from mean line through character.
Line Advance Time	50 msec maximum
Character Synchronization	Variable reluctance pick-off senses drum position.
Physical Characteristics	
Height	1.14 m (45 in.)
Width	0.81 m (32 in.)
Depth	0.56 m (22 in.)
Weight	150 kg (330 lb.)

LPV11

Ribbon Characteristics	
Type	Inked roll
Width	38.1 cm (15 in.)
Length	18.288 m (20 yd)
Thickness	0.01 cm (0.004 in.)
Paper Characteristics	
Type	Standard fanfold, edge punched, 27.94 cm (11 in.) between folds
Width	10.16 cm to 42.55 cm (4 in. to 16-3/4 in.)
Weight	15-lb. bond minimum (single copy) 12-lb. bond with single-sheet carbon for up to six parts (multiple copy)
Environmental	
Operating Temperature	10° to 32° C (50° to 90° F)
Humidity	30 to 90% (no condensation)
Print Rates	
LP05-VA, -VB, -VC, -VD (64-character drum)	300 lines per minute
LP05-WA, -WB, -WC, -WD (96-character drum)	240 lines per minute

LA180 DECprinter

Power	90-132 Vac or 180-264 Vac 50 or 60 Hz ±1 Hz 400 W max (printing) 200 W max (idle)
Printable Characters	96 upper- and lowercase character set (7 × 7 dot matrix): +,-./0123456789 :;<=>?@ ABCDEFGHIJK LMNOPQRS TUVWXYZ [\]↑_abcdef ghijklmnopqr stuvwxyz {|}~!"#$%&'()*

LPV11

Code Format	ASCII
Non-printable Characters	Six Commands: BEL, BS, LF, FF, CR, DEL
Number of Characters per Line	132 max
Type of Character Transfer	Parallel (7-bit plus parity)
Printer Characteristics	
Print Cycle Speed	Up to 180 characters per second
Line Printing Speeds	70 lines per minute on full line 300 lines per minute on short lines
Print Size	0.254 cm (10 characters per inch) horizontal 0.233 cm (6 lines per inch) vertical

DESCRIPTION

General

The M8027 interface module comprises functions that control the flow of data between the LSI-11 bus and the line printer (see Figure 1). The interface signals are different for the LP05 and the LA180 line printers, but the LPV11 detects a ground in the interface cable, and automatically configures itself for the proper printer. Each function of the interface is described in the following paragraphs. The LA180 and LP05 strobe timing diagrams are shown in Figures 2 and 3.

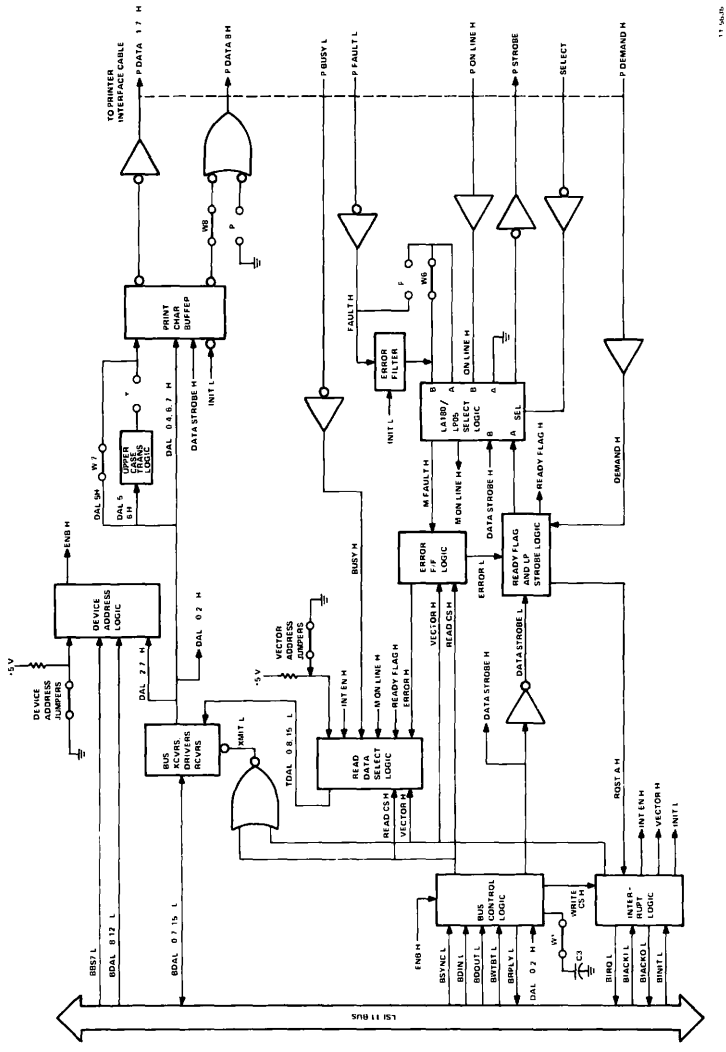
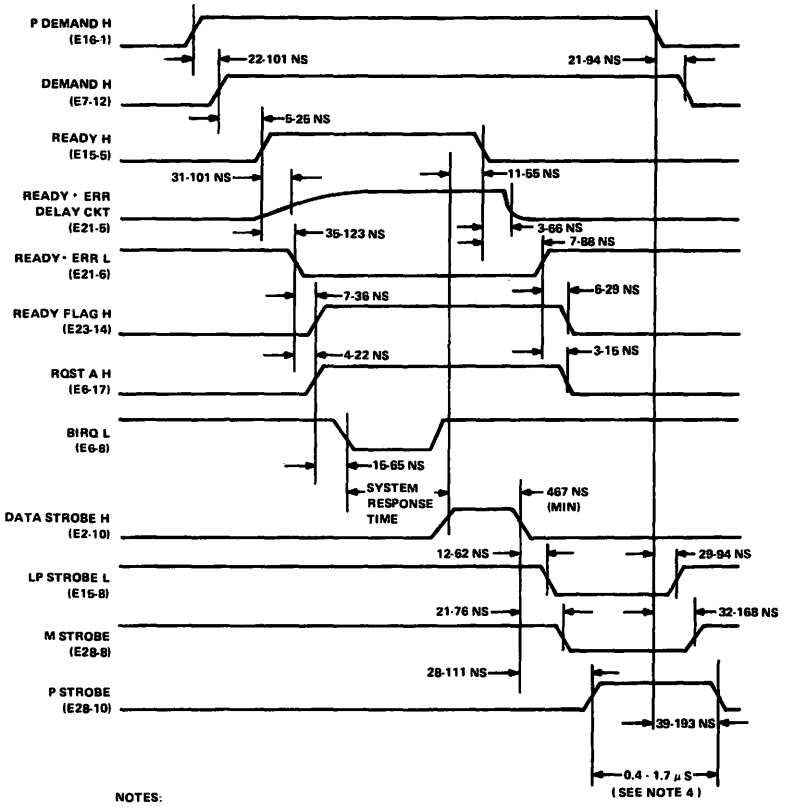


Figure 1 LPV11 Interface Logic Functions

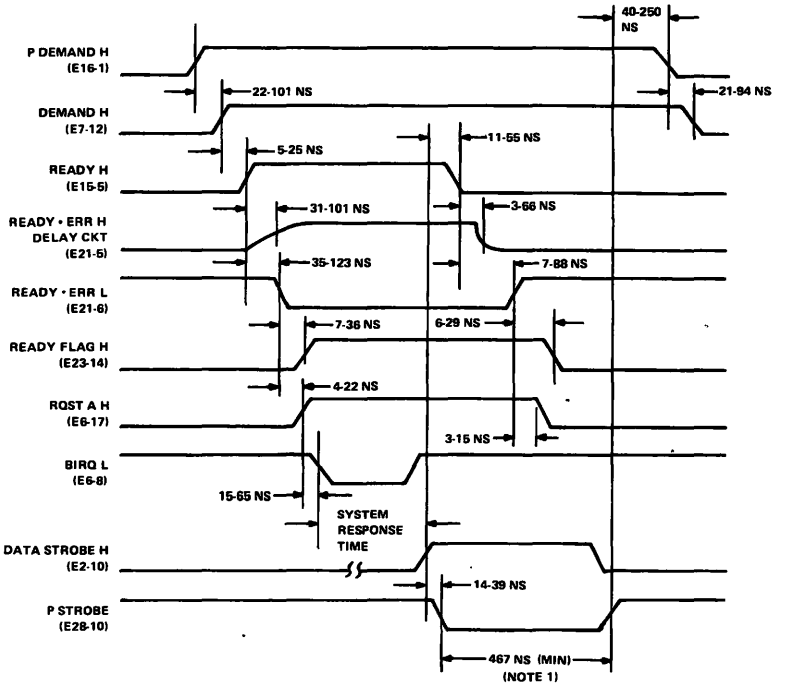


NOTES:

1. TIMING SHOWN IS TYPICAL, AND SHOWN FOR REFERENCE PURPOSES ONLY
2. TIMING SHOWN WITH JUMPER W1 INSTALLED
3. ( ) = INTEGRATED CIRCUIT PINS.
4. TIME IS DETERMINED BY LP05 PRINTER LOGIC.

11-5638

Figure 2 LP05 Internal Timing



NOTES:
1. JUMPER W1 INSTALLED (REQUIRED) FOR TIMING SHOWN.
2. TIMING IS TYPICAL, AND SHOWN FOR REFERENCE PURPOSES ONLY.
3. ( ) = INTEGRATED CIRCUIT PINS.

11-5637

Figure 3 LA180 Internal Timing

Bus Transceivers and Drivers

Bus transceivers (DEC 8641) receive the LSI-11 bus BDAL (0:7) L signals and distribute the bits on DAL (0:7) H lines. In addition, they transmit LPCS bits or interrupt vector address bits during a DATI bus cycle or interrupt sequence. Bus drivers (DEC 8881) transmit LPCS bits 8 and 15 during a DATI bus cycle in which the LPCS is addressed.

Device Address Decoding

Device address decoding logic receives DAL (2:7) H, BDAL (8:12) L, and BBS7 signals and compares the address to the device address jumpers; when the LSI-11 bus address bits 2 through 15 equal the jumper-configured address for the LPV11, ENB H goes active. Note that address bits 13, 14 and 15 are not decoded by the LPV11; the processor asserts BBS7 when these bits are all logical 1s, indicating an address is present in bank 7. In addition, address bits (0:2) are decoded for the device register (and byte) in the bus control logic. Bus control logic programmed transfer functions are enabled by the active ENB H signal.

Print Data Transmission

Print data is transmitted to the printer from the LSI-11 bus under program control. The print character buffer functions as the LPDB register. It is an 8-bit register, including the optional parity/D8 bit. The bus control logic produces WRITE DB H during a DATO or DATOB bus cycle in which the LPDB is addressed. Jumper W8 can be removed to disable program transfer of LPDB bit 7 to the printer. When W8 is removed, P DATA 8 is forced low; if desired, jumper P can be installed to force P DATA 8 high.

Uppercase translation logic gives the user the option to print upper/lowercase data files on an uppercase letters-only printer (LP05-VA, VB, VC, VD). Software overhead is reduced by performing the lowercase to uppercase translation in hardware, rather than in software. Jumper W7 normally applies unmodified upper/lowercase ASCII characters to the print character buffer. When the lowercase to uppercase letters translation is desired, jumper W7 is removed and jumper T is installed. The result is that ASCII codes 140 through 177 are translated to 100 through 137 (bit 5 = 0), as shown in Table 2.

Read Data Select Logic

Read data select logic functions enable the processor to read the LPCS register under program control or the LPV11's interrupt vector during an interrupt transaction. Control signals READ CS H and VECTOR H select the bits. LPCS bits are produced by various LPV11 interface functions as shown in Figure 1.

Table 2 Uppercase-Only Code Translation

ASCII Input		ASCII Output	
Code	Character	Code	Character
140	‘	100	@
141	a	101	A
142	b	102	B
143	c	103	C
144	d	104	D
145	e	105	E
146	f	106	F
147	g	107	G
150	h	110	H
151	i	111	I
152	j	112	J
153	k	113	K
154	l	114	L
155	m	115	M
156	n	116	N
157	o	117	O
160	p	120	P
161	q	121	Q
162	r	122	R
163	s	123	S
164	t	124	T
165	u	125	U
166	v	126	V
167	w	127	W
170	x	130	X
171	y	131	Y
172	z	132	Z
173	{	133	[
174	|	134	\
175	}	135	]
176	↑	136	↑
177	DEL	137	-

Ready Flag and LP Strobe Logic

The ready flag (LPCS bit 7) and line printer (LP) strobe logic provide the proper control signal interface to the printer. The LP strobe function is used only for LP05 printers. The LA180 uses the DATA STROBE H signal generated by the bus control logic. Selection of the appropriate strobe source is automatically produced by the LA/LP select logic function. Connecting the proper interface cable for the LA180 grounds the SELECT line, causing the LA/LP select logic to select LA180 (data selector port B) functions. When the LP05 is used, the interface cable does not ground the line and LP05 (data selector Port A) functions are selected. The LA180 strobe is a negative-going pulse. The LP05 strobe is a positive-going pulse initiated by the leading edge of P DEMAND H and cleared by the trailing edge of P DEMAND H.

The ready flag is produced by the logic function when the printer is requesting a character (P DEMAND H goes active) and no error is present. In addition to setting the LPCS ready flag, the RQST A signal input to the interrupt logic goes active; if interrupts are enabled (LPCS bit 6 is set), an interrupt request is initiated (BIRQ L goes active). The ready flag is cleared by an active DATA STROBE L signal when writing a new character into the print character buffer.

When an error condition occurs in the printer, the printer asserts P FAULT L. The fault is applied to the error flip-flop logic (via the M FAULT H signal), producing an active ERROR L signal and an active ERROR H signal (LPCS bit 15). The ready flag logic function responds by not producing a ready flag, although P DEMAND H may be active, and by producing an active RQST A H signal. Thus, an error conditon will initiate an interrupt request (if LPCS bit 6 is set) and set LPCS bit 15. The error flag is cleared by the processor reading the LPCS register if the ready flag is not set, or when the LPV11 interrupt vector is read.

Error Filter

The error filter is always used (automatically selected) with the LA180 printer and jumper-selected for optional use with the LP05 printer. This function is produced by a clock pulse generator/counter circuit that requires an active P FAULT L signal for 8 ms before the M FAULT H signal is produced. The minimum time requirement for the fault signal presence prevents false errors due to noise.

BRPLY Delay

Bus control logic generation of BRPLY L signals is delayed 400 ns (approximately) by factory-installed jumper W1. W1 connects C3 to

the DC004 RxCx input pin, delaying the BRPLY L signal for proper operation with LA180 printers. When LP05 printers are used, the jumper may be either left installed or removed to reduce the BRPLY delay, as desired.

Initialization

The processor initializes devices on the LSI-11 bus by asserting BINIT L. BINIT L is received by the interrupt logic and distributed as the INIT L signal. INIT L clears the print character buffer, error flip-flop logic, and interrupt enable bit (LPCS bit 6), and sets the ready flag.

LP05 Line Printers

LP05 printers use a 132-column, 64- (LPV11-VA, -VB, -VC, -VD) or 96- (LPV11-WA, -WB, -WC, -WD) character rotating drum, and solenoid-driven hammers to print characters. Characters are transmitted to the LP05's print buffer under program control via the M8027 interface module. The LP05 print buffer stores up to a 132-character line. Each print cycle is initiated by a terminating character. Terminating characters include carriage return (CR), line feed (LF), and form feed (FF). Printing requires two revolutions of the drum. Odd-numbered and even-numbered columns are printed during alternate revolutions of the drum. Circuits in the LP05 scan the print buffer characters stored for a line in synchronization with the rotating drum. Each character is printed, as appropriate, by driving the hammmer for those odd- or even-numbered columns in which a particular character appears. An inked ribbon and paper pass between the drum and the hammers, and thus the characters are printed.

Note that LP05 printers are available with uppercase letters only (64-character set) or upper- and lowercase letters (96-character set), depending on the model. All models are capable of printing numerals and punctuation marks.

LA180 DECprinter

The LA180 DECprinter included with LPV11-PA, -PB, -PC, and -PD models is a free-standing, pedestal-type impact printer that is capable of printing a maximum of 132 characters per line. To initiate a print cycle, a line terminator character (LF, FF, or CR) is required. The printer contains a 256 by 8 character buffer, which stores printable and nonprintable characters. This buffer is loaded character-by-character via the LPV11 interface under program control. After each character is stored in the buffer, a read function is performed to determine if the character is a line-terminator character. If it is, the characters

stored in the buffer are printed; if it is not, the next characters are input until the complete line is stored, as indicated when the line-terminator character is received and stored.

Each character is transferred to the printer as a parallel 7-bit ASCII-plus-optional parity code. The printer is a high-speed dot matrix printer that prints at speeds up to 180 characters per second. It produces a hard copy original plus up to five duplicate copies on tractor-driven, continuous forms, varying in width from 10.2 cm (4 in) to 37.8 cm (14-7/8 in). The average printing speeds are 70 lines per minute on full lines. The printer responds only to codes representing the LA180 character set and six command characters. All other codes are ignored.

CONFIGURATION

General

The M8027 interface module is shipped from the factory with jumpers configured for standard (DIGITAL software-compatible) device and interrupt vector assignments. It is normally not necessary for the user to configure the address or vector jumpers, unless special device addresses and/or interrupt vectors are desired. The factory-installed jumpers are shown in Figure 4. These jumpers can be removed by carefully cutting each end close to the printed circuit board. In addition to the factory jumpers, there is an alternate set of wire-wrap pins that allow the user to install additional or replacement jumpers by using the designated wire-wrap pins. In Figure 4, the dots represent wire-wrap pins and a line indicating a pair of pins shows the electrical connection that must be wire-wrapped to insert that jumper. Table 3 lists the factory jumpers that can be installed and the additional jumpers installed, as well as the associated functions. The factory-set addresses are listed in Table 4.

NOTE

Jumpers F+ (factory-installed W6) and F− do not have associated wire-wrap pins. These jumpers must be installed by soldering and removed by cutting or unsoldering.

Table 3 Jumper Designations

Jumper*	Function	Jumper*	Function
A3	Device Address	P	Parity
A4(W2)	Device Address	T(W7)	Translate to Uppercase
A5(W3)	Device Address	V2(W9)	Interrupt Vector
A6	Device Address	V3(W10)	Interrupt Vector
A7(W4)	Device Address	V4(W11)	Interrupt Vector
A8	Device Address	V5(W12)	Interrupt Vector
A9	Device Address	V6(W13)	Interrupt Vector
A10	Device Address	V7	Interrupt Vector
A11	Device Address	V8(W14)	Interrupt Vector
A12	Device Address	W1	Bus Reply Timing
F(W6)	Error Filter		

* Jumpers without W designation are not normally installed by factory.

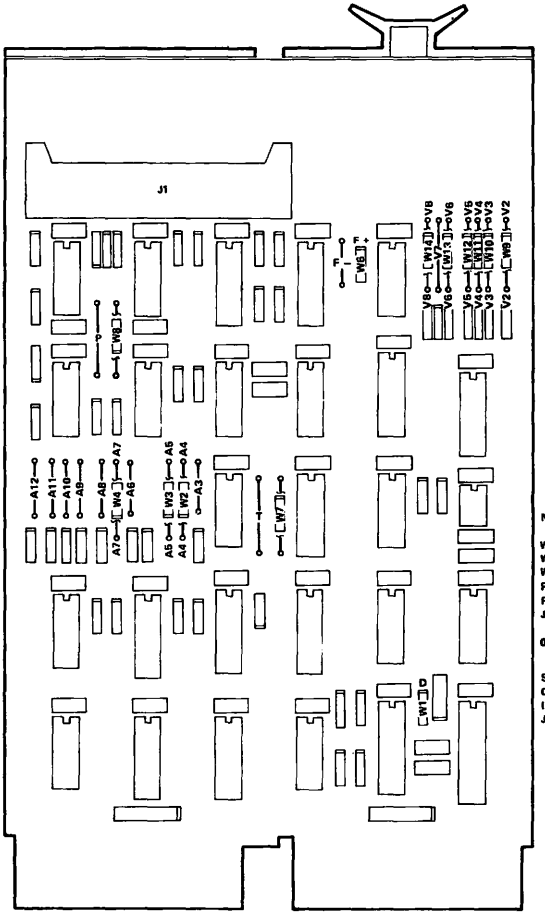


Figure 4 LPV11 Interface Module

Table 4 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address	Second Module Address
Registers				
Control/Status	LPCS	R/W	177514	(Use floating
Data Buffer	LPDB	R/W	177516	address space)
Interrupts				
Done or Error		—	200	(Use floating vector space)

Device Address

The LPV11 is factory-configured for a device control/status register (CSR) address equal to 177514. The data buffer register (DBR) is always the configured CSR address +2; thus, the standard DBR address is 177516. If more than one LPV11 option is installed in the system, or if special device addresses are desired, remove and/or install jumpers (one for each CSR address bit) as directed in Figure 5.

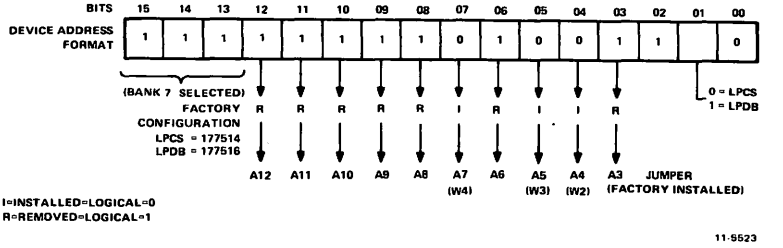


Figure 5 LPV11 Device Address Format and Jumpers

Interrupt Vector

The LPV11 is factory-configured for an interrupt vector equal to 200_8. If more than one LPV11 option is installed in the system, or if a special interrupt vector is desired, remove and/or install jumpers (one for each vector bit) as directed in Figure 6.

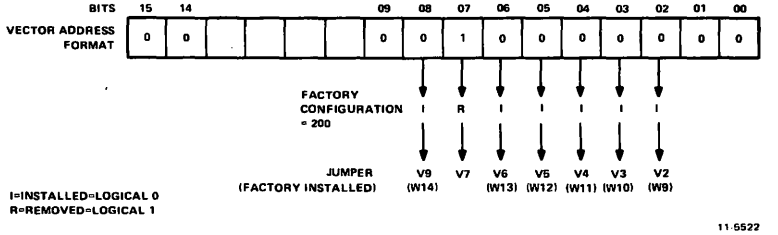


Figure 6 LPV11 Interrupt Vector Format and Jumpers

Bus Reply Timing

Jumper D (W1) is factory-installed to delay the BRPLY L bus signal timing for LPV11 use with LA180 printers. If desired, this jumper can be removed for use with future printers; however, the LP05 will function if it is left installed.

Uppercase Only

Jumper W7 is factory-installed and jumper T is not installed, enabling upper- and lowercase letters to be printed. If lowercase letters are not desired, remove W7 and install jumper T. This will cause the LPV11 interface to translate all lowercase letters to uppercase letters before transmission to the printer. This feature will allow printing files configured for 96-character printers on 64-character printers with minimum software overhead.

Do not configure the module with both jumpers W7 and T installed.

Parity

Jumpers W8 and P select the desired parity mode. The LPV11 is factory-configured with W8 installed and jumper P not installed, enabling parity bit 7 to be transmitted to the printer. Configure the parity option desired as follows:

Parity Option	Jumper W8	Jumper P
Normal parity bit	Installed	Removed
No parity, bit 7 low	Removed	Removed
No parity, bit 7 high	Removed	Installed

Do not configure the module wih both jumpers W8 and P installed.

NOTE

If the LPV11 interface module is used with an LP05 printer equipped with the Direct Access Vertical Form Unit (DAVFU), it is recommended that the user remove jumper W8. The LPV11 interface module does not support the DAVFU function.

Error Filter

The LPV11 interface module contains an error filter (time delay) circuit that is automatically selected when the module is used with an LA180 DECprinter. Jumper F+ (W6) is factory-installed, selecting the error filter for use with LP05 printers; however, its use with LP05 is optional. If desired, remove the error filter by removing jumper W6 and installing jumper F−. Do not configure the module with both F− and W6 installed.

LPV11 Device Registers

All programmed communication with the LPV11 option is via two device registers in the LPV11 interface module. These registers include the line printer control and status (LPCS) and line printer data buffer (LPDB). These registers are factory-configured with LSI-11 bus addresses 177514 and 177516, respectively, and are software-compatible with DIGITAL software. However, if additional LPV11 options are added to the system, or if the user requires addresses other than those factory-configured, it will be necessary to alter interface module jumpers and provide an LPV11 program using these special device addresses. Each register is described in Tables 5 and 6 and both are shown in Figure 7.

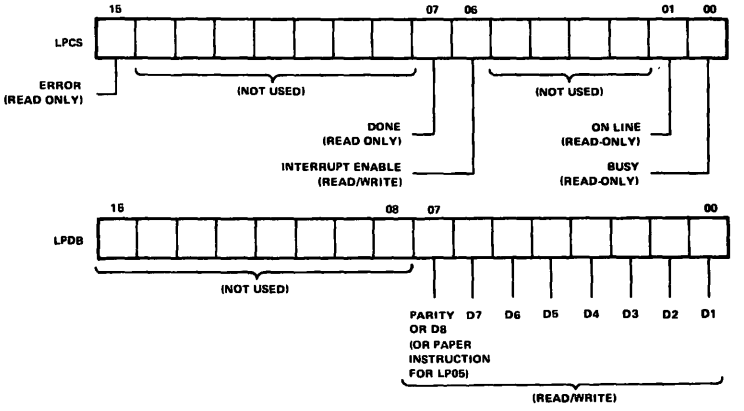


Figure 7 LPV11 Word Formats

Table 5 LPCS Register Bit Functions

Bit: 15 **Name:** Error
Description: Asserted (1) whenever an error condition exists in the line printer. Error conditions include:

LP05 Errors

1. Power off
2. No paper
3. Printer drum gate open
4. Over-temperature alarm
5. PRINT INHIBIT switch off
6. Printer off-line
7. Torn paper

LA180 Errors

1. Fault (paper fault)
2. On-line switch (in OFF position)

Reset by manual correction of error condition if LPCS bit 6 is not set. If bit 6 is set, bit 15 is reset by manual correction of the error and: (1) reading the interrupt vector if the interface is "ready," or (2) after reading the LPCS if the interface is "not ready." Read-only.

Bit: 14-8 **Name:** Not used
Description: Read as 0s.

Bit: 7 **Name:** Done
Description: LP05—Asserted (1) whenever printer is ready for next character to be loaded. Indicates that previous function is either complete or has been started and continued to a point where the printer can accept the next command. This bit is set by the processor asserting BINIT L; if bit 6 is also set, an interrupt sequence is initiated. Also set by the printer when on-line and ready to accept a character. Cleared by loading (writing into) the LPDB register. Inhibited when bit 15 is set. Read-only.

LA180—Asserted (1) when the printer is ready to accept another character. Done is set by the processor asserting BINIT L and is cleared by loading (output transfer to) the LPDB register. If the Interrupt Enable bit is set, setting Done will initiate an interrupt request.

Bit: 6 **Name:** Interrupt Enable
Description: Set or cleared by the program. Also cleared by the processor asserting BINIT L. When set, an interrupt sequence is initiated if either the Error or Done bit is set.

Bit: 5-2 **Name:** Not used
Description: Read as 0s.

Bit: 1 **Name:** On Line
Description: Not supported and not required by DIGITAL software. The following information is provided for reference only.

LA180—Set when the LA180 is on-line. Read-only.

LP05—Not used. Read as 0.

Bit: 0 **Name:** Busy
Description: Not supported and not required by DIGITAL software. Information is provided for reference only.

LA180—Set when the LA180 is printing a line or advancing paper.

LP05—Not used. Read as 0.

Table 6 LPDB Register Bit Functions

Bit: 15-8 **Name:** Not used
Description: Read as 0s. Data written into these bits is lost.

Bit: 7 **Name:** Parity or D8
Description: Optional use. Read as 0. LA180—Optional parity bit. LP05—Optional paper instruction bit. Not supported by the LPV11. Read as 0.

Bit: 6-0 **Name:** Data
Description: 7-bit ASCII character register. Characters are sequentially output to the printer buffer via this register. Read as 0s.

Interrupts

Programs written for use with the LPV11 are generally composed of an interrupt-driven routine. When the LPCS register Interrupt Enable bit is set and either the Done or Error bit is set, an interrupt request is initiated. Entry to the LPV11 service routine is normally via the factory-configured vector addresses 200_8 (PC) and 202_8 (PS). When servicing an interrupt and a second interrupt occurs, the second (and subsequent) interrupt may not be recognized. This condition can be avoided by checking for both interrupt conditions (Done and Error) in the interrupt service routine.

REV11-A, -C

REV11-A TERMINATOR, REV11-C DMA REFRESH, BOOTSTRAP

GENERAL

The REV11-A DMA refresh, bootstrap/terminator module consists of DMA refresh circuits, a bootstrap ROM, and 120-ohm termination circuits. The REV11-C is similar to the REV11-A, but does not have the 120-ohm termination circuits.

FEATURES

- Dynamic MOS memory refresh
- ROM programs for booting paper tapes, RXV11 floppy disks, and RKV11 cartridge disks
- ROM diagnostics for CPU and memory
- 120-ohm LSI-11 bus terminations (REV11-A only)

SPECIFICATIONS

Identification	M9400-YA (REV11-A) M9400-YC (REV11-C)
Size	Double
Power	+5 V ±5% at 1.64 A (REV11-A) +5 V ±5% at 1.0 A (REV11-C)
Bus loads	
AC	2.2
DC	1

DESCRIPTION

Addressing – The module includes a 512 X 16-bit ROM array that is addressed in two 256-word segments. These address segments are reserved for REV11 options and reside in the upper 4K address bank, normally used for peripheral device addresses. The reserved addresses range from 165000–165776 and 173000–173776. A power-up mode, which will cause the processor to access ROM location 173000 upon power-up, is jumper-selectable on the processor module.

Initialization – The bootstrap ROM logic is initialized only when BDCOK H goes false. This condition occurs during a power failure and produces active BD INIT H and BD INIT L signals. These signals clear the 9-bit address latch and circuits contained in the DMA refresh logic. The option does not respond to the LSI-11 bus BINIT L signal.

Terminations (REV11-A Only)
Each bus signal line terminates with two resistors as shown in Figure 7. These termination resistors are generally contained in a 16-pin, dual-in-line package which is identical to an IC package. Each package contains 14 termination pairs. The values used are shown in the figure. Daisy-chained grant signals are terminated and jumpered. BIAKI L is jumpered (with etch) to BIAKO L, and BDMGI L is connected to BDMGO L via factory-installed jumper W1.

CONFIGURATION

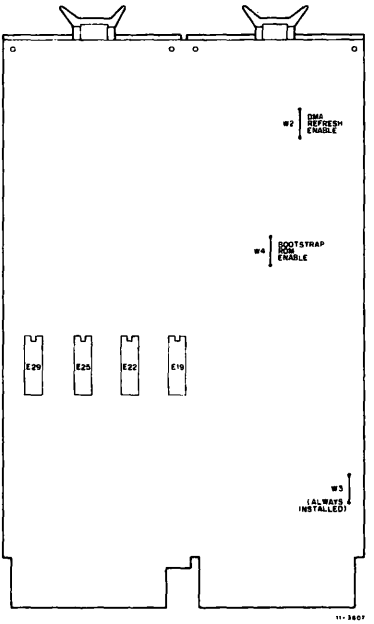


Figure 1 REV11-A, -C, Jumpers

W2 Insert to enable DMA refresh.
W4 Insert to enable bootstrap ROM.

PROGRAMMING

Using REV11-A and REV11-C Commands

General — The REV11 hardware option contains programs stored in read-only memory. The normal starting address for the program is 173000. When started at this location, the program executed is a non-memory modifying processor test. If no errors are detected, the program outputs a dollar-sign ($) for display on the console device. This character is the prompt character for the operator to enter a command.

The starting address can be entered and program operation started either manually, using the console ODT GO command, or automatically during power-up. Automatic operation is accomplished by selecting power-up mode 2 by appropriately configuring jumpers on the processor module. The normal power-up response for this mode results in the console device displaying the $ prompt character instead of the @ console ODT prompt character.

Unsuccessful execution of the non-memory modifying processor test program results in the $ prompt character not being displayed. Instead, the program hangs (branch to self) when a sequence of instructions does not execute properly, or the processor halts due to a double bus error. A halt normally results in the console terminal displaying the PC contents (the address of the halt +2) followed by the console ODT prompt character.

REV11-A and REV11-C Command Set — Once the $ prompt character is displayed, the operator can enter one of the commands described in Table 1. Note that in the command examples, characters printed by the program are shown underlined; characters not underlined are entered by the operator. Command inputs to the program can be either be upper- or lower-case characters. If an invalid command is entered following the $ prompt character, the program responds by displaying ? after the invalid command and a new $ prompt character on a new line. For example, program response to the invalid "XJ" command is shown below:

```
$XJ?
$
```

NOTE

The <CR> function in Table 1 represents the non-printable character "carriage return," which is recognized as an execute command.

Table 1 REV11 ROM Program Commands

Command: OD
Function: ODT (Halt). This allows the operator to examine and/or alter memory and register locations via the console device. Control can be returned to the REV11 program by entering the ODT P (proceed) command, if the PC has not been altered, and the console device will display the $ prompt character. If the PC has been altered, the operator can start program execution by entering the starting address 165006 and the G (go) command as follows:

@ 165006G
$

The processor responds by displaying the $ prompt character on a new line and another REV11 command can be entered.

Command: XM<CR>
Function: Memory diagnostic program. After successfully completing the diagnostic, the prompt character ($) is displayed on the console device. Errors are indicated by the following displays on the console device:

1. 173732
   @
   This is an address test error. The expected (normal) data is in R3 and the invalid data is in the memory location pointed to by R2. If desired, continue diagnostic program execution by entering the ODT P command.
2. 173756
   @
   This is a data test error. The expected (normal) data is stored in R3 and the invalid data is in the memory location pointed to by R2. If desired, continue diagnostic program execution by entering the ODT P command.
3. 000010
   @
   A time-out trap has occurred in testing memory locations outside the first (lowest) 4K memory.
4. nnnnnn
   @
   A time-out trap has occurred in testing memory locations within the first 4K memory. The nnnnnn displayed is an indeterminate number.

The actual test consists of an address test and a data test. The address test first writes all memory locations with addresses; it then reads and verifies the addresses. The data test consists of two parts. An "all 1s" word is first walked through all memory locations, which are initially 0. The second part consists of walking an "all 0s" word through all memory locations which are all 1s.

Command: XC<CR>
Function: Processor diagnostic program. This is a memory-modifying instruction test. Successful execution of the diagnostic program results in the prompt character ($) being displayed on the console device. Errors are indicated by:

1. The program halting when an instruction sequence is not correctly executed.
2. The program halting in the trap vector area for various traps.

Command: AL<CR>
Function: Absolute loader program, normal (absolute address) loading operation. Entering AL<CR> specifies that a paper tape is to be loaded via the console device (CSR address = 177560). However, another device can be specified by entering the appropriate CSR address. For example, to load paper tapes in absolute loader format via a device whose CSR address is 177550, enter the following command:

$AL177550<CR>

The program responds by first executing the memory-modifying CPU instruction test and memory test (refer to the XC and XM commands). Successful test execution results in the execution of the absolute loader program.

A successful program load is indicated by the loaded program automatically starting execution or by the console device displaying:

165626
@

Absolute loader errors are:

- Checksum error, with the program halting and producing the display:

165534
@

- Program halts in the trap vector area for traps other than a time-out trap
- Time-out trap occurs, causing the display of $ on a new line on the console device

This program can be restarted without first executing the diagnostic programs by the following:

1. Load R4 with 165414 (AL starting address).
2. Load the highest available memory address into R5. (For example, if the system contains 4K of read/write memory, load R5 with 17776.)
3. Start the program at 165242.

Command: AR<CR>
Function: Absolute loader program; relocated loading operation. When this command is entered, the memory-modifying CPU instruction test and memory test are automatically executed first (refer to the XC and XM commands), followed by the absolute loader program. Successful execution of the tests results in the program halting with the following console display:

```
165412
@
```

The operator must then enter the appropriate "software switch register" contents in R4. To select relocated loading, which uses an address (bias) contained in the software switch register, enter the following commands:

```
@ R4/xxxxxx nnnnnn<CR>
@ P
```

The value nnnnnn is a relocation value selected by the operator. Observe that the least significant "n" value entered must be an odd number. This sets the software switch register (R4) bit 0 to a logical 1, selecting the relocated loading mode. Note that the program being loaded must be in position-independent code (PIC) format for relocated loading.

When large programs are contained on more than one tape, the program halts at the end of the tape. Install the second tape in the reader, and enter a "1" in R4 using the ODT command shown below. Resume loading by entering the P command.

```
@ R4/xxxxxx 1 <CR>
@ P
```

The six octal digits (xxxxxx) are the present contents of R4. Entering a value of 1 selects relocated loading for the next program tape starting at the address following the end of the previous load operation. The P command allows the absolute loader program execution to continue the loading process once the software switch register value has been entered.

A successful program load is indicated by the loaded program automatically starting execution, or by the console device displaying:

165626
@

Absolute loader errors are the same as for the AL command.

This program can be restarted without first executing the diagnostic programs by the following:

1. Load R4 with 165406 (AR starting address).
2. Load the highest available memory address in R5. (For example, if the system contains 4K of read/write memory, load R5 with 17776.)
3. Start the program at 165242.

Command: DX<CR> or DXn<CR>
Function: RXV11 floppy disk system bootstrap. Entering the DX<CR> command starts the memory-modifying CPU instruction test and memory test execution. (See the XC and XM commands.) Successful test execution results in the execution of the bootstrap program for disk drive 0, the system disk. Or, specify the drive number (n) as 0 (drive 0) or 1 (drive 1). Floppy disk bootstrap errors are:

1. The program halts and the console device displays:

   165316
   @

   indicating that the device done flag in the RXV11 interface was not set within the required time (approximately 1.3 seconds). The bootstrap can be restarted by entering the P command; the $ is then displayed on the console device and the bootstrap command can be entered.
2. The program halts and the console displays:

   165644
   @

indicating that a bootstrap error occurred. The RXV11 error register contents are stored in R2. By examining the contents of R2 and using the information in this handbook on the RXV11, the exact nature of the error can be determined. Examine the contents of R2 (nnnnnn) as follows:

@ R2/nnnnnn<CR>
@P
$

After examining R2, the bootstrap can be restarted by the P command; enter the desired bootstrap command immediately after the $ prompt character.

3. The program halts in the trap vector for traps; a time-out trap returns the program to the $ prompt character. If a time-out trap occurs first, check for proper system cable connections and device interface module installations. Then, attempt to successfully bootstrap the system by again entering the desired command.

The bootstrap for disk drive 0 (DX) can be started without first executing the diagnostic programs by the following.

1. Load R4 with 165264 (the DX bootstrap starting address).
2. Start the program at 165242.

Command: DK<CR> or DKn<CR>
Function: RKV11-D disk drive system bootstrap. Entering the DK command starts the memory-modifying CPU instruction test and memory test execution. (See the XC and XM commands.) Successful test execution results in execution of the bootstrap program for disk drive 0, the sytem disk. Or, specify the drive number n as 0 (drive 0), 1 (drive 1), or 2 (drive 2).

Disk bootstrap errors are:

1. The program halts and the console device displays:

165724
@

indicating that the device done flag in the RKV11-D interface was not set within the required time (approximately 1.3 seconds). The bootstrap can be started by entering the P command; the $ is then displayed on the terminal and the bootstrap command can be entered.

2. The program halts and the console displays:

   165644
   @

   indicating that a bootstrap error occurred. The RKV11-D error register contents are stored in R2. By examining the contents of R2 and using the information contained in the RKV11-D option description, the nature of the error can be determined. Examine the contents of R2 (nnnnnn) as follows:

   @R2/nnnn<CR>
   @P
   $

   After examining R2, the bootstrap can be restarted by the P command; enter the desired bootstrap command immediately after the $ prompt character.

3. The program halts in the trap vector for traps; a time-out trap returns the program to the $ prompt character. If a time-out trap occurs first, check for proper system cable connections and device interface module installation. Then, attempt to successfully bootstrap the system by again entering the desired bootstrap command.

RKV11-D RK05 DISK DRIVE CONTROLLER

SPECIFICATIONS

LSI-11 Bus Module

Identification	M7269
Size	Double
Power	+5 V ±5% at 1.8 A
Bus Loads	
AC	1.9
DC	1

RKV11-D Controller

Input Voltage	
RKV11-DA	100-127 Vac, 50/60 Hz ±1 Hz
RKV11-DB	200-254 Vac, 50/60 Hz ±1 Hz
Input Power	140 W max
Power Supply	H780
Line Protection	
115 Vac	5 A fast blow fuse
230 Vac	2.5 A fast blow fuse
LSI-11 bus backplane signal from RKV11-D power supply	BPOKH (power supply AC LO) BDCOKH (Bus DC LO)
Module Complement	
M7254	Control/Status
M7255	Disk Control
M7256	Data Paths
M7268	Bus Adapter
M930	Drive Bus Terminator
M7269	Bus Control
Cables	Two 40-conductor flat 70-09026-02 (to first RK05 drive) Two 40-conductor flat BC05L (to LSI-11 bus interface)

CONFIGURATION

General

The RKV11-D/RK05 disk drive system can be configured with up to eight RK05-J disk drives daisy-chained on the drive bus (DR bus).

Each disk drive must have an M7700 module of revision J or later. The M7700 module has a rotary switch that defines the logical disk drive DR bus position. The first disk drive on the DR bus is normally set to switch position 1 on the M7700 module and is designated as disk drive 0. The second disk drive would then be designated as drive 1 (switch position 2), and so on, up to the eighth disk drive (switch position 8). This configuration (Figure 1) may be varied as DR bus length allows. The maximum length of the DR bus is 15 m (50 ft). The DR bus must be terminated with the M930 module at the last RK05 on the bus.

Module Jumpers

The M7269 module has jumpers to configure the interrupt vector and device register addresses. The M7256, M7255 and M7254 modules have jumpers to configure certain RK05 disk drive functions. The jumpers on the M7269 module have been factory-configured for an interrupt vector of 220_8 and device addresses of 177400_8 through 177416_8. These addresses are the normal user addresses and should not be altered. Figure 2 shows the jumper locations for the interrupt vector and device address jumpers on the M7269 module. The interrupt vector and device address word formats are shown in Figures 3 and 4 and described in Table 1.

Table 1 Standard Assignments

Description	Mnemonic	Read/ Write	M7269 Module Address
Registers			
Drive Status	RKDS	R	177400
Error	RKER	R	177402
Control/Status	RKCS	R/W	177404
Word Count	RKWC	R/W	177406
Bus Address/Current Memory Address	RKBA	R/W	177410
Disk Address	RKDA	R/W	177412
Unused			177414
Data Buffer	RKDB	R (PIO)	177416
Interrupt Vector			
Interrupt Vector	—	—	220

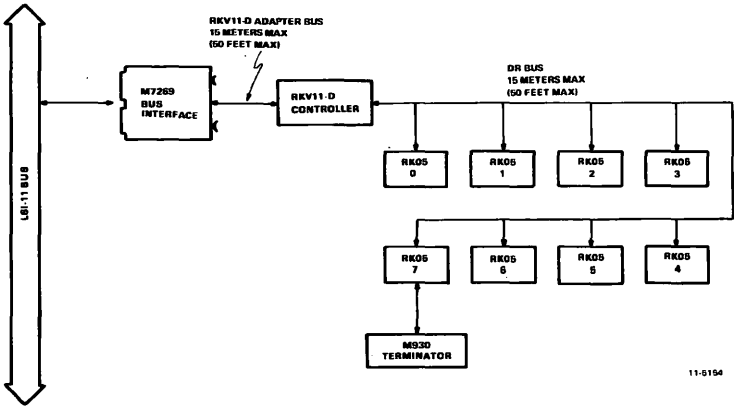


Figure 1 RKV11-D/RK05 System Configuration

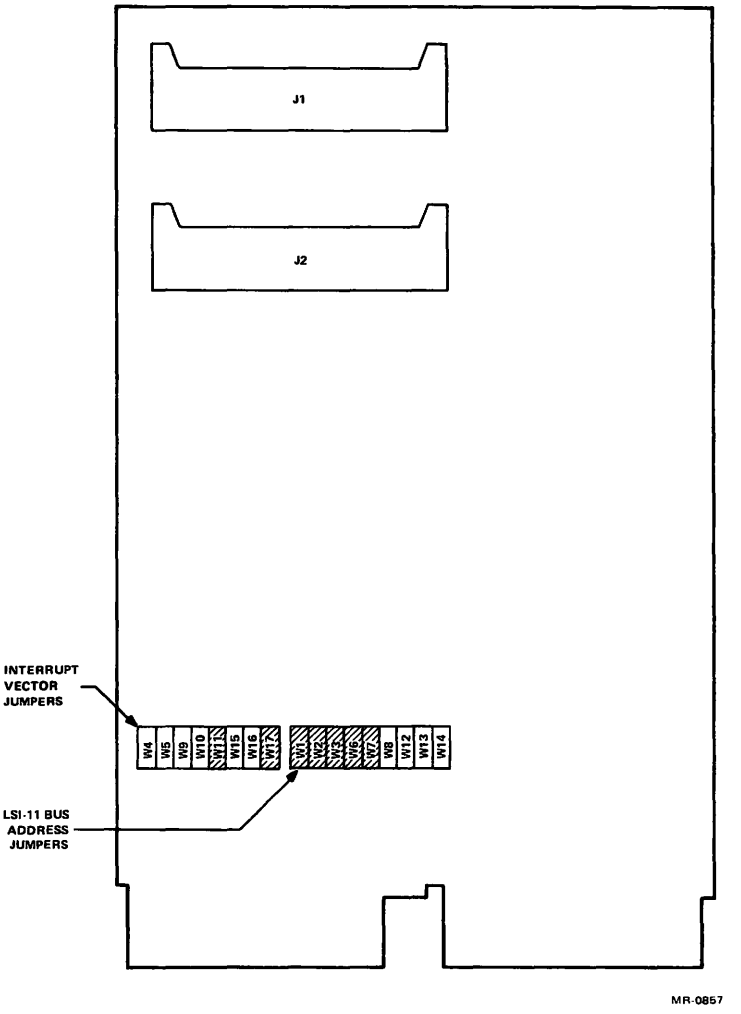


Figure 2 M7269 Module Jumpers

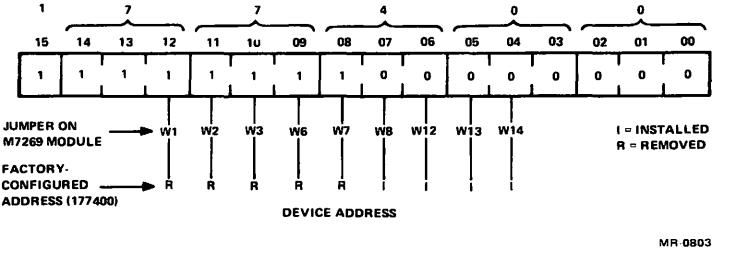


Figure 3 M7269 Device Address Format

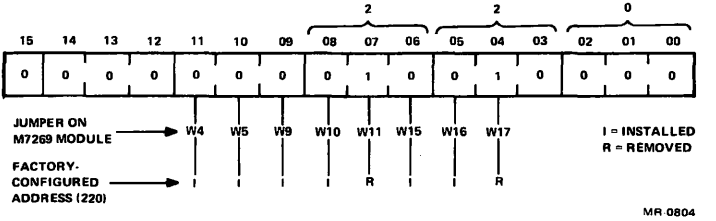


Figure 4 M7269 Interrupt Vector Format

Module Utilization

Of the six modules supplied with the RKV11-D, four are installed in the RKV11-D controller backplane as shown in Figure 5. The M930 terminator module is plugged into the last RK05 disk drive on the DR bus, and the M7269 double-height module is plugged into the LSI-11 bus. The RKV11-D is a DMA device. Priority of DMA devices on the LSI-11 bus is determined by the devices' electrical distance from the processor. The DMA device closest to the processor has the highest DMA priority.

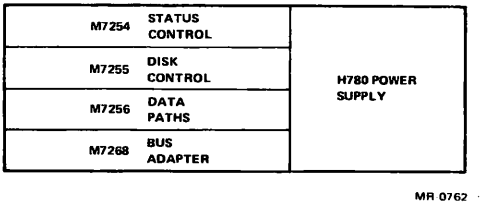


Figure 5 RKV11-D Module Utilization

Cabling

The RKV11-D is supplied with two BC05L cables which connect the M7269 LSI-11 bus control module to the M7268 bus adapter module. The BC05L cables are connected from J1 to J1 and from J2 to J2 on each module (Figures 2 and 6). Two 70-09026-02 cables are also supplied for connecting J3 and J4 on the M7268 module (Figure 6) to the RK05 M993-YA module.

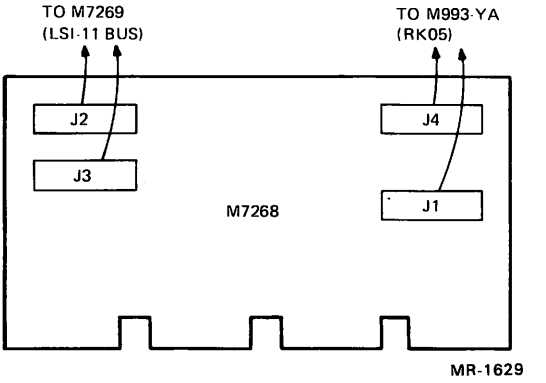


Figure 6 M7268 Cable Connections

Registers

The RKV11-D contains seven 16-bit programmable registers that provide software interface to the LSI-11 bus. These registers are addressable from the processor and are listed in Table 2. The formats for these registers are shown in Figures 7 through 13. Bit descriptions are in Tables 3 through 9.

Table 2 RKV11-D Addressable Registers

Register Name	Mnemonic	Address*
RKV11-D Drive Status Register	RKDS	177400
RKV11-D Error Register	RKER	177402
RKV11-D Control/Status Register	RKCS	177404
RKV11-D Word Count Register	RKWC	177406
RKV11-D Bus Address Register (Current Memory Address)	RKBA	177410
RKV11-D Disk Address Register	RKDA	177412
RKV11-D Data Buffer Register	RKDB	177416

* Address 177414 is unused.

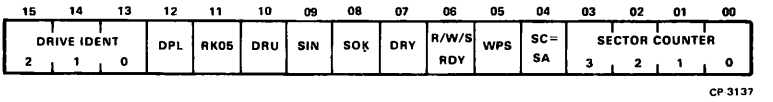


Figure 7 Drive Status Register (RKDS) Address 177400

NOTE

This register is a read-only register, and contains the selected drive status and current sector address.

Table 3 Drive Status Register Bit Descriptions

Bit: 0-3 **Name:** SC (Sector Counter)
Description: These four bits are the current sector address of the selected drive. Sector address 0 is defined as the sector following the sector that contains the index pulse.

Bit: 4 **Name:** SC=SA (Sector Counter equals Sector Address)
Description: Indicates that the disk heads are positioned over the disk address currently held in the sector address register.

Bit: 5 **Name:** WPS (Write Protect Status)
Description: Set when the selected disk is in the write-protected mode.

Bit: 6 **Name:** R/W/S RDY (Read/Write/Seek Ready)
Description: Indicates that the selected drive head mechanism is not in motion, and that the drive is ready to accept a new function.

Bit: 7 **Name:** DRY (Drive Ready)
Description: Indicates that the selected disk drive complies with the following conditions:

a. The drive is properly supplied with power.
b. The drive is loaded with a disk cartridge.
c. The disk drive door is closed.
d. The LOAD/RUN switch is set to RUN.
e. The disk is rotating at proper speed.
f. The heads are properly loaded.
g. The disk is not in a DRU (bit 10 of RKDS) condition.

Bit: 8 **Name:** SOK (Sector Counter OK)
Description: Indicates that the sector counter operating on the selected drive is not in the process of changing, and is ready for examination. If this bit is not set, the sector counter is not ready for examination, and a second attempt should be made.

Bit: 9 **Name:** SIN (Seek Incomplete)
Description: Indicates that because of some unusual condition, the seek function cannot be completed. Can be accompanied by RKER 15 (drive error). Cleared by a drive reset function.

Bit: 10 **Name:** DRU (Drive Unsafe)
Description: Indicates that an unusual condition has occurred in the disk drive, and it is unable to properly perform any operations. Reset by setting the RUN/LOAD switch to LOAD. If, when the switch is returned to RUN, the condition recurs, an inoperative drive can be assumed, and corrective maintenance procedures should begin. Can be accompanied by RKER 15 (drive error).

Bit: 11 **Name:** RK05 (RK05 Disk On Line)
Description: Always set to identify the selected disk drive as RK05.

Bit: 12 **Name:** DPL (Drive Power Low)
Description: Sets when an attempt is made to initiate a new function, or if a function is actively in process when the control senses a loss of power to one of the disk drives. Can be accompanied by RKER 15 (drive error). Reset by BUS INIT or a control reset function.

Bit: 13-15 **Name:** ID (Identification of Drive)
Description: If an interrupt occurs as the result of a hardware poll operation, these bits will contain the binary representation of the logical drive number that caused the interrupt.

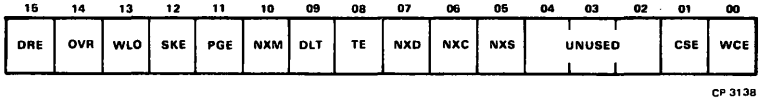


Figure 8 Error Register (RKER)—Address 177402

NOTE
This is a read-only register.

Table 4 Error Register Bit Descriptions

Bit: 0 **Name:** WCE (Write Check Error)
Description: Indicates that an error was encountered during a write-check function as a result of a faulty bit comparison between disk data and memory data. Clears upon the initiation of a new function. This is a soft error condition.

Bit: 1 **Name:** CSE (Checksum Error)
Description: Sets while performing a read function as a result of a faulty recalculation of the checksum. Cleared upon the initiation of any new function. This is a soft error condition.

Bit: 2-4 **Name:** Unused

NOTE
The remaining bits of the RKER are all hard errors, and are cleared only by BUS INIT or by a control reset function.

Bit: 5 **Name:** NXS (Nonexistent Sector)
Description: Indicates that an attempt was made to a sector address greater than 13_8.

Bit: 6 **Name:** NXC (Nonexistent Cylinder)
Description: Indicates that an attempt was made to initiate a transfer to a cylinder address greater than 312_8.

Bit: 7 **Name:** NXD (Nonexistent Disk)
Description: Indicates that an attempt was made to initiate a function on a nonexistent drive.

Bit: 8 **Name:** TE (Timing Error)
Description: Indicates that a loss of timing pulses for at least 5 μs has been detected.

Bit: 9 **Name:** DLT (Data Late)
Description: Sets during a write or write-check function when the multibuffer file is empty and the operation is not yet complete. Sets during a read function when the multibuffer file is filled and the operation is not yet complete.

Bit: 10 **Name:** NXM (Nonexistent Memory)
Description: Sets if memory does not respond with a RPLY within 20 μs of the time when the RKV11-D becomes bus master during a DMA sequence. Because of the speed of the RK05 disk drive, it is possible that NXM will be accompanied by RKER 9 (data late).

Bit: 11 **Name:** PGE (Programming Error)
Description: Indicates that the RKCS 10 (format) was set while initiating a function other than read or write.

Bit: 12 **Name:** SKE (Seek Error)
Description: Sets if the disk head mechanism is not properly positioned while executing a normal read, write, read-check, or write-check function. The control checks 16 times before flagging this error. A simple jumper change will force the control to check just once.

Bit: 13 **Name:** WLO (Write Lockout Violation)
Description: Sets if an attempt is made to write on a disk that is currently write-protected.

Bit: 14 **Name:** OVR (Overrun)
Description: Indicates that, during a read, write, read-check, or write-check function, operations on sector 13_8, surface 1 of cylinder address 312_8, were finished and the RKWC has not yet overflowed. This is essentially an attempt to overflow out of a disk drive.

Bit: 15 **Name:** DRE (Drive Error)
Description: Sets if a function is either initiated or in process, and:

a. One of the drives in the system senses a loss of either ac or dc power, or

b. The selected drive is not ready or is in some error condition.

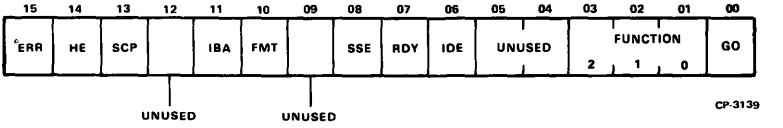


Figure 9 Control/Status Register (RKCS)—Address 177404

Table 5 Control/Status Register Bit Descriptions

Bit: 0 **Name:** GO
Description: This write-only bit can be loaded by the operator and causes the control to carry out the function contained in bits 1-3 of the RKCS (functions). Remains set until the control actually begins to respond to GO, which may take from 1 μs to 3.3 ms, depending on the current operation of the selected disk drive (to protect the format structure of the sector).

Bit: 1-3 **Name:** Function
Description: The function register, or function read/write bits, are loaded with the binary representation of the function to be performed by the control when a GO command is initiated. These bits are loaded by the program and cleared by BUS INIT. The binary codings are as follows:

	Bit		
3	**2**	**1**	**Operation**
0	0	0	Control reset
0	0	1	Write
0	1	0	Read
0	1	1	Write check
1	0	0	Seek
1	0	1	Read check
1	1	0	Drive reset
1	1	1	Write lock

Bit: 4,5 **Name:** Unused

NOTE

The RKV11-D uses these bits. Since the LSI-11 bus structure has no provision for extended addressing, no connection is made to the bus from these bits on the RKV11-D. They will respond as two unused read/write bits in the status register, but like the RKV11-D, they will increment should the RKBA overflow.

Bit: 6 **Name:** IDE (Interrupt on Done Enable)
Description: When set, this read/write bit causes the control to issue a bus request and interrupt to vector address 220_8 if:

a. A function has completed activity.
b. A hard error is encountered.
c. A soft error is encountered and bit 8 of the RKCS (SSE) is set.
d. RKCS 7 (RDY) is set and GO is not set.

Bit: 7 **Name:** RDY (Control Ready)
Description: This read-only bit indicates that the control is ready to perform a function. Set by INIT, a hard error condition, or by the termination of a function. Cleared by GO being set.

Bit: 8 **Name:** SSE (Stop on Soft Error)
Description: If a soft error is encountered when this read/write bit is set:

a. all control action will stop at the end of the current sector if RKCS 6 (IDE) is reset, or
b. all control action will stop and a bus request will occur at the end of the current sector if RKCS 6 (IDE) is set.

Bit: 9 **Name:** Unused

Bit: 10 **Name:** FMT (Format)
Description: This read/write bit is under program control, and must be used only in conjunction with normal read and write functions. Used to format a new disk pack or to reformat any sector erased because of control or drive failure. Alters the normal write operation under which the header is rewritten each time the associated sector is rewritten; the head position is not checked for proper positioning be-

fore the write. Alters the normal read operation in that only one word, the header word, is transferred to memory per sector. For example, a 3-word read function in format mode will transfer header words from three consecutive sectors to three consecutive memory locations for software checking.

Bit: 11 **Name:** IBA (Inhibit Incrementing the RKBA)
Description: This read/write bit inhibits the RKBA from incrementing during a normal tranfer function. This allows data transfers to occur to or from the same memory location throughout the entire transfer operation.

Bit: 12 **Name:** Unused

Bit: 13 **Name:** SCP (Search Complete)
Description: This read-only bit indicates that the previous interrupt was the result of some previous seek or drive reset function. Cleared at the initiation of any new function.

Bit: 14 **Name:** HE (Hard Error)
Description: This read-only bit sets when any of RKER 5-15 are set. Stops all control action, and processor reaction is dictated by RKCS 6 (IDE), until cleared, along with RKER 5-15, by INIT or by a control reset function.

Bit: 15 **Name:** ERR (Error)
Description: This read-only bit sets when any bit of the RKER sets. Processor reaction is dictated by RDCS 6 and RKCS 8 (IDE and SSE). Cleared if all bits in the RKER are cleared.

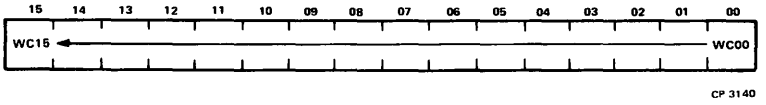


Figure 10 Word Count Register (RKWC)—Address 177406

Table 6 Word Count Register Bit Descriptions

Bit: 0-15 **Name:** WC00-WC15
Description: The bits in this register contain the 2's complement of words to be affected or transferred by a given function. The register increments by one after each word transfer. When the register overflows (all WC bits go to zero), the transfer is complete and RKV11-D operation is terminated at the end of the present disk sector. However, only the number of words specified in the RKWC are transferred.

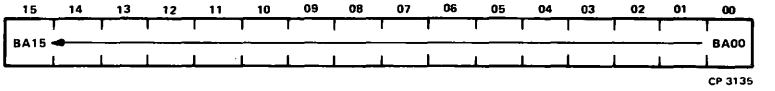


Figure 11 Bus Address Register(RKBA)—Address 177410

Table 7 Bus Address Register Bit Descriptions

Bit: 0-15 **Name:** BA00-BA15
Description: The read/write bits in this register contain the bus address to or from which data will be transferred. The register is incremented by two at the end of each transfer.

NOTE

This register will not respond to commands while the controller is busy. Therefore, RKDA bits are loaded from the bus data lines only in the control ready (bit 7 of the RKCS) state, and are cleared by BUS INIT and control reset. The RKDA is incremented automatically at the end of each disk sector.

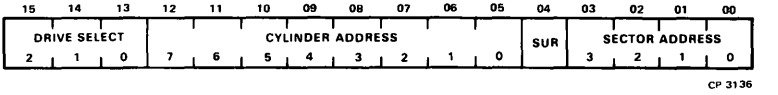


Figure 12 Disk Address Register (RKDA)—Address 177412

Table 8 Disk Address Register Bit Descriptions

Bit: 0-3 **Name:** SA (Sector Address)
Description: Binary representation of the disk sector to be addressed for the next function. The largest valid address (or number) for the sector address is 13_8.

Bit: 4 **Name:** SUR (Surface)
Description: When active, enables the lower disk head so that operation is performed on the lower surface; when inactive, enables the upper disk head.

Bit: 5-12 **Name:** CYL ADDR (Cylinder Address)
Description: Binary representation of the cylinder address currently being selected. The largest valid address or number for the cylinder address is 312_8.

Bit: 13-15 **Name:** DR SEL (Drive Select)
Description: Binary representation of the logical drive number currently being selected.

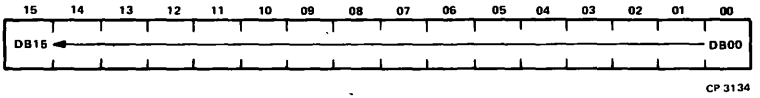


Figure 13 Data Buffer Register (RKDB)—Address 177416

Table 9 Data Buffer Register Bit Descriptions

Bit: 0-15 **Name:** BD00-BD15
Description: The read-only bits of this register work as a general data handler in that all information transferred between the control and the disk drive must pass through this register. Loaded from the bus only while the RKV11-D is bus master during a DMA sequence.

PROGRAMMING

RKV11 Boot Program

The following boot program can be used to boot an RKV11/RK05 system from drive unit 0.

```
@1000/000000                    12700<LF>
001002      000000              177406<LF>
001004      000000              12710<LF>
001006      000000              177400<LF>
001010      000000              12740<LF>
001012      000000              5<LF>
001014      000000              105710<LF>
001016      000000              100376<LF>
001020      000000              5007<CR>
@1000G
```

RLV11

RLV11 RL01 DISK DRIVE CONTROLLER

GENERAL

The RLV11 option is designed to interface RL01 disk drives with the LSI-11 bus. The RLV11 controller can be used only in an H9273-A type backplane (PDP-11/03L or BA11-NE), which incorporates the LSI-11 bus in slot AB and an interboard bus in slot CD. The 2-card controller can interface up to four RL01 disk drives for a complete system. The RLV11 option consists of two quad-size boards, an RL01 disk drive, and all the necessary cables.

The RL01 disk drive is a random access, mass storage system that stores data in fixed-length blocks on a preformatted disk cartridge. Each drive can store 5.24 million bytes and a complete system can store up to 21 million bytes. The RLV11 transfers data to and from the LSI-11 bus using direct memory access (DMA) techniques. This allows data transfers to occur without any processor interruptions and at the bus bandwidth speed.

FEATURES

- 5.24 million bytes per RL01 disk drive; 21 million bytes per system
- 10.48 million bytes per RL02 disk drive; 42 million bytes per system
- Up to four RL01 or RL02 disk drives or a combination can be used with one RLV11 controller
- Universal power supply, 110/220 V, 50/60 Hz
- Bootstrap provided on BDV11
- Mounts in a PDP-11/03-L system, BA11-N expansion box, or H9273-A backplane
- DMA transfers to and from the LSI-11 bus at 256K words per second
- 256 word silo buffer that eliminates late data errors on normal reads and writes

SPECIFICATIONS

LSI-11 Bus Modules

Identification	M8013 M8014
Size	Two quads
Power	+5 Vdc ±5% at 6.5 A +12 Vdc ±3% at 1 A
Bus Loads	
AC	3.2
DC	1

RLV11

RL01 Disk Drive

Data Organization	256 bytes per sector 40 sectors per track 256 tracks per surface 256 cylinders per cartridge 2 surfaces per cartridge
Formatted Capacity	10,240 bytes per track 20,480 bytes per cylinder 5.24M bytes per cartridge 21M bytes per controller
Recording Density	125 tracks/in. 3725 bits/in (max.)
Recording Method	MFM
Performance	
Peak Transfer Rate	3.9 μs per word 512.5K bytes per second
Head Positioning Time	15 ms track-to-track 55 ms average 100 ms maximum
Rotational Latency	12.5 ms average
Operating Environment	
Temperature Range	10° to 40° C (50° to 104° F) at sea level
Relative Humidity No Condensation	10 to 90%
Max. Wet Bulb	28° C (82° F)
Altitude	Up to 240 m (8000 ft.) at max. temperature of 36° C (96° F)
Heat Dissipation	150 W (600 Btu/hr.)
Operation	
Start Time	50 seconds
Stop Time	30 seconds
Rotational Speed	2400 rev/min.
Power	
Drive	Single-phase
Start Current	5 A/1.6 A max., 110V, 50/60 Hz
Running Current	2.5 A/0.85 A max., 230V, 50/60 Hz

RLV11

Mechanical Drive	
Size	48 cm wide × 63.4 cm deep × 27 cm high (19. in wide × 25 in. deep × 10.5 in. high)
Weight	33.75 kg (75 lb.)
Mounting	RETMA standard 48.26 cm (19 in.) rack-mounted on slides (provided). Recommended maximum height from floor is 18.9 cm (48 in.).
	Stand-alone cabinets for expansion (standard option) available.
Cartridge	2 data surfaces Embedded servo Top loading
Cable Lengths	
Standard	
Power	3.05 m (10 ft.)
Controller to Drive	3.05 m (10 ft.)
Drive to Drive	3.05 m (10 ft.)
Optional	
Drive Cables	6.96, 12.19, 18.29, m (20, 40, 60 ft.)

NOTE

Maximum physical length from controller to last drive should be 30.48 m (100 ft.).

DESCRIPTION

General

The RLV11 controller was designed to interface the RL01 disk drives to the LSI-11 bus. One RLV11 controller can support up to four RL01 disk drives. The controller consists of two quad-height modules that plug directly into an LSI-11 backplane assembly. The backplane should be structured as an H9273 (slots AB are LSI-11 bus and slots CD are an interboard bus. Refer to section H9273.)

RLV11

The M8014 module contains all the LSI-11 bus-related circuits. Items such as the bus control circuits, bus transceivers and decoders, programmable registers, and the FIFO circuits are located on this module. The bus control function consists of the register protocol, interrupt control, operation incomplete timer, direct memory access, and nonexistent memory timer. The bus transceiver circuits transmit and receive both data and address information on the bus. The programmable registers consist of the control/status register, bus address word counter, disk address register, and the multipurpose register. The FIFO circuits are a first-in/first-out memory that can store up to 256 16-bit data words.

The M8013 module contains all the controller timing and sequence logic and the data formatting circuits necessary to read and write on the disk. The microsequencer logic decodes the function command and proceeds to the address of the routine associated with the command. The write precompensation logic encodes the data into modified frequency modulation and precompensates the data for peak shifting effects. The cyclic redundancy checker is used to detect errors and compute CRC on a write operation. The data source selector allows the multiplexing of the data under control of the microsequencer. The header compare circuits compare the first header word received from the data separator with the serial disk address word coming from the disk address register.

The major functional sections of the RLV11 controller are shown in Figure 1. The processor controls the RL01 disk drives indirectly by means of the RLV11 controller. The controller has four registers: the bus address register (BAR), disk address register (DAR), control/status register (CSR), and a multipurpose register (MPR). Of these four registers, the CSR is always written last because it initiates the microsequencer operation. These registers can be addressed like any other memory location.

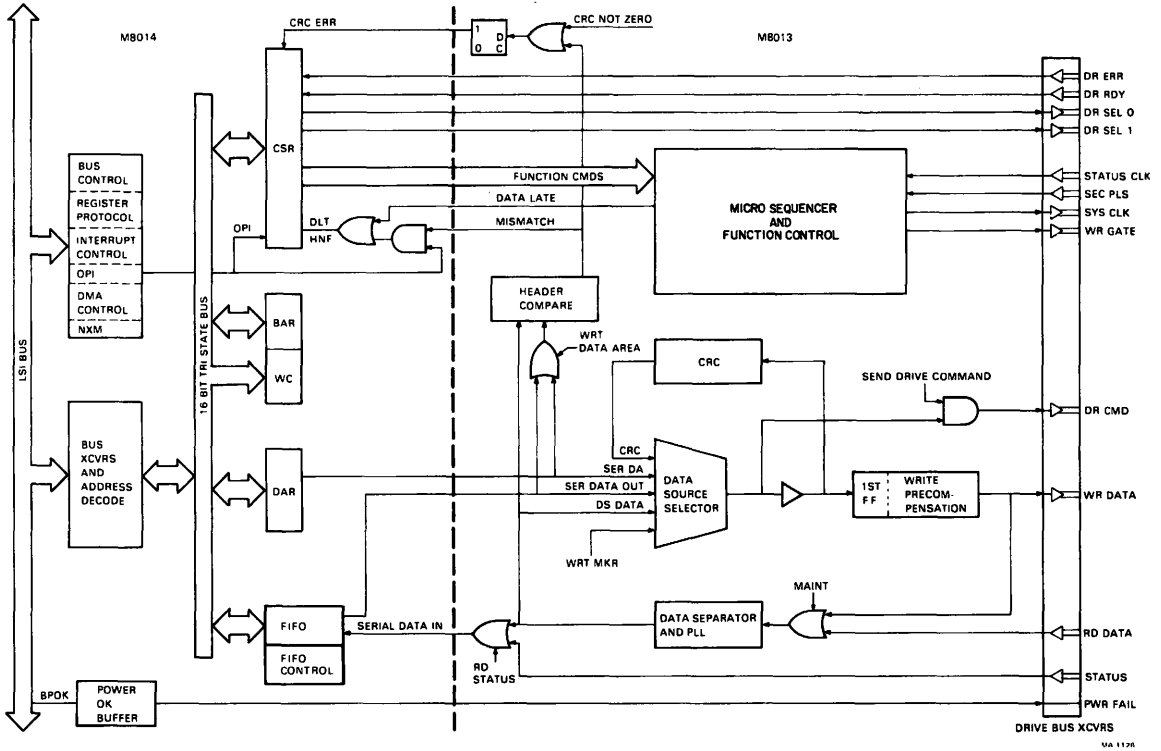


Figure 1 RLV11 Controller Simplified Block Diagram

To issue a function command, the processor places the address and data onto the LSI-11 bus in a multiplexed fashion. The RLV11 controller decodes the information and channels it to the appropriate register. Once the desired function command is written into the control/status register, it begins the microsequencer routine. The control microsequencer goes through a different routine for each of the eight possible command functions. These routines manipulate the data formatting circuits to format the data properly. Included in the data formatting function is an error detection feature that uses cyclic redundancy checking (CRC).

The data buffer (silo) is a data storage element used primarily when reading or writing the RL01K disk under DMA control. It is a FIFO memory that can store up to 256 words of data. The data buffer also performs data conversion functions. It converts parallel data coming off the LSI-11 bus into the serial form that can be written onto the disk. When performing a read operation, it reverses the direction of data flow and converts the serial disk data back into its parallel form.

Bus Control Functions

The bus control block consists of five separate functional units.

- Register Protocol Circuit—This circuit selects the controller register to be read or written and supplies the required control signals for loading and reading.
- Interrupt Control Circuit—This circuit sends out a bus interrupt request to the processor when the controller has completed a command operation and the interrupt enable bit is set. It also passes or blocks the processor interrupt acknowledge along the priority daisy chain and produces control signals for the generation of RPLY and vector data.
- OPI Circuit—This circuit is the operation incomplete (OPI) timer. This timer is initiated upon issuing a controller command. If the command sequence is not completed within the 490 msec nominal OPI time-out period, an OPI error bit is set in the control/status register. The controller ready bit is also set and the processor receives an interrupt request if enabled.
- DMA Control Circuit—The direct memory access (DMA) circuit coordinates the timing of the controller FIFO during DMA data exchanges with memory.
- NXM Circuit—The nonexistent memory (NXM) circuit is a timer used when the controller is attempting to read or write from memory. It is initialized by the bus SYNC signal and gives the memory device 10

μsec to reply to a controller data in (DIN) or data out (DOUT) signal. If the reply (BRPLY) is not received within 10 μsec, the NXM error bit is set in the CSR. NXM time-out can also occur because of a failure at the controller or drive.

Bus Tranceivers

These circuits transmit and receive both data and address information on the bus. The address decoder circuit compares each incoming address with the controller's preset base address. When a match is found, the register protocol circuit is enabled.

Programmable Registers

Control/Status Register (CSR) — The CSR is a holding register for command control information such as drive select, function to be performed, interrupt enable, and extended address bits. It also indicates drive ready and error conditions.

Bus Address Register (BAR) — The BAR contains the 16-bit memory address to which the next DMA transfer is to be made. It is incremented by 2 under control of the DMA control circuit at the end of each DMA transfer.

Disk Address Register (DAR) — The DAR contains the next sector address where data is to be read or written on the disk. It is incremented by 1 at the end of each sector read or written. The DAR is used also to store drive command information that is sent to the drive during a seek or get status operation.

Multipurpose Register (MPR) — The MPR is not a single physical entity like the other registers. It consists of two separate registers, the word counter and the FIFO output buffer, both bearing the same base address.

When writing the MPR, the data word is loaded into the word counter (WC) register. The WC register contains the number of data words remaining to be transferred under DMA control. The WC register is incremented by 1 under control of the DMA control circuit at the end of each DMA transfer.

When reading the MPR, the data word is read from the FIFO output buffer. After a read header command, it contains the header words. After a get status, it contains the disk drive status.

FIFO

The FIFO is a first-in/first-out silo-type memory element that can store up to 256 data words. When full, it holds two sectors of data. A FIFO

serializer circuit converts the FIFO parallel data into the serial form needed for writing to the disk. Similarly, the serial data read from the disk is converted to parallel form through the same serializer circuit.

The FIFO contents can be recovered by reading the current data word in the MPR. For example, to recover three FIFO words requires three successive readings of the MPR. During disk read and write operations, the FIFO is emptied and filled under control of the DMA logic.

Microsequencer Logic

The microsequencer first decodes the function command by using three funcion bits to point to an address in the sequencer ROM. There it finds a routine that corresponds to the command issued. It then proceeds to generate the timing and control signals needed to channel the incoming or outgoing data through all its various paths within the controller.

Write Precompensation

This circuit performs two major functions. It encodes digital data into its MFM form, and it precompensates this data for peak shifting effects.

MFM encoding is a magnetic recording technique used by the RL01 drive. A flux reversal is written on the disk in the center of a bit cell to represent a logical 1. To represent two successive logical 0s, a flux reversal is written at this common cell boundary. This recording technique guarantees at least one flux reversal for every two cell bits.

One of the problems associated with magnetic recording is a phenomenon called peak shift. Adjacent flux reversals on a track appear to be displaced from where they were written. To offset peak shift, the precompensation logic is used to displace the encoded data pulses in the opposite direction as the expected peak shift before they are written.

Data Separator

The data separator circuit makes use of a phase-locked loop oscillator to detect and decode incoming MFM disk data into its digital logical representation. It also generates the timing signals used by the microsequencer to control the read data operations.

CRC Circuit

The cyclic reduncancy checker (CRC) is an error-detection circuit. For any data written on the disk, a code is generated in the CRC circuit by

an internal algorithm. The code is then appended onto the end of each header sector in the form of a CRC word. When this header or sector is read from the disk, the data is channeled through the CRC circuit. Any errors introduced into the data or its CRC word are detected and a CRC error bit is set in the CSR.

Data Source Selector

This circuit allows the multiplexing of different data sources under the control of the microsequencer. There are five different sources of data: CRC data, serial disk address data, serial FIFO output data, data separator (DS) data, and the write marker pulse.

Header Compare Circuit

The function of the header compare circuit is to compare the first header word coming from the data separator with the serial disk address word coming from the DAR. This compare is done serially on a bit-by-bit basis. If any pair of bits is not identical, a mismatch signal is generated. At the end of a compare, the result is available to the microsequencer.

CONFIGURATION

General

All software control of the RLV11 controller is performed by means of four device registers. These registers are assigned addresses and can be read or written (as required) under software control. DIGITAL software requires that the device addresses are within the range of 160000 to 177777. This device address is preset at the factory to 174400. The address can be changed by setting the rocker switches designated "bus address switches" in Figure 2. These switches are used to assign a specific address to the control/status register (CSR) and the remaining registers will be assigned the next three addresses as shown in Table 1. A logical 1 is represented when the switch is placed on the ON position. Figure 3 shows the switch positions for the factory set address. The M8014 module must be located immediately after the M8013 module on the LSI-11 bus priority chain.

RLV11

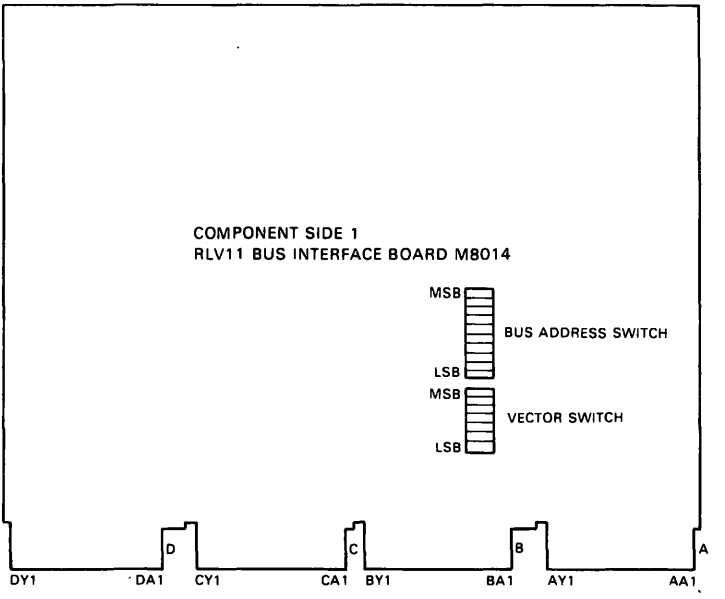


Figure 2 RLV11 Bus Interface Module (M8014)

Table 1 Standard Assignments

Description	Mnemonic	Read/ Write	Address
Registers			
Control/Status	CSR	R/W	174400
Bus Address	BAR	R/W	174402
Disk Address	DAR	R/W	174404
Multipurpose	MPR	R/W	174406
Interrupts			
Interrupt Vector			160

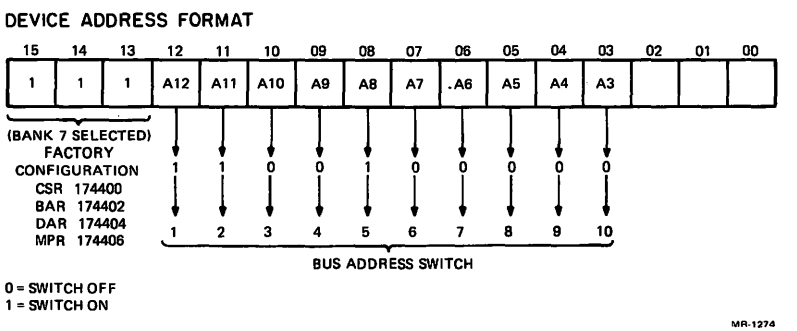


Figure 3 RLV11 Device Address Format

The interrupt vectors are allocated memory locations from 0-774. The recommended interrupt vector for the RLV11 is 160 and is preset at the factory for this vector. The user may set the rocker switches designated "vector switches" in Figure 2 for any vector within the allocation. A logical 1 is presented when the switch is placed to the ON position. Figure 4 shows the switch positions for the factory set address.

Jumpers

There are four jumpers (W1 to W4) installed on the M8013 printed circuit board as shown in Figure 5. These jumpers are installed in the factory and are used as described in Table 2.

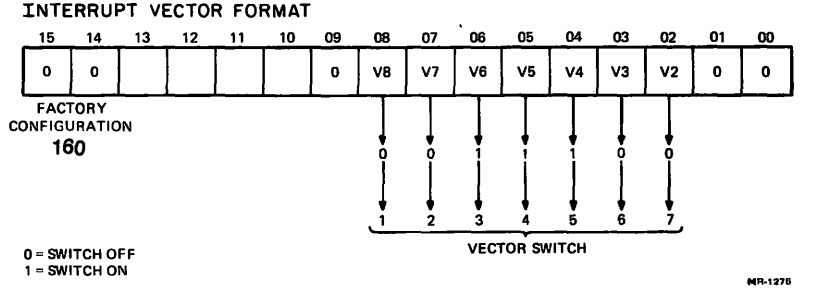


Figure 4 RLV11 Interrupt Vector Format

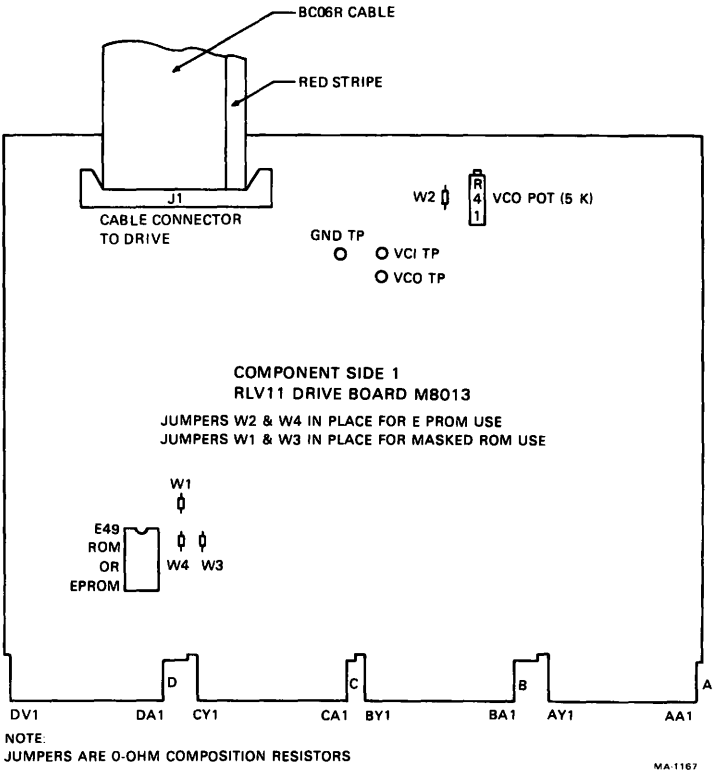


Figure 5 RLV11 Drive Module (M8013)

Table 2 M8013 Jumpers

Jumper	Definition
W1	Used with masked ROMs
W2	Used with EPROMs
W3	Used with masked ROMs
W4	Used with EPROMs

Masked ROMs W1, W3 — These jumpers are installed when using masked ROMs in E49. Jumpers W2 and W4 are removed.

EPROMs W2, W4 — These jumpers are installed when using EPROMs in E49. Jumpers W1 and W3 are removed.

Registers

Control/Status Register (CSR) — The control/status register (Figure 6) is a 16-bit, word-addressable register with a standard address of 174400. Bits 1 through 9 can be read or written; the other bits can only be read. The bit functions are described in Table 3.

When the LSI-11 bus is initialized (BINIT L), bits 1-6 and 8-13 are cleared, and bit 7 is set. Bit 0 is set whenever the selected drive is in the ready condition; otherwise the bit is cleared. Bit 14 is cleared as long as there is no drive error; otherwise the bit is set and remains set until the drive error is corrected or the drive error is cleared by a get status command with drive reset (bit 3) set. Bit 15 is set only when there is a drive or controller error (bits 10-14).

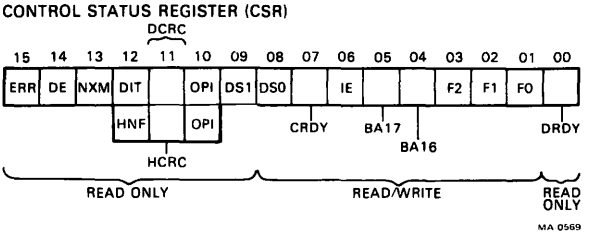


Figure 6 Control/Status Register

Table 3 CSR Word Format

Bit: 0 **Name:** DRDY
Description: (Drive Ready)
When set, this bit indicates that the selected drive is ready to receive a command or supply valid read data. The bit is cleared when a seek operation is initiated and set when the seek operation is completed.

Bit: 1-3 **Name:** F2-F0
Description: (Function Code)
These bits are set by software to indicate the command to be executed.

F2	F1	F0	Command	Octal Code
0	0	0	Maintenance Mode	0
0	0	1	Write Check	1
0	1	0	Get Status	2
0	1	1	Seek	3
1	0	0	Read Header	4
1	0	1	Write Data	5
1	1	0	Read Data	6
1	1	1	Read Data Without Header Check	7

Command execution starts when CRDY (bit 7) of the CSR is cleared by software. In a sense, then, bit 7 can be considered a negative GO bit.

Bit: 4-5 **Name:** BA16, BA17
Description: (Bus Address Extension Bits)
Two upper order bus address bits. Read and written as bits 4 and 5 of the CSR, they function as address bits 16 and 17 of the BAR.

Bit: 6 **Name:** IE
Description: (Interrupt Enable)
When this bit is set by software, the controller is allowed to interrupt the processor at the assertion of CRDY. This occurs at the normal or error termination of a command. Once an interrupt request is posted in the LSI bus, it is not removed until serviced, even if IE is cleared.

Bit: 7 **Name:** CRDY
Description: (Controller Ready)
When cleared by software, this bit indicates that the command in bits 1-3 is to be executed. Software cannot set this bit because no registers are accessible while CRDY is 0.

Bit: 8-9 **Name:** DS0, DS1
Description: (Drive Select)
These bits determine which drive will communicate with the controller via the drive bus.

Bit: 10 **Name:** OPI
Description: (Operation Incomplete)
When set, this bit indicates that the current command was not completed within the OPI timer period.

Bit: 11 **Name:** DCRC or HCRC
Description: (Data CRC) or (Header CRC)
IF OPI (bit 10) is cleared and bit 11 is set, the CRC error occurred on the data (DCRC). If OPI (bit 10) is set and bit 11 is also set, the CRC error occurred on the header (HCRC).

NOTE

Cyclic redundancy checking is done only on the desired header. It is performed on the first and second header words, even though the second header word is always 0.

Bit: 12 **Name:** DLT or HNF Error
Description: (Data Late) or (Header Not Found)
When OPI (bit 10) is cleared and bit 12 is set, it indicates that a data-late condition occurred in a read without a header check operation. The FIFO was more than half full and the controller was unable to transfer the next sequential sector.

When OPI (bit 10) is set and bit 12 is also set, it indicates that a timeout occurred while the controller was searching for the correct sector to read or write (no header compare).

Bit: 13 **Name:** NXM
Description: (Nonexistent Memory)
When set, this bit indicates that during a DMA data transfer, the memory location addressed did not respond within 10 μs.

Bit: 14 **Name:** DE
Description: (Drive Error)
This bit is buffered from the drive error interface line. When set, it indicates that the selected drive has flagged an error, the source of which can be determined by executing a get status command.

Bit: 15 **Name:** ERR
Description: (Composite Error)
When set, this bit indicates that one or more of the error bits (bits 10-14) are set. When an error occurs, the current operation terminates and an interrupt routine is initiated if the interrupt enable bit (bit 6 of the CSR) is set.

At the beginning of each controller command, error bits 10-13 are automatically cleared. At the completion of each controller command, bit 7 is automatically set. (Bit 7 is also set if an error is detected during command execution.)

The functions of control/status register bits 1-3 are described in the following paragraphs.

Maintenance Function (0) The maintenance command provides a means of exercising the controller logic circuits to test whether the major data paths and data storage functions are operating. This command is used during the diskless diagnostic routine to detect controller malfunctions or to establish a level of confidence in controller operations.

The first circuitry tested is the microsequencer wait and branch logic, followed by branch conditions WCOFLW and MISMATCH. Upon successful completion of this test, the DAR is incremented by 1. This is used as a trace feature to show in which test a failure occurred.

The next circuit element to be tested is the silo (first-in/first-out buffer). A microsequencer routine is initiated to transfer 256 words of data from memory into the silo and then back to memory again. This exchange is performed under DMA control and again the DAR is incremented by 1 (which is the original DAR + 3).

Next a test word previously loaded into the disk address register (DAR) is sequenced through the controller data path and cyclic redundancy checking (CRC) logic to end up in the silo. The resultant silo word is in the form of the CRC of the test word.

The DAR is then incremented by 1 and the test word + 1 is sequenced through the same data paths and CRC to become the second silo word. This second silo word is in the form of the CRC of the test word + 1. The DAR is then incremented by 1 again.

Finally, to exercise the silo serial output stage, this second silo word is shifted out of the silo and sequenced through the same data paths and CRC circuit another time before coming to rest in the silo again. It now becomes the new second silo word and has the form of the CRC of the test word + 1. The DAR is then incremented by 1 again.

The results of this exercise are two adjacent data blocks in memory, two test words residing in the silo, and the test word + 3 residing in the DAR.
The silo buffer contains 225 words and each data block in memory occupies 256 locations.

The two words residing in the silo can be accessed via the multipurpose register. The first word is a test of the data paths. The second word is a test of the data paths plus the silo serial output stage. These words are read into memory and software monitored for malfunctions.

Write Check (1) The write check command compares the data in the memory buffer to the data on the disk. Write check functions the same as a read, except the data transfer is from the memory.

Get Status Function (2) The get status command initiates a microsequencer routine that shifts a drive command word from the controller to a selected drive. This word is a status request word that asks the drive to return information concerning its current operation and error status. If the reset bit in the status request is set, the drive will first clear all soft errors (those no longer present) before sending back drive status. When the drive sends back its status word, it is stored in the controller silo to await later access through the multipurpose register.

One prerequisite for issuing the get status command is a knowledge that the controller is in the ready state. It is important to note that the drive does not have to be ready (for example, during a seek or when in the load state) to issue a get status command.

The only programming prerequisite is that the status request word be loaded first into the disk address register before issuing the get status command.

Seek Function (3) The seek command initiates a microsequencer routine that shifts a drive command word from the controller DAR to the drive. This drive command word contains head position information that includes the cylinder distance to be moved, the direction of movement, and the head to be selected for the next data transfer operation. Once this positioning information is received by the drive, the heads seek to the new track location.

There are several prerequisites for issuing a seek command. First, the present location must be known and this is available from the read header function. Once this is known, the software must calculate the cylinder difference information needed by the drive to reposition the heads. Then, before issuing the seek command, the software must know that the controller is in the ready state.

The only programming prerequisite is to load the disk address register with the head positioning information prior to issuing the seek function.

Read Header Function (4) The functions of the read header command are to read the first header encountered on the selected drive and to store the three header words in the silo. These are: header WD1, which contains the cylinder address, head select, the selector;

header WD2, which contains all zeros; and header WD3, which contains the header CRC. One or more header words can then be extracted from the silo by reading the MPR. Extracting the first header word alone provides sufficient head positioning information to permit software calculation of cylinder difference for a subsequent seek operation to a new track address.

The only prerequisite for issuing the read header command is knowledge that the controller is in the ready state.

Write Data Function (5) The write data command initiates a microsequencer routine that enables the controller DMA circuitry. The controller eventually becomes LSI-11 bus master and data words are loaded into the silo. When the drive is ready, header information is continually read off the disk and compared with the first sector address stored in the DAR. Once a header match is found, the silo data is written on the disk in successive sectors until the word counter overflows. For partial sector writes, the remaining sector area is filled with 0s.

There are two prerequisites for the write data command. The first is that the heads must already be located at the correct track. This implies issuing a seek command if necessary. Also, the software must know that the controller is in the ready state before issuing a command.

Read Data Function (6) The read data command initates a controller microsequencer routine that reads successive headers off the disk and compares them against the first sector address in the DAR. When a header match is found, disk data is transferred into the silo and out to the LSI-11 bus under DMA control. The data transfer ends when the word counter overflows.

There are two prerequisites for the read data command. The first is that the heads must be located at the correct track. This implies issuing a seek command if necessary. The second is that software must know that the controller is ready to accept a command.

Read Without Header Check Function (7) This command allows the recovery of data if the headers become unreadable. If header not found (HNF) or header CRC (HCRC) errors are encountered on a particular sector, then data is not recoverable by the standard read data command.

To convert this data, a seek command must be issued if the heads are not already located on the track where the bad sector is. Then the

sector preceding the bad sector must be located by performing successive read header commands. Finally a read header without header check command can be issued within 300 μs to recover the next sector if the controller is ready.

Bus Address Register (BAR) — The bus address register (Figure 7) is a 16-bit, word-addressable register with an address of 174402. Bits 0 through 15 can be read or written; bit 0 should normally be written as 0. Expansions bits 16 and 17 are programmable via bits 4 and 5 of the CSR.

The bus address register indicates the memory location involved in the DMA data transfer during a read or write operation. The contents of the BAR are automatically incremented by 2 as each word is transferred between the system memory and the controller.

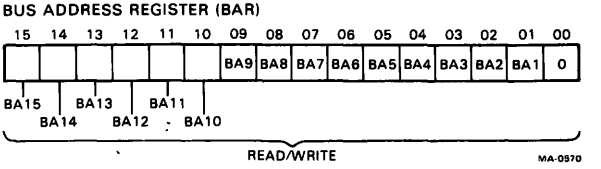


Figure 7 Bus Address Register

Clearing of the BAR is accomplished by executing a BUS INIT.

Disk Address Register (DAR) — The disk address register is a 16-bit, read/write, word-addressable register with an address of 174404. Its contents can have one of three meanings, depending on the function being performed. Clearing of this register is accomplished by executing a BUS INIT.

DAR During a Seek Command To perform a seek function, it is necessary to provide address difference, head select, and head directional information to the selected drive as indicated in Figure 8. The word format is described in Table 4.

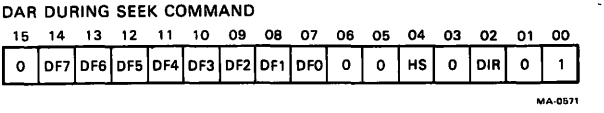


Figure 8 DAR Seek Command

Table 4 DAR Seek Command Word Format

Bit: 0 **Name:** MRKR
Description: (Marker)
Must be a 1.

Bit: 1 **Name:**
Description: Must be a 0, indicating to the drive that a seek command is being requested and that the remaining bits in the register will contain the seek specifications.

Bit: 2 **Name:** DIR
Description: (Direction)
This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 7-14).

Bit: 3 **Name:**
Description: Must be a 0.

Bit: 4 **Name:** HS
Description: (Head Select)
Indicates which head (disk surface) is to be selected. Set = lower, clear = upper.

Bit: 5-6 **Name:**
Description: Reserved

Bit: 7-14 **Name:** DF (07:00)
Description: (Cylinder Address Difference)
Indicates the number of cylinders the heads are to move on a seek.

Bit: 15 **Name:**
Description: Must be a 0.

DAR During Read or Write Data Command For a read, write, or write-check operation, the DAR is loaded with the address of the first sector to be transferred. Thereafter, as each adjoining sector is transferred, the DAR is automatically incremented by 1 (Figure 9). If the DAR increments to the nonexistent sector address (50_8), OPI time-out will occur. The word format is described in Table 5.

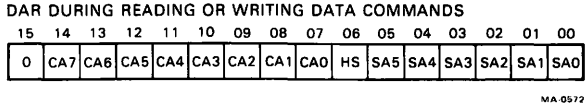


Figure 9 DAR Read/Write Data Command

Table 5 DAR Read/Write Data Command Word Format

Bit: 0-5 **Name:** SA (5:0)
Description: (Sector Address)
Address of one of the 40 sectors on a track. (Octal range is 0 to 47).

Bit: 6 **Name:** HS
Description: (Head Select)
Indicates which head (disk surface) is to be selected. Set = lower; clear = upper.

Bit: 7-14 **Name:** CA (7:0)
Description: (Cylinder Address)
Address of one of the 256 cylinders. (Octal range is 0 to 377).

Bit: 15 **Name:** Not used
Description: Must be a 0.

DAR During a Get Status Command After the get status command is deposited in the CSR, it is the DAR's responsibility to get the command transferred to the drive. Therefore, the DAR must also be programmed along with the CSR to do the get status command.

For a get status command, the DAR register bits must be programmed as shown in Figure 10; the word format is described in Table 6.

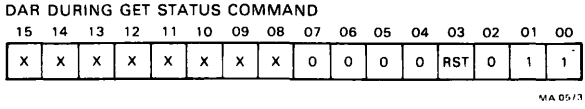


Figure 10 DAR Get Status Command

Table 6 DAR Get Status Command Word Format

Bit: 0 **Name:** MRKR
Description: (Marker)
Must be a 1.

Bit: 1 **Name:** GS
Description: (Get Status)
Must be a 1, indicating to the drive that its status word is being requested. At the completion of the get status command, the drive status word is read into the controller multipurpose (MP) register (output stage of FIFO). With this bit set, bits 8-15 are ignored by the drive.

Bit: 2 **Name:** Not used
Description: Must be a 0.

Bit: 3 **Name:** RST
Description: (Reset)
When this bit is set, the drive clears its error register of soft errors before sending a status word to the controller.

Bit: 4-7 **Name:** Not used
Description: Must be a 0.

Bit: 8-15 **Name:**
Description: Not used.

Multipurpose Register (MPR) — The MPR is made up of two registers bearing the same base address. When writing into that location, the word counter accepts the data. When reading from that location, the FIFO output buffer provides the data.

MPR During a Get Status Command When a get status command is executed and a status word is returned to the controller, the MPR (FIFO output stage) format is as shown in Figure 11 and described in Table 7.

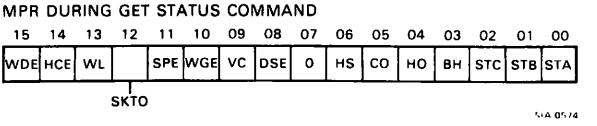


Figure 11 MPR Status Word

Table 7 MPR Status Word Format

Bit: 0-2 **Name:** State (C:A)
Description: These bits define the state of the drive:

C	B	A	
0	0	0	Load State
0	0	1	Spin up
0	1	0	Brush cycle
0	1	1	Load heads
1	0	0	Seek track counting
1	0	1	Seek linear mode (lock on)
1	1	0	Unload heads
1	1	1	Spin down

Bit: 3 **Name:** BH
Description: (Brush Home)
Asserted when the brushes are not over the disk.

Bit: 4 **Name:** HO
Description: (Heads Out)
Asserted when the heads are over the disks.

Bit: 5 **Name:** CO
Description: (Cover Open)
Asserted when the cover is open or the dust cover is not in place.

Bit: 6 **Name:** HS
Description: (Head Select)
Indicates the currently selected head.

Bit: 7 **Name:**
Description: Reserved. Will be 0.

Bit: 8 **Name:** DSE
Description: (Drive Select Error)
Indicates multiple drive selection is detected.

Bit: 9 **Name:** VC
Description: (Volume Check)
VC is set every time the drive goes into load heads state. This asserts a drive error at the controller but not on the front panel. VC is an indication that program does not really know which disk is present until it has read the serial number and bad selector file. (The disk might have been changed while the heads were unloaded.)

Bit: 10 **Name:** WGE
Description: (Write Gate Error)
Indicates the drive sensed that write gate was asserted when sector pulse was asserted, or write gate was set with the drive not ready, or the drive was write-locked.

Bit: 11 **Name:** SPE
Description: (Spin Error)
Indicates the spindle is not reaching speed in the required time, or over speeding.

Bit: 12 **Name:** SKTO
Description: (Seek Time Out)
Indicates the heads did not come on track in the required time during a seek command.

Bit: 13 **Name:** WL
Description: (Write Lock)
Indicates write lock status of selected drive.

Bit: 14 **Name:** HCE
Description: (Head Current Error)
Indicates write current was detected in the heads when write gate was not asserted.

Bit: 15 **Name:** WDE
Description: (Write Data Error)
Indicates write gate was asserted but no transitions were detected on the write data line.

MPR During a Read Header Command When a read header command is executed, three words will be stored in the multipurpose register (FIFO output buffer). The first header word will contain sector address, head select, and cylinder address information. The second word will contain all 0s. The third word will contain the header CRC information. All three words are readable by the main program (Figure 12).

MPR During Read/Write Data Commands When transferring data via DMA, the MPR functions as a word counter and is loaded by the program with the 2's complement of the number of words to be transferred. It is then incremented by 1 by the controller as each word is transferred. The reading or writing operation generally is terminated when the word counter overflows. The word counter can keep track of from one data word to the full 40-sector count of 5120 data words (decimal). The maximum number of words that can be transferred in a

single operation is limited by the number of sectors available to be written in the track (Figure 13). The word counter format is described in Table 8.

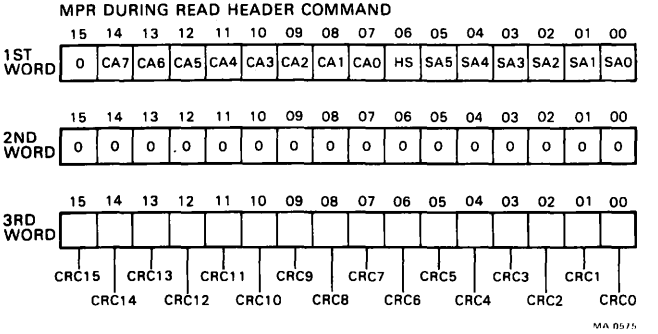


Figure 12 MPR Three Header Words

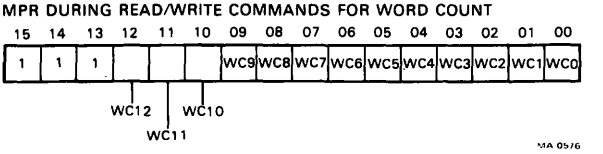


Figure 13 MPR Used as Word Counter

Table 8 MPR Word Counter Format

Bit: 0-12 **Name:** WC (12:0)
Description: (Word Count)
2's complement of total number of words to be transferred.

Bit: 13-15 **Name:**
Description: Must be all 1s for word count in correct range.

Operator Controls and Indicators

The following switches and indicators are located on the RL01 front bezel.

1. RUN/STOP switch with LOAD indicator light
2. UNIT SELECT switch with READY indicator light
3. FAULT indicator light
4. WRITE PROTECT switch with WRITE PROTECT indicator light

Power ON/OFF control is via a rear panel circuit breaker switch which is normally left in the ON position. Operation of this circuit breaker switch will not damage the drive in any way.

RUN/STOP Switch with LOAD Indicator — The RUN/STOP switch is a push/push alternating action switch which, when depressed, energizes the spindle motor. When released, it de-energizes the spindle motor provided the heads are not loaded and the brushes are retracted. If the heads are loaded, it causes the heads to unload and then de-energizes the spindle motor.

The switch contains mechanical memory. In the event of main power disruption and subsequent restoration, the drive will cycle up if the switch is in the depressed state.

The LOAD indicator is lit whenever the spindle is stopped, heads home, brushes home, and the spindle motor is not energized. A cartridge can be loaded when this indicator is lit.

UNIT SELECT Switch with READY Indicator — The UNIT SELECT switch is a cam-operated switch which is actuated by inserting a numbered cam button. The numbered cam button is such that the drive logic will recognize the drive address code corresponding to the unit select number on the cam button. The numbered indicator lights to indicate the condition identified, such as heads loaded and locked on a cylinder, or drive ready for read or write operations.

FAULT Indicator — The FAULT indicator is lit whenever a fault or error condition occurs in the drive.

WRITE PROTECT Switch with WRITE PROTECT Indicator — The WRITE PROTECT switch is a push/push alternating action switch. When depressed, it sets the drive in write protect mode. If the drive is in the process of writing at the time that the switch is depressed, writing will continue until the write gate is negated at the next sector pulse. The WRITE PROTECT indicator will not be illuminated until the write protect function is enabled. Removal of write protect will occur immediately upon the deactivation of the WRITE PROTECT switch.

I/O Transfer Operations

There are three kinds of I/O transfers that are used to interface the processor with the RLV11 controller. They are programmed I/O transfers, DMA transfers, or interrupt-driven transfers.

Programmed I/O transfers are executed by single- or double-operand PDP-11 instructions. By including the device's address as the effective source or destination address, the user specifies the transfer as an input or output operation. Programmed I/O allows information to be transferred between the RLV11 addressable registers and LSI-11 memory locations and processor registers. The transfer of each word requires the execution of a PDP-11 instruction.

DMA transfers, on the other hand, require only a few programmed I/O transfers to set control information. Then a large block of data can be moved to or from memory without any support from the processor. DMA transfers are the fastest method of transferring data between memory and a device. They can occur between processor bus cycles and do not alter processor status in any way. Blocks of data can be moved at speeds that are not limited by processor instruction execution via the DMA transfer mode. The read and write data in the controller FIFO is received and transmitted under DMA control.

Interrupt-driven transfers allow the processor to continue a programmed operation without waiting for the controller to become ready. When the controller becomes ready, it interrupts the processor's background program sequence and causes execution of the controller's service routine. After the controller's service routine has been executed, the background program is restored and program execution resumes at the point where it was interrupted.

Programmed I/O Transfers — Every processor instruction requires one or more I/O operations. The first operation required is a data input transfer (DATI), which fetches an instruction from memory at the location addressed by the program counter. This operation is called a DATI bus cycle. If the controller is referenced, additional DATI, or data output transfer (DATO) bus cycles are required.

Writing Controller Registers When writing the controller registers, the CPU is the bus master and the controller is the slave. The initial DATI fetch cycle is followed by a DATO cycle.

Reading Controller Registers When reading the controller registers, the CPU is bus master and the controller is the slave. The processor performs a DATI cycle to obtain the data from the RLV11 registers.

The DATI cycle is a result of a processor-programmed instruction which addresses the controller registers.

DMA I/O Transfers — Direct memory access (DMA) is used to transfer data between the controller FIFO and memory without program control. The processor can service DMA requests between bus cycles. Upon receiving BDMR requests from the bus, the processor sets up the conditions for DMA transfer by granting bus mastership to the BDMG priority daisy-chain. If a high-priority device is requesting bus mastership, it will receive it and inhibit passage of the processor's grant, regardless of other low priority requests. If it is not requesting bus mastership, it will pass the processor's BDMGO through other nonrequesting devices to the one that is requesting the mastership. In practice, the disk controller is the highest priority device, after memory, in the system.

Once the controller is bus master and memory is the slave, DMA transfers can occur without processor intervention. The DMA protocol circuit limits transfers to four words at a time to allow other devices to be serviced and to prevent interference with the memory refresh cycle. After a time-out of 4 μs, if the processor is bus master, the controller can reassert mastership and continue the transfer with another four words.

Interrupt-Driven I/O Transfers — Interrupts are requests made by the controller that cause the processor to temporarily suspend its present program sequence to execute the controller service routine. The controller can interrupt the processor only when its interrupt control circuit is enabled. This circuit is enabled by an interrupt enable (IE) bit in the control/status register. A program must set this bit before an interrupt request can be issued.

An interrupt vector associated with the RVL11 controller is located in the controller interface/control logic. This vector is an address pointer that allows automatic entry into the controller service routine without device polling. The vector is switch-selectable in the range 0-774.

The controller requests interrupt service by asserting BIRQ L. The processor acknowledges the interrupt request by asserting BDIN L followed by BIAKO L. The first device on the bus receives this daisy-chained signal at its BIAKI L input. If it is not requesting service, it passes the signal via its BIAKO L output to the next device, and so on, until the requesting device receives the signal. The requesting device responds by asserting BRPLY L and placing its interrupt vector on the data/address bus lines BDAL (0:15) L. Automatic entry to the service routine is then executed by the processor.

Bus Signal Timing

Diagrams illustrating the bus timing requirements between the processor and the RLV11 controller, given in general master/slave device terms, may be found in the *Microcomputer Processor Handbook* published by Digital Equipment Corporation.

RXV11 FLOPPY DISK OPTION

SPECIFICATIONS

Module	
Identification	M7946
Size	Double
Power	+5 V ±5% at 1.5 A
Bus Loads	
AC	1.8
DC	1
Drive	
Identification	RX01
Size	46.3 cm w × 28.7 cm h × 53.3 cm d (19 in w × 10.5 in h × 21 in d)
Recommmended Service Clearance (front and rear)	55 cm (22 in)
AC Power	4 A at 115 Vac; 2 A at 230 Vac (dual drive)
Cable Included	BC05L-15 (15 ft)
Drive Performance	
Capacity (8-bit bytes)	
Per diskette	256,256 bytes
Per track	3,328 bytes
Per sector	128 bytes
Data Transfer Rate	
Diskette to controller buffer	4 μsec/data bit (250K bits/sec)
Buffer to RXV11 interface	2 μsec/bit (500K bits/sec)
RXV11 interface to LSI-11 I/O bus	18 μsec/8-bit byte (<50K bytes/sec)
Track-to-track move	6 msec/track maximum
Head settle time	25 msec maximum
Rotational speed	360 rpm±2.5%; 166 msec/rev nominal

Recording surfaces per disk	1
Tracks per disk	77 (0-76) or ($0\text{-}114_8$)
Sectors per track	26 (1-26) or ($0\text{-}32_8$)
Sectors per disk	2002
Recording technique	Double frequency
Bit density	3200 bits/in at inner track
Track density	48 tracks/in
Average access	262 msec, computed as follows:

Seek	Settle	Rotate	Total

(77 tks/3) × 6 msec + 25 msec + (166 msec/2) = 262 msec

Environmental Characteristics

Temperature

RX01, operating	15° to 32° C (59° to 90° F) ambient; maximum temperature gradient = −6.7° C/hr (20° F/hr)
RX01, nonoperating	−35° to +60° C (−30° to +140° F)
Media, nonoperating	−35° to +52° C (−30° to +125° F)

NOTE

Media temperature must be within operating temperature range before use.

Relative Humidity

RX01, operating	25° C (77° F) maximum wet bulb 2° C (36° F) minimum dew point 20% to 80% relative humidity
RX01, nonoperating	5% to 98% relative humidity (no condensation)
Media, nonoperating	10% to 80% relative humidity
Magnetic field	Media exposed to a magnetic field strength of 50 oersteds or greater may lose data.

System Reliability	
Minimum number of revolutions/track	3 million/media (head-loaded)
Seek error rate	1 in 10^6 seeks
Soft read error rate	1 in 10^9 bits read
Hard read error rate	1 in 10^{12} bits read

NOTE

The above error rates apply only to media that are properly cared for. Seek error and soft read errors are usually attributable to random effects in the head/media interface, such as electrical noise, dirt, or dust. Both are called "soft" errors if the error is recoverable in ten additional tries or less. "Hard" errors cannot be recovered. Seek error retries should be preceded by an initialize.

CONFIGURATION

General

The factory jumper locations on the M7946 interface module are shown in Figure 1. Note that two styles of modules are used; one style (etch Rev B) has machine-inserted jumpers; the other (etch Rev C) has wire-wrap jumpers. All M7946 interface modules are configured and shipped with preselected register addresses and vectors as shown in Figure 2. The control/status register (RXCS) address is 177170, and the data buffer register (RXDB) address is 177172. The interrupt vector is 264_8. As supplied, the factory-configured jumpers are for the normal addresses used with DIGITAL software. However, in applications where more than one RXV11 system is required, appropriate register addresses and vectors may be configured by installing or removing jumpers. A second RXV11 system would normally be assigned register addresses 177174 (RXCS) and 177176 (RXDB), with an interrupt vector of 270_8 (Table 2).

Register Descriptions

Control/Status Register (RXCS)(177170) — The format for the RXCS register is shown in Figure 3. Bit descriptions are presented in Table 3. Loading the RXCS register while the RX01 is not busy and with bit 0 = 1 will initiate a function described in Table 3.

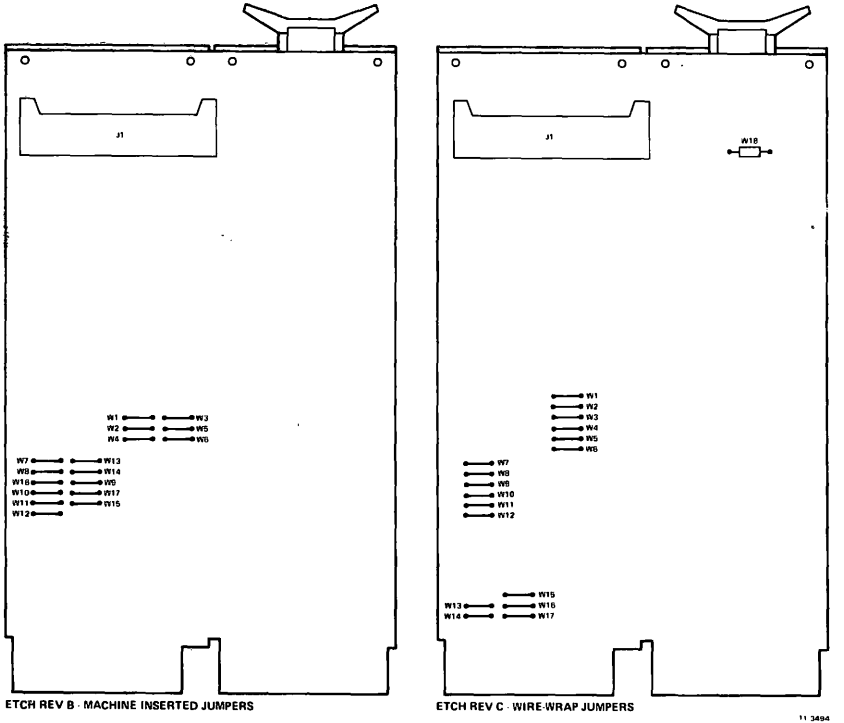


Figure 1 RXV11 Device Register and Interrupt Vector Jumper Locations

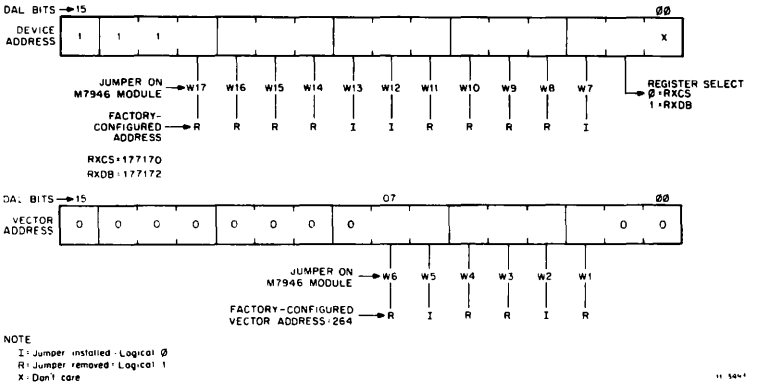


Figure 2 Device Register Address and Interrupt Vector

Table 1 RXV11 Configurations

System	Disk Drive	Line Voltage*
RXV11-AA	Single drive system	115V/60 Hz
RXV11-AC	Single drive system	115V/50 Hz
RXV11-AD	Single drive system	230V/50 Hz
RXV11-BA	Dual drive system	115V/60 Hz
RXV11-BC	Dual drive system	115V/50 Hz
RXV11-BD	Dual drive system	230V/50 Hz

* 50 Hz versions are available in voltages of 105, 115, 220, and 240 Vac by field-pluggable conversion.

Table 2 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address	Second Module Address
Registers				
Control/Status	RXCS	R/W	177170	177174
Data Buffer	RXDB	R/W	177172	177176
Interrupt				
Function Complete	Done	—	264	270

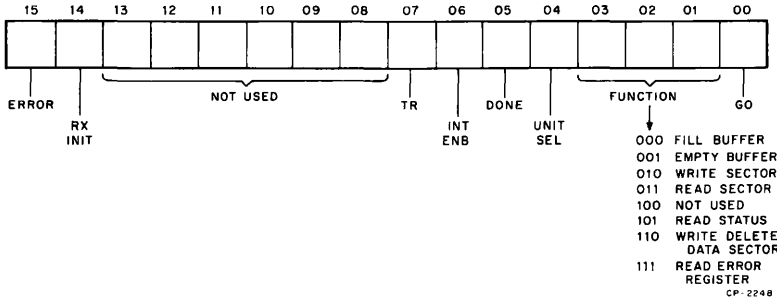


Figure 3 RXCS Format

Table 3 RXCS Bit Descriptions

Bit	Description
0	Go. Initiates a command to RX01. This is a write-only bit.
1-3	Function Select. These bits code one of the eight possible functions described in detail in this section. These are write-only bits.
4	Unit Select. This bit selects one of the two possible disks for execution of a desired function. This is a write-only bit.

5	Done. This bit indicates the completion of a function. Done will generate an interrupt when asserted if interrupt enable (RXCS bit 6) is set. This is a read-only bit.
6	Interrupt Enable. This bit is set by the program to enable an interrupt when the RX01 has completed an operation (done). The condition of this bit is normally determined at the time a function is initiated. This bit is cleared by LSI-11 bus initialize (BINIT L) signal, but it is not cleared by the RXV11 initialize bit (RXCS bit 14). This is a read/write bit.
7	Transfer Request. This bit signifies that the RXV11 needs data or has data available. This is a read-only bit.
8-13	Unused.
14	RXV11 Initialize. This bit is set by the program to initialize the RXV11 without initializing all of the devices on the LSI-11 bus. This is a write-only bit.

Caution

1. Loading the lower byte of the RXCS will also load the upper byte of the RXCS.
2. Setting this bit (BIS instruction) will not clear the interrupt enable bit (RXCS bit 6).

Upon setting this bit in the RXCS, the RXV11 will negate done and move the head position mechanism of drive 1 (if two are available) to track 0. Upon completion of a successful initialize, the RX01 will zero the error and status register, set initialize done, and set RXES bit 7 (DRV RDY) if unit 0 is ready. It will also read sector 1 of track 1 on drive 0.

15	Error. This bit is set by the RX01 to indicate that an error has occurred during an attempt to execute a command. This read-only bit is cleared by the initiation of a new command or by setting the initialize bit. When an error is detected, the RXES is automatically read into the RXDB.

Data Buffer Register (RXDB)(177172)

This RX01 interface register serves as a general purpose data path between the RX01 and the interface. It may represent one of five RX01 registers according to the protocol of the command function in progress. The RX01 registers include RXDB, RXTA, RXSA, RXES, and RXER; each is described below.

This register is read/write if the RX01 is not in the process of executing a command. That is, it may be manipulated without affecting the RX01 subsystem. If the RX01 is actively executing a command, this register will accept data only if RXCS bit 7 (TR) is set. In addition, valid data can be read only when TR is set.

Caution

Violation of protocol in manipulation of this register may cause permanent data loss.

RX Data Buffer (RXDB) (Figure 4) — All information transferred to and from the floppy media passes through this register. It is addressable only under the protocol of the function in progress.

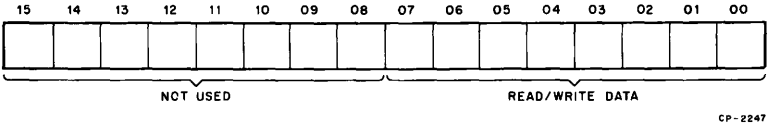


Figure 4 RXDB Format

RX Track Address (RXTA) (Figure 5) — This register is loaded to indicate on which of the 114_8 tracks a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.

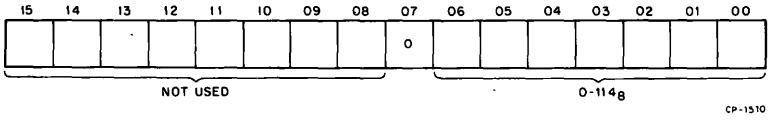


Figure 5 RXTA Format

RX Sector Address (RXSA) (Figure 6) — This register is loaded to indicate on which of the 32_8 sectors a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.

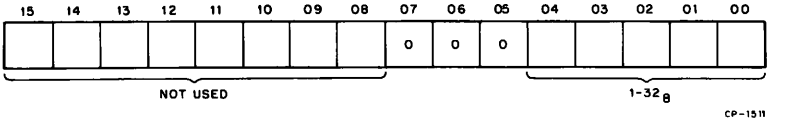


Figure 6 RXSA Format

RX Error and Status (RXES) (Figure 7) — This register contains the current error and status conditions of the drive selected by bit 4 (unit select) of the RXCS. This read-only register can be addressed only under the protocol of the function in progress. The RXES is located in the RXDB upon completion of a function. Table 4 lists the RXES bit descriptions.

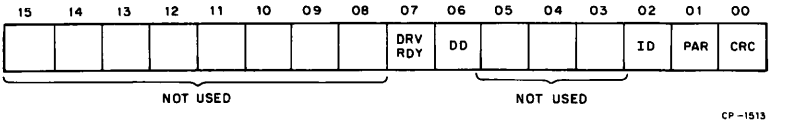


Figure 7 RXES Format

Table 4 RXES Bit Descriptions

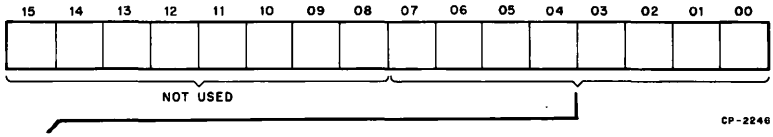
Bit	Description
0	CRC Error. A cyclic redundancy check error was detected as information was retrieved from a data field of the diskette. The RXES is moved to the RXDB, and error and done are asserted.
1	Parity Error. A parity error was detected on command or on address information being transferred to the RX01 from the LSI-11 bus interface. A parity error indication could mean that there is a problem in the interface cable between the RX01 and the interface. Upon detection of a parity error, the current function is terminated; the RXES is moved to the RXDB, and error and done are asserted.
2	Initialize Done. This bit is asserted in the RXES to indicate completion of the initialize routine, which can be caused by RX01 power failure, system power failure, or programmable or LSI-11 bus initialization.
3-5	Unused.
6	Deleted Data Detected. During data recovery, the identification mark preceding the data field was decoded as a deleted data mark.
7	Drive Ready. This bit is asserted if the unit currently selected exists, is properly supplied with power, has a diskette installed correctly, has its door closed, and has a diskette up to speed.

NOTE

The drive ready bit is only valid when retrieved via a read status function or at completion of initialize when it indicates status of drive 0.

If the error bit was set in the RXCS but error bits are not set in the RXES, then specific error conditions contained in the RXER can be accessed from the RXDB via a read error register function.

RX Error (RXER) (Figure 8) — This register is located in the RX01 and contains specific RX01 error information. This information is normally accessed when RXCS error bit 15 is set but RXES error bits 0 and 1 are not set. This is a read-only register.



Octal Code	Error Code Meaning
010	Drive 0 failed to see home on initialize.
020	Drive 1 failed to see home on initialize.
030	Found home when stepping out 10 tracks for INIT.
040	Tried to access a track greater than 77.
050	Home was found before desired track was reached.
060	Self-diagnostic error.
070	Desired sector could not be found after looking at 52 headers (2 revolutions).
110	More than 40 μsec and no SEP clock seen.
120	A preamble could not be found.
130	Preamble found but no I/O mark found within allowable time span.
140	CRC error on what was thought to be a header.
150	The header track address of a good header does not compare with the desired track.
160	Too many tries for an IDAM (identifies header).
170	Data AM not found in allotted time.
200	CRC error on reading the sector from the disk. No code appears in the ERREG.
210	All parity errors.

Figure 8 RXER Format

Function Codes

Data storage and recovery on the RXV11 system is accomplished by careful manipulation of the RXCS and RXDB registers according to the strict protocol of individual functions. The penalty for violation of protocol can be permanent data loss. Each of the functions is encoded and written into RXCS bits 1-3, as shown in Figure 3. Programming protocol for each function is described below.

Fill Buffer (000) — This function is used to fill the RX01 buffer with 128 8-bit bytes of data from the host processor. Fill buffer is a complete function in itself. The function ends when the buffer has been filled. The contents of the buffer can be written onto the diskette by means of a subsequent write sector function, or the contents can be returned to the host processor by an empty buffer function.

RXCS bit 4 (unit select) does not affect this function, since no diskette drive is involved. When the command has been loaded, RXCS bit 5 (done) is negated. When the TR bit is asserted, the first byte of data may be loaded into the data buffer. The same TR cycle will occur as each byte of data is loaded. The RX01 counts the bytes transferred. It will not accept less than 128 bytes and will ignore those in excess. Any read of the RXDB during the cycle of 128 transfers results in invalid read data.

Empty Buffer (001) — This function is used to empty the internal buffer of the 128 data bytes loaded from a previous read sector or fill buffer command. This function will ignore RXCS bit 4 (unit select) and negate done.

When TR sets, the program may unload the first of 128 data bytes from the RXDB. Then the RXV11 again negates TR. When TR resets, the second byte of data may be unloaded from the RXDB, which again negates TR. Alternate checks on TR and data transfers from the RXDB continue until 128 bytes of data have been moved from the RXDB. Done sets, ending the operation and initiating an interrupt if RXCS bit 6 (interrupt enable) is set. RXES contents are moved to the RXDB where they can be read.

NOTE

The empty buffer function does not destroy the contents of the sector buffer.

If the deleted data address mark was detected, the control will assert RXES bit 6 (DD). As data enters the sector buffer, a CRC is computed, based on the data field and CRC bytes previously recorded. A non-

zero residue indicates that a CRC error has occurred. The control sets RXES bit 0 (CRC error) and RXCS bit 15 (error). The RXV11 ends the operation by moving the contents of the RXES to the RXDB, sets done, and initiates an interrupt if RXCS bit 6 (interrupt enable) is set.

Read Status (101) — The RXV11 will negate RXCS bit 5 (done) and begin to assemble the current contents of the RXES into the RXDB. RXES bit 7 (drive ready) will reflect the status of the drive selected by RXCS bit 4 (unit select) at the time the function was given. All other RXES bits will reflect the conditions created by the last command. RXES may be sampled when RXCS bit 5 (done) is again asserted. An interrupt will occur if RXCS bit 6 (interrupt enable) is set.

NOTE

The average time for this function is 250 ms. Excessive use of this function will result in substantially reduced throughput.

Write Sector with Deleted Data (110) — This operation is identical to function 010 (write sector), with the exception that a deleted data address mark precedes the data field instead of a standard data address mark.

Read Error Register Function (111) — The read error register function can be used to retrieve explicit error information contained in the RXER when RXCS error bit 15 is set. The function is initiated, and bits 0-6 of the RXES are cleared. Out is asserted and done is negated. The controller then generates the appropriate number of shift pulses to transfer the specific error code from the RXER to the interface register and completes the function by asserting done. The RXDB program can then read the error code to determine the type of failure that occurred (Figure 8).

NOTE

Care should be exercised in the use of this function since, under certain conditions, erroneous error information may result.

Power Fail — There is no actual function code associated with power fail. When the RX01 senses a loss of power, it will unload the head and abort all controller action. All status signals are invalid while power is low.

When the RX01 senses the return of power, it will remove done and begin a sequence to:

1. Move drive 0 head position mechanism to track 0.
2. Clear any active error bits.
3. Read sector 1 of track 1 of drive 0 into the sector buffer.
4. Set RXES bit 2 (initialize done) after which done is again asserted.
5. Set drive ready of the RXES according to the status of drive 0.

Write Sector (010) — This function is used to locate a desired track and sector and write the sector with the contents of the internal sector buffer. The initiation of this function clears bits 0, 1 and 6 of RXES (CRC error, parity error, and deleted data detected) and negates done.

When TR is asserted, the program must first move the desired sector address into the RXDB, which will negate TR. When TR is again asserted, the program must move the desired track address into the RXDB, which will negate TR. If the desired track is not found, the RXV11 will abort the operation, move the contents of the RXES to the RXDB, set RXCS bit 15 (error), assert done, and initiate an interrupt if RXCS bit 6 (interrupt enable) is set.

TR will remain negated while the RX01 attempts to locate the desired sector. If the RX01 is unable to locate the desired sector within two diskette revolutions, the RXV11 will abort the operation, move the contents of the RXES to the RXDB, set RXCS bit 15 (error), assert done, and initiate an interrupt if RXCS bit 6 (interrupt enable) is set.

If the desired sector is successfully located, the RXV11 will write the 128 bytes stored in the internal buffer followed by a 16-bit CRC character that is automatically calculated by the RX01. The RXV11 ends the operation by asserting done and initiating an interrupt if RXCS bit 6 (interrupt enable) is set.

NOTE

The contents of the sector buffer are not valid data after a power loss has been detected by the RX01. The write sector function, however, will be accepted as a valid function, and the random contents of the buffer will be written, followed by a valid CRC.

The write sector function does not destroy the contents of the sector buffer.

Read Sector (011) — This function is used to locate a desired track and sector and transfer the contents of the data field to the microCPU controller sector buffer. The initiation of this function clears bits 0, 1, and 6 of RXES (CRC error, parity error, and deleted data detected) and negates done.

When TR is asserted, the program must first move the desired sector address into the RXDB, which will negate TR. When TR is again asserted, the program must move the desired track address into the RXDB, which will negate TR.

If the desired track is not found, the RXV11 will abort the operation, move the contents of the RXES to the RXDB, set RXCS bit 15 (error), assert done, and initiate an interrupt if RXCS bit 6 (interrupt enable) is set.

TR and done will remain negated while the RX01 attempts to locate the desired track and sector. If the RX01 is unable to locate the desired sector within two diskette revolutions after locating the presumably correct track, the RXV11 will abort the operation, move the contents of the RXES to the RXDB, set RXCS bit 15 (error), assert done, and initiate an interrupt if RXCS bit 6 (interrupt enable) is set.

If the desired sector is successfully located, the control will attempt to locate a standard data address mark or a deleted data address mark. If either mark is properly located, the control will read data from the sector into the sector buffer.

There is no guarantee that information being written at the time of a power failure will be retrievable. However, all other information on the diskette will remain unaltered.

One method of aborting a function is through the use of RXCS bit 14 (RXV11 initialize); however, this will not clear the interrupt enable bit (RXCS bit 6). Another method is through the use of the system initialize signal that is generated by the PDP-11 RESET instruction, the console ODT Go command, or system power failure.

PROGRAMMING

Bootstrapping the RXV11

The RXV11 bootstrap loader program loads the system monitor from disk into system memory. No system operation can occur until the monitor is contained in system memory. Bootstrapping ("booting") the system can be accomplished via a hardware-implemented bootstrap in the REV11-A, REV11-C, or the BDV11 option, or it can be entered and executed via the console device.

RXV11

When a bootstrap option is not included in the system, the operator must enter a bootstrap program via the console device. Place the processor in the Halt mode and proceed as shown below; The bootable volume must be in drive zero. All devices are at standard addresses and vectors. Enter the code starting at location 1000. Inhibit all interrupts by entering RS/__340 <CR>. Initialize the program counter by entering R7/__1000 <CR>. After the code has been entered, type P.

	RX01		RX01
LOCATION	**CODE**	**LOCATION**	**CODE**
1000	12702	1040	111023
1002	100247	1042	30211
1004	12701	1044	1776
1006	177170	1046	100756
1010	130211	1050	103766
1012	1776	1052	105711
1014	112703	1054	100771
1016	7	1056	5000
1020	10100	1060	22710
1022	10220	1062	240
1024	402	1064	1347
1026	12710	1066	122702
1030	1	1070	247
1032	6203	1072	5500
1034	103402	1074	5007
1036	112711		

RXV21 FLOPPY DISK OPTION

GENERAL

The RXV21 floppy disk option is a random access mass memory device that stores data in fixed-length blocks on a preformatted, flexible diskette. Each diskette can store and retrieve up to 512K 8-bit bytes of data. The RXV21 system is rack-mountable and consists of an interface module, an interface cable, and either a single or dual RX02 floppy disk drive.

FEATURES

- Compact disk system
- Stores/retrieves 512K 8-bit bytes of data
- Rack mountable
- Available with either single or dual disk drive
- Available for 115 or 230 Vac, 50 or 60 Hz
- Can be converted (50 Hz version) for 105, 115, 220 or 240 Vac operation
- Direct Memory Access data tranfer
- Industry-compatible mode under software selection

SPECIFICATIONS

Module

Identification	M8029
Size	Double
Power	+5V ±5% at 1.8A typically
Bus Loads	
AC	3
DC	1

Drive

Identification	RX02
Size	46.3 cm w × 28.7 cm h × 53.3 cm d (19 in. w × 10.5 in. h × 21 in. d)
Recommended Service	55 cm (22 in.) Clearance (front and rear)

RXV21

AC Power	4A at 115 Vac; 2A at 230 Vac (dual drive)
Cable Included	BC05L-15 (15 ft.)
Drive Performance	
Capacity (8-bit bytes)	
Per diskette	512,512 bytes
Per track	6,656 bytes
Per sector	256 bytes
Data Transfer Rate	
Diskette to controller buffer	2 μsec/data bit (500K bits/sec)
Buffer to RXV21 interface	1.2 μsec/bit (500K bits/sec)
RXV21 interface to LSI-11 I/O bus	23 μsec/16-bit word
Track-to-track move	6 msec/track maximum
Head settle time	25 msec maximum
Rotational speed	360 rpm ±2.5%; 166 msec/rev nominal
Recording surfaces per disk	1
Tracks per disk	77 (0-76) or ($0\text{-}114_8$)
Sectors per track	26 (1-26) or ($0\text{-}32_8$)
Sectors per disk	2002
Recording technique	Double frequency (FM) or modified (MFM)
Bit density	3200 bpi (FM); 6400 bpi (modified MFM)
Track density	48 tracks/in.
Average access	262 msec, computed as follows:

Seek	Settle	Rotate	Total

(77 tks/3) × 6 msec + 25 msec + (166 msec/2) = 262 msec

Environmental Characteristics	
Temperature	
RX02, operating	15° to 32° C (59° to 90° F) ambient; maximum temperature gradient = 11°C/hr (20°F/hr)
RX02, nonoperating	−35° to +60° C (−30° to +140° F)
Media, nonoperating	−35° to +52° C (−30° to +125° F)

NOTE

Media temperature must be within operating temperature range before use.

Relative Humidity	
RX02, operating	25° C (77° F) maximum wet bulb 2° C (36° F) minimum dew point 20% to 80% relative humidity
RX02, nonoperating	5% to 98% relative humidity (no condensation)
Media, nonoperating	10% to 80% relative humidity
Magnetic field	Media exposed to a magnetic field strength of 50 oersteds or greater may lose data.
System Reliability	
Minimum number of revolutions/track	3 million/media (head-loaded)
Seek error rate	1 in 10^6 seeks
Soft read error rate	1 in 10^9 bits read
Hard read error rate	1 in 10^{12} bits read

NOTE

The above error rates apply only to DIGITAL-approved media that is properly cared for. Seek error and soft read errors are usually attributable to random effects in the head/media interface, such as electrical noise, dirt, or dust. Both are called "soft"

errors in that the error is recoverable in ten additional tries or less. "Hard" errors cannot be recovered. Seek error retries should be preceded by an initialize.

DESCRIPTION

The interface module converts the RX02 I/O bus to the LSI-11 bus structure. It controls the RX02 interrupts to the processor, decodes device addresses for register selection, and handles the data interchange between the RX02 and the processor via DMA transfers. Power for the interface module is supplied by the LSI-11 bus.

The RXV21 floppy disk system is available in the configurations described in Table 1.

Table 1 RXV21 Configurations

System	Disk Drive	Line Voltage*
RXV21-AA	Single drive system	115V/60 Hz
RXV21-AC	Single drive system	115V/50 Hz
RXV21-AD	Single drive system	230V/50 Hz
RXV21-BA	Dual drive system	115V/60 Hz
RXV21-BC	Dual drive system	115V/50 Hz
RXV21-BD	Dual drive system	230V/50 Hz

* 50 Hz versions are available in voltages of 105, 115, 220, and 240 Vac by field-pluggable conversion.

CONFIGURATION

General

The factory jumper locations on the M8029 interface module are shown in Figure 1. All M8029 interface modules are configured and shipped with preselected register addresses and vectors as shown in Figure 2. The control/status register (RX2CS) address is 177170, and the data buffer register (RX2DB) address is 177172. The interrupt vector is 264_8. As supplied, the factory-configured jumpers are for the normal addresses used with DIGITAL software. However, in applications where more than one RXV21 system is required, appropriate register addresses and vectors may be configured by installing or removing jumpers. A second RXV21 system would normally be assigned register addresses 177200 (RX2CS) and 177202 (RX2DB), with an interrupt vector of 270_8 (Table 2).

Register Descriptions

Control/Status Register (RXCS)(177170) — The format for the RX2CS register is shown in Figure 3. Bit descriptions are presented in Table 3. Loading the RX2CS register while the RX01 is not busy and with bit 0 = 1 will initiate a function described in Table 3.

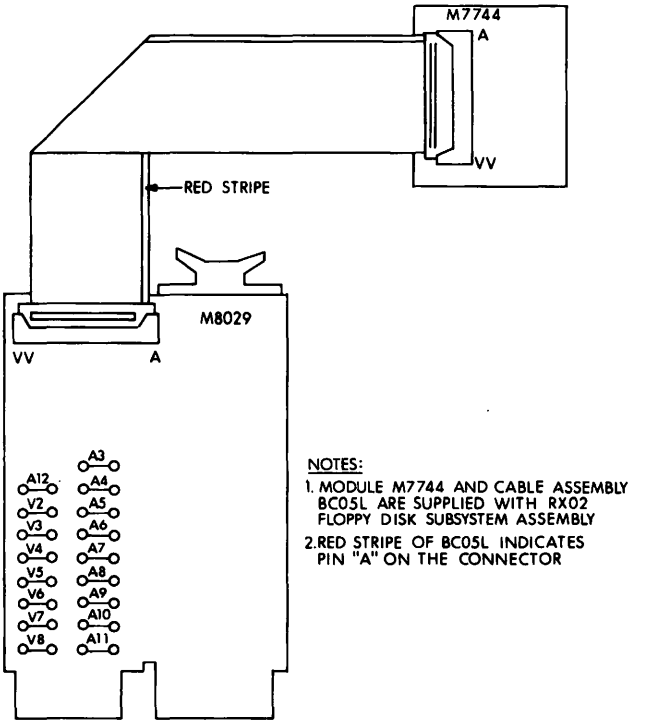


Figure 1 RXV21 Device Register and Interrupt Vector Jumper Locations

To select the standard address, the following jumpers are installed:

A12	Installed
A11	Installed
A10	Installed
A9	Installed
A8	Removed
A7	Removed
A6	Installed
A5	Installed
A4	Installed
A3	Installed

The standard Interrupt Vector is selected by installing the following jumpers:

V2	Installed
V3	Removed
V4	Installed
V5	Installed
V6	Removed
V7	Installed
V8	Installed

Figure 2 Device Register Address and Interrupt Vector

Table 2 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address	Second Module Address
Registers				
Control/ Status	RX2CS	See register description	177170	177150
Data Buffer	RX2DB		177172	177152
Interrupt				
Function Complete	Done	—	264	270

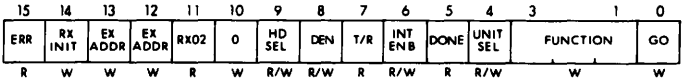


Figure 3 RXV21 Command and Status Register (RX2CS)

Table 3 RX2CS Bit Descriptions

Bit: 0 **Name:** GO
Function: Initiates a command to the RX02. Write-only.

Bit: 1-3 **Name:** Function Select
Function: These bits code one of the eight possible functions described in the Programming Specification. Write-only.

Bit: 4 **Name:** Unit Select
Function: This bit selects one of the two possible disks for execution of the desired function. This bit is readable only when DONE is set. At that time, it indicates the unit previously selected. At any other time it is not valid.

Bit: 5 **Name:** DONE
Function: Indicates the completion of a function. DONE will generate an interrupt upon being asserted if Interrupt Enable (RX2CS Bit 6) is set. Read-only.

Bit: 6 **Name:** Interrupt Enable
Function: This bit is set by the program to enable an interrupt when the RX02 has completed an operation (DONE). The condition of this bit is normally determined at the time a function is initiated. Cleared by initialize. Read/write.

Bit: 7 **Name:** Transfer Request
Function: This bit signifies that the RXV21 needs the next word in the register protocol sequence (see Programming Specification). Read-only.

Bit: 8 **Name:** Density
Function: This bit determines the density of the function to be executed. This bit is readable only when DONE is set. At that time, it indicates the density of the function previously executed. This bit is not valid at any other time.

Table 3 RX2CS Bit Descriptions (Cont)

Bit: 9 **Name:** Head Select
Function: This bit selects one of two heads for double sided operation. This bit is readable only when DONE is set. At that time, it indicates the side that was previously selected. At any other time, it is not valid.

Bit: 10 **Name:**
Function: Reserved Note: Must be written 0.

Bit: 11 **Name:** RX02
Function: This bit is set by the interface to inform the programmer that this is an RX02 system. Read-only.

Bit: 12-13 **Name:** Extended Address
Function: These bits are used to declare an extended bus address. Write-only.

Bit: 14 **Name:** RXV21 Initialize
Function: This bit is set by the program to initialize the RXV21 without initializing all of the devices on the UNIBUS.

CAUTION: Loading the lower byte of the RX2CS will also load the upper byte of the RX2CS. Upon setting this bit in the RX2CS, the RXV21 will drop DONE and move the head position mechanism of both drives (if two are available) to track zero. Upon completion of a successful initialize, the RX02 will zero error and status and set DONE. It will also read sector one of track one on drive 0. At termination, drive 0 head is at track one.

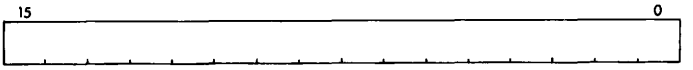
Bit: 15 **Name:** ERROR
Function: This bit is set by the RX02 to indicate that an error has occurred during an attempt to execute a command. Cleared by the initiation of a new command. Read-only.

RXV21 Data Buffer Register (RX2DB)
This register serves as a general purpose data path between the RX02 and the RXV21. It may represent one of six RX02 registers according to the protocol in progress. (See Programming Specification.) This register is read/write if the RX02 is not in the process of executing a command; it may be manipulated without affecting the RX02.

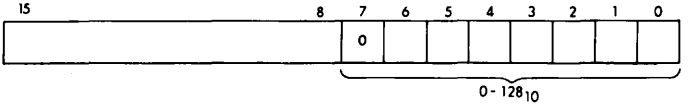
Caution

Violation of protocol in manipulation of this register may cause permanent data loss.

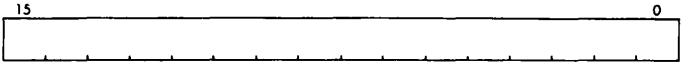
RX2DB—RXV21 Data Buffer Register



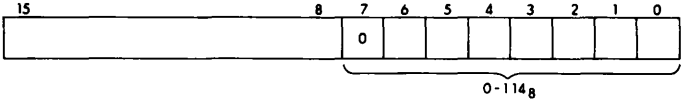
RX2WC—RXV21 Word Count Register — For a double density sector the maximum word count is 128_{10}. For a single density sector the maximum word count is 64_{10}. If a word count is beyond the limit for the density indicated, the control asserts Word Count Overflow (Bit 10 of RX2ES). Write-only register. The actual word count and *not* the 2's complement of the word count is loaded into the register.



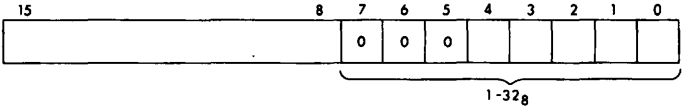
RX2BA—RXV21 Bus Address Register — This register specifies the bus address of data transferred during Fill Buffer, Empty Buffer, and Read Definitive Error operations. Incrementation takes place after a memory transaction has occurred. The RX2BA, therefore, is loaded with the address of the first data word to be transferred. This is a 16-bit write-only register (See Programming).



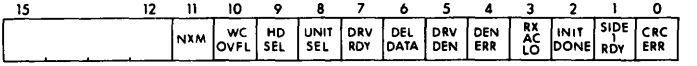
RX2CA—RXV21 Track Address Register — This is a write-only register which is loaded to indicate on which of the 77_{10} tracks a given function is to operate. It is addressed only under the protocol of the function in progress.



RX2SA—RXV21 Sector Address Register — This is a write-only register which is loaded to indicate on which of the 26_{10} sectors a given function is to operate. It can be addressed only under the protocol of the function in progress.



RX2ES—RXV21 Error and Status Register — The RX2ES is a read-only register available at the termination (DONE) of each function. The Drive Ready bit is only updated during an Initialize or Read Status function. At the termination of any other function, it reflects the drive status of the last Read Status or Initialize command.



Bit: 0 **Name:** CRC Error
Function: The cyclic redundancy check at the end of the data field has indicated an error. The data collected must be considered invalid. It is suggested that the data transfer be re-tried up to 10 times, as most data errors are recoverable (soft).

Bit: 1 **Name:** Side 1 Ready
Function: This bit, when set, indicates that a double-sided diskette is mounted in a double-sided drive and is ready to execute a function. This bit is only valid at the termination of an Initialize sequence or a Maintenance Read Status command.

Bit: 2 **Name:** Initialize Done
Function: Indicates completion of the initialize routine. Can be asserted due to: a) a RX02 power failure, B) system power failure, C) programmable or bus initialize.

Bit: 3 **Name:** RX AC LO
Function: RX power failure. Bit is set when the subsystem power is gone.

Bit: 4 **Name:** Density Error
Function: Indicates that the density of the function in progress does not match the Drive Density. Upon detection of this error, the control terminates the operation and asserts Error and Done.

Bit: 5 **Name:** Drive Density
Function: Indicates the density of the diskette mounted in the drive indicated by the Unit Select bit.

Bit: 6 **Name:** Deleted Data
Function: In the course of recovering data, the "deleted data" address mark was detected at the begining of the data field. The Drv Den bit(s) indicate whether the mark was an address mark. The data fol-

lowing the mark will be collected and transferred normally, as the deleted data mark has no further significance other than to establish drive density. Any alteration of files or actual deletion of data, due to this mark, must be accomplished by user software.

Bit: 7 **Name:** Drive Ready
Function: The selected drive is ready if Bit 7 = 1. All conditions for disk operation are satisfied, such as door closed, power OK, diskette up to speed, etc. The RX02 may be presumed to be ready to perform any operation. This bit is only valid when retrieved with a Read Status function or initialize.

Bit: 8 **Name:** Unit Select
Function: This bit indicates the drive on which the previous command was executed. This bit should agree with bit 4 of the RX2CSR for commands which require drive operation.

Bit: 9 **Name:** Reserved
Function:

Bit: 10 **Name:** Word Count Overflow
Function: The Word Count Register resides in the control. If the control senses that the word count is beyond sector size it will terminate the Fill or Empty Buffer operation and set Error and Done.

Bit: 11 **Name:** Nonexistent Memory Error
Function: This bit is set when a DMA transfer is being performed and the memory address specified in RX2BA is nonexistent (does not respond to MSYN within 10 μsec.).

PROGRAMMING
Data storage and recovery on the RXV21 occurs with careful manipulation of the two RXV21 registers (RX2CS, RX2DB) following the strict protocol of the individual function. Data may be permanently lost if the protocol is not followed. New functions given before the completion of a previous function are ignored.

Function Codes

The following is a detailed description of the programming protocol associated with each function encoded and written into bits 1-3 of RX2CS if DONE is set.

Function	Description
000	Fill Buffer
	This function is used to fill the RX02 data buffer with the number of words of data specified by the RX2WC register. "Fill Buffer" is a complete function in itself. The function ends when RX2WC overflows and, if necessary, the control has zero-filled the remainder of the buffer. The contents of the buffer may be written on the disk, by means of a subsequent Write Sector command, or returned to the host processor by an "Empty Buffer" command. To initiate this function, the RX2CS is loaded with the function. Bit 4 of the RX2CS (Unit Select) does not affect this function, since no disk operation is involved. Bit 8 (Density) must be properly selected since this determines the Word Count limit. When the command has been loaded, the DONE bit (RX2CS Bit 5) goes false. When the TR bit is asserted, the RX2WC may be loaded into the data buffer register. When TR is again asserted, the RX2BA may be loaded into the RX2DB. The data words are transferred directly from memory and DONE goes true, ending the operation, when RX2WC overflows and the control has zero-filled the remainder of the sector buffer, if necessary. If bit 6 RX2CS (Interrrupt Enable) is set, an interrupt is initiated. Any read on the RX2DB during the data transfer is ignored by the RXV21. After DONE is true, the RX2ES is located in the RX2DB register.
001	Empty Buffer
	This function is used to empty the contents of the internal buffer through the RXV21 for use by the host processor. This data is in the buffer as the result of a previous "Fill Buffer" or "Read Sector" command.
	The programming protocol for this function is identical to that for the "Fill Buffer" command. The RX2CS

is loaded with the command to initiate the function. This function will ignore bit 4 RX2CS (Unit Select). RX2CS bit 8 (Density) must be selected to allow the proper word count limit. When the command has been loaded, the DONE bit (RX2CS bit 5) goes false. When the TR bit is asserted, the RX2WC may be loaded into the RX2DB. When TR is again asserted, the RX2BA may be loaded into the RX2DB. The RXV21 assembles one word of data at a time and transfers it directly to memory. Transfers occur until Word Count overflow, at which time the operation is complete and DONE goes true. If bit 6 RX2CS (Interrupt Enable) is set, an interrupt is initiated. After DONE is true the RX2ES is located in the data buffer register.

010 Write Sector

This function is used to locate a desired sector on the diskette and fill it with the contents of the internal buffer. The initiation of the function clears RX2ES, TR, and DONE.

A. When TR is asserted, the program must load the desired Sector Address into RX2DB, which will drop TR.

   TR will remain unasserted while the RX02 attempts to locate the desired sector. The diskette density is determined at this time and is compared to the function density. If the densities do not agree, the operation is terminated; bit 4 RX2ES is set, RX2ES is moved to the RX2DB, Error (bit 15 RX2CS) is set, DONE is asserted, and an interrupt is initiated if bit 6 RX2CS (Interrupt Enable) is set.

   If the densities agree but the RX02 is unable to locate the desired sector within two diskette revolutions, the RXV21 will abort the operation, move the contents of RX2ES to the RX2DB, set ERROR (bit 15 RX2CS), assert DONE, and initiate an interrupt if Bit 6 RX2CS (Interrupt Enable) is set.

B. If the desired sector has been reached and the densities agree, the RXV21 will write the 128_{10} or 64_{10} words stored in the internal buffer followed by a CRC character which is automatically calculated by the RX02. The RXV21 ends the function by asserting DONE and if bit 6 RX2CS (Interrupt Enable) is set, initiating and interrupt.

CAUTION:

The contents of the sector buffer are not valid data after a power loss has been detected by the RX02. "Write Sector" however, will be accepted as a valid instruction and the (random) contents of the buffer will be written, followed by a valid CRC.

NOTE:

The contents of the sector buffer are not destroyed during a write sector operation.

011 Read Sector

This function is used to locate the desired sector and transfer the contents of the data field to the internal buffer in the control. This function may also be used to rapidly retrieve (5 ms) the current status of the drive selected. The initiation of this function clears RX2ES, TR, and DONE.

A. When TR is asserted, the program must load the desired Sector Address into the RX2DB, which will drop TR. When TR is again asserted, the program must load the desired Cynlinder Address into the RX2DB, which will drop TR.

   TR and DONE will remain unasserted while the RX02 attempts to locate the desired sector. If the RX02 is unable to locate the desired sector within two diskette revolutions for any reason, the RXV21 will abort the operation, set DONE and ERROR (Bit 15 RX2CS), move the contents of the RX2ES to the RX2DB, and if Bit 6 RX2CS (Interrupt Enable) is set, initiate an interrupt.

B. If the desired sector is successfully located, the control reads the data address mark and determines the density of the diskette. If the diskette (drive) density does not agree with the function

density, the operation is terminated and DONE and ERROR (bit 15 RX2CS) are asserted. Bit 4 RX2ES is set (Density Error) and the RX2ES is moved to the RX2DB. If Bit 6 RX2CS (Interrupt Enable) is set, an interrupt is initiated.

D. If the desired sector is successfully located, the densities agree, and the data are transferred with no CRC error, DONE will be set and if Bit 6 RX2CS (Interrupt Enable) is set, the RXV21 initiates an interrupt.

100 Set Media Density

This function causes the entire diskette to be reassigned to a new density. Bit 8 RX2CS (Density) indicates the new density. The control reformats the diskette by writing new data address marks (double or single density) and zeroing out all of the data fields on the diskette.

The function is initiated by loading the RX2CS with the command. Initiation of the function clears RX2ES and DONE. When TR is set, an ASCII "I" (111) must be loaded into the RX2DB to complete the protocol. This extra character is a safeguard against an error in loading the command. When the control recognizes this character it begins executing the command.

The control starts at Sector 1, Track 0 and reads the header information, then starts a write operation. If the header information is damaged, the control will abort the operation.

If the operation is successfully completed, DONE is set and if Bit 6 RX2CS (Interrupt Enable) is set, an interrupt is initiated.

NOTE:

If double-sided media is mounted in a double-sided drive, both sides are set to the same density automatically.

CAUTION:

This operation takes about 15 seconds and should not be interrupted. If for any reason the operation is interrupted, an illegal diskette has been generated which may have data marks of both densities. This diskette should again be completely reformatted.

101 Maintenance Read Status

This function is initiated by loading the RX2CS with the command. DONE is cleared. The Drive Ready bit (Bit 7 RX2ES) is updated by counting index pulses in the control. The Drive Density is updated by loading the head of the selected drive and reading the first data mark. All other RX2ES bits reflect the conditions created by the last command. During this function, in addition to status, the control performs the wraparound mode in the device electronics. If an error occurs while wrapping the data from the Sector Buffer through the device electronics, the Error bit (Bit 15 RX2CS) is set. The RX2ES is moved into the RX2DB. The RX2CS may be sampled when DONE (Bit 5 RX2CS) is again asserted and if Bit RX2CS (Interrupt Enable) is set, an interrupt will occur. This operation requires approximately 250 msec to complete.

NOTE:

If double-sided media is mounted in a double-sided drive, the Side 1 Ready bit (RX2ES bit 1) is set.

110 Write Sector With Deleted Data

This operation is identical to function 011 (Write Sector) with the exception that a deleted data address mark is written preceding the data rather than the standard data address mark. The Density bit associated with the function indicates whether a single or double density deleted data address mark will be written.

111 Read Error Code

The Read Error Code function implies a read extended status. In addition to the specific Error code, a dump of the control's internal scratch pad registers

also occurs. This is the only way that the Word Count Register can be retrieved. This function is used to retrieve specific information as well, as drive status information, depending on detection of the general ERROR BIT.

The transfer of the registers is a DMA transfer. The function is initiated by loading the RX2CS with the command. DONE goes false. When TR is true, the RX2BA may be loaded into the RX2DB and TR goes false. The registers are assembled one word at a time and transferred directly to memory.

Following is the Register Protocol.

NOTE:

The Density bit (bit 8 RX2CS) must be loaded with the function. If the wrong assumption was made, an error is returned.

Following is the Register Protocol.

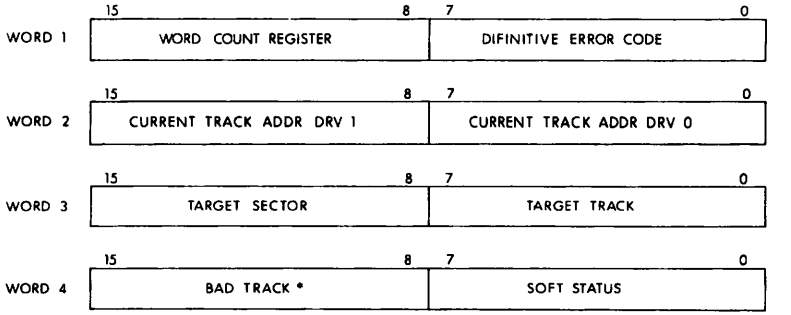


Table 4 Definitive Error Codes

10	DRIVE 0 FAILED TO SEE HOME ON INITIALIZE
20	DRIVE 1 FAILED TO SEE HOME ON INITIALIZE
40	TRIED TO ACCESS A TRACK GREATER THAN 76
50	HOME WAS FOUND BEFORE DESIRED TRACK WAS REACHED

Table 4 Definitive Error Codes (Cont)

70	DESIRED SECTOR COULD NOT BE FOUND AFTER 52 TRIES
110	MORE THAN 40 MICROSECONDS AND NO SEP CLOCK SEEN
120	A PREAMBLE COULD NOT BE FOUND
130	A PREAMBLE FOUND BUT NO ID MARK FOUND WITHIN ALLOWABLE TIME
150	THE TRACK ADDRESS OF A GOOD HEADER DOES NOT COMPARE WITH DESIRED TRACK
160	TOO MANY TRIES FOR IDAM
170	DATA ARE NOT FOUND IN ALLOTTED TIME
200	CRC ON READING THE SECTOR FROM THE DISK
220	FAILED MAINTENANCE WRAPAROUND CHECK
230	WORD COUNT OVERFLOW
240	DENSITY ERROR
250	INCORRECT KEY WORD ON SET DENSITY COMMAND

RX02 Power Fail or Initialize

When the RX02 control senses a loss of power within the RX02, it will unload the head and abort all controller action. The RXAC L line is asserted to indicate to the RXV21 that subsystem power is gone. The RXV21 asserts DONE and ERROR and sets the RXAC L bit in the RX2ES.*

When the RX02 senses the return of power, it will remove DONE and begin a sequence to:

1. Move each drive head position mechanism to track 00
2. Clear any active error bits
3. Read sector 1 of track 1, on drive 0
4. Assert Initialize DONE in the RXES

Upon completion of the power-up sequence, DONE is again asserted. There is no guarantee that information being written at the time of a power failure will be retrievable; however, all other information on the diskette will remain unaltered.

LSI-11 Bus Power Fail

When the BPOK H line is negated by the LSI-11, the RXV21 asserts the Initialize line and holds it asserted. The RX02 control unloads the head and aborts controller action as detailed above. When LSI-11 power is restored, the above power-up sequence is started.

* This is the only valid bit in the RX2ES at this time.

Programming Examples for Typical Operation

Disk Write

A typical disk write sequence, which is initiated by the user program, would occur in two steps.

Fill Buffer—A command to fill the buffer is moved into the RX2CS. The GO bit must be set. The program tests for TR. When TR is detected, the program moves the desired word count into the RX2DB. TR goes false while the word count is moved to the RX02. The program retests TR and moves the Bus Address into the RX2DB. The device now requests bus mastership and DMA's one data word at a time into the RX2DB and shifts it across the RX02 data bus bit serially one 8 bit byte at a time into the sector buffer. When the Word Count Register overflows and, if necessary, the RX02 control zero fills the remainder of the sector buffer, the DONE bit is set and an interrupt will occur if the program has enabled interrupts.

Write Sector—A command to write the contents of the sector buffer onto the disk is moved into the RX2CS. The program tests TR and when TR is set, moves the desired sector address to the RX2DB. TR remains false while the sector address is shifted to the RX02 control. The control retests TR and when it is again set, moves the desired track address register to the RX2DB. Again TR is negated. The RX02 locates the desired track and sector and compares the diskette density against the assigned function density and writes the contents of the sector buffer onto the disk if the densities agree. When the write operation is completed, the DONE bit is set and an interrupt will occur if the program has enabled interrupts.

Disk Read

A typical disk read operation occurs in the reverse order. First, the desired track and sector are located and the contents of the sector are read into the sector buffer (Read Sector). Then, the contents of the sector buffer are unloaded into memory (Empty Buffer). In either case, the contents of the sector buffer are not valid if either a Power Fail or Initialize follows a Fill Buffer or Read Sector function.

BOOTSTRAPPING THE RXV21

The RXV21 bootstrap loader program loads the system monitor from disk into system memory. No system operation can occur until the monitor is contained in system memory. Bootstrapping ("booting") the system can be accomplished via a hardware-implemented bootstrap in the BDV11 optiion, the MXV11-A with MXV11-A2 boot chips, or it can be entered and executed via the console device.

The following bootstraps are entered under microcode ODT. The bootable volume must be in drive zero. All devices are at standard addresses and vectors. Enter the code starting at location 1000. Inhibit all interrupts by entering RS/__340 <CR>. Initialize the program counter by entering R7/__1000 <CR>. After the code has been entered, type P.

	RX02 DOUBLE DENSITY	RX02 SINGLE DENSITY
LOCATION	CODE	CODE
1000	12700	12700
1002	100240	100240
1004	12701	12701
1006	177170	177170
1010	5002	5002
1012	12705	12705
1014	200	100
1016	12704	12704
1020	401	401
1022	12703	12703
1024	177172	177172
1026	30011	30011
1030	1776	1776
1032	100437	100437
1034	12711	12711
1036	407	7
1040	30011	30011
1042	1776	1776
1044	100432	100432
1046	110413	110413

RXV21

LOCATION	RX02 DOUBLE DENSITY CODE	RX02 SINGLE DENSITY CODE
1050	304	304
1052	30011	30011
1054	1776	1776
1056	110413	110413
1060	304	304
1062	30011	30011
1064	1776	1776
1066	100421	100421
1070	12711	12711
1072	403	3
1074	30011	30011
1076	1776	1776
1100	00414	100414
1102	10513	10513
1104	30011	30011
1106	1776	1776
1110	100410	100410
1112	10213	10213
1114	60502	60502
1116	60502	60502
1120	122424	122424
1122	120427	120427
1124	3	7
1126	3735	3735
1130	12700	12700
1132	0	0
1134	5007	5007
1136	0	0

TEV11 TERMINATOR

GENERAL

The TEV11 terminator module provides 120-ohm termination circuits as shown in Figure 1.

FEATURES

SPECIFICATIONS

Identification	M9400-YB
Size	Double
Power	+5 Vdc ± 5% at 0.54A
Bus Loads	0
AC	0
DC	

DESCRIPTION

General

Each bus signal line terminates with two resistors as shown in Figure 2. These termination resistors are generally contained in a 16-pin, dual-in-line package which is identical to an IC package. Each package contains 14 termination pairs. The values used are shown in the figure. Daisy-chained grant signals are terminated and jumpered. BIAKI L is jumpered to BIAKO L and BDMGI L is connected to BDMGO L via factory-installed jumper W1.

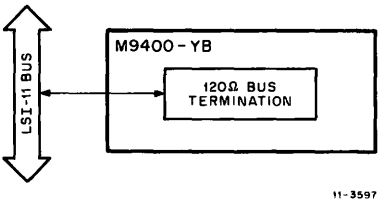


Figure 1 TEV11 Functions

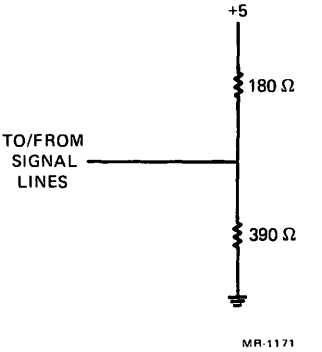


Figure 2 Typical 120-Ohm Bus Termination

TU58 CARTRIDGE TAPE DRIVE

GENERAL

The TU58 is a low-cost intelligent mass memory device that offers random access to block-formatted data on pocket-size cartridge media. It is ideal as a small computer systems device, as inexpensive archive mass storage, or as a software update distribution medium. A dual drive TU58 offers 512 Kb of storage space, making it one of the lowest cost complete mass storage subsystems available.

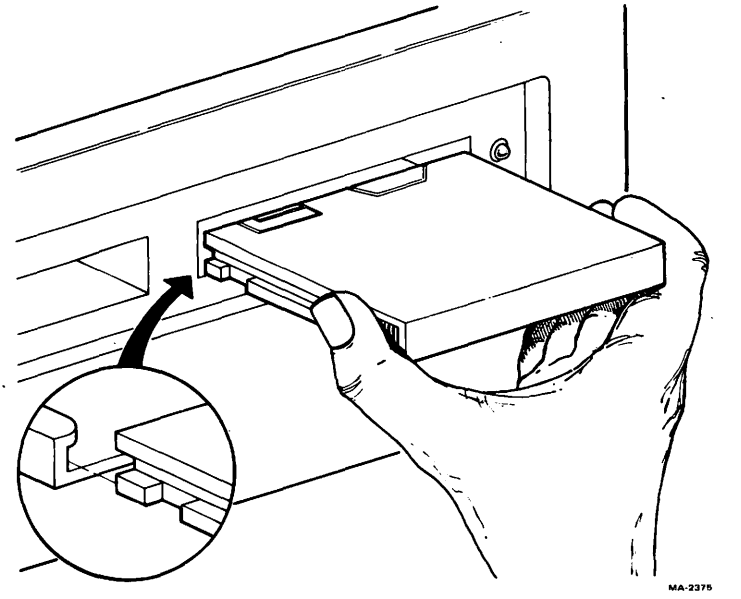


Figure 1 Loading a Cartridge

TU58

FEATURES

- 512 Kb per dual drive subsystem
- RS422, RS423, and RC232-C serial line I/O
- Reliable 30 inches per second read/write tape speed combined with 60 inches per second bidirectional search speed
- Flexible baud rates from 150 to 38,400
- Complete tape subsystem on one P.C. module for compact mounting
- Microprocessor-based subsystem with automatic soft-error recovery via rereads.

SPECIFICATIONS

Performance

Capacity per cartridge	262,144 bytes, formatted in 512 blocks of 512 bytes each
Data reliability	
Soft data error rate	1 in 10^7 bits read (before self-correction)
Hard error rate	1 in 10^9 bits read (unrecoverable within eight automatic retries)
Hard error rate with write verify and system correction	2 in 10^{11} bits read/written
Error checking	Checksum with rotation
Average access time	9.3 seconds
Maximum access time	28 seconds
Read/write tape speed	76 cm/s (30 ips)
Search tape speed	152 cm/s (60 ips)
Bit density	315 bits/cm (800 bits/in.)
Flux reversal density	945 fr/cm (2400 fr/in.)
Recording method	Ratio encoding
Medium	DECtape II cartridge with 42.7 m (140 ft.) of 3.81 mm (0.150 in.) tape Size: 6.1 × 8.1 × 1.3 cm (2.4 × 3.2 × 0.5 in.)

TU58

Track format	Two tracks, each containing 1024 individually numbered, firmware-interleaved "records." Firmware manipulates four records at each operation to form 512-byte blocks.
Drive	Single motor, head integrally cast into molded chassis.
Drives per controller	1 or 2. Only one may operate at a time.

Electrical

Power consumption	
Module and 1 or 2 drives	11 W, typical, drive running +5V ±5% at 0.75A, maximum +12V + 10% −5% at 1.2A, peak 0.6A average running 0.1A idle
Serial interface standards	In accordance with RS422 or RS423; compatible with RS232-C.

Mechanical

Drive	8.1 H × 8.3 D × 10.6 W cm (3.2 × 3.3 × 4.1 in.) with 19 cm (7.5 in.) cable 0.23 Kg (0.516 lbs.)
Board (Module)	13.2 H × 26.5 D × 3.5 W cm (5.19 × 10.44 × 1.4 in.) 0.24 Kg (0.5316 lbs.)
Power connector to module	AMP 87159-6 with 87027-3 contacts (DEC part nos. 12-12202-09, 12-12203-00)
Interface connector to module	AMP 87133-5 with 87124-1 locking clip contacts and 87179-1 index pin (DEC part nos. 12-14268-02, 12-14267-00, 12-15418-00)

Environmental

Maximum dissipation

TU58-AB, TU58-BB	34 Btu/hour
Temperature	
TU58-AB,BB operating	15°C (59°F) to 4 °C (108°F)
TU58-AB,BB nonoperating	−34°C (−30°F) to 60°C (140°F)
Medium operating temperature	0°C (32°F) to 50°C (122°F)
Maximum temperature difference between system ambient and TU58 module	18°C (32.4°F)
Relative Humidity, noncondensing	
TU58 operating	
Maximum wet bulb	26°C (79°F)
Minimum dew point	2°C (36°F)
Relative humidity	20% to 98%
TU58 nonoperating	5% to 98%
Medium nonoperating	10% to 80%

DESCRIPTION

General

The tape cartridges are DIGITAL preformatted miniature reel-to-reel packages containing 42.7 m (140 ft.) of 3.81 mm (0.15 in.) wide tape. The tape is driven by a single puck which engages a roller which moves an elastomer drive belt in the cartridge. This belt loops around both tape spools and provides uniform tension and spill-free winding without mechanical linkages (Figure 1). The simple single-point drive mechanism allows high reliability for the entire system.

The control and drive circuitry of the TU58 is located on a single circuit board. The motor, tape head control, driver, and switching circuits to manage the tape drives are located on the printed circuit board along with the subsystem's microprocessor. Operational amplifiers, comparators, and logic circuits perform amplification, signal switching and

conditioning, proportional control, and logic steering functions in the controller. The tape is protected by motor current limiting and an anti-runaway timer. Although the controller supports one or two drives, only one drive can operate at a time. Head selection and motor selection, speed and direction changes, etc., are managed by outputs from I/O ports on a peripheral IC. The mechanical actions of the drives themselves are supervised by the microprocessor to improve the system's performance.

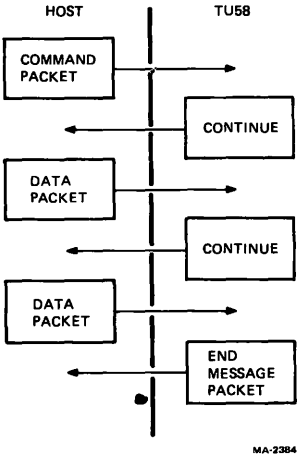


Figure 2 An Exchange in Radial Serial Protocol

Because of the microprocessor intelligence, requests from the host for data retrieval or storage need only contain simple specifications about the transfer. The controller positions the tape and performs the transfer without supervision from the host.

The host and controller communicate in a format called Radial Serial Protocol (RSP). The RSP uses two kinds of byte sequences called message packets. Both commands and data packets have protocol information placed in specific locations in the byte sequence. This format is easily generated by the TU58, making host-peripheral interaction possible at a high level with low cost.

Figure 2 illustrates a typical RSP exchange between a host computer and the TU58.

The serial host interface operates on full-duplex, asynchronous 4-wire lines at jumper-selectable rates from 150 to 38,400 baud. The send and receive rates may be independently set with jumpers to operate in accordance with Electronic Industries Association (EIA) Standards RS422 or RS423. When set to RS423, the TU58 is also compatible with devices complying with RS232-C.

Figure 3 illustrates the structure of the TU58 system. The data path is along the top of the diagram, passing to the host through the processor at the right. The drive control is at the lower left, also closely associated with the processor through the I/O ports. The ports, memory, and universal asynchronous receiver-transmitter (UART) are tied to the processor by an 8-bit-wide data/address bus.

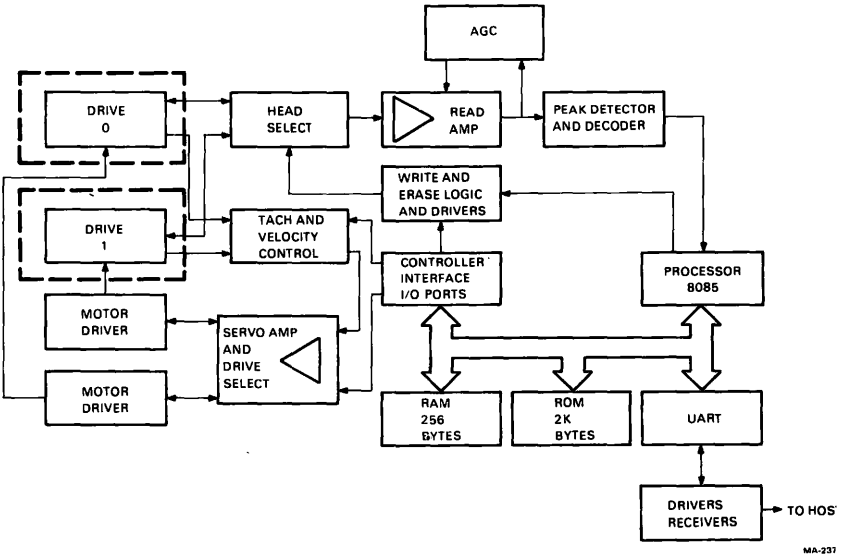


Figure 3 TU58 Block Diagram

The cartridge drive motors are powered by servo-regulated speed and direction circuits. These are controlled by the processor, which monitors with tachometers and with signals from the tape. The heads are selected by processor-controlled switches and either feed the automatic-gain-controlled (AGC) read amplifier and decoder circuits or are driven by write currents encoded by the processor.

The processor consists of an 8085 processor supported by firmware in a 2 Kb read-only memory (ROM) and by scratchpad and data buffer memory in a 256-byte random access memory (RAM). The processor communicates with the drive control circuitry through a bidirectional I/O port. The UART exchanges data between the TU58 processor bus and the host computer via the serial line drivers and receivers.

CONFIGURATION

The TU58 is available in the following configurations with accompanying designations:

Components

TU58-AB	Serial interface controller module, surface mounting, with one drive.
TU58-BB	Serial interface controller module, surface mounting, with two drives.

Additional Supplies

TU58-K preformatted tape cartridges.
TUC-01 Tape Drive Cleaning Kit.

OPERATION

The TU58 may be supplied with power from a host system. It is ready for operation within 1 second of voltage stabilization. It does not need to be turned off when not in use; its idling power consumption is less than 5 W.

When power is applied, the TU58 initializes itself, performs its internal diagnostic tests, and then asks the host for an acknowledgement before it settles down to wait for instructions. Refer to the Programming section for a description of the required exchange.

If power is removed while a tape is being written, data may be lost, but there are no other restrictions on power removal.

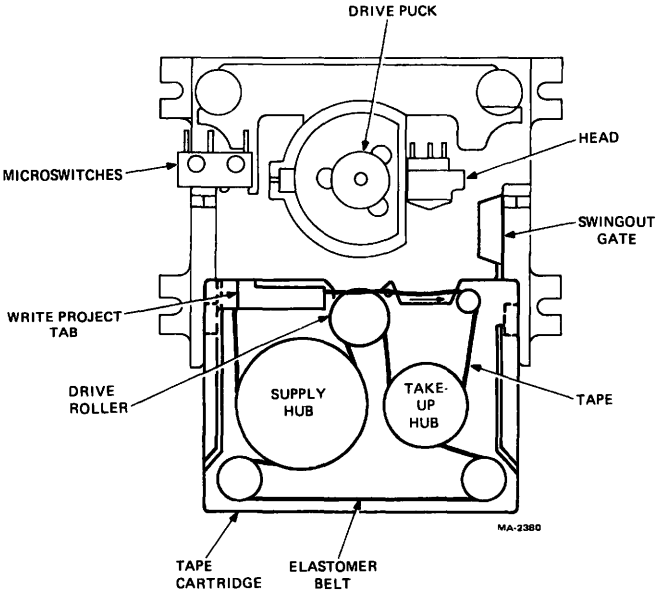


Figure 5 Tape Cartridge Partially Inserted Into Drive

Cartridge Loading

The TU58 drive is designed to make correct loading easy. To load the cartridge, hold it label-up, line it up with the grooves in the chassis, and slide it in with a firm push. Figure 1 illustrates the fit of the cartridge into the drive chassis grooves.

Cartridge Unloading

Unloading the cartridge is as simple as loading. Just pull it straight out. It is best to wait for the tape to stop, as indicated by the run light, before removing the cartridge. The mechanism cannot be damaged by removing the cartridge while the tape is moving, but if a write is in progress, data may be lost. An error message will be sent to the host if a command is interrupted by removal of a cartridge.

Keeping Track of Cartridges

If the TU58 is used in a non-file-structured system, the cartridge does not have an identifying number or label recorded on the tape. If a cartridge is changed, the TU58 will not know that a different cartridge was loaded; the operator must keep track of the contents of various cartridges.

Write Protect Tab

Each tape cartridge has a movable tab which, when properly positioned, protects data on the tape from unintended write operations. When this write protect tab (Figure 6) is in the inner position (toward the drive roller), it locks out the write circuity.

When the write protect tab is in the outer position, it closes a switch in the chassis and allows the controller to write when it is commanded to. The operator should be sure that system or program tapes are backed up with copies before loading them into the TU58 with their write protect tabs set to record.

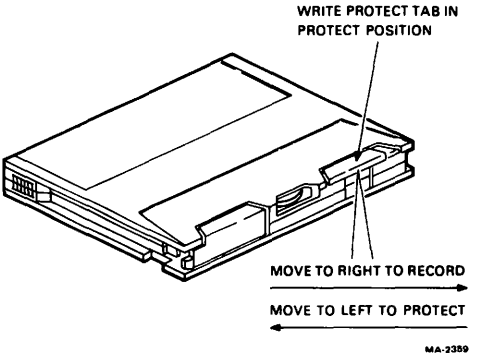


Figure 6 Write Protect Tab

Cartridge Storage and Care

Store cartridges in their cases, away from dust and heat or direct sunlight. Do not touch the tape; there is no safe way to clean the tape and permanent errors may result. Keep tools and other ferrous or magnetic objects away. If a tape is suspected of having been exposed to environmental extremes as listed in the specifications and if the software operating system permits, wind it all the way through by requesting positioning to blocks at each end of the tape before attempting to store data on the cartridge.

MAINTENANCE

Head and Puck Cleaning

After 100 hours of tape running time or semi-annually, clean the head and motor puck with a long handled cotton applicator moistened with DEC cleaning fluid (from cleaning kit TUC-01), 95 percent isopropyl alcohol, fluorocarbon TF, 113 or equivalent (Figure 7). Push the puck around with the applicator to clean its entire surface. Regular cleaning minimizes tape and head wear and prevent tape damage and data errors caused by contamination. A new drive requires head cleaning after the first 20 hours of actual use. After this initial cleaning, 100 hour intervals are adequate. This is the only regular maintenance required for the TU58.

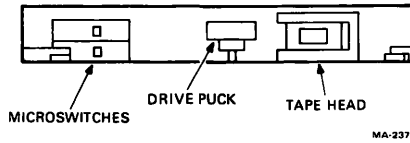


Figure 7 View Into Tape Drive Cartridge Slot

PROGRAMMING

The TU58 is controlled by a high-level command set that relieves the host computer of device-related operations such as tape positioning and read retries. The TU58 firmware contains subroutines that are activated by brief strings of command bytes. The command strings contain the numerical code for the operation to be performed and the location and size of data files that are to be transferred, when applicable. They also contain various housekeeping characters that are part of the Radial Serial Protocol (RSP) under which the byte sequences are defined. The byte sequences are called message packets and are designed to be transmitted by asynchronous interfaces.

Block Number, Byte Count, and Drive Number

The TU58 uses the block number and byte count to write or retrieve data. If all of the desired data is contained within a single 512-byte block, the byte count will be 512 or less. When the host asks for a particular block and a 512-or-less byte count, the TU58 will position the specified drive (unit) at that block and transfer the number of bytes specified. If the host asks for a block and also a byte count greater

than that of the 512-byte boundary, the TU58 will read as many sequential blocks as are needed to fulfill the byte count. The same process applies to the write function. This means that the host software or an on-tape file directory need only store the number of the first block in a file and the file's byte count to read or write all the data without having to know the additional block numbers.

Special Handler Functions

Some device-related functions are not dealt with directly in the RSP or in the TU58 firmware.

A TU58 handler should check the success code (byte 3 of the RSP end message) for the presence of soft errors. This enables action to be taken before hard errors (permanent data losses) occur. For example, if the number of retries on a particular cartridge reaches some value, a message like "Tape Maintenance Required" could be presented to the operator. This would suggest that prompt tape copying and head cleaning is in order.

RADIAL SERIAL PROTOCOL (RSP)

Message Packets

All communication between the TU58 and the host is divided into message packets, which are groups of bytes arranged in fixed order. Position within the packet determines the meaning of each byte. There are three kinds of message packets: command, data, and end messages. The end message is a special case of the command packet. In addition, there are three single-byte protocol management messages: INIT, Continue, and XOFF.

Each packet begins with a flag byte, which announces its contents. The next byte in a message packet is the byte count. This is the number of message characters in the packet, excluding the flag, byte count, and checksum. Up to 128 message bytes may be in each packet. Larger blocks of data are sent with multiple packets. The last two byte pairs of the message packet are a 16-bit checksum. The checksum is formed by summing sucessive byte pairs taken as 16-bit words and using an end-around carry from bit 15 to bit 0. The flag and byte count are included in the checksum.

Flag Byte Op Codes

Bits 7-5 of the op code are reserved.

01_8	00001	Data
02_8	00010	Control (command)
04_8	00100	INIT
10_8	01000	Bootstrap
20_8	10000	Continue
23_8	10011	XOFF

Data — This flag informs the receiver that data rather than commands are arriving. The receiver loads the incoming bytes into a buffer area in memory. It does not look for an op code to execute.

Command — The command flag informs the TU58 that a command packet follows. An instruction code will be in this packet. The flag is particularly important when the TU58 encounters an error condition. In this case, it sends an end packet before data transfer is complete. The host knows that the end packet has been sent because the packet received has a command flag instead of a data flag.

INIT — This op code is sent from the host to cause the TU58 to execute its power-up sequence. The TU58 returns Continue after completion. It is sent from the TU58 to the host to indicate that the power-up sequence has occurred. When the TU58 makes a protocol error or receives an invalid command, it reinitializes and send INIT continuously to the host. When the host recognizes INIT, it send Break to the TU58 to restore the protocol.

Bootstrap — A flagbyte saying Bootstrap (octal 10), followed by a byte containing a drive number, causes the TU58 to read block 0 of the selected drive. It returns the 512 bytes without radial serial packaging. This simplifies bootstrap operations. Bootstrap may be sent by the host instead of a second INIT as part of the initialization process described below.

Continue	After a message is sent from host to the TU58, the host must wait until the TU58 sends Continue before any more messages can be sent. This permits the TU58 to control the flow of data.
XOFF	Ordinarily, the TU58 does not have to wait between messages to the host. However, if the host is unable to receive all of a message from the peripheral at once, it may send XOFF. The TU58 stops transmitting immediately and waits until the host sends Continue to complete the transfer when it is ready. (Two characters may be sent by the UART to the host after the TU58 receives XOFF).

Break and Initialization

Break is a unique logic entity that can be interpreted by the TU58 and the host regardless of the state of the protocol. Break is transmitted when the serial line, which normally switches between two logic states called mark and space, is kept in the "space" condition for more than one character time. This causes the TU58's UART to set its framing error bit. The TU58 will interpret the framing error as break.

Break has two applications in the TU58: one is routinely used, and the other is for special conditions. When the TU58 is powered up, it performs its internal checkout and initialization and then transmits INITs continuously to the host to inform the host that it is present. The host acknowledges the TU58 by sending break for a minimum of one character time, and then sending two INITs. The TU58 responds with Continue and enters an idle state in which it will wait for further instructions.

If communications break down, due to any transient problem, the host may restore order by sending break and INIT as outlined above. Whatever faulty operations were underway will be cancelled, and the TU58 will reinitialize itself, return Continue, and wait for instructions.

With DIGITAL serial interfaces, the initialize sequence may be sent by the following sequence of operations. Set the break in the transmit control status register, then send two null characters. When the transmit ready flag is set again, remove the break bit. This will time Break to be one character time long. The second character will be discarded by the TU58 controller. Next, send two INIT characters. The first will be discarded by the TU58. The TU58 will respond to the second INIT by sending Continue. When Continue has been received, the initialize sequence is complete and any command packet may follow.

COMMAND SET

The command set for the TU58 provides capabilities for random access operations. To allow for future development, certain op codes in the command set have been reserved; these commands have unpredictable results and should not be used. Op codes not listed in the command set are illegal and result in the return of an end packet with the "bad op code" success code.

A data transfer operation uses three or more message packets. The first packet is the command packet from host to the TU58. Next, the data is transferred in 128-byte packets in either direction (as required by read or write). After all data is transferred, the TU58 sends an end packet. If the TU58 encounters a failure before all data has been transferred, it sends the end packet as soon as the failure occurs.

Command Packets

The command packet format is shown in Table 1. Bytes 0, 1, 12, and 13 are the message delivery bytes. Their definitions are as follows.

Table 1 Command Packet Structure

Byte	Byte Contents
0	Flag = 0000 0010 (02_8)
1	Message Byte Count = 0000 1010 (12_8)
2	Op Code
3	Modifier
4	Unit Number
5	Switches
6	Sequence Number—Low
7	Sequence Number—High
8	Byte Count—Low
9	Byte Count—High
10	Block Number—Low
11	Block Number—High
12	Checksum—Low
13	Checksum—High

0	Flag	This byte is set to 00000010 to indicate that the packet is a Command packet.

1	Message Byte Count	Number of bytes in the packet excluding the four message delivery bytes. This is decimal 10 for all command packets.
12, 13	Checksum	The 16-bit checksum of bytes 0 through 11. The checksum is formed by treating each pair of bytes as a word and summing words with end-around carry.

The remaining bytes are defined as follows.

2	Op Code	Operation being commanded. Refer to Table 2 for definitions.
3	Modifier	Permits variations of commands.
4	Unit Number	Selects drive 0 or 1.
5	Switches	Selects maintenance mode.
6, 7	Sequence Number	Always zero for TU58.
8, 9	Byte Count	Number of bytes to be transferred by a read or write command. Ignored by other commands.
10, 11	Block Number	The block number to be used by commands requiring tape positioning.

Table 2 Instruction Set

Decimal	Op Code Octal	Op Code Instruction
0	0	NOP
1	1	INIT
2	2	Read
3	3	Write
4	4	(Reserved)
5	5	Position
6	6	(Reserved)
7	7	Diagnose
8	10	Get Status
9	11	Set Status
10	12	(Reserved)
11	13	(Reserved)

Maintenance Mode — Setting bit 4 of the switches byte (byte 5) to 1 in a read command inhibits retries on data errors. Instead, the incorrect data is delivered to the host followed by an end packet. The success code in the end packet indicates a hard data error. Since data is transmitted in 128-byte packets, a multiple packet read progresses normally until a checksum mismatch occurs. Then the bad packet is transmitted, followed by the end packet, and the operation terminates.

Special Address Mode — Setting the most significant bit of the modifier byte to 1 selects special address mode. In this mode, all tape positioning operations are addressed by 128-byte blocks (0-2047) instead of 512-byte blocks (0-511). Zero-fill in a write operation only fills out to a 128-byte boundary in this mode.

Data Packets

The data packet is shown in Table 3. The flag byte is set to 00000001. The number of data bytes may be between 1 and 128 bytes. For data transfers larger than 128 bytes, the transaction is broken up and sent 128 bytes at a time. The host is assumed to have enough buffer capacity to accept the entire transaction, whereas the TU58 only has 128 bytes of buffer space. For write commands, the host must wait between message packets for the TU58 to send the Continue flag (00010000) before sending the next packet. Since the host has enough buffer space, the TU58 does not wait for a continue flag between message packets when it sends back read data.

Table 3 Data Packets

Byte	Byte Contents
0	Flag = 0000 001
1	Byte Count = M
2	First Data Byte
3	Data
.	.
.	.
.	.
M	Data
M+1	Last Data Byte
M+2	Checksum L
M+3	Checksum H

End Packets

The end packet is sent to the host by the TU58 after completion or termination of an operation or on an error. The end packet is shown in Table 4. The definition of bytes 0, 1, 12, and 13 are the same as for the command packet. The remaining bytes are defined as follows.

Byte 2		Op Code—0100 0000 for end packet
Byte 3	Octal	Success Code
	0	−0 = Normal
	1	−1 = Success but with Retries
	377	−1 = Failed Self-Test
	376	−2 = Partial Operation (End of Medium)
	370	−8 = Bad Unit Number
	367	−9 = No Cartridge
	365	−11 = Write Protected
	357	−17 = Data Check Error
	340	−32 = Seek Error (Block Not Found)
	337	−33 = Motor Stopped
	320	−48 = Bad Op Code
	311	−55 = Bad Block Number (i.e., > 511)
Byte 4		Unit Number 0 or 1 for Drive Number
Byte 5		Always 0

Bytes 6, 7 — Sequence Number — always 0 as in command packet

Bytes 8, 9 — Actual Byte Count — number of bytes handled in transaction. In a good operation, this will be the same as the data byte count in the command packet.

Bytes 10, 11 — Summary Status

Byte 10
Bit 0

Byte 11 Reserved
Bit 0
1
2
3
4 Logic Error
5 Motion Error
6 Transfer Error
7 Special Condition (Errors)

Table 4 End Packet

Byte	Byte Contents
0	Flag = 0000 0010
1	Byte Count = 0000 1010
2	Op Code = 0100 0000
3	Success Code
4	Unit
5	Not Used
6	Sequence No. L
7	Sequence No. H
8	Actual Byte Count L
9	Actual Byte Count H
10	Summary Status L
11	Summary Status H
12	Checksum L
13	Checksum H

THE INSTRUCTION SET

The instructions and their op codes are shown in Table 2. The following is a brief description and usage example of each.

OP CODE 0 NOP

This instruction causes the TU58 to return an end packet. There are no modifiers to NOP. The NOP packet is shown below.

BYTE				
0	0000	0010	FLAG	
1	0000	1010	MESSAGE BYTE CNT	
2	0000	0000	OP CODE	
3	0000	0000	MODIFIER	
4	0000	000X	UNIT NUMBER (IGNORED)	
5	0000	0000	SWITCHES (NOT USED)	
6	0000	0000	SEQ NO.	
7	0000	0000	SEQ NO. NOT USED	
8	0000	0000	BYTE COUNT L	NO DATA
9	0000	0000	BYTE COUNT H	INVOLVED
10	0000	0000	BLOCK NO. L	NO TAPE
11	0000	0000	BLOCK NO. H	POSITION
12	0000	001X	CHECKSUM L	
13	0000	1010	CHECKSUM H	

The TU58 returns the following end packet.

0	0000	0010	FLAG	
1	0000	1010	MESSAGE BYTE CNT	
2	0100	0000	OP CODE	
3	0000	0000	SUCCESS CODE	
4	0000	000X	UNIT NUMBER (IGNORED)	
5	0000	0000	NOT USED	
6	0000	0000	SEQ. L	
7	0000	0000	SEQ. H NOT USED	
8	0000	0000	ACTUAL BYTE CNTL	NO DATA
9	0000	0000	ACTUAL BYTE CNTH	INVOLVED
10	0000	0000	SUMMARY STATUS L	
11	XXXX	XXXX	SUMMARY STATUS H	
12	000X	XXXX	CHECKSUM L	
13	XXXX	XXXX	CHECKSUM H	

OP CODE 1 INIT

This instruction causes the TU58 controller to reset itself to a ready state. No tape positioning results from this operation. The command packet is the same as for NOP except for the op code and the resultant change to the low order checksum byte. The TU58 sends the same end packet as for NOP after reinitializing itself. There are no modifiers to INIT.

OP CODE 2 Read, and Read with Increased Threshold

This instruction causes the TU58 to position the tape in the drive selected by Unit Number to the block designated by the block number bytes. It reads data starting at the designated block and continues reading until the byte count (command bytes 8 and 9) is satisfied. After data has been sent, the TU58 sends an end packet. Byte 3 indicates success, success with retries, or failure of the operation. In the event of failure, the end packet is sent all the time of failure without filling up the data count. The end packet will be recognized by the host by the flag byte. The host will see a command flag (0000 0010) instead of a data flag (0000 0001).

There is one modifier to the read command. A modifier of 0000 0001 causes the TU58 to read the tape with an increased threshold in the data recovery circuit. This makes the tape drop bits if any weak spots are present. Thus, if the TU58 can read error-free in this mode, the data is healthy. The read transaction between TU58 and host is shown in Figure 8.

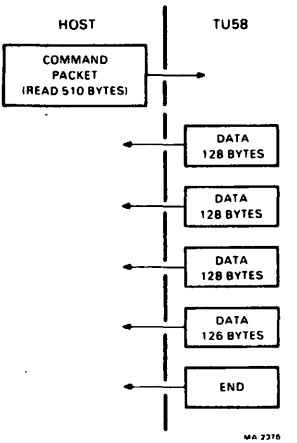


Figure 8 Read Command Packet Exchange

OP CODE 3 Write, and Write and Read Verify

This op code causes the TU58 to position the tape in the selected drive to the block specified by the number in bytes 10 and 11 of the command packet and write data from the first data packet into that block. It writes data from subsequent data packets into one or more blocks until the byte count called out in bytes 8 and 9 of the command packet has been satisfied.

The controller automatically zero-fills any remaining bytes in a 512-byte tape block.

There is one modifier permitted with the write command. A modifier of 000 0001 causes the TU58 to write all of the data and then back up and read the data just written with increased threshold and test the checksum of each record. If all of the checksums are correct, the TU58 sends an end packet with the success code set to 0 (or 1 if retries were necessary to read the data). Failure to read correct data results in a success code of -17 (1110 1111) to indicate a hard read error.

The write operation has to cope with the fact that the TU58 only has 128 bytes of buffer space. It is necessary for the host to send a data packet and wait for the TU58 to write it before sending the next data packet. This is accomplished using the continued flag. The continue flag is a single byte response of 001 0000 from TU58 to host. The write operation is shown for both write and write/verify operations in Figure 9.

OP CODE 4 (RESERVED)

OP CODE 5 POSITION

This command causes the TU58 to position tape on the selected drive to the block designated by bytes 10 and 11. After reaching the selected block, it sends an end packet. No modifiers are used.

OP CODE 6 (RESERVED)

OP CODE 7 DIAGNOSE

This command causes the TU58 to run its internal diagnostic program which tests the processor, ROM, and RAM. Upon completion, TU58 sends an end packet with appropriate success code (0 = Pass, −1 = Fail).

OP CODE 8 GET STATUS

This command is treated as an NOP. The TU58 returns an end packet.

OP CODE 9 SET STATUS

This command is treated as an NOP because TU58 status cannot be set from the host. The TU58 returns an end packet.

OP CODE 10 (RESERVED)

OP CODE 11 (RESERVED)

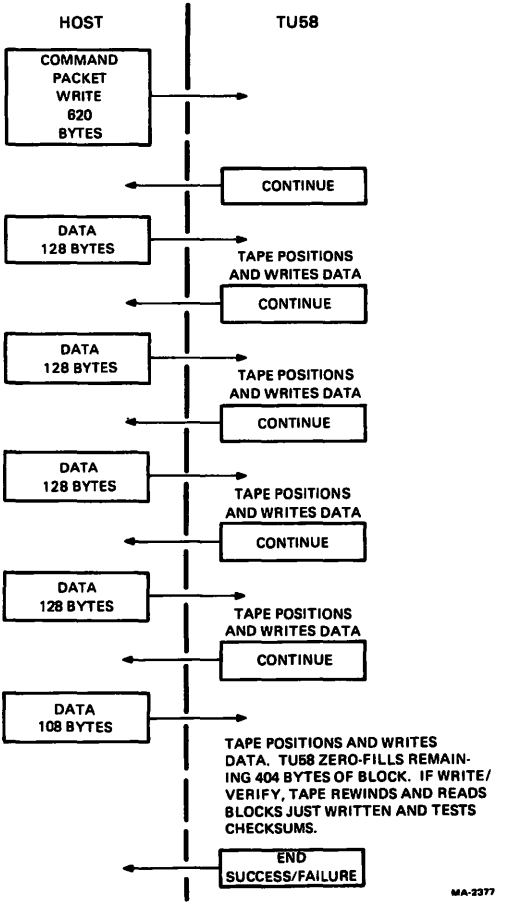


Figure 9 Write Command Packet Exchange

DRIVE AND MODULE INSTALLATION

Figures 10 and 11 provide the mounting dimensions for the circuit board (module) and drive mechanism. The drive has a 19 cm (7.5 in.) cable which plugs into the module header with the wires coming out of the plug toward the center of the module. The plug is keyed to ensure proper orientation. The cartridge extends 1.60 cm (0.62 in.) from the front of the drive. If the drive is recessed in a panel, clearance must be provided around the opening for fingers to grip the cartridge. Ideally, the cartridge slot in a front panel will be somewhat larger than minimum, to allow easy insertion. The opening should be at least the dimensions of the cartridge, 1.3 cm (0.5 in.) × 8.1 cm (3.2 in.), located not more than 0.53 cm (0.17 in.) above the bottom mounting surface.

The module should be mounted on a flat surface with 3 mm (4-40) hardware and 1 cm (3/8 in.) standoffs. Both the module and the drive may be mounted at any angle. For mounting to a surface above the drives, the 1.80 cm (0.71 in.) clearance is required; hole spacing is given in the outline drawings. For mounting to a surface below the drives, an 8.18 cm (3.22 in.) × 8.89 cm (3.50 in.) chassis cutout is required, with the same mounting hole spacing.

CAUTION

The mounting surface for the drives must be flat within 0.64 cm (0.025 in.).

INTERFACE STANDARDS SELECTION AND SETUP

The TU58 is shipped with factory-installed jumpers for a transmission rate of 38.4 kilobaud and the RS-423 unbalanced line interface (Figure 14). A variety of standards and rates may be selected by changing the jumpers on the controller module. Table 5 provides a list of all the pins on the board and their functions, including the wire-wrap (WW) pins, interface, and power connectors.

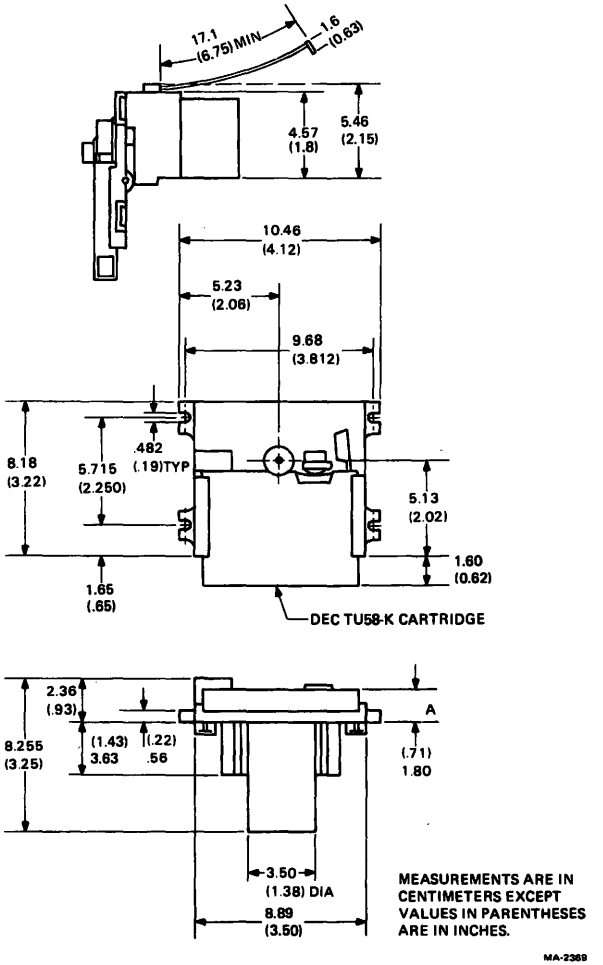
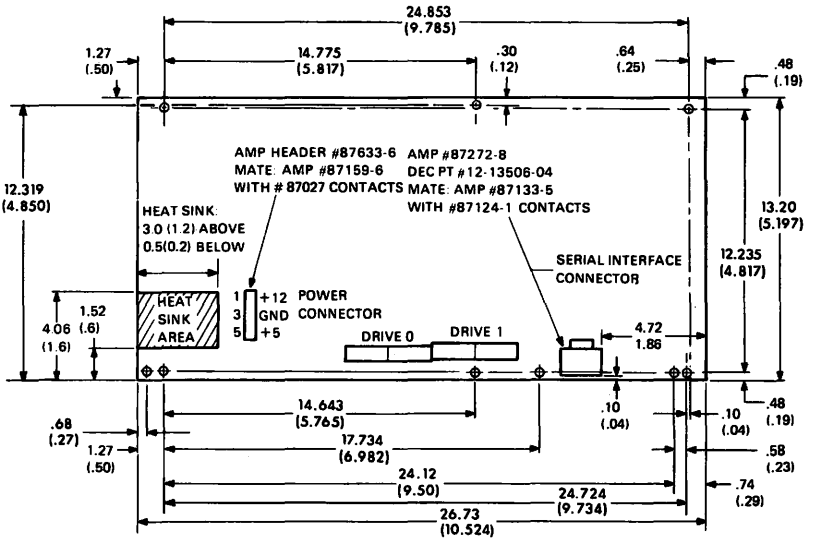


Figure 10 Drive Outline Drawings

TU58



MEASUREMENTS ARE IN
CENTIMETERS EXCEPT VALUES IN
PARENTHESES ARE IN INCHES
MEASUREMENTS ARE ±.013 (.005) CENTER TO
CENTER

MA-2370

Figure 11 Module Outline Drawing

Table 5 TU58 Module Connections

Wire-Wrap Pins	
WW1	150 baud
WW2	300 baud
WW3	600 baud
WW4	1200 baud
WW5	2400 baud
WW6	4800 baud
WW7	9600 baud
WW8	19,200 baud
WW9	38,400 baud
WW10	UART Receive Clock
WW11	UART Transmit Clock
WW12	Auxiliary A (to interface connector pin L)
WW13	Auxiliary B (to interface connector pin A)

WW14	Factory Test Point
WW15	Ground
WW16	Boot Connect together for auto-boot on power-up
WW17	RS-423 Driver
WW18	RS-423 Common (Ground)
WW19	Transmit Line +
WW20	Transmit Line –
WW21	RS-422 Driver +
WW22	RS-422 Driver –
WW23	Receiver Series Resistor
WW24	(Jump for RS-422)

Serial Interface Connector

J2-10	Auxiliary B	J2-5	Ground
J2-9	Ground	J2-4	Transmit Line –
J2-8	Receive Line +	J2-3	Transmit Line +
J2-7	Receive Line –	J2-2	Ground
J2-6	Key (no connection)	J2-1	Auxiliary A

Power Input Connector

J1-1	+12V
J1-3	Ground
J1-5	+5V
J1-6	Ground

Drive Cable

J3,4-1	Cart L	J3,4-9	LED
J3,4-2	No Connection	J3,4-10	Head Shield Ground
J3,4-3	Permit L	J3,4-11	Erase Return
J3,4-4	Signal Ground	J3,4-12	Erase 1
J3,4-5	Motor +	J3,4-13	Erase 0
J3,4-6	Motor –	J3,4-14	Head Return
J3,4-7	+12V	J3,4-15	Head 0
J3,4-8	Tachometer	J3,4-16	Head 1

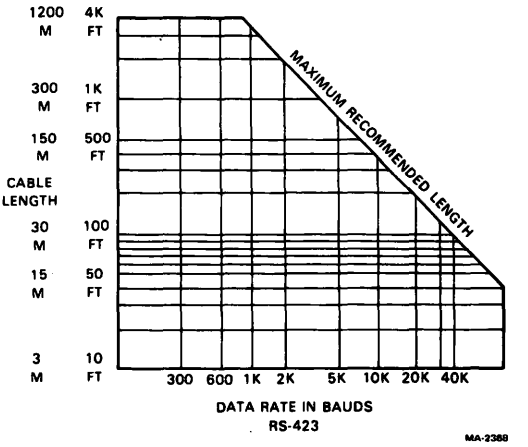


Figure 12 Data Rate and Cable Length for RS-423

Selecting Interface Standards

The serial interface operates on full-duplex, asynchronous 4-wire lines at rates from 150 baud to 38.4 kilobaud. The transmit and receive rates may be independently set. Each 8-bit byte is transmitted with one start bit, one stop bit, and no parity. The line driver and receiver may be set to operate with EIA RS-422 balanced or RS-423 unbalanced signal standards. When set to RS-423, the TU58 is compatible with devices complying with RS232-C.

The TU58 is shipped prewired for operation at 38.4 kilobaud transmit and receive on RS-423. The maximum wire length that may be used at the data rate in an electrically quiet environment is approximately 27 m (90 ft.). The wire used with any installation should be no less than 24 AWG diameter.

Longer wire runs may be made if data rates are reduced. RS-422 is considerably more noise-immune than RS-423 and can be used over at least 1200 m (4000 ft.) at any TU58 data rate. Figure 12, derived from the EIA standards, illustrates the variations in distance needed by RS-423 for different data rates. For more information, consult the standards for RS-422 and RS-423 published by the Electronic Industries Association.

Connecting Standard Jumpers

The jumper pins are standard 0.635 mm (0.025 in.) wire-wrap posts which may be connected using 30 AWG wire and a hand tool. Other techniques that may be used include slip-on connectors such as DEC H821 Grip Clips, 915 patchcords, 917 daisy-chain, or soldering.

The baud rates may be set independently for transmission and reception, or both can operate together. Simply connect the pin with the desired baud value to either the XMIT or RCV pins or both. Figure 13 illustrates the pin locations, and Figure 14 shows the factory-wired configuration.

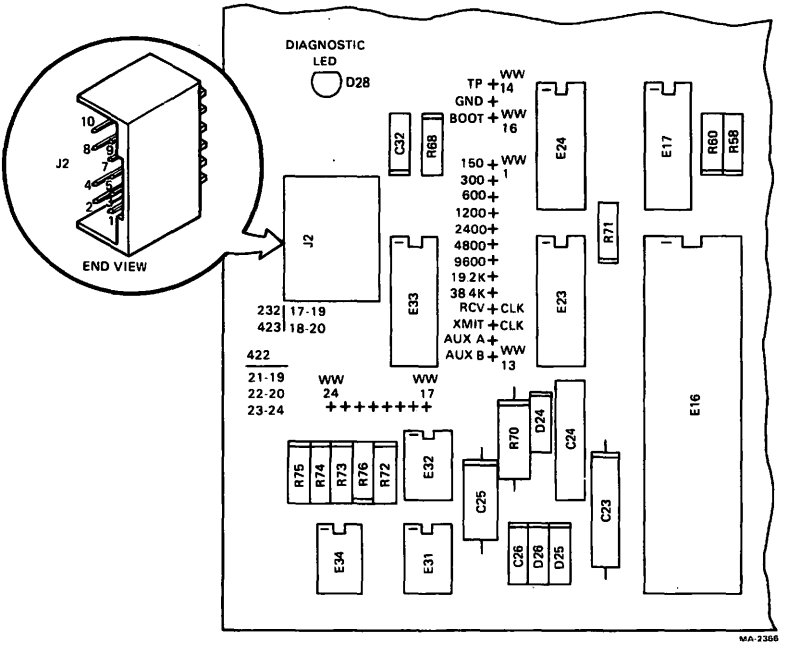


Figure 13 Interface Selection Jumper Pin Locations

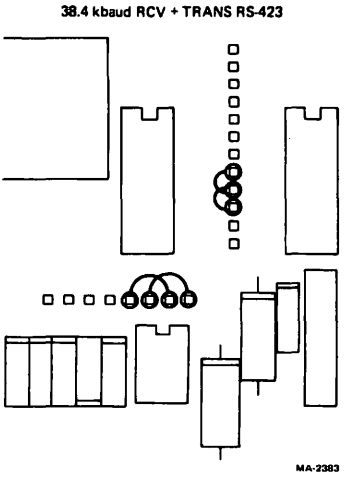


Figure 14 Factory Wiring

The interface standards may be selected by connecting sets of pins together. The connections are listed in abbreviated form in Figure 13. The group of pins 17 through 24 are the interface pins. The module is shipped prewired for RS-423 with pin 17 connected to pin 19, and pin 18 connected to pin 20. No other pins in the group are connected.

For RS-422, pin 21 should be tied to pin 19, pin 22 to pin 20, and pin 23 to pin 24. No other pins in the group are connected.

BLOCK DIAGRAM

Figure 3 shows the signal and control paths between the various elements of the TU58 and between the TU58 and its internal microprocessor. This diagram illustrates the control the microprocessor has over activities in the TU58.

Data Flow, Tape to Interface

The tape track is selected by signals from the I/O ports. Recorded data passes through the selection circuits to the read amplifier. There, the signal amplitude is adjusted to a standard level by the automatic gain control (AGC) action of the circuit. The Gain Reduce signal allows detection of weak recordings. The slope changes of the sinusoidal signal are sensed by the peak detector that produces a squarewave with a duty cycle similar to that of the original encoded data. The duty cycle is decoded to data bits by an integrater in the bit detector that

delivers the bits to the microprocessor serial data input (SID) with a strobe signal from the peak detector.

The microprocessor deserializes the read data and stores it in the data buffer area of memory. After a 128-byte record has been stored, a checksum calculated from the read data is compared with the checksum read from the tape. If they do not match, retries are attempted. Failure is indicated to the host in an end packet. Success results in the transfer of the data, one byte at a time, to the interface. If the unit has a parallel interface, the data is transferred eight bits at a time upon receipt of a strobe from the host. If the unit has a serial interface, the data is loaded into a UART and transmitted through line drivers with one start bit and one stop bit. A charge pump supplies negative voltage for the bipolar EIA line drivers since the power supply only produces positive voltages.

Data Flow, Interface to Tape

Data enters the interface and is latched (parallel) or deserialized and stored in a register (serial). The microprocessor receives a ready signal from the interface and transfers the data to a buffer area in memory. The data then re-enters the microprocessor, is serialized, ratio-encoded, and sent to the write circuit through the serial data output (SOD). When the write circuit interlock is released by the cartridge-activated write permit switches on the drives, write current is delivered to the correct head gap by selection circuits under microprocessor control. The erase circuit control logic is part of this control loop.

VELOCITY CONTROL

Velocity Sensing

Each motor has a LED lamp focussed on a phototransistor through a slotted disk on the motor shaft. (Only the activated drive delivers a tachometer signal.) This optical tachometer output is amplified and shaped by a comparator to produce a pulse rate proportional to the shaft speed of the motor. The buffered pulses from the optical tachometer go into an 18-bit shift register. The clock for the shift register is selected to give a quarter-period delay to the pulses at the desired shaft speed. The delayed and undelayed pulses are then exclusive-ORed to yield a pulse width modulated representation of the actual velocity. Modulation occurs because the shift-register delay, a fixed amount of time, is a different fraction of a period for different tachometer frequencies. Therefore, the amount of overlap varies between delayed aand undelayed waves. The overlap is extracted by the exclusive-OR gate, averaged to a dc level by a capacitor, and buffered by an operational amplifier (op amp).

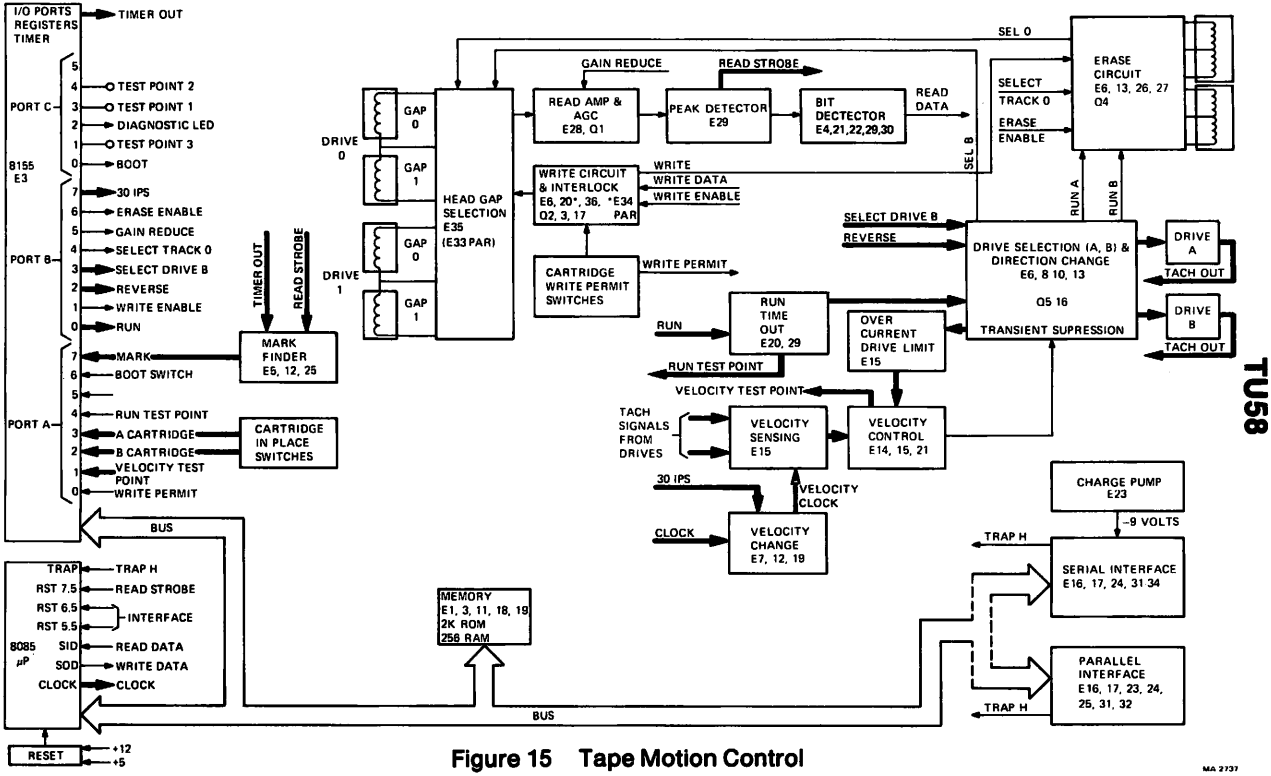


Figure 15 Tape Motion Control

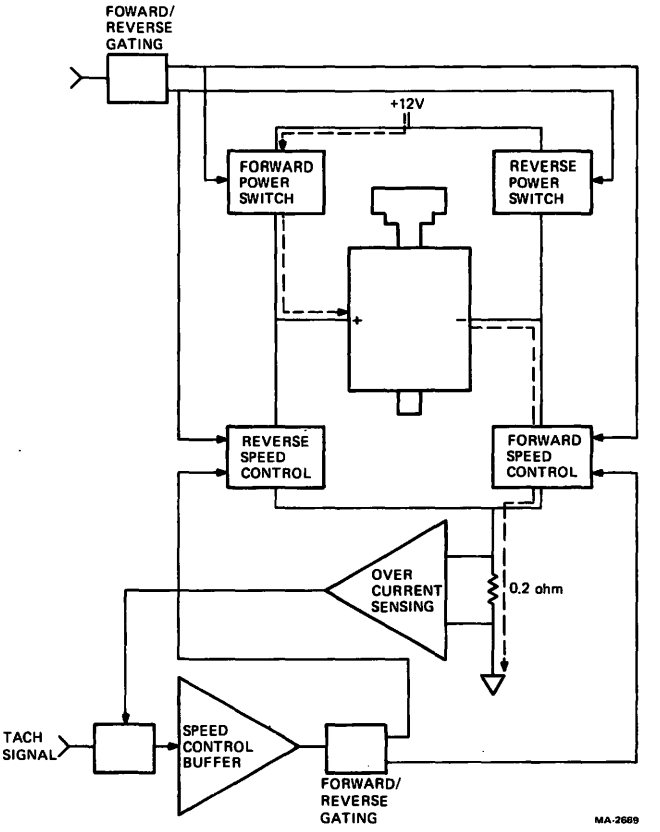


Figure 16 Motor Bridge

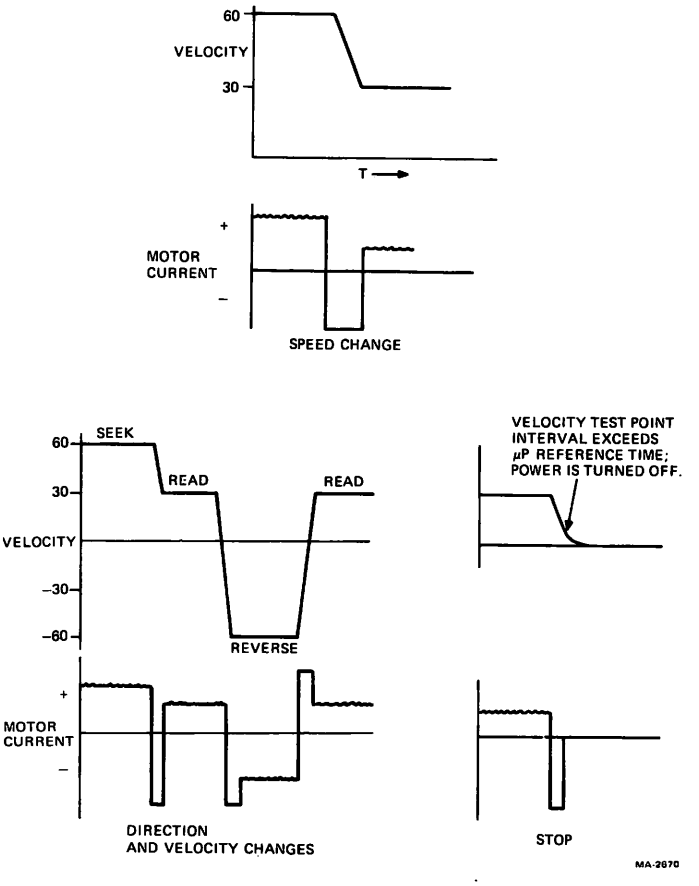


Figure 17 Velocity Change Waveforms

HEAD SELECTION

The read/write heads are selected by signals from the microprocessor. The microprocessor generates a SEL DRV B signal to choose the head. The gap for track 0 or track 1 is chosen by SEL 0 H from the microprocessor. The selected head gap is connected to the read and write circuitry through a dual 4 to 1 multiplexing analog switch IC. The IC's dual circuits are paralleled to minimize series resistance in the low impendance write driver circuit. The common taps of both heads are connected together, so only one lead per gap needs to be switched.

WRITE CIRCUIT AND INTERLOCK

The write drivers are two transistors (Q2, Q3) arranged as a constant current source and sink operating at 7.5 mA. They use tristate buffers as data-gated switches and return paths. Writing is gate-interlocked by the mechanical interlock on the cartridge in the drive being selected. Also, the microprocessor tests the mechanical switch for the Write Permit signal before turning on write current. Attempting to write while the cartridge is write-protected results in an error report to the host. The microprocessor Write Enable signal turns the write current on and off at the proper times. In the absence of write enabling, the tristate outputs become open-circuited and source and sink transistors Q2 and Q3 are biased off.

ERASE CIRCUIT

Erase gaps are selected by the same pair of signals that select read/write gaps. They are also enabled by ERASE ENA L. A 26 mA current source supplies the erase gaps in common. Current through the desired gap is passed to ground through a peripheral driver (high current capacity) gate which is part of a decoder for the control signals. A diode across each erase head winding clamps the inductive voltage spike when the erase current is turned off.

DATA ENCODING AND DETECTION

Data is recorded on tape using the ratio encoding method. Each data bit is given a cell with room for three flux reversals. After an initial positive transition, only one of the remaining reversal positions is used. If the reversal occurs in the first available position, the bit is a zero. If it occurs in the second position, the bit is a one. These position shifts correspond to duty cycles or ratios of 1/3 and 2/3 (Figure 18). To compensate for waveform distortion in the recording process, the actual write encoding ratio is ¼ to 3/4.

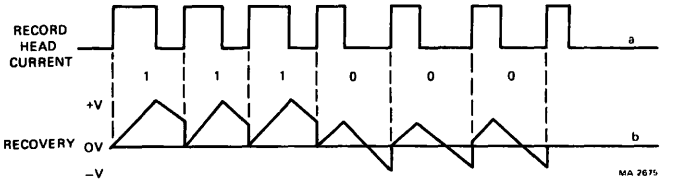


Figure 18 Data Encoding and Decoding

The beginning of a bit cell is defined by a positive peak at the read amplifier. The second flux reversal is defined by the next negative peak. The peaks are detected by a comparator.

The read amplifier output is fed to one input of the comparator. The same signal is phase-shifted and fed to the other output. The output is high for a positive slope input and low for a negative slope input. A small amount of hysteresis is added to prevent oscillation at the zero-sloped-point.

The output of the comparator has a duty cycle similar to that of the original encoded signal. The data are recovered using an integrater as shown in Figure 18B. The integrater is discharged by an analog switch on the positive edge of the data waveform. The integrater is sampled by a flip-flop on the next edge. If the integrater is positive at sample time, the recorded bit was one. If the integrater is negative at sample time, the bit was zero.

Decoded data is delivered to the serial data input (SID) on the 8085 microprocessor, while a strobe corresponding to the moment of integrater sampling triggers an interrupt to get the microprocessor to store the data bit in a register.

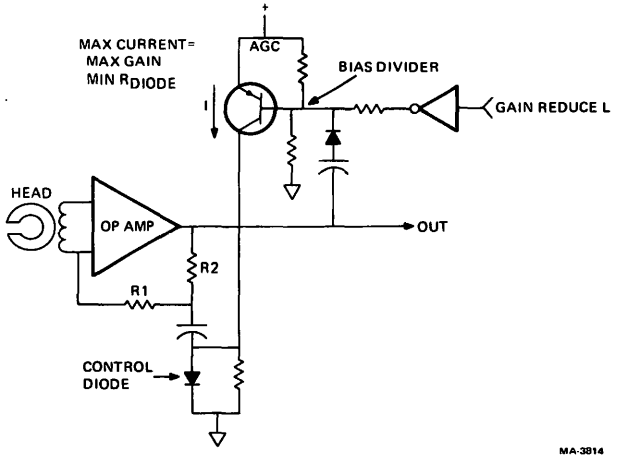


Figure 19 Read Amplifier and Automatic Gain Control

READ AMPLIFIER AND AUTOMATIC GAIN CONTROL

An op amp amplifies the signals coming from the selected head. Automatic gain control (AGC) maintains a constant output to following stages in the presence of large variations in output from the tape because of worn tape or recording variations (Figure 19).

CHARGE PUMP

The principle behind the operation of the charge pump is that of charge storage in a capacitor. This is illustrated by the simplified example in Figure 20. Assume that a capacitor is connected between a positive charge source, e.g., +12V and ground. Electrons will accumulate at the grounded end. If the capacitor is disconnected from the source and ground, it still has 12V across it, because the electron charge accumulated may not move. If the original positive end is connected to ground, the 12V extends its polarity below ground because now there is an excess of electrons relative to ground. This negative potential is available to do work at a rate subject to the charge capacity of the storage element (capacitor).

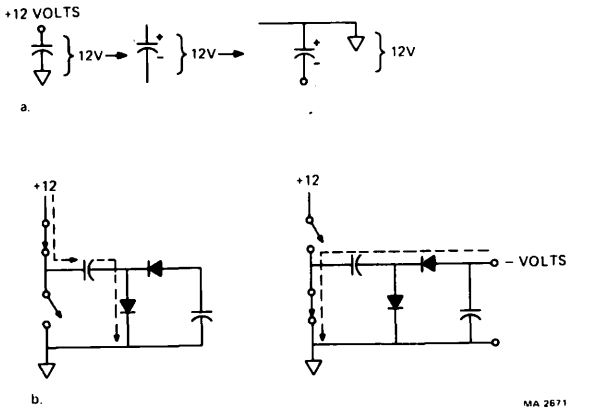


Figure 20 Simplified Charge Pump

MARK FINDER

A specially encoded signal is recorded on the DECtape II as part of the formatting operation. The signal is recorded at one quarter of the normal bit density and is located at the beginning and end of the tape (BOT and EOT) and also between each of the formatted records. The signal is called a mark and indicates the location of the beginning of each record header. This allows the microprocessor to count the passage of records past the head at winding speed, and alerts the microprocessor when the tape enters the BOT or EOT regions. Header marks and BOT-EOT marks are distinguished by different bit patterns. BOT is all zeros, EOT is all ones, and the header mark alternates ones and zeros. The mark is detected by a circuit that detects the lower bit density of the mark compared with normal data. The microprocessor sets up the timer in the 8155 to provide a clock to the mark finder. The clock is chosen to allow the MARK H output to be set while the pulse rate coming in through the read strobe input is lower than that of the timer. MARK H appears at an input port that is examined by the mark-detecting routine in the microprocessor.

INTERFACES

Serial Interface

Data moves within the TU58 microprocessor on an 8-bit parallel bus. Data is transferred between the TU58 and the host computer through a full-duplex asynchronous serial interface that uses one signal loop

(conductor pair) for each direction. The universal asynchronous receiver/transmitter (UART) performs the parallel to serial and serial to parallel conversions that make the economy of wire possible. The UART, a single IC, contains circuitry allowing wired programming of its conversion format, plus microprocessor bus protocol management, and the capability to detect conversion and timing errors.

MICROPROCESSOR AND MEMORY

All TU58 activities are supervised or directly controlled by an 8085 microprocessor. The microprocessor operates with firmware stored in a 2K × 8 read-only memory (ROM). Scratchpad memory for the microprocessor computations, and a 128-byte buffer for data coming from the host, are located in a 256 × 8 random access memory (RAM).

I/O Ports

The I/O ports provides most of the communication paths between the microprocessor and the TU58 hardware. Port A provides the inputs for the various status signals from the mechanism, such as cartridge present and write permit. Port B delivers control signals to the system, such as velocity and direction commands. Port C controls the self-test indicator lamp and causes the interface to the host to transmit Break as a part of the boot sequence.

Port C also carries three signals useful for module testing. Test Point 1 (pin 1) pulses high when the header of a sought record is successfully read (confirmed by the record number complement). Test Point 2 (pin 2) pulses high each time the header of any record is unsuccessfully read. Test Point 3 (pin 38) pulses high after a record of data is read but fails the checksum test.

Registers and Timer

The 8155 registers control the operation of the I/O ports and timer. The registers are addressed as I/O locations like the ports. The control/status register defines the ports as input or outputs and sets the timer start and stop characteristics. The timer registers define the cycle characteristics and load the value required to generate the desired pulse interval with the system clock at the timer's clock input. A 14-bit counter, parallel-loaded by the registers, provides the timer function.

FIRMWARE

The TU58 operates under control of a microprocessor whose instructions are stored in a ROM. These instructions, called firmware, define the functions and capabilities of the TU58 as an integral part of the

normal TU58 operation. No extensive coverage is attempted because firmware problems cannot be repaired in any direct way. The self-test checks for proper contents in the ROM and halts the processor if a fault is detected. The self-test checks other things as well but does not isolate the problem to a particular component. Field repair is the replacement of the module.

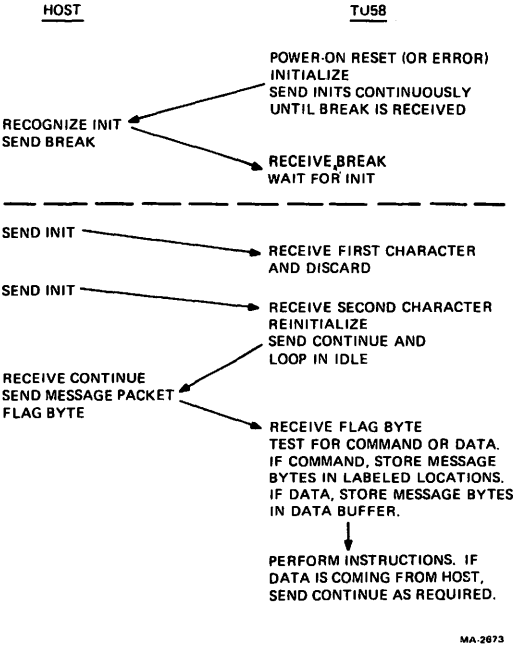


Figure 21 Host TU58 Power-Up Interchange

VK170-CA

SERIAL VIDEO MODULE

GENERAL

The VK170 module forms an integral part of a terminal. The module accepts serial ASCII encoded data to be stored in a refresh memory to generate a display for a video monitor. The VK170 also accepts parallel data from a keyboard (on strobe demand) to generate serial ASCII output.

The VK170 is an extended-length, double-height, single-width board. Mounting holes are provided for stand-off mounting via handle rivets and two holes located near the module fingers (Figure 2).

FEATURES

- Complete video subassembly on a double-height module
- Displays a full 80 characters per line and 25 lines
- 7 × 7 characters displayed in 8 × 8 character cells using standard installed character ROM
- 8 × 8 character cell allows simple graphics with customer-defined character set
- Selectable attributes:
  - blink
  - half intensity
  - reverse video
  - characters, from customer-defined character set
- Customer may enable video attributes on a character-by-character basis
- I.C. socket for two customer-defined character sets (2716 EPROM or equivalent)
- Simple EIA RS-423 serial interface for direct interconnect to DLV11-J or MXV11, consequently no bus loading
- Jumper-selectable baud rates: 150, 300, 600, 1200, 2400, 4800, 9600, 19,200, 38,400
- Smooth scroll is used to move text up the screen to allow entry of new data on the bottom line of the display
- Drives standard video monitors over coaxial cable per EIA RS170, or jumper-selectable for direct drive monitor

VK170-CA

- Interfaces to a standard keyboard (8-bit ASCII)
- Can be plugged into LSI-11 backplanes or mounted on stand-offs applying power via H807 edge connector

SPECIFICATIONS

Height	13.2 cm (5.2 in.)
Length	22.3 cm (8.5 in.)
Width	1.27 cm (0.5 in.)
Power Requirements	+5V ±5%, 1.2A +12V (or −15V) ±3%, .15A

The VK170 module operates under the following conditions:

- Environment must conform to:
  Temperature 5°C to 60°C
  Humidity 10% to 95% (no condensation)
- Power dissipation is based on circuit requirements of 1.8 amps maximum. If only 5 Vdc is used, power dissipation does not exceed 9 watts. An additional 2 watts (nominal) is dissipated when the ± HV (nominal 12 volts) is enabled.

DESCRIPTION

The VK170 functions as separate input and output devices. Parallel data bits from a user-supplied keyboard are serialized and transmitted (XMIT DATA SERIAL ASCII) to a computer serial line interface (e.g., DLV11-J).

Serial data bits received from a serial line are decoded in the internal logic to determine whether a received character is a displayable character or a control character (e.g., CR, LF). Displayable characters are written into an internal memory which is continuously read to generate the video signal used to refresh the screen of the customer-supplied video monitor.

The communications port contains the necessary level converters to allow the module to communicate with the serial lines in either EIA RS-423 or 20mA current loop.

A master crystal clock generates the required timing for the baud rates for the UART in the communications port and also generates the horizontal and vertical synchronization signals for the external video monitor.

The internal charge pump power supply runs on either +12V or −15V input. Output from the power supply is used to power the EIA RS-423 driver for the serial line as well as provide a source of −12V for the external keyboard.

The cursor and attribute logic provides control over the individual attributes as selected by the wire-wrap jumpers and the control characters as well as relocating the video cursor as required. This logic also provides internal control over the scroll function, allowing a normal smooth scroll to be replaced by a high-speed jump scroll if the data input is faster than the execution time for smooth scroll.

The video image consists of 25 lines of 80 characters each presented in adjacent 8 × 8 dot cells (Figure 1).

Horizontal Frequency = 15.36 kHz
Vertical Frequency = 60 Hz
Horizontal scan lines per frame = 256 lines

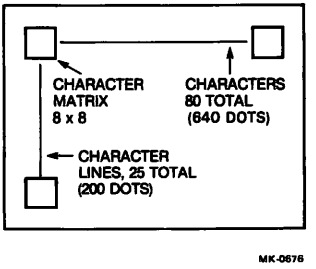


Figure 1 Video Image

Smooth scrolling rolls a clear line into the bottom of the image display. It is used whenever an attempt is made to move the cursor down with a line feed (LF) or a vertical tab (VT) after the cursor has reached the bottom line.

Direct cursor addressing is available (VT52 compatible).

Character attributes allow selection of blink, forward and reverse video, alternate character set, or half intensity. The selected attribute may be set or cleared with bit 8 of the received data or with ASCII character SO/SI (Shift Out/Shift In).

The cursor is a flashing reversed video cell with a 500 millisecond nominal period and a reversed duty of 60% to 80%.

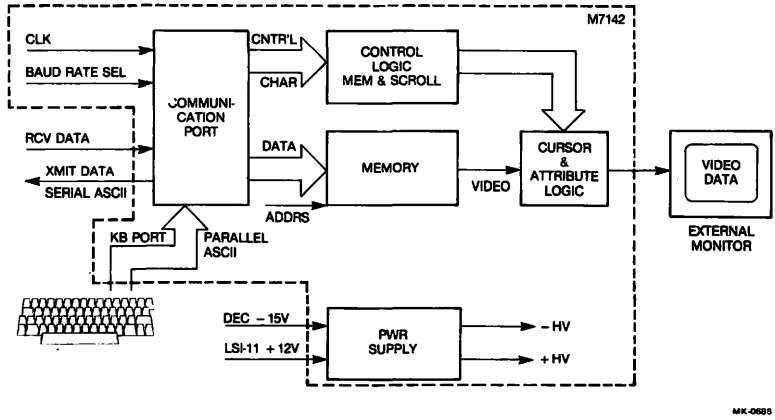


Figure 2 Port Interaction

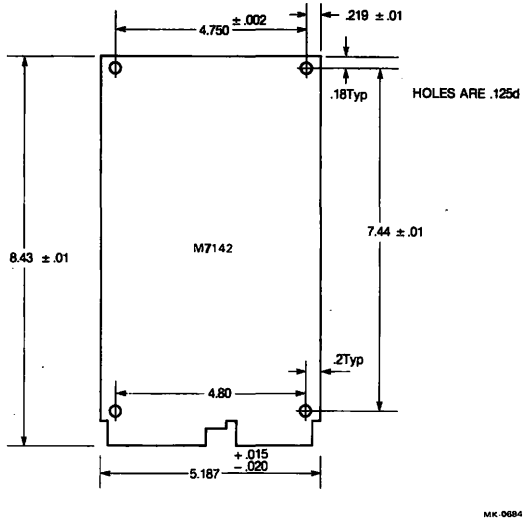


Figure 3 Mechanical Packaging

CONFIGURATION

Interface

This section describes the sequences of signal exchanges that occur among the VK170 and other external devices. Figure 4 shows the pin number locations of the interfacing connectors.

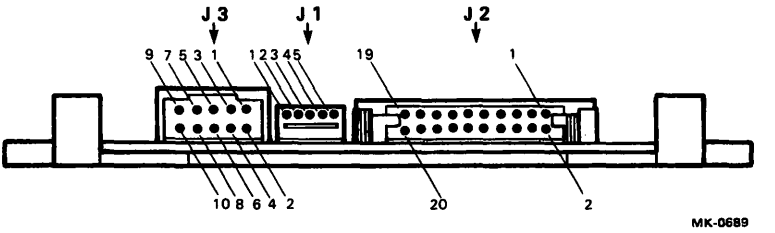


Figure 4 Connector Pin Number Location Diagram

Keyboard/VK170 Interface

The keyboard interfaces to the VK170 via a 20-pin connector (J2). The DIGITAL mating connector is the H8561. Table 1 presents the connector pin numbers and associated signal names.

Table 1 Keyboard/VK170 Connector (J2)

Pin No.	Signal Name	Pin No.	Signal Name
1	+5 Volts	11	KB4
2	−12 Volts	12	Not used
3	GND	13	KB3
4	KB8	14	BREAK (GND)
5	KB7	15	KB2
6	GND	16	GND
7	KB6	17	KB1 (LSB)
8	KBSTRB H	18	GND
9	KB5	19	Not Used
10	BREAK	20	Not Used

Edge Connector

VK170 edge connector pins and associated signals are presented in Table 2.

Table 2 VK170 Edge Connector

Pin No.	Signal Name
AA2,BA2	+5 Vdc
AC2,AT1,BC2,BT1	GND
AB2	−15 Volts
AD2	+12 Volts
Others	Not Connected

Video Output Connector

Video output is provided as RS170 compatible and as separate TTL output lines. A 5-pin MOLEX* connector (J1) is used with pin assignments as shown in Table 3. (Mating connector = H8562.)

Composite video output provides RS170 output generated by combining the video signal with a composite sync signal. The picture from the balancing level to reference white across 75 ohms is 1 volt. The synchronizing levels are imposed at 40% of the signal.

* Vendor Trademark

Table 3 Video Output Connector (J1)

Pin No.	Signal Name	Timing/Freq
1	HORIZONTAL DRIVE H	15.36 kHz/27 μs
2	VERTICAL DRIVE L	60 Hz/520 μs
3	VIDEO HI Z	
4	GND	
5	RS170 VIDEO	

0 volts = SYNC
0.4 volts = BLACK
1.4 volts = WHITE

For direct drive output, jumper W4 must be cut, providing a high impedance source at the MOLEX* connector, pin 3. The VK170 has been tested with the following direct drive monitors:

- ITOH
- Ball Brothers
- Elston

Communications Port Connector

The communications port is a 10-pin connector (J3), pinned for direct DLV11-J connection. The electrical interface may be wired for RS-423

or 20 mA communication (see Figure 5). The DIGITAL mating connector is H8560. Table 4 presents the pin assignments and associated signal names.

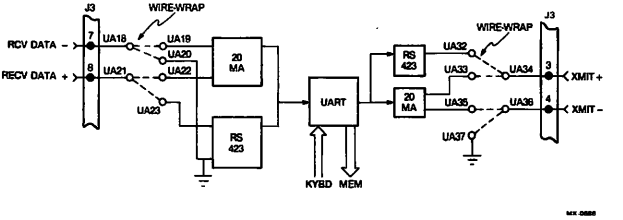


Figure 5 Select RS-423/20 mA Loop

* Vendor Trademark

Table 4 Communications Port Connector (J3)

Pin No.	Signal Name
1	CLOCK I/O
2	GND
3	XMIT DATA +
4	XMIT DATA –
5	GND
6	NOT USED/POLARIZING POINT
7	RCV DATA –
8	RCV DATA +
9	GND
10	20 mA SOURCE

Installation Procedures

The following sections describe the installation of the VK170 module.

Jumper Configurations

Figure 6 illustrates the location of the various jumpers and wire wrap posts of the VK170. Verify that the factory-installed jumpers are configured per Table 5. Any jumper configuration changes required for user applications should be made at this time.

Data Rate Selection

The data rates are generated via a 13.5168 MHz crystal and selected through a dual 4-bit decade and binary counter. The following data rates are selectable: 150, 300, 600, 1200, 2400, 4800, 9600, 19,200, and 38,400 bits per second.

The UART may be configured to transmit and receive at either the same data rate or at split data rates. Data rates are configured by connecting a jumper from the selected data rate wire-wrap pin to the clock input pin(s) of the UART. When configuring at the same data rate, the wire-wrap pins may be daisy-chained. Table 6 lists the data rates and their respective pin numbers.

The UART can be configured to operate from an external clock source via pin 1 of J3. Both UA26 and UA27 must be jumpered to the external clock. Do not select a data rate pin when using an external clock.

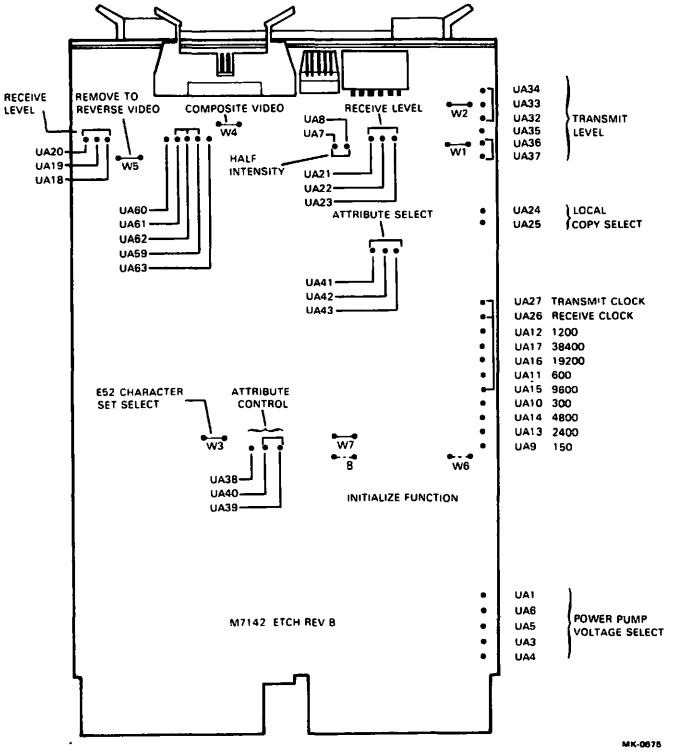


Figure 6 Jumper and Wire Wrap Post Locations

Table 5 Factory Installed Jumper Configurations

Jumper	Function Implemented
W1 (or UA1 to UA5)	+12V operation
W2 (or UA4 to UA6)	
W4	RS170 operation
W7	Form feed receive enabled for remote initialization
UA59 to UA61 to UA62	8-bit—no parity
UA18 to UA20	
UA21 to UA23	EIA RS-423 operation
UA34 to UA32	
UA36 to UA37	
W3	E52 character set enabled
UA39 to UA40	SI/SO (Shift In/Shift Out) attribute control
W5	Forward video
UA41 to UA43	Blink attribute enabled
UA26 to UA27 to UA15	9600 data rate selected

Table 6 Data Rate Jumper Configurations

FROM	TO Pin	Data Rate
	UA9	150
	UA10	300
Transmit clock	UA11	600
pin UA27	UA12	1200
and/or	UA13	2400
Receiver clock	UA14	4800
pin UA26	UA15	9600
	UA16	19200
	UA17	38400

Attributes and Attribute Control Selection

Several jumpers are used for attribute and attribute control selection. Table 7 lists the various attribute and attribute control configurations.

Communications Selection

Four jumpers are used for communications selection. Table 8 lists the jumper configurations required for either EIA RS-423 or 20 mA current loop communications.

Table 7 Attribute Jumper Configurations

Jumper	Characteristic
W3	Install to enable character ROM E52 Remove to enable character ROM XE53
W5	Install for forward video Remove for reverse video
UA7 to UA8	Install to disable half intensity
UA41 to UA42	Install to select reverse attribute
UA41 to UA43	Install to select blink attribute
UA40* to UA38	Install to select character bit 8 for attribute control
UA40* to UA39	Install to select SI/SO for attribute control

UA40 can either be jumpered to UA38 or UA39, but not both at the same time.

Table 8 Communications Jumper Configurations

	TO	
FROM	**RS423**	**20 mA**
UA18	UA20	UA19
UA21	UA23	UA22
UA34	UA32	UA33
UA36	UA37	UA35

Parity Selection

As many as three jumpers can be used to select ASCII serial data format. Table 9 lists the jumper configurations required to select either odd, even, or no parity.

Voltage Selection

As many as six jumpers (two are optional) can be used for voltage selection. Table 10 lists the jumper configurations required for either +12 Volt or −15 Volt operation.

Table 9 Parity Jumper Configuration

Characteristic	Jumper
No Parity (8 data bits)	UA59 to UA61 to UA62
Odd Parity (7 data bits)	UA60 to UA61 to UA62 to UA63
Even Parity (7 data bits)	UA60 to UA61 to UA62 and UA59 to UA60

Table 10 Voltage Jumper Configurations

Jumper	+12V	−15V
W1 (or UA1 to UA5)	In	Out
W2 (or UA4 to UA6)	In	Out
UA3 to UA5	Out	In
UA1 to UA6	Out	In

Remote Initialize Selection

As many as three jumpers are used for remote initialize selection. Table 11 lists the jumper configuration required for remote initialization.

Table 11 Remote Initialize Jumper Configurations

Characteristic	W6	W7	W8
Form Feed Receive	Out	In	Out
Break	In	Out	In
None	Out	Out	In
Form Feed or Break	In	In	Out

Module Mounting

The VK170 module is mounted by one of two methods.

1. The module can be mounted in a DIGITAL computer backplane, taking care that all signals (e.g., grant lines) are jumpered on the backplane as required.
2. The module can be mounted on a panel or chassis using nylon hardware (i.e., spacers and #2-56 screws and nuts as required), using the mounting holes in the module.

   The H807 edge connector is available to provide power connection to the VK170 when used in this mounting configuration.

Checkout Procedures

Two checkout methods are available to the user:

1. When the VK170 is used on a PDP-11 system, run the diagnostic CZVTO in accordance with the instructions distributed with the diagnostic.
2. To check out the VK170 without a processor, local testing can be done over the RS-423 or 20 mA communication lines.

   If the VK170 is configured for RS-423 operation, jumper J3-3 (XMIT DATA +) to J3-8 (RCV DATA +) to provide local testing with a user-supplied display monitor and keyboard.

   If the VK170 is configured for 20 mA current loop (passive), local testing is provided by the following three jumpers:

   J3-10 (+ Voltage) to J3-3 (XMIT DATA +)
   J3-4 (XMIT DATA −) to J3-7 (RCV DATA +)
   J3-8 (RCV DATA −) to J3-9 (GND)

   Once these three jumpers are installed, a user-supplied keyboard and display monitor can be used to check the operation of the module.

PROGRAMMING

Control/Function Characters

The control/function characters are interpreted as non-graphic data. The following actions occur at the terminal upon receipt of these characters from the communication port:

- BS (backspace)—the cursor moves one position to the left, if it is not currently in it leftmost position (left margin).
- HT (horizontal tab)—the cursor moves one position to the right, if it is not currently in its rightmost position (right margin).
- FF (form feed)—the module is reinitialized if the remote-initialize form-feed jumper is installed (34 ms of no transmission fill-time required).
- CR (carriage return)—the cursor moves to the left margin.
- LF (line feed)—the cursor moves down one line if not in scroll mode. (Scroll mode is entered when the cursor enters the bottom line, scroll mode is exited by an initialize operation.) If required, a smooth scroll occurs and a clear line is provided. If a scroll operation occurs at data rates above 19,200, 512 microseconds are required before another scroll can be requested.

- VT (vertical tab)—the cursor moves as in a line feed, except the next line is not cleared. If a scroll operation occurs at data rates above 19,200, 512 microseconds are required before another scroll can be requested.
- BREAK (spacing condition)—an initialize sequence similar to power-up initialization is generated if remote initialize BREAK jumpers are installed (34 ms of no transmission fill-time required).

Cursor Addressing

Direct cursor addressing allows movement to any position on the screen by transmitting an escape sequence to the module.

The ESC character followed by the Y character sets up the logic for a new cursor location : e.g.,

<ESC> <Y> <Line number> <Column number>

- <ESC> <Y> = Defines cursor addressing function
- <Line number> = one character
  040 = top line (ASCII space)
  041 = second line (ASCII !)
  .
  .
  .
  070 = bottom line (ASCII 8)
- <Column number> = one character
  040 = leftmost column (ASCII space)
  .
  .
  .
  157 = rightmost column (ASCII o)

The cursor is moved to the specified column of the specified line. For example, the sequence <ESC> <Y> <)> <A> places the cursor on the tenth line (because ASCII <)> is 51_8) and in the thirty-fourth column (because ASCII <A> is 101_8; and -40_8 for the offset results in octal column 41). The initial sequence should be preceded by a form feed (FF) to initialize the screen registers, if a scroll has been performed.

Optional Character Set Selection

Selection of the optional character ROM is accomplished via the removal of jumper W3. An optional character-generator socket is provided on the VK170.

Data Formats

The data mode for ASCII serial input is eight-level without parity. In this case, the lower order bits represent the appropriate character with bit 8 as the attribute select bit. If bit 8 is set, the selected attribute is enabled for the character received.

For the 7 bits with odd or even parity mode, SI/SO can be used to select the attribute bits. When enabled, all characters received after SO have the attribute selected. All characters received after SI have the attribute deselected. The implemented ASCII 7-bit character set is shown in Figure 7.

Attributes

Selection of the various attributes is controlled by setting ASCII bit 8 to a logical one (1) or manipulation of SI/SO and adding/deleting wire-wrap jumpers on the VK170 module (see Figure 8).

This section contains a description of each attribute, instructions for implementation, and illustrations of each attribute as it appears on the screen.

Reverse Video Versus Forward Video

The forward video display on the CRT consists of white characters on a black background. To change the entire display to reverse video, (black characters on a white background), jumper W5 must be removed as shown in Figure 9.

Reverse Video Attribute

The reverse video attribute reverses the video on a character-by-character basis. Wire-wrap UA41 to UA42 must be installed for the reverse video function. (Refer to Figure 9.)

b_7 b_6 b_5 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
BITS ↓	b_4	b_3	b_2	b_1	COLUMN → / ROW ↓	0	1	2	3	4	5	6	7
	0	0	0	0	0			SP	0	@	P	`	p
	0	0	0	1	1			!	1	A	Q	a	q
	0	0	1	0	2			"	2	B	R	b	r
	0	0	1	1	3			#	3	C	S	c	s
	0	1	0	0	4			$	4	D	T	d	t
	0	1	0	1	5			%	5	E	U	e	u
	0	1	1	0	6			&	6	F	V	f	v
	0	1	1	1	7			'	7	G	W	g	w
	1	0	0	0	10	BS		(	8	H	X	h	x
	1	0	0	1	11	HT		)	9	I	Y	i	y
	1	0	1	0	12	LF		*	:	J	Z	j	z
	1	0	1	1	13	VT	ESC	+	;	K	[	k	{
	1	1	0	0	14	FF		,	<	L	\	l	|
	1	1	0	1	15	CR		-	=	M	]	m	}
	1	1	1	0	16	SO		.	>	N	^	n	~
	1	1	1	1	17	SI		/	?	O	-	o	

Figure 7 ASCII Character Set MK-0688

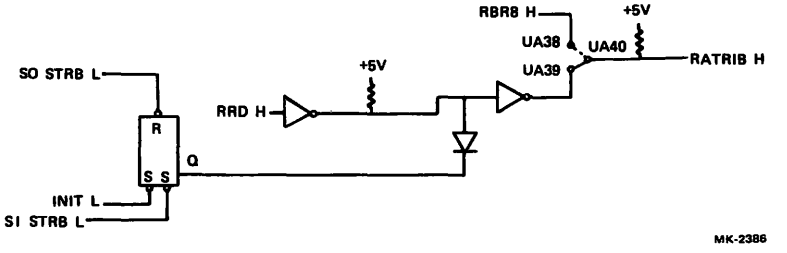


Figure 8 Attribute Selection Flow

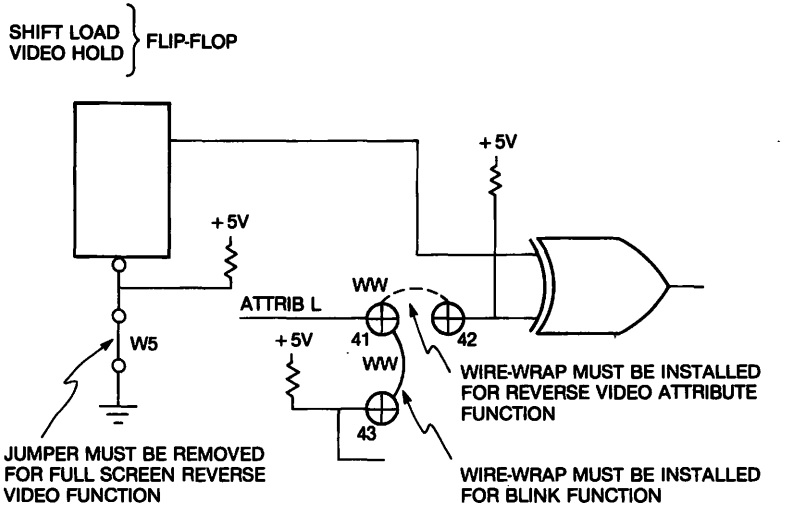


Figure 9 Reverse Video and Blink Attributes

Blink Attribute
A wire-wrap must be installed as shown in Figure 9 to implement the blink attribute.

Half Intensity
The wire-wrap shown in Figure 10 must be removed to enable the half intensity attribute.

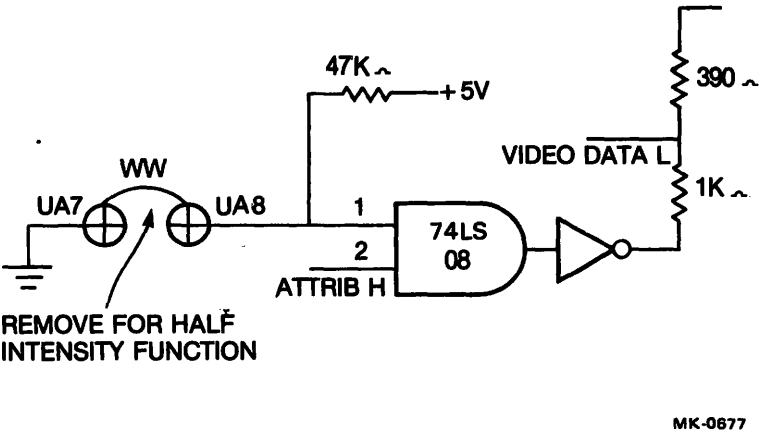


Figure 10 Half Intensity Wire-Wrap Removal

W9500 HIGH-DENSITY WIRE-WRAPPABLE MODULES

GENERAL

The W9500 series of high-density wire wrappable modules enable a user to easily configure special interface logic for the LSI-11 Microcomputer systems. These modules consist of DIGITAL's standard double and quad height sizes and are available with or without premounted Dual-In-Line Packages (DIP) low-profile sockets.

SPECIFICATIONS

W9511 Quad-Height Without Sockets

Height	Quad, 10.5 in. (26.6cm)
Length	Extended, 8.9 in. (22.8cm)
Width	Single, 0.5 in. (1.27cm)
Vcc Pins	AA2, BA2, CA2, DA2
GND Pins	AT1, BT1, CT1, DT1, AC2, BC2, CC2, DC2

W9512 Double-Height Without Sockets

Height	Double, 5.2 in. (13.2cm)
Length	Extended, 8.9 in. (22.8cm)
Width	Single, 0.5 in. (1.27cm)
Vcc Pins	AA2, BA2
GND Pins	AT1, BT1, AC2, BC2

Figure 1 LSI-11 Bus-Compatible Modules (With DIP Sockets)

Figure 2 LSI-11 Bus-Compatible Modules (No DIP Sockets)

DESCRIPTION

The LSI-11 compatible series consists of four modules: a quad-height with and without premounted sockets and a double height with and without premounted sockets.

Table 1 provides a brief summary of each type. All modules are **single**-width; the height of each pin is 5/16 in.

Each module without premounted sockets is configured to accept IC packages with pin centers on 0.3 in. (7.62cm); 0.4 in. (10.16cm); and 0.6 in. (15.24cm). The IC package density for these modules is shown in the drawings in this data sheet. Each module can be wrapped by standard automatic wrapping techniques as well as by hand.

Those modules with premounted sockets accept 16-pin IC's with 0.3 in. centers. Space is provided between the sockets for decoupling capacitors or other discrete components as required by the user. In addition, these modules supplied with sockets also contain universal areas that will accept IC's with pin centers of 0.3 in. (7.62cm); 0.4 in. (10.16cm); and 0.6 in. (15.24cm). The accompanying photos and drawings point out these universal areas and their capacities.

The printed circuit on each board connects the appropriate edge connector pins to the Vcc plane on side 2 of the board and the ground plane (GND) on side 1 (component side). The remaining edge connector pins terminate to a double row of wire wrap pins for user designated functions. Each of the modules also includes a 40-pin male cable connector to allow an interface cable to be attached to the module logic. The pins of the cable connector are also terminated to a double row of wire wrap pins. The quad height modules are also provided with a space where an additional 40-pin cable connector (labeled J2) can be inserted by the user. When a connector is not required, additional IC packages with .3, .4, and .6 in. centers can be installed in the space reserved for the connector. Each board contains insulated standoffs to maintain the required clearance between adjacent modules and prevent shorting of wire wrap pins. A helpful alphanumeric X-Y grid pattern is also etched onto each board to facilitate ease in wire wrap pin location and identification.

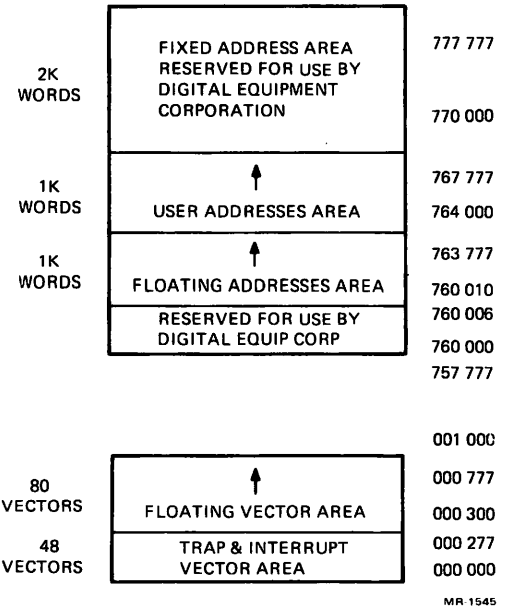
Table 1 W9500 Series Modules

Module No.	Description
W9511	Quad height, extended length, single width module with extractor handle. No DIP sockets included. One 40-pin male cable connector premounted on board and space for additional 40-pin connector provided.
W9514	Same as W9511 except with 58 premounted DIP sockets.
W9512	Double height, extended length, single width module with flip chip handle. No DIP sockets included. One 40-pin male cable connector premounted on board.
W9515	Same as W9512 except with 25 premounted DIP sockets.

APPENDIX A

ASSIGNMENT OF ADDRESSES AND VECTORS

ADDRESS MAP



FLOATING VECTORS

The conventions for the assignments of floating vectors for modules on the LSI-11 bus will adhere to those established for UNIBUS devices. UNIBUS devices are used to explain the priority ranking for floating vectors and are included in the subsequent table of trap and interrupt vectors as a guide to the user.

The floating vector convention used for communications and for devices that interface with the PDP-11 series of products assigns vectors sequentially starting at 300 and proceeding upward to 777. (Some LSI-11 bus modules, such as the DLV11 and DRV11, have an upper vector limit of 377). The following table shows the sequence for assigning vectors to modules. It can be seen that the first vector address, 300, is

assigned to the first DLV11 in the system. If another DLV11 is used, it would then be assigned vector address 310, etc. When the vector addresses have been assigned to all the DLV11s (up to a maximum of 32), addresses are then assigned consecutively to each unit of the next highest ranked device (DRV11 or DLV11-E, etc.), then to the other devices according to their rank.

Ranking for Floating Vectors
(Start at 300 and proceed upward.)

Rank	UNIBUS	LSI-11 Bus
1	DC11	
2	KL11, DL11-A, -B	DLV11, -F, -J
3	DP11	
4	DM11-A	
5	DN11	
6	DM11-BB	
7	DR11-A	DRV11-B
8	DR11-C	DRV11
9	PA611 Reader	
10	PA611 Punch	
11	DT11	
12	DX11	
13	DL11-C, -D, -E	DLV11-E
14	DJ11	
15	DH11	
16	GT40	
17	LPS11	
18	DQ11	
19	KW11-W	KWV11
20	DU11	DUV11

INTERRUPT AND TRAP VECTORS

Vector	UNIBUS	LSI-11 Bus
000	DEC reserved	DEC reserved
004	CPU errors	Bus time-out and illegal in-
.		structions (e.g., JMP R0)
.		(odd address and stack
.		overflow traps not

APPENDIX A

INTERRUPT AND TRAP VECTORS (Cont)

Vector	UNIBUS	LSI-11 Bus
.		implemented on LSI-11)
010	Illegal and reserved	Illegal and reserved
.	instructions	instructions
014	BPT, breakpoint trap	BPT instruction and T bit
020	IOT, input/output trap	IOT instruction
024	Power-fail	Power-fail
030	EMT, emulator trap	EMT instruction
034	TRAP instruction	TRAP instruction
040	System software	
044	System software	
050	System software	
054	System software	
060	Console terminal,	Console terminal, input
.	keyboard/reader	
064	Console terminal,	Console terminal, output
.	printer/punch	
070	PC11, paper tape reader	
074	PC11, paper tape punch	
100	KW11-L, line clock	External event line interrupt
104	KW11-P, programmable clock	
110		
114	Memory system errors	
120	XY plotter	
124	DR11-B DMA interface;	DRV11-B
.	(DA11-B)	
130	AD01, A/D subsystem	
134	AFC11, analog subsystem	
140	AA11, display	
144	AA11, light pen	
150		
154		
160	RL11	RLV11
164		
170	User reserved	
174	User reserved	
200	LP11/LS11, line printer;	LAV11, LPV11
.	LA180	
204	RS04/RF11, fixed head disk	

APPENDIX A

INTERRUPT AND TRAP VECTORS (Cont)

Vector	UNIBUS	LSI-11 Bus
210	RC11, disk	
214	TC11, DECtape	
220	RK11, disk	RKV11
224	TU16/TM11/TS03, magnetic tape	
230	CD11-CM11-CR11, card reader	
234	UDC11, digital control subsystem	
240	PIRQ, program interrupt request (11/45)	
244	Floating-point error	FIS (optional)
250	Memory management	
254	RP04/RP11 disk pack	
260	TA11, cassette	
264	RX11, floppy disk	RXV11, RXV21
270	User reserved	User reserved
274	User reserved	
300	(Start of floating vectors)	
.		
.		
374		
400		
404		ADV11-A
410		
414		
420		
424		IBV11-A
430		
434		
440		
444		KWV11-A
450		
.		User reserved
.		
.		
777	(End of floating vectors)	

APPENDIX A

FLOATING ADDRESSES

The conventions for the assignment of floating addresses for modules on the LSI-11 bus are the same as UNIBUS devices. UNIBUS devices are used to explain the ranking sequence.

The floating address convention used for communications and for other devices that interface with the PDP-11 series of products assigns addresses sequentially starting at 760 010 (or 160 010) and proceeds upward to 763 776 (or 163 776). For compatiblity with UNIBUS convention, addresses are expressed as consisting of 18 bits (7XX XXX) rather than 16 bits (1XX XXX).

Floating addresses are assigned in the following sequence:

Rank	UNIBUS Device	LSI-11 Device
1	DJ11	
2	DH11	
3	DQ11	
4	DU11	DUV11
5	DUP11	
6	LK11A	
7	DMC11	
8	DZ11	DZV11
9	KMC11	
10	RL11 (extras)	RLV11 (extras)

DEVICE ADDRESSES

Address	UNIBUS	LSI-11 Bus
777 776	Processor status word (PS)	
777 774	Stack limit	
777 772	Program interrupt request (PIRQ)	
777 770	DIGITAL reserved	
.		
.		
.		
777 720		

APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS	LSI-11 Bus
777 716	CPU Registers	
.		
.		
.		
777 710		
777 707	R7 (PC)	
777 706	R6 (SP)	
777 705	R5	
777 704	R4 — General Registers	
777 703	R3	
777 702	R2	
777 701	R1	
777 700	R0	
777 676	Memory management	
.		
.		
.		
777 600		
777 576		(SR2)
777 574	Memory mgt status register	(SR1)
777 572		(SR0)
777 570	Console switch and display register	
777 566	(XBUF) — Console Terminal	Console Terminal
777 564	(XCSR)	
777 562	(RBUF)	
777 560	(RCSR)	
777 556	PC11/PR11	
777 554		
777 552		
777 550		
777 546	KW11-L, DL11-W	(LTC) KPV11 BDV11
777 544	XY11	
.		
.		
.		
777 530		
777 526	Unassigned	

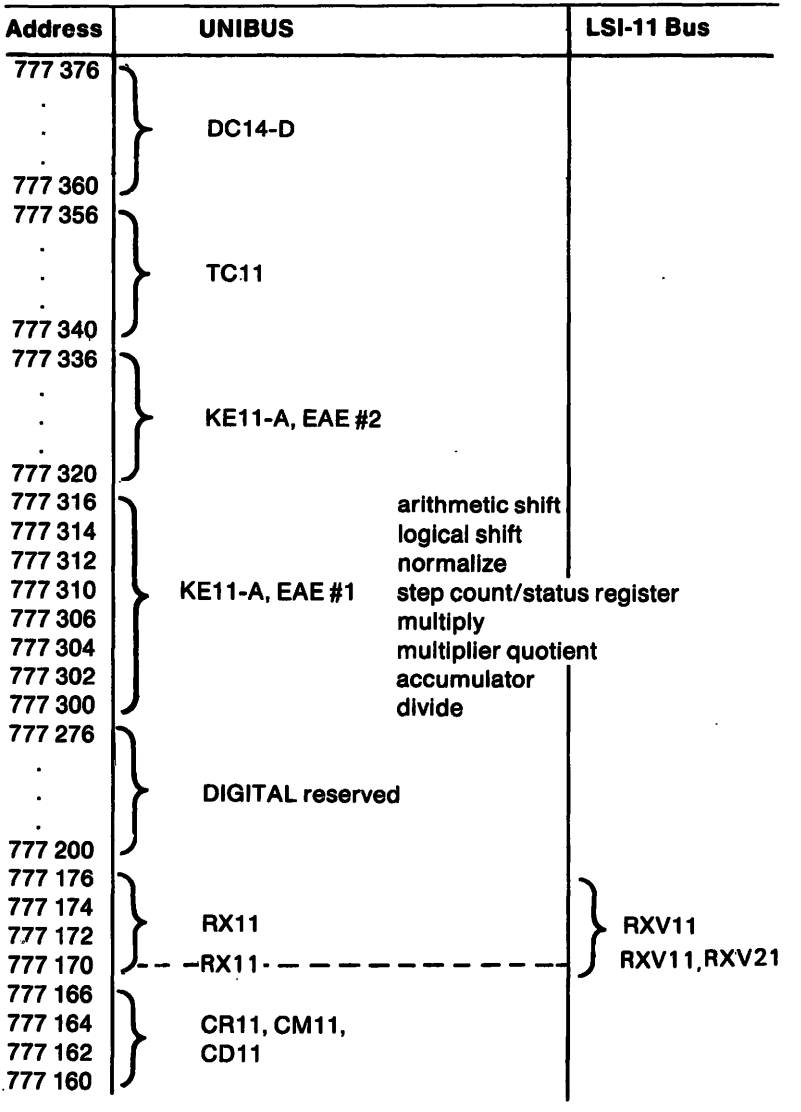
APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS		LSI-11 Bus
777 524			
777 522	Unassigned		BDV11
777 520			
777 516	LA180, LP11		
777 514	LS11, LV11		LAV11, LPV11
777 512			
777 510			
777 506			
.			
.	TA11		
.			
777 500			
777 476			
.			
.	RF11		
.			
777 460			
777 456			
.			
.	RC11		
.			
777 440			
777 436		#8	
777 434		#7	
777 432		#6	
777 430	DT11, bus switch	#5	
777 426		#4	
777 424		#3	
777 422		#2	
777 420		#1	
777 416			
.			
.	RK11		RKV11
.			
777 400			

APPENDIX A

DEVICE ADDRESSES (Cont.)



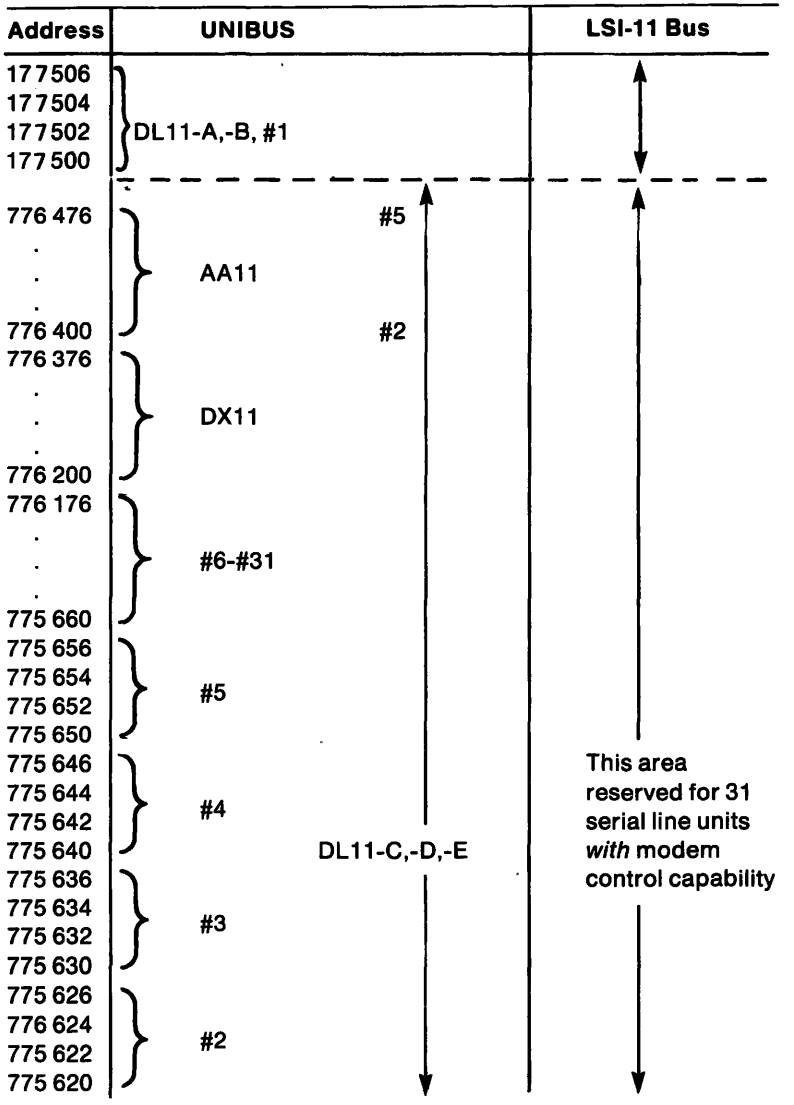
APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS	LSI-11 Bus
777 156 ... 777 000	DIGITAL reserved	
776 776 ... 776 770	AD01	
776 766 ... 776 750	AA11 #1	
776 746 ... 776 740	Unassigned	
776 736 ... 776 700	RP11	
776 676 ... 177 530	DL11-A, -B #4-#16	This area reserved for 16 serial line units *without* modem control capability
177 526 177 524 177 522 177 520	DL11-A,-B, #3	
177 516 177 514 177 512 177 510	DL11-A,-B #2	

APPENDIX A

DEVICE ADDRESSES (Cont.)



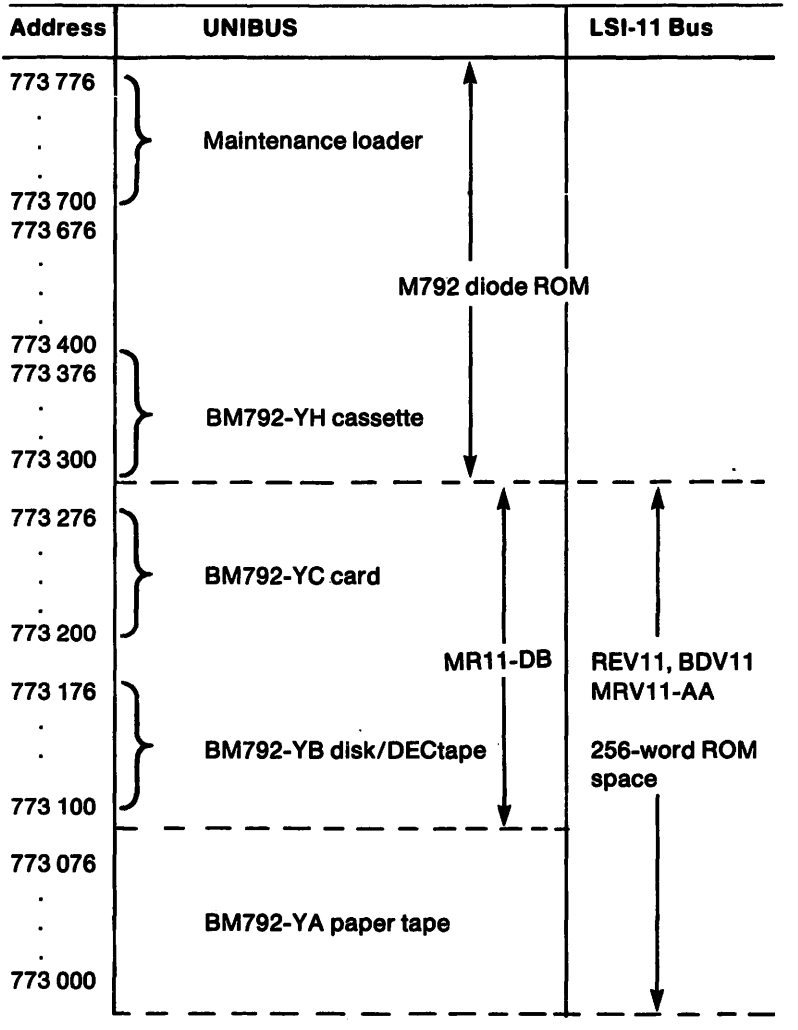
APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS		LSI-11 Bus
775 616 775 614 775 612 775 610	#1		
775 606 775 604 775 602 775 600	DIGITAL reserved		
776 576 . . . 775 400	DS11	#4 #1	
775 376 . . . 775 200	DN11	#16 #1	
775 176 . . . 775 000	DM11	#15 #1	
774 776 . . . 774 410	DP11	#1	
774 406 774 404 774 402 774 400	DP11 RL01	 #32	RLV11
774 376 . . . 774 000	DC11	#32 #1	

APPENDIX A

DEVICE ADDRESSES (Cont.)



DEVICE ADDRESSES (Cont.)

Address	UNIBUS	LSI-11 Bus
772 776 . . . 772 700	PA611 typeset punch	
772 676 . . . 772 600	PA611 typeset reader	
772 576 772 574 772 572 772 570 772 566	AFC11	
. . . 772 560	DIGITAL reserved	
772 556 . . . 772 550	DIGITAL reserved	
772 546 772 544 772 542 772 540	KW11-P	
772 536 772 534 772 532 772 530 772 526 772 524 772 522 772 520	TM11	

APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS	LSI-11 Bus
772 516	Memory mgt status register (SR3)	
772 514		
.		
.	OST	
.		
772 500		
772 456		
.		
.	DR11-B, #3	
.		
772 450		
772 446		
.		
.	TJU16	
.		
772 440		
772 436		
772 434		
772 432	DR11-B, #2	DRV11-B, #3
772 430		
772 426		
772 424		
772 422	DIGITAL reserved	DRV11-B, #2
772 420		
772 416		
772 414		
772 412	DR11-B,-C, #1	DRV11-B, #1
772 410		
772 406		
.		
.	KW11-W	
.		
772 400		
772 376		
.		
.	Memory management	
.		
772 200		

APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS	LSI-11 Bus
772 176 . . . 772 160	FP11	
772 156 . . . 772 140	Unassigned	
772 136 . . . 772 110	Memory parity	
772 106 . . . 772 102	Unassigned	
772 100	MS11-K, -LP, MM11-LP	
772 076 . . . 772 070	RL11	
772 066 . . . 772 040	RJS04	
772 036 . . . 772 020	DIGITAL reserved	

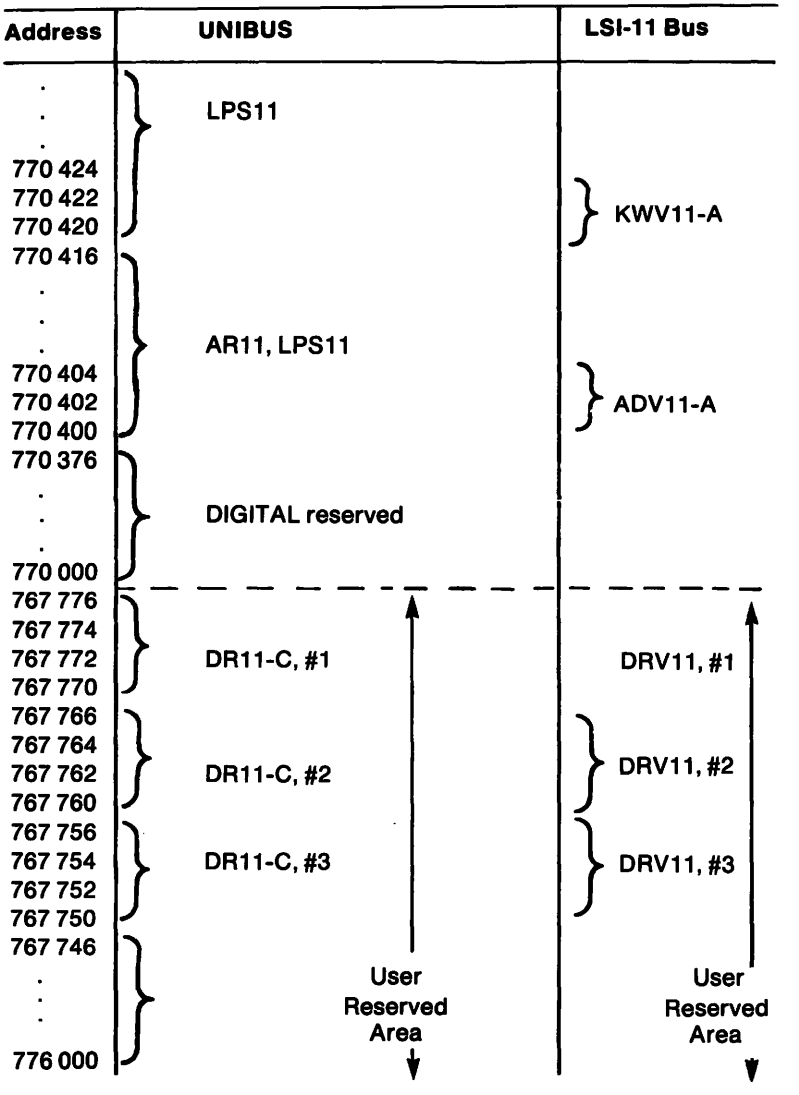
APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS	LSI-11 Bus
772 016 . . . 772 000	GT40, VT48	
771 776 . . . 771 000	UDC functional I/O modules	
770 776 . . . 770 700	KG11 #8 #1	
770 676 . . . 770 500	DM11-BB #16 #1	
770 476 . . . 770 460	ADF11	
770 456 . . . 770 450	Unassigned	
770 446 770 444 770 442 770 440 770 436	LPS11	AAV11-A

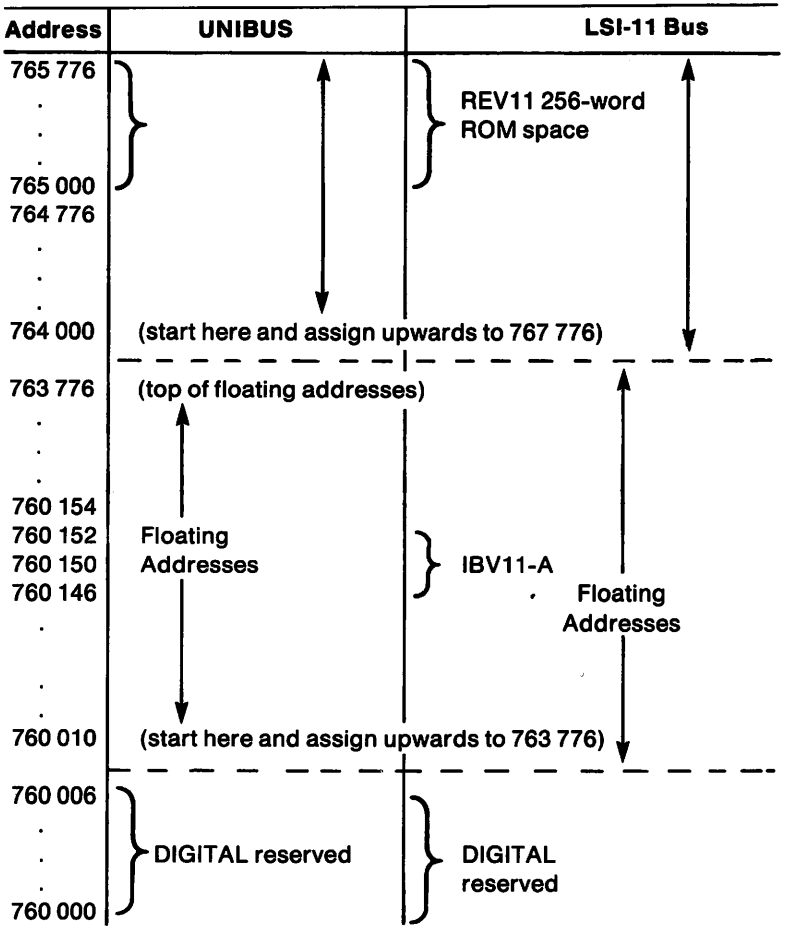
APPENDIX A

DEVICE ADDRESSES (Cont.)



APPENDIX A

DEVICE ADDRESSES (Cont.)



APPENDIX B

LSI-11 BUS SIGNALS

MODULE CONTACT FINGER DESIGNATION

DIGITAL interface modules all use the same contact finger (pin) identification system. The LSI-11 I/O bus is based on the use of double-height modules. These modules plug into a 2-slot bus connector, each containing 36 lines per slot (18 each on component and solder sides of the circuit board). Although the LSI-11 processor module and core memory modules are quad-height modules that plug into four connector slots, only two slots (A and B) are used for interface purposes on the processor module. Etched circuit jumpers on the unused portion of the module maintain continuity of grant signals BIAKI L to BIAKO L and BDMGI L to BDMGO L. These daisy-chained signals are described later.

Slots, shown as Row A and Row B in Figure 1, include a numeric identifier for the side of the module. The component side is designated side "1" and the solder side is designated side "2." Letters ranging from A through V (excluding G, I, O, Q) identify a particular pin on a side of a slot. Hence, a typical pin is designated as:

BE2

Slot (Row) Identifier "Slot B"

Pin Identifier "Pin E"

Module-Side Identifier "solder side"

Note that the positioning notch between the two rows of pins mates with a protrusion on the connector block for correct module positioning.

Quad-height modules are similarly pin numbered. They are identified in Figure 2.

Individual connector pins, viewed from the underside (wiring side) of a backplane, are identified as shown in Figure 3. Only the pins for one bus location (two slots) are shown in detail. This pattern of pins is repeated eight times on the H9270 backplane, allowing the user to install one LSI-11 microcomputer module (four slots) and up to six additional 2-slot modules.

APPENDIX B

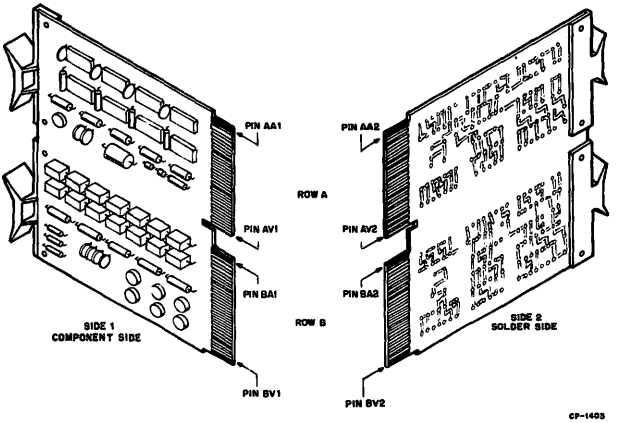


Figure 1 Dual Module Contact Finger Identification

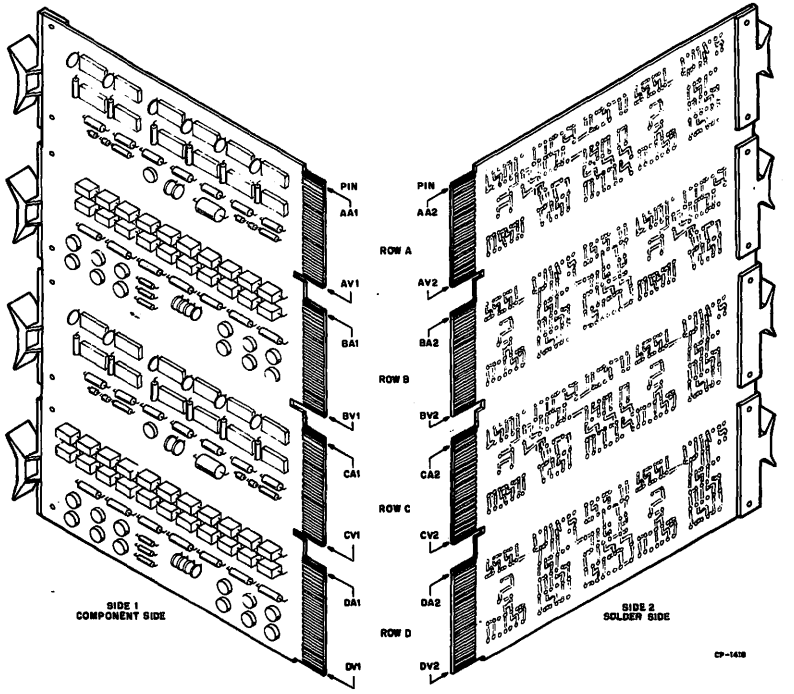


Figure 2 Quad Module Contact Finger Identification

APPENDIX B

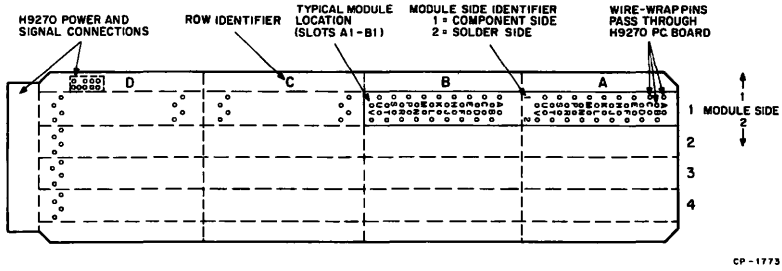


Figure 3 LSI-11 Backplane Module Pin Identification

BUS SIGNALS

H9270 backplane pin assignments are listed and described in Table 1. Only slots A and B are listed. However, they are identical to slots C and D respectively. Table 2 alphanumerically lists the LSI-11 bus pin assignments.

Table 1 Backplane Pin Assignments

Bus Pins	Mnemonic	Description
AA1 AB1	BIRQ5 L BIRQ6 L	Interrupt Request priority level 5 Interrupt Request priority level 6
AC1 AD1	BDAL16 BDAL17	Extended address bits.
AE1 AF1 AH1	SSPARE1 SSPARE2 SSPARE3	Special Spare (not assigned, not bused; available for user interconnections).
AJ1	GND	Ground—system signal ground and dc return.
AK1 AL1	MSPAREA MSPAREA	Maintenance Spare—normally connected together on the backplane at each option location (not bussed connection).

APPENDIX B

AM1	GND	Ground—system signal ground and dc return.
AN1	BDMR L	Direct Memory Access (DMA) Request—a device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not the bus master (it has completed a bus cycle and BSYNC L is not being asser.@1 by the processor), it grants bus mastership to the requesting device by asserting BDMGO L. The device responds by negating BDMR L and asserting BSACK L.
AP1	BHALT L	Processor Halt—when BHALT L is asserted,the processor responds by halting normal program execution. External interrupts are ignored but memory refresh interrupts (enabled if W4 on the processor module is removed) and DMA request/grant sequences are enabled. When in the halt state, the processor executes the ODT microcode and the console device operation is invoked.
AR1	BREF L	Memory Refresh—asserted by a processor microcode-generated refresh interrupt sequence (when enabled) or by an external device. This signal forces all dynamic MOS memory units to be activated for each BSYNC L/BDIN L bus transaction.

APPENDIX B

		CAUTION The user must avoid multiple DMA data transfers (burst or "hog" mode) during a processor-generated refresh operation so that a complete refresh cycle can occur once every 16 ms.
AS1	+12B	+12V Battery Power—secondary +12V power connection. Battery power can be used with certain devices.
AT1	GND	Ground—system signal ground and dc return.
AU1	PSPARE1	Spare (not assigned, customer usage not recommended).
AV1	+5B	+5V Battery Power—secondary +5V power connection. Battery power can be used with certain devices.
BA1	BDCOK H	DC Power OK—power supply-generated signal that is asserted when there is sufficient dc voltage available to sustain reliable system operation.
BB1	BPOK H	Power OK—asserted by the power supply when primary power is normal. When negated during processor operation, a power-fail trap sequence is initiated.
BC1 BD1 BE1 BF1 BH1	SSPARE4 SSPARE5 SSPARE6 SSPARE7 SSPARE8	Special Spare (not assigned, not bused; available for user interconnections).

APPENDIX B

BJ1	GND	Ground—system signal ground and dc return.
BK1 BL1	MSPAREB MSPAREB	Maintenance Spare—normally connected together on the backplane at each option location (not a bused connection).
BM1	GND	Ground—system signal ground and dc return.
BN1	BSACK L	This signal is asserted by a DMA device in response to the processor's BDMGO L signal, indicating that the DMA device is bus master.
BP1	BIRQ7 L	Interrupt request priority level 7
BR1	BEVNT L	External Event Interrupt Request—when asserted, the processor responds (if PS bit 7 is 0) by entering a service routine via vector address 100_8. A typical use of this signal is a line-time clock interrupt.
BS1	PSPARE4	Spare (not assigned; customer usage not recommended).
BT1	GND	Ground—system signal ground and dc return.
BU1	PSPARE2	Spare (not assigned; customer usage not recommended).
BV1	+5	+5V Power—normal +5 Vdc system power.
AA2	+5	+5V Power—normal +5 Vdc system power.
AB2	−12	−12V Power—−12 Vdc (optional) power for devices requiring this voltage.

APPENDIX B

		NOTE LSI-11 modules which require negative voltages contain an inverter circuit (on each module) which generates the required voltage(s); hence, −12 V power is not required with DIGITAL-supplied options.
AC2	GND	Ground—system signal ground and dc return.
AD2	+12	+12V Power—+12 Vdc system power.
AE2	BDOUT L	Data Output—BDOUT, when asserted, implies that valid data is available on BDAL0-15 L and that an output transfer, with respect to the bus master device, is taking place. BDOUT L is deskewed with respect to data on the bus. The slave device responding to the BDOUT L signal must assert BRPLY L to complete the transfer.
AF2	BRPLY L	Reply—BRPLY L is asserted in response to BDIN L or BDOUT L and during IAK transactions. It is generated by a slave device to indicate that it has placed its data on the BDAL bus or that is has accepted output data from the bus.
AH2	BDIN L	Data Input—BDIN L is used for two types of bus operation: 1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master, and requires a re-

		sponse (BRPLY L). BDIN L is asserted when the master device is ready to accept data from a slave device. 2. When asserted without BSYNC L, it indicates that an interrupt operation is occurring. The master device must deskew input data from BRPLY L.
AJ2	BSYNC L	Synchronize—BSYNC L is asserted by the bus master device to indicate that it has placed an address on BDAL0-17 L. The transfer is in process until BSYNC L is negated.
AK2	BWTBT L	Write/Byte—BWTBT L is used in two ways to control the bus cycle: 1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow (DATO or DATOB), rather than an input sequence. 2. It is asserted during BDOUT L, in a DATOB bus cycle, for byte addressing.
AL2	BIRQ4 L	Interrupt Request—A device asserts this signal when its interrupt enable and interrupt request flip-flops are set. If the processor's PS word bit 7 is 0, the processor responds by acknowledging the request by asserting BDIN L and BIAKO L.

AM2 AN2	BIAKI L BIAKO L	Interrupt Acknowledge Input and Interrupt Acknowledge Output—this is an interrupt acknowledge signal which is generated by the processor in response to an interrupt request (BIRQ L). The processor asserts BIAKO L, which is routed to the BIAKI L pin of the first device on the bus. If it is requesting an interrupt, it will inhibit passing BIAKO L. If it is not asserting BIRQ L, the device will pass BIAKI L to the next (lower priority) device via its BIAKO L pin and the lower priority device's BIAKI L pin.
AP2	BBS7 L	Bank 7 Select—The bus master asserts BBS7 L when an address in the upper 4K word bank is placed on the bus. BSYNC L is then asserted and BBS7 L remains active for the duration of the addressing portion of the bus cycle.
AR2 AS2	BDMGI L BDMGO L	DMA Grant Input and DMA Grant Output—This is the processor-generated daisy-chained signal which grants bus mastership to the highest priority DMA device along the bus. The processor generates BDMGO L, which is routed to the BDMGI L pin of the first device on the bus. If it is requesting the bus, it will inhibit passing BDMGO L. If it is not requesting the bus, it will pass the BDMGI L signal to the next (lower priority) device via its BDMGO L pin. The device as-

		serting BDMR L is the device requesting the bus, and it responds to the BDMGI L signal by negating BDMR, asserting BSACK L, assuming bus mastership, and executing the required bus cycle. **CAUTION** DMA device transfers must be single transfers and must not interfere with the memory refresh cycle.
AT2	BINIT L	Initialize—BINIT L is asserted by the processor to initialize or clear all devices connected to the I/O bus. The signal is generated in response to a power-up condition (the negated condition of BDCOK H).
AU2 AV2	BDAL0 L BDAL1L	Data/Address Lines—These two lines are part of the data/address bus over which address and data information are communicated. Address information is first placed on the bus by the bus master device. The same device then either receives input data from, or outputs data to, the addressed slave device or memory over the same bus lines.
BA2	+5	+5V Power—normal +5 Vdc system power.
BB2	−12	−12V Power—−12 Vdc (optional) power for devices requiring this voltage.
BC2	GND	Ground—system signal ground and dc return.

APPENDIX B

BD2	+12	+12V Power—+12 Vdc system power.
BE2	BDAL2 L	Data/Address Lines—These 14 lines are part of the data/address bus previously described.
BF2	BDAL3 L	
BH2	BDAL4 L	
BJ2	BDAL5 L	
BK2	BDAL6 L	
BL2	BDAL7 L	
BM2	BDAL8 L	
BN2	BDAL9 L	
BP2	BDAL10 L	
BR2	BDAL11 L	
BS2	BDAL12 L	
BT2	BDAL13 L	
BU2	BDAL14 L	
BV2	BDAL15 L	

APPENDIX C

NOMENCLATURE FOR CIRCUIT SCHEMATICS

BASIC SIGNAL NAMES

Signal names on DIGITAL print sets are in the following form:

SOURCE (ASSERTION) SIGNAL NAME (STATE) POLARITY

SOURCE indicates the drawing number of the print from which the signal originates. The drawing number of a print is located in the lower right corner of the print title block (D1, D2, D3, etc.).

ASSERTION is either blank or a NOT sign. A blank indicates reference to the asserted state (the true state) of the signal; a NOT sign indicates reference to the negated state (the false state) of the signal. Signals originating from flip-flops do not use the NOT sign to indicate *assertion;* instead, they use a 1 or 0 in parentheses following the signal name for assertion indication.

SIGNAL NAME is the proper name of the signal. The names used on the print are also in this manual for correlation between the two.

STATE is present when the signal source is a flip-flop; it is either 0 or 1.

POLARITY is either H or L to indicate the voltage level of the signal; H means +3V; L means ground.

For example, the signal

D5 TX DONE H

originates on sheet 5 of the drawings and is read "when TX DONE is true, this signal is at +3V."

LSI-11 bus signal lines carry a dual source indicator. These signal names represent a bidirectional wire-ORed bus; as a result, multiple sources for a particular bus signal exist.

FLIP-FLOP SIGNAL NAMES

Flip-flop signal names add an extra dimension. Although flip-flops have only two outputs, four signal names are possible (Figure 1). The two real outputs are RX DONE (1) H on pin 5 and RX DONE (0) H on pin 6. The two additional outputs are simply the two real outputs reidentified. RX DONE (1) L is electrically the same as RX DONE (0) H and RX DONE (0) L is electrically the same as RX DONE (1) H. For example,

the signal RX DONE (0) L is read "when the RX DONE flip-flop is clear (holding a zero), this signal is at ground."

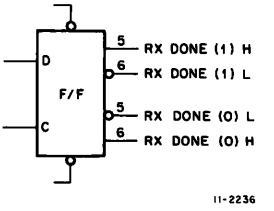


Figure 1 Flip-Flop Signal Names

APPENDIX D

ASYNCHRONOUS SERIAL LINE UNIT (SLU) COMPARISONS

The characteristics listed in Tables 1, 2, and 3 compare the different members of the DLV11 (LSI-11 bus) and DL11 (UNIBUS) families of asynchronous serial line products. All modules of the DLV11 series are dual-height modules. The DLV11-E, -F, and -J modules detect overrun conditions which are reported in the receiver CSR. These modules will not generate phantom interrupts on overrun.

DLV11-J

Each of the four serial ports on this module are separate and independent from the others. This is *not* a multiplexed module. Each port has its own CSRs, data buffers, interrupt vectors, baud rates, UARTs, etc. The net effect of this module is to achieve a 4:1 compression ratio over the DLV11. The main functional difference between the ports of the DLV11-J and the DLV11 is that the DLV11-J provides an RS-232C-compatible interface (using RS-422 and RS-423) only and requires the DLV11-KA module (one per port) to accommodate the 110 baud, 20 mA current loop interface.

DLV11-E

This module is functionally equivalent to the DL11-E except that it has programmable baud rates. This module provides one serial port that has full modem control.

DLV11-F

This module is functionally equivalent to the DL11-F except that it has programmable baud rates. This module will eventually replace the DLV11.

DZV11-B

The DZV11-B is a multiplexer interface between four asynchronous serial data communication channels and the LSI-11 bus. The DZV11-B provides EIA level conversion and full modem control suitable for support of Bell series 103, 202, or equivalent modems. Program compatibility is maintained with the UNIBUS option, DZ11-A. The only compatibility exception is the number of serial channels supported. As a product enhancement feature, additional modem control leads are supported to allow half-duplex operation on switched-network-type lines.

MXV11-A

This multifunction module consists of two serial ports, RAM and ROM memory, and a 60 Hz clock. The two serial ports are RS-423 (RS-232-C-compatible, data leads only) The MXV11-A has two completely separate serial ports, where each port has its own CSRs, data buffers, baud rate generation, etc.

Table 1 Comparison of Hardware Features

	Unibus					LSI-11 bus						
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KA	DZV11-B	MXV11-A
No. of ports per module	1	1	1	1	1	1	1	1	4	1	4	2
EIA RS-232C												
Full modem control					X		X				X	
Limited modem interface		X		X		X		X	X			X
EIA RS-423, RS-422												
Data leads only									X			**
20 mA current loop												
RCVR active or passive						X		X	*	X		
XMIT active or passive						X		X	*	X		
XMIT active only	X	X	X	X								

* The external 20 mA option (DLV11-KB) is required to implement this function.

† Optional feature.

‡ Applies only to the port assigned to the console Device.

§ The loop-back cable is required to implement this function.

| 110 baud only.

** RS-423 only

	Unibus					LSI-11 bus						
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KA	DZV11-B	MXV11-A
CCITT		X		X	X						X	
Halt on framing error†						X	X	X	‡			‡
Boot on framing error†							X	X	‡			‡
Baud rates (Table 3)												
Programmable							X	X			X	
On-board clocks for split speed	X	X	X	X	X		X	X			X	
Reader run control	X		X			X		X	*			
Error flags	X	X	X	X	X		X	X			X	

* The external 20 mA option (DLV11-KB) is required to implement this function.

† Optional feature.

‡ Applies only to the port assigned to the console Device.

§ The loop-back cable is required to implement this function.

| 110 baud only.

	Unibus					LSI-11 bus						
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KA	DZV11-B	MXV11-A
Break generation bit	X	X	X	X	X	X	X	X	X		X	X
Receiver active bit	X	X	X	X	X		X	X				
Maintenace bit	X	X	X	X	X	§	X	X	§		X	§
UART cleared by INIT	X	X	X	X	X		X	X	X			
UART cleared by DCOK						X			X			
No trap on write to input buffer	X	X	X	X	X		X	X				

* The external 20 mA option (DLV11-KB) is required to implement this function.

† Optional feature.

‡ Applies only to the port assigned to the console Device.

§ The loop-back cable is required to implement this function.

| 110 baud only.

	Unibus					LSI-11 bus						
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KA	DZV11-B	MXV11-A
Easy configuration using wire-wrap jumpers							X	X	X			X
Stop bits												
1			X	X	X	X	X	X	X		X	X
1.5			X	X	X						X	
2	X	X	X	X	X	X	|	|	X		X	X

* The external 20 mA option (DLV11-KB) is required to implement this function.

† Optional feature.

‡ Applies only to the port assigned to the console Device.

§ The loop-back cable is required to implement this function.

| 110 baud only.

Table 2 Baud Rates

Baud Rate	Unibus					LSI-11 bus						
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KA	DZV11-B	MXV11-A
50	X	X	X	X	X	X	X	X			X	
75	X	X	X	X	X	X	X	X			X	
110	X	X	X	X	X	X	X	X	*		X	
134.5			X	X	X	X	X	X			X	
150	X	X	X	X	X	X	X	X	X		X	X
200			X	X	X	X						
300	X	X	X	X	X	X	X	X	X		X	X
600	X	X	X	X	X	X	X	X	X		X	
1200	X	X	X	X	X	X	X	X	X		X	X
1800	X	X	X	X	X	X	X	X			X	
2000							X	X			X	
2400	X	X	X	X	X	X	X	X	X		X	X
3600							X	X			X	
4800			X	X	X	X	X	X	X		X	X
7200			X	X	X		X	X			X	
9600			X	X	X	X	X	X	X		X	X
19200							X	X	X			X
38,400									X			X
External						X		X	X	X		

* The external 20 mA option (DLV11-KB) is required to implement this function.

Table 3 Comparison of Software Features

			Unibus					LSI-11 bus				
			DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	MXV11-A
Register	**Bit**	**Name**										
RCSR	15	Data Set Status/ Interrupt					X					
	14	Ring				X		X				
	13	CTS					X		X			
	12	CD					X		X			
	11	Receiver Active	X	X	X	X	X		X	X		
	10	2d Receive					X		X			
	9,8,4	Unused	X	X	X	X	X	X	X	X	X	X
	7	Receive Done	X	X	X	X	X	X	X	X	X	X
	6	Receive Int Enb	X	X	X	X	X	X	X	X	X	X
	5	Data Set Int Enb					X		X			
	3	2d XMT					X		X			
	2	RTS					X		X			
	1	PTR					X		X			
	0	Rdr Enable	X		X			X		X	*	

* The external 20 mA option (DLV11-KB) is required to implement this funtion.

Register			Unibus					LSI-11 bus				
			DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	MXV11-A
RBUF	15	Error			X	X			X	X	X	X
	14	OE			X	X	X		X	X	X	X
	13	FE			X	X	X		X	X	X	X
	12	PE			X	X	X		X	X	X	X
	11-8	Unused	X	X	X	X	X	X	X	X	X	X
	7-0	Receive Data	X	X	X	X	X	X	X	X	X	X
XCSR	15-8	Unused	X	X	X	X	X	X	X	X	X	X
	7	XMT Ready	X	X	X	X	X	X	X	X	X	X
	6	XMT Int Enb	X	X	X	X	X	X	X	X	X	
	5-3,1	Unused	X	X	X	X	X	X	X	X	X	X
	2	Maintenance	X	X	X	X	X	*	X	X	*	*
	0	XMT Break			X	X	X	X	X	X	X	X
XBUF	15-8	Unused	X	X	X	X	X	X	X	X	X	X
	7-0	XMT BUF	X	X	X	X	X	X	X	X	X	X

* The external 20 mA option (DLV11-KB) is required to implement this funtion.

APPENDIX E

COMPARISON OF DATA TRANSMISSION TECHNIQUES

Frequently, the application arises where a data transmission path has to be established between two devices. Usually the distance between the device is known and also the rate of data transmission. The problem is deciding which is the best communication technique to use to interconnect the devices.

Figure 1 is a graph of data versus distance for the various standard transmission techniques. Parallel data transmission techniques (PLUs and DMA) give the highest data rate; however, they are good only for relatively short distances. The serial techniques (RS-232C, RS-422 and current loops) are good for longer distances but at limited data rates.

While analyzing Figure 1, remember that the axes are logarithmic and that the data in words per second rather than baud rate. The limits established for distance and data rate are a function of both the inherent limitations of the transmission technique and of the DIGITAL device used to do the interconnection. As an example, look at the 422 section of the graph. Maximum distance is 4000 feet as established by EIA standard RS-422, but the maximum data rate of 1920 words per second is based on the maximum baud rate of the DLV11-J which is 38.4K baud.

Table 1 is a summary of the LSI-11 bus and UNIBUS devices which can be used with each communication technique. Currently, there is no UNIBUS device for EIA RS-422.

APPENDIX E

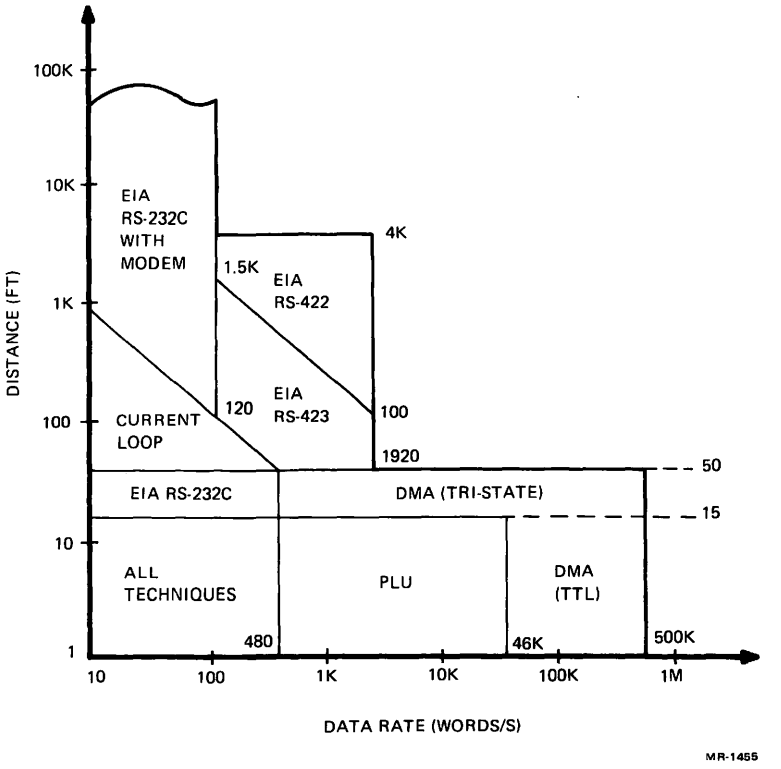


Figure 1 Data Rate vs Distance with DIGITAL Devices

Table 1 Communication Techniques

	LSI-11	UNIBUS
Loop	DLV11	DL11-C
EIA (RS-232C)	DLV11	DL11-D
EIA with Modem	DLV11-E	DL11-E
RS422, RS423	DLV11-J	—
PLU	DRV11	DR11-C
DMA	DRV11-B	DR11-B

APPENDIX E

NOTES AND ASSUMPTIONS FOR FIGURE 1

1. Data Rate Definition
   a. One word equals 16 bits.
   b. For serial techniques, one word equals two characters formatted with one start bit, eight data bits, and one stop bit. Asynchronous serial transmission is assumed.
2. Serial Line Maximum Data Rate
   a. Modems were limited to 120 words/sec (2400 baud) because modems with higher rates cost more than LSI-11 systems usually warrant. Higher data rate modems are generally synchronous rather than asynchronous.
   b. 480 words/sec is equal to 9600 baud, the limit of the DLV11 SLU.
   c. 1920 words/sec is equal to 38.4 baud, the limit of DLV11-J SLU.
3. PLU (Parallel Line Unit) Limits
   a. The TTL inputs/outputs of the DRV11 limit the distance to 15 feet.
   b. 46K words/sec assumes non-interrupt-driven program servicing with bit testing (TSTB, BMI, MOV and SOB). 97K words/sec is maximum rate with program servicing without bit testing (MOV and BR). With interrupt-driven servicing, the maximum limit is 20K words/sec assuming 50 μs for interrupt latency and software servicing of interrupt.
4. DMA (Direct Memory Access) Limits
   a. The DRV11-B can be used up to 50 feet because it has tri-state drivers and receivers. The distance is limited to 15 feet with TTL devices like the DR11-B.
   b. DMA transfer with the DRV11-B and the DR11-B are limited to 500K words/sec in burst mode operation; 250K words/sec is the limit for single-cycle mode operation with either device. These limits are device-dependent, not LSI-11 bus-dependent. Note that burst mode can disrupt memory refreshing if bus refreshing (DMA and microcode) is used. Self-refreshing memories (MSV11-CD or MSV11-D) eliminate this problem.

APPENDIX F

INTEGRATED CIRCUITS

Bus Receivers and Bus Drivers

The equivalent circuits of LSI-11 bus-compatible drivers and receivers are shown in Figure 1. To perform the receiver and driver functions, Digital Equipment Corporation uses two monolithic integrated circuits with the characteristics listed in Table 1. A typical bus driver circuit is shown in Figure 2. Note that 8641 quad transceivers can be used, combining LSI-11 bus receiver and driver functions in a single package. Bus receiver (8640), bus driver (8881), and bus transceivers (8641) are shown in Figures 3, 4, and 5, respectively.

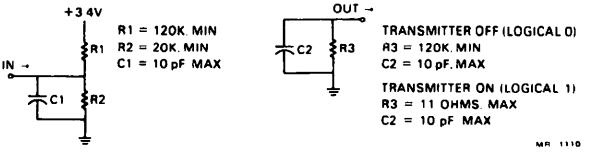


Figure 1 Bus Driver and Receiver Equivalent Circuits

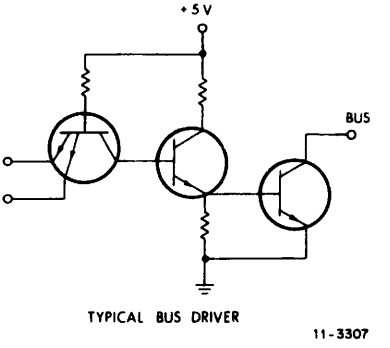


Figure 2 Typical Bus Driver Circuit

APPENDIX F

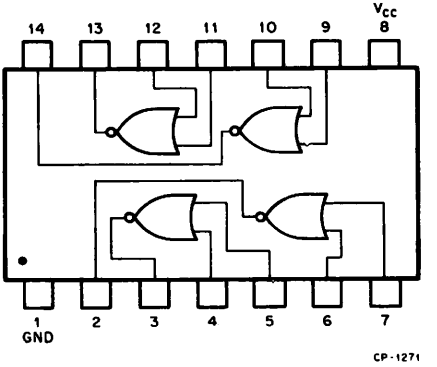


Figure 3 8640 Quad 2-Input NOR Gates (Bus Receiver)

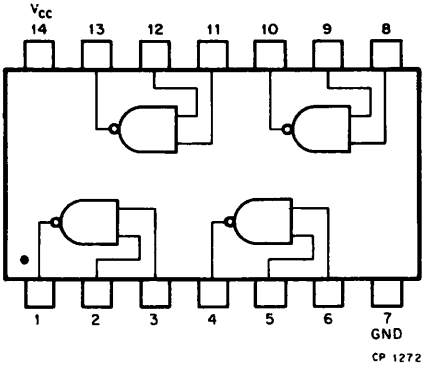


Figure 4 8881 Quad 2-Input NAND Gate (Bus Driver)

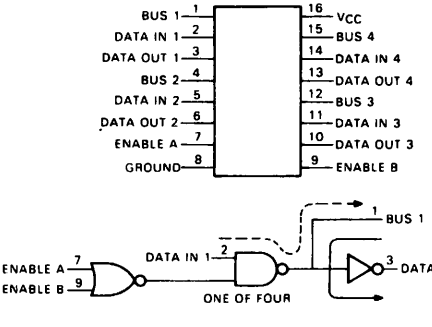


Figure 5 8641 Quad Unified Bus Transceiver (Bus Receiver/Driver)

APPENDIX F

Table 1 LSI-11 Bus Driver, Receiver, Transceiver Characteristics

Device	Characteristic	Sym	Specifications	Notes
Receiver	Input high voltage	V_{IH}	1.7 V min	1
(8640)	Input low voltage	V_{IL}	1.3 V max	1
(8641)	Input current at 3.8 V	I_{IH}	80 μA max	1, 3
	Input current at 0 V	I_{IL}	10 μA max	1, 3
	Output high voltage	V_{OH}	2.4 V min	2
	Output high current	V_{OH}	(16 TTL loads)	2, 3
	Output low voltage	V_{OL}	0.4 V max	2
	Output low current	I_{OL}	(16 TTL loads)	2, 3
	Propagation delay to high state	TPDH	10 ns min 35 ns max	4, 5
	Propagation delay to low state	TPDL	10 ns min 35 ns max	1, 5
Driver	Input high voltage	V_{IH}	2.0 V min	
(8881)	Input low voltage	V_{IL}	0.8 V max	
(8641)	Input high current	I_{IH}	60 μA max	6
	Input low current	I_{IL}	−2.0 mA max	6
	Output low voltage 70 mA sink	V_{OL}	0.8 V max	1
	Output high leakage current at 3.5 V	I_{OH}	25 μA max	1, 3
	Propagation delay to low state	TPDL	25 ns max	1, 5
	Propagation delay to high state	TPDH	35 ns max	1, 5

NOTES

1. This is a critical parameter for use on the I/O bus. All other parameters are shown for reference only.
2. This is equivalent to being capable of driving 16 unit loads of standard 7400 series TTL integrated circuits.
3. Current flow is defined as positive if into the terminal.
4. Conditions of load are 390 Ω to +5 V and 1.6 kΩ in parallel with 15 pF to ground for 10 ns min and 50 pF for 35 ns max.
5. Times are measured from 1.5 V level on input to 1.5 V level on output.
6. This is equivalent to 1.25 standard TTL unit loading of input.

Bus receivers and drivers should be well grounded and use V_{CC} to ground bypass capacitors. These gates should be located as close as practical to the module fingers which plug into the backplane and all etch runs to the bus should be kept as short as possible. Attention to these cautions should yield a module design with minimum bus loading (capacitance).

APPENDIX G

CABLING SUMMARY

Preassembled cables are available in a variety of lengths and types as listed in Table 1 The H854 and H856 connectors are shown in Figure 1.

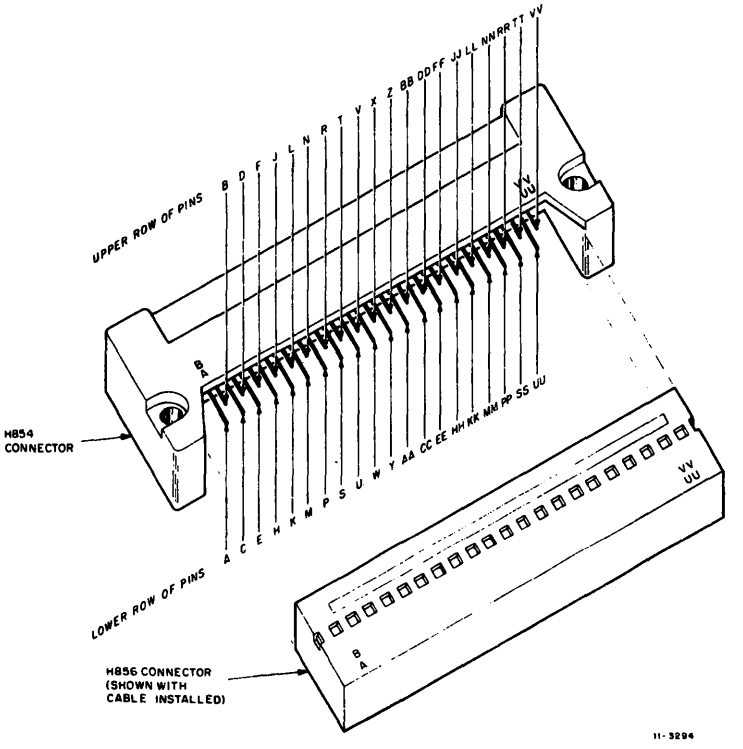


Figure 1 J1 or J2 Connector Pin Locations

APPENDIX G

Function	Module Type	Cable Recommendations
Serial I/O–Asynchronous		
20 MA	DLV11-F 1-Line DLV11-J 4-Line	BC05M-2C DLV11-KA (1 per line)
EIA RS-232C Data only	DLV11-F 1-Line	BC01V-25 (M)
(DLV11-J is also RS422/423)	DLV11-J 4-Line MXV11-A	BC21B-05 (M) or 1 per line BC20N-05 (T)
EIA RS-232C with Modem Control	DLV11-E 1-Line DZV11-B 4-Line MUX	BC01V-25 (M) Cable included
Serial I/O–Synchronous EIA RS-232C with Modem Control	DUV11-DA 1-Line	BC05C-25 (M)
Digital I/O		
Programmed Transfer	DRV11 16 in/16 out	BC07D-15(U) 2 ea or
DMA Transfer	DRV11-B 16 in/16 out	BC08R-12(B)
Analog I/O		
A/D	ADV11-A 16 channel	BC07D-15(U)
D/A	AAV11-A 4 channel	BC08R-12(B)
Mass Storage		
Tape Cartridge	TU58-BB	BC20N-05 plus a Serial Modem (M) cable
Double Density Floppy Diskette	RXV21-BA	Includes cable
Hard Disk (H9273 Backplane Req'd)	RLV11-AK	Includes cable

Note: M–Connects to a Modem T–Connects to an EIA Terminal
U–User end unterminated B–User end terminated with 40 pin Berg Connector

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