Rainbow™ 100

Technical Manual

digital

EK-PC100-TM-001

Rainbow™ 100

Technical Manual

digital equipment corporation

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WARNING: The Rainbow 100 computer has been certified to comply with the limits for a Class B computing device, pursuant to Subpart J of Part 15 of FCC Rules. Only peripherals (computer input/output devices, terminals, printers, etc.) certified to comply with the Class B limits may be attached to this computer. Operation with noncertified peripherals is likely to result in interference to radio and television reception.

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna.
- Move the computer away from the receiver.
- Plug the computer into a different outlet so that computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

How to Identify and Resolve Radio-TV Interference Problems

This booklet is available from the US Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

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PREFACE

This manual contains information needed by field service engineers, technicians, or other interested persons who have a need to know how the Rainbow 100™ computer is designed and operates. Included are explanations of the features, capabilities, system architecture, and technical characteristics as well as general reference data. The information is presented in twelve chapters and three appendixes.

Chapter 1	Contains a general description and specifications of the units comprising the Rainbow 100 computer.
Chapter 2	Provides basic operator information, including use of the keyboard and Set-Up modes for setting or changing the computer operating characteristics.
Chapter 3	Describes the functions and interaction of each hardware unit at the system level.
Chapter 4	Contains the technical description of the system module.
Chapter 5	Contains the technical description of the RX50 controller module.
Chapter 6	Contains the technical description of the RX50 diskette drive.
Chapter 7	Contains the technical description of the power supply and fan assemblies.
Chapter 8	Contains the technical description of the LK201 keyboard.
Chapter 9	Contains the technical description of the VR201 video monitor.
Chapter 10	Describes how to test and troubleshoot the Rainbow 100 computer using either the internal ROM-based or diskette-based diagnostic programs.
Chapter 11	Describes procedures for adjusting the monitor and provides removal and replacement procedures for modules and mechanical assemblies.
Chapter 12	Describes the multinational character codes supported by the Rainbow 100 computer.
Appendix A	Contains a recommended spare parts list and ordering information for parts and computer reference manuals.
Appendix B	Contains a list of ROM-based and diskette-based diagnostic error messages.
Appendix C	Contains a glossary of terms, acronyms, and abbreviations used in this manual.

Many terms used in this manual are written out the first time they appear, followed by an abbreviation or mnemonic in parentheses. Thereafter, the abbreviation or mnemonic is generally used.

The keys on the Rainbow 100 keyboard that are mentioned in text appear in boldface (for example, press the **Shift** key). Note that **<Return>** represents the **Return** key, and to press **<Shift/A>** means to hold down the **Shift** key and press the **A** key at the same time.

CHAPTER 1
INTRODUCTION

NOTE
The Rainbow 100 computer described in this manual is model PC100A and should have been installed according to instructions in the *Rainbow™ 100 Installation Guide.*

1.1 GENERAL DESCRIPTION

The Rainbow 100 computer is a high performance personal computer that runs a wide selection of CP/M®-based and MS™-DOS-based software. A dual processor system architecture allows execution of 8-bit or 16-bit application programs using the CP/M®-86/80 operating system.

The basic Rainbow 100 computer consists of:

- A video monitor
- A keyboard
- A dual processor (Z80A® and 8088™)
- 64K bytes* of main memory (expandable to either 128K bytes or 256K bytes)
- A standard dual-diskette drive containing 800K bytes of on-line auxiliary memory on two 5-¼ inch diskettes, with a second dual-diskette drive provided optionally for an added 800K bytes of on-line auxiliary memory
- A printer/communications controller for adding an optional printer and/or an optional modem

The Rainbow 100 computer is housed in three separate units: the video monitor, the keyboard, and the system unit. Figure 1-1 shows the Rainbow 100 computer in two views: with the system unit positioned horizontally, and with the system unit positioned vertically in the optional floor stand.

CP/M® is a registered trademark of Digital Research Inc.
MS™-DOS is a trademark of Microsoft Corporation.
Z80A® is a registered trademark of Zilog, Inc.
8088™ is a trademark of Intel Corporation.
*A byte = 1 character location; 1K byte = 1024 bytes.

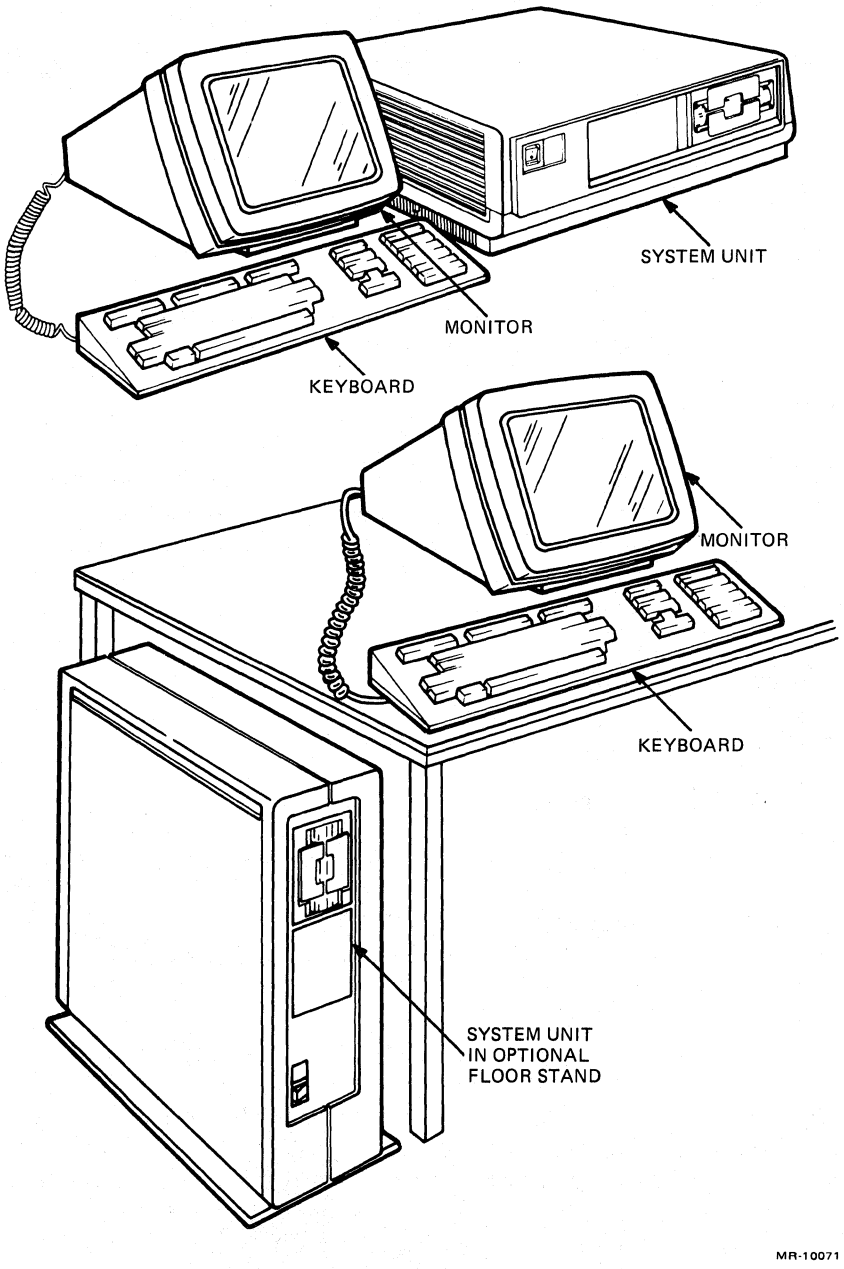


Figure 1-1 Rainbow 100 Computer

1.2 PHYSICAL DESCRIPTION

1.2.1 Video Monitor

The Rainbow 100 computer monitor has a video screen with a diagonal dimension of 30.5 cm (12 in). The screen is coated to reduce glare. (Avoid touching the screen since fingerprints show up very easily. When necessary, clean the screen with the cleaner provided.)

The monitor displays video information from the video control system on the screen. (The video control system resides on the system module inside the system unit.) The monitor also provides the internal connection for the keyboard and has the following features:

- 24-line × 80- or 132-column display
- Jump or smooth scrolling
- Double-height characters (by line)
- Double-width characters (by line)
- Normal and reverse video (by character)
- Boldface, blinking, and underlined characters (by character)
- Dark or light screen background
- Auto-screen blanking
- Brightness and contrast controls

Figure 1-2 shows the brightness and contrast adjustments located on the back of the monitor.

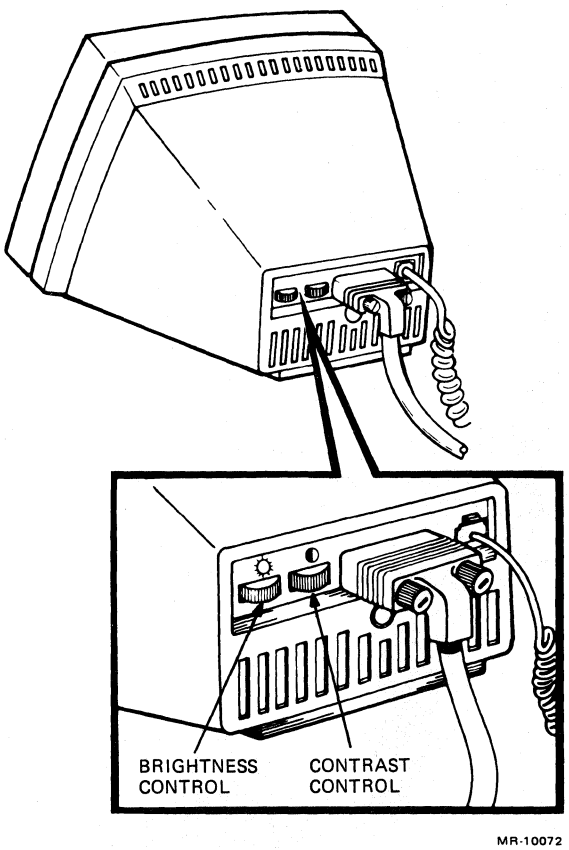


Figure 1-2 Brightness and Contrast Controls

1.2.2 The Keyboard

The Rainbow 100 computer has a low-profile keyboard with 105 keys, as shown in Figure 1-3. The standard keys at the left and center provide the uppercase and lowercase letters, numbers, and punctuation. To the right of these keys are the editor keys (**Find, Insert Here**, **Remove**, **Select**, **Prev Screen**, and **Next Screen**) and the cursor control keys (↑, ↓, ←, →). On the far right is the numeric keypad.

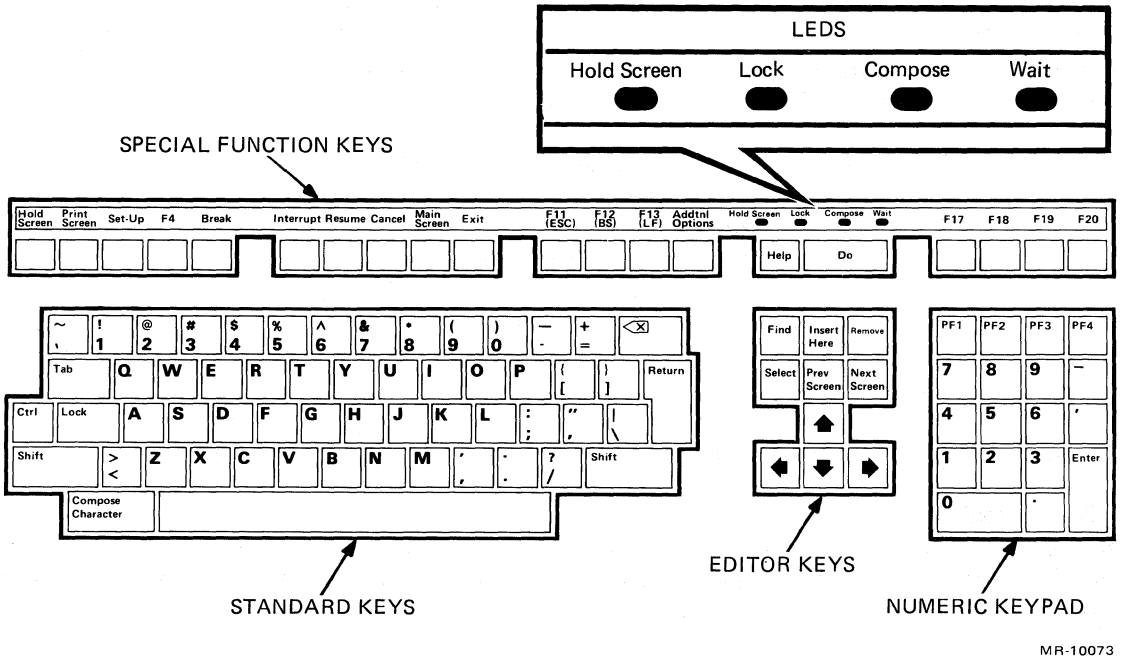


Figure 1-3 Keyboard Controls and Indicators

Across the top of the keyboard are the special function keys. Included in these keys are the **Set-Up** key, the **Help** key, and the **Do** key. The **Help** key calls a help message to the screen in Set-Up mode and during applications that use this key. The **Do** key separates the "execute" function from the "carriage return" function within an application program that can distinguish between these functions.

Also included in the top row are the special function keys for different types of applications—word processing, electronic mail, accounting spreadsheets, etc. These keys can be custom labeled with a removable strip for each application.

1.2.2.1 Keyboard Features – The keyboard has the following features:

- A low profile that allows access to the dual-diskette drive in the system unit, should you want to place the two components on the same table or desk.
- Keyclick sounds as the keys are pressed. You can adjust the keyclick volume or turn it off.
- A keyboard tone generator that produces a margin bell. The tone volume is also adjustable.
- Auto-repeat of all keys on the main keypad array, the numeric keypad, and the function keys (including **Space**, <kbd>X</kbd>, and **Tab**). Exceptions are the **Return** key and any key used in conjunction with the **Control** key.

The keys are arranged in an electrical matrix, which is scanned for keys that are pressed. A single-chip, 8-bit processor detects whenever a key is pressed and transmits the event to the system module.

1.2.2.2 Keyboard LEDs – The keyboard has four lights (LEDs) that indicate when a specific function is in operation. The functions indicated are: Hold Screen, Lock, Compose, and Wait. During normal operation, the lights have the following meanings when they are on.

Indicator	Meaning
Hold Screen	The **Hold Screen** key has been pressed. New data will not be added to the monitor's screen until you press **Hold Screen** again.
Lock	The **Lock** key has been pressed, enabling caps lock mode.
Compose	The **Compose Character** key has been pressed (for special applications only). (CP/M-86/80 does not support this key.)
Wait	Keyboard transmission has been temporarily stopped by the system. If this light is on, any additional characters typed are lost. The keyboard beeps once for each key pressed.

The lights can also signal error conditions. All four lights flash when the power-up selftest fails.

1.2.3 The System Unit

The system unit, shown in Figure 1-4, contains the power supply, the system module, a dual-diskette drive, a fan, and the system power switch. This unit can be placed horizontally on a desk or vertically in the optional floor stand.

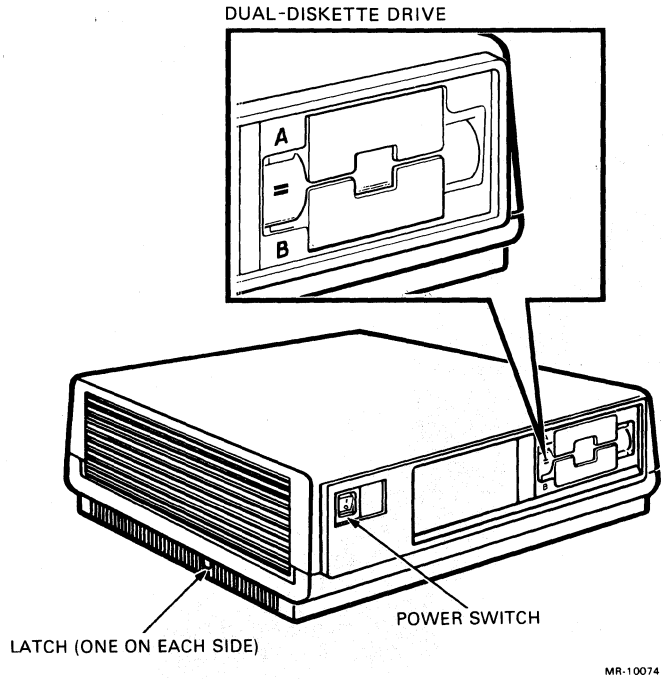


Figure 1-4 System Unit Controls and Indicators (Front)

Placing the system unit in the floor stand decreases the amount of desk space needed by the personal computer. The floor stand also keeps the unit fixed and allows it enough airflow.

The components of the system unit are designed to make installation of options and maintenance of components easy. The system unit's cover is secured by sliding latches under its left and right sides. The diskette drives can be removed by releasing their latches, the power supply can be removed by disconnecting the cables. The system module slides out the back of the system unit.

The connectors for power and peripheral devices are at the back of the system unit, as shown in Figure 1-5. They are unique in design to prevent misconnections and are labeled: COMM (for an optional communications line), PRINTER, and VIDEO (for the monitor cable).

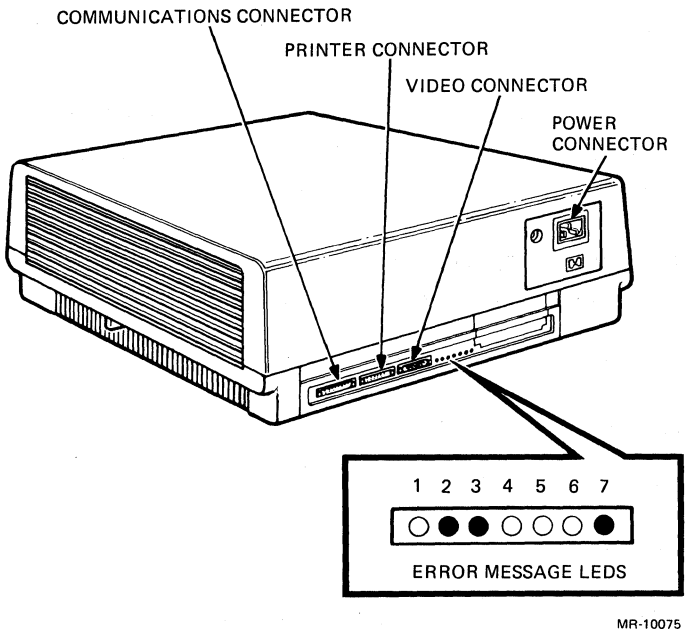


Figure 1-5 System Unit Controls and Indicators (Rear)

Seven LEDs at the back of the system unit indicate the source of any problem with the computer. The LEDs provide a backup to error messages and are especially useful should the monitor fail.

1.2.3.1 The System Module – The system module, located inside the system unit, is made up of electrical components and circuits. Its major components are the two processors (Z80A and 8088), memory chips, and communications hardware. Mounted on the system module is the RX50 controller module. It controls reading and writing on the diskette drives. The system module has other connectors for mounting a memory extension option and other options as they become available.

You can expand the system module's memory by adding a 64K byte or a 192K byte memory extension option. The system module also has a 24K byte ROM, which contains diagnostic tests, a bootstrap program, and the terminal emulation program.

The Z80A processor has sole access to the RX50 controller module. Available to the processor are 64K bytes of RAM, which are divided into 62K bytes of shared memory and 2K bytes of unshared memory. The 62K bytes are shared with the 8088 processor.

The 8088 processor controls the monitor, the keyboard, the printer, and the communications line. It also controls any additional options that may be added to the system module. A screen memory and an attribute memory allow it to control the information on the monitor.

1.2.3.2 The RX50 Dual-Diskette Drive – The Rainbow 100 computer uses a compact diskette subsystem that consists of a diskette controller module and a dual-diskette drive, which controls two 5-¼ inch diskettes. The diskettes provide mass storage, data exchange, and file backup capabilities. Each diskette stores 400K bytes of information.

The dual-diskette drive has two spindles that are turned by the same drive motor. The drive accesses its two diskettes by a single-head carriage assembly, which is moved by one stepper motor/lead screw combination.

Each diskette drive has two sensors that detect when a diskette is installed. These sensors also look for the notch on the side of the diskette's protective cover to see if the diskette is write protected. If this notch is covered, the diskette drive cannot write on the diskette.

1.3 FEATURES AND CAPABILITIES

The following features are standard on all Rainbow 100 computers:

- Selftest diagnostics with LED readouts
- 80- or 132-column video display
- 64K byte main memory
- 800K byte auxiliary storage
- Built-in controllers for additional diskette drive, printer, and modem
- Programmable bit rates
- Hardware/software error messages

The Rainbow 100 computer:

- Operates CP/M or MS-DOS
- Recognizes programs written for 8- or 16-bit processors (Z80A or 8088) when running CP/M-86/80
- Can be expanded to 128K bytes or 256K bytes main memory
- Is RS-232 and RS-423 compatible

- Supports an additional diskette drive
- Supports an optional printer and/or modem
- Provides optional color/graphics
- Provides optional extended communications

1.4 RAINBOW 100 COMPUTER SPECIFICATIONS

1.4.1 System Specifications

Standard System:	System unit, keyboard, monitor, and operating system
System Unit:	
Processors	Z80A and 8088 processors
Memory	64K bytes
Printer connector	Serial, RS-423
Communications connector	Speeds up to 19,200 baud with modem control, RS-423
Storage	Dual-diskette drive (2 × 400K bytes)
Video Output:	Monochromatic, RS-170 compatible
Operating System:	CP/M-86/80 or MS-DOS
Environment:	Class A: air-conditioned office or light assembly area
Temperature	
Operating*	15° C to 32° C (59° F to 90° F)
Not operating	−34° C to 60° C (−29° F to 140° F)
Relative humidity	
Operating	20% to 80% with maximum wet bulb 25° C (77° F) and minimum dew point 2° C (36° F)
Not operating	5% to 95% (noncondensing)
Altitude (maximum)	
Operating	2440 m (8,000 ft)
Not operating	9144 m (30,000 ft)
Magnetic field	The RX50 diskette may lose data when exposed to a magnetic field strength of 50 oersteds or more.

* Maximum allowable temperature is reduced by 1.8° C per 1000 m (1° F per 1000 ft) above sea level. Example: At 2.4 km (8000 ft), the maximum temperature is 27.5° C (82° F).

System Expansion:	Three dedicated spaces for option modules that are user-installable

Hardware Options:

Additional memory	64K or 192K bytes
Second dual-diskette drive	(2 × 400K bytes)

Any serial printer with the same FCC classification as the Rainbow 100 computer (Class B), such as the LA50 Personal Printer, LA100 Letterprinter 100, or LQP02 Letter-Quality Printer

Optional floor stand for vertical mounting of the system unit

1.4.2 Video Monitor Specifications

Characters:	7 × 9 dot matrix; includes 2-dot descenders
Format:	24 lines × 80 or 132 characters

Physical Description:

Height	29.2 cm (11.5 in)
Width	34.9 cm (13.75 in)
Depth	31.1 cm (12.25 in)
Weight	6.4 kg (14 lb)
Cord	1.9 m (6 ft)

Adjustable Tilt:	+5° to −25°
Video Format:	Monochromatic, composite

1.4.3 Keyboard Specifications

Audio and Visual Indicators:	4 lights and bell tone generator
Cord:	1.9 m (6 ft) coiled cord; 4-pin, telephone-type modular connectors; plugs into back of monitor
Physical Description:	Low-profile, detachable

Height	5 cm (2.0 in) at highest point
Length	53.3 cm (21 in)
Width	17.1 cm (6.75 in)
Weight	4 kg (4.5 lb)

Keypad:	Sculptured key array
Home Row Key Height:	3 cm (1.2 in) above desktop

Keys:	105 keys; matte, textured, concave surface
Size (each)	1.27 cm (0.50 in) square
Spacing	1.9 cm (0.75 in) center-to-center (single-width keys)
Wobble	Less than 0.5 mm (0.020 in)
Force to activate	53 g to 79 g (1.8 oz to 2.7 oz); space bar is double this amount
Travel to activate	Less than 0.3 cm (0.12 in)
Numeric Keypad:	18 keys
Function Keys:	36 keys; firmware- and software-driven; 20 function keys horizontally positioned below label strip
Power:	+12 V ± 5% @ 400 mA, 4.8 W maximum

1.4.4 System Unit and Power Supply Specifications

Physical Description:

Height	16.5 cm (6.5 in)
Length	48.3 cm (19 in)
Width	36.3 cm (14.3 in)
Weight (maximum)	13.6 kg (30 lb)
Power Supply Type:	Transistor, switching-type ac-to-dc converter
AC Input:	Switch-selectable
115 V (nominal)	Single-phase, 3-wire, 90 V to 128 V rms; 47 Hz to 63 Hz line frequency
230 V (nominal)	Single-phase, 3-wire, 174 V to 256 V rms; 47 Hz to 63 Hz line frequency
Line Current:	3 A @ 115 Vac 1.5 A @ 230 Vac
AC Power Consumption:	218 W
Regulated Voltages:	+5.1 V ±6% over the current range of 2.5 A to 11.5 A +12.1 V ±6% over the current range of 0.6 A to 6.7 A −12 V ±7% over the current range of 0.0 A to 0.15 A
Circuit Protection:	Circuit breaker, externally accessible

1.4.5 RX50 Dual-Diskette Drive Specifications

Performance:

Diskettes per dual-diskette drive	2
Number of recording surfaces per diskette	1
Storage capacity per diskette (80 tracks)	400K bytes
per track (10 sectors)	5K bytes
per sector	512 bytes
Transfer rate	250 bits/s
Average access time	290 ms

Functional Specifications:

Rotational speed	300 r/min
Density	96 tracks per inch

Physical Specifications:

Height	8.4 cm (3.3 in)
Width	14.7 cm (5.8 in)
Depth	21.6 cm (8.5 in)
Weight	1.7 kg (3.8 lb)

CHAPTER 2
OPERATING INFORMATION

2.1 INTRODUCTION

This chapter describes the procedures for operating the Rainbow 100 computer without going into details on the use of software or application programs. Refer to the *Rainbow™ 100 User's Guide* for that information.

2.2 USING DISKETTES

1. Use only RX50K diskettes formatted for the Rainbow 100 computer.

2. Always handle diskettes by the label end.

3. Keep diskettes away from magnets or magnetic tools.

4. Insert diskettes so that the orange arrow on the diskette points to the orange strip on the front bezel, which becomes visible when the drive door is open.

5. Never insert or remove diskettes when the power is off.

6. Never remove a diskette when the LED on the front of that drive is on.

7. Use write-protect tabs for the operating system diskettes and for other diskettes you want to write protect. (Write-protect tabs are available at most computer stores.)

2.3 POWERING UP THE RAINBOW 100 COMPUTER

Use the following procedure.

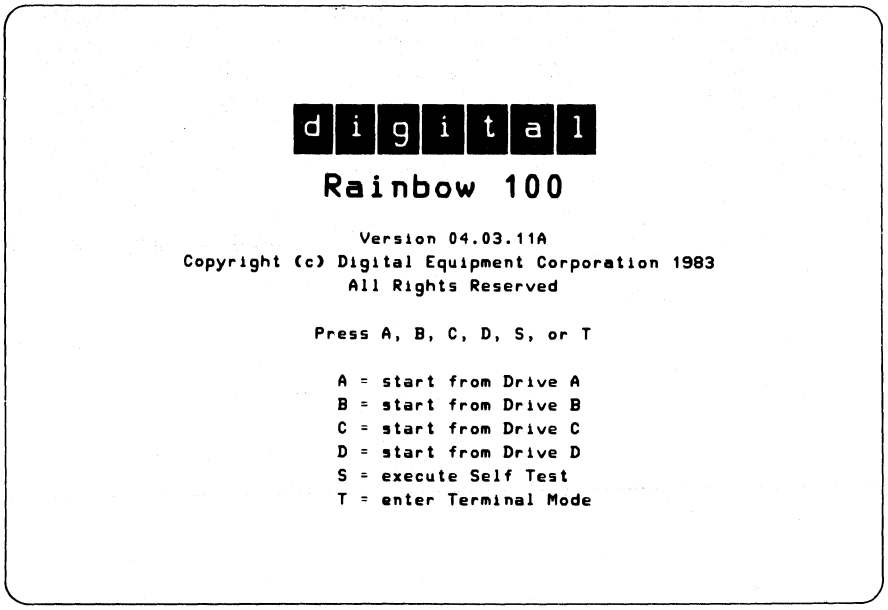
1. Place the power switch on the front of the system unit to 1 (On). At this point, the Rainbow 100 computer tests its main memory and looks for any hardware malfunctions. If the power-up test is successful, the Main System Menu (refer to Figure 2-1a) is displayed on the screen. If the test is not successful, an error message is displayed at the top of the screen. These messages are of two types:

   a. A nonfatal error message, such as that shown in Figure 2-1b, which allows you to select another choice from the system menu.

   b. A fatal, flashing error message at the top without the Main System Menu, as shown in Figure 2-1c.

   Refer to Appendix B for an interpretation of these messages.

2. After the Main System Menu is displayed, set up the computer according to Paragraph 2.4.



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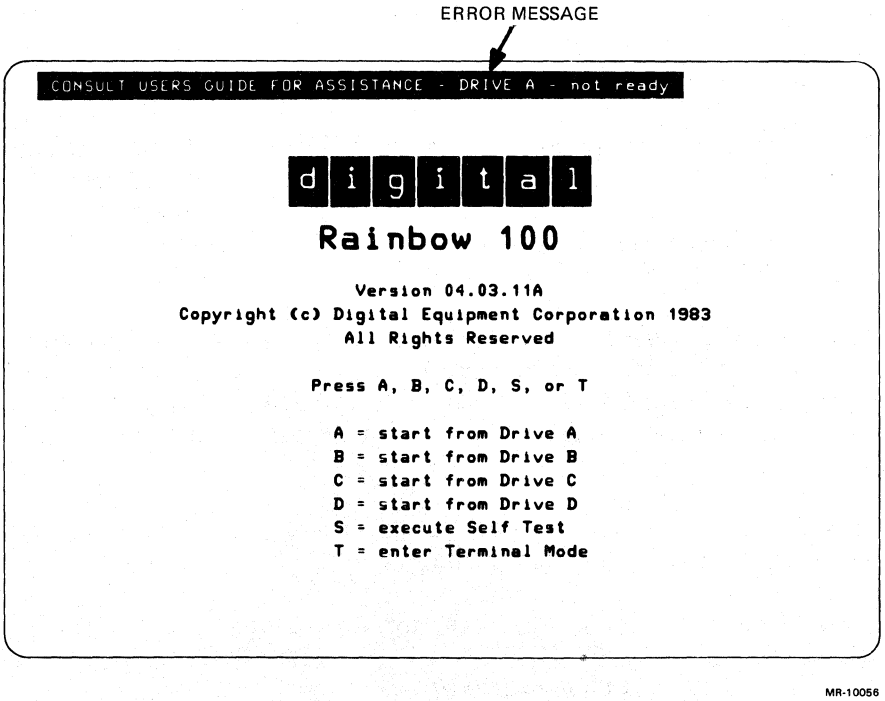
a. Main System Menu



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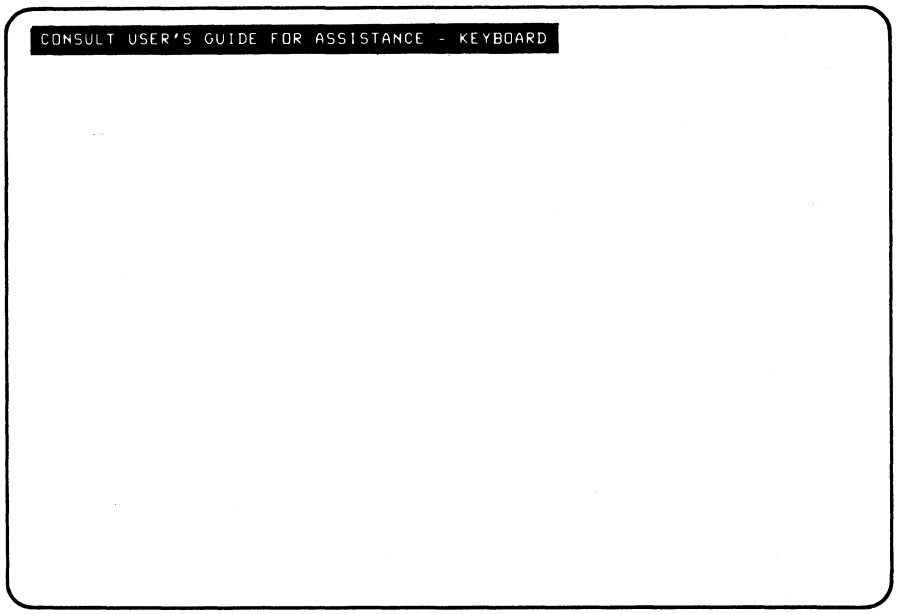
b. Nonfatal Error Message



c. Fatal Error Message

Figure 2-1 Main System Menu and Error Messages

2.4 SETTING UP THE COMPUTER

Pressing the **Set-Up** key, shown in Figure 2-2, causes the system to enter the Set-Up mode and places the Set-Up display on the screen, as shown in Figure 2-3. When entering Set-Up, the text on the screen will be replaced temporarily by the Set-Up display. However, if you perform one of the following procedures while in Set-Up, the text will be erased.

- Change the screen width
- Recall default Set-Up values (pressing the **Shift** and **D** keys simultaneously)
- Recall previously saved Set-Up values (pressing the **Shift** and **R** keys simultaneously)

The Set-Up mode allows you to change the following Rainbow 100 computer features:

- Tab stops
- Settings to match those of the printer
- Settings to match those of any communications device attached to the computer
- Number of characters displayed across the screen (screen width)
- Cursor style to block or underline
- Screen background to dark or light
- Automatic repeating of keyboard keys
- Margin bell volume
- Keyclick volume
- Entry of a 20-character message for identification on a communications line

These features are divided into areas of common usability called major headings. Each major heading has a specific display associated with it that is displayed on the screen. There are six major headings in the Rainbow 100 computer. Each has a number of selections that can be changed, known as minor headings. The major headings and the number of selections in each are as follows:

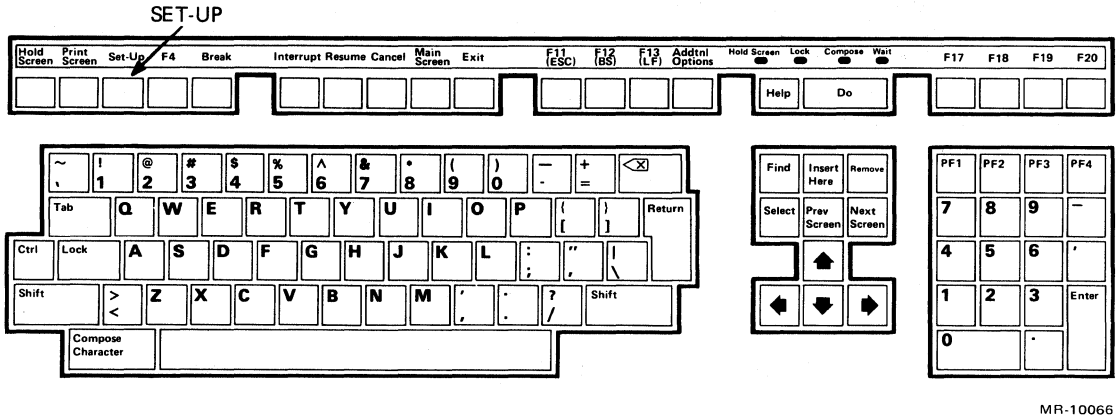


Figure 2-2 Set-Up Key Location

Major Heading	Number of Selections (Minor Headings)	See Paragraph Below for Description
Tabs	2	2.4.2
Param(eter) Set(tings)	24	2.4.3
Modem	5	2.4.4
Printer	2	2.4.5
Misc(ellaneous)	3	2.4.6
Memory	1	2.4.7

Once you press the **Set-Up** key, you can move from one major heading to another by using the **Next Screen** or **Prev Screen** keys. Once you select a major heading, you can step through its minor headings, parameters, or tab settings by using the → or ← keys.

The minor heading selected is displayed in reverse video; a tab setting is displayed by a cursor position. You can step through the values of each selection by using the ↑ or ↓ keys.

2.4.1 Help

While in Set-Up, pressing the **Help** key causes a help message to be displayed on the screen. This help message is a quick reminder on how to change the settings in Set-Up. Pressing the **Help** key again returns you to the current major heading.

2.4.2 Tabs Major Heading

When you enter Set-Up, you are automatically in the Tabs major heading, as shown in Figure 2-3. In this heading you can change the tab stop settings and switch the computer between line and local operations. You can move to the next major heading by pressing the **Next Screen** key. To return to the Tabs major heading, press the **Prev Screen** key.

NOTE

The number 04.03.11A, shown in Figure 2-3, is the revision of the computer's firmware, which in the computer may be different.

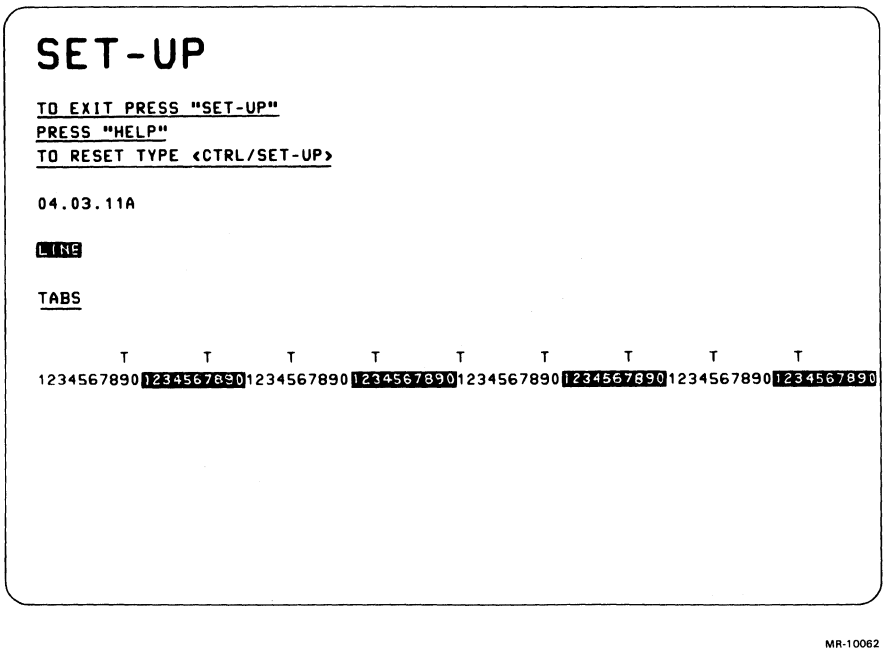


Figure 2-3 Set-Up Display – Tabs

2.4.2.1 Tab Stops – When entering Set-Up, the numbers across the middle of the screen represent the columns in which you can place characters. There are either 80 or 132 possible character positions, depending on the screen-width setting. The Ts indicate the current tab stop settings. For information on setting tab stops, refer to the *Rainbow™ 100 User's Guide.*

2.4.2.2 Local and Line Modes – In the terminal mode, the Rainbow 100 computer must be set to LINE in order for it to communicate with its diskette drives and any external device (a printer or a telephone line). When you place the computer in Set-Up, either LINE or LOCAL is displayed on the screen to indicate the computer's current mode. It will stay in this mode unless you change it. If you place the computer in local mode and exit Set-Up, the keys you press on the keyboard will echo their characters on the screen. (Normally, you would leave this feature on LINE.) While in Set-Up you can change this feature by typing **L**.

If you want to return to the Main System Menu while in Set-Up, press the **Set-Up** key; otherwise press **<Ctrl Set-Up>**. To continue in Set-Up, press **<Next Screen>** to select the Parameter Settings major heading.

2.4.3 Parameter Settings Major Heading

The Parameter Settings (PARAM SET) major heading is shown in Figure 2-4. The current selections (0s or 1s) of all the settings in this major heading are printed on a line across the middle of the screen. Each selection's name is also printed on the screen when the cursor is positioned on the selection. Below the name is the meaning of each value you select. Figure 2-5 summarizes the selections possible and shows their default values. Table 2-1 lists the selections in the order in which they are displayed on the screen. Certain selections have meaning only when the Rainbow 100 computer is being used as a terminal (in terminal mode). These selections are identified by an asterisk in Table 2-1.

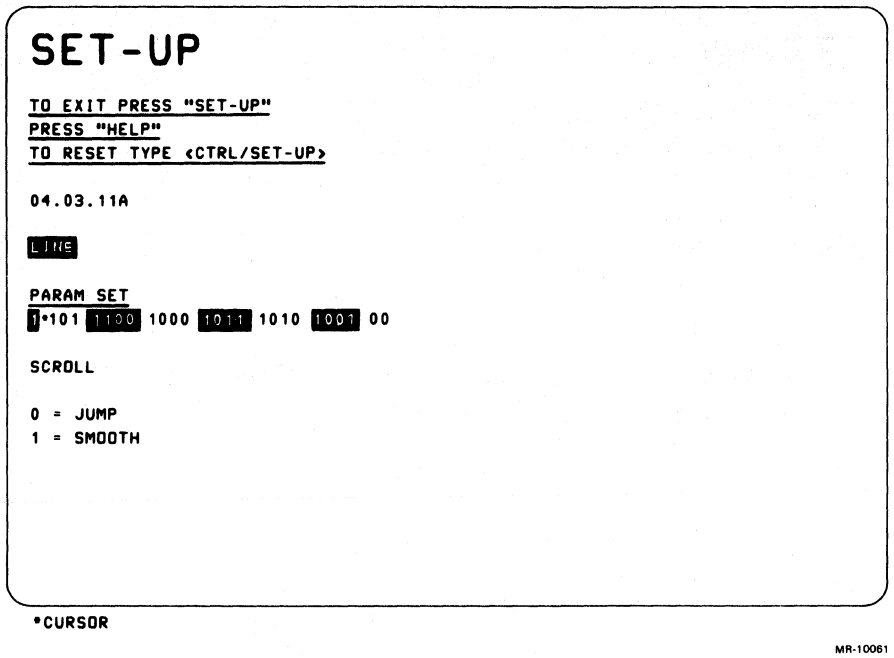


Figure 2-4 Set-Up Display – Param(eter) Set(tings)

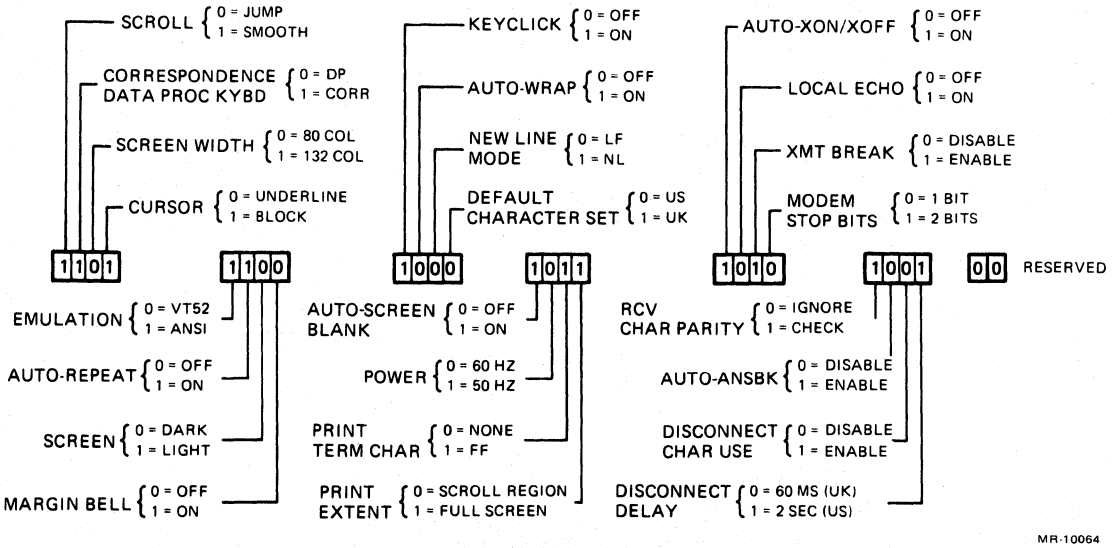


Figure 2-5 Summary of Parameter Settings

Table 2-1 Parameter Settings Major Heading

Selection (Minor Heading)	Values*
Scroll	0 = Jump **1** = Smooth
Correspondence/ data processing keyboard	0 = DP (data processing) **1** = Corr. (correspondence)
Screen width	**0** = 80 (columns) 1 = 132 (columns)
Cursor	0 = Underline **1** = Block
Emulation	0 = VT52 **1** = ANSI
Auto-repeat	0 = Off **1** = On
Screen	**0** = Dark 1 = Light
Margin bell	**0** = Off 1 = On
Keyclick	0 = Off **1** = On
Auto-wrap	**0** = Off 1 = On
New line mode	**0** = LF (line feed) 1 = NL (new line)
Default character set	**0** = U.S. ASCII (#) 1 = U.K. (£)
Auto-screen blank	0 = Off **1** = On
Power	**0** = 60 Hz 1 = 50 Hz
Print termination character†	0 = None **1** = FF (form feed)
Print extent†	0 = Scroll region **1** = Full screen

*Values in boldface are the default settings.

†This selection has meaning only in terminal mode.

Table 2-1 Parameter Settings Major Heading (Cont)

Selection (Minor Heading)	Values*
Auto-XON/XOFF†	0 = Off **1** = On
Local echo†	**0** = Off 1 = On
Transmit break†	0 = Disable **1** = Enable
Modem stop bits	**0** = 1 (bit) 1 = 2 (bits)
Received character parity†	0 = Ignore **1** = Check
Auto-answerback†	**0** = Disable 1 = Enable
Disconnect character use†	**0** = Disable 1 = Enable
Disconnect delay†	0 = 60 ms **1** = 2 s

*Values in boldface are the default settings.

†This selection has meaning only in terminal mode.

To change the value of the current selection, press the ↑ or ↓ key. To proceed to the next selection, press the → key or the space bar. To return to a previous selection, press the ← key. To return to the first selection shown in Figure 2-5, press the **Return** key.

The CP/M-86/80 operating system needs certain selections set to specific values. Table 2-2 lists these selections.

Table 2-2 Parameters Set for CP/M-86/80 Compatibility

Parameter	Selection	Value
Emulation (ANSI/VT52)	ANSI	1
Auto-wrap	Off	0
New line mode	LF (Line feed)	0

The following paragraphs describe the selections you should check when you add a communications line or a printer to the Rainbow 100 computer. The selections meant primarily for the operator are described in the *Rainbow™ 100 User's Guide.*

2.4.3.1 Scroll – This selection applies to the upward and downward movement of lines of text on the screen to make room for new lines. With jump scroll, the characters on the screen advance upward a full line of characters at a time, and new lines of characters are added at the bottom of the monitor. If auto-XON/XOFF is off, use jump scroll.

With smooth scroll, the characters on the screen advance one-tenth of a line (one scan line) at a time. Smooth scrolling increases the ability to read new data as you receive it. You can set a limit on the smooth scroll rate in the Misc major heading. A scroll rate setting of 1, 2, or 3 represents 3, 6, or 12 lines per second, respectively. If auto-XON/XOFF is on, you may wish to use smooth scroll.

2.4.3.2 Correspondence/Data Processing Keyboard – For non-American keyboards, this feature allows you to select character printing. When this bit is set to 1, accents and other language-specific marks appear with the characters. However, such characters are not acceptable for entrance into a computer program. With this bit set to 0, it eliminates the accents and language-specific marks and replaces them with data processing oriented characters.

2.4.3.3 Screen Width – This setting allows you to select the monitor's screen width, either 80 or 132 columns. The number of characters that can be displayed in each screen width are as follows.

Screen Width	Single-Width Characters	Double-Width Characters
80	80	40
132	132	66

CAUTION

Changing the screen width will erase the data you had displayed on the monitor before you entered Set-Up.

2.4.3.4 Cursor – This feature allows you to select a cursor that is a blinking underscore or a blinking block.

2.4.3.5 Emulation – With VT52 selected, the Rainbow 100 computer emulates VT52 character processing. With ANSI selected, the Rainbow 100 computer uses functions according to the format of the American National Standards Institute (ANSI).

2.4.3.6 Auto-Repeat – This setting allows you to automatically repeat a key if it is held down for more than one-half second, except for the control characters, **Set-Up**, **Escape**, **Return**, **Compose Character**, **Break**, **Print Screen**, **Enter**, **F4**, and **Hold Screen** keys.

2.4.3.7 Screen – This feature allows you to set the screen to a dark background with light characters, or a light background with dark characters.

2.4.3.8 Margin Bell – This selection allows you to enable or disable a bell that rings when the cursor moves past the eighth character position from the end of the line.

2.4.3.9 Keyclick – This selection allows you to enable or disable a clicking sound when a key is pressed.

2.4.3.10 Auto-Wrap – With auto-wrap enabled, any displayable character received when the cursor is at the right margin is automatically placed at the beginning of the next line, scrolling up if needed. With auto-wrap disabled, any character entered past the right margin prints over the last character position on that line. The auto-wrap feature should be off for the CP/M-86/80 operating system. In terminal mode, this feature should be set to match the remote computer.

2.4.3.11 New Line Mode – In line feed (LF) mode, a received line feed will perform a cursor index to the same character position on the next line. Pressing the **Return** key sends the carriage return code only.

NOTE
At the bottom margin, pressing the Return key may cause a scroll to occur.

In new line (NL) mode, a received line feed will cause the cursor to move to the beginning of the next line. Pressing the **Return** key causes the transmission of both a carriage return and a line feed code. New line mode should be off for the CP/M-86/80 operating system.

2.4.3.12 Default Character Set – When you set this parameter to 0, the computer transmits codes that agree with the American Standard Code for Information Exchange (ASCII). These codes are standard for printers and communications devices so they can transfer information using a common data pattern. When you set this parameter to 1, the code for the # symbol on reception only causes display of the British pound sterling character (£).

2.4.3.13 Auto-Screen Blank – With this feature on (the default condition), the output to the screen will be turned off after about 30 minutes of not receiving characters. A blinking phantom cursor will appear on the screen, as shown in Figure 2-6, to indicate that the system is still on. To bring back the data you had on the screen, press the **Shift** key and the display on the screen will be restored. The **Shift** key has no meaning to a program (important here since the program may have been waiting for a response from you before the screen went blank).

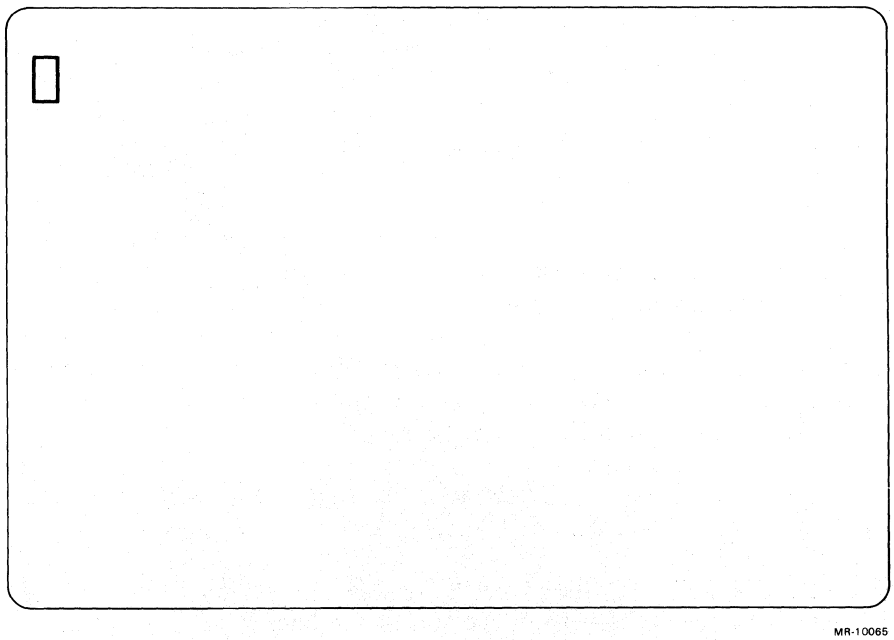


Figure 2-6 Auto-Screen Blank Phantom Cursor

2.4.3.14 Power – This feature sets the monitor's scan rate to match the power line frequency in order to maintain correct screen height and prevent display jitter. You should set this parameter to 0 for 60 Hz (common in the U.S.) or to 1 for 50 Hz (common in other countries).

2.4.3.15 Print Termination Character – In the terminal mode, this setting determines if a form feed (FF) character is to be sent automatically to the printer at the end of every print screen function.

2.4.3.16 Print Extent – This selection applies only to the terminal mode. It determines the characters that will be printed during a print screen operation. When you set the feature to full screen, all characters on the screen print. When you set the feature to scroll region, only the characters in the scroll region print. The scroll region is the screen area between the top and bottom margins. Normally, the remote computer selects the margins; if it does not, all characters on the screen print.

2.4.3.17 Auto-XON/XOFF – This selection applies only to the terminal mode. When auto-XON/XOFF is on, the Rainbow 100 computer will automatically be synchronized to a host computer that uses XON and XOFF control signals. When the Rainbow 100 computer receives more characters than it can handle, it automatically sends an XOFF control character to the host computer, which tells it to stop sending data. When the Rainbow 100 computer can accept more data, it sends an XON control character to tell the host computer to resume data transmission.

2.4.3.18 Local Echo – This feature applies only to the terminal mode. When on (except in Set-Up), all keys typed are echoed (displayed) on the screen and are transmitted to the host computer. Enable this feature if the host computer is not echoing the characters you type. When this feature is off, all keys typed are transmitted to the host computer without their being echoed on the monitor.

When not in the terminal mode, the operating system of the Rainbow 100 computer echoes the characters you type on the screen.

2.4.3.19 Transmit Break – When this selection is enabled in the terminal mode, pressing the **Break** key places a space signal on the transmit data line. If the terminal is not transmitting, no signal will be sent. Also, no space signal will be sent if this selection is disabled.

NOTE

Disabling the transmit break function does not affect a <Shift/Break>, which causes the modem line to disconnect, or a <Ctrl/Break>, which sends the answerback message on the transmit data line.

2.4.3.20 Modem Stop Bits – The selection places 1 or 2 stop bits at the end of each character's data pattern. Normally, 1 stop bit is used with baud rates higher than 110, and 2 stop bits are used with baud rates of 110 and lower.

2.4.3.21 Received Character Parity – This selection applies only to the terminal mode. When set to "check," this selection allows the computer to check for errors in the data patterns of received characters. For example, suppose the remote computer has sent an even number of data pulses for even parity. If the Rainbow 100 computer does not receive an even number of pulses, it does not display the character; instead, it displays the substitution character ▒.

When this selection is set to "ignore," the Rainbow 100 computer does not check for parity errors in received characters.

2.4.3.22 Auto-Answerback – With this feature enabled in the terminal mode, the Rainbow 100 computer automatically transmits its answerback message when a telephone connection is made. (See Answerback Message in Paragraph 2.4.3.25.) When this feature is disabled, no message is sent.

2.4.3.23 Disconnect Character Use – When this selection is enabled in the terminal mode, and the Rainbow 100 computer receives a disconnect character, it will disconnect the telephone line. (See Paragraph 2.6 for additional information.) Pressing **<Shift/Break>** sends a disconnect character on the transmit data line.

2.4.3.24 Disconnect Delay – In the terminal mode, this selection allows either a 60 ms delay (typical in the United Kingdom) or a 2 second delay (typical in the United States and other countries) before disconnecting the telephone line.

NOTE

Disconnect delay is active only for FDXB and FDXC modem protocols. This selection is ignored by FDXA modem protocol.

2.4.3.25 How to Store an Answerback Message – You can store an answerback message in the computer while in any of the major headings. (The computer remembers the current major heading.) Start by typing **<Shift/A>**. The terminal responds by displaying AUTO-ANSBK and A = on the screen, as shown in Figure 2-7. Next, type a delimiter, which may be any character, followed by a message of up to 20 characters. (The delimiter is not sent as part of the message.)

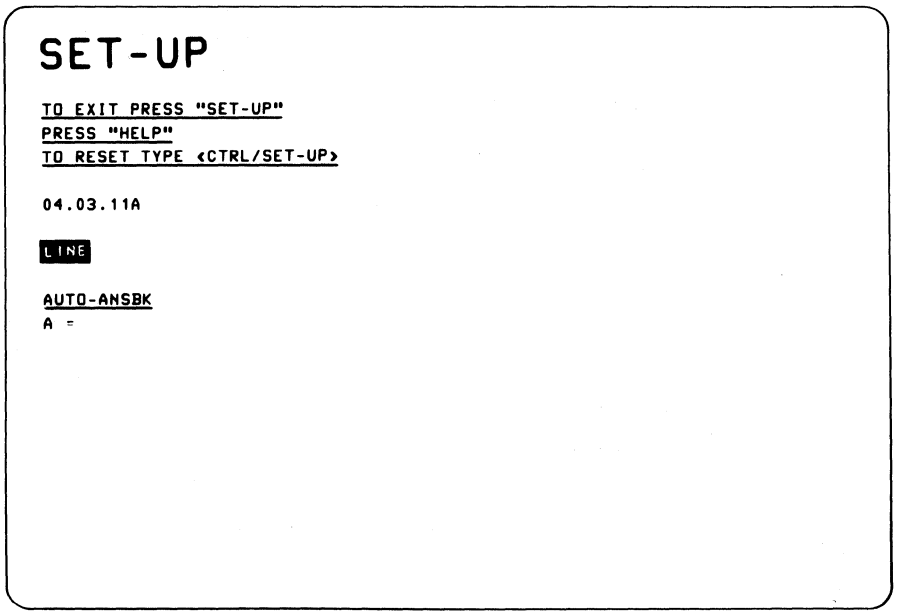


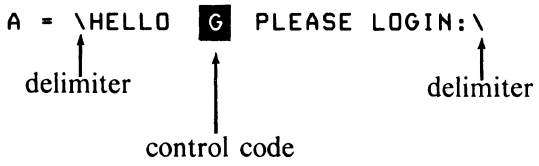
Figure 2-7 Set-Up Display – Auto-Answerback

NOTE

You may use control characters, such as <Return>, in the message. A control character is echoed on the screen as a reverse-video-associated ASCII character. For example, a bell is a reverse-video G for <Ctrl/G>; a <Return> is a reverse-video M.

The message automatically terminates after you enter the 20th character. You may also end the message early by typing the same delimiter you started with. This will also return you to the current major heading.

Example:



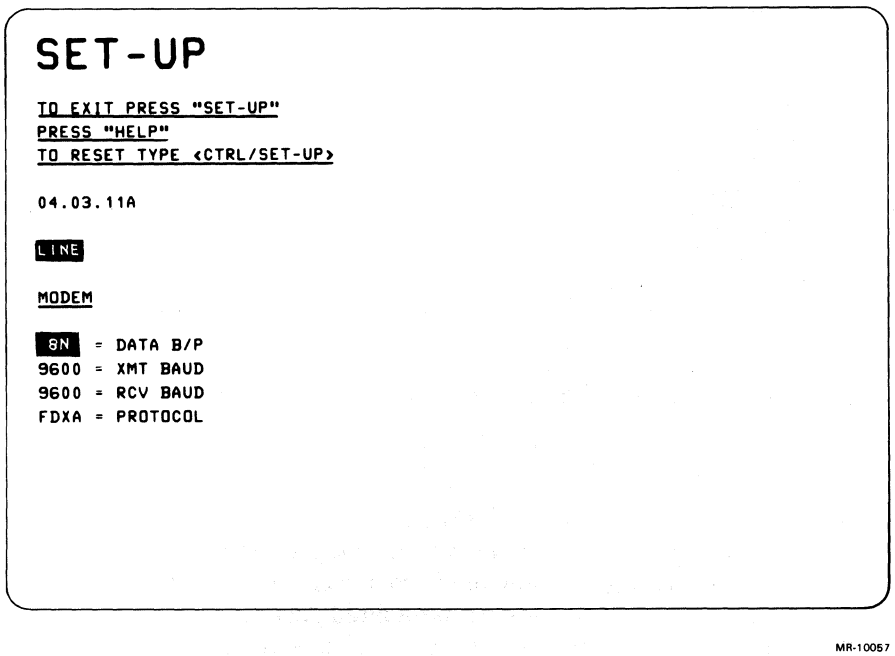
You can correct an error in the message only by exiting answerback, reentering, and retyping the message. Beginning a message with two identical characters causes the message to be erased. To save the answerback message along with the other parameters, type **<Shift/S>**.

The saved answerback message cannot be displayed once it is stored in memory. The answerback message is transmitted to the host computer when the Rainbow 100 computer receives an ENQ (enquire) control code from the host computer or an application. You can also transmit the message by typing **<Ctrl/Break>**.

2.4.4 Modem Major Heading

This major heading allows you to set the features of the communications (COMM) connector, which is on the back of the system unit. This connector allows you to attach a communications cable to a telephone modem or to another computer. Select the Modem major heading by pressing **<Next Screen>**.

A typical Modem major heading is shown in Figure 2-8. You can change the selection by pressing the → or ← key, and change the value of that selection by pressing the ↑ or ↓ key.



MR-10057

Figure 2-8 Set-Up Display – Modem

2.4.4.1 Changing Modem Data Bits and Parity – This selection determines two separate but related communications features—data bits and parity. Information travels on the communications line according to a data pattern. The pattern begins with a start bit, uses 7 data bits (common in the United States) or 8 data bits (common in other countries), adds a parity bit, and terminates with 1 or 2 stop bits. This selection determines if the computer is to use 7 or 8 data bits for each character and the type of parity to be used, as listed in Table 2-3. Press the ↑ or ↓ key to change the value to the selection needed.

Table 2-3 Modem Data Bits and Parity Selection

Characters Displayed	Data Bits per Character	Type of Parity Upon Transmission	Action on Parity Upon Reception
7O	7	Odd	Checked
7E	7	Even	Checked
7N	7	No parity	Ignored
7M	7	Mark	Ignored
7S	7	Space	Ignored
8O	8	Odd	Checked
8E	8	Even	Checked
8N	8	No parity	Ignored

2.4.4.2 Setting the Transmit Baud Rate – Press the → key to select the transmit baud rate, shown in Figure 2-8. This selection determines the speed (baud rate) at which characters are transmitted by the Rainbow 100 computer. (The current speed is shown in reverse video on the screen.) This setting must match the receive speed of the host computer. Press the ↑ or ↓ key to cycle through the following transmit baud rates. Stop when the baud rate needed is displayed.

50, 75, 110, 134.5, 150, 200, 300, 600, 1200,
1800, 2000, 2400, 3600, 4800, 9600, 19200

2.4.4.3 Setting the Receive Baud Rate – Press the → key to select the receive baud rate, shown in Figure 2-8. The receive baud rate feature selects the speed of the characters coming from the communications line as expected by the Rainbow 100 computer. This speed must be set to match the transmit speed of the host computer. Press the ↑ or ↓ key to cycle through the available receive baud rates, which are the same as the choices listed above for the transmit baud rate. You can set a receive baud rate different from the transmit baud rate as long as the host computer is set to match these different rates.

2.4.4.4 Setting Modem Protocol – This selection applies only to the terminal mode. The rules for communications, the signals used, and how the signals are interpreted all form the communications protocol. Press the → key to select the modem selection parameter shown in Figure 2-8. The protocol selected determines the method used to disconnect a telephone line. Press the ↑ or ↓ key to cycle through the available modem protocols, listed in Table 2-4. The modem protocols are explained in more detail in Paragraph 2.6.3.

Table 2-4 Modem Protocols

Characters Displayed	Modem Protocol Selected
FDXA	Full-duplex, no modem (data leads only) with or without auto-XON/XOFF control
FDXB	Full-duplex, full modem control with or without auto-XON/XOFF control
FDXC	Asymmetrical full-duplex with modem control (requires a special cable)

2.4.5 Printer Major Heading

The Printer major heading, shown in Figure 2-9, allows you to set the communications settings for the PRINTER connector, which is on the back of the system unit. This connector allows you to connect a printer, such as Digital Equipment Corporation's LA50 Personal Printer, LA100 Letterprinter 100, or LQP02 Letter-Quality Printer, to the Rainbow 100 computer. The communications settings of the printer connector must be set to match the settings on the printer. The Printer major heading has two minor headings:

- Data bits/parity
- Transmit/receive baud rate

The minor heading selected is shown in reverse video (or underlined) on the screen. You can change the minor heading by pressing the → or ← key, and change the values of each minor heading by pressing the ↑ or ↓ key.

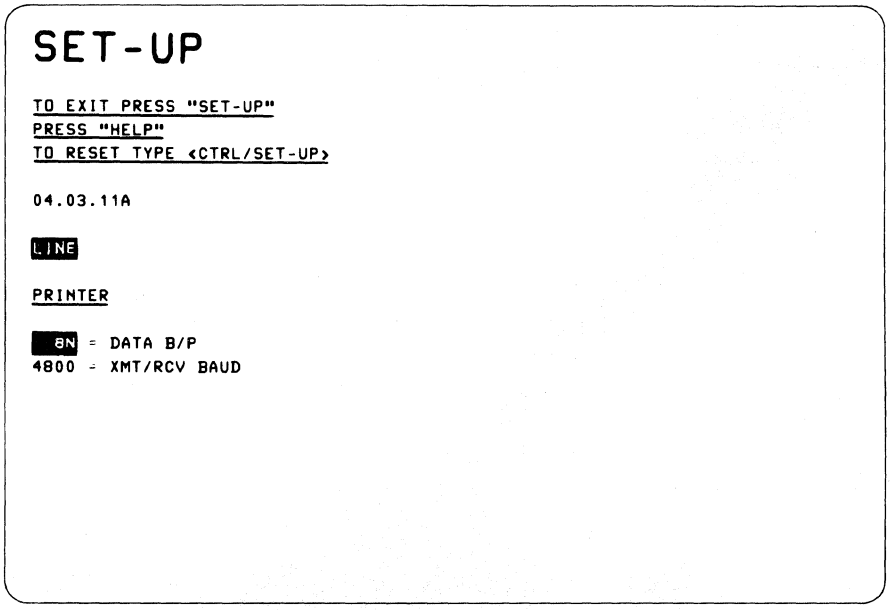


Figure 2-9 Set-Up Display – Printer

2.4.5.1 Setting Printer Data Bits and Parity – This minor heading selects the data bits per character for the printer, and also selects the parity of the data pattern. When selected, the current setting of this minor heading is shown in reverse video. Press the ↑ or ↓ key to cycle through the available selections, listed in Table 2-3. Stop when the selection needed is displayed. The selection must be set to match the settings of the printer.

2.4.5.2 Setting Printer Transmit/Receive Baud Rate – Press the → key to select the transmit/receive baud rate minor heading, shown in Figure 2-9. When selected, the current setting of the baud rate (speed) is shown in reverse video. Press the ↑ or ↓key to cycle through the baud rates available for the printer listed below. Stop when the displayed baud rate matches the baud rate set on the printer.

Baud Rate	Stop Bits
75	2
150	1
300	1
600	1
1200	1
2400	1
4800	1
9600	1

Table 2-5 lists the range of baud rates for the printers referred to above.

Table 2-5 Baud Rates for Digital Equipment Corporation's Personal Printers

Printer	Factory Set Baud Rate	Available Range
LA50 Personal Printer	4800	110 to 4800
LA100 Letterprinter 100	4800	50 to 9600
LQP02 Letter-Quality Printer	4800	110 to 9600

2.4.6 Misc Major Heading

Press **<Next Screen>** to select the Misc(ellaneous) major heading, shown in Figure 2-10. Use this heading to select the scroll rate for smooth scrolling, the keyboard bell volume, and the keyclick volume.

2.4.6.1 Scroll Rate – This feature allows you to set the smooth scroll speeds to 3, 6, or 12 lines per second by setting this parameter to 1, 2, or 3, respectively.

2.4.6.2 Bell Volume – This feature allows you to set the bell tone volume from 1 through 8 (8 is the loudest).

2.4.6.3 Click Volume – This feature allows you to set the keyclick volume from 1 through 8 (8 is the loudest).

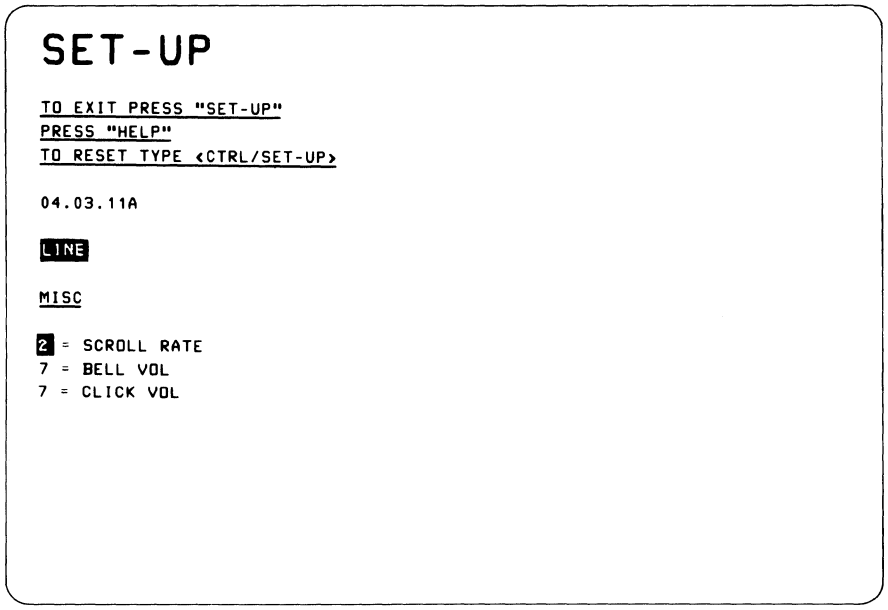


Figure 2-10 Set-Up Display – Misc(ellaneous)

2.4.7 Memory Major Heading

Press **<Next Screen>** to select the Memory major heading, shown in Figure 2-11. Use this heading when you install the Rainbow 100 memory extension option to let the computer know you have changed the size of its memory.

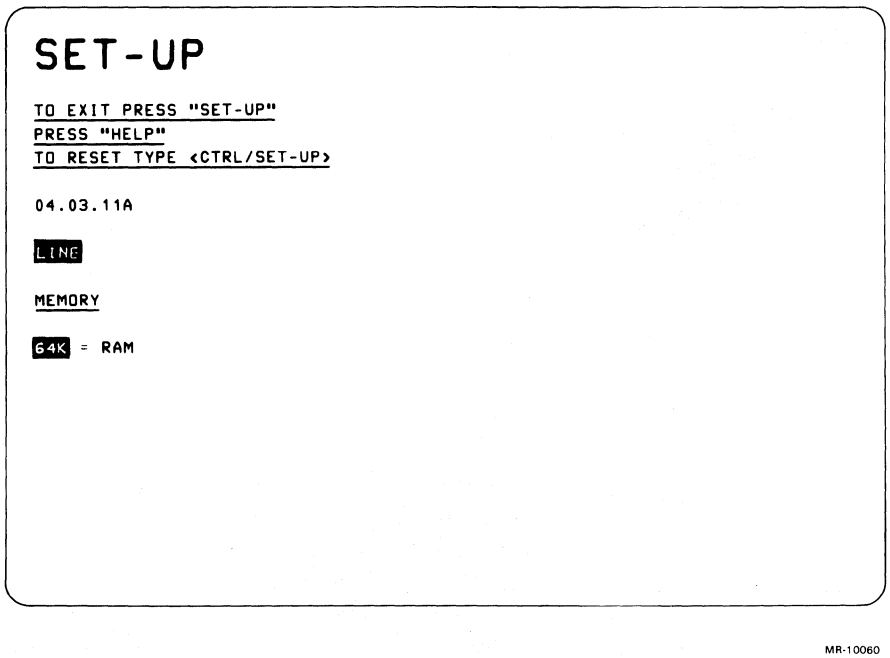


Figure 2-11 Set-Up Display – Memory

The Rainbow 100 computer has a standard memory size of 64K bytes. (The K stands for 1024; a byte represents one character position.) Adding the 64K memory extension option makes the total memory equal to 128K bytes. Adding the 192K memory extension option makes the total memory equal to 256K bytes.

Use the up and down arrows (↑, ↓) to set the parameter according to the computer's memory size.

NOTE

Using the default Set-Up parameters resets this value to 64K. If this value differs from the actual memory size, an error will be detected during selftests.

2.4.8 Save Set-Up Values

To save the values you have selected in Set-Up, hold down the **Shift** key and type **S**. This action places the values you have selected in a nonvolatile memory that preserves them for the computer when the power is turned off and on.

2.4.9 Recall Set-Up Values

When you change one or more Set-Up features, the computer uses the new values even if you have not saved them by pressing **<Shift/S>**. However, the values previously saved will be recalled when you turn off the power, or when you recall the Set-Up values by pressing **<Shift/R>**.

CAUTION

The recall action erases any text you may have had on the screen before you entered Set-Up.

2.4.10 Default Set-Up Values

When the computer was delivered from the factory, its Set-Up features were set to specific values called default values. The Parameter Settings default values are shown in Figure 2-5. To recall these default values, press **<Shift/D>**. The default values are not saved; they are just loaded into the operating memory.

NOTE

Recalling the default Set-Up values also recalls the default communications baud rates, data bits, and parity for both the COMM connector and the PRINTER connector. In addition, the memory parameter default of 64K is also recalled.

CAUTION

Recalling the default Set-Up values erases any text you may have had on the screen before you entered Set-Up.

2.4.11 Execute System Reset

While in Set-Up, press **<Ctrl>** and **<Set-Up>** at the same time to execute a system reset. The computer performs a brief selftest of its main memory, recalls its Set-Up features, and displays its Main System Menu.

If an error is found and you can still operate the system in one of its operating modes, either as a terminal or as a personal computer (but not both), an error message is displayed on the screen above the Main System Menu.

If an error message is displayed without a menu, you must find and correct the error before continuing. See Appendix B for a list of the error messages and their corrective actions.

2.5 USING THE COMPUTER'S OPERATING SYSTEM

Perform the following procedure when the Main System Menu is displayed on the screen.

1. Insert the operating system diskette in one of the diskette drives.
2. Close the diskette drive door.
3. Press the **A**, **B**, **C**, or **D** key, depending upon which drive contains the operating system.
4. The Rainbow 100 computer is now under the control of the operating system you just inserted in the drive. If you are using the CP/M-86/80 operating system, refer to the *Rainbow™ 100 Getting Started* manual. For all other operating systems, refer to the appropriate user's manual.

2.6 USING A HOST COMPUTER OPERATING SYSTEM

This paragraph describes how the Rainbow 100 computer communicates with a host computer by a telephone line (and modem) or by direct connection, as shown in Figure 2-12. In either case, the communications connector (labeled COMM) on the back of the system unit is used. This paragraph defines the signals transmitted through this connector and how in the case of a telephone connection each modem protocol (as selected in Set-Up) uses these signals.

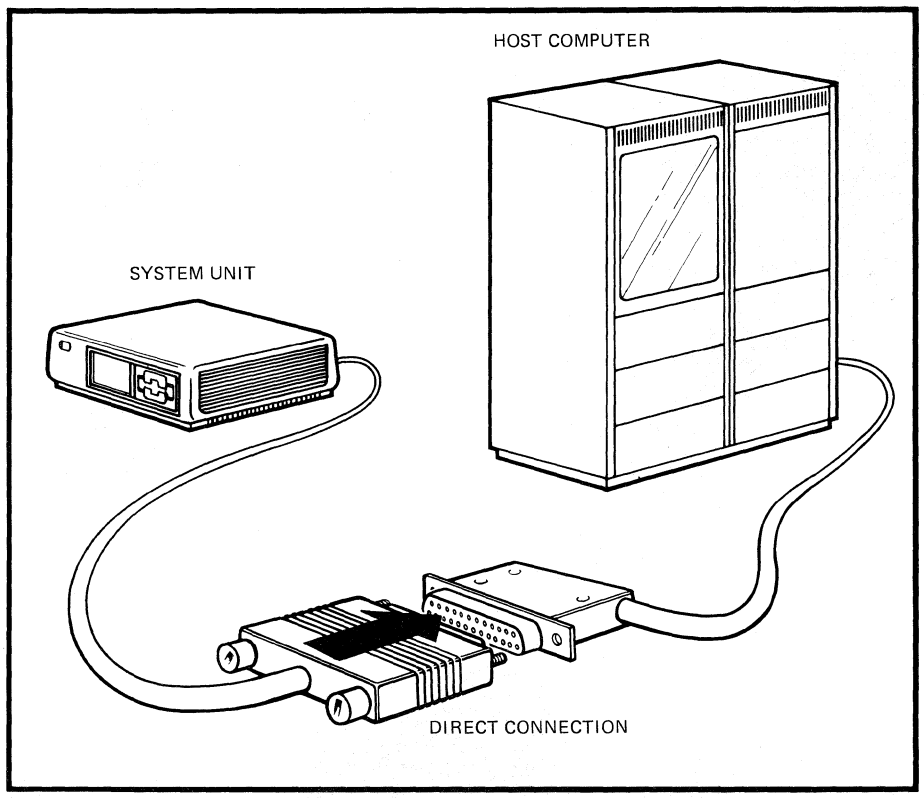


Figure 2-12 Connecting the Rainbow 100 Computer to a Host Computer

2.6.1 Connecting the Rainbow 100 Computer to a Host Computer

When using a telephone line, a modem (data set) is needed. The modem changes the signals produced by the Rainbow 100 computer into signals that can be transmitted over the telephone line. Many types of modems are available, but the modems on both ends of the telephone line must be compatible with each other.

2.6.1.1 Cables – Cables used to connect the communications connector with most asynchronous, Bell System-type modems must be asynchronous modem cables with an RS-232 female connector on one end and a corresponding male connector on the other. Digital Equipment Corporation's BCC04 (or BCC14) modem cable meets these requirements.

Cables used to connect the communications connector with most synchronous, Bell System-type modems must be synchronous modem cables with an RS-232 female connector on one end and a corresponding male connector on the other. Digital Equipment Corporation's BC22C modem cable meets these requirements. (Synchronous communications requires a special application program.)

Different cables may be required by other serial devices. Check with the devices' vendors for more information.

2.6.1.2 Connection – Use the following procedure to connect the Rainbow 100 computer to a modem:

1. Set the power switch (marked 1/0) on the front of the system unit to 0 (off).
2. If the system unit is installed in the optional floor stand, open the door on the back of the floor stand to access the back of the system unit.
3. Connect the female connector of the modem cable to the communications connector (COMM) on the back of the system unit. Refer to Figure 2-13 if you are not using the optional floor stand, and Figure 2-14 if you are. Tighten the cable's hold-down screws.
4. Connect the other end of the modem cable to the modem and tighten the cable's hold-down screws.
5. Close the door on the floor stand (if applicable).
6. Connect the modem's ac power cord to a wall receptacle. If the modem has a power on/off switch, turn on the modem.
7. Turn on the Rainbow 100 computer.

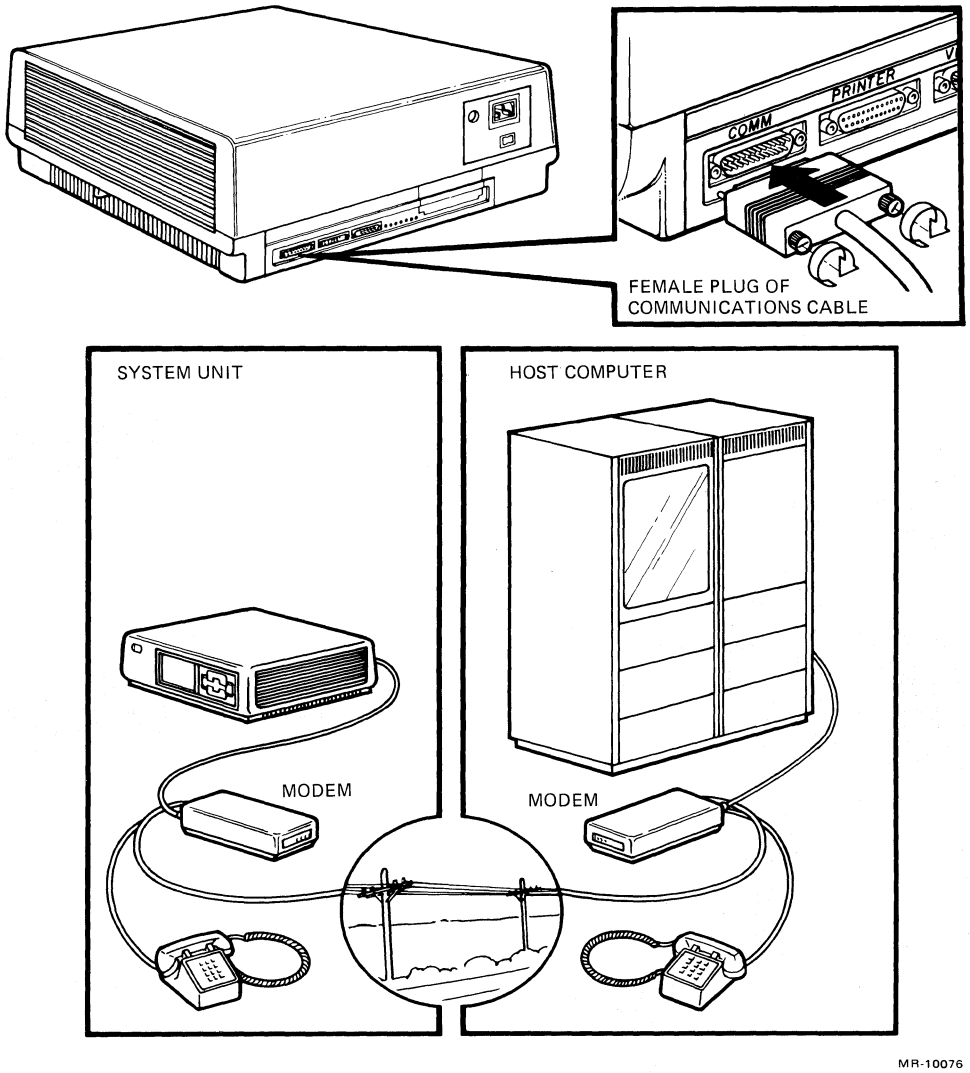


Figure 2-13 Connecting a Communications Cable to the System Unit (Without Floor Stand)

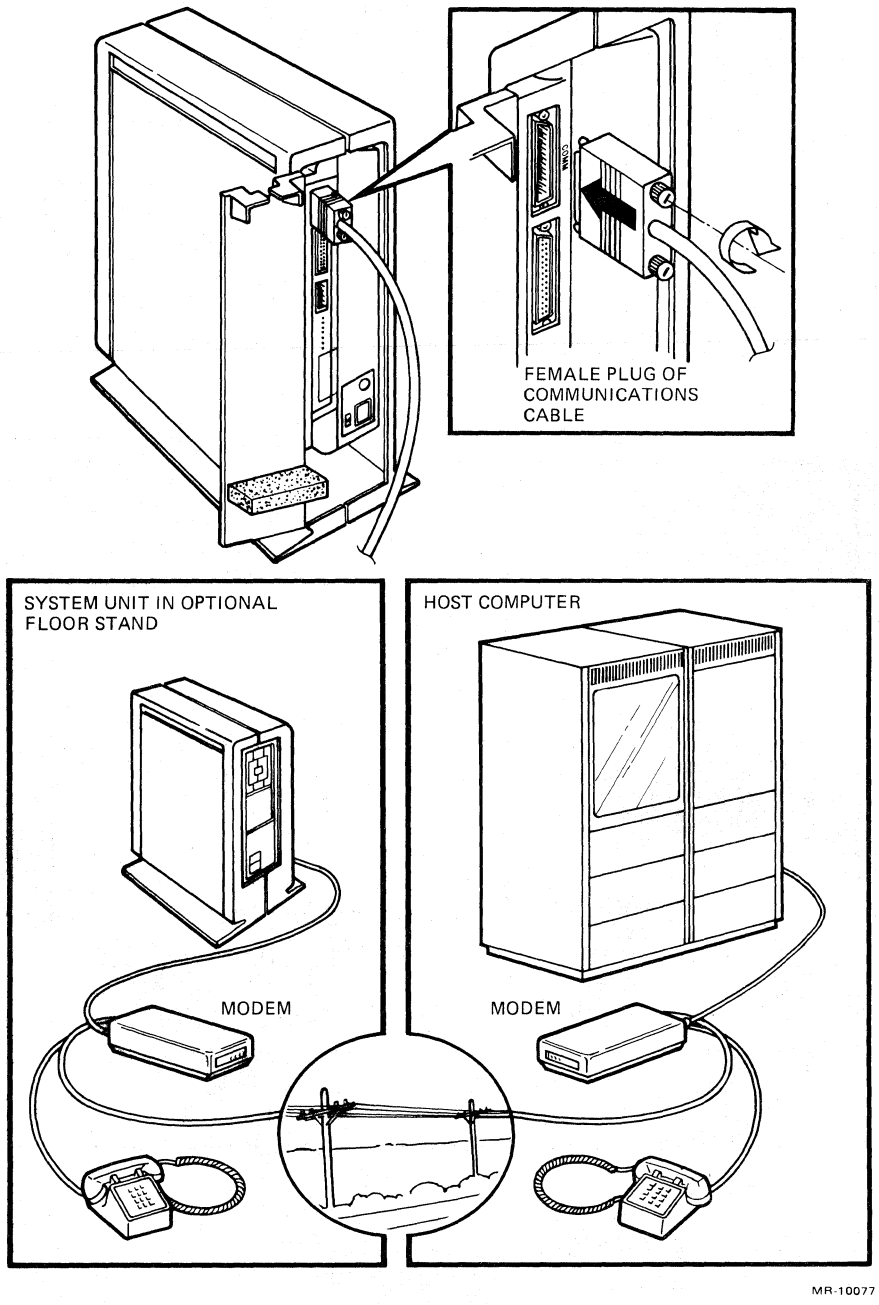


Figure 2-14 Connecting a Communications Cable to the System Unit in the Floor Stand

2.6.2 Communications Set-Up Parameters

You can change the following communications parameters on the Rainbow 100 computer:

- Data bits per character
- Parity
- Transmit speed (baud rate)
- Receive speed (baud rate)
- Protocol
- Auto-XON/XOFF
- Transmit break
- Modem stop bits
- Received character parity
- Disconnect delay
- Disconnect character use

Refer to Paragraph 2.4 for directions on setting these parameters.

2.6.3 Modem Protocol

The Rainbow 100 computer uses a full-duplex modem. A full-duplex modem transmits and receives characters at the same time.

The rules for communications, the signals used, and how the signals are interpreted all form the communications protocol. In the Rainbow 100 computer you can select one of three communications protocols, listed in Table 2-6.

Table 2-6 Communications Protocols

Selection	Description	Usual Application
FDXA	Full-duplex with no modem control (data leads only)	Full-duplex communications with direct connection to a remote computer or with a modem that does not use modem control signals.
FDXB	Full-duplex with modem control	Full-duplex communications with a modem that uses modem control signals.
FDXC	Asymmetrical full-duplex with modem control	Full-duplex communications with a half-duplex modem using the secondary channel. FDXC requires a special cable.

2.6.3.1 Full-Duplex With No Modem Control (FDXA) – The FDXA selection allows the Rainbow 100 computer to communicate without using modem control signals. The computer is ready to transmit or receive when its power is turned on and it is on-line.

FDXA Connect Conditions – When the Rainbow 100 computer is turned on, it enables Data Terminal Ready and Request to Send. Communication is then allowed.

FDXA Disconnect Conditions – The Rainbow 100 computer disconnects the telephone line by turning off Data Terminal Ready. This signal is turned off when any one of the following occurs:

- A disconnect character is received.
- A recall or system reset is executed.
- A **Shift/Break** is typed.

2.6.3.2 Full-Duplex With Modem Control (FDXB) – The FDXB selection allows the Rainbow 100 computer to communicate with a modem that uses modem control signals (such as Clear to Send and Data Set Ready). These control signals make sure that a connection occurs and is maintained before and during the communication process. Communication stops if the connection is not maintained.

FDXB Connect Conditions – The signals shown in Table 2-7 must be enabled before communication is allowed.

Table 2-7 Modem Connect Conditions

Name	Signal	Source
CTS	Clear to Send	Modem
DSR	Data Set Ready	Modem
RLSD	Receive Line Signal Detector (Carrier Detect)	Modem
DTR	Data Terminal Ready	Rainbow 100 computer

FDXB Disconnect Conditions – The Rainbow 100 computer disconnects the telephone line by turning off Data Terminal Ready. This signal is turned off when any one of the following occurs:

- The Rainbow 100 computer is placed off-line.
- A recall or system reset is executed.
- A disconnect **<Shift/Break>** is enabled.
- A disconnect character is received, and the disconnect character enable Set-Up selection is on.
- Data Set Ready (DSR) is turned off.
- Receive Line Signal Detector (RLSD) is lost longer than the time allowed by the disconnect delay Set-Up selection.
- RLSD is not turned on within 30 seconds after DSR is turned on.

2.6.3.3 Asymmetrical Full-Duplex (FDXC) – With the FDXC selection, the Rainbow 100 computer can use full-duplex communications on a half-duplex modem. The Rainbow 100 computer receives characters on the primary channel and transmits characters on the secondary channel at 75 baud.

To use this protocol, the modem must support a secondary channel. This is accomplished through a special cable that redirects the secondary transmitting signals, leaving the modem to the Rainbow 100 computer's primary transmitting signals.

The secondary signals from the modem are: SRTS; SCTS; and STXD. These are mapped to the primary side of the Rainbow 100 computer: RTS; CTS; TXD.

FDXC Connect Conditions – The signals shown in Table 2-7 must be enabled before communication is allowed.

FDXC Disconnect Conditions – The Rainbow 100 computer disconnects the telephone line by turning off Data Terminal Ready. This signal is turned off under the same conditions specified for FDXB.

2.6.4 Break

You can enable or disable a Break signal by using the transmit break Set-Up selection. The Break signal is a transmitted space (0) condition that lasts 0.275 seconds (±10%) on the transmit data line. The host computer's response to the Break signal depends on the type of computer and its software.

A disconnect **<Shift/Break>** can always be performed when the Rainbow 100 computer is in terminal mode and on-line. It turns off the Data Terminal Ready (DTR) and Request to Send (RTS) signals.

When the disconnect character enable Set-Up selection is on, the Rainbow 100 computer transmits the disconnect character before it turns off the DTR and RTS signals.

Typing **<Shift/Break>** is the usual way to disconnect the Rainbow 100 computer from its communications line.

2.6.5 Auto-XON/XOFF

It is recommended that you have the auto-XON/XOFF Set-Up feature on. With this feature, the Rainbow 100 computer automatically sends an XOFF control character when it receives more characters than it can handle. The XOFF control character tells the host computer to stop sending data. When the Rainbow 100 computer can accept more data, it sends an XON control character to the host computer to tell it to continue transmitting data.

2.6.6 Communications Connector Signals

The communications connector signals meet the following standards:

- Electronic Industry Association (EIA) RS-423 and RS-232-C
- International Telegraph and Telephone Consultative Committee (CCITT) recommendations V.21, V.22, V.23, V.24, and V.28

The communications connector's pin numbers are shown in Figure 2-15. The signals on each pin are listed in Table 2-8. This table also lists the signals used by each modem protocol. Signals and pins not listed are not used by the Rainbow 100 computer.

Table 2-8 Communications Connector Signals

Pin	Signal	Name	CCITT/EIA	FDXA	FDXB	FDXC	Description
1	Protective Ground	PROT GND	101/AA	X	X	X	Chassis ground; ac power cord ground.
2	Transmitted Data	TXD	103/BA	X	X	X	Data transmitted from the Rainbow 100 computer; asserted high (Mark state) when not transmitting.
3	Received Data	RXD	104/BB	X	X	X	Characters received from the remote computer.
4	Request to Send	RTS	105/CA	X	X	X	On when the Rainbow 100 computer is on-line, and off when off-line.
5	Clear to Send	CTS	106/CB	X	X	X	Indicates the modem is ready for transmission.
6	Data Set Ready	DSR	107/CC	X	X	X	Indicates the modem is in data mode.
7	Signal Ground	SGND	102/AB	X	X	X	Common ground for internal circuits (except protective ground).
8	Receive Line Signal Detector (Carrier Detect)	RLSD	109/CF	–	X	X	The modem turns this signal on when the carrier signal is of sufficient quality and magnitude.
12	Speed Indicator	SI	112/CI	–	X	–	When on, the transmit and receive speeds are 1200 baud; when off, these speeds are as established in Set-Up.
13	Secondary Clear to Send*	SCTS	121/SCB	–	–	X	When on, the modem is ready for the Rainbow 100 computer to transmit data; when off, the modem is not ready.

X = Used with this protocol selection.
*These signals are supported by using a special cable for FDXC modem protocol.

Table 2-8 Communications Connector Signals (Cont)

Pin	Signal	Name	CCITT/EIA	FDXA	FDXB	FDXC	Description
14	Secondary Transmit Data*	STXD	118/SBA	-	-	X	Transmits secondary channel information, such as Break signals; Mark state when no characters are transmitted.
15	Transmitter Clock	TSET	114/DB				External clock from the modem.
17	Receiver Clock	RSET	115/DD				External clock from the modem.
19	Secondary Request to Send	SRTS	120/SCA	-	-	X	When on, the Rainbow 100 computer is ready to receive characters; when off, the computer is ready to transmit characters.
20	Data Terminal Ready	DTR	108.2/CD	X	X	X	When on, the Rainbow 100 computer is ready to receive data; when off, this signal causes the modem to disconnect and not answer calls.
22	Ring Indicator	RI	125/CE	-	-	-	Ignored; used by the modem.
23	Speed Select	SPDS	111/CH	-	X	-	When on, the Rainbow 100 computer's receive speed is greater than 600 baud; when off, the computer's receive speed is equal to or less than 600 baud.

X = Used with this protocol selection.
*These signals are supported by using a special cable for FDXC modem protocol.

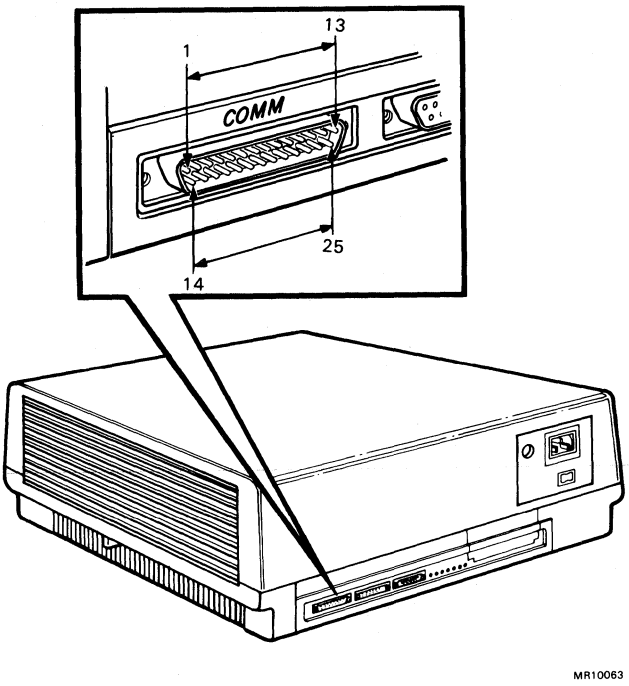


Figure 2-15 Communications Connector Pin Numbers

2.7 USING RAINBOW 100 COMPUTER DIAGNOSTICS

When you first power up the Rainbow 100 computer, it performs some abbreviated diagnostic selftest procedures. However, an added selftest and a diskette diagnostic procedure may also be used to test the Rainbow 100 computer. These procedures are described in Chapter 10, Testing and Troubleshooting.

CHAPTER 3
SYSTEM TECHNICAL DESCRIPTION

3.1 INTRODUCTION

This chapter describes the function and interaction of each hardware component comprising the Rainbow 100 personal computer, which is a system consisting of several functional or replaceable units. The purposes and major functions of the units are described in this chapter at the system level. The detailed unit level descriptions are provided in subsequent chapters devoted to each unit.

3.2 BASIC SYSTEM COMPONENTS

The Rainbow 100 computer consists of three components: the system unit, the monitor, and the keyboard. These three components are shown in Figure 3-1.

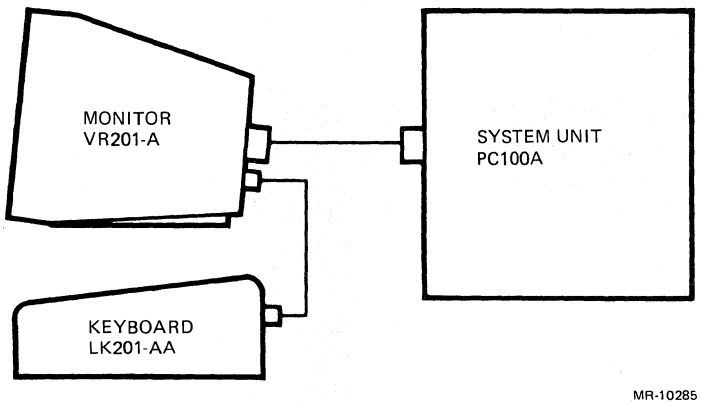


Figure 3-1 Rainbow 100 Computer Basic System Components

The system unit is the main component of the system and contains assemblies and modules that are functionally independent of the computer system. This design makes it easy to replace parts and add hardware options.

3.2.1 System Unit

The system unit is the part of the Rainbow 100 computer that controls the rest of the system, does the computing tasks, and stores information. It contains the system module, the RX50 controller, the RX50 diskette drive(s), the power supply, and the power switch and fan assembly. Figure 3-2 is a block diagram that shows where each component fits in the system unit. The figure also shows where the RX50 controller module and option modules fit on the system module.

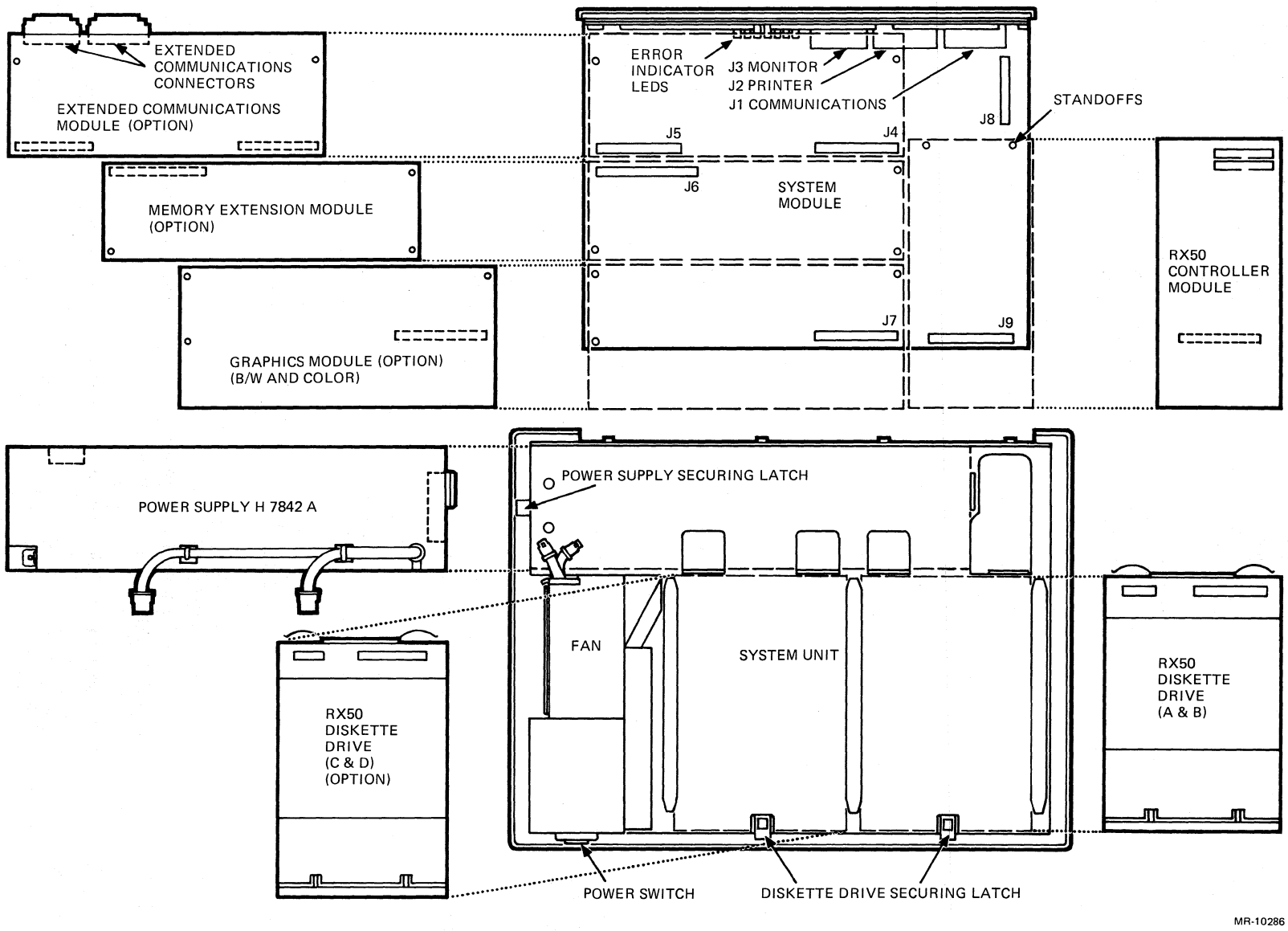


Figure 3-2 System Unit Physical Block Diagram

The system module contains the 8088 and Z80A processors and support circuits. It provides the basic intelligence of the system as well as a way to interconnect all options. The system module lies horizontally along the bottom of the system unit and is secured by thumbscrews to the rear panel. When released, the system module slides out of the rear of the system unit. Standoffs on the system module support any installed options.

The H7248A power supply is a 138 W switching regulator power supply with a switch selectable 115/230 Vac primary circuit. The power supply provides dc power for the system module and any installed options, the keyboard, RX50 diskette drives, and the video monitor. The power supply fits into a slot in the mounting plate of the system unit and is secured by a slide tab.

The RX50 diskette drive unit is a dual platter system that drives two diskettes and is the main storage device for the Rainbow 100 system. The RX50 diskette drive permits the Rainbow 100 computer to read, write, and store data on 133.4 mm (5-1/4 in.) diskettes. Each diskette stores 400K bytes of data, or 800K bytes for each dual-diskette drive unit. Two of these dual-diskette drive units can be installed in the system unit.

The RX50 diskette drive(s) slide into the front of the system unit on plastic tracks located on the mounting plate. The drive unit is secured by a locking/release tab on the front of the system unit.

3.2.2 Video Monitor (VR201)

The video monitor supplies video information to the user by a 30.5 cm (12 in.) diagonal nonglare screen. The monitor housing contains the CRT, yoke assembly, and video monitor board. Two external controls on the rear of the monitor housing adjust the screen brightness and contrast. Also mounted on the rear of the monitor housing are a 15-pin video connector and a 4-pin keyboard connector.

A two meter (six foot) BCC02 cable is used to connect the video monitor to the system unit. This cable carries power, video signals, and keyboard transmit and receive data to the video monitor. The power and keyboard transmit and receive data are routed through the 4-pin connector on the video monitor to the keyboard.

3.2.3 Keyboard (LK201)

The keyboard allows the operator to enter information to the system unit for processing or storage. The keyboard also has a bell-tone generator and four lights (LEDs).

The keyboard case contains the keyboard switch matrix and a printed circuit board. The printed circuit board contains the electronic circuitry to process, control, and transfer information entered from the keyboard or received from the system unit. The keyboard has 105 keys arranged in four groups.

The keyboard is connected to the monitor by a two meter (six foot) BCC01 coiled cable. This cable carries the keyboard power and received data from the system unit and the keyboard transmitted data to the system unit.

3.3 SYSTEM FUNCTIONAL DESCRIPTION

The system block diagram (Figure 3-3) shows the relationship between the basic logic elements of the Rainbow 100 system module and the other system components.

A functional description of the system module and the other system components is presented in the following paragraphs.

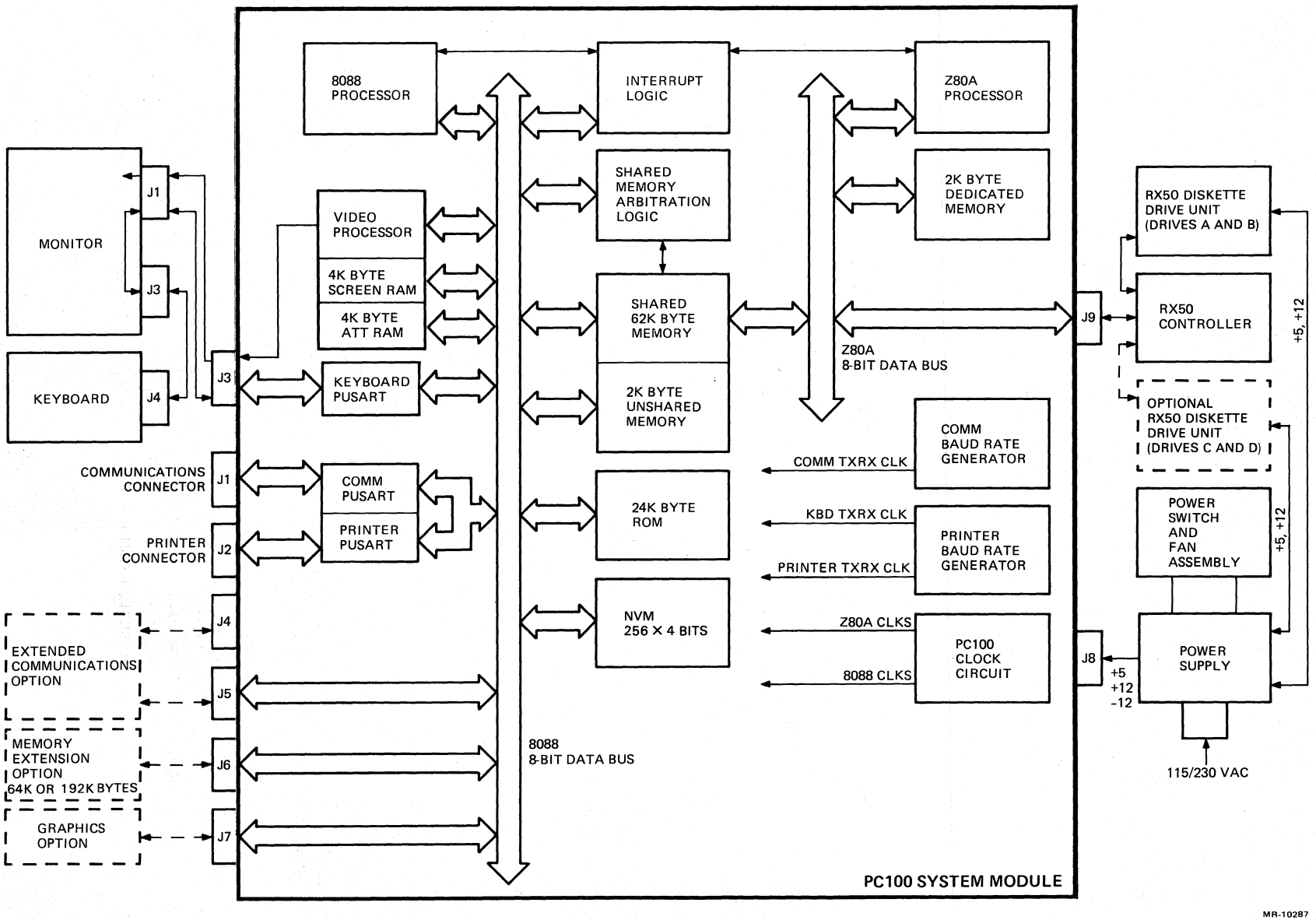


Figure 3-3 Rainbow 100 System Block Diagram

3.3.1 System Module

The PC100 system module includes a two-processor architecture based on the simultaneous operation of an 8088 processor and a Z80A processor. These processors operate from and transfer data through a shared block of 62K bytes of RAM. In addition to this block of shared memory, each processor has its own 2K bytes of unshared RAM and peripheral circuitry.

Each processor supports a needed function of the system module in addition to running application/user software. The Z80A performs the functions required to read from and write to the RX50 diskette drive. The 8088 handles the video output to the monitor, keyboard I/O, printer port, and communications with a host computer as well as any other options installed on the system module.

The system module includes the following features:

- 8088 processor
- Z80A processor
- 64K byte dynamic RAM (62K byte shared and 2K byte unshared)
- 2K byte static RAM
- 24K byte ROM (bootstrap, diagnostics, terminal mode)
- 256 × 4 bits nonvolatile memory
- 4K byte screen RAM
- 4K byte attribute RAM
- Asynchronous/bisynchronous communications port
- Printer port
- LK201 keyboard interface
- RX50 diskette drive controller (on separate module)
- Option expansion capability
    - Extended memory (64K or 192K bytes)
    - Color graphics
    - Extended communications

3.3.1.1 8088 Processor – The 8088 processor controls most of the system module functions. It features a 20-bit address bus, an 8-bit data bus, and 16-bit internal architecture. The 8088 operates at a frequency of 4.815 MHz and controls the following elements in the system:

- Video Monitor
- Keyboard
- Printer
- Communications line
- Optional color/graphics module
- Optional extended communications module
- Optional extended memory module

The 8088 also controls the RESET input of the Z80A processor and thus can start or stop the Z80A at any time.

If the 8088 tries to access the shared memory while it is being used by the Z80A or refresh logic, the shared memory arbitration logic causes the 8088 to enter wait states until the Z80A or refresh logic complete their cycles and release the shared memory.

3.3.1.2 8088 Memory – The memory available to the 8088 processor consists of ROM, RAM, and nonvolatile RAM. The memory types and memory sizes are the following:

- 64K byte dynamic RAM (62K byte shared with Z80A)
- 24K byte ROM
- 4K byte video screen RAM (static)
- 4K byte video attribute RAM (static)
- 256 × 4 bits nonvolatile memory (NVM)
- 64K or 192K byte optional unshared dynamic RAM

3.3.1.3 Shared Memory – The 64K byte shared memory consists of eight 64K × 1 bit dynamic RAM chips. The 8088 processor has access to all 64K bytes of memory and uses the first 2K bytes to store interrupt vectors and other information that must not be changed by the Z80A processor. For this reason, the Z80A cannot access the first 2K bytes and can only use the last 62K bytes of this memory. Parity generation/detection is not implemented with the 64K byte shared RAM. The shared memory can be accessed by the 8088, the direct memory access (DMA) channels of the extended communications option, the Z80A, and the refresh logic. A shared memory arbitration circuit monitors memory access requests to establish the priority and decides which device is allowed to access the memory. Refresh has the highest priority for memory cycles. The 8088 has approximately equal priority with the Z80A except in those instances where both processors simultaneously request access to the shared memory. If the 8088 and the Z80A simultaneously contend for access to memory, the shared memory arbitration logic will give memory priority to the Z80A.

3.3.1.4 24K Byte ROM – There are 24K bytes of ROM on the system module that is addressable by the 8088. The ROM consists of three 8K × 8 chips that contain Z80A code and 8088 code for diagnostic testing, bootstrap, and VT102 emulation programs. The programs for the Z80A must be moved into shared memory by the 8088 before they can be executed by the Z80A.

When the 8088 accesses this memory, wait states are not required. However, wait states are required when the refresh logic executes refresh cycles because the refresh logic assumes that all memory is dynamic RAM.

The system module supports ROMs of the 2732/2764 pinout variety with access times equal to or less than 450 ns.

3.3.1.5 NVM – The system module contains 1024 bits of nonvolatile memory (NVM) arranged in a 256 × 4 bit matrix. The NVM is used to store programmable system configuration information that would otherwise have to be reentered every time the system was powered up.

The device contains a 256 × 4 bit static RAM that overlays a 256 × 4 bit NVM. The static RAM stores the Set-Up information on a temporary basis while the NVM stores the Set-Up information on a permanent basis. When the system is initialized, the 8088 processor does a RECALL of the NVM to transfer the data stored in the NVM to the static RAM. After the system has been initialized, any read or write to the device will read data from or write data to the static RAM. Data in the static RAM can be stored in the NVM on a permanent basis by performing a SAVE operation during the Set-Up procedure. The Set-Up information stored in the NVM will determine the system configuration when the system is turned off and on.

3.3.1.6 4K Byte Screen RAM and 4K Byte Attribute RAM – The screen RAM and attribute RAM are static memories that are used by the 8088 processor and the video processor logic. The 8088 uses these memories to temporarily store the character and attribute data to be displayed on the screen of the monitor. The video processor directly accesses the memories and converts the data into electrical signals that the screen displays as letters, numbers, and symbols.

The contents of the screen RAM directly control the display of the lines and characters on the monitor. The contents of the attribute RAM determine the character, line, and screen attributes. The 8088 modifies and updates the information in the screen and attribute RAMs during the time the RAMs are not being accessed by the video processor.

The memories are available to the 8088 approximately 90 percent of the time during the operation of a typical program. In the remaining 10 percent of the time, the video processor accesses these memories and the 8088 is held in a wait state. The longest time that the 8088 can be held in a wait state due to memory contention with the video processor is approximately 65 microseconds.

3.3.1.7 Video Processor – The video processor is controlled by the 8088 processor. It converts character and attribute data supplied by the 8088 into a video signal that the monitor circuits use to generate an alphanumeric/graphics display. The video signal sent to the monitor is a composite of two types of signals, video and sync. The video portion of the composite video signal varies the intensity of the electron beam in the monitor's cathode ray tube (CRT) to produce the visible display. The sync portion of the composite video signal determines the horizontal and vertical position of the display on the CRT.

The video processor provides the following features for the monitor display:

- 24-line × 80- or 132-column display
- Jump or smooth scrolling
- Double-height characters (by line)
- Double-width characters (by line)
- Normal and reverse video (by character)
- Boldface, blinking, and underlined characters (by character)
- Dark or light screen background
- Auto-screen blanking
- 256 character set
- Composite video output

The video processor includes two central devices (DC011 timing and DC012 control chips) and supporting logic including 4K bytes of screen RAM, and 4K bytes of attribute RAM, a 4K × 8 bit character generator ROM. The DC011 is a custom designed, bipolar, integrated circuit that provides most of the timing signals needed by the video processor. The DC012 control chip is also a custom designed, bipolar, integrated circuit. The DC012 accepts attribute specifications and timing signals and delivers addresses to the character generator ROM and attributes for video output to the monitor. The character generator ROM is a 4K × 8 bit ROM that is addressed by the coded representation of the desired character stored in the screen RAM. Each code is used as the high 8 bits of a 12-bit address to the character generator ROM. The low 4 address bits for the character generator ROM are provided by a scan counter in the DC012.

3.3.1.8 Keyboard Interface – The keyboard communicates with the 8088 processor through an RS-423 full-duplex connection to an 8251A programmable universal synchronous/asynchronous receiver-transmitter (PUSART). The PUSART takes parallel data from the 8088 data bus, converts the parallel data to a serial format, and transmits the data to the keyboard via connectors on the monitor. Input serial data from the keyboard is received by the PUSART, converted to parallel data, and placed on the 8088 data bus.

The PUSART communicates asynchronously with the keyboard at a fixed 4800 baud rate. The serial data is transmitted and received in an 8-bit, no parity character format. The 8088 processor programs the PUSART to operate with several standards and parameters. Character length, number of stop bits, parity enabling and format, baud rate multiplication factor, and asynchronous operation are all programmed in at power-up through the mode instructions from the 8088.

3.3.1.9 Communications and Printer Interface – The communications and printer interface functions are performed by a dual-channel multiprotocol serial controller (MPSC). The MPSC is a microcomputer peripheral device that can be programmed to support the following three basic communications protocols:

1. Asynchronous (start/stop)
2. Byte synchronous (monosync/bisync)
3. Bit synchronous (high level data link control [HDLC], synchronous data link control [SDLC])

The flexible architecture of this controller allows the basic protocol unit or frame to be built into increasingly complex protocols by defining special control characters and fields, and by grouping frames together into larger units. Virtually all communications protocols currently in use are based on one of the three basic protocols.

Communications Connector – The MPSC provides two independent serial receiver/transmitter channels. The communications connector uses one channel and the printer connector uses the other channel. The MPSC is a single, 40-pin integrated circuit (IC) that implements the following functions:

- Parallel-to-serial and serial-to-parallel data conversion
- Buffering of outgoing and incoming data, allowing the processor time to respond
- Insertion and deletion of framing bits and characters
- Calculation and checking of parity and cyclic redundancy check (CRC) error checking
- Informing the processor when and what action needs to be taken
- Interfacing with the outside world over discrete modem control lines

The MPSC can be programmed by the 8088 processor to operate in a nonvectored (polled) or vectored interrupt mode.

The communications connector of the MPSC is used to communicate with a host computer either directly or by telephone lines (and modem). The Rainbow 100 computer can be connected to a host computer and operated in its terminal mode, similar to a VT102 terminal. Detailed information for the VT102 can be obtained from the *VT102 Video Terminal User's Guide* (EK-VT102-UG-003). The terminal emulation program is part of the firmware located in the 24K byte ROM.

The serial data and modem control signals are transmitted and received through a 25-pin D-type communications connector located on the system module. This communications connector has full modem control. This connector has asynchronous as well as bisynchronous modes (with specific applications only) with Electronic Industry Association (EIA) RS-423 and RS-232-C interface standard conforming to International Telegraph and Telephone Consultative Committee (CCITT) recommendations V.21, V.22, V.23, V.24, and V.28. Break detection is also supported by this connector.

The baud rates for the communications connector are selected to match the baud rates of the host computer by a Set-Up procedure and are stored in the NVM. This procedure sets the communications baud rate generator on the system module. The transmit and receive baud rates can be independently programmed (split baud operation). The following baud rates are available:

50, 75, 110, 134.5, 150, 200, 300, 600, 1200,

1800, 2000, 2400, 3600, 4800, 9600, 19200

The communications connector supports the following modem control signals:

- Receive data
- Transmit data
- Secondary transmit data
- Request to send
- Secondary request to send
- Clear to send
- Secondary clear to send
- Receive line signal detect
- Secondary receive line signal detect/speed indicator (Bell 212A)
- Ring indicator
- Data set ready
- Speed select

Printer Connector – The printer connector of the MPSC is a general purpose printer port that provides signals that meet the EIA recommendations RS-423 and RS-232-C, and the CCITT recommendation V.28. The printer connector is a 25-pin D-type connector located on the system module.

NOTE
This connector is wired as data communications equipment (DCE) and therefore appears to a printer as though it were a modem.

The following signals are available at the printer connector:

- Printer transmit data
- Printer receive data
- Data terminal ready
- Data set ready (asserted high)
- Clear to send (asserted high)

The baud rates for the printer connector are selected by a Set-Up procedure. This procedure programs the printer baud rate generator on the system module. These baud rates must be set to match the transmit/receive speed of the printer being used. Transmit and receive baud rates cannot be set independently. The following printer transmit/receive baud rates are available:

75, 150, 300, 600, 1200, 2400, 4800, 9600

The printer port can be programmed to provide the different character formats required by different types of printers. The following character format selections are available:

- Number of data bits per character (7 or 8)
- Parity (odd, even, mark, space, or none)

3.3.1.10 Z80A Processor – The Z80A is the processor that has access to the RX50 controller and thus is responsible for controlling the diskette drive unit(s) via programmed I/O instructions for all applications. The Z80A transfers data and internal state information through an 8-bit bidirectional data bus. Memory and peripheral device addresses are transmitted over a separate 16-bit unidirectional address bus.

The Z80A internal registers contain 208 bits of read/write memory that are accessible to the programmer. All Z80A output signals are fully decoded and timed to control the 62K bytes of shared memory, 2K bytes of dedicated memory, and the RX50 controller.

The Z80A runs at a frequency of 4.0 MHz (250 ns clock period). Accesses to the 2K bytes of dedicated memory do not require wait states by the Z80A. Shared memory accesses cause Z80A wait states on machine one (M1) cycles and for cycles in which there is contention for the memory by the 8088 processor or refresh logic.

The only interrupts to the Z80A are nonmaskable interrupts from the 8088. When the Z80A is interrupted, it places a vector address on the Z80A bus that causes the processor to execute a mode 0 restart (RST) 30 instruction.

3.3.1.11 Z80A Shared Memory – The 64K bytes of memory available to the Z80A processor consist of 62K bytes of memory that is shared with the 8088 processor and 2K bytes of memory dedicated to the Z80A. Accesses to the shared portion of the memory select the corresponding address in the standard bank of 64K byte RAMs. Accesses to the unshared portion of the memory will cause the Z80A memory address decoding logic to select the 2K bytes of dedicated static RAM.

3.3.1.12 Z80A 2K Byte RAM – The Z80A dedicated memory is a 2K × 8 bit static RAM contained in a 24-pin IC package. The dedicated RAM can be accessed by the Z80A processor at any time without any wait states. If the shared RAM is "busy" at the time of Z80A access, the Z80A will execute wait states until the RAM is free. The RAM is considered "busy" when an 8088 cycle or a refresh cycle is in progress or is pending. In addition to wait states due to memory contention, all M1 cycles from the shared RAM have one extra wait cycle due to the timing for this type of machine cycle. In any case, the Z80A is held in a wait state for no longer than approximately two microseconds. If both processors are executing out of the shared memory, the Z80A cannot reliably access the diskette drive unit(s), resulting in errors caused by lost data.

3.3.1.13 Interrupt Logic – Interrupts in the 8088 processor can be hardware or software initiated. Software interrupts originate from program execution (for example, execution of a breakpoint instruction) or indirectly through program logic (for example, attempting to divide by zero). Hardware interrupts originate from external logic and are classified as maskable interrupts. All interrupts, whether software or hardware initiated, result in the transfer of control to a new program location.

The 8088 can be interrupted by any one of seven devices. Each device is assigned an interrupt priority level and an 8-bit interrupt type number. The interrupt logic supplies the interrupt type number and places it on the 8088 address/data bus during the interrupt acknowledge sequence. The type number is used by the 8088 to vector through a 256-element table to the new vector address of the interrupt service program.

Table 3-1 lists the interrupt sources, the priority levels, interrupt type numbers, and vector addresses.

The 8088 is the only source of interrupts for the Z80A. Interrupts to the Z80A processor are nonmaskable interrupts and must be enabled in software in order to operate. The Z80A must be programmed to service interrupts in the mode 0 interrupt response mode.

When the Z80A accepts an interrupt from the 8088, it acknowledges the interrupt by placing a hardwired 8-bit interrupt vector address on its data bus. The interrupt vector address (F7H) causes the Z80A to execute a restart (RST) instruction at restart location 30H in page 0 of memory.

Table 3-1 8088 Interrupt Addresses

Priority Level*	Interrupt	Interrupt Source	Interrupt Type†	Vector Address†
7	Vertical Frequency	Video Processor	20	80
6	Not Used			
5	Graphics	Graphics Module‡	22	88
4	DMA Controller	Extended Communications Module‡	23	8C
3	Communications/ Printer	MPSC 7201 Serial Controller	24	90
2	Extended Communications	Extended Communications Module‡	25	94
1	Keyboard	Keyboard PUSART 8251A	26	98
0	Interrupt 88	Z80A I/O Decoder	27	9C

*7 = highest, 0 = lowest priority
† Hexadecimal
‡ Option Modules

3.3.1.14 Communications Baud Rate Generator – The communications baud rate generator supplies the transmitter and receiver clocks for the communications channel of the dual-channel MPSC. The baud rate generator is contained in an 18-pin IC package and is driven by a 6 MHz clock that is derived from the 24 MHz master clock oscillator.

The receiver and transmitter clock outputs of the baud rate generator can be independently programmed to allow the communication port to operate at a split baud rate. One of sixteen possible frequencies can be selected for the transmitter or receiver clock. The baud rate generator must be programmed to provide a transmitter and receiver clock that has a frequency that is 16 times the desired baud rate. The 8088 selects the frequencies with an 8-bit data byte (four bits for receiver clock selection and four bits for transmitter clock selection) routed to the baud rate generator via the buffered output data bus.

3.3.1.15 Printer Baud Rate Generator – The printer baud rate generator supplies the transmitter and receiver clock for the printer channel of the dual-channel MPSC. The baud rate generator logic consists of a divide-by-13 counter driven from a 4 MHz signal obtained from the PC100 clock circuit. Then the signal is driven into an 8-bit binary counter. The outputs of the 8-bit binary counter are applied to an eight-to-one decoder. The 8088 selects one of the eight possible frequencies, with the three least significant bits of an 8-bit data byte routed to the eight-to-one decoder via the buffered output data bus.

The transmitter and receiver clocks cannot be independently programmed for the printer channel. The selected output of the eight-to-one decoder will have a frequency 16 times the desired printer baud rate.

The printer baud rate generator also supplies a fixed receiver/transmitter clock for the keyboard PUSART. This clock is obtained from the 76.8 kHz output of the 8-bit binary counter and allows the keyboard to operate at a fixed 4.8K baud rate.

3.3.1.16 PC100 Clock Circuit – The PC100 clock circuit supplies the basic clock pulses for the 8088 and Z80A processors and their supporting logic as well as the clock pulses needed by peripheral devices.

A 24.0734 MHz crystal oscillator provides the master clock for the system module. The master clock is used by various frequency dividers to produce three groups of clock pulses with the correct frequency and phase relationship to synchronize the processors, peripheral devices, and supporting logic.

The first group of clock pulses is used by the 8088 and its supporting logic. The basic clock for the 8088 is obtained from a frequency divider that divides the master clock frequency by five to produce asymmetrical clock pulses at 4.815 MHz (208 ns period). Other 4.815 MHz outputs from the 5:1 divider are delayed in phase and are used to synchronize the 8088 supporting logic.

The second group of clock pulses is used by the Z80A and its supporting logic. The basic clock for the Z80A is obtained from a frequency divider that divides the master clock frequency by six to produce symmetrical clock pulses at 4.012 MHz (250 ns period). Other outputs from the 6:1 divider are delayed in phase and used to synchronize the Z80A supporting logic.

The third group of clock pulses (8, 4, 2, and 1 MHz; 500 and 250 kHz) generated by the clock circuits is used by the RX50 controller logic and by the system module during diagnostic loopback testing.

The 8, 4, and 2 MHz clock pulses are used by the RX50 controller's write precompensation circuit. The 1 MHz clock pulses are used by the write precompensation circuits and the 1793 formatter/controller. The 500 kHz clock pulses are used by the RX50 controller's data separator circuit to separate the data and clock signals in the raw data stream received from the diskette drive during a read operation. The 250 kHz clock pulses are used by the system module during diagnostic loopback testing.

3.3.1.17 RX50 Controller – The RX50 controller is a 9.906 cm (3.9 in) by 24.130 cm (9.5 in) printed circuit module that contains three connectors and the controller logic circuits. Two of the connectors (J2 and J3) on the module are 34-pin connectors that are used to make the connection via cables to the diskette drive unit(s). The other connector (J1) is a 40-pin connector that plugs into a 40-pin connector (J9) on the system module.

The controller controls up to four diskette drives. It can perform implied seeks, read from, and write to specified sectors and tracks on single-sided diskettes. The controller supports soft-sectored, single-sided, double-density diskettes using a phase-locked loop (PLL) circuit. The controller drive capability and signal definitions conform to the ANSI standard for minidiskette drives.

The Z80A transfers binary command, status, and 8-bit data between the controller and disk drives by accessing registers in the controller module. When writing to the diskette, the controller converts the binary data from the Z80A into modified frequency modulation (MFM) data. MFM is a magnetic recording method for disk drives in which a clock signal is encoded in the flux transitions recorded on the magnetic surface of the diskette.

When the Z80A reads the serial MFM data from the diskette, the RX50 controller synchronizes on the data transitions and, with the PLL circuit and MFM decoder, separates the clock from the data information. The data is then converted to 8-bit parallel binary data for transfer to the Z80A data bus.

3.3.2 RX50 Diskette Drive Unit

The RX50 is a dual-diskette drive that mounts in the system unit. (A second optional dual-diskette drive can also be installed in the system unit). The diskette drive is connected to the RX50 controller and power supply with a signal cable and a power cable. The signal cable transfers command, status, and data between the diskette drive and the RX50 controller module. The power cable carries the +5 and +12 Vdc power required by the diskette drive.

Each RX50 dual-diskette drive is capable of read/writing on a single surface of two diskettes. The diskettes are inserted into two access slots located on the front of the diskette drive unit. Each diskette provides 409,600 8-bit bytes (formatted) for a total of 819,200 bytes of storage.

The RX50 diskette drive performs read, write, and seek operations to store (write) and retrieve (read) programs/data on the diskette. To perform these operations, the diskette drive has the following electronic and electromechanical components:

Printed Circuit Boards

- Seek and interface modules
- Motor control module
- Read/write module

Electromechanical Components

- Spindle motor
- Stepper motor
- Two head load solenoids
- Two read/write heads
- Diskette sensors

The electronic components contain the diskette drive logic circuits. The electromechanical components all plug into the printed circuit boards.

3.3.3 Power Supply

The H7842-A power supply is a 138 W, switching type, ac/dc regulated voltage converter circuit. It converts the ac input (either 115 or 240 Vac) to +5, +12, and −12 Vdc and supplies this dc power to the system module, the diskette drive unit(s), the monitor, the keyboard, and any installed options.

The power supply is mounted at the rear of the system unit and secured to the system unit mounting plate by a locking device.

The power supply contains six connectors. Three of the connectors are used for the ac input/output connections and the remaining three connectors are used for dc power connections to the system module and diskette drive unit(s). A 13-pin flat cable is used to carry the dc power from the power supply to the power connector (J8) on the system module. Two 4-pin connectors and cables permanently attached to the power supply provide the dc power for each diskette drive.

The single phase, 3-wire, ac input power connection is made to a 3-pin connector located on the rear panel of the power supply. The ac power is then routed internally to two additional 3-pin connectors located on one end of the power supply. One of these connectors is used to route the ac power to the fan assembly and the other connector routes the ac power to and from the on/off power switch located on the front of the system unit.

The power supply includes two types of control circuits: regulation and protection. The regulation circuits maintain the output voltages at the proper level. The protection circuits prevent internal damage to the power supply and to the system components due to incorrect voltage and/or current conditions. There are three protection circuits: overvoltage, start-up undervoltage, and overcurrent.

3.4 OPTION MODULES

Optional modules can be added to the Rainbow 100 computer to increase memory size, expand the communications functions, and provide a color/graphics capability. These optional modules are mounted on the system module and plug directly into connectors provided for them. A brief description of the available options is given in the following paragraphs. Additional information for these options can be obtained from the following installation guides:

Title	Document Number
Rainbow™ Memory Extension Option Installation Guide	EK-PCMXE-IN
Rainbow™ 100 Extended Communication Option Installation Guide	EK-PCEXC-IN
Rainbow™ Color/Graphics Option Installation Guide	EK-PCCOL-IN

3.4.1 Memory Extension Option

The memory extension option for the Rainbow 100 computer allows the user to upgrade the system memory with an additional 64K bytes or 192K bytes of dynamic random-access memory (DRAM) that can be written into as well as read. Two versions of the memory extension option are available: a 64K byte option (part number PC1XX-AA) and a 192K byte option (part number PC1XX-AB). The memory option is installed in the J6 connector on the system module. These options added to the existing 64K bytes of DRAM on the system module provide the Rainbow 100 computer with a total system memory of 128K bytes or 256K bytes.

Both versions of the memory extension option use the same printed circuit board etch and the same type of 64K × 1 bit memory chips. The 64K byte version of the option contains nine 64K × 1 bit chips and the 192K byte version contains twenty-seven 64K × 1 bit chips arranged as three 64K byte memory stacks. Eight of the 64K × 1 chips in each stack contain the 8 bits of the data byte and the ninth contains the parity bit. The 64K byte version of the option is not user upgradable.

When installed, this added memory is always available to the 8088 processor and will require wait states only when the memory cycle and refresh cycle contend for use of the memory.

The memory option is equipped with a parity generation and parity error detection circuit to notify the 8088 processor when a parity error occurs. If a parity error occurs, the memory option transmits a parity error signal to the nonmaskable interrupt input of the 8088. The 8088 then vectors to a ROM parity error program in the 24K byte ROM that will display an error message on the screen.

3.4.2 Extended Communications Option

The extended communications option is a major component of the Rainbow 100 computer and is plugged directly into two 40-pin connectors (J4 and J5) on the system module. The module contains a dual-channel multiprotocol serial controller (MPSC) and supporting logic. The purpose of the option is to add a second communications connector with bit and byte synchronous capability to the Rainbow 100. This option also provides a separate high-speed communications connector.

The extended communications option performs the following functions:

1. By means of the 8237 DMA controller, transfers data bidirectionally between memory and the high-speed communications link (MPSC) with minimum processor intervention. The transfer to/from memory uses the shared 64K byte RAM only and not any installed optional memory.

2. Provides two complete serial communications controllers in a single MPSC package to:

   a. Convert parallel data (from the processor) to serial data, as required by various communications protocols.

b. Convert serial data streams of the protocols back to parallel data for the processor.

c. Buffer incoming and outgoing data, allowing the processor time to respond.

d. Insert and delete framing bits and characters.

e. Calculate/check parity and check CRC error.

f. Inform the CPU about what actions need to be taken and when.

g. Interface with other computers over discrete modem control lines.

3. Provides an optional bit/byte synchronous/asynchronous RS-232 connector that is similar to the Rainbow 100 communications connector.

4. Supports bit protocols at a clock rate of 880 kHz by means of the MPSC.

5. Uses an MPSC bus interface controller to provide:

a. Bus control logic (BCL), which determines the internal source or destination of data and control transfers between the MPSC and the processor bus.

b. Interrupt control logic (ICL), which sets priorities for internal input requests and places information on the data bus during an interrupt acknowledge cycle (provided the MPSC vectored interrupt feature has been enabled).

c. DMA control logic (DMACL), which enables the MPSC to transfer data without interrupting the processor. DMACL accepts service requests (if they are prioritized) and, like ICL (above), places information on the data bus at appropriate times. DMACL also accepts information from the data bus. When enabling the MPSC, DMACL activates an internal controller to move data directly from the MPSC to memory or vice versa.

d. Clocks and reset logic (C&RL), which controls timing states in the MPSC and is usually connected to the processor clock.

The extended communications option consists of the following main components mounted on a printed circuit board:

1. A 5 MHz 8237 direct memory access controller (DMAC).

2. A multiprotocol serial controller (MPSC) with the following features:

a. A high-speed, synchronous serial communications connector, EXT COMM A, with external clocks and RS-422 differential drive capability.

b. A general-purpose synchronous/asynchronous serial communications connector, EXT COMM B, with RS-423 drive capability, capable of supporting bisync modes.

The extended communications option is reset by a write to the 8088 I/O port 27H. The write to port 27H is performed by the firmware in the 24K byte ROM when the Rainbow 100 is powered up, and any time the extended communications option issues a DMAC interrupt request.

3.4.3 Graphics Option

The graphics option generates bit-mapped video drive signals for a monochrome or optional color monitor. The graphics module is plugged into a 40-pin connector (J7) on the system module.

The graphics option will emulate the functionality of the VT100, VT102, and VT125 video terminals. The Rainbow 100 computer with the color/graphics option installed can operate in one of two modes: text only or graphics/text. In text only (VT100 text mode), the graphics option video will be deselected. During this time, the video processor (DC11 and DC12) on the system module will be responsible for supplying the video signals to the monitor. During graphics/text mode, the graphics option is selected and will supply the bit-mapped video signals to the monitor.

The graphics option for the Rainbow 100 supports the following features:

- Low resolution mode – 384 × 240 pixels × 4 planes
- High resolution mode – 800 × 240 pixels × 2 planes
- 16 simultaneous colors from a palette of 4096 (in low resolution mode)
- 4 simultaneous colors from a palette of 1024 (in high resolution mode)
- 9600 baud character throughput (hardware only)
- Smooth and jump split-screen scrolling

3.5 SYSTEM INTERFACE CONNECTORS

There are nine connectors on the system module. These connectors provide the interconnection between the system module and the other components and options in the Rainbow 100 system. Some of the components and options are connected to the system module via cable while others are plugged directly into headers on the printed circuit board. Figure 3-4 shows the connectors on the system module and how they connect to the other system components and options.

The system module connectors are listed in Table 3-2 and described in the following paragraphs:

Table 3-2 System Module Connectors

Connector Number	Function	Type
J1	Communications	25-pin male D-subminiature
J2	Printer	25-pin female D-subminiature
J3	Video/keyboard	15-pin male D-subminiature
J4	Extended communications	40-pin (2 × 20) header
J5	Extended communications	40-pin 2 × 20) header
J6	Memory extension option	52-pin (2 × 26) header
J7	Graphics option	40-pin (2 × 20) header
J8	Power	13-pin in-line header
J9	Diskette drive controller	40-pin (2 × 20) header

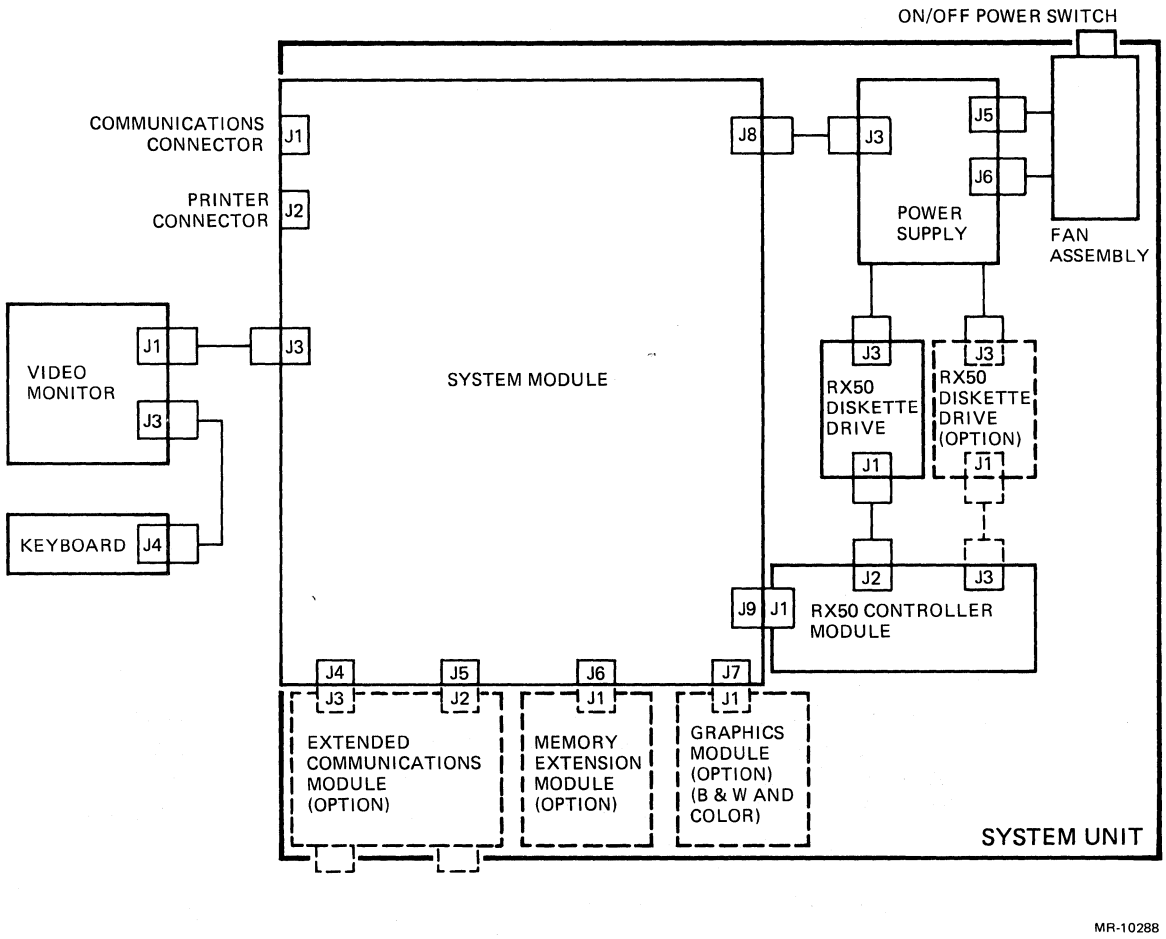


Figure 3-4 System Interface Connectors

3.5.1 Communications Connector (J1) Signals

The communications connector (J1) allows the Rainbow 100 computer to communicate with a host computer over a cable connected directly to the host computer or to a modem or telephone line. The Rainbow 100 computer communicates with the host computer using any one of the following three communications protocols:

- FDXA Full-duplex with no modem control (data leads only)
- FDXB Full-duplex with modem control
- FDXC Asymmetrical full-duplex with modem control

The signals transmitted through the connector are listed in Table 3-3.

Table 3-3 Communications Connector (J1) Signals

Pin Number	Signal	Mnemonic	Direction*
1	Protective Ground	PROT GND	
2	Transmit Data	XMIT DATA	Out
3	Receive Data	REC DATA	In
4	Request to Send	RTS	Out
5	Clear to Send	CTS	In
6	Data Set Ready	DSR	In
7	Signal Ground	GND	
8	Receive Line Signal Detect	RLSD	In
9	Not Used		
10	Not Used		
11	Not Used		
12	Speed Indicator/Secondary Receive Line Signal Detect	SI/SRLSD	In
13	Not Used		
14	Not Used		
15	Send Clock	SEND CLK	In
16	Not Used		
17	Receive Clock	REC CLK	In
18	Not Used		
19	Secondary Request to Send	SRTS	Out
20	Data Terminal Ready	DTR	Out
21	Not Used		
22	Ring Indicator	RI	In
23	Speed Select	SPDSEL	Out
24	Not Used		
25	Not Used		

*Direction of signals with respect to the system module

Communications Signal Functions – The functions of the signals on the communications connector pins are described in Table 3-4.

Table 3-4 Communications Signal Functions

Signal	Function*
Protective Ground	This signal is connected to chassis ground via jumper W17.
Transmitted Data	Signals on this line represent the serially encoded characters that are transmitted from the communications connector. This signal is held in the marking state during intervals between characters and at all times when no data is being transmitted.
Receive Data	Signals on this line represent the serially encoded characters to be received.
Request to Send	Assertion of this signal indicates that the channel is ready for transmission.
Clear to Send	When this signal is asserted, it indicates that the modem is ready for transmission.
Data Set Ready	The ON condition of DSR indicates that the modem is in data mode, and that the control signals asserted by the modem are valid.
Signal Ground	This circuit establishes the common ground reference potential for all interface circuits except protective ground.
Receive Line Signal Detector	Also called Carrier Detect. The modem asserts this signal ON when the received signal is of sufficient quality and magnitude.
Speed Indicator	This signal allows some modems to control channel bit rates.
Secondary Receive Line Signal Detect†	This circuit is used in half-duplex coded control with reverse channel.

* The following terminology is used interchangeably to describe the communications signals:
Negative Voltage = 1 = Mark = OFF
Positive Voltage = 0 = Space = ON

† Secondary Receive Line Signal Detect and Speed Indicator are two different functions performed by the same physical line.

‡ These signals are supported by using a special cable for FDXC modem protocol.

Table 3-4 Communications Signal Functions (Cont)

Signal	Function*
Secondary Clear to Send‡	In FDX, this signal is the same as clear to send. In Asymmetric FDX, it provides the functionality for a secondary channel.
Secondary Transmitted Data‡	In FDX, this signal is the same as Transmitted Data, but when operating in Asymmetric FDX, it provides functionality for the secondary channel.
Send Clock	This is an external transmit clock that is supplied by the modem. It substitutes for the communications transmit clock when the synchronous select bit is set.
Receive Clock	This is an external receive clock that is supplied by the modem. It substitutes for the communication receive clock when the synchronous select bit is set.
Secondary Request to Send‡	This signal is used for HDX restraint mode and Asymmetric FDX Secondary Request to Send.
Data Terminal Ready	This signal is turned ON whenever the channel is ready for transmission.
Ring Indicator	The ON condition indicates that a ringing signal is being received from the communications line.
Speed Select	This signal allows the 8088 processor to control the modulation method of the modem to coincide with its selected bit rate.

* The following terminology is used interchangeably to describe the communications signals:
Negative Voltage = 1 = Mark = OFF
Positive Voltage = 0 = Space = ON

† Secondary Receive Line Signal Detect and Speed Indicator are two different functions performed by the same physical line.

‡ These signals are supported by using a special cable for FDXC modem protocol.

3.5.2 Printer Connector (J2) Signals

The printer connector signals meet the following standards:

- Electronic Industry Association (EIA) standard RS-423 and RS-232-C
- International Telegraph and Telephone Consultative Committee (CCITT) recommendation V.28

The printer connector signals and their pin assignments are listed in Table 3-5.

Table 3-5 Printer Connector (J2) Signals

Pin* Number	Signal	Mnemonic	CCITT/EIA	Description
1	Protective Ground	PROT GND	101/AA	Chassis ground; ac power cord ground. This signal is connected to chassis ground via jumper W16.
2	Transmitted Data (input)	TXD	103/BA	XON/XOFF control signals and other characters from the printer.
3	Received Data (output)	RXD	104/BB	Data received by the printer from the Rainbow 100 computer. This signal is asserted high (mark state) when not in use.
5	Clear to Send (output)	CTS	106/CB	Always asserted high (mark state).
6	Data Set Ready (output)	DSR	107/CC	Always asserted high.
7	Signal Ground	SGND	102/AB	Common ground for all signals.
20	Data Terminal Ready (input)	DTR	108.2/CD	This signal from the printer indicates its status.

*Pins not listed are not used by the printer connector.

3.5.3 Keyboard/Monitor Connector (J3) Signals

This connector carries the video signals, data signals, and power used by the keyboard and monitor. The connector signals meet the following standards:

- Video signals – Similar to EIA RS-170

NOTE

The composite video (Mono Video) signal on pin 12 is dc coupled and therefore not in strict agreement with RS-170. To agree with RS-170, the composite video signal would require a 10 microfarad capacitor in series with the output.

- Keyboard data signals – EIA RS-423

The keyboard/monitor signals and their pin assignments are listed in Table 3-6.

Table 3-6 Keyboard/Monitor Connector (J3) Signals

Pin	Signal	Mnemonic	Description
1	Red shield ground		Shield ground for color monitor cable
2	Green shield ground		Shield ground for color monitor cable
3	Blue shield ground		Shield ground for color monitor cable
4	Mono shield ground		Shield ground for composite video coaxial cable
5,6	Ground		Video, data, and power ground
7,8	+12 V		+12 V power to monitor and keyboard
9	Blue video		Color video signal from graphics option
10	Green video		Color video signal from graphics option
11	Red video		Color video signal from graphics option
12	Mono video		Composite B/W video from the video processor on the system module
13	Not used		
14	Keyboard received data (output)	KBD RXD	Serial data transmitted to keyboard
15	Keyboard transmitted data (input)	KBD TXD	Serial data received from keyboard

3.5.4 Extended Communications Connectors (J4 and J5)

The extended communications option plugs into two 40-pin headers on the system module. The extended communications signals and their pin assignments are listed in Tables 3-7 and 3-8.

Table 3-7 Extended Communications Connector (J4) Signals

Pin*	Signal	Mnemonic	Description
1	Initialize	INITL	Initializes extended communications option on power-up.
2	−12 V		-12 V output
3,6,18,20, 22,24,26,28	Ground	GND	
4,8	+12		+12 V output
5	Direct Memory Access Control Interrupt	DMAC INTL	This signal allows the option to make a data transfer without interrupting the processor.
7	Communications Select 1	COM SEL 1L	This output signal selects one of the two receiver/transmitter channels in the MPSC.
8	+12 V		+12 V output
9	Communications Request	COM REQ L	This input signal informs the shared memory arbitrator that the option requests use of the shared memory.
12,14,16	+5 V		+5 V output
23	Communications Interrupt	COM INTR L	This input signal is the interrupt request to the 8088 processor.
25	Communications Acknowledge	COM ACK L	This signal informs the option that its interrupt request is acknowledged.
27	2.5 MHz		Clock signal for the MPSC
29	Clock Pulses	05A	
31	Clock Pulses	05C L	

*Pins not listed are not used by the extended communications option.

Table 3-7 Extended Communications Connector (J4) Signals (Cont)

Pin*	Signal	Mnemonic	Description
33	Communications Write	BWR88 H	This output signal indicates that the 8088 is performing a write cycle.
35	Communications Read	BRD88 H	This output signal indicates that the 8088 is performing a read cycle.
37	Clock Pulses	05 C	
40		eL	This is a signal from the shared memory arbitration logic to indicate that an unshared memory cycle is in progress.

*Pins not listed are not used by the extended communications option.

Table 3-8 Extended Communications Connector (J5) Signals

Pin*	Signal	Mnemonic	Description
1	Address/Data Bit	BAD 0	Buffered address/data bits to/from extended communications option
3		BAD 1	
5		BAD 2	
7		BAD 3	
9		BAD 4	
11		BAD 5	
13		BAD 6	
15		BAD 7	
17	Address	88 A0	Latched address bits to extended communications option
19		88 A1	
21		88 A2	
23		88 A3	
25	Communications Select 2	COM SEL 2 L	This signal selects one of two receiver/transmitter channels in the MPSC
27,29,31	+5 V	+5 V	+5 V output
33,35,37	Ground	GND	

*Pins 39 and 40 are not used.

Table 3-8 Extended Communications Connector (J5) Signals (Cont)

Pin*	Signal	Mnemonic	Description
2	Shared Memory Data Bit	SHRAM D0	Shared memory data bits to/from extended communications option
4		SHRAM D1	
6		SHRAM D2	
8		SHRAM D3	
10		SHRAM D4	
12		SHRAM D5	
14		SHRAM D6	
16		SHRAM D7	
18	Shared Memory Address Bit	SHMA 0	Shared memory address bits from extended communications option
20		SHMA 1	
22		SHMA 2	
24		SHMA 3	
26		SHMA 4	
28		SHMA 5	
30		SHMA 6	
32		SHMA 7	
34	Shared Memory Row Address Strobe	SCHRAM RAS L	Row address strobe from extended communications option
36	Shared Memory Column	SCHRAM CAS L	Column address strobe from extended communications option
38		COM SH WR L	Read/write signal from extended communications option

*Pins 39 and 40 are not used.

3.5.5 Memory Extension Connector (J6) Signals

The memory extension option plugs into a 52-pin header on the system module. This connector carries all the address, data, and control signals required to operate the memory extension option. The signals and their pin assignments are listed in Table 3-9.

Table 3-9 Memory Extension Connector (J6) Signals

Pin*	Signal	Mnemonic	Description
1,2,3,51,52	Ground	GND	
4	Row Address Strobe	RAS88 H	This output signal strobes the row address into the extended memory.
6	Address Bit 6	A6	Memory extension address bits
8	Address Bit 1	A1	
9	Address Bit 13	A13	
10	Address Bit 8	A8	
11	Address Bit 3	A3	
12	Address Bit 10	A10	
13	Address Bit 0	A0	
14	Address Bit 14	A14	
15	Address Bit 7	A7	
16	Address Bit 2	A2	
17	Address Bit 5	A5	
18	Address Bit 9	A9	
19	Address Bit 12	A12	
20	8088 Multiplexer Select	MUX 88 H	This signal allows Address bits <15:10> from the 8088 processor to be applied to the extended memory.
21	Address Bit 11	A11	Memory extension address bit
22	Address Bit 4	A4	
23	Refresh Row Address Strobe	RFSH RAS H	This output signal refreshes the extended memory.
24	Parity Test	PARITY TEST H	This output signal enables testing of the parity circuits on the extended memory.
25,27,28,35	+5 V		+5 V output
26	Parity Error	PARITY ERROR L	This input signal informs the 8088 that a memory parity error has occurred.
29	Memory Present	MEM PRES L	This input signal informs the 8088 that the memory extension is installed.
30		e L	The output signal is asserted by the shared memory arbitration logic when an unshared memory cycle is in progress.

*Pins not listed are not used by the memory extension option.

Table 3-9 Memory Extension Connector (J6) Signals (Cont)

Pin*	Signal	Mnemonic	Description
31	Do Refresh	DO RFSH L	This output signal indicates that the extended memory must be refreshed.
32	Select Memory Bank 2	S64K 2 L	This output signal selects the second 64K byte memory bank.
33	Refresh Done	RFSH DONE H	This output signal indicates that memory refresh operation is completed.
34	Initialize	INIT L	This output signal initializes the memory extension logic on power-up.
36	Buffered Address Data	BAD 7	Memory extension data bit 7
37	Column Address Strobe	CAS88 H	This output signal strobes the column address into the extended memory.
38	Buffered Address Data	BAD 6	Memory extension data bit 6
39	Data Transmit/Receive	DT/R	This output signal controls the direction of data to/from the memory extension.
40	Buffered Address Data	BAD 5	Memory extension data bit 5
41	Memory Read	BRD88 H	This output signal indicates that the 8088 is performing a read cycle.
42	Buffered Address Data	BAD 4	Memory extension data bit 4
43	Select Memory Bank 3	S64K 3 L	This output signal selects the third 64K byte memory bank.
44	Buffered Address Data	BAD 3	Memory extension data bit 3
45	Memory Write	BWR88 L	This output indicates that the 8088 is performing a write cycle.
46	Buffered Address Data	BAD 2	Memory extension data bit 2
47	Select Memory Bank 1	S64K 1 L	This output signal selects the first 64K memory bank.
48	Buffered Address Data	BAD 1	Memory extension data bit 1
49	Ground	GND	
50	Buffered Address Data	BAD 0	Memory extension data bit 0

*Pins not listed are not used by the memory extension option.

3.5.6 Graphics Connector (J7) Signals

The graphics option plugs into a 40-pin header on the system module. This connector carries all the address, data, monographics video, direct-drive color monitor signals, and power required for operation of this option. The signals and their pin assignments are listed in Table 3-10.

Table 3-10 Graphics Connector (J7) Signals

Pin*	Signal	Mnemonic	Description
1	Address Bit 3	A3	This output signal is used for graphics display control.
2	Initialize	INIT L	This output signal initializes the graphics option on power-up.
3	Buffered Address Data	BAD 0	Graphics option data bit 0.
4	Graphics Select	GRAPHIC SEL L	This output signal selects the graphics option.
5	Buffered Address Data	BAD 1	Graphics option data bit 1.
6	Graphics Read	BRD88 H	This output signal indicates that the 8088 is performing a read cycle.
7	Buffered Address Data	BAD 2	Graphics option data bit 2.
8	Graphics Write	BWR88 H	This output signal indicates that the 8088 is performing a write cycle.
9	Buffered Address Data	BAD 3	Graphics option data bit 3.
10,14,16	+5 V		+5 V output.
11	Buffered Address Data	BAD 4	Graphics option data bit 4.
13	Buffered Address Data	BAD 5	Graphics option data bit 5.
15	Buffered Address Data	BAD 6	Graphics option data bit 6.
17	Buffered Address Data	BAD 7	Graphics option data bit 7.
18	Ground	GND	

*Pins not listed are not used by the graphics option.

Table 3-10 Graphics Connector (J7) Signals (Cont)

Pin*	Signal	Mnemonic	Description
19	Address Bit 0	A0	This output signal is used for graphics display control.
20,22,24, 26,28	Ground	GND	
21	Address Bit 1	A1	This output signal is used for graphics display control.
23	Address Bit 2	A2	This output signal is used for graphics display control.
25	Red Drive	RED	This input signal is routed to the Keyboard/Monitor connector (J3) to directly drive the red gun of a color monitor.
27	Green Drive	GREEN	This input signal is routed to the Keyboard/Monitor connector (J3) to directly drive the green gun of a color monitor.
29	Blue Drive	BLUE	This input signal is routed to the Keyboard/Monitor connector (J3) to directly drive the blue gun of a color monitor.
30,32	+12 V		+12 V output
31	Graphics Video 1	GRF VID 1 H	This signal is the first bit-mapped graphics video input.
33	Graphics Video 2	GRF VID 2 H	This signal is the second bit-mapped graphics video input.
35	Graphics Blanking	GRF BLANK L	This input signal is used to blank out the graphics display during the CRT beam retrace interval.
37	Graphics Sync	GRF SYNC L	This input signal is used as the synchronizing signal for the graphics video.
38	Graphics Interrupt	GRF INTR L	This input signal is asserted by the graphics option when it wishes to display video.
39	Graphics Option Present	GRAPHICS PRES L	This input signal informs the 8088 that the graphics option is installed.
40	Vertical Blanking	VERT BLANK L	This input is the vertical blanking signal for the graphics video.

*Pins not listed are not used by the graphics option.

3.5.7 Power Supply Connector (J8) Signals

The power supply connector on the system module is a 13-pin in-line connector. A 13-pin flat cable, detachable at both ends, is used to connect the system module to the power supply. The power supply dc voltages and control signals that are applied to this connector are listed in Table 3-11.

Table 3-11 Power Supply Connector (J8) Signals

Pin	Signal	Mnemonic	Description
1	AC Voltage Okay	ACOK H	This signal indicates the presence or absence of valid ac power entering the power supply. When valid ac power is present, this signal will be high. When the ac power is lower than the required minimum input voltage, this signal will be low.
2	Voltage Bias	VBIAS	This signal is connected to the communications control register via a jumper on the system module. The jumper is installed only for manufacturing testing.
3	None		This pin is missing to provide a key for the cable connector.
4	−12 V		−12 V input
5, 6	+12 V		+12 V input
7, 8, 9	+5 V		+5 V input
10, 11, 12, 13	Ground	GND	DC power return and signal ground

3.5.8 RX50 Controller Connector (J9) Signals

The RX50 controller connector is a 40-pin header that provides the interface between the Z80A processor and the RX50 controller module. This connector carries all the address, read/write data, control signals, and dc power needed for operation of the module. The signals and their pin assignments are listed in Table 3-12.

Table 3-12 RX50 Controller Connector (J9) Signals

Pin*	Signal	Mnemonic	Description
1	Diskette Drive Read	ZFPRD L	This output signal asserted by the Z80A I/O select logic allows the RX50 controller to place read data from the diskette drive onto the Z80A data bus (ZD<7:0>).
2	Printer Transmitted Data	PRT TXD	This output signal is a serial stream of data from the printer PUSART. This data is sent to the data separator circuit when DIAG LOOPBACK H is asserted and allows the 8088 and Z80A processors to test the data separator circuits without the use of a diskette drive.
3	Diskette Drive Write	ZFPWR L	This output signal asserted by the Z80A I/O select logic gates data from the Z80A data bus (ZD<7:0>) into the RX50 controller.
4	Diagnostic Loopback	DIAG LOOPBACK H	This output signal, together with PRT TXD, allows the data separator circuit to be tested through the printer port.
5	Z80A Reset	ZRESET L	This output signal will reset the RX50 controller at power-up.
7	AC Voltage Okay	BACOK H	This output signal allows the RX50 controller to transfer write data to the disk drive only when the ac input to the power supply is at the correct voltage level.
9	Diskette Drive Register Read	ZFPREG RD L	This output signal asserted by the Z80A I/O select logic allows the Z80A to read the status of the diskette drive.
10,30	+5 V		+5 V output
11	Z80A Data Bit 7	ZD 7	This bidirectional data bus bit is used to transfer data, control, and status information between the Z80A and the RX50 controller.

*Pins not listed are not used by the RX50 Controller Module.

Table 3-12 RX50 Controller Connector (J9) Signals (Cont)

Pin*	Signal	Mnemonic	Description
12	Z80A Address Bit 0	ZA0	Address bit 0 together with address bit 1 selects 1 of 5 registers in the RX50 controller to transmit/receive data on the ZD<7:0> bus.
13	Z80A Data bit 6	ZD6	This bidirectional data bus bit is used to transfer data, control, and status information between the Z80A and the RX50 controller.
14,24	Ground	GND	Signal and power ground
15	Z80A Data Bit 5	ZD5	
17	Z80A Data Bit 4	ZD4	
19	Z80A Data Bit 3	ZD3	These bidirectional data bus bits are used to transfer data, control, and status information between the Z80A and the RX50 controller.
21	Z80A Data Bit 2	ZD2	
23	Z80A Data Bit 1	ZD1	
25	Z80A Data Bit 0	ZD0	
26	Z80A Address Bit 1	ZA1	Address bit 1 together with address bit 0 selects 1 of 5 registers in the RX50 controller to transmit/receive data on the ZD<7:0> bus.
27	8 MHz Clock Pulse	08 A	This clock pulse signal is used by the write precompensation circuit in the RX50 controller.
29	4 MHz Clock Pulse	4 MHZ	
31	2 MHz Clock Pulse	2 MHZ	This clock pulse signal is used by the write precompensation circuit in the RX50 controller.
32,34	+12 V		+12 V Output
33	1 MHz Clock Pulse	1 MHZ	This clock pulse signal is used by the write precompensation circuit in the RX50 controller.

*Pins not listed are not used by the RX50 Controller Module.

Table 3-12 RX50 Controller Connector (J9) Signals (Cont)

Pin*	Signal	Mnemonic	Description
35	500 kHz Clock Pulse	500 KHZ	This clock pulse signal is used by the data separator circuit in the RX50 controller.
36	−12 V		−12 V Output
37		ZFPREG WR L	This output signal asserted by the Z80A I/O select logic enables a write only control register in the RX50 controller. The contents of the register are used to select the drive, turn on the drive motor, write the precompensation values, and select the surface of the diskette to be accessed.
38	Diskette Drive Present	FLPY PRES L	This input signal informs the 8088 that the RX50 controller is installed.
39	Diagnostic Read	ZDIAG RD L	This output signal asserted by the Z80A I/O select logic enables the general/status register on the RX50 controller to place diskette drive status information on the ZD<7:0> data bus.

*Pins not listed are not used by the RX50 Controller Module.

3.6 FIRMWARE INTRODUCTION

The firmware for the Rainbow 100 computer is contained in a 24K byte ROM consisting of three 8K × 8 bit chips. The firmware provides the following services:

- Power-up initialization of hardware
- Selftest diagnostics
- Terminal and console modes
- Image of Z80A RAM space to be loaded
- Boot loader to read track 0, sector 1 of diskette
- Opening menu selection process
- Automatic shut-off of monitor display after 30 minutes of nonuse, and restoration of display on first activity (any keyboard or received character).

3.6.1 Terminal Mode

When in the terminal mode, the Rainbow 100 computer runs a firmware program using the 8088 processor and looks similar to a VT102 terminal. It provides subfunctions in modules usable to other programs. These other programs need to be able to execute similar functions. The Rainbow 100 computer processes incoming character strings in the same manner as a VT102 terminal. The Rainbow 100 computer also returns characters to the host computer in a manner similar to that of the VT102 terminal given the same Set-Up conditions.

The firmware is organized such that the VT102 emulation primitives form the console functionality for use by applications through the interface layer. When in terminal mode, a background loop is entered that calls on the console primitives and adds the necessary functionality to provide full terminal mode.

An interface layer is placed over the console primitives to provide an application with means of accessing those primitives.

NOTE

In console mode there is no support provided for the printer or the communications connectors. This hardware (communications/printer MPSC) must be controlled directly by the operating system.

For those applications that need more immediate control of the hardware, the firmware provides services to obtain raw key information, enable/disable the cursor, and transfer data directly to the screen RAM.

The interface between the application and the firmware is implemented using a software interrupt, with arguments passed and returned in the 8088 registers.

This leads to a layered firmware structure as shown in Figure 3-5. From the firmware viewpoint, the operating system in this example is an application. It can be anything, including another firmware routine.

All entries to firmware routines from external processes are via a software interrupt vector 40H. This makes the interface release-independent because ROM code loads the proper vectors during initialization.

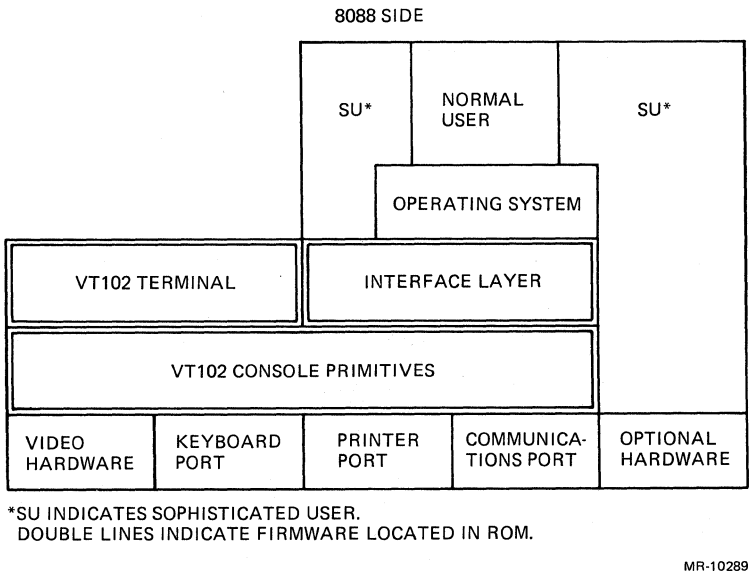


Figure 3-5 Firmware Organization

3.6.2 ROM Selftest Diagnostics

The Rainbow 100 ROM diagnostics tests the basic operational system hardware to determine if the Rainbow 100 computer can load a diskette and run as a terminal. The Rainbow 100 ROM diagnostic is started by four different means:

- Power-Up
- Reset
- Typing **S** on the keyboard in response to the Main System Menu
- Detection of a massive hardware failure (MHFU)

If an error is detected while a Rainbow 100 diagnostic is running, two types of error messages can be displayed: a message on the screen; and a 7-bit numeric value, displayed by seven lights on the back of the system unit.

If an error is fatal, a message will be displayed on the screen, the keyboard lights will blink, the keyboard bell will sound three times, and the lights on the back of the system unit will light in a specific pattern. If the error is nonfatal, the message will be displayed in blinking reverse video, the keyboard bell sounds twice, and no lights are lit on the back of the system unit. If no errors are detected, the keyboard bell will sound once and the Main System Menu will be displayed on the screen.

CHAPTER 4
SYSTEM MODULE TECHNICAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides a technical description of the Rainbow 100 system module for repair or maintenance personnel. The system module is described both to the block diagram level and the functional block diagram level. The logic circuits are generally not described to the detailed circuit level except in those cases where such description is considered necessary for a clear understanding of the subject matter.

4.1.1 Chapter Organization

The information in this chapter is divided into four sections:

- A general description of the functions performed by the system module (Paragraph 4.2)
- A physical description of the system module (Paragraph 4.3)
- A functional description of the system module (Paragraph 4.4)
- A description of the system module connectors (Paragraph 4.5)

4.1.2 Related Documentation

In some of the block diagrams within this chapter, the logic blocks contain the word SHEET followed by a number. This refers to a sheet number of the system module circuit schematics. These numbers may be used while reading this chapter to locate the detailed circuit logic represented by the function logic blocks. The PC100 system module circuit schematics (D-CS-5415486-0-1) consist of 13 sheets and are a part of the PC100 Field Maintenance Print Set (MP-01491-00).

4.2 GENERAL DESCRIPTION

The system module has a dual-processor architecture that uses an 8088 16-bit processor coupled with a Z80A 8-bit processor. Figure 4-1 is a block diagram that shows the relationship between the processors and their supporting logic. The processors operate from and transfer data through a shared block of 62K bytes of RAM to direct, control, and monitor the system's functions. Each processor has, in addition to the shared block of memory, 2K bytes of private RAM and peripheral circuitry.

Each processor supports a portion of the system's function in addition to running 8-bit or 16-bit application/user software. The 8088 processor controls the monitor, keyboard, communications connector, and all options added to the system. The 8088 communicates with its supporting logic and installed options via a 20-bit unidirectional address bus and an 8-bit bidirectional data bus.

The Z80A processor transfers address/data and control signals to the RX50 controller, which uses these signals to read data from and write data to the dual-diskette drives. The Z80A communicates with its supporting logic and the RX50 controller via a 16-bit unidirectional address bus and an 8-bit bidirectional data bus.

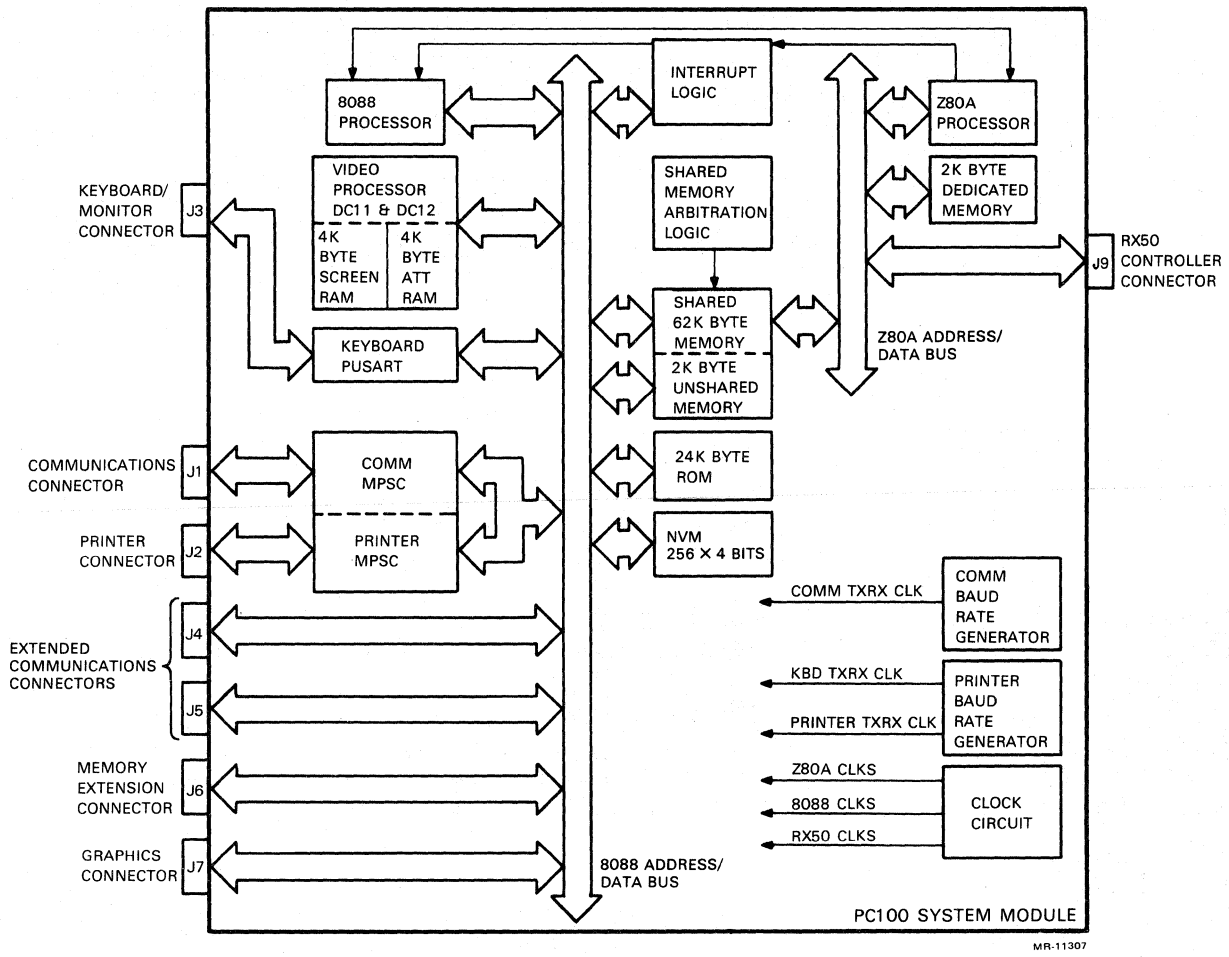


Figure 4-1 System Module Block Diagram

The system module also contains two programmable baud rate generators, one for communications and one for the printer. The communications baud rate generator provides the transmitter and receiver clocks for the communications channel of the multiprotocol serial controller (MPSC). The transmitter and receiver clock baud rate for this channel may be independently programmed.

The printer baud rate generator provides the transmitter and receiver clocks for the printer channel of the multiprotocol serial controller (MPSC) and the keyboard PUSART. The transmitter and receiver clock baud rates for the printer MPSC cannot be independently programmed. The printer baud rate generator also supplies the transmitter and receiver clocks for the keyboard PUSART at a fixed 4.8K baud rate.

The clock circuit on the system module provides three groups of clock pulses that are derived from the master crystal clock oscillator. One group of clock pulses is used by the 8088 and its supporting logic. A second group of clock pulses is used by the Z80A and its supporting logic. The third group of clock pulses is used by the RX50 controller logic.

The system module includes the following features:

- 8088 processor
- Z80A processor
- 64K byte shared dynamic RAM
- 2K byte Z80A dedicated RAM
- 24K byte ROM
- 256 × 4 bit nonvolatile memory (NVM)
- DC011, DC012 video processor
- 4K byte screen RAM
- 4K byte attribute RAM
- Async/bisync communications port
- Printer port
- Keyboard interface
- RX50 controller interface
- Option expansion capability
    - Extended communications
    - Color/graphics
    - Extended memory (64K or 192K bytes)

4.3 PHYSICAL DESCRIPTION

The system module is a modified quad module that is 35.56 cm (14 in) long, 26.42 cm (10.4 in) wide, and 2.25 cm (0.9 in) high. The height of the module is the combined thickness of the printed circuit board and printed circuit board connectors. A metal and plastic back panel attached to the rear of the printed circuit board contains three rectangular holes for the module connection to external devices and eight round holes for viewing the diagnostic lights. The back panel also contains four thumbscrews that are used to secure the system module to the system unit.

The system module contains nine connectors of three different types. Type 1: Three D-type connectors mounted on the rear edge of the system board provide the external connections to the communications device, printer, and keyboard/monitor. Type 2: The input dc power connector is a 13-pin in-line connector with one of the pins removed to provide a locating key. Type 3: The remaining five connectors are dual-row headers and are used to directly connect the system module to the RX50 controller module, the memory extension option, the extended communications option, and the color/graphics option. The RX50 controller module and option modules are secured by plastic standoffs located at appropriate places on the system module. Figure 4-2 shows the locations of the connectors, the main logic elements, the diagnostic lights, and the manufacturing test/configuration jumpers.

4.4 SYSTEM MODULE FUNCTIONAL DESCRIPTION

This section provides a description of the functions performed by the 8088 and Z80A processors and their support circuits. It describes the system logic used for making decisions. If you need detailed information on the 8088 or Z80A processors that is not provided in this manual, you can find it in the following manuals:

iAPX 88 Book
Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051

Z80™-CPU/Z80A™-CPU Technical Manual
Zilog, Inc.
1315 Dell Avenue
Campbell, California 95008

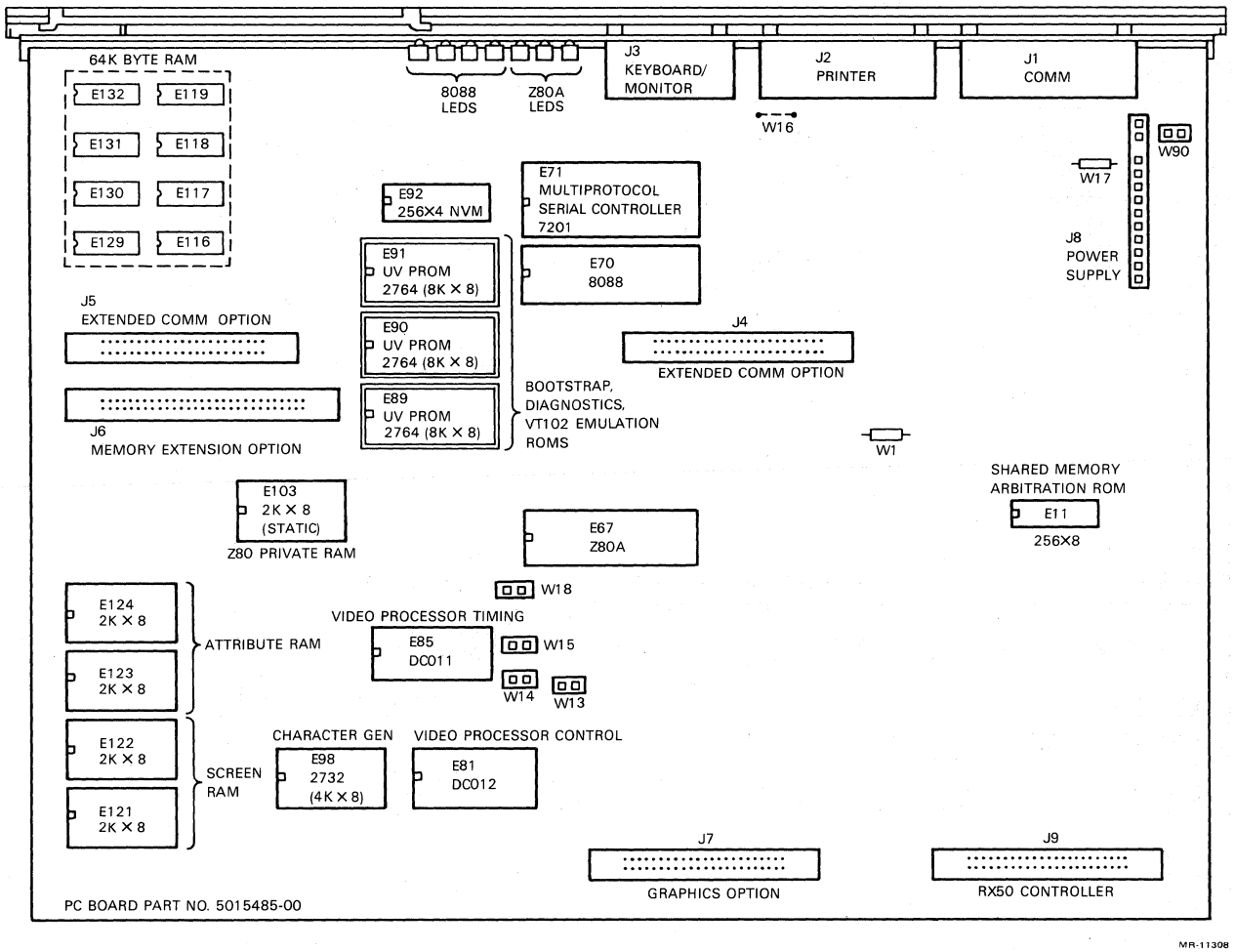


Figure 4-2 System Module Physical Layout

All illustrations in this section are functional block diagrams. Logic symbols appearing on the block diagrams indicate function and may not represent actual circuitry.

4.4.1 System Module Address and Data Buses

The system module has two primary address and data buses, one for each of the 8088 and Z80A processors over which they operate and transfer data to/from their supporting logic, I/O devices, and the shared memory. The system module also contains a number of secondary address and data buses. These secondary buses transfer data between the primary address and data buses and the video processor or shared memory logic. Figure 4-3 shows the primary and secondary address and data buses and their relation to the main logic elements on the system module.

4.4.1.1 8088 Address and Data Buses – The 8088 address A<19:0> and data BAD<7:0> buses support the monitor, keyboard, communications connector, options, the video processor, the shared memory logic, and the 8088 control logic. The address bus is a 20-bit unidirectional bus obtained by latching and combining the AD<7:0> and A<19:8> bits from the 8088. The address and data bus AD<7:0> connecting the 8088 with the address latch, output data buffer, 24K byte ROM, and the data bus transceiver is bidirectional for data transfers and unidirectional for address cycles.

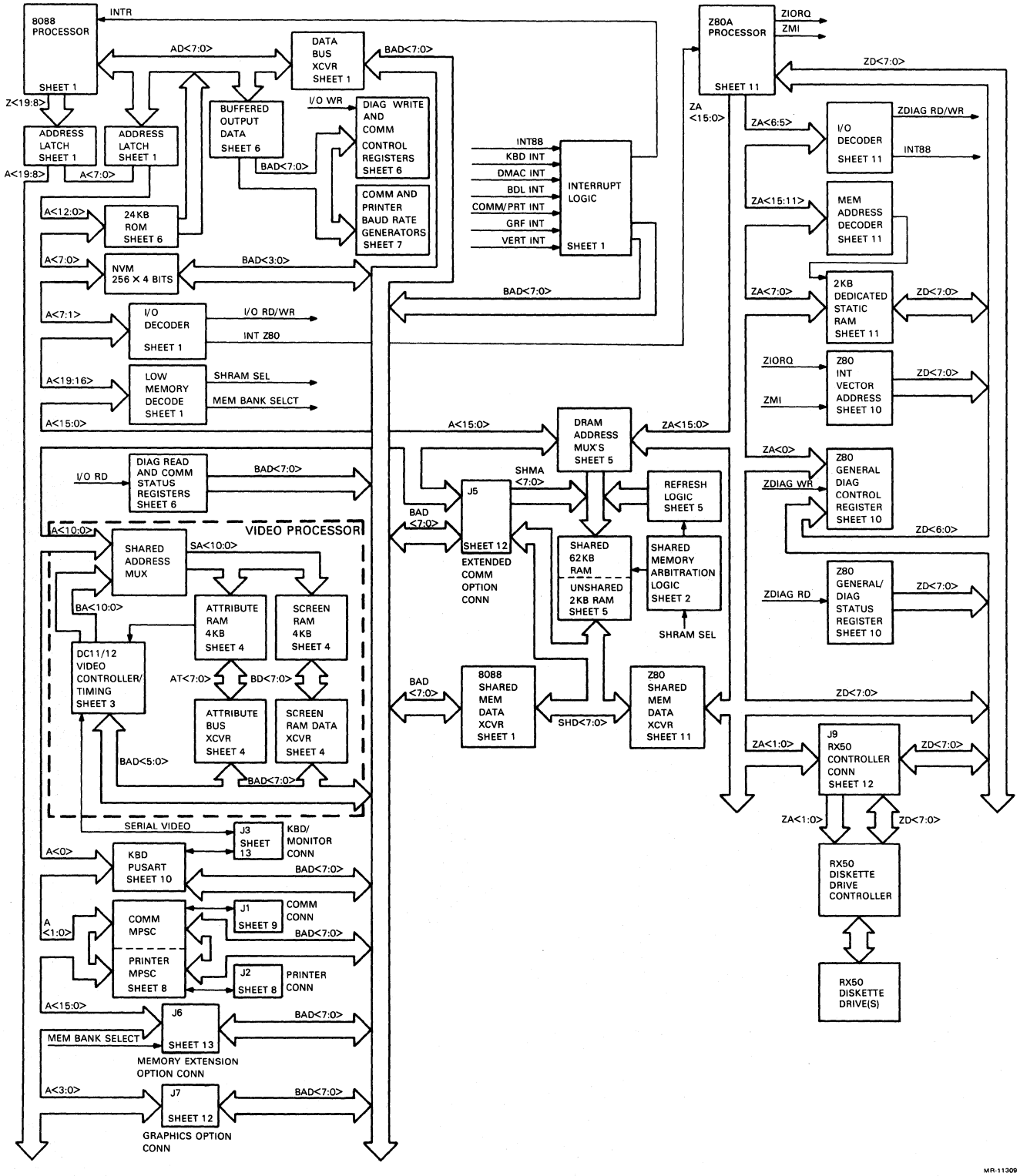


Figure 4-3 System Module Address and Data Buses

4.4.1.2 Z80A Address and Data Buses – The Z80A processor address ZA<15:0> and data ZD<7:0> buses support the RX50 controller and the Z80A control logic. The address bus is a 16-bit unidirectional bus which accesses the 64K byte memory through a DRAM address multiplexer. The data bus ZD<7:0> is an 8-bit bidirectional bus which transfers data to/from the 62K byte shared memory through the Z80A shared memory data transceiver.

4.4.1.3 Buffered Output Data Bus – The buffered output data bus BOD<7:0> is a unidirectional bus obtained by buffering the address and data AD<7:0> bits from the 8088 processor. The BOD bus supplies the bits to the communications control register, the diagnostic write register, the communications baud rate generator, and the printer baud rate generator.

The 8088 uses this bus to write modem control and diagnostic error information into the communications register, diagnostic control information into the diagnostic register, and programming information for the baud rate generators.

4.4.1.4 Video Processor Shared Address Bus – The shared address bus SA<10:0> is a unidirectional bus used to access the 4K byte screen RAM and the 4K byte attribute RAM in the video processor subsystem. The SA<10:0> bits are obtained by multiplexing the 8088 processor address A<10:0> and the buffered address BA<10:0> bits from the video processor.

The 8088 uses the bus to access the screen and attribute RAMs to store the character and attribute information to be displayed on the monitor.

The video processor uses this bus to retrieve the stored character and attribute information by direct memory accesses to the screen and attribute RAMs.

4.4.1.5 Video Processor Buffered Address Bus – The buffered address bus BA<10:0> is used by the video processor to access the screen and attribute RAMs to retrieve character and attribute information to be displayed on the monitor.

4.4.1.6 Video Processor Attribute Bus – The attribute bus AT<7:0> is a bidirectional data bus that carries character, line, and screen information. Only the four least significant bits are used by the video processor.

The AT bus is used by the 8088 processor to store attribute information in the attribute RAM. The default attribute information is obtained from the nonvolatile memory (NVM) via the BAD<7:0> bus and attribute RAM data transceiver.

The video processor uses the AT bus to retrieve the four least significant bits from the attribute RAM and then uses these bits to specify the attributes of the character, line, and screen display.

4.4.1.7 Video Processor Buffered Data Bus – The buffered data bus BD<7:0> is a bidirectional data bus used by the 8088 processor and the video processor. The 8088 uses this bus to store an ASCII coded representation of the character to be displayed in the screen RAM. The character to be stored is obtained from the 8088 via the BAD<7:0> bus and screen RAM data transceiver.

The video processor uses this bus to retrieve the stored ASCII encoded character by direct memory accesses to the screen RAM, and then converts the data into an electrical signal that the monitor can display as letters, numbers, and symbols.

4.4.1.8 Shared Memory Address Bus – The shared memory address bus SHMA<7:0> is an 8-bit unidirectional bus that is used by the 8088 and Z80A processors, the extended communications option, and the refresh logic to access the 64K byte RAM. The 8088 address A<15:0> and Z80A address ZA<15:0> bits are transferred to the shared memory address bus through two DRAM address multiplexers that are controlled by the shared memory arbitration logic. The shared memory arbitration logic continuously monitors and establishes the priority for the devices using the SHMA<7:0> bus.

4.4.1.9 Shared Data Bus – The shared data bus SHD<7:0> is a bidirectional bus used by the 8088 and Z80A processors and the extended communications option to transfer data to and from the 64K byte shared memory. The 8088 data BAD<7:0> and Z80A data ZD<7:0> bits are connected to their respective shared memory data transceivers. The direction and gating of the data bits through the 8088 and Z80A transceivers is determined by control signals from the 8088 and the Z80A. The shared memory arbitration logic continuously monitors the devices and establishes priority using the SHD<7:0> bus.

4.4.2 Clock Circuit

The clock circuit logic generates three groups of clock pulses that determine the basic timing for the Rainbow 100 computer. The clock circuit block diagram is shown in Figure 4-4.

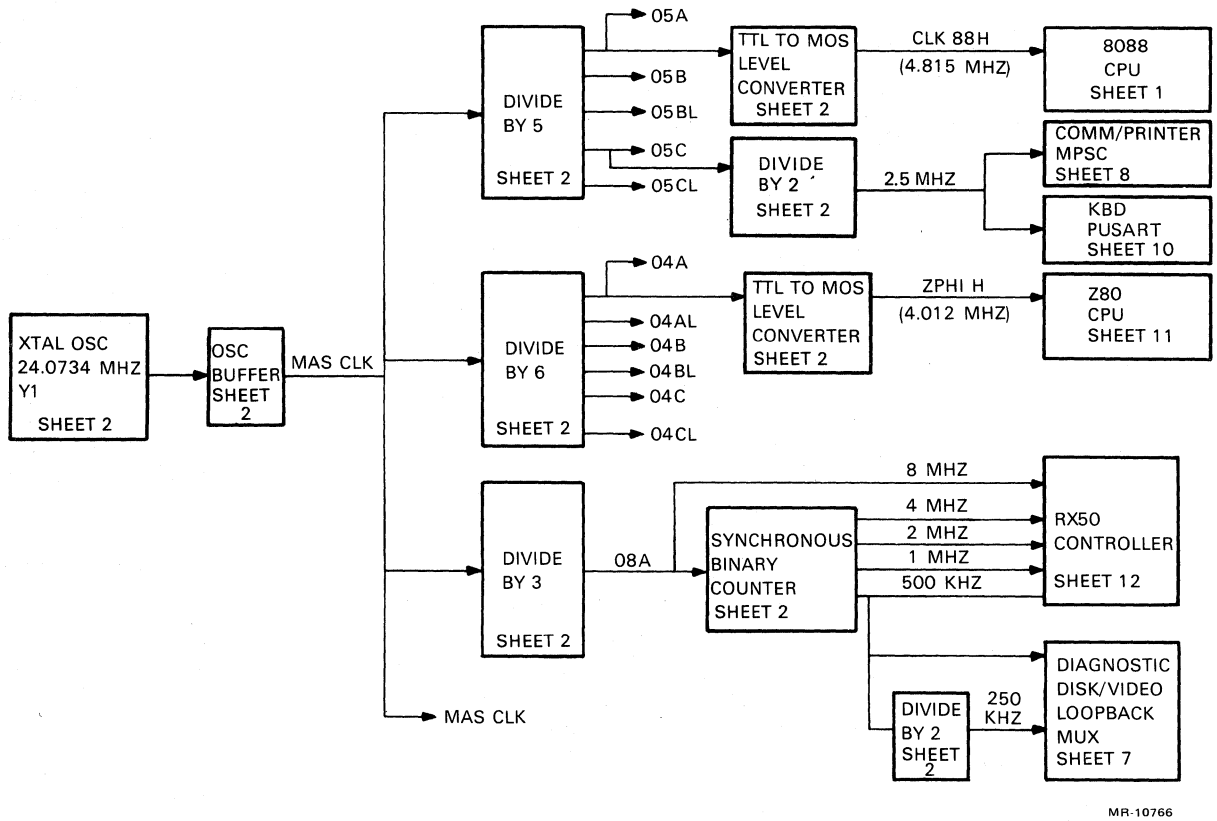


Figure 4-4 Clock Circuit Block Diagram

4.4.2.1 Master Clock – The master clock is a crystal controlled oscillator that runs at 24.0734 MHz. The output of the oscillator is buffered and then used by three frequency dividers to produce clock pulses for the 8088 processor and its support logic, the Z80A processor and its support logic, and the RX50 controller logic.

4.4.2.2 8088 Clock Logic – The 8088 clock logic consists of a 5:1 frequency divider and a TTL to MOS level converter. The 5:1 frequency divider provides three asymmetrical clock pulses (05A, 05B, and 05C) and their complements (05AL, 05BL, and 05CL) at a frequency of 4.815 MHz. The phase difference between the clock pulses is 40 ms. These clock pulses and their complements provide the basic timing for the 8088 and its support logic. The 05A clock pulses are converted to MOS voltage levels, then applied to the 8088 microprocessor. The 05C clock pulses are sent to a 2:1 frequency divider to provide 2.5 MHz clock pulses for the communications/printer MPSC and the keyboard PUSART. The 8088 clock pulse timing is shown in Figure 4-5.

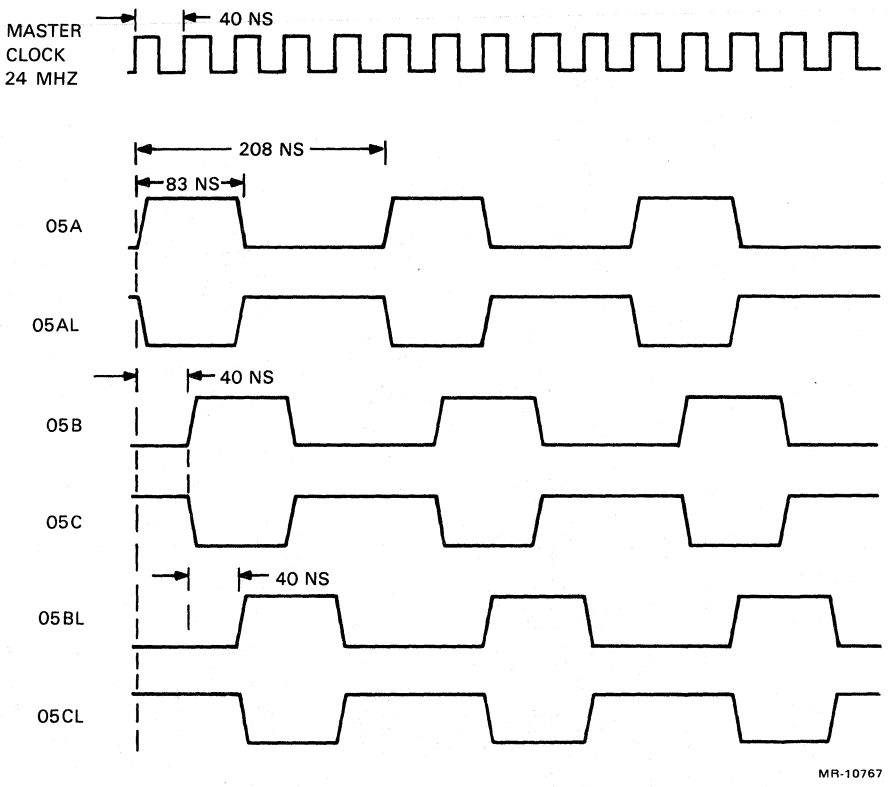


Figure 4-5 8088 Clock Pulses

4.4.2.3 Z80A Clock Logic – The Z80A clock logic consists of a 6:1 frequency divider and a TTL to MOS level converter. The 6:1 frequency divider provides three symmetrical clock pulses (04A, 04B, and 05C) and their complements (04AL, 04BL, and 04CL) at a frequency of 4.012 MHz. The phase difference between the clock pulses is 40 ns. The 04A clock pulses are converted to MOS voltage levels, then applied to the Z80A processor. The Z80A clock pulse timing is shown in Figure 4-6.

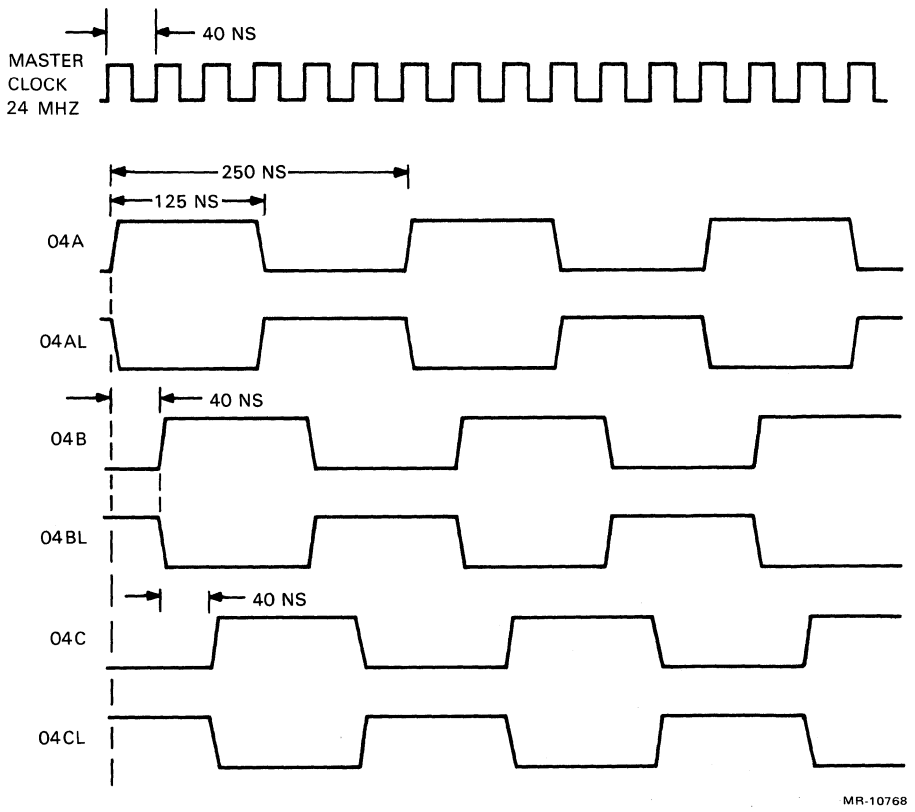


Figure 4-6 Z80A Clock Pulses

4.4.2.4 RX50 Controller Clock Logic – The RX50 controller logic consists of a 3:1 frequency divider and a 4-bit synchronous binary counter (Figure 4-3). The input to the 3:1 frequency divider is the 24 MHz master clock. The 8 MHz output of the 3:1 frequency divider is divided into 4, 2, and 1 MHz, and 500 kHz clock pulses by the synchronous binary counter. The 8, 4, 2, and 1 MHz and 500 kHz clock pulses are used to synchronize various logic functions of the RX50 controller.

The 500 kHz output of the synchronous counter is divided by 2 to produce 250 kHz clock pulses. The 500 and 250 kHz clock pulses are applied to the diagnostic disk/video loopback multiplexer and are used only during diagnostic testing.

4.4.3 8088 Processor

The 8088 is a high performance processor implemented in N-channel, depletion load, silicon gate technology (HMOS). It is mounted in a 40-pin dual in-line (DIP) package. The processor has attributes of both 8- and 16-bit processors.

The 8088 features a time-multiplexed address and data bus that permits some pins to serve dual functions. It can be operated in one of two modes (minimum or maximum) depending on the strapping of a single input pin to ground or +5 Vdc. In the Rainbow 100 computer, the 8088 operates in the minimum mode.

4.4.3.1 8088 Architecture

The 8088 processor has two separate processing units: the execution unit (EU) and the bus interface unit (BIU). These two processing units are shown in Figure 4-7.

The EU executes all instructions, provides data and addresses to the BIU, manipulates the eight general registers, and a flag register. Except for a few control pins, the EU is completely isolated from the external support logic.

The BIU executes all external bus cycles. The BIU controls six segment and two communications registers, the instruction pointer register, and the 4-byte instruction object code queue. The BIU combines segment and offset values in its dedicated adder to derive 20-bit addresses, transfers data to and from the EU on the arithmetic logic unit (ALU) data bus, and loads instructions into the instruction queue.

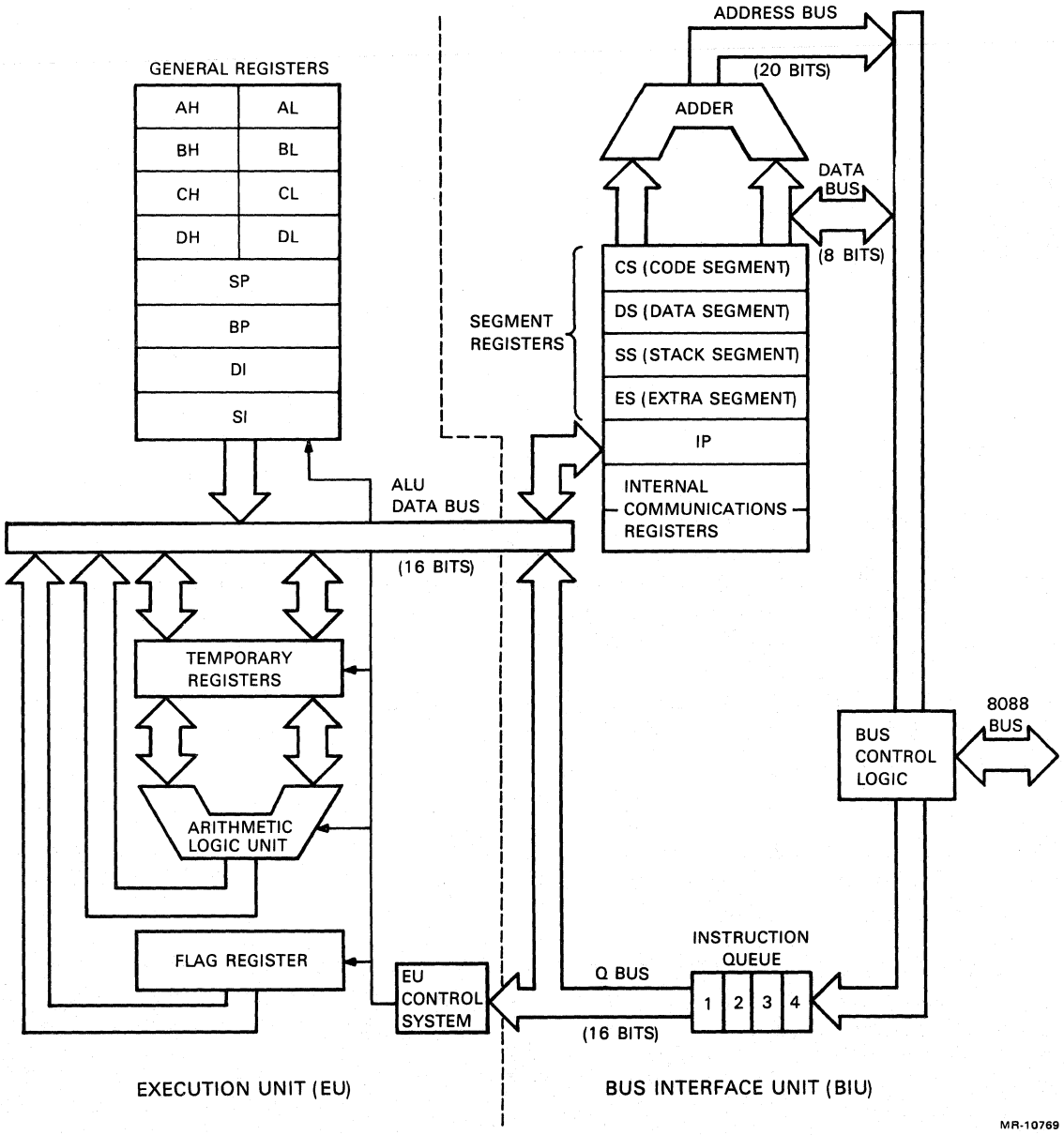


Figure 4-7 8088 Processor Block Diagram

When the EU is ready to execute an instruction, it fetches the instruction object code byte from the BIU's instruction queue and then executes the instruction. If the queue is empty, the EU waits for the instruction byte to be fetched. In the course of instruction execution, if a memory location or I/O port must be accessed, the EU requests the BIU to perform the required bus cycle.

The two processing sections of the processor operate independently. When one byte of the 4-byte queue is empty, the BIU executes an instruction fetch cycle. The 8088 accesses one instruction object code byte per bus cycle. If the EU issues a request for bus access while the BIU is processing an instruction fetch bus cycle, the BIU completes the cycle before honoring the EU's request.

4.4.3.2 Bus Operation – A bus cycle is an asynchronous event in which the 8088 processor transfers to the bus the address of a memory location or an I/O peripheral followed by either a read control signal (to read the data from the addressed device) or a write control signal and associated data (to write the data to the addressed device). The selected device (memory or I/O peripheral) accepts the data on the bus during a write cycle or places the data on the bus during a read cycle. On termination of the cycle, the device latches the data written or removes the data read.

All 8088 bus cycles consist of a minimum of four clock (CLK88H) cycles identified as states T1, T2, T3, and T4. A typical BIU bus cycle is shown in Figure 4-8. Detailed information for all the 8088 bus cycles can be obtained from Intel's *iAPX 88 Book*.

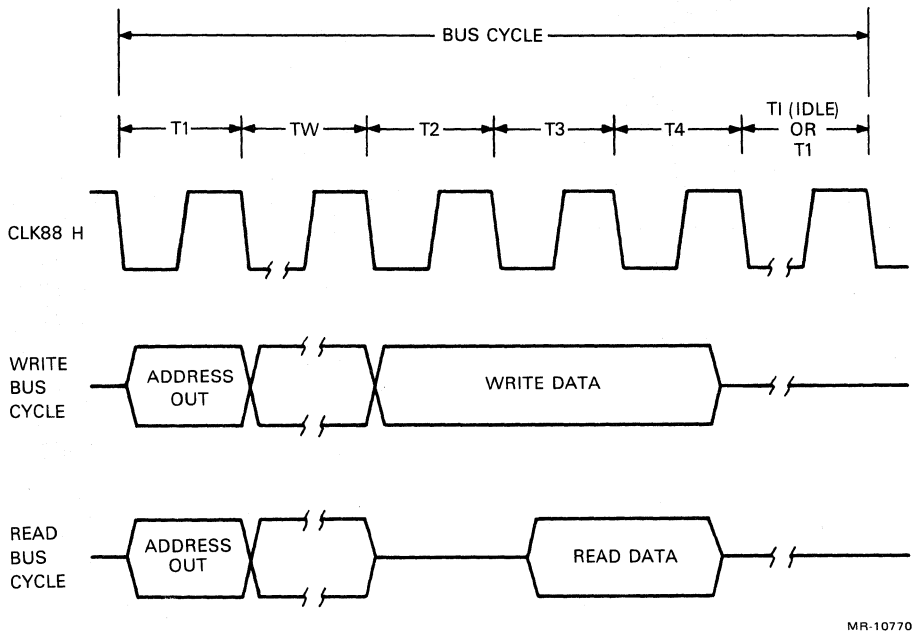


Figure 4-8 Typical BIU Bus Cycles

The 8088 places the address of the memory or I/O device on the address bus during state T1. During a write bus cycle, the 8088 places the data on the AD<7:0> bus from state T2 until T4. During a read bus cycle, the 8088 places the address on the multiplexed address/data bus in state T1 and then floats the bus in state T2 to allow the 8088 to change from the write mode to the read mode (input data). The 8088 accepts the data present on the address/data bus during states T3 and T4.

It is important to note that the BIU executes a bus cycle only when a bus cycle is requested by the EU as part of instruction execution or when it must fill the instruction queue. Consequently, clock periods in which there is no BIU activity can occur between bus cycles. These inactive clock periods are referred to as idle states (TI) and occur between state T4 of one bus cycle and state T1 of the succeeding bus cycle.

In addition to the idle state previously described, the 8088 includes a mechanism for inserting additional T-states in the bus cycle to compensate for devices (memory or I/O) that cannot transfer data at the rate determined by the clock period. These extra T-states are called wait states (TW) and, when required, are inserted between states T1 and T2. During a wait state, the data on the bus remains unchanged. When the device can complete the transfer (present or accept the data), it signals the 8088 to exit the wait state and to enter state T2.

4.4.3.3. 8088 Pin Description – The 40 pins of the 8088 processor are divided into six functional groups:

1. Address bus
2. Address/status bus
3. Address/data bus
4. Bus control outputs
5. Processor control inputs
6. Power inputs

The function of a number of the 8088 control pins is defined by the voltage level (Vcc or ground) applied to the minimum/maximum mode input (pin 33). Three of the 40 available pins of the 8088 are not used in the Rainbow 100 computer. The pin functions are described in Tables 4-1 and 4-2.

Table 4-1 8088 Processor Pin Descriptions

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
9–16	AD7–AD0	AD7–AD0	I/O	ADDRESS DATA BUS: These lines are the time multiplexed memory/IO address (T1) and data (T2, T3, TW, and T4) bus. These lines are active high and float to 3-state OFF during interrupt acknowledge.
2–8,39	A15–A8	A15–A8	O	ADDRESS BUS: These lines provide address bits 8 through 15 for the entire bus cycle (T1–T4). These lines do not have to be latched by ALE to remain valid. A15–A8 are active high and float to 3-state OFF during interrupt acknowledge.
38	A16	A16/S3	O	ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are low. During memory and I/O operations, status information is available on these lines during T2, T3, TW, and T4. S6 is always low. The status of the interrupt enable flag bit (S5) is
37	A17	A17/S4	O	
36	A18	A18/S5	O	
35	A19	A19/S6	O	

* Indicates direction of signal with respect to the 8088 processor. (O = output, I = input)

Table 4-1 8088 Processor Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
				updated at the beginning of each clock cycle. S4 and S3 are encoded as shown in Table 4-2. This information indicates which segment register is presently being used for data accessing.
32	RD88 L	RD	O	READ 88: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/M pin or S2. This signal is used to read devices that reside on the 8088 local bus. RD is active low during T2, T3, and TW of any read cycle, and is guaranteed to remain high in T2 until the 8088 local bus has floated.
22	READY H	READY	I	READY: is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. This signal is active high. The 8088 READY input is not synchronized. When READY is active low, wait states (TW) are added to the 8088 bus cycle.
18	INTR H	INTR	I	INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active high.
23	COMM/PRT INTR L	TEST	I	COMMUNICATION/PRINTER INTERRUPT REQUEST: input is examined by the "wait for test" instruction. If the COMM/PRT INTR input is low, execution continues; otherwise the processor waits in an idle state. This input is synchronized internally during each clock cycle on the leading edge of CLK88 H.
17	PARITY ERROR L	NMI	I	PARITY ERROR: is a nonmaskable interrupt input from the memory extension option. It is active low when a parity error occurs. The edge triggered input causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. Parity

* Indicates direction of signal with respect to the 8088 processor. (O = output, I = input)

Table 4-1 8088 Processor Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
				error is not maskable internally by software. The transition of the parity error signal from HIGH to LOW initiates the interrupt at the end of the current instruction. This input is internally synchronized.
21	RESET H	RESET	I	RESET: causes the processor to immediately terminate its present activity. The signal must be active high for at least four clock cycles. It restarts execution when RESET returns low. RESET is internally synchronized.
19	CLK88 H	CLK	I	CLOCK 8088: provides the basic timing for the processor. It is asymmetric with a 33% duty cycle to provide optimized internal timing. The frequency of the clock signal is 4.815 MHz.
40	+5 V	Vcc		VCC: is the +5 V power input.
1,20	GND	GND		GND: are the ground pins.
33	MN/MX	MN/MX	I	MINIMUM/MAXIMUM: determines the operating mode of the processor. A low on MN/MX selects maximum mode. A high on MN/MX selects minimum mode. This signal is tied to +5 V through a 330 ohm resistor in the Rainbow 100 computer.
28	IO/M	IO/M	O	INPUT OUTPUT/MEMORY: This status line is used to distinguish a memory access from an I/O access. IO/M becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = high, M = low).
29	WR88 L	WR	O	WRITE 88: Strobe indicates that the processor is performing a write memory or write I/O cycle depending on the state of the IO/M signal. WR88 L is active for T2, T3, and TW of any write cycle. It is active low.
24	INTAL	INTA	O	INTERRUPT ACKNOWLEDGE: is used as a read strobe for interrupt acknowledge cycles. It is active low for T2, T3, and TW of each interrupt acknowledge cycle.
25	ALE H	ALE	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the address latches. It is a high pulse active during T1 of any bus cycle. ALE is never floated.

* Indicates direction of signal with respect to the 8088 processor. (O = output, I = input)

Table 4-1 8088 Processor Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
27	DT/R	DT/R	O	DATA TRANSMIT/RECEIVE: is used to control the direction of data flow through the 8088 data transceivers. The timing of this signal is the same as IO/M (T = high, R = low).
26	DEN L	DEN	O	DATA ENABLE: is an output enable for the AD<7:0> data bus transceiver and the video processor data transceivers. The signal is active low during each memory and I/O access, and for interrupt acknowledge (INTA) cycles. For a read or INTA cycle, it is active from the middle of T2 until the middle of T4. For a write cycle, it is active from the beginning of T2 until the middle of T4.
31		HOLD	I	HOLD: When active high, this signal indicates that another bus master is requesting a local bus hold. This signal is not used in the Rainbow 100 computer and is tied to ground (low).
30		HLDA	O	HOLD ACKNOWLEDGE: is active high to acknowledge a HOLD request to the processor. This signal is not used by the Rainbow 100 computer.
34		SSO	O	STATUS LINE: The combination of SSO, IO/M, and DT/R allow the system to completely decode the current bus cycle. This signal is not used in the Rainbow 100 computer.

* Indicates direction of signal with respect to the 8088 processor. (O = output, I = input)

Table 4-2 Segment Register Status Encoding

S4*	S3	Characteristics
0 (Low)	0	Alternate Data
0	1	Stack
1 (High)	0	Code or None
1	1	Data

*S6 is 0 (low)

4.4.4 Z80A Processor

The Z80A is an 8-bit parallel processor mounted in a 40-pin dual in-line package. It has a 16-bit unidirectional address bus and an 8-bit bidirectional data bus for interfacing to 62K bytes of shared memory, 2K bytes of dedicated memory, the RX50 controller, and supporting logic. All output signals are fully decoded and timed to control the memory and RX50 controller.

The Z80A has internal registers that contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general purpose registers, which can be used individually as either 8-bit registers or 16-bit pairs. In addition, there are two sets of accumulator and flag registers. A group of exchange instructions make either set of main or alternate registers accessible to the programmer.

The Z80A also contains an additional set of six registers with assigned functions. Four of these are 16-bit registers, one for the stack pointer, one for the program counter, and two for indexed addressing. The Z80A also has two 8-bit registers: the interrupt register and the 8-bit refresh register.

The Z80A requires only a single +5 V power supply source. The internal block diagram (Figure 4-9) shows the primary functions of the Z80A processor.

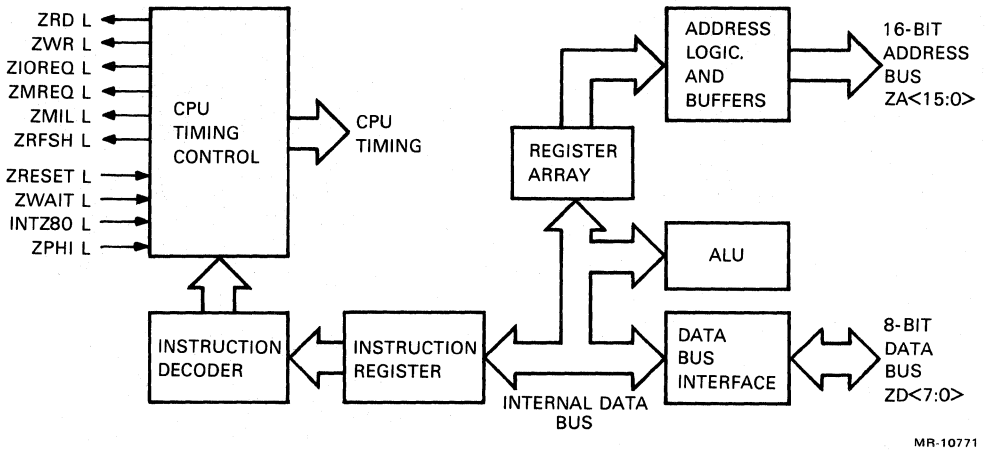


Figure 4-9 Z80A Processor Block Diagram

4.4.4.1 Z80A Basic Timing – The Z80A processor executes instructions in the following sequence:

1. Opcode fetch
2. Memory read or write
3. I/O device read or write
4. Interrupt acknowledge
5. Reset

Each instruction cycle consists of one or more machine cycles (M1, M2, M3, etc.). The number of machine cycles required depends on the specific instruction being executed. Each machine cycle consists of three or more T cycles (T1, T2, T3, T4).

Machine cycles can be extended either by the Z80A automatically inserting one or more wait cycles (TW) or externally by the Z80A support logic. The support logic supplies the wait control signal (ZWAIT L) to the Z80A whenever the memory or the RX50 controller needs more time to complete the data transfer.

Figure 4-10 shows the basic timing for a typical read or write cycle. The figure shows the typical timing of the Z80 clock, address, read, and write data. It does not show the control signals received or output during the cycle. Detailed information on the timing for the various machine cycles can be obtained from Zilog's *Z80™-CPU/Z80A™-CPU Technical Manual.*

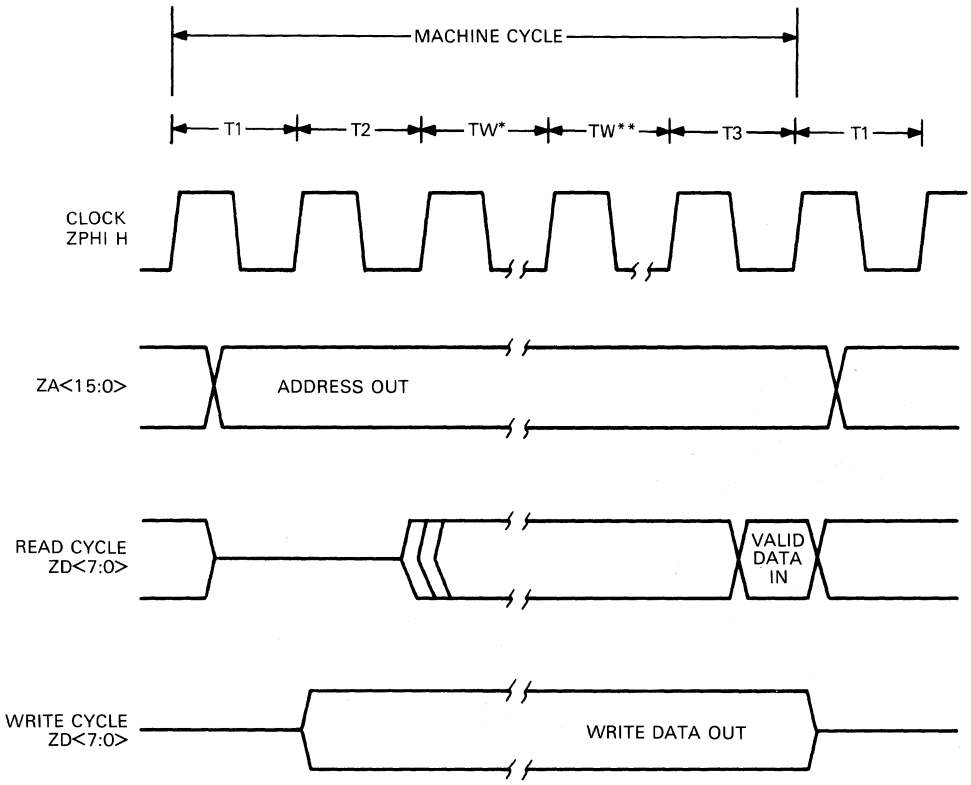


Figure 4-10 Basic Timing for Typical Z80A Read or Write Cycle

The Z80A places the address of the memory location or I/O device on the address bus ZA<15:0> during the T1 cycle where it remains throughout T2, T3, and any wait cycles that were added to the machine cycle. During a read cycle, the Z80A accepts data that was placed on the ZD<7:0> bus by the memory or I/O device in the T3 cycle.

During a write cycle, the Z80A places the write data to the memory or I/O device on the ZD<7:0> bus from the T2 cycle through the T3 cycle.

4.4.4.2 Z80A Pin Description – The 40 pins of the Z80A processor are divided into seven functional groups.

1. Address bus (16 pins)
2. Data bus (8 pins)
3. System control (6 pins)
4. Processor control (5 pins)
5. Processor bus control (2 pins)
6. Processor timing (1 pin)
7. Power (2 pins)

The Z80A processor as implemented in the Rainbow 100 computer does not require the functions provided by all of the 40 pins. The Rainbow 100 computer uses only 36 of the 40 pins. The pin functions are described in Table 4-3.

Table 4-3 Z80A Processor Pin Descriptions

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
1–5, 30–40	ZA<15:0>	A0–A15	O	ADDRESS BUS: ZA<15:0> form a 16-bit address bus. The address bus provides the address for memory data bus exchanges and I/O device exchanges.
23		BUSACK	O	BUS ACKNOWLEDGEMENT: indicates to the requesting device that the address bus, data bus, and control signals have entered their high-impedance states. This signal is not used by the Rainbow 100 computer.
25	BUSREQ	BUSREQ	I	BUS REQUEST: This signal, when active (low), forces the Z80A address bus, data bus, and control signals to go to a high-impedance state so that other devices can control these lines. This signal is always in active in the Rainbow 100 computer. It is tied to +5 V through a 4.7K resistor.
6	ZPHI L	CK	I	CLOCK: provides the basic timing for the Z80A. It is a symmetrical clock signal with a frequency of 4.012 MHz.
7–10 12–15	ZD<7:0>	D0–D7	I/O	DATA BUS: is the 8-bit bidirectional bus used for data exchanges with memory and I/O devices.
29	GND	GND		GROUND: is the Z80A ground pin.

* Indicates direction of signal with respect to the Z80A (O = output, I = input)

Table 4-3 Z80A Processor Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
18		HALT	O	HALT STATE: When active (low), this signal indicates that the Z80A has executed a Halt instruction and is awaiting either a nonmaskable or a maskable interrupt before operation can resume. This signal is not used in the Rainbow 100 computer.
16	INTZ80 L	INT	I	INTERRUPT REQUEST: This is the interrupt request from the 8088. The Z80A honors this request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop is enabled.
20	ZIORQ L	IORQ	O	INPUT/OUTPUT REQUEST: When low, this signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. ZIORQ L is also generated concurrently with ZMI L during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.
27	ZMI L	MI	O	MACHINE CYCLE ONE: ZMI L, together with ZMREQ L, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. ZMI L, together with ZIORQ L, indicates an interrupt acknowledge cycle.
19	ZMREQ L	MREQ	O	MEMORY REQUEST: When LOW, ZMREQ L indicates that the address bus holds a valid address for a memory read or memory write operation.
17	NMI	NMI	I	NONMASKABLE INTERRUPT: This signal is not used in the Rainbow 100 computer. It is tied to +5 V through a 4.7K ohm resistor to hold it inactive (high).
21	ZRD L	RD	O	MEMORY READ: When low, this signal indicates that the Z80A wants to read data from memory or an I/O device. The addressed memory or I/O device uses this signal to gate data on the ZD<7:0> bus.

* Indicates direction of signal with respect to the Z80A (O = output, I = input)

Table 4-3 Z80A Processor Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
26	ZRESET L	RESET	I	RESET: When low, Z RESET L initializes the Z80A as follows: it resets the interrupt enable flip-flop, clears the PC and the I and R registers, and sets the interrupt status to mode 0. During reset time, the address and data bus go to a high impedance state, and all control output signals go to the inactive state.
28	ZRFSH L	RFSH	O	REFRESH: This signal is active low. ZRFSH L together with ZMREQ L indicate that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.
24	ZWAIT L	WAIT	I	WAIT: ZWAIT L indicates to the Z80A that the addressed memory or I/O device is not ready for a data transfer. The Z80A continues to enter a wait state as long as this signal is active low.
22	ZWR L	WR	O	MEMORY WRITE: When low, indicates that the Z80A data bus holds valid data to be stored at the addressed location.
11	+5 V	Vcc		VCC: is the +5 V power input.

* Indicates direction of signal with respect to the Z80A (O = output, I = input)

4.4.5 System Module Memory

The system module memory available to the 8088 and the Z80A processors consists of ROM, RAM, and nonvolatile RAM. The memory types and memory sizes are as follows:

- 64K byte shared RAM (dynamic)
- 256 × 4 bit NVM
- 2K byte Z80A dedicated RAM (static)
- 4K byte screen RAM (static)
- 4K byte attribute RAM (static)

Additional memory is available to the 8088 and the Z80A when an optional memory extension module is installed on the system module. The memory extension module is available in two versions: 62K bytes (Part Number PC1XX-AA) or 192K bytes (Part Number PC1XX-AB). Both of these versions are dynamic random access memories (DRAM) that plug into connector J6 on the system module. The memory option is described in Chapter 3.

The 8088 memory map is shown in Figure 4-11.

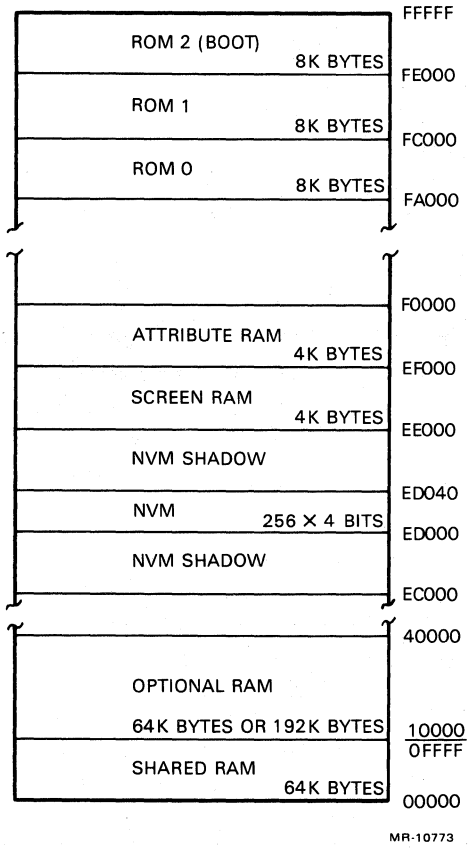


Figure 4-11 8088 Memory Map

The Z80A memory map is shown in Figure 4-12. The Z80A memory addresses are remapped in the 62K byte shared RAM and the 2K byte Z80A dedicated RAM when the address bit ZA<15> is inverted. ZA<15> is inverted by writing the diagnostic write register at address 21 H.

Figure 4-13 shows the memories and their relation to the 8088 and Z80A address and data buses. The system module memories are described in the following paragraphs.

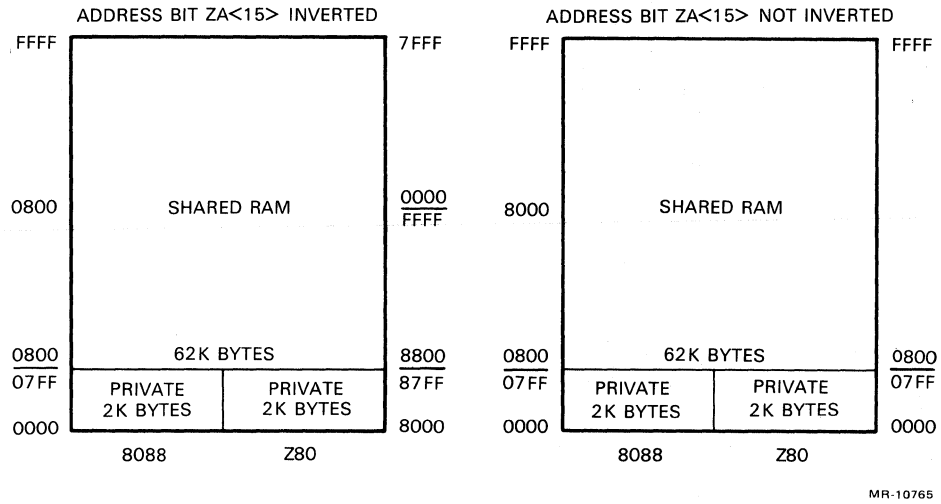


Figure 4-12 Z80A Memory Map

4.4.5.1 64K Byte Shared Memory – The 64K byte shared memory can be accessed by the 8088 processor, the Z80A processor, or the refresh logic via the shared memory address bus (SHMA<7:0>). The 8088 can access all 64K bytes of memory and uses the first 2K bytes to store interrupt vectors and other information that must not be changed by the Z80A. Therefore, the Z80A is prevented from accessing the first 2K bytes of the shared memory. Z80A addresses in the first 2K byte range will access the Z80A 2K byte dedicated RAM.

Accesses to the shared memory are controlled by the shared RAM row address strobe (SHRAM RAS L), the shared RAM column address strobe (SHRAM CAS L), and the shared RAM write (SHRAM WR L) signals from the RAS, CAS timing, and read/write (R/W) select logic. The shared memory arbitration logic supplies the input signals for the RAS, CAS timing, and R/W select logic and determines the priority for accesses to the shared memory. Refresh has the highest priority for memory accesses. The 8088 has approximately equal priority with the Z80A except in those instances where both processors simultaneously request access to the memory. If the 8088 and Z80A simultaneously request access to memory, the arbitration logic gives memory priority to the Z80A.

Data is written into or read from the shared memory by the 8088 or Z80A via the shared data bus (SHD<7:0>) and the shared memory data transceivers. The read or write operation of the shared memory is controlled by the SHRAM WR L signal from the RAS, CAS timing and R/W select logic. The SHRAM L signal level is determined by the 8088 data transmit/receive (DT/R) or the Z80A data transmit/receive (ZT/R) output signal, depending on which processor is accessing memory. These two signals, DT/R or ZT/R, are also used to control the direction of data transfer through the shared memory data transceivers.

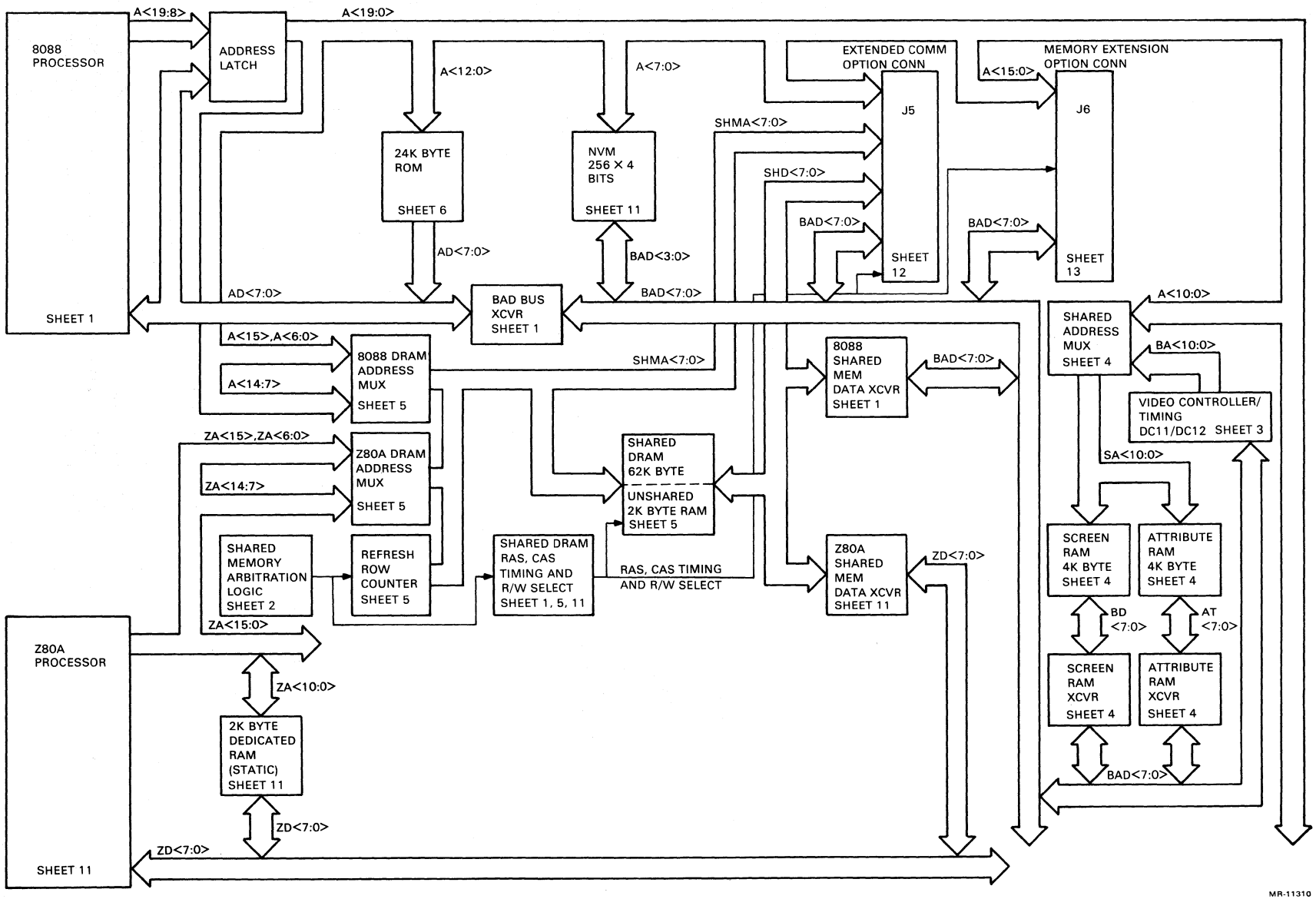


Figure 4-13 System Module Memory

4.4.5.2 24K Byte ROM – The 24K byte ROM consists of three 8K × 8 bit ROMs and are labeled ROM 0, ROM 1, and ROM 2. These ROMs contain the firmware for the Rainbow 100 system. The firmware consists of 8088 and Z80A code for diagnostic, terminal emulation, language translation, Set-Up, and bootstrap programs.

The 8088 accesses the 24K byte ROM via address bits A<12:0>. The data is read out of the ROM via the 8088 address/data bus AD<7:0>. The read operation is controlled by ROM select signals from the ROM select decoder and the read signal (RD88L) from the 8088. Figure 4-14 is a block diagram that shows the relationship of the 24K byte ROM to the ROM select decoder and the 8088.

Address bits A<15:13> are decoded by the ROM select decoder to select one of the three ROMs. Address bits A<19:16>, R/DT, and M/IO signals are active during a memory cycle and are used to gate out ROM 0 SEL L, ROM 1 SEL L, or ROM 2 SEL L, depending on the combination of address bits A<15:13> applied to the ROM select decoder. The RD88 L signal is applied to the enable input of the 24K byte ROM and gates the data onto the AD<7:0> bus.

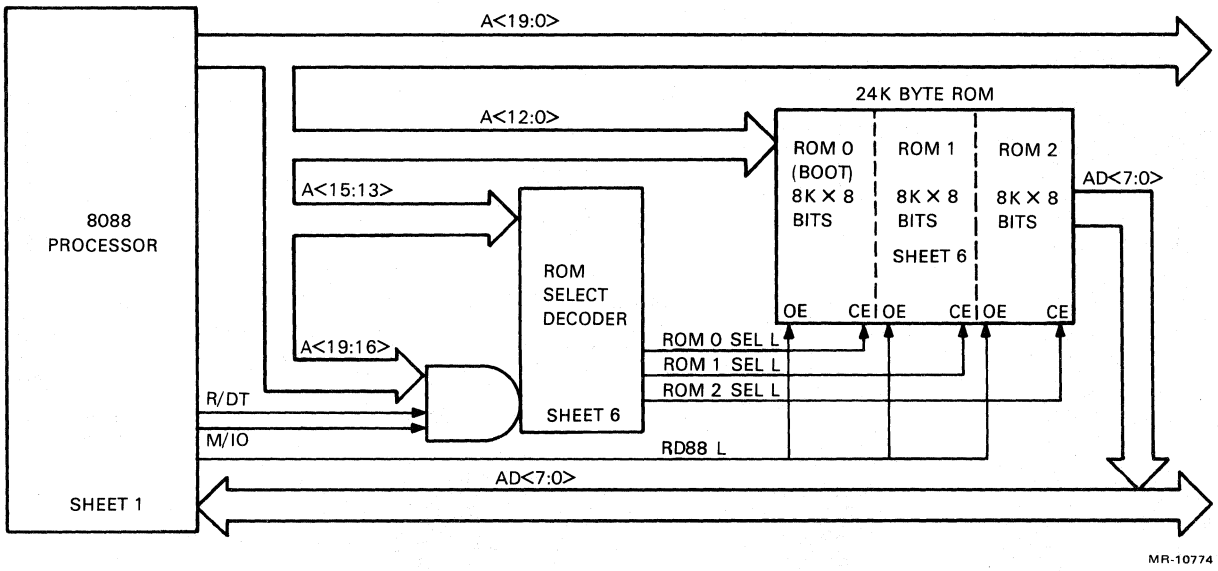


Figure 4-14 24K Byte ROM Block Diagram

4.4.5.3 256 × 4 Bit NVM – The NVM is a 256 × 4 bit nonvolatile memory that is overlaid by a 256 × 4 bit static RAM. The NVM is used to store the system Set-Up information desired when the Rainbow 100 computer is powered up. The Set-Up parameters stored in the NVM can be changed by writing new parameters into the static RAM and then storing this information in the NVM by performing a SAVE operation.

The 8088 processor accesses the NVM via address bits during a memory cycle through a combination of address bits A<19:13> and A<7:0>. Data is written into or read from the NVM via buffered address/data bits BAD<4:0>. Figure 4-15 is a block diagram that shows the relationship of the NVM to the 8088 and the NVM control logic.

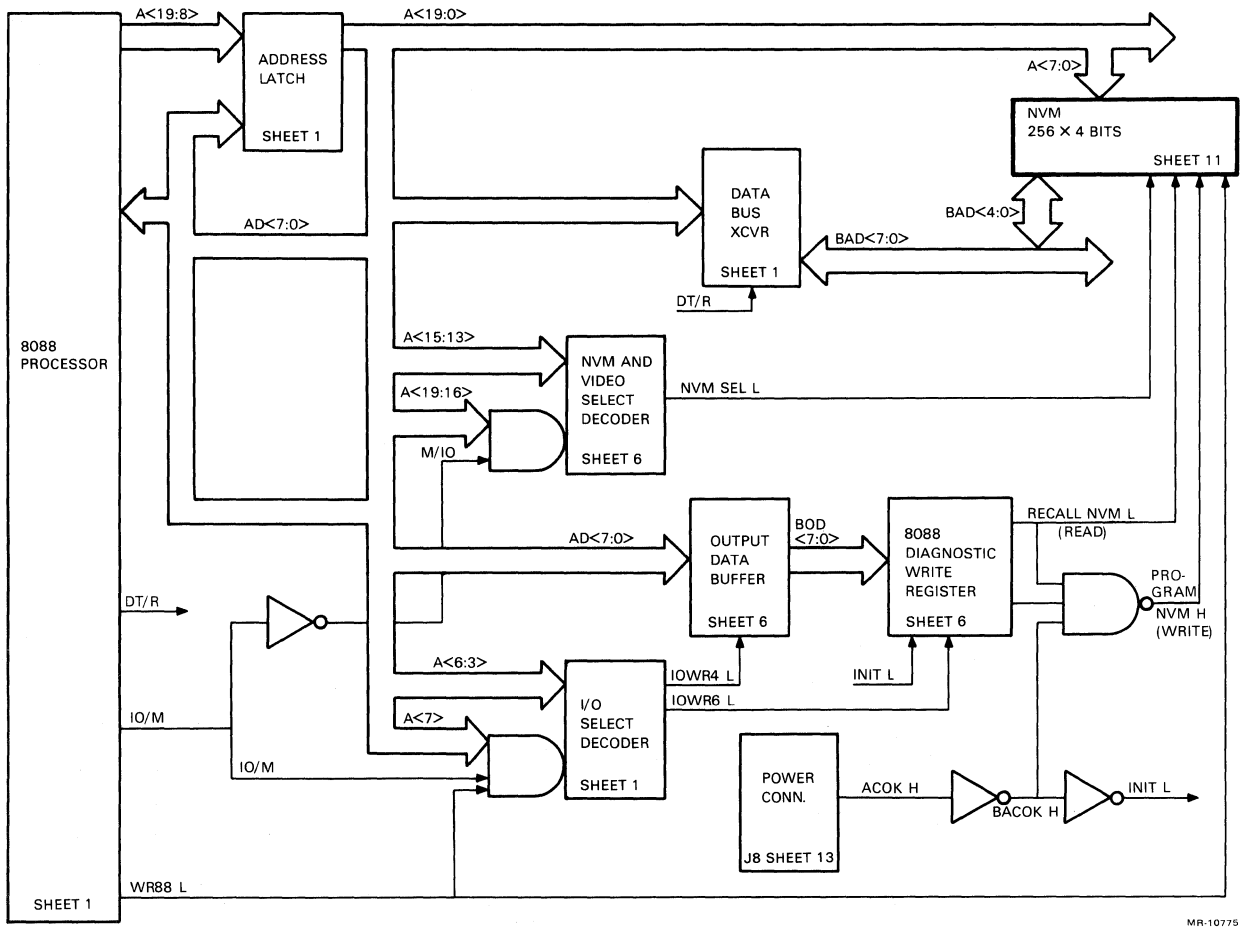


Figure 4-15 NVM Block Diagram

The following signals control the operation of the NVM:

- NVM SEL L
- RECALL NVM L
- PROGRAM NVM H
- WR88 L

The NVM SEL L signal is the chip select input of the NVM. This signal is asserted low by the NVM and video select decoder when the 8088 transfers a 1110110 binary bit pattern in address bits A<19:13> during a memory cycle. Address bits A<7:0> of the 20-bit address are applied to the address inputs of the NVM. Address bits A<12:8> are not decoded when accessing the NVM. This decoding scheme places the NVM contents in the 8088 memory map in locations ED000H through ED040H as well as a shadow of the NVM in two other blocks of address locations (See Figure 4-11).

The RECALL NVM L signal is bit 7 of the diagnostic write register. RECALL NVM is activated during Set-Up by performing a RECALL operation which recalls the original Set-Up features stored in the NVM. Bit 7 is set to 0 by the INIT L signal when the system is powered up. This bit is set to a 1 by the firmware before data from the NVM RAM is available. To perform a RECALL of the contents of the NVM after initialization, bit 7 of the register must be set to 0 and then back to 1.

The PROGRAM NVM L signal is bit 6 of the diagnostic write register. This bit is activated during Set-Up by performing a SAVE operation. The SAVE operation transfers the Set-Up features from static memory and stores them on a permanent basis in the NVM. This bit is used to transfer data from the static memory and store it on a permanent basis in the NVM. This bit is also set to 0 when the system is powered up. To perform a PROGRAM NVM operation, this bit is set to 0 and then back to 1. Once the PROGRAM NVM bit is set, the NVM cannot be accessed by the 8088 for 10 ms. During this time, the device is storing the data into the NVM. If another device operation is attempted within the 10 ms, it is ignored. Once the PROGRAM NVM operation is started, it cannot be changed unless the power is turned off. In this case, data in the device is not valid.

The WR88 L signal from the 8088 is applied to the I/O select decoder and the write enable input of the NVM. This signal is active low when the 8088 is performing a write operation to the shadow RAM.

4.4.5.4 2K Byte Z80A Dedicated RAM (Static) – The Z80A processor's dedicated memory is a 2K × 8 bit static RAM that is accessed by the Z80A via address bits ZA<10:0>. Data is written into or read from the memory via data bits ZD<7:0>. Figure 4-16 is a block diagram that shows the relationship of the 2K byte dedicated RAM to the Z80A address bus, data bus, and memory control logic.

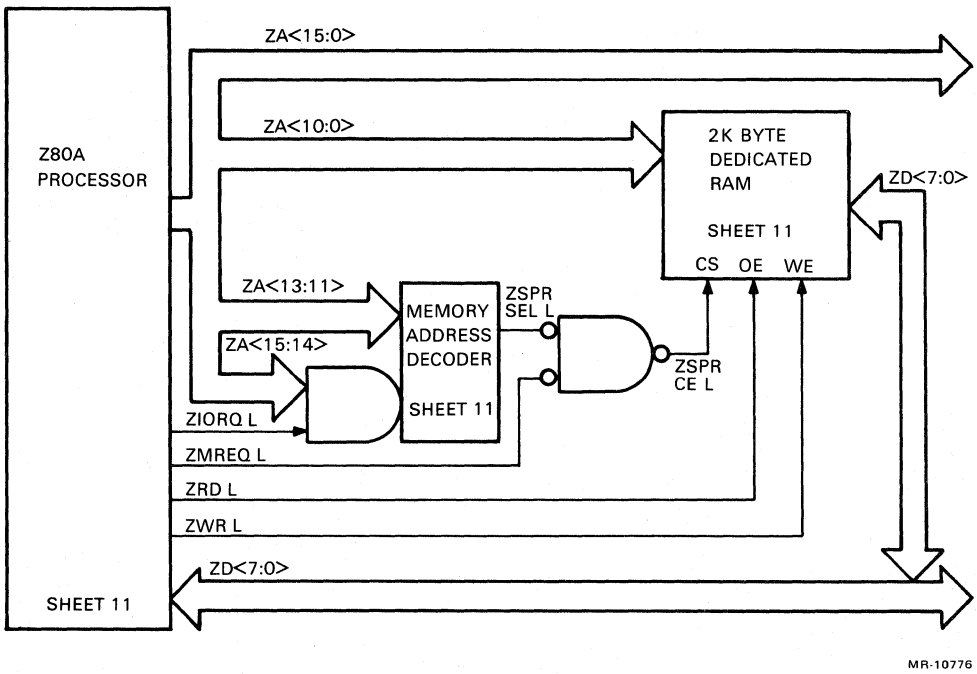


Figure 4-16 2K Byte Dedicated RAM Block Diagram

The following signals control the operation of the 2K byte dedicated RAM:

- ZSPR CE L
- ZRD L
- ZWR L

The Z80A scratch pad RAM chip enable (ZSPR CE L) signal is applied to the chip select input of the 2K byte RAM. This signal is asserted low by the Z80 scratch pad RAM select (ZSPR SEL L) signal and the

memory request (ZMREQ L) signal from the Z80A during a memory cycle. ZSPR SEL L is asserted by the memory address decoder when the Z80A outputs an address in the 0000H to 07FFH (0 to 2K) range and an I/O cycle is not in progress.

The Z80A read (ZRD L) signal is applied to the output enable input of the 2K byte RAM. ZRD L is asserted by the Z80A during a memory read cycle to gate the data onto the ZD<7:0> bus.

The Z80A write signal is applied to the write enable input of the 2K byte RAM. This signal is asserted during a memory write cycle to take data from the ZD<7:0> bus and store it in the memory location specified by address bits ZA<10:0>.

4.4.5.5 4K Byte Screen RAM and 4K Byte Attribute RAM (Static) – The screen RAM and attribute RAM can be accessed by the 8088 processor or the video processor. The 8088 uses these memories to temporarily store the character and attribute (character, line, and screen) data to be displayed on the screen. The video processor directly accesses the memories (DMA) via its address bus to retrieve the stored character and attribute data and then converts the data into a video signal that the monitor uses to produce the screen display. Figure 4-17 is a block diagram that shows the memories and their relation to the 8088, the video processor, and the control logic.

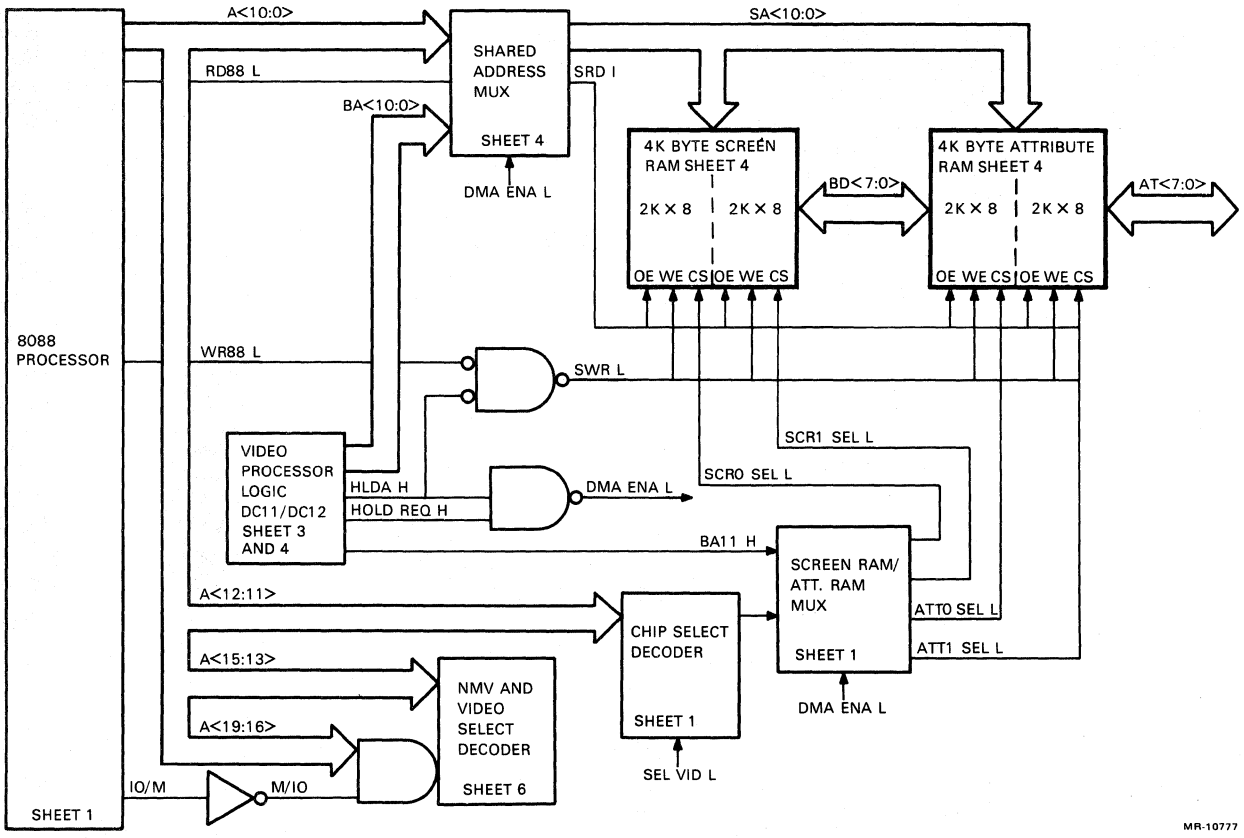


Figure 4-17 Screen RAM and Attribute RAM Control

The screen RAM and attribute RAM each consist of two 2K × 8 bit static RAMs. The RAMs are accessed via the shared address bus SA<10:0> from the shared address multiplexer. The address inputs to the shared address multiplexer are address bits A<10:0> from the 8088 and the buffered address bits BA<10:0> from the video proccessor. The direct memory access enable (DMA ENA L) signal applied to the select input of the shared address multiplexer determines whether the 8088 or the video processor accesses the memories. DMA ENA L is asserted low when the video processor is accessing the memories.

Character data is written into or read out of the screen RAM via the buffered data bus BD<7:0>. The data on this bus is transferred from the BAD<7:0> bus through the screen RAM transceiver.

Attribute data is written into or read out of the attribute RAM via the attribute bus AT<7:0>. The data on this bus is transferred from the BAD<7:0> bus through the attribute RAM transceiver.

The following signals control the operation of the screen RAM and attribute RAM:

- SCR0 SEL L
- SCR1 SEL L
- ATT0 SEL L
- ATT1 SEL L
- SRD L
- SWR L

The inputs to the screen RAM/attribute RAM multiplexer are obtained from the video processor logic during a DMA or the 8088 when character and attribute data is to be written into the screen RAM. The buffered address bit BA11 from the video processor logic is used by the screen RAM/attribute RAM multiplexer to select either attribute RAM 0 or 1 during a DMA.

During a non-DMA, the 8088 supplies the chip select inputs to the screen RAM/attribute RAM multiplexer through a 2-line to 4-line chip select decoder. Address bits A<12:11> are decoded and sent to the screen RAM/attribute RAM multiplexer to produce the screen RAM select or attribute RAM select signals (SCR0 SEL L, SCR1 SEL L, ATT0 SEL L and ATT1 SEL L).

The 8088 outputs address bits A<19:13> and the IO/M signals during a screen RAM and attribute RAM access to the NVM and video select decoder. When these address bits are in the correct screen and attribute RAM address range (EEOOOH to FOOOOH), the NVM and video select decoder asserts SEL VID L to enable the chip select decoder.

Data is written into the screen and attribute RAM by the 8088 during a write memory cycle. The WR88 L signal from the 8088 is ANDed with the HLDA H signal from the video processor logic to produce SWR L. HLDA will be negated (low) if the video processor is not performing a DMA. SWR L is applied to the write enable inputs of the screen RAM and attribute RAM to gate the data on the BA<7:0> and AT<7:0> bus into the screen and attribute RAM address location specified by address bits A<10:0>.

Data is read out of the screen and attribute RAM by the video processor during a DMA read memory cycle. The RD88 L signal from the 8088 is gated through the shared address multiplexer by DMA ENA L. The 8088 is held in a wait state during a video processor DMA. The SRD L signal from the shared address multiplexer is applied to the output enable input of the screen and attribute RAM to gate the data out of the screen and attribute address location specified by address bits BA<10:0> and onto the BD<7:0> and AT<7:0> buses. The BD<7:0> and the lowest four attribute bits AT<3:0> are then sent to the video processor where they are used to generate the video signal for the monitor.

4.4.6 I/O Decoders

The system module contains two sets of I/O decoders that are used by the 8088 processor and the Z80A processor to select and control the transfer of data through the I/O ports. The 8088 and Z80A I/O decoders are described in the following paragraphs.

4.4.6.1 8088 I/O Decoders – Three I/O decoders are used by the 8088 processor to supply read/write control signals to the various registers and select signals to the communications/printer serial controller, the keyboard PUSART, the color/graphics option, and the extended communications option. The three decoders are the I/O read decoder, the I/O write decoder, and the I/O port select decoder. The I/O decoders supply control and select signals to the following registers and devices:

- Communications status register
- Communications control register
- Diagnostic read register
- Diagnostic write register
- DC11 write register
- DC12 write register
- Massive hardware failure (MHFU) detection logic
- Communications baud rate generator
- Printer baud rate generator
- Communications/printer serial controller
- Keyboard PUSART
- Graphics option
- Extended communications option

Figure 4-18 is a block diagram that shows the relationship between the I/O decoders, the 8088, the registers, and the I/O devices. The I/O decoders use address bits A<7:1>, the read/write signals, and the input/output memory signal from the 8088 to control their operation. All three I/O decoders are 3-line to 8-line decoders.

The 8088 I/O port select decoder decodes address bits A<6:4> when it is enabled by address bit A<7> and the input/output memory signal. IO/M will be active high when the 8088 is performing an input/output read or write cycle. When address bits A<6:4> are all active low, the I/O decoder enable signal will go low to provide one of the enable inputs to the I/O read and I/O write decoders. The active selected output of the I/O port select decoder is determined by various combinations of address bits A<6:4>.

The 8088 I/O write decoder decodes address bits A<3:1> when it is enabled by the write (WR88 L) signal and the I/O decoder enable signal from the I/O port select decoder. The outputs of the I/O write decoder are used to enable a particular register or baud rate generator to accept the write data from the 8088. When address bits A<3:1> are all active low, the 88INTZ signal will go low and reset the INT Z80A flip-flop to interrupt the Z80A processor.

The 8088 I/O read decoder decodes address bits A<3:1> when it is enabled by the read (RD88 L) signal and the I/O decoder enable signal from the I/O port select decoder. Two of the outputs from the I/O read decoder are applied to the communications status register and the diagnostic read register to read the contents of these registers onto the 8088 BAD<7:0> bus. The third output, CLR88 L, is active low when all address bits A<3:1> are low. The CLR88 L signal clears the interrupt 8088 flip-flop to prevent the Z80A from interrupting the 8088.

Data, control, and status information is read from or written into the various registers under software control. These registers are read or written by the program using instructions referring to a particular register address. Table 4-4 lists the I/O addresses and the registers they access.

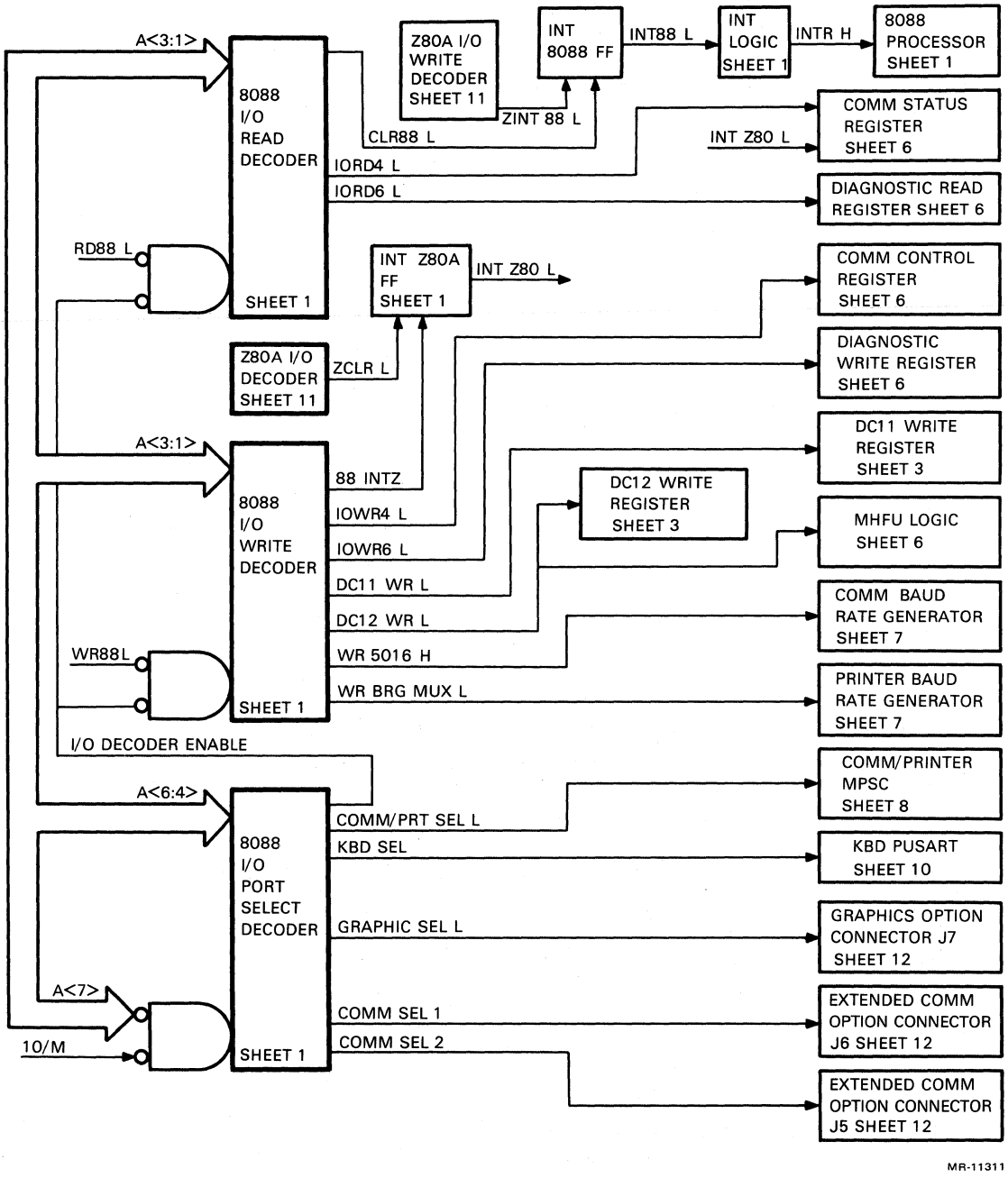


Figure 4-18 8088 I/O Decoders

Table 4-4 8088 I/O Addresses

Address (Hexadecimal)	Function	Type*
00H	Interrupts Z80A flop	WO
00H	Clears 8088 interrupt flop	RO
02H	Communications and LED register	WO
02H	General communications status	RO
04H	DC011 write register	WO
06H	Communications baud rate register	WO
OAH	Maintenance port	WO
0AH	Maintenance port	RO
0CH	DC012 write register	WO
OEH	Printer baud rate register	WO
10H	Keyboard data register (8251A)	R/W
11H	Keyboard control/status register (8251A)	R/W
20H–2FH	Extended communications option/option select 1	R/W
40H	Communications data register (MPSC)	R/W
41H	Printer data register (MPSC)	R/W
42H	Communications control/status register (MPSC)	R/W
43H	Printer control/status register (MPSC)	R/W
5H0–5FH	Graphics option select	R/W
60H–6FH	Extended communications option/option select 2	

*WO = Write only, RO = Read only, R/W = Read/write

4.4.6.2 Z80A I/O Decoders – The Z80A processor uses two I/O decoders to supply read/write control signals to nine status and control registers for the diskette drive. These registers are located both on the system module and the RX50 controller module. The read/write control signals for the status and control registers located on the RX50 controller module are routed through the RX50 controller connector (J9). The decoders also supply interrupt control signals for the Z80A and the 8088 processors.

The two I/O decoders supply the read/write control signals to the following registers:

- Diskette control register (RX50 controller module)
- Diskette status register (RX50 controller module)
- General/diagnostic status register (RX50 controller and system module)
- General/diagnostic control register (system module)
- FDC command register (RX50 controller)
- FDC status register (RX50 controller)
- FDC track register (RX50 controller)
- FDC sector register (RX50 controller)
- FDC data register (RX50 controller)

Figure 4-19 is a block diagram that shows the relationship between the I/O decoder, the Z80A processor, and the registers. Address bits ZA<6:5>, input/output read (ZIORD L), and input/output write (ZIOWR L) are used to control the operation of the I/O decoders. Both of the decoders are 2-line to 4-line decoders.

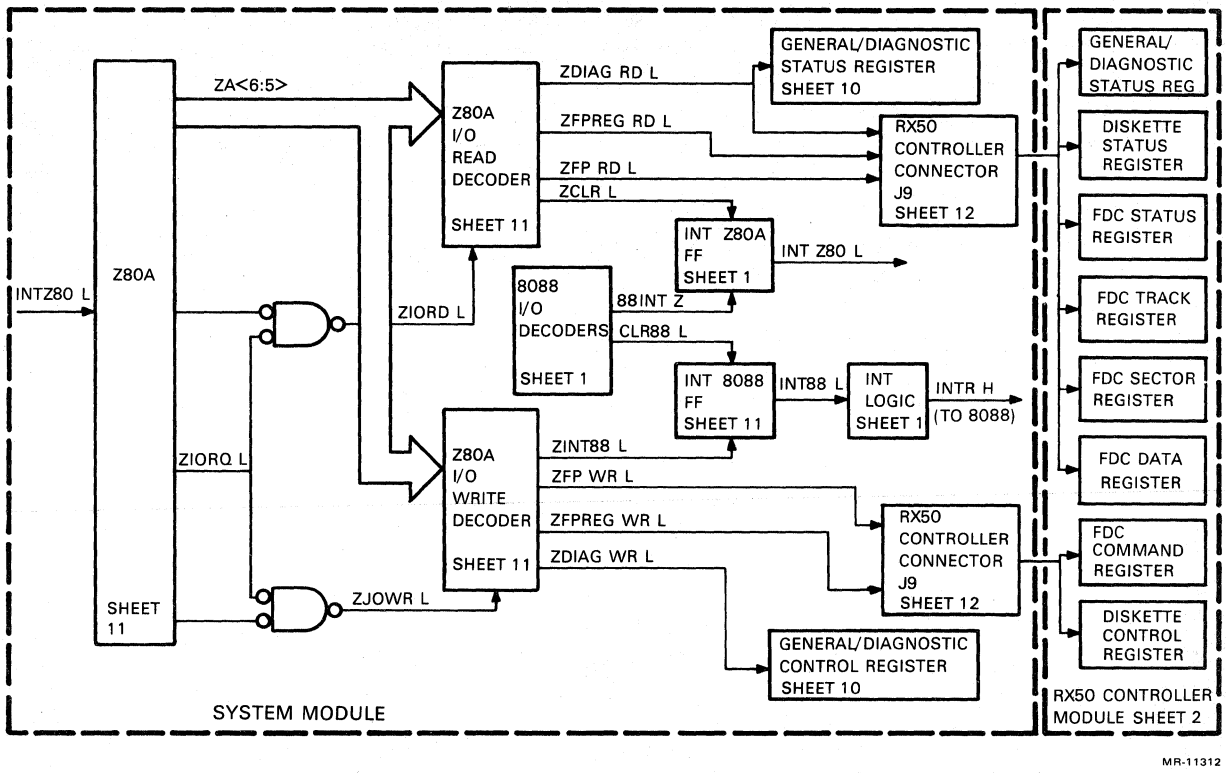


Figure 4-19 Z80A I/O Decoders

The I/O read decoder decodes address bits ZA<6:5> when it is enabled by ZIORD L during a Z80A I/O read cycle. The I/O read decoder outputs are applied to the general diagnostic status register, the diskette status register, and to internal registers of the FDC controller chip to transfer the contents of these registers onto the ZD<7:0> bus. Note that bits ZD<2:0> of the general/diagnostic register are obtained from the system module, and the remaining bits ZD<7:3> are obtained from the RX50 controller module. When address bits ZA<6:5> are low, ZCLR L is asserted and clears the INT Z80A flip-flop.

The I/O write decoder decodes address bits ZA<6:5> when it is enabled by the ZIOWR L during a Z80A I/O write cycle. The I/O write decoder outputs are applied to the general/diagnostic control register, the diskette control register, and the internal registers of the FDC controller chip to enable the registers to accept the write data from the Z80A. When address bits ZA<6:5> are low, the I/O write decoder asserts ZINT88 L to clear the INT 8088 flip-flop and interrupt the 8088.

The I/O addresses and the registers they access are listed in Table 4-5.

Table 4-5 Z80A I/O Addresses

(Address* (Hexadecimal)	Function	Type†
00H	Clear interrupt to Z80A	RO
00H	Interrupts 8088	WO
21H	General/diagnostic status register	RO
21H	General/diagnostic control register	WO
40H	Diskette status register	RO
40H	Disk control register	WO
60H	FDC status register	RO
60H	FDC control register	WO
61H	FDC track register	R/W
62H	FDC sector register	R/W
63H	FDC data register	R/W

* The above Z80A I/O addresses are remapped within their own pages and are also remapped starting at address 80H. Writing the general/diagnostic control register at address 21H will reset the ZFLIP bit (A<0>). Writing the general/diagnostic control register at address 20H will set the ZFLIP bit.

† WO = Write only, RO = Read only, R/W = Read/write

4.4.7 Interrupt Logic

The 8088 processor accepts maskable interrupts from seven sources according to priority levels assigned to each interrupting source and one nonmaskable interrupt. The only interrupt source for the Z80A processor is the interprocessor interrupt from the 8088. When the 8088 or the Z80A receives an interrupt request, the interrupted processor will complete execution of the current instruction and then jump to the interrupt service routine for the interrupting source. Figure 4-20 is a block diagram that shows the interrupt logic for the 8088, the Z80A, and the interprocessor interrupts.

4.4.7.1 8088 Interrupts – Interrupts to the 8088 processor can be initiated by software or hardware. Software interrupts originate directly from program execution or indirectly through program logic. Hardware interrupts originate from external logic and are classified as either maskable or nonmaskable. All interrupts, whether initiated by software or hardware, result in transfer of control to an interrupt service program.

The seven maskable hardware interrupts to the 8088 come from the following sources:

- Interprocessor interrupt from the Z80A
- Keyboard
- Communications or printer MPSC
- Video controller (DC12)
- Optional color/graphics module
- Optional extended communications module (two interrupts)

The nonmaskable hardware interrupt (NMI) to the 8088 is asserted by the memory extension option when it detects a parity error. The NMI will cause the 8088 to display an error message on the screen and then halt. Once the 8088 receives an NMI, it can be restarted only by entering Set-Up and resetting the system.

The seven hardware interrupts are sent through seven transparent latches to an 8-line to 3-line interrupt priority encoder. The interrupt priority encoder sends a 3-bit priority level code to the interrupt type encoder for temporary storage and, at the same time, asserts the INTR H signal to interrupt the 8088. The interrupt type encoder uses the 3-bit priority level code to encode the BAD<2:0> bits of the interrupt type number. The BAD<7:3> bits of the interrupt type number are hardwired into the interrupt type encoder.

When the 8088 accepts the interrupt request, it asserts interrupt acknowledge (INTA L) to disable the interrupt latches and gate the interrupt type bits onto the BAD<7:0> bus. The interrupt type bits are used by the 8088 as pointers to the interrupt vector addresses. The 8088 interrupt vector addresses are described in Table 4-6.

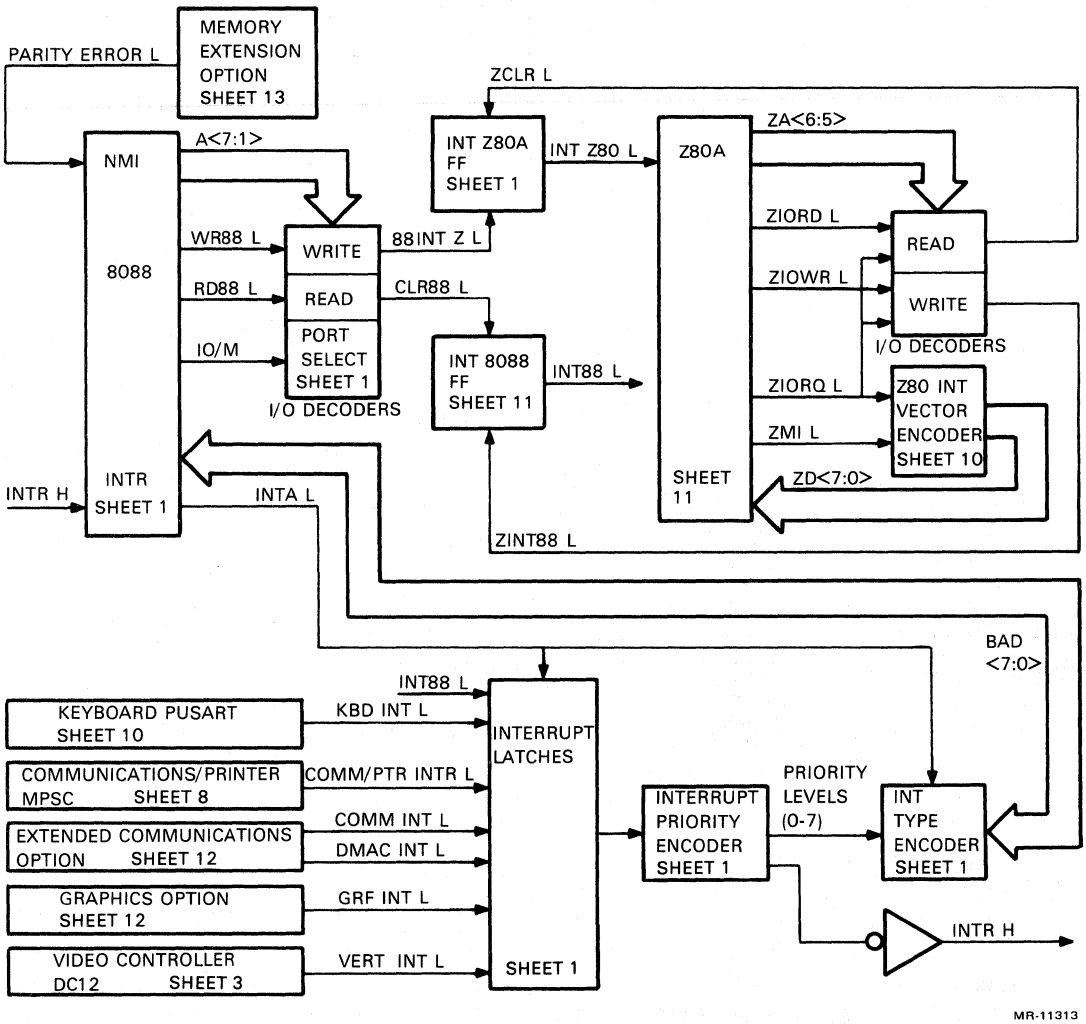


Figure 4-20 Interrupt Logic Block Diagram

Table 4-6 8088 Interrupt Vector Addresses

Priority Level*	Mnemonic	Interrupt Source	Interrupt Type†	Vector Address†
7	VERT INTR L	DC12 video controller	20	80
6	NOT USED			
5	GRF INTR L	Color/graphics module (optional)	22	88
4	DMAC INTR L	DMA controller (hard disk drive or input to extended communications option)	23	8C
3	COMM/PTR INTR L	Communications/printer MPSC	24	90
2	COMM INTR L	Optional extended communications interrupt	25	94
1	KBD INT L	Keyboard PUSART	26	98
0	INT88 L	Interrupt from Z80A	27	9C

*7 = Highest, 0 = Lowest
† Hexadecimal

4.4.7.2 Z80A Interrupts – The Z80A processor can be interrupted only by the 8088 processor through a D-type flip-flop. When the Z80A accepts the interrupt request (INTZ80 L) from the 8088, it will complete execution of the current instruction and then initiate an interrupt request/acknowledge cycle. During this cycle, ZIORQ L and ZMI L are asserted low to enable the Z80A interrupt vector encoder and gate the Z80A interrupt vector address onto the ZD<7:0> bus.

The interrupt vector address (F7H) placed on the bus is hardwired into the Z80A interrupt vector encoder. The F7H interrupt vector address causes the Z80A to perform an RST 30 instruction in interrupt mode 0.

4.4.7.3 Z80A/8088 Interprocessor Interrupts – Each processor has a D-type flip-flop that it uses to interrupt the other processor. The Z80A processor uses the INT 8088 FF and the 8088 processor uses the INT Z80A FF.

1. INT Z80A FF – The INT Z80A FF is set and cleared by control signals from the 8088 I/O write decoder and the Z80A I/O read decoder. The flip-flop is set when the 8088 performs an I/O write cycle to I/O port OOH and causes the I/O write decoder to assert 88INTZ L. The flip-flop is cleared by the ZCLR L signal from the I/O read decoder when the Z80A performs an I/O read cycle to port OOH. The read/write data is irrelevent. The firmware clears the flip-flop when the system is turned on.

2. INT 8088 FF – The INT 8088 FF is set and cleared by control signals from the Z80A I/O write decoder and the 8088 I/O read decoder. The flip-flop is set when the Z80A performs an I/O write cycle to I/O port OOH and causes the I/O write decoder to assert ZINT88 L. When set, the flip-flop asserts INT88 L and interrupts the 8088 at priority level 0. The flip-flop is cleared by the CLR88 L signal from the I/O read decoder when the 8088 performs an I/O read cycle to port OOH. The read/write data is irrelevent. The firmware clears the flip-flop when the system is turned on.

4.4.8 Video Processor

The video processor is a subsystem of the system module that converts data from the 8088 processor into a composite video signal that the monitor uses to display letters, numbers, and symbols. The video processor subsystem consists of two central devices (the DC11 video timing and DC12 video control chips), the screen RAM, attribute RAM, character generator ROM, and supporting logic. Figure 4-21 is a block diagram that shows the address and data flow through the video processor.

The 8088 processor puts ASCII encoded character data to be displayed in the screen RAM and attribute data in the attribute RAM. The video processor then retrieves the character and attribute data a line at a time by direct memory accesses (DMAs) to the screen and attribute RAMs. The character data is converted into streams of pulses, modified according to the attributes selected. The pulses are sent to the monitor where they are converted into light to form characters on the monitor screen. The DC11 and DC12 custom ICs provide the complex timing and control signals necessary to convert the ASCII data into the composite video signal required by the monitor.

The video processor supports the following features:

- 24-line × 80-column display
- 24-line × 132-column display
- Smooth scrolling (full screen and split screen)
- Jump scrolling (full screen and split screen)
- Double-height lines
- Double-width lines
- Reverse video
- Bold characters
- Underlined characters
- Block or underline blinking cursor
- ROM-resident character generator patterns
- Composite video output

The video processor can also modify various attributes of the monitor display. These functions are performed by the DC11 and DC12 chips. Three groups of attributes apply to the Rainbow 100 computer display: screen, line, and character.

The screen attributes affect the characteristics of the entire screen area. The attributes are stored in the NVM. During Set-Up, power-up, or reset, the 8088 processor reads the Set-Up specifications and writes them into the DC11 and DC12 via the BAD<7:0> bus to establish the screen attributes. The screen attributes are the following:

- Jump or smooth scrolling
- 80- or 132-column screen width
- Dark or light screen background
- 50 Hz or 60 Hz screen refresh rate

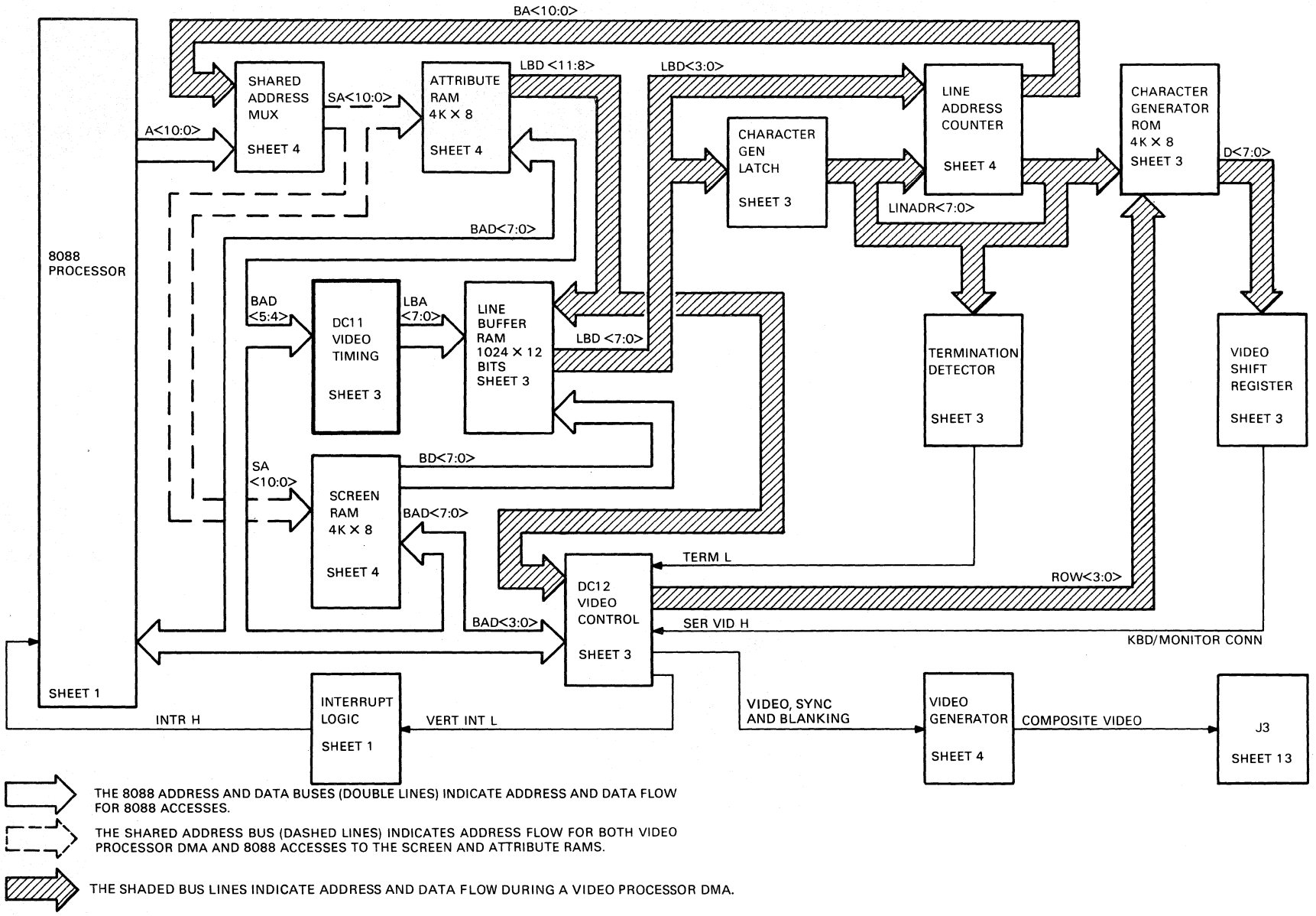


Figure 4-21 Video Processor Block Diagram

Line attributes affect the characteristics of all characters on a single line of the screen. These attributes are selected by software on a line-by-line basis and include the following:

- Single-width characters
- Double-width characters
- Double-height and double-width characters
- Scroll to indicate that the line is in a scrolling or nonscrolling area of the display

Character attributes are selected by software on a character-by-character basis to affect the appearance of characters displayed on the screen. The attributes can be selected singly or in any combination. The character attributes include the following:

- Underlined character
- Reversed video character
- Bold character (increased intensity)
- Blinking character

4.4.8.1 8088 Processor-Video Processor Interface – The 8088 processor communicates with the video processor in the following ways:

1. During Set-Up, the 8088 reads the Set-Up specifications and writes them into the DC11 and DC12 to establish the screen attributes.

2. The contents of the screen RAM and the attribute RAM directly control the display of the lines and characters. These RAMs contain the displayable characters, the character attributes, the line attributes, and the addresses that link one line of characters to the next.

3. During smooth scrolling, the 8088 updates the scroll latch in the DC12 control chip.

4.4.8.2 Screen RAM and Attribute RAM – The screen RAM and attribute RAM store the character and attribute data for display on the monitor screen. The RAMs are organized according to the Set-Up screen width specifications. The RAMs can hold 24 lines of 80 or 132 characters and their line/character attributes.

The 8088 can access these RAMs to read and write data 90 percent of the time. For the remaining time, the video processor takes full control of these memories to retrieve and process the data for display. When the video processor controls the memories, it holds the 8088 in a wait state and provides its own addresses BA<10:0> to directly access the memories (DMA) to retrieve the stored data. The video processor needs the fast access the DMA provides because the data rate required to display a line of characters is greater than the 8088 can handle.

The 8088 and the video processor access the 4K byte screen RAM and the 4K byte attribute RAM through a shared address multiplexer. The 8088 stores each character in a line in one of a group of adjoining locations in the screen RAM. The character and line attributes are stored in adjoining locations in the attribute RAM. Only the four least significant bits of the character attribute bytes are actually looked at by the video processor.

The screen and attribute addresses access corresponding locations in adjacent 4K byte banks of the 8088 memory (Figure 4-11).

The screen RAM addresses access locations in the lower 4K byte bank and start at address EE000 H. The attribute RAM addresses access locations in the upper 4 K byte bank and start at address EF000 H.

Three bytes of control data are located at the end of each line of characters stored in memory. Figure 4-22 shows the line organization of the stored data for the different combinations of screen and line attribute parameters.

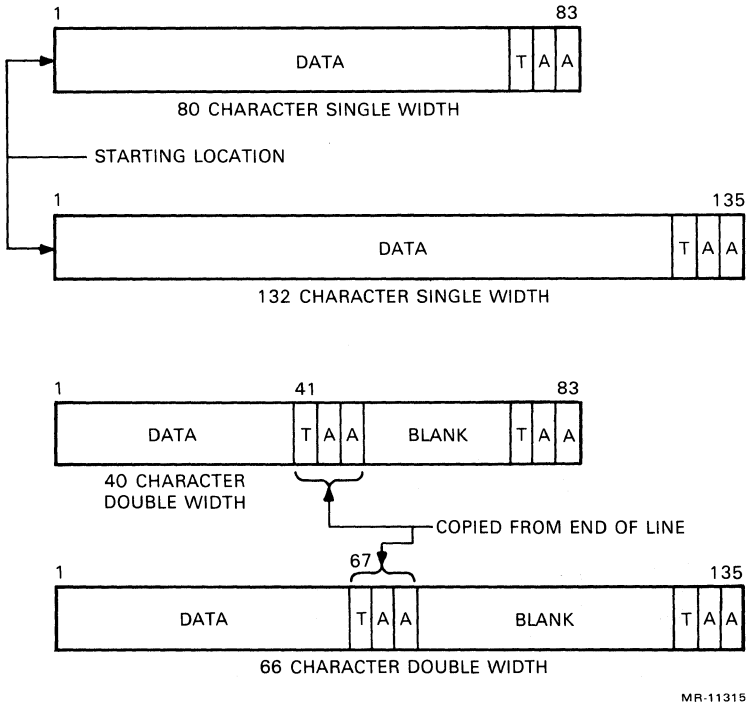


Figure 4-22 Line Organization

The first control byte FFH (Figure 4-23) is called the terminator and is a unique character that the video processor recognizes as the end of the line. The five least significant bits of the second byte and all 8 bits of the third byte are an address pointing to the first character of the next line to be displayed. The three most significant bits of the second byte define the line attributes of the line pointed to by the address.

During power-up or reset, the 8088 writes control bytes (terminator and addresses) into the screen RAM according to the specified line width (80 or 132 columns) and screen refresh rate (50 or 60 Hz). The 50/60 Hz refresh choice causes the micro-processor to arrange fill lines to place the beginning of the display in the right time slot relative to the vertical reset and blanking signals from the DC11. The line length parameter determines the location of the control bytes. For 80-column lines, the memory space is arranged in 83 byte intervals; for 132-column lines the interval is 135.

At program start, the 8088 reads the Set-Up parameters from the NVM and places them in the Set-Up area of the screen RAM. Then the processor reads the Set-Up parameters, erases the screen RAM area, and writes in the terminator and attribute/address bytes at the selected line width intervals. The address at the end of each line points to the first address location of the next line. At start-up, this is the next screen location. The end of the last line points to a fill line that points to itself. The fill line repeats until the DC11 asserts vertical reset.

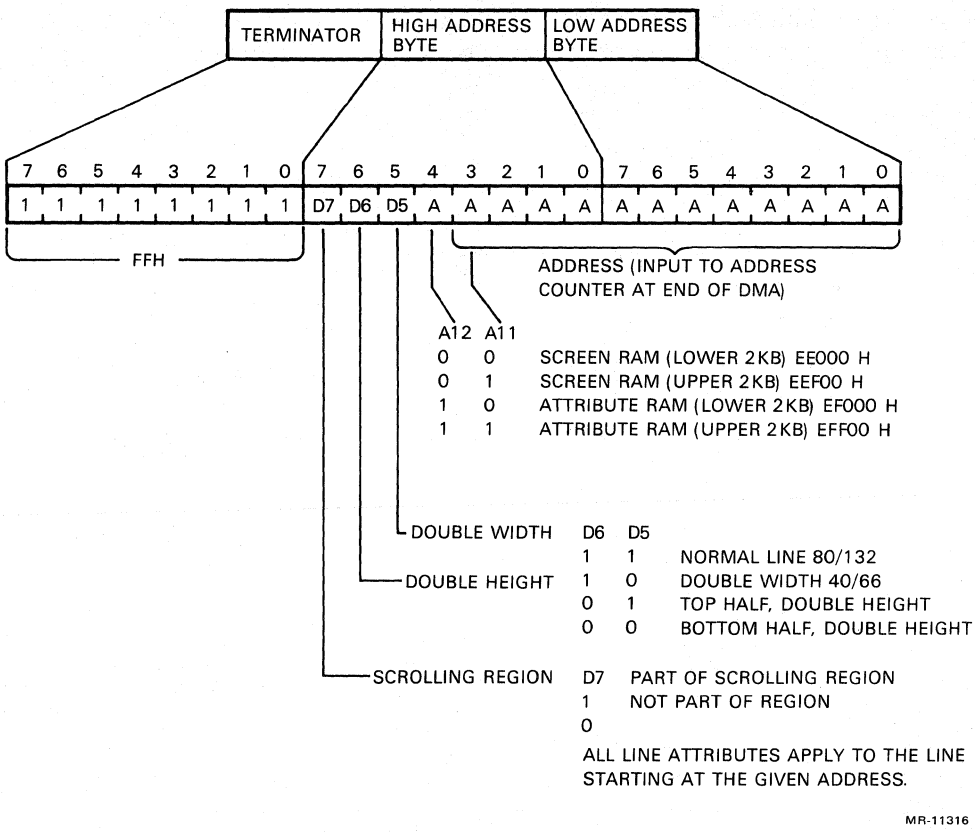


Figure 4-23 Terminator and Address Bytes

4.4.8.3 DC11 Timing Chip – The DC11 is a custom designed bipolar integrated circuit that provides most of the timing signals required by the video processor. Internal counters divide the output of the 24.0734 MHz master clock oscillator into the lower frequencies that define dot, character, scan, and frame timing. The counters are programmable through the BAD<5:4> lines to control the number of characters per line (screen width), the frequency at which the screen is refreshed (50 or 60 Hz), and whether the display is interlaced or noninterlaced (240 or 480 scans). These parameters can be controlled through Set-Up or by a host computer.

The outputs of the DC11 are various timing signals for the DC12 and other supporting logic in the video processor. The DC11 also provides the 8-bit address that is used to access the line buffer RAM during a DMA to retrieve the stored attribute and character data. These addresses sequence in a pattern that repeats exactly for each 10 scans that are required to recall each line of characters in the line buffer RAM.

4.4.8.4 DC12 Control Chip – The DC12 control chip, like the timing chip, is a custom bipolar device. It accepts control chip commands from the NVM via the BAD<3:0> bits, attributes from the line buffer RAM, and timing signals from the DC11. The DC12 delivers the low four bits ROW<3:0> of a 12-bit address for the character generator ROM and modifies the video output according to the specified character attributes (reverse video, underline, bold, and blink). It also generates a vertical interrupt (VERT INT L) signal that interrupts the 8088 processor and a hold request (HOLD REQ H) signal to initiate DMAs to get lines of data out of the screen and attribute RAMs. The vertical interrupt signal causes the 8088 to enter wait states until the video processor completes the DMA.

The DC12 performs three main functions:

1. Scan Count Generation. This logic involves two counters, a multiplexer to switch between the counters, double-height logic, scroll and line attribute latches, and various logic controlling switching between the two counters. This logic performs the major functions of the chip, which includes all scrolling, double-height logic, underline, and hold request circuits.

2. Generation of HOLD REQUEST and VERT INT. This logic uses information from the scan counters and the scrolling logic to decide when to generate HOLD REQUEST and VERT INT.

3. Video Modification. This logic provides dot stretching, blanking, additions of attributes to video outputs, and multiple intensity levels.

4.4.8.5 Video Processor Memory Addressing – The video processor accesses the screen and attribute RAMs during a DMA by generating a 12-bit address to select a particular byte in the lower 4K byte bank (character RAM) and a corresponding byte in the upper 4K byte bank (attribute RAM). The addresses are generated by the DMA address counter and applied to the screen and attribute RAMs through the shared address multiplexer. Only the low eleven bits BA<10:0> are applied to the memories. The 12th address bit BA<11> is applied to a screen/attribute selector to select either the upper or lower 2K byte bank in the attribute RAM. The low four bits LBD<11:8> of the attribute byte and all eight bits BD<7:0> of the character byte are passed to the line buffer RAM in parallel.

The video processor uses the ASCII character code as the high eight bits LINADR<7:0> of a 12-bit address to the character generator ROM. The attribute bits LBD<11:8> are used by the DC12 to modify the video data.

The video processor begins reading the screen RAM at starting address EEOOOH and the attribute RAM at starting address EFOOOH following each vertical reset by the DC11. The vertical reset signal initiates the DMA process to read one line of character and attribute data from the screen and attribute RAMs. The characters and attributes are stored in the line address buffer RAM during the first scan of a DMA and then recalled by the DC11 on each of the remaining nine scans until the next DMA.

The line organization and bit assignments of the character and attribute data stored in the screen and attribute RAMs are shown in Figures 4-24 and 4-25.

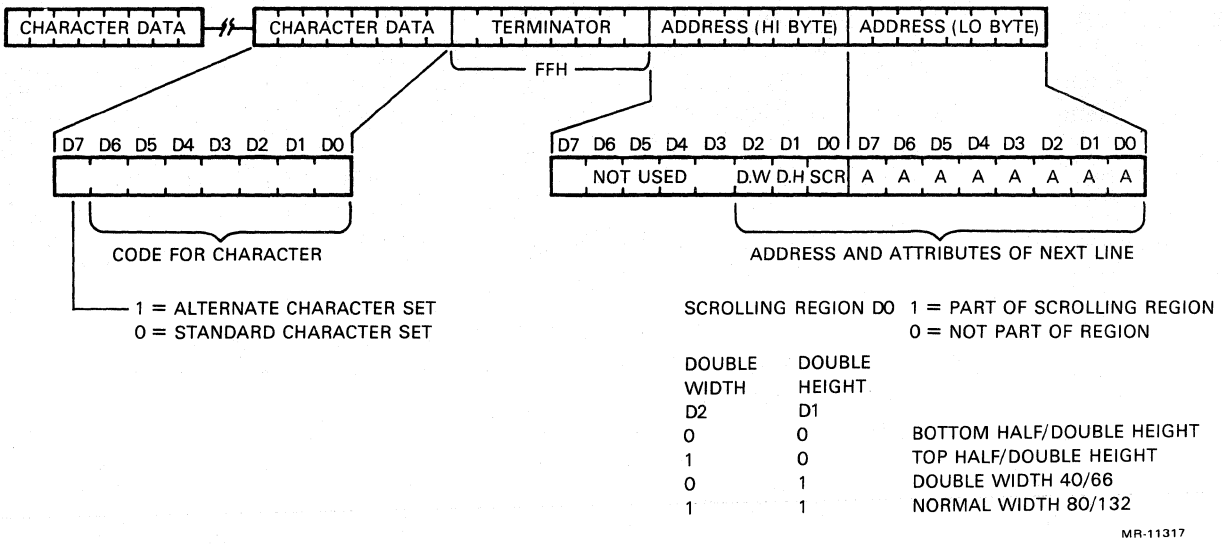


Figure 4-24 Character RAM Line Organization

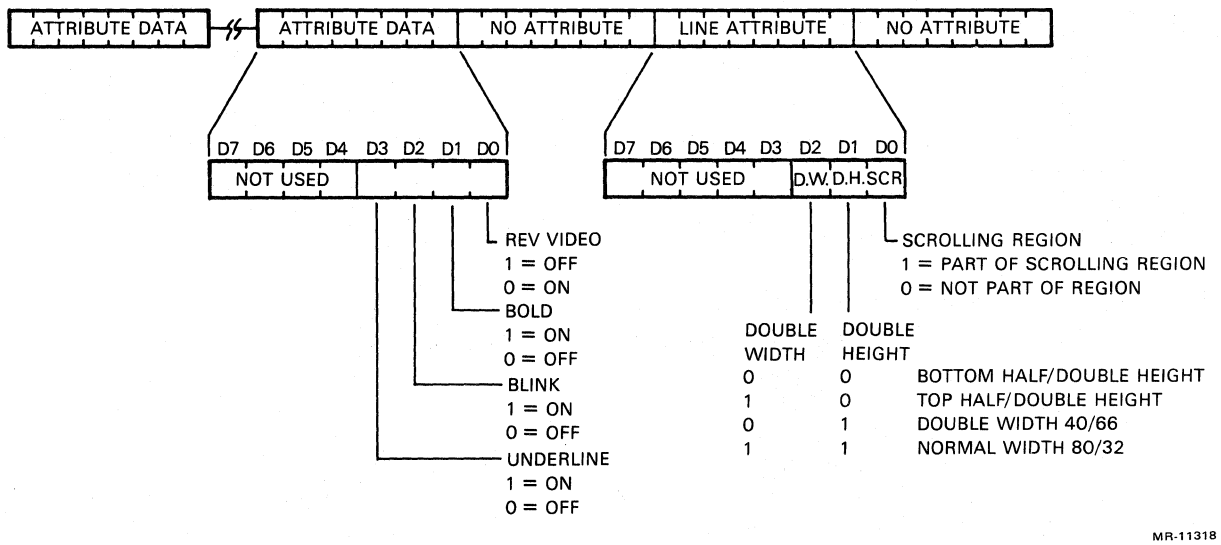


Figure 4-25 Attribute RAM Line Organization

4.4.8.6 DC11 Programming Information – The DC11 video timing chip can be accessed by the 8088 processor (write only) via the BAD<5:4> bits at I/O address 04H. The DC11 must be programmed with the desired refresh rate and column mode on power-up and after any mode changes. To program the DC11, write two of the following four command codes listed in Table 4-7.

Table 4-7 DC11 Command Codes

Code (Hexadecimal)	BAD<5>	BAD<4>	Configuration	Operation Performed
0 0	0	0	80-column mode	Sets interlaced mode
1 0	0	1	132-column mode	
2 0	1	0	60 Hz mode	Resets interlaced mode
3 0	1	1	50 Hz mode	

Interlaced/noninterlaced mode is determined by the order in which the 80/132 column and the 50/60 Hz refresh rate are set. When BAD<5> is low, the number of columns is programmed according to the state of BAD<4>. When BAD<5> is high, the refresh rate is programmed. Interlace mode is always selected when the column mode is set, and noninterlaced mode is selected when the refresh rate is set. The interlace mode that is in use depends on whether the column mode or refresh mode was selected last.

Every time the DC11 is programmed, its internal timing chain is reset. Since this causes the screen display to jump, the DC11 should be programmed only if absolutely necessary. For example, the following two instructions set the DC11 to 80 column, 60 Hz, and no interlace:

```
MOV AX,2000H
OUT DC011,AX
```

NOTE

When 80-column mode is selected, the video processor is capable of displaying 83 columns in single-width mode or 41 columns in double-width/double-height mode. When 132-column mode is selected, 137 columns can be displayed in single-width mode or 68 columns in double-width/double-height mode.

4.4.8.7 DC12 Programming Information – The DC12 video control chip can be accessed by the 8088 processor (write only) via the BAD<3:0> bits at I/O address OCH. The four-bit command codes listed in Table 4-8 are defined for the DC12.

On power-up, the DC12 can be programmed to bring it to a known state. Typically, codes 00H, 04H, 09H, 0BH, and 0DH will be programmed at power-up time.

The value to which the scroll latch is set determines which scan row the first line of a scrolling region starts on. Likewise, it determines the last scan row displayed for the last line in a scrolling region.

For example, when the latch is set to zero (the degenerate case), the first line of the scroll region starts at scan row zero (so the line is completely visible). The last line of the scrolling region terminates at scan row 9 (so this line is also completely visible).

Table 4-8 DC12 Command Codes

Code (Hexadecimal)	BAD 3	2	1	0	Result
0 0	0	0	0	0	Set scroll latch LSBs to 00
0 1	0	0	0	1	Set scroll latch LSBs to 01
0 2	0	0	1	0	Set scroll latch LSBs to 10
0 3	0	0	1	1	Set scroll latch LSBs to 11
0 4	0	1	0	0	Set scroll latch MSBs to 00
0 5	0	1	0	1	Set scroll latch MSBs to 01
0 6	0	1	1	0	Set scroll latch MSBs to 10
0 7	0	1	1	1	Set scroll latch MSBs to 11
0 8	1	0	0	0	Toggle blink flip-flop
0 9	1	0	0	1	Clear vertical frequency interrupt
0 A	1	0	1	0	Set reverse field on
0 B	1	0	1	1	Set reverse field off
0 C	1	1	0	0	Not supported
0 D	1	1	0	1	Set basic attribute to reverse video with 24 lines and set blink flip-flop off
0 E	1	1	1	0	Not supported
0 F	1	1	1	1	Set basic attribute to reverse video with 48 lines and set blink flip-flop off

When the scroll latch is nonzero, for example 5, the first line of the scrolling region starts with scan row 5 (so only the bottom half of the line is visible). The last line of the scrolling region terminates at scan row 4 (so only the top half of the line is visible).

If the scroll latch is incremented from 0 through 9 and back to 0 again once each frame, the screen appears to smooth scroll from bottom to top (assuming that line linkages and line attributes are properly handled). On the other hand, if the scroll latch is decremented from 0 to 9 then down through 0, the screen appears to smooth scroll from top to bottom (again assuming that all line linkages and line attributes are properly handled).

A scrolling region is defined as a group of lines with their scrolling attributes set, surrounded by lines whose scrolling attributes are not set. Note that the scrolling attribute for a line resides in the line pointer

information at the end of the previous line. Also, the first line on the screen (the one at RAM location 0), has its scrolling attribute reset by definition. Also note that the definition of a scrolling region does not preclude the definition of more than one scrolling region per screen, although that is of dubious value.

Whenever the scroll latch is nonzero, each scrolling region on the screen requires an extra (scrolling) line to be linked in. For example, if the scrolling region is 10 lines long when the scroll latch is set to nonzero, there must be an eleventh line linked in. If scrolling up (incrementing the scroll latch), the line must be linked in at the bottom. When the scroll latch is incremented back to 0 again, the top line of the scrolling region must be unlinked. When scrolling down (decrementing the scroll latch), new lines must be linked in at the top of the scroll region and unlinked down at the bottom. All line linking/unlinking should be done during the vertical blanking interval (after the vertical frequency interrupt is asserted). In 60 Hz mode, there are two blanked lines at the beginning of the screen: the line at RAM location 0, and the line that it points to.

The first line (at location 0) is guaranteed to have been read by the time that the interrupt service routine is entered. Any changes to this line will not affect the screen until the next frame time. The second line will not be read for over 500 microseconds after asserting the interrupt.

If the line is to be changed, it must be done very soon after entering the interrupt service routine in order to guarantee that the change will be visible in the current frame.

Therefore, if the first visible line on the screen is involved in the scroll region and is being either linked in or unlinked, then the vertical interrupt routine must guarantee that its pointer (which resides in the second invisible line) is changed within approximately 500 microseconds after the assertion of the interrupt.

The timing for setting the scroll latch is much less critical. Because the scroll latch is loaded by the DC12 by the vertical reset at the beginning of each frame, the only requirement is that the scroll latch be modified before the next frame begins. Note that the scroll latch value is the value that will be used during the next frame, rather than the current frame.

4.4.8.8 Line Buffer RAM – The line buffer RAM is a 1024 ×12-bit static RAM that stores one line of characters (including the three control bytes) during a scan on which a DMA occurs. The line buffer RAM then recalls these characters on each successive scan until the next DMA.

The DC11 provides a sequence of addresses LBA<7:0> that change at each character clock. These addresses are used to store data from the screen and attribute RAMs in a unique location in the line buffer RAM. The data is written into the line buffer RAM during the first scan of a DMA when the DC11 asserts the WR LB L signal.

The data outputs of the line buffer RAM are the four attribute bits LBD<11:8> and the line buffer data bits LBD<7:0>. The LBD<11:8> bits are applied through a latch clocked by the character clock into the attribute inputs of the DC12. The LBD<7:0> bits are applied to the line address counter, the termination detector, and the eight most significant address inputs of the character generator ROM. The LBD<3:0> bits are sent directly to the last four stages of the 12-bit line address counter. All eight LBD<7:0> bits are sent through a line address buffer clocked by the character clock into the first eight stages of the line address counter.

4.4.8.9 Line Address Counter – The line address counter is a 12-bit up counter that provides 11-bit addresses BA<10:0> to access the screen and attribute RAMs. The 12th bit BA<11> of this counter is sent to a data selector to select either the lower or upper 2K byte bank of the attribute RAM. The vertical reset signal from the DC11 clears the line address counter to zero so that the video processor begins to process from the starting locations of the screen and attribute RAMs after each vertical reset. The counter is loaded with a new address LBD<3:0> and LINADR<7:0> from the line buffer RAM at the end of each DMA when the DC11 asserts the address load ADR LD L signal. The address counter counts

forward from this address at the character clock rate, using the address count (ADR CNT H) signal from the DC11. ADR CNT H only occurs when the DC12 asserts hold request (HOLD REQ H); thus, the address counter only counts during the DMA portion of each line. The address is loaded into the address counter at the end of the DMA scan and held until the next DMA begins.

In double-width mode, the address count pulses occur half as often as in normal width. The line buffer RAM receives the normal number of WR LB L pulses, however, so each character gets copied into two adjacent locations in the line buffer RAM.

4.4.8.10 Termination Detector – The eight bits of each character address LIN ADR<7:0> go to an eight-input termination detector. The last three bytes in each line of characters stored in the screen RAM are a terminator character (FFH) and two address bytes. Only the terminator byte activates the termination detector. During the character time when the terminator byte reaches the termination detector, the first address byte is at the input of the character generator latch, and the second address byte is at the input of a screen RAM latch. On the next character clock, the termination detector output (TERM L) causes the DC12 to blank the display and end the hold request.

The address load (ADDR LD L) pulse from the DC11, timed to arrive before the next character after the terminator byte, loads the address counter and the DC12 inputs with the final two address bytes. The outputs BA<10:0> of the address counter designate the address of the first character of the next line to be displayed. The three most significant bits of the high address byte go to the DC12 and designate the line attributes of the next line to be displayed.

4.4.8.11 Character Generator ROM – The character generator is a 4 K × 8 bit ROM that is addressed by the coded representations of the desired characters stored in the screen RAM. Each code is used as the eight most significant bits of the ROM address. The four least significant bits of the ROM address are provided by a scan counter in the DC12. The eight character (LINADR<7:0> bits combine with the 4-bit scan count (ROW<3:0>) to provide the 12-bit address for the ROM. The data stored at each address (character + scan) are 8 bits representing the presence or absence of dots of light at sequential horizontal positions within that scan.

The character generator ROM holds 255 characters corresponding to character codes OOH through FEH. Character code FFH is reserved for use as the terminator byte for the termination detector. The character codes OOH through FEH correspond to address OOOH through FEFH in the character generator ROM. The final hexadecimal digit of an address indicates the scan (ROW<3:0>) of the character being addressed. Table 4-9 lists the relation of the scan address digit to the scan number.

Table 4-9 Character Generator Scan Addresses

Scan Address	Character Scan Number	
F	1	Normally blank
0	2	Top of normal upper case character
1	3	
2	4	
3	5	
4	6	
5	7	
6	8	Bottom of normal upper case character
7	9	Normal descenders (underline scan)
8	10	Normal descenders
9-E		Not used (never displayed)

Each byte of information in the character generator ROM at a valid scan address represents 8 bits of horizontal scan information. Figure 4-26 shows the bit patterns stored in the ROM for an uppercase and lowercase letter A. The characters are displayed on the screen in a 10 × 10 matrix of dots. Each 10 dot × 10 scan group is a character cell, where each character can be displayed.

The low order bit (DO) is a fill bit; it is used not only as the rightmost bit in the character, but also fills in the right-hand space between characters. This intercharacter space is two dot intervals in 80-column mode, and one dot interval in 132-column mode.

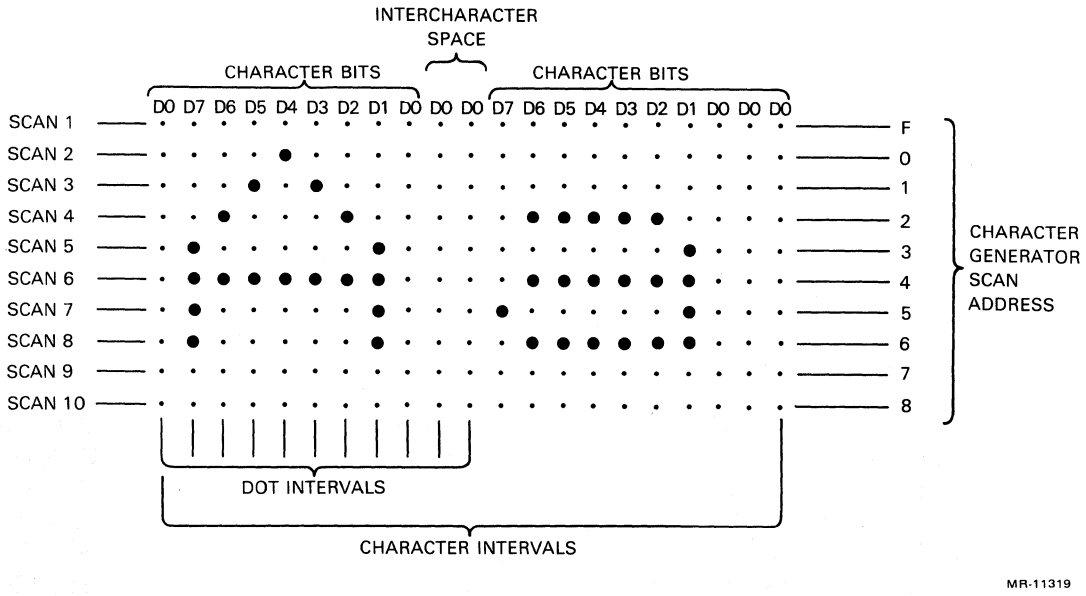


Figure 4-26 Character Generator ROM Patterns

4.4.8.12 Video Shift Register – The video shift register converts the parallel character data bits from the character generator into serial video data that is applied to the DC12 video control chip. The seven most significant bits (D<7:1>) are latched into the video shift register and the least significant bit (D<0>) is latched into a flip-flop when the DC11 asserts the video shift register load (VSR LD L) signal. At the same time, the last bit shifted out during the previous character time is latched into the input of the video shift register. The video shift register is continuously clocked by the dot clock (DOT CLK H) signal from the DC11. The first bit shifted out in the new character time is the same value as the last bit of the previous character, providing horizontal continuity from one character cell to the next. The seven new data bits are then shifted into the serial video input of the DC12.

Meanwhile, the flip-flop that stored the D<0> bit has delivered that bit to the serial input of the video shift register. This bit was shifted into each successive register position as the first eight bits were shifted out. Now the shifting continues, for one more bit for 132-column mode and two more bits for 80-column mode, causing the last bits shifted out to be the value that was stored in the flip-flop.

VSR LD H then latches the next character into the video shift register and flip-flop with that last multiply-shifted bit in the first position. In this way, the least significant bit (D<0>) defines the two or three dots between characters, and the seven most significant bits define the character.

At the end of the scan, the horizontal blanking (HOR BLANK H) signal from the DC11 forces the flip-flop output low. Since horizontal blanking lasts more than one character time, the low level will be shifted to the first position in the video shift register before the start of the next line. This ensures that the first dot on the next scan will be at the screen background level.

4.4.8.13 Video Generator – The video generator uses four signals from the DC12 to produce a composite video signal consisting of vertical blanking pulses, horizontal and vertical synchronizing pulses, and video. There are different levels of illumination within the video signal ranging from totally black through maximum brightness.

The four signals from the DC12 are the composite sync (COMP SYNC L), vertical blanking (VERT BLANK L), video out 1 (VID OUT 1 H), and video out 2 (VID OUT 2 H). These signals are applied to three open collector NAND gates wire-ANDed and applied to the base of a transistor. The output of the transistor is the 75 ohm composite video signal consisting of four intensity levels, and the composite synchronizing pulses. This signal is connected to connector J3 and can directly drive a standard video monitor. The output is dc coupled. Although the use of dc coupling is not in strict agreement with the EIA RS-170 standard, this presents no problems with most monitors because their input is usually ac coupled. The composite video output is illustrated in Figure 9-5, Chapter 9.

4.4.8.14 Composite Video Signal Characteristics – The composite video output provides a compatible EIA RS-170 output generated by combining the video signal with a composite sync signal.

NOTE

The use of dc coupling is not in strict agreement with the EIA RS-170 standard. To agree with RS-170, the video generator output load would require a 10 microfarad capacitor in series with the output. Without the capacitor, the RS-170 2 milliamp dc short circuit requirement is violated.

The composite video output has the following nominal characteristics:

1. Output impedance = 75 ohms, dc coupled to 0.0 V
2. Sync level = 0.0 V
3. Reference black level = approximately 0.3 V with a 75 ohm load
4. Reference white level = approximately 1.0 V with a 75 ohm load
5. The composite sync waveform conforms to EIA RS-170 standards. The vertical interval is composed of six equalizing pulses, six vertical sync pulses, and six more equalizing pulses. The timing is as follows:

Equalizing pulse width	= 2.33 μs + or − 50 ns
Vertical pulse width	= 27.28 μs + or − 200 ns
Horizontal pulse width	= 4.71 μs + or − 50 ns
Horizontal blank width	= 11.84 μs + or − 50 ns/80-column mode
	= 12.34 μs + or − 50 ns/132-column mode
Front porch	= 1.54 μs + or − 50 ns

4.4.9 8088 Diagnostic and Control/Status Registers

There are two diagnostic registers, one control register, and one status register accessed by the 8088 processor. The two 8-bit diagnostic registers are used during diagnostic testing to control and read the status of various system functions. The control register is used to control the modem control lines of the communications port and to write diagnostic error codes into the four 8088 LEDs. The status register is used to read the status of the modem control lines of the communications port, the interrupt line of each processor, and the MHFU logic enable signal. The registers are shown in Figure 4-27 and described in the following paragraphs.

4.4.9.1 Diagnostic Write Register: 8088 Processor – The diagnostic write register is an 8-bit write-only register that is used for diagnostic control purposes. This register also contains a bit to loopback the transmitted data of the ports through a loopback multiplexer into the received data input of the ports. This register is accessed by performing a write to address 0AH. The register bit format is shown in Figure 4-28 and the bits are described in Tables 4-10, 4-11, 4-12, 4-13, and 4-14.

4.4.9.2 Diagnostic Read Register: 8088 Processor – The diagnostic read register is an 8-bit read-only register that is used during diagnostic testing to read the status of a number of diagnostic control signals. The register is accessed by performing a read to address 0AH. The register bit format is shown in Figure 4-29 and the bits are described in Table 4-15.

4.4.9.3 Communications Status Register: 8088 Processor – The communications status register is an 8-bit read-only register that stores the status of the modem control lines for the communications port, the interrupt line for each processor, and the MHFU enable signal. This register is accessed by performing a read to address 02H. The register bit format is shown in Figure 4-30 and the bits are described in Table 4-16.

4.4.9.4 Communications Control Register: 8088 Processor – The communications control register is an 8-bit write-only register that controls the modem lines on the communications port and writes diagnostic error codes into the four 8088 LEDs. This register is accessed by performing a write to address 02H. The register bit format is shown in Figure 4-31 and the bits are described in Table 4-17.

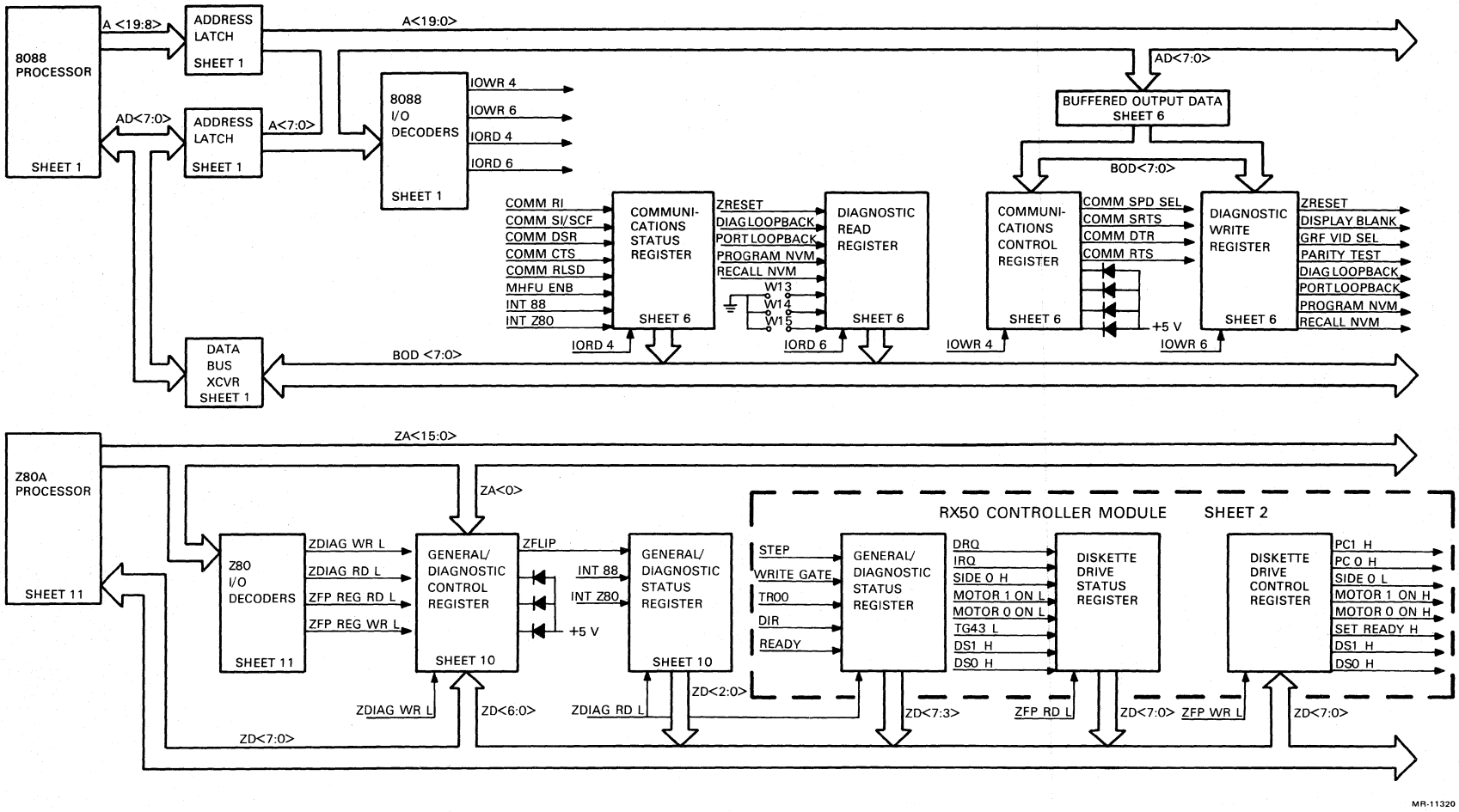


Figure 4-27 System Module Control, Status, and Diagnostic Registers

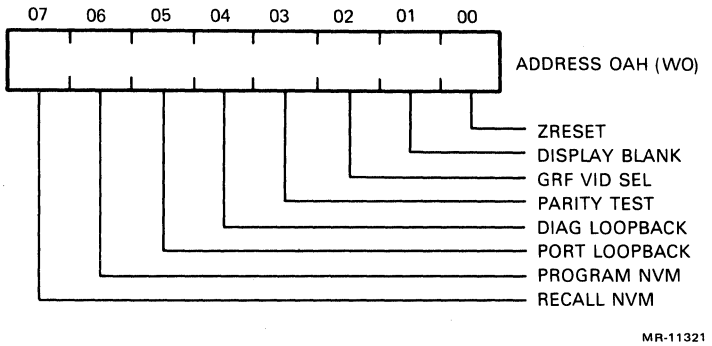


Figure 4-28 Diagnostic Write Register (8088) Format

Table 4-10 Diagnostic Write Register (8088) Bit Description

Bit	Name	Description
0	ZRESET	When this bit is high (1), it resets the Z80A processor from the 8088 processor side. This bit is active at power-up.
1	DISPLAY BLANK	When this bit is low (0), the display will be blanked.
2	GRF VID SEL	When this bit is low (0), the system module video is selected. When high (1), the graphics module video is selected.
3	PARITY TEST	When high (1), this bit enables testing of the parity circuit on the optional memory module.
4	DIAG LOOPBACK	This bit is a maintenance bit that is cleared (0) on power-up. When high(1), this bit allows the RX50 controller data separator and the serial video output from the DC12 to be tested through the use of the printer port. Tables 4-11 and 4-12 describe how the signals are routed through the printer port.
5	PORT LOOPBACK	This bit is a communications port loopback maintenance bit. This bit is cleared (0) on power-up. When high (1), this bit sets up the loopback multiplexers for the communications, printer, and keyboard ports to allow testing. The port loopbacks are done in such a way that bit rate errors of one port can be detected by another. Tables 4-13 and 4-14 describe how the signals are routed through the ports.
6	PROGRAM NVM	When high (1), this bit allows data to be written into the NVM.
7	RECALL NVM	When high (1), this bit allows data to be recalled (read) from the NVM.

Table 4-11 Printer Port Diagnostic Signal Routing*

Diagnostic Loopback Bit 4 =	Signal Source From	Signal Input To
0	PRT RCV DATA	PRT RXD
1	VIDEO OUT 2	PRT RXD
0	PRT RXTXC	PRT RXTXC
1	500 KHZ	PRT RXTXC
0	MASTER CLK	VIDEO CLK
1	250 KHZ	VIDEO CLK
0	RAW DATA	DATA SEPARATOR
1	PRT TXD	DATA SEPARATOR

* During diagnostic loopback, the TEST input of the 8088 is connected to the COMM/PRINTER INTR L output of the multiprotocol serial controller (MPSC). Thus, using the 8088 processor's wait instruction in a polled I/O loop, the diagnostic firmware is able to keep up with the 500K baud data rate of the MPSC.

Table 4-12 Printer Port Diagnostic Signal Description

Direction	Signal Source	Description
From	PRT RCV DATA	Data received from the printer through connector J2.
From	VIDEO OUT 2	DC12 serial video output data to the printer port during diagnostic loopback testing.
To	PRT RXD	Printer received data input to the MPSC from the printer or DC12 serial video.
From	PRT RXTXC	Printer receiver/transmitter clock input to the MPSC from the printer baud rate generator.
From	500 KHZ	Printer receiver/transmitter clock input to the MPSC during diagnostic loopback testing.
To	PRT RXTXC	Printer receiver/transmitter clock input to MPSC from printer baud rate generator or 500 kHz pulses from the clock circuit.
From	MASTER CLK	Master clock pulse input to the video loopback multiplexer.
From	250 KHZ	250 kHz clock pulse input to the video loopback multiplexer.

Table 4-12 Printer Port Diagnostic Signal Description (Cont)

Direction	Signal Source	Description
To	VIDEO CLK	Video clock input to the DC11 from the master clock or 250 kHz outputs of the clock circuit.
From	RAW DATA	Raw data (clocks and data) from the disk drives.
From	PRT TXD	Data transmitted from the MPSC to the printer, the keyboard loopback multiplexer, and the diskette drive data separator.
To	DATA SEPARATOR	Data input to data separator from the diskette drives, or printer transmitted data from the MPSC.

Table 4-13 Port Loopback Signal Routing

Port Loopback Bit 5 =	Signal Source From	Signal Input To
0	COMM RCV DATA	COMM RXD
1	COMM TXD	COMM RXD
0	PRT RCV DATA	PRT RXD
1	KBD TXD	PRT RXD
0	KBD RCV DATA	KBD RXD
1	PRT TXD	KBD RXD

Table 4-14 Port Loopback Signal Description

Direction	Signal Source	Description
From	COMM RCV DATA	Communications received data from the communications connector J1 applied to the communications loopback multiplexer.
From	COMM TXD	Communications transmitted data from the MPSC applied to the communications loopback multiplexer.
To	COMM RXD	Communications received data input to the MPSC from the communications device or communications transmitted data from the MPSC during port loopback testing.
From	PRT RCV DATA	Printer received data from printer connector J2 applied to printer loopback multiplexer.
From	KBD TXD	Keyboard transmitted data from the keyboard PUSART to the printer loopback multiplexer via the video loopback multiplexer.
To	PRT RXD	Printer received data input to the MPSC from the printer, or the keyboard transmitted data during port loopback testing.
From	KBD RCV DATA	Keyboard received data from the keyboard connector J3 to the keyboard loopback multiplexer.
From	PRT TXD	Printer transmitted data from the MPSC to the keyboard loopback multiplexer.
To	KBD RXD	Keyboard received data input to the keyboard PUSART from the keyboard connector or the printer transmitted data during port loopback testing.

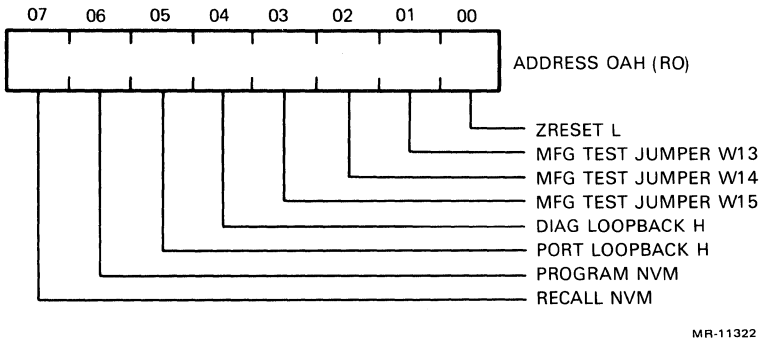


Figure 4-29 Diagnostic Read Register (8088) Format

Table 4-15 Diagnostic Read Register (8088) Bit Description

Bit	Name	Description
0	ZRESET L	This bit represents the state of bit 0 of the 8088 diagnostic write register.
1–3	MFG TEST JUMPER	These bits represent the state of the W13, W14, and W15 manufacturing test jumpers. These bits are normally high (1).
4	DIAG LOOPBACK H	This bit represents the state of bit 4 of the 8088 diagnostic write register (diagnostic loopback H).
5	PORT LOOPBACK H	This bit represents the state of bit 5 of the 8088 diagnostic write register (port loopback H).
6	PROGRAM NVM	This bit represents the state of bit 6 of the 8088 diagnostic write register (program NVM).
7	RECALL NVM	This bit represents the state of bit 7 of the 8088 diagnostic write register (recall NVM).

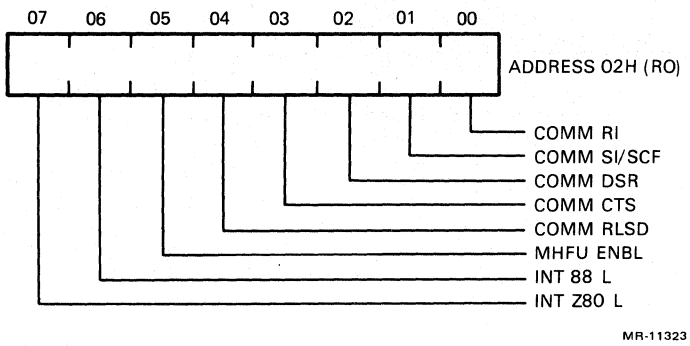


Figure 4-30 Communications Status Register (8088) Format

Table 4-16 Communications Status Register (8088) Bit Description

Bit	Name	Description
0	COMM RI	This bit reflects the status of the ring indicator line of the communications port.
1	COMM SI/SCF	This bit reflects the status of the speed indicator line or the secondary receive line signal detect of the communications port.
2	COMM DSR	This bit reflects the status of the data set ready line of the communications port.
3	COMM CTS	This bit reflects the status of the clear to send line of the communications port.
4	COMM RLSD	This bit reflects the status of the receive line signal detect of the communications port.
5	MHFU ENB L	This bit reflects the status of MHFU enable L.
6	INT88 L	This bit reflects the status of the INT88 L bit that is asserted by the Z80A to interrupt the 8088.
7	INTZ80 L	This bit reflects the status of the INTZ80A L bit that is asserted by the 8088 to interrupt the Z80A.

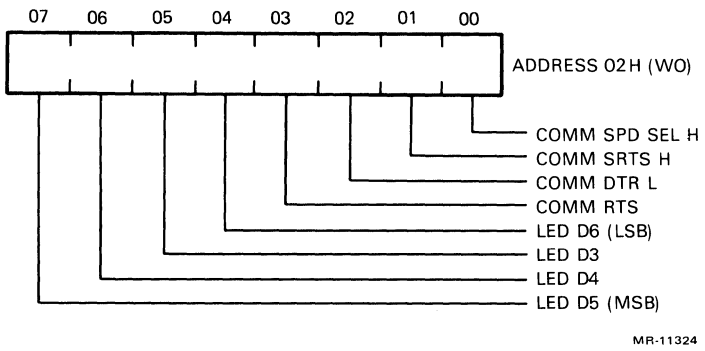


Figure 4-31 Communications Control Register (8088) Format

Table 4-17 Communications Control Register (8088) Bit Description

Bit	Name	Description
0	COMM SPD SEL H	This bit controls the speed select line of the communications port.
1	COMM SRTS H	This bit controls the secondary request to send line of the communications port.
2	COMM DTR L	This bit controls the data terminal ready line of the communications port.
3	COMM RTS	This bit controls the request to send line of the communications port.
4	LED (D6)	This bit displays the least significant bit of the diagnostic error message code. When written with a 0, the LED lights.
5	LED (03)	This bit displays the second bit of the diagnostic error message code. When written with a 0, the LED lights.
6	LED (D4)	This bit displays the third bit of the diagnostic error message code. When written with a 0, the LED lights.
7	LED (D5)	This bit displays the most significant bit of the diagnostic error message code. When written with a 0, the LED lights.

4.4.10 Z80A Registers

The Z80A processor can access registers on the system module and the RX50 controller module to control and monitor the status of the diskette drives and a number of other functions for diagnostic and general purposes. These registers are shown in Figure 4-27 and described in the following paragraphs.

The registers that the Z80A can access are as follows:

- General/diagnostic status register
- General/diagnostic control register
- Diskette drive status register
- Diskette drive control register

The Z80A can access five other diskette drive registers that are located in the floppy disk controller (FDC) chip on the RX50 controller module. These registers are listed here for reference only and are described in detail in Chapter 5.

- FDC status register
- FDC control register
- FDC track register
- FDC sector register
- FDC data register

4.4.10.1 General/Diagnostic Status Register: Z80A Processor – The general/diagnostic status register is an 8-bit read-only register that holds the status of interprocessor interrupts, ZFLIP, and diskette drive control signals. The three least significant bits of this register are located on the system module, and the five most significant bits are located on the RX50 controller module. This register is accessed by performing a read to address 21H. The register bit format is shown in Figure 4-32 and the bits are described in Table 4-18.

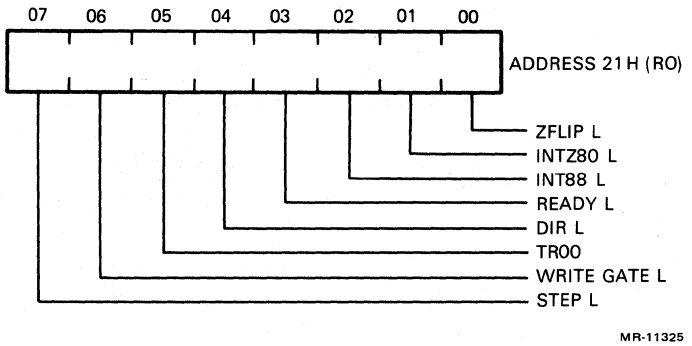


Figure 4-32 General/Diagnostic Status Register (Z80A) Format

Table 4-18 General/Diagnostic Status Register (Z80A) Bit Description

Bit	Name	Description
0	ZFLIP L	This bit is the read back for the ZFLIP L bit in the general/diagnostic control register (Z80A).
1	INTZ80 L	This bit reads the INTZ80 bit that is sent by the 8088 to interrupt the Z80A.
2	INT88 L	This bit reads the INT88 bit that is sent by the Z80A to interrupt the 8088.
3	READY L	This bit reflects the status of the READY L signal coming from the diskette drive.
4	DIR L	This bit reflects the status of the DIRECTION signal from the FDC chip going to the diskette drive. This bit is used to control the step direction (in or out) of the read/write heads in the diskette drive.
5	TR00	This bit reflects the status of the TRACK 0 signal coming from the diskette drive. When high (1), the heads are on the track 0 position.
6	WRITE GATE L	This bit reflects the status of the WRITE GATE signal from the FDC chip. Used to gate write data to the diskette drive.
7	STEP L	This bit reflects the status of the STEP signal from the FDC chip that is used to step the diskette drive read/write heads in or out.

4.4.10.2 General/Diagnostic Control Register: Z80A Processor – The general/diagnostic control register is an 8-bit write-only register that holds the bit (ZFLIP) that determines whether the Z80A address bit Z<15> is inverted and three bits of Z80A diagnostic LED information. Only the four most significant bits of this register are used. This register can be accessed by performing a write to address 20H or 21H. The register bit format is shown in Figure 4-33 and the bits are described in Table 4-19.

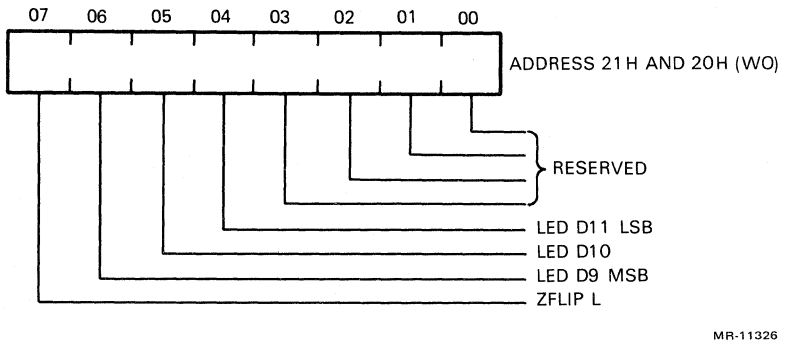


Figure 4-33 General/Diagnostic Control Register (Z80A) Format

Table 4-19 General/Diagnostic Control Register (Z80A) Bit Description

Bit	Name	Description
0–3		These bits are reserved for future use.
4	LED D11	This bit displays the least significant bit of the diagnostic error message code. When written with a 0, the LED lights.
5	LED D10	This bit displays the second bit of the diagnostic error message code. When written with a 0, the LED lights.
6	LED D9	This bit displays the most significant bit of the diagnostic error message code. When written with a 0, the LED lights.
7	ZFLIP L	Z80A address bit A<0> is the input for bit 7 of this register. When A<0>, address line A<15> of the Z80A is inverted. In this case, ZFLIP is low and the 2K byte unshared RAM appears at address 8000H instead of 0000H. ZFLIP is low whenever the Z80A is reset. It can be set high by writing to the register at address 21H. It is reset by writing to address 20H.

4.4.10.3 Diskette Drive Status Register: Z80A Processor – The diskette drive status register is an 8-bit read-only register that holds the status of diskette drive lines coming from the RX50 controller module and going to the diskette drives. Three of the diskette drive status signals come from the FDC chip, and the remaining five come from the diskette drive control register. The diskette drive status register is located on the RX50 controller module and can be accessed by a read to address 40H. The register bit format is shown in Figure 4-34 and the bits are described in Table 4-20.

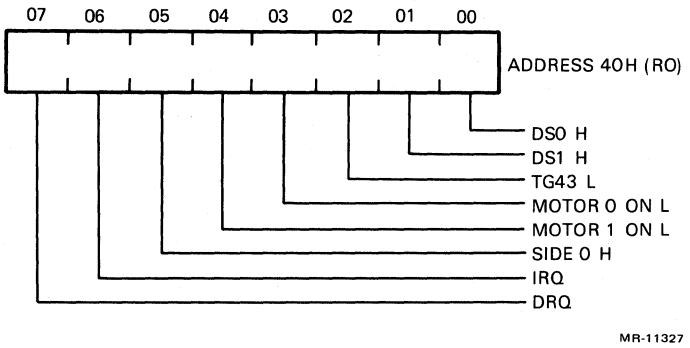


Figure 4-34 Diskette Drive Status Register (Z80A) Format

Table 4-20 Diskette Drive Status Register (Z80A) Bit Description

Bit	Name	Description
0–1	DS0–DS1	These bits reflect the status of bits 0 and 1 from the diskette drive control register. They indicate which drives have been selected.
2	TG43 L	This bit reflects the status of the TRACK GREATER THAN 43 signal sent from the FDC chip to the diskette drive.
3	MOTOR 0 ON L	This bit reflects the status of the MOTOR 0 ON line at connector J2 of the RX50 controller module. When low (0), this bit indicates that the MOTOR 0 ON bit is set in the diskette drive control register.
4	MOTOR 1 ON L	This bit reflects the status of the MOTOR 1 ON line at connector J3 of the RX50 controller module. When low (0), this bit indicates that the MOTOR 1 ON bit is set in the diskette drive control register.
5	SIDE 0 H	This bit reflects the status of the SIDE select signal at connectors J2 and J3 of the RX50 controller module. For single-sided drives, this bit will always read low (0).
6	IRQ	This bit reflects the status of the INTERRUPT REQUEST signal coming from the FDC chip. It indicates that a status bit has changed.
7	DRQ	This bit reflects the status of the DATA REQUEST signal from the FDC chip. It indicates that the FDC chip has read data to be transferred or requires new write data.

4.4.10.4 Diskette Drive Control Register: Z80A Processor – The diskette drive control register is an 8-bit write-only register that holds the write data precompensation select signals (PC0,PC1), drive select signals (MOTOR ON 0 L and MOTOR ON 1 L), a diagnostic override bit (SET READY H), and a diskette side select signal (SIDE 0 L).

The drive motor on signals, drive select signals, and the diskette side select signal are sent to the diskette drives and the diskette drive status register. The write data precompensation select signals provide two of the address inputs for a write data precompensation ROM. The diagnostic override bit enables the FDC chip to perform a read or write operation.

The diskette drive control register can be accessed by a write to address 40H. The register bit format is shown in Figure 4-35 and the bits are described in Tables 4-21 and 4-22.

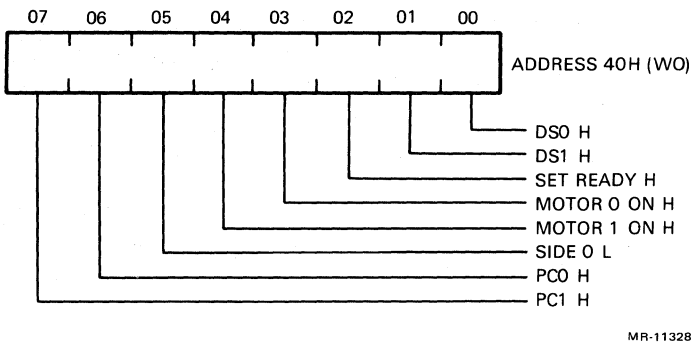


Figure 4-35 Diskette Drive Control Register (Z80A) Format

Table 4-21 Diskette Drive Control Register (Z80A) Bit Description

Bit	Name	Description
0–1	DS0–DS1	These bits control the selection of the diskette drives. The binary values (0–3) written in these bits select drives 0 through 3. Only one drive can be selected at any given time.
2	SET READY H	This bit is the diagnostic READY override bit. When set (1), this bit asserts DRIVE READY to the FDC chip.
3	MOTOR 0 ON H	When high (1), this bit turns on the motor in the first drive unit. (drives A and B)
4	MOTOR 1 ON H	When high (1), this bit turns on the motor in the second drive unit. (drives C and D)
5	SIDE 0 L	This bit selects the side of the diskette to be accessed. For single-sided drives, this bit is always set to 0 for side 0.
6–7	PC0–PC1	These binary bits are used to specify the write data precompensation values. Table 4-22 lists the precompensation values for all 80 tracks on the diskette.

Table 4-22 Write Data Precompensation Codes

	Precompensation		Track
TG43*	PC1	PC0	Number
0	0	0	0–9
0	0	0	10–19
0	0	0	20–29
0	0	0	30–39
1	0	0	40–49
1	0	0	50–60
1	0	1	61–69
1	0	1	70–79

* 0 = write operation to outer tracks (0–43); 1 = write operation to inner tracks (44–79)

4.4.11 MPSC General Description

The 7201 multiprotocol serial controller (MPSC) is a 40-pin dual-in-line microcomputer peripheral device that supports asynchronous (start/stop), byte synchronous (monosync, IBM bisync), and bit synchronous (ISOs, HDLC, SDLC) protocols. The serial controller's flexible architecture allows easy implementation of many variations of these three protocols with low software and hardware overhead.

The MPSC has the following features:

- Asynchronous, byte synchronous, and bit synchronous operation
- Two independent full-duplex transmitters and receivers
- Baud rate: 50 to 19200 baud
- Asynchronous
    - 5–8 bits per character
    - Odd, even, or no parity
    - 1 or 2 stop bits
    - Error detection: framing, overrun, and parity
- Byte synchronous
    - Character synchronization: internal or external
    - One- or two-sync characters
    - Automatic CRC generation and checking (CRC-16)
    - IBM bisync compatible
- Bit synchronous
    - HDLC/SDLC flag generation and recognition
    - 8 bit address recognition
    - Automatic zero bit insertion and deletion
    - Automatic CRC generation and checking (CCITT-16)
    - CCITT X.25 compatible
- Polled and interrupt driven modes

The MPSC contains two independent serial receiver/transmitter channels. One receiver/transmitter channel is used by the Rainbow 100 computer for communications with a host computer (either directly or through a modem), and the other channel is used to interface to a printer through the printer connector. Each channel consists of a transmitter, receiver, and a set of read/write registers that are used to initialize and control the device.

The MPSC as implemented on the system module supports two processor data transfer modes: polled and interrupt driven. In the polled mode of operation, the 8088 processor periodically reads (polls) an MPSC status register to determine when a character has been received, when a character is needed for transmission, and when transmission errors are detected. In the interrupt-driven mode, the MPSC interrupts the 8088 when a character has been received, when a character is needed for transmission, and when transmission errors are detected.

The block diagram of the MPSC is shown in Figure 4-36 and the MPSC pin functions are described in Table 4-23.

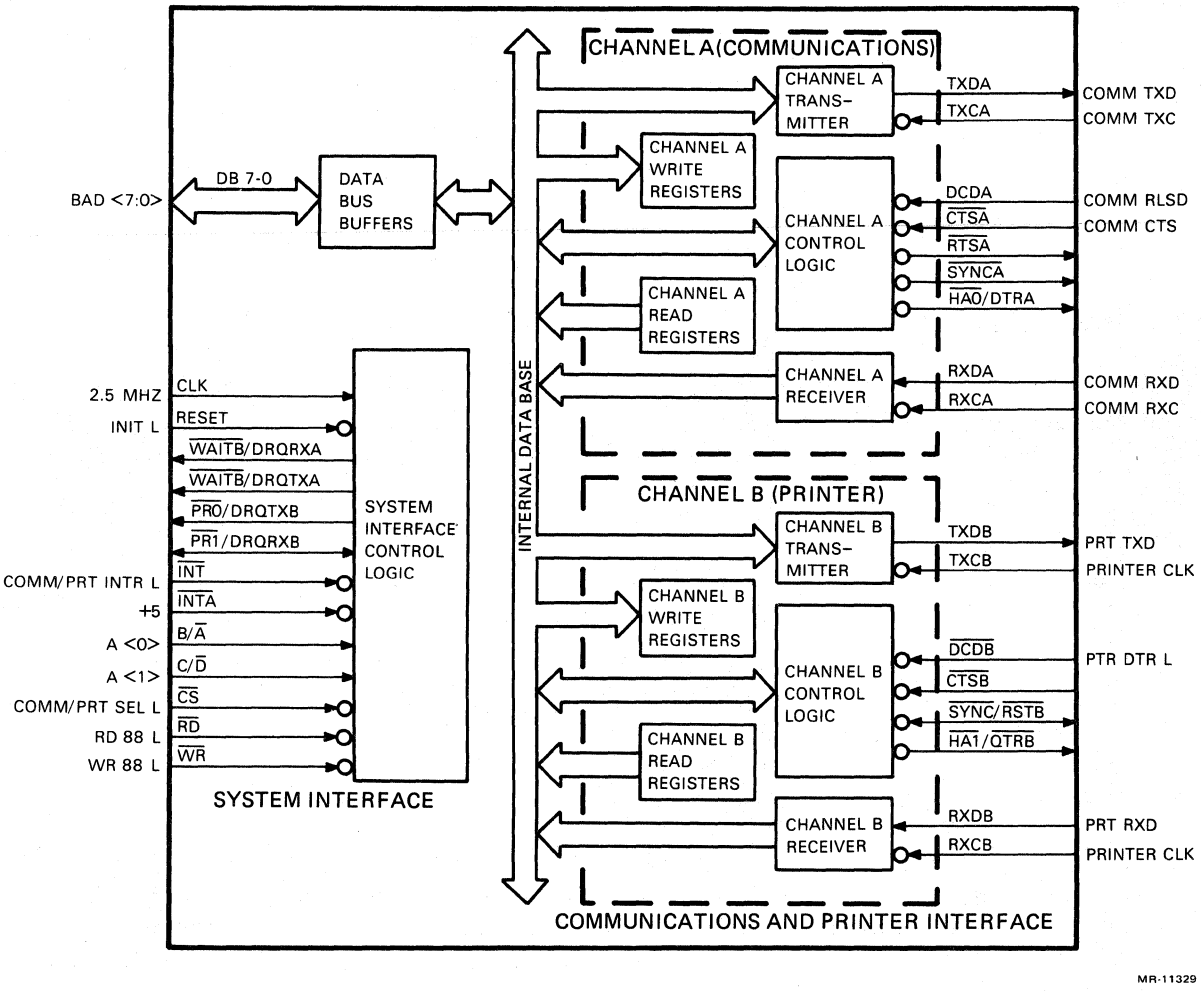


Figure 4-36 Multiprotocol Serial Controller Block Diagram

Table 4-23 MPSC Pin Descriptions

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
1	2.5 MHZ	CLK	I	CLOCK INPUT: 2.5 MHz clock pulse input to the MPSC.
2	INIT L	RESET	I	INITIALIZE: During power-up, this signal is low (0). The low signal forces the MPSC to an idle state. The COMM TXD and PRT TXD outputs are forced high. The modem interface signals are also forced high. The MPSC will remain idle until the control registers are initialized. INIT L must be low for one complete clock cycle.
3	COMM RLSD	DCDA	I	CARRIER DETECT (channel A): This signal indicates that line transmission has started. The MPSC will begin to sample data on the COMM RXD line if modem enables are selected.
4	PRINTER CLK	RXCB	I	PRINTER RECEIVER CLOCK: This signal clocks data (PRT RXD) from the printer into the channel B receiver at the baud rate programmed into the printer baud rate generator.
5		DCDB	I	CARRIER DETECT (channel B): This pin is not used in the Rainbow 100 computer.
6	PTR DTR L	CTSB	I	CLEAR TO SEND (channel B): This signal indicates that the printer is ready to accept data from the channel B transmitter.
7	PRINTER CLK	TXCB	I	PRINTER TRANSMITTER CLOCK (channel B): This signal clocks data (PRT TXD) from the channel B transmitter to the printer at the baud rate programmed into the baud rate generator.
8	PRT TXD	TXDB	O	PRINTER TRANSMIT DATA (channel B): This signal is the serial data transmitted to the printer.
9	PRT RXD	RXDB	I	PRINTER RECEIVE DATA (channel B): This signal is the input from the printer.

*O = Output, I = Input, I/O = Input/Output

Table 4-23 MPSC Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
10		SYNC/RSTB	I/O	SYNCHRONOUS DETECTION (channel B): This pin is not used in the Rainbow 100 computer.
11		WAIT B/DRQTXA	I/O	WAIT/DMA REQUEST (channel B): This pin is not used in the Rainbow 100 computer.
12–19	BAD<7:0>	D7–D0	I/O	DATA BUS: This bus transfers data, control, command, and status information between the 8088 and the MPSC. BAD<0> is the least significant bit.
20	GND	GND		GROUND.
21	WR88 L	WR	I	WRITE 8088: This signal is negated low (0) to transfer data or commands from the 8088 to the MPSC.
22	RD88 L	RD	I	READ 8088: This signal, when low (0), indicates an I/O read operation is in progress. It is used with A<1>, A<0> and COMM/PRT SEL L to transfer data from the MPSC to the 8088.
23	COMM/PRT SEL L	CS	I	COMMUNICATIONS/PRINTER SELECT: This signal, when low (0), enables the MPSC to accept command or data inputs from the 8088 during a write cycle, or to transmit data to the 8088 during a read cycle.
24	A<1>	C/D	I	CONTROL OR DATA SELECT: This address bit defines the type of information transfer performed between the 8088 and the MPSC. A high (1) during a processor write to or read from the MPSC indicates that the data on the BAD<7:0> bus is a command for the channel selected by address bit A<0>. A low (0) indicates a data transfer.
25	A<0>	B/A	I	CHANNEL A or B SELECT: This address bit selects channel A or B during a data transfer between the 8088 and the MPSC. When this address bit is high (1), channel B is selected.

*O = Output, I = Input, I/O = Input/Output

Table 4-23 MPSC Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
26		HAI/DTRB	I	DMA ACKNOWLEDGE: This pin is not used by the Rainbow 100 computer.
27	+5 V	INTA	I	INTERRUPT ACKNOWLEDGE INPUT: When low (0), this signal allows the highest priority interrupting device to generate an interrupt vector. This signal is tied to +5 V in the Rainbow 100 computer.
28	COMM/PRT INTR L		O	COMMUNICATIONS/PRINTER INTERRUPT REQUEST: When low (0), this signal informs the interrupt logic that the MPSC requires service from the 8088.
29		PRI/DRQRXB	I	INTERRUPT PRIORITY IN: This pin is not used in the Rainbow 100 computer.
30		PRO/DRQTXB	O	INTERRUPT PRIORITY OUT: This pin is not used in the Rainbow 100 computer.
31		HAO/DTRA	O	DMA ACKNOWLEDGE: This pin is not used in the Rainbow 100 computer.
32		WAIT A/DRQRXA	I/O	WAIT/DMA REQUEST (channel A): This pin is not used in the Rainbow 100 computer.
33		SYNCA	I/O	SYNCHRONOUS DETECTION (channel A): This pin is not used in the Rainbow 100 computer.
34	COMM RXD	RXDA	I	COMMUNICATIONS RECEIVE DATA (channel A): This signal is the serial data input from the communications device.
35	COMM RXC	RXCA	I	COMMUNICATIONS RECEIVER CLOCK (channel A): This signal clocks data (COMM RXD) from the communications device into the channel A receiver at the baud rate programmed into the communications baud rate generator.

*O = Output, I = Input, I/O = Input/Output

Table 4-23 MPSC Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
36	COMM TXC	TXCA	I	COMMUNICATIONS TRANSMITTER CLOCK (channel A): This signal clocks data (COMM TXD) from the channel A transmitter to the communications device at the baud rate programmed into the communications baud rate generator.
37	COMM TXD	TXDA	O	COMMUNICATIONS TRANSMIT DATA (channel A): This signal is the serial data transmitted to the communications device.
38		RTSA	O	REQUEST TO SEND (channel A): This signal is not used in the Rainbow 100 computer.
39	COMM CTS	CTSA	I	COMMUNICATIONS CLEAR TO SEND (channel A): When low (0), this signal indicates that the modem is ready to accept data from the channel A transmitter.
40	+5 V	VCC		POWER: +5 V Supply

*O = Output, I = Input, I/O = Input/Output

The MPSC interfaces to the 8088 processor over the BAD<7:0> bus. The system interface control logic in the MPSC uses the A<1:0>, COMM/PTR SEL L, RD88 L, and WR88 L input signals from the 8088 to communicate with the internal registers of the MPSC. Each serial I/O channel responds to two I/O addresses. Table 4-24 lists the operations performed by the MPSC for the various combinations of address bits A<1:0> and control signals.

Table 4-24 MPSC Register Addressing

COMM/PTR SEL L	A<1>	A<0>	READ OPERATION RD88 L	WRITE OPERATION WR88 L
0	0	0	Ch. A Data Read	Ch. A Data Write
0	1	0	Ch. A Status Read	Ch. A Command/Parameter
1	0	1	Ch. B Data Read	Ch. B Data Write
1	1	1	Ch. B Status Read	Ch. B Command/Parameter
1	X	X	High Impedance	High Impedance

Command, parameter, and status information is stored in 22 registers within the MPSC (8 write-only registers and 3 read-only registers for each channel). These registers are all accessed by means of the command/status ports for each channel. An internal pointer register selects which of the command or status registers will be written or read during a command/status access of an MPSC channel. The block diagram in Figure 4-37 shows the command/status register architecture for each serial channel. In the following discussion, the writable registers are referred to as WR0 through WR7 and the readable registers as RR0 through RR2.

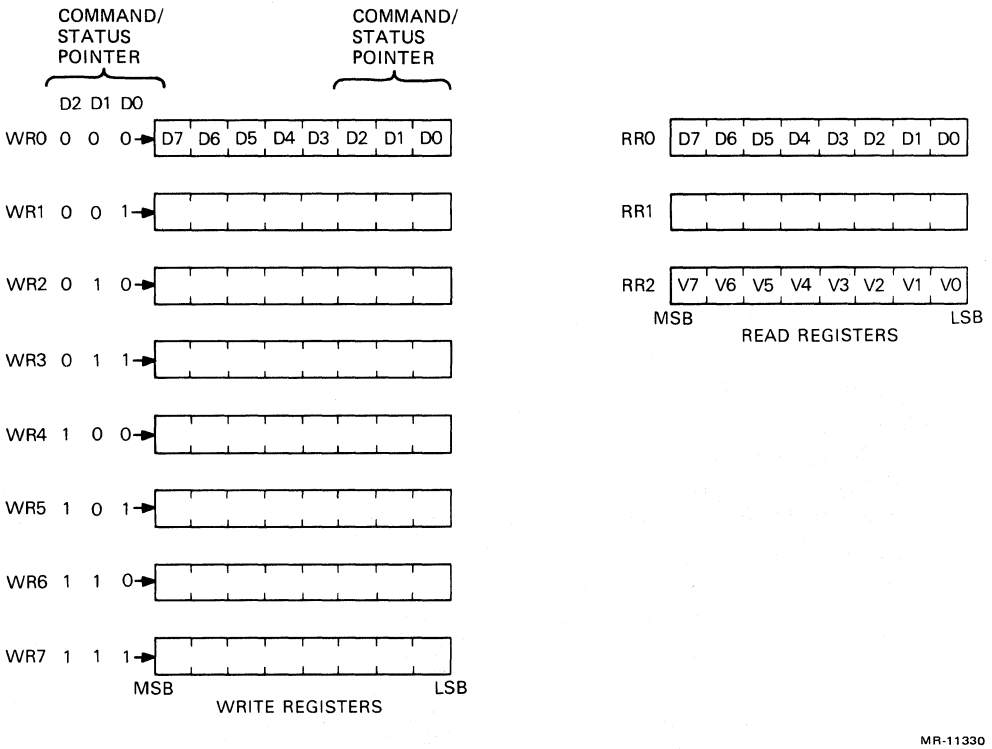


Figure 4-37 MPSC Command/Status Registers (Each Channel)

The three least significant bits of WR0 are automatically loaded into the pointer register every time WR0 is written. After reset, WR0 is set to zero so that the first write to a command register causes the data to be loaded into WR0 (which sets the pointer register). After WR0 is written, the following read or write accesses the register selected by the pointer. The pointer is reset after the read or write operation is completed.

In this manner, reading or writing an arbitrary MPSC channel register requires two I/O accesses. The first access is always a write command. This write command is used to set the pointer register. The second access is either a read or write command; the pointer register (previously set) will ensure that the correct internal register is read or written. After this second access, the pointer register is automatically reset. Note that writing WR0 and reading RR0 does not require presetting of the pointer register.

During initialization and normal MPSC operation, various registers are read and/or written by the 8088. These actions are discussed in detail in the following paragraphs. Note that WR6 and WR7 are not used in the asynchronous communications mode.

4.4.12 MPSC Communications Channel

The communications channel of the MPSC is used to communicate with another computer through the communications port connector J2. It has full modem support and supports the same signals as the VT102. Detailed information on the VT102 can be obtained from the *VT102 Video Terminal User's Guide*, (EK-VT102-UG-003). United States and European full- and half-duplex modems can be supported by this port. The port has asynchronous as well as bisynchronous modes with an RS-423 (V.24, V.28) interface conforming to CCITT standards V.21, V.22, and V.23. Break detection by this port is supported. Baud rates supported are:

50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, 19200

The bit rates are set by writing a byte to the communications baud rate register at I/O address 06H. The four least significant bits 0<3:0> of the byte D<7:0> select the communications receiver clock (COMM RXC) bit rate and the four most significant bits D<7:4> select the communications transmit clock (COMM TXC) bit rate. The format for the communications baud rate register is shown in Figure 4-38.

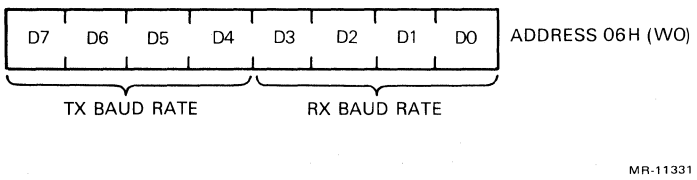


Figure 4-38 Communications Baud Rate Register Format

The communications transmitter and receiver bit rates are software selectable according to the bit values in Table 4-25.

Table 4-25 Communications Baud Rate Selection

D<7:4>–D<3:0> Value (Hexadecimal)	Baud Rate	D<7:4>–D<3:0> Value (Hexadecimal)	Baud Rate
0	50	8	1200
1	75	9	1800
2	110	A	2000
3	134.5	B	2400
4	150	C	3600
5	200	D	4800
6	300	E	9600
7	600	F	19200

When the Rainbow 100 computer is connected to a host computer through a modem, the transmit and receive clocks are supplied to the MPSC by the modem. These external clocks are selected by bit 3 of the printer baud rate register at address 0EH. When bit 3 is high (1), the external clock source supplies the transmit and receive clocks for the communications channel in the MPSC. When bit 3 is low (0), the transmit and receive clocks are supplied by the communications baud rate generator. Note that bits <2:0> of the printer baud rate register select the printer transmit and receive baud rate.

4.4.12.1 Asynchronous Operation – Asynchronous operation (start/stop) is a method of data transmission in which the transmitting and receiving systems need not be synchronized.

Instead of transmitting data clocking information with the data, locally generated clocks at the same rate or 16, 32, or 64 times as fast as the data transmission rate are used by the transmitting and receiving systems. When a character of information is sent by the transmitting system, the character data is framed (preceded and followed) by special start and stop bits. This framing information permits the receiving system to temporarily synchronize with the data transmission.

For operation in the asynchronous mode, the following registers must be initialized with the specified parameters:

- Received character length: WR3, bits D7 and D6
- Transmitted character length: WR5, bits D6 and D5
- Clock rate: WR4, bits D7 and D6
- Number of stop bits: WR4, bits D3 and D2
- Odd, even, or no parity: WR4, bits D1 and D0
- Interrupt mode: WR1, WR2
- Receiver enable: WR3, bit D0
  or
- Transmitter enable: WR5, bit D3

The asynchronous mode register setup is shown in Figure 4-39.

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
WR3	00 RX 5 B/CHAR 01 RX 7 B/CHAR 10 RX 6 B/CHAR 11 RX 8 B/CHAR		AUTO ENABLES	0	0	0	0	RX ENABLE
WR4	00 X1 CLOCK 01 X16 CLOCK 10 X32 CLOCK 11 X64 CLOCK		0	0	00 ENABLE SYNC MODES 01 1 STOP BIT 10 1½ STOP BITS 11 2 STOP BITS		EVEN/ ODD PARITY	PARITY ENABLE
WR5	DTR	00 TX 5 B/CHAR 01 TX 7 B/CHAR 10 TX 6 B/CHAR 11 TX 8 B/CHAR		SEND BREAK	TX ENABLE	0	RTS	0

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Figure 4-39 Asynchronous Mode Register Setup

When loading these parameters into the MPSC, WR4 information must be written before the WR1, WR3, and WR5 parameters/commands.

For transmission via a modem or RS-423 interface, the Request To Send bit (RTS) (WR5; D1) and Data Terminal Ready bit (DTR) (WR5; D7) must be set along with the Transmit Enable bit (WR5; D3). Setting the Auto Enables bit (WR3; D5) allows the programmer to send the first character of the message without waiting for a clear to send (CTS).

Both the Framing Error and Receive Overrun Error flags are latched and cause an interrupt.

If the External/Status Interrupt bit (WR1; D0) is enabled, Break Detect (RR0; D7) and Carrier Detect (RR0; D3) will cause an interrupt. Reset External/Status Interrupts (WR0; D5, D4, D3) will clear Break Detect and Carrier Detect bits if they are set.

A status read after a data read will include error status for the next word in the buffer. If the Interrupt on First Character (WR1; D4, D3) is selected, then data and error status are held until an Error Reset command (WR0; D5, D4, D3) is given.

If the Interrupt on Every Character Mode bit (WR1; D4, D3) is selected, the interrupt vector is different if there is an error status in RR1. When the character is read, the error status bit is set and the Special Receive Condition vector is returned if Status Affects vector (WR1B; D2) is selected.

In a polled environment, the Receive Character Available bit (RR0; D0) must be monitored so that the CPU can determine when data is available. The bit is reset automatically when the data is read. If the X1 clock mode is selected, the bit synchronization must be accomplished externally.

4.4.12.2 Synchronous Operation (Monosync, Bisync) – Synchronous operation is a method of data transmission in which the transmitting station is synchronized to the receiving station through the recognition of a special sync character(s) (byte synchronous) or bit patterns (bit synchronous). Two examples of byte synchronous communications protocol are monosync and bisync. Monosync has one starting sync character per message, while bisync has two starting sync characters per message. Bit synchronous (HDLC/SDLC) operation is described in Paragraph 4.4.12.3.

When using the MPSC for monosync or bisync communications, the following registers must be initialized with the specified parameters:

- Odd or even parity: WR4, bits D1 and D0
- X1 clock mode: WR4, bits D7 and D6
- 8- or 16-bit sync character: WR4, bits D5 and D4
- CRC polynomial: WR5, bit D2
- Transmitter enable: WR5, bit D3
- Interrupt modes: WR1, WR2
- Transmit character length: WR5, bits D6 and D5
- Receive character length: WR3, bits D7 and D6

The synchronous mode register setup for monosync or bisync communications is shown in Figure 4-40.

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
WR3	00 RX 5 B/CHAR 01 RX 7 B/CHAR 10 RX 6 B/CHAR 11 RX 8 B/CHAR		AUTO ENABLES	ENTER HUNT MODE	RX CRC ENABLE	0	SYNC CHAR LOAD INHIBIT	RX ENABLE
WR4	0	0	00 8-BIT SYNC 01 16-BIT SYNC 11 EXT SYNC		0	0	EVEN/ ODD PARITY	PARITY ENABLE
WR5	DTR	00 TX 5 B/CHAR 01 TX 7 B/CHAR 10 TX 6 B/CHAR 11 TX 8 B/CHAR		SEND BREAK	TX ENABLE	1 (SELECTS CRC-16)	RTS	TX CRC ENABLE

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Figure 4-40 Synchronous Mode Register Setup – Monosync/Bisync

WR4 parameters must be written before WR1, WR3, WR5, WR6, and WR7.

The data is transmitted on the falling edge of the transmit clock (TXC) and is received on the rising edge of the receive clock (RXC). The X1 clock is used for both transmit and receive operations for all three sync modes: monosync, bisync, and external.

4.4.12.3 Synchronous Operation (HDLC/SDLC) – HDLC/SDLC synchronous communications is a bit-oriented, code independent protocol for data transmission between a transmitting and receiving station. The high level data link control (HDLC) is a standard communication link protocol established by the International Standards Organization (ISO). HDLC is the protocol used to implement ISO X.25 packet switching systems. The synchronous data link control (SDLC) is a communications link protocol used to implement the system network architecture (SNA). Both HDLC and SDLC are ideal for full-duplex communications.

When using the MPSC for HDLC or SDLC communications, the following registers must be initialized with the specified parameters:

- SDLC mode: WR4, bits D5 and D4
- SDLC polynomial: WR5, bit D2
- Request to send, data terminal ready, and transmit character length: WR5, bits D6 and D5
- Interrupt modes: WR1, WR2
- Transmit enable: WR5, bit D3
- Receive enable: WR3, bit D0
- Auto enable: WR3, bit D5
- External/status interrupt: WR1, bit D0

WR4 parameters must be written before WR1, WR3, WR5, WR6, and WR7.

The synchronous mode register setup for HDLC or SDLC communications is shown in Figure 4-41.

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
WR3	00 RX 5 B/CHAR 01 RX 7 B/CHAR 10 RX 6 B/CHAR 11 RX 8 B/CHAR		AUTO ENABLES	ENTER HUNT MODE	RX CRC ENABLE	ADDRESS SEARCH MODE	0	RX ENABLE
WR4	0	0	1 0 (SELECTS SDLC/ HDLC MODE)		0	0	0	0
WR5	DTR	00 TX ≤5 B/CHAR 01 TX 7 B/CHAR 10 TX 6 B/CHAR 11 TX 8 B/CHAR		0	TX ENABLE	0 (SELECTS SDLC/ HDLC CRC)	RTS	TX CRC ENABLE

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Figure 4-41 Synchronous Mode Register Setup – HDLC/SDLC

4.4.13 MPSC Printer Channel

The printer channel (channel B) of the MPSC is used as a general purpose printer port that provides an EIA RS-423 interface compatible with a number of Digital Equipment Corporation printers. The printer transmit/receive data and printer control signals are routed from the MPSC to the printer through connector J2 on the system module. The following EIA signals are supported:

- Transmit Data (PRT TXD)
- Receive Data (PRT RXD)
- Data Terminal Ready (PTR DTRL)
- Data Set Ready (PTR DSR), always asserted high
- Clear to Send (PTR CTS), always asserted high

Data transmission between the MPSC and the printer is an asynchronous operation. The MPSC WR3, WR4, and WR5 registers must be initialized with the character format required for asynchronous operation as described in Paragraph 4.4.12.1.

Software programmable character formats supported are 5 to 8 bits per character with 1 or 2 stop bits per character. Parity can be selected as odd, even, or none. Software should support XON/XOFF restraint protocol for the printer port. The data set ready (DSR) and clear to send (CTS) outputs of the printer port are tied to +5 V and therefore are always asserted high (1). A null modem cable is not required, and the printer is directly connected to the printer connector on the system module.

The printer port supplies the following software programmable baud rates:

75, 150, 300, 600, 1200, 2400, 4800, 9600

The baud rates are set by writing a byte to the printer baud rate register at address 0EH. The three least significant bits of the byte D<2:0> select a printer transmitter and receiver clock (PRINTER CLK) frequency, that is 16 times the baud rate. The transmitter and receiver clocks for the printer port cannot be independently programmed. Note that bit D<3> of the printer baud rate register is used to select either an internal or external transmitter and receiver clock for the communications channel.

The format for the printer baud rate register is shown in Figure 4-42.

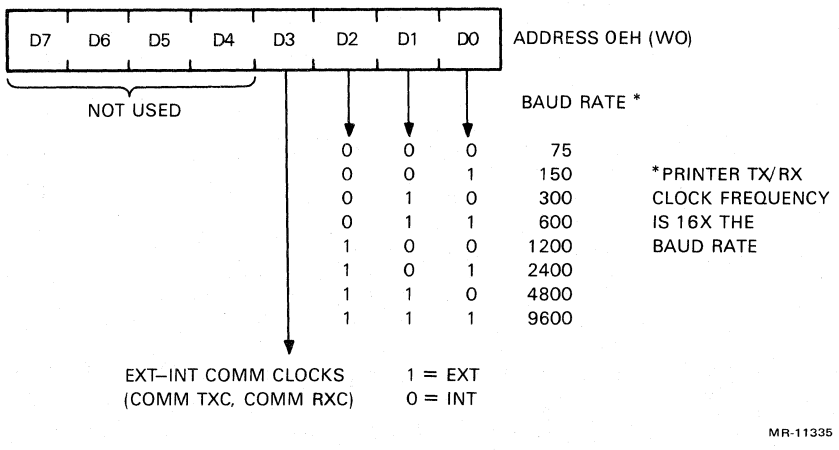


Figure 4-42 Printer Baud Rate Register Format

4.4.14 Keyboard Interface

The keyboard interface is a serial port (J3) on the system module that performs asynchronous serial communications between the keyboard and the 8088 processor using an 8251A programmable synchronous/asynchronous receiver-transmitter (PUSART), a line driver, and a line receiver. The interface provides standard EIA RS-423 signal levels and communicates with the keyboard using full-duplex communications protocol. The interface transfers the character information in groups of 8-bit standard patterns described by the American Standard Code for Information Interchange (ASCII). The character information is transferred at a fixed 4800 baud rate, with an 8-bit, no parity character format.

4.4.14.1 8251A PUSART General Description – The 8251A PUSART is a 28-pin, dual-in-line, microcomputer peripheral device. It contains a transmitter, receiver, I/O buffer, read/write control logic, and shift registers for controlling synchronous or asynchronous data transfers between the 8088 processor and the keyboard. The PUSART, as implemented in the Rainbow 100 computer, is programmed to operate only in the asynchronous mode. The PUSART converts parallel data from the BAD<7:0> bus into serial data for transmission to the keyboard. Simultaneously, it converts serial data from the keyboard into parallel data that is placed on the BAD<7:0> bus for processing by the 8088. The block diagram for the PUSART is shown in Figure 4-43 and the pin functions are described in Table 4-26.

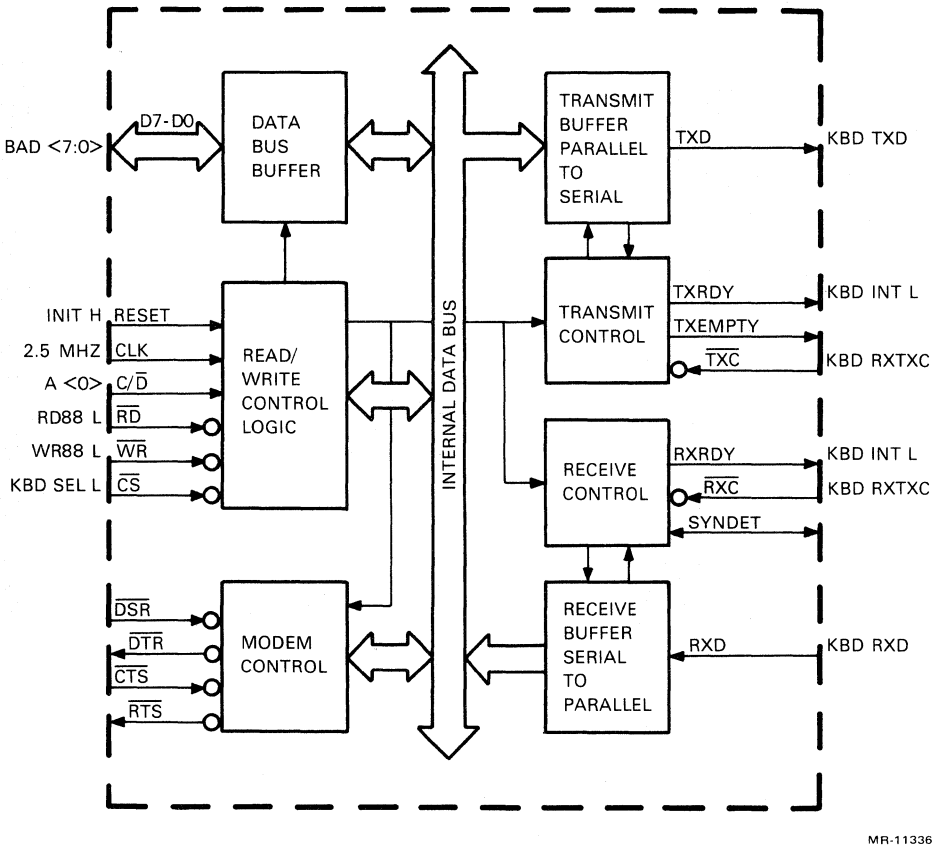


Figure 4-43 8251A PUSART Block Diagram

Table 4-26 8251A PUSART Pin Descriptions

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
1,2,5 6,7,8, 27,28	BAD<7:0>	D7–DO	I/O	DATA BUS: This bus transfers data, control, command, and status information between the 8088 and the keyboard PUSART. Data is transmitted or received by the PUSART upon execution of I/O instructions from the 8088. BAD <0> is the least significant bit.
3	KBD RXD	RXD	I	KEYBOARD RECEIVE DATA: This signal is serial input from the keyboard.
4	GND	GND		GROUND.
9	KBD RXTXC	TXC	I	KEYBOARD RECEIVE/TRANSMIT CLOCK: This signal controls the rate at which the character is transmitted to the keyboard. In asynchronous mode, the frequency of KBD RXTXC is 16 times the 4800 keyboard baud rate.
10	WR88 L	WR	I	WRITE 8088: This signal, when low (0), indicates that the 8088 is writing data or control information to the PUSART.
11	KBD SEL L	CS	I	KEYBOARD SELECT: This signal, when low (0), enables the PUSART to accept data, control, and command inputs from the 8088 during a write cycle, or to transmit data or status inputs to the 8088 during a read cycle.
12	A<0>	C/D	I	CONTROL/DATA SELECT: This address bit, in conjunction with the WR88 and RD88 inputs, informs the PUSART that the word on the data bus BAD<7:0> is either a data character, control word, or status information. 1 = Control, 0 = Data.
13	RD88 L	RD	I	READ 8088: This signal, when low (0), indicates that the 8088 is reading data or status information from the PUSART.

*O = Output, I = Input, I/O = Input/Output

Table 4-26 8251A PUSART Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
14	KBD INT L	RXRDY	O	RECEIVER READY: When low (0), this signal interrupts the 8088 to indicate that the PUSART is ready to accept a character. RXRDY is automatically reset when the character is read by the 8088.
15	KBD INT L	TXRDY	O	TRANSMITTER READY: When low (0), this signal interrupts the 8088 to indicate that the PUSART is ready to accept a character. TXRDY is automatically reset when a character is loaded from the 8088.
16		SYNDET	I/O	SYNC DETECT: This pin is not used by the Rainbow 100 computer.
17		CTS	I	CLEAR TO SEND: This signal, when low (0), enables the PUSART to transmit serial data if the transmitter enable bit TXEN in the command byte is high (1). This signal is tied to ground in the Rainbow 100 computer.
18		TXEMPTY	O	TRANSMITTER EMPTY: This signal is not used in the Rainbow 100 computer.
19	KBD TXD	TXD	O	KEYBOARD TRANSMITTED DATA: This signal is the serial transmitted data from PUSART to the keyboard.
20	2.5 MHZ	CLK	I	CLOCK: This clock input is used to generate internal PUSART timing and is connected to the 2.5 MHz clock source.
21	INIT L	RESET	I	INITIALIZE: During power-up, this signal is low (0). The low signal forces the PUSART to an idle state. The PUSART will remain in the idle state until a new set of control words is written into the PUSART.

*O = Output, I = Input, I/O = Input/Output

Table 4-26 8251A PUSART Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
22		DSR	I	DATA SET READY: During normal operation, this signal is inactive high (1). During manufacturing testing, this signal is jumpered to ground.
23		RTS	O	REQUEST TO SEND: This signal is not used in the Rainbow 100 computer.
24		DTR	O	DATA TERMINAL READY: This signal is not used in the Rainbow 100 computer.
25	KBD RXTXC	RXC	I	KEYBOARD RECEIVE/TRANSMIT CLOCK: This signal controls the rate at which the PUSART receives characters. In asynchronous mode, the frequency of KBD RXTC is 16 times the 4800 keyboard baud rate.
26	+5 V	VCC		POWER: +5 V Supply

*O = Output, I = Input, I/O = Input/Output

The functions of the PUSART are controlled by internal control, status, and data buffer registers that are programmed by the system's software. These registers are described in the following paragraphs.

4.4.14.2 Control Register: 8251A – The control register is an 8-bit write-only register that must be loaded with a set of control words by the 8088 processor before the PUSART can transmit or receive data. These control words define the complete functional definition of the PUSART and must immediately follow a reset operation (internal or external). The control words are split into two formats:

1. Mode instruction
2. Command instruction

The mode instruction defines the general characteristics of the PUSART. It must follow a reset operation. Once the mode instruction has been written into the PUSART, command instructions can be written.

The command instruction defines a status word that is used to control the operation of the PUSART. Both the mode instruction and command instruction must conform to a specified sequence for proper operation. The mode instruction must be written immediately following a reset operation, prior to using the PUSART for data communications. All control words written into the PUSART after the mode instruction will load the command instruction. Command instructions can be written into the PUSART at any time in the data block during operation of the PUSART. To return to the mode instruction format, a bit (D6) in the command instruction word can be set to initiate an internal reset operation that automatically places the PUSART back into the mode instruction format.

The control register is accessed by performing a write operation to address 11H. The mode instruction and command instruction formats are shown in Figures 4-44 and 4-45.

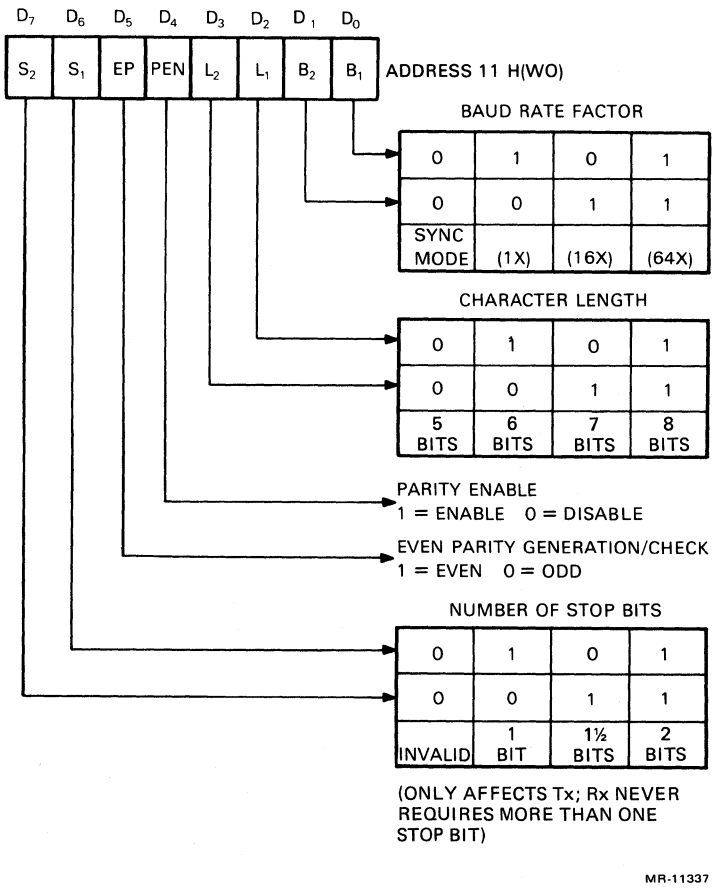


Figure 4-44 Mode Instruction (8251A) Format

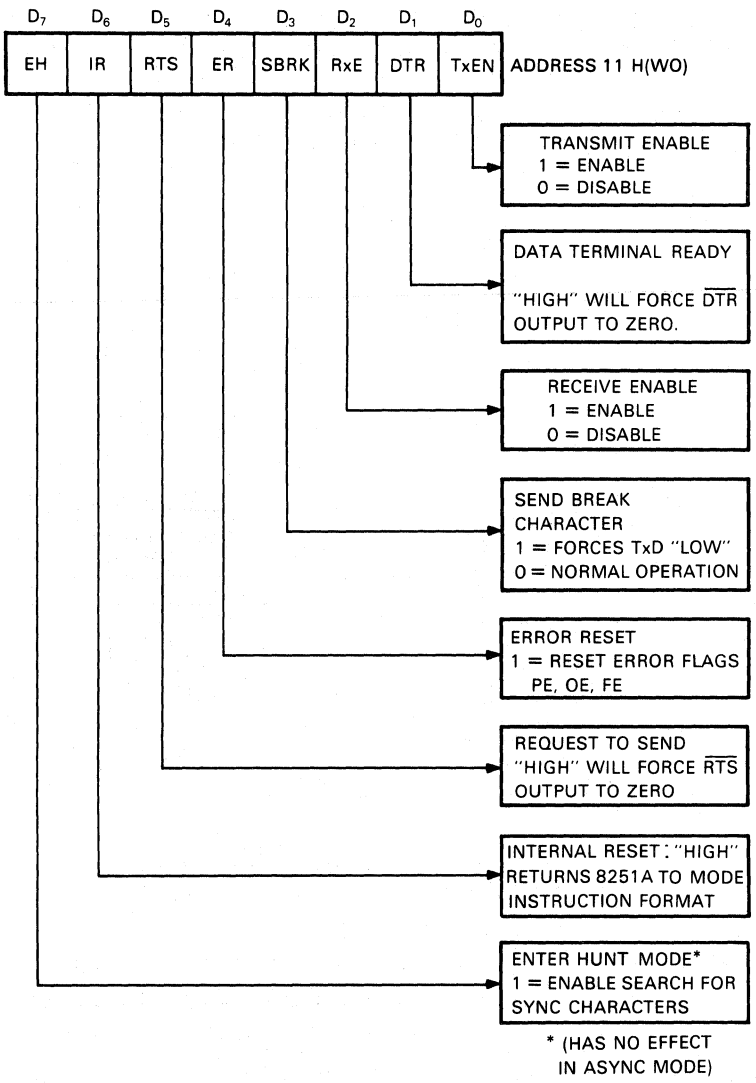


Figure 4-45 Command Instruction (8251A) Format

4.4.14.3 Status Register: 8251A – The status register is an 8-bit read-only register that holds the status of the active device to determine if data transfer errors or other conditions have occurred that require 8088 processor intervention. The status of the active device can be read at any time by issuing a normal read command at address 11H.

Some of the bits in the status register have identical meanings to the pin descriptions listed in Table 4-26 so that the PUSART can be used in a completely polled environment or in an interrupt driven environment. The status register format is shown in Figure 4-46.

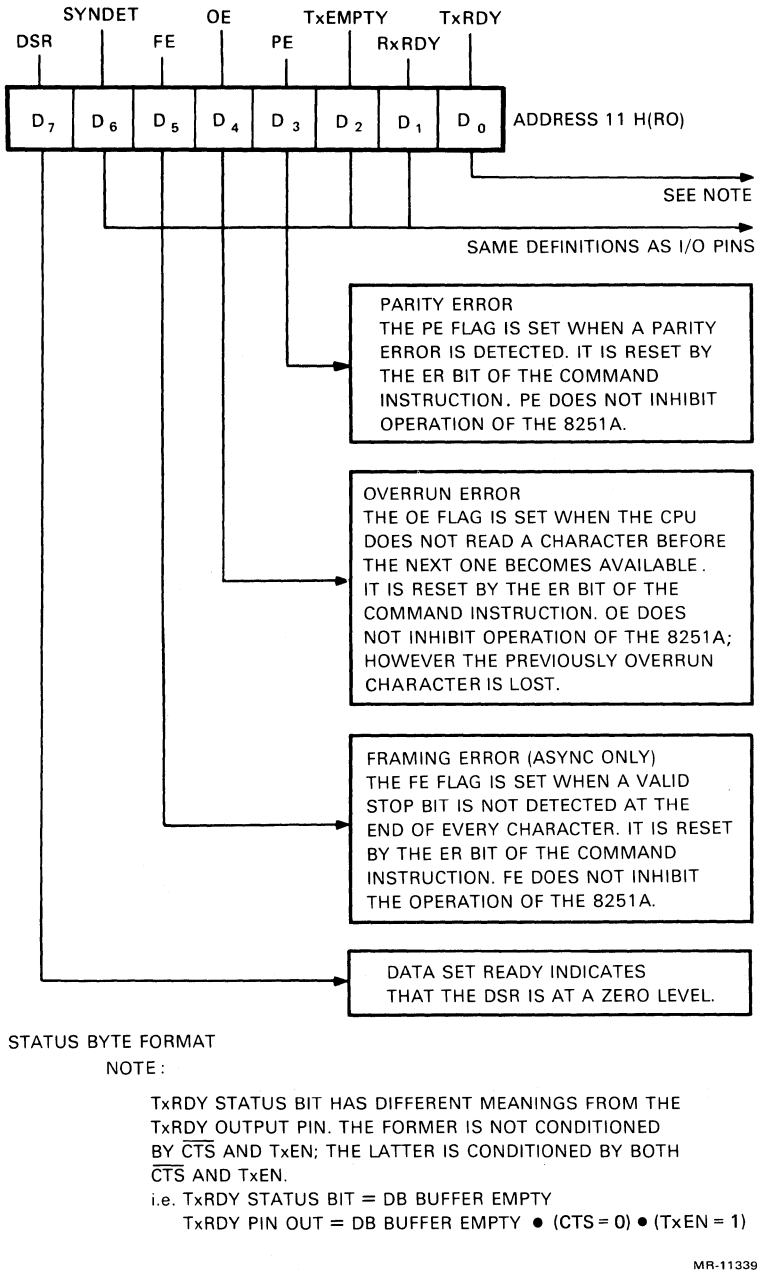


Figure 4-46 Status Register (8251A) Format

4.4.14.4 Transmit and Receive Data Registers: 8251A – The transmit data (WO) and receive data (RO) registers hold the 8-bit characters and the start/stop bits transmitted to or received from the keyboard. In the Rainbow 100 computer, the transmit and receive character length will always be 8 bits with no parity. The character length and the number of stop bits are specified by the mode instruction written into the control register following a reset operation.

When transmitting data, the 8251A will add start and stop bits to the 8-bit character output of the 8088 processor and then shift out the assembled serial data to the keyboard. When receiving data, the 8251A shifts the serial data (character, start, and stop bits) from the keyboard into the receive data register. The 8251A then checks the received data for the correct format, discards the start and stop bits, and places the 8-bit character in parallel on the BAD <7:0> bus. The keyboard data registers are accessed by performing a write or read operation to address 10H.

The transmit and receive data formats are shown in Figure 4-47.

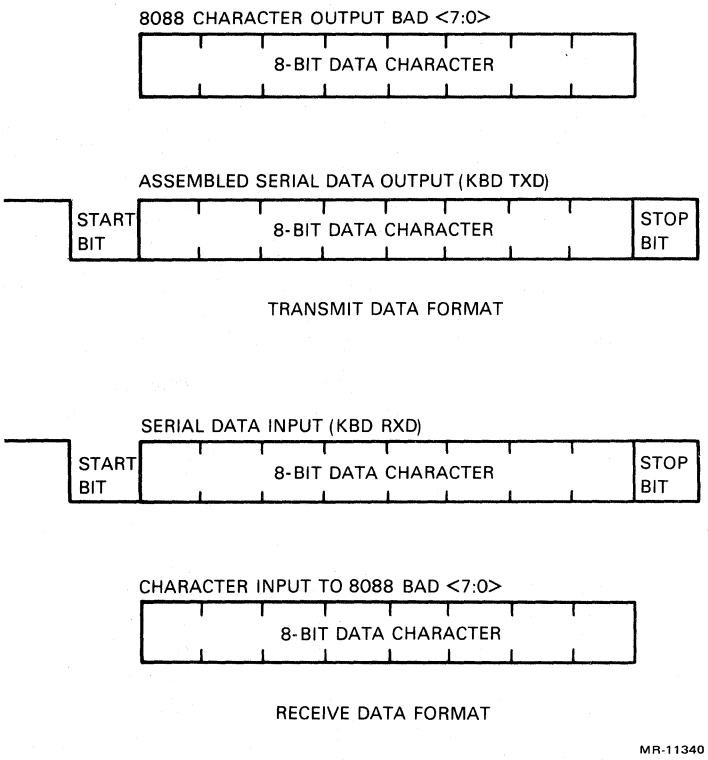


Figure 4-47 Transmit and Receive Data Format

4.4.15 MHFU Detection Logic

A massive hardware failure (MHFU) detection circuit on the system module is provided to detect situations in which the 8088 processor has lost most of its functions. If the 8088 does not acknowledge a video processor vertical interrupt within approximately 108 milliseconds, the MHFU detection circuit will apply a reset signal to the 8088 for 108 milliseconds. This reset causes the 8088 to begin executing the power-up or reset boot ROM code at address FFFF:0.

MHFU detection is disabled by writing to the DC12 write register at address 10CH. It is enabled by writing to the DC12 at address 0CH. The status of the MHFU enable/disable signal may be read from bit D<5> of the communications status register at address 02H. When the firmware begins executing the program at location FFFF:0, it assumes a power-up reset if MHFU detection is disabled or an MHFU reset if MHFU detection is enabled.

The MHFU detection logic consists of an MHFU timer and an MHFU enable flip-flop. The MHFU detection logic is shown in Figure 4-48.

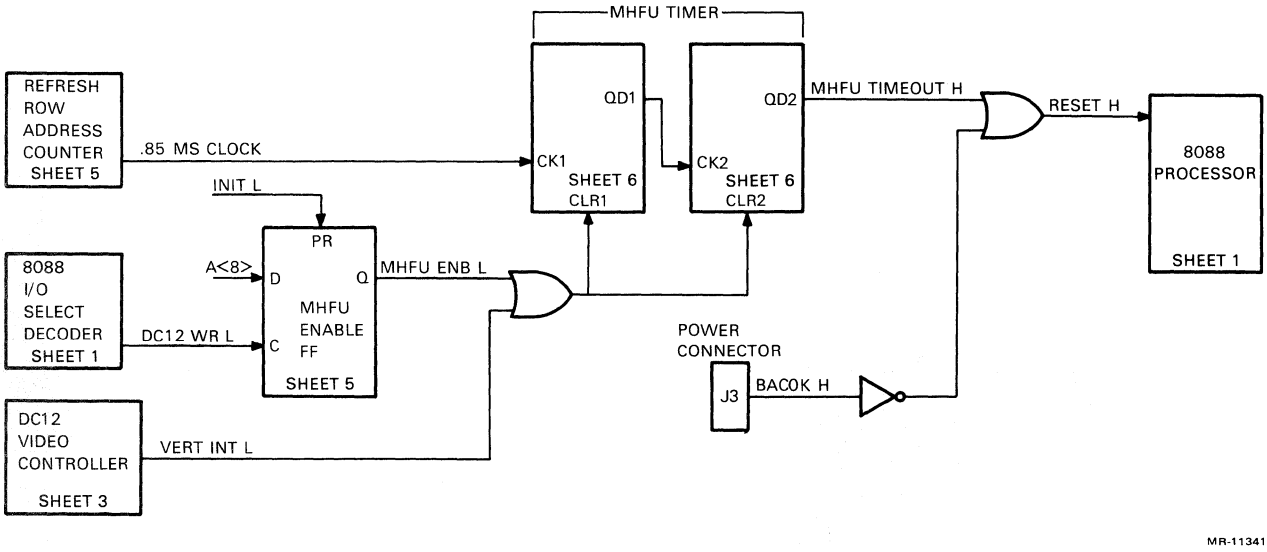


Figure 4-48 MHFU Detection Block Diagram

The MHFU timer is an 8-bit binary counter clocked by .85 millisecond period clock pulses from the refresh row address counter. The MHFU timer is reset by signals from two sources: the VERT INT L signal from the DC12 video controller, or the MHFU ENB L signal from the MHFU enable flip-flop. The output of the MHFU timer will go active high (1) if the 8088 has not acknowledged a video processor interrupt within approximately 108 milliseconds.

4.5 SYSTEM MODULE CONNECTORS

The system module contains nine connectors that provide the interconnection to the other system components and option modules. Three of these connectors (J1, J2, and J3) are D-type subminiature connectors that are used to connect the system unit via cables to the video monitor, printer, and a remote computer. The other six connectors (J4 through J9) are printed circuit board headers that are used to provide the signal and power connection for option modules, the RX50 controller module, and the power supply. The connector locations on the system module are shown in Figure 4-2. The connector signals are described in Tables 3-2 through 3-12 of Chapter 3.

4.6 SYSTEM MODULE SPECIFICATIONS

The following paragraphs describe the physical, power, and environmental specifications for the system module.

4.6.1 Physical Dimensions

Length	35.56 cm (14 in)
Width	26.42 cm (10.4 in)
Height	2.25 cm (0.9 in) The height of the module is the combined thickness of the printed circuit board and printed circuit board connectors.

4.6.2 DC Power

The dc power required by the system module is as follows:

+5 Vdc	+ or − 5% at 5.5 A maximum
+12 Vdc	+ or − 10% at 0.3 A maximum
−12 Vdc	+ or − 10% at 0.3 A maximum

4.6.3 Environmental

The system module meets the environmental requirements of Digital Equipment Corporation Standard 102, class B, and the conducted and radiation emission limits established by FCC rules for class B computing devices.

4.6.3.1 Temperature

Storage	−40° C to 80° C (−40° F to 176° F)
Operating	−5° C to 60° C (41° F to 140° F)

When the temperature is beyond the operating range, the unit must first be brought to an environment within the operating range and allowed to stabilize for at least five minutes before operating the system module.

When the system is operating at the maximum temperature, airflow must maintain the inlet-to-outlet air temperature rise across the system module at not more than 5° C (9° F). Derate the maximum operating temperature by 0.56° C (1° F) for each 305 m (1,000 feet) of altitude above 2,440 m (8,000 feet).

4.6.3.2 Relative Humidity

Storage	5% to 95%, noncondensing
Operating	5% to 95%, noncondensing

4.6.3.3 Altitude

Storage	15.24 km (50,000 feet), 90 mm mercury maximum

The module is not mechanically or electrically damaged at altitudes up to 50,000 feet.

Operating	2,440 m (8,000 feet)

The maximum operating temperature must be derated at high altitudes (Paragraph 4.6.3.1).

CHAPTER 5
RX50 CONTROLLER MODULE

5.1 INTRODUCTION

This chapter provides a technical description of the RX50 controller module for repair or maintenance personnel. The RX50 controller module is described to the functional block diagram level. The logic circuits are generally not described to the detailed circuit level except in those cases where such description is considered necessary for a clear understanding of the subject matter.

5.1.1 Chapter Organization

The information in this chapter is divided into five sections.

- Section 5.2 provides a general description of the functions performed by the RX50 controller module.
- Section 5.3 provides a physical description of the RX50 controller module.
- Section 5.4 provides a functional description of the RX50 controller module.
- Section 5.5 describes the RX50 controller connectors.
- Section 5.6 provides the RX50 controller module specifications.

5.1.2 Related Documentation

The logic blocks in some of the block diagrams used in this chapter contain the word SHEET followed by a number. This refers to a sheet number of the RX50 controller module schematics. These numbers may be used to locate the detailed circuit logic represented by the function logic blocks. The RX50 controller module circuit schematics (D-CS-5415482-0-1) consists of two sheets and are a part of the PC100 Field Maintenance Print Set (MP-01491-00).

5.2 GENERAL DESCRIPTION

The RX50 controller module provides an interface to the system module for up to two RX50 diskette drives. Each diskette drive contains two counter-rotating spindles that rotate two diskettes. The RX50 controller module plugs into connector J9 on the system module and supports double density, 96 tracks per inch (TPI), single-sided diskettes. Sector locations on the diskette are controlled by the software (soft-sectored).

The RX50 controller converts binary data from the Z80A processor into modified frequency modulation (MFM) data. The MFM data is then transmitted to the diskette drive, where it is recorded on the diskette. MFM is a magnetic recording method for diskette drives in which a clock signal is encoded in the flux transitions recorded on the diskette. When reading data from the diskette, the RX50 controller synchronizes on the read data transitions; and with a phase-locked loop (PLL) and MFM decoder, the controller recovers the clocks and data.

Commands, status, and data transfers to and from the diskette drives are controlled by the Z80A, which accesses eight registers on the RX50 control module. Three of these registers are discrete component registers, mounted on the module, and the remaining five registers are inside the 1793 formatter/controller chip.

5.3 PHYSICAL DESCRIPTION

The RX50 controller module is a high density, four-layer, printed circuit board that is 9.90 cm (3.9 in) wide and 24.13 cm (9.5 in) long. The module contains one 40-pin connector, for the interface to the system module, and two 34-pin connectors, for the interface to the diskette drives. The 40-pin connector is located on the solder side (side 2) of the module, and the two 34-pin connectors are on the component side (side 1). Each diskette drive is connected to the RX50 controller module by a shielded 34-conductor ribbon cable.

The module also contains three jumpers (W1, W2, and W3), a potentiometer, and a test point. Jumpers W2 and W3 are always installed, and W1 is never installed. The potentiometer and the test point are used to adjust the free running frequency of a voltage controlled oscillator to ensure proper operation of the data separator circuit.

NOTE

The data separator adjust potentiometer is set during manufacturing testing and should not be recalibrated in the field.

The locations of the connectors, jumpers, data separator adjust potentiometer, precompensation data pattern ROM, and the 1793 formatter/controller chip are shown in Figure 5-1.

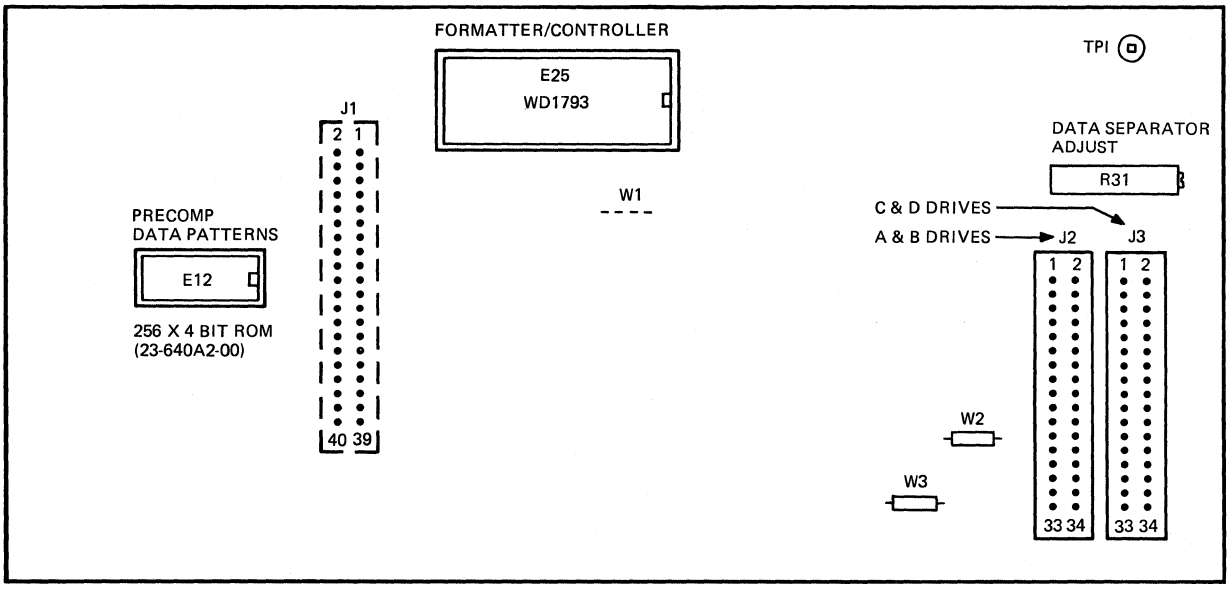


Figure 5-1 RX50 Controller Module Physical Layout

5.4 FUNCTIONAL DESCRIPTION

The RX50 controller module contains the following major circuits:

- WD1793 formatter/controller
- Data separator
- Write precompensation
- Diskette drive/diagnostic data selector
- Diskette drive select logic
- Diskette status register
- Diskette control register
- General/diagnostic status register

The major RX50 controller circuits, shown in Figure 5-2, are described in the following paragraphs.

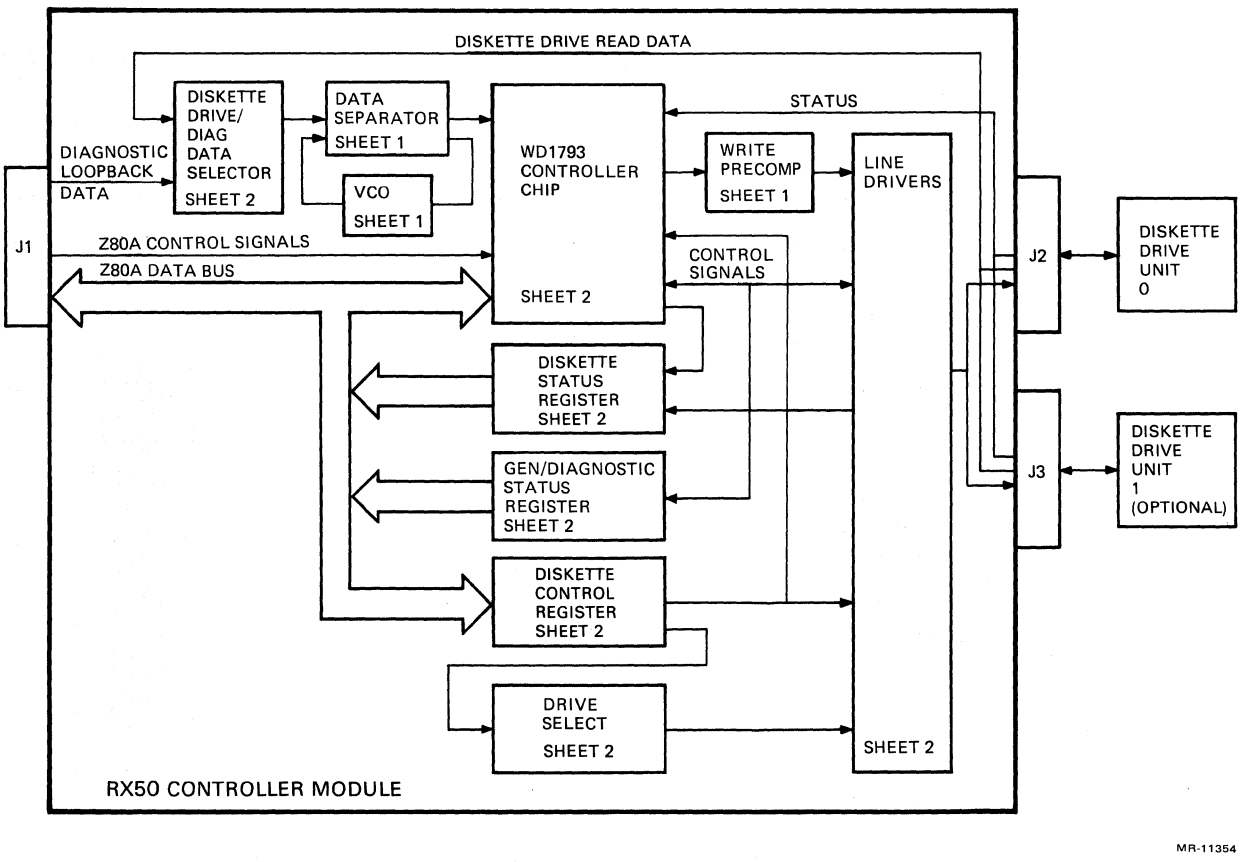


Figure 5-2 RX50 Controller Module Block Diagram

5.4.1 Diskette Drive Formatter/Controller

The diskette drive formatter/controller is a 40-pin, dual-in-line MOS, LSI circuit that provides the interface from the RX50 controller module to the Z80A processor and the diskette drives. The Z80A controls the operation of the formatter/controller to read from, and write data to, the diskette drives by writing commands to, and reading status from, the five internal registers.

Figure 5-3 shows the internal registers and other logic contained in the formatter/controller. The primary sections include the parallel process interface and the diskette drive interface.

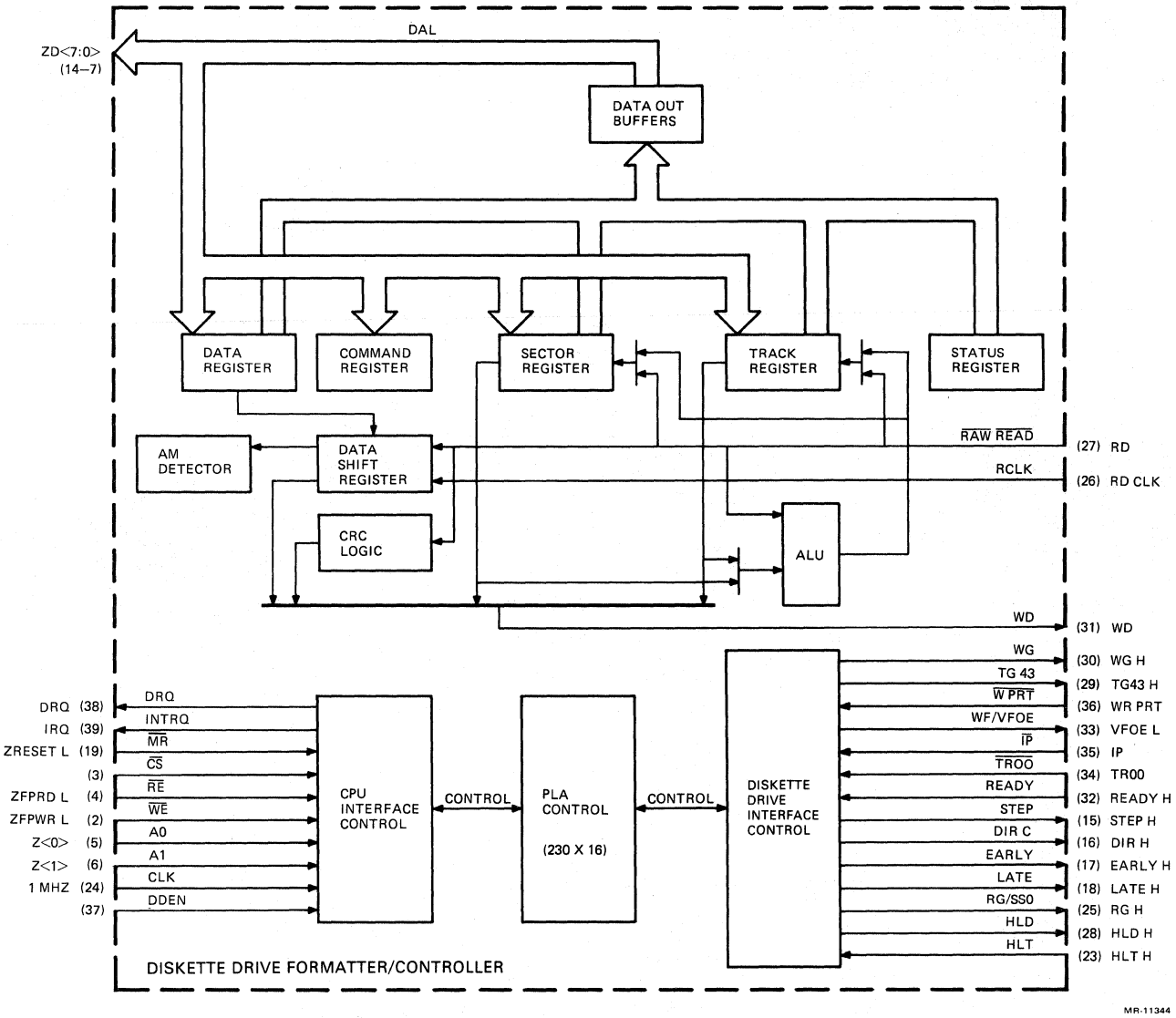


Figure 5-3 Diskette Drive Formatter/Controller Block Diagram

5.4.1.1 Processor Interface – The interface of the formatter/controller to the Z80A processor consists of an 8-bit bidirectional data bus ZD<7:0> read/write controls, and interrupt lines. After the device is selected by the chip select (CS) signal, the five internal registers can be accessed by a combination of the Z80A address bits ZA<1:0> and the read/write control signals. Table 5-1 describes the registers and their addresses.

Table 5-1 Formatter/Controller Register Selection

Chip Select (CS)*	Address Bits ZA<1>	ZA<0>	Read (ZFPRD L)	Write (ZFPWR L)
0	0	0	FDC Status Register	FDC Command Register
0	0	1	FDC Track Register	FDC Track Register
0	1	0	FDC Sector Register	FDC Sector Register
0	1	1	FDC Data Register	FDC Data Register

*This signal is tied to ground in the RX50 controller.

Each time a command is issued to the formatter/controller, the busy bit is set in the FDC status register, and the interrupt request (IRQ) line is reset. The busy bit is reset whenever the formatter/controller is idle and awaiting a new command. Once set, the IRQ line can only be reset by a read of the FDC status register or by issuing a new command. The Z80A reset signal does not affect IRQ.

Other Z80A interface lines are a 1 MHz clock signal, double density enable (DDEN), and ZRESET L. DDEN is tied to ground in the RX50 controller to select the double density mode of operation. The ZRESET L signal from the 8088 processor diagnostic write register clears and initializes all internal registers and causes the RX50 controller to issue a restore command to the diskette drive.

5.4.1.2 Diskette Drive Interface – The diskette drive interface can be divided into three sections: motor control, write signals, and read signals. All of the output lines are applied to the RX50 controller diskette drive connectors (J2 and J3) through open collector line drivers.

The step and direction (DIR) lines provide motor control. The step line issues stepping pulses with a period defined by the rate field in all type I commands. The DIR line defines the stepping direction of the read/write heads. (DIR = 1, heads step in; DIR = 0, heads step out).

Other control lines include the index pulse (IP) and the track zero (TROO) input signal. The IP goes to the diskette drive's index sensor and makes an active transition for each revolution of the diskette. TR00 connects to the track zero sensor in the diskette drive to inform the formatter/controller that the read/write head is on track zero of the diskette.

The READY input signal informs the formatter/controller that a diskette is in the selected diskette drive side. The formatter/controller checks the status of this signal before executing any read/write commands.

Writing of data is accomplished by the use of write data (WD), write gate (WG), any track greater than 43 (TG 43), EARLY, and LATE output signals. WG is used to enable write current at the diskette drive's read/write head. It is made active prior to writing data on the diskette. Write data (WD) are the serial MFM pulses to be recorded as flux transitions on the diskette. WD contains the unique address marks as well as data and clocks in MFM formats.

The TG43 output signal is used to inform the diskette drive electronics to reduce the write current because the data will be written on a track greater than 43. Bit density is greater on the inner tracks of the diskette, and therefore less write current is needed to produce the flux transitions.

The EARLY and LATE outputs of the formatter/controller are used in conjunction with WD to determine the precompensation values for the MFM write data.

The read signal inputs to the formatter/controller are the read data (RD) and the read clocks (RD CLK). Both of these signals are obtained from the data separator circuit. When the formatter/controller encounters the sync field of the read data, it asserts the read gate (RG) and allows the separator circuit to lock on the incoming data.

5.4.1.3 FDC Control Register (Write Only) Address 60H – This eight-bit register holds the command presently being executed. The formatter/controller will accept nine commands from the Z80A processor. All commands, except the force interrupt, should be loaded into the control register when the busy status bit is off. The force interrupt can be loaded at any time.

Type I commands are for head positioning. The stepping rate of these commands is dictated by the characteristics of the diskette drive. R1 and R0 = 0 (6 ms) is the recommended stepping rate for the RX50 diskette drive.

The head load flag determines if the head is loaded at the beginning of the command. Otherwise, the head is loaded at the end of a command.

The verification flag allows a verification operation to take place on the destination track. The verification consists of reading the first encountered ID field off the diskette.

The track address of the ID field is compared to the track register. If there is a match and a valid ID cyclic redundancy check (CRC), the verification is complete. If not valid, the seek error status bit in the status register is set.

The step, step-in, and step-out commands contain an update flag for updating the track register when this bit is set after the step has been completed.

Type I command bits are described in Table 5-2 and type I command flags are described in Table 5-3.

The type iI commands are to read and write sectors to the diskette. Prior to loading the type II command into the command register, the sector register must be loaded with the desired sector number.

Upon receipt of the command, the busy status bit is set. If the e flag is set (normal case), the head is loaded and the HLT signal is sampled after 30 ms; otherwise, there is no delay after a command.

The HLT does not become active until 500 ms (500 ms is specific to the RX50 drive) after the head is loaded to allow the spindle motor to reach full speed. The formatter/controller then attempts to find the ID field with the specified track and sector.

If the desired field is not found within five revolutions of the diskette, the record not found status bit is set. When the desired field is found, the formatter/controller executes the command by generating data requests (DRQs) for servicing the data register.

Each of the type II commands contains an m flag that determines if multiple sectors are to be read or written, depending on the command. When set, multiple sectors are read or written with the sector register internally updated for address verification on the next track.

Table 5-2 Type I Command Bit Description

Bit	Name	Description
0,1	Stepping rate (r1, r0)	These bits control the rate at which the stepping pulses are sent to the diskette drive. See Table 5-4 for stepping rate breakdown.
2	Track verify (v)	This bit determines if there is a verification operation to take place on the destination track. During verification the head is loaded, and after a 30 ms delay, the HLT input is sampled. After a 500 ms motor start-up time, the HLT input becomes active. When HLT is set, the first ID field is read off the diskette. The track address of the ID field is compared to the track register. If there is a match and a valid ID CRC, the verification is complete and an interrupt is generated. If not valid, the seek error status is set.
3	Head load flag (h)	This bit determines if the head is to be loaded at the beginning of a command. If the head is loaded, then the head remains loaded until either the formatter/controller receives a command that specifically disengages the head or 15 revolutions of the diskette have passed with the busy bit equal to 0.
4	Update (step commands) (u)	When set (1), the track register is updated for each step; otherwise the track register is not affected.
5–7		These bits determine the command to be executed.

Table 5-3 Type I Command Flags

Bit	Flag	Name	Function
3	h	Head load flag	h = 1, Load head at beginning h = 0, Unload head at beginning
2	v	Verify flag	v = 1, Verify on destination track v = 0, No verify
0, 1	r1, r0	Stepping motor rate	r1 r0 0 0 6 ms 0 1 12 ms 1 0 20 ms 1 1 30 ms
4	u	Update flag	u = 1, Update track register u = 0, No update

The formatter/controller continues to do the data transfers until the sector register exceeds the number of sectors on the track or until a force interrupt command is loaded into the command register.

NOTE

If the command is not terminated by software, the formatter/controller continues looking for five index pulses after the last sector on the diskette has been read or written.

If the sector register exceeds the number of sectors on the track, the Record Not Found status bit is set. When the head is loaded, the Busy status bit is set, and when an ID field is encountered that has the correct track, sector, side numbers, and correct CRC, the data field is presented to the Z80A (read) or presented by the Z80A (write).

At the end of the read operation, the type of data address mark encountered is recorded in the status register (bit 5). On a write operation, the a0 flag (bit 0) determines the type of data address mark to be written onto the diskette. If bit 0 is set, a deleted data mark is written. If bit 0 is reset, a data mark is written.

Type II command bits are described in Table 5-4 and type II command flags are described in Table 5-5.

Table 5-4 Type II Command Bit Description

Bit	Name	Description
0	Data address mark	When set upon a write sector command, this bit defines a data mark (OFBH) to be written on the diskette. If the bit is not set, then a deleted data mark (OF8H) is written onto the diskette. When writing valid data on the diskette, this bit should be set.
1		Always 0.
2	30 ms delay	When set during a command, there is a 30 ms delay before reading begins. For maximum controller throughput, this bit should be 0. It should be set if the last command was a seek or new drive select. (See Table 5-5).
3		Always 0.
4	Multiple sector	When set, this bit allows multiple sectors to be transferred.
5–7		These bits determine the command to be executed.

Table 5-5 Type II and III Command Flags

Bit	Flag	Name	Function
4	m	Multiple record flag	m = 1, single record m = 1, multiple records
0	a0	Data address mark	a0 = 0, 373° (data mark) a0 = 1, 370° (deleted data mark)
2	e	30 ms delay	e = 1, 30 ms delay e = 0, No delay

The type III command is the read address command. When the formatter/controller receives this command, the read/write head in the diskette drive is loaded and the busy bit is set in the status register. The next encountered ID field is then read in from the diskette drive, the six data bytes of the ID field are assembled and transferred to the data register, and a data request (DRQ) is generated for each byte. The six bytes of the ID field are the track address, side number, sector address, sector length, and two bytes of CRC characters.

The formatter/controller checks the CRC characters for validity and sets the CRC error status bit if there is a CRC error. The track address of the ID field is written into the sector register. At the end of the operation, an interrupt is generated and the busy bit in the status register is reset.

Type III command bits are described in Table 5-6 and type III command flags are described in Table 5-5.

Table 5-6 Type III Command Bit Description

Bits	Description
0,1	Always set to 0.
2	Same as bit 2 for type II commands. (See Table 5-5.)
3–7	Determine the command to be executed.

The type IV command is the force interrupt command. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set), the command will be terminated and an interrupt will be generated when the condition specified in bits 3:0 of Table 5-7 is encountered.

Table 5-7 Type IV Command Flags

Bit	Flag	Name	Function
0	I0	Interrupt condition	I0 = 1, Not ready-to-ready transition
1	I1	Interrupt condition	I1 = 1, Ready-to-not ready transition
2	I2	Interrupt condition	I2 = 1, Index pulse
3	I3	Interrupt condition	I3 = 1, Immediate interrupt (requires reset)*

* If I3–I0 = 1, there is no interrupt generated, but the current command is terminated and busy is reset. This is the only command that will enable the immediate interrupt to clear on a subsequent load command register or read status register.

Table 5-8 summarizes the command types that are written into the FDC control register.

Table 5-8 Formatter/Controller Command Summary

Command Type*	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	v	r1	r0
I	Seek	0	0	0	1	h	v	r1	r0
I	Step	0	0	1	u	h	v	r1	r0
I	Step in	0	1	0	u	h	v	r1	r0
I	Step out	0	1	0	u	h	v	r1	r0
II	Read sector	1	0	0	m	0	e	0	0
II	Write sector	1	0	0	m	0	e	0	a0
III	Read address	1	1	1	0	0	e	0	0
III	Read track	1	1	1	0	0	e	0	0
III	Write track	1	1	1	1	0	e	0	0
IV	Force interrupt	1	1	0	1	I3	I2	I1	I0

*Read track and write track are not supported by the RX50 controller.

5.4.1.4 FDC Status Register (Read Only) Address 60H – The read-only register resides at the same address as the control register. It contains the 8-bit status resulting from the completion of a command.

Upon receipt of any command, except the force interrupt command, the busy status bit is set and the rest of the status bits are updated or cleared for the new command. If the force interrupt command is received when there is a current command under execution, the busy status bit is reset, and the rest of the status bits are unchanged. If the force interrupt command is received when a current command is not under execution, the busy status bit is reset, and the rest of the status bits are updated or cleared. In this case, the status bits reflect the type I commands.

The format of the status register for all type I and type II (read sector and write sector) commands is shown in Figures 5-4, 5-5, and 5-6. The status register bits are described in Tables 5-9, 5-10, and 5-11.

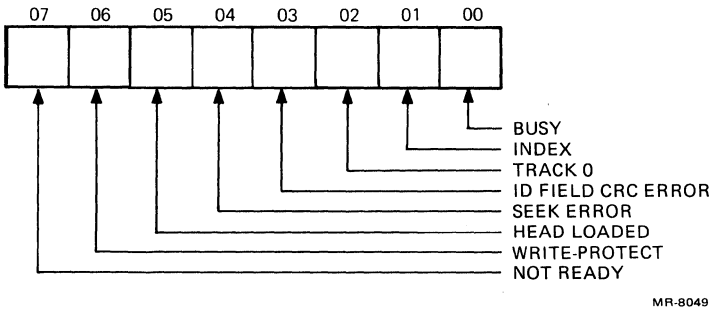


Figure 5-4 Type I Status Register Format

Table 5-9 Type I Status Register Bit Description

Bit	Name	Description
0	Busy	When this bit is set (1), the formatter/controller is currently executing a command. Only a type IV command can be issued when this condition exists.
1	Index	When this bit is set (1), the index hole in the diskette is under the index sensor.
2	Track 0	When this bit is set (1), the read/write head is positioned at track 0.
3	ID field CRC error	When set, this means that there was a CRC error in the ID field.
4	Seek error	When set, a seek error was encountered, meaning that the destination track address was not found.
5	Head loaded	This bit reflects the current status of the head. When set, the head is loaded and the HLT input is asserted.
6	Write-protect	When set, the bit means that the current diskette is write protected. An attempt to write a sector generates an interrupt if the device interrupt enable bit is set.
7	Not ready	When set, the bit indicates that the diskette drive is not ready. This could mean that the drive is not selected, the diskette is in upside down, or the door is open. This bit must be clear before any commands are issued to the formatter/controller.

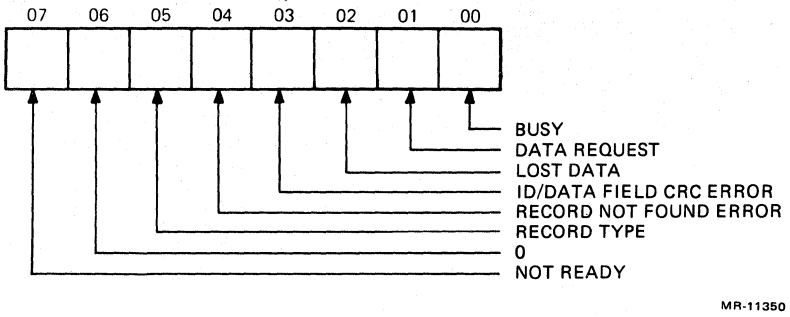


Figure 5-5 Type II Read Sector Status Register Format

Table 5-10 Type II Read Sector Status Register Bit Description

Bit	Name	Description
0	Busy	Same as type I status.
1	Data request	When set, this bit means that the data register is full and is waiting for the CPU to read the register.
2	Lost data	When set, this bit means that the data register had not been serviced within 27.0 microseconds and the data in the data register is not valid.
3	ID/data field CRC error	When set, this bit indicates that an error was found in one or more ID fields or data field. This bit is reset when updated.
4	Record not found error	When set, this bit means that a data address mark was not found within 43 bytes of the last ID field CRC byte; or it can indicate that the desired track, sector, or side was not found.
5	Record type	This bit reflects the type of data mark that was encountered during the read. When set, a deleted data mark was found. If clear, a data mark was encountered.
6		Always set to 0.
7	Not ready	Same as type I not ready status bit.

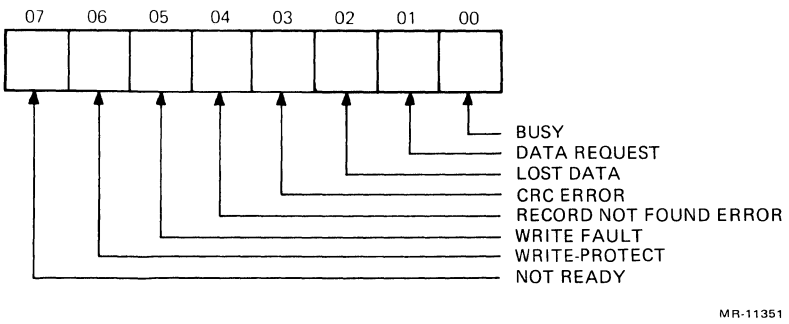


Figure 5-6 Type II Write Sector Status Register Format

Table 5-11 Type II Write Sector Status Register Bit Description

Bit	Name	Description
0	Busy	Same as type I status busy bit.
1	Data request	When set, this bit means that the data register is empty, and it is waiting for the CPU to write the register.
2	Lost data	When set, this bit means that data register had not been written within 23.0 μs and the data on the diskette is not valid (zero bytes are substituted for data lost).
3	CRC error	When set, this bit indicates an error in one or more ID fields. This bit is reset when updated.
4	Record not found error	When set, this bit means that the desired track, sector, or side was not found.
5	Write fault	Not implemented; should always be zero.
6	Write-protect	When this bit is set after a write command, an attempt was made to write on a write-protected diskette.
7	Not ready	Same as type I not ready status bit.

5.4.1.5 FDC Track Register (Read/Write) Address 61H – This read/write 8-bit register holds the updated address of the current read/write head position. It is incremented by one every time the head is stepped in (towards track 79) and decremented by one every time the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during diskette read, write, and verify operations.

5.4.1.6 FDC Sector Register (Read/Write) Address 62H – This read/write 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during diskette read and write operations.

5.4.1.7 FDC Data Register (Read/Write) Address 63H – This 8-bit register is used as a holding register during diskette drive read and write operations. In diskette read operations, the assembled data byte is

transferred in parallel to the data register from the data shift register. In diskette write operations, the data byte is transferred in parallel from the data register to the data shift register.

When executing a seek command, the data register holds the address of the desired track position.

5.4.1.8 Formatter/Controller Register Delays – Because of internal synchronization cycles, certain time delays must be introduced when operating under programmed I/O. The delays required for formatter/controller register-to-register accesses are listed in Table 5-12.

Table 5-12 Formatter/Controller Register Delays

Operation	Next Operation	Delay Required (microseconds)
Write to command register	Read busy bit (FDC status register bit 0)	12
Write to command register	Read status bits <7:1>	28
Write to any register	Read from a different register	No delay
Write to track, sector, or data register	Read from same register	8
Write to any register	Write to another register	14
Interrupt register	Read status register	4

5.4.1.9 Data Shift Register – This 8-bit register assembles serial data from the read data (RD) input during read operations and transfers serial data to the write data (WD) output during write operations.

5.4.1.10 CRC Logic – This logic is used to check or generate the 16-bit cyclic redundancy check (CRC). The polynomial is: $G(x) = X^{16} + X^{12} + X^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

5.4.1.11 Arithmetic Logic Unit (ALU) – The ALU is a serial comparator, incrementer, and decrementer. It is used for register modification and comparisons with the diskette recorded ID field.

5.4.1.12 AM Detector – The address mark (AM) detector detects ID, data, and index address marks during read and write operations.

5.4.1.13 Formatter/Controller Pin Descriptions – The 40 pins of the formatter/controller can be divided into the following three functional groups:

1. Z80A processor interface
2. Diskette drive interface
3. Power inputs and master reset

The pin functions are described in Table 5-13.

Table 5-13 Formatter/Controller Pin Descriptions

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
1		NC		Pin 1 is internally connected to a back bias generator and must be opened by the user.
19	ZRESET L	RESET	I	Z80A RESET: This low input from the 8088 diagnostic write register resets the formatter controller, loads 03H into the command register, and resets the not ready (status bit 7). When ZRESET goes high (1), a restore command is executed regardless of the state of the ready signal from the diskette drive and 01H is loaded into the sector register.
20	GND	VSS	I	DC power ground
21	+5 V	VCC	I	+5 V power input
40	+12 V	VDD	I	+12 V power input
Z80A Processor Interface				
2	ZFPWR L	WE	I	Z80A DISKETTE DRIVE WRITE: A logic low (0) on this input gates data on ZD<7:0> into the selected register when pin 3 (CS) is low.
3	CS	CS	I	CHIP SELECT: A logic low (0) on this input selects the chip and enables Z80A communication with the formatter/controller. This signal is tied to ground in the Rainbow 100 computer.
4	ZFPRD L	RE	I	Z80A DISKETTE DRIVE READ: A logic low (0) on this input controls the placement of data from a selected register on the ZD<7:0> bus when pin 3 (CS) is low.
5,6	ZA<1:0>	A1, A0	I	Z80A ADDRESS BITS <1:0>: The address bits select the register to receive/transfer data on the ZD<7:0> lines under ZFPRD and ZFPWR control:

ZA<1>	ZA<0>	ZFPRD	ZFPWR
0	0	status reg.	command reg.
0	1	track reg.	track reg.
1	0	sector reg.	sector reg.
1	1	data reg.	data reg.

*I = Input, 0 = Output, I/O = Input/Output

Table 5-13 Formatter/Controller Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
14–7	ZD<7:0>	DAL7, DAL0	I/O	Z80A DATA BUS: The formatter/controller transmits or receives data, control, and status information over this 8-bit bidirectional bus when enabled by ZFPWR or ZFPRD.
24	1 MHZ	CLK	I	1 MHZ CLOCK: This input is a free-running clock for internal timing reference.
38	DRQ	DRQ	O	DATA REQUEST: This open drain output indicates that the data register contains assembled data in read operations, or the data register is empty in write operations. This signal is reset when serviced by the Z80A reading or writing the data register.
39	IRQ	INTRQ	O	INTERRUPT REQUEST: This open drain output is set at the completion of any command and is reset when the status register is read or the command register is written.
Diskette Drive Interface				
15	STEP H	STEP	O	STEP: This 2 μs pulse is an output to the diskette drive. For every step pulse issued, the diskette drive moves the read/write one track location in the direction specified by the direction output.
16	DIR H	DIR	O	DIRECTION: This signal goes high (1) when the read/write head is stepping in and low (0) when the read/write head is stepping out.
17	EARLY H	EARLY	O	EARLY: When this signal is high (1), the write data pulse is shifted early for write precompensation.
18	LATE H	LATE	O	LATE: When this signal is high (1), the write data pulse is shifted late for write precompensation.
22		TEST	I	TEST: This signal is not used by the Rainbow 100 computer. It is tied to +5 V.
23	HLT H	HLT	I	HEAD LOAD TIMING: When this signal goes high (1), the formatter/controller assumes that the read/write head is loaded, and the drive motor has come up to speed.

*I = Input, 0 = Output, I/O = Input/Output

Table 5-13 Formatter/Controller Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
25	RG H	RG	O	READ GATE: This signal goes high (1) when the formatter/controller encounters the sync field in the read data. It allows the data separator circuit to synchronize on the incoming data.
26	RD CLK	RC	I	READ CLOCK: This signal is derived from the incoming raw data stream by the data separator circuit.
27	RD	RD	I	READ DATA: This signal is derived from the incoming raw data stream by the data separator circuit.
28	HLD H	HLD	O	HEAD LOAD: This signal controls the loading of the read/write heads against the diskette surface, and enables drive selection.
29	TG43 H	TG43	O	TRACK GREATER THAN 43: When high (1), this signal informs the diskette drive that data is to be written to or read from tracks 44–79. This output is valid only during read and write commands.
30	WG H	WG	O	WRITE GATE: This signal goes high (1) before writing data to the diskette.
31	WD	WD	O	WRITE DATA: This signal is the 500 ns write pulse to the diskette drive. WD contains the unique address marks as well as data and clocks.
32	READY H	RDY	I	READY: When this signal from the diskette drive goes high (1), it indicates that read/write commands can be executed. If READY is low, the read or write operation is not performed and the formatter/controller generates an interrupt request (IRQ). Type I commands are performed regardless of the state of READY. The READY input appears in inverted format as bit 7 of the status register.
33	VFOE L	WF/VFOE	O	VFO ENABLE: This signal enables the data separator. It is valid when WG = 0. VFOE will go low (0) during a read operation after the head has loaded (HLT = 1), and will remain low until the end of a data field.

*I = Input, 0 = Output, I/O = Input/Output

Table 5-13 Formatter/Controller Pin Descriptions (Cont)

Pin No.	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
34	TR00	TR00	I	TRACK ZERO: This signal informs the formatter/controller that the read/write head is positioned over track 0.
35	IP	IP	I	INDEX PULSE: This signal informs the formatter/controller when the index hole is encountered on the diskette.
36	WR PRT	WP	I	WRITE PROTECT: This signal is sampled whenever a write command is received. When low (0), this signal terminates the command and sets the write-protect status bit 6.
37	DDEN L	DDEN	I	DOUBLE DENSITY ENABLE: When this signal is low (0), the formatter/controller operates in double density mode. This signal is tied to ground in the Rainbow 100 computer.

*I = Input, 0 = Output, I/O = Input/Output

5.4.2 Data Separator

The data separator circuit receives the raw serial data input from the diskette drive and produces read data (RD) pulses whose leading edges ideally fall within a read clock (RD CLK) window. The RD CLK window occurs at a nominal frequency of 250 kHZ and is used to strobe each RD pulse into the formatter/controller. Figure 5-7 shows the relation between the data separator, incoming data, and the formatter/controller.

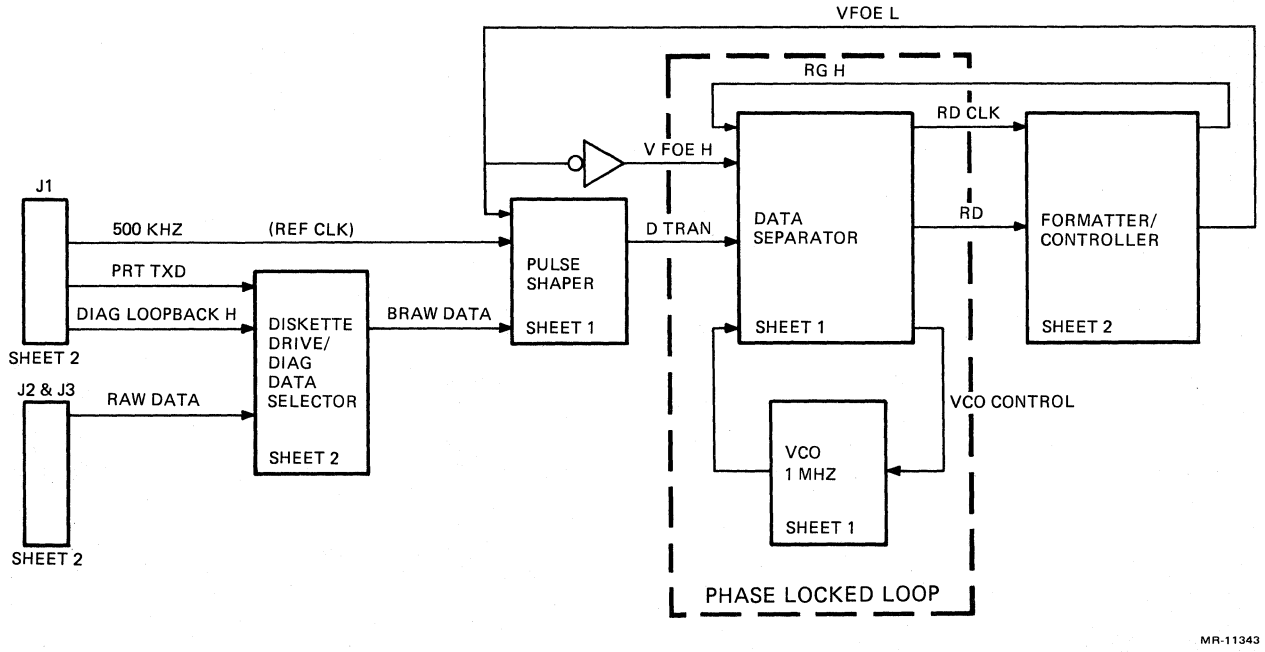


Figure 5-7 Data Separator Block Diagram

Diskette drive motor speed variation, bit shifts, and diskette drive read amplifier recovery circuits all cause the RAW DATA pulses to drift away from their nominal positions. As this occurs, the RAW DATA pulses will shift left or right with respect to RD CLK. Eventually, a data pulse will make its transition outside of its RD CLK window, causing either a CRC error or a record-not-found error at the formatter/controller.

The phase lock loop (PLL) circuit (data separator and VCO) prevents this undesirable condition from occurring. The PLL provides synchronization between the RD CLK and RD signals. As RAW DATA pulses are fed to the PLL, the data separator provides a varying dc signal to make minor adjustments to the nominal 1 MHZ voltage controlled oscillator (VCO) frequency. If the RAW DATA pulses are occurring too far apart, the RD CLK frequency is decreased to keep the RD pulses in the center of the RD CLK window. If the RAW DATA pulses begin occurring too close together, RD CLK frequency is increased until this new higher frequency is reached. In normal read operation, the PLL constantly adjusts the RD CLK frequency in an attempt to match the RAW DATA frequency.

The variable frequency oscillator enable (VFOE) signal is an output from the formatter/controller that signifies that the head has been loaded and valid data pulses are occurring on the RAW DATA line. It is used to enable the data separator and to prevent random pulses from producing an erratic RD CLK signal when the diskette drive head is disengaged.

The read gate (RG) signal from the formatter/controller is used to inform the PLL to synchronize to the incoming read data. RG goes high (1) when the formatter/controller detects the four sync bytes in the sync field. The formatter controller must then find an address mark within the next 16 bytes; otherwise, RG is reset and the formatter/controller continues searching for sync bytes in the incoming data stream.

After the data field of the target sector has been read or a time-out error occurs, the formatter/controller unasserts the VFOE signal. This enables the phase lock loop to lock on to a 500 kHZ signal (REF CLK) and stay within the capture range of the VCO for the next read cycle.

The RX50 controller module aiso contains a diskette drive/diagnostic data selector that provides a means to test the PLL circuit without a diskette drive being connected to the system. It is used during diagnostic testing to determine if read errors are due to a fault in the data separator circuit or the diskette drive.

During normal operation, the RAW DATA pulses from the diskette drives are routed through the data selector to a 300 ns pulse shaper and then to the data separator.

During diagnostic testing, the DIAG LOOPBACK signal goes high (1) to allow the printer transmit data (PRT TXD) from the printer MPSC to simulate a track of MFM data and clocks. The formatter/controller receives the simulated MFM data and forwards it to the Z80A processor, which verifies that the RX50 controller received the same data that was sent by the 8088 processor.

5.4.3 Write Precompensation

The MFM recording method produces an undesirable shifting of the peaks of adjacent flux transitions on the diskette that causes them to move from the position where they were written. The write precompensation circuit shifts the write data in a direction opposite to that expected by the peak shift of the read voltage waveforms as a result of the MFM encoding. Figure 5-8 shows binary data encoded into MFM format and Figure 5-9 shows how the diskette flux reversals shift the peaks of the composite read waveform.

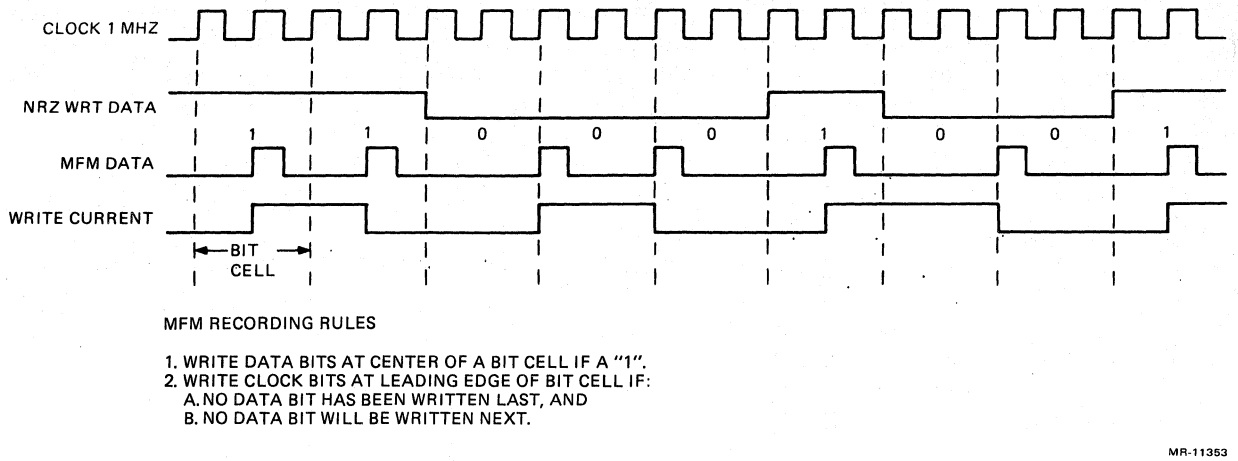


Figure 5-8 MFM Encoding

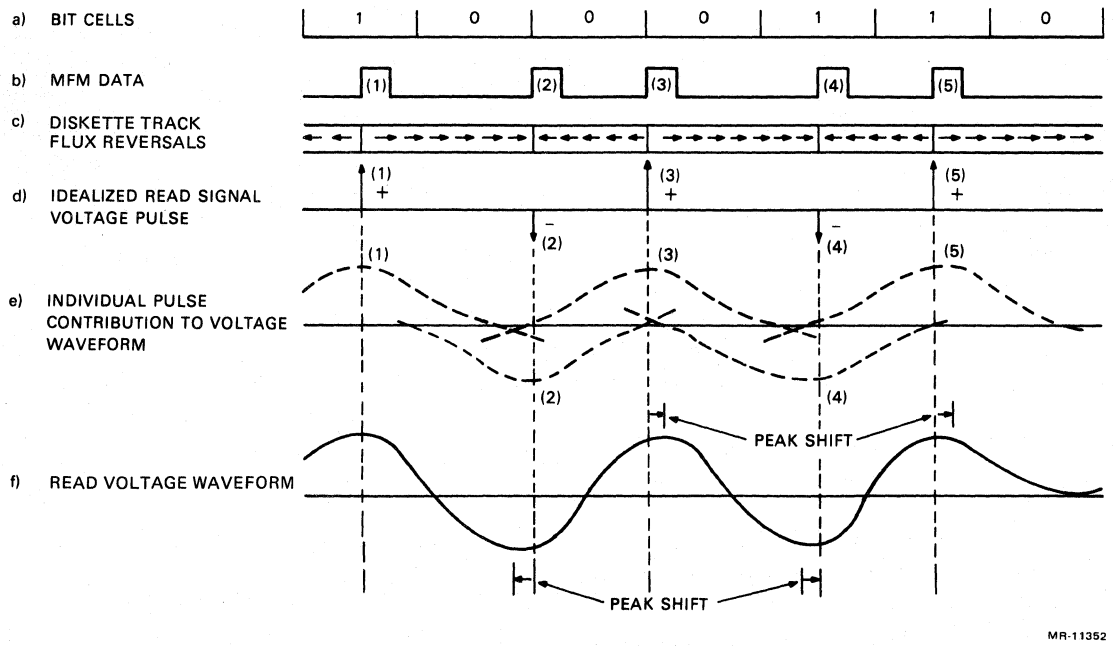


Figure 5-9 Peak Shift Waveform

The write precompensation circuit consists of a 256 × 4 bit precompensation ROM, a 3-bit latch, a write data bit latch, and a data shaper. Figure 5-10 shows the relation of the write precompensation circuit to the formatter/controller and the diskette drive connectors.

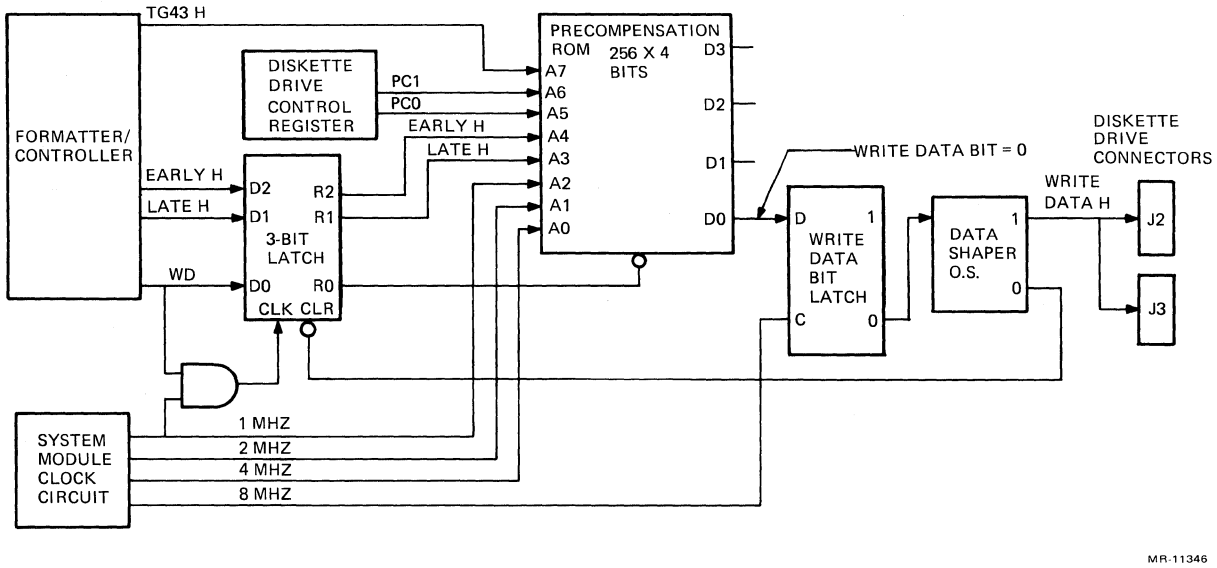


Figure 5-10 Write Data Precompensation

The formatter/controller provides three signals to select the write data precompensation value. Write data (WD), EARLY, and LATE are clocked into a 3-bit latch by 1 MHz clock pulses from the system module clock circuit. The formatter/controller asserts EARLY or LATE at least 125 ns before or after the write data pulse. An algorithm internal to the formatter/controller decides whether to assert EARLY or LATE depending on the previous bit pattern sent.

The write precompensation delay values are stored in tabular form in the precompensation ROM in address locations specified by TG43, PC1, PC0, EARLY, LATE, and the 1, 2, and 4 MHz clocks. The 1, 2, and 4 MHz clocks step through the addresses at 125 ns intervals until an address location containing a "0" in the D0 bit is encountered.

When D0 = 0, the write data bit latch will output a positive pulse to trigger a one-shot data shaper. The data shaper sends the 500 ns precompensated write data pulse to the diskette drive connectors (J2 and J3) and at the same time clears the 3-bit latch.

5.4.4 Diskette Drive Select Logic

The diskette drive select logic provides a diskette select signal and a drive motor on signal to activate any one of four drives (A, B, C, or D) when data is to be written to or read from a diskette. Diskette drive unit 0 contains drives A and B, and the optional diskette drive unit 1 contains drives C and D. The diskette drive select block diagram is shown in Figure 5-11.

The Z80A processor controls the selection of the drive and turns on the diskette drive motor by writing to the diskette drive control register at address 40H via the ZD<7:0> bus. DS0 H (bit 0) and DS1 H (bit 1) of the diskette drive control register are sent to the diskette drive select and decoder circuit. These bits are decoded when the diskette drive select and decoder circuit is enabled by either the MOTOR O ON H (bit 3), MOTOR 1 ON H (bit 4), or the head load (HLD H) signal from the formatter/controller. Table 5-14 lists the drive selected as a result of decoding the DS0 and DS1 bits.

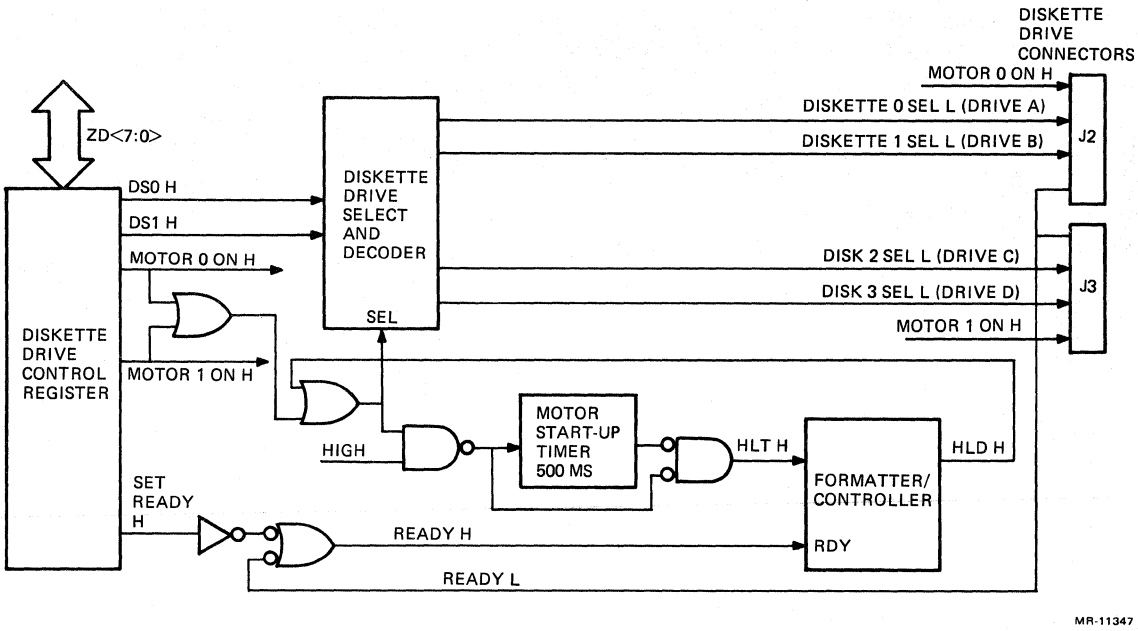


Figure 5-11 Diskette Drive Select Block Diagram

Table 5-14 Drive Select Decoding

DS1	DS0	SEL	Drive A*	Drive B	Drive C	Drive D
0	0	0	1	1	1	1
0	0	1	0	1	1	1
0	1	1	1	0	1	1
1	0	1	1	1	0	1
1	1	1	1	1	1	0

* 0 = Drive selected
1 = Drive deselected

The drive motor in diskette drive 0 and 1 can be turned on by the MOTOR O ON H and MOTOR 1 ON H signals from the diskette drive control register or the HLD H signal from the formatter/controller. The motor on signals are sent directly to the diskette drives and also through an "OR" gate to the select input of the diskette drive select and decoder circuit. This arrangement is necessary to ensure that the motor in the drive selected by DS0 and DS1 will be turned on before the read/write head is loaded. The read/write head is loaded when the DISK 0, 1, 2, or 3 SEL signal goes low.

The select signal for the diskette drive select and decoder circuit can also be asserted high by HLD H from the formatter/controller. HLD is asserted at the beginning of a type I command if the head load flag is set (h=1), at the end of a type I command if the verify flag is set (V=1), or upon receipt of any type II or III command. Once HLD is asserted, it remains asserted until either a type I command is received (h = 0, v = 0); or if the formatter/controller is in an idle state (not busy) and 15 index pulses have occurred.

The diskette drive select circuit also contains a 500 ms motor start-up timer that generates the head load timing (HLT H) signal to inform the formatter/controller that the read/write head has been loaded. The motor start-up timer is a one shot that is triggered by either MOTOR 0 or 1 ON bit or HLD H. The motor start-up timer delays the start of a second selected drive motor for 500 milliseconds after the start of the first drive motor. While the first drive motor is on, the 500 millisecond timer is unusable for a second drive unless the first drive motor is turned off. The second drive motor has to be timed by the program if the first drive motor is on. This delay is necessary to ensure that the selected drive motor is rotating at the correct speed before reading from or writing to the diskette.

The SET READY H (bit 2) signal from the diskette drive control register is used during diagnostic testing to override the READY L signal from the diskette drive.

NOTE

If MOTOR 1 ON is active and drive A or B is enabled at the same time, both motors turn on simultaneously.

5.4.4.1 Diskette Drive Ready Status – The Z80A processor monitors the status of the READY L line from the diskette drive to determine if the drive is ready for a read or write operation. READY L is sent directly to the general/diagnostic status register and through an "OR" gate to the formatter/controller under the following conditions:

- The diskette drive is selected, and
- A diskette is present in the diskette drive and the door is closed. The diskette drive motor does not have to be up to speed.

The ready condition for the formatter/controller can be made valid by the following conditions:

- The diskette drive is actually in a ready state (READY L asserted) or
- The SET READY H bit in the diskette drive control register has been set by software.

5.4.4.2 Diskette Drive Select Light Operation – The front bezel of each diskette drive unit contains two head load lights to inform the operator that the diskette drive is active. The diskette must not be removed while these lights are on.

During power-up, the INIT L signal from the system module initializes the drive select logic and deselects all drives. Each light will be turned on by the select logic in the diskette drive when the following conditions exist:

- The spindle motor is operating.
- A diskette is inserted and the door is closed.
- The diskette drive side is selected.

5.4.5 Diskette Status Register (Read Only) Address 40H

This eight-bit read-only register holds the status of control signals coming from the formatter/controller and going to the RX50 diskette drive. The status bits are gated onto the ZD<7:0> bus when the Z80A I/O select decoder asserts ZFP REG RD L. The format of the status register bits is shown in Figure 5-12, and the bits are described in Table 5-15.

5.4.6 Diskette Control Register (Write Only) Address 40H

This eight-bit write-only register holds control bits used to select the diskette drives and precompensation values for the write data. The control bits are gated into the control register from the ZD<7:0> bus when the Z80A I/O select decoder asserts ZFP REG WR L. The format of the diskette control register is shown in Figure 5-13 and the bits are described in Table 5-16.

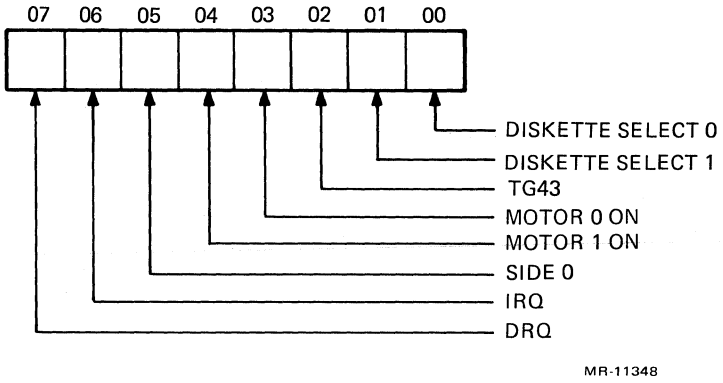


Figure 5-12 Diskette Status Register Format

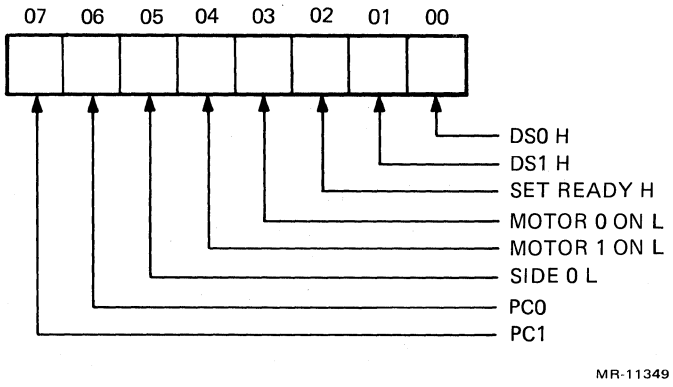


Figure 5-13 Diskette Control Register Format

Table 5-15 Diskette Status Register Bit Description

Bit	Name	Description
0,1	DISKETTE SELECT	These bits read back the status of bits 0 and 1 from the diskette drive control register. They indicate which drives have been selected. They are encoded as follows: **Bit 1** **Bit 0** **Drive Selected** 0 0 Drive 0 0 1 Drive 1 1 0 Drive 2 1 1 Drive 3
2	TRACK GREATER THAN 43	This bit reflects the status of the TG43 signal from the formatter/controller going to the diskette drive. When 0, it indicates that the read/write head is positioned on a track greater than 43.
3	MOTOR 0 ON	This bit reflects the status of the MOTOR 0 ON line at the diskette drive connector J2. When 0, it indicates that the MOTOR 0 ON bit is set.
4	MOTOR 1 ON	This bit reflects the status of the MOTOR 1 ON line at the diskette drive connector J3. When 0, it indicates that the MOTOR 1 ON bit is set.
5	SIDE SELECT	This bit reflects the status of the side select signal at diskette drive connectors J2 and J3. When high (1), side 0 of the diskette is selected.
6	INTERRUPT REQUEST	This bit reflects the status of the IRQ signal coming from the formatter/controller. It is set (1) at the completion of any command and reset (0) when the FDC status register is read or the FDC control register is written to.
7	DATA REQUEST	This bit reflects the status of the DRQ bit from the formatter/controller. When high (1), indicates that the formatter/controller has read data to be transferred or requires new write data.

Table 5-16 Diskette Control Register Bit Description

Bit	Name	Description
0,1	DISKETTE SELECT	These bits control the selection of the diskette drives. The binary value written to them (0–3) selects drive 0 through 3. Only one drive can be selected at a time.
2	SET READY	This bit is used during diagnostic testing to override the READY L signal from the diskette drive. When this bit is set, it informs the formatter/controller that a read or write operation can be performed.
3	MOTOR 0 ON	This bit controls the MOTOR 0 ON bit. When set (1), it turns on the motor in the first drive unit.
4	MOTOR 1 ON	This bit controls the MOTOR 1 ON bit. When set (1), it turns on the drive motor in the second drive unit.
5	SIDE 0	This bit selects the side of the diskette to be accessed. For single-sided drives, this bit is always set to 0 for side 0 of the diskette.
6,7	PC0, PC1	These binary bits are used to control the write delay precompensation values. The following table lists the values available.

TG43	PC1	PC0	Delay (ns)
0	0	0	125
0	0	0	125
0	0	0	125
0	0	0	125
1	0	0	250
1	0	0	375
1	0	1	375
1	0	1	375

5.4.7 General/Diagnostic Status Register (Read Only) Address 21H

This eight-bit read-only register holds the status of control signals from the formatter/controller to the diskette drive and input signals from the diskette drive. Bits <2:0> of this register are used by the Z80A processor to monitor the status of interprocessor interrupts and are described in Chapter 4, Paragraph 4.4.10.1. The status bits are gated onto the ZD<7:0> bus when the Z80A I/O select decoder asserts ZDIAG RD L. The format of the general/diagnostic register bits is shown in Figure 5-14 and the bits are described in Table 5-17.

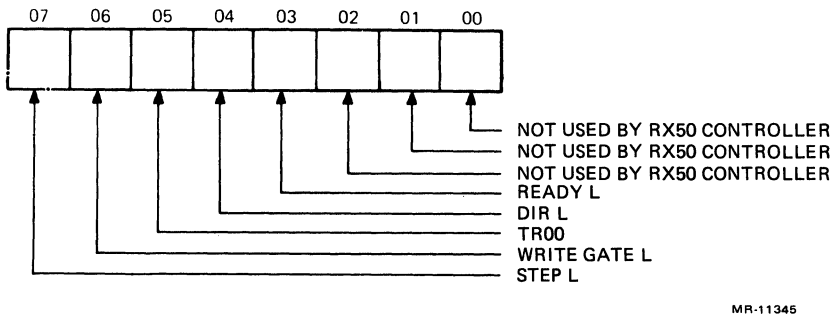


Figure 5-14 General/Diagnostic Status Register Format

Table 5-17 General/Diagnostic Status Register Bit Description

Bit	Name	Description
0	ZFLIP L	Not used by RX50 controller module
1	INTZ80 L	Not used by RX50 controller module
2	INT88 L	Not used by RX50 controller module
3	READY L	This bit reflects the status of READY signal from the diskette drive. The diskette drive asserts this signal when a diskette is inserted and the door is closed.
4	DIR L	This bit reflects the status of the DIRECTION signal from the formatter/controller to the diskette drive. When high (1), the read/write head will step toward the center of the diskette. When low (0), the read/write head will step away from the center of the diskette.
5	TR00	This bit reflects the status of the TRACK 0 signal coming from the diskette drive. When high (1), it indicates that the read/write head is on track 0.
6	WRITE GATE L	This bit reflects the status of the WRITE GATE signal from the formatter/controller to the diskette drive. When low (0), data can be written to the diskette.
7	STEP L	This bit reflects the status of the STEP signal from the formatter/controller to the diskette drive. The read/write head will step from one track to the next for each STEP pulse. The direction in which the head will step is determined by the state of the DIRECTION signal.

5.5 RX50 CONTROLLER MODULE CONNECTORS

The RX50 controller module contains one 40-pin connector (J1) and two 34-pin connectors (J2 and J3). Connector J1 carries address, data, and control information between the RX50 controller module and the system module. Connectors J2 and J3 carry control, status, and read and write data signals between the RX50 controller module and the diskette drive(s). If the system contains a single diskette drive unit, it must be connected to connector J2. When an optional diskette drive unit is installed, it is connected to connector J3. All signals, except three, are wired to J2 and J3 in parallel.

The signals on connector J1 are described in Table 5-18 and those for J2 and J3 are described in Table 5-19.

Table 5-18 RX50 Controller Connector (J1) Signals

Pin*	Signal	Mnemonic	Description
1	DISKETTE DRIVE READ	ZFPRD L	This input signal asserted by the Z80A I/O select logic allows the RX50 controller to place read data from the diskette drive onto the Z80A data bus (ZD<7:0>).
2	PRINTER TRANSMITTED DATA	PRT TXD	This input signal is a serial stream of data from the printer MPSC. This data is sent to the data separator circuit when DIAG LOOPBACK H is asserted and allows the 8088 and Z80A processors to test the data separator circuits without the use of a diskette drive.
3	DISKETTE DRIVE WRITE	ZFPWR L	This input signal asserted by the Z80A I/O select logic gates data from the Z80A data bus ZD<7:0> into the selected formatter/controller register.
4	DIAGNOSTIC LOOPBACK	DIAG LOOPBACK H	This input signal, together with PRT TXD, allows the data separator circuit to be tested through the printer port.
5	Z80A RESET	ZRESET L	This input signal will reset the RX50 controller at power-up.
7	AC VOLTAGE OKAY	BACOK H	This input signal allows the RX50 controller to transfer write data to the diskette drive only when the ac input to the power supply is at the correct voltage level.

*Pins not listed are not used by the RX50 Controller Module.

Table 5-18 RX50 Controller Connector (J1) Signals (Cont)

Pin*	Signal	Mnemonic	Description
9	DISKETTE DRIVE REGISTER READ	ZFPREG RD L	This input signal asserted by the Z80A I/O select logic allows the Z80A to read the status of the diskette drive.
10	+5 V		+5 V input
11	Z80A DATA BIT 7	ZD7	This bidirectional data bus bit is used to transfer data, control, and status information between the Z80A and the RX50 controller.
12	Z80A ADDRESS BIT 0	ZA0	Address bit 0, together with address bit 1, selects one of five registers in the RX50 controller to transmit/receive data on the ZD<7:0> bus.
13	Z80A DATA BIT 6	ZD6	This bidirectional data bus bit is used to transfer data, control, and status information between the Z80A and the RX50 controller.
14	GROUND	GND	Signal and power ground
15	Z80A DATA BIT 5	ZD5	These bidirectional data bus bits are used to transfer data, control, and status information between the Z80A and the RX50 controller.
17	Z80A DATA BIT 4	ZD4	
19	Z80A DATA BIT 3	ZD3	
21	Z80A DATA BIT 2	ZD2	
23	Z80A DATA BIT 1	ZD1	
24	GROUND	GND	Power and signal ground.
25	Z80A DATA BIT 0	ZD0	This bidirectional data bus bit is used to transfer data, control, and status information between the Z80A and the RX50 controller.
26	Z80A ADDRESS BIT 1	ZA1	Address bit 1 together with address bit 0 selects 1 of 5 registers in the RX50 controller to transmit/receive data on the ZD<7:0> bus.

*Pins not listed are not used by the RX50 Controller Module.

Table 5-18 RX50 Controller Connector (J1) Signals (Cont)

Pin*	Signal	Mnemonic	Description
27	8 MHZ CLOCK PULSE	08A	This clock pulse signal is used by the write precompensation circuit in the RX50 controller.
29	4 MHZ CLOCK PULSE	4 MHZ	This clock pulse signal is used by the write precompensation circuit in the RX50 controller.
30	+5 V		+5 V input
31	2 MHZ CLOCK PULSE	2 MHZ	This clock pulse signal is used by the write precompensation circuit in the RX50 controller.
32	+12		+12 V input
33	1 MHZ CLOCK PULSE	1 MHZ	This clock pulse signal is used by the write precompensation circuit in the RX50 controller.
34	+12		+12 V input
35	500 KHZ CLOCK PULSE	500 KHZ	This clock pulse signal is used by the data separator circuit in the RX50 controller.
36	−12 V		−12 V input
37		ZFPREG WR L	This output signal asserted by the Z80A I/O select logic enables a write-only control register in the RX50 controller. The contents of the register are used to select the drive, turn on the drive motor, write the precompensation values, and select the surface of the diskette to be accessed.
38	DISKETTE DRIVE PRESENT	FLPY PRES L	This output signal informs the 8088 that the RX50 controller is installed.
39	DIAGNOSTIC READ	ZDIAG RD L	This input signal asserted by the Z80A I/O select logic enables the general/status register on the RX50 controller to place diskette drive status information on the ZD<7:0> data bus.

*Pins not listed are not used by the RX50 Controller Module.

Table 5-19 RX50 Controller Connector J2 and J3 Signals

Pin* J2	J3	Signal	Mnemonic	Description
2	2	TRACK GREATER THAN 43	TG43	This output informs the diskette drive that the read/write head is positioned between tracks 44–79. This output is valid only during read and write commands.
8	8	INDEX PULSE	IP	This input informs the formatter/controller when the index hole in the diskette is encountered. Minimum pulse width is 20 microseconds. This signal indicates the start of a diskette track.
10		DISK 0 SELECT	DISK 0 SEL L	When this output is asserted low, diskette drive A is selected for read or write operations.
	10	DISK 2 SELECT	DISK 2 SEL L	When this output is asserted low, diskette drive C is selected for read or write operations.
12		DISK 1 SELECT	DISK 1 SEL L	When this output is asserted low, diskette drive B is selected for read or write operations.
	12	DISK 3 SELECT	DISK 3 SEL L	When this output is asserted low, diskette drive D is selected for read or write operations.
16		DRIVE MOTOR 0 ON	MOTOR 0 ON L	When this output is asserted low, the spindle motor in diskette drive unit 0 (drives A and B) is turned on.
	16	DRIVE MOTOR 1 ON	MOTOR 1 ON L	When this output is asserted low, the spindle motor in diskette drive unit 1 (drives C and D) is turned on.
18	18	DIRECTION	DIR L	When this output signal is low, the read/write head will step towards the center of the diskette. When high, the read/write head will step away from the center of the diskette.
20	20	STEP PULSE	STEP L	When this 2 microsecond output pulse is asserted low, the read/write head will move one track position in the direction determined by DIR L.

* Pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, and 33 are tied to ground. Pin 4 is not used.

Table 5-19 RX50 Controller Connector J2 and J3 Signals (Cont)

Pin* J2	Pin* J3	Signal	Mnemonic	Description
22	22	WRITE DATA	WRITE DATA L	This 500 ns output pulse is the data to be written on the diskette. Each transition from a logical 1 to a logical 0 causes the read/write head current to be reversed, thereby writing a data bit. This line is enabled when WRITE GATE is active.
24	24	WRITE GATE	WRITE GATE L	This output is asserted low before data can be written on the diskette.
26	26	TRACK 0	TR0 0	When asserted low, this input signal informs the formatter/controller that the read/write head is positioned over track 0.
28	28	WRITE PROTECT	WR PRT	This input is sampled whenever a write command is received. When asserted low, the command terminates and sets the write-protect status bit in the formatter/controller status register.
30	30	RAW READ DATA	RAW DATA	This input is the raw data signal from the diskette drive. This signal should be a negative pulse from a minimum of 750 ns to a maximum of 1250 ns for each flux transition.
32	32	DISKETTE SIDE 0	SIDE 0 H	When this output signal is asserted high, side 0 of the diskette is selected. This signal is always high for single surface drives.
34	34	READY	READY H	This input indicates drive readiness when low, and is sampled for a logic high before a read or write operation. This signal means that a diskette is inserted, the drive door is closed, and the drive is selected. The drive motor does not have to be turned on.

* Pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, and 33 are tied to ground. Pin 4 is not used.

5.6 SPECIFICATIONS

The following paragraphs describe the physical dimensions, power requirements, and environmental specifications for the RX50 controller module.

5.6.1 Physical Dimensions

Length	24.13 cm (9.5 in)
Width	9.90 cm (3.9 in)

5.6.2 DC Power

The dc power required by the RX50 controller module is as follows:

+5 Vdc at 475 mA typical (739 mA maximum)
+12 Vdc at 25 mA typical (30 mA maximum)
−12 Vdc at 8.4 mA typical (15 mA maximum)

5.6.3 Environmental

The RX50 controller module meets the environmental requirements of Digital Equipment Corporation standard 102, class B, and the conducted and radiation emission limits established by FCC rules for class B computing devices.

Temperature

Operating*	10° C to 40° C (50° F to 104° F)
Storage	40° C to 70° C (−40° F to 158° F)

Humidity

10% to 90% noncondensing
maximum wet bulb, 28° C (82° F)
minimum dew point, 2° C (36° F)

Altitude (maximum)

Operating Limit	2440 m (8000 ft)
Storage Limit	9144 m (30,000 ft)

* Maximum allowable temperature is reduced by 1.8° C per 1000 m (1° F per 1000 ft) above sea level.

CHAPTER 6
RX50 DISKETTE DRIVE

6.1 INTRODUCTION

The RX50 dual-diskette drive is the storage component of the RX50 controller and drive subsystem for the Rainbow™ 100 computer. Figure 6-1 shows its relationship to the other components that make up the Rainbow™ 100 computer.

6.1.1 Related Documentation

For further information, refer to the RX50 Field Maintenance Print Set (MP-01482-00).

6.1.2 General Information

The RX50 drive is a field replaceable unit (FRU PN RX50-AA) that mounts in the Rainbow™ 100 computer system unit. One cable connects the RX50 drive to a controller (see Paragraph 5.5 for a description of the signals on the RX50 controller connectors). A power cable (FRU PN 17-00281) connects the power supply to the RX50 drive.

The RX50 drive is a field replaceable part rather than a field repairable part. No adjustment or alignment procedures are provided in this chapter because of the test equipment required. The RX50 drive is adjusted and aligned at the time of manufacture.

6.1.3 Physical Description

Figure 6-2 shows the RX50 drive. The front bezel has two access slots with swinging doors to insert or remove diskettes. A head load LED at the front of each diskette slot lights when that unit is busy.

NOTE
Do not open either access door if either LED is lit.
This damages data stored on either diskette.

Internally, the drive has two counterrotating spindles. The spindles are belt driven by a single dc motor/tachometer combination.

Each diskette has a read/write (R/W) head located back-to-back between the diskettes on a head carriage assembly. The heads are positioned over each track by a single stepper motor/lead screw combination.

The electronic components are mounted on three printed circuit modules. All motors and sensors plug into these modules. The power and interface cables from the controller plug into one of the circuit modules from the top rear of the RX50 drive.

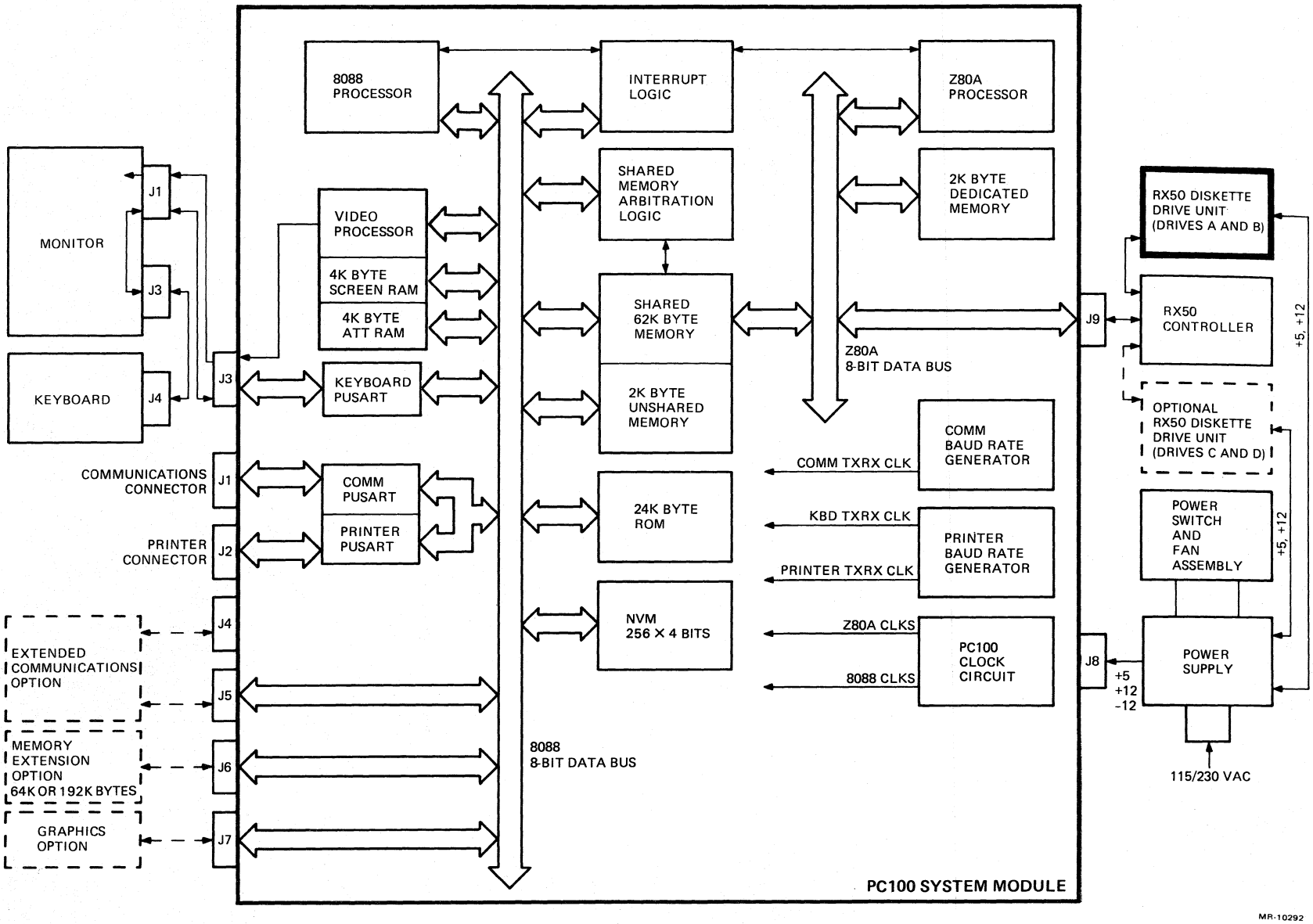


Figure 6-1 RX50 Dual-Diskette System Relation

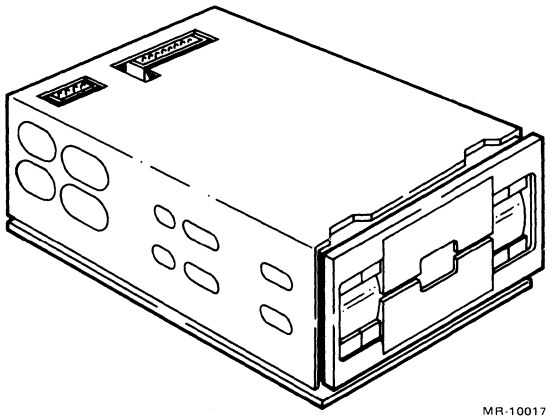


Figure 6-2 RX50 Dual-Diskette Drive

6.1.4 Diskette Description

The RX50 drive uses standard 133.4 mm (5.25 inch) square diskettes (Figure 6-3). The recording medium is a magnetic oxide coated flexible Mylar™ diskette, 130.2 mm (5.125 in) in diameter. It is contained inside a protective cover. In addition, a paper envelope is provided to protect the diskette when it is not in use.

As the medium rotates inside the cover, it is continuously cleaned by a soft fabric liner. There are four openings in the cover: one each for the spindle, the R/W head, the write-protect sensor, and the index sensor.

The write-protect opening is a small square notch along one side of the cover. When this opening is covered, the diskette is write protected. For further information see Paragraph 6.1.5.2.

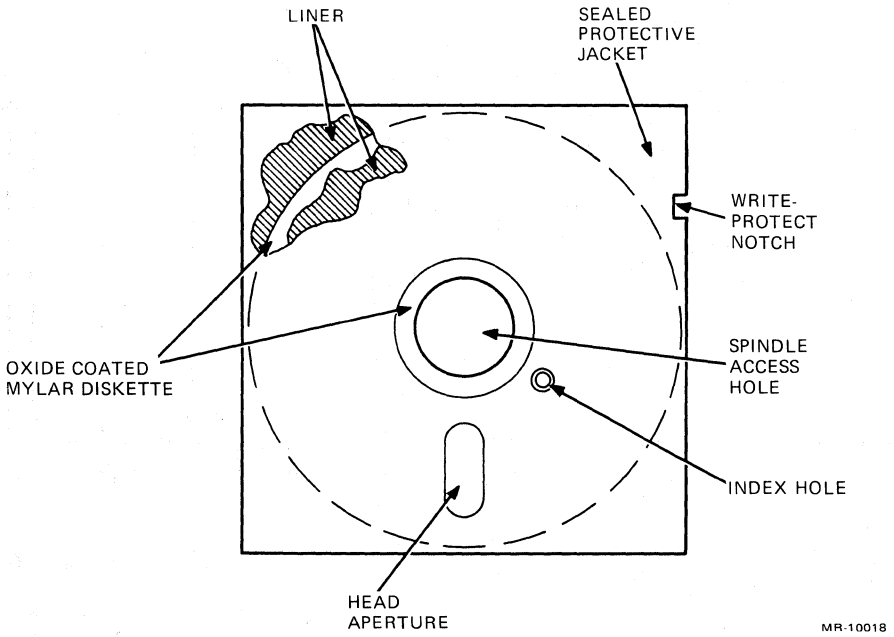


Figure 6-3 The 5-1/4 Inch Diskette

*Mylar™ is a trademark of DuPont de Nemours & Company, Inc.

6.1.5 Operating Procedures

The following paragraphs describe the diskette operating procedures.

6.1.5.1 Diskette Handling and Storage – Improper handling or storage of diskettes can destroy recorded data and damage the R/W head. The following are some suggestions for diskette handling.

- Return the diskette to its protective paper envelope when it is not installed in the RX50 drive.
- Store diskettes vertically and loosely to prevent warping.
- Use a felt tip pen to mark the diskette label. A pencil or ballpoint pen may imprint through the cover and damage the diskette inside.
- Insert the diskette into the drive carefully. Never force the door closed if it seems to be stuck. This could crush the diskette.
- Never remove or insert a diskette if either LED at the front of the diskette slots is lit.
- Never open or close the diskette door if either LED at the front of the diskette slots is lit.
- Avoid touching the Mylar recording surface where the jacket is cut away for the R/W heads. Fingerprints dirty the R/W heads and can cause data errors.
- Do not store diskettes in direct sunlight or near heaters where temperatures go above 52° C (125° F). High temperatures warp the covers.
- Never bend or fold the diskette cover.
- Never bring the diskette near any strong magnetic fields (5 gauss or more) or touch the diskette with any steel objects. This could erase or weaken the data on the diskette.

6.1.5.2 Write Protection of Diskettes – The RX50 drive is equipped with a write-protect feature that protects the diskette from accidental writing. To write-protect a diskette, cover the write-protect notch on the side of the cover. You may use adhesive-backed write-protect tabs (usually provided with diskettes) or ordinary adhesive-backed labels may be substituted. Figure 6-4 shows how to apply write-protect tabs.

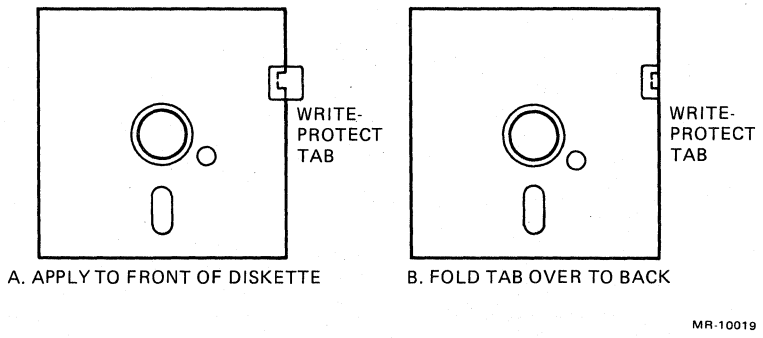


Figure 6-4 Write-Protect Tab Application

6.1.5.3 Diskette Loading/Unloading –

NOTE
Do not open either of the RX50 drive doors if either LED at the front of the diskette slots is lit.

To load a diskette into the RX50 drive, perform the following procedure:

1. Make sure that both indicators are not lit.
2. Open the door of the desired drive.
3. Align the diskette with the slot.
4. Insert the diskette until it hits a solid stop.
5. Close the door.

To open the door, press on the outer edge of the door (Figure 6-5). The diskette should be oriented so that the R/W head access slot in the cover is inserted into the drive first. The drive records on the surface of the diskette closest to the center of the drive (Figure 6-6).

To close the door, gently push the slotted edge of the door toward the center of the drive until it is flush with the front bezel (Figure 6-7). Each of the head load LEDs on the front bezel light when the controller is accessing the diskette on the indicated side.

6.1.6 Configuration Options

An RX50 dual-diskette drive can be configured to be selected by one of two groups of select signals from the controller.

One configuration of the RX50 drive requires no jumper on connector J17 (see Paragraph 6.4.5.7). This enables controller signals DRIVE SEL 0 and DRIVE SEL 1 to select circuits in the drive (see Paragraph 6.3.2.1).

The other configuration of the RX50 drive requires a jumper (PN 12-14314-00) installed on connector J17. This enables controller signals DRIVE SEL 2 and DRIVE SEL 3 to select circuits in the drive.

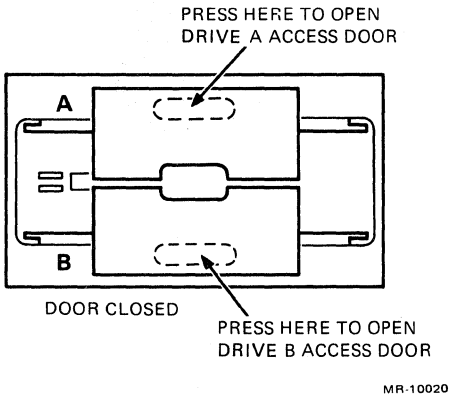


Figure 6-5 Opening Access Doors

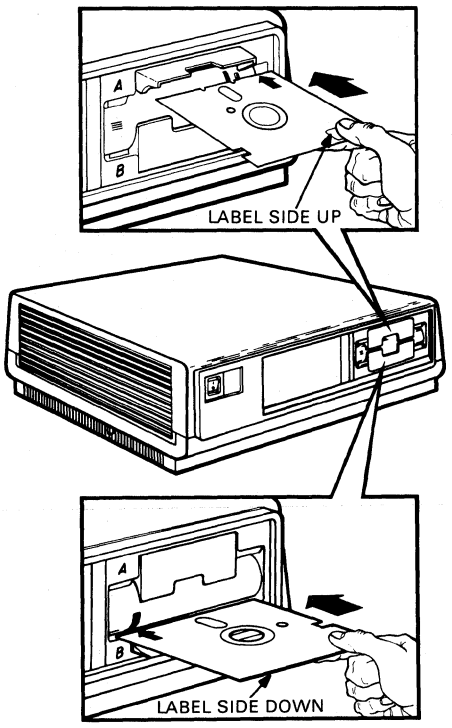


Figure 6-6 Inserting Diskette

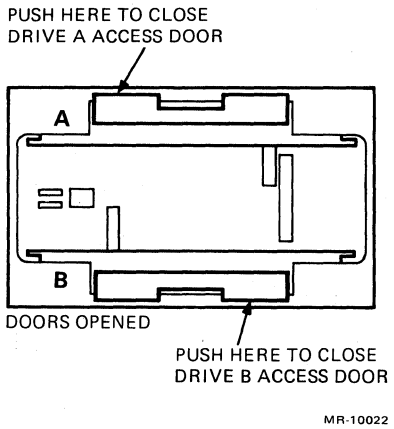


Figure 6-7 Closing Access Doors

6.2 FUNCTIONAL COMPONENTS

Figure 6-8 is a simple block diagram of the RX50 drive. It shows the general operation and data flow of the drive.

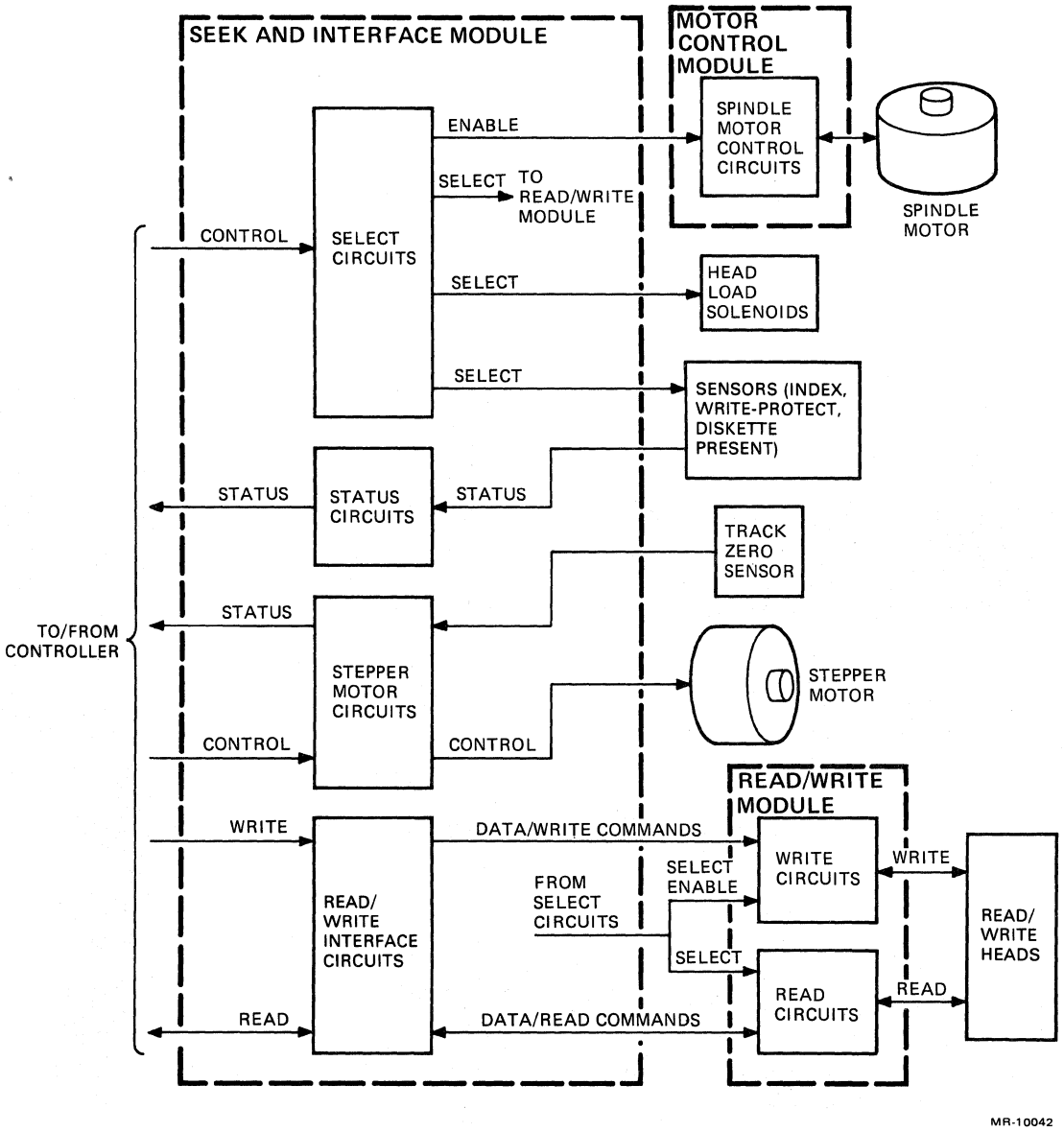


Figure 6-8 Simple Block Diagram

The RX50 drive contains the following elements to perform read, write, and seek operations:

- Seek and interface module
    - Select circuits
    - Status circuits
    - Stepper motor circuit
    - Read/write interface circuits
- Motor control module
    - Spindle motor control circuits
- Spindle motor
- Two head load solenoids
- Diskette sensors
- Stepper motor
- Read/write (R/W) module
    - Write circuits
    - Read circuits
- Two read/write heads

6.2.1 Seek and Interface Module Functions

The seek and interface module contains the following circuits:

- Select circuits
- Status circuits
- Stepper motor circuits
- Read/write interface circuits

The select circuits act as an interface between the controller and the RX50 drive. These circuits perform the following functions:

- Enable the motor control module.
- Select the head load solenoids.
- Select the sensors.
- Select and enable the circuits in the R/W module.

The status circuits interface with the sensors to the controller. These circuits pass status signals to the controller from the selected sensors.

The stepper motor circuits interface with the controller to the stepper motor. These circuits convert controller signals to stepper motor control signals.

The R/W interface circuits interface with the controller and the R/W module. For a write operation, these circuits pass data and commands from the controller to the R/W module. For a read operation, these circuits pass commands from the controller to the R/W module and data from the R/W module to the controller.

6.2.2 Motor Control Module and Spindle Motor Function

The motor control module contains spindle motor control circuits that control the rotational speed of the spindle motor. These circuits are enabled to rotate the spindle motor or disabled to stop the spindle motor by select circuits.

When enabled, these circuits provide current to the spindle motor to keep it rotating at a constant speed. When disabled, these circuits inhibit current to the spindle motor so it does not rotate.

As the spindle motor rotates, a belt drives two counter-rotating spindles. Each spindle rotates the diskette within its cover.

6.2.3 Head Load Solenoid Function

The RX50 drive contains two head load solenoids, one for each R/W head. The selected solenoid releases the head load arm and pad. This applies pressure to the surface of the medium and brings the R/W head in contact with the diskette.

6.2.4 Sensor Functions

The RX50 drive contains two groups of sensors, one group for each side. A sensor group is selected by the select circuits. Each sensor group senses the following conditions:

- The presence of a diskette
- The write protection status of a diskette
- The index of a diskette
- Track zero home position

6.2.5 Stepper Motor Function

The RX50 drive contains a stepper motor that positions R/W heads over a data track. The motor is controlled by the stepper motor circuits. As this motor rotates, a head carriage assembly, moving in a linear plane, moves the R/W heads over the diskette.

6.2.6 Read/Write Module Function

The R/W module contains both read and write circuits. The read circuits convert the analog data sensed by the R/W heads to digital data. The write circuits generate the write currents for the R/W heads to record data on the diskette.

The read circuits receive a select signal from the select circuits. The select circuits select one of the two R/W heads. A read command from the R/W interface function then enables the read circuits to pass read data to the R/W interface circuits.

The write circuits are enabled by the select circuits. The select circuits select one of the two R/W heads. The write data and commands from the R/W interface circuits then control the currents generated by the write circuits for the heads.

6.2.7 RX50 Drive Set-Up Sequence

Prior to read and write operations, the following Set-Up sequence must be performed:

1. Execute a restore unit command. This turns on the spindle motor and causes it to seek track zero.
2. Load the target track and sector registers.
3. Execute a read or write sector command. This causes the heads to load and the stepper motor to seek the target track.

6.3 THEORY OF OPERATION

The following paragraphs describe the operation of the RX50 drive.

6.3.1 Drive Mechanism Detailed Operation

The following paragraphs describe the mechanical operations of the RX50 drive. These operations use mechanisms that orient the diskettes, allow the modules to read and write to the diskette, and perform seek operations.

Figure 6-9 is an exploded view showing the mechanical detail of the drive. Figure 6-10 shows the functional detail of the drive.

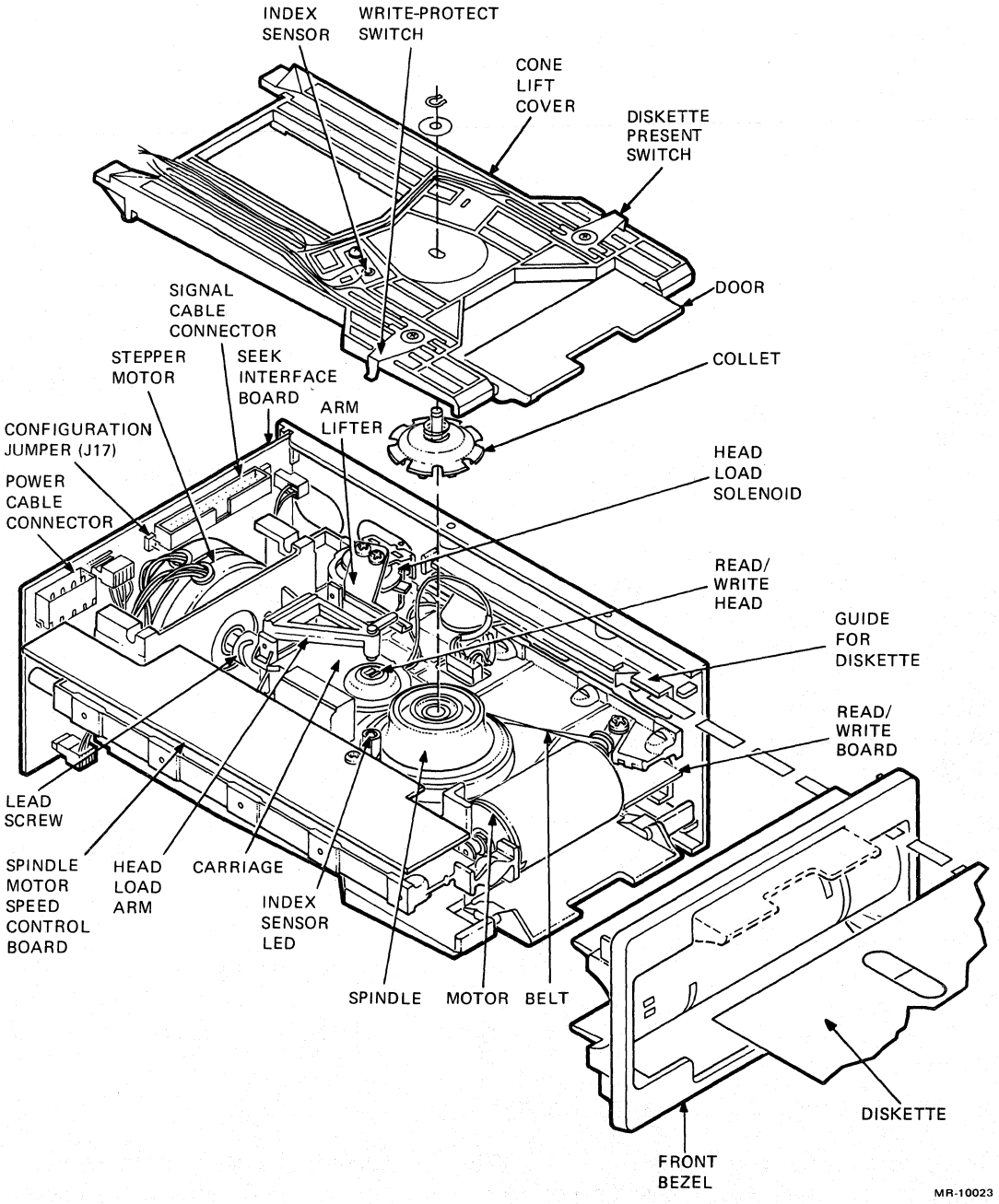


Figure 6-9 Mechanical Detail

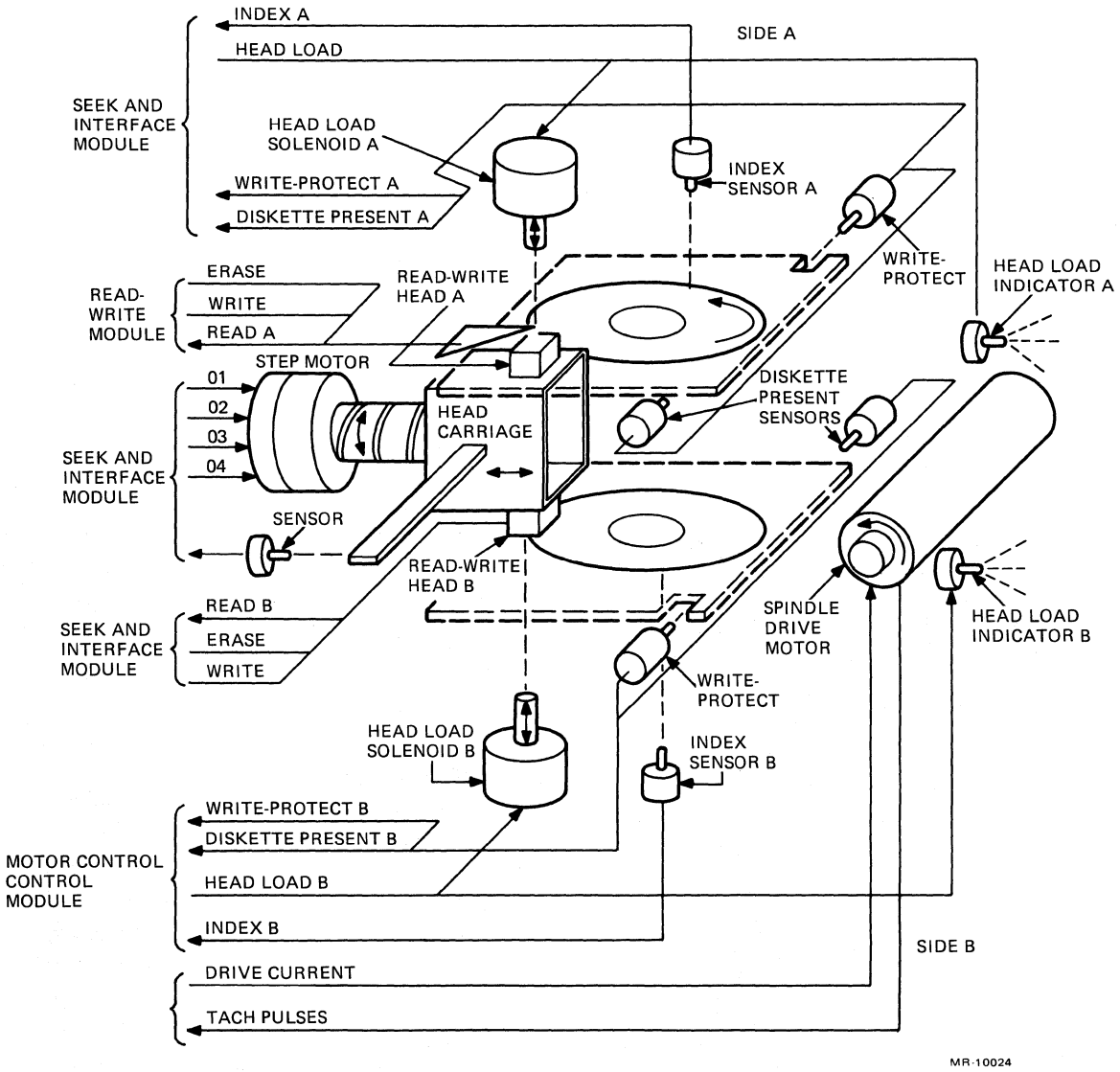


Figure 6-10 Drive Mechanism Functional Detail

6.3.1.1 Diskette Positioning Mechanism – With the door open on either side A or B, a diskette slides easily in or out of the drive on grooves. These grooves are in the drive's side panels and have a solid backstop to position the diskette.

Each door operates a cone lift cover. When the door is closed, the cone lift cover moves over the diskette. A collet, on the cone lift cover, clamps the diskette to the spindle through the diskette cover cutout.

The diskette is pressed lightly against a reference plane near the R/W head, ensuring proper head-to-diskette height. The plane pushes the soft cover liner against the diskette. This wipes the surface of the diskette clean before it comes into contact with the R/W head.

Positioning the diskette in each drive side brings two switches in contact with the diskette. The switches pass status information, disk presence, and write protection to the seek and interface module. For further information see Paragraph 6.3.1.5.

6.3.1.2 Spindle Drive Mechanism – The drive contains two counterrotating spindles, one for each drive side. A single 12 Vdc spindle motor/tachometer combination drives the spindles with a belt. The motor operates at 1800 r/min while the spindles rotate at 300 r/min.

The motor control module keeps the motor rotating at a constant 1800 r/min. The module compares the tachometer pulses coming from the motor to a constant reference. This comparison determines the motor's current requirements provided by the motor control module. For further information on the motor control modules see Paragraph 6.3.3.

6.3.1.3 Head Positioning Mechanism – A stepper motor control circuit on the seek and interface module controls a four-phase motor. The stepper motor positions the R/W heads over the data tracks on the diskette by rotating a grooved step cam lead screw. This positions a head carriage assembly over the 80 data tracks on the diskette. The stepper motor rotates in 15 degree increments, moving the head carriage assembly one data track for each increment.

The grooved step cam lead screw has a flat spot between each track ramp. A ruby ball, attached to the head carriage assembly, runs in the groove. The flat spots on the lead screw prevent the transfer of small angular vibrations from the screw to the ruby ball.

The head carriage assembly moves smoothly along two rods. Its position over the data tracks is determined by the location of the ruby ball in the lead screw. Two heads, located back to back on the head carriage assembly, can be positioned over any one of 80 data tracks on either diskette.

The head carriage assembly also contains a track zero interrupter bar. This bar is sensed when the head carriage assembly is near track zero and a signal is sent to the seek and interface module. For further information see Paragraph 6.3.1.5.

6.3.1.4 Head Load Mechanism – A head load mechanism is a solenoid actuated arm with a head load pad. When energized, the solenoid releases a head load pad arm to press against the diskette opposite the R/W head. The pad conforms the medium to the contour of the R/W head. This ensures good head-to-medium contact during read or write operations.

When the head load solenoid is deenergized, the head load pad arm is raised away from the diskette. This reduces wear on the diskette and the R/W head.

The head automatically unloads if any of the following conditions occur:

- Either of the doors is open.
- The spindle motor is off.
- The drive side is not selected.
- No diskette is present in the drive side.

The front bezel of the drive contains two head load LEDs. Each LED lights when its corresponding head is loaded. The LEDs warn the operator not to remove the diskette while the controller is accessing it.

For further information on the control of the head solenoids and LEDs, see Paragraph 6.3.4.

6.3.1.5 Sensors – The drive contains switch sensors and photosensitive sensors for passing status information to the seek and interface module. Figure 6-10 shows that there are two sets of sensors for each drive side and one track zero sensor. Each set of sensors provides disk presence, write protection, and index hole location information.

Track Zero Sensor
The track zero sensor consists of an LED and a phototransistor combination. As the carriage assembly nears track zero, a tab passes between the diode and the phototransistor. This turns off the phototransistor and asserts the track zero signal TKOS H to the seek and interface module. For further information see Paragraph 6.3.7.

Diskette Present and Write-Protect Sensors
Each drive side has a write-protect switch sensor and a diskette present switch sensor. A switch pair for each side is selected simultaneously. Signal SEL A L selects the switches for drive side A. Signal SEL B L selects the switches for drive side B.

When the door is closed, the switches come in direct contact with an inserted diskette. The switches are normally closed. However, inserting a write-protected diskette in the drive opens both switches. When the switches are open and selected, the DP and WP signals assert. These signals provide the seek and interface module with status signals. For further information see Paragraph 6.3.6.

Index Sensor Detail Description
Each index sensor consists of an LED and a phototransistor combination. As the index hole in the diskette passes by a sensor, the light from the diode passes through the hole, striking the phototransistor. This causes the phototransistor to turn on and assert the appropriate index signal, INDEX A L or INDEX B L, to the seek and interface module. For further information see Paragraph 6.3.6.

6.3.2 Select Circuit Detailed Operation
Figure 6-11 shows the operational detail of the select circuits. These circuits perform the following functions for the RX50 drive:

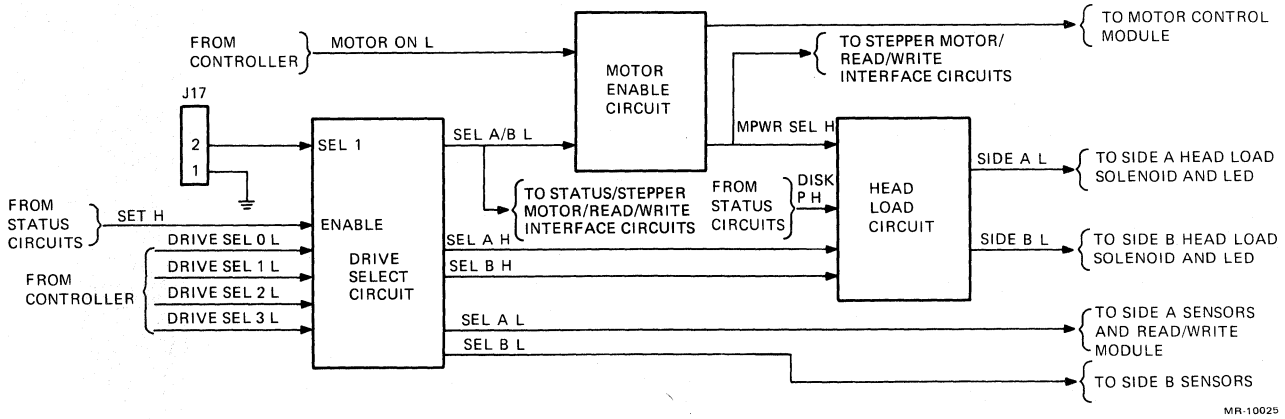


Figure 6-11 Select Circuit Functional Detail

- Pass an enable signal to the motor control module.
- Generate a circuit enable signal.
- Activate head load solenoids and associated LEDs.
- Generate sensor select and R/W head select signals.

The select circuit contains the following elements to perform these functions which are described in the following sections:

- Drive select circuit
- Motor enable circuit
- Head load circuit

6.3.2.1 Drive Select Circuit Detail – The drive decodes the four drive select lines, DRIVE SEL 0 L through DRIVE SEL 3 L, depending on the condition of J17 (configuration jumper). With J17 open (without a jumper), the drive select circuit decodes DRIVE SEL 0 L and DRIVE SEL 1. With J17 closed (with a jumper), the drive select circuit decodes DRIVE SEL 2 L and DRIVE SEL 3.

The drive select circuit is enabled by a dc voltage status signal, SET H, from the status circuits. When the SET H signal is asserted, the drive select circuits decode the input signals and assert the output select signals.

Table 6-1 shows how the asserted DRIVE SEL inputs control the SEL outputs when a jumper is not installed at J17. Table 6-2 shows how the asserted DRIVE SEL inputs control the SEL outputs when a jumper is installed at J17.

Table 6-1 Select Signals, Jumper J17 Removed

DRIVE SEL INPUTS	A/B L	SEL OUTPUTS A L	B L	A H	B H
SEL 0 L	yes	yes	no	yes	no
SEL 1 L	yes	no	yes	no	yes
SEL 2 L	no	no	no	no	no
SEL 3 L	no	no	no	no	no

Table 6-2 Select Signals, Jumper J17 Installed

DRIVE SEL INPUTS	A/B L	SEL OUTPUTS A L	B L	A H	B H
SEL 0 L	no	no	no	no	no
SEL 1 L	no	no	no	no	no
SEL 2 L	yes	yes	no	yes	no
SEL 3 L	yes	no	yes	no	yes

6.3.2.2 Motor Enable Circuit Detail – The motor enable circuit performs the following functions:

- Asserts a spindle motor control circuit enable signal, MPWR H, when the controller asserts MOTOR ON L.
- Asserts a circuit enable signal, MPWR SEL H, when the drive is selected (SEL A/B L is asserted) and the spindle motor control circuit is enabled (MPWR H is asserted).

When the drive is selected and the motor is enabled, the head load circuits, stepper motor circuits, and the R/W interface circuits are enabled.

6.3.2.3 Head Load Circuit Detail – The head load circuits assert one of two select signals, SIDE A L or SIDE B L. Each of these signals activates a head load solenoid and a head load LED.

An asserted SEL A H or SEL B H asserts the corresponding side signal when the following conditions exist:

- A diskette is present in the selected side and the door is closed (DISK P H is asserted).
- The drive is selected and the spindle motor is turned on (MPWR SEL H is asserted).

6.3.3 Motor Control Circuit Detail

Figure 6-12 shows the operational detail of the spindle motor control circuits. These circuits receive dc power and an enable signal, MPWR H, from the seek and interface module.

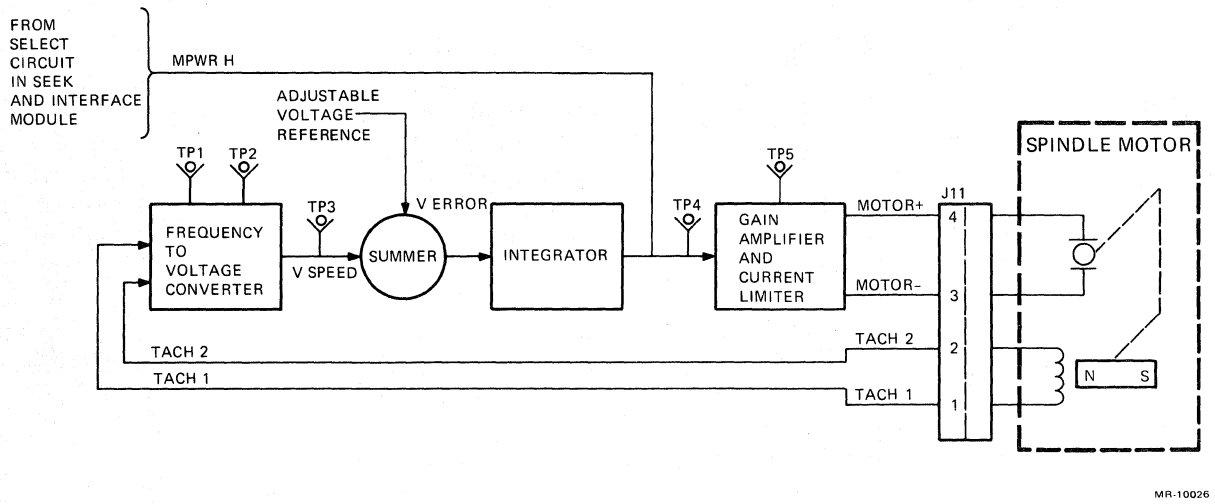


Figure 6-12 Motor Control Circuit Functional Detail

When enabled, these circuits supply drive current to the spindle motor. They also monitor the motor speed and regulate the motor current. This maintains the spindle motor's constant angular speed.

To perform these functions, this circuit consists of the following elements. These elements are described in the following sections.

- Frequency to voltage converter
- Summer
- Integrator
- Gain amplifier and current limiter

6.3.3.1 Frequency to Voltage Converter Detail – The spindle motor contains a tachometer. When the motor is operating, the tachometer returns sinusoidal signals, TACK 1 and TACK 2, to the frequency to voltage converter. These signals represent the motor's angular rotation.

The tachometer signal is converted to a voltage. This voltage, V SPEED, represents the motor's speed as follows:

1. Each zero voltage crossing of the tachometer signal converts to alternating pulses. These pulses are observable at test point TP1 (Figure 6-13).

2. The leading edge of each pulse generates a transition from 0 V to 5 V, or 5 V to 0 V. These transitions, which appear as a rectangular wave, are observable at TP2 (Figure 6-13).

3. The low transitions are averaged with the high transitions. This forms a sawtooth wave that rides at an average voltage level. This signal, the speed voltage, is observable at test point TP3 (Figure 6-13).

6.3.3.2 Summer Detail – The summer adds a constant reference voltage to the speed voltage (V SPEED) signal. This adjusts the average voltage level of the V SPEED signal to the linear range of the integrator and gain amplifier. The reference voltage, adjusted at the time of manufacture, is not field adjustable.

The output of the summer equals the speed error, V ERROR, for the integrator.

6.3.3.3 Integrator Detail – The integrator inverts the sawtooth wave of the V ERROR signal. This converts a decreasing average voltage to an increasing average voltage, and vice versa. This inversion is needed because the sensed speed error voltage drops as the speed decreases. However, the motor requires more power to increase its speed, and vice versa.

The output of the integrator is observable at test point TP4 (Figure 6-13). An asserted spindle motor control circuit enable signal, MPWR H, allows the integrator output to pass to the gain amplifier and current limiter. When MPWR H is unasserted, the gain amplifier and current limiter is disabled.

6.3.3.4 Gain Amplifier and Current Limiter – The gain amplifier couples power to the spindle motor. The current limiter limits the amount of power coupled to the motor. This protects the motor during circuit or hardware faults and when the circuit is first enabled.

The gain amplifier operates in its linear range, except when the spindle motor control circuit is first enabled. When initially enabled, the gain amplifier is forced into saturation. This occurs because the motor's sensed speed causes the integrator to generate the maximum driving signal.

As the motor approaches its required speed, the integrator generates a sawtooth wave (see Paragraph 6.3.3.3). This signal operates the gain amplifier in its linear range.

The high peaks of the sawtooth wave turn the gain amplifier on and off, forming current pulses for the motor. These pulses are observable at test point TP5 as voltage pulses (Figure 6-13).

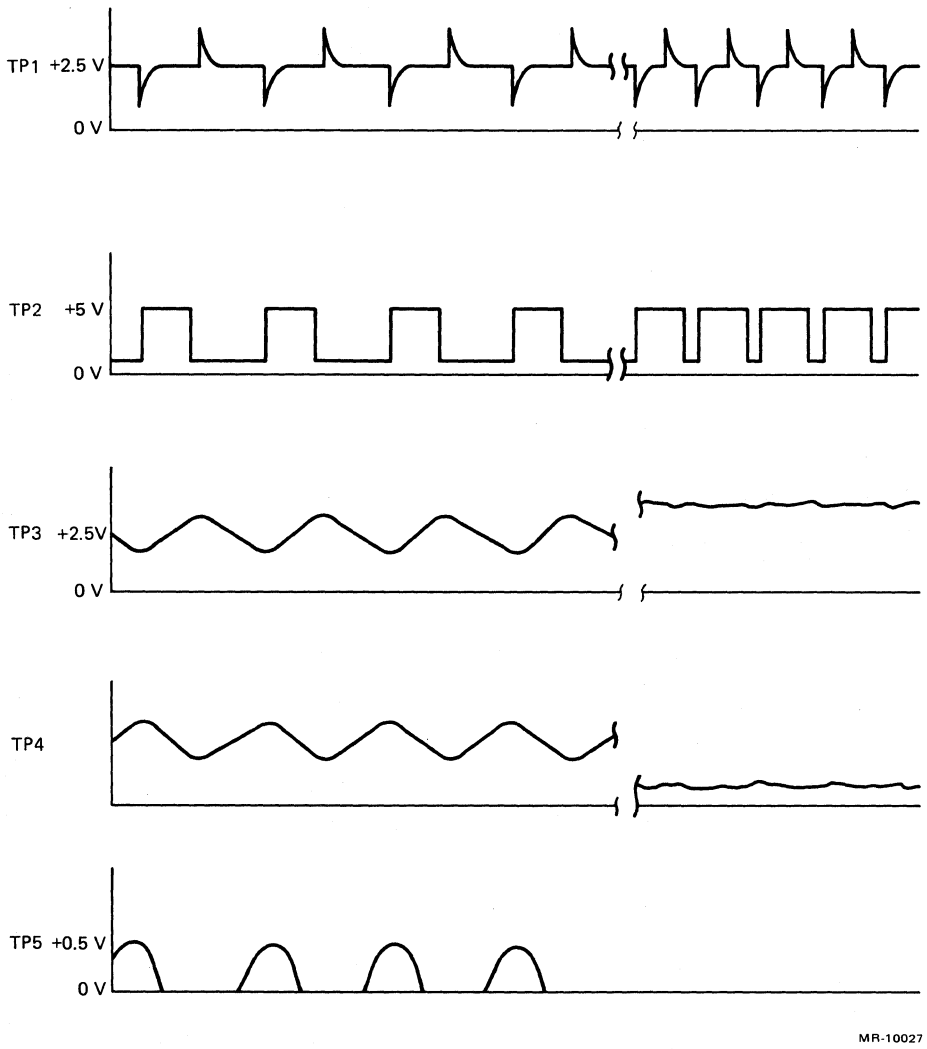


Figure 6-13 Motor Control Wave Forms

6.3.4 Head Load Solenoids and LEDs

Figure 6-14 shows the electrical connections to the head load solenoids and LEDs that are controlled by the select circuits. The drive contains two solenoids and two LEDs, one set for each drive side. The select logic activates one set at a time when the following conditions exist:

- The spindle motor is operating.
- A diskette is properly inserted and the door is closed.
- The drive side is selected.

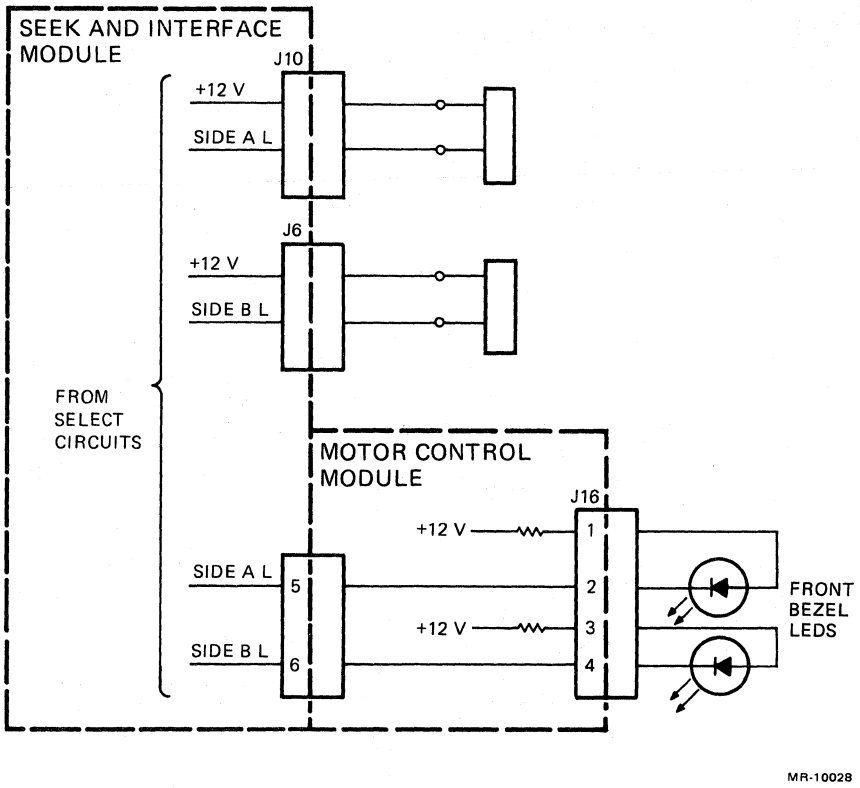


Figure 6-14 Electrical Connections to Head Load Solenoids and LEDs

6.3.5 Status Circuit Detail

Figure 6-15 shows the detail operation of the status circuits. Figure 6-16 shows the timing relationships between the circuit signals. These circuits perform the following functions for the RX50 drive:

- Pass status signals from the drive to the controller
- Monitor the dc power for fluctuations

These functions are performed by the following status circuit elements:

- Write-protect status circuit
- Diskette present status circuit
- Output drivers
- +5 V monitor

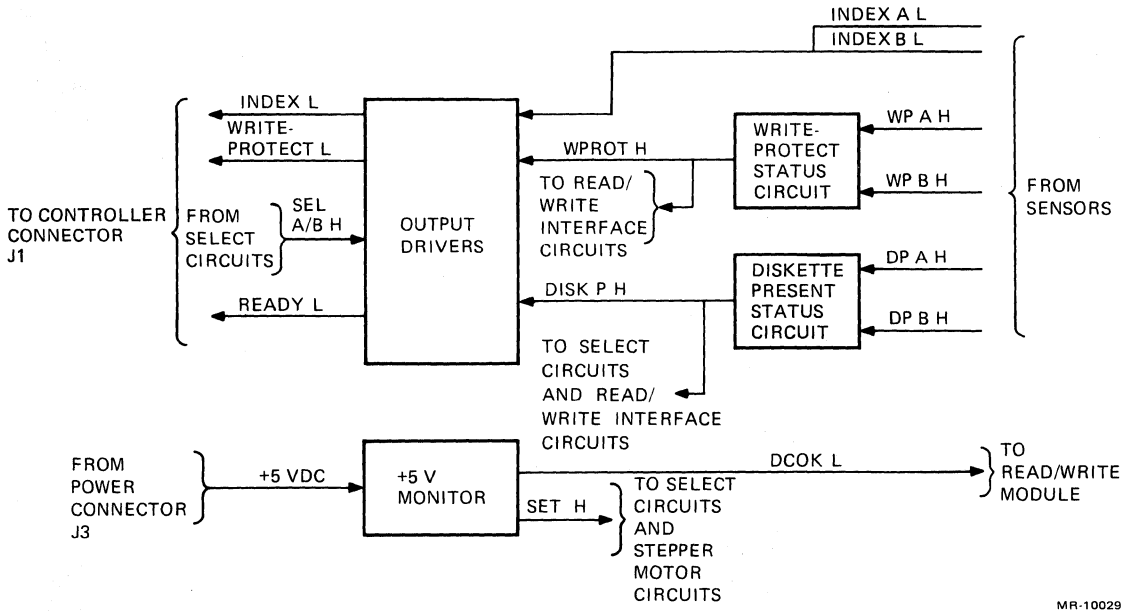


Figure 6-15 Status Circuit Detail

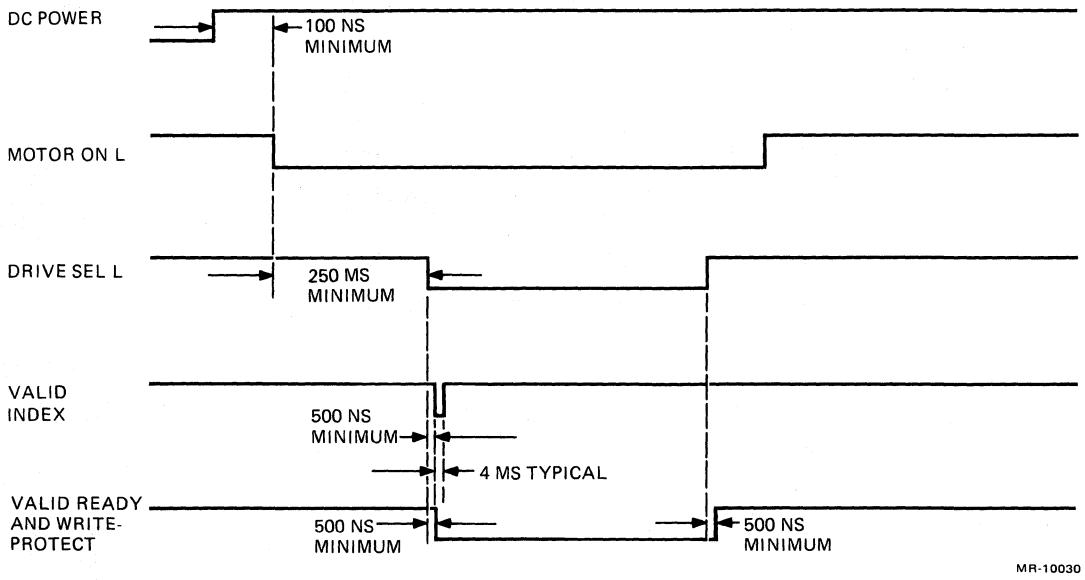


Figure 6-16 Status Circuit Timing Relationships

6.3.5.1 Write-Protect Status Circuit Detail – This circuit monitors the write-protect status signals, WP A H and WP B H, from the write-protect sensors (see Paragraph 6.3.6.2). If either signal asserts, this circuit asserts the write-protect signal, WPROT H, for the output drivers and the R/W interface circuits.

6.3.5.2 Diskette Present Status Circuit Detail – This circuit monitors the diskette present status signals, DP A H and DP B H, from the diskette present sensors (see Paragraph 6.3.6.2). If either signal asserts, this circuit asserts the diskette present signal, DISK P H, for the output drivers, select circuits, and the R/W interface circuits.

6.3.5.3 Output Driver Detail – These drivers pass the status signals from the RX50 drive to the controller. They are enabled when the SEL A/B H signal from the select circuits is asserted. The output drivers pass the signal state of the index (see Paragraph 6.3.6.1), write-protect, and diskette present signal as INDEX L, WRITE PROTECT L, and READY.

6.3.5.4 +5 Volt Monitor – This monitor generates enable and reset signals for the RX50 drive. It continually monitors the state of the +5 V power of the drive. If the power goes beyond the tolerance range, the monitor deasserts DCOK L and SET H.

The DCOK L signal enables the write circuits to operate when they are selected. The SET H signal enables the select and stepper motor circuits.

6.3.6 Status Sensor Detail

Figure 6-17 shows the detail operation of the status sensors. These sensors are a series of LEDs with photosensitive transistors and switches. These sensors perform the following functions for the RX50 drive:

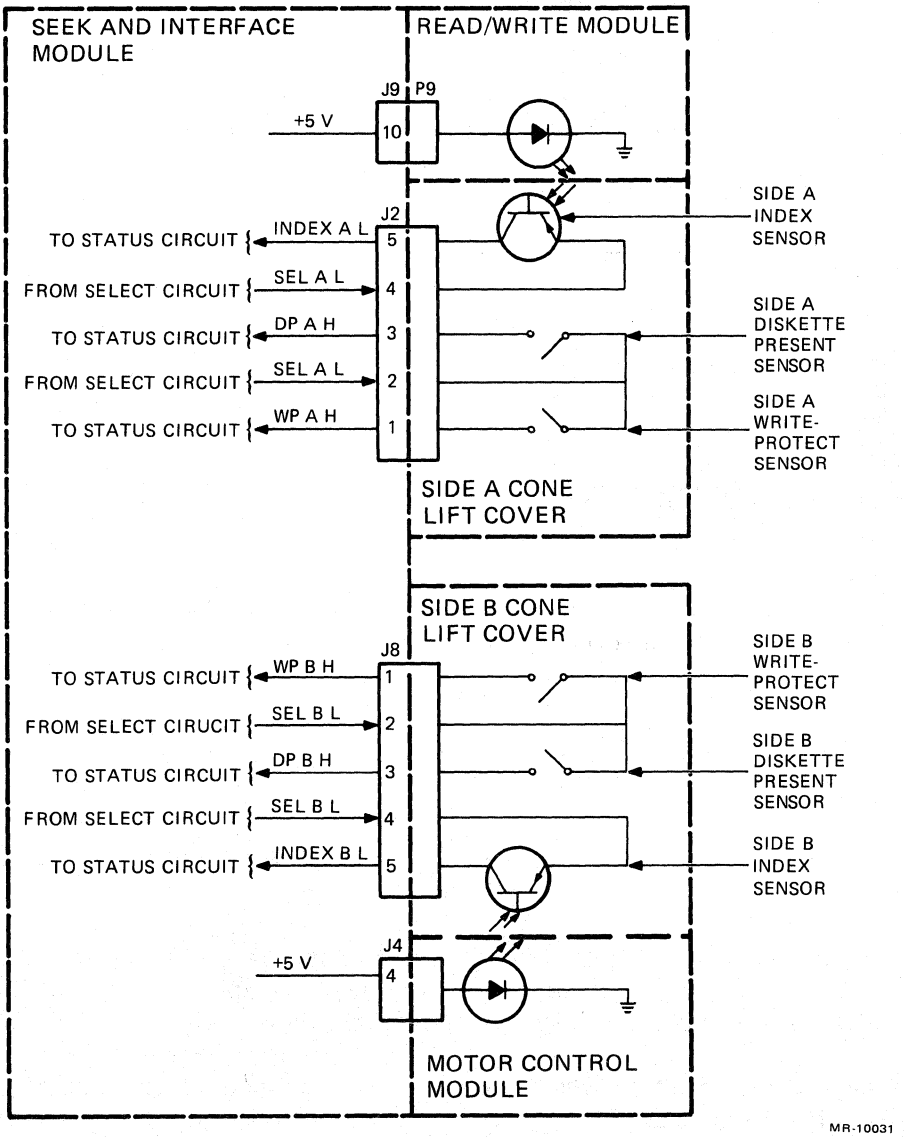


Figure 6-17 Sensor Detail

- Sense the presence of the diskette for the status circuits.
- Sense the location of the index hole in the diskette for the status circuits.
- Sense the write-protect status of the diskette for the status circuits.

6.3.6.1 Index Sensor Detail – The drive contains two index sensors, one sensor for each drive side. Each index sensor consists of an LED and a photosensitive transistor. A select signal from the select circuits enables the photosensitive transistor. When the select signal is unasserted, the sensor is disabled.

When a sensor is enabled, it controls a status signal, INDEX A L or INDEX B L, for the status circuits. The signal is asserted when the index hole in the diskette passes by the selected sensor. The light from the LED then strikes the photosensitive transistor, turns it on, and asserts the index signal.

6.3.6.2 Diskette Present and Write-Protect Sensor Detail – The drive contains two sets of diskette present and write-protect sensors, one set for each drive side. Each sensor provides a status signal to the status circuits. The sensors are switches selected by the select circuits.

Each drive side has a write-protect switch and a diskette present switch. The switches for each side are selected as pairs. Signal SEL A L selects the switches for drive side A. Signal SEL B L selects the switches for drive side B.

When the door is closed, the switches come in direct contact with a diskette inserted in the drive side. The switches are normally closed. Inserting a write protected diskette in the drive opens both switches. When the switches are open and selected, the diskette present and write-protect signals are asserted.

6.3.7 Stepper Motor Circuit Detail

Figure 6-18 shows the detailed operation of the stepper motor circuits. Figure 6-19 shows the timing relationships between the circuits signals. These circuits perform the following functions:

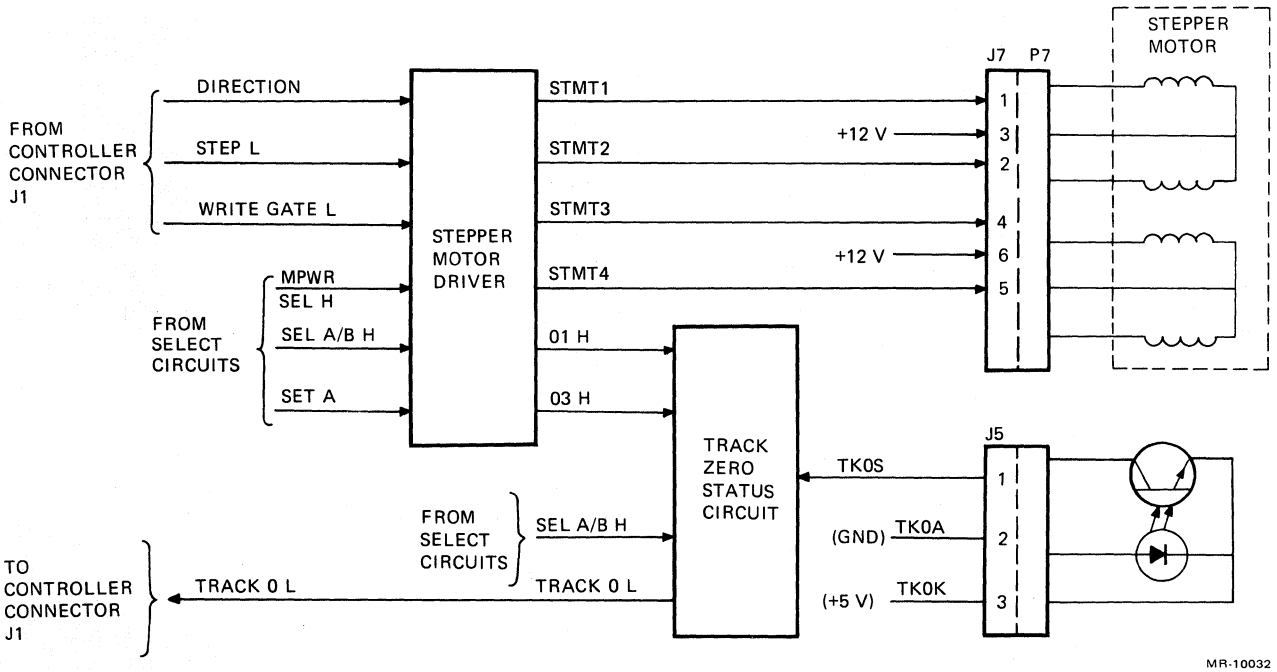


Figure 6-18 Stepper Motor Circuit Detail

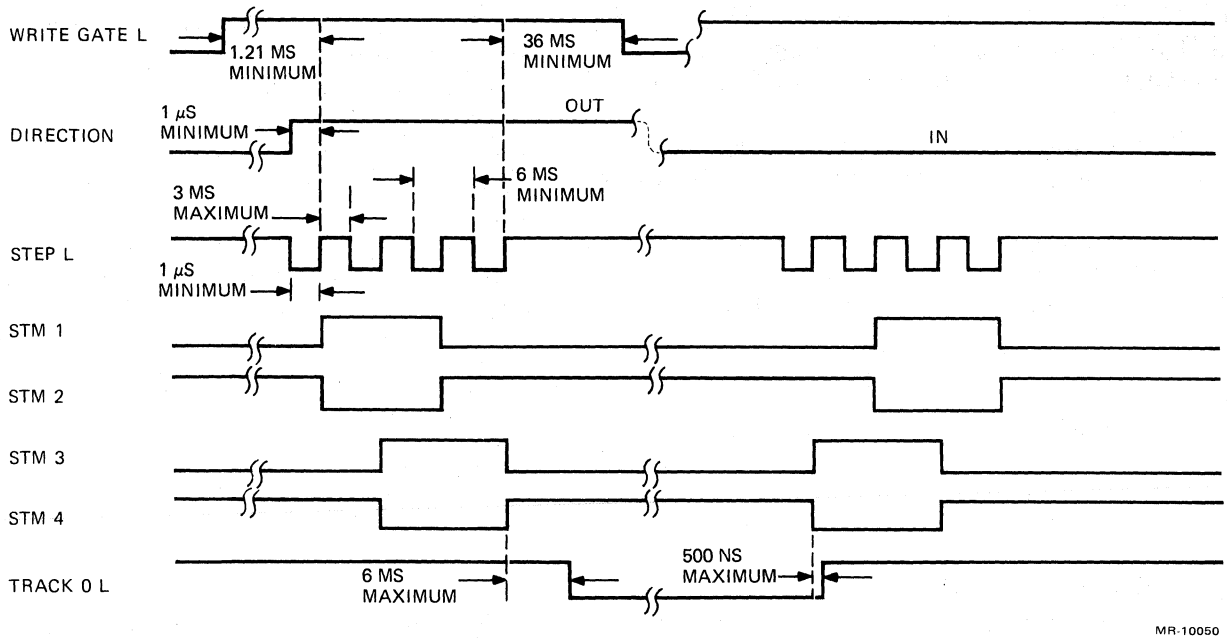


Figure 6-19 Stepper Motor Timing Relationships

- Generate control signals that actuate the stepper motor
- Pass a track zero status signal to the controller

These functions are performed by the following stepper motor circuit elements:

- Stepper motor driver
- Track zero sensor
- Track zero status circuit

6.3.7.1 Stepper Motor Driver Detail – The stepper motor driver decodes control signals from the controller and generates phase control signals for the stepper motor coils. This driver also passes phase control signals to the track zero status circuit. These signals indicate a possible track zero head position.

The select and status circuits and the controller enable the stepper motor driver. The driver requires an asserted MPWR SEL H, SEL A/B H, and SET H while WRITE GATE L is unasserted. These signal states indicate that the following conditions exist for the stepper motor driver operation:

- The spindle motor is operating.
- The drive is selected.
- The +5 V power level is in tolerance.
- The drive is not enabled for write operations.

The stepper motor controller generates four phase-control signals for the operation of the stepper motor, STMT1, STMT2, STMT3, STMT4. These driver outputs are decoded from two controller signals, DIRECTION and STEP L. Figure 6-19 shows the timing relationships between the controller inputs and the driver outputs.

The DIRECTION signal indicates the direction the stepper motor rotates. The STEP L signal indicates the number of steps the motor moves.

6.3.7.2 Track Zero Sensor Detail – The drive contains one track zero sensor. This sensor consists of an LED and a photosensitive transistor and is always enabled. When the heads are located at track 0, 1, or 2, this sensor asserts a track zero sense signal, TK0S, for the stepper motor circuits.

The TK0S signal is asserted when a tab on the carriage assembly passes by the sensor. The tab stops light from the LED from striking the photosensitive transistor. This turns off the transistor and asserts TK0S.

6.3.7.3 Track Zero Status Circuit Detail – The track zero status circuit monitors for a track zero R/W head location. When the drive is selected, this circuit is enabled by the select circuits. When enabled, this circuit returns a track zero status signal, TRACK 0 L, to the controller.

The track zero status circuit asserts the TRACK 0 L signal when the following conditions exist:

- When the heads are located over track 0, 1, or 2, (TK0S H asserted).
- When the stepper motor driver asserts the zero phase signals to the motor, (01 H and 03 H signals asserted).

6.3.8 Read/Write Interface Circuit Detail

Figure 6-20 shows the R/W interface circuit operational detail. Figures 6-21 and 6-22 show the timing relationships between the circuit signals and valid data. These circuits perform the following functions for the RX50 drive:

- Pass write data from the controller to the R/W module
- Pass write control signals from the controller to the R/W module
- Generate an erase control signal for the R/W module
- Pass read data from the R/W module to the controller

These functions are performed by the following R/W interface circuit elements:

- Write driver circuit
- Erase gate timer
- Output driver

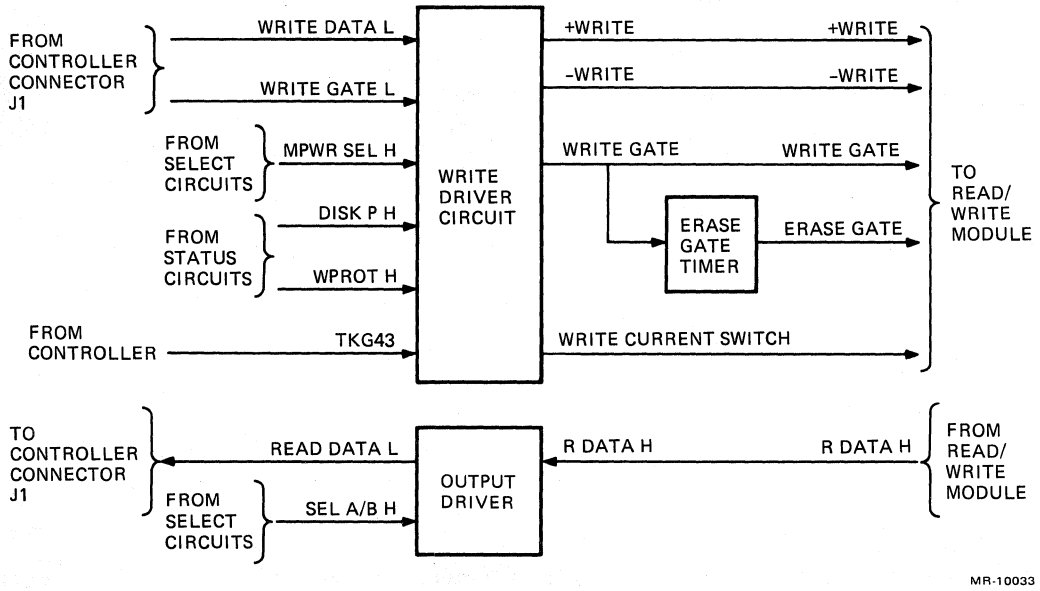


Figure 6-20 Read/Write Interface Circuit Detail

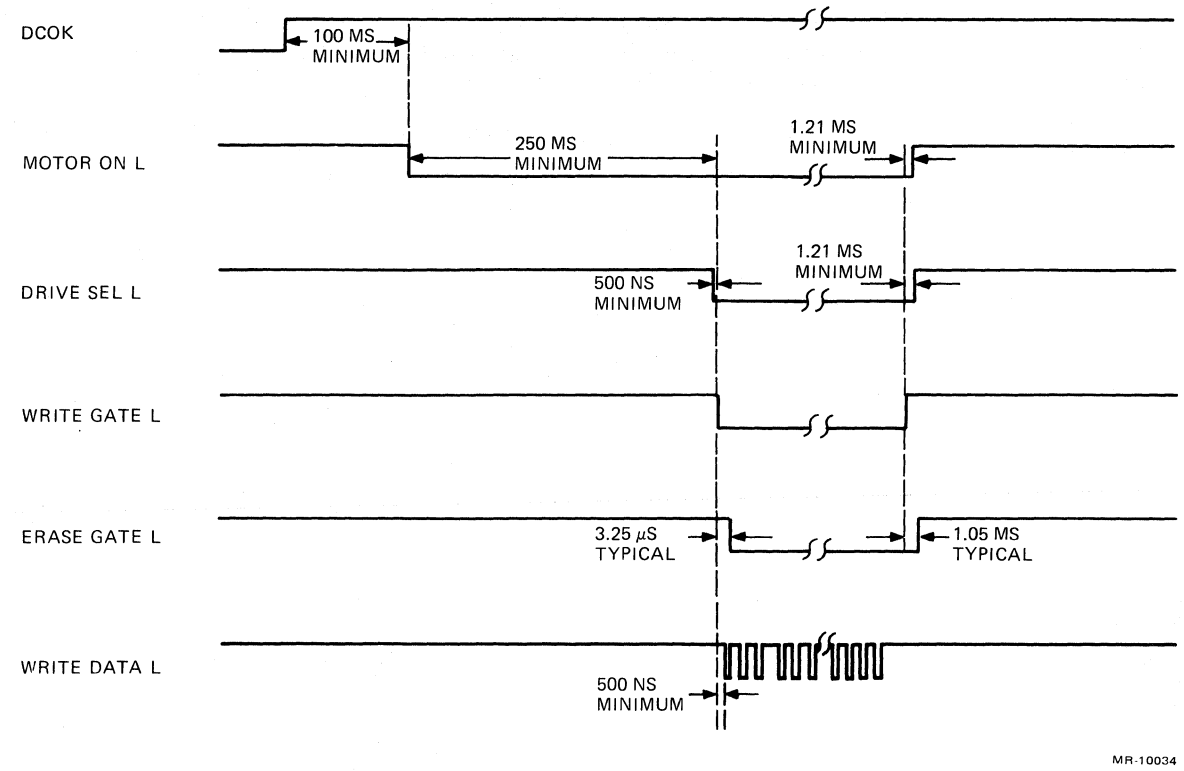


Figure 6-21 Write Data Timing Relationships

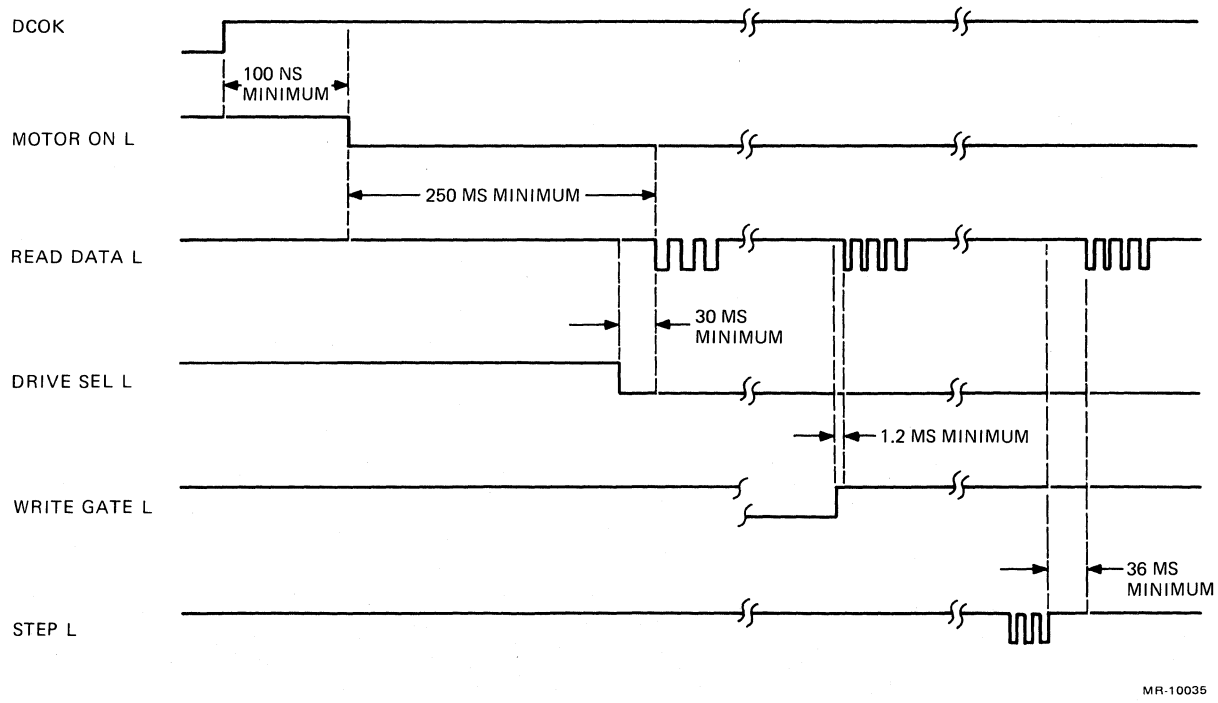


Figure 6-22 Read Data Timing Relationships

6.3.8.1 Write Driver Circuit – When enabled, the write driver circuit passes write data and commands to the erase gate and R/W module. This circuit is enabled by the controller, select circuits, and status circuits (Figure 6-20). The write driver circuit is enabled when the following conditions exist:

- The controller selects a write function by asserting WRITE GATE L.
- The spindle motor is enabled and the drive is selected. This is indicated by an asserted MPWR SEL H signal.
- A diskette is present in the selected side and the door is closed. This is indicated by an asserted DISK P H signal.
- The diskette is not write protected. This is indicated by an unasserted WPROT H signal.

When enabled, the write driver circuit divides write data from the controller by two. It then passes the data on differential lines to the R/W module. This converts the write data pulses to leading edge triggered differential data. For further information on the write data see Paragraph 6.3.9.4.

The driver also passes two control signals from the controller to the R/W module: the WRITE GATE L signal as WRITE GATE, and the TKG43 signal as WRITE CURRENT SWITCH. The WRITE GATE signal enables the write circuits in the R/W module. The WRITE CURRENT SWITCH signal controls the level of write current the write circuits generate.

6.3.8.2 Erase Gate Timer Detail – The erase gate timer delays the WRITE GATE signal to generate an ERASE GATE signal. This delay is necessary because of the R/W head design (See Paragraph 6.3.11). Figure 6-21 shows the timing relationships of the ERASE GATE and WRITE GATE.

6.3.8.3 Output Driver Detail – The output driver passes read data, R DATA H, from the R/W module to the controller. Figure 6-22 shows the timing relationships between the circuit signals and the read data.

The output driver is enabled by the select logic when SEL A/B H is asserted. This signal state indicates that the RX50 drive is selected.

6.3.9 Write Circuit Detailed Operation

Figure 6-23 shows the write circuit operational detail. These circuits perform the following functions for the RX50 drive:

- Generate write currents for the heads
- Generate an erase current for the heads
- Generate head select signals
- Protect the heads and previously written data when the dc power is out of tolerance

These functions are performed by the following write circuit elements:

- Write current generator
- Voltage reference
- +12 V gate
- Differential write switch
- Erase current generator
- Multiplexer

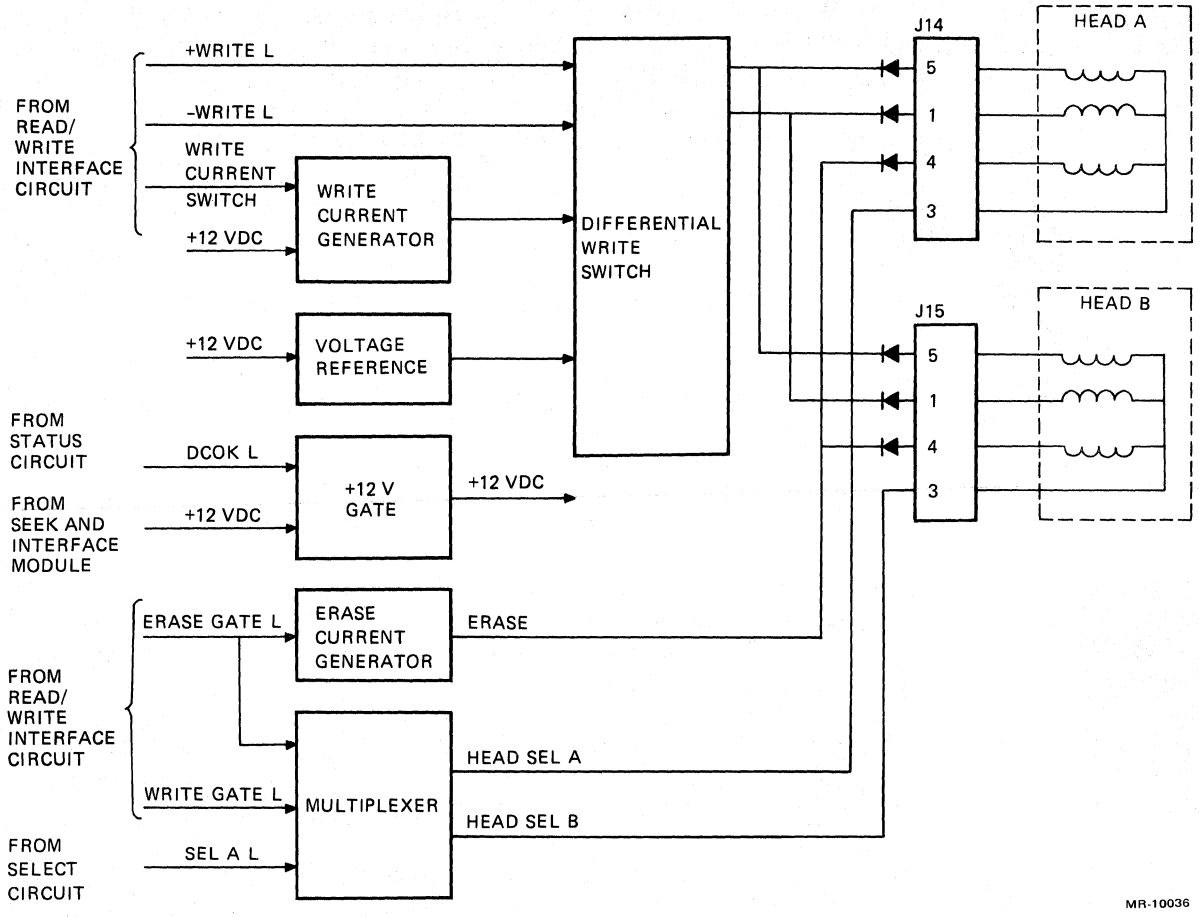


Figure 6-23 Write Circuit Detail

6.3.9.1 Write Current Generator Detail – The write current generator provides a selectable current for the differential write switch. These currents are derived from the +12 V from the +12 V gate.

When the WRITE CURRENT SWITCH signal is asserted, a low current for the inner tracks (44 through 79) is provided to the differential write switch. When the WRITE CURRENT SWITCH signal is unasserted, a high current for the outer tracks (0 through 43) is provided to the differential write switch.

6.3.9.2 Voltage Reference Detail – The voltage reference provides a stable voltage to the differential write switch. This reference voltage makes sure that the outputs of the differential write switch are balanced.

6.3.9.3 +12 V Gate Detail – The +12 V gate receives the R/W modules supply voltage (+12 Vdc) and a DCOK signal. If DCOK remains asserted, the gate passes +12 Vdc to the module's circuits. This makes sure that the write circuits are disabled if a low power condition exists.

6.3.9.4 Differential Write Switch Detail – The differential write switch converts the write data from the R/W interface circuits to write currents for the R/W heads. Figure 6-24 shows the conversion of WRITE DATA from the controller (Paragraph 6.3.8.1) to write currents for the heads. For this conversion, the differential write switch requires a write current and a reference voltage.

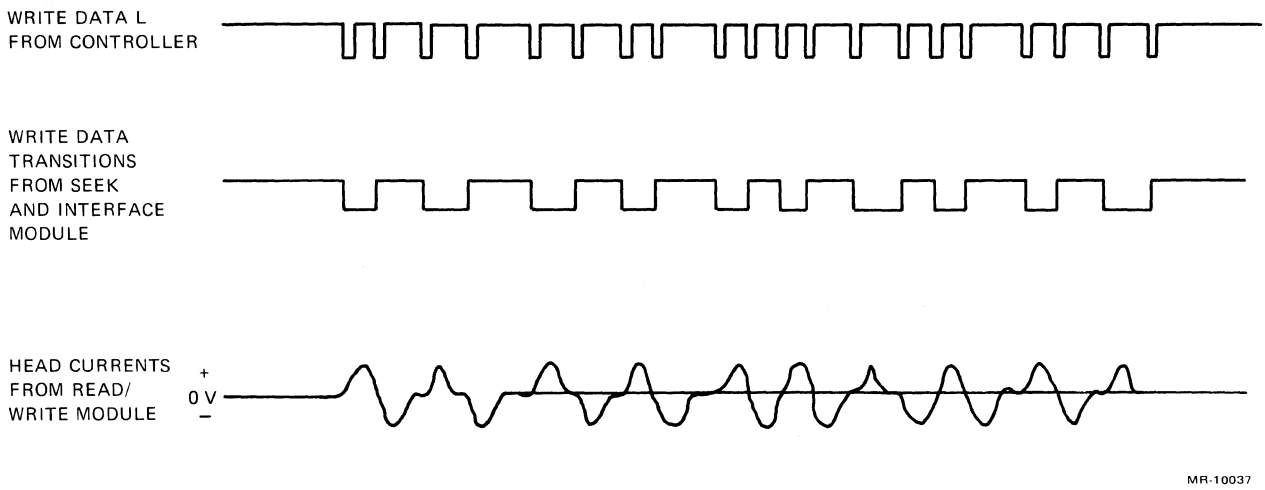


Figure 6-24 Write Data to Head Current Conversion

The write currents, +WRITE and –WRITE, generate magnetic fields in the heads that record data on the diskette. For further information on the recording techniques see Paragraph 6.3.11.

6.3.9.5 Erase Gate Generator Detail – The erase gate generator converts the ERASE GATE L signal to an ERASE current for the R/W heads. This current generates a magnetic field in the heads which tunnel erases recorded data on the diskette. For information on recording techniques see Paragraph 6.3.11.

6.3.9.6 Multiplexer Detail – The multiplexer decodes three signals (ERASE GATE, WRITE GATE, and SELECT) to generate head select signals for a write function. Table 6-3 shows how the inputs assert the outputs, HEAD SEL A and HEAD SEL B signals.

Table 6-3 Write Function Head Select

INPUTS			OUTPUTS	
ERASE GATE L	**WRITE GATE L**	**SEL A L**	**HEAD SEL A**	**HEAD SEL B**
no	no	no	write not selected	
no	yes	no	yes	no
yes	no	no	yes	no
yes	yes	no	yes	no
no	no	yes	write not selected	
no	yes	yes	no	yes
yes	no	yes	no	yes
yes	yes	yes	no	yes

6.3.10 Read Circuit Detailed Operation

Figure 6-25 shows the detailed operation of the read circuits. These circuits perform the following functions for the RX50 drive:

- Select a R/W head and read data
- Convert the analog read data to digital data

These functions are performed by the following read circuit elements:

- Read amplifier
- Multiplexer

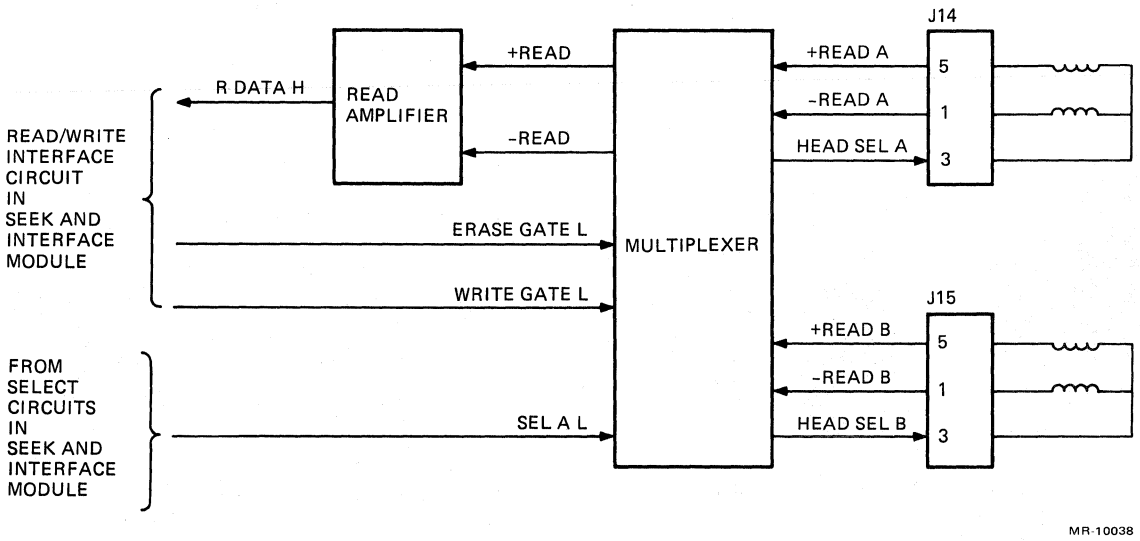


Figure 6-25 Read Circuit Detail

6.3.10.1 Read Amplifier Detail – The read amplifier converts analog read signals, developed in the R/W heads by the diskette, to digital read data for the R/W interface circuits. Magnetic flux reversals on the medium generate the analog signals. These flux reversals represent previously recorded data and clocks. Figure 6-26 shows the possible frequency combinations and the conversion results.

6.3.10.2 Multiplexer Detail – The multiplexer decodes three signals (ERASE GATE, WRITE GATE, and SELECT) to generate head select signals and select read data for the read amplifier. The write circuits use the same multiplexer; however, the ERASE GATE L and WRITE GATE L signals are unasserted for a read function.

Table 6-4 shows how the seek and interface module inputs select read data and head select signals.

6.3.11 Write/Read Head Detailed Operation

The RD50 drive has two R/W heads, one for each drive side. The heads are selected by either the write circuits or read circuits. Figure 6-23 shows the head connections for a write function and Figure 6-25 shows the head connections for a read function.

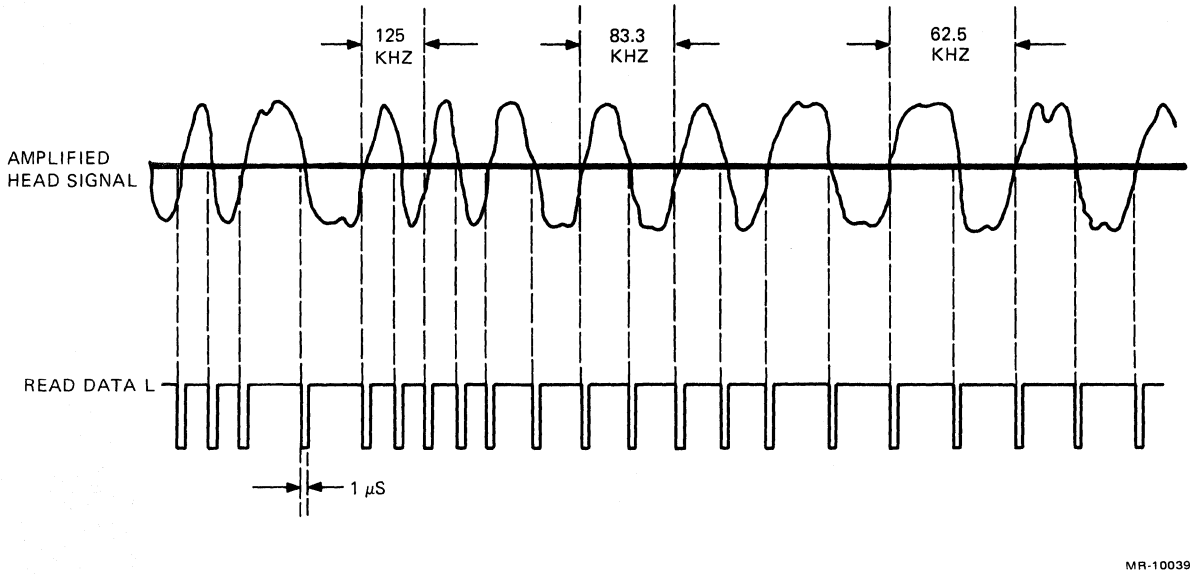


Figure 6-26 Head Signal to Read Data Conversion

Table 6-4 Read Function Head Select

ERASE GATE L	WRITE GATE L	SEL A L	HEAD SEL A	HEAD SEL B	HEAD DATA
no	no	yes	yes	no	A
no	yes	yes	read not selected		
yes	no	yes	read not selected		
yes	yes	yes	read not selected		
no	no	no	no	yes	B
no	yes	no	read not selected		
yes	no	no	read not selected		
yes	yes	no	read not selected		

Each head consists of a R/W ferrite core wound with a differential coil. The head also contains a forked erase ferrite core wound with a coil. The erase core is located behind the write core, with the forked core straddling the write core. This accounts for the delayed erase gate signal. For more information, refer back to Paragraph 6.3.8.2.

During write operations, current flows through the coils and generates a magnetic flux in the core. When the diskette passes under the R/W core, the surface of the medium is magnetized in one direction. Reversing the current magnetizes the surface in the opposite direction.

The forked erase core trims the edges of the magnetized surface. This ensures off-track reading capability for diskette interchangeability between drives.

During read operations, only the R/W core is used. The erase core is not used. When the diskette passes under the R/W core, the recorded flux reversals generate small alternating currents in the R/W coils. This current passes to the read circuits for conversion to digital data.

6.4 INTERMODULE SIGNAL DEFINITIONS

This section defines all control and data signals that pass between the controller and the RX50 drive and between the modules of the RX50 drive. All signal definitions in this section are grouped by common connector for easy recognition.

6.4.1 Seek and Interface/Controller Module Connector J1

This section describes the signals passed between the seek and interface module and the RX50 controller module. Figure 6-27 shows the control and data interface signal direction between the controller and the drive. The seek and interface module is part of the RX50 drive. Chapter 5 discusses the controller module in detail.

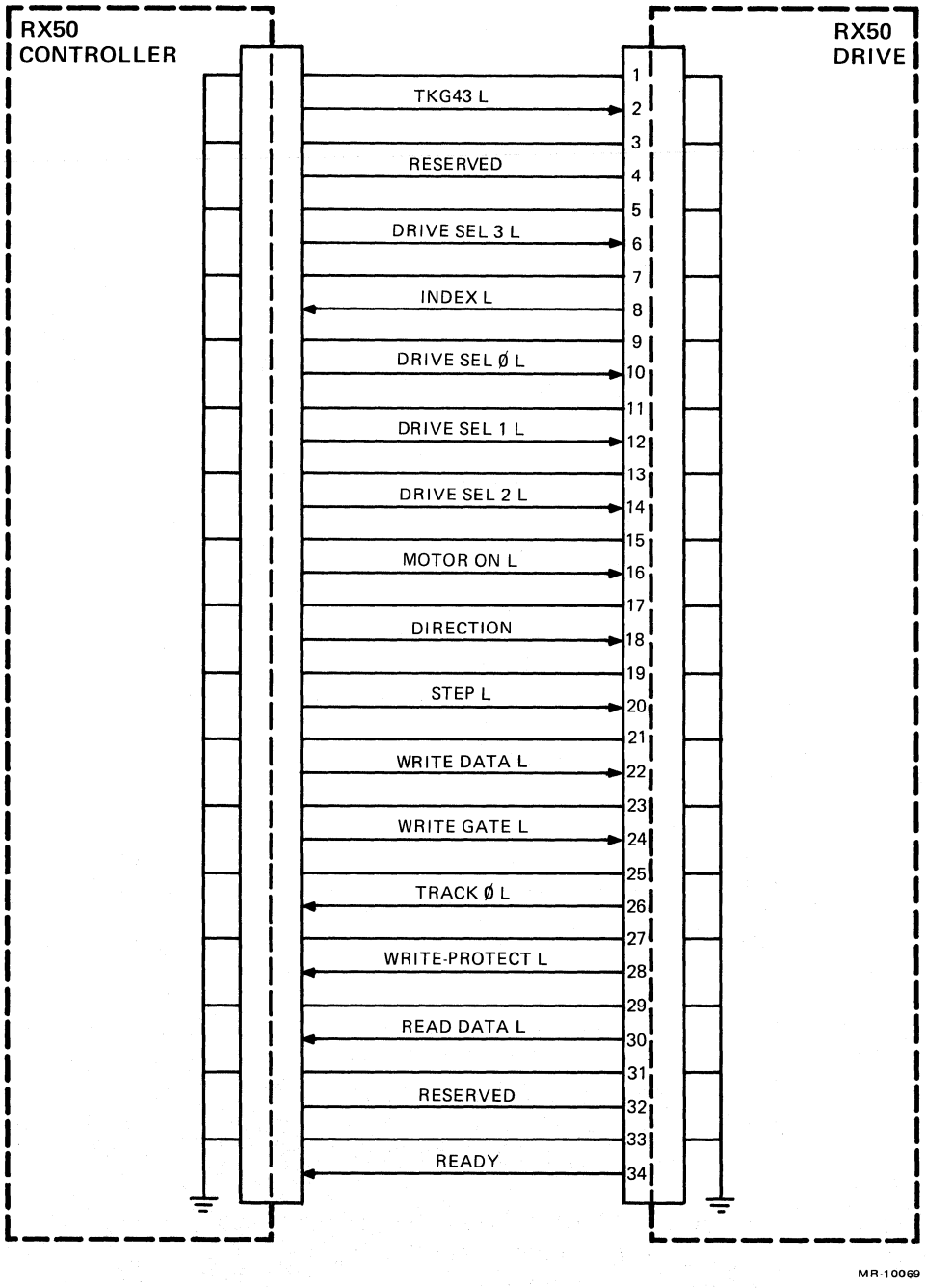


Figure 6-27 RX50 Controller and Drive Interface Signal Flow

Figure 6-28 shows the location of J1 and other connectors of the module. Odd numbered pins are grounded and are not discussed. An L attached to a signal name designates it asserted low (logic 0).

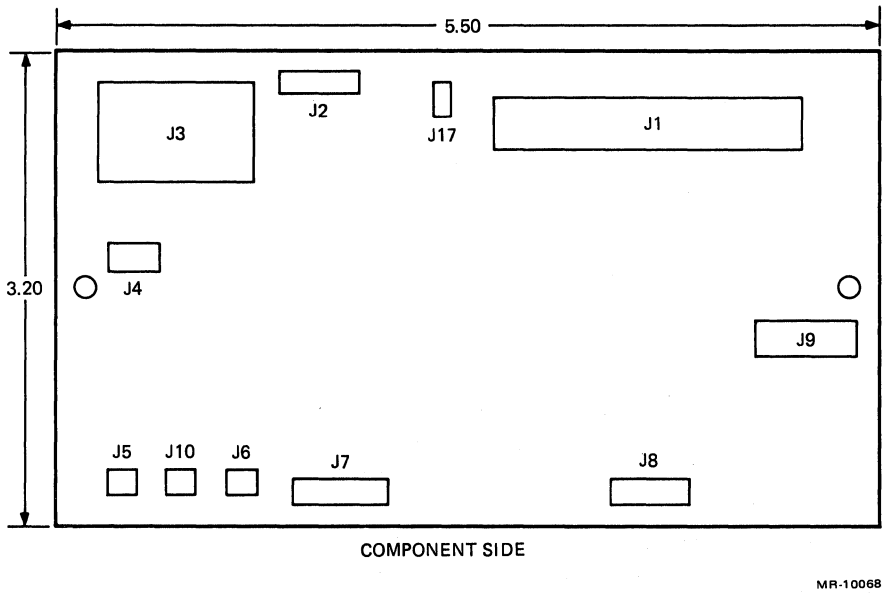


Figure 6-28 Seek and Interface Module Connector Locations

Pin	Mnemonic	Function
2	TKG43 L	Controls write current level
4	Reserved	Not used
6	DRIVE SEL3 L	Selects drive side B if J17 installed
8	INDEX L	Indicates index mark of selected side
10	DRIVE SEL0 L	Selects drive side A if J17 not installed
12	DRIVE SEL1 L	Selects drive side B if J17 not installed
14	DRIVE SEL2 L	Selects drive side A if J17 installed
16	MOTOR ON L	Turns spindle motor on or off
18	DIRECTION	Controls head movement direction
20	STEP L	Controls head movement distance
22	WRITE DATA L	Data to be stored on diskette
24	WRITE GATE L	Activates write circuits
26	TRACK 0 L	Track 0 head location LED
28	WRITE PROTECT L	Indicates selected diskette is write protected
30	READ DATA L	Data retrieved from diskette
32	Reserved	Not used
34	READY L	Indicates selected drive side contains a diskette

6.4.1.1 TKG43 L Input Signal – The RX50 controller generates this signal. It is asserted when writing data to tracks 44 through 79. In the asserted state, the seek and interface module reduces the write current. In the unasserted state, the seek and interface module generates a normal write current.

6.4.1.2 DRIVE SEL 0 through DRIVE SEL 3 Input Signals – These signals select the drive side (A or B) on which a function occurs. When J17 is not installed, signal DRIVE SEL 0 selects drive side A and signal DRIVE SEL 1 selects drive side B. When J17 is installed, signal DRIVE SEL 2 selects drive side A, and signal DRIVE SEL 3 selects drive side B.

6.4.1.3 TRACK 0 L Output Signal – This signal indicates the heads are located over track 0 (the outermost track). This signal is valid only when a drive side is selected.

6.4.1.4 MOTOR ON L Input Signal – This signal controls the motor control module, which controls the spindle motor. When this signal is asserted, the spindle motor rotates. The spindle motor reaches the rated rotational speed within one half second after an asserted MOTOR ON signal.

6.4.1.5 DIRECTION Input Signal – This signal defines the moving head direction when STEP input line is pulsed. Step-out (moving away from the center of the disk) is defined as high level of this signal (logic 1). Step-in (moving towards the center of the disk) is defined as low level of this signal (logic 0).

6.4.1.6 STEP L Input Signal – When pulsed, this signal moves the heads. Each pulse moves one track space in the direction indicated by the DIRECTION signal. The minimum pulse width is 1 μs. The minimum width between step pulses is 6 ms. This signal is ignored when WRITE GATE L is asserted, MOTOR ON L is unasserted, or no drive side is selected.

6.4.1.7 WRITE DATA L Input Signal – This signal represents data to be stored on the diskette. Each transition to the asserted state reverses the current to the R/W heads. Write pulses must begin a minimum of 500 ns after WRITE GATE is asserted. A minimum of 36 ms is required after the last STEP pulse occurs. Write pulses are ignored when WRITE GATE or MOTOR ON are unasserted, the diskette is write protected, no diskette is present, or no drive side is selected.

6.4.1.8 WRITE GATE L Input Signal – This signal enables writing and tunnel erasing of data to the diskette. This signal is ignored when the diskette is write protected.

6.4.1.9 INDEX L Output Signal – The leading edge of this pulse signal indicates the detection of the index hole in the selected drive side. The INDEX L pulse is valid 250 ms after MOTOR ON L is asserted. This signal is invalid if no drive side is selected.

6.4.1.10 WRITE-PROTECT L Output Signal – When asserted, this signal indicates that the write enable notch of the selected diskette is masked, and the writing of new data is inhibited. This signal is invalid if no drive side is selected.

6.4.1.11 READ DATA L Output Signal – This signal represents data retrieved from the diskette. READ DATA L is valid 250 ms after MOTOR ON L is asserted, 36 ms after receiving the last STEP L pulse, 1.21 ms after WRITE GATE signal is unasserted, or 30 ms after the drive side is selected.

6.4.1.12 READY Output Signal – This signal indicates that a diskette is present in the selected drive side. It is valid only if a drive side is selected.

6.4.2 Seek and Interface/Motor Control Modules Connector J4

This section describes the signals passed between the seek and interface module and the motor control module. Figure 6-28 shows the location of J4 and other connectors of the module. Power and ground signals are not discussed in detail. An L attached to a signal name designates it asserted low (logic 0). An H attached to a signal name designates it asserted high (logic 1).

Pin	Mnemonic	Function
1, 2	+12 V RET	Ground
3	MPWR H	Turns on spindle motor
4	+5 V DC	Side B index LED power source
5	SIDE A L	Drive A LED control
6	SIDE B L	Drive B LED control
7, 8	+12 V DC	Spindle motor and control logic power source

6.4.2.1 MPWR H Input Signal – This signal controls the spindle motor. When the signal is asserted, the spindle motor control logic is enabled and the spindle motor turns on.

6.4.2.2 SIDE A L Input Signal – This signal controls the drive A operational indicator on the front panel. When the signal is asserted, the indicator lights when the drive is in use.

6.4.2.3 SIDE B L Input Signal – This signal controls the drive B operational indicator on the front panel. When the signal is asserted, the indicator lights when the drive is in use.

6.4.3 Seek and Interface, Read/Write Modules Connector J9

This section describes the signals passed between the seek and interface module and the R/W module. Figure 6-28 shows the location of J9 and other connectors of the module. Power and ground signals are not discussed in detail. An L attached to a signal name designates it asserted low (logic 0). An H attached to a signal name designates it asserted high (logic 1).

Pin	Mnemonic	Function
1	DCOK L	Turns on +12 V power to module
2	+12 V RET	Ground
3	+WRITE L	Plus write data
4	R DATA H	Read data
5	W GATE L	Enables a write function
6	−WRITE L	Minus write data
7	SIDE 0	Not used
8	WRITE CURRENT SWITCH	Controls the level of the write current
9	ERASE GATE L	Controls tunnel erase function
10	+5 V DC	Side B index LED power source
11	SEL A L	Head select control signal
12	+12 V DC	+12 V power source

6.4.3.1 DCOK L Output Signal – This signal controls the +12 V power on the R/W module. When asserted, +12 V power is applied to the write and erase circuits on the module. When unasserted, +12 V power is removed from the circuits for protection of data on the diskette.

6.4.3.2 ±WRITE L Output Signals – This differential signal pair switches the direction of the write current in the R/W heads. The signals are alternately asserted, but not simultaneously asserted. During write protected or nonwrite operations, both signals are unasserted.

6.4.3.3 R DATA H Input Signal – This signal is the data output of the R/W module to the seek and interface module. The signal contains positive going pulses averaging 1 μs in duration. Positive going edges contain timing information to reconstruct nonreturn to zero (NRZ) data.

6.4.3.4 W GATE L Output Signal – This signal controls the write circuits on the R/W module. When asserted, this signal enables the write circuits. This signal is unasserted during both nonwrite and write protected operations. It is also unasserted if the spindle motor is off, the drive side is not selected, the diskette is missing, or the diskette is in backwards.

6.4.3.5 WRITE CURRENT SWITCH Output Signal – This signal switches the write current level above and below track 44. This action minimizes peak shift in the heads and media due to close tolerances of the flux changes. When asserted, this signal enables a high write current when the heads are positioned over tracks 0 through 43. When unasserted, this signal enables a low write current when the heads are over tracks 44 through 79.

6.4.3.6 ERASE GATE L Output Signal – This signal controls the current to the erase coils. When asserted, a current is produced in the selected erase coil. When writing is inhibited, this signal stays unasserted to disable the erase current.

6.4.3.7 SEL A L Output Signal – This signal selects one of the heads for read, write, and erase operations. When asserted, head A of drive side A is selected. When unasserted, head B of drive side B is selected.

6.4.4 Seek and Interface Power Connector J3

This section describes the connector that receives power for the entire drive. Figure 6-28 shows the location of J3 and other connectors of the module. Refer to Paragraph 6.2.4 for the power requirements.

Pin	Mnemonic	Function
1	+12 VDC	Plus 12 Vdc
2	+12 VDC RET	Ground
3	+5 VDC RET	Ground
4	+5 VDC	Plus 5 Vdc

6.4.5 Seek and Interface Connectors J2, J5, J6, J7, J8, J10, and J17

This section describes the functions of the remaining connectors of the seek and interface module. A brief description of signal functions is also given. Figure 6-28 shows the location of these connectors and other connectors of the module. An L attached to a signal name designates it asserted low (logic 0). An H attached to a signal name designates it asserted high (logic 1).

6.4.5.1 Side A Switches and Indicators Connector J2

Pin	Mnemonic	Function
1	WP A H	Write-protect LED
2	SEL A L	Write-protect/diskette present LED select
3	DP A H	Diskette present indicator
4	SEL A L	Index LED select
5	INDEX A L	Index LED

6.4.5.2 Track 0 Sensor Connector J5

Pin	Mnemonic	Function
1	TK0S H	Track zero indicator
2	TK0A	Transmitter diode +5 V source
3	TK0K	Transmitter/receiver diode sink

6.4.5.3 Side B Head Load Solenoid Connector J6

Pin	Mnemonic	Function
1	+12 VDC	Head load solenoid power source
2	SIDE B L	Solenoid control signal

6.4.5.4 Stepper Motor Connector J7

Pin	Mnemonic	Function
1	STM1	Stepper motor phase 1 control
2	STM2	Stepper motor phase 2 control
3	+12 VDC	Stepper motor +12 Vdc power source
4	STM3	Stepper motor phase 3 control
5	STM4	Stepper motor phase 4 control
6	+12 VDC	Stepper motor +12 Vdc power source

6.4.5.5 Side B Switches and Indicators Connector J8

Pin	Mnemonic	Function
1	WP B H	Write-protect LED
2	SEL B L	Write-protect/diskette present LED select
3	DP B H	Diskette present LED
4	SEL B L	Index LED select
5	INDEX B L	Index LED

6.4.5.6 Side A Head Load Solenoid Connector J10

Pin	Mnemonic	Function
1	+12 VDC	Head load solenoid power source
2	SIDE A L	Solenoid control signal

6.4.5.7 Drive Select Jumper J17

Pin	Mnemonic	Function
1	GND	Ground
2	SEL 1 H	This signal selects the drive configuration. When asserted, and the jumper is removed, DRIVE SEL 0 L and DRIVE SEL 1 L access the drive. When unasserted, and the jumper is installed, DRIVE SEL 2 L and DRIVE SEL 3 L access the drive.

6.4.6 Motor Control Modules Connectors J4, J11, J16

This section describes the connectors of the motor control module. Figure 6-29 shows the location of these connectors and other connectors of the module. Connector J4 connects to the seek and interface modules connector J4 and is described in Paragraph 6.4.2.

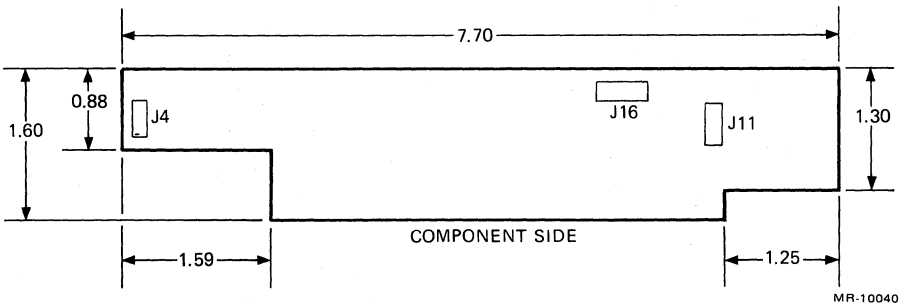


Figure 6-29 Motor Control Module Connector Locations

6.4.6.1 Spindle Motor Connector J11

Pin	Mnemonic	Function
1	TACH 1	Half of tachometer differential pair
2	TACH 2	Half of tachometer differential pair
3	MOT RET	Spindle motor power return
4	+12 VDC	+ 12 V motor power source

6.4.6.2 Front Panel Operational LEDs Connector J16

Pin	Mnemonic	Function
1	+12 VDC	LED power source for side A
2	SIDE A L	Side A LED control signal
3	+12 VDC	LED power source for side B
4	SIDE B L	Side B LED control signal

6.4.7 Read/Write Module Connectors J9, J14, J15

This section describes the connectors of the R/W module. Figure 6-30 shows the location of these connectors and other connectors of the module. Connector J9 connects to the seek and interface modules connector J9 and is described in Paragraph 6.4.3.

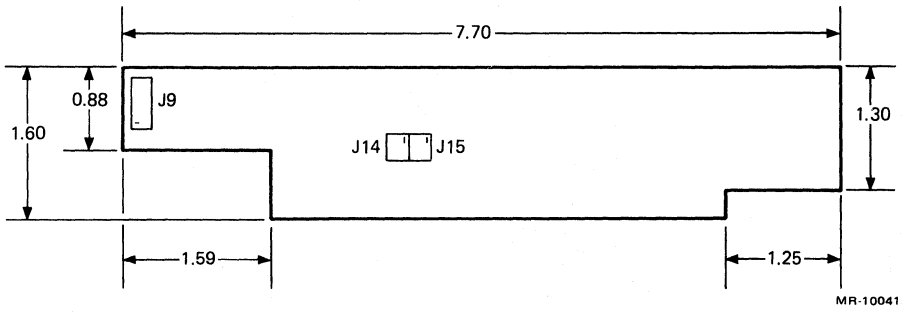


Figure 6-30 Read/Write Module Connector Locations

6.4.7.1 Side A Read, Write, and Erase Head Connector J14

Pin	Mnemonic	Function
1	HEAD SEL A	Side A head common
2	SHIELD	Head control line shield
3	ERASE COIL	Erase coil control line
4	+ COIL	Plus R/W coil control line
5	– COIL	Minus R/W coil control line
6	-	Not used

6.4.7.2 Side B Read, Write, and Erase Head Connector J15

Pin	Mnemonic	Function
1	HEAD SEL B	Side B head common
2	SHIELD	Head control line shield
3	ERASE COIL	Erase coil control line
4	+ COIL	Plus R/W coil control line
5	– COIL	Minus R/W coil control line
6	–	Not used

6.5 SPECIFICATIONS

The following paragraphs provide the specifications for the RX50 dual-diskette drive.

6.5.1 Performance Specifications

Capacity (Formatted)	**MFM**	
Per drive	819,200	(800K bytes)
Per surface	409,600	(400K bytes)
Per track	5,120 bytes	
Diskette quantity	2	

Transfer Rate	**MFM**	
Per drive	250,000	(bits/s)

Access Time	**Minimum**	**Typical**	**Maximum**
Track to track	6 ms	–	–
Head settling time	–	–	30 ms
Head load time	–	–	30 ms
Rotational latency	–	100 ms	200 ms
Random access	–	164 ms	–
Drive motor start	–	–	500 ms

6.5.2 Reliability Specifications

Mean time between failures	6000 power-on hours at 30% duty cycle
Spindle motor	2000 power-on hours at 100% duty cycle
Mean time to repair	15 min
Error rates (Typical Random Exerciser)	
Soft read errors	1 per 10^9 bits read
Hard read errors	1 per 10^{12} bits read
Seek errors	1 per 10^6 seeks
Medium life	3×10^6 passes
Medium insertion	1×10^4 insertions

6.5.3 Functional Specifications

Rotational speed	300 r/min
Speed variations	−1.5% to +1.5% max
Flux density (track 79)	5576 flux changes per inch
Track density	96 tracks per inch
Tracks (per diskette)	80
Outside track radius	57.15 mm (2.25 in)
Inside track radius	36.51 mm (1.427 in)
Data sectors (soft)	10
Data bytes per sector	512
Index	1

6.5.4 Electrical Specifications

Requirement	Minimum	Typical	Maximum
5 V Power	4.75 V	5.0 V	5.25 V
Ripple	–	–	50 mV
Current	–	0.50 A	0.80 A
12 V Power	11.4 V	12.0 V	12.6 V
Ripple	–	–	100 mV
Standby current	–	0.12 A	0.25 A
Operating current (seeking)	–	1.25 A	1.8 A
Start-up current for 0.25 s	–	–	2.7 A

6.5.5 Environmental Specifications

Ambient temperature	15° C to 32° C (59° F to 90° F)
Relative humidity	20% to 80% noncondensing
Maximum wet bulb	25° C (78° F)
Shock and vibration	1 gravity acceleration
Shipping shock	2 gravity acceleration
Diskette jacket	40° C (40° F) max

6.5.6 Mechanical Specifications

Width	14.6.1 mm (5.75 in)
Height	82.55 mm (3.25 in)
Depth	215.9 mm (8.50 in)
Weight	2.18 kg (4.8 lb)
Operating power dissipation	17.5 W typical
Standby power dissipation	4.2 W typical

CHAPTER 7
POWER SUPPLY AND FAN

7.1 INTRODUCTION

This chapter provides a description of the Rainbow 100 computer power supply (part number H7842) and the fan (part number 70-19572). Figure 7-1 shows the relationship of the power supply to other components of the Rainbow 100 computer.

7.2 PHYSICAL DESCRIPTION

The power supply, shown in Figure 7-2, is connected to the other system components as follows:

- To the fan bracket assembly on the front panel through a three- and four-pin connector (on later models, with another connector for dc power)
- To each diskette drive through a four-pin connector mounted on the top cover
- To the system module through a 13-pin connector

The power supply is mounted at the rear of the system unit. A latch locking device on the early system units locks the power supply in place. On later models, a latch on the power supply secures it to the system unit. (See Figure 7-3.) The fan bracket assembly is mounted on the left of the system unit and is held in place with three mounting screws on the top cover. The fan bracket assembly connectors are keyed so they can only be inserted one way.

A circuit breaker is located on the back of the power supply to the left of the ac input connector and an ac selector switch is located below the connector. (See Figure 7-4.) The ac selector switch slides to the right for 115 V and to the left for 230 V.

If 115 V power is applied with the ac selector switch in the 230 V position, the computer will be inoperable, although the fan will operate at a much lower speed. If 230 V power is applied with the selector switch in the 115 V position, internal components will be damaged.

The fuse is located beneath the electromagnetic interference (EMI) filter.

WARNING

The ac select switch must be in the 230 V position when applying 230 V or internal components will be damaged.

WARNING

Before removing the power supply cover, turn off the power and wait five minutes. Before handling any of the power supply components, make certain that there are no high voltages present by checking with a voltmeter.

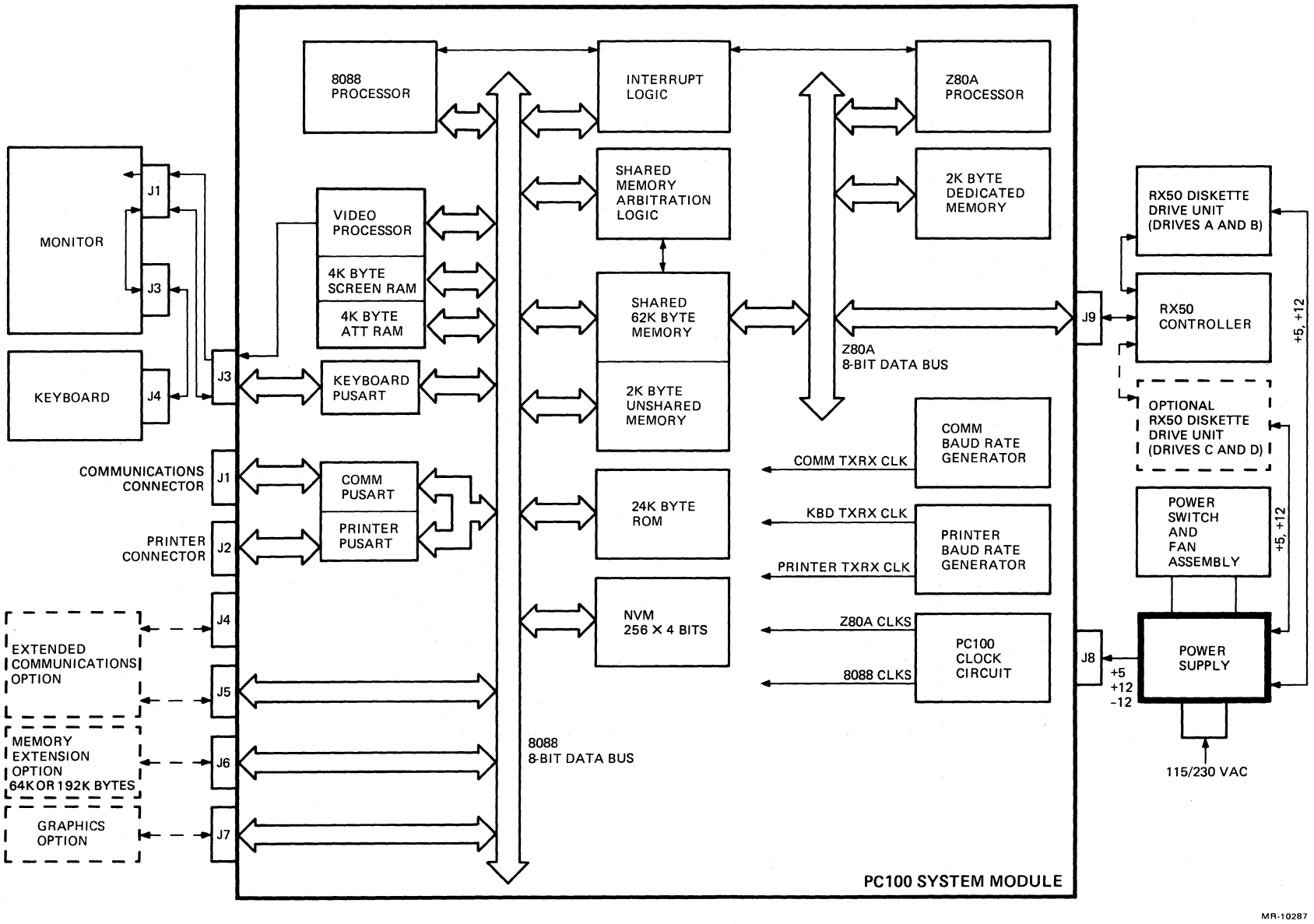


Figure 7-1 System Block Diagram

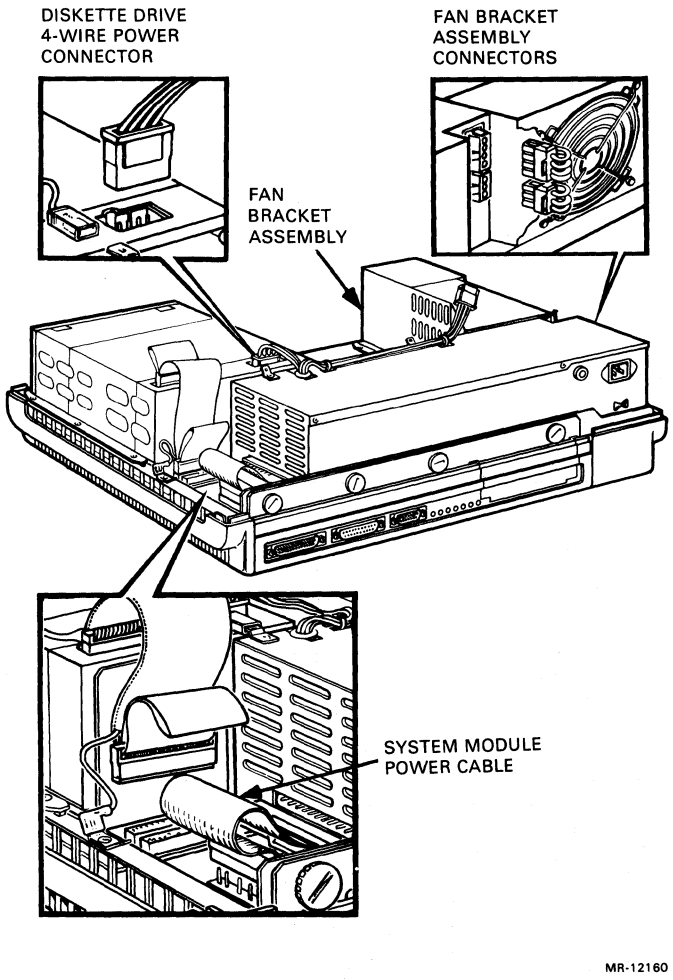


Figure 7-2 Power Supply Connectors

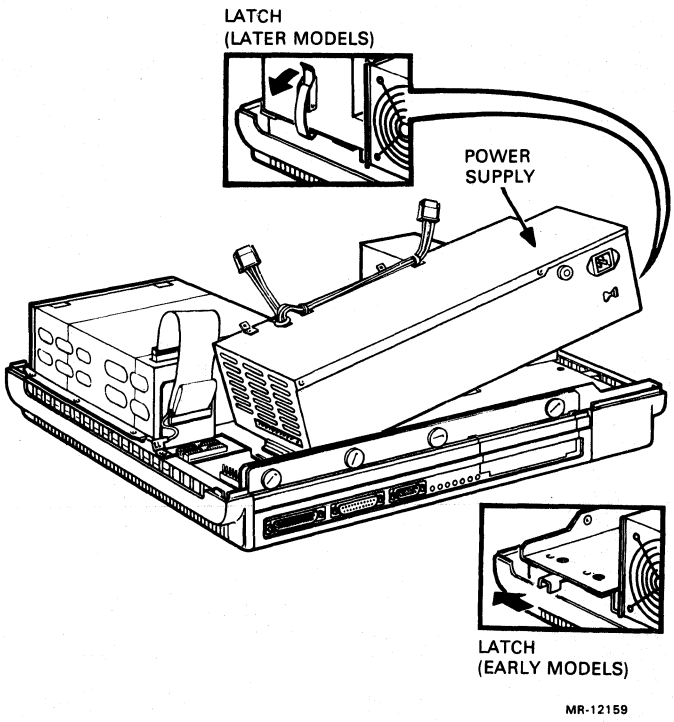


Figure 7-3 Power Supply Latch Types

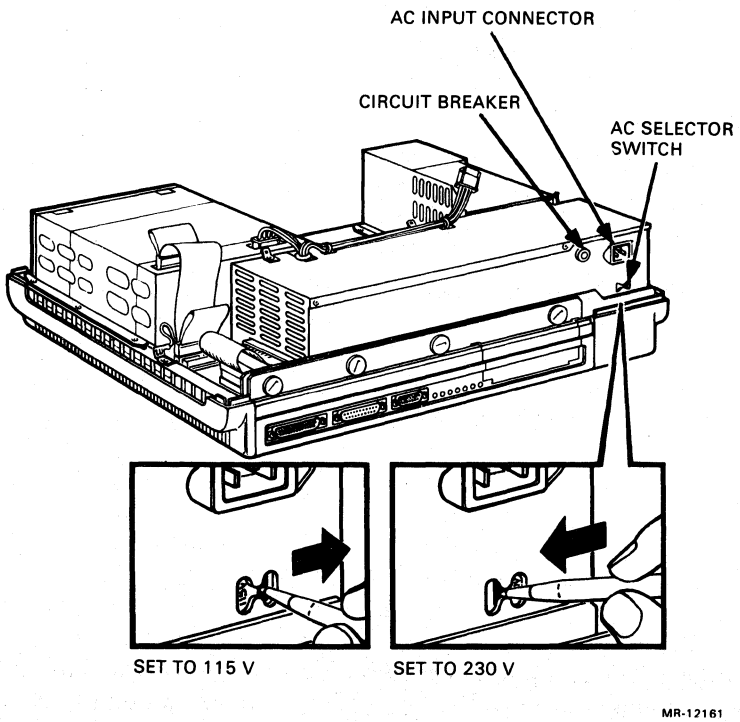


Figure 7-4 AC Input Connector, Circuit Breaker, and AC Selector Switch

7.3 FUNCTIONAL DESCRIPTION

The power supply converts the ac input (either 115 Vac or 230 Vac) to +12, −12, and +5 Vdc. Figure 7-5 is a functional diagram of the power supply and fan assemblies.

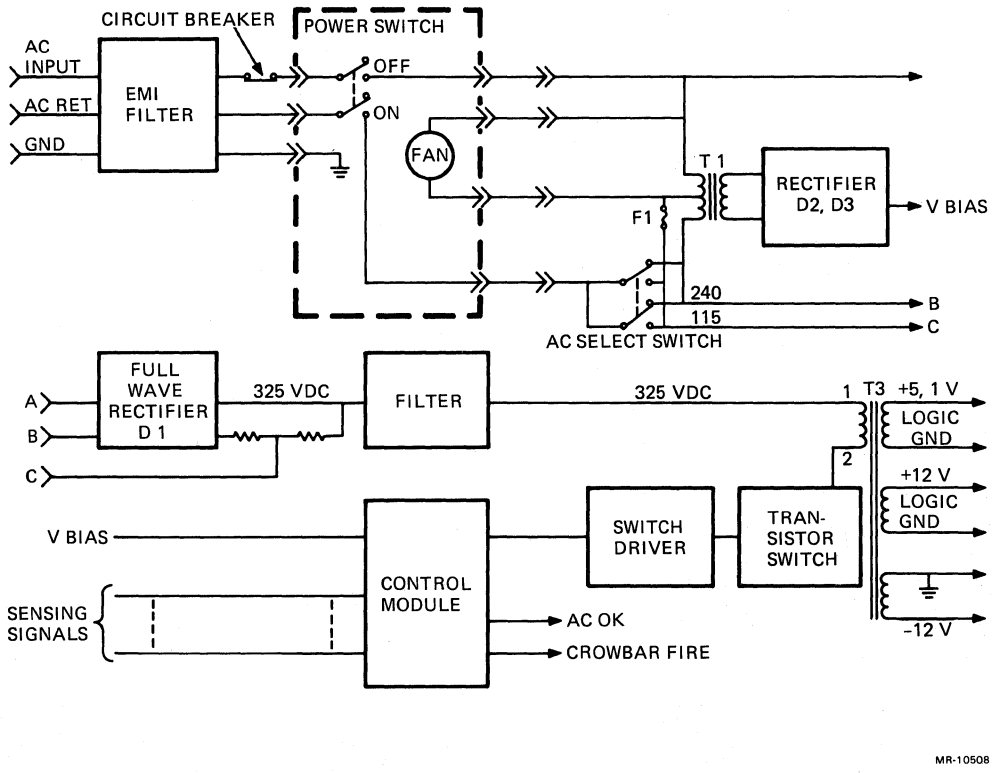


Figure 7-5 Power Supply Functional Diagram

Refer to circuit schematics CS5415187-0-1 and CS5451543-0-1 while reading the functional circuit descriptions.

One side of the ac input line is connected across the EMI filter, a 4A circuit breaker, and a power switch (mounted on the front panel) to the fan, transformer T1, and bridge rectifier D1. The other side of the ac input line is connected across the EMI filter, the power switch, the ac select switch, to T1 (if 230 is selected) or to the fuse and voltage doubler (if 115 is selected). The other side of the fuse is connected to the return side of the fan and the center tap of T1.

The fuse protects the fan from damage caused by applying incorrect ac voltages.

Transformer T1 is used for providing ac voltage to the fan and as ac source voltage for the V bias signal, which is used as the dc source voltage for the control module board.

Bridge rectifier D1 provides full-wave rectifying of the 230 Vac input, and is configured as a voltage doubler circuit when in the 115 Vac input mode. In both cases, the rectifier circuit output is 325 Vdc and is applied to the primary winding (pin 1) of T3. Pin 2 of the primary winding is connected to the transistor switch.

The transistor switch controls current flow through the primary winding of T3 and is turned on and off by the pulse width modulator (PWM) output signal from the control module, through the switch driver (Q4).

Transformer T3 includes three secondary windings that produce all of the output dc voltages. The secondary winding for the +5.1 Vdc supply is made up of two parallel connected windings, while the +12 and −12 Vdc secondary windings are made up of single windings.

7.4 DETAILED CIRCUIT DESCRIPTION

Refer to circuit schematics CS5415187-0-1 and CS5451543-0-1 while reading the detailed circuit descriptions.

7.4.1 Power Conversion Circuits

The output of the bridge rectifier (when 230 V is used) or the voltage doubler (when 115 V is used) is 325 Vdc (measured between pins 1 and 4 of L1). L1 and C3 are used to prevent switching spikes from contaminating the ac input line.

Switching transistor Q1 is controlled by the secondary windings of T2. The switching rate is determined by the output of the pulse width modulator (PWM) from pin 19 of the control module. The PWM output controls switch driver Q4, which induces current flow through the primary of T2. The width of the PWM output pulse is determined by the power supply load, thereby controlling the amount of power that is coupled across transformer T3 to the power supply output.

Transformer T3 consists of three secondary windings. The +5.1 V and +12 V secondaries are operated in the forward converter mode providing half-wave rectifying. Resistors R9 and R14 provide overcurrent sensing information, which is sent to the control module. Overvoltage sensing information from the output lines is also sent to the control module.

A crowbar protection circuit in the +5.1 supply causes the power supply to go into an overcurrent condition whenever the control module senses out-of-tolerance conditions in the output lines. Whenever the crowbar fires, the power supply must be reset in order to clear D10.

The +5.1 Vdc output is filtered and connected to pins 5 and 6 of J2, and pins 7, 8, and 9 of J3.

The +12.2 Vdc output is filtered and connected to pins 5 and 6 of J3, and pins 7 and 8 of J2.

The −12 Vdc secondary is operated in the flyback mode and shunt regulated with Q2, Q3, and zener diode D15. The −12 Vdc output is connected to pin 4 of J3.

7.4.2 Control and Sensing Circuits

The control module monitors the output dc voltages, and shuts down the power supply if the +5.1 Vdc line exceeds its tolerances.

7.4.2.1 AC OK – The ac OK signal is generated (high) as long as a favorable comparison exists between the Bulk Sense signal and the V PR signal. The V PR signal is the V Bias signal zenered down to +5.1 Vdc.

7.4.2.2 Lockout Drive – The lockout drive circuit monitors the V Bias signal. A comparator circuit uses +5.1 Vdc as a reference. If the V Bias signal has not attained a high enough voltage level at turn on, the output of the comparator goes high, which turns on transistor Q1 and then transistor Q4. When Q4 turns on, +12 Vdc is applied to the base of transistor Q4 on the main board, forcing it to stay on and thereby inhibiting any pulses from being transferred to Q1 (the main switching transistor).

7.4.2.3 Crowbar Fire – The crowbar fire circuit monitors the +5 V and −12 V overvoltage sense signals. Whenever any one of these signals exceeds its tolerances, the crowbar fire signal is applied to the crowbar D10 on the main board, causing it to fire and creating an overcurrent condition on the +5.1 Vdc bus.

NOTE
Once the crowbar has fired, it can only be cleared by resetting the power supply.

7.4.2.4 Antisaturation – The antisaturation circuit monitors the voltage across D13, which is a function of the current through pins 5 and 6 of T3. The comparator circuit samples the flyback voltage on a pulse-to-pulse basis.

During a fault condition, when the voltage drop across D13 exceeds the sample input level to the comparator, pin 13 stays high and forces a high on the shutdown pin (10) of the pulse width modulator, thereby shutting it down.

7.4.2.5 Voltage Time Limit (ETL) – The voltage time limit (ETL) circuit compares the half-wave rectified output from the secondary (pins 11 and 12) of T3 against the reference voltage applied to the comparator. As long as the output of the secondary is below the reference voltage, the comparator output remains low; otherwise, it goes high, thereby forcing a high on the shutdown pin (pin 10) of the pulse width modulator. When pin 10 goes high, it shuts down the pulse width modulator.

7.5 SPECIFICATIONS

7.5.1 Input Specifications

7.5.1.1 Voltage

Single Phase, 3 Wire	90 Vrms to 128 Vrms or 180 Vrms to 256 Vrms
Frequency	47 Hz to 63 Hz
Current	3.0 Arms maximum at 115 Vrms 2.0 Arms maximum at 230 Vrms
Input Power	226 VA apparent, 138 W maximum including fan power of 23 W

7.5.1.2 Electrical Magnetic Interference Susceptibility

Conducted Transients

Single voltage transient, survival	Single voltage transient without causing system degradation: 1 kV peak at 2.5 W/s maximum.
Conducted CW noise	Unit operates without error at 3 Vrms superimposed on the ac lines, in the frequency range of 10 kHz to 30 MHz.
RF field susceptibility	10 kHz to 30 MHz: 2 V/M 30 MHz to 1 GHz: 5 V/M with power supply installed.

Power Line Disturbances

Ride-through capability	The power supply provides a minimum of 20 ms ride-through during a power outage condition during low line and full load. During this time, the power supply outputs must be within their specified limits.
Overvoltages	The power supply withstands for one second, maximum, 150 Vac for the 115 Vac configuration, and 300 Vac for the 230 Vac configuration without causing system degradation or damage.
Undervoltages, disturbances, and outages	The power supply withstands undervoltage disturbances and power interruptions without physical damage.
High voltage potential test	Input to frame for 1 minute: 1.25 kVrms, 50 Hz Input to output for 1 minute: 3.75 kVrms, 50 Hz Input to output for 1 minute: 2.5 kVrms, 50 Hz

7.5.2 Output Specifications

7.5.2.1 Output Power

+5.1 V at 2.5 A minimum to 11.5 A maximum
+12.2 V at 0.6 A minimum to 6.7 A maximum
−12 V at 0.0 A minimum to 0.15 A maximum

7.5.2.2 +5 Vdc, +12 Vdc, −12 Vdc Specifications

	+5 Vdc	+12 Vdc	−12 Vdc
Output Voltage Variations:			
Total tolerance	±6%	±6%	±7%
Initial tolerance	±2%	±2%	±3%
Line regulation	±1%	±1%	±1.5%
Load regulation	±3%	±3%	±4.0%
Load interaction	±3%	±3%	±3%
Temperature stability	±0.05%/°C	±0.05%/°C	±0.05%/°C
Long term stability	±1%/1000 h	±1%/1000 h	±1%/1000 h
Ripple and Noise	50 mV peak-to-peak	75 mV peak-to-peak	120 mV peak-to-peak
Overcurrent Trip Point:			
Minimum	10.7 A	6.8 A	0.4 A
Maximum	14.5 A	10.0 A	1.5 A
Short Circuit Current	8.0 A (maximum)	4.0 A (maximum)	3.0 A (maximum)

Overvoltage Protection Range:

Minimum trip point	5.80 V	NA	−13.0 V
Absolute maximum output voltage	7.0 V	NA	−15.0 V

CHAPTER 8
KEYBOARD

8.1 INTRODUCTION

This chapter describes the LK201 keyboard used with the Rainbow 100 computer. The shaded part of Figure 8-1 shows its relationship in the system block diagram.

The keyboard is the user interface to the system. It detects keystrokes, encodes them, and transmits the information to the central processor. The keyboard also receives information from the central processor.

Communication between the keyboard and the central processor in the system unit is full-duplex, serial asynchronous at a speed of 4800 baud. The communication lines conform to EIA Standard RS-423, which applies to unbalanced voltage interfaces.

Refer to the LK201 Maintenance Print Set (MP-01395-00) while reading the following description of the keyboard.

8.2 PHYSICAL DESCRIPTION

The keyboard used with the Rainbow 100 computer has 105 keys arranged in the following four groups. (Refer to Figure 8-2.)

- Main keypad (57 keys)
- Numeric keypad (18 keys)
- Special function keypad (20 keys)
- Editing keypad (10 keys)

The keycaps can be installed manually, but require a special tool for removal. (Refer to Appendix A for part number and ordering information.)

The keyboard circuitry is contained in a low profile cabinet with a nominal height of 30 mm from table top to home row. The keyboard case is made of two plastic shells that can be separated with a screwdriver. Nonslip plastic strips along the bottom prevent the keyboard from sliding on a table top. Two feet can be manually inserted in holes to raise the back edge of the keyboard.

A plastic window along the top edge above the special function keys can be lifted to insert a keyboard label strip. The label, a thin paper strip, fits into the indented space and varies according to the application program.

There are four LEDs located beneath the plastic window. They are labeled HOLD SCREEN, LOCK, COMPOSE, and WAIT.

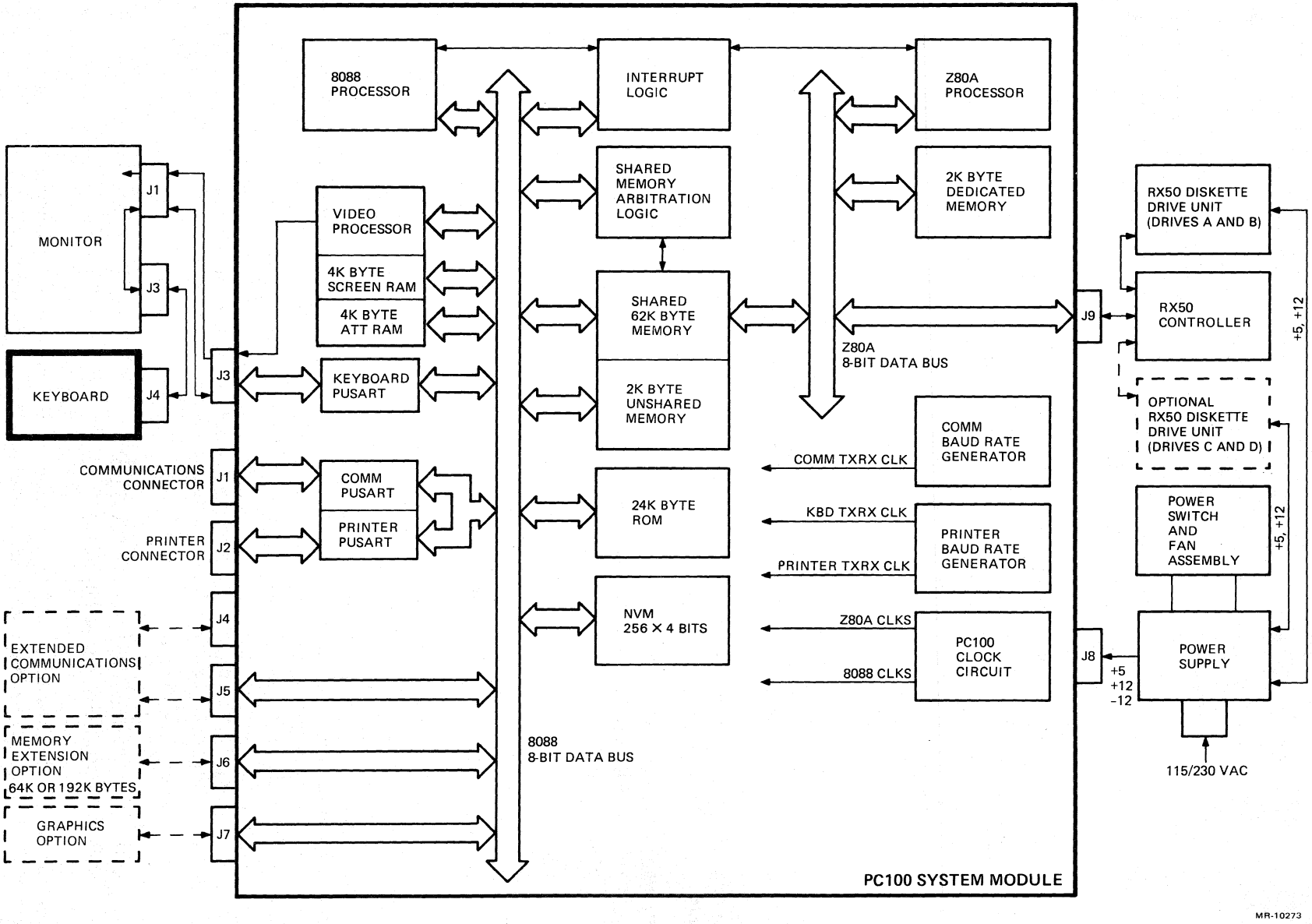


Figure 8-1 System Block Diagram

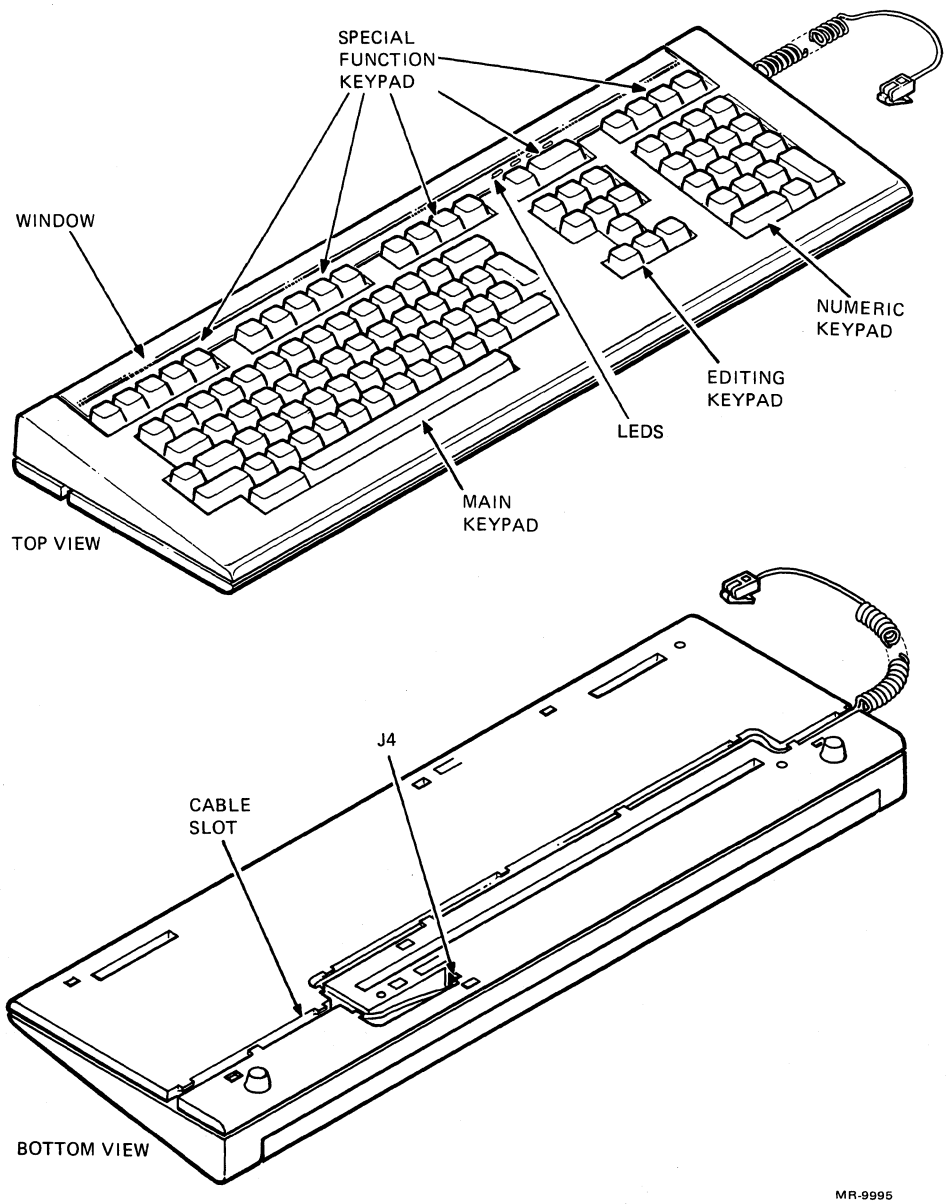


Figure 8-2 LK201 Keyboard

A coiled cable (PN BCC01), with a 4-pin modular connector on each end, connects the keyboard to the video monitor. The keyboard transmits four types of signals to the monitor that pass unchanged via the video cable to the system unit (Figure 8-3). The four signals are as follows:

- +12 V power to keyboard
- Ground to keyboard
- SERIAL OUT (transmit line from keyboard)
- SERIAL IN (receive line to keyboard)

The cable can be placed in a channel in the bottom case and the modular type telephone connector fits into the jack, J4. The cable can be inserted in the channel to either side of the keyboard.

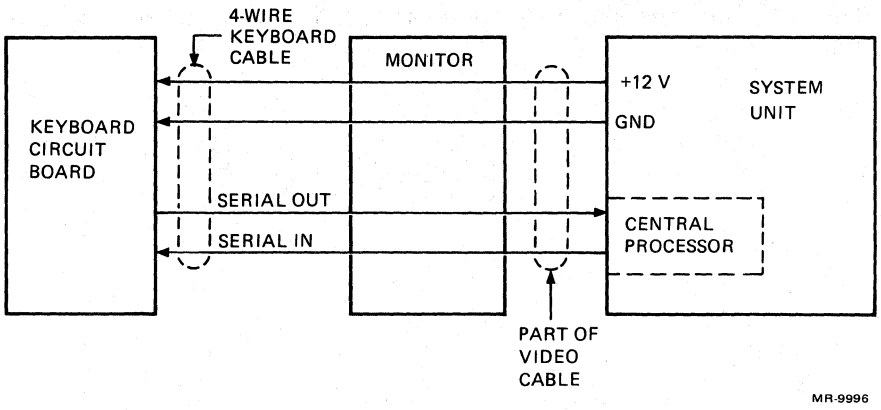


Figure 8-3 Keyboard Cable Connections

8.3 BLOCK DIAGRAM DESCRIPTION

Figure 8-4 shows a simplified block diagram of the keyboard circuitry. Everything except the block marked KEYBOARD MATRIX is on the printed circuit board. This block represents the connections between the keyboard switches and the signals from the 8051 microprocessor.

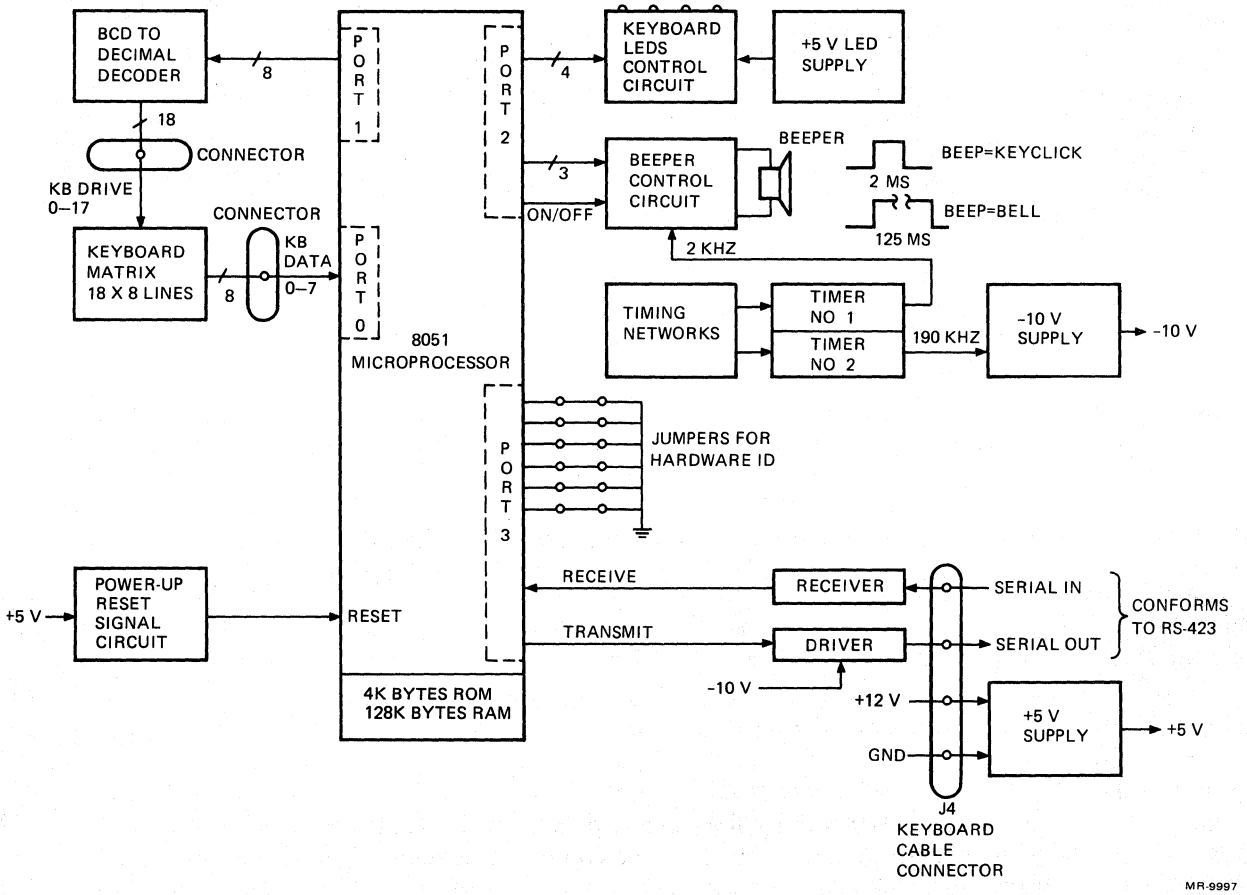


Figure 8-4 Simplified Block Diagram of LK201 Keyboard Circuitry

The firmware in the 8051 8-bit microprocessor controls the following three major keyboard operations at the same time:

1. Scans the keyboard to detect changes in the keyboard matrix
2. Transmits the results of the keyboard scan to the system central processor
3. Receives information from the system central processor

8.3.1 Keyboard Scanning

The keyboard switches are connected at the intersections of an 18 × 8 line matrix. This provides a fixed position identifier for each key.

The firmware scans the 18-line axis and detects a depressed or newly released key by reading the 8-line axis. The firmware then verifies the detected keystroke and changes this positional information into an 8-bit code that is unique to that key.

8.3.2 Control of Audio Transducer and Indicators

Two circuits control the audio transducer and the indicators. One circuit receives its inputs from the 8051 and controls the transducer (beeper). A long beep represents the bell and a short beep represents the keyclick.

A separate circuit, controlled by a signal from the 8051, controls each of the four indicators. The firmware, responding to commands received from the system central processor, turns the indicators on or off.

8.3.3 Keyboard Firmware Functions

This paragraph describes the keyboard firmware functions. The functions are divided into two categories: those that cannot be changed by instructions from the system central processor, and those that can be changed by instructions from the system central processor.

8.3.3.1 Functions Not Changed by System Central Processor Instructions – The following functions cannot be changed by instructions from the system central processor:

- Power-up test
- Keycodes
- Special codes

Power-Up Test

Upon power-up, the firmware performs a selftest in less than 70 ms. The test results are transmitted to the system central processor in four bytes.

The keyboard indicators are lit during the selftest. The indicators blink once during the selftest routine. The indicators go off if the test is passed, but remain lit if the test fails. The system module can also request selftest at any time.

Keycodes

The keycodes represent fixed positions in the key switch matrix. The key associated with a particular matrix position is always represented by the same keycode.

Special Codes

There are 13 special codes transmitted by the keyboard. Four codes transmit the results of the power-up selftest. The other nine codes are status indicators or command acknowledgements.

8.3.3.2 Functions Changed by System Central Processor Instructions – The system central processor can issue instructions to change some keyboard transmission characteristics and to control the keyboard indicators and beeper.

Upon completion of a successful power-up selftest, the firmware sets certain functions to predetermined conditions. They are referred to as default conditions. The conditions can be changed, but they always come up to the default condition after a successful power-up selftest.

8.3.3.3 Firmware Functions That Can be Changed – Certain firmware functions can be changed by commands (instructions) from the system central processor. These commands are categorized as transmission commands and peripheral commands. Transmission commands include a Mode Set command and an Auto-Repeat Rate Set command. Peripheral commands include a variety of commands. For more information refer to Peripheral Commands, Paragraph 8.5.5.3.

8.4 DETAILED KEYBOARD CIRCUIT DESCRIPTION

The following section describes the keyboard circuitry. Figure 8-4 shows the LK201 keyboard block diagram.

8.4.1 Keyboard Matrix Scanning

The key locations are arranged in an 18 × 8 line matrix. Each key switch is connected across a matrix intersection. This gives a fixed position for each key connected in the matrix. This matrix accommodates all 105 keys in the LK201 keyboard.

Figure 8-5 is a simplified block diagram of the matrix scanning circuit. Eight lines from port 1 of the 8051 microprocessor go to the binary coded decimal (BCD) inputs of two 74LS145 BCD-to-decimal decoders. Ten outputs from one decoder and eight outputs from the other decoder provide the drive lines for the matrix. These 18 lines are called KB DRIVE 0–17.

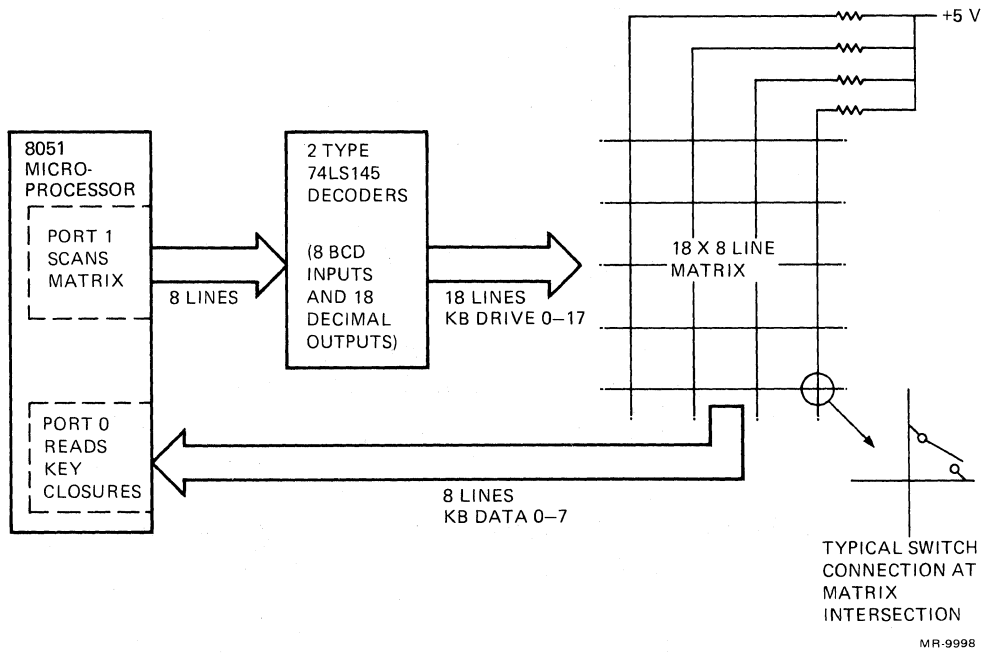


Figure 8-5 Simplified Block Diagram of Matrix Scanning Circuit

The other axis of the matrix consists of eight lines tied to +5 V through pull-up resistors. These lines go to port 0 of the 8051 microprocessor and are called KB DATA 0–7.

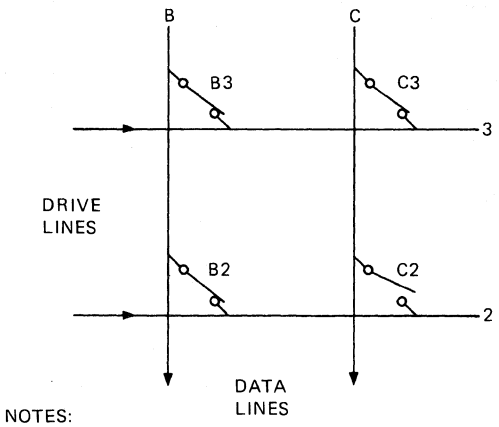
The 8051 scans the 18 drive lines. Key closures are detected by reading the eight data lines. The complete matrix is scanned every 8.33 ms.

When a key closure is detected, it is scanned again to verify that it is a key closure and not electrical noise.

Once the key closure is verified, the 8051 firmware translates the position information into a key code and transmits it to the system central processor. Transmission is handled by the Universal Asynchronous Receiver Transmitter (UART) in the 8051.

A sneak path or ghost key indication can occur when three of the four corners of a matrix rectangle are closed (Figure 8-6). The key positions in the matrix are arranged to avoid sneak paths. However, if a sneak path does occur, the firmware prevents the keycode for the key (which caused the sneak path) to be transmitted until one of the involved keys is released. This prevents transmission of ghost keys entirely.

Table 8-1 shows the keyboard matrix on the LK201-AA (U.S.A.) keyboard. Keycap designations are shown for reference only and can be compared to Figure 8-7.



NOTES:

1. CONDITIONS ARE: SWITCHES B2, B3, AND C3 CLOSED, SWITCH C2 OPEN; LINE 2 IS BEING DRIVEN, AND LINE C IS BEING READ.
2. INTERSECTION C2 IS BEING LOOKED AT. IT SHOULD NOT SHOW A KEY CLOSURE BECAUSE SWITCH C2 IS OPEN.
3. HOWEVER, A SNEAK PATH IS PRESENT FROM LINE 2 THROUGH SWITCHES B2, B3, AND C3 TO LINE C. A GHOST KEY IS READ AT INTERSECTION C2.

MR-9999

Figure 8-6 Example of Ghost Key Generation

Table 8-1 Keyboard Matrix (LK201-AA)

KB Drive	KB Data 7	6	5	4	3	2	1	0
17	Reserved	F19	Reserved	F20	PF4	N— (Note 1)	N,	Enter
		G22		G23	E23	D23	C23	A23
16	F18	PF3	Reserved	N9	↓	N6	N3	N.
	G21	E22		D22	B17	C22	B22	A22
15	F17	PF2	Reserved	N8	N5	→	N2	N0 (Note 2)
	G20	E21		D21	C21	B18	B21	
14	PF1	Next Screen	Remove	↑	N7	N4	N1	N0
	E20	D18	E18	C17	D20	C20	B20	A20
13	Insert Here	— -	DO	Prev Screen	{ [	" '	Reserved	Reserved
	E17	E11	G16	D17	D11	C11		
12	Find	+ =	Help	Select	}]	Return	←	
	E16	E12	G15	D16	D12	C13	B16	C12
11	Addtnl Options	⟨X⟩ (delete)	Reserved	) 0	P	(Note 3)	: ;	? /
	G14	E13		E10	D10		C10	B10
10	Reserved	F12 (BS)	Reserved	F13 (LF)	(9	O	L	.
		G12		G13	E09	D09	C09	B09
9	Reserved	F11 (ESC)	Reserved	Reserved	* 8	I	K	, ,
		G11			E08	D08	C08	B08
8	Reserved	Main Screen	Reserved	Exit	& 7	U	J	M
		G08		G09	E07	D07	C07	B07

NOTES

1. Note that N0–N9, N—, N, and N. refer to the numeric keypad.
2. N0 of the numeric keypad can be divided into two keys. Normally only the N0 keyswitch is implemented as a double-size key.
3. The Return key occupies two positions which are decoded as the Return (C13) key.

Table 8-1 Keyboard Matrix (LK201-AA) (Cont)

KB Drive	KB Data 7	6	5	4	3	2	1	0
7	Reserved	Cancel	Reserved	Resume	^ 6	Y	H	N
		G07		G06	E06	D06	C06	B06
6	Reserved	Reserved	Reserved	Inter-rupt	% 5	T	G	B
				G05	E05	D05	C05	B05
5	F4	Break	Reserved	$ 4	R	F	V	SPACE
	G02	G03		E04	D04	C04	B04	A01–A09
4	Reserved	Print Screen	Reserved	Set-Up	# 3	E	D	C
		G00		G01	E03	D03	C03	B03
3	Hold Screen	@ 2	Reserved	Tab	W	S	X	> <
	G99	E02		D00	D02	C02	B02	B00
2	Reserved	Reserved	Reserved	~	! 1	Q	A	Z
				E00	E01	D01	C01	B01
1	Ctrl	Lock	Compose	Reserved				
	C99	C00	A99					
0	Shift							
	B99,B11							

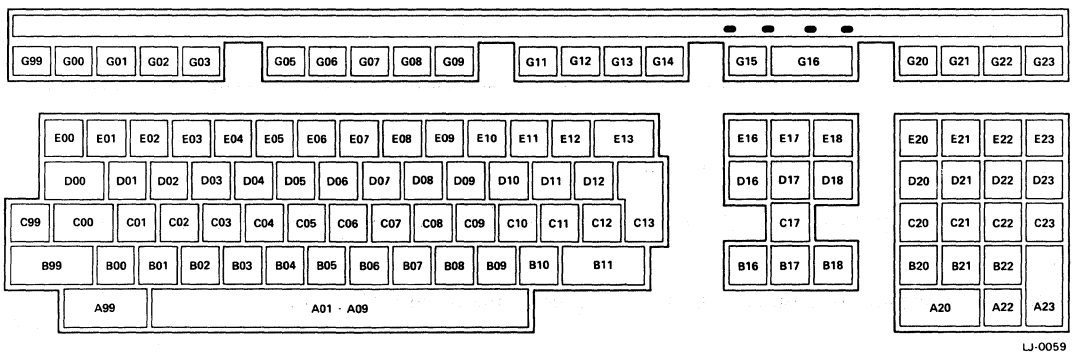


Figure 8-7 LK201 Keyboard Layout

8.4.2 Audio Transducer Control Circuit

Figure 8-8 shows the audio transducer or beeper control circuit. The beeper is driven by a transistor whose base is connected to a 2 kHz square wave from a 556 timer IC. This signal is biased by a network of four type 74LS05 open collector inverters. The 8051 microprocessor controls all four inverters via the firmware. The ON/OFF inverter connects directly to the transistor base. When the 8051 puts a high on the ON/OFF inverter input, its output goes low and removes the 2 kHz square wave from the transistor base. This cuts off the transistor and disables the beeper.

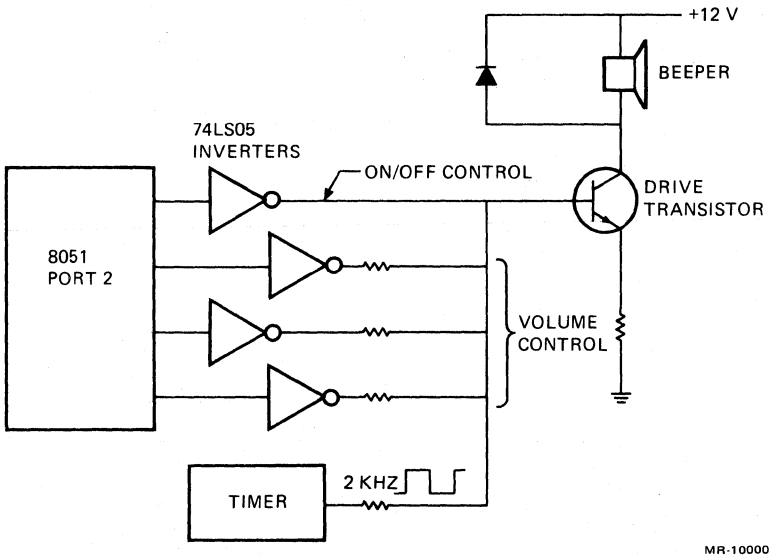


Figure 8-8 Audio Transducer (Beeper) Control Circuit

To turn on the beeper, the 8051 puts a low on the ON/OFF inverter input. Its output goes high and allows the 2 kHz signal to reach the transistor base. This turns on the beeper. The firmware generates a keyclick (on for 2 ms) or a bell tone (on for 125 ms).
The 8051 sets up the three level control inverters by putting one of eight binary combinations on the inverter inputs. All highs give the softest sound and all lows give the loudest sound.

The firmware controls the keyclick and the bell tone independently. The bell tone is sounded only upon request from the system control processor. The keyclick is sounded (unless disabled) under the following conditions:

- When a key is pressed
- When a metronome code is sent
- When a command to sound the keyclick is received from the system control processor

8.4.3 Indicator (LED) Control Circuit

Figure 8-9 shows the LED indicator control circuit.

The control signal for each LED comes from port 2 of the 8051 to the input of a type 74LS05 open collector inverter. The inverter output goes to the LED cathode; its anode is connected to +5 V. A separate +5 V source relieves the LED's load on the main +5 V supply.

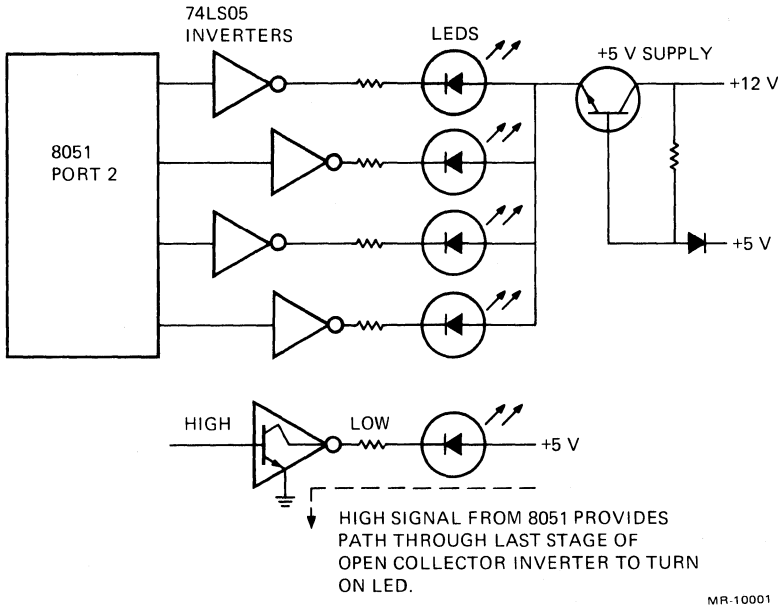


Figure 8-9 Indicator (LED) Control Circuit

A low signal from the 8051 drives the inverter output high, which cuts off the LED. A high signal from the 8051 drives the inverter output low. This provides a path to ground from the +5 V through the LED. The LED then turns on.

8.4.4 Keyboard Communication

8.4.4.1 Keyboard Transmit Mode – The keyboard codes and a few other special codes are transmitted via a serial line output in port 3 of the 8051. The transmitted signal goes from the 8051 to a driver, through the keyboard cable, monitor, and video cable to the system central processor. A UART within the 8051 controls the transmission.

Transmitted characters conform to a specific format. Each character is 10 bits long. The first bit is the START bit. It is always a logical 0 (space). The next eight bits represent the encoded data. The last bit is the STOP bit. It is always a logical 1 (mark). Figure 8-10 shows the character format.

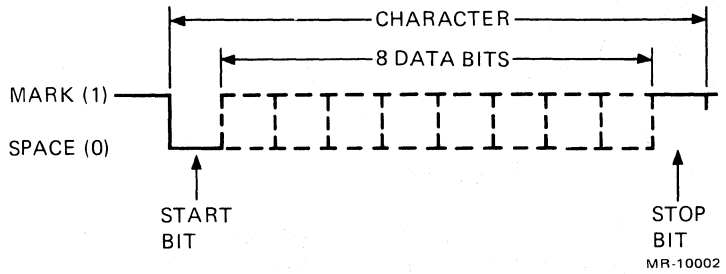


Figure 8-10 Keyboard Transmit and Receive Character Format

8.4.4.2 Keyboard Receive Mode – The firmware contains features that can be enabled by commands from the system central processor. There are two categories of features: one sets keyboard transmission characteristics, and the other controls the keyboard peripherals. A peripheral command covers indicator control, bell and keyclick volume, keyboard ID code, and reinstate keyboard. The commands come from the system central processor, through the video cable, monitor, and keyboard cable to the receiver and into the 8051 via port 3. They go to the UART in the 8051.

Received characters conform to the same 10-bit format used for transmitted characters. The eight data bits are arranged in a specified protocol depending on the command type.

8.4.5 Reset Signal for 8051 Microprocessor

Whenever the system is turned on, the 8051 microprocessor in the keyboard must be reset. This allows the 8051 to start operating.

The reset signal generator is active only during power-up. The input is +5 V. The output is connected to the reset input of the 8051. When power is turned on, the +5 voltage starts to rise from zero. The reset signal circuit output follows it and drops off when a steady state of +5 V is reached. This circuit holds the 8051 reset input high (+3.5 V to +5 V) long enough to enable the reset action in the 8051. This action occurs only during power-up.

8.4.6 Hardware Keyboard Identification (ID)

At power-up, the keyboard performs a selftest and sends the results to the system central processor. One piece of information to be sent is the keyboard hardware ID which is read from hardwired jumpers.

There are six jumpers. Each jumper line goes from an input in port 3 of the 8051 to ground. All jumpers are installed so the keyboard hardware ID is zero.

8.4.7 Voltage Supplies

The only voltage sent to the keyboard is +12 V. However, +5 V and −10 V are also required. These voltages are derived from the +12 V.

There is a +5 V supply that handles most of the requirements for this voltage. The four keyboard LEDs have their own +5 V supply. A −10 V supply provides voltage for the driver in the SERIAL OUT line.

8.5 KEYBOARD PROGRAMMING

This section describes the functions that the keyboard performs under system central processor control. It also describes keyboard programming machine language. High level user programming is not described here.

8.5.1 Keyboard Layout and Key Identification

Each keyboard key has a unique location. Each location is scanned, and when closure or release is detected, the location is verified. This is then decoded to an 8-bit keycode. Figure 8-7 shows the keyswitch locations. Table 8-2 shows the 14 functional divisions of the keyboard. Table 8-3 shows the divisions, keycaps, and keycodes.

Table 8-2 Keyboard Functional Divisions

Division	Description	Representation
1	48 graphic keys, spacebar	0001
2	Numeric keypad	0010
3	Delete character (E12)	0011
4	Return (C13) Tab (D00)	0100
5	Lock (C00) Compose (A99)	0101
6	Shift (B99 and B11), Ctrl (C99)	0110
7	Horizontal cursors (B16 and B18)	0111
8	Vertical cursors (B17 and C17)	1000
9	Six keys directly above the cursor keys (D16–D18 and E16–E18)	1001
10	Function keys (G99–G03)	1010
11	Function keys (G05–G09)	1011
12	Function keys (G11–G14)	1100
13	Function keys (G15–G16)	1101
14	Function keys (G20–G23)	1110

Table 8-3 Keycode Translation Table

Division	Position	Keycap*	Keycode† (decimal)	Keycode (hexadecimal)
Function Keys				
10	G99	Hold Screen	086	56
	G00	Print Screen	087	57
	G01	Set-Up	088	58
	G02	F4	089	59
	G03	Break	090	5A
		Reserved	091–098	5B–62
11		Reserved	099	63
	G05	Interrupt	100	64
	G06	Resume	101	65
	G07	Cancel	102	66
	G08	Main Screen	103	67
	G09	Exit	104	68
		Reserved	105–110	69–6E
12			111	6F
		Reserved	112	70
	G11	F11 (ESC)	113	71
	G12	F12 (BS)	114	72
	G13	F13 (LF)	115	73
	G14	Addtnl Options	116	74
		Reserved	117–122	75–7A
13		Reserved	123	7B
	G15	Help	124	7C
	G16	Do	125	7D
14		Reserved	126–127	7E–7F
	G20	F17	128	80
	G21	F18	129	81
	G22	F19	130	82
	G23	F20	131	83
		Reserved	132–135	84–87
Basic Editing Keys				
9		Reserved	136–137	88–89
	E16	Find	138	8A
	E17	Insert Here	139	8B
	E18	Remove	140	8C
	D16	Select	141	8D
	D17	Prev Screen	142	8E
	D18	Next Screen	143	8F
		Reserved	144	90

*The legends under **Keycap** are taken from the keycap legends of the LK201-AA (U.S.A.).
†Keycodes 000 through 064 are reserved. Keycodes 065 through 085 are unused.

Table 8-3 Keycode Translation Table (Cont)

Division	Position	Keycap*	Keycode† (decimal)	Keycode (hexadecimal)
Numeric Keypad				
2		Reserved	145	91
	A20	0	146	92
		Reserved	147	93
	A22	.	148	94
	A23	Enter	149	95
	B20	1	150	96
	B21	2	151	97
	B22	3	152	98
	C20	4	153	99
	C21	5	154	9A
	C22	6	155	9B
	C23	,	156	9C
	D20	7	157	9D
	D21	8	158	9E
	D22	9	159	9F
	D23	-	160	A0
	E20	PF1	161	A1
	E21	PF2	162	A2
	E22	PF3	163	A3
	E23	PF4	164	A4
		Reserved	165	A5
Cursor Keys				
7		Reserved	166	A6
	B16	Left	167	A7
	B18	Right	168	A8
8	B17	Down	169	A9
	C17	Up	170	AA
		Reserved	171–172	AB–AC
Shift, Lock, Ctrl, A99, and A10				
6		Reserved	173	AD
	B99,B11	Shift	174	AE
	C99	Ctrl	175	AF
5	C00	Lock	176	B0
	A99	Compose	177	B1
		Reserved	178	B2

*The legends under **Keycap** are taken from the keycap legends of the LK201-AA (U.S.A.).
†Keycodes 000 through 064 are reserved. Keycodes 065 through 085 are unused.

Table 8-3 Keycode Translation Table (Cont)

Division	Position	Keycap*	Keycode† (decimal)	Keycode (hexadecimal)
Special Codes				
		All Ups	179	B3
		Metronome	180	B4
		Output error	181	B5
		Input error	182	B6
		KBD LOCKED acknowledge	183	B7
		TEST MODE acknowledge	184	B8
		PREFIX to keys down	185	B9
		MODE CHANGE acknowledge	186	BA
		Reserved	187	BB
Delete				
3	E13	Delete ⟨X⟩	188	BC
Return and Tab				
4	C13	Return	189	BD
	D00	Tab	190	BE
48 Graphics Keys and Space Bar				
2	E00	~	191	BF
	E01	!1	192	D0
	D01	Q	193	C1
	C01	A	194	C2
	B01	Z	195	C3
		Reserved	196	C4
	E02	@2	197	C5
	D02	W	198	C6
	C02	S	199	C7
	B02	X	200	C8
	B00	><	201	C9
		Reserved	202	CA
	E03	#3	203	CB
	D03	E	204	CC
	C03	D	205	CD
	B03	C	206	CE
		Reserved	207	CF

*The legends under **Keycap** are taken from the keycap legends of the LK201-AA (U.S.A.).

†Keycodes 000 through 064 are reserved. Keycodes 065 through 085 are unused.

Table 8-3 Keycode Translation Table (Cont)

Division	Position	Keycap*	Keycode† (decimal)	Keycode (hexadecimal)
	E04	$4	208	D0
	D04	R	209	D1
	C04	F	210	D2
	C04	V	211	D3
	A01–A09	Space	212	D4
		Reserved	213	D5
	E05	%5	214	D6
	D05	T	215	D7
	C05	G	216	D8
	B05	B	217	D9
		Reserved	218	DA
	E06	^6	219	DB
	D06	Y	220	DC
	C06	H	221	DD
	B06	N	222	DE
		Reserved	223	DF
	E07	&7	224	E0
	D07	U	225	E1
	C07	J	226	E2
	B07	M	227	E3
		Reserved	228	E4
	C08	*8	229	E5
	D08	I	230	E6
	C08	K	231	E7
	B08	"	232	E8
		Reserved	233	E9
	E09	(9	234	EA
	D09	0	235	EB
	C09	L	236	EC
	B09	. .	237	ED
		Reserved	238	EE
	E10	)0	239	EF
	D10	P	240	F0
		Reserved	241	F1
	C10	: ;	242	F2
	B10	? /	243	F3
		Reserved	244	F4
	E12	+ =	245	F5
	D12	}]	246	F6
	C12	| \	247	F7
		Reserved	248	F8
	E11	_ -	249	F9
	D11	{ [	250	FA
	C11	' "	251	FB
		Reserved	252-255	FC-FF

8.5.2 Modes

This section describes the function of the keycode transmission modes. The Mode Set command allows any one of the 14 keyboard divisions to be set to any one of the following three modes. (Division defaults are described in subsequent paragraphs.)

Down only mode – The keyboard transmits a keycode when the key is pressed.

Auto-repeat down – The keyboard transmits a keycode when the key is first pressed. If the key is held down past the specified timeout period (usually 300 to 500 ms), a fixed metronome code is sent at the specified rate until the key is released.

Down/up – The keyboard transmits a keycode when the key is pressed and an up code when the key is released. If any other down/up keys are pressed, the up code is a repeat of the down code. If no other down/up keys are pressed, the keyboard sends an ALL UPS code.

8.5.2.1 Special Considerations Regarding Auto-Repeat – The Auto-Repeat Rate Set command allows the following changes in the auto-repeat mode:

- The auto-repeat rate buffer association can be changed for the selected keyboard division.
- The timeout and interval values can be changed in any one of the four auto-repeat rate buffers.
- If multiple auto-repeating keys are held down, metronome codes are still generated. The metronome codes apply to the keycode transmitted most recently. If the last key pressed down is released, and another key is still down, the keycode of the key still down is retransmitted.

  Example: The **A** key is held down.

  This produces the following transmission:

  A metronome metronome

  Now the **B** key is pressed. This produces the following transmission:

  A metronome metronome B metronome metronome

  Now the **B** key is released. This produces the following transmission:

  A metronome metronome B metronome metronome A metronome met . . .

  While metronome codes are being generated for an auto-repeating key, a nonauto-repeating keycode or special code may be transmitted. The keyboard transmits this special code instead of the next metronome code and then returns to the auto-repeated code. The keycode to be auto-repeated is always the last byte transmitted.

  Example: The **A** key is held down.

  This produces the following transmission:

  A metronome metronome

Now the **SHIFT** key is pressed. This produces the following transmission:

A metronome metronome shift A metronome

Now the **SHIFT** key is released. This produces the following transmission:

A metronome metronome shift A metronome ALL UPS A metronome . . .

- If an auto-repeating key is not to auto-repeat (for example, **Ctrl C**), the system module must issue a Temporary Inhibit Auto-Repeat command. This halts the transmission of any metronome codes or keyclicks for that key only. Metronome codes continue when another key is pressed. The command must be issued after the keycode for the auto-repeating key is received.

- Auto-repeat can be enabled and disabled independently of the division settings by using the Enable/Disable Auto-Repeat commands. These commands apply to all keys on the keyboard. When auto-repeat is disabled, internally the keyboard continues to auto-repeat characters. However, it does not transmit metronome codes or keyclicks. When auto-repeat is enabled, the keyboard transmits the metronome codes from the point where they were before auto-repeat was disabled. This may be within either the timeout or interval period, depending upon the time elapsed since the key was pressed.

- If the keyboard receives a request to change a division mode to auto-repeat while a key is being pressed, the keyboard makes the change immediately. After the specified timeout period, the keyboard transmits metronome codes for the pressed key. In place of the first metronome code, the keyboard transmits the keycode of the auto-repeating key.

All auto-repeating division modes can be changed to down only with one command. This and other auto-repeat commands are grouped with the peripheral commands. (See Peripheral Commands, Paragraph 8.5.5.3.)

8.5.2.2 Special Considerations Regarding Down/Up Mode – If two down/up keys are released simultaneously (within the same scan), and there are no other down/up keys down on the keyboard, only one ALL UPS code is generated.

8.5.2.3 Auto-Repeat Rates – There are four buffers in the keyboard to store auto-repeat rates. They are numbered 0 through 3. Each buffer stores the following two values. These values can be changed by the system module.

- The timeout value
- The interval value

Timeout is the amount of time that the keyboard waits before starting to auto-repeat a character. The timeout value is the amount of time between the detection of a down key and the transmission of the first metronome code (defaults range from 300 to 500 ms). The rate of auto-repeating a character is called the interval. The interval value is the number of metronome codes per second (defaults to 30).

Each division is associated with one of the four buffers. Rates are taken from the associated buffer each time the auto-repeat timers are loaded. This buffer-to-division association can be changed by the system module or left to default.

8.5.3 Keyboard Peripherals

This section describes the peripherals available on the keyboard. The keyclick, bell, and LEDs are all considered keyboard peripherals. See Peripheral Commands, Paragraph 8.5.5.3, for information on system module control of these peripherals.

8.5.3.1 Audio – The keyclick is a 2 ms beep and the bell is a 125 ms beep. The bell is sounded only upon request from the system module. The keyclick (if not disabled by the system module) is sounded under the following three conditions:

- When a key is pressed
- When a metronome code is sent
- When the system module receives a sound keyclick command

If either the **B11** or **B99** keys (the left and right **SHIFT** keys on the LK201) or the **C99** key (the **Ctrl** key on the LK201) are pressed, the keyclick is not generated. However, if a command is sent from the system module to enable the keyclick on the **C99** key, the keyclick is generated (Peripheral Commands, Paragraph 8.5.5.3). Figure 8-7 shows the positions of these keys.

The keyclick or bell (or both) may be disabled and will not sound. If the system module requests sound (see Peripheral Commands, Paragraph 8.5.5.3), the keyclick or the bell does not sound.

Both the keyclick and bell may be set independently to one of the following eight volume levels:

000 – highest
001
010 – default
011
100
101
110
111 – lowest

8.5.3.2 Indicators (LEDs) – The system module normally transmits indicator control commands. However, the following are exceptions:

- Upon power-up, the keyboard turns all LEDs off.
- After receiving the Inhibit Transmission command, the keyboard turns on the LOCK LED. The LED is turned off after the keyboard receives a Resume Transmission command.

8.5.4 Keyboard-to-System Module Protocol

The following paragraphs describe the keyboard-to-system module protocol.

8.5.4.1 Keycode Transmission – The keyboard transmits single byte keycodes that reflect the keyboard matrix status. The 8-bit codes above 64 (decimal) are used for keycodes. Every key is identified by a unique keycode. There are no special codes for shifted or control keys.

Refer to Figure 8-7 and Tables 8-1 and 8-3 for the complete keycode matrix translation table.

8.5.4.2 Special Code Transmission – There are 13 special codes: nine codes with values above 64 (decimal) and four codes below.

The following are the nine special codes above 64 (decimal) keycode value range:

Special Codes	Keycode (Decimal)	Keycode (Hexadecimal)
ALL UPS	179	B3
METRONOME CODE	180	B4
OUTPUT ERROR	181	B5
INPUT ERROR	182	B6
KBD LOCKED ACK	183	B7
TEST MODE ACK	184	B8
PREFIX TO KEYS DOWN	185	B9
MODE CHANGE ACK	186	BA
RESERVED	127	7F

ALL UPS – indicates to the system module that a down/up mode key was just released and no other down/up keys are being pressed.

METRONOME CODE – indicates to the system module that an interval has passed, a keyclick has been generated, and the last key received by the system module is still being pressed.

OUTPUT ERROR – indicates an output buffer overflow to the system module. The overflow occurred after receiving a Keyboard Inhibit command from the system module and some keystrokes may be lost.

INPUT ERROR CODE – indicates to the system module that the keyboard received a meaningless command, too many, or too few parameters.

KEYBOARD LOCKED ACKNOWLEDGE – indicates to the system module that the keyboard received an Inhibit Transmission command (see Peripheral Commands, Paragraph 8.5.5.3).

TEST MODE ACKNOWLEDGE – indicates that the keyboard has entered test mode. This is a special mode used during the production test. If the system module receives this acknowledge, it sends 80 hexadecimal. This terminates the test mode and jumps to power-up.

PREFIX TO KEYS DOWN – indicates that the next byte is a keycode for a key already down in a division which has been changed to down/up (Mode Set Commands, Paragraph 8.5.5.4).

MODE CHANGE ACKNOWLEDGE – indicates that the keyboard has received and processed a Mode Change command (see Mode Set Commands, Paragraph 8.5.5.4).

RESERVED – Keycode 7F is reserved for internal use.

The following four special codes are below 64 (decimal) value range:

Special Codes	Keycode (Decimal)	Keycode (Hexadecimal)
KEYBOARD ID – FIRMWARE	01	01
KEYBOARD ID – HARDWARE	00	00
KEY DOWN ON POWER-UP ERROR CODE	61	3D
POWER-UP SELFTEST ERROR CODE	62	3E

KEYBOARD ID – This is a two byte identification code, transmitted after the power-up selftest (Power-Up Transmission, Paragraph 8.5.4.3). It is also sent on request from the system module (see Peripheral Commands, Paragraph 8.5.5.3).

KEY DOWN ON POWER-UP ERROR CODE – indicates that a key was pressed on power-up.

POWER-UP SELFTEST ERROR CODE – indicates to the system module that the ROM or RAM selftest of the system module failed (see Power-Up Transmission, Paragraph 8.5.4.3).

8.5.4.3 Power-Up Transmission – Upon power-up, the keyboard performs a selftest in less than 70 ms. It transmits the selftest results to the system module in 4 bytes.

Byte 1: KBID (firmware) – This is the keyboard identification (ID) that is stored in the firmware.

Byte 2: KBID (hardware) – This is the keyboard ID that is read from hardware jumpers.

Byte 3: ERROR – Two error codes indicate either failure of the ROM or RAM selftest within the processor (3E hexadecimal), or keydown on power-up (3D hexadecimal). No error is indicated by 00.

Byte 4: KEYCODE – This byte contains the first keycode detected if there was a key down on power-up. No error is indicated by 00.

If the ROM selftest (CHECKSUM) fails and the error is fatal, the keyboard is unable to transmit. Nonfatal errors permit the keyboard to continue operation.

If the keyboard finds a key down on the first scan, it continues to look for an ALL UP condition. The keyboard sends the corrected 4-byte power-up sequence when the depressed key is released. This avoids a fatal error condition if a key is pressed by mistake while powering up.

The keyboard LEDs are lit during the power-up selftest. If the selftest is passed, the keyboard turns the LEDs off. If a bell is selected on power-up, the system module can transmit a Sound Bell command to the keyboard. However, this should not be done until the system module receives the last byte of the 4-byte sequence. The request for selftest tests the serial line and system module connection. The power-up selftest takes 70 ms or less.

The system module can request a jump to power-up at any time. This causes the LEDs on the keyboard to blink on and off (for the power-up selftest).

8.5.5 System Module to Keyboard Protocol

The system module controls both the peripherals associated with the keyboard and the keyboard transmit characteristics. Figure 8-11 shows the protocol for the transmission of commands and parameters from the system module to the keyboard.

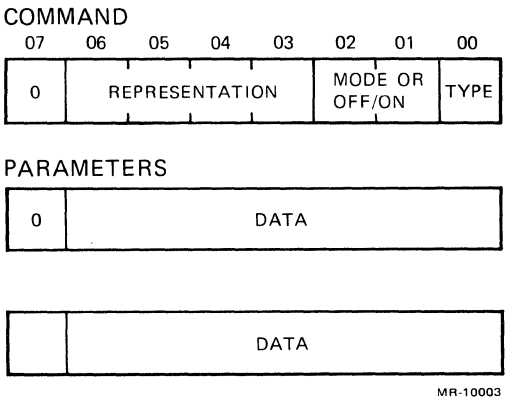


Figure 8-11 System Module to Keyboard Protocol

8.5.5.1 Commands – There are two kinds of commands—those that control keyboard transmission characteristics and those that control keyboard peripherals. The low bit of the command is the TYPE flag. It is clear if the command is a transmission command. It is set if the command is a peripheral command.

Transmission Commands	**Peripheral Commands**
Mode Set	Flow Control
Auto-Repeat Rate Set	Indicator
	Audio
	Keyboard ID
	Reinitiate Keyboard
	Some Auto-Repeat Control
	Jump to Test Mode
	Reinstate Defaults

The high order bit of every command is the PARAMS flag. If there are any parameters to follow, this flag is clear. If there are no parameters, this flag is set.

8.5.5.2 Parameters – The high order bit of every parameter is the PARAMS flag. It is clear if there are parameters to follow. It is set on the last parameter. The remaining seven bits of the parameter are for data.

8.5.5.3 Peripheral Commands – Two commands can turn the data flow from the keyboard off and on:

- Inhibit Keyboard Transmission – This command shuts off or locks the keyboard and turns on the LOCK LED. After receiving the Inhibit command, the keyboard sends a special command to the system central processor. If the system central processor receives this code without requesting it, this indicates that noise on the line was interpreted as the Inhibit command. The central processor then responds immediately with the Resume Keyboard Transmission command.

- Resume Keyboard Transmission – This command turns on or unlocks the keyboard and turns off the LOCK LED. If any keystrokes are lost, the keyboard responds with an error code.

Each keyboard LED can be turned on and off.

The following are the eight commands that control the keyclick and bell sounds:

- Disable Keyclick
- Enable Keyclick and Set Volume
- Disable **Ctrl** Keyclick
- Enable **Ctrl** Keyclick
- Sound Keyclick
- Disable Bell
- Enable Bell and Set Volume
- Sound Bell

The following four commands are related to the control of the auto-repeat mode:

- Temporary Auto-Repeat Inhibit – Auto-repeat is stopped for a specific key only. It resumes automatically when another key is pressed.

- Enable Auto-Repeat Across the Board – Starts transmission of metronome codes without affecting auto-repeat timing or keyboard division.

- Disable Auto-Repeat Across the Board – Stops transmission of metronome codes without affecting auto-repeat timing or keyboard division.

- Change All Auto-Repeat to Down Only – Changes all keyboard auto-repeating divisions to down only mode.

The following are three other miscellaneous commands:

- Request Keyboard ID – The keyboard sends the two-byte ID (firmware and hardware). The keyboard does not jump to the power-up sequence.

- Reinitiate Keyboard – The keyboard jumps to the power-up sequence. Transmission to the keyboard should be held until the host processor receives the last byte of the power-up selftest.

- Reinstate Defaults – Sets the following functions back to the default settings after a successful completion of the power-up selftest:

  Division mode settings
  Auto-repeat interval and timeout rates
  Auto-repeat buffer selections
  Audio volume
  Ctrl key keyclick

To send a peripheral command, set the TYPE flag (low order bit). Bits 6–3 contain a command representation from the chart below. Bits 2 and 1 specify on (01), off (00), or sound (11). Bit 7 should be set if there are no parameters to follow.

See Table 8-4 for the peripheral commands (in hexadecimal).

Table 8-4 Peripheral Commands in Hexadecimal

Function	Hexadecimal	Parameters
Flow control		
Resume Keyboard Transmission	8B	None
Inhibit Keyboard Transmission	89	None
Indicators		
Light LEDs	13	Bit pattern
Turn Off LEDs	11	Bit pattern
Audio		
Disable Keyclick	99	None
Enable Click, Set Volume	1B	Volume
Disable Ctrl Keyclick	B9	None
Enable Ctrl Keyclick	BB	None
Sound Keyclick	9F	None
Disable Bell	A1	None
Enable Bell, Set Volume	23	Volume
Sound Bell	A7	None
Auto-repeat		
Temporary Auto-Repeat Inhibit	C1	None
Enable Auto-Repeat Across Keyboard	E3	None
Disable Auto-Repeat Across Keyboard	E1	None
Change All Auto-Repeat to Down Only	D9	None
Other		
Request Keyboard ID	AB	None
Jump to Power-Up	FD	None
Jump to Test Mode	CB	None
Reinstate Defaults	D3	None

Command	Representation
Flow Control	0001
Indicator (LEDs)	0010
Keyclick	0011
Bell	0100
Keyboard ID	0101
Keyclick for **Ctrl** Key	0111
Temporarily Inhibit Auto-Repeat	1000
Jump to Test Mode	1001
Change All Auto-Repeat Characters to Down Only	1010
Enable/Disable Auto-Repeat	1100

The Jump to Power-Up command is FD hexadecimal.

The following are some of the peripheral commands:

- Flow Control – The system module can lock the keyboard with the Inhibit Keyboard Transmission command. When the keyboard is unlocked, it responds with an error code if any keystrokes were missed (see Keyboard Locked Condition, Paragraph 8.5.6.2).
- Indicators (LEDs) – Figure 8-12 shows the LED parameter. Figure 8-13 shows the LED layout on the LK201 keyboard without the label strip installed.
- Audio – Figure 8-14 shows the audio volume parameter.

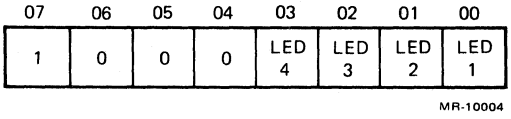


Figure 8-12 Indicator (LED) Parameter

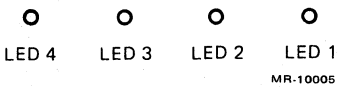


Figure 8-13 Indicator (LED) Layout

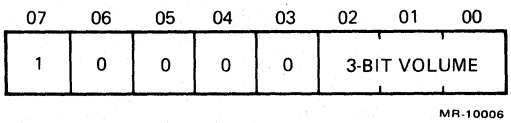


Figure 8-14 Audio Volume Parameter

The volume levels for the audio are as follows:

000 – highest
001
010
011
100
101
110
111 – lowest

The keyclick or the bell (or both) can be disabled. When the keyclick or bell is disabled, it does not sound, even if the system module requests it.

The following are additional peripheral commands:

- Temporary Auto-Repeat Inhibit – Stops auto-repeat for this key only. Auto-repeat automatically continues when another key is pressed.
- Disable/Enable Auto-Repeat Across Keyboard – Stops/starts transmission of metronome codes without affecting auto-repeat timing or division settings.
- Change All Auto-Repeat to Down Only – Changes division settings for all auto-repeating divisions to down only.
- Request Keyboard ID – Keyboard sends a 2-byte keyboard ID. Keyboard does not jump to power-up.
- Reinitiate Keyboard – Keyboard jumps to its power-up routine. The system module should not try to transmit anything to the keyboard until the last byte of the power-up sequence is received.
- Jump to Test Mode – Special test mode for manufacturing testing.
- Reinstate Defaults – Set the following functions back to the default settings after a successful completion of the power-up selftest:

  Division mode settings
  Auto-repeat interval and timeout rates
  Auto-repeat buffer selections
  Audio volume
  Ctrl key keyclick

8.5.5.4 Mode Set Commands – The following describe the Mode Set commands:

- Division mode settings – See Modes, Paragraph 8.5.2, for an explanation of transmission modes and rates.
- Each division on the keyboard has a unique 4-bit representation (see Keyboard Layout and Key Identification, Paragraph 8.5.1). Table 8-2 describes these representations.
- Each mode has a unique 2-bit code.

Modes	Representation
Down only	00
Auto-repeat down	01
Down/up	11

To set the key transmission mode on a particular keyboard division, the system module must send the PARAMS flag, then the keyboard division representation with the mode code, and then followed by the TYPE flag (cleared).

Example: Set main array to down/up (Figure 8-15).

The PARAMS flag is set to 1 if there are no parameters. The PARAMS flag is clear if there are parameters.

Auto-repeat rate buffer association – If the auto-repeat mode is selected, the system module can transmit a parameter to change the buffer association of the selected division. Refer to Auto-Repeat Rates, Paragraph 8.5.2.3, and Default Conditions, Paragraph 8.5.7, for additional information.

Example: Set main array to auto-repeat, change buffer association to buffer 3 (Figure 8-16).

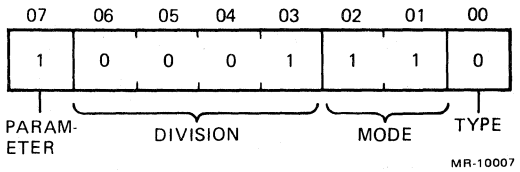


Figure 8-15 Setting Key Transmission Mode

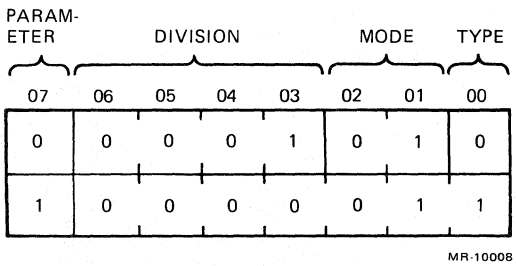


Figure 8-16 Setting Auto-Repeat Rate Buffer Association

Auto-repeat rate buffer values – At keyboard power-up time, the four auto-repeat rate buffers contain default values (see Auto-Repeat Rates, Paragraph 8.5.2.3, and Default Conditions, Paragraph 8.5.7). The system module may change these values.

In the command byte, bit 7 (PARAMS flag) should be clear, bits 6–3 are 1111 (to indicate that this is a Rate Set command), bits 2 and 1 should be the buffer number (0 to 3), bit 0 (TYPE flag) is clear.

There should be two parameters carrying the rate set data.

Example: Change rates in buffer 3 (Figure 8-17).

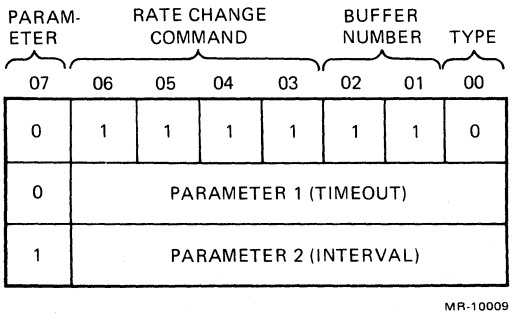


Figure 8-17 Setting Auto-Repeat Rate Buffer Values

The first parameter specifies the timeout to the store in the selected buffer. The second parameter specifies the interval. See Special Considerations Regarding Auto-Repeat, Paragraph 8.5.2.1, for definitions of these parameters.

For example, to set the auto-repeat rate in buffer 1, the system module firmware transmits 00000011 followed by two bytes of numeric parameters.

The auto-repeat timeout is the transmitted number times 5 ms. To specify a rate of 5 ms delay, the first parameter received is 00000001. The maximum allowable time is 630 ms (01111110). The system module must not send 635 (01111111).

NOTE

The code (01111111) is reserved for internal keyboard use. 00 is an illegal value.

Auto-repeat timeout is implemented as a multiple of 8.33 ms, the keyboard's internal scan rate. Timeout rates can vary ± 4.15 ms.

The auto-repeat interval is the number of metronome codes per second. In order to specify a speed of 16 Hz, the second parameter received is 10010000. Note that the high order bit is set because it is the last parameter. The highest value that may be sent is 124 (11111100).

The lowest rate that can be implemented by the keyboard is 12 Hz. Values as low as 1 can be transmitted, but are translated to 12 Hz.

NOTE

The system module must not send 125 – or 11111101. This code is the Power-Up command.

8.5.6 Special Considerations

The following paragraphs describe the special codes and their considerations.

8.5.6.1 Error Handling – There are four error codes. The first two are sent at power-up if the selftest fails (see Power-Up Transmission, Paragraph 8.5.4.3). The other two codes are the INPUT ERROR code and the OUTPUT ERROR code.

The OUTPUT ERROR (B5 hexadecimal) is sent after the keyboard receives a Resume Transmission command, if the output buffer overflowed while the keyboard was locked.

The INPUT ERROR (B6 hexadecimal) is sent when the keyboard detects noise (unidentified command or parameter) on the line. B6 is also sent if the keyboard detects a delay of more than 100 ms when expecting a parameter.

8.5.6.2 Keyboard Locked Condition – When the keyboard receives an Inhibit Transmission command, it lights the LOCK LED and transmits one more byte. This is a special code indicating that the keyboard is locked (KEYBOARD LOCKED ACKNOWLEDGE). If the system module receives this code without a request, it indicates that noise on the line was interpreted as an Inhibit Transmission command. The system module should immediately send the Resume Transmission command to unlock the keyboard.

The output first in first out (FIFO) buffer in RAM is four bytes. When the keyboard is locked, it attempts to store characters received from the keyboard. The keyboard stops scanning its matrix. When the keyboard is unlocked by the system module, it transmits all four bytes in the output buffer. If any keystrokes have been missed due to buffer overflow, the keyboard transmits an error code as the fifth byte (OUTPUT ERROR). Any keys that were not transmitted and are being held down when the keyboard is unlocked are processed as new keys. An error code upon unlocking the keyboard indicates a possible loss of keystrokes to the system module.

The keyboard stops scanning its matrix when its buffer is full. However, it processes all incoming commands.

8.5.6.3 Reserved Code – The number 7F (hexadecimal) is reserved for the internal keyboard input and output buffers handling routines.

8.5.6.4 Test Mode – The keyboard jumps into a test mode by command during production test. It transmits a special code to the system module to confirm the test mode. If the system module receives this code, it should send the byte 80 (hexadecimal) to continue. This causes a jump to power-up.

8.5.6.5 Future Expansion – Some keycodes are reserved for future use as special codes or keycodes. Table 8-5 lists these reserved codes.

Table 8-5 Keyboard Division Default Modes

Keyboard Division	Mode	AR Buffer
Main array	Auto-repeat	0
Keypad	Auto-repeat	0
Delete	Auto-repeat	1
Cursor keys	Auto-repeat	1
Return and Tab	Down only	
Lock and Compose	Down only	
Shift and Control	Down/up	
Six basic editing keys	Down/up	

Table 8-6 Default Rates in Auto-Repeat Buffers

Buffer Number	Timeout (ms)	Internal (Hz)
0	500	30
1	300	30
2	500	40
3	300	40

8.5.7 Default Conditions

- Certain keyboard divisions have specific default modes. Some divisions default to the auto-repeat mode; therefore, they have an associated buffer that contains the default values for timeout and interval. Table 8-5 shows the default modes and Table 8-6 shows the default rates in the four keyboard division auto-repeat rate buffers.

- The volume level for the keyclick and bell has an eight step range. The default volume level for the keyclick and bell is the third loudest. Both keyclick and bell volumes are 2 decimal (010 binary) by default. The key in position C99 of the keyboard (the **Ctrl** key in the LK201) does not generate a click unless enabled by the system module. The keys in position B99 and B11 (**SHIFT** keys on the LK201) never generate a keyclick.

- For the LK201 keyboard, the **Ctrl** key defaults to the no keyclick state.

8.6 SPECIFICATIONS

8.6.1 Functional

Electronics	8-bit microprocessor, 4K bytes of ROM, 256 bytes of RAM, 4 LEDs, transducer
Cord	1.9 m (6 ft), coiled, 4-pin telephone-type modular connectors, plugs into display monitor (PN BCC01)
Keypad	Sculptured key array
Home row key height	3 cm (1.2 in) above desk top
Keys	105 matte, textured-finish keys
Main keypad	57 keys
Numeric keypad	18 keys
Special function keypad	20 keys; firmware and software driven
Editing keypad	10 keys

Spacing	1.9 cm (0.75 in) center-to-center (single-width keys)
Wobble	Less than 0.5 cm (0.020 in)
Diagnostics	Power-up selftest, generates identification upon passing test

8.6.2 Physical

Height	5 cm (2.0 in) at highest point
Length	53.3 cm (21 in)
Width	17.1 cm (6.75 in)
Weight	2 kg (4.5 lb)

CHAPTER 9
VIDEO MONITOR

9.1 INTRODUCTION

The VR201 monochrome monitor is a raster scan device for displaying alphanumeric/graphic video information. The shaded part of Figure 9-1 shows its relationship in the system block diagram. Refer to the VR201 Monochrome Monitor Field Maintenance Print Set (MP-01410-00) while reading this chapter.

The VR201 monochrome monitor is enclosed in a wedge-shaped cabinet (Figure 9-2). The CRT face provides a viewing area of 12.7 × 20.3 cm (5 × 8 inches) on a screen that measures 30.5 cm (12 inches) diagonally. A plastic button covers a screw on the cabinet rear. This screw holds the cabinet to the internal wire frame. The CRT and the monochrome monitor module are mounted inside this frame.

The frame has metal finger stock that presses against the screw mounting bracket and a metal shield. To prevent electromagnetic radiation, this shield covers the entire inside of the cabinet. There is a folding handle on the bottom rear of the cabinet.

The glass front of the monitor, the CRT face, is coated with a special treatment to reduce glare to the operator.

The monitor viewing angle is adjustable between +5 to −25 degrees. To adjust the angle, the operator pushes a release on the right side. This causes a friction lock foot to drop down from the bottom of the cabinet housing.

The contrast and brightness controls are on the rear panel. There are also two connectors on the rear of the monitor: J1 and J3. J1 is a 15-pin D-type connector that connects to the system unit with a cable (PN BCC02). J3, a modular telephone-type jack, connects to the keyboard with another cable (PN BCC01).

The following are the physical dimensions of the monochrome monitor:

Height	24.38 cm (9.75 in)
Width	29.33 cm (11.73 in)
Depth	30.57 cm (12.23 in)
Weight	6.6 kg (14.5 lb)

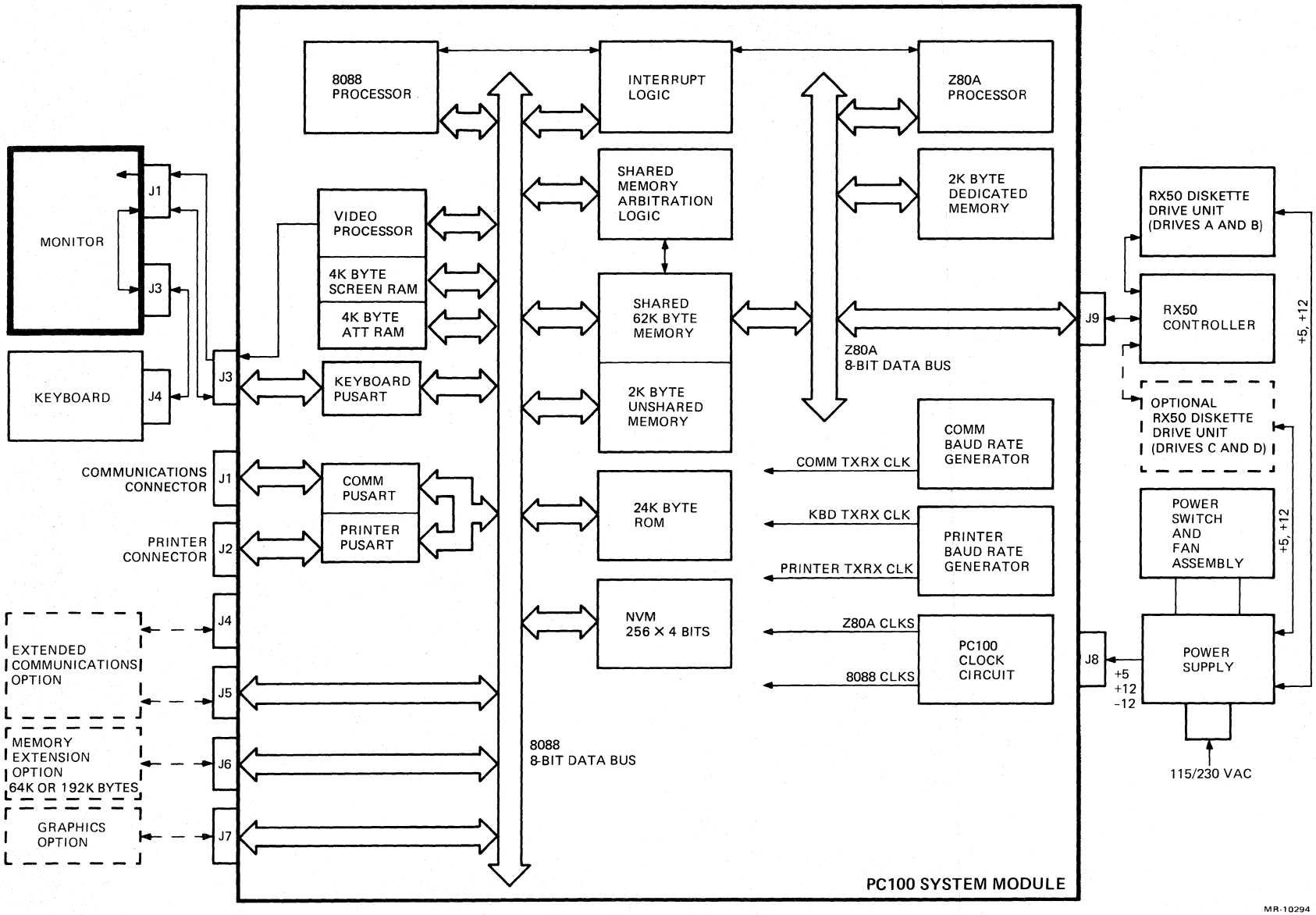


Figure 9-1 System Block Diagram

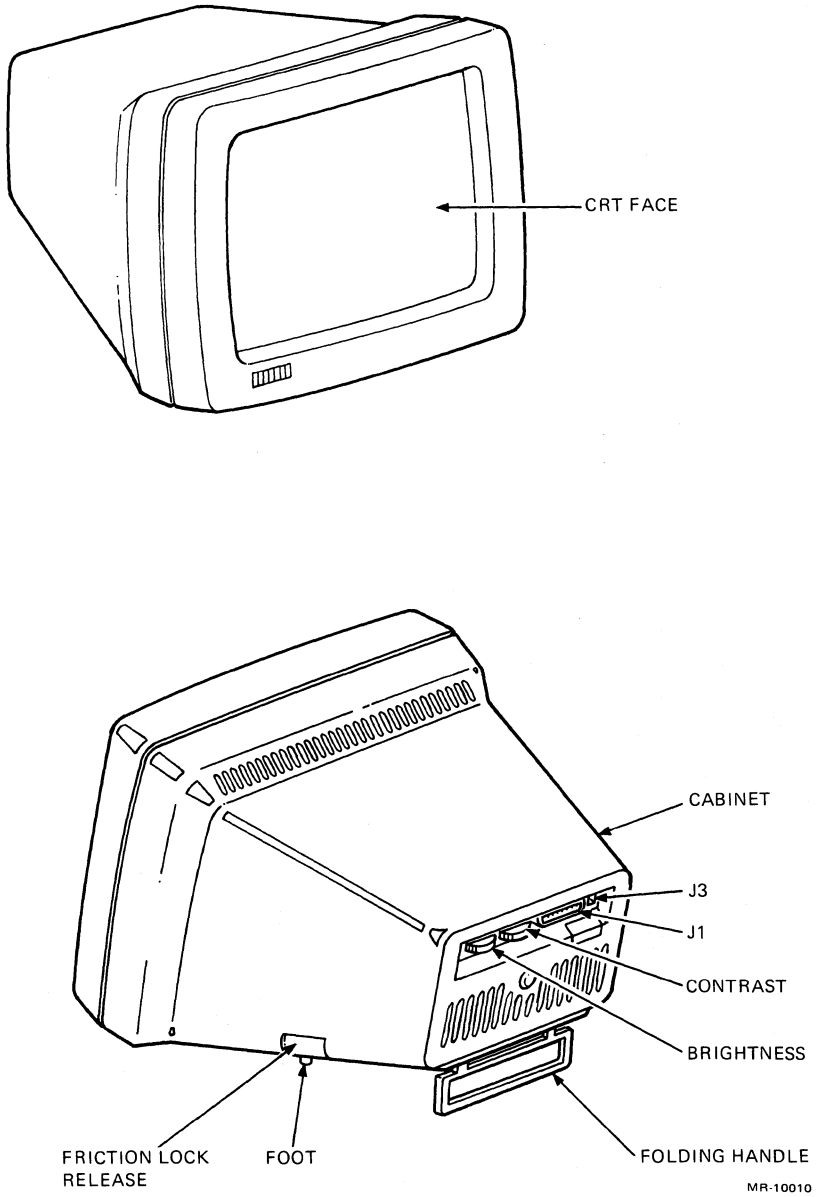


Figure 9-2 VR201 Monochrome Monitor Exterior View

9.2 BLOCK DIAGRAM DESCRIPTION

The VR201 monochrome monitor consists of two main components: a 12-inch diagonal CRT with a yoke assembly mounted on it, and a monitor module (Figure 9-3).

Display activity is the primary function of the monitor. A secondary function is to route information between the system unit and the keyboard. The keyboard connects with the monitor via J3 (Figure 9-3). J3 is hardwired on the module to J1, which connects to the system unit.

The monitor module controls the CRT and the yoke assembly. A composite video signal is input to the module from the system unit (Figure 9-4). This signal consists of two types of information: video data (Paragraph 9.2.1), and sync data (Paragraph 9.2.2).

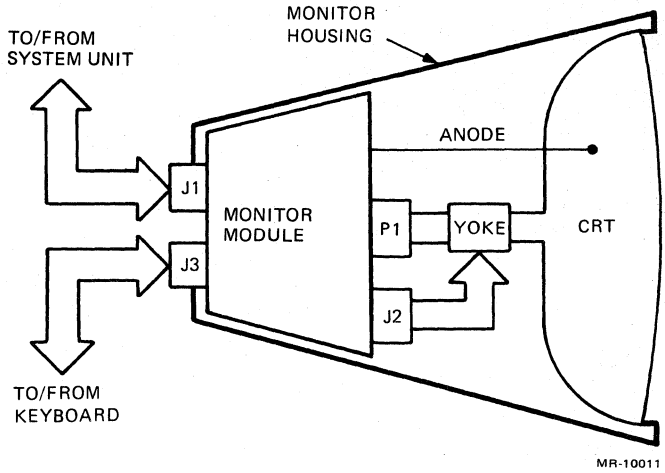


Figure 9-3 VR201 Monochrome Monitor Block Diagram

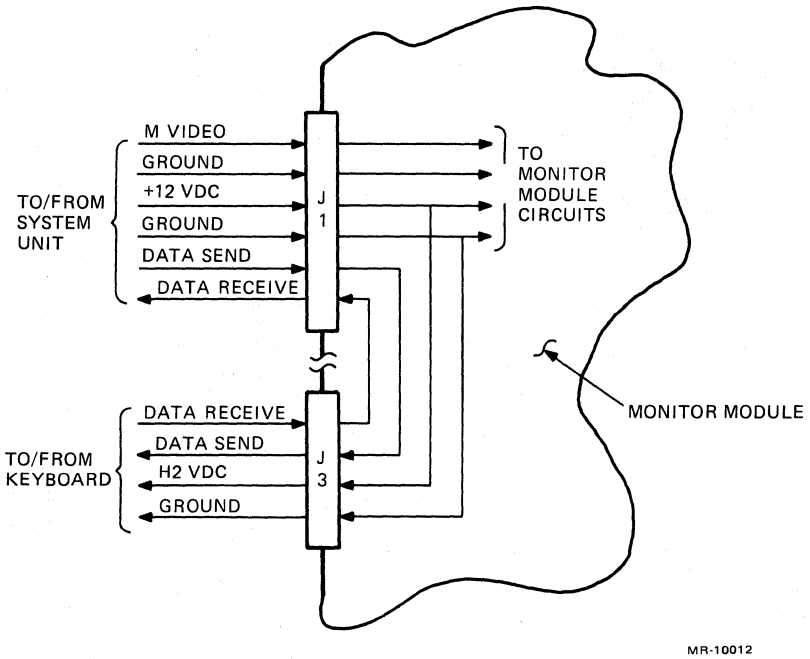


Figure 9-4 VR201 Monochrome Monitor System Communications Diagram

The monitor module provides the following power to the CRT:

- Anode voltage
- Grid 1 voltage (brightness)
- Grid 2 voltage (cutoff)
- Grid 4 voltage (focus)
- Heater voltage
- Cathode voltage

The control inputs to the CRT refine the electron beam. The anode voltage attracts the beam to the faceplate and provides a single connection between the CRT and the module (Figure 9-3). P1 provides all other CRT inputs. P1 is mounted directly on the CRT and is hardwired to the module.

9.2.1 Video Data

The monitor module uses the video portion of the signal to generate outputs to the CRT cathode. The CRT responds to the video by generating various intensities in the electron beam. The intensity of the beam is dependent on the amplitude of the video signal provided.

9.2.2 Sync Data

The sync portion of the video synchronizes the generation of horizontal and vertical signals to the yoke assembly. The horizontal and vertical processor chips use peak detector circuits to separate the synchronizing signals. The yoke assembly, which connects to the monitor module via J2, consists of electromagnetic coils (Figure 9-3). These coils use the signals output by the module to generate magnetic fields which position the electron beam generated by the CRT. The horizontal signal to the yoke controls the sweep of the electron beam horizontally across the faceplate (each sweep is called a scan line). The vertical signal controls the positioning of the beam to a new scan line for vertical positioning.

9.3 MONOCHROME MONITOR SYSTEM COMMUNICATION

The monochrome monitor connects with both the system unit and the keyboard. The system unit connects to the monitor via J1, a 15-pin D-type subminiature connector. The keyboard connects via J3, a modular telephone-type jack.

J1 has three basic functions: the supply of video input used only at the monitor, the supply of operational voltages used by both the monitor and the keyboard, and the transfer of keyboard data (Figure 9-4). The operational voltage and keyboard data lines are hardwired from J1 to J3 on the monitor module.

Table 9-1 provides a pin-out for J1 with signal identifications and functional descriptions. Table 9-2 provides the same information for J3.

Table 9-1 J1 Pin-out

Pin(s)	Signal	Description
1–3	(Not used)	None
4	Ground	Video signal ground potential
5, 6	Ground	Operational voltage ground potential
7, 8	+12 Vdc	Operational voltage input
9–11	(Not used)	None
12	M Video	Composite video (refer to Paragraph 9.4)
13	Ground	Tied to pins 5 and 6
14	Data Receive	Serial data line from the keyboard output to the system unit (via J3)
15	Data Send	Serial data line from the system unit output to the keyboard (via J3)

Table 9-2 J3 Pin-out

Pin	Signal	Description
1	Data Send	Serial data line for output from the system unit to the keyboard (via J1, pin 15)
2	+12 Vdc	Output of operational voltage to the keyboard (from J1, pins 7 and 8)
3	Ground	Operational voltage ground potential (from J1, pins 5, 6, and 13)
4	Data Receive	Serial data line for input from the keyboard to the system unit (via J1, pin 14)

9.4 COMPOSITE VIDEO SIGNAL

The video input to the monitor is a composite of two types of signals: video and sync. There are different levels of illumination within the video signal, ranging from totally black through maximum brightness.

Figure 9-5 represents a typical composite video signal and identifies the major terms associated with it. This signal, used with the monochrome monitor, is compatible with EIA RS-170 standards. However, it is dc coupled to ground at the monitor module. Table 9-3 provides typical signal values.

Figure 9-6 shows the composite video signal and the sync portion of this signal. Table 9-4 describes the values for the sync components identified.

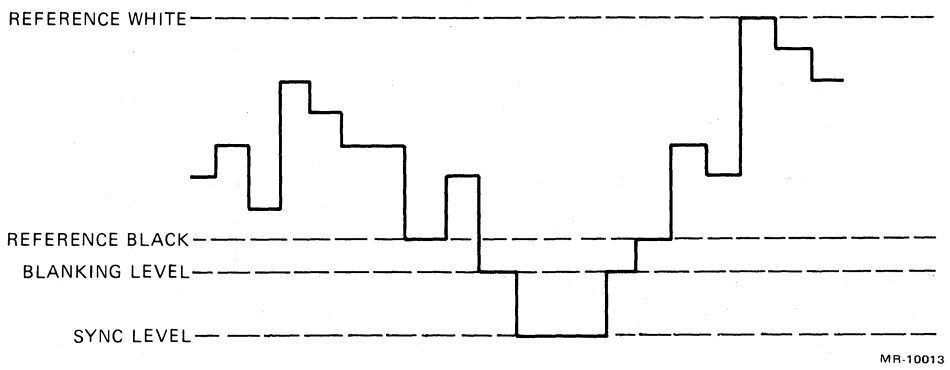


Figure 9-5 Composite Video Signal Representation

Table 9-3 Composite Video Values

Characteristics	Value
Output impedance	75 Ohms, dc coupled to 0.0 V.
Amplitude	1.0 V peak-to-peak nominal (The monitor accepts signals with peak-to-peak values of 0.9 V through 1.5 V.)
Reference black	The low limit of display value. It equals 30% of the peak-to-peak value (0.3 V nominal), and is the lowest voltage value to be amplified linearly at the monitor module.
Reference white	The high limit of display value. It equals 100% of the peak-to-peak value (1.0 V nominal), and is the highest voltage value to be amplified linearly at the monitor module.
Blanking level	Voltage value which reduces CRT electron beam current below cutoff.
Sync level	Voltage level at which sync actions can take place; 0.0 V nominal (dc coupled video to ground).
Continuous input	+2.0 V maximum (2.0 V saturates the video amplifier unless the contrast thumbwheel adjustment is reduced).

9.5 CRT

The CRT provides the final video output—an electron beam fired at a phosphor-coated faceplate.

The electron beam generation is controlled directly by the monitor module inputs. The module controls the yoke, which in turn controls positioning the beam at the faceplate.

The CRT contains an electron gun. The gun consists of the heater element, a cathode, three grids (G1, G2, and G4), an anode, and the faceplate, all encased in a vacuum.

The three grids control the beam generated by the gun: G1 for brightness, G2 for beam cutoff, and G4 for focus.

G1 is directly affected by the brightness control thumbwheel. This enables the operator to adjust the background intensity of the display. G2 provides sharpening capabilities of the video. To do this, G2 acts as a gate or valve to the electron beam. A voltage, provided to G2, prevents the electron beam from passing to the faceplate unless the beam is of a specific minimum intensity. G4 focuses the electron beam.

The CRT plugs directly into P1, which is hardwired onto the module. Through P1, the operational voltages for the heater element, the cathode, and the three grids are provided. The anode voltage is provided by a separate connection between the module and the CRT. Its ground goes to the CRT case. This ground reduces shock hazard and consists of three parts: a connection between the module and a terminal block on the yoke, a connection between the block and the CRT case, and a connection between the block and P1.

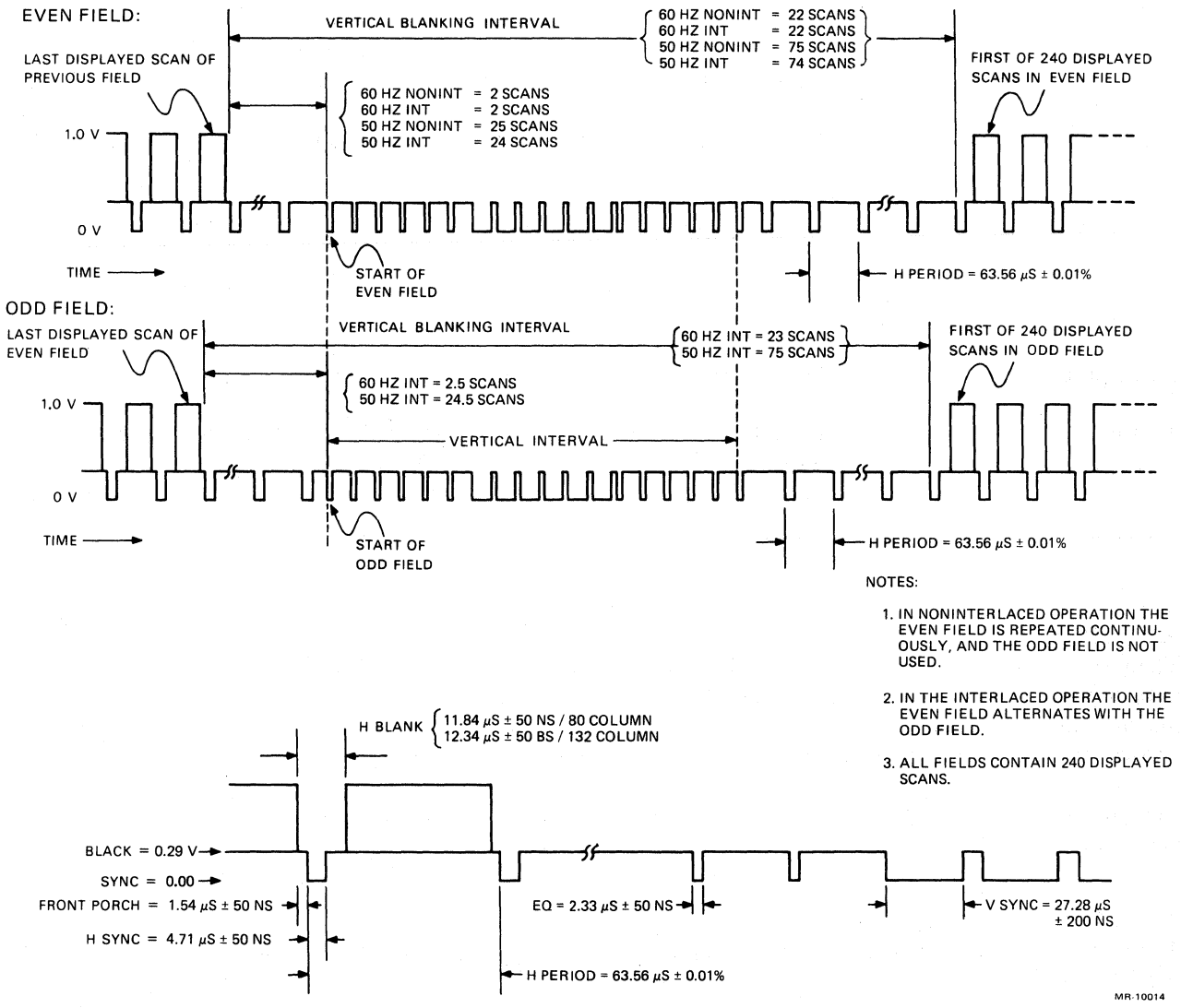


Figure 9-6 Composite Video Sync Timing Diagram

Table 9-4 Composite Video Sync Component

Component	Description
Vertical blanking interval	Period of time screen is blanked for vertical retrace activity. Vertical retrace is completed in less than 1.0 ms, and within an allowed frequency range of 49 to 61 times per second.
V Sync	Period of time in which vertical deflection circuitry on the monitor module is synchronized to the next frame.
H Sync	Period of time in which horizontal deflection circuitry on the monitor module is synchronized for retrace.
H Period	Period of time for the horizontal scan plus horizontal blanking (63.5 μs)
EQ	Equalizer pulse that synchronizes vertical deflection circuitry on the monitor module for vertical retrace activity.
Front porch	Delay value between start of blanking and start of sync pulse.
Vertical interval	Period of time the actual synchronizing of the vertical deflection circuitry on the monitor module takes place. Consists of six EQ pulses, six V sync pulses, and six more EQ pulses.

9.6 YOKE

The yoke is a set of electromagnetic devices mounted on the neck of the CRT. One device is for horizontal deflection of the electron beam, the other is for vertical deflection. Currents to control the horizontal scan line are applied to the yoke's coil (inductance) through the width inductor and the linearity inductor. The vertical trace control current comes from the vertical processor chip.

The yoke connects to the monitor module through J2: pins 2 and 3 for the horizontal deflection magnetic coils, pins 1 and 4 for the vertical.

9.7 MONITOR MODULE

The monitor module is made of discrete analog components. It can be divided into seven circuits to control the CRT and yoke.

Figure 9-7 is a block diagram of the module showing the seven circuits. The figure also identifies the fuse for the power input (F1), and three connectors (a fourth connector, J3, which routes signals between J1 and the keyboard, is not shown). Descriptions of each of the items identified in Figure 9-7 are provided in the following paragraphs.

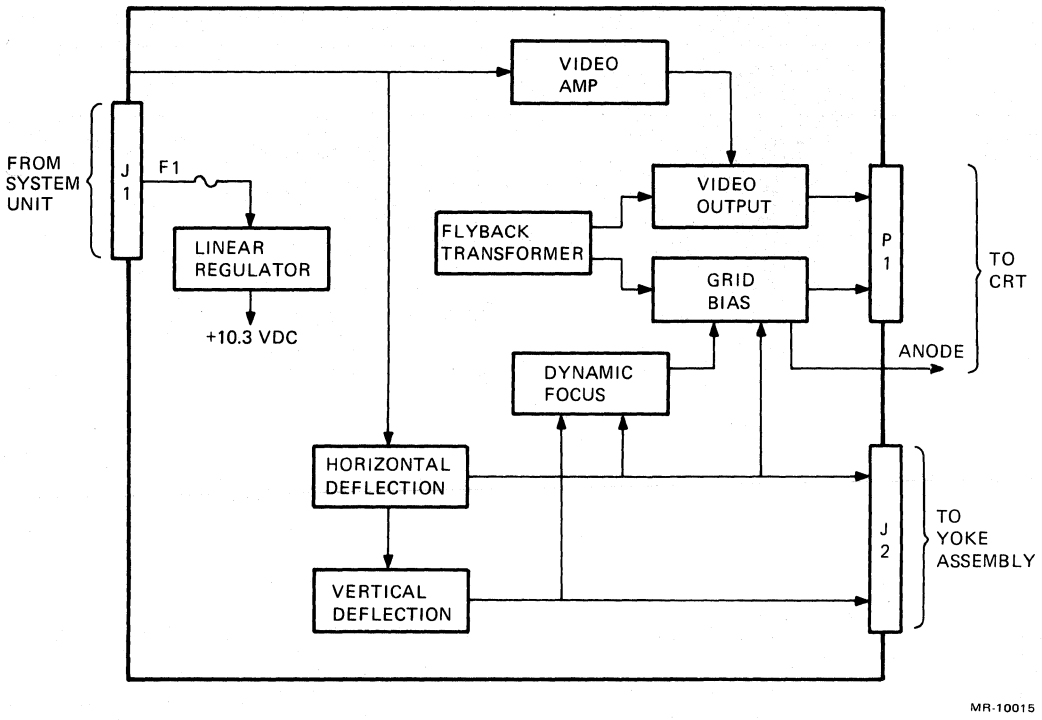


Figure 9-7 Monitor Module Block Diagram

9.7.1 Dynamic Focus

This circuit creates different focus voltages for different areas of the screen. Output from this circuit is tied to focus biasing circuitry within the grid bias circuit. This output offsets focus biasing based on horizontal and vertical deflection values. The circuit is primarily a single transistor that acts as a mixer for parabolic inputs from the horizontal and vertical deflection circuits. This changes focus biasing as a function of the position of the beam on the tube.

9.7.2 Grid Bias

This circuit generates CRT biasing values: focus (G4), cutoff (G2), and brightness (G1). These voltages are developed from the flyback transformer and are routed to the G4 and G2 circuits. There are resistor networks, each containing potentiometers for adjusting the bias in question, R43 for G4 (focus), or R120 for G2 (cutoff). The remaining bias circuit, G1 (brightness), is a resistor network between two voltage sources, +40 Vdc and −150 Vdc. This adjustment allows the operator to adjust the display background intensity. The voltage on G1 is adjustable from approximately 0 to −47 Vdc.

9.7.3 Horizontal Deflection

This circuit drives the CRT beam across the faceplate horizontally. This circuit contains the following elements:

- A horizontal processor
- A sync buffer circuit
- A horizontal driver and output
- RC networks that bias circuits within the horizontal processor

- A horizontal deflection generator output stage (width and linearity inductors, horizontal output transistor, damper diode, retrace capacitor, and yoke inductor)

An oscillator within the horizontal processor allows the horizontal deflection circuit to free run. The sync pulses then synchronize the operating running rate to the video input.

The sync buffer circuit amplifies the sync pulse and then applies it to the horizontal processor. When the horizontal output turns off, the electron beam flies back, returning the beam to the left of the screen. At the end of retrace, the conducting of the damper diode establishes a ramp of current in the yoke inductor. To make sure the output transistor is turned on at the proper time, the horizontal deflection IC also provides the correct timing on its output pulse. This allows the current ramp to continue after the damper diode stops conducting. The width coil portion of the output stage adjusts the width of the display. Two of the RC networks contain potentiometers for adjusting their biasing values: R211 for hold (horizontal), and R218 for centering (phase).

A secondary output from the generator is provided to the vertical deflection circuitry as a vertical sync signal.

9.7.4 Linear Regulator

This circuit provides power to the flyback transformer during initial power-up and also regulates the input voltage. During initial power-up, the +12 Vdc voltage is applied to the regulator. The voltage input (rising from 0 V to +12 Vdc) is shunted through a series of 4 diodes and then through the flyback transformer. This generates 40 Vdc at the input of L300 to the regulator field effect transistor sources (FETS). The FETS are then turned on and conduct the load current instead of the diodes. A precision zener diode plus the regulator transistor's V_{BE} cause the circuit to provide 10.3 Vdc regulated output.

9.7.5 Vertical Deflection

This circuit positions the CRT beam across the faceplate vertically. This circuit contains the following elements:

- A vertical processor
- Various RC networks responsible for biasing of circuits internal to the vertical processor
- An output filter network.

An oscillator within the vertical processor allows the vertical deflection circuit to free run. The sync pulses synchronize the vertical deflection to prevent vertical roll.

Three of the RC networks contain potentiometers for adjusting biasing values: R48 for hold (vertical), R50 for height, and R53 for linearity. At the beginning of each refresh cycle, the vertical processor receives a vertical sync pulse from the horizontal processor circuit. The horizontal processor detects the vertical sync pulse and sends it to the vertical processor. This sync pulse comes from the composite video input to the monitor module. The vertical sync pulse causes the beam to fly back vertically and begin a new frame.

9.7.6 Video Amplifier

The video amplifier consists of an input and output stage. The video signal is applied to an input push/pull transistor network that is part of an encapsulated transistor array. The input is provided from R5, the contrast thumbwheel potentiometer. The potentiometer is adjustable by the operator for personal contrast preference. The potentiometer, R119, provides a preamplifier adjustment to preset the range that can be affected by the contrast thumbwheel. Biasing of the input stage affects the biasing of the output stage, which is another transistor network. The more positive the input to the input stage, the more positive the output from the transistor network. This output is provided to the video output stage.

The video output stage provides the operational voltage for the CRT beam. The video output stage uses the voltage from the flyback transformer (40 Vdc) to generate its output. The sync pulses (horizontal and vertical) set the video output to or below the cutoff voltage so the operator does not see the retrace lines. Applying increased positive video amp signal decreases the output to the CRT. This also increases the intensity of the CRT display.

9.7.7 Flyback Transformer

The flyback transformer is the high voltage power supply and is synchronized to the horizontal deflection. It generates the voltages used by the grid bias circuit (G1, G2, G4), the anode voltage (12.5 kV nominal), and the 40 Vdc voltage used by the linear regulator and video amplifier.

WARNING

The monochrome monitor contains shock hazard voltages. Use extreme caution when servicing the monitor.

There is a high voltage (12 kV nominal) on the anode lead and the anode cup on the side of the CRT.

To avoid shock, use the following procedure when discharging the anode:

1. **Turn off system power and connect the monitor cable.**
2. **Attach the clip lead of the anode discharge tool to the metal frame.**
3. **Hold the tool by its insulated handle. Using one hand, carefully slide the tip of the tool under the plastic anode cap until it touches the anode. Avoid scratching or poking the glass CRT envelope.**
4. **Once the anode is discharged, remove the tool and clip lead.**

There are also 700 Vdc on the monitor module near the flyback transformer. Use caution when performing adjustments in this area. This area is covered with a protective shield.

CAUTION

Before removing the system module monitor cable, turn off the system power. Static discharge in the CRT can damage the monitor module and/or keyboard electronics.

Be sure the system power is off before connecting or disconnecting the monitor's cable for service or to move the monitor. When performing adjustments, secure the monitor's cable to the monitor with its thumbscrews so the cable does not loosen.

Failure to follow this procedure can damage monitor and/or keyboard components.

9.7.8 J1

This connector provides the voltage and video signals to the monitor module. Refer to Paragraph 9.3 for the pin-out and signal descriptions for J1.

9.7.9 J2

This connector provides the horizontal and vertical deflection currents between the monitor module and the yoke assembly. It is a 4-pin connector. Pins 1 and 4 are used for vertical deflection, pins 2 and 3 for horizontal deflection.

9.7.10 P1

This connector mounts on the monitor module the CRT plugs into. Figure 9-8 shows the pin-out for P1.

9.8 SPECIFICATIONS

Height	24.38 cm (9.75 in)
Width	29.33 cm (11.73 in)
Depth	30.57 cm (12.23 in)
Weight	6.6 kg (14.5 lb)

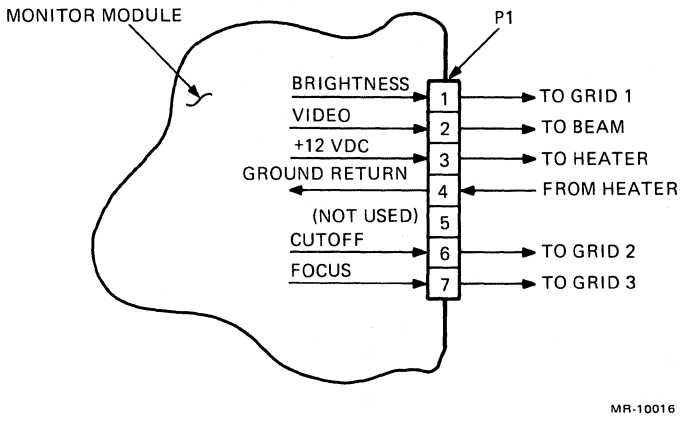


Figure 9-8 Monitor Module P1 Pin-out

CHAPTER 10
TESTING AND TROUBLESHOOTING

10.1 INTRODUCTION

This chapter describes the procedures for testing and troubleshooting the Rainbow 100 computer. Fault detection is limited to the lowest field replaceable units (FRUs) listed below:

1. System module (motherboard)
2. Memory extension option
3. ROM 0
4. ROM 1
5. ROM 2
6. Power supply
7. RX50 diskette drive
8. RX50 controller
9. Monitor
10. Monitor module
11. Keyboard
12. Fan
13. Power Switch

10.1.1 Fault Detection Strategy

The recommended fault detection strategy is to test the suspected FRU last in order to build up a confidence level in the FRUs that will be used to test the suspected FRU.

10.1.2 Fatal vs. Nonfatal Errors

The terms "fatal" and "nonfatal" with respect to faults or errors refer to the usability of the system. For example, if the system has two diskette drives and they are both out of operation, this is not fatal because the computer can still be used in the terminal mode of operation. However, if the keyboard is out of operation, this is fatal because the entire system depends upon the keyboard.

10.1.3 Categories of Testing

The Rainbow 100 computer contains ROM-based diagnostics and diskette-based diagnostics. The ROM-based diagnostics consist of selftests that automatically run during power-up and reset, and extended selftests that run by pressing the **S** key when the Main System Menu is displayed on the screen. The diskette-based diagnostics consist of tests that are menu selectable for use during maintenance and troubleshooting.

NOTE

There are two versions of the diskette-based diagnostics, version 1 and version 2. Although the screens differ slightly, they are compatible with all Rainbow computers.

If the computer-based diagnostics cannot be run, the field service engineer must determine the kind of testing that is required. For example, if the monitor does not display anything, it is up to the field service engineer to determine if power is lost to the system or just to the monitor, and whether to replace the monitor, a cable, the power supply, etc. Primarily, this category of testing by field service engineers isolates fatal errors, while the computer-based diagnostics are used to isolate additional fatal errors, as well as nonfatal errors.

10.2 ROM-BASED DIAGNOSTICS

10.2.1 Automatic Selftests

The automatic selftests are run during power-up and reset. These tests check the internal logic of the system. The error messages that can appear on the screen during the automatic selftests are listed in Appendix B.

Upon successful completion of the automatic selftests, the Main System Menu is displayed on the screen. If the test is unsuccessful and the error is nonfatal, an error message is displayed above the Main System Menu (refer to Figure 10-1). If the error is fatal, only the error message is displayed (Figure 10-2).

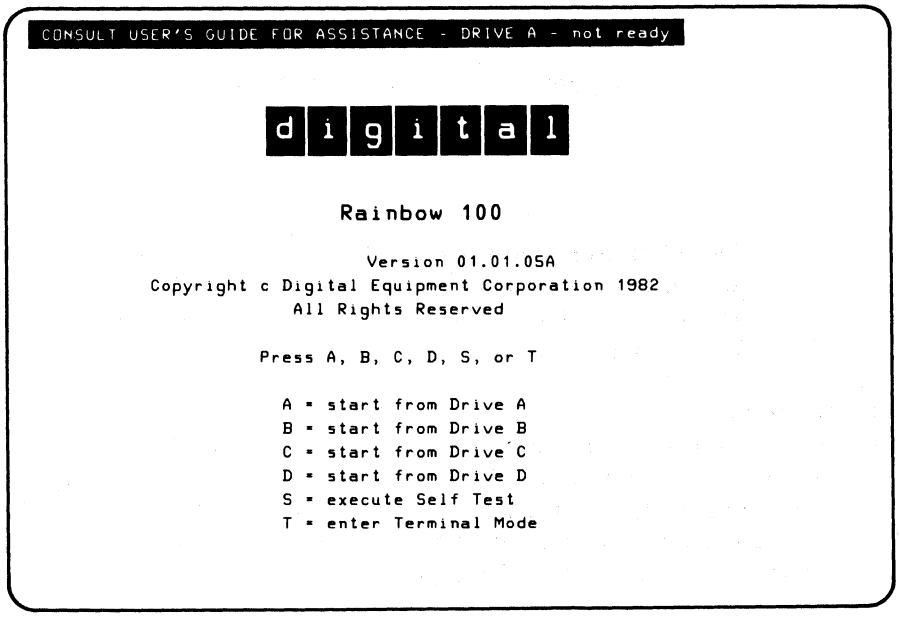


Figure 10-1 Main System Menu with Nonfatal Error Message

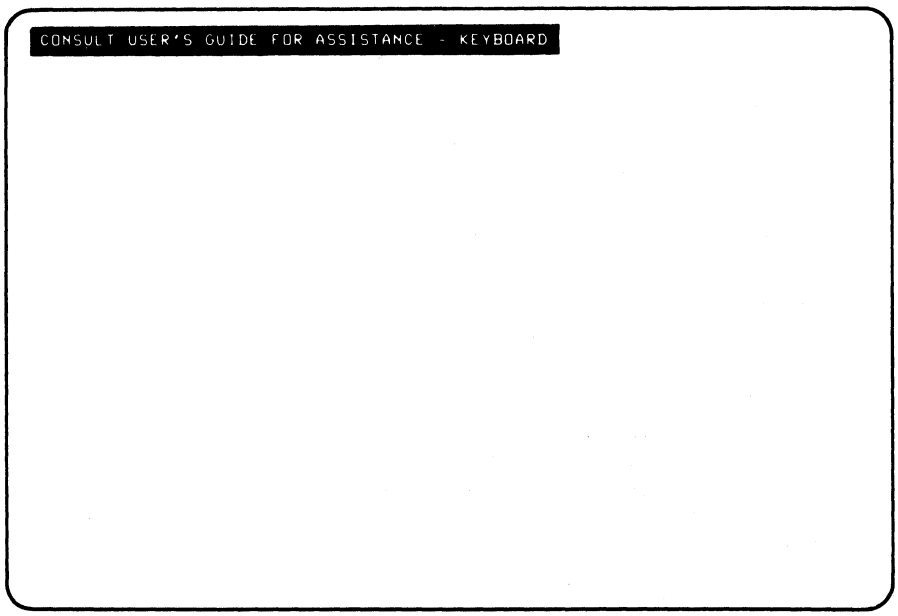


Figure 10-2 Fatal Error Message

NOTE
The LED display at the rear of the system unit also provides an indication of faults. See the *Rainbow*™ *100 Owner's Manual* for an interpretation of the LED display.

10.2.2 Extended Selftests

The extended selftests are run when the Main System Menu is displayed and the S key is pressed. The extended selftests exercise extensively more of the system than the automatic selftests and, therefore, require more time (approximately 90 seconds for 64K of memory and approximately 2 minutes for 256 K of memory). In order to complete all of the extended selftests, drive A must contain a diskette. (Drive B does not have to contain a diskette, but if it does, it will also be tested.)

Perform the extended selftests as follows:

1. Set the power switch to 1 (on).
2. Place a diskette in drive A and close drive A door.
3. When the Main System Menu is displayed, press the S key.
4. Refer to Appendix B for a description of the error messages that can be displayed during the extended selftests.

10.3 DISKETTE-BASED DIAGNOSTICS

The diskette-based diagnostics are used to detect faults that cannot be found by the ROM-based diagnostics.

NOTE

The diagnostic diskette referred to in this section is the one provided with the system, not the diagnostic diskettes that are provided when purchasing an option. Paragraph 10.3.5 describes how to copy the option diagnostics onto the main diagnostic diskette. This procedure also updates the diagnostics menu to include the option that is being added.

10.3.1 Running the Diskette Diagnostics

1. After the system is powered up, insert the diagnostic diskette in any drive and then close the drive door.

2. Press the **A**, **B**, **C**, or **D** key to select the drive that contains the diagnostic diskette.

3. When the Main Diagnostic Menu (Figure 10-3) is displayed, selections can be made as follows:

   a. Typing **1** and then pressing the **Return** key tests drives A and B, and requires blank Rainbow-formatted diskettes.

   b. Typing **2** and then pressing the **Return** key tests the entire computer including drives A and B, and also requires blank or scratch Rainbow-formatted diskettes.

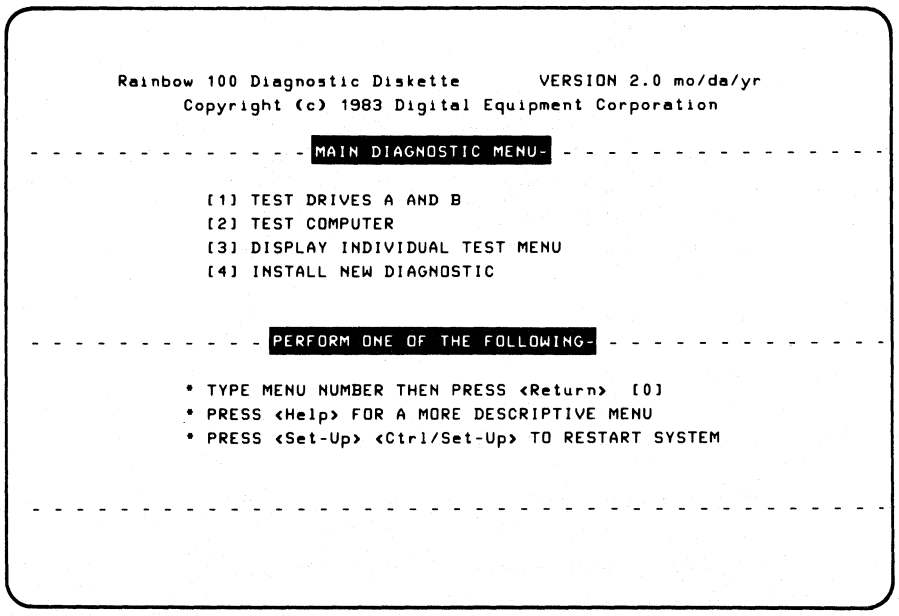


Figure 10-3 Main Diagnostic Menu

c. Typing **3** and then pressing the **Return** key displays the Individual Test Menu (refer to Figure 10-4). Each test can be run individually by typing the test number followed by pressing the **Return** key.

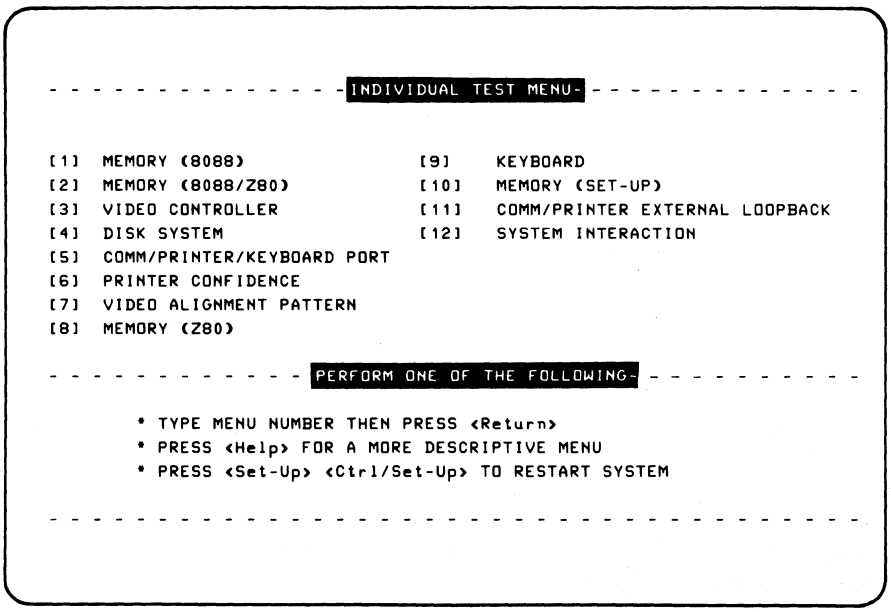


Figure 10-4 Individual Test Menu

d. Typing **4** and then pressing the **Return** key causes the following message to be displayed:

INSERT OPTION DISK IN DRIVE B - THEN PRESS <Return>:

This message requests the diagnostic diskette for an option, such as extended memory, to be inserted in drive B so it can be copied onto the main diagnostic diskette in drive A.

e. Pressing the **HELP** key displays a wordier Main System Menu.

f. Pressing the **Set-Up** key and then pressing the **Ctrl** and **Set-Up** keys simultaneously restarts the system.

The following paragraphs describe the tests selected from the Main Diagnostic Menu:

10.3.2 Main Diagnostic Menu Selection 1

NOTE
These tests require two blank or scratch Rainbow-formatted diskettes.

Selection 1 tests drives A and B. If the system includes drives C and D, these may be tested by performing the individual tests described in Paragraph 10.3.4.

Table 10-1 Time to Complete Diagnostic Tests

Main Tests		Approximate Time to Complete (min)
1.	Test drives A and B	2.0
2.	Test computer	24.0
3.	Display Individual Test Menu (See Individual Tests below)	
4.	Install new diagnostic	2.0
Individual Tests (Item 3)		
1.	Memory (8088 processor) (not including options)	3.0
2.	Memory (8088/Z80A processors)	1.0
3.	Video controller	2.0
4.	Diskette system	3.0
5.	Comm/printer/keyboard port	4.0
6.	Printer confidence	0.5
7.	Video alignment pattern	0.5
8.	Memory (Z80A)	0.5
9.	Keyboard	2.0
10.	Memory (Set-Up)	0.5
11.	Comm/printer external loopback	25.0
12.	System interaction	2.0
13.	*	
14.	*	
15.	*	
16.	*	

*Test 13 is not used. Tests 14, 15, and 16 are reserved for options.

10.3.3 Main Diagnostic Menu Selection 2

Selection 2 tests the entire computer and takes up a considerable amount of time. The tests that are performed and the time it takes to run each test are listed in Table 10-1.

10.3.4 Main Diagnostic Menu Selection 3

Selection 3 displays the Individual Test Menu as shown in Figure 10-4. Each test is selected and run individually.

10.3.5 Main Diagnostic Menu Selection 4

Selection 4 is used to copy an option diagnostic diskette onto the main diagnostic diskette so that the diagnostic tests for the entire system, including the options, are contained on one diskette. Selection 4 also updates the Individual Test Menu to include the option diagnostics.

To copy an option diagnostic diskette onto the main diagnostic diskette and to update the main diagnostic diskette menu, perform the following procedure:

1. Place power switch to the 1 (on) position.
2. Insert the main diagnostic diskette in drive A.
3. Press the **A** key on the keyboard.
4. Press the **4** key and the **Return** key.
5. Insert the option diagnostic diskette in drive B.
6. Press the **Return** key.

After a few seconds the system will copy the option diagnostic diskette onto the main diagnostic diskette, and then include the option diagnostic tests in the Individual Test menu.

10.4 TROUBLESHOOTING

The recommended procedure for troubleshooting the Rainbow 100 computer is listed in Table 10-2.

NOTE

For each symptom in Table 10-2, there may be several causes. The most likely causes associated with a symptom are listed first, followed by the causes that are less likely. Refer to Chapter 11 for FRU removal and replacement procedures.

Table 10-2 Troubleshooting Guide

Problem	Possible Causes
Fan does not operate with power turned on.	No ac at wall outlet.
	Internal connectors from fan to switch are not properly seated.
	Bad power switch.
	Defective fan.
	Defective power supply.
Fan operates, blank screen.	Intensity control is set too low.
	Video connector not seated properly.
	Defective system module.
	Defective monitor.
Printer prints garbage or nothing.	Printer baud rate selected in Set-Up not the same as printer's baud rate. See the *Rainbow™ 100 Owner's Manual.*

Table 10-2 Troubleshooting Guide (Cont)

Problem	Possible Causes
Screen displays garbage.	Modem baud rate selected in Set-Up not correct. See the *Rainbow™ 100 Owner's Manual.*
	Run Individual Test 11.
	Language ROM improperly installed or defective.
Screen flickers or rolls.	Parameter setting for power in Set-Up not set correctly, should be set to 60 Hz in any country.
Screen displays everything except what is typed on the keyboard when in the computer mode.	Keyboard defective.
	Language translation ROM defective.
Screen displays garbage or nothing when in the terminal mode.	Modem baud rate in Set-Up not correct. See the *Rainbow™ 100 Owner's Manual.*
	Run Individual Test 11.
Diskette drive will not load any programs.	Dirty or scratched diskette.
	Programs on diskettes are not in a format recognized by the Rainbow 100 computer operating system.
	Defective or improperly seated cables between the drives and the power supply.
	Defective RX50 controller.
	Defective RX50 diskette drive.
	Defective system module.

CHAPTER 11
SERVICE INFORMATION

11.1 INTRODUCTION

This chapter provides service information for the Rainbow 100 computer. When appropriate, checking and adjustment procedures are described. However, the maintenance philosophy for the Rainbow computer is replacement of the field replaceable unit (FRU). Removal procedures are described for the following FRUs. To install the same FRU, perform the removal steps in reverse order unless otherwise noted.

- Monitor
- Monitor module
- System module
- RX50 controller module
- Language ROM
- ROMs 0 and 1
- Diskette drive
- Power supply
- Fan bracket assembly

11.2 MONITOR

This paragraph provides service information for the VR201 black and white monitor, as well as specific adjustments if it is used with the color/graphics option. For service information for the VR241 color video monitor, refer to the *VR241 Color Video Monitor Pocket Service Guide* (EK-VR241-PS).

NOTE

If the monitor is to be stored or shipped, pack the monitor in its original shipping box.

11.2.1 Monitor Removal

Perform the following steps:

WARNING

For your safety, make sure the power is switched OFF at the system unit if you have a black and white video monitor.

1. Make sure the power switch on the system unit is set to 0 (off).
2. Unplug the power cable.
3. Unplug the monitor cable.
4. Unplug the keyboard cable.
5. The monitor is now free.

11.2.2 Monitor Module Removal

Perform the following steps:

WARNING

For your safety, make sure the power is switched off at the system unit.

1. Make sure the power switch on the system unit is set to 0 (off).
2. Unplug the power cable.
3. Unplug the monitor cable.
4. Unplug the keyboard cable.
5. Place some protective material over the screen to prevent scratches.
6. Place the monitor face down on a flat surface.
7. If the monitor is equipped with a tilt foot, extend it.

CAUTION

If the tilt foot is not fully extended, it will catch on the internal wires of the monitor when you remove the cover.

8. Remove the screw cap from the back of the monitor (Figure 11-1).

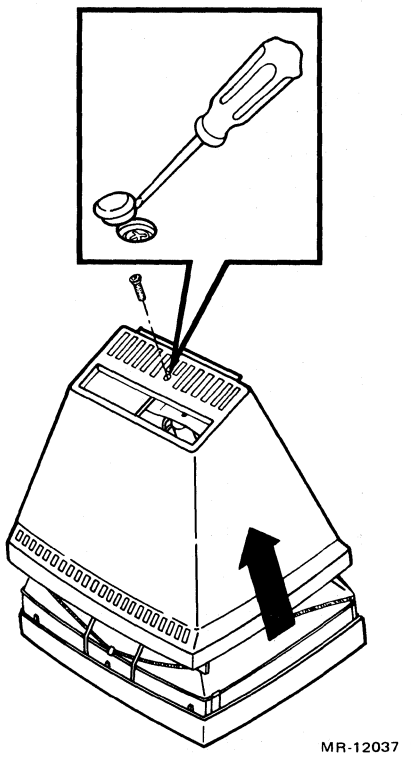


Figure 11-1 Monitor Cover Removal

9. Unscrew the cover retaining screw and remove it (Figure 11-1).

10. Slide the cover off and place it to one side.

WARNING

Before you remove the monitor module, you must, for your safety, turn the power OFF. The monitor holds a charge of over 12,000 V even with the power off. Therefore, use extreme care when changing the video monitor module, especially around the following high voltage parts (Figure 11-2):

- **Anode and anode wire**
- **Flyback transformer**
- **Connector at neck of CRT**

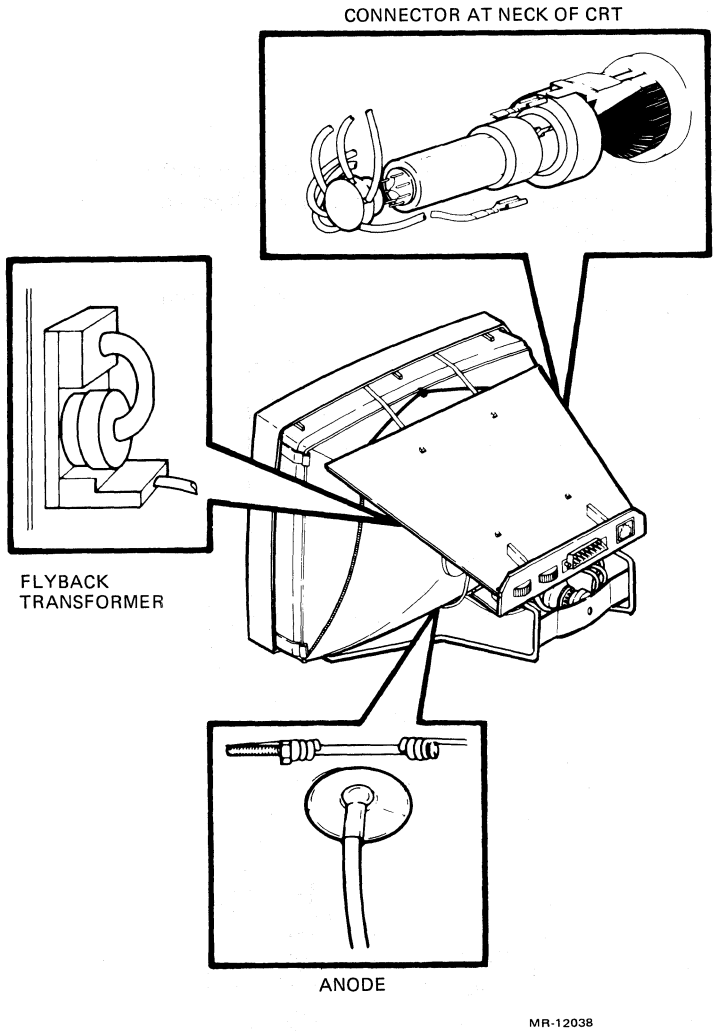


Figure 11-2 Sources of High Voltage

11. Discharge the anode connection of the CRT by performing the following steps:

NOTE

The high voltage at the anode will normally discharge by itself over a short period of time when the power is turned off. However, this discharge procedure is necessary in case there is a problem in the high voltage power supply on the monitor module that prevents it from discharging automatically.

WARNING

Perform step (a) before performing step (b) to prevent hazardous electrical shock.

a. Clip the anode discharge tool or a test probe to the wire frame of the monitor assembly, as shown in Figure 11-3.

WARNING

Do not scratch the glass of the CRT with the tip of the discharge tool. Scratches can weaken the glass and increase the danger of an implosion.

b. Slide the tip of the anode discharge tool or test probe under the rubber boot as shown in Figure 11-3. Hold for a *full 3 seconds*.

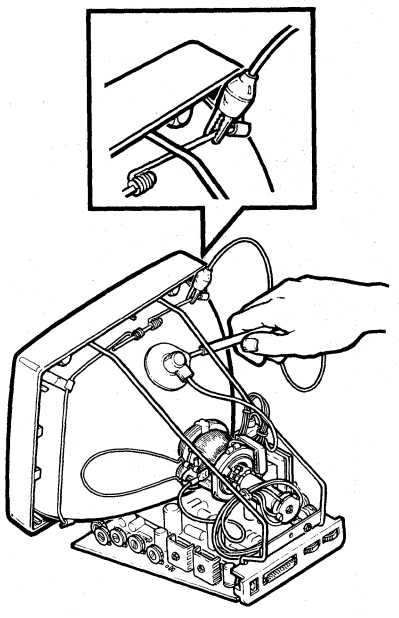


Figure 11-3 Discharging CRT Anode

12. Disconnect the anode wire from the CRT by pushing the anode further into its socket. Rock it from side to side and roll it out, as shown in Figure 11-4.

13. Unplug the connector from the neck of the CRT, as shown in Figure 11-5.

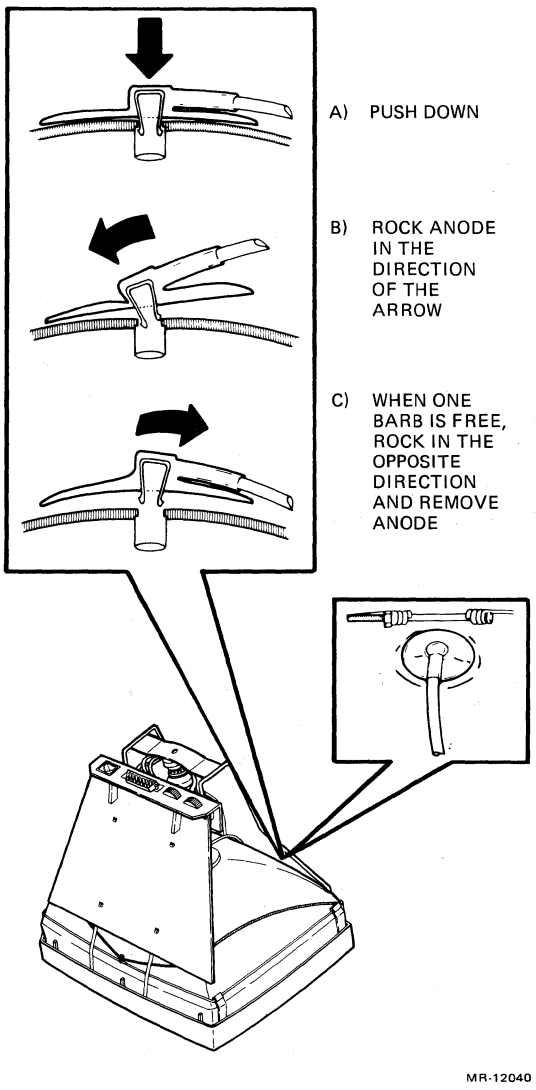


Figure 11-4 Anode Removal

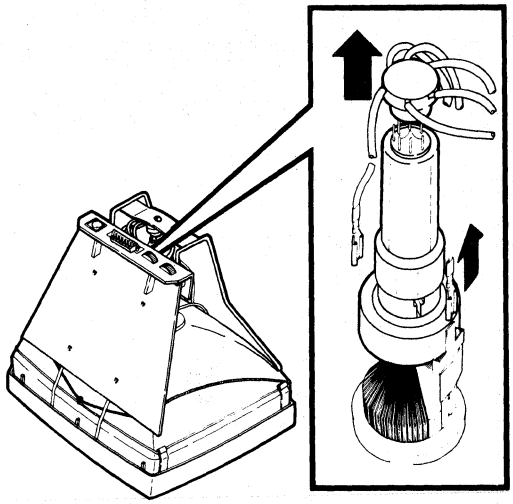


Figure 11-5 Removing CRT Connector

14. Unplug the associated white ground wire from the lug on the neck of the CRT. Also, remove the white ground wire from the chassis frame.

15. Remove the rear panel from the edge of the monitor module, as shown in Figure 11-6.

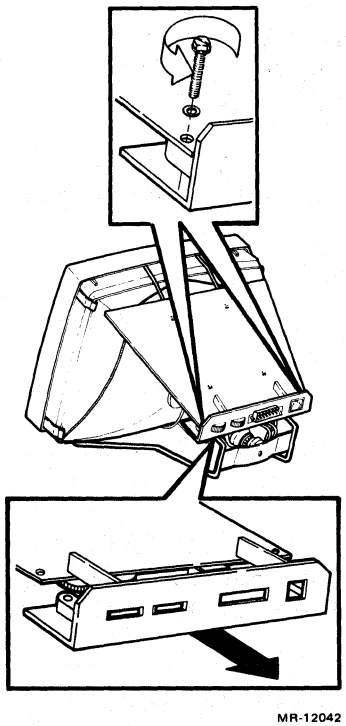


Figure 11-6 Monitor Module Rear Panel Removal

16. With needlenose pliers, release the standoffs holding the module, as shown in Figure 11-7. Do not worry if the standoffs break; the new module comes with new standoffs.

17. Remove the 4-wire connector from the center of the monitor module.

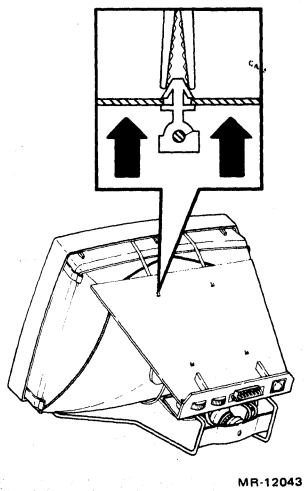


Figure 11-7 Monitor Module Standoff Removal

11.2.3 Monitor Adjustments

The series of checks and adjustments to be made to the monitor is described in Paragraph 11.2.3.2. However, before making any adjustments, you must follow the preparation procedure described in Paragraph 11.2.3.1.

WARNING
For your safety, turn the power OFF.

11.2.3.1 Preparation – Use the following procedure:

1. Unplug all of the cables from the back of the monitor.
2. Place some protective material over the screen to prevent scratches.
3. If the monitor is equipped with a tilt foot, extend it.

CAUTION
If the tilt foot is not fully extended, it will catch on the internal wires of the monitor when you remove the cover.

4. Place the monitor face down on a flat surface.
5. Remove the screw cap from the back of the monitor.

6. Unscrew the cover retaining screw and remove it.

7. Slide the cover off and place it to one side.

WARNING

The monitor holds a charge of over 12,000 V, even with the power off. Therefore, use extreme care when adjusting the monitor, especially around the following parts shown in Figure 11-2:

- **Anode and anode wire**
- **Flyback transformer**
- **Connector at neck of CRT**

8. Return the monitor to its normal operating position.

WARNING

Place the monitor on a nonconductive surface to avoid an electrical short.

9. Remove the protective material from the screen.

10. Reconnect all the cables to the back of the monitor, and set the power switch to 1 (on).

11. Load the Rainbow diagnostic diskette into one of the diskette drives, and select the Display Individual Test Menu from the Main Diagnostic Menu. If you have a color/graphics option installed, load the GSX-86 diskette and select the Graphics Option Hardware Diagnostic Test.

12. Select the video (or monitor) alignment pattern. The video alignment pattern fills the screen with Es. The graphics monitor alignment pattern creates a crosshatch pattern on the screen.

11.2.3.2 Checks and Adjustments – Make all adjustments under the following conditions:

- 80-column screen width (not 132 columns)
- Dark screen (white characters on a dark background)

The procedure for changing the Set-Up features is explained in Chapter 2.

Brightness and Contrast – Use the following procedure to adjust brightness and contrast:

1. Turn the brightness and contrast controls to the minimum setting.

2. Increase the brightness control until the raster appears; then, decrease it until the raster just disappears.

3. Set the contrast control for easy viewing.

Vertical Hold (VH) – Use the following procedure to adjust the vertical hold:

1. Examine the monitor display for rolling or any other sign of vertical instability.

2. If needed, adjust the vertical hold (VH) control (Figure 11-8) to stop any vertical movement.

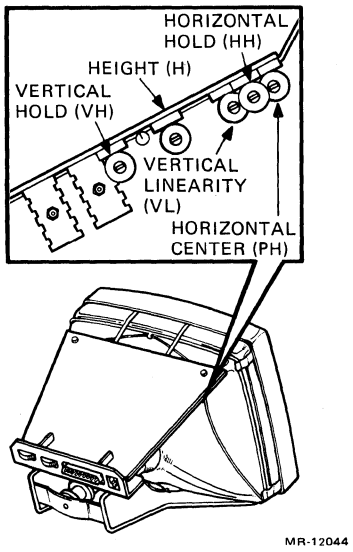


Figure 11-8 Monitor Module Controls – Left Side

Horizontal Hold (HH) – Use the following procedure to adjust the horizontal hold:

1. Examine the monitor display for tearing or any other sign of horizontal instability.
2. If needed, adjust the horizontal hold (HH) control (Figure 11-8) to stop any horizontal movement.

Focus – Use the following procedure to adjust the focus control:

1. Examine the pattern at the four corners and in the center of the screen. Each line should be sharp and well defined.
2. If the lines are not sharp and well defined, adjust the focus control (FOC), Figure 11-9, for the sharpest overall display.

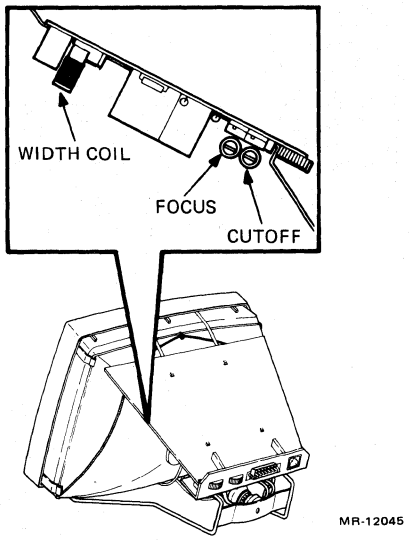


Figure 11-9 Monitor Module Controls – Right Side

Vertical Centering and Rotation Check Without Color/Graphics Option – Use the following procedure to check the vertical centering and rotation:

NOTE
If you have a color/graphics option, this adjustment is more critical, and you must use a video alignment template (29-24371). See next paragraph.

1. The screen of Es should be about 4 mm (3/16 in) below center. If the screen of Es is too high or too low, replace the entire monitor. Vertical centering is not adjustable.

2. If the screen of Es slants across the screen or curves or bows by more than 3 mm (1/8 in) at the top or bottom of the screen, replace the entire monitor. Rotation (slanting) and pincushion (bowing) are not adjustable.

Vertical Centering and Rotation Check for Color/Graphics Option – Use the following procedure to check the vertical centering and rotation:

NOTE
A video alignment template is required for the following checks.

1. Measure the distance in three places between the bottom edge of the alignment pattern and the monitor bezel (Figure 11-10). Use the scale on the template for the measurements. Make a note of each measurement.

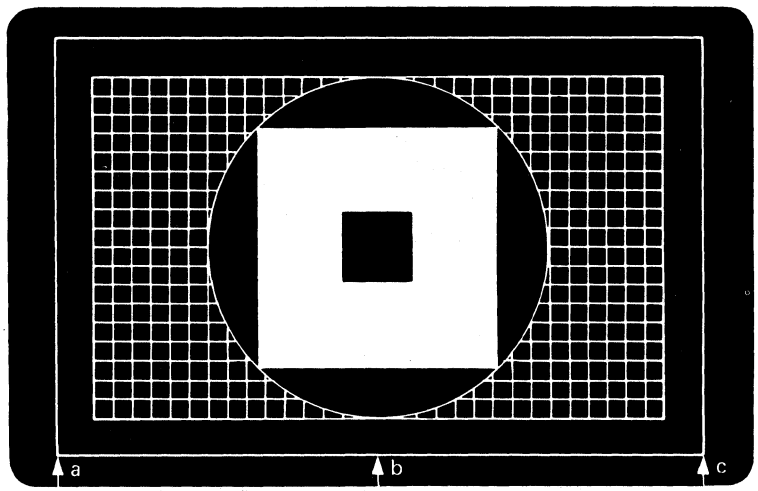


Figure 11-10 Vertical Centering and Rotation Check With Alignment Template

2. Compare all three measurements. The difference between the measurements should not be greater than ±2 mm. If the difference is greater, go to step 5.

3. Measure the distance between the top center edge of the alignment pattern and the monitor bezel. Use the scale on the template for the measurement.

4. Compare the measurements from steps 1 and 3. The top measurement should be larger by at least 1 mm but no more than 7 mm. If the difference is greater, go to step 5.

NOTE
The electrical center of the screen is not the same as the apparent physical center of the screen. When the monitor is adjusted correctly, the display will be offset towards the bottom of the screen.

5. If any of the measurements are out of tolerance, replace the monitor assembly.

NOTE
You cannot adjust vertical centering and rotation.

Horizontal Centering and Width Coil – These two adjustments can affect each other and may also affect the horizontal hold adjustment. Therefore, after adjusting either the horizontal centering control or the width coil, you may have to readjust the others slightly.

NOTE
If you have a color/graphics option, these adjustments are more critical, and you must use a video alignment template (29-24371).

1. Adjust the horizontal centering (PH) control (Figure 11-8) so that the screen of Es is centered side-to-side.

2. Adjust the width coil (Figure 11-9) for comfortable viewing.

3. Recheck the horizontal hold adjustment.

Height and Vertical Linearity – The height and vertical linearity controls can affect each other and may affect the vertical hold adjustment. After adjusting either the height or the vertical linearity controls, you may have to readjust the vertical hold slightly.

NOTE
If you have a color/graphics option, these adjustments are more critical, and you must use a video alignment template (29-24371).

1. Adjust the vertical linearity (VL) control (Figure 11-8) until there is no distortion in the screen of Es (the Es on the top of the screen are the same height as the Es on the bottom and at the center of the screen).

2. Adjust the height (H) control (Figure 11-8) for comfortable viewing.

Horizontal Centering for Color/Graphics Option – Use the following procedure to check the horizontal centering:

NOTE
A video alignment template is required for this adjustment (29-24371).

1. Measure the distance between the center left edge of the alignment pattern and the monitor bezel (Figure 11-11). Use the scale on the template for the measurement. Make a note of the measurement.

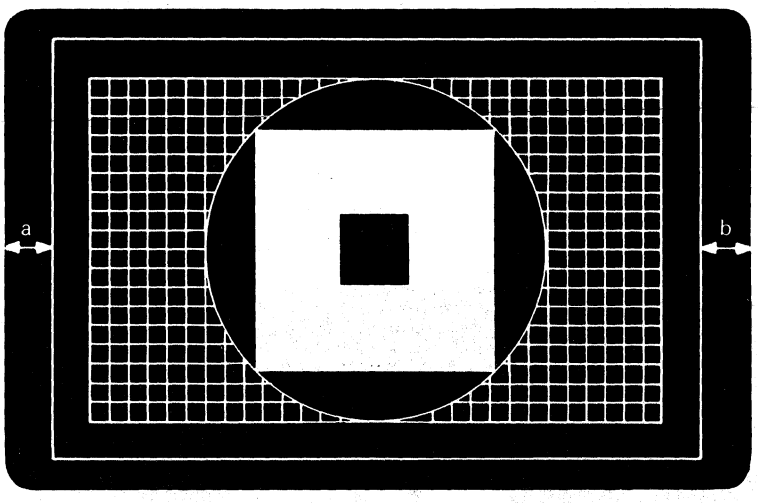


Figure 11-11 Horizontal Centering for Color/Graphics Option

2. Measure the distance between the center right edge of the alignment pattern and the monitor bezel. Use the scale of the template for the measurement. Make a note of the measurement.

3. Compare the measurements from steps 1 and 2. If the difference between the two measurements is greater than 6 mm, adjust the horizontal center (PH) control (Figure 11-8).

4. Repeat steps 1 and 2 to verify that the adjustment is less than 6 mm.

Cutoff – The cutoff control (Figure 11-9) sets the monitor's sensitivity to the video signal from the system module. It sets the video signal voltage needed to blank out a spot on the screen. This control is only changed when you install a new monitor module (see Paragraph 11.2.4).

Aspect Ratio (Horizontal Width and Height) for Color/Graphics Option – Use the following procedure to adjust the aspect ratio:

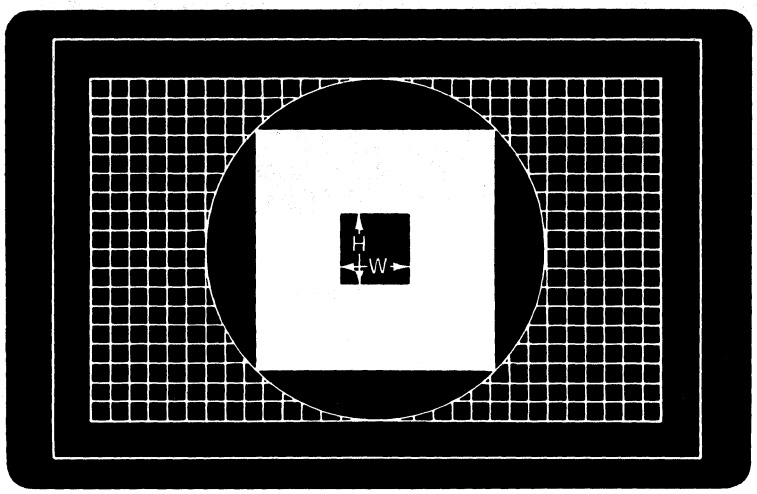
NOTE
A video alignment template is required for this adjustment (29-24371).

1. Place the alignment template over the center square of the alignment pattern.

2. Measure the height of the center square. This measurement should be 25 mm ± 2 mm (Figure 11-12). If not, adjust the Height (H) control (Figure 11-8) until the height is within this tolerance.

3. Measure the width of the center square. This measurement should be within 1 mm of the height measurement you set in step 2. If the width is not within this tolerance, adjust the width coil (Figure 11-9).

4. Check the horizontal centering and the vertical linearity.



H = 25 mm (±2 mm)
W = H (±1 mm)

MR-12333

Figure 11-12 Aspect Ratio

Vertical Linearity for Color/Graphics Option – Use the following procedure to adjust the vertical linearity:

NOTE
A video alignment template is required for this adjustment (29-24371).

1. Check the height of the crosshatch pattern near the four corners of the display. The pattern should have the same height in all four corners.

2. If not, adjust the vertical linearity (VL) control (Figure 11-8) until the pattern is the same height in all four corners.

3. Check the aspect ratio.

11.2.4 Monitor Module Replacement – When installing a new monitor module, you should perform the following steps:

WARNING
Discharge the anode wire of the new module by touching it to the white ground wire on the new module. The new module may contain a stored high voltage charge left over from manufacturing testing.

1. Place the old and the new monitor modules side-by-side with the cutoff controls (CO) at the same end.

2. Set the cutoff control on the new monitor module to match the setting on the old module (Figure 11-9).

3. Check the video monitor adjustments (see Paragraph 11.2.3).

4. Replace any broken standoffs.

5. Plug the connector (6 wires) into the center of the monitor module.

6. Connect one of the two white ground wires from the connector to the lug on the neck of the CRT.

7. Connect the other white ground wire from the connector to the chassis frame.

8. Install the monitor module on the standoffs.

9. Install the monitor module rear panel.

10. Reconnect the anode wire to the CRT.

WARNING
Use extreme care when performing the following steps, especially around the following high voltage parts shown in Figure 11-2.

- **Anode and anode wire**
- **Flyback transformer**
- **Connector at neck of CRT**

11. Before installing the cover, connect the keyboard cable and the monitor cable from the system unit.

12. Set the system unit power switch to 1 (on).

13. Boot the diagnostic diskette. Select the video alignment pattern from the Individual Test Menu. Run the Rainbow diagnostic diskette.

14. Look at the display, and adjust the monitor according to the procedures in Paragraph 11.2.3.

15. After adjustment, turn the power off and disconnect the cables to the keyboard and system unit. Then, install the monitor cover and reconnect the cables to the keyboard and system unit.

16. When you are finished, clean the monitor screen with a glass cleaning solution or isopropyl alcohol.

11.3 SYSTEM MODULE REMOVAL

Use the following procedure to remove the system module:

1. Remove any diskettes from the diskette drives.

2. If you have a floor stand, remove the system unit.

3. Set the power switch to 0 (off).

4. Unplug the power cord from the wall and from the back of the system unit. Unplug all cables from the system unit.

5. Make sure the diskette drive doors are closed. Pull the cover release tabs toward you and out until they lock in place. Lift the cover up.

6. Remove the power cable from the power supply first, then from the system module.

7. If diskette drive C/D is present, remove its cable from the connector. Leave the cable's ground clip attached to the ground lug on the chassis.

8. Using the pull tab, remove the signal cable for diskette drive A/B from the connector. Leave the cable's ground clip attached to the ground lug on the chassis.

9. With a coin, turn all the four screws at the back of the system unit once. Repeat until they are all loose. Slide the system module out of the system unit.

NOTE

If the system module is being replaced, remove and save all the options and insert them into the new system module.

11.4 RX50 CONTROLLER MODULE REMOVAL

Use the following procedure to remove the RX50 controller:

1. Remove the system module (Paragraph 11.3).

2. Press the top of the standoffs and connector clips away to loosen the RX50 controller module. Then lift the controller module off of the system module (Figure 11-13).

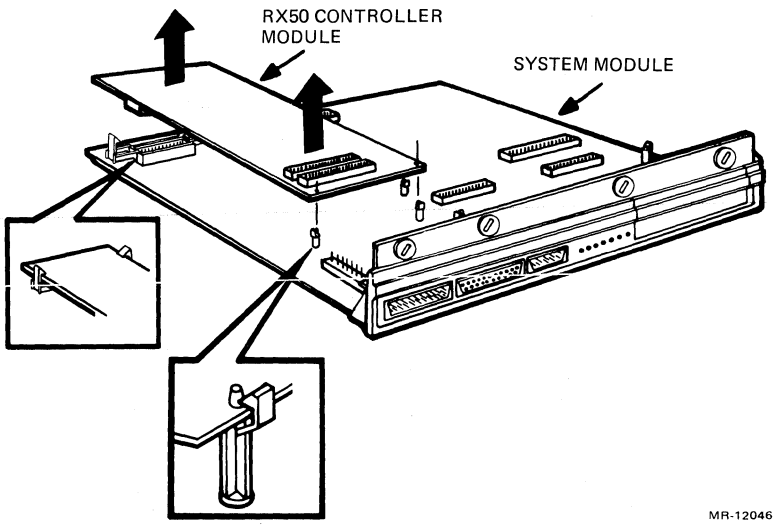


Figure 11-13 RX50 Controller Module Removal

11.5 LANGUAGE ROM

Use the following procedure to remove the language ROM:

1. Remove the system module (Paragraph 11.3).

2. Remove the extended communications option, if present, or any other option covering the ROM.

3. Pull up firmly on the ends of the language ROM and remove the ROM. Do not pry the ROM from only one end, or you may break its socket (Figure 11-14).

CAUTION

Avoid static: For example, do not walk across a carpeted floor while holding the ROM. Instead, place the old ROM in the box that contained the new ROM.

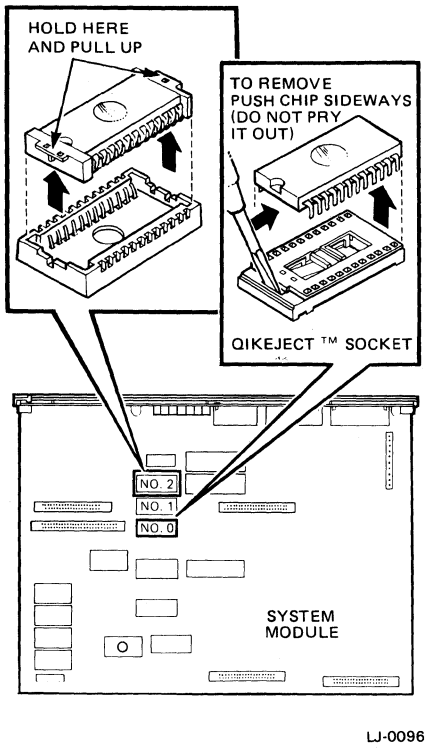


Figure 11-14 Language ROM Removal

11.6 ROMS 0 AND 1 REMOVAL AND REPLACEMENT

You should always replace ROMs 0 and 1 as a pair in the Rainbow 100 computer to ensure that the firmware programming in each has the same version number. Perform the following steps to replace these ROMs:

WARNING
For your safety, disconnect the power cord.

1. Remove the system module. (Refer to Paragraph 11.3.)
2. Remove the memory board, if present.
3. Remove the extended communications option board, if present.
4. Remove the hard disk controller, if present.

CAUTION
If your system module has a QIKEJECT™ chip socket, as shown in Figure 11-14, it will break if you pry the chip up out of the socket. Use a screwdriver to push the chip sideways instead.

QIKEJECT™ is a trademark of Burndy, Inc.

5. If your unit has the QIKEJECT socket, release each one of the two ROMs by using a tiny flat screwdriver to push the chip socket sideways, as shown in Figure 11-14. If your unit has another type of socket, examine the socket carefully to see how to remove the ROMs.

CAUTION
To avoid damaging the new ROM, do not pull the new chip out of its conductive foam pad.

6. Unpack the new ROM and gently press the foam against the surface of the system module to remove any static charge; then remove the ROM from the conductive foam.

7. Straighten any bent pins.

8. Align the new ROM so that the notch on one end is in the same direction as the notches of all of the other chips on the module.

9. Press the new ROM down into the socket. You will have to press firmly to insert the ROM.

10. Remove and replace the other ROM in the same manner.

11.7 DISKETTE DRIVE REMOVAL

Use the following procedure to remove the diskette drive(s):

1. Remove any diskettes from the diskette drives, then turn off the computer.

2. Perform the following procedure to set the diskette drive read mechanism at its starting position:

   a. Set the power switch to 1 (on).

   b. Wait for a beep sound from the keyboard.

   c. Set the power switch to 0 (off).

3. Insert the carriage restraint card in diskette drive A (and diskette drive C if present). (Be sure printing on card faces up.) Close the diskette drive doors.

4. Unplug the power cord from the wall and remove all cables from the back of the system unit. If the system unit is in a floor stand, remove the system unit.

5. Remove the top cover from the system unit.

6. Unplug the 4-wire power cable and the flat cable from the top of the diskette drive (Figure 11-15). Unplug the ground clip on the flat signal cable from the ground lug on the power supply.

7. With a pencil, press down on the latch in front of the diskette drive and slide the diskette drive forward and out of the system unit.

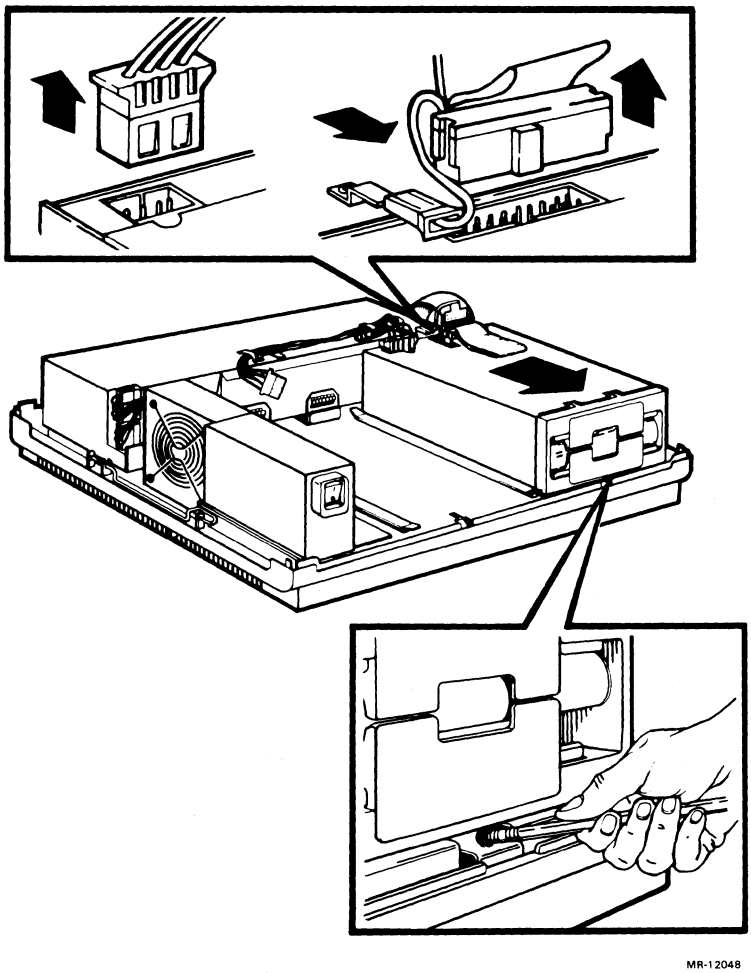


Figure 11-15 Diskette Drive 4-Wire Power Cable Removal

11.8 POWER SUPPLY REMOVAL

Use the following procedure to remove the power supply:

1. Remove any diskettes from the diskette drives and close the doors.
2. Set the power switch to 0 (off).

WARNING
For your safety, disconnect the power cord.

3. Unplug the power cord from the wall and from the back of the system unit. Unplug all cables from the system unit.
4. If you have a floor stand, remove the system unit.
5. Turn the system unit around and remove the top cover. Unplug the system module dc power cable from the power supply first, then from the system module.

6. Unplug the diskette drive flat cable(s) from the connector on the system module. Unplug the ground clip(s) from the ground lug(s).

7. Unplug the 4-wire power cable from the top of the diskette drive(s).

8. Unplug the ground clip on the flat signal cable for the diskette drive(s) from the ground lug(s) on the power supply. Leave the cable(s) attached to the diskette drive(s) (Figure 11-16).

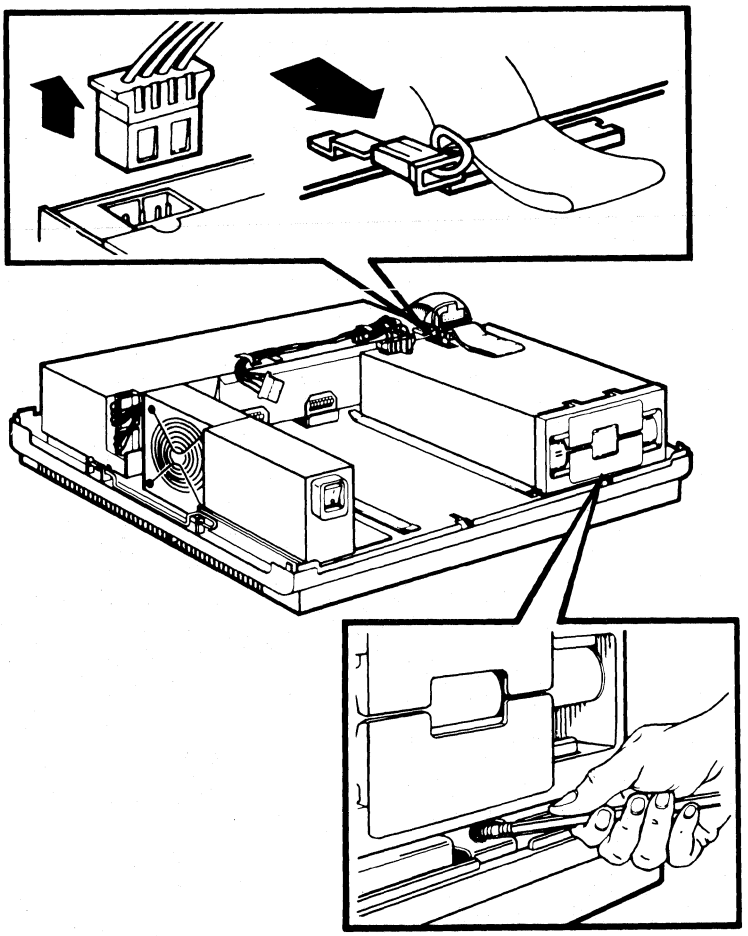


Figure 11-16 Slide Diskette Drive Forward

9. With a pencil, press down on the latch in front of the diskette drive(s) and slide them part way out of the system unit.

10. Squeeze the lock tabs at the ends of the plugs and pull them from the end of the power supply. The plugs are tight and may require being pulled in an up and down direction (Figure 11-17).

11. While pressing down on the power supply, release the latch, as shown in Figure 11-18. If the power supply is of the type with no side-mounted latch, press down on the power supply and slide the chassis-mounted latch toward the back of the system unit. Tilt the power supply up and remove the power supply, being careful not to damage the flat cables.

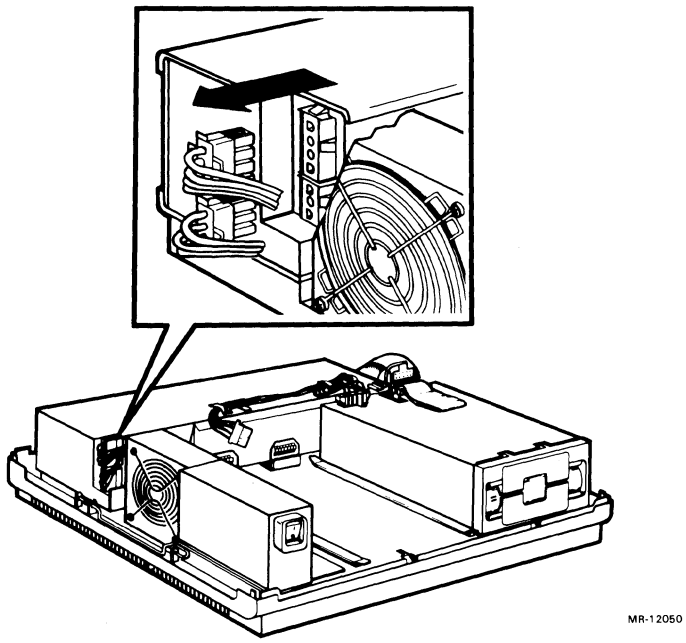


Figure 11-17 Power Supply Connectors

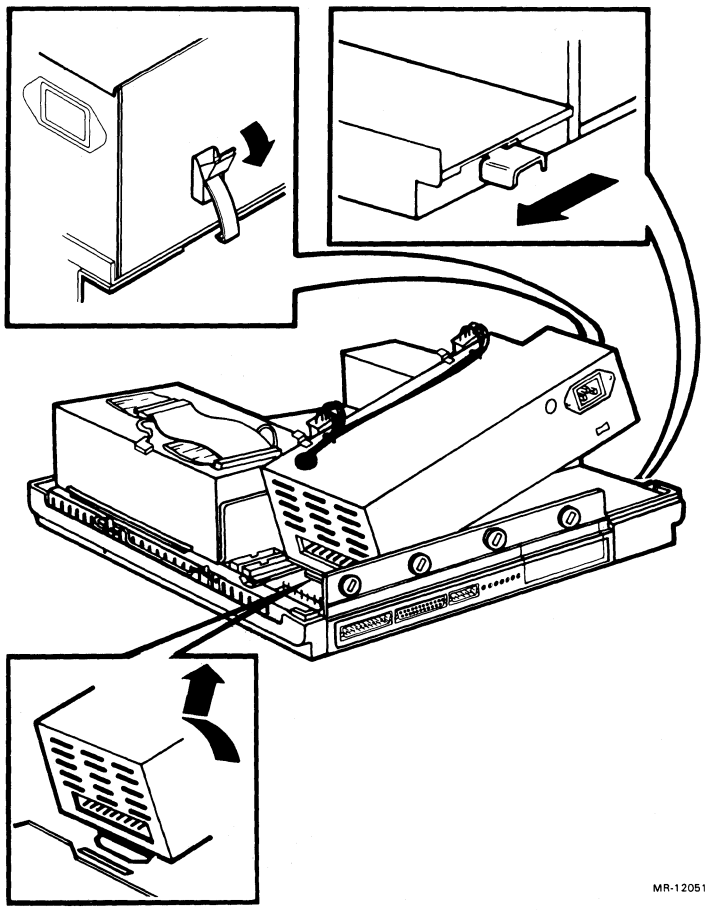


Figure 11-18 Power Supply Latches

CAUTION

When installing a new power supply, check its voltage switch. An incorrect setting can damage your computer. The common setting is 115 V in the U.S.A. and 230 V in other countries.

12. Check the voltage switch. If necessary, use a ball-point pen to set the switch to the correct setting.

11.9 FAN BRACKET ASSEMBLY REMOVAL

Use the following procedure to remove the fan bracket assembly:

1. Remove any diskettes from the diskette drives and close the doors.

2. Set the power switch to 0 (off).

WARNING

For your safety, disconnect the power cord.

3. Unplug the power cord from the wall and from the back of the system unit. Unplug all cables from the system unit

4. If you have a floor stand, remove the system unit.

5. Pull the cover release tabs toward you and out until they lock in place. Lift the cover up.

6. Squeeze the lock tabs at the ends of the plugs and pull them from the end of the power supply. The plugs are tight and may require pulling them in an up and down direction (Figure 11-17).

7. Remove the three screws from the top of the fan assembly with a Phillips screwdriver (Figure 11-19).

8. Rock and lift the fan assembly out of its slots in the system unit.

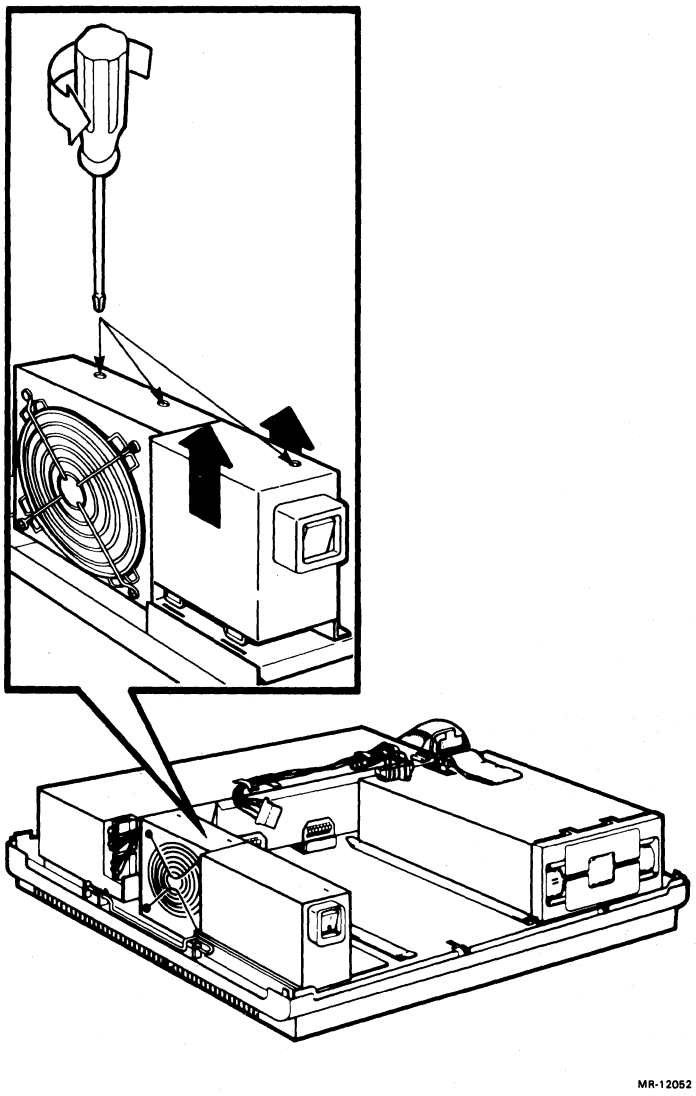


Figure 11-19 Fan Bracket Assembly Removal

CHAPTER 12
RAINBOW 100 CHARACTER SETS

12.1 DESCRIPTION

The Rainbow 100 computer recognizes all of the 8-bit character codes of the DEC Multinational Character Set shown in Figure 12-1. It also recognizes the Special Graphics Character Set shown in Figure 12-2 when it is preceded by a Select Character Set (SCS) sequence. (SCS sequences are described in subsequent paragraphs.)

Using the DEC Multinational Character Set allows the Rainbow 100 computer to process character codes from the following keyboards.

Keyboard	Part Number	Keyboard	Part Number
American (English)	LK201AA	Finnish	LK201AF
Austrian/German	LK201AG	Italian	LK201AI
Belgian/Flemish	LK201AB	Norwegian	LK201AN
Belgian/French	LK201AP	Spanish	LK201AS
British	LK201AE	Swedish	LK201AM
Canadian (French)	LK201AC	Swiss (French)	LK201AK
Danish	LK201AD	Swiss (German)	LK201AL
Dutch	LK201AH		

Each of the 15 keyboards supported by the Rainbow 100 computer is used with corresponding language ROMs that are inserted into the system module depending on the keyboard in use. The language ROMs translate keyboard position codes into the required character codes necessary for further processing.

The Rainbow 100 computer processes 7-bit character codes as though they were 8-bit character codes with the eighth bit not set.

Each character set consists of displayable or graphic characters, and nondisplayable or control characters.

In 7-bit coded character sets, control characters are contained in columns 0 and 1, and in position 7/15, while graphic characters are contained in the remaining positions of columns 2 through 7.

In 8-bit coded character sets, control characters are contained in columns 0, 1, 8, and 9 and in positions 7/15 and 15/15, while graphic characters are contained in the remaining positions of columns 2 through 7, and 10 through 15.

In all character sets, the control characters in columns 0 and 1, and position 7/15 are designated as belonging to the control character group C0. The graphic characters in the remaining positions of columns 2 through 7 are designated as belonging to the graphics left character group GL.

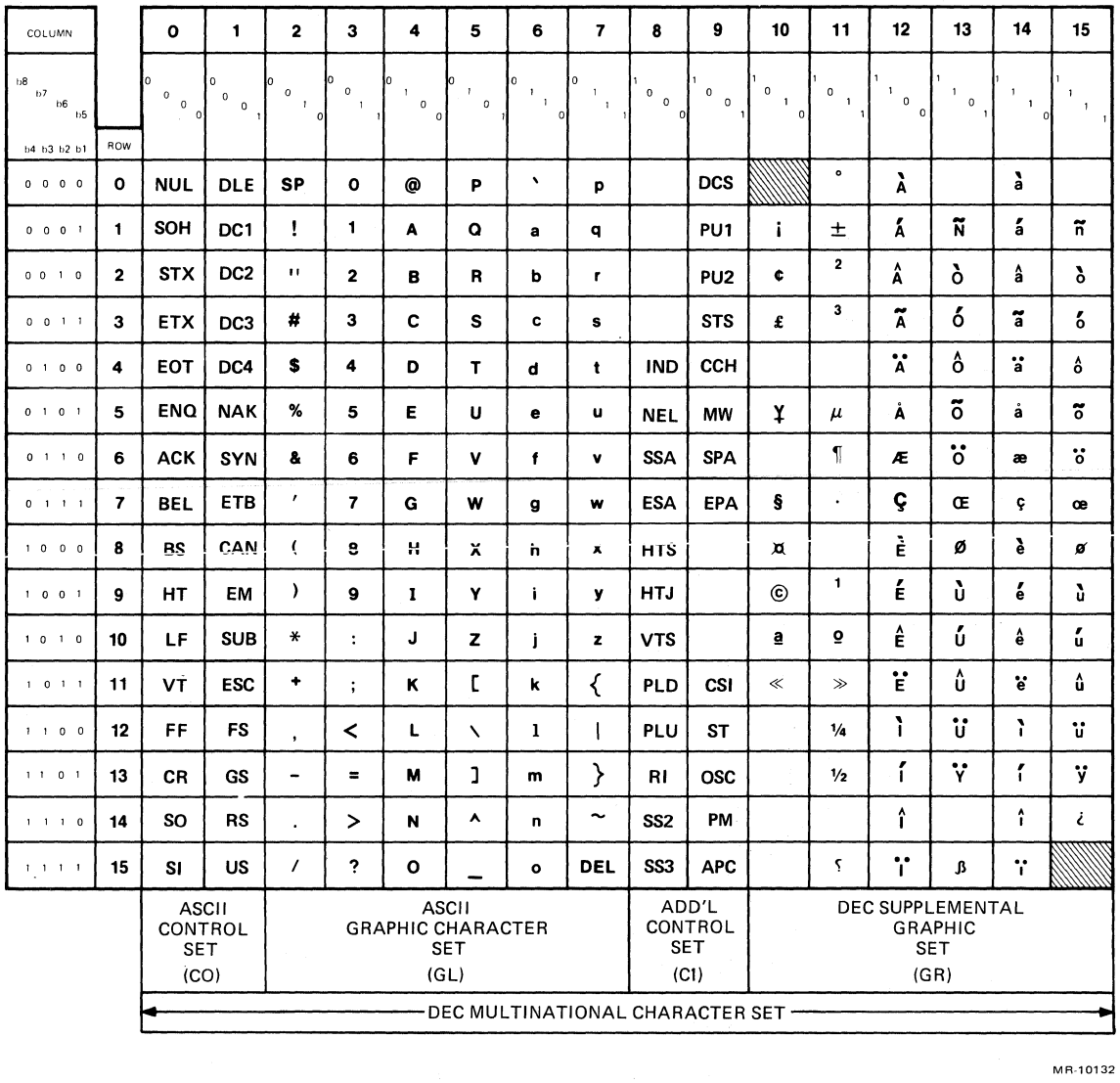


Figure 12-1 DEC Multinational Character Set

The control characters in columns 8 and 9, and position 15/15 are designated as belonging to the control character group C1. The graphic characters in the remaining positions of columns 10 through 15 are designated as belonging to the graphics right character group GR.

Figure 12-3 illustrates how the character sets are designated and used in the Rainbow 100 computer.

ROW	COLUMN 0		1		2		3		4		5		6		7	
	BITS b8 b7 b6 b5 / b4 b3 b2 b1	0 0 0 0	0 0 0 1		0 0 1 0		0 0 1 1		0 1 0 0		0 1 0 1		0 1 1 0		0 1 1 1	
0	0 0 0 0	NUL	0 0 0		20 16 10	SP	40 32 20	0	60 48 30	@	100 64 40	P	120 80 50	♦	140 96 60	— SCAN 3	160 112 70
1	0 0 0 1		1 1 1	DC1 (XON)	21 17 11	!	41 33 21	1	61 49 31	A	101 65 41	Q	121 81 51	▒	141 97 61	— SCAN 5	161 113 71
2	0 0 1 0		2 2 2		22 18 12	"	42 34 22	2	62 50 32	B	102 66 42	R	122 82 52	␤	142 98 62	— SCAN 7	162 114 72
3	0 0 1 1	ETX	3 3 3	DC3 (XOFF)	23 19 13	#	43 35 23	3	63 51 33	C	103 67 43	S	123 83 53	␋	143 99 63	— SCAN 9	163 115 73
4	0 1 0 0	EOT	4 4 4		24 20 14	$	44 36 24	4	64 52 34	D	104 68 44	T	124 84 54	␌	144 100 64	┼	164 116 74
5	0 1 0 1	ENQ	5 5 5		25 21 15	%	45 37 25	5	65 53 35	E	105 69 45	U	125 85 55	␍	145 101 65	⎺	165 117 75
6	0 1 1 0		6 6 6		26 22 16	&	46 38 26	6	66 54 36	F	106 70 46	V	126 86 56	␀	146 102 66	⊥	166 118 76
7	0 1 1 1	BEL	7 7 7		27 23 17	'	47 39 27	7	67 55 37	G	107 71 47	W	127 87 57	␁	147 103 67	⊤	167 119 77
8	1 0 0 0	BS	10 8 8	CAN	30 24 18	(	50 40 28	8	70 56 38	H	110 72 48	X	130 88 58	␈	150 104 68	⎸	170 120 78
9	1 0 0 1	HT	11 9 9		31 25 19	)	51 41 29	9	71 57 39	I	111 73 49	Y	131 89 59	␉	151 105 69	⎽	171 121 79
10	1 0 1 0	LF	12 10 A	SUB	32 26 1A	*	52 42 2A	:	72 58 3A	J	112 74 4A	Z	132 90 5A	␊	152 106 6A	⎼	172 122 7A
11	1 0 1 1	VT	13 11 B	ESC	33 27 1B	+	53 43 2B	;	73 59 3B	K	113 75 4B	[	133 91 5B	␋	153 107 6B	⎻	173 123 7B
12	1 1 0 0	FF	14 12 C		34 28 1C	,	54 44 2C	<	74 60 3C	L	114 76 4C	\	134 92 5C	␌	154 108 6C	≠	174 124 7C
13	1 1 0 1	CR	15 13 D		35 29 1D	-	55 45 2D	=	75 61 3D	M	115 77 4D	]	135 93 5D	␍	155 109 6D	£	175 125 7D
14	1 1 1 0	SO	16 14 E		36 30 1E	.	56 46 2E	>	76 62 3E	N	116 78 4E	^	136 94 5E	␎	156 110 6E	·	176 126 7E
15	1 1 1 1	SI	17 15 F		37 31 1F	/	57 47 2F	?	77 63 3F	O	117 79 4F		137 95 5F	␏ SCAN 1	157 111 6F		177 127 7F

KEY

CHARACTER **ESC** 33 OCTAL / 27 DECIMAL / 1B HEX

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Figure 12-2 Special Graphics Character Set

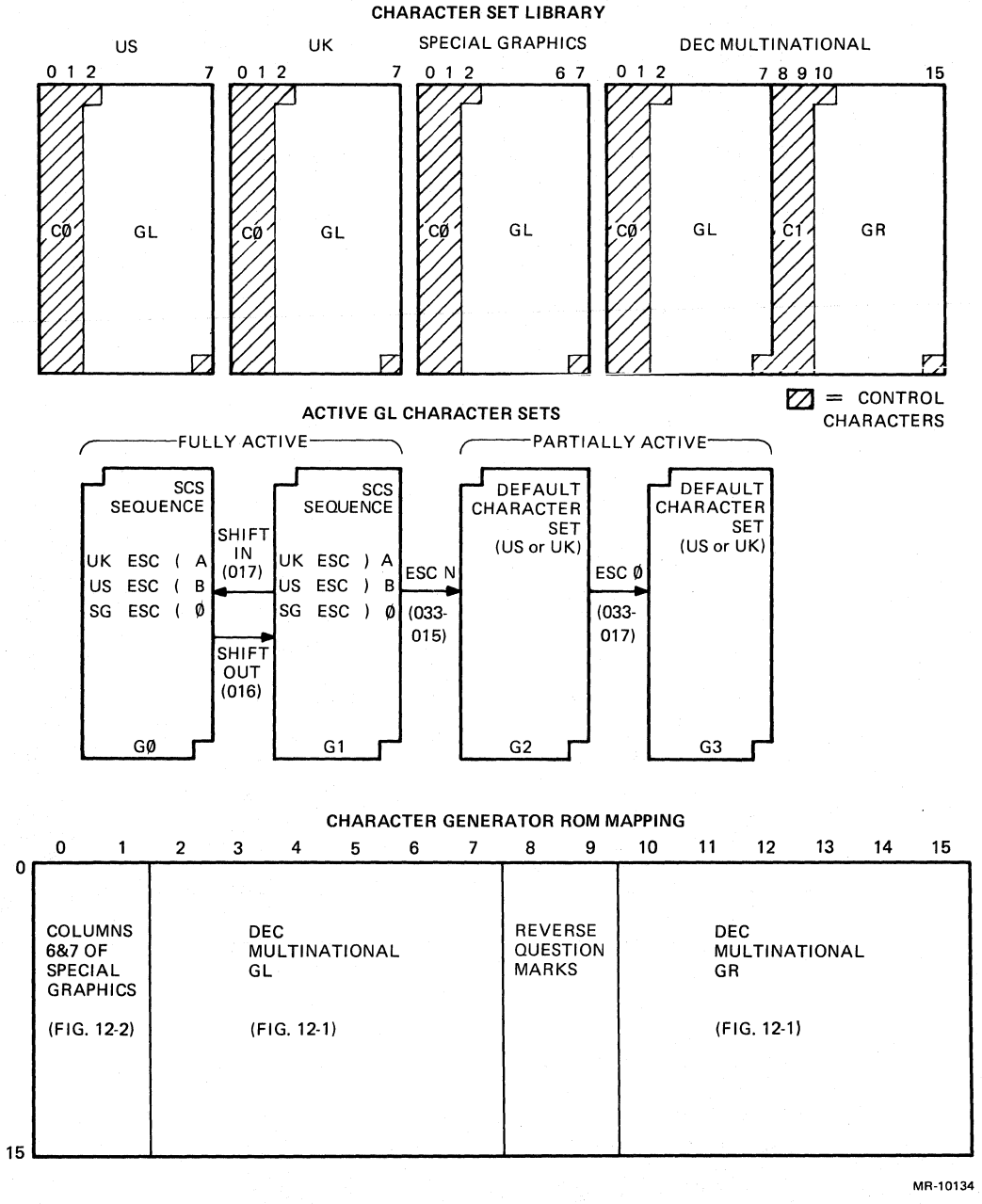

Figure 12-3 Character Set Designations

12.2 CHARACTER SET SELECTION

A GL character set is selected by using Select Character Set (SCS) sequences. SCS sequences are used to designate two GL Character Sets as fully active and two GL character sets as partially active. The two fully active GL character sets, once designated, are selected with a Shift In or Shift Out control character. Once a fully active GL character set is selected, all subsequent characters are assumed as belonging to that GL character set until an SCS sequence is again detected.

The two partially active GL character sets are selected with an escape N or escape O control character. Once a partially active GL character set is selected, only the following character is assumed as belonging to that GL character set. All subsequent characters are assumed as belonging to the previously selected, fully active GL character set.

If the Rainbow 100 firmware does not detect an SCS sequence, it assumes that all characters belong to the default GL character set. The default GL character set is assigned or determined by the value of the twelfth bit that appears on the screen in the Set-Up mode under Parameter Settings (PARAM SET). If this bit is 1, the default character set is UK; if it is 0, the default character set is USASCII.

The SCS sequences and their octal equivalents for selecting the fully active GL character sets (G0 and G1) and the partially active GL character sets (G2 and G3) are listed in Figure 12-4. Note that both the G2 and G3 designated GL character sets will always be the default character set determined in the Set-Up mode under Parameter Settings (PARAM SET).

CHARACTER SET	SCS SEQUENCE (NUMBERS IN SEQUENCE ARE IN OCTAL)			
	G0	G1	G2	G3
UK	ESC (A 033 050 101	ESC) A 033 051 101	ESC N 033 115 (IF UK SELECTED IN SET-UP MODE)	ESC O 033 117 (IF UK SELECTED IN SET-UP MODE)
USASCII	ESC (B 033 050 102	ESC) B 033 051 102	ESC N 033 115 (IF US SELECTED IN SET-UP MODE)	ESC O 033 117 (IF US SELECTED IN SET-UP MODE)
SPECIAL GRAPHICS	ESC (0 033 050 060	ESC) 0 033 051 060		

NOTE: ALL NUMBERS ARE IN OCTAL

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Figure 12-4 Character Set Selection

12.3 DISPLAYING CHARACTERS

All character codes are processed by Rainbow 100 firmware in the following order:

1. If no SCS sequences are detected, all character codes are assumed to belong to the default character set.

2. If an SCS sequence is detected, the character code is translated so that when it is input to the character generator ROM, it produces the proper character display.

NOTE

A translation between the character code received and the character code expected by the character generator ROM is necessary because, as shown in Figure 12-5, the ROM mapping for graphic characters does not always agree with the character set mapping in Figures 12-1 and 12-2.

3. All character codes with the eighth bit set will be processed as belonging to the DEC Multinational GR Character Set.

COLUMN		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
b8 b7 b6 b5		0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
b4 b3 b2 b1	ROW																
0 0 0 0	0		SCAN 3	SP	0	@	P	`	p		ς		°	À	ς	à	ς
0 0 0 1	1		SCAN 5	!	1	A	Q	a	q	ς	ς	¡	±	Á	Ñ	á	ñ
0 0 1 0	2		SCAN 7	"	2	B	R	b	r	ς	ς	¢	²	Â	Ò	â	ò
0 0 1 1	3		SCAN 9	#	3	C	S	c	s	ς	ς	£	³	Ã	Ó	ã	ó
0 1 0 0	4			$	4	D	T	d	t	ς	ς	ς	ς	Ä	Ô	ä	ô
0 1 0 1	5			%	5	E	U	e	u	ς	ς	¥	µ	Å	Õ	å	õ
0 1 1 0	6			&	6	F	V	f	v	ς	ς	ς	¶	Æ	Ö	æ	ö
0 1 1 1	7			'	7	G	W	g	w	ς	ς	§	·	Ç	Œ	ç	œ
1 0 0 0	8			(	8	H	X	h	x	ς	ς	¤	ς	È	Ø	è	ø
1 0 0 1	9			)	9	I	Y	i	y	ς	ς	©	¹	É	Ù	é	ù
1 0 1 0	10			*	:	J	Z	j	z	ς	ς	ª	º	Ê	Ú	ê	ú
1 0 1 1	11			+	;	K	[	k	{	ς	ς	«	»	Ë	Û	ë	û
1 1 0 0	12			,	<	L	\	l	|	ς	ς	ς	¼	Ì	Ü	ì	ü
1 1 0 1	13			-	=	M	]	m	}	ς	ς	ς	½	Í	Ý	í	ý
1 1 1 0	14			.	>	N	^	n	~	ς	ς	ς	ς	Î	ς	î	ς
1 1 1 1	15		SCAN 1	ς	/	?	O	_	o	DEL	ς	ς	ς	¿	Ï	ß	ï	
		SPECIAL GRAPHICS		GL						NOT USED		GR					

NOTE: REVERSE QUESTION MARKS (ς) ARE POSITIONS RESERVED FOR FUTURE STANDARDIZATION

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Figure 12-5 Character Generator ROM Displayable Characters

Figure 12-6 illustrates the data paths in various Rainbow 100 computer modes. When character codes are input to the Rainbow 100 computer application programs in the console mode, the applications software is responsible for transmitting the actual codes for each key that is pressed on the keyboard. That is, if the **Escape** key is pressed, the applications software must send Rainbow 100 firmware the character code for the **Escape** key (27 decimal, 33 octal, or 18 hexadecimal). The same thing applies to host processor software, when the Rainbow 100 computer is in the line mode. In the local mode, keyboard outputs are transmitted directly to the translation process firmware.

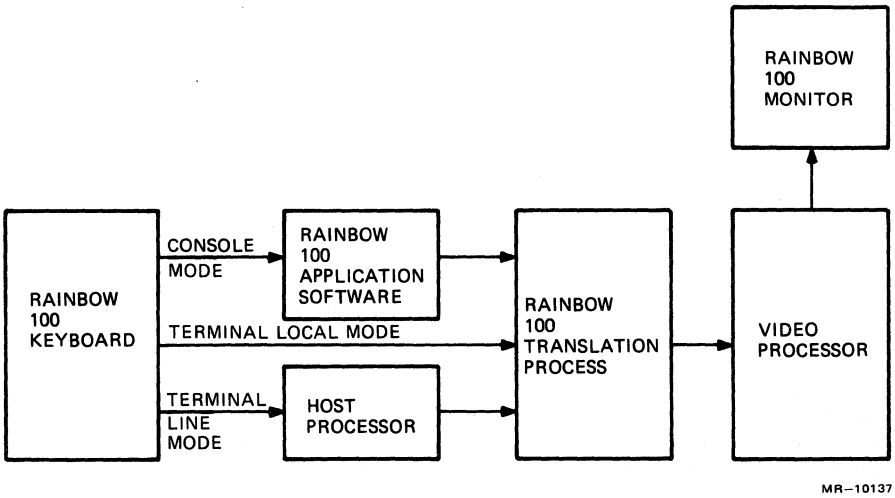

Figure 12-6 Keyboard Output Processing

APPENDIX A
SPARE PARTS, REFERENCE MANUALS, AND ORDERING INFORMATION

A.1 SPARE PARTS AND REFERENCE MANUALS

Table A-1 lists the recommended spare parts for the Rainbow 100 computer. Table A-2 lists the Rainbow 100 computer reference manuals.

Table A-1 Rainbow 100 Computer Recommended Spares List

Description	Digital Part Number
1. System module	70-19974-00
RX50 controller module	54-15482
64K-byte memory extension option, PC1XX-AA	54-15490-AA
192K-byte memory extension option, PC1XX-AB	54-15490-BA
Language ROM/carrier	
Belgium/Flemish	BG-R378A-BV
Canadian (French)	BG-R873A-BV
Danish	BG-R875A-BV
Finnish	BG-R872A-BV
Belgian/French	BG-R877A-BV
German/Austrian	BG-R878A-BV
Dutch	BG-R881A-BV
Italian	BG-R376A-BV
Norwegian	BG-R879A-BV
Spanish	BG-R377A-BV
Swedish	BG-R880A-BV
Swiss (French)	BG-R376A-BV
Swiss (German)	BG-R375A-BV
United Kingdom (British)	BG-R876A-BV
U.S.A.	70-20274-15
Color/graphics option board	54-15688-01
Extended communications option board	54-15703
Hard disk controller board	54-16019
2. Power supply	H7842-A
3. RX50 dual-diskette drive	RX50-AA

Table A-1 Rainbow 100 Computer Recommended Spares List (Cont)

Description	Digital Part Number
4. Keyboard	
U.S.A. (English)	LK201-AA
Austrian/German	LK201-AG
Belgian/French	LK201-AP
British (English)	LK201-AE
Canadian (French)	LK201-AC
Danish	LK201-AD
Dutch	LK201-AH
Finnish	LK201-AF
Belgian/Flemish	LK201-AB
Italian	LK201-AI
Norwegian	LK201-AN
Swedish	LK201-AM
Swiss (French)	LK201-AK
Swiss (German)	LK201-AL
Spanish	LK201-AS
Keyboard label strip	36-20220-12
Keycap removal tool	74-27314-01
5. Video monitor assembly (white phosphor)	VR201-A
Video monitor assembly (green phosphor)	VR201-B
Video monitor assembly (amber phosphor)	VR201-C
Color monitor	VR241-A
6. Cables	
Keyboard	17-00294
Modem	BCC15
Monitor 1.8 m (6 ft)	17-00283-00
Power supply to system modules 10.1 cm (4 in)	17-00318-02
RX50 shielded 20.3 cm (8 in)	17-00317-03
RX50 shielded 36.8 cm (14.5 in)	17-00317-04
Communications/printer 3 m (10 ft)	BCC04-10
Color monitor	17-00284-02 or BCC17
Hard disk drive	17-00427-01
7. Chassis assembly	BA25-A
8. Miscellaneous	
Fan bracket assembly, ac	70-19572-00
Line cord, 115 Vac (U.S.A., Canada, Japan)	17-00083-09
Line cord, 230 Vac	17-00199-00
Standoff, system module	12-19857-01

Table A-1 Rainbow 100 Computer Recommended Spares List (Cont)

Description	Digital Part Number
Standoff, hard disk controller	74-29164-01
Dress panel, PC100	74-26678-01
Filler panel, PC100	74-27174-01
Option panel, PC100	74-27175-01
Rainbow 100A medallion	74-27256-03
Video alignment template	29-24371-00
Communications connector loopback plug	12-15336-01
EXT COMM B loopback plug	12-15336-04
PRINTER connector loopback plug	29-24631-00
RX50 diskettes (pack of ten)	RX50K-10
Multibox suitcase	29-24209
Connector clip, RX50 controller	74-28702-01
Connector clip, RD51 controller	74-28702-02
The following parts are specific to the Rainbow 100B variation:	
Chassis assembly	BA25-CA
System module	70-19974-02
128K-byte memory board	PC1XX-AC
256K-byte memory board	PC1XX-AD
ROM 0	23-022E5-00
ROM 1 cluster 1 (German, French, English)	23-020E5-00
ROM 1 cluster 2 (Dutch, French, English)	23-015E5-00
ROM 1 cluster 3 (Finnish, Swedish, English)	23-016E5-00
ROM 1 cluster 4 (Danish, Norwegian, English)	23-017E5-00
ROM 1 cluster 5 (Spanish, Italian, English)	23-018E5-00
Power supply	H7842-D
Fan bracket assembly, dc	70-20816-01
Communications loopback plug	12-15336-04

Table A-2 Reference Manuals

Title	Digital Part Number
Rainbow™ 100 Installation Guide	EK-P100E-IN
Rainbow™ 100 Owner's Manual	EK-P100E-OM
Rainbow™ 100 User's Service Guide	EK-P100E-SV
Rainbow™ 100 Pocket Service Guide	EK-PC100-PS
PC100 Rainbow™ 100 System Unit IPB	EK-SB100-IP
VR241-A Color Video Monitor Pocket Service Guide	EK-VR241-PS

Digital customers may purchase manuals by contacting:

Digital Equipment Corporation
Accessories and Supplies Group
P.O. Box CS2008
Nashua, New Hampshire 03061

Digital Field Service personnel may order manuals from:

Publishing and Circulation Services
Order Processing Department
444 Whitney Street, NR2-2/W03
Northboro, Massachusetts 01352

A.2 ORDERING INFORMATION

Contact your local Digital Equipment Corporation Sales office or call Digital's Direct Catalog Sales toll-free (800) 258-1710 from 8:30 a.m. to 5:00 p.m. eastern standard time (U.S. customers only). In New Hampshire, Alaska, and Hawaii, call (603) 884-6660.

Terms and conditions include net 30 days and FOB from the Digital shipping point. Freight charges are prepaid by Digital and added to the invoice. (Orders placed against an open line of credit require the customer to pay the shipment charge.)

Shipment charges for all cash orders (that is, payment by check, MasterCard™, Visa®, or American Express®) are paid by Digital for shipment within the continental United States.

The payment of state and local taxes, duties, and levies is the responsibility of the buyer.

The minimum order is $35.00, but this minimum does not apply when full payment is sent with the order.

Make checks and money orders payable to *Digital Equipment Corporation.*

A.3 RELATED DOCUMENTS

The following documents provide additional technical and programming information for the Rainbow 100™ computer.

Title	Order From
Z80™-CPU/Z80A™-CPU Technical Manual *Z80 CPU Programmer's Reference Guide*	Zilog, Inc 1315 Dell Avenue Campbell, California 95008
8251A Programmable USART Specification *iAPX 86, 88 User's Manual* *iAPX 88 Book*	Intel Corporation 3065 Bowers Avenue Santa Clara, California 95051
PD7201 Technical Manual	NEC Electronics, Inc. One Natick Executive Park Natick, Massachusetts 01760

APPENDIX B
ERROR MESSAGES

NOTE

To use the error messages effectively, you should know which test generated the error message (power-up, reset, selftest, or the diagnostic diskette test number). Then look under the appropriate column in Table B-1, or the individual test in Table B-2, for the error message and the corrective action.

B.1 ROM-BASED DIAGNOSTIC ERROR MESSAGES

Table B-1 lists the error messages that can be displayed during power-up, reset, or selftest. It also shows the corresponding LED display on the back of the system unit. (Refer to Figure B-1.)

B.2 DISKETTE-BASED DIAGNOSTIC ERROR MESSAGES

Table B-2 lists the error messages that can be displayed while running the diskette-based diagnostic tests. The error messages in Table B-2 are grouped according to the tests that generate the error message. Within groups, the error messages are listed alphabetically. There are 12 individual tests, not including options, that can be run, and each individual test generates error messages unique to that particular test.

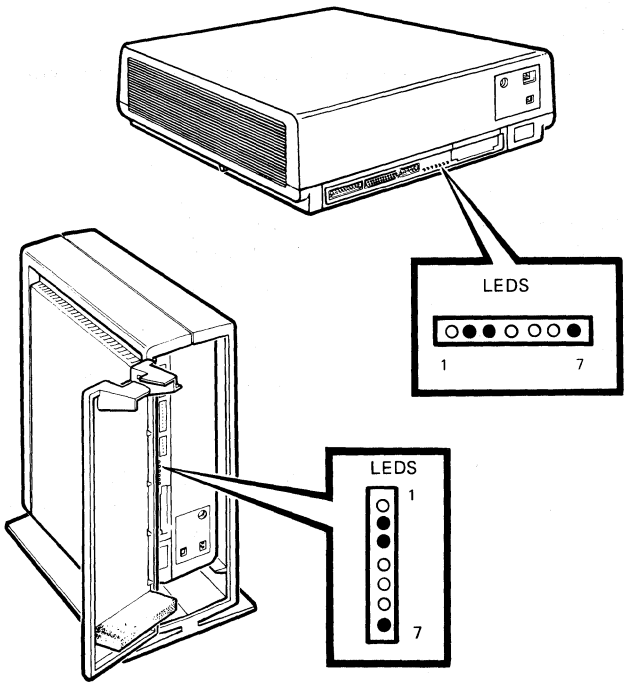

Figure B-1 Example of LED Display on the Back of the System Unit

Table B-1 Internal Diagnostic Test Messages

Message Number*	Message	Tested During: Power-Up	Reset	Self-test	Light Display 1 2 3 4 5 6 7	Fatal	Corrective Action
1	Main Board [video]†	Yes	No	Yes	o ● ● o ● o ●	Yes	Replace system module.
2	Main Board [unsolicited] interrupt††	Yes	Yes	Yes	● ● ● ● o ● o	Yes	Check switches and components on the memory board. See *Rainbow™ Memory Test Procedure* (EK-RBMXE-IN-CN1). For PC100B model, run diagnostic test without memory board installed. If error persists, replace system module.
3	Drive X [index]	No	No	Yes	o o ● o o ● ●	No	Check diskette, it may be upside down. If error persists, replace diskette drive.
4	Drive X [motor]	No	No	Yes	● ● o o o ● ●	No	Try a new diskette. If error persists, replace diskette drive.
5	Drive X [seek]	No	No	Yes	o ● o o o ● ●	No	Diskette may be unformatted; try a new diskette. If error persists, replace diskette drive.
6	Drive X [read]	No	No	Yes	● o o o o ● ●	No	Diskette is bad or is for a different computer; try a new diskette. If error persists, replace diskette drive.
7	Drive X [restore]	Yes	No	Yes	o ● ● o o ● ●	No	Check connection between board and drive. Replace diskette drive unit assembly. Try again.
8	Drive X [step]	Yes	No	Yes	● o ● o o ● ●	No	Check connection between board and drive. Replace diskette drive unit assembly. Try again.

9	System Load Incomplete [system load]	No §	No	No	o o o o o o o	No	Try another operating system diskette.
10	Main Board [video vfr]	Yes	No	Yes	● ● ● o ● o ●	Yes	Replace system module.
11	System Load Incomplete [boot load]	No §	No	No	o o o o o o o	No	RX50 diskette is blank and unformatted; try a new diskette.
12	Drive X [not ready]	No	No	Yes	o o o o o ● ●	No	Make sure a diskette is installed in Drive X and its door is closed. If error persists, replace diskette drive.
13	Keyboard	Yes	Yes	Yes	● ● o ● o ● o	Yes	Make sure keyboard cable is plugged in. Do not press any keys while the computer is going through power-up or reset. Check for any keys that may be stuck. Make sure video cable is securely plugged in. Replace keyboard or its cable.
14	Main Board [nvm data]	Yes	No	Yes	● ● ● ● o ● ●	No	Enter Set-Up and recall default settings by pressing **<Shift/D>**. Save these settings by pressing **<Shift/S>**. Turn power off then on; if this error still occurs, replace system module.
16	Interrupts Off [Main Board, interrupts off]††	Yes	Yes	Yes	● ● ● o o o o	Cond.	If this error occurs during power-up or selftest, turn power off then on again. If error persists, replace system module; if this error occurs during an application program, the error can be a program "bug" (in either the operating system or the application program) that turns off the interrupts for an excessive time.

* The message number displays on the PC100B model only.
† The words in brackets in the message column are those that the PC100A version of the computer displays.
†† These errors can occur at any time because their circuits are tested constantly.
§ These messages may occur on the PC100B model during power-up if auto-boot is selected.

NOTES:

● = On, o = Off, - = On or Off.
Cond. = Conditional
Drive X = Drive A, B, C, or D.

Table B-1 Internal Diagnostic Test Messages (Cont)

Message Number*	Message	Tested During: Power-Up	Reset	Self-test	Light Display 1 2 3 4 5 6 7	Fatal	Corrective Action
17	Main Board [video ram]	Yes	Yes	Yes	● ● ● o ● ● o	Yes	Replace system module.
18	Main Board [Z80 crc]	Yes	Yes	Yes	● ● ● ● o o ●	Yes	Replace system module.
19	Main Board [ram 0–64K]	Yes	Yes	Yes	- - - ● ● o ●	Yes	Replace system module.
20	Main Board [unsolicited interrupt, Z80]††	Yes	Yes	Yes	● ● ● o o o ●	Yes	Replace system module.
21	Drive Not Ready	No§	No	No	o o o o o ● ●	No	Make sure a diskette is installed in Drive X and its door is closed. If error persists, replace diskette drive.
22	Remove Card or Diskette	Yes	Yes	Yes	o ● ● o o o ●	No	Remove card or check diskette.
23	Non-System Diskette	No§	No	No	o o o o o o o	No	Try another operating system diskette.
24	New Memory Size = nnnK	Yes	No	No	o o o o o o o	No	Not an error. Monitor displays this message after installing or removing additional memory. (PC100B only)
25	Set-Up Defaults Stored	Yes	Yes	Yes	o o o o o o o	No	Check Set-Up selections.
26	Main Board [ram arbitration]	Yes	No	Yes	● ● ● o ● o o	Yes	Replace system module.
27	Memory Board [ram option]	No	No	Cond.	- - - ● ● o o	No	Check Set-Up display–memory on PC100A model. Be sure to save the memory size. Reseat memory board. Try again. Replace memory board. For PC100B model, see *Rainbow™ Memory Test Procedure* (EK-RBMXE-IN-CN1).

28	RX50 Controller Board	Yes	No	Yes	● ● ● o o ● ●	No, but you cannot boot a diskette; use terminal mode only.	Make sure RX50 controller module is seated firmly on system module. Replace RX50 controller.
29	Main Board [Z80 response]††	Yes	Yes	Yes	● ● ● ● o o o	No	Make sure you are not using a VT180 system diskette. Turn computer off, then on again. If error persists, replace system module.
30	Main Board [rom crc, rom 0]	Yes	No	Yes	● ● ● ● ● ● ●	Yes	Replace system module.
31	Main Board [rom crc, rom 1]	Yes	No	Yes	● ● ● ● ● ● o	Yes	Replace system module.
	Main Board [rom crc, rom 2]	Yes	No	Yes	● ● ● o ● ● ●	Yes	Replace system module.
33	Main Board [contention]	Yes	No	Yes	o o o o o ● o	Yes	Replace system module.
40	Main Board [printer port]	Yes	No	Yes	● o ● ● o ● o	No, but you cannot use the printer.	Replace system module.
50	Main Board [keyboard port]	Yes	No	Yes	o o ● ● o ● o	Yes	Replace system module.
60	Main Board [comm port]	Yes	No	Yes	o ● ● ● o ● o	No, but terminal mode is not operational.	Replace system module.

* The message number displays on the PC100B model only.
† The words in brackets in the message column are those that the PC100A version of the computer displays.
†† These errors can occur at any time because their circuits are tested constantly.
§ These messages may occur on the PC100B model during power-up if auto-boot is selected.

NOTES:

● = On, o = Off, - = On or Off.
Cond. = Conditional
Drive X = Drive A, B, C, or D.

Table B-2 Diskette-Based Diagnostic Error Messages

Error Message	Corrective Action
System Tests Error Messages	
SYSTEM ERROR: (followed by:)	Try another system diskette.
COMPUTER CANNOT FIND SUFFICIENT MEMORY	
DISK READ OR WRITE FAILED RESTART SYSTEM	
COMPUTER CANNOT READ TEST FILE FROM THE DISK	
COMPUTER CANNOT READ MESSAGE FILE FROM THE DISK	
COMPUTER NOT RUNNING CORRECTLY	
Individual Test 1 (Memory - 8088) Messages)	
ERROR: OPTION MEMORY BOARD NOT PRESENT; SET-UP SHOWS IT PRESENT	Check memory board connection.
ERROR: OPTION MEMORY BOARD PRESENT SET-UP SHOWS IT NOT PRESENT	Check memory board connection.
ERROR: SET-UP FOR MEMORY SIZE IS NOT CORRECT	Check memory board connection.
FAILURE: MAIN BOARD: INVALID SET-UP DATA FOR OPTIONAL MEMORY	Retry test. If error persists, replace system module.
FAILURE: MAIN BOARD: MEMORY STORES DATA INCORRECTLY	Retry test. If error persists, replace system module.
FAILURE: MEMORY OPTION BOARD: MEMORY STORES DATA INCORRECTLY	Check connection. Retry test. If error persists, replace memory option.
FAILURE: MEMORY OPTION BOARD: PARITY DETECTION DOES NOT WORK	Check connection. Retry test. If error persists, replace memory option.
FAILURE: OPTION MEMORY: MEMORY SIZE IS INCORRECT	See *Rainbow™ Memory Test Procedure.*
FAILURE: OPTION MEMORY: MEMORY SIGNAL IS INCORRECT	Replace memory board.
SYSTEM ERROR: SYSTEM CANNOT FIND SUFFICIENT MEMORY	Try another diskette. If error persists, replace system module.

Table B-2 Diskette-Based Diagnostic Error Messages (Cont)

Error Message	Corrective Action
SYSTEM ERROR: SYSTEM CLOCK DOES NOT WORK	Try another diskette. If error persists, replace system module.
TEST CANNOT CONTINUE – PLEASE RESTART SYSTEM	Press <**Set-Up**>, then <**Ctrl**> <**Set-Up**>
Individual Test 2 (Memory – 8088/Z80) Messages	
FAILURE: MAIN BOARD: MEMORY STORES DATA INCORRECTLY	Retry test. If error persists, replace system module.
SYSTEM ERROR: SYSTEM CANNOT FIND SUFFICIENT MEMORY	Try another diskette. If error persists, replace system module.
SYSTEM ERROR: TEST PROGRAM DOES NOT FUNCTION CORRECTLY	Try another diskette. If error persists, replace system module.
Individual Test 3 (Video Controller) Messages	
FAILURE: MAIN BOARD: VIDEO ERROR-LOOPBACK CHECK IS INCORRECT	Retry test. If error persists, replace system module.
FAILURE: MAIN BOARD: VIDEO ERROR-VERTICAL RETRACE RATE	Retry test. If error persists, replace system module.
Individual Test 4 (Disk System) Messages	
FAILURE: DRIVE X: DISKETTE WRITE PROTECTED	Remove write-protect tab on diskette. Try again.
FAILURE: DRIVE X: DRIVE NOT READY	Check connector between drive and board. Close door or insert diskette correctly. Replace diskette drive.
FAILURE: DRIVE X: (followed by:) INDEX PULSE MOTOR SPEED MULTI-TRACK TIMING READ SECTOR RESTORE SEEK (with verify) STEP STEP-IN STEP-OUT WRITE SECTOR	Try another diskette. Check connector between board and drive. If error persists, replace drive.
FAILURE: MAIN BOARD: ILLEGAL INTER-RUPT TO Z80	Repeat tests. If error persists, replace system module.

Table B-2 Diskette-Based Diagnostic Error Messages (Cont)

Error Message	Corrective Action
FAILURE: MAIN BOARD: Z80 RESPONSE FAILURE	Repeat tests. If error persists, replace system module.
FAILURE: RX50 CONTROLLER BOARD: (followed by:) FORCED LOST DATA (read) FORCED LOST DATA (write) FORCED RECORD NOT FOUND (read) FORCED RECORD NOT FOUND (write) FORCED SEEK HEAD LOAD TIMING INTERNAL REGISTER LOOP BACK READ MOTOR SHUT OFF NO TRACK GREATER THAN 43 SIGNAL RESTORE SEEK (with no verify) WRITE SECTOR	Reseat the controller board and retry tests. If error persists, replace controller.
SYSTEM ERROR: INSUFFICIENT MEMORY FOR DIAGNOSTICS	Try another diagnostic diskette.
Z80 DIAGNOSTIC FILE NOT FOUND	Try another diagnostic diskette.
Individual Test 8 (Memory – Z80) Messages	
FAILURE: MAIN BOARD: (followed by:) Z80 CANNOT COPY DATA TO SHARED (Z80/8088) MEMORY	Retry test. If error persists, replace system module.
Z80 CANNOT RESTORE DATA TO Z80 PRIVATE MEMORY – TEST CANNOT CONTINUE, PLEASE RESTART SYSTEM	
Z80 DID NOT EXECUTE THE TEST CORRECTLY	
Z80 FAILED TO COMPLETE MEMORY TEST	
Z80 FAILED TO START MEMORY TEST	
Z80 PRIVATE MEMORY DOES NOT STORE DATA CORRECTLY	

Table B-2 Diskette-Based Diagnostic Error Messages (Cont)

Error Message	Corrective Action
SYSTEM ERROR: CANNOT LOAD Z80 TEST PROGRAM FROM THE DISKETTE	Try another diskette. If error persists, replace system module.
SYSTEM ERROR: TEST DOES NOT FUNCTION CORRECTLY	Try another diskette. If error persists, replace system module.
Individual Test 9 (Keyboard) Messages	
SYSTEM ERROR: KEY PROCESSING INCONSISTENCY	Try another diskette. If error persists, replace system module.
Individual Test 10 (Memory - Setup) Messages	
FAILURE: MAIN BOARD: CANNOT COPY SET-UP MEMORY	Replace system module.
FAILURE: MAIN BOARD: SET-UP MEMORY DOES NOT STORE DATA CORRECTLY	Replace system module.
Individual Test 11 (Comm/Printer Ext Loopback) Messages	
FAILURE: MAIN BOARD: COMM:	Make sure loopback plug is properly seated. If error persists, replace system module.
Individual Test 12 (System Interaction) Messages	
FAILURE: DISKETTE WRITE PROTECTED	Remove write-protect tab.
FAILURE: DRIVE B WRITE ERROR	Retry test. If error persists, replace system module.
FAILURE: MAIN BOARD: (followed by:) COMM CHANNEL (A) ERROR DISK WRITE ERROR I/O ERROR PRINTER/KEYBOARD PORT ERROR SYSTEM ERROR	Retry test. If error persists, replace system module.
Z80 DIAGNOSTIC FILE NOT FOUND	Try another diagnostic diskette.

APPENDIX C
GLOSSARY OF TERMS AND ABBREVIATIONS

A

Access Time – The time interval between the request to store (or retrieve) data and the actual start of the storage (or retrieval) process.

Address – A number, label, or name that indicates the location of data in memory.

Alphanumeric Character – A character generated by a standard keyboard (alphabetic, numeric, symbol, or control character).

Architecture – The basic building blocks of a hardware or software system.

ASCII – American Standard Code for Information Interchange.

ASCII Code – A code consisting of 7 binary digits to represent 128 different characters (letters, numbers, symbols, carriage return, tab, etc.).

Assembly – A hardware item consisting of two or more subassemblies, such as the power and fan assemblies. In software, the process of converting a program written in assembly language into a binary coded program that is capable of being executed.

Asynchronous – Pertaining to a communications method in which the data has its own synchronizing information in start and stop bits.

Attribute – A characteristic assigned to a character or a word, such as boldface, underlining, or blinking.

Attribute RAM – A memory bank (4K bytes of Random Access Memory) for storing the attributes of each character in screen memory.

Auto-Answerback – A feature in the Rainbow 100 computer that allows it to send its answerback message to a host computer when communications are established between computers.

Auto-Screen Blank – A feature in the Rainbow 100 computer that turns off the display on the screen after 30 minutes, leaving only a "phantom" blinking cursor.

Auto-Wrap – A feature in the Rainbow 100 computer that prevents characters from printing over the last character on a line; instead, they continue printing on the next line.

Auto-XON/XOFF – A feature in the Rainbow 100 computer that automatically synchronizes it to a host computer so as not to lose data.

Auxiliary Memory – A device used for storing information from the computer, such as disks, tapes, drums, etc. (Also called secondary storage.)

B

Baud Rate – The rate at which data is received or transmitted in bits/second for serial transmissions, and bytes/second for parallel transmissions.

Binary – Two-valued arithmetic or logic, using values 1 and 0. All computer programs use the binary form.

Bit – A binary digit whose value is either a zero or a one. The smallest unit of data in a computer.

Bootstrap – A program that is used to load the operating system. The program requires nothing more than the application of power and proper insertion of the operating system disk into the disk drive.

Break – 1) To open. 2) A signal to stop transmission. 3) A space (0) on the transmit data line of transmission is enabled. 4) The key used to generate such a signal.

Buffer – A storage area meant to temporarily hold data being transferred between two devices.

Bus – A circuit or group of circuits that provide a communication path between two or more devices, such as between a central processor, memory, and peripherals.

Byte – A group of binary digits that are used to represent a unit of information, such as a letter of the alphabet, a numeral, a symbol, etc. In the Rainbow computer, a byte consists of eight binary digits (bits).

C

CCITT – Comite Consultatif International Telegraphique et Telephoniques (International Telegraph and Telephone Consultive Committee), which sets international communications standards.

Channel – A path for electrical transmission between two points.

Character – A letter, a digit, a symbol, or an operation (such as a space, carriage return, tab, etc.) that is recognized by the computer.

Character Generator – An electronic circuit, in conjunction with other circuits, that causes a letter, numeral, or symbol to be displayed on a video monitor when an 8-bit code is received by it.

Character Set – A group of characters, each of which is recognized by the computer in the form of 8 binary digits. The Rainbow computer character set consists of up to 255 characters that include foreign characters and symbols.

Checksum – A value representing the total or sum of all bytes in a program. The checksum is used to verify that the entire program has been loaded.

Chip – A thin slice of silicon or germanium, containing electronic circuits, that is typically wired or plugged into a printed circuit board.

Command – An instruction to a computer program, entered by typing on the keyboard.

Communications Controller – Circuits used to interface the computer with another computer.

Component – A functional part of a system, subsystem, module, etc.

Contention – A conflict between the two processors in the Rainbow 100 computer over a signal's availability.

Control (Ctrl) – The key used to start a control function.

Control Character – A nondisplayable character, such as return, space, horizontal tab, etc.

Control Function – An action that affects the processing, transmission, or interpretation of data.

Controller – Circuits used to control the transfer of address, data, and control signals between a computer and a peripheral device.

CP/M-86 – An operating system used with the Rainbow 100 computer developed by Digital Research Inc.

CRT – Cathode ray tube. Displays video information. Converts electrical signals to light.

Cursor – The blinking marker on the screen that indicates where the next character typed will be placed.

Cyclic Redundancy Check (CRC) – An error detection scheme in which a check character is generated by taking the remainder after dividing all the serialized bits in a block of data by a predetermined binary number. This remainder is then appended to the transmitted data and recalculated and compared at the receiving point to verify data accuracy.

D

Data – A general term for information (numbers, letters, and symbols) stored, for example, on a diskette.

Default – The value of a selection assumed by the computer when a specific value is not supplied by the user.

Delimiter – A character that terminates a character string or message, or separates it from the surrounding text.

Diagnostic Program – A program that detects and isolates malfunctions.

Direct Memory Access (DMA) – A method of transferring blocks of data directly between a peripheral device and system memory without the need of microprocessor intervention. This method significantly increases the data transfer rate, hence system efficiency.

Diskette – A flat, circular, flexible, plastic platter (similar to a 45-rpm phonograph record) that is used for storing information. Normally, the diskette is housed in a square-shaped cover with cutouts to allow its being used without removing it from its cover. (Also known as a floppy disk.)

Display – The current active area of the screen—that is, the area inside the scrolling region or the entire screen, depending on the origin mode.

Dot – The smallest displayable unit of information on the screen.

Dual-Diskette Drive – Storage device that uses a single motor to spin two diskettes (for magnetically recording or reading information).

Dual Processor – The use of two processors (the Z80A and the 8088) to execute 8- and 16-bit instructions, respectively.

Duplex – Simultaneous, two-way, independent transmissions in both directions; also called full duplex.

Dynamic RAM – Memory devices that use the presence or absence of a capacitive charge to store a value. The charge must be refreshed periodically.

E

EIA – 1) Electronic Industry Association, 2001 Eye Street, N.W., Washington, D.C. 20006. 2) A communications standard set by the EIA. 3) A signal that conforms to EIA standards.

Emulation – A Rainbow 100 computer feature that enables control functions similar to those of the VT52 DECscope or those that agree with current ANSI standards.

Escape (ESC) – A control character (ASCII 033_8) that provides supplementary characters or code extensions. ESC introduces a control or escape sequence.

Escape Sequence – A series of characters, the first of which is the Escape character, that instruct the computer to perform a specific operation. For example, the three characters ESC, C, and B, instruct the computer to consider the characters following as belonging to the British character set.

Extended Communications – A Rainbow 100 computer option which provides an additional general purpose port and a special high speed port.

F

FCC – Federal Communications Commission

FDXA – A full-duplex communications protocol that does not use modem control signals.

FDXB – A full-duplex communications protocol that uses modem control signals.

FDXC – A full-duplex communications protocol that uses modem control signals on a half-duplex modem; requires a special cable.

Firmware – A program of instructions that is in read-only memory (ROM) so it will not be changed. The Rainbow 100 computer's firmware includes a selftest program that runs when the computer is turned on and displays the Main System Menu.

Floppy Disk – A diskette.

Formatted diskette – A diskette that has its data track pattern already recorded on its surface. The Rainbow 100 computer must use formatted diskettes.

Function Keys – Keyboard keys that, instead of representing a character, issue a command to the computer to perform a specific operation such as entering a Set-Up mode, displaying helpful information, and other functions assigned to these keys by the software system.

H

Hardware – The physical elements that comprise a computer system; mechanical, electrical, or electronic devices.

Hertz (Hz) – A unit of frequency equal to one cycle per second.

Hex – Hexadecimal number system.

Host Processor – A computer system containing an operating system that other computing systems can use by being electrically connected to it.

I

Index – 1) To move the cursor down to the same character position on the next line. 2) The small hole in the diskette that marks the beginning of the recorded tracks.

Instructions – A repertoire of commands to the computer that follow a specific format. The repertoire of commands is usually referred to as the instruction set.

Integrated Circuit (IC) – A solid-state microcircuit consisting of interconnected active and passive semiconductor devices diffused into a single silicon chip.

Interface – Circuits that allow two or more components, units, subsystems, or systems to interact with each other.

Interlace – A kind of video display where the information from two fields is displayed by offsetting the vertical position of one field slightly from the other so the scans of one field appear between the scans of the other.

Interrupt – A request to the processor to change the flow of instruction execution by executing another set of instructions.

K

Key – A single button on the keyboard that, when pressed, sends a letter, number, symbol, or function code to the keyboard's electronic circuitry.

Keyboard – The typing device that causes characters and commands to be generated when its keys are pressed.

Keyclick – An audible sound made by the tone generator inside the keyboard when a key is pressed. In the Rainbow 100 computer the keyclick volume is adjustable in Set-Up.

L

Large Scale Integration (LSI) – High density integrated circuits for complex logic functions. LSI circuits can range up to several thousand transistors on a one-tenth of an inch silicon chip.

LED – A light emitting diode that illuminates when current passes through it.

Line Attribute – An attribute that affects an entire line of characters displayed on the screen, such as double-width and double-height characters.

Load – To insert a diskette into the diskette drive and close its door.

M

Mark State – The presence of a signal, or logical 1 condition, on the communications line.

Matrix – An arrangement that allows addressing of many individual points with few address lines. Used in the keyboard switch array.

Memory Map – A listing of addresses or symbolic representations of addresses that define the boundaries of the memory address space occupied by a program or series of programs.

Menu – A list of services or functions displayed on the screen from which you select one for the computer to do.

Microprocessor – The part of a microcomputer that contains the circuits for fetching, decoding, and executing programmed instructions and maintaining the status of results as the program is executed.

Modem – Short term for a device that MOdulates and DEModulates a signal for use in transmitting and receiving data over telephone lines.

Module – Usually refers to a plug-in electronic circuit board, such as the RX50 controller module, the extended communications module, etc.

Monitor – 1) The device that contains the video screen. 2) The video screen itself.

Monochromatic – Having only one color.

MPSC – Multiprotocol Serial Controller. Provides three basic programmable protocols: asynchronous (start/stop), byte synchronous (monosync/bisync), and bit synchronous (HDLC, and SDLC).

MS-DOS – A disk operating system developed by Microsoft Corporation.

Multiplexer (MUX) – A circuit that allows selecting one of several input signals as the output signal.

N

New Line Mode – A feature in the Rainbow 100 computer that, when in effect, causes the cursor to move to the beginning of the next line when the **Return** key is pressed.

Nonvolatile Memory (NVM) – A type of memory the contents of which can be changed. The data, however, is not lost when the computer power is turned off.

Nonvolatile RAM – Same as nonvolatile memory.

Null Modem Cable – A cable used to connect two RS-232 devices when a modem is not needed. The transmit and receive lines are reversed at the cable connectors.

O

On-Line Auxiliary Memory – A memory storage device that is electrically connected and immediately available to the computer.

Operating System – A structured set of software routines whose function is to control the execution sequence of programs run on a computer, supervise the input/output activities of these programs, and support the development of new programs through such functions as assembly, compilation, editing, and debugging.

Overrun Error – Occurs in the PUSART if the microprocessor did not read a character before the next one arrived.

P

Parallel – A data path where all bits travel simultaneously on separate wires.

Parity – 1) A method of checking for correct data that involves counting the 1 bits in each character's data pattern, and then making the sum either even or odd. 2) The choice in Set-Up for the method of checking parity, whether even, odd, mark, space, or no parity.

Peripheral Device – An active device of a computer system, such as a diskette drive, keyboard, monitor, or a printer that extends the system's capacity or functionality.

Phase Locked Loop (PLL) – A circuit used to separate and synchronize the data and clocks from the raw read data received from the diskette drive.

Polling – A process in which a number of peripheral devices, remote stations, or modes in a computer network are interrogated one at a time to determine if service is required.

Priority – The sequence in which various entries and tasks are processed or peripheral devices serviced. Priorities are based on analyses of codes associated with an entry or task, or the positional assignment of a peripheral device.

Program – A complete sequence of computer instructions necessary to solve a specific problem, perform a specific action, or respond to external stimuli in a prescribed manner. As a verb, it means to develop a program.

Protocol – The format the computer uses to transmit and receive communications signals.

PUSART – Programmable Universal Synchronous/Asynchronous Receiver Transmitter. Receives parallel data from the microprocessor and converts it to serial data, which it transmits to the keyboard. Receives serial data from the keyboard and converts it to parallel data, which it transmits to the microprocessor.

R

Random Access – Accessing or storing information simply by using its location (address). Any random location can be read or written into in the same amount of time as any other location.

Random Access Memory (RAM) – A computer's main memory to which data is written and from which data is read. This memory can be expanded in the Rainbow 100 computer by adding the memory extension option.

Raster – On a CRT screen, the effect of continuous vertical and horizontal deflections of the electron beam covering the full height and width of the screen. If the beam is turned off, the raster is not visible.

Read-Only Memory (ROM) – Part of the computer's main memory that permanently stores data that cannot be altered, even when the computer is turned off. This memory contains the instructions for the power-up and reset sequences, the selftest, and the program that interprets the keyboard's keys.

Refresh – 1) The process of repeatedly rewriting the screen with data so it appears to be constantly lit. 2) Periodically accessing dynamic memory so it will not lose its data.

Reverse Screen – A screen attribute. When the reverse screen attribute is selected, the entire screen is rendered as black characters on a white background.

Reverse Video – A character attribute. Characters are seen as dark areas in fields of light.

Rollover – Ability to accept more than one key pressed at the same time.

RS-232-C – EIA standard for communications equipment. Off or mark signals can be −3 V to −25 V; on or space signals can be +3 V to +25 V.

RS-423 – EIA standard for digital interface circuits. Signals for a binary 1 state can be −4 V to −6 V; signals for a binary 0 state can be +4 V to +6 V.

S

Screen Attribute – Applies to the entire display area; reverse screen, smooth scrolling.

Screen Memory – A memory bank (4K bytes of Random Access Memory) for storing the characters to be displayed on the screen. Same as screen RAM.

Screen Width – 1) The maximum number of characters that can be displayed across the screen on one line. 2) The setting in Set-Up that allows you to select 80 or 132 columns.

Scrolling – The movement of the lines of characters on a video monitor in a direction toward the top or bottom of the screen, in the same manner as in the old days when a proclamation was read from a scroll.

SCS Sequence – A Select Character Set sequence is a series of characters beginning with the Escape character that instructs the computer to consider the characters that follow as belonging to the character set designated by the sequence. (See also Escape sequence.)

Sector – One-tenth of a track on a diskette; it holds 512 data characters.

Serial Transmission – A method of transferring data in which the bits of the characters are sent sequentially on a single path.

Set-Up – A mode of the computer that is entered by pressing the Set-Up key, which allows you to change such features as the screen width, tab stops, margins, printer/communications baud rates, etc.

Shared Memory – The part of memory that is accessible by both processors.

Smooth Scroll – Scrolling in which the data on the screen moves only one scan per frame.

Software – The computer programs that are necessary to do useful work with the computer. Software is generally meant to include the operating system.

Space – The absence of a signal on the communications line; a logical 0 condition.

Split Screen – Display operation where one part of the screen can scroll while another part remains stationary.

Start Bit – The first bit in a serial, asynchronous byte transmission, always a space.

Static RAM – Memory devices that do not require periodic refresh cycles, unlike dynamic RAMs.

Stop Bit(s) – One or two pulses at the end of a character's data pattern that signal(s) the end of that pattern.

Synchronization – 1) Operation in exact coincidence in time or rate 2) Timing.

Synchronous – A method of transferring serial binary data between computer systems or between a computer system and a peripheral device; binary data is transmitted at a fixed rate, with the transmitter and receiver synchronized. Synchronization characters are located at the beginning of each message or block of data to synchronize the flow.

System – A combination of hardware and software that performs specific processing operations.

T

Terminal Mode – 1) An operational mode in the Rainbow 100 computer that allows it to act like a terminal, such as a VT102 video terminal. 2) Selection T on the Main System Menu.

Track – A path on a diskette that holds data. There are 80 tracks on each diskette.

U

Unit – A major component of a system, such as the keyboard, the monitor, etc.

V

Vector – The address of the first instruction for an interrupt handling routine.

Vectored Interrupt – An interrupt that points to a location in memory where a routine is stored that is associated with the interrupt.

Video Monitor – A cathode ray tube (CRT) used for displaying information.

Voltage Controlled Oscillator (VCO) – An oscillator whose frequency output is varied by increasing or decreasing the amplitude of a dc voltage input.

W

Wait State – A condition in which a process is interrupted until completion of another process, after which the interrupted process is resumed.

X

XON/XOFF – 1) The control characters that synchronize the Rainbow 100 computer to a host computer so that data transmitted between them is not lost. XON starts data transmission, XOFF stops it. 2) The Set-Up feature that enables these characters automatically. (See Auto-XON/XOFF.)

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