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Power and Energy Characterization of the Itsy Pocket Computer (Version 1.5)

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Power and Energy Characterization of the Itsy Pocket Computer (Version 1.5)

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Abstract

This technical report presents a characterization of the power consumption of the Itsy Pocket Computer Version 1.5 [1], a state-of-the art pocket computer developed by Compaq Computer Corporation's Palo Alto Labs. This characterization seeks to is to identify specific architectural features of the Itsy Pocket Computer that the operating system and applications can use to reduce total energy consumption. A secondary goal is to gather background data that can be used to explain application-specific energy usage.

This report examines the power and energy cost of: running the system at between 59 MHz and 206 MHz, reading and writing data (with and without enabling the MMU, data cache, and write buffer), reading and writing flash memory, flushing the instruction and data caches, enabling the UART, transmitting data over a serial line at numerous baud rates, and enabling and disabling the LCD.

This report also presents the DRAM access times and bandwidths supported by the Itsy Pocket Computer Architecture, as a function of the processor clock speed.

Some of the material presented in this technical note is discussed in a paper authored by Keith I. Farkas, Jason Flinn, Godmar Back, Dirk Grunwald, and Jennifer Anderson, which will appear in the Proceedings of the *ACM SIGMETRICS 2000 International Conference on Measurement and Modeling of Computer Systems.*

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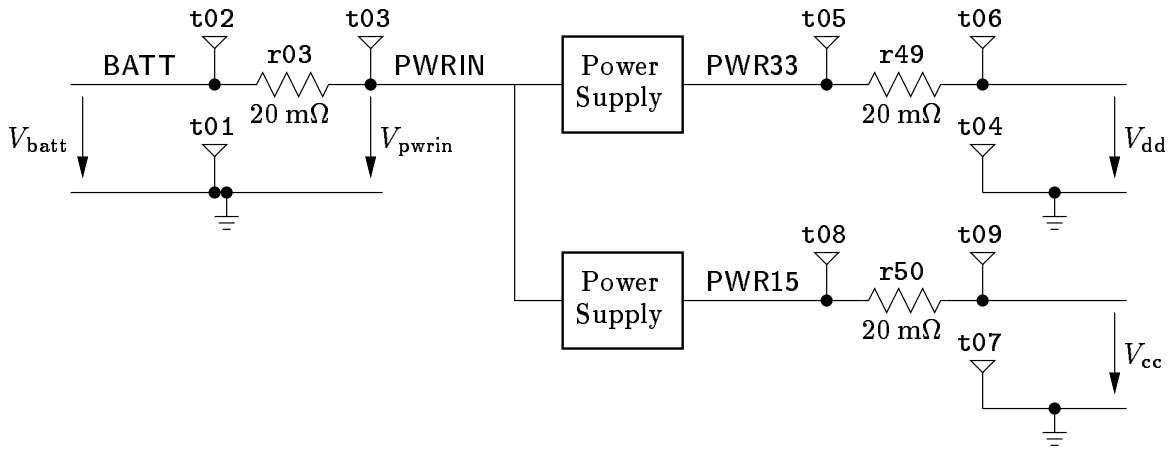

Figure 1: Precision resistors for current measurement (Itsy Version 1.5)

1 Background

This study characterizes the power consumption of the Itsy Pocket Computer [1] with a series of micro-benchmarks. The main goal is to identify specific architectural features that the operating system and applications can use to reduce total energy consumption. A secondary goal is to gather background data that can be used to explain application-specific energy usage.

This report also presents the DRAM memory access times and bandwidths of the Itsy Pocket Computer Architecture as a function of the processor speed. This data is given in the Appendix A.

Some of the material presented in this technical note is discussed in a paper authored by Keith I. Farkas, Jason Flinn, Godmar Back, Dirk Grunwald, and Jennifer Anderson, which will appear in the Proceedings of the *ACM SIGMETRICS 2000 International Conference on Measurement and Modeling of Computer Systems.*

1.1 Measurement Methodology

In this report, we examine the power and energy consumption of the Itsy Pocket Computer Version 1.5 and its components. This version of the Itsy contains two power domains, a 3.3 Volt domain, *PWR33*, and a 1.5 Volt domain, *PWR15*. The PWR15 domain powers the Itsy's microprocessor, which is a 200 MHz StrongARM SA-1100 [2]. The PWR33 domain powers all the other components. More information on the architecture of the Itsy Pocket Computer Version 1.5 is provided in the *Itsy Pocket Computer Version 1.5 Hardware Description Manual*, which is available as part of the Itsy Version 1.5 Hardware Specifications. See [3] for more information.

To measure the power consumed by each of these domains and the power supplied to the Itsy (the input power), the following procedure is used. First, consider the input power.

The input power at a time T is equal to the product of the current flowing into the Itsy at time T from a power source (e.g., a battery or power supply) and the voltage this current induces. The input current is measured indirectly by measuring the differential voltage across a small valued

resistor in the main current path. This resistor is labeled r_{03} in Figure 1; this figure shows the two power domains, and the three resistors provided for measuring current. Given that this resistor is a 20 m$\Omega \pm 1\%$ resistor, the current of interest, I_{r03}, is equal to $\frac{V_{r03}}{0.02}$, where V_{r03} is the differential voltage across r_{03}. The voltage induced by I_{r03} is the voltage between test points t_{03} and t_{01}, that is, voltage V_{pwrin}.

The instantaneous power consumed by each of the two power domains is similarly measured and calculated. Thus, six voltage measurements are required to measure both the input power and the power consumption of each power domain.

The data reported here was obtained by measuring these six voltages using six differential amplifiers and a data acquisition (DAQ) system, while the Itsy was powered by an external voltage supply. The amplifiers were employed to minimize the error introduced into our measurements by electro-magnetic noise, and the limited precision of the DAQ system. The output of each amplifier was connected to one of the analog inputs of the DAQ system. The DAQ system was in turn connected to a workstation, which initiated the measurement acquisition process and recorded the results.

The micro-benchmarks used in this work were designed to exhibit a constant load on the Itsy for a period of several seconds. During this time, the DAQ system was used to measure each of the six voltages, one at a time, as the DAQ system could only measure one channel at a time. The data reported here for each benchmark represents the average of these readings, with the first and last set of six-voltage measurements excluded. The first and last measurement were excluded because they can be inaccurate, owing to the sequential measuring of the six voltages. The power measurements from two successive trials of the same benchmark were found to differ by as much as 2 mW. Note that while this methodology is suitable for measuring the power usage of the tasks reported on here, it is not suitable for capturing more dynamic power usage, such as that from booting of an operating system.

The duration of each benchmark was measured using the StrongARM SA-1100's OS Timer Count Register (OSCR), which runs off the 3.6864 MHz oscillator. Since this register is not accurate when the processor is switching clock frequencies, care was taken to avoid measurements which spanned changes in the clock frequency.

Each benchmark was run directly on top of the hardware using the Itsy Monitor [3] (version 1.3). Therefore, no OS overhead is included in these results.

2 Clock-Rate Micro-benchmarks

2.1 Description

These micro-benchmarks examine the effect of the core clock frequency of the processor on Itsy power usage. The frequency of the SA-1100 core clock can be varied from 59.0 MHz to 206.4 MHz. Operations performed at lower clock frequencies generally consume less power, but require more time to complete. Therefore, one of the goals of these benchmarks is to examine whether reducing the core clock frequency can reduce *energy* usage.

Additionally, the SA-1100 supports a clock-switching mode, in which the core clock frequency is normally twice the speed at which the external (system) bus is run. If a read miss occurs, the

core clock frequency drops to the bus speed until the needed data is read from memory. If clock switching is disabled, then the core clock frequency is always the same as the bus speed. For example, if clock-switching is disabled and the core clock-frequency is set to 206.4 MHz, then both the core and bus operate at 103.2 MHz.

For each benchmark described below, the SA-1100 core clock frequency is varied from 59.0 MHz to 206.4 MHz. Unless otherwise noted, all configurable hardware components are disabled, with the exception of the DRAM banks, static memory, and the instruction cache.

- Sleep - measures power usage while the Itsy is in sleep mode. The benchmark stops the 3.6864 MHz oscillator and places the Itsy in sleep mode.
- Idle - measures power usage while the Itsy is in idle mode. The benchmark sets the clock speed and disables clock-switching before entering idle mode.
- Wait - measures power usage while the Itsy executes a busy-wait loop. The benchmark sets an OS match timer (OSMR0) to expire in five seconds, then continuously polls the status register until the timer expires. Clock-switching is enabled for this benchmark.
- Add - measures power usage for a compute-intensive application. The benchmark performs 300 million additions within a small loop, so that no DRAM accesses are required within the inner loop. Clock-switching is enabled for this benchmark.
- Add/NS - measures power usage for a compute-intensive application when clock-switching is disabled. As a result, the processor core always runs at the bus speed. With the exception of disabling clock-switching the benchmark is identical to the `Add` benchmark.

2.2 Data

- Figure 2: Input Power Consumption for Clock-Rate Micro-benchmarks
- Figure 3: Main (3.3 V) Power Consumption for Clock-Rate Micro-benchmarks
- Figure 4: Core (1.5 V) Power Consumption for Clock-Rate Micro-benchmarks
- Figure 5: Duration of Clock-Rate Micro-benchmarks
- Figure 6: Energy Consumption of Clock-Rate Micro-benchmarks
- Figure 7: Power consumption when the SA-1100's core voltage was lowered from 1.5 V to 1.23 V.

Clock Freq. (MHz)	Power (W)				
	Sleep	Idle	Wait	Add	Add/NS.
59.0	0.010	0.092	0.225	0.314	0.209
73.7		0.099	0.262	0.375	0.244
88.5		0.106	0.300	0.434	0.276
103.2		0.113	0.338	0.494	0.312
118.0		0.119	0.375	0.553	0.343
132.7	0.010	0.126	0.412	0.612	0.376
147.5		0.133	0.450	0.670	0.410
162.2		0.140	0.487	0.728	0.447
176.9		0.147	0.523	0.785	0.475
191.7		0.154	0.560	0.843	0.511
206.4	0.011	0.161	0.596	0.899	0.541

Figure 2: Input Power Consumption for Clock-Rate Micro-benchmarks

Clock Freq. (MHz)	Power (W)				
	Sleep	Idle	Wait	Add	Add/NS
59.0	0.009	0.034	0.035	0.039	0.041
73.7		0.034	0.035	0.039	0.043
88.5		0.034	0.035	0.039	0.042
103.2		0.034	0.035	0.039	0.045
118.0		0.034	0.035	0.039	0.043
132.7	0.010	0.034	0.035	0.039	0.042
147.5		0.034	0.035	0.039	0.043
162.2		0.034	0.036	0.039	0.048
176.9		0.034	0.036	0.039	0.043
191.7		0.034	0.036	0.040	0.047
206.4	0.011	0.034	0.036	0.040	0.043

Figure 3: Main (3.3 V) Power Consumption for Clock-Rate Micro-benchmarks

Clock Freq. (MHz)	Power (W)				
	Sleep	Idle	Wait	Add	Add/NS
59.0	0.000	0.031	0.096	0.143	0.087
73.7		0.034	0.115	0.174	0.104
88.5		0.038	0.135	0.204	0.121
103.2		0.041	0.154	0.235	0.138
118.0		0.044	0.173	0.266	0.154
132.7	0.000	0.048	0.192	0.296	0.172
147.5		0.051	0.211	0.326	0.188
162.2		0.055	0.230	0.357	0.205
176.9		0.058	0.249	0.387	0.222
191.7		0.062	0.268	0.416	0.239
206.4	0.000	0.065	0.287	0.447	0.256

Figure 4: Core (1.5 V) Power Consumption for Clock-Rate Micro-benchmarks

Clock Freq. (MHz)	Duration (s)	
	Add	Add/NS
59.0	20.345	40.690
73.7	16.276	32.552
88.5	13.563	27.127
103.2	11.626	23.251
118.0	10.173	20.345
132.7	9.042	18.084
147.5	8.138	16.276
162.2	7.398	14.796
176.9	6.782	13.563
191.7	6.260	12.520
206.4	5.813	11.626

Figure 5: Duration of Clock-Rate Micro-benchmarks

Clock Freq. (MHz)	Energy(J)	
	Add	Add/NS
59.0	6.388	8.504
73.7	6.104	7.943
88.5	5.886	7.487
103.2	5.743	7.254
118.0	5.626	6.978
132.7	5.534	6.800
147.5	5.452	6.673
162.2	5.386	6.614
176.9	5.324	6.442
191.7	5.277	6.398
206.4	5.226	6.290

Figure 6: Energy Consumption of Clock-Rate Micro-benchmarks

2.3 Discussion

As expected, sleep mode power usage does not depend upon the initial clock-rate. However, the power usage in idle mode varies significantly as the initial clock-rate changes. This variation is due to the power consumed by the microprocessor's components that still run while the it is in idle mode. This observation suggests that the core-clock frequency should be reduced whenever it is likely that the Itsy will remain idle for a significant period of time. This check could be performed in the Linux[1] idle procedure before entering idle mode.

Disappointingly, reducing the clock-frequency appears to produce no significant energy savings in other circumstances. Performing a given set of operations at a lower clock-frequency consumes less power, but also takes longer to complete. These two effects compete against each other, producing approximately equal energy consumption. The main reason for this behavior is that the voltage supplied to the SA-1100 is not reduced at the same time as is the clock frequency. These results do indicate that significant power savings might be achieved with a chip that allowed a variable voltage supply, since the energy usage is roughly equivalent without any voltage variation. Further, in this study we assume only ideal battery behavior, but as Tom Martin showed in his Ph.D. dissertation [4], lowering clock-frequency can be beneficial if the effects of non-ideal battery behavior are considered.

To understand better the power reduction that is achieved with a voltage reduction, we modified the Itsy Pocket Computer so that we could run the SA-1100 at either 1.5 Volts or 1.23 Volts; Figure 7 lists the power consumption of the Itsy and the processor for three of the micro-benchmarks at these two power levels. Clearly there is a power saving when running at a lower core voltage. Note that for the "busy wait" benchmark when the LCD was turned on, the SA-1100 would not operate properly at 206 MHz and 1.23 Volts.

As expected, disabling clock-switching increases the energy used to execute a tight loop. The

[1] The Linux operating system has been ported to the Itsy Pocket Computers.

Micro-Benchmark	Processor Voltage	Measurement	Power (Watts) at Specified MHz		
			59.0	132.7	206.4
Busy Wait	1.5	input	0.225	0.412	0.596
		core	0.096	0.192	0.287
	1.23	input	0.177	0.324	0.469
		core	0.063	0.126	0.189
Busy Wait, LCD enabled	1.5	input	0.263	0.447	0.604
		core	0.098	0.195	0.290
	1.23	input	0.217	0.363	−−
		core	0.060	0.127	−−
Addition Loop	1.5	input	0.314	0.612	0.899
		core	0.143	0.296	0.447
	1.23	input	0.247	0.490	0.719
		core	0.093	0.195	0.294

Figure 7: Power consumption when the SA-1100's core voltage was lowered from 1.5 V to 1.23 V.

time to complete the loop doubles, but the corresponding power savings is smaller.

3 Memory Micro-benchmarks

3.1 Description

These micro-benchmarks examine energy usage while reading from and writing to DRAM. The read benchmark executes a large number of load instructions inside of a tight loop that has been unrolled sixteen times. The write benchmark executes a large number of stores in a similar loop. In each benchmark, 100 MB of data is read/written. Each address in memory is read or written many times.

Both the read and write benchmarks are executed with two different patterns of data access. When the `in-cache` pattern is used, all load (or store) instructions hit in the data cache. When the `out-of-cache` pattern is used, all load (or store) instructions miss in the data cache.

Each micro-benchmark is executed with the following memory-management options:

- IMWD - The instruction cache, MMU, write-buffer and data cache are all enabled.
- IMW - The instruction cache, MMU, and write-buffer are enabled. The data cache is disabled.
- IM - The instruction cache and MMU are enabled. The data cache and write-buffer are disabled.
- I - Only the instruction cache is enabled. All data is addressed physically.

For each of scenario, the core clock frequency was varied from 59 MHz to 206.4 MHz. In addition, each benchmark was executed with clock-switching enabled and with switching disabled.

3.2 Data

- Figure 8: Input Power Consumption of Memory Micro-benchmarks with Clock-Switching Enabled
- Figure 9: Input Power Consumption of Memory Micro-benchmarks with Clock Switching Disabled
- Figure 10: Main (3.3V) Power Consumption of Memory Micro-benchmarks with Clock-Switching Enabled
- Figure 11: Main (3.3V) Power Consumption of Memory Micro-benchmarks with Clock Switching Disabled
- Figure 12: Core (1.5V) Power Consumption of Memory Micro-benchmarks with Clock-Switching Enabled
- Figure 13: Core (1.5V) Power Consumption of Memory Micro-benchmarks with Clock Switching Disabled
- Figure 14: Duration of Memory Micro-benchmarks with Clock-Switching Enabled

Clock Freq. (MHz)	Data Locality	Power (W)							
		Read				Write			
		IMWD	IMW	IM	I	IMWD	IMW	IM	I
59.0	In Cache	0.385	0.503	0.504	0.504	0.383	0.730	0.568	0.566
59.0	Out of Cache	0.458	0.522	0.523	0.523	0.731	0.730	0.568	0.566
73.7	In Cache	0.462	0.589	0.591	0.591	0.461	0.868	0.671	0.669
73.7	Out of Cache	0.518	0.613	0.614	0.612	0.868	0.868	0.671	0.669
88.5	In Cache	0.538	0.635	0.636	0.625	0.538	1.006	0.777	0.774
88.5	Out of Cache	0.565	0.658	0.660	0.658	1.006	1.006	0.777	0.774
103.2	In Cache	0.614	0.713	0.714	0.712	0.613	1.143	0.879	0.876
103.2	Out of Cache	0.624	0.740	0.742	0.739	1.142	1.143	0.879	0.876
118.0	In Cache	0.689	0.791	0.792	0.789	0.688	1.170	0.981	0.976
118.0	Out of Cache	0.680	0.821	0.824	0.820	1.168	1.170	0.981	0.976
132.7	In Cache	0.763	0.811	0.813	0.809	0.762	1.292	1.081	1.075
132.7	Out of Cache	0.719	0.843	0.844	0.840	1.290	1.292	1.081	1.075
147.5	In Cache	0.837	0.881	0.883	0.879	0.835	1.321	1.073	1.066
147.5	Out of Cache	0.709	0.916	0.918	0.913	1.318	1.321	1.073	1.066
162.2	In Cache	0.909	0.951	0.953	0.948	0.909	1.436	1.164	1.157
162.2	Out of Cache	0.715	0.989	0.992	0.986	1.432	1.434	1.164	1.157
176.9	In Cache	0.980	0.961	0.963	0.958	0.980	1.448	1.130	1.122
176.9	Out of Cache	0.746	0.998	1.000	0.995	1.443	1.448	1.130	1.122
191.7	In Cache	1.052	1.025	1.027	1.023	1.050	1.489	1.127	1.120
191.7	Out of Cache	0.789	1.065	1.068	1.063	1.484	1.489	1.127	1.120
206.4	In Cache	1.133	1.025	1.027	1.023	1.120	1.579	1.191	1.183
206.4	Out of Cache	0.777	1.065	1.068	1.063	1.572	1.579	1.191	1.183

Figure 8: Input Power Consumption of Memory Micro-benchmarks with Clock-Switching Enabled

- Figure 15 : Duration of Memory Micro-benchmarks with Clock Switching Disabled
- Figure 16 : Energy Consumption of Memory Micro-benchmarks with Clock Switching Enabled
- Figure 17 : Energy Consumption of Memory Micro-benchmarks with Clock-Switching Disabled

3.3 Discussion

Virtual addressing (turning on the MMU) does not incur any noticeable cost, in terms of energy or performance, when compared to physical addressing. The data collected with the MMU and instruction cache enabled is virtually identical to the data collected with only the instruction cache enabled for all benchmarks.

Clock Freq. (MHz)	Data Locality	Power (W)							
		Read				Write			
		IMWD	IMW	IM	I	IMWD	IMW	IM	I
59.0	In Cache	0.245	0.458	0.460	0.457	0.238	0.588	0.552	0.546
59.0	Out of Cache	0.443	0.473	0.475	0.474	0.585	0.588	0.552	0.546
73.7	In Cache	0.287	0.535	0.537	0.534	0.281	0.690	0.652	0.645
73.7	Out of Cache	0.500	0.554	0.557	0.554	0.687	0.690	0.652	0.645
88.5	In Cache	0.329	0.582	0.584	0.580	0.323	0.793	0.753	0.747
88.5	Out of Cache	0.547	0.602	0.604	0.602	0.790	0.793	0.753	0.747
103.2	In Cache	0.371	0.653	0.655	0.651	0.366	0.897	0.852	0.846
103.2	Out of Cache	0.602	0.676	0.677	0.676	0.893	0.897	0.852	0.846
118.0	In Cache	0.413	0.722	0.723	0.719	0.407	0.880	0.950	0.943
118.0	Out of Cache	0.655	0.748	0.750	0.746	0.878	0.880	0.947	0.943
132.7	In Cache	0.455	0.748	0.750	0.746	0.449	0.968	1.047	1.039
132.7	Out of Cache	0.695	0.775	0.776	0.774	0.965	0.968	1.044	1.039
147.5	In Cache	0.496	0.814	0.816	0.811	0.491	0.955	1.056	1.048
147.5	Out of Cache	0.690	0.844	0.845	0.843	0.950	0.955	1.056	1.048
162.2	In Cache	0.538	0.879	0.880	0.875	0.532	1.034	1.146	1.138
162.2	Out of Cache	0.698	0.911	0.911	0.909	1.031	1.034	1.142	1.138
176.9	In Cache	0.578	0.895	0.897	0.892	0.573	1.004	1.120	1.113
176.9	Out of Cache	0.730	0.927	0.926	0.925	1.000	1.004	1.116	1.113
191.7	In Cache	0.620	0.955	0.956	0.951	0.615	1.004	1.123	1.116
191.7	Out of Cache	0.771	0.991	0.990	0.987	1.000	1.004	1.119	1.116
206.4	In Cache	0.660	0.961	0.963	0.958	0.655	1.059	1.187	1.179
206.4	Out of Cache	0.762	0.997	0.995	0.994	1.055	1.059	1.183	1.179

Figure 9: Input Power Consumption of Memory Micro-benchmarks with Clock Switching Disabled

Clock Freq. (MHz)	Data Locality	Power (W)							
		Read				Write			
		IMWD	IMW	IM	I	IMWD	IMW	IM	I
59.0	In Cache	0.043	0.361	0.360	0.361	0.037	0.476	0.411	0.411
59.0	Out of Cache	0.329	0.379	0.379	0.378	0.478	0.476	0.411	0.411
73.7	In Cache	0.043	0.420	0.420	0.420	0.037	0.558	0.483	0.483
73.7	Out of Cache	0.364	0.442	0.442	0.442	0.560	0.558	0.483	0.483
88.5	In Cache	0.043	0.450	0.450	0.450	0.037	0.640	0.557	0.557
88.5	Out of Cache	0.391	0.473	0.473	0.473	0.643	0.640	0.557	0.557
103.2	In Cache	0.043	0.502	0.502	0.503	0.037	0.722	0.627	0.627
103.2	Out of Cache	0.425	0.529	0.529	0.529	0.725	0.722	0.629	0.627
118.0	In Cache	0.043	0.555	0.556	0.556	0.037	0.702	0.697	0.697
118.0	Out of Cache	0.458	0.585	0.585	0.585	0.705	0.702	0.697	0.697
132.7	In Cache	0.043	0.566	0.566	0.567	0.038	0.771	0.764	0.765
132.7	Out of Cache	0.479	0.597	0.597	0.597	0.774	0.771	0.767	0.765
147.5	In Cache	0.043	0.612	0.612	0.613	0.037	0.754	0.754	0.754
147.5	Out of Cache	0.469	0.646	0.646	0.646	0.756	0.754	0.755	0.754
162.2	In Cache	0.043	0.658	0.658	0.659	0.038	0.815	0.815	0.815
162.2	Out of Cache	0.470	0.695	0.695	0.695	0.818	0.816	0.817	0.817
176.9	In Cache	0.043	0.662	0.663	0.663	0.038	0.783	0.783	0.782
176.9	Out of Cache	0.486	0.698	0.699	0.698	0.785	0.783	0.785	0.784
191.7	In Cache	0.044	0.705	0.705	0.705	0.038	0.778	0.779	0.779
191.7	Out of Cache	0.509	0.743	0.744	0.744	0.780	0.778	0.779	0.779
206.4	In Cache	0.044	0.700	0.700	0.700	0.038	0.818	0.819	0.819
206.4	Out of Cache	0.497	0.738	0.739	0.739	0.820	0.818	0.819	0.819

Figure 10: Main (3.3V) Power Consumption of Memory Micro-benchmarks with Clock-Switching Enabled

Clock Freq. (MHz)	Data Locality	Power (W)							
		Read				Write			
		IMWD	IMW	IM	I	IMWD	IMW	IM	I
59.0	In Cache	0.043	0.328	0.325	0.324	0.037	0.476	0.396	0.397
59.0	Out of Cache	0.315	0.343	0.341	0.341	0.477	0.476	0.396	0.397
73.7	In Cache	0.043	0.380	0.378	0.377	0.037	0.557	0.466	0.466
73.7	Out of Cache	0.348	0.399	0.397	0.397	0.560	0.557	0.466	0.466
88.5	In Cache	0.043	0.412	0.409	0.409	0.037	0.640	0.537	0.537
88.5	Out of Cache	0.375	0.431	0.429	0.430	0.643	0.640	0.537	0.537
103.2	In Cache	0.043	0.459	0.457	0.456	0.037	0.722	0.605	0.606
103.2	Out of Cache	0.407	0.481	0.479	0.479	0.725	0.722	0.605	0.606
118.0	In Cache	0.043	0.505	0.503	0.502	0.037	0.702	0.673	0.673
118.0	Out of Cache	0.438	0.531	0.527	0.529	0.705	0.702	0.672	0.673
132.7	In Cache	0.044	0.521	0.519	0.518	0.037	0.770	0.738	0.739
132.7	Out of Cache	0.460	0.548	0.544	0.545	0.774	0.770	0.737	0.739
147.5	In Cache	0.044	0.565	0.563	0.561	0.037	0.753	0.741	0.741
147.5	Out of Cache	0.454	0.594	0.590	0.592	0.756	0.753	0.741	0.741
162.2	In Cache	0.044	0.606	0.605	0.603	0.037	0.814	0.801	0.802
162.2	Out of Cache	0.456	0.638	0.635	0.636	0.818	0.814	0.800	0.802
176.9	In Cache	0.044	0.615	0.614	0.612	0.037	0.782	0.775	0.776
176.9	Out of Cache	0.472	0.647	0.643	0.644	0.785	0.782	0.774	0.776
191.7	In Cache	0.044	0.654	0.652	0.651	0.037	0.777	0.776	0.777
191.7	Out of Cache	0.495	0.689	0.685	0.686	0.781	0.777	0.774	0.777
206.4	In Cache	0.044	0.654	0.652	0.651	0.037	0.818	0.816	0.817
206.4	Out of Cache	0.485	0.688	0.684	0.686	0.821	0.818	0.814	0.817

Figure 11: Main (3.3V) Power Consumption of Memory Micro-benchmarks with Clock Switching Disabled

Clock Freq. (MHz)	Data Locality	Power (W)							
		Read				Write			
		IMWD	IMW	IM	I	IMWD	IMW	IM	I
59.0	In Cache	0.176	0.073	0.074	0.074	0.178	0.130	0.080	0.079
59.0	Out of Cache	0.066	0.074	0.074	0.074	0.130	0.130	0.080	0.079
73.7	In Cache	0.215	0.088	0.088	0.088	0.218	0.158	0.096	0.095
73.7	Out of Cache	0.079	0.088	0.088	0.088	0.158	0.158	0.096	0.095
88.5	In Cache	0.255	0.095	0.095	0.095	0.258	0.186	0.112	0.110
88.5	Out of Cache	0.089	0.095	0.096	0.095	0.186	0.186	0.112	0.110
103.2	In Cache	0.294	0.108	0.108	0.107	0.297	0.214	0.128	0.126
103.2	Out of Cache	0.102	0.108	0.109	0.108	0.213	0.213	0.128	0.126
118.0	In Cache	0.333	0.120	0.121	0.119	0.336	0.239	0.144	0.141
118.0	Out of Cache	0.113	0.121	0.121	0.120	0.238	0.238	0.144	0.141
132.7	In Cache	0.371	0.125	0.126	0.124	0.375	0.267	0.159	0.156
132.7	Out of Cache	0.123	0.125	0.126	0.124	0.265	0.267	0.159	0.156
147.5	In Cache	0.410	0.137	0.138	0.136	0.413	0.292	0.161	0.158
147.5	Out of Cache	0.123	0.137	0.139	0.136	0.289	0.292	0.161	0.158
162.2	In Cache	0.448	0.149	0.150	0.148	0.452	0.319	0.175	0.172
162.2	Out of Cache	0.126	0.149	0.150	0.148	0.316	0.318	0.175	0.172
176.9	In Cache	0.485	0.152	0.152	0.150	0.489	0.344	0.175	0.171
176.9	Out of Cache	0.134	0.152	0.153	0.150	0.340	0.342	0.175	0.171
191.7	In Cache	0.523	0.163	0.164	0.161	0.526	0.368	0.175	0.172
191.7	Out of Cache	0.143	0.163	0.164	0.161	0.364	0.368	0.175	0.172
206.4	In Cache	0.560	0.166	0.166	0.164	0.564	0.395	0.189	0.184
206.4	Out of Cache	0.144	0.166	0.166	0.164	0.390	0.393	0.189	0.184

Figure 12: Core (1.5V) Power Consumption of Memory Micro-benchmarks with Clock-Switching Enabled

Clock Freq. (MHz)	Data Locality	Power (W)							
		Read				Write			
		IMWD	IMW	IM	I	IMWD	IMW	IM	I
59.0	In Cache	0.106	0.067	0.069	0.068	0.105	0.056	0.079	0.077
59.0	Out of Cache	0.068	0.067	0.068	0.068	0.056	0.056	0.079	0.077
73.7	In Cache	0.128	0.080	0.081	0.080	0.127	0.066	0.094	0.092
73.7	Out of Cache	0.079	0.080	0.081	0.080	0.065	0.066	0.094	0.092
88.5	In Cache	0.149	0.088	0.089	0.087	0.149	0.075	0.110	0.108
88.5	Out of Cache	0.090	0.088	0.089	0.088	0.074	0.075	0.110	0.108
103.2	In Cache	0.170	0.100	0.101	0.099	0.171	0.085	0.125	0.123
103.2	Out of Cache	0.102	0.100	0.101	0.099	0.084	0.085	0.125	0.123
118.0	In Cache	0.192	0.111	0.112	0.110	0.192	0.087	0.140	0.137
118.0	Out of Cache	0.113	0.111	0.112	0.110	0.087	0.087	0.139	0.137
132.7	In Cache	0.213	0.116	0.117	0.115	0.213	0.096	0.155	0.152
132.7	Out of Cache	0.122	0.116	0.117	0.116	0.095	0.096	0.154	0.152
147.5	In Cache	0.235	0.128	0.129	0.126	0.235	0.099	0.159	0.156
147.5	Out of Cache	0.123	0.127	0.129	0.127	0.097	0.099	0.159	0.156
162.2	In Cache	0.256	0.139	0.140	0.137	0.256	0.107	0.173	0.170
162.2	Out of Cache	0.126	0.139	0.140	0.137	0.105	0.107	0.172	0.170
176.9	In Cache	0.277	0.143	0.143	0.141	0.277	0.108	0.174	0.171
176.9	Out of Cache	0.134	0.143	0.143	0.141	0.107	0.108	0.173	0.171
191.7	In Cache	0.298	0.153	0.154	0.152	0.299	0.111	0.175	0.172
191.7	Out of Cache	0.143	0.153	0.154	0.151	0.110	0.111	0.174	0.172
206.4	In Cache	0.319	0.156	0.157	0.155	0.320	0.118	0.187	0.184
206.4	Out of Cache	0.144	0.156	0.157	0.154	0.117	0.118	0.186	0.184

Figure 13: Core (1.5V) Power Consumption of Memory Micro-benchmarks with Clock Switching Disabled

Enabling the write buffer incurs a significant energy penalty for the write benchmarks. With clock-switching enabled, the benchmark is performed slightly faster with the write buffer enabled, but power consumption is much higher. One possible explanation for this behavior may be that when the benchmark fills all available write buffer entries, the processor stalls but the core clock frequency does not drop to the speed of the bus. Indeed, when clock-switching is disabled, the write benchmark uses significantly less energy. In fact, with clock-switching disabled, enabling the write buffer reduces energy consumption.

Enabling the data cache provides the expected benefit when reads and write hit in the cache. When reads and writes miss in the cache, more energy is consumed with the data cache enabled. This is mostly due to the longer time needed to perform the benchmark. However, the out-of-cache benchmark exhibits pathologically bad cache behavior that may not occur under any realistic workload.

Clock Freq. (MHz)	Data Locality	Time (s)							
		Read				Write			
		IMWD	IMW	IM	I	IMWD	IMW	IM	I
59.0	In Cache	0.592	7.375	7.375	7.375	0.592	5.369	6.323	6.246
59.0	Out of Cache	18.425	7.368	7.368	7.368	5.327	5.369	6.315	6.315
73.7	In Cache	0.474	5.900	5.900	5.900	0.474	4.294	5.059	5.059
73.7	Out of Cache	14.750	5.894	5.894	5.894	4.260	4.294	5.050	5.050
88.5	In Cache	0.395	5.509	5.509	5.509	0.395	3.574	4.211	4.211
88.5	Out of Cache	12.848	5.503	5.503	5.503	3.546	3.574	4.205	4.205
103.2	In Cache	0.338	4.718	4.718	4.718	0.338	3.061	3.607	3.607
103.2	Out of Cache	10.992	4.714	4.714	4.714	3.037	3.061	3.602	3.602
118.0	In Cache	0.296	4.133	4.133	4.133	0.296	3.127	3.160	3.160
118.0	Out of Cache	9.630	4.130	4.130	4.130	3.102	3.127	3.156	3.155
132.7	In Cache	0.263	4.068	4.068	4.068	0.263	2.778	2.807	2.807
132.7	Out of Cache	8.927	4.065	4.065	4.065	2.756	2.778	2.803	2.803
147.5	In Cache	0.237	3.662	3.662	3.662	0.237	2.857	2.861	2.861
147.5	Out of Cache	9.374	3.659	3.659	3.659	2.835	2.857	2.857	2.857
162.2	In Cache	0.215	3.328	3.328	3.328	0.215	2.596	2.600	2.600
162.2	Out of Cache	9.431	3.325	3.325	3.325	2.576	2.596	2.597	2.597
176.9	In Cache	0.197	3.349	3.349	3.349	0.197	2.678	2.680	2.680
176.9	Out of Cache	8.928	3.347	3.347	3.347	2.657	2.678	2.678	2.678
191.7	In Cache	0.182	3.092	3.092	3.092	0.182	2.746	2.747	2.747
191.7	Out of Cache	8.241	3.090	3.090	3.090	2.725	2.746	2.746	2.746
206.4	In Cache	0.169	3.125	3.125	3.125	0.169	2.549	2.550	2.550
206.4	Out of Cache	8.607	3.123	3.123	3.123	2.530	2.549	2.550	2.550

Figure 14: Duration of Memory Micro-benchmarks with Clock-Switching Enabled

Clock Freq. (MHz)	Data Locality	Time (s)							
		Read				Write			
		IMWD	IMW	IM	I	IMWD	IMW	IM	I
59.0	In Cache	1.184	8.326	8.326	8.326	1.184	5.369	6.554	6.554
59.0	Out of Cache	19.299	8.308	8.308	8.308	5.335	5.369	6.535	6.535
73.7	In Cache	0.947	6.663	6.663	6.663	0.947	4.294	5.242	5.242
73.7	Out of Cache	15.438	6.649	6.649	6.649	4.266	4.294	5.226	5.226
88.5	In Cache	0.789	6.142	6.142	6.142	0.789	3.574	4.364	4.364
88.5	Out of Cache	13.426	6.132	6.132	6.132	3.551	3.574	4.353	4.353
103.2	In Cache	0.677	5.262	5.262	5.262	0.677	3.061	3.738	3.738
103.2	Out of Cache	11.493	5.255	5.255	5.255	3.042	3.061	3.728	3.728
118.0	In Cache	0.592	4.611	4.611	4.611	0.592	3.127	3.275	3.275
118.0	Out of Cache	10.076	4.601	4.601	4.601	3.106	3.127	3.267	3.267
132.7	In Cache	0.526	4.493	4.493	4.493	0.526	2.778	2.909	2.909
132.7	Out of Cache	9.322	4.485	4.485	4.485	2.760	2.778	2.902	2.902
147.5	In Cache	0.474	4.043	4.043	4.043	0.474	2.857	2.909	2.909
147.5	Out of Cache	9.729	4.037	4.037	4.037	2.838	2.857	2.902	2.902
162.2	In Cache	0.431	3.675	3.675	3.675	0.431	2.596	2.643	2.643
162.2	Out of Cache	9.751	3.669	3.669	3.669	2.579	2.596	2.637	2.637
176.9	In Cache	0.395	3.670	3.667	3.667	0.395	2.678	2.702	2.702
176.9	Out of Cache	9.222	3.662	3.662	3.662	2.659	2.678	2.697	2.697
191.7	In Cache	0.364	3.385	3.385	3.385	0.364	2.746	2.752	2.752
191.7	Out of Cache	8.513	3.380	3.380	3.380	2.727	2.746	2.747	2.747
206.4	In Cache	0.338	3.398	3.398	3.398	0.338	2.549	2.554	2.554
206.4	Out of Cache	8.859	3.393	3.393	3.393	2.532	2.549	2.550	2.550

Figure 15: Duration of Memory Micro-benchmarks with Clock Switching Disabled

Clock Freq. (MHz)	Data Locality	Energy (J)							
		Read				Write			
		IMWD	IMW	IM	I	IMWD	IMW	IM	I
59.0	In Cache	0.228	3.710	3.717	3.717	0.227	3.919	3.591	3.535
59.0	Out of Cache	8.439	3.846	3.853	3.853	3.894	3.919	3.587	3.574
73.7	In Cache	0.219	3.475	3.487	3.487	0.219	3.727	3.395	3.384
73.7	Out of Cache	7.641	3.613	3.619	3.607	3.698	3.727	3.389	3.378
88.5	In Cache	0.213	3.498	3.504	3.443	0.213	3.595	3.272	3.259
88.5	Out of Cache	7.259	3.621	3.632	3.621	3.567	3.595	3.267	3.255
103.2	In Cache	0.208	3.364	3.369	3.359	0.207	3.499	3.171	3.160
103.2	Out of Cache	6.860	3.488	3.498	3.484	3.468	3.499	3.166	3.155
118.0	In Cache	0.204	3.269	3.273	3.261	0.204	3.659	3.100	3.084
118.0	Out of Cache	6.548	3.391	3.403	3.387	3.623	3.659	3.096	3.080
132.7	In Cache	0.201	3.299	3.307	3.291	0.200	3.589	3.034	3.018
132.7	Out of Cache	6.419	3.427	3.431	3.415	3.555	3.589	3.030	3.013
147.5	In Cache	0.198	3.226	3.234	3.219	0.198	3.774	3.070	3.050
147.5	Out of Cache	6.646	3.352	3.359	3.341	3.737	3.774	3.066	3.045
162.2	In Cache	0.195	3.165	3.172	3.155	0.195	3.728	3.026	3.008
162.2	Out of Cache	6.743	3.288	3.298	3.278	3.689	3.724	3.023	3.005
176.9	In Cache	0.193	3.218	3.225	3.208	0.193	3.878	3.028	3.007
176.9	Out of Cache	6.660	3.340	3.347	3.330	3.834	3.878	3.026	3.005
191.7	In Cache	0.191	3.169	3.175	3.163	0.191	4.089	3.096	3.077
191.7	Out of Cache	6.502	3.291	3.300	3.285	4.044	4.089	3.095	3.076
206.4	In Cache	0.191	3.203	3.209	3.197	0.189	4.025	3.037	3.017
206.4	Out of Cache	6.688	3.326	3.335	3.320	3.977	4.026	3.037	3.017

Figure 16: Energy Consumption of Memory Micro-benchmarks with Clock Switching Enabled

Clock Freq. (MHz)	Data Locality	Energy (J)							
		Read				Write			
		IMWD	IMW	IM	I	IMWD	IMW	IM	I
59.0	In Cache	0.290	3.813	3.830	3.805	0.282	3.157	3.618	3.578
59.0	Out of Cache	8.549	3.930	3.946	3.938	3.121	3.157	3.607	3.568
73.7	In Cache	0.272	3.565	3.578	3.558	0.266	2.963	3.418	3.381
73.7	Out of Cache	7.719	3.684	3.703	3.684	2.931	2.963	3.407	3.371
88.5	In Cache	0.260	3.575	3.587	3.562	0.255	2.834	3.286	3.260
88.5	Out of Cache	7.344	3.691	3.704	3.691	2.805	2.834	3.278	3.252
103.2	In Cache	0.244	3.436	3.447	3.426	0.248	2.746	3.185	3.162
103.2	Out of Cache	6.919	3.552	3.558	3.552	2.717	2.746	3.176	3.154
118.0	In Cache	0.239	3.329	3.334	3.315	0.241	2.752	3.111	3.088
118.0	Out of Cache	6.600	3.442	3.451	3.432	2.727	2.752	3.094	3.081
132.7	In Cache	0.235	3.361	3.370	3.352	0.236	2.689	3.046	3.022
132.7	Out of Cache	6.479	3.476	3.480	3.471	2.663	2.689	2.030	3.015
147.5	In Cache	0.232	3.291	3.299	3.279	0.233	2.728	3.072	3.049
147.5	Out of Cache	6.713	3.407	3.411	3.403	2.696	2.728	3.065	3.041
162.2	In Cache	0.228	3.230	3.234	3.216	0.229	2.684	3.029	3.008
162.2	Out of Cache	6.806	3.342	3.342	3.335	2.659	2.684	3.011	3.001
176.9	In Cache	0.226	3.285	3.292	3.274	0.226	2.689	3.026	3.007
176.9	Out of Cache	6.732	3.395	3.391	3.387	2.659	2.689	3.010	3.002
191.7	In Cache	0.226	3.233	3.236	3.219	0.224	2.757	3.090	3.071
191.7	Out of Cache	6.564	3.350	3.346	3.336	2.727	2.757	3.074	3.066
206.4	In Cache	0.223	3.265	3.234	3.255	0.221	2.699	3.032	3.011
206.4	Out of Cache	6.751	3.383	3.376	3.373	2.672	2.699	3.017	3.006

Figure 17: Energy Consumption of Memory Micro-benchmarks with Clock-Switching Disabled

Since enabling the data cache requires that the write-buffer also be enabled, the data cache experiments exhibit some of the poor write-benchmark performance noticed previously. When writes miss in the cache, disabling clock-switching reduces energy consumption. However, when writes hit in the cache, disabling clock-switching incurs an energy penalty. This behavior suggests that it may be beneficial to disable clock-switching before performing a large block of writes that are known to have poor data locality. This idea is examined further in the next section, which benchmarks a large data copy.

Clock Freq. (MHz)	Power (W)		
	Switching	No Switching	Ratio
59.0	0.704	0.569	0.808
73.7	0.832	0.665	0.799
88.5	0.956	0.760	0.795
103.2	1.083	0.856	0.790
118.0	1.106	0.865	0.782
132.7	1.214	0.948	0.781
147.5	1.237	0.952	0.770
162.2	1.331	1.022	0.768
176.9	1.347	1.014	0.753
191.7	1.391	1.018	0.732
206.4	1.463	1.068	0.730

Figure 18: Input Power Consumption of Copy Micro-benchmark

4 Copy Micro-benchmark

4.1 Description

This micro-benchmark examines the effect of disabling clock-switching while copying a large block of data. The benchmark copies a 128 KB block of data from one memory location to another using a copy implementation virtually identical to the Linux kernel `memcpy` implementation. The benchmark performs this copy 1000 times.

Two scenarios were measured, one in which clock-switching was enabled and the other in which clock-switching was disabled. In both cases, the instruction cache, MMU, data cache, and write-buffer are all enabled.

4.2 Data

- Figure 18: Input Power Consumption of Copy Micro-benchmark
- Figure 19: Main (3.3 V) Power Consumption of Copy Micro-benchmark
- Figure 20: Core (1.5 V) Power Consumption of Copy Micro-benchmark
- Figure 21: Duration of Copy Micro-benchmark
- Figure 22: Energy Consumption of Copy Micro-benchmark

4.3 Discussion

By disabling clock-switching, the total energy used to copy 128 KB of data can be reduced by almost 27%. At the same time, copy performance decreases by less than 0.3%. This indicates

Clock Freq. (MHz)	Power (W)	
	Switching	No Switching
59.0	0.461	0.430
73.7	0.535	0.498
88.5	0.606	0.564
103.2	0.678	0.631
118.0	0.659	0.632
132.7	0.715	0.688
147.5	0.702	0.687
162.2	0.750	0.735
176.9	0.726	0.723
191.7	0.726	0.723
206.4	0.758	0.755

Figure 19: Main (3.3 V) Power Consumption of Copy Micro-benchmark

Clock Freq. (MHz)	Power (W)	
	Switching	No Switching
59.0	0.126	0.072
73.7	0.154	0.086
88.5	0.181	0.100
103.2	0.208	0.115
118.0	0.231	0.119
132.7	0.258	0.132
147.5	0.277	0.134
162.2	0.301	0.145
176.9	0.322	0.148
191.7	0.346	0.150
206.4	0.367	0.159

Figure 20: Core (1.5 V) Power Consumption of Copy Micro-benchmark

Clock Freq. (MHz)	Time (s)		
	Switching	No Switching	Ratio
59.0	29.645	31.731	1.070
73.7	23.705	25.373	1.070
88.5	19.827	21.212	1.070
103.2	16.982	18.178	1.070
118.0	17.171	17.865	1.040
132.7	15.316	15.932	1.040
147.5	15.794	16.127	1.021
162.2	14.504	14.806	1.021
176.9	14.877	14.923	1.003
191.7	15.106	15.149	1.003
206.4	14.182	14.222	1.003

Figure 21: Duration of Copy Micro-benchmark

Clock Freq. (MHz)	Energy (J)		
	Switching	No Switching	Ratio
59.0	20.870	18.055	0.865
73.7	19.723	16.873	0.856
88.5	18.955	16.121	0.851
103.2	18.392	15.560	0.846
118.0	18.991	15.453	0.814
132.7	18.594	15.104	0.813
147.5	19.537	15.353	0.786
162.2	19.305	15.132	0.784
176.9	20.039	15.132	0.755
191.7	21.012	15.422	0.734
206.4	20.748	15.189	0.732

Figure 22: Energy Consumption of Copy Micro-benchmark

that energy savings may be achieved by inserting additional logic in common routines such as `memcpy`, `memset`, `bcopy`, and `bzero` to disable clock-switching if a large number of writes are to be performed. Further exploration is needed to develop appropriate heuristics to determine when disabling clock-switching is beneficial.

5 Flash Micro-benchmarks

5.1 Description

These micro-benchmarks examine energy consumption when reading or writing flash memory. The read benchmark executes a large number of load instructions inside of a tight loop that has been unrolled sixteen times. It reads the same amount of data as the DRAM read benchmark (100 MB), so that the results of the two benchmarks can be compared. Two read scenarios are examined, one in which each load hits in the data cache (which is enabled), and one in which each load misses in the data cache. Read performance is shown for different clock frequencies, as well as with clock switching enabled and disabled.

The write benchmark programs a 1K region of flash 50 times. The amount of data written is significantly less than for both the flash read benchmark and also the DRAM write benchmark. Therefore, the results of these benchmarks should not be directly compared. Two write modes are examined, one in which the data being written is merged with the existing data stored in the flash memory, and one in which the data in flash is ignored.

5.2 Data

- Figure 23: Input Power Consumption of Flash Micro-benchmarks
- Figure 24: Main (3.3V) Power Consumption of Flash Micro-benchmarks
- Figure 25: Core (1.5V) Power Consumption of Flash Micro-benchmarks
- Figure 26: Duration of Flash Micro-benchmarks
- Figure 27: Energy Consumption of Flash Micro-benchmarks

5.3 Discussion

When data accesses miss in the data cache, reducing the clock frequency has a small benefit when reading data from flash. Reading data from flash consumes less power than reading data from DRAM, but executes two to three times slower. Therefore, reading from flash consumes more energy (approximately 18%) than reading from DRAM. This suggests that data in flash which is read fairly often could be copied to DRAM to save energy. However, data that is read only a few times may be best left in flash.

Writing flash is extremely slow compared to writing DRAM. Although clock frequency does not appear to affect energy usage, disabling clock-switching while writing flash yields a small energy benefit.

Clock Freq. (MHz)	Power (W)							
	Read - In Cache		Read - Out of Cache		Write - Merge		Write - Ignore	
	Switching	No Switching	Switching	No Switching	Switching	No Switching	Switching	No Switching
59.0	0.396	0.249	0.318	0.313	0.561	0.511	0.559	0.504
73.7	0.476	0.294	0.322	0.318	0.564	0.513	0.555	0.507
88.5	0.555	0.338	0.326	0.323	0.560	0.511	0.556	0.508
103.2	0.634	0.382	0.371	0.367	0.558	0.515	0.557	0.508
118.0	0.711	0.425	0.369	0.367	0.561	0.509	0.560	0.510
132.7	0.788	0.469	0.372	0.370	0.562	0.514	0.553	0.502
147.5	0.868	0.512	0.406	0.403	0.567	0.508	0.560	0.511
162.2	0.940	0.555	0.405	0.404	0.575	0.513	0.560	0.507
176.9	1.020	0.597	0.407	0.405	0.561	0.503	0.558	0.507
191.7	1.089	0.640	0.435	0.434	0.561	0.508	0.559	0.508
206.4	1.162	0.682	0.435	0.434	0.567	0.509	0.561	0.507

Figure 23: Input Power Consumption of Flash Micro-benchmarks

Clock Freq. (MHz)	Power (W)							
	Read - In Cache		Read - Out of Cache		Write - Merge		Write - Ignore	
	Switching	No Switching	Switching	No Switching	Switching	No Switching	Switching	No Switching
59.0	0.043	0.041	0.207	0.200	0.225	0.210	0.226	0.206
73.7	0.043	0.041	0.205	0.198	0.222	0.214	0.222	0.207
88.5	0.042	0.041	0.203	0.198	0.224	0.213	0.221	0.207
103.2	0.042	0.041	0.231	0.225	0.227	0.209	0.223	0.205
118.0	0.032	0.041	0.225	0.220	0.224	0.211	0.220	0.208
132.7	0.042	0.041	0.222	0.217	0.223	0.212	0.221	0.208
147.5	0.042	0.041	0.242	0.237	0.221	0.208	0.219	0.202
162.2	0.042	0.045	0.237	0.232	0.223	0.203	0.220	0.208
176.9	0.042	0.041	0.233	0.229	0.222	0.212	0.220	0.207
191.7	0.042	0.041	0.249	0.224	0.220	0.206	0.219	0.212
206.4	0.042	0.041	0.244	0.240	0.221	0.213	0.218	0.210

Figure 24: Main (3.3V) Power Consumption of Flash Micro-benchmarks

Clock Freq. (MHz)	Power (W)							
	Read - In Cache		Read - Out of Cache		Write - Merge		Write - Ignore	
	Switching	No Switching	Switching	No Switching	Switching	No Switching	Switching	No Switching
59.0	0.184	0.108	0.059	0.059	0.176	0.157	0.173	0.156
73.7	0.225	0.131	0.062	0.062	0.176	0.157	0.174	0.156
88.5	0.266	0.153	0.065	0.065	0.176	0.157	0.174	0.156
103.2	0.307	0.176	0.074	0.074	0.176	0.157	0.174	0.156
118.0	0.347	0.198	0.076	0.076	0.175	0.157	0.174	0.156
132.7	0.387	0.220	0.079	0.079	0.174	0.156	0.174	0.156
147.5	0.427	0.243	0.086	0.086	0.174	0.158	0.174	0.155
162.2	0.467	0.266	0.089	0.089	0.175	0.156	0.174	0.155
176.9	0.506	0.287	0.091	0.091	0.175	0.157	0.174	0.155
191.7	0.546	0.309	0.097	0.098	0.174	0.158	0.174	0.155
206.4	0.584	0.331	0.100	0.100	0.174	0.157	0.174	0.155

Figure 25: Core (1.5V) Power Consumption of Flash Micro-benchmarks

Clock Freq. (MHz)	Time (s)							
	Read - In Cache		Read - Out of Cache		Write - Merge		Write - Ignore	
	Switching	No Switching	Switching	No Switching	Switching	No Switching	Switching	No Switching
59.0	0.592	1.184	25.185	26.077	18.605	17.879	16.994	16.556
73.7	0.474	0.947	25.496	26.183	18.076	17.621	16.603	16.438
88.5	0.395	0.789	25.696	26.301	17.667	17.697	16.423	16.342
103.2	0.338	0.677	21.989	22.524	17.629	17.542	16.621	16.323
118.0	0.296	0.592	22.594	23.060	17.935	17.658	16.483	16.354
132.7	0.263	0.526	23.064	23.453	18.058	17.531	16.472	16.593
147.5	0.237	0.474	20.718	21.109	17.737	17.543	16.333	17.582
162.2	0.215	0.431	21.302	21.622	17.633	17.370	16.430	16.575
176.9	0.197	0.395	21.742	22.035	17.430	17.353	16.376	16.548
191.7	0.182	0.364	20.074	20.348	17.399	17.418	16.494	16.322
206.4	0.169	0.338	20.545	20.797	17.531	17.484	16.287	16.243

Figure 26: Duration of Flash Micro-benchmarks

Clock Freq. (MHz)	Energy (J)							
	Read - In Cache		Read - Out of Cache		Write - Merge		Write - Ignore	
	Switching	No Switching	Switching	No Switching	Switching	No Switching	Switching	No Switching
59.0	0.234	0.295	8.009	8.162	10.437	9.136	9.500	8.344
73.7	0.226	0.278	8.210	8.326	10.195	9.040	9.215	8.334
88.5	0.219	0.267	8.377	8.495	9.894	9.043	9.131	8.302
103.2	0.214	0.259	8.158	8.266	9.837	9.034	9.258	8.292
118.0	0.210	0.252	8.337	8.463	10.062	8.988	9.230	8.341
132.7	0.207	0.247	8.580	8.678	10.149	9.011	9.109	8.330
147.5	0.206	0.243	8.412	8.507	10.057	8.912	9.146	8.984
162.2	0.202	0.239	8.627	8.735	10.139	8.911	9.201	8.404
176.9	0.201	0.236	8.849	8.924	9.778	8.729	9.138	8.390
191.7	0.198	0.233	8.732	8.831	9.761	8.848	9.220	8.292
206.4	0.196	0.231	8.937	9.026	9.940	8.899	9.137	8.235

Figure 27: Energy Consumption of Flash Micro-benchmarks

Clock Rate (MHz)	Wait Type	Power (W)		
		Disabled	Auto	Enabled
59.0	Idle	0.092	0.136	0.137
132.7	Idle	0.126	0.170	0.171
206.4	Idle	0.160	0.205	0.205
59.0	Wait	0.224	0.268	0.269
132.7	Wait	0.413	0.457	0.458
206.4	Wait	0.598	0.642	0.642

Figure 28: Input Power Consumption for UART Mode Micro-benchmarks

6 UART Mode Micro-benchmarks

6.1 Description

These micro-benchmarks examine the effect of the UART mode on the Itsy's power usage. The next set of micro-benchmarks examine power usage while the UART is transmitting data.

The UART mode benchmarks are executed with all configurable hardware components disabled, with the exception of the DRAM banks, static memory, and instruction cache. For each benchmark, power usage was measured while the SA-1100 was in idle mode, and while the processor was executing a busy-wait loop. The three UART modes measured are:

- Disabled - Note that this benchmark is identical to the idle and busy-wait clock-rate benchmarks. It is included here for reference.
- Auto - measures power usage while the UART is in auto-shutdown mode. In this mode, the UART is enabled while it is connected to another serial port (e.g, that of a workstation), and disabled otherwise. No data is transmitted during this benchmark, but the serial port of the UART is connected to the serial port of a workstation.
- Enabled - measures power usage while the UART is enabled. No data is transmitted during this benchmark, but the Itsy is connected to the serial port of a workstation.

6.2 Data

- Figure 28: Input Power Consumption for UART Mode Micro-benchmarks
- Figure 29: Main (3.3V) Power Consumption for UART Mode Micro-benchmarks
- Figure 30: Core (1.5V) Power Consumption for UART Mode Micro-benchmarks

Clock Rate (MHz)	Wait Type	Power (W)		
		Disabled	Auto	Enabled
59.0	Idle	0.035	0.079	0.079
132.7	Idle	0.035	0.079	0.080
206.4	Idle	0.036	0.080	0.081
59.0	Wait	0.038	0.082	0.083
132.7	Wait	0.039	0.083	0.083
206.4	Wait	0.039	0.083	0.084

Figure 29: Main (3.3V) Power Consumption for UART Mode Micro-benchmarks

Clock Rate (MHz)	Wait Type	Power (W)		
		Disabled	Auto	Enabled
59.0	Idle	0.030	0.030	0.030
132.7	Idle	0.047	0.047	0.047
206.4	Idle	0.064	0.065	0.065
59.0	Wait	0.096	0.096	0.096
132.7	Wait	0.193	0.193	0.193
206.4	Wait	0.288	0.288	0.288

Figure 30: Core (1.5V) Power Consumption for UART Mode Micro-benchmarks

6.3 Discussion

These results show that the energy costs of enabling the UART is fairly constant at approximately 44 mW. If auto-shutdown mode is employed and the UART is connected to a serial port, the 44mW cost is incurred even when no data is being transmitted. It would be interesting to see if the UART uses any energy in auto-shutdown mode when it is not connected to a serial port.

Clock Rate (MHz)	Power (W)				
	9600	19200	38400	57600	115200
59.0	0.142	0.149	0.162	0.175	0.215
132.7	0.175	0.183	0.195	0.206	0.243
206.4	0.209	0.217	0.228	0.242	0.276

Figure 31: Input Power Consumption for UART Rate Micro-benchmarks

Clock Rate (MHz)	Power (W)				
	9600	19200	38400	57600	115200
59.0	0.081	0.085	0.095	0.104	0.134
132.7	0.081	0.085	0.093	0.102	0.128
206.4	0.081	0.085	0.093	0.101	0.127

Figure 32: Main (3.3V) Power Consumption for UART Rate Micro-benchmarks

7 UART Rate Micro-benchmarks

7.1 Description

This micro-benchmark measures the effect of using different data rates to transmit data using the Itsy UART to/from a workstation over a serial connection. The benchmark transmits 100,000 bytes of data from the Itsy to the host computer. All supported data rates between 9,600 and 115,200 baud were measured for three different clock frequencies. All other configurable hardware components are disabled, with the exception of the DRAM banks, static memory, and the instruction cache.

7.2 Data

- Figure 31: Input Power Consumption for UART Rate Micro-benchmarks
- Figure 32: Main (3.3V) Power Consumption for UART Rate Micro-benchmarks
- Figure 33: Core (1.5V) Power Consumption for UART Rate Micro-benchmarks
- Figure 34: Duration of UART Rate Micro-benchmarks
- Figure 35: Energy Consumption of UART Rate Micro-benchmarks

7.3 Discussion

No energy benefit is achieved by reducing the UART transmission rate (in fact, the opposite is true since the decrease in power consumption does not offset the increased transmission time). However,

Clock Rate (MHz)	Power (W)				
	9600	19200	38400	57600	115200
59.0	0.032	0.033	0.035	0.037	0.042
132.7	0.049	0.050	0.052	0.054	0.059
206.4	0.066	0.067	0.069	0.071	0.076

Figure 33: Core (1.5V) Power Consumption for UART Rate Micro-benchmarks

Clock Rate (MHz)	Duration (s)				
	9600	19200	38400	57600	115200
59.0	104.167	52.083	26.042	17.361	8.681
132.7	104.167	52.083	26.042	17.361	8.681
206.4	104.167	52.083	26.042	17.361	8.681

Figure 34: Duration of UART Rate Micro-benchmarks

Clock Rate (MHz)	Duration (s)				
	9600	19200	38400	57600	115200
59.0	14.791	7.760	4.219	3.038	1.866
132.7	18.229	9.531	5.078	3.576	2.109
206.4	21.771	11.302	5.938	4.201	2.396

Figure 35: Energy Consumption of UART Rate Micro-benchmarks

reducing the clock frequency before beginning transmission can significantly reduce energy usage. This may be related to the results of the idle mode benchmark discussed previously, since the Itsy is placed in idle mode when it is not transmitting or receiving data. It may be that a solution that changes the clock frequency before entering idle mode could also help reduce energy consumption when the UART is transmitting data.

Clock Rate (MHz)	Wait Type	Power (W)				
		Disabled	Enabled		Auxiliary	
			Grey-Scale	Astronaut	Grey-Scale	Astronaut
59.0	Idle	0.094	0.135	0.146	0.119	0.115
132.7	Idle	0.128	0.164	0.175	0.153	0.149
206.4	Idle	0.162	0.198	0.210	0.187	0.184
59.0	Wait	0.227	0.263	0.274	0.247	0.247
132.7	Wait	0.416	0.447	0.459	0.437	0.438
206.4	Wait	0.604	0.632	0.642	0.626	0.622

Figure 36: Input Power Consumption for LCD Micro-benchmarks

8 LCD Micro-benchmarks

8.1 Description

These micro-benchmarks examine the effect of the LCD display power usage. Note that the Itsy uses a reflective, passive matrix display with no back light. The benchmarks measure power usage for both the main and auxiliary LCD controllers. Where applicable, the power used to display multiple images is measured. Each benchmark was performed with the SA-1100 in idle mode, and while executing a busy-wait loop. Also, three different clock-rates were used.

Unless otherwise noted, all configurable hardware components are disabled, with the exception of the DRAM banks, flash memory, and the instruction cache.

- Disabled - measures power usage while both the main and auxiliary controllers are disabled. Note that this is identical to the idle and busy-wait clock-rate benchmarks.
- Auxiliary - measures power usage while the auxiliary LCD controller is used to display an image in black and white. Power usage is measured for the standard grey-scale and astronaut images.
- Enabled - measures power usage while the main LCD controller is enabled. Power usage is measured for the standard grey-scale and astronaut images.

8.2 Data

- Figure 36: Input Power Consumption for LCD Micro-benchmarks
- Figure 37: Main (3.3V) Consumption for LCD Micro-benchmarks
- Figure 38: Core (1.5V) Power Consumption for LCD Micro-benchmarks

Clock Rate (MHz)	Wait Type	Power (W)				
		Disabled	Enabled		Auxiliary	
			Grey-Scale	Astronaut	Grey-Scale	Astronaut
59.0	Idle	0.034	0.071	0.081	0.058	0.055
132.7	Idle	0.034	0.066	0.077	0.059	0.055
206.4	Idle	0.035	0.066	0.077	0.059	0.056
59.0	Wait	0.037	0.071	0.081	0.057	0.057
132.7	Wait	0.037	0.065	0.076	0.057	0.059
206.4	Wait	0.040	0.067	0.077	0.062	0.058

Figure 37: Main (3.3V) Consumption for LCD Micro-benchmarks

Clock Rate (MHz)	Wait Type	Power (W)				
		Disabled	Enabled		Auxiliary	
			Grey-Scale	Astronaut	Grey-Scale	Astronaut
59.0	Idle	0.031	0.033	0.033	0.031	0.031
132.7	Idle	0.048	0.050	0.050	0.048	0.048
206.4	Idle	0.065	0.068	0.068	0.065	0.065
59.0	Wait	0.097	0.098	0.098	0.097	0.097
132.7	Wait	0.193	0.195	0.195	0.194	0.194
206.4	Wait	0.289	0.290	0.290	0.289	0.289

Figure 38: Core (1.5V) Power Consumption for LCD Micro-benchmarks

8.3 Discussion

There appears to be considerable variation in the energy consumption of the LCD controllers. When the SA-1100 is in idle mode, enabling the main LCD controller consumes an additional 36-41 mW when the grey-scale image is displayed and an additional 47-52 mW when the astronaut image is displayed. When a busy-wait loop is executed, the LCD controller uses an additional 28-36 mW when the grey-scale image is displayed and an additional 38-47 mW when the astronaut image is displayed.

The auxiliary LCD controller uses a surprising amount of power. In idle mode, the auxiliary controller uses 25 mW to display the grey-scale image and 21-22 mW to display the astronaut image. During a busy-wait, the auxiliary controller uses 20-22 mW to display the grey-scale image and 18-22 mW to display the astronaut image.

9 Cache Flush Micro-benchmarks

9.1 Description

This set of micro-benchmarks measure the cost of flushing data from the instruction and data caches. These measurements include both the cost of the actual flush operation, as well as the additional cost necessary to reload data into the cache. For the data cache, it is also necessary to write possibly dirty data back to memory before the flush is performed, and this cost is also included in the measurements.

The cost of flushing the cache will depend on the usage patterns of the particular application performing the flush. These benchmarks are structured to assume that most flushed data will need to be reloaded. Therefore, they are a worse-case scenario for the cost of flushing the cache. Applications that do not reload flushed data may see a considerably smaller energy penalty. The three cache flush operations examined are:

- Instruction Cache Flush - This benchmark flushes the instruction cache, then reloads approximately 8K of instructions into the cache. This scenario is compared with a warm-cache scenario in which the 8K of instructions are executed in a loop without flushing the cache.
- Data Cache Flush - This benchmark writes the contents of the data cache to memory (which is necessary to write back any dirty cache blocks), invalidates all blocks in the data cache, and then reloads the cache by reading data from memory. This scenario is compared with a warm-cache scenario in which the cache is not flushed.
- Data Block Flush - This benchmark writes a word back to memory, invalidates the data cache block, and reloads it from memory. Like the previous benchmarks, the cost of the cache flush is measured by comparison with a scenario in which the flush is not performed.

Each benchmark measures the time to perform the actual flush (including the time needed to write dirty data back to memory). The benchmarks also measure the cost of flushing the cache by comparing a cold-cache scenario (in which the cache is flushed) with an equivalent warm-cache scenario (in which the cache is not flushed).

9.2 Data

- Figure 39: Cost of Flushing Data and Instruction Caches

9.3 Discussion

The cost of an instruction cache flush is very application-dependent, since the actual flush takes approximately 1 μs., and consequently consumes only a small amount of energy. A potentially greater cost in both time and power occurs when instruction data must be reloaded. As the benchmark shows, in a worse-case scenario, an instruction cache flush incurs a performance penalty of 79 μs. and 48 μJ.

Benchmark	Flush Time (μs)	Time (μs)		Power (mW)		Energy (μJ)	
		Warm	Cold	Warm	Cold	Warm	Cold
Instruction Cache Flush	1	129	208	804	730	104	152
Data Cache Flush	20	51	457	950	768	48	351
Data Line Flush	<1	0.019	0.068	902	827	0.017	0.056

Figure 39: Cost of Flushing Data and Instruction Caches

The cost of a data cache flush is also somewhat application-dependent. It takes approximately 20 μs. to clean and flush the cache. However, reloading the cache can be expensive. In a worse-case scenario, this incurs a penalty of 493 μs. and 303 μJ.

Flushing a line from the data cache is very quick, and consequently incurs little penalty (0.039 μJ), even if that line is immediately reread from memory.

A Memory Access Times and Bandwidths

This appendix presents the DRAM memory access times and bandwidths supported by the Itsy Pocket Computer Architecture, as a function of the bus clock frequency. This data is valid for version 1.5, version 2.1, and version 2.2 of the Itsy Pocket Computer.

Table 1 gives the data for 50-nano-second EDO DRAMs, while Table 2 gives the data for 45-nano-second EDO DRAMs. Note that the tables show all possible frequencies of the SA-1100, even those beyond specifications.

Memory settings and access speed are different if all the DRAM is on the mother-board than if there is some DRAM on a memory expansion daughter-card. Note that in the latter case, access to the mother-board DRAM banks are as slow as to the daughter-card banks (i.e., all banks are accessed at the speed of the slowest one).

Access time and bandwidth are shown both for single-word accesses and for 8-word burst accesses (cache line fill).

	DRAM on Mother-board only				DRAM on Daughter-Card			
	1 x 32 bit		8 x 32 bit		1 x 32 bit		8 x 32 bit	
Freq. [MHz]	Time [ns]	Bandw. [MB/s]	Time [ns]	Bandw. [MB/s]	Time [ns]	Bandw. [MB/s]	Time [ns]	Bandw. [MB/s]
59.0	152.6	26.2	627.3	51.0	186.5	21.4	661.2	48.4
73.7	149.2	26.8	529.0	60.5	149.2	26.8	529.0	60.5
88.5	124.3	32.2	440.8	72.6	124.3	32.2	440.8	72.6
103.2	106.6	37.5	377.8	84.7	106.6	37.5	377.8	84.7
118.0	93.2	42.9	330.6	96.8	110.2	36.3	347.6	92.1
132.7	98.0	40.8	308.9	104.0	105.5	37.9	316.5	101.0
147.5	94.9	42.1	284.8	112.0	94.9	42.1	332.3	96.3
162.2	92.5	43.3	308.3	104.0	92.5	43.3	308.3	104.0
176.9	90.4	44.2	288.2	111.0	101.7	39.3	339.1	94.4
191.7	88.7	45.1	271.3	118.0	99.1	40.4	318.2	101.0
206.4	92.0	43.5	295.5	108.0	96.9	41.3	334.2	95.7
221.2	90.4	44.2	280.3	114.0	90.4	44.2	312.0	103.0
235.9	89.0	44.9	296.7	108.0	97.5	41.0	334.8	95.6
265.4	90.4	44.2	301.4	106.0	94.2	42.5	331.5	96.5
294.9	88.2	45.4	301.8	106.0	94.9	42.1	332.3	96.3
309.7	87.2	45.9	290.6	110.0	93.7	42.7	319.7	100.0
324.4	89.4	44.7	305.2	105.0	92.5	43.3	329.8	97.0
353.9	87.6	45.7	285.4	112.0	98.9	40.4	336.3	95.2
383.4	86.1	46.5	305.2	105.0	91.3	43.8	346.9	92.2

Table 1: 50-ns EDO DRAMs

	DRAM on Mother-board only				DRAM on Daughter-Card			
	1 x 32 bit		8 x 32 bit		1 x 32 bit		8 x 32 bit	
Freq. [MHz]	Time [ns]	Bandw. [MB/s]	Time [ns]	Bandw. [MB/s]	Time [ns]	Bandw. [MB/s]	Time [ns]	Bandw. [MB/s]
59.0	152.6	26.2	627.3	51.0	152.6	26.2	627.3	51.0
73.7	122.1	32.8	501.8	63.8	149.2	26.8	529.0	60.5
88.5	124.3	32.2	440.8	72.6	124.3	32.2	440.8	72.6
103.2	106.6	37.5	377.8	84.7	106.6	37.5	377.8	84.7
118.0	93.2	42.9	330.6	96.8	93.2	42.9	330.6	96.8
132.7	82.9	48.3	293.9	109.0	82.9	48.3	293.9	109.0
147.5	81.4	49.2	271.3	118.0	94.9	42.1	284.8	112.0
162.2	86.3	46.3	258.9	124.0	86.3	46.3	302.1	106.0
176.9	84.8	47.2	282.6	113.0	84.8	47.2	282.6	113.0
191.7	78.3	51.1	260.8	123.0	83.5	47.9	302.6	106.0
206.4	77.5	51.6	247.0	130.0	82.3	48.6	285.8	112.0
221.2	76.9	52.0	266.7	120.0	85.9	46.6	275.8	116.0
235.9	80.5	49.7	258.6	124.0	84.8	47.2	292.5	109.0
265.4	79.1	50.6	263.7	121.0	82.9	48.3	293.9	109.0
294.9	78.0	51.3	267.9	119.0	84.8	47.2	274.7	117.0
309.7	80.7	49.5	261.6	122.0	84.0	47.6	287.4	111.0
324.4	77.1	51.9	249.7	128.0	80.1	49.9	274.3	117.0
353.9	76.3	52.4	254.3	126.0	84.8	47.2	282.6	113.0
383.4	75.6	52.9	258.2	124.0	80.9	49.5	281.7	114.0

Table 2: 45-ns EDO DRAMs

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