DEC-11-HDCD-D

DC11 asynchronous line interface manual

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FOREWORD

This manual provides the user with the theory of operation and logic diagrams necessary to understand and maintain the DC11 Asynchronous Line Data Set Interface. The information in this document is directed at the reader who is familiar with basic digital computer theory.

Although signals and data are transferred between the DC11 and the PDP-11 Unibus, this manual does not cover the operation of the PDP-11 System and the Unibus. A detailed description of the PDP-11 is presented in the set of *PDP-11/20 Manuals* (DEC-11-HR1A-D through DEC-11-HR7A-D), and a detailed description of the Unibus is presented in the *PDP-11 Unibus Interface Manual* (DEC-11-HIAA-D).

The DC11 is an interface between the PDP-11 and the Bell 103A/E/F/G/H, the Bell 202 C/D, or any equivalent modems that are compatible with the above equipments. However, this manual does not discuss operation of these units. Detailed operation and description of the Bell 103A/E/F/G/H and the Bell 202 C/D units are found in their respective *Bell System Communications Technical Reference Manuals.*

A complete set of engineering logic drawings is provided with each Teletype Control. These drawings are bound in a separate volume entitled *DC11 Asynchronous Line Interface Engineering Drawings.* The reduced drawings in the above manual reflect the latest print revisions and correspond to the specific component shipped to the customer.

This manual is divided into five major sections. a) general description, b) installation, c) operational programming, 3) detailed description, and e) maintenance.

CHAPTER 1
GENERAL DESCRIPTION

The DC11 is a fully-buffered interface between the PDP-11 System and a serial asynchronous line. The DC11 can be used to connect the PDP-11 to a variety of asynchronous terminals or to another computer through a common-carrier communications facility. The communications facility can be bypassed, and asynchronous terminal devices and other computers can be connected locally to the PDP-11 computer.

The DC11 supplies the necessary control signals and levels to interface the Bell 103 and 202 modems or their equivalent. The levels are EIA- or CCITT-compatible for data set operation. For other types of operation, level converters can be supplied from the DF-11 series of level converters. The DC11 is ideally suited for interfacing a moderate number of serial asynchronous lines to PDP-11 Systems. Applications of the PDP-11 such as numerical control, data acquisition, physics, biomedical, and data processing often require several asynchronous serial line interfaces to be connected to either terminals or other computers. The DC11 is also a flexible asynchronous interface when used in small time-sharing systems. Terminal manufacturers can easily interface the DC11 to their terminals by choosing the proper level converter.

The DC11 has the flexibility to handle many different types of terminals. The programmer can vary the line speed, character length, stop-code length, and the modem control lines. Input and output speeds of the line can be varied independently.

The PDP-11 Unibus serves as a multiplexer for adding multiple asynchronous line interfaces. Each two interfaces requires the mounting space of one PDP-11 System Unit. The prewired system unit and clock module (M454) are designated as the DC11-AA, DC11-AB, or DC11-AC depending on the programmable line speeds or baud rates desired. The DC11-DA is the module set (M794, M591, M7821, M105, and BC01R Cable Assembly) that interfaces the PDP-11 to a serial asynchronous line through EIA and CCITT levels. Two DC11-DA's mount in each DC11-AA, -AB, or -AC unit. The DC11-AA, -AB, or -AC contains the clock for both DC11-DA module sets.

1.1 DC11 FUNCTIONAL DESCRIPTION

The DC11 is a serial asynchronous line interface capable of program controlled full- or half-duplex operation with a serial modem device. The DC11 provides a choice of four programmable character lengths or codes (5, 6, 7, or 8 bits) that are automatically parity checked on input. The prewired system unit and clock module options each provide a set of four programmable line speeds. The options are:

a. clock frequencies or line speeds of 300, 150, 134.5, and 110 baud for the DC11-AA,
b. clock frequencies of 1800, 1200, 300 and 110 baud for the DC11-AB,
c. clock frequencies of 1200, 600, 150, and 110 baud for the DC11-AC,
d. clock frequencies of 1200, 300, 150, and 134.5 baud for the DC11-AG,
e. clock frequencies of 1800, 1200, 134.5, and 110 baud for the DC11-AH,
f. clock frequencies of 150, 134.5, 110, and 50 baud for the DC11-AD,
g. clock frequencies of 150, 134.5, 110, and 75 baud for the DC11-AE,
h. clock frequencies of X, 150, 134.5, and 110 baud for the DC11-AX where X is any non-standard speed between 600 baud and 19.6 kilobaud.

1.1.1. DC11 Data Set Devices

Generally, the DC11 interfaces Bell 103 A/F/G/H or Bell 202 C/D data set line units. Detailed information on these units is contained in their respective *Bell System Data Communications Technical Reference Manuals.*

It is important that the data set handshaking sequence be discussed in relation to the DC11 used with data sets. In this case, the discussion applies to the Bell 103 type data set (for 202 procedure consult the appropriate manual). The handshaking sets up the computer, the DC11, and the data set for data communication. Handshaking is accomplished through call and acknowledge signals between the three units. The DC11 translates these signals between the computer and the data set through the DC11 status register to obtain a data communication channel.

To establish a data communication channel, the data set at the computer is called by another remote data set (see Figure 1-1), and a RING signal is sent to the DC11. The RING signal initiates an interrupt to the computer, if INTERRUPT ENABLE is set. The software determines that the interrupt was caused by RING and, through a service routine in the software, issues a DATA TERMINAL READY signal. The DATA TERMINAL READY signal causes the data set to answer the call; a CARRIER signal is then sent to the caller. The caller acknowledges the CARRIER signal with its own CARRIER signal, which causes another interrupt to the computer. The computer then goes to a software service routine after recognizing the CARRIER interrupt. At this point, a data channel has been established between the caller and the computer, and the DC11 now can either receive or transmit data. The only prerequisites for the handshaking sequence are that the software service routines be in use and that INTERRUPT ENABLE be set in the DC11.

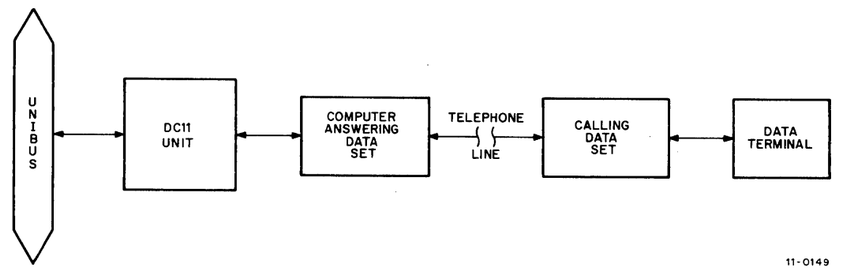


Figure 1-1 Asynchronous Data Communication Block Diagram

1.1.2 DC11 Device Interface

The DC11 is a character-buffered communications interface designed to convert asynchronous serial bit format data to parallel character data and vice versa (see Figure 1-2). The DC11 comprises two independent data transfer units (receiver and transmitter) capable of simultaneous two-way communication. The receiver accepts

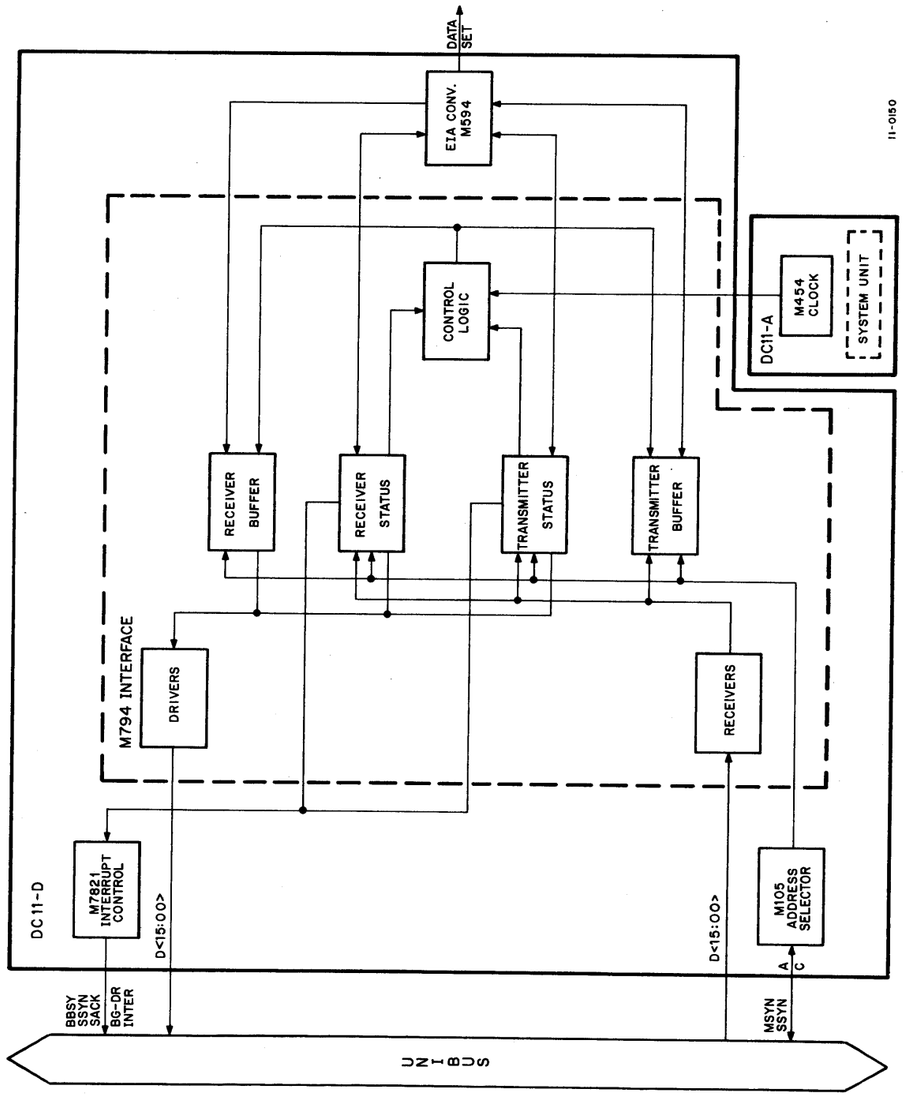


Figure 1-2 DC11 Functional Block Diagram

serial data from the data set lines for parallel conversion and interface to the Unibus. The transmitter shifts serial data onto the data set lines after the interface and parallel conversion of the Unibus data. Each of these units operates through two registers: a) Receiver Control and Status Register (RCSR), Receiver Buffer Register (RBUF); b) Transmitter Status Control and Register (TCSR), Transmitter Buffer Register (TBUF). The Receiver and Transmitter Status Registers control the DC11.

The receiver offers serial-to-parallel conversion of 5-, 6-, 7-, or 8-level codes. The serial character code consists of a start bit, 5 to 8 data bits, and one or two stop bits. The data code size is controlled by the program and appears right-justified in the data buffer without start or stop bits. When the character has been received, its parity is available to the programmer for testing. An interrupt request is generated in the middle of the last data bit of the character being received. If the program does not remove the character from the data buffer before the middle of the next start bit, a data overflow error bit is set in the device. Both the receiver and transmitter character length and stop code length are simultaneously controlled by the program and are always identical.

The transmitter performs parallel-to-serial conversion of 5-, 6-, 7-, or 8-level codes. An interrupt request is generated at the end of the last data bit set. The transmitter is capable of transmitting a continuous space.

The control section of the DC11 Interface provides all leads for the Bell 103 and 202 type data sets, with the exception of DATA SET READY. The data set is controlled by the program. Data set interrupt requests are generated when the RING signal appears or at the transition of the CARRIER DETECT signal. The control section provides four distinct clocking rates that initiate independent transmission and receiving rates. In addition, the DC11-DA contains an EIA converter that converts bipolar inputs to logic levels and logic level outputs to bipolar signals. The EIA converter provides failsafe operation of the control leads (they will appear off if the data set loses power). Other level converters listed in the DF-11 series can be used in place of the EIA converter. Consult the DF-11 option series list for the various types of level converters available.

1.2 DC11 SPECIFICATIONS

The DC11 specifications are grouped into four general categories: a) physical description, b) environmental limits, c) operational interface characteristics, and d) power requirements.

1.2.1 Physical Description

Two DC11 interface units occupy one PDP-11 System unit within the PDP-11 System mounting box (see Figure 1-3). The user may have one or two DC11s per system unit; in which case one unit requires a G727 Jumper Module (supplied with the DC11-AA, -AB, and -AC) for proper operation. One or two DC11 interface units consist of: a) a PDP-11 System unit, b) an M920 Bus Connection Module, c) an M454 Clock Module, and d) power connections. In addition, each DC11 unit consists of: a) an M794 Interface Module, b) an M7821 Interrupt Control Module, and c) an M105 Address Selector Module. If the system is EIA- or CCITT-compatible, then the unit also consists of an M594 Level Converter Module and data set cable connections. If the system is not EIA- or CCITT-compatible, then the appropriate converter module and cable are selected from the DF-11 series. Figure 1-3 illustrates the module layout for a two-DC11 system. In the case of EIA or CCITT levels, the data set connection is provided by a 25-ft cable (BC01R-25) EIA RS 232 C compatible, with a 25-pin connector.

NOTE

If DC11 System Unit is the last unit connected to the Unibus, the last M920 is replaced by a BC11A or Bus Terminator (see Figure 1-3).

1.2.2 Environmental, Interface, and Power Specifications

Environmental limits, operational interface characteristics, and power requirements are listed in Table 1-1.

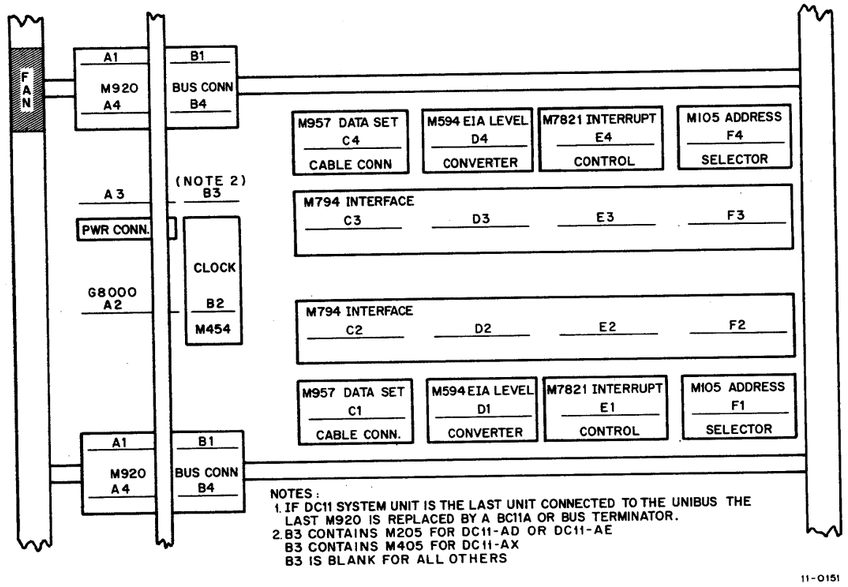


Figure 1-3 DC11 System Unit Layout

Table 1-1
DC11 Specifications

Specification	Description
ENVIRONMENTAL LIMITS	
Temperature	+10° to +50° C (+40° to +120° F) ambient
Humidity	20% to 95% relative humidity
OPERATIONAL INTERFACE CHARACTERISTICS	
Operating Mode	Full- or half-duplex (program-controlled) 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800 baud (four speeds for each of the three options)
Data Rates†	
DC11-AA	300, 150, 134.5, and 110 baud
DC11-AB	1800, 1200, 300, and 110 baud
DC11-AC	1200, 600, 150, and 110 baud
DC11-AD	150, 134.5, 110, and 50 baud
DC11-AE	150, 134.5, 110, and 75 baud
DC11-AG	1200, 300, 150, and 134.5 baud
DC11-AH	1800, 1200, 134.5, and 110 baud
DC11-AX	X†††, 150, 134.5, and 110 baud
Registers	
	Receiver Buffer Register (RBUF) 8-bit register, addressed at 174XX2††
	Transmitter Buffer Register (TBUF) 8-bit register, addressed at 174XX6††
	Receiver Status Register (RCSR) 16-bit register, addressed at 174XX0††

Table 1-1 (Cont)
DC11 Specifications

Specification	Description
	Transmitter Status Register (TCSR) 16-bit register, addressed at 174XX4††
Interrupt Vector Addresses	Addresses 300 through 370 are reserved for as many as eight KL11 Teletype Controls. The address of the first DC11 depends on the number of KL11 addresses used. For example, if two KL11s are addressed the first DC11 (receive) address is 320. The address list below is for eight DC11s assuming eight KL11s are being used and addressed.

Unit	Receiver	Transmitter
0	400	404
1	410	414
2	420	424
3	430	434
4	440	444
5	450	454
6	460	464
7	470	474

Data Format	1 start bit, character length 5, 6, 7, or 8 bits (program-controlled) 1 or 2 bit stop code (program-controlled)
Program Response Time	stop code + 15/16 bit time
Bit Transmission Order	low-order bit first
Parity	computed on incoming data
Distortion	
input	as much as 40% per character
output	less than 3% per character
Bus Load	One line unit represents one unit load to the Unibus. The Unibus can handle 20 unit loads.
(More than 20 unit loads require a bus extender, DB11.)	
Data Signals	For the M594 converter module, conform to EIA RS-232-C and CCITT specifications. Other DF level converters can be used (see DF-11 series converter options).
Control Signals	All Bell 103 and 202 control leads connect to the DC11, except DATA SET READY.
POWER REQUIREMENTS	
Current drawn	4 amps for two line units in a system unit.

†Transmitting and receiving rates are independent.
††XX can range from 00 to 40 for a possible 32 slots.
††† X must be between 600 baud and 19.6 kilobaud

1.4 RELATED DOCUMENTS

A list of documents related to the DC11 and pertaining to its use as a peripheral interface for the PDP-11 Computer are included in this section (refer to Table 1-2).

Table 1-2
Related Documents

Title	Number	Description
GENERAL		
PDP-11 Handbook	Second Edition, 1970	Discussion of overall system, addressing modes, and basic instruction set from a programming point of view. Some interface and installation data.
Instruction List	None	Pocket-size list of instructions. Lists group names, functions, codes, and bit assignments. Includes ASCII codes and the bootstrap loader.
Logic Handbook	DEC, 1970	Presents functions and specifications of the M-Series logic modules and accessories used in PDP-11 interfacing. Includes other types of logic produced by DEC but not used with the PDP-11.
HARDWARE		
UNIBUS Interface Manual	DEC-11-HIAB-D	Used in conjunction with this manual. Provides detailed theory, flow, and logic descriptions of Unibus and external device logic. Discusses methods of interface construction and provides examples of typical interfaces.
PDP-11/20 System	DEC-11-HR1A-D	Introduction, general description specifications of entire PDP-11/20 System. Also contains operating procedures and controls and indicators for both PDP-11 and Teletype.
KA11 Processor	DEC-11-HR2A-D	Block diagram discussion, detailed theory of operation related to flow diagrams, instruction set, module descriptions and related logic diagrams, maintenance, and adjustments.
MM11-E Core Memory	DEC-11-HR3A-D	General discussion, detailed theory of operation, bus transactions, adjustments, maintenance aids, and logic drawings.

Table 1-2 (Cont)
Related Documents

Title	Number	Description
HARDWARE (cont)		
KL11 Teletype Control	DEC-11-HR4A-D	Theory of operation, adjustment and calibration, programming data, maintenance, aids, and logic drawings.
H720 Power Supply & Mounting Box	DEC-11-HR5A-D	Power supply block diagram discussion, theory of operation, circuit diagrams. Mounting box description and specifications for all models and cabinets. Includes installation information.
KY11-A Programmer's Console	DEC-11-HR7A	General description, flow diagram discussion, module description, and related logic diagram. Operation and controls and indicators covered in *PDP-11/20 System Manual.*
PDP-11 Conventions	DEC-11-HR6A-D	*a.* General Maintenance *b.* Logic Symbology *c.* Drawing Set Explanation *d.* Processor Signals *e.* Product Identification Code *f.* Glossary *g.* Abbreviations
SOFTWARE		
Paper Tape Software Programming Handbook	DEC-11-GGPA-D	Detailed discussion of the PDP-11 software system used to load, dump, edit, assemble and debug PDP-11 programs. Also included is a discussion of input/output programming and the floating-point and math package.
DATA SETS		
Bell System Data Communications Data Sets 103 E/G/H Technical Reference Manual	None	Data Set Interface specifications. Data Set description and options including interface signals and timing.
Bell System Data Communications Data Sets 202 C/D Technical Reference Manual	None	Data Set Interface specifications. Data Set description and options including interface signals and timing.
NOTE **Equivalent modem documentation is included when used with the DC11.**		

CHAPTER 2
DC11 INSTALLATION PLANNING

The information necessary to install the DC11 and to achieve operational status is contained in this chapter. All necessary power and interface connections, priority and address references, and optional system configurations are also included in this chapter.

2.1 CONFIGURATIONS

Table 2-1 lists the available DC11 options, their prerequisites, and a brief description.

Table 2-1
DC11 Options

DEC NO.	Description	Prerequisite
DC11-AA	Dual serial asynchronous line system unit and clock. Provides space for mounting two DC11-DA line units. Clock gives 110-, 134.5-, 150-, and 300-baud signals (typical signals for Bell 103 Modem).	PDP-11/20
DC11-AB	Same as DC11-AA except clock gives 110-, 300-, 1200-, 1800-baud signals (typical signals for Bell 202 Modem).	PDP-11/20
DC11-AC	Same as DC11-AA except clock gives 110-, 150-, 600-, 1200-baud signals (typical European frequencies).	PDP-11/20
DC11-AD	Same as DC11-AA except clock gives 150-, 134.5-, 110-, 50-baud signals.	
DC11-AE	Same as DC11-AA except clock gives 150-, 134.5-, 110-, 75-baud signals.	
DC11-AG	Same as DC11-AA except clock gives 134.5-, 150-, 300-, and 1200-baud signals.	
DC11-AH	Same as DC11-AA except clock gives 110-, 134.5-, 1200-, and 1800-baud signals.	
DC11-AX	Same as DC11-AA except clock gives X-, 150-, 134.5-, 110-baud signals.	
DC11-DA	Full-duplex serial asynchronous line unit with modem control features. Allows programmable variation of line-speed character size, stop-code length and data set control lines. Transmitting and receiving speeds are independent. Data-set lines conform to EIA RS 232C and CCITT specifications. Compatible with Bell 103, 202, or equivalent modems. Includes 25-ft modem cable.	DC11-AA DC11-AB, or DC11-AC
H312A	Asynchronous null modem cable. Allows direct connection of a PDP-11 to any peripheral with a data-set type interface that conforms to EIA RS 232C and CCITT specifications. Also allows direct serial asynchronous computer-to-computer data transfers between two PDP-11s. Each PDP-11 must have a DC11-DA, and the maximum separation must not exceed 50 ft.	DC11-DA

The basic DC11 configuration is: two DC11-DA units per PDP-11 System unit with one clock module. The DC11 can connect a variety of terminals to the PDP-11 System, either remotely or locally. These possible configurations are shown in Figure 2-1.

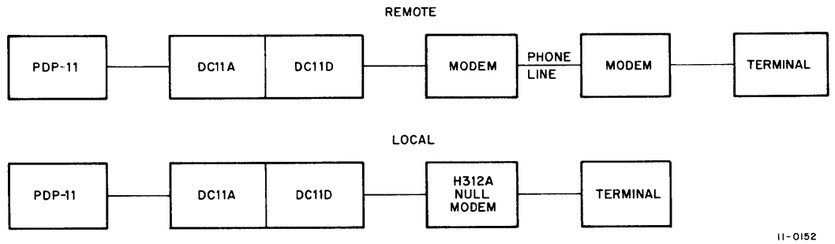


Figure 2-1 Modem Configurations

The DC11 can also connect two PDP-11s; the connections can be either remote or local as shown in Figure 2-2.

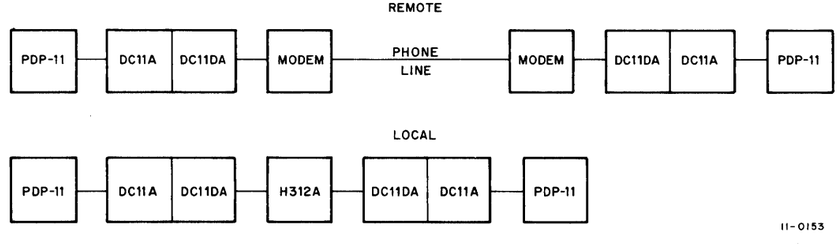


Figure 2-2 Interface Configurations For Two PDP-11s

2.3 CABLING AND TERMINATIONS

The DC11-DA option provides an EIA RS 232 C compatible level converter and cable assembly for data sets. The cable assembly consists of the asynchronous lines connecting the data set and the DC11 in the form of a 25-ft cable (BC01R-25). This cable connects to a data set through a CHINCA DB 25 D connector; it connects to

the DC11 through an M957 Cable Connector Module. Figure 2-3 shows the asynchronous lines of this cable and their respective signal names, color codes, and termination designations. Each line of the cable provides the necessary control signals and data channels for interfacing data sets and the DC11. The control line DATA SET READY is not connected to the DC11. In the case of non-EIA or non-CCITT compatible signals, the DF-11 series of converters can easily replace the present converter.

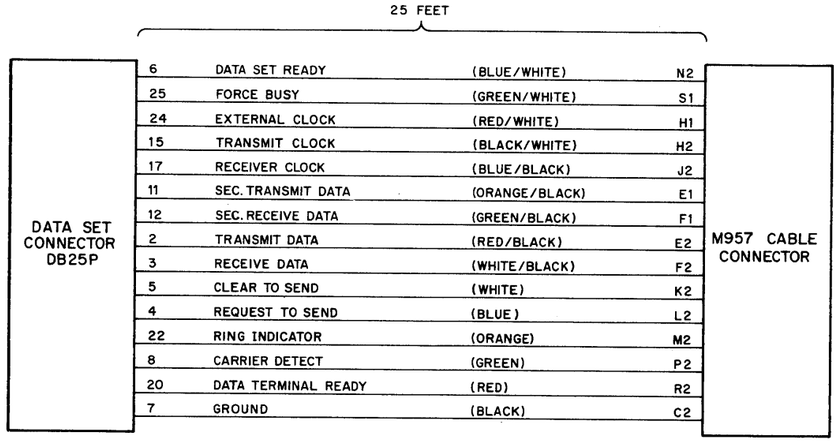


Figure 2-3 Cabling Terminations

2.4 ADDRESS AND PRIORITY ASSIGNMENTS

The DC11 is addressed through the M105 Address select card, and its interrupt vector is determined by the M7820 interrupt card. Each specific DC11 unit uses a different set of vector addresses. These addresses are pre-assigned and are listed in Paragraph 3.3. The priority assignment is determined by the jumper connections that plug into the M794 Module. The normally-supplied priority for the DC11 is Bus Request Line 5 (BR5).

2.5 POWER CONNECTIONS

Power connections to the DC11 are provided by the PDP-11 System (see Figure 1-2). When power is applied to the PDP-11 System, the DC11 receives power also. These power connections are discussed in detail in the *PDP-11 Interface Manual* (DEC-11-HIAB-D).

2.6 INSTALLATION TESTING

Installation testing is performed by running the Off-Line diagnostic program (MAINDEC-11-HIAA) when the system has been completely installed. This program is contained on the diagnostic tape supplied with the DC11. Instructions for running the diagnostic are included with the diagnostic program tape. The Off-Line diagnostic configuration is shown in Figure 5-5. On line tests should also be run if data sets are available.

CHAPTER 3
OPERATIONAL PROGRAMMING

Software-related aspects of the DC11 are discussed in this chapter. The chapter includes a description of the device registers, asynchronous timing considerations, and data format. Programming examples are also provided to illustrate the functions of these software-related areas and to illustrate basic DC11 operation.

3.1 DEVICE REGISTERS

Each of the four DC11 registers and their specific bit assignments are included in the following paragraphs.

3.1.1 Receiver Status Register

RCSR **(Bits shown after POWER CLEAR)** **Address: 174XX0**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0		0	0	0	0	0		0	0	-	0	-*

Bit 0	DATA TERMINAL READY	Control lead to Modem. This bit conditions the automatic answer and is both read and write. This bit must be asserted for data to be received.
Bit 1	BREAK	Bit, when asserted, pulls the output data line to a space. This bit is read and write.
Bit 2	CARRIER DETECT	Control lead from modem. This bit indicates status of carrier and is asserted when channel is established. This bit is read only.
Bit 3, 4	RECEIVER SPEED SELECT	These bits specify the baud rate of the receiver:

4	3	
0	0	Lowest
0	1	
1	0	
1	1	Highest

These bits are both read and write.

Bit 5	PARITY CHECK	This bit provides a parity check to incoming data: Bit 5 = 1 Odd parity checks Bit 5 = 0 Odd parity fault Bit 5 = 0 Even parity checks Bit 5 = 1 Even parity fault Bit is Read Only and is valid until the next character start pulse is received.
Bit 6	INTERRUPT ENABLE	This bit enables the receiver interrupt facility. This bit is both read and write.
Bit 7	DONE	This bit indicates character available and is cleared by reading the receiver buffer. This bit is read only.
Bit 8	SUPERVISORY TRANSMIT DATA	This bit provides signaling capability on reverse channel of 202 C/D modems. This bit is both read and write.
Bit 9, 10	CHARACTER LENGTH	These bits specify the number of bits per character:

10	9	
0	0	8 bits/character
0	1	7 bits/character
1	0	6 bits/character
1	1	5 bits/character

These bits are both read and write.

Bit 12	DATA OVERFLOW	This bit signals an error condition. It is set when the start pulse is received and the done flag is still set. Cleared on read of receiver CSR. This bit is read only.
Bit 13	RING INDICATOR	This bit sets when data set rings. Cleared on read of receiver CSR. This bit is read only.
Bit 14	CARRIER TRANSITION	This bit sets when carrier detect changes state. Cleared on read on receiver CSR. This bit is read only.
Bit 15	ERROR	The logical OR of Bits 12, 13, 14. Causes an interrupt and is read only.

*Data terminal ready not cleared by power clear.

3.1.2 Transmitter Status Register

TSCR **(Bits shown after POWER CLEAR)** **Address: 174XX4**

15		8	7	6		4	3	2	1	0
-		0	0	0		0	0	0	-	0

Bit 0	REQUEST TO SEND	Control lead to modem. This bit is both read and write.
Bit 1	CLEAR TO SEND	Control lead from modem; required that this bit be asserted for transmit interrupt. This bit is read only.
Bit 2	MAINTENANCE	Maintenance function that connects transmitter serial output to receiver serial input. This bit is both read and write.

Bit 3, 4	TRANSMITTER SPEED SELECT
Bit 6	INTERRUPT ENABLE
Bit 7	READY
Bit 8	STOP CODE
Bit 15	SUPERVISORY RECEIVE DATA

These bits specify the baud rate of the transmitter:

4	3	
0	0	Lowest
0	1	
1	0	
1	1	Highest

These bits are both read and write.

This bit enables the transmitter interrupt facility. This bit is both read and write.

Indicates transmitter ready to output data. Cleared by loading transmitter buffer, set by having transmitter buffer zero'd. This bit is read only.

Sets the stop code sent by the transmitter:

0 – Set Stop Code to 2
1 – Set Stop Code to 1

This bit is both read and write.

This bit provides receive capability on reverse channel of 202 C/D modems. This bit is read only.

3.1.3 Data Registers

RBUF RECEIVER BUFFER **Address: 174XX2**

	8-BIT DATA

TBUF TRANSMISSION BUFFER **Address: 174XX6**

	8-BIT DATA

NOTE

Line speed and format are completely specified in the status register. This enables the line unit to handle a variety of terminal equipment without a hardware change. However, the unit is not capable of handling any terminal without some prior knowledge of what types of terminals to expect, i.e., a program that steps through various speeds and formats looking for some predetermined response.

3.2 ADDRESSES

Each line unit contains four registers and requires four addresses. Address space has been assigned for 32 line units. Line unit number 0 starts at 174000; line unit 1 is at address 174010; up to line unit 32 at address 774376.

The four registers and their address are listed below for the first line unit:

a.	Receiver Status Register	174000
b.	Receiver Buffer Register	174002
c.	Transmitter Status Register	174004
d.	Transmitter Buffer Register	174006

The interrupt vectors for the DC11 lie in the communication vector space which starts at location 300. They are assigned contiguously after the KL11 vectors. For example, if the system had two KL11's, then the first DC11 vector would be at location 320.

3.3 TIMING CONSIDERATIONS

The DC11 has two basic timing considerations: a) the baud rate selection, and b) the time restriction for getting a character off the Receiver Buffer Register.

The baud rate is selected by the program. The selected baud rate is reflected in the status registers, in bits 3 and 4. Four possible baud rates are available to the programmer, according to the option (DC11-AA, DC11-AR) being incorporated. Bits 3 and 4 of the Receiver Status Register and the Transmitter Status Register can be set to any of the four possible baud rates. It is not necessary that the line speed of transmission be the same as the line speed of reception. The bit configurations for the four speeds are shown in Table 3-1.

Table 3-1
Bit Configurations

Bit 4	Bit 3	DC11-AA Speed	DC11-AB Speed	DC11-AC Speed	DC11-AD Speed	DC11-AE Speed	DC11-AG Speed	DC11-AH Speed	DC11-AX Speed
0	0	110	110	110	50	75	134.5	110	110
0	1	134.5	300	150	110	110	150	134.5	134.5
1	0	150	1200	600	134.5	134.5	300	1200	150
1	1	300	1800	1200	150	150	1200	1800	X

X = between 600 and 19.6K baud.

These bits are set by the two bus receiver data lines (BD 04 and BD 03).

When a character is received in the Receiver Buffer Register, an interrupt is generated in the center of the last bit received. The computer then has until the center of the start bit of the next character to read the character (see Figure 3-1). The time the computer has depends on whether or not there is one or two stop code bits and whether or not the line is transmitting at maximum rate. If this character is not read in this time period, the new character coming into the register causes an overflow condition to exist that generates an error condition and an interrupt.

3.4 DATA FORMAT

There are four programmable character lengths in the DC11. These character lengths are program-controlled through bits 9 and 10 of the Receiver Status Register (see Figure 3-1). These bits are set by two bus receiver data lines (BD 09 and BD 10). The bit configurations for the four possible character lengths are shown in Table 3-2.

Table 3-2
Bit Configurations

Bit 10	Bit 9	Character Length
0	0	8 bits/character
0	1	7 bits/character
1	0	6 bits/character
1	1	5 bits/character

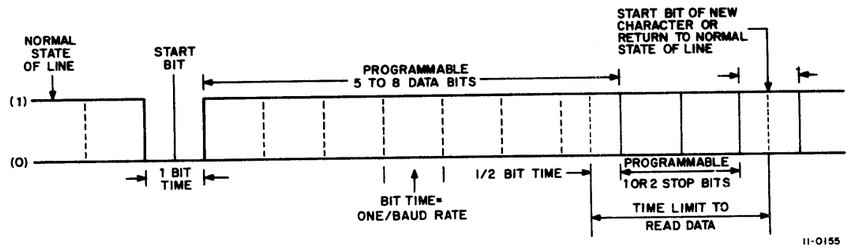


Figure 3-1 DC11 Data Character Format

3.5 PROGRAMMING EXAMPLES

This section illustrates DC11 data communication processes through program examples. These examples demonstrate the use of the DC11 for interfacing data in relation to the entire PDP-11 System. Three programming examples are presented: a) a handshaking service routine, b) a receiver service routine, and c) a transmission service routine.

3.5.1 Handshaking Service Routine

The handshaking service routine demonstrates how a data channel is established between the computer and the data set calling it. Basically, the data channel is established by checking the RCSR for data set signals. Each bit causes the computer to perform a specific service to obtain a data set reply.

```
HANDSHAKE:  MOV RCSR, R0          MOVE RCSR TO REGISTER 0
            BIT #100000, R0       TEST BIT 15
            BEQ RCV, SERVICE      GO TO RECEIVER SERVICE
            BIT #20000, R0        TEST RING
            BEQ CARRIER           CHECK CARRIER
            BIS #1, RCSR          SET DATA TERMINAL READY
            DELAY                 DELAY 10 SEC TO WAIT FOR CARRIER
            BIT #2, RCSR          CHECK FOR CARRIER
            BNE CHAN MODE         BRANCH TO CHANNEL ESTABLISH MESSAGE
            BIC #1, RCSR          CALL IS NOT DATA SET, DROP LINE
            RTI
```

3.5.2 Receiver Service Routine

This routine serves two receiver purposes: a) the contents of the RCSR are moved to the computer; here these are checked for interrupt conditions that occur as each character is being received, b) the contents of the RBUF are moved to a computer register and then incorporated into memory or another storage area.

```
RCV SRV:    MOV RCSR, TEMP        ; RCSR MOVED TO TEMP REGISTER
            BMI ERROR             ;CHECK ERROR BIT
            TSTB TEMP             ;TEMP TESTED FOR DONE FLAG
            BPL FLS INT           ;FALSE INTERRUPT
            MOVB RBUF, @INBUF     ;RBUF MOVED TO COMPUTER REGISTER
            INC INBUF             ;RBUF INCORPORATED IN MEMORY
            RTI
ERROR:      .
            .
            .
            .
            .
            RTI
FLS INT:    .
            .
            .
            .
            .
            RTI
```

3.5.3 Transmitter Routine

When the program has a message to output, it loads the message in a specific core area. The program then enables the interrupt bit of the transmitter control status register. When the ready bit comes on and CLEAR TO SEND is on, an interrupt is requested. An interrupt routine puts one character in the transmitter buffer, increments the pointer, decrements the count, and then returns. When a character has been transmitted, the ready bit signals for another interrupt, and so on until the counter is reduced to zero. When the counter is reduced to zero, the interrupt bit is disabled on TCSR. This procedure is shown below.

The main program loads the buffer, initializes the pointer address and character count, and sets the interrupt bit.

```
            MOV     #X1,    POINTER
            MOV     #X2,    COUNT
            MOV     #100,   TCSR            ;ENABLE INT
```

When the ready bit comes on, an interrupt is requested. When an interrupt is granted, the unit jumps to service the transmit routine.

```
SERVICE T:
            MOVB    @POINTER, TBUF      ;MOVE CHARACTER TO BUFFER
            INC     POINTER
            DEC     COUNT
            BEQ     DONE
            RTI
DONE:
            CLRB    TCSR                ;CLEAR INT FLAG
            RTI
```

CHAPTER 4
DC11 DETAILED DESCRIPTION

Chapter 4 is a detailed description of the DC11 interface unit. The DC11 can be divided into seven major functional groups:

a. selection logic
b. interrupt logic
c. clock logic
d. converter logic
e. receiver logic
f. transmitter logic
g. maintenance mode logic.

Each of these areas is presented separately in the following paragraphs. A brief description of the task of each functional unit is as follows:

Selection Logic - The selection logic determines if the DC11 unit has been selected for use, and what type of operation (transmit or receive) has been selected. It consists of the M105 Address Selector Module and portions of the M794 Module.

Interrupt Logic - The interrupt logic permits the DC11 to gain bus control and perform an interrupt program. The priority level of the bus request (BR) line can be changed by the user. This logic consists of an M7821 Interrupt Control Module and portions of the M794 Module.

Clock Logic - The clock logic provides a total of six baud rates from a crystal clock and one baud rate from a reed oscillator for clocking data transfer rates. Three combination options of four speeds are available. This logic consists of the M454 Clock Module.

Converter Logic - The converter logic converts TTL logic levels to levels suitable for transmission. The M594 Level Converter converts to EIA and CCITT bipolar signals. Other DF-11 series level converters can be used.

Receiver Logic - The receiver logic converts serial data from an asynchronous line into parallel data for gating to the bus. This logic consists of part of the M794 Interface Module.

Transmitter Logic - The transmitter logic converts parallel data from the bus to serial data for transmission on the asynchronous data lines. This logic consists of part of the M794 Interface Module.

NOTE

The DC11 unit performs two basic operations: Receiving and transmitting data. When receiving data, it is inputting data from the data lines and outputting data to the bus; conversely, when transmitting data it is inputting data from the bus and outputting data onto the data lines.

The discussions presented in this chapter are supported by a complete set of engineering drawings located at the end of this manual.

4.1 SELECTION LOGIC

The DC11 selection logic is used to decode the address on the bus lines and to determine if the DC11 unit has been selected for use. A unique address is assigned to both the receiver and the transmitter; consequently, the incoming address determines if a character is to be received off the data lines or transmitted onto the data lines.

The DC11 consists of four registers or bus addresses. The selection logic is used to control the flow of information between the Unibus and the device registers. The selection logic produces SELECT lines, the logic also produces gating IN or OUT signals that determine the register to be used, and whether the register is to perform a receive or transmit function.

The selection logic consists of an M105 Address Selector Module, gating logic, and bus drivers and receivers.

4.1.1 Address Selector Module†

The M105 Address Selector Module decodes the address information from the bus and provides two gating signals and four select line signals that are used to activate appropriate DC11 circuits for the selected function. The M105 Module jumpers are arranged to allow the module to respond to only the standard device register address. Although these addresses have been selected by DEC as the standard assignments for the DC11, the customer can change the jumpers to any address desired.

4.1.2 Gating Logic

The gating signals and select line signals from the M105 Address Selector are applied to the gating logic (drawing D-CS-M794-0-1 Sheet 2 of 5), which provides the pulses that activate either the receiver or transmitter circuits. These pulses enable the bus drivers and bus receivers that are connected to the Receiver Buffer (RBUF) and Receiver Status (RCSR) Registers in the receiver logic, and are also connected to the Transmitter Buffer (TBUF) and Transmitter Status (TCSR) registers in the transmitter logic.

The four register select signals (SELECT 0, SELECT 2, SELECT 4, and SELECT 6) indicate the register being referenced. The two gating signals (IN, OUT) indicate the direction of data flow in reference to the Unibus. The gating signals either gate data from the DC11 to the bus (IN) or gate data from the bus into the DC11 (OUT).

The gating signals, select lines, and related functions are listed in Table 4-1.

4.1.3 Bus Drivers and Receivers†

Bus drivers and bus receivers are logic gates; these gates are used to pass signals to and from the Unibus while maintaining the transmission-line characteristics of the bus. These logic gates have the high input impedence and proper logic thresholds required by the bus signals.

†The descriptions provided in Paragraphs 4.1.1, 4.1.3, and 4.2 are basic descriptions. For more detailed discussions refer to the 1970 *DEC Logic Handbook* and the *Unibus Interface Manual* (DEC-11-HIAB-D).

Table 4-1
Gating and Select Line Signals

Select 0	Select 2	Select 4	Select 6	Gating Signal	Function Selected	Register	Bus Cycle
0	1	0	0	IN	GATES BUS DRIVERS	RBUF	DATIP or DATI
1	0	0	0	IN	RCSR GATED TO BUS	RCSR	DATIP or DATI
0	0	1	0	IN	GATES BUS DRIVERS	TCSR	DATIP or DATI
0	0	0	1	OUT	BUS GATED TO TBUF	TBUF	DATOB or DATO
1	0	0	0	OUT	BUS GATED TO RCSR	RCSR	DATOB or DATO
0	0	1	0	OUT	BUS GATED TO TCSR	TCSR	DATOB or DATO

4.2 INTERRUPT CONTROL†

The M7821 Interrupt Control Module enables the DC11 unit to gain control of the bus (become bus master) and perform an interrupt operation. When the last bit of data is in the RBUF, the DONE bit is set. If the INTERRUPT ENABLE bit (bit 6) is set in the RCSR, the interrupt control is activated and the interrupt software service routine is entered. When TRANSMIT INTERRUPT (bit 6) of the TCSR is set and the READY bit is up, the interrupt control is activated, and the transmit interrupt software routine is entered. The jumpers on the M782 Module determine the vector address of the interrupt.

The receiver initiates an interrupt whenever RING = 1, or CARRIER TRANSITION = 1 (both leads from the data set), or DATA OVERFLOW = 1, or when DONE = 1. The transmitter initiates an interrupt whenever READY = 1 AND CLEAR TO SEND = 1. The standard priority level is determined by the MAINDEC program's reference of level 5 and is set at the BR5 level for the DC11. Although a standard level, the priority level can be changed by the user.

4.3 CLOCK LOGIC

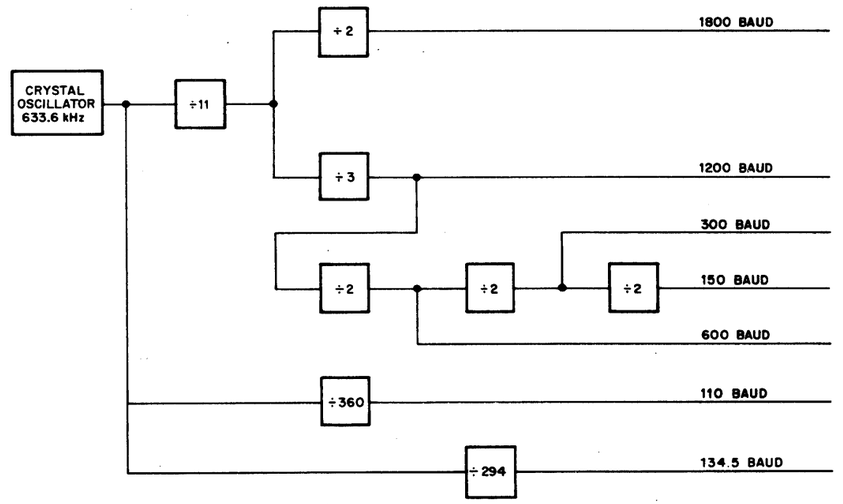
The selectable baud rate clocking signals are generated on the M454 Clock Module. The clock module logic provides seven different baud rates through a series of logic divider circuits. These circuits are driven by a 633.6 kHz Crystal Oscillator that generates seven baud frequencies through the dividers. Each of these baud frequencies is 16 times the baud rate. The pulse widths are 500 ns to 1000 ns and negative going. The clock module divider logic and oscillators are shown on drawing (D-CS-M454-0-1). Figure 4-1 shows the divider progressions off the oscillators in block diagram form for generating the necessary baud rate signals.

4.4 CONVERTER LOGIC

The converter logic for data sets consists of the M594 Level Converter Module, which converts TTL logic levels to EIA- and CCITT-compatible bipolar signals. Other DF-11 series converters can be used other than the EIA converter. Consult the DF-11 series for the various types of converters.

4.5 RECEIVER LOGIC

The receiver logic is activated by the start bit of the incoming data. The data set sends data through the RECEIVE DATA asynchronous line to the RBUF of the DC11. The RBUF consists of two four-bit shift registers that are loaded serially and generate a parallel output. The character format is such that spaces correspond to binary 0s and marks correspond to binary 1s.



NOTE
Each baud output is 16 times the baud rate.

Figure 4-1 Clock Module Functional Block Diagram

A detailed description of the operation of the receiver logic is presented in the following paragraphs. The receiver logic circuits are shown on drawing D-CS-M794-0-1, sheet 4 of 5, and the related control circuits are shown on drawing D-CS-M794-0-1, sheet 3 of 5. Receiver flow is shown in Figure 4-2, receiver logic timing is shown in Figure 4-3.

4.5.1 Initialization

When power is applied to the PDP-11 computer system, the computer processor generates BUS INIT (L). The BUS INIT (L) signal clears the CSRs and flip-flops of the receiver logic.

4.5.2 Receiver Data Transfer

To achieve proper data transfer, the DC11 must be program-prepared with the correct character length or level and correct baud rate. The DC11 hardware cannot determine the character length and baud rate; therefore, the unit must be given the character length and baud rate of the data before receiving the data. Knowledge of the character length and baud rate enables the DC11 to load the RBUF at the proper bit and to clock the data at the proper rate. These conditions are necessary to avoid misinterpretation of data.

†Refer to the footnote on page 4-1.

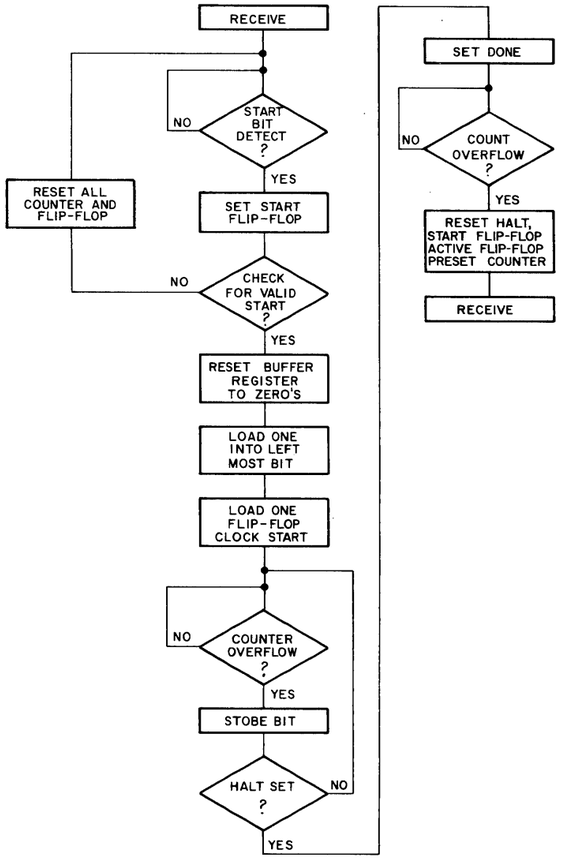


Figure 4-2 Receive Communication Flow Diagram

Data is clocked or strobed serially into the RBUF by the receiver counter. The character length select bit gates the data to the proper leftmost bit of the RBUF. The first bit to be strobed in is the start bit; each incoming bit is shifted to the right as another bit is strobed in. If the correct character length has been chosen, the RBUF is loaded when the start bit is shifted through the RBUF, which sets the HALT flip-flop. Setting the HALT flip-flop sets the DONE flip-flop, which causes an interrupt to the computer if the interrupt enable bit is set in the RCSR. The computer can retrieve data from the RBUF until the middle of the next character's start bit. The computer obtains data from the RBUF through the logic that generates SELECT 2 (H). SELECT 2 (H) clears the DONE flip-flop for the next character. If a new start bit is strobed in while the previous character is in the RBUF, the signals START PULSE (L) and DONE (L) will gate to set DATA OVERFLOW (bit 12 of the RCSR). DATA OVERFLOW generates ERROR, which causes an interrupt to the computer if INT ENB (1) through RCV INT (H). This interrupt causes the computer to branch to an error service routine.

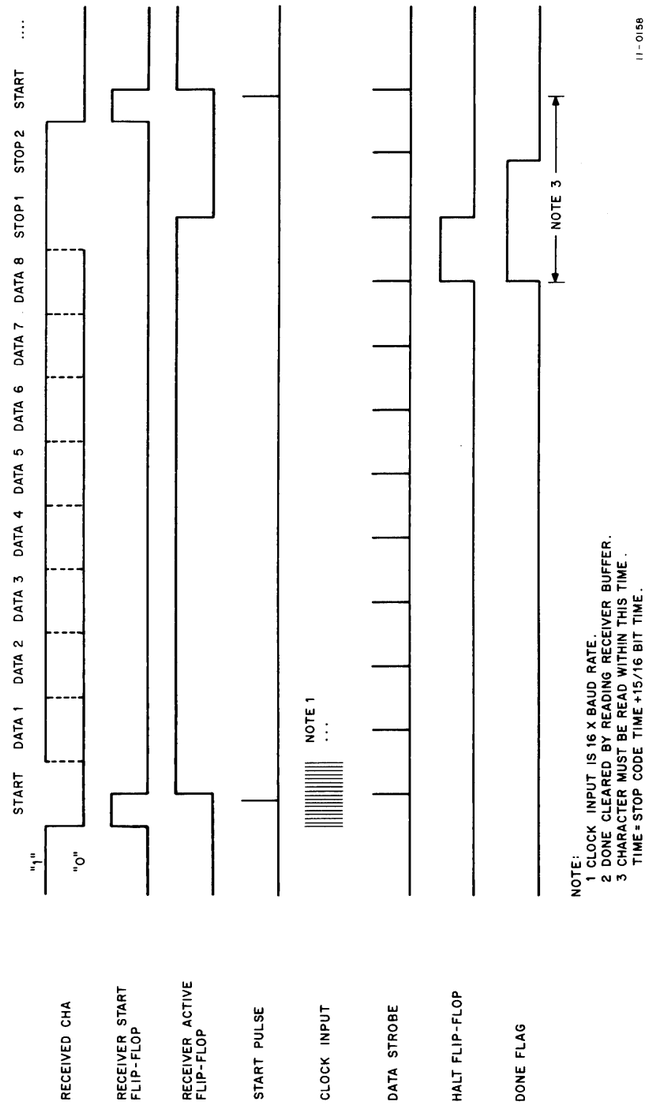


Figure 4-3 Receiver Logic Timing Diagram

4.5.3 Receiver Timing

The correct baud rate or line speed must be selected to generate the proper clock signal to the receiver counter through RCV CK (H). When the character level goes from mark to a space, the RCV START flip-flop is set. This flip-flop along with RCV CK (H) starts the receiver counter. RCV CK (H) is 16 times the selected baud rate, because the receiver counter is a 16-state device and strobes the data once for every 16 times it is clocked. The initial state of the receiver counter is eight. If during the counter's first strobe pulse (which occurs on counter overflow) a space bit is still present, there is a valid start bit, setting the RCV ACTIVE flip-flop. If the start bit is not present at this time, then the mark-to-space transition was simply a random pulse, and RCV ACTIVE does not set. The counter resets the registers; presets the count to eight; and the counter stops.

The counter also generates a start pulse that resets the RBUF and a data strobe signal that strobes the inverted start bit into the RBUF. The counter is initially on eight; thus, it overflows at the center of the start bit, thereby generating the start pulse and strobe signals (start pulse occurs 1/16 of a bit time before strobe). The counter similarly overflows for each succeeding bit until stopped. Therefore, as each bit of data is gated to the RBUF, it is strobed in by the counter.

After the last data bit is transferred, the inverted start bit is shifted through the RBUF and sets the HALT flip-flop, which in turn sets the DONE flip-flop. The next strobe pulse does not strobe in a bit, but generates a stop signal that resets the RCV ACTIVE flip-flop and resets the counter to eight; it is then ready for the next character. This stop signal also resets the HALT and RCV ACTIVE flip-flops. When the counter is stopped, the registers are in the inactive state until the next start bit is detected. If the computer has taken the character from the register, then the receiver is ready for the next character and no overflow error will occur.

4.6 TRANSMITTER LOGIC

When handshaking has occurred, the transmitter is ready for data communication. On program command, a character from a memory location is sent in parallel format to the TBUF for transmission to the data set calling for it. The TBUF consists of two four-bit shift registers. The transmitter logic generates a start bit, shifts the character bits serially to the line, and generates either one or two stop bits (programmable). The character length and baud rate are predetermined by the software before transmission; the stop code is also predetermined by software.

The transmitter data transfer and timing are described in the following paragraphs. The transmitter logic circuits are shown in drawing D-CS-M794-0-1 sheet 5 of 5, and related control logic is shown in drawing D-CS-M794-0-1 sheet 3 of 5. The transmitter flow is shown in Figure 4-4, and the transmitter timing diagram is shown in Figure 4-5.

4.6.1 Initialization

When the computer power is asserted, the B INIT (L) signal appears in the DC11 and clears all registers. In the transmitter, the B INIT (L) signal clears all flip-flops, except the LINE flip-flop which is set. Setting the LINE flip-flop generates a continuous mark, which is the normal state of the line.

4.6.2 Transmitter Data Transfer

When BUS to TRAN BUF (H) appears at the transmitter, the RUN flip-flop is clocked, the POINTER flip-flop is set, and TBUF is loaded. At this point, TBUF is ready to shift parallel data to the line. The data is shifted through the register one bit at a time. The last bit shifted is the pointer bit, which is generated by the POINTER flip-flop. The purpose of the pointer is to indicate that the data transfer is complete. This data is serially clocked through the LINE START flip-flop and then the LINE flip-flop. Initially, the LINE flip-flop generates a continuous mark; however, it is cleared when the first data bit is shifted to the LINE START flip-flop, and generates a space on the line followed by the data. This space is the start bit for the transmitting character. The pointer bit at the rear of the data bits becomes the stop bit or bits depending on the stop code length selected.

Stop code timing is accomplished in the HALT 1 and HALT 2 flip-flops. When the stop code bit in the TCSR is set, a stop code length of one bit is required. In this case, the stop code bit generates the signal HALT 2 FLOP

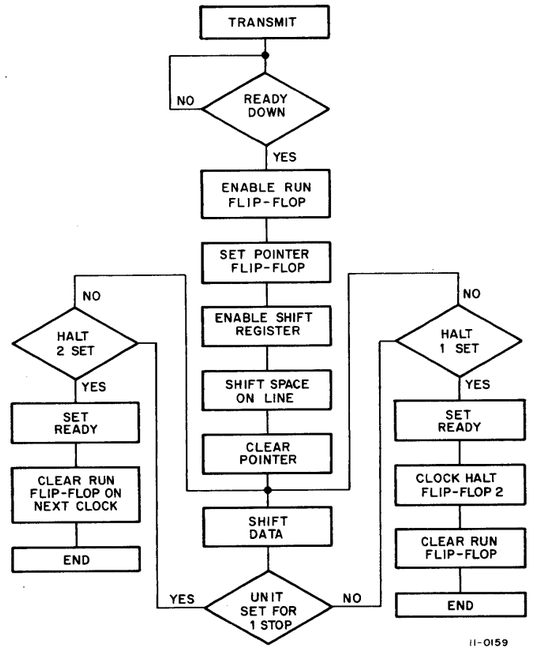


Figure 4-4 Transmitter Communication Flow Diagram

(L), which enables the HALT 2 flip-flop to be set on the next shift pulse after the pointer is shifted into the LINE START flip-flop. When the stop code bit in the TCSR is clear (2 bit stop code), the signal STOP CODE SELECT 1 (H) is generated by the stop code control logic. The STOP CODE SELECT 1 (L) signal enables the HALT 1 flip-flop, which outputs the HALT IN 0 (L) when the pointer is shifted into Line. Thus, HALT 1 prevents the TBUF from shifting and enables another clock cycle. In the stop code logic, the HALT IN 0 (L) signal generates HALT 2 FLOP (L), which enables the HALT 2 flip-flop. HALT 2 then clears the RUN flip-flop on the next shift pulse, shuts off the clock.

4.6.3 Transmitter Timing

The transmitter clock is enabled by the RUN flip-flop. The TRAN CK (L) signal initiates the proper program-selected baud rate to the transmitter clock.

At the start of transmission, the BUS-to-TRANS BUF signal sets the RUN flip-flop, which enables the clock. The action of loading TBUF clears the READY bit. The TRAN CK (L) is divided by 16 to provide a square wave at the baud rate. This square wave clocks the TBUF register, which shifts the data serially onto the line. When the pointer clears the TBUF, READY is asserted in the TCSR. For a 1-bit stop code, HALT 2 stops the clock by clearing the RUN flip-flop. For the 2-bit stop code, the HALT 1 flip-flop sets; one cycle time later, the HALT 2 flip-flop sets. At the next cycle time Halt 2 clears and stops the clock.

4.7 MAINTENANCE MODE

The maintenance mode is used to check the operation of the DC11 logic. Figure 4-6 is a simplified diagram of the maintenance mode. If in maintenance mode, when a character is loaded into the TBUF from a memory

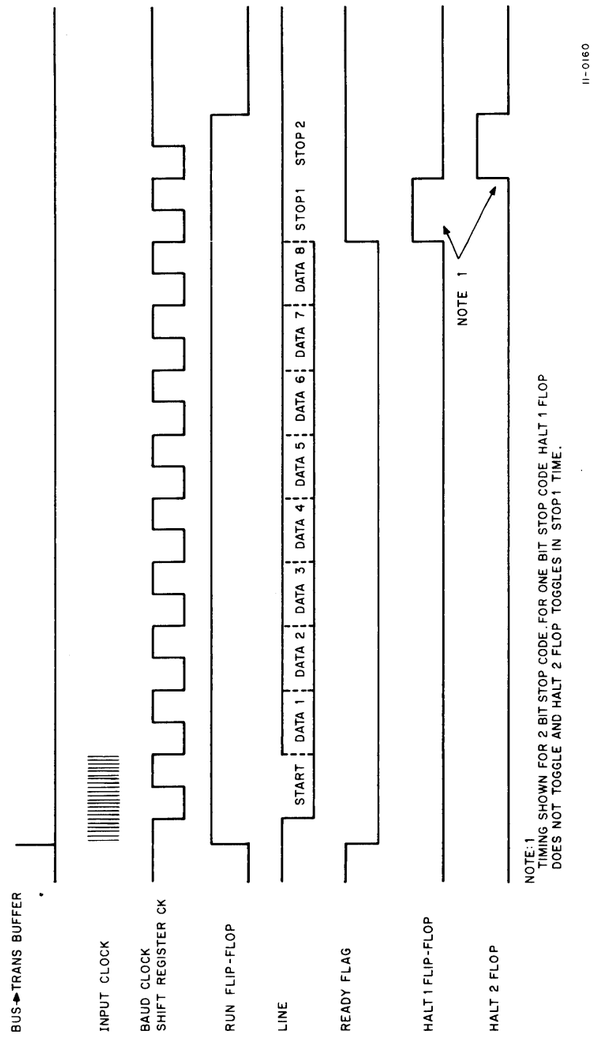


Figure 4-5 Transmitter Timing Diagram

location, the transmitted serial data is fed back into the receiver, which converts it back to parallel data. If the character received by the bus is identical to the transmitted character, then both the transmitter and the receiver are functioning properly.

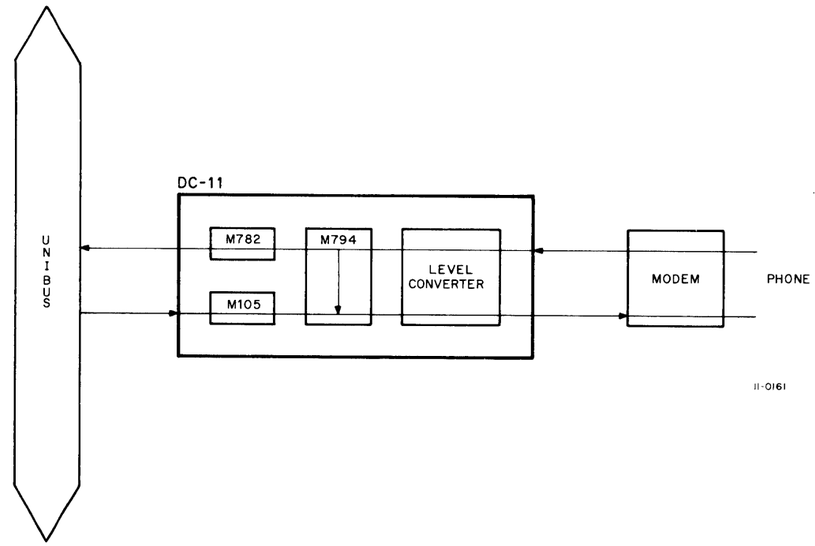


Figure 4-6 Maintenance Mode Configuration

The program selects the maintenance mode by setting MAINTENANCE (bit 2) in the TCSR, which sets the MAINT flip-flop in the transmitter logic (see drawing D-CS-M794-0-1 sheet 5 of 5). When the MAINT flip-flop is set, the serial output of the transmitter (LINE flip-flop output) is gated to the input of the receiver logic.

The receiver logic is activated by a start bit (regardless of where the start bit comes from); the receiver is activated as soon as it receives the first input from the transmitter. After the receiver assembles the data, the receiver DONE bit is set, and the program can compare the received character with the transmitted character to determine if the DC11 is functioning properly.

The above maintenance mode operation is basically what occurs when the off-line diagnostic is run. Chapter 5 is a discussion of the diagnostics and their hardware configurations.

CHAPTER 5
MAINTENANCE

Two basic diagnostic programs are provided with the DC11: MAINDEC-11-D9A (DC11 Off-Line Tests), and MAINDEC-11-D9BA (DC11 On-Line Tests). The Off-Line Tests diagnostic checks all DC11 logic and can be used to test up to 16 DC11s individually. The Off-Line Tests diagnostic does not require the use of a modem or data set; however, a special jumper (see Figure 5-1) connector is required. The On-Line Tests diagnostic is essentially a data reliability test requiring the use of modems and a suitable terminal device.

The following paragraph lists the equipments required to run the diagnostics. In addition, Figures 5-2 through 5-5 show some diagnostic maintenance configurations.

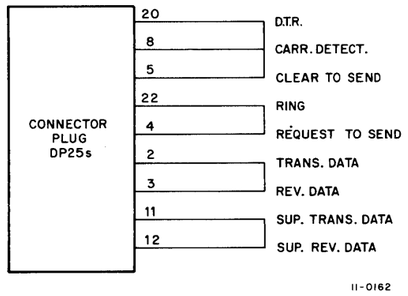


Figure 5-1 Special Jumper Connector

5.1 REQUIRED EQUIPMENT

The following equipments are required to run the diagnostic programs listed in Table 5-1.

a. PDP 11/20 System

b. DC11 (up to 16 units)

c. Special Jumper Connector (supplied with DC11 module set, see Figure 5-1)

Table 5-1 lists the diagnostic tests available in each MAINDEC package.

The diagnostic programs are supplied with the DC11 on paper tape; a complete set of operating instructions for the diagnostics and a program print-out are also included.

Table 5-1
Diagnostic Tests

Off-Line Tests	On-Line Tests
Program 0: Input/Output Logic Tests	Program 0: Transmit Single Character On-Line
Program 1: Transmitter Scope Loop	Program 1: Transmit Binary Count On-Line
Program 2: Receiver Scope Loop	Program 2: Transmit Message On-Line
Program 3: Single Character Maintenance Mode Data Test	Program 3: Receive Data From Terminal (Requires full-duplex line)
Program 4: Special Binary Count Maintenance Mode Data Test	Program 4: Maintenance Mode Interaction Test

5.2 CONFIGURATIONS

For the Off-Line Tests, Figure 5-2 shows the configuration for program 0 (Input/Output Logic Tests) using the special jumper connector. Off-Line programs 1 through 4 all use the maintenance mode configuration shown in Figure 4-6 of the maintenance mode section. For the On-Line Tests, Program 0 (Transmit Single Character) and 1 (Transmit Binary Count) can use any of the possible configurations shown in Figures 5-3 through 5-5. The configuration shown in Figure 5-5 can only be used in full-duplex mode. On-Line programs 2 (Transmit Message) and 3 (Receive Data From Terminal) can be run in the configuration shown in Figure 5-3.

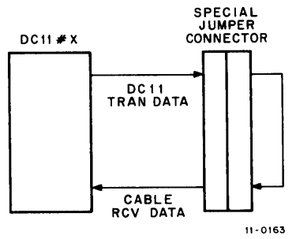


Figure 5-2 Off-Line Program 0 Configuration

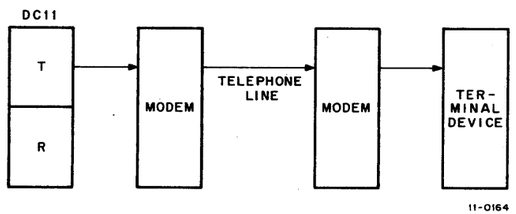


Figure 5-3 Program 0 or 1 Configuration #0

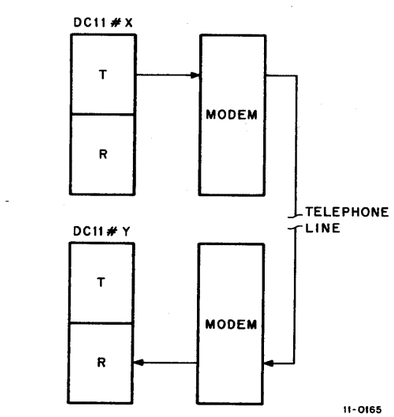


Figure 5-4 Program 0/1 Configuration #1

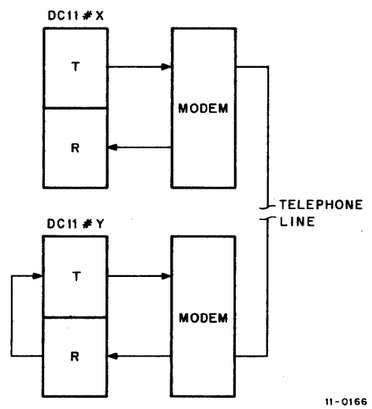


Figure 5-5 Program 0/1 Configuration 2

CHAPTER 6
ENGINEERING DRAWINGS

ENGINEERING DRAWINGS

A complete set of engineering drawings and module circuit schematics is provided with each DC11 System. These are located in the *DC11 Asynchronous Line Interface Engineering Drawing* Manual. The general logic symbols used on these drawings are described in the *DEC Logic Handbook,* 1970. Specific symbols as well as special ICs and circuits are discussed in the *KA11 Processor Manual.*

The *DC11 Asynchronous Line Interface Engineering Drawing* Manual contains the drawings listed in Table 6-1.

Table 6-1
DC11 Engineering Drawings

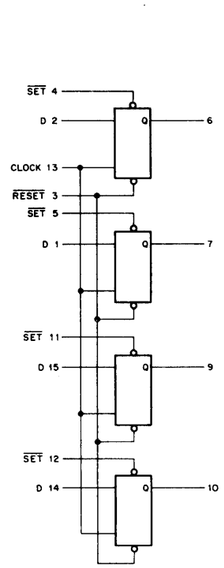
Drawing No.	Title
D-DI-DC11-A-1	Drawing Index List (DC11-A)
D-AD-7007091-0-0	Wired Assy (DC11-A)
A-PL-7007091-0-0	Wired Assy (DC11-A)
D-MU-DC11-A-2	Module Utilization
A-PL-DC11-A-2	Module Utilization PL
K-WL-DC11-A-3	Wire List DC11-A
C-CS-M454-0-1	Crystal Clock
B-CS-G8000-0-1	Filter Network
B-CS-M204-0-1	Counter Buffer
B-CS-M405-0-1	Crystal Clock
A-PL-DC11-DA-0	Data Set Interface
D-MU-DC11-DA-02	Module Utilization
A-PL-DC11-DA-02	Module Utilization PL
D-BS-DC11-DA-03	Device Control
D-IC-DC11-DA-04	Bus & Power Connectors
C-IA-7408925-0-0	Test Connector
D-CS-M7821-0-1	Interrupt Control Card
C-CS-M594-0-1	EIA Level Converter
D-CS-M794-0-1	Modem Interface & Control Card
D-UA-BC01R-0-0	Cable Card Assembly
A-PL-DC11-A-0	Asynchronous Data
A-SP-DC11-A-4	Asynchronous Line Data Acceptance Test
B-BS-DC11-DA-05	M594 Block Schematic

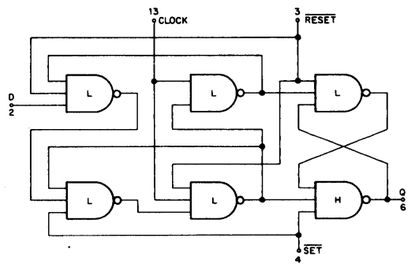
APPENDIX A
IC DESCRIPTIONS

This appendix provides logic diagrams, truth tables, and pin assignment diagrams of the integrated circuit units used in the DC11. The ICs covered are:

4015	Quad Type D Flip-Flop
8271	4-Bit Shift Register
74153	Dual 4-Line-to-1-Line Data Selector/Multiplexers
74197	50-MHz Presettable Decode and Binary Counters/Latches

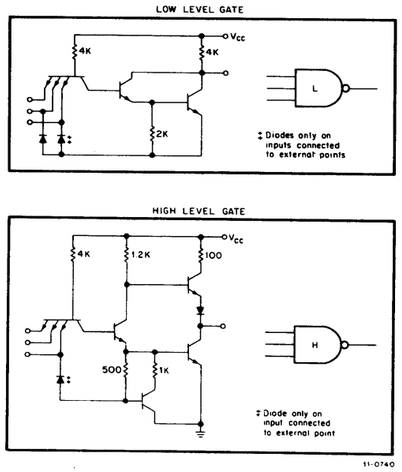
4015 QUAD TYPE D FLIP-FLOP





1/4 OF DEVICE SHOWN
CLOCK AND $\overline{\text{RESET}}$ COMMON TO ALL FOUR FLIP-FLOPS
V_{CC} = PIN 16
GND = PIN 8

11-0739



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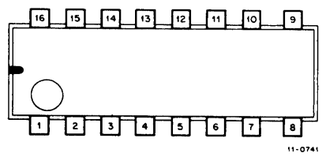


11-0741

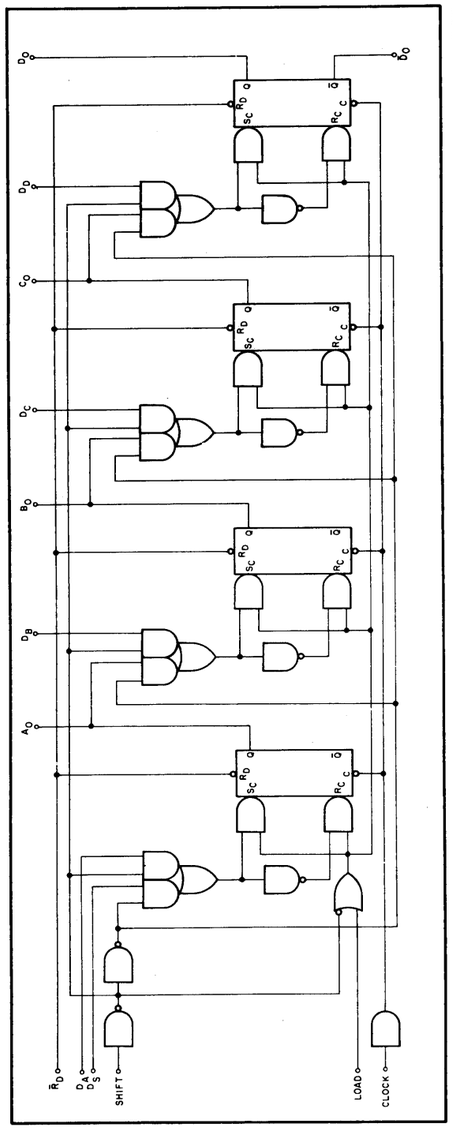
TRUTH TABLE

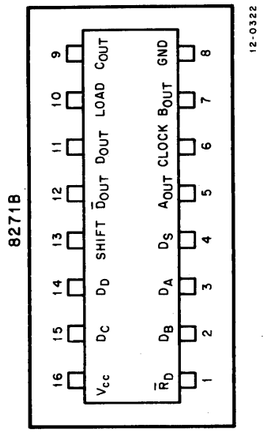
D	Q_{n-1}	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

Q_{n-1} = time period prior to clock pulse

Q_n = time period following clock pulse

8271 4-BIT SHIFT REGISTER

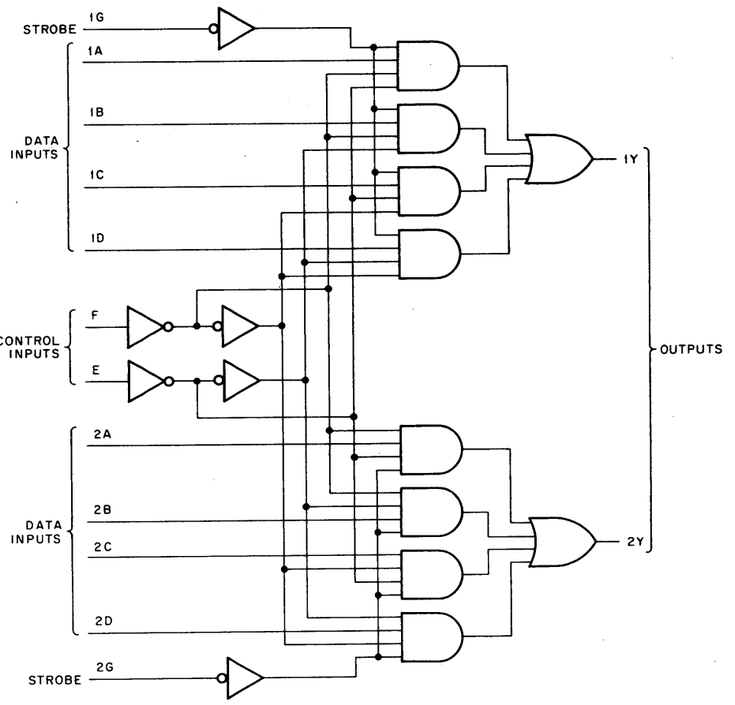




TRUTH TABLE

Control State	Load	Shift
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1

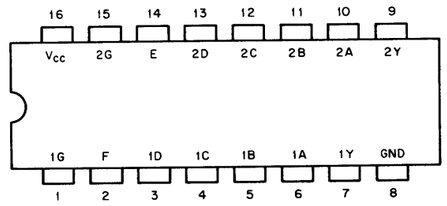
74153 DUAL 4-LINE-to-1-LINE DATA SELECTOR/MULTIPLEXERS



LOGIC DIAGRAM

CONTROL INPUT		STROBE	OUTPUT
E	F	G	Y
LOW	LOW	LOW	A
HIGH	LOW	LOW	B
LOW	HIGH	LOW	C
HIGH	HIGH	LOW	D
DON'T CARE		HIGH	LOW

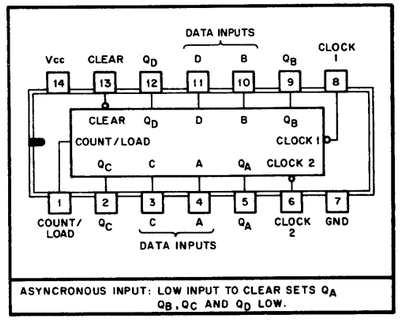
TRUTH TABLE (EACH HALF)



PIN LOCATOR
(TOP VIEW OF IC)

8E-0138

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE
(TOP VIEW)*



ASYNCRONOUS INPUT: LOW INPUT TO CLEAR SETS Q_A, Q_B, Q_C AND Q_D LOW.

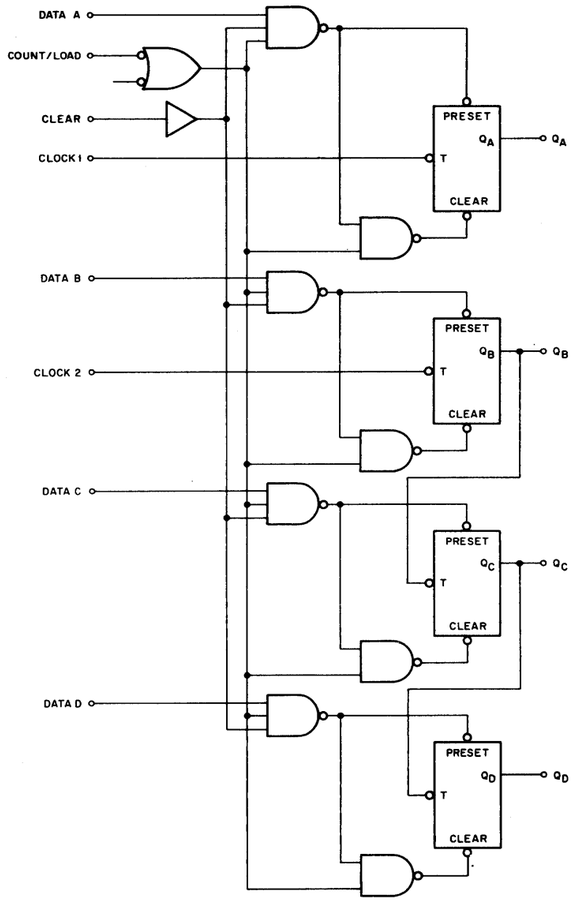
*Pin assignments for these circuits are the same for all packages.

11-0482

SN74197 TRUTH TABLE
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE A: Output Q_A connected to clock-2 input.



11-0481

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DEC-11-HDCD-D

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