EK-M8203-TM-002

M8203 Line Unit Technical Manual

digital

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Technical Manual

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PREFACE

The *M8203 Technical Manual* is a stand-alone document that describes typical line unit applications, circuit functions, and maintenance procedures based on a module replacement philosophy. Recommended cables and connectors, and installation considerations are provided in Appendix B. Detailed installation is provided in relevant systems documentation in which the line unit is implemented (such as the *DMP11-AD Technical Manual* – EK-DMP11-TM-001 or *DMR11 Technical Manual* – EK-DMR11-TM-002).

A Glossary of terms and abbreviations, selected integrated circuit descriptions, and microdiagnostic tests are also provided.

The following documents contain necessary reference information:

- *M8207 Technical Manual* (EK-M8207-TM-001)
- *M8207 Print Set* (D-CS-M8207-XX)
- *M8203 Print Set* (D-CS-M8203-XX)
- *DMP11-AD Technical Manual* (EK-DMP11-TM-001)
- *DMR11 Technical Manual* (EK-DMR11-TM-002)
- Electronic Industries Association (EIA) Specifications

CHAPTER 1
INTRODUCTION

1.1 PURPOSE

The M8203 is a high performance line unit designed for multipoint or point-to-point systems. The line unit is capable of cyclic redundancy check (CRC) or parity checking for both character and bit oriented protocols. Receive and Transmit Silos buffer the data to allow UNIBUS delays during transmission. However, for special bit and character oriented protocols, the line unit can be run without using the silos. Character oriented protocols use three types of error checking; CRC 16, even and odd, and vertical parity. The bit oriented protocols use two types of Comite Consultatif Internationale de Telegraphie et Telephone (CCITT) CRC 16 error checking; initialized to 0 and 1. Both protocols can be run without error checking for transparent or special operations.

1.2 DESCRIPTION

The M8203:

- is a full multilayer hex module containing three 40-pin berg connectors.
- has no cables permanently attached.
- contains three switch packs that must be set up when the module is installed.
- power consumption is +5V at 3 AMPS, +15V at 180 milliamps, and −15V at 150 milliamps.
- fits into any hex Small Peripheral Controller (SPC) slot or in a powered backplane (microprocessors are restricted to non-processor request (NPR) SPC slots DD11-C or D).
- is not a stand alone device; the line unit must be controlled by a microprocessor.
- provides no ac or dc loading to any UNIBUS signals.

All data going to the line must go through the Universal Synchronous Receiver/Transmitter (USYRT). Transmit and Receive Silos are used to interface between the USYRT and the microprocessor.

M8203 Features:

- Addressing – Addressed through the microprocessor IBUS and OBUS eight bit byte registers 10-17.
- Indirect Addressing – Used to address the USYRT; bypasses the silos and standard hardware to run special protocols and variable character length operations.
- Berg Port – The main interface to the microprocessor for all data and control of the line unit.

- Integral Modem - Runs at 56K bps, 250K bps, 500K bps, and 1M bps. (Integral Modem specifications are provided in Chapter 3, Technical Description.)
- Interfaces are listed in Table 1-1.

Table 1-1 M8203 Line Unit Interfaces

INTERFACE	SPEED	MODEM	CABLE
EIA RS-232-C* CCITT V.28/ISO 2110*	Up to 19.2K bps	Bell 208, 209	Panel Cable BC55C-10 Modem Cable BC05D-25
EIA RS-423-A Compatible with Federal 1030; CCITT V.10/ISO 4902 and X.26	Up to 56K bps†		Panel Cable BC55C-10 Modem Cable BC55D-33
EIA RS-422-A Compatible with Federal 1020; CCITT V.11/ISO 4902 and X.27	Up to 1M bps		Panel Cable BC55B-10 Modem Cable BC55D-33
CCITT V.35/ISO 2953	Up to 250K bps	Bell 500A	BCO5Z-25
INTEGRAL MODEM using Twinax/Triax	56, 250, 500K bps 1M bps	Integral	BC55A-10

*Drivers are protected to ±10 Volts not ±15 Volts
†Limited to 20K bps by RS-449 and 9600 bps by ISO 4902

1.3 MAJOR FUNCTIONAL AREAS

A simplified block diagram of the M8203 is provided in Figure 1-1. A brief description of the subject areas is as follows:

- INBUS Registers 10-17 Functions (as seen by the microprocessor):
  - Read data and status in the Receive Silo and Shift Silo
  - Microcode uses switches for line status (switches set up at installation time)
  - Receiver status
  - Status and control of the Modem Interface
  - Extended address bits
  - Maintenance functions
  - Full or half-duplex on all interfaces
- OUTBUS Registers 10-17 Functions (loaded by the microprocessor):
  - Load data and status into Transmit Silo and Shift Silo
  - Control transmit circuitry
  - Enable maintenance mode
  - Status and control of Modem Interface
  - Extended address bits
  - Load data into data registers (only in extended mode)
  - Maintenance functions
- Switch Packs:
  - Defined by microcode (see specific options manual)
- Receive Silo:
  - First in first out (FIFO) 64 × 12
  - Loaded from the USYRT via a crystal controlled sequencer.
- Transmit Silo:
  - FIFO 64 × 12
  - Loaded from the microprocessor

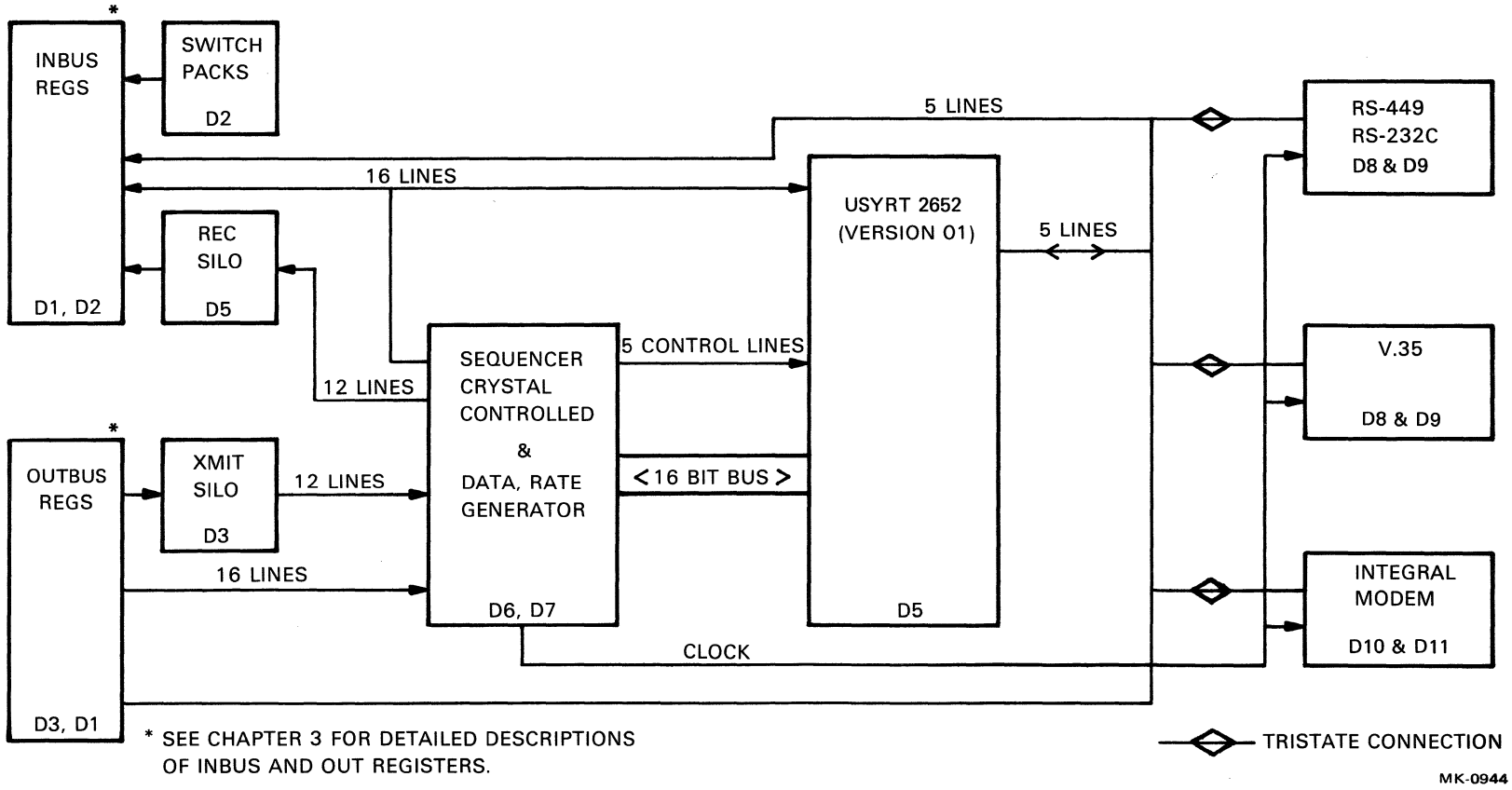


Figure 1-1 Major Functional Areas

- Sequencer:
  - Controls all data in and out of the USYRT and all clear functions on the module
  - Timing is controlled by a crystal (20 MHz for 100 ns increments)
- USYRT:
  - All received data to the line unit must go through the USYRT
  - Handles the basic protocol and error detection

    Character Oriented Protocol:

    1. Parallel to serial conversion
    2. Synchronous (Sync) character recognition and generation
    3. Sync character stripping
    4. CRC checking if enabled
    5. Vertical parity if enabled

    Bit Oriented Protocol:

    1. Parallel to serial conversion
    2. Zero stuffing (insertion) and stripping
    3. CRC checking if enabled
    4. Flag recognition and generation
    5. Abort recognition and generation
    6. Go-Ahead recognition and generation
- Modem Interface

  A summary of the Modem Interfaces is provided in this section. Detailed descriptions are contained in Chapter 2, Interface.

  - RS-449/International Standards Organization (ISO) 4902/CCITT V.24: Common interface defined by all Electronic Industries Association (EIA) interfacing cables used with RS-422-A and RS-423-A.
  - RS-232-C: EIA defined signals and characteristics for older modems (drivers are not protected from shorts to signals over 10 volts).
  - RS-422-A (Federal Standard 1020) (ISO 4902/CCITT V.11 and X.27): Differential balanced interface used in conjunction with RS-449.
  - RS-423-A (Federal Standard 1030) (ISO 4902/CCITT V.10 and X.26): Single-ended (unbalanced) signal levels used with RS-449 cables.
  - V.35: CCITT Standard/ISO 2593 Standard

- Integral Modem: Diphase-space modulation compatible with the DMC11 Integral Modem and the encoding/decoding of the DIGITAL DC017 IC chip.

  Transmitter output = 5.6 volts peak-to-peak minimum into a 30-ohm load.

  Receiver signal = 150mV peak-to-peak minimum @ 20% maximum distortion.

  Transformer coupled 500 volt common mode.

NOTE

Modules do not include any modem or Modem Interface cables.

1.4 M8203 LINE UNIT/MICROPROCESSOR INTERFACE

The M8203 Line Unit connects to the network via (1), the twinax or triaxial cables in local network applications or (2), the modems and common carrier facilities in remote network applications. The M8203 runs up to 1M bps on both Modem Interface and Integral Modems.

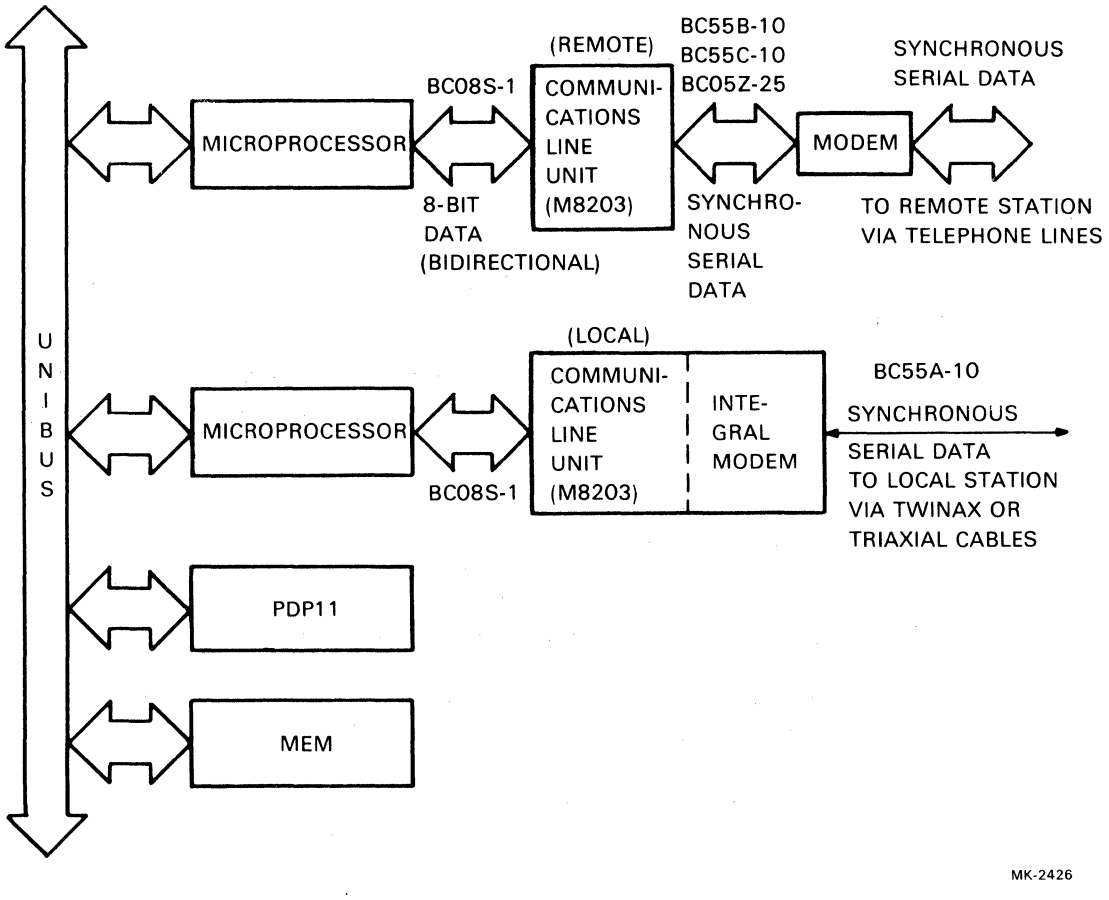


Figure 1-2 Typical PDP-11 Applications

Figure 1-2 shows typical PDP-11 local/remote applications, while Figure 1-3 illustrates similar VAX-11/780 applications. Local stations are connected by a single twinaxial or triaxial cable for half-duplex operation or two cables for full-duplex operation. Remote stations are connected via modems that use common carrier facilities.

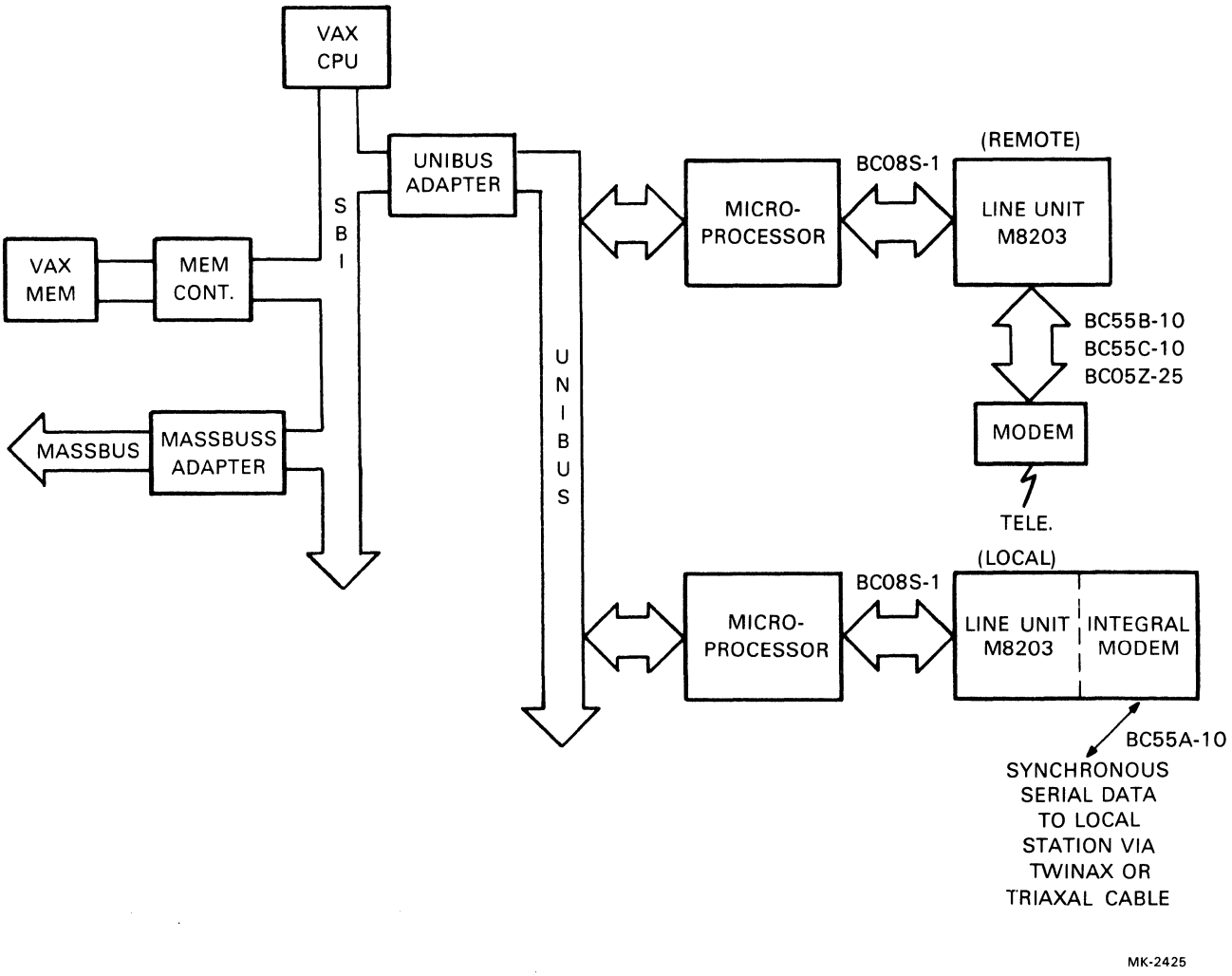


Figure 1-3 Typical VAX-11/780 Applications

CHAPTER 2
INTERFACE

2.1 SCOPE

The M8203 Line Unit is used in a wide range of synchronous communications applications. The M8207 or M8204 Microprocessors can be used with the line unit and can be programmed to handle a variety of protocols and interfaces. This section presents full and half-duplex connections, standard and special applications, compatible standards, and interfacing information.

2.2 FULL-DUPLEX/HALF-DUPLEX OPERATION

The M8203 Line Unit is capable of either full-duplex or half-duplex operation. The microprogram controls selection of half-duplex mode; the line unit controls and eliminates contention problems.

Operation of the M8203 Line Unit requires hardware considerations. The full-duplex operation requires two separate local link cables while half-duplex operation requires only one.

Although full-duplex operation requires two cables, it also provides full throughput potential. Half-duplex operation implies half the throughput potential but requires only one cable. The following questions should be considered when selecting full-duplex or half-duplex operation.

1. Traffic Flow – Is most of the data going one way or is data flow nearly equal in both directions?

2. Data Rate

   a. Is it necessary to use maximum data rate now and in the foreseeable future?

   b. Will the maximum data rate cause UNIBUS latency problems?

NOTE

Each UNIBUS system has a maximum Non-Processor Request (NPR) activity rate. Consider all NPR devices on the UNIBUS using the maximum activity rating.

3. Cable Expense – Is the two cable full-duplex operation worth the expense?

Wiring for half-duplex operation is done by connecting the transmitter and receiver together. A switch setting, defined by microcode, must be selected on the line unit to inform the microprocessor that the line unit is installed (Figure 2-1).

NOTE

Refer to the appropriate option Technical Manual for switch definitions and jumper configurations.

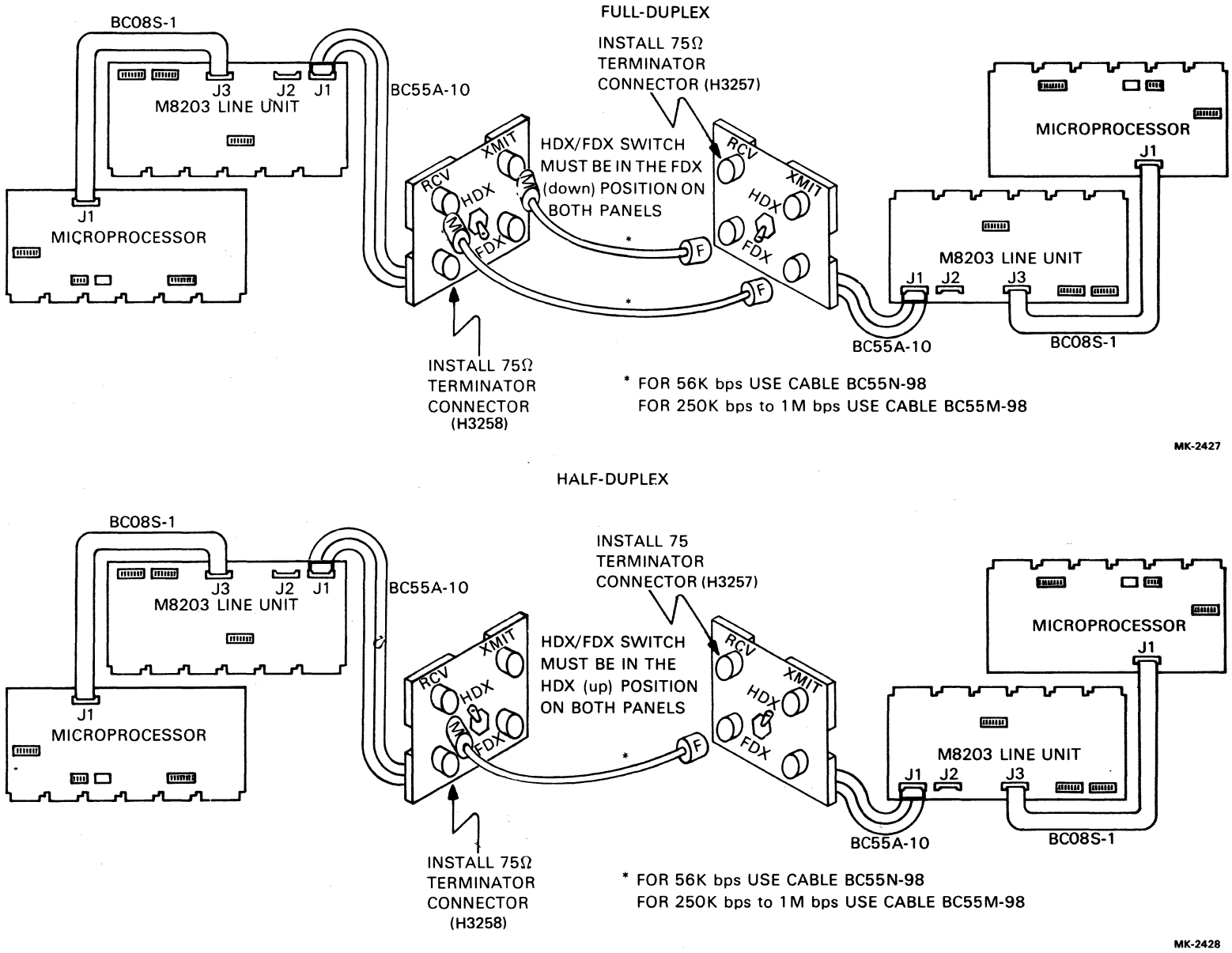
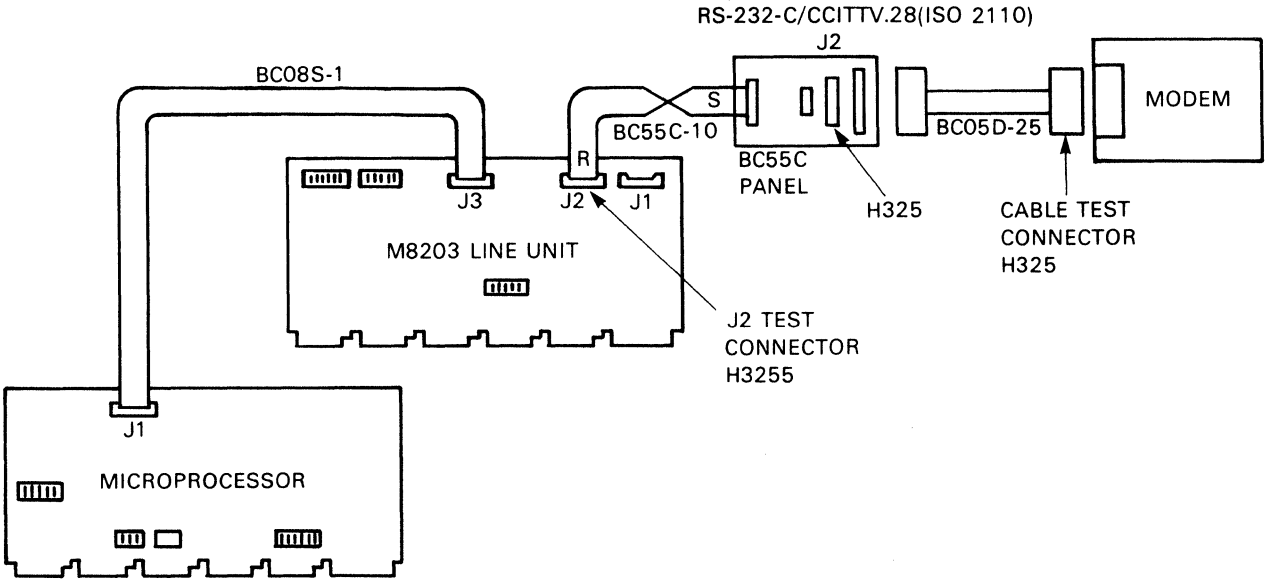


Figure 2-1 Full-Duplex/Half-Duplex Connections

2.3 STANDARD APPLICATIONS

The most common application is the Integral Modem which runs at four switch selectable speeds. The system should be designed in accordance with the guidelines provided in the description of the Integral Modem in Chapter 3, Technical Description.

There are three interfaces (RS-423-A, RS-422-A, and RS-232-C) that use RS-449 common interface and standard cables to meet Electronic Industries Association (EIA) specifications. See Figure 2-2 and Table 1-1.



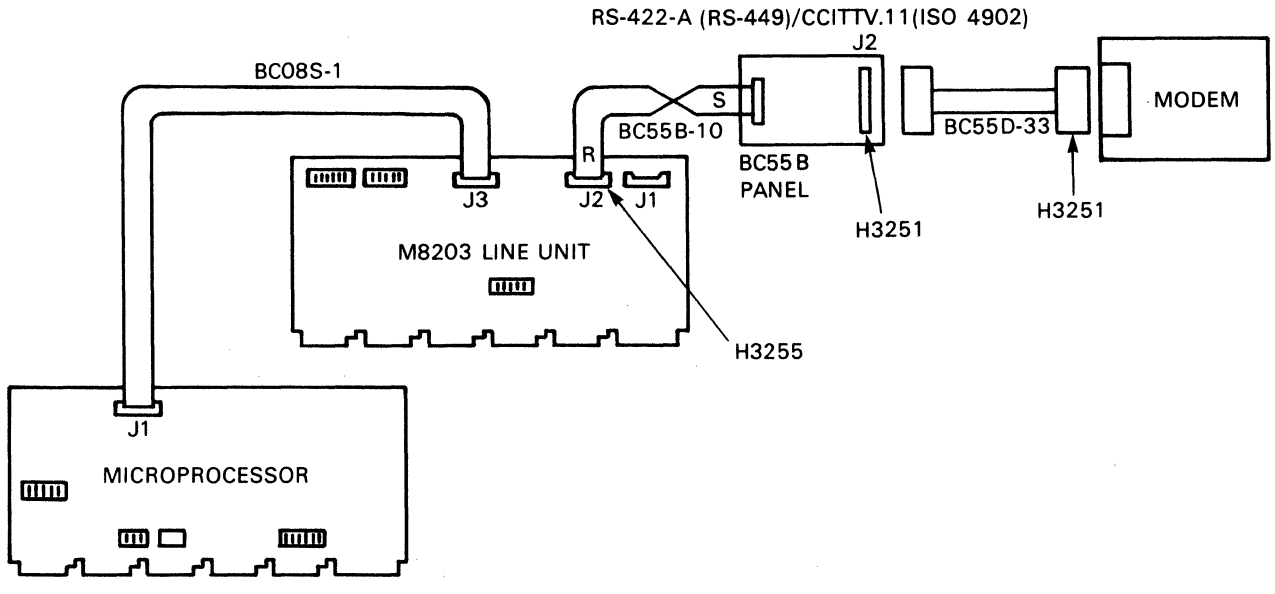


Figure 2-2 Standard (Common) Interfaces (Sheet 1 of 2)

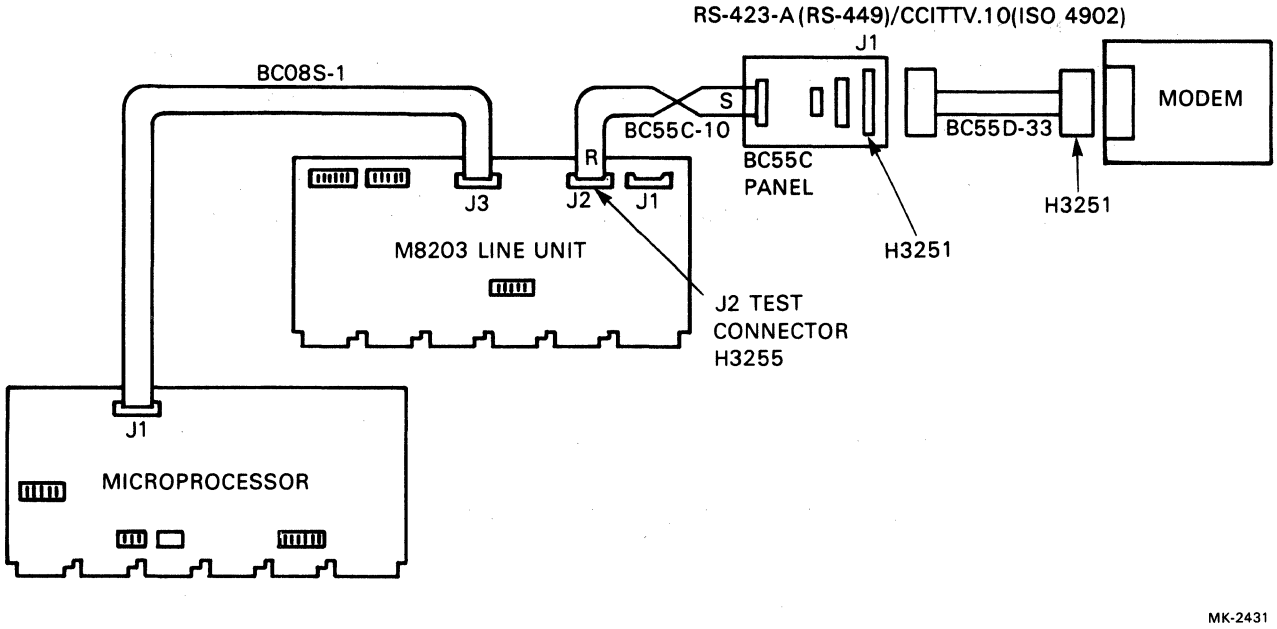


Figure 2-2 Standard (Common) Interfaces (Sheet 2 of 2)

2.4 COMPATIBLE STANDARDS

All cables used with the Modem Interfaces are described in the following sections and must be ordered separately. (See Figures 2-3 and 2-4.)

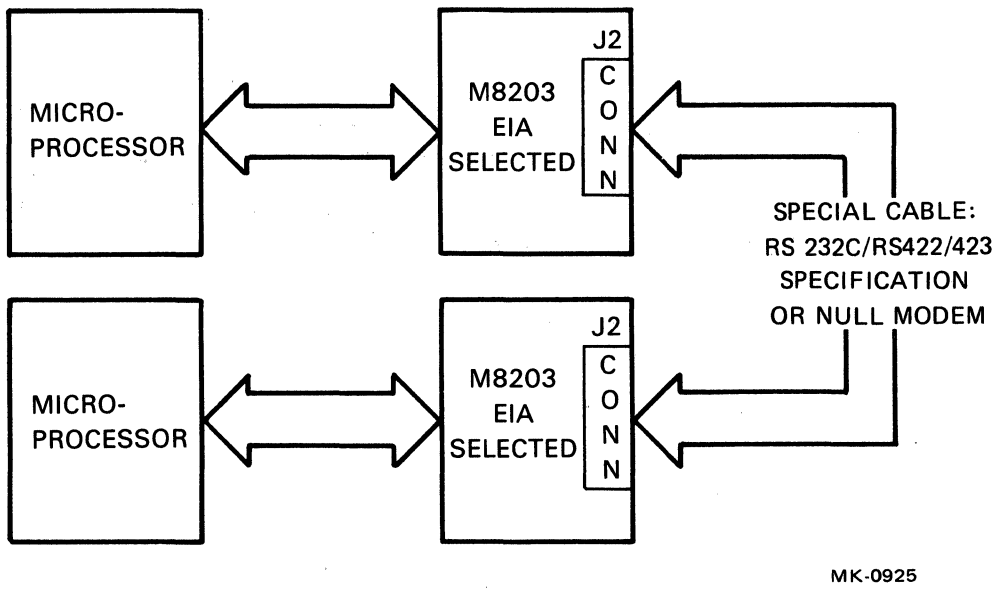


Figure 2-3 Special Application

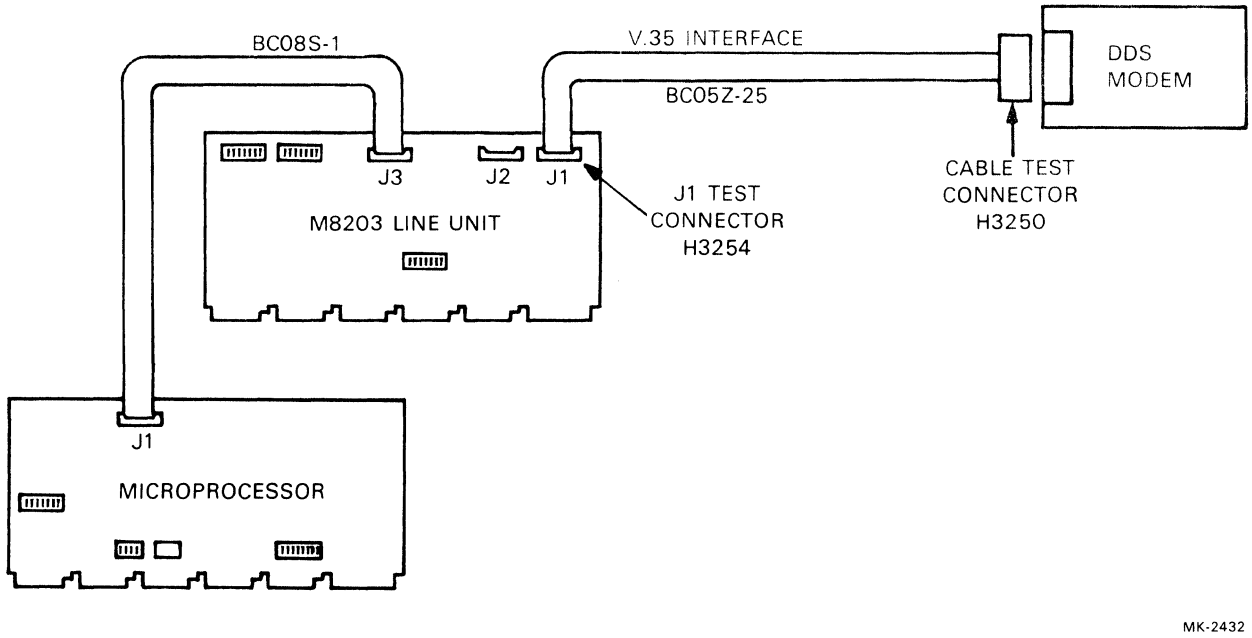


Figure 2-4 CCITT V.35 (ISO 2593) Interface

2.4.1 RS-232-C/CCITT V.28 (ISO 2110) Modem Interface

The RS-232-C interface uses the BC55C-10 panel cable, the BC05D-25 modem cable, and the H325 test connector or alternate. (See Figure 2-2.) M8203 implementation meets RS-232-C standards except driver protection against shorts to other lines over 10 volts and the drive impedance. RS-232-C states minimum drive impedance of 300 ohms without controlled rise and fall times. The new drivers have a 500 ohm impedance on the line accomplishing the same effect. A switch in the Modem Interface Selection Circuitry of the M8203 Line Unit (D7 of the *M8203 Print Set*) must be set to the single-ended output.

RS-232-C interfacing is limited to a maximum speed of 19.2K bps and is designed to interface to existing modems. The new EIA interface specifications RS-449 and RS-422-A/RS-423-A should be implemented.

The speed of the NULL clock is switch selectable and should not be set above 19.2K bps (see Section 3.5, Data Rate Generator). The maximum cable length for the RS-232-C interface is 15.24 meters (50 feet).

NOTE

1. **In some configurations, the BC05C-25 cable can be used in place of the BC05D-25 cable for RS-232-C applications. However, some options such as the DMR11 do not support using the alternate cable. Refer to specific options manual for use of the BC05C-25.**

2. **In configurations where the BC05C-25 cable is used, removal of certain M8203 jumpers may be necessary to ensure acceptable operation.**

Jumper	Condition
W7	**To disable Signal Rate (on some modems used as a test clock)**
W8	**To disable Data Mode– May cause problems with some modems where pin 18 is used for dibit clock**
W9	**To disable Null Clock– May cause problems with some modems**
W10	**To disable Terminal Ready– May cause problems with some modems where pin 10 is used for a negative test voltage**
W12	**To disable Terminal in Service – May cause problems on some modems**

2.4.2 EIA Standard RS-423-A

The RS-423-A is compatible with the Federal Standard 1030 and the Comite Consultatif Internationale de Telegraphie et Telephone (CCITT)V.10 and X.26/International Standards Organization (ISO) 4902. RS-423-A interface is single-ended and is subject to the RS-449 and Federal Standard 1031 interface with a new cable and test connector. Panel cable BC55C-10, modem cable BC55D-33, and test connector H3251 are used. The BC55C panel cable is a flat cable and the BC55D-33 modem cable is a round extension cable used for unprotected external runs.

A switch (E39-7) in the Modem Interface Selection Circuitry of the M8203 Line Unit (D7 of the *M8203 Print Set*) must be set to the single-ended mode. Signal levels are provided in Section 2.4.4. The maximum speed is limited to 56K bps by the rise time (limited to 20K b/s by RS-449 and 9600 b/s by ISO 4902). (Refer to the RS-423-A specification for more detail.) The maximum cable length is 60.48 meters (200 feet) as defined by the rise time used in the RS-423-A specification.

The RS-423-A interface standard specifies unbalanced circuits, but the M8203 uses a balanced differential receiver (26LS32) with a common return for improved performance at greater distances. The speed limitation of the M8203 electrical circuits under RS-423-A implementation without RS-449 implementation is limited to 56K bps which is imposed by software and other factors.

Applications using RS-423-A with RS-449 implementation are limited to a maximum speed of 20K bps and for ISO 4902 the speed is limited to 9600 bps.

2.4.3 EIA Standard RS-422-A

RS-422-A is compatible with Federal Standard 1020 and CCITT V.11 and X.27/ISO 4902. It is a differential interface and subject to EIA specification RS-449 and Federal Standard 1031 (signal levels are provided in Section 2.4.4). RS-422-A uses the panel cable BC55B-10, modem cable BC55D-33, and test connector H3251.

A switch (E39-7) in the Modem Interface Selection Circuitry of the M8203 Line Unit (D7 of the *M8203 Print Set*) must be set to the differential mode as defined in the RS-449 specification. The maximum data rate for the RS-422-A interface is limited to 1M bps by the line unit. The rise time is less than 200 ns. Maximum cable length is defined by RS-422-A.

The balanced circuits of RS-422-A use differential generators and receivers over a pair of wires for each signal. This type of circuit requires more wires in a cable to support all the signals, but only circuits that are speed sensitive generally use this interface standard. The circuits which are speed sensitive are defined as Category I type circuits under the RS-449 Interchange Standard, and those that are not speed sensitive as Category II type circuits. The speed sensitive circuits are data signals, timing signals, and any control signal that must respond quickly. These speed sensitive circuits (Category I type) usually implement balanced type circuits using the RS-422-A Electrical Standard. Terminating resistors (R_T) are used at the receiver to achieve top performance for distance and speed.

NOTE
Terminating resistors of 100 ohms are built into the BC55B-10 cable.

If properly terminated, the maximum cable length is 1.22 km (3865 feet); if terminating resistors are not used, the maximum cable length is 12.19 meters (40 feet).

2.4.4 EIA Standard RS-449

The RS-449 is compatible with CCITT Standards V.24, ISO Standard 4902, and Federal Standard 1031. RS-449 is used by all EIA interfacing cables, either single-ended or differential. The switch (E39-7) in the Modem Interface Selection Circuitry of the M8203 Line Unit (D7 of the *M8203 Print Set*) can be set to single-ended (unbalanced) or differential (balanced) mode with no interlock between the cable and the interface. The maximum speed for each EIA interface is specified in relevent sections of this manual and in more detail in the EIA specifications.

NOTE
EIA Specifications may be obtained from:

EIA Engineering Department
Electronic Industries Association
2001 Eye Street N.W.
Washington, D.C. 20006

RISE TIMES:

- Single-ended = 5 microseconds
- Differential = 200 nanoseconds

RISE TIME LIMITATIONS:

- Provides a means of calculating maximum cable length for use with each EIA interfacing level
- Rise times may be adjusted for specific variations of the M8203

CABLE LENGTHS:

- RS-232-C limited to 15.24 meters (50 feet) by specification
- RS-423-A limited to 60.48 meters (200 feet) by rise time

- RS-422-A must be terminated with a maximum limit of 1.22 km (3865 feet) if all the guidelines in the RS-422-A specification are followed
- Standard cables are all modem interfaces of 7.62 meters (25 feet) for older cables and 10 meters (33 feet) for new cables
- Special cable or NULL modem arrangements (Contact Computer Special Systems (CSS))

SIGNAL LEVELS (New RS-449 Specifications):

- Maximum output voltage = ±6 volts
- Minimum output voltage with no load = ±5 volts (single-ended outputs)
- A 450 ohm resistor used as a load will not drop the output voltage more than 10 percent
- The differential outputs maximum output = ±5 volts (referenced between the outputs with no load). With a balanced 100 ohm load, the output will not drop more than 10 percent
- The minimum output with no load = ±2 volts
- The balance error will not exceed 0.4 volts
- System ground differences cannot exceed 3 volts
- The output is protected to ±10 volts at 150 milliamps from voltages applied to the wrong pins when the modem is connected
- RECEIVE COMMON is tied to ground by a 100 ohm resistor for a fail-safe condition when no receiver ground is supplied to the interface
- SEND COMMON is tied directly to ground and is not current limited
- The shield grounds also tie directly to ground and are not current limited

The receivers are set up to accommodate differential inputs for the RS-422-A (see Section 2.4.3). Resistors are provided for fail-safe operation. The differential signals can be changed to single-ended (or when not connected) and allow the receivers to go to the fail-safe state. The receivers also go to the fail-safe state when power is off on the modem. The maximum signal off-set is 3 volts. The receivers can withstand a maximum voltage of plus or minus 25 volts without damage to the components. The operating range is ±15 volts. The RS-449 is a fail-safe interface when no signal is provided or the wire is open for that particular receiver. The Integral Modem Cable selects the interface when the cable is plugged in.

NOTE
The software is unable to tell if the cable is not connected or if the modem is not operating.

The M8203 reports that the RS-449 interface is enabled for either single-ended or differential mode. The RS-449 interface is made as fail-safe as possible. If a ground line or return line is open, there are pull-up resistors that compensate for the open-line. The signals received are pulled to a fail-safe state when power is off on the modem or when any of the lines except data and timing are open or left unterminated.

The M8203 supports the following RS-449 category 1 signals:

Circuit	Description
SD	Send Data
RD	Receive Data
TT	Terminal Timing (Null Clock)
ST	Send Timing
RT	Receive Timing
RS	Request to Send
CS	Clear to Send
RR	Receiver Ready (Carrier)
TR	Terminal Ready (Data Terminal Ready = DTR)
DM	Data Mode (Modem Ready)

These circuits are supported in differential and single-ended mode for RS-449. The receivers and drivers are all fail-safe circuits so the differential receivers handle single-ended lines. Drivers are selected by a switch and must match the interface cable.

2.4.5 CCITT V.35/ISO 2593

The V.35 interface uses the BCO5Z-25 cable and the H3250 test connector (the same connector used by the Integral Modem). When the cable is plugged in, a bit is set in the extended registers (see Chapter 3, Technical Description) that indicates that the V.35 mode has been selected. The maximum speed is 250K bps. The NULL clock is switch selectable from 2.4K bps to 1M bps (see Chapter 3, Technical Description).

2.5 INTERFACE SIGNALS

Table 2-1 lists all the signals handled by the standards described in the previous sections and the associated pins at the modem.

A list of interchange circuits showing the nearest equivalent RS-232-C, RS-449, and CCITT identification in accordance with recommendation V.24 is presented in Table 2-2. It should not be inferred that circuit definitions given are in exact accord with RS-232-C, RS-449, and CCITT recommendations.

2.6 ADDITIONAL LINE UNIT OPTIONS

The M8203 Line Unit is set up so the CRC 32 chip can be used with the Universal Synchronous Receiver/Transmitter (USYRT) by cutting four etches and installing the chip.

NOTE

This option must be factory installed. It may not be installed in the field.

2.7 HARDWARE VARIABLES

The M8203 contains three switch packs (E39, E121, and E134) and 17 jumpers (W1 through W17) which are used to select certain features and/or configuration variations. Some of these switches and

jumpers may be used differently in specific options such as the DMR11. For a more detailed description of each switch and jumper, refer to the specific options manual.

The purpose of this section is to identify each switch and jumper, and to provide a general description of each.

- Jumper Functions – Jumpers W1-W17 are used to select various interface standard parameters and modem interface signals, depending on application and modem type. Additional jumpers are available on the BC55C (panel) cable for additional interface signal selection.

- Switch Pack E39 Functions – This switch pack allows proper selection of interface driver and receiver control logic and different line speeds for various applications.

- Switch Pack E121 Functions – This switch pack is physically connected to internal registers. The function of each switch is microprogram dependent and may be different depending on the option selected. Refer to specific option manual for details.

- Switch Pack E134 Functions – This switch pack is physically connected to internal registers. The function of each switch is microprogram dependent and may be different depending on the option selected. Refer to specific option manual for details.

Table 2-1 Interface Signals/Pins at the Modem

SIGNALS	PIN AT MODEM			
		RS-449		
	RS-232-C	RS-423-A	RS-422-A	V.35
CLEAR TO SEND (+)	5	9	9	D
CLEAR TO SEND (−)		27	27	
DATA MODE (+)	6	11	11	E
DATA MODE (−) (Modem Ready)		29	29	
INCOMING CALL (Ring)	22	15	15	
LOCAL LOOP	18*	10	10	
NEW SIGNAL		34	34	
PROTECTIVE GROUND	1			
RECEIVE COMMON		20	20	
RECEIVE DATA (+)	3	6	6	R
RECEIVE DATA (−)		24	24	T
RECEIVER READY (+)	8	13	13	F
RECEIVER READY (−) (Carrier)		31	31	

*Selected by a jumper on the BC55C-10 cable.

Table 2-1 Interface Signals/Pins at the Modem (Cont)

SIGNALS	PIN AT MODEM			
		RS-449		
	RS-232-C	RS-423-A	RS-422-A	V.35
RECEIVE TIMING (+)	17*	8	8	V
RECEIVE TIMING (−)		26	26	X
REMOTE LOOP	21*	14	14	
REQUEST TO SEND (+)	4	7	7	C
REQUEST TO SEND (−)			25	
SELECT STANDBY		32	32	
SEND COMMON		37	37	
SEND DATA (+)	2	4	4	P
SEND DATA (−)			22	S
SEND TIMING (+)	15*	5	5	Y
SEND TIMING (−)		23	23	a

*Selected by a jumper on the BC55C-10 cable.

Table 2-1 Interface Signals/Pins at the Modem (Cont)

SIGNALS	PIN AT MODEM			
		RS-449		
	RS-232-C	RS-423-A	RS-422-A	V.35
SHIELD GROUND	1*	1*	1	
SIGNAL GROUND	7	19	19	A
SIGNAL QUALITY	21*	33	33	
SIGNAL RATE INDICATOR	23*	2	2	
SIGNAL RATE SELECT	23*	16	16	
STANDBY INDICATION	25*	36	36	
TERMINAL IN SERVICE	25*	28	28	
TERMINAL READY (+)	20	12	12	H
TERMINAL READY (−) (Data Terminal Ready = DTR)			30	
TERMINAL TIMING (+)	24	17	17	U
TERMINAL TIMING (−) (Null Clock)			35	W
TEST MODE	25*	18	18	

*Selected by a jumper on the BC55C-10 cable.

Table 2-2 Equivalency Table

EIA RS-449	EIA RS-232-C	CCITT RECOMMENDATION V.24	J2 BERG CONN PIN
	AA SHIELD GROUND		UU
SG SIGNAL GROUND	AB SIGNAL GROUND	102 SIGNAL GROUND	VV
	AA PROTECTIVE GROUND		A/B
SC SEND COMMON		102a DTE COMMON	A
RC RECEIVE COMMON		102b DCE COMMON	B
IS TERMINAL IN SERVICE			C
IC INCOMING CALL	CE RING INDICATOR	125 CALLING INDICATOR	X
TR TERMINAL READY (+)	CD DATA TERMINAL READY	108/2 DATA TERMINAL READY	DD
TR TERMINAL READY (–)			W
DM DATA MODE (+)	CC DATA SET READY	107 DATA SET READY	Z
DM DATA MODE (–)			U
SD SEND DATA (+)	BA TRANSMITTED DATA	103 TRANSMITTED DATA	F
SD SEND DATA (–)			KK
RD RECEIVE DATA (+)	BB RECEIVED DATA	104 RECEIVED DATA	S
RD RECEIVE DATA (–)			J

Table 2-2 Equivalency Table (Cont)

EIA RS-449	EIA RS-232-C	CCITT RECOMMENDATION V.24	J2 BERG CONN PIN
TT TERMINAL TIMING	DA TRANSMITTER SIGNAL ELEMENT TIMING (DTE SOURCE)	113 TRANSMITTER SIGNAL ELEMENT TIMING (DTE SOURCE)	L
TT TERMINAL TIMING (–)			EE
ST SEND TIMING (+)	DB TRANSMITTER SIGNAL ELEMENT TIMING (DCE SOURCE)	114 TRANSMITTER SIGNAL ELEMENT TIMING (DCE SOURCE)	N
ST SEND TIMING (–)			TT
RT RECEIVE TIMING (+)	DD RECEIVER SIGNAL ELEMENT TIMING	115 RECEIVER SIGNAL ELEMENT TIMING (DCE SOURCE)	SS
RT RECEIVE TIMING (–)			R
RS REQUEST TO SEND (+)	CA REQUEST TO SEND	105 REQUEST TO SEND	V
RS REQUEST TO SEND (–)			AA
CS CLEAR TO SEND (+)	CB CLEAR TO SEND	106 READY FOR SENDING	T
CS CLEAR TO SEND (–)			PP
RR RECEIVER READY (+)	CF RECEIVED LINE SIGNAL DETECTOR	109 DATA CHANNEL RECEIVED LINE SIGNAL DETECTOR	BB
RR RECEIVER READY (–)			H
SQ SIGNAL QUALITY	CG SIGNAL QUALITY DETECTOR	110 DATA SIGNAL QUALITY DETECTOR	MM

Table 2-2 Equivalency Table (Cont)

EIA RS-449	EIA RS-232-C	CCITT RECOMMENDATION V.24	J2 BERG CONN PIN
NS NEW SIGNAL			HH
SF/SR* SELECT FREQUENCY/ SIGNALING RATE SELECTOR	CH DATA SIGNAL RATE SELECTOR (DTE SOURCE	126 SELECT TRANSMIT FREQUENCY 111 DATA SIGNALING RATE SELECTOR (DTE SOURCE)	RR
SI SIGNALING RATE INDICATOR	CI DATA SIGNAL RATE SELECTOR (DCE SOURCE)	112 DATA SIGNALING RATE SELECTOR (DCE SOURCE)	Y
LL LOCAL LOOPBACK		141 LOCAL LOOPBACK	K
RL REMOTE LOOPBACK		140 REMOTE LOOPBACK	FF
TM TEST MODE		142 TEST INDICATOR	E
SS SELECT STANDBY		116 SELECT STANDBY	CC
SB STANDBY INDICATOR		117 STANDBY INDICATOR	M
DTE = Data Terminal Equipment DCE = Data Circuit-terminating Equipment			

* SF and SR share the same pin.

CHAPTER 3
TECHNICAL DESCRIPTION

3.1 SCOPE

The technical description and programming of the M8203 Line Unit Circuitry is presented at the functional level. The intent is to provide the Field Service representative with enough information to troubleshoot the line unit. Logic block diagrams supplement the text and make reference to the *M8203 Print Set* thereby providing the additional information required to troubleshoot to the gate level. Definition of the register bits and special chips may be useful to the programmer as well as the technician.

The major functional areas shown in Figure 1-1 are described in the following sections in the sequence given below.

- Berg Port Interface
- Silos
- Sequencer
- Data Rate Generator
- Universal-Synchronous Receiver/Transmitter (USYRT) Device
- Modem Interface
- Integral Modem

NOTE

D(x) references in the text are based on the signal map rather than actual sheet numbers of the *M8203 Print Set*.

3.2 BERG PORT INTERFACE

The Berg Port Interface has eight basic input and output registers expanded by second level addressing to eight more registers (See Figure 3-1).

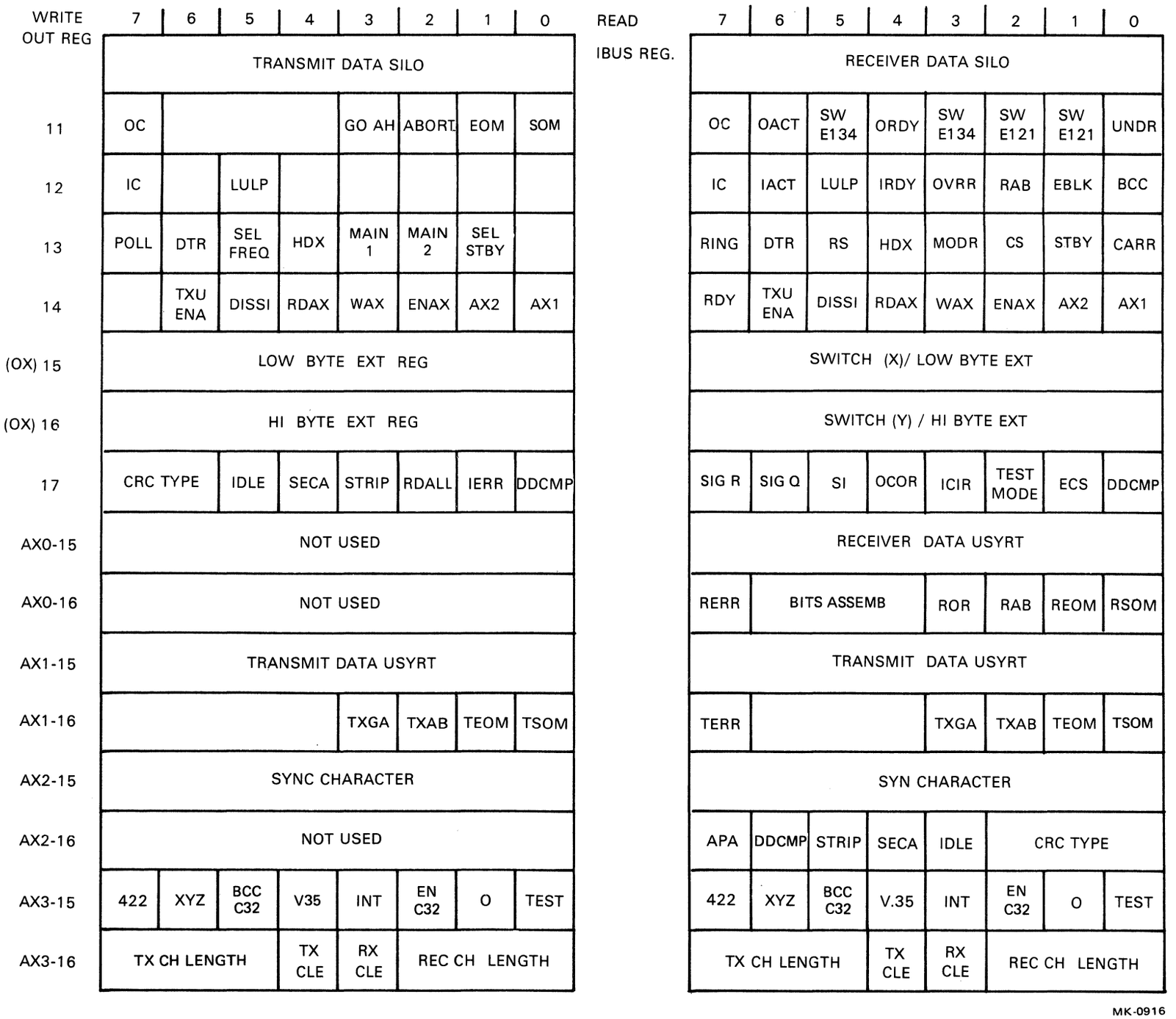


Figure 3-1 Input/Output Registers

INBUS/OUTBUS and INBUS*/OUTBUS* refer to two register groups or categories within, and accessed by, the microprocessor. This terminology is used in microinstruction formatting. It defines the group of registers to be accessed by the microprocessor and whether the particular register is used as a source or destination for data.

- The "*" indicates one register group; the absence of the "*" indicates the other register group.
- The "IN" portion of the term identifies the specific register as the data source.
- The "OUT" portion of the term identifies the specific register as the destination for data.
- The "BUS" portion of the term does not refer to a physical BUS.
- The following terms are synonymous:

  OUTBUS and OUT
  INBUS* and IBUS*
  OUTBUS* and OUT*
  INBUS and IBUS

Registers in the "*" group (IBUS*/OUT*) are located in the Microprocessor Multiport Random Access Memory (RAM):

CSR Bytes 0-7	(Registers 0 to 7 are R/W)
NPR Control	(Register 10 is R/W)
μP Miscellaneous	(Register 11 is R/W)

Registers in the INBUS/OUTBUS group located in the microprocessor:

IN DATA LB	Register 0 – R/W = Low Byte	DMA data from memory to the microprocessor
IN DATA HB	Register 1 – R/W = High Byte	
OUT DATA LB	Register 2 – R/W = Low Byte	DMA data from the microprocessor to memory
OUT DATA HB	Register 3 – R/W = High Byte	
IN BA <7:0>	Register 4 – R/W = Low Byte	DMA address for data from memory to the microprocessor
IN BA <15:8>	Register 5 – R/W = High Byte	
OUT BA <7:0>	Register 6 – R/W = Low Byte	DMA address for data from the microprocessor to memory
OUT BA <15:8>	Register 7 – R/W = High Byte	

Registers in the INBUS/OUTBUS group located in the line unit:

RECEIVER DATA SILO	Register 10 – Read = Receive Data FIFO
TRANSMIT DATA SILO	Register 10 – Write = Transmit Data FIFO
OUT CONT	Register 11 – R/W = Output Control
IN CONT	Register 12 – R/W = Input Control
MODEM CONT	Register 13 – R/W = Modem Control
SYNC REG	Register 14 – R/W = SYNC Character/Secondary Address
SW PACK (X)	Register 15 – Read only – Contents = Switch Pack X/Low Byte of Extended Register.
SW PACK (Y)	Register 16 – Read only – Contents = Switch Pack Y/High Byte of Extended Register.
MAINT REG	Register 17 – R/W = Maintenance

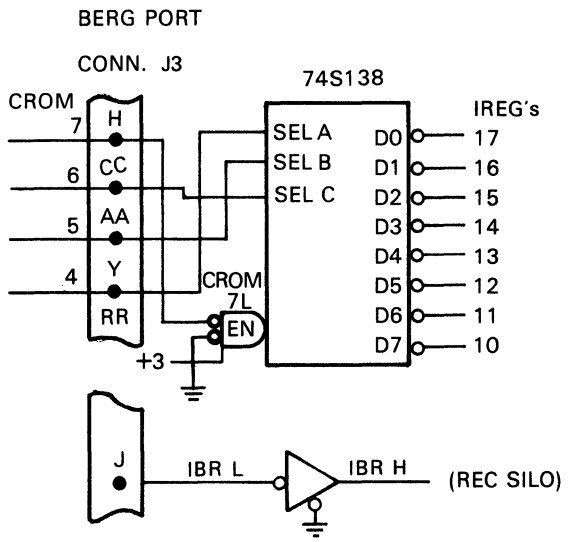
NOTE

1. **Address Extended (AX) registers are indirectly addressed by using AX1 and AX2 for address, Write to Extended registers (WAX) for write, Read to Extended registers (RDAX) for read, registers 15 and 16 for data, Enable Extended registers (ENAX) going to a one to start the operation, and Ready (RDY) to tell when the operation is complete.**

2. **The bit map as seen by the KMC11 and DMC11 Microprocessors.**

3.2.1 Read IBUS Registers

The line unit input registers are 12 tristate D-Type flip-flops (74LS374s). Extended registers are primarily used to load or verify USYRT registers. They can also be used for special protocols. IBUS and extended IBUS register selection is done by the microprocessor Control Read Only Memory (CROM) lines 4-7. The lines are decoded via a 74S138 decoder/multiplexer and used to enable the selected input register (See Figure 3-2). INBUS Read (IBR H) is used to shift data out of the receive silo (D5 of the *M8203 Print Set*).



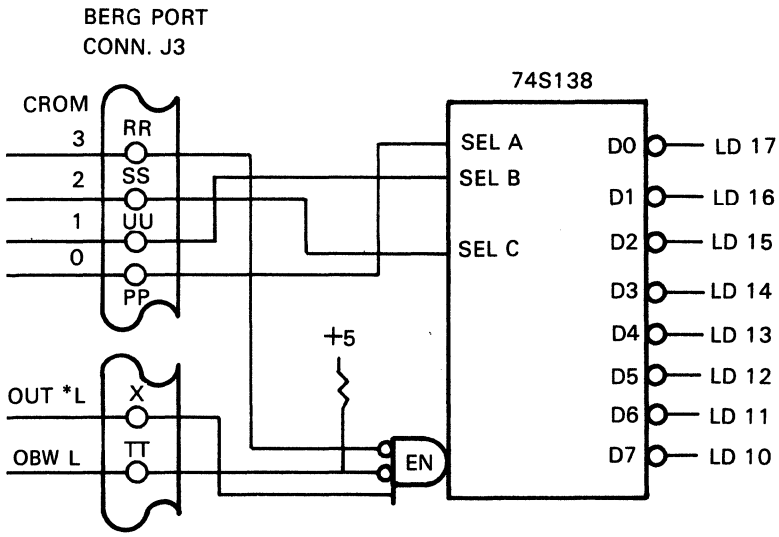
INPUTS		OUTPUTS
EN	SELECT C B A	IREG EN
0	0 0 0	17
0	0 0 1	16
0	0 1 0	15
0	0 1 1	14
0	1 0 0	13
0	1 0 1	12
0	1 1 0	11
0	1 1 1	10

MK-0924

Figure 3-2 IBUS Register Select

3.2.2 OBUS Registers

The buffered Arithmetic Logic Unit (ALU) lines from the microprocessor are inverted via a 74S240 then routed to the output register inputs. Selection of the output registers is done by the microprocessor CROM lines 3-0 which are decoded via a 74S138 decoder/multiplexer (See Figure 3-3). OUTBUS Write (OBWL) is used to gate the load pulse to the registers (D3 of the *M8203 Print Set*).



INPUTS		OUTPUTS
EN	SELECT C B A	OUT REG CLK
0	0 0 0	17
0	0 0 1	16
0	0 1 0	15
0	0 1 1	14
0	1 0 0	13
0	1 0 1	12
0	1 1 0	11
0	1 1 1	10

EN = OUT*L
OBW L
CROM 3 L

SELECT
CROM 2 = C
CROM 1 = B
CROM 0 = A

MK-0929

Figure 3-3 OBUS Register Select

3.2.3 IBUS/OBUS Registers Bit Descriptions

Figures 3-4 through 3-19 provide the input and output registers, bit descriptions, and qualifications for read and write operations.

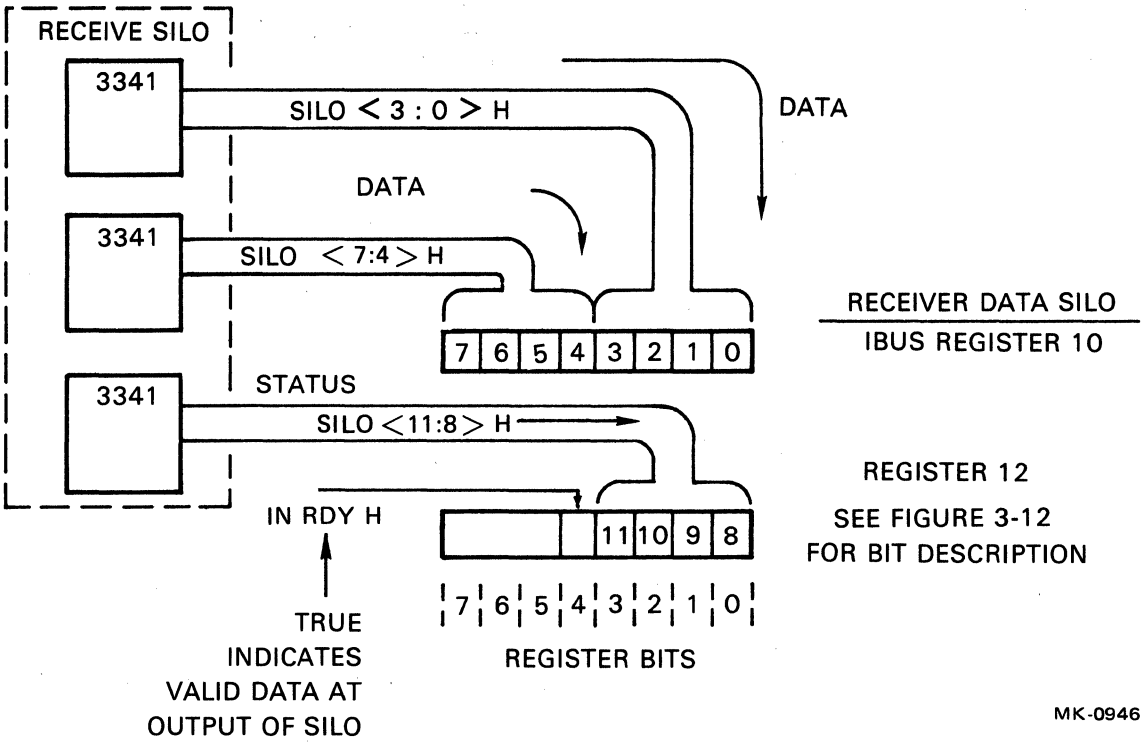


Figure 3-4 IBUS Register 10

Read Operation:

- Reads data in and shifts the silo.
- Status bits (register 12) are read first.
- Register 12 status bit 4, in RDY H, must be true before any data is read from the silo.

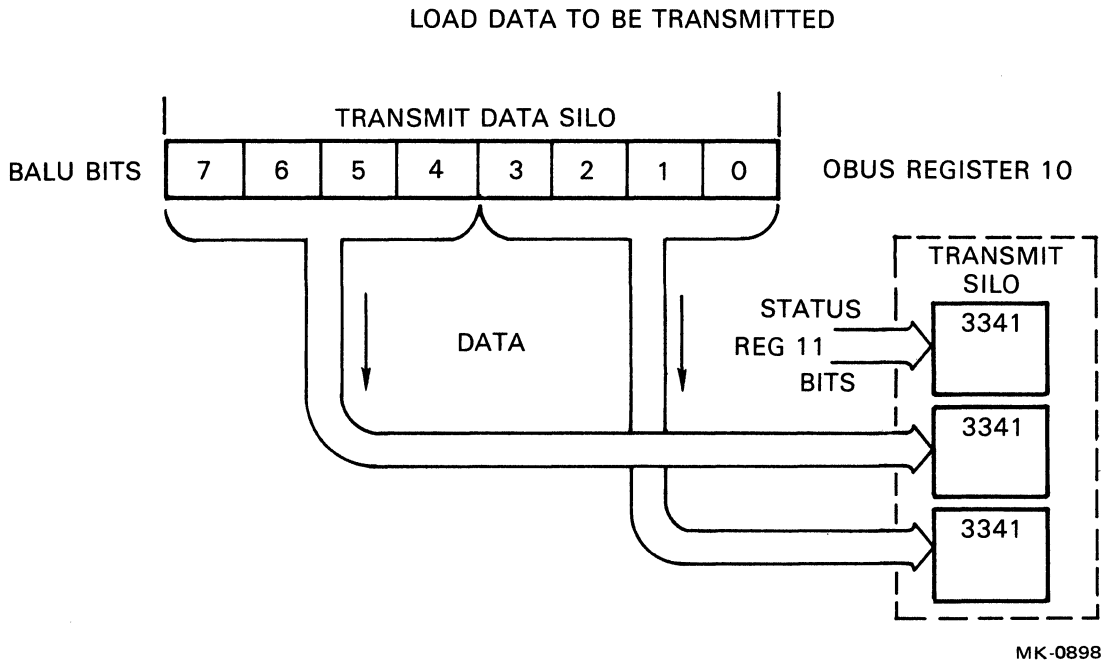


Figure 3-5 OBUS Register 10

Write Operation:

- Loads data to be transmitted into and shifts the silo.
- Status bits (BALU 3-0) from OBUS register 11 are also loaded into the silo when OBUS register 10 loads the silo. The status bits, if they are required, should be loaded first.
- All bits are cleared when the silo is shifted.
- Data should not be written into register 10 unless status Bit 4 of read IBUS register 11 (Out Ready) is set.

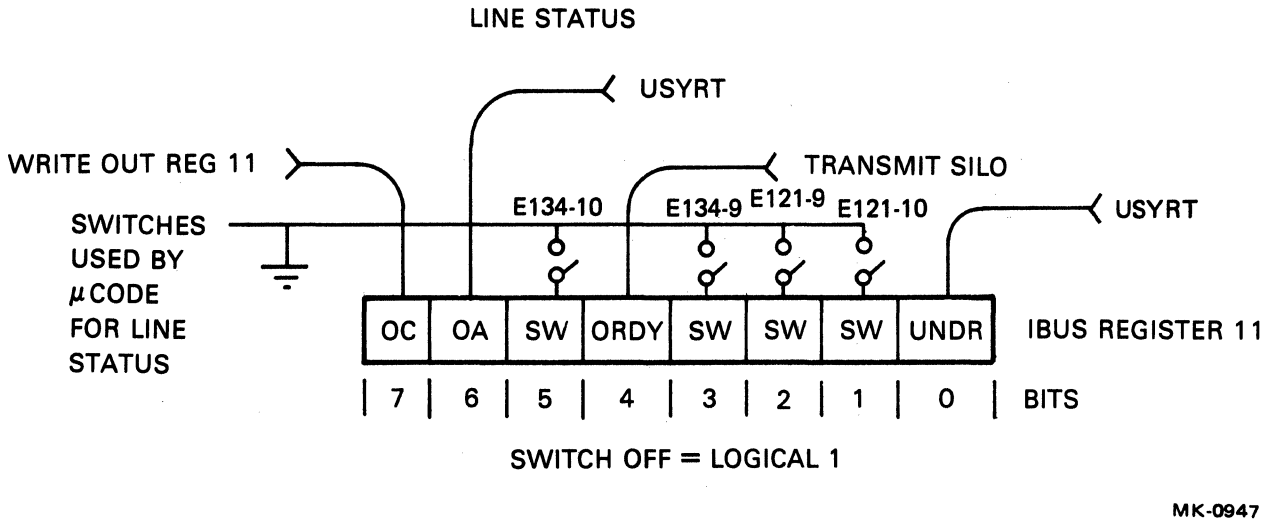


Figure 3-6 IBUS Register 11

Read Operation:

- Bits 1-3 and 5 (switch) have no hardware control. They should be set up when the module is installed in the field according to the customer link (the microcode and microprocessor used). Refer to the appropriate Options Technical Manual.
- Bit 0 = a transmitter underrun has occurred meaning characters have not been supplied to the transmitter fast enough, causing the USYRT to go to the IDLE state. (Can only be cleared by the next Start of Message (SOM) or by clearing the transmitter.)
- Bit 4 = Out Ready – the silo is ready for another character. If the silo is disabled, it indicates that the USYRT is ready for another character.
- Bit 6 = Out Active – the USYRT is in the process of transmitting data. If Out Active is set and Request to Send is not set, no characters are processed (check Modem Ready and Clear to Send bits in IBUS register 13).
- Bit 7 = Out Clear – transmitter is in the process of being cleared and should not be addressed. This bit must not be set until In Clear (IBUS register 12, bit 7) is clear; that is, Out Clear should not be set when an In Clear is in progress.

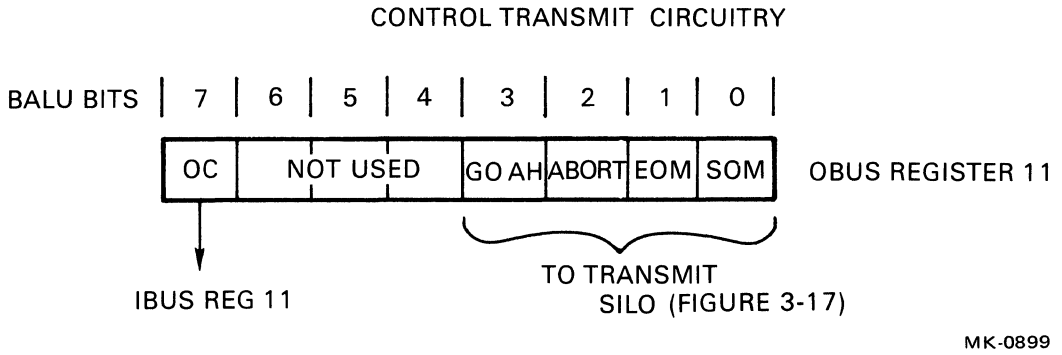


Figure 3-7 OBUS Register 11

Write Operation:

- Bits 0 to 3 are loaded into the silo before register 10 loads the silo and are used to transmit characters or cyclic redundancy check (CRC).

  Bit 0 = Start of Message (SOM) – used to transmit flags (01111110) in bit oriented protocols or is loaded with a sync character to set up the transmitter and receiver for data that is to follow.

  Bit 1 = End of Message (EOM) – used to send the CRC character, if CRC is enabled in both protocols, and the trailing flag or sync character.

  NOTE
  A minimum of two SOMs must be sent at the start of a character oriented message.

  Bit 2 = Send Abort – used in bit oriented protocol (11111111).

  Bit 3 = Send Go-Ahead – used in bit-oriented protocols only (01111111).

- Bit 7 = Clear the Transmit Circuitry – Out Clear (OC, IBUS register 11) must be 0 before loading the transmitter.

  NOTE
  If the transmit silo is full, the Out Clear function will not clear the transmitter.

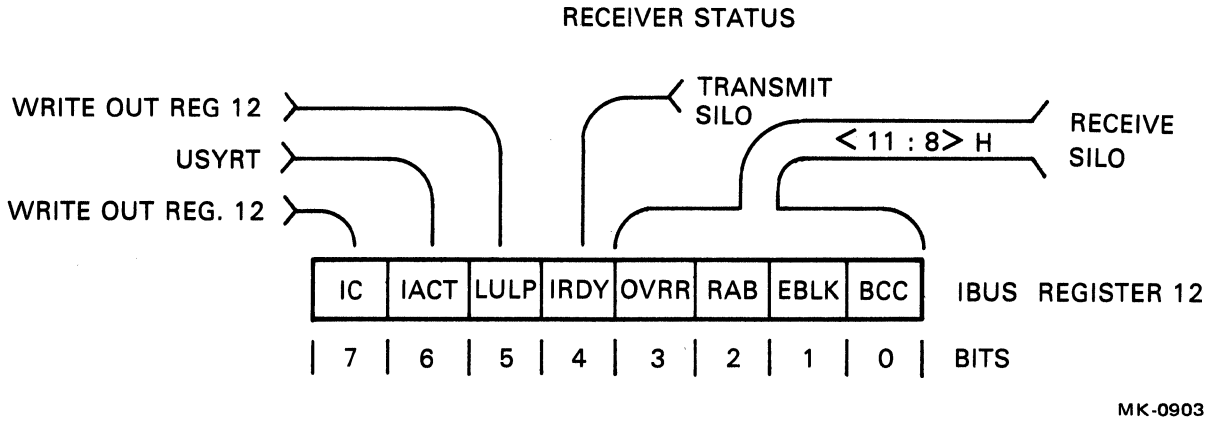


Figure 3-8 IBUS Register 12

Read Operation:

- Bits 0-3 = status of the USYRT (data character in IBUS register 10). When IBUS register 10 is read, bits 0-3 are updated to the next character.

  0 = Block Check Character (BCC) match – only valid at the end of the message or after the last data character (bit oriented protocol when EOM is set).

  NOTE

  BCC match is valid two characters before the previous DMC11 Line Units (M8201 and M8202).

  One = correct CRC or match in character oriented protocol.

  Zero = correct CRC or match in bit oriented protocol.

  Bit 1 = End of Block in bit oriented protocol – indicates End of Message & BCC match is valid.

  Bit 2 = Received Abort – bit oriented protocol, 7 ones received.

  Bit 3 = Receiver Overrun – data is not being removed fast enough from the receiver silo meaning data for this message is not valid and should be discarded. OVRR will clear when receiver is cleared (IC).

- Bit 4 = In Ready – the next character is ready to be read from the receiver silo. If the silo is disabled, a character is ready to be read from the USYRT.

- Bit 5 = Line Unit Loop – line unit is in maintenance mode and transmit data is being turned around in the USYRT.*

*Strictly internal to the USYRT; not to be confused with the line unit loop set in the microprocessor CSR 0 which is a loop back mode that is external to the USYRT. If RUN on the microprocessor:

(1) is set, the USYRT is run at 24K bps.
(2) is not set, the clock is generated from the Step Line Unit bit 12 of CSR 0.

- Bit 6 = Receiver Active – receiver has started to process data. The carrier bit M IBUS register 13 must be set or the receiver will not become active.

- Bit 7 = In Clear – receiver circuit of USYRT and the silos are in the process of being cleared.

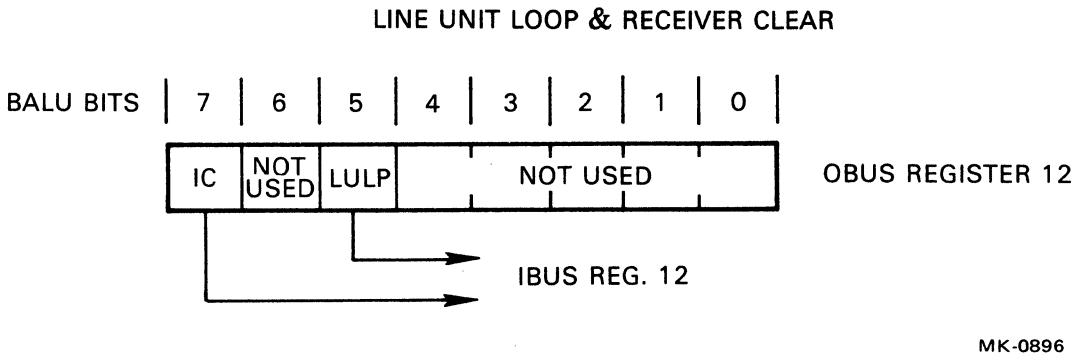


Figure 3-9 OBUS Register 12

Write Operation:

- Bit 5 = Line Unit Loop – enables the maintenance mode of the USYRT which loops the data back internally to the USYRT. Selects internal clock if RUN is set or Step Line Unit if RUN is not set.

- Bit 7 = Clear the Receiver Circuit of the USYRT (silos also cleared) – used to clear the receiver CRC in byte oriented protocol. In Clear must not be set until Out Clear (IBUS register 12, Bit 7) is clear; that is, In Clear should not be set when Out Clear is in progress.

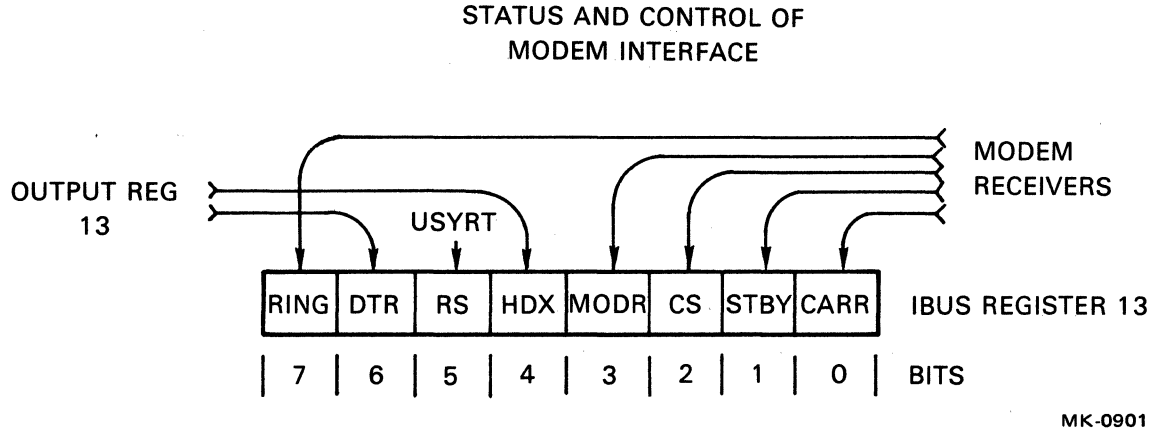


Figure 3-10 IBUS Register 13

Read Operation:

- Bit 0 = Carrier (Receiver Ready) – indicates that the Integral Modem or Modem Interface is active. The carrier signal must be set before the USYRT receiver processes characters. The carrier is used by the USYRT to clear the CRC registers between messages.
- Bit 1 = Standby – references standby indication from the modem (see EIA specification).
- Bit 2 = Clear to Send – a reply from the modem used by hardware to start sending data. Clear to Send must be low for Request to Send to set. With the Integral Modem, a 100 μs delay occurs before Clear to Send is set.
- Bit 3 = Modem Ready (Data Mode) – modem is in service. Used with Modem Interface and is a hardware lockout of Request to Send until modem ready is set (see EIA specification).
- Bit 4 = Half-Duplex – the line unit logic is set in the half-duplex mode.
- Bit 5 = Request to Send – the USYRT is ready to start transmitting data and will start as soon as Clear to Send is true. Request to Send does not set unless Out Active is set, Modem Ready is set, and Clear to Send is not set.
- Bit 6 = Data Terminal Ready (Terminal in Service) – signal to modem from the line unit indicating that the line unit is available and on line (see EIA specification).
- Bit 7 = Ring or Incoming Call – the modem has just been dialed and data is forthcoming (see EIA specification).

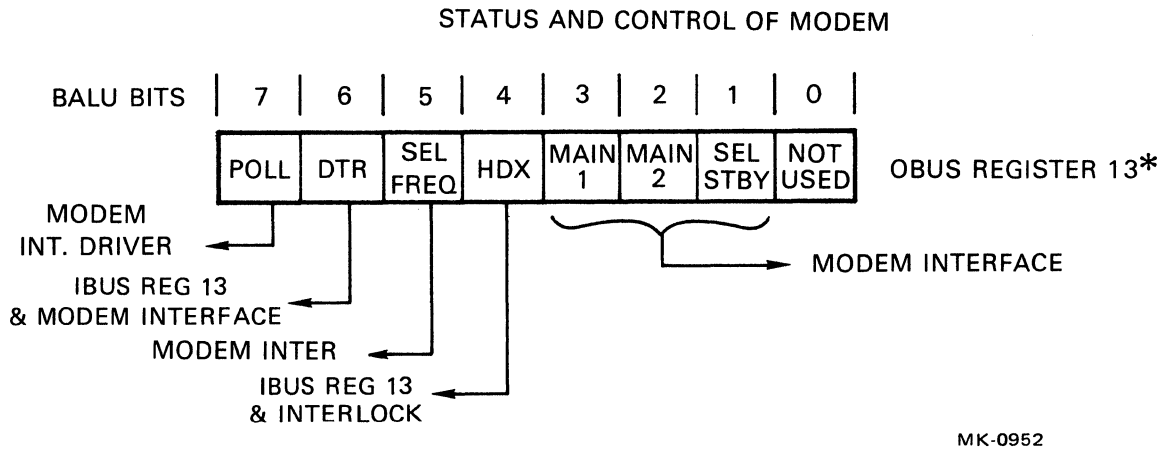


Figure 3-11 OBUS Register 13

Write Operation:

- Bit 1 = Select Standby when a modem interface is used (see EIA specification).
- Bit 2 = Maintenance Mode 2 – remote loopback using the modem interface and the external modem. It is used to test the modem (see EIA specification).
- Bit 3 = Maintenance Mode 1 – local loop using the Modem Interface and the external modem – tests the interface to the modem (see EIA specification).
- Bit 4 = Half-Duplex – sets the line unit in the half-duplex mode; the line unit either transmits or receives at any given time (hardware interlocked controlling the line unit).
- Bit 5 = Select Frequency – used on Modem Interface to change modem data rates (see EIA specification).
- Bit 6 = Data Terminal Ready (Terminal Ready) – indicates to the modem that the line unit is ready to receive or transmit data. It must be set when the Modem Interface is used, otherwise, the modem ignores other control signals from the line unit.
- Bit 7 = Polling – a new function for RS-422-A, RS-423-A, and RS-449 (not clearly defined). Intended for use with multidrop modems.

*For switched line booting, OBUS Register 13 is not cleared by a Master Clear or Initialize.

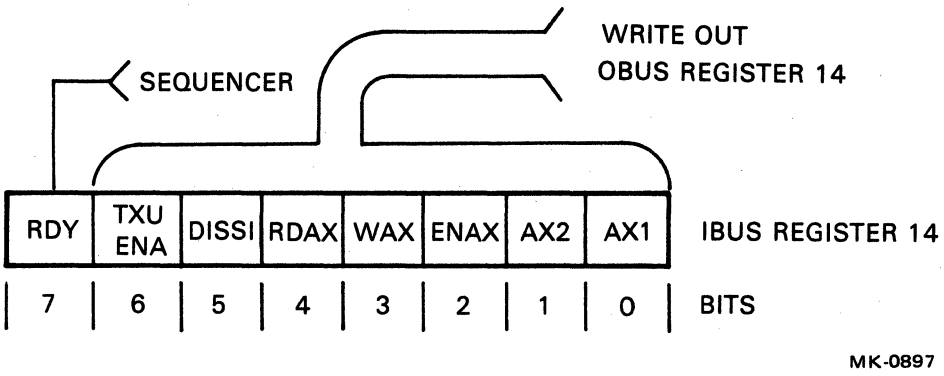


Figure 3-12 IBUS Register 14

Read/Write Operations:

NOTE

Sync character or secondary address must be loaded through the extended registers. Register 14 is used for extended register control (unlike previous DMC11 line units).

- Bit 0 = Extended Address Bit 1 – used to select the USYRT register that is being written to or read from.
- Bit 1 = Extended Address Bit 2.
- Bit 2 = enables the extended registers – starts the extended operation when set.
- Bit 3 = selects a write operation through the extended registers.
- Bit 4 = selects a read operation through the extended registers.
- Bit 5 = disables the silos so that the USYRT can be loaded and read directly.
- Bit 6 = Transmitter Enable – must be set before characters are loaded into the USYRT when the line unit is programmed with the silos disabled. When the silo is enabled, keeps Request to Send set.
- Bit 7 = Ready (Read only) – the operation executed through the extended registers is completed. Other bits in registers 14, 15, and 16 should not change unless the Ready bit is set.

The normal operation using extended registers:

- Extended address must be loaded first.
- If a write: data must be loaded in write out (OBUS) registers 15 & 16. Set WAX and the enable bit.
- If a read: Set RDAX and the enable bit.
- The operation is complete when Bit 7 becomes true.

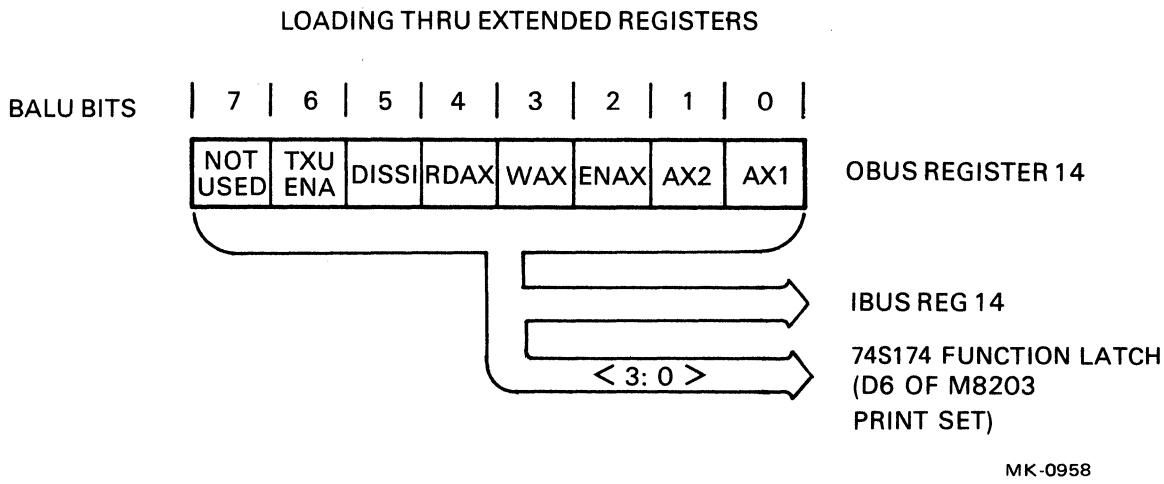


Figure 3-13 OBUS Register 14

Read/Write Operations:

Refer to Figure 3-13 for bit definitions.

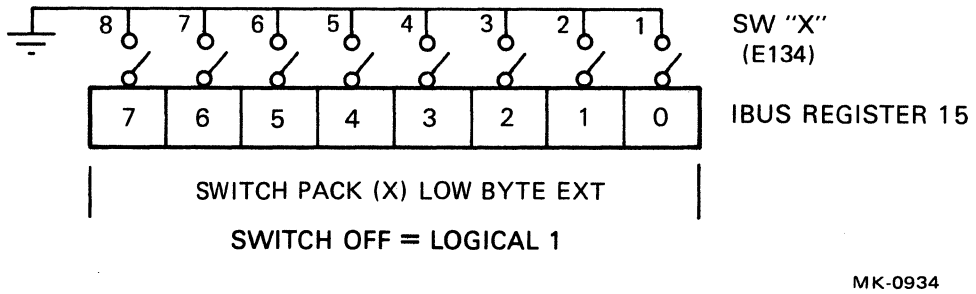


Figure 3-14 IBUS Register 15

Read Operation:

- A normal read from register 15 is a switch pack defined by microcode. Refer to the appropriate Options Technical Manual.
- In extended addressing mode, IBUS register 15 is the low byte of data read from the extended register defined by the extended address bits. (See Extended Register Description, Section 3.2.4.)
- The extended address data is only true when the relevant bits are set for the extended address and Bit 7 of register 14 is set. (See Extended Register Description, Section 3.2.4.)

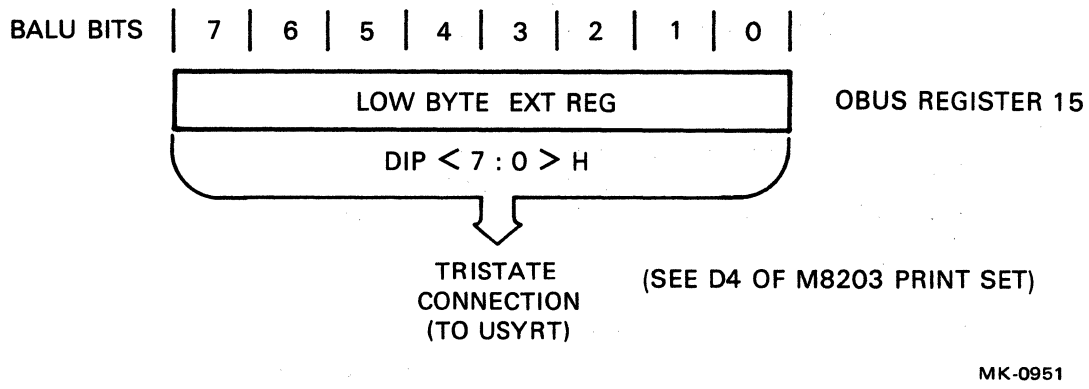


Figure 3-15 OBUS Register 15

Write Operation:

- A write to OBUS register 15 in normal mode is not valid.
- A write to OBUS register 15 is only valid in extended mode.
- Any write to OBUS register 15 is loaded in the extended data register (low byte), but data is not used until the extended address is set up and WAX and ENAX are set, except AX3-15, which must be selected before data is written into OBUS register 15.
- See Extended Register Description, Section 3.2.4.

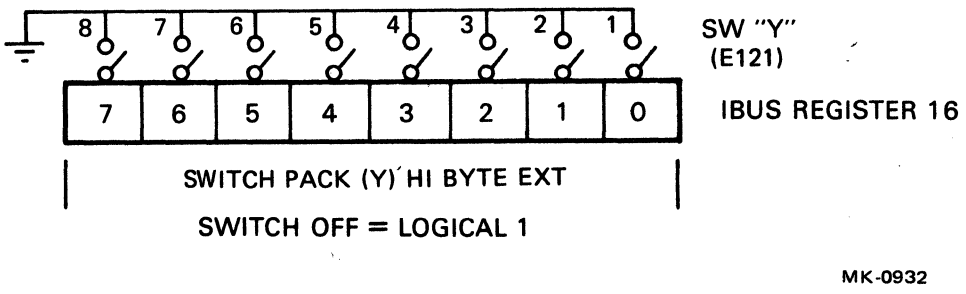


Figure 3-16 IBUS Register 16

Read Operation:

- Similar to Register 15.
- A normal read is from the switch pack defined by microcode.
- In extended mode, the register is the high data byte for extended addressing, whose data is only valid when Bit 7 of register 14 is set.
- Refer to Extended Register Description, Section 3.2.4.

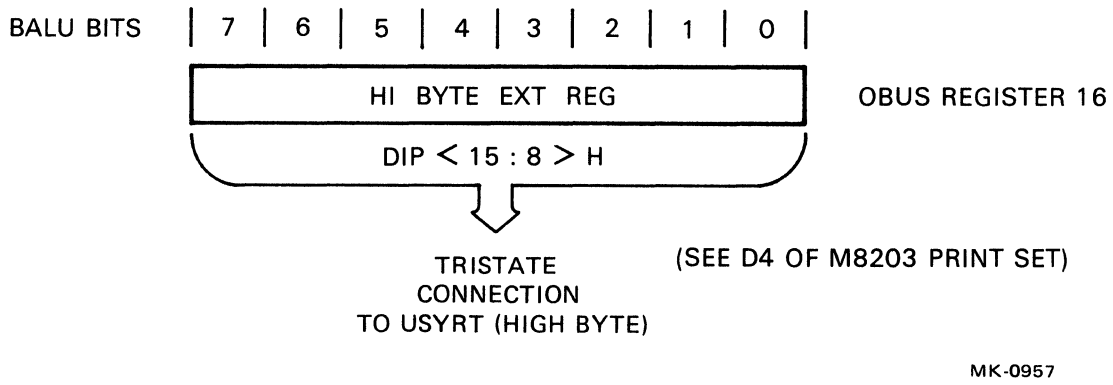


Figure 3-17 OBUS Register 16

Write Operation:

- A write to register 16 loads data only into the data register for the extended addressing function.
- The data is used after the address is set up and WAX and ENAX are set.
- Refer to Extended Register Description, Section 3.2.4.

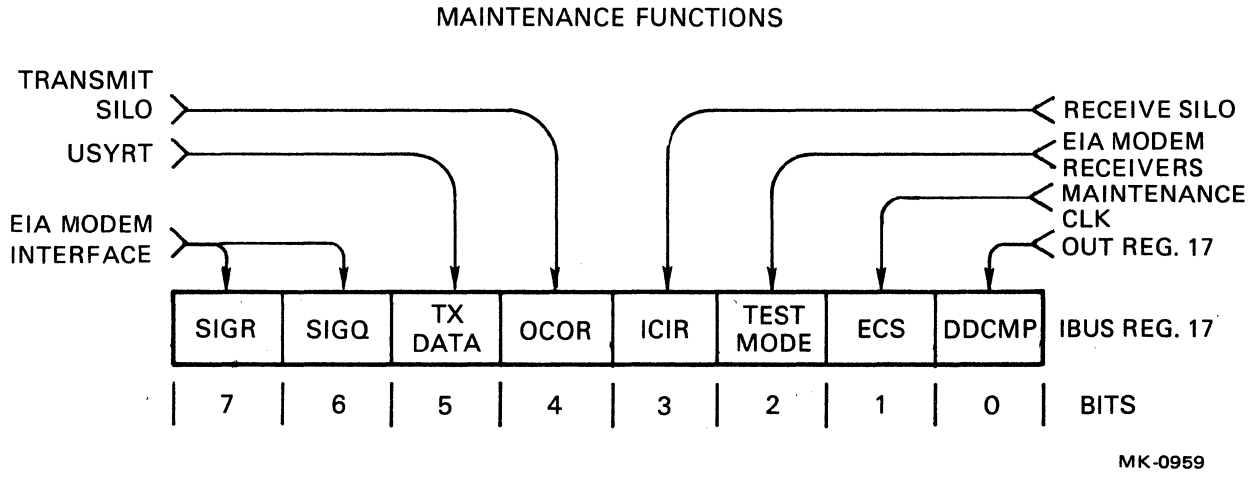


Figure 3-18 IBUS Register 17

Read Operation:

- Bit 0 = Line unit mode
  0 = Bit oriented protocol
  1 = Character oriented protocol (initializes to a 1).
- Bit 1 = Maintenance clock step line unit or 48 KHz.
- Bit 2 = Test mode, modem attached to EIA interface is in the test mode (see EIA specification).

- Bit 3 = In composite ready, the receive silos are ready to receive another character (maintenance mode only).
- Bit 4 = Out composite ready, data is present at the bottom of the transmit silo for transfer to the USYRT (maintenance mode only).
- Bit 5 = indicates that a data bit is present on the output of the USYRT serial data stream (maintenance mode only).
- Bit 6 = Signal quality indication from the EIA Modem Interface (see EIA specification).
- Bit 7 = Signal rate from EIA Modem Interface (see EIA specification).

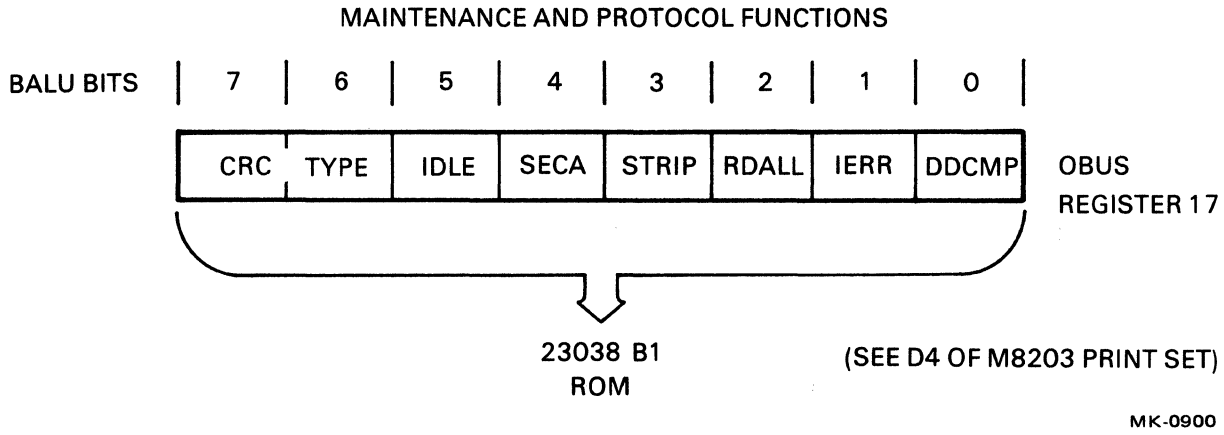


Figure 3-19 OBUS Register 17

Write Operation:

- Bit 0 = Mode of line unit – initializes to a 1.
  1 = Character oriented protocol
  0 = Bit oriented protocol
- Bit 1 = Insert error when line unit loop is set in microprocessor CSR; all bits are shifted into the USYRT when this bit is set to 1.
- Bit 2 = Read All Parties – used in bit oriented protocol; all parties address (11111111) and the normal secondary address.
- Bit 3 = Strip sync character in character oriented protocol after the first two characters.
- Bit 4 = Secondary address mode for bit oriented protocol. Enables auto detection of the secondary address and accepts messages with its secondary address or the all parties address if bit 3 is set.
- Bit 5 = Idle – Uses the 23038B1 ROM, which normally sets Idle in the USYRT (sync characters must be loaded by the microprocessor). With Idle clear the USYRT will MARK when underrun occurs.

- Bits 6 & 7 = Determine the type of error checking being used:

Bits 7 6	Character Oriented Protocol	Bit Oriented Protocol
0 0	CRC 16	CCITT 16 initialized to one
0 1	Odd vertical parity	CCITT 16 initialized to zero
1 0	Even vertical parity	Not used
1 1	No error checking	No error checking

Register 17 initializes to character oriented protocol with CRC 16.

3.2.4 Extended Registers/Indirect Addressing

Indirect addressing is used to address the USYRT directly, thereby bypassing the silos and standard hardware to run special protocols and variable word lengths. Indirect addressing is accomplished by setting up address AX in OUT/IBUS register 14, then the data in extended registers 15 and 16.

- Extended address must be loaded first.
- For a write operation, set Enable AX and WAX. Data must be loaded in OBUS registers 15 and 16.
- For a read operation, set Enable AX and RDAX.

When bit 7 of IBUS register 14 is set, the operation is complete.
Figures 3-20 through 3-27 provide the write IBUS/OBUS register bit descriptions and qualifications for read operations.

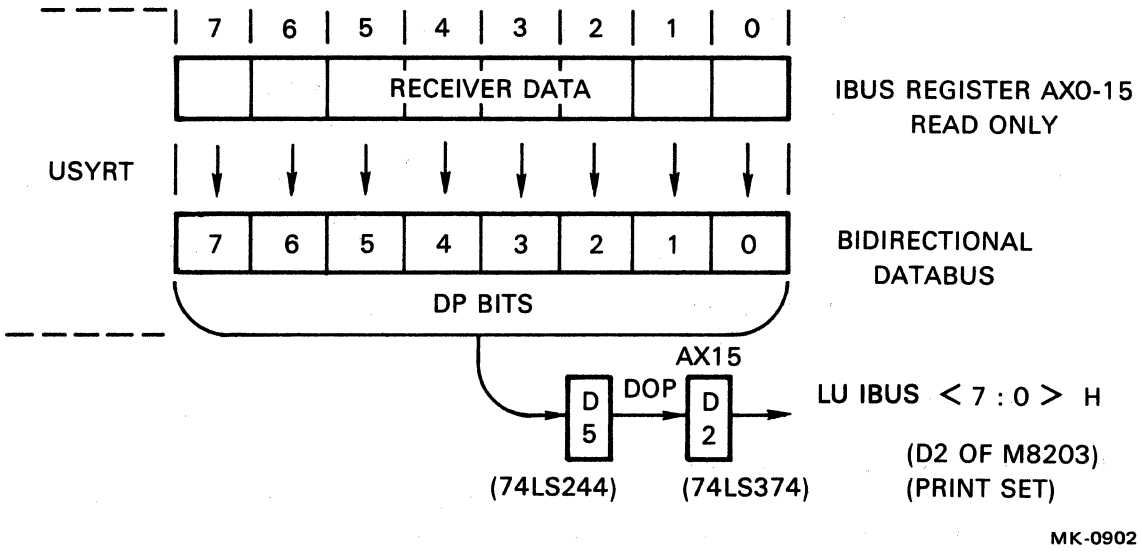


Figure 3-20 AX0-15 Register

Read only:

- Receiver data is directly from the USYRT.
- The silo must be disabled (DISSI must be set).
- Set RDAX and Enable AX.
- IBUS register 15 is the low byte of the data read from AXO-15 as defined by the extended address bits.
- The operation is complete when Ready bit 7 (IBUS register 14) becomes true.

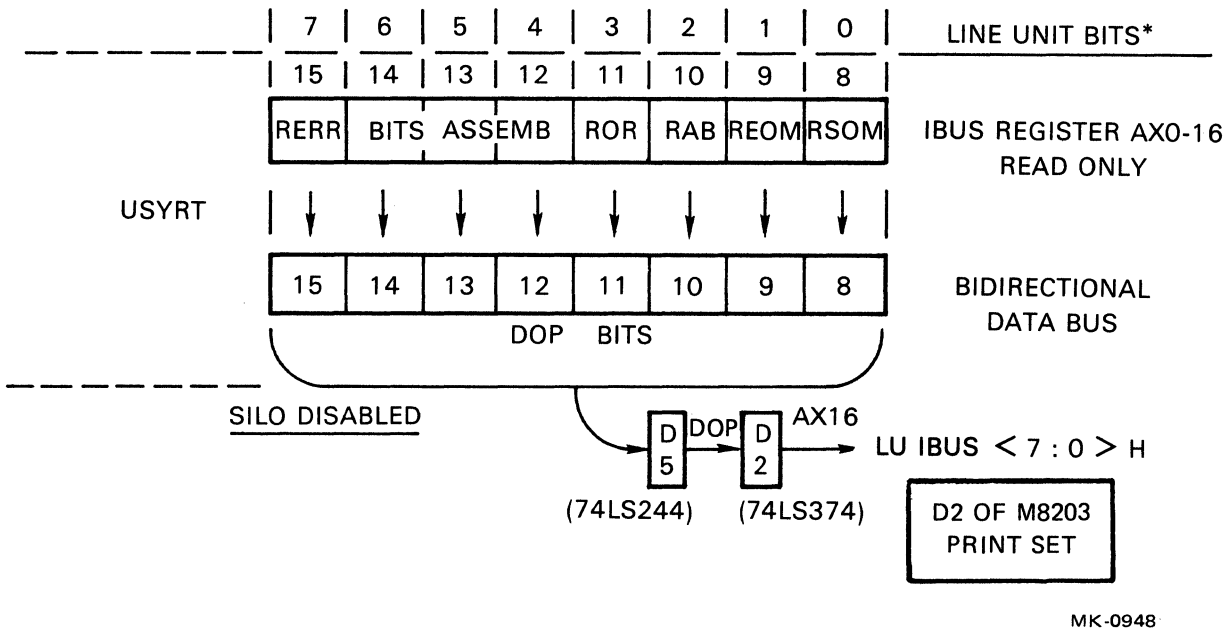


Figure 3-21 AX0-16 Register

Read only: Receiver status of each character from USYRT.

- Bit 0 = Received Start of Message (bit oriented protocol). A flag has been received followed by a non-flag character.
- Bit 1 = Received End of Message (bit oriented protocol). The closing flag has been received. The RERR bit is valid if CRC is enabled.
- **Bit 2 = Received Abort (bit oriented protocol). Seven or eight ones have been received. Invalid character in bit oriented protocol.**
- Bit 3 = Receiver Overrun (data is invalid, the message should be discarded indicating that the data characters have not been removed fast enough).
- Bits 4, 5, 6 = Number of bits assembled in the last data character when the closing flag was received (used in variable length bit oriented protocols).
- Bit 7 = Receiver Error (BCC match or parity error). Valid with the last character when CRC is enabled. A one indicates an error in bit oriented protocol.

*USYRT bits <15:8> are interpreted (seen) by the microprocessor as line unit bits <7:0>.

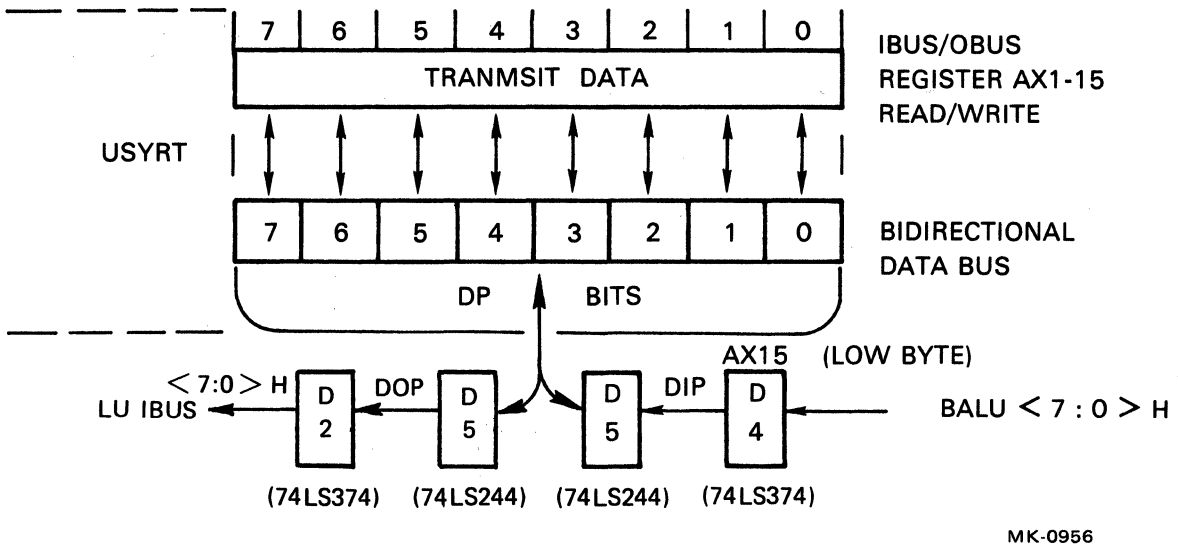


Figure 3-22 AX1-15 Register

Read/Write:

- Transmit data loaded into USYRT should only be used with the silos disabled (DISSI) and only read when the clock is disabled as a maintenance function.
- With the silos disabled, OUT RDY Bit 4 (ORDY) in IBUS register 11 indicates when the next register can be loaded into AX1-15.
- AX1-15 should not be read unless IN RDY Bit 4 of IBUS register 12 is set.
- IBUS register 16 is the high byte of the data read from AX1-15.

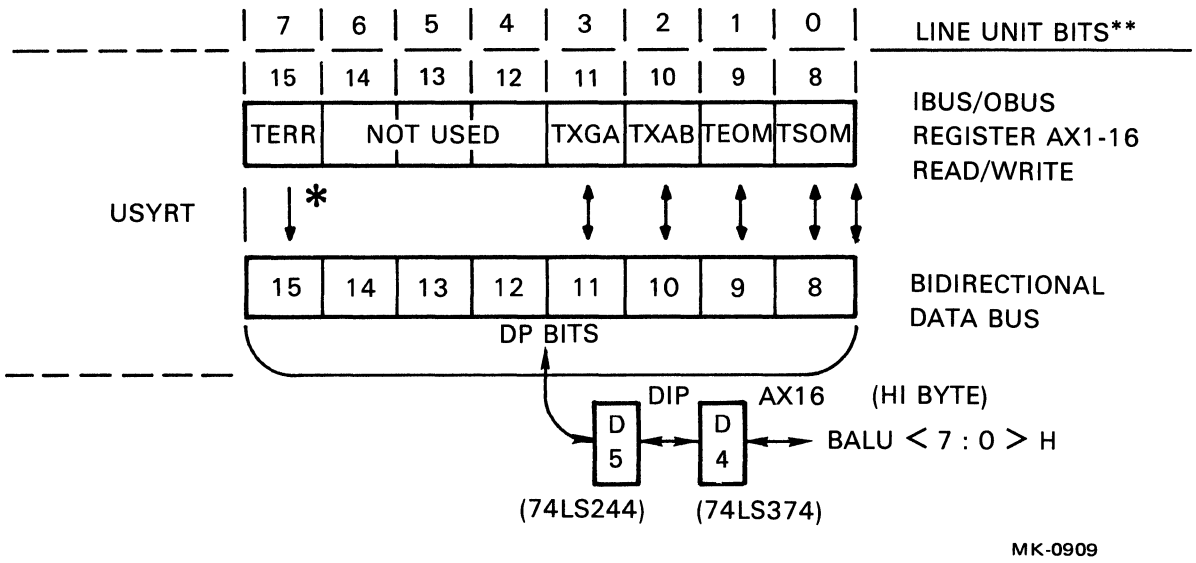


Figure 3-23 AX1-16 Register

Read/Write (Transmitter Control):

- Bit 0 = Transmit Start of Message generates sync or flag character and starts CRC calculation.
- Bit 1 = Transmit End of Message ends CRC generation, transmits CRC 16-bit character and flag or sync character.
- Bit 2 = Transmit Abort, (bit oriented protocol) transmits an abort character if IDLE Bit 5 of OBUS register 17 is cleared, or a flag character if IDLE is set.
- Bit 3 = Transmit Go Ahead; special for bit oriented protocol (0111111).
- Bit 7 = Transmitter Underrun (read only). Characters have not been supplied to the transmitter fast enough.

*READ ONLY
**USYRT bits <15:8> = line unit bits <7:0> as seen by the microprocessor

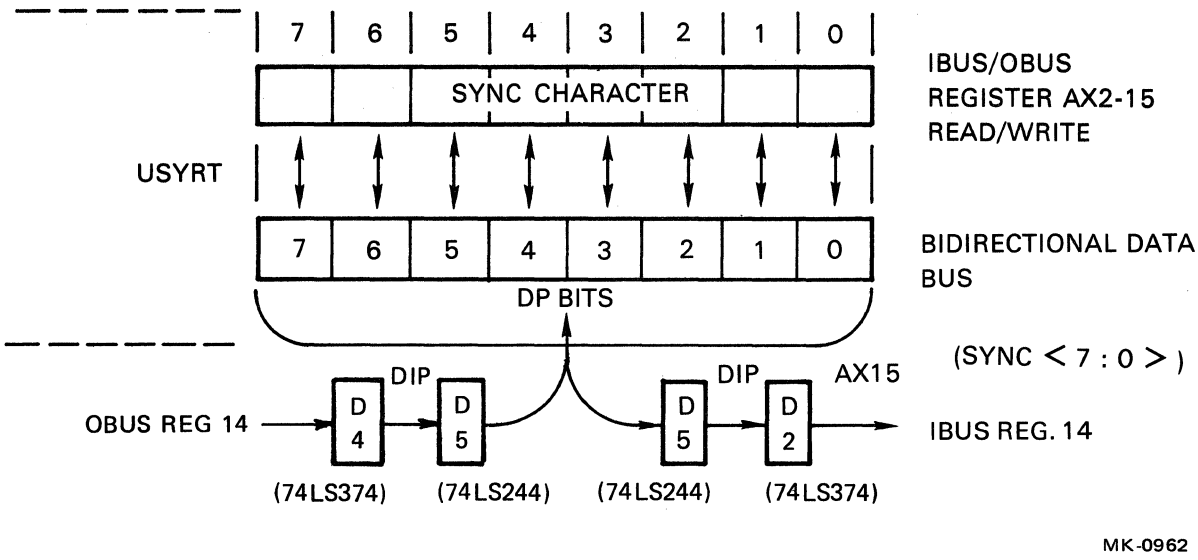


Figure 3-24 AX2-15 Register

Read/Write:

- Sync character in character oriented protocol or secondary address for bit oriented protocol.

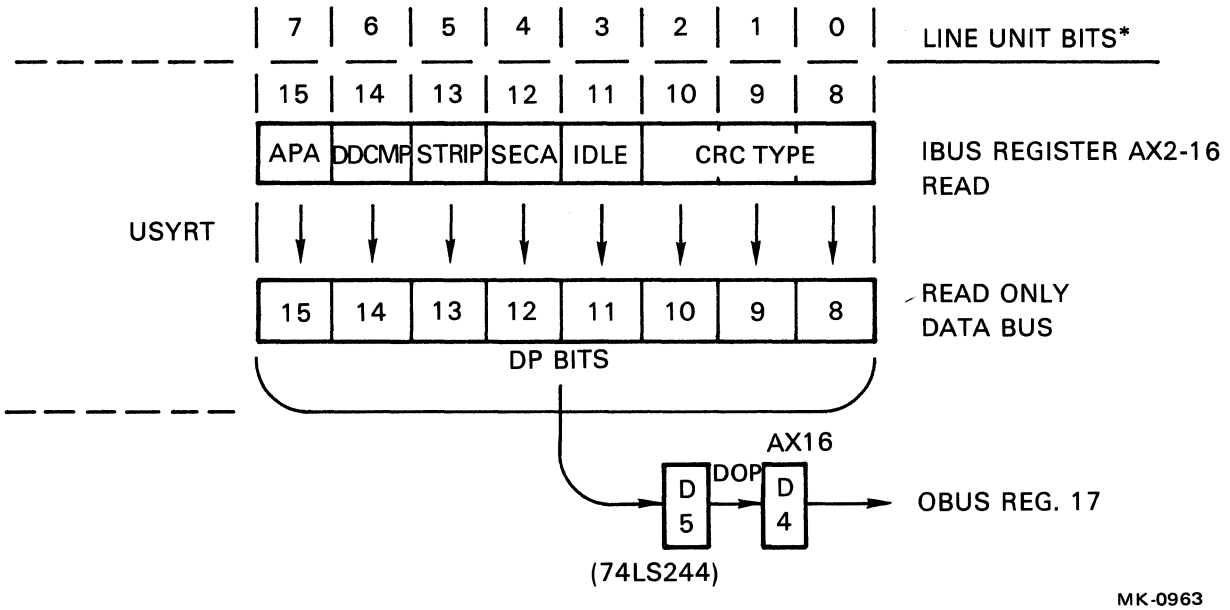


Figure 3-25 AX2-16 Register

Read: (Functions set via OBUS register 17)

- Bits 2, 1, 0 = CRC/Error Checking

*USYRT bits <15:8> = line unit bits <7:0> as seen by the microprocessor.

Bits 2 1 0	Character Oriented Protocol	Bit Oriented Protocol
0 0 0	-	CCITT 16 initialized to a one.
0 0 1	-	CCITT 16 initialized to a zero.
0 1 0	Not used	Not used.
0 1 1	CRC 16	-
1 0 0	Odd parity	-
1 0 1	Even parity	-
1 1 0	Not used	Not used.
1 1 1	No error checking	No error checking.

- Bit 3 = Idle: Determines what will be sent when an underrun occurs or when Transmit Abort Bit 2 of AX1-16 is set (0 = marks are sent, 1 = flags or syncs are sent in transparent modes, usually run with CRC disabled).
- Bit 4 = Secondary address enable for bit oriented protocol.
- Bit 5 = Strip sync characters for character oriented protocols.
- Bit 6 = 1 for character oriented protocol
  = 0 for bit oriented protocols.
- Bit 7 = Receive all parties (SEC address 377).

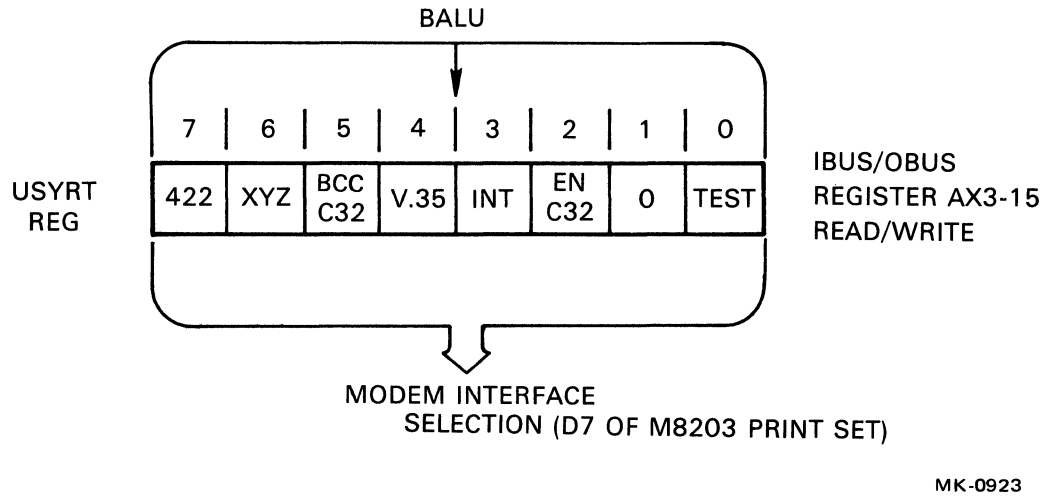


Figure 3-26 AX3-15 Register

Read/Write:

AX3-15 is a test register for the Modem Interface and does not affect the USYRT. This register is used only for maintenance purposes. When addressing this register do not set WAX or RDAX. It is used to:

1. Read which interface is selected, or

2. Select the interface when test connectors are used.

   - Bit 0 = Select Interface Bit; when a 1, the Modem Interface is selected by other bits in the register (via 74LS157-D7 of the *M8203 Print Set*). Used when H3254 and H3255 test connectors are installed.
   - Bit 1 = Reserved.
   - Bit 2 = Enables CRC 32 chip if installed (E124).†
   - Bit 3 = Integral Modem has been selected.*
   - Bit 4 = V.35 Interface selected by appropriate cable if bit 0 is not set (BCO5Z cable is connected to J1 connector) or if bits 0 and 4 are set (diagnostic selection).
   - Bit 5 = Enables CRC 32 BCC match, if installed.†
   - Bit 6 = EIA single-ended (unbalanced) interface (includes RS-232-C and RS-423-A; default when bit 0 is not set; true when bits 0 and 6 are set).
   - Bit 7 = RS-422-A Differential (balanced) Interface – must be switch selected in normal mode.

NOTE
Selects the maintenance function when bit 0 is set and read back true for the function selected.

*Bit 3 – Write when bit 0 is set, selects the Integral Modem. Does not select speed or filter for the Integral Modem. The proper cable or test connector must be used and correct data rate must be selected by switch pack number E39, switches 8, 9 and 10.

†All bits are active low except bits 2 and 5.

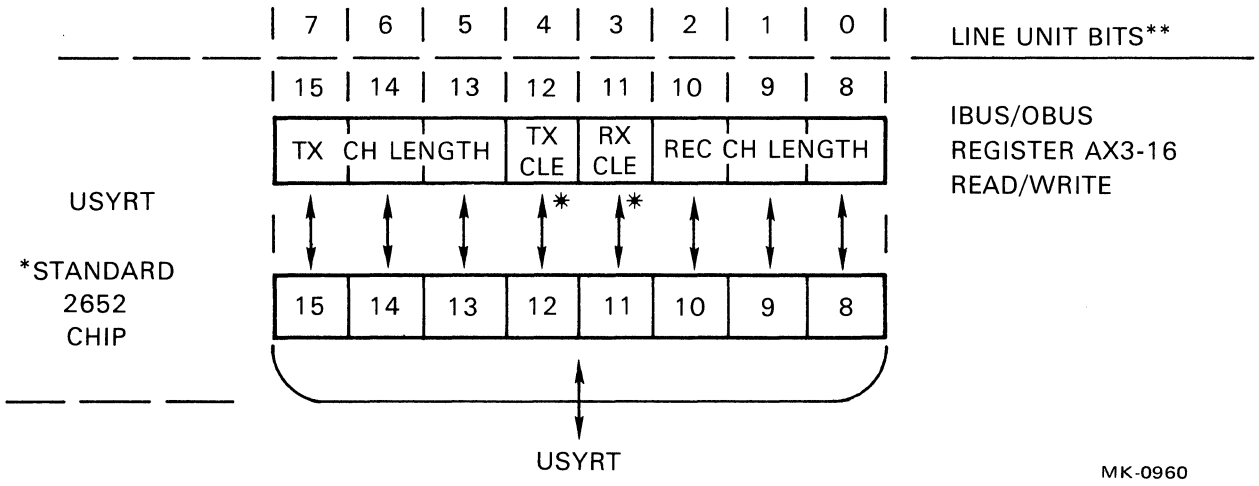


Figure 3-27 AX3-16 Register

Read/Write:

AX3-16 is for special protocols handled by the USYRT (directly address the USYRT). When the module is initialized, zero is loaded into the register.

- Bits 2, 1, 0 = Receiver character length control bits.
  001 through 111 are the number of bits for special protocols.

  000 is for standard eight-bit character.

- Bit 3 = Receiver character length enable.**

- Bit 4 = Transmitter character length enable.**

- Bits 7, 6, 5 = Transmitter character length control bits.
  001 through 111 are the number of characters for special protocols.

  000 is for standard eight-bit character.

USYRT bits <15:8> = line unit bits <7:0> as seen by the microprocessor.

3.3 SILOS

The silos are used to buffer transmit and receive data of up to 64 bytes plus 4 status bits per byte. This feature provides time for the microprocessor and the UNIBUS to handle characters at speeds above 56K bps and decrease the possibility of overruns and underruns. The silos are 12 bits wide with eight data bits and four status bits. Each silo is composed of three 3341 sixty-four by four bit first in first out (FIFO) chips that are used to interface the USYRT and the microprocessor.

3.3.1 Transmit Silo

Data and status should not be loaded unless outready (ORDY) bit 4 of register 11 is high. Register 11, transmit status bits 0-3, must be loaded first followed by loading data bits into register 10. The loading of register 10 will shift the four status bits from register 11 followed by the eight data bits from register 10, into the Transmit Silo. Termination of the shift cycle clears register 11, bits 0-3 and all of register 10. ORDY will set when the silo is ready for the next character. (See Figure 3-28.)

**With Signetics 2652 or equivalent.

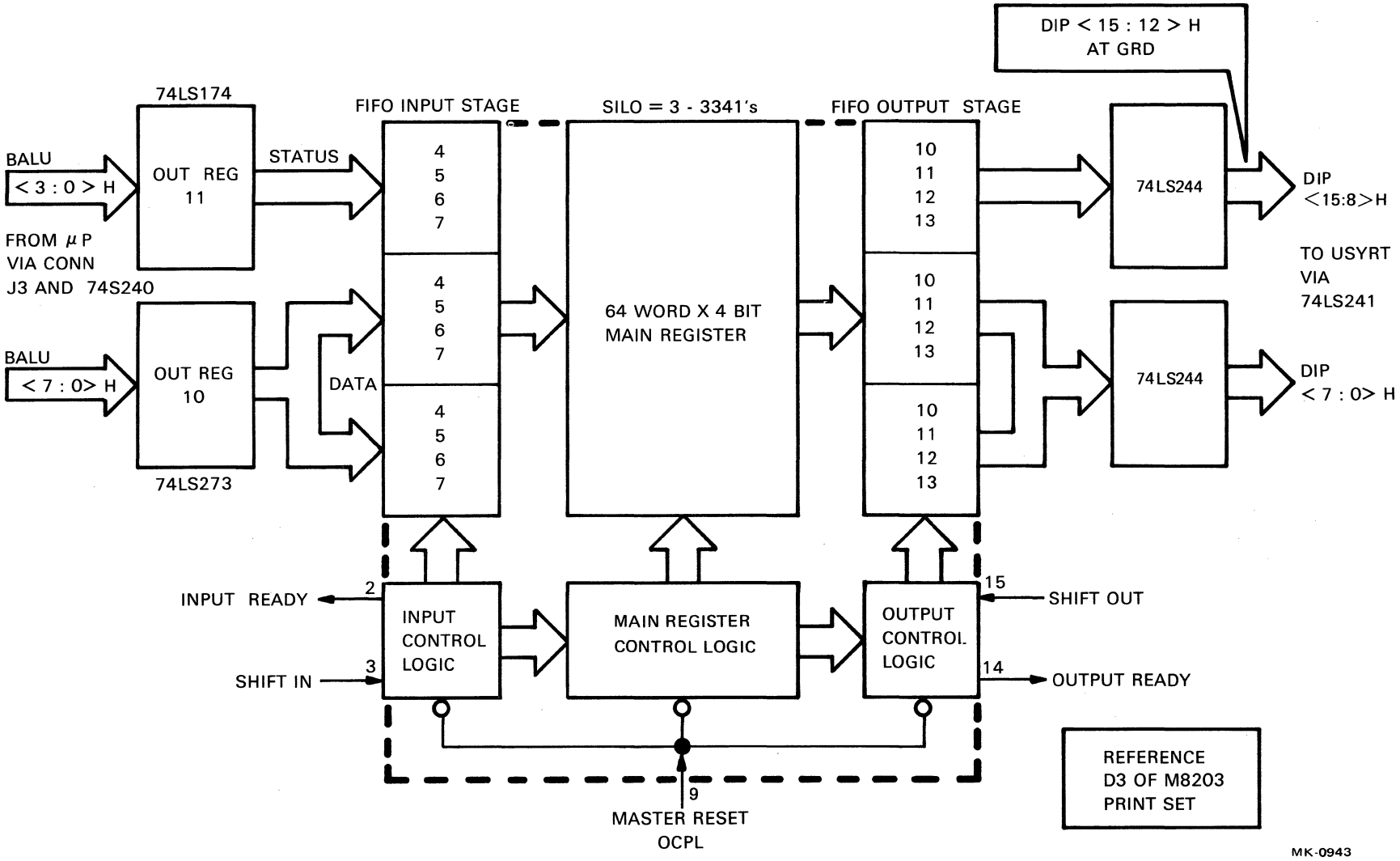


Figure 3-28 Transmit Silo

The output of the silo is shifted into the USYRT by the sequencer when the USYRT is looking for the next character and both Output Ready and Shift Out are asserted. Transfer Enable (TXENA) activates the transmit section of the USYRT when the silos are disabled. TXENA keeps Request To Send set when the silos are enabled. If the transmit section of the USYRT is not disabled between message transmissions, the CRC register is not cleared and causes a CRC error at the receiver. Control logic for the Transmit Enable signal of the USYRT automatically clears when (1), EOM is set with abutted messages and (2), the silos are enabled.

The USYRT generates Transmitter Buffer Empty (TBMTY) when it is ready for the next character. TBMTY is routed through buffer circuitry (74L244), whose output TXBMT H is ANDed with Out Composite Ready (OCOR H) from the silos generating the load signal (Load H) to the sequencer.

The sequencer uses the load signal to generate the timing for transferring a character from the silo to the USYRT. Completion of the sequencer cycle effectively shifts the characters out of the silo (the sequencer is defined in Section 3.4).

3.3.2 Receive Silo

The Receive Silo is loaded from the USYRT with timing provided by the sequencer. USYRT generates a data ready signal when the next character is ready to be transferred into the silo. If the silo is full and the next character cannot be loaded, a receive overrun may occur. (See Figure 3-29.)

If an overrun occurs, the next time a character is loaded into the silo, the status flag is loaded for a receiver overrun. The overrun bit (IBUS register 12, bit 3) remains set until the receiver is cleared. The sequencer looks for Input Ready from the silo and Data Ready from the USYRT (See Figure 3-30) to generate the timing sequence to load the silo (if the silo is full, it will not return Input Ready). The status bits (bits 11-8) are routed in IBUS register 12 and read. The data is taken from the silo when a character (bits 7-0) is read in IBUS register 10 where the data is buffered and the silo is shifted out. If the valid data flag register 12 bit 4 (Input Ready) is not set, IBUS registers 10 and 12 should not be read.

3.4 SEQUENCER

The Sequencer controls all data in and out of the USYRT. Two 1K by 4 bit ROMs determine the priority of the tasks performed (D6 of the *M8203 Print Set*). Timing is generated by a 20 MHz crystal to generate 100 ns increments (D7 of the *M8203 Print Set*). The ROMs can be set up to mask out any operation or to create different versions of the line unit for the utilization of special functions. This flexibility allows the line unit to create several versions, e.g., depopulating the module with special protocol functions. A 20-pin space socket is included on the module for special function chips such as the CRC 32 chip. This section discusses only the standard set of ROMs used with the M8203 Line Unit. Other options will require a "Y" version and will be described in the documentation relevent to the option implemented.

The Sequencer controls all clear functions on the module with the ability to load the USYRT status registers following execution of a clear and before any other operations are performed. The line unit should not be addressed until two microseconds after the clear is initiated to allow the line unit time to initialize. The basic clear operation is controlled by the ROMs after all registers and the USYRT have been cleared. The ROMs clear the transmit and receive circuits and then load the USYRT status registers to a default value specified by the 23038B1 ROM. The line unit is then ready to handle status and data.

The 20 MHz crystal that provides the timing to the sequencer is also used by the data rate generator. A main counter is preset at the beginning of a task and cannot be interrupted. The task continues until the counter overflows. The overflow state is held until a new task is initiated. This is accomplished by clocking the two function registers every 100 ns until a task is assigned. If more than one task is ready, the F1 ROMs will execute the Task with the highest priority. The output of the function registers address the two ROMs that control the sequencer.

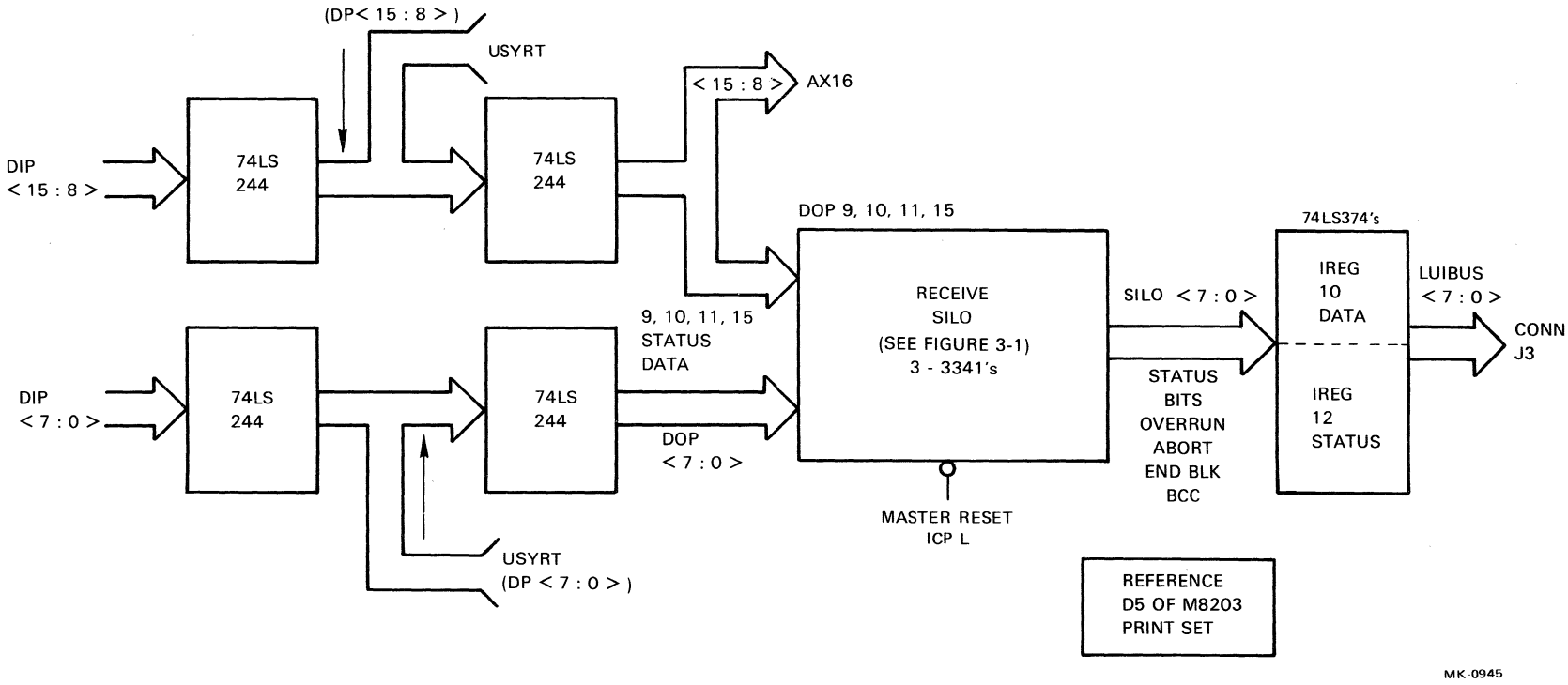


Figure 3-29 Receive Silo

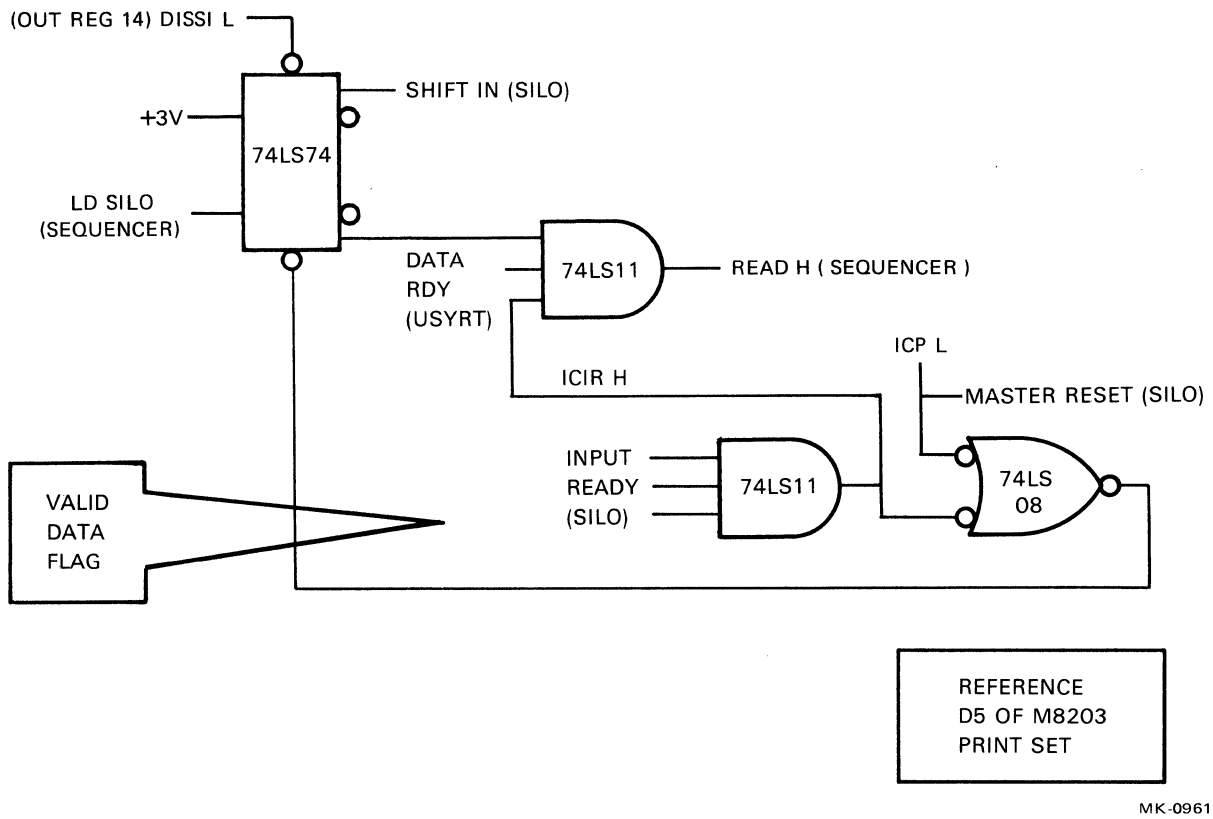


Figure 3-30 Load Silo

Sequencer output is a 23042B1 ROM used to generate the clocks for moving data. ROM output is clocked every 100 ns via the master clock.

Priority is set in the ROMs in the basic M8203 module to:

1. Initialize – Set the character length for both the transmitter and receiver to eight bits.
2. I/O Clear – Input/Output clear (clears the silos and receive/transmit logic).
3. Load Mode – Sets the mode to character oriented protocol with CRC 16 selected on INIT and parameter adjustment when OBUS register 17 is loaded.
4. Read – Read data and status from the USYRT.
5. Load EOM – Load the End of Message into the transmit status register.
6. Load Data – Load data and transmit status into the USYRT.
7. Extended Registers Read the USYRT – Read the USYRT and load the data into the extended registers.
8. Extended Registers Write Data – Write data from the extended registers into the USYRT.

The first three are done automatically on a Master Clear or INIT to the microprocessor and line unit. The functions are executed in the priority shown following the clear sequence of the line unit. The priority structure in ROM can be changed to accommodate the special variations to be implemented.

3.5 DATA RATE GENERATOR

The data rates are generated via two counters. The first counter is a Schottky Binary Counter (93S16) that is loaded on overflow and clocked from the 20 MHz crystal that provides the master clock to the M8203 module. The 1M bps rate does not use the counter (is common to the Master clock). The 500K bps and 250K bps rates use the counter as a binary divider. The 56K (55.5556K) data rate uses an additional flip-flop (74LS74) to create a divide by 18 function. The second counter (74LS161) is a pure binary counter which generates four clock speeds directly: 19.2K bps, 9.6K bps, 4.8K bps, and 2.4K bps rates. The speeds below 56K bps are generated by the overflow to the first counter for a divide by 26 and a flip-flop (74LS74) which provides the clock input to the second counter. (See Figure 3-31.)

The outputs go to an eight-to-one multiplexer (74S151) whose select inputs are controlled by a switch (See Figure 3-36). The multiplexer output (20X CLK) is input to a divide by 10 counter (74LS161 shift register for the 20X CLK). The Integral Modem 74S112 flip-flop is the last divider for the data rate or NULL clock.

3.6 USYRT

The Universal Synchronous Receiver/Transmitter (USYRT) functions as a Large Scale Integration (LSI) subsystem for synchronous communications. All data to the line unit must go through the USYRT. The USYRT provides the necessary logic support via program parameter registers for basic protocol handling and error detection. Protocol handling conforms to standards but is slightly different in each version. The 2652 chip, version 01, is implemented in the M8203. Replacement of the USYRT changes about half of the logic on the M8203 in one chip. In many cases, this chip or the timing going into this chip will be a problem area.

Typical start and receive sequences in bit and character oriented protocols are provided in Figures 3-32 through 3-35.

Troubleshooting of the M8203 module should be done in both direct and indirect modes before determining where the problem area exists. Refer to A-PS-2112517-0-0 *Purchase Specification* for detailed information on the USYRT.

Timing diagrams, terminal connections and an internal bit map are provided in Appendix C, Integrated Circuit Descriptions.

3.7 MODEM INTERFACE

The modem contains several interfaces as described below.

- EIA levels are based on:
  - EIA RS-449 specifications that use the J2 connector for plugging in the BC55C cable for RS-423-A/CCITT V.10 (ISO 4902)/X.26 and Federal Standards 1030/1031,
  - The BC55B cable for RS-422-A/CCITT V.11 (ISO 4902)/X.27 and Federal Standards 1030/1031, and
  - The BC55C cable for RS-232-C/CCITT V.28 (ISO 2110).
- The J1 connector can be used for plugging in the BC05Z cable for the CCITT V.35 (ISO 2593) interface or the BC55A-10 cable for the Integral Modem interface.

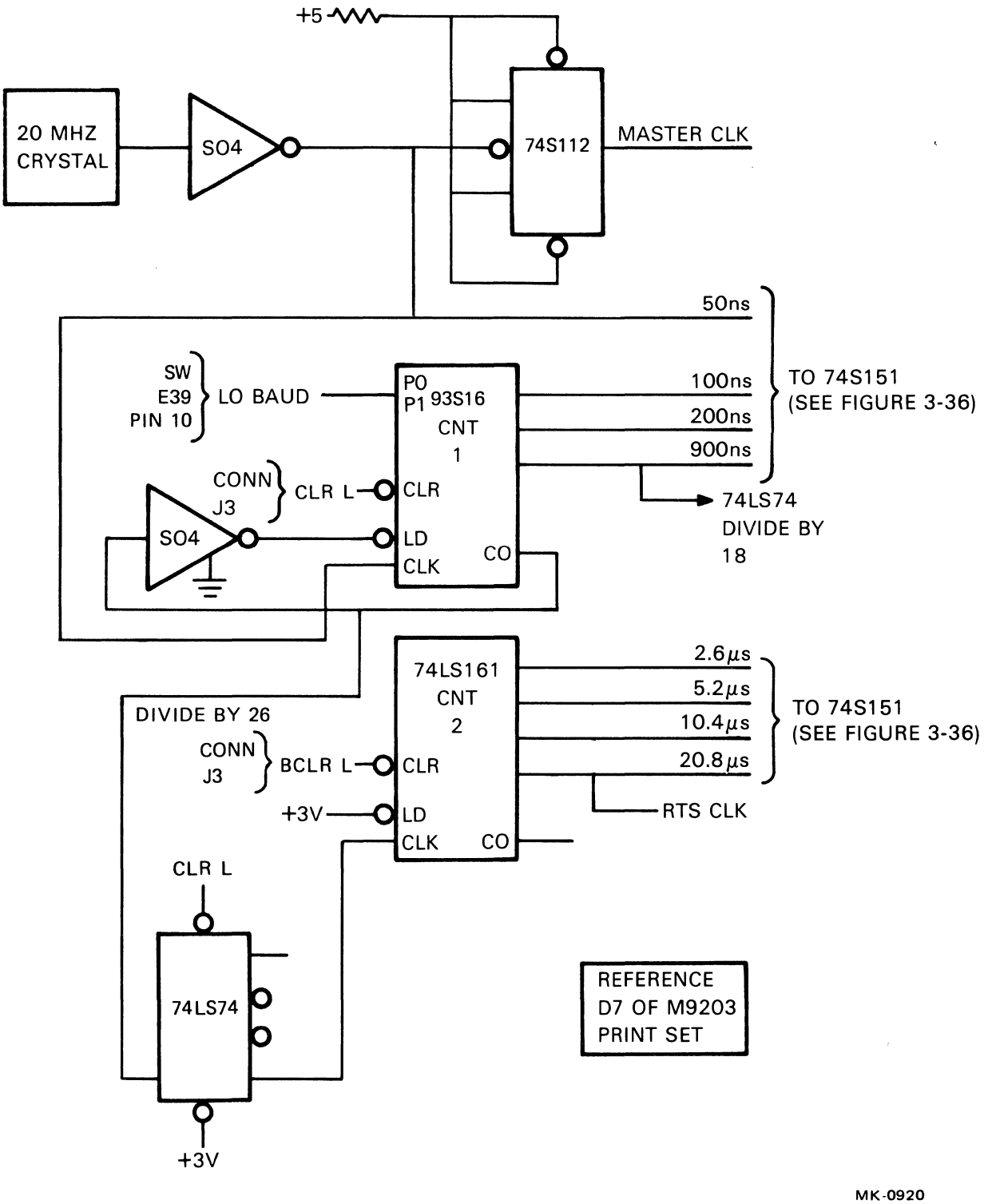


Figure 3-31 Data Rate Generator

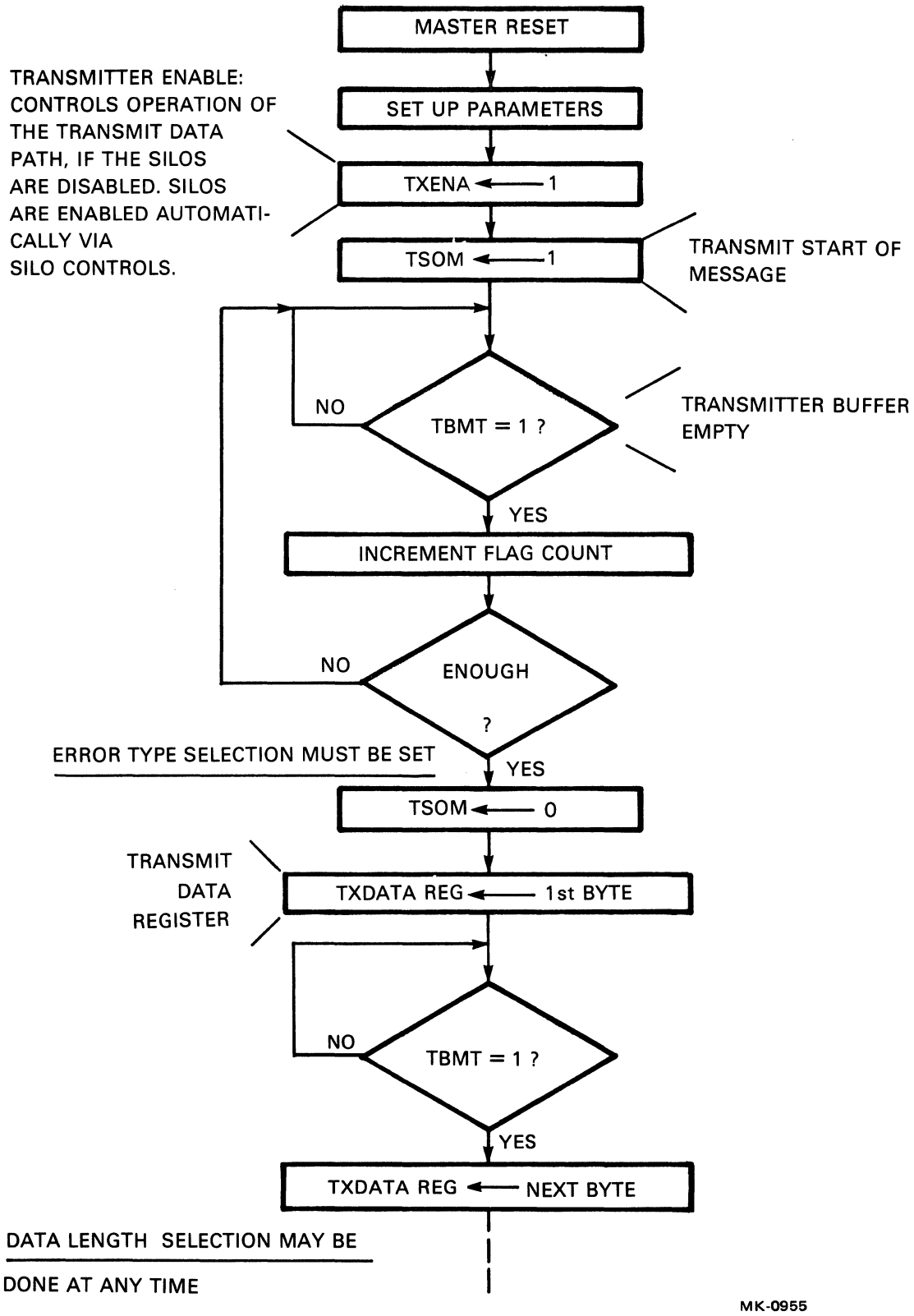


Figure 3-32 Typical Start Sequence for the USYRT Bit Oriented Protocol Transmission Flowchart

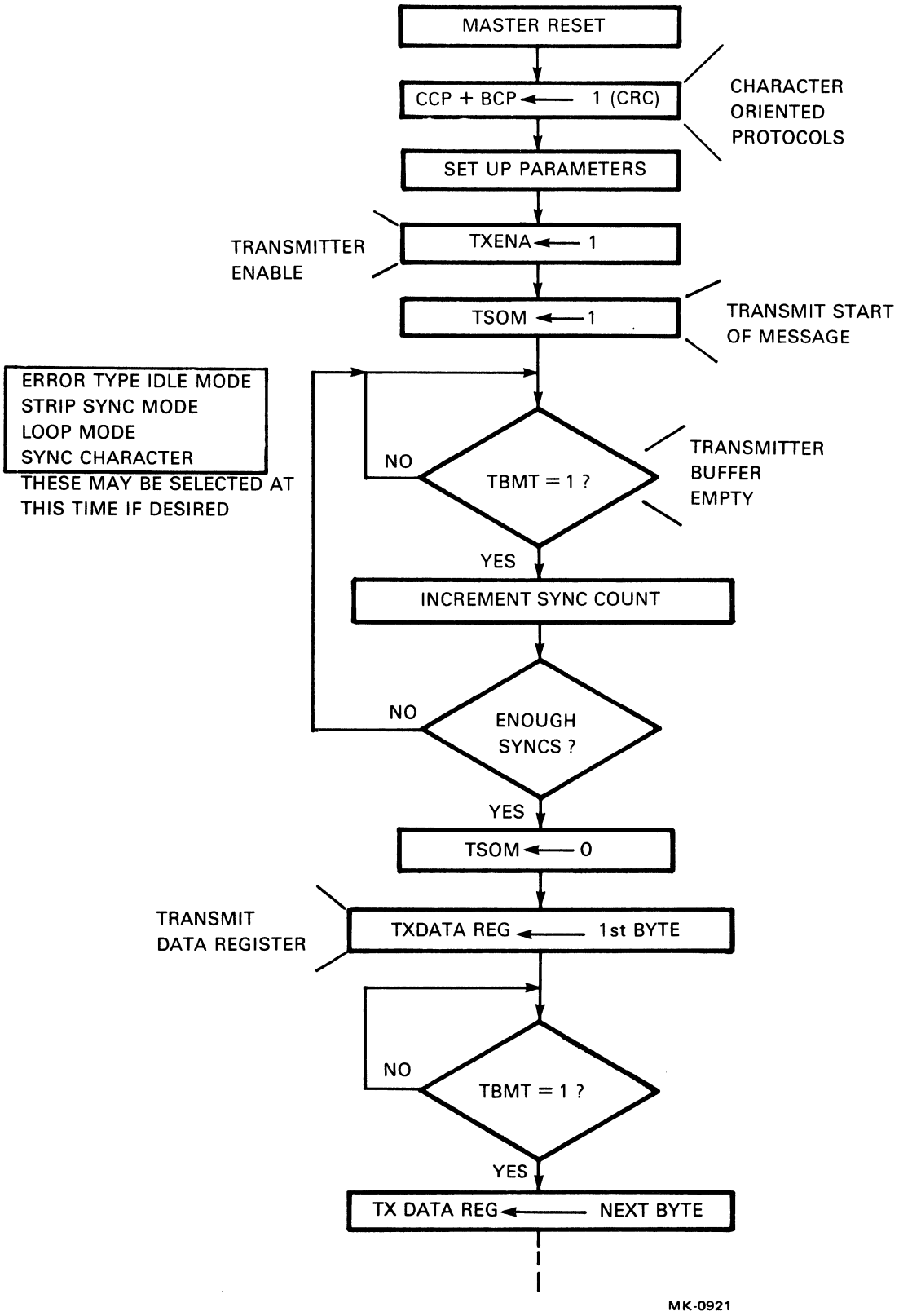


Figure 3-33 Typical Start Sequence for the USYRT Character Oriented Protocol Transmission Flowchart

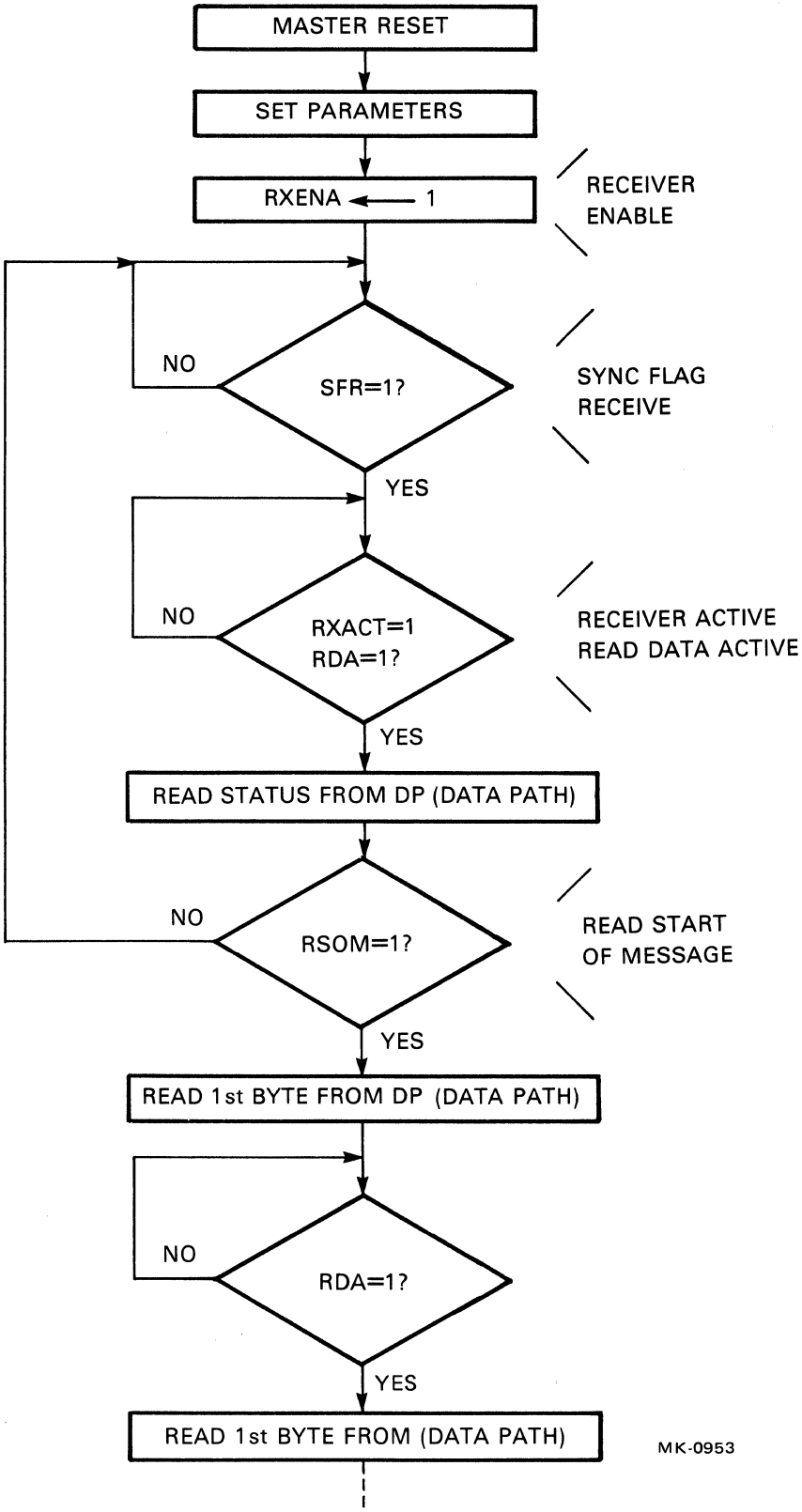


Figure 3-34 Typical Receive Sequence for the USYRT Bit Oriented Protocol Flowchart

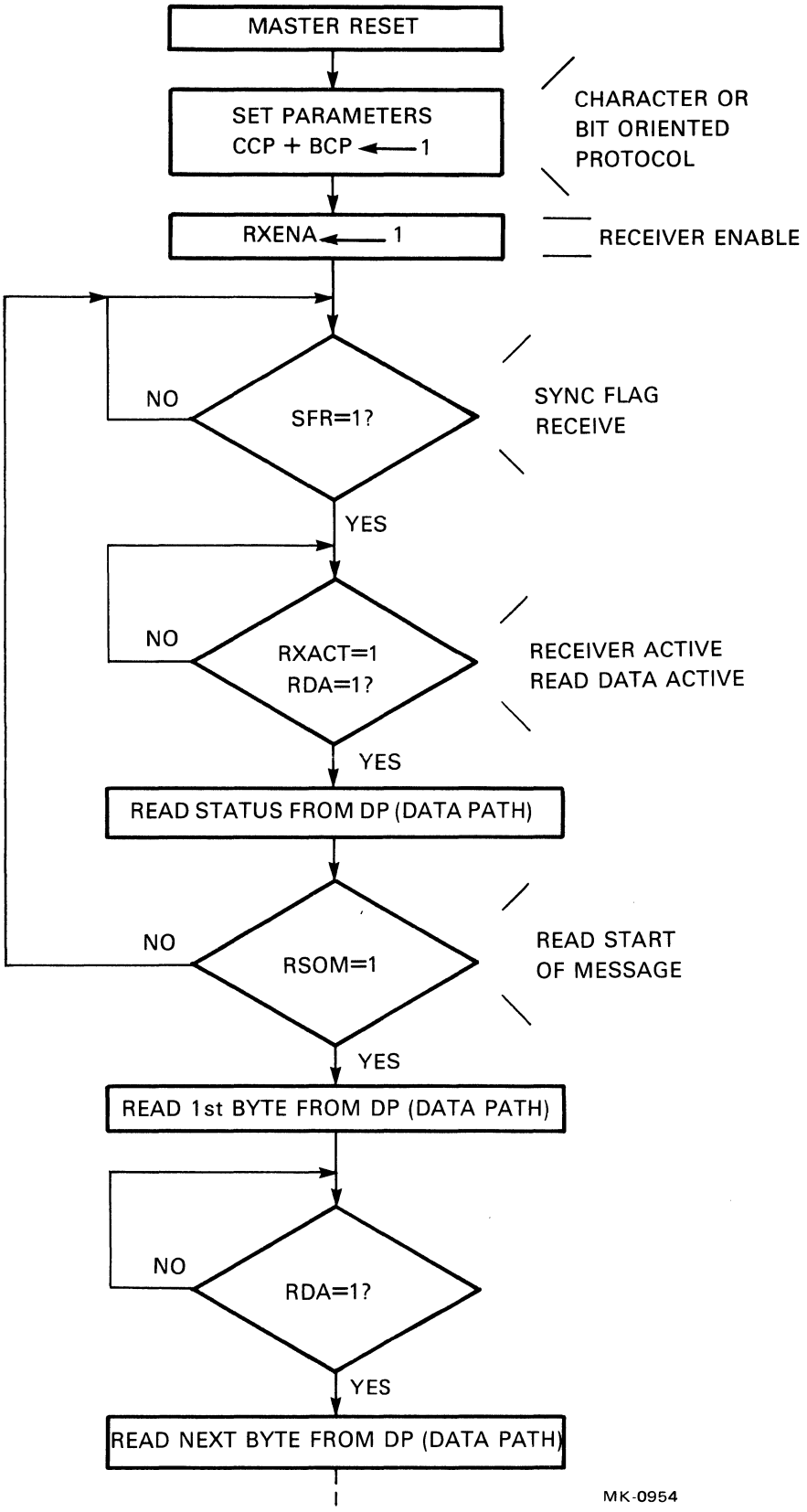
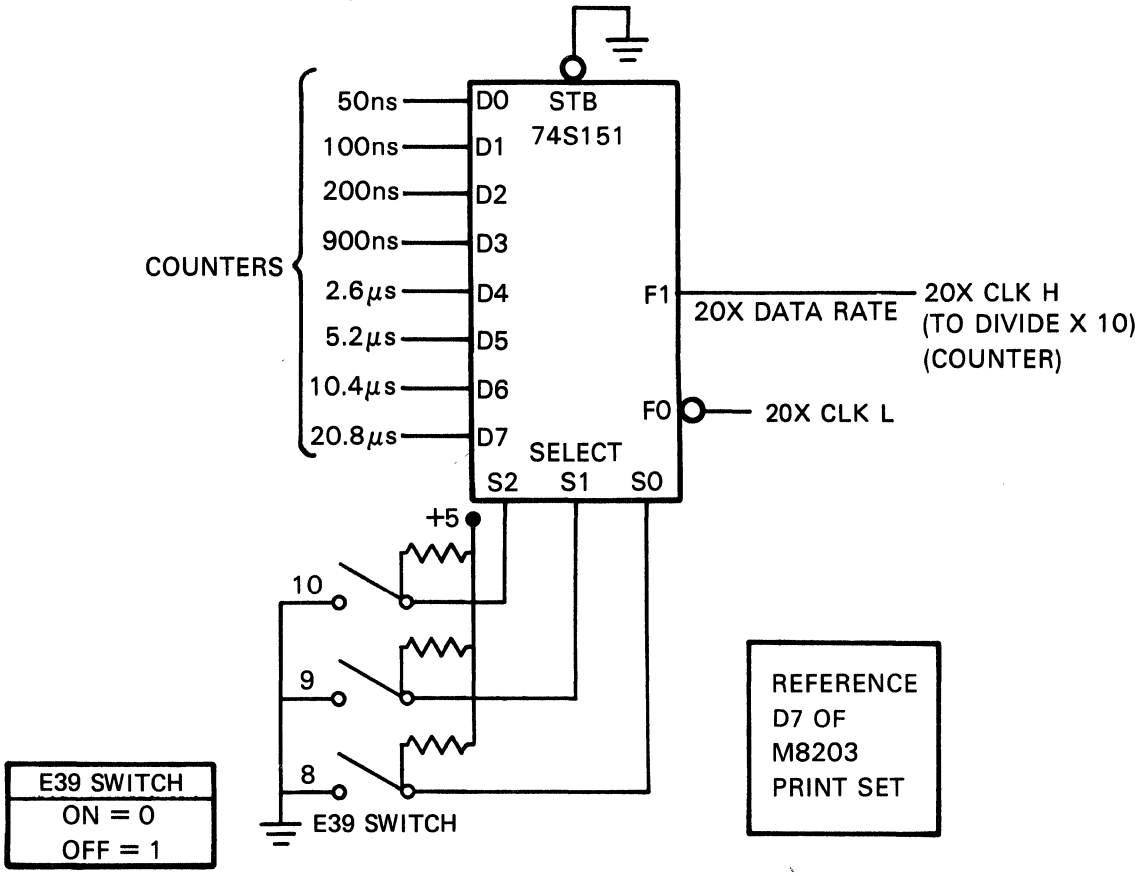


Figure 3-35 Typical Receive Sequence for the USYRT Character Oriented Protocol Flowchart

- The M8203 module will be shipped with two test connectors (H3254 and H3255) that will turn around the Modem Interface and the Integral Modem signals for test purposes only. This allows the logic to select any interface and test it in a loop back mode. The cables are options and must be ordered separately with the test connectors.

- The Modem Interfaces all have a NULL clock controlled by a counter that is switch selectable from 2400 bps to one Mbps. The speed must be matched to the interfacing level used for maintenance or null modem speeds. (Refer to Figure 3-36.)



INPUTS			STROBE	BAUD RATE
SELECT/SWITCH				
S2/10	S1/9	S0/8		
0	0	0	0	1 MBPS
0	0	1	0	500 KBPS
0	1	0	0	250 KBPS
0	1	1	0	56 KBPS
1	0	0	0	19.2 KBPS
1	0	1	0	9.6 KBPS
1	1	0	0	4.8 KBPS
1	1	1	0	2.4 KBPS

MK-0933

Figure 3-36 Data Rate Select

- The EIA interface accepts three cables but cannot distinguish one from the others. The interface requires that switch E39, position 7, be set to select either the single-ended (unbalanced) or differential balanced drivers. Switch position 7 "ON" selects the differential interface. The program can read the switch setting, without opening the cabinet to check the module, to determine if the setting is correct. Differential interface is only used with the BC55B cable and the EIA RS-422-A interface level.

- The Modem Interface receivers (D8 of *M8203 Print Set*) are fail-safe and can operate with either single-ended or differential interfaces. The receivers also have space for inserting terminating resistors to accommodate differential signals. These resistors are built into the cable to allow swapping of modules without adding components.

- The V.35 interface is a special interfacing level with balanced termination at both ends of the line. It is a high speed interface that can operate at up to 250K bps.

  Qualifications for using a V.35 Interface:

  - A BC05Z cable with an H3250 test connector must be plugged into the J1 connector on the M8203 module.

  - Switch E39 position 5 ON selects the correct interface chips for V.35.

  - The interface level can be read by the program through the extended registers.

  - The cable or test connector must be removed from connector J2.

3.8 INTEGRAL MODEM SPECIFICATIONS

The Integral Modem may be used for a point-to-point multi-point unit, master/slave, or a multimaster system and:

- Is compatible with previous versions of the Integral Modem such as the DMC11-M(X) and can be connected using triax/twinax cable. Data and sync sequence are compatible.

- Is connected through a Berg connector and the interlock selects the Integral Modem using a BC55A-10 interlock cable.

- Runs at four switch selectable speeds (56K bps, 250K bps, 500K bps, and 1M bps).

- Is transformer coupled to a 70 to 150 ohm line which must be a twinax or triax cable for high common mode rejection and common mode voltages of up to 500 volts.

- Requires two intersystem cables for full-duplex and one intersystem cable for half-duplex operation.

- The line unit must be terminated with a 75 ohm line or a line matching resistor on each end. Other impedance lines can be used if properly terminated, e.g., the 150 ohm DECdataway.

- The line must be terminated at both ends with the characteristic impedance.

3.8.1 Receiver

The received data enters the modem through an isolation transformer whose output is directed to a differential amplifier to eliminate common mode noise. The amplifier's second stage uses an active Butterworth filter with an added passive filter which provides high and low-cut off. The filter complementary outputs are input to a comparator which detects zero crossover. Positive and negative transitions from the comparator clock the UP and DOWN flip-flops. All clocking is done at a clock rate 20 times the bps rate and the UP and DOWN flip-flops latch until cleared by the TRANS flip-flop. (Refer to Figure 3-37 for the block diagram and Figures 3-38 and 3-39 for timing considerations.)

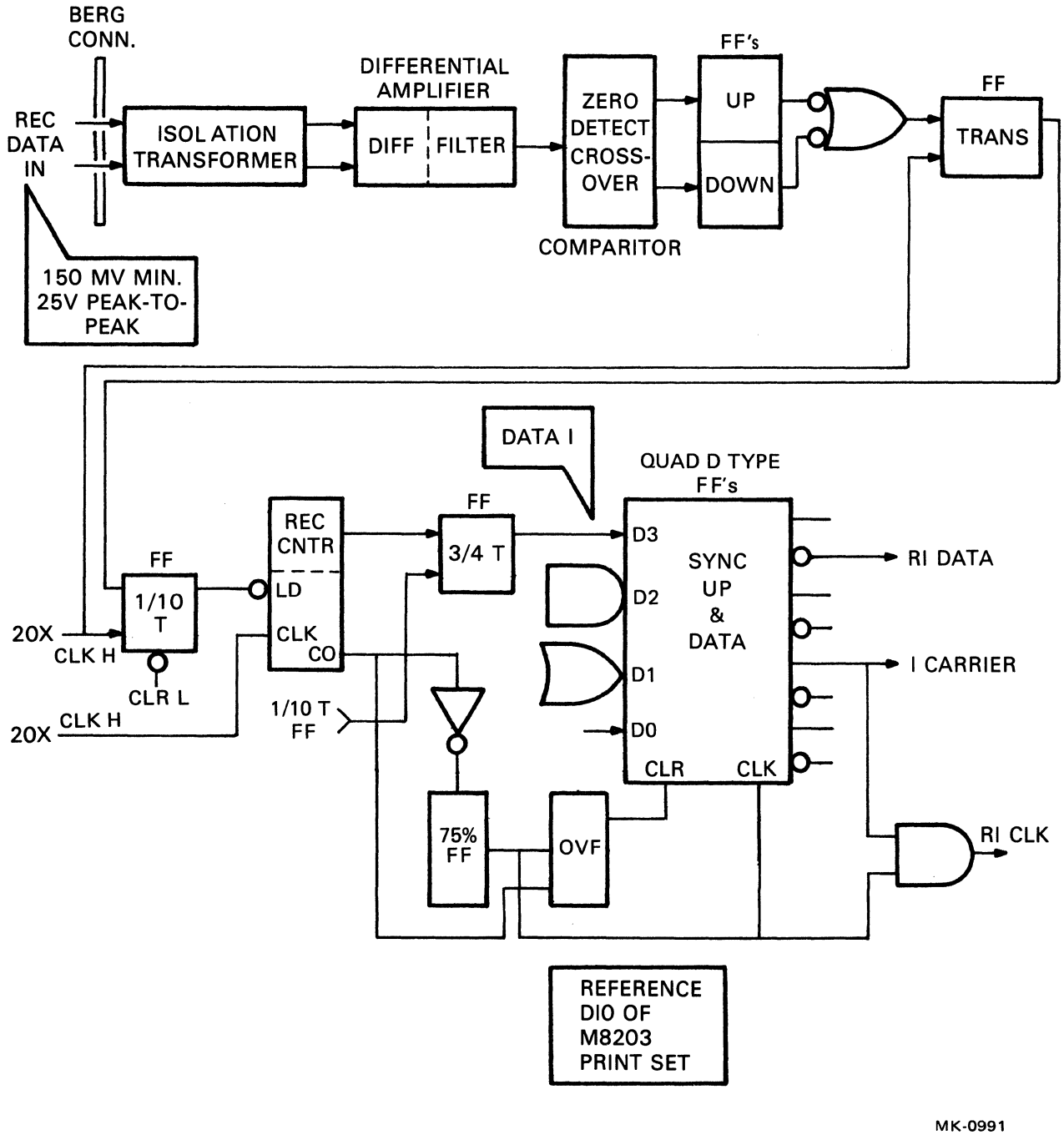


Figure 3-37 Modem Receiver Block Diagram

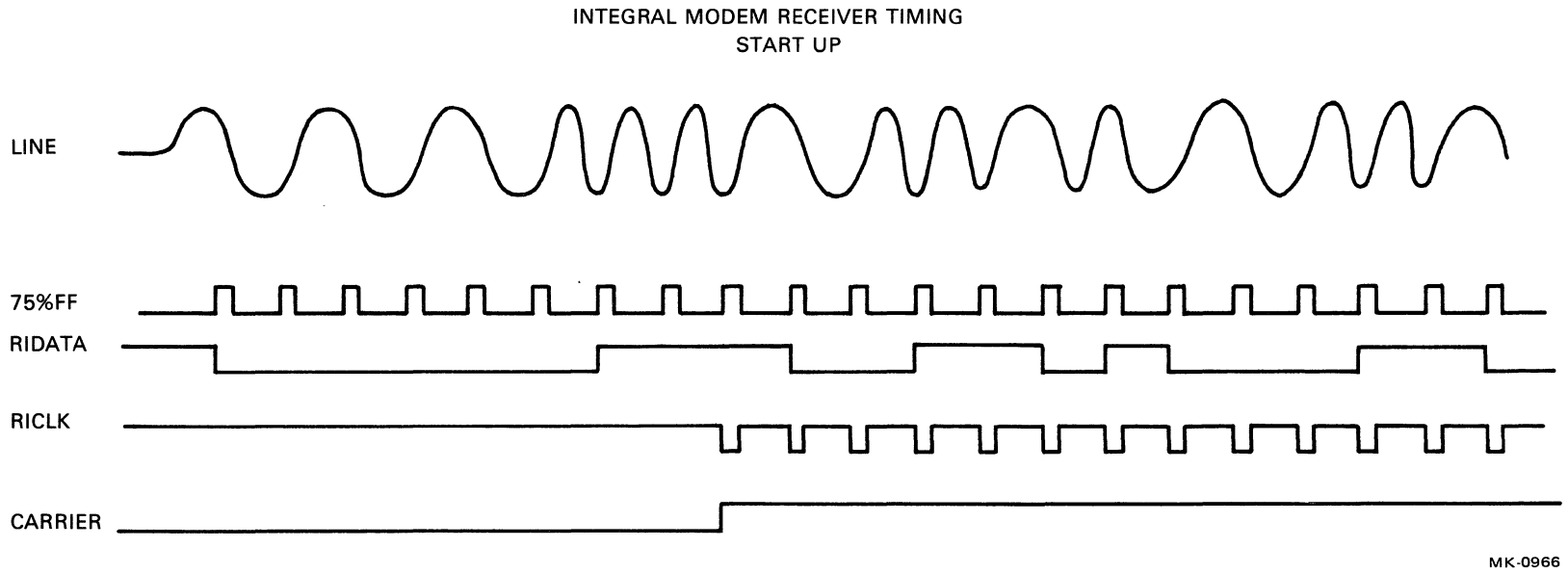


Figure 3-38 Modem Receiver Timing Diagram – Start-Up

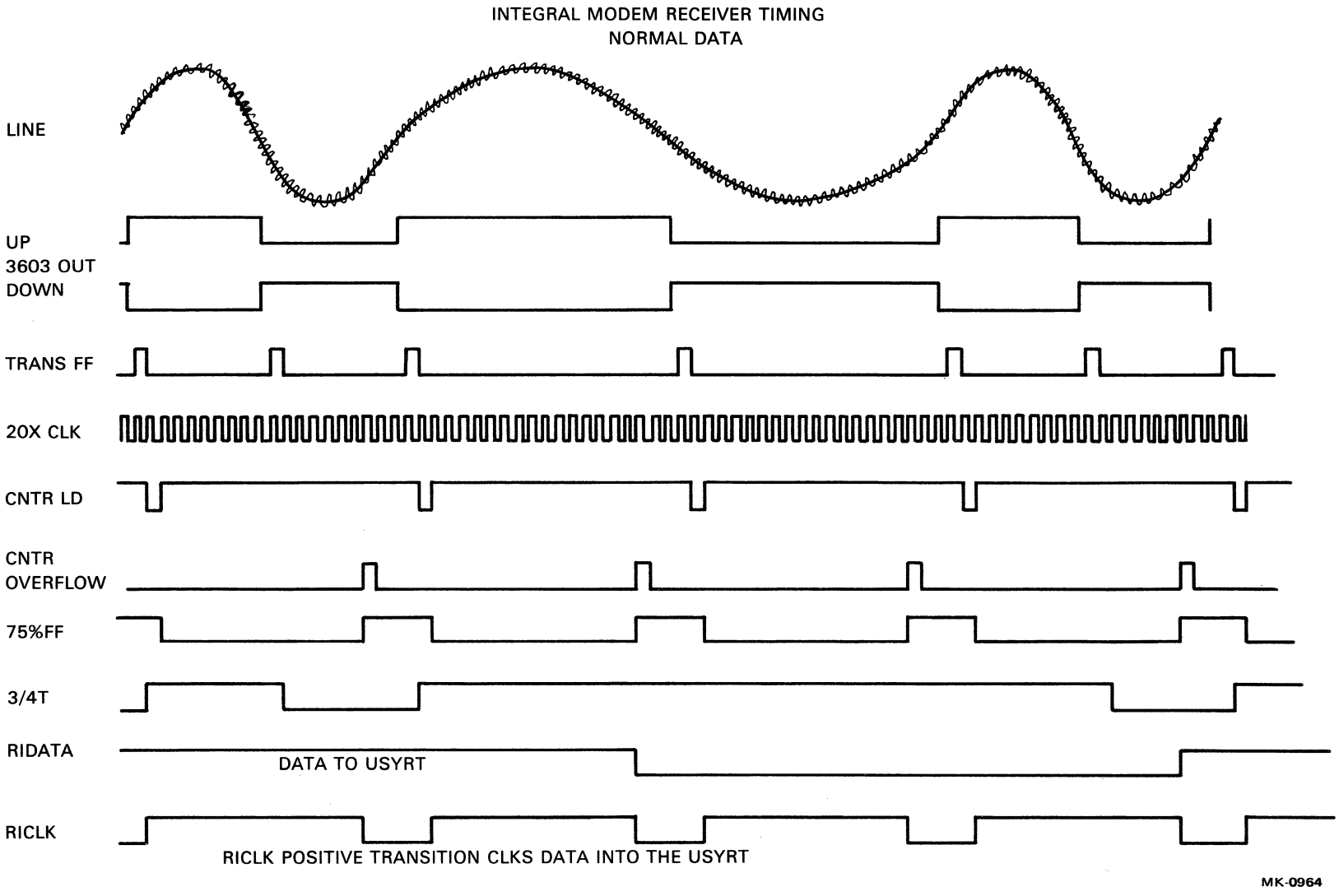


Figure 3-39 Modem Receiver Timing Diagram – Normal Data

When either the UP or DOWN flip-flop is set, the next clock pulse loads the transitions (TRANS) flip-flop which then clears the UP or DOWN flip-flop, and holds it clear for one clock time. The clock input to the TRANS flip-flop and REC CNTR is 20 times the data rate clock time.

The next clock loads the 1/10 time flip-flop which in turn clears the TRANS flip-flop. The output of the 1/10 time flip-flop controls the load (LD) input to the receive counter (REC CNTR).

When the 3/4 time flip-flop is set, and the time between transitions is less than 16 clock times, the DATA I flip-flop (SYNC UP & DATA chip, D3 input) is clocked to zero. If the transition time at the 3/4 time flip-flop is greater than 16 clock times, the DATA I flip-flop is clocked to a one. The minimum time between transitions is .05 to .10 bit times, which is accomplished by the TRANS flip-flop clearing the UP and DOWN flip flops.

The REC CNTR is clocked at half clock time (or inverted 20X clock). The counter is loaded if the 1/10 time flip-flop is set and 16 clocks have occurred since the last load. The count control is true except in an overflow condition or when operating in half-duplex mode with the transmitter active.

The overflow flip-flop clears the CARRIER SYNC UP & DATA register until the next one followed by two zeros sequence. Overflow occurs when no transition has occurred in one and one-half bit times.

The SYNC UP & DATA register is clocked at three quarter time and loads DATA I into the first flip-flop of the register. The next three quarter time clock causes DATA I to be ANDed with the output of the first flip-flop, provided that this output is a zero, and sets the second flip-flop. The next clock sets the third flip-flop from an ORed input that latches this flip-flop once it is set. The third flip-flop is cleared at one and one-half bit times (overflow) which then clears the SYNC UP & DATA register.

- The low output of the first flip-flop presents data.
- The output of the third flip-flop presents an I CARRIER signal which enables the receiver clock for serial data bits (first data character) to be transferred to the USYRT and indicates the receiver is in SYNC with the transmitter.

Receiver specifications are shown below:

- Receiver sensitivity

150 MV P-P	with 12% distortion on the line at 250K bps to 1M bps
200 MV P-P	with 15% distortion on the line at 250K bps to 1M bps
150 MV P-P	with 20% distortion on the line at 56K bps

- Protection

  500 volts dc common mode voltage
  15 volts P-P normal mode voltage

- Line loading Power on or off

  2500 ohms at 1M bps
  6000 ohms at 500K bps
  10000 ohms at 250K bps
  10000 ohms at 56K bps

NOTE

Jumpers W14 and W15 can be installed to reduce the bandwidth of the Integral Modem receiver filter for 56K bps operation only. These jumpers usually are not installed.

3.8.2 Transmitter

The transmitter creates a simulated sync wave by step reproduction. A crystal controlled oscillator (with no adjustments) supplies the transmitter clocking signal (XMIT CLK). The data rate select clock (10X CLK or 5X CLK) and the data to be transmitted are gated through clock phase data ANDing circuitry to provide the clocking signal to the SINE GEN. Sine generator output goes to a bipolar line driver that generates an ac signal with zero crossover points. (Refer to Figure 3-40 for the block diagram and Figures 3-41 and 3-42 for timing considerations.)

Line driver output is connected to the protection transformer through two VMOS transistors. The VMOS transistors are switched off with the beginning of the start up sequence and the end of the shut down sequence. The +5V low circuit turns off the VMOS transistors on low logic power to keep the line from generating noise or from loading the line. During power-up this circuit keeps the modem in the disabled state for several milliseconds to prevent the transmission of nonsense characters that would interfere with transmission in progress on a multipoint line.

The transmitter is disabled or tristated when line units are not transferring data. The transmitter does not load the line when power is off.

Transmitter specifications are shown below:

- Transmitter drive

  5.6 volts P-P minimum into a 30 ohm load

- Protection

  500 volts dc common mode on the line

  30 volts normal mode on the line when the transmitter is disabled

  Will withstand a shorted line without damage to the circuitry

- Transmitter loading disabled or power off

  3000 ohms at 1M bps
  5000 ohms at 500K bps
  10000 ohms at 250K bps
  15000 ohms at 56K bps

NOTE

Signals above 200 volt microseconds saturate the transformers. This causes noise problems on the line when the transformers collapse as well as possible errors in the recover circuit.

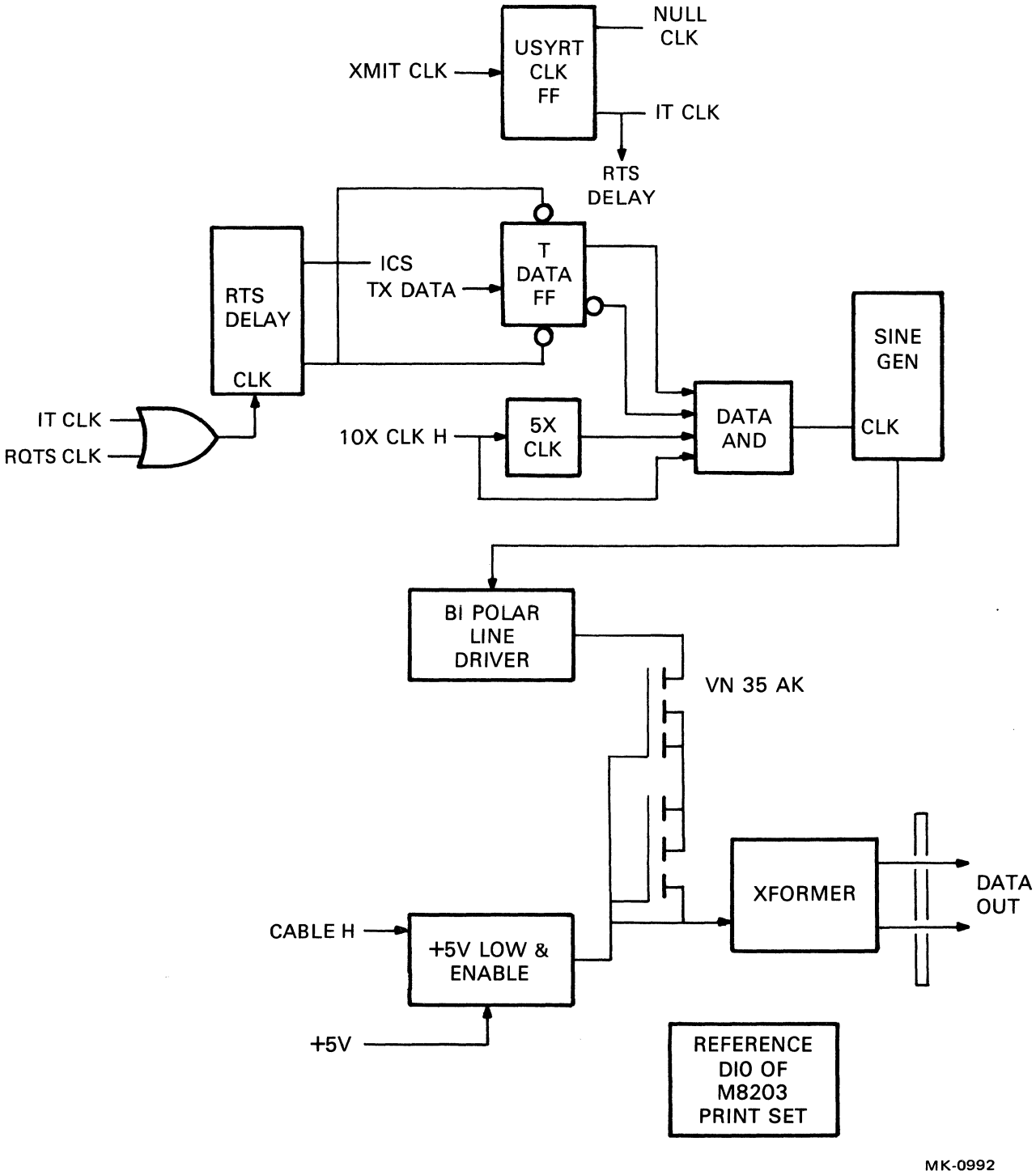


Figure 3-40 Modem Transmitter Block Diagram

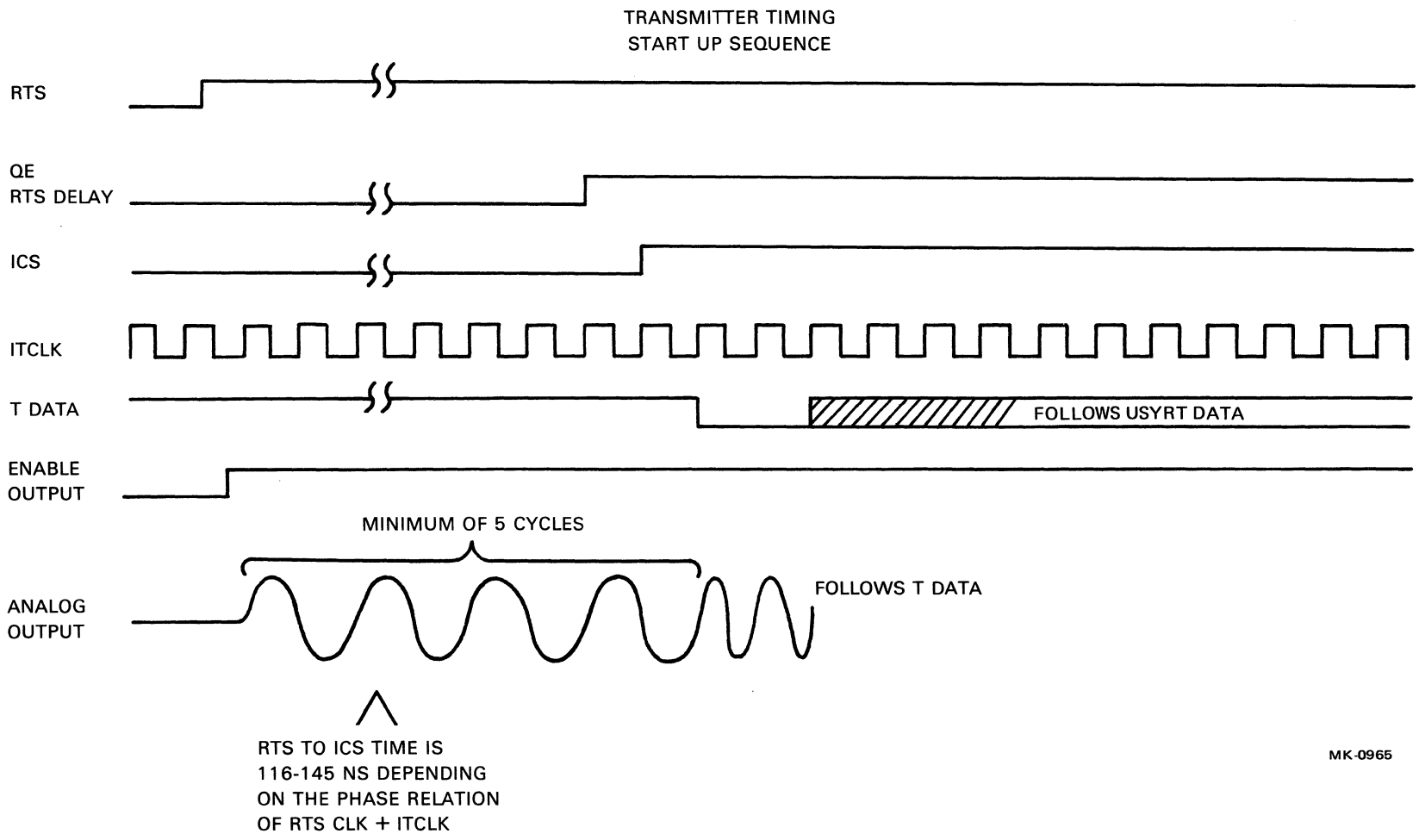


Figure 3-41 Modem Transmitter Timing Diagram – Start-Up

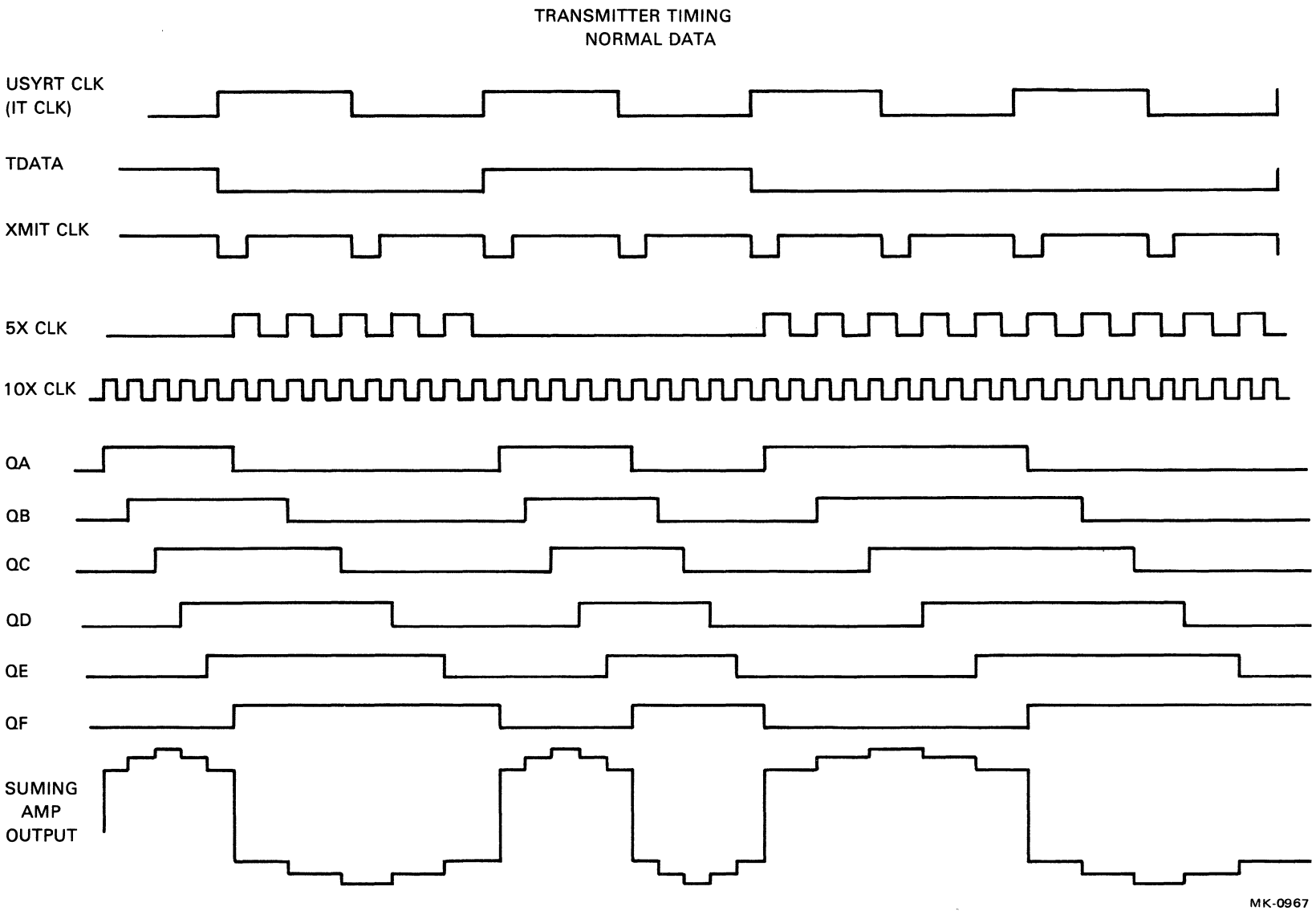


Figure 3-42 Modem Transmitter Timing Diagram – Normal Data

CHAPTER 4
SERVICE

4.1 SCOPE

Servicing information for the M8203 module consists of preventive maintenance procedures which are based on established system preventive maintenance schedules and corrective maintenance via the use of line unit microdiagnostics. Cable specifications and recommendations are provided in Appendix B, Recommended Cables/Connectors.

4.2 MAINTENANCE PHILOSOPHY

The M8203 is the Field Service Field Replacable Unit (FRU). Isolation to the module level must be done through the use of DIGITAL Diagnostics and/or any microdiagnostics that may have been incorporated in the microprocessor Control Read Only Memory (CROM).

4.2.1 Preventive Maintenance

Preventive maintenance (PM) for the M8203 module is recommended for voltages and connections during system PM or when problems exist. Keep a record of the initial local link cable characteristics, particularly the propagation time delay and short circuit line resistance as indicated in this section. Once the system is operational, record the received signal amplitude at the M8203 (See Figure 4-1). Repeat this measurement at every scheduled system PM date (should be at least four times a year). If a deviation of 20 percent is observed in signal amplitude, disconnect both ends of the cable from the M8203 and measure both open and short circuit resistance of the line (See Figure 4-2).

If a measured open circuit resistance is less than 20 megohms, inspect the cable for contamination of the dielectric, adverse effects of sharp bends at stress points, elevated temperatures, or aging. If the line resistance with a shorted end increases above the value measured at installation, inspect the cable connectors for loose fits, contamination, and excessive tension on the cable.

To locate a defective section, an ohmeter can be used to diagnose an open line or a low impedance shorted line by checking one section at a time until the faulty section is located. If the cable is not partitioned into small enough sections, the distance to the fault can be measured by making use of time domain reflectometry (TDR).

Although TDR cable testers are available from Tektronix and other manufacturers, a pulse generator and oscilloscope can be used for approximate measurements. Disconnect both ends of the cable, and drive one end with a 5V peak and a 100 ns wide pulse with a repetition rate below 10 kHz. Measure the time interval between the leading edge of the driven pulse and the leading edge of the first reflection. The reflected pulse will be in the 10 mV to 1V range. This range is normal for an open line, but inverted for a shorted line. Figure 4-3 shows typical oscilloscope traces for both cases. The time interval represents the propagation time delay for a round trip from the signal generator to the fault and back. The distance D to the fault in feet (meters) is:

$$D = T_p/2p$$

where T_p is the measured time delay in nanoseconds, and p is the propagation time in nanoseconds per foot (meter) recorded before the cable was installed.

THE VOLTAGE CAN BE MEASURED BY RUNNING THE DIAGNOSTIC LOOPING ON TEST #17 of CZDMS.* THE PEAK TO PEAK VOLTAGE CAN THEN BE MEASURED WITH A SCOPE ACROSS THE TERMINATING RESISTORS AT EACH END OF THE CABLE SYSTEM. BOTH THE TRANSMITTED AND RECEIVED VOLTAGE SHOULD BE RECORDED FOR REFERENCE.

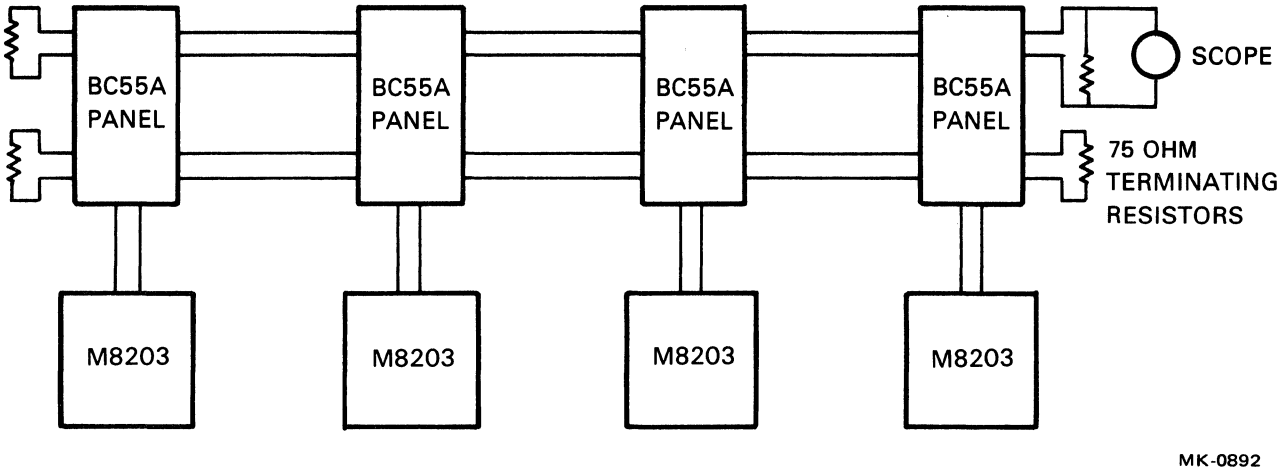


Figure 4-1 Received Signal Measurement

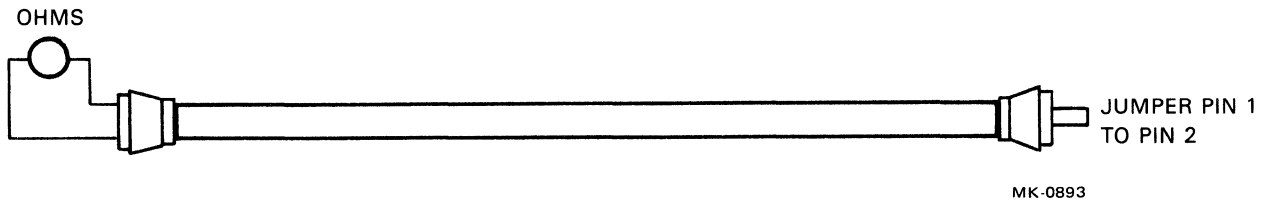


Figure 4-2 Open and Short Circuit Resistance

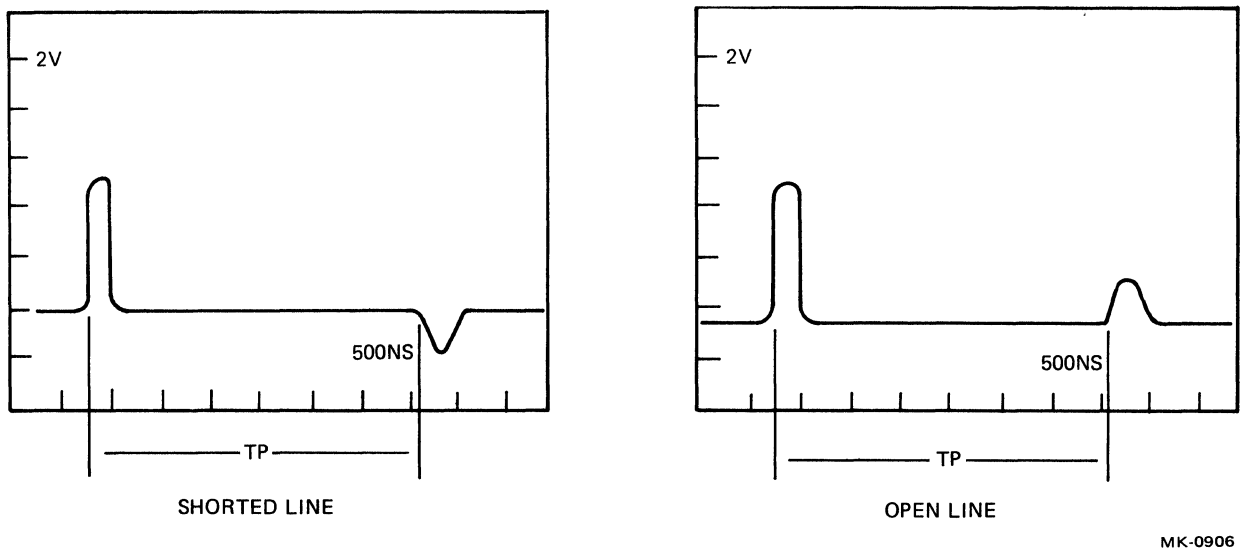


Figure 4-3 Signal Reflections from a Line Fault

4.2.2 Corrective Maintenance

Standard test equipment may be used during corrective maintenance (CM). M8203 Line Unit microdiagnostics are provided in Appendix A of this document. The line unit microdiagnostic tests are run following completion of the microprocessor microdiagnostics.

NOTE
Modem status can be checked quickly by observing LEDs mounted on the board.

D10	Signal Quality	Not used with the Integral Modem
D11	Carrier	Indicates receiver is in sync
D12	Receiver Data	
D13	Transmit Data	
D14	Request to Send	
D15	Been Polled	From microprocessor indicating that the slave unit has been polled. This LED may be used differently depending on the option selected. For example, in the DMR11 option, it is referred to as the heartbeat LED. Refer to specific options manual for detailed use of this LED.

APPENDIX A
MICRODIAGNOSTIC TESTS

A.1 INTRODUCTION

The M8203 Line Unit microdiagnostic tests have been implemented in the M8207-YA and RA modules. Developers using other versions of the M8207 Microprocessor (or similar microprocessor) should include this microprogram with the microcoded diagnostics they generate for their application.

A.2 HARDWARE REQUIREMENTS

The following hardware is required to run the diagnostics:

- Central Processing Unit (CPU)
- M8207 Microprocessor
- M8203 Line Unit

A.3 INTERNAL MICRODIAGNOSTICS

Internal microdiagnostics need no supporting software; they are written in KDA Assembler format that runs on initialization within the Microprocessor subsystem. These diagnostics are Go/No Go types and are specifically developed to test the M8203 depending on the application. The example shown on the following pages is provided as a typical routine, but not necessarily the only possibility. Developers can use this example to create different variations of microdiagnostics to suit special needs. Errors are isolated to the module level. When an error is detected, the microcode attempts to insert an error number in BSEL 4, and enters an indefinite loop. CPU software may visually inspect the RUN bit at the end of the test. The current test number is entered in BSEL 6.

NOTE

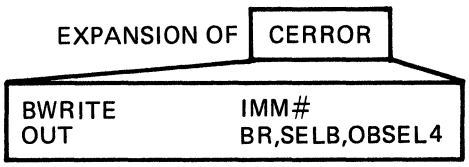
Some options may use registers other than BSEL 4 to indicate microdiagnostic test results.

A.4 LINE UNIT TESTS

Line unit microdiagnostic tests are run when the microdiagnostic tests are completed on the M8207 Microprocessor. A brief message is sent through the line unit. Observe and ensure that the message returns correctly. Also observe the block check character (BCC) bit and cyclic redundancy check character (CRC) 16 word.

In the following tests, CERROR is a macro that when expanded generates an error number (current error number), inputs this number into BSEL 4, and increments the error number to identify the next error.

EXAMPLE:



MK-0907

```
DLUT:   BRWRTE  IMM,264          ;INDICATE THAT YOU'RE IN LINE UNIT
                                 ;TEST
        OUT     BR,SELB,OBSEL6

                ;PICK UP CONSTANTS

        BRWRTE  IMM,40
        OUT     BR,SELB,OXREG2   ;SET LOOP BACK.

        ;NOW LOAD UP SILO

DLUTO:  BRWRTE  IMM,51           ;SET CRC16,IDLE,STRIP,, AND DDCMP
        OUT     BR,SELB,OXREG7
        BRWRTE  IMM,2
        OUT     BR,SELB,OXREG4   ;YOU ARE GOING TO SET
        BRWRTE  IMM,226
        OUT     BR,SELB,OXREG5   ;THE RECEIVER SYNC CHAR AT 226.
        BRWRTE  IMM,16
        OUT     BR,SELB,OXREG4
1$:     BRWRTE  IBUS,XREG4       ;WAIT TILL READY.
        BR7     2$
        CERROR                   ;ERROR-DID NOT BECOME READY,
                                 ;ERROR #61
        ALWAYS  1$
2$:     BRWRTE  IMM,O            ;CLEAR EXTENDED REG ENABLE
        OUT     BR,SELB,OXREG4   ;
DSHAME:
        NODST   IMM,O,LDMAR      ;NOW LOAD ADDR. O
        NODST   IMM,O,LDMAR      ;PUT ALL THE
                                 ;CHARACTERS THAT YOU
                                 ;WANT TO SEND IN MEMORY.

        MEMINC  IMM,1
        MEMINC  IMM,226          ;1ST SYNC
        MEMINC  IMM,1
        MEMINC  IMM,226          ;2ND SYNC
        MEMINC  IMM,O
        MEMINC  IMM,41           ;1ST CHAR.
        MEMINC  IMM,O
        MEMINC  IMM,125          ;2ND CHAR.
        MEMINC  IMM,O
        MEMINC  IMM,252          ;3RD CHAR.
        MEMINC  IMM,O
```

```
        MEMINC  IMM,377         ;4TH CHAR.
        MEMINC  IMM,2           ;SETS EOM
        MEMINC  IMM,O
        MEMINC  IMM,2
        MEMINC  IMM,O           ;2ND EOM
        MEMINC  IMM,2
        MEMINC  IMM,O           ;3RD EOM
        MEMINC  IMM,2
        MEMINC  IMM,O           ;4TH EOM.
        NODST   IMM,O,LDMAR     ;LOAD ADDR. O

        BRWRTE  IMM,1O.         ;NUMBER OF CHARACTER STORED MINUS
                                ;ONE.
        SP      BR,SELB,SP6
2$:     CERROR                  ;OUTPUT FAILED TO BECOME
                                ;READY IF FAILS HERE, ERROR #62
                                ;CHECK FOR SILO READY.
        BRWRTE  IBUS,XREG1
        BR4     3$
        ALWAYS  2$
3$:     BRWRTE  MEMI,SELB       ;GET DATA FOR OXREG1
        OUT     BR,SELB,OXREG1
        BRWRTE  MEMI,SELB       ;GET CHAR.
        OUT     BR.SELB,OXREGO

        SPBR    BR,DECA,SP6     ;DONE ENOUGH?
        Z       4$              ;DONE ENOUGH
        ALWAYS  2$
4$:
                                ;SILO IS NOW LOADED.

                                ;AFTER SILO IS LOADED IT TAKES
                                ;3 CLOCK CYCLES TO ACTIVATE, THEN
        BRWRTE  IMM,256         ;8 CYCLES TO OUTPUT 1ST SYNC CHAR
                                ;AS 1ST SYNC CHAR IS OUTPUTTED
        SP      BR,,SELB,SPO    ;THE NEXT ONE IS BEING LOADED INTO
                                ;THE USYRT (DOUBLE BUFFERED) 1ST
                                ;REAL CHAR
DLUTL:  SPBR    BR,DECA,SPO     ;ISN'T REALIZED (INPUT RDY-1) UNTIL
        Z       DLUT2           ;APP: 46 CLOCK CYCLES AFTER LOADED
        ALWAYS  DLUTL           ;APP: 1.9 MILLISEC


        ALWAYS  DLUT2
DLUT2:

        CERROR                  ;ERROR #63 IF NOT READY FOR FIRST
                                ;CHARACTER
        CALLSB  SPO,DINRDY      ;WAIT FOR READY

        SP      IBUS,XREGO,SP1  ;READ 1ST CHAR FROM SILO
```

```
        BRWRTE  IMM,41
        NODST   BR,SUBOC,SP1        ;IF 1ST CHAR=O THEN IT WILL BE 377
        Z       DLUT20              ;BR IF OK
        CERROR                      ;ERROR #64 IF FIRST CHAR DATA BAD
        ALWAYS  DLUTER              ;ELSE GO TO ERROR

DLUT20: CERROR                      ;WAITING FOR 2ND CHAR, ERROR #65
        CALLSB  SPO,DINRDY          ;WAIT FOR READY
        SP      IBUS,XREGO,SP1      ;READ SECOND CHAR FROM SILO
        BRWRTE  IMM,125             ;SHOULD BE BACK = 125
        NODST   BR,SUBOC,,SP1       ;DO ONE'S COMP SUB = 377 EQUAL
        Z       DLUT2A              ;BR IF OK
        CERROR                      ;ERROR #66 IF SECOND CHARACTER DATA
                                    ;ERROR
        ALWAYS  DLUTER              ;ELSE GO TO ERROR
DLUT2A: CERROR                      ;WAITING FOR 3RD CHAR, ERROR #67
        CALLSB  SPO,DINRDY          ;WAIT FOR RDY
        CERROR                      ;ERROR #10 IF BCC DATA ERROR
        SPBR    IBUS,XREG2,SP2      ;LOOK AT BCC BIT, S/B CLEAR
        BRO     DLUTER              ;IF SET GO TO ERROR
DLUT2B:
        SP      IBUS,XREGO,SP1      ;READ THIRD CHAR FROM SILO
        BRWRTE  IMM,252             ;S/B A 252
        NODST   BR,SUBOC,SP1        ;DO ONE'S COMPSUB = 377 IF EQUAL
        Z       DLUT2C              ;BR IF OK
        CERROR                      ;ERROR #70 IF THIRD CHARACTER DATA
                                    ;ERROR
        ALWAYS  DLUTER              ;ELSE GO TO ERROR

DLUT2C: CERROR                      ;WAITING FOR 4TH CHAR, ERROR #71
        CALLSB  SPO,DINRDY          ;WAIT FOR CHAR
        BRWRTE  SELB,XREG2          ;READ REG 12
        BRO     DLUT3               ;BIT O S/B SET (BCC BIT)
        CERROR                      ;ERROR #72 IF BCC BIT NOT CLEAR
        ALWAYS  DLUTER              ;IF NOT, ERROR

DLUT3:  SP      IBUS,XREGO,SP1      ;READ 4TH CHAR
        Z       DLUT4               ;IF 377 EXIT
        CERROR                      ;ERROR #73 IF FOURTH CHAR DATA
                                    ;ERROR
        ALWAYS  DLUTER              ;ELSE REPORT ERROR

DLUT4:  CERROR                      ;WAITING FOR 1ST CRC CHAR,
                                    ;ERROR #74
        BRWRTE  IMM,377
        SP      BR,SELB,SP7         ;INDICATE PAGE 2 RETURNS.
        CALLSB  SPO,DINRDY          ;WAIT FOR CHAR
        SP      IBUS,XREGO,SP1      ;READY 1ST CRC CHAR
        BRWRTE  IMM,44              ;S/B 44
        NODST   BR,SUBOC,SP1        ;COMPARE IF EQUAL, RESULTS =377
        Z       DLUT5               ;ERROR #75 IF FIRST CRC CHAR BAD
        CERROR                      ;1ST CRC CHAR WRONG!
        ALWAYS  DLUTER
```

```
DLUT5:  CERROR                          ;WAITING FOR 2ND CRC CHAR,
                                        ;ERROR #76
        CALLSB  SPO,DINRDY              ;WAIT FOR NEXT CHAR
        SP      IBUS,XREGO,SP1          ;READ LAST CRC CHAR
        BRWRTE  IMM,314                 ;S/B 314
        NODST   BR,SUBOC,SP1            ;COMPARE IF EQUAL, RESULTS = 377
        Z       DLUTE                   ;IF=,EXIT
        CERROR                          ;2ND CRC CHAR WRONG, ERROR #77
        ALWAYS  DLUTER                  ;ELSE, ERROR
DLUTE:

        BRWRTE  IMM,200                 ;NOW CLEAR XMITTER AND RECEIVER
        OUT BR,SELB,OXREG1              ;FIRST CLEAR THE XMITTER.
                                        ;THIS WILL RESULT IN THE
                                        ;UNUSEABILITY OF THE XMITTER FOR
                                        ;8 MICRO-SECONDS

        OUT     BR,SELB,OXREG2          ;NEXT CLEAR THE RECEIVER.
                                        ;NOW THE LINE UNIT IS IN THE STATE IT
                                        ;WAS IN BEFORE YOU
                                        ;CAME TO IT.

DLUTER: ALWAYS  DIADON                  ;END OF TESTS GO TO DMP CODE

DINRDY -        ROUTINE USED BY LINE UNIT
                TEST TO WAIT FOR "RDY"
                PROGRAM COULD HANG HERE


DINRDY:
1$:
        SPBR    IBUS,XREG2,SP2
        BR4     DINEX
        ALWAYS  1$
DINEX:
DINEXO: RTNSUB  SPO,P2

DIADON: BWRITE  IMM,305                 ;CODE SPECIFYING COMPLETION OF
        OUT     BR,SELB,OBSEL6          ;INTERNAL MICRO-DIAGNOSTICS

        MICRODIAGNOSTICS END, USER INIT CODE STARTS
```

APPENDIX B
RECOMMENDED CABLES/CONNECTORS

B.1 SCOPE

Twinax and Triax cable specifications are provided in this appendix. The customer must purchase cables that adhere to the specifications presented. Cabling and wiring practices and associated connectors necessary for successful installation of the M8203 are discussed in detail.

B.2 CABLING RECOMMENDATIONS

The line unit is set up for use with the seven standard cables indicated in Table 1-1. DIGITAL does not sell cables of over 100 feet for use with Integral Modem Line Units. DIGITAL sells (1), the BC55N – 30 meter (98 ft) cable for all speeds in point-to-point operation or 56K bps in multipoint operation and (2), the BC55M – 30 meter (98 ft) cable for 250K bps, 500K bps, and 1M bps in multipoint operation.

NOTE

The cable should be provided and installed by the customer.

B.3 CABLE SPECIFICATIONS

The M8203 runs on multidrop or point-to-point lines from 75 to 150 ohms. All terminations of the line must be done in the cabling of the system.

Point-to-point lines should be terminated at the receiver end while multidrop lines should be terminated at both ends of the line.

There is no interlock between the cable and the line unit for half-duplex operation. A bit must be set in the line unit to inform the microcode to select the half-duplex mode.

The total loading effect of the units on the line for a multidrop system should not be lower than the impedance on the line. Both the driver and receiver on the M8203 can withstand a 30 decibel (dB) drop on the line, with restrictions of 20% maximum distortion.

Refer to Table B-1, Belden Twinax Cable Specifications and Table B-2, Belden Triax Cable Specifications.

Table B-1 Belden Twinax Cable Specifications

PARAMETER	BELDEN CABLES	
	9182 (or equivalent)	9272
Impedence	150 ohms	78 ohms
DC Resistance Conductors	22 AWG stranded tinned copper (19 strands of 34 AWG) 46 ohms/km (14 ohms/1000 ft)	20 AWG stranded tinned copper (7 strands of 28 AWG) 31.2 ohms/km (9.5 ohms/1000 ft)
Shield	Foil with drain wire 100% coverage 20.7 ohms/km (6.3 ohms/ 1000 ft)	Copper braid 93% coverage 12.5 ohms/km (3.8 ohms/ 1000 ft)
Capacitance		
Between wires in a pair	28.9 pF/m (8.8 pF/ft)	64.6 pF/m (19.7 pF/ft)
One wire to shield	57.8 pF/m (17.6 pF/ft)	129.3 pF/m (39.4 pF/ft)
Voltage Rating	300 volts	300 volts
Velocity of Propagation	78%	66%
Insulation	Polypropolalene	Polyethylene
Jacket	Polyvinal chloride (PVC)	Polyvinal chloride (PVC)

Table B-2 Belden Triax Cable Specifications

PARAMETER	BELDEN CABLES	
	8232	8233
Impedance	75 ohms	75 ohms
DC Resistance		
Center Conductor	20 AWG Copperweld 112 ohms/Km (35 ohms/1000 ft)	14 AWG Solid Copper 8.5 ohms/km (2.6 ohms/1000 ft)
Shield	8.53 ohms/km (2.6 ohms/1000 ft)	4.6 ohms/km (1.4 ohms/1000 ft)
Capacitance	56.7 pF/m (17.3 pF/ft)	same
Inductance	0.318 microhenry/meter (0.097 microhenry/ft)	same
Velocity of Propagation	78%	same
Voltage Rating	175 Vrms	same
Sweep Test	22 dB minimum	same
Physical Requirements	Triaxial, cellular polyethylene insulation and minimum of:	
Center Conductor	20 AWG	14 AWG

B.3.1 Cable Resistance Versus Distance

B.3.1.1 Twinax Cables – The cable must have a characteristic impedance of 72 to 150 ohms. The two conductors must be tied together at one end of the cable and the dc resistance measured between the two conductors at the other end. The maximum total capacitance between conductors for the Belden 9182 must be less than .07 uF for a cable length of 2 km (6562 ft.) and .21 uF for 6 km (19,865 ft).

The jacket for both cables is polyvinal chloride (PVC). These cables may not be suitable for outdoor or direct inground installations (check manufacturer's recommendations).

B.3.1.2 Triax Cables – The cable used must have a characteristic impedance of 75 ohms. The shield and center conductor should be shorted at one end of the cable and the dc resistance measured between the shield and center conductor at the other end. The maximum total dc resistance for the Belden 8232 cable shield and center conductor must be less than 200 ohms for a cable length of 2 km (6562 ft), and 400 ohms for a cable length of 6 km (19,685 ft). The maximum total resistance for the Belden 8233 cable shield and center conductor must be less than 30 ohms for a cable length of 2 km (6562 ft) and 90 ohms for 6 km (19,865 ft).

The maximum total capacitance from the shield to the center conductor must be less than 0.14 uF for the 2 km (6562 ft) cable and 0.4 uF for the 6 km (19,685 ft) cable. The double shield provides excellent noise rejection when properly grounded. The cellular polyethylene dielectric provides low signal loss and low distortion. The polyethylene jacket has excellent weather and abrasion resistance. However, this does not mean that these cables are suitable for outdoor or direct inground installations (check manufacturer's recommendations).

NOTE

Typical cables using 20 AWG copper weld center conductors vary from 35 to 70 ohms dc resistance. Use of dc resistance over 112 ohms per km (35 ohms per 1000 ft) severely derates the maximum length of the cable. The longer cable must use solid copper, 14 AWG.

B.3.2 75 Ohm Systems

For 75 ohm systems, the cable must be twinax or triax. The recommended cable for 56K bps is a twinax cable, Belden 9272. For higher speed, triax cables should be used.

BELDEN 9272

- 56K bps, 6 km (18K ft) point-to-point and up to 24 loads multidrop.
- Over 24 loads, the maximum distance is derated by 73 meters (240 ft) per M8203 transformer loads and 25 meters (80 ft) per DMV11 transformer loads.
- Higher speeds can be run with Belden 9272 with no derating for loads.
- 250K bps, point-to-point or multipoint maximum distance is 2 km (6K ft) (maximum128 transformer loads).
- 500K bps, point-to-point or multipoint maximum distance is 1.2 km (4K ft) (maximum 128 transformer loads).
- 1M bps, point-to-point or multipoint maximum distance is 600 Meters (2K ft) (maximum 64 transformer loads).

There are two recommended triax cables: (1), the Belden 8232 is easy to work with and (2), the Belden 8233 for long runs which, however, is difficult to work with (the center conductor is 14 AWG). Triax cables work best in higher speeds of 250K bps to 1M bps.

BELDEN 8232

- 56K bps, point-to-point and multipoint up to 20 transformer loads with a maximum distance of 4.3 km (14K ft). Above 20 transformer loads derate at 76 meters (250 ft) per M8203 transformer load. (DMV11 loads derate the maximum length by 37 meters (120 ft).)

- 250K bps, point-to-point or multipoint maximum distance is 3 km (10K ft) and no derating (maximum 128 transformer loads).

- 500K bps, point-to-point or multipoint maximum distance is 3 km (10K ft) and no derating (maximum 128 transformer loads).

- 1M bps, point-to-point or multipoint maximum distance is 2 km (6K ft) and derating (maximum 128 transformer loads).

BELDEN 8233

- 56K bps, point-to-point and multipoint up to 20 transformer loads maximum length is 6 km (18K ft). Above 20 transformer loads derating is at 55 meters (180 ft) per transformer load.

- 250K bps, point-to-point or multipoint maximum length is 5 km (16K ft) and no derating (maximum 128 transformer loads).

- 500K bps, point-to-point or multipoint maximum length is 3.7 km (12K ft) and no derating (maximum 128 transformer loads).

- 1M bps, point-to-point or multipoint maximum distance is 3 km (10K ft) and no derating (maximum 128 transformer loads).

NOTE

All derating for transformers relates only to the transformers used on the M8203. All others must be characterized and specified on an individual basis.

B.3.3 150 Ohm Systems

The cable is the Belden 9182 or equivalent, which is a twinax point of sale cable developed for the DECdataway.

This cable should only be used for 56K bps. The twinax cable produces a higher level of distortion than the triax, with the major limiting factor of distortion not attenuation. The 9182 cable is harder to work with because it is not as flexible as the 9272 or 8232. It also uses a polypropolene base inner insulation which is highly flammable when the ends of the cable are stripped back and the inner insulation is exposed.

- 56K bps, point-to-point and multipoint up to 10 M8203 loads maximum length is 4.5 km (15K ft) without derating for loads. Derating for loads is 110 meters (360 ft) per M8203 load. (DMV11 derates the maximum length by 23 meters (75 ft) per load).

- 250K bps, point-to-point and multipoint maximum length is 3 km (10K ft) with no derating for loads.

- 500K bps, point-to-point and multipoint maximum length is 2.5 km (8K ft) with no derating for loads.

- 1M bps, point-to-point and multipoint maximum length is 1.2 km (4K ft) with no derating for loads but with a maximum of 64 loads.

B.3.4 Cable Attenuation

When selecting a cable, several factors must be considered in determining cable attenuation. The value given by the cable vendor is for room temperature and is nominal, being subject to deviations of up to 20 percent. The attenuation increases with temperature at approximately 0.20 percent per degree Celsius (0.11 percent per degree Fahrenheit). At 50° C (122° F) an additional loss of 5 percent over the room temperature specification can be expected. Finally, use at elevated temperatures causes aging at a faster than normal rate and, after 5 years, could produce yet another permanent 10 percent increase in attenuation. Thus, the initial nominal 8.53 dB/km (2.6 dB/1000 ft) loss could become, after 5 years use at high temperature, 17.06 dB/km (5.2 dB/1000 ft).

B.4 INSTALLATION CONSIDERATIONS

The characteristics of the local link cable should be measured prior to installation. In particular, there are two parameters that the user should measure and note for future reference. These are the propagation time delay, which can be measured with a pulse generator and an oscilloscope, and the dc resistance of the cable with the far end of the center conductor shorted to the inner shield. For the Belden 8232, these parameters can be expected to be nominally 4.26 ns/m (1.30 ns/ft) and 105 ohms/km (32 ohms,1000 ft). For Belden 8233, these parameters can be expected to be nominally 4.26 ns/m (1.30 ns/ft) and 13 ohms/km (4 ohms/1000 ft). Once the cable is installed, and both ends are therefore not available at the same place, the latter parameter can still be measured easily, and the former can be measured by use of the time domain reflectometry (TDR) method described in Chapter 4, Service.

While installing the cable, a complete map of its layout should be made showing the position of the cable with respect to buildings, equipment and so forth, and also the locations of all access points, including not only splices and in-line connectors, but pull boxes as well. Cable lengths between landmarks should be carefully measured and recorded. Such a map greatly facilitates maintenance.

The following factors must be taken into account when installing the local link cable.

TEMPERATURE – The polyethylene used as the dielectric material in most coaxial and triaxial cables begins to soften at temperatures above 80° C. As the conductor moves off center, variations in cable characteristics occur. If installed under tension with sharp bends, the conductor may short to the shield. Additionally, the open circuit resistance should be measured after installation to ensure against shorts incurred during installation. This resistance should be ⩾20K ohms. The closed circuit resistance should be 118.4 ohms/km (36.1 ohms/1000 ft).

MOISTURE – Moisture, or moisture related impurities, may enter the cable through cuts or scratches in the outer jacket or through improperly installed connectors. Minute amounts of water vapor will condense into water, which can migrate along the braid. Water condensed from a polluted atmosphere can contaminate the entire length of cable, shorten its lifetime, and seriously degrade performance.

PULLING TENSION – For most environmental conditions, it is generally preferred that the cable be installed in a conduit, through which the cable must be pulled. During installation, the total pulling tension on the 20 AWG center conductor must not exceed 8.8N (2 pounds).

For ease in maintenance, it is best to divide the cable into sections. For long cable runs in a conduit, it is convenient to have a pull box every 30.48 meters (100 ft). A 90 degree conduit bend is equal to 9.15 meters (30 ft) of straight level conduit. It is also recommended that an antifriction agent be used during pulling, providing that the agent is compatible with the cable jacket material.

SPLICES AND CONNECTORS – The cable layout should provide access points for test purposes and for replacing defective sections. Strain relief must be provided at all splices and in-line connectors.

RECOMMENDED WIRING PRACTICES – Chapter 8, Article 800 of the *National Electric Code* defines wiring rules for communications circuits. These rules must be observed for safe operation of the line unit. In particular, the following provisions of the code should be noted.

"Communication conductors shall not be placed in a raceway, compartment, outlet box, junction box or similar fitting with conductors for light and power..."

"Communication conductors may be run in the same shaft with conductors for light and power provided the conductors of the two systems are separated by at least two inches."

"Suitable protective devices must be employed for wiring between buildings."

SURGE WITHSTAND CAPABILITY – The receiver has no provision for protection against normal mode voltage (voltage across the receiver input) surges exceeding 30 volts. If surge withstand is required, a separate circuit must be installed to condition signals to the receiver.

NOISE – The M8203 is designed to operate with a common mode rejection ratio 500:1. Cable selection, installation grounding and noise suppression are means of reducing line error rates.

B.5 RECOMMENDED CONNECTORS

The following components are recommended for use in joining cable sections and also for connecting the cable to the M8203 BC55A panel. All of these components, which are shown in Figure B-1, are manufactured by AMP Inc., Harrisburg, Pennsylvania.

Component	DIGITAL Part Number	AMP Part No.
Small cable clamp	12-11430-00	206062-1
Large cable clamp	12-11430-01	206358-1
Male housing	12-12527	206153-1
Male pin	12-12001	66589-2
Female housing	12-12526	206060-1
Female pin	12-12000	66590-2
14 ga male pin	12-12001-1	66587-2

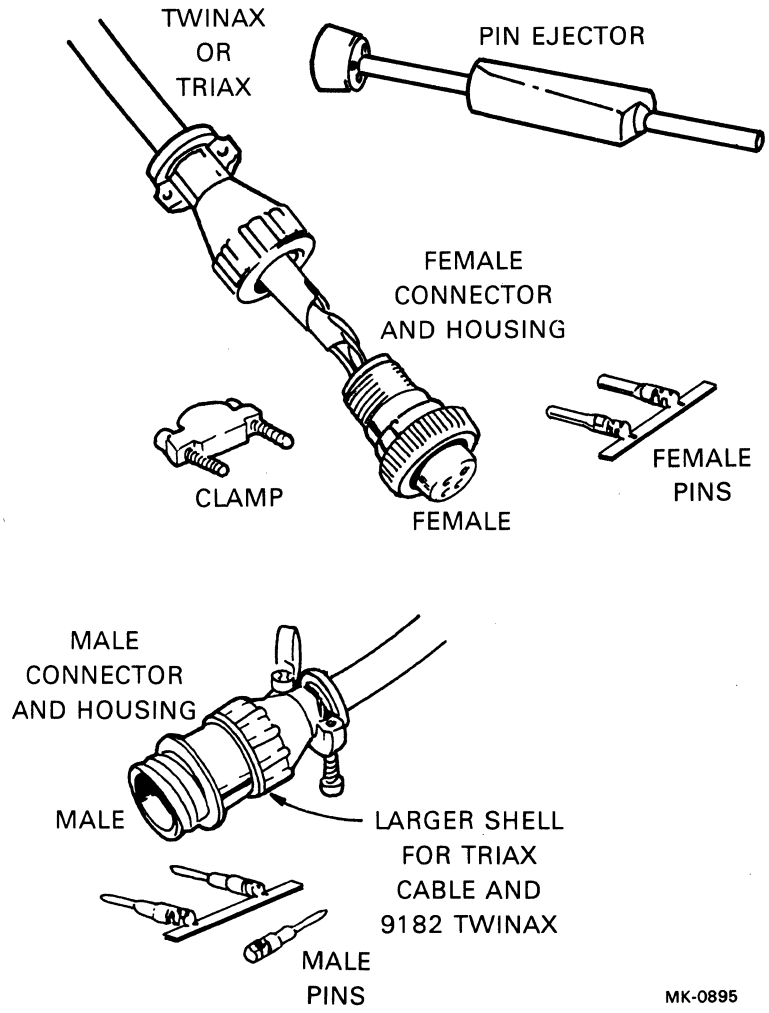


Figure B-1 Local Link Cable Connectors

The connectors are installed by crimping the pins to the cable; the recommended crimper is the AMP Type V1, 90277-1. It is very unlikely that one can install a set of connectors without requiring the use of an ejector, to remove pins that have been inserted incorrectly. The proper ejector for the above pins is the AMP 305183.

The pin holes in the housing and receptacle are numbered. When working with a connector, it should always be oriented so that hole 1 (signal +) is at the top, hole 4 (outer shield) is at the bottom, and the holes on either side are 2 (signal −) and 3 (second signal −, used with triax only).

NOTE

The system should be polarized and must be terminated at both ends. The system should be such so that any computer system can be removed and the connectors tied together without the need for additional ports.

1. The cable clamp assembly is supplied as a shell, with two screws and three clamps, of which the one for the largest cable size should be used. The shell slides on the cable.

2. The center conductor must be dressed back enough so it will fit into a pin with the pin crimped back to its insulation as well as to the conductor. Both shields must be dressed back about another half inch, and the final half inch of the inner insulation tapered so that its tip fits into the pin, and about a quarter inch fits into the connector along with the center conductor. The appropriate male/female pin must then be crimped to both the conductor and its insulation, and inserted in the hole.

    a. For twinax cables, appropriate pins are simply crimped, as indicated in the previous statement, to the colored wire of the pair.

3. For triax cables, the inner shield must be separated into two parts, the pins attached to them, and inserted into holes 2 and 3. For twinax cables, the pins are attached to the transparent or black wire and inserted into hole 2.

4. The outer shield is then pulled together, insulated from the inner shield, a pin crimped to it, and inserted in hole 4 for splicing connections.

5. The shell must be screwed into the housing, and the clamp screwed to the shell.

6. After male and female connectors have been plugged together, the other ring of the female housing must be screwed over the male housing.

B.6 GROUNDING RECOMMENDATIONS

This paragraph describes the proper grounding techniques that must be used to prevent the possibility of personal injury.

There is a possibility of a difference in ground potential between two computers that are separated by some distance, especially if they are powered from different sockets.

If in doubt about the recommendations in this paragraph, consult a competent professional (Electrical/Electronic Engineer) for advice.

The following warnings should be adhered to:

WARNING

1. **The outer shield of the local link cable is connected to the computer cabinet by the BC55A at each drop.**

2. **The difference in grounds must be checked before connecting the cable to the BC55A panel.**

   Ideally, the potential difference should be near zero. If a potential difference does exist, it is advisable to check with higher levels of Field Support authority.

The computer system chassis must be grounded. The grounding conductor should be connected to a water pipe electrode, or if none is available, to the power service conduit, service equipment closure, or grounding electrode conductor where the grounding conductor of the power service is connected to a water pipe electrode at the building.

When neither of the above means of grounding is available, it is permissible to connect the grounding conductor to the service conduit, service equipment enclosure, grounding electrode conductor, or grounding electrode of the power service of a multigrounded neutral power system.

If it is impossible to ground the computer system chassis by one of the above methods, the grounding conductor must be connected to one of the following:

1. A concrete-encased electrode of not less than 6.09 meters (20 ft) of bare copper conductor, no smaller than 4 AWG, encased in at least 5.08 cm (2 in) of concrete, and located within and near the bottom of a concrete foundation footing that is in direct contact with the earth.

2. An effectively grounded metal structure.

3. A continuous and extensive underground gas-piping system, where acceptable to both the servicing gas supplier and to the authority having jurisdiction.

4. A ground rod or pipe driven into permanently damp earth.

NOTE

The minimum ground wire size is 4 AWG.

WARNING

Under no circumstances shall the grounding conductor be connected to a steam or hot water pipe, a lightning rod conductor, or pipe or rod electrodes grounding other than multiground neutral power circuits.

APPENDIX C
INTEGRATED CIRCUIT DESCRIPTIONS

C.1 INTRODUCTION

Selected integrated circuits (IC) shown in the *M8203 Print Set* are provided in this appendix as an aid in troubleshooting to the IC level. The descriptions include one or more of the following: pin/signal designations, equivalent logic block diagrams, logic symbols, and truth/function tables.

The following ICs are included:

26LS29	Quad Three-State Single Ended RS-423-A Line Driver
26LS30	Quad Driver RS-422-A/RS-423-A
26LS31	Quad Driver RS-422-A High Speed
26LS32	Quad Differential Line Receiver RS-422-A/RS-423-A
2652	USYRT, Universal Synchronous Receiver/Transmitter
3341	Four-Bit × 64 Word Propagable Register (FIFO)
3603	High Speed Dual Line Receivers
74S138	Decoder Multiplexer
74S151	Data Selectors/Multiplexers
74LS161	Synchronous Four-Bit Counter
74S174	HEX/QUAD D-Type F-F with Clear
74S240	Octal Inverter and Line Driver with 3-State Output
74LS244	Octal Three-State Buffer
74LS374	Octal D-Type Transparent Latches & Edge-Triggered FF
75110	Dual Line Driver
93S16	BCD Decade/Four-Bit Binary Counter

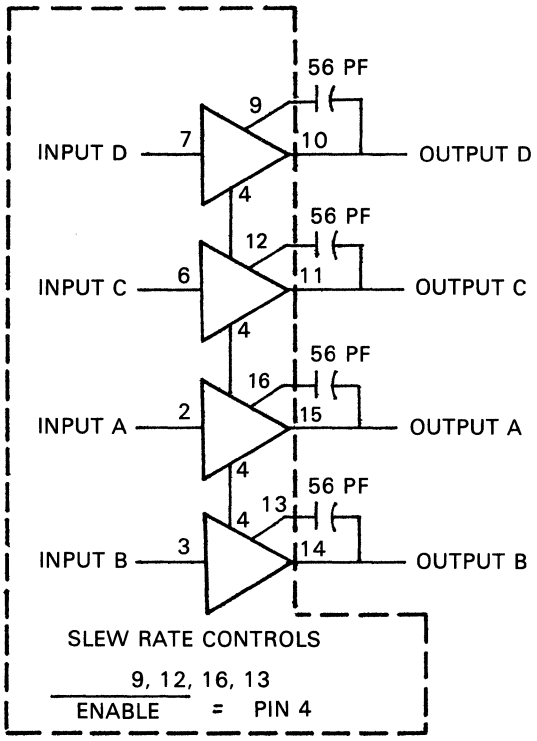
C.2 SELECTED INTEGRATED CIRCUITS

26LS29 – Quad Three-State Single-Ended RS-423-A Line Driver

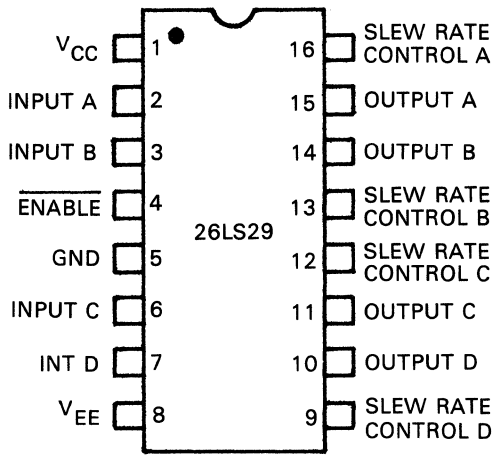
The 26LS29 is a quad single-ended line driver which meets all requirements of the Electronics Industries Association (EIA) Standard RS-423-A and Federal Standard 1030. This line driver features four buffered outputs with high source and sink current, and output short circuit protection.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

LOGIC DIAGRAM
26LS29



CONNECTION DIAGRAM
TOP VIEW



NOTE: PIN 1 IS MARKED FOR ORIENTATION.

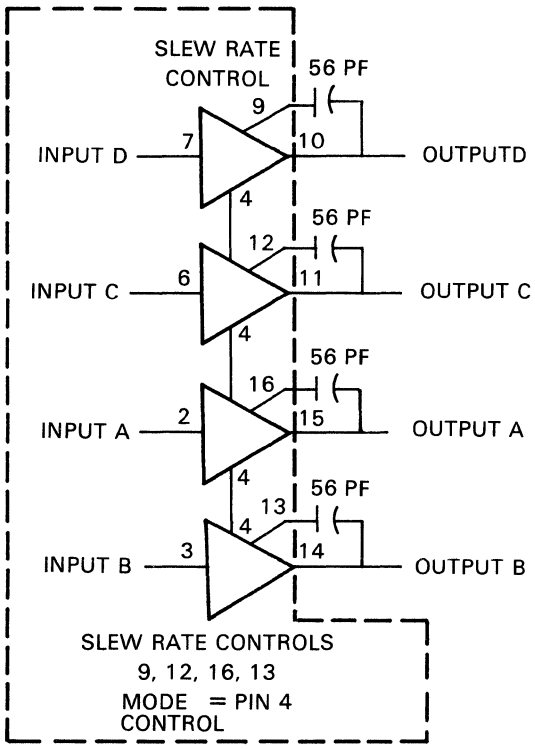
MK-0950

26LS30 – Quad Single-Ended RS-423-A Line Driver

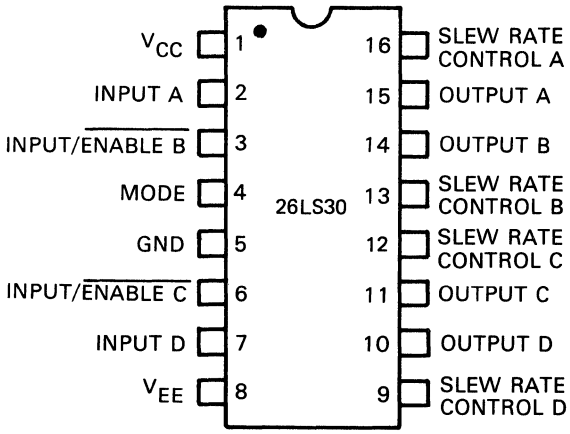
The 26LS30 is a single-ended line driver which meets all of EIA Standard RS-423-A. The line driver features four independent single-ended outputs. A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

LOGIC DIAGRAM
26LS30

TYPICAL APPLICATION



CONNECTION DIAGRAM — TOP VIEW



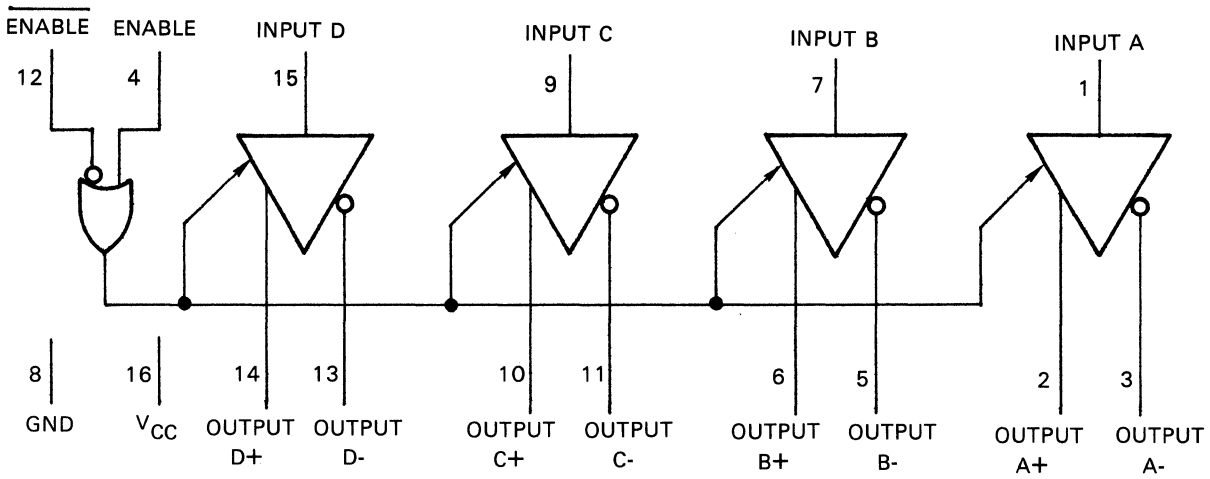
NOTE:
PIN 1 IS MARKED FOR ORIENTATION.

MK-0949

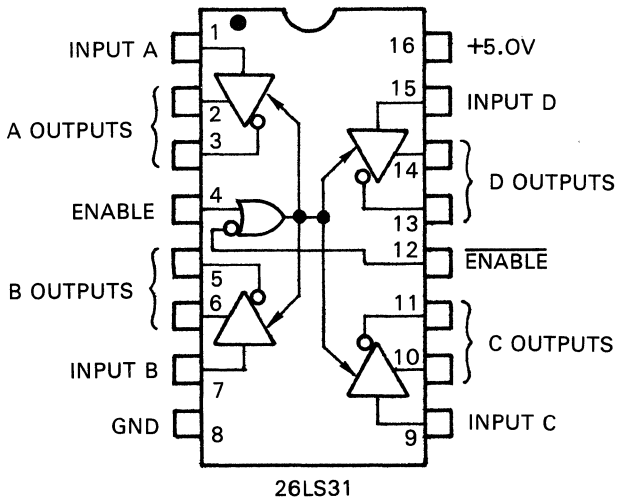
26LS31 - Quad High Speed Differential Line Driver

The 26LS31 is a quad differential line driver which meets all of the requirements of EIA Standard RS-422-A and Federal Standard 1020. This line driver provides unipolar differential drive to twisted-pair or parallel-wire transmission lines. The circuit also provides an enable and disable function common to all four drivers.

LOGIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



26LS31

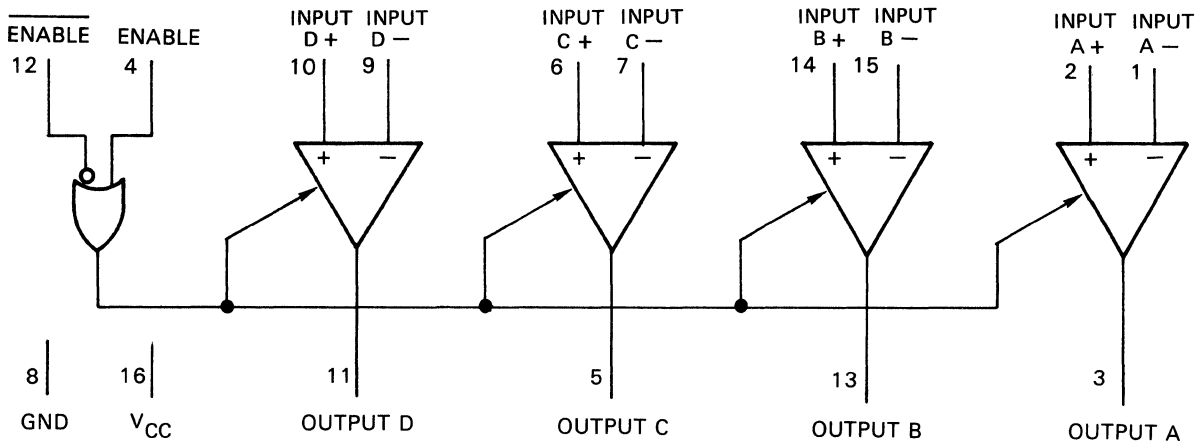
NOTE: PIN 1 IS MARKED FOR ORIENTATION.

MK-0938

26LS32 - Quad Differential Line Receiver

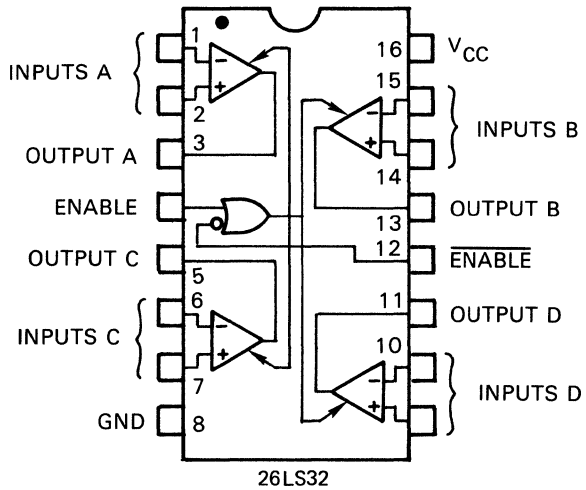
The 26LS32 is a quad line receiver which meets the requirements of EIA Standards RS-422-A, RS-423-A, and Federal Standards 1020 and 1030. The circuit provides an enable and disable function common to all four receivers. The 26LS32 features 3-State outputs and incorporates a failsafe input-output relationship which keeps the outputs high when the inputs are open.

LOGIC DIAGRAM



CONNECTION DIAGRAM

TOP VIEW



26LS32

NOTE: PIN 1 IS MARKED FOR ORIENTATION

MK-0937

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2652 – Universal Synchronous Receiver/Transmitter (USYRT)
Complete serialization, deserialization and buffering is provided by the data paths of the USYRT. Output signals are provided to the USYRT controller to indicate the state of the data paths. The internal logic does not provide the intelligence to make higher level decisions such as incorporation of command fields or recognition of extended address fields. These tasks must be performed by the USYRT controller.

The USYRT is a dual-in-line package (DIP). A terminal connection (identification) diagram is presented in Figure C-1.

Data port bits DP07:DP00 are dedicated to service four eight-bit wide registers. Bits DP15:DP08 **service either control information or status registers. The PCSCR register is reserved and the M8203** Line Unit uses this register as a test register for the modem interface (does not affect the USYRT). (See Table C-1.)

A suggested block diagram is shown in Figure C-2 and receive and transmit signal timing waveforms are given in Figures C-3 and C-4 respectively. Figure C-5 shows the timing waveforms at the tri-state outputs.

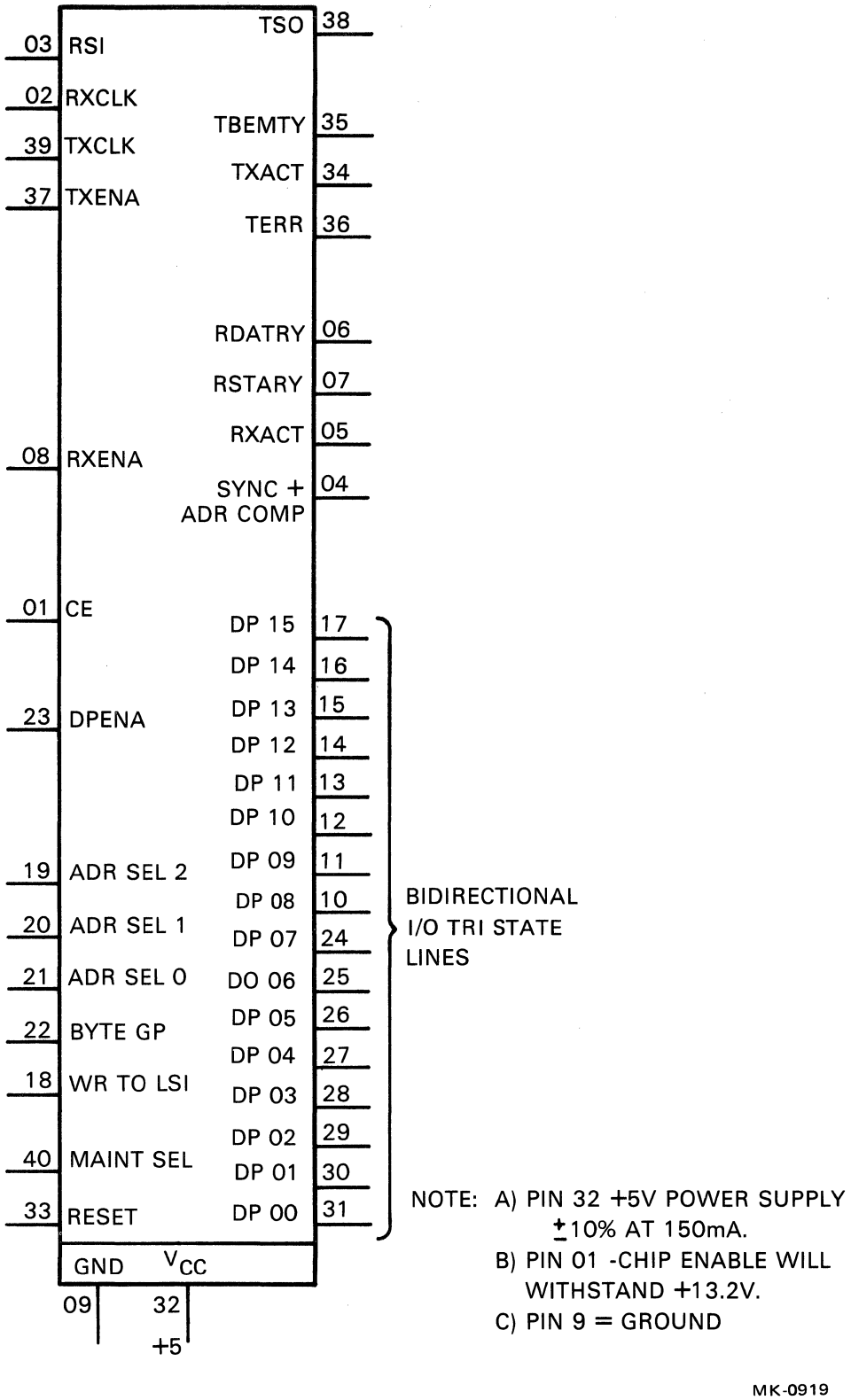


Figure C-1 Terminal Connection (Identification) Diagram
(2112517-01 Variation)

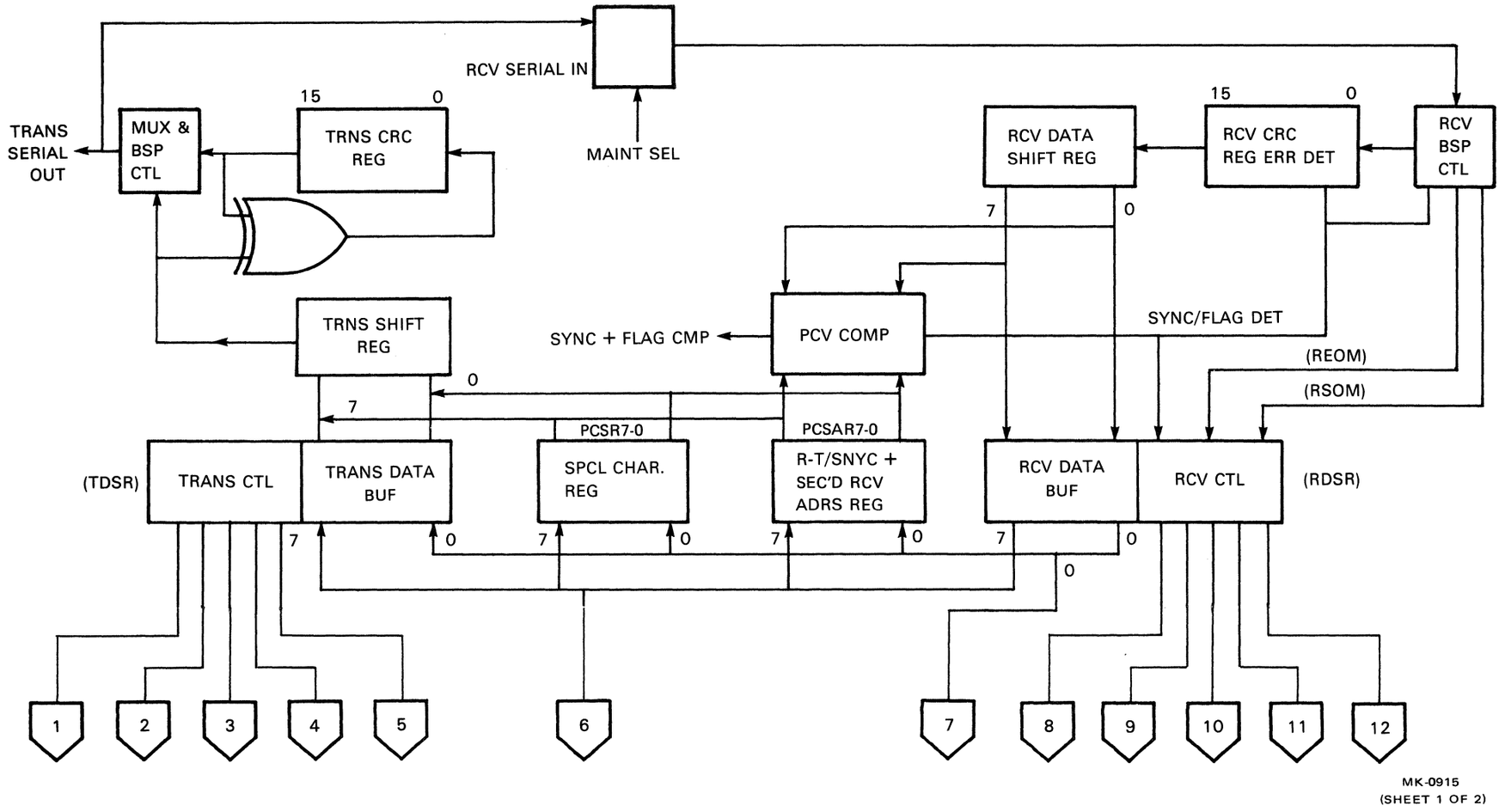


Figure C-2 Suggested Block Diagram (Sheet 1 of 2)

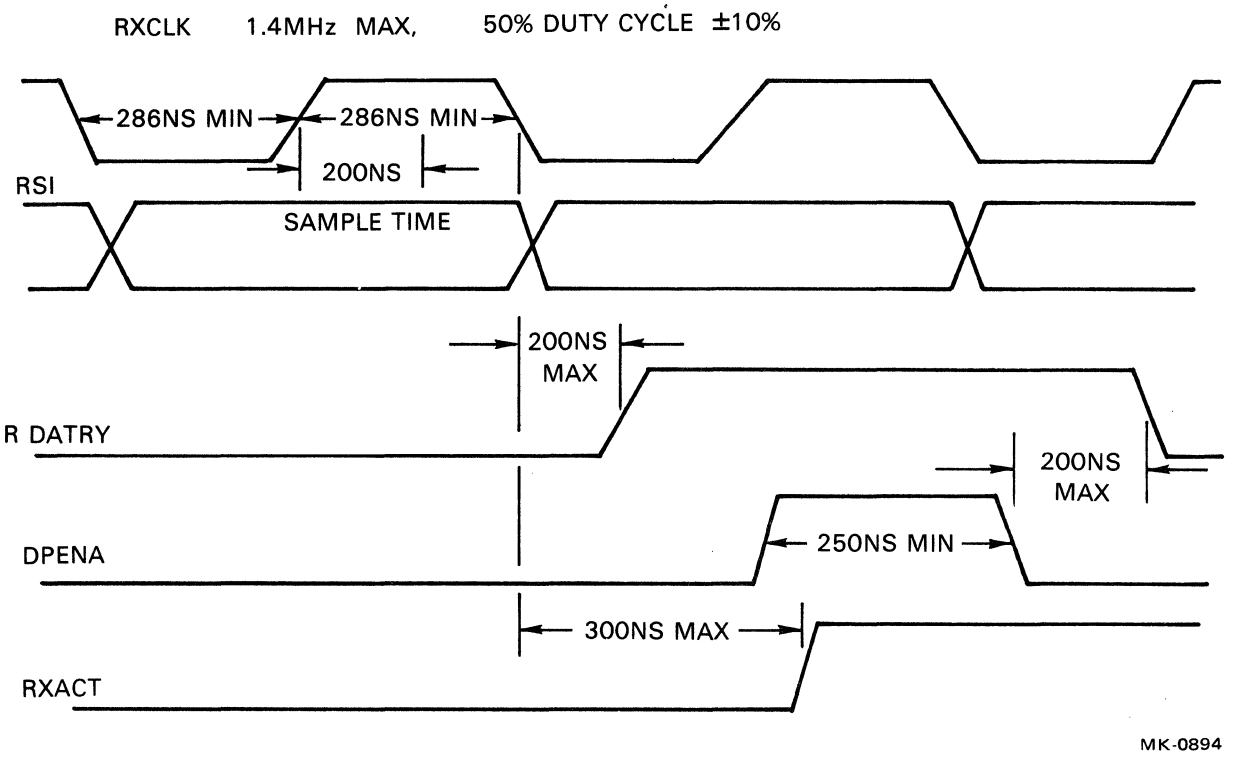


Figure C-3 Receive Signal Timing Waveforms

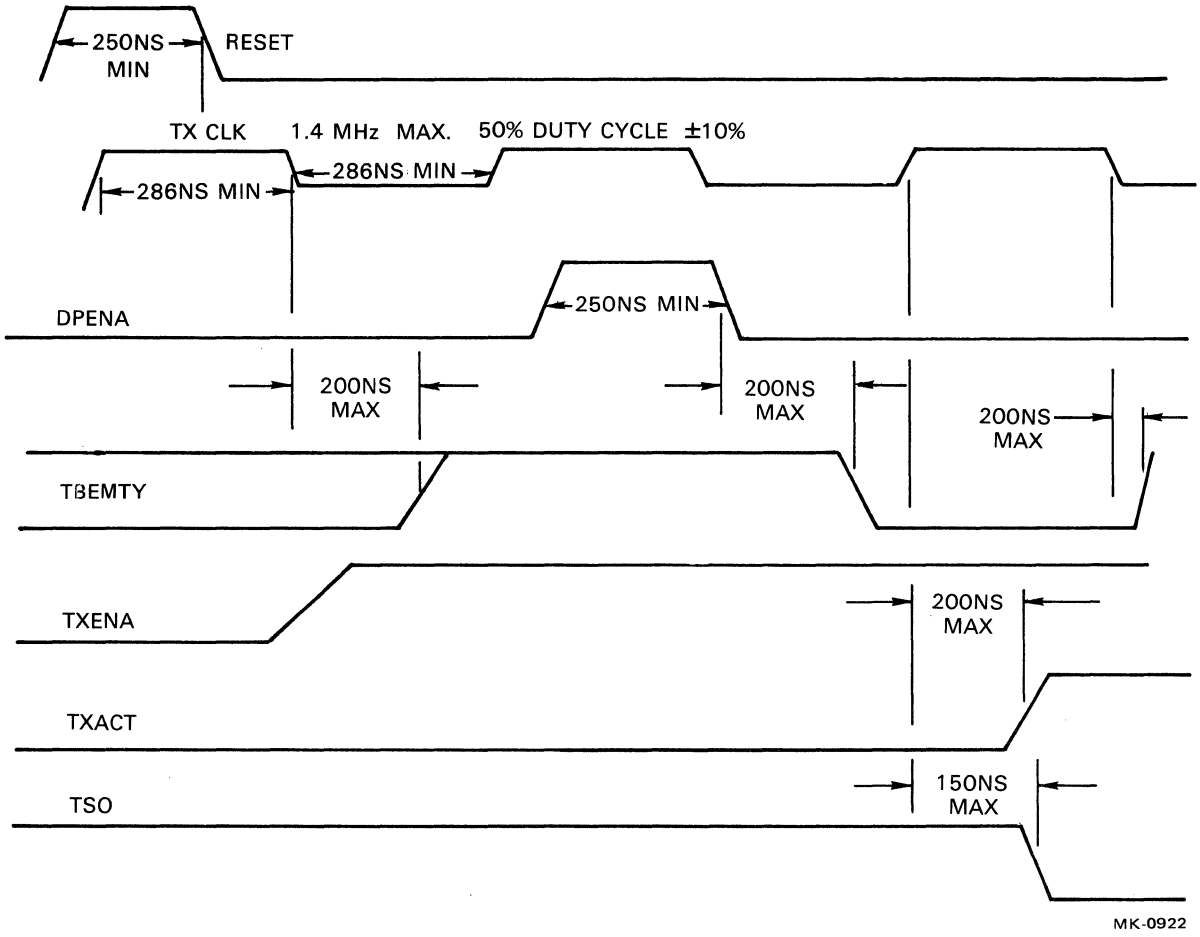


Figure C-4 Transmit Signal Timing Waveforms

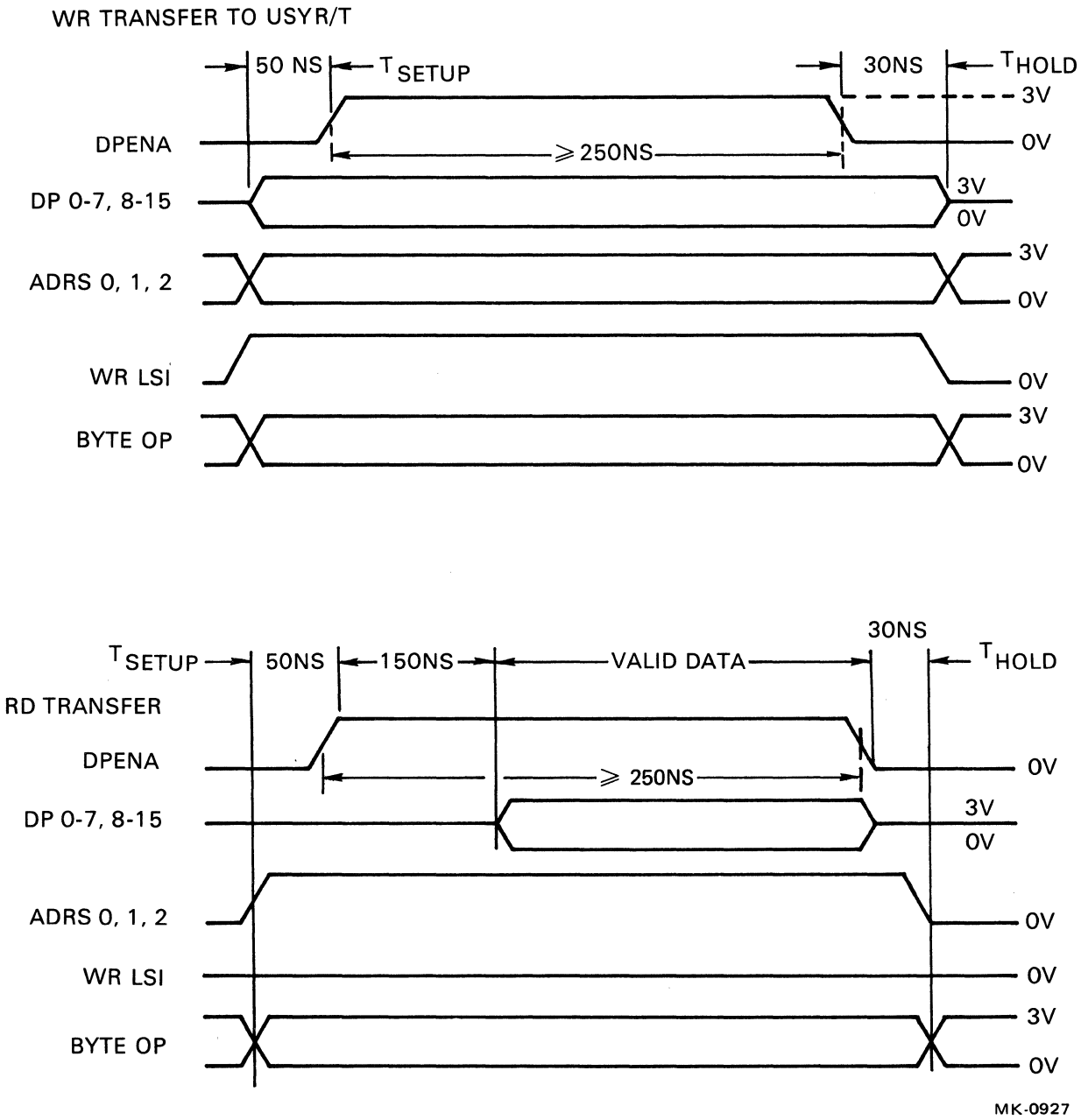


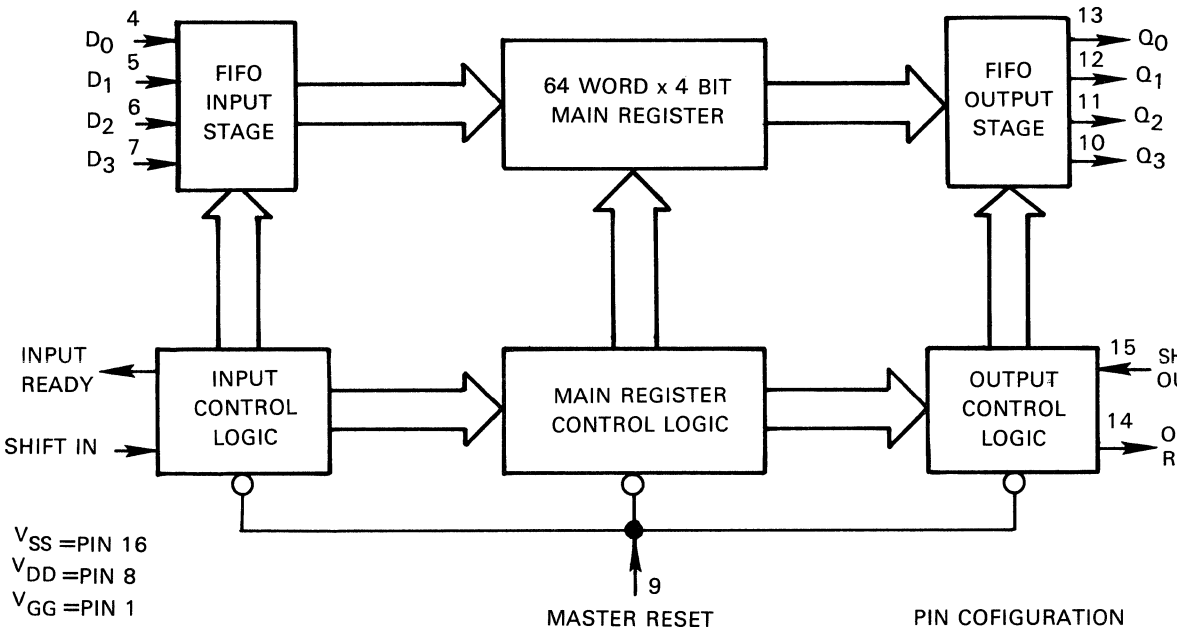
Figure C-5 Tri-State Output Waveforms

3341 – Four-Bit × 64-Word Propagable Register (FIFO)

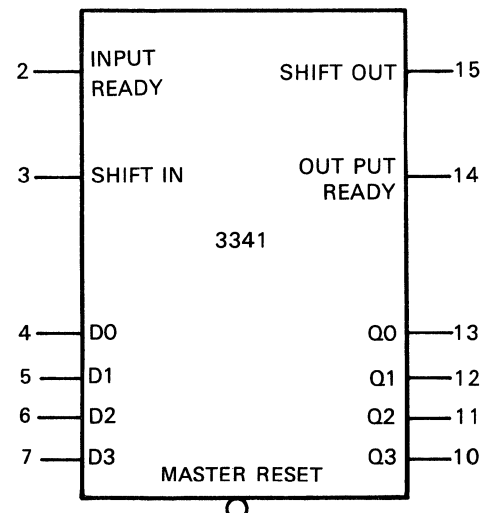
The 3341 is a 64-word × 4-bit memory that operates in a first in first out (FIFO) mode. Inputs and outputs are completely independent (no common clocks). When both INPUT READY and SHIFT IN are high, the four bits on D0-D3 are loaded into the first bit position where they stay until INPUT READY and SHIFT IN go low. This causes the bits to propagate to the second bit position (if empty) where they are propagated to the bottom of the silo by internal control signals.

When data has been transferred to the bottom of the memory, OUTPUT READY goes high indicating the presence of valid data. When both OUTPUT READY and SHIFT OUT are high, data is shifted out of the silo. This causes OUTPUT READY to go low. Data is maintained until both OUTPUT READY and SHIFT OUT are low. At this time, the bits in the adjacent upstream cell are transferred into the last cell causing OUTPUT READY to go high again. If the silo has been emptied, OUTPUT READY stays low.

LOGIC BLOCK DIAGRAM

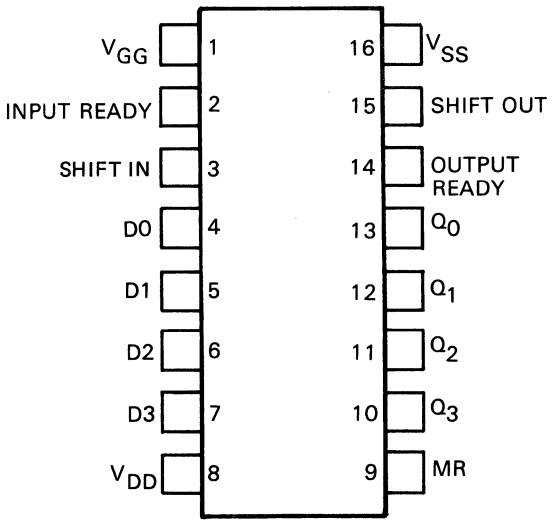


LOGIC SYMBOL



V_{SS} = PIN 16 +5V
V_{DD} = PIN 8 GND
V_{GG} = PIN 1 -12V

PIN COFIGURATION (TOP VIEW)

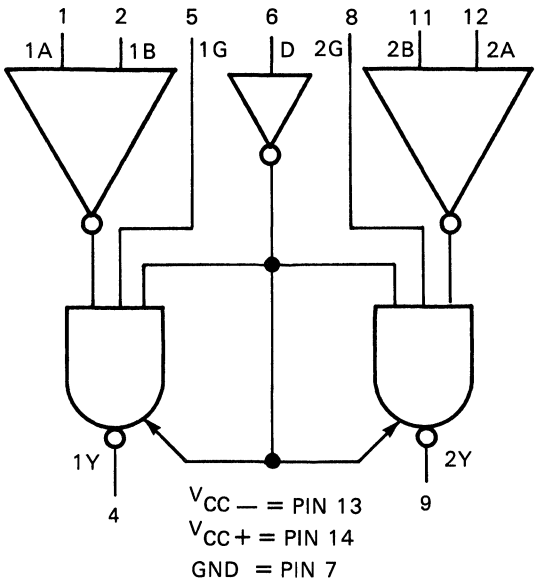


MK-0942

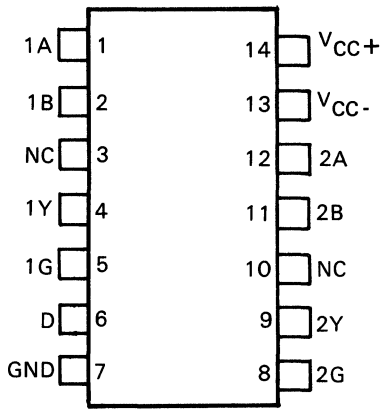
3603 - High Speed Dual Line Receivers

The 3603 line receivers are used to receive data in balanced, unbalanced or party-line transmission systems. The two receivers share the common voltage and ground busses and have a three-state output for bus organized systems.

LOGIC SYMBOL



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: PIN 1 IS MARKED FOR ORIENTATION.
NC = NO CONNECTION.

FUNCTION TABLE

DIFFERENTIAL INPUT VOLTAGE $V_{ID} = VA - VB$	INPUTS		OUTPUT
	GATE	DISABLE	
	G	D	Y
$V_{ID} > +25mV$	X	L	H
$-25mV < V_{ID} < +25mV$	H	L	?
$V_{ID} < -25mV$	H	L	L
X	L	L	H
X	X	H	Z

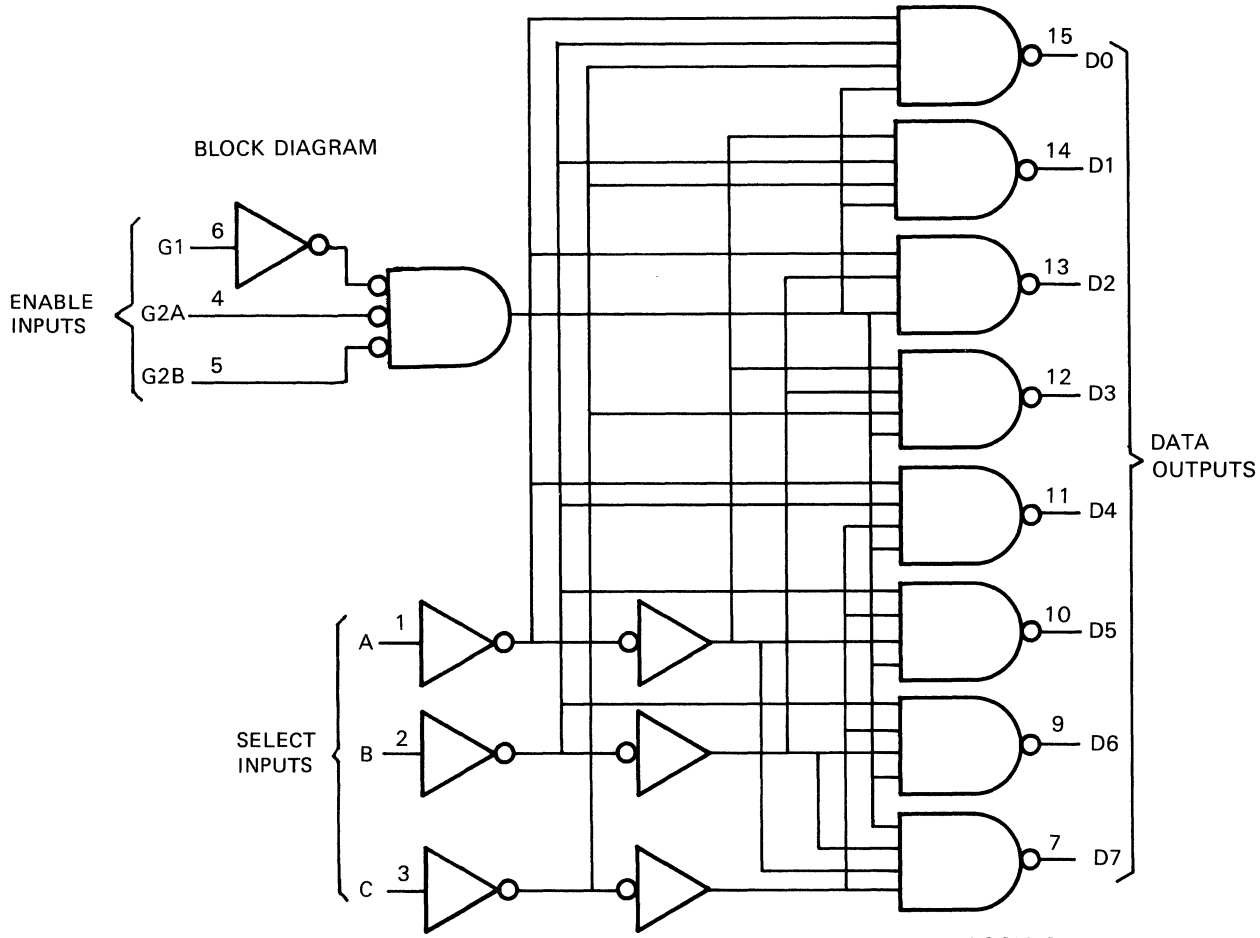
H = HIGH
L = LOW
X = DON'T CARE
? = DON'T KNOW
Z = HIGH-IMPEDANCE STATE

MK-0931

74S138 – Decoder Multiplexer

The 74S138 decodes one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expandng.

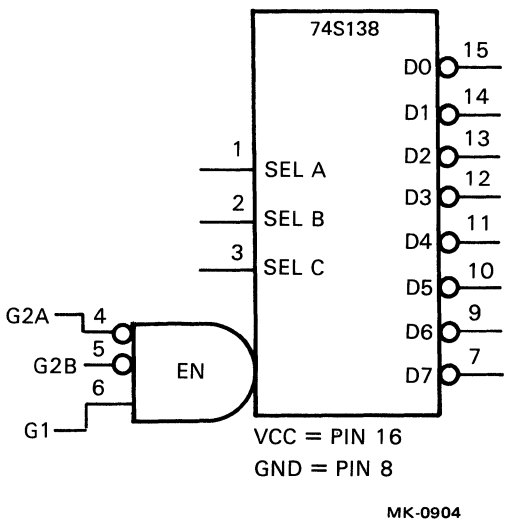
BLOCK DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
ENABLE	SELECT	
G1 G2	C B A	D0 D1 D2 D3 D4 D5 D6 D7
X H	X X X	H H H H H H H H
L X	X X X	H H H H H H H H
H L	L L L	L H H H H H H H
H L	L L H	H L H H H H H H
H L	L H L	H H L H H H H H
H L	L H H	H H H L H H H H
H L	H L L	H H H H L H H H
H L	H L H	H H H H H L H H
H L	H H L	H H H H H H L H
H L	H H H	H H H H H H H L

LOGIC SYMBOL



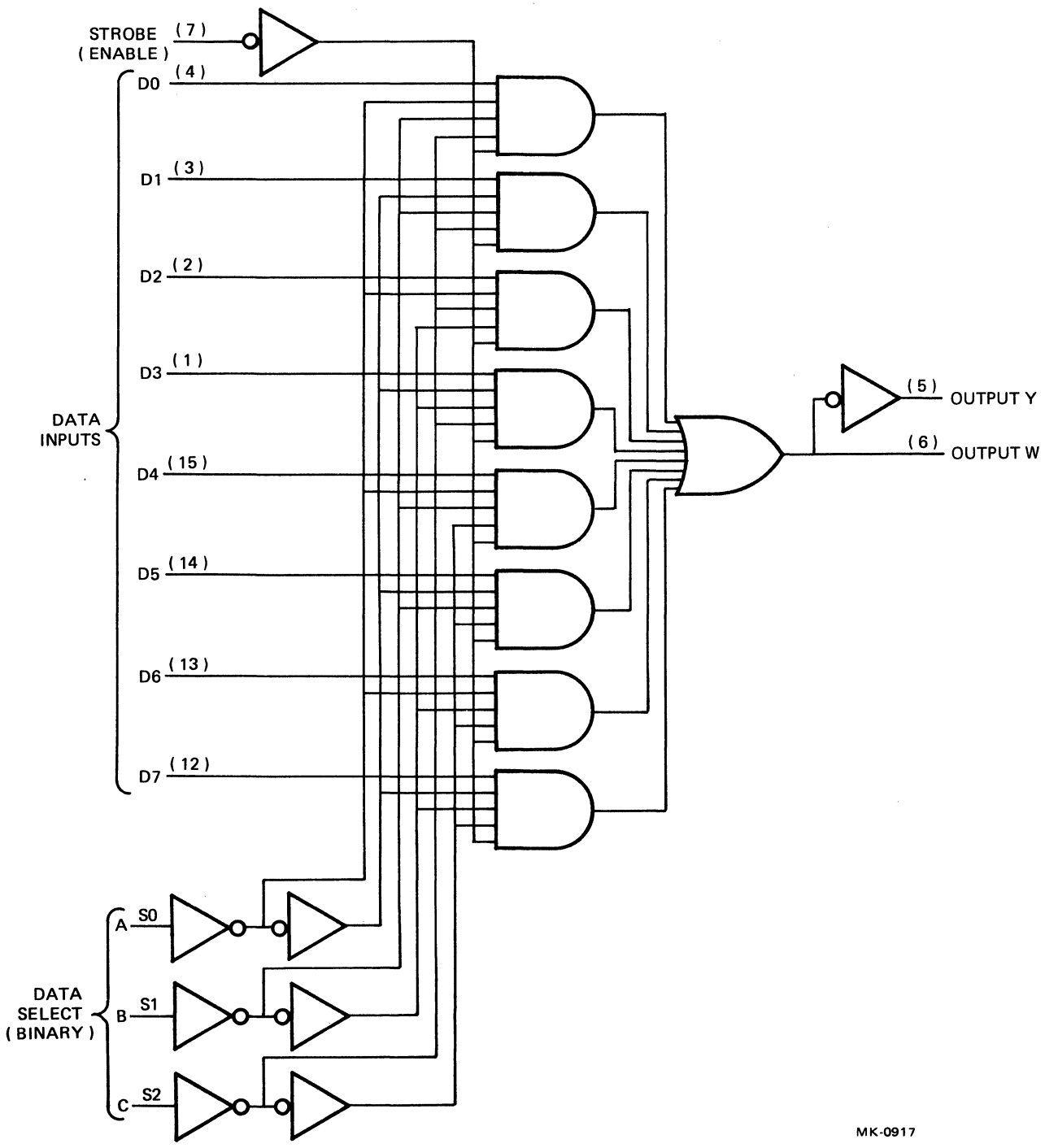
MK-0904

G2 = G2A+G2B

H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

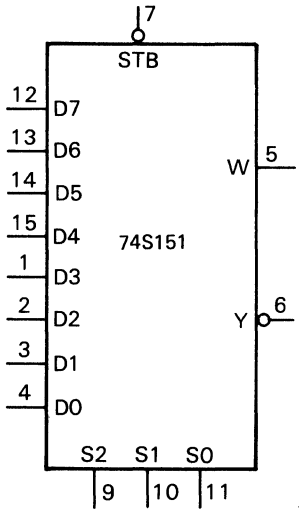
74S151 – Data Selector/Multiplexer

The 74S151 monolithic data selector/multiplexer contains full on-chip binary decoding to select the desired data source. The 74S151 selects one of eight data sources and has a strobe input which must be at a low logic level to enable the device. A high level at the strobe forces the W output high, and the Y output (as applicable) low.



74S151 — Data Selector/Multiplexer (Cont)

LOGIC SYMBOL



74S151 TRUTH TABLE

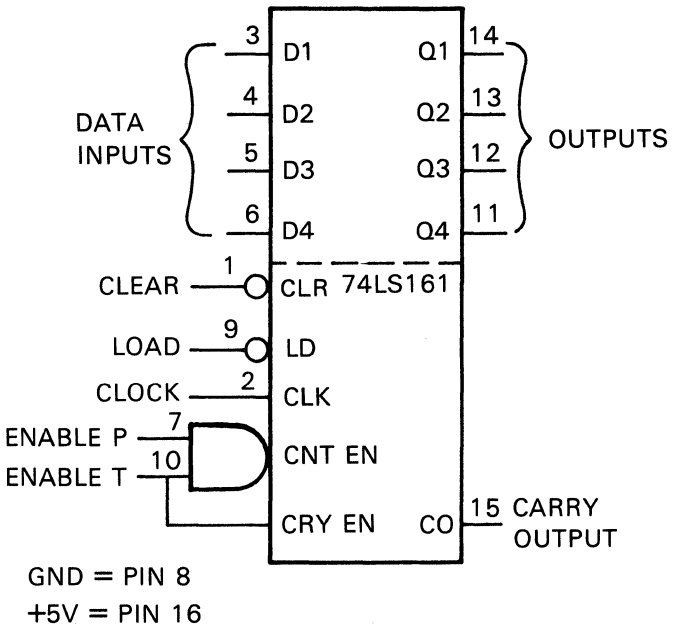
INPUTS												OUTPUTS	
S2	S1	S0	STB	D0	D1	D2	D3	D4	D5	D6	D7	W	Y
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

WHEN USED TO INDICATE AN INPUT X = IRRELEVANT.

MK-0918

74LS161 – Synchronous 4-Bit Counter

The 74LS161 is a synchronous, presettable binary counter which features an internal carry look-ahead for application in high-speed counting

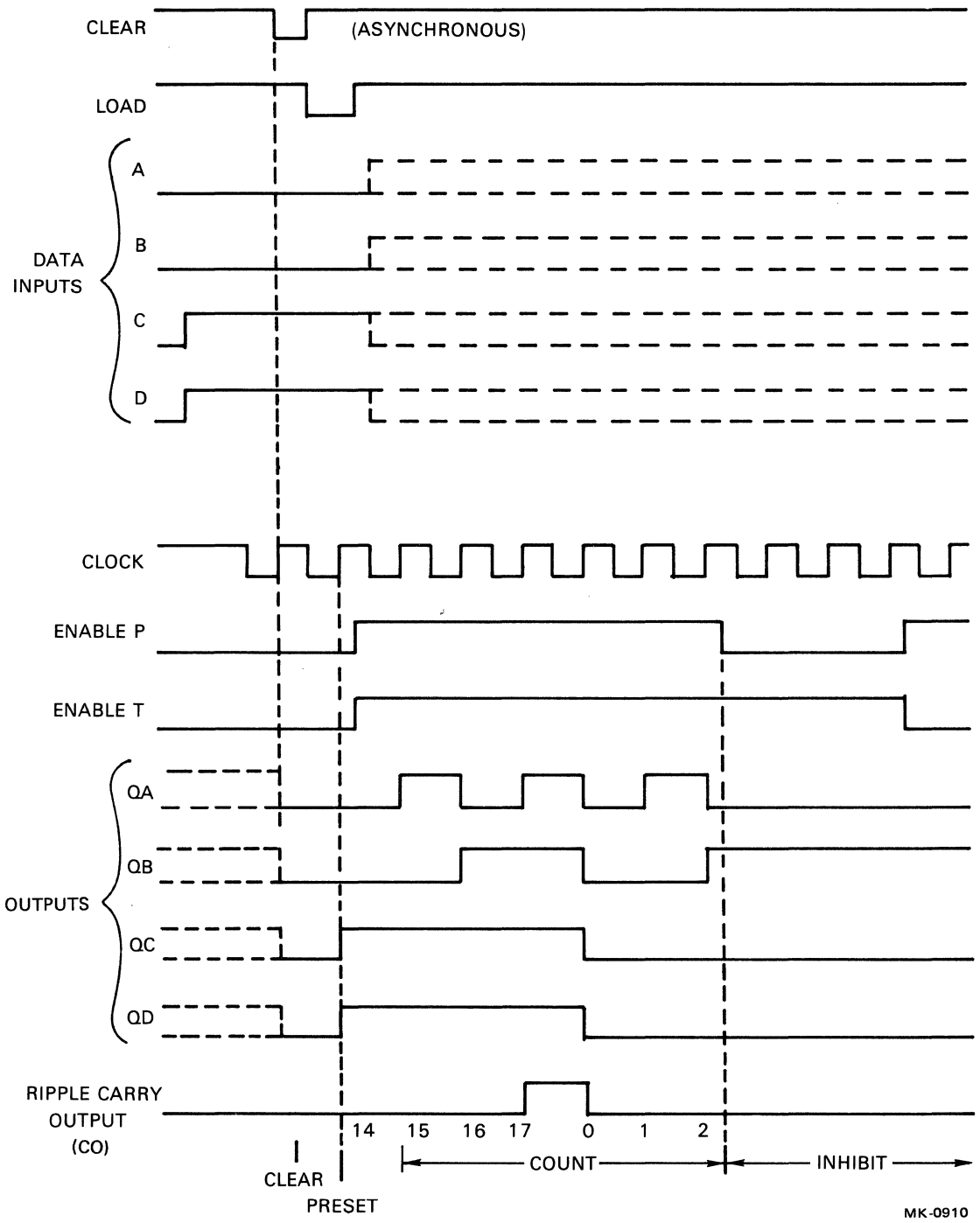


74LS161 — Synchronous 4-Bit Counter (Cont)

TYPICAL, CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCE:

ILLUSTRATED BELOW IS THE FOLLOWING SEQUENCE:

1. CLEAR OUTPUT TO 0.
2. PRESET TO BINARY 14.
3. COUNT TO 15,16, 17, 0, 1, AND 2.
4. INHIBIT

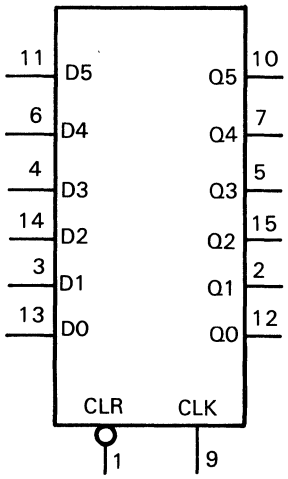


74S174 - Hex D-Type Flip-Flops with Clear

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the R outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

LOGIC SYMBOL

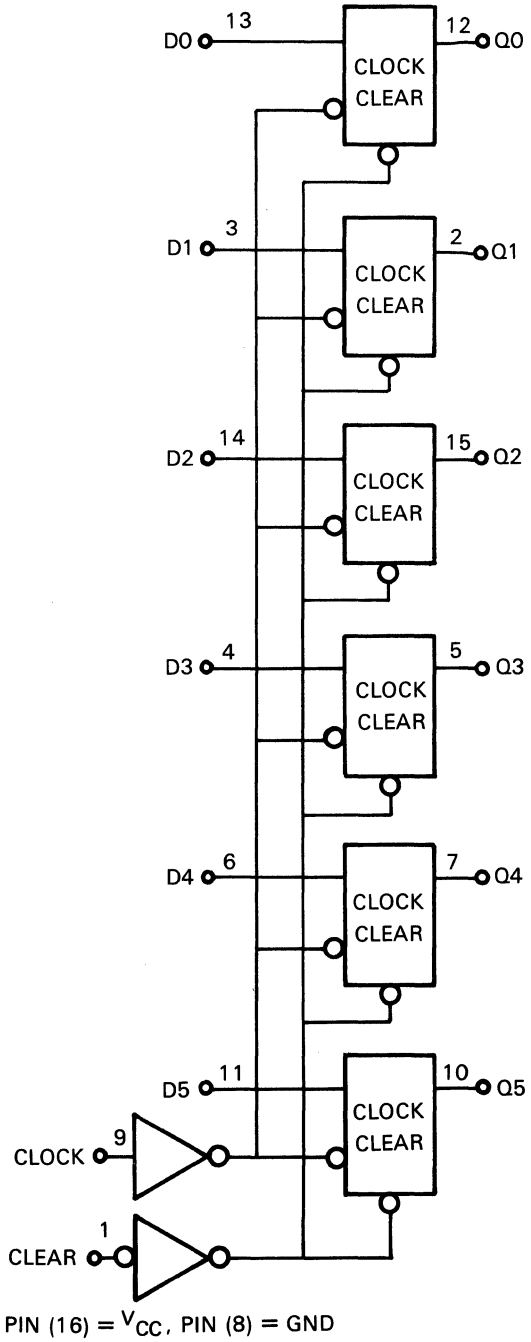


FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = HIGH LEVEL (STEADY STATE)
L = LOW LEVEL (STEADY STATE)
X = IRRELEVANT
↑ = TRANSITION FROM LOW TO HIGH LEVEL
Q_0 = THE LEVEL OF Q BEFORE THE INDICATED STEADY STATE INPUT CONDITIONS WERE ESTABLISHED.

BLOCK DIAGRAM

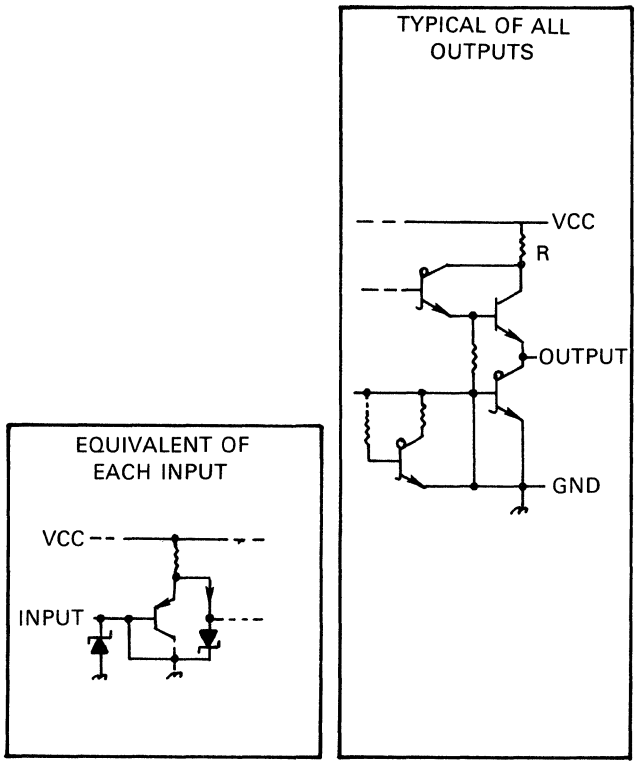


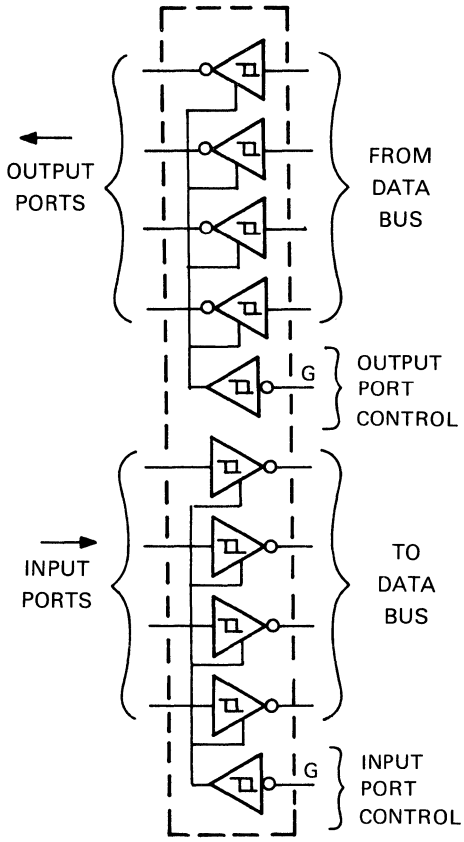
PIN (16) = V_{CC}, PIN (8) = GND

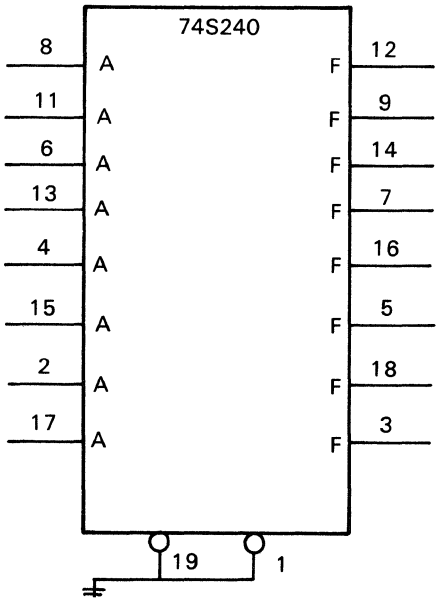
MK-0930

74S240 – Octal Inverter and Line Driver with 3-State Output

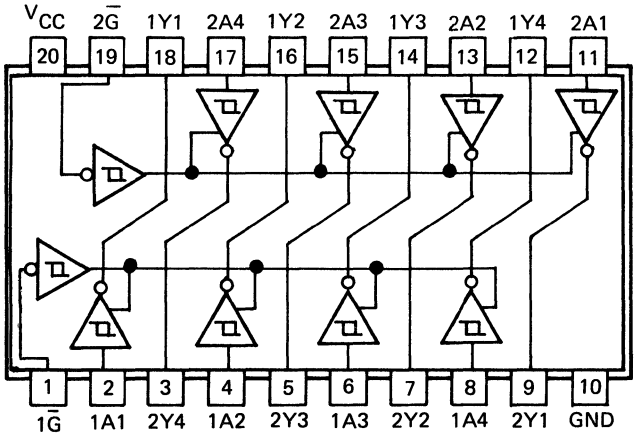
These octal inverters and line drivers provide inverting outputs, and G (active-low output control) inputs. G selects four inverting buffers.







(TOP VIEW)



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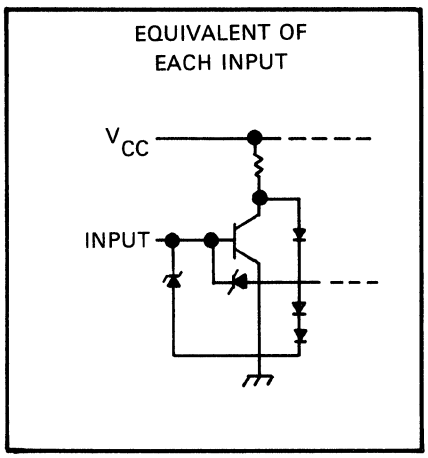
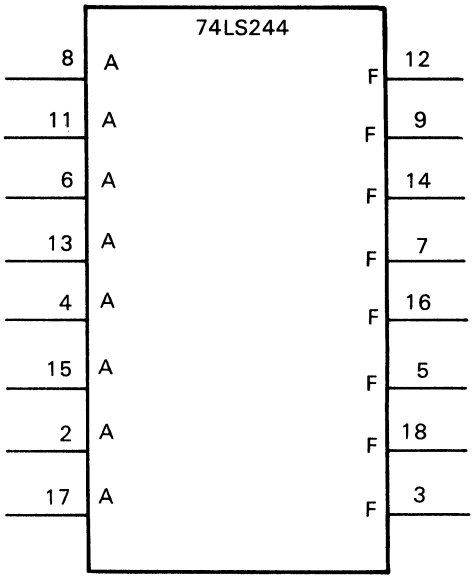
74LS244 – Octal Buffer and Line Driver with 3-State Output

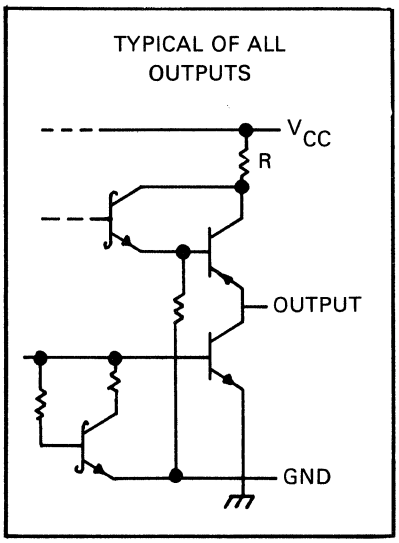
These octal buffers and line drivers provide selection of inverting and non-inverting outputs, symmetrical G (active-low output control) inputs and complementary G and G inputs.

SCHEMATIC OF INPUTS

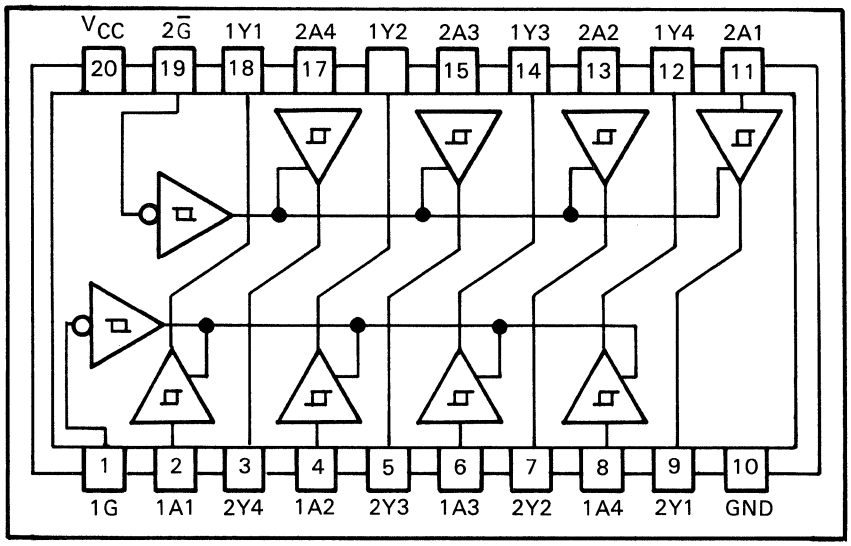




SCHEMATIC OF OUTPUTS



(TOP VIEW)



MK-0911

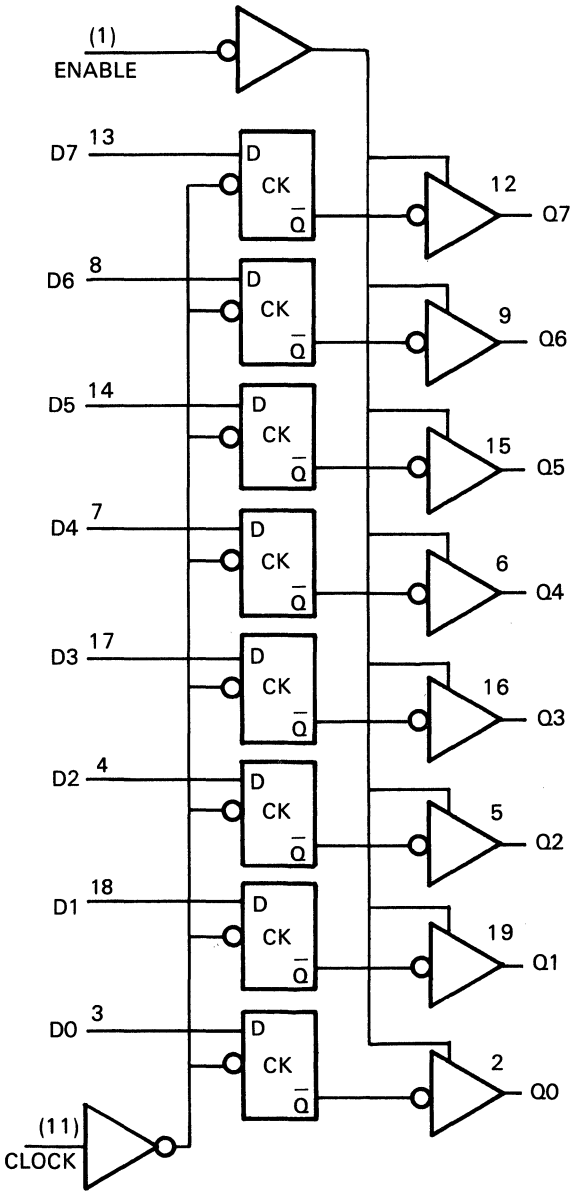
74LS374 - Octal D-Type Edge-Triggered Flip-Flops

The eight flip-flops of the 74LS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the R outputs will be set to the logic states that were setup at the D inputs.

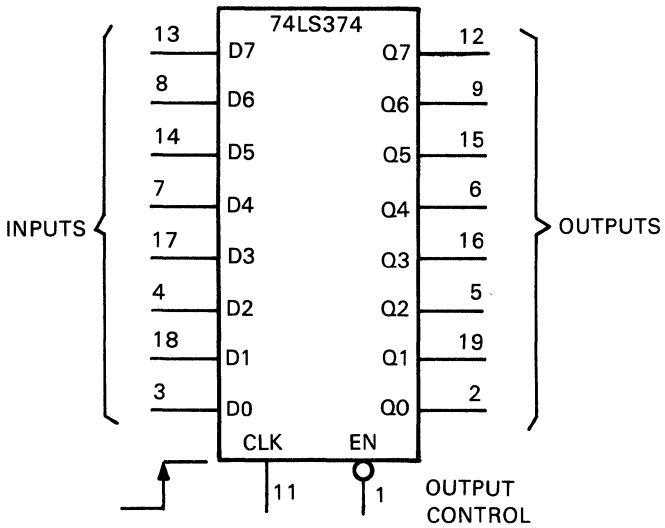
A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered while the outputs are off.

BLOCK DIAGRAM
POSITIVE-EDGE TRIGGERED FLIP-FLOPS



LOGIC SYMBOL



FUNCTION TABLE

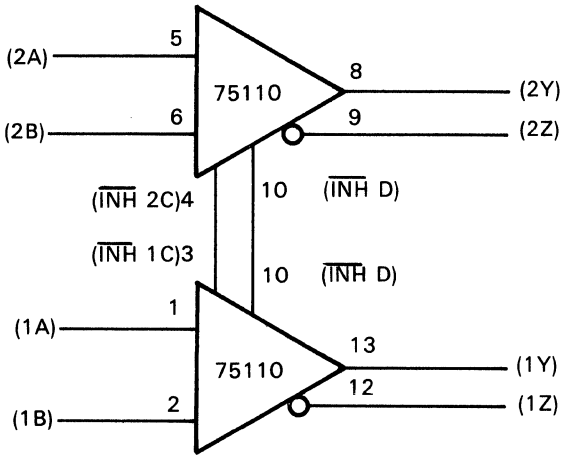
OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH LEVEL
L = LOW LEVEL
↑ = TRANSITION FROM LOW TO HIGH LEVEL
X = IRRELEVENT (ANY INPUT INCLUDING TRANSITIONS)
Z = OFF (HIGH IMPEDANCE) STATE OF A THREE-STATE OUTPUT
Q_0 = LEVEL OF R BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED

MK-0941

75110 – Dual Line Driver

The 75110 driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the inhibit inputs.



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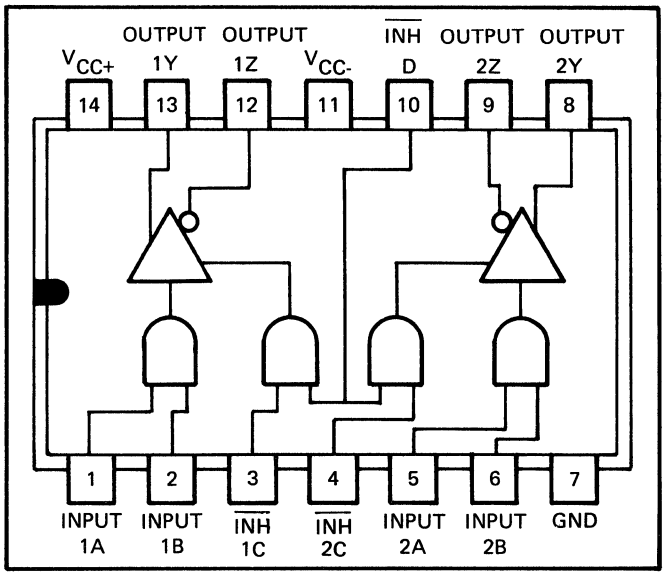


FUNCTION TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVENT

MK-0940

93S16 – BCD Decade/Four-Bit Binary Counter

The 93S16 is a fully synchronous 4-bit decimal and binary counter. With the parallel enable (LD) low, data on the inputs is parallel loaded on the positive clock transition. When LD is high and both count enables are also high, counting will occur on the low-to-high clock transition.

The terminal count state 1111 is decoded and ANDed with CRY EN in the terminal count (CO) output. If CRY EN is high and the counter is in its terminal count state, then CO is high.

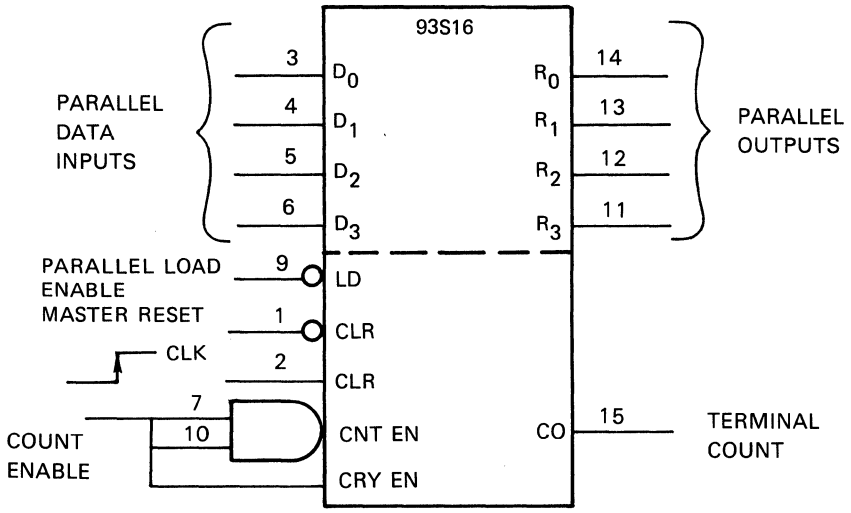
The counter has an asynchronous master reset (CLR). A low on the CLR input forces the outputs low independent of all other inputs. The only requirements on the LD, CNT EN, CRY EN, and D0-D3 inputs is that they meet the setup time requirements before the clock low-to-high transition.

FUNCTION TABLE

INPUTS									OUTPUTS			
CLK	CLR	LD	CNT EN 7	CNT EN 10	D_0	D_1	D_2	D_3	R_0	R_1	R_2	R_3
X	L	X	X	X	X	X	X	X	L	L	L	L
↑	H	L	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3
↑	H	H	L	L	X	X	X	X	NC	NC	NC	NC
↑	H	H	L	H	X	X	X	X	NC	NC	NC	NC
↑	H	H	H	L	X	X	X	X	NC	NC	NC	NC
↑	H	H	H	H	X	X	X	X	COUNT			

H = HIGH
L = LOW
X = DON'T CARE
NC = NO CHANGE
D_1 MAY BE EITHER HIGH OR LOW
↑ LOW-TO-HIGH TRANSITION

LOGIC SYMBOL



MK-0914

GLOSSARY

ABORT
In bit oriented protocol, a character with eight ones/non-valid character. It is usually used to terminate a message that cannot be completed with valid data, or transmitter shutdown after a valid flag has been sent for the end of the message.

AX
Address extended registers on the M8203.

BCC
Block check character, error checking, usually a cyclic redundancy check character (CRC) status bit.

BOP
Bit oriented protocol.

BPS
Bits per second.

CARR
Carrier, indication from the receiver that a signal is present.

CCP
Character oriented protocol.

CRC
Cyclic redundancy check character.

CS
Clear to send from the Integral Modem or Modem Interface, used for controlling the data flow on the start of the transmission. This is normally a reply to Request to Send being sent.

DISSI
Used on the M8203 to disable the silos to access the Universal Synchronous Receiver/Transmitter (USYRT) directly.

DMC
Data communications microcontroller option designation for the read only memory (ROM) controlled microprocessors and line units that are run by the microcontroller.

DTR
Electronic Industries Association (EIA) signal indicating that the data terminal is ready to accept data.

E BLK
Bit oriented protocol, indicates that the end flag is to be transmitted or the receiver has received a valid flag character to terminate the message.

ECS
Maintenance clock, 24 KHz on the M8203.

ENAX
Enable extended registers on the M8203.

EOM
End of Message flag.

GO AH
In bit oriented protocol, seven ones followed by a zero, used for stuffing or abutting messages.

HDX
Half-duplex, indicates transmission of data in one direction at a time.

IC
In Clear or receiver clear on the M8203.

ICIR
In Composite Ready, indicates that the Receiver Silo is ready to receive another character from the USYRT.

IDLE
A state when no valid data or flags are available to be sent. This is a character determined by the protocol being used and can be abort, go ahead, flag or sync characters.

IERROR
Maintenance function that allows ones to be inserted in the data that is looped back between the transmitter and receiver in the maintenance mode.

I RDI
In Ready indicates that a valid character is ready to be read from the receiver silo.

KMC
Random Access Memory (RAM) controlled microcontroller, K indicates the general use option.

LULP
Line unit loop, this is a maintenance function that loops back data internally in the USYRT.

O ACT
Out Active, this means the transmitter is in the process of transmitting data or control characters.

OC
Out Clear, this is used to clear the transmit section of the M8203.

OCOR
Out Composite Ready, this indicates that a valid character is ready to be loaded into the USYRT.

O RDO
Out Ready, this indicates that the Transmit Silo is ready to receive another character from the microprocessor.

POLL
This is a new signal under RS449 that is not defined, but is to be used to multidrop configurations for modem control.

R ACT
Receiver active, this indicates that the receiver is synced up and receiving characters.

RDAX
Read extended registers, this is used in the M8203 to start the read cycle of the extended registers.

READY
Ready indicates that the extended register function has been completed and data is ready or the out registers are ready to be loaded for the next transfer.

RING
Incoming Call, this is used by the Modem Interface to indicate that the modem has been called or dialed by another modem and start up will be coming.

RTS
Request to Send, this is used to start the transmitter section of the modem and indicates that the USYRT is ready to start transmitting as soon as Clear to Send is returned from the modem.

SEC A
Secondary address mode, this is used for multidrop environments in bit oriented protocol to select the receiver on the line.

SEL FR
Select frequency is used in the Modem Interface to select the data transmission speed.

SEL SBY
Select standby is used by the Modem Interface to put the modem in the standby mode.

SI
This is used in maintenance to monitor the data on a bit by bit shift of data out of the USYRT.

SIG Q
Signal Quality, this comes from the modem interface and is used to determine if the line quality is good for the data being received.

SIG R
Signal rate, this is an indication from the Modem Interface of the speed at which the modem is running.

SOM
Start of Message.

STBY
Standby, this indicates the modem is in the standby mode.

STRIP
Strip is used to strip sync or flag characters received.

SW
Switch.

TEST M
Test mode, this indicates that the modem is in the test mode.

WAX
Write to the extended registers on the M8203.

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EK-M8203-TM-002

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