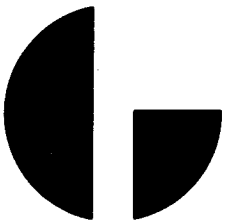

DATA GENERAL
CORPORATION
Southboro,
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HOW TO MAINTAIN

THE NOVA

PREFACE

This manual is intended to aid personnel in the maintenance of the Nova. Included are descriptions of the control logic for the teletype, reader and punch, but separate manufacturers' manuals are furnished for the devices themselves.

The first chapter presents a general description of the system and its operation. This includes a discussion of the physical and electrical characteristics of the computer, its logical organization, and the controls and indicators on the operator console. Chapter 2 presents a complete, detailed description of the system logic, including a discussion of the symbols and notation used in the logic drawings. Chapter 3 contains information useful in maintaining the system, including a discussion of maintainance programs, troubleshooting procedures, and instructions for removing, repairing and replacing both major and minor components.

Following Chapter 3 are lists of logic signals and components and an illustrated parts breakdown. Drawings referred to in the text are grouped at the back of the manual.

CONTENTS

Signal Reference, Teletype
Signal Reference, Paper Tape Reader
Signal Reference, Paper Tape Punch
Signal Reference, Real Time Clock
Signal Reference, Power Monitor

B Components

Chip Identification
Chip Identification - IO
Component Totals - IC
Component Totals - Resistors
Component Totals - Capacitors
Component Totals - Transistors
Component List - Power Supply, Console

ILLUSTRATED PARTS LIST

ENGINEERING DRAWINGS

C H A P T E R O N E

INTRODUCTION

In order to understand the material in this manual the reader should be familiar with the general characteristics of the Nova, the number and instruction formats it uses, and the instructions and various special operations it is capable of performing. All of this information is presented in Chapters 1 and 2 of the reference manual, How to Use the Nova and the Supernova, and is not duplicated here. For information on interfacing and installation refer to Appendices A and B of the reference manual.

PHYSICAL CHARACTERISTICS

In dimensions the table model differs from the rack model only in that it has a cabinet covering the basic chassis. The layout of the chassis is shown in installation drawing 000055. At the rear are the power supplies and sockets for connecting to external equipment. The central part of the chassis contains seven slots for 15x15-inch printed circuit boards or DGC subassembly frames. The slots are numbered from the bottom up, and boards are inserted and removed from the right side. Slots 1 and 2 are used for the central processor, the rest are for memories and IO interfaces. The general, CPU-1 contains the timing and control logic, CPU-2 contains the registers, gating, IO drivers, and skip logic. Since the computer usually includes a teletype and at least one memory, slot 3 usually contains the basic IO board, which has the teletype interface and can have interfaces for reader, punch and real time clock, and slot 4 usually contains a memory. The unit is cooled by two fans mounted at the rear. An expansion chassis with space for a power supply and seven more boards can be mounted above the unit.

The contact fingers on a board are inserted into sockets mounted on the back panel, which is at the left side of the chassis. All connections among the boards and from the boards to external connectors are made at this back panel, which is shown in detail in drawing 000024. The bottom two connectors are wired for the processor. The upper five connectors are identical and are wired to both the in-out and memory buses; blank spaces indicate pins available for connecting interfaces to external equipment.

The power supply for the teletype is mounted in its pedestal. Line power is usually supplied through the convenience outlet at the rear of the computer chassis. The reader and punch are contained in a single cabinet.

ELECTRICAL CHARACTERISTICS

The computer uses 47 to 63 Hz single phase line power, generally either 115±10% or 230±10% vac (other frequencies and voltages are available on special order). The power source should be capable of supplying 15 amperes. The power cable has a standard

OPERATION

The lights in the upper right on the generator console display control conditions, the rows of lights in the upper center display the processor registers. Below the latter is a register of toggle switches through which the operator can supply addresses and data to the processor (the up position of a switch represents a 1). The register can be used in conjunction with some of the operating switches, and its contents are read by the READS instruction.

In the row at the bottom of the panel are the operating switches. Each switch lever is actually two momentary-contact logical switches with a common off position in the center. Lifting the lever up turns on the switch whose name is printed above it; pressing it down turns on the switch whose name is written below.

At the upper left is a 3-position key-operated rotary switch that controls power and locks the console. Turning it to ON simply turns on power. Turning it to LOCK keeps power on and disables the operating switches so no one can interfere with the operation of the processor (the operator can still use the data switches to supply information to the program). Located at the back of the chassis are the power cord, fuse, circuit breaker, convenience outlet, and sockets for signal connections to external equipment.

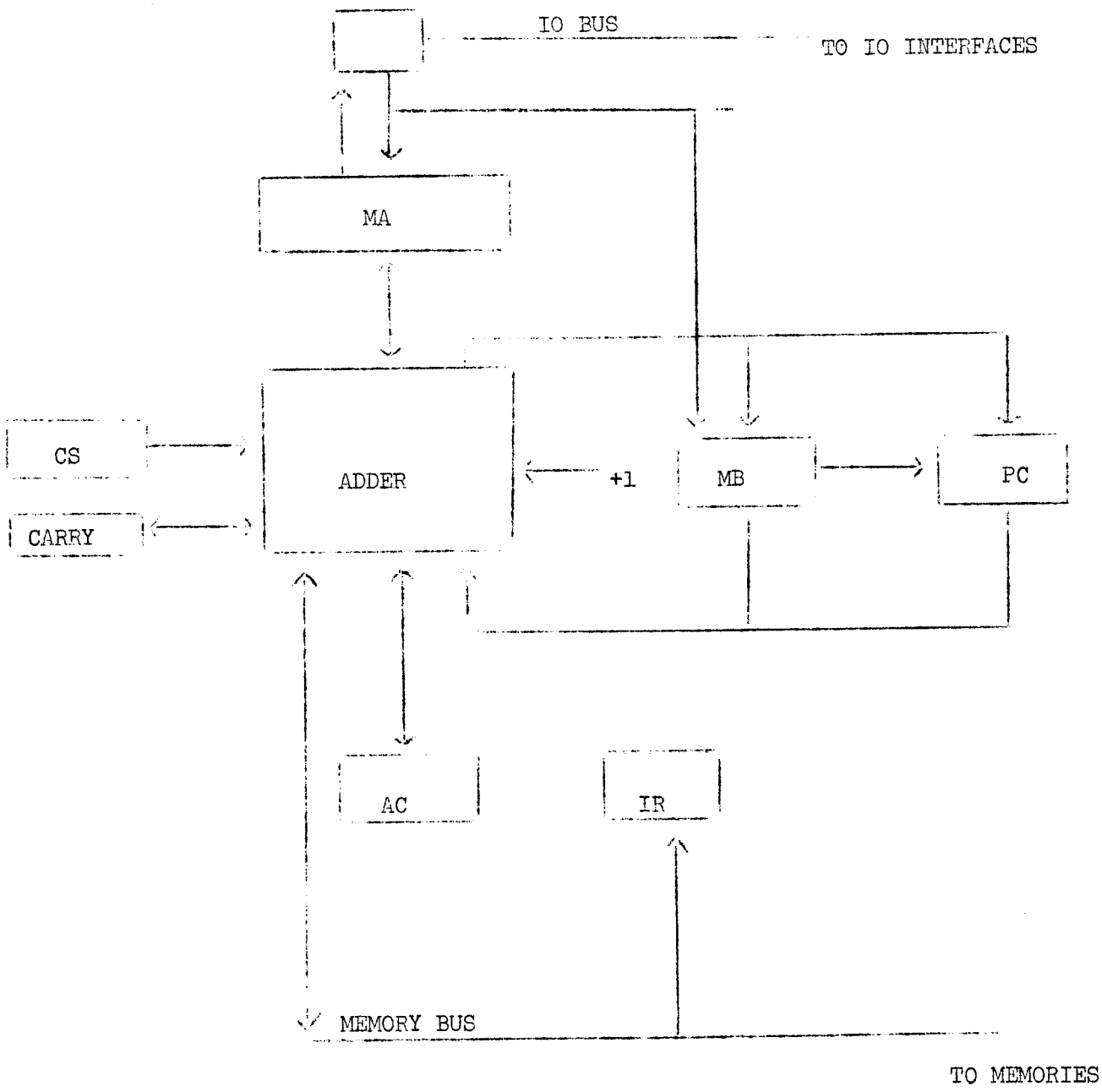
Indicators When any indicator is lit the associated flipflop is in the 1 state or the associated function is true. A few indicators display useful information while the processor is running, but most change too frequently and are therefore discussed in terms of the information they display when the processor has stopped.

The instruction lights display the left eight bits of the instruction being executed or just completed (these lights are all off if the processor stops following a program interrupt or data channel cycle). The address lights display the contents of PC, and the data lights display the contents of the Carry flag and the memory buffer.

Among the central indicators, RUN is lit while the processor is in normal operation with one instruction following another; when the light goes off, the computer stops. ION is the interrupt ON flag, which indicates that the interrupt is enabled. Of the remaining control lights, FETCH, DEFER, EXECUTE, DCH and PI, one and only one must be lit, and it indicates the major state the processor will enter next.

Operating Switches All of the switches in the bottom row except STOP and RESET are interlocked so that they have no effect if RUN is lit. The four pairs of switches at the left are for depositing data in the accumulators and examining their contents. Lifting a switch lever up loads the contents of the data switches into the specified accumulator; pressing it down displays the contents of the accumulator in the data lights. At completion FETCH is lit and the instruction lights are off.

The switches at the right perform the following functions when turned on.



PROCESSOR DATA FLOW

and in adding the complement, the adder input gating receives the compliment of MA. The AND function is produced by disabling one set of adder inputs and supplying two words through AND gates to the other set. The adder is also used for reading the console switches, incrementing PC, and transferring data between MB and the memory bus. The only transfers not made through the adder are from MB to PC, the loading of an instruction from the memory bus into IR, and transfers involving the in-out bus. All output to the IO bus is from MA, but input from the bus goes to MA only in programmed transfers and for a data channel address- data channel data input goes directly to MB.

All operations are performed by a sequence of processor cycles, each of which begins with a memory cycle. The processor cycles are of different types called major states: these are fetch, defer, execute, DCH and PI. In the fetch state the processor retrieves an instruction from memory. If the instruction is in the arithmetic and logical class or the in-out class, or is a JMP or JSR that uses direct addressing, the processor also executes it in the fetch cycle. If the instruction references memory and calls for indirect addressing, the processor enters the defer state to retrieve an address word; autoincrementing or autodecrementing, if required, are also performed in a defer cycle. Every level of indirect addressing requires another defer cycle, and an indirect JMP or JSR is executed in the final such cycle. After completing the effective address calculation, for any other memory reference instruction (whether defer cycles are required or not), the processor enters the execute state to process the operand. Upon completing an instruction, the processor returns to the fetch state unless there is a request for data channel access or a program interrupt. The data channel has priority, so if there are requests for access, the processor enters the DCH state for as many cycles as are necessary. It then returns to the fetch state unless there is an interrupt, in which case it first enters the PI state to store PC in location 0, and then the defer state to simulate a JMP @1 by retrieving an address from location 1.

Each processor cycle is divided into time states (TS); the number of time states in a given cycle depends upon the type of major state and the operation being performed. In every cycle the memory read operation takes place in TS0, the subsequent write operation occurs in the next time state, which may be either TS1 or TS4. The time states control the sequence of operations within the cycle; eg in an arithmetic instruction the source and destination accumulators are retrieved in TS1 and TS2, the result is loaded in TS3, and PC is incremented in TS4.

The only operations in which sixteen bits are processed in parallel are transfers to and from the IO bus. Al other transfers and all arithmetic and logical functions are performed in four steps, wherein the processor handles four bits at a time. A set of four states of the processor time generator (PTG) controls these steps.

3-wire plug and should be plugged into a receptacle rated at 15 amperes.

	Processor	Teletype
Line current (115 vac)	4 amperes	2 amperes
Dissipation	400 watts	Turnon surge, 7 amperes 92 watts

The logic voltage output of the power supply is +5 vdc; this output can deliver 12 amperes, of which about 5-1/2 are used by the processor with 4K of memory and a teletype interface; the rest is available for additional memories and IO interfaces. The low and high steady-state levels used in the logic are 0 and +3.5 vdc, with tolerances of 0 to .400 and 2.500 to 5). Levels on the IO bus are 0 and +2.7 vdc, with tolerances of 0 to .500 and 2.500 to 3.3. Although overshoots are common, any steady-state voltage outside of these ranges should be regarded as cause for concern.

The nominal drive voltages used in the memory are the following.

	Voltage	Current
X and Y windings	22 volts	350 ma
Inhibit windings	17.5 volts	640 ma

The voltages that actually occur in a given memory depend upon temperature and are controlled by thermistors in each memory. The voltages listed above are the power supply outputs and these are the true voltages at 25°C. Within a given memory the voltage vary by -.45% per degree centigrade.

The schematic of the power supply is drawing 000015. The unregulated +30 volts generated in the upper left is used only within the supply. The lower part of the drawing shows the generation of the regulated voltages for the logic, the memory, and a -5 volt output used only in the memory sense amplifiers. The circuits in the upper right generate signals to indicate that power has reached adequate levels at power turnon or that power is failing.

LOGICAL ORGANIZATION

The central register in the processor is MA, which does serve as the memory address register, but is also the accumulator or arithmetic register. The registers referred as accumulators in the reference manual are such only in programming sense; in terms of the hardware they are simply general purpose registers that supply data to MA and receive results from it. Arithmetic and logical operations are actually performed in an adder, which also serves as the connecting link for most data transfers. Thus in the ADD instruction the source AC is first transferred to MA through the adder, then the sum of MA and the destination AC is formed in the adder and loaded into MA. Finally, if the instruction calls for loading the result, it is sent (perhaps shifted or swapped) to the destination AC, again through the adder. A carry into the lease significant adder bit allows such functions as incrementing and subtraction; in the latter case

TABLE
SIGNAL REFERENCE
CENTRAL PROCESSOR (CPU)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
READ1	E8Ø	4(B72)	CPU1	Ø26-3
READ1*	E81	8	"	"
READ2	E8Ø	2(B7Ø)	"	"
RESET*	E12	11	CPU1	Ø26-1
RINHØ		B83	MEM	Ø14-3
RINH1		B77	"	
RINH2		B92	"	"
RINH3		B94	"	"
RINH4		A35	"	"
RINH5		A39	"	"
RINH6		A45	"	"
RINH7		A41	"	"
RINH8		A5	"	"
RINH9		A9	"	"
RINH1Ø		A15	"	"
RINH11		A11	"	"
RINH12		B7	"	"
RINH13		B9	"	"
RINH14		A51	"	"
RINH15		A53	"	"
RQENB	E3	12	IO	Ø1
RQENB*	E44	1Ø(B41)	CPU1	Ø26-3
RUN(1)	E1Ø	9(A77)	"	Ø26-1
RXR		B43	MEM	Ø14-1
RXS		B45	"	"
RYR		B42	"	"
RYS		B44	"	"
SARD1(Ø)	E43	9(B18)	"	"
SARD1(1)	E43	8	"	"
SARD2(Ø)	E43	5(B12)	"	"
SARD2(1)	E43	6	"	"
SARD3(Ø)	E43	3(B1Ø)	"	"
SARD3(1)	E43	4	"	"
SELECT	E43	2	"	"
SKIP	E41	6	CPU2	Ø27-4
SNSØ*	E23	2	MEM	Ø14-3
SNS1*	E23	4	"	"
SNS2*	E23	1Ø	"	"
SNS3*	E23	12	"	"
SNS4*	E6Ø	2	"	"
SNS5*	E6Ø	4	"	"

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
CENTRAL PROCESSOR (CPU)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
PCØ(1)	E13	15	CPU2	Ø27-1
PC1(1)	E12	15(B44)	"	"
PC2(1)	E11	15(B4Ø)	"	"
PC3(1)	E1Ø	15(B23)	"	"
PC4(1)	E13	14(B53)	"	"
PC5(1)	E12	14(B43)	"	"
PC6(1)	E11	14(B37)	"	"
PC7(1)	E1Ø	14(B27)	"	"
PC8(1)	E13	13(B54)	"	"
PC9(1)	E12	13(B46)	"	"
PC1Ø(1)	E11	13(B38)	"	"
PC11(1)	E1Ø	13(B25)	"	"
PC12(Ø)	E13	11	"	"
PC12(1)	E13	12(B68)	"	"
PC13(Ø)	E12	11	"	"
PC13(1)	E12	12(B47)	"	"
PC14(Ø)	E11	11	"	"
PC14(1)	E11	12(B39)	"	"
PC15(Ø)	E1Ø	11	"	"
PC15(1)	E1Ø	12(B24)	"	"
PC CLOCK	E18	6(B31)	CPU1	Ø26-2
PC ENABLE	E51	12(A87)	"	"
PC ENABLE*	E69	6	"	"
PC LOAD*	E73	11(B69)	"	Ø26-2
PI(1)	E5	6(A16)	"	Ø26-1
PI SET*	E37	6	"	"
PI TSØ*	E73	8	"	Ø26-2
PRESET*	E19	8	"	Ø26-1
PTGØ(Ø)	E92	4	CPU2	Ø27-2
PTGØ(1)	E31	6(B83)	CPU1	Ø26-1
PTG1(1)	E31	1Ø(B92)	"	"
PTG=Ø	E42	1Ø	CPU2	Ø27-3
PTG=Ø	E48	6(B44)	CPU1	Ø26-1
PTG=Ø*	E45	8(A35)	"	"
PTG=1	E92	1Ø(B91)	CPU2	Ø27-2
PTG=2	E92	12(B94)	"	"
PTG=3	E48	4(B23)	CPU1	Ø26-1
PTG=3*	E45	11(A91)	"	"
PUN ACK	E25	6	IO	Ø1
PWR CLR*	E41	2	CPU1	Ø26-1
RD ACK	E25	8	IO	Ø1

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
CENTRAL PROCESSOR (CPU)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
MB DECREMENT	E75	1Ø	CPU1	Ø26-2
MB ENABLE	E73	6(A67)	"	"
MB LOAD*	E71	6(B67)	"	"
MEMØ	E3	4(A29)	MEM	Ø14-1
MEM1	E3	1(A3Ø)	"	"
MEM2	E3	13(A31)	"	"
MEM3	E3	1Ø(A32)	"	"
MEM CLEAR	E8Ø	12(B16)	CPU1	Ø26-3
MEM CLOCK*	E48	8(B14)	"	Ø26-1
MEM ENABLE	E69	1Ø(A95)	"	Ø26-2
MFTSØ	E55	12	"	Ø26-1
MFTSØ*	E22	3	"	"
MODEØ	E13	12	"	Ø26-3
MODEØ*	E13	13(B17)	"	"
MODE1	E13	1Ø	"	"
MODE1*	E13	11(B21)	"	"
MSKO	E3	6	IO	Ø1
MSKO*	E51	1(A38)	CPU2	Ø27-4
MTGØ(Ø)	E8Ø	1Ø	CPU1	Ø26-3
MTGØ(1)	E64	15	"	"
MTG1(1)	E64	14	"	"
MTG2(1)	E64	13	"	"
MTG3(Ø)	E64	11	"	"
MTG3(1)	E64	12	"	"
MTG4(Ø)	E8Ø	6	"	"
MTG4(1)	E65	15	"	"
MTG5(1)	E65	14	"	"
MTG6(Ø)	E8Ø	8	"	"
MTG6(1)	E65	13	"	"
MTG7(Ø)	E65	11	"	"
MTG7(1)	E65	12	"	"
NEG EXTEND	E55	6	"	Ø26-2
NOSH + SWAP ENABLE	E43	6	CPU2	Ø26-2
NOSH + SWAP ENABLE*	E15	8(A12)	"	"
ONE ENABLE	E51	6(A37)	CPU1	Ø26-2
OUTPUT TIME	E5	8(A9)	"	Ø26-3
OVFLO	E29	1(B39)	"	"

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
CENTRAL PROCESSOR (CPU)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
MA12(1)	E38	12	CPU2	Ø27-1
MA13(Ø)	E37	11	"	"
MA13(1)	E37	12	"	"
MA14(Ø)	E36	11	"	"
MA14(1)	E36	12	"	"
MA15(Ø)	E35	11	"	"
MA15(1)	E35	12	"	"
MAA ENABLE	E52	8(A89)	CPU1	Ø26-2
MAB ENABLE	E5Ø	3(A85)	"	"
MA CLEAR*	E22	6(B19)	"	"
MA CLOCK	E18	8(B77)	"	"
MA ENABLE	E5Ø	6(A83)	"	"
MAL ENABLE	E55	1Ø	CPU2	Ø27-2
MANUAL DEPOSIT*	E72	6	CPU1	Ø26-2
MANUAL FUNCTION	E25	12	"	Ø26-1
MANUAL FUNCTION*	E4Ø	3	"	"
MAR ENABLE	E55	12	CPU2	Ø27-2
MAR ENABLE*	E54	11	"	"
MBØ(1)	E25	15(B71)	CPU2	Ø27-1
MB1(1)	E24	15(B52)	"	"
MB2(1)	E23	15(B41)	"	"
MB3(1)	E22	15(B36)	"	"
MB4(1)	E25	14(B7Ø)	"	"
MB5(1)	E24	14(B49)	"	"
MB6(1)	E23	14(B42)	"	"
MB7(1)	E22	14(B33)	"	"
MB8(1)	E25	13(B51)	"	"
MB9(1)	E24	13(B5Ø)	"	"
MB1Ø(1)	E23	13(A41)	"	"
MB11(Ø)	E15	12	"	"
MB11(1)	E22	13(B34)	"	"
MB12(Ø)	E25	11(B48)	"	"
MB12(1)	E25	12(B15)	"	"
MB13(Ø)	E24	11	"	"
MB13(1)	E24	12(B17)	"	"
MB14(Ø)	E23	11	"	"
MB14(1)	E23	12(B35)	"	"
MB15(Ø)	E22	11	"	"
MB15(1)	E22	12(B21)	"	"
MB CLOCK	E19	6(B45)	CPU1	Ø26-2
MB COUNT	E74	8	"	"

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
CENTRAL PROCESSOR (CPU)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
IRØ(1)	E84	15	CPU2	Ø27-1
IR1(1)	E84	14(A57)	"	"
IR2(1)	E84	13(A59)	"	"
IR3(Ø)	E84	11	"	"
IR3(1)	E84	12(A61)	"	"
IR4(1)	E83	15(A53)	"	"
IR5(1)	E83	14(A51)	"	"
IR6(1)	E83	13(A49)	"	"
IR7(Ø)	E83	11	"	"
IR7(1)	E83	12(A47)	"	"
IR8(1)	E68	9(A84)	"	"
IR CLEAR*	E75	8(A55)	CPU1	Ø26-2
IR CLOCK	E34	1Ø(A63)	"	"
IR CLOCK*	E34	9	"	"
ISZ	E14	6	"	Ø26-1
ISZ*	E85	11	CPU2	Ø27-1
JSR	E14	1Ø	CPU1	Ø26-1
JSR*	E85	12	CPU2	Ø27-1
JSR.F	E41	4	CPU1	Ø26-2
KEY DEPOSIT	E9	6	"	Ø26-1
KEY NEXT	E9	3	"	"
KEY SYNC(1)	E26	9	"	"
LDA	E14	12	"	"
LDA*	E86	12	CPU2	Ø27-1
MAØ(1)	E38	15	"	"
MA1(1)	E37	15	"	"
MA2(1)	E36	15	"	"
MA3(1)	E35	15	"	"
MA4(1)	E38	14	"	"
MA5(1)	E37	14	"	"
MA6(1)	E36	14	"	"
MA7(1)	E35	14	"	"
MA8(1)	E38	13	"	"
MA9(1)	E37	13	"	"
MA1Ø(1)	E36	13	"	"
MA11(1)	E35	13	"	"
MA12(Ø)	E38	11	"	"

*INDICATES "NOT"

C H A P T E R O N E

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SIGNAL REFERENCE
CENTRAL PROCESSOR (CPU)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
INH15	E1	9	MEM	Ø14-1
INHIBIT	E78	12(B8)	CPU1	Ø26-3
INTA	E51	4(A4Ø)	CPU2	Ø27-4
INTA*	E65	12	"	"
INT ACK	E3	1Ø	IO	Ø1
INT ENABLE	E78	4	CPU1	Ø26-3
INTP OUT*	E26	4	IO	Ø1
INT REQ	E59	6	CPU1	Ø26-3
IO	E92	8	CPU2	Ø27-1
IO*	E86	1Ø	CPU2	Ø27-1
IO CLEAR*	E54	4	"	Ø27-2
IO DATAØ	E5Ø	2	"	Ø27-4
IO DATA1	E49	1Ø	"	"
IO DATA2	E49	6	"	"
IO DATA3	E48	6	"	"
IO DATA4	E5Ø	8	"	"
IO DATA5	E49	12	"	"
IO DATA6	E49	4	"	"
IO DATA7	E48	12	"	"
IO DATA8	E5Ø	1Ø	"	"
IO DATA9	E5Ø	6	"	"
IO DATA1Ø	E49	2	"	"
IO DATA11	E48	1Ø	"	"
IO DATA12	E5Ø	12	"	"
IO DATA13	E5Ø	4	"	"
IO DATA14	E49	8	"	"
IO DATA15	E48	8	"	"
IO INPUT	E66	6(A13)	CPU2	Ø27-1
ION	E79	6(A25)	"	Ø27-4
IO OUTPUT	E66	8(A9Ø)	"	Ø27-1
IOPLS	E14	13(A74)	"	Ø27-4
IO PULSE*	E54	5	"	Ø27-2
IO RESET	E6	1Ø	IO	Ø1
IO RESET*	E6	8	"	"
IORST	E14	1(A7Ø)	CPU2	Ø27-4
IO SKIP	E92	6	"	"
IO SKIP*	E82	5	"	Ø27-1
IO START*	E54	3	"	Ø27-2

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
CENTRAL PROCESSOR (CPU)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
D SET*	E36	12	CPU1	Ø26-1
DSZ	E14	4	"	"
DSZ*	E85	1Ø	CPU2	Ø27-1
DTIA*	E82	12	"	"
DTIB	E52	12	CPU2	Ø27-4
DTIB*	E82	1Ø	CPU2	Ø27-1
DTIC	E52	4	CPU2	Ø27-4
DTIC*	E82	3	CPU2	Ø27-1
DTOA*	E82	11	"	"
DTOB	E52	6	CPU2	Ø27-4
DTOB*	E82	9	CPU2	Ø27-1
DTOC	E52	2	CPU2	Ø27-4
DTOC*	E82	4	CPU2	Ø27-1
EFA	E75	6(A43)	CPU1	Ø26-2
EFA*	E58	6	"	"
E SET*	E38	6	"	Ø26-1
EXECUTE(1)	E6	8(A78)	"	"
FETCH(1)	E7	8(A45)	CPU1	Ø26-1
F SET	E36	2	"	"
F SET ENABLE	E36	1Ø	"	"
IN	E75	2	CPU1	Ø26-2
IN*	E74	3	"	"
INHØ	E31	5	MEM	Ø14-1
INH1	E31	9	"	"
INH2	E33	5	"	"
INH3	E33	9	"	"
INH4	E64	5	"	"
INH5	E64	9	"	"
INH6	E63	5	"	"
INH7	E63	9	"	"
INH8	E32	5	"	"
INH9	E32	9	"	"
INH1Ø	E29	5	"	"
INH11	E29	9	"	"
INH12	E2	5	"	"
INH13	E2	9	"	"
INH14	E1	5	"	"

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
CENTRAL PROCESSOR (CPU)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
DATA12	E7	1Ø	IO	Ø1
DATA12*	E26	1Ø	IO	Ø1
DATA12*	E63	1(B59)	CPU2	Ø27-4
DATA13	E7	12	IO	Ø1
DATA13*	E26	13	IO	Ø1
DATA13*	E62	1(B64)	CPU2	Ø27-4
DATA14	E6	12	IO	Ø1
DATA14*	E61	1(B56)	CPU2	Ø27-4
DATA15	E6	2	IO	Ø1
DATA15*	E6Ø	1(B66)	CPU2	Ø27-4
DATA IN A	E4	6	IO	Ø1
DATA OUT A	E5	4	IO	Ø1
DATA OUTPUT*	E61	6(B81)	CPU1	Ø26-3
DATIA	E39	1(A44)	CPU2	Ø27-4
DATIA*	E4Ø	11(A88)	CPU2	Ø27-4
DATIB	E39	13(A42)	CPU2	Ø27-4
DATIC	E26	13(A54)	"	"
DATOA	E39	4(A58)	"	"
DATOB	E39	1Ø(A56)	"	"
DATOC	E26	1Ø(A48)	"	"
DCH(1)	E6	6(A17)	CPU1	Ø26-1
DCHA*	E29	13(A6Ø)	CPU1	Ø26-3
DCHI	E29	1Ø(B37)	"	"
DCHO	E29	4(B33)	"	"
DCH REQ	E13	6	"	"
DCH SET	E36	8	CPU1	Ø26-1
DCH SET*	E37	8	"	"
DEFER(1)	E7	6(A41)	CPU1	Ø26-1
DP + EX + EXN + DPN	E8	8	"	"
OP + EX + EXN + DPN*	E24	4	"	"
DSØ*	E14	1Ø(A72)	CPU2	Ø27-4
DS1*	E14	4(A68)	"	"
DS2*	E1	13(A66)	"	"
DS3	E4	1Ø	IO	Ø1
DS3*	E1	1Ø(A46)	CPU2	Ø27-4
DS4	E5	12	IO	Ø1
DS4*	E1	4(A62)	CPU2	Ø27-4
DS5	E6	6	IO	Ø1
DS5*	E1	1(A64)	CPU2	Ø27-4

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
CENTRAL PROCESSOR (CPU)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
BMA5(Ø)	E77	12(B24)	CPU2	Ø27-2
BMA6(Ø)	E77	8(B26)	CPU2	Ø27-2
BTSG3(Ø)	E69	8	CPU1	Ø26-1
CARRY(1)	E3Ø	9(A34)	CPU2	Ø27-1
CARRY SAVE	E3Ø	6(A79)	CPU2	Ø27-1
CLEAR	E4	2	IO	Ø1
CLK ACK	E25	1Ø	IO	Ø1
CLOCK ENABLE	E79	6	CPU1	Ø26-1
CLOCK1Ø MHZ	E6Ø	6	CPU1	Ø26-1
CLOCK RESET*	E15	1Ø	CPU1	Ø26-1
CLR	E26	4(A5Ø)	CPU2	Ø27-4
COMMON SELECT	E3	2	IO	Ø
CONT + ISTP + MSTP*	E24	2	CPU1	Ø26-1
CPU CLOCK(1)	E15	6(A34)	CPU1	Ø26-1
CPU INST	E15	4(A11)	CPU2	Ø27-4
CPU INST*	E2	8	"	"
CRY	E28	6	"	Ø27-3
CSØ	E4	8	CONSOLE	Ø8
CS1	E4	6	"	"
CS2	E8	8	"	"
CS3	E8	6	"	"
CS ENABLE	E72	12(A73)	CPU1	Ø26-2
DATAØ*	E63	1Ø(B62)	CPU2	Ø27-4
DATA1*	E62	1Ø(B65)	"	"
DATA2*	E61	1Ø(B82)	"	"
DATA3*	E6Ø	1Ø(B73)	"	"
DATA4*	E63	13(B61)	"	"
DATA5*	E62	13(B57)	"	"
DATA6*	E61	13(B95)	"	"
DATA7*	E6Ø	13(B55)	"	"
DATA8	E7	2	IO	Ø1
DATA8*	E63	4(B6Ø)	CPU2	Ø27-4
DATA9	E7	4	IO	Ø1
DATA9*	E62	4(B63)	CPU2	Ø27-4
DATA1Ø	E7	6	IO	Ø1
DATA1Ø*	E26	1	IO	Ø1
DATA1Ø*	E61	4(B75)	CPU2	Ø27-4
DATA11	E7	8	IO	Ø1
DATA11*	E6Ø	4(B58)	CPU2	Ø27-4

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
CENTRAL PROCESSOR (CPU)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
ACØ (1)	E72	11	CPU2	Ø27-2
AC1 (1)	E72	11	CPU2	Ø27-2
AC2 (1)	E74	11	CPU2	Ø27-2
AC3 (1)	E75	11	CPU2	Ø27-2
ACC ENABLE*	E44	4(A94)	CPU1	Ø26-2
ACDØ*	E85	9	CPU2	Ø27-1
ACD1*	"	3	"	"
ACD2*	"	4	"	"
ACD3*	"	5	"	"
ACD ENABLE*	E54	12(A14)	CPU1	Ø26-2
ACDP	E24	1Ø	"	Ø26-1
ACDP + ACEX	E9	8	"	"
ACDP + ACEX*	E24	6	"	"
AC ENABLE	E71	8	"	Ø26-2
ACEX	E24	12	"	Ø26-1
AC LOAD	E32	8	CPU1	Ø26-1
AC READ*	E56	8	CPU1	Ø26-2
ACSØ*	E86	9	CPU2	Ø27-1
ACS1*	"	3	"	"
ACS2*	"	4	"	"
ACS3*	"	5	"	"
ACS ENABLE*	E53	11(A86)	CPU1	Ø26-2
AC WRITE ENABLE	E74	11	"	"
ADDRESS ENABLE*	E78	2(B71)	"	Ø26-3
ALC	E15	1Ø(A76)	CPU2	Ø27-1
ALC*	E81	12(A15)	"	"
ALC2	E69	4(A39)	CPU1	Ø26-2
ALC2*	E5Ø	11	"	"
ALC + IO	E54	8	CPU1	Ø26-1
ALC + IO*	E55	4	"	"
AND ENABLE	E69	12(A81)	"	Ø26-2
AND ENABLE*	E7Ø	8	"	"
BDS3*	E4	4	IO	Ø1
BDS4*	E5	2	"	"
BDS5*	E6	4	"	"
BMA1(Ø)	E77	2(B18)	CPU2	Ø27-2
BMA2(Ø)	E77	4(B12)	"	"
BMA3(Ø)	E77	6(B1Ø)	"	"
BMA4(Ø)	E77	1Ø(B28)	"	"

*INDICATES "NOT"

IN-OUT BUS SIGNAL CONNECTIONS

H	High	B	Bidirectional	P	From device to processor
L	Low	D	From processor to device		

Signal	Level	Direction	Panel Pin	External Bus Pin	Signal	Level	Direction	Panel Pin	External Bus Pin
CLR	H	D	A50	2	DCHM0	L	P	B17	27
DATA0	L	B	B62	3	DCHM1	L	P	B21	28
DATA1	L	B	B65	4	DCHO	H	D	B33	29
DATA2	L	B	B82	5	DCHP IN	L	D*	A94	30
DATA3	L	B	B73	6	DCHP OUT	L	D*	A93	
DATA4	L	B	B61	7	DCHR	L	P	B35	31
DATA5	L	B	B57	8	DS0	L	D	A72	32
DATA6	L	B	B95	9	DS1	L	D	A68	33
DATA7	L	B	B55	10	DS2	L	D	A66	34
DATA8	L	B	B60	11	DS3	L	D	A46	35
DATA9	L	B	B53	12	DS4	L	D	A62	36
DATA10	L	B	B75	13	DS5	L	D	A64	37
DATA11	L	B	B58	14	INTA	H	D	A40	38
DATA12	L	B	B59	15	INTP IN	L	D*	A95	39
DATA13	L	B	B64	16	INTP OUT	L	D*	A95	
DATA14	L	B	B56	17	INTR	L	P	B29	40
DATA15	L	B	B66	18	IOPLS	H	D	A74	41
DATIA	H	D	A44	19	IORST	H	D	A70	42
DATIB	H	D	A42	20	MSKO	L	D	A38	43
DATIC	H	D	A54	21	OVFLO	H	D	B39	44
DATOA	H	D	A58	22	RQSNB	L	D	B41	45
DATOB	H	D	A56	23	SELB	L	P	A82	46
DATOC	H	D	A48	24	SELD	L	P	A80	47
DCFA	L	D	A60	25	STRT	H	D	A52	48
DCHI	H	D	B37	26	Power on	+5	D		49

*For the two pairs of priority-determining signals, the in signal comes from the processor or the preceding device, the out signal goes to the next device. If the computer is operated with an interface board removed (or a slot is not used), jumper pin A93 to A94 and A95 to A96 to maintain bus continuity.

Pins 1 and 50 of the external bus are grounded, and the ground wires from all twisted pairs are connected to them. The power-on line cannot be used to supply power to any external device; it is available only for picking up relays for remote power turnon.

APPENDIX A

High Speed Punch - Technical Manual
High Speed Tape Punch Set
(BRPE)
Bulletin 215B

High Speed Tape Punch Set
(BRPE)
Parts
Bulletin 1154B

High Speed Reader - (Digitronics Model (2540EP)

Perforated Tape Reader
Operation and Maintenance
Manual

Lubrication Requirements

Teletype - Keyboard KS7470 (oil)
KS7471 (grease)

Typing unit KS7470 (oil)
KS7471 (grease)

Reader KS7470 (oil)
KS7471 (grease)
Lupriplate 105

High Speed Punch (BRPE11)
KS7470 (oil)
145867 (grease)

High Speed Reader SAELO (oil)

Reccommended spares - one each

High Speed Reader - Lamp incandescent
Digitronics TLNBF009
GE (08305) (P/N1638)

High Speed Punch - Drivebelt #135097

Read/Write and Inhibit currents are measured with a current probe attached to the appropriate drive current test loop adjustment procedure:

1. Machine running, executing a JMP to itself instruction.

2. Current probe attached on Read X or Y drive current test loop, located on the lower left hand corner of the memory board.

3. Adjust trimpot(VMEM) for a nominal value of 350 MA.

4. Repeat for Inhibit, with current probe on any one of 16 Inhibit current test loops adjusting trimpot. (VINH)

Nominal Values - READ/WRITE and INHIBIT

READ 1	1.2 us	350 ma
READ 2	1.1 us	350 ma
STROBE	100 ns	
INHIBIT	.5 us	640 ma
WRITE	.4 us	350 ma

Various figures in the appendix illustrate the current probe in use, identify various test points on the memory board and adjustments in the power supply. Memory waveforms and timing are also illustrated.

3.10.6 IO - Maintenance other than lubrication, minor adjustments and part changes should be performed by DGC personell or respective manufacturer representatives. Lubrication should be performed in accordance with the appropriate manual listed below:

Applicable Manuals

Teletype - Technical Manual
33 Teletype writer sets
Bulletin 310B Volume I

Technical Manual
33 Teletype writer sets
Bulletin 310B Volume II

33 Page Printer set
ASR, KSR and RO
Parts
Bulletin 1184B

7. General - Both sides of the line are fused with a 10A little fuse (Buss type). A circuit breaker is located on the rear of the computer and is a physical part of the power supply.

3.10.5 MEMORY

Address decoding and data word transfer failures are the types of memory malfunctions most frequently encountered. The inability to store or fetch a word from or into a selected core location is usually an indication of the former while storing or fetching a word which is modified by one or two bits is an indication of the latter.

Address test and checkerboard are memory diagnostics designed to verify memory reliability. The two programs will detect and, in most cases, identify the cause of a malfunction. Address test is primarily intended to test address selection logic and verifies the ability to address all core locations. Checkerboard is a worst case noise test designed to detect the picking up or dropping of bits in a data word transfer.

In the case of intermittent failures it may be desirable to revert to console troubleshooting, utilizing short closed loop routines which are toggeled in. Programs such as the one illustrated below are valuable in the resolving of failures.

SAMPLE DIAGNOSTIC LOOP

1. Deposit data word in AC2
2. Deposit program in core
3. Start - Program halts - Load address in console switches and continue

```
LOC
0000    063077      DOC Ø, CPU      :Halt Inst.
0001    060477      DIA 1, CPU      :Reads Switches
0002    044011      STA 1, 11       :Store Addr
0003    052011      STA 2, @11      :Data to Addr
0004    000001      JMP. -3         :Loop
```

Note: The address can be varied by changing the contents of console switches.

The above routine will store the contents of AC2 (DATA word) into the address in AC1. It is useful in monitoring Read/Write currents and individual Inhibit currents.

Two 2K trimpots, located on the circuit board in the power supply provide for the adjustment of Read/Write and Inhibit currents. The trimpot governing Read/Write current varies the value of +VMEM, that governing Inhibit current varies +VINH. The nominal value of +VMEM is 22 volts, while that of +VINH is 17.5 volts.

Signal Reference, Teletype
Signal Reference, Paper Tape Reader
Signal Reference, Paper Tape Punch
Signal Reference, Real Time Clock
Signal Reference, Power Monitor

B Components

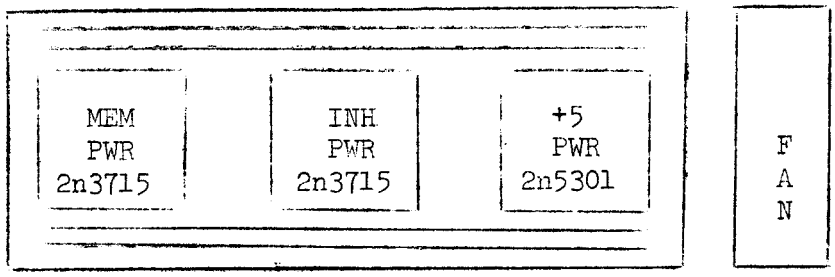
Chip Identification
Chip Identification - IO
Component Totals - IC
Component Totals - Resistors
Component Totals - Capacitors
Component Totals - Transistors
Component List - Power Supply, Console

ILLUSTRATED PARTS LIST

ENGINEERING DRAWINGS

4. Power Transistors - MEM, INH and +5 power transistors are located on the underside of the heat sink. To replace, remove 4 Philips head screws holding the heat sink in place. The -5 power transistor (2N3715) is located in a heat sink on the Power Supply Circuit Board.

INHIBIT CAPACITOR



HEAT SINK
TOP VIEW

POWER SUPPLY PLUGS

P1

1	2	3
+50K	GND	-5
POW-ER FAIL	MEM OK	-5

P2

1	2	3	4	5	6	7	8	9	10
T2	T2	GND				GND			
11 SUP. -5	12	13	14 THERM + MEM	15 +3Ø	16 BASE MEM	17 THERM - MEM	18	19 +V MEM	20 +V EMIT. MEM
O			Y	BU	WT	B		Y	W

P3

1	2	3	4	5	6	7	8	9	10
BASE +5									THERM INH
11	12 OUT PUT +5	13 GND	14 COLL. +5	15	16 BASE INH	17	18 THERM INH	19 GND	20 VINH +
	R	BK	BU		GN		GN	BK	GN

3.10.4 POWER SUPPLY

One compact power supply of advanced design supplies all the power requirements of the NOVA. Voltages for CPU logic and memory are regulated. Two 2K trimpots associated with memory voltages are the only adjustment provided.

1. Table of outputs

VL	Nonregulated - console lamps
+VMEM	Regulated (E7) Memory READ/WRITE CURRENTS
+VINH	Regulated (E5) Memory Inhibit current
-5V	Regulated (#8)
+5V	Regulated (E6)
+50K	
PWR FAIL	
MEM OK	

2. Resistant readings - all readings taken with a Simpson model 260 or equivalent (RX1-scale)

READING	OHM/S
AC line to AC line	Inf
AC line to chassis	Inf
AC gnd to chassis	0
+5 to chassis Forward	>50
+5 to chassis Reverse	5-15
+5 gnd to chassis	0
VMEM to chassis Forward	Inf
VMEM to chassis Reverse	>50
VINH to chassis Forward	>50
VINH to chassis Reverse	5-15
VINH to gnd to chassis	0
VL to chassis Forward	Inf
VL to chassis Reverse	50
VL gnd to chassis	0
-5 to chassis Forward	>50
-5 to chassis Reverse	>50

3. Output Voltage Readings - Taken with a Simpson Model 260 or equivalent. (Oscilloscope may be used).

CHECK	READING
VL	13-15VDC
VINH	17.5VDC (Adj by 2K Trimpot)
VMEM	22VDC (Adj by 2K Trimpot)
+5VDC	+5VDC + .4 -.3
-5VDC	-5VDC - .3 +.3
+5 OK	7-8VDC
PWR FAIL	3-4VDC
MEM OK	3-4VDC

TABLE 3-4
BACK PANEL TO CONSOLE
PLUG AND CONNECTOR CONFIGURATION

P3

10	BLK PC7	B/BLK PC11
	W PC15	BLK/W PC3
	R MB11	R/W PTG=3
	G MB7	G/W MB15
	O MB14	B/W MB13
	B MB3	BLK/R MB12
	W/BLK IR4	W/R CS3
	R/BLK IR1	O/R CS2
	G/BLK IR2	B/R CS1
1	O/BLK IR3	R/G CSØ

P4

10	BLK GND	B/BLK +5V
	$\overline{\text{W}}$ $\overline{\text{ACC2}}$	$\overline{\text{BLK/W}}$ $\overline{\text{RSTRT.ENB}}$
	$\overline{\text{R}}$ $\overline{\text{ACCØ}}$	$\overline{\text{R/W}}$ $\overline{\text{RST}}$
	$\overline{\text{O}}$ $\overline{\text{ACC1}}$	$\overline{\text{O/W}}$ $\overline{\text{ACC.ENB}}$
	$\overline{\text{O}}$ $\overline{\text{ACC3}}$	$\overline{\text{B/W}}$ $\overline{\text{ACDP}}$
	$\overline{\text{B}}$ $\overline{\text{EX}}$	$\overline{\text{BLK/R}}$ $\overline{\text{MSTP}}$
	$\overline{\text{W/BLK}}$ $\overline{\text{DP}}$	$\overline{\text{W/R}}$ $\overline{\text{STOP}}$
	$\overline{\text{R/BLK}}$ $\overline{\text{DPN}}$	$\overline{\text{O/R}}$ $\overline{\text{ST}}$
	$\overline{\text{G/BLK}}$ $\overline{\text{EXN}}$	$\overline{\text{B/R}}$ $\overline{\text{ACEX}}$
1	$\overline{\text{O/BLK}}$ $\overline{\text{ISTP}}$	$\overline{\text{R/G}}$ $\overline{\text{CONT}}$

TABLE 3-4
BACK PANEL TO CONSOLE
PLUG AND CONNECTOR CONFIGURATION

P1

10	BLK MBØ	B/BLK PC12
	W MB4	BLK/W MB9
	R PTG=Ø	R/W MB1
	G PTG=2	G/W PC8
	O +5V	B/W +5V
	B PI (1)	BLK/R RUN (1)
	W/BLK DCH	W/R ALC
	R/BLK ION	O/R IR7
	G/BLK Ov1	B/R FETCH
1	O/BLK MB1Ø	R/G DEFER

P2

10	BLK MB6	B/BLK PC4
	W PC1	BLK/W MB8
	R PC9	R/W MB5
	G PC5	G/W PC13
	O GND	B/W GND
	B PTG=1	BLK/R MB2
	W/BLK +5V	W/R PC2
	R/BLK EXECUTE	O/R PC14
	G/BLK IR6	B/R PC1Ø
1	O/BLK IR5	R/G PC6

3.10.2 COMPONENT REPLACEMENT

The replacement of a component requires care to prevent damage to circuit board etch. Clipping a component from the circuit board rather than unsoldering is the preferred method. Excessive heat from a soldering iron may result in damage to the component being replaced. The use of a soldering iron with an isolation transformer, a small copper alligator clip as a heat sink and a delay between the soldering of individual pins of a chip are recommended. With the extender board in use the weight of the board under test should be supported by a non-conductive material. Various figures in the appendix illustrate the extender board, IC test clip and current probe in use. Replacing a console switch or Indicator requires the removal of the console subassembly. The following is the procedure to be followed when replacing a console (Data) switch:

1. Remove the four Allen head screws attaching the console subassembly to the main frame.

2. Remove four Phillip head screws holding the circuit board assembly to the console casting.

3. Remove the power switch and individual knurled nuts from each of the data switches. Seperate the dead front from the circuit board.

4. Replace the defective switch and reassemble in reverse order.

To replace a console indicator follow steps 1-3 above and in addition remove two slotted flathead screws holding the Bendolex to the circuit board. Replace and reassemble in reverse order.

3.10.3 BACK PANEL TO CONSOLE CONNECTORS

Table 3-4 illustrates pin configuration for the four cables connecting the back panel and console.

3.9 PREVENTIVE MAINTENANCE

The key to reducing costly downtime and perhaps costly repairs is a preventive maintenance program which is faithfully adhered to. By following a regularly scheduled preventive maintenance program, unnecessary wear and tear on IO devices can be alleviated. In addition a certain percentage of malfunctions can be detected while in the process of occurring. Diagnostic routines should play a major role in preventive maintenance programs. Suggested items that should be included are as follows:

1. Diagnostics - Run exerciser daily for a reliability check of the entire system. Instruction timer should be run daily and a record of readings kept. A gradual daily change in recorded times is an indication of an incipient malfunction. All ofther diagnostics should be run at least once weekly.

2. IO devices - Clean daily, removing the dust that normally accumulates as the device is used. Check for excessive vibration, overheating of bearings, and signs of excessive mechanical play or wear. Check punch and teletype belts for wear and fraying. Empty the punch chad box and remove chad from within the device itself. Clean the type face of the teletype. Look for and remove excess oil and grease from within the devices.

3. General - Check all power and IO cables for fraying or wear. Check all plugs and connectors; tighten if necessary. Check the cooling fans on either end of the computer power supply removing lint and dust as necessary.

4. Lubrication - Faithfully following the lubrication schedules as set forth in the IO device pamphlets is perhaps the most important phase of a preventive maintenance program.

3.10 MAINTENANCE

A malfunction usually comes to light as the result of a diagnostic failing or the inability of a user to perform a certain task. Malfunctions are generally of two types, the solid failure which is normally easy to resolve and the intermittent failure which usually requires a more sophisticated approach. In either case, the three most important tools of trouble shooting are the diagnostic program, the simple diagnostic routine toggeled in at the console and a calm, logical approach to the problem.

3.10.1 GENERAL

Maintaining and troubleshooting the NOVA beyond isolating to the board stage requires the use of an extender board, IC test clip, oscilloscope and perhaps a multimeter or current probe. The use of diagnostic routines is dependent upon the ability to load the program into core. Failure to read in a program is in itself a clue to the malfunction and usually means resorting to consele switches as a means of trouble shooting.

TABLE 3-3
NOVA DRAWING LIST

DWG	SHEET	BOARD	TITLE
000026	1	CPU1	Timing, major states, manual functions
	2		Register control
	3		Memory control and I0
00027	1	CPU2	Major register and instruction decoding
	2		Accumulators and MA decoding
	3		Register gating
	4		I0 devices and interrupt control
000014	1	MEMORY	4K memory buffer and flippers
	2		4K memory XY drive
	3		4K memory sense and inhibit
000016	1	MEMORY	2K memory buffer and flippers
	2		2K memory XY drive
	3		2K memory sense and inhibit
000001		I0	I0 bus RCVRS and common sel
000003		I0	Real time clock
000004		I0	Paper tape reader control 4011
000005		I0	Paper tape punch control 4011
000011		CPU1	Power monitor
000025		I0	Teletype control
000008			Console
000015			Nova power supply
000017			Flow diagram
000018			Timing diagram
000024			Back panel
000055			Nova installation

Locating the malfunction is then the next logical step. The following is a suggested plan for effective casualty analysis:

1. Investigation - record the state of the machine on error occurence. Look for obvious symtoms including operator error, loose plugs or connectors, blown fuses or tripped circuit breaker.

2. Isolation - through the use of diagnostic programs or console trouble shooting techniques attempt to isolate the malfunction to a particular board.

3. Component Isolation - Isolate the faulty component using an oscilloscope and short diagnostic loops either toggled in at the console or as part of a diagnostic. Selecting the correct external synch is of importance at this point.

4. Replace the faulty component and retest by running the diagnostic that originally failed.

5. Record for future reference, the symptoms, cause, unique trouble shooting method/s used to isolate the malfunction.

3.8 NOVA ENGINEERING DRAWINGS

Table 3-3 lists the engineering drawings necessary for the effective maintenance of a basic NOVA system and standard IO. A complete set of these drawings is supplied with the NOVA. On occassion, it may be necessary to refer to individual IC schematics. These can normally be found in the manufacturer's IC catalog. Table A in the Appendix references alphabetically logic signals by board, chip, pin and drawing. Table B in the appendix lists individual chip types per board.

3.6 DIAGNOSTIC PROGRAMS

Are individual programs which together test all facets of a NOVA system. Individually the programs test various logic areas of the computer and IO. The majority of NOVA's diagnostic routines are capable of diagnosing malfunctions down to the Logic Level. The diagnostics provide a means of measuring the performance of the system. Copies of diagnostic tapes as well as individual program documentation are part of the software package delivered with the NOVA. Individual program documentation provides information as to operating procedures, error interpretation, console switch settings and logical areas tested. Certain diagnostics are normally part of the daily and weekly preventive maintenance routines.

NOVA DIAGNOSTIC PROGRAMS

PROGRAM	DESCRIPTION
Address Test	Routine to test the memory address selection logic.
Checkerboard II	Worst case memory noise test.
Logic Test	Gate by gate test of CPU Logic (less IO)
Instruction Timer	Routine to test CPU clock logic, prints instruction times of basic NOVA instruction set.
Exerciser	Reliability test - tests CPU logic, TTY Reader, punch, high speed paper tape reader, paper tape punch and real time clock. Halts on error.
Teletype Test II	Routine to test TTY logic, PI system and IO Bus logic.
Reader, Punch Test	Routine to test high speed paper tape reader and punch.
Real Time Clock Test	Routine to test Real Time Clock logic.
Power Shut Down Test	Test retention of memory data on power loss. Tests power monitor auto restart option.

3.7 TROUBLE SHOOTING PHILOSOPHY

Effective trouble shooting is accomplished in a minimum of time by following a series of logical steps. The ultimate aim is to effectively pinpoint the actual problem using all information available.

TRANSFORMERS

XFMR (Balcn)	DGC 104-000009	2
XFMR 3:1	DGC 104-000010	2
XFMR 1:1	DGC 1Ø4-000011	1

CONTENTS

TABLE 3-1

RECOMMENDED COMPONENT SPARES

IC's

5033	1	9005	2
7474	3	9006	1
7483	1	9007	1
7525	1	9008	3
8H90	1	9009	1
8T80	2	9016	6
8T90	1	9022	1
8280	1	9300	3
8281	1	9301	2
8880	1	9601	1
8881	3	SG83	1
9002	5	SH6405	2
9003	2	BC728	2
9004	2	MICRO 723	1
		NE51ØA	1

CAPACITORS

6000 MFD 1ØV	1
.05 MFD 50V	2
6.8 MFD 35V	2

RESISTORS

17.5 OHM 1% (DALE SPR-275)	2
15Ø OHM 1%	2

TRANSISTORS

2N4123	2
2N4125	2
2N3715	1
2N3724	3
2N4918	1
2N5301	1

DIODE

CD-8434	1Ø

BULB

28V (Hudson 2187D)	5

SWITCH

ON/OFF (C and K 7101-PC)	2
ON/OFF (C and K 7105-PC)	2
DPTT (C and K 7205-PC)	1

is also located on this board. The CPU2 board contains all of the major Registers, the logic for Register and Instruction decoding, AC and MA decoding, register gating, IO and PI control. The IO board of a basic system includes IO common select and teletype control logic. Interface logic for the high speed paper tape reader and punch as well as logic for the real time clock option are included on the IO board. Sense, inhibit, XY drive logic and the memory make up the memory board.

3.4 IC COMPLEMENT

The NOVA for its power and capabilities has a surprisingly small complement of IC's. This was a design criteria. To minimize the types of IC's used while providing for a second source as replacement was the design objective. All IC's were chosen on the basis of quality of design, performance and reliability. The following includes the basic NOVA as well as standard IO.

NOVA IC COMPLEMENT

FAIRCHILD	SIGNETICS	TEXAS INSTRUMENT
5033*	----	----
9002	8889	----
9003	8879	----
9004	8819	----
9005	8840	----
9006	----	----
9007	----	----
9008	8848	----
9009	8859	74H40
9016	8H90	----
9022	----	----
9300	----	----
9301	----	----
9308	----	----
9601	----	----
----	8T80	----
----	8T90	----
----	8280	----
----	8281	----
----	8828	7474
----	8880	----
----	8881	7401N
----	----	7483
----	----	7525
SH6405	----	----
MICRO 723	----	----
----	NE510A	----
FA3470	----	BC728

* Equivalent-Transitron
TMC 3164E

3.5 RECOMMENDED COMPONENT SPARES

The number of spare components to be maintained for efficient maintenance of NOVA with a minimum of down time depends on the individual user. Tables of this sort are normally compiled on the basis of number of components and failure rate if known versus number of hours of system usage. The following table which includes at least one spare IC for each IC in the complement is to be regarded as a minimum number of spares for effective maintenance of the CPU/and memory. Table 3-2 lists the quantities of individual circuit components for the basic NOVA and standard IO.

Slots 5-6-7 are available for additional memories, IO or DGC sub-assembly boards. The Bus connector (referred to as the back panel) occupies the left side of the unit with the console sub-assembly making up the front. Connectors for an extended IO Bus and IO devices are located at the rear of the unit. One power receptacle for remote turn on of an IO device is also included here. Reset for the circuit breaker located in the power supply is also located at the rear of the unit.

The teletype is mounted on a pedestal which contains a power supply for the unit. Line power for the teletype is normally obtained from the power receptacle at the rear of the computer. The High Speed Reader and Punch are usually mounted together in one common cabinet.

Only eight bolts are needed to mount the rack model with its draw slides (the unit is shipped with the movable parts of the slides attached). The chassis (without console) is 20 1/4 inches deep, but 2 inches should ordinarily be left open at the back of the rack for cabling. The console protrudes 1 3/4 inches at the front of the rack, and the entire unit slides out 22 inches. An expansion chassis with the same dimensions can be mounted above the unit.

	Height (inches)	Width (inches)	Depth (inches)	Weight (pounds)
Table model	6 3/4	22 1/2	24 1/2	80
Rack model	5 1/4	19	20 1/4 (22 with console)	60

The computer uses 47 to 63 Hz single phase line power, generally either 115±10% or 230±10% vac (other frequencies and voltages are available on special order). The power source should be capable of supplying 15 amperes. The power cable has a standard 3-wire plug and should be plugged into a receptable rated at 15 amperes.

	Processor	Teletype
Line current (115 vac)	4 amperes	2 amperes Turnon surge, 7 amperes
Dissipation	400 watts	92 watts

The +5 vdc output of the power supply can deliver 12 amperes, of which about 5 1/2 are used by the processor with 4K of memory and teletype control; the rest is available for additional memories and IO interfaces. Extra power supplies can be mounted at the back of an expansion chassis.

3.3 LOGIC DESCRIPTION

Timing, major state, manual function, register and memory control logic is included on the CPU1 board. Power monitor option logic

CHAPTER III
MAINTENANCE

3.1 SPECIAL TOOLS AND TEST EQUIPMENT

The following is a list of special tools and test equipment recommended for efficient maintenance of the Nova.

MULTIMETER	SIMPSON MODEL 260 OR EQUIVALENT
OSCILLOSCOPE	TEKTRONIX 453 OR EQUIVALENT
LONG LEAD PROBES	TEKTRONIX P6010-10X OR EQUIVALENT
CURRENT PROBE	TEKTRONIX P6022 OR EQUIVALENT
NOVA EXTENDER BOARD	DGC 107-000007-02
WIRE WRAP TOOL (24 GAUGE)	GARDNER DENVER Model 14AX2 OR EQUIVALENT
IC TEST CLIP	MANUFACTURED BY A P INC. Cleveland, Ohio (part no. 9237ØØ)
SOLDERING IRON	WELLER ISOLATED MODEL W-TCP OR EQUIVALENT

3.2 PHYSICAL DESCRIPTION

The table model is housed in a cabinet, but the NOVA is also available for mounting in a standard 19 inch rack. The power supply located at the rear of the unit has long life PAMOTOR fans mounted at either end. Seven slots numbered from the bottom up and accomodating 15 x 15 inch printed circuit boards are contained in the unit. Circuit boards are removed and inserted from the right side. Slot allocation is normally as follows:

SLOT	BOARD
1	CPU1
2	CPU2
3	IO
4	MEMORY

and controls shifting so that each bit is read in the middle of its period. The lower register receives a character from the bus and supplies it serially to the output line with the necessary start and stop bits. As the character goes out, the register fills with 1s allowing the net at the left to determine when transmission is complete.

Reader. The logic shown in the center of drawing 4 turns on the reader, senses the leading edge of the feed hole, and generates a strobe to read the data holes into the reader buffer when the feed hold is centered over its photodiode.

Punch. The logic in the upper left of drawing 5 senses the proper position in the punch operating cycle to trigger a one-shot that allows 1s in the punch buffer to drive the solenoids in the punch (the leftmost driver always goes on to punch the feed hold). Holding on the punch feed switch keeps the buffer clear and allows every synchronizing signal from the punch to trigger the one-shot and thus produce blank tape. The optional logic in the center of the drawing allows the program (instead of the operator) to turn on the punch, and it remains on unless it is not called for five seconds. A more detailed description of the punch interface is given on page A21 in the reference manual.

PROCESSOR OPTIONS

Through the logic in the lower right of drawing 3 the program selects the interrupt frequency for the real time clock. The binary and decade counters above generate three clock frequencies from a 16 KHz source. The logic at the left requests interrupts at the specified frequency as selected through the four AND gates in the lower left corner (the bottom gate is for line frequency).

Drawing 11 shows the optional power monitor. An insipient failure in the main supply output sets the Power Failure flag at the top, and 1 to 2 ms later RUN clears (drawing 26-1 A4). Following restoration of adequate levels in both memory and logic power, the one-shot sets RESTART if the Key is in the locked position at the console. This in turn sets RUN and triggers the processor timing circuits through the logic associated with the console switches.

Drivers for the data lines, device selection lines and various control lines on the in-out bus are at the right in drawing 27-4. Decoding of IO instructions and generation of levels to control input and output are at the right of IR in print 27-1. The loading of MA from the bus is controlled directly by the input gating to PE at the left end of that register on the same print. The control bits in an IO transfer instruction are decoded by the net in the upper left on print 27-2. The Interrupt On flag and the decoding of the interrupt instructions is in the lower left of drawing 27-4. Timing gates for data output are at bottom center in print 26-3; the generation of control signals for the interrupt and the data channel are at the left in that print and at the lower left in print 26-2.

The table on the first page of Appendix A lists the level, direction, and back panel and external bus pin connections for all the signals on the IO bus. Pages A3-A5 of the reference manual describe all of these signals. Pages A11-A17 present a detailed discussion of the timing for all operations over the bus.

Basic IO Equipment. The basic logic networks used in all interfaces are described on pages A18-A20 of the reference manual. The interfaces for teletype, reader and punch are usually mounted on a single IO board (the board may also contain the real time clock, but this is treated as a processor option). The common receivers, device selection signals and interrupt priority determining circuits on this board are shown in drawing 1.

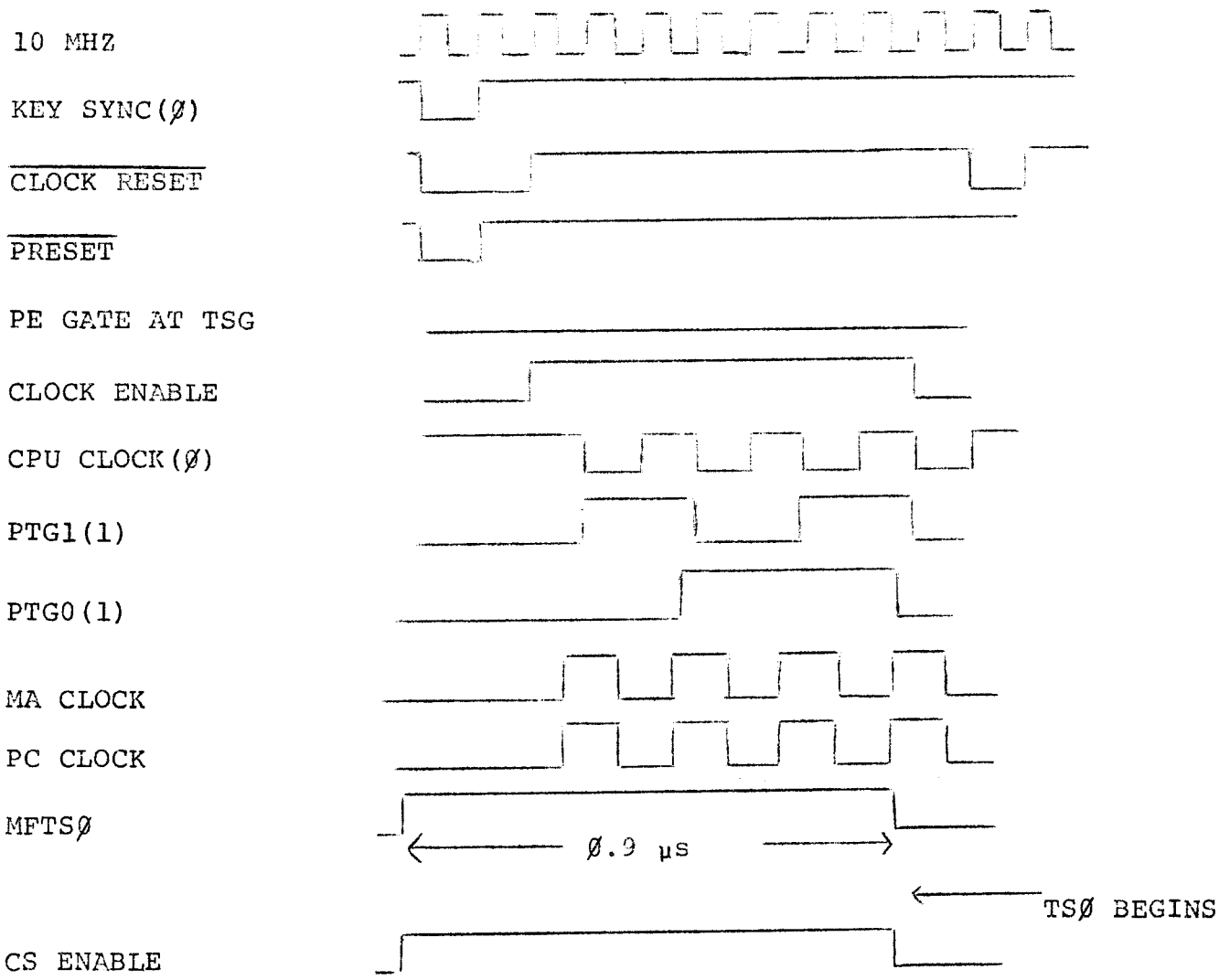
Drawing 25 shows the teletype interface. The keyboard and printer are two separate devices, and the Busy, Done and interrupt logic for both of them are in the lower half of the drawing. The Busy flag for input is set only to turn on the reader, which is controlled by the flipflop in the upper right corner. The circuit includihg the 4 bit counter at right center generates an input clock, which is divided by four by the flipflops at the lower right to produce the output clock. The clock frequencies depend upon teletype speed, but for the standard Models 33 and 35 the input clock is 880 Hz and the output clock is 220 Hz. The input clock must be faster in order properly to receive the asynchronous input.

Both input and output use shift registers to handle the serial transmission of teletype characters. The upper register receives input from the incoming line. The logic in the upper left detects the start bit (space), prevents the receiver from responding to a transient on the line,

single Y winding at 16 core locations. Inhibit and sense windings thread through planes of cores so that each winding intersects every location at the same bit. The two sets of switches at the right in drawing 14-1 establish current paths to and from the X and Y windings in the selected memory. The lines at the right of the lower set are the current source and return lines for the X windings. RXR should be regarded as being connected through a resistance to some positive voltage, whereas RXS should be regarded as being connected through a resistance to ground. In the read part of the cycle, the left pair of switches connect the read source line to RXR and the read return line to RXS. Similarly for writing, the right pair connect the write source to RXR and the write return to RXS.

The X and Y windings and associated selection logic are shown in drawing 14-2. In each of the matrices a single winding is driven by turning on one switch in the group at the left of the matrix and one switch in the group below the matrix; this allows current to pass through only that winding that is connected to the two on switches. Consider the selection of the Y winding for location 0. MA is clear so the Y selection signals SY00 and SY0 are generated, turning on the switches associated with them. For read, a current path is established from the read source through the upper diode at SY00, through the winding at the left end of the bottom row, through the leftmost diode at SY0, and through the switch to the read return. For write, the source and return wires are connected to the opposite switches so that current flows in the opposite direction. The path is from the write source through the diode just at the left of the SY0 switch, through the rightmost diode at that switch, through the winding at the left end of the bottom row, through the SY00 switch, and the lower diode at that switch to the write return.

In both read and write, half of the drive current is applied to an X winding and half to a Y winding so that a full drive current is applied to the core location at which the windings intersect. For read, the direction of the current is such that all the cores are driven to the 0 state. Hence any cores that were 1, change state, producing pulses on the sense windings threaded through those planes. These pulses, through the sense amplifiers in drawing 14-3, set individual bits of the MEM register. For write, the drive current is applied in the opposite direction and thus tends to drive all the cores in the selected location to the 1 state. But flipflops in MEM that contain 0s enable inhibit drivers among those shown in print 14-3. Hence inhibit current that opposes the X and Y drive current is applied to those planes corresponding to 0s in the word to be written. In the selected location the X and Y drive currents, therefore, change the states of only those cores that correspond to 1s in the data.



TIMING FOR MANUAL FUNCTIONS

when the function terminates. The flipflop is also cleared by a power failure, a programmed halt, or the operator pressing stop or reset.

The operational sequences that occur in the console functions are shown at the bottom of the flow diagram. The setting of KEY SYNC not only sets RUN, but also clears the CLOCK RESET flipflop (drawing 26-1 C7) to trigger the timing sequence shown in the illustration on the next page.

MEMORY

The 8-bit shift register shown at the left in print 26-3 is in the processor, but it supplies timing for the memories connected to the memory bus. The sequence of states in the memory time generator is shown in the bottom half of the timing diagram (print 18). MTG acts as a straight shift register governed by the 10 MHz clock until MTG5 sets, at which time the gating connected to PE holds that state until data just read has been transferred to the processor. Shifting is then resumed until the memory cycle is completed, when the gating again enables PE to clear the register and hold it clear. The generator outputs provide the various memory timing signals shown at the upper left.

A single 4K memory is shown in the three sheets of drawing 14 (drawing 16 shows equivalent logic for a 2K memory). The given memory is selected by decoding bits 1-3 of MA as shown in the lower left and in the center of print 14-1. Bits 4-15 of MA are decoded in four sets of three bits for signals that select the X and Y windings. The decoding of MA4-6 is duplicated in each memory and is shown at bottom center of print 14-1; selection signals are decoded from the remaining nine MA bits in the processor and supplied to all memories by via the bus (lower left, print 27-2).

Data is transferred between the memory bus and the selected core bank through the buffer at the left in drawing 14-1. Data transfers between MEM and the bus are made four bits at a time. The memory clock, which is simply a buffered processor clock (print 26-1 D6), shifts in four bits at a time from the adder outputs, or makes four bits at a time available to the bus as the MEM signals. Transfers between MEM and core are in parallel. Data levels are supplied to the inhibit drivers from the flipflop 0 outputs; to receive a word from core the register must first be cleared, and then individual flipflops are set by the sense amplifier outputs.

The Nova uses a 3-wire memory in which the X and Y drive windings use bidirectional current polarities for reading and writing. Each X and Y threads through a plane of cores in such a way that every X winding intersects with a

next. The ONE ENABLE signal supplies an initial carry into the LSB in the first step for incrementing and subtraction. For a skip the first gate at the right in the Σ3 stage combined with the carry allows incrementing by two. In all other steps the carry into Σ3 is that saved from the previous step. The net in the upper left generates a carry that depends only on the carry out of the Σ0 stage except in the final step, when it depends also upon the present state of CARRY and the base value selected by bits 10 and 11 of the instruction. The net at the input to CARRY SAVE includes not only the adder carry output but also gates for shifting, at the completion of the function the same net supplies input to CARRY unless loading is inhibited.

Register Control. The circuits that generate the gating inputs to the adder and the load and clock inputs to the various registers are almost all shown in drawing 26-2. The clocks are always produced in sets of four, but in the unusual case of a parallel transfer only one is used (eg MB LOAD shown at B5 is generated only in the final PTG period of TS5 before the processor enters the DCH state, so only the final MB clock transfers data into MB from the bus). The conditions that product any given signal can be determined from the positions at which the function appears in the flow chart. In general the meanings of the names are self-evident: EFA controls the calculation of the effective address, NEG EXTEND governs the extension of a negative displacement into a full word. The signal AC WRITE ENABLE in B6 is used to generate AC LOAD from the processor clock in print 26-1 D7. The gates that control input from the IO bus to MA are shown at the left end of MA in print 27-1. Some AC control signals are generated by the logic shown at the left of the ACs in print 27-2. Decoder E54 decodes instruction bits 8 and 9 for IO pulses in a nonskip IO instruction, but otherwise decodes them for the levels to control shifting and swapping.

The only remainign control input to the adder is the skip signal, whose generation is shown in the upper left of drawing 27-4. During an operation in the adder, the flip-flop at the top gets set and stays set only if the result is zero. The gates below it test for the various arithmetic conditions in an ALC instruction, for zero in a DXZ or ISZ, or for the selected state of Busy, Done or Interrupt On in an IO skip.

Console Control. Drawing 8 shows the logic signals associated with the switches and indicators on the console. The control logic for the operating switches is in the lower left of drawing 26-1. Through the net in A7 the closure of any switch except stop, continue, instruction step or memory step generates a preset that initializes the computer state. Any switch closure except stop or reset acts through a circuit including Schmidt triggers and flipflops to set RUN. But if the switch function is not one which requires the computer to go into continuous operation, run clears

PREFACE

This manual is intended to aid personnel in the maintenance of the Nova. Included are descriptions of the control logic for the teletype, reader and punch, but separate manufacturers' manuals are furnished for the devices themselves.

The first chapter presents a general description of the system and its operation. This includes a discussion of the physical and electrical characteristics of the computer, its logical organization, and the controls and indicators on the operator console. Chapter 2 presents a complete, detailed description of the system logic, including a discussion of the symbols and notation used in the logic drawings. Chapter 3 contains information useful in maintaining the system, including a discussion of maintainance programs, troubleshooting procedures, and instructions for removing, repairing and replacing both major and minor components.

Following Chapter 3 are lists of logic signals and components and an illustrated parts breakdown. Drawings referred to in the text are grouped at the back of the manual.

The remaining processor registers are the accumulators shown at the top of print 27-2. Each register package contains four bits of each accumulator. The package is arranged as a 4 x 4 matrix such that a high level on one of the upper four lines coincident with a high arc on one of the lower lines will connect a single flipflop to both the input and output. The upper four OR gates select a single AC, and the lower OR gates connect a single bit of that AC to the input and output in each package. Thus the outputs AC0 to AC3 are a 4-bit contiguous byte of the selected accumulator and the Σ levels supply data input to the same bits. The order in which the bytes are selected is the standard one except in a swap.

CONTROL LOGIC

Control other than for memory and in-out includes the adder, the generation of the control signals for the adder and the registers, and the circuits associated with the console.

Adder. In drawing 27-3 each of the inverted Vs represents a 1-bit, 3-input adder circuit. Each stage in the adder receives two summand inputs and a carry input from the preceding stage; the outputs are a 1-bit sum and a carry out to the next stage. In a given stage the sum is true if an odd number of inputs are true (i.e., a single one or all three); the carry out is true if two or more of the inputs are true. A straightforward transfer is accomplished through the adder by enabling only one set of summand inputs. A word is shifted right or left by taking as input at each stage the bit one place to the left or right respectively. The AND function is performed by disabling one set of summand inputs and supplying MA and an AC through AND gates as the other set. Subtraction is accomplished by using the complement for one set of summand inputs and inserting a carry into the least significant bit.

Since all functions are performed in four 4-bit steps, the circuits in the upper left and the lower right, together with the CARRY SAVE flipflop at the extreme lower right corner of drawing 27-1, handle the carry from one step to the

REGISTERS

The major registers are shown in drawing 27-1. PC, MB and MA are each composed of four 4-bit shift registers; each shift register package contains one bit from each of the four 4-bit bytes in the word, so that after each shift, complementary outputs for a new byte of four contiguous bits are available. A low level at MR clears the four flipflops in the package. The effect of a clock input at CP depends on the level at PE. If PE is high, each clock, shifts the contents of the register right one place with data for the left bit supplied at the complementary inputs J and $\bar{K}$. If PE is low, J and K are disabled and a single clock load the inputs at pins 4-7 directly into the flipflops. Hence MA and MB can both receive sixteen bits in parallel from the IO bus. The load inputs to PC include only four bits from MB and the others are connected to PC outputs in a shoft configuration; hence while PC LOAD is true, four clocks are required to shift MB into PC. The shift inputs to all three registers are the Σ outputs of the adder except that in right shifting the normal Σ0 and Σ3 inputs to MA are replaced by MA15 and CARRY SAVE.

The bits in IR (at the bottom of the drawing) are connected so that each clock brings in the four data bits from the memory bus into the first four IR bits and shifts four contiguous bits into the next package. The circuits above IR decode the AC addresses and decode function codes for all but the ALC instructions. If IR0 is 0, E86 decodes bits 1 and 2 for an instruction; when IR0 is 1, outputs 4-7 are actually decoding bits 1 and 2 for an AC address when the appropriate enabling level is present at D. Similarly E85 decodes either the jump and memory modify instructions or the destination AC.

The console switch register is shown at the center of print 8. Here each of the PTG levels selects four switches for input to the adder.

TIMING FOR ADD INSTRUCTION

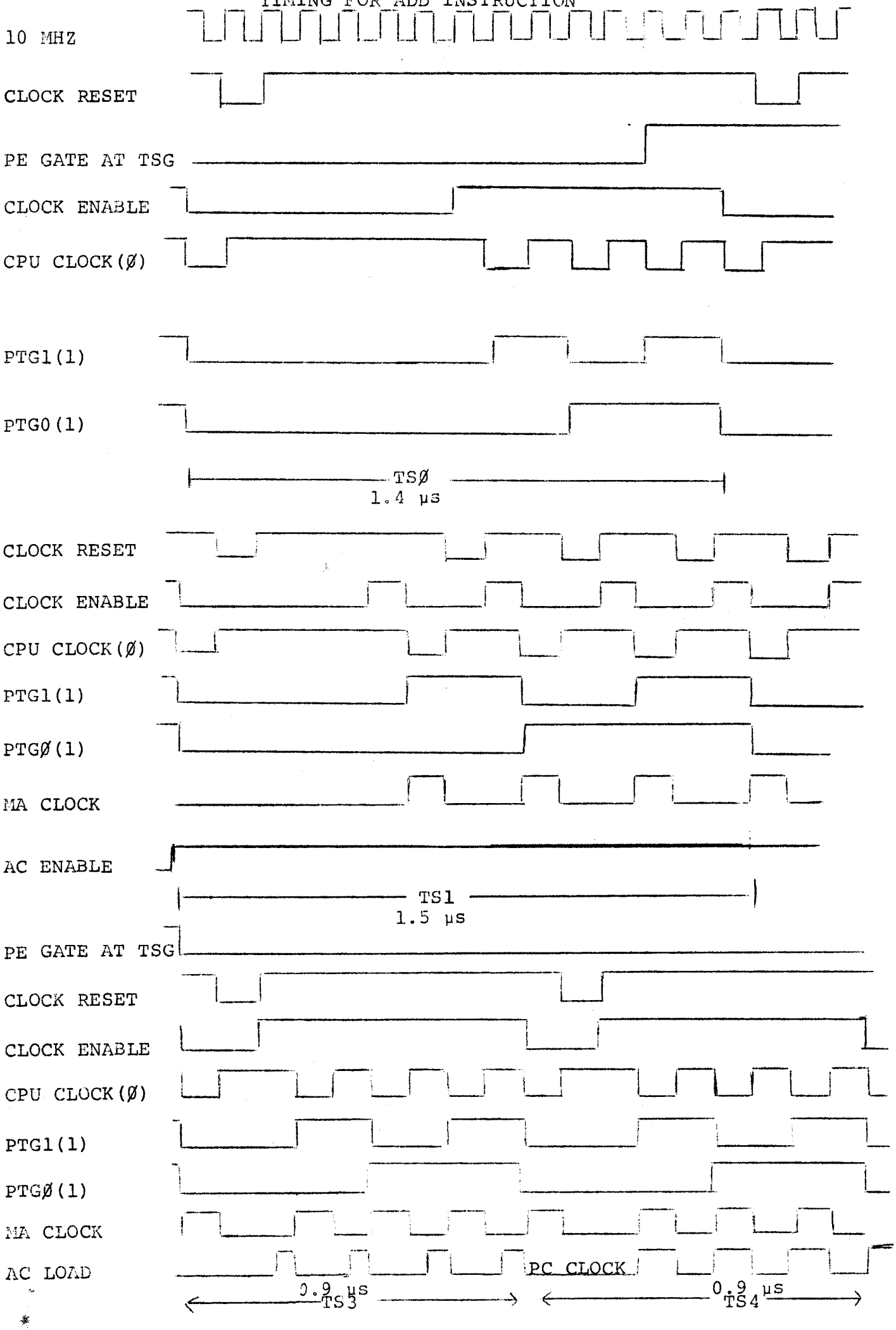
Note 1: TSØ -- MEM to MGM,MB.
In STA, TSØ is 1.7 μs with CPU CLOCK spaced every .3 μs.

Note 2: TS1 - ACS to MA.
TS2 timing is identical - ACD to MA.
In instruction with AC access time state is 1.2 μs with CPU CLOCK spaced every .2 μs.

Note 3: TS3 - MA to ACD,MA.

Note 4: PC + S + 1 to MA,PC.

TIMING FOR ADD INSTRUCTION



TIMING

Drawing 26-1 shows the logic for processor timing. From left to right in the upper part of the drawing are the processor clock, the processor time generator, the time state generator, and a set of five flipflops that determine the major state of the processor. The sequence of major states and time states within them and the specific operations that occur at each time state are shown in the flow diagram, print 17. A preset signal generated by power clear or certain actions at the console (print 26-1 A7) clears all the PTG and TSG flipflops and places the processor in the fetch state.

The basic timing element is the 10 MHz clock shown at B2. This is the clock input to all flipflops and gates that control 4-step transfers in the processor. In particular it controls CPU CLOCK (C7) and together with that clock controls the processor time generator. Gates shown above the PTG flipflops generate timing levels during the first and last PTG states for gating the adder and other elements involved in transfers and other functions. Similar levels for the intermediate two states are generated at the AC input gating shown in C6 of print 27-2. The 10 MHz clock, appropriately gated, also generates the clocks that control shifting in the various registers. These include AC LOAD in the upper left of print 26-1 and the clocks for PC, MA, MB and IR in the upper left of print 26-2. Some processor timing is shown in the memory timing diagram (print 13), and complete timing for the ADD instruction is shown in the illustration on the next page. The MTG inputs to the gating for CPU CLOCK are from the memory timing generator whose operation is shown in the memory timing diagram.

The time state generator at D4-5 in print 26-1 is a shift register that controls the sequence of time states. The input to CP from PTGO can sequence the generator through the time states in order as shown in the right column on print 18, but the gating connected to PE (and depending upon the state of TSGO) can advance the generator directly to TS4 from TS0, TS1 or TS2 or return it to TS0 when the cycle is complete.

In every cycle, one and only one of the major state flip-flops is set, and it determines the type of cycle, ie the major state in which the cycle takes place. At the end of each cycle the return to 0 of TSG3 alters the major state according to the conditions in the input gating shown below the flipflops. These conditions correspond to those shown in TS4 and TS5 in the flow chart.

Signal Notation. Flipflop outputs are named by the output in parentheses following the flipflop name. Hence the 1 output of CARRY is CARRY (1) and the 0 output of bit 6 of MA is MA6(0). Other signal names are mnemonics that indicate the function or meaning of the signal. These often employ full words so that the meaning is obvious, or use letter combinations (such as the instruction mnemonics) that are defined in the reference manual.

every circuit by type and by physical location. The symbology used is substantially equivalent to that of military specification 806B. For examples consider drawing 27-1. A triangle represents an inverter, a D-shaped symbol is an AND gate, an arrow-shaped symbol is an OR gate. The small rectangles at the lower right are flipflops; the twelve large horizontal boxes in the upper part of the drawing are 4-bit shift registers; the three vertical boxes just below them are binary-to-decimal decoders (used for binary to octal). Other boxes are actually labeled with the name of the circuit, such as a clock or a Schmidt trigger.

Each box is also labeled with the letter E followed by a number; this indicates the position of the IC on the board. These position numbers are etched right on the board in the vicinity of each IC whenever possible, but in any event the numbers are assigned from left to right beginning at the connector end of the board. (The power monitor, if present, occupies positions E1, E2 and E3 on CPU-1.) The numbers of the IC input and output pins are written where the signal lines intersect the boundary of the circuit symbol. Each of the large boxes such as a shift register or a decoder is an entire IC. The two flipflops in the lower right of drawing 27-1 are both contained in a single IC at position E30. Note that in the input gating to the lower flipflop there are no pin numbers at the outputs of the AND gates or the inputs to the OR gate; in this case only the OR gate is labeled for position and all of the AND gates are contained within the same IC. A circle at the opposite end of a signal line from a circuit logic symbol indicates a contact finger on the board and is labeled with the back panel pin number (e.g., the clock signal in A1).

By convention a logic level is regarded as true when high and false when low. If a line carries a logic level that represents some logic function X, then the line is labeled X if it is high when X is true, but is labeled $\overline{X}$ (not X) if it is low when X is true. A circle at the input or output of a box indicates that a low signal satisfies the function involved. Consider the gates beginning with E66 in B8 of print 27-1. Three high inputs to the bottom AND gate produce a low output, any low input to the OR gate above it produces a high output, and both inputs high at the top gate produces a low signal out. In the input gating at the left of the CARRY flag (B2-3) the circle at pin 1 of inverter E42 indicates that the circuit is enabled by a low signal. Since the input is $\overline{TS3}$ (which indicates that TS3 is true when the signal is low), the AND function for gate E80 can be satisfied only during time state 3. On the other hand the second AND gate from the bottom in A2 also has $\overline{TS3}$ as an input, but there is no circle; hence this gate is satisfied by a carry only in some time state other than 3.

Flipflops such as those shown in A1 and B1 have a clock input, a synchronous data input, asynchronous set and clear inputs, and complementary outputs. A positive transition at input C sets the flipflop if D is high, clears it if D is low, unless there is a circle at the D input, in which case the flipflop is set when D is low, cleared when D is high. In the set state the flipflop 1 output is high, the 0 output is low. Asynchronous set and clear inputs are shown only if used and are respectively at the top and bottom of the box; e.g., IR8 in A5 is cleared by a ground level at pin 13. Inputs of this type take precedence over the clock input. The JK type of flipflop is also used, always with AND gates at the data inputs (refer to the upper left of print 26-2). A positive transition at the clock input sets the flipflop if only J is high, clears it if only K is high, but complements it if both are high.

CHAPTER TWO

SYSTEM LOGIC

Accompanying each Nova is a complete set of drawings, consisting of reduced copies of D-size logic block diagrams and other electrical drawings. At the lower right corner of every drawing, below the title, is a letter indicating size, a 3-digit drawing code, a 6-digit drawing number, and a 2-digit revision number. If a single drawing consists of several sheets, both the sheet number and the number of sheets are written at the left of the size letter.

The code number indicates the type of drawing. In general the only drawing types of interest to the user are electrical drawings code 001, mechanical code 002, and printed circuit boards code 107. Contained in this manual are a single mechanical drawing showing the installation, and a number of electrical drawings including logic drawings, a flow chart, a timing diagram, the back panel layout and the power supply.

The revision number indicates the number of times the drawing (and hence the equipment shown) has been revised since being signed by the project engineer. The revision numbers on the drawings in this manual reflect the standard production model machine at the time the manual was published. A particular drawing for some machine in the field may have a revision number lower or higher than the one on that drawing in this manual. Thus the manual drawings should be used for instruction purposes only, and maintenance personnel should use the separate drawing package for work on the equipment.

For convenience leading zeros will be dropped in drawing references, and for drawings with two or more sheets, the sheet number will be given after a dash following the drawing number. Hence sheet 2 of drawing 000027 is variously referred to in the text as drawing 27-2 or print 27-2. Sections of a drawing are called out by the coordinates printed at the edges.

LOGIC DRAWINGS

The logic drawings are block diagrams that show the function of every logic element used in the computer. They also indicate the signal present at any IC pin or connector pin that carries a logic signal or some special voltage. In addition to giving the function of every logic element, the drawings identify

MEMORY STEP — Perform a single processor cycle in the state indicated by the lights and then stop. At completion the lights indicate the next state to be executed.

CAUTION

Using the AC switches between memory steps within an instruction usually destroys information necessary for the execution of the rest of the instruction.

RESET — Stop at the end of the current processor cycle. Clear the flags in all IO devices, clear Interrupt On, and set the clock to line frequency.

EXAMINE can be used to load PC for beginning any single step procedure. Instruction stepping can also be begun by pressing START while holding STOP on.

To use the various examine and deposit switches between instruction steps, simply remember what PC is and restore it before continuing.

EXAMINE — Load the address contained in the data switches into PC (which is displayed in the address lights) and display the contents of the addressed location in the data lights. At completion FETCH is lit.

DEPOSIT — Deposit the contents of the data switches in the memory location specified by the address lights. At completion FETCH is lit and the data lights display the word deposited.

EXAMINE NEXT — Add 1 to the PC address lights and display the contents of the location specified by the incremented address in the data lights. At completion FETCH is lit.

DEPOSIT NEXT — Add 1 to the PC address displayed in the address lights and deposit the contents of the data switches in the memory location specified by the incremented address. At completion FETCH is lit and the data lights display the word deposited.

START — Load the address contained in the data switches into PC, light FETCH and RUN, and begin normal operation by executing the instruction at the location specified by PC.

STOP — Stop with FETCH on before beginning the next instruction. Thus the processor finishes the current instruction, and then stops with the instruction lights displaying the instruction, unless a device is waiting for data channel access or a program interrupt, in which case it performs all such operations before stopping with the instruction lights off. The address lights point to the next instruction.

CAUTION

If the current instruction contains an infinitely long indirect addressing chain or there are continuous data channel requests, pressing STOP will not stop the computer (See RESET, below).

CONTINUE — Turn on RUN and begin normal operation in the state indicated by the lights.

INST STEP — Begin operation in the state indicated by the lights but then stop as though STOP had been pressed at the same time. If the stop occurs at the end of an instruction, the data displayed by the data lights depends on the instruction as follows.

LDA, STA, ISZ, DSZ	Operand
JMP	Effective address
JSR	The address loaded into AC3 (old PC + 1)
Arithmetic and logical	Instruction
In-out	Instruction

Note that the AC switches can be used between instruction steps without requiring any readjustment.

DATA GENERAL
CORPORATION
Southboro,
Massachusetts 01772
(617) 485-9100

HOW TO MAINTAIN

THE NOVA

TABLE
SIGNAL REFERENCE
CENTRAL PROCESSOR (CPU)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
SNS6*	E6Ø	1Ø	MEM	Ø14-3
SNS7*	E6Ø	12	"	"
SNS8*	E2Ø	4	"	"
SNS9*	E2Ø	2	"	"
SNS1Ø*	E2Ø	12	"	"
SNS11*	E2Ø	1Ø	"	"
SNS12*	E6	2	"	"
SNS13*	E6	4	"	"
SNS14*	E6	1Ø	"	"
SNS15*	E6	12	"	"
STA	E14	8	CPU1	Ø26-1
STA*	E86	11	CPU2	Ø27-1
START	E5	6	IO	Ø1
STOP	E24	8	CPU1	Ø26-1
STROBE*	E79	8(A33)	CPU1	Ø26-3
STRT	E26	1(A52)	CPU2	Ø27-4
SUMMATIONØ	E58	2	"	Ø27-3
SUMMATIONØ*	E59	15(B78)	"	"
SUMMATION1	E58	12	"	"
SUMMATION1*	E59	2(B79)	"	"
SUMMATION2	E58	1Ø	"	"
SUMMATION2*	E59	6(B74)	"	"
SUMMATION3	E58	9	"	"
SUMMATION3*	E59	9(B76)	"	"
SXØ	E3	4(A17)	"	Ø27-2
SXØØ	E4	6(A23)	"	"
SX1	E6	1Ø(B93)	"	"
SX2	E3	6(A18)	"	"
SX3	E6	12(B96)	"	"
SX4	E3	2(A16)	"	"
SX5	E6	6(B87)	"	"
SX6	E3	1Ø	"	"
SX7	E6	2(B89)	"	"
SX1Ø	E5	12(B86)	"	"
SX2Ø	E3	12(A21)	"	"
SX3Ø	E6	8(B9Ø)	"	"
SX4Ø	E3	8(A2Ø)	"	"
SX5Ø	E6	4(B88)	"	"
SX6Ø	E4	4(A22)	"	"
SX7Ø	E5	1Ø(B85)	"	"
SYØ	E4	8(A28)	"	"
SYØØ	E48	8	MEM	Ø14-1

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
CENTRAL PROCESSOR (CPU)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
SY1	E5	2(B3Ø)	CPU2	Ø27-2
SY2	E4	1Ø(A27)	"	"
SY3	E5	8(B32)	"	"
SY4	E4	12(A26)	"	"
SY5	E5	6(B2Ø)	"	"
SY6	E4	2(A24)	"	"
SY7	E5	4(B22)	"	"
SY1Ø	E48	1Ø	MEM	Ø14-1
SY2Ø	E48	12	"	"
SY3Ø	E43	12	"	"
SY4Ø	E43	1Ø	"	"
SY5Ø	E48	6	"	"
SY6Ø	E48	4	"	"
SY7Ø	E48	2	"	"
TSØ	E4	4	CPU1	Ø26-1
TSØ*	E2Ø	6	"	"
TS1	E4	8(A1Ø)	"	"
TS1*	E2Ø	11	"	"
TS2	E4	6(A6)	"	"
TS2*	E2Ø	3	"	"
TS3	E13	2	"	"
TS3*	E22	11(A36)	"	"
TS4	E13	4(B84)	"	"
TS4*	E22	8	"	"
TS5	E4	1Ø	"	"
TS5*	E2Ø	8	"	"
TSGØ(Ø)	E4	2	"	"
TSGØ(1)	E21	15	"	"
TSG1(Ø)	E4	12	"	"
TSG1(1)	E21	14	"	"
TSG2(Ø)	E36	6	"	"
TSG2(1)	E21	13	"	"
TSG3(Ø)	E21	11	"	"
TSG3(1)	E21	12	"	"
TSØ.DCH	E75	4	"	Ø26-2
TSØ.DCH*	E74	6	"	"
TSØ.F	E48	12	"	"
TSØ SET	E36	4	"	Ø26-1
TTI ACK	E25	4	IO	Ø1
TTO ACK	E25	2	"	"
WRITE	E6Ø	8(B68)	CPU1	Ø26-3
+5ØK*	E41	12	"	Ø26-1

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
TELETYPE (ASR33)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
DATA8*	E13	13(B6Ø)	IO	Ø25
DATA9*	E15	4(B63)	"	"
DATA1Ø*	E15	13(B75)	"	"
DATA11*	E13	1(B58)	"	"
DATA12*	E13	1Ø(B59)	"	"
DATA13*	E15	1(B64)	"	"
DATA14*	E13	4(B56)	"	"
DATA15	E12	1	"	"
DATA15*	E15	1Ø(B66)	"	"
ILU(1)	E18	9	"	"
INPUT CLOCK	E2	12	"	"
INTR*(TTI)	E12	1Ø(B29)	"	"
INTR*(TTO)	E12	13(B29)	"	"
LINE(Ø)	E28	11	"	"
LINE91)	E28	12	"	"
OUTPUT CLOCK	E16	5	"	"
READER RUN(1)	E18	5	"	"
READER START*	E42	11	"	"
READER STOP*	E39	8	"	"
SELB*	E11	1(A8Ø)	"	"
SELD*	E11	1Ø(A82)	"	"
SPIKE DETECT(Ø)	E19	8	"	"
SPIKE DETECT(1)	E19	9	"	"
START(1)	E28	13	"	"
STOP1(1)	E9	14	"	"
STOP2(1)	E9	15	"	"
STRT + CLR + RST	E4Ø	8	"	"
SYNCØ(1)	E2Ø	8	"	"
SYNC1(1)	E21	9	"	"
SYNC2(1)	E21	5	"	"
TTI DATI	E32	4	"	"
TTI DONE(1)	E17	9	"	"
TTI INT DISABLE(1)	E36	9	"	"
TTI INT REQ(1)	E37	8	"	"
TTI RUN(1)	E22	9	"	"
TTI SELECT	E32	12	"	"
TTI START(Ø)	E2Ø	5	"	"
TTI START(1)	E2Ø	6	"	"

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
TELETYPE (ASR33)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
TTOØ(1)	E9	13	IO	Ø25
TTO1(1)	E9	12	"	"
TTO2(1)	E8	15	"	"
TTO3(1)	E8	14	"	"
TTO4(1)	E8	13	"	"
TTO5(1)	E8	12	"	"
TTO6(1)	E28	15	"	"
TTO7(1)	E28	14	"	"
TTO BUSY(1)	E35	5	"	"
TTO DONE(1)	E35	9	"	"
TTO FINISH	E32	2	"	"
TTO INT DISABLE(1)	E36	5	"	"
TTO INT REQ(1)	E37	6	"	"
TTO SELECT	E32	1Ø	"	"
TT RDR BUSY(1)	E17	5	"	"

TABLE
SIGNAL REFERENCE
H.S. PAPER TAPE READER (PTR)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
CH1	E63	7(A69)	IO	Ø4
CH2	E63	6(A67)	"	"
CH3	E63	5(A65)	"	"
CH4	E63	4(A63)	"	"
CH5	E64	7(A61)	"	"
CH6	E64	6(A59)	"	"
CH7	E64	5(A57)	"	"
CH8	E64	4(A49)	"	"
DATA8*	E49	13	"	"
DATA9*	E49	1	"	"
DATA1Ø*	E49	1Ø	"	"
DATA11*	E49	4	"	"
DATA12*	E48	13	"	"
DATA13*	E48	1Ø	"	"
DATA14*	E45	1	"	"
DATA14*	E48	4	"	"
DATA15*	E48	1	"	"
FWD	E44	2(A47)	"	"
GO(Ø)	E79	6	"	"
GO(1)	E79	5	"	"
INTR*	E45	4	"	"
RD BUSY(Ø)	E46	8	"	"
RD BUSY(1)	E46	9	I/O Bd.	"
RD CLEAR*	E44	12	IO	"
RD DONE(Ø)	E46	6	"	"
RD DONE(1)	E46	5	"	"
RD INT DISABLE(Ø)	E47	8	"	"
RD INT DISABLE(1)	E47	9	"	"
RD INT REQ(Ø)	E47	5	"	"
RD INT REQ(1)	E47	6	"	"
RDRØ	E64	15	"	"
RDR1	E64	14	"	"
RDR2	E64	13	"	"
RDR3	E64	12	"	"
RDR4	E63	15	"	"
RDR5	E63	14	"	"
RDR6	E63	13	"	"
RDR7	E63	12	"	"
RD READY*		A75	"	"
RD SELECT	E81	8	"	"
RD STROBE(Ø)	E79	8	"	"

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
H.S. PAPER TAPE READER (PTR)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
RD STROBE(1)	E79	9	IO	Ø4
SELB*	E45	1Ø(A82)	"	"
SELD*	E45	13(AØ)	"	"
SPKT		A77	"	"
STOP	E81	6(A71)	"	"

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
H.S. PAPER TAPE PUNCH (PTP)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
DATA14*	E71	1(B56)	IO	Ø5
DATA15*	E71	4(B56)	"	"
FEED HOLE	E71	1Ø	"	"
HOLE1	E74	1Ø(B25)	"	"
HOLE2	E74	4(B28)	"	"
HOLE3	E74	1(B4Ø)	"	"
HOLE4	E74	13(B48)	"	"
HOLE5	E76	1Ø(B67)	"	"
HOLE6	E76	4(B34)	"	"
HOLE7	E76	1(B49)	"	"
HOLE8	E76	13(B31)	"	"
INTR*	E57	1Ø(B29)	"	"
OUT OF TAPE	E72	8(B36)	"	"
PUNØ	E75	15	"	"
PUN1	E75	14	"	"
PUN2	E75	13	"	"
PUN3	E75	12	"	"
PUN4	E73	15	"	"
PUN5	E73	14	"	"
PUN6	E73	13	"	"
PUN7	E73	12	"	"
PUN BUSY(Ø)	E56	6	"	"
PUN BUSY(1)		5	"	"
PUNCH FEED*	B23		"	"
PUN COMPLETE	E87	6	"	"
PUN DONE(Ø)	E56	8	"	"
PUN DONE(1)	E56	9	"	"
PUN INT DISABLE(Ø)	E55	8	"	"
PUN INT DISABLE(1)	E55	9	"	"
PUN INT REQ(Ø)	E55	5	"	"
PUN INT REQ(1)	E55	6	"	"
PUN SELECT	E58	1Ø	"	"
PUN START*	E59	11	"	"
PWR ON*	E89	8(B11)	"	"
SELB*	E57	4(A82)	"	"
SELD*	E57	1(A8Ø)	"	"
UP TO SPEED	E91	6	"	"

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
REAL TIME CLOCK (RTC)

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
CLKØ(Ø)	E7Ø	6	IO	Ø3
CLKØ(1)	E7Ø	5	"	"
CLK1(Ø)	E7Ø	8	"	"
CLK1(1)	E7Ø	9	"	"
CLK INT DISABLE(Ø)	E66	8	"	"
CLK INT DISABLE(1)	E66	9	"	"
CLK RESET	E52	4	"	"
CLK SELECT	E52	6	"	"
1Ø HZ	E84	12	"	"
1ØØ HZ	E85	12	"	"
1ØØØ HZ	E67	12	"	"
INTR*	E65	13	"	"
SELB*	E65	4	"	"
SELD*	E65	1Ø	"	"
SELECT 1Ø	E68	6	"	"
SELECT 1ØØ	E68	1Ø	"	"
SELECT 1ØØØ	E68	8	"	"

*INDICATES "NOT"

TABLE
SIGNAL REFERENCE
POWER MONITOR

LOGICAL SIGNAL	CHIP	PIN	BOARD	DWG
PWR LOW(Ø)	E2	6	CPU1	Ø11
PWR LOW(1)	E2	5	"	"
RESTART(Ø)	E2	9	"	"
RESTART(1)	E2	8	"	"
RESTART ENABLE	E1	12(B46)	"	"
SELD	E1	1(A8Ø)	"	"

APPENDIX B

TABLE

CHIP IDENTIFICATION LIST

CHIP	CPU1	CPU2	MEMORY(4K)	PWR. SUPP.	CONSOLE
E1	8881	8880	7474/8828	NE510A	8T90
E2	7474/8828	9007	7474/8828	NE510A	8T90
E3	9601	9016/8H90	8881	NE510A	8T90
E4	9016/8H90	9016/8H90	8T80	NE510A	8819/9004
E5	7474/8828	9016/8H90	7525	MICRO 723	8T90
E6	7474/8828	9016/8H90	9016/8H90	MICRO 723	8889/9002
E7	7474/8828	9008/8848	7525	MICRO 723	8T90
E8	9004/8819	9008/8848	8T90	MICRO 723	8819/9004
E9	9002/8889	9008/8848	8T90		8T90
E10	7474/8828	9300	8T90		8T90
E11	9004/8819	9300	8T90		8T90
E12	9002/8889	9300	SH6405		
E13	9016/8H90	9300	SH6405		
E14	9016/8H90	8880	FA3470		
E15	9022	9016/8H90	FA3470		
E16	9008/8848	9301	FA3470		
E17	9007	9301	FA3470		
E18	9009/8859	9301	7525		
E19	9009/8859	9008/8848	7525		
E20	9002/8889	9008/8848	9016/8H90		
E21	9300	9008/8848	SH6405		
E22	9002/8889	9300	SH6405		
E23	SG83/SG82	9300	9016/8H90		

TABLE

CHIP IDENTIFICATION LIST

CHIP	CPU1	CPU2	MEMORY(4K)	PWR. SUPP.	CONSOLE
E24	9016/8H90	9300	7525		
E25	9003/8879	9300	7525		
E26	7474/8828	8880	8T80		
E27	9008/8848	9002/8889	SH6405		
E28	9005/8840	9005/8840	8T80		
E29	8880	9008/8848	7474/8828		
E30	9004/8819	7474/8828	SH6405		
E31	9022	9008/8848	7474/8828		
E32	9005/8840	9008/8848	7474/8828		
E33	9022	9008/8848	7474/8828		
E34	9022	9008/8848	FA3470		
E35	9003/8879	9300	FA3470		
E36	9016/8H90	9300	FA3470		
E37	9004/8819	9300	FA3470		
E38	9003/8879	9300	FA3470		
E39	9002/8889	8880	FA3470		
E40	9002/8889	9002/8889	FA3470		
E41	9016/8H90	9005/8840	FA3470		
E42	9003/8879	9016/8H90	9004/8819		
E43	9002/8889	9002/8889	9016/8H90		
E44	8881	9004/8819	8T90		
E45	9002/8889	9008/8848	9002/8889		
E46	9008/8848	9008/8848	9009/8859		
E47	9004/8819	9008/8848	9009/8859		

TABLE
CHIP IDENTIFICATION LIST

CHIP	CPU1	CPU2	MEMORY(4K)	PWR. SUPP.	CONSOLE
E48	8H90	9016/8H90	9016/8H90		
E49	9003/8879	9016/8H90	9301		
E50	9002/8889	9016/8H90	8T90		
E51	9003/8879	8881/7401N	SH6405		
E52	9003/8879	9016/8H90	SH6405		
E53	9002/8889	9008/8848	SH6405		
E54	9003/8879	9301	SH6405		
E55	9016/8H90	9016/8H90	FA3470		
E56	9008/8848	9005/8840	FA3470		
E57	9005/8840	9002/8889	FA3470		
E58	9003/8879	9016/8H90	FA3470		
E59	9002/8889	7483	7525		
E60	9009/8859	8881	9016/8H90		
E61	9005/8840	8881	7525		
E62	9008/8848	8881	8T80		
E63	9008/8848	8881	7474/8828		
E64	9300	9002/8889	7474/8828		
E65	9300	9003/8879			
E66	9005/8840	9003/8879			
E67	9008/8848	9005/8840			
E68	9005/8840	7474/8828			
E69	9016/8H90	9002/8889			
E70	9004/8819	9002/8889			
E71	9003/8879	9016/8H90			

TABLE

CHIP IDENTIFICATION LIST

CHIP	CPU1	CPU2	MEMORY(4K)	PWR. SUPP.	CONSOLE
E72	9003/8879	5033			
E73	9002/8889	5033			
E74	9002/8889	5033			
E75	9016/8H90	5033			
E76	9005/8840	9009/8859			
E77	9008/8848	9016/8H90			
E78	9016/8H90	9004/8819			
E79	9002/8889	9002/8889			
E80	9016/8H90	9003/8879			
E81	9002/8889	9016/8H90			
E82		9301			
E83		9300			
E84		9300			
E85		9301			
E86		9301			
E87		9009/8859			
E88		9009/8859			
E89		9301			
E90		9009/8859			
E91		9009/8859			
E92		9016/8H90			

TABLE
CHIP IDENTIFICATION LIST-IO

CHIP	COM SEL,TTY	PTR	PTP	RTC
E1	NE51ØA			
E2	8281			
E3	9016/8H90			
E4	9016/8H90			
E5	9016/8H90			
E6	9016/8H90			
E7	9016/8H90			
E8	9300			
E9	9300			
E10	9004/8819			
E11	8881			
E12	8881			
E13	8881			
E14	9300			
E15	8881			
E16	7474/8828			
E17	7474/8828			
E18	7474/8828			
E19	7474/8828			
E20	7474/8828			
E21	7474/8828			
E22	7474/8828			
E23	9003/8879			
E24	9002/8889			

TABLE

CHIP IDENTIFICATION LIST-IO

CHIP	COM SEL,TTY	PTR	PTP	RTC
E25	9016/8H90			
E26	8881			
E27	9016/8H90			
E28	9300			
E29	8T80			
E30	9007			
E31	9002/8889			
E32	9016/8H90			
E33	9004/8819			
E34	9300			
E35	7474/8828			
E36	7474/8828			
E37	7474/8828			
E38	9002/8889			
E39	9016/8H90			
E40	9003/8879			
E41	9002/8889			
E42	9002/8889			
E43	9002/8889			
E44		9016/8H90		
E45		8881		
E46		7474/8828		
E47		7474/8828		
E48		8881		

TABLE
CHIP IDENTIFICATION LIST-IO

CHIP	COM SEL,TTY	PTR	PTP	RTC
E49		8881		
E50				9004/8819
E51				9002/8889
E52				9016/8H90
E53				7474/8828
E54				9008/8848
E55			7474/8828	
E56			7474/8828	
E57			8881	
E58			9016/8H90	
E59			9002/8889	
E60			9004/8819	
E61		9002/8889		
E62		9004/8819		
E63		9300		
E64		9300		
E65				8881
E66				7474/8828
E67				8281
E68				9016/8H90
E69				9002/8889
E70				7474/8828
E71			8881	
E72			9002/8889	

TABLE

CHIP IDENTIFICATION LIST-IO

CHIP	COM SEL,TTY	PTR	PTP	RTC
E73			9300	
E74			8881	
E75			9300	
E76			8881	
E77	(Used with Option 4011A)			
E78		9002/8889		
E79		7474/8828		
E80		9601		
E81		9016		
E82		9002/8889		
E83				NE510A
E84				8280
E85				8280
E86			9006	
E87			9601	
E88			NE51ØA	
E89			9016/8H90	
E90			9601	
E91			9601	

TABLE
CPU, MEMORY AND IO
COMPONENT TOTALS - IC

					IO BOARD						
IC	CPU1	CPU2	MEM (4K)	PWR MON	STD	TTY	PTR	BRPE11 PTP	4013	RTC	TOTAL
5033		4									4
7474	5	2	8	1		10	3	2		3	34
7483		1									1
7525			8								8
8H90	1										1
8T80			4			1					5
8T90			6								6
8280										2	2
8281						1				1	2
8880	1	4									5
8881	1	5	1	1	1	4	3	4		1	21
9002	15	8	1		1	5	3	2		2	37
9003	11	3			1	1					16
9004	6	2	1			2	1	1		1	14
9005	7	4									11
9006								1			1
9007	1	1				1					3
9008	8	15								1	24
9009	3	5	1*								10
9016	11	16	6		6	3	2	2		2	48
9022	4										4
9300	3	14				5	2	2			26
9301		8	1								9
9601				1			1	1	2		5
3G83	1										1

*Actual total is (2).

TABLE
CPU, MEMORY AND IO
COMPONENT TOTALS - RESISTORS

					IO BOARD						
OHM	CPU1	CPU2	MEM (4K)	PWR MON	STD	TTY	PTR	PTP	4013	RTC	TOTAL
10			4								4
75			16								16
100	1	1	8			1		2			13
150								1			1
150*			32								32
180								2			2
220	2						1	1	1	1	6
330	5	19			2			2			28
390	6	20		1	2						29
470		8	24			1	1				34
470**						1					1
560			16								16

*1/8 W 1%
**3 W 5%

TABLE
CPU, MEMORY AND IO
COMPONENT TOTALS - RESISTORS

					IO BOARD						
OHM	CPU1	CPU2	MEM (4K)	PWR MON	STD	TTY	PTR	PTP	4013	RTC	TOTAL
680			2								2
750								1			1
1K			64			1					65
1.5K	2		33							2	37
2.2K			4							1	5
2.7K						1			1		2
3K		2		3	1	6	10			2	24
3.3K						4				4	8
4.7K			32			1					33
5.6K						1					1
7.5K							1				1
8.2K	1										1
15K								1			1
33K				1				2			3
68K								1			1

TABLE
CPU, MEMORY AND IO
COMPONENT TOTALS - CAPACITORS

					IO BOARD					
CAPACITOR	CPU1	CPU2	MEM (4K)	PWR MON	STD	TTY	PTR	PTP	4013	RTC
220PF			8							
470PF							1			
560PF, 300V						1				
820PF										1
1200PF	1									
.01MFD, 50V										9
.05MFD, 50V	35	47	4	1	4	14	8	10		
.22MFD, 20V							1			
1MFD								2		
6.8MFD, 6V			8	1						
6.8MFD, 35V	14	13	23		1	2	3	3		3
47MFD, 20V									2	

TABLE
CPU, MEMORY AND IO
COMPONENT TOTALS - TRANSISTORS, ETC.

					IO BOARD					
COMPONENT	CPU1	CPU2	MEM (4K)	PWR MON	STD	TTY	PTR	PTP	4013	RTC
DIODE FDH 600	1									1
DIODE CD-8434			150			1	1			
2N3724			16							
2N4123						1			2	1
2N4125						1		1		2
NE510A						1		1		1
SH6405*			10							
T1496**			16							
9009H/8859H***			1							
XTAL 10 MC	1									
XTAL 14.08 KC										
XTAL 16 KC										
XFMR "B"			16							
XFMR 3:1			16							
XFMR 1:1			8							

* QUAD Transistor
** Transipads (Sealectro)
***Selected IC

TABLE

COMPONENT LIST-POWER SUPPLY, CONSOLE

COMPONENT	PWR SUPP	CONSOLE	RES BRD	PTP PWR CNTL
.1 ohm 2W 1% (OMI T2C)	2			
1 " 3W 5% (SPRAGUE 242E-IR05)	1			
10 " ¼W "	1			1
17.5 " " 1% (Dale SPR-275)			20	
47 " " 5%	2			
75 " ¼W "	1			
82 " " "	1			
100 " " "	3			2
150 " " "		47		
180 " 2W "	2			
220 " ¼W "	5			
270 " " "	1			
330 " " "	2			
330 " 3W "	3			
390 " ¼W "	1			
470 " " "	1			
560 " " "	3			
600 " 3W "	1			
750 " ¼W "	4			
1K " " "	3			
1.5K " " "	7			
1.8K " " "	3			
2K " " "	1			
2.2K " " "	5			
2.7K " " "	5			
3K " " "	1	48		
3.3K " " "	13			
3.9K " " "	1			
4.7K " " "	5			
5.6K " " "	4			
8.2K " " "	3			
10K " " "	1			
12K " " "	1			
15K " " "	2			
22K " " "	1			
2K(POT) BOURNS #3005P-1-202	2			
.0022 MFD (ERIE)			4	
.01 MFD 50v				1
470 PF				1
6.8 MFD 35v		1		
8MFD 50v (SPRAGUE 6747HP)			2	
50 MFD 50v (SPRAGUE 8908HA)			13	
BULB 28v (HUDSON 2187D)		47		
SWITCH ON/OFF (C and K 7101-PC)		16		
SWITCH ON/OFF (C and K 7105-PC)		5		
SWITCH DPDT (C and K 7205-PC)		4		
SWITCH MICRO (J321D8)		1		
SWITCH MICRO (J3223D8)		2		

TABLE

COMPONENT LIST-POWER SUPPLY, CONSOLE

COMPONENT	PWR SUPP	CONSOLE	RES BRD	PTP PWR CNTL
2N3715	3			
2N4123	2			
2N4125	5			
2N4441	1			
2N4918	2			
2N5301	1			
SC45B (TRIAC)				1
DIODE 1N3879R	2			
" 1N5231	2			
" 1N5240	1			
" MDA-950-1	1			
" FDH600	6			1
" 1N4997	2			
" .5M5.1ZS1	1			
RELAY (BRSRI-901)				1
THERMISTOR (FENWAL KA1L1)	2			
FAN,AX1D1 (PAMOTOR #8500)	2			
DIODE BRIDGE (MDA 962-1)	1			
CKT BKR (AIRPAX #6915)	1			
TRANSFORMER (TRIAD F-60U)	1			
" (TRIAD F-109U)	1			
CHOKE (FERROXCUBE 4229P-L00-387)	2			
CHOKE (FERROXCUBE 3622P-L00-3E)	2			
FUSE 10A	2			
CAP 21000 MFD 40v SPRAGUE	1			
" 32000 " 25v "	1			
" .1MFD 250 H-1PASS	2			
" 6000 MFD 10v SPRAGUE 36D	2			
.01 MFD 50v	1			

ILLUSTRATED

PARTS LIST

ILLUSTRATED PARTS LIST

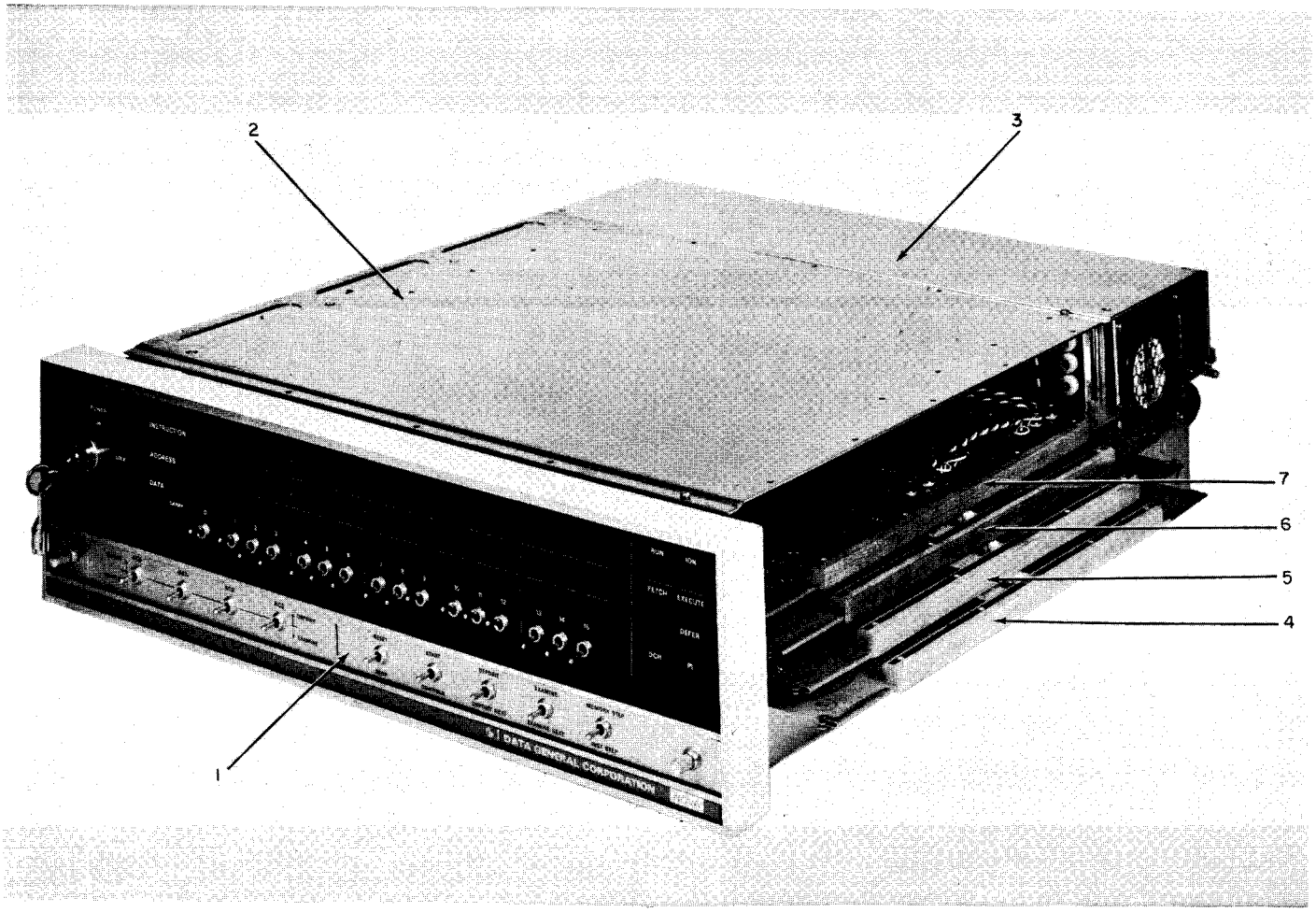


Figure 1 NOVA SYSTEM

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
1	005 000 036	CONSOLE	1	0010
2	005 000 040	CHASSIS	1	0010
3	005 000 020	POWER SUPPLY	1	0010
4	005 000 003	CENTRAL PROC.-1	1	0010
5	005 000 005	CENTRAL PROC.-2	1	0010
6	005 000 009	BASIC I/O Control	1	0010
7	005 000 006	4K MEMORY	1	0010

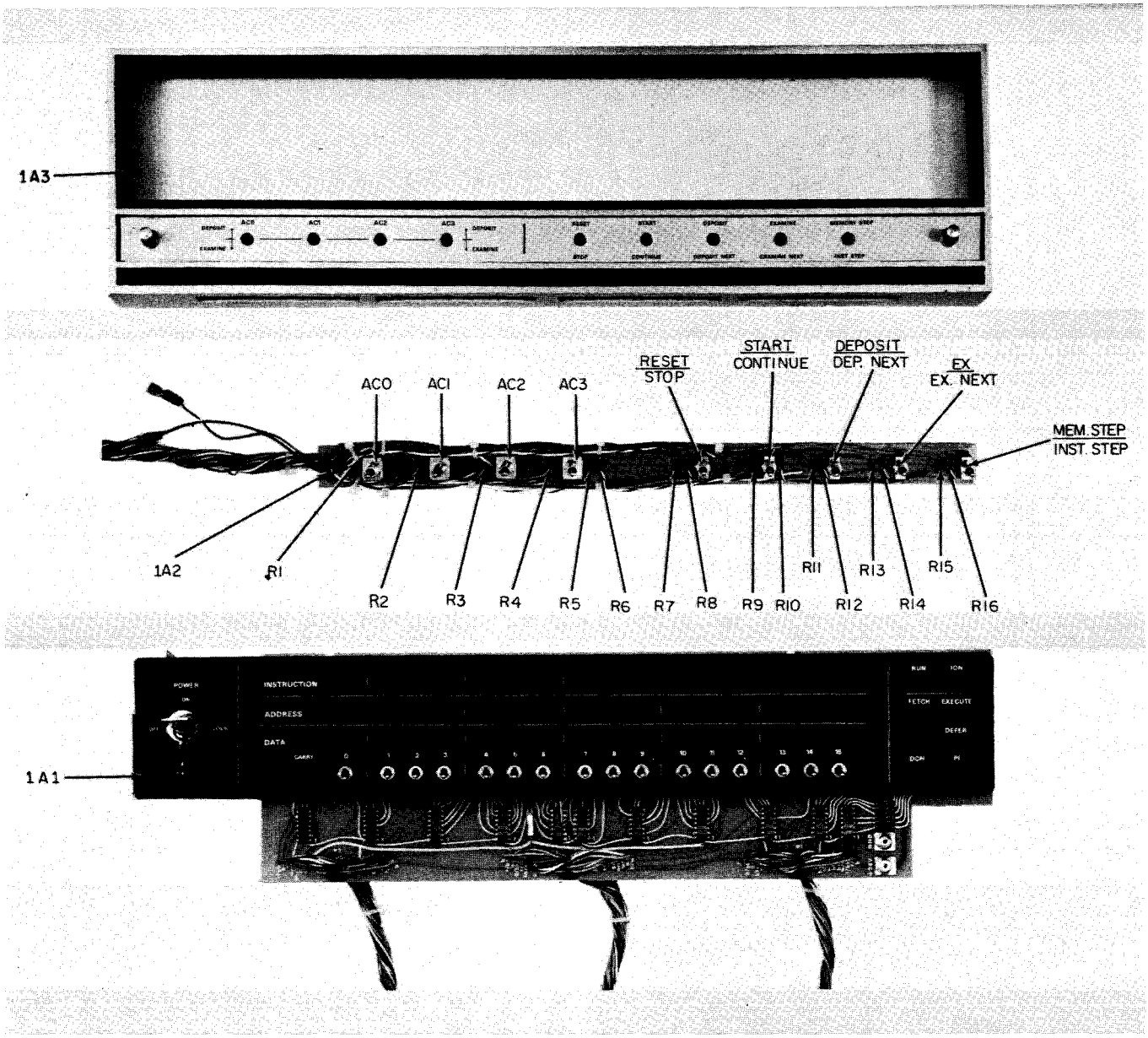


Figure 2-1 CONSOLE

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
1A1	005 000 033	CONSOLE #1 ASS'Y	1	0010
1A2	005 000 034	CONSOLE#2 ASS'Y	1	0010
1A3	005 000 035	CONSOLE CASTING ASS'Y	1	0010
ACCO thru ACC3	7205 PC	SWITCH, DPDT	4	0012
Reset/Stop, etc.	7105 PC	SWITCH, on/off/on	5	0012
Rl thru R16	CB1515	RESISTOR, 150Ω, 1/4W, +5%	16	0011

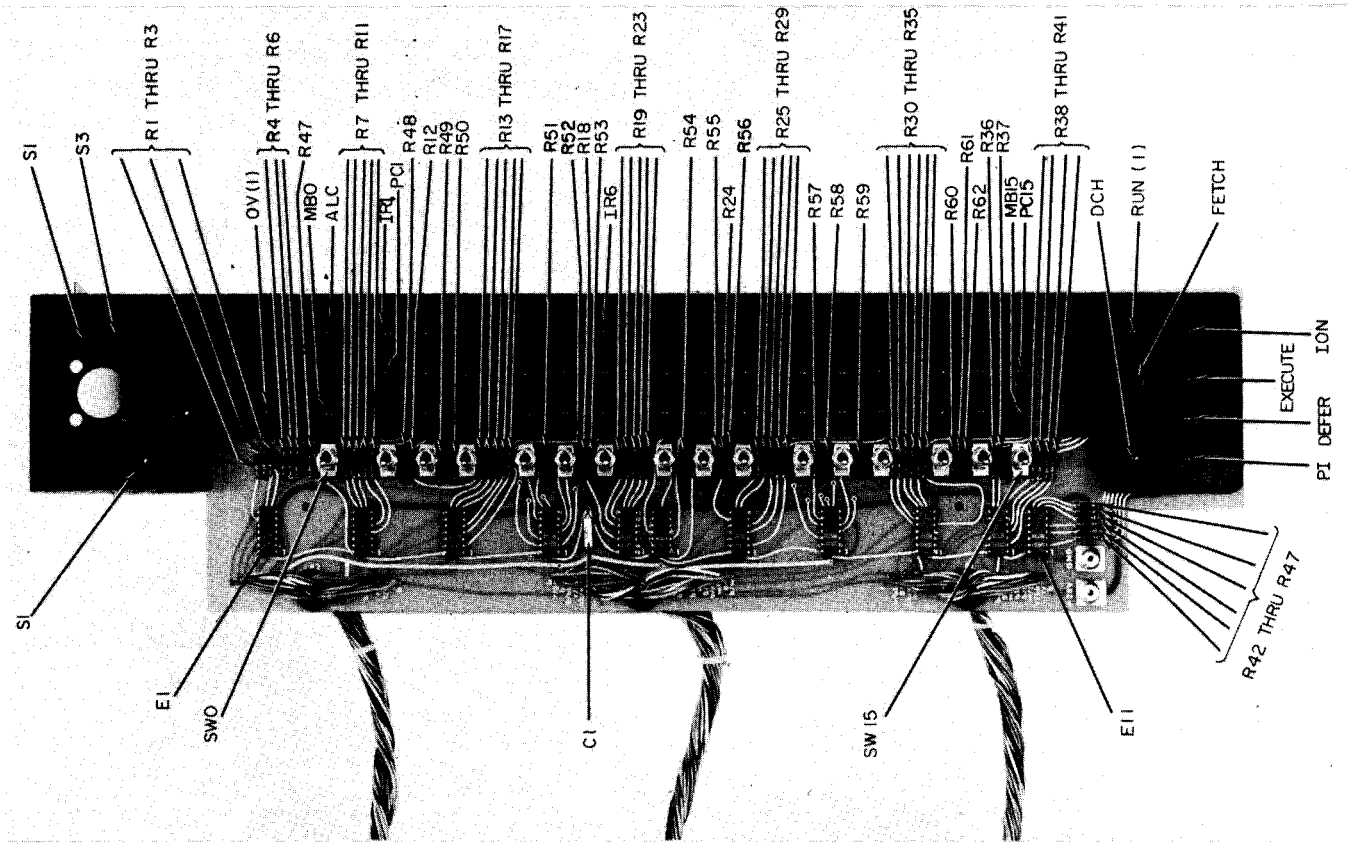


Figure 2-2 CONSOLE, # 1 ASSEMBLY

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
E1, E2, E3,) E5, E7, E9,) E10, E11)	8T90	DIP, Hex Inv. Int. Gate	8	0014
E4, E8	9004/8819*	DIP, Dual 4 Input Gate	2	0013/14
E6	9002/8889*	DIP, Quad 2 Input Gate	1	0013/14
R1 thru R47	CB1515	RESISTOR, 150Ω, 1/4W, +5%	47	0011
R47 thru R62	CB3025	RESISTOR, 3K, 1/4W, +5%	16	0011
OV1 thru PI	2187D	BULB, 28 volt	47	0016
C1	150D685X9035B2	CAPACITOR 6.8ufd, 35V	1	0015
SW0 thru SW15	7101 PC	SWITCH, on/off	16	0012
S1	J321D8	SWITCH, Micro	1	0017
S2, S3	J323D8	SWITCH, Micro	2	0017

* - alternate

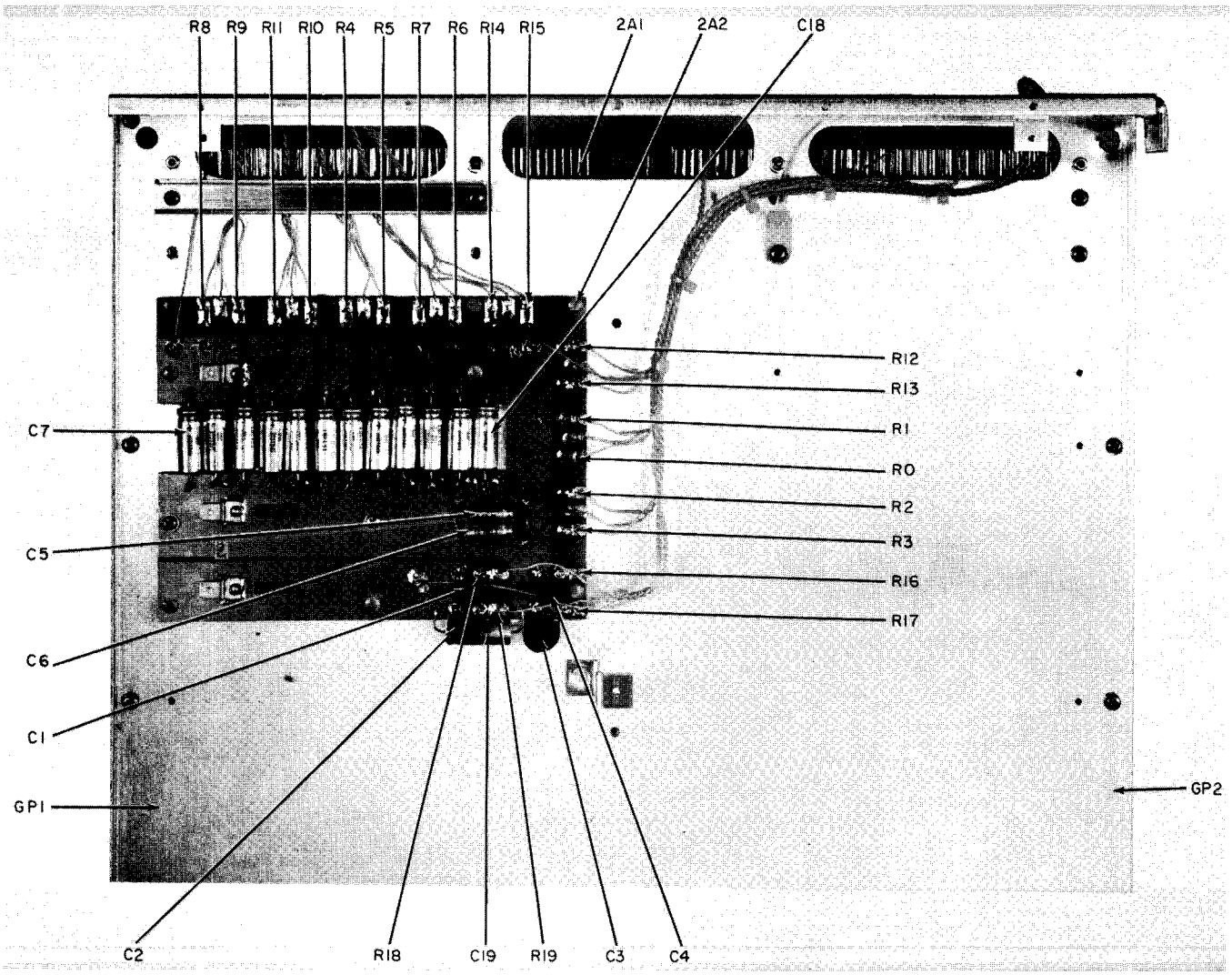


Figure 3-1 CHASSIS

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
2A1	005 000 041	CONN. FRAME ASS'Y	1	0010
2A2	005 000 042	RESISTOR BOARD ASS'Y	1	0010
R0 thru R19	SPR-275	RESISTOR, 17.5Ω, 1%	20	0018
C1 thru C4	XSFO-222K	CAPACITOR, .0022ufd	4	0019
C5, C6	6747HP	CAPACITOR, 8ufd, 50V	2	0015
C7 thru C19	6908HA	CAPACITOR, 50ufd, 50V	13	0015
GP1	002 000 014	GUIDE PLATE, rear	1	0010
GP2	002 000 016	GUIDE PLATE, front	1	0010

P1

O/BLK MB1ø	G/BLK OV1	R/BLK ION	W/BLK DCH	B PI(1)	O +5V	G PTG=2	R PTG=ø	W MB4	BLK MBø
R/G DEFER	B/R FETCH	O/R IR7	W/R ALC	BLK/R Run(1)	B/W +5V	G/W PC8	R/W MB1	BLK/W MB9	B/BLK PC12

P2

O/BLK IR5	G/BLK IR6	R/BLK Execute	W/BLK +5V	B PRG=1	O GND	G PC5	R PC9	W PC1	BLK MB6
R/G PC6	B/R PC1ø	O/R PC14	W/R PC2	BLK/R MB2	B/W BND	G/W PC13	R/W MB5	BLK/W MBR	B/BLK PC4

P3

O/BLK IR3	G/BLK JR2	R/BLK IR1	W/BLK IR4	B MB3	O HB14	G MB7	R MB11	W PC15	BLK PC7
R/G CSø	B/R CS1	O/R CS2	W/R CS3	BLK/R MB12	B/W MB13	G/W MB15	R/W PTG=3	BLK/W PC3	B/BLK PC11

P4

$\overline{\text{O/BLK}}$ $\overline{\text{ISTP}}$	$\overline{\text{G/BLK}}$ $\overline{\text{EXN}}$	$\overline{\text{R/BLK}}$ $\overline{\text{DPN}}$	$\overline{\text{W/BLK}}$ $\overline{\text{DP}}$	$\overline{\text{B}}$ $\overline{\text{EX}}$	$\overline{\text{O}}$ $\overline{\text{ACC3}}$	$\overline{\text{G}}$ $\overline{\text{ACC1}}$	$\overline{\text{R}}$ $\overline{\text{ACCø}}$	$\overline{\text{W}}$ $\overline{\text{ACC2}}$	BLK GND
$\overline{\text{R/G}}$ $\overline{\text{CONT}}$	$\overline{\text{B/R}}$ $\overline{\text{ACEX}}$	$\overline{\text{O/R}}$ $\overline{\text{ST}}$	$\overline{\text{W/R}}$ $\overline{\text{STOP}}$	$\overline{\text{BLK/R}}$ $\overline{\text{MSTP}}$	$\overline{\text{B/W}}$ $\overline{\text{ACDP}}$	$\overline{\text{G/W}}$ $\overline{\text{Acc.ENB}}$	$\overline{\text{R/W}}$ $\overline{\text{RST}}$	$\overline{\text{BLK/W}}$ $\overline{\text{Restart ENB}}$	B/BLK +5V

Figure 3-2 BACK PANEL CONNECTOR DIAGRAM

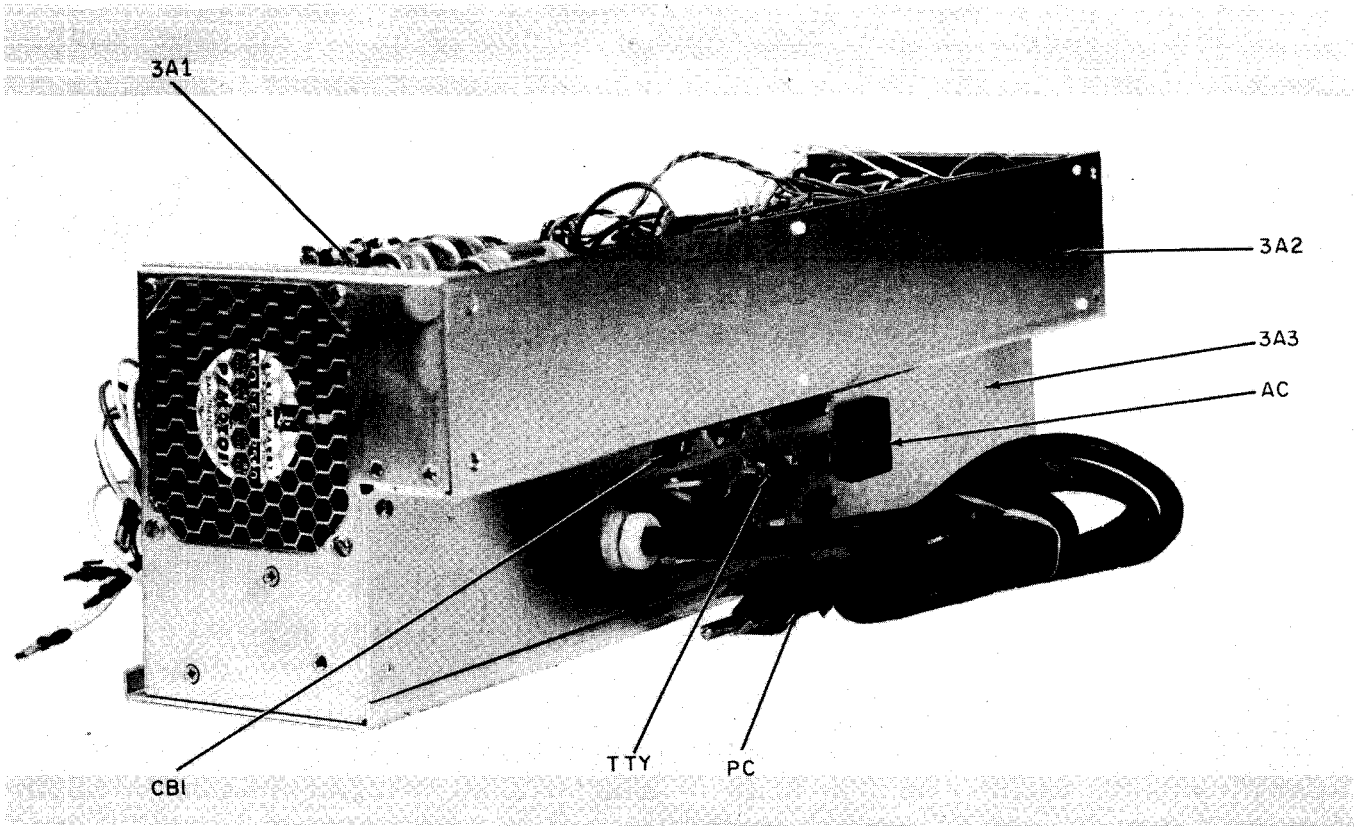


Figure 4-1 POWER SUPPLY

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
3A1	005 000 017	CHASSIS ASS'Y	1	0010
3A2	005 000 018	REAR PANEL ASS'Y	1	0010
CB1	6915	CIRCUIT BREAKER	1	0020
3A3	005 000 019	CONN. PLATE ASS'Y	1	0010
PC	17406S	POWER CORD	1	0021
TTY	DEC 9S	CONN. SOCKET, 9 Pin	1	0022
AC	1369	CONN., AC Outlet	1	0023

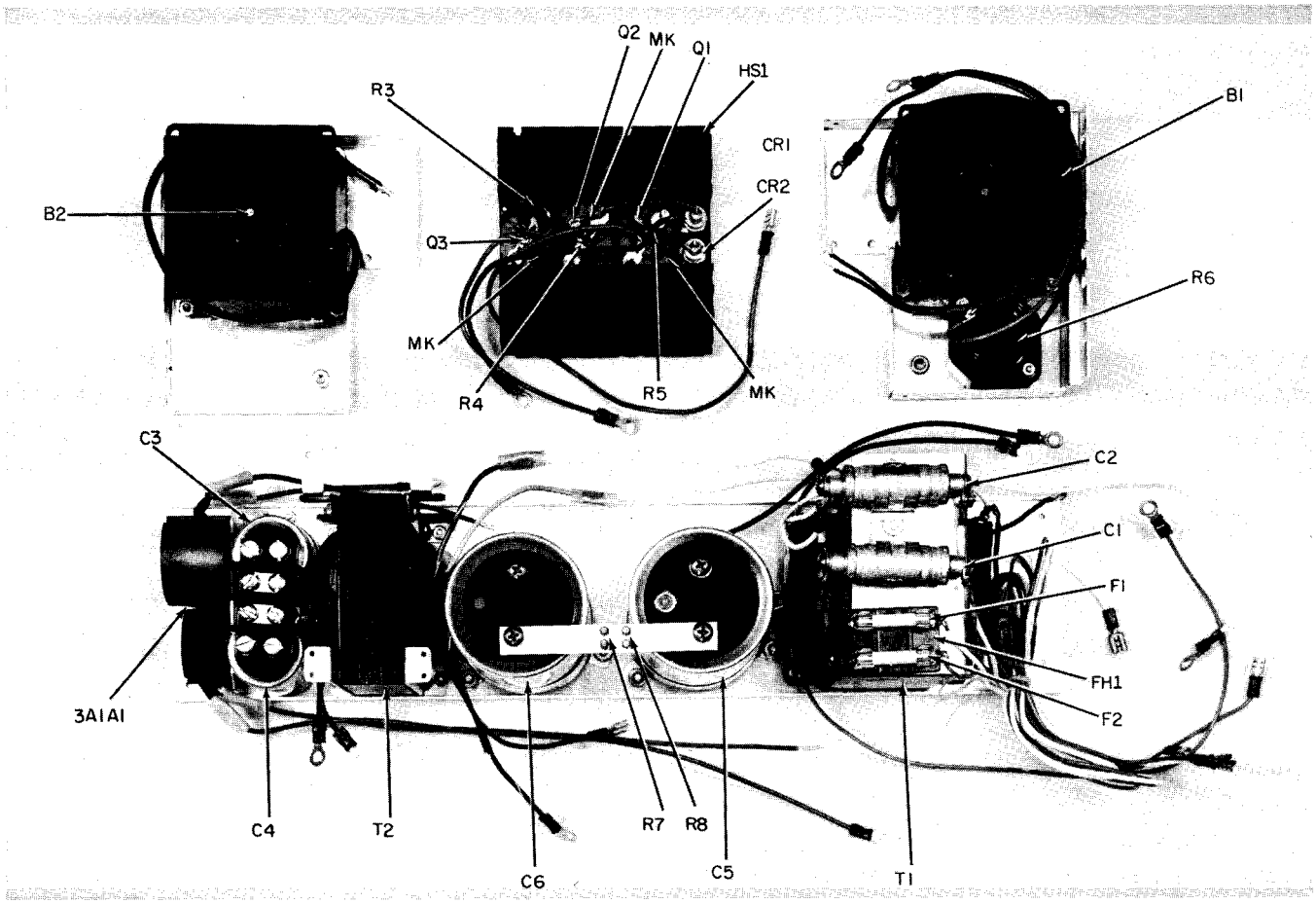


Figure 4-2 POWER SUPPLY CHASSIS ASSEMBLY

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
T1	F109H	TRANSFORMER	1	0024
FH1	3823-2	FUSEHOLDER	1	0025
F1, F2	314010	FUSE, 3AB 10A	2	0025
C1, C2	48P9	CAPACITOR, .1ufd, 250 VAC	2	0015
T2	F60U	TRANSFORMER	1	0024
C3, C4	36D602G010AA2A	CAPACITOR, 6000ufd, 10V	2	0015
HS1	002 000 056	HEAT SINK	1	0010
Q1	2N5301	TRANSISTOR	1	0026
Q2, Q3	2N3715	TRANSISTOR	2	0026
CR1, CR2	1N3879R	DIODE	2	0026
MK	MK-20	MOUNTING KIT, Xsistor	3	0026
R3	OM1T2C	RESISTOR, .1Ω, 2W, 1%	1	0027
R4	CB1015	RESISTOR, 100Ω, 1/4W, 5%	1	0011
R5	CB4705	RESISTOR, 47Ω, 1/4W, 5%	1	0011
3A1A1	005 000 025	CHOKE ASS'Y	1	0010
B1, B2	8500	FAN, Axial	2	0029
R6	MDA 962-1	DIODE BRIDGE	1	0026
R7, R8	KA1L1	THERMISTOR	2	0028
C5	36D213G040CC2A	CAPACITOR, 21,000ufd, 40V	1	0015
C6	36D323G025CC2A	CAPACITOR, 32,000ufd, 25V	1	0015
3A1A1	005 000 025	CHOKE ASS'Y	1	0010

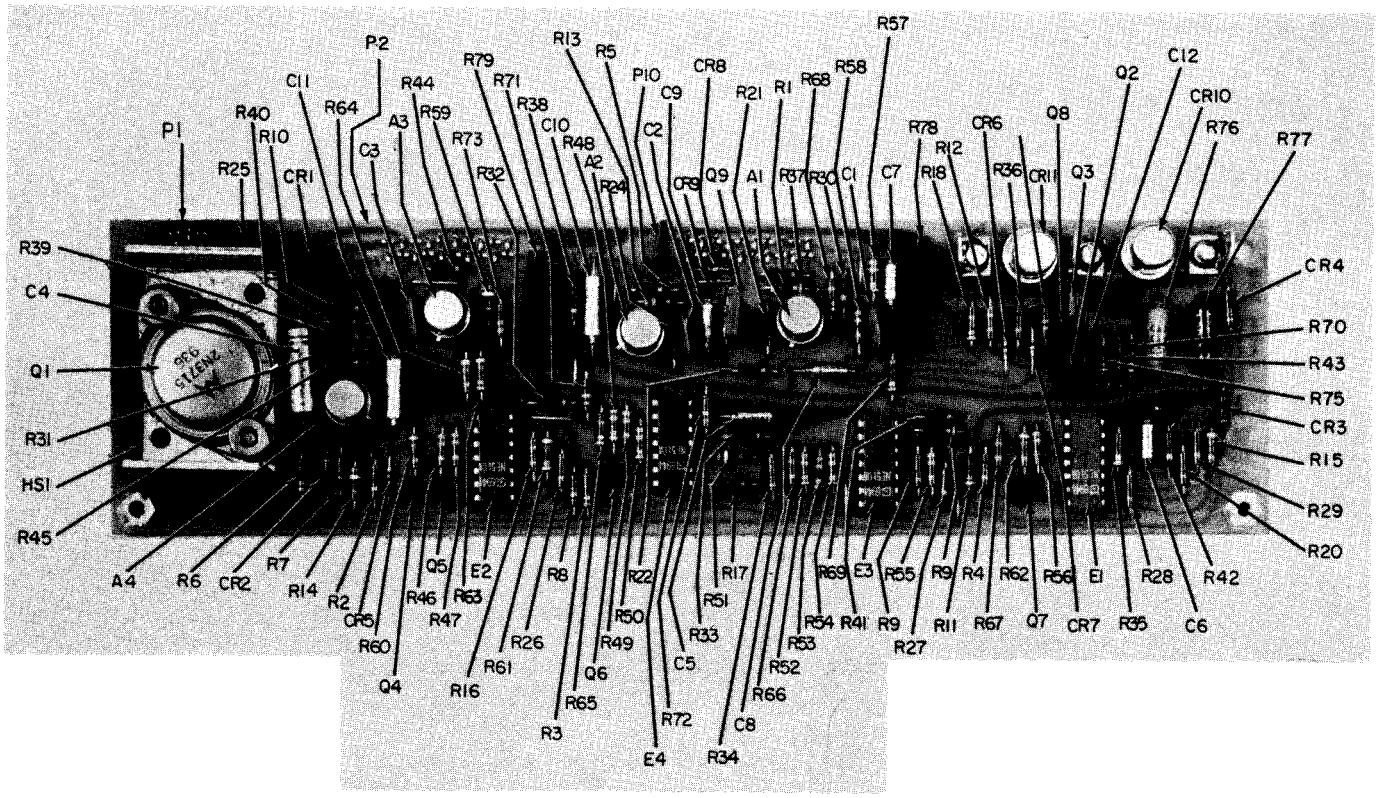


Figure 4-3 POWER SUPPLY REGULATOR ASSEMBLY

P1

1	+5 OK	60 ~	-5V
4	PWR FAIL	MEM OK	-5V

P2

1	Y	R/Y	GND				+V MEM GND			
11	6K CAP			THERM +V MEM	+30	+V MEM BASE	THERM GND		+V MEM	+V MEM EMIT.

P3

1	+5V BASE									THERM +V INH
11		+5V	GND +5V	SWITCH +30		+V INH BASE		THERM +V INH	GND +V INH	+V INH

Figure 4-3 POWER SUPPLY REGULATOR ASSEMBLY

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
R1	CB4705	RESISTOR, 47Ω, 1/4W 5%	1	0011
R2	CB7505	RESISTOR, 75Ω, 1/4W 5%	1	0011
R3	CB8205	RESISTOR, 82Ω, 1/4W 5%	1	0011
R4, R5	CB1015	RESISTOR, 100Ω, 1/4W 5%	2	0011
R6 thru R10	CB2215	RESISTOR, 220Ω, 1/4W 5%	5	0011
R11	CB2715	RESISTOR, 270Ω, 1/4W 5%	1	0011
R12, R13	CB3315	RESISTOR, 330Ω, 1/4W 5%	2	0011
R14	CB3915	RESISTOR, 390Ω, 1/4W 5%	1	0011
R15	CB4715	RESISTOR, 470Ω, 1/4W 5%	1	0011
R16 thru R18	CB5615	RESISTOR, 560Ω, 1/4W 5%	3	0011
R19 thru R21	CB7515	RESISTOR, 750Ω, 1/4W 5%	3	0011
R22 thru R24	CB1025	RESISTOR, 1K, 1/4W 5%	3	0011
R25 thru R31	CB1525	RESISTOR, 1.5K, 1/4W 5%	7	0011
R32 thru R34	CB1825	RESISTOR, 1.8K, 1/4W 5%	3	0011
R35	CB2025	RESISTOR, 2K, 1/4W 5%	1	0011
R36 thru R40	CB2225	RESISTOR, 2.2K, 1/4W 5%	5	0011
R41 thru R45	CB2725	RESISTOR, 2.7K, 1/4W 5%	5	0011
R46 thru R58	CB3325	RESISTOR, 3.3K, 1/4W 5%	13	0011
R59	CB3925	RESISTOR, 3.9K, 1/4W 5%	1	0011
R60 thru R64	CB4725	RESISTOR, 4.7K, 1/4W 5%	5	0011
R65 thru R68	CB5625	RESISTOR, 5.6K, 1/4W 5%	4	0011
R69	CB8225	RESISTOR, 8.2K, 1/4W 5%	1	0011
R70	CB1035	RESISTOR, 10K, 1/4W 5%	1	0011
R71	CB1235	RESISTOR, 12K, 1/4W 5%	1	0011
R72, R73	CB1535	RESISTOR, 15K,1/4W 5%	2	0011
R74	CB2235	RESISTOR, 22K, 1/4W 5%	1	0011
R75	CB3025	RESISTOR, 3K, 1/4W 5%	1	0011
R76	2736	RESISTOR, 330Ω, 3W 5%	1	0030
R77	2742	RESISTOR, 600Ω, 3W, 5%	1	0030
R78, R79	3005P-1-202	POTENTIOMETER, 2K	2	0031
E1 thru E4	NE510A	DIP, Dual Ampl.	4	0014
A1 thru A4	uA723	DIP, Prec. Volt. Reg.	4	0013
Q1	2N3715	BRANSISTOR	1	0026
Q2, Q3	2N4123	TRANSISTOR	2	0026
Q4 thru Q8	2N4125	TRANSISTOR	5	0026
Q9, Q10	2N4918	TRANSISTOR	2	0026
CR1	MDA 950-1	DIODE	1	0026
CR2	1N5231	DIODE	1	0026
CR3	1N2864	DIODE	1	0026
CR4	1N5240	DIODE	1	0026
CR5 thru CR9	CD8434	DIODE	5	0034
CR10, CR11	1N4997	DIODE	2	0026
C1 thru C3	CK103	CAPACITOR, .01ufd, 50V	3	0032
C4	150D476X9020R2	CAPACITOR, 47ufd, 20V	1	0015
C5 thru C9	150D224X9035A2	CAPACITOR, .22ufd, 35V	5	0015
C10, C11	150D685X9035B2	CAPACITOR, 6.8ufd, 35V	1	0015
C12	X5FO 222K	CAPACITOR, 2200PFD	1	0019
HS1	NC631-3	HEAT SINK	1	0033

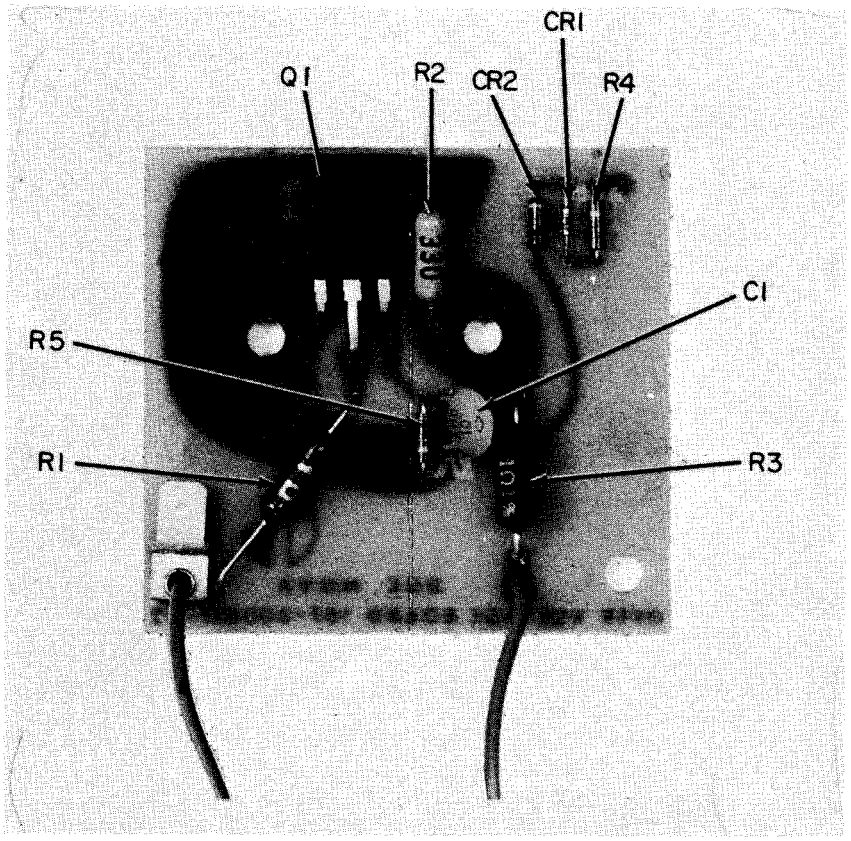


Figure 4-4 POWER SUPPLY OVERVOLTAGE ASSEMBLY

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
R1	242E-1ROS	RESISTOR, 1Ω, 3W, 5%	1	0015
R2	2736	RESISTOR, 330Ω, 3W 5%	1	0030
R3	OMIT2C	RESISTOR, .1Ω, 2W 1%	1	0027
R4	CB1005	RESISTOR, 10Ω, 1/4W 5%	1	0011
R5	CB7515	RESISTOR, 750Ω, 1/4W 5%	1	0011
C1	CK103	CAPACITOR, .01ufd, 50V	1	0032
Q1	2N4441	TRANSISTOR	1	0026
CR1	CD8434	DIODE	1	0034
CR2	1N5231	DIODE	1	0026

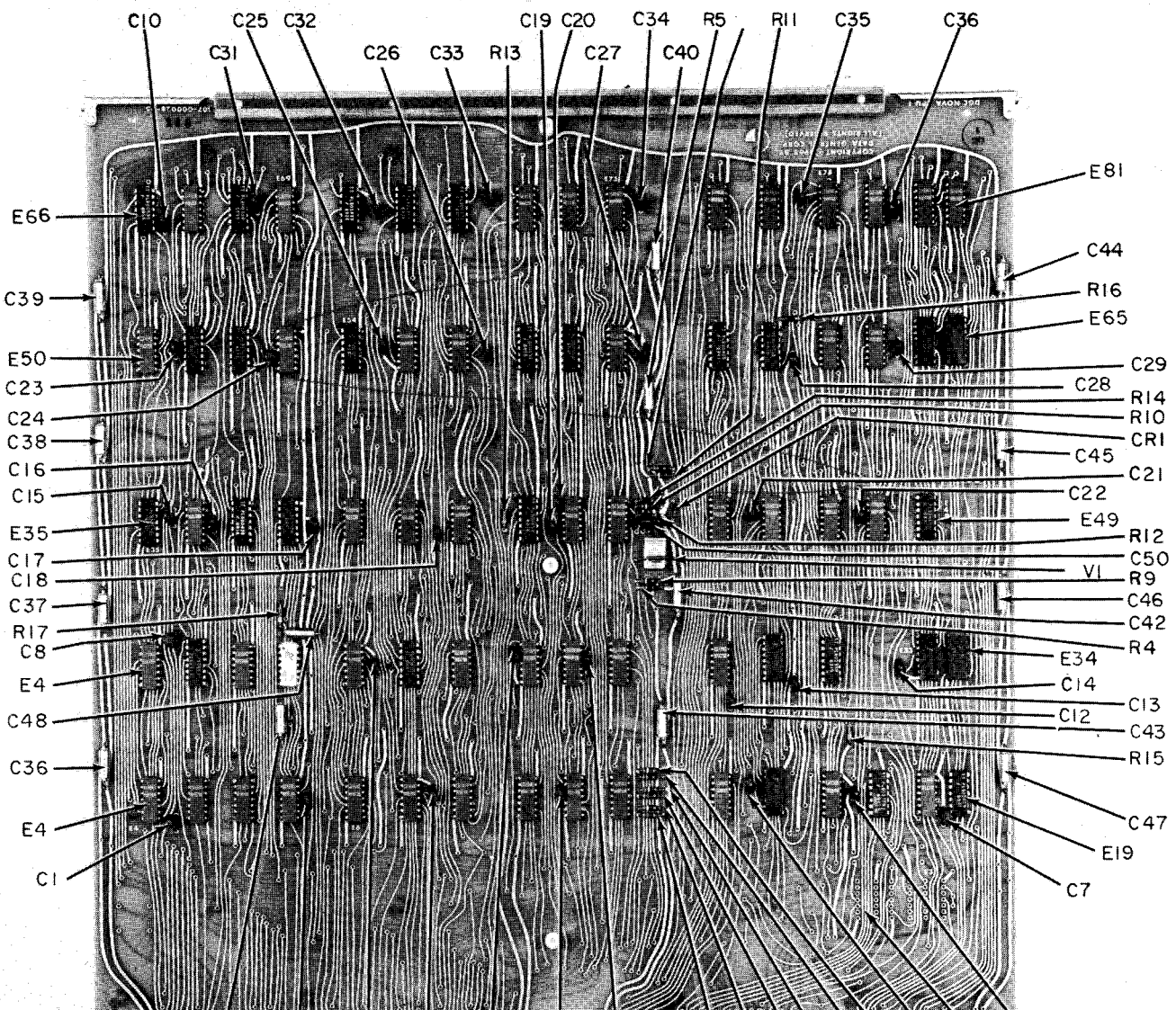

C10
C25
C32
C31
C26
C33
R13
C19
C20
C27
C34
C40
R5
R11
C35
C36
E81
E66
C44
C39
R16
E65
E50
C29
C23
C28
C24
R14
R10
C38
CR1
C16
C45
C15
C21
C22
E35
E49
C17
R12
C18
C50
V1
R9
C37
C46
R17
C42
C8
R4
E34
E4
C14
C13
C48
C12
C43
C36
R15
E4
C47
E19
C1
C7

Figure 5 CENTRAL PROCESSOR 1

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
E9, E12, E20, E22, E39, E40, E43, E45, E50, E53, E59, E73, E74, E79, E81	9002/8889*	DIP, Quad 2 Input Gate	15	0013/14
E25, E35, E38, E42, E49, E51, E52, E54, E58, E71, E72	9003/8879*	DIP, Triple 3 Input Gate	11	0013/14
E8, E11, E30, E37, E47, E70	9004/8819*	DIP, Dual 4 Input Gate	6	0013/14
E28, E32, E57, E61, E66, E68, E76	9005/8840*	DIP, Dual 2 Wide AOI	7	0013/14
E17	9007	Single 8 Input Gate	1	0013
E16, E27, E46, E56, E62, E63, E67, E77	9007/8848*	Single 4 Wide AOI	8	0013/14
E4, E13, E14, E24, E36, E41, E55, E69, E75, E78, E80	9016/8H90*	Hex Inverter	11	0013/14
E15, E31, E33, E34	9022	Dual JK Flip-Flop	4	0013
E21, E64, E65	9300	MSI 4 Bit Univ. Reg.	3	0013
E2, E5 thru E7, E10, E26	7474/8828*	D-Flop	6	
E1, E44	8881	2 Input NAND (OC)	2	0014
E29	8880	Quad 2 Input NAND Gate	1	0014
E23	SG83	ONE SHOT	1	0035
E18, E19, E60	9009/8859*	BUFFER	3	0013/14
R1 thru R5	CB3315	RESISTOR, 330Ω, 1/4W 5%	5	0011
R6 thru R11	CB3915	RESISTOR, 390Ω, 1/4W 5%	6	0011
R12, R13	CB2215	RESISTOR, 220Ω, 1/4W 5%	2	0011
R14	CB1015	RESISTOR, 100Ω, 1/4W 5%	1	0011
R15, R16	CB1525	RESISTOR, 1.5K, 1/4W 5%	2	0011
R17	CB8225	RESISTOR, 8.2K, 1/4W 5%	1	0011
C1 thru C35	Y5FO-503M	CAPACITOR, .05ufd, 50V	35	0019
C36 thru C49	150D685X9035B2	CAPACITOR, 6.8ufd, 35V	14	0015
C50	CD7FA122J	CAPACITOR, 1200pFd	1	0036
V1	N/A	CRYSTAL, 10MC	1	0037
CR1	CD8434	DIODE	1	0034

*alternate

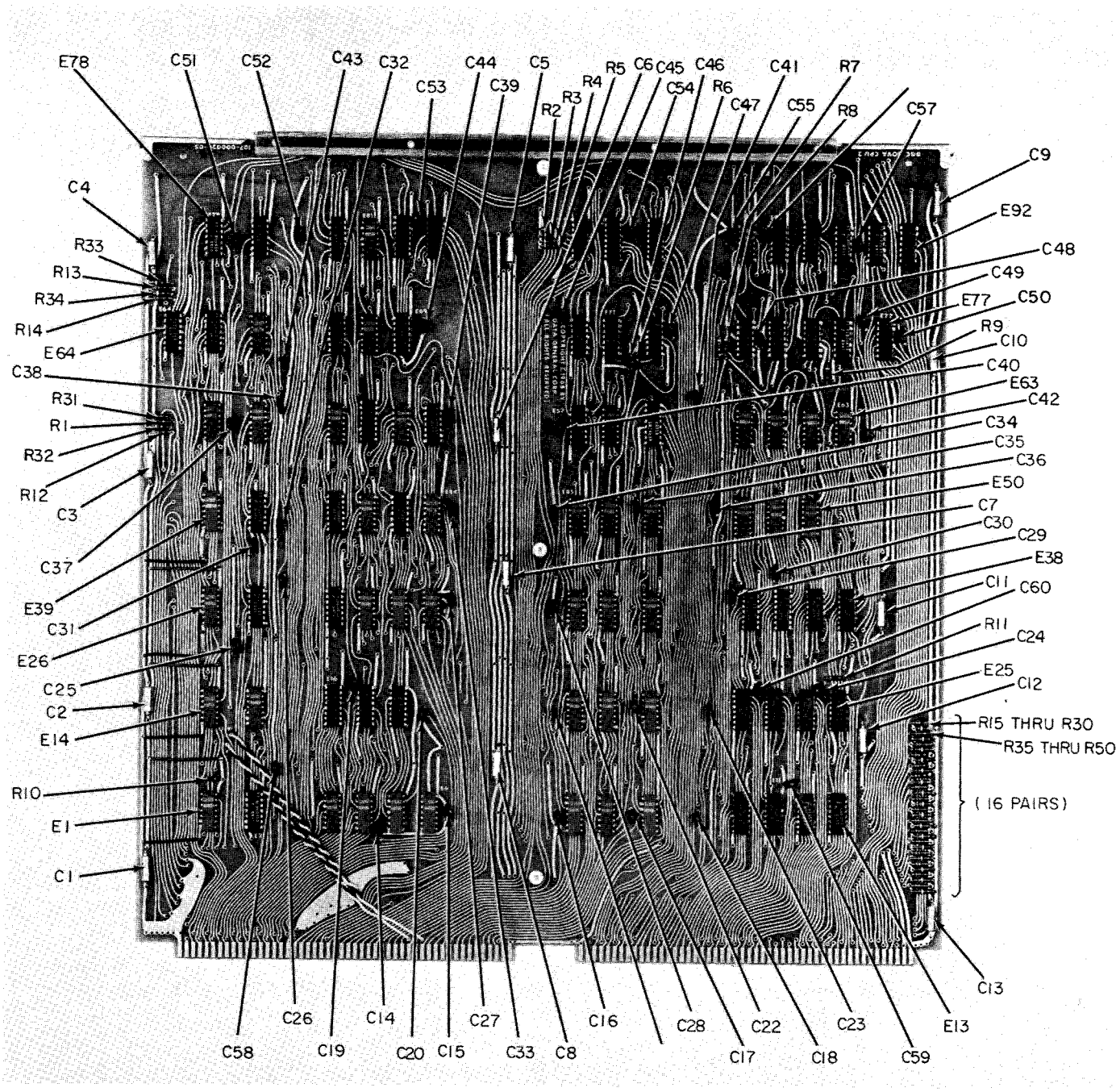


Figure 6 CENTRAL PROCESSOR 2

Figure 6 CENTRAL PROCESSOR 2

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
E27, E40, E43, E57, E64, E69, E70, E79	9002/8889*	DIP, Quad 2 Input Gate	8	0013/14
E65, E66, E80	9003/8879*	DIP, Triple 3 Input Gate	3	0013/14
E44, E78	9004/8819*	DIP, Dual 4 Input Gate	2	0013/14
E28, E41, E56, E67	9005/8840*	DIP, Dual 2 Wide AOI Gate	4	0013/14
E2	9007	DIP, Single 8 Input Gate	1	0013
E7 thru E9, E19 thru E21 E29, E31 thru E34, E45 thru E47, E53	9008/8848*	DIP, Single 4 Wide AOI Gate	15	0013/14
E76, E87, E88, E90, E91	9009/8859*	DIP, Dual 4 Input Buffer	5	0013/14
E3 thru E6, E15, E42, E48 thru E50, E52, E55, E58, E71, E77, E81, E92	9016/8H90*	DIP, Hex Inverter	16	0013/14
E10 thru E13, E22 thru E25, E35 thru E38, E83, E84	9300	DIP, MSI 4 Bit Univ. Reg.	14	0013
E16 thru E18, E54, E82, E85, E86, E89	9301	DIP, MSI 1 of 10 Decoder	8	0013
E72 thru E75	5033	DIP, MSI	4	0013
E30, E68	7474/8828*	DIP, Dual D Binary	2	0038/14
E51, E60 thru E63	8881	DIP, 2 Input NAND (OC)	5	0014
E1, E14, E26, E39	8880	DIP, Quad 2 Input NAND Gate	4	0014
E59	7483	DIP, 4 Bit Adder	1	0038
R1	CB1015	RESISTOR, 100Ω, 1/4W 5%	1	0011
R2 thru R9	CB4715	RESISTOR, 470Ω, 1/4W 5%	8	0011
R10, R11	CB3025	RESISTOR, 3K, 1/4W 5%	2	0011
R12 thru R30	CB3315	RESISTOR, 330Ω, 1/4W 5%	19	0011
R31 thru R50	CB3915	RESISTOR, 390Ω, 1/4W 5%	20	0011
C1 thru C13	150D685X9035B2	CAPACITOR, 6.8ufd, 35V	13	0015
C14 thru C61	Y5FO-503M	CAPACITOR, .05ufd, 50V	48	0019

*alternate

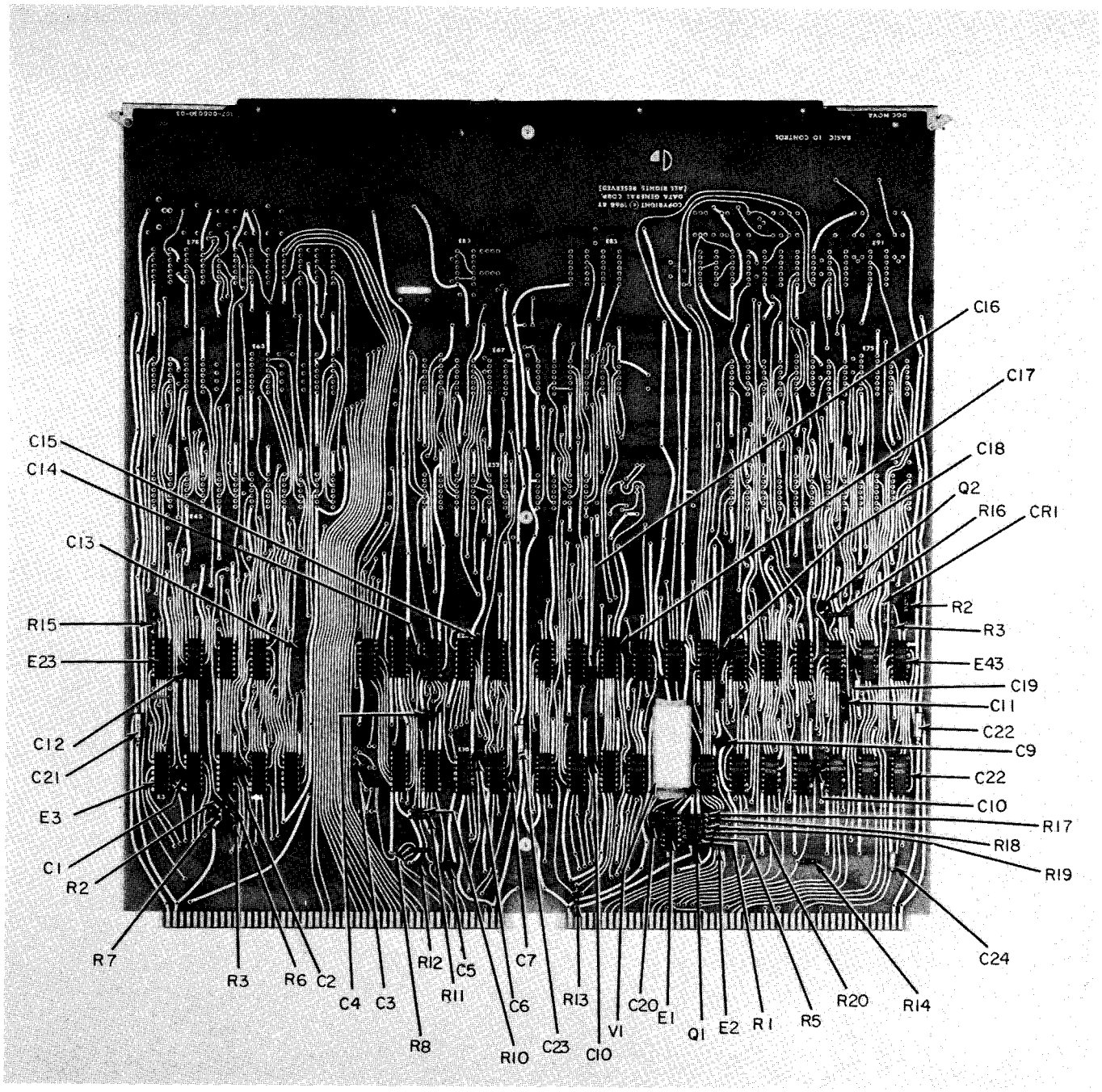


Figure 7-1 I/O Board with TTY Option

Figure 7-1 I/O BOARD WITH TTY OPTION

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
E24, E31, E38, E41 thru E43	9002/8889*	DIP, Quad 2 Input Gate	6	0013/14
E23, E40	9003/8879*	DIP, Triple 3 Input Gate	2	0013/14
E10, E33	9004/8819*	DIP, Dual 4 Input Gate	2	0013/14
E30	9007	DIP, Single 8 Input Gate	1	0013
E3 thru E7, E25, E27, E32, E39	9016/8H90*	DIP, Hex Inverter	9	0013/14
E8, E9, E14, E28, E34	9300	DIP, MSI 4 Bit Univ. Reg.	5	0013
E16 thru E22 E35 thru E37	8828	DIP, Dual D Binary	10	0014
E2	8281	DIP, Binary Counter	1	0014
E1	NE510A	DIP, Dual Ampl.	1	0014
E11, thru E13 E15, E26	8881	DIP, 2 Input NAND (OC)	5	0014
E29	8T80	DIP	1	0014
R1	CB2215	RESISTOR, 220Ω, 1/4W 5%	1	0011
R2		RESISTOR, 470Ω, 2W 5%	1	
R3	CB4725	RESISTOR, 4.7K 1/4W 5%	1	0011
R5	CB1815	RESISTOR, 180Ω, 1/4W 5%	1	0011
R6, R7	CB3915	RESISTOR, 390Ω, 1/4W 5%	2	0011
R8, R9	CB1025	RESISTOR, 1K, 1/4W 5%	2	0011
R10 thru R16	CB3025	RESISTOR, 3K, 1/4W 5%	7	0011
R17 thru R20	CB3325	RESISTOR, 3.3K, 1/4W 5%	4	0011
C1 thru C19	Y5FO-503M	CAPACITOR, .05ufd, 50V	19	0019
C20	CD7FA471J	CAPACITOR, 470pFd	1	0036
C21 thru C23	150D685X9035B2	CAPACITOR, 6.8ufd 35V	3	0015
C24	150D105X9035A2	CAPACITOR, 1ufd 35V	1	0015
CR1	CD8434	DIODE	1	0034
Q1	2N4125	TRANSISTOR	1	0026
V1	N/A	CRYSTAL, 14.08 KC	1	037
Q2	2N4123	TRANSISTOR	1	0026

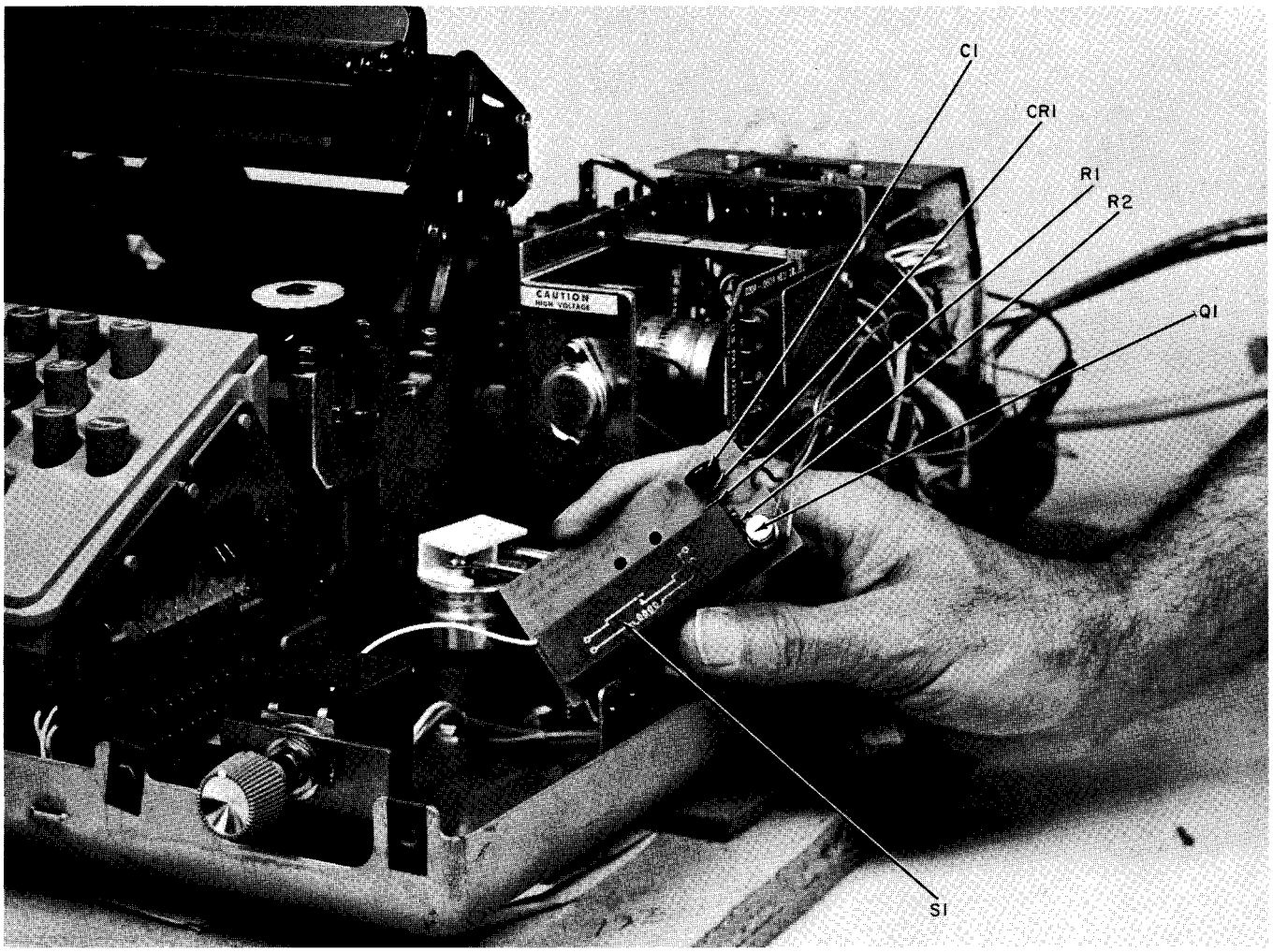


Figure 7-2 TTY Modification

Circuit Reference	Part #	Description	Qty. Per. Assembly	Mfr.
R1	CB1005	RESISTOR, 10Ω, 1/4W 5%	1	0011
R2	CB1015	RESISTOR, 100Ω, 1/4W 5%	1	0011
CR1	CD8434	DIODE	1	0034
Q1	40526	TRIAC	1	0039
C1	CD7FA471J	CAPACITOR, 470 pFd	1	0036
S1	BRSR1-901	RELAY	1	0040

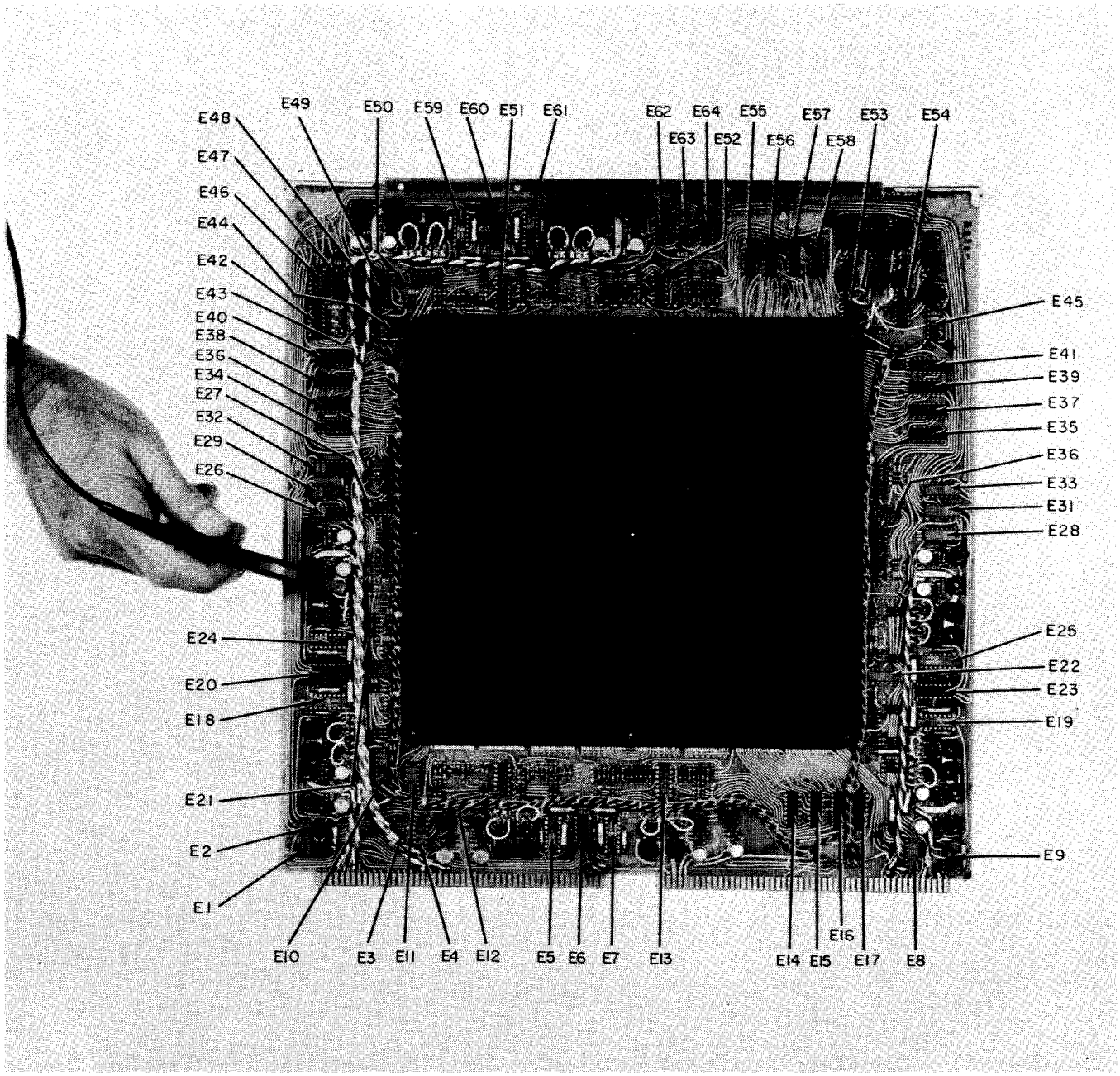
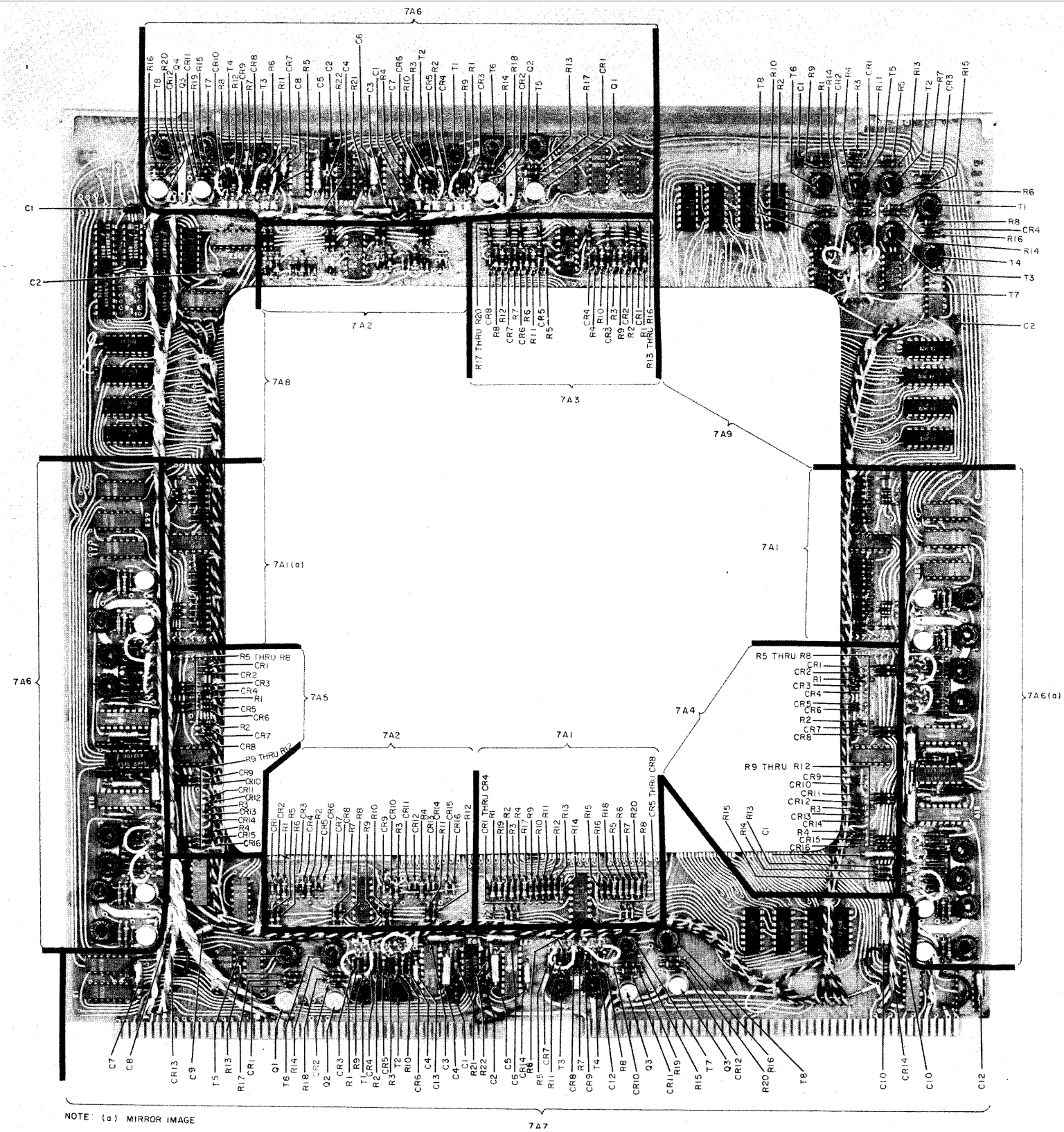


Figure 8-1 4K Core Memory Dip Locations

Figure 8-1 4K CORE MEMORY DIP LOCATIONS

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
E1, E2, E29, E31 thru E33, E63, E64	7474/8828*	DIP, Dual D Binary	8	0038/14
E3	8881	DIP, Quad 2 Input NAND (OC)	1	0014
E4, E26, E28, E62	8T80	DIP, Quad 2 Input NAND Int. Gate	4	0014
E5, E7, E18, E19, E24, E25, E59, E61	7525	DIP, 6 Bit Sense Amp	8	0038
E8 thru E11, E44, E50	8T90	DIP, Hex Inv. Int. Element	6	0014
E42	9004/8819*	DIP, Dual 4 Input Gate	1	0013/14
E6, E20, E23, E43, E48, E60	9016/8H90*	DIP, Hex Inverter	6	0013/14
E45	9002	DIP, Quad 2 Input Gate	1	0013/14
E46, E47	9009/8859*	DIP, Dual 4 Input Buffer	1	0013/14
E49	9301	MSI, 1 of 10 Decoder	1	0013
E12, E13, E21, E22, E27, E30, E51 thru E54	SH6405	DIP, PNP Xistor PAC	10	0013
E47	100 000 040	DIP Buffer	1	0010

*alternate


7A6
7A2
7A3
7A8
7A9
7A1
7A1(a)
7A5
7A4
7A6(a)
7A7
C1
C2
R5 THRU R8
CR1
CR2
CR3
CR4
R1
CR5
CR6
R2
CR7
CR8
R9 THRU R12
CR9
CR10
CR11
CR12
R3
CR13
CR14
R4
CR15
CR16
R13 THRU R16
R17 THRU R20
CR5 THRU CR8
CR1 THRU CR4
NOTE: (a) MIRROR IMAGE

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
7A1		MEMORY SUBASSEMBLY	3	0010
R1 thru R8	CB1515	RESISTOR, 1.5K, 1/4W 5%	8	0011
R9 thru R16	CB1025	RESISTOR, 1.0K, 1/4W 5%	8	0011
R17 thru R20	CB4725	TESISTOR, 4.7K, 1/4W 5%	4	0011
CR1 thru RC8	CD8434	DIODE	8	0034
7A2		MEMORY SUBASSEMBLY	2	0010
CR1 thru CR16	CD8434	DIODE	16	0034
R1 thru R4	CB4725	RESISTOR, 4.7K, 1/4W 5%	4	0011
R5 thru R12	CB1025	RESISTOR, 1.0K, 1/4W 5%	8	0011
7A3		MEMORY SUBASSEMLBY	1	0010
R1 thru R8	CB1525	RESISTOR, 1.5K, 1/4W 5%	8	0011
R9 thru R12	CB4725	RESISTOR, 4.7K, 1/4W 5%	4	0011
R13 thru R20	CB1025	RESISTOR, 1.0K, 1/4W 5%	8	0011
CR1 thru CR8	CD8434	DIODE	8	0034
7A4		MEMORY SUBASSEMBLY	1	0010
CR1 thru CR16	CD8434	DIODE	16	0034
R1 thru R4	CB4725	RESISTOR, 4.7K, 1/4W 5%	4	0011
R5 thru R12	CB1025	RESISTOR, 1.0K, 1/4W 5%	8	0011
R13, R14	CB6815	RESISTOR, 680Ω, 1/4W 5%	2	0011
R15	CB1525	RESISTOR, 1.5K, 1/4W 5%	1	0011
C1	150D685X9035B2	CAPACITOR, 6.8uFd, 35V	1	0015
7A5		MEMORY SUBASSEMBLY	1	0010
CR1 thru CR16	CD8434	DIODE	16	0034
R1 thru R4	CB4725	RESISTOR, 4.7K, 1/4W 5%	4	0011
R5 thru R16	CB1025	RESISTOR, 1.0K, 1/4W 5%	8	0011

Circuit Reference	Part #	Description	Qty. Per Assembly	Mfr.
7A6		MEMORY SUBASSEMBLY	3	0010
R1 thru R8	NC4(RN556)	RESISTOR, 150Ω, 1/8W 1%	8	0041
R9 thru R12	CB7505	RESISTOR, 75Ω, 1/4W 5%	4	0011
CR1 thru CR12	CD8434	DIODE	12	0034
R13 thru R16	CB5615	RESISTOR, 560Ω, 1/4W 5%	4	0011
R17 thru R20	CB4715	RESISTOR, 470Ω, 1/4W 5%	4	0011
C1, C2	CD7FC221J	CAPACITOR, 220 PFd	2	0036
C3 thru C6	150D685X9035B2	CAPACITOR, 6.8uFd, 35V	4	0015
C7, C8	150D685X9006A2	CAPACITOR, 6.8uFd, 6V	2	0015
R21	CB2225	RESISTOR, 2.2K, 1/4W 5%	1	0011
R22	CB1005	RESISTOR, 10Ω, 1/4W 5%	1	0011
Q1 thru Q4	2N3724	TRANSISTOR	4	0013
T1 thru T4	104 000 009	TRANSFORMER, Bifilar	4	0010
T5 thru R8	104 000 010	TRANSFORMER 3:1	4	0010
7A7		MEMORY SUBASSEMBLY	1	0010
R1 thru R8	NC4 (RN556)	RESISTOR, 150Ω, 1/8W 1%	8	0041
R9 thru R12	CB7505	RESISTOR, 75Ω, 1/4W 5%	4	0011
CR1 thru CR14	CD8434	DIODE	14	0034
R13 thru R16	CB5615	RESISTOR, 560Ω, 1/4W 5%	4	0011
R17 thru R20	CB4715	RESISTOR, 470Ω, 1/4W 5%	4	0011
C1, C2	CD7FL221J	CAPACITOR, 220PFd	2	0036
C3 thru C12	150D685X9035B2	CAPACITOR, 6.8uFd, 35V	10	0015
C13, C14	150D685X9006A2	CAPACITOR, 6.8uFd 6V	2	0015
R21	CB2225	RESISTOR, 2.2K, 1/4W 5%	1	0011
R22	CB1005	RESISTOR, 10Ω, 1/4W 5%	1	0011
Q1 thru Q4	2N3724	TRANSISTOR	4	0013
T1 thru T4	104 000 009	TRANSFORMER, Bifilar	4	0010
T5 thru T8	104 000 010	TRANSFORMER, 3:1	4	0010
7A8		MEMORY SUBASSEMBLY		0010
C1, C2	Y5FO-503M	CAPACITOR, .05uFd	2	0019
7A9		MEMORY SUBASSEMBLY	1	0010
C1, C2	Y5FO-503M	CAPACITOR, .05uFd	2	0019
R1 thru R8	CB4715	RESISTOR, 470Ω, 1/4W 5%	8	0011
R9 thru R16	CB1015	RESISTOR, 100Ω, 1/4W 5%	8	0011
CR1 thru CR4	CD8434	DIODE	4	0034
T1 thru T8	104 000 011	TRANSFORMER, 1:1	8	0010

ENGINEERING

DRAWINGS

ENGINEERING DRAWINGS

Number	Board	
1	IO	IO Bus Receivers and Common Select
3	IO	Real Time Clock
4	IO	Paper Tape Reader Control 4011
5	IO	Paper Tape Punch Control 4012
8		Console
11	CPU-1	Power Monitor
14-1	Memory	4K Memory Buffer and Flippers
14-2	Memory	4K Memory XY Drive
14-3	Memory	4K Memory Sense and Inhibit
15		Power Supply
16-1	Memory	2K Memory Buffer and Flippers
16-2	Memory	2K Memory XY Drive
16-3	Memory	2K Memory Sense and Inhibit
17		Flow Diagram
18		Timing Diagram
24		Back Panel
25	IO	Teletype Control
26-1	CPU-1	Timing, Major States and Manual Functions
26-2	CPU-1	Register Control
26-3	CPU-1	Memory Control and IO
27-1	CPU-2	Major Registers and Instruction Decoding
27-2	CPU-2	Accumulators and MA Decoding
27-3	CPU-2	Register Gating
27-4	CPU-2	IO Drivers, Skip and Interrupt Control
55		Installation