DataGeneral

Technical Reference

microNOVA INTEGRATED CIRCUITS

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microNOVA
INTEGRATED
CIRCUITS

PREFACE

This manual describes Data General's microNOVA line of integrated circuits. It provides technical specifications for these integrated circuits and functional descriptions of them. It also explains how they are connected to make a microcomputer system. For further information about the microNOVA computer system, see the Programmer's Reference Manual for the microNOVA Computer (DGC no. 015-000050) and the Technical Reference for the microNOVA Computer System (DGC no. 014-000073).

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SECTION I
microNOVA LINE OF INTEGRATED CIRCUITS

INTRODUCTION

Data General's microNOVA line of integrated circuits is a set of eight integrated circuits that includes a microprocessor, memories, peripheral controllers and supporting circuits required to form a microcomputer system. Although the circuits may be used independently, they have been designed to operate together and may be combined conveniently to form data processing elements that are commonly used in computer systems; e.g., a central processing unit, memory elements, etc. In particular, these data processing elements may be connected to compose a microNOVA computer system. The line includes the following circuits:

Integrated Circuit	Model Number
Microprocessor (CPU)	mN601
4K Dynamic RAM	mN606
I/O Controller (IOC)	mN603
Memory Transceiver	mN634
Address Driver	mN633
Sense Amp/Bus Driver	mN506
CPU I/O Transceiver	mN629
IOC I/O Transceiver	mN636

The CPU, the RAM and the IOC are the principal integrated circuits in the product line. They are all large-scale, N-channel, silicon-gate, metal-oxide, semi-conductor integrated circuits. Each of these circuits performs complex sequences of operations and consequently contains a large number of circuit elements. The high component density that can be achieved in MOS circuits makes it possible for such sequences of operations to be performed by a single integrated circuit.

The other five circuits perform electrical conversions and simple logical functions necessary for the transfer of information to and from the LSI MOS circuits. They are medium-scale and small-scale bipolar circuits. These circuits are not integrated into the large-scale MOS circuits because of the heat dissipated in them during their operation.

MICROPROCESSOR

The microprocessor (CPU) is a complete central-processing unit in a 40-pin package. It contains all the control logic and data manipulation logic required to perform the data processing operations typically performed by the central processing unit of a minicomputer.

It has an extensive and proven instruction set, a program interrupt facility and a data channel facility similar to those of Data General's NOVA 3 computer. The instruction set includes memory reference instructions (including instructions that alter program flow), arithmetic/logical instructions, multiply/divide instructions, stack instructions, trap instructions and I/O instructions. The program interrupt facility alters program flow at the request of a peripheral. The data channel facility transfers data between a peripheral and a memory element at the request of the peripheral.

The CPU contains four 16-bit accumulators, a 15-bit program counter, a 15-bit stack pointer and a 15-bit frame pointer.

The CPU communicates with 32,768 memory locations via three memory control pins and sixteen memory address/data pins. During one memory operation, it may transfer sixteen bits of data from and/or to one memory location.

The CPU communicates with 61 peripherals via four I/O data pins and two I/O request pins. During one I/O operation, it transfers sixteen bits of data to or from one peripheral.

The CPU is designed to operate with the other circuits in the microNOVA product line. It is ordinarily connected to memory transceivers and an I/O transceiver to form a CPU module. Furthermore, the CPU is designed so that memory elements that communicate with the CPU via the memory control pins and memory address/data pins may be conveniently formed of 4K dynamic RAMs. Similarly, peripherals that communicate with the CPU via the I/O data pins and I/O request pins may be conveniently designed around an I/O controller.

4K DYNAMIC RAM

The 4K dynamic RAM is a 4096-bit dynamic random-access memory in a 20-pin package. It performs read, write and refresh operations. A read operation may be performed in 300 nanoseconds; a write or refresh operation may be performed in 600 nanoseconds.

Read and write operations are performed on one bit at a time. The bit to be read or written is selected by a 12-bit address.

Refresh operations are performed on sixty-four bits simultaneously; all bits in the RAM must be refreshed every 2.4 milliseconds. The bits to be refreshed are selected by a 6-bit address.

The RAM receives addresses via twelve address pins. An address is latched at the beginning of a read, write or refresh operation so that it need not be maintained on the pins for the duration of the operation.

The RAM is designed so that sixteen of them may be conveniently connected to form a 4K x 16-bit memory module that operates in the microNOVA computer system. In such a module, the RAMs are supported by two address drivers and four sense amplifiers.

I/O CONTROLLER

The I/O controller (IOC) is a circuit that facilitates the design of peripherals that operate in the microNOVA computer system. The IOC is mounted in a 40-pin package.

The IOC performs operations that are commonly performed by peripherals in the microNOVA computer system. It decodes and executes I/O commands and data-channel-acknowledge codes received from the CPU. It transforms serial format in which the CPU transmits data to parallel format convenient within peripherals and vice-versa. It makes program interrupt and data channel requests in accordance with the microNOVA system constraints related to the request enable code and interrupt and data channel priority chains among controllers.

The IOC is ordinarily connected to an IOC I/O transceiver to form an IOC module.

MEMORY TRANSCEIVER

The memory transceiver is the interface between the memory address/data pins of the CPU and the microNOVA memory bus. It is mounted in a 20-pin package. The memory transceiver contains eight pairs of 2-input, open-collector OR gates. It drives and receives eight address/data lines of the memory bus.

Two memory transceivers are required in every CPU module.

ADDRESS DRIVER

The address driver is the interface between the address and data inputs of a 4K x 16-bit memory module and the microNOVA memory bus. It is mounted in a 20-pin package.

The address driver buffers the relatively high input capacitance of the address pins of the 4K dynamic RAMs. Each address driver buffers eight memory bus signals.

Two address drivers are required in every 4K x 16-bit memory module.

SENSE AMP/BUS DRIVER

The sense amplifier is the interface between the data outputs of a 4K x 16-bit memory module and the microNOVA memory bus. It is mounted in a 16-pin package.

The sense amp/bus driver is a current amplifier that drives data onto the memory bus. Each sense amp/bus driver drives four memory bus signals.

Four sense amplifiers are required in each 4K x 16-bit memory module; however, four sense amplifiers may be shared by two 4K x 16-bit memory modules.

CPU I/O TRANSCEIVER

The CPU I/O transceiver is the interface between the I/O data pins of the CPU and the microNOVA I/O bus. It is mounted in a 20-pin package.

It contains flip-flops, differential transmitters and differential receivers. It performs the necessary electrical conversions between the CPU's I/O data pins and the differential pairs of data signals of the I/O bus. It synchronizes information transferred via these signals by clocking information from the CPU's I/O data pins when the CPU is transmitting information to the I/O bus and by strobing data from the bus when the CPU is receiving information from the I/O bus. The CPU I/O transceiver also transmits a differential master clock signal to synchronize the operation of peripherals on the I/O bus with that of the CPU.

One CPU I/O transceiver is required in each CPU module.

IOC I/O TRANSCEIVER

The IOC I/O transceiver is the interface between the I/O data pins of the IOC and the signals of the microNOVA I/O bus. It is mounted in a 20-pin package.

The IOC I/O transceiver performs functions for the IOC similar to those that the CPU I/O transceiver performs for the CPU. It receives the master clock transmitted by the CPU I/O transceiver.

One IOC I/O transceiver is required in each IOC module.

MODULES

As indicated above, the integrated circuits in the microNOVA product line are connected to form data processing elements called modules. In these modules, the LSI MOS circuits are combined with the bipolar circuits that support them. Accordingly, there are three types of modules: CPU modules, RAM modules and IOC modules.

The CPU module is a central processing unit; functionally, it is almost identical to the microprocessor. However, in the CPU module, the microprocessor is connected to supporting circuits that make the module compatible with RAM and IOC modules. The CPU module is composed of a microprocessor, memory transeivers, a CPU I/O transeiver and a small number of SSI TTL components.

The RAM modules are memory elements that respond properly to the protocols that the CPU follows in communications with memory. There are two types of RAM modules, a 4K x 16-bit RAM module that contains 4096 16-bit memory locations and an 8K x 16-bit RAM module that contains 8192 16-bit memory locations. (An 8K x 16-bit RAM module is composed of two 4K x 16-bit RAM modules that share some components.) Each RAM module is composed of 4K dynamic RAMs, address drivers, sense amplifiers and a small number of SSI TTL components.

The IOC module facilitates the design of peripherals that communicate with the CPU. It performs operations that most peripherals must perform in order to respond properly to the protocols that the CPU follows in communications with peripherals. Functionally, the IOC module is almost identical to the I/O controller. However, in the IOC module, the I/O controller is connected to supporting circuits that make the module compatible with the CPU module. Each IOC module consists of an I/O controller, an IOC I/O transceiver and a small number of SSI TTL components.

microNOVA COMPUTER SYSTEM

The microNOVA computer system is composed of three types of data processing elements: a central processing unit, memory elements and peripherals. These data processing elements communicate as shown in the following block diagram.

The group of signals via which the central processing unit commiunicates with memory elements is called the microNOVA memory bus. It consists of three control lines and sixteen address/data lines. All lines are TTL-compatible busses with external pull-up resistors.

The group of signals via which the central processing unit communicates with peripherals is called the microNOVA I/O bus. It consists of eleven lines: three differential pairs of bidirectional data busses, a differential pair of master clock lines, two 1-bit TTL-compatible request busses, and a TTL-compatible clear line. Information is transferred via the data busses in a 2-bit serial format. (Two of the differential pairs carry data and one carries timing information.) The master clock lines synchronize the operation of peripherals with that of the CPU. The request busses carry external interrupt and data channel requests from peripherals to the CPU. The clear line indicates that peripherals are to reset themselves (e.g., during power-up).

Peripherals also communicate among themselves via two sets of signals called the interrupt and data channel priority chains (INTP chain and DCHP chain, respectively). The protocols that the CPU follows in communications with peripherals demand that peripherals sometimes determine among themselves which one is to perform a sequence of operations specified by the CPU. Peripherals communicate among themselves via the priority chains to make this determination. The priority signals are usually considered to be part of the I/O bus.

Central Processing Unit

The central processing unit in the microNOVA computer system is the CPU module described above.

Memory Elements

Memory elements in the system are any data processing elements with which the CPU communicates via its memory control and address/data pins. Memory elements may perform a wide variety of operations; however, the protocols that the CPU follows in communications with its memory pins favor data storage and retrieval operations (i.e., writing and reading). microNOVA line RAM modules are ordinarily used for this purpose.

Peripherals

Peripherals in the system are any data processing elements with which the CPU communicates via its I/O data and I/O request pins. Peripherals vary greatly in the operations they perform and therefore in their design; however, the CPU follows the same protocols in communications with each. Consequently, the IOC module is the interface between most peripherals and the I/O bus.

ORDERING

Each microNOVA integrated circuit is available in packages of one, five, twenty-five, one hundred and five hundred. The circuits are also available in a CPU/4K chip set (8563A) and a General-Purpose Interface chip set (4210A) that facilitate engineering evaluation.

Each package has a model number that specifies the circuit that the package contains. The model numbers are as follows:

Model Number	Integrated Circuit
100-0601	mN601 microprocessor
100-0606	mN606 4K dynamic RAM
100-0603	mN603 I/O Controller
100-0634	mN634 memory transceiver
100-0633	mN633 address driver
100-0506	mN506 sense amp/bus driver
100-0636	mN636 CPU I/O transceiver
100-0629	mN629 IOC I/O transceiver

If the package contains more than one circuit, a letter suffix indicates the number of circuits that it contains. The letter suffixes are as follows:

Letter	Quantity
5	M
25	N
100	P
500	Q

The CPU/4K chip set includes all the components of a CPU module and a 4K x 16-bit memory module. In addition to the required microNOVA integrated circuits, the set includes all supporting TTL circuits, an etched circuit board, schematics and all other system documentation.

The General Purpose Interface chip set includes all the components of an IOC module. In addition to the required microNOVA integrated circuits, the set includes all supporting TTL circuits, an etched circuit board, schematics and all other system documentation.

MEMORY ELEMENT

MEMORY ELEMENT

MEMORY

$\overline{BPG}$
$\overline{BSAEG}$
$\overline{BWEG}$

MEMORY BUS

BDATA[0-15]

CPU MODULE

I/O BUS

$\overline{BEXTINT}$
$\overline{BDCHINT}$

MCLOCK
$\overline{MCLOCK}$
BI/O CLOCK
$\overline{BI/O\ CLOCK}$
BI/O DATA1
$\overline{BI/O\ DATA1}$
BI/O DATA2
$\overline{BI/O\ DATA2}$
$\overline{CLEAR}$

TO ADDITIONAL PERIPHERALS

HALT

$\overline{CLAMP}$

IOC MODULE

IOC MODULE

$\overline{INT\ SYNC}$
$\overline{DCH\ SYNC}$
INTP
DCHP

$\overline{DATOA}$
$\overline{DATIA}$
$\overline{DATOB}$
$\overline{DATIB}$
$\overline{DATOC}$
$\overline{DATIC}$
$\overline{STRT}$
$\overline{CLR}$
$\overline{IOPLS}$
$\overline{IORST}$
$\overline{MSKO}$
$\overline{DCHA}$
$\overline{DCHI}$
$\overline{DCHO}$
$\overline{WCEZ}$
$\overline{NOP}$

BUSY
DONE
SET BUSY
SET DONE
D[0-15]

PERIPHERAL

PERIPHERAL

INTP IN

DCHP IN

INTP OUT
DCHP OUT

TO NEXT PERIPHERAL

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ORGANIZATION OF THIS MANUAL

This manual contains sections that describe each integrated circuit in the microNOVA product line and sections that explain how the circuits are connected in a microNOVA computer system.

In each section that describes a circuit, four kinds of information about the circuit are presented: package information, definition of pin names, electrical specifications and a functional description.

The package information lists the package(s) in which the circuit is available. All packages are described in Appendix A.

The definition of pin names is a diagram that assigns a name to each pin of the circuit. Pins are referenced by name in the electrical specifications and the functional description of the circuit. By convention, the name of a pin is overscored if the function suggested by the name of the pin is performed when the pin is at low level or in the low state. For example, the CPU only performs a data channel break when the pin named $\overline{\text{DCH INT}}$ is at low level.

Electrical specifications are given for each pin of the circuit.

The functional description explains the functional relation between the pins of the circuit. It takes the form of a schematic diagram, timing diagrams or any other representation that describes the behavior of the circuit. The functional description presumes that all power pins are at their normal operating voltages, and unless otherwise specified, that all output loads are 20 picofarads.

CONVENTIONS

For clarity and brevity, the following conventions are employed in this manual.

1) A group of pins whose names differ from one another only in their rightmost numeral(s) may be designated by a single name followed by a list of numerals in square brackets. A hyphen represents all numerals whose values are between those of the numerals adjacent to it. For example, the pins named MB0, MB2, MB13, MB14 and MB15 may be designated by MB[0,2,13-15].

2) Information may be represented by a binary numeral. Each binary digit represents one bit.

3) An ordered sequence of binary digits may be represented by an octal numeral. An octal digit represents three binary digits as follows: 0=000, 1=001, 2=010, 3=011, 4=100, 5=101, 6=110 and 7=111. If the number of bits in such a sequence is not an integral multiple of three, the leftmost octal digit represents only one or two bits, as required.

SECTION II

mN601
MICROPROCESSOR (CPU)

- PACKAGE

- PIN NAMES AND NUMBERS

- DC (STATIC) CHARACTERISTICS

- FUNCTIONAL DESCRIPTION

PACKAGE

The mN 601 integrated circuit is supplied in a 40-pin, ceramic, dual in-line plug package (DIP).

PIN NUMBERS AND NAMES

Name	Pin		Pin	Name
V$_{BB}$	1		40	V$_{SS}$ (ground)
PG	2		39	N/C
WEG	3		38	V$_{DD}$
SAEG	4		37	HLT
$\overline{DCH\ INT}$	5		36	N/C
$\overline{EXT\ INT}$	6		35	$\overline{CLAMP}$
V$_{GG}$	7		34	N/C
V$_{SS}$ (ground)	8		33	$\overline{PAUSE}$
MB0	9		32	α1,3
MB1	10		31	α2,4
MB2	11		30	I/O DATA 1
MB3	12		29	I/O DATA 2
MB4	13		28	I/O INPUT
MB5	14		27	I/O CLOCK
MB6	15		26	V$_{SS}$ (ground)
MB7	16		25	MBI5
V$_{CC}$	17		24	MBI4
MB8	18		23	MBI3
MB9	19		22	MBI2
MB10	20		21	MBI1

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ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range V$_{BB}$	-2	to	-7	Volts
Supply Voltage Range V$_{CC}$	-0.3	to	+7	Volts
Supply Voltage Range V$_{DD}$	-0.3	to	+13	Volts
Supply Voltage Range V$_{GG}$	-0.3	to	+17	Volts
Input Voltage Range V$_I$	-0.3	to	+7	Volts
Input Current Range I$_I$	0	to	6	mAmps
Operating Temperature Range T$_A$	0	to	+70	°C
Storage Temperature Range T$_{stg}$	-55	to	+125	°C
Average Power Dissipation			1	Watt

NOTES *All voltages in this document are referenced to V$_{ss}$ (ground).*

Subjecting a circuit to conditions either outside these limits or at these limits for an extended period of time may cause irreparable damage to the circuit. As such, these ratings are not intended to be used during the operation of the circuit. Operating specifications are given in the DC (STATIC) CHARACTERISTICS TABLE.

D. C. (STATIC) CHARACTERISTICS
mN601

OPERATING SPECIFICATIONS

T_A range __0__ to __70__ $^\circ$C V_{GG} = 14 ± 1.0 Volts I_{CC} = __20__ mAmps Average I_{BB} = __-.1__ mAmps Average

V_{CC} 5 ± 0.25 Volts V_{BB} = -4.25 ± .25 Volts I_{DD} = __50__ mAmps Average I_{SS} = __-150__ mAmps Average

V_{DD} = 10 ± 1.0 Volts V_{SS} = 0 ± 0.0 Volts I_{GG} = __20__ mAmps Average

CHARACTERISTIC	SYMBOL	UNITS	PINS	LIMITS MIN.	LIMITS MAX.
INPUT LOW VOLTAGE	V_{IL}	Volts	α1, 3 and α2, 4	-2.0	+0.5
			MB 0-15 , $\overline{CLAMP}$ EXTINT, DCH INT	-1.0	+1.0
			I/O CLOCK, I/O DATA 1, I/O DATA 2	-1.0	+0.5
INPUT CURRENT FOR LOW STATE	I_{IL}	mAmps	α1, 3 and α2, 4	-	+.01
			MB 0-15	0	-2.0
			$\overline{EXTINT}$, $\overline{DCH INT}$, $\overline{CLAMP}$	-2.0	-4.0
			I/O CLOCK, I/O DATA 1, I/O DATA 2	-2.0	-4.0
INPUT HIGH VOLTAGE	V_{IH}	Volts	α1, 3 and α2, 4	+13.0	+15.0
			MB 0-15 , $\overline{CLAMP}$ $\overline{EXTINT}$, $\overline{DCH INT}$	+4.25	+5.8
			I/O CLOCK, I/O DATA 1, I/O DATA 2	+2.5	+5.8
INPUT CURRENT FOR HIGH STATE	I_{IH}	mAmps	α1, 3 and α2, 4	-	-.01
			MB 0-15	-	-.06
			I/O CLOCK, I/O DATA 1, I/O DATA 2	-	-1.0
			$\overline{EXTINT}$, $\overline{DCH INT}$	-	-.02
			$\overline{CLAMP}$	-	+.001
OUTPUT LOW VOLTAGE	V_{OL}	Volts	HALT	-	+3.0
			MB 0-15 , I/O INPUT, $\overline{PAUSE}$, SAEG, WEG, PG	-	+0.4
			I/O CLOCK, I/O DATA 1, I/O DATA 2		+0.5
OUTPUT CURRENT FOR LOW STATE	I_{OL}	mAmps	PG, I/O INPUT	+4.0	
			MB 0-15 , I/O CLOCK I/O DATA 1, I/O DATA 2 $\overline{PAUSE}$, SAEG, PG, HALT	+2.0	-
OUTPUT HIGH VOLTAGE	V_{OH}	Volts	MB 0-15 I/O CLOCK, I/O DATA 1, I/O DATA 2 I/O INPUT, PAUSE, SAEG, WEG, PG	+4.25	-
			HALT	V_{CC}-0.5	
OUTPUT CURRENT FOR HIGH STATE	I_{OH}	mAmps	HALT	-	-.01
			MB 0-15	-	-.06
			I/O INPUT, PG	-	-.02
			I/O CLOCK, I/O DATA 1, I/O DATA 2, PAUSE SAEG, WEG	-	-.01
INPUT CAPACITANCE	C_I	pF	α1, 3 and α2, 4	-	100
			$\overline{CLAMP}$ MB 0-15 , I/O CLOCK I/O DATA 1, I/O DATA 2 $\overline{EXTINT}$, $\overline{DCH INT}$	-	10

NOTE

Logic "1" is defined as the more positive voltage as are the maximum figures given under voltage limits. Logic "0" is defined as the more negative voltage as are the minimum figures given under voltage limits.

Positive current, in the conventional sense, is defined as flowing into the pin.

On power-up, V_{BB} must be within its specified operating range (with respect to V_{SS}) before any of the other power supply voltages are applied to the circuit.

FUNCTIONAL DESCRIPTION

The microprocessor (CPU) is a complete central processing unit. It contains all the control logic and data manipulation logic necessary to perform data processing operations typically performed by the central processing unit of a minicomputer. It executes instructions, performs program interrupts and performs data channel breaks.

In performing these operations, the CPU transmits and receives information via its pins; it stores information in registers that it contains; and it performs arithmetic and logical operations on information received via its pins and stored within it.

Internal Organization

The following block diagram shows how the pins, registers and other internal components of the CPU are organized.

Registers

The CPU stores information within itself in thirteen registers. The registers and the amount of information that is stored in each one are listed in the following table.

Register	Size
accumulator 0	16 bits
accumulator 1	16 bits
accumulator 2	16 bits
accumulator 3	16 bits
stack pointer	15 bits
frame pointer	15 bits
program counter	15 bits
carry bit	1 bit
interrupt enable bit	1 bit
real-time-clock enable bit	1 bit
stack-overflow request bit	1 bit
real-time-clock request bit	1 bit
refresh address counter	6 bits

In registers that hold fifteen or sixteen bits of information, the bits are numbered. The bits in 15-bit registers are numbered from 1 to 15. The bits in 16-bit registers are numbered from 0 to 15.

Pins

The CPU transmits and receives information via thirty of its forty pins. (The other pins supply power to the CPU or are unused.) The thirty pins may be divided into functional groups as shown in the following table.

Functional Group	Pins
Clock Pins	alpha 1,3
	alpha 2,4
Memory Control Pins	PG
	SAEG
	WEG
Memory Address/Data Pins	MB[0-15]
I/O Data Pins	I/O CLOCK
	I/O DATA1
	I/O DATA2
	I/O INPUT
I/O Request Pins	EXT INT
	DCH INT
Other Pins	CLAMP
	HALT
	PAUSE

Clock Pins

In order for the CPU to operate, non-overlappping clocks must be applied to alpha 1,3 and alpha 2,4, as shown in the following timing diagram.

mN601 CLOCKS

PERIOD = 120ns

	MIN.	MAX.
T_F	10	15
T_R	10	15
T_D	10	25
T_H	95	110
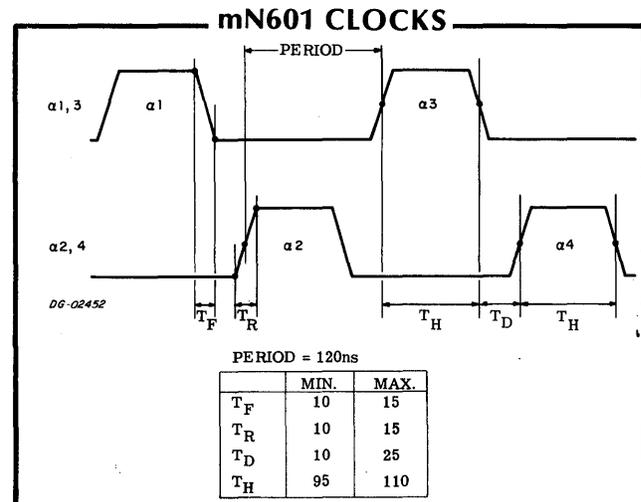
Each interval during which alpha 1,3 or alpha 2,4 is at high level is called an alpha cycle. There are four kinds of alpha cycles called alpha 1, alpha 2, alpha 3 and alpha 4 cycles. Alternate intervals during which alpha 1,3 is at high level are alpha 1 cycles and alpha 3 cycles. Alternate intervals during which alpha 2,4 is at high level are alpha 2 cycles and alpha 4 cycles.

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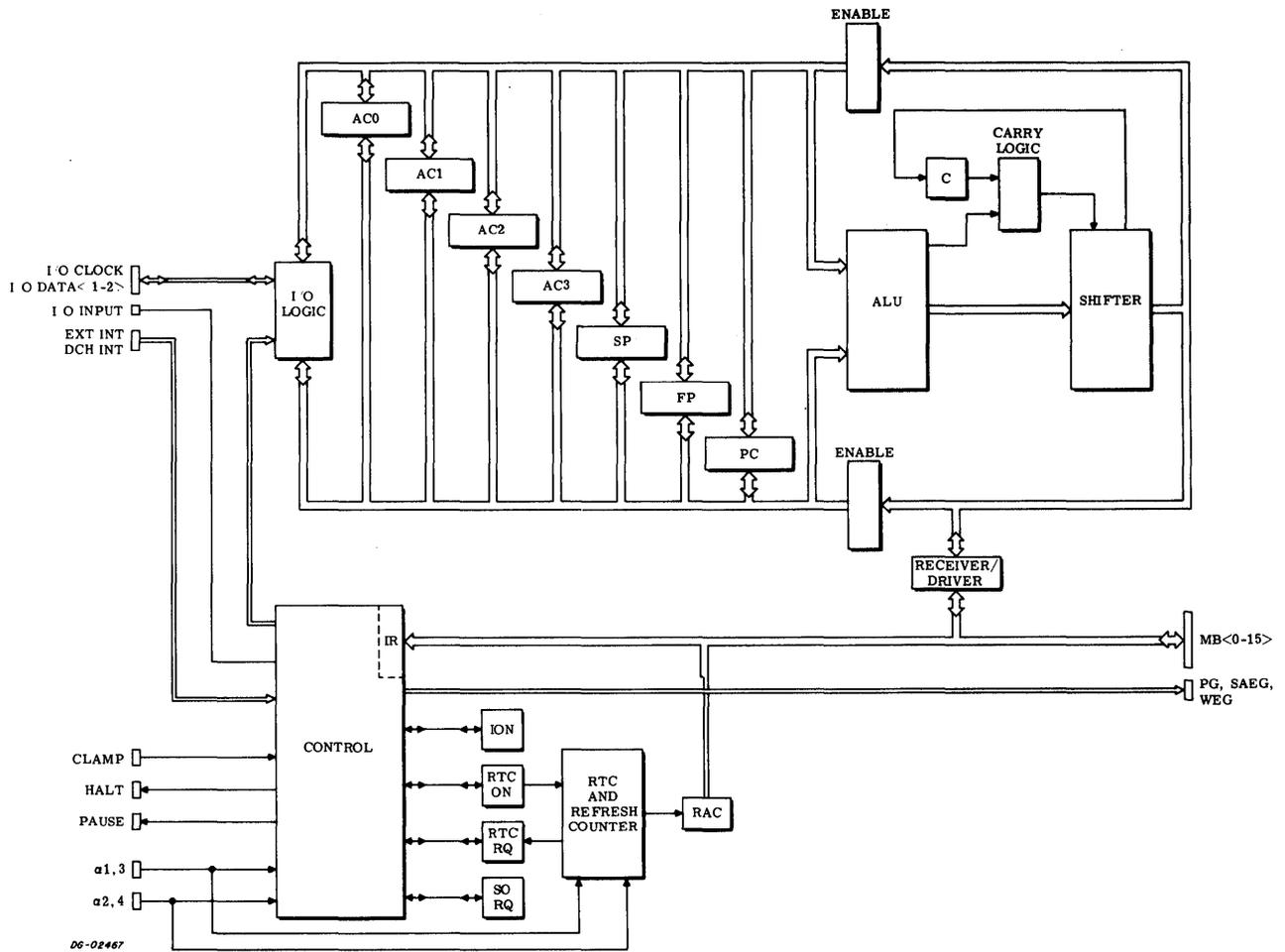
Following power-up, alpha 1,3 must go to high level before alpha 2,4. This first interval during which alpha 1,3 is at high level is an alpha 1 cycle. The interval during which alpha 2,4 is at high level immediately succeeding this alpha 1 cycle is an alpha 2 cycle.

Different events occur on the pins of the CPU during each kind of alpha cycle. Therefore, alpha cycles are labeled in all following timing diagrams.

For simplicity, the remainder of this description of the CPU presumes that all alpha cycles are 120 nanoseconds.

Memory Control and Memory Address/Data Pins

The CPU communicates with memory elements via the memory control and memory address/data pins. These pins, their significance to the CPU and the direction in which information is transferred through them are listed in the following table.

Pin	Significance	Direction
PG	initiates memory operation	From CPU
SAEG	indicates data transfer to CPU	From CPU
WEG	indicates data transfer from CPU	From CPU
MB[0-15]	carry address and data	To and from CPU

The CPU performs four kinds of operations on the memory control and address/data pins: read operations, write operations, read-modify-write operations and refresh operations.

During the first three of these operations, data is transferred between the CPU and one of $32,768_{10}$ memory locations. A read operation is an operation in which a 16-bit datum is transferred from a memory location to the CPU. A write operation is an operation in which a 16-bit datum is transferred from the CPU to a memory location. A read-modify-write operation is an operation in which a 16-bit datum is transferred to the CPU from a memory location and a different datum (the result of an operation performed on the data just transferred in) is transferred from the CPU to the same memory location.

During a refresh operation, the CPU specifies 512_{10} locations to be refreshed but transfers no data. This facilitates the use of memories composed of dynamic RAMs in microNOVA computer systems. The 512_{10} locations are one sixty-fourth of memory and are selected by a 6-bit refresh address. A memory location that must be refreshed may be refreshed only during a refresh operation; at all other times it must must be available for read, write and read-modify-write operations.

Whether the CPU is performing a memory operation or not, MB[0-15] are precharged during every alpha 2 cycle. Damage to the CPU circuit may result if any of these pins is at low voltage during an alpha 2 cycle. Damage does not result if the load on each of these pins during an alpha 2 cycle sinks less current than one TTL open-collector output in the high state and a 1-unit-load TTL input in parallel.

The CPU receives information (the contents of memory locations) via MB[0-15] by precharging these pins during an alpha 2 cycle and by sampling the levels of these pins at the end of the next alpha 3 cycle. It is expected that during this alpha 3 cycle external drivers discharge any of MB[0-15] that are to receive 0.

The CPU transmits information (addresses and data) by precharging MB[0-15] during an alpha 2 cycle and by discharging any of these pins that are to transmit 0 during the next alpha 4 cycle. If external drivers discharge these pins during an alpha 3 cycle when they are about to transmit information or during an alpha 4 or alpha 1 cycle while they are transmitting it, that information is lost.

The rise times of PG, SAEG and WEG are between 15 and 25 nanoseconds. Their fall times are between 5 and 15 nanoseconds.

The rise times of MB[0-15] are 20 to 40 nanoseconds. Their fall times are 5 to 15 nanoseconds.

For reference, bits transmitted and received are numbered from 0 to 15. A bit transmitted via MB0 is bit 0, a bit transmitted or received via MB1 is bit 1, etc.

The events that occur on the memory pins during memory operations are described below.

READ OPERATION
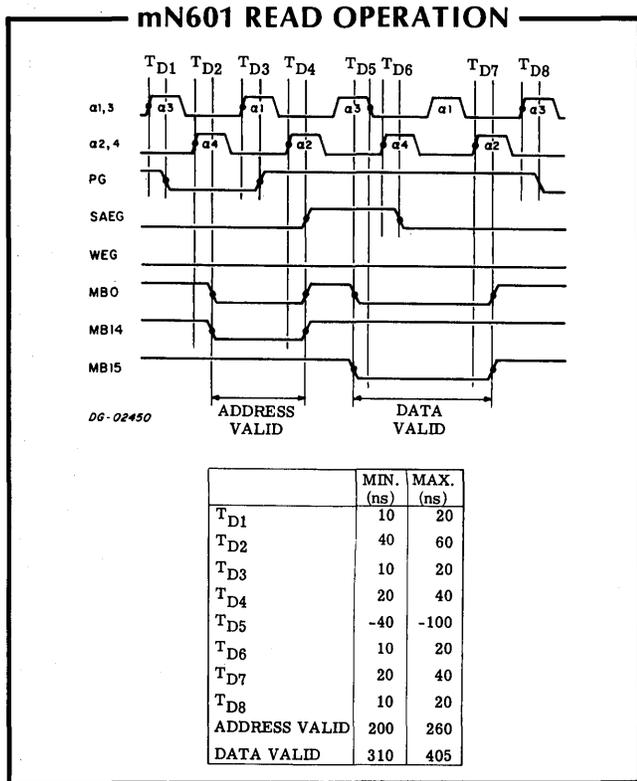
mN601 READ OPERATION

DG-02450

ADDRESS VALID   DATA VALID

	MIN. (ns)	MAX. (ns)
T_{D1}	10	20
T_{D2}	40	60
T_{D3}	10	20
T_{D4}	20	40
T_{D5}	-40	-100
T_{D6}	10	20
T_{D7}	20	40
T_{D8}	10	20
ADDRESS VALID	200	260
DATA VALID	310	405

PG assumes the high state during an alpha 1 cycle. It may assume the low state again during the second alpha 3 cycle after that alpha 1 cycle or during any subsequent alpha 3 cycle. The alpha 3 cycle during which it assumes the low state is the one immediately preceding the next memory operation. As shown in this timing diagram, PG assumes the low state during the earliest possible alpha cycle.

SAEG assumes the high state during the first alpha 2 cycle after PG assumes the high state and assumes the low state during the next alpha 4 cycle.

WEG remains in the low state for the duration of a read operation.

During the alpha 4 cycle immediately preceding the alpha 1 cycle during which PG assumes the high state, the address of the memory location to be read is transmitted via MB[0-15]. Each of MB[0-15] is discharged to transmit 0 or remains undischarged to transmit 1. MB0 always transmits 0; each of MB[1-15] may transmit 0 or 1. MB14 is shown as a typical pin transmitting 0; MB15 is shown as a typical pin transmitting 1.

During the alpha 1 cycle during which PG assumes the high state, MB[0-15] are in the neutral state. Unless they are charged and/or discharged by external drivers, they continue to transmit the address of the memory location to be read.

During the next alpha 2 cycle, MB[0-15] are precharged.

At the end of the next alpha 3 cycle, the levels at MB[0-15] are sampled. The information received is interpreted as the contents of the specified memory location. Low level is interpreted as 0; high level is interpreted as 1. MB0 and MB15 are shown as typical pins receiving 0. MB14 is shown as a typical pin receiving 1.

During the next alpha 2 cycle and any succeeding ones, MB[0-15] are precharged.

During all succeeding alpha 3, alpha 4 and alpha 1 cycles until the alpha 3 cycle during which PG assumes the low state, MB[0-15] are in the neutral state. Unless they are discharged by external drivers, they remain at high voltage.

WRITE OPERATION
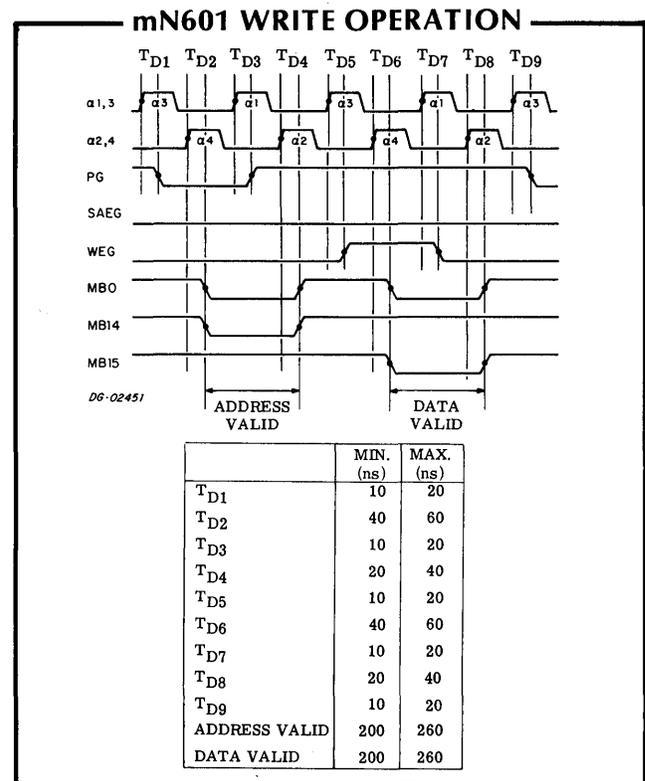
mN601 WRITE OPERATION

DG-02451

ADDRESS VALID   DATA VALID

	MIN. (ns)	MAX. (ns)
T_{D1}	10	20
T_{D2}	40	60
T_{D3}	10	20
T_{D4}	20	40
T_{D5}	10	20
T_{D6}	40	60
T_{D7}	10	20
T_{D8}	20	40
T_{D9}	10	20
ADDRESS VALID	200	260
DATA VALID	200	260

PG assumes the high state during an alpha 1 cycle and assumes the low state during the second succeeding alpha 3 cycle.

SAEG remains in the low state for the duration of a write operation.

WEG assumes the high state during the first alpha 3 cycle after the alpha 1 cycle during which PG assumes the high state. It assumes the low state during the next alpha 1 cycle.

During the alpha 4 cycle immediately preceding the alpha 1 cycle during which PG assumes the high state, the address of the memory location to be written is transmitted via MB[0-15]. Each of MB[0-15] is discharged to transmit 0 or remains undischarged to transmit 1. MB0 always transmits 0; each of MB[1-15] may transmit 0 or 1. MB14 is shown as a typical pin transmitting 0; MB15 is shown as a typical pin transmitting 1.

During the alpha 1 cycle during which PG assumes the high state, MB[0-15] are in the neutral state. Unless they are charged and/or discharged by external drivers, they continue to transmit the address of the memory location to be written.

During the next alpha 2 cycle, MB[0-15] are precharged.

During the next alpha 3 cycle, MB[0-15] are in the neutral state. Unless they are discharged by external drivers, they remain at high voltage.

During the next alpha 4 cycle, the datum to be written to the specified memory location is transmitted via MB[0-15]. Each of MB[0-15] is discharged to transmit 0 or remains undischarged to transmit 1. MB0 and MB15 are shown as typical pins transmitting 0. MB14 is shown as a typical pin transmitting 1.

During the next alpha 1 cycle, MB[0-15] are in the neutral state. Unless they are charged and/or discharged by external drivers, they continue to transmit the datum to be written to the specified location.

During the next alpha 2 cycle, MB[0-15] are precharged.

During the alpha 3 cycle during which PG assumes the low state, MB[0-15] are in the neutral state. Unless they are discharged by external drivers, they remain at high voltage.

READ-MODIFY-WRITE OPERATION
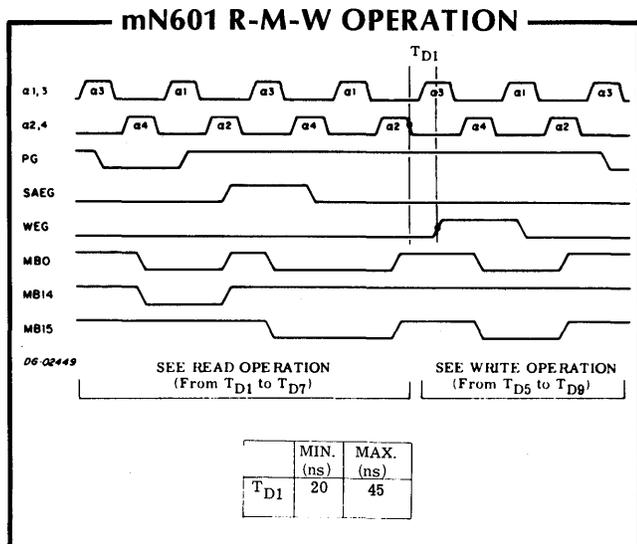
mN601 R-M-W OPERATION

PG assumes the high state during an alpha 1 cycle. It may assume the low state again during the third alpha 3 cycle after that alpha 1 cycle or during any subsequent alpha 3 cycle.

SAEG assumes the high state during the first alpha 2 cycle after PG assumes the high state and assumes the low state during the next alpha 4 cycle.

WEG may assume the high state during the second alpha 3 cycle after PG assumes the high state or during any subsequent alpha 3 cycle. It assumes the low state during the next alpha 4 cycle. PG always assumes the low state during the first alpha 3 cycle after WEG assumes the low state.

As shown in this timing diagram, WEG assumes the high state and the low state and PG assumes the low state during the earliest possible alpha 3 cycle.

During the alpha 4 cycle immediately before the alpha 1 cycle during which PG assumes the high state, the address of the memory location to be read and written is transmitted via MB[0-15]. Each of MB[0-15] is discharged to transmit 0 or remains undischarged to transmit 1. MB0 always transmits 0; each of MB[1-15] may transmit 0 or 1. MB14 is shown as a typical pin transmitting 0; MB15 is shown as a typical pin transmitting 1.

During the alpha 1 cycle during which PG assumes the high state, MB[0-15] are in the neutral state. Unless they are charged and/or discharged by external drivers, they continue to transmit the address of the memory location to be read and written.

During the next alpha 2 cycle, MB[0-15] are precharged.

At the end of the next alpha 3 cycle, the levels at MB[0-15] are sampled. The information received is interpreted as the contents of the specified memory location. Low level is interpreted as 0; high level is interpreted as 1. MB0 and MB15 are shown as typical pins receiving 0. MB14 is shown as a typical pin receiving 1.

During the next alpha 4 and alpha 1 cycles, MB[0-15] are in the neutral state.

During the next alpha 2 cycle and any succeeding ones, MB[0-15] are precharged.

During all succeeding alpha 3, alpha 4 and alpha 1 cycles until the alpha 4 cycle after WEG assumes the high state, MB[0-15] are in the neutral state. Unless they are discharged by external drivers, they remain at high voltage.

During the alpha 4 cycle after WEG assumes the high state, the datum to be written to the specified memory location is transmitted via MB[0-15]. Each of MB[0-15] is discharged to transmit 0 or remains undischarged to transmit 1. MB0 and MB15 are shown as typical pins transmitting 0. MB14 is shown as a typical pin transmitting 1. During the next alpha 1 cycle, MB[0-15] are in the neutral state. Unless they are charged and/or discharged by external drivers, they continue to transmit the datum to be written to the specified location.

During the next alpha 2 cycle, MB[0-15] are precharged.

During the alpha 3 cycle during which PG assumes the low state, MB[0-15] are in the neutral state. Unless they are discharged by external drivers, they remain at high voltage.

REFRESH OPERATION
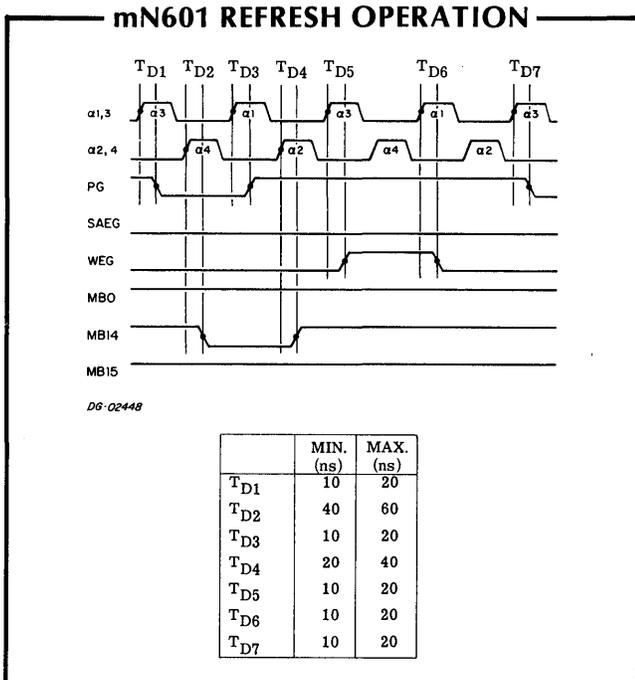
mN601 REFRESH OPERATION

	MIN. (ns)	MAX. (ns)
T_{D1}	10	20
T_{D2}	40	60
T_{D3}	10	20
T_{D4}	20	40
T_{D5}	10	20
T_{D6}	10	20
T_{D7}	10	20

PG assumes the high state during an alpha 1 cycle and assumes the low state during the second succeeding alpha 3 cycle.

SAEG remains in the low state for the duration of a refresh operation.

WEG assumes the high state during the first alpha 3 cycle after the alpha 1 cycle during which PG assumes the high state. It assumes the low state during the next alpha 1 cycle.

During the alpha 4 cycle immediately before PG assumes the high state, the refresh address is transmitted via MB[0-15]. Each of MB[0-15] is discharged to transmit 0 or remains undischarged to transmit 1. MB[0-9] always transmit 1; each of MB[10-15] may transmit 0 or 1. MB14 is shown as a typical pin transmitting 1; MB15 is shown as a typical pin transmitting 0.

During the alpha 1 cycle during which PG assumes the high state, MB[0-15] are in the neutral state. Unless they are charged and/or discharged by external drivers, they continue to transmit the refresh address.

During the next two alpha 2 cycles, MB[0-15] are precharged.

During the alpha 3, alpha 4 and alpha 1 cycles between these two alpha 2 cycles, MB[0-15] are in the neutral state.

During the alpha 3 cycle during which PG assumes the low state, MB[0-15] are in the neutral state. Unless they are discharged by external drivers, they remain at high voltage.

I/O Data Pins

The CPU communicates with peripherals via the I/O data pins. These pins, their significance to the CPU, and the direction in which information is transferred through them are listed in the following table.

Pin	Significance	Direction
I/O CLOCK	synchronizes information transfers	To and from CPU
I/O DATA1	carries control information and data	To and from CPU
I/O DATA2	carries control information and data	To and from CPU
I/O INPUT	indicates direction of transfers	From CPU

The CPU performs five kinds of operations on the I/O data pins: request-enable operations, data-channel-acknowledge operations, I/O command operations, I/O data-out operations and I/O data-in operations. These operations are described below.

In all of these operations, the rise times of the I/O data pins are 15 to 25 nanoseconds, and their fall times are 10 to 15 nanoseconds. The skew between the I/O data pins and the I/O CLOCK pin is always within ± 10 nanoseconds.

REQUEST-ENABLE OPERATIONS

During a request-enable operation, a 2-bit code called a request-enable code is transmitted via the I/O data pins to synchronize program-interrupt and data-channel requests from peripherals. The CPU performs these operations at irregular intervals that are determined by the other operations that it is performing. The following timing diagram depicts the events that occur at the I/O data pins during a request-enable operation.
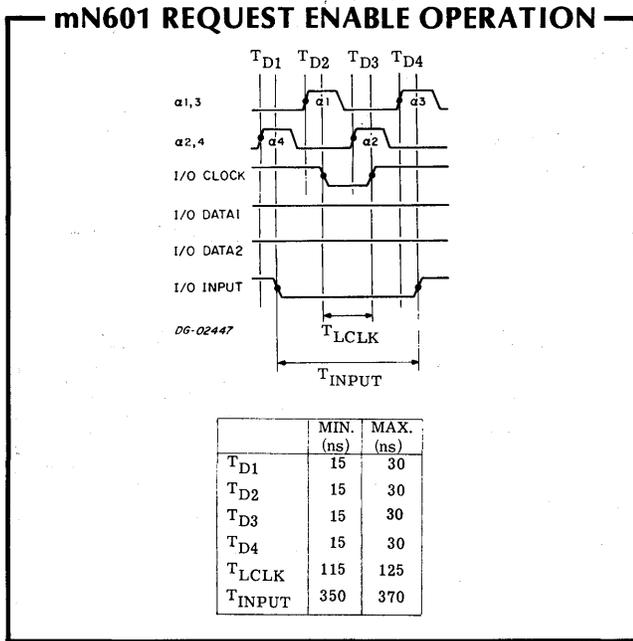
mN601 REQUEST ENABLE OPERATION

DG-02447

	MIN. (ns)	MAX. (ns)
T_{D1}	15	30
T_{D2}	15	30
T_{D3}	15	30
T_{D4}	15	30
T_{LCLK}	115	125
T_{INPUT}	350	370

I/O INPUT assumes the low state during an alpha 4 cycle.

I/O CLOCK assumes the low state during the next alpha 1 cycle and assumes the high state during the alpha 2 cycle after that.

During the interval when I/O CLOCK is in the low state, I/O DATA1 and I/O DATA2 remain in the high state.

During the next alpha 3 cycle, I/O INPUT assumes the high state.

DATA-CHANNEL-ACKNOWLEDGE OPERATIONS

During a data-channel-acknowledge operation, a 2-bit code is transmitted via the I/O data pins to indicate that the CPU has begun a data channel break. The CPU performs these operations (only) during data channel breaks. The following timing diagram depicts the events that occur at the I/O data pins during a data-channel-acknowledge operation.
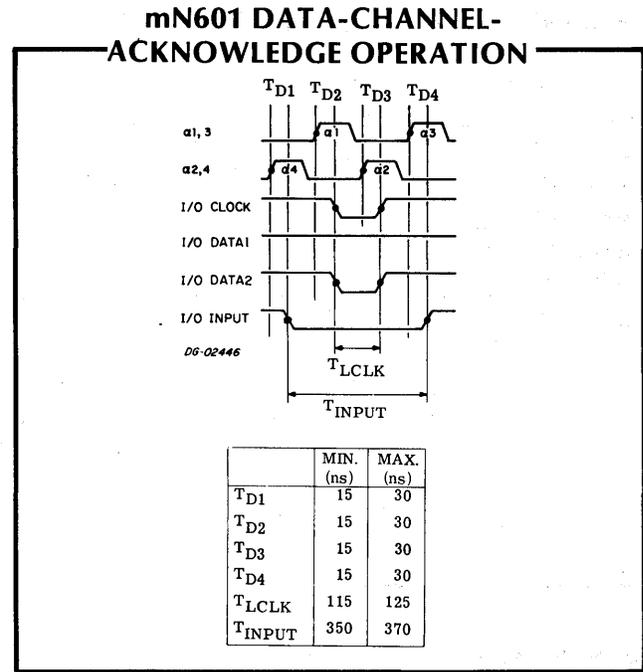
mN601 DATA-CHANNEL- ACKNOWLEDGE OPERATION

DG-02446

	MIN. (ns)	MAX. (ns)
T_{D1}	15	30
T_{D2}	15	30
T_{D3}	15	30
T_{D4}	15	30
T_{LCLK}	115	125
T_{INPUT}	350	370

I/O INPUT assumes the low state during an alpha 4 cycle.

I/O CLOCK assumes the low state during the next alpha 1 cycle and assumes the high state during the alpha 2 cycle after that.

During the interval when I/O CLOCK is in the low state, I/O DATA1 is in high state, and I/O DATA2 is in the low state.

During the next alpha 3 cycle, I/O INPUT assumes the high state.

I/O COMMAND OPERATIONS

During an I/O command operation, a 2-bit code and a 16-bit I/O command are transmitted via the I/O data pins to specify a programmed-I/O operation that the peripheral is to perform. The CPU performs an I/O command operation whenever it executes an I/O instruction. The following timing diagram depicts the events that occur at the I/O data pins during an I/O command operation.

mN601 I/O COMMAND OPERATION

	MIN. (ns)	MAX. (ns)
T_{D1}	15	30
T_{D2}	15	30
T_{D3}	15	30
T_{D4}	15	30
T_{BIT}	115	125
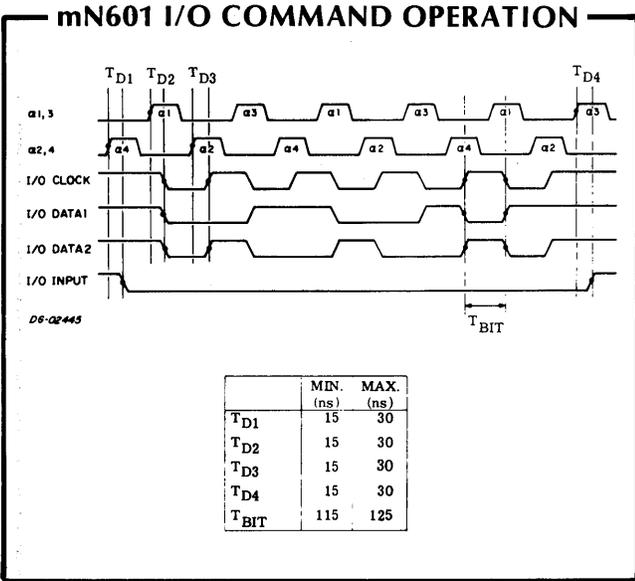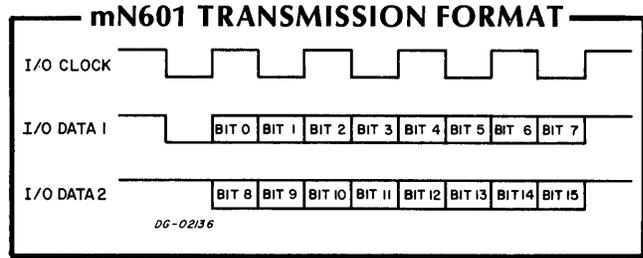
I/O INPUT assumes the low state during an alpha 4 cycle.

I/O CLOCK assumes the low state during each of the next five alpha 1 and alpha 3 cycles and assumes the high state during the alpha 2 and alpha 4 cycles that succeed those alpha 1 and alpha 3 cycles.

During the first interval when I/O CLOCK is in the low state, I/O DATA1 and I/O DATA2 both assume the low state.

Thereafter, during each interval delimited by a change in the state of I/O CLOCK, I/O DATA1 transmits one bit and I/O DATA2 transmits one bit. They assume the low state to transmit 0 and the high state to transmit 1. In this diagram, they are shown transmitting 062622_8. I/O INPUT assumes the high state during the alpha 3 cycle following the alpha 2 cycle when I/O CLOCK assumes the high state for the fifth (last) time.

For reference, bits transmitted during an I/O command operation are numbered as shown in the following diagram.

mN601 TRANSMISSION FORMAT

I/O DATA-OUT OPERATIONS

During an I/O data-out operation, a 2-bit code and a 16-bit data word are transmitted via the I/O data pins. They occur during data channel breaks and the execution of I/O instructions. The following timing diagram depicts the events that occur on the I/O data pins during an I/O operation.
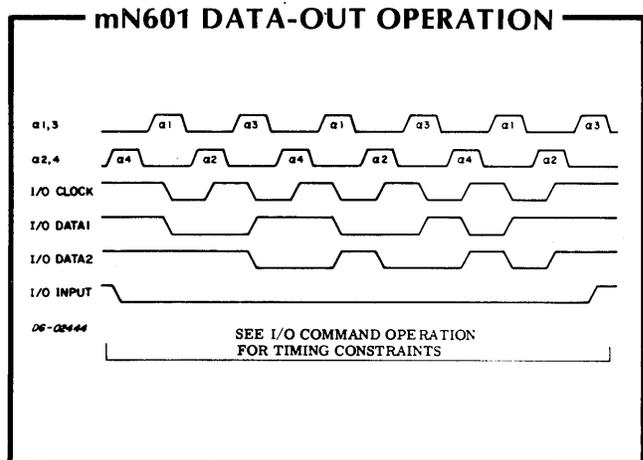
mN601 DATA-OUT OPERATION

SEE I/O COMMAND OPERATION
FOR TIMING CONSTRAINTS

I/O INPUT assumes the low state during an alpha 4 cycle.

I/O CLOCK assumes the low state during the next five alpha 1 and alpha 3 cycles and assumes the high state during the alpha 2 and alpha 4 cycles that succeed each of those alpha 1 and alpha 3 cycles.

During the first interval when I/O CLOCK is at low level, I/O DATA1 and I/O DATA2 assume the low state and high state, respectively.

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Thereafter, during each interval delimited by a change in the state of I/O CLOCK, I/O DATA1 transmits one bit and I/O DATA2 transmits one bit. They assume the low state to transmit 0 and the high state to transmit 1. In this diagram, they are shown transmitting 062622_8. For reference, bits transmitted during an I/O data-out operation are numbered as shown in the following diagram.

mN601 TRANSMISSION FORMAT

I/O CLOCK

I/O DATA 1 — BIT 0 | BIT 1 | BIT 2 | BIT 3 | BIT 4 | BIT 5 | BIT 6 | BIT 7

I/O DATA 2 — BIT 8 | BIT 9 | BIT 10 | BIT 11 | BIT 12 | BIT 13 | BIT 14 | BIT 15

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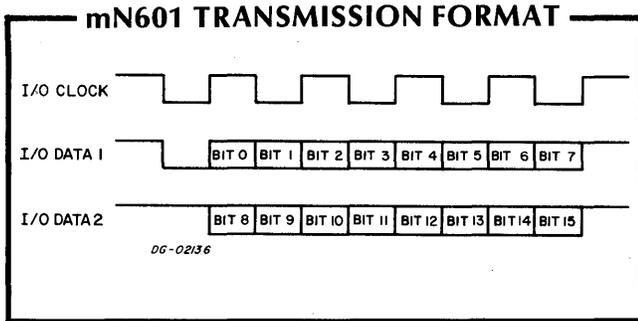
I/O DATA-IN OPERATIONS

During an I/O data-in operation, I/O CLOCK and I/O DATA[1-2] are inputs for 20 alpha cycles. (During this interval, it is expected that information is received from a peripheral in response to the data-channel-acknowledge code or an I/O command.) I/O data-in operations are performed during data channel breaks and during the execution of I/O instructions; they are always immediately preceded by a data-channel-acknowledge operation or by an I/O command operation. The following timing diagram depicts the events that occur on the pins of the I/O port during an I/O data-in operation.

An I/O data-in operation begins at the beginning of an alpha 3 cycle and ends at the end of the sixth succeeding alpha 1 cycle. There is no event that signals the beginning of an I/O data-in operation. The beginning of the I/O data-in operation is implicit in the preceding data-channel-acknowledge or I/O command operation. (See the descriptions of data channel breaks and I/O instructions.)

I/O INPUT remains in the high state and I/O CLOCK and I/O DATA[1-2] behave as input pins for the duration of an I/O data-in operation. It is expected that during this interval, I/O CLOCK and I/O DATA[1-2] receive information from a peripheral that is responding to an I/O command or data-channel-acknowledge code that the CPU has already transmitted.

I/O CLOCK, I/O DATA1 and I/O DATA2 behave as input pins much longer than the minimum time required for the CPU to receive information through the I/O port. The CPU has been designed in this way to allow a delay between the time when a peripheral receives a data-channel-acknowledge code or I/O command and the time when the information that is transmitted in response by the peripheral arrives at the CPU. This allows peripherals time to process data-channel-acknowledge codes and I/O commands they receive and also allows time for transmission delays between peripherals and the CPU. As shown in the diagram, I/O CLOCK must go to low level and return to high level five times. There is no constraint on the phase relation between I/O CLOCK and alpha 1,3 or alpha 2,4. The only timing constraints on I/O CLOCK relative to alpha 1,3 and alpha 2,4 are that the CPU does not register changes in the levels at I/O CLOCK if they occur before the first alpha 3 cycle or after the last alpha 1 cycle of the I/O data-in operation.

mN601 I/O DATA-IN OPERATION

	MIN. (ns)	MAX. (ns)
T_{D1}	15	30
T_{D2}	15	30
T_{D3}	10	20

DG-02443

SEE I/O COMMAND TRANSFER FOR TIMING CONSTRAINTS

SEE I/O COMMAND TRANSFER FOR TIMING CONSTRAINTS
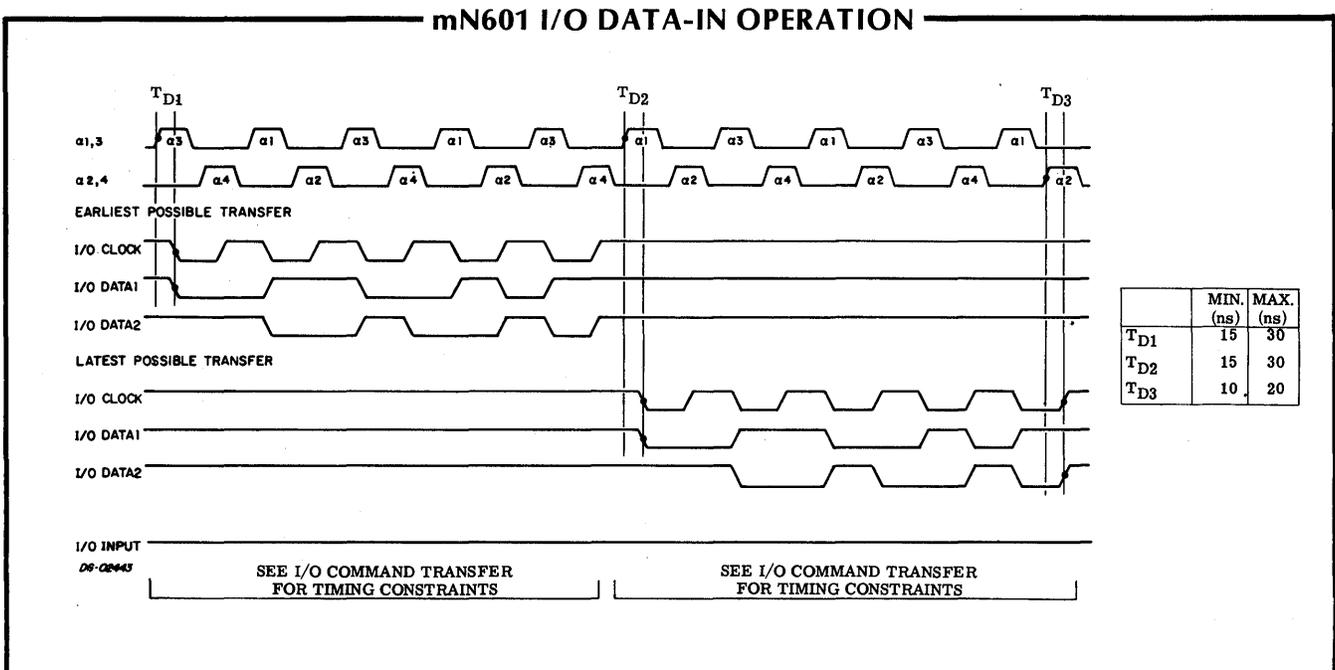
During the first interval when I/O CLOCK is at low level, I/O DATA1 and I/O DATA2 must be at low level and high level, respectively.

Thereafter, during each interval delimited by a change in the level of I/O CLOCK , the CPU receives one bit of information via I/O DATA1 and one bit via I/O DATA2. At each of these pins, low level is interpreted as 0, and high level is interpreted as 1. In this timing diagram, they are shown receiving 062622_8. For reference, bits received during an I/O data-in operation are numbered from 0 to 15, as shown in the following diagram.

mN601 TRANSMISSION FORMAT

I/O CLOCK

| I/O DATA 1 | BIT 0 | BIT 1 | BIT 2 | BIT 3 | BIT 4 | BIT 5 | BIT 6 | BIT 7 |

| I/O DATA 2 | BIT 8 | BIT 9 | BIT 10 | BIT 11 | BIT 12 | BIT 13 | BIT 14 | BIT 15 |

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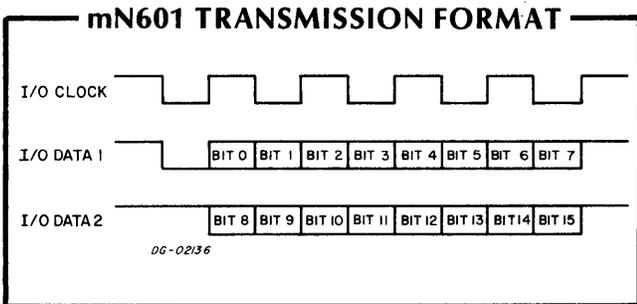
I/O Request Pins

The CPU receives information via the I/O request pins that determines when it performs external interrupts and data channel breaks. These pins and their functions are listed in the following table.

EXT INT	receive requests for external interrupts from peripherals
DCH INT	receive requests for data channel breaks from peripherals

In order to understand the significance of these pins see the descriptions of program interrupts and data-channel sequences. The only timing constraints imposed on the levels at these pins are imposed by the interaction of peripherals in the microNOVA computer system.

Other Pins

CLAMP

When the CPU is first powered up, it does not perform any operation as long as CLAMP is at low level. When CLAMP goes to high level, the CPU is initialized (see the description of power-up). Once the CPU is initialized, CLAMP has no effect on the operation of the CPU until the next time the CPU is powered up.

HALT

Whenever the CPU is halted, HALT assumes the high state periodically. At all other times it is in the low state. When HALT assumes the high state, it does so during an alpha 4 cycle and assumes the low state during the succeeding alpha 2 cycle, as shown in the following timing diagram.

HALT

	MIN. (ns)	MAX. (ns)
T_{D1}	40	60
T_{D2}	10	20
T_R	40	80
T_F	10	20

PAUSE

PAUSE is reserved for future use.

Information as Operands

During the execution of instructions, program interrupts, and data channel breaks, information is transferred between registers, the memory address/data pins, and the I/O data pins. In addition, arithmetic, logical and shift operations are performed on information in registers and information received via these pins. Before the actual sequences of operations that the CPU performs on information are described, some general, definitive statements on the interpretation of information by the CPU are presented here.

When arithmetic operations are performed on the contents of a register, the contents of each bit in the register are interpreted as a binary digit. (0 is interpreted as binary 0, and 1 is interpreted as binary 1.) The lower the number of a bit, the more significant the digit it represents, as shown in the following diagram.

mN501 BIT NUMBERING

◄── MORE SIGNIFICANT										LESS ──► SIGNIFICANT				
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

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When the contents of a register are transmitted via the memory address/data pins as data, the contents of bit 0 of the register are transmitted via pin **MB0**, the contents of bit 1 are transferred via pin **MB1**, etc.

When the contents of a register are transmitted via the memory address/data pins as an address, the contents of bits 1 to 15 of the register are transmitted via pins **MB[1-15]** as if they were data. However, the contents of bit 0 are not transferred; the state that pin **MB0** assumes depends on the operation that the CPU is performing on the pins of the memory port.

When the result of an arithmetic or logical operation is transferred out of the CPU via the memory pins as an address or data, it is transferred as if it were the contents of a register.

When information received via the memory pins is loaded into a register, the information transferred via **MB0** is loaded into bit 0 of the register, the information transferred via **MB1** is loaded into bit 1, etc.

When an arithmetic or logical operation is performed on information received via the memory pins, the information is interpreted as if it were the contents of a register.

Instruction Execution

The CPU fetches and executes instructions whenever it is not reset or halted and is not performing a program interrupt or a data channel break. Instructions are sixteen bits; each instruction is read from a single memory location.

The CPU fetches an instruction by reading a memory location and loading the contents of the location into the instruction register.

The memory location from which the instruction is read is the location whose address is contained in the program counter. Therefore, program flow depends on the operations that the CPU performs on the information in the program counter. The CPU performs operations on the contents of the program counter during program interrupts and during the execution of instructions.

When the CPU is halted, it is started by a program interrupt. Immediately after the CPU performs a program interrupt (and any data channel breaks that follow it), it fetches an instruction. The contents of the program counter at this time are the contents loaded into it during the program interrupt.

Thereafter, during the execution of each instruction, the CPU loads new contents into the program counter, and at the end of the execution of the instruction, it performs a program interrupt or fetches another instruction (unless it has just halted).

Ordinarily, the new contents that are loaded into the program counter during the execution of an instruction are the old contents (interpreted as a binary number) incremented by one. However, an instruction may specify a skip or a jump. When the instruction specifies a skip, the new contents are the old contents incremented by two. When the instruction specifies a jump, the new contents are determined by an indexed address calculation and possibly an indirect address calculation.

Immediately after the execution of one instruction, the CPU fetches and executes another one from the memory location specified by the new contents of the program counter (unless the CPU is reset or halted during the execution of the instruction or has determined that it is to perform a program interrupt or data channel break).

Indexed Address Calculation

During the execution of some instructions, the CPU calculates an indexed address. These instructions are called memory reference instructions, although not all of them actually specify a data transfer to or from memory. Bits 6 to 15 of memory reference instructions specify how the indexed address calculation is to be performed. As shown in the following diagram, bits 6 and 7 are called the index bits, and bits 8 to 15 are called the displacement.

						INDEX		DISPLACEMENT							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
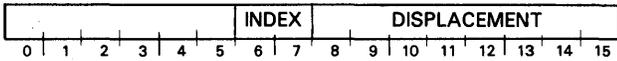
During an indexed address calculation, the CPU converts the displacement to a 15-bit intermediate result. This result is either interpreted as the indexed address without further calculation, or is interpreted as a number and is added to the contents of the program counter, accumulator 2, or accumulator 3. If the CPU adds the intermediate result to the contents of a register, the indexed address is bits 1 to 15 of the result. Bits 6 and 7 of the instruction that the CPU is executing determine how the CPU interprets the intermediate result and what operation the CPU performs on that result.

If bits 6 and 7 are both 0, the indexed address is equal to the displacement interpreted as an unsigned 8-bit number. Bits 1 to 7 of the intermediate result are all 0. Bits 8 to 15 of the intermediate result are equal to bits 8 to 15 of the instruction, respectively. The indexed address is equal to the intermediate result.

If bit 6 is 0 and bit 7 is 1, the indexed address is equal to the sum of the contents of the PC and the displacement interpreted as an 8-bit signed number. Bits 1 to 8 of the intermediate result are equal to bit 8 of the instruction, and bits 9 to 15 of the intermediate result are equal to bits 9 to 15 of the instruction, respectively. (In other words, the sign of the displacement is extended in the intermediate result.) The indexed address is equal to the sum of the intermediate result and the contents of the PC. At the time the CPU performs an indexed address calculation during the execution of an instruction, the contents of the PC is the address of the location from which the instruction has been fetched.

If bit 6 is 1 and bit 7 is 0, the indexed address is equal to the sum of the contents of AC2 and the displacement interpreted as an 8-bit signed number. The sign of the displacement is extended in the intermediate result as described above. The indexed address is the sum of the intermediate result and the contents of AC2.

If bits 6 and 7 are both 1, the indexed address is equal to the sum of the contents of AC3 and the displacement interpreted as an 8-bit signed number. The sign of the displacement is extended in the intermediate result as described above. The indexed address is the sum of the intermediate result and the contents of AC3.

mN501 INDEXED ADDRESS CALCULATION

START

INDEX BITS=00? — YES → DISPLACEMENT BITS GO TO INTERMEDIATE ADDRESS AS UNSIGNED NUMBER

NO

INDEX BITS=01? — YES → DISPLACEMENT BITS AS SIGNED NUMBER ARE ADDED TO INSTRUCTION ADDRESS

NO

INDEX BITS=10? — YES → DISPLACEMENT BITS AS SIGNED NUMBER ARE ADDED TO CONTENTS OF ACCUMULATOR 2 → LOW ORDER 15 BITS GO TO INTERMEDIATE ADDRESS

NO

INDEX BITS=11? — YES → DISPLACEMENT BITS AS SIGNED NUMBER ARE ADDED TO CONTENTS OF ACCUMULATOR 3

INDIRECT BIT=0? — YES →

NO

COUNTER = 0

RETRIEVE WORD AT INTERMEDIATE ADDRESS

COUNTER = COUNTER + 2

COUNTER > 15? — YES → HALT

NO

INTERMEDIATE ADDRESS 20-27₈ ? — YES → ADD 1 TO RETRIEVED WORD AND REPLACE. USE NEW VALUE TO CONTINUE

NO

INTERMEDIATE ADDRESS 30-37₈ ? — YES → SUBTRACT 1 FROM RETRIEVED WORD AND REPLACE. USE NEW VALUE TO CONTINUE

NO

BITS 1-15 GO TO INTERMEDIATE ADDRESS

COUNTER = COUNTER + 1

BIT 0 = 0? — NO / YES

COUNTER > 15? — NO / YES → HALT

INTERMEDIATE ADDRESS IS EFFECTIVE ADDRESS

END

DG-02403

II-15

Indirect Address Calculation

During the execution of memory reference instructions and during program interrupts, the CPU may calculate indirect addresses. When the CPU performs an indirect address calculation during the execution of a memory reference instruction, the initial indirect address is the indexed address calculated during the execution of the instruction. When the CPU performs an indirect address calculation during a program interrupt, the initial indirect address is the contents of bits 1 to 15 of the memory location through which the program interrupt is performed.

Once the CPU has calculated an initial indirect address or read one from memory, it performs the indirect address calculation as follows. The CPU reads the memory location specified by the indirect address. If bit 0 of that memory location is 0, bits 1 to 15 of the location contain the final address and indirect addressing is complete. If bit 0 of the memory location is 1, bits 1 to 15 of the location are interpreted as another indirect address, and the operation is repeated.

The CPU performs neither refresh operations nor data channel breaks during an indirect address calculation. Therefore, there is a limit on the number of memory read operations that the CPU performs during one indirect address calculation. In the CPU is a counter that is initialized at the beginning of every indirect address calculation. Every time an indirect address is read from memory, the counter is incremented by two (or by three if the indirect address is read from an autoincrementing or autodecrementing location, see below). If the indirect address calculation is not complete by the time the counter has been incremented by sixteen, the CPU halts.

Autoincrementing Locations

Memory locations whose addresses are between 20_8 and 27_8 are called autoincrementing locations.

During the calculation of indirect addresses, the CPU performs read-modify-write operations on these locations instead of read operations. The data that is written to an autoincrementing location during such a read-modify-write operation is the contents of the location incremented by one.

The address that the CPU uses to continue the indirect address calculation is bits 1 to 15 of the incremented result. The unincremented contents of bit 0 of the location determine whether the CPU interprets this address as an indirect address or a final address, as described above.

Autodecrementing Locations

Memory locations whose addresses are between 30_8 and 37_8 are called autodecrementing locations.

During the calculation of indirect addresses, the CPU performs read-modify-write operations on these locations instead of read operations, as it does on autoincrementing locations. The data that is written into an autodecrementing location during such a read-modify-write operation is the contents of the location decremented by one.

The address that the CPU uses to continue the indirect address calculation is bits 1 to 15 of the decremented result. The undecremented contents of bit 0 of the location determine whether the CPU interprets this address as an indirect address or a final address, as described above.

Memory Reference Instructions

The following instructions are memory reference instructions. During the execution of each of these instructions, an effective address is calculated and then some other operation or operations are performed on the effective address and on other operands.

The effective address is calculated as follows. The indexed address calculation specified by bits 6 to 15 is performed. If bit 5 is 0, the effective address is the resulting indexed address. If bit 5 is 1, an indirect address calculation is performed, and the effective address is the resulting final address.

The other operations performed depend on the instruction and are described below.

Jump

0	0	0	0	0	@	INDEX	DISPLACEMENT
0	1	2	3	4	5	6 7	8 9 10 11 12 13 14 15
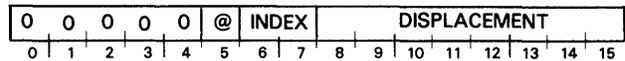
The effective address is loaded into the program counter.

Jump to Subroutine

0	0	0	0	1	@	INDEX	DISPLACEMENT
0	1	2	3	4	5	6 7	8 9 10 11 12 13 14 15
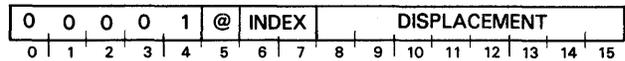
The contents of bits 1 to 15 of the program counter are loaded into bits 1 to 15 (respectively) of accumulator 3; 0 is loaded into bit 0 of accumulator 3. Then, the effective address is loaded into the program counter.

Increment and Skip If Zero
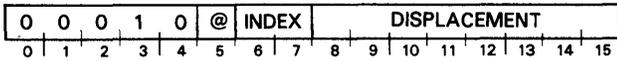
0	0	0	1	0	@	INDEX	DISPLACEMENT
0	1	2	3	4	5	6 7	8 9 10 11 12 13 14 15

A read-modify-write operation is performed on the location specified by the effective address. The data written to the location during the read-modify-write operation is the data read from the location incremented by one. If the data written to the location is 000000_8, the program counter is incremented by two. Otherwise, the program counter is incremented by one.

Decrement and Skip If Zero
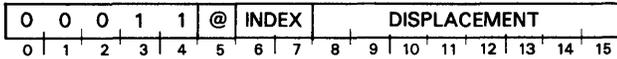
0	0	0	1	1	@	INDEX	DISPLACEMENT
0	1	2	3	4	5	6 7	8 9 10 11 12 13 14 15

A read-modify-write operation is performed on the location specified by the effective address. The data written to the location during the read-modify-write operation is the data read from the location decremented by one. If the data written to the location is 000000_8, the program counter is incremented by two. Otherwise, the program counter is incremented by one.

Load Accumulator
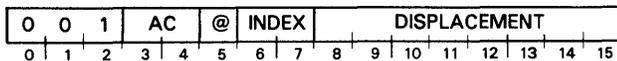
0	0	1	AC	@	INDEX	DISPLACEMENT
0	1	2	3 4	5	6 7	8 9 10 11 12 13 14 15

A read operation is performed on the memory location specified by the effective address. The data read from memory is loaded into the accumulator specified by bits 3 and 4 of the instruction; these bits specify accumulators as shown in the following table. The program counter is incremented by one.

Bit 3	Bit 4	Accumulator
0	0	accumulator 0
0	1	accumulator 1
1	0	accumulator 2
1	1	accumulator 3

Store Accumulator
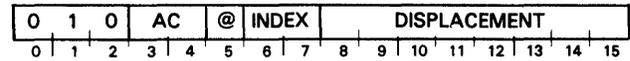
0	1	0	AC	@	INDEX	DISPLACEMENT
0	1	2	3 4	5	6 7	8 9 10 11 12 13 14 15

A write operation is performed on the memory location specified by the effective address. The data written to the memory location is the contents of the accumulator specified by bits 3 and 4 of the instruction; these bits specify accumulators as shown in the table in the description of the load-accumulator instruction. The program counter is incremented by one.

I/O Instructions

The following instructions are I/O instructions. During the execution of each of these instructions, an I/O command operation is performed; the information that is transmitted during this operation is (a copy of) the instruction. The operations performed thereafter depend on the instruction and are described below.

I/O Output

0	1	1	AC		0	
0	1	2	3 4	5 6	7	8 9 10 11 12 13 14 15
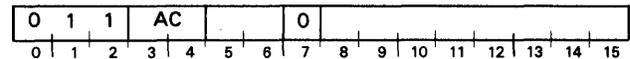
An I/O data-out operation is performed. The information transmitted is the contents of the accumulator specified by bits 3 and 4 of the instruction; these bits specify the accumulator as in a load-accumulator instruction. The program counter is incremented by 1.

The following timing diagram depicts the operations that are performed on the I/O data pins during the execution of an I/O data-out instruction. For brevity, only events that occur on I/O CLOCK and I/O INPUT are represented.
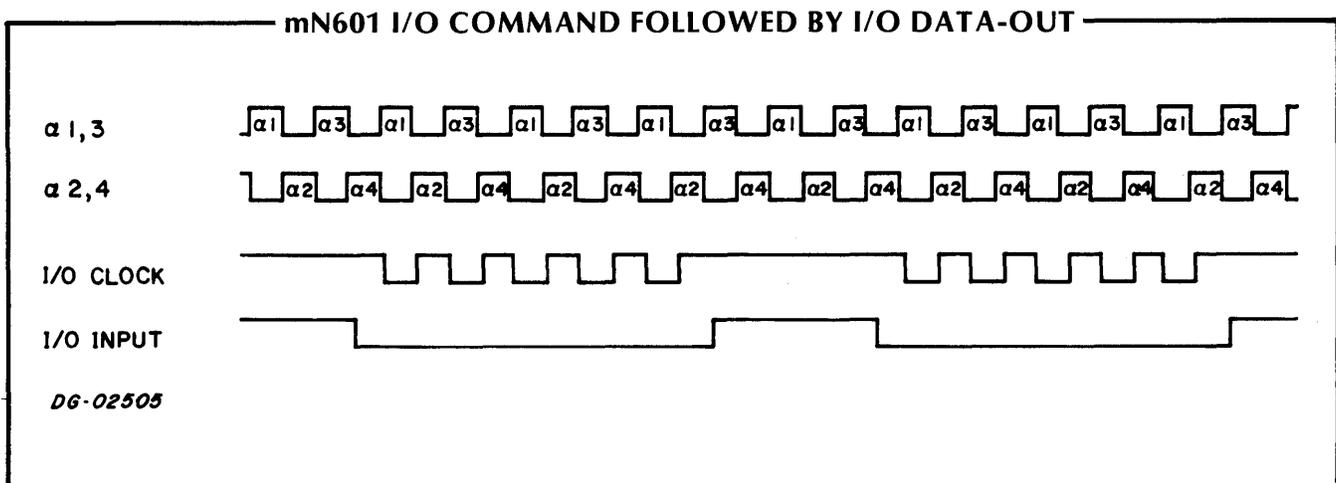
mN601 I/O COMMAND FOLLOWED BY I/O DATA-OUT

DG-02505

I/O Input

0	1	1	AC	0	0	1									
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

0	1	1	AC	0	1	1									
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

0	1	1	AC	1	0	1									
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
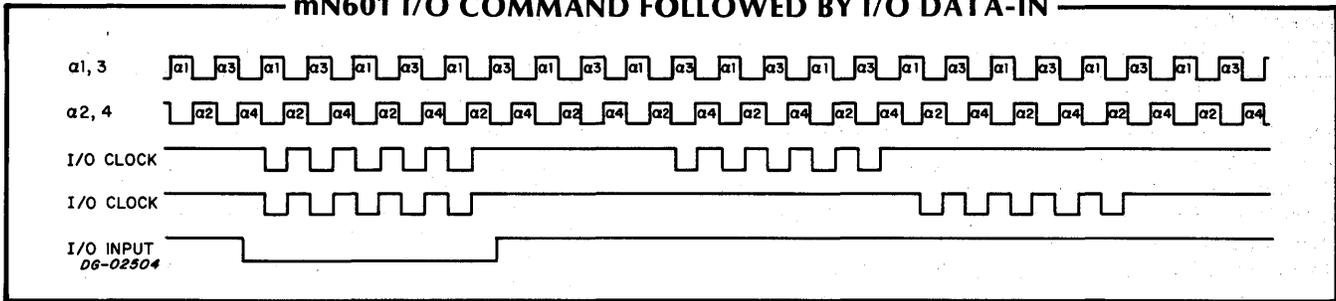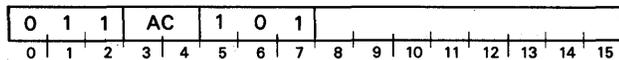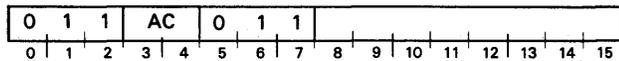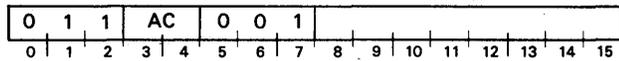
An I/O data-in operation is performed. The information received is loaded into the accumulator specified by bits 3 and 4 of the instruction; these bits specify the accumulator as in a load-accumulator instruction. The program counter is incremented by 1.

The timing diagram above depicts the operations that are performed on the I/O datta pins furing the execution of an I/0 data-in instruction. For brevity, only events that occur on I/O CLOCK and I/O INPUT are represented.

I/O Skip (Busy and Done- bars)

0	1	1			1	1	1	SKP							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
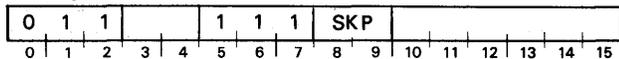
An I/O data-in operation is performed. Only bits 0 and 1 of the information received are significant; they are called $\overline{Done}$ and $\overline{Busy}$, respectively. Bits 2 to 15 are ignored. (However, bits 2 to 15 must be received, as indicated in the description of the I/O data-in operation.)

The program counter is incremented by 1 or by 2, depending on bits 8 and 9 of the instruction and on $\overline{Done}$ and $\overline{Busy}$. The following table indicates the conditions under which the program counter is incremented by 2.

Bit 8	Bit 9	Condition
0	0	$\overline{Busy} = 0$
0	1	$\overline{Busy} = 1$
1	0	$\overline{Done} = 0$
1	1	$\overline{Done} = 1$

The operations that are performed on the I/O data pins during the execution of an I/O skip instruction are indentical to those that are performed on the I/O data pins during an I/O data-in instruction.

CPU Instructions

I/O instructions in which bits 10 to 15 are all 1's are called CPU instructions. During the execution of each of these instructions, operations are performed in addition to the I/O command operation and I/O data-out or I/O data-in operation described above. The operations that are performed during the execution of these instructions are described below.

Standard CPU Instructions

0	1	1	AC	0	0	0	ION	1	1	1	1	1	1
0	1	2	3	4	5	6	7	8	9	10 11	12 13	14 15	

0	1	1	AC	0	0	1	ION	1	1	1	1	1	1

0	1	1	0 0 0 1 0	ION	1	1	1	1	1	1

0	1	1	AC	0	1	1	ION	1	1	1	1	1	1

0	1	1	AC	1	0	0	ION	1	1	1	1	1	1

0	1	1	AC	1	0	1	ION	1	1	1	1	1	1
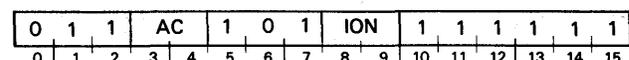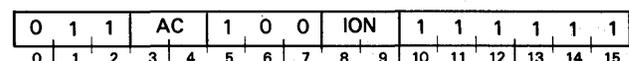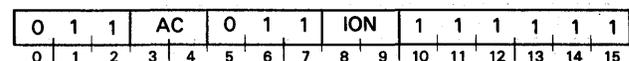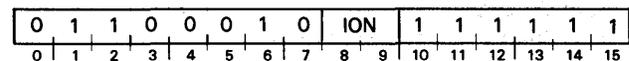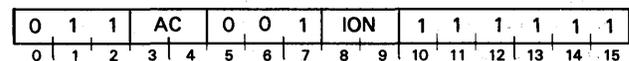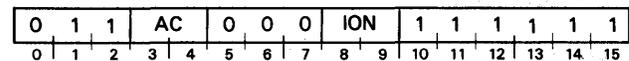
An I/O command operation and an I/O data-out or I/O data-in operation are performed, as during the execution of an I/O data-out instruction or an I/O data-in instruction.

Bits 8 and 9 of the instruction determine whether an operation is performed on the interrupt-enable bit and, if so, which operation. If bits 8 and 9 are 0 and 1, respectively, 1 is loaded into the interrupt-enable bit during the succeeding instruction execution. (If the interrupt-enable flag contains 0 during the execution of such a CPU instruction, no program interrupt occurs until one more instruction has been fetched and executed.) If bits 8 and 9 are 1 and 0, respectively, 0 is loaded into the interrupt-enable bit. (A program interrupt is never performed immediately after such a CPU instruction.)

The program counter is incremented by 1.

Real-time Clock Enable

0	1	1	0	1	0	1	0	ION	1	1	1	1	1	1
0	1	2	3	4	5	6	7	8 9	10	11	12	13	14	15

An I/O command operation and an I/O data-out operation are performed, as during the execution of an I/O data-out instruction. Bits 8 and 9 determine the operation (if any) that is performed on the interrupt-enable bit, as during the execution of a standard CPU instruction. 1 is loaded into the real-time-clock-enable bit. The program counter is incremented by 1.

Real-time Clock Disable

0	1	1	0	0	0	1	0	ION	1	1	1	1	1	1
0	1	2	3	4	5	6	7	8 9	10	11	12	13	14	15

An I/O command operation and an I/O data-out operation are performed as during the execution of an I/O data-out instruction. Bits 8 and 9 determine the operation (if any) that is performed on the interrupt-enable bit, as during the execution of a standard CPU instruction. 0 is loaded into the real-time-clock-enable bit. The program counter is incremented by 1.

> **NOTE** *The following instruction performs the same operations as the real-time-clock-enable and real-time-clock-disable instructions, except that the operation that is performed on the real-time-clock bit is not determinate.*

0	1	1	1	1	0	1	0	ION	1	1	1	1	1	1
0	1	2	3	4	5	6	7	8 9	10	11	12	13	14	15

Halt

0	1	1	AC	1	1	0		1	1	1	1	1	1
0	1	2	3 4	5	6	7	8 9	10	11	12	13	14	15

An I/O command operation and an I/O data-out operation are performed, as during the execution of an I/O data-out instruction. 1 is loaded into the interrupt-enable bit. The program counter is incremented by 1. The CPU is halted. (I.e., it does not fetch and execute another instruction until it has performed a program interrupt.)

CPU Skip

0	1	1		1	1	1	SKP	1	1	1	1	1	1
0	1	2	3 4	5	6	7	8 9	10	11	12	13	14	15

An I/O command operation and an I/O data-in operation are performed, as during the execution of an I/O skip instruction.

The program counter is incremented by 1 or by 2, depending on bits 8 and 9 of the instruction and on the contents of the interrupt-enable bit. The following table indicates the conditions under which the program counter is incremented by 2.

Bit 8	Bit 9	Condition
0	0	when interrupt-enable bit contains 1
0	1	when interrupt-enable bit contains 0
1	0	never
1	1	always

Multiply and Divide Instructions

The following instructions are multiply and divide instructions. Although they have the form of I/O instructions, the operations that are performed during their execution are different from those performed during the execution of any I/O instruction. An I/O command operation is performed during the execution of these instructions, but it is never followed by an I/O data-out or I/O data-in operation.

Multiply

0	1	1	1	0	1	1	0	1	1	0	0	0	0	0	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

The product of the contents of accumulator 1 and accumulator 2 is added to the contents of accumulator 0. The contents of the accumulators are interpreted as 16-bit unsigned operands. The result is a 32-bit unsigned number. The sixteen most significant bits of the result are loaded into accumulator 1; the sixteen least significant bits of the result are loaded into accumulator 0. The contents of the program counter are incremented by 1.

Divide

0	1	1	1	0	1	1	0	0	1	0	0	0	0	0	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Unless there is an overflow condition, the contents of accumulators 1 and 0 are divided by the number in accumulator 2. The contents of accumulator 1 are interpreted as the sixteen most significant bits of a 32-bit unsigned dividend; the contents of accumulator 0 are interpreted as the sixteen least significant bits of that dividend. The contents of accumulator 2 are interpreted as a 16-bit unsigned divisor. A 16-bit unsigned quotient is loaded into accumulator 1; a 16-bit unsigned remainder is loaded into accumulator 2.

There is an overflow condition if the contents of accumulator 2 are greater than the contents of accumulator 1 before the division is performed. This condition indicates that if the division were performed, the quotient would be more than sixteen bits. If there is an overflow condition, 1 is loaded into the carry bit and the division is not performed.

In either case, the contents of the program counter are incremented by 1.

Stack Instructions

The following instructions are stack instructions. Although they have the same form as I/O instructions, the operations that are performed during their execution are different from those performed during any I/O instruction. An I/O command operation is performed during the execution of these instructions, but it is never followed by an I/O data-out operation or an I/O data-in operation. The other operations that are performed during the execution of these instructions are described below.

Move To Frame Pointer
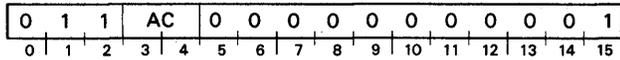
0	1	1	AC	0	0	0	0	0	0	0	0	0	0	1
0	1	2	3 4	5	6	7	8	9	10	11	12	13	14	15

The contents of bits 1 to 15 of the accumulator specified by bits 3 and 4 of the instruction are loaded into bits 1 to 15 (respectively) of the frame pointer. Bits 3 and 4 of the instruction specify accumulators as in a load-accumulator instruction. The contents of the program counter are incremented by 1.

Move From Frame Pointer
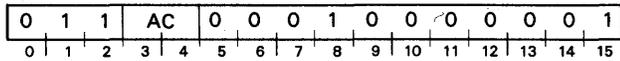
0	1	1	AC	0	0	0	1	0	0	0	0	0	0	1
0	1	2	3 4	5	6	7	8	9	10	11	12	13	14	15

The contents of bits 1 to 15 of the frame pointer are loaded into bits 1 to 15 (respectively) of the accumulator specified by bits 3 and 4 of the instruction; 0 is loaded into bit 0 of the specified accumulator. Bits 3 and 4 of the instruction specify accumulators as in a load-accumulator instruction. The contents of the program counter are incremented by 1.

Move To Stack Pointer
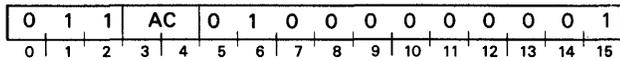
0	1	1	AC	0	1	0	0	0	0	0	0	0	0	1
0	1	2	3 4	5	6	7	8	9	10	11	12	13	14	15

The contents of bits 1 to 15 of the accumulator specified by bits 3 and 4 of the instruction are loaded into bits 1 to 15 (respectively) of the stack pointer. Bits 3 and 4 of the in-struction specify accumulators as in a load-accumulator instruction. The contents of the program counter are incremented by 1.

Move From Stack Pointer

0	1	1	AC	0	1	0	1	0	0	0	0	0	0	1
0	1	2	3 4	5	6	7	8	9	10	11	12	13	14	15
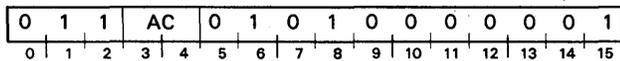
The contents of bits 1 to 15 of the stack pointer are loaded into bits 1 to 15 (respectively) of the accumulator specified by bits 3 and 4 of the instruction; 0 is loaded into bit 0 of the specified accumulator. Bits 3 and 4 of the instruction specify accumulators as in a load-accumulator instruction. The contents of the program counter are incremented by 1.

Push

0	1	1	AC	0	1	1	0	0	0	0	0	0	0	1
0	1	2	3 4	5	6	7	8	9	10	11	12	13	14	15
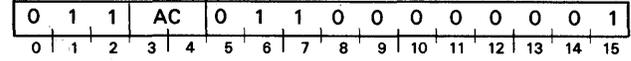
The contents of the stack pointer are incremented by 1. A write operation is performed on the memory location whose address is contained in the stack pointer. The data written to the memory location is the contents of the accumulator specified by bits 3 and 4 of the instruction; bits 3 and 4 of the instruction specify accumulators as in a load-accumulator instruction. The contents of the program counter are incremented by 1. If the new contents of bits 8 to 15 of the stack pointer are 000_8 (i.e., if the stack has passed a 256_{10} -word boundary), 1 is loaded into the stack-overflow request bit.

Pop
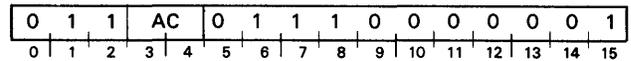
0	1	1	AC	0	1	1	1	0	0	0	0	0	0	1
0	1	2	3 4	5	6	7	8	9	10	11	12	13	14	15

A read operation is performed on the memory location whose address is contained in the stack pointer. The data read from the location is loaded into the accumulator specified by bits 3 and 4 of the instruction; bits 3 and 4 of the instruction specify accumulators as in a load-accumulator instruction. The contents of the stack pointer are decremented by 1. The contents of the program counter are incremented by 1.

Save

0	1	1		1	0	1	0	0	0	0	0	0	0	1
0	1	2	3 4	5	6	7	8	9	10	11	12	13	14	15
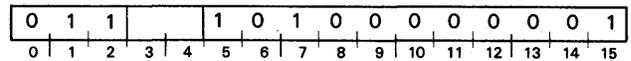
The stack pointer is incremented by 1 five times. After the stack pointer is incremented each time, a write operation is performed on the memory location whose address is in the stack pointer at that time.

During the first, second and third write operations, the contents of accumulator 0, the contents of accumulator 1 and the contents of accumulator 2, respectively, are written to the specified memory locations. During the fourth write operation, 0 is transferred to bit 0 of the specified memory location and the contents of bits 1 to 15 of the frame pointer are transferred to bits 1 to 15 of the specified memory location. During the fifth write operation, the contents of the carry bit are transferred to bit 0 of the specified memory location and the contents of bits 1 to 15 of the accumulator 3 are transferred to bits 1 to 15 of the specified memory location.

The contents of bits 1 to 15 of the frame pointer are loaded into bits 1 to 15 of the stack pointer and bits 1 to 15 of accumulator 3; 0 is loaded into bit 0 of accumulator 3.

The contents of the program counter are incremented by 1.

If the incremented contents of bits 8 to 15 of the stack pointer are 000_8 at any time during the execution of the instruction, 1 is loaded into the stack-overflow-request bit.

Return

0	1	1	AC		1	0	1	1	0	0	0	0	0	0	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

The contents of the frame pointer are loaded into the stack pointer.

The stack pointer is decremented by 1 five times. Just before it is decremented each time, a read operation is performed on the memory location whose address is contained in the stack pointer at that time.

Bit 0 of the data read during the first read operation is loaded into the carry bit; bits 1 to 15 of that data are loaded into bits 1 to 15 of the program counter (respectively).

Bit 0 of the data read during the second read operation is ignored; bits 1 to 15 are loaded into bits 1 to 15 of accumulator 3 (respectively).

The data read during the third, fourth and fifth read operations is loaded into accumulator 2, accumulator 1 and accumulator 0 (respectively).

Two-accumulator Multiple-operation Instructions

The following instructions are two-accumulator multiple-operation instructions. The sequence of operations performed during the execution of each of these instructions is determined by bits 1 to 15 of the instruction. These bits are divided into seven groups, as shown.

1	ACS		ACD		OP			SH		C		N	SKP		
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Bits 1 and 2 are called the source accumulator field. They specify an accumulator (called the source accumulator).

Bits 3 and 4 are called the destination accumulator field. They specify an accumulator (called the destination accumulator).

The contents of the source and destination accumulator fields specify accumulators as shown in the following table.

Bit 1	Bit 2	Source Accumulator
Bit 3	Bit 4	Destination Accumulator
0	0	accumulator 0
0	1	accumulator 1
1	0	accumulator 2
1	1	accumulator 3

Bits 10 and 11 are called the carry field. They specify a base carry. As shown in the following table, they may specify a value or they may specify a function of the contents of the carry bit. (In this table, C represents the contents of the carry bit.)

Bit 10	Bit 11	Base Carry
0	0	C
0	1	0
1	0	1
1	1	ones-complement of C

Bits 5 to 7 are called the operation code field. The contents of the operation code field specify an operation that is performed on the contents of the source accumulator, the contents of the destination accumulator and the base carry. The operation yields a sixteen-bit arithmetic/logical (A/L) result and a shift-carry-in. Each operation code has a name; the operation codes and their names are listed in the following table.

Bit 5	Bit 6	Bit 7	Operation Code Name
0	0	0	COM
0	0	1	NEG
0	1	0	MOV
0	1	1	INC
1	0	0	ADC
1	0	1	SUB
1	1	0	ADD
1	1	1	AND

The operation specified by each operation code is described below.

COM

The A/L result is the ones-complement of the contents of the source accumulator. The shift-carry-in is the base carry.

NEG

The A/L result is the twos-complement of the contents of the source accumulator. If the result is 000000_8, the shift-carry-in is the ones-complement of the base carry; otherwise, the shift-carry-in is the base carry.

MOV

The A/L result is the contents of the source accumulator. The shift-carry-in is the base carry.

INC

The A/L result is the sixteen least significant bits of the contents of the source accumulator incremented by one. If the A/L result is 000000_8, the shift-carry-in is the ones-complement of the base carry; otherwise, the shift-carry-in is the base carry.

ADC

The A/L result is the sixteen least significant bits of the sum of the ones-complement of the contents of the source accumulator and the contents of the destination accumulator. If the contents of the destination accumulator interpreted as an unsigned number are greater than the contents of the source accumulator interpreted as an unsigned number, the shift-carry-in is the ones-complement of the base carry; otherwise, the shift-carry-in is the base carry.

SUB

The A/L result is the sixteen least significant bits of the sum of the twos-complement of the contents of the source accumulator and the contents of the destination accumulator. If the contents of the destination accumulator interpreted as an unsigned number are greater than or equal to the contents of the source accumulator interpreted as an unsigned number, the shift-carry-in is the ones-complement of the base carry; otherwise, the shift-carry-in is base carry.

ADD

The A/L result is the sixteen least significant bits of the sum of the contents of the source accumulator and the contents of the destination accumulator. If there is a carry out of the most significant bits during the addition, the shift-carry-in is the ones-complement of the base carry; otherwise, the shift-carry-in is the base carry.

AND

The A/L result is the bitwise logical product (AND) of the contents of the source accumulator and the contents of the destination accumulator. The shift-carry-in is the base carry.

Bits 8 and 9 are called the shift code field. They specify a shift operation that is performed on the result and shift-carry-in produced by the operation specified by bits 5 to 7. The shift operation yields a 16-bit shifted result and a shift-carry-out. The shift codes and their names are listed in the following table.

Bit 8	Bit 9	Shift Code Name
0	0	none
0	1	L
1	0	R
1	1	S

The shift operation specified by each shift code is described below.

None - The shifted result is the arithmetic/logical result, and the shift-carry-out is the shift-carry-in.

DG-02509
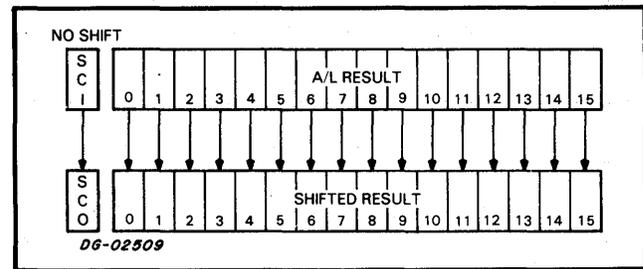
L - The shifted result and shift-carry-out are the arithmetic/logical result shifted and shift-carry-in rotated left one bit, as shown in the following diagram.

DG-02510

II-22
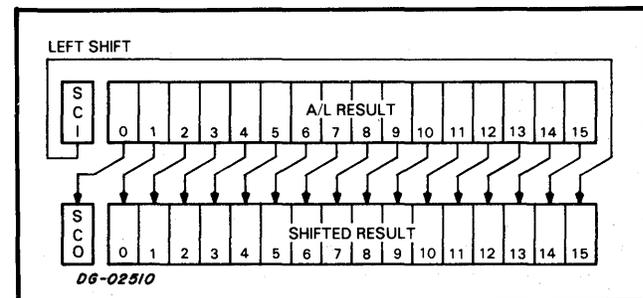
R - The shifted result and shift-carry-out are the arithmetic/logical result and shift-carry-in rotated right one bit, as shown in the following diagram.

RIGHT SHIFT

DG-0251I
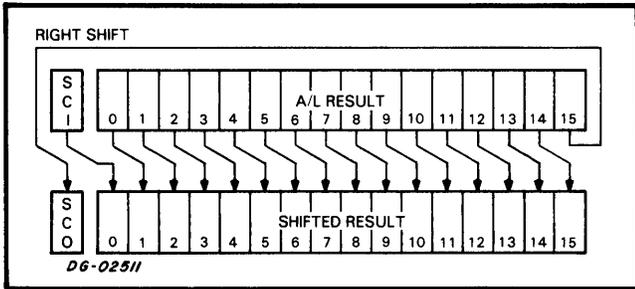
S - The shifted result is the arithmetic result rotated eights bits (i.e., the left and right bytes are swapped), as shown. The shift-carry-out is the shift-carry-in.

SWAP

DG-02513
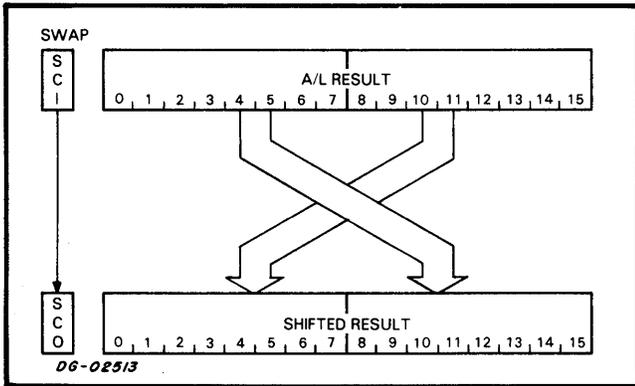
Bit 12 is the no-load bit. If this bit is 0, the shifted result is loaded into the destination accumulator and the shift-carry-out is loaded into the carry bit. Otherwise, the destination accumulator and carry bit are not loaded.

Bits 13 to 15 are the skip code field. They specify a skip condition. If the specified condition is met, the program counter is incremented by two; otherwise, the program counter is incremented by 1. The skip codes and the conditions they specify are listed in the following table. In this table, C represents the shift-carry-out, and R represents the shifted result.

bit 13	bit 14	bit 15	
0	0	0	never
0	0	1	always
0	1	0	if C is 0
0	1	1	if C is 1
1	0	0	if R is 000000_8
1	0	1	if R is not 000000_8
1	1	0	if C is 0 or R is 000000_8
1	1	1	if C is 1 and R is not 000000_8

Trap Instructions

The following instructions are trap instructions. They have the form of two-accumulator multiple-operation instructions that specify that the carry bit and destination accumulator are not to be loaded and the program counter is to be incremented by 1 (i.e., no load and no skip); however, the operations that are performed during their execution are different from any two-accumulator multiple-operation instruction.
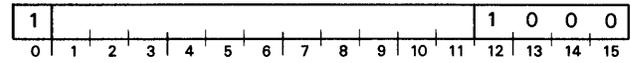
A write operation is performed on the memory loocation whose address is 46_8. Bit 0 of the data written to this location is 0; bits 1 to 15 are bits 1 to 15 (respectively) of the address of the memory location from which the instruction has been fetched.

A read operation is perfomed on the memory location whose address is 47_8. If bit 0 of the contents of this location is 0, bits 1 to 15 of the contents of the location are loaded into bits 1 to 15 (respectively) of the program counter. If bit 0 of the contents of the memory location is 1, an indirect address calculation is performed. The initial indirect address is the contents of bits 1 to 15 of the memory location. The final address resulting from this calculation is loaded into the program counter.

Program Interrupts

Program interrupts are sequences of operations during which the CPU writes the contents of the program counter to a memory location and loads the program counter with the contents of another memory location. They are performed at the request of peripherals, at the request of the real-time clock in the CPU (see the description of the real-time clock) and on the occurence of a stack overflow condition (see the description of the push and save instructions).

The CPU performs three types of program interrupts: external interrupts, real-time clock interrupts and stack overflow interrupts. External interrupts are performed through location 1; real-time clock interrupts are performed through location 2; and stack overflow interrupts are performed through location 3.

The CPU performs a program interrupt as follows. It loads 0 into the interrupt-enable flag, writes the contents of the program counter into memory location 0 and reads the memory location through which the interrupt is to be performed. If bit 0 of that memory location contains 0, bits 1 to 15 of the location are loaded into the program counter. If bit 0 of the location contains 1, the contents of the location are interpreted as an indirect address, an indirect address calculation is performed, and the final address resulting from that calculation is loaded into the program counter. If the program interrupt is a

real-time-clock interrupt, 0 is loaded into the real-time-clock-request bit. If the program interrupt is a stack-overflow interrupt, 0 is loaded into the stack-overflow-request bit.

The CPU performs program interrupts only when it is halted and when it is about to fetch an instruction and the interrupt-enable flag contains 1. At these times, the CPU performs an external interrupt if EXT INT is at low level (i.e., when a peripheral is requesting an interrupt). It performs a real-time clock interrupt if the real-time clock-enable bit contains 1 and the real-time-clock-request bit contains 1 (i.e., when the real-time-clock is requesting an interrupt). It performs a stack overflow interrupt if the stack-overflow-request bit contains 1 (i.e., a stack-overflow condition has occurred since the last stack-overflow interrupt).

The three types of interrupts are arranged in order of priority (from highest to lowest) as follows: stack overflow interrupts, real-time clock interrupts, external interrupts. When conditions that imply more than one type of interrupt arise concurrently, the CPU performs the highest priority interrupt first.

Data Channel Breaks

Data channel breaks are sequences of operations during which the CPU transfers data between a memory location and a peripheral. They are performed at the request of peripherals, and allow peripherals to transfer data to or from memory without recourse to an alteration of program flow in the CPU.

There are two types of data channel breaks: those during which data is transferred to a memory location from a peripheral, and those during which data is transferred from a memory location to a peripheral. The type of a data channel break is determined by the peripheral after the CPU has begun the data channel break.

The CPU begins every data channel break by performing the same operations. It performs a data-channel-acknowledge, an I/O data-in operation, and then a memory operation. It is expected that in

response to the data-channel-acknowledge code transmitted during the data-channel-acknowledge operation, some peripheral performs an I/O data-out operation to transmit sixteen bits of data (called a control word) to the CPU via the I/O data pins while the CPU is performing the I/O data-in operation. The CPU interprets bit 0 of the control word as a 1-bit indicator of the direction of data transfer and bits 1 to 15 of the control word as a 15-bit address specifying the memory location to which or from which data is to be transferred. (The direction indicator is called the mode bit, and the address is called the data channel address.) The address transferred to memory during the memory operation is the data channel address. The memory operation is a read operation or a read-modify-write operation; the type of memory operation depends on the type of data channel break that the CPU performs.

The CPU determines which type of data channel break to perform from the data channel mode bit.

If the mode bit is 0, the CPU performs a read operation and then an I/O data-out operation. The address transferred to memory during the read operation is the data channel address. The data that is transferred from the CPU during the I/O data-out operation is the data read from memory.

If the mode bit is 1, the CPU performs a read-modify-write operation and simultaneously performs another I/O data-in operation. The address transferred to memory during the read-modify-write operation is the data channel address. The data read from memory is not used. The data written to memory during the read-modify-write operation is the data received during the second I/O data-in operation. It is expected that a peripheral that has transmitted a mode bit equal to 1 during a data channel transfer, performs an I/O data-out operation to transmit sixteen bits of data to the CPU via the I/O port while the CPU is performing the latter I/O data-in operation. The following timing diagrams depict the operations that are performed on the PG, SAEG and WEG (to indicate the memory operations performed) and I/O CLOCK and I/O INPUT (to indicate I/O operations) during a data channel break.

mN601 DATA TRANSFER FROM PERIPHERAL TO MEMORY
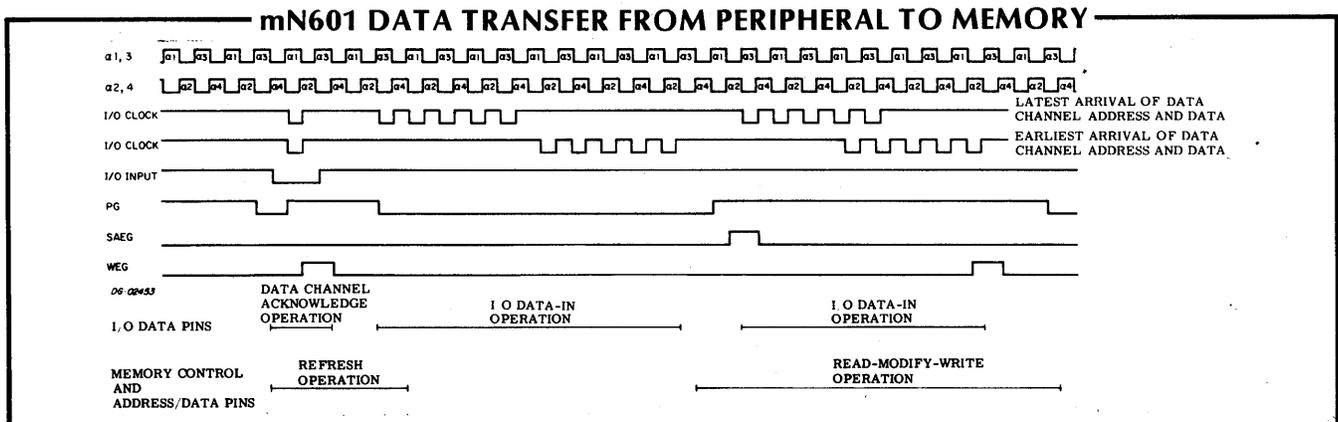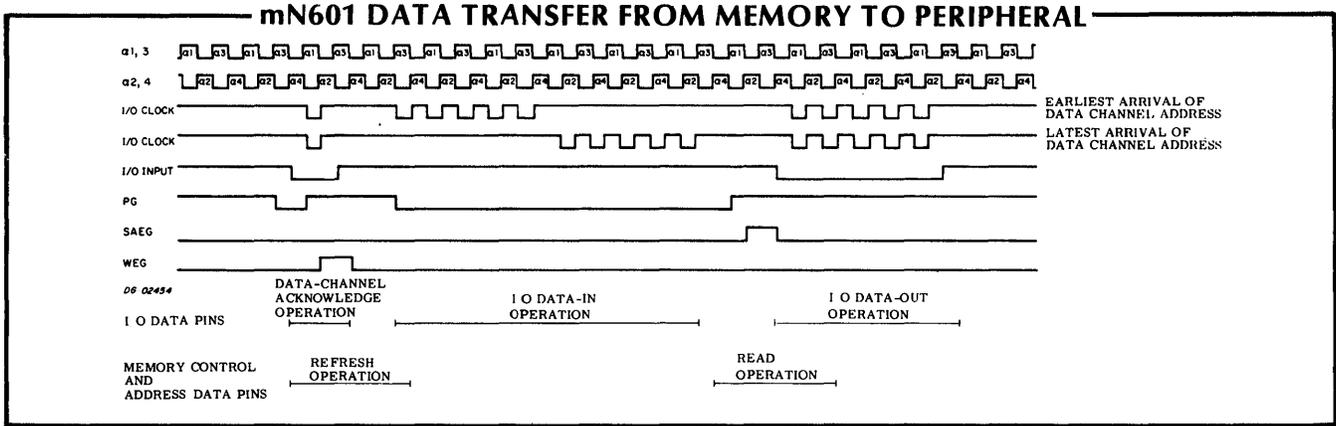
CPU may perform data channel breaks: 1) when it is about to fetch an instruction; 2) during the execution of some instructions; or 3) when it is halted. At these times, it performs a data channel break if the pin DCH INT is at low level.

If $\overline{\text{DCH INT}}$ is still at low level at the end of a data channel break, the CPU performs another data channel break.

If $\overline{\text{DCH INT}}$ is no longer at low level at the end of a data channel break, the CPU returns to the sequence of operations it was performing prior to the data channel break. If it was about to fetch an instruction, it fetches the instruction or performs a program interrupt. If it was executing an instruction, it continues with the execution of that instruction. If it was halted, it is halted again.

The delay between the time when $\overline{\text{DCH INT}}$ goes to low level and the time when the CPU performs a data channel break depends on the operations that the CPU is performing. If the CPU does not perform indirect address calculations, the longest possible delay occurs during the execution of a save instruction; this delay is 72 alpha cycles. The CPU does not perform data channel breaks during indirect address calculations.

Reset

When the CPU is reset, 0 is loaded into the interrupt-enable, real-time-clock-enable and stack-overflow request bits. After the CPU is reset, it is halted.

The CPU is reset if I/O CLOCK is at low level for fifteen consecutive alpha cycles or more. If I/O CLOCK is at low level for 8-15 consecutive alpha cycles, the CPU may or may not be reset; if I/O CLOCK is at low level for fewer than eight alpha cycles, the CPU is not reset.

The cpu is halted when I/O CLOCK returns to high level after the CPU is reset.

Real-time Clock

The CPU has a real-time-clock facility to perform program interrupts at regular intervals.

Whenever the CPU is operating and is not reset, 1 is loaded into the real-time-clock-request bit every 20,000 alpha cycles (every 2.4 milliseconds with alpha 1,3 and alpha 2,4 at 8.333MHz).

As indicated in the description of program interrupts, if the interrupt-enable and real-time-clock-enable bits both contain 1, a real-time-clock interrupt is performed whenever 1 is loaded into the real-time-clock-request bit.

During a real-time-clock interrupt, 0 is loaded into the real-time-clock-request bit so that another real-time-clock interrupt is not performed for another 2.4 milliseconds.

Memory Refreshing

To facilitate the use of memory elements composed of dynamic RAMs in the microNOVA computer system, the CPU has a "hidden refresh" facility.

From time to time when the CPU is operating and is not reset, it performs a refresh operation on the memory locations specified by the contents of the refresh address counter. A refresh operation is performed only at times when it does not delay a memory operation that is part of an instruction execution, program interrupt or data channel break (hence the term "hidden refresh").

A new refresh address is loaded into the refresh address counter every 312 alpha cycles during the operation of the CPU, so that the refresh address counter contains each of the sixty-four refresh addresses at some time during any interval of 20,000 alpha cycles.

The loading of the refresh address counter is not synchronized with the performing of refresh operations. However, the CPU performs refresh operations frequently enough that during one interval of 20,000 alpha cycles, every memory location is refreshed at least once. (Some locations may be refreshed several times.)

Power-up

When the CPU is powered up, it performs no operation as long as $\overline{CLAMP}$ remains at low level. When $\overline{CLAMP}$ goes to high level, 0 is loaded into the real-time-clock-enable bit and the stack-overflow-request bit, 1 is loaded into the interrupt-enable bit, and the CPU is halted. Thereafter, $\overline{CLAMP}$ has no effect on the operation of the CPU until the next time it is powered up.

> **NOTE** *The CPU may be damaged if V_{BB} is at a positive voltage with respect to any other pin of the CPU. Because this condition is most likely to arise during power up, special precautions should be taken to ensure that the voltage at V_{BB} is within its specified operating range before power is applied to any other pin.*

SECTION III

mN606
4K DYNAMIC RAM

- **PACKAGE**

- **PIN NAMES AND NUMBERS**

- **DC (STATIC) CHARACTERISTICS**

- **FUNCTIONAL DESCRIPTION**

PACKAGE

The mN 606 integrated circuit is supplied in a 20-pin plastic dual in-line package (DIP).

PIN NUMBERS AND NAMES

V_{BB}	1	20 V_{SS}
A_3	2	19 P (CLOCK)
A_2	3	18 WE
A_{10}	4	17 D/I
A_{11}	5	16 $\overline{D/O}$
A_7	6	15 $\overline{CS}$
A_8	7	14 A_6
A_9	8	13 A_1
A_4	9	12 A_0
A_5	10	11 V_{DD}

DG-02355 DG-02361
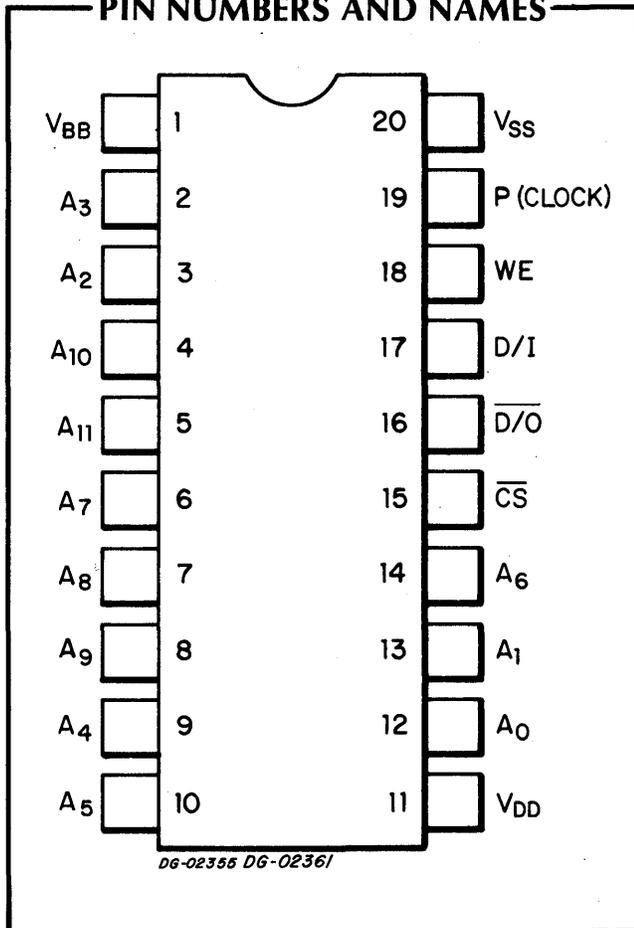
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range V_{BB}	-2 to -7 Volts
Supply Voltage Range V_{DD}	-0.3 to +17 Volts
Clock Input Voltage Range V_{ICLK}	-0.3 to +17 Volts
All Other Inputs V_I	-0.3 to +7 Volts
Output Voltage Range V_O	0 to 4 Volts
Operating Temperature Range T_A	0 to 70 °C
Storage Temperature Range T_{stg}	-55 to +125 °C
Average Power Dissipation	0.7 Watts

NOTES *All voltages in this document are referenced to V_{SS} (ground).*

Subjecting a circuit to conditions either outside these limits or at these limits for an extended period of time may cause irreparable damage to the circuit. As such, these ratings are not intended to be used during the operation of the circuit. Operating specifications are given in the DC (STATIC) CHARACTERISTICS TABLE.

OPERATING SPECIFICATIONS

T_A range __0__ to __70__ °C I_{DD} = __26__ mAmps Average

V_{DD} = __14 ± 1.0__ Volts I_{BB} = __-0.15__ mAmps Average

V_{BB} = __-4.25 ± .25__ Volts I_{GND} = __-26__ mAmps Average

GND = __0 ± 0.0__ Volts

CHARACTERISTIC	SYMBOL	UNITS	PINS	LIMITS MIN.	LIMITS MAX.
INPUT LOW VOLTAGE	V_{IL}	Volts	P (CLOCK), A<0-11> $\overline{CS}$, WE, D I	-0.5	+0.8
INPUT CURRENT FOR LOW STATE	I_{IL}	mAmps	P(CLOCK) A 0-11 $\overline{CS}$, WE, DI	-	+0.003
INPUT HIGH VOLTAGE	V_{IH}	Volts	P (CLOCK)	+13.0	+15.5
			A 0-11 $\overline{CS}$, WE, D I	+4.0	+6.0
INPUT CURRENT FOR HIGH STATE	I_{IH}	mAmps	P(CLOCK)	-	+0.3
			A 0-11 $\overline{CS}$, WE, D I		+.003
OUTPUT LOW VOLTAGE	V_{OL}	Volts	$\overline{D O}$	-	+2.4
OUTPUT CURRENT FOR LOW STATE	I_{OL}	mAmps	$\overline{D O}$	1.5	7.0
OUTPUT HIGH VOLTAGE	V_{OH}	Volts	$\overline{D O}$	-2.6	-
OUTPUT CURRENT FOR HIGH STATE	I_{OH}	mAmps	$\overline{D O}$	0	0.003
INPUT CAPACITANCE	C_I	pF	P(CLOCK)		23
			A 0-11 $\overline{CS}$, WE, D I		7

NOTE

Logic "1" is defined as the more positive voltage as are the maximum figures given under voltage limits. Logic "0" is defined as the more negative voltage as are the minimum figures given under voltage limits.

Positive current, in the conventional sense, is defined as flowing into the pin.

On power-up, V_{BB} must be within its specified operating range (with respect to V_{SS}) before any of the other power supply voltages are applied to the circuit.

FUNCTIONAL DESCRIPTION

The 4K dynamic RAM is a 4096-bit dynamic random-access memory. It reads and writes each bit individually and refreshes sixty-four bits simultaneously.

Pins

The pins of the memory and brief descriptions of their functions are given in the following table.

Pin	function
P	clock input
CS	chip select
WE	write-enable
A[0-11]	address inputs
D/O	data output
D/I	data input

Memory Operations

A memory operation is initiated when P goes to high level. At this time, the address on A[0-11] is sampled. A change in the electrical levels of these pins after they are sampled does not affect the operation of the RAM.

The operation that the RAM performs depends on the level at CS at the time P rises. If CS is low, a read operation is initiated. The address sampled on the rising edge of P selects one data bit in the memory. Soon after the address is sampled, D/O assumes the low state and then assumes the high state or the low state as required to reflect the contents of the selected data bit.

Once a read operation is initiated, it may be converted to a read followed by a write by a high level at WE. A rising edge of WE places D/O in the high state. A falling edge of WE loads the selected data bit from D/I. D/I and D/O have the same sense; that is, if D/I is at high level when a data bit is loaded, D/O assumes the high state when the data bit is read.

When P rises and CS is high, a refresh operation is initiated. The address sampled on the rising edge of P selects sixty-four data bits in the memory. D/O remains in the high impedance state for the duration of the memory refresh operation.

Once a refresh operation is initiated, WE determines whether or not the sixty-four selected data bits are refreshed. A falling edge of WE refreshes the selected data bits. A bit is refreshed if the address bits most recently latched from [A 6-11] are identical to the address bits that would be latched from A[6-11] in order to select the bit for reading or writing. The contents of every bit remain unchanged during a refresh operation; no bit is loaded from D/I.

The memory operation is concluded when P goes to low level. After a read operation, the falling edge of P may occur as soon as the data has been read. After a write or refresh operation, there is a minimum delay between the falling edges of WE and P. There is also a minimum delay between the falling edge of P that concludes a memory operation and the rising edge of P that initiates the next one.

The following timing diagrams depict the events that occur on the pins of the RAM during the memory operations described above.

REFRESH OPERATION
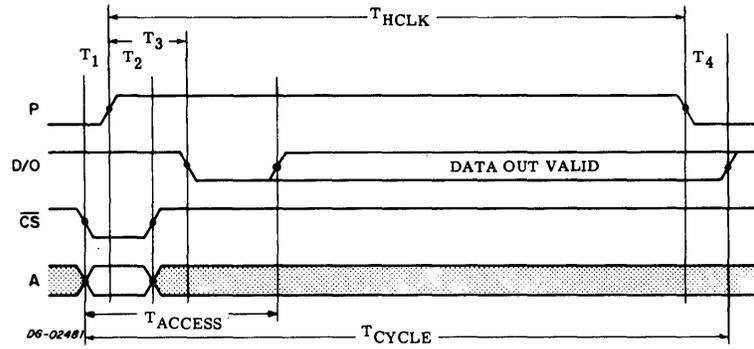
Conditions:

V_{BB} = -4.25 Volts
V_{SS} = 0 Volts
V_{DD} = +14 Volts

P(CLOCK) Input Rise Time 10 to 20ns
P(CLOCK) Input Fall Time 10 to 20ns
All Other Input Fall Times 5 to 15ns
All Other Input Rise Times 5 to 15ns

	MIN (ns)	MAX (ns)
T_1	15	-
T_2	30	-
T_3	80	-
T_4	145	-
T_5	145	-
T_6	145	-
T_{HCLK}	-	2000
T_{CYCLE}	-	2.4ms

READ OPERATION

Conditions:

V_{BB} = -4.25 Volts
V_{SS} = 0 Volts
V_{DD} = +14 Volts

P(CLOCK)	Input Rise Time	10 to 20ns
P(CLOCK)	Input Fall Time	10 to 20ns
All Other	Input Fall Times	5 to 15ns
All other	Input Rise Times	5 to 15ns

	MIN (ns)	MAX (ns)
T_1	15	-
T_2	30	-
T_3	55	-
T_4	0	-
T_{ACCESS}	-	160
T_{HCLK}	-	2000
T_{CYCLE}	-	2.4ms
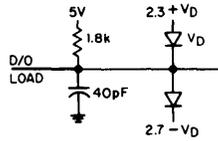
WRITE OPERATION
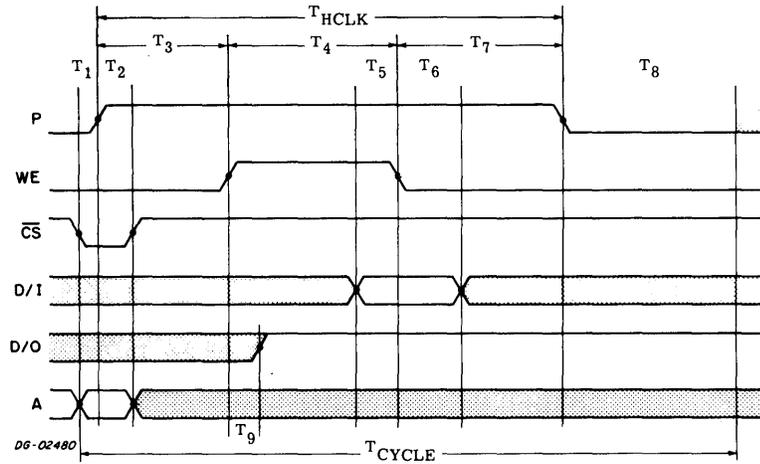
Conditions:

V_{BB} = -4.25 Volts
V_{SS} = 0 Volts
V_{DD} = +14 Volts

P(CLOCK)	Input Rise Time	10 to 20ns
P(CLOCK)	Input Fall Time	10 to 20ns
All Other	Input Fall Times	5 to 15ns
All Other	Input Rise Times	5 to 15ns

	MIN (ns)	MAX (ns)
T_1	15	-
T_2	30	-
T_3	135	-
T_4	145	-
T_5	35	-
T_6	55	-
T_7	145	-
T_8	145	-
T_9	25	-
T_{HCLK}	-	2000
T_{CYCLE}	-	2.4ms

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SECTION IV

mN603
I/O CONTROLLER (IOC)

- PACKAGE

- PIN NAMES AND NUMBERS

- DC (STATIC) CHARACTERISTICS

- FUNCTIONAL DESCRIPTION

PACKAGE

The mN603 integrated circuit is supplied in a 40-pin ceramic dual in-line package (DIP).

PIN NUMBERS AND NAMES

V_BB	1	40	V_GG
PHASEB	2	39	V_DD
PHASEA	3	38	$\overline{DONE}$
D0	4	37	$\overline{BUSY}$
D1	5	36	$\overline{INT\ SYNC}$
D2	6	35	$\overline{INTR}$
D3	7	34	$\overline{DCHR}$
D4	8	33	DCHP
D5	9	32	$\overline{DCH\ SYNC}$
D6	10	31	INTP
D7	11	30	I/O CLOCK
D8	12	29	I/O DATA2
D9	13	28	I/O DATA1
D10	14	27	I/O INPUT
D11	15	26	F3
D12	16	25	F2
D13	17	24	F1
D14	18	23	F0
D15	19	22	$\overline{F\ STROBE}$
V_SS (GND)	20	21	V_CC

DG-02131 DG-02364

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range V_{BB}	-2 to -7	Volts
Supply Voltage Range V_{CC}	-0.3 to +7	Volts
Supply Voltage Range V_{DD}	-0.3 to +13	Volts
Supply Voltage Range V_{GG}	-0.3 to +17	Volts
Input Voltage Range V_I	-0.3 to +7	Volts
Output Current Range I_I	0 to 6	mAmps
Operating Temperature Range T_A	0 to +70	°C
Storage Temperature Range T_{stg}	-55 to +125	°C
Average Power Dissipation	1	Watt

NOTES *All voltages in this document are referenced to V_{SS} (ground).*

*Subjecting a circuit to conditions either outside these limits or at these limits for an extended period of time may cause irreparable damage to the circuit. As such, these ratings are not intended to be used during the operation of the circuit. Operating specifications are given in the DC (STATIC) CHARACTERISTICS TABLE.

DC (STATIC) CHARACTERISTICS
mN603

OPERATING SPECIFICATIONS

T_A range __0__ to __70__ $^\circ$C V_{GG} = 14 ± 1.0 Volts I_{CC} = __20__ mAmps Average I_{BB} = __-.1__ mAmps Average

V_{CC} 5 ± 0.25 Volts V_{BB} = -4.25 ± .25 Volts I_{DD} = __50__ mAmps Average I_{SS} = __-150__ mAmps Average

V_{DD} = 10 ± 1.0 Volts V_{SS} = 0 ± 0.0 Volts I_{GG} = __20__ mAmps Average

CHARACTERISTIC	SYMBOL	UNITS	PINS	LIMITS MIN.	LIMITS MAX.
INPUT LOW VOLTAGE	V_{IL}	Volts	PHASE A, PHASE B	-2.0	+0.8
			D 0-15	-1.0	+10
			I/O CLOCK, I/O DATA 1, I/O DATA 2	-1.0	+0.5
			BUSY, DONE	-1.0	+1.0
			INT, INTP, DCHP, DCH SYNC	-1.0	+1.0
INPUT CURRENT FOR LOW STATE	I_{IL}	mAmps	PHASE A, PHASE B	-	+.01
			D 0-15	-	-2.0
			I/O CLOCK, I/O DATA 1, I/O DATA 2	-	-2.0
			BUSY, DONE	-	-2.0
			INT, INTP, DCHP, DCH SYNC	-	-2.0
INPUT HIGH VOLTAGE	V_{IH}	Volts	PHASE A, PHASE B	+13.0	+15.0
			D 0-15	+4.0	+6.0
			I/O CLOCK, I/O DATA 1, I/O DATA 2	+2.5	+6.0
			BUSY, DONE	+4.0	+6.0
			INT, INTP, DCHP, DCH SYNC	+4.0	+6.0
INPUT CURRENT FOR HIGH STATE	I_{IH}	mAmps	PHASE A, PHASE B	-	+.01
			D 0-15	-	-.07
			I/O CLOCK, I/O DATA 1, I/O DATA 2	-	-.04
			BUSY, DONE	-	-.07
			INT, INTP, DCHP, DCH SYNC	-	-.07
OUTPUT LOW VOLTAGE	V_{OL}	Volts	D 0-15	-	+0.4
			I/O CLOCK, I/O DATA 1, I/O DATA 2	-	+0.4
			F 0-3, F STROBE	-	+0.4
			BUSY, DONE	-	+0.4
			DCHR, INTR, I/O INPUT	-	+0.4
OUTPUT CURRENT FOR LOW STATE	I_{OL}	mAmps	D 0-15	+2.0	-
			I/O CLOCK, I/O DATA 1, I/O DATA 2	+2.0	-
			F 0-3, F STROBE	+4.0	-
			BUSY, DONE	+2.0	-
			DCHR, INTR, I/O INPUT	+4.0	-
OUTPUT HIGH VOLTAGE	V_{OH}	Volts	D 0-15	+4.0	-
			I/O CLOCK, I/O DATA 1, I/O DATA 2	+3.0	-
			F 0-3, F STROBE	+2.7	-
			BUSY, DONE	+4.0	-
			DCHR, INTR, I/O INPUT	+2.7	-
OUTPUT CURRENT FOR HIGH STATE	I_{OH}	mAmps	D 0-15	-	-.07
			I/O CLOCK, I/O DATA 1, I/O DATA 2	-	-.04
			F 0-3, F STROBE	-	-.10
			BUSY, DONE	-	-.07
			OUT, DCHR, INTR	-	-.10
INPUT CAPACITANCE	C_I	pF	PHASE A, PHASE B	-	50
			D 0-15	-	10
			I/O CLOCK, I/O DATA 1, I/O DATA 2	-	10
			BUSY, DONE	-	10
			INT, INTP, DCHP, DCH SYCN	-	10

NOTE

Logic "1" is defined as the more positive voltage as are the maximum figures given under voltage limits. Logic "0" is defined as the more negative voltage as are the minimum figures given under voltage limits.

Positive current is defined, in the conventional sense, as flowing into the pin.

On power-up, V_{BB} must be within its specified operating range (with respect to V_{SS}) before any of the other power supply voltages are applied to the circuit.

FUNCTIONAL DESCRIPTION

The I/O controller (IOC) is intended to facilitate the design of peripherals that communicate with the microNOVA CPU. It is designed to be built into a peripheral, and contains circuitry to perform many of the operations that a peripheral must perform in order to communicate with the CPU. One IOC is ordinarily used in every peripheral in a microNOVA computer system.

An IOC is the interface between the peripheral of which it is a part and the I/O bus. The IOC communicates with the other components of the peripheral via some of its pins and with the CPU via others. The protocols that the IOC follows in communications with the other components of the peripheral have been selected to reduce the number of external components required to translate those communications into independent control signals to which the peripheral may easily respond. The protocols that the IOC follows in communications with the CPU are the same as the protocols that the CPU follows in communications with peripherals.

Internal Organization

The following block diagram shows the control logic, the registers and the data paths in the IOC.

The control logic of the IOC includes the programmable logic array, the state change logic and the state counter. The control logic determines the operations that are performed during data channel sequences and the execution of I/O commands.

The programmable logic array is a read-only memory. It contains information that defines the machine states of the IOC.

The state change logic determines the order in which the IOC enters the states defined in the programmable logic array. The order in which it selects the states depends on information received from the programmable logic array and status information received from the other components of the IOC.

The state counter is a register that contains the address of the information in the programmable logic array that defines the current state of the IOC.

The I/O shift register (IOSR) is a dual eight-bit shift register. It performs serial/parallel conversion between the data pins of the I/O port and the data paths of the IOC.

The address register is a 15-bit register. Its contents are incremented during data channel sequences and are transmitted via the I/O port if external registers are not enabled.

The word count register is a 16-bit register. Its contents are incremented during data channel sequences, and the peripheral is notified via the device port when it is incremented to 0.

The T register is a 16-bit register. It contains the direction indicator and data channel address during data channel sequences.

The device code register, the polarity bit and the external-register-enable bit are loaded with information received via the device port during the execution of an IORST command.

The device code register is a 6-bit register. The IOC executes an I/O comand only if bits 10 to 15 of the command are equal to the contents of bits 0 to 5 (respectively) of the device code register.

The polarity bit is a 1-bit register that determines the sense of data bits transmitted and received via the device port. If this bit contains 1, a low level on the data pins of the device port is interpreted as a 0, and a 0 is transmitted through those pins as a low level. If the polarity bit contains 0, data transferred through the data pins of the device port have the opposite sense.

The external-register-enable bit is a 1-bit register. If this bit contains 0, the data channel address transmitted via the I/O port during data channel sequence is the contents of the memory address register; otherwise, the data channel address is information received via the device port.

The mask-out driver and the interrupt disable logic together determine the contents of a 1-bit register called the interrupt disable bit. The contents of this bit are altered only during the execution of a MSKO command. The contents of the bit are determined by comparing data received via the I/O port with information received via the device port. The IOC only makes program interrupt requests when the contents of the interrupt disable bit are 0.

The busy/done logic contains two 1-bit registers called the busy bit and the done bit. The contents of these bits are loaded by operations performed during the execution of I/O commands and by operations performed on the device port by the peripheral. The contents of these bits are transmitted via the I/O port during the execution of an I/O skip command.

The interrupt request logic determines when the IOC is making a program interrupt request. It contains a 1-bit register called the interrupt-request bit; the IOC is making an interrupt request when this bit contains 1.

The data channel request logic determines when the IOC is making a data channel request. It contains a 1-bit register called the data channel request bit; the IOC is making a data channel request when this bit contains 1.
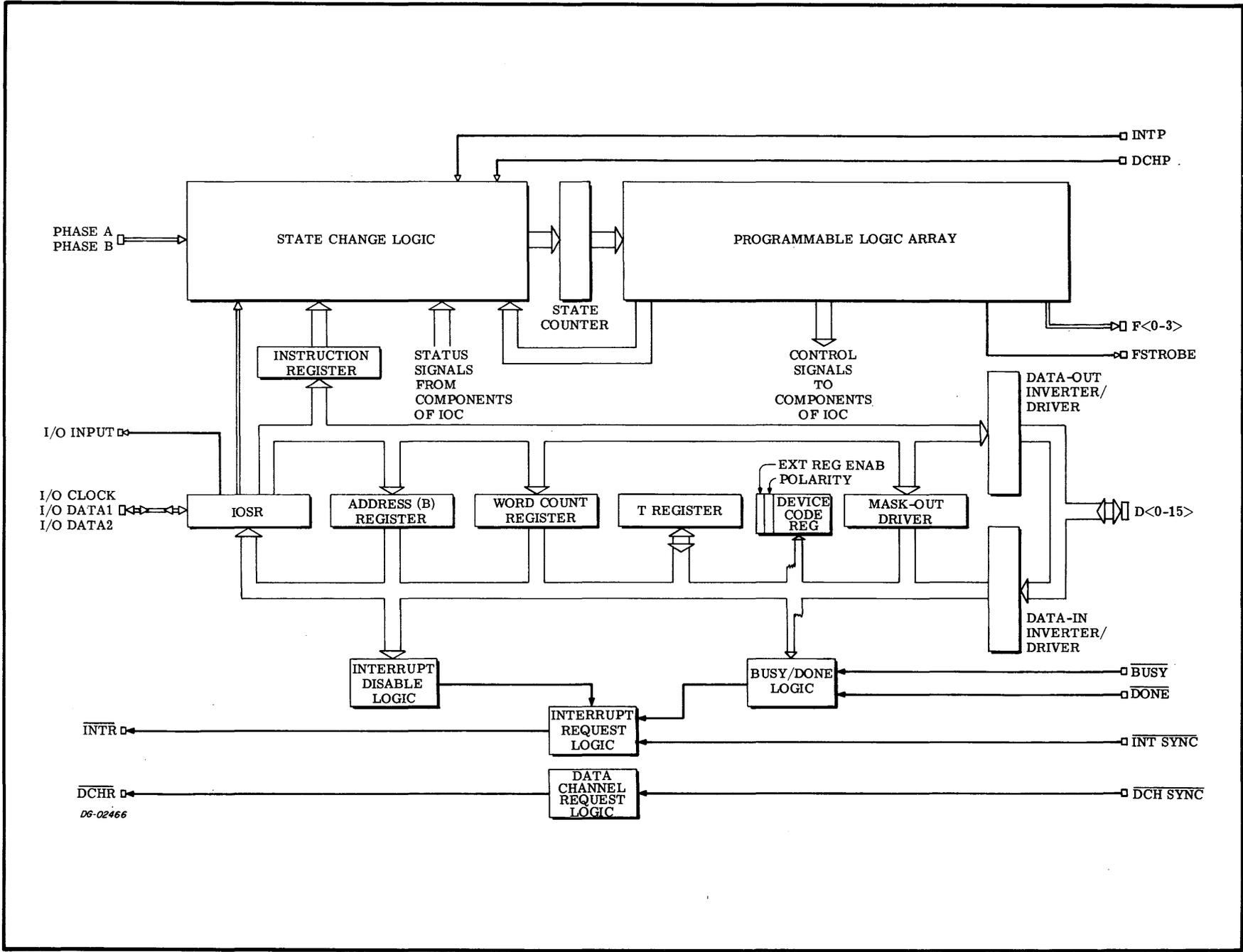
Pins

The pins via which the IOC receives and transmits information may be divided into groups as shown in the following table:

Group	Pins	Purpose
clock pins	PHASE A PHASE B	receive timing information
I/O data pins	I/O CLOCK I/O DATA1 I/O DATA2 I/O INPUT	receive and transmit data on I/O bus (via IOC I/O transceiver)
priority pins	INTP DCHP	receive priority information
function code pins	FSTROBE F[0-3]	transmit control information to other components
device data pins	D[0-15]	transmit data to other components or peripherals and receive data from them
busy/done, request pins	BUSY DONE INT INTR	transmit and receive control pulses to/from busy/done logic and interrupt-request logic
data channel request pins	DCH SYNC DCHR	receive data channel requests from other components or peripherals and transmit them on I/O bus

Clock Pins

In order for the IOC to operate, non-overlapping clocks must be applied to PHASE A and PHASE B, as shown in the following diagram.

mN603 CLOCKS

PERIOD = 120ns

	MIN.	MAX.
T_F	10	15
T_R	10	15
T_D	10	25
T_H	95	110
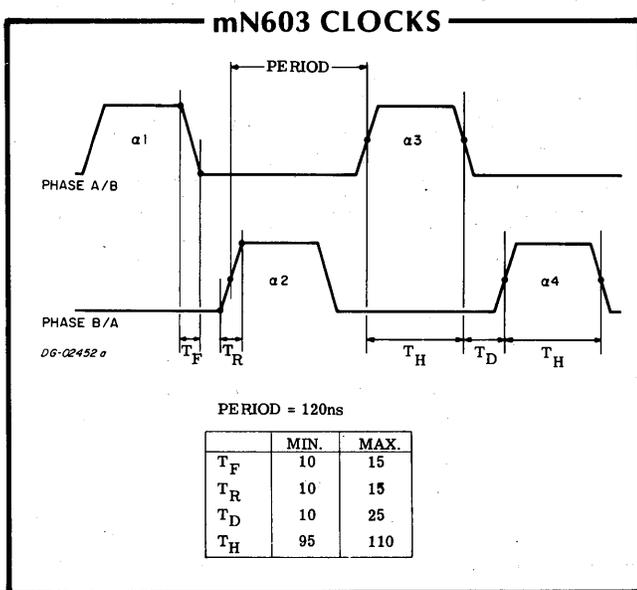
Each interval during which PHASE A or PHASE B is at high level is called an alpha cycle. There are four kinds of alpha cycles called alpha 1, alpha 2, alpha 3 and alpha 4 cycles.

When the IOC is reset, the first complete alpha cycle following a falling edge of I/O CLOCK is an alpha 3 cycle. (Note that this alpha 3 cycle may be an interval during which PHASE A is at high level or one during which PHASE B is at high level.) The next three alpha cycles are alpha 4, alpha 1 and alpha 2 cycles (in that order). Thereafter, every alpha 3 cycle is followed by an alpha 4 cycle; the alpha 4 cycle is followed by an alpha 1 cycle; the alpha 1 cycle is followed by an alpha 2 cycle; and the alpha 2 cycle is followed by an alpha 3 cycle. Alpha 1, alpha 2, alpha 3, and alpha 4 cycles are redefined every time the IOC is reset.

Different events occur on the pins of the IOC during each kind of alpha cycle. Therefore, alpha cycles are labeled in all following timing diagrams.

For simplicity, the remainder of this description of the IOC presumes that all alpha cycles are 120 nanoseconds.

In a microNOVA computer system, it is important that the delay between alpha cycles in the IOC and the corresponding alpha cycles in the CPU remain constant. Therefore, the source of the signals that drive PHASE A and PHASE B is ordinarily the CPU. These signals are the I/O bus signals BMCLOCK and BMCLOCK. They are received by the IOC I/O transceiver.

I/O Data Pins

The IOC communicates with the CPU in a microNOVA computer system via the I/O data pins. These pins, their significance to the IOC and the direction in which information is transferred through them are listed in the following table.

Pin	Significance	Direction
I/O CLOCK	synchronizes information transfers	to and from IOC
I/O DATA1	carries control information and data	to and from IOC
I/O DATA2	carries control information and data	to and from IOC
I/O INPUT	indicates direction of transfers	from IOC

Whether the I/O data pins are transmitting or receiving information, their minimum and maximum rise times are 15 and 25 nanoseconds and the minimum and maximum fall times are 10 and 15 nanoseconds, respectively. The maximum skew between I/O CLOCK, and either I/O DATA1 or I/O DATA2 is 10 nanoseconds.

RECEIVING INFORMATION VIA THE I/O DATA PINS

Most of the time, the I/O bus data pins behave as input pins. The IOC recognizes that information is being transferred to it when it is not already engaged in the reception of information and I/O CLOCK goes to low level. The levels of I/O DATA1 and I/O DATA2 at this time determine how much information the IOC expects to receive and how that information is interpreted.

The IOC interprets information received via the I/O data pins as a request-enable code, as a data-channel-acknowledge code, as an I/O command, or as I/O data. The following timing diagrams depict the four types of information that are recognized by the IOC.

Request-enable Code - I/O CLOCK goes to low level and then to high level. During the interval when I/O CLOCK is at low level, I/O DATA1 and I/O DATA2 are at high level.

mN603 REQUEST-ENABLE CODE FROM BUS

DG-02468
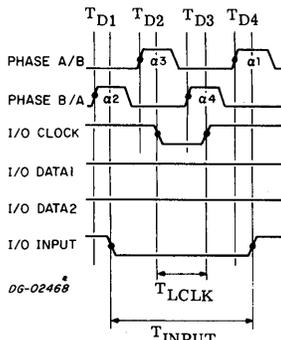
	MIN. (ns)	MAX. (ns)
T_{D1}	15	30
T_{D2}	15	30
T_{D3}	15	35
T_{D4}	15	30
T_{LCLK}	115	125
T_{INPUT}	350	370

Data-channel-acknowledge Code - I/O CLOCK goes to low level and then to high level. During the interval when I/O CLOCK is at low level, I/O DATA1 and I/O DATA2 are at high level and low level, respectively.

mN603 DATA-CHANNEL-ACKNOWLEDGE CODE FROM BUS

DG-02471
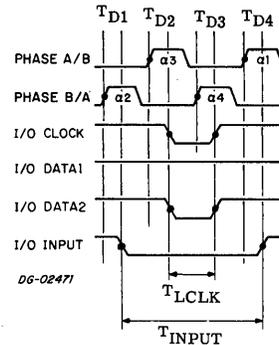
	MIN. (ns)	MAX. (ns)
T_{D1}	15	30
T_{D2}	15	30
T_{D3}	15	35
T_{D4}	15	30
T_{LCLK}	115	125
T_{INPUT}	350	370

I/O Command - I/O CLOCK goes to low level and then to high level. During the interval when I/O CLOCK is at low level, I/O DATA1 and I/O DATA2 are both at low level.

mN603 I/O COMMAND FROM BUS

DG-02469
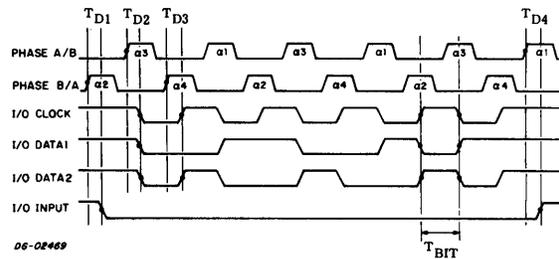
	MIN. (ns)	MAX. (ns)
T_{D1}	15	30
T_{D2}	15	30
T_{D3}	15	35
T_{D4}	15	30
T_{BIT}	115	125

Thereafter, it is expected that I/O **CLOCK** goes to low level and then to high level four times. During each interval delimited by a change in the level at I/O **CLOCK**, I/O **DATA1** and I/O **DATA2** each receive one bit. Low level at these pins is interpreted as 0, and high level at these pins is interpreted as 1. In this diagram, they are shown receiving 062622$_8$.

For reference, the bits of an I/O command are numbered from 0 to 15, as shown in the following diagram.

mN603 RECEPTION FORMAT
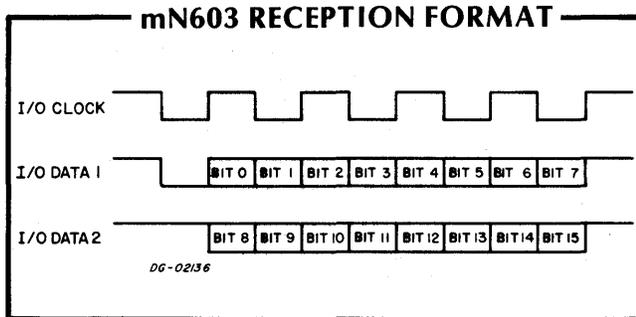
I/O·Data - I/O **CLOCK** goes to low level and then to high level. During the interval when I/O **CLOCK** is at low level, I/O **DATA1** and I/O **DATA2** are at low level and high level, respectively.
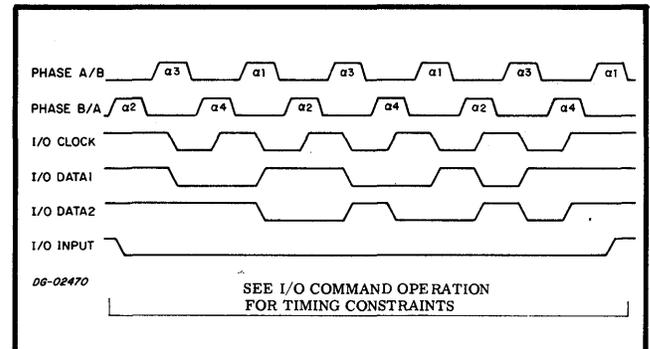
SEE I/O COMMAND OPERATION FOR TIMING CONSTRAINTS

Thereafter, it is expected that I/O **CLOCK** goes to low level and then to high level four times. During each interval delimited by a change in the level at I/O **CLOCK**, I/O **DATA1** and I/O **DATA2** each receive one bit. Low level at these pins is interpreted as 0, and high level at these pins is interpreted as 1. In the diagram, they are shown receiving 062622$_8$.

For reference, the bits of I/O data are numbered from 0 to 15, as shown in the following diagram.

mN603 RECEPTION FORMAT
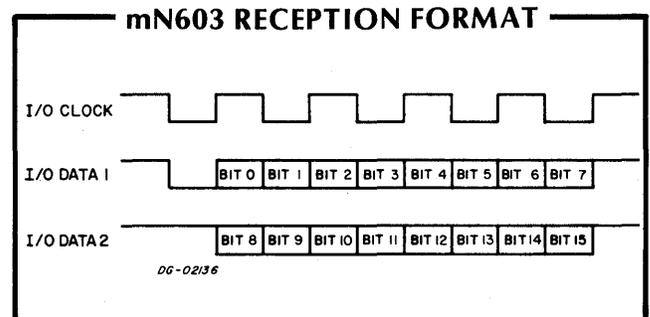
TRANSMITTING INFORMATION VIA THE I/O DATA PINS

During some sequences of operations that the IOC performs, it transmits information via the I/O data pins. The format of the information is the format that is interpreted by the CPU as I/O data. (That is, it is in the format that the CPU expects when it is performing an I/O data-in operation on its I/O data pins.) The operation during which information is transmitted via the I/O data pins is called an I/O data-out operation.

I/O Data-out Operation - During an I/O data-out operation, a 2-bit code and a 16-bit data word are transmitted via the I/O data pins. The following timing diagram depicts the sequence of events that occur on the I/O data pins during an I/O data-out operation.

I/O CLOCK assumes the low and high states five times, as shown in the diagram.
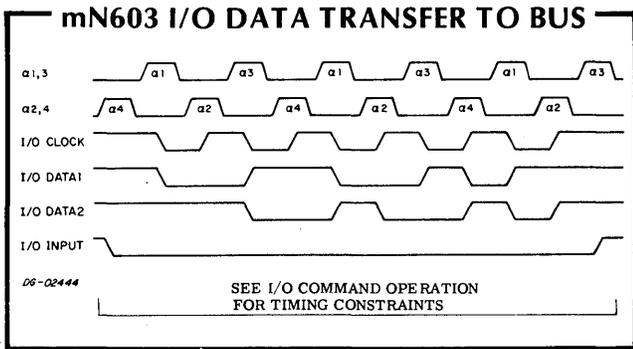
mN603 I/O DATA TRANSFER TO BUS

SEE I/O COMMAND OPERATION
FOR TIMING CONSTRAINTS

During the first interval when **I/O CLOCK** is in the low state, **I/O DATA1** and **I/O DATA2** assume the low state and the high state, respectively, to indicate that the IOC is performing an I/O data-out operation.

Thereafter, during each interval delimited by a change in the state of **I/O CLOCK**, **I/O DATA1** transmits one bit, and **I/O DATA2** transmits one bit. They assume the low state to transmit 0 and the high state to transmit 1. In this diagram, they are shown transmitting 062622_8.

For reference, bits transmitted during an I/O data-out operation are numbered as shown in the following diagram.

mN603 TRANSMISSION FORMAT
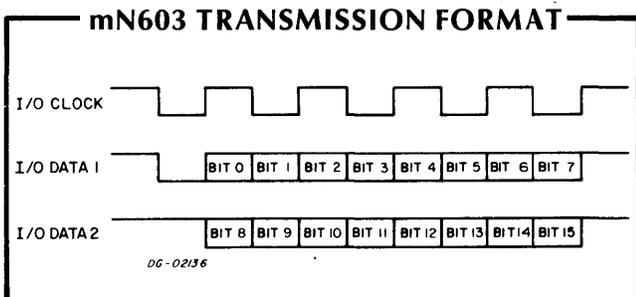
Priority Pins

The information that the IOC receives via the priority pins determines how the IOC responds to data-channel-acknowledge codes and INTA I/O commands. In order to understand the significance of these pins, see the descriptions of data-channel sequences and INTA commands. The only timing constraints on these pins are imposed by the interaction of peripherals in the microNOVA computer system. These timing constraints are explained in the Interface Manual.

Function Code Pins

Whenever the IOC is operating, $\overline{\text{FSTROBE}}$ is a square wave with a period of four alpha cycles. The interval during which $\overline{\text{FSTROBE}}$ is in the low state is called an **F** cycle.

During each **F** cycle, **F[0-3]** each transmit one bit. They assume the low state to transmit 0 and the high state to transmit 1. **F[0-3]** only change state while $\overline{\text{FSTROBE}}$ is in the high state, that is, between **F** cycles.

The information transmitted via **F[0-3]** during one **F** cycle is called a function code; there are sixteen of them. Fifteen of the sixteen function codes indicate an operation that the IOC is performing and may imply that the IOC expects some response from the other components of the peripheral. The other code indicates that the IOC is performing no operation and that no response is expected from the other components of the peripheral. For reference, each function code has a name; the function codes and their names are shown in the following table.

F0	F1	F2	F3	Name
0	0	0	0	DATOA
0	0	0	1	DATIA
0	0	1	0	DATOB
0	0	1	1	DATIB
0	1	0	0	DATOC
0	1	0	1	DATIC
0	1	1	0	STRT
0	1	1	1	CLR
1	0	0	0	IOPLS
1	0	0	1	IORST
1	0	1	0	MSKO
1	0	1	1	DCHA
1	1	0	0	DCHI
1	1	0	1	DCHO
1	1	1	0	WCEZ
1	1	1	1	NOP

NOP is the function code that indicates that the IOC is not performing any operation. The significance of the other function codes is indicated in the descriptions of data-channel sequences and I/O commands below.

The following timing diagram depicts the electrical events that occur on the function code pins during two successive **F** cycles. In the diagram, **F[0-3]** are transmitting the **DATIB** code during the first **F** cycle and the **STRT** code during the second **F** cycle.

mN603 FUNCTION CODES

	MIN. (ns)	MAX. (ns)
T_1	10	25
T_2	10	30
T_3	10	30
T_4	20	45
T_R	10	20
T_F	4	12

DG-02497
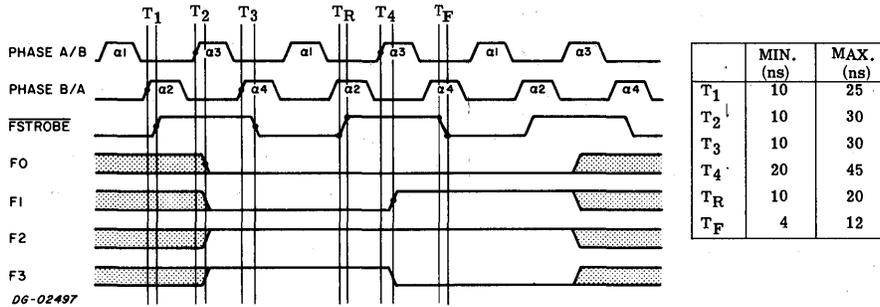
minimum and maximum rise times for the function code pins are 15 and 25 nanoseconds, and the minimum and maximum fall times are 10 and 15 nanoseconds, respectively.

Device Data Pins

The IOC transmits information to the other components of the peripheral and receives information from them via the device data pins. The significance of the information transmitted or received via these pins is determined by the operation that the IOC is performing. As described above, the operations that the IOC performs are indicated by the function code pins, and the transmission and reception of data via the device data pins are synchronized with the operations that the IOC performs on the function code pins, as shown in the following timing diagrams.

RECEIVING INFORMATION VIA THE DEVICE DATA PINS

When the IOC receives information via the device data pins, the pins are precharged during alpha 3 and are sampled during alpha 1. D14 is shown as a typical pin receiving a low level; D15 is shown as a typical pin receiving a high level. The operation that the IOC is performing and the contents of the polarity bit determine whether low level at the device data pins is interpreted as 0 or 1.

For reference, bits received via the device data pins are numbered. The bit received via D0 is bit 0, the bit received via D1 is bit 1, etc.

TRANSMITTING INFORMATION VIA THE DEVICE DATA PINS

When the IOC transmits information via the device data pins, the pins are discharged or precharged during alpha 3. D14 is shown as a typical pin that assumes the low state (i.e., that is discharged); D15 is shown as a typical pin that assumes the high state (i.e., that is not discharged). The contents of the polarity bit determine whether the device data pins assume a low level or a high level to transmit 0.

mN603 DATA FROM DEVICE

DG-02496
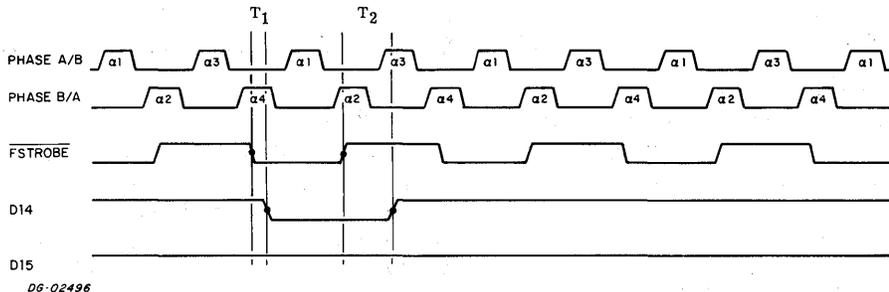
DATA LINES FALL TIMES 5-15

	MIN. (ns)	MAX. (ns)
T_1	0	100
T_2	0	100
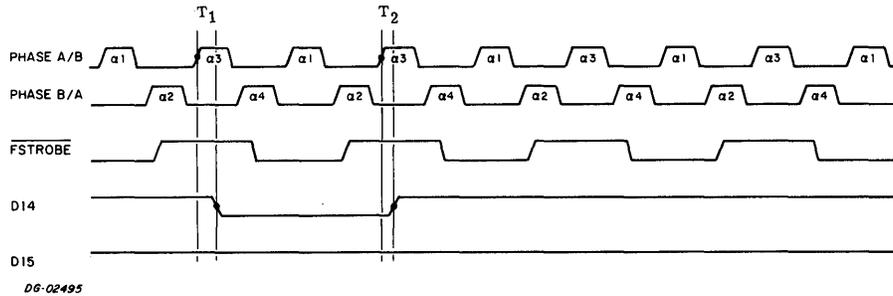
DG-02495

DATA LINES RISE AND FALL TIMES: 10-20

	MIN. (ns)	MAX. (ns)
T_1	10	30
T_2	10	30

The minimum and maximum rise times for the device data pins are 15 and 25 nanoseconds, and the minimum and maximum fall times are 10 and 15 nanoseconds, respectively.

For reference, bits transmitted via the device data pins are numbered. The bit transmitted via **D0** is bit 0, the bit transmitted via **D1** is bit 1, etc.

Busy/Done and Interrupt-request Pins

The relation between the pins $\overline{\text{BUSY}}$, $\overline{\text{DONE}}$, $\overline{\text{INT SYNC}}$ and $\overline{\text{INTR}}$ are described by the schematic diagram below. In this schematic, the signals **RQENB**, **STRT**, **CLR**, **IOPLS** and **IORST** are hypothesized to assist in the description. The signal **RQENB** goes from low level to high level during request-enable sequences. **STRT**, **CLR**, **IOPLS** and **IORST** are signals that are asserted whenever **STRT**, **CLR**, **IOPLS** and **IORST** codes (respectively) are transmitted via **F[0-3]**.

Data-channel Request Pins

$\overline{\text{DCHR}}$ assumes the low state when the IOC is making a data-channel request. The IOC determines when to make data-channel requests from the informatin that it receives via $\overline{\text{DCH SYNC}}$. In order to understand the significance of these pins, see the description of request-enable and data-channel sequences.

Sequences of Operations

The IOC performs sequences of operations in response to request-enable codes, data-channel-acknowledge codes and I/O commands that it receives via the I/O bus data pins. The operations are performed on the registers in the IOC and on its pins. The sequences of operations are described below.
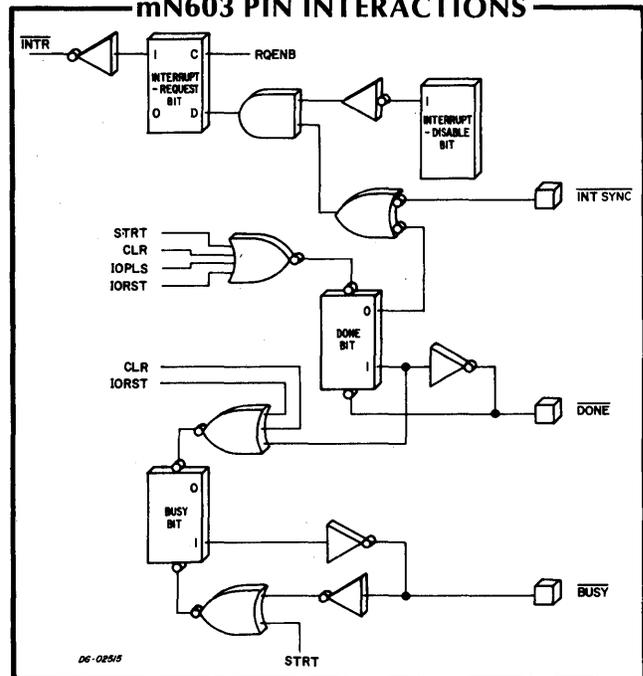
DG-02515

Request-enable Sequences

The IOC performs a request-enable sequence if a request-enable code is received via the I/O data pins when the IOC is not already performing a sequence of operations. During a request-enable sequence, the following operations are performed.

If the done bit contains 1 or $\overline{\text{INT SYNC}}$ is at low level during the alpha 3 cycle when the request-enable code is received, 1 is loaded into the interrupt-request bit, and $\overline{\text{INTR}}$ assumes the low state during the next alpha 2 cycle; otherwise, 0 is loaded into the interrupt-request bit, and $\overline{\text{INTR}}$ assumes the high state during the next alpha 2 cycle.

If the data-channel-pending bit contains 0 and $\overline{\text{DCH}}$ $\overline{\text{SYNC}}$ is at low level during the alpha 3 cycle when the request-enable code is received, a data channel control word is loaded into the T register as follows:

1. The DCHA code is transmitted via F[0-3] during the next F cycle. During this F cycle, data is received via D[0-15].

2a. If the external-register-enable bit contains 1, the data received is loaded into the T register.

2b. If the external-register-enable bit contains 0, the data received via D0 is loaded into bit 0 of the T register, and the contents of bits 1 to 15 of the address register are loaded into bits 1 to 15 of the T register. The contents of the address register are then incremented.

3. The contents of the word count register are incremented. If the new contents are 000000_8, the WCEZ code is transmitted via F[0-3] during the F cycle following the one during which the DCHA code is transmitted.

1 is loaded into the data-channel-pending bit to indicate that the T register is in use.

If the data-channel-pending bit contains 1 during the alpha 3 cycle when the request-enable code is received (i.e., if the T register is already in use because of some prior request-enable sequence, data-channel sequence or I/O command), 1 is loaded into the data-channel-request bit, and $\overline{\text{DCHR}}$ assumes the low state during the next alpha 2 cycle; otherwise, the contents of the data-channel-request bit and the state of $\overline{\text{DCHR}}$ are not changed.

The following timing diagram depicts the operations that are performed on the I/O data pins and the function code pins during a request-enable operation. For brevity, I/O DATA[1-2] and F[0-3] are omitted. The information that is transmitted via these pins is indicated by labels.

mN603 REQUEST-ENABLE OPERATION TO DEVICE

DG-02490
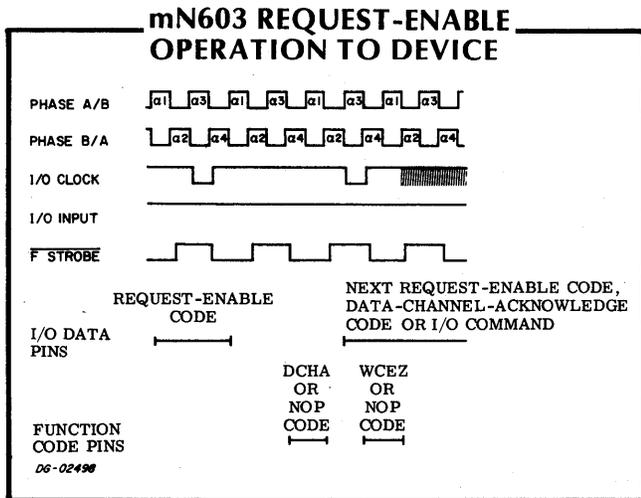
Data-channel Sequences

The IOC performs a data-channel sequence if it receives a data-channel-acknowledge code via the I/O data pins when the IOC is not already performing a sequence of operations. During a data-channel sequence, the following operations are performed.

If the data-channel-request bit contains 1 and the pin DCHP is at high level, the IOC performs a data channel transfer as follows.

An I/O data-out operation is performed. The data transmitted via the I/O data pins is data-channel control word in the T register (loaded during a prior request-enable sequence or data-channel sequence). Bit 0 of the data channel control word is called the direction indicator; bits 1 to 15 are called the data channel address.

If the direction indicator is 0, a data channel transfer into the peripheral is performed. A DCHO code is transmitted via F[0-3] on the twelfth F cycle following the receipt of the data-channel-acknowledge code. During this F cycle, the contents of the IOSR are transmitted via the pins D[0-15]. It is expected that the IOC receives I/O data via the I/O bus data pins between the transmission of the data-channel control word via the I/O data pins and the transmission of the DCHO code via F[0-3]. This data is calld the data-channel data.

If the direction indicator is 1, a data channel transfer out of the peripheral is performed. A DCHI code is transmitted via F[0-3] during the sixth F cycle following the receipt of the data-channel-acknowledge code. During this F cycle, data is received via D[0-15]. An I/O data-out operation is performed. The data transmitted via the I/O port during this operation is the data received via D[0-15]. This data is called the data-channel data.

If the IOC does not perform a data-channel transfer, it performs a request-enable sequence as if the request-enable code were received during the alpha 3 cycle following the one during which the data-channel-acknowledge code is received.

If the IOC does perform a data-channel transfer, it performs all the operations of a request-enable sequence as just described, except that the information loaded into the data-channel-pending bit and data-channel-request bit is different. If $\overline{\text{DCH SYNC}}$ is at low level during the alpha 3 cycle following the one during which the data-channel-acknowledge code is received, 1 is loaded into each of these bits; otherwise, 0 is loaded into each of them.

The following timing diagrams depict a data-channel sequence during which the IOC transmits data channel data and a data channel sequence during which the IOC receives data channel data. For brevity, I/O DATA[1-2] and F[0-3] are omitted. The information that is transferred via these pins is indicated by labels.

mN603 DATA CHANNEL SEQUENCE TO DEVICE

PHASE A/B

PHASE B/A

I/O CLOCK

I/O INPUT

FSTROBE
DG-02499

| DATA-CHANNEL-ACKNOWLEDGE CODE | I/O DATA-OUT OPERATION (DATA CHANNEL CONTROL WORD) | I/O DATA-OUT OPERATION (DATA CHANNEL DATA) | NEXT REQUEST-ENABLE CODE, DATA-CHANNEL-ACKNOWLEDGE CODE OR I/O COMMAND |

I/O DATA PINS

FUNCTION CODE PINS

DCHA OR NOP CODE   WCEZ OR NOP CODE   DCHI CODE

mN603 DATA CHANNEL SEQUENCE FROM DEVICE

PHASE A/B

PHASE B/A

I/O CLOCK

I/O INPUT

FSTROBE

| DATA-CHANNEL ACKNOWLEDGE CODE | I/O DATA-OUT OPERATION (DATA CHANNEL CONTROL WORD) | I/O DATA (DATA CHANNEL DATA) | NEXT REQUEST-ENABLE CODE, DATA-CHANNEL-ACKNOWLEDGE OR I/O COMMAND |

I/O DATA PINS

DG-02500

DCHA OR NOP CODE   WCEZ OR NOP CODE   DCHO CODE

I/O Command Execution

The IOC executes an I/O command if it receives the I/O command when it is not already performing a sequence of operations.

Bits 10 to 15 of an I/O command determine how the other bits of the command are interpreted. These bits are called the device code field of the I/O command. Unless the device code field is 77_8 or is equal to the contents of the device code register, the IOC performs no operations. If the IOC does perform a sequence of operations, the operations that it performs depend on the the device code field and the other bits of the I/O command.

I/O Commands with Device Code 77_8

The operations specified by I/O commands whose device code fields contain 77_8 are described below.

I/O Reset

			0	0	0	1	0			1	1	1	1	1	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

The IOC is reset. 0 is loaded into the interrupt-request bit, the data-channel-request bit and the data-channel-pending bit; 00000_8 is loaded into the address register; and 000000_8 is loaded into the word count register.

The IORST code is transmitted via F[0-3] for one F cycle. During this F cycle, data is received via D[8-15]. If D8 is at low level, 1 is loaded into the external-register-enable bit; otherwise 0 is loaded into this bit. If D9 is at low level, 1 is loaded into the polarity bit; otherwise, 0 is loaded into this bit. The data received from D[10-15] is loaded into bits 0 to 5 (respectively) of the device code register.

The contents of the polarity bit do not affect the interpretation of data received via D[0-15] during the execution of an I/O reset command.

Mask Out

					1	0	0			1	1	1	1	1	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

The MSKO code is transmitted via F[0-3] for one F cycle. During this F cycle, data is received via D[0-15]. The IOC waits to receive I/O data via the I/O bus data pins for 15 alpha cycles. It is expected that the CPU performs an I/O data-out operation to transfer data to the IOC at this time. The data received via the I/O bus data pins is logically ANDed with the data received via D[0-15]. If any bit of the result is 1, 1 is loaded into the interrupt disable bit. Otherwise, 0 is loaded into the interrupt disable bit.

The contents of the polarity bit do not affect the interpretation of data received via D[0-15] during the execution of a mask out command.

Interrupt Acknowledge

				0	1	1			1	1	1	1	1	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

If the interrupt-request bit contains 1 and the pin INTP is at high level, the IOC performs an I/O data-out operation. Otherwise, the IOC performs no operation. If an I/O data-out operation is performed, bits 0 to 9 of the data transmitted via the I/O bus pins are all 0. Bits 10 to 15 of the data transmitted are equal to the contents of bits 0 to 5 (respectively) of the device code register.

I/O Commands Whose Device Code Field Is Equal To the Contents of the Device Code Register

The operations specified by I/O commands whose device code fields are equal to the contents of the device code register are decribed below.

The sequence of operations that the IOC performs during the execution of each of these I/O commands is determined by bits 5 to 9 of the I/O command. These bits are divided into two groups.

Bits 5 to 7 of the I/O command are called the transfer code field. The information in this field is called a transfer code. The transfer codes and their names are listed in the following table.

Bit 5	Bit 6	Bit 7	Code Name
0	0	0	NIO
0	0	1	DIA
0	1	0	DOA
0	1	1	DIB
1	0	0	DOB
1	0	1	DIC
1	1	0	DOC
1	1	1	SKP

Bits 8 and 9 of the I/O command are called the pulse code field. The information in this field is called a pulse code. The pulse codes and their names are listed in the following table.

Bit 8	Bit 9	Code Name
0	0	none
0	1	S
1	0	C
1	1	P

The name of an I/O command is the name of the transfer code that the I/O command contains followed by the name of the pulse code that the I/O command contains. For example, the name of the I/O command that contains the transfer code DOA and the pulse code S is DOAS. If bits 8 and 9 of the command are both 0, then the name of the I/O command is just the name of the transfer code.

During the execution of an I/O command, the operations specified by the transfer code are performed. Then, if the transfer code is not the SKP code, the operations specified by the pulse code are performed. If the transfer code is the SKP code, the pulse code is ignored. The operations specified by the transfer and pulse codes are described below.

NIO

During the first six F cycles following the receipt of the I/O command, the NOP code is transmitted via F[0-3].

DIA

During the second F cycle following the receipt of the I/O command, the DATIA code is transmitted via F[0-3]. During this F cycle, data is received via D[0-15]. Then an I/O data-out operation is performed. The data transmitted via the I/O bus data pins during this operation is the data received via D[0-15].

DOA

During the first five F cycles following the receipt of the I/O command, the NOP code is transmitted via F[0-3]. It is expected that data is received via the I/O data pins during this interval. During the next F cycle, the DATOA code is transmitted via F[0-3] and the data received via the I/O data pins is transmitted via D[0-15].

DIB

During the second F cycle following the receipt of the I/O command, the DATIB code is transmitted via F[0-3]. During this F cycle, data is received via D[0-15]. Then an I/O data-out operation is performed. If the external-register-enable bit contains 0, the data transmitted via the I/O bus data pins during this operation is the contents of the address register. Otherwise, the data transmitted is the data received via D[0-15].

DOB

During the first five F cycles following the receipt of the I/O command, the NOP code is transmitted via F[0-3]. It is expected that data is received via the I/O data pins during this interval. During the next F cycle, the DATOB code is transmitted via F[0-3] and the data received via the I/O data pins is transmitted via D[0-15]. If the external-register-enable bit contains 0, bits 1 to 15 of that data are also loaded into bits 1 to 15 (respectively) of the address register.

DIC

During the second F cycle following the receipt of the I/O command, the DATIC code is transmitted via F[0-3]. During this F cycle, data is received via D[0-15]. Then an I/O data-out operation is performed. The data transmitted via the I/O bus data pins during this operation is the data received via D[0-15].

DOC

During the first five F cycles following the receipt of the I/O command, the **NOP** code is transmitted via F[0-3]. It is expected that data is received via the I/O data pins during this interval. During the next F cycle, the **DATOC** code is transmitted via F[0-3] and the data received via the I/O data pins is transmitted via D[0-15]. If the external-register-enable bit contains 0, that data is also loaded into the word-count register.

SKP

An I/O data-out operation is performed. If the done bit contains 1, bit 0 of the data transmitted is 0; otherwise, bit 0 of the data transmitted is 1. If the busy bit contains 1, bit 1 of the data transmitted is 0; otherwise, bit 0 of the data transmitted is 1.

The operations specified by the pulse codes are as follows.

None

During the next F cycle, the **NOP** code is transmitted via F[0-3].

S

During the next F cycle, the **STRT** code is transmitted via F[0-3]. 1 is loaded into the busy bit, and 0 is loaded into the done bit.

C

During the next F cycle, the **CLR** code is transmitted via F[0-3]. 0 is loaded into the busy bit and the done bit.

P

During the next F cycle, the **IOPLS** code is transmited via F[0-3]. 0 is loaded into the done bit.

The following timing diagrams depict the operations that are performed on the I/O data pins and the function code pins during the execution of I/O commands during which I/O data is transmitted and received by the IOC. For brevity, I/O DATA[1-2] and F[0-3] are omitted. The information that is transmitted and recieved via these pins is indicated by labels.

Reset

The IOC is reset if I/O CLOCK is at low level for fifteen consecutive alpha cycles or more. If I/O CLOCK is at low level for eight alpha cycles or more, the IOC may or may not be reset. The IOC is not reset if I/O CLOCK is at low level for fewer than seven alpha cycles.

The first falling edge of I/O CLOCK after the IOC is reset defines alpha 1, alpha 2, alpha 3 and alpha 4 cycles, as indicated in the description of the clock pins.

mN603 DATA TRANSFER TO DEVICE

mN603 DATA TRANSFER FROM DEVICE
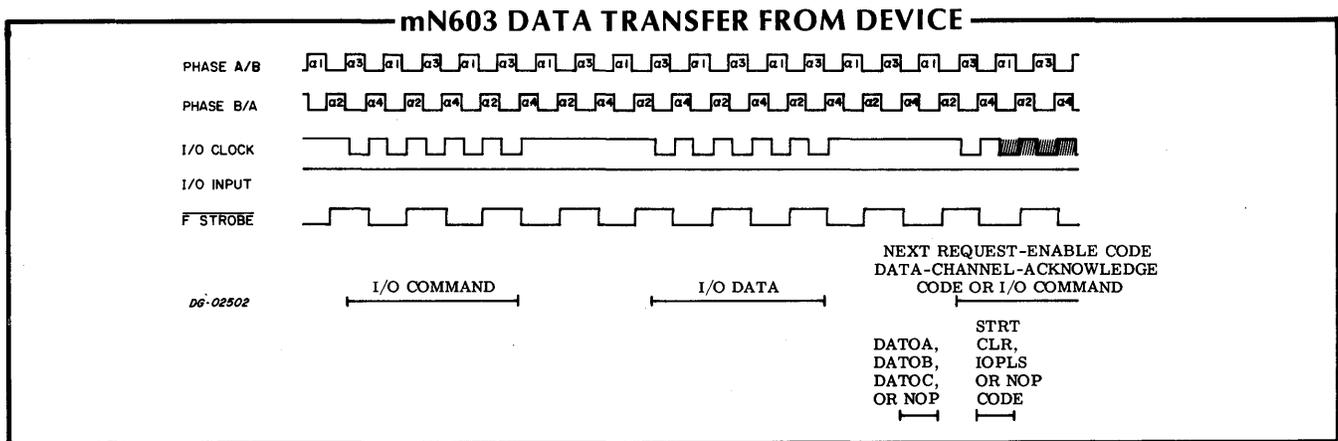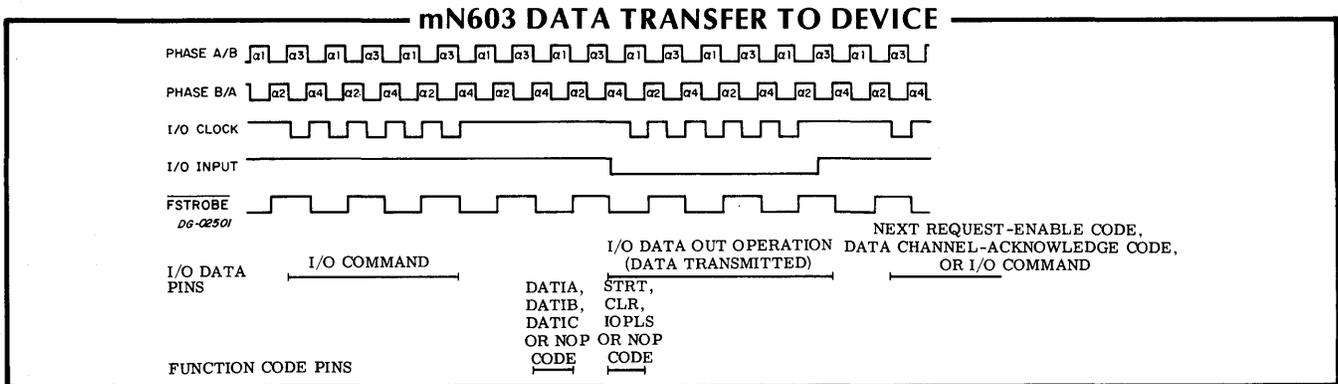
It is expected that this falling edge of I/O CLOCK is part of a request-enable code. Following such a request-enable code, the IOC performs the sequence of operations specified by an I/O reset command.

Power-up

When the IOC is powered up, it should be reset as described above.

> **NOTE** *The IOC may be damaged if V_{BB} is at a voltage positive with respect to any other pin of the IOC. Because this condition is most likely to arise during power-up, special precautions should be taken to ensure that the voltage at V_{BB} is within its specified operating range before power is applied to any other pin.*

SECTION V

mN634
MEMORY TRANSCEIVER

- PACKAGE

- PIN NAMES AND NUMBERS

- DC (STATIC) CHARACTERISTICS

- FUNCTIONAL DESCRIPTION

PACKAGE

The mN634 integrated circuit is supplied in a 20-pin ceramic dual in-line package (DIP).

PIN NUMBERS AND NAMES

$\overline{A_{IN}}$	1	20	V_{CC}
A_0	2	19	B_{IN}
B_0	3	18	A_7
B_1	4	17	B_7
A_1	5	16	B_6
A_2	6	15	A_6
B_2	7	14	A_5
B_3	8	13	B_5
A_3	9	12	B_4
GND	10	11	A_4
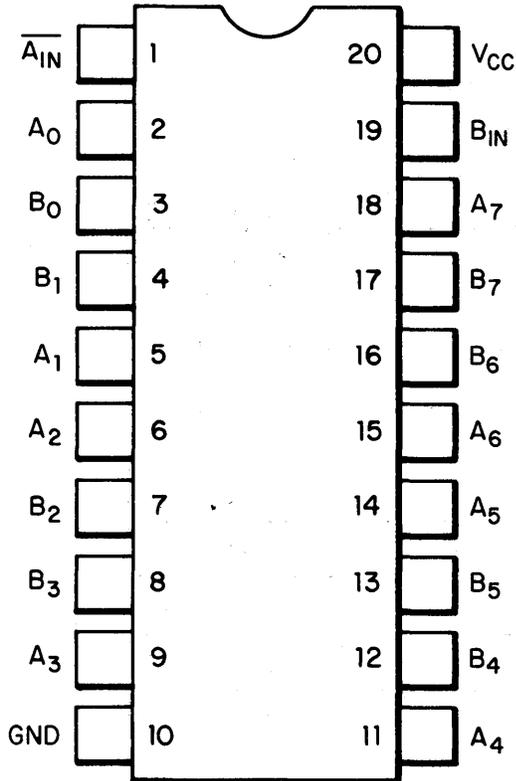
DG-02355 DG-02362

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range V_{CC}	-0.3 to +7Volts
Input Voltage Range V_I	-0.3 to +7Volts
Output Current Range I_O	0 to +60mAmps
Operating Temperature Range T_A	0 to 70°C
Storage Temperature Range T_{stg}	-55 to +125°C
Average Power Dissipation	3.0Watts

NOTES *All voltages in this document are referenced to GND.*

*Subjecting a circuit to conditions either outside these limits or at these limits for an extended period of time may cause irreparable damage to the circuit. As such, these ratings are not intended to be used during the operation of the circuit. Operating specifications are given in the DC (STATIC) CHARACTERISTICS TABLE.

DC (STATIC) CHARACTERISTICS
mN634

OPERATING SPECIFICATIONS

T_A range __0__ to __70__ C

V_{CC} 5± 0.25 Volts

GND = 0 ± 0.0 Volts

I_{CC} = __300__ mAmps maximum

CHARACTERISTIC	SYMBOL	UNITS	PINS	LIMITS	
				MIN.	MAX.
INPUT LOW VOLTAGE	V_{IL}	Volts	A<0-7> B<0-7>	-	+0.8
			$\overline{A_{IN}}$, B_{IN}	-	+0.8
INPUT CURRENT FOR LOW STATE	I_{IL}	mAmps	A<0-7> B<0-7>	-	-2.0
			$\overline{A_{IN}}$, B_{IN}	-	-2.0
INPUT HIGH VOLTAGE	V_{IH}	Volts	A<0-7> B<0-7>	+2.0	-
			$\overline{A_{IN}}$, B_{IN}	+2.0	-
INPUT CURRENT FOR HIGH STATE	I_{IH}	mAmps	A<0-7> B<0-7>	-	+0.06
			$\overline{A_{IN}}$, B_{IN}	-	+0.06
OUTPUT LOW VOLTAGE	V_{OL}	Volts	A<0-7> B<0-7>	-	+0.65
OUTPUT CURRENT FOR LOW STATE	I_{OL}	mAmps	A<0-7> B<0-7>	+40	-
OUTPUT HIGH VOLTAGE	V_{OH}	Volts	A<0-7> B<0-7>	-	5.0
OUTPUT CURRENT FOR HIGH STATE	I_{OH}	mAmps	A<0-7> B<0-7>	-	+0.06
INPUT CAPACITANCE	C_I	pF	A<0-7> B<0-7>	-	15
			$\overline{A_{IN}}$, B_{IN}	-	5

NOTE

Logic "1" is defined as the more positive voltage as are the maximum
figures given under voltage limits. Logic "0" is defined as the more
negative voltage as are the minimum figures given under voltage limits.

Positive current, in the conventional sense, is defined as flowing
into the pin.

— FUNCTIONAL DESCRIPTION —

A_0 • 2 — 3 • B_0

A_1 • 5 — 4 • B_1

A_2 • 6 — 7 • B_2

A_3 • 9 — 8 • B_3

A_4 • 11 — 12 • B_4

A_5 • 14 — 13 • B_5

A_6 • 15 — 16 • B_6

A_7 • 18 — 17 • B_7

$\overline{A_{IN}}$ • 1 B_{IN} • 19

PIN 20 = V_{CC}
PIN 10 = GND

DG-02425

T_1 T_2

IN

OUT
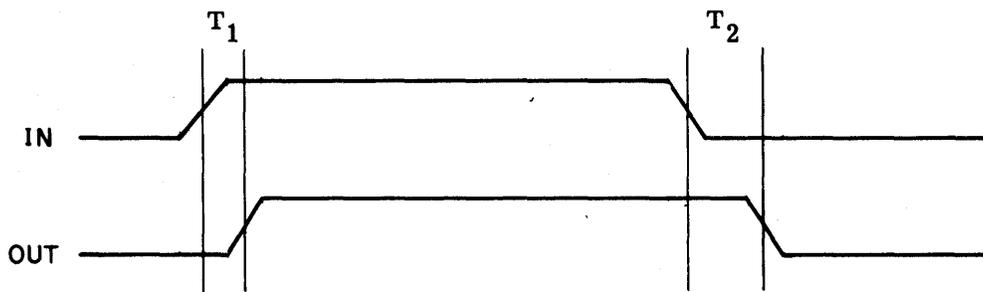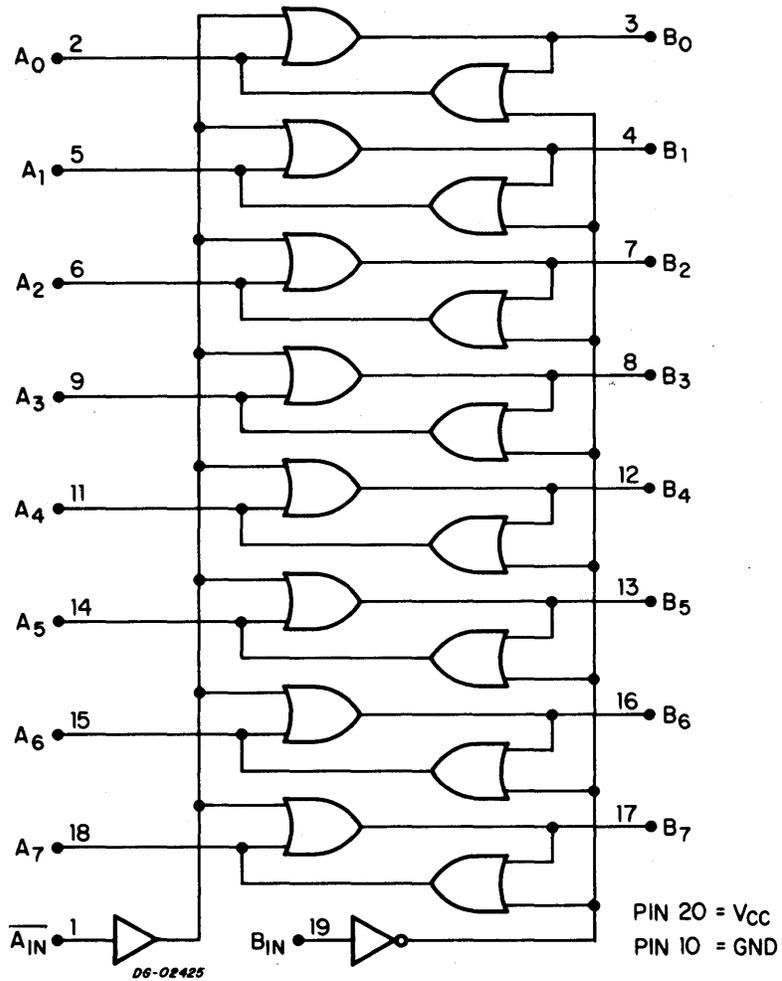
DG-02350

Conditions:

V_{CC} = 5 volts

Load = 140 Ω to V_{CC}, 200pF to ground

Input Rise Times   5 to 15ns
Input Fall Times   5 to 15ns

	MIN. (ns)	MAX. (ns)
T_1	18	25
T_2	18	35

SECTION VI

mN633
ADDRESS DRIVER

- PACKAGE

- PIN NAMES AND NUMBERS

- DC (STATIC) CHARACTERISTICS

- FUNCTIONAL DESCRIPTION

PACKAGE

The mN633 integrated circuit is supplied in a 20-pin ceramic dual in-line package (DIP).

PIN NUMBERS AND NAMES

$\overline{ENB}$	1	20	V_{CC}
A_I	2	19	N/C
A_O	3	18	H_I
B_O	4	17	H_O
B_I	5	16	G_O
C_I	6	15	G_I
C_O	7	14	F_I
D_O	8	13	F_O
D_I	9	12	E_O
GND	10	11	E_I
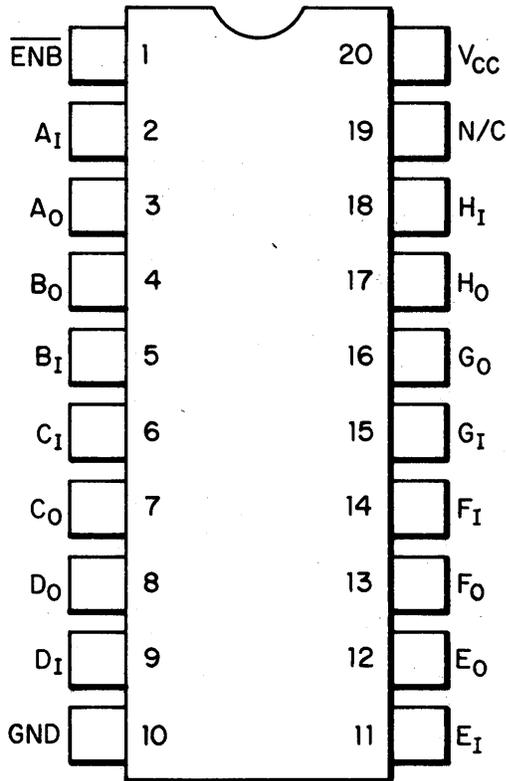
DG-02355 DG-02360

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range V_{CC}	-0.3	to	+7 Volts
Input Voltage Range V_I	-0.3	to	+7 Volts
Output Current Range I_O	0	to	+60 mAmps
Operating Temperature Range T_A	0	to	+70 °C
Storage Temperature Range T_{stg}	-55	to	+125 °C
Average Power Dissipation			+1.6 Watts

NOTES *All voltages in this document are referenced to GND.*

Subjecting a circuit to conditions either outside these limits or at these limits for an extended period of time may cause irreparable damage to the circuit. As such, these ratings are not intended to be used during the operation of the circuit. Operating specifications are given in the DC (STATIC) CHARACTERISTICS TABLE.

DC (STATIC) CHARACTERISTICS
mN633

OPERATING SPECIFICATIONS

T_A range __0__ to __70__ °C

V_{CC} 5 ± 0.25 Volts

GND   =   _0_ Volts

I_{GND} =   __300__ mAmps Maximum

CHARACTERISTIC	SYMBOL	UNITS	PINS	LIMITS MIN.	LIMITS MAX.
INPUT LOW VOLTAGE	V_{IL}	Volts	A_I, B_I, C_I, D_I, E_I, F_I, G_I, H_I, $\overline{ENB}$	-	+0.8
INPUT CURRENT FOR LOW STATE	I_{IL}	mAmps	A_I, B_I, C_I, D_I, E_I, F_I, G_I, H_I, $\overline{ENB}$	-	-2.0
INPUT HIGH VOLTAGE	V_{IH}	Volts	A_I, B_I, C_I, D_I, E_I, F_I, G_I, H_I, $\overline{ENB}$	+2.0	-
INPUT CURRENT FOR HIGH STATE	I_{IH}	mAmps	A_I, B_I, C_I, D_I, E_I, F_I, G_I, H_I, $\overline{ENB}$	-	+0.06
OUTPUT LOW VOLTAGE	V_{OL}	Volts	A_O, B_O, C_O, D_O, E_O, F_O, G_O, H_O	-	+0.65
OUTPUT CURRENT FOR LOW STATE	I_{OL}	mAmps	A_O, B_O, C_O, D_O, E_O, F_O, G_O, H_O	+40	-
OUTPUT HIGH VOLTAGE	V_{OH}	Volts	A_O, B_O, C_O, D_O, E_O, F_O, G_O, H_O	-	+5.0
OUTPUT CURRENT FOR HIGH STATE	I_{OH}	mAmps	A_O, B_O, C_O, D_O, E_O, F_O, G_O, H_O	-	+.06
INPUT CAPACITANCE	C_I	pF	A_I, B_I, C_I, D_I, E_I, F_I, G_I, H_I, $\overline{ENB}$	-	15

NOTE

Logic "1" is defined as the more positive voltage as are the maximum
figures given under voltage limits. Logic "0" is defined as the more
negative voltage as are the minimum figures given under voltage limits.

Positive current, in the conventional sense, is defined as flowing
into the pin.

— FUNCTIONAL DESCRIPTION —

$\overline{ENB}$ • 1

A_I • 2

3 • A_O

B_I • 5

4 • B_O

C_I • 6

7 • C_O

D_I • 9

8 • D_O

E_I • 11

12 • E_O

F_I • 14

13 • F_O

G_I • 15

16 • G_O

H_I • 18

17 • H_O
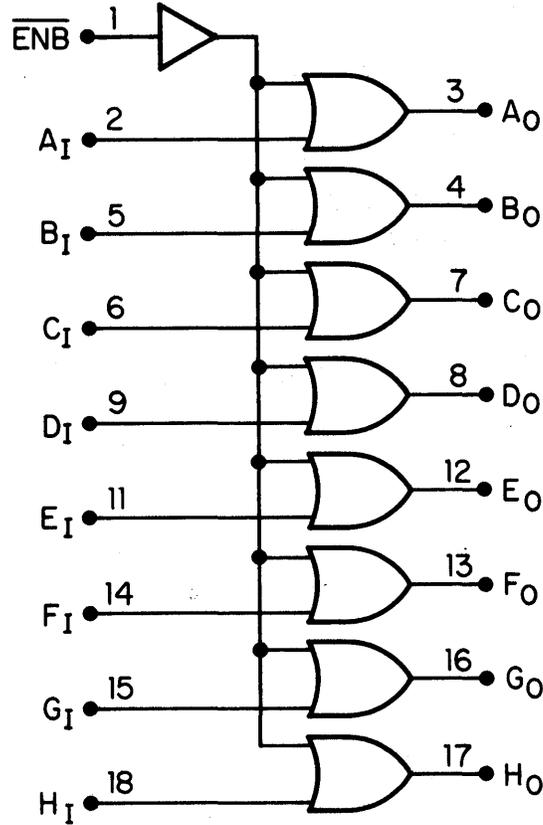
DG-02426

PIN 20 = V_{CC}

PIN 10 = GND
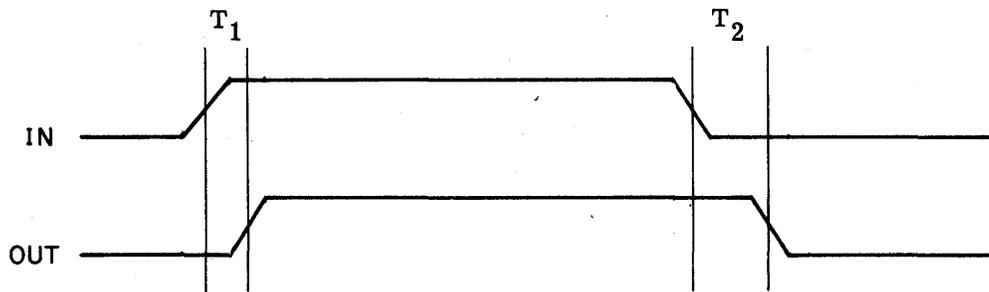
T_1 T_2

IN

OUT

DG-02350

Conditions:

V_{CC} = 5 volts

Load = 140Ω to V_{CC}, 200pF to ground

Input Rise Times   5 to 15ns
Input Fall Times   5 to 15ns

	MIN. (ns)	MAX. (ns)
T_1	18	35
T_2	18	25

SECTION VII
mN506
SENSE AMP/BUS DRIVER

- **PACKAGE**

- **PIN NAMES AND NUMBERS**

- **DC (STATIC) CHARACTERISTICS**

- **FUNCTIONAL DESCRIPTION**

PACKAGE

The mN506 integrated circuit is supplied in a 14-pin ceramic dual in-line package (DIP).

PIN NUMBERS AND NAMES

V_{CC1}	1		14	V_{CC2}
A_I	2		13	D_I
A_O	3		12	D_O
$\overline{STROBE}$ 1	4		11	$\overline{STROBE}$ 2
B_O	5		10	C_O
B_I	6		9	C_I
GND	7		8	V_{EE}

DG-02353 DG-02358
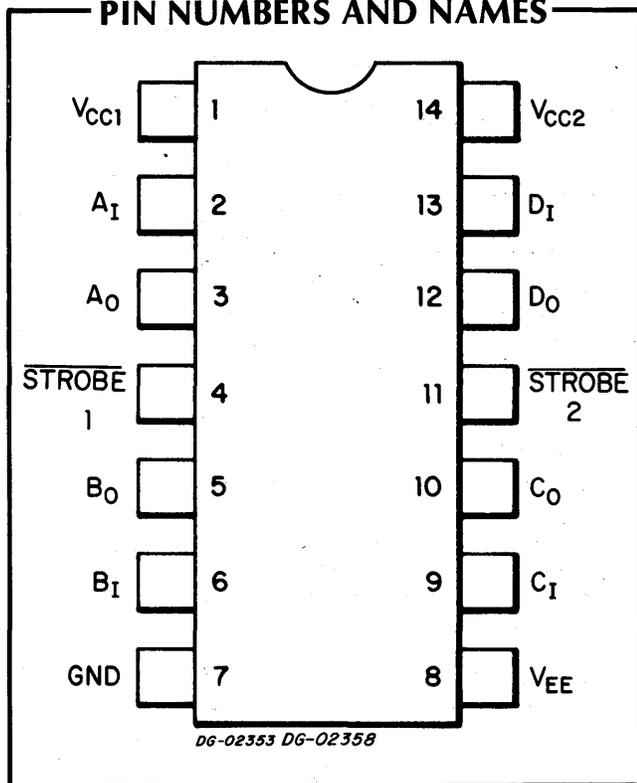
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range V_{CC1}	-0.5	to	+7 Volts
Supply Voltage Range V_{CC2}	-0.5	to	+7 Volts
Supply Voltage Range V_{EE}	0	to	-7 Volts
Input Voltage Range V_I	0	to	+5.5 Volts
Output Current Range I_O	0	to	60 mAmps
Operating Temperature Range T_A	0	to	70 °C
Storage Temperature Range T_{stg}	-25	to	+150 °C
Average Power Dissipation			0.8 Watts

NOTES *All voltages in this document are referenced to GND.*

*Subjecting a circuit to conditions either outside these limits or at these limits for an extended period of time may cause irreparable damage to the circuit. As such, these ratings are not intended to be used during the operation of the circuit. Operating specifications are given in the DC (STATIC) CHARACTERISTICS TABLE.

OPERATING SPECIFICATIONS

T_A range __0__ to __70__ °C $\quad$ V_{CC2} = 5 ± 0.5 Volts $\quad$ GND = 0 ± 0.0 Volts $\quad$ I_{EE} = __-55__ mAmps Average

V_{CC1} 5 ± 0.5 Volts $\quad\quad$ V_{EE} = -5 ± .0125 Volts $\quad$ I_{CC1} = ⎫
$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad$ $\quad$ $\qquad$ __105__ mAmps Average $\qquad$ I_{GND} = __50__ mAmps Average
$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad$ $\quad$ I_{CC2} = ⎭

CHARACTERISTIC	SYMBOL	UNITS	PINS		LIMITS	
					MIN.	MAX.
INPUT LOW VOLTAGE	V_{IL}	Volts	$A_I \quad\quad B_I$ $C_I \quad\quad D_I$		-	+2.0
			$\overline{STROBE\ 1}$, $\overline{STROBE\ 2}$		-	+0.8
INPUT CURRENT FOR LOW STATE	I_{IL}	mAmps	$A_I \quad\quad B_I$ $C_I \quad\quad D_I$		-1.5	-4.0
			$\overline{STROBE\ 1}$, $\overline{STROBE\ 2}$		-	-4.0
INPUT HIGH VOLTAGE	V_{IH}	Volts	$A_I \quad\quad B_I$ $C_I \quad\quad D_I$		+3.0	-
			$\overline{STROBE\ 1}$, $\overline{STROBE\ 2}$		+2.0	-
INPUT CURRENT FOR HIGH STATE	I_{IH}	mAmps	$A_I \quad\quad B_I$ $C_I \quad\quad D_I$		-	+4.0
OUTPUT LOW VOLTAGE	V_{OL}	Volts	$A_O \quad\quad B_O$ $C_O \quad\quad D_O$		-	+0.5
OUTPUT CURRENT FOR LOW STATE	I_{OL}	mAmps	$A_O \quad\quad B_O$ $C_O \quad\quad D_O$		-	+35
OUTPUT HIGH VOLTAGE	V_{OH}	Volts	$A_O \quad\quad B_O$ $C_O \quad\quad D_O$		-	+5.5
OUTPUT CURRENT FOR HIGH STATE	I_{OH}	mAmps	$A_O \quad\quad B_O$ $C_O \quad\quad D_O$		-	0.050
INPUT CAPACITANCE	C_I	pF	$A_I \quad\quad B_I$ $C_I \quad\quad D_I$		-	10
			STROBE 1, STROBE 2		-	5

NOTE

Logic "1" is defined as the more positive voltage as are the maximum
figures given under voltage limits. Logic "0" is defined as the more
negative voltage as are the minimum figures given under voltage limits.

Positive current, in the conventional sense, is defined as flowing
into the pin.

— FUNCTIONAL DESCRIPTION —
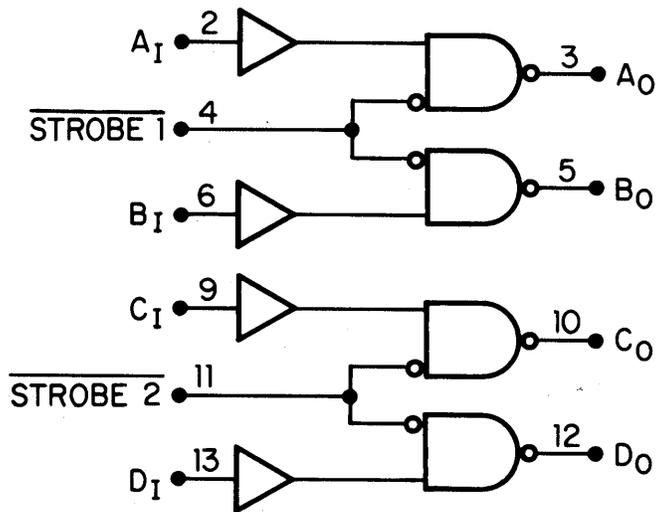
DG-02427

PIN 1 = V_{CC1}
PIN 7 = GND
PIN 8 = V_{EE}
PIN 14 = V_{CC2}
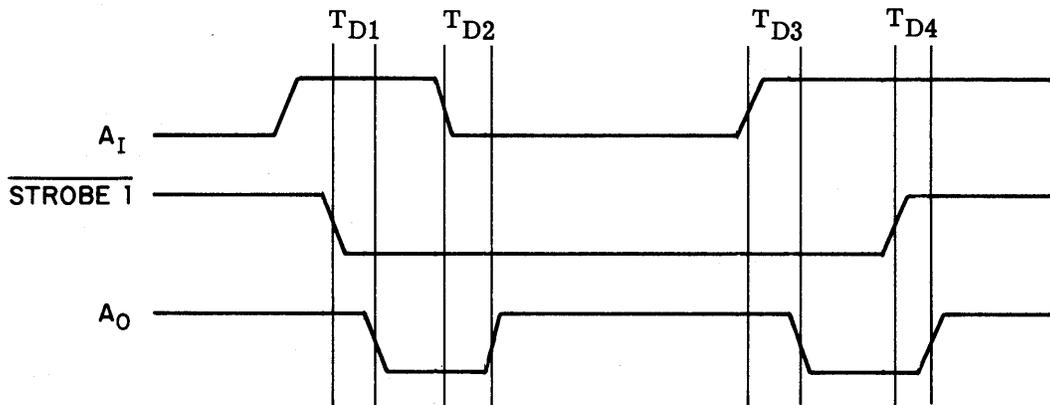
DG-02349

Conditions:

V_{CC1} = __+5__ Volts
V_{CC2} = __+5__ Volts
V_{EE} = __-5__ Volts
Load = __160__ Ω to V_{CC1}, 200pF to ground

Input Rise Times __5__ ns
Input Fall Times __5__ ns

T_{D1}	Range	__7__	to	__15__	ns
T_{D2}	Range	__25__	to	__38__	ns
T_{D3}	Range	__10__	to	__22__	ns
T_{D4}	Range	__7__	to	__15__	ns

SECTION VIII

mN629
CPU I/O TRANSCEIVER

● **PACKAGE**

● **PIN NAMES AND NUMBERS**

● **DC (STATIC) CHARACTERISTICS**

● **FUNCTIONAL DESCRIPTION**

PACKAGE

The mN629 integrated circuit is supplied in a 20-pin plastic dual in-line package (DIP).

PIN NUMBERS AND NAMES

I/O DATA 1	1		20	V_{CC}
$\overline{\text{B I/O DATA 1}}$	2		19	I/O DATA 2
B I/O DATA 1	3		18	$\overline{\text{B I/O DATA 2}}$
$\overline{\text{CLEAR}}$	4		17	B I/O DATA 2
$\overline{\text{I/O INPUT}}$	5		16	I/O CLOCK
I/O INPUT	6		15	$\overline{\text{B I/O CLOCK}}$
PHASE B	7		14	B I/O CLOCK
PHASE A	8		13	BMCLOCK
MCLOCK	9		12	$\overline{\text{BMCLOCK}}$
GND	10		11	V_{EE}
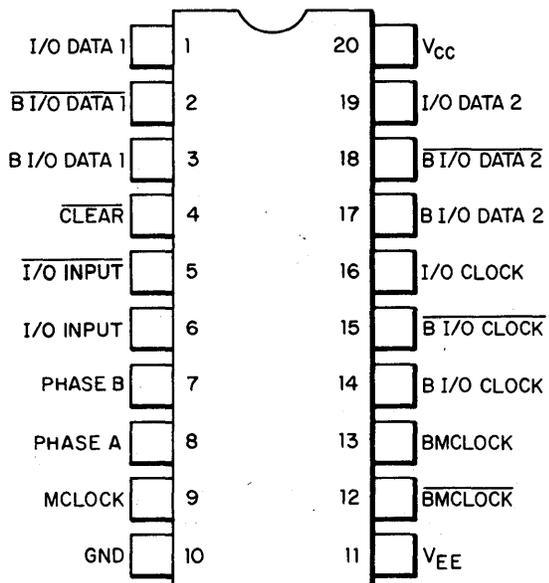
D6-02355 D6-02405

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range V_{CC}	-0.5	to +7Volts
Supply Voltage Range V_{EE}	+0.5	to - 7Volts
Input Voltage Range V_I	-0.5	to +5.5Volts
Transmitter Output Current Range I_{OT}	0	to 80 mAmps
All Other Output Current Range I_O	0	to 50 mAmps
Operating Temperature Range T_A	0	to 70°C
Storage Temperature Range T_{stg}	-25	to +150°C
Average Power Dissipation	0.95 Watts	

NOTES *All voltages in this document are referenced to V_{SS} (ground).*

*Subjecting a circuit to conditions either outside these limits or at these limits for an extended period of time may cause irreparable damage to the circuit. As such, these ratings are not intended to be used during the operation of the circuit. Operating specifications are given in the DC (STATIC) CHARACTERISTICS TABLE.

DC (STATIC) CHARACTERISTICS
mN629

OPERATING SPECIFICATIONS

T_A Range 0 to +70°C I_{EE} = -20 mAmps Average

V_{CC_6} = 5± 0.25Volts I_{GND} = 150 mAmps Average

I_{CC} = +170mAmps Average   GND = 0± 0.0Volts

V_{EE} = -5± 0.25Volts

CHARACTERISTIC	SYMBOL	UNITS	PINS	LIMITS MIN.	LIMITS MAX.
INPUT LOW VOLTAGE	V_{IL}	Volts	MCLOCK	-	+0.8
			I O INPUT	-	+0.8
			I/O CLOCK, I/O DATA1, I/O DATA 2 I/O INPUT, CLEAR	-	+0.8
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	+0.8	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	+0.8	-
INPUT CURRENT FOR LOW STATE	I_{IL}	mAmps	MCLOCK	-	-4.8
			I O INPUT	-	-3.2
			I/O CLOCK, I/O DATA1, I/O DATA2, INPUT, CLEAR	-	-1.6
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	-
INPUT HIGH VOLTAGE	V_{IH}	Volts	MCLOCK	+2.0	-
			I O INPUT	+2.0	-
			I O CLOCK, I O DATA1, I O DATA2, I O INPUT, CLEAR	+2.0	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	+2.0
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	+2.0
INPUT CURRENT FOR HIGH STATE	I_{IH}	mAmps	MCLOCK	-	+0.12
			I O INPUT	-	+0.08
			I O CLOCK, I O DATA1, I O DATA2, I O INPUT, CLEAR	-	+0.04
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	-
OUTPUT LOW VOLTAGE	V_{OL}	Volts	α 1,3 and α 2,4	-	+0.4
			I O CLOCK, I O DATA1, I O DATA2, I O INPUT	-	+0.4
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	-	+0.4
OUTPUT CURRENT FOR LOW STATE	I_{OL}	mAmps	α 1,3 and α 2,4	+5	-
			I O CLOCK, I O DATA1, I O DATA2, I O INPUT	+16	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	+25	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	+25	-
OUTPUT HIGH VOLTAGE	V_{OH}	Volts	α 1,3 and α 2,4	+2.5	-
			I O CLOCK, I O DATA1, I O DATA2, I O INPUT	+2.5	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	+2.3	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	-	*
OUTPUT CURRENT FOR HIGH STATE	I_{OH}	mAmps	α 1,3 and α 2,4	-	-0.4
			I O CLOCK, I O DATA1, I O DATA2, I O INPUT	-	-0.4
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	-	+25
INPUT CAPACITANCE	C_I	pF	MCLOCK	-	7
			I O INPUT	-	7
			I O CLOCK, I O DATA1, I O DATA2, I O INPUT, CLEAR	-	7
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	7
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	7

*Leakage = 60µAmps @ 2.5V

NOTE

Logic "1" is defined as the more positive voltage as are the maximum figures given under voltage limits. Logic "0" is defined as the more negative voltage as are the minimum figures given under voltage limits.

Positive current, in the conventional sense, is defined as flowing into the pin.

FUNCTIONAL DESCRIPTION
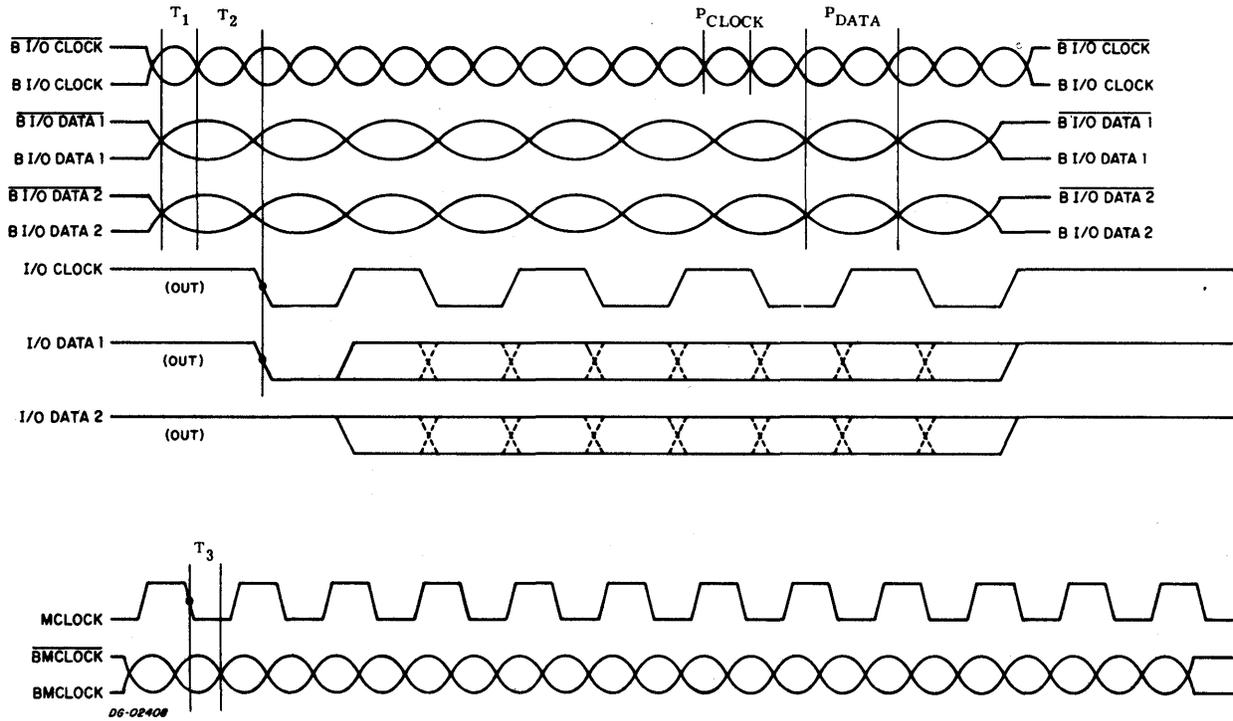
Conditions:

V_{CC} = +5.0Volts
V_{EE} = -5.0Volts
P_{CLOCK} = 60ns
P_{DATA} = 120ns

	Min. (ns)	Max. (ns)
T_1	40	60
T_2	43	55
T_3	5	18

Output rise and fall times range 3 to 12 ns

mN629

VIII-5

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V_{CC}=PIN 20
V_{EE}=PIN 11
GND=PIN 10
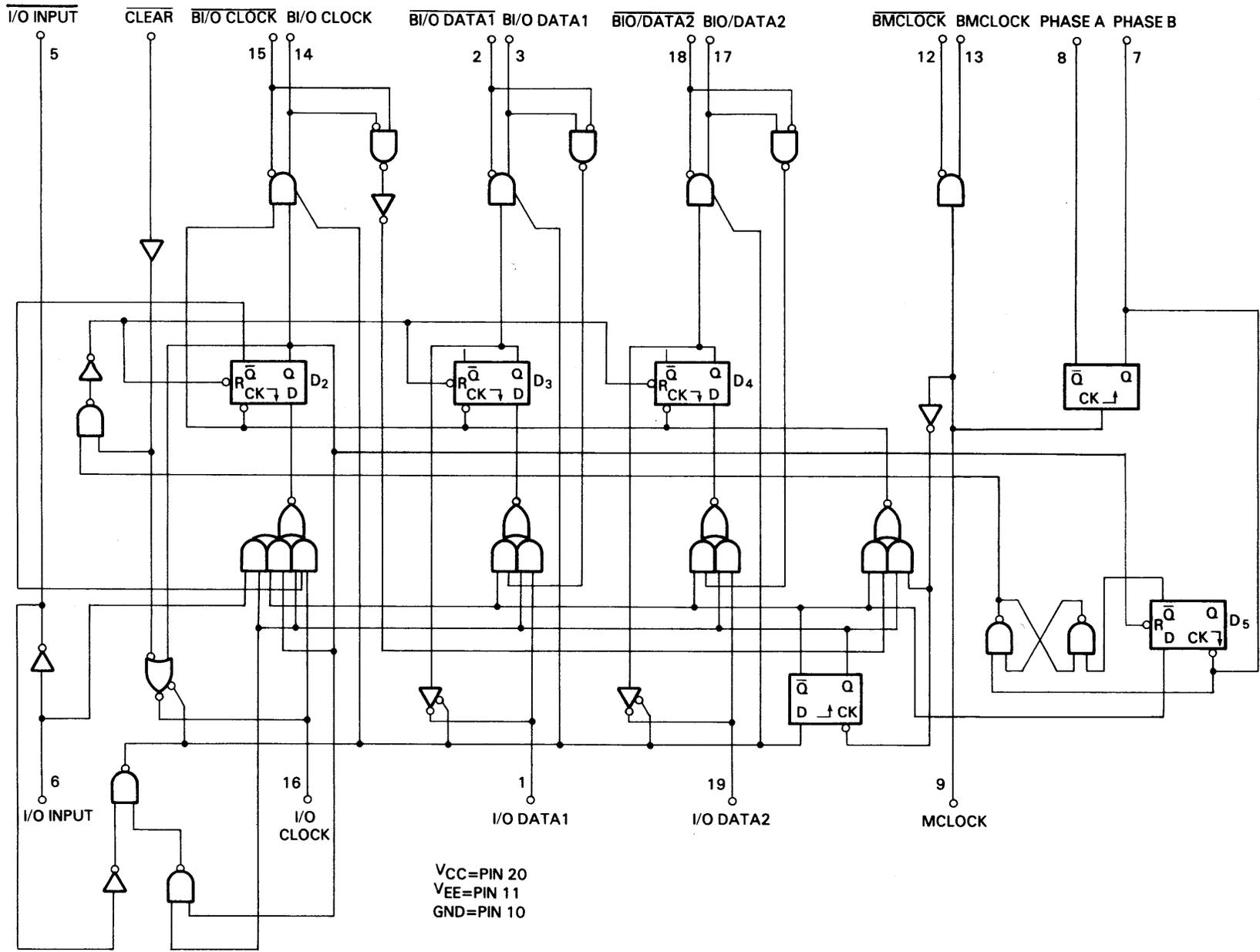
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SECTION IX

mN636
IOC I/O TRANSCEIVER

- PACKAGE

- PIN NAMES AND NUMBERS

- DC (STATIC) CHARACTERISTICS

- FUNCTIONAL DESCRIPTION

PACKAGE

The mN636 integrated circuit is supplied in a 20-pin plastic dual in-line package (DIP).

── PIN NUMBERS AND NAMES ──

I/O DATA 1	1	20	V_{CC}
$\overline{\text{B I/O DATA 1}}$	2	19	I/O DATA 2
B I/O DATA 1	3	18	$\overline{\text{B I/O DATA 2}}$
$\overline{\text{CLEAR}}$	4	17	B I/O DATA 2
$\overline{\text{I/O INPUT}}$	5	16	I/O CLOCK
I/O INPUT	6	15	$\overline{\text{B I/O CLOCK}}$
PHASE B	7	14	B I/O CLOCK
PHASE A	8	13	BMCLOCK
MCLOCK	9	12	$\overline{\text{BMCLOCK}}$
GND	10	11	V_{EE}

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── ABSOLUTE MAXIMUM RATINGS* ──

Supply Voltage Range V_{CC}	-0.5 to +7 Volts
Supply Voltage Range V_{EE}	+0.5 to -7 Volts
Input Voltage Range V_I	-0.5 to +5.5 Volts
Transmitter Output Current Range I_{OT}	0 to 80 mAmps
All Other Output Current Range I_O	0 to 50 mAmps
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	-25 to +150°C
Average Power Dissipation	0.95 Watts

NOTES *All voltages in this document are referenced to GND.*

*Subjecting a circuit to conditions either outside these limits or at these limits for an extended period of time may cause irreparable damage to the circuit. As such, these ratings are not intended to be used during the operation of the circuit. Operating specifications are given in the DC (STATIC) CHARACTERISTICS TABLE.

mN636

OPERATING SPECIFICATIONS

T_A Range 0 to +70°C I_{CC} = +170mAmps Average

V_{CC} = 5± 0.25 Volts I_{EE} = -20mAmps Average

V_{EE} = 5± 0.25 Volts I_{GND} = +150mAmps Average

GND   = 0 ± 0.0 Volts

CHARACTERISTIC	SYMBOL	UNITS	PINS	LIMITS MIN.	LIMITS MAX.
INPUT LOW VOLTAGE	V_{IL}	Volts	I/O INPUT	-	+0.8
			I/O CLOCK, I/O DATA1, I/O DATA2, I/O INPUT, CLEAR	-	+0.8
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	+0.8	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	+0.8	-
INPUT CURRENT FOR LOW STATE	I_{IL}	mAmps	I/O INPUT	-	-3.2
			I/O CLOCK, I/O DATA1, I/O DATA2, I/O INPUT, CLEAR	-	-1.6
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	-
INPUT HIGH VOLTAGE	V_{IH}	Volts	I/O INPUT	-	+2.0
			I/O CLOCK, I/O DATA1, I/O DATA2, I/O INPUT, CLEAR	-	+2.0
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	+2.0	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	+2.0	-
INPUT CURRENT FOR HIGH STATE	I_{IH}	mAmps	I/O INPUT	-	+0.08
			I/O CLOCK, I/O DATA1, I/O DATA2, I/O INPUT, CLEAR	-	+0.04
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	-	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	-	-
OUTPUT LOW VOLTAGE	V_{OL}	Volts	PHASE A, PHASE B	-	+0.4
			I/O CLOCK, I/O DATA1, I/O DATA2, I/O INPUT, CLEAR	-	+0.4
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	+0.4
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	+0.4
OUTPUT CURRENT FOR LOW STATE	I_{OL}	mAmps	PHASE A, PHASE B	+5	-
			I/O CLOCK, I/O DATA1, I/O DATA2, I/O INPUT	+16	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	+25	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	+25	-
OUTPUT HIGH VOLTAGE	V_{OH}	Volts	PHASE A, PHASE B	+2.5	-
			I/O CLOCK, I/O DATA1, I/O DATA2, I/O INPUT	+2.5	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	+2.3	-
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	*
OUTPUT CURRENT FOR HIGH STATE	I_{OH}	mAmps	PHASE A, PHASE B	-	-0.4
			I/O CLOCK, I/O DATA1, I/O DATA2, I/O INPUT	-	-0.4
			BI/O CLOCK, BI/O DATA1, BI/O DATA2	-	+25
INPUT CAPACITANCE	C_I	pF	INPUT	-	7
			I/O CLOCK, I/O DATA1, I/O DATA2, I/O INPUT, CLEAR	-	7
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	-	7
			BI/O CLOCK, BI/O DATA1, BI/O DATA2, BMCLOCK	-	7

*Leakage = 60μAmps @ 2.5V

NOTE

Logic "1" is defined as the more positive voltage as are the maximum
figures given under voltage limits. Logic "0" is defined as the more
negative voltage as are the minimum figures given under voltage limits.

Positive current, in the conventional sense, is defined as flowing
into the pin.

━ FUNCTIONAL DESCRIPTION ━
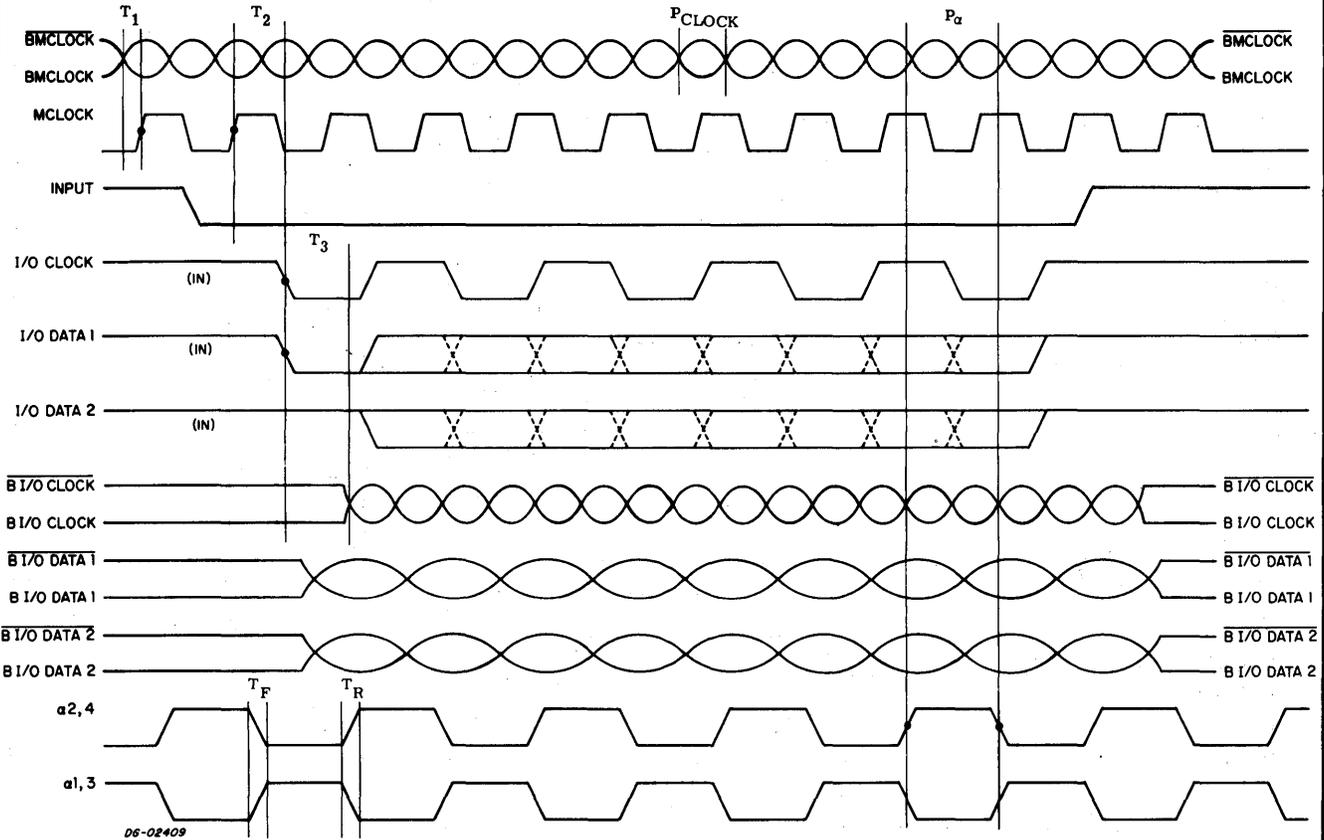
Conditions:

V_{CC1} = +5.0Volts

V_{EE} = -5.0Volts

P_{CLOCK} = 60ns
P_α = 120ns

	MIN. (ns)	MAX. (ns)
T_1	45	55
T_2	55	60
T_3	27	40
T_F	3	10
T_R	10	20

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I/O INPUT
CLEAR
BI/O CLOCK
BI/O CLOCK
BI/O DATA1
BI/O DATA1
BIO/DATA2
BIO/DATA2
BMCLOCK
BMCLOCK
α1,3
α2,4

5
4
15
14
2
3
18
17
12
13
8
7

D2
D3
D4
D5

6
16
1
19
9

I/O INPUT
I/O CLOCK
I/O DATA1
I/O DATA2
MCLOCK

VCC=PIN 20
VEE=PIN 11
GND=PIN 10
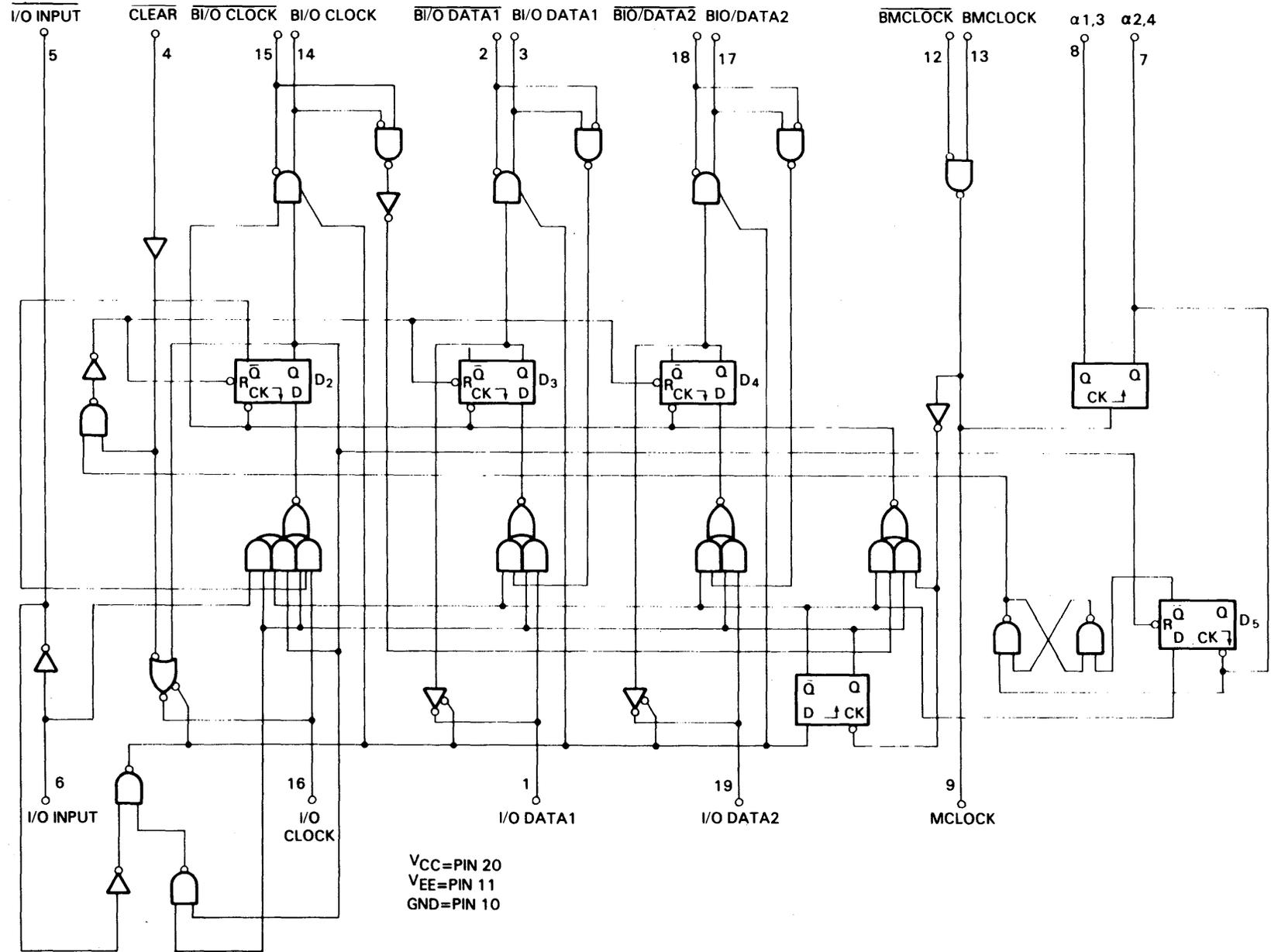
microNOVA CPU MODULE
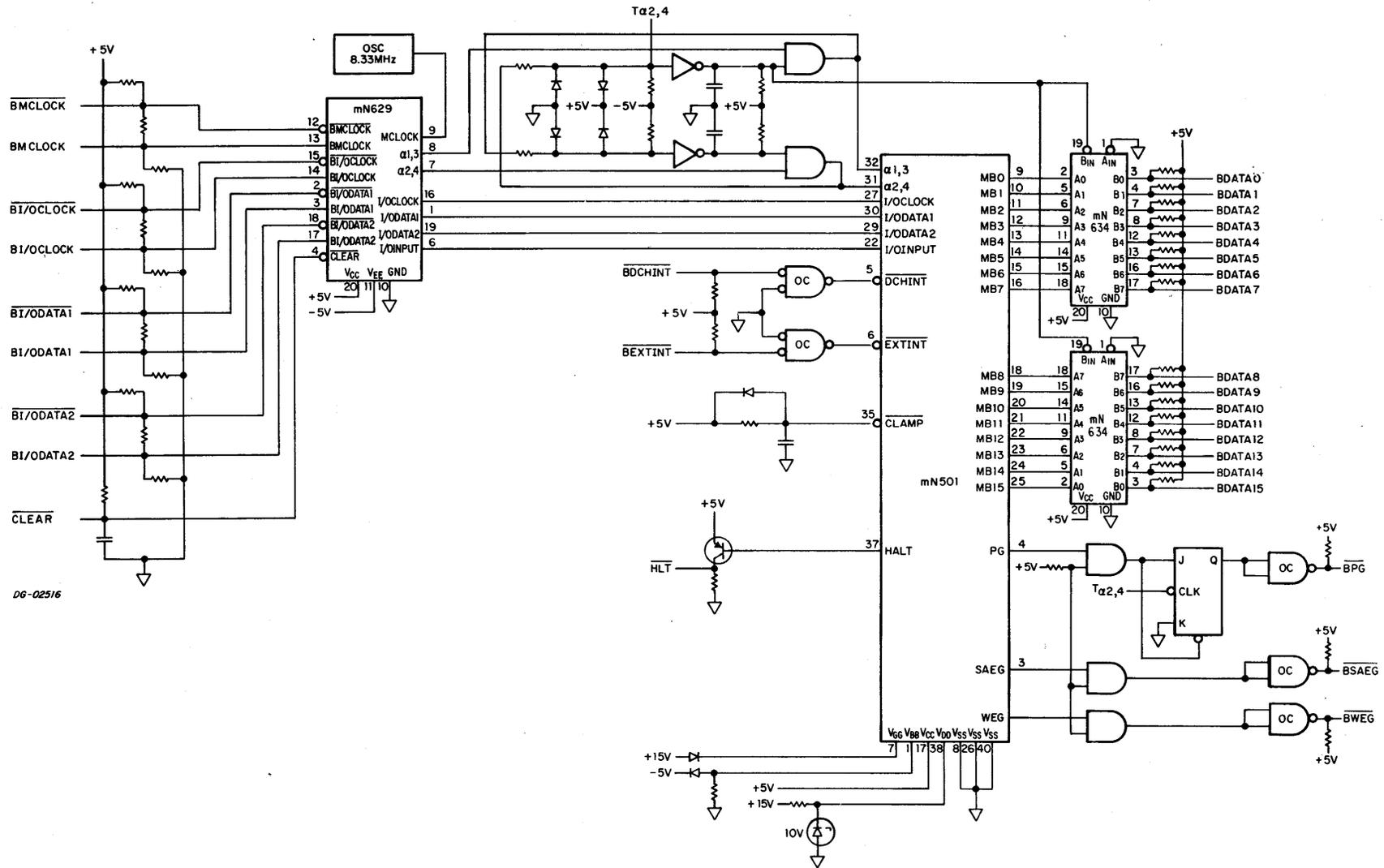
DG-02516

SECTION X
CPU MODULE

INTRODUCTION

As indicated in the introductory section of this manual, a microNOVA CPU (mN501), two memory transceivers (mN633) and a CPU I/O transceiver (mN629) may be connected to form a CPU module. Such a module also includes resistors, capacitors, diodes, transistors and SSI TTL components. The following schematic diagram shows what components are required and how they are connected.

FUNCTIONAL OVERVIEW

The CPU module is functionally identical to the CPU circuit.

EXERNAL
ELECTRICAL CONNECTIONS

The external electrical connections to a CPU module are of four kinds: power, memory bus, I/O bus and $\overline{\text{HLT}}$. The connections of each type are discussed below.

Power

The CPU module requires power at +5 volts DC, +15 volts DC and -5 volts DC.

The +5 volt source is connected directly to pin Vcc of the CPU circuit, the pin Vcc of each memory transceiver, the pin Vcc of the CPU I/O transceiver and to all TTL components. It is connected to signals of the memory bus and signals of the I/O bus through pull-up resistors. It is also divided through a resistor and zener diode to yield the signal V+ at an intermediate voltage used as a high input to TTL gates.

The +15 volt source is connected directly to the driving components of the clock driver circuit and through a voltage-drop diode to the pin Vgg of the CPU circuit. It is also divided by a resistor and zener diode to yield the operating voltage specified for the pin Vdd of the CPU circuit.

The -5 volt source is connected directly to the pin Vee of the CPU I/O transceiver. It is also divided through a resistor and diode to yield the operating voltage specified for the pin Vbb of the CPU circuit.

Memory Bus

The memory bus is the group of signals via which the CPU module communicates with memory locations. It includes the signals $\overline{\text{BPG}}$, $\overline{\text{BWEG}}$, $\overline{\text{BSAEG}}$ and BDATA[0-15]. The protocols that the CPU module follows in communications via these signals are functionally identical to those followed by the CPU circuit in communications via the pins PG, SAEG, WEG and MB[0-15] respectively.

I/O Bus

The I/O bus is the group of signals via which the CPU module communicates with peripherals. It includes the signals BMCLOCK, $\overline{\text{BMCLOCK}}$, BI/OCLOCK, $\overline{\text{BI/OCLOCK}}$, BI/ODATA1, $\overline{\text{BI/ODATA1}}$, BI/ODATA2, $\overline{\text{BI/ODATA2}}$, $\overline{\text{CLEAR}}$, $\overline{\text{BEXTINT}}$ and BDCHINT.

The signals BMCLOCK and $\overline{\text{BMCLOCK}}$ are a differential pair of master clock signals. They carry complementary square waves with frequencies equal to the frequency of the output of the oscillator connected to the pin MCLOCK of the CPU I/O transceiver (ordinarily 8.333 MHz).

BI/OCLOCK, $\overline{\text{BI/OCLOCK}}$, BI/ODATA1, $\overline{\text{BI/ODATA1}}$, BI/ODATA2 and $\overline{\text{BI/ODATA2}}$ are differential pairs of signals that carry information between peripherals and the CPU module. The signals BI/OCLOCK, BI/ODATA1 and BI/ODATA2 are functionally identical to the pins I/O CLOCK, I/O DATA1 and I/O DATA2 (respectively) of the CPU circuit, and $\overline{\text{BI/OCLOCK}}$, $\overline{\text{BI/ODATA1}}$ and $\overline{\text{BI/ODATA2}}$ are their respective complements.

The signal $\overline{\text{CLEAR}}$ is a system reset signal that may be pulled to low level by any element of the microNOVA computer system.

The signals $\overline{\text{BEXTINT}}$ and $\overline{\text{BDCHINT}}$ are I/O request signals that may be pulled to low level by any peripheral to transmit an interrupt or data-channel request to the CPU module.

All of the I/O bus signals are TTL-compatible signals. The signals $\overline{\text{MCLOCK}}$, $\overline{\text{BI/OCLOCK}}$, $\overline{\text{BI/ODATA1}}$, $\overline{\text{BI/ODATA2}}$, BEXTINT, $\overline{\text{CLEAR}}$, and $\overline{\text{BDCHINT}}$ have external pull-up resistors and are driven by TTL open-collector drivers. The signals MCLOCK, BI/OCLOCK, BI/ODATA1, and BI/ODATA2 have external pull-down resistors and are driven by open-emitter drivers. There are also terminating resistors between the signals of each differential pair.

HLT

The signal $\overline{\text{HLT}}$ indicates whether or not the CPU module is halted. It carries the information transmitted via the pin HALT of the CPU circuit. It is frequently used to control a "RUN" indicator (typically a light-emitting diode).

Because the electrical characteristics of the pin HALT are not TTL compatible and are not suitable for driving a light-emitting diode, the signal $\overline{\text{HLT}}$ has a push-up resistor and is driven by a PNP transistor.

CIRCUIT ELEMENTS

The components of the CPU module are functionally divided into the following groups: CPU circuit, memory control driver circuitry, memory transceiver circuitry, I/O transceiver circuitry, I/O request receiver circuitry, an oscillator, clock driver circuitry, clamp circuitry and power circuitry.

The CPU circuit is the microNOVA CPU.

The memory control driver circuitry is the source of $\overline{\text{BPG}}$, $\overline{\text{BSAEG}}$ and $\overline{\text{BWEG}}$. It consists of TTL open-collector drivers and pull-up resistors. It also includes a J-K flip-flop that synchronizes the levels of $\overline{\text{BPG}}$ with the levels of the pins alpha 1,3 and alpha 2,4.

The memory transceiver circuitry is the source and destination of the signals BDATA[0-15]. It consists of memory transceivers and pull-up resistors. The memory transceivers drive the signals BDATA[0-15] (i.e., transmit from MB[0-15]) at all times. However, they drive the pins MB[0-15] of the CPU (i.e., receive from BDATA 0-15) only when the pin alpha 1,3 is at high level. This ensures that the memory transceivers do not pull the pins MB[0-15] to low voltage while they are precharged.

The I/O transceiver circuitry is the source of the signals MCLOCK and $\overline{\text{MCLOCK}}$; it is the source and destination of BI/OCLOCK, $\overline{\text{BI/OCLOCK}}$, BI/ODATA1, $\overline{\text{BI/ODATA1}}$, BI/O DATA2 and $\overline{\text{BI/ODATA2}}$; and it is the destination of $\overline{\text{CLEAR}}$. It consists of a CPU I/O transceiver and pull-up, pull-down and terminating resistors for these signals.

The I/O request circuitry is the destination of $\overline{\text{BEXTINT}}$ and $\overline{\text{BDCHINT}}$. It consists of TTL receivers and terminating resistors.

The oscillator is the master timing generator for the entire microNOVA computer system. It ordinarily yields a square wave with a frequency of 8.333MHz. The CPU I/O transceiver transmits this clock to the clock driver in the CPU module via its pins alpha 1,3 and alpha 2,4 and to all peripherals via the signals MCLOCK and $\overline{\text{MCLOCK}}$.

The clock driver circuitry drives the clock pins of the CPU circuit. It consists of two voltage and current amplifiers (represented here as AND gates) and a network of voltage dividing resistors, clamping diodes and delay capacitors. This network ensures that the outputs of the amplifiers are never in the high state concurrently (i.e., that the alpha 1,3 and alpha 2,4 clocks do not overlap).

The clamp circuitry ensures a delay between the time when power at +5 volts DC comes up and the time when the pin CLAMP of the CPU goes to high level. It consists of a capacitor, a resistor and a diode. When power goes down, the capacitor is discharged rapidly through the diode. When power comes up, the capacitor is charged relatively slowly through the resistor.

The power circuitry yields voltages within the specified operating ranges of the power pins of the other components of the CPU module from the +5, +15 and -5 volt sources. It consists of filter capacitors and voltage dividing resistors and diodes.

SECTION XI
4K x 16-bit RAM MODULE

INTRODUCTION

As indicated in the introductory section of this manual, sixteen 4K dynamic RAMs (mN606), two address drivers (mN633) and four sense amp/bus drivers (mN506) may be connected to form a 4K x 16-bit RAM module. Such a module also includes resistors, capacitors, diodes and SSI TTL components.

FUNCTIONAL OVERVIEW

The 4K x 16-bit RAM contains 4096 16-bit memory locations and performs read, write, read-modify-write and refresh operations on them in accordance with the protocols that the microNOVA CPU module follows in communications with memory. It performs read, write and read-modify-write operations on one location at a time and performs refresh operations on sixty-four locations at a time. The module determines which operations to perform and which location(s) to perform them on from information received via the signals $\overline{BPG}$, $\overline{BWEG}$, $\overline{BSAEG}$ and BDATA[0-15].

In accordance with the protocols that the CPU module follows in communications with memory, the memory location on which a read, write, or read-modify-write is performed is specified by a 15-bit address. Since only a 12-bit address is necessary to select one of 4096 locations within the module, three bits of the address determine whether or not the module performs any operation on a location at all; these bits are called the module select bits of the address. The module select bits are the same in the addresses of all locations in the RAM module. This permits as many as eight RAM modules to operate on one microNOVA memory bus. Each of these modules contains locations with a different set of 4096 addresses; the address of every location in one module differs from the addresses of locations in every other module in the module select bits.

EXTERNAL ELECTRICAL CONNECTIONS

The external electrical connections to a 4K x 16-bit RAM module are of two kinds: power and memory bus.

Power

The 4K x 16-bit RAM module requires power at +5 volts DC, +15 volts DC and -5 volts DC.

The +5 volt source is connected directly to the pin V_{cc} of each RAM circuit, the pin V_{cc} of each address driver, the pin V_{cc} of each sense amp and to all TTL components. It also is connected to the signals of the memory bus via pull-up resistors.

The +15 volt source is connected directly to the driving comonents of the clock driver circuit. It is also divided through a resistor and zener diode to yield the operating voltage specified for V_{DD} of the RAM circuits.

The -5 volt source is connected directly to the pin V_{EE} of each sense amplifer.

Memory Bus

The memory bus is the group of signals via which the 4K x 16-bit RAM module communicates with the central-processing unit and other elements of the computer system. It includes the signals BPG, BWEG, BSAEG, and BDATA[0-15]. The protocols the module follows in communications via these signals are those followed by the microNOVA CPU module.

CIRCUIT ELEMENTS

The components of the 4K x 16-bit RAM module are functionally divided into the following groups: address driver circuitry, RAMs, module select circuitry, control driver circuitry, sense amp/bus drivers, and power circuitry.

The address driver circuitry receives BDATA[0-15] and drives the information they carry (addesses and data) onto DI[0-15]. It consists of address drivers and pull-up resistors for DI[0-15].

The RAM circuits are connected in such a way that each RAM circuit contains one bit of every memory location in the module. The signals DI[4-15] are connected to each one in parallel so that they all receive the same addresses. Similarly, the outputs of the control drivers are connected to each RAM circuit in parallel, so that they all latch addresses and write data simultaneously. Only the data inputs and data outputs differ from one RAM circuit to another. The data input of each RAM circuit receives information from a different memory bus address/data line, so that when data is written to the memory module, a different bit is written into each RAM circuit. Similarly, the data output of each RAM module transmits information to a different memory bus address/data line, so that when data is read from the memory module, a different bit is read from each RAM circuit. The memory bus address/data line from which each RAM circuit receives data is the address/data line on which the circuit transmits data.

The module select circuitry determines whether the module is to perform an operation when BPG goes to low level to initiate a read, write or read-modify-write operation. It consists of three open-collector EXCLUSIVE-OR gates and a pull-up resistor. The output of the module select circuitry is at high level only if the module select bits of the address on BDATA[1-15] have the values selected by the jumpers W1, W2 and W3.

The control driver circuitry receives the signals BPG, BWEG and BSAEG and transmits the control information they carrry to the RAM circuits in the module via MP0, MP1, MSAE and MWEG. It consists of NOR gates, clock drivers and an inverter. If the output of the module select logic is high or bit 0 of the address is 1 (i.e., the operation is a refresh operation), cross-coupled NOR gates latch high when BPG goes to low level. When the latched output of these NOR gates is high, the module is active. The clock drivers (represented here as AND gates) drive the P pins of all the RAM circuits to high level to latch the address whenever the module becomes active. MSAE is only asserted when the module is active. MWE may be asserted whether the module is active or not; however, if the module is not active, MP0 and MP1 are at low level, so the RAM circuits are not affected.

The sense amp/bus drivers are the inteface between the data outputs of the RAM circuits and the address/data ines of the memory bus. There are four of them.

The power circuitry yields voltages within the operating ranges specified for the V_{BB} and V_{DD} pins of the RAM circuits. It consists of voltage dividing resistors and diodes.
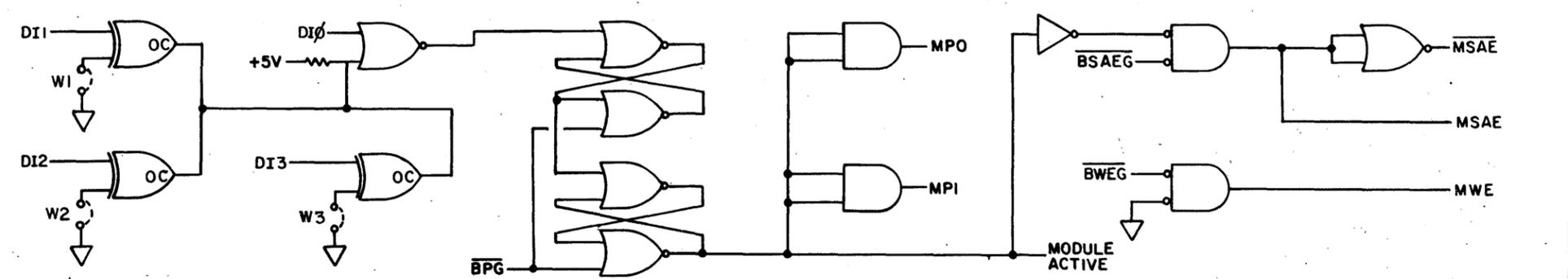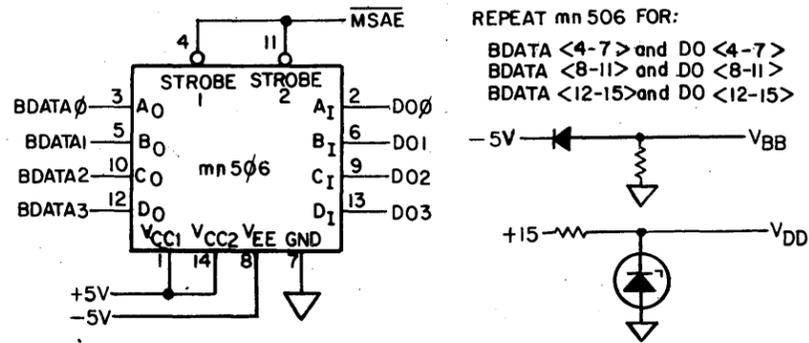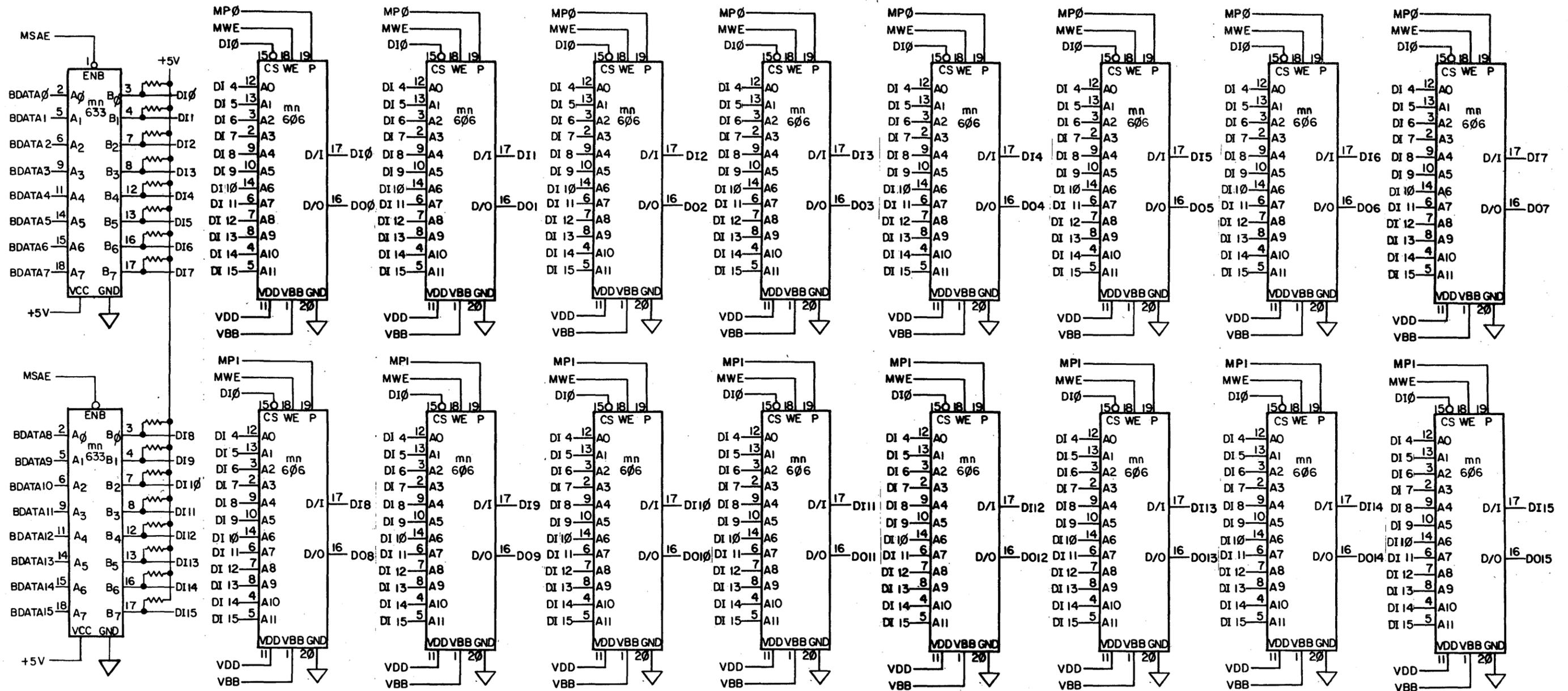
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SECTION XII
IOC MODULE

INTRODUCTION

As indicated in the introductory section of this manual, a microNOVA IOC (mN603) and an IOC I/O transceiver (mN633) may be conected to form an IOC module. Such a module also includes resistors, capacitors, diodes and SSI TTL components. The schematic diagram on the following page shows what components are required and how they are connected.

FUNCTIONAL OVERVIEW

The IOC Module is functionally identical to the microNOVA IOC.

EXTERNAL ELECTRICAL CONNECTIONS

The external electrical connections to the IOC module are of three kinds: power, I/O bus, and device signals. The connections of each type are discussed below.

Power

The IOC module requires power at +5 volts DC, +15 volts DC and -5 volts DC.

The +5 volt source is connected directly to the pin Vcc of the IOC circuit, the pin Vcc of the IOC I/O transceiver and to all TTL components.

The +15 volt source is connected directly to the driving components of the clock driver circuit and through a voltage-drop diode to the pin Vgg of the IOC circuit. It is also divided through a resistor and a zener diode to yield the operating voltage specified for the pin Vdd of the IOC circuit.

The -5 volt source is connected directly to the pin Vee of the IOC I/O transceiver. It is also divided through a resistor and diode to yield the operating voltage specified for the pin Vbb of the CPU.

I/O Bus

The I/O bus is the group of signals via which the IOC module communicates with a central-processing unit. It includes the signals $\overline{\text{BMCLOCK}}$, BMCLOCK, $\overline{\text{BI/OCLOCK}}$, BI/OCLOCK, $\overline{\text{BI/ODATA1}}$, BI/ODATA1, BI/ODATA2, $\overline{\text{BI/ODATA2}}$, $\overline{\text{CLEAR}}$, $\overline{\text{BEXTINT}}$ and $\overline{\text{BDCHINT}}$.

The signals BMCLOCK and $\overline{\text{BMCLOCK}}$ are a differential pair of master clock signals. They must receive complementary square waves. Ordinarily these square waves are provided by a CPU module. They have frequencies of 8.333 MHz and are synchronized with the clock signals in the central-processing unit.

The signals BI/OCLOCK, $\overline{\text{BI/OCLOCK}}$, BI/ODATA1, $\overline{\text{BI/ODATA1}}$, BI/ODATA2 and $\overline{\text{BI/ODATA2}}$ are are differential pairs of signals that carry information between a central-processing unit and the IOC module. The signals BI/OCLOCK, BI/ODATA1 and BI/ODATA2 are functionally identical to the pins I/O CLOCK, I/O DATA1 and I/O DATA2 (respectively) of the IOC circuit, and $\overline{\text{BI/OCLOCK}}$, $\overline{\text{BI/ODATA1}}$ and $\overline{\text{BI/ODATA2}}$ are their respective complements.

The signal $\overline{\text{CLEAR}}$ is a system reset signal that may be pulled low by any element of the microNOVA computer system.

The signals $\overline{\text{BEXTINT}}$ and $\overline{\text{BDCHINT}}$ are I/O request signals via which the IOC module transmits interrupt and data-channel requests.

All of the I/O bus signals are TTL-compatible bus signals. The signals $\overline{MCLOCK}$, $\overline{BI/OCLOCK}$, $\overline{BI/ODATA1}$, $\overline{BI/ODATA2}$, $\overline{CLEAR}$, $\overline{BEXTINT}$ and $\overline{BDCHINT}$ are driven by open-collector drivers. The signals MCLOCK, BI/OCLOCK, BI/ODATA1 and BI/ODATA2 are driven by open-emitter drivers. It is expected that these signals are connected to appropriate pull-up, pull-down and terminating resistors in the central-processing unit.

Device Signals

The device signals are the signals via which the IOC module communicates with the other components of the peripheral of which it is a part. They are busy/done signals, request signals, the device control signals and device data signals.

The busy/done signals are the signals via which the peripheral controls and monitors the contents of the busy and done bits in the IOC circuit. They are the signals SET BUSY, SET DONE, BUSY and DONE. The signals SET BUSY and SET DONE drive the pins $\overline{BUSY}$ and $\overline{DONE}$ of the IOC circuit, and the signals BUSY and DONE transmit the states of those pins.

The request signals are the signals via which the peripheral indicates that it requires interrupt and data-channel requests. They are the signals $\overline{INT\ SYNC}$ and $\overline{DCH\ SYNC}$. Functionally, the signals $\overline{INT\ SYNC}$ and $\overline{DCH\ SYNC}$ are identical to the pins $\overline{INT\ SYNC}$ and $\overline{DCH\ SYNC}$ (respectively) of the IOC circuit.

The device control signals are the signals via which the IOC module indicates the operations that it is performing to the peripheral. These signals indicate, among other things, whether the IOC module is transmitting or receiving data via the device data signals and, if so, what the significance of that data is. There is one device control signal for each code transmitted via the function code pins of the IOC circuit; the signals are listed in the following table.

DATOA	IOPLS
DATIA	IORST
DATOB	MSKO
DATIB	DCHA
DATOC	DCHI
DATIC	DCHO
STRT	WCEZ
CLR	NOP

The device data signals carry data between the IOC module and the other components of the peripheral. They are D[0-15] and $\overline{D[0-15]}$.

Priority Signals

The priority signals are signals via which the IOC module communicates with other peripherals to determine whether it should respond to data-channel-acknowledge codes and interrupt-acknowledge commands that it receives via the I/O bus and to indicate that it is making data-channel and interrupt requests. The priority signals are INTP IN, INTP OUT, DCHP IN, and DCHP OUT.

CIRCUIT ELEMENTS

The components of the IOC module are functionally divided into the following groups: IOC circuit, IOC I/O transceiver circuitry, I/O request drivers, busy/done circuitry, function decoder circuitry, device data drivers, priority circuitry, I/O reset drivers, a mask-out driver, clock driver circuitry and power circuitry.

The IOC circuit is the microNOVA IOC.

The IOC I/O transceiver circuitry is the source and destination of the signals BI/OCLOCK, $\overline{BI/OCLOCK}$, BI/ODATA1, $\overline{BI/ODATA1}$, BI/ODATA2 and $\overline{BI/ODATA2}$; it is the destination of the signals MCLOCK, $\overline{MCLOCK}$ and $\overline{CLEAR}$. It consists of an IOC I/O transceiver and a filter capacitor for $\overline{CLEAR}$. The I/O request drivers are sources of the signals $\overline{BEXTINT}$ and $\overline{BDCHINT}$. It consists of open-collector TTL bus drivers.

The busy/done circuitry is the source of the signals BUSY and DONE and the destination of the signals SET BUSY and SET DONE. It consists of TTL drivers.

The function decoder is the source of the device control signals. It is a TTL MSI 4-to-16 decoder. The control signals it asserts are determined by the function codes transmitted via the pins SF[0-3] of the IOC circuit. The function decoder is enabled only when the pin $\overline{FSTROBE}$ of the IOC circuit is in the low state, so that control signals are only asserted when the states of the pins F[0-3] of the IOC circuit are stable.

The device data drivers are the source of the device data signals. They are TTL drivers.

The priority circuitry is the source of the signals INTP OUT and DCHP OUT and the destination of the signals INTP IN and DCHP IN. It consists of open-collector TTL AND gates. According to the protocols of the microNOVA I/O bus, the signal INTP IN is at high level in a peripheral if no peripheral of higher priority is making an interrupt request. It is the obligation of each peripheral to pull the signal INTP OUT to low level if and only if the peripheral is making an interrupt request or some higher priority peripheral is making an interrupt request (i.e., the signals INTP IN is at low level). The signals INTP OUT of each peripheral is the signal INTP IN of the peripheral of immediately lower priority. The I/O bus protocols constrain the signals DCHP IN, DCHP OUT and the making of data-channel requests in a similar way.

IOC I/O
TRANSCEIVER
mN636

IOC
mN603

4-TO-16
DECODER

DG-02527
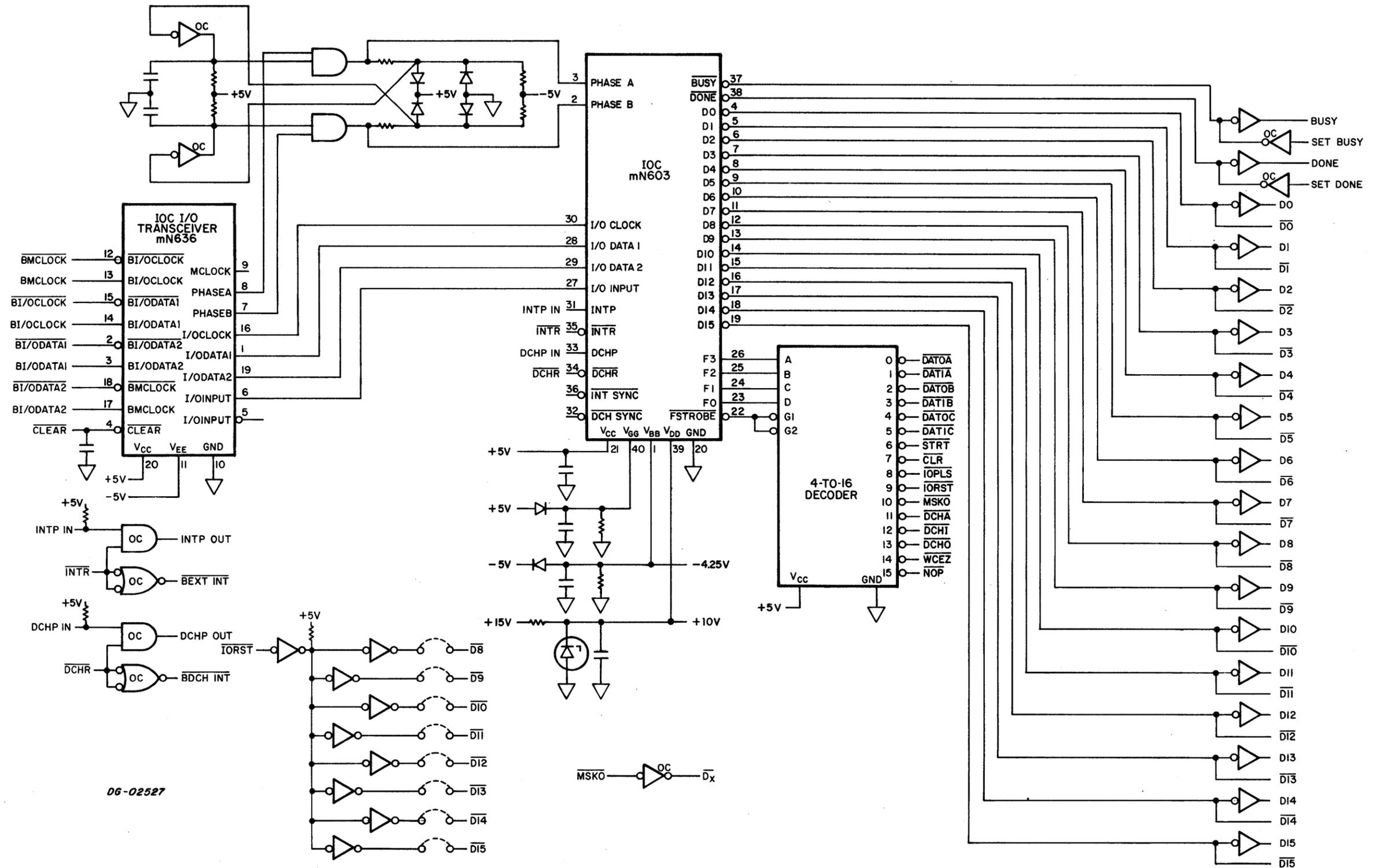
The I/O reset drivers transmit the device code of the peripheral and the new contents of the external-register-enable and polarity bits to the IOC circuit when the device control signal IORST is asserted. This signal is asserted after the IOC circuit is reset and when it is executing an I/O reset command, and indicates that the IOC is to load its device code register, external-register-enable bit and polarity bit from the signals D[8-15]. The device data signals that are pulled low by these drivers depend on the device code of the peripheral and the desired contents of those control bits; as shown, they are determined by jumpers.

The mask-out driver pulls one of the device data signals to low level when the device control signal MSKO is asserted. This signal is asserted when the IOC circuit is executing a mask-out command, and indicates that the IOC circuit is to accept a mask word

from D[0-15]. The device data signal that is pulled low by the mask-out driver depends on the mask bit of the peripheral. As shown, the driver is connected to Dx , where Dx is any of D[0-15].

The clock driver circuitry drives the clock pins of the IOC circuit. It consists of two voltage and current amplifers (represented here as AND gates) and a network of voltage dividing resistors, clamping diodes and delay capacitors. This network ensures that the outputs of the amplifiers are never in the high state concurrently (i.e., that the PHASEA and PHASEB clocks do not overlap).

The power circuitry yields voltages within the specified operating ranges of the power pins of the other components of the IOC module from the +5, +15 and -5 volts sources. It consists of filter capacitors and voltage dividing resistors and diodes.

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APPENDIX A
PACKAGE
SPECIFICATIONS

40-PIN CERAMIC

20-PIN CERAMIC

0.975 / 0.930

20 19 18 17 16 15 14 13 12 11

0 025 R NOM

1 2 3 4 5 6 7 8 9 10

0.310 / 0.290

0.300 / 0.245

0.050 NOM

SEATING PLANE

105° / 90° 20 PLACES

0.014 / 0.008

0 070 MAX 20 PLACES

GLASS SEALANT

0.170 MAX

0 130 MIN

0 020 MIN

0 012 MIN 4 PLACES

0.030 MIN 16 PLACES

0.023 / 0.015 20 PLACES

0.050 / 0.015 4 PLACES

PIN SPACING 0 100 TP

20-PIN PLASTIC

1 070 MAX

20 19 18 17 16 15 14 13 12 11

0.093 R NOM

0 160 NOM

1 2 3 4 5 6 7 8 9 10

0.300 · 0 010

0 250 · 0 010

0.080 NOM

0.010 NOM

0.200 MAX

105° / 90° 20 PLACES

SEATING PLANE

0.011 · 0.003 20 PLACES

0.155 / 0.125

0.325 ±0.025 10 PLACES

0.070 MAX 20 PLACES

0.020 MIN

0.033 MIN 20 PLACES

0.018 ± 0.003 20 PLACES

0.075 MAX 4 PLACES

PIN SPACING 0.100 T.P.

14-PIN CERAMIC

0.785 / 0.755

14 13 12 11 10 9 8

0.025 R NOM

1 2 3 4 5 6 7

0.310 / 0.290

0.280 / 0.245

0.050 NOM

105° / 90° 14 PLACES

SEATING PLANE

0.014 / 0.008

0.070 MAX 14 PLACES

GLASS SEALANT

0.200 MAX

0.130 MIN

0.020 MIN

0.100 / 0.070 4 PLACES

0.030 MIN 14 PLACES

0.023 / 0.015 14 PLACES

PIN SPACING 0.100 TP

A-2

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