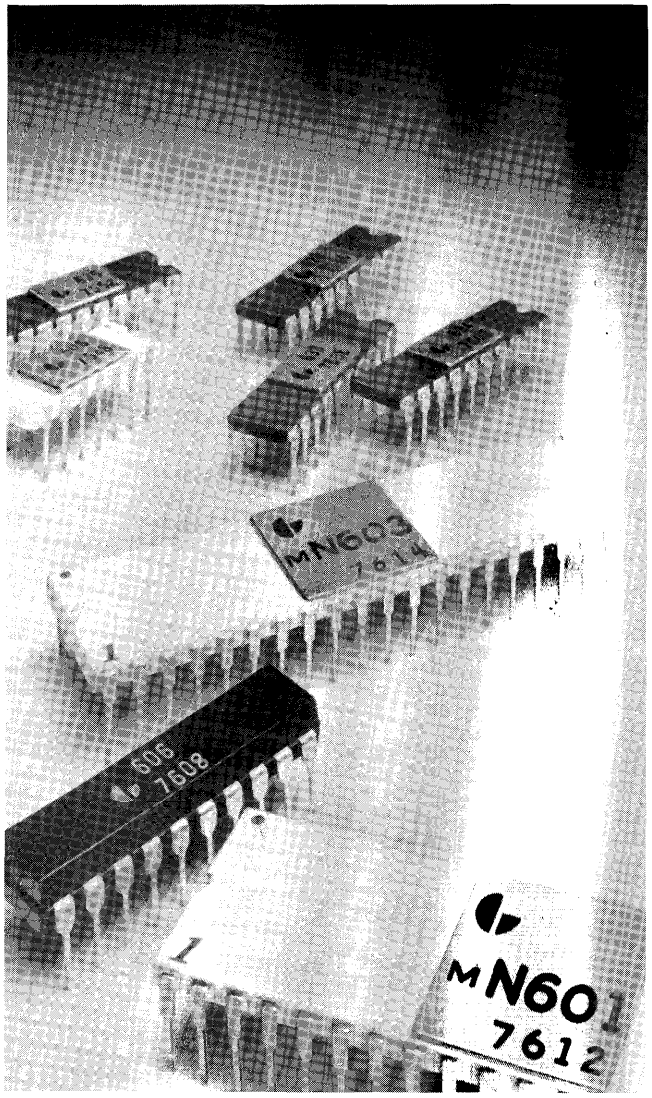
DataGeneral

FEATURES

- Complete microprocessor chip set based on Data General's advanced in-house, silicon-gate NMOS technology.
- Designed as a total microprocessor system with optimized distribution of function in memory, I/O, and buffers.
- System expandable to 32Kwords, with multiple high-performance I/O devices.
- mN601 microprocessor: 40-pin NMOS microNOVA CPU
  - full NOVA 16-bit architecture and instruction set on a single chip, plus:
    - hardware stack and frame pointer
    - powerful SAVE and RETURN instructions for subroutine calls
    - 16-bit multiply and divide
    - real-time clock
    - all memory control and timing
    - integral hidden refresh logic for dynamic RAMs
    - per-device data channel control
- mN603 I/O Controller (IOC): 40-pin NMOS circuit
  - "intelligent" I/O device control
  - interprets and executes NOVA I/O instruction set
  - provides simple 16-bit parallel user interface
  - integral Busy and Done control
  - integral device identification and interrupt control
  - data channel control logic
  - full address and word count register for data channel operation
- mN606 4K RAM: 20-pin NMOS dynamic Random Access Memory circuit
  - fast 160-nanosecond access time
  - separate pins for all 12 address bits plus data in and data out
- System Buffer Elements (SBE's): for full expansion capability and high noise immunity
  - mN634 Octal Memory Bus Transceiver buffers 16-bit parallel memory bus
  - mN633 Octal Memory Address Driver provides address and bank drive for 4K- or 8K-word memory array
  - mN506 Quad Sense Amplifier strobes memory data onto 16-bit memory bus
  - mN629 and mN636 I/O Transceivers provide bidirectional I/O bus buffering up to 100 feet
- Supporting microNOVA peripheral interfaces:
  - general purpose I/O
  - asynchronous controller
  - diskette subsystem
- Packaging accessories
  - 9-slot cardframe/backplane
  - expansion chassis
  - power supply
  - battery backup
  - handheld programmer's console
  - console debug
  - PROM programmer
  - extender boards



DESCRIPTION

Data General's microNOVA chip set facilitates engineering evaluation of circuit components and gives users an economical way to design and manufacture microcomputers. The set is based on the Data General-manufactured silicon-gate NMOS mN601 microprocessor that implements the complete 16-bit NOVA architecture plus multiply/divide, and real-time clock in a single 40-pin ceramic Dual-Inline-Package. The CPU is supported by Data General-manufactured mN606 4K Random Access Memory and the mN603 I/O Controller (IOC), as well as System Buffer Elements. The 4096-bit mN606 uses cost-effective dynamic RAM technology to implement the microNOVA family's large memory orientation. The mN603 IOC delivers the full functional capability of NOVA's 47-line I/O bus, and incorporates controller functions that simplify interfacing. Data General designed and manufactured System Buffer Elements using standard bipolar and advanced Schottky processes let microNOVA support up to 32K words of memory and a full complement of peripherals.

The microNOVA chip set is compatible with the other elements of the microNOVA family -- the computer-on-a-board and the completely packaged MOS minicomputer. The microNOVA family comes with proven Data General development and run-time software that includes the Real-Time Operating System and the diskette-based Disc Operating System. A NOVA 3-based development system is also available.

The Data General worldwide service network gives microNOVA users wide-ranging support that includes training, documentation, maintenance, and a large staff of sales engineers and systems support specialists.

These features make the microNOVA family ideal for applications like complex instrumentation, industrial automation, communications, and data acquisition, where 16-bit NOVA power and precision are required.

mN601 CENTRAL PROCESSING UNIT

The microNOVA mN601 CPU features the NOVA 16-bit, multi-function instruction set, including hardware multiply/divide; multiple addressing modes including absolute, relative, indexed, deferred, and auto increment/decrement; multiple accumulators, including two that can be used as index registers; hardware stack and frame pointers with stack overflow protection; programmed priority interrupt to 16 levels; and separate memory and input/output busses. A Real-Time Clock and Random Access Memory refresh control are an integral part of the CPU. It also incorporates all CPU and memory control for per-device DataChannel (DMA).

The microNOVA CPU features an input/output structure with a unique encoding/decoding scheme that, in conjunction with the IOC chip, provides the functional equivalent of the 47-line NOVA bus. The differentially driven I/O bus can extend up to 100' with no performance degradation.

Programmed priority interrupt enables real-time response to random events. Hardware stacks facilitate reentrant and recursive subroutine programming. Multiple accumulators reduce program size. Multiple addressing modes ensure efficient memory use. And the powerful microNOVA instruction set increases programmer productivity.

mN603 I/O CONTROLLER

The mN603 IOC is a 40-pin package that provides an "intelligent" I/O bus interface for each peripheral device. It provides the function of the 47-line NOVA I/O bus by decoding a 16.6 megabit/second encoded data stream from the CPU and presenting a 16-bit bidirectional interface, 4 encoded function bits, and a function strobe, for simple interfacing. The "intelligent" IOC goes beyond this bus adapter function to incorporate complex functions that are outboard on the most powerful minicomputer systems. It includes integral device identification, BUSY-DONE interrupt logic, and a per-device interrupt masking capability. For block-oriented controllers, it includes data channel (DMA) bus hand-shaking, and full 15-bit address and block length registers. Power-up initialization logic, orderly power shutdown circuitry, and user-selectable data bus signal polarity are also provided.

mN606 4096-BIT DYNAMIC RAM

Data General's mN606 RAM is organized 4096-bits by one. Its 20-pin packaging permits separate pins for each of 12 address bits as well as data in and data out. The chip access time is 160 nanoseconds-one of the fastest in the industry - and contributes significantly to the microNOVA family's high performance.

SYSTEM BUFFER ELEMENTS

Five high-density Data General designed and manufactured SBE's, using standard bipolar and Schottky processes, give the microNOVA family its full expansion capability and high noise immunity. Two mN634 Memory Bus Transceivers, each handling eight lines, buffer the 16-bit parallel memory bus. Two mN633 Memory Address Drivers, each handling eight lines, provide the address and bank-selection drive for each 4K-word memory array.

Four mN506 Sense Amplifier/Bus Drivers, each sensing four mN606 RAM "data out" signals, strobe buffered data directly onto the 16-bit memory bus.

The mN629 CPU I/O Transceiver and the mN636 IOC I/O Transceiver buffer the I/O bus. They provide differential drive and receive circuits for noise immunity and hundred-foot length. They also clock bus signals in transmit mode and reclock them in receive mode using a high noise immunity detection scheme.

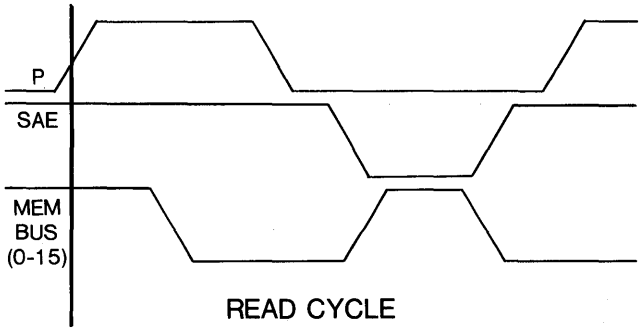
Standard Bipolar Chips A few Small Scale Integration (SSI) TTL chips and discrete components like diodes, resistors, and capacitors handle miscellaneous functions. The microNOVA signal levels are compatible with industry standard bipolar parts.

MEMORY BUS

A clock generator that produces a two-phase clock provides microNOVA timing information for the mN601 CPU and I/O circuits. This clock synchronizes memory and I/O with the CPU.

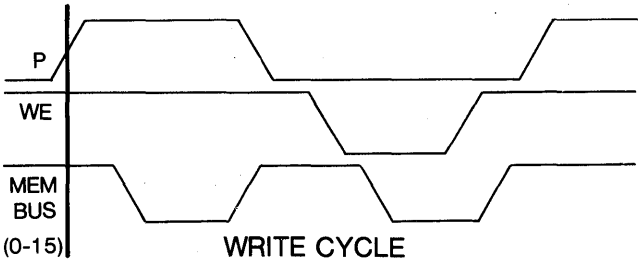
The CPU memory bus consists of 16 bidirectional data lines (used for both address and data) and three control lines. During any memory cycle, the data lines are first driven with the address of the location that has to be accessed. All memory cycles are initiated by asserting the P signal. The CPU performs three kinds of data transfer operations via the memory bus: read, write, read-modify-write.

Read Cycle. At the beginning of the read cycle the P signal is asserted and the CPU data lines are driven by the two mN634s. Address values are in bits 1 through 15 with zero in bit 0. The addresses are buffered in each memory array by two mN633s, and latched by the P signal in the RAM chips. Later in the cycle, as the RAM chips present the data at the addressed memory cells, SAE (Sense Amp Enable) is asserted. The data lines in the "selected" memory array are gated onto the memory bus, back through the mN634s, and into the CPU.



READ CYCLE

Write Cycle. On the write cycle, the P signal is asserted and the data lines are driven by the CPU with the address values in bits 1 through 15, with bit 0 again zero. The RAMs latch the address. Later in the cycle, the CPU outputs the data to be written, and WE (write enable) strobes the new data into the "selected" memory array.



WRITE CYCLE

Read-Modify-Write Cycle. In a read-modify-write operation, data is transfered to the CPU from a memory location and different data (the result of an operation performed on the transfered data) is transfered back from the CPU to the same location. A read-modify-write cycle can occur if SAE (Read) is enabled first and then WE is enabled later without having the P signal go high.

Refresh Cycles. On refresh cycles, only the low-order six bits of the data bus are used, and bit 0 of the address is forced to a one. This has the effect of disabling the CS (chip select) input on all the MOS memories and, as a result, refreshing 64 storage cells in each 4K RAM simultaneously. Sixty-four refresh cycles with all the possible values of the six least-significant bits of the memory address are provided by the CPU every two milliseconds. A unique "hidden refresh" technique overlaps refresh with CPU execution, so no performance degradation occurs.

I/O BUS

The microNOVA I/O bus consists of nine signals, some driven differentially for noise immunity at high data rates. It can be extended up to 100 feet from the CPU, carried on an economical, easy-to-handle, 16-line flat-ribbon cable. It provides communications between the CPU chip and multiple IOC chips (typically one IOC per device interfaced to the CPU). Bus transceivers provide bidirectional buffering for signals placed on the I/O bus by the CPU chip or any of the IOC chips.

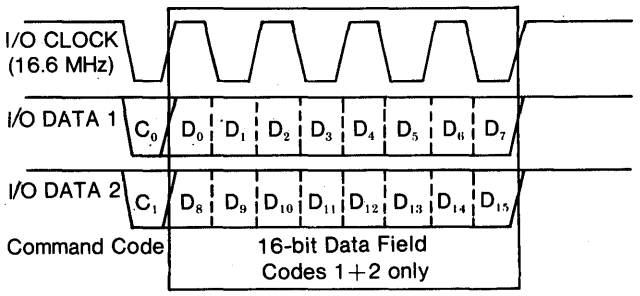
Synchronization. Two signals provide initialization and system synchronization: MASTER CLOCK (driven differentially), and CLEAR.

Interrupts. Four lines are used to coordinate program interrupts and data channel (DMA) breaks. The "External Program Interrupt Request" (EXT INT) and "Data Channel Interrupt Request" (DCH INT) signals coming into the CPU are the wired "OR" of all the IOC's "Request" signals. For Program Interrupts, each IOC is preset under software control to one of sixteen priority levels. IOC's above the "System Priority Level" set by the CPU at any given time may issue an interrupt. If more than one IOC interrupts during a single CPU instruction, the one closest to the CPU along the chained 'Interrupt Priority"(INTP) signal will have its interrupt honored. In the case of the Data Channel, multiple "Requests" during the same CPU instruction will similarly be arbitrated by the chained "Data Channel Priority" (DCHP) signal.

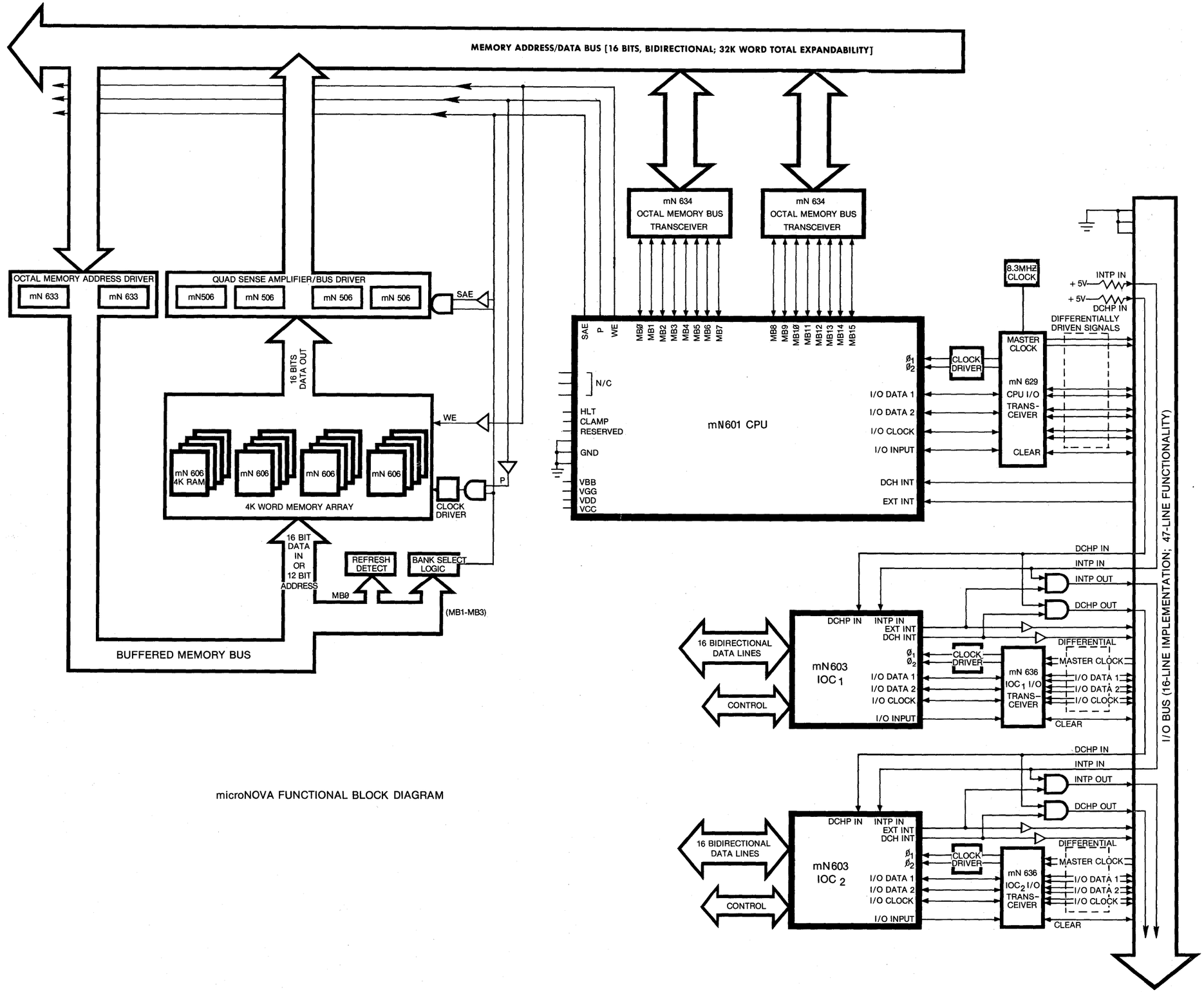
Data Transfers. Data transfer occurs on two differentially driven, bidirectional data lines (IODATA 1 and IODATA 2), clocked by the I/O clock signal. Clock rate is 8.3 million bits per second on each line, for an aggregate data transfer rate of 16.6 million bits per second. There are four types of data transfer, each identified by the value of IODATA 1 and IODATA 2 at the first clock pulse.

Code 1 is "I/O Command" and transfers I/O instruction commands from the CPU to IOC, where they are executed. Code 2 is "I/O Data", and transmits data words in either direction between the CPU and selected IOC. The codes for "I/O Command" and "I/O Data" are immediately followed by a trailing 16-bit data field (eight bits per data line); the entire 18-bit burst takes 2.16 microseconds.

Code 3 is "Request Enable", and is issued by the CPU to synchronize pending program interrupts and data channel breaks. Code 4 is "Data Channel Address Request", issued by the CPU to request a memory address from the IOC previously synchronized for a data channel operation. Codes 3 and 4 do not have any trailing data fields associated with them, taking only a single clock pulse.



The IOCs provide full decoding of this command stream, making bus protocol transparent to the user. The IOC provides a fully parallel 16-bit data bus for device interfacing and incorporates common controller functions for programmed I/O, program interrupt, and data channel (DMA) functions.



microNOVA FUNCTIONAL BLOCK DIAGRAM

microNOVA FAMILY SUPPORT

The microNOVA chip set is supported by a number of microNOVA family components that let users integrate at the chip, board, or fully packaged MOS minicomputer level.

Memory Boards. 4K- and 8K-word RAM boards support the microNOVA 32K-word memory capacity. These boards feature NMOS technology, fast access time, and refresh control from the microNOVA CPU. Additional 1/2K-, 1K-, 2K-, and 4K-word PROM modules are used in applications where programs or data must be fixed permanently within the system. A PROM programmer board permits PROM chip burning under program control.

Interface Boards. An asynchronous interface board connects teleprinters and 6012 video displays to the microNOVA I/O bus. It also provides full modem control, including automatic answer capability. The firmware-based Console Debug Option for the asynchronous interface board allows any ASCII console to supervise program execution as well as examine and/or modify RAM location and CPU registers. A general-purpose interface board provides a generalized programmed I/O, program interrupt, and data channel interface plus predrilled areas for user-designed and built circuitry.

Software. The microNOVA family is supported by powerful Data General runtime software including the Real-Time Operating System (RTOS), Symbolic Debugger, and libraries for arithmetic subroutines, character handling, and I/O.

Data General's RTOS is a powerful real-time executive. It is compact and memory resident, and has real-time multitasking capabilities for controlling real-time applications. RTOS provides standard interrupt servicing, device handling, and execution scheduling functions.

The Symbolic Debugger facilitates debugging with symbolic designation of user labels, assembler mnemonics, and program offsets. Symbolic references allow program debugging in source-language terms that do not require cumbersome binary translation.

Data General libraries cover complex character-formatting I/O routines, logarithmic, exponential and trigonometric function evaluation, and comprehensive array handling.

Development Systems. microNOVA and NOVA 3 development systems complement the microNOVA family. The microNOVA system features an MOS microNOVA minicomputer with 16K words memory, automatic program load, battery backup, power fail/auto restart, handheld programmer's console, terminal subsystem, and dual diskette subsystem. The diskette subsystem provides 157K words (single drive) or 315K words (dual drive) of on-line storage, and includes a Data Channel controller.

The NOVA 3 development system includes a 16K NOVA 3/12 with automatic program load, battery backup, power-fail/auto-restart, programmer's console, terminal subsystem, and dual diskette subsystem. Expansion options allow system growth to 128K words memory, with NOVA peripherals, and the Real-Time Disc Operating System (RDOS).

Both microNOVA and NOVA 3 development systems operate under Data General's diskette based Disc Operating System (DOS). DOS is supported by a Command Line Interpreter, Text Editor, Macro Assembler, Library File Editor, Relocatable Loader and FORTRAN IV Compiler, in addition to the microNOVA RTOS capabilities. The NOVA 3/12 development system operates under the same software. Full program compatibility between microNOVA and NOVA 3, and the diskette's format compatibility permit easily transported software between development systems.

Customer Support. Data General maintains a worldwide support network that offers users contractual services for Applications Engineers, Service Engineers, and Customer Training. Software and Hardware Subscription Services are available. The Data General User's Group allows interchange of user programs. Each system is supported by full technical documentation.

SPECIFICATIONS

CHIP SET COMPONENTS

mN601 CPU Circuit - 40-pin, NMOS microprocessor.
mN634 Octal Memory Bus Transceivers (2 per CPU) - 20-pin bipolar.
mN606 4K RAM (16 per 4K-word array) - 20-pin NMOS.
mN633 Octal Memory Address Driver (2 per memory array) - 20-pin bipolar.
mN506 Quad Sense Amplifier (4 per memory array) - 14-pin bipolar.
mN629 CPU I/O Transceiver (1 per CPU) - 20-pin bipolar.
mN603 I/O Controller (1 per interface) - 40-pin NMOS.
mN636 I/O Transceiver (1 per IOC) - 20-pin bipolar.

CPU

Word Length: 16 bits.
General-Purpose Accumulators: 4.
Stack Facility: 1 Stack Pointer, 1 Frame Pointer.

MEMORY

Memory CycleTime: 960 nanoseconds.
Memory Configurability: RAM/PROM memory combinations up to 32K words.

INPUT/OUTPUT SYSTEM

16 priority-level interrupt structure, 61-device Programmed I/O addressability.

GENERAL

Add Time: 2.4 microseconds.
Accumulator Load Time: 2.9 microseconds.
Address Modes: Absolute, indexed, deferred, relative and auto-increment/decrement.
Bus System: Separate I/O and Memory busses.
Direct Memory Access Channel: Input - 148,000 words/second; output - 173,000 words/second.

ENVIRONMENTAL

Temperature Range: 0°C to 55°C operating; -35°C to 70°C storage.
Relative Humidity: to 90% operating; to 95% storage.
Altitude Range: to 10,000' operating; to 50,000' storage.

Southboro, Massachusetts 01772, (617) 485-9100, TWX (710) 390-0309, TLX 94-8460, Waltham MA, Scottsdale AZ, El Segundo CA, Palo Alto CA, Sacramento CA, San Diego CA, San Francisco CA, Santa Ana CA, Santa Barbara CA, Denver CO, North Haven CT, Orlando FL, St. Petersburg FL, Atlanta GA, Peoria IL, Richmond VA, Schaumburg IL, Indianapolis IN, Louisville KY, Baton Rouge LA, Southfield MI, Minneapolis MN, Clayton MO, Kansas City MO, Saddle Brook NJ, Albuquerque NM, Buffalo NY, Commack Long Island NY, Ithaca NY, New York NY, Rochester NY, Schenectady NY, Syracuse NY, Greensboro NC, Wayne NJ, Euclid OH, Dayton OH, Tulsa OK, Portland OR, Blue Bell PA, Carnegie PA, Austin TX, Dallas TX, HoustonTX, Salt Lake City UT, Falls Church VA, Renton WA, Menomonee Falls WI, Calgary Alta., Edmonton Alta., North Vancouver B.C., Winnipeg Man., London Ont., Mississauga Ont., Dollard-Des-Ormeaux P.Q., Hull P.Q., and in Australia, Austria, Belgium, Brazil, Costa Rica, Denmark, England, Finland, France, Greece, Hong Kong, Iran, Italy, Japan, Korea, Malaysia, Mexico, Netherlands, Philippines, Portugal, Puerto Rico, Scotland, Singapore, Spain, Sweden, Switzerland, West Germany

---