

TEXT LISTING

068-000638-01

PROGRAM

MICRO-NOVA DIGITAL TO ANALOG
INTERFACE EXERCISER

TEXT TAPE

097-000638-01

ABSTRACT

THE PURPOSE OF THIS EXERCISER IS TO PROVIDE A MEANS OF FINDING AND TROUBLE-SHOOTING PROBLEMS IN THE ANALOG SECTION OF THE D-A BOARD. THIS IS ACCOMPLISHED BY A SERIES OF TESTS WHICH ARE WRITTEN AS SCOPE LOOPS AND DISPLAY A PATTERN ON THE FACE OF THE "O" SCOPE FOR VISUAL VERIFICATION.

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; PROGRAM NAME: MNDAE.TX          PART NUMBER: 097-000638
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; DESCRIPTION: MICRO-NOVA DIGITAL TO ANALOG INTERFACE EXERCISER
;
; REVISION HISTORY:
;
; REV.      DATE
;
; 00      04/28/78
; 01      08/18/78
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; 1. PROGRAM NAME:
; MNDAE - MICRO NOVA DIGITAL TO ANALOG EXERCISER
; SOURCE FILE- MNDAE.SR (094-001-058-RR)
;
; 2. REVISION HISTORY:
; REV. 00 - 04/28/78
; REV. 01 - 08/18/78 (TO ALLOW FOR SHORT TIME-
;           OUTS IN "Z-PULSE" CKTS.)
;
; 3. MACHINE REQUIREMENTS:
; A) MICRO NOVA CPU WITH MINIMUM OF 4K READ/WRITE
;    MEMORY IN ADDRESSES 0-7777 (OCTAL)
; B) ASYNCHRONOUS INTERFACE FOR THE MICRO NOVA
; C) TTY OR CRT TERMINAL WITH DEVICE CODE 10 FOR INPUT
;    AND DEVICE CODE 11 FOR OUTPUT
; D) PAPER TAPE READER, OR DISKETTE DRIVE
;
; 4. TEST REQUIREMENTS:
; A) MICRO NOVA D-A INTERFACE BOARD
; B) THIS TEST: MNDAE.AB - 095-000638
;               MNDAE.LS - 096-000638
; C) EITHER W22 OR W21 ON THE D-A BOARD MUST BE IN
;    FOR THE INTENSITY TEST (Z MODE)
; D) AN OSCILLOSCOPE COMPARABLE TO THE TEKTRONIX 465
;    IS NEEDED TO RUN ALL THE TESTS; HOWEVER, PROVISIONS
;    HAVE BEEN MADE SO THAT PRELIMINARY TESTING CAN BE
;    DONE WITH A VOLT METER.
; E) FOR CALIBRATION AT LEAST A FOUR AND A HALF DIGIT
;    VOLT METER WILL BE NEEDED.
; F) THE DIGITAL TO ANALOG INTERFACE DIAGNOSTIC
;    (PM. 095-000-340-RR) MUST FIRST RUN ON
;    THE BOARD UNDER TEST BEFORE STARTING THIS
;    EXERCISER

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15. SUMMARY:
THE PURPOSE OF THIS EXERCISER IS TO PROVIDE A MEANS
OF FINDING AND TROUBLE-SHOOTING PROBLEMS IN THE ANALOG
SECTION OF THE D-A BOARD. THIS IS ACCOMPLISHED BY A
SERIES OF TESTS WHICH ARE WRITTEN AS SCOPE LOOPS AND
DISPLAY A PATTERN ON THE FACE OF THE "0" SCOPE FOR
VISUAL VERIFICATION.

16. RESTRICTIONS:
1) THIS TEST IS APPLICABLE TO ONE D-A INTERFACE AT
A TIME.
2) ALL DEVICES CONNECTED TO THE D-A SHOULD BE RE-
MOVED.
3) WITH THE EXCEPTION OF DONE NOT SETTING WITHIN A
REASONABLE TIME OR A LATE CONVERSION, NO ERROR
DETECTION OR REPORTING TAKES PLACE. ALL ERROR
DETECTION IS BY OBSERVATION OF THE "0" SCOPE
FOR THE PROPER DISPLAY(S).

17. PROGRAM DISCUSSION / THEORY OF OPERATION:

NOTE: THE FOLLOWING CONVENTION IS USED IN THE
DESCRIPTION TO INDICATE LOW ACTIVE SIGNALS:

/ SIGNALNAME/ = SIGNALNAME

1) DIGITAL TO ANALOG CONVERTER OPERATION:
A) THE D/A INTERFACE FOR THE MICRO NOVA CONSISTS OF
TWO 12-BIT HYBRID D/A CONVERTERS WITH SCOPE CONTROL,
LOGIC AND INTERFACE CIRCUITRY. VOLTAGE RANGES FOR
THE DACS (JUMPER SELECTABLE) ARE 0-5, 0-10,
+/- 5, +/- 10 VOLTS DC. THE VOLTAGE RANGES OF THE TWO
DACs ARE INDEPENDENT OF EACH OTHER. MAXIMUM SETTLING
TIME TO 0.01% OF FULL SCALE READING IS TYPICALLY 7 US.
LINEARITY AND DIFFERENTIAL LINEARITY ARE EACH +/-
1/2 LSB AND CONVERSION IS MONOTONIC. EACH DAC HAS
AN OUTPUT AMPLIFIER ENABLING IT TO DRIVE 5 MA LOADS.
AN ON BOARD DC-DC CONVERTER PROVIDES THE +/- 15 VDC
NECESSARY FOR THE ANALOG CIRCUITRY. CODING FOR THE
CONVERTERS (JUMPER SELECTABLE) ARE EITHER OFFSET BINARY
OR TWO'S COMPLEMENT.

B) A DOUBLE BUFFERING SCHEME ALLOWS SYNCHRONIZATION OF
OUTPUT DATA TO THE D/A CONVERTERS WITH EITHER AN
INTERNAL OR EXTERNAL CLOCK. THE FIRST BUFFER IS LOADED
BY A DDC INSTRUCTION FOR PROGRAMMED I/O (PIO) OR
/DCHO/ FOR DATA CHANNEL (DCH) CONVERSIONS. AT THIS
POINT, BOTH THE DAC DATA READY STATUS BIT
(READABLE BY A DIA INSTRUCTION) AND OUTPUT SIGNAL
(JUMPER SELECTABLE ACTIVE HIGH OR LOW) BECOME ACTIVE.
THEY REMAIN ACTIVE UNTIL A CLOCK SIGNAL OCCURS TO
LOAD THE SECOND BUFFER WHICH SENDS THE DATA TO
ONE OF THE DACS FOR CONVERSION TO ITS EQUIVALENT
ANALOG VOLTAGE OUTPUT. APPROXIMATELY 7 US LATER,
AFTER THE DAC HAS SETTLED TO ITS NEW VALUE, THE DAC
DATA VALID OUTPUT SIGNAL BECOMES ACTIVE (ALSO JUMPER
SELECTABLE ACTIVE HIGH OR LOW) AND REMAINS ACTIVE
UNTIL THE NEXT CONVERSION IS STARTED.

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C) THERE ARE SEVEN DIFFERENT CLOCK SOURCES FOR SENDING
DATA TO THE DACS. FOR PROGRAMMED I/O (PIO) THEY ARE:
/STRT/, NO CLOCK SYNCHRONIZATION, INTERNAL CLOCK
SYNCHRONIZATION, EXTERNAL CLOCK SYNCHRONIZATION.
FOR DATA CHANNEL (DCH) TRANSFERS THEY ARE: /IOPLS/
(ONE CONVERSION FOR EVERY /IOPLS/ ISSUED TO THE D/A),
DATA READY (OCCURS ONE FSTROBE AFTER /DCHO/ AND
REPRESENTS THE MAXIMUM TRANSFER RATE), INTERNAL
CLOCK SYNCHRONIZATION, EXTERNAL SYNCHRONIZATION.
FOR /IOPLS/ DCH TRANSFERS, THE TIME BETWEEN
SUBSEQUENT IOPLS'S SHOULD BE GREATER THAN THE
MAXIMUM DATA CHANNEL LATENCY. ALSO, AN I/O
INSTRUCTION WITH AN IOPLS APPENDED (I.E. NIOP)
SHOULD NOT BE GIVEN TO THE D/A UNTIL DATA READY
IS ACTIVE (DATA LOADED INTO FIRST BUFFER). THIS
CAN BE CHECKED BY READING THE D/A STATUS (DIA).

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D) IF AN EXTERNAL CLOCK IS USED, THE CLOCK SIGNAL MUST BE HIGH FOR AT LEAST 2 US AND LOW FOR AT LEAST 2 US AND HAVE A PERIOD GREATER THAN THE SETTLING TIME OF THE DACS (7 US TYPICAL). AND FOR DATA CHANNEL TRANSFERS, HAVE A PERIOD GREATER THAN THE MAXIMUM DATA CHANNEL LATENCY.

E) THE CLOCK SOURCE IS SELECTED BY THREE STATUS BITS IN A DOA INSTRUCTION. THE DOA INSTRUCTION ALSO CONTAINS AN ALTERNATE BIT, WHICH IS SET TO INDICATE ALTERNATING CONVERSIONS BETWEEN THE TWO DACS, A DAC SELECT BIT TO SELECT WHICH DAC RECEIVES THE FIRST DATA AND FOUR SELECTABLE SCOPE FUNCTION BITS. THEY ARE /SCOPE MODE/, /NON-STORE/, /WRITE-THROUGH/ AND /ERASE/. THE ERASE STATUS BIT CAUSES A PULSE OF DURATION APPROXIMATELY 2 MS ON THE /ERASE/ LINE (A13). LOW ACTIVE OPEN COLLECTOR SIGNAL WHICH CAN BE USED TO ERASE A SCOPE. THE DOA COMMAND SHOULD NOT BE GIVEN IF BUSY IS SET AND MUST APPEAR FIRST BEFORE DOB AND DOC IN A DATA CHANNEL SETUP SEQUENCE. ALL STATUS BITS REMAIN THE SAME UNTIL THE NEXT DOA INSTRUCTION OR /IORST/, WHICH CLEARS ALL STATUS BITS. SYNCHRONIZATION TO A CLOCK OCCURS ON THE FALLING EDGE OF THE CLOCK.

F) WHEN POWER IS FIRST APPLIED TO THE DAC BOARD THE DIGITAL CODE FOR 0 VOLTS IS APPLIED TO EACH DAC UNTIL THE FIRST CONVERSION. /IORST/ AGAIN CAUSES 0 VOLTS TO BE OUTPUTTED FROM EACH DAC. OTHERWISE, THE VOLTAGE OUTPUT OF EACH DAC IS THAT OF THE LAST CONVERSION.

G) IF THE /SCOPE MODE/ IN A DOA INSTRUCTION (DA) IS 0 (ACTIVE LOW SIGNAL), A Z-AXIS PULSE WILL OCCUR EVERY TIME A NEW DIGITAL CODE IS SENT TO EITHER DAC X OR DAC Y (JUMPER SELECTABLE). THE Z PULSE, WHICH IS AN INTENSIFICATION PULSE, ACTUALLY OCCURS AFTER A 7 US DELAY TO ALLOW DAC SETTLING. THE Z PULSE MAY BE AC OR DC COUPLED (JUMPER SELECTABLE). THE DC LEVEL OF THE Z-AXIS SIGNAL SHOULD BE ADJUSTED BY THE POT PROVIDED SO THAT THE CRT OR OSCILLOSCOPE TRACE IS JUST BARELY BLANKED. THE Z PULSE CAN BE UP TO THREE 0.5 VOLT LEVELS ABOVE OR BELOW THIS DC LEVEL (UP-DOWN IS JUMPER SELECTABLE). THE AMPLITUDE OF THE Z PULSE CAN BE INCREASED TO THREE 2 VOLT LEVELS BY CHANGING THE 3.3K RESISTOR TO 680 OHMS AND IS DETERMINED BY BITS 14 AND 15 OF THE DATA WORD WHICH CAUSES THE Z PULSE (NOTE THAT BITS 0-11 CONTAIN D/A DATA). THE FOLLOWING CODES DETERMINE THE BRIGHTNESS:

D14	D15	BRIGHTNESS LEVEL
0	0	1.5 VOLTS +/- DC LEVEL
0	1	1.0 VOLTS +/- DC LEVEL
1	0	0.5 VOLTS +/- DC LEVEL
1	1	NO CHANGE IN DC LEVEL DURING Z PULSE

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H) ALL PROGRAMMED I/O DIGITAL-TO-ANALOG CONVERSIONS SHOULD NORMALLY BEGIN WITH A DOCS INSTRUCTION. THE DOCS INSTRUCTION WILL LOAD THE FIRST BUFFER WITH DATA. PIO CONVERSIONS THAT ARE SYNCHRONIZED TO AN INTERNAL OR EXTERNAL CLOCK WILL OCCUR WITHOUT THE START COMMAND, ON THE FIRST FALLING EDGE OF THE CLOCK PULSE AFTER THE DOCS COMMAND HAS BEEN ISSUED. HENCE, IF IT IS DESIRED TO DO PROGRAMMED, SYNCHRONIZED CONVERSIONS WITHOUT SETTING DONE, THE DOCS COMMAND ALONE MAY BE GIVEN. FOR NON-SYNCHRONIZED PROGRAMMED I/O CONVERSIONS, THE I/O START COMMAND MUST BE GIVEN TO SEND THE DATA FROM THE FIRST BUFFER TO THE SECOND BUFFER AND OUT TO THE DACS FOR CONVERSION.

I) FOR DATA CHANNEL TRANSFERS, THE I/O START COMMAND CAUSES THE FIRST DATA CHANNEL TRANSFER TO THE FIRST BUFFER. SUBSEQUENTLY, THE CLOCK SOURCE SELECTED BY THE DOA INSTRUCTION OUTPUTS THE DATA TO THE APPROPRIATE DAC AND REQUESTS ANOTHER DATA CHANNEL TRANSFER.

J) THE EVENT WHICH CAUSES DONE TO BE SET VARIES, DEPENDING ON THE MODE IN WHICH INTERFACE IS BEING USED. FOR UNSYNCHRONIZED CONVERSIONS IN WHICH THE SCOPE MODE IS NOT BEING USED (NO Z-AXIS PULSES TRIGGERED AFTER THE CONVERSION), THE DOCS COMMAND TO START A CONVERSION WILL, OF COURSE, SET BUSY BUT DONE WILL NEVER BE SET IN THIS MODE BECAUSE OF THE FAST SPEED OF THE CONVERSION (BUSY WILL REMAIN SET). BEFORE NEW STATUS BITS ARE SELECTED (VIA A DOA INSTRUCTION), BUSY SHOULD BE CLEARED (VIA AN I/O CLEAR). DONE IS SET AS FOLLOWS:

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01 01 10007 MNDAAE          ? 10008 MNDAAE
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04 04 10007 MNDAAE          ? 10008 MNDAAE
05 05 10007 MNDAAE          ? 10008 MNDAAE
06 06 10007 MNDAAE          ? 10008 MNDAAE
07 07 10007 MNDAAE          ? 10008 MNDAAE
08 08 10007 MNDAAE          ? 10008 MNDAAE
09 09 10007 MNDAAE          ? 10008 MNDAAE
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41 41 10007 MNDAAE          ? 10008 MNDAAE
42 42 10007 MNDAAE          ? 10008 MNDAAE
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49 49 10007 MNDAAE          ? 10008 MNDAAE
50 50 10007 MNDAAE          ? 10008 MNDAAE
51 51 10007 MNDAAE          ? 10008 MNDAAE

DOA INSTRUCTION STATUS BITS
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MODE      CLOCK SYNC  /SCOPE
DCH      --  --  /MODE
D0      01  D4  --
D1      00  --  --
D2      00  --  --
D3      00  --  --
D4      00  --  --
D5      00  --  --
D6      00  --  --
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DONE SETTING SOURCE
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END OF Z PULSE
END OF Z PULSE
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END OF Z PULSE
2ND BUFFER CLOCK PULSE
(FALLING EDGE OF
EXTERNAL/INTERNAL CLK
INDICATES DATA SENT
TO DAC)
END OF Z PULSE AFTER
/WCEZ/ (NOTE: LAST
DATA CHANNEL WORD MUST
CAUSE Z PULSE OR ELSE
DONE WILL NOT SET)
2ND BUFFER CLOCK PULSE
AFTER /WCEZ/(SYNCHRONIZED
TO FALLING EDGE OF
/IOPLS/ OR /DATA READY/
-- INDICATES LAST DATA
IN DCH TRANSFER HAS
BEEN SENT TO DAC
END OF Z PULSE AFTER
/WCEZ/ (SEE NOTE ABOVE)
2ND BUFFER CLOCK PULSE
AFTER /WCEZ/. SYNCHRO-
NIZED TO FALLING EDGE
OF INTERNAL/EXTERNAL
CLOCK - INDICATES LAST
DATA IN DCH TRANSFER HAS
BEEN SENT TO DAC

NOTE - IN THE DATA CHANNEL MODES ABOVE, DONE MAY
ALSO BE SET BY THE LATE CONVERSION SIGNAL, IF THE
APPROPRIATE JUMPER CONNECTION IS MADE.

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K) IF THE PERIOD OF THE SYNCHRONIZING CLOCK IN DATA
CHANNEL MODE IS LESS THAN THE DATA CHANNEL LATENCY
TIME, DATA WILL NOT BE LOST, BUT IT WILL NOT APPEAR
AT THE DAC AT THE CORRECT SYNCHRONIZING CLOCK EDGE.
RAATHER, IT WILL APPEAR AT THE APPROPRIATE DAC AT THE
TIME OF THE FIRST TRAILING EDGE OF THE CLOCK AFTER
THE FIRST BUFFER HAS BEEN LOADED WITH NEW DATA. THE
DATA APPEARING AT THE DACS IS LATE FOR SYN-
CHRONIZATION, HOWEVER, AND THE LATE CONVERSION SIGNAL
IS SET. THIS SIGNAL MAY BE READ IN AS A STATUS
BIT BY A DIA INSTRUCTION AND MAY, BY
SETTING A JUMPER, SET DONE. THE LATE CONVERSION
SIGNAL IS CLEARED BY AN I/O CLEAR OR DOA INSTRUCTION.

L) IF THIS INTERFACE IS BEING USED TO DISPLAY ON A SCOPE
AN ARRAY OF POINTS LOCATED IN MEMORY, DATA CHANNEL
MODE SHOULD BE USED WITH THE ALTERNATE BIT SET. THE
/SCOPE MODE/ BIT RESET (THIS IS AN ACTIVE-LOW SIGNAL)
AND DATA ARRIVED IN MEMORY YXYYXY...OR YXYYXY...
IN THE FORMER CASE, DAC X IS SELECTED AS THE FIRST
DAC TO RECEIVE DATA AND THE SCOPE CIRCUITRY IS JUMPED
SO THAT A Z PULSE OCCURS AFTER CLOCK Y, AND THE
BRIGHTNESS CIRCUIT IS JUMPED FOR BRITYMSB AND
YXYYXY... OR YXYYXY... ORIENTATION, SET UP
IS REVERSED. THE Z DELAY (7 US) + THE Z PULSE
WIDTH MAY NOT EXCEED THE CLOCK PERIOD. HENCE,
THE Z INTENSIFICATION PULSE IS DONE BEFORE ANY DAC IS
UPDATED WITH NEW DATA.

M) AN EXTERNAL INTERRUPT MAY BE REQUESTED BY PULLING THE
/EXTERNAL INTERRUPT/ LINE LOW WHICH WILL REQUEST AN
INTERRUPT WITHOUT SETTING DONE. THE EXTERNAL
INTERRUPT REQUEST IS CLEARED BY AN I/O CLEAR OR DOA
INSTRUCTION.

N) A DIA INSTRUCTION INPUTS FOUR STATUS BITS TO THE CPU:
AN EXTERNAL ERASE INPUT BIT WHICH IS SET BY PULLING
THE /EXTERNAL ERASE INPUT/ LINE LOW; A DATA READY BIT
TO INDICATE THAT NEW DATA HAS BEEN LOADED INTO THE
FIRST BUFFER (USEFUL FOR THE IOPLS DATA CHANNEL MODE)
A LATE CONVERSION ERROR BIT; AND A BIT INDICATING
THE PRESENCE OF AN EXTERNAL INTERRUPT.

O) THE FOLLOWING ARE THE NOMINAL RANGES (PERIODS) FOR
THE INTERNAL CLOCK AND THE ZPULSE (ADJUSTABLE BY
POTENTIOMETERS ON THE DOA BOARD):

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WHAT      MIN      MAX      POT.
----      - - -      - - -
INTERNAL CLOCK  16 US  190 US  R43
ZPULSE         4 US  150 US  R32

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2) PROGRAM OPERATION:
THE PURPOSE OF THIS EXERCISOR IS TO PROVIDE A CONTINUOUS STREAM OF "KNOWN" DATA IN ORDER TO ASSURE PROPER OUTPUT FROM THE D/A AND A MEANS OF SCOPING THE PROBLEM SHOULD THERE BE ONE. THE THIRTEEN TESTS WERE DESIGNED TO EXERCISE THE FOLLOWING:

- 1 - PULSE AMPLITUDE
- 2 - PULSE WIDTH
- 3 - SWITCH DUMP
- 4 - STAIRCASE
- 5 - INTENSITY ("Z"-AXIS)
- 6 - SLEW RATE
- 7 - EXERCISE THE 3 SCOPE CONTROL BITS
- 8 - CALIBRATION

EACH TEST RUNS UNTIL STOPPED BY THE OPERATOR, SO AS TO PROVIDE A SYNC AND SCOPE LOOP.

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78. OPERATING MODES/SWITCH SETTINGS:
SWITCH PACK-N/A
STARTING ADDRESSES ARE 200 OR 500
9. OPERATING PROCEDURES/OPERATOR INPUT:
(NOTE: WHEN REMOVING AND/OR INSERTING PC BOARDS THE POWER SHOULD BE OFF IN THE SYSTEM)

TO RUN THIS DIAGNOSTIC:
1) THE D-A MUST BE IN THE SYSTEM WITH INTP AND DCHP PROPERLY CONNECTED.
2) CONNECT THE OUTPUT OF THE X CONVERTER TO CH 1 OF THE SCOPE.
3) CONNECT THE OUTPUT OF THE Y CONVERTER TO THE CH 2 SCOPE INPUT.
4) PLACE THE "0" SCOPE HORIZONTAL SWEEP RATE TO THE X-Y POSITION.
5) THE CH 2 VERTICAL CHANNEL IS TO BE SELECTED
6) TURN THE SYSTEM ON, LOAD THE PROGRAM, START AT LOC 200 (OR 500).
7) ANSWER THE FOLLOWING QUESTIONS:
A) DEVICE CODE OF D-A IS --. (ENTER THE SIX BIT DEVICE CODE OF THE D-A INTER-FACE IN OCTAL--MUST BE GREATER THAN 5 AND LESS THAN 77)
8) DOES THE Z PULSE COME FROM X (0) OR Y (1)
C) IS THE X-DAC JUMPED FOR OFFSET BINARY (0) OR TWO'S COMPLEMENT (1) ?
D) IS THE Y-DAC JUMPED FOR OFFSET BINARY (0) OR TWO'S COMPLEMENT (1) ?
(SEE TABLE 1 FOR FULL JUMPER INFO.)

8) AT THIS TIME A PROMPT (I) WILL BE ISSUED AND THE OPERATOR IS SETUP FOR TESTS 1, 2, AND 3. HE MAY START THE TESTS BY TYPING T"N" WHERE "N" IS 1, 2, OR 3. THE TEST WILL START AND DISPLAY A SQUARE OF FULL DEFLECTION (FROM BOTH DACS) ON THE FACE OF THE "0" SCOPE.

9) TEST 1 IS A BASIC SQUARE WAVE AS FOLLOWS:
START BY SETTING X AND Y TO THEIR MINIMUM VALUE (IF THE D-A'S ARE SET TO DIFFERENT VOLTAGE RANGES A RECTANGLE WILL OCCUR--STILL MEASURABLE ON THE CRT), X IS THEN INCREMENTED TO 77 (OCTAL) SHORT OF THE MAX (1.5K) WITH Y HELD @ 0. NEXT Y IS INCREMENTED THE SAME WAY W/X HELD AT IT'S LAST VALUE WITH Y AT 98.5% OF MAX X IS THEN DECREMENTED TO MINIMUM, FOLLOWED IN SIMILAR MANNER BY Y. (IN THE + OR - RANGE, 98.5% IS .3 VOLTS FROM MAX) IT GOES TO THE D-A IN THE DATA CHANNEL, DATA READY MODE (THE FASTEST); IT IS IN SCOPE MODE SENDING AN ERASE; ALTERNATING BETWEEN X + Y; W/X FIRST

10) TEST 2 IS LIKE TEST 1 WITH TWO EXCEPTIONS: THE SCOPE MODE IS WRITE TROUGH; AND THE "Z" AXIS (INTENSITY) IS STEPPED FOR EACH SIDE OF THE SQUARE (RECTANGLE)

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11) TEST 3 IS LIKE TEST 1 WITH TWO EXCEPTIONS :
IT IS OUTPUT TO THE D-A IN THE PROGRAMMED I/O
MODE WITH START SYNC FOR TRIGGERING; AND THE
SCOPE MODE IS NON-STORE.
(NOTE: TO OBSERVE THE SCOPE CONTROL BITS
(ERASE,WRITE THROUGH, NON-STORE, THE "Z" AXIS)
CALL THE TEST IT APPEARS IN(1-3). THEN SET THE
SCOPE AS FOLLOWS: HORIZ. SWEEP- 1 (OR 2) MS/CM
SYNC ON CH1; VERT. SELECT- CH2 (OR CHOP) AND
USE THE CH2 PROBE TO SEE THE BIT COMMING OFF
THE INTERFACE. ALL SIGNALS ARE DIGITAL
(EXCEPT "Z") SO 2V/CM ON THE VERT AMP WILL DO.
THE "Z" PULSE IS .5V - 1.5V PER STEP AS
DICTATED BY THE RESISTORS DESCRIBED
IN SECTION 7.1 PARAGRAPH G)

10012 MNDAAE

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12) THE OTHER TESTS (4-12) USE ONE OF TWO MODES:
1) THE SINGLE CHANNEL TESTS ARE DCH, DATA
READY; NO "Z" PULSE; NO ALTERNATE; OUTPUT
TO X (OR Y).
2) THE DUAL TRACE TESTS (6,11,12) USE DCH,
DATA READY; ALTERNATE W/X FIRST; NO "Z"
PULSE.
FOR TESTS 4-12 THE OPERATOR IS TO SET THE "0"
SCOPE HORIZONTAL SWEEP RATE AND VERTICAL CH
SELECTION AS FOLLOWS:

TEST	HORIZ. SWEEP RATE	VERT. SELECT
4	.5 MS/CM	CH1
5	.5 MS/CM	CH2
6	1 MS/CM	CHOP
7	.5 MS/CM	CH1
8	.5 MS/CM	CH2
9	.5 MS/CM	CH1
10	.5 MS/CM	CH2
11	1 MS/CM	CHOP
12	1 MS/CM	CHOP

13) TEST 4 IS A STAIRCASE OF 16 STEPS, MINIMUM TO
MAXIMUM SCALE FROM THE X CONVERTER.
14) TEST 5 IS THE SAME AS TEST 4 BUT FROM THE Y
CONVERTER.
15) TEST 6 IS TEST 4 & 5 TOGETHER FOR COMPARISON.
16) TEST 7 IS AN ADJUSTABLE SQUARE WAVE FROM THE X
CONVERTER.
17) TEST 8 IS WITH DEFAULT VALUE OF 3/4 SCALE.
18) TEST 9 IS AS TEST 7 FROM THE Y CONVERTER.
19) TEST 10 IS A MULTI-LEVEL, ADJUSTABLE SQUARE
WAVE FROM THE X CONVERTER WITH MINIMUM SCALE
AS REFERENCE WITH 1/4 AND 3/4 SCALE AS DEFAULT
FOR THE ADJUSTABLE VALUES.
20) TEST 11 IS TEST 9 WITH Y OUTPUTTING.
21) TEST 12 IS TESTS 9 & 10 TOGETHER.
TO GET A TEST STARTED, AGAIN TYPE T"N",
WHERE "N" IS 4,5,6,7,8,9,10,11, OR 12.

10013 MNDAAE

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21 ?
22 ?
23 ?
24 ?
25 ?
26 ?

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22) TO RUN THE TESTS IN SEQUENCE, THE OPERATOR NEED ONLY TYPE A "C" (CONTINUE) TO START THE NEXT TEST. (THIS WILL START TEST 1 IF THE PRESENT TEST IS 12 OR WHEN JUST STARTING UP)

23) IN TESTS 7-12 THE OPERATOR IS ASKED IF DEFAULT VALUES ARE TO BE USED. IF SO A CARRIAGE RETURN WILL START THE TEST, OTHERWISE TYPE A 1, CARRIAGE RETURN, AND NEW VALUE(S) WILL BE ASKED FOR. THE PROGRAM LEFT JUSTIFIES THESE QUERRIES IS 0-7777 (OCTAL). AS THE PROGRAM ISN'T CONCERNED ABOUT THE VOLTAGE RANGE OF THE D-A THE FOLLOWING CHART MAY BE USEFUL HERE. (THESE ARE ABSOLUTE VALUES AS THE PROGRAM CONVERTS TO BI-POLAR WHEN NECESSARY.)

D-A VOLT RANGE	0>5V	-5V>+5V*	0>10V	-10V>+10V*
7777:	+5V	+5V	+10V	+10V
7000:	+4.375V	+3.75V	+8.75V	+7.5V
6000:	+3.75V	+2.5V	+7.5V	+5V
5000:	+3.125V	+1.25V	+6.25V	+2.5V
4000:	+2.5V	0V	+5V	0V
3000:	+1.875V	-1.25V	+3.75V	-2.5V
2000:	+1.25V	-2.5V	+2.5V	-5V
1000:	+.625V	-3.75V	+1.25V	-7.5V
0000:	0V	-5V	0V	-10V

10014 MNDAAE

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21 ?

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24) THE PROGRAM HAS ONLY 3 ERROR REPORTS (AS THE D-A DIAGNOSTIC IS TO BE RUN FIRST) WHICH ARE: DONE NOT SETTING AFTER A REASONABLE TIME(TWO CASES); AND ALSO "LATE CONVERSION", IF ONE OF THESE ERRORS IS ENCOUNTERED THE TEST WILL CONTINUE TO LOOP BUT WILL ALSO PRINT OUT THE MESSAGE EACH TIME. IN ORDER TO AVOID THIS, THE OPERATOR MAY HIT AN "I" ON THE TTY (OR DISPLAY) TO INHIBIT THE REPORT.

25) THE TOTAL COMMAND SUMMARY IS:

T"N" - START TEST "N" (1-13) AND RUN UNTIL STOPPED
C - END THE CURRENT TEST AND START THE NEXT SEQUENTIAL ONE - UNLESS THE CURRENT TEST IS 12 - THEN START 1
ESC - (ESCAPE) STOPS THE PROGRAM AND EXITS TO THE PROMPT (1)
I - INHIBIT THE ERROR PRINTOUT
O - (AND TO)-EXIT TO THE OCTAL DEBUG TOOL.(OCT)
D - INHIBIT ALL .TXT MESSAGES
E - ENABLE ALL .TXT MESSAGES

10017 MNDAAE

```

01 OTHER COMMANDS TO OPEN CELLS ARE:
02
03 "ADR"/ OPEN THE CELL AND PRINT ITS CONTENTS
04 ./ OPEN THE CELL CURRENTLY POINTED TO BY THE POINTER
05 AND PRINT ITS CONTENTS.
06 +"ADR"/ ADD "ADR" TO THE POINTER, OPEN THE CELL AND PRINT
07 ITS CONTENTS.
08 *-ADR"/ SUBTRACT "ADR" FROM THE POINTER, OPEN
09 THE CELL AND PRINT ITS CONTENTS.
10 "CR" THE RETURN KEY IS USED TO CLOSE THE OPEN CELL
11 WITH OR WITHOUT MODIFICATION.
12 "LF" LINE FEED IS USED TO CLOSE THE OPEN CELL WITH OR
13 WITHOUT MODIFICATION AND TO OPEN THE SUCCEEDING
14 CELL.
15 * CLOSE THE OPEN CELL WITH OR WITHOUT MODIFICATION
16 AND OPEN THE PRECEDING CELL
17 / CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
18 OPEN THE CELL POINTED TO BY ITS CONTENTS.
19 +"ADR"/ CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
20 OPEN THE CELL POINTED TO BY ITS CONTENTS + "ADR".
21 -"ADR"/ CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
22 OPEN THE CELL POINTED TO BY ITS CONTENTS - "ADR".
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10018 MNDAAE

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:11.3.3 OTHER ODT COMMANDS
RUBOUT THIS KEY IS USED TO DELETE ERRONEOUSLY TYPED
DIGITS. EACH TIME THE KEY IS PRESSED THE RIGHT MOST
DIGIT IS DELETED AND ECHOED ON THE TERMINAL. IF
THE RUBOUT KEY IS PRESSED RIGHT AFTER OPENING A
CELL THEN IT DELETES THE RIGHT MOST DIGIT OF THE CELLS
CONTENTS. THIS ALLOWS THE MODIFICATION OF THE CELL
AS IF ITS CONTENTS WERE TYPED IN JUST BEFORE THE
KEY WAS PRESSED.
"ADR"B INSERT A BREAK POINT AT LOCATION "ADR".
ONLY ONE BREAK POINT CAN BE INSERTED AND ANY
ENTRY TO ODT AFTER EXECUTING A BREAK POINT WILL
CAUSE IT TO BE DELETED.
D DELETE THE BREAK POINT IF ANY.
P RESTART THE EXECUTION OF THE PROGRAM AT LOCATION
POINTED BY "A".
"ADR"R START EXECUTING THE PROGRAM AT "ADR" AFTER AN
IO-RESET.
K KILL THE STRING TYPED SO FAR. THE ODT RESPONDS
WITH A "2" AND THE OPEN CELL IS CLOSED WITHOUT
MODIFICATION.
= PRINT THE OCTAL VALUE OF THE INPUT ONLY.
THIS WILL CLOSE ANY OPEN CELLS WITHOUT
MODIFICATION AND WILL NOT OPEN A CELL

```

NOTE: IN PROGRAMS WHICH RELOCATE THEMSELVES THE USER SHOULD PLACE BREAK POINTS ONLY IN THE ORIGINAL PROGRAM AREA. IF A BREAK POINT IS PLACED OUTSIDE THIS AREA THE RESULTS WILL BE UNPREDICTABLE.

10019 MNDAAE

```

01 ? ;11-4 INSTRUCTION SET:
02 ? DOA: OUTPUT STATUS BITS TO THE INTERFACE, CLEARS
03 ? EXTERNAL INTERRUPT REQUEST AND LATE CONVERSION.
04 ? SHOULD NOT BE GIVEN IF BUSY IS SET AND MUST APPEAR
05 ? BEFORE DOB AND DOC IN DATA CHANNEL SETUP SEQUENCE.
06 ?
07 ? D0, D1, D2 ARE THE CLOCK SOURCE BITS FOR SENDING
08 ? DIGITAL DATA TO THE D/A CONVERTERS:
09 ?
10 ? D0 D1 D2 CLOCK SOURCE TO SEND DAC DATA
11 ? -- -- --
12 ? 0 0 0 /STRT/, NO SYNC
13 ? 0 0 1 NO CONVERSIONS
14 ? 0 1 0 INTERNAL CLOCK SYNC *
15 ? 0 1 1 EXTERNAL CLOCK SYNC *
16 ? 1 0 0 /IOPLS/ (1 DATA CONVERSION
17 ? FOR EVERY /IOPLS/ FOLLOWING
18 ? /STRT/, NO SYNC) **
19 ? 1 0 1 /DATA READY/ (OCCURS 1
20 ? /STRT/ AND 1 /IOPLS/ FOLLOWING)
21 ? 1 1 0 & IS MAXIMUM TRANSFER RATE)
22 ? 1 1 1 INTERNAL CLOCK SYNC
23 ?
24 ? * FIRST FALLING EDGE AFTER DOC COMMAND
25 ? ** DATA SHOULD BE READY IN THE FIRST BUFFER BEFORE
26 ? /IOPLS/ IS ISSUED
27 ?
28 ?
29 ? ;D3 ALTERNATE BIT 0 DO NOT ALTERNATE BETWEEN
30 ? DAC X AND DAC Y.
31 ?
32 ?
33 ?
34 ?
35 ?
36 ? ;D4 /SCOPE MODE/ BIT 0 Z-AXIS PULSES OUTPUTTED
37 ? 1 FOR NON-STORE, OC TRUE-LOW
38 ? OUTPUT (PINS A9 AND A10)
39 ?
40 ?
41 ?
42 ?
43 ? ;D5 /NON-STORE/ 1 FOR NON-STORE, OC TRUE-LOW
44 ? OUTPUT (PINS A9 AND A10)
45 ?
46 ? ;D6 /WRITE-THROUGH/ 1 FOR WRITE-THROUGH, OC TRUE-LOW
47 ? OUTPUT (PINS A11 AND A12)
48 ?
49 ? ;D7 /ERASE/ 1 FOR 2 MS PULSE TO SCOPE,
50 ? OC TRUE-LOW OUTPUT
51 ? (PINS A13 AND A14)
52 ?
53 ? ;D15 DAC SELECT BIT 0 SELECTS DAC X
54 ? 1 SELECTS DAC Y
55 ?
56 ? ; THE DEFAULT STATE OF ALL THESE STATUS BITS
57 ? UPON POWER-UP OR IORST IS 0.

```

10020 MNDAAE

```

01 ? ;DOB: OUTPUTS TO ADDRESS REGISTER FOR DATA CHANNEL
02 ? TRANSFERS.
03 ?
04 ? ;DOC: OUTPUTS TO WORD-COUNT REGISTER FOR DATA CHANNEL
05 ? TRANSFERS. IN PROGRAMMED I/O MODE (OO=0 IN
06 ? DOA INSTRUCTION) THIS INSTRUCTION CAUSES THE
07 ? FIRST BUFFER TO BE LOADED WITH THE DATA IN
08 ? THE ACCUMULATOR BITS 0-11, 14 AND 15.
09 ? BITS 0-11 ARE THE D/A DATA, WITH BIT 0 THE MSB.
10 ? BITS 14 AND 15 CONTAIN BRIGHTNESS INFORMATION
11 ? FOR Z-AXIS PULSES. A CLOCK SIGNAL AS SELECTED BY
12 ? THE DOA INSTRUCTION THEN OUTPUTS THE DATA TO THE
13 ? SECOND BUFFER AND THE APPROPRIATE DAC.
14 ?
15 ? ;D1A: INPUTS STATUS BITS FROM THE INTERFACE
16 ?
17 ? ;D0 1 IF EXTERNAL INTERRUPT REQUEST HAS OCCURRED,
18 ? 0 OTHERWISE
19 ? ;D1 1 IF DATA READY=1, 0 OTHERWISE. THIS INDICATES
20 ? THE PRESENCE OF DIGITAL DATA IN THE FIRST BUFFER.
21 ?
22 ? ;D8 1 IF LATE CONVERSION=1, 0 OTHERWISE. THIS INDICATES
23 ? A LOSS OF SYNCHRONIZATION WITH THE INTERNAL OR
24 ? EXTERNAL CLOCK IN DATA CHANNEL MODE.
25 ?
26 ? ;D15 1 IF /EXTERNAL ERASE INPUT/ LINE IS PULLED LOW,
27 ? 0 OTHERWISE.
28 ?
29 ? ;D18: INPUTS CURRENT DATA CHANNEL ADDRESS REGISTER
30 ?
31 ? ;DIC: NOT USED

```

10021 MNDAAE

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5) MACROS USED (3)

- 1) "OUTP" - DOES A CARRIAGE RETURN LINE FEED, OUTPUTS .TXT MESSAGE FROM LOCATION USED AS A MACRO CALL ARGUMENT (I.E. OUTP PROMT OUTPUTS THE TEXT FROM LOCATION "PROMT") THEN FOLLOWS UP W/2ND C.R. + L.F.
- 2) "OCTIN" INPUTS OCTAL DIGITS + ERROR RETURNS (KEY OTHER THAN 0-7 WAS HIT) TO THE MACRO CALL ARGUMENT. (I.E. OCTIN F13Z GETS OCTAL DIGITS UNTIL A C.R. OR IF AN ILLEGAL CHAR WAS HIT IT WILL GO TO F13Z)
- 3) "ADJS" SHIFTS A BINARY NO IN AC1 FOUR PLACES TO THE LEFT THEN STORES AC1 TO THE LOCATION SPECIFIED BY THE MACRO CALL ARGUMENT (I.E. ADJS X1 TAKES THE NO IN AC1, SHIFTS IT FOUR PLACES TO THE LEFT AND STORES IT IN LOC "X1")

10022 MNDAAE

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6. SUBROUTINES

- 1) INPUT - CHECKS THE ASCII CLEAR TO DETERMINE IF IT WAS A COMMAND - EXITS TO COMMAND INTERPRETER OR WHERE IT CAME FROM
- 2) INUMR - A "I" COMMAND GETS YOU HERE - IT THEN INPUTS THE TEST NO) - CHECK FOR <14 THEN GOES TO APPROPRIATE TEST OR TO THE PROMPT IF IN >14.
- 3) STROB - GETS D-A COMMAND WORD (CALLED DOAWD) AND SENDS IT TO THE D-A, GETS THE DATA CHANNEL STARTING ADDR) AND SENDS IT TO THE D-A, GETS THE NEGATIVE WORD COUNT AND SENDS IT TO THE D-A, STARTS THE D-A DCH CYCLE, TIMES IT, AND LOOPS.
- 4) NEWV1 - GETS OPERATOR VALUE TO USE AS X1. (ALL SINGLE CHANNEL TESTS USE "X1" OTHERWISE IT IS THE X CONVERTER VALUE)
- 5) SLOOP - JUST HELPS TO BUTLD THE DCH BUFFER
- 6) NEW2V - USED IN TEST 9 + 10 TO GET THE TWO VALUES FOR THE MULTI-LEVEL SQUARE WAVE. USES "X2" + "X1"
- 7) TOVAL - USED TO GET X1 + Y1 FOR THE TWO CHANNEL SQUARE WAVE OF TEST 11
- 8) GET4 - USED FOR GETTING X1*2 + Y1*2 FOR THE DUAL TRACE, MULTI-LEVEL SQUARE WAVE OF TEST 12.
- 9) S.TRCS - MAKES THE PATTERN IN THE DCH BUFFER THAT FORMS THE 16 STEP BY 16 WORD STAIRCASE OF TESTS 4,5,+6 (TEST 6 MAKES IT 16 STEPS X 32 WORDS PER STEP TO ALTERNATE X OR Y TO HAVE 16 X 16 EACH)
- 10) S.GUAR - MAKES THE 64 DOT X 64 DOT SQUARE FOR TESTS 1,2,+3
- 11) Z.MODE - USED BY TEST 3 TO SET EACH SIDE OF THE SQUARE (DIVIDES BUFFER INTO QUARTERS) INCREMENTS THE INTENSITY (WHICH PUTS OUT 1 OF 4 AT ANY ONE TIME).
- 12) T.TIME - A PLACE TO WAIT FOR THE DCH TO FINISH- SHOULD FINISH IN 10 MS BUT DELAY ALLOWS ABOUT 30 MS - ALSO CHECK FOR THE TTL. AFTER DCH FINISHES + SETS DONE THE STATUS IS CHECKED FOR A LATE CONVERSION.
- 13) P.OLET - CHECK THE CONVERSION MODE OF EACH OF THE D-A'S AND DOCTORS THE DATA BUFFER ACCORDINGLY.

10024 MNDAAE

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TABLE 1 - JUMPER SELECTION

W1-W10: VOLTAGE RANGE SELECT DACY
 RANGE DACX W7,W9
 +-10V W2,W4 W7,W10
 +-5V W3,W5 W6,W8,W10
 5V W1,W3,W5 W6,W10
 10V

W11-W14: OFFSET BINARY OR 2'S COMPLIMENT (ONE OR THE OTHER MUST EXIST) X-DAC Y-DAC
 W11 W13
 W12 W14

W15-W20: DEVICE CODE SELECT

W21-W22: SELECT Z AXIS FROM DACX OR DACY
 W21 - DACY
 W22 - DACX

A JUMPER IN IS EQUAL TO A "ONE" ON THE DATA (D) BUSS. THEY ARE READ AS FOLLOWS:
 D10 - W19
 D11 - W20
 D12 - W15
 D13 - W16
 D14 - W17
 D15 - W18

10023 MNDAAE

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12. SPECIAL NOTES/FEATURES

1. CALIBRATION IS ACCOMPLISHED WITH THE USE OF TEST 13 AND A FOUR AND A HALF (OR FULL SIX) DIGIT DMM (DVM). TO CALIBRATE THE D-A DO THE FOLLOWING:

- 1 - CONNECT THE DESIRED JUMPERS FOR POLARITY AND RANGE (W1-W14)
- 2 - LET THE D-A WARM-UP (ABOUT 30 MIN)
- 3 - CONNECT THE DVM TO THE OUTPUT OF THE X CONVERTER AND ITS RETURN
- 4 - CALL TEST 13 AND ENTER 0000 FOR BOTH CONVERTERS R2
- 5 - ADJUST OFFSET POT R2 UNTIL THE OUTPUT VOLTAGE IS EXACTLY -FSR/2* FOR BI-POLAR OR 0 FOR UNI-POLAR.

*NOTE: FSR=FULL SCALE RANGE (I.E. + OR - 10V FSR=20V SO THAT -FSR/2=-10V)

- 6 - CONNECT TO THE OUTPUT OF THE Y CONVERTER AND ITS RETURN AND ADJUST R8 AS IN STEP 5 WITH DVM STILL ON THE Y CONVERTER RE-CALL TEST 13 AND ENTER 7777 FOR X AND Y VALUES.
- 8 - ADJUST R7 FOR EXACTLY +FSR/2-1LSB IF BI-POLAR OR FSR-1LSB FOR UNI-POLAR (SEE TABLE TWO FOR EXACT VALUES)

CONNECT DVM TO THE X CONVERTER AND ITS RETURN AND ADJUST R1 IN STEP 8

- 9 - REPEAT ALL PROCEDURES TO COMPENSATE FOR POSSIBILITY OF GAIN ADJUSTMENT UPSETTING THE OFFSET ADJUSTMENT.

13. RUN TIME
 N/A

10025 MNDAAE

```

01 ; W23-W26:
02 ; SELECTS INTENSITY LEVEL ORIGIN OF Z AXIS
03 ;
04 ; W23 + W24 SELECT BITS 14 AND 15 OF DAC X WORD
05 ; W25 + W26 SELECT BITS 14 AND 15 OF DAC Y WORD
06 ;
07 ; NOTE: NORMALLY W21 GOES W/W25+W26;
08 ; W22 GOES W/W23+W24 IF W23-W26
09 ; ARE NOT IN, THE Z AXIS WILL BE
10 ; AT MAXIMUM INTENSITY.
11 ; W27:
12 ; SELECTS POLARITY OF Z AXIS
13 ; W27 IN == POSITIVE
14 ; W27 OUT == NEGATIVE
15 ;
16 ; W28+W29:
17 ; SELECT DATA VALID HIGH OR LOW TRUE
18 ; W28 == HIGH TRUE
19 ; W29 == LOW TRUE
20 ;
21 ; W30-W31:
22 ; SELECTS DATA READY HIGH OR LOW TRUE
23 ; W30 == HIGH TRUE
24 ; W31 == LOW TRUE
25 ;
26 ; W32:
27 ; (SELECT DONE ON A LATE CONVERSION)
28 ; W32 IN == SET DONE ON LATE CONVERSION.
29 ; W32 OUT == DO NOT SET DONE ON A LATE CONVERSION

```

10026 MNDAAE

```

01 ;
02 ;
03 ; + AND == FSR RANGES (BI-P. = BI-POLAR)
04 ; (FOR DVM'S WITH LESS THAN SIX DIGITS == ROUND OFF THE FOLLOWING)
05 ;
06 ; RANGE
07 ; MIN(0000) MAX(7777)
08 ; (-FSR/2 BI-P.) (+FSR/2-1LSB BI-P.)
09 ; +-10V +-9.99512V
10 ; 5V +-4.99756V
11 ; 10V 0.00000V +-9.99756V
12 ;
13 ; THE FOLLOWING ARE THE VOLTAGE GAINS FOR EACH
14 ; BINARY COUNT TO THE D-A CONVERTERS
15 ;
16 ; RANGE VOLTAGE (IN MILLI-VOLTS) FOR 1 COUNT
17 ; +-10V 4.6
18 ; +-5V 2.44
19 ; 5V 1.22
20 ; 10V 2.44
21 ;
22 ;
23 ;
24 ; *TITL MNDAAE

```

!0027 MNDAE
**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS