DATA GENERAL
CORPORATION
Southboro,
Massachusetts 01772
(617) 485-9100

PROGRAM

Memory Checkerboard II

TAPES

Binary: 095-000007

ABSTRACT

Memory Checkerboard II is a maintenance program designed to produce worst case noise conditions on the sense/inhibit wires. The program should be run to insure proper operation of sense amps, inhibit drivers, and memory currents.

097-000002-01

```
0001  .MAIN

                ;                       MEMORY CHECKERBOARD

                ;1.     ABSTRACT
                ;               CHECKERBOARD  IS A MAINTENCE PROGRAM DESIGNED
                ;               TO PRODUCE WORST CASE NOISE CONDITIONS ON THE
                ;               SENSE/INHIBIT WIRES. THE PROGRAM SHOULD BE RUN
                ;               TO INSURE PROPER OPERATION OF SENSE AMPS,INHIBIT
                ;               DRIVERS, AND MEMORY CURRENTS.


                ;2.     MACHINE REQUIREMENTS
                ;2.1            STANDRED NOVA PROCESSOR
                ;2.2            4K READ/WRITE MEMORY (SEE 4.6.2 FOR OTHER SIZES)


                ;3.     SWITCH SETTINGS
                ;3.1            STARTING ADDRESS        =000002
S               ;3.2            SWITCH 0(1)             =1024 READ/WRITE DISTURB
                ;3.3            SWITCH 15(1)            =INHIBIT HALT ON ERROR


                ;4.     OPERATING PROCEEDURE
                ;4.1            LOAD THE PROGRAM VIA THE BINARY LOADER
                ;4.2            SET SWITCHES TO 000002
                ;4.3            PRESS START
                ;4.4            IF THE FAILURES ARE MARGINAL, SETTING SWITCH
                ;               0 MAY AID IN INDUCING A FAILURE TO OCCURE.
                ;4.5            WHEN SCOPING OR ADJUSTING CURRENTS, SETTING
                ;               SWITCH 15 WILL INHIBIT THE ERROR HALT. THE
                ;               BELL WILL STILL BE RUNG.
                ;4.6            PROGRAM MODIFICATIONS
RESS            ;4.6.1                  C(3)=ADR        THE STARTING PATTERN ADD
ESS             ;4.6.2                  C(4)=FINAL      THE  ENDING PATTERN ADDR
                ;                                       BITS 10-15 MUST=77.
                ;4.6.3                  C(5)=INHIBIT    INHIBIT THE CHECKERBOARD
                ;                                       PATTERN ON CLEARED BITS.
```

```
A 0002  .MAIN

                15.     PROGRAM OUTPUT/ERROR DISCRIPTION
OT              15.1            AT EACH OCCURANCE OF ERROR, IF THE TELETYPE IS N
RO              !               BUSY THE BELL WILL BE RUNG. IF SWITCH (15) IS Z
                !               THE PROGRAM WILL HALT AT LOCATION "ER".
                15.2            WHEN A ERROR HALT OCCURES:
 UP             !                       C(CARRY)=1      IF BITS HAVE BEEN PICKED
                !                       C(CARRY)=0      IF BITS HAVE BEEN DROPED
                !                       C(1)=THE ERROR WORD
                !                       C(2)=THE ERROR ADDRESS
                15.3            SET SWITCH (15) IF  SCOPING,PRESS CONTINUE.
                15.4            SYNC PULSES
                !                       A "P" PULSE (A74) IN STORE CYCLE.
D.              !                       A "S" PULSE (A52) CHECK ONES PATTERN WOR
RD.             !                       A "C" PULSE (A50) CHECK ZEROS PATTERN WO

                16.     PROGRAM DISCRIPTION
                16.1            STORE THE CHECKERBOARD PATTERN
                16.2            IF SWITCH 0(1) DISTURB THE CONTENTS OF MEMORY BY
                !               REFFERANCING LOCATIONS 0101,0202,0303,ETC. 512
                !               TIMES. THIS PRODUCES 1024 READ/WRITE DISTURBS.
                16.3            CHECK THE PATTERN WORD
                16.4            COMPLEMENT AND CHECK THE WORD
                16.5            RESTORE THE WORD
                16.6            WHEN THE END OF THE PATTERN IS REACHED THE
                !               PROGRAM COMPLEMENTS THE PATTERN WORD AND RE-
                !               TURNS TO STEP 6.1 .

                17.     LIMITATIONS
                !               NONE
```

```
▲ 0003  .MAIN

        000002 .LOC 2
00002 000024           JMP BEGIN

00003 000157 ADR:      CEND+1          ;PATTERN STARTING ADDRESS
00004 007577 FINAL:    7577            ;PATTERN FINAL ADDRESS
00005 177777 INH:      -1              ;MASK FOR INHIBITED BITS
00006 000000 PATT:     0               ;PATTERN WORD
00007 000000 ERET:     0

00010 000017 C17:      17
00011 000400 C400:     400
00012 000077 C77:      77
00013 007777 C7777:    7777
00014 000207 C207:     207
00015 000101 C101:     101
00016 060200 CNIOC:    NIOC 0
00017 060100 CNIOS:    NIOS 0
00020 070000 C070000:          070000
00021 000000 MODUAL:   0
00022 000000 EDIST:    0

00023 063077           HALT            ;OPERATOR ERROR FIX C(ADR)
00024 034003 BEGIN:    LDA 3,ADR
00025 030020           LDA 2,C070000
00026 020004           LDA 0,FINAL
00027 143400           AND 2,0
00030 040022           STA 0,EDIST
00031 173400           AND 3,2
00032 050021           STA 2,MODUAL    ;THE MEMORY MODUAL
00033 024156           LDA 1,CEND
00034 136033           ADCZ# 1,3,SNC   ;STERT MUST BE <
00035 000023           JMP BEGIN-1     ;STOP OR ,OPERATOR GOOF

00036 034012 IPAT:     LDA 3,C77       ;INITIALIZE A PATTERN
00037 030003           LDA 2,ADR
00040 024011           LDA 1,C400
00041 020006           LDA 0,PATT      ;PRESET PATTERN
00042 147404           AND 2,1,SZR
00043 100000 IPAT1:    COM 0,0
00044 024005           LDA 1,INH
00045 123400           AND 1,0         ;MASK INHIBITED BITS
00046 024010           LDA 1,C17

00047 060300 FILL:     NIOP 0          ;SYNC AT A74
00050 041000           STA 0,0,2       ;FILL MEMORY WITH
00051 151400           INC 2,2         ;PATTERN
00052 133414           AND# 1,2,SZR    ;SKIP EVERY 16 TIMES
00053 000047           JMP FILL
00054 157414           AND# 2,3,SZR    ;SKIP EVERY 64 TIMES
00055 000043           JMP IPAT1
00056 020004           LDA 0,FINAL     ;TEST FOR FINAL ADDRESS
00057 142432           SUBZ# 2,0,SZC   ;EVERY 64 LOC, 4K
00060 000040           JMP IPAT+2      ;FILL TIME=100MS,
```

```
▲ 0004  .MAIN

00061 030021 DISTURB:        LDA 2,MODUAL    ;DISTURB MODULE SELECT
00062 020013          LDA 0,C7777      ;DISTURB AT LOCATION
00063 024022          LDA 1,EDIST      ;0101,0202,0303,ETC.
00064 123000          ADD 1,0
00065 024015          LDA 1,C101       ;EVERY OTHER CORE IN MEMORY
00066 133000          ADD 1,2          ;IS DISTURBED AT LEAST
00067 074477          READS 3          ;1024 TIMES+INHIBIT DISTURBS.
00070 175112          MOVL# 3,3,SZC    ;BUT ONLY IF SWITCH 0
00071 142433          SUBZ# 2,0,SNC    ;IS SET TO A ONE.
00072 000100          JMP ICHECK       ;END OF DISTURB
00073 176400          SUB 3,3
00074 025000          LDA 1,0,2        ;REFFERANCE MEMORY
00075 175704          INCS 3,3,SZR
00076 000074          JMP .-2
00077 000065          JMP DISTURB+4

00100 030003 ICHECK: LDA 2,ADR        ;INITIALIZE CHECK CYCLE
00101 024011          LDA 1,C400
00102 020006          LDA 0,PATT       ;X LINE INIT PATTERN
00103 133414          AND# 1,2,SZR
00104 100000 ICK:     COM 0,0
00105 034005          LDA 3,INH
00106 163400          AND 3,0          ;MASK INHIBITED BITS
00107 024017          LDA 1,CNIOS      ;"S" PULSE
00110 114044          COMO 0,3,SZR     ;"C" PULSE
00111 024016          LDA 1,CNIOC      ;ON I/O DISTURB SIGNELS
00112 044113          STA 1,CHECK

00113 000000 CHECK:  0                ;A SYNC PULSE ISSUED
00114 025000          LDA 1,0,2        ;SIGNELS RWVZ,RWV1
00115 106414          SUB# 0,1,SZR
00116 004142          JSR ERR1
00117 055000          STA 3,0,2
00120 025000          LDA 1,0,2
00121 136414          SUB# 1,3,SZR     ;SIGNELS UV1,UVZ
00122 004143          JSR ERR2
00123 041000          STA 0,0,2
00124 151400          INC 2,2
00125 024010          LDA 1,C17        ;COUNT 16 TIMES
00126 147414          AND# 2,1,SZR
00127 000113          JMP CHECK

00130 034012 ECHECK: LDA 3,C77
00131 157414          AND# 2,3,SZR     ;CHECK FOR END OF
00132 000104          JMP ICK          ;LINE
00133 024004          LDA 1,FINAL      ;EVERY 64 TIMES
00134 146432          SUBZ# 2,1,SZC    ;CHECK FOR END OF CORE
00135 000101          JMP ICHECK+1
00136 020006          LDA 0,PATT       ;COMP THE
00137 100000          COM 0,0          ;PATTERN
00140 040006          STA 0,PATT
00141 000024          JMP BEGIN
```

```
00142 101020 ERR1:   MOVZ 0,0          ;DISTURB ENTRY
00143 054007 ERR2:   STA 3,ERET        ;UNDISTURB ENTRY
00144 101005         MOV 0,0,SNR       ;C(CARRY)=1 FOR PICK BIT
00145 101060         MOVC 0,0          ;C(CARRY)=0 FOR DROP BIT
00146 034014         LDA 3,C207        ;C(1)=ERROR WORD
00147 063411         SKPBN TTO         ;C(2)=ERROR ADDRESS
00150 075111         DOAS 3,TTO        ;SET SWITCH 1 TO
00151 074477         READS 3           ;INHIBIT HALT
00152 175213         MOVR# 3,3,SNC     ;THE BELL WILL BE RUNG
00153 063077 ER:     HALT              ;IF TTY NOT BUSY
00154 114040         COMO 0,3          ;TURN OF TTY IF
00155 002007         JMP @ERET         ;TO NOISEY.
00156 000156 CEND:   .
                     .END
```