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Diablo Systems Incorporated
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HyTerm Communications Terminal
Model 1610/1620
Maintenance Manual

PREFACE

This manual contains only theory of operation (Section 2) and Maintenance (Section 3) information, and schematics and logic drawings (Section 4). Refer to the Product Description manual, no. 82332, for operating instructions, specifications, functional description, interface information and installation instructions.

This revision supercedes Revision B published in December 1976. Comments on this manual and its use are welcome. Please address comments to Diablo Systems, Inc., 24500 Industrial Boulevard, Hayward, California 94545.

Diablo Systems, Inc., reserves the right to make improvements to products without incurring any obligation to incorporate such improvements in units previously sold.

WARRANTY

The Diablo Model 1610 and Model 1620 HyTerm
Communications Terminals are warranted against defects in
materials and workmanship for 90 days from the date of
shipment. Any questions with respect to the warranty
should be directed to your Diablo sales representative.

All requests for repairs should be directed to the Diablo
repair depot in your area. This will assure you of the fastest
possible service.

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Figure 1-1. HyTerm Communications Terminal

SECTION 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The HyTerm communications terminal, Figure 1-1, transmits data to and receives data from a host computer or remote terminal over a communications link via an EIA standard RS-232 interface. In local operation, the Model 1620 can also serve as a document writer for correspondence and other secretarial functions.

The HyTerm consists of a Diablo HyType II printer with microprocessor-driven electronics and an integral power supply, all contained in an attractive table top unit. A full complement of optional features, including keyboard, forms tractor, pin-feed platen, carbon ribbon, interchangeable type fonts, etc., is available to adapt the HyTerm to virtually any communications situation.

1.2 SCOPE

This manual provides information on theory of operation, maintenance, and module/subassembly replacement. It also includes data covering the electronic components used and explanations of the logic symbology and drawing conventions used. It does not include operating instructions, installation procedures, or information on the functional operation of the HyTerm; these are all contained in the Product Description manual listed in the related documents.

1.3 RELATED DOCUMENTS

(1) HYTERM COMMUNICATIONS TERMINAL, PRODUCT DESCRIPTION. Diablo Systems, Inc. Publication No. 82332.

(2) SERIES 1300 HYTYPE II PRINTER PARTS CATALOG. Diablo Systems, Inc. Publication No. 82404.

(3) SERIES 1600 HYTERM TERMINAL PARTS CATALOG. Diablo Systems, Inc. Publication No. 82334.

(4) INTERFACE BETWEEN DATA TERMINAL EQUIPMENT AND DATA COMMUNICATION EQUIPMENT EMPLOYING SERIAL BINARY DATA INTERCHANGE. EIA Standard RS-232-C, August, 1969. Engineering Dept., Electronic Industries Assn., 201 Eye St. N.W., Washington, D.C. 20006.

(5) USA STANDARD CODE FOR INFORMATION INTERCHANGE, USAS X3.4-1977. American National Standards Institute, 1430 Broadway, New York, N.Y. 10018.

(6) DATA SET 103A INTERFACE SPECIFICATION, February, 1967, Engineering Director, Data Communications, American Telephone and Telegraph Co. Publication No. 41101.
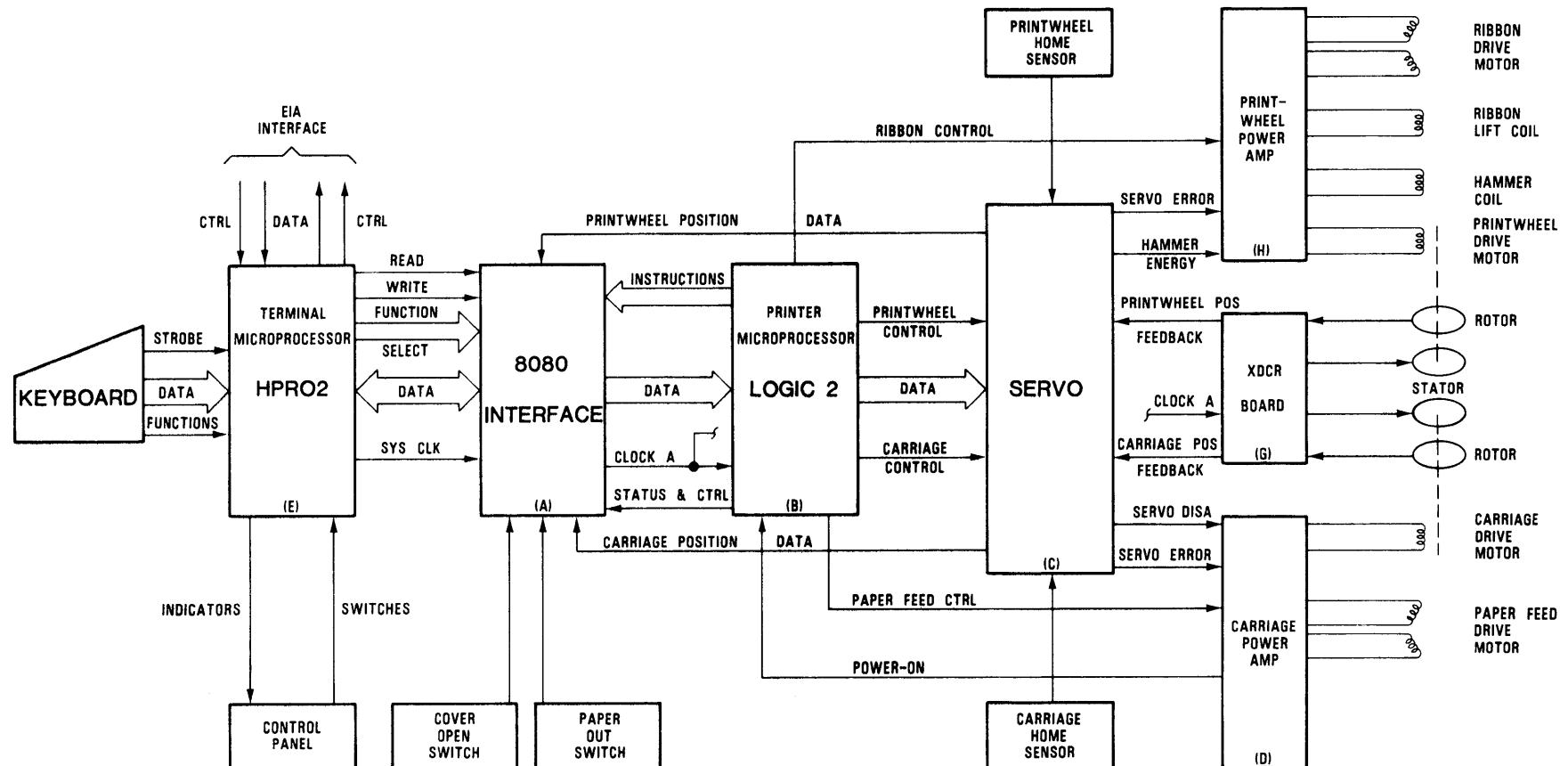
Figure 2-1. HyTerm Block Diagram

SECTION 2
THEORY OF OPERATION

2.1 INTRODUCTION (Figure 2-1)

The HyTerm employs two separate, asynchronous, processing systems. One, called the "printer microprocessor," is an integral part of all HyType II printers. The other, called the "terminal microprocessor," provides the additional functions that transform a HyType II printer into a communications terminal.

The terminal microprocessor, located on the HPRO board, slot E, controls the overall terminal functions of sending and receiving data over the EIA interface, receiving data from the keyboard, and monitoring the control panel. It also communicates with the printer microprocessor, contained on the LOGIC-2 board, slot B. This second microprocessor system initiates movement of the printer carriage, printwheel, paper, and ribbon, and monitors feedback from the carriage and printwheel circuits to effect proper execution of these motion commands. It also maintains a record of the printwheel's absolute position at all times, it provides printer status information to the terminal microprocessor, and it performs other "housekeeping" functions.

The 8080 INTERFACE board, slot A, is located logically between the two microprocessors. It provides temporary storage for data and status information, and synchronizes the transfer of data from the terminal microprocessor to the printer microprocessor, and the transfer of status information back. It also contains some control logic for the servo feedback system and provides the CLOCK A signal that drives the printer microprocessor.

The SERVO board, slot C, receives printwheel and carriage motion commands from the printer microprocessor in digital form and converts these to analog signals representative of the distance and direction to be moved. These servo "error" signals are passed on to the printwheel and carriage power amplifiers, which drive their respective servo motors. Feedback signals, derived from the printwheel and carriage rotary transducers, are amplified by the XDCR board, slot G, and passed through the SERVO board to the 8080 INTERFACE board. Here they are available to the printer microprocessor, which uses them to regulate the error signals. The SERVO board also converts digital hammer-energy signals into their analog counterparts.

The PRINTWHEEL POWER AMPLIFIER, slot H, provides drive for the printwheel servo motor, the ribbon step motor, and the hammer-fire and ribbon-lift magnet coils.

The CARRIAGE POWER AMPLIFIER, slot D, drives the carriage servo motor and the paper feed stop motor. It also monitors the input voltages and develops the POWER ON signal to initiate the Restore operation.

The optional HCURL board, slot F, serves as the interface beeween the terminal microprocessor and the current loop network.

2.2 HYTERM PROCESSOR (HPRO) BOARD (Figure 2-2), PART NOS. 23702 (HPRO1) AND 23704 (HPRO2)

Depending upon the optional features employed and other manufacturing procedures, either of two HPRO boards, HPRO1 or HPRO2, may be used. Although the two boards appear quite different physically, the only functional difference is in the ROM integrated circuits. Both boards contain most of the terminal microprocessor system, including the 8080 microprocessing unit (MPU), the memory, several Input/Output ports, and all control electronics. They also contain the Universal Synchronous/Asynchronous Receiver/Transmitter (USART) and the RS-232 interface components.

NOTE

Throughout this manual, two terms will be used extensively: *"terminal microprocessor"* refers mainly to the entire HPRO circuit board, whereas *MPU* refers to the 8080 integrated circuit.

2.2.1 General Operation

The terminal microprocessor is actually a miniature computer. It receives its instructions from Read Only Memory (ROM). These instructions are arranged to form a "microprogram." As it executes this microprogram, the MPU receives data from the various input ports and stores it in memory, or reads data out of memory and sends it to the various output ports. Between input and output instructions, the MPU may perform other operations on the data, make logical decisions concerning the data, or "jump" to a different portion of its program.

The main portion of the microprogram periodically scans the control panel switches, performs the output commands to the printer, control panel indicators, and the USART, and takes care of other "housekeeping" functions. When an input is received from either the communications link (via the USART) or the keyboard, the MPU is "interrupted," and it jumps out of the main program loop into an "interrupt subroutine." During this subroutine, the input character is received, decoded, and placed in the print buffer and/or the transmit buffer (in memory). Then the MPU returns to the same point in the main program at which it was interrupted, and continues processing. Thus, input characters are received via the interrupt subroutine, and output characters are sent via the main program loop.
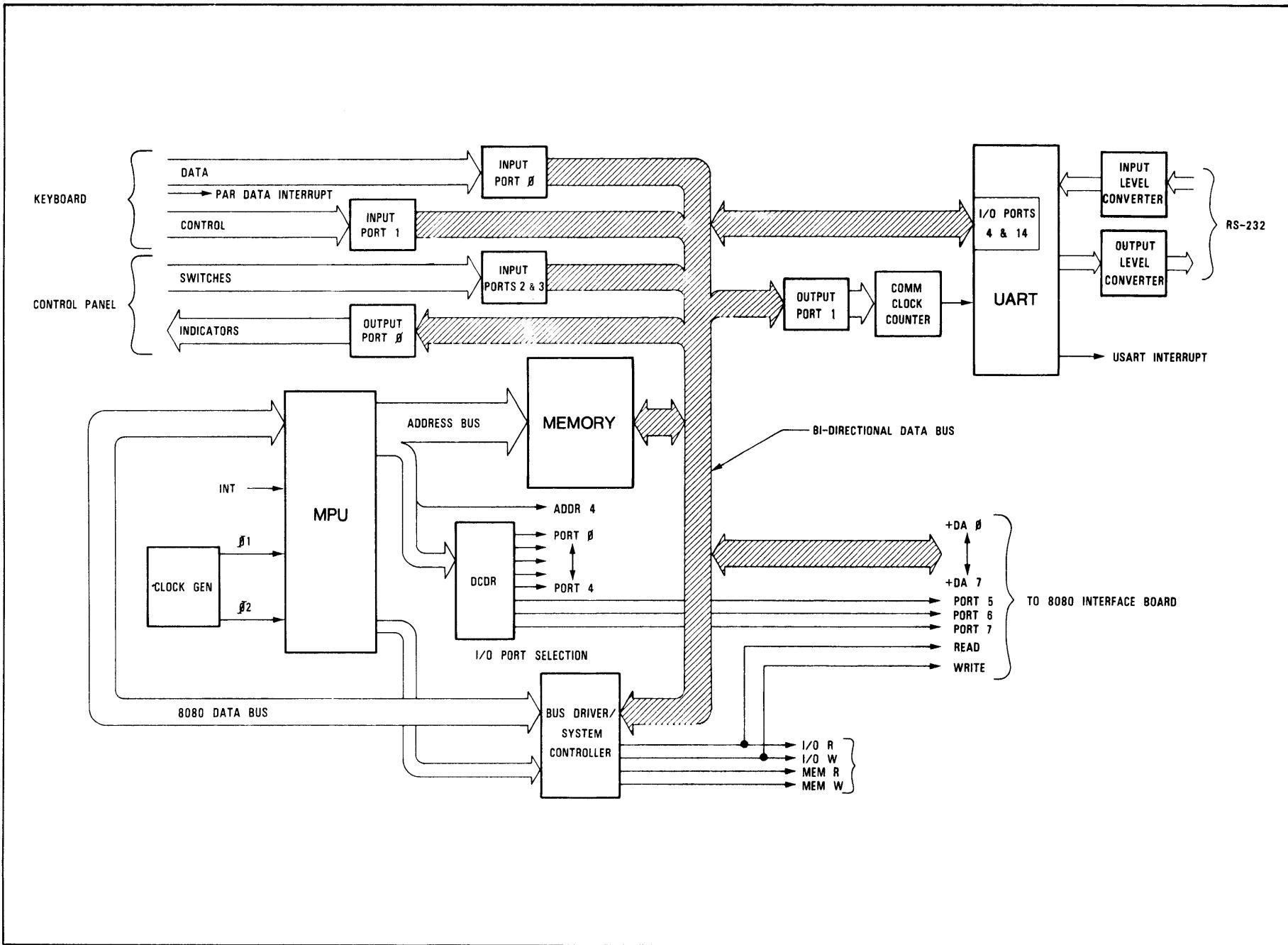
Figure 2-2. HPRO Board Block Diagram

2.2.2 8080 Microprocessing Unit (MPU)

The 8080 is an 8-bit microprocessor contained in a single 40-pin integrated circuit (IC) package. It has an 8-bit wide bi-directional data bus used for both input and output. It has a 16-bit address bus, capable of addressing up to 65,536 memory locations, although the HyTerm uses substantially less than this maximum. The MPU's instructions are located in memory, from where they are fetched and executed sequentially. There are over 100 separate instructions possible, although many are similar, the difference being only in the various MPU internal registers specified.

2.2.2.1 ARCHITECTURE

To understand the operation of the terminal microprocessor, it is only necessary to know that the MPU contains an instruction register, a program counter, a memory address register, a stack pointer, and other registers and logic elements. The instruction register contains the 8-bit instruction op code. The program counter contains the 16-bit memory address of the next instruction to be fetched. The memory address register is made up of two 8-bit registers, referred to as the H and L register pair. It is used to address memory for memory read and memory write instructions. Other internal MPU registers can also be used to address memory. The stack pointer is generally used to "remember" the address of the next sequential main program instruction while an interrupt subroutine is being executed. Still other elements internal to the MPU perform the arithmetic and logic operations and control the input and output over the data bus.

This is admittedly a very brief description of the MPU architecture, but this background should be sufficient to allow understanding of the material to follow. Further information on the MPU can be found in the integrated circuit information presented in Section 4.

2.2.2.2 TIMING

Timing is controlled by two 12V (nominal) non-overlapping clocks, $\emptyset1$ and $\emptyset2$. These clocks are provided at a frequency of 2 MHz by a Clock Generator IC.

2.2.2.3 BASIC PROCESSOR OPERATION

MPU operation is divided into time periods called "cycles" and "states." There are two types of cycles: instruction cycles and machine cycles. The material that follows is summarized in the timing chart in Figure 2-3.
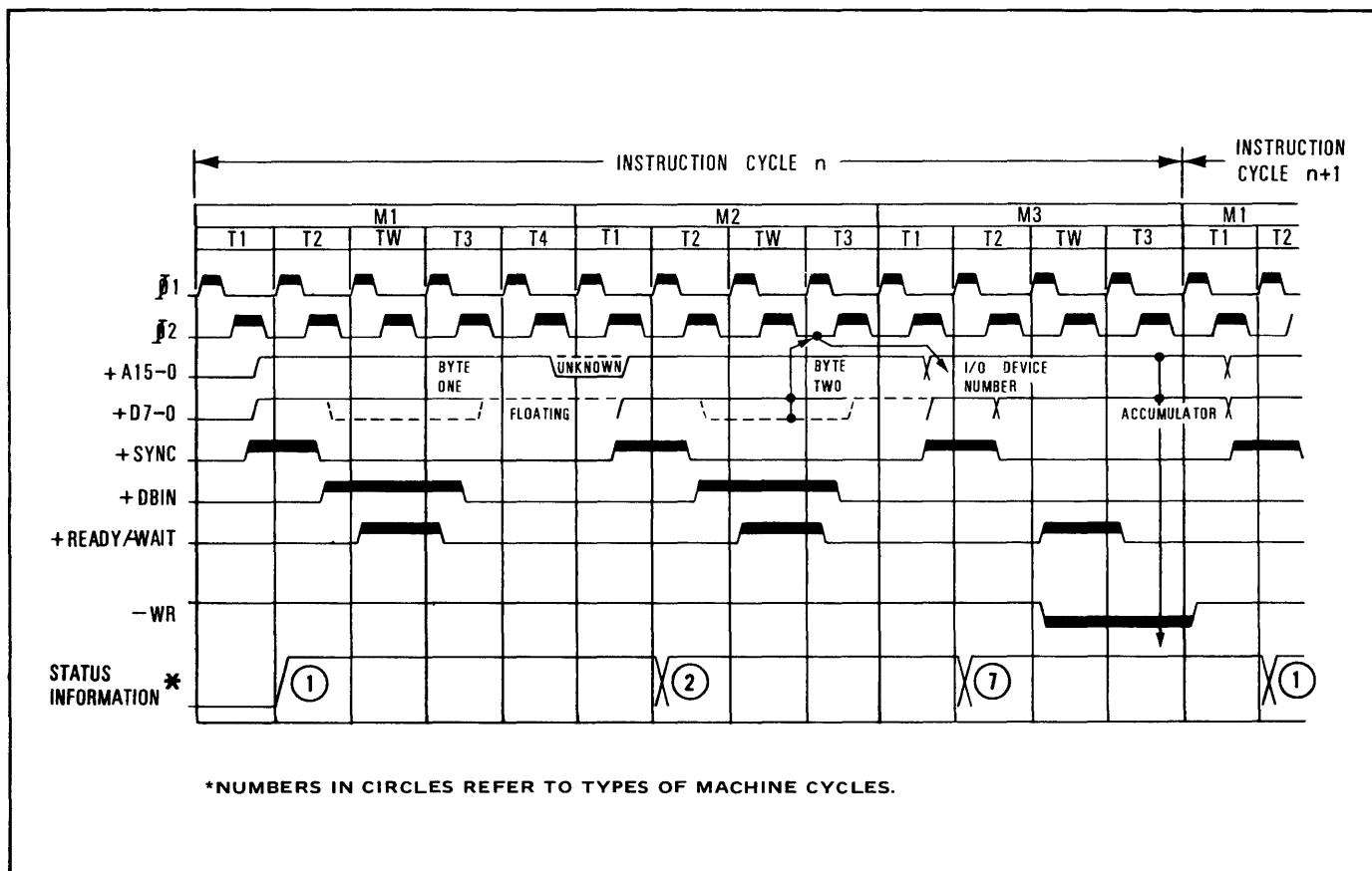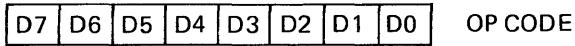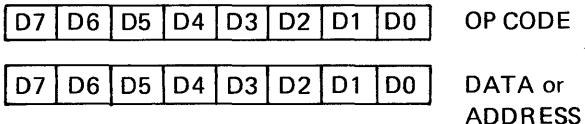
Figure 2-3. Typical Instruction Cycle (Output Instruction)

2.2.2.3.1 Instruction Cycle. An instruction cycle includes both the fetching of the instruction from memory and the execution of the instruction. Each instruction can be either one, two, or three 8-bit bytes in length. Multiple byte instructions must be stored in successive memory locations. Figure 2-4 illustrates the three instruction formats. The actual bit configuration of the op code is not important to the understanding of the terminal processor operation.

One Byte Instructions

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | OP CODE

Two Byte Instructions

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | OP CODE

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DATA or ADDRESS

Three Byte Instructions

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | OP CODE

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | } DATA or
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | } ADDRESS
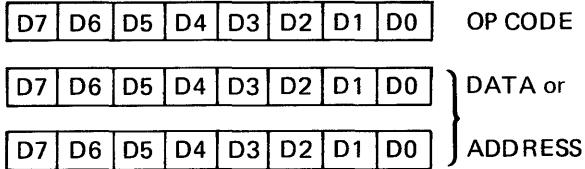
Figure 2-4. MPU Instruction Format

2.2.2.3.2 Machine Cycle. A machine cycle is required each time an I/O port or the memory is accessed. Each instruction cycle can contain from one to five machine cycles. There are ten different types of machine cycles possible, as follows:

(1) Instruction Fetch
(2) Memory Read
(3) Memory Write
(4) Stack Read
(5) Stack Write
(6) Input
(7) Output
(8) Interrupt Acknowledge
(9) Halt Acknowledge
(10) Interrupt Acknowledge While in Halt

The latter two do not occur in the HyTerm since the HALT instruction is not used in the microprogram.

2.2.2.3.3 States. A state is defined as the time interval (50 ns) from leading edge to leading edge of the $\phi1$ clock. There are six possible states, numbered T1 through T5 and TW (representing "wait"). TW follows T2. All machine cycles include T1, T2, TW, and T3. T4 and T5 are omitted during execution of instructions not requiring them.

2.2.2.3.3.1 T1. During T1 either a memory address or an I/O port address is placed onto the memory address bus. Also, the MPU places eight bits of status information on the data bus which identify the type of machine cycle being performed. Following the rising edge of $\phi2$, the SYNC signal is produced by the MPU, which identifies the beginning of a machine cycle. See Figure 2-3.

2.2.2.3.3.2 T2. During T2 the MPU monitors its RDY input. If it is high, the MPU goes on to state 3, if it is low, the MPU goes on to the Wait state. In the HyTerm, the WAIT output, which goes high during TW, is connected to the RDY input. This causes TW to always follow T2.

During the machine cycles that bring data into the MPU (Instruction Fetch, Memory Read, Stack Read, Input, and Interrupt Acknowledge), the Data Bus In signal, DBIN, is developed at $\phi2$ during T2. DBIN remains high through TW and into T3. This signal develops READ and MEMR at the proper time to provide the input data needed by the MPU. (This is covered more fully in Section 2.2.4.)

2.2.2.3.3.3 TW. The wait state provides the MPU delay required for proper memory access. No internal processing occurs during this state. The MPU monitors its RDY input, and if it is low, it remains in the Wait state; if it is high, the MPU goes on to state 3. In the HyTerm, the RDY input is always high during TW, so the MPU always goes on to T3 after one state time (500 ns) in TW.

During machine cycles in which the MPU outputs data (Memory Write, Stack Write, Output), it develops the WR (Write) signal during TW and holds it low until after the end of T3. This signal is used by other logic on the HPRO board to strobe the output data to memory or the selected output port.

2.2.2.3.3.4 T3. During T3 the data or instruction byte is actually transferred between the MPU and memory or an I/O port. The source and destination of the byte is determined by the type of machine cycle being performed. For example, during an instruction fetch cycle, the source of the data (instruction byte) is the memory location addressed during state 1; the destination is the MPU. During an Output machine cycle, the source is the MPU and the destination is the I/O port selected (addressed) in state 1.

2.2.2.3.3.5 T4 and T5. These two states are used only when required for manipulation of data with the MPU.

2.2.3 Clock Generator (8224)

The clock generator is contained in a single integrated circuit that provides several functions. First, it provides the two non-overlapping 12V signals, $\phi1$ and $\phi2$, required by the MPU. The frequency of these signals (2 MHz) is controlled by an external quartz crystal. A TTL equivalent of the $\phi2$ signal, $+\phi2T$, is also developed for use in timing other functions on the HPRO board.

2-4

Second, the 8224 converts the MPU's SYNC signal into the Status Strobe signal, STSTB. This signal is used to load the status information, put out by the MPU at the beginning of each machine cycle, into the Bus Driver/System Controller IC. This is covered more fully in section 2.2.4.

Third, the clock generator IC develops +CLEAR, which is used to reset and initialize the entire HPRO board. This occurs both at power-on and when the RESET switch is operated.

The 8224 has other capabilities not utilized by the terminal microprocessor.

2.2.4 Bus Driver/System Controller (8228)

This module is another single IC that performs three basic functions: bi-directional bus control, system logic control, and interrupt handling.

2.2.4.1 BUS CONTROL

The 8228 provides a buffer between the MPU and the memory and I/O ports. Controlling the two 8-bit data buses on the HPRO board is concerned with not only switching the data on and off in the proper direction at the right time, but also in providing the required voltage and current levels. Since the MPU is an MOS device, it requires a voltage of at least +3.3 volts for a "logic 1" or "true" indication on

its data inputs. The 8228 provides a minimum of +3.6 volts on the 8080 Data Bus, which is substantially higher than can be guaranteed by standard TTL devices. For output data, the MPU can provide only 1.9 mA of current drive. With many I/O ports and the memory connected to the bi-directional data bus, this value could easily be exceeded, so the 8228 is used to provide over 10 mA to satisfy this requirement. The direction of data flow on the buses is controlled internally by the same signals that furnish the system control function performed by this IC.

2.2.4.2 SYSTEM LOGIC CONTROL

At the beginning of each machine cycle, the MPU issues "status" information on the 8080 data bus that indicates the type of cycle about to be performed. At the same time, the clock generator module develops STSTB, which loads this status information into a status latch inside the 8228. This status latch output is decoded [along with DBIN, WR, and HLDA (Hold Acknowledge) from the MPU] into the system control signals MEM R (Memory Read), MEM W (Memory Write), I/O R (I/O Read), and I/O W (I/O Write). The latter two are named simply -READ and -WRITE as they leave the HPRO board. (These decoded signals also provide the internal control of the bus driver.) Note that these signals are not levels, but that they are gated by DBIN or WR from the MPU at the proper time. The status information provided by the MPU, and the system control signals developed for each of the ten types of machine cycles are shown in Figure 2-5.

TYPE OF MACHINE CYCLE

Bit	Status	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
D0	INTA	0	0	0	0	0	0	0	1	0	1
D1	WO	1	1	0	1	0	1	0	1	1	1
D2	STACK	0	0	0	1	1	0	0	0	0	0
D3	HLTA	0	0	0	0	0	0	0	0	1	1
D4	OUT	0	0	0	0	0	0	1	0	0	0
D5	M1	1	0	0	0	0	0	0	1	0	1
D6	INP	0	0	0	0	0	1	0	0	0	0
D7	MEMR	1	1	0	1	0	0	0	0	1	0

Machine cycle types: INSTRUCTION FETCH, MEMORY READ, MEMORY WRITE, STACK READ, STACK WRITE, INPUT READ, OUTPUT WRITE, INTERRUPT ACKNOWLEDGE, HALT ACKNOWLEDGE, INTERRUPT ACKNOWLEDGE WHILE HALT

CONTROL SIGNALS:
INTA
(NONE)
INTA
I/O W
I/O R
MEM W
MEM R
MEM W
MEM R
MEM R

Figure 2-5. MPU Status and Resultant Control Signals

2-5
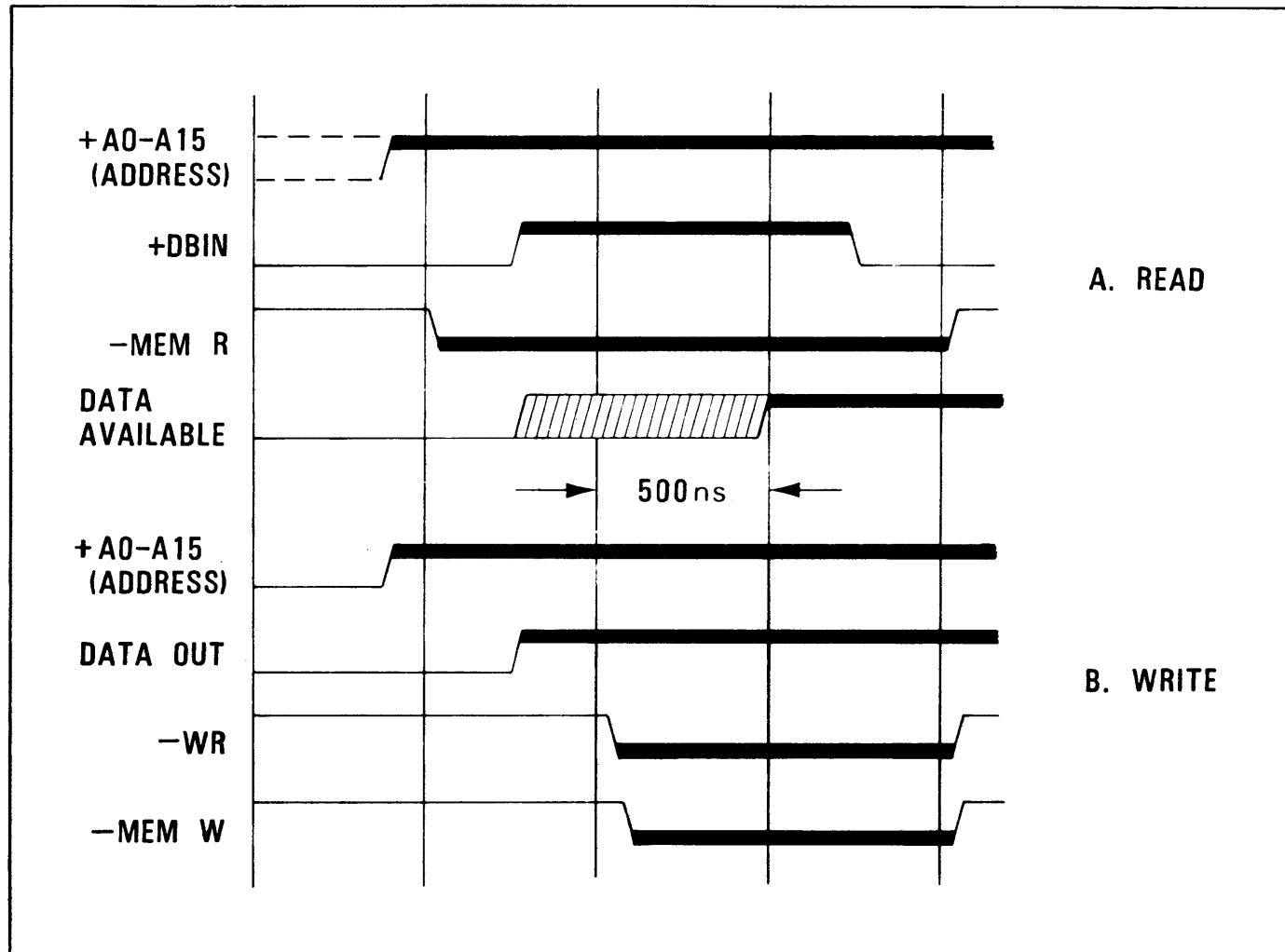
Figure 2-6. Memory Timing

Table 2-1. I/O Port Numbering

Input	Port No.	Output
Keyboard Data	00	Control Panel Indicators
Keyboard & Miscellaneous Controls	01	Baud Rate Factor
Control Switches	02	Not Used
Control Switches	03	Not Used
Received Data	04	Send Data
USART Status	14	USART Control
Printer Status	05	Printer Control & Strobe
Printer Status (Not Used)	06	Printer Low Order Data
Not Used	07	Printer High Order Data

2.2.4.3 INTERRUPT HANDLING

The 8228 is capable of handling interrupts in either of two different ways. Only one of these methods is used in the HyTerm, in which the Interrupt Acknowledge pin (23) is connected to +12V through a resistor. Connected this way, (when the MPU is interrupted (by an input from the keyboard or USART) and it performs an INTERRUPT ACKNOWLEDGE machine cycle, the 8228 automatically forces an RST 7 (Restart 7) instruction into the MPU. This instruction causes the MPU to fetch its next instruction from memory location 56_{10}, which begins the routine needed to process the input character.

2.2.5 Memory

The HyTerm memory contains both Read-Only Memory (ROM) and Random-Access (Read/Write) Memory (RAM) integrated circuits. The HPRO1 board contains two 1K x 8-bit erasable ROMs. The HPRO2 board contains a single 2K x 8-bit mask-programmed ROM. Both boards contain two 256 x 4-bit RAMs.

2.2.5.1 ADDRESSING

The eight low-order bits of the memory address bus are used to directly address all memory ICs. A8, A9, and A10 are applied to the ROM(S) to allow access to the larger memory capacity. The A11 line is applied to the Chip Enable or Chip Select inputs of all memory ICs; this line must be low in order to access any memory. A12 is not used. A13 selects between ROM and RAM: when A13 is low, ROM is accessed, and when it is high, RAM is accessed.

2.2.5.2 READING

All memory ICs are three-state devices. This means that the outputs remain in the high-impedance, or "off" state, at all times when the IC is not selected. (This allows the same memory address bus to be used for addressing I/O devices; the address lines can assume any configuration, but there will be no input to or output from memory without the proper system control signals.) ROM selection is accomplished by having address lines A11 and A13 low and by having the MEM R signal from the bus driver/system controller low. RAM selection requires A11 low and A13 high. The MEM R signal is connected to the "output disable" input of the RAMs (pin 9). This maintains the RAM outputs in their high-impedance state at all times other than during a memory read.

2.2.5.3 WRITING

When memory write is performed, A11 and A13 still select the RAMs, but the RAM output remains disabled (MEM R is high), and MEM W being low allows information on the bi-directional data bus to be written into the addressed RAM location. Note that both RAMs operate in parallel, one servicing the low-order four bits of the bi-directional bus, and the other taking care of the high-order four bits.

2.2.5.4 TIMING

Typical idealized timing waveforms are shown in Figure 2-6. Specific timing requirements for each of the memory IC types can be found in the IC information in Section 4. In all cases, the timing shown in Figure 2-6 is within the timing constraints of the invividual ICs.

2.2.6 Input/Output

The HyTerm has eight input ports and seven output ports. Five input ports and four output ports are physically located on the HPRO board; these ports represent the keyboard, control panel, and USART. The rest of the ports, pertaining to the printer, are on the 8080 INTERFACE board. Of the ports on the HPRO board, four of the inputs and two of the outputs are implemented by type 8212 I/O port ICs; the others are built into the USART.

2.2.6.1 ADDRESSING

The ports are numbered 00 through 07 and 14_{16}. Most port numbers can represent either an input or an output, depending upon the operation being performed by the MPU. For example, port 04 represents the USART. If port 04 is addressed and READ is developed, the MPU is performing an Input machine cycle and one 8-bit data byte will be transferred from the USART to the MPU. On the other hand, if port 04 is addressed and WRITE is developed, the MPU is performing an output machine cycle and it will transfer one 8-bit data byte to the USART. Table 2-1 lists the I/O ports and provides a brief description of their purpose.

The low-order four bits of the MPU's Memory Address Bus are decoded into eight signals, —PORT 0 through —PORT 7. One of these signals is developed during each I/O instruction to enable one input port or one output port. In the case where there is both an input port and an output port having the same number, the state of the READ and WRITE signals determines which will be enabled. (The use of ports 5, 6, and 7 is covered in more detail in Section 2.3.) The +ADDR4 signal from the Memory Address Bus is not decoded, but goes directly to the USART to determine whether data or control/status information is to be transferred. This is covered more fully in Section 2.2.6.8.

2.2.6.2 I/O PORT IC (8212)

All of the I/O ports on the HPRO board other than the USART use the 8212 I/O port integrated circuit. This IC can be used as either an input port or an output port, but not as both. It has one set of eight inputs which supplies eight D-type latches. These latches follow the inputs until they are clocked, at which time the data is latched. The latches' outputs go to a set of 3-state gates, which drive the IC's outputs. In addition to the data inputs and outputs, the 8212 has four control inputs: DS1, DS2, MD, and STB. The first two of these are used for device selection; when DS1 is low and DS2 is high, the port is selected. The MD input selects the operating mode of the 8212. When MD is low, it is an input port; when MD is high, it is an output port. The STB (Strobe) input is used to clock the data latches in the input mode. Further information can be found in the integrated circuit information in Section 4.

2.2.6.3 KEYBOARD DATA INPUT (PORT 0)

The eight data lines from the keyboard are continuously monitored by input port 0. When +KYSTB (Key Strobe) is received from the keyboard, it sets a D-type flip-flop. The reset side of the flip-flop drives the STB input to port 0 low, latching the data. The set side of the flip-flop develops +PAR(allel) DATA INTERRUPT, which interrupts the MPU. During subsequent execution of the interrupt service routine, the MPU performs an Input instruction from port 0. When port 0 is selected, its output drivers are turned on and the data character is placed on the bi-directional data bus for input to the MPU. After the MPU has received the data character, another instruction in the same interrupt service routine outputs a 0 on the +DA2 line of the bi-directional data bus, to output port 0. This clears the KYSTB flip-flop, which removes the interrupt from the MPU. A short time later, the MPU performs still another output to port 0, this time putting a 1 on the +DA2 line. This re-enables parallel data interrupts by removing the clear from the KYSTB flip-flop.

+BUSY is affected by +PAR DATA INTERRUPT and +EN PAR INT (Enable Parallel Interrupt). +BUSY is not used in the standard HyTerm, but is included for use in a parallel 8-bit interface should the HyTerm be utilized as a computer local output printer.

2.2.6.4 KEYBOARD CONTROL SWITCH INPUT (PORT 1)

Input port 1 receives not only the keyboard control switch inputs, but other system control functions as well. Table 2-2 lists all information entered through port 1.

Table 2-2. Input Port 1

Bit	Information
0	—CARRIER DETECT
1	—ASCII KYBD
2	+ PAR DATA INT
3	+Remote/—Local
4	—Upper Case Only
5	—Shift
6	—Control
7	—Form Feed

Unlike port 0, port 1 is not directly related to an interrupt. Instead, it is "polled" at the appropriate places in the microprogram to determine the state of the individual switches. For example, when an interrupt occurs, the microprogram must determine whether the interrupt was raised by the USART, by the keyboard, or both. (The USART status is checked first, and the USART is serviced if it has a character ready for the MPU.) The MPU polls port 1 and checks the +PAR DATA INT bit to determine the presence of a keyboard interrupt. If the keyboard has interrupted, the MPU "looks at" the Upper Case Only, Shift, Control, and ASCII KYBD bits to determine exactly what character was entered. It also checks the Remote/ Local bit to determine whether or not the transmit and/or print subroutine is to be performed.

—ASCII KYBD refers to the type of keyboard being used. The HyTerm microprogram is capable of handling either an ASCII-coded keyboard or a position-encoded keyboard, so it "looks at" this status bit to determine which section of the microprogram to use. This status bit is controlled by a jumper (see 2.2.7.3).

—CARRIER DETECT is a modem status signal. It is included here because there was no room for it in the USART status word (see Figure 2-7.)

—Form Feed is checked periodically during the main program loop.

2.2.6.5 CONTROL PANEL SWITCH INPUTS (PORTS 2 AND 3)

All control panel switches other than POWER and FORM FEED are wired into input ports 2 and 3. The BREAK switch on the keyboard is also wired to port 2. All of these switches are monitored periodically as the microprogram goes through its main program loop. The speed of the MPU is such that there is no noticeable delay between operation of a switch and the resultant action. It is virtually impossible to operate a switch without the MPU "seeing" it.

2.2.6.6 BAUD RATE FACTOR (OUTPUT PORT 1)

The HyTerm can transmit and receive at either 10, 15, 30, or 120 characters per second (110, 150, 300, or 1200 baud, respectively). If the 1200 baud option (see 2.2.7.3) is not used, the microprogram "reads" the position of the SPEED switch on the control panel and sends a corresponding 8-bit data byte to port 1 to control the USART transmit/receive rate. If the 1200 baud option is used, the microprogram bypasses the SPEED switch and supplies a different 8-bit byte to port 1. The eight bits are used by the frequency divider to develop a square wave at 64 times the desired baud rate, which is the clock frequency used by the USART.

Note that the —2X COMM CLK signal, shown on sheet 2 of the HPRO schematic, is not 64 times the baud rate; it is 128 times the baud rate, and is non-symmetrical. This signal is halved in frequency and made symmetrical by the D-type flip-flop on sheet 3 having its set output tied directly to the USART transmit and receive clock inputs, TXC and RXC.

2.2.6.7 MISCELLANEOUS OUTPUTS (PORT 0)

Output port 0 (sheet 2) has already been mentioned in relation to synchronizing the entry of keyboard data (see 2.2.6.3). This same port is used to drive the ERROR lamp and the audible alarm. It also has a bit that controls the communications +OPTION ON line, which is not used in the standard HyTerm.

Output ports 2 and 3 do not exist.

2.2.6.8 USART (PORTS 4 AND 14)

The type 8251 USART (Universal Synchronous/ Asynchronous Receiver/Transmitter) IC accepts an 8-bit byte of data from the MPU in parallel format and converts it to a serial stream of data for transmission over the communications link. Similarly, it receives data characters from the link in serial format and converts them into parallel data bytes for the MPU. During transmission, the USART adds start, stop, and parity bits. During reception, it strips these bits and also checks parity, if desired. It also checks for data framing errors and overrun errors, and can monitor modem status. It has many capabilities that are not used in the HyTerm (synchronous transmit/receive, character lengths down to 5 bits, etc.).

2.2.6.8.1 Addressing.
The CS (Chip Select) input is driven low whenever the MPU addresses port 4. No information can be transferred between the USART and the MPU until the USART is selected.

The USART also has a C/D input, which is connected to the +ADDR4 line of the Memory Address Bus. When this line is high, control information is to be transferred; when it is low, data is transferred.

2.2.6.8.2 Information Transfer.
Two inputs, RD and WR, determine the direction of information transfer. When RD is low, the USART places data or status information (determined by the C/D input) on the bi-directional data bus for input to the MPU. When WR is low, data or control information from the MPU is taken off the data bus and loaded into the USART. The RD and WR inputs are controlled by —READ and —WRITE, respectively, from the bus driver/system controller.

Note that all information transfer between the MPU and the USART is over the bi-directional data bus, through a bi-directional, 3-state buffer within the USART. Information transfer between the USART and the data link is over individual lines for Send Data, Receive Data, and each of the modem status and control lines, through a voltage level converter, to (or from) the modem. (Refer to Section 4 for information on the level converter ICs.)

2.2.6.8.2.1 Read Data.
When the USART receives a character from the data link, it raises its RXRDY (Receiver Ready) line, which sends +USART INTERRUPT to the MPU. In servicing this interrupt, the MPU performs a sequence of instructions, one of which is an input from I/O port 4. With CS low, RD low, and C/D low, the USART puts an 8-bit byte of data onto the bi-directional data bus, from where it is accepted by the MPU. The USART, having presented the data byte to the bus, resets its READY line, until the next character is received and the entire sequence repeats.

As the data is received from the data link, the USART strips off the start and stop bits, checks the parity bit (if parity checking is enabled — see 2.2.6.8.2.4), and checks for framing errors (lack of a stop bit at the proper time). If an error is detected, a bit is set in the internal Status Register. The USART also checks to see that the previous character has been accepted by the MPU — if RXRDY is still high (has not been reset by the MPU having read in the previous character), the overrun status bit is set.

2.2.6.8.2.2 Write Data.
When the MPU wishes to send data to the USART, it addresses port 4, places the data character on the bi-directional data bus, and develops —WRITE. This combination (CS, WR, and C/D all low) loads the character into the USART, which then adds the start, stop, and parity bits, and immediately begins to shift the character out, one bit at a time.

There are two status bits pertaining to data transmission: TXE (Transmitter Empty) and TXRDY (Transmitter Ready). Both of these become reset when a character is loaded into the USART from the MPU. If a relatively long time has passed since the previous character was loaded, TXRDY sets again almost immediately. This allows a second character to be loaded, even though the first has not been fully shifted out. TXRDY again resets as the second character is loaded, but this time it remains reset until the first character is completely shifted out. Then it sets again, allowing another character to be loaded. When all data characters have been fully transmitted, TXE again sets.

2.2.6.8.2.3 Read Status. When the MPU wishes to know the status of the USART, it performs an Input from port 14. This occurs after any interrupt, since the MPU needs to know if it is the USART that is interrupting, and before every data output to the USART, because the MPU must check to see that the USART is able to accept the data character.

When port 14 is addressed, the −PORT 4 signal enables the USART by driving its CS input low, and +ADDR 4 drives the USART's C/D input high, which directs the USART to transfer control/status information. −READ again directs the USART to output information onto the bi-directional data bus, but because the C/D input is high, the USART outputs status information instead of data. This status word is shown in Figure 2-7, and further information is contained in the IC data in Section 4.

2.2.6.8.2.4 Write Control. When the MPU outputs to port 14, it sends control information to the USART. However, complete control of the USART requires more than 8 bits of information. The USART is designed to accept two different control bytes, a "Command" byte and a "Mode" byte. It accepts the Mode byte only as the first control instruction following a reset. All subsequent "control writes" are accepted as Command bytes. Both of these are shown in Figure 2-7. Further information is contained in the IC data in Section 4.

2.2.7 Miscellaneous Circuitry

2.2.7.1 3-TERMINAL VOLTAGE REGULATORS

There are three 3-terminal voltage regulator ICs, shown on sheet 1 of the HPRO logic drawings, that provide the source of −5V, −12V, and +12V. These voltages are derived from the ± 15V provided by the power supply, which also provides +5V.

2.2.7.2 LEVEL CONVERTERS

The input and output voltage level converters provide the interface between the TTL inputs and outputs of the USART and the 12V (nominal) requirements of RS-232-C and the HCURL board, if used (see 2.9).

More information concerning these ICs (75150 and 75154) can be found in the integrated circuit information in Section 4 and in Section 4 of the Product Description manual.
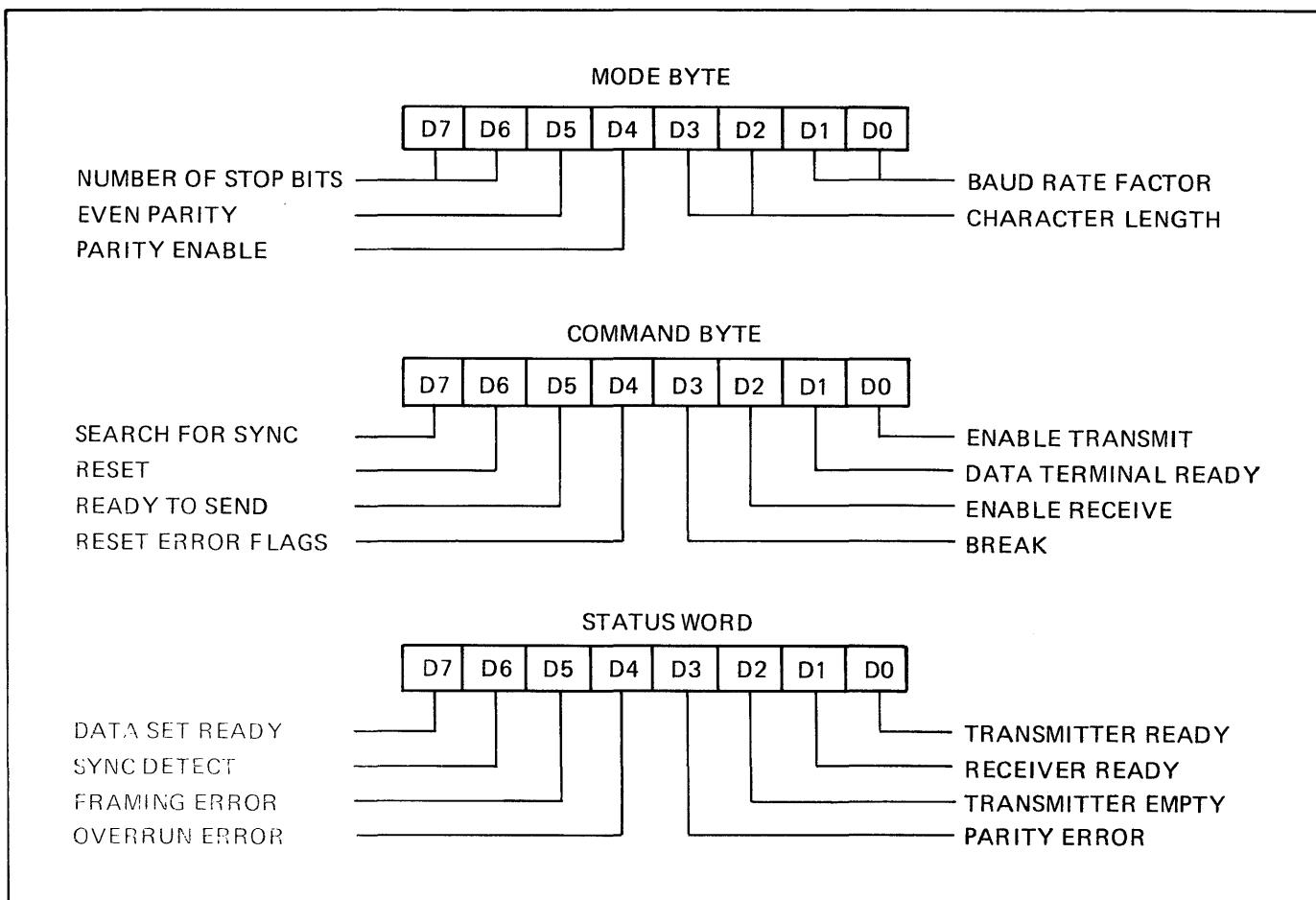
Figure 2-7. USART Control/Status Words

2-10

2.2.7.3 JUMPERS

There are four jumpers on the HPRO board that provide variations in operation. Table 2-3 lists the jumpers and their locations on the HPRO board. Most jumper installation requires soldering a 1/2-inch (1.2 cm) length of 26 AWG wire to the board. Jumper removal can be accomplished by unsoldering or simply by cutting the jumper. Later revision boards are equipped with a miniature socket for installation of the 1200 baud jumper; in this case a small shorting plug, Diablo part no. 10634, is simply plugged into the board or pulled out, instead of soldering or cutting a jumper.

2.2.7.3.1 1200 BAUD.
This option provides 1200 baud data transmission and reception. With this jumper or plug installed, 1200 baud is the only speed available; the SPEED switch on the control panel is non-functional.

2.2.7.3.2 GND CNCT.
This jumper is factory-installed. It provides the connection between pin 1 (chassis ground) and pin 7 (signal ground) of the EIA connector. If modem requirements dictate separation of these two circuits, remove this jumper.

2.2.7.3.3 ASCII KYBD.
Install this jumper when an ASCII-coded keyboard is used. When a position-encoded keyboard is used the jumper must not be installed.

2.2.7.3.4 LOCAL.
For normal HyTerm operation this jumper is left out. When installed, it allows Local operation only. This is required when the HyTerm is used as a computer output printer, for example, instead of a terminal.

2.3 8080 INTERFACE BOARD, PART NO. 40644-XX

The 8080 INTERFACE board contains I/O Ports 5, 6, and 7, which transfer data and control/status information between the terminal microprocessor and the printer microprocessor. It also contains logic that receives and temporarily stores carriage and printwheel position feedback signals from the SERVO board and supplies this data to the printer microprocessor when requested. Other circuits provide option jumper status to the printer microprocessor and develop the CLOCK A signal used by the printer microprocessor.

2.3.1 I/O Ports 5, 6, and 7

Ports 5, 6, and 7 are used to synchronize the transfer of information between the two processors. When the terminal microprocessor performs an output instruction to port 5, 6, or 7, the output information is stored on the 8080 INTERFACE board, where it is available to the printer microprocessor. The printer microprocessor periodically "reads" the 8080 INTERFACE board to see if there is any information that it should process. Similarly, as the printer microprocessor goes through its steps of controlling the printer, it provides status information to the 8080 INTERFACE board. This status is monitored by the terminal microprocessor prior to each output command.

Table 2-3. HPRO Jumpers

Option	Circuit Board			
	HPRO1		HPRO2	
	Rev. D or Earlier	Rev. E Or Later	Rev. B Or Earlier	Rev. C Or Later
1200 BAUD	Jumper F17	Plug F23	Jumper B2	Plug B2
GND CNCT	Jumper F3		Jumper A4	
ASCII KYBD	Jumper A2		Jumper E4	
LOCAL	Jumper A6		Jumper F7	

Use 26 AWG wire for jumpers; use Diablo part no. 10634 for plug.
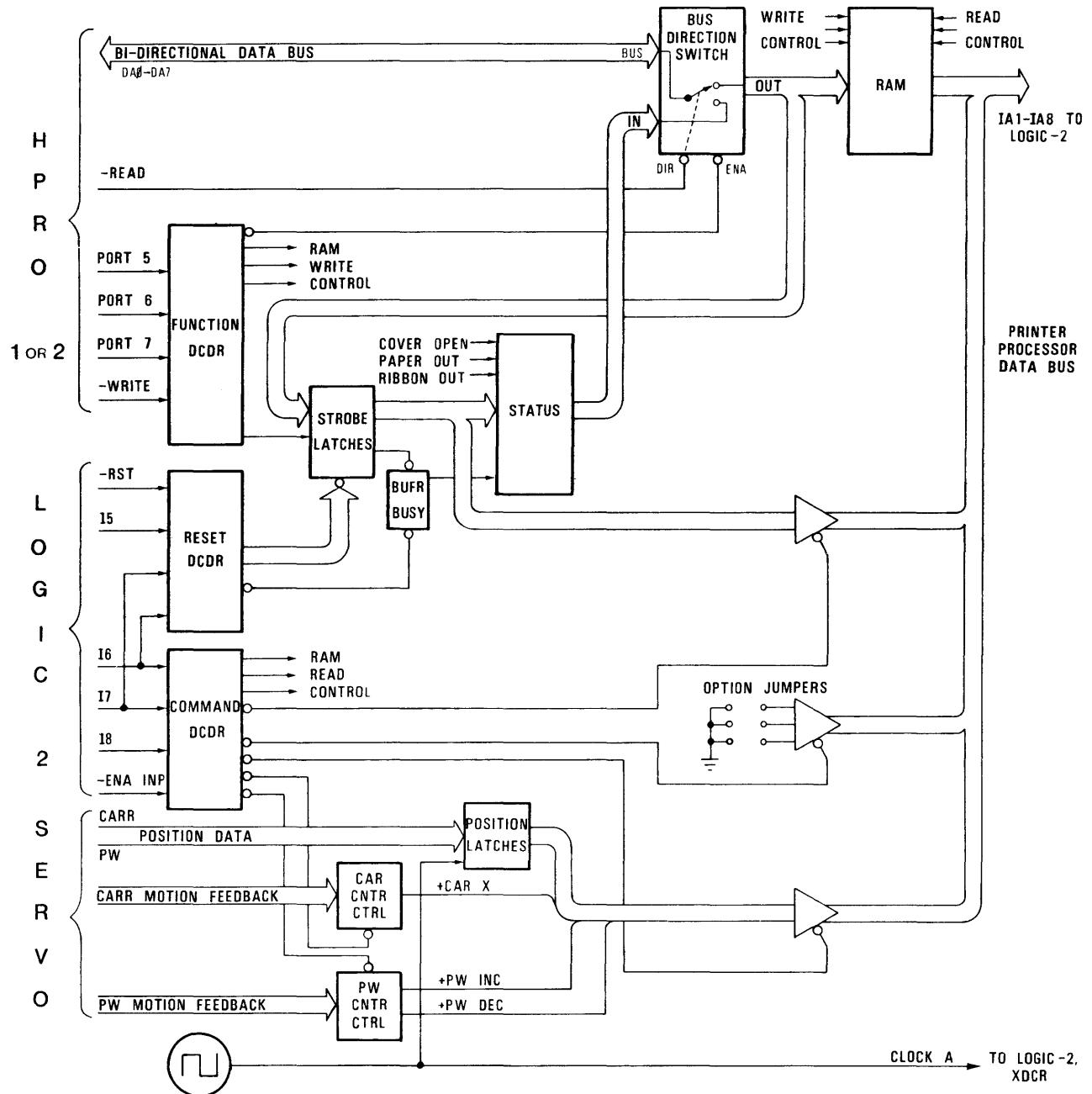
Figure 2-8. Block Diagram, 8080 INTERFACE Board

2.3.1.1 TRANSFER OF INFORMATION TO THE PRINTER

The transfer of a printer command from the terminal microprocessor to the printer microprocessor involves the following steps (refer to Figure 2-8):

(1) Terminal microprocessor "writes" low-order eight bits to port 6 (stored in RAM).

(2) Terminal microprocessor "writes" high-order bits (and direction bit) to port 7 (stored in RAM).

(3) Terminal microprocessor "writes" control word, containing strobe bit, to port 5 (stored in STROBE LATCHES), and sets BUFFER BUSY flip-flop.

(4) Printer microprocessor "reads" STROBE LATCHES to determine nature of command.

(5) Printer Microprocessor reads high-order bits and direction bit from RAM.

(6) Printer microprocessor reads low-order eights bits of data (from RAM), resets BUFFER BUSY.

2.3.1.1.1 <u>WRITE to Ports 6 and 7.</u> When a write command is executed to either port 6 or 7, the data appears on the bi-directional data bus simultaneously with the development of the —WRITE signal and —PORT 6 or —PORT 7. The FUNCTION DCDR block in Figure 2-8 contains random logic which both enables (turns on) the BUS DIRECTION SWITCH, and addresses the RAM according to the I/O port selected. Since —READ is high at this time, the BUS DIRECTION switch allows data to flow from its "bus" connection to its output, from where it is written into the RAM.

2.3.1.1.2 <u>WRITE to Port 5.</u> The control word, containing the strobe bit (or control bit, in the case of printer control functions) appears on the bi-directional data bus as —WRITE and —PORT 5 are developed. Data flow through the BUS DIRECTION SWITCH is again from the "bus" connection to the output, only this time the information on the output is not written into RAM. Instead, it is clocked into the STROBE LATCHES. Normally, only one of these latches is set at a time. The BUFFER BUSY flip-flop also sets at this time.

2.3.1.1.3 <u>Read Strobe Latches.</u> The printer microprocessor, as part of its normal processing loop, reads the contents of the STROBE LATCHES. It provides the conditions on the I5 through I8 lines (along with the —ENABLE INP signal) to gate the contents of the latches onto the IA1-IA8 bus, from where the information is received by the printer microprocessor on the LOGIC-2 board.

Depending upon the nature of the information it receives from the STROBE LATCHES, the printer microprocessor performs different operations. For example, should the RC (Ribbon Control) or RSTR (Restore) latch be set, the printer microprocessor will immediately execute the appropriate control action. On the other hand, if either the CAR (Carriage), PW (Printwheel), or PF (Paper Feed) latch is set, the printer microprocessor will go through the steps necessary to read in data from RAM storage. (The OPT latch is not used.)

2.3.1.1.4 <u>Read RAM Data.</u> After sensing either a carriage, a paper-feed, or a printwheel strobe, the printer microprocessor is directed to the steps in its microprogram that allow it to read the data stored in the RAM. The storage locations read are the same in all three instances. It reads the high-order bits first by supplying the correct combination of signals on the I5-I8 lines. It then reads the low-order eight bits from the other RAM location, and finally, it resets the BUFFER BUSY flip-flop.

2.3.1.2 TRANSFER OF INFORMATION FROM THE PRINTER

The only information received from the printer is status information. It is received by the terminal microprocessor when it performs a READ instruction from port 5. Ports 6 and 7 are not used for input to the terminal microprocessor.

The —PORT 5 signal, through the FUNCTION DCDR, turns on the BUS DIRECTION SWITCH. This time, however, —READ, being low, guides status information on the switch's input to the "bus" connection, where it is placed on the bi-directional data bus and provided to the terminal microprocessor. In addition to the contents of the STROBE LATCHES, this status information also provides COVER OPEN, PAPER OUT, and BUFFER BUSY status.

2.3.2 Carriage and Printwheel Position Data

This portion of the 8080 INTERFACE logic is identical to that found on a standard HyType II LOGIC-1 board. It consists basically of two groups of logic, the "position latches" and the counter control flip-flops.

2.3.2.1 POSITION LATCHES

On earlier boards (40644-01 and -02), there are four position latches, one each for the carriage and printwheel "even" signals, and one each for the carriage and printwheel "home" signals. These four signals occur at random in relation to the printer microprocessor operation, so they are synchronized to the microprocessor by clocking the latches with +CLOCK A. On later boards (40644-03) those latches are eliminated because other circuit changes and printer microprocessor program alterations make them unnecessary.
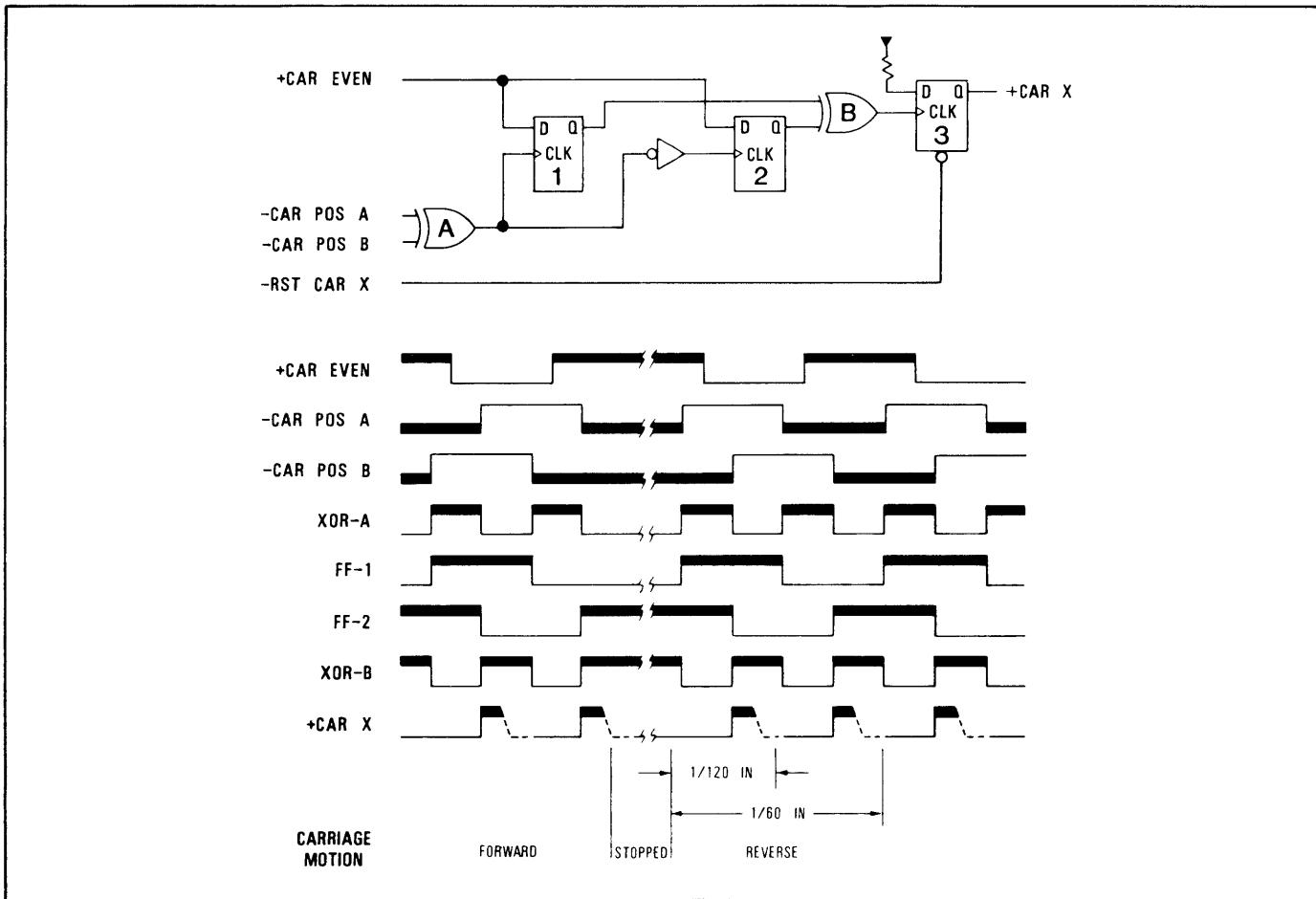
Figure 2-9. Carriage Counter Decrement Control
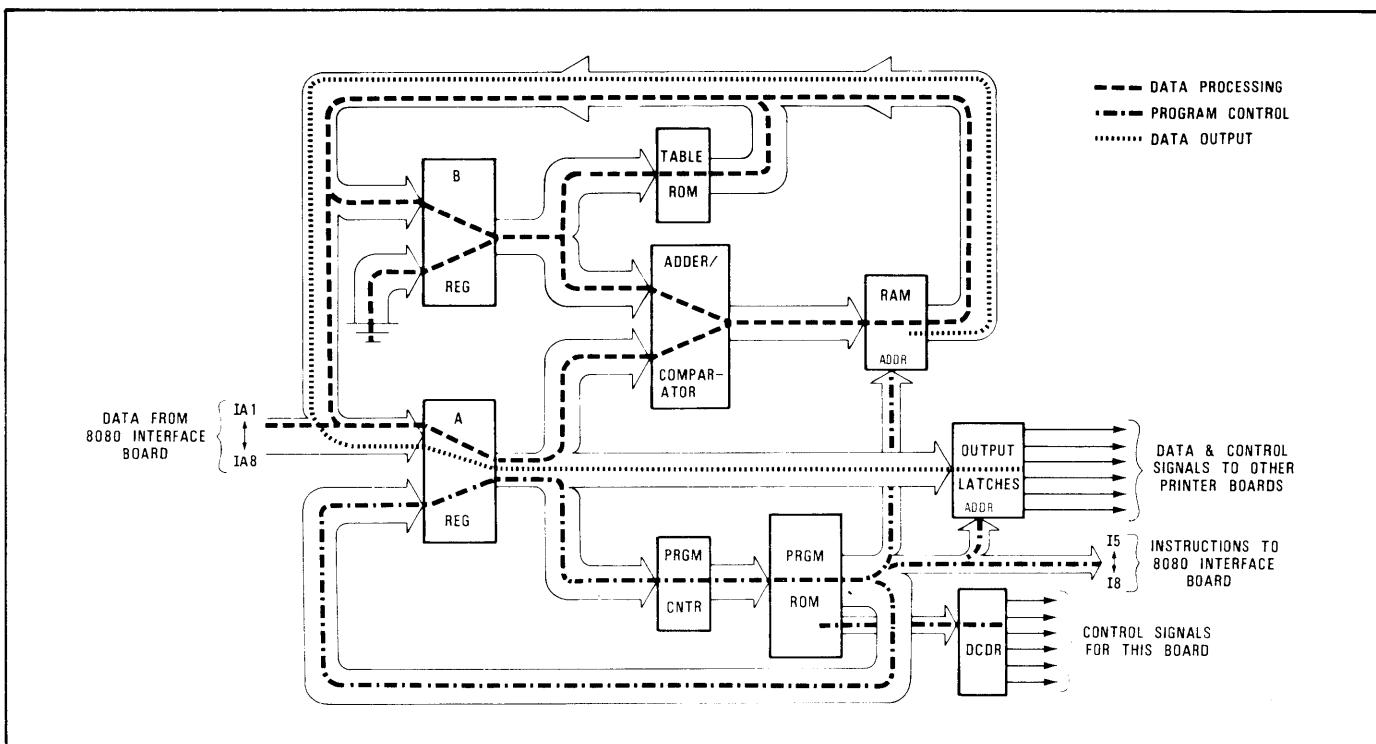
Figure 2-10. Block Diagram, LOGIC-2 Board

2.3.2.2 CARRIAGE COUNTER CONTROL

When a carriage movement command is received, the printer microprocessor loads a value, representing the number of 1/120-inch increments the carriage is to move, into a "difference counter" (in RAM). It then initiates the carriage movement, the amount of drive current fed to the carriage motor being controlled by the printer microprocessor according to the value in the difference counter. Signals fed back from the carriage motor's rotary transducer are used to decrement the difference counter for each 1/120-inch of movement. When the difference counter is decremented to zero, the carriage movement is complete, and the microprocessor terminates the operation.

The CAR EVEN (Carriage Even), CAR POS A, and CAR POS B (Carriage Position A and B) signals are developed on the SERVO board; they are derived from signals fed back from the carriage motor's rotary transducer. Their timing relationships are shown in Figure 2-9, along with waveforms of the 8080 INTERFACE board circuitry that they drive. These three input signals each make one full "cycle" for each 1/60 inch of carriage movement, which results in a single pulse on the +CAR X line for each "half cycle," or 1/120-inch increment of carriage travel.

Once it has initiated carriage movement, the printer microprocessor "reads" the +CAR X line periodically to monitor the carriage movement. When it finds +CAR X high, it decrements the difference counter, and issues an instruction to reset the counter control flip-flop. Since the response time of the printer microprocessor will vary, the length of the +CAR X pulse in Figure 2-9 is shown by a dotted line.

2.3.2.3 PRINTWHEEL COUNTER CONTROL

The printer microprocessor maintains a running log of printwheel position in its "printwheel absolute position counter," located in RAM. Thus, the microprocessor always "knows" the current printwheel position, and when it receives a command to print a new character, it calculates the shortest direction and the distance to be moved to access the new character. It then initiates printwheel movement, and uses feedback signals from the printwheel motor's transducer to update the absolute position counter. Since the printwheel can move in either direction, the counter can be either incremented or decremented. Each time the microprocessor increments or decrements the counter, it compares the counter with the desired destination; when the two are equal, it removes printwheel motor drive current and steps to the hammer-fire sequence. (This logic also keeps track of printwheel position should the wheel be turned by hand.)

Logic on the 8080 INTERFACE board receives the three feedback signals from the SERVO board, PW EVEN (Printwheel Even), PW POS A and PW POS B (Printwheel Positions A and B). Depending upon the sequence in which the position signals appear (determined by printwheel direction of rotation), either +PW INC (Printwheel Increment) or +PW DEC (Printwheel Decrement) will be developed. The printer microprocessor continually

monitors these two signals and, finding one or the other high, it makes the appropriate change to the printwheel absolute position counter, and outputs an instruction back to the 8080 INTERFACE board to clear the PW INC or PW DEC flip-flops.

The logic that develops +PW INC and +PW DEC is very similar to that which produces +CAR X, shown in Figure 2-9. The major difference is that there are six flip-flops instead of three, because both increment and decrement pulses must be developed. Only three flip-flops set/reset during each printwheel movement, depending upon the direction of rotation; the other three remain static.

2.3.3 Option Jumpers

There is provision for three jumpers to be installed on the 8080 INTERFACE board, but two of these cannot be used with the Model 1610/1620 HyTerm. They provide for terminal microprocessor control of ribbon advance and printwheel addressing/hammer energy control. Since the terminal processor's microprogram does not have the capability of handling these items, the corresponding jumpers should not be installed.

The third jumper, at board coordinates J53 on older boards and H73 on newer boards, provides for 1/2 the normal ribbon advance. It may be installed if a carbon film ribbon is not used.

2.3.4 Oscillator

A simple LC feedback oscillator provides the CLOCK A signal at 5 MHz, ±10%. This signal controls circuitry on the 8080 INTERFACE board and on the XDCR board, and provides the basic clock for the printer microprocessor on the LOGIC-2 board.

2.4 LOGIC-2 BOARD, PART NO. 40510-4X

The LOGIC-2 board contains the printer microprocessor. Refer to the block diagram in Figure 2-10. The wide buses represent 8-bit bytes of data, and the narrow buses represent three or four bits. The Output Latches provide over 30 separate signals to the other printer boards.

The A and B registers provide temporary storage for data. Both are 8-bit registers with the capability of accepting data from either of two 8-bit data sources (although one of the B-register's sources is hard-wired to provide all zeros). The Table ROM contains up to 512 8-bit factors (e.g., hammer intensity values) used by the microprogram; the Program ROM provides up to 512 16-bit instructions. The computation logic contains an adder and a comparator. When necessary to simply pass data through the adder to the RAM, the microprogram adds zero to the data. RAM capacity is 32 8-bit bytes. RAM output is the complement of its input data. The output latches store over 30 bits of output data, but a maximum of eight of them can be changed at any one time.

The buses are connected to form three interrelated loops: a Program control loop, a Data Processing loop, and a Data Output loop. The Program Control loop components control the other two loops. Thus they control all data movement on the LOGIC-2 board, as well as all data movement to and from the board.

2.4.1   Program Control Loop

After initialization, the Program Counter is reset, and first addresses location zero of the Program ROM. This ROM acts as both Program Memory and Instruction Register. That is, it contains all printer microprocessor instructions, and, when addressed by the Program Counter, outputs the current instruction for as long as necessary for completion.

For sequential program execution, the complete Program Control loop is not used. Instead, the Program Counter, the Program ROM, and the decoder are all that is needed to control data flow in the other two loops. The A register is still used, however, to feed "immediate" data from the Program ROM to the Data Processing loop. The Program Control loop is completed when it becomes necessary for the program to "branch" or "jump" to a non-sequential location. When this occurs, the new instruction address is first loaded into the A-register, and then transferred to the Program Counter. The next instruction executed is that located in the Program ROM at the new address.

2.4.2   Data Processing Loop

The data processing loop receives data from one or two of four possible sources, performs some mathematic operation on this data, and stores the result in RAM.

The sources of data are (1) the 8080 INTERFACE board, (2) the Table ROM, (3) the RAM, and (4) the Program ROM. The A and B registers are used as working registers, to temporarily hold the two 8-bit data bytes being manipulated. Possible operations include adding the two bytes together, subtracting the A register byte from that in the B register, comparing the two bytes to see if they are equal, complementing the RAM data, and passing data through unchanged.

2.4.3   Data Output Loop

Data is read from RAM, loaded into the A register, and then loaded into the Output Latches, where it is continually available to the rest of the printer. Note that since the RAM output is inverted, the complement of the desired output data must be stored in RAM by some previous instruction.

This loop is used only for printer control data. Output to the 8080 INTERFACE board is in the form of instructions (on the I5-I8 lines) which are decoded on that board to provide the desired action.

2.4.4   Basic Operation

Refer to Figure 2-11. Instruction execution is divided into two halves, called phase 1 and phase 2. The op code is present on the I1-I3 lines during both phases. The "from" address, or data source, is on the I5-I12 lines during phase 1, and the "to" address, or destination, is on the I5-I8 lines during phase 2. The I9-I12 lines are not used during phase 2.

The I4 line is used primarily to extend the ROM addressing capability; the I5-I8 lines are used for the basic RAM address, and the I4 line selects which of two sets of RAMs will be used.

2.4.5   Timing

Figure 2-12 illustrates the basic timing involved in the operation of the printer microprocessor. Two clock signals, +B and +C, are derived from the −CLOCK A signal (from the 8080 INTERFACE board) once +POWER ON goes high. The +C clock is used to divide the instruction execution into the two phases, and the +B clock provides intermediate timing. The A Register is loaded at the end of every phase 1, when −C goes low. The B Register is loaded at the midpoint of every phase 2, when +B goes low. The final waveforms in Figure 2-12 illustrate the timing of several important signals relative to the B and C clocks; note that these final signals do not occur in every instruction cycle, but only in those requiring them.

2.5   SERVO BOARD, PART NO. 40520-XX

As shown in Figure 2-13, this board logically follows the 8080 INTERFACE board and the LOGIC-2 board. It has four functions. First, it receives strobed processed command data from the LOGIC-2 board, and converts this digital data input to a voltage level representative of the absolute value of the desired velocity at which the carriage or printwheel is to be moved. Since incoming data is multiplexed, this D-to-A converter part of the circuit is common, the printwheel and carriage functions being steered to nearly identical but separate sample-and-hold circuits. The voltage level output from each sample-and-hold circuit is then switched in polarity to control the direction of movement, and the resultant polarized voltage
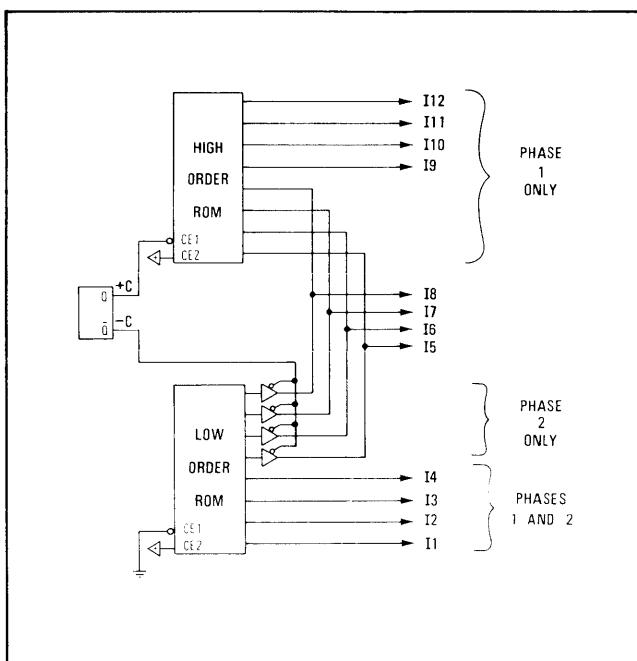
Figure 2-11. Basic Operation, Printer Microprocessor

2-16

is presented to a summing amplifier as the velocity command signal. Second, dual tachometer circuits convert incoming analog position signals to a voltage level which represents the actual servo velocity. Three digital position signals are derived from the analog position signals by a series of comparators. These digital position signals represent distance moved, and are supplied back to the 8080 INTERFACE board where they are used to generate increment and/or decrement counts for the position memories on the LOGIC-2 board. Third, the voltage level of velocity is summed with the velocity command signal to generate a 0 to 7 volt maximum servo error signal used to develop the actual servo motor drive current. Fourth, the D-to-A converter output is used on a multiplexed basis to process print hammer energy commands, which are forwarded to the PW PWR AMP board.

Refer to Figure 2-13 and to the schematic diagram to aid in understanding the following discussions.
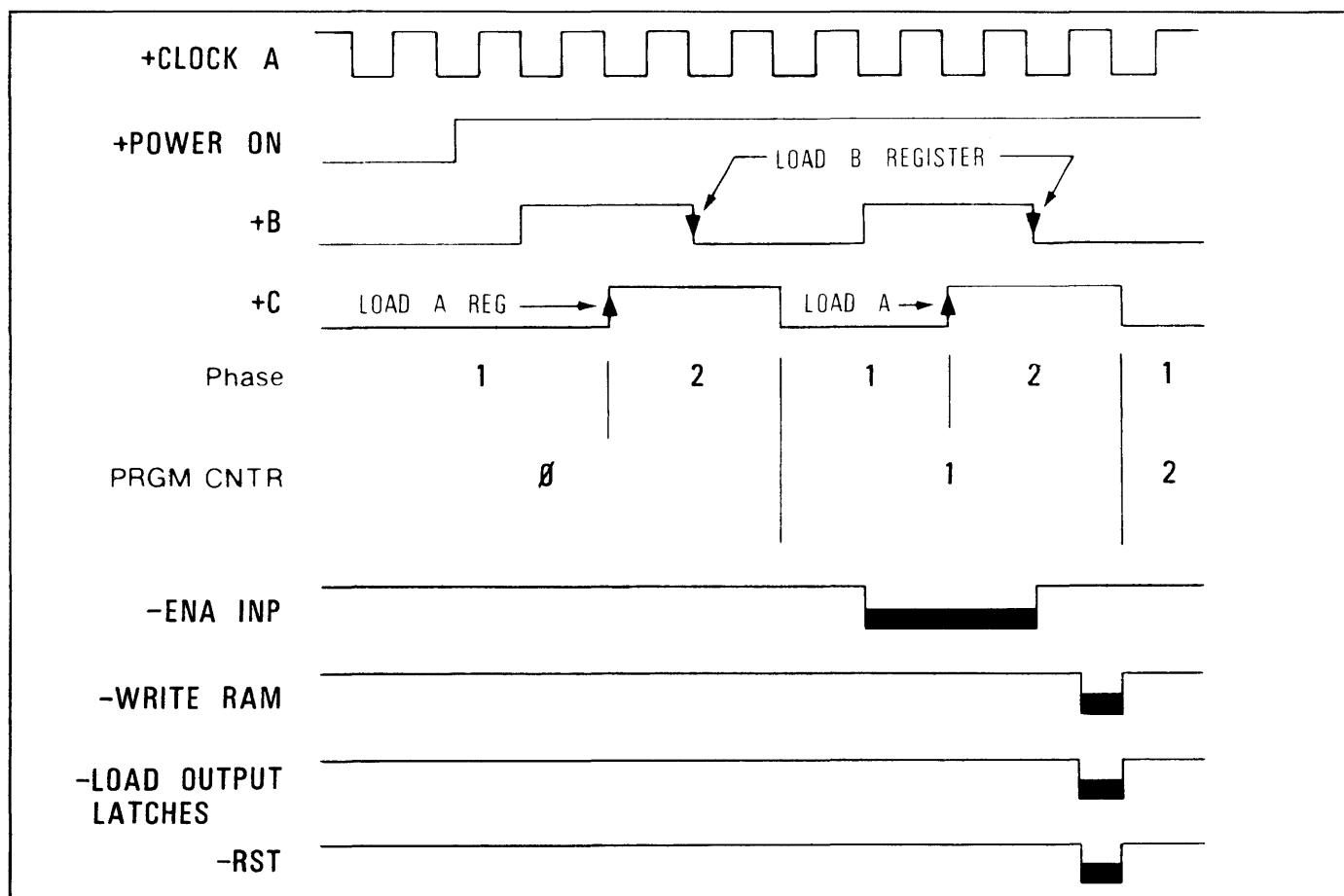
Figure 2-12. Basic Timing, Printer Microprocessor
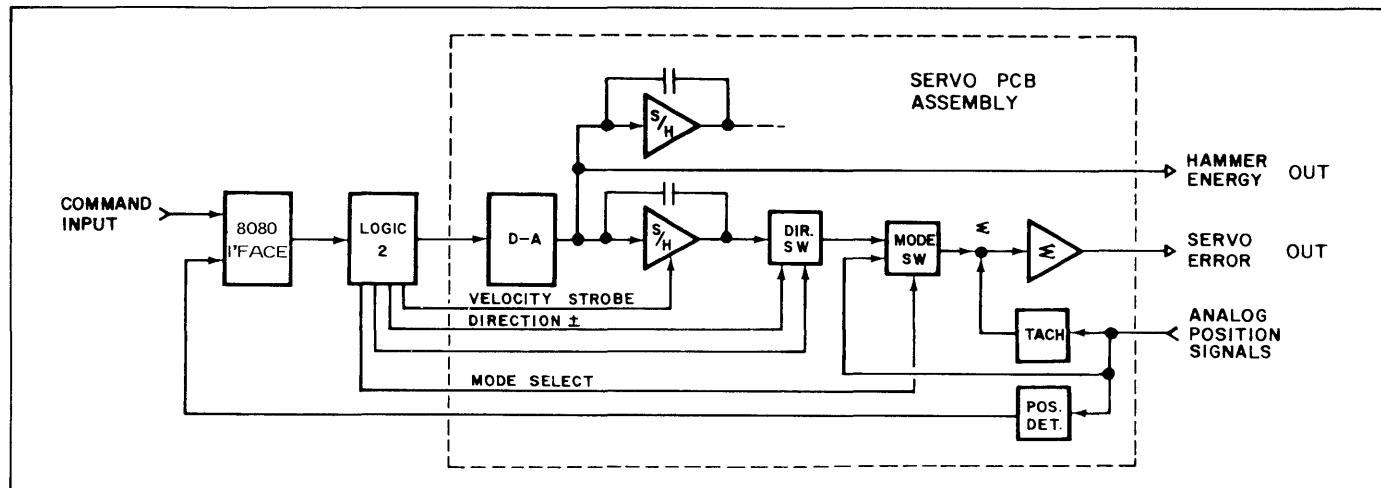
Figure 2-13. Block Diagram, SERVO Board

2.5.1 D-A Converter Circuit

This common input stage serves both the carriage and printwheel channels as well as the print hammer circuit. It consists of an 8-bit D-A converter, an operational amplifier, a buffer/driver transistor, and associated components as shown in Figure 2-14.

A reference current generator, consisting of resistors F9 and F10 and noise suppressing capacitors F6 and F7, provides a reference current for the D-A Converter G12, a monolithic 8-bit digital-to-analog converter. It supplies an output current which is the product of the 8-bit digital word input and the reference current input. This output consists of the decimal equivalent of the binary weighted value of the digital input divided by 256 such that if ALL inputs were high (=255), the output current would equal 255/256 or 99.6% of the reference current.

The output of G12 is supplied to operational amplifier E12-6. This amplifier, with its associated components, comprises a current-to-voltage converter. Buffer/driver transistor E6 in its feedback loop provides a drive current source for the stages following, through resistors D10 and F23. The output level from transistor E6 is 0 volts (all inputs low) to approximately +9.95 volts (all inputs high).

During hammer-fire sequences, this circuit is utilized to provide a time/amplitude profiled output to the hammer drive circuits which serves to regulate the print hammer energy synchronized with the character to be printed, where some characters, such as periods and commas, require much less printing energy than others, such as the M.

2.5.2 Sample and Hold Circuit

Figure 2-15 illustrates a typical Sample and Hold circuit with the basic timing involved. As shown, the circuit consists of an input switching FET, an operational amplifier (A) coupled to a buffer/driver transistor (Q), and associated components.

In operation, the output of the D-A Converter is presented to the switching FET through a resistor R1 (shown as resistors D10 and F23 on the schematic diagram). Approximately 6 microseconds after the arrival of data on the data bus input to the D-A Converter, the printer microprocessor issues a 2–microsecond Velocity Strobe pulse through an inverter and voltage divider network to turn on the switching FET. When on, the FET couples the output voltage from the D-A Converter to

holding capacitor C in the feedback circuit of amplifier A. Capacitor C holds this voltage until the printer microprocessor again strobes the D-A output. The microprocessor's cycle rate is such that it may update the charge on the capacitor 100-200 times before it actually modifies the data. The processor can modify this data only when the associated transducer has experienced a "track crossing", which occurs each time the carriage or printwheel has moved one increment. Amplifier A follows and inverts the charge on capacitor C, to produce a 0-to-negative-going voltage which represents the velocity command for the associated servo. Transistor Q buffers the amplifier's output, and provides drive current for the circuits following.

2.5.3 Servo Direction Switching

Refer to the schematic diagram. The carriage and printwheel Sample and Hold circuits are nearly identical. Each contains two paths. One path goes through a 2K resistor to a switching FET, while the other path goes through an inverting operational amplifier to a second switching FET, with the output of both FETs tied together. This means that the negative-going output of the Sample and Hold circuit is supplied as a negative-going voltage to one FET and as a positive-going voltage to the other FET. The gates of these FETs are controlled by inputs from the printer microprocessor, labeled FWD and REV, through inverters and voltage divider networks. The microprocessor can then select the correct polarity of signal to be presented to the summation circuit to control ultimate direction of servo movement.

During those times in printer operation when carriage and/or printwheel motion has stopped, and before the hammer-fire sequence is complete, the associated servo must be detented to hold its position. To accomplish this, a signal called LINEAR POS SIG is generated on the XDCR board and presented to a third switching FET whose output is also tied to the summation circuit. This FET is A12-7 for the carriage circuit, and A32-15 for the printwheel circuit. The input to the gates of these FETs comes from the printer microprocessor through the normal inverter/divider network, and is labeled LINEAR MODE. This associated servo system is detented when the microprocessor gates the LINEAR POS SIG to the summation point, while at the same time holding the two associated position switching FETs in their off state.

30 ms after gating in the LINEAR POS SIG following the last position command strobe, the printer microprocessor activates the SERVO DISABLE signal. This turns off the power amplifier and effectively removes current flow through the servo while it is at rest. This is called the "Float Mode".

In the printwheel circuit, the absolute counter is maintained in synchronization with printwheel position at all times, even if the printwheel is manually moved or should drift. In this way, printwheel movement in response to the next command can start from wherever the printwheel happens to be when the command is received.

Carriage position information is not maintained within the printer circuits. Any carriage drift or non-commanded movement would desynchronize the terminal microprocessor's carriage position information. Any carriage movement, therefore, triggers a response to remove the "float mode" and drive the carriage back to its last commanded position.
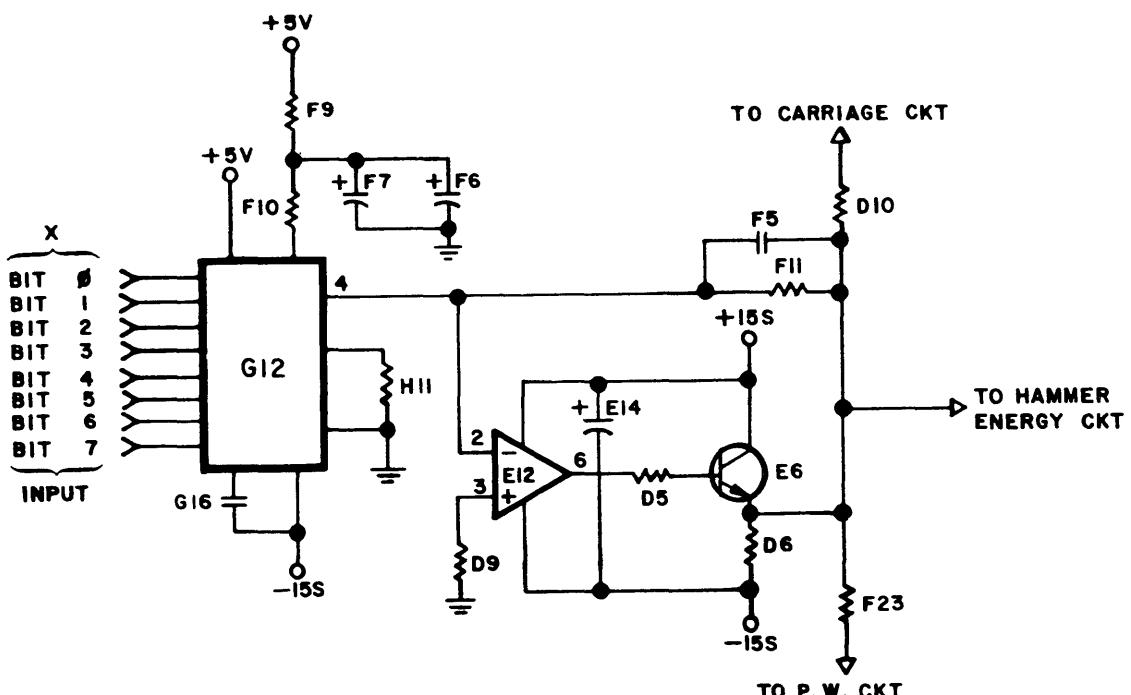
Figure 2-14. D-A Converter
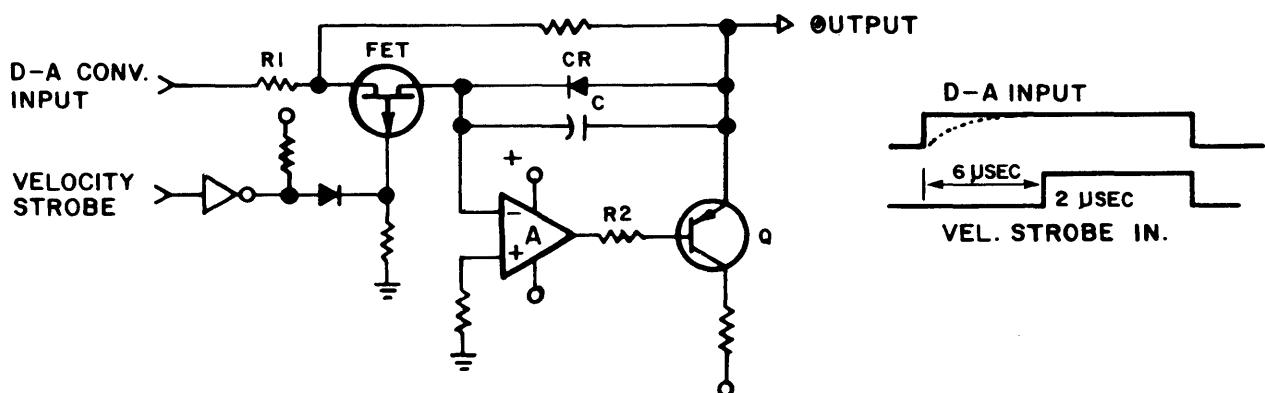
Figure 2-15. Typical Sample and Hold Circuit
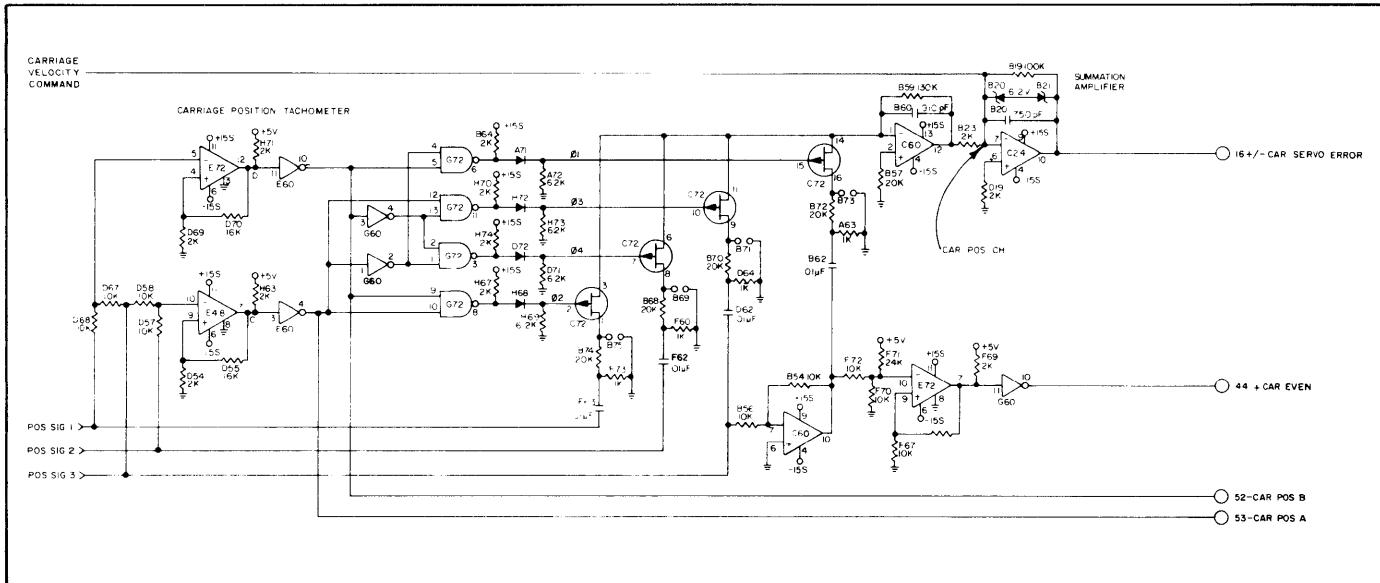
Figure 2-16. Carriage Position Tachometer Circuit
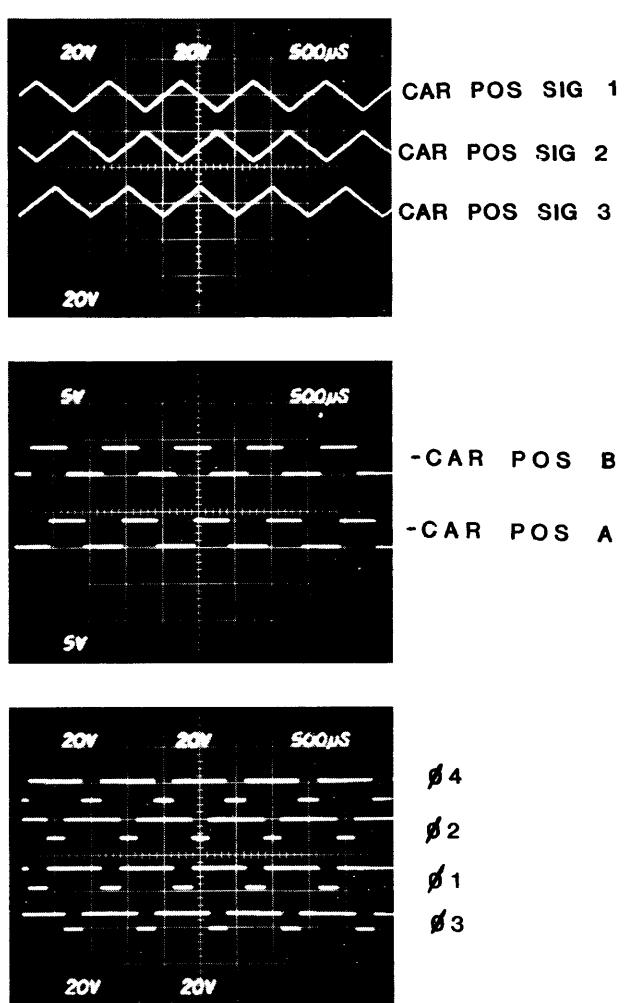
Figure 2-17. CAR POS Tachometer Waveforms

2.5.4 Servo Tachometer Circuits

Figure 2-16 is a partial schematic diagram showing the carriage position tachometer and associated circuits. Only the carriage circuit will be discussed; the printwheel circuit is very similar.

Figure 2-17 shows waveforms taken in these circuits. The design of the transducer on the carriage servo motor is such that each complete cycle of the sawtooth waveform inputs represents 1/120 inch (.212 mm) of carriage travel. Thus, while these sawtooth inputs do not vary in amplitude, they do vary in frequency. This variation, or modulation, follows actual servo speed, with the waveshape itself tracking carriage position.

Three phase-modulated triangular waveshapes are generated by the XDCR board in response to movement of the servo shaft. These signals, POS SIG 1, 2, and 3 (Figure 2-17) become the inputs to high speed comparators E48 and E72 (Figure 2-16). Their outputs are squarewaves. The duration of these squarewaves follows the frequency of the sawtooths inputs. They pass through inverters, whose outputs, -CAR POS A and -CAR POS B, are sent to the 8080 INTERFACE board for use in the position counter increment/decrement circuits. The CAR POS SIG 3 input is also sent through inverting amplifier C60-10 to develop the +CAR EVEN signal also supplied to the 8080 INTERFACE board.

The POS A and B squarewaves are also channeled through a series of inverters and gates to supply waveforms φ1, φ2, φ3, and φ4. These signals are used to control the feedback FETs C72-15, -2, -10, and -7, respectively.
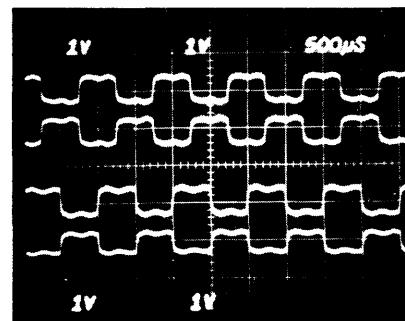
The three POS SIG sawtooth waveforms, and POS SIG 3 inverted, are supplied to the control FETs through differentiating networks. Figure 2-18 shows the waveforms taken at the capacitor-resistor junction in each network. Since servo velocity is seen here as frequency, the higher or lower the velocity, the higher or lower the level of the differentiated squarewave. The waveforms in Figure 2-18 depict carriage motion at a constant velocity. Servo velocities of less than that shown would produce a lower differentiated input to the FETs, while velocities greater than this would produce higher inputs. The control pulse to each FET will turn on the FET to pass either the positive or negative portion of the differentiated signal, depending on the direction of servo movement. The FET outputs are applied contiguously to the input (pin 1) of amplifier C60-12, with the combined result representing servo velocity. Amplifier C60-12 inverts the input and presents it to the velocity summation junction (pin 7) of the servo summation amplifier C24-10 as negative feedback.

2.5.5 Servo Summation Amplifier

This amplifier, C24-10 for carriage and C36-12 for printwheel, is the output of the servo velocity command circuit. It is an operational amplifier with a compensating capacitor, zener clamp diodes, and a gain resistor in its feedback loop. The back-to-back 6.2 volt zener diodes, plus their normal voltage drop, provide a bi-directional voltage clamp which limits the amplifier output to +7 volts. Since each volt of signal output here produces a fixed value of drive current later on in the servo motor, it is necessary to establish this voltage limit to safeguard the servo motor.

The input to this amplifier is then either the sum of actual velocity and velocity command voltages, or the LINEAR POS SIG input and velocity signal. The output is a voltage which is directly proportional to the desired amount of servo drive current. The output is labeled +/- SERVO ERROR.

Figure 2-18. CAR POS FET Input Waveforms

a

b
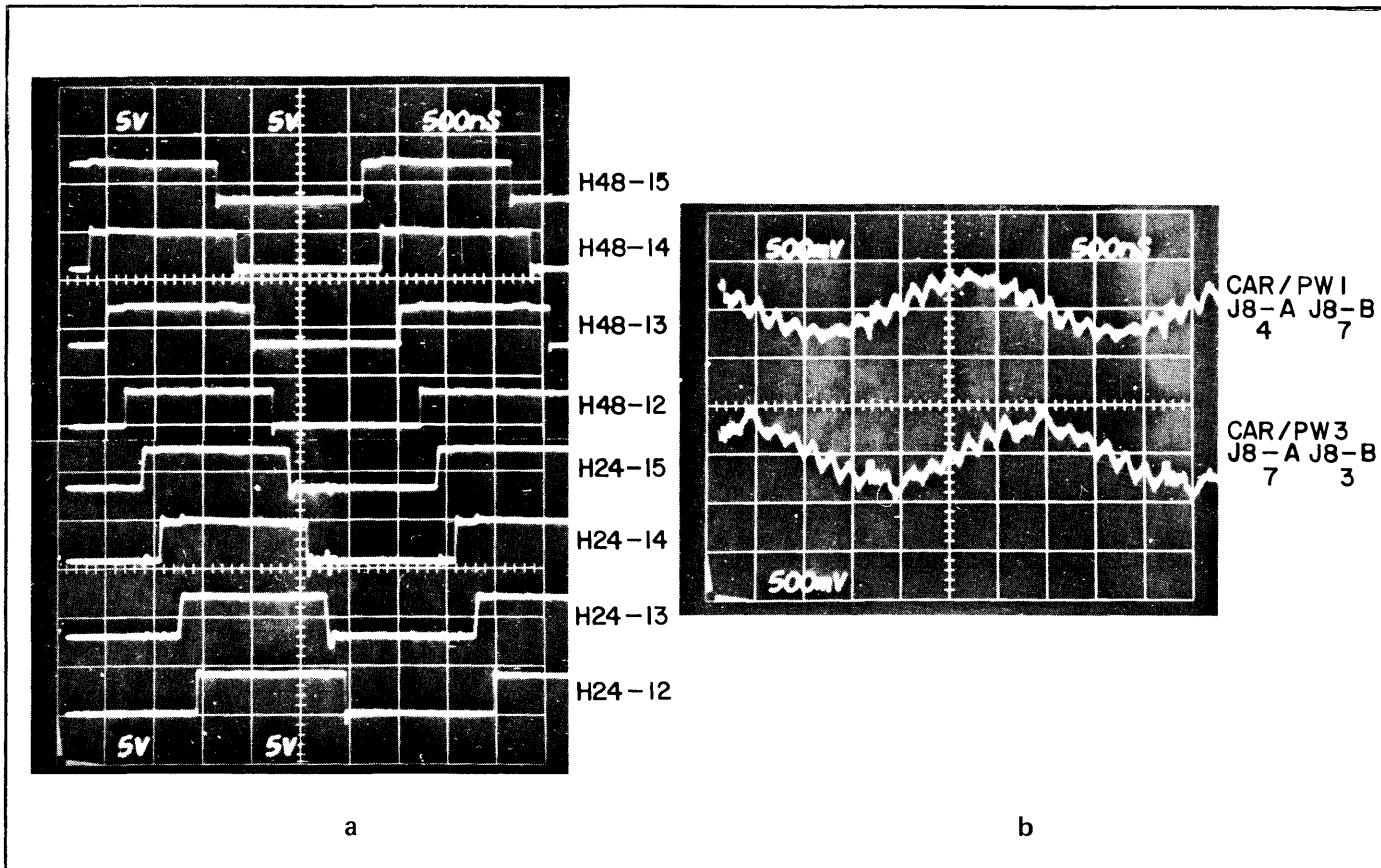
Figure 2-19. Sinewave Drive Generator Waveforms

STATOR

ROTOR

(A REPRESENTATION - WINDING DIMENSIONS EXAGGERATED FOR CLARITY)

ROTOR SEGMENTS

STATOR SEGMENTS

NO - OFFSET STATOR

90° OFFSET STATOR
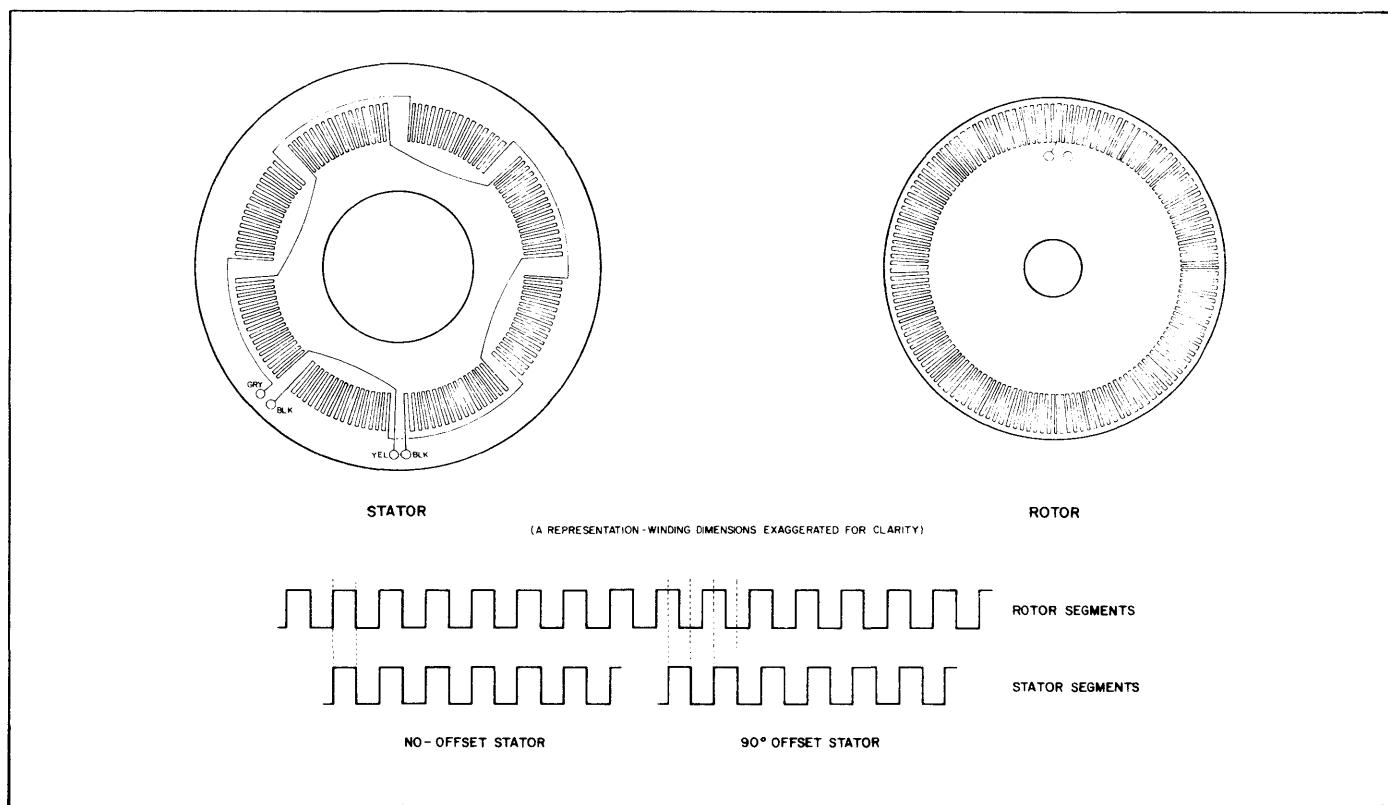
Figure 2-20. Servo Position Transducer

2.6 TRANSDUCER (XDCR) BOARD, PART NO. 40515-03

This assembly contains all of the circuits necessary to generate the sine-wave drive for the carriage and printwheel transducer stator windings, to demodulate the resultant phase-modulated carrier coming from the transducer rotor winding, and to produce three triangular position signals and one linear mode signal each for the carriage and printwheel tachometer circuits on the SERVO board (Figure 2-16). Where carriage circuits are discussed in the following paragraphs, similar circuits exist for the print-wheel.

2.6.1 Sine-Wave Drive Generator

The 5 MHz -CLOCK A input from the 8080 INTER-FACE board is used to clock two shift registers, H24 and H48. These two modules are 4-bit parallel-access shift registers connected to form a divide-by-sixteen circuit. The outputs, shown in Figure 2-19a, are squarewaves, where the output of H48-15 is followed one clock later by H48-14, and so forth. When H24-12 goes high, feedback through H24-11 (low) and through gate H30-8 drives the output H48-15 low. This condition then cascades through the registers again until H24-12 goes low, when H24-11 (high) will drive H48-15 high to start the cycle again.

These squarewave outputs are connected through inverters, pull-up resistors, and load resistors to four output lines—two for carriage circuit use and two for printwheel circuit use. The inverters act as switches, allowing current to flow through the associated load resistors whenever the inverter output is low. Seven of the inverter outputs are selected for summation to form each of the four output signals, CAR 1, CAR 3, PW 1, and PW 3. The values of the several load resistors, plus a capacitor connected from each output line to their common return line produces a set of two-phased sinusoidal waveforms, shown in Figure 2-19b, for both the carriage and the printwheel circuits. These two signals are fed to the stator "windings" on their respective position transducer.

2.6.2 Servo Position Transducer

The Servo Position Transducer consists of rotor and stator members made up as flat disks with "windings"

etched on adjacent surfaces. The rotor is mounted on the free end of the servo motor shaft, with the stator mounted over it and fastened to the motor case. Output signals from the rotor are picked up by means of an axially mounted rotary transformer.

As shown in Figure 2-20, the stator has an eight-segment "winding," with alternate segments connected together to form two groups of four. The four segments of one group are displaced laterally from the other group by a distance equal to one-half a winding width. This displacement is equal to a $90°$ phase difference. The rotor has a single symmetrical winding.

The two sinusoidal waveforms shown in Figure 2-19b are applied to the transducer's stator windings. Since all the windings in the device are nearly 1:1, the only transformation of the inputs is phase modulation caused by rotar movement. The phase-modulated output (Figure 2-22a) is applied to the Servo Feedback Amplifier.

2.6.3 Servo Feedback Amplifier

Figure 2-21 is a partial schematic showing the Carriage Servo Feedback Amplifier, which comprises a two-stage RF amplifier and a squaring circuit. Since both carriage and printwheel circuits are nearly alike, only the carriage channel will be discussed.

Figure 2-22 shows waveforms appearing in this circuit. Waveform A is the phase-modulated servo transducer output, as seen at the input to the first video amplifier, B10-1&14. Amplifier B10 has an adjusted gain of approximately 20. It amplifes and partially filters the input, as shown at its output, waveform B, taken at B10-7&8. The second video amplifier, D10, also with a gain of about 20, further filters the signal and generates a 10-volt peak-to-peak output waveform (C) which displays some squaring due to saturation limiting. This output, from D10-7&8, is applied to a high-speed squaring comparator module F10. This amplifier is overdriven, and produces a squarewave output, which is passed on to the Servo Feedback Demodulator/Integrator/Amplifier.
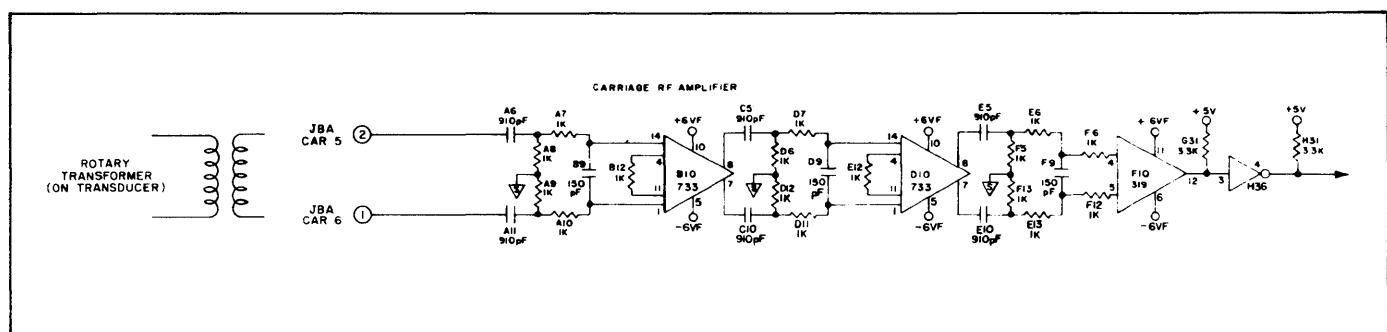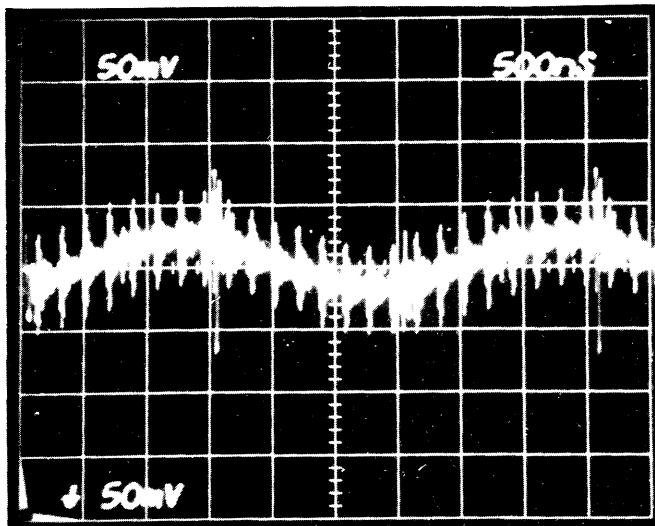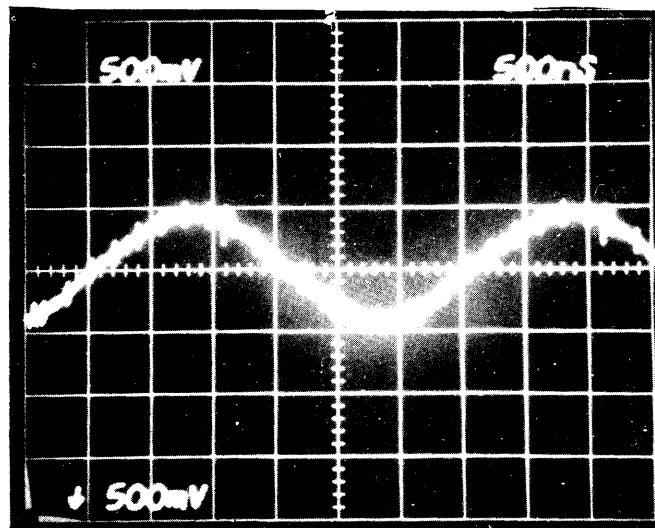
Figure 2-21. Servo Feedback Amplifier

A

1st VIDEO AMPL. INPUT
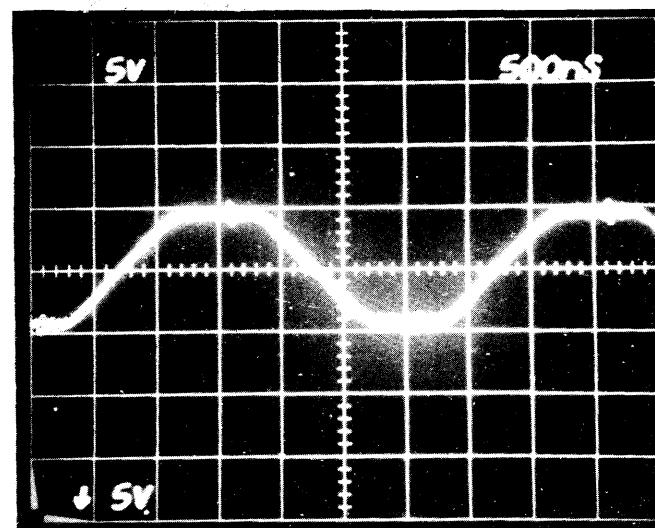
B10−1/14 (B10−1 INVERTED)

B

1st VIDEO AMPL. OUTPUT

B10−7/8 (B10−7 INVERTED)

C

2nd VIDEO AMPL. OUTPUT

D10−7/8 (D10−7 INVERTED)

Figure 2-22. Servo Feedback Amplifier Waveforms

2.6.4 Servo Feedback Demodulator/Integrator/Amplifier

Figure 2-23 is a partial schematic of the Carriage Servo Feedback Demodulator/Integrator/Amplifier. This circuit receives the output of the Servo Feedback Amplifier, synchronizes it with the Sine-Wave Drive Generator, and develops the three sawtooth waveforms, CAR POS SIG 1, 2, and 3, which are then passed on to the SERVO board.

The "input" in Figure 2-23 is the phase-modulated signal from the carriage servo transducer, after it has been squared and inverted by the Servo Feedback Amplifier (output of comparator F10). This is also shown as waveform B in Figure 2-24a. The "REF" inputs, one of which is shown as waveform A in Figure 2-24a, are from the Sine-Wave Drive Generator. These signals are exclusive-ORed to produce a waveform such as that shown at C in Figure 2-24a. The XOR outputs are applied to integrators which
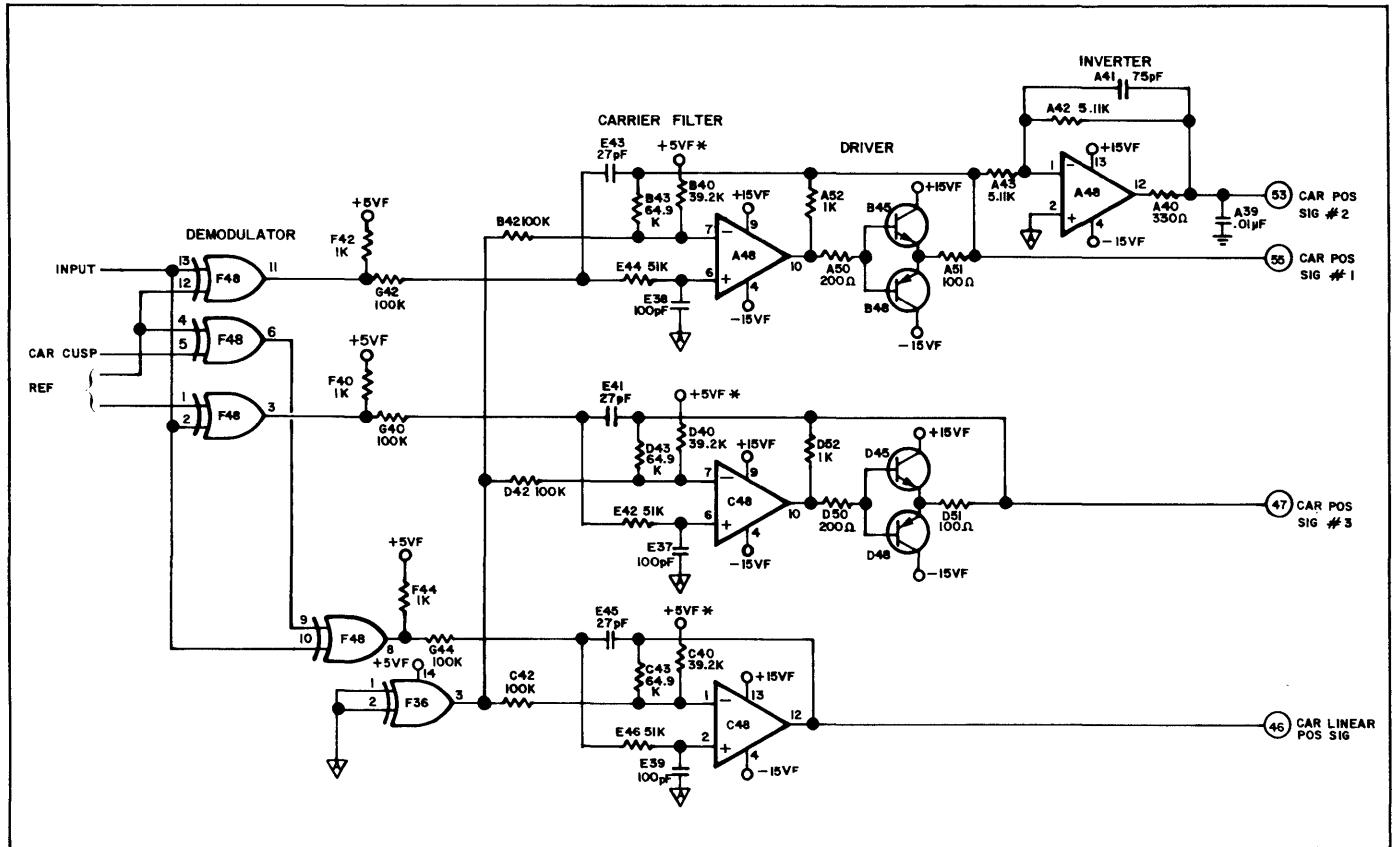
Figure 2-23. Servo Feedback Demodulator/Integrator/Amplifier
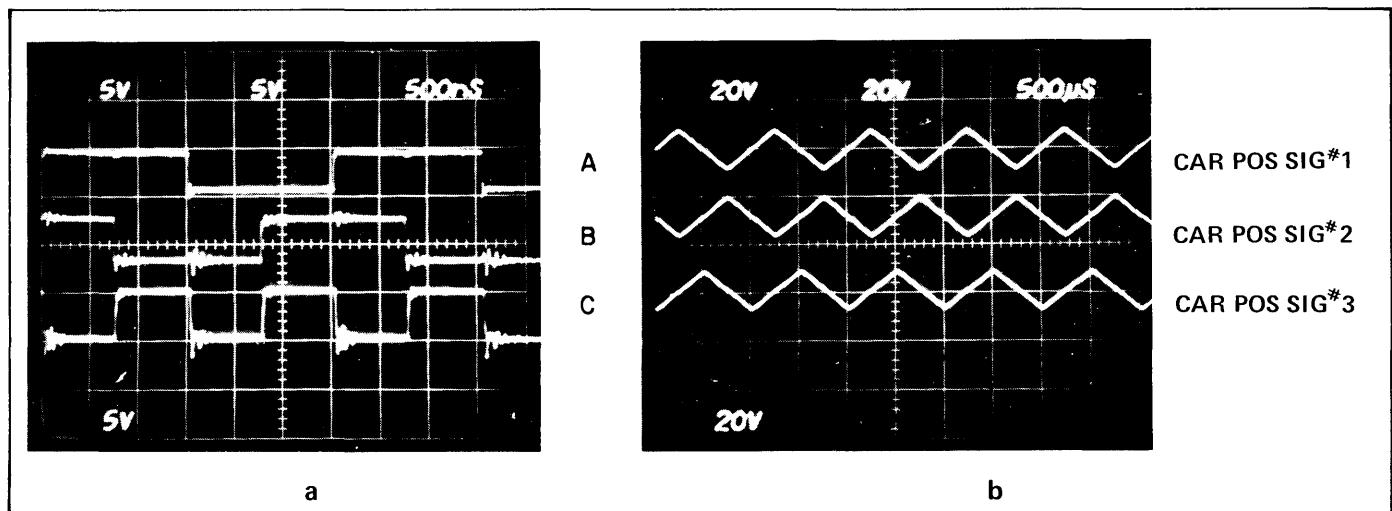
Figure 2-24. Servo Feedback Demodulator/Integrator/Amplifier Waveforms

"average" the voltage in the pulse train. This instantaneous average voltage is amplified to produce the carriage position signals shown in Figure 2-24b.

If the two inputs and the output of one of the XOR gates F48-3 or F48-11 are observed on a multi-channel oscilloscope (synchronized to the Sine-Wave Drive Generator), moving the carriage by hand will cause the input from the Servo Feedback Amplifier (waveform B) to move with respect to the "reference" input (waveform A). This causes the high/low ratio of the output (waveform C) to vary.

Refer now to Figure 2-25. As the carriage moves, the varying output of the XOR gate is applied to an integrator, which takes the average voltage value of the pulse train and applies it to an amplifier. The output of the amplifier is one of the sawtooth waveforms, CAR POS SIG 1, 2, and 3.

When the carriage is stopped, the lower circuit in Figure 2-23 develops CAR LIN POS SIG, which is used to detent the servo.
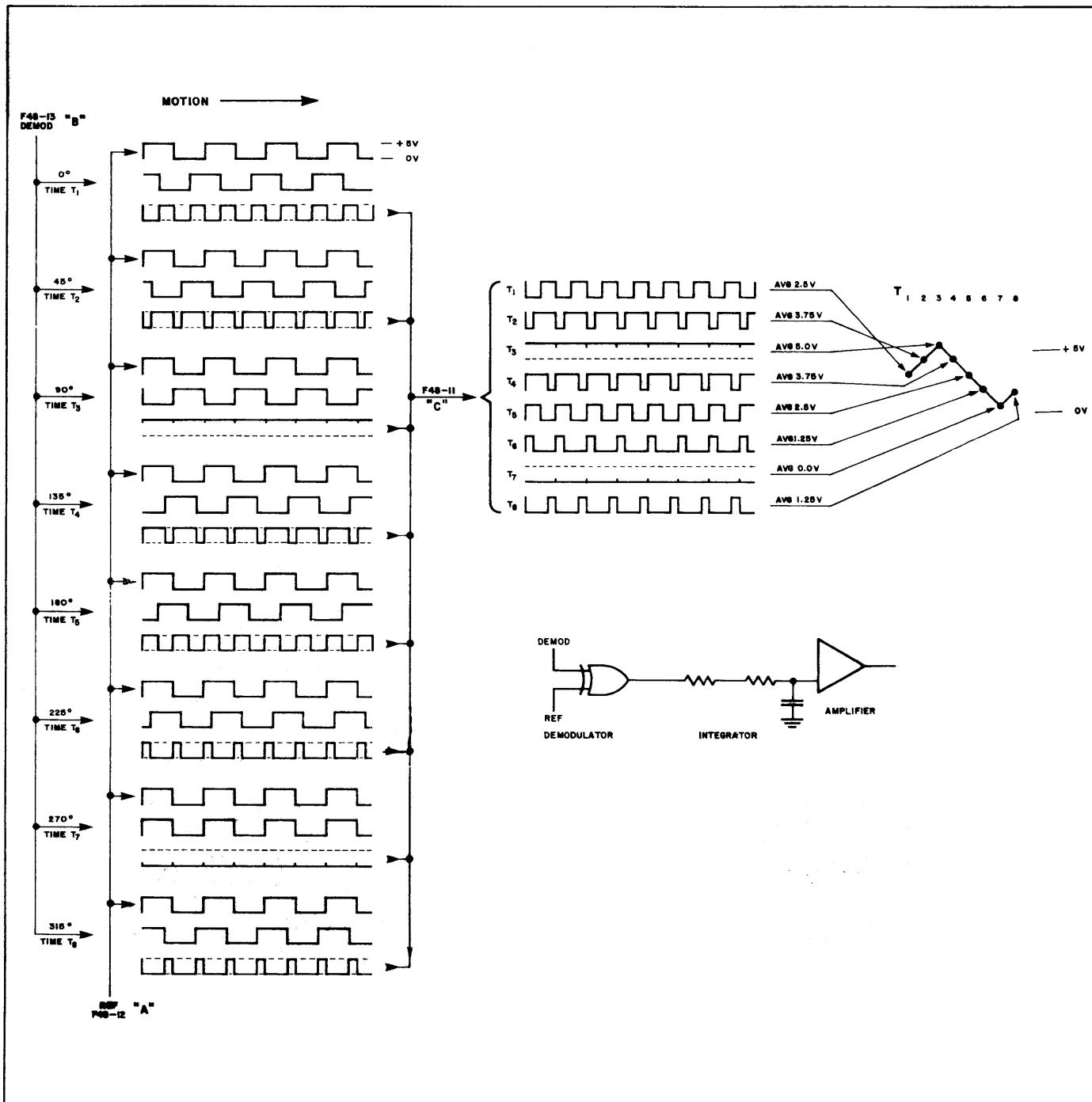
Figure 2-25. CAR POS SIG Development

2.7 CARRIAGE POWER AMPLIFIER BOARD, PART NO. 40525-XX

This assembly includes the Carriage Servo Power Amplifier, the Paper Feed Drivers, and the Power Monitor circuits. It is located in board slot D, and has a finned heat sink attached to it, to help cool the several driver transistors.

NOTE

DO NOT stand the HyType II Printer on its rear heat sink panels. The finned heat sinks are mounted on plug-in circuit boards which can be easily damaged by this practice.

2.7.1 Carriage Power Amplifier Circuit

NOTE

This circuit is nearly identical to the Printwheel Power Amplifier Circuit described in Section 2.8.1

This circuit supplies and controls current flow to the carriage servo drive motor. It is designed as an "H" bridge, allowing all current to flow through the motor from supply to supply instead of through circuit ground, to avoid circuit noise problems. Figure 2-26 illustrates the basic circuit in simplified form, where certain transistors in the actual circuit are represented as switches. Closing switches S1 and S4 will cause current to flow through the motor and resistor R right to left, while closing switches S2 and S3 will cause current to flow left to right.

Referring to the schematic diagram and Figure 2-26 will aid in understanding the operation of the circuit itself. Since the amplifier is composed of several similar circuits, only one path will be discussed.

Assume a CAR SERVO ERROR signal input of +1 volt for a commanded motor current of 1 ampere. The output of operational amplifier B55-6 will be low, and this will place a low potential on the base of transistor G58 and on the emitter of transistor G73. G73 will turn off. G73 being off turns transistor E70 off, which turns transistor E65 on to turn on PULSE REV transistor F63.

The error signal is also supplied to amplifier A50-6, the output of which is zero volts with a positive input. This will turn off transistor d42, which turn D45 off and E44 on, which turns on DRIVE REV transistor D48.

Referring to Figure 2-26 transistor D48 is shown as switch S2, while transistor F63 is shown as switch S3. Turning these two transistors on establishes a current path from the +15 volt supply through D48, resistor C53, the drive motor, and F63 to the −15 volt supply.
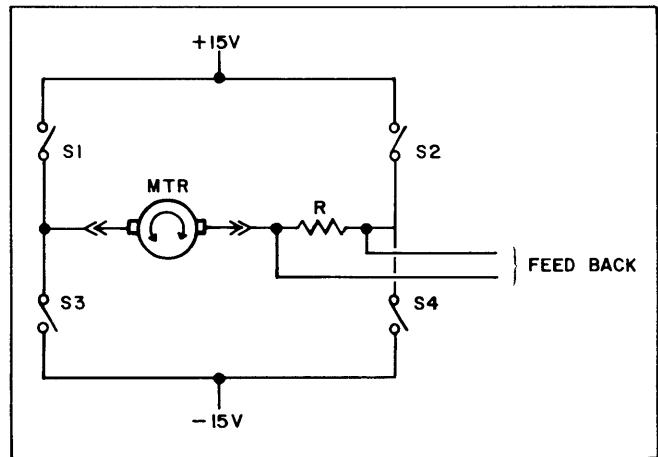
Figure 2-26. Simplified Diagram, Carriage Power Amplifier

Figure 2-27 is a simplified schematic diagram of the feedback circuit. This circuit includes the 0.1 Ohm resistor C53 located in one of the lines to the servo motor, across which is connected a precision balanced 10K Ohm resistor network and difference amplifier B62-10. The value of resistor C53 is such that its voltage drop to current ratio is 1 to 10 (0.1 volt drop equals 1.0 ampere of motor current). Difference amplifier B62-10 inverts this voltage, and presents the result to the servo error input terminal 2 of amplifier B55-6. The two signals are summed at a ratio of 10 input to 1 feedback. As current through the drive motor approaches the command level, the output of B55-6 will diminish. When motor current matches command current, the PULSE REV transistor F63 will be turned off. This removes motor current, which removes feedback voltage, and F63 is turned back on again. The circuit will oscillate in this manner to maintain motor current at the commanded level.

Should the Power Monitor circuit detect an input voltage error, it will turn transistor E77 on, turning off PULSE FWD and PULSE REV transistors F47 and F63 to disable carriage servo movement.
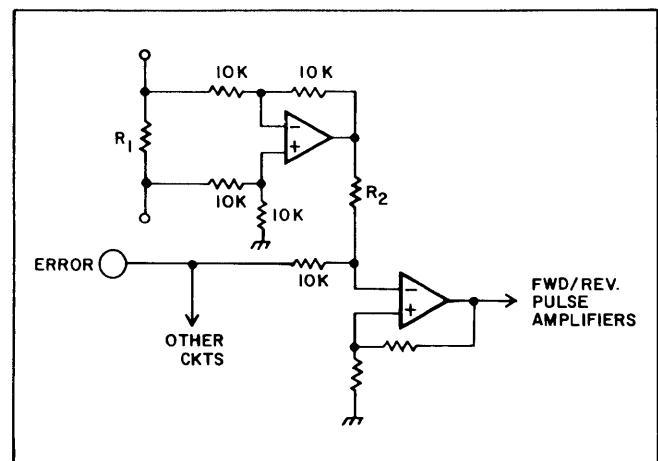
Figure 2-27. Servo Feedback Circuit

2.7.2 Power Monitor Circuit (Figure 2-28)

The purpose of this circuit is to inhibit paper feed, printwheel movement, and carriage movement by generating a series of disabling signals any time one or more of the three supply voltages drops below a level where incorrect operation might result. These signals also reset all printer microprocessor program and logic circuits to their initial or zero condition.

The circuit operates as follows: as power is turned on, the base of transistor B12 takes a negative value, and transistors B12 and B13 are off. Three divider networks begin to sample the voltage levels being supplied: zener diode B5 and resistor A11 sample the +5 volt input; zener diode A7 and resistor A9 sample the +15 volt input; and zener diode B7 and resistor B6 sample the −15 volt input. As these voltages approach their appropriate values, diodes A12, A8, B8, and B9 (operating as an AND gate) are reverse-biased. The base of transistor B12 becomes slightly positive, and transistors B12 and B13 turn on. Up to this time, transistor B16 had been on. When transistors B12 and B13 turn on, transistor B16 turns off, capacitor A22 begins to charge through resistor A24, and transistor B22 is biased off. With transistor B22 off, transistors A30, B23, C36, and C34 are all biased on, and their outputs are all clamped low.

This condition disables the printer functions as outlined above.

At the end of the delay (approximately 25 ms), transistor B22 is turned on, turning transistors A30, B23, C36, and C34 off, allowing their outputs to all go high. This removes the circuit disable clamps, starts the LOGIC-2 program counter, and initiates a Restore sequence.

Any subsequent interruption in, or decrease of, any of the three input voltage levels sampled will disable the input AND circuit leading to discharge of capacitor A22. This clamps the output low again to disable the printer. Complete restoration of power recycles this circuit, putting the printer in a proper condition to resume operation.

2.7.3 Paper Feed Drive Circuit

The paper feed stepping motor has two sets of windings, referred to as Phase A and Phase B. Current can be driven through both coils in either direction, providing four different combinations. The sequence in which the current is switched in the two windings (90° out of phase) determines the direction of motor rotation (Figure 2-29). When Phase A leads Phase B, the motor rotates clockwise (viewing the shaft end), providing upward paper movement; when Phase B leads Phase A, the motor rotates counter-clockwise, moving the paper down.
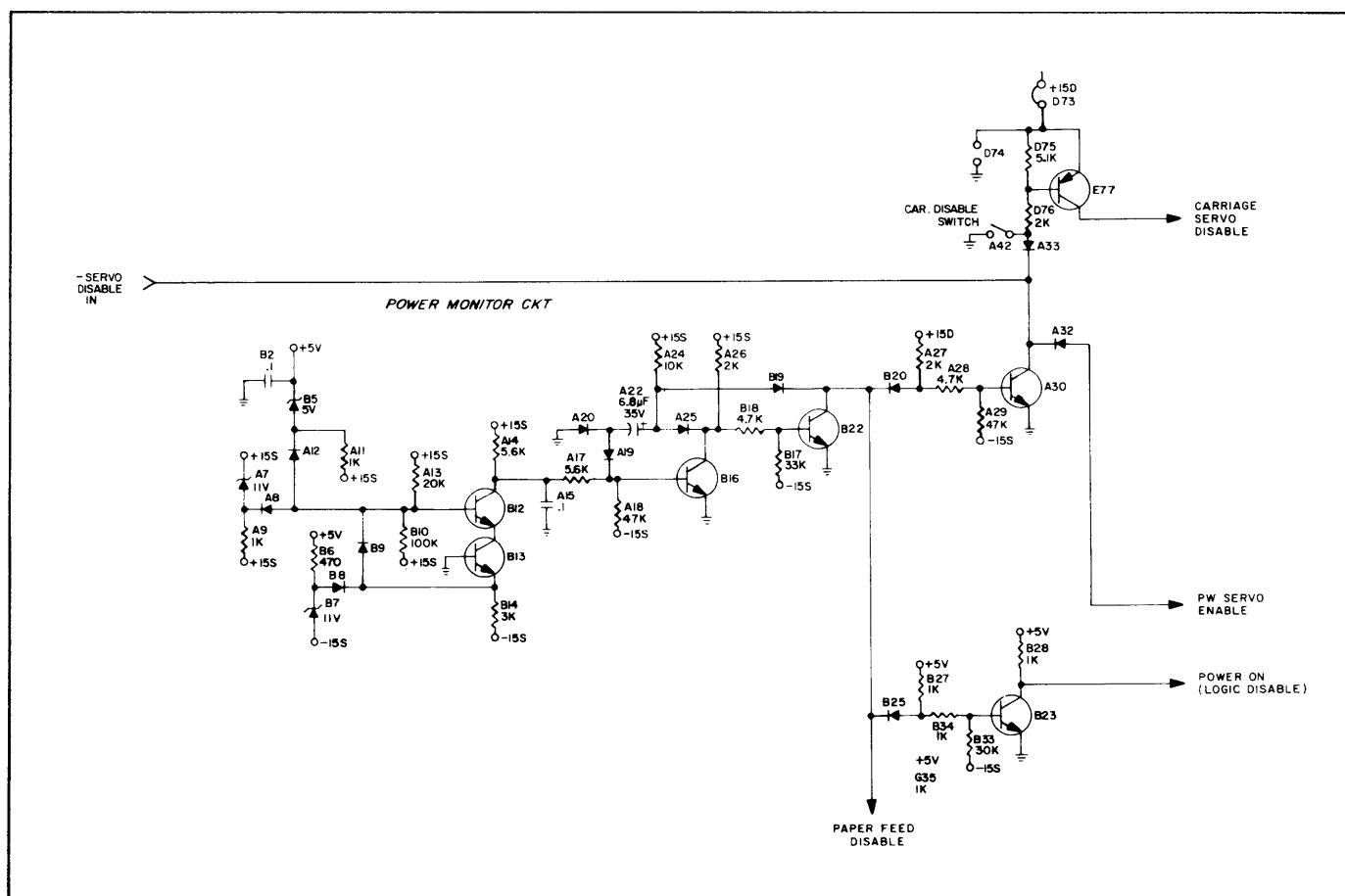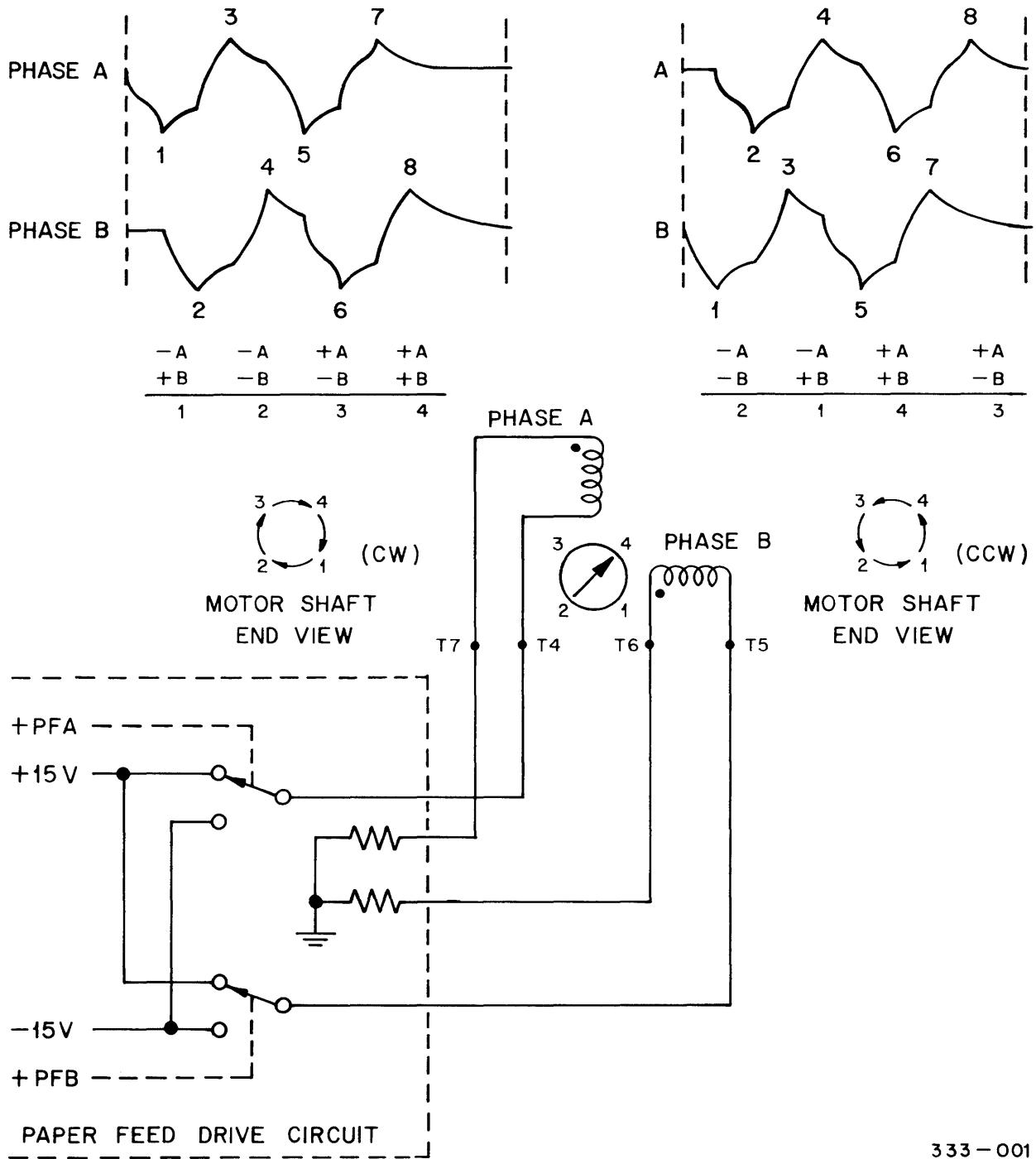
Figure 2-28. Power Monitor Circuit

Figure 2-29.   Paper Feed Stepping Motor Operations
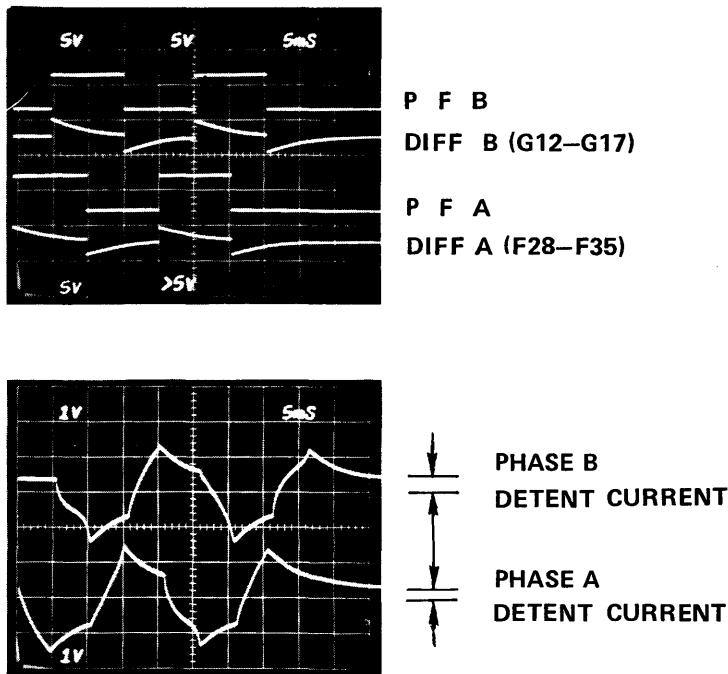
Figure 2-30. Paper Feed Drive Waveforms

The Paper Feed Drive circuit consists of two identical channels, one for Phase A and one for Phase B. The printer microprocessor provides pulses on +PFA and +PFB in the correct sequence and quantity for the desired direction and distance of paper movement. Refer to the Phase B circuit at the bottom of schematic no. 40525. (The Phase A circuit is the same—only the Phase B circuit will be covered.) Incoming pulses (Figure 2-30) are differentiated by the circuit comprising capacitor G12 and resistors G17 and G20, providing a 4-5 ms pulse to the input (pin 7) of the amplifier F18-10. This amplifier's output is coupled to current amplifiers D22/24 and E12/21, which provide the higher current required for stepping the motor.

The waveforms in Figure 2-30 represent one complete line feed operation (eight 1/48 inch increments at 6 lines per inch). One increment is represented by each level change in either Phase A or Phase B, and is equal to 7-1/2° of stepping motor shaft rotation. Thus each line feed produces 8 x 7.5° = 60° of shaft rotation at 6 lines per inch.

The paper feed motor is detented electrically when paper movement is complete. Again, discussing channel B only, a circuit comprising resistors G10, G16, and G18 (+5 volts to -15 volts) provides enough output from amplifier F18-10 to supply about .4 amp motor current, sufficient to hold the stepping motor in position.

2.8 PRINTWHEEL POWER AMPLIFIER BOARD, PART NO. 40530-XX

This assembly includes the Printwheel Servo Power Amplifier, the Ribbon Lift and Ribbon Feed Drivers, the End-of-Ribbon sensor amplifier, and the Hammer Energy Control and Driver circuits. It is located in Printer board slot H, and has a finned heat sink attached to it, to help cool the several drive transistors.

NOTE

DO NOT stand the HyType II Printer on its rear heat sink panels. The finned heat sinks are mounted on plug-in circuit boards which can be easily damaged by this practice.

2.8.1 Printwheel Power Amplifier Circuit

NOTE

This circuit is nearly identical to the Carriage Power Amplifier circuit described in Section 2.7.1.

This circuit supplies and controls current flow to the printwheel servo drive motor. It is designed as an "H"

2-30

bridge, allowing all current to flow through the motor from supply to supply instead of through circuit ground, to avoid circuit noise problems. Figure 2-26 illustrates the basic circuit in simplified form, where certain transistors in the actual circuit are represented as switches. Closing switches S1 and S4 will cause current to flow through the motor and resistor R right to left, while closing switches S2 and S3 will cause current to flow left to right.

Referring to the schematic diagram and Section 2.7.2 will aid in understanding the operation of the circuit itself. Since the amplifier is composed of several similar circuits, only one path will be discussed.

Assume a PW SERVO ERROR signal input of +5 volts for a commanded motor current of 1 ampere. The output of operational amplifier A31-6 will be low, and this will place a low potential on the base of transistor H18 and on the emitter of transistor H35. H35 will turn off. H35 being off turns transistor F32 off, which turns transistor E30 on to turn on PULSE REV transistor G26.

The error signal is also supplied to amplifier A19-7. The output of amplifier A19-7 will be zero volts with a positive input, which will turn transistor C4 off. This will turn transistor D5 off and transistor E6 on to turn on DRIVE REV transistor C10.

Referring back to Figure 2-26, transistor C10 is shown as switch S1, while transistor G26 is shown as switch S4. Turning these two transistors on establishes a current path from the −15 volt supply through G26, resistor G23, the drive motor, and C10 to the +15 volt supply.

Figure 2-27 is a simplified schematic diagram of the feedback circuit. This circuit includes a 1.0 Ohm resistor G23 located in one of the lines to the servo motor, across which is connected a precision balanced 10K Ohm resistor network and difference amplifier A45-12. The value of resistor G23 is such that its voltage drop to current ratio is two-to-one (2-volt drop equals 1 ampere of motor current). Difference amplifier A45-12 inverts this voltage and presents the result to the servo error input terminal 2 of amplifier A31-6. The two signals are summed at a ratio of 10 input to 1.6 feedback, so that as motor current approaches the command level, the output of A31-6 will diminish. When motor current matches command current, the PULSE REV transistor G26 will be turned off. This removes motor current, which removes feedback voltage, and G26 is turned back on again. The circuit will oscillate in this manner to maintain motor current at the commanded level.

Should the Power Monitor circuit detect an input voltage error, it will drive the +PW SERVO ENABLE signal low. This will turn transistor E35 on, turning off PULSE FWD and PULSE REV transistors G10 and G26 to disable printwheel servo movement.

2.8.2 Ribbon Lift Driver Circuit

This circuit consists of two subcircuits; one for ribbon lift and one for ribbon hold. The ribbon lift portion includes transistors G67 and H59. The −RIBBON LIFT signal turns G67 on to apply a ground potential to the base of H59. H59 turns on, applying −15 volts to one side of the ribbon lift coil. The opposite side of the coil is connected to +15 volts. The coil is then energized with a potential of 30 volts, to provide maximum power to rapidly lift the ribbon. At the end of the ribbon lift sequence, the printer microprocessor removes the −RIBBON LIFT signal and replaces it with the −RIBBON HOLD signal. The ribbon hold portion of the circuit includes transistors H67 and H61. The −RIBBON HOLD signal turns on transistor H67 applying a ground potential to the base of H61. H61 turns on, applying a ground potential to one side of the ribbon lift coil. The coil is then maintained in its energized state (ribbon lifted) with a potential of 15 volts.

2.8.3 Ribbon Feed Drive Circuit

NOTE

This circuit is nearly identical to the Paper Feed Drive circuit described in Section 2.7.3.

Refer to Figures 2-29, 2-30, and schematic no. 40530. The Ribbon Feed Drive circuit consists of two identical channels, A and B. Figure 2-30 shows typical input and output waveforms for each channel.

The A and B inputs, 90° out of phase, are presented to type 747 operational amplifiers E74-12/-10 where they are squared and amplified. The output of these amplifiers is coupled to current amplifiers of F48/D50-D43/F45 for channel A, and F64/D64-D58/E58 for channel B, where the drive for the ribbon feed step motor is developed.

The information in Figure 2-29 further illustrates the development of the stepping motor rotation from the two out-of-phase inputs. It should be noted, however, that unlike the paper feed operation, ribbon feed is in one direction only.

2.8.4 Hammer Energy Control and Drive Circuit

Figure 2-31 is a simplified schematic diagram of the Hammer Energy Control circuit. The HAMMER ENERGY CONTROL signal from the D-A Converter on the SERVO board is the input to this circuit. This is a signal whose instantaneous level depends on the character to be printed. The normal range of this signal is 0 to +10 volts.

The input is applied to board pin 50 and to the wiper arm of the operator's Impression Control Switch. The output of the amplifier A45-10 is then dependent on the
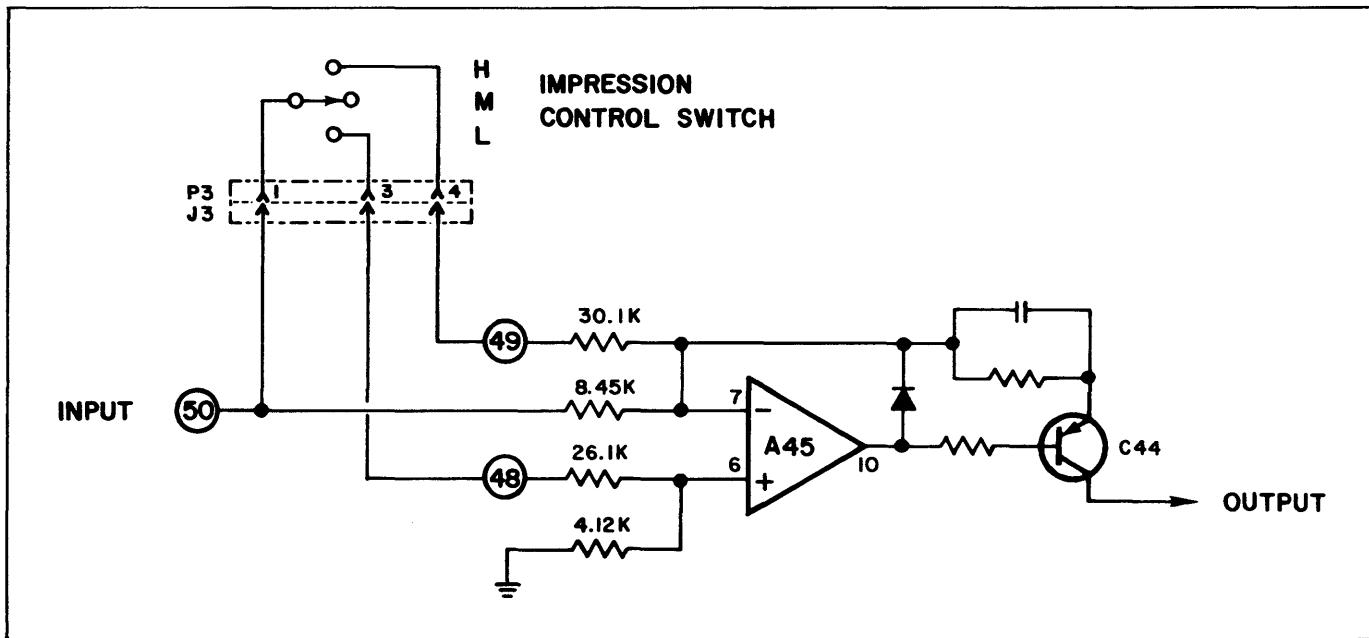
Figure 2-31. Hammer Energy Control Circuit

position of this switch, i.e., whether a portion of the Impression Control Switch input is added to or subtracted from the Hammer Energy Control input.

The —HAMMER FIRE pulse from the printer microprocessor turns transistor H50 on, to drive the hammer enabling circuits. The hammer-fire pulse from H50 is compared with the hammer energy level in comparator A64-7, and also enables transistor C65. The output of C65 switches driver transistor C73, and also establishes its output level to control the amount of current flowing to the hammer coil.

2.9 HCURL BOARD (OPTIONAL)

This section provides a brief theory of operation and circuit description of both the HCURL board electronics and the current loop network.

2.9.1 General Operation

The HCURL board serves as the interface between the terminal microprocessor (on the HPRO board) and the current loop network. This is shown in Figure 2-32. The HPRO board operates in the same manner regardless of the type of network used, and the HCURL board, through the proper placement of the jumpers and resistors, is tailored to adapt the HPRO board to a particular type of network.

The normal use of the HPRO board I/O circuitry is to drive an EIA RS-232-C interface. To accomplish this, it has voltage level converters on its I/O lines to adapt the TTL USART to the EIA interface voltage levels. The HCURL board uses identical voltage level converters to change these EIA levels back to TTL levels. Optical couplers are used to

pass the data between the level converters and the current loop network while providing electrical isolation between the HyTerm and the network. (Note that the Opto Coupler boxes in Figure 2-32 include not only the optical couplers, but also the additional support circuitry necessary. These circuits are explained in 2.9.2 and 2.9.3.)

2.9.2 Receiver Circuit

Refer to Figure 2-33. The receiver circuit can be thought of as having three terminals, two of them inputs and one an output. The two inputs are the connections to the LED in the opto coupler. The output provides data, at EIA voltage levels, to the HPRO board. This data is ultimately passed on to the 8080A MPU by the USART.

Depending upon the type of current loop network employed, the actual connections to the LED are different. This is discussed in 2.9.4. In any case, current flowing in the loop represents a "Mark," or logic 1 condition. This illuminates the LED in the opto coupler, which turns on the phototransistor, placing a "high" at the input to the 75150 level converter. This drives -DATA RECEIVED to approximately -7 Volts, the EIA level for a "Mark" condition.

When current flow in the loop ceases, the LED goes dark, the phototransistor turns off, and -DATA RECEIVED rises to about +7 Volts, the EIA level for a Space condition.

The resistor between the emitter and base of the phototransistor acts as a positive feedback to help in speeding up the turn-off time. The phototransistor output is fed into a 7414 Schmitt trigger inverter, which provides noise immunity and clean edges on all signal transitions.

FULL-DUPLEX
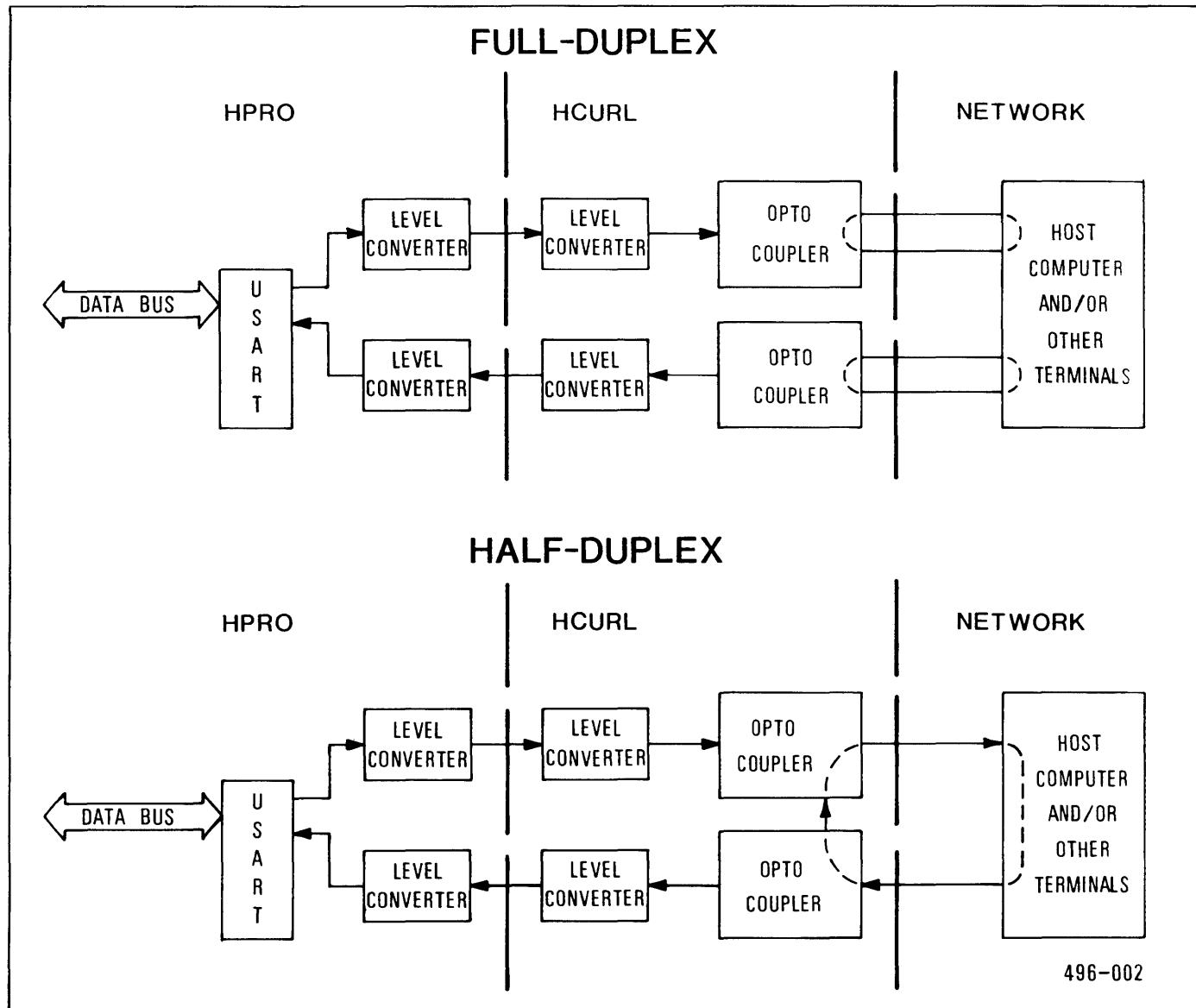
Figure 2-32. Block Diagram, Current Loop Data Flow
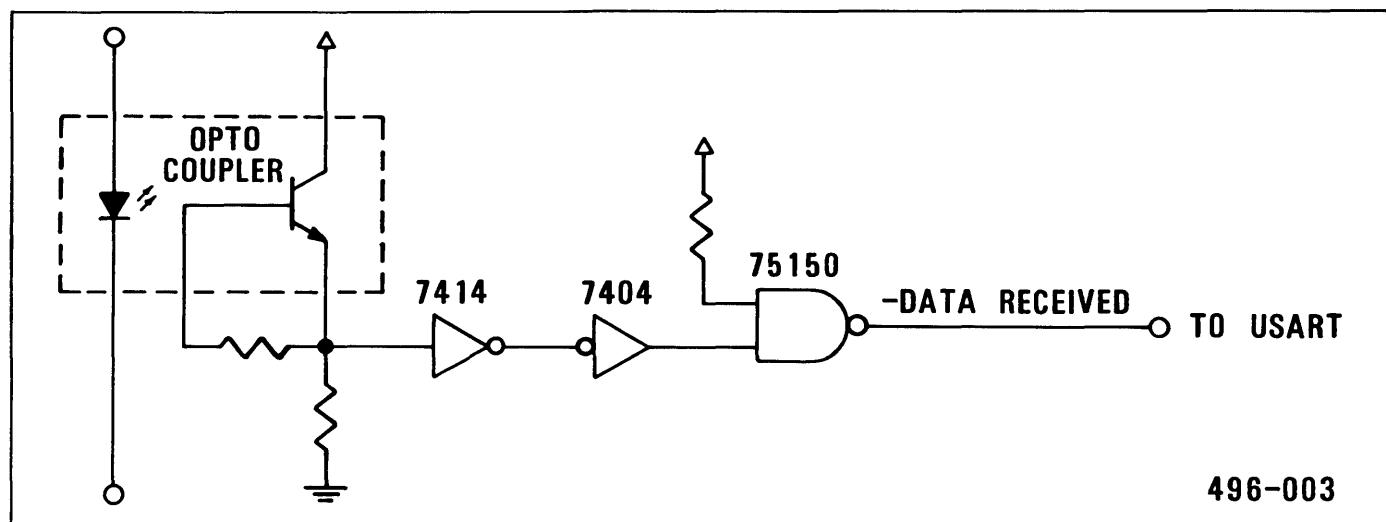
Figure 2-33. Receiver Circuit

2-33

2.9.3 Transmitter Circuit

Like the receiver circuit, the transmitter circuit can be thought of as having three terminals. Its input, at EIA voltage levels, comes from the USART (through a level converter) on the HPRO board. Its two outputs are connected to the current loop network so that the transmitter is essentially a switch, opening and closing the current loop.

Refer to Figure 2-34. EIA data to be transmitted (-XMIT DATA) is applied to a 75154 voltage converter. A "Mark" condition on -XMIT DATA is seen as a level of approximately -7 Volts. This is "inverted" by the 75154 to a +5 Volt level, which is again inverted to light LED1, and double-inverted to turn off LED2. This causes photo-transistor A to turn on and B to turn off, which allows transistor C to turn on, thus "closing the switch" in the current loop.

When a "Space" is received from the HPRO board (+7 Volts), the 75154 inverts this to a 0 Volt level, turning off phototransistor A and turning on phototransistor B, which turns off transistor C, opening the current loop.

Like the receiver circuit, the transmitter's connections to the current loop can be made in several different ways, depending upon the type of current loop network used.

However, the operation of the basic transmitter is the same in all cases.

The extra transmitter on the HCURL board, fed by +OPTION ON from the HPRO board and having outputs labeled DEMAND and DEMAND RTN, is not used in normal current loop operation. These components are provided only for use in a special 1610, part no. 23940-XX.

2.9.4 Current Loop Operation

There are basically four different current loop configurations in which the HCURL board can be used. (The only difference between the 20 mA and 60 mA active circuits is in the value of the resistor used in the current generator; these two will be discussed together under the "active" headings.) The four types are as follows:

> Full-duplex, passive
> Full-duplex, active
> Half-duplex, passive
> Half-duplex, active

In the following paragraphs, each of these will be discussed individually. In the accompanying illustrations, the receiver circuit is shown as an LED, and the transmitter circuit is shown as a transistor. Bear in mind that these symbols represent the complete circuits, discussed in 2.9.2 and 2.9.3.
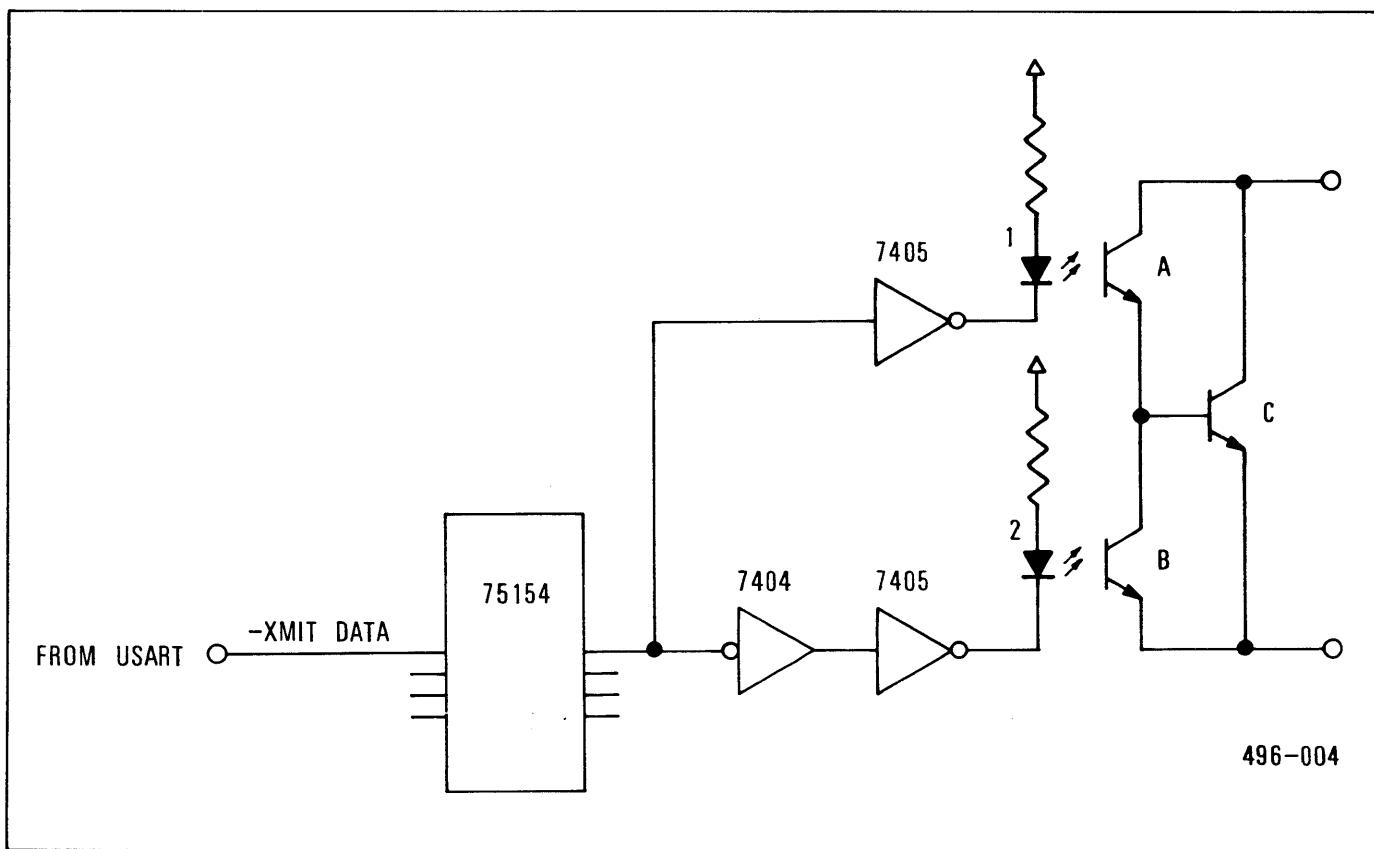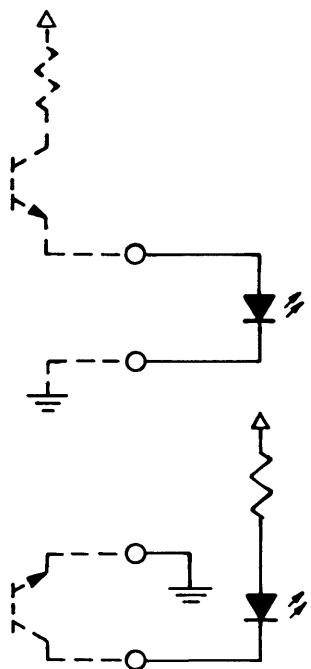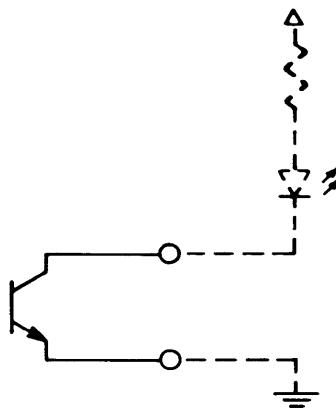
Figure 2-34. Transmitter Circuit

RECEIVER   TRANSMITTER

A.
FULL-DUPLEX
PASSIVE

B.
FULL-DUPLEX
ACTIVE

CURRENT   SOURCE

C.
HALF-DUPLEX
PASSIVE

D.
HALF-DUPLEX
ACTIVE

496-005

Figure 2-35. Current Loop Operation

2-35

2.9.4.1 FULL-DUPLEX, PASSIVE

See Figure 2-35a. Two independent external current sources are used. One, switched on and off by the external transmitter, drives the HCURL receiver circuit. The other drives the external receiver circuit, as controlled by the HCURL transmitter circuit.

2.9.4.2 FULL-DUPLEX, ACTIVE

See Figure 2-35b. Again two separate current generators are used, but this time they are located on the HCURL board. The external transmitter still controls current flow through the HCURL receiver, and the HCURL transmitter controls current flow through the external receiver. HCURL board patching is altered (from the passive configuration) to provide a return path for the current.

2.9.4.3 HALF-DUPLEX, PASSIVE

In half-duplex, only one current generator is used, and all current flows through both the receiver and the transmitter in series. See Figure 2-35c.

There are two important factors to remember in half-duplex operation. First, when one transmitter is transmitting, the other transmitter must remain "on" to allow current to flow in the loop. This is easily reconcilable, since the "idle" condition of the line is the "Mark" state (current flowing), and whenever a transmitter stops sending, it returns to the mark condition. Thus, if neither device is sending, current is flowing in the loop.

Second, when a device is transmitting, its own receiver also sees the data being transmitted. Thus, when the HCURL board is transmitting, the data is also being seen by the HCURL receiver, which echoes the data back to the USART. This data is automatically printed by the HyTerm as though it were normal received data. Therefore, the DUPLEX switch on the control panel must be in the FULL position during current loop operation. If it is in the HALF position, it will cause all transmitted data to be printed twice: once as a result of normal HyTerm half-duplex operation, in which all transmitted data is printed, and once as a result of "receiving" the same data after it is transmitted.

2.9.4.4 HALF-DUPLEX, ACTIVE

This is similar to passive half-duplex operation, except that the current generator is located on the HCURL board, and the HCURL jumpers are changed to provide a complete loop for the current. See Figure 2-35d.

2.9.5 Power Supplies

Power is provided to the HCURL board through the edge connector (+5V, +15V, and -15V). A pair of 3-terminal IC voltage regulators is used to convert the 15-volt supplies to ±12 volts, needed for the level converters to drive the EIA interface. The +12-volt supply is also used to drive the current generator(s) when the HCURL board is used in the active configuration.

1. Function keys with individual signal outputs routed to the edge connector.
2. Alternate mounting pads allow key positions 16, 31, & 46 to be mounted as shown by dotted line.
3. Keys 32 & 47 have their outputs connected together and routed to the connector.
4. Keys 49 & 60 have their outputs connected together and routed to the connector.
5. Key 33 is a shift lock key.
6. Positions which may be populated with repeat type keys.
7. Positions which have pads in circuit board and power/ground traces connected, but no signal traces.

Figure 2-36. Key Positions of Hall-Effect and Saturable-Core Keyboards

2.10 KEYBOARD

Either of two types of keyboards may be used in the 1620, one employing Hall-effect keyswitches (Microswitch) and one employing saturable-core keyswitches (Cortron). The external appearance and the interface characteristics of both keyboards are very similar, but the internal operation is substantially different.

The 7-bit code produced by the keyboard is the binary representation of the relative key position. This code is then converted to the corresponding ASCII code by the terminal microprocessor program: it uses the position code as part of a memory address, and reads the ASCII code from ROM.

Key positions are illustrated in Figure 2-36. Not all positions are used. Positions used by each of the different types of keyboards are noted in the keyboard layouts in the Product Description manual.

Function key output is not encoded — instead, each key has its output brought out to the connector separately. All function keys produce low-level signals when depressed.

2.10.1 Hall-Effect Keyboard (Schematic No. 23897)

The basic construction and operation of all Hall-effect keyboards is the same, even though the key complement and layout may vary. The keyboard features solid-state Hall-effect key switches, MOS encoding, and n-key rollover. Refer to the block diagram in Figure 2-37. Each alphameric key depressed provides a pulse simultaneously on 2 of the 13 code lines going into the MOS decoder/encoder. This chip performs several functions: it transforms this 2-of-13 code into the proper 7-bit key position code, it keeps track of the sequence in which keys are operated (n-key rollover), it provides latches for the output data, and it develops an output strobe signal. Each 7-bit position code is loaded into the output latches, which develop the —DATA 0-6 signals. +KYSTB is then developed, which is 10 to 100 microseconds (nominally 50 microseconds) in length. The —DATA 0-6 signals are levels, which change only when replaced by the next code.

The 2-of-13 code and the binary position code produced by a key in each possible keyboard position are listed in Table 2-4. Note that the binary value of the position code is not a <u>direct</u> indicator of key position; it is simply a unique code used as an address by the terminal microprocessor.

2.10.1.1 KEY ENCODING

Each individual keyswitch contains an integrated circuit chip which is sensitive to a magnetic field set up by magnets mounted on the keystem plunger. When the key is actuated, the magnetic field around the chip is altered, and the IC produces a short negative pulse.

This pulse is routed, via the circuit board, to two of the inputs of the large MOS decoder/encoder. Note that the
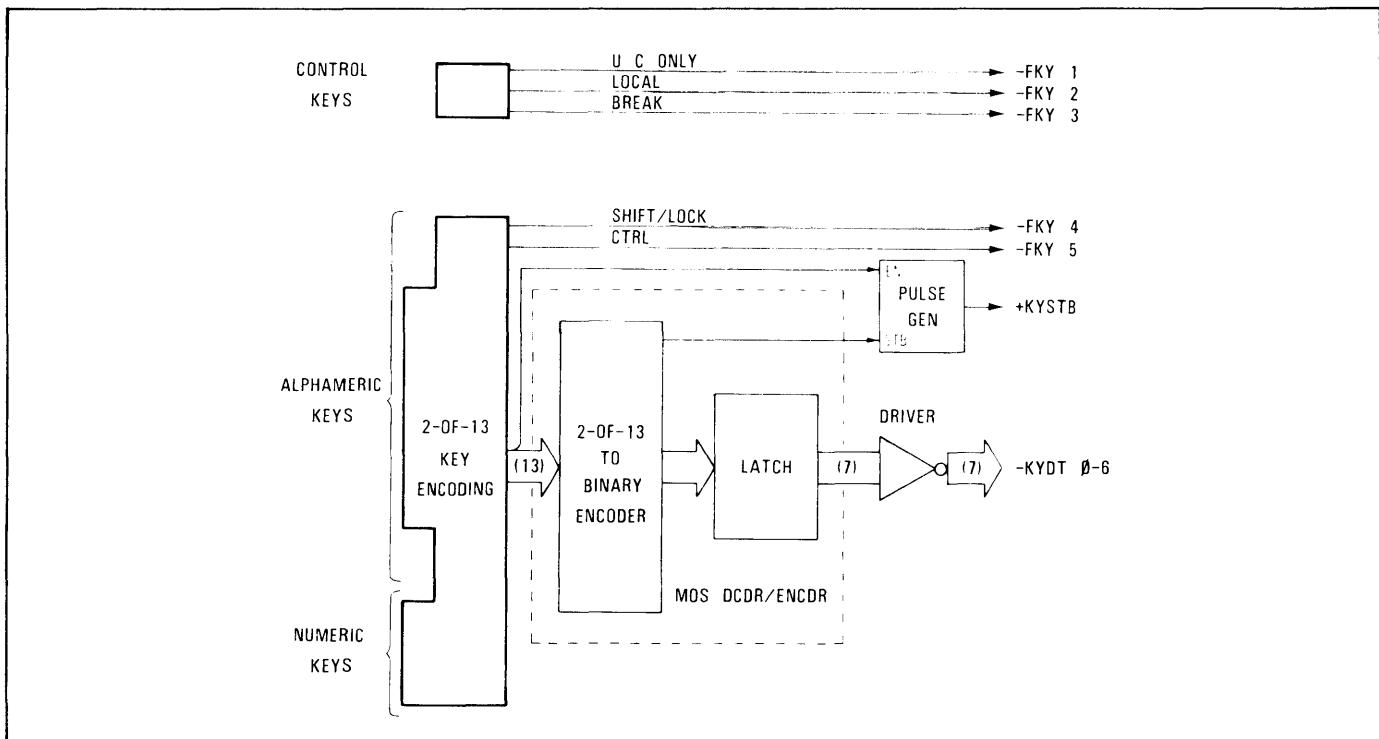
Figure 2-37. Block Diagram Hall-Effect Keyboard

2-37

2-of-13 encoding is accomplished on the circuit board: the position of the keyswitch on the board determines which two of the 13 inputs to the MOS integrated circuit will be activated.

All keys in the numeric section of the keyboard and all keys in the alphameric section except the CTRL, SHIFT and LOCK keys are coded in this manner. The function keys operate in a similar manner, but their outputs are levels, and are brought directly out to the connector. The CTRL and SHIFT/LOCK key outputs are not encoded: instead, they go through the interface connector to the terminal microprocessor on the HPRO circuit board.

2.10.1.2 MOS DECODER/ENCODER

The MOS chip receives the pulsed 2-of-13 codes from the various keys, decodes the 2-of-13 code, and re-encodes it into the proper 7-bit key position code. This position code is loaded into the 7-bit output latch, and then the strobe is developed.

The 7-bit code set into the output latches remains there until it is replaced by another code. Thus, if no key has been operated for quite some time, the output latches still reflect the code corresponding to the last key actuated.

2.10.1.3 STROBE GENERATION

The +KYSTB signal is generated by a special integrated circuit which has two modes of operation, one for normal action and another for repeat-type keys.

2.10.1.3.1 Normal Action. For normal operation, the enable input (pin 5) is low, and the output appears

Table 2-4. Key Position Encoding (Half-Effect and Saturable-Core Keyboards)

Pos. No.	Input Pair*	Output Code 6543210	Pos. No.	Input Pair	Output Code 6543210	Pos. No.	Input Pair	Output Code 6543210
1		Not Used	33		Lock	65	7,11	0111011
2	3,6	0001100	34	4,12	0100000	66	7,12	0111100
3	2,8	0000011	35	4,13	0100001	67	7,13	0111101
4	2,9	0000100	36	5,6	0100010	68	8,9	0111110
5	2,10	0000101	37	5,7	0100011	69	8,10	0111111
6	2,11	0000110	38	5,8	0100100	70	8,11	1000000
7	2,12	0000111	39	5,9	0100101	71	8,12	1000001
8	2,13	0001000	40	5,10	0100110	72	8,13	1000010
9	3,4	0001001	41	5,11	0100111	73	9,10	1000011
10	1,3	0001010	42	5,12	0101000	74	9,11	1000100
11	3,5	0001011	43	5,13	0101001	75	9,12	1000101
12	2,7	0000010	44	2,4	0111001	76	2,5	1000110
13	1,4	0001101	45	1,10	0101011	77	2,6	1000111
14	1,5	0001110	46	1,11	0101100	78	9,13	1001000
15	1,6	0001111	47		Control	79	10,11	1001001
16	1,7	0010000	48		Not Used	80	10,13	1001010
17		Not Used	49		Shift	81	11,13	1001011
18	3,8	0010010	50	6,7	0101101	82		Break
19	3,9	0010011	51	1,12	0101110	83	12,13	1001100
20	3,10	0010100	52	6,8	0101111	84	10,12	1001101
21	3,11	0010101	53	6,9	0110000	85		Local
22	3,12	0010110	54	6,10	0110001	86	11,12	1001110
23	3,13	0010111	55	6,11	0110010	87	7,9	0110111
24	4,5	0011000	56	6,12	0110011	88		UC Only
25	4,6	0011001	57	6,13	0110100	89		Not Used
26	4,7	0011010	58	1,13	0110101	90	3,7	0010001
27	4,8	0011011	59	7,8	0110110	91	4,11	0011110
28	4,9	0011100	60		Shift	92		Not Used
29	4,10	0011101	61		Not Used	93		Not Used
30	1,2	0000001	62	2,3	0111000	94		Not Used
31	1,8	0011111	63	1,9	0101010	95		Not Used
32		Control	64	7,10	0111010			

*Numbers refer to pin numbers of MOS integrated circuit.

essentially the same as the strobe input. When keys are operated in more rapid succession, the n-key rollover is accomplished by shortening the length of +KYSTB. This results in presenting characters to the HPRO board more rapidly than before, but still not faster than they can be handled by the terminal microprocessor. The speed at which the microprocessor operates is so much faster than the fastest possible keyboard entry that no useful data is ever lost.

2.10.1.3.2 Repeat Keys. Two qualifications are necessary to provide repeat action (repeat strobes) for a key. First, a special keyswitch module must be installed, and, second, the module's no. 1 output must be connected to pin 1 or pin 2 of the MOS encoder/decoder. Also connected to these pins is a voltage level sensing circuit, the output of which drives the Enable input of the pulse generator IC.

When a repeat-type key is depressed, the initial strobe is produced in the same manner as a normal strobe. However, if the key is held down, its output that is connected to pin 1 or pin 2 of the MOS encoder/decoder does not return all the way to +5 volts, but instead rises to only +4.1 volts. This drives the enable input of the special IC high, and allows it to generate repetitive strobe pulses at a rate of approximately 20 per second. Representative waveforms are shown in Figure 2-38.

2.10.1.4 OUTPUT DRIVERS

The outputs of the seven latches and the strobe output are applied to 7404 hex inverters to provide the standard TTL drive current necessary. Function key output is direct from the keyswitch to the terminal microprocessor input ports, with no intermediate drivers.

2.10.1.5 LOGIC LEVELS

All keyboard interface signals use TTL levels. Keyboard output signals are normally high, and go low when activated. The +KYSTB signal latches the position code into the input port on the HPRO board on its trailing (positive-going) edge.

2.10.2 Saturable-Core Keyboard (Schematic No. 400512-01

The basic construction and operation of all keyboards using the saturable-core keyswitches is the same, although keyswitch complement and layout and keytop engraving may vary. In addition to the contactless, ferrite core keyswitches, the keyboard features MOS encoding and n-key rollover.

2.10.2.1 BASIC OPERATION

This is a scanning keyboard. The Encoder/Decoder/ Processor electronically scans all keyswitches several times per second to see if they are up or down. When a key's status changes from, "up" to "down," the Encoder/ Decoder/Processor outputs a code, representing the key's relative position, onto the data lines, and develops a strobe pulse (+KYSTB). Function key status is loaded into a latch so that "level" signals are available at all times.

Refer to the block diagram in Figure 2-39. An oscillator drives the MOS Encoder/Decoder/Processor with 12.2 μs square waves. This processor sends a different address to the Addressing Logic about every 50 μs.
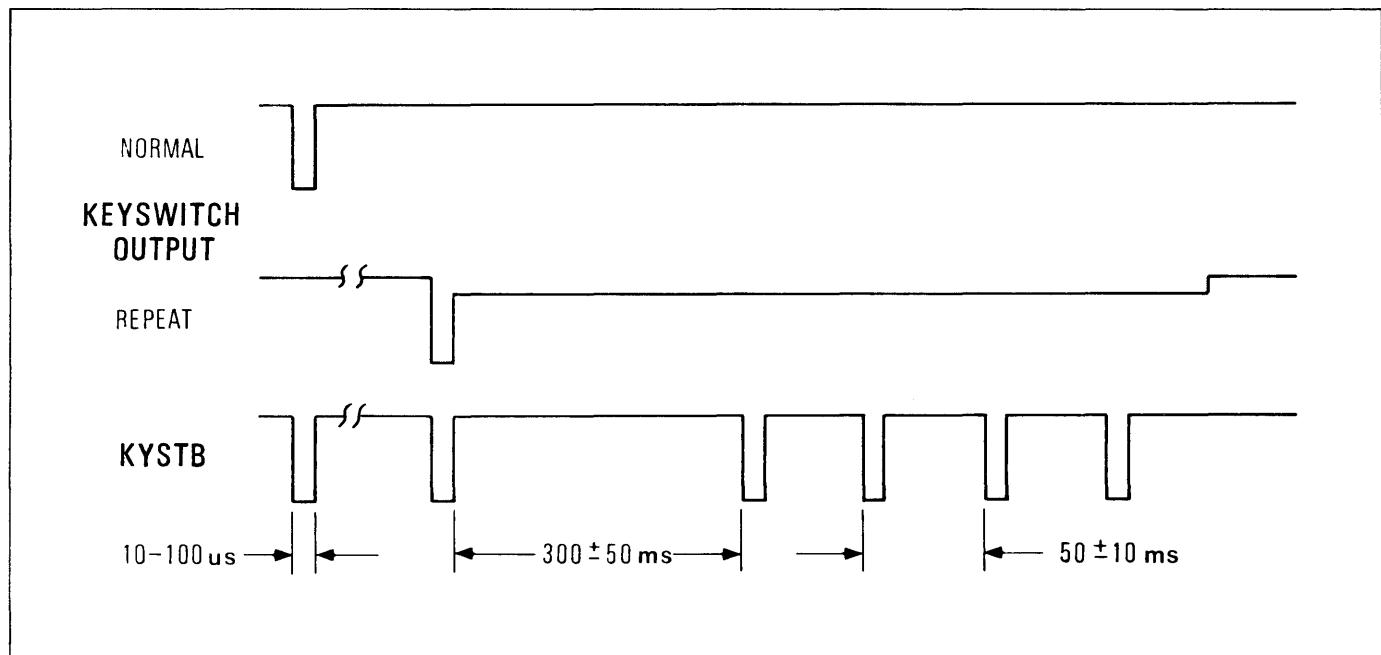
Figure 2-38. Keyboard Strobe Generation

The keyswitches are arranged electrically in an 8 x 16 matrix, providing up to 128 possible key positions. The addressing logic sends a drive pulse down two wires, which intersect at only one keyswitch. If the switch is not depressed, nothing else happens, but if the key is depressed, a signal appears on the sense line. This signal is amplified to become Shift Register IN, SRIN, which is returned to the Encoder/Decoder/Processor to inform it that the key addressed by its present address is down. The decoder portion outputs the position code for this key onto the data bus, and the Strobe Logic develops a pulse on +KYSTB.

On each scan the position of all function keys is set into a latch, providing level outputs for the five FKY signals.

2.10.2.2 KEYSWITCH

The keyswitch is a linear saturable ferrite core with two preformed wires snapped through it. One wire, called the drive wire, is periodically driven by a current pulse. The response to the drive pulse appears, through transformer action, on the second wire called the sense wire. This core module assembly is snapped into the switch housing together with the plunger and return spring. A pair of magnets are located on the plunger so that in the undepressed position the magnets are saturating the core. With the core saturated, signals on the drive wire are not coupled to the sense wire. As the plunger is depressed, the magnets clear the core, bringing it out of saturation and allowing the drive signals to be coupled to the sense wire. These sense signals are amplified to become the SRIN signal.

2.10.2.3 ENCODER/DECODER/PROCESSOR

This integrated circuit is actually a special-purpose microprocessor. It can be logically divided into the following sections:

(a) Timing Section
(b) Count Register Section
(c) Data and Strobe Section

2.10.2.3.1 Timing Section. The input to the timing section is a train of 12.2μs square waves from the oscillator. From this, the timing section generates the main clock signal train which drives the Count Register Section and generates clock phases $\phi 1$, $\phi 2$, and $\phi 3$. $\phi 1$ is the interrogation enable signal. $\phi 2$ (used internally only) loads the data into the data latch and generates the strobe. $\phi 3$ is used by the external electronics for various "housekeeping" functions. A $\phi 4$ signal is also generated externally.

2.10.2.3.2 Scanning Counter. The scanning counter is a 7-bit binary counter which provides the address for the external pROM, part of the addressing logic.

2.10.2.3.3 Data/Strobe Section. This section comprises a 7-bit data latch and a 128-bit shift register. After each key is interrogated, a bit in the shift register corresponding to the key's position on the keyboard is either set or reset, depending upon the keyswitch's status. As each key is interrogated, its status in relation to its status during the previous scan is determined by comparing it with the shift register output. Only when a key's status changes from "up" to "down" will the output latch be loaded (at $\phi 1$) and a strobe generated.
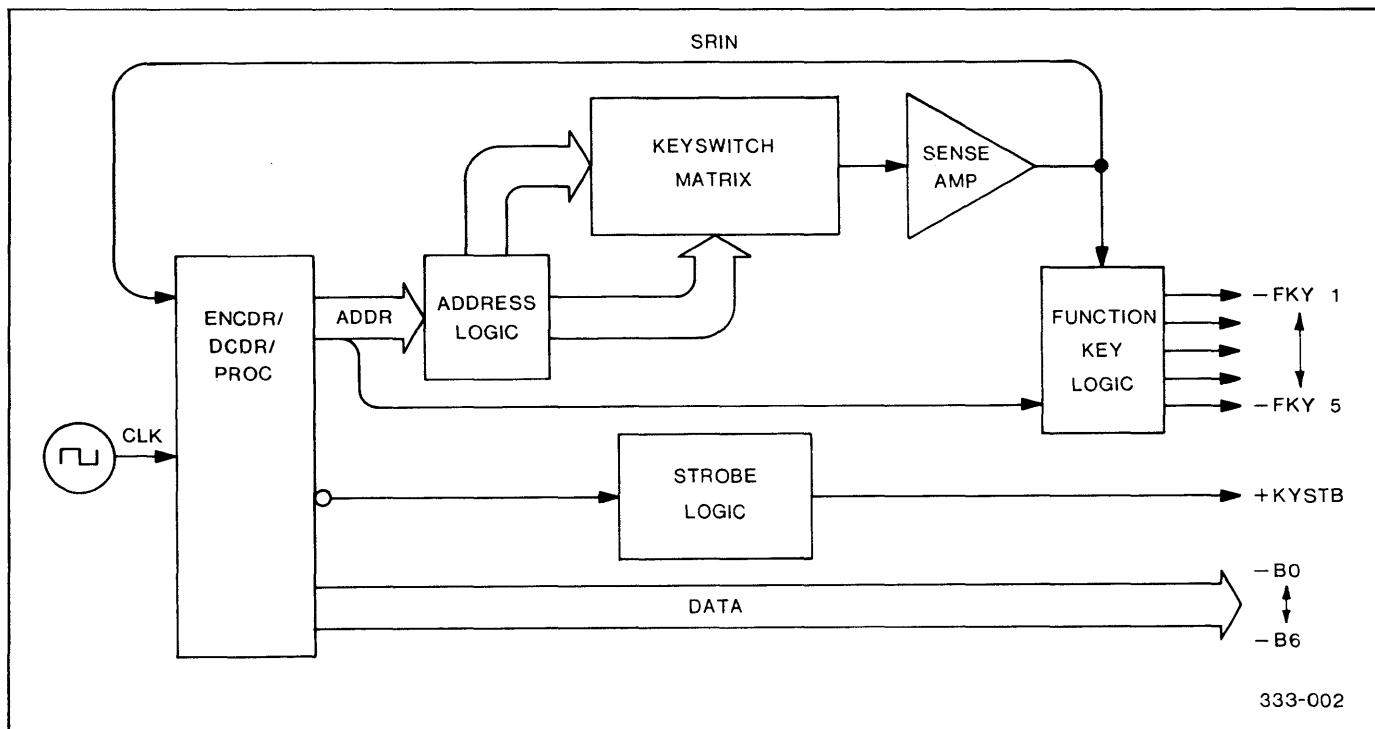
Figure 2-39. Block Diagram, Saturable-Core Keyboard

2.10.2.4 ADDRESS LOGIC

The address logic is made up of a pROM, a 4-bit latch, and three binary-to-decimal decoders.

The pROM is a 256 x 4-bit array, but is used as a 128 x 8-bit array. This is accomplished by addressing one of the low-order 128 bytes (4 bits) first and storing the output in the latch. Then the corresponding byte in the high-order 128 bytes is addressed and the output is used directly. At the moment of key interrogation (ϕ1), the latch outputs are applied to the "X" (sense line) decoder, and the pROM outputs address the "Y" (drive line) decoders. The fourth bit of the latch is used to select one of the two "Y" decoders. The fourth bit of the pROM output (again, at the moment of interrogation) is used to flag "repeat" keys.

Refer to the schematic and to Figure 2-40. Note that the low-order seven bits of the pROM are addressed by the Encoder/Decoder/Processor (the scanning counter). During the early part of the interrogation cycle +ϕ4 is low, allowing the low-order 128 bytes of the pROM to be addressed. The pROM output is loaded into the 4-bit latch when +ϕ3 goes low, and at the next transition of +CLK, +ϕ4 goes high, allowing the high-order 128 bytes of the pROM to be addressed.

The keyswitch matrix sense lines, also referred to as the "X" lines, are continuously driven by the output of the latch. However, to interrogate a particular keyswitch, one of the drive lines, also referred to as the "Y" lines, must also be driven low. The pROM output is applied to both "Y" decoders, and at ϕ1 time one of these decoders (determined by bit no. 1 of the latch) is enabled, causing one of the sixteen drive lines to go low. With one sense line (X) and one drive line (Y) low, one particular key is interrogated.

At the end of ϕ4 time, the Encoder/Decoder/Processor increments the 7-bit address, thus addressing the next
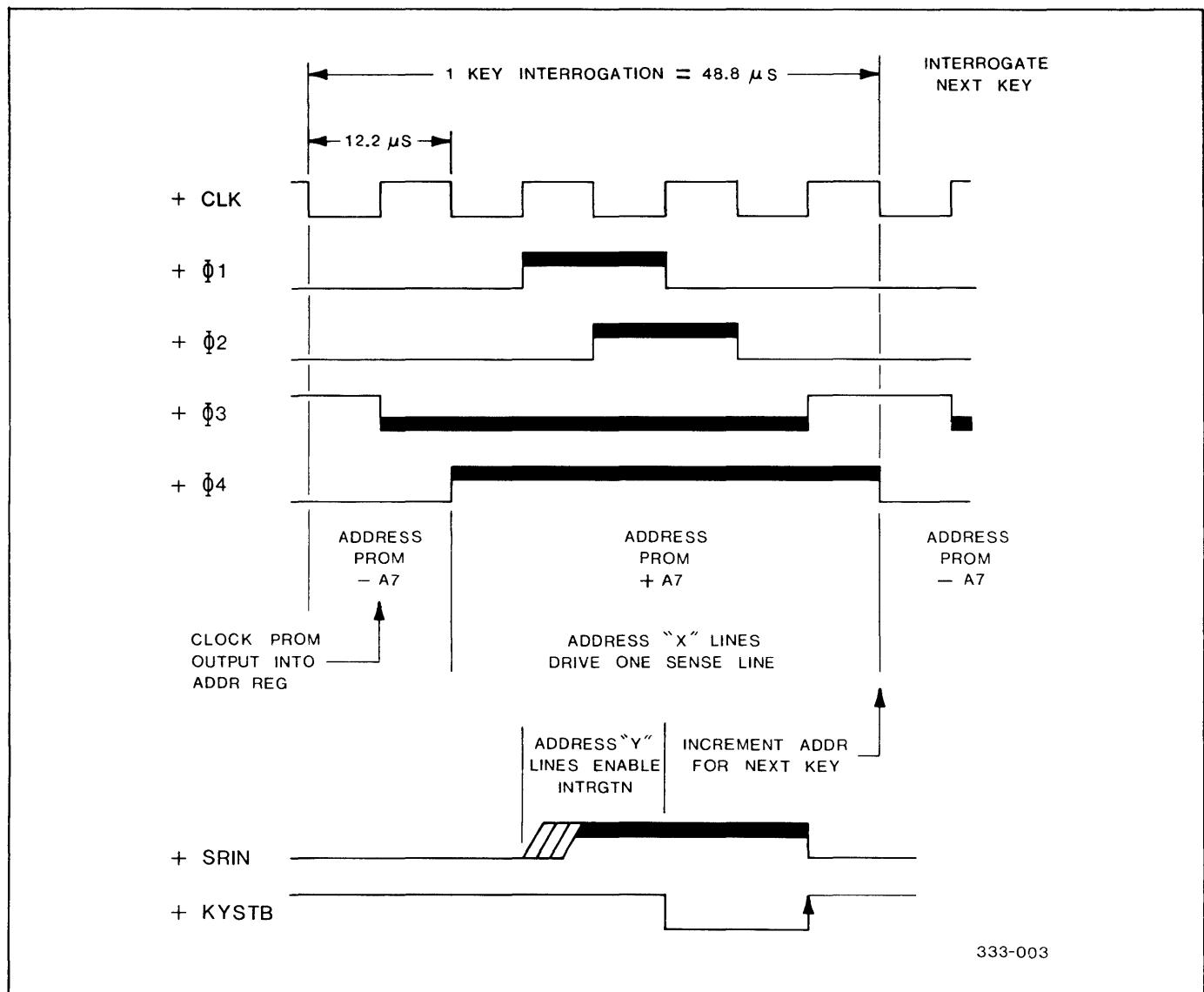
Figure 2-40. Timing Cycle, Cortron Keyboard

location in the pROM and enabling the interrogation of a different key. A new key is interrogated approximately once every 50μs.

When a key is detected as having been depressed, the code placed on the output bit lines by the Encoder/Decoder/Processor is the same as the 7-bit address used to address the pROM (a <u>position</u> code). Thus encoding of keys is accomplished in the pROM: addresses and output codes are incremented sequentially, but keyswitches are actually interrogated as addressed by the pROM. The scanning sequence can jump from key to key in random fashion, but the codes produced by the keyboard on any one scan will be <u>incremental</u>, with the lowest binary value first.

2.10.2.5 KEYSWITCH MATRIX

All keyswitches are arranged electrically into an 8 x 16 matrix. There are eight sense (X) lines and 16 drive (Y) lines. Each sense line passes through a maximum of 16 keyswitch cores, and each drive line through a maximum of 8 cores. (Not all 128 possible keyswitch locations are populated.)

All matrix lines are driven by the same type of ICs, 74145 binary-to-decimal decoders. The X decoder is always enabled (binary 8 input low), so one of its outputs is always low. The Y decoder is enabled by +φ1, when one of the 16 lines is driven low; at -φ1 time, all outputs are high.

All sense lines are terminated in an 8-legged AND gate. This AND gate is normally <u>not</u> satisfied, since <u>one</u> of its inputs is low. Only when a Y line is driven low, and the keyswitch at the intersection of the enabled Y line and the enabled X line is depressed, will the signal on the Y line be coupled to the X line, and the X line will go high to satisfy the AND gate.

At first glance it might seem that this coupling would simply drive the X line <u>more</u> negative. However, by passing the X and Y lines through each keyswitch core in <u>opposite</u> directions, the "low" on the X line is <u>cancelled</u>, instead of being aided. This allows the large AND gate to be satisfied momentarily, producing a positive spike at Test Point A (TPA).

2.10.2.6 SENSE AMPLIFIER

The input signal at TPA, Figure 2-41, is amplified by the transistor at U2-3, 4, and 5 to produce a TTL compatible signal at TPB, also shown in Figure 2-41. This signal is gated with φ1 to set the keyswitch latch and produce the Shift Register IN signal, + SRIN. This signal is returned to the Encoder/Decoder/Processor, where it causes the corresponding bit in the 128-bit shift register to become set.

The SRO output from the Encoder/Decoder/Processor provides hysteresis by controlling the transistor at U2-1, 2, and 3. For example, if a given keyswitch had been depressed on the previous scan, +SRO would be high on the present scan, driving U2-3 lower. This would require a relatively lower signal on U2-4 to provide an output at TPB and +SRIN. On the other hand, after the key has been released and +SRO remains low, U2-3 is slightly higher, requiring a relatively higher signal on U2-4 to trigger the transistor. This hysteresis, plus the fact that the amplitude of the signal on TPA and U2-4 is a function of how far the key is depressed (how close the magnet is to the core), provide effective debouncing in both directions of keyswitch travel.

2.10.2.7 STROBE LOGIC

The normal strobe logic is simple and straightforward; the repeat strobe logic is somewhat more complex. The Encoder/Decoder/Processor produces a low active pulse on its STB output at φ2 time whenever a key's status changes from "up" to "down" (see 2.10.2.3). This signal enables the KYSTB flip-flop, which then sets at the end of φ1 time, driving the +KYSTB signal low. At the end of φ3 time, the flip-flop is cleared and +KYSTB returns high. (The HPRO logic uses the trailing edge of the +KYSTB pulse.)

The balance of the strobe logic is used for repeat key timing. When a key is depressed and held down, the first strobe is generated in the usual manner. Then, after an initial delay of about .3 second, +KYSTB pulses are generated at the rate of about 20 per second.

When a repeat key is addressed, output O4 of the pROM (pin 9) goes high, and if the key is depressed, this output ANDed with +SRIN presets both U20 flip-flops. When U20-9 sets, the preset clamp is removed from U19-4, and the clamp circuit holding the two counter ICs, U21 and U22 clear, is disabled. Counter U22, a binary counter, is incremented at the end of each scan, and it increments counter U21 after every eight scans. U21 is a divide-by-six counter, so its QD output rises after six input pulses, and sets U19-9. The next +φ1 sets the KYSTB flip-flop and generates a pulse on +KYSTB. Thus:

$$6.25 \text{ ms/scan} \times 8 \times 6 = 300 \text{ ms}$$

which is the initial delay after the "normal" strobe and before the first repeat strobe. When +KYSTB is developed, both counters are reset to 0 through gate U18-8.

After the initial strobe, with U19-9 set, a +KYSTB pulse is generated every eight scans: the QA output of U21 is ANDed with U19-9 to set the KYSTB flip-flop. The +KYSTB pulse clears both counters, and the process is repeated as long as the key is held down. Repeat strobes are generated at the rate of approximately one every 50ms (6.25 ms/scan x 8 scans).
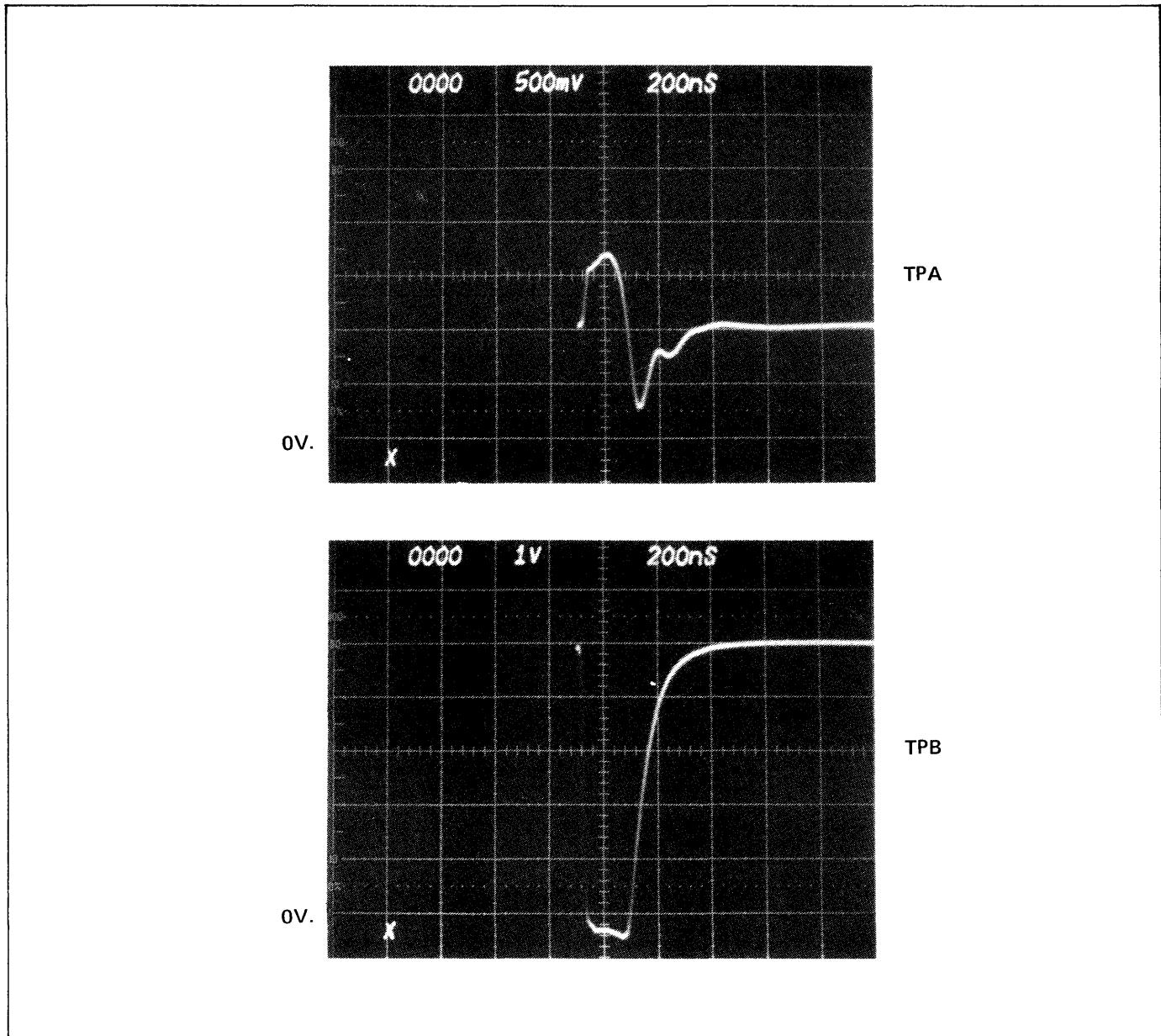
Figure 2-41. Sense Amplifier TPA and TPB

2.10.2.8 FUNCTION KEY LOGIC

Throughout the scan cycle, the status of each key (SRIN) is shifted into Shift Register U11. During all but the very end of the scan cycle, this information is not used. However, when A6 and A7 (U5) are both high during the later portion of the scan cycle, the decoded pROM (U7) outputs address the function keys, which are the last eight keys interrogated (five function keys and three unused positions). At the very end of the scan cycle, when A7 goes low, the contents of U11 are loaded into U12, which provides level outputs.

While A6 and A7 (U5) are high, a low is applied to the input to the Encoder/Decoder/Processor, thus disabling any STB output.

2.11 CONTROL PANEL

Both the Model 1610 (RO) and 1620 (KSR) use the same control panel assembly. However, there are different versions of the assembly, which may be found on any HyTerm. The major difference is in the POWER switch; it is mounted on the control panel on some units, and it is mounted on the bottom cover on others. The control panel that does not include the POWER switch does include a volume control for the audible alarm.

PRIMARY REFERENCED TO COMMON RETURN ◇ ▮ OUTPUT CIRCUIT REFERENCED TO SIGNAL GROUND ⏚

2-44
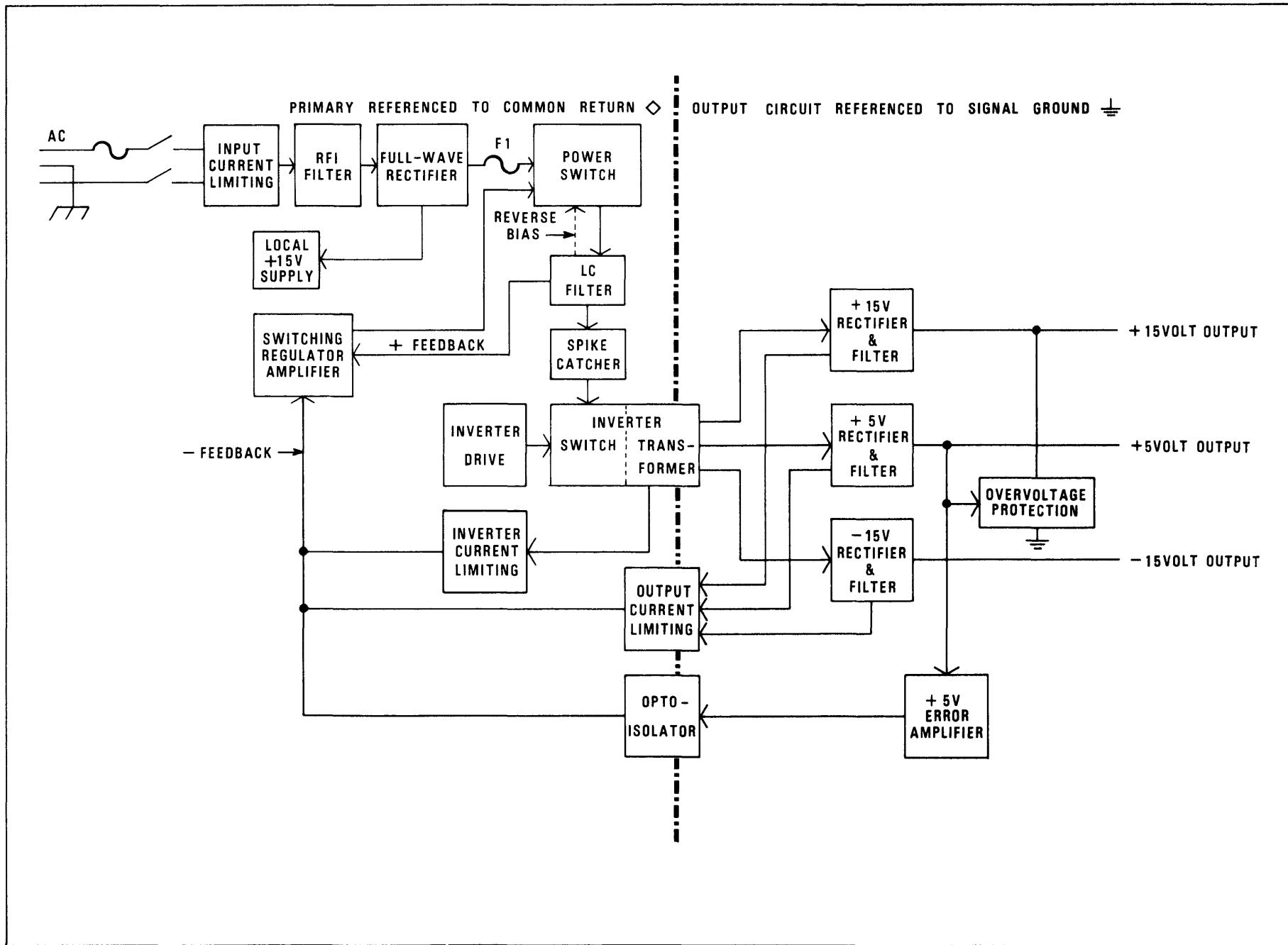
Figure 2-42. Block Diagram, Boschert Power Supply

2.11.1   Switches

The wiring of all switches except the POWER switch is shown on the control panel schematic, no. 23708 for control panels with the attached POWER switch, and no. 23710 for units with the volume control. (POWER switch wiring is shown on the power distribution schematic, no. 23859.) The wipers of all switches are connected to GND, and the NO/NC contacts that are used are connected to +5 volts through a resistor on the HPRO board. Thus all outputs appear high to the input ports on the HPRO board until the respective switch is operated. (Note that the CLEAR switch output, —RESET, does not go to an input port, but drives the 8224 Clock Generator IC directly.)

2.11.2   Form Length Switch

The 12 outputs of the FORM LENGTH switch are encoded into binary format to reduce the number of input lines to the terminal microprocessor. A priority encoder IC is utilized, but there is no priority involved; only one input to the priority encoder is active at any one time.

2.11.3   Audible Alarm

The audible alarm is mounted on the control panel circuit board. It is driven by a peripheral driver IC when the —BELL signal is brought low by the terminal micro-processor. The other side of the audible alarm is returned to +12 volts. When the volume control is used, it is connected between the audible alarm and +12 volts.

2.11.4   Indicators

There are two LED indicators mounted on the control panel circuit board. The POWER indicator is lit whenever the +5 volt supply is energized. The ERROR indicator lights when —ERROR is driven low by the terminal microprocessor.

2.12   POWER SUPPLY

Either of two types of power supplies may be used on the 1610/1620; one is the Boschert and the other is the LHR. Both operate on the principle of switching regulation, using a power transistor/control module assembly as a pulse-width-modulated switch/chopper converter.

2.12.1   Boschert Power Supply Part No. 26021-XX (See Figure 2-42)

The regulated power supply is provided in either of two input voltages, 115 or 220 volts. Variation of input voltage can be ±15% for either supply. Line frequency can be 47 to

63 Hz. An AC line fuse is located inside the machine at the right, and is accessible by removing the access cover. The POWER switch is at the right side of the control panel. There are three regulated output voltages:

+5V @ 4A (8A surge)
+15V @ 4A (10A surge)
-15V @ 4A (10A surge)

Foldback current limiting is provided on all output voltages (11A±2A for 5V, 13A±2A for 15V) as well as on the inverter primary. Overvoltage protection takes over when the +5 volt output reaches approximately 5.6 volts. The primary circuit, which may generate switching transients, is electrically isolated from the secondary (output) circuit.

The power supply operates on the principle of switching regulation, using a power transistor as a pulse-width-modulated switch, controlled by a negative feedback loop from the output circuit. AC line voltage is rectified, chopped, smoothed, inverted at 20 kHz, then finally rectified for output to the terminal circuits. Operation at this frequency, rather than at 60 Hz, permits the use of much smaller, lighter transformers and inductors that dissipate far less heat.

2.12.1.1   GENERAL DESCRIPTION

Refer to the block diagram, Figure 2-42 and the schematic diagram, Drawing No. 26021-xx in the Schematics/Reference Section of this manual. A thermistor in the power supply input line limits power-up inrush of current to charge a large capacitor in the rectifier circuit. An input radio frequency interference (RFI) filter prevents switching transients generated by the power supply from being reflected back onto the AC line. A full-wave bridge rectifier produces approximately 100 volts DC. A portion of the rectifier output is tapped off through a resistance network to supply a local 15-volt regulated power supply that furnishes power to the primary circuit. An internal fuse at the output of the rectifier protects it from catastrophic failure of circuit elements in the primary. Raw DC from the rectifier is applied to a power transistor driven at 20 kHz by a switching regulator amplifier. Chopped DC from the power switch is smoothed in an L/C filter network. A positive feedback loop from the filter to the switch driver maintains self-oscillation. Voltage regulation is imposed by a negative feedback loop from the output circuit. The duty cycle of the power switch is varied in response to the feedback signal, providing more "on" time to increase the average voltage from the L/C filter, less "on" time to decrease the average voltage. Current limiting signals from both the primary circuit and the output circuit are fed back through this same loop.

A "spike catcher" between the L/C filter and the inverter switch suppresses large transients that may be

generated if conduction of the two transistors in the inverter switch overlaps. The inverter switch is two power transistors that are driven at 20 kHz, conducting alternately. The output of the inverter switch is fed to the transformer. Current is fed to each half of the transformer primary alternately in opposite directions. The inverter operates on a 50% duty cycle, producing square waves.

Each output voltage has its own full-wave rectifier and filter circuit. A coil in the toroidal transformer of each output is used to sense current in the circuit. This inductive coupling to the output current limiting circuit serves to isolate the output voltages from the primary side of the power supply, while establishing a feedback loop to the switching regulator amplifier. If current in any output tends to rise excessively, the negative feedback signal causes the switching regulator to decrease the "on" time of the power switch, reducing the average voltage applied to the inverter switch, which results in a reduction of the current through the transformer. The +5 volt output is compared to a reference voltage, and the difference is amplified and applied to the switching regulator amplifier via an opto-isolator, which isolates the output circuit from the primary circuit. The error signal is used to modify the duty cycle of the switch regulator in much the same way as in the current limiting circuit. Coupling between windings in the inverter transformer makes it possible to regulate all outputs by monitoring any one.

Overvoltage protection is provided by a silicon controlled rectifier connected across the +15 volt output. Under normal operating conditions, the SCR presents a very high resistance, but if the regulating circuit fails and a preselected limit is exceeded (nominally 5.6 volts on the +5 volt output), the SCR is fired, placing a short across the +15 volt output. This effectively shorts the entire transformer secondary. Current limiting then takes over automatically to protect the power supply.

2.12.1.2 ISOLATION

The primary circuits of the power supply are electrically isolated from the secondary, or output circuits. Note from the schematic diagram that there is no common ground reference between the primary and secondary circuits. While outputs are returned to the normal signal ground, primary circuits are returned to a "common return," NOT GROUND, indicated by a diamond on the schematic ($\Diamond$). The only interfaces between the primary and secondary circuits are the inverter transformer (inductive), the output current limiter (inductive), and the opto-isolator (optical).

WARNING

Hazardous voltages are present in the primary circuit.

CAUTION

When troubleshooting the primary side of the power supply under power, do not use test instruments having a third-wire ground, or damage to the instrument will result. Make measurements between circuit elements and the primary circuit common return, NOT ground.

2.12.1.3 THEORY OF OPERATION

The following paragraphs present a more detailed description of the operation of the power supply. Refer to the schematic diagram, No. 26021-xx, in the Schematics/Reference Section.

2.12.1.4 INPUT CURRENT LIMITING

When AC power is initially applied, electrolytic filter capacitor C23 demands a high rate of charging current. To protect the diodes in the rectifier, thermistor RT1 is inserted in the line. This thermistor has a negative coefficient of temperature, initially offering a relatively high resistance, then lowering resistance when current passing through it raises the temperature. The initial high resistance limits the charging rate of C23 to a safe level. When the temperature of RT1 rises, the resistance drops to a very low value. The AC ripple component from the rectifier is sufficient to keep the thermistor above the ambient temperature and at a low resistance.

2.12.1.5 INPUT RFI FILTER

Switching power supplies tend to generate sharp transients, which can be reflected onto the power line. The purpose of the RFI filter is to suppress these switching transients. Inductor L1, the RFI filter, has two windings with a common magnetic core. The two windings develop a higher Q and provide better filtering of both sides of the power line than two single inductors.

2.12.1.6 FULL-WAVE BRIDGE RECTIFIER

The full-wave rectifier, consisting of diodes CR1 through CR4 connected in a bridge configuration, converts the off-the-line AC directly into DC. Capacitor C23 provides filtering and storage of the rectified voltage. The cathode of C23 defines the primary circuit common return. Note that the rectifier is returned to the primary circuit common return, NOT to signal ground. Fuse F1, at the output of the rectifier, protects the diodes in the event of a catastrophic failure in the primary circuit. The output of the rectifier is then applied to the power switch, Q1, and to the local +15 volt power supply via a resistor–network.

2.12.1.7 LOCAL +15 VOLT POWER SUPPLY

Transistors Q5 and Q6 are the basic components of the local +15 volt regulated power supply that powers the

switching regulator amplifier IC, U1. Zener diode VR1 and resistors R12, R13, and R14 provide a reference voltage that is compared by Q5 to the sampled voltage. The error signal developed is used to control Q6, the series-pass element, producing the required regulation.

2.12.1.8 POWER SWITCH AND SWITCHING REGULATOR AMPLIFIER

Power transistor Q1, the power switch, is controlled by Type 723 switching regulator amplifier U1, an integrated circuit voltage regulator, through a chain of power-boosting transistors. The switching signal generated within the IC at approximately 20 kHz turns the power switch on and off. Regulation is effected by modifying the duty cycle of the switch in response to feedback signals from the +5 volt output. Low output voltage results in increasing "on" time; high output causes a reduction in "on" time. Modifying the duty cycle raises or lowers the average voltage delivered to the inverter.

The output of U1 is boosted by transistor Q7 to drive complementary Darlington stage Q3. Q3, a PNP transistor, in turn drives Darlington-connected Q2, the immediate driver stage of Q1, the power switch. The 20 kHz chopped DC output from the power switch is applied to an LC filter for smoothing. The switch output signal is fed back to pin 4 of U1 via inductor L2 and resistors R27 and R17 to maintain self-oscillation. To overcome the effect of charge storage, reverse emitter-base bias is injected into the power switch from a secondary winding on inductor L2. The reverse bias signal is applied via a network of resistors R2, R3, and R5, capacitor C5, and diode CR5. The phasing of the secondary of L2 causes a pulse of turn-off bias to be applied to both Q1 and Q2 at the termination of the switch "on" period. Turnoff of the switch becomes regenerative, and is greatly accelerated.

2.12.1.9 LC SMOOTHING FILTER

The regulated, pulsed DC is applied to a filter network made up of inductor L2 and capacitor C10. Diode CR6 maintains output current flow during switch "off" periods by providing a current path to discharge the energy stored in the magnetic field of the inductor during "on" periods. CR6 is reverse-biased when the power switch is "on" to prevent upsetting DC conditions. The smoothed, regulated DC output of the filter is applied to the inverter via a "spike catcher" network.

2.12.1.10 SPIKE CATCHER

The purpose of the spike catcher network, inductor L3, diode CR10, resistors R29 and R48, and capacitor C11, is to suppress large current spikes that can be generated when conduction of the two inverter transistors overlaps. This is not a common occurrence, but can happen during start-up or during recovery from an overload condition. This suppression not only reduces RFI radiation, but also protects the inverter transistors and the power switch

transistor. Diode CR10 is polarized to damp production of counter emf's in L3 should transients occur in the inverter.

2.12.1.11 INVERTER

The smoothed DC input is chopped at 20 kHz by the two power transistors, Q10 and Q11, which conduct alternately, feeding current to the two halves of the non-saturating output transformer T1 in opposite directions. Supporting circuitry consists of a saturating transformer, T2, diodes CR11 through CR15, resistors R29 through R32, and capacitor C12. The transformer is a self-excited type.

2.12.1.12 DC OUTPUT CIRCUITS

Each output has its own full-wave center-tap rectifier and low-pass LC filter. In addition, there are two electrolytic filter capacitors across the entire output from +15 volts to -15 volts. There is a bleeder resistor across the entire output, and one across the +5 volt supply to discharge the capacitors when power is turned off. The filters remove the high-frequency ripple component, mostly 40 kHz, from the output voltages.

The rectifier for the +15 volt supply is made up of transformer T6, diodes CR17 and CR22, and capacitors C35 and C38. Inductor L4 and capacitor C18 provide filtering. The -15 volt supply uses transformer T5, diodes CR18 and CR21, and capacitors C36 and C37. Filtering is provided by inductor L6 and capacitor C20. The +5 volt filter is a pi type consisting of inductor L5 and capacitors C19 and C25. R54 is the +5 volt bleeder resistor. Filter capacitors C32 and C33, and bleeder resistor R51 are connected between the +15 and -15 volt outputs.

2.12.1.13 +5 VOLT ERROR AMPLIFIER

The +5 volt output is sampled by a voltage divider, resistors R43 and R44, and applied to the non-inverting input of Type 723 voltage regulator IC U2 via resistor R41. The adjustable reference voltage is derived from potentiometer R40 and applied to the inverting input of the voltage regulator via resistors R39 and R38. The two voltages are compared within U2, and the difference is applied to the opto-isolator, U3. Only the +5 volt output is adjustable and regulated. The close electro-magnetic coupling in the transformer secondary makes it possible to control all output voltages by controlling any one.

2.12.1.14 OPTO-ISOLATOR

The opto-isolator, U3, consists of a light-emitting diode (LED) and a phototransistor. The output of the error amplifier is applied to the LED, illuminating it in proportion to the error. The optical energy is read by the phototransistor, which has no electrical connection to its base. The output of the phototransistor is fed back through resistor R33 to the switching regulator amplifier, U1, where the signal is used to modify the duty cycle of the power switch, regulating the voltage. Since there is no direct electrical connection through the Opto-Isolator, and the photo-

transistor output is returned to the primary circuit common return, the output circuit is effectively isolated from the primary.

2.12.1.15 OUTPUT CURRENT LIMITING SENSE AMPLIFIER

Current in a winding of a toroidal transformer in each output is monitored and fed back to the switching regulator amplifier to modify the switch duty cycle. Resistor R58 is connected across a winding of transformer T4 in the +5 volt circuit. Current through the transformer develops a voltage drop across the resistor. Transistors Q14 and Q15 sense and amplify the voltage drop. In the -15 volt supply, resistor R59 is across the winding of T5, and transistors Q16 and Q17 are the sense amplifiers. In the +15 volt output, the circuit elements are transformer T6, resistor R60, and transistors Q18 and Q19. The collectors of all the transistors are connected to the base of transistor Q13 through resistor R70. Q13 amplifies the error signal, which can originate in any of the outputs, and applies it to the switching regulator amplifier along with the voltage regulation feedback signal. As current increases, the duty cycle of the switch regulator, and of the power switch, is modified

to reduce switch "on" time, reducing the average voltage applied to the inverter, limiting current through the inverter transformer. A shorted output will reduce current to a very low level that can be tolerated indefinitely.

2.12.1.16 OVERVOLTAGE PROTECTION

Overvoltage protection is provided primarily to protect the loads in the event of failure of the regulating circuit. Silicon controlled rectifier SCR1 is connected across the +15 volt output. The gate circuit of SCR1 monitors the +5 volt output through zener diode VR2, which has a 5.6 volt breakdown rating. If the +5 volt supply exceeds the zener breakdown voltage, the diode conducts, firing SCR2, which places a direct short across the +15 volt output. In effect, this "crowbars" all outputs because of the close coupling of the inverter transformer secondary. To protect the power supply, the current limiting circuit takes over, reducing the power switch output to a safe level. Once fired, the SCR will continue conducting until power is turned off. When the condition causing the overvolt condition is corrected and power is applied, the overvolt protect circuit is automatically restored to normal.

(083 - 013)
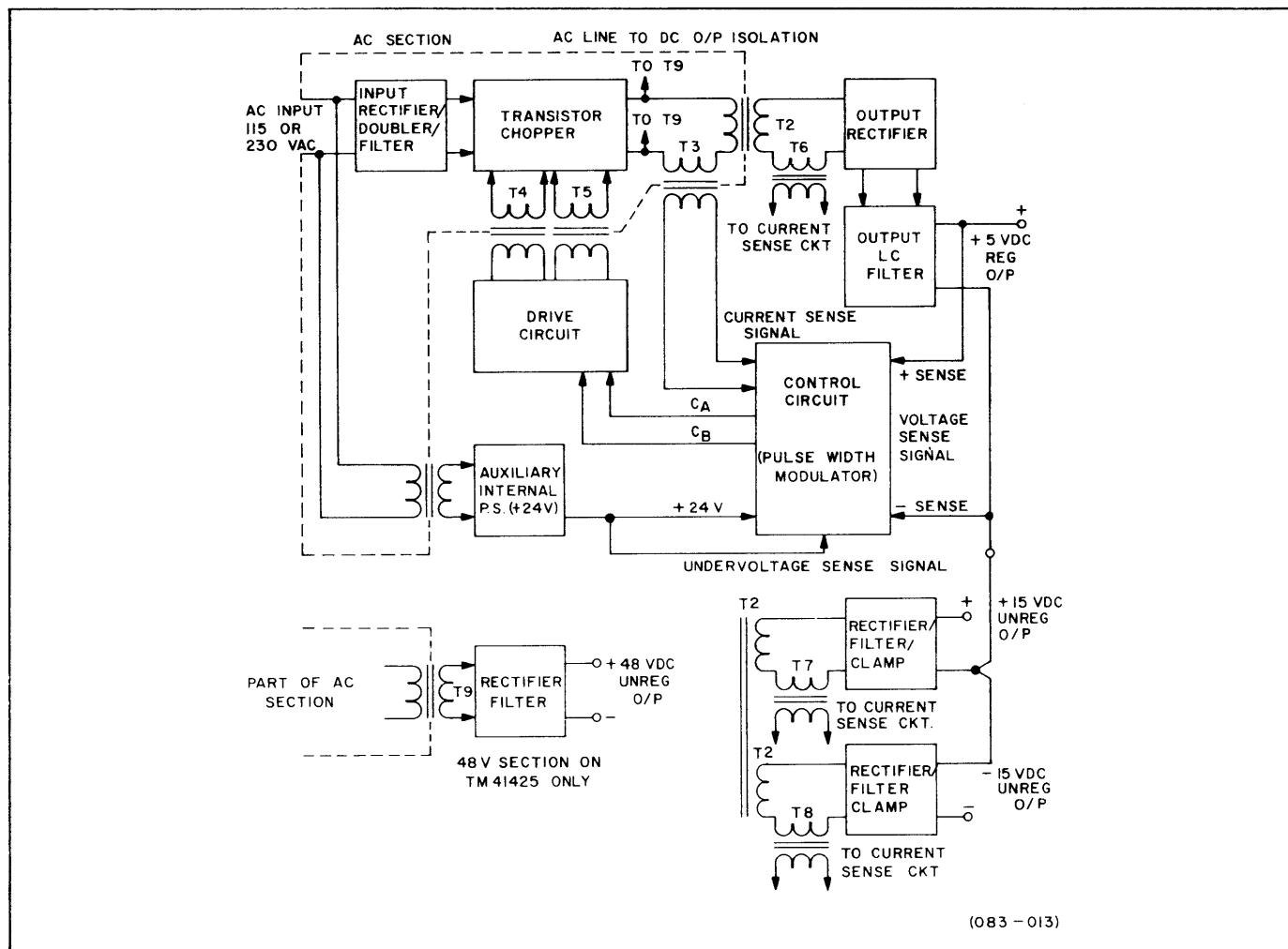
Figure 2-43. Block Diagram, LHR Power Supply

2.12.2 LHR Power Supply, Part No. 400062-01 (See Figure 2-43)

The main output of the Switching Power Supply is a pulse-width modulated chopper converter. The ac input is rectified, doubled and filtered to 300Vdc and then chopped and transformed to a lower voltage by a half-bridge. This transformer secondary output (consisting of a quasi-square wave) is rectified and filtered to the final dc output value.

The output is sensed and the error signal voltage is amplified and used to control the pulse width of the chopper, thus regulating the output voltage within narrow limits under all conditions of the input line and the output load. The output and all control circuitry are isolated from the ac input line.

This power supply has input undervoltage sense, soft start control, output current limiting, output overvoltage protection and crowbar on the +5V. The unregulated ±15V outputs have current limiting circuits and overvoltage clamps.

2.12.2.1 DETAILED DESCRIPTION (See Schematic 400062-XX)

2.12.2.1.1 Input Filter. The input filter consists of L1, C1, and C2, that form an RF noise suppression filter. R1
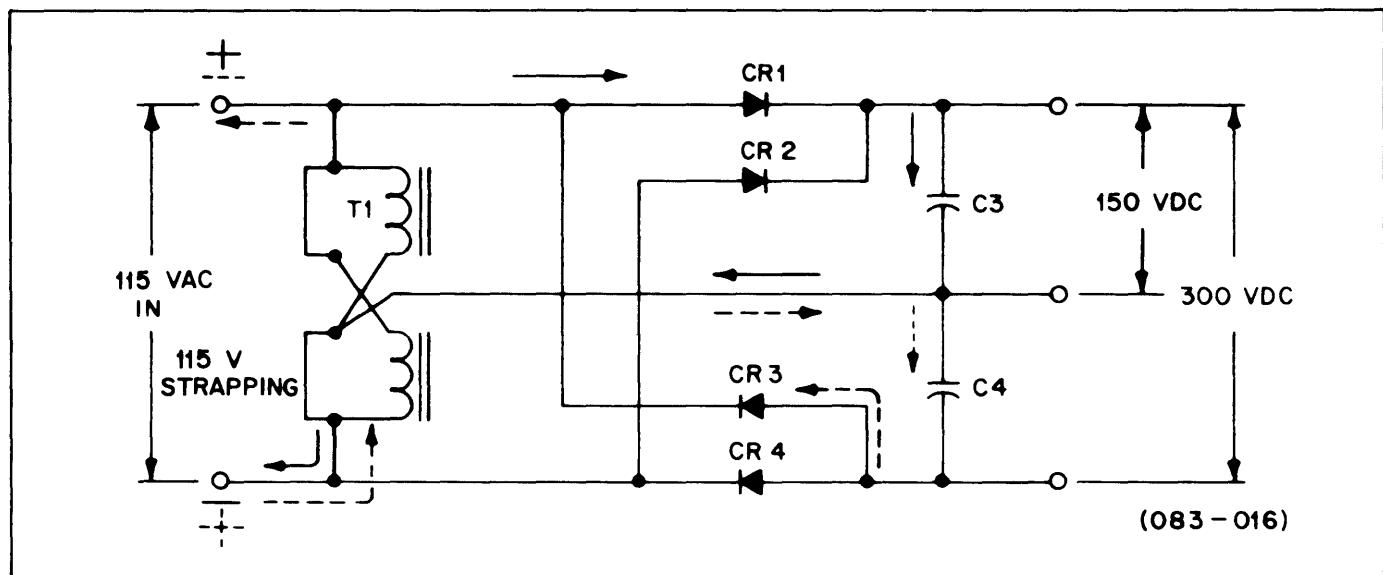
Figure 2-44. LHR Simplified Input Rectifier/Filter Doubler Section
(115 VAC Input Strapping)
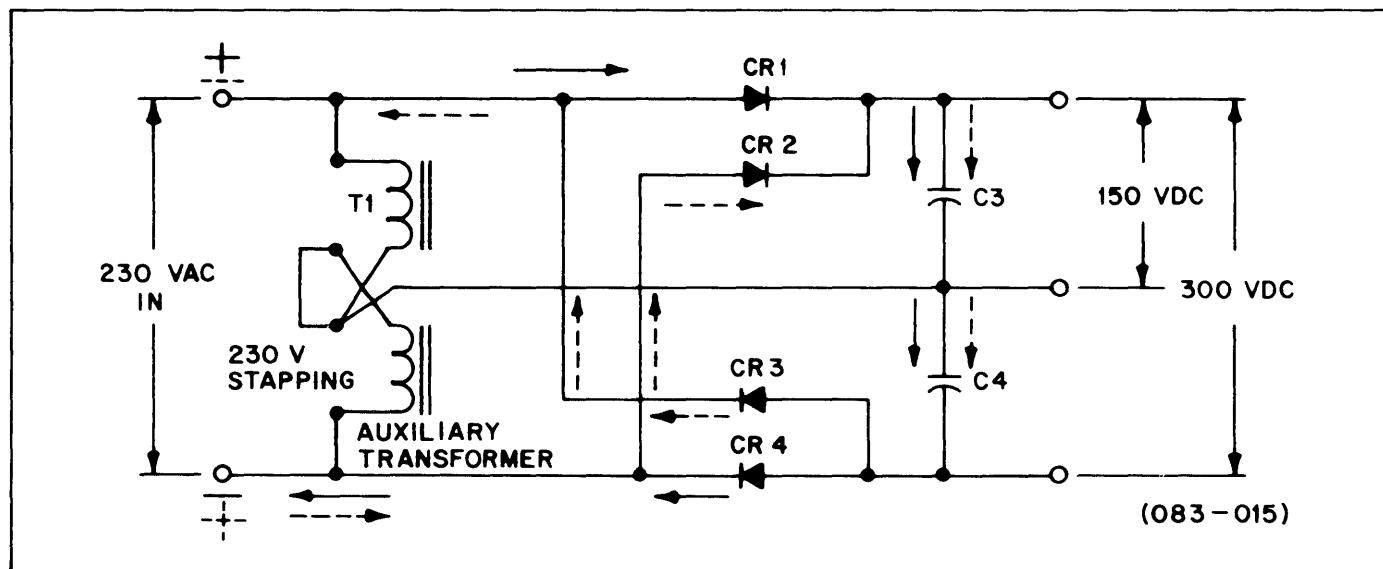
Figure 2-45. LHR Simplified Input Rectifier/Filter Doubler Section
(230 VAC Input Strapping)

and R2 are thermistors with a high resistance at low temperature. The thermistors limit the input start-up current. The filter operation, including polarity and current flow is described by Figures 2-44 and 2-45. The strapping connections at T2 allow the use of the same assembly for 115 or 230 Vac input. R3 and R4 are the bleeder resistors.

2.12.2.1.2   Chopper Section (See Figures 2-46 and 2-47).   Transistors Q1 and Q2 are alternately turned on and off at a 20 kHz rate. C7 is a balance capacitor and T3 is a current sensing transformer. R5 and C8 form a primary RC snubber to attenuate voltage overshoots. CR7 and CR8 prevent reverse conduction of Q1 and Q2 during transient conditions. The switching action of Q1 and Q2 applies a quasi-square voltage waveform of 300 volts peak-to-peak to the primary of T2.

2.12.2.1.3   Output Rectifier and Filter (See Figure 2-47).   The quasi-square voltage waveform is transformed down by T2. The output is rectified by BR1 and filtered by an LC filter, consisting of L2, C15, C30, and C31. Ripple and RFI are further reduced by C16 and C17. C9 and R25 form a secondary snubber network.

2.12.2.1.4   Internal Auxiliary Power Supply.   Transformer T1 transforms the 115 or 230 Vac line voltage to supply unregulated +24 Vac to the control circuit. CR13, CR14, CR15, and CR16 form a full bridge rectifier and C10 filters the output.

2.12.2.1.5   Control Circuitry.   The control module assembly contains a pulse-width-modulator, IC SG3524, (see Figures 2-48 and 2-49) and provides all the basic control functions as follows:

1.   Voltage Amplifier and Reference
2.   Overvoltage Protection
3.   Undervoltage Protection
4.   Soft Start
5.   Remote On/Off (not used)
6.   Power Fail
7.   Current Limit

The adjustments on the control module assembly are factory set, and it should not normally be necessary to readjust the factory settings.

Table 2-5 defines the voltage/current levels at nominal line and load conditions.

2.12.1.1.6   Chopper Drivers.   Drive to the bridge transistors Q1 and Q2 is provided by two pair of push-pull current source drivers Q3, Q4, Q5, and Q6. Q4 and Q5 bases are held at a 5.1V level. Q3 and Q6 are alternately turned on by C_A and C_B. C_A and C_B levels are clamped at 5.7V by CR19 and CR20 (see Figure 2-47). Transformers T4 and T5 couple drive signals to the base of Q1 and Q4. The snubbers consists of R11, C11, R16 and C13. Resistors R12 and R17 control the drive current.
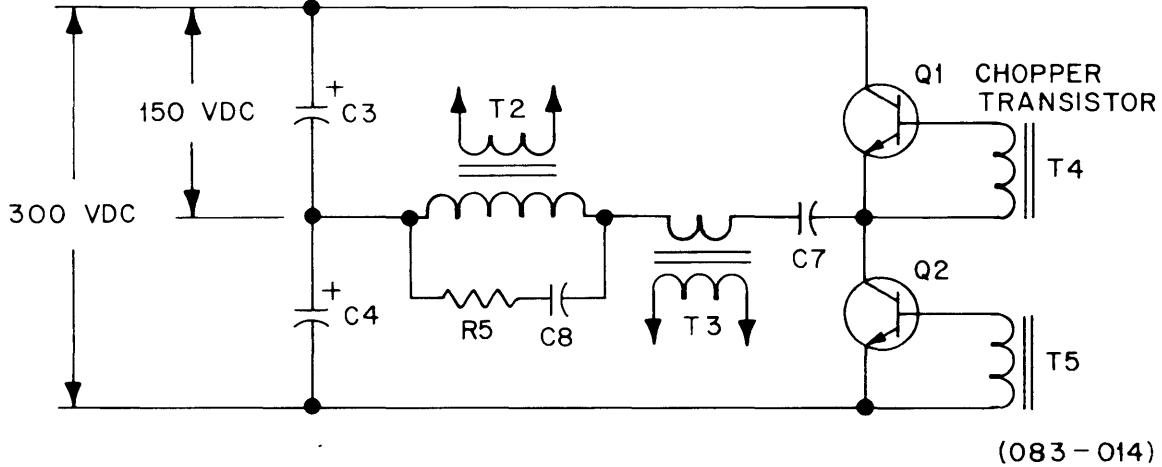
Figure 2-46. LHR Simplified Transistor Chopper (Half-Wave)
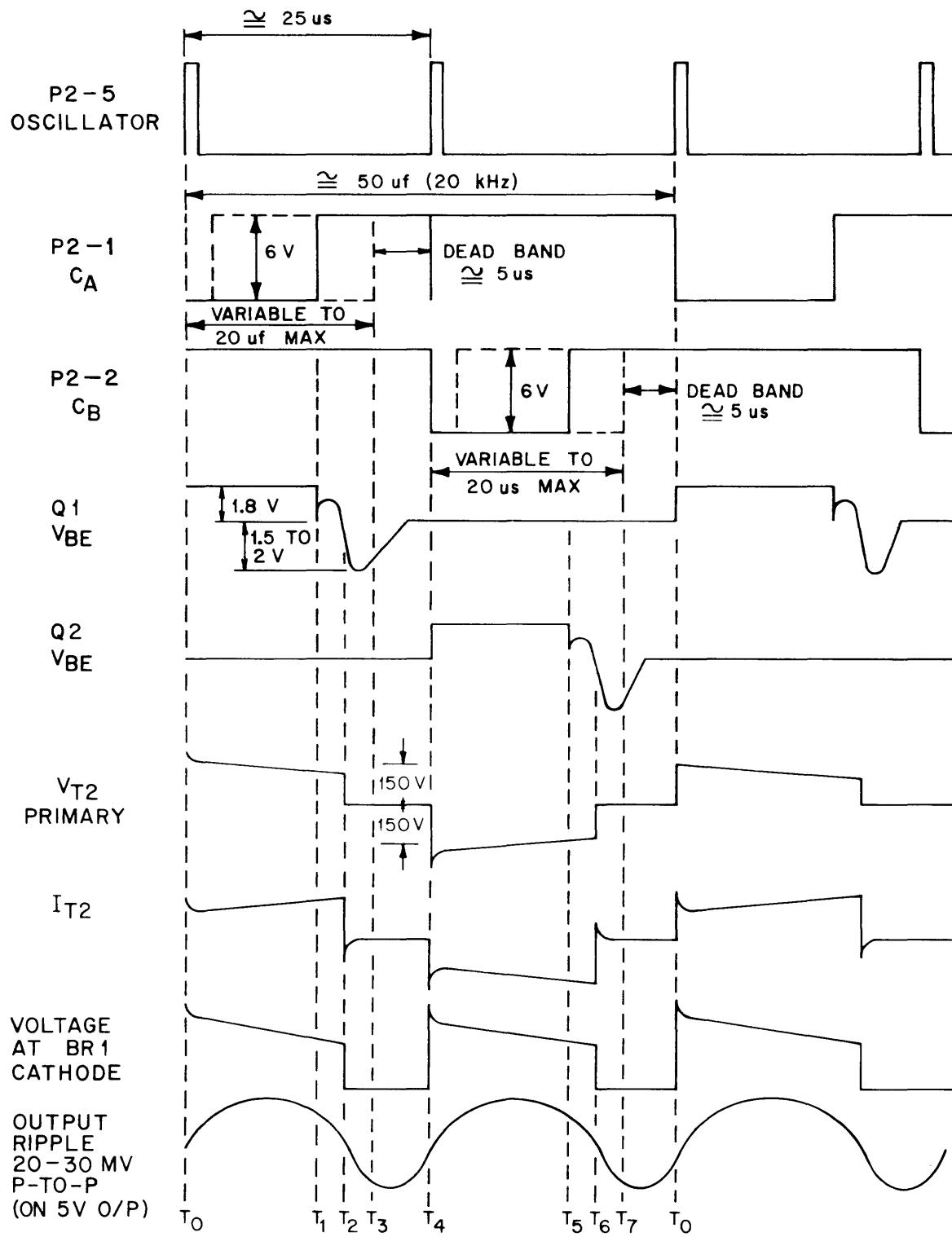
Figure 2-47. LHR Power Supply Waveforms

(083-017)
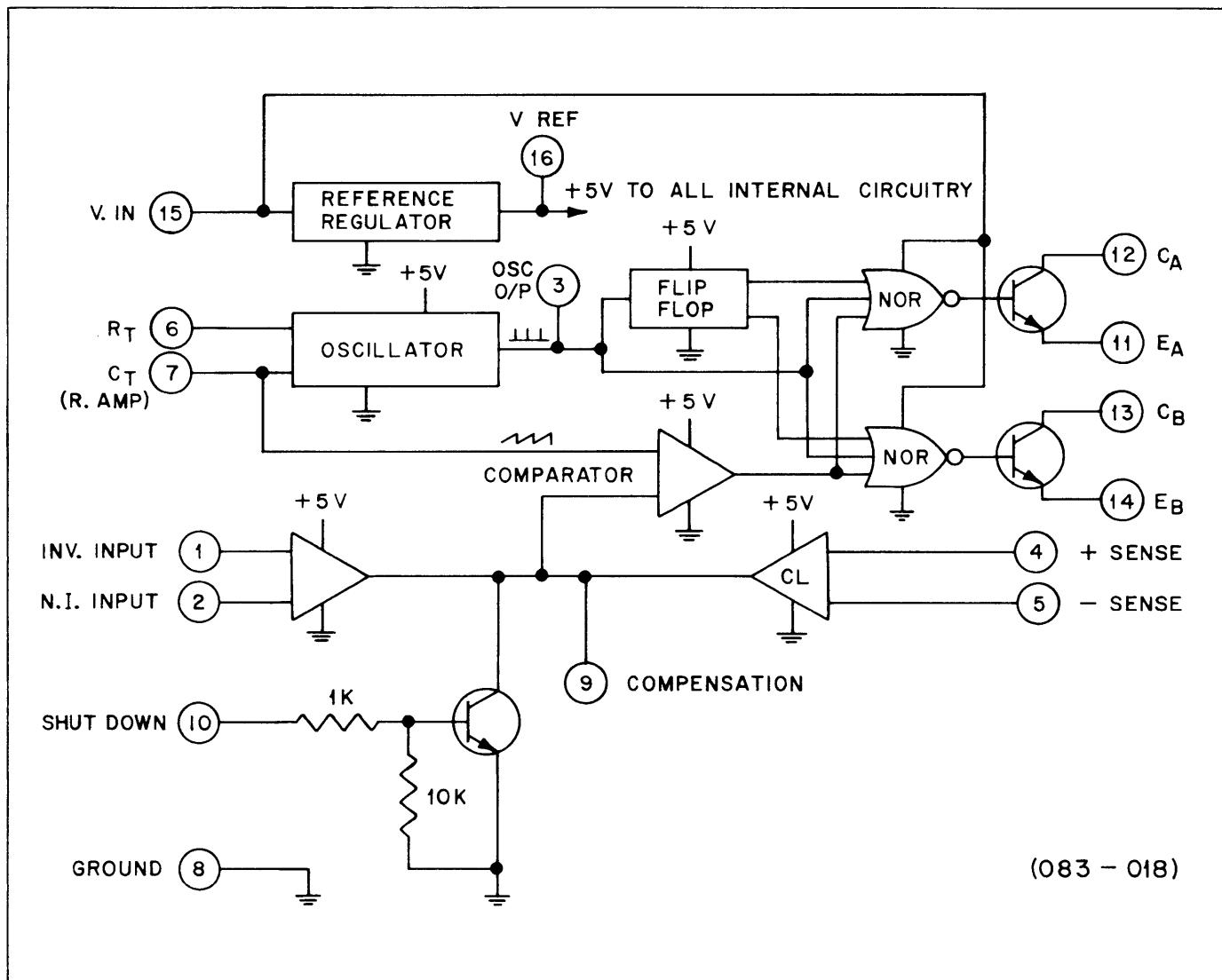
Figure 2-48. LHR Control Module Block Diagram
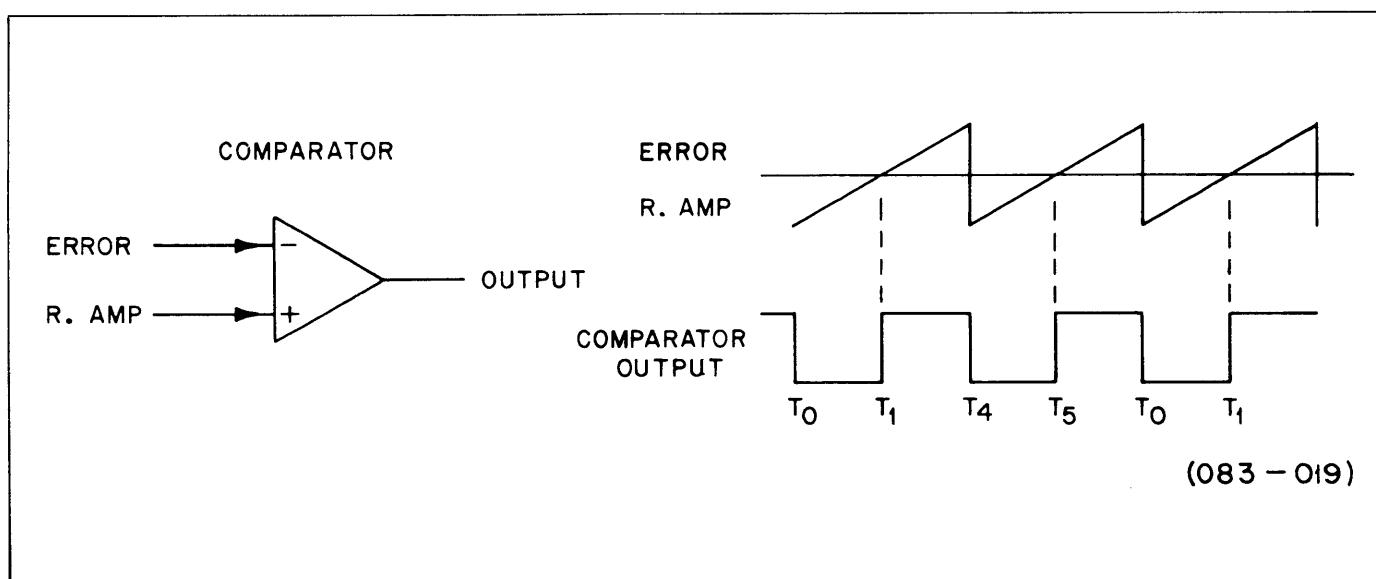
Figure 2-49. LHR Control Module Timing Diagram (SG3524)

Table 2-5. Voltage/Current Levels

Pin	Function	Measurement	Pin	Function	Measurement
P1-1	OVP	2.3V	P2-1	C_A	See Fig. 2-47
P1-2	Current Limit	Square Wave, 1.4V Peak	P2-1	C_B	See Fig. 2-47
			P3-3	Power Fail	3.5-5V dc
P1-3	Current Limit	.5-.6V dc	P2-4	-Sense	0
P1-4	Remote On/Off	1-4V dc	P2-5	OSC out	See Fig. 2-47
			P2-6	+Sense Divider	2.2-2.8V dc
P1-5	UVS	12-18V dc			
P1-6	+24V Input	22-25V dc	P2-7	R_T	
P1-7	Current Lim Bias	.5-.7V dc	P2-8	Common	0

Note: All measurements are made with respect to pins P2-4 or P2-8.

2.12.1.1.7 The +5V Main Output Crowbar. Components CR34, R29, R28 and SCR1 form an overvoltage crowbar circuit. If the +5V regulated output goes above 6.3V, the SCR1 fires and keeps the output low. The power supply must be turned off to re-start after the overvoltage condition has been removed.

2.12.1.1.8 Secondary Current Limiting Circuitry. Transformer T6, R27, and CR22 through CR25 are part of the secondary current limit circuit.

2.12.1.1.9 The ±15V Unregulated Outputs. The +15V and the -15V unregulated circuits are identical. Only the +15V unregulated circuit will be described. The quasi-square voltage waveform is transformed down by T2, rectified by BR2 and filtered by L3 and C20. C21 is an RFI suppression capacitor. R31 and C29 form an RC snubber to suppress overshoot. T7, R30, and CR26 through CR29 are part of the +15V current limit circuit.

2.12.1.1.10 The ±15V Overvoltage Limit. The +15V and the -15V overvoltage limit circuits are identical. Only the +15V circuit will be described. Components R36, CR35, CR36, and R37 are a biasing network to turn on Q7, when the output voltage is greater than 17 volts. The circuit limits the no load output voltage to 17 volts.

2.12.1.1.11 The +48V Unregulated Output. (Not used in 1610/1620.) The primary of transformer T9 is paralled with the primary of transformer T2. The quasi-square voltage waveform is transformed down by T9, rectified by BR4 and filtered by L5 and C27. R34 preloads the output to help limit the no load voltage. The +48 volt output does not have current limit.

3.1 INTRODUCTION

Maintenance of the HyTerm is generally divided into two broad categories: (1) module/subassembly removal, replacement, and adjustments; and (2) detailed trouble-shooting and repair of circuit boards. Since some trouble-shooting is also involved in locating the faulty module before it can be replaced, there is no clear-cut dividing line between these categories, and overlap will occur in many areas.

This section is generally divided so that those performing module replacement will use the next three sub-headings, (3.2) PREVENTIVE MAINTENANCE, (3.3) MODULE REPLACEMENT, and (3.4) ADJUSTMENTS. The remainder of this section contains component location/identification information that will be useful in trouble-shooting.

NOTE

Preventive Maintenance, when performed according to the procedures listed here, will not affect the Diablo warranty. However, any module replacement or adjustment unsuccessfully attempted will render the warranty null and void. All time and material required to restore the HyTerm to working order will be billed at the prevailing rates.

3.1.1 General Rules

There are a few general rules that should always be observed:

(1) Never remove or install any circuit boards, or connect or disconnect any plugs, while power is on.

(2) Applying power to the HyTerm initiates a printer Restore sequence, which includes carriage movement. Make sure the carriage is free to move to the left before applying power.

(3) Whenever the access cover is removed, be careful not to brush against the cover-open switch: operating this switch could allow the carriage to move suddenly, which could cause an injury. When operating the HyTerm with the access cover removed (and the cover-open switch in the "override" position), keep fingers, hair, etc., away from the printer.

(4) Never remove the top cover without first disconnecting the power cord from the wall outlet.

(5) When tipping the HyTerm up to gain access to its underside, first position the power cord and the EIA cable to the sides so they will not be in the way. Make sure the surface behind the HyTerm is flat and free of any foreign objects. Then tip the HyTerm up approximately 70 degrees so that it balances on the rear edge of its bottom cover. Do not allow the table surface or any objects to apply pressure to the finned heat sinks on the rear; since these heat sinks are mounted on the power amplifier boards, any pressure could damage the circuit boards or the mother board and its connectors. Also, while the HyTerm is tilted up in this manner, hold onto it with one hand to prevent it from failing.

(6) Do not use alcohol to clean the platen, the paper feed rollers, or any other rubber parts. Alcohol dries out the rubber and hardens it, eventually resulting in paper feed problems. Use "Fedron Platen Cleaner" or its equivalent.

CAUTION

Fedron Platen Cleaner and similar products are flammable, and have a very low flash point.

(7) Take care not to touch plastic parts with platen cleaner. These products are usually harmful to plastics. Use alcohol to clean plastic parts.

3.1.2 Top Cover Removal

Removal of the top cover is a prerequisite to most HyTerm maintenance procedures. It is relatively easy, but slightly more difficult on HyTerms having the control panel mounted to the top cover; on these units, have the HyTerm adjacent to a table or other work surface on which the cover can be placed after it is removed, since it will still be connected to the HyTerm by its cables. Proceed as follows:

(1) Unplug the power cord from the wall.

(2) Raise or remove the access cover. Remove the plastic skirts over the ends of the platen shaft, if so equipped.

(3) Remove the platen: grasp the platen knobs in both hands, press down the platen latches with your thumbs, and lift the platen straight up.

(4) Release the top cover by pulling forward on the two latches inside the cover at the sides, just in front of the platen. Lift the cover straight up.

(5) If the control panel is not mounted to the cover, set the cover aside. If the cover has the control panel attached, hold the cover in one hand while removing the ribbon cables from their cable clamps to provide more cable length. (Note the routing of the cables for later replacement.) Then set the cover down next to the HyTerm. The HyTerm can be operated in this condition, but if the power cord is plugged in with the top cover removed, stay away from the power switch terminals, which have line voltage present on them.

3.2 MAINTENANCE PROCEDURES

The maintenance procedures described below are divided into three levels. The first level is preventive maintenance and may be accomplished by any user. The second level is corrective maintenance involving on-site exchange of printed circuit boards and subassemblies, and minor adjustments. The third level, also corrective in nature, involves depot and/or factory repair or refurbishment of assemblies and printed circuit boards.

Levels 2 and 3 are warranty and post-warranty periods in the maintenance of the machine. As long as the 1610/1620 terminal's warranty remains in force, maintenance by the user will be limited to Level 1 Procedures. Diablo Customer Service should be contacted for assistance with more serious problems.

NOTE

The Diablo warranty is null and void when a Level 2 or 3 procedure has been unsuccessfully attempted. All time and material required to restore the terminal to working order will be billed at prevailing rates. No adjustments should be attempted unless equipment malfunction indicates a specific need.

3.2.1 Supplies

The following supplies are necessary for proper preventive/corrective maintenance (numbers are Diablo part numbers):

Level 1: Ribbon cartridge and printwheel change; surface cleaning and lubrication; adjustment of print impression and platen position controls; and minor assembly exchanges of platens and paper cradle.

(1) Fedron Platen Cleaner, or equivalent.
(2) Diablo #70243 light oil, Shell Turbo 27, or equiv. (2 drops/app.)
(3) Diablo #70364 Polyoil (light white grease)
(4) Diablo #70825 Multipurpose grease 2 oz. tube
(5) Diablo #99000-01 Alcohol Pads (91% Isopropyl alcohol) or equiv.
(6) Lint free wipers
(7) Clean, low pressure compressed air (optional)
(8) Diablo #70870-01 Permabond 240TM adhesive 1 oz. (printwheel home sensor tab only)
(9) Diablo #70847-01 Vibratite TM adhesive, 8cc (all

locations required other than printwheel home sensor tab).

CAUTION

1. Do NOT use alcohol on rubber items.
2. Do NOT use platen cleaners on plastic items.
3. Platen cleaners are flammable, and have a very low flash point, so use with care.
4. Observe OSHA safety rules for use of compressed air, including safety goggles.

Level 2: Level 1 items, plus unit replacement, circuit board exchange, subassembly replacement, and minor adjustments and alignments.

(1) One set of circuit boards
(2) Keyboard assembly (appropriate type)
(3) Power Supply
(4) Control Panel assembly, no. 23710
(5) One Platen (appropriate type)
(6) One Carriage assembly
(7) One Carrier assembly, complete with paper feed motor
(8) One Carriage Drive Motor
(9) One Carriage Drive Cable assembly
(10) One Forms Tractor assembly, if appropriate
(11) Assortment of hand tools adequate for electronic/mechanical repair, including a T-handle spring tool (Diablo #99009) and a long nose self-locking clamp (Hemostat, Diablo #16424)
(12) TORX ® Driver Bit #T15 no. 70826-01
     Tools Driver Bit #T9 no. 70826-02
           Screwdriver #T15 no. 70826-03
           Screwdriver #T9 no. 70826-04
           Key Wrench #T15 no. 70826-05
           Key Wrench #T9 no. 70826-06
(13) Connector Extractor, 3M #3438, no. 70832
(14) Combination Adjustment Tools no. 40795 or 40795-01, and 40796
(15) Tensiometer, Electromatic Equipment Co. Model DXX-IKD or equivalent, calibrated for Diablo cable
(16) Cable ties, no. 10538-01
(17) Thermal compound, no. 10549

Level 3: Level 1 and 2 items, plus major disassembly and refurbishment of subassemblies, and repair of circuit boards.

(1) One Circuit Board Extender assembly, no. 40539-03
(2) One Carriage Motor Extender Cable assembly, no. 40667
(3) One Transducer Extender Cable assembly, no. 40666
(4) One Printwheel Motor
(5) One Paper Feed Motor
(6) Oscilloscope, vbw 15MHz, vds 100 mV/cm, sweep speed 50ns/cm

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TORX® is a registered trademark of Camcar Screw & Mfg.

3.2.2 Cleaning and Inspection

It is difficult to state specific rules concerning the frequency of preventive maintenance inspections, because of differences in the hours of usage and other environmental considerations from one machine to another. It is recommended, therefore, that the following preventive maintenance procedure be performed at least every 500 hours of printing time, or every six months, whichever occurs first:

(1) Remove power from the terminal. Raise the access cover and remove the top cover as noted in Section 3.1.2.

(2) Inspect the printer for signs of wear and loose or broken hardware. Check carriage cable for signs of wear, and cable pulleys for loose bearings. Check platen for looseness or wobble. Check platen drive gears for looseness. Check the carriage for looseness, wobble, or accumulations of foreign material on the rails which might cause uneven movement of the carriage.

(3) Remove the platen, paper cradle, ribbon cartridge, and printwheel. Inspect for signs of wear.

(4) Clean the printer thoroughly, using alcohol saturated cleaning pads, and wipers. Remove accumulations of paper residue, ink, dust, etc., with special attention to the carriage rails and pulley grooves. Heavy deposits may be first removed by blowing with compressed air. Be sure to observe all safety precautions when using compressed air.

NOTE

Use of compressed air is NOT recommended when the terminal is located close to other equipment that is sensitive to dirt and dust.

(5) Clean the platen, paper bail tires, and paper feed rollers with a good platen cleaner which is non-injurious to rubber products, such as "Fedron Platen Cleaner." Do NOT use alcohol.

(6)* Clean the rest of the HyTerm as required—remove all dust and foreign material.

(7)* Inspect the entire machine for loose hardware and frayed wires or cables.

(8)* Check to be certain that the fan is operating.

(9) Check all power supply voltages (see 3.4.3).

Items above marked with an asterisk (*) should be checked on every machine visit, not only at the P.M. inspection.

3.2.3 Lubrication

Lubricate the various parts of the cleaned and inspected printer according to the following schedule. DO NOT exceed this schedule. Too much lubricant is often worse than none at all!

(To be done every six months or if printer has not been used for more than a week.)

3.2.3.1 CARRIER SYSTEM (Figure 3-1)

(1) Paper Feed Roller Shaft Pins (A) — Lightly grease the 8 pressure roller shaft pins with No. 70825-01 grease.
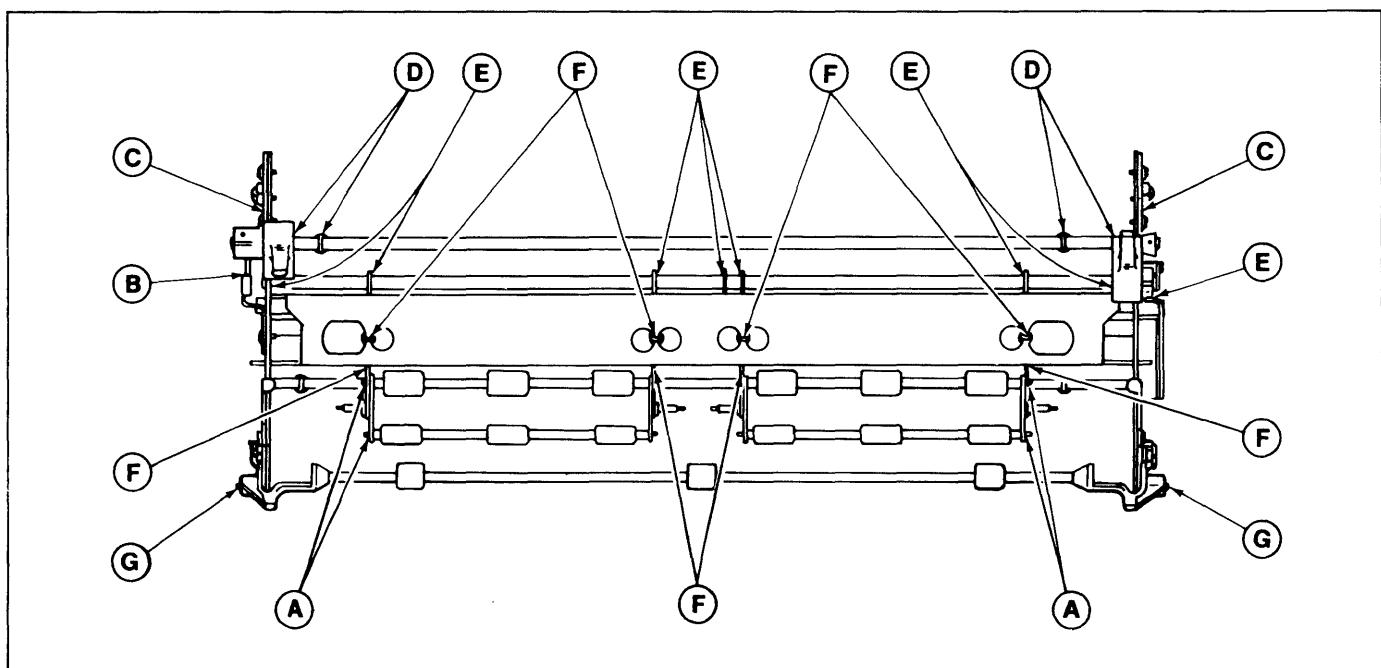
Figure 3-1. Carrier System Lubrication Points
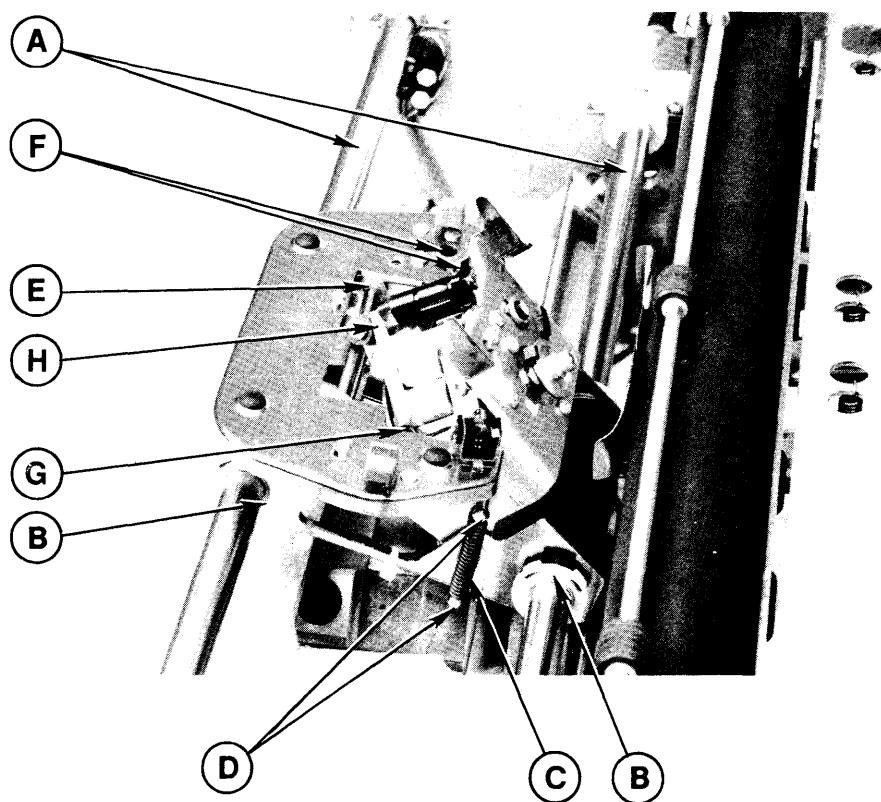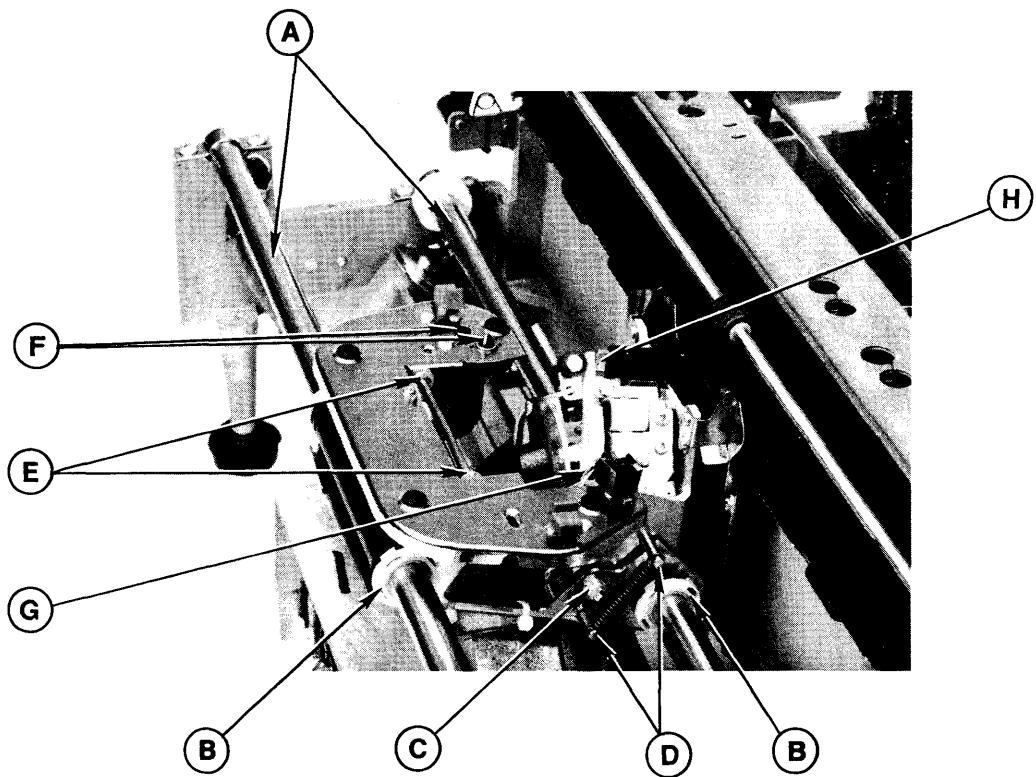
Figure 3-2. Carriage System Lubrication Points

(2) Platen Position Lever Detent Plate (B) — Lightly grease the inside of this plate with No. 70825-01 grease.

(3) Platen Position Slide Plates (Carrier Frame) (C) — Lightly grease exposed slide surfaces (lever moved limit to limit), and all points of contact with pivots, eccentrics, guides, etc., with No. 70825-01 grease.

(4) Platen Position Torque Shaft Ends, Bearing Surfaces, and Spring Loops (D) — Lightly grease these points with No. 70825-01 grease.

(5) Paper Release Lever Tab Ramp and Shaft Pivots (E) — Lightly grease these points with No. 70825-01 grease.

(6) Paper Release Torque Shaft Pivots and Arm Slots (F) — Lightly grease these points with No. 70825-01 grease.

(7) Paper Bail Pivots (G) — Lightly grease these two points with No. 70825-01 grease.

3.2.3.2 CARRIAGE SYSTEM (Figure 3-2)

(1) Carriage Rails (A) — Clean these items only with alcohol wipers.

(2) Carriage Rail Bearings (B) — Put 4 or 5 drops of No. 70243 oil on each side of carriage rails and move carriage back and forth slowly by hand, allowing oil to saturate the felts.

(3) Carriage Pivots (C) — Apply one drop of No. 70243 oil to the pivot on each side of the carriage frame.

(4) Carriage Pivot Spring Loops (D) — Lightly grease the end loops and posts of the pivot spring on each side of the carriage frame with No. 70825-01 grease.

(5) Ribbon Base Plate Pivots (E) — Saturate the felt washer on each end of the base plate pivot shaft with No. 70243 oil.

(6) Ribbon Drive System (F) — Apply one drop of No. 70243 oil to the drive and idler gear shafts, and to the drive key slot.

(7) Hammer Armature Pivots (G) — Remove the two rubber cups, and fill the grease chambers with No. 70364 Polyoil grease. Replace the rubber cups.

(8) Print Hammer (H) — DO NOT lubricate this item. If cloth ribbon is used, insure that hammer is clean.

3.2.3.3 PLATEN SYSTEM (Figure 3-3)

(1) Paper Feed Idler Gear (A) — Inspect the large felt washer behind this gear. If it is becoming white in color, saturate with No. 70364 Polyoil.

(2) Platen Latches (B) — Lightly grease the contact area between these arms and the carrier side frames.

(3) Platen Hubs (C) — Apply one drop of No. 70243 oil to the bore of the hub at each end of the platen.
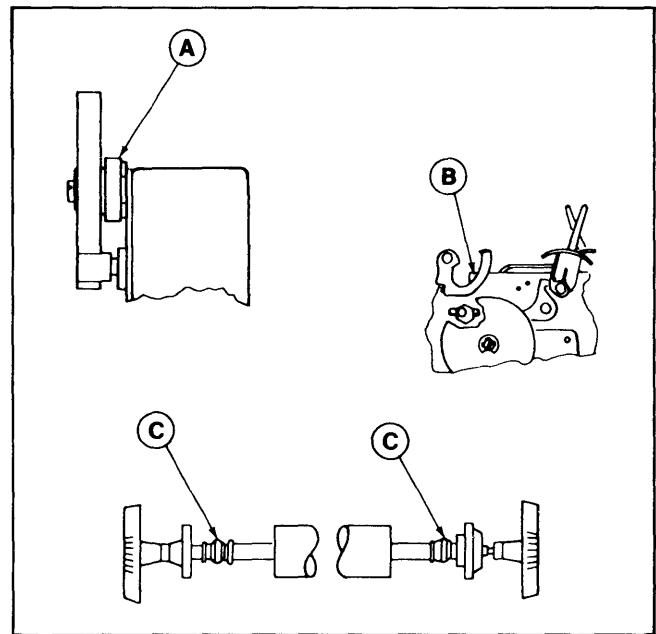
Figure 3-3. Platen System Lubrication Points

3.2.4 Covers and Switches

Reassemble the HyTerm and note the following items:

(1) Replace printer top cover. Check for proper keyboard and control panel alignment. If any keys or switches rub against the cover, reposition the keyboard, control panel, and/or cover.

(2) Check for proper operation of the paper-out switch.

(3) Check for proper operation of the cover-open switch. If the access cover fits too loosely, adjust and/or form its clamping springs.

(4) Replace all covers and test. Operate all keys and switches in Local mode and verify proper HyTerm operation. If facilities are available, establish a remote data link and test transmit/receive capabilities.

3.3 MODULE/SUBASSEMBLY REMOVAL AND REPLACEMENT

Always make sure power is off before attempting to replace any components, modules, or subassemblies.

When module replacement is impractical, subassembly replacement is a ready alternative.

All modules have been assigned "assembly numbers" according to the system adopted by the American National Standards Institute (ANSI) in their standard no. Y32.16, "Reference Designations for Electrical and Electronics Parts and Equipments". Table 3-1 lists all major assemblies, and the smaller assemblies that are normally considered replaceable as modules, along with their reference designations. These designators are used in the remainder of this section and in the schematics and wiring diagrams, to identify the various assemblies.

3.3.1 Circuit Boards

CAUTION

Never remove or insert circuit boards or plugs with the power on.

REMOVAL

(1) Turn off power to the HyTerm.

(2) Remove paper or forms from the printer. Remove tractor feed if so equipped. Raise or remove the printer access cover. Remove the platen (refer to Section 2.4.3 of the Product Description manual if necessary).

(3) Remove the top cover (3.1.2).

(4) Using a Phillips screwdriver, loosen the single screw in the center of the circuit board clamp (Figure 3-4) and remove the clamp.

(5) Locate the board to be removed. See Figure 3-4.

(6) Grasp the board firmly at the two upper corners and pull it straight up.

(7) Disconnect any remaining cables from the board.

REPLACEMENT

(1) If the HPRO board is being installed, first attach the keyboard cable to the P2 connector on the circuit board.

(2) Holding the board with the components toward the front of the machine (toward the platen), insert the board into the guides and slide it all the way in.

Table 3-1. Major Assemblies and Modules

Assembly No. (Reference) Designator)	Description
A1	HyType II printer
A1A1	8080 INTERFACE board
A1A2	LOGIC-2 board
A1A3	SERVO board
A1A4	CAR PWR AMP board
A1A5	HPRO1 or HPRO2 board
A1A7	XDCR board
A1A8	P/W PWR AMP board
A2	Power Supply
A3	Keyboard
A4	Control Panel

(3) Using firm, equal pressure on both upper corners of the board, push it in so that it is fully seated into the socket. If excessive resistance is encountered, check first to make sure the proper board is being installed in the socket: all boards are keyed so they will not fit in the wrong socket. Refer to Figure 3-4.

(4) Reconnect any remaining cables. Make sure the lower plug (J8B) on the XDCR board is not turned over — it is possible to install this plug upside down. The control panel ribbon connectors that plug into the HPRO board are numbered; P2 is on the left, P3 on the right.

(5) Replace the platen, insert a sheet of paper, and test the HyTerm briefly.

(6) After determining that the HyTerm is operating properly, remove the platen, replace the circuit board clamp, the top cover, the platen, and test again.

3.3.1.1 HCURL BOARD FIELD INSTALLATION

(1) Remove the old (standard) interface cable, unplug the black connector from the J1 plug in the upper left-hand corner of the HPRO board, remove cable clamp fastened to the left printer side frame, and slide the cable out through the rear of the terminal.

(2) There are six different versions of the HCURL board; refer to Table 3-2 for the correct board.

(3) Install the new HCURL board in position F, just behind the HPRO board.
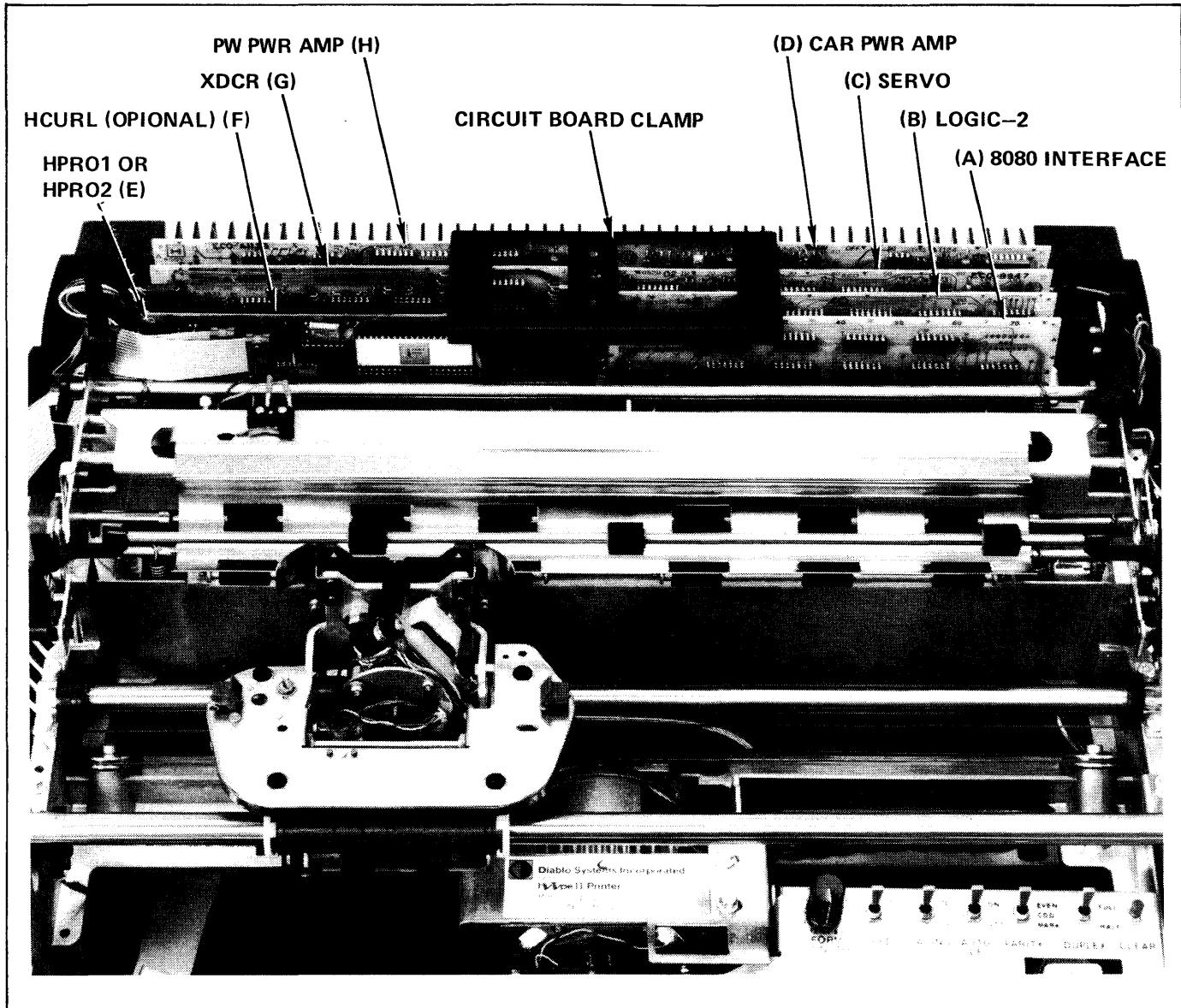
Figure 3-4. Circuit Board Location
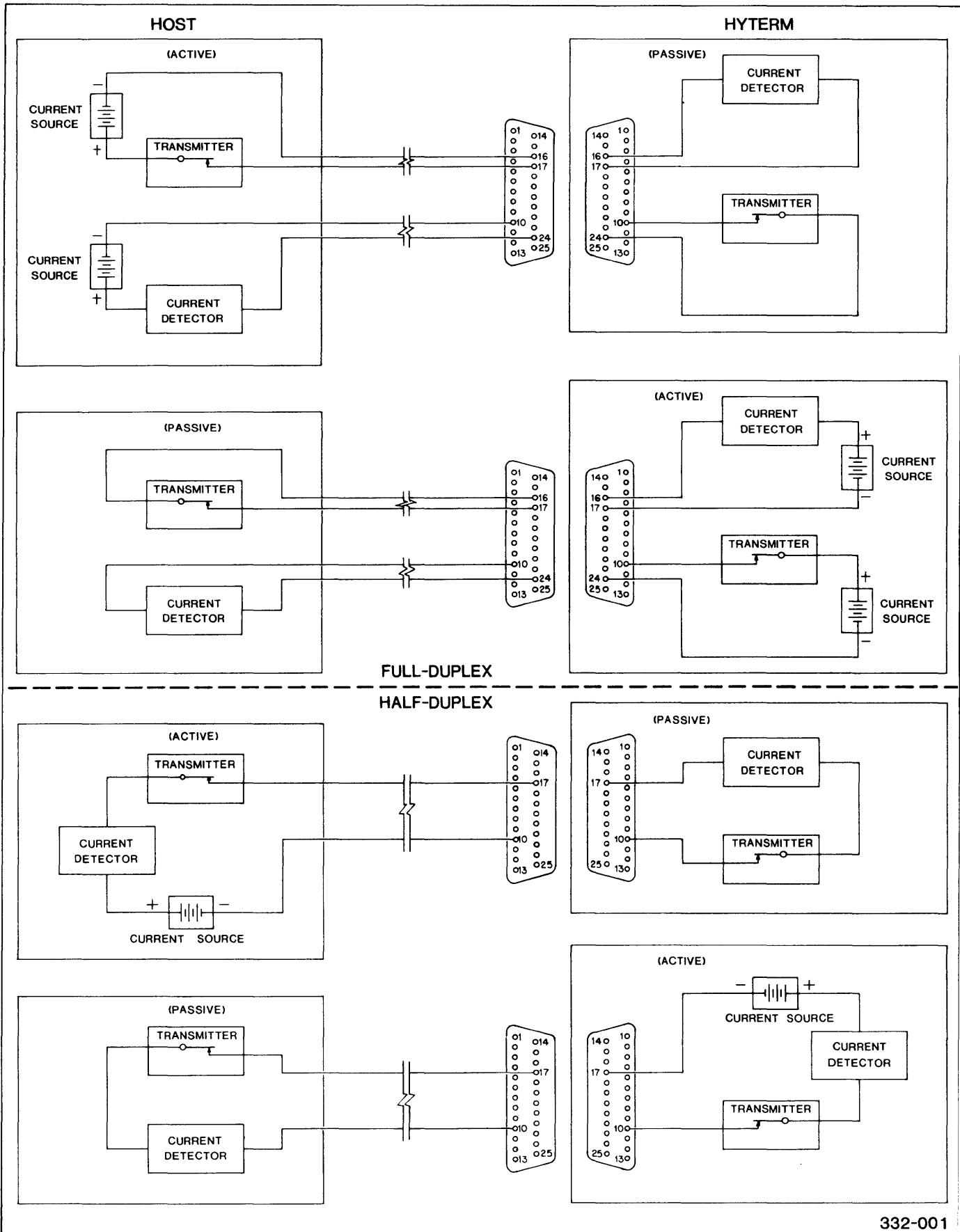
Table 3-2. Current Loop Kit Parts

1. HCURL Board

Kit Part #	HCURL Part #	Type of Operation
400495-01	23942-01	Passive, half-duplex
400495-02	23942-02	20 mA active, full-duplex
400495-03	23942-03	20 mA active, half-duplex
400495-04	23942-04	60 mA active, full-duplex
400495-05	23942-05	60 mA active, half-duplex
400495-99	23942-99	Passive, full-duplex

2. Interface cable assembly, part no. 400017-01.

3. Information Packet, part no. 400496-01.

Figure 3-5. Current Loop Connections

(4) Install the new interface cable

  (a) Insert the end with the two small plugs (P2 and P3) into the left rear of the HyTerm.

  (b) Connect P2 (the 14-pin connector) to the J1 connector on the HCURL board.

  (c) Connect P3 (the 12-pin connector) to the J1 connector on the HPRO board.

  (d) Dress the cable neatly and install the cable clamp (removed in step 1) to hold it in place.

NOTE

The DUPLEX switch on the control panel must be in FULL position.

(5) Refer to Figure 3-5. Wire a compatible socket [25-pin subminiature: Cannon or Cinch DB25P, or AMP housing 205208-1 with 1-66506 pin inserts; with an AMP 206472-1 (or equivalent) hood enclosing the plug] to the current loop wires, and connect it to the new HyTerm interface cable plug.

3.3.2 Power Supply

REMOVAL

(1) Make sure the HyTerm is disconnected from its power source.

(2) Move the HyTerm to a location where both the top and bottom will be accessible when the machine is tilted up.

(3) Raise the access cover. Remove the platen, paper cradle and top cover.

NOTE

If the top cover is the type having the control panel fastened to it, unplug the control panel cables from the HPRO board, free the cables, and set the top cover aside.

(4) Remove the five screws holding the power supply assembly to its aluminum cover screen and the printer frame. This will allow the power supply to drop slightly, but it will still be held in place by the bottom cover.

(5) Remove the last two rear circuit boards which have the heat sinks mounted onto them. Tilt the HyTerm up so it is resting on the rear edge of the bottom cover.

CAUTION

Whenver the HyTerm is tilted up in this manner, hold on to it with one hand to prevent it from falling over.

(6) Loosen the three front screws and three rear screws that hold on the bottom plate. Do not remove. (The rear screws are more accessible if the HyTerm is positioned close to the edge of its table or other supporting surfaces.) Remove the single screw on each side of the bottom plate. Bow the plate out in the middle to free the top or bottom edge from the mounting screws, and remove the plate.

(7) Swing the power supply out to access the terminal strip. Disconnect the wires. Set the power supply assembly safely aside and tilt the HyTerm down onto its feet.

REPLACEMENT

(1) Tilt the HyTerm up and connect the wires to the new supply as per Figure 3-6. Observe the caution about tilting the HyTerm noted in step (5) of the removal procedure.

(2) Swing the power supply into position inside the printer casting. Make sure all wires and cables are positioned securely.

(3) Holding the power supply in position, insert the mounting screws through the top cover screen and the printer casting and start them into the threads in the power supply frame. Start all five mounting screws.

(4) Tilt the HyTerm down onto its feet. Tighten all five mounting screws securely.

(5) Replace the two rear circuit boards noted in step (5) of the removal procedures.

(6) Refer to section 3.4.3, +5 volt adjustment, steps (1) - (9), to check out the Power Supply.

(7) Tilt the HyTerm back up.

(8) Replace the bottom plate: slide it under the rear screws first, bow it out in the center and slip it under the front screws. Then insert the two side screws and tighten all of the screws.

(9) Tilt the HyTerm down onto its feet. Remove the circuit board extender and replace the HCURL board, if applicable. Install the top cover, the paper cradle, and the platen. Close the access cover, insert a sheet of paper, apply power, and test thoroughly.

TB1

POWER

SUPPLY

1   WHITE (2) **+5V**

2   BLACK (2) **GND**

3   BLACK (1) **GND**

4   RED (2) **+15V**

5   BROWN (2) **-15V**

6   NOT USED

7   FRAME GND
(NOT USED)

AC TO FAN { BLACK 8   BLACK } AC FROM POWER SWITCH

{ WHITE 9   WHITE }
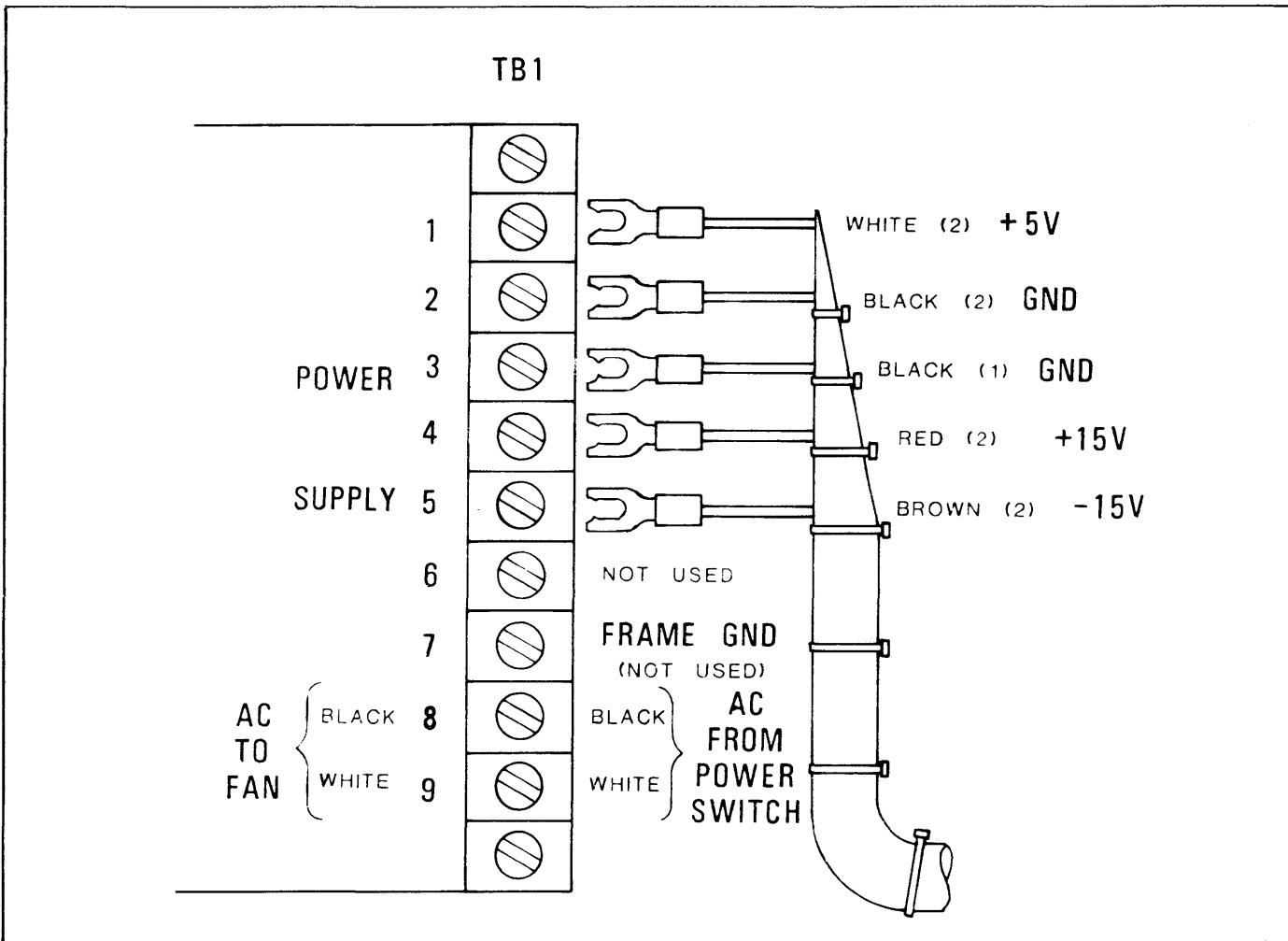
Figure 3-6. Power Supply Connections

3.3.3 Control Panel

REMOVAL

(1) Unplug the HyTerm from its power source.

(2) Raise the access cover. Remove the platen skirts, the platen and the top cover.

(3) If the control panel is the type mounted to the top cover, remove the two mounting nuts with a 5/16-inch end wrench, remove the cables from the cable clamps, and remove the control panel from the cover.

(4) Unplug the control panel cables from the two connectors on the HPRO board, and slide the flat cables out of the cable clamps.

NOTE

Observe flat cable routing so the new cables can be installed the same way.

(5) For control panels mounted to the printer casting, remove the three screws that fasten the control panel mounting brackets to the printer frame, two on the carriage motor frame and one on the right side frame.

REPLACEMENT

(1) On control panels mounted to the top cover, position the panel on the cover, install and tighten the two lock nuts, and skip to step (3).

(2) On control panels mounted to the printer casting, place the control panel in position and insert the three mounting screws. Tighten all screws just snug enough to hold the panel in position, but still allow it to be moved by hand.

(3) Dress the cables between the keyboard and the printer casting, around the left side of the printer, and up to the HPRO board. Insert the cables into the flat cable clamps. Plug the cables into the HPRO board. The two cables have numbers stamped on them. The one stamped "2" plugs into the left-hand

(4)   Replace the top cover.

(5)   For panels mounted to the cover, go on to step (6). For panels mounted to the printer casting, move the control panel assembly right-to-left until the switches are centered in the switch openings, and tighten the three bracket mounting screws. Test all switches for proper operation. If the switches do not operate properly, or if it is difficult to attach the top cover properly, it will be necessary to adjust the control panel up-and-down or backward-and-forward. Refer to Section 3.4.2 for this procedure.

(6)   Replace the platen and the platen skirts, plug into a power source, and test for proper operation.

3.3.4   Keyboard

REMOVAL

(1)   Unplug the power cord from the wall outlet.

(2)   Raise or remove the access cover. Remove the platen skirts and the platen. Remove the top cover (3.1.2).

(3)   Unplug the keyboard cable from the keyboard.

(4)   Remove the four screws that mount the keyboard to its mounting bracket. Lift out the keyboard and set it aside where it will not be subject to damage.

REPLACEMENT

(1)   Position the new keyboard in place on the mounting brackets. Start all four mounting screws. Position the keyboard in its approximate final position and tighten one screw on each end.

(2)   Attach the keyboard cable plug to the keyboard.

```
┌─────────────────────────────────────┐
│               WARNING                │
│                                      │
│  When the HyTerm is connected to a   │
│  power source, line voltage is present at │
│  the POWER switch terminals. To avoid a │
│  dangerous shock when power is applied │
│  and the top cover is removed, keep  │
│  fingers away from the POWER switch  │
│  terminals.                          │
└─────────────────────────────────────┘
```

(3)   Plug the power cord into the wall outlet, turn on power, and test for proper keyboard operation. (Pull the cover-open switch plunger out to its override position to allow normal operation with the covers off.)

(4)   Turn off power and unplug the power cord. Carefully position the top cover in place, while checking for proper clearance between the keytops and the cutout in the top cover. Using a trial-and-error process, reposition the keyboard until the top cover can be installed fully with no interference between the keytops and the cover.

(5)   When the correct position of the keyboard has been obtained, again remove the printer cover, tighten all four keyboard mounting screws fully, and reinstall the cover.

(6)   Replace the platen and the platen skirts. Plug in the power cord, turn on power, and test the HyTerm again.

3.3.4.1   KEYSWITCH REPLACEMENT

Once the keyboard has been removed, individual key-switches can be replaced, using a soldering iron and two special module removal tools. The special tools are available from the Micro Switch division of Honeywell, Freeport, Illinois. Order no. SD-10101. Proceed as follows:

CAUTION

When removing the LOCAL or UC ONLY keytops, make sure the switch plunger is in its upper position; otherwise, the module will be damaged.

(1)   Remove the keytop from the module being replaced, by lifting or prying upward with a padded tool. Remove the keytops from the modules on either side of the one to be replaced. It may be necessary to remove other adjacent keytops to provide adequate work space.

A special keytop puller, no. SW-10485, is available from Micro Switch.

(2)   Unsolder the four module terminals from the circuit board. Use a solder removal tool to remove all solder from the pin holes in the circuit board.

(3)   Insert the module removal tools, one in front and one behind the module being removed.

(4)   Grip the switch module with a pair of pliers and pull it straight out.

(5)   Install the replacement module. Before snapping it into place, make sure it is oriented properly and that all four pins are through the circuit board.

(6) Solder the new switch terminals, using 60/40 rosin core solder and a 750°F soldering iron with a 1/8" chisel tip.

CAUTION

Never hold the soldering iron to the module pins for more than four seconds.

(7) The solder joints may be cleaned (on the bottom of the circuit board) with mild solvent. Be careful not to get any solvent on the switch modules or keytops.

(8) Replace all keytops. Make sure they are replaced on the right key and that the legends are properly oriented.

3.3.5 Cooling Fan

REMOVAL

(1) Remove the printer covers and unplug the HyTerm from its power source.

(2) Using a TORX T15 screwdriver remove the two (2) 8-32x.625 screws holding the fan to the printer frame and retrieve the spacers.

(3) Gently pull the fan up and away from the carriage frame to provide enough room to disconnect the motor leads.

(4) Disconnect the two motor leads from the fan cable assembly by pulling the connectors apart.

(5) If the fan cable assembly must be replaced, first follow the procedures for removal of the power supply (Section 3.3.2) to gain access to the fan cable connectors. Then unscrew the two (2) connectors from pins 8 and 9 of the power supply terminal strip.

REPLACEMENT

(1) Reverse the removal steps with a new fan and/or fan cable assembly.

3.3.6 Paper Feed Motor

REMOVAL

NOTE

This procedure can be used with or without the carrier subassembly being removed from the printer. If the carrier subassembly is not to be removed, then complete Steps 1, 2, 3 and 4 of Procedure 3.3.7.

(1) Using a TORX T15 screwdriver, remove the three (3) 8-32 x 3/4" screws holding the paper feed motor to the right-hand carrier side frame as follows: remove the two bottom screws first, and retrieve their spacers from between the motor flange and the carrier frame. Remove the upper right-hand (as you view it) screw last, and retrieve its spacer from behind the motor flange. Note that this spacer has a shoulder which fits into the motor flange hole to prevent side play. Refer to Figure 3-7.

(2) Tilt the motor down and out of the carrier side frame, and gently pull its connecting wires free from the wire bundle inside the printer.

(3) Using an 11/32" open end wrench and a blade screwdriver, remove the paper feed idler gear mounting stud eccentric, nut, and washers (2) from the paper feed motor's upper left-hand flange hole (as you view it). Refer to Figure 3-7.

(4) Transfer the items removed in Step (3) above to the replacement motor exactly as they were arranged on the removed motor (upper left-hand flange hole, nut and washers to the rear side).

IDLER GEAR ECCENTRIC

PAPER FEED MOTOR

(TOP P.O. SW. BAIL SHAFT HOLE)

UPPER MOUNTING SCREW (SPECIAL SPACER)

LOWER MOUNTING SCREWS (PLAIN SPACERS)
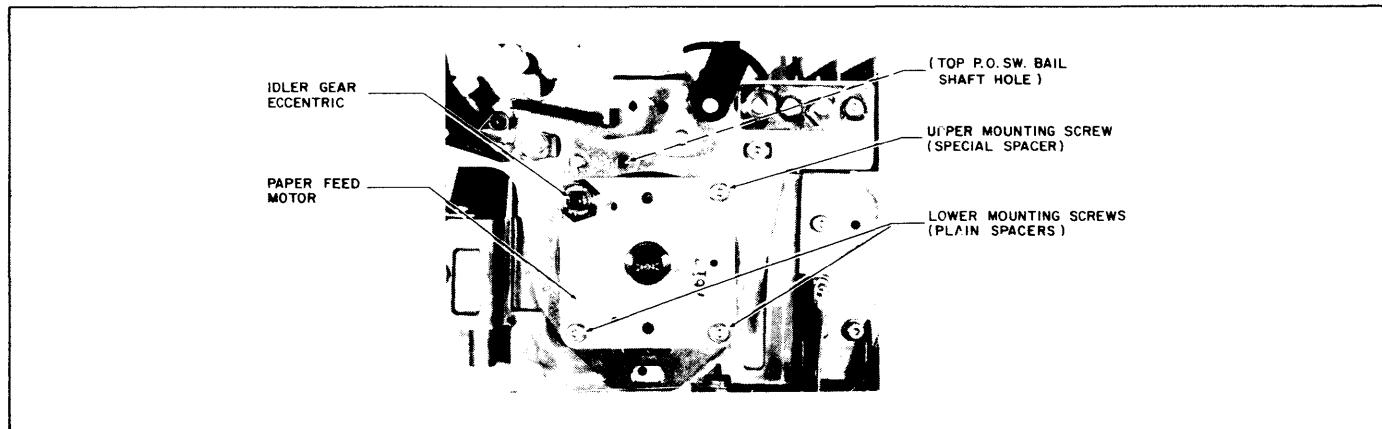
Figure 3-7. Paper Feed Motor Removal

REPLACEMENT

(1) Carefully insert the replacement paper feed motor's connecting wires into the opening in the right-hand carrier side frame, and tilt the motor into position in the frame opening.

(2) Orient the paper feed motor with the idler gear eccentric stud upper left, as shown in Figure 3-7. Insert the special shoulder spacer [removed *last* in Step (1) of the removal procedures above] behind the motor's upper right flange, with its shoulder extending into the hole in the flange. Loosely thread one of the 8-32 x 3/4'' screws into the carrier side frame through the motor flange and spacer.

(3) Place spacers behind and insert 8-32 x 3/4'' screws [removed *first* in Step (1) of removal procedures above] through the two bottom motor mounting holes; then finger tighten only. Now tighten the first screw [step (2) above] until snug, but not so tight as to restrict lateral movement of the motor.

This completes the installation of the paper feed motor *only* on a carrier subassembly. If this was a motor replacement only (did not involve paper carrier removal),

skip to Section 3.3.7, Step (6) for the remaining steps to reconnect the motor electrically, and for directions leading up to its adjustment.

3.3.7 Paper Carrier Subassembly

REMOVAL

(1) Remove the access cover, platen, and top cover (make sure power is off first).

(2) Remove and store the ribbon cartridge, printwheel, and paper cradle.

(3) Use the no. 99009 T-Handle Spring Hook to disengage the four (4) Carrier System load springs from the printer's main frame (2 long springs in front, and 2 short springs in the rear). Open the wire bundle and disconnect the four (4) paper feed motor wires from the mother board. Refer to Figure 3-8.

(4) Remove the 'E' ring and the paper feed idler gear. Locate the two carrier assembly load springs, one on each end, mounted between the inboard end of the rear support screw on the main frame. Remove these springs also. Store the springs, gear, and 'E' ring in a safe place. Refer to Figures 3-8 and 3-9.
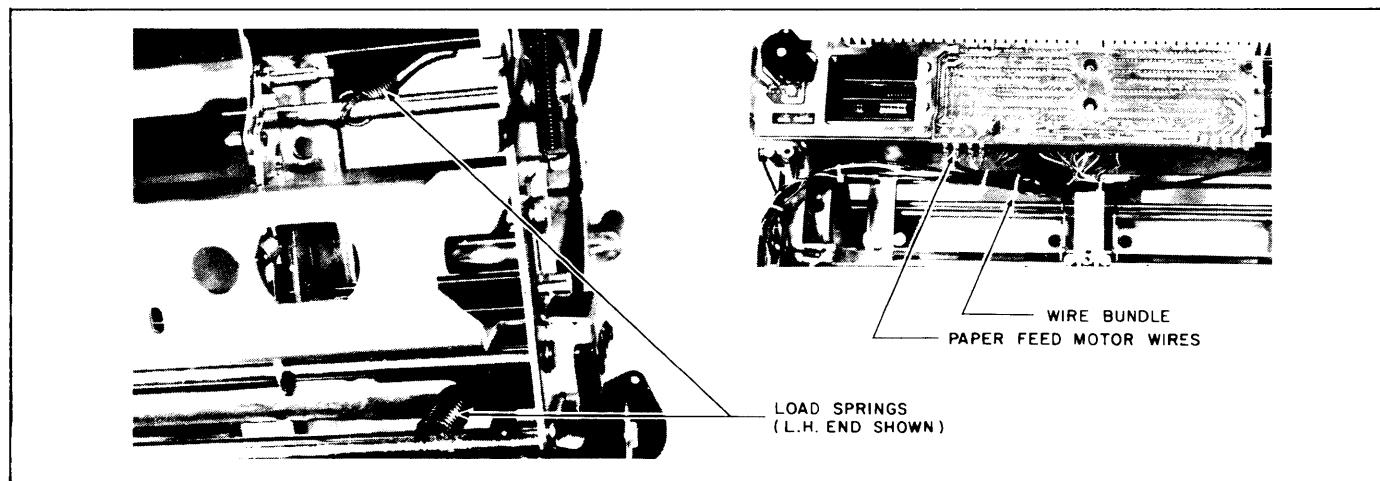
Figure 3-8. Carrier System Removal
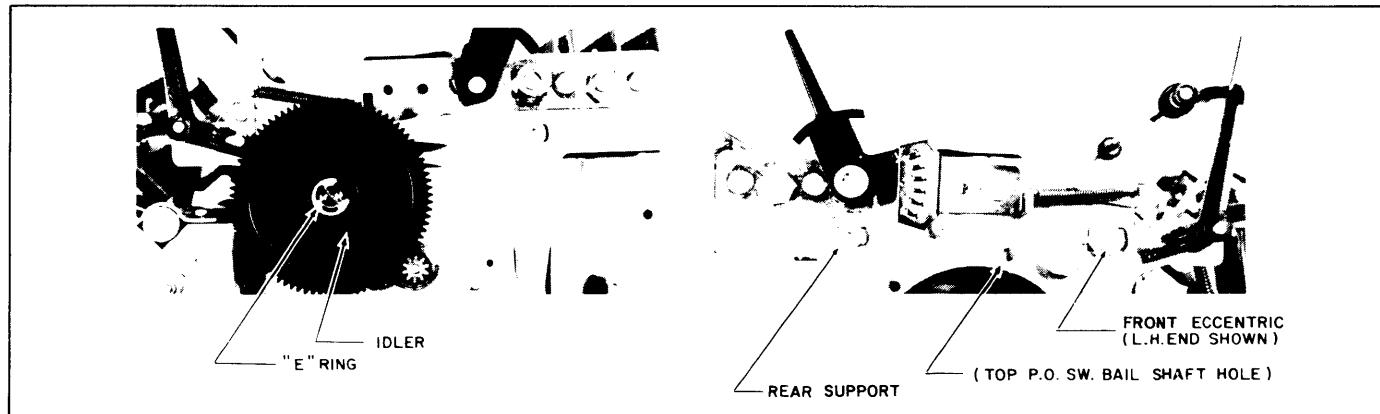
Figure 3-9. Carrier System Removal

(5) Using a 1/4" wrench or nut driver, remove the left- and right-hand front carrier subassembly height adjustment eccentrics. Using a TORX T15 screwdriver, remove the left- and right-hand rear carrier subassembly support shoulder screws. Store these items in a safe place. Refer to Figure 3-9.

(6) Carefully lift the carrier subassembly, including the paper feed drive motor, free of the printer main frame, as shown in Figure 3-10. Be sure the motor wires are free and not caught in the wire bundle.

REPLACEMENT

(1) Clean all carrier subassembly bearing surfaces on the printer main frame of old grease, etc. Reapply a light coating of multipurpose grease to these points, on both ends of the main frame. Refer to Figure 3-11.
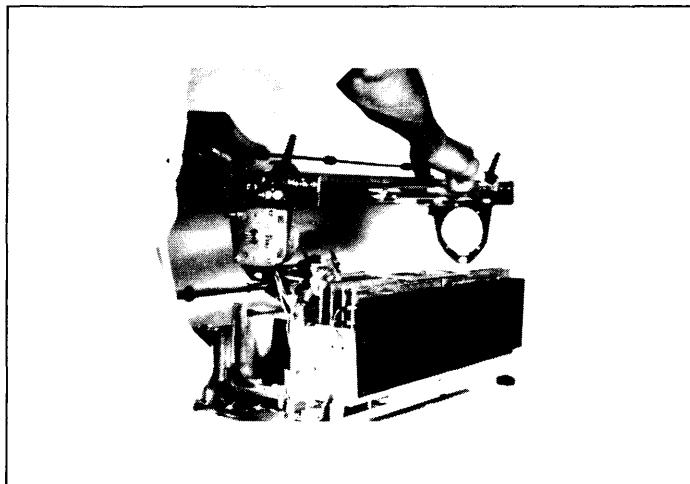
Figure 3-10. Carrier System Removal

(2) Carefully lower the carrier subassembly into position on the printer main frame. Refer to Figure 3-10.

(3) Insert the left- and right-hand rear carrier subassembly shoulder support screws removed in Section 3.3.7 removal procedures, Step (5), using the TORX T15 screwdriver. Make sure the screw shoulders pass into the slots in the carrier side frame, and tighten the screws firmly, but DO NOT overtighten and strip the threads from the holes in the main frame casting.

(4) Insert the left- and right-hand front carrier subassembly height adjustment eccentrics removed in Section 3.3.7 removal procedures, Step (5), using a 1/4" wrench or nutdriver. Make sure the shoulders of the eccentrics pass into the slots in the carrier side frames, and thread the screws in enough to retain the eccentrics snugly in the slots, but do not tighten. The eccentrics should be positioned so their lobes point toward the rear of the machine.

(5) Use the #99009 T-Handle Spring Hook to connect the loose ends of the four carrier subassembly load springs to the main frame making use of the holes provided. Section 3.3.7 removal procedures, Step (3), detailed the unhooking of these springs for the old subassembly just removed.

(6) Arrange the four wires from the paper feed motor into the wire bundle running along the edge of the mother board, and connect them to the push-on terminals on the mother board as follows: gray wire to terminal T4; black wire to terminal T5; yellow wire to terminal T6; and the red wire to terminal T7. Secure the wire bundle with plastic cable ties or equivalent.

TORQUE SHAFT BEARING NOTCH

CARRIER SIDE PLATE
SLIDING BEARING SURFACES

(R.H. END SHOWN)
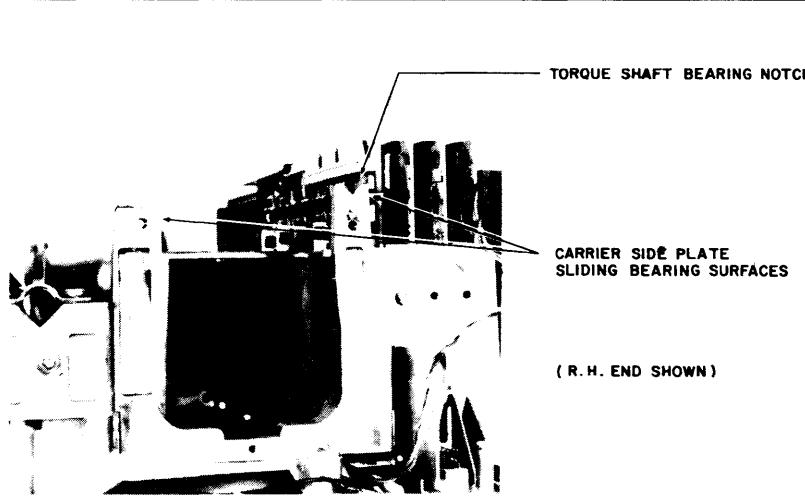
Figure 3-11. Carrier System Replacement

3.3.8 Carriage Subassembly

REMOVAL

(1) Remove the access cover, platen, and top cover (make sure power is off).

(2) Remove and store the ribbon cartridge and printwheel.

(3) Open the left-hand (as shown in Figure 3-12) wire bundle, and unplug the sheathed printwheel drive cable connector P4 at mother board connector J4. Separate this cable from the wire bundle for later removal. Also disconnect the black ground wire, which is a part of this cable, where it is fastened to the main frame near the end of the cable's shield spring.

(4) Open the other wire bundle. Locate the sheathed cable extending from connector J8B on the Transducer board (Slot G) to the carriage through the smaller cable shield spring. Unplug this cable at the circuit board, and prepare it for later removal from the printer with the carriage.

NOTE

If the optional Bottom Feed Paper Chute is installed, skip to Step (6).

(5) Refer to Figure 3-13. Using the TORX T15 screwdriver, reach down behind the left end of the rear carriage rail and unscrew the four (4) #6-32 x 1/2" screws holding the white plastic spring cable clamps to the bottom plate. Retrieve and store these screws. Reach down behind the right end of the rear rail and remove the large spring cable shield from the two spring clips holding it to the bottom plate.

(6) This step applies only to those printers with the optional bottom feed paper chute installed. Refer to Figure 3-12.
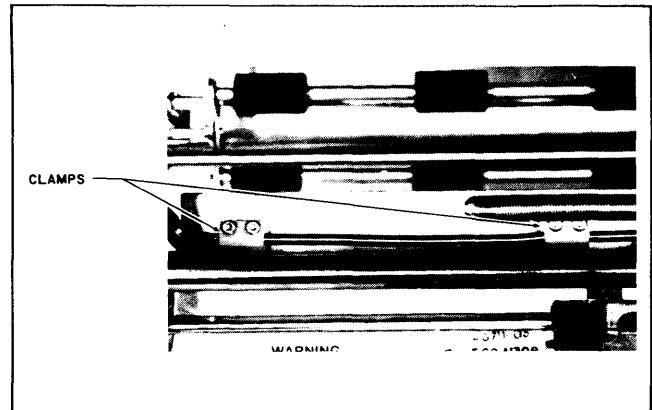
Figure 3-13. Cable Clamp Removal

● Use the TORX T15 screwdriver to remove the four (4) no. 8-32 x .625" screws which fasten the bottom plate to the printer's main frame.

● Move this plate away from the frame far enough to release the large spring cable shield from the two spring clips, and to gain access to the four (4) no. 6-32 x 1/2" screws used to clamp the small spring cable shield to the bottom plate. Remove these screws using the TORX T15 screwdriver.*

*Service Note: If the printer being worked on has other wire bundles fastened to the bottom plate with snap-in metal spring clips, remove these clips and replace them with cable ties.

(7) Refer to Figure 3-14. Position the carriage slightly to the right of center, to gain access along the right side of the carriage servo motor to the mounting screw for the carriage drive cable pulley. Install the hemostat clamp on the pulley as shown (use a piece of heavy paper between the pulley and clamp jaws to protect the pulley flanges). This prevents the pulley from moving or flipping over and releasing the drive cables. Refer especially to Figure 3-14b. Note that the clamp is installed to trap the upper forward right-hand cable
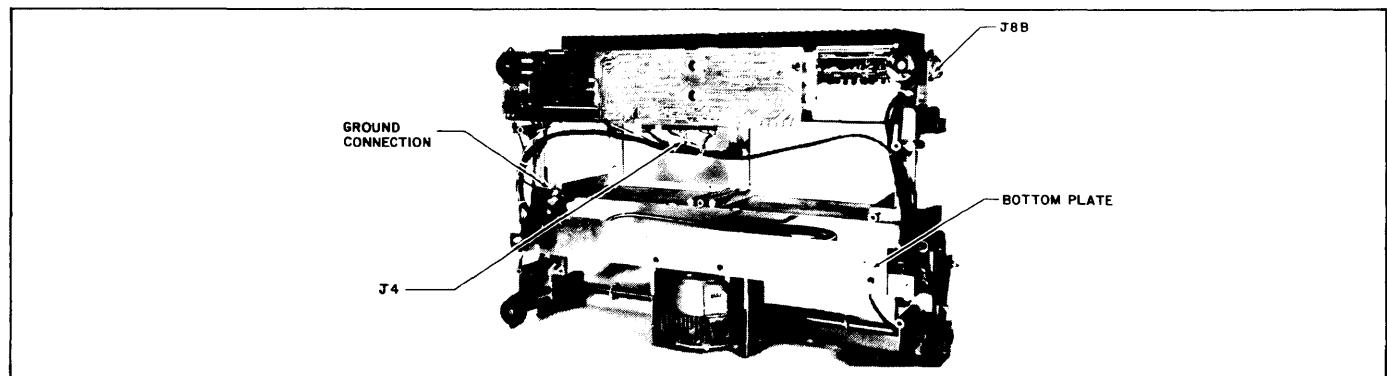
Figure 3-12. Prepare Carriage Cables for Removal

a   b
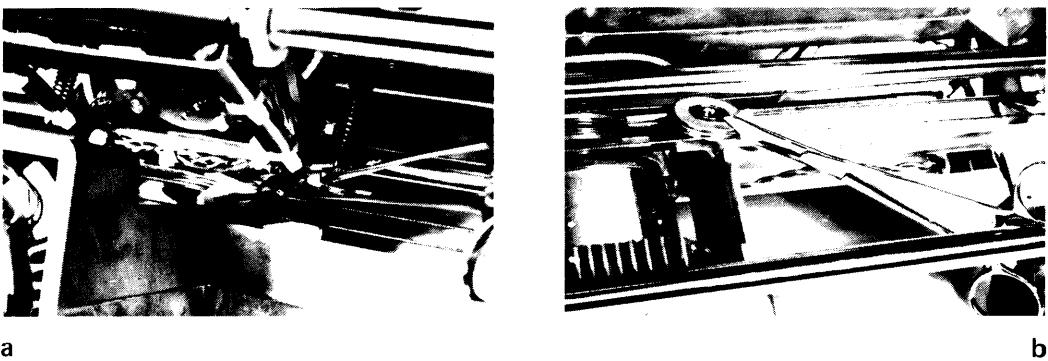
Figure 3-14. Disconnecting the Carriage Drive Cable

segment between its jaws as it is clamped to the pulley. Make sure this has been done, and that the clamp is secure before proceeding.

Use the TORX T15 screwdriver to reach up beside the carriage motor and remove the pulley mounting screw. Make sure the pulley is free from the carriage frame, and gently move the carriage to the left to clear the pulley. Retrieve the spacer from the top of the pulley, and note that the spacer has a shoulder which extends down into the center of the pulley when properly assembled. Store the spacer and pulley mounting screw. *DO NOT* remove the hemostat clamp from the pulley!

(8)   Refer to Figure 3-15. Using the TORX T15 screwdriver, remove the eight (8) no. 8-32 x .625" carriage rail clamp screws, clamps, and the impression control switch, and store the loose items. Grasp the carriage and rails in one hand and carefully lift the assembly up out of the printer main frame while guiding the two shielded cables and their connectors clear of the printer structure.

(9)   Lay the carriage and rail assembly on a clean flat surface. Slide the front rail sideways out of the front carriage bearing sleeve and put it aside in a safe place. Slide the heavy rubber bumper washers off the ends of the rear rail. Note that there are two washers on the left end, and only one on the right end. Store these washers. Finally, slide the rear rail sideways out of the rear carriage bearing sleeve, and place with the front rail.

REPLACEMENT

Replacement carriage subassemblies are complete, jig aligned, and functionally tested at the factory. They are ready for installation and operation as received, and usually require only a minor readjustment or two for print quality after installation.

(1)   Carefully remove the white felt washers from their plastic bag (shipped with each carriage subassembly), and saturate 4 of them (there are usually 1 or 2 extra) with light oil.

RAIL
CLAMPS

RAIL
CLAMPS

IMPRESSION
CONTROL
SWITCH
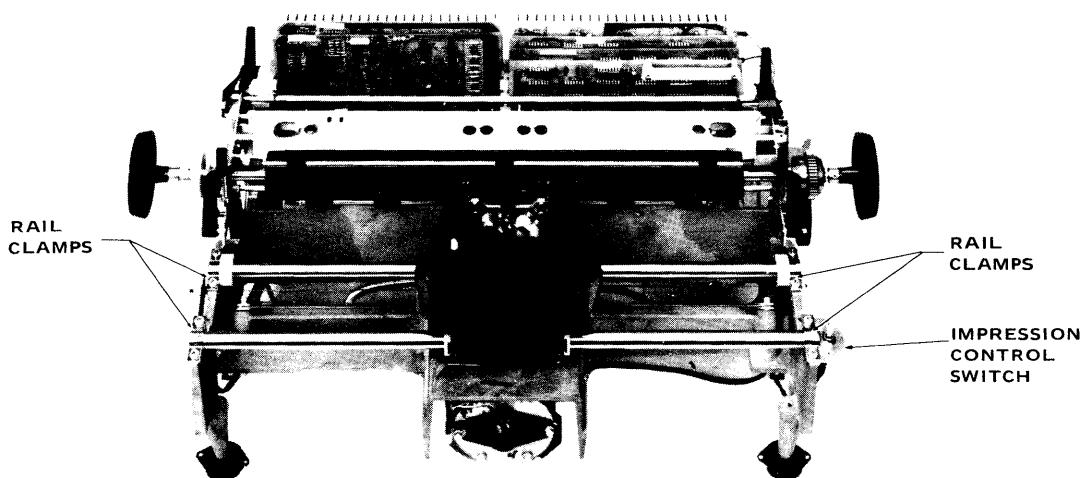
Figure 3-15. Carriage Rail Clamps

3-16

(2) Unless replacement of the carriage drive cable is to be included at this time, remove the drive pulley and spacer from the underside of the carriage.

(3) Retrieve the carriage rails from their storage place, and thoroughly clean them with alcohol. After cleaning, check both rails for straightness and surface defects. Replace any rail which is bent or defaced.

(4) Refer to Figure 3-16. Slide the cleaned and inspected carriage rails through the front and rear carriage bearing sleeves.

(5) Gently slide an oil saturated felt washer on each rail end, followed by a white plastic bearing wiper. Be very careful not to stretch or break the felt washer. Push the washers into their bearing sleeves with the bearing wipers, and snap the wipers into position over the ends of the bearing sleeves.

(6) Install the heavy rubber bumper washers on the rear carriage rail, two on the left end, and one on the right end.

(7) Gently lower the carriage subassembly and rails down onto the printer main frame, with the rail ends nested in the frame notches. Move the rails until even on each end, reinstall the rail clamps, and the impression control switch. Tighten the 8 clamp screws firmly, using the TORX T15 screwdriver.

(8) Hold the two spring shielded cables up out of the way, and gently slide the carriage back and forth as far as it will go. Carriage movement must be smooth and even, with no evidence of binding or roughness.

CAUTION

DO NOT slide the carriage to the left so as to damage the carriage home sensor (mounted on the main frame) with the sensor flag (mounted on the carriage).

(9) Place the spacer on top of the carriage drive pulley with its shoulder extending down into the center of the pulley. Position the carriage over the clamped pulley, and insert the shoulder screw. The spacer and screw were removed in Step (7), Section 3.3.8 removal procedures. Tighten the screw firmly with the TORX T15 screwdriver, and remove the Hemostat Clamp.

NOTE

If the optional bottom feed paper chute is installed, skip to Step (12).

(10) Arrange the small (transducer) spring shielded cable (from the right side of the carriage) down inside the printer main frame behind the carriage drive cable, and back to the left along the center of the bottom plate. Extend the free end out of the bottom of the printer to the left. Position the first plastic clamp over the threaded screw hole farthest left in the bottom plate, with its holes to the rear. Thread in two (2) no. 6-32 x 1/2" screws, place the spring shield in the clamp with about 1/8" of the spring extending to the left beyond the clamp, and with the loop of the spring as straight as possible vertically, tighten the two clamp screws using a TORX T15 screwdriver. Move the second plastic clamp into
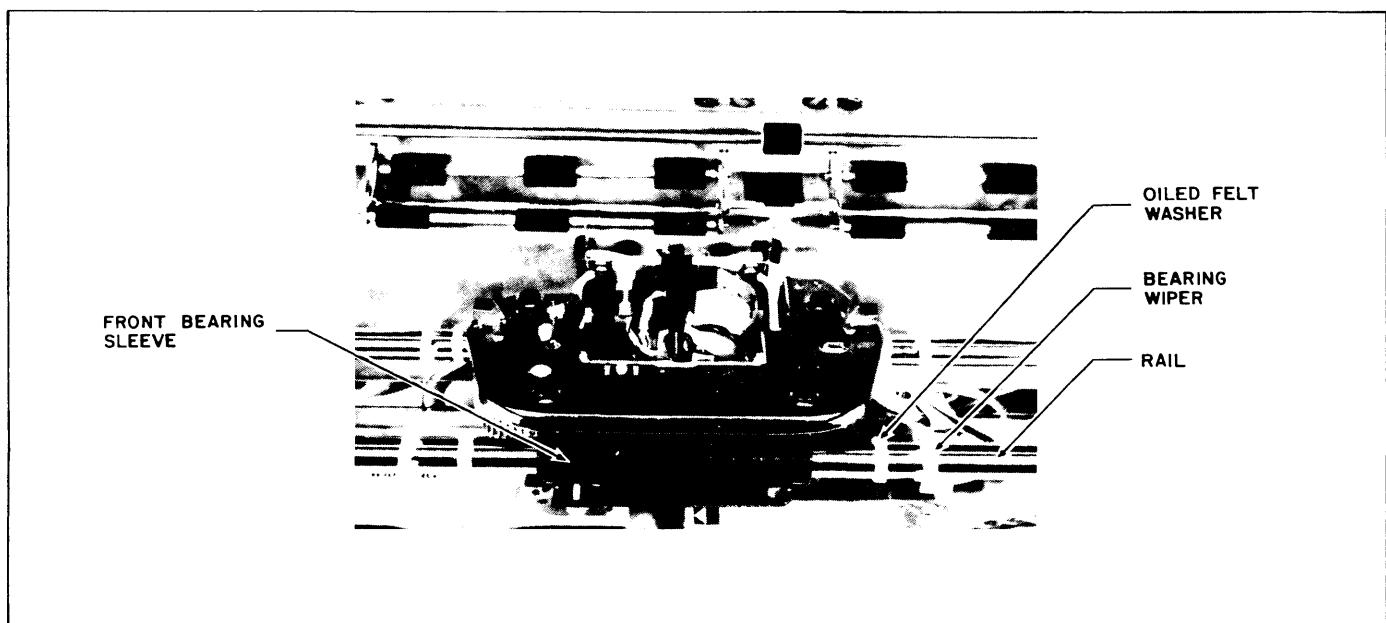
Figure 3-16. Carriage and Rail Assembly

3-17

position, holes to the rear, just left of center on the bottom plate over the two threaded holes provided; insert two more no. 6-32 x 1/2" screws and tighten them securely.

(11) Arrange the large (printwheel drive) spring shielded cable (from the left side of the carriage) down inside the printer main frame behind the smaller spring cable just installed, and along the rear edge of the bottom plate. Extend the free end out the bottom of the printer to the right. Position the spring as straight as possible vertically, with the end of the shield spring about 1/8" beyond the spring clip mounted farthest right on the bottom plate, and push the spring back under the clip. Push the body of the spring shield under the second spring clip located just to the right of the center on the bottom plate.

(12) This step applies only to those printers with the optional bottom feed paper chute installed.

● Position the bottom plate behind the carriage, in the area of the platen, with its spring clips (for the large cable) to the right on top.

● Loop the small (transducer) spring shielded cable (from the right side of the carriage) back around to the left, and position its plastic clamps over the screw holes left of center and near the left end of the bottom plate. Thread in the no. 6-32 x 1/2" screws to hold the clamps in place, but do not tighten them.

● Loop the large (printwheel driver) spring shielded cable (from the left side of the carriage) back around to the right over the smaller spring shielded cable, and snap it into the two spring clips right of center and near the right end of the bottom plate.

● Work the bottom plate, with cables attached, back through the main frame. Move the plate into position and fasten with the four (4) no. 8-32 x .625" screws removed in Step (6) of Section 3.3.8 removal procedures, using the TORX T15 screwdriver. Secure the carriage drive motor wire bundles to the plate with cable ties.

(13) Arrange the two sheathed cables into the wire bundles from which their counterparts were removed in Steps (3) and (4), Section 3.3.8 removal procedures, and plug them in; Transducer cable to connector J8B on the Transducer board (Slot G); and the Printwheel Drive cable to connector J4 on the mother board. Secure the two wire bundles with cable ties.

3.4 ADJUSTMENTS

Any necessary tests and/or adjustments should be performed in the sequence outlined in this section, because some adjustments affect others. No adjustments should be attempted unless a malfunction indicates a specific need.

3.4.1 Printer

Several printer adjustments can be made using the Combination Adjustment Tools, Diablo part no. 40795 or 40795-01, and 40796.

NOTE

In the following procedures you are often told to tilt the carriage forward or rearward: forward means toward the keyboard, the operator, the front of the terminal; rearward means toward the platen. The carriage will detent in either position. To move it forward, first remove the ribbon cartridge. Then simply grasp it by the "ears" near the ribbon guides and pull it away from the platen. To move it rearward, simply push it back up toward the platen.

3.4.1.1 PRINT QUALITY TEST

The print quality test can provide an indication as to possible needed adjustments. Proceed as follows:

(1) Print a full line of capital letter "H"s.

(2) Refer to Figure 3-17 and compare the test results with the illustration.

(a) Impressions similar to this with uniform density and good edge definition indicate proper adjustment of the printer. A gradual change in density (lighter or darker) from one end of the line to the other indicates a Platen-to-Printwheel adjustment may be required.
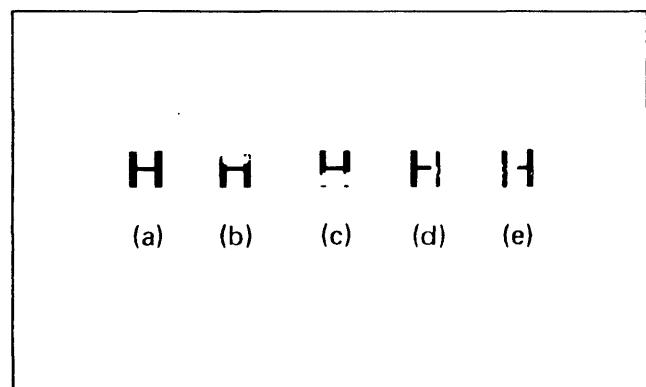
Figure 3-17. Print Quality Standards

(b) Impressions similar to this indicate Platen Height adjustment may be required for platen too low.

(c) Impressions similar to this indicate Platen Height adjustment may be required for platen too high.

(d,e) Impressions similar to this indicate that a Printwheel-to-Hammer adjustment may be required.

3.4.1.2 PAPER CARRIER SYSTEM

3.4.1.2.1 Carrier Assembly.

(1) Carrier Assembly Bias Shaft, Figure 3-18, item (A). Check for axial movement = .002 in., +.000 in., -.001 in. (.05mm, +.00mm, -.03mm). Adjust the collar at (A) as required to achieve this dimension.

(2) Platen Position Torque Shaft, Figure 3-18, item (B). Check that the setscrews in the eccentric collars (C), at each end of this shaft, are aligned vertical with each other when the platen position lever is full forward, and that the shaft end play = .001 in. ± .0005 in. (.03 mm ± .01 mm). Adjust these collars as required to achieve these two goals.

(3) Platen Position Lever, Figure 3-18, item (D). Move the lever back and forth. A positive detenting force must be felt for all positions. Adjust the detent plate (E), as necessary to achieve an even detenting action. The carrier assembly must move equally at both ends in increments of .005 in. ± .002 in. (.13 mm ± .05 mm) between detent positions.

3.4.1.2.2 Paper Feed Rollers. Refer to Figure 3-19. With the paper release lever (A) fully forward, the paper feed rollers (G) must clear the platen (E) by a minimum gap of .080 in. (2 mm). To achieve this, and other goals, adjust the paper feed system as follows:

(1) Insert 4 sheets of standard form paper (.012 in. or .3 mm) and move the paper release lever fully rearward.

(2) Ensure that the torque shaft arm tabs (B) are touching the lower edge of the feed roller support arm slots (C).

(3) Ensure that the paper release actuator (D) is touching the ramp on the paper release lever. Loosen the actuator's setscrew and adjust the actuator to achieve this condition, then retighten the setscrew.

(4) Remove the 4 sheets of paper, and insert one strip of paper 1 in. wide (or a .004 in. shim) between the
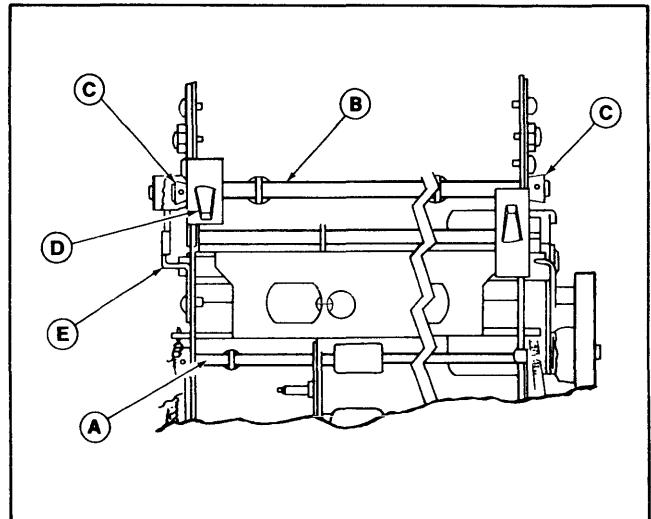
Figure 3-18. Carrier Assembly Adjustment
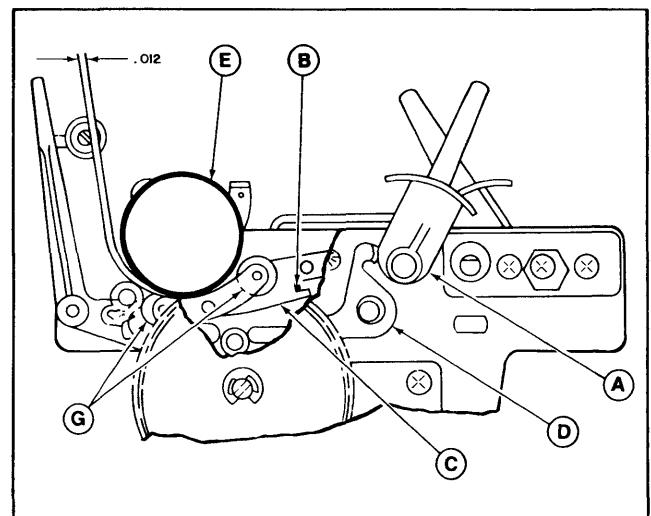
Figure 3-19. Paper Feed Adjustments

front paper feed rollers and the platen. Check that both platen and rollers rotate when the strip (or shim) is pulled free. Repeat for all rollers front and rear. If no rotation occurs, the torque shaft arm tabs (B) have been pushed down too low.

3.4.1.2.3 Paper Feed (Platen) Drive. Refer to Figure 3-20. With paper feed motor drive gear (A) locked, platen drive gear (B) must have a .002 in. (.05 mm) maximum play [total play includes idler gear (C)].

(1) Loosen the paper feed motor mounting screws (D).

(2) Rotate eccentric (E) counterclockwise ONLY (clockwise will not allow the platen to be installed properly), until a minimum backlash is obtained with no binding effect when rotating idler (C) a full 360°.

(3) Install the platen. Rotate the paper feed motor clockwise about mounting screw (D1) to remove

backlash between platen gear (B) and idler gear (C).
Tighten all screws.

3.4.1.2.4   Platen Knob End Play.   Refer to Figure 3-21.
End play should be .002 in. (.05 mm) maximum, as shown.
Adjust for proper clearance by loosening the setscrews in
the platen release gear hub (A) and moving the hub.
Retighten the setscrews.

3.4.1.3   CARRIAGE DRIVE CABLE (Figure 3-22)

(1)   With the carriage positioned against the left hand
mechanical stop, check the cable tension midway
along the exposed cable for a force of 16.5 ± 3.3 lbs.
(7.5 ± 1.5kg) necessary to distort the cable as shown.

NOTE

*If the Tensiometer, listed in Section
3.1.3, is not used, the dimensions
between force points must be carefully
followed.*

(2)   Adjust cable tension by tightening or loosening cable
tension nut (B).

CAUTION

*The square shank on the end of the cable
(A), must not rotate while adjusting nut
(B).*

After adjusting the nut (B), move the carriage back
and forth several times to redistribute cable tension,
and recheck.

3.4.1.4   PRINT QUALITY ADJUSTMENTS

Certain conditions are necessary prior to making adjust-
ments, they are:

(1)   Power

Power is to be applied to the HyTerm while making
these adjustments. It is used to electrically detent the
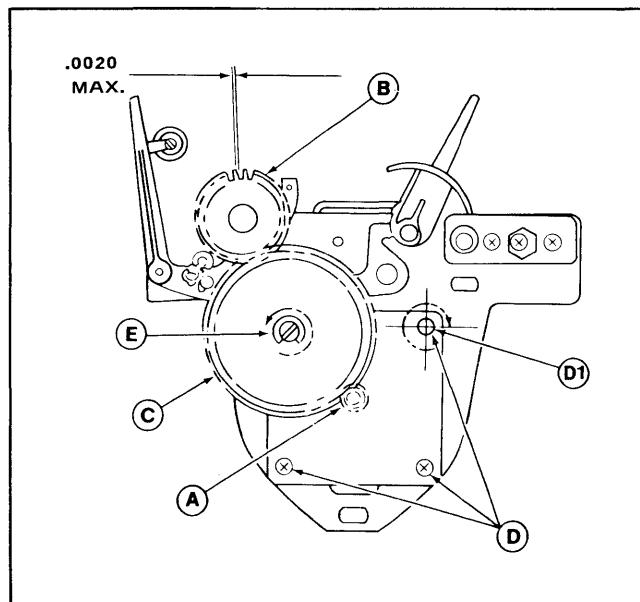
Figure 3-20. Paper Feed (Platen) Drive Adjustments
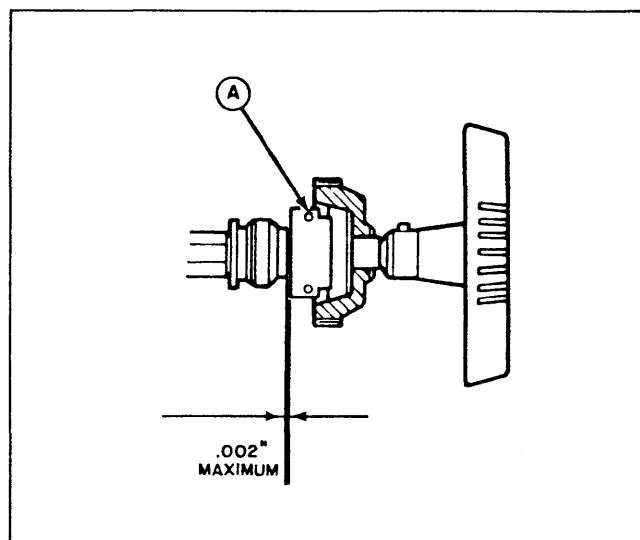
Figure 3-21. Platen Knob End Play Adjustment
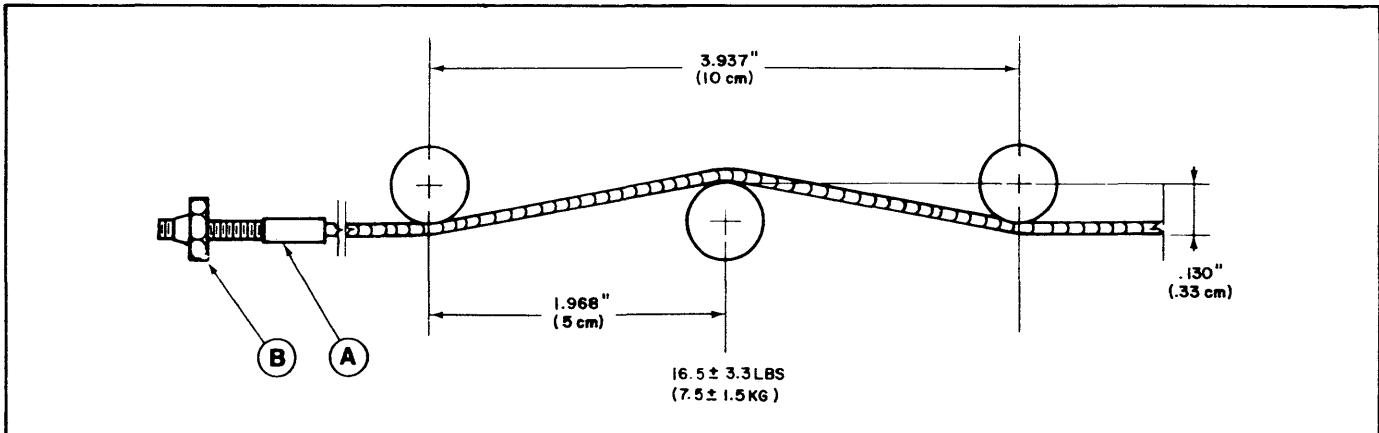
Figure 3-22. Carriage Drive Cable Adjustment

printwheel and carriage servo motors, and for cycling the printer through a Restore sequence when required.

(2) Platen

Platen Carrier adjustments are to be made with a platen installed whose surface is in good condition and free from wear or defects.

(3) Controls

The Platen Position (manifold) lever is to be brought fully forward for these tests and adjustments.

(4) Precautions

Always remove the alignment tool from the printwheel motor shaft before initiating a Restore sequence, to prevent damage to the printer. Also always ensure that the tool is properly seated prior to making any measurement. When it is necessary to move the carriage with the alignment tool installed, first tilt the carriage forward, away from the platen. This will avoid possible damage to the platen.

Either of two alignment tools, 40795 or 40795-01, may be used in making these adjustments. In most cases, the procedures are the same with either tool, but in some cases two separate procedures are listed. The following adjustments are included in this group:

(1) Printwheel-to-Hammer

(2) Platen-to-Printwheel

(3) Platen Height

(4) Card Guide Height and Position

(5) Ribbon

(6) Hammer

(7) Carriage Home

Figure 3-23 identifies the several alignment/adjustment features of the alignment tools by a number-letter designator. These designations are used in the procedures that follow.
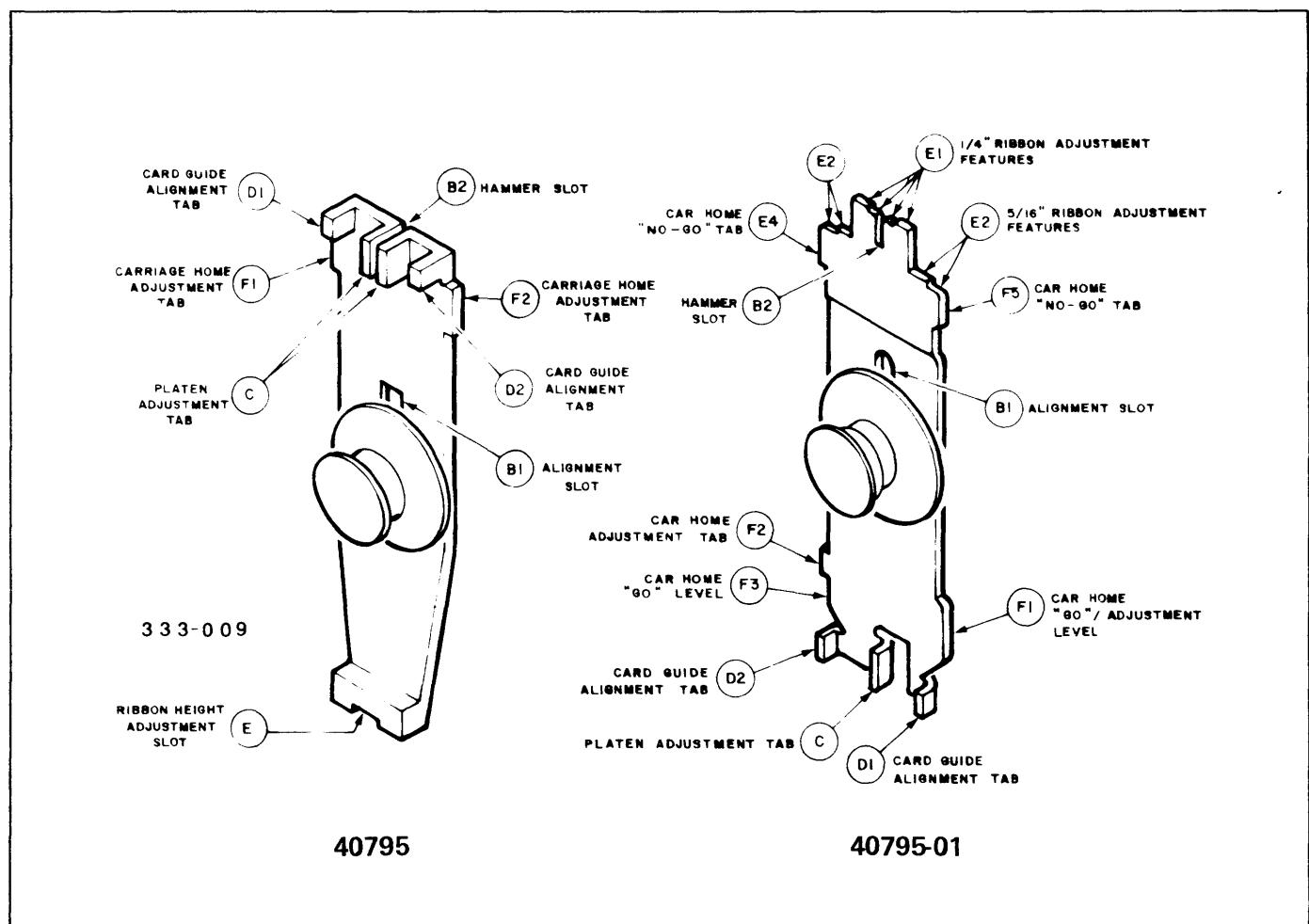
Figure 3-23. Adjustment Tools

CARRIAGE ASSY REF

ADJUSTMENT TOOL
301445-01

ALIGNMENT TOOL
40795-01

333-008
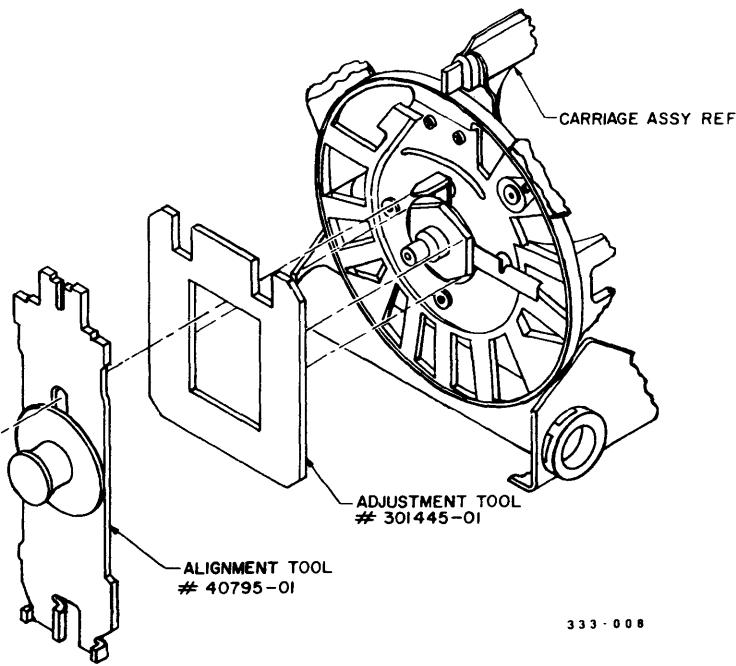
Figure 3-24a Printwheel Alignment

3.4.1.4.1 Printwheel-to-Hammer. Refer to Figures
3-24a and 3-24b. Proceed as follows:

(1) Apply power to the printer and verify completion of
a RESTORE sequence. Remove any paper, the ribbon
cartridge, and the printwheel.

(2) Refer to Figure 3-24a. Install adjustment tool
#301445-01 over the nut on the front of the
printwheel hub. Install alignment tool #40795-XX
firmly on the printwheel motor shaft hub and ensure
that it is properly seated with its alignment slot
engaged over the hub's alignment tab.

(3) Rotate the alignment tool to bring its hammer slot in
front of the print hammer. Block the home sensor by
inserting a piece of dark paper into its slot to detent
the printwheel motor.

(4) Manually push the print hammer toward the platen
until its face enters the alignment tool's hammer slot.
If the hammer slides easily into the slot without
contacting the sides, printwheel-to-hammer alignment
is correct. If the hammer contacts either side of the
slot, or the hammer will not enter the slot, continue
with this procedure.

(5) Refer to Figure 3-24b. Place a screwdriver blade at
point 1 or 2. By twisting the screwdriver you will be
moving the alignment tab in relation to the print-
wheel hub. Move the adjustment tool as necessary to
achieve proper alignment.

CAUTION

*Carriages with the mechanical printwheel
hub DO NOT REQUIRE USE OF ANY
ADHESIVE.*

3.4.1.4.2 Platen-to-Printwheel. Refer to Figure 3-25.
Proceed as follows:

(1) Preparation

NOTE

*It will be necessary to readjust platen height
for print quality, and the card guide after
completion of this procedure.*

(a) Loosen the card guide mounting screws, and
lower the guide as far as it will go.

(b) Tilt the printwheel motor forward, away from
the platen, and install the Alignment Tool.
Make sure the tool is fully seated. Tilt the
motor rearward and verify that the tool clears
the card guide completely. Tilt it forward again.

(c) Place the carriage servo switch, located near the
top edge of the CAR PWR AMP board, slot D,
in its off position.

(d) Loosen the front eccentric on each end of the
carrier assembly, and set each to its mid-range
(lobe facing rearward) with a 7/16 in. open end
wrench. Retighten the eccentric lock screws.

3-22

40795-01

301445-01

①&② SCREW DRIVER ADJUSTMENT POINTS

333-008
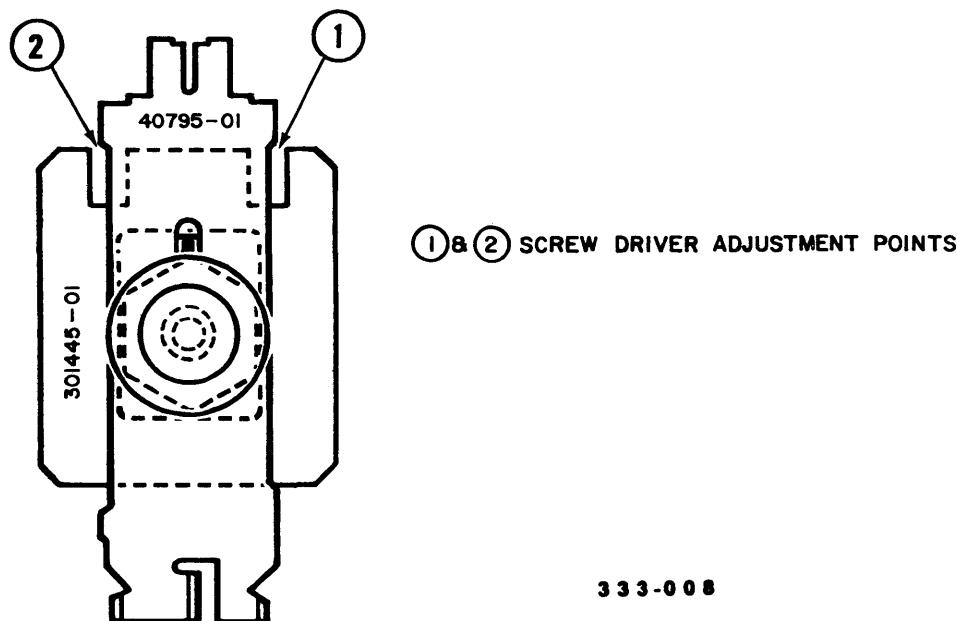
Figure 3-24b. Printwheel Alignment

MANIFOLD
LEVER
FORWARD

PLATEN

AR

AE

ADJUST REAR
ECCENTRIC
(7/16" WRENCH)

FRONT ECCENTRIC
(BOTH SIDES)

TOOL

IDLER GEAR MAY BE REMOVED
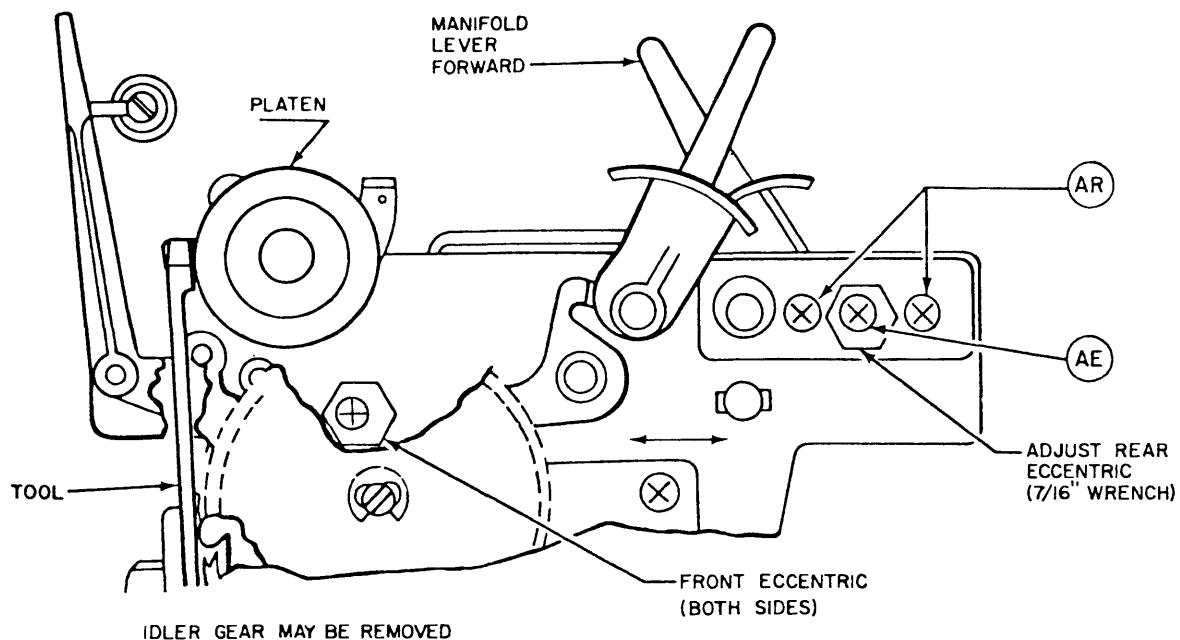
Figure 3-25. Platen-to-Printwheel Adjustment
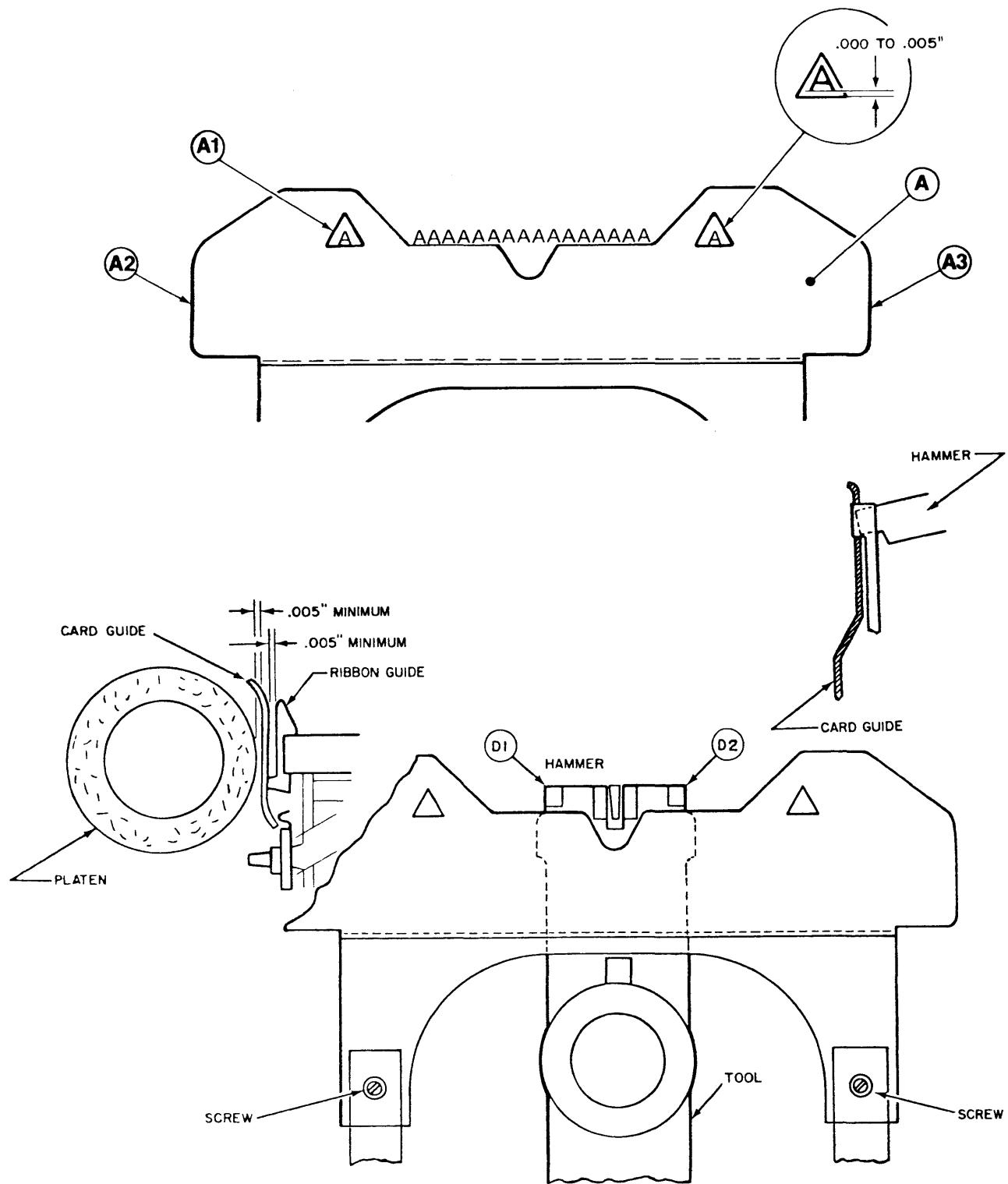
Figure 3-26. Card Guide Adjustments

(2) Alignment Check

Move the carriage as far left as it will go. Tilt the printwheel motor rearward and verify that .0002" - .003" (.005-.076 mm) clearance exists between tabs C of the tool and the platen surface. Tilt the printwheel motor forward (away from the platen) and move the carriage as far right as it will go. Tilt the printwheel motor rearward again, and check the platen-to-tool relationship. If the platen adjustment is within these limits, AND is equal for both ends of the platen, no adjustment is necessary. If these criteria are not met, continue with this procedure.

(3) Platen Adjustment (Repeat for each end)

Loosen the two rear eccentric slide clamp screws (AR) and the screw for the rear eccentric itself (AE). Adjust the rear eccentric, using a 7/16 in. open end wrench, to bring the platen clearance to within the limits specified. Tighten the slide clamp screws. Move the carriage to the opposite end of the platen and check for proper clearance. Repeat these steps until the clearances on each end are within the limits specified, and are equal. Tighten the rear eccentric slide clamp screws when this adjustment has been completed, and then tighten eccentric screws.

When this adjustment has been completed, be certain to perform the Platen Height adjustment (3.4.1.4.3) and the Card Guide adjustment (3.4.1.4.4).

3.4.1.4.3 Platen Height. Refer to Figure 3-25. Proceed as follows:

(1) Preparation

Make sure the Platen-to-Printwheel adjustment (3.4.1.4.2) is correct. Install the printwheel normally used.

(2) Adjustment Check

All characters should print with equal darkness on top and bottom all across the print line. Check with a line of capital "H"s. Refer to the print quality check (3.4.1.1) and Figure 3-6.

(3) Platen Height Adjustment

Loosen the clamp screws on the front eccentric on each end of the carrier assembly. Turn the eccentrics as required to obtain the proper print quality uniformly along the length of the platen. Tighten the clamp screws and recheck the print quality.

3.4.1.4.4 Card Guide Height and Position. Refer to Figure 3-26. Proceed as follows:

(1) Preparation

If the card guide is loose from the preceding adjustment, go on to step (3). If not, remove the adjustment tool, install a printwheel and a sheet of paper, and type a series of identical characters along one line.

(2) Alignment/Adjustment Check

The bottom edge of the triangular openings (A1) must be in line with the bottom lines of a series of identical characters within .000 in. to .0058 in. (.00 mm to .13 mm).

(3) Card Guide Alignment/Adjustment

Install the alignment tool on the printwheel motor shaft, making sure it is firmly seated. The procedure from this point is slightly different depending upon which alignment tool is used. (See Figure 3-23.)

(a) Tool No. 40795:

Push the print hammer into the Hammer Slot B2 on the tool, and hold it there. Raise the card guide gently, until its top edge contacts the undersides of Card Guide Alignment Tabs D1 and D2 with equal pressure. Release the hammer and, while holding the card guide in contact with the tool, tighten the two mounting screws.

(b) Tool No. 40795-01:

Raise the card guide until its top edge contacts the undersides of Adjustment Tool Tabs D1 and D2. Gently move the tool slightly from side to side while raising the card guide until it contacts the tabs with EQUAL pressure. Hold the card guide firmly in this position, and tighten the two card guide mounting screws.

Using a .005 in. plastic shim, check for no-drag shim clearance between the card guide and the ribbon guide posts on both sides of the carriage. Normally, this dimension is set by the depth of the ribbon guide post tabs. Shim drag indicates the card guide has become tilted, in which case its support arms should be gently reformed to achieve proper clearance around the ribbon guide posts.

Using the .005 in. plastic shim, check for no-drag clearance between the card guide and the platen along the full length of the platen.

3.4.1.4.5 <u>Ribbon.</u> Refer to Figure 3-27. Proceed as follows:

(1) Preparation

Remove the ribbon and the printwheel, and rotate the 40795 Alignment Tool to bring Ribbon Height Adjustment Slot E to the Top, or rotate 40795-01 Alignment Tool to bring its Slot B2 to the top with the bottom of the slot to the bottom part of the ribbon. Install a multistrike carbon ribbon cartridge.

(2) Ribbon Adjustment Check

(a) Tool. no. 40795:

The 1/4 in. ribbon can only be used in making the adjustment with this tool.

1/4 in. ribbon:

The TOP EDGE of the ribbon must appear through slot E, but not above the top of the tool.

(b) Tool no. 40795-01:

Either 1/4 in. or 5/16 in. ribbon may be used in making the adjustment with this tool.

1/4 in. ribbon:

The TOP EDGE of the ribbon must appear between the high and low planes of features E1.

5/16 in. ribbon:

The BOTTOM EDGE of the ribbon must appear between the high and low planes of features E2.

(3) Ribbon Adjustment

(a) Adjust the ribbon height eccentric "20" as required to achieve the proper ribbon height by first loosening the 3/16 in. eccentric lock screw on the inside of the carriage frame or the locknut on the outside of the eccentric and then moving the eccentric "20" with a blade
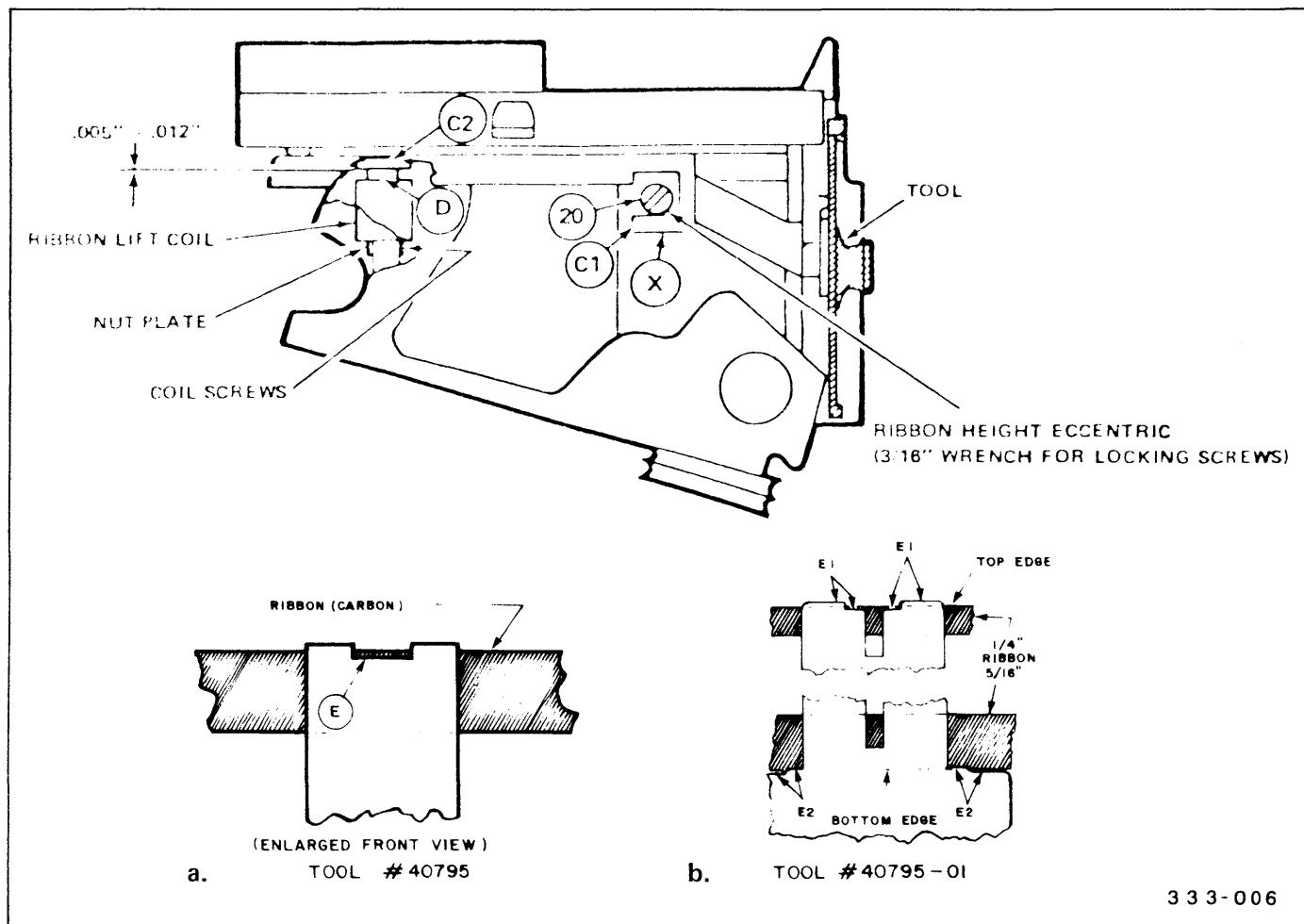
Figure 3-27. Ribbon Height Adjustment

screwdriver or wrench, as required. Retighten the eccentric lock screw.

(b)   Remove the ribbon cartridge. Place a .005 in. plastic shim between the ribbon lift coil laminations "D" and ribbon base plate pole piece "C2". Push up on the ribbon base plate tab "X" so that the grommet "C1" is firmly against the eccentric "20". Energize the ribbon lift coils and check for an even .005 in. gap between the laminations "D" and the pole piece "C2". Loosen the 3/16 in. coil mounting screws and adjust the position of the coils with respect to the pole piece as required to achieve these goals. Retighten the mounting screws and remove the shim.

Recheck the ribbon height (a) as outlined above. Readjust as required, then recheck the coil adjustment (b) if readjustment of the ribbon height was necessary.

3.4.1.4.6   Hammer.   There are two hammer adjustments: hammer coil position and armature stop eccentric. These adjustments are simplified when tool no. 40796 is used, but they can be performed without it if necessary. Refer to Figures 3-28 and 3-29.

(1)   Preparation

The following conditions should be present: power off, printwheel installed, ribbon removed, and platen position lever fully forward.

(2)   Adjustment Check (the Platen-to-Printwheel adjustment, 3.4.1.4.2, must be correct before checking hammer adjustments).

To check hammer coil position, first rotate the printwheel to place one of the larger characters (M, W, E, etc.) in front of the hammer. Then insert H2 of tool no. 40796 (see Figure 3-29) between the armature (A) and the anvil of the print hammer (C), and push the armature against the hammer coils (F). This will force the hammer (C) in to nestle the selected printwheel petal (D) lightly against the platen (E). Gently rock the printwheel slightly back and forth, and verify that the petal can move with a very slight drag. Repeat this check, rotating the platen and/or moving the carriage each time, to check the entire printing surface.

If tool no. 40796 is not available, hold the armature against the hammer coils while pushing the hammer against the printwheel to obtain the relationship noted above, and measure the clearance between the armature and the hammer anvil. It should be .073 in. to .083 in. (1.85 mm to 2.10 mm).
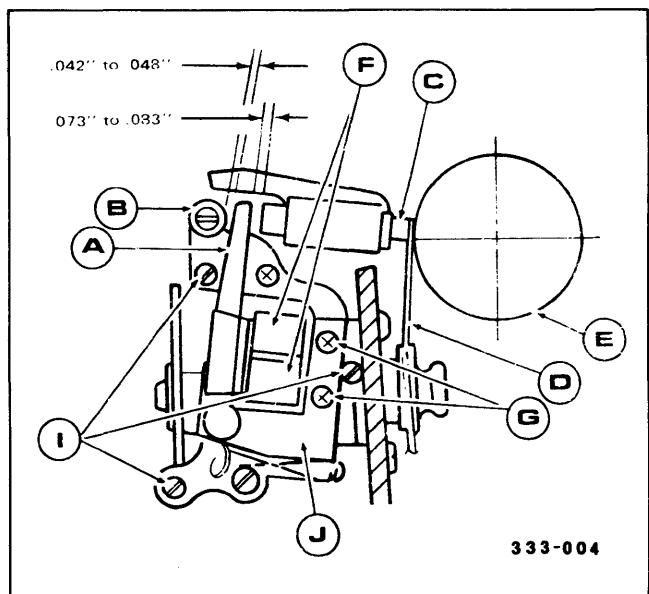
Figure 3-28. Hammer Adjustments
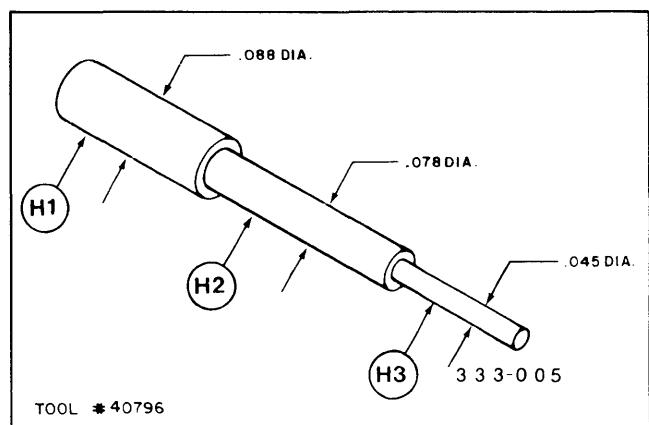
Figure 3-29. Hammer Adjustment Tool

(3)   Hammer Coil Adjustment

Loosen the hammer coil mounting screws (G) and reposition the coils to obtain the proper relationship between the hammer and the platen as noted above. Retighten the screws. Recheck the armature stop eccentric adjustment.

(4)   To check the armature stop eccentric, hold the armature (A) against the hammer coils (F), and check the clearance between the armature and the stop (B). There should be .042 in. to .048 in. (1.07 mm to 1.22 mm) clearance, or H3 of tool no. 40796 should fit with very light resistance.

(5)   Armature Stop Eccentric Adjustment

Loosen the lock nut slightly, and turn the screw until the desired clearance is obtained. Prevent the screw from turning as the lock nut is retightened.

3.4.1.4.7 Carriage Home (Figure 3-30)

(1) Preparation

With power applied to the printer, initiate a Restore sequence.

(2) Adjustment Check

    (a) Tool No. 40795:

Insert the tool between the left side of the printer's main frame casting and the carriage frame, just above the carriage home sensor. The maximum clearance between tool Tabs F1/F2 and the printer assemblies should be .017 in. (.43 mm).

    (b) Tool No. 40795-01:

Insert the tool between the left side of the printer's main frame casting and the carriage frame, just above the carriage home sensor. Using tool tabs F1-F5, check for proper clearance as follows:

Tabs F1/F3 should pass (go)
Tabs F4/F5 should not pass (no go)

(3) Carriage Home Sensor Flag Adjustment

Unlock the carriage home sensor flag eccentric, and adjust it to move the flag LEFT for "not enough" clearance, or RIGHT for "too much" clearance. After each movement of the eccentric, remove the align-ment tool, turn off power, move the carriage to the right, restore power, and cycle the printer through the RESTORE sequence. When this adjustment is being changed, try to achieve a clearance as close as possible to tool Tabs F1/F2 (either tool). Tighten the eccentric clamp screw when the adjustment is complete.

3.4.1.5 BOTTOM-FEED PAPER CHUTE (Figure 3-31)

This is an optional feature, not found on all HyTerms.

(1) Preparation

    (a) Make sure the following adjustments are correct:

Paper Feed Rollers	3.4.1.2.2
Platen Position	3.4.1.4.2
Platen Height	3.4.1.4.3
Card Guide	3.4.1.4.4

    (b) Turn off power. Raise or remove the access cover, and remove the platen. Remove any paper.

(2) Adjustment Check

    (a) The top edge of the paper chute (B) must be in line vertically within .030 in. (.76 mm) of the top 45-degree bend of the card guide (C). This must not vary more than .030 in. (.76 mm) over the entire length of the carriage travel.

    (b) There should be .040 in. to .060 in. (1.0 mm to 1.5 mm) clearance between the paper chute and
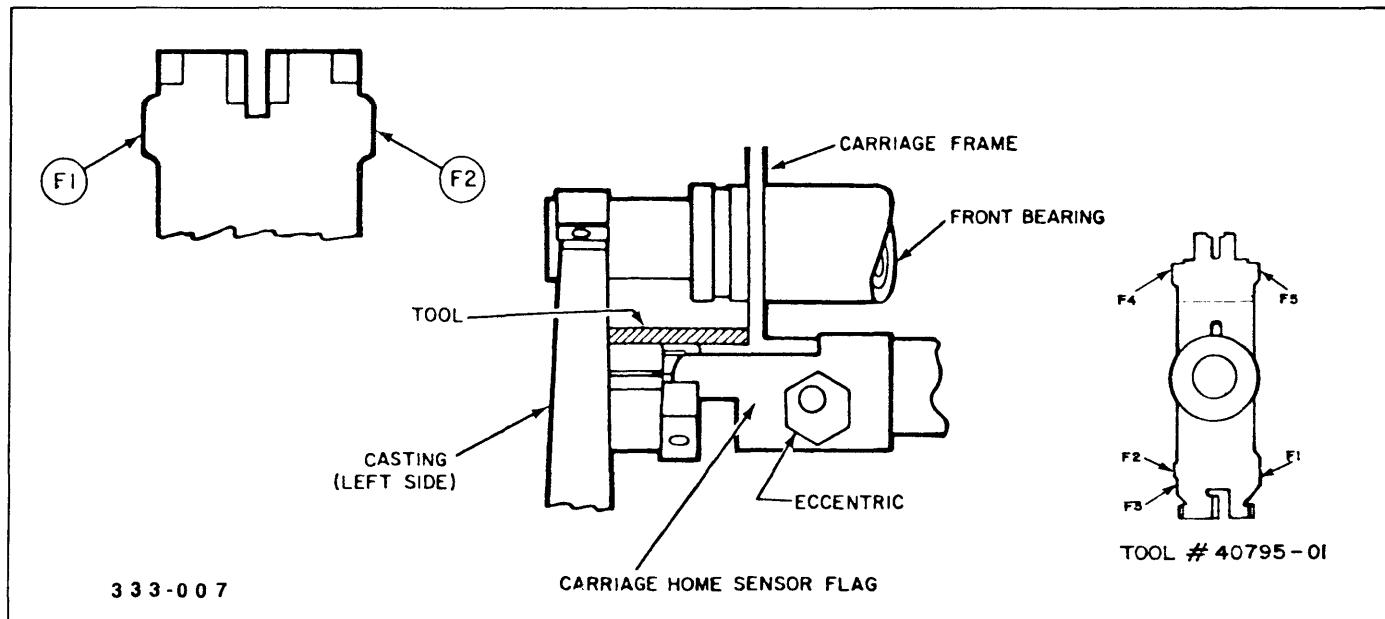
Figure 3-30. Carriage Home Adjustment

the front pressure rollers. Clearance should be equal at both ends.

(c) The paper-out bail should touch the chute at both ends.

(3) Paper Chute Adjustments

NOTE

If any of these adjustments are performed, be certain to check the bottom-feed paper-out switch adjustment (3.4.6.2).

(a) To adjust the height of the chute, loosen screws (D) and (F), position the chute properly, and tighten screws (D). Then perform adjustment (b).

(b) To adjust the paper chute/pressure roller clearance, loosen screws (F), position the chute properly, and tighten screws (F).

(c) To adjust the paper-out bail, loosen the setscrews in the hubs at both ends of the bail, form the bail slightly, if needed, and tighten the setscrews.

3.4.2 Control Panel

The only adjustment on the control panel is a volume control adjustment for the audible alarm.

3.4.2.1 VOLUME CONTROL

Remove the access cover from the HyTerm. With a small screwdriver, turn the adjusting potentiometer until the desired volume is obtained. The potentiometer is accessible through a hole in the right side of the control panel near the buzzer. To sound the audible alarm after each adjustment, operate the RESET key and then attempt to print a character. The alarm will sound for a cover-open error.

3.4.3 Power Supply

The most common adjustment procedure of the power supply is the +5 voltage adjustment. In the Boschert power supply, there is one additional adjustment procedure following the replacement of the U3 opto-coupler. On the LHR power supply, there are two additional adjustment procedures — overvoltage protection, and current limit.

All voltages should be checked whenever the power supply or one of its components is replaced, when one of the voltage regulator ICs on the HPRO board is replaced,
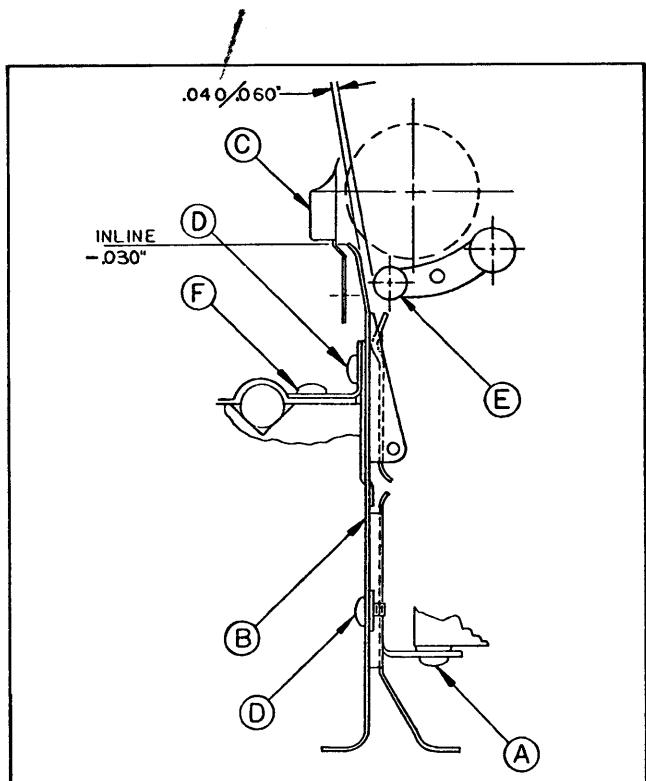
Figure 3-31. Paper Chute Adjustment

and any other time that power supply problems are suspected. The tolerances given in the following procedures are for adjustment purposes only. That is, if a voltage is slightly outside the limits listed, but the HyTerm is operating properly, no adjustment is required. On the other hand, if a voltage is within the specified limits, but at the fringe, and power supply problems are suspected, perform the +5 voltage adjustment. The use of a digital voltmeter is recommended because of the more precise readings obtainable. Proceed as follows:

+5V Adjustment Procedures: (Both Boschert and LHR Power Supplies)

(1) Unplug the HyTerm from its power source. Raise or remove the access cover, remove the platen, and remove the top cover (3.1.2).

(2) Remove the HCURL board (if installed) from slot (F) and install a circuit board extender into slot (F).

(3) Plug the HyTerm power cord into the wall outlet.

WARNING

When the HyTerm is connected to a power source, line voltage is present at the POWER switch terminals. To avoid a dangerous shock when power is applied with top cover removed, keep your fingers away from the POWER switch terminals.

Turn on the power and measure each voltage.

Spade Lugs*	Extender Pins	
T13-T14*	Pins 1-2	GND
T15*	Pins 5-6	+5.0V ± .1V
T12*	Pins 41-42	+15.25V ± .75V
T11*	Pins 23-24	-15.25V ± .75V

*If the machine is equipped with mother board 46080-XX, these voltages may be measured at the dc power spade lugs on the right side of the mother board.

(4)   If the +5 volt supply is correct and some other supply is not, a malfunction is present and must be corrected. If the +5 volt supply is not correct, proceed with step (5).

(5)   Turn off the power. Tilt the HyTerm up so that it is resting on the rear edge of its bottom cover.

CAUTION

When tipping the HyTerm up, be certain to use a flat surface, with no foreign objects in the way. Any small objects could cause pressure to be applied to the rear heat sinks, which are mounted on the power amplifier boards. Excess pressure on these boards could damage the boards and/or the mother board.

CAUTION

Whenever the HyTerm is tilted up in this manner, hold on to it with one hand to prevent it from falling over.

(6)   Remove the screen-like bottom pan from the HyTerm by loosening the rear three screws, removing the remaining five screws, and lifting the bottom pan off the machine.

(7)   Fasten the voltmeter probe firmly to the +5V measuring point.

```
WARNING

In the following step, be very careful not to
touch any part of the power supply, because
extremely high voltages (200 - 300 volts) are
present.
```

(8)   Turn on the power. Using a non-metallic screwdriver, adjust the power supply potentiometer to provide +5 volts ±.1 volt.

(9)   If any 15 volt measurement is still outside its tolerance after the +5 volt supply has been adjusted properly, the source of the problem must be located; either the power supply is defective, or some printer malfunction is causing an unusual current drain. A current foldback condition in any supply will affect the other outputs as well.

(10)   Turn off the power. Replace the bottom plate. Tilt the HyTerm back down onto its feet, remove the board extender, replace the top cover and the platen. Test the HyTerm for proper operation.

3.4.3.1   Boschert Power Supply, Part No. 26021-XX

Procedures following replacement of U3 opto-coupler:

(1)   Follow the procedures (1-7) for removal of power supply (3.3.2).

(2)   Fasten one voltmeter probe on TB1-2 (GND) and the other probe at the junction of R35, R36, and U3-2. (See Assy. Dwg. 26021-XX for exact location.)

```
WARNING

In the following steps, be very careful not to
touch any part of the power supply, because
extremely high voltages (200-300 volts) are
present.
```

(3)   Turn on the power.

(4)   The voltage across R35 is directly proportional to the resistance. The value of R35 may vary from 680 ohms to 2.4K ohms, 1/4 Watt 5%.

(a)   Increase the resistance of R35 if the voltage drops below 1 volt when the +5V output is 8 amps (fully loaded).

(b)   Decrease the resistance of R35 if the voltage exceeds 2 volts when the +5V output is 2 amps (minimum load).

(5)   After resistance of R35 is corrected, proceed to steps (1-5) of replacement of power supply (3.3.2).

3.4.3.2   LHR Power Supply, Part No. 400062-01

These adjustments are performed at the factory and under normal conditions do not require field adjustment. These adjustments may be required if a problem is suspected or a component in the power supply has been replaced.

Overvoltage Protection:

(1)   Disconnect the power supply outputs from the terminal and connect a dummy load to the +5V output which draws approximately 1 amp.

(2)   While monitoring the +5V output, adjust potentiometer R22 clockwise and note the maximum voltage

obtainable (after which the overvoltage circuit takes over and causes the output to drop). This should be between +5.5V and +6.3V, preferably around +6.0V.

(3) Adjust potentiometer R23 on the control module (the small circuit board attached to the power supply's main circuit board) clockwise to trigger the overvoltage circuit at a higher point, or counterclockwise for a lower point.

NOTE

If the output reaches +6.3V before triggering the OVP circuit, the SCR "crowbar" circuit may trigger, requiring removal of the input power before the power supply can restart. If this occurs, turn off power, turn pots R23 on the control module and R22 both counterclockwise slightly, restore power, and continue the test as described.

Current Limit:

(1) This adjustment should be made with the input voltage at a nominal value (115V or 230V) — not at either of its extremes.

(2) The outputs should be loaded so that the power supply delivers about 320 watts of total power for no longer than 30 seconds while making this adjustment.

(3) Adjust potentiometer R19 until the output begins to drop off at the 320 watts total power point.

3.4.4   Keyboard

The only keyboard adjustment is the positioning of the keyboard for proper top cover fit. This is normally required only when the keyboard has been removed or when a different top cover is installed. This adjustment entails trial-and-error positioning of the keyboard followed by installation of the top cover. See 3.3.4 for details.

3.4.4.1   KEYSWITCHES

One of the failure modes of the Keyboard is a leaky output of the keyswitches. This failure produces intermittent operation of the keyboard by holding one of the encoder inputs (U3) low. With one input low, only the keyswitches that have that line in common will function. In this case, one of the functioning keyswitches is defective.

Even though this failure mode is intermittent, it may be isolated when the keyboard is functioning. A leaky keyswitch can be identified by measuring the voltage at the encoder inputs (pins 1 through 13 on U3) with respect to +5V using a digital voltmeter. Typically, the meter will read

between -14mV and -22mV. Pins 1 and 2 are about 1mV lower than the others due to the repeat circuitry tied to these lines. A leaky keyswitch will load the encoder input line causing a greater voltage drop. Also, the encoder line in question will be electrically noisy if looked at with an oscilloscope.

Normally, the greater voltage drop can be seen immediately after power up, but occasionally power may have to be applied for up to an hour to exhibit the leakage problem.

After identifying the encode line with the defective keyswitch, all of the keyswitches common to that line should be replaced. See 3.3.4.1 for keyswitch removal.

3.4.5   Cover-Open Switch

Before making any adjustment, be sure that the top cover fits the bottom cover properly, and that the access cover fits the top cover properly and is tight. Adjust and/or form the access cover clamp springs (replace if necessary) to tighten the access cover. If switch adjustment is still necessary, loosen the cover-open switch operating bracket (fastened to the inside lower edge of the access cover), move the bracket up or down slightly, and retighten the lock screw. Check the adjustment by making sure the switch operates each time the access cover is opened or closed.

3.4.6   Paper-Out Switch

The procedure for adjusting the paper-out switch varies, depending upon whether the standard top-feed or the optional bottom-feed paper supply is used.

3.4.6.1   TOP-FEED

This switch is functional only when a forms tractor or pin-feed platen is used. When a friction-feed platen is used (without forms tractor), the switch is held in its non-operated (paper in) position by the paper release lever's being in its rearward position. When the paper release lever is moved to its forward position, the switch operating mechanism is unlocked and allowed to sense the paper-out condition.

Before starting this adjustment, be certain that the Paper Feed Rollers adjustment (3.4.1.2.2) and the Platen Position (3.4.1.4.2) and Platen Height (3.4.1.4.3) are correct. Perform the adjustment with the platen installed and the paper release lever in its rearward position (pressure applied). Referring to Figure 3-32, proceed as follows:

(1) Using a .050 in. Allen setscrew wrench, loosen the setscrew (1) in the bell crank on the end of the paper-out bail pivot shaft (2). The front edge of the
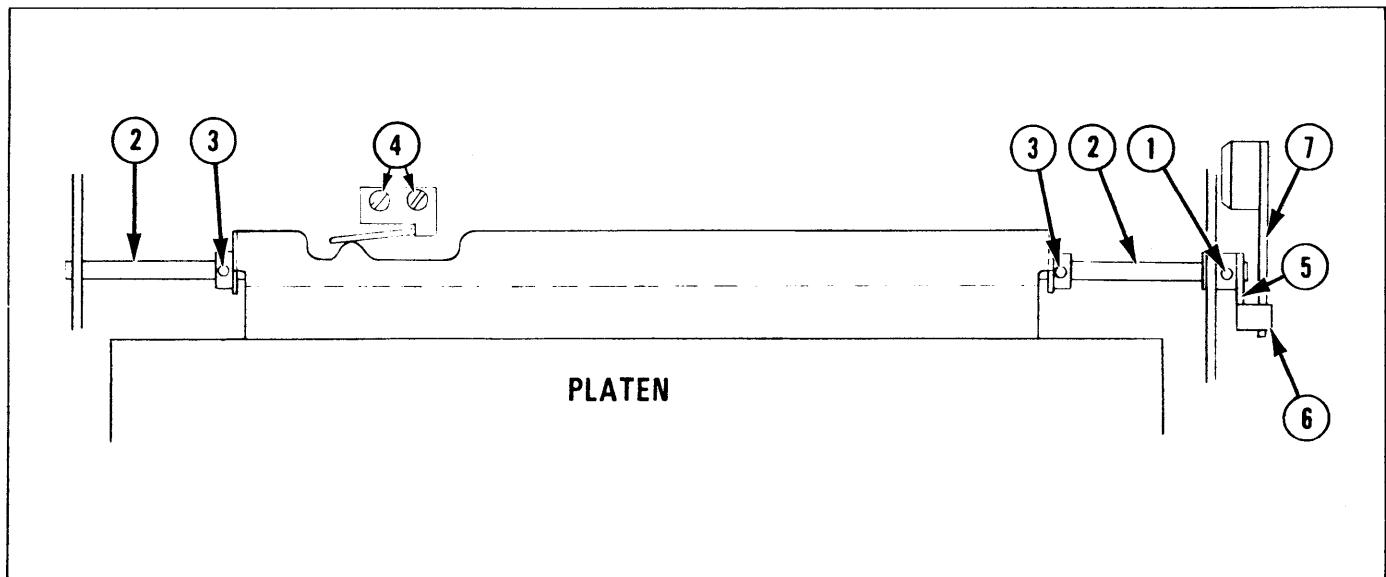
Figure 3-32. Paper-Out Switch Adjustment

bail should touch the platen surface squarely within .003 in. (.08 mm). [A gap of .010 in. (.25 mm) maximum due to bowed paper-out bail is permissible.] If necessary to adjust, loosen the setscrew (3) at either end (or both), adjust, and tighten the screw(s).

(2) Loosen the switch mounting screws (4), and adjust the switch to transfer when the bail is .010-.020 in. (.2-.5mm) away from the platen. Tighten the screws.

(3) Move the bail back away from the platen fully. The bail legs must bottom against the printer "comb" frame, and not against the switch. If necessary, form the switch arm to allow the switch to transfer sooner, and reposition the switch to obtain the proper adjustment as noted in step (2).

(4) Remove the platen, and move the bail rearward until its legs come within .030 in. (.76 mm) of the comb. Hold the bail in this position and rotate bellcrank (5) until its ear (6) rests against the actuator lever arm (7). Tighten setscrew (1). After tightening the screw, the shaft (2) should pivot freely with .005 in. (.13 mm) maximum end play. Install the platen, move the pressure release lever back and forth several times, and stop with the lever in the rearward position. There must be at least .090 in. (2.3 mm) clearance between the bail and the platen.

3.4.6.2 BOTTOM-FEED (OPTIONAL)

This switch is functional only when the enable/override switch, mounted to the left of the front carriage rail, is in the ON position (toward the rear). When the enable/override switch is OFF, it overrides the paper-out switch, making it non-functional.

Before adjusting the bottom-feed paper-out switch, make sure the Bottom-feed Paper Chute (3.4.1.6) is adjusted properly.

The paper-out switch should transfer when the paper-out bail is .025-.040 in. (.63-1.0 mm) away from the front paper chute. Loosen the switch mounting screws and reposition the switch to obtain this adjustment. Tighten the screws. If adjusting the switch limits the movement of the paper-out bail to less than .100 in. (2.5 mm), form the switch arm to allow the switch to transfer sooner, and reposition the switch to obtain the proper adjustment.

3.5 COMPONENT IDENTIFICATION

There are two methods used to identify components within the HyTerm. The first is an extension of the reference designator system used to identify replaceable modules (Section 3.3). The second is a coordinate system used to identify components on the plug-in circuit boards. Also, closely related to component identification is the location of connectors and the numbering of connector pins.

3.5.1 Reference Designator System

The reference designator system is used to identify individual components mounted to the printer frame, as well as components on the control panel, in the power supply, and on the keyboard. Table 3-3 defines the class letters used on schematics and wiring diagrams to refer to various items. On the control panel and keyboard, the reference designators for each component are etched on the circuit board. To locate a particular component in the power supply, you will first need to locate it on the power supply assembly drawing, and then find it on the power supply.

Table 3-3. Reference Designators

Designator	Description
A	Assembly
B	Fan (blower)
C	Capacitor
CR	Diode (including bridge rectifiers, LEDs)
DS	Alarm (buzzer)
E	Individual terminal
F	Fuse
FL	Filter
J	Jack (connector, stationary portion)
L	Inductor (coil)
P	Plug (connector, movable portion)
Q	Transistor
R	Resistor
RT	Resistor, temperature-sensitive (thermistor)
S	Switch
T	Transformer
TB	Terminal board
TP	Test point
U	Integrated circuit
VR	Voltage regulator (zener diode)
W	Cable
X	Circuit board socket, fuseholder

3.5.2   Coordinate System

Components are identified on the logic drawings as to type and location. The location information consists of a letter and a number, each representing coordinates on the circuit board. Refer to Figure 3-33. Letters are printed on the circuit board in the approximate center of the area they refer to, whereas numbers appear at the beginning of their respective area. As an example, to locate resistor E62, follow the "E" row horizontally to where it intersects the "60" column. Below the "60" and a little to the right (at "62") you will find resistor E62. Coordinates given for IC chips are the approximate location of pin no. 1. Coordinates for other "horizontally mounted" components (as in Figure 3-33) refer to the location of the leftmost lead. Letter coordinates for vertically mounted components that overlap rows usually refer to the row in which the largest portion of the component is located.

NOTE

When locating components on the HPRO1 board, note that the alphabetic coordinates are opposite that shown here. "A" is at the plug end of the board.

Pin no. 1 of each IC is easily identified from the bottom (solder) side of the board by its square solder pad. This lessens the chance of errors in counting pin numbers.

The mother board, the keyboard, and the control panel circuit boards do not use the coordinate system because of the small number of components involved. These boards use standard reference designators, which are silkscreened or etched onto the board, and referenced on the schematics.

3.5.3   Pin Numbering

Industry standards are followed for pin numbering of integrated circuits. Pin identification for all integrated circuits, including metal-can ICs, can be found in Section 4.

3.5.3.1   DISCRETE SEMICONDUCTORS

Pin identification for most discrete semiconductors is presented in Figure 3-34.

NOTE

Components in Figure 3-34 that are listed by Diablo part number should not be replaced by standard industry types. They should be ordered by Diablo part number because in some cases there are more stringent tolerances for the Diablo parts, and restrictions as to approved manufacturers, due to reliability and functional differences.

3.5.3.2   CIRCUIT BOARDS AND MOTHER BOARD

Pin numbering of circuit boards that plug into the left-hand half of the HyTerm is shown in Figure 3-33. Circuit boards on the right side are mirror images, so pin no. 1 is on the left side; pin no. 56 on the right. This is also shown in Figure 3-35a and b.

The numbering of all mother board pins is shown in Figure 3-35a and b. Signal names for all points, including power connections, are shown on schematic no. 40614 and 46080, respectively.
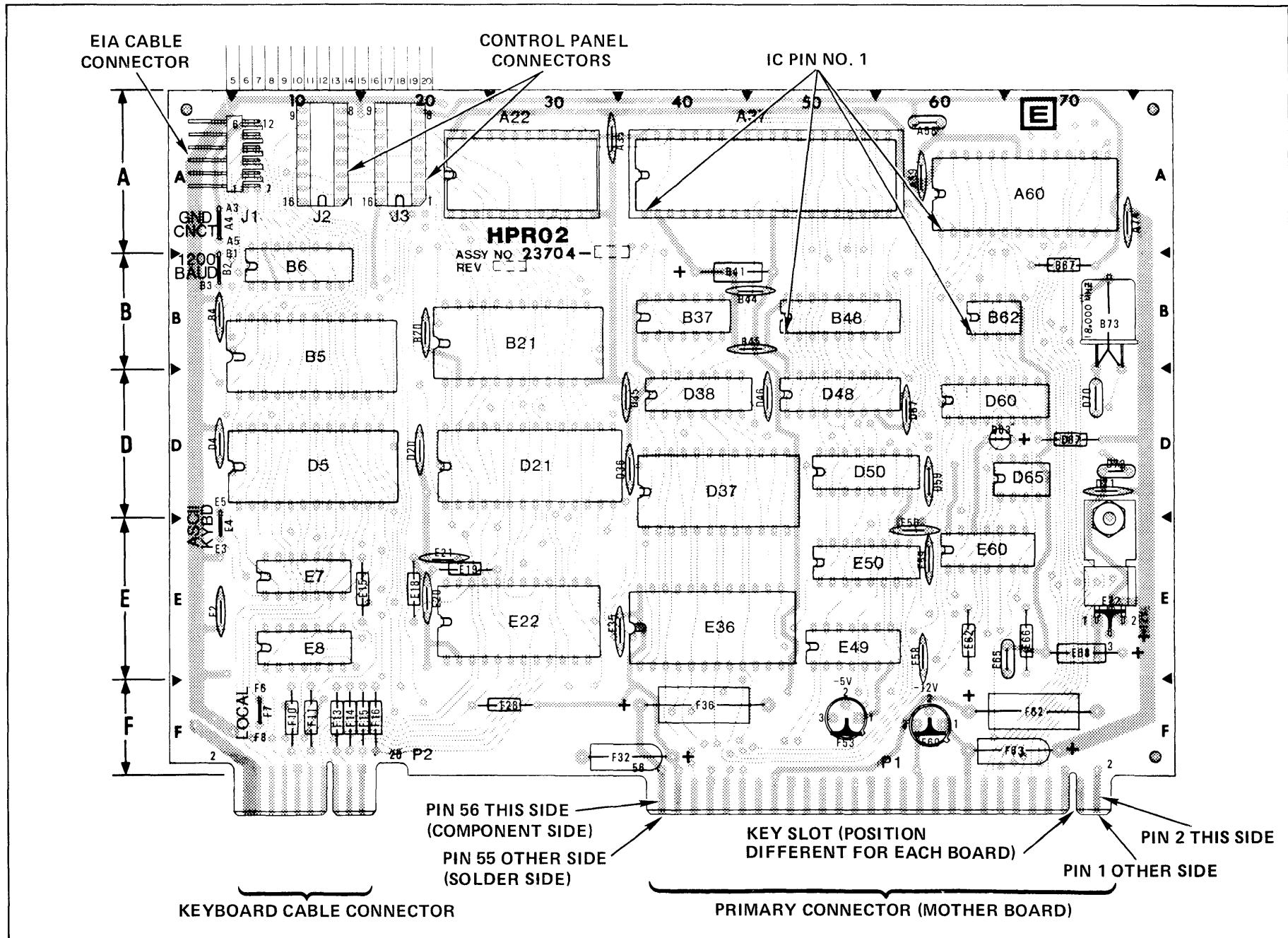
Figure 3-33. Circuit Board Component Location and Pin Numbering
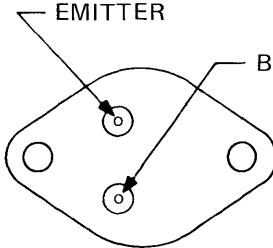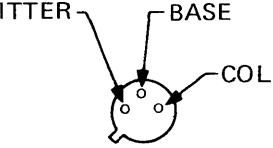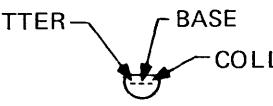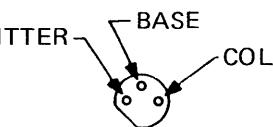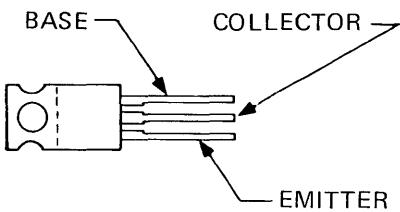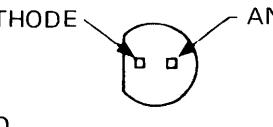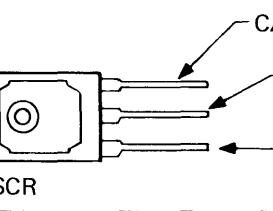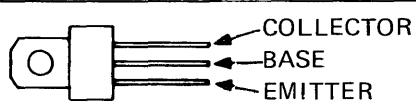
OUTLINE (BOTTOM VIEW)	DIABLO PART NUMBER	INDUSTRY TYPE NUMBER
EMITTER BASE (COLLECTOR CONNECTED TO CASE)	180013-01 180013-01 42190-29 42190-30 USE SJ7280 USE 2N6545 USE SJ7280 42190-71	CPS1540B (Matched Pair) SJ6211 (Matched Pair) SJ7280 SJ7280 (Matched Pair) 2N6306 (SJ7280) 2N6308 2N6544 2N6545
EMITTER BASE COLLECTOR	42220-01 42190-72 10422-01 10443-01 10444-01	2N2219A 2N3439 2N3725 2N5320 2N5322
EMITTER BASE COLLECTOR	10105 42190-26 13013 42190-21 USE MPS-U60 42190-28 42190-60	2N3644 2N4126 2N4401 MPS-A43 MPS-A93 MPS5172 MPS6516
EMITTER BASE COLLECTOR	10105	2N3644
BASE COLLECTOR EMITTER	10445-01 10177-02 13063 13064 42190-27 42190-70 13007	2N6103 TIP31A TIP41A TIP42A TIP47 TIP49 TIP125
CATHODE ANODE (+) LED	14005-01	MV5753
CATHODE ANODE GATE SCR	42190-43	C122F (50316)
COLLECTOR BASE EMITTER	42190-25	MPS-U60

Figure 3-34. Semiconductor Lead Identification
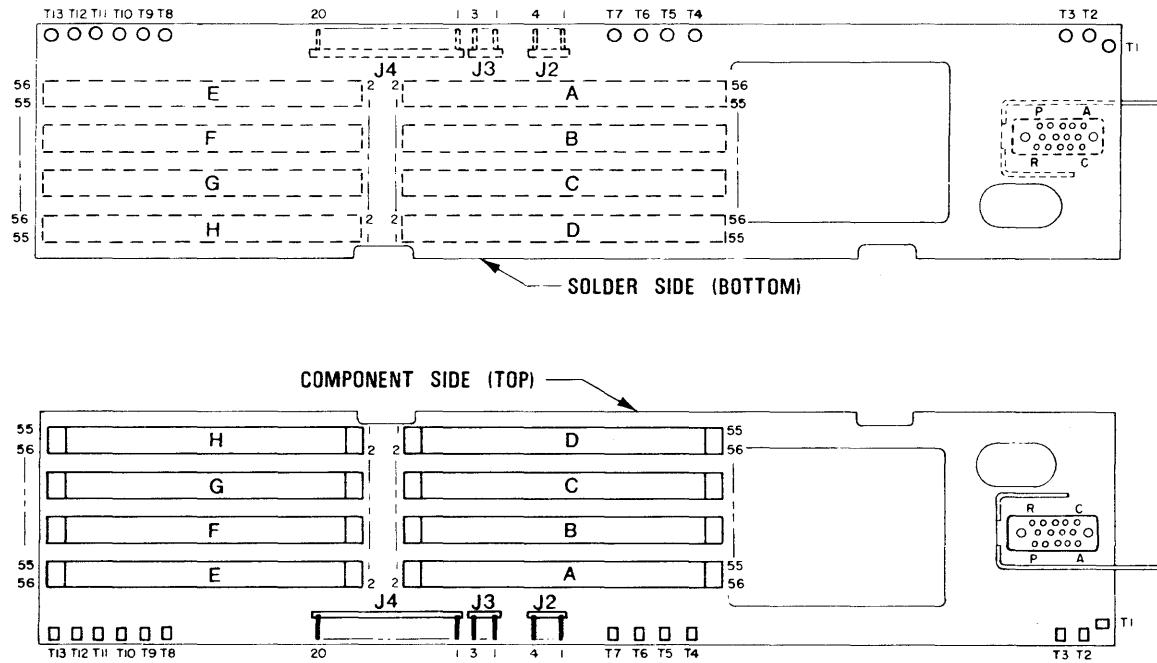
Figure 3-35a. Mother Board Pin Numbering (No. 40614)
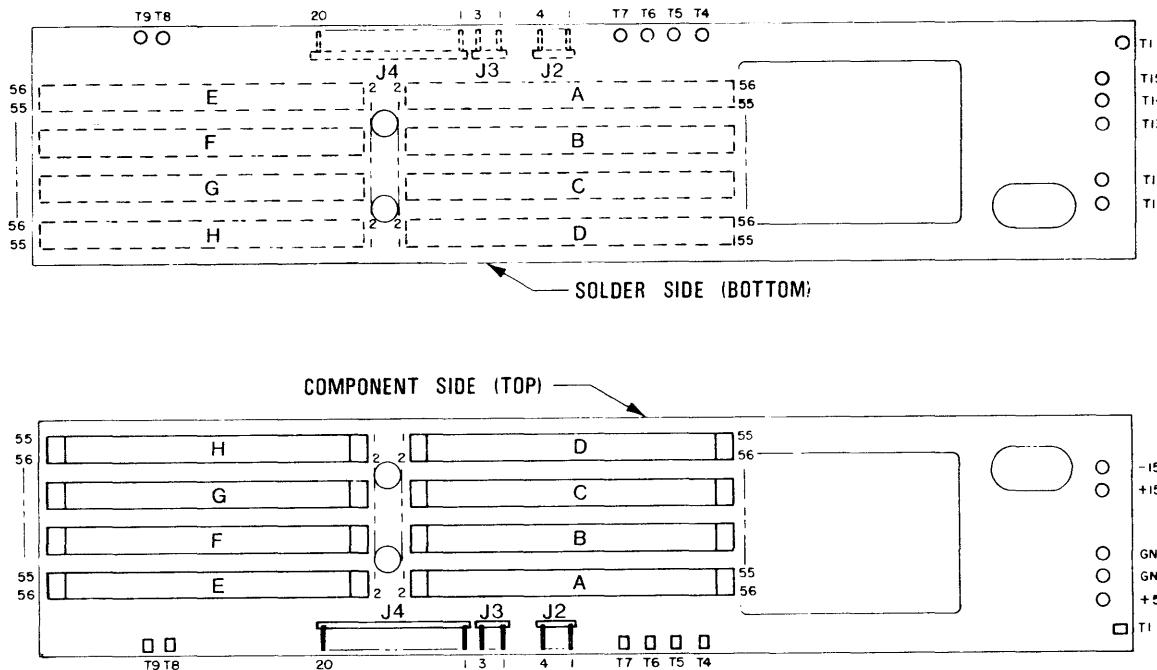
Figure 3-35b. Mother Board Pin Numbering (No. 46080)

3-36

3.5.3.3 KEYBOARD CABLE

Pin numbers are shown in Figure 3-36. Pin numbers and signal names are the same at both ends. Odd-numbered pins are on the top (component side) of the keyboard and the back (solder side) of the HPRO board; even-numbered pins are on the bottom (solder side) of the keyboard and the front (component side) of the HPRO board. Signal names are listed in Table 3-4.

Table 3-4. Keyboard Signal Names

Pin No.	Signal Name	Function
1	+5V	
2	SIGNAL GND	
3	+5V	
4	SIGNAL GND	
5	-FKY4	Shift
6	-FKY5	Control
7	-FKY1	Upper Case Only
8	-FKY2	Local
9	+BUSY	
10	-FKY3	Break
11	-12V	
12	+KYSTB	
13	-DATA0	
14	-DATA7	
15	-DATA6	
16	-DATA1	
17	-DATA5	
18	-DATA2	
19	-DATA4	
20	-DATA3	
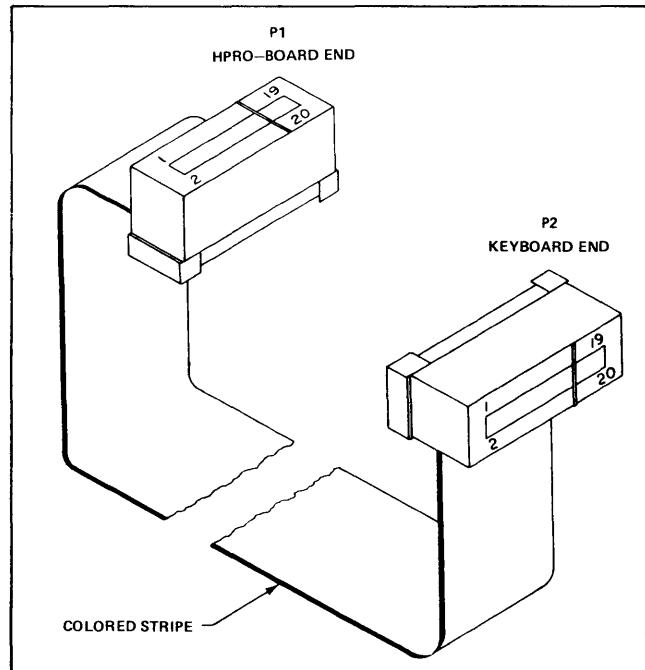
Figure 3-36. Keyboard Cable

3.5.3.4 CONTROL PANEL

The two control panel cables are permanently mounted to the control panel circuit board. The control panel schematic (23708 for HPCPL or 23710 for HPCPN) shows the wiring of both the circuit board and the cables. Note that cable W2 is stamped with a "2" and plugs into socket J2 on the HPRO board, and that cable W1 is stamped with a "3" and plugs into socket J3 on the HPRO board. The sockets are the same as 16-pin integrated circuit sockets, and the pins are numbered the same. Pin no. 1 is identified in several ways: by the square solder pad on the solder side of both the HPRO board and the HPCPL/HPCPN boards, by the angle or dot on one corner of the sockets on the HPRO board, and by the red-painted edge of the flat ribbon cable. Numbers progress from 1 to 16 counterclockwise when viewed from the component side of any circuit board; clockwise when viewed from the solder side. Figure 3-37 shows the numbering of the pins on the end of the control panel cables.

Signal names for these cables are shown on the control panel schematics and on the Signal Cable Interconnection Diagram, no. 23732.
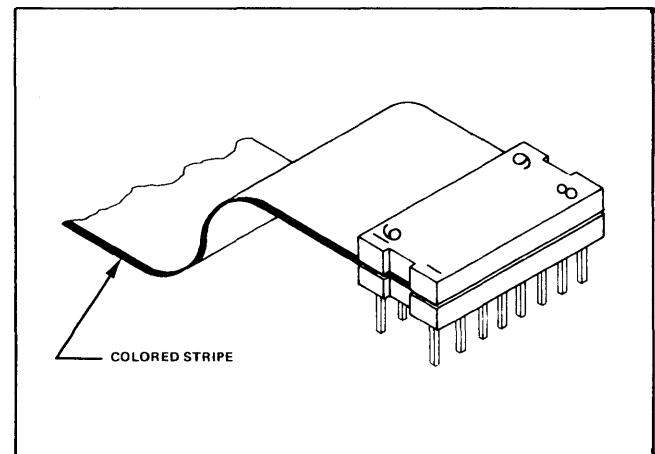
Figure 3-37. Control Panel Cable Pin Numbering

3.5.3.5 EIA CABLE

Complete information on the wiring of the EIA cable is given in Figure 3-38. Note that the male EIA connector is shown; the female connector on the modem or acoustic coupler is a mirror image of this. Note also that the J1 connector on the HPRO board is a mirror image of the P1 connector shown.

3.5.3.6 POWER SUPPLY

Figure 3-39 shows the wiring of the power supply cable and the connections to the power supply. Note that there are some unused pins in the female connector (P1), but that the J1 connector on the mother board that mates with it has all pins connected in some manner. The mother board schematic, no. 40614, lists all power connections.
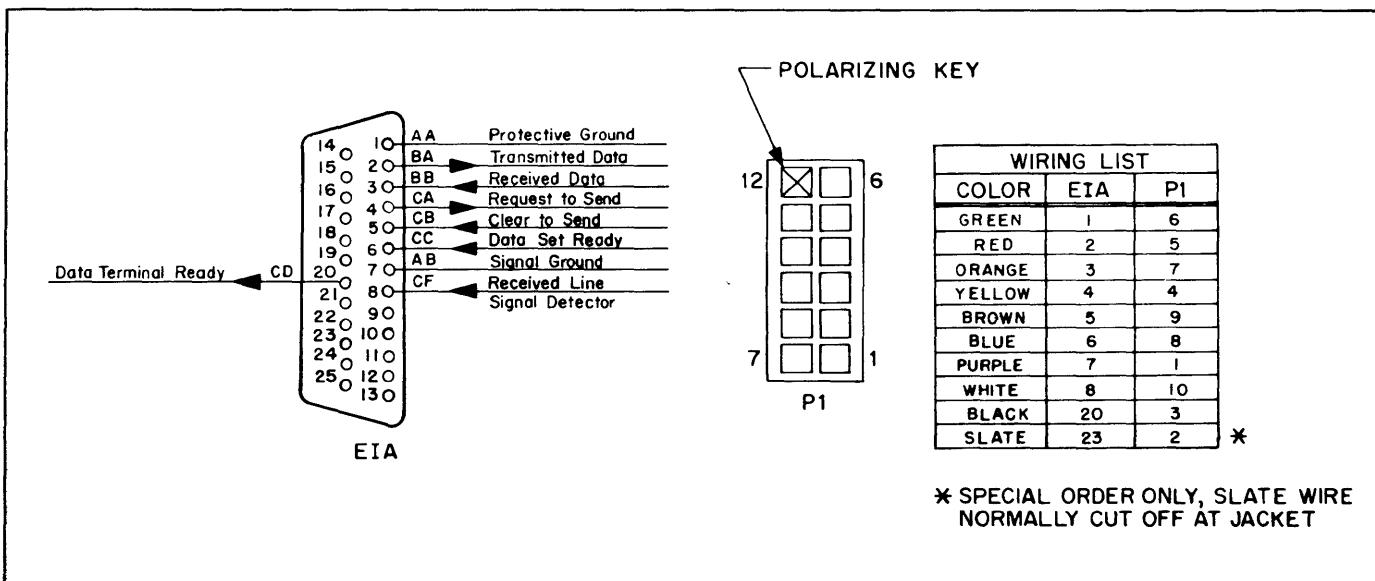
Figure 3-38. EIA Cable Pin Identification

WIRING LIST		
COLOR	EIA	P1
GREEN	1	6
RED	2	5
ORANGE	3	7
YELLOW	4	4
BROWN	5	9
BLUE	6	8
PURPLE	7	1
WHITE	8	10
BLACK	20	3
SLATE	23	2

✳ SPECIAL ORDER ONLY, SLATE WIRE NORMALLY CUT OFF AT JACKET
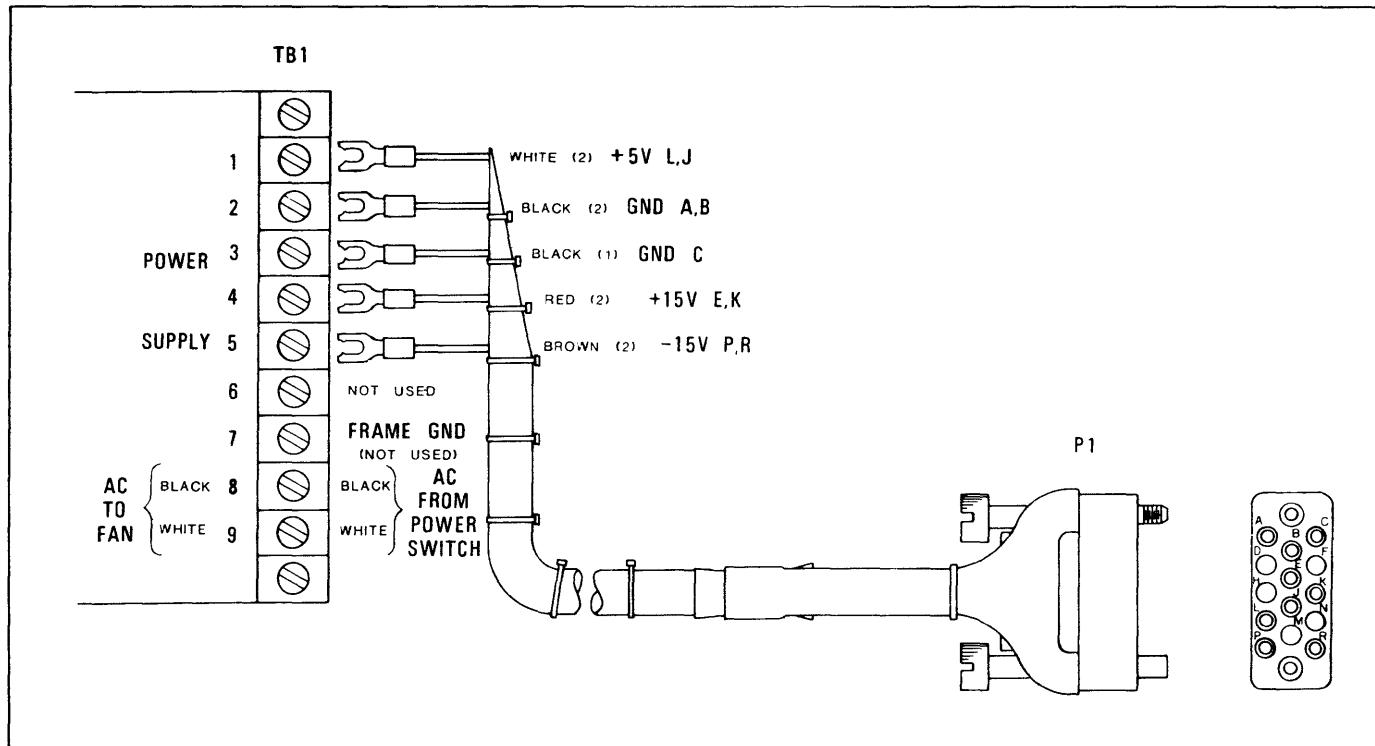
Figure 3-39. Power Supply Connections
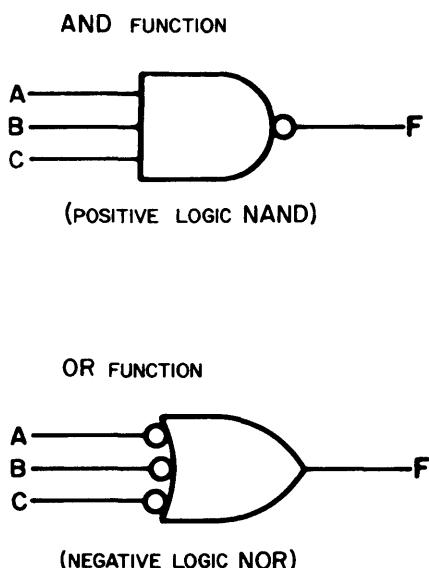
4.1 INTRODUCTION

This section contains information on logic symbology and drawing conventions used in the HyTerm schematics and logic diagrams, and information on the integrated circuits used.

4.2 FUNCTIONAL LOGIC

The HyTerm logic diagrams are primarily intended for use by field service personnel as troubleshooting aids. As such, the first responsibility of a set of logic diagrams is to illustrate a design's principles of operation. For this reason, Diablo Systems logic diagrams emphasize the functions performed by the logic elements rather than the kinds of devices used to implement the functions.

For example, a NAND gate may appear on a logic diagram as either a positive logic AND function with the output inverted (NAND), or as a negative logic OR function with the inputs inverted (NOR). See Figure 4-1. This practice runs contrary to some logic drawing standards, which require the use of the NAND symbol for both functions. But, in Diablo Systems diagrams, different symbols are used to distinguish between the two functions because the functional elements are considered to be more relevant to the design theory than symbolic representation of the kinds of devices used.

AND FUNCTION

(POSITIVE LOGIC NAND)

OR FUNCTION

(NEGATIVE LOGIC NOR)

A	B	C	F
L	L	L	H
H	L	L	H
L	H	L	H
H	H	L	H
L	L	H	H
H	L	H	H
L	H	H	H
H	H	H	L

H = +5V   L = 0V

Figure 4-1. Example of Functional Logic

4.3 SIGNAL NOMENCLATURE

The active level of each logic signal is assigned a descriptive name. A signal is considered active when it either causes or represents some logic event that is significant to the progress of an operation. Consequently, the name given a signal usually provides one of two kinds of functional information:

(1) Describes the effect that the signal's active level has on the logic it feeds; for example, -ENABLE INP allows data to be brought into the printer microprocessor.

(2) Represents a condition or event that develops elsewhere in the logic; for example -FUN SWITCH 4 is the name of the signal that is active whenever the number 4 function switch (FORM FEED) is operated.

A plus sign (+) or a minus sign(—) generally precedes each signal name to identify which of the two voltage levels used in the logic system is considered to be that signal's active level. The + sign represents the relatively higher logic level and the — sign, the relatively lower level. (This means relatively higher or lower with respect to each other; the signs do not always indicate signal polarity with respect to ground.) For example, if -RESET is low (0 volts), it means Reset is active; if -RESET is high (+5 volts), the Reset function is inactive. If +USART INTERRUPT is high, it means the USART has received a character from the data link and is ready to forward it to the MPU; if +USART INTERRUPT is low, it means the USART has not received any data from the data link that has not already been accepted by the MPU.

The actual voltage levels represented by the signs will depend on the logic family being used. For example, in TTL circuits, the signal identified by -RESET is active when it is at 0V (nominal) and inactive at +5V (nominal).

Sometimes a signal serves as the input to both positive logic and negative logic elements. Ordinarily in such cases, the sign preceding the signal name agrees with the active level indicated at the output of the logic element that produced the signal.

Signal names appearing in the text are printed in all capital letters to distinguish them from functions being performed. For example, '-RESET' refers to an actual signal name, whereas 'Reset' refers to the reset operation in general.

4.4 LOGIC SYMBOLOGY

The logic function symbols used in Diablo Systems logic diagrams conform closely to those set forth in MIL-STD-806. Most small scale integration (SSI) circuits are represented by function symbols. Medium scale integration (MSI) devices, such as shift registers and counters, may be represented by rectangles with functional labels.

Generally, a circle drawn at an input to a symbol indicates that the input is active when it is low (0V nominal). The absence of a circle at an input means that input is logically active when it is high (+5V nominal). The presence or absence of a circle at a symbol output has similar meanings for the active level of that output. Usually, all logic symbols are drawn with inputs on the left and outputs on the right. Symbols for all integrated circuits used are shown in the IC data contained in this section.

4.5 INTEGRATED CIRCUITS

Table 4-1 summarizes all integrated circuits used in the HyTerm. All of the ICs listed were used at some point in the HyTerm manufacturing process, but all will not be found in current production machines. Further information is contained in the following several pages. IC data on the following pages is arranged the same order as listed in Table 4-1, so the table can be used as an index when looking for data on a particular IC.

Table 4-1. Integrated Circuits

Digital:

Type	Description	Diablo Part No.
833	DTL Dual 4-Input Expander	42191-31
7400	TTL Quad 2-Input NAND Gate	10134
74LS00	TTL Quad 2-Input NAND Gate, Low Power Schottky	13077
7402	TTL Quad 2-Input NOR Gate	10135
74LS02	TTL Quad 2-Input NOR Gate, Low Power Schottky	42350-01

Table 4-1. Integrated Circuits (Continued)

Type	Description	Diablo Part No.
7404	TTL Hex Inverter	10136
74L04	TTL Hex Inverter, Low Power	10389
74LS04	TTL Hex Inverter, Low Power Schottky	10209
7405	TTL Hex Inverter, Open Collector	13145
7406	TTL Hex Inverter Buffer/Driver	10460
7407	TTL Hex Buffer/Driver	10391
7408	TTL Quad 2-Input AND Gate	10119
74LS08	TTL Quad 2-Input AND Gate, Low Power Schottky	10210
7410	TTL Triple 3-Input NAND Gate	10133
74LS10	TTL Triple 3-Input NAND Gate, Low Power Schottky	13080
7411	TTL Triple 3-Input AND Gate	10301
7414	TTL Hex Schmitt-trigger Inverter	10299-01
7420	TTL Dual 4-Input NAND Gate	10125
74H21	TTL Dual 4-Input AND Gate	10319
7426	TTL Quad 2-Input NAND High-Voltage Interface Gate	10120
7432	TTL Quad 2-Input OR Gate	10302
7442A	TTL BCD-To-Decimal Decoder	10146
74LS42	TTL BCD-To-Decimal Decoder, Low Power Schottky	13083
7451	TTL Dual AND-OR-INVERT Gate	10280
7453	TTL 4-wide Expandable AND-OR-INVERT Gate	10192
7474	TTL Dual D Flip-flop	10139
74LS74	TTL Dual D Flip-flop, Low Power Schottky	13085
7483A	TTL 4-Bit Binary Full Adder	10140
74LS83	TTL 4-Bit Binary Full Adder, Low Power Schottky	13086
7486	TTL Quad 2-Input Exclusive OR Gate	10303
3101/7489	TTL 16 x 4-Bit RAM, Open Collector	10193
8599/74S189	TTL 16 x 4-Bit RAM, Three-state	10334
3101A/74S289	TTL 16 x 4-Bit RAM, Open Collector Schottky	13088
7492A	TTL Divide-by-12 Counter	10304
7493A	TTL 4-Bit Binary Counter	10141
74107	TTL Dual J-K Master-Slave Flip-flop	10305
74LS107	TTL Dual J-K Master-Slave Flip-flop, Low Power Schottky	10389
74145	TTL BCD-to-Decimal Decoder/Driver	10172-29
74148	TTL 8-Line to 3-Line Priority Encoder	10394
74155	TTL Dual 2:4 Decoder	10194
74LS155	TTL Dual 2:4 Decoder, Low Power Schottky	13090
74161	TTL 4-Bit Synchronous Binary Counter	10335
74163	TTL 4-Bit Synchronous Binary Counter	10356
74LS164	TTL 8-Bit Shift Register, Low Power Schottky	42392-01
74170	TTL 4 x 4-Bit RAM	10195
74LS170	TTL 4 x 4-Bit RAM, Low Power Schottky	13092
74174	TTL Hex D Latch	10336
74LS174	TTL Hex D Latch, Low Power Schottky	10393
74LS175	TTL Quad D Flip-flop, Low Power Schottky	42363-XX
74195	TTL 4-Bit Parallel-Access Shift Register	10191

Table 4-1. Integrated Circuits (Continued)

Type	Description	Diablo Part No.
9334/74259	TTL 8-Bit Addressable Latch	10339
74LS259	TTL 8-Bit Addressable Latch, Low Power Schottky	13094
74298	TTL Quad 2-Input Multiplexer/Register	10196
74LS298	TTL Quad 2-Input Multiplexer/Register, Low Power Schottky	13095
74367	TTL Hex Bus Driver, Three-State	10197
74LS367	TTL Hex Bus Driver, Three-State, Low Power Schottky	13096
8080A	MOS 8-Bit Microprocessing Unit	42338
8205	TTL 3-Line to 8-Line Decoder	42335
25LS138	TTL 3-Line to 8-Line Decoder	42403
8212	TTL 8-Bit I/O Port, Schottky	42337
8216	TTL 4-Bit Bi-directional Bus Driver	42339
8224	TTL Clock Generator/Driver, Schottky	10215
8228	TTL Bus Driver/System Controller, Schottky	42331
8251	MOS USART	42336
82S115	TTL 512 x 8-Bit PROM, Three-State	
8316A	TTL 2K x 8-Bit ROM, Three-State	
8708	MOS 1K x 8-Bit EROM, Three-State	42329
2111	MOS 256 x 4-Bit Static RAM, Three-State	42334
SW-10667	DTL Pulse Generator	14027
TTL-117	Phototransistor Opto-Isolator	42168-XX
MCT2	Phototransistor Opto-Isolator	41290-01
MM5873	Keyboard Encoder/Decoder/Processor	42191-33
SW-20314	MOS Keyboard Decoder/Encoder	14026

Interface:

Type	Description	Diablo Part No.
75150P	Dual Line Driver	10353
75154	Quad Line Receiver	10354
75451	Dual AND-Gate Peripheral Driver	10181

Linear:

Type	Description	Diablo Part No.
LM319	Dual High-Speed Voltage Comparator	10168
LM310H-5	Voltage Regulator, 3-Terminal	42155-05
LM320H-12	Voltage Regulator, 3-Terminal	42155-12
LM341P-12	Voltage Regulator, 3-Terminal Positive	42154-12
LM723CD	Voltage Regulator	10321
LM733C	Differential Video Amplifier	10124
MC1741SCP1	Op Amp, High Slew Rate	10167
72747	Dual Op Amp, General Purpose	10165
72747	Dual Op Amp, Selected	13072
72748	Op Amp	10166

Table 4-1. Integrated Circuits (Continued)

Miscellaneous Special Purpose:
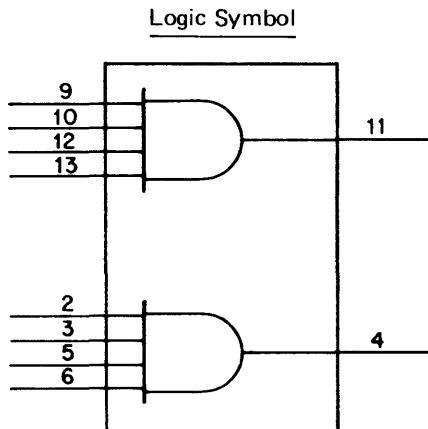
Type	Description	Diablo Part No.
CA3086	NPN Transistor Array	42191-32
8041	Quad FET	10190
1408L-6	Digital-to-Analog Converter	13060
	Resistor Network, 1K (15 resistors)	10239-01
	Resistor Network, 1K (13 resistors)	10761
	Resistor Network, 10K (8 resistors)	13044

Dual 4-Input Expander   Part No. 42191-31   Type 833

Logic Symbol

This device is an expander element which allows increased fan-in for buffer units.

VCC-14, GND-7   (083-030)

TTL Quad 2-Input NAND Gate   Part No. 10134   Type 7400
TTL Quad 2-Input NAND Gate, Low Power Schottky   Part No. 13077   Type 74LS00
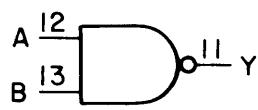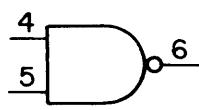
Logic Symbol   Alternate Symbol   Truth Table

A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

VCC-14, GND-7

Loading:
    Inputs   1 Unit Load (.2 for 74LS00)
    Outputs   10 Unit Loads (5 for 74LS00)

TTL Quad 2-Input NOR Gate

Part No. 10135
Part No. 42350-01

Type 7402
Type 74LS02

Logic Symbol

Alternate Symbol

Truth Table

A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

VCC-14, GND-7

Loading:	7402	74LS02
Inputs	1 Unit Load	0.2 Unit Load
Outputs	10 Unit Loads	5.0 Unit Loads

TTL Hex Inverter
TTL Hex Inverter, Low Power
TTL Hex Inverter, Low Power Schottky

Part No. 10136
Part No. 10389
Part No. 10209
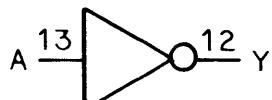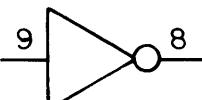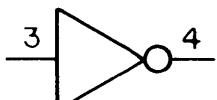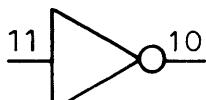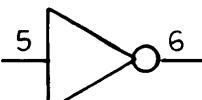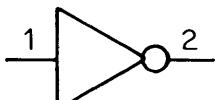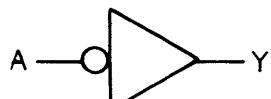
Type 7404
Type 74L04
Type 74LS04

Logic Symbol

Alternate Symbol
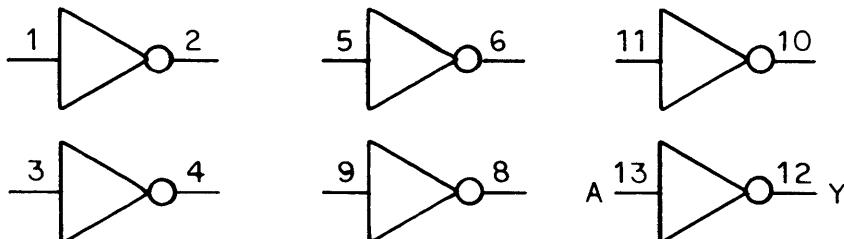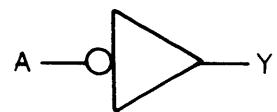
VCC-14, GND-7

Loading:
Inputs   1 Unit Load (.1 for 74L04, .2 for 74LS04)
Outputs   10 Unit Loads (2 for 74L04, 5 for 74LS04)
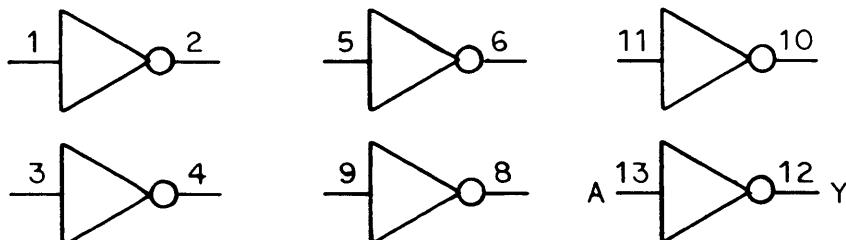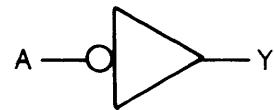
TTL Hex Inverter, Open-Collector   Part No. 13145   Type 7405

Logic Symbol   Alternate Symbol

1 ▷○ 2   5 ▷○ 6   11 ▷○ 10

3 ▷○ 4   9 ▷○ 8   A 13 ▷○ 12 Y   A ─○▷─ Y

VCC-14, GND-7

Loading:
        Inputs   1 Unit Load
        Outputs   10 Unit Loads

TTL Hex Inverter Buffer/Driver   Part No. 10460   Type 7406
    These drivers have high-voltage (up to 30V)
open-collector outputs for interfacing with high-level
circuits or for driving high current loads.

Logic Symbol   Alternate Symbol

1 ▷○ 2   5 ▷○ 6   11 ▷○ 10

3 ▷○ 4   9 ▷○ 8   A 13 ▷○ 12 Y   A ─○▷─ Y

VCC-14, GND-7

Loading:
        Inputs   1 Unit Load
        Outputs   25 Unit Loads

These drivers have high-voltage (up to 30V) open-collector outputs for interfacing with high-level circuits or for driving high current loads.

Logic Symbol

VCC-14, GND-7

Loading:
    Inputs   1 Unit Load
    Outputs   25 Unit Loads

TTL Quad 2-Input AND Gate   Part No. 10119   Type 7408
TTL Quad 2-Input AND Gate, Low Power Schottky   Part No. 10210   Type 74LS08
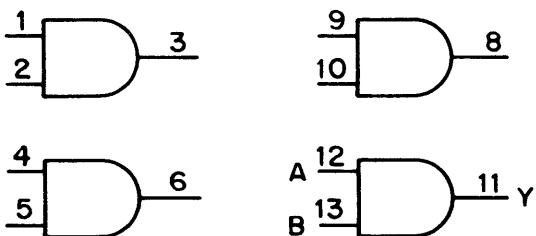
Logic	Symbol	Truth Table

A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

VCC-14, GND-7

Loading:
    Inputs   1 Unit Load (.2 for 74LS08)
    Outputs   10 Unit Loads (5 for 74LS08)
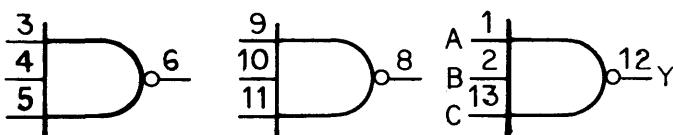
TTL Triple 3-Input NAND Gate Part No. 10133 Type 7410
TTL Triple 3-Input NAND Gate, Low Power Schottky Part No. 13080 Type 74LS10

Logic Symbol
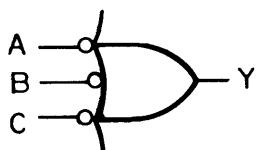
Truth Table

A	B	C	Y
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

VCC-14, GND-7

Alternate Symbol

Loading:
Inputs   1 Unit Load (.2 for 74LS10)
Outputs   10 Unit Loads (5 for 74LS10)
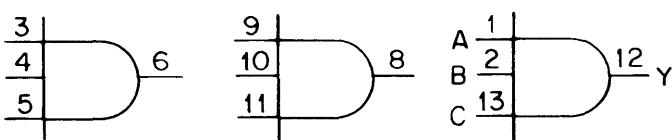
TTL Triple 3-Input AND Gate Part No. 10301 Type 7411

Logic Symbol
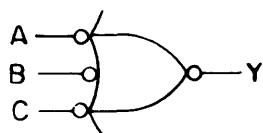
Truth Table

A	B	C	Y
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

VCC-14, GND-7

Alternate Symbol

Loading:
Inputs   1 Unit Load
Outputs   10 Unit Loads
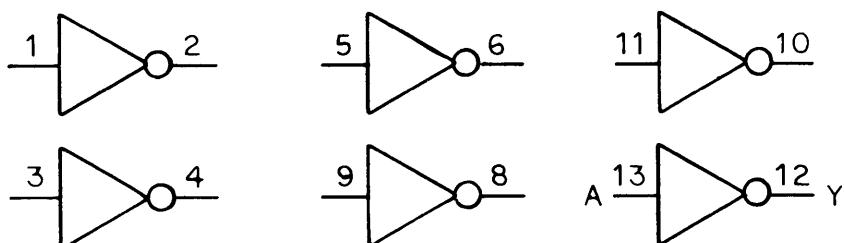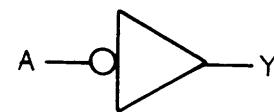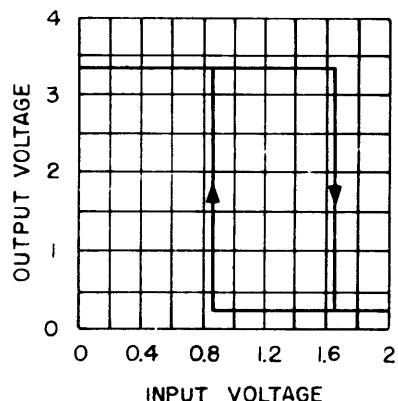
Logically, these gates act like ordinary inverters but because of the Schmitt action, each gate has different input threshold levels for positive- and negative-going signals. The hysteresis, which is the difference between the two levels, is typically 800 mV.

Alternate Symbol

A ──○▷── Y

Logic Symbol

1 ▷○ 2   5 ▷○ 6   11 ▷○ 10

3 ▷○ 4   9 ▷○ 8   A 13 ▷○ 12 Y

VCC-14, GND-7
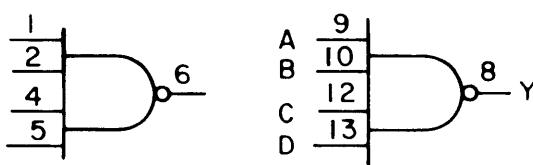
Waveforms

Loading:
  Inputs   .75 Unit Load
  Outputs   10 Unit Loads
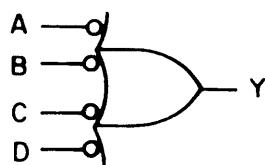
Logic Symbol

VCC-14, GND-7. Pins 3 & 11 not used.
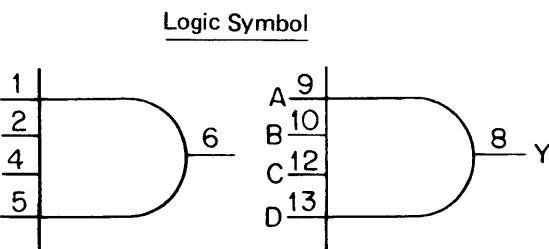
Alternate Symbol

Truth Table

A	B	C	D	Y
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	L	L	H
L	H	L	H	H
L	H	H	L	H
L	H	H	H	H
H	L	L	L	H
H	L	L	H	H
H	L	H	L	H
H	L	H	H	H
H	H	L	L	H
H	H	L	H	H
H	H	H	L	H
H	H	H	H	L
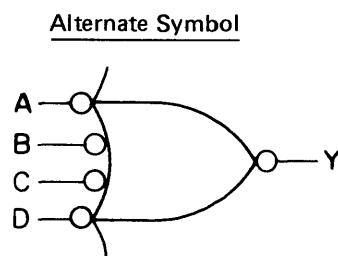
Loading:
  Inputs   1 Unit Load
  Outputs   10 Unit Loads

TTL Dual 4-Input AND Gate — Part No. 10319 — Type 74H21

Logic Symbol

VCC-14, GND-7 Pins 3 & 11 not used

Alternate Symbol
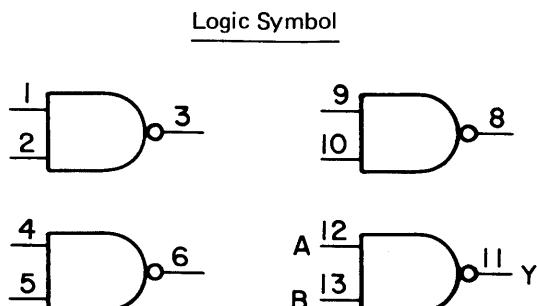
Truth Table

A	B	C	D	Y
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H

Loading:

Inputs 1.25 Unit Loads

Outputs 12.5 Unit Loads

TTL Quad 2-Input NAND High-Voltage Interface Gate — Part No. 10120 — Type 7426

These gates have high-voltage (up to 15V) open-collector outputs for interfacing with high-level circuits.

Logic Symbol

VCC-14, GND-7

Alternate Symbol

Truth Table

A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

Loading:

Inputs 1 Unit Load
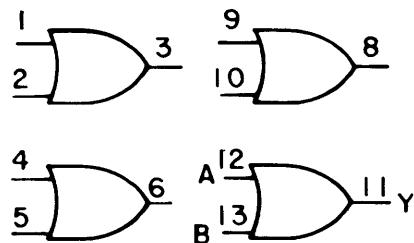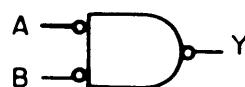
Outputs 10 Unit Loads

Logic Symbol   Alternate Symbol   Truth Table

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

VCC-14, GND-7

Loading:
Inputs   1 Unit Load (.25 for 74LS32)
Outputs   10 Unit Loads (5 for 74LS32)
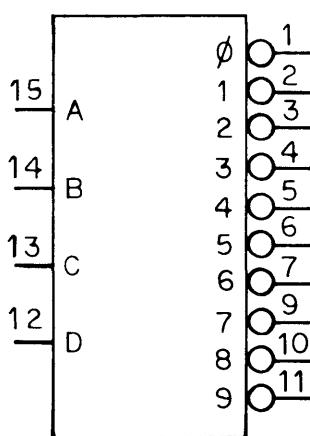
TTL BCD-To-Decimal Decoder   Part No. 10146   Type 7442A
TTL BCD-To-Decimal Decoder, Low Power Schottky   Part No. 13083   Type 74LS42

Logic Symbol   Truth Table
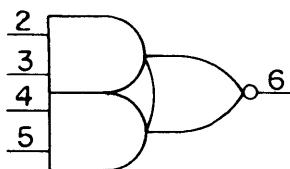
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

VCC-16, GND-8

A1-A8 = Binary address input
0-9 = Decimal output

Loading:
Inputs   1 Unit Load (.25 for 74LS42)
Outputs   10 Unit Loads (5 for 74LS42)

TTL Dual AND-OR-INVERT Gate   Part No. 10280   Type 7451

Logic Symbol

VCC — 14, GND — 7

Truth Table

A	B	C	D	Y
L	X	L	X	H
L	X	X	L	H
X	L	X	L	H
X	L	L	X	H
H	H	X	X	L
X	X	H	H	L
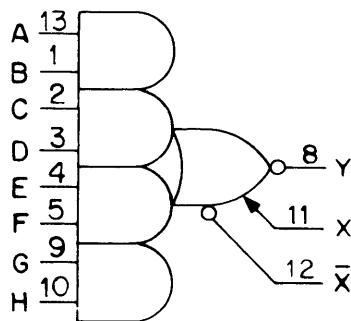
$$Y = \overline{AB + CD}$$

(Make no connections to pins 11 and 12.)

Loading:
Inputs	1 Unit Load
Outputs	10 Unit Loads

TTL 4-Wide Expandable AND-OR-INVERT Gate   Part No. 10192   Type 7453

Up to four type 7460 expander gates may be connected to the expander inputs. Both expander inputs must be used simultaneously. If the expander inputs are not used, they should be left open.

Logic Symbol

VCC-14, GND-7

$$Y = \overline{AB+CD+EF+GH+X}$$

Loading:
Inputs	1 Unit Load
Outputs	10 Unit Loads

4-13

TTL Dual D Flip-flop
TTL Dual D Flip-Flop, Low Power Schottky
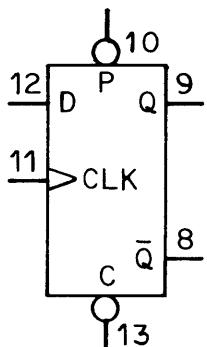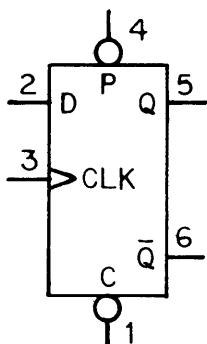
Part No. 10139
Part No. 13085

Type 7474
Type 74LS74

The 7474 contains two D-type edge-triggered flip-flops with direct preset and clear inputs. A low level on the preset or clear input will set or reset the flip-flop, respectively, regardless of other input condi- tions. When both the preset and clear are high, the logic level on D is transferred to Q on the positive-going edge of the clock.
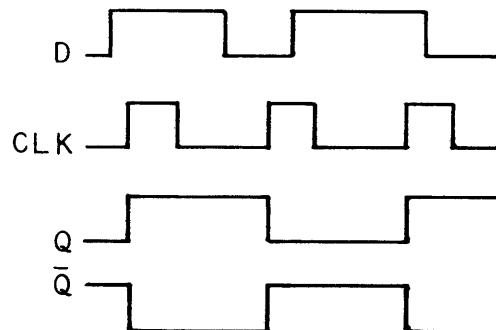
Logic Symbol

VCC-14, GND-7

P   = Preset input
D   = Data input
CLK = Clock input
C   = Clear input
Q,Q̄ = Data outputs

Loading:

		Unit Loads	
		7474	74LS74
Inputs	CLK	2	.5
	D	1	.25
	P	1	.5
	C	2	.75
Outputs	Q,Q̄	10	5

Timing Waveforms

Truth Table

Function	Inputs				Outputs	
	Preset	Clear	Clock	D	Q	Q̄
Preset	L	H	X	X	H	L
Clear	H	L	X	X	L	H
Clear	L	L	X	X	H	H*
Set	H	H	▲	H	H	L
Reset	H	H	▲	L	L	H
Set Up	H	H	L	X	No Change	

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high level).
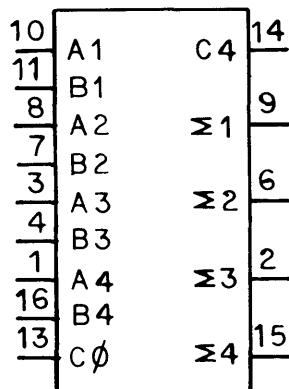
| TTL 4-Bit Binary Full Adder | Part No. 10140 | Type 7483A |
| TTL 4-Bit Binary Full Adder, Low Power Schottky | Part No. 13086 | Type 74LS83 |
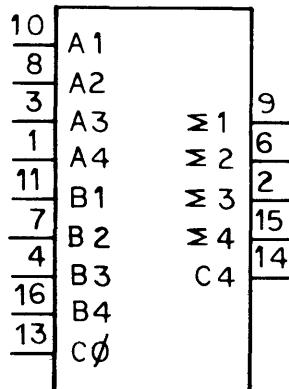
This device adds two 4-bit binary numbers and a carry (CØ input). The sum (Σ) outputs are provided for each bit and the carry output (C4) is obtained from the fourth bit. Note the non-standard VCC and GND connections to this device.

Logic Symbol

NOTE: VCC-5, GND-12

Alternate Symbol

Truth Table
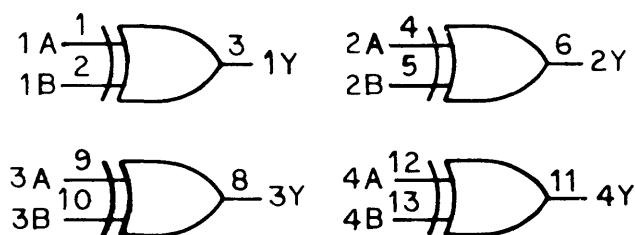
				Outputs					
Inputs				When CØ=L			When CØ=H		
					When C2=L			When C2=H	
A1 / A3	B1 / B3	A2 / A4	B1 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE: Input conditions at A1, B1, A2, B2, and CØ are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Loading:

						Unit Loads	
						7483A	74LS83
Inputs	A1,	A3,	B1,	B3,	CØ	1 or 2*	1
	A2,	A4,	B2,	B4		1 or 2*	.25
Outputs	Sum	1-4				10	5
	C4					5	5

*Depending upon manufacturer.

Logic Symbol

1A 1
1B 2 — 3 1Y   2A 4
2B 5 — 6 2Y

3A 9
3B 10 — 8 3Y   4A 12
4B 13 — 11 4Y

VCC-14, GND-7

Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Loading:

Inputs	1 Unit Load
Outputs	10 Unit Loads

TTL 16 x 4-bit Random Access Memory, Open Collector   Part No. 10193   Type 3101/7489
TTL 16 x 4-bit Random Access Memory, Three-State   Part No. 10334   Type 8599/74S189
TTL 16 x 4-bit Random Access Memory, Open Collector Schottky   Part No. 13088   Type 3101A/74S289
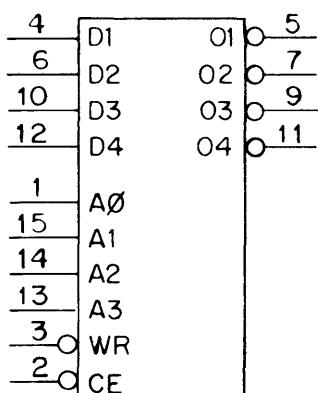
Logic Symbol

4 — D1   O1 — 5
6 — D2   O2 — 7
10 — D3   O3 — 9
12 — D4   O4 — 11

1 — AØ
15 — A1
14 — A2
13 — A3
3 — WR
2 — CE

VCC-16, GND-8

Function Table

Inputs			
CE	WR	Outputs	Function
L	L	H*	Write
L	H	Complement of stored data	Read
H	X	H*	Inhibit

H* = high for open-collector, high-impedance for three state. Some manufacturers specify this as indeterminate.
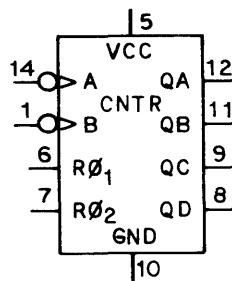
Loading:

Inputs (7489, 8599)	1 Unit Load
Others	.16 Unit Load (.25 ma)
Outputs	10 Unit Loads
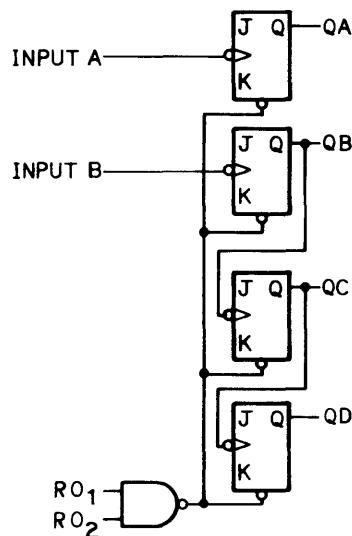
Each of these chips contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-six.

To use the maximum count length of the counters, the B input is connected to the QA output. The input count pulses are applied to input A and the outputs are as described in the truth table.

Logic Symbol   Alternate Symbol   Truth Table

Truth Table

	Output			
Count	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

Output Q_A is connected to input B.

H = high level, L = low level, X = irrelevant

Reset/Count

Reset Input		Output
R01	R02	Q
H	H	L
L	X	Count
X	L	Count
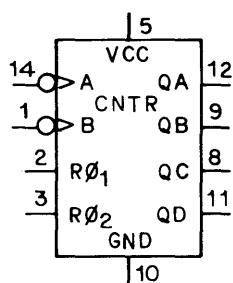
Loading:
Any Reset	1 Unit Load
A	2 Unit Loads
B	3 Unit Loads
Output	10 Unit Loads
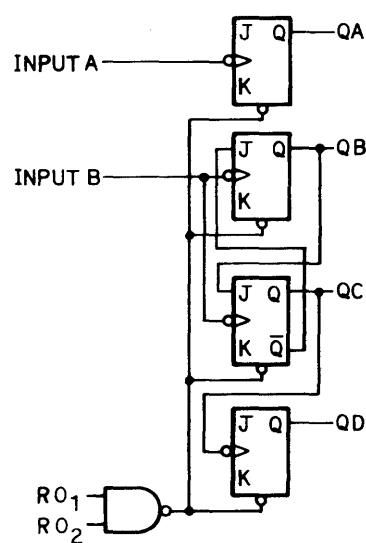
Each of these chips contains four master-slave flip-flops and additional gating to provide a divide by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

To use the maximum count length of the counters, the B input is connected to the QA output. The input count pulses are applied to input A and the outputs are as described in the truth table.

Logic Symbol   Alternate Symbol   Truth Table

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output QA is connected to input B.
H = high level, L = low level, X = irrelevant

Reset/Count

Reset Inputs		Output
RO_1	RO_2	Q
H	H	L
L	X	Count
X	L	Count

Loading:
Inputs
    Any Reset   =   1 Unit Load
    A   =   2 Unit Loads
    B   =   2 Unit Loads
    Outputs   =   10 Unit Loads
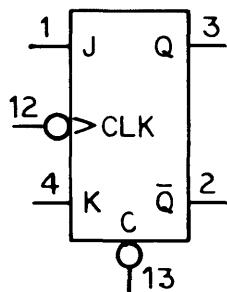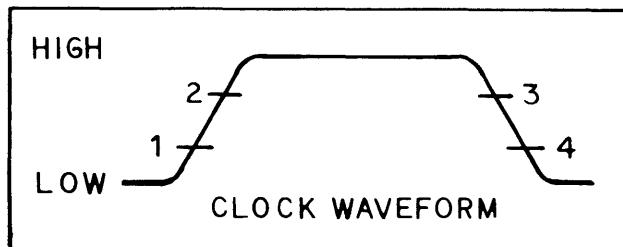
Logic Symbol

Timing Waveform
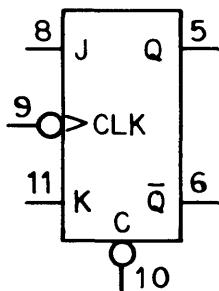
1. Isolate slave from master
2. Enable entry of data from J and K inputs to master
3. Disable entry of data from J and K inputs
4. Transfer information from master to slave

J, K = Data inputs
CLK = Clock inputs
C   = Clear inputs
Q, $\bar{Q}$ = Data outputs

VCC-7, GND-14

Truth Table

(Each Flip-Flop)

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$

t_n = time when clock is high (2-3)
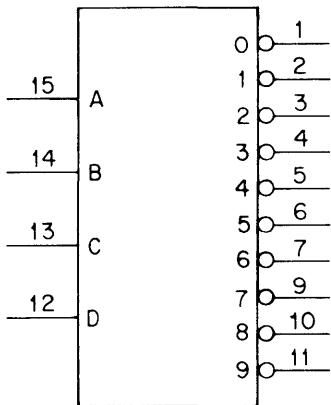
t_{n+1} = time after clock goes low (4)

Loading:

C, CLK	2 Unit Loads (.5 for 74LS107)	
J, K	1 Unit Load (.25 for 74LS107)	
Outputs	10 Unit Loads (5 for 74LS107)	

This BCD-to-decimal decoder/driver consists of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10-15) binary input conditions.

Logic Symbol

VCC — 16
GND — 8

(083 — 035)

Truth Table

No.	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)
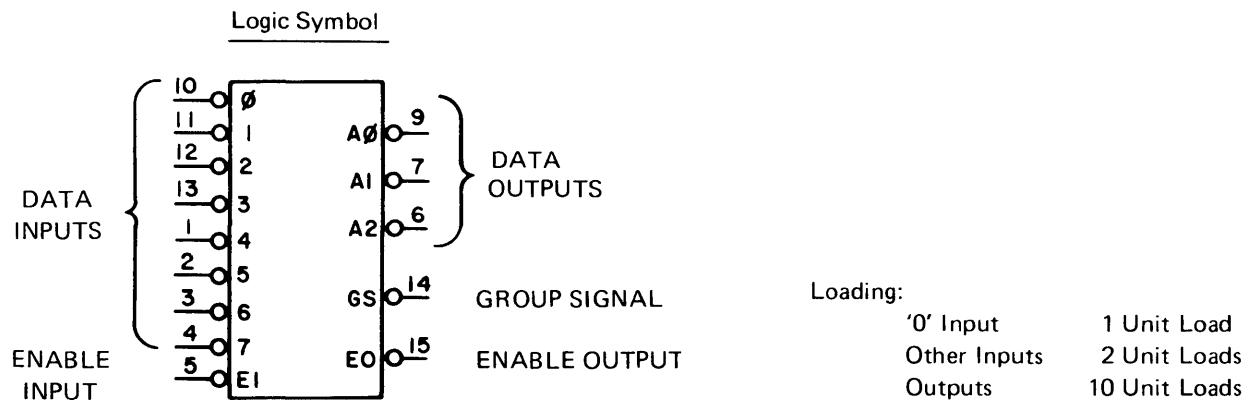
Loading:
Input   1 Unit Load
Output   =   12.5 Unit Loads

This device accepts data from 8 low-active inputs and provides a binary representation on the three low-active outputs. A priority is assigned to each input so that when two or more inputs are active simultaneously, the input with the highest priority is represented on the output. Input line '7' has the highest priority; line '0', the lowest.

A high on the Enable Input (EI) pin forces all outputs high, effectively blocking the encoder. The Group Signal (GS) output goes low when any input (in addition to EI) is low. Enable Out (EO) is low only when all inputs (other than EI) are high.

Logic Symbol

DATA INPUTS

ENABLE INPUT

DATA OUTPUTS

GROUP SIGNAL

ENABLE OUTPUT

VCC-16, GND-8

Loading:

'0' Input	1 Unit Load
Other Inputs	2 Unit Loads
Outputs	10 Unit Loads

Truth Table

	Inputs									Outputs				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High   L = Low   X = Irrelevant
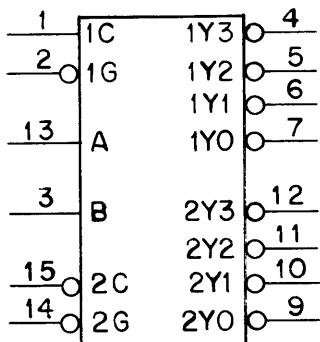
Logic Symbol

```
 1  ┌─────────────┐
────│ 1C     1Y3 │o──── 4
 2  │             │o──── 5
───o│ 1G     1Y2 │
    │        1Y1 │o──── 6
13  │             │
────│ A      1Y0 │o──── 7
    │             │
 3  │             │o──── 12
────│ B      2Y3 │
    │        2Y2 │o──── 11
15  │             │
───o│ 2C     2Y1 │o──── 10
14  │             │
───o│ 2G     2Y0 │o──── 9
    └─────────────┘
```

VCC-16, GND-8

Truth Table

Inputs				Outputs			
Select		Gate	Data				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H
		2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

Loading:

Inputs   1 Unit Load (.25 for 74LS155)

Outputs   10 Unit Loads (5 for 74LS155)
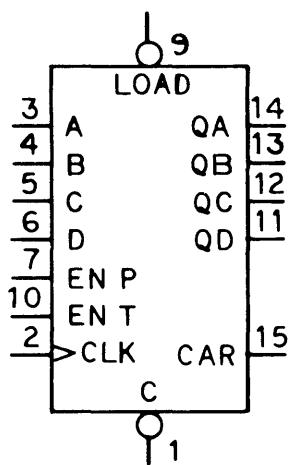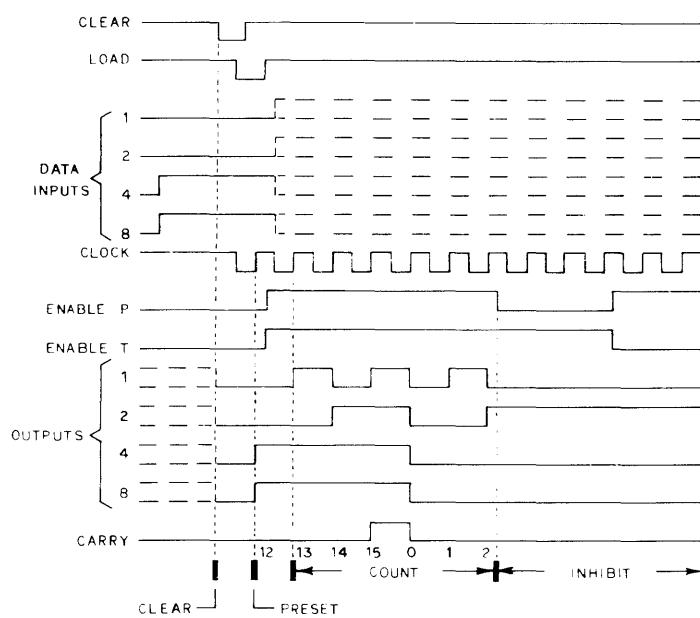
All flip-flops in this chip are clocked simultaneously, so all output changes occur simultaneously. A low on the Clear input overrides other inputs, and drives all outputs low.

Logic Symbol

VCC-16, GND-8

Loading:

		Unit Loads	
		74161	74LS161
Inputs	LOAD	1	.5
	CLK, EN-T	2	.5
	Other	1	.25
Outputs		10	5

Timing Waveforms

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit
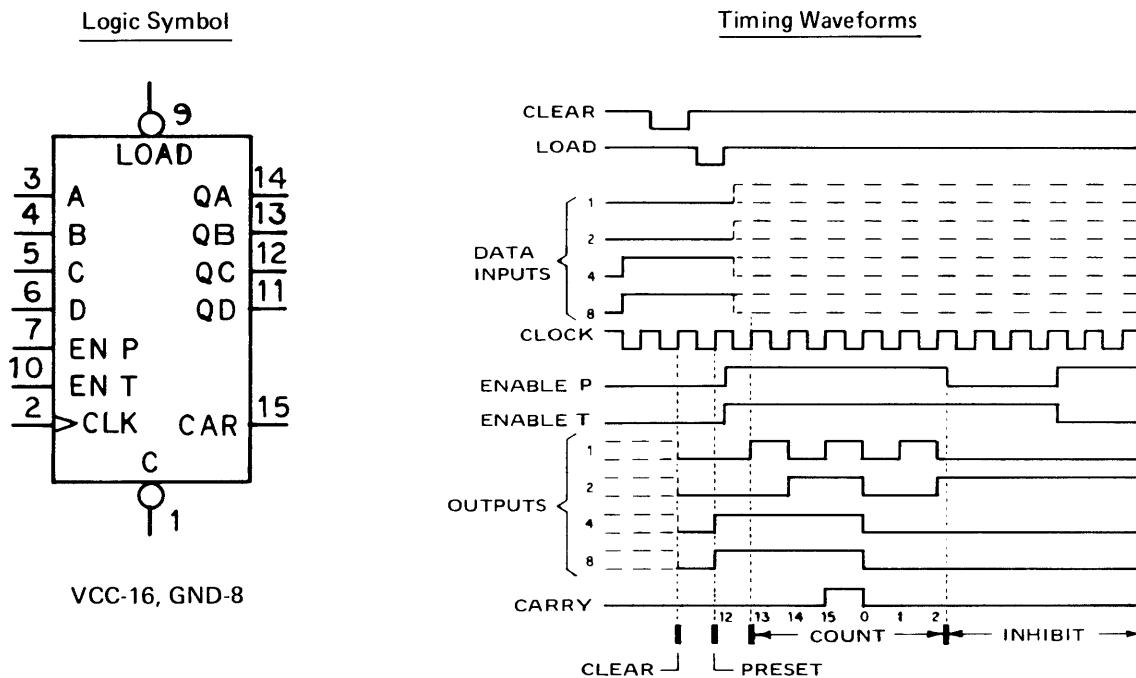
Truth Table

INPUTS						OUTPUTS
CLK	EN-P	EN-T	LOAD	C	A,B,C,D	
H	X	X	X	X	X	No Change
L	X*	X*	X*	X	X	No Change
X	X	X	X	L	X	All LOW
↑	X	X	L	H	DATA	Preset to A,B,C,D, input data
↑	L	L	H	H	X	No Change
↑	H	L	H	H	X	No Change
↑	L	H	H	H	X	No Change
↑	H	H	H	H	X	Count Up

*Avoid changes to inputs while CLK is low.

All flip-flops in this chip are clocked simultaneously, so all output changes occur simultaneously. A low on the Clear input overrides all other inputs, and drives all outputs low at the next positive-going clock.

Logic Symbol

VCC-16, GND-8

Loading:

CLK, EN-T	2 Unit Loads
All other inputs	1 Unit Load
Outputs	10 Unit Loads

Timing Waveforms

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit

Truth Table

INPUTS						OUTPUTS
CLK	EN-P	EN-T	LOAD	C	A,B,C,D	
H	X	X	X	X	X	No Change
L	X*	X*	X*	X	X	No Change
↑	X	X	X	L	X	All LOW
↑	X	X	L	H	DATA	Preset to A,B,C,D, input data
↑	L	L	H	H	X	No Change
↑	H	L	H	H	X	No Change
↑	L	H	H	H	X	No Change
↑	H	H	H	H	X	Count Up

*Avoid changes to inputs while CLK is low.

This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low as either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the set-up requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input.
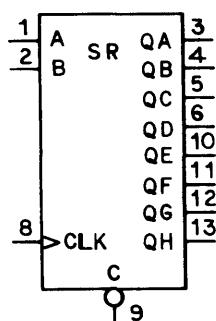
Logic Symbol

VCC = 14   GND = 7

Truth Table

Inputs				Outputs		
Clear	Clock	A	B	QA	QB...QH	
L	X	X	X	L	L	L
H	L	X	X	X	X	X
H	↑	H	H	H	X	X
H	↑	L	X	L	X	X
H	↑	X	L	L	X	X
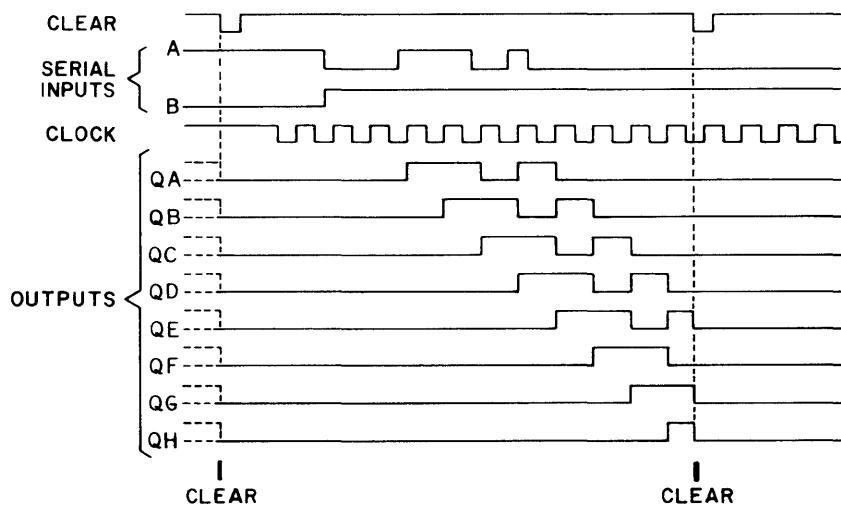
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level

Timing Waveforms

Loading:
Inputs = 1 Unit Load (.25 For 74LS164)
Outputs = 5 Unit Loads
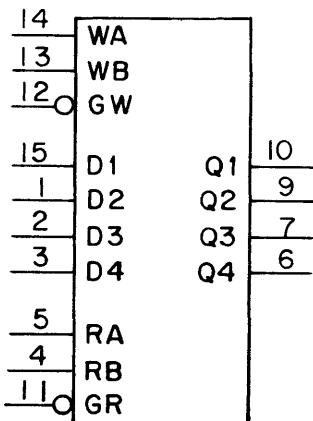
TTL 4 x 4-bit RAM
TTL 4 x 4-bit RAM, Low Power Schottky

Part No. 10195
Part No. 13092
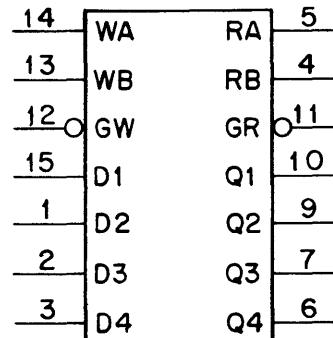
Type 74170
Type 74LS170

This RAM has independent read and write addressing and gating, which allows simultaneous reading and writing to/from different addresses. Outputs are open-collector.

Logic Symbol

Alternate Symbol

VCC-16, GND-8

Write Function Table

Write Inputs			Function
GW	WB	WA	
L	L	L	Write Word 0
L	L	H	Write Word 1
L	H	L	Write Word 2
L	H	H	Write Word 3
H	X	X	No Change

Read Function Table

Read Inputs			Function
GR	RB	RA	
L	L	L	Read Word 0
L	L	H	Read Word 1
L	H	L	Read Word 2
L	H	H	Read Word 3
H	X	X	All Outputs High

Loading:
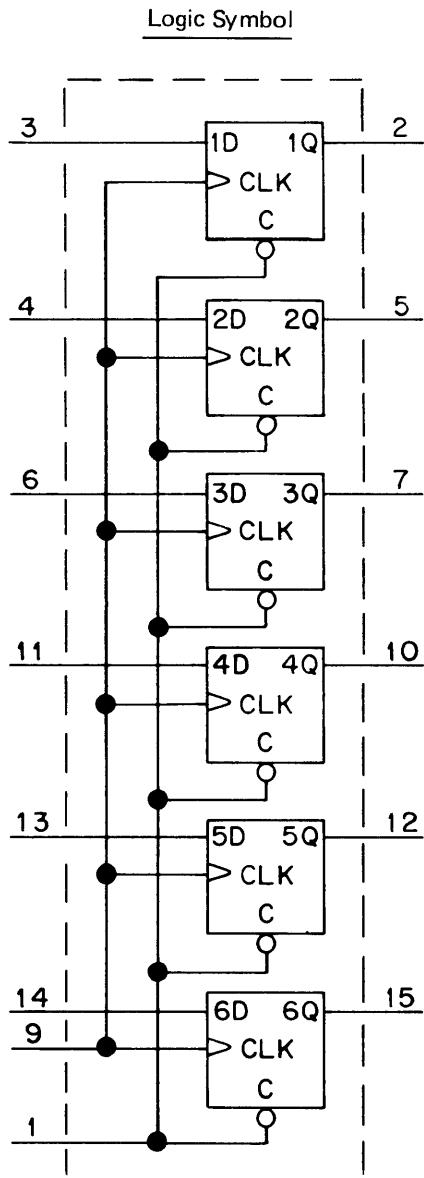
		Unit Loads	
		74170	74LS170
Inputs	Any D,R,W	1	.25
	GR, GW	1	.5
Outputs	Q1-Q4	10	5

TTL Hex D. Latch   Part No. 10336   Type 74174
TTL Hex D Latch, Low Power Schottky   Part No. 13093   Type 74LS174

All flip-flops in this chip are clocked or cleared simultaneously. A low on the clear input overrides all other inputs.

Logic Symbol

VCC-16, GND-8

Truth Table
(Each Flip-Flop)

INPUTS			OUTPUT
C	CLK	D	Q
L	X	X	H
H	▲	H	H
H	▲	L	L
H	L	X	No Change

H = High level
L = Low Level
X = Irrelevant
▲ = Transition from low to high level

1D – 6D = Data Inputs
CLK = Clock Input
C = Clear
1Q – 6Q = Data Outputs

Loading:

Inputs   1 Unit Load (.25 for 74LS174)
Outputs   10 Unit Loads (5 for 74LS174)

TTL Quad D Flip-Flop   Part No. 10337   Type 74175
TTL Quad D Flip-Flop, Low Power Schottky   Part No. 42363-01   Type 74LS175

This positive-edge-triggered flip-flop utilizes TTL circuitry to implement D-type flip-flop logic, with a direct clear input and complementary outputs from each flip-flop.

Data at the D inputs meeting set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Truth Table

(Each Flip-Flop)

Inputs			Outputs	
C	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	No Change	
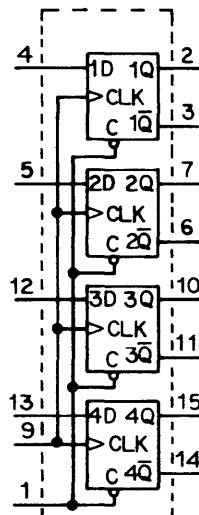
H = high level
L = low level
X = irrelevant
↑ = transition from low level
    to high level

Logic Symbol

VCC = 16, GND = 8

1D - 4D = Data Inputs
CLK   = Clock Input
C   = Clear
1Q - 4Q = Data Outputs
$\overline{1Q}$ - $\overline{4Q}$ = Complementary
                    Data Outputs
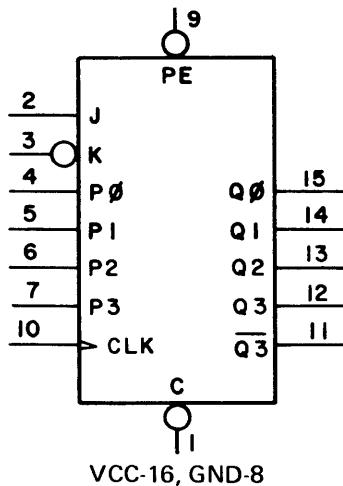
Loading:
    Inputs = 0.25 Unit Load
    Outputs = 10 Unit Loads

Data can be loaded into this register either serially or in parallel. When Parallel Enable (PE) is low, parallel data is loaded into the flip-flops on every positive-going clock. When PE is high, data is shifted from the J and K inputs to flip-flop 0, and from 0 to 1, 1 to 2, and 2 to 3, at each positive-going clock transition. A low on the Clear (C) input overrides all other controls.

Logic Symbol

VCC-16, GND-8

Truth Table

Inputs						Outputs					
C	PE	CLK	J	K	P0-P3	Q0	Q1	Q2	Q3	$\overline{Q3}$	
L	X	X	X	X	X	L	L	L	L	H	Clear
H	L	↑	X	X	abcd	a	b	c	d	$\overline{d}$	Parallel Load
H	H	L	X	X	X	Q0n	Q1n	Q2n	Q3n	$\overline{Q3n}$	No Change
H	H	↑	L	L	X	L	Q0n	Q1n	Q2n	$\overline{Q2n}$	
H	H	↑	L	H	X	$\overline{Q0n}$	Q0n	Q1n	Q2n	$\overline{Q2n}$	
H	H	↑	H	L	X	$\overline{Q0n}$	Q0n	Q1n	Q2n	$\overline{Q2n}$	Shift
H	H	↑	H	H	X	H	Q0n	Q1n	Q2n	$\overline{Q2n}$	

H   = High
L   = Low
X   = Irrelevant
Q0n = State of Q0 before positive transition of CLK

Loading:

Inputs	1 Unit Load	
Outputs	10 Unit Loads	

TTL 8-bit Addressable Latch
TTL 8-bit Addressable Latch, Low Power Schottky

Part No. 10339
Part No. 13094

Type 9334
Type 74LS259

This is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with high-active outputs. It incorporates a low-active common clear for resetting all latches, as well as a low-active enable.
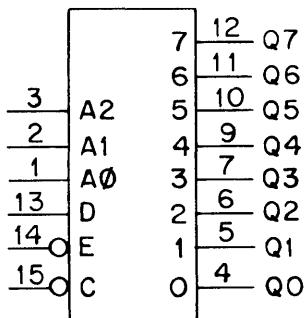
There are two modes of operation, shown in the Function Table. In the addressable latch mode, when E is LOW, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input, with all nonaddressed latches remaining in their previous states. When E is HIGH all latches

remain in their previous state and are unaffected by the data or address inputs. When operating as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while E is HIGH.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input, with all other outputs in the LOW state.

When E is HIGH and C is LOW all outputs are LOW and unaffected by the address and data inputs.
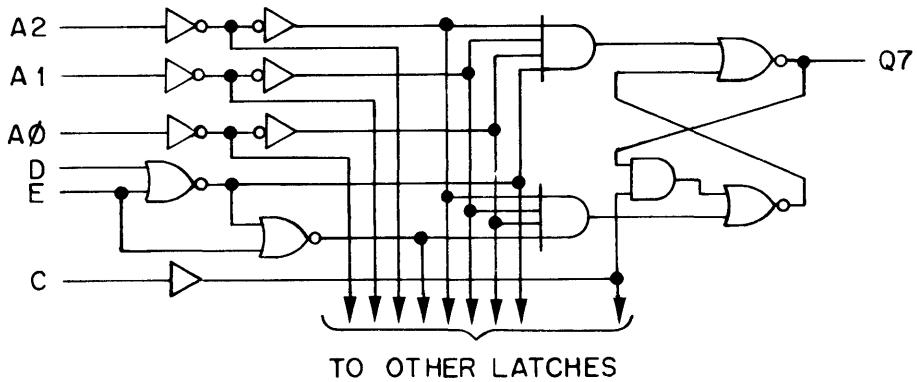
Logic Symbol

VCC-16, GND-8

Logic Diagram

ONLY ONE LATCH SHOWN FOR CLARITY

TO OTHER LATCHES

Function Table

Inputs			Outputs		
C	E	D	Addressed Latch	Others	Mode
L	L	L	L	L	} Demultiplexer
L	L	H	H	L	
L	H	X	L	L	Clear
H	L	L	L	No Change	} Addressable
H	L	H	H	No Change	} Latch
H	H	X	No Change	No Change	

Loading:

		Unit Loads	
		9334	74LS259
Inputs	E	1.5	.25
	Other	1	.25
Outputs		6	5
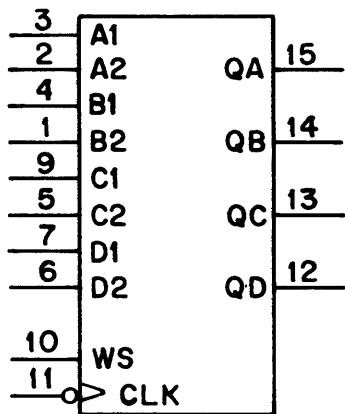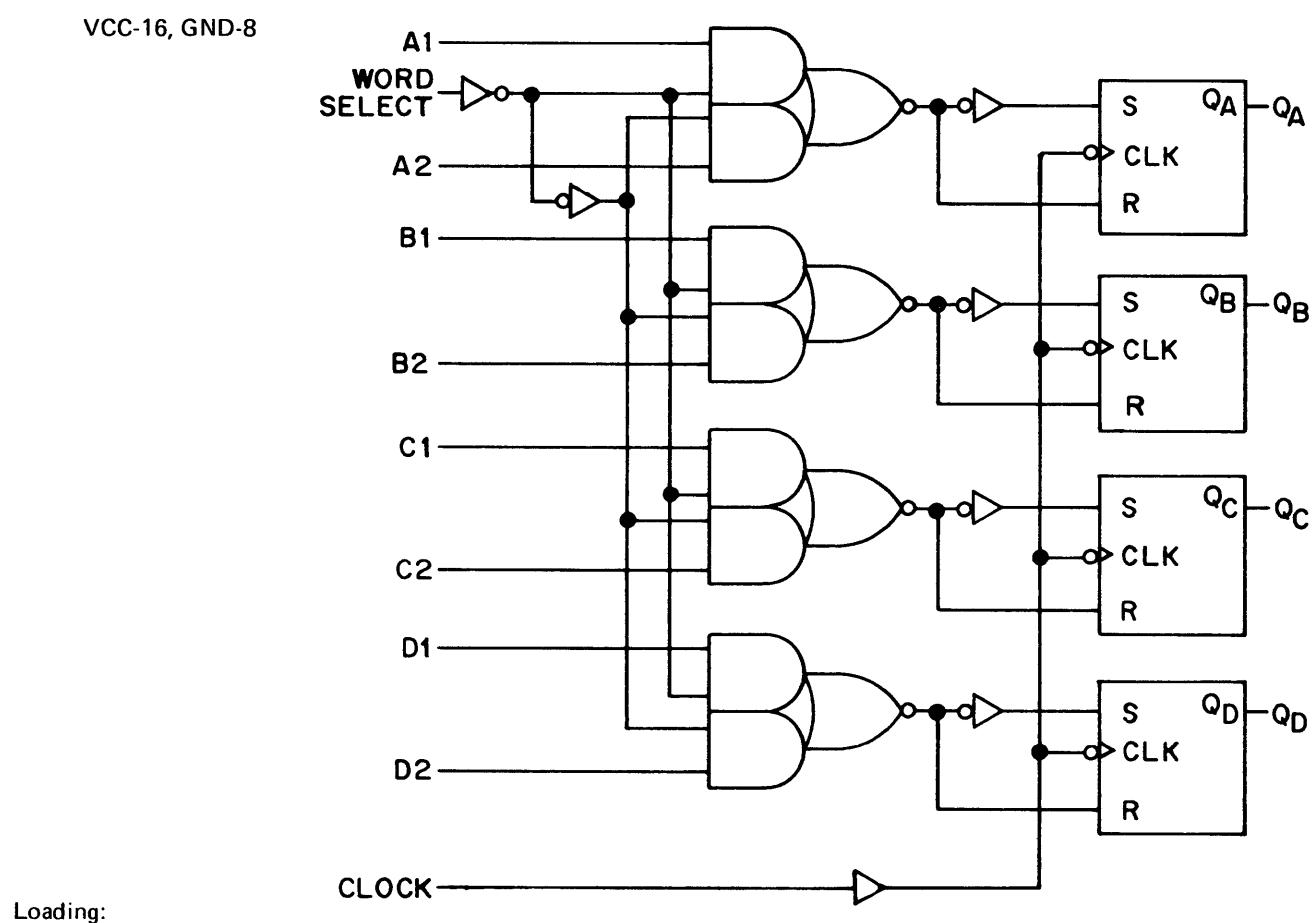
Data is stored on the negative-going edge of the CLK. With WS low, word 1 (A1, B1, C1, D1) is stored; with WS high, word 2 is stored.

Logic Symbol

VCC-16, GND-8

Logic Diagram

Loading:

	Unit Loads	
	74298	74LS298
Inputs	1	.25
Outputs	10	5
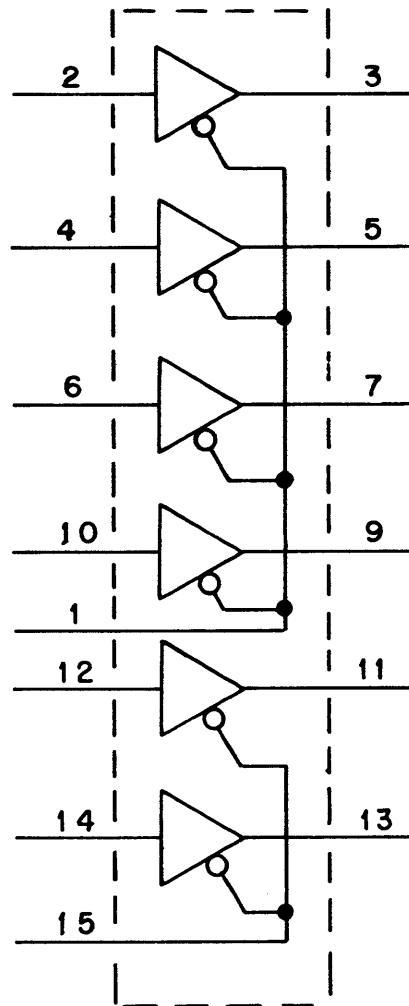
Logic Symbol

VCC-16, GND-8

Loading:

	Unit Loads	
	74367	74LS367
Inputs (Gate enabled)	1	.25
Outputs	20	10

This is a single chip 8-bit parallel microprocessor which forms a microcomputer system when interfaced with any type or speed of standard semiconductor memory up to 64K 8-bit words and an I/O device. The MPU inputs and outputs data over an 8-bit bi-directional three-state data bus (D0-D7). It addresses memory and I/O devices over a 16-bit three-state memory address bus (A0-A15). It is driven by two 12-volt non-overlapping clocks, Ø1 and Ø2. There are four input signals, INT (Interrupt), RDY (Ready), HOLD, and RST (Reset). Output signals include INTE (Interrupt Enable), DBIN (Data Bus In), WR (Write), SYNC, WAIT, and HLDA (Hold Acknowledge).

The 8080A contains a register array made up of six 16-bit registers: a Program Counter, a Stack Pointer, and four register "pairs," each made up of two 8-bit registers. One of these is the Temporary Register, called W/Z, which is used for the internal execution of instructions. The other three are working registers, called B/C, D/F, and H/L. The six general purpose registers can be used as either single 8-bit registers or 16-bit register pairs; W/Z is not program addressable.
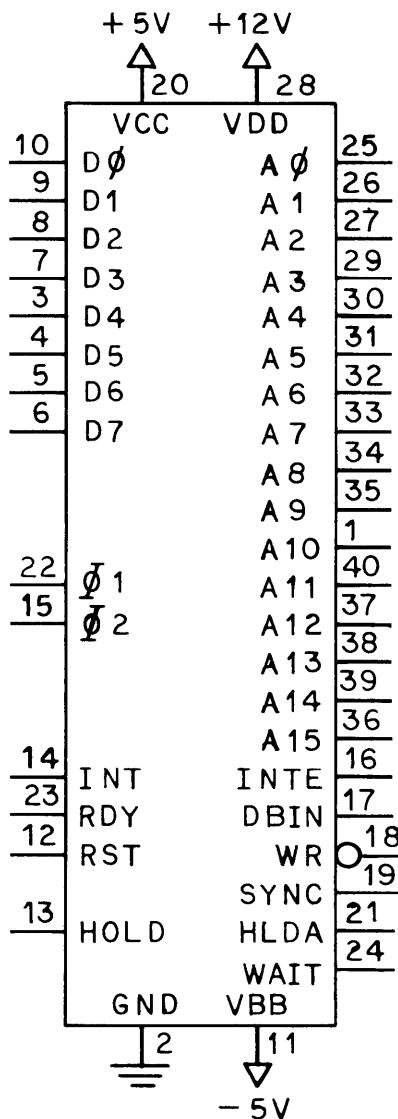
The 8080A also contains an Arithmetic and Logic Unit (ALU), containing an 8-bit accumulator (ACC), an 8-bit temporary accumulator (ACT), an 8-bit temporary register (TMP), and a 5-bit flag register. All arithmetic and logic instructions are performed in this section.

The third major part of the 8080A contains the Instruction Register, Instruction Decoder, and all timing and control logic. The last major portion is the Data Bus Buffer, a 3-state bi-directional 8-bit latch that serves to isolate the the MPU's internal data bus from the external bus.

The instruction set consists of over 100 different instructions, which provide conditional and unconditional branching, decimal and binary arithmetic, and logical, register-to-register, stack control, memory reference, and I/O instructions. Up to 256 input ports and 256 output ports can be addressed. Instructions may be either one, two, or three 8-bit bytes in length. Memory can be referenced four ways: direct, register, register indirect, and immediate. Non memory-reference instructions can be executed in 2 microseconds when a 2 MHz clock is used. The sequential program execution can be interrupted by driving the INT input high.

The 8080A uses its internal stack pointer to access external memory, allowing it to handle multiple-level priority interrupts. This also allows adequate subroutine nesting.

Logic Symbol

Loading:

Outputs   1.2 Unit Loads

Mnemonic	Description	D7	D6	D5	D4	D3	D2	D1	D0	Clock[2] Cycles
MOV r1,r2	Move register to register	0	1	D	D	D	S	S	S	5
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart (3)	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4

Notes:

1)

	Register							
	A	B	C	D	E	H	L	Mem
DDD or SSS	111	000	001	010	011	100	101	110

2) Two possible cycle times (11/17 or 5/11) indicate instruction cycles dependent on condition flags.

3) After a Restart instruction, the next instruction is fetched from memory at the address eight times AAA.

1. The first memory cycle (M1) is always an instruction fetch; the first (or only) byte, containing the op code, is fetched during this cycle.

2. If the READY input from memory is not high during T2 of each memory cycle, the processor will enter a wait state (TW) until READY is sampled as high.

3. States T4 and T5 are present, as required, for operations which are completely internal to the CPU. The contents of the internal bus during T4 and T5 are available at the data bus; this is designed for testing purposes only. An "X" denotes that the state is present, but is only used for such internal operations as instruction decoding.

4. Only register pairs rp = B (registers B and C) or rp = D (registers D and E) may be specified.

5. These states are skipped.

6. Memory read sub-cycles; an instruction or data word will be read.

7. Memory write sub-cycle.

8. The READY signal is not required during the second and third sub-cycles (M2 and M3). The HOLD signal is accepted during M2 and M3. The SYNC signal is not generated during M2 and M3. During the execution of DAD, M2 and M3 are required for an internal register-pair add; memory is not referenced.

9. The results of these arithmetic, logical or rotate instructions are not moved into the accumulator (A) until state T2 of the next instruction cycle. That is, A is loaded while the next instruction is being fetched; this overlapping of operations allows for faster processing.

10. If the value of the least significant 4-bits of the accumulator is greater than 9 or if the auxiliary carry bit is set, 6 is added to the accumulator. If the value of the most significant 4-bits of the accumulator is now greater than 9, or if the carry bit is set, 6 is added to the most significant 4-bits of the accumulator.

11. This represents the first sub-cycle (the instruction fetch) of the next instruction cycle.

12. If the condition was met, the contents of the register pair WZ are output on the address lines (A_{0-15}) instead of the contents of the program counter (PC).

13. If the condition was not met, sub-cycles M4 and M5 are skipped; the processor instead proceeds immediately to the instruction fetch (M1) of the next instruction cycle.

14. If the condition was not met, sub-cycles M2 and M3 are skipped; the processor instead proceeds immediately to the instruction fetch (M1) of the next instruction cycle.

15. Stack read sub-cycle.

16. Stack write sub-cycle.

17. CONDITION   CCC

CONDITION		CCC
NZ	— not zero (Z = 0)	000
Z	— zero (Z = 1)	001
NC	— no carry (CY = 0)	010
C	— carry (CY = 1)	011
PO	— parity odd (P = 0)	100
PE	— parity even (P = 1)	101
P	— plus (S = 0)	110
M	— minus (S = 1)	111

18. I/O sub-cycle: the I/O port's 8-bit select code is duplicated on address lines 0-7 (A_{0-7}) and 8-15 (A_{8-15}).

19. Output sub-cycle.

20. The processor will remain idle in the halt state until an interrupt, a reset or a hold is accepted. When a hold request is accepted, the CPU enters the hold mode; after the hold mode is terminated, the processor returns to the halt state. After a reset is accepted, the processor begins execution at memory location zero. After an interrupt is accepted, the processor executes the instruction forced onto the data bus (usually a restart instruction).
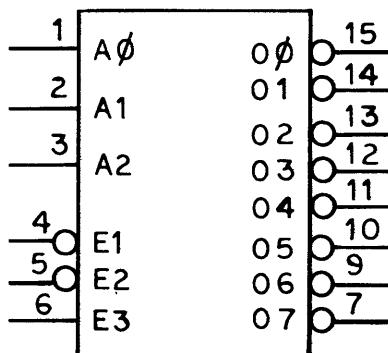
SSS or DDD	Value	rp	Value
A	111	B	00
B	000	D	01
C	001	H	10
D	010	SP	11
E	011		
H	100		
L	101		

MNEMONIC	OP CODE		M1[1]					M2		
	D7 D6 D5 D4	D3 D2 D1 D0	T1	T2[2]	T3	T4	T5	T1	T2[2]	T3
MOV r1,r2	0 1 D D	D S S S	PC OUT STATUS	PC = PC +1	INST→TMP/IR	(SSS)→TMP	(TMP)→DDD			
MOV r, M	0 1 D D	D 1 1 0				X[3]		HL OUT STATUS[6]	DATA→DDD	
MOV M, r	0 1 1 1	0 S S S				(SSS)→TMP		HL OUT STATUS[7]	(TMP)→DATA BUS	
SPHL	1 1 1 1	1 0 0 1				(HL)————→SP				
MVI r, data	0 0 D D	D 1 1 0				X		PC OUT STATUS[6]	B2→DDDD	
MVI M, data	0 0 1 1	0 1 1 0				X			B2→TMP	
LXI rp, data	0 0 R P	0 0 0 1				X			PC = PC + 1 B2→r1	
LDA addr	0 0 1 1	1 0 1 0				X			PC = PC + 1 B2→Z	
STA addr	0 0 1 1	0 0 1 0				X			PC = PC + 1 B2→Z	
LHLD addr	0 0 1 0	1 0 1 0				X			PC = PC + 1 B2→Z	
SHLD addr	0 0 1 0	0 0 1 0				X		PC OUT STATUS[6]	PC = PC + 1 B2→Z	
LDAX rp[4]	0 0 R P	1 0 1 0				X		rp OUT STATUS[6]	DATA→A	
STAX rp[4]	0 0 R P	0 0 1 0				X		rp OUT STATUS[7]	(A)→DATA BUS	
XCHG	1 1 1 0	1 0 1 1				(HL)←→(DE)				
ADD r	1 0 0 0	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)→A	
ADD M	1 0 0 0	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA→TMP	
ADI data	1 1 0 0	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2→TMP	
ADC r	1 0 0 0	1 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)+CY→A	
ADC M	1 0 0 0	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA→TMP	
ACI data	1 1 0 0	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2→TMP	
SUB r	1 0 0 1	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)-(TMP)→A	
SUB M	1 0 0 1	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA→TMP	
SUI data	1 1 0 1	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2→TMP	
SBB r	1 0 0 1	1 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)-(TMP)-CY→A	
SBB M	1 0 0 1	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA→TMP	
SBI data	1 1 0 1	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2→TMP	
INR r	0 0 D D	D 1 0 0				(DDD)→TMP (TMP) + 1→ALU	ALU→DDD			
INR M	0 0 1 1	0 1 0 0				X		HL OUT STATUS[6]	DATA→TMP (TMP)+1→ALU	
DCR r	0 0 D D	D 1 0 1				(DDD)→TMP (TMP)+1→ALU	ALU→DDD			
DCR M	0 0 1 1	0 1 0 1				X		HL OUT STATUS[6]	DATA→TMP (TMP)-1→ALU	
INX rp	0 0 R P	0 0 1 1				(RP) + 1————→RP				
DCX rp	0 0 R P	1 0 1 1				(RP) - 1————→RP				
DAD rp[8]	0 0 R P	1 0 0 1				X		(ri)→ACT	(L)→TMP, (ACT)+(TMP)→ALU	ALU→L, CY
DAA	0 0 1 0	0 1 1 1				DAA→A, FLAGS[10]				
ANA r	1 0 1 0	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)→A	
ANA M	1 0 1 0	0 1 1 0	PC OUT STATUS	PC = PC +1	INST→TMP/IR	(A)→ACT		HL OUT STATUS[6]	DATA→TMP	

4-36

M3			M4			M5				
T1	T2[2]	T3	T1	T2[2]	T3	T1	T2[2]	T3	T4	T5
HL OUT STATUS[7]	(TMP) → DATA BUS									
PC OUT STATUS[6]	PC = PC + 1	B3 → rh								
	PC = PC + 1	B3 → W	WZ OUT STATUS[6]	DATA → A						
	PC = PC + 1	B3 → W	WZ OUT STATUS[7]	(A) → DATA BUS						
	PC = PC + 1	B3 → W	WZ OUT STATUS[6]	DATA → L, WZ = WZ + 1		WZ OUT STATUS[6]		DATA → H		
PC OUT STATUS[6]	PC = PC + 1	B3 → W	WZ OUT STATUS[7]	(L) → DATA BUS, WZ = WZ + 1		WZ OUT STATUS[7]		(H) → DATA BUS		
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)+CY→A									
[9]	(ACT)+(TMP)+CY→A									
[9]	(ACT)-(TMP)→A									
[9]	(ACT)-(TMP)→A									
[9]	(ACT)-(TMP)-CY→A									
[9]	(ACT)-(TMP)-CY→A									
HL OUT STATUS[7]	ALU → DATA BUS									
HL OUT STATUS[7]	ALU → DATA BUS									
(rh)→ACT	(H)→TMP (ACT)+(TMP)+CY→ALU	ALU→H, CY								
[9]	(ACT)+(TMP)→A									

MNEMONIC	OP CODE D7 D6 D5 D4	D3 D2 D1 D0	M1[1] T1	T2[2]	T3	T4	T5	M2 T1	T2[2]	T3
ANI data	1 1 1 0	0 1 1 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2	→TMP
XRA r	1 0 1 0	1 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)+(TPM)→A	
XRA M	1 0 1 0	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
XRI data	1 1 1 0	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2	→TMP
ORA r	1 0 1 1	0 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)+(TMP)→A	
ORA M	1 0 1 1	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
ORI data	1 1 1 1	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2	→TMP
CMP r	1 0 1 1	1 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)-(TMP), FLAGS	
CMP M	1 0 1 1	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
CPI data	1 1 1 1	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2	→TMP
RLC	0 0 0 0	0 1 1 1				(A)→ALU ROTATE		[9]	ALU→A, CY	
RRC	0 0 0 0	1 1 1 1				(A)→ALU ROTATE		[9]	ALU→A, CY	
RAL	0 0 0 1	0 1 1 1				(A), CY→ALU ROTATE		[9]	ALU→A, CY	
RAR	0 0 0 1	1 1 1 1				(A), CY→ALU ROTATE		[9]	ALU→A, CY	
CMA	0 0 1 0	1 1 1 1				(Ā)→A				
CMC	0 0 1 1	1 1 1 1				C̄Y→CY				
STC	0 0 1 1	0 1 1 1				1→CY				
JMP addr	1 1 0 0	0 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1 B2	→Z
J cond addr[17]	1 1 C C	C 0 1 0				JUDGE CONDITION		PC OUT STATUS[6]	PC = PC + 1 B2	→Z
CALL addr	1 1 0 0	1 1 0 1				SP = SP − 1		PC OUT STATUS[6]	PC = PC + 1 B2	→Z
C cond addr[17]	1 1 C C	C 1 0 0				JUDGE CONDITION IF TRUE, SP = SP − 1		PC OUT STATUS[6]	PC = PC + 1 B2	→Z
RET	1 1 0 0	1 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA	→Z
R cond addr[17]	1 1 C C	C 0 0 0			INST→TMP/IR	JUDGE CONDITION[14]		SP OUT STATUS[15]	SP = SP + 1 DATA	→Z
RST n	1 1 N N	N 1 1 1			φ→W INST→TMP/IR	SP = SP − 1		SP OUT STATUS[16]	SP = SP − 1 (PCH)	→DATA BUS
PCHL	1 1 1 0	1 0 0 1			INST→TMP/IR	(HL) → PC				
PUSH rp	1 1 R P	0 1 0 1				SP = SP − 1		SP OUT STATUS[16]	SP = SP − 1 (rh)	→DATA BUS
PUSH PSW	1 1 1 1	0 1 0 1				SP = SP − 1		SP OUT STATUS[16]	SP = SP − 1 (A)	→DATA BUS
POP rp	1 1 R P	0 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA	→r1
POP PSW	1 1 1 1	0 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA	→FLAGS
XTHL	1 1 1 0	0 0 1 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA	→Z
IN port	1 1 0 1	1 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1 B2	→Z, W
OUT port	1 1 0 1	0 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1 B2	→Z, W
EI	1 1 1 1	1 0 1 1				SET INTE F/F				
DI	1 1 1 1	0 0 1 1				RESET INTE F/F				
HLT	0 1 1 1	0 1 1 0				X		PC OUT STATUS	HALT MODE[20]	
NOP	0 0 0 0	0 0 0 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	X				

M3			M4			M5						
T1	T2[2]	T3	T1	T2[2]	T3	T1	T2[2]	T3	T4	T5		
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)-(TMP); FLAGS											
[9]	(ACT)-(TMP); FLAGS											
PC OUT STATUS[6]	PC = PC + 1 B3 →W										WZ OUT STATUS[11]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1 B3 →W										WZ OUT STATUS[11,12]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1 B3 →W		SP OUT STATUS[16]	(PCH) SP = SP - 1	→DATA BUS	SP OUT STATUS[16]	(PCL)→ DATA BUS				WZ OUT STATUS[11]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1 B3 →W[13]		SP OUT STATUS[16]	(PCH) SP = SP - 1	→DATA BUS	SP OUT STATUS[16]	(PCL)→ DATA BUS				WZ OUT STATUS[11,12]	(WZ) + 1 → PC
SP OUT STATUS[15]	SP = SP + 1 DATA →W										WZ OUT STATUS[11]	(WZ) + 1 → PC
SP OUT STATUS[15]	SP = SP + 1 DATA →W										WZ OUT STATUS[11,12]	(WZ) + 1 → PC
SP OUT STATUS[16]	(TMP = 00NNN000) →Z (PCL)→DATA BUS										WZ OUT STATUS[11]	(WZ) + 1 → PC
SP OUT STATUS[16]	(rl) →DATA BUS											
SP OUT STATUS[16]	FLAGS →DATA BUS											
SP OUT STATUS[15]	SP = SP + 1 DATA→rh											
SP OUT STATUS[15]	SP = SP + 1 DATA→A											
SP OUT STATUS[15]	DATA→W		SP OUT STATUS[16]	(H) →DATA BUS		SP OUT STATUS[16]	(L)→ DATA BUS		(WZ)→HL			
WZ OUT STATUS[18]	DATA →A											
WZ OUT STATUS[18]	(A) →DATA BUS											

Logic Symbol

```
      1  ┌──────────┐
 ─────────│ A∅    0∅ │o──15──
      2   │          │
 ─────────│ A1    01 │o──14──
      3   │          │   13
 ─────────│ A2    02 │o──────
      4   │       03 │o──12──
 ────o────│ E1    04 │o──11──
      5   │       05 │o──10──
 ────o────│ E2    06 │o──9───
      6   │       07 │o──7───
 ─────────│ E3       │
          └──────────┘
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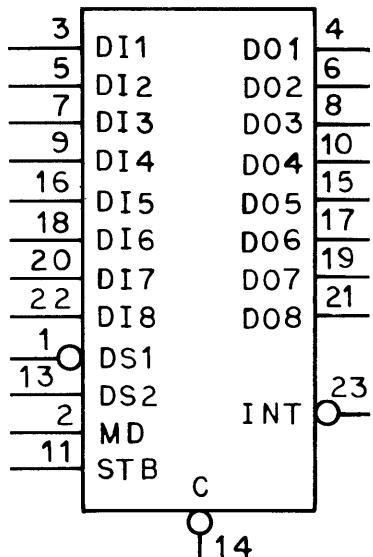
VCC-16, GND-8

Truth Table
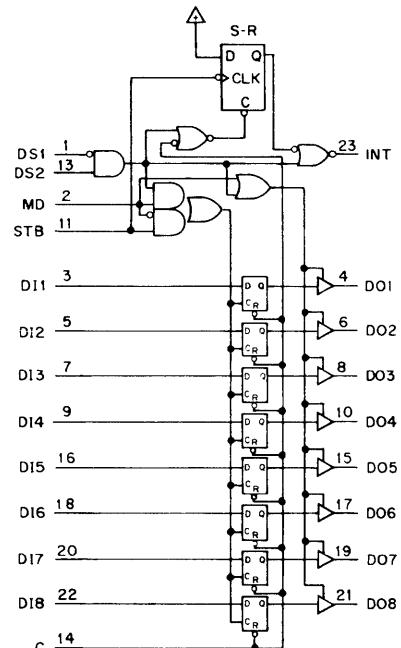
Inputs						Outputs							
A0	A1	A2	E1	E2	E3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

Loading:	8205	25LS138
Inputs	.16 Unit Load	.25 Unit Load
Outputs	6 Unit Loads	5 Unit Loads

This device contains an 8-bit latch with three-state output buffers and logic to allow independent control of input and output. It also has an internal Service Request flip-flop for generating interrupts for the MPU.

Logic Symbol

VCC-24, GND-12

Logic Diagram

Function Table

Mode	Inputs				Outputs	Internal
	MD	DS1=L DS2=H	STB	DI1-8	DO1-8	Latches
Input	L	No	L	X	Hi-Z	No Change
	L	No	H	L	Hi-Z	Load L
	L	No	H	H	Hi-Z	Load H
	L	Yes	L	X	Previous H/L	No Change
	L	Yes	H	H	H	Load H
	L	Yes	H	L	L	Load L
Output	H	No	X	X	Previous H/L	Read
	H	Yes	X	H	H	Load H
	H	Yes	X	L	L	Load L
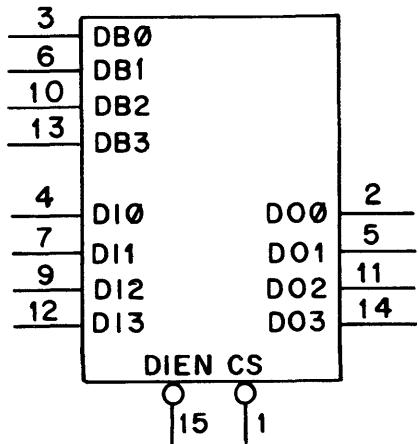
Loading:

Inputs	
C, DS2, DI1-8, STB	.16 Unit Load
MD	.46 Unit Load
DS1	.62 Unit Load
Outputs	9 Unit Loads
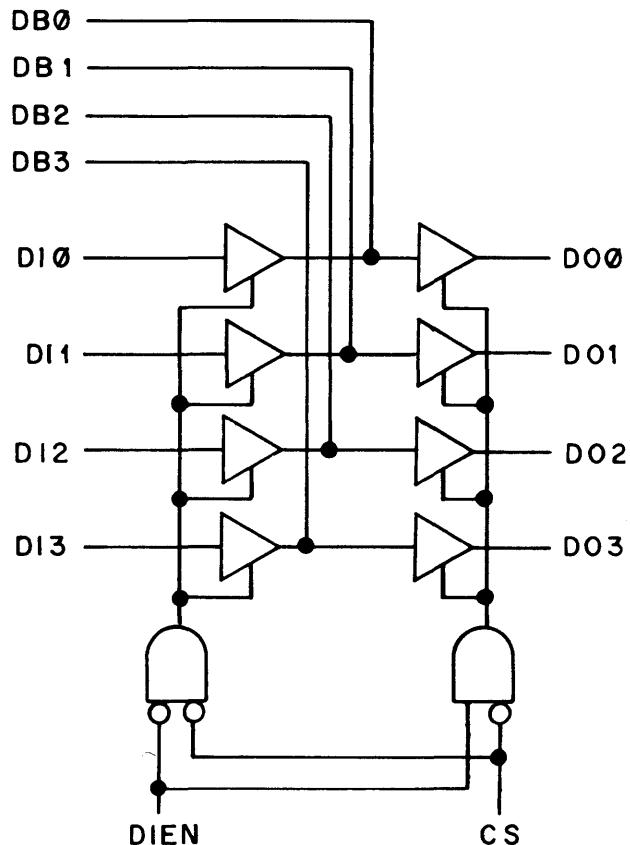
Interrupt Generation

Inputs			S-R	Output
DS1=L DS2=H	C	STB	ff	INT
No	L	L	L	H
No	H	L	No Change	
No	H	▼	H	L
Yes	X	X	X	L

Logic Symbol

Logic Diagram

VCC-16, GND-8

Loading:
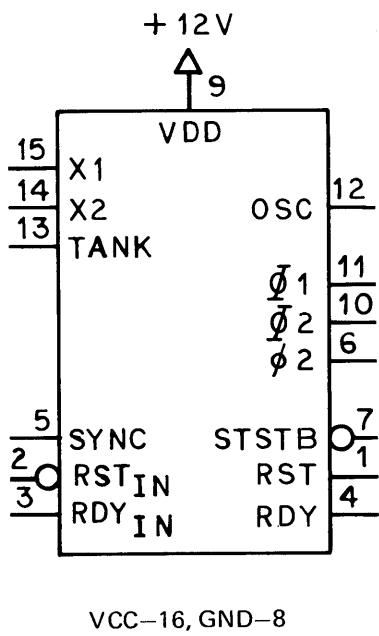
Inputs
    CS,DIEN   .31 Unit Load
    DI,DB   .16 Unit Load

Outputs
    DB   33 Unit Loads
    DO   9 Unit Loads

The device provides the 12 volt, non-overlapping clocks required by the 8080 MPU. The frequency of the output signals is determined by an external crystal (crystal frequency = 9 times clock frequency). It also provides power-up Reset and Status Strobe functions.

Logic Symbol

+ 12 V

VCC—16, GND—8

Loading:

Inputs	.16 Unit Load
Outputs	
RDY,RST,STSTB	1.5 Unit Loads
ϕ2,OSC	9 Unit Loads

Clock Generator

The clock generator provides the 12 volt ϕ1 and ϕ2 signals needed by the 8080, plus a ϕ2 TTL signal for related logic.

Status Strobe

The SYNC signal from the 8080 is used to generate STSTB (low active) at the earliest possible moment that the 8080 status data is stable on the MPU data bus (at the beginning of each 8080 machine cycle). This STSTB signal is used by the 8228 System Controller IC. STSTB is also developed when RST is produced.

Reset

A pulse is developed automatically at turn-on when power reaches a minimum predetermined value. A level is produced when the RST-IN input is driven low.
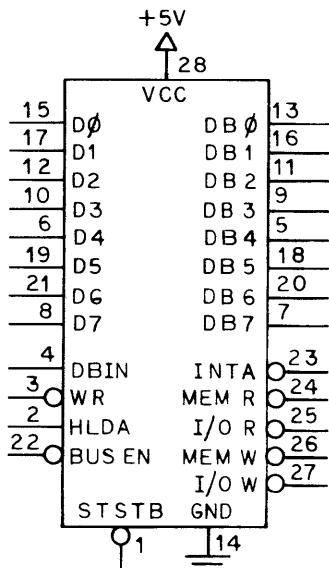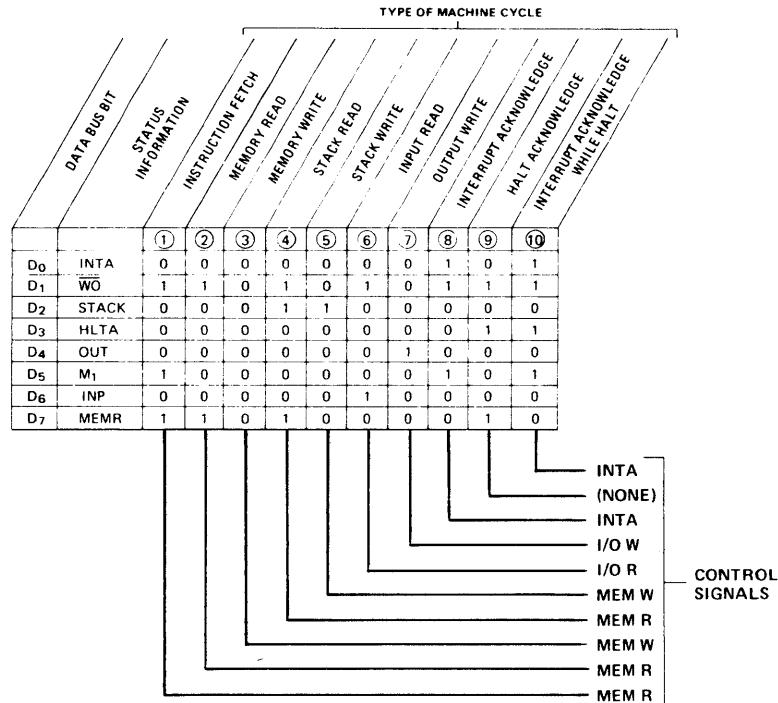
Ready

The RDY input to the 8080 must meet certain critical timing requirements. An asynchronous signal can be applied to the 8224 on the RDY-IN input, and the RDY output of the 8224 will be synchronized properly with the 8080.

This is a combination bi-directional 8-bit bus driver and system controller for use with the 8080 MPU.
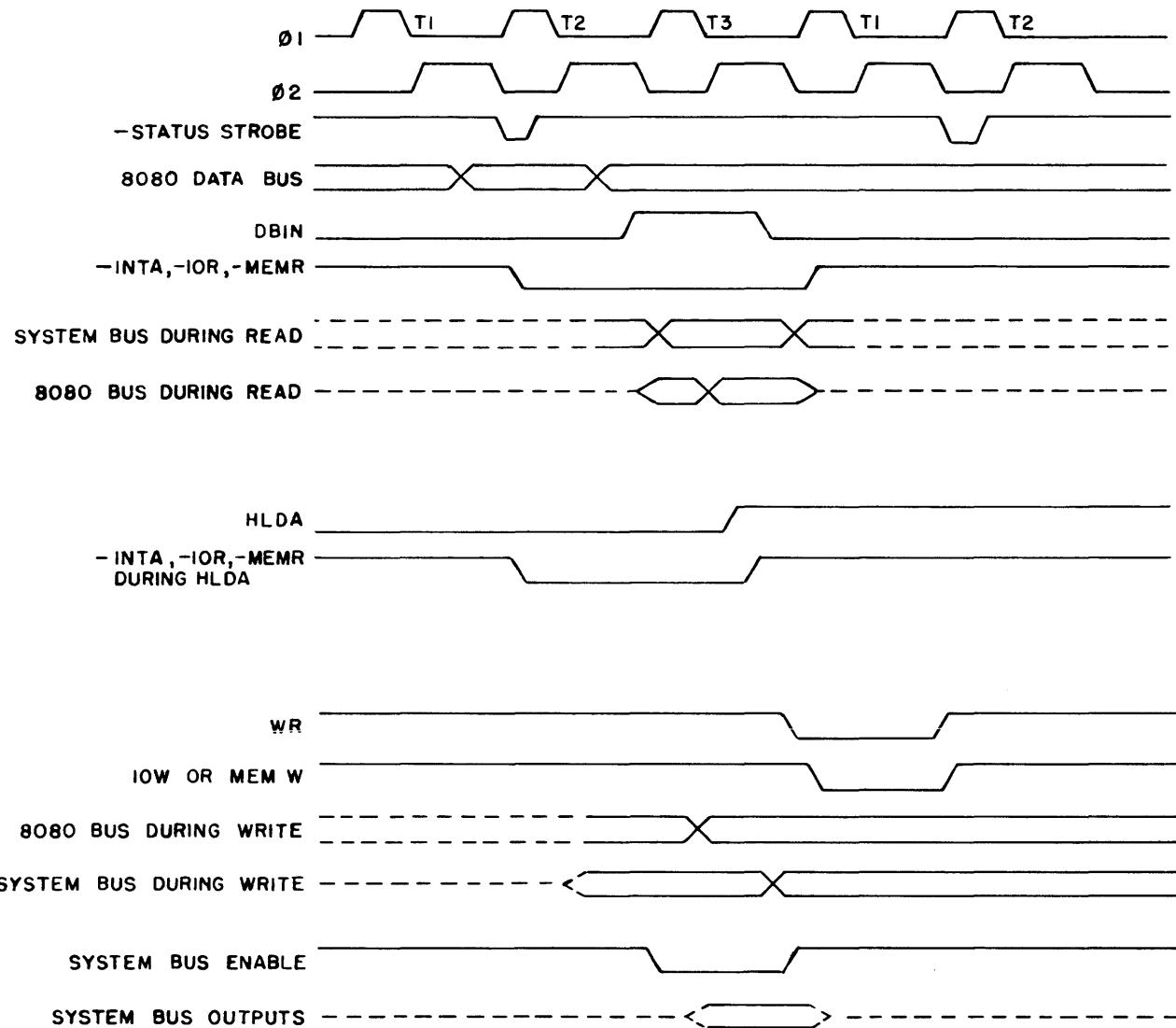
Logic Symbol

Status Word Chart

		INSTRUCTION FETCH	MEMORY READ	MEMORY WRITE	STACK READ	STACK WRITE	INPUT READ	OUTPUT WRITE	INTERRUPT ACKNOWLEDGE	HALT ACKNOWLEDGE	INTERRUPT ACKNOWLEDGE WHILE HALT
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

CONTROL SIGNALS:
INTA
(NONE)
INTA
I/O W
I/O R
MEM W
MEM R
MEM W
MEM R
MEM R

Bus Driver

When driving into the 8080 MPU, this device provides a minimum of +3.6 volts, well above the +3.3 volts required by the 8080. On 8080 output, this device provides 10 ma of drive current, as opposed to the 8080's 1.9 ma. The direction of data flow on the bus is controlled by the System Controller portion of this IC. The BUS EN input turns the bus driver on and off; when BUS EN is high, the bus outputs are in the three-state high-impedance condition.

System Controller

At the beginning of each 8080 machine cycle, the status information from the 8080 is loaded into a 6-bit latch inside the 8228. The STSTB signal from the 8224 IC strobes this latch. The outputs of this latch are then gated by the DBIN, WR, and HLDA outputs from the 8080 to produce the system control outputs MEM R, MEM W, I/O R, I/O W, and INTA. Interrupt Acknowledge (INTA) is normally used to gate instruction data from the peripheral circuitry onto the data bus after the MPU has been interrupted. A special feature of this IC allows an RST7 (Restart 7) instruction to be gated into the MPU automatically whenever the MPU is interrupted. This is accomplished by connecting the INTA output to +12 volts through a 1K resistor.

Type 8228
Timing Waveforms

Ø1   T1   T2   T3   T1   T2

Ø2

−STATUS STROBE

8080 DATA BUS

DBIN

−INTA,−IOR,−MEMR

SYSTEM BUS DURING READ

8080 BUS DURING READ

HLDA

−INTA,−IOR,−MEMR
DURING HLDA

WR

IOW OR MEM W

8080 BUS DURING WRITE

SYSTEM BUS DURING WRITE

SYSTEM BUS ENABLE

SYSTEM BUS OUTPUTS

Loading:
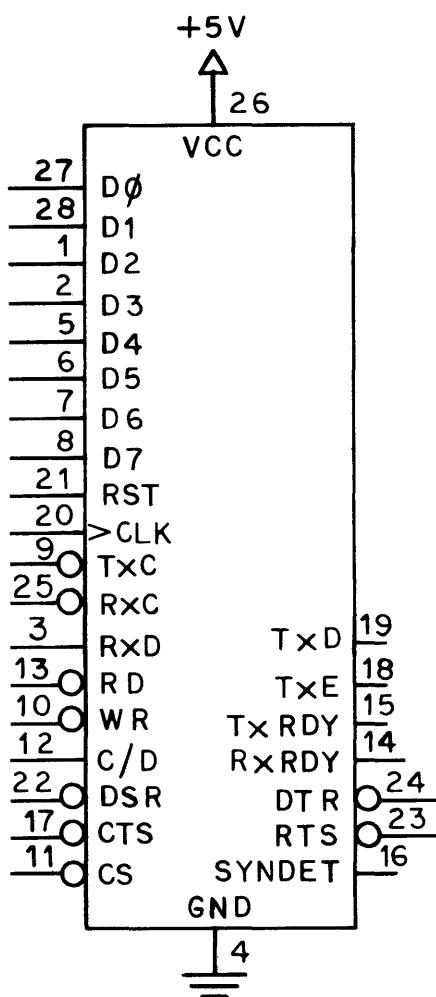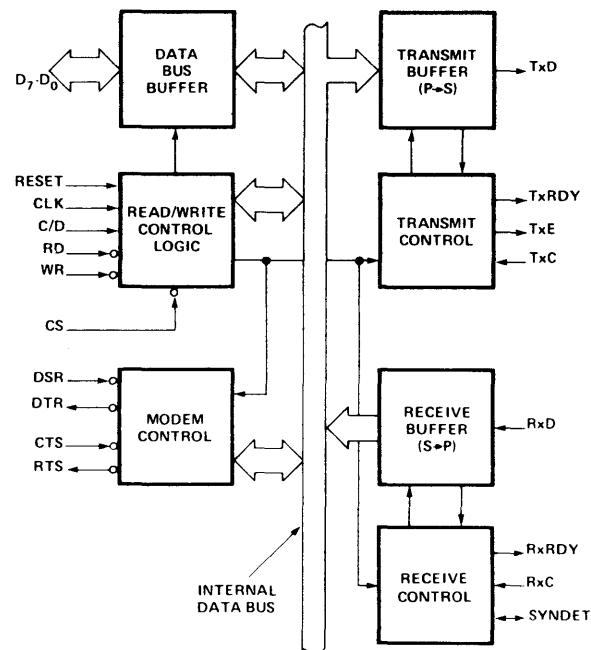
Inputs
D2,D6	.46 Unit Load
STSTB	.31 Unit Load
Others	.16 Unit Load

Outputs
D0-D7	1.25 Unit Loads
Others	9 Unit Loads

The USART is used to interface the serial data channel of a terminal or communications device to the parallel data channel of a computer or terminal. The transmitter section converts parallel data into serial words with start bits, stop bits, and (if desired) parity bits. The receiver section converts serial data into parallel words, while stripping off the start bits and stop bits, checking word length, and, if desired, checking parity. Both the receiver and transmitter are double buffered. Parallel words can contain up to eight bits. Serial word length can be 5, 6, 7, or 8 bits. Parity can be even or odd, or parity checking and generation can be inhibited. The number of stop bits can be either one or two (or 1-1/2 when word length = 5 bits). Transmitting and receiving can occur simultaneously (full-duplex). Transmit and Receive Clocks must be supplied at 1, 16, or 64 times the desired baud rate.

Logic Symbol

Block Diagram

Loading:

Outputs   1 Unit Load

Data Bus Buffer

This is a three-state, bi-directional, 8-bit buffer used to interface the 8251 to the MPU system data bus. Data, control words, command words, and status information are transferred through this buffer.

Read/Write Control Logic

Control inputs from the MPU system are received and stored here. Control/command bits stored here influence subsequent 8251 operation.

RST (Reset). A high on this input forces the 8251 into an "idle" condition, where it remains until a Mode instruction is received.

CLK (Clock). This input is normally driven by the $\phi 2$ (TTL) output of the 8224 Clock Generator, to provide timing for internal operations. This clock must be greater than 30 times the RxC and TxC frequency for synchronous operation and 4.5 times for asynchronous operation.

WR (Write). A low on this input signals the 8251 that the MPU is writing (outputting) to the 8251.

RD (Read). A low on this input signals the 8251 that the MPU is reading from the 8251.

C/D (Control/Data). This input, along with the WR and RD inputs, informs the 8251 whether the word on the data bus is a data, control, or status word.

C/D	WR	RD	Function
L	X	X	Data
H	H	L	Status
H	L	H	Control

CS (Chip Select). A low on this input enables the 8251. A high disables all reading and writing and drives all outputs into the high-impedance state.

Modem Control

These inputs and outputs can be used to interface to the modem, or they can be used for other functions as desired.

DSR (Data Set Ready). This input is normally used to test modem conditions such as Data Set Ready. Its condition is tested by the MPU performing a status read operation.

CTS (Clear to Send). A low on this input enables the 8251 to transmit serial data if the TxN bit in the command byte is set to a 1.

DTR (Data Terminal Ready) and RTS (Request to Send). These two outputs can be set low by programming the appropriate bits in the command instruction word. They are normally used for modem control.

Transmit Buffer

This buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits, and outputs a composite serial stream of data on the TxD pin. It consists essentially of two buffers, a transmit buffer and a holding register.

Transmit Control

This section controls the Transmit Buffer and provides the signals necessary to synchronize transmission with the MPU.

TxRDY (Transmit Ready). This output goes high to inform the MPU that the transmit holding register is ready to accept the next character. The MPU can also check this condition by performing a status read operation. This output goes low (at least momentarily) when a character is received from the MPU, and returns high when the character is transferred from the holding register to the transmit buffer.

TxE (Transmitter Empty). This output goes high when the transmitter has no more characters to transmit. It goes low when a character is received from the MPU.

TxC (Transmit Clock). The signal applied to this input controls the rate of data transmission. In synchronous transmission, the baud rate is the same as the TxC rate. In asynchronous transmission, the TxC rate can be 1, 16, or 64 times the baud rate, determined by the Mode instruction. The serial data is shifted out of the 8251 on the falling edge of TxC.

Receive Buffer

This buffer accepts serial data from the RxD input, converts it to parallel format, checks for bits or characters according to the established mode and control words, and provides this data to the MPU.

Receive Control

This section controls the Receive Buffer and provides the signals for synchronizing it with the MPU.

RxRDY (Receiver Ready). This output goes high to inform the MPU that the 8251 has a character ready to be input to the MPU. This condition can also be checked via a status read operation. The output is driven low when the character is received by the MPU (when RD is driven low).
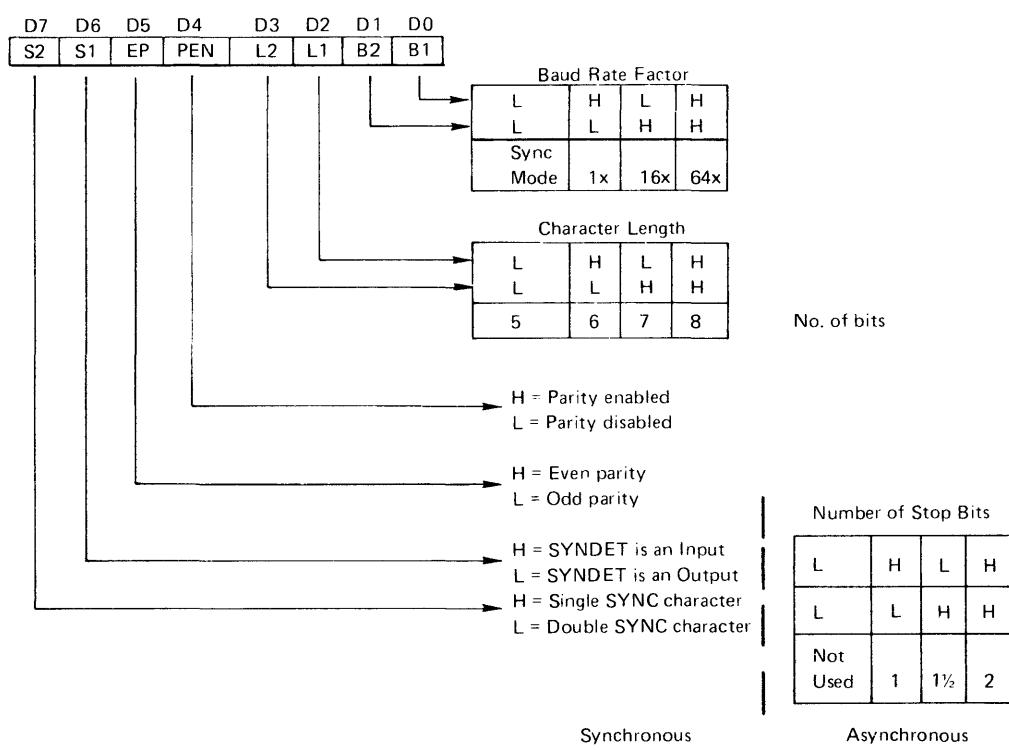
RxC (Receiver Clock). The signal applied to this input controls the rate of data reception. In synchronous mode, the RxC rate must be the same as the baud rate. In asynchronous mode, the RxC rate can be 1, 16, or 64 times the baud rate, as determined by the Mode instruction. The data on the RxD input is sampled and shifted into the 8251 on the rising edge of RxC.

SYNDET (SYNC Detect). This pin is used in synchronous mode only, and it can be used as either an input or an output, programmable through the Control word. When used as an output, it goes high to indicate that the 8251 has received a SYNC character. If the 8251 is programmed to use double SYNC characters, then SYNDET goes high in the middle of the last bit of the second SYNC character. The condition of this output is also available to the MPU via a status read operation, which automatically resets the SYNDET condition.

SYNDET may be used as an input if the check for synchronization is made by external logic. In this case, when SYNDET is driven high, the 8251 begins assembling serial input data into characters on the falling edge of the next RxC.
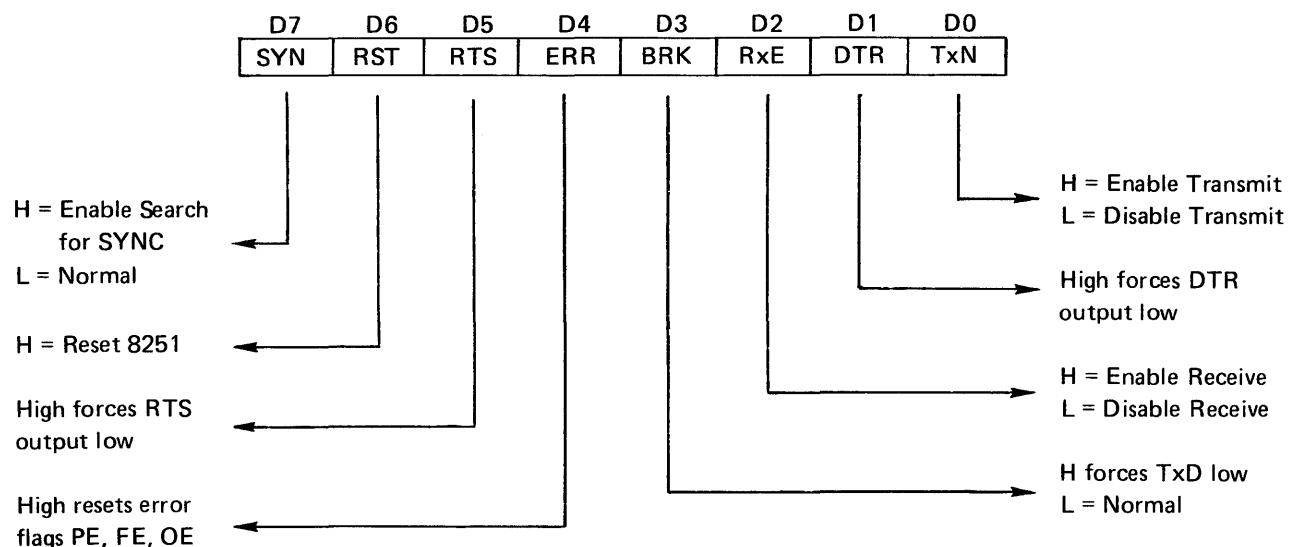
Mode Instruction

The first "control" (C/D high) write after a Reset loads the Mode instruction into the 8251. Any subsequent control writes load Command instructions. The Mode instruction format is as follows:

D7	D6	D5	D4	D3	D2	D1	D0
S2	S1	EP	PEN	L2	L1	B2	B1

Baud Rate Factor

L	H	L	H
L	L	H	H

Sync Mode	1x	16x	64x

Character Length

L	H	L	H
L	L	H	H

5	6	7	8	No. of bits

H = Parity enabled
L = Parity disabled

H = Even parity
L = Odd parity

H = SYNDET is an Input
L = SYNDET is an Output

H = Single SYNC character
L = Double SYNC character

Number of Stop Bits

L	H	L	H
L	L	H	H
Not Used	1	1½	2

Synchronous   Asynchronous
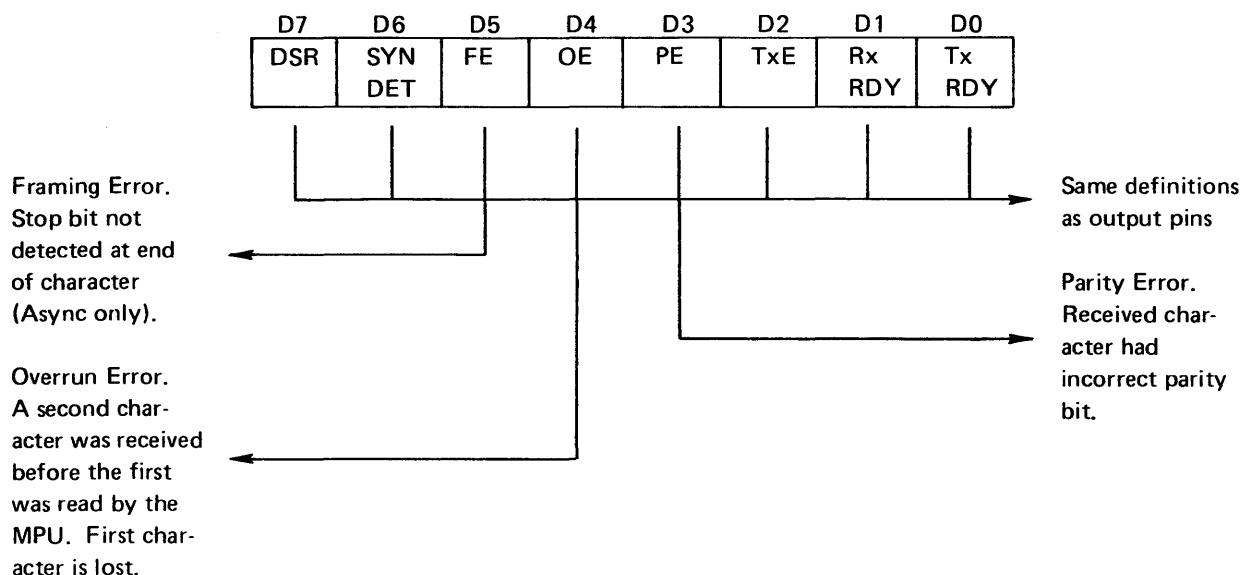
Command Instruction

After the mode instruction has been loaded, subsequent control writes load the Command instruction, as follows:

D7	D6	D5	D4	D3	D2	D1	D0
SYN	RST	RTS	ERR	BRK	RxE	DTR	TxN

H = Enable Search
     for SYNC
L = Normal

H = Reset 8251

High forces RTS
output low

High resets error
flags PE, FE, OE

H = Enable Transmit
L = Disable Transmit

High forces DTR
output low

H = Enable Receive
L = Disable Receive

H forces TxD low
L = Normal
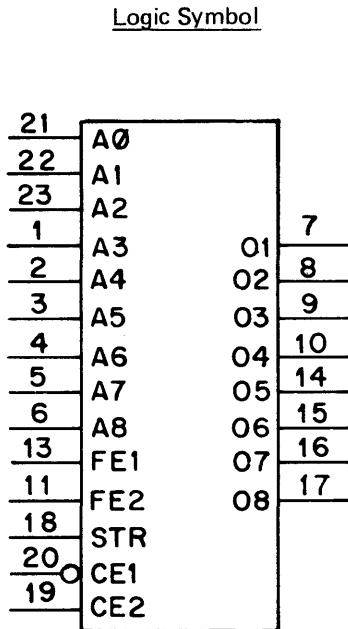
Status Read

When a Read operation is performed with the C/D input high, status is provided to the MPU on the parallel data bus as follows:

D7	D6	D5	D4	D3	D2	D1	D0
DSR	SYN DET	FE	OE	PE	TxE	Rx RDY	Tx RDY

Framing Error.
Stop bit not
detected at end
of character
(Async only).

Overrun Error.
A second character was received
before the first
was read by the
MPU. First character is lost.

Same definitions
as output pins

Parity Error.
Received character had
incorrect parity
bit.

These devices are Programmable Read-Only memories which are normally programmed by the vendor. No truth table appears here because each program requires a separate table. Note that the part number above is the Diablo number for the unprogrammed pROMs: a new number is assigned when the pROM is programmed. Part numbers for programmed pROMs appear on the schematic. Access time is typically 35 ns (60 ns maximum).

There are two modes of operation. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the bit drivers are controlled solely by CE1 and CE2 lines.

In the LATCHED READ mode, outputs are held in their previous state (1, 0, or Hi-Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the Hi-Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the Hi-Z condition if the chip was disabled.

Logic Symbol

Pin	Signal		Signal	Pin
21	AØ			
22	A1			
23	A2			
1	A3	O1		7
2	A4	O2		8
3	A5	O3		9
4	A6	O4		10
5	A7	O5		14
6	A8	O6		15
13	FE1	O7		16
11	FE2	O8		17
18	STR			
20	CE1			
19	CE2			

VCC-24, GND-12

AØ-A8   = Address Inputs
FE1, FE2 = Programming Inputs
STR   = Strobe Input
CE1, CE2 = Chip Enable Inputs
O1-O8   = Data Outputs

Loading:

    Inputs   .1 Unit Load
    Outputs   6 Unit Loads
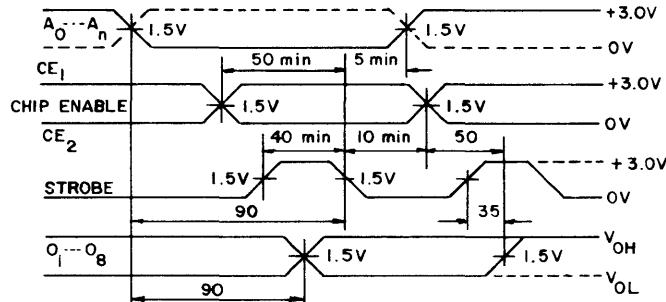
Waveforms
(Times shown are maximum unless noted)
(Times shown are in nanoseconds)
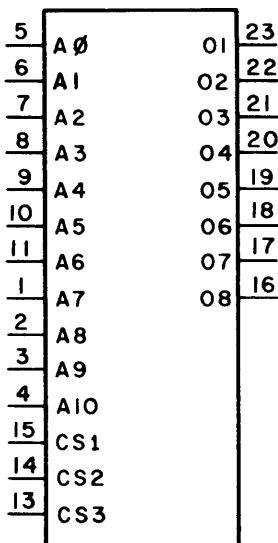
Latched Read

This is a Read-Only Memory that is programmed during manufacture. No part number is given because each program requires a separate part number. Part numbers are given on the schematics. Outputs are 3-state, controlled by three programmable chip-select inputs. Any combination of high- or low-active chip select inputs can be defined, and the desired chip select code is programmed into the chip during manufacture. Maximum access time is 1.5 μs. Only a single power supply voltage (+5V) is required.
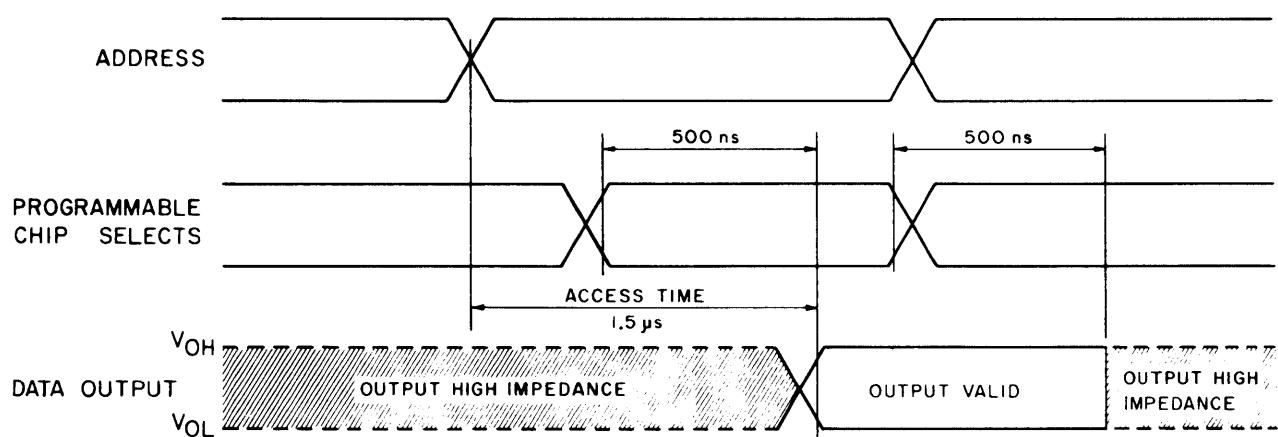
Logic Symbol

```
  5 ┌──────────────┐ 23
────┤ AØ        O1 ├────
  6 │              │ 22
────┤ A1        O2 ├────
  7 │              │ 21
────┤ A2        O3 ├────
  8 │              │ 20
────┤ A3        O4 ├────
  9 │              │ 19
────┤ A4        O5 ├────
 10 │              │ 18
────┤ A5        O6 ├────
 11 │              │ 17
────┤ A6        O7 ├────
  1 │              │ 16
────┤ A7        O8 ├────
  2 │              │
────┤ A8           │
  3 │              │
────┤ A9           │
  4 │              │
────┤ A10          │
 15 │              │
────┤ CS1          │
 14 │              │
────┤ CS2          │
 13 │              │
────┤ CS3          │
    └──────────────┘
```

VCC-24, GND-12

Waveforms
(All times shown are maximum)
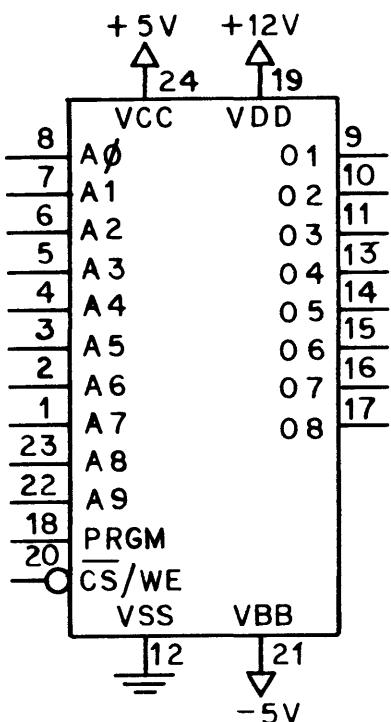
Loading:
        Outputs   1.1 Unit Loads

This Read-Only Memory is programmed at the Diablo factory. It has a transparent quartz lid which allows exposure to ultraviolet light to erase the bit pattern. It is electrically compatible with the type 8308 ROM. Access time is 450 ns. Outputs are 3-state, controlled by the Chip Select (CS) input.
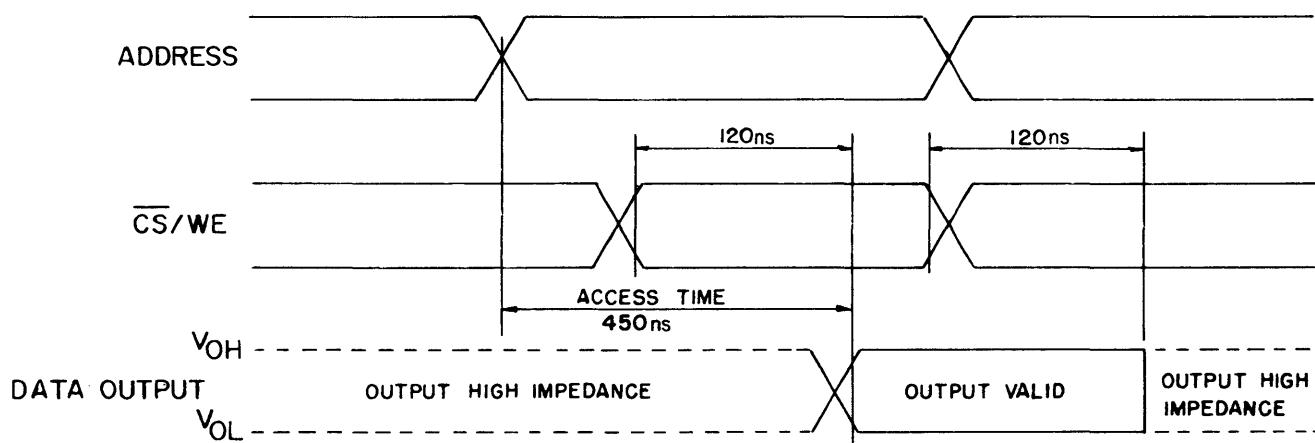
Logic Symbol

VBB = +5V
VCC = +5V
VDD = +12V
VSS = GND

Waveforms
(All times shown are maximum)
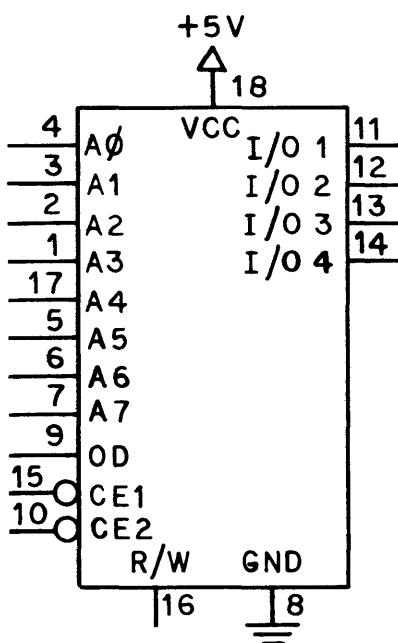
Loading:

Outputs   1 Unit Load
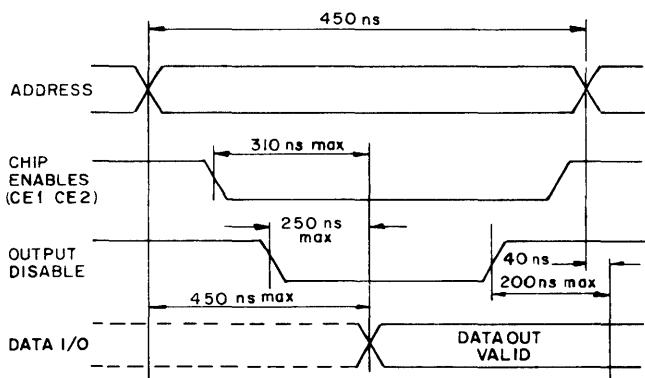
This is the 450 ns member of a family of random-access memories available in several speed ranges. The Output Disable pin (9), when high, drives the Input/Output pins to their high-impedance state.

Logic Symbol
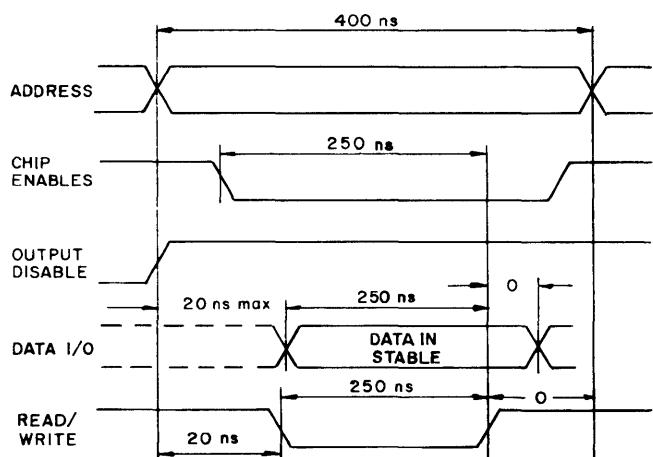
Timing Waveforms
(All times are minimum unless noted)

Read Cycle

Write Cycle

Loading:
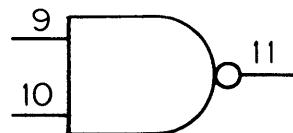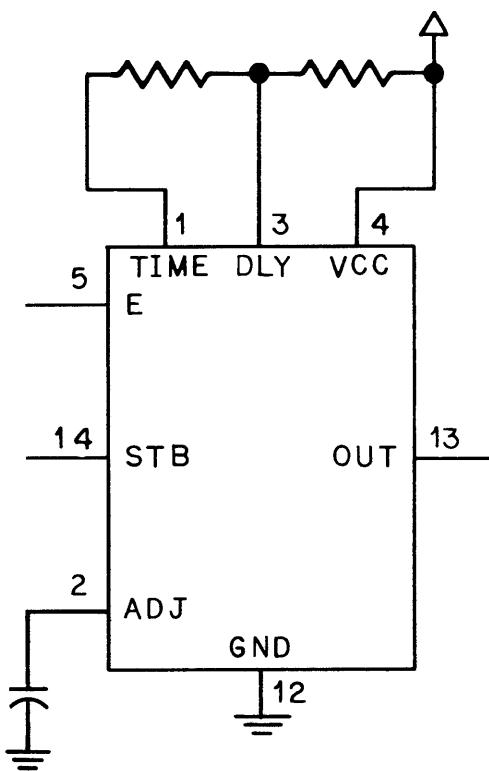
    Outputs   1.25 Unit Loads

This is a custom IC used in Micro Switch keyboards to produce the keyboard Strobe pulses. It includes a repeat circuit with an initial delay and two independent DTL NAND gates. It requires two external resistors and one capacitor: the resistor connected between pins 1 and 3 determines the length of time between repeat pulses; the resistor between pins 3 and 4 adjusts the initial delay (the initial delay is a function of both resistors); the

capacitor determines the length of the entire repeat cycle ("on" time plus "off" time) and also affects the initial delay. The repeat pulses are produced (after the initial delay) when the Enable input is driven high; with Enable Low, the Strobe input pulses pass through unchanged.

Note the non-standard VCC and GND connections.

Logic Symbol

Loading:

Inputs	1 Unit Load
Outputs	
Gate 1 (pin 8)	3.75 Unit Loads
Other	2.5 Unit Loads
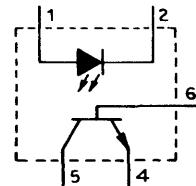
Phototransistor Opto-Isolator   Part No. 42168-XX   Type TIL-117

This circuit element consists of a solid-state gallium arsenide diode lamp optically coupled to an NPN silicon planar phototransistor. Its function is to couple two circuits optically, while isolating them electrically.

Logic Symbol

Absolute Maximum Ratings
(@ 25°C)

Input Diode		Output Transistor	
Forward Current	60 mA	Power Dissipation	150 mW
Power Dissipation	100 mW	VCE	30 V
Reverse Voltage	3 V	VCB	70 V
		VEC	5V

Isolation: 42168-01   1500 volts
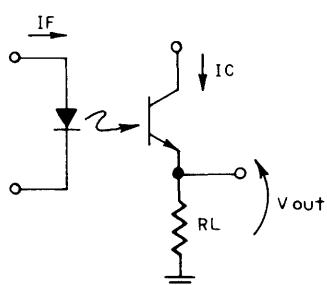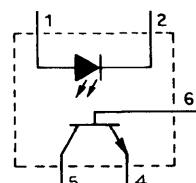
Phototransistor Opto-Isolator   Part No. 42190-01   Type MCT2
                                                                            MCT2E
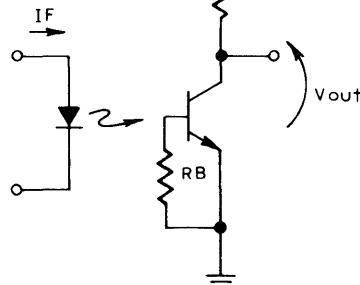
This circuit element consists of a solid-state gallium arsenide diode lamp optically coupled to an NPN silicon planar phototransistor. It is mounted in a six-lead plastic DIP. Its function is to couple two circuits optically, while isolating them electrically.

Logic Symbol

Circuit 1   Circuit 2

Absolute Maximum Ratings
(@ 25°C)

Forward Current	60 mA	Power Dissipation	200 mW
Power Dissipation	200 mW	VCE	30 V
Reverse Voltage	3 V	VCB	70 V
		VEC	7 V

Isolation: 2500 volts

This is a 128 key non-programmed MOS/LSI Scanner, in a 28-Lead dual-in-line package. Used in Cortron Up/Dn stroke keyboard. Supply Voltages:

Vss = 5V at 40 mA.
Vdd = 0V at 50 mA (for TTL outputs).
Vgg = -12V at 40 mA.

The device has 12 TTL/DTL outputs which are capable of sinking 1.6 mA. These outputs are:

Pin		Pin	
12.	$\Phi1$	18.	Flag (FF)
13.	$\Phi3$	19.	Shift Register Out
14.	Strobe	21.-27.	B1 through B7

Each of these outputs has the following specifications:

Logic "1" (high) = 2.4V min. at 100 uA
Logic "0" (low) = 0.4V max. at 1.6 mA

The device has 7 standard TTL/DTL compatible outputs, each capable of sinking 3.2 mA. These outputs are A1 through A7.

Each of these outputs has the following specifications:

Logic "1" (high) = 2.4V min. at 200 uA.
Logic "0" (low) = 0.4V max. at 3.2 mA.

This device has 6 logic inputs:
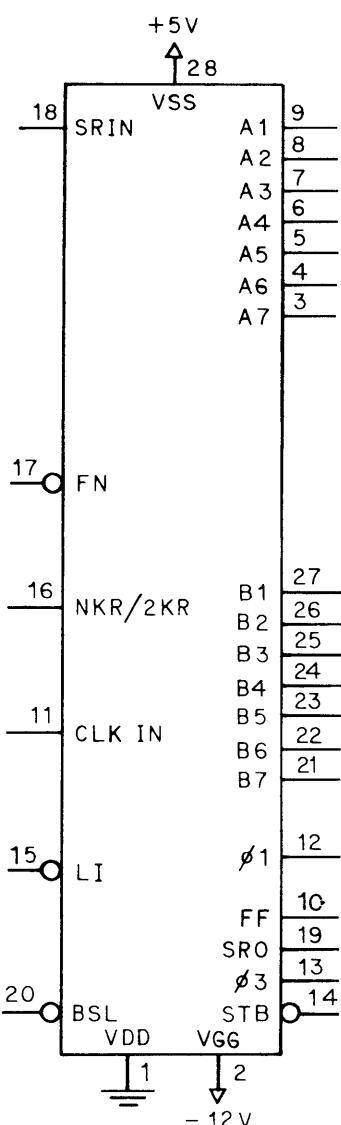
Pin		Pin	
10.	Data in (SRIN)	16.	NKR/2KR
11.	Clock in	17.	Function (FN)
15.	Latch Inhibit	20.	Bypass shift logic

Each input has the following specification:

Vin (Logic 1) = Vss -2V min.
      = Vss +0.3V max.
Vin (Logic 0) = Vgg min.
      = Vss -4.0V max.
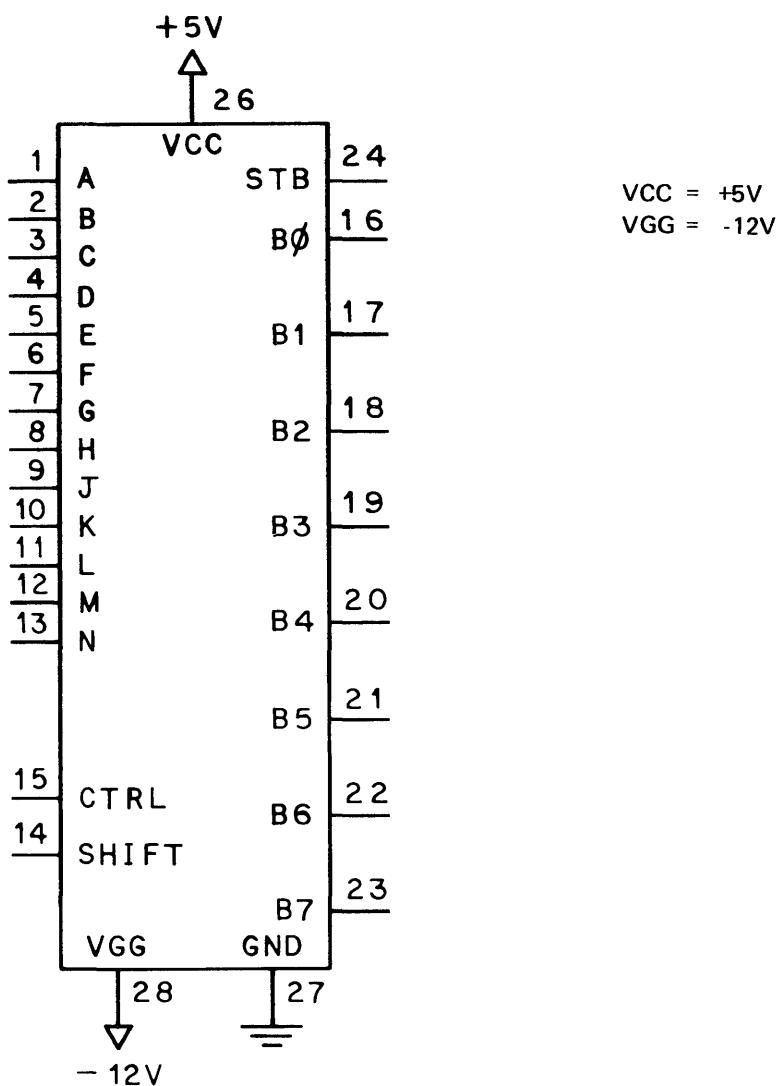
A pull-up resistor is provided for each input on the device.

Logic Symbol
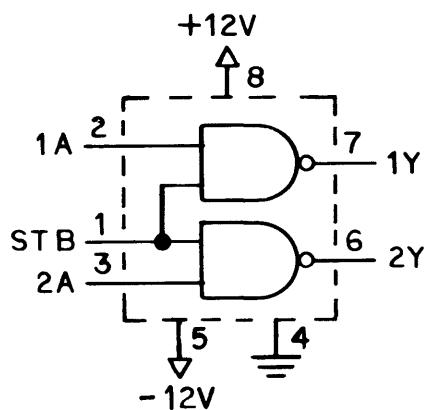
This is a custom IC used in Micro Switch keyboards to accomplish the keyswitch decoding/output encoding functions. It has eight output latches which store the decoded output data until it is replaced by newer data. Note the non-standard power and ground connections.

Logic Symbol

+5V

26 VCC

Pin	Label		Label	Pin
1	A		STB	24
2	B		BØ	16
3	C			
4	D		B1	17
5	E			
6	F		B2	18
7	G			
8	H		B3	19
9	J			
10	K		B4	20
11	L			
12	M		B5	21
13	N			
15	CTRL		B6	22
14	SHIFT		B7	23

VGG   GND
 28   27
-12V

VCC = +5V
VGG = -12V
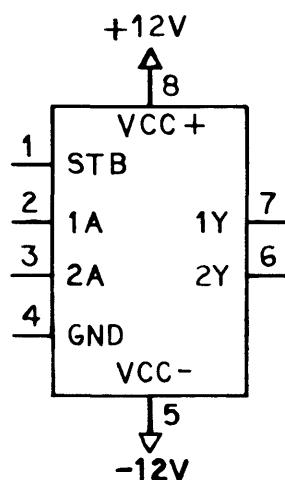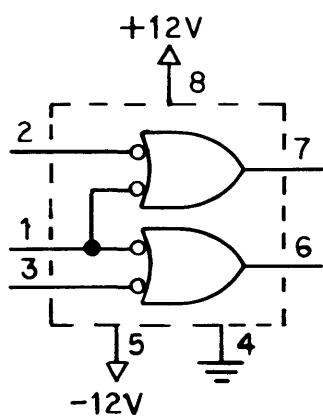
This line driver is commonly used to interface data terminal equipment to data communication equipment utilizing the EIA Standard RS-232-C. Input is TTL/DTL compatible, and output is ±12V.

Logic Symbol

Truth Table

INPUTS		OUTPUT
STB	A	Y
L	X	+12
H	L	+12
H	H	-12
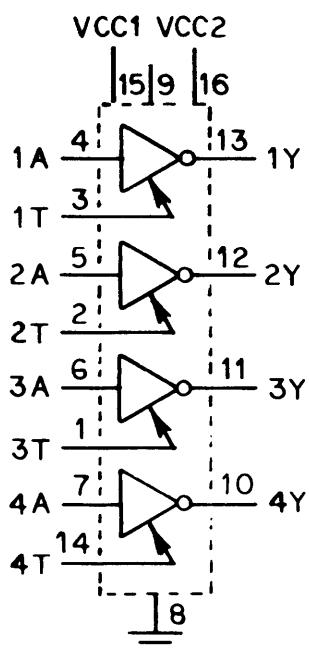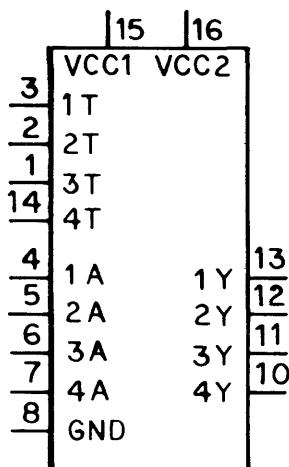
L = 0V
H = +5V
X = Irrelevant

Alternate Symbols

Loading:
     Inputs   1 Unit Load
     Strobe   2 Unit Loads

This receiver satisfies the requirements of the interface between data communication equipment and data terminal equipment as defined by EIA Standard RS-232-C. Input is from +25V to -25V, and output is either 0V or +5V. For normal operation, the threshold control terminal is connected to VCC1. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold levels. In this mode of operation, if the input voltage goes to zero (or open-circuit), the output will remain either low (0V) or high (+5V) as determined by the previous input. For fail-safe operation, the threshold terminal is left floating. This reduces the hysteresis loop, causing the negative-going threshold to be above 0V. The positive-going threshold is unchanged. In this mode, if the input voltage goes to 0V or is open-circuited, the output goes high (+5V) regardless of the previous input condition. VCC can be either +5V or +12V. Pin 9 should not be connected externally.
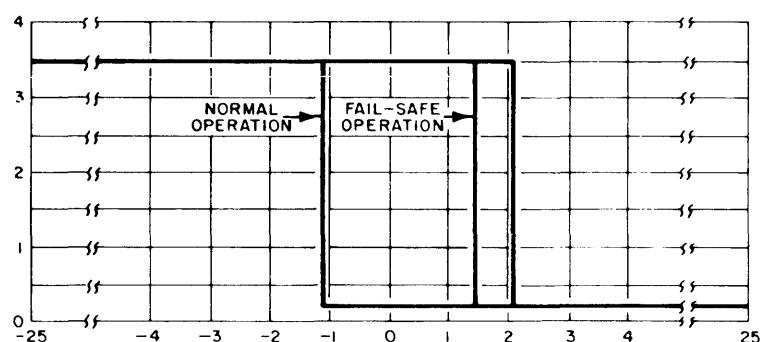
Logic Symbol

A = input
Y = output
T = threshold control
VCC1 = +5V
VCC2 = +12V

Alternate Symbol

Truth Table
(each receiver)
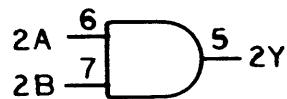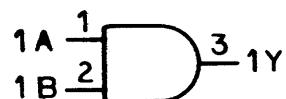
INPUT A	OUTPUT Y
-12	H (+5)
+12	L (0)

Waveforms

Loading:
  Outputs   10 Unit Loads

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Logic Symbol

1A — 1 —⌐ 3 —1Y
1B — 2 —

2A — 6 —⌐ 5 —2Y
2B — 7 —

Truth Table
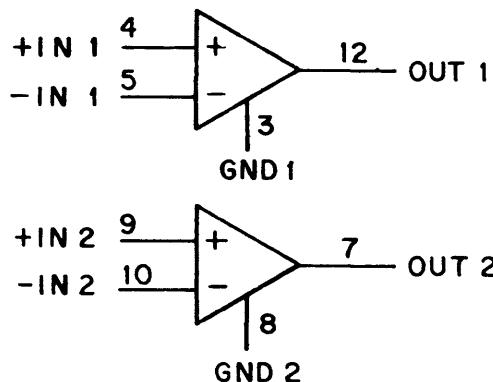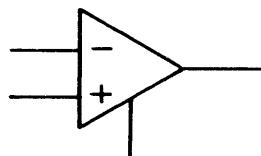
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

VCC-8, GND-4

Loading:

Input   1 Unit Load
Output   300 ma

This device can operate on voltage supplies up to ±15V, but can also operate off of a single +5V supply, depending upon the application. Note the non-standard voltage connections.

Logic Symbol   Alternate Symbol

+IN 1 — 4 — +
−IN 1 — 5 — − — 12 — OUT 1
     3
   GND 1

+IN 2 — 9 — +
−IN 2 — 10 — − — 7 — OUT 2
     8
   GND 2

V+, pin 11
V- , pin 6

3-Terminal Negative Voltage Regulator, 5 Volt   Part No. 42155-05   Type LM320H-5
3-Terminal Negative Voltage Regulator, 12 Volt   Part No. 42155-12   Type LM320H-12
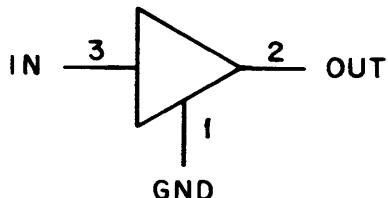
     This series of negative regulators provides precision regulation of output currents up to .5A, while also providing current limiting and thermal overload protection.
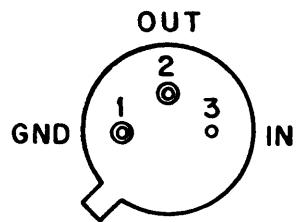
Logic Symbol

Pinout
(Bottom View)

Maximum Voltages

	-05	-12
IN	-7 to -25	-14 to -35
OUT	-4.8 to -5.2	-11.6 to -12.4

3-Terminal Positive Voltage Regulator, 12-Volt   Part No. 42154-12   Type LM341P-12
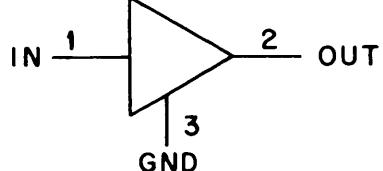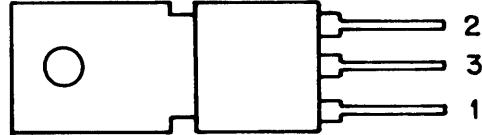
     This series of positive regulators provides precision regulation of output currents up to .5A, while also providing current limiting and thermal overload protection.

Logic Symbol
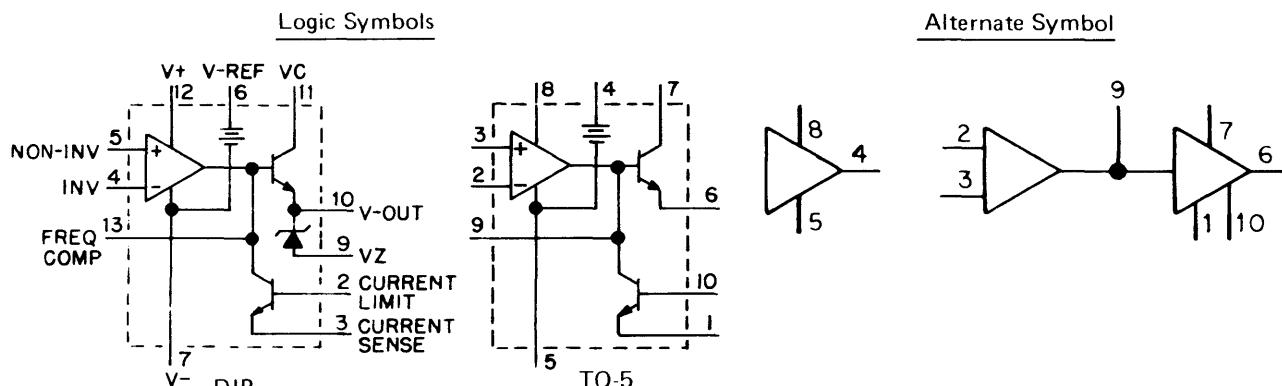
Pinout
(Top View)
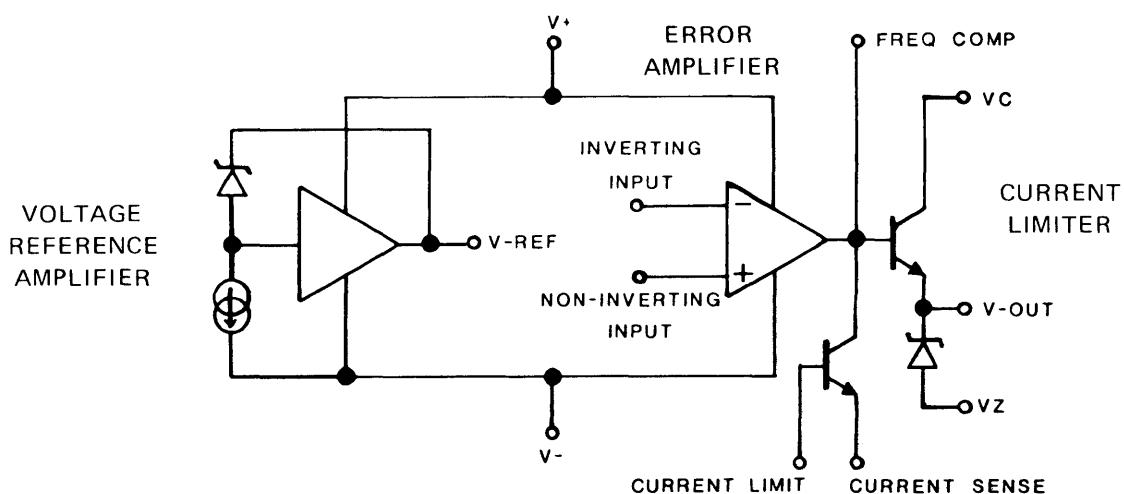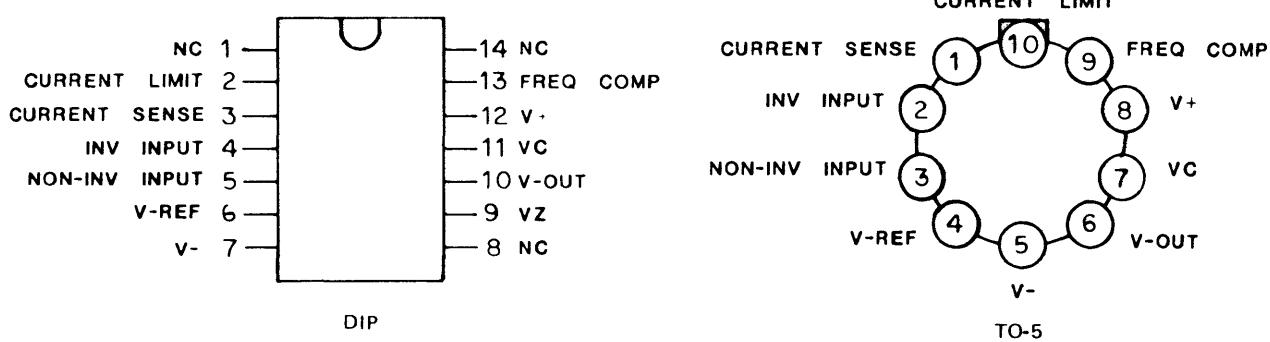
Input (1) = +14.8 to +27V
Output (2) = +11.4 to +12.6V

This device is used primarily in series regulator applications. It can supply output current up to 150 mA, but larger currents can be controlled by using the output to drive external transistors. It features extremely low standby current drain, provision for either linear or foldback current limiting, up to 40V maximum input voltage, and an output voltage range of 2V to 37V. It contains a 7V reference source, which can be utilized through suitable external resistors to provide any desired output voltage. An external reference can also be used, if desired. The Vz output is not provided in the TO-5 package: if required, a 6.2V zener diode should be connected in series with V-OUT.
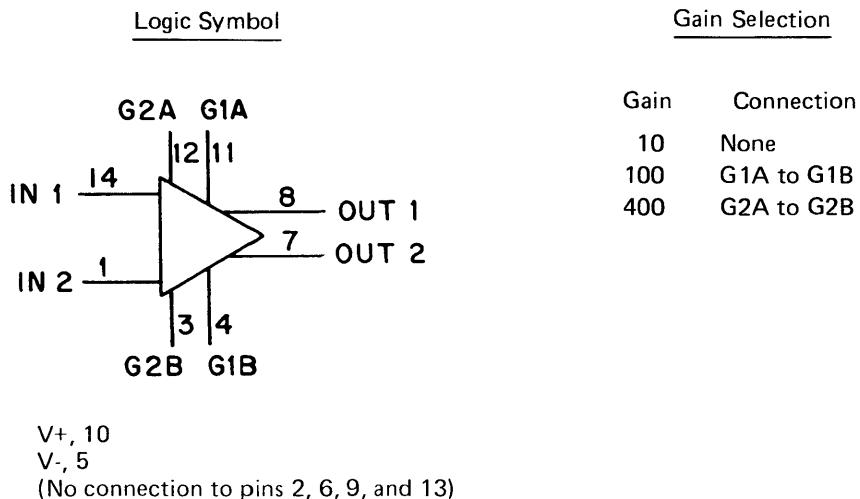
Logic Symbols   Alternate Symbol
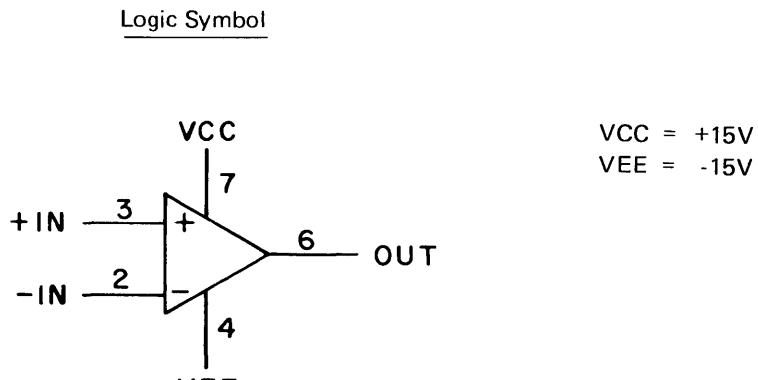
Logic Diagram

Pinouts
(Top Views)

Differential Video Amplifier   Part No. 10124   Type LM733C

This differential-input/differential-output amplifier provides selectable gains of 10, 100, and 400.

Logic Symbol   Gain Selection

G2A G1A   Gain   Connection

|12|11   10   None
IN 1 —14—   8 — OUT 1   100   G1A to G1B
                              7 — OUT 2   400   G2A to G2B
IN 2 —1—
        |3|4

G2B G1B

V+, 10
V-, 5
(No connection to pins 2, 6, 9, and 13)

OP Amp, High Slew Rate   Part No. 10167   Type MC1741SCP1

This device exhibits fast settling time, a high slew rate (10V/microsecond min.), low power consumption, and short-circuit protection. It is housed in an 8-pin DIP.

Logic Symbol

VCC

7
+IN —3— +
                    6 — OUT
−IN —2— −

4

VEE   VCC = +15V
                                        VEE = -15V
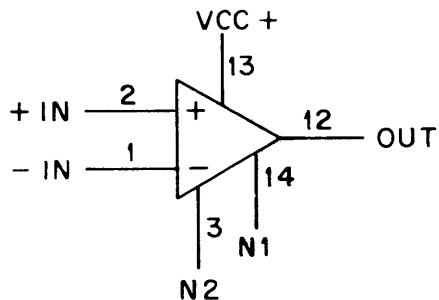
Pin 1 = Offset null
Pin 8 No connection

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Dual Op Amp, General Purpose   Part No. 10165   Type 72747
Dual Op Amp, Selected   Part No. 13072   Type 72747

Logic Symbol

VCC +
              13
+ IN ──2── + ──────12── OUT
− IN ──1── −   14
          3 N1
        N 2

              9
       6 ── +   ──10
       7 ── − 8
          5

VCC-4, No Connection -11
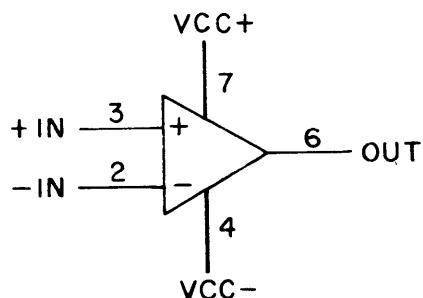
Op Amp, General Purpose   Part No. 10166   Type 72748

This single op amp is housed in an 8-pin DIP.
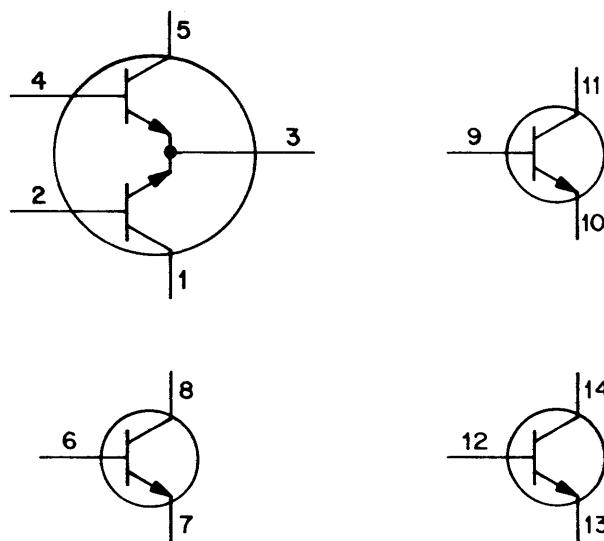
Logic Symbol

VCC+
                    7
Pin 1 = Offset null/Comp   + IN ──3── + ────6── OUT
Pin 5 = Offset null (N2)   − IN ──2── −
Pin 8 = Comp   4
                            VCC −

This device consists of five general-purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

Logic Symbol

(083-040)

Quad Field Effect Transistor (FET)   Part No. 10190   Type 8041
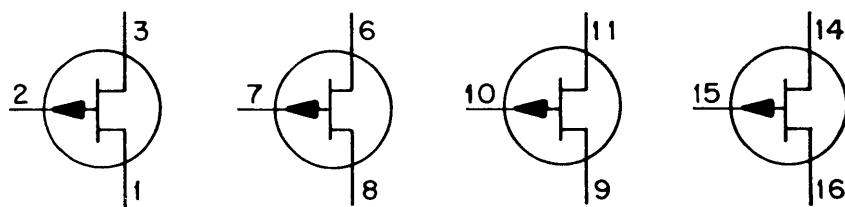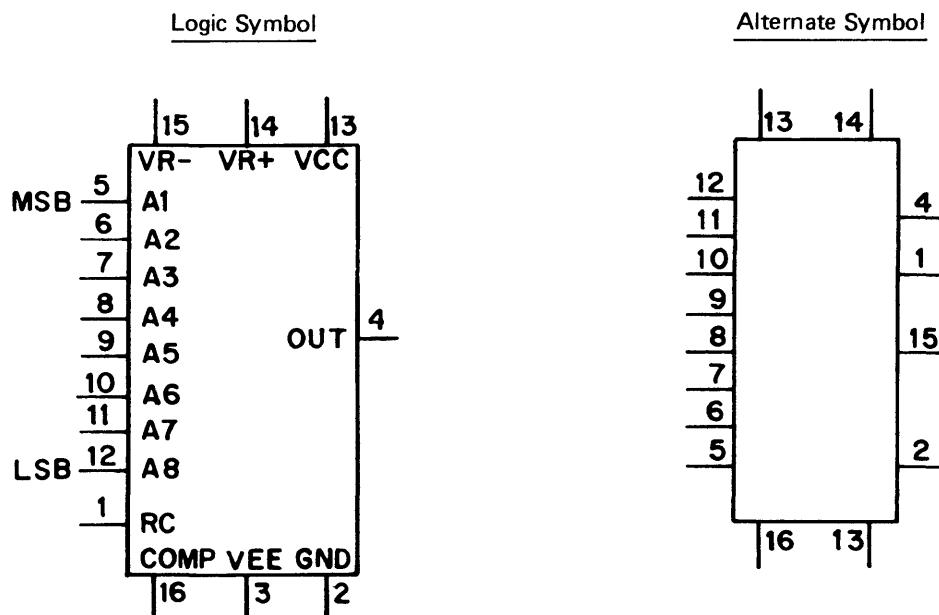
This IC contains four independent p-channel FETs.

Logic Symbol

This eight-bit multiplying D-to-A converter provides a current output which is the product of a digital word (applied to the A1-A8 inputs) and an analog reference voltage (applied to the VR+ and VR- inputs). Digital inputs are TTL and CMOS compatible. Output voltage swing is +0.5V to -0.6V with the Range Control (pin 1) grounded; leaving pin 1 open enables the negative voltage swing to reach -5V when maximum power supply voltages are applied. Frequency compensation capacitors are connected to pin 16. Note the non-standard VCC and GND connections.

Logic Symbol   Alternate Symbol

NOTE: VCC-13, GND-2

VCC = +5V
VEE = -5V to -15V (current source)
VR- = -15V (max.)
VR+ = +5V (max.)
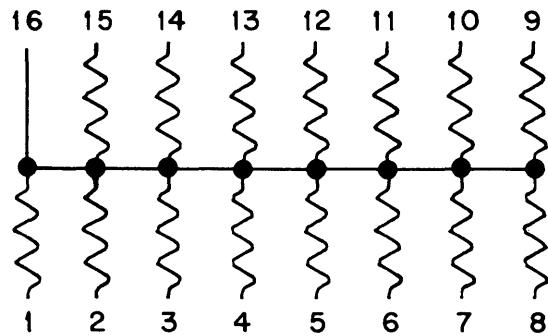
Loading:

Inputs (digital)   1 Unit Load
Output   2.0 ma.

```
┌─────────────────────────────────────────┐
│ Resistor Network, 1K x 15    Part No. 10239-01 │
│                                           │
│                  Pinout                   │
│                                           │
│   16   15   14   13   12   11   10   9    │
│                                           │
│    1    2    3    4    5    6    7    8    │
└─────────────────────────────────────────┘
```

```
┌─────────────────────────────────────────┐
│ Resistor Network, 1K x 13     Part No. 10761 │
│                                           │
│                  Pinout                   │
│                                           │
│   14   13   12   11   10    9    8        │
│                                           │
│    1    2    3    4    5    6    7        │
└─────────────────────────────────────────┘
```

```
┌─────────────────────────────────────────┐
│ Resistor Network, Quad 10K x 2   Part No. 13044 │
│                                           │
│                  Pinout                   │
│                                           │
│   1 ─⋁⋁⋁─ 2      7 ─⋁⋁⋁─ 5                │
│         └─⋁⋁⋁─ 3        └─⋁⋁⋁─ 6          │
│                                           │
│   8 ─⋁⋁⋁─ 9     14 ─⋁⋁⋁─ 12               │
│         └─⋁⋁⋁─ 10       └─⋁⋁⋁─ 13         │
│                                           │
│        (Pins 4 and 11, no connection)     │
└─────────────────────────────────────────┘
```

4.6 ASCII CODE CHART

Appendix A of the Product Description manual, the ASCII code chart, is reproduced in Figure 4-2 for convenience.

4.7 SCHEMATICS AND LOGIC DRAWINGS

Figure 4-3 explains the meaning of the various notations contained on the logic drawings and schematics. For more information on component locations and connector pin numbers, etc., see Section 3.

Table 4-2 lists the schematics and logic drawings contained in the remainder of this manual.

Table 4-2. Schematics and Logic Drawings

Drawing Number	Description
23702-99	HPRO1 Board
23704-99	HPRO2 Board
40644-03	8080 INTERFACE Board
40510-XX	LOGIC-2 Board
40520-04	SERVO Board
40515-03	XDCR Brd
40525-06	CAR PWR AMP Board
40530-08	PW PWR AMP Board
23940	PW Assy. HCURL Board
23897	Keyboard Assy. (Hall-effect)
400512-01	Keyboard Assy. (Cortron)
23708	Control Panel Assy., HPCPN
40614	Mother Board
46080-01	Mother Board
26021	Power Supply (Boschert)
400062-XX	Power Supply (LHR)
24471	Printer Cables
23859	Power Distribution
23732	Signal Cables
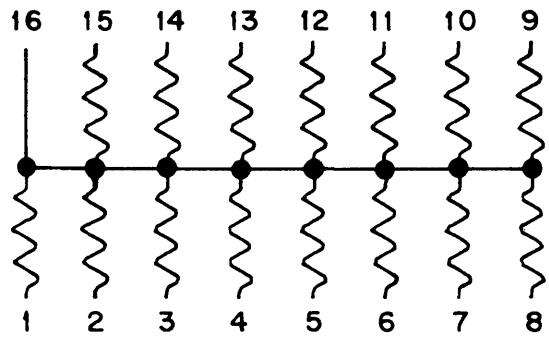
Diablo Systems can provide schematics for older units and specially-built units. Contact your local Diablo representative, and provide circuit board part numbers and revision levels for fastest service.
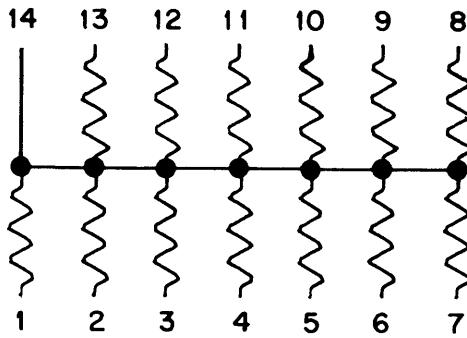
Resistor Network, 1K x 15   Part No. 10239-01
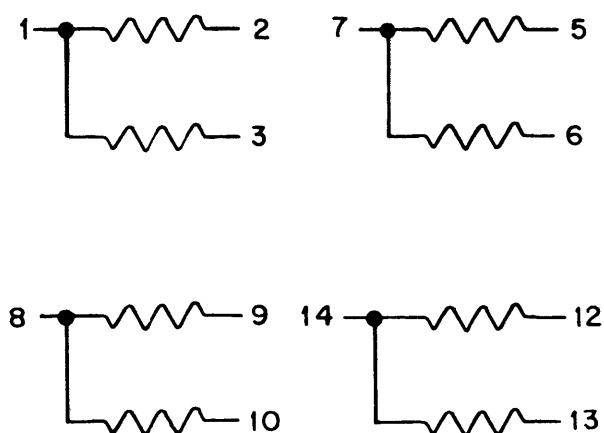
Pinout

Resistor Network, 1K x 13   Part No. 10761

Pinout

Resistor Network, Quad 10K x 2   Part No. 13044

Pinout

(Pins 4 and 11, no connection)

4.6 ASCII CODE CHART

Appendix A of the Product Description manual, the ASCII code chart, is reproduced in Figure 4-2 for convenience.

4.7 SCHEMATICS AND LOGIC DRAWINGS

Figure 4-3 explains the meaning of the various notations contained on the logic drawings and schematics. For more information on component locations and connector pin numbers, etc., see Section 3.

Table 4-2 lists the schematics and logic drawings contained in the remainder of this manual.

Table 4-2. Schematics and Logic Drawings

Drawing Number	Description
23702	HPR01 Board
23704	HPR02 Board
40644-XX	8080 INTERFACE Board
40644-03	8080 INTERFACE Board
40510 Rev. L	LOGIC-2 Board
40510 Rev. U	LOGIC-2 Board
40520-03	SERVO Board
40520-04	SERVO Board
40515	XDCR Board
40525-XX	CAR PWR AMP Board
40525-05	CAR PWR AMP Board
40530-XX	PW PWR AMP Board
40530-07	PW PWR AMP Board
40614	Mother Board
23708	Control Panel Assy., HPCPN
23710	Control Panel Assy., HPCPL
23897	Keyboard Assy.
24471	Printer Cables
26021	Power Supply
26021	Power Supply Assy.
23836-01	Power Supply, 115v.
23836-01	Power Supply, 115v., Assy.
23836-02	Power Supply, 220v.
23836-02	Power Supply, 220v., Assy.
23859	Power Distribution
23732	Signal Cables

Figure 4-3. Logic Drawing Notation

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
   +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8;
   +5V TO PIN 24 OF 24-PIN IC, GND TO PIN 12.
5. INSTALL JUMPER A2 IF ASCII KEYBOARD IS TO BE USED.
6. WITH NO JUMPER POSITION ENCODED KEYBOARD IS ASSUMED.
   LOCATION E62 IS FOR PROGRAM EROM OR ROM, FOR P/N
   REFER TO INDIVIDUAL PARTS LIST.
7. STRAP AT E3 PROVIDES AN OPTIONAL DISCONNECTION BETWEEN
   PROTECTIVE GROUND AND SIGNAL GROUND PER RS-232-C.
8. LOCATION D62 IS FOR FEATURE LOOK-UP EROM.
   FOR PART NUMBER REFER TO INDIVIDUAL PARTS LIST.
9. INSTALL STRAP A6 BETWEEN A5 & A7 TO PROVIDE LOCAL ONLY
   MODE.
10. INSTALL PLUG F23 BETWEEN F22 & F24 TO PROVIDE
    1200 BAUD ONLY.

+ ADDR 4   SH3 - H16
+ ADDR 3   SH3 - G16
+ ADDR 2   SH3 - G16
+ ADDR 1   SH3 - H16
+ ADDR Ø   SH3 - H16

SH3 - L3   + USART INTERRUPT
SH2 - E3   + PAR DATA INTERRUPT

+ DA Ø   P1 (9)   SH2-L16 , SH3-L16
+ DA 1   (12)
+ DA 2   (11)   SH2-K16 , SH3-L16
          SH2-K16 , SH3-L16
+ DA 3   (13)   SH2-K16 , SH3-L16
+ DA 4   (8)   SH2-K16 , SH3-L16
+ DA 5   (10)   SH2-K16 , SH3-L16
+ DA 6   (14)   SH2-K16 , SH3-K16
+ DA 7   (16)   SH2-K16 , SH3-K16

J2 (4)   - RESET

SH2 - E3   PULL UP 1

LM320H 5.0   A59
LM320H-12   A58
LM341P-12   A41

P1 (23)(24)
P1 (41)(42)   (11) P2
P1 (5)(6)   (8) J3
(53)(54)
J3 (15)
P2 (1)(3)
P1 (1)(2)
(55)(56)

P2 (2)(4)
(16) J3
(1) J1
(6) J1
(8) J2

GND CNCT   F4 F3 F2

SPARES: E22 A9-3

- READ   P1 (37)   SH3 - H16
- WRITE   (39)   SH2 - E16 , SH3 - H16
+ CLEAR   SH2 - F16 , SH3 - K16
+ Ø2T   SH2 - J16 , SH3 - K16
+ SYSTEM CLOCK   (52)   SH3 - B16

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY HP RO1

1610/1620

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY HPR01

MODEL 1610/1620

23702-99

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PRODUCT NO. 23702-99

PR DUCT NO. 23702-99   DEVELOPMENT REV. D8

SH1 - J7   + DA Ø
SH1 - J7   + DA 1
SH1 - J7   + DA 2
SH1 - G7   + DA 3
SH1 - G7   + DA 4
SH1 - G7   + DA 5
SH1 - F7   + DA 6
SH1 - F7   + DA 7
SH1 - B7   + CLEAR
SH1 - B7   + Ø 2T

+5V
26
VCC
27 DØ
28 D1
1   D2
2   D3
4   D4
5   D5   USART
6   D6
7   D7   D45
21 RST   8251
20 CLK
9   TxC
25 RxC
3   RD
10 WR
12 C/D
22 DSR
17 CTS
11 CS
GND
4

TxD   19
TxE   18
15
Tx RDY 14
Rx RDY 13
DTR   24
RTS   23
SYNDET 16

+ USART INTERRUPT   SH1 - J17
- DTR   SH2 - C16

+12V
B43 7515ØP
+5V
A15
1K
- XMIT DATA   J1 (5)
+ REQUEST TO SEND (4)
-12V

-5V
15 9 16
VCC1 R1 VCC2
3   1T   RCVR
2T
2T
4T   E7
1A   1Y 13
2A   2Y 12
3A   3Y 11
4A   4Y 10
GND
75154

J1
(7) - DATA RECEIVED
(8) + DATA SET READY
(9) + CLEAR TO SEND
(10) + CARRIER DETECT
     - 2x COMM CLK

SH2 - J3   PULL UP 1
SH2 - E3   - READ
SH1 - C7   - WRITE
SH1 - B7   + ADDR 4
SH1 - L7   - FKY 3

P2 (10)

D34
7432

P 5
D-FF
A8
7474
CLK
Q

A50 4
7404

+ READ   SH2 - E16

SH1 - L7   + ADDR Ø
SH1 - L7   + ADDR 1
SH1 - L7   + ADDR 2
SH1 - L7   + ADDR 3
SH2 - E3   + PAR DATA INTERRUPT

1 AØ   Ø0 15
2 A1   01 14
3 A2   DCDR 02 13
         03 12
4 E1   E36   04 11
5 E2   8205 05 10
6 E3   06 9
               07 7

A23 +5V
1K

- PORT Ø   SH2 - E16
- PORT 1   SH2 - J16

- PORT 5   P1 (50)
- PORT 6   (48)
- PORT 7   (46)

-PRINTER SELECT (18)

P2
(8) - FKY 2
(7) - FKY 1
(5) - FKY 4
(6) - FKY 5

KEYBOARD MODE +5V
A3 A2 A1
LOCAL
A7 A6 A5

+5V
14   14
A9   E22
1K   1K

J3
(3) - FUN SWITCH 4
(1) - FUN SWITCH 5
(4) - FUN SWITCH 6

(11) - FUN SWITCH 7
(13) - FUN SWITCH 8
(16) - FUN SWITCH 9
(12) - FUN SWITCH 10
(10) - FUN SWITCH 11

DI1 I/O DO1 4
DI2 PORT DO2 6
DI3   DO3 8
DI4   DO4 10
DI5 B5   DO5 15
DI6   DO6 17
DI7   DO7 19
DI8   DO8 21
DS1
DS2 8212
MD   INT 23
STB
C 14

J2
(14) - FUN SWITCH 13
(1) - FUN SWITCH 14
(5) - FUN SWITCH 15
(6) - FUN SWITCH 16
(7) - FUN SWITCH 17
(3) - FUN SWITCH 18
(2) - FUN SWITCH 19
(15) - FUN SWITCH 20

SH1 - B7   + SYSTEM CLOCK
SH2 - F3   - CLEAR

1200 BAUD
F23
F24   F22

DI1 I/O DO1 4
DI2 PORT DO2 6
DI3   DO3 8
DI4   DO4 10
DI5 D5   DO5 15
DI6   DO6 17
DI7   DO7 19
DI8   DO8 21
DS1
DS2 8212
MD   INT 23
STB
C 14

DI1 I/O DO1 4
DI2 PORT DO2 6
DI3   DO3 8
DI4   DO4 10
DI5 D20 DO5 15
DI6   DO6 17
DI7   DO7 19
DI8   DO8 21
DS1
DS2 8212
MD   INT 23
STB
C 14

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY HP R01

MODEL 1610/1620

SYSTEM LOGIC NO.

PRODUCT NO. 23702-99

E 7487 7-23-76
D 7447
C 7-24
B 7413 23 MAR 76
A 7367 2 FEB 76

12-11-75

SCHEMATIC INCLUDES SHEETS 1 THRU 3

SHEET 3 TOTAL SHEETS 11 SIZE D PRODUCT NO. 23702-99 REV E

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23702 HPR01 Processor Board

Rev. A	ECO	7367	As released.
B		7413	(1) Add 1K resistor (E22-7) from +INT (F37-14) to +5V.
			(2) Add .1 microfarad capacitor at B39 to improve noise immunity.
			(3) Change ROMs 23734 and 23735 to Rev. B; change ROM 23738 to Rev. A, to eliminate ribbon lift problem.
C		7424	Connect +12V to J3-8 to drive audible alarm.
D		7447	Allow use of plastic IC packages instead of ceramic for 2111, 8205, 8212, and 8224.
E		7487	Add pullups to DATA 0-7 lines to improve noise immunity. Replace 1200-baud jumper with socket for shorting plug.
F		7693	{ Changes some metal/ceramic IC's to plastic. (Types: 8224, 8228, 8205,
G		7816	{ 8251, 8212, 8080A, and 25LS138). No schematic changes.
H		7975	Hardware change only. No schematic changes.

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE $\frac{1}{4}$ WATT, $\pm 5\%$.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
   +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8;
   +5V TO PIN 24 OF 24-PIN IC, GND TO PIN 12.
5. INSTALL JUMPER E4 IF ASCII KEYBOARD IS TO BE USED.
   WITH NO JUMPER, POSITION ENCODED KEYBOARD IS ASSUMED.
6. STRAP AT A4 PROVIDES AN OPTIONAL DISCONNECTION BETWEEN
   PROTECTIVE GROUND AND SIGNAL GROUND PER RS-232-C.
7. LOCATION A22 IS FOR PROGRAM MASKED ROM.
   FOR PART NUMBER REFER TO INDIVIDUAL PARTS LIST.
8. INSTALL STRAP F7 BETWEEN F6 AND F8 TO PROVIDE
   LOCAL ONLY MODE.
9. INSTALL PLUG B2 BETWEEN B1 AND B3 TO PROVIDE
   1200 BAUD ONLY.

+ ADDR 4 → SH3-H16
+ ADDR 3 → SH3-G16
+ ADDR 2 → SH3-G16
+ ADDR 1 → SH3-H16
+ ADDR 0 → SH3-H16

SH3-L3 → + USART INTERRUPT
SH2-D3 → + PAR DATA INTERRUPT

A37 8080A CPU

J2 → − RESET

SH2-D3 → PULL UP 1

A60 8228 BUS DVR

+ DA 0 → SH2-K16, SH3-L16
+ DA 1 → SH2-K16, SH3-L16
+ DA 2 → SH2-K16, SH3-L16
+ DA 3 → SH2-K16, SH3-L16
+ DA 4 → SH2-K16, SH3-L16
+ DA 5 → SH2-J16, SH3-L16
+ DA 6 → SH2-J16, SH3-K16
+ DA 7 → SH2-J16, SH3-K16

− READ (37)
− WRITE (39) → SH3-H16
→ SH2-E16, SH3-H16
+ CLEAR → SH2-E16, SH3-K16
+ φ2T → SH2-J16
+ SYSTEM CLOCK (52) → SH3-B16

SPARES:

SCHEMATIC DIAGRAM
Diablo Systems Incorporated

PW ASSY, HPRO2
1610/1620

23704-99 REV C

4-75

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, HP R02

1610/1620

23704-99

+5V
26
VCC

SH1 - G6   + DA Ø   27 DØ
SH1 - G6   + DA 1   28 D1   USART
SH1 - G6   + DA 2   1   DØ
SH1 - F6   + DA 3   2   D3   D21
SH1 - F6   + DA 4   5   D4
SH1 - E6   + DA 5   6   D5   8251   + USART INTERRUPT   SH1 - H17
SH1 - E6   + DA 6   7   D6   - DTR   SH2 - E16
SH1 - E6   + DA 7   8   D7
SH1 - E6   + CLEAR   21 RST
SH1 - C6   + Ø2T   20 CLK
                      29 TxC
                      3   RxC
                      13 RxD   TxD 19   +12V
                      10 RD   TxE 18   D65 7515ØP
- DATA RECEIVED (7) 12 WR   TxRDY 15   3   16   - XMIT DATA   J1 (5)
+ DATA SET READY (8) 22 C/D   RxRDY 14   +5V
+ CLEAR TO SEND (9) 17 DSR   DTR 24   E62
+ CARRIER DETECT (10)   CTS   RTS 23   1K   1   7   + REQUEST TO SEND J1 (4)
                      11 CS   SYNDET 16
J1   GND   14   -12V
         + 2x COMM CLK
SH2 - J3   PULL UP 1   + READ   SH2 - E16
SH2 - D3 - READ
SH1 - D6 - WRITE
SH1 - C6 + ADDR 4
SH1 - L6 - FKY 3   P2 (10)   F10 +5V
                                           1K

SH1 - K6 + ADDR Ø   AØ DCDR OØ 15   - PORT Ø   SH2 - E16
SH1 - L6 + ADDR 1   A1   O1 14   - PORT 1   SH2 - J16
SH1 - L6 + ADDR 2   A2   O2 13
SH1 - L6 + ADDR 3   E50 O3 12
SH1 - L6 + PAR DATA INTERRUPT   O4 11
SH2 - D3   E66 8205 O5 10   - PORT 5   P1 (50)
                           1K   O6 9
                                     O7 7   - PORT 6   (48)

- FKY 2 (8)   ASCII KYBD +5V   +5V   - PORT 7   (46)
- FKY 1 (7)   E5 E4 E3   - PRINTER SELECT (18)
- FKY 4 (5)   LOCAL   E7   B37
- FKY 5 (6)   F6 F8   1K   1K
P2

- FUN SWITCH 4 (3)   DI1 I/O DO1
J3 - FUN SWITCH 5 (1)   DI2 PORT DO2
- FUN SWITCH 6 (4)   DI3   DO3
                          DI4   DO4
- FUN SWITCH 7 (11)   DI5 D5 DO5
- FUN SWITCH 8 (13)   DI6   DO6
- FUN SWITCH 9 (16)   DI7   DO7
- FUN SWITCH 10 (12)   DI8   DO8
- FUN SWITCH 11 (10)   DS1
                          DS2 8212
                          MD INT
                          STB C 14

- FUN SWITCH 13 (14)   1200 BAUD   DI1 I/O DO1
J2 - FUN SWITCH 14 (1)   B2   DI2 PORT DO2
- FUN SWITCH 15 (5)   DI3   DO3
- FUN SWITCH 16 (6)   B1   B3   DI4   DO4
- FUN SWITCH 17 (7)   DI5 B5 DO5
- FUN SWITCH 18 (3)   DI6   DO6
- FUN SWITCH 19 (2)   DI7   DO7
- FUN SWITCH 20 (15)   DI8   DO8
                                     DS1
                                     DS2 8212
                                     MD INT
                                     STB C 14

SH1 - B6 + SYSTEM CLOCK   DI1 I/O DO1
SH2 - E3 - CLEAR   DI2 PORT DO2
                            DI3   DO3
                            DI4   DO4
                            DI5 B21 DO5
                            DI6   DO6
                            DI7   DO7
                            DI8   DO8
                            DS1
                            DS2 8212
                            MD INT
                            STB C 14

VCC1 R1 VCC2
1T   RCVR
2T
3T
4T
1A B6 1Y
2A 75154 2Y
3A   3Y
4A   4Y
GND

E60
7432   D-FF
          E8
          7474

E49
7404

SCHEMATIC DIAGRAM
Diablo Systems Incorporated
PW ASSY, HP RO2
1610/1620

23704 HPR02 Processor Board

Rev. A	ECO	7434	As released.
B		7437	Connect +12V to J3-8 to drive audible alarm.
C		7487	Add pullups to DATA 0-7 lines to improve noise immunity. Replace 1200-baud jumper with socket for shorting plug.
D		7605	New artwork. No schematic changes.
E		7676	Hardware change only. No schematic changes.
F		7683	Changed some metal/ceramic IC's to plastic. (Types: 8224, 8228, 8205,
G		7816	8251, 8212, 8080A, and 25LS138). No schematic changes.
H		7975	Hardware change only. No schematic changes.
J		A4015	

Additional solid state components used:

IC   C8316A   A22

8080 INTERFACE
40644-03
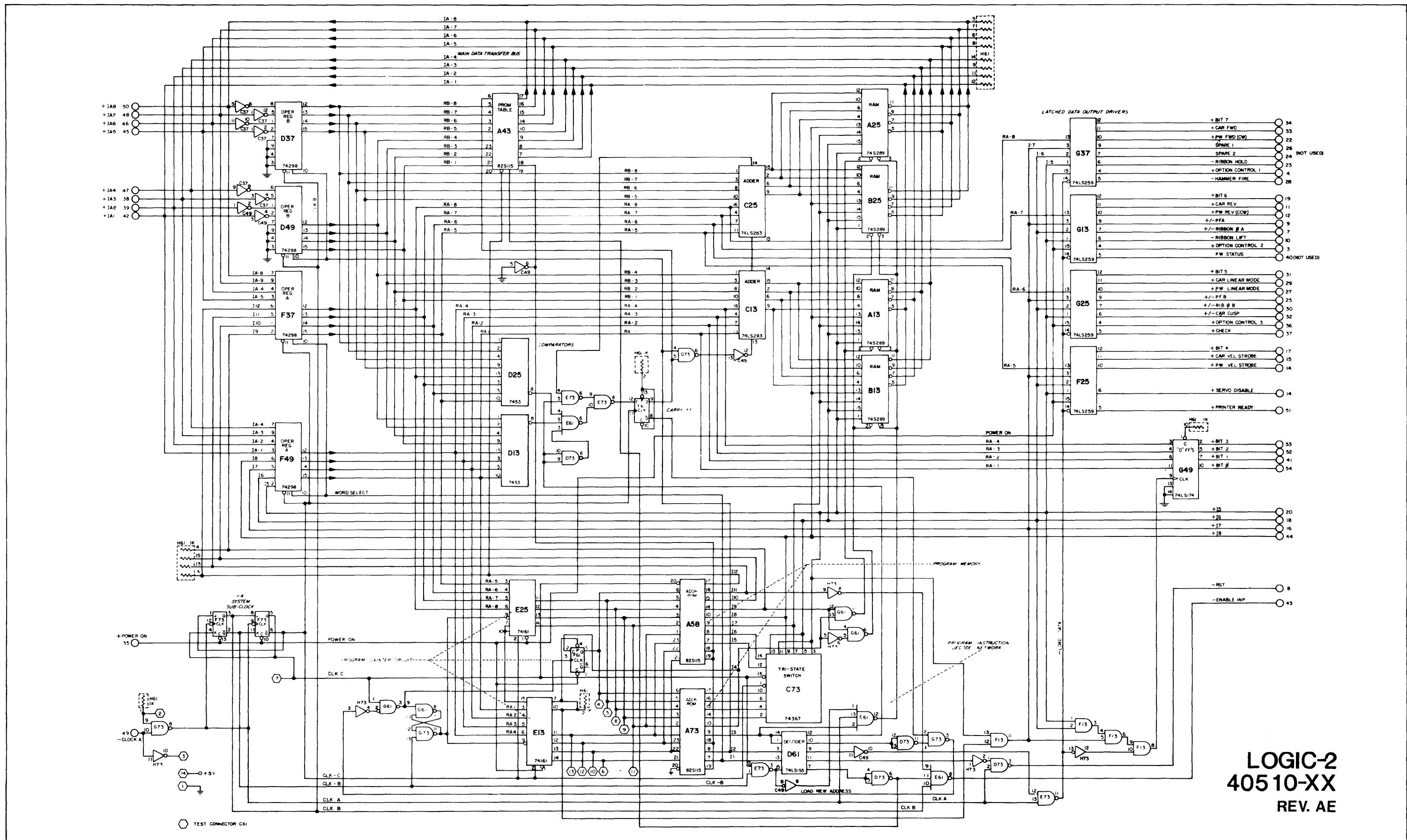
REV. E

40644-03 8080 INTERFACE Board

Rev. D	ECO 1120	Circuit board revised: all IC locations changed; 74174 eliminated; 7404, 7414, and 7432s added to CAR & PW inputs for noise immunity; CAR & PW CNTR CTRL circuits modified to allow printwheel to turn without loss of PW position in memory.
E	A3879	Documentation change only. No schematic changes.

LOGIC-2
40510-XX
REV. AE

MAIN DATA TRANSFER BUS

LATCHED DATA OUTPUT DRIVERS

+ BIT 7
+ CAR FWD
+ PW FWD (CW)
SPARE 1
SPARE 2   (NOT USED)
- RIBBON HOLD
+ OPTION CONTROL 1
+ HAMMER FIRE

+ BIT 6
+ CAR REV
+ PW REV (CCW)
+/- PFA
+/- RIBBON Ø A
- RIBBON LIFT
+ OPTION CONTROL 2
PW STATUS   (NOT USED)

+ BIT 5
+ CAR LINEAR MODE
+ PW LINEAR MODE
+/- PFB
+/- RIB Ø B
+/- CAR CUSP
+ OPTION CONTROL 3
+ CHECK

+ BIT 4
+ CAR VEL STROBE
+ PW VEL STROBE

+ SERVO DISABLE
+ PRINTER READY

POWER ON

+ BIT 3
+ BIT 2
+ BIT 1
+ BIT Ø

+I5
+I6
+I7
+I8

- RST
- ENABLE INP

+IA8 50
+IA7 48
+IA6 46
+IA5 45

+IA4 47
+IA3 38
+IA2 39
+IA1 42

OPER REG B   D37
OPER REG B   D49
OPER REG   F37
OPER REG A   F49

PROM TABLE   A43

ADDER   C25
ADDER   C13

RAM   A25
RAM   B25
RAM   A13
RAM   B13

COMPARATORS
D25   7453
D13   7453

CARRY 11

SYSTEM SUB-CLOCK

PROGRAM MEMORY

PROGRAM COUNTER CIRCUIT

ADDR DRAM   E25   74161
ADDR ROM   A73   82S115
ADDR ROM   E13   74161

TRI-STATE SWITCH   C73   74367

DECODER   D61   74LS156

PROGRAM INSTRUCTION DECODE NETWORK

LOAD NEW ADDRESS

WORD SELECT

POWER ON

CLK C
CLK A
CLK B

- CLOCK A

+5V

TEST CONNECTOR C61

CLK C
CLK B
CLK A
CLK B

A58   82S115

G37   74LS259
G13   74LS259
G25   74LS259
F25   74LS259

G49   74LS174

4-81

REVISION HISTORY — #40510-XX LOGIC-2 BOARD

Rev. M   ECO #9988   Revise documentation and assembly to move ROM's for heat consideration; change to axial lead bypass capacitors; revise RESET logic; and improve fan out.

N   A1274   Revise PROM program to correct problem of failing to recognize PBV command.

P   A1247   (1)   Change circuit to enable Table ROM (A43-19) only when it is to be read (was previously enabled also when RAM was accessed); lengthen IC life.

    (2)   Add delay (via H73-12) to eliminate possible race condition on Bit 0 — Bit 3 output latches.

    (3)   Add delay (via C49-9) to increase RAM address hold time from $\approx$ 5 ns to $\approx$ 20 ns.

Q   A1444
R   A1523
S   A1501   ROM changes for other HyType II models; not applicable to HyTerm. No schematic changes.
T   A1578
U   A1622
V   A1841
W   A1879
X   A1945

Y   A1977   ROM change to lower maximum carriage/paper feed velocity slightly, to prevent possible missing of incr/decr pulse.
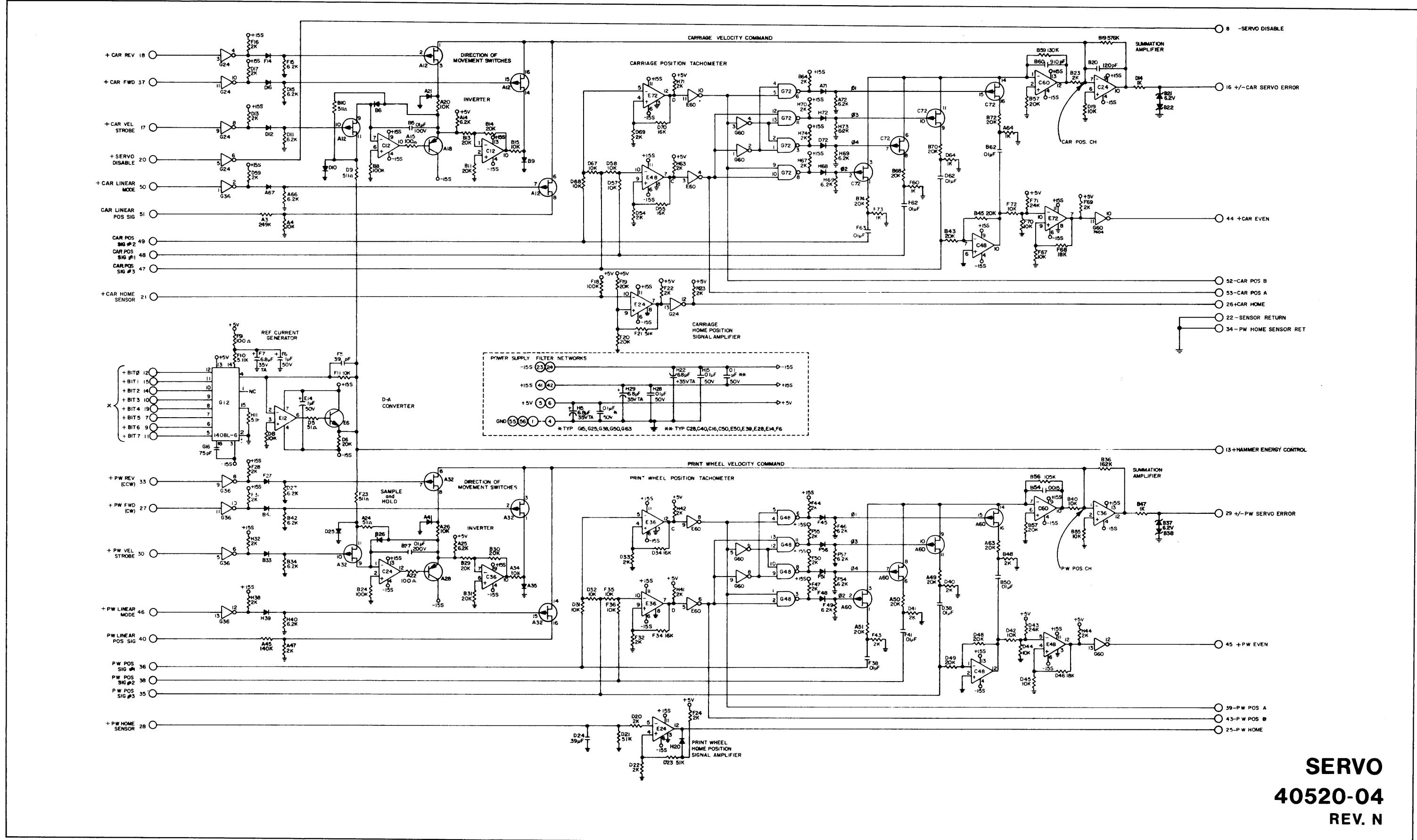
Z   A3093   Allow use of ceramic ROMs to improve reliability; ROM changes for other HyType II models. No schematic changes.

AA   A3250   ROM changes for other HyType II models. No schematic changes.

AB   A3289   Hardware change only. No schematic changes.

AC   A3508   ROM changes for other HyType II models. No schematic changes.
AD   A3917

AE   A3929   PROM changes for other HyType II models. No schematic changes.

SERVO
40520-04
REV. N

REVISION HISTORY # 40520-04 SERVO PCB ASSEMBLY

Rev. M   ECO#9923   New artwork, minor component changes; prevents possible motor burnout following component failure.

N   A1504   Remove assembly number from etch; this circuit also used for other assemblies. No schematic changes.

Additional Solid State Components used:
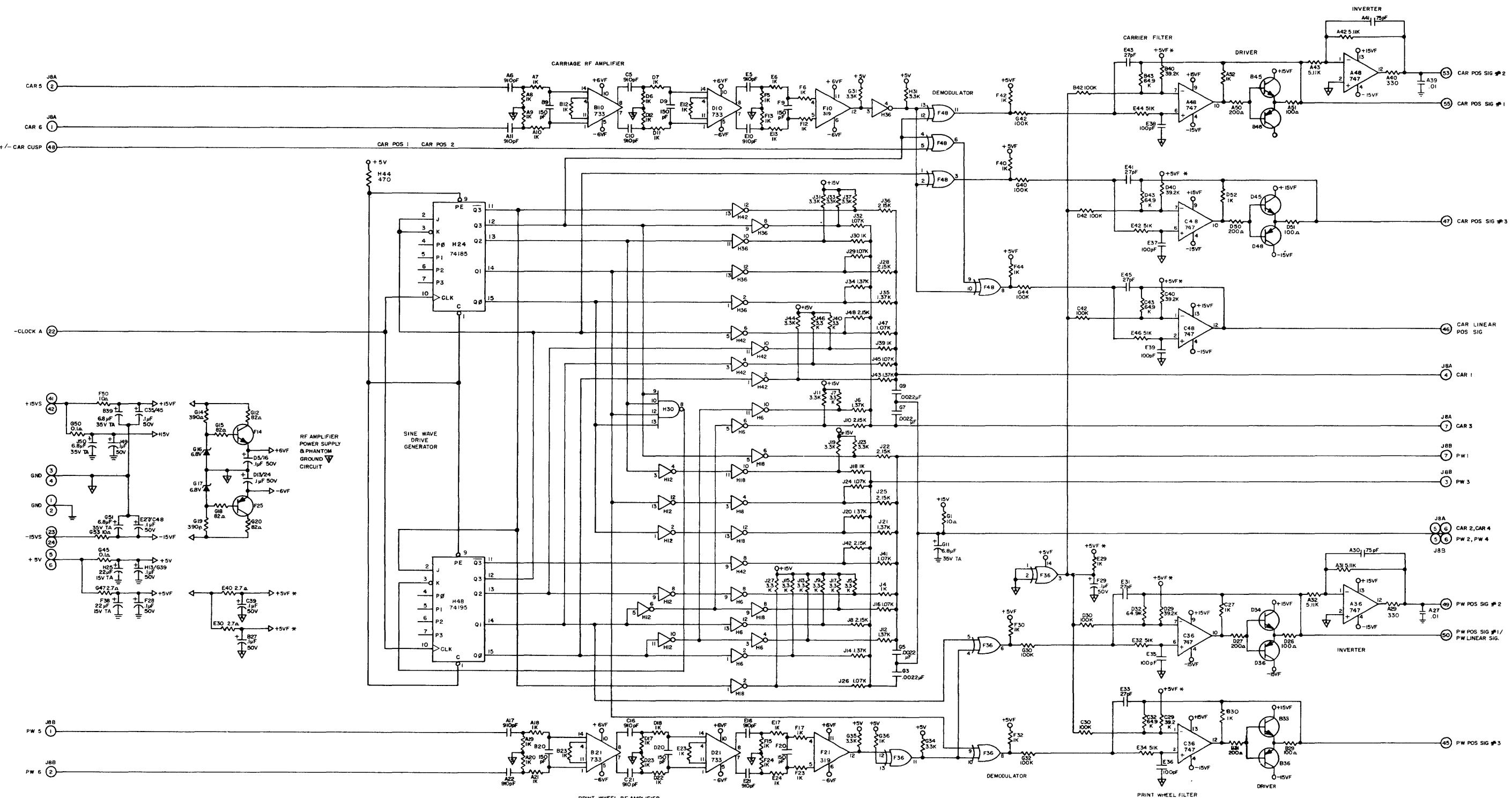
IC's	7404	G60, E60
	7406	G24, G36
	7426	G48, G72
	741S	E12
	747C	C12, C24, C36, C48
	8041	A12, A32, A60, C72
	319	E24, E36, E48, E72

OP, AMP
Low Offset   C60

Transistor	2N4401	E6
	PN3644	A18, A28

Zener Diode 6.2V
1N5234B   B21, B22, B37

Diode   1N4454   A21, A35, A41, A67, A71, B6, B9, B26, B33, B41, D10, D12, D16, D25, D72, F14, F27, F45, F48, F51, F56, H20, H39, H68, H72.

XDCR

40515-03

REV. A

4-85

REVISION HISTORY — # 40515-01 TRANSDUCER PCB ASSEMBLY

Rev. A	ECO#9742	B/M and Assembly as Released.
B	9830	Revise documentation and Assembly to change resistor type at G1 from film to composition. Cut "Key" pins on connectors J8A and B.
C	A1483	Change transistor at F25 from 2N5322L to 2N5322. Correct several schematic errors.

 # 40515-02

Rev. A	ECO#A1695	Add .01 μf capacitors from CAR POS SIG #2 (pin 53) and PW POS SIG #2 (pin 49) to GND. Change series resistors A40 and A29 (same circuits) to 330 ohms. To increase noise immunity of op amps; eliminate printwheel retry. Change -01 to -02; change revision level to Rev. A.
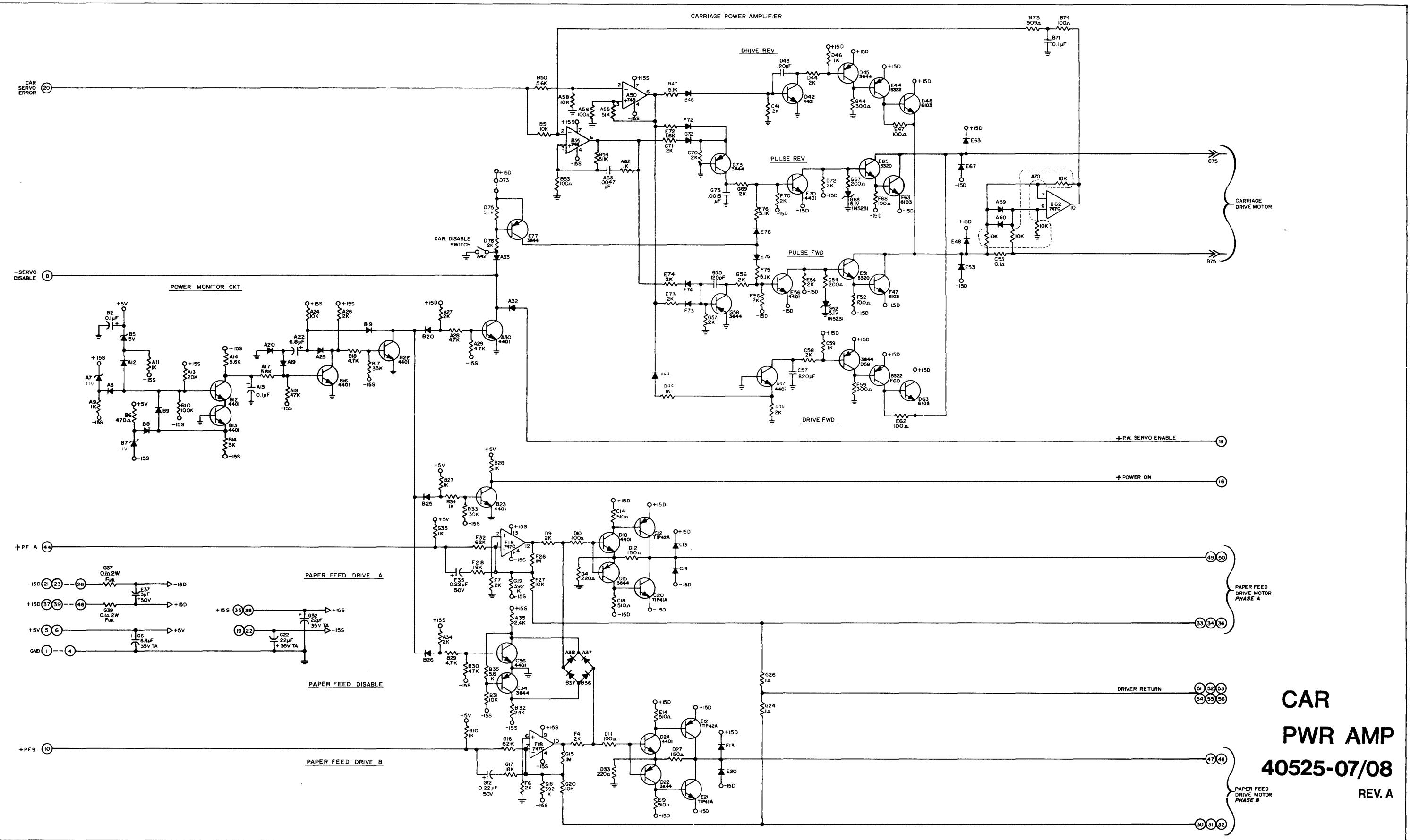
#40515-03

Rev. A	ECO#A1720	Change circuit board and artwork to accommodate changes incorporated in -02 (ECO#A1695). Change location of capacitor A28 to A27.

Additional Solid State Components Used:

IC's	7404	H12
	7406	H6, H18, H36, H42
	7420	H30
Transistor	2N3644	B36, B48, D36, D48
	2N4401	B33, B45, D34, D45
	2N4736A	G16, G17
	2N5320	F14
	2N53	F25

CARRIAGE POWER AMPLIFIER

CAR
PWR AMP
40525-07/08
REV. A

DRIVE REV
PULSE REV
PULSE FWD
DRIVE FWD

CARRIAGE DRIVE MOTOR

CAR SERVO ERROR
-SERVO DISABLE
CAR. DISABLE SWITCH

POWER MONITOR CKT

PAPER FEED DRIVE A
PAPER FEED DISABLE
PAPER FEED DRIVE B

+ PW. SERVO ENABLE
+ POWER ON
DRIVER RETURN

PAPER FEED DRIVE MOTOR PHASE A
PAPER FEED DRIVE MOTOR PHASE B

+PF A
+PF B
GND

4-87

REVISION HISTORY — # 40525-05 CARRIAGE POWER AMPLIFIER PCB ASSEMBLY

Rev. N   ECO#A1260   Revise schematic, documentation and assembly. Change

B33	from	75K	to	15K
F32/G16	from	82K	to	62K
G18/G19	from	523K	to	392K
C56	from	2K	to	1K

Label G52 and G68 5.1V. Remove −5.1V line from junction G52 and G54.
Change from −XX to −05.

P   A1260A   Correct error on B/M. No schematic or part changes.

Q   A1565   Correct error on B/M. No schematic or part changes.

#40525-06

Rev. A   ECO#A3128   Change circuit board and artwork to accommodate changes for the other
HyType IIs. Only schematic changes are in the following locators:

WAS	IS
C54	B46
C55	B47
C56	B44
C67	A44
D54	A45
D56	A47

#40525-07/08

A   A3278   Revise -05 PCB's to -07 configuration and revise -06 PCB's to -08 con-
figuration. Remove zener diode D74, replace D73 with a jumper. Change
zener diodes A7 and B7 to 11 volt devices, resistor D75 to 5.1K and resistor
B33 to 30K.
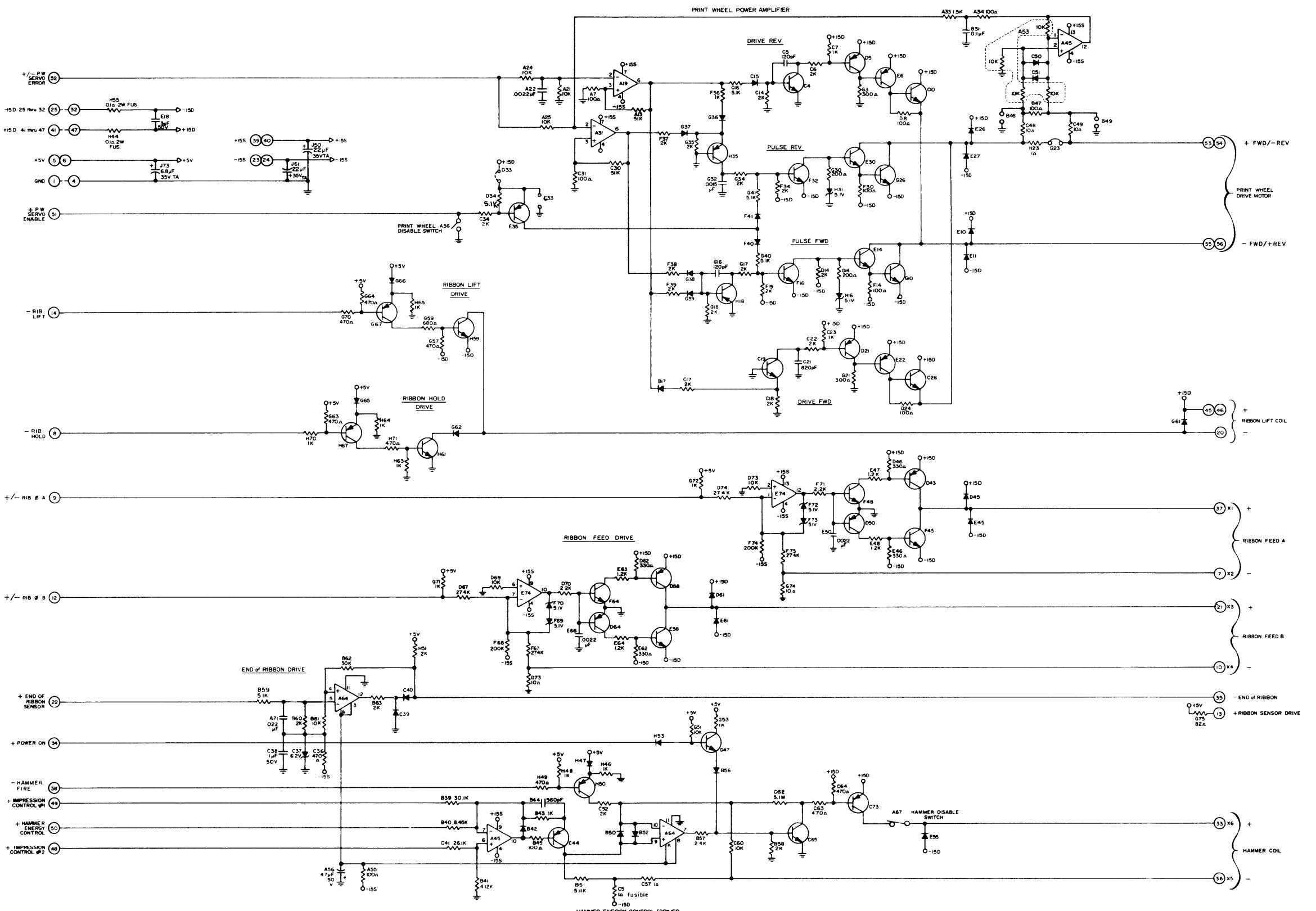
C   A3966   Documentation change and material change of a hardware part to reduce
cost. No schematic changes.

Additional Solid State Components Used:

Diode	1N4002	C13, C19, E13, E20
	1N4454	A8, A12, A19, A20, A25, A32, A33, A37, A38, A59, A60, B8, B9, B19, B20, B25, B26, B36, B37, C54, C67, E75, E76, F72, F73, F74, G72
	1N5415	E53, E67
	1N5807	E48, E63

Zener Diode

5V	1N4733	B5
12V	1N5242B	A7, B7

PW PWR AMP

40530-08

REV. C

4-89

REVISION HISTORY — # 40530-06 PRINT WHEEL POWER AMPLIFIER PCB ASSEMBLY

Rev. M	ECO#A1030	Revise documentation and assembly to allow use of # 40531-06 PCB for # 40530-02 Assembly.
N	A1050	Revise documentation and assembly to change Zener Diode C37 from a 6.8 volt ½W to a 6.2 volt 1W device.
P	A1123	Revise documentation and assembly. Change C34 from 5.1K to 2K. Allow power up sequencing when using power supplies with a low current foldback.
Q	A1230	Revise documentation and assembly. Delete C68, D68, D72, D75, E75 and F66. Change F67 and F75 from 10K to 27.4K. Correct ribbon drive problems. Change drawing No. from 40530-XX to 40530-06.

40530-07

Rev. R	ECO#A1413	Remove .01 μf capacitors from B46, B49 (printwheel drive motor feedback circuit). To help eliminate printwheel retries.

#40530-08

Rev. A	ECO #A3278	Change -07 to -08 configuration. Remove C33, D33, replace D33 with a jumper, and change resistor D34 to 5.01K. Prevents printwheel spin on power-down.
B	A3754	Hardware changes only. No schematic changes.
C	A3966	Documentation change and material change of a hardware part to reduce cost. No schematic changes.

Additional Solid State Components Used:

IC's	319	A64
	747C	A45, E74
	748	A19, A31

Resistor Network
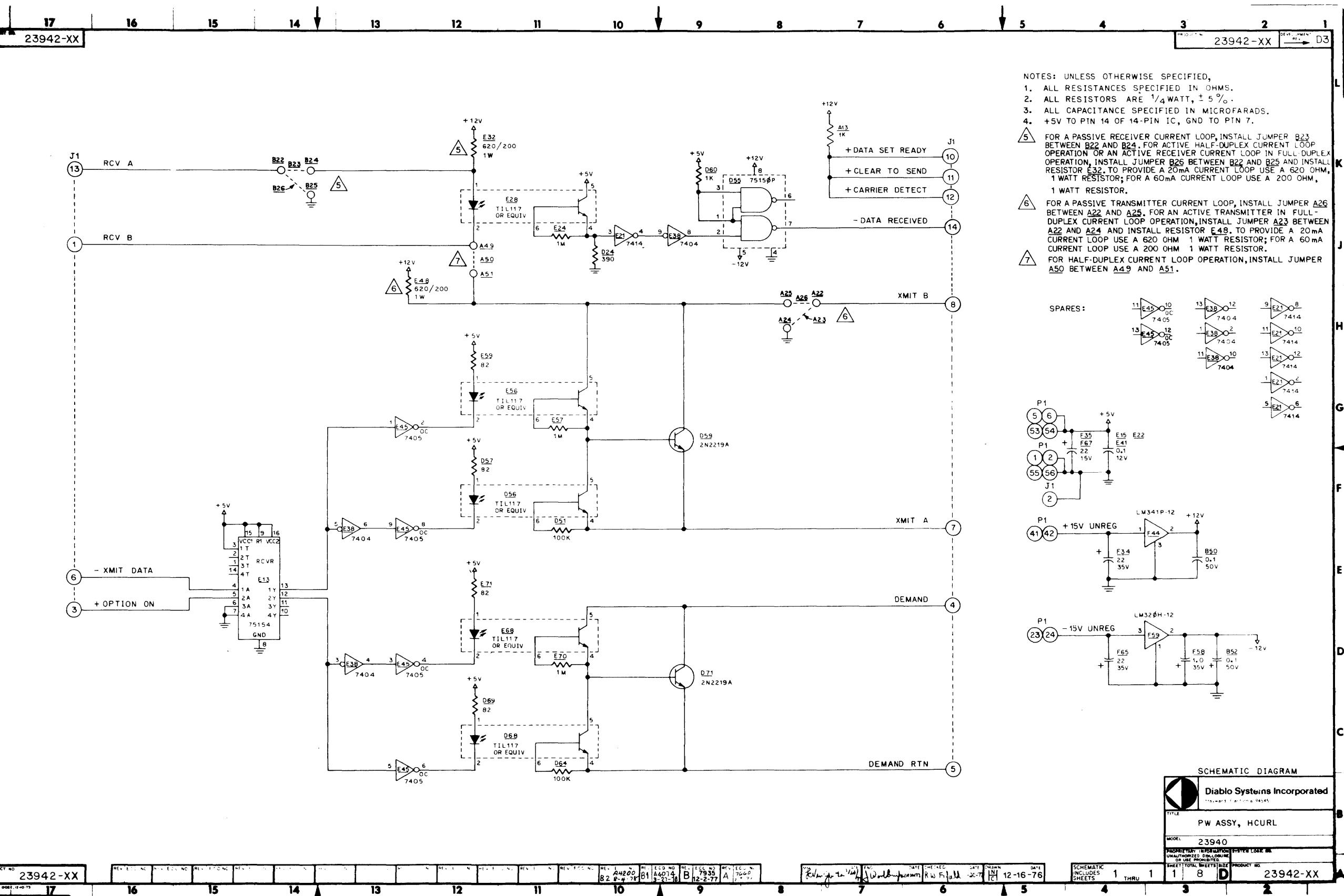
	10K	A53

Transistor	2N3644	C44, D5, D21, D43, D50, D58, D64, E35, G67, H18, H35, H50, H67
	2N4401	C4, C19, C65, E58, F16, F45, F48, F64, G47, H61
	2N5320	E14, E30, H59
	2N5322	E6, E22
	2N6103	C10, C26, G10, G26
	TIP 125	C73

Diode	1N4002	D45, D61, E45, E55, E61, G61, G62
	1N4454	B17, B42, B50, B52, B56, C15, C39, C40, C50, C51, F40, F41, G36, G37, G38, G39, G65, G66, H47, H53
	1N5231	C33, F69, F70, F72, F73, H16, H31
	1N5415	E10, E11, E26, E27

Zener Diode

6.2V	1M6.2Z52	C37

23942-XX DEVELOPMENT D3

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE $1/4$ WATT, $\pm 5\%$.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7.

△5 FOR A PASSIVE RECEIVER CURRENT LOOP, INSTALL JUMPER B23 BETWEEN B22 AND B24. FOR ACTIVE HALF-DUPLEX CURRENT LOOP OPERATION OR AN ACTIVE RECEIVER CURRENT LOOP IN FULL-DUPLEX OPERATION, INSTALL JUMPER B26 BETWEEN B22 AND B25 AND INSTALL RESISTOR E32. TO PROVIDE A 20mA CURRENT LOOP USE A 620 OHM, 1 WATT RESISTOR; FOR A 60mA CURRENT LOOP USE A 200 OHM, 1 WATT RESISTOR.

△6 FOR A PASSIVE TRANSMITTER CURRENT LOOP, INSTALL JUMPER A26 BETWEEN A22 AND A25. FOR AN ACTIVE TRANSMITTER IN FULL-DUPLEX CURRENT LOOP OPERATION, INSTALL JUMPER A23 BETWEEN A22 AND A24 AND INSTALL RESISTOR E48. TO PROVIDE A 20mA CURRENT LOOP USE A 620 OHM, 1 WATT RESISTOR; FOR A 60mA CURRENT LOOP USE A 200 OHM, 1 WATT RESISTOR.

△7 FOR HALF-DUPLEX CURRENT LOOP OPERATION, INSTALL JUMPER A50 BETWEEN A49 AND A51.

SPARES:

J1 RCV A 13
RCV B 1
+12V
E32 620/200 1W
B22 B23 B24
B26 B25

E28 TIL117 OR EQUIV
E24 1M
7414
7404
D24 390

+12V A13 1K
+ DATA SET READY J1 10
+ CLEAR TO SEND 11
+ CARRIER DETECT 12
D60 1K
D55 75150P
- DATA RECEIVED 14
-12V

A49
A50
A51
+12V
E48 620/200 1W
A25 A26 A22
A24 A23
XMIT B 8

E59 82
E56 TIL117 OR EQUIV
E57 1M
D59 2N2219A
7405
D57 82
D56 TIL117 OR EQUIV
D51 100K
7404 7405
XMIT A 7

+5V
VCC1 R1 VCC2
1T
2T
3T
4T RCVR
1A 1Y
2A 2Y
3A 3Y
4A 4Y
75154
GND
E13

- XMIT DATA 6
+ OPTION ON 3

E71 82
E68 TIL117 OR EQUIV
E70 1M
D71 2N2219A
DEMAND 4
D69 82
D68 TIL117 OR EQUIV
D64 100K
7405
DEMAND RTN 5

P1
5 6
53 54
55 56
1 2
J1
2
E35
E67 22 15V
E15 E41 0.1 12V
E22

P1 41 42 +15V UNREG
LM341P-12 +12V
E44
E34 22 35V
B50 0.1 50V

P1 23 24 -15V UNREG
LM320H-12
E53
E65 22 35V
E58 1.0 35V
B52 0.1 50V
-12V

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, HCURL
MODEL 23940

SCHEMATIC INCLUDES SHEETS 1 THRU 1
SHEET 1 TOTAL SHEETS 8 SIZE D
23942-XX

Diablo Systems HCURL

ASSY NO. 23942-[ ] REV

J1 10   14   20   40   50   60   70

NOTES —

⚠ ASSEMBLY DASH NUMBER AND REVISION LEVEL SHALL BE MARKED ON THE PWB WITH NON-CONDUCTIVE INK.

⚠ CUT PIN 9 FLUSH WITH CONNECTOR SURFACE, ITEM 5 AS SHOWN TO POLARIZE CONNECTOR.

DASH N°	DESCRIPTION	INSTALL
-99	PASSIVE FULL-DUPLEX	JUMPER A26 BETWEEN A22 AND A25 JUMPER B23 BETWEEN B22 AND B24
-01	PASSIVE HALF-DUPLEX	JUMPER A26 BETWEEN A22 AND A25 JUMPER B23 BETWEEN B22 AND B24 JUMPER A50 BETWEEN A49 AND A51
-02	20 mA ACTIVE FULL-DUPLEX	JUMPER A23 BETWEEN A22 AND A24 JUMPER B26 BETWEEN B22 AND B25 RESISTORS E32 AND E48 (620 OHMS)
-03	20 mA ACTIVE HALF-DUPLEX	JUMPER A23 BETWEEN A22 AND A24 JUMPER B26 BETWEEN B22 AND B25 JUMPER A50 BETWEEN A49 AND A51 RESISTOR E32 (620 OHMS)
-04	60 mA ACTIVE FULL-DUPLEX	JUMPER A23 BETWEEN A22 AND A24 JUMPER B26 BETWEEN B22 AND B25 RESISTORS E32 AND E48 (200 OHMS)
-05	60 mA ACTIVE HALF-DUPLEX	JUMPER A23 BETWEEN A22 AND A24 JUMPER B26 BETWEEN B22 AND B25 JUMPER A50 BETWEEN A49 AND A51 RESISTOR E32 (200 OHMS)

.100 ± .030 (3) PLACE

Diablo Systems Incorporated
Hayward California 94545

PWA, HCURL ASSEMBLY

DRAWN N. HOLLANDER 1-19-77
CHECKED R.W. F____ 1-20-77

DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE

B1 A4074 9-27-78, B2 A4200 8-4-78
A 76__ B 7935 12-1-77
REVISIONS

FIRST USED 23940

SCALE 2x   SHEET 2   TOT SH 8

SIZE D   23942-X

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED
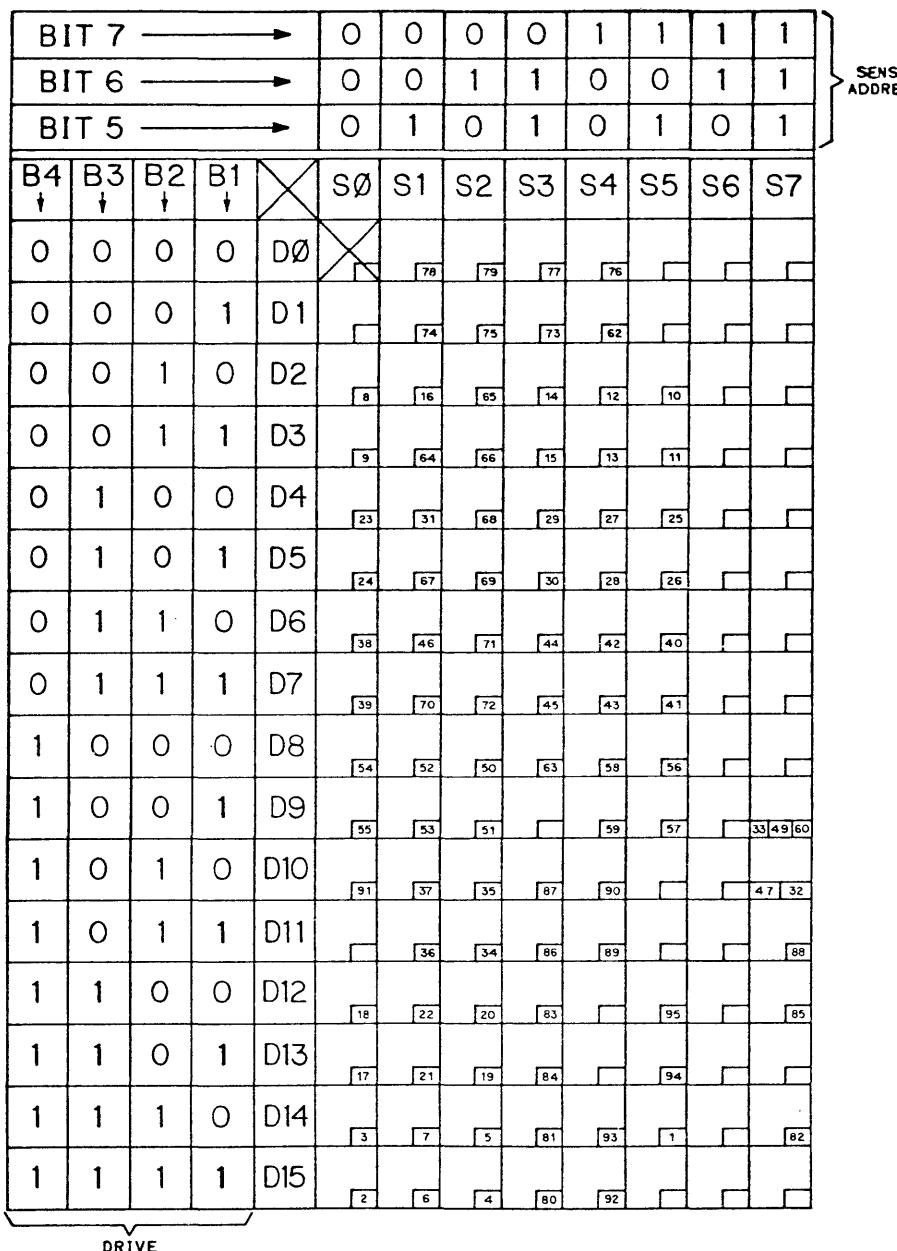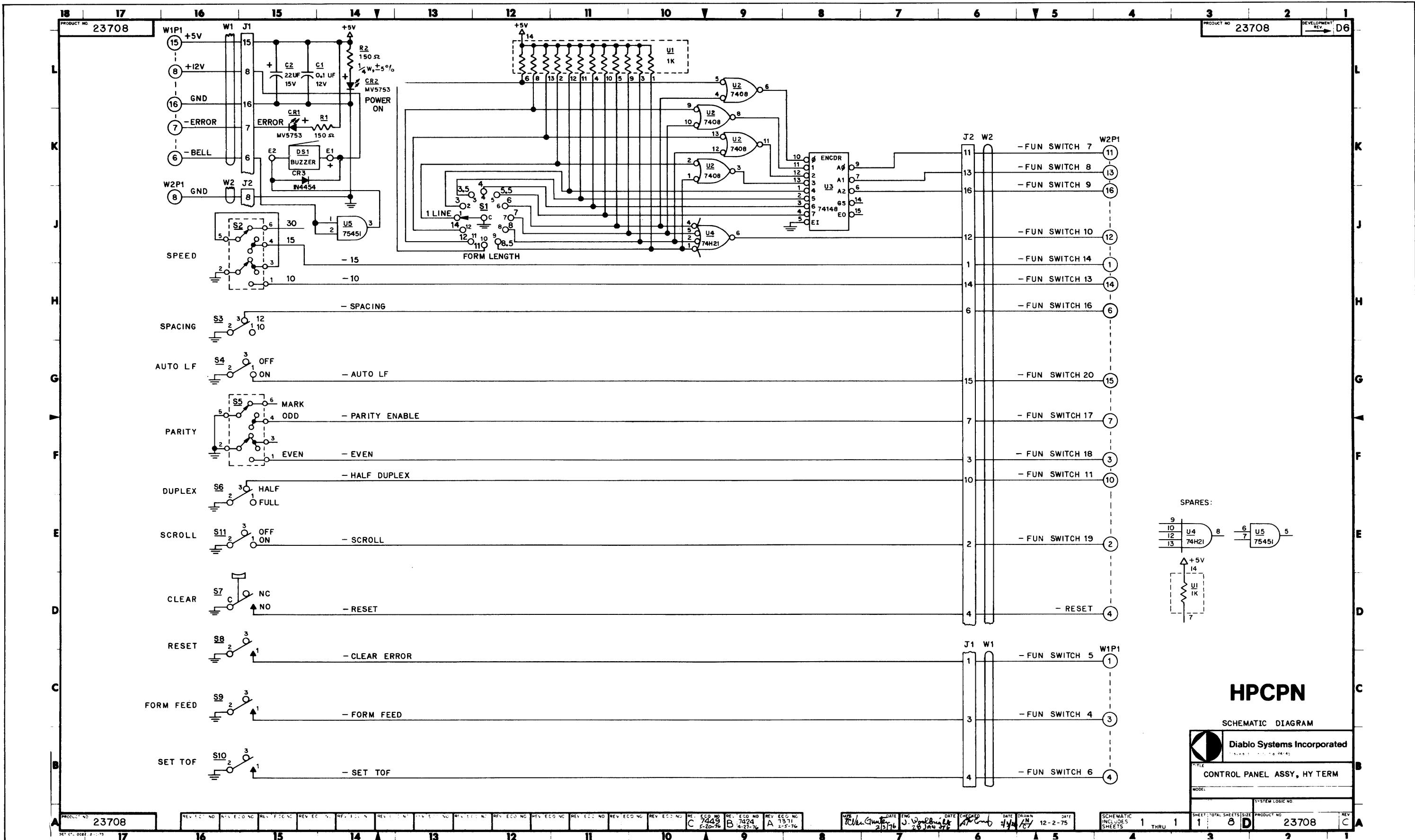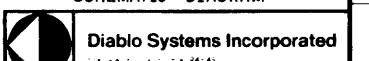
23897 — D1

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT. ±5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC: GND TO PIN 7.
5. R31 AND R32 NOT INSTALLED.
6. SOLID-STATE SWITCH MODULES.
7. DIABLO PART NUMBER.
8. R21, R23, Q26 NOT INSTALLED ON SOME KEYBOARD VERSIONS.

+5V
R24 8.2K   R23 8.2K
Q27 MPS6516   Q26 MPS6516
R22 2.4K   R21 2.4K
R25 270

ENCODED KEYS

+5V
R20 5.62K   R19 25.5K
TPB DETECT
TPA STB
TIME DLY VCC
PULSE GEN
E
STB   OUT
U4
14027
ADJ   GND
C28 15 16V

NORMAL
10-100µs (NOMINALLY 50µs)
REPEAT
300 ±50ms   50 ±10ms

U1 7404   U2 7404   + KYSTB (12)

2 OF 13

MATRIX

+5V
VCC
A B C D E F G H J K L M N
ENCDR/DCDR
U3
14026

STB
BØ   − DATA Ø (13)
B1   − DATA 1 (16)
B2   − DATA 2 (18)
B3   − DATA 3 (20)
B4   − DATA 4 (19)
B5   − DATA 5 (17)
B6   − DATA 6 (15)
B7   (14)
CTRL
SHIFT
VGG   GND
−12V

U2 7404   U1 7404

R32 R31

R18 R17 R16 R15 R14 R10 R11 R12 R13
300 300 300 300 300 300 300 300

33

+5V
+5V   −12V
C29 15 16V   C30 0.1 16V

SPARES:
U1 7404
PART OF U4

TYPICAL SWITCH MODULE
(BOTTOM VIEW)
+5V
OUTPUT 2
OUTPUT 1
GND

KEY 33,49,60   SHIFT   − FKY 4 (5)
KEY 32,47   CTRL   − FKY 5 (6)
KEY 88   UC ONLY   − FKY 1 (7)
KEY 85   LOCAL   − FKY 2 (8)
KEY 82   BREAK   − FKY 3 (10)

+5V
R5 6.8K   R7 6.8K   R6 6.8K   R8 6.8K   R9 6.8K

Diablo Systems Incorporated

SCHEMATIC: KEYBOARD ASSY
1620 HyTERM

23897   REV A

6-16-76

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

DRAWINGS FURNISHED BY CORTRON INC.
FOR MAINTENANCE PURPOSES ONLY.

SCHEMATIC: CORTRON KEYBOARD
Hu TERM 1620, TYPE PR LOGICAL BIT PAIR

SHEET 1 OF 2

DWG NO. 400512-01

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE ±5%, 1/4 WATT.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
   +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
5. FOR INDIVIDUAL KEY DEFINITIONS REFER TO APPLICABLE
   KEYBOARD SPECIFICATION DRAWING.

REF DIABLO P/N	CORTRON P/N	PROM P/N	REV
23962-XX	55-500190	80-551581	A
23963-XX	55-500221	80-551660	ORIG

4-95

					SENSE ADDRESS							
BIT 7 →					0	0	0	0	1	1	1	1
BIT 6 →					0	0	1	1	0	0	1	1
BIT 5 →					0	1	0	1	0	1	0	1

B4 ↓	B3 ↓	B2 ↓	B1 ↓		S0	S1	S2	S3	S4	S5	S6	S7
0	0	0	0	D0	X	78	79	77	76			
0	0	0	1	D1		74	75	73	62			
0	0	1	0	D2	8	16	65	14	12	10		
0	0	1	1	D3	9	64	66	15	13	11		
0	1	0	0	D4	23	31	68	29	27	25		
0	1	0	1	D5	24	67	69	30	28	26		
0	1	1	0	D6	38	46	71	44	42	40		
0	1	1	1	D7	39	70	72	45	43	41		
1	0	0	0	D8	54	52	50	63	58	56		
1	0	0	1	D9	55	53	51		59	57		33 49 60
1	0	1	0	D10	91	37	35	87	90			47 32
1	0	1	1	D11		36	34	86	89			88
1	1	0	0	D12	18	22	20	83		95		85
1	1	0	1	D13	17	21	19	84		94		
1	1	1	0	D14	3	7	5	81	93	1		82
1	1	1	1	D15	2	6	4	80	92			

DRIVE ADDRESS

SCHEMATIC DIAGRAM

4-96

HPCPN

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

CONTROL PANEL ASSY, HY TERM

PRODUCT NO 23708

DEVELOPMENT REV D6

W1P1 — +5V (15)
— +12V (8)
— GND (16)
— ERROR (7)
— BELL (6)

W2P1 — GND (8)

W1 J1 15, 8, 16, 7, 6
W2 J2 8

C2 22UF 15V
C1 0.1 UF 12V
R2 150Ω 1/4W, ±5%
CR2 MV5753 POWER ON
CR1 MV5753 ERROR
R1 150Ω
DS1 BUZZER
CR3 1N4454
E2, E1

U5 75451
U1 1K
U2 7408
U3 74148
U4 74H21

ENCDR A0, A1, A2, GS, EO, EI

SPEED — S2 — 30, 15, 10
SPACING — S3 — 12, 10
AUTO LF — S4 — OFF, ON
PARITY — S5 — MARK, ODD, EVEN
DUPLEX — S6 — HALF, FULL
SCROLL — S11 — OFF, ON
CLEAR — S7 — NC, NO
RESET — S8
FORM FEED — S9
SET TOF — S10

S1 1 LINE
FORM LENGTH

— SPACING
— AUTO LF
— PARITY ENABLE
— EVEN
— HALF DUPLEX
— SCROLL
— RESET
— CLEAR ERROR
— FORM FEED
— SET TOF

J2 W2   W2P1
11 — FUN SWITCH 7 (11)
13 — FUN SWITCH 8 (13)
16 — FUN SWITCH 9 (16)
12 — FUN SWITCH 10 (12)
1 — FUN SWITCH 14 (1)
14 — FUN SWITCH 13 (14)
6 — FUN SWITCH 16 (6)
15 — FUN SWITCH 20 (15)
7 — FUN SWITCH 17 (7)
3 — FUN SWITCH 18 (3)
10 — FUN SWITCH 11 (10)
2 — FUN SWITCH 19 (2)
4 — RESET (4)

J1 W1   W1P1
1 — FUN SWITCH 5 (1)
3 — FUN SWITCH 4 (3)
4 — FUN SWITCH 6 (4)

SPARES:
U4 74H21
U5 75451
U1 1K
+5V

23708 HPCPN Control Panel
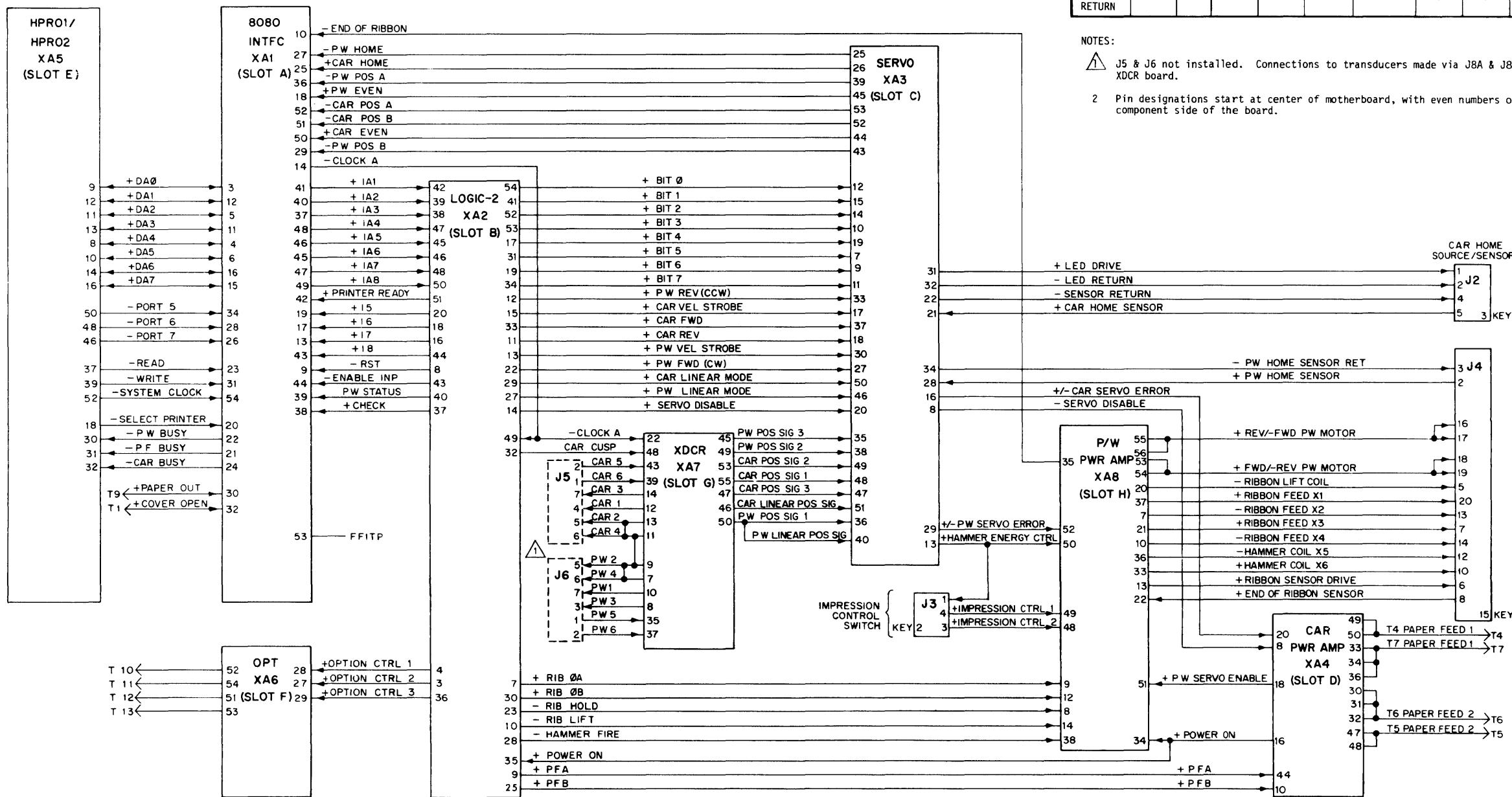
Rev. A   ECO 7371   As Released.

    B   7424   (1)   U5 (75451) added to drive audible alarm. Return side of alarm connected to +12V. CR3 added for noise suppression.
                              (2)   Schematic corrected: U1-6 was shown as U1-7.

    C   7449   Hardware changes to improve ease of assembly and adjustment. No circuit changes.

    D   7507   Change height of LEDs to .650 in overall.

POWER DISTRIBUTION

CONNECTOR

VOLTAGE	J1	J4	XA1	XA2	XA3	XA4	XA5	XA6	XA7	XA8	TERM
SIGNAL GROUND	A,B,C	11	1,2 55,56	1,2 55,56	1-4 55,56	–	1-4 55,56	1-4 55,56	1-4	–	T2,T3 T8
+5V	L,J	–	7,8	5,6 21	5,6	5,6	5,6	5,6	5,6	5,6	–
+15VS	F,K,D	–	–	–	41,42	35,38	41,42	41,42	41,42	39,40	–
-15VS	R,N	–	–	–	23,24	19,22	23,24	23,24	23,24	23,24	–
+15VD	H,E	4,9	–	–	–	37,39-43, 45,46	–	49,50	–	41-47	–
-15VD	P,M	–	–	–	–	21,23-29	–	31,32	–	25-32	–
ANALOG GND	A,B,C	–	–	–	–	1-4	–	–	–	1-4	–
DRIVER RETURN	A,B,C	–	–	–	–	51-56	21,22	21,22	–	–	–

NOTES:

⚠ J5 & J6 not installed. Connections to transducers made via J8A & J8B on XDCR board.

2 Pin designations start at center of motherboard, with even numbers on the component side of the board.

HPRO1/ HPRO2 XA5 (SLOT E)

8080 INTFC XA1 (SLOT A)

LOGIC-2 XA2 (SLOT B)

SERVO XA3 (SLOT C)

XDCR XA7 (SLOT G)

P/W PWR AMP XA8 (SLOT H)

CAR PWR AMP XA4 (SLOT D)

OPT XA6 (SLOT F)

CAR HOME SOURCE/SENSOR

- END OF RIBBON
- PW HOME
+ CAR HOME
- PW POS A
+ PW EVEN
- CAR POS A
- CAR POS B
+ CAR EVEN
- PW POS B
- CLOCK A

+ DA0
+ DA1
+ DA2
+ DA3
+ DA4
+ DA5
+ DA6
+ DA7

- PORT 5
- PORT 6
- PORT 7

- READ
- WRITE
- SYSTEM CLOCK

- SELECT PRINTER
- PW BUSY
- PF BUSY
- CAR BUSY

+ PAPER OUT
+ COVER OPEN

+ IA1
+ IA2
+ IA3
+ IA4
+ IA5
+ IA6
+ IA7
+ IA8
+ PRINTER READY
+ I5
+ I6
+ I7
+ I8
- RST
- ENABLE INP
PW STATUS
+ CHECK

FFITP

+ BIT 0
+ BIT 1
+ BIT 2
+ BIT 3
+ BIT 4
+ BIT 5
+ BIT 6
+ BIT 7
+ PW REV (CCW)
+ CAR VEL STROBE
+ CAR FWD
+ CAR REV
+ PW VEL STROBE
+ PW FWD (CW)
+ CAR LINEAR MODE
+ PW LINEAR MODE
+ SERVO DISABLE

- CLOCK A
CAR CUSP
CAR 5
CAR 6
CAR 3
CAR 1
CAR 2
CAR 4

PW 2
PW 4
PW 1
PW 3
PW 5
PW 6

PW POS SIG 3
PW POS SIG 2
CAR POS SIG 2
CAR POS SIG 1
CAR POS SIG 3
CAR LINEAR POS SIG
PW POS SIG 1
PW LINEAR POS SIG

+ LED DRIVE
- LED RETURN
- SENSOR RETURN
+ CAR HOME SENSOR

- PW HOME SENSOR RET
+ PW HOME SENSOR

+/- CAR SERVO ERROR
- SERVO DISABLE

+/- PW SERVO ERROR
+HAMMER ENERGY CTRL

+ REV/-FWD PW MOTOR
+ FWD/-REV PW MOTOR
- RIBBON LIFT COIL
+ RIBBON FEED X1
- RIBBON FEED X2
+ RIBBON FEED X3
- RIBBON FEED X4
- HAMMER COIL X5
+ HAMMER COIL X6
+ RIBBON SENSOR DRIVE
+ END OF RIBBON SENSOR

+ PW SERVO ENABLE

+ POWER ON

IMPRESSION CONTROL SWITCH
+IMPRESSION CTRL 1
+IMPRESSION CTRL 2

+OPTION CTRL 1
+OPTION CTRL 2
+OPTION CTRL 3

+ RIB 0A
+ RIB 0B
- RIB HOLD
- RIB LIFT
- HAMMER FIRE
+ POWER ON
+ PFA
+ PFB

+ PFA
+ PFB

T4 PAPER FEED 1
T7 PAPER FEED 1
T6 PAPER FEED 2
T5 PAPER FEED 2

J2
J4
J3

MOTHER BOARD
40614-XX
REV. E

4-99

40614 Hy Term Mother Board

Rev.	A	ECO 9853	As released.
	B	9877	Add —SERVO DISABLE signal from SERVO board (XA3-8) to CAR PWR AMP board (XA4-8). Cut traces and add twisted pairs to reduce noise problems.
	C	9911	Mother board lowered to improve cooling.
	D	A1028	J5 and J6 connectors and twisted pairs removed: not needed when used with 40515 XDCR board.
	E	A1290	Document change only. Schematic error corrected; FF2TP (pin 20), FF3TP (pin 23), and FF4TP (pin 21) removed.

POWER DISTRIBUTION

CONNECTOR
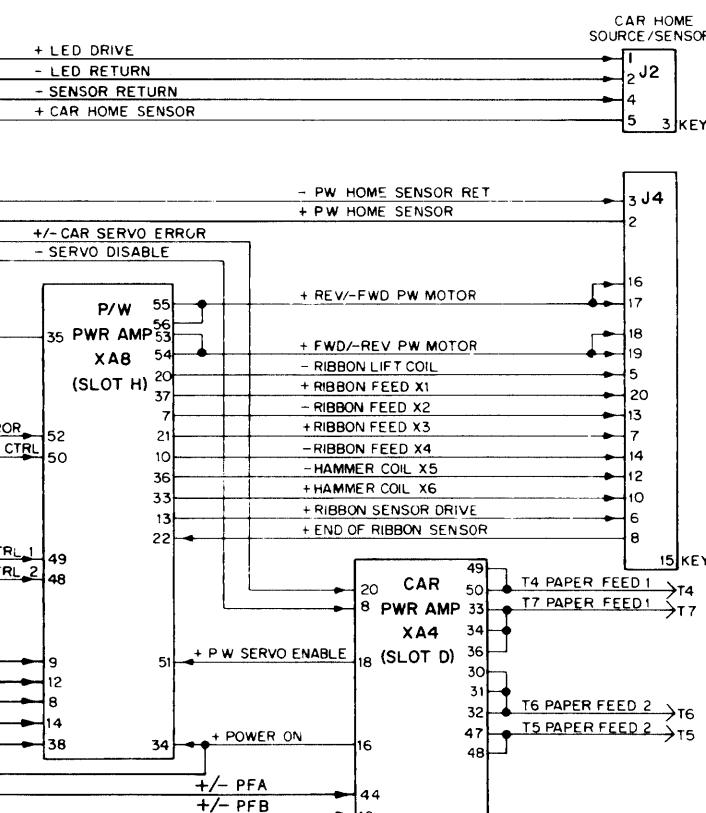
VOLTAGE	J4	XA1	XA2	XA3	XA4	XA5	XA6	XA7	XA8	TERM
SIGNAL GROUND	11 —	1,2 33,35 55,56	1,2 55,56	1-4 55,56	—	1-2 55,56	1-2 55,56	1-4	—	T2,T3 T8,T14
+5V	—	7,8	5,6 21	5,6	5,6	5,6 53,54	5,6 53,54	5,6	5,6	T15
+15VS	—	—	—	41,42	35,38	41,42	41,42	41,42	39,40	T12
-15VS	—	—	—	23,24	19,22	23,24	23,24	23,24	23,24	T11
+15VD	4,9	—	—	—	37,39-43, 45,46	—	—	51,52	41-47	T12
-15VD	—	—	—	—	21,23-29	—	—	27,28	25-32	T11
ANALOG GND	—	—	—	—	1-4	—	—	—	1-4	T13
DRIVER RETURN	—	—	—	—	51-56	—	—	—	—	T14

NOTES:

⚠ All pins of XA5 connected to corresponding pin # of XA6.

2 Pin designations start at center of motherboard, with even numbers on the component side of the board.

MOTHER BOARD 46080-01

REV.C
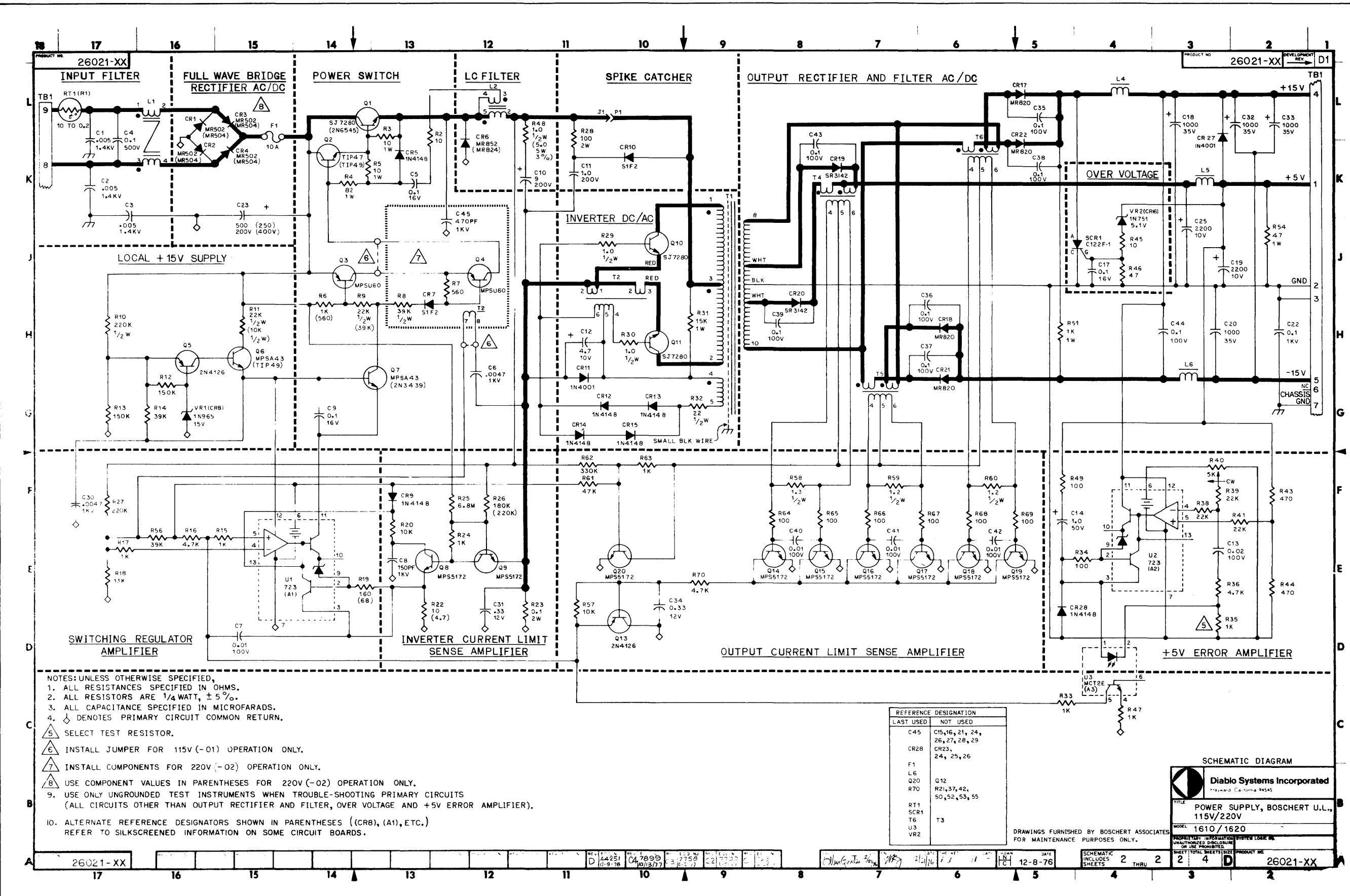
REVISION HISTORY — 46080-01 MOTHER BOARD
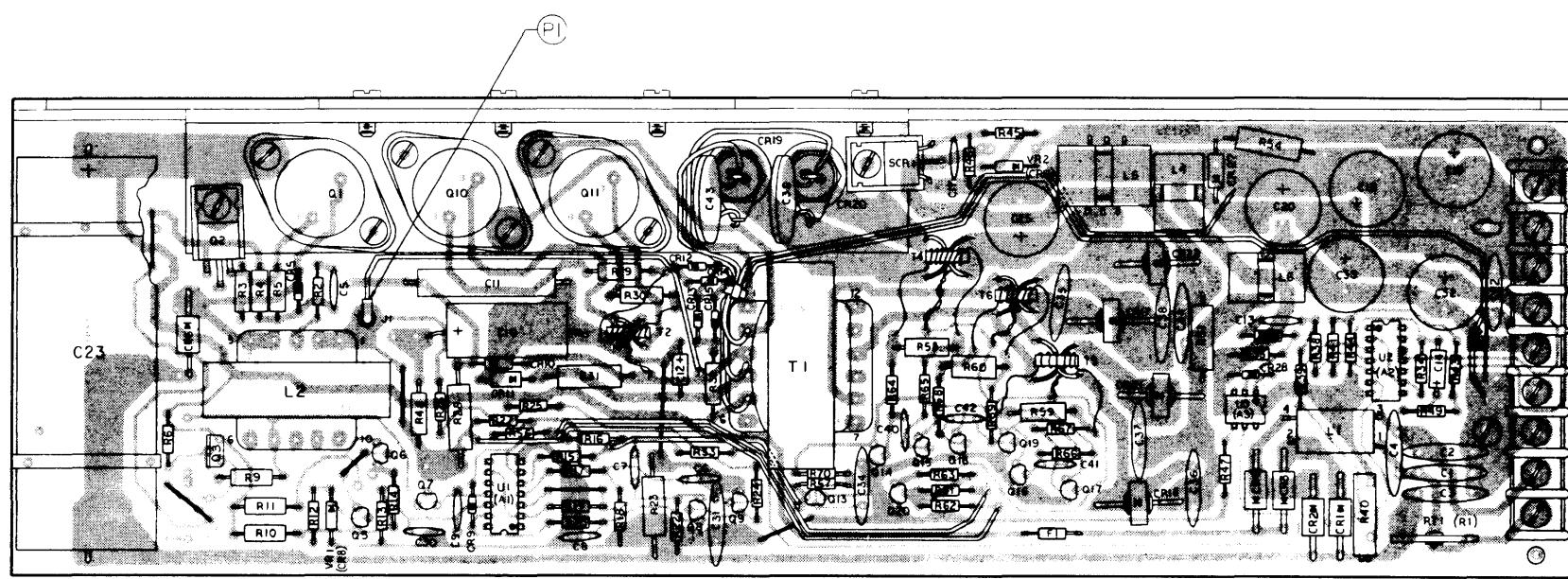
Rev. A   ECO A1759   As released.

    B   A1869   Correct error in part no. on bill of material. No change to board.

    C   A3603   Hardware change only. No change to board.

SCHEMATIC POWER SUPPLY 26021-XX

INPUT FILTER

FULL WAVE BRIDGE RECTIFIER AC/DC

POWER SWITCH

LC FILTER

SPIKE CATCHER

OUTPUT RECTIFIER AND FILTER AC/DC

OVER VOLTAGE

LOCAL +15V SUPPLY

INVERTER DC/AC

SWITCHING REGULATOR AMPLIFIER

INVERTER CURRENT LIMIT SENSE AMPLIFIER

OUTPUT CURRENT LIMIT SENSE AMPLIFIER

+5V ERROR AMPLIFIER

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. ◇ DENOTES PRIMARY CIRCUIT COMMON RETURN.
5. SELECT TEST RESISTOR.
6. INSTALL JUMPER FOR 115V (-01) OPERATION ONLY.
7. INSTALL COMPONENTS FOR 220V (-02) OPERATION ONLY.
8. USE COMPONENT VALUES IN PARENTHESES FOR 220V (-02) OPERATION ONLY.
9. USE ONLY UNGROUNDED TEST INSTRUMENTS WHEN TROUBLE-SHOOTING PRIMARY CIRCUITS (ALL CIRCUITS OTHER THAN OUTPUT RECTIFIER AND FILTER, OVER VOLTAGE AND +5V ERROR AMPLIFIER).
10. ALTERNATE REFERENCE DESIGNATORS SHOWN IN PARENTHESES (e.g. (CR8), (A1), ETC.). REFER TO SILKSCREENED INFORMATION ON SOME CIRCUIT BOARDS.

REFERENCE DESIGNATION	
LAST USED	NOT USED
C45	C15,16, 21, 24, 26, 27, 28, 29
CR28	CR23, 24, 25, 26
F1	
L6	
Q20	Q12
R70	R21, 37, 42, 50, 52, 53, 55
RT1	
SCR1	
T6	T3
U3	
VR2	

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

TITLE: POWER SUPPLY, BOSCHERT U.L., 115V/220V

MODEL: 1610/1620

DRAWINGS FURNISHED BY BOSCHERT ASSOCIATES FOR MAINTENANCE PURPOSES ONLY.

DATE 12-8-76

SCHEMATIC INCLUDES SHEETS 2 THRU 2

26021-XX

4-103

115V A.C. VERSION

(26021-01)

TB1
1 [+5V]
2 [GND]
3 [GND]
4 [+15V]
5 [−15V]
6 [N.C.]
7 [CHASSIS GND]
8 [A.C. HOT]
9 [A.C. NEUT.]

220V A.C. VERSION

(26021-02)

TB1
1 [+5V]
2 [GND]
3 [GND]
4 [+15V]
5 [−15V]
6 [N.C.]
7 [CHASSIS GND]
8 [A.C. HOT]
9 [A.C. NEUT.]

**ASSEMBLY DWG.
POWER SUPPLY
26021-XX**

"DRAWINGS FURNISHED BY BOSCHERT ASSOICATES
FOR MAINTENANCE PURPOSES ONLY."

Revision History — #26021-XX Power Supply

Rev. A   ECO#7472   As released

Rev. B   ECO#7504   Add requirement for label containing part number, serial number, and mfg. date code.

Rev. C   ECO#7587   Add special label to 220V units.

Rev. C1   ECO#7631   Add schematic and assembly drawings to part no.

Rev. C2   ECO#7700   Correct minor schematic errors, add alternate reference designators.

Rev. C3   ECO#7758   Correct error on connection drawing, sheet 1.

Rev. C4   ECO#7899   Move cathode of diode CR27 from input to output of L4; reduces 5V ripple.

Make the following component changes:

Component	Was	Is
R3,R4,R5	¼ Watt	1 Watt
Q1	SJ7280(2N6308)	SJ7280(2N6545)
Q3,Q4	MPSA93	MPSU60
CR19,CR20	1N3889	SR3142
R8	22K	39K
R9	22K	22K(39K)
R19	160(33)	160(68)
R22	10(2.2)	10(4.7)

NOTE: Component values in parentheses are for 220V operation.

Rev. D   ECOA#4251   Remove L3 to reduce noise

REVISION HISTORY — MISCELLANEOUS WIRE & CABLE ASSEMBLIES
(Including 24471 Rev. C)

Rev. A   ECO#9684   As Released.
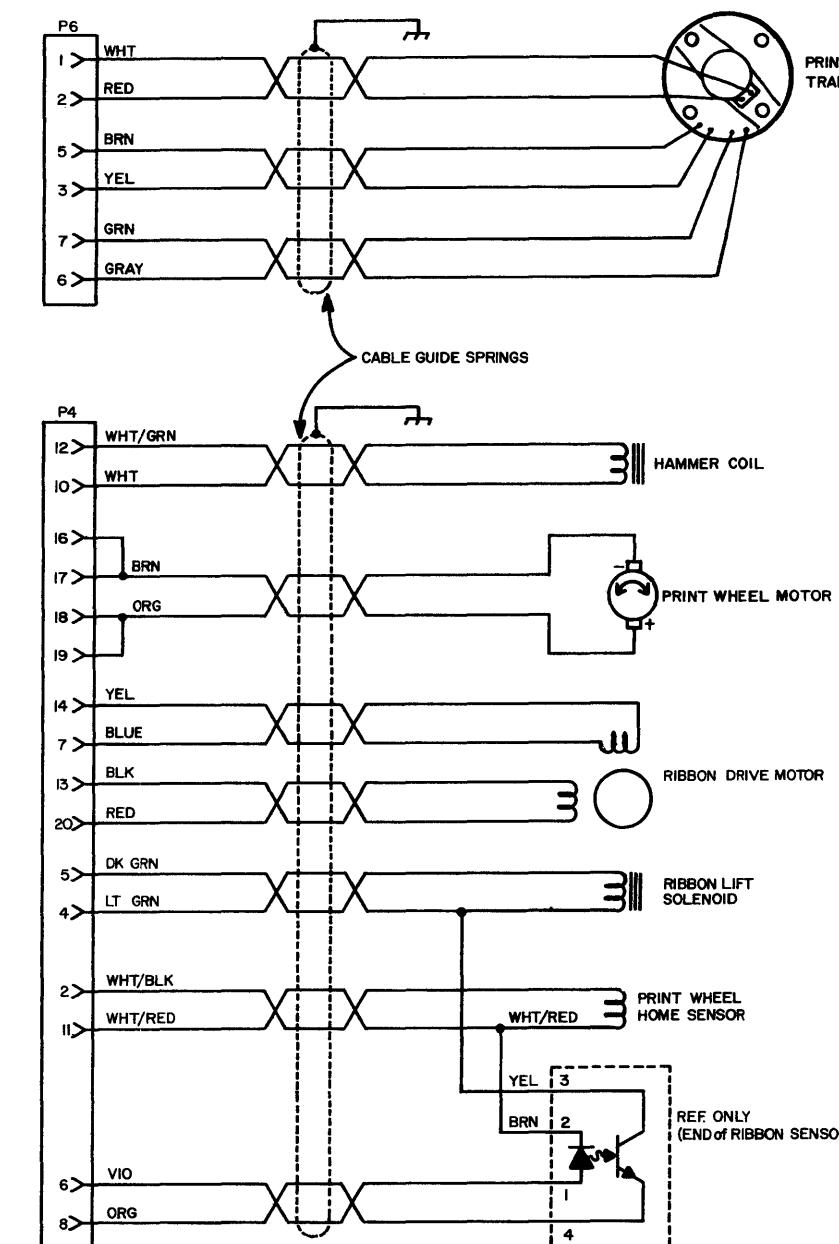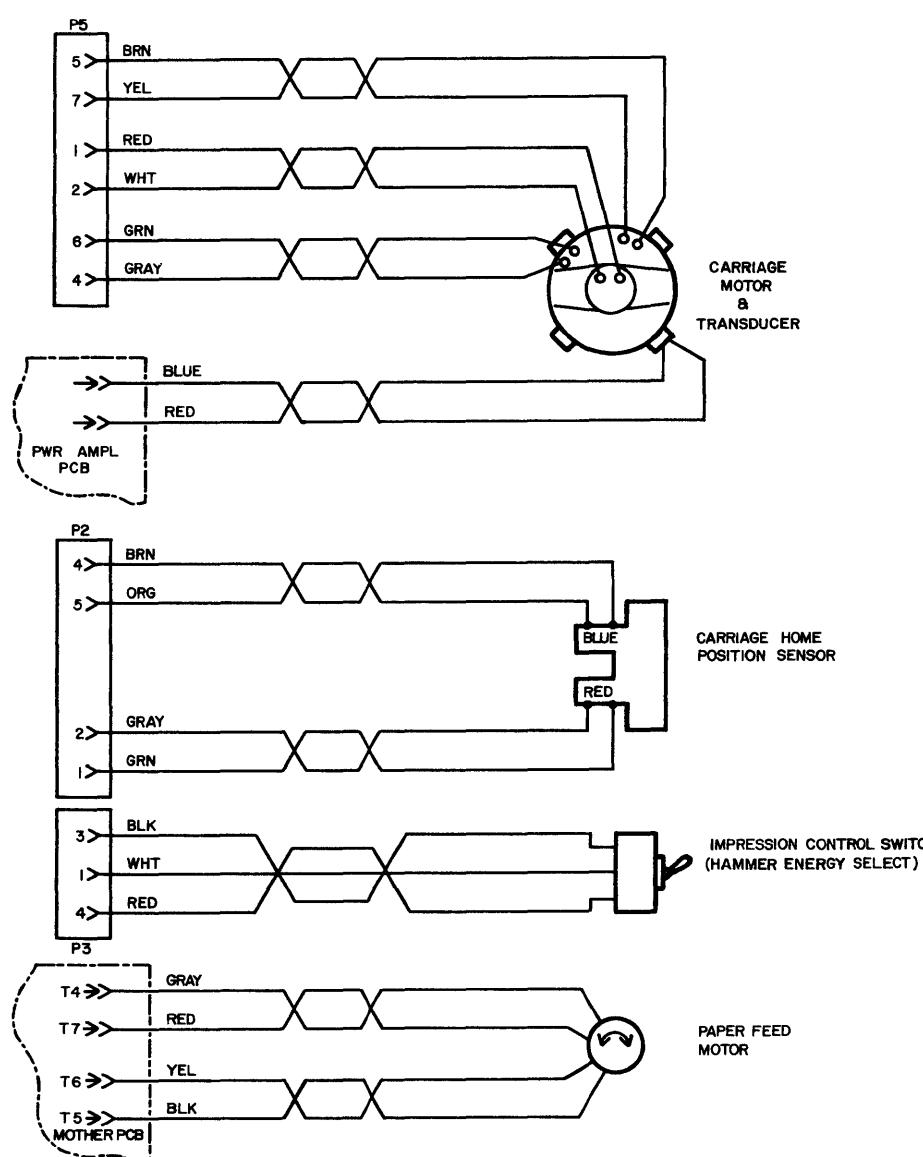
B   9797   Revise documentation and assembly to remove two wires from cable spring to improve flexibility.

C   9901   Revise documentation and assembly to prevent wire breakage in cable spring.
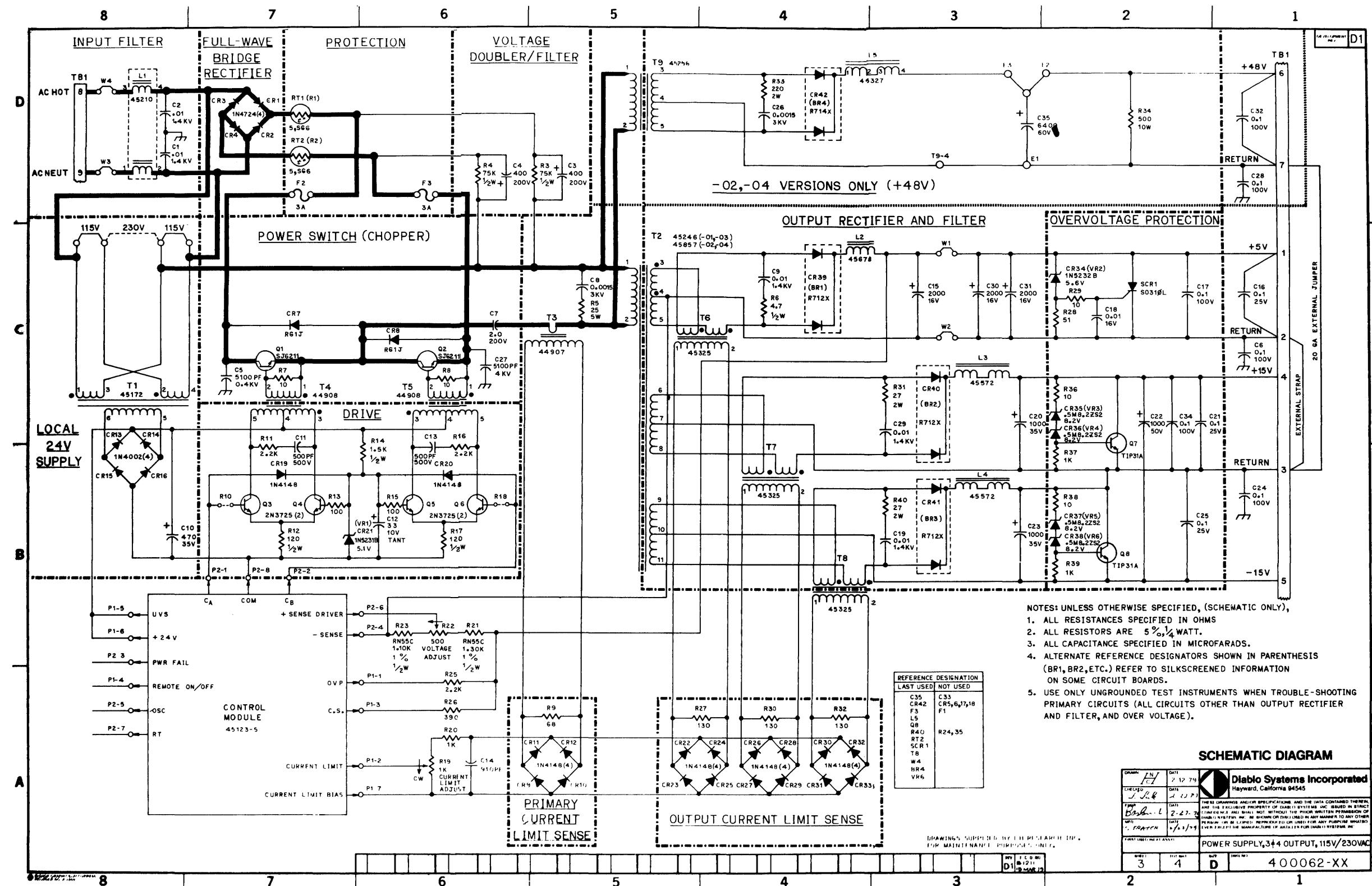
D   A1102   Add wiring for l.h. paper feed (split platen) motor. (Not applicable to HyTerm.)
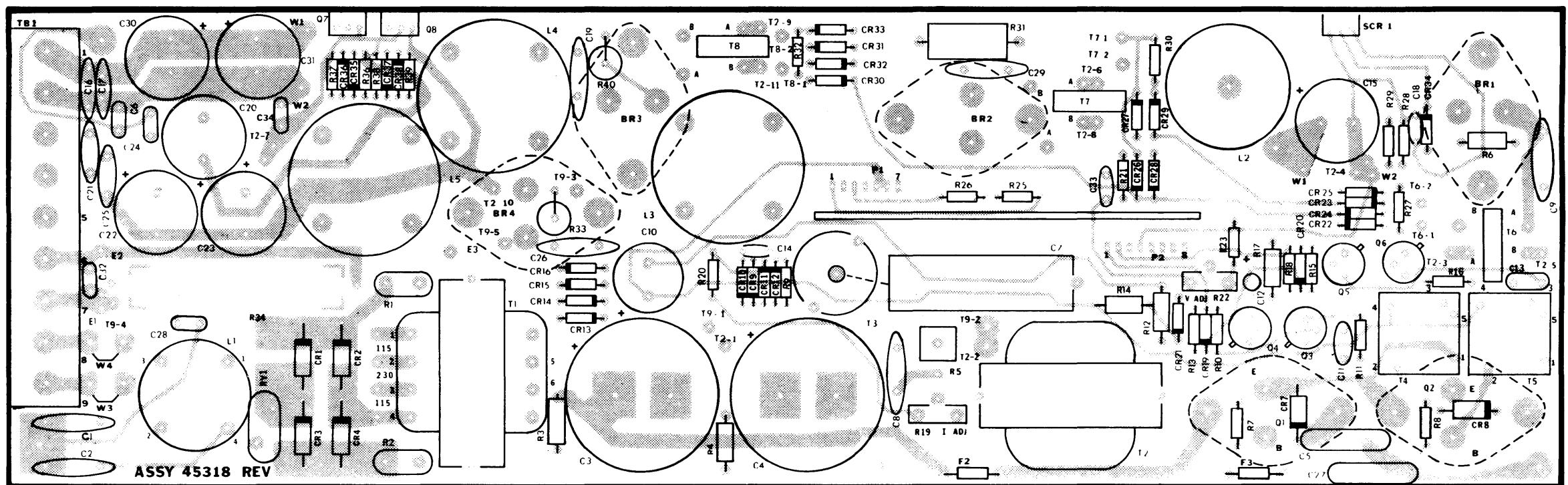
E   A1244   Correct schematic error: swap wires on T10 & T12. (Not applicable to HyTerm.)

F   A1582   Gray and green wires on P2-1&2 interchanged: gray to pin 2, green to pin 1.

PRINTER CABLES

24471

REV. F

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

POWER SUPPLY, 3+4 OUTPUT, 115V/230VAC
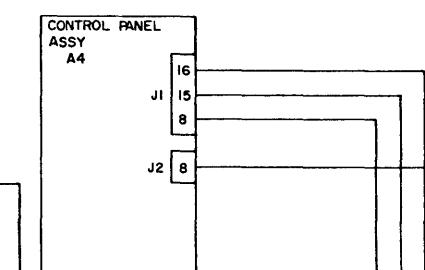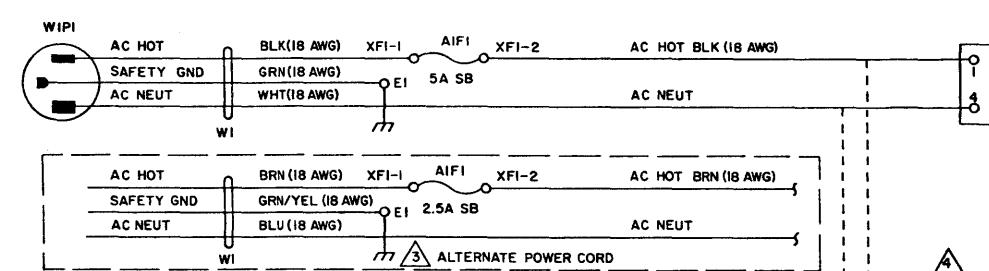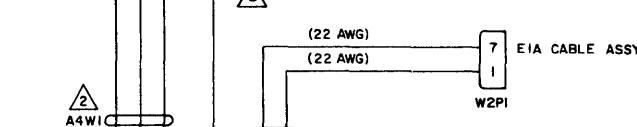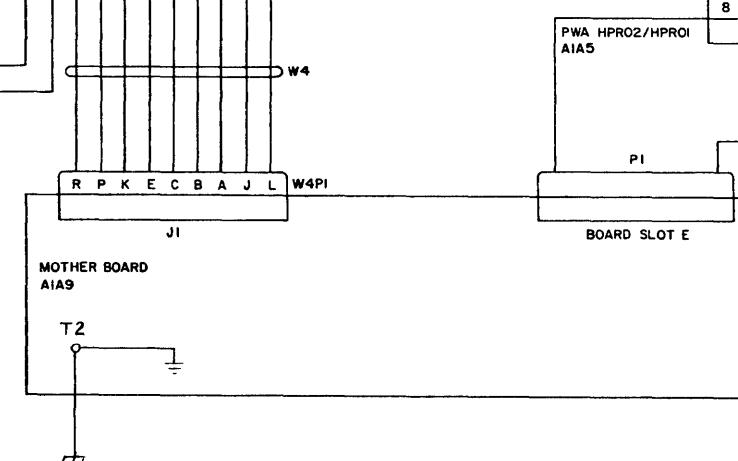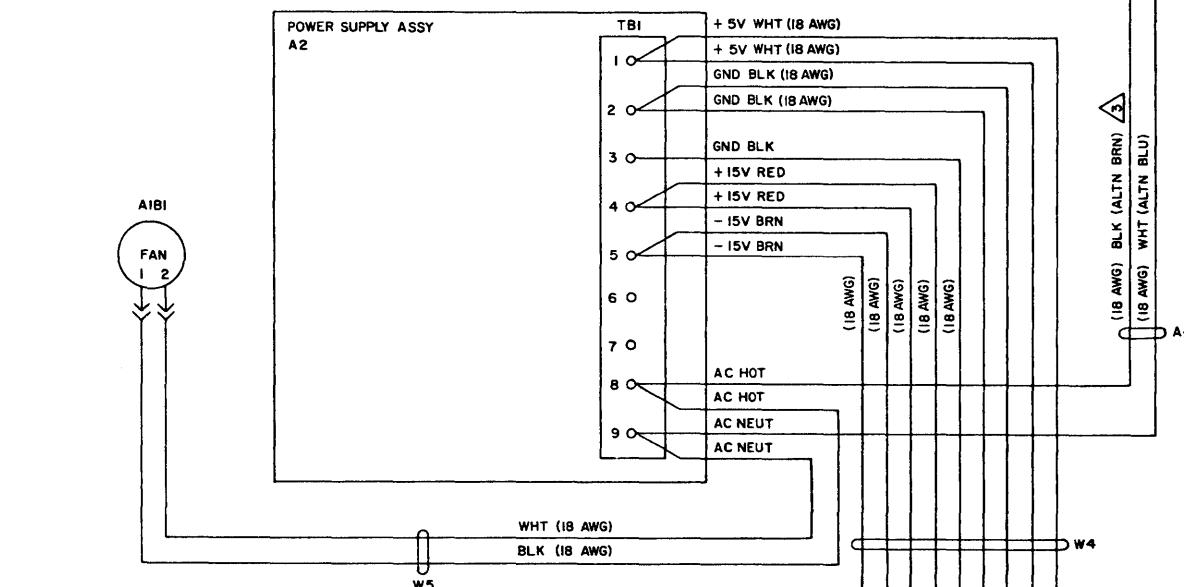
400062-XX

DRAWING FURNISHED BY L.H. RESEARCH INC
FOR MAINTENANCE PURPOSES ONLY

ASSEMBLY DWG.
POWER SUPPLY
400062-XX

DEVELOPMENT REV D1

DWG NO 23859

DEVELOPMENT REV D1

NOTES:

1. KEYBOARD NOT PART OF MODEL 1610.

2. ONLY POWER LEADS ARE SHOWN IN THESE CABLES. REFER TO 23732 FOR COMPLETE WIRING.

3. ALTERNATE POWER CORD IS USED FOR GREATER THAN 115 VAC OPERATION.

4. CHANGE IN AC WIRING WHEN CONTROL PANEL IS NOT INSTALLED.

CONTROL PANEL ASSY A4

J1 16 15 8

J2 8

W1P1

AC HOT   BLK (18 AWG)   XF1-1   A1F1   XF1-2   AC HOT BLK (18 AWG)
SAFETY GND   GRN (18 AWG)
AC NEUT   WHT (18 AWG)   E1   5A SB   AC NEUT
W1

AC HOT   BRN (18 AWG)   XF1-1   A1F1   XF1-2   AC HOT BRN (18 AWG)
SAFETY GND   GRN/YEL (18 AWG)
AC NEUT   BLU (18 AWG)   E1   2.5A SB   AC NEUT
W1   ALTERNATE POWER CORD

POWER SUPPLY ASSY A2

TB1

1   + 5V WHT (18 AWG)
    + 5V WHT (18 AWG)
2   GND BLK (18 AWG)
    GND BLK (18 AWG)
3   GND BLK
    + 15V RED
4   + 15V RED
    − 15V BRN
5   − 15V BRN
6
7
8   AC HOT
    AC HOT
9   AC NEUT
    AC NEUT

A1B1   FAN 1 2

WHT (18 AWG)
BLK (18 AWG)
W5

W4

A4W3

A4W2

A4W1

+ 12V (28 AWG)
+ 5V (28 AWG)
GND (28 AWG)
A4W1P1
GND (28 AWG)
A4W2P1
GND
CHASSIS GND

(22 AWG)
(22 AWG)   7 EIA CABLE ASSY 1   W2P1

W2

PWA HPR02/HPR01 A1A5

J3   8 15 16   J2   8   J1   1 6   W2P2

P2   KEYBOARD ASSY A3

P1

R P K E C B A J L   W4P1

J1   BOARD SLOT E

MOTHER BOARD A1A9

T2

11 4 3 2 1   W3P2

W3   W3P1

(28 AWG) −12V
(28 AWG) GND
(28 AWG) +5V
(28 AWG) GND
(28 AWG) +5V
J1

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

POWER DISTRIBUTION 1610/1620

FIRST USED NEXT ASSY 23743

SIZE D   DWG NO 23859
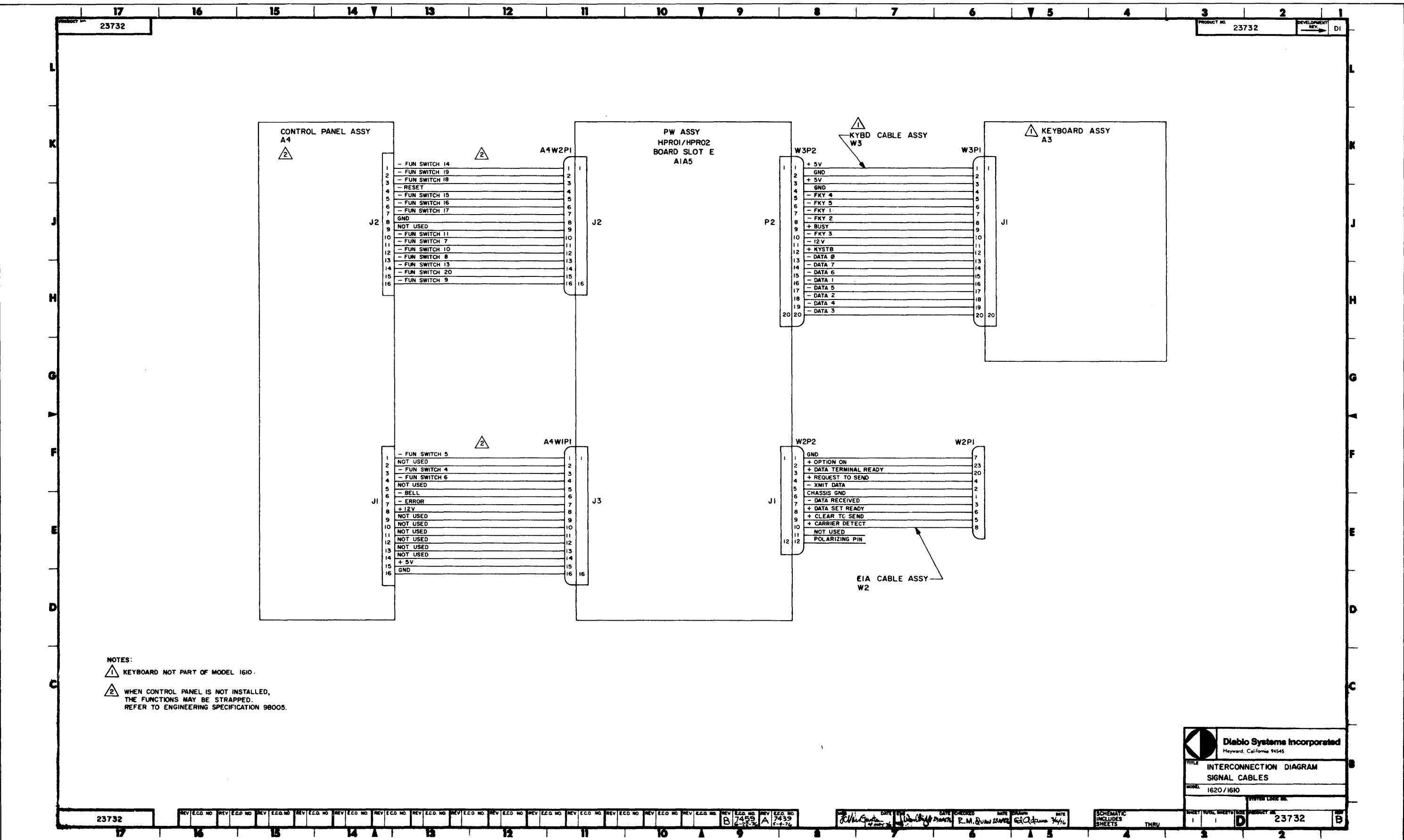
23859 Power Distribution

Rev. A   ECO 7439   As released.

       B   7459   Add Note 4 and alternate connections for machines without control panel.

       C   7501   Change S12 to S1 and remove from control panel assy. to phase in new control panel assy.

INTERCONNECTION DIAGRAM SIGNAL CABLES

PRODUCT NO. 23732

CONTROL PANEL ASSY
A4
⚠2

A4W2PI

1	– FUN SWITCH 14
2	– FUN SWITCH 19
3	– FUN SWITCH 18
4	– RESET
5	– FUN SWITCH 15
6	– FUN SWITCH 16
7	– FUN SWITCH 17
8	GND
9	NOT USED
10	– FUN SWITCH 11
11	– FUN SWITCH 7
12	– FUN SWITCH 10
13	– FUN SWITCH 8
14	– FUN SWITCH 13
15	– FUN SWITCH 20
16	– FUN SWITCH 9

J2   ⚠2   J2

PW ASSY
HPRO1/HPRO2
BOARD SLOT E
A1A5

⚠1 KYBD CABLE ASSY
W3

W3P2

1	+ 5V
2	GND
3	+ 5V
4	GND
5	– FKY 4
6	– FKY 5
7	– FKY 1
8	– FKY 2
9	+ BUSY
10	– FKY 3
11	– 12 V
12	+ KYSTB
13	– DATA 0
14	– DATA 7
15	– DATA 6
16	– DATA 1
17	– DATA 5
18	– DATA 2
19	– DATA 4
20	– DATA 3

P2   J1   W3PI

⚠1 KEYBOARD ASSY
A3

A4WIPI

1	– FUN SWITCH 5
2	NOT USED
3	– FUN SWITCH 4
4	– FUN SWITCH 6
5	NOT USED
6	– BELL
7	– ERROR
8	+ 12V
9	NOT USED
10	NOT USED
11	NOT USED
12	NOT USED
13	NOT USED
14	NOT USED
15	+ 5V
16	GND

J1   ⚠2   J3

W2P2

1	GND	7
2	+ OPTION ON	23
3	+ DATA TERMINAL READY	20
4	+ REQUEST TO SEND	4
5	– XMIT DATA	2
6	CHASSIS GND	1
7	– DATA RECEIVED	3
8	+ DATA SET READY	6
9	+ CLEAR TC SEND	5
10	+ CARRIER DETECT	8
11	NOT USED	
12	POLARIZING PIN	

J1   W2PI

EIA CABLE ASSY
W2

NOTES:

⚠1 KEYBOARD NOT PART OF MODEL 1610.

⚠2 WHEN CONTROL PANEL IS NOT INSTALLED,
THE FUNCTIONS MAY BE STRAPPED.
REFER TO ENGINEERING SPECIFICATION 98005.

| REV | E.C.O. NO | REV | E.C.O. NO |
| B | 7459 6-28-76 | A | 7439 5-4-76 |

CHECKED R.M. QUAN

SCHEMATIC INCLUDES SHEETS   THRU

SHEET 1 TOTAL SHEETS 1 SIZE D PRODUCT NO. 23732

**23732 Signal Interconnections**

Rev. A   ECO 7439   As released.

      B   7459   Add Note 2 for machines without control panel.

COMMENT SHEET

FROM

NAME _____ OFFICE/DEPT NO. _____

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To make this manual more useful to you, we want your comments: what additional information should be included in the manual; what description or figure could be clarified; what subject requires more explanation; what presentation is particularly helpful to you; and so forth.

How do you rate this manual: EXCELLENT_____ GOOD_____ FAIR_____ POOR_____

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