DIGI-DATA CORPORATION
8580 Dorsey Run Rd., Jessup, Md. 20794

NRZI FORMATTER
OPERATION MANUAL

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NOTE

This manual contains information for more than one configuration.

Units with a multiple card formatter should ignore pages 8-10 through 8-13.

Units with a single card formatter should ignore pages 8-3 through 8-8 and pages 8-15 through 8-17.

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LIST OF DRAWINGS

FORMATTER/TRANSPORT CONFIGURATION

CUSTOMER _____

FORMATTER _____

FORMATTER ADDRESS _____

TRANSMIT CRCC & LRCC _____

WRITE LAST WORD _____

DENSITY

LOW _____

HIGH _____

SPEED

LOW _____

HIGH _____

TRANSPORTS

	SERIAL #	HEAD	MODE	DENSITY	SPEED
SLT 0					
SLT 1					
SLT 2					
SLT 3					

PHYSICAL DESCRIPTION

Two versions of the NRZI FORMATTER are currently available.

The single board version, NFM, is a 15" x 17" PCB which is housed in the outrigger chassis. Fully loaded it contains 128 integrated circuits.

The multiple board version is comprised of three PCB s: NF, NFTB, and NFTC. NF is a 15-3/4" x 7-1/2" board which contains WRITE, READ, and CONTROL formatting electronics. Fully loaded, it contains 84 integrated circuits. No adjustments are required. NFTB is a 15-3/4" x 7-1/2" board which contains the formatter time base, the controller I/O interface, and a +5 VDC regulator (when mounted inside a tape unit chassis). SPEED and DENSITY options are programmed (jumpered platforms) on this board at time of manufacture. Fully loaded, this board contains 32 integrated circuits. One adjustment is provided: a 100 ohm variable resistor to adjust the output of the +5 VDC voltage regulator. NFTC is a 5-1/2" x 3" board which contains the driving and receiving interface required to control up to four OEM tape units.

While the single board version is always mounted in the outrigger chassis, the multiple board version may also be housed within the tape unit.

Three single-pole, double throw switches are located on the NFM/NFTB PCBs. S1, the CHECK CHARacter switch, allows the read clocks which identify the check character(s) to be transmitted from the FORMATTER to the controller in the ALLOW position; in the BLANK position, the CHECK CHARACTER CLOCKS are suppressed. S2, the FAD switch, has two positions (0 and 1) which determines the FORMATTER ADDRESS. S3, the LAST WORD switch, conditions the FORMATTER to accept the LWD command SYNCHRONOUSLY or ASYNCHRONOUSLY with respect to the WSTR.

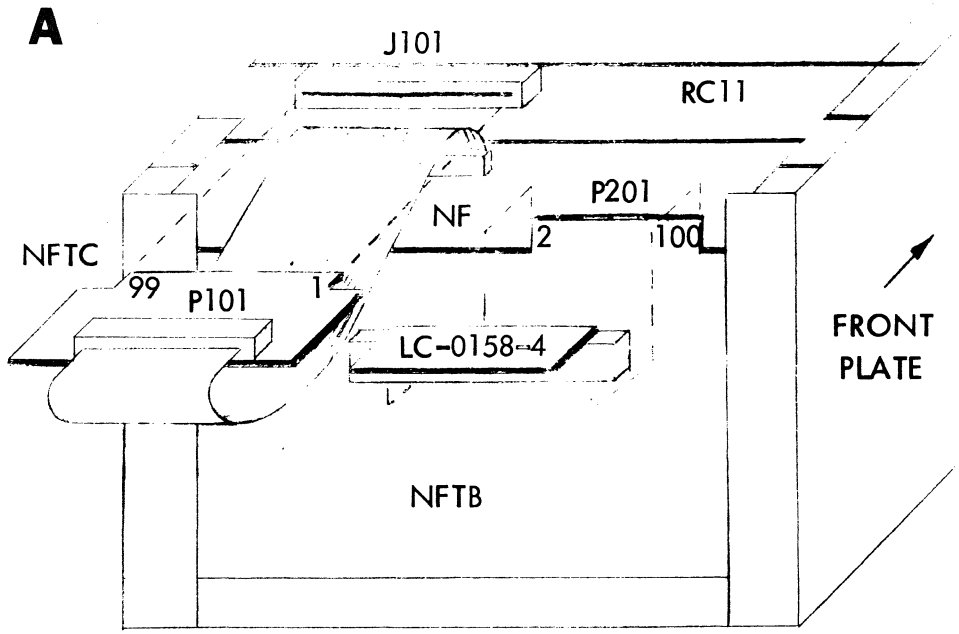
Although the single board and multiple board NRZI formatters are basically functionally equivalent, some differences do exist between their reference designations. The text contains the reference designations for the multiple board version. Summarized on the following page are the designation differences by page number.

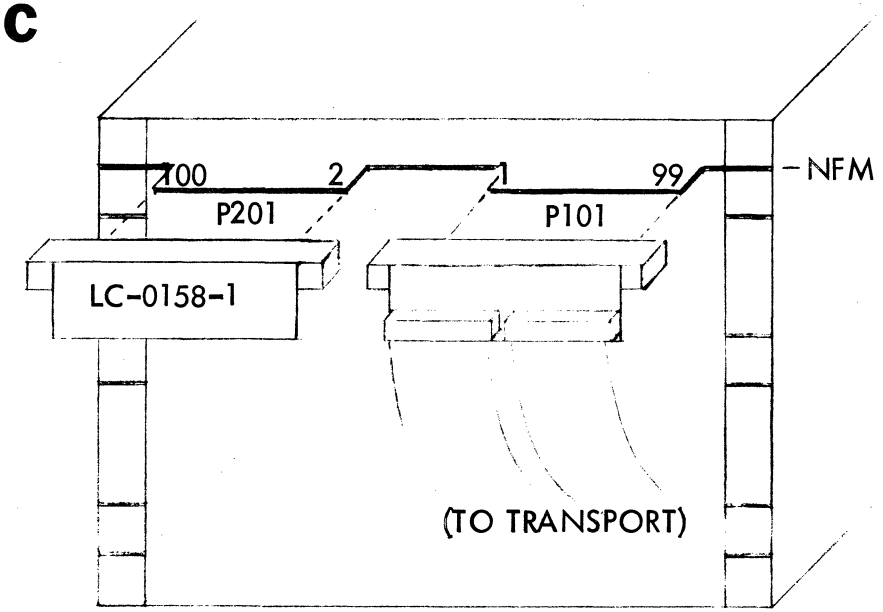
PAGE NUMBER	MULTIPLE BOARD	SINGLE BOARD
3-4	210-12	214-10
	210-2	214-8
	217	213
	221	210
	218-12	209-12
	222	212
	223	211
4-3	219	207
	220	218
	212	206
	208	204
4-4	208	204
5-4	211	205
	207	217
	208	204
	212	206
	220	218
5-5	206	201
5-7	208	204
	204	219
	224	220
	223	211
	201	221
	206	201
5-11	224	220

FIG. A: NRZI FORMATTER INSTALLED IN 1100/1600 TRANSPORT CHASSIS.

FIG. B: MULTIPLE-BOARD NRZI FORMATTER INSTALLED IN OUTRIGGER BOX.

FIG. C: SINGLE-BOARD NRZI FORMATTER INSTALLED IN OUTRIGGER BOX.





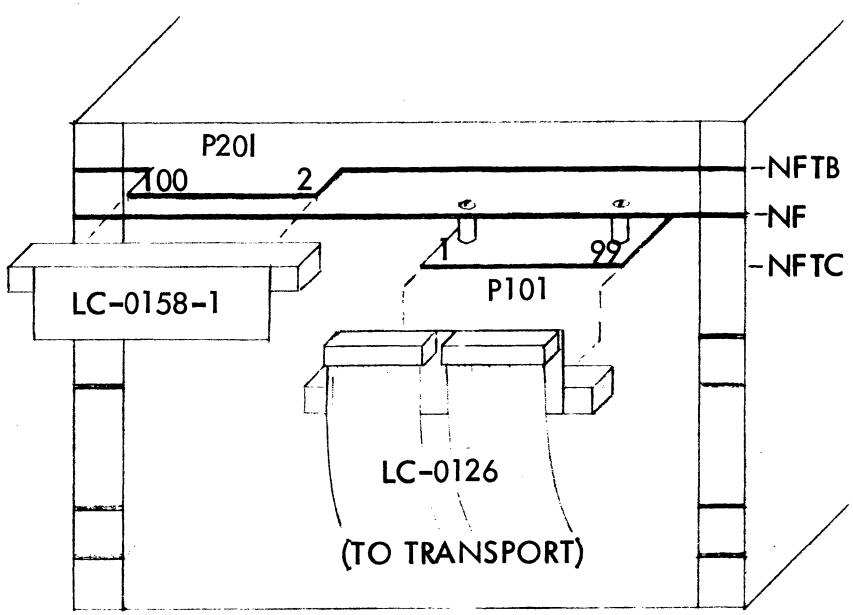
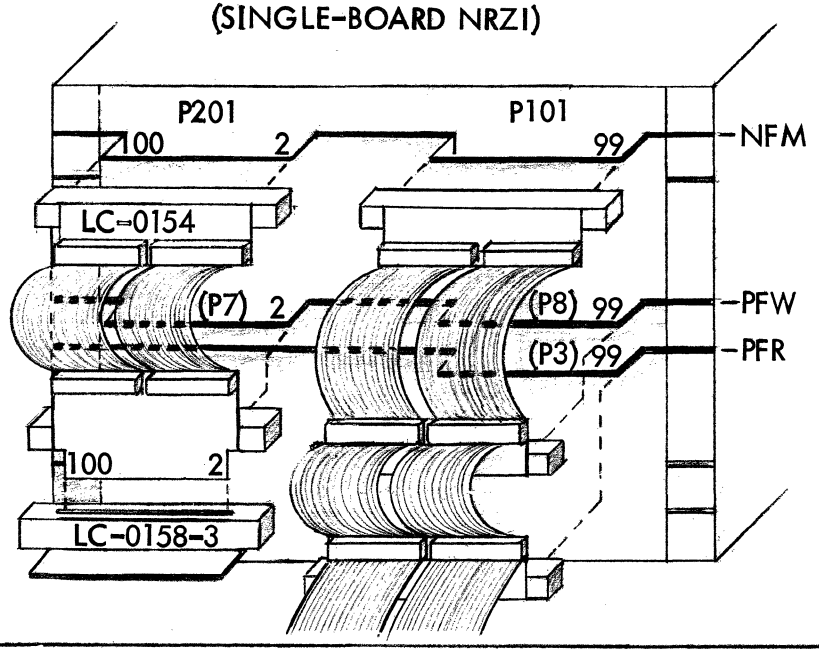


FIG 2-1

NRZI SINGLE-FORMATTER I/O CONFIGURATIONS	DIGI-DATA CORPORATION
	SHEET OF

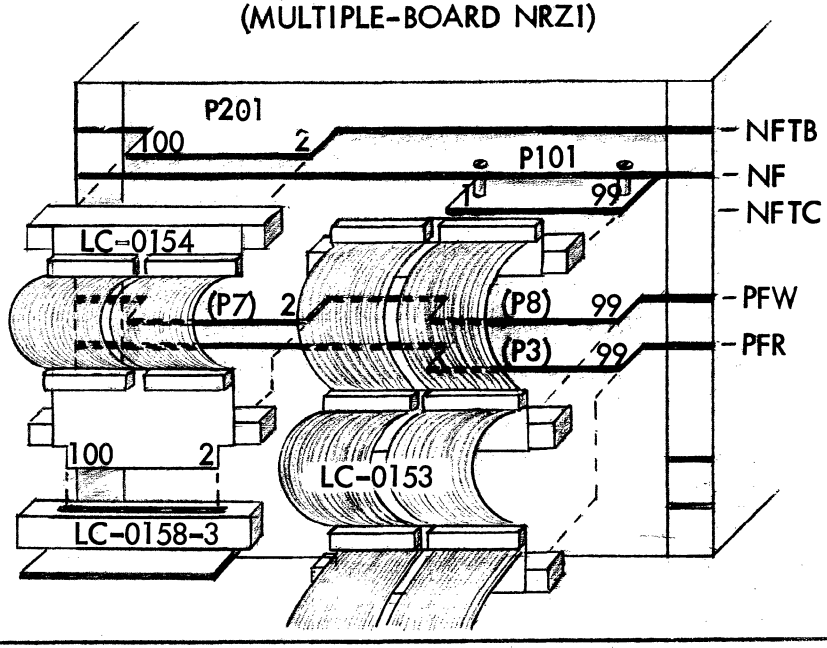
A

NRZI/PE DUAL FORMATTER
(SINGLE-BOARD NRZI)



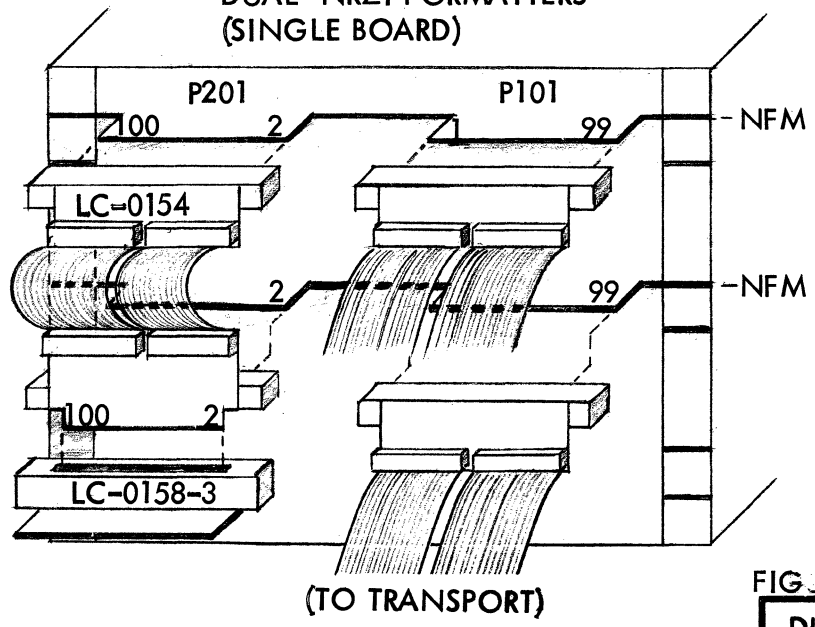
B

NRZI/PE DUAL FORMATTER
(MULTIPLE-BOARD NRZI)



C

DUAL NRZI FORMATTERS
(SINGLE BOARD)



D

DUAL NRZI FORMATTERS
(MULTIPLE-BOARD)

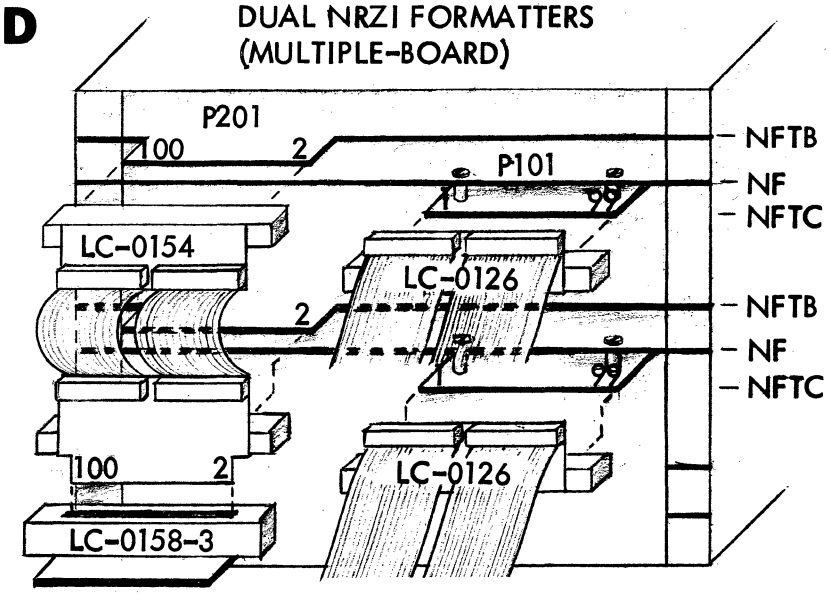


FIG 2-2

DUAL-NRZI AND NRZI/PE FORMATTER I/O CONFIGURATIONS	DIGI-DATA CORPORATION
	SHEET OF

THEORY OF OPERATION
COMMON ELECTRONICS

BLOCK DIAGRAM DESCRIPTION

Referring to the formatter block diagram (DWG. NO. LC-0119) at the end of the manual, COMMAND lines from the CONTROLLER are latched at GO time and applied to the selected transport's I/O, provided the FORMATTER is enabled (FEN) and addressed (FAD). The MODE/MOTION CONTROL circuitry is activated and a PRE-RECORD delay is generated.

The WRITE CONTROL logic is activated whenever an operation requiring WRITE current has been commanded. WSTR clocks data from the CONTROLLER into the WRITE DATA circuits; concurrently, the CRCC register is clocked (9T); subsequently, WDS outputs the data to the transport I/O. The CONTROLLER signals the end of the data block with the assertion of LWD. The WRITE CONTROL electronics transmits the check characters to the transport I/O and signals the MODE/MOTION CONTROL to commence the POST-RECORD and DECELERATION delays.

The READ CONTROL electronics is enabled when reading or while writing with a dual stack head. The transport's READ DATA lines are latched and the vertical and longitudinal parity is checked. While the data portion of the record is always transmitted to the controller, the check characters may be suppressed while reading forward. Recognition circuits provide a status output, FMK, when FILE MARKS are read.

TAPE SPEED CLOCK (Refer to FIG 3-1)

The formatter time base is derived from a medium speed gated oscillator circuit. An 8.640 MHz astable clock drives a 5 bit counter which is preset by the high speed/ low speed decoders. Only one decoder is enabled at a time and is dependent upon the selected tape drive's speed identification. The output of the counter is applied to a pulse-stretching network which provides a normalized output frequency of 38, 400 PULSES/IN.

The high speed/low speed decoders are programmed with jumpers as follows: (1 = jumper)

TAPE DRIVE SPEED	DECODER INPUTS	TAPE SPEED CLK
(IPS)	16 8 4 2 1	(MHZ)
12.5	1 / / / 1	.480
18.75	/ 1 / 1 1	.720
25	/ 1 / / /	.960
37.5	/ / 1 / 1	1.44
45	/ / 1 / /	1.728
75	/ / / 1 /	2.88

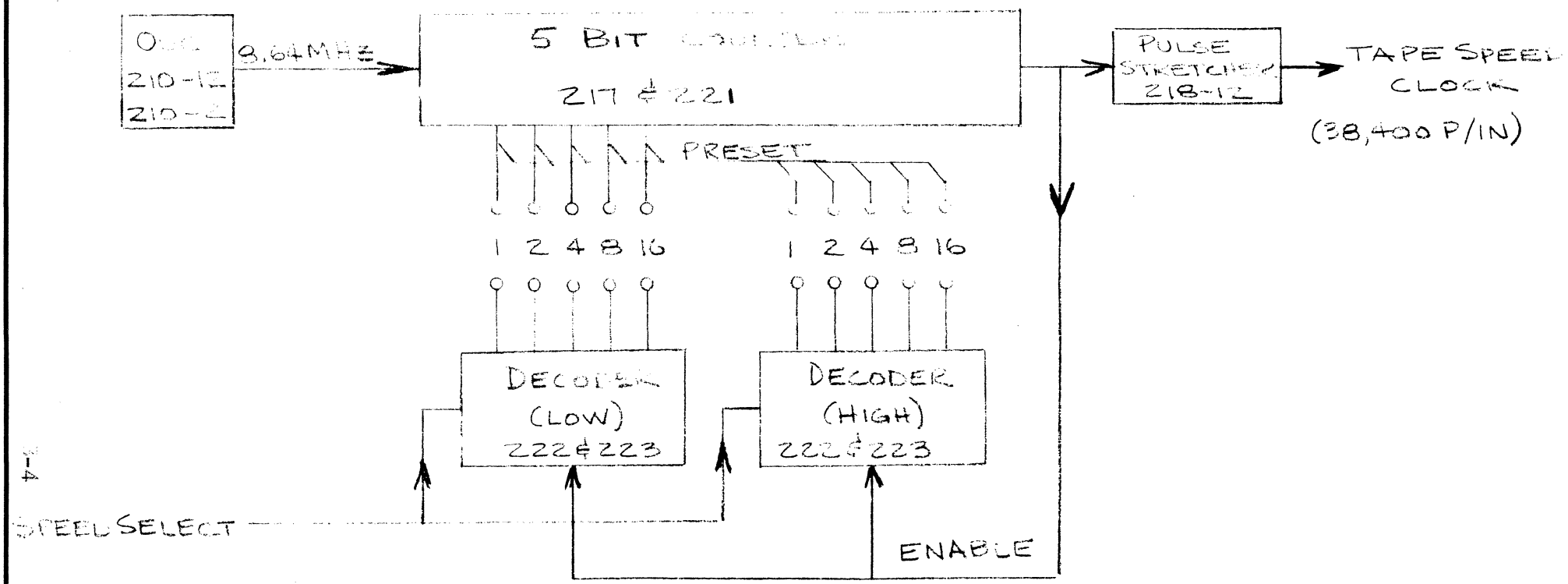


FIG 3-1

A	CIRCUIT CHANGE JJ 9-20-72

DIGI-DATA CORPORATION

SHEET OF

MOTION/MODE CONTROL (Refer to FIGS 3-2 and 3-3)

Interface GO commands are gated then latched by the FGO flip-flop provided that:

A.) The formatter is not busy; or

B.) The stay-at-speed window is true.

Each gated GO command samples nine control lines and copies this information into a nine bit latch. The latch retains this information until the next GO command is accepted. Coincident with the trailing edge of GO, FBY is set true.

DELAYED FGO is synthesized by subjecting FGO to two DC delays which displace its leading and trailing edges 3 μs and 250 μs respectively from the edges of FGO.

While FGO is true and DELAYED FGO is false, the latch presents five information bits to the tape deck to condition it for the forthcoming operation. The sixth bit, REV/FWD, is gated by DELAYED FGO which starts the tape in motion and initiates the pre-record delay.

When the tape has reached synchronous speed (80% of synchronous speed for read operations), and the pre-record delay is completed, DBY is set true.

Tape motion will continue until:

A.) (WRITE ONLY) A record is written or an erase operation is completed; or

B.) (READ ONLY OR READ AFTER WRITE) A record has passed the read head or an erase operation is completed.

Subsequent to A or B above, a post-record delay is generated. Completion of the post-record delay will clear DBY and FGO.

FGO false and DELAYED FGO true is gated to generate a 250 μs stay-at-speed window. Receipt of a GO command during this window will set FGO true and the tape will stay at synchronous speed.

If a GO command is not received during this window , the tape will begin to decelerate after the trailing edge of DELAYED FGO. When tape motion has ceased, FBY will go false.

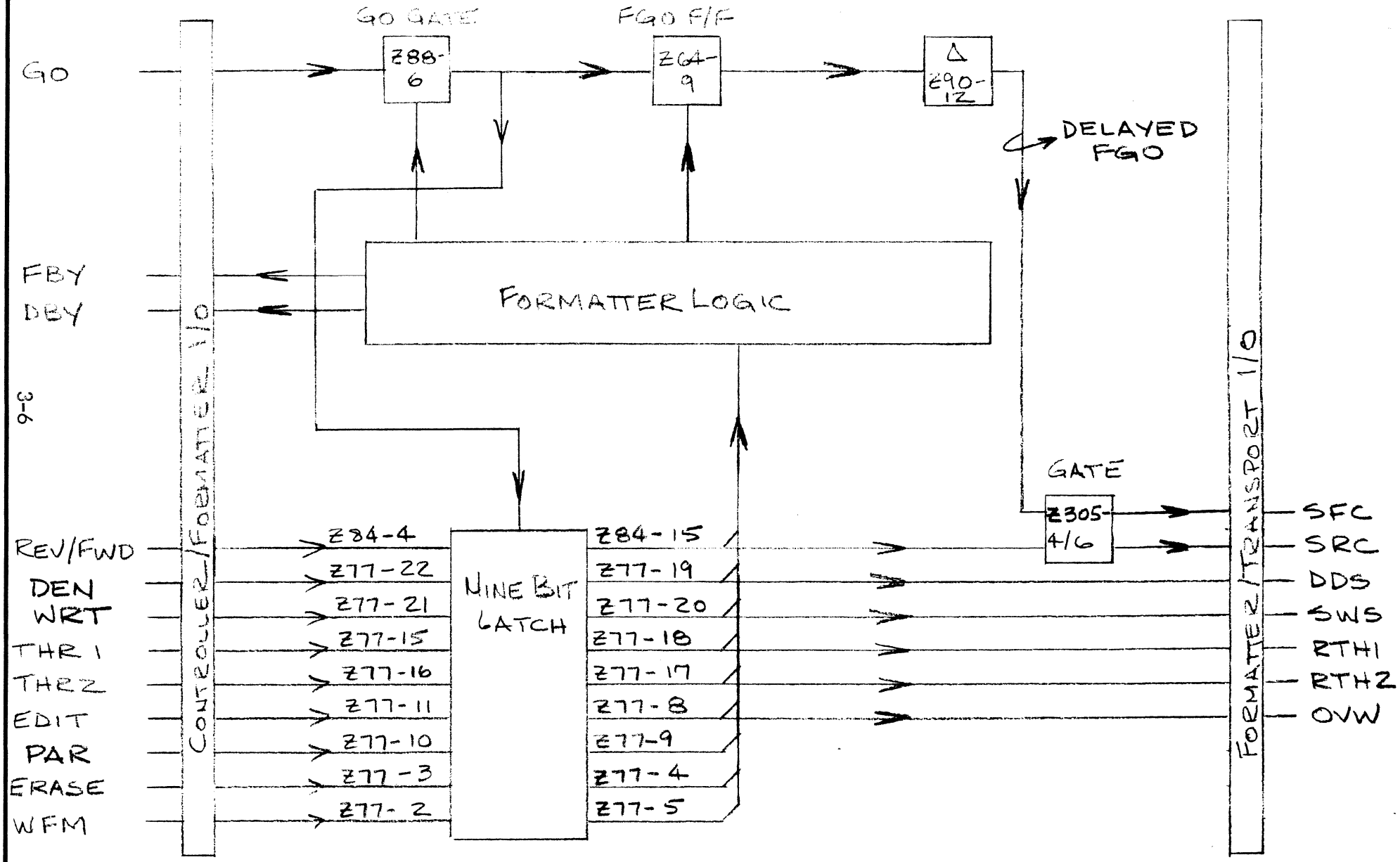


FIG 3-2

A	REF DES CHANGED JJ 9-20-72
BLOCK DIAGRAM MOTION/MODE CONTROL JJ 12-27-71	DIGI-DATA CORPORATION
	SHEET OF

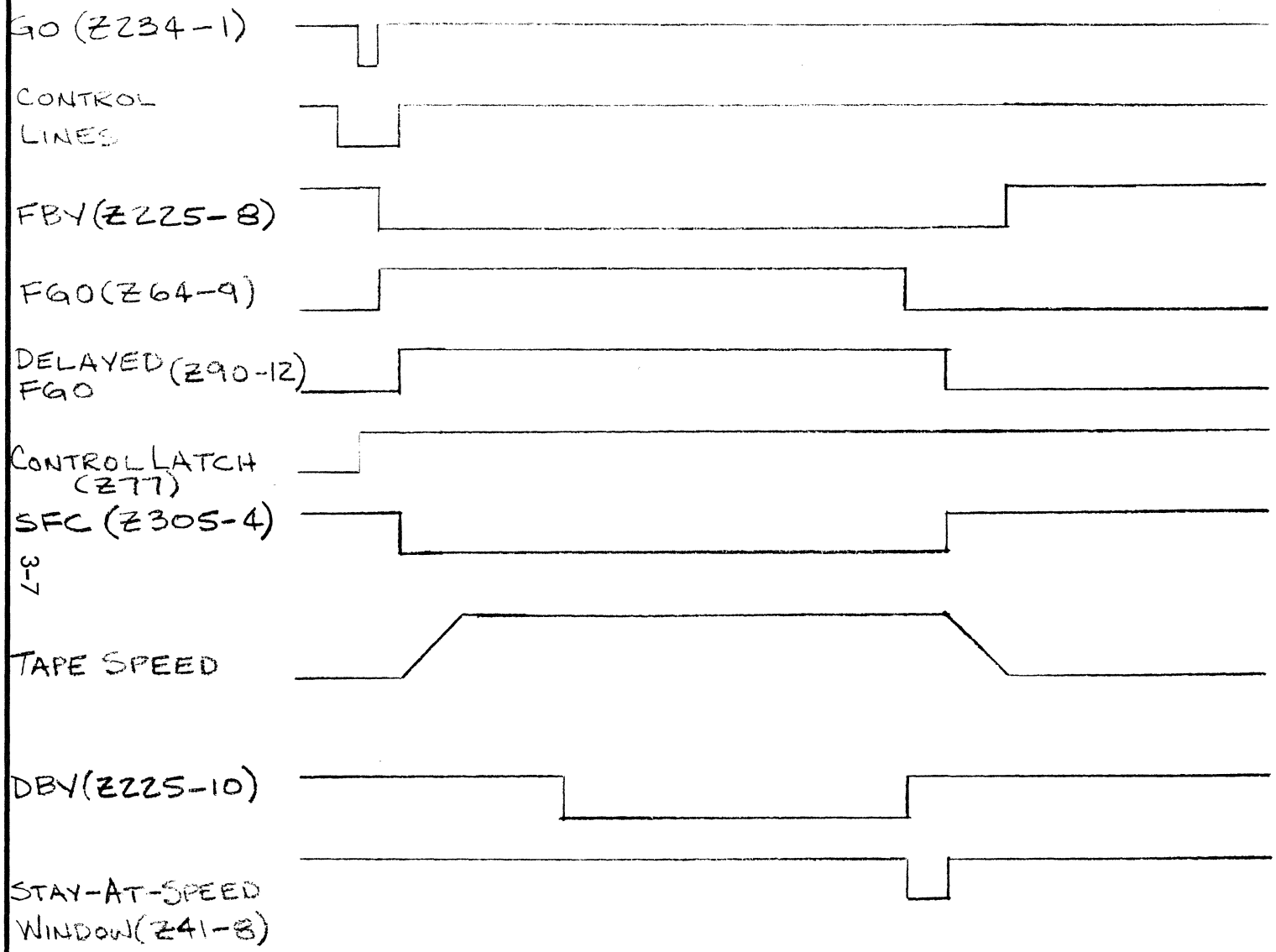


FIG 3-3

A	REF DES CHANGED JJ 9-20-72
TIMING DIAGRAM MOTION/MODE CONTROL JJ 12-27-71	DIGI-DATA CORPORATION
	SHEET OF

PRE-RECORD DELAY

DELAYED FGO true and AS (At speed) false gate TAPE SPEED CLOCKS to a twenty-bit resettable counter. When the count is reached for the selected pre-record delay, AS flip-flop is set, DBY (data busy) goes true, and the 20-bit counter is cleared (Refer to Table 3-1).

POST-RECORD DELAY

F DATA COMPLETE flip-flop will set when any of the following conditions exist:

SINGLE GAP HEAD

A.) END CC WRITE true

B.) DATA ABSENT true

DUAL GAP HEAD

A.) END CC WRITE and FERASE true

B.) DATA ABSENT true

FDATA COMPLETE true gates TAPE SPEED CLOCKS to the 20-bit resettable counter. When the count is reached for the selected post-record delay, STOP TAPE is generated which resets the AS and FDATA COMPLETE flip-flops, clearing the 20-bit counter; DBY goes false (Refer to Table 3-1).

In addition, STOP TAPE clears the FGO flip-flop. FGO false and FBY (Formatter Busy) true gates TAPE SPEED CLOCKS to the 20-bit counter. When the selected count is reached (tape motion has ceased), the FBY flip-flop will be reset, clearing the 20-bit counter.

PRE-RECORD DELAYS

COMMAND	Distance In.	TAPE SPEED - IPS.					
		12.5	18.75	25	37.5	45	75
		DELAY-MS					
READ NORMAL	.147	23.5	15.7	11.7	7.85	6.55	3.92
READ FROM BOT	1.68	150	100	75	50	41.6	25
WRITE 9T (Single Gap)	.37	45	29.9	22.5	14.9	12.4	7.5
WRITE 7T (Single Gap)	.505	56	37.4	28	18.7	15.5	9.35
WRITE FROM BOT	6.66	550	367	275	184	153	92
WRITE EOF	6.66	550	367	275	184	153	92
WRITE 9T (Dual Gap)	.24	34	22.7	17	11.3	9.5	5.65
WRITE 7T (Dual Gap)	.21	32	21.4	16	10.7	8.9	5.35
DATA RATE (KHZ)		10	15	20	30	36	60
DECELERATION DELAY (MS)		36	23.8	18	12	10	6

POST-RECORD DELAYS

COMMAND	Distance In.	TAPE SPEED-IPS.					
		12.5	18.75	25	37.5	45	75
		DELAY-MS					
WRITE FWD	.093	7.4	4.95	3.7	2.48	2	1.23
READ FWD	---	---	---	---	---	---	---
READ REV 9 T	.093	7.4	4.95	3.7	2.48	2	1.23
READ REV 7 T	.213	16.8	11.2	8.4	5.6	4.66	2.8
READ REV 9 T (Edit)	.174	14	9.35	7	4.66	3.9	2.34
READ REV 7T (Edit)	.268	22	14.7	11	7.35	6.1	3.67

TABLE 3-1

DIGI-DATA CORPORATION

PRE/POST RECORD DELAYS-NRZI FORM.

SHEET OF

5/14/73

FORMATTER ADDRESS AND ENABLE

After power-up clearing is performed, FORMATTER UP will be true only if the formatter is enabled and addressed.

FAD (formatter address), exhibits the following address table:

FAD SWITCH POSITION	LOGICAL INPUT
0	False
1	True

The formatter may be cleared at the customer interface by either:

A.) Disabling FEN (false level)

B.) Not addressing FAD per the preceding address table.

The formatter address is determined by the position (0 or 1) of a single pole, double throw switch (S2) located on either the NFM or NFTB PCB (single/multiple board formatter).

When the NRZI FORMATTER is coupled with a PE FORMATTER (9T, DUAL DENSITY CONFIGURATIONS), the NRZI FORMATTER is normally addressed as FAD 0 while the PE FORMATTER is FAD 1.

TRANSPORT ADDRESSES

When the formatter is addressed, customer SELECT lines are converted to decimal form and applied to the tape drive according to the following truth-table:

CUSTOMER		TAPE DRIVE			
TAD 0	TAD 1	SLT 0	SLT 1	SLT 2	SLT 3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

TRANSPORT CONFIGURATION AND STATUS LINES

Whenever a tape deck is selected, its configuration and status lines will ripple through the formatter and be buffered and applied to the customer I/O.

TAPE DECK CONFIGURATION LINE	TRUE WHEN TAPE DECK IS
SPEED	LOW SPEED UNIT
SINGLE	SINGLE GAP UNIT
NRZ1	NRZI UNIT
7 TR	7T UNIT

TAPE DECK STATUS LINE	TRUE WHEN TAPE DECK IS
RDY	See INTERFACE and
EOT	APPLICATION SUMMARY
LPT	
FPT	
RWD	
ONL	
DEN STAT	

In addition, when a tape deck is selected, and placed ON LINE, customer REWIND and OFF LINE commands may be asynchronously activated. These commands are routed directly to the transport and do not cause the FORMATTER to become BUSY.

ZERO TO TEN CONVERTER

When a seven track tape drive is selected, PAR is true, and customer WRITE DATA = 00_8, the formatter will present WRITE DATA = 12_8 to the tape drive.

PARITY GENERATION AND CHECKING

Whenever the selected drive is a nine track unit, the formatter will always write odd parity characters. When reading, the formatter will check for odd parity characters. In the event that a parity error is detected, the ERROR status line will go true just prior to the CUSTOMER READ STROBE associated with the character in error. The ERROR line will stay true for approximately one character period, enveloping the associated READ STROBE.

When a seven track drive is selected, the formatter will generate/check parity a s commanded by the customer PAR line. With the line true, EVEN PARITY will be generated/checked.

DENSITY SELECT & DENSITY STATUS

The customer DEN input is utilized when:

A.) Selecting a dual-density tape deck; or

B.) Selecting a tape deck in a multi-tape deck configuration with at least two drives of different density.

DEN ripples through the formatter and is applied to the selected drive. The selected drive will then identify the density ((HIGH/LOW) at which it is operating. The recorder status line (DDI) conditions the formatter density circuits and is then buffered and applied to the customer I/O.

Whenever the selected Tape Unit is 9 track, the NRZI FORMATTER will operate at 800 BPI regardless of the state of DEN.

Whenever the NRZI FORMATTER is daisy-chained with a PHASE-ENCODED FORMATTER to drive 9T DUAL DENSITY TAPE UNITS, DEN must be set true when the NRZI FORMATTER is addressed. Failure to do this will result in a format mismatch between the FORMATTER and TAPE UNIT.

Density options are programmed on wired platforms on either the NFM or NFTB PCB at time of manufacture (single/multiple board formatter). Refer to page 8-2.

+5 VDC POWER SUPPLY

When the formatter is configured inside the chassis of a tape drive, it is powered by a supply mounted on the TIME BASE board (NFTB).

The supply is a series voltage regulator which provides an output current of 2.5A at 5.0 VDC. RAW DC, full-wave rectified and filtered AC, is provided to the input of the regulator by the associated tape drive. The output of the supply is resistively sampled and applied to a differential amplifier referenced to the tape drive +5 VDC. The output of the amplifier is applied to a Beta multiplier which drives the series regulator. A 100 Ω variable resistor is provided in the sampling network to permit the output voltage to be adjusted to 5.0 VDC.

Current limiting is provided by sampling the output current via a .1 Ω resistor in the load circuit. Under excessive load current, the current supplied by the differential amplifier is diverted from the Beta multiplier to the collector of Q3.

When the formatter is housed within the outrigger chassis, it is powered by a similar regulator on the RDC-03 PCB adjacent to the front panel.

THEORY OF OPERATION
WRITE ELECTRONICS

WRITE OPERATION

3X WRITE CLOCK (Refer to FIGS 4-1 and 4-2)

The TAPE SPEED CLOCK is applied to a resettable 6 BIT counter. For 200/800 BPI operation the 3X WRITE CLOCK is generated by dividing the TAPE SPEED CLOCK by 64/16. For 556 BPI tapes, the selected decoder detects a count of 22 and clears the 3X WRITE CLOCK flip-flop. The flip-flop in turn clears the counter. The next TAPE SPEED CLOCK pulse sets the flip-flop enabling the counter. Hence, one 3X WRITE CLOCK is generated for every twenty-three TAPE SPEED CLOCKS.

WRITE FORWARD (Refer to FIG 4-3)

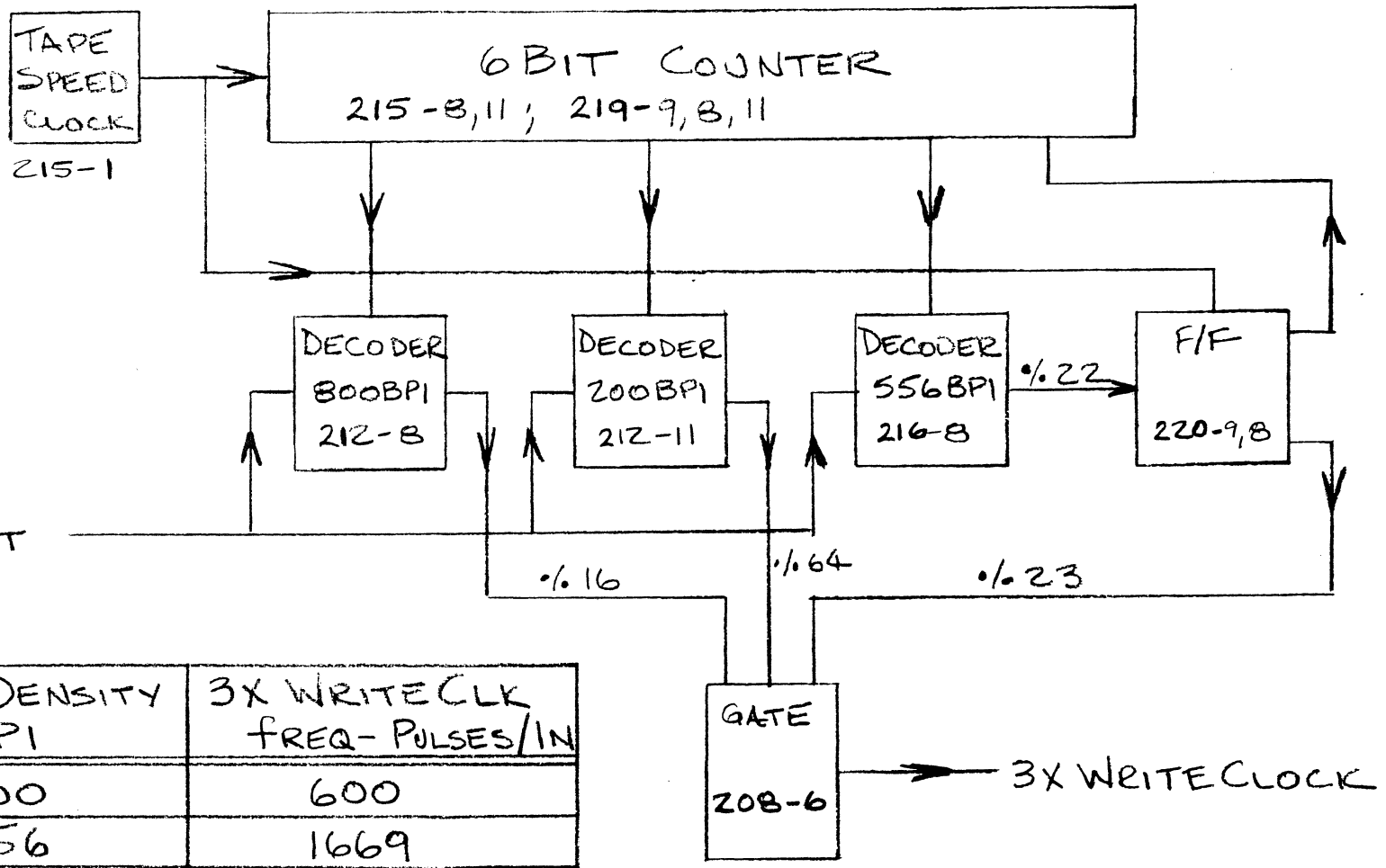
The 3X WRITE CLOCK is applied to a resettable 2 BIT counter. The counter is enabled 6 μs after the appropriate pre-record delay has been completed and stays enabled until the LRCC has been commanded. WRITE T1, 1/3 character period in width, is generated by detecting the 1-$\emptyset$ state of the counter. WRITE T1 is applied to a DC delay whose output is inverted and gated with WRITE T1 to generate3 μs WRITE T1 PULSES coincident with the leading edge of WRITE T1.

CUSTOMER WRITE STROBE and CLOCK CR are generated by gating WRITE T1 and the PLC flip-flop (past last character) when not writing EOFs. The PLC flip-flop will be set on the first true-false transition of WRITE T1 subsequent to activation of the LAST WORD customer input. The PLC flip-flop is reset after the completion of the post-record delay (AS false).

GATE WRITE DATA, utilized to enable customer DATA lines to be presented to the drive I/O, goes true after the pre-record delay is complete and returns to the false state after the PLC flip-flop has been set, provided that an erase/write EOF operation is not being performed.

For each CUSTOMER WRITE STROBE there is a corresponding WRITE DATA STROBE (generated by gating WRITE T1 PULSE) when an erase operation is not being performed.

On the leading edge of WRITE T1 (leading edge of CUSTOMER WRITE STROBE), the customer DATA lines are copied into the CR register. Hence, the DATA lines must be stable prior to the leading edge of CUSTOMER WRITE STROBE.



TAPE DENSITY BPI	3X WRITE CLK FREQ - PULSES/IN
200	600
556	1669
800	2400

FIG 4-1

A	REF DES. CHANGE JJ1 9-21-72
BLOCK DIAGRAM - 3X WRITE CLOCK	DIGI-DATA CORPORATION
JJ1 12-27-71	SHEET OF

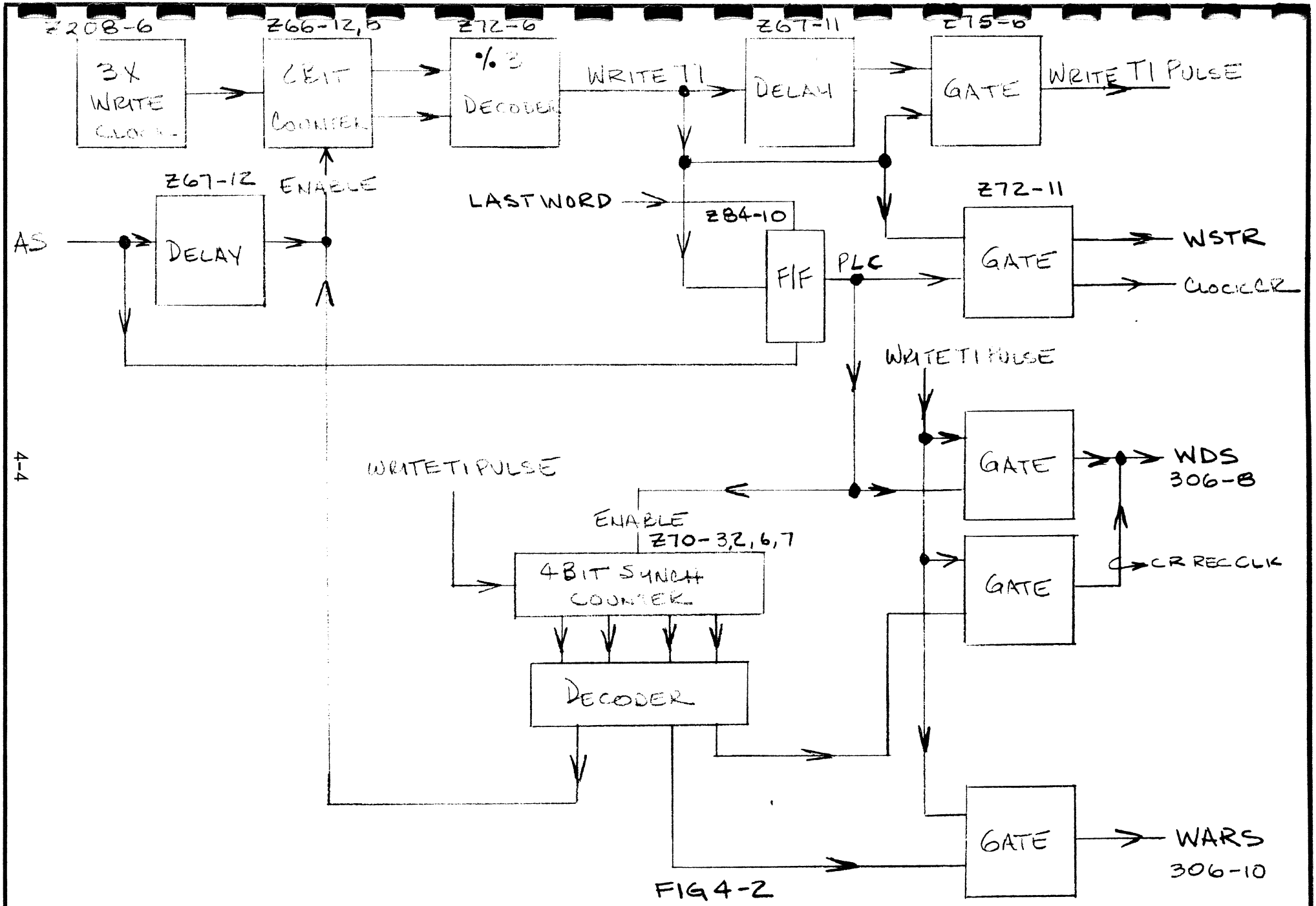
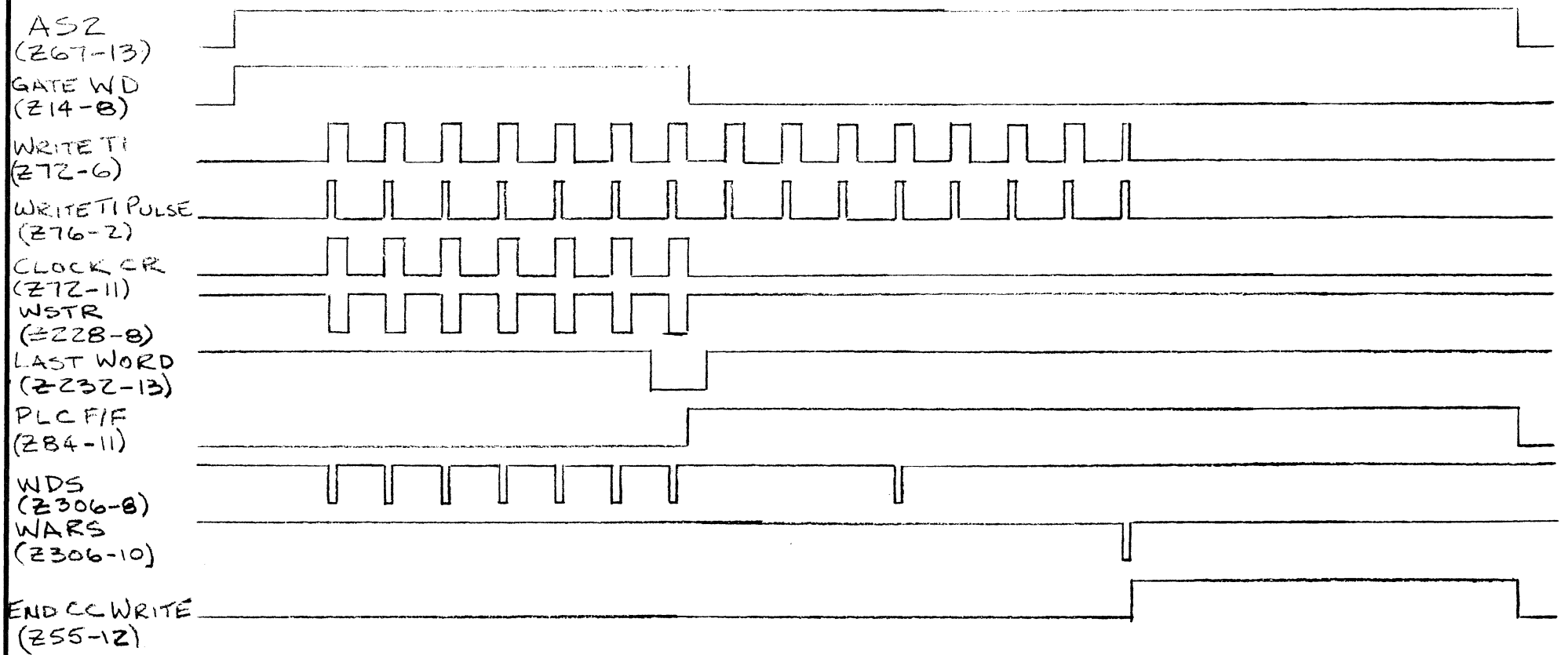


FIG 4-2

4-4

A	REF DES. CHANGE JJ 9-21-72	BLOCK DIAGRAM — WRITE FWD OPERATION JJ 1-12-72	DIGI-DATA CORPORATION SHEET OF



CUSTOMER WRITE CLK FREQ - KC

TAPE DENSITY BPI	TAPE SPEED IPS					
	12.5	18.75	25	37.5	45	75
200	2.5	3.75	5	7.5	9	15
556	6.95	10.4	13.9	20.9	25	41.8
800	10	15	20	30	36	60

FIG 4-3

A	REF DES. CHANGE JJ1 9-21-72
TIMING DIAGRAM - WRITE FWD OPERATION	DIGI-DATA CORPORATION
JJ1 12-27-71	SHEET OF

WRITE OPERATION (Cont.)

The write head current reversal occurs on the trailing edge of WRITE T1 PULSE (occurs while CUSTOMER WRITE STROBE is true). Hence, the trailing edge of CUSTOMER WRITE STROBE is ideally suited to be employed as a benchmark for the initiation of DATA line changes. In summary, DATA lines should be stable prior to and during CUSTOMER WRITE STROBE.

When PLC is set true, a synchronous 4 bit counter is enabled to count WRITE T1 PULSES.

During the interval between the counts of two and eight, the character contained in the CR register is presented to the drive I/O. (GATE CR true). The corresponding WRITE DATA STROBE is generated by gating WRITE T1 PULSE during the interval between the counts of three and four (non-erase/7T/EOF operation).

WARS is generated by gating WRITE T1 PULSE during the interval between the counts of seven and eight (9T) or three and four (7T) (non-erase operations).

After the count of eight is reached, END CC WRITE goes true and disables the 3X WRITE CLOCK counter. After the appropriate post-record delay is completed, the PLC flip-flop and the 4 bit synchronous counter are cleared.

VARIABLE LENGTH ERASE

VARIABLE LENGTH ERASE operations are performed in a manner similar to WRITE FORWARD operations. CUSTOMER WRITE STROBE is generated as normal. LAST WORD will be set true when it is desired to terminate a VARIABLE LENGTH ERASE operation. F ERASE inhibits the generation of WRITE DATA STROBE and WARS thereby DC erasing the tape in the direction of the inter-record gap.

WRITE EOF (Refer to FIG 4-4)

During the appropriate pre-record delay, the synchronous 4 bit counter is preset to the count of fifteen. CUSTOMER WRITE STROBE, CLOCK CR, and GATE WRITE DATA are inhibited while the 4 bit counter is enabled.

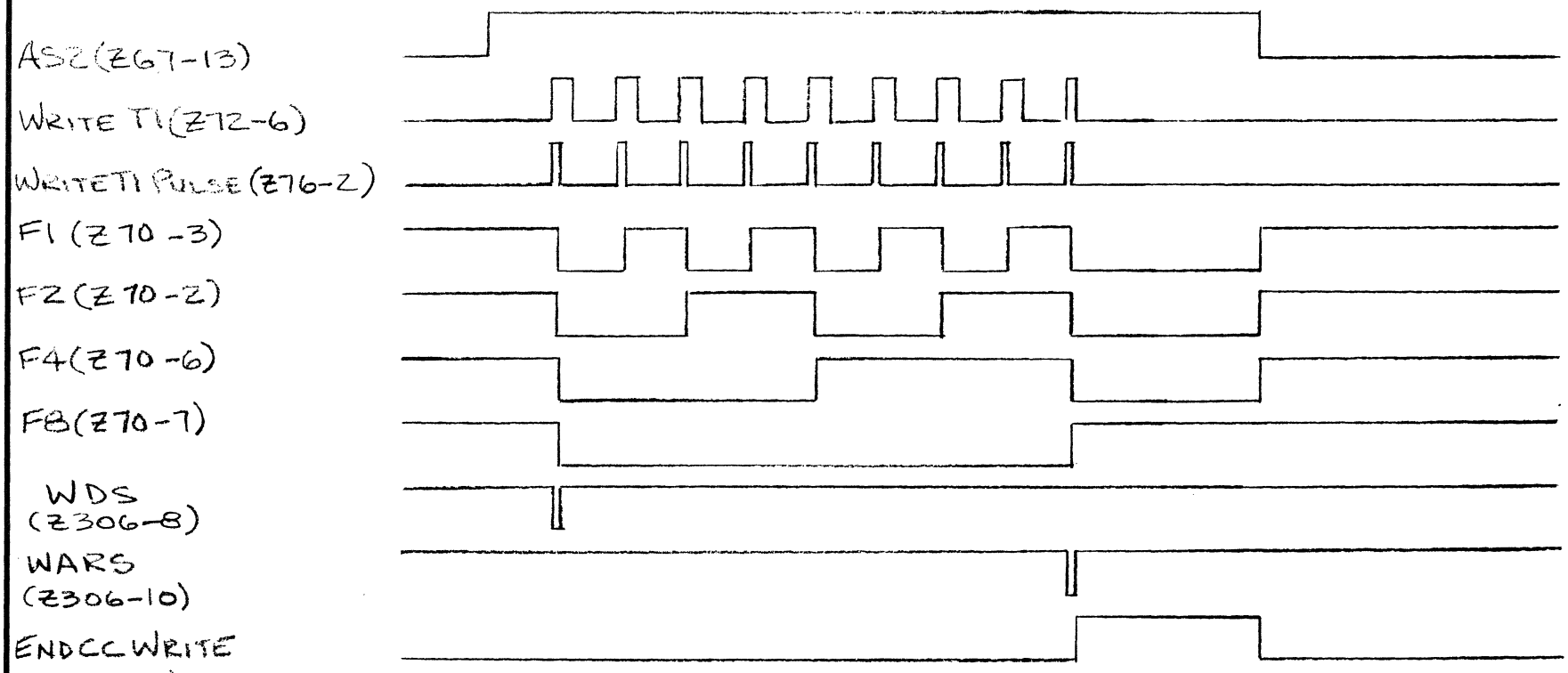


FIG 4-4

A	REF DES. CHANGE JJ1 9-21-72	
TIMING DIAGRAM — WRITE EOF OPERATION (9T)		DIGI-DATA CORPORATION
JJ1 12-27-71		SHEET OF

GATE 7/9 FILE is true for the entire operation (transmitting the appropriate EOF character to the drive I/O). WRITE DATA STROBE is generated by gating WRITE T1 PULSE with the count of fifteen. The WRITE DATA STROBE associated with the CR is suppressed while WARS and the completion of the operation are performed as during a normal WRITE FORWARD operation.

FIXED LENGTH ERASE

This operation is performed identically as a WRITE FILE MARK operation except that WRITE DATA STROBE and WARS are suppressed.

EXTERNAL PARITY GENERATION (Refer to FIG 4-5)

When performing WRITE DATA transfers, it may be desirable to generate parity external to the formatter. Two formatter inputs are employed to accomplish this:

A. GATE WRITE DATA P/C

This input must be held true for the duration of the write transfer. Normally, it is set true prior to the transmission of the GO command which initiates the transfer and remains true until the trailing edge of DBY.

B. WRITE PARITY

With GATE WRITE DATA P/C true, WRITE PARITY is switched to the WRITE DATA PARITY track input. This input should be switched as a normal DATA input; i.e., the line must be stable prior to, during, and just after each WRITE STROBE.

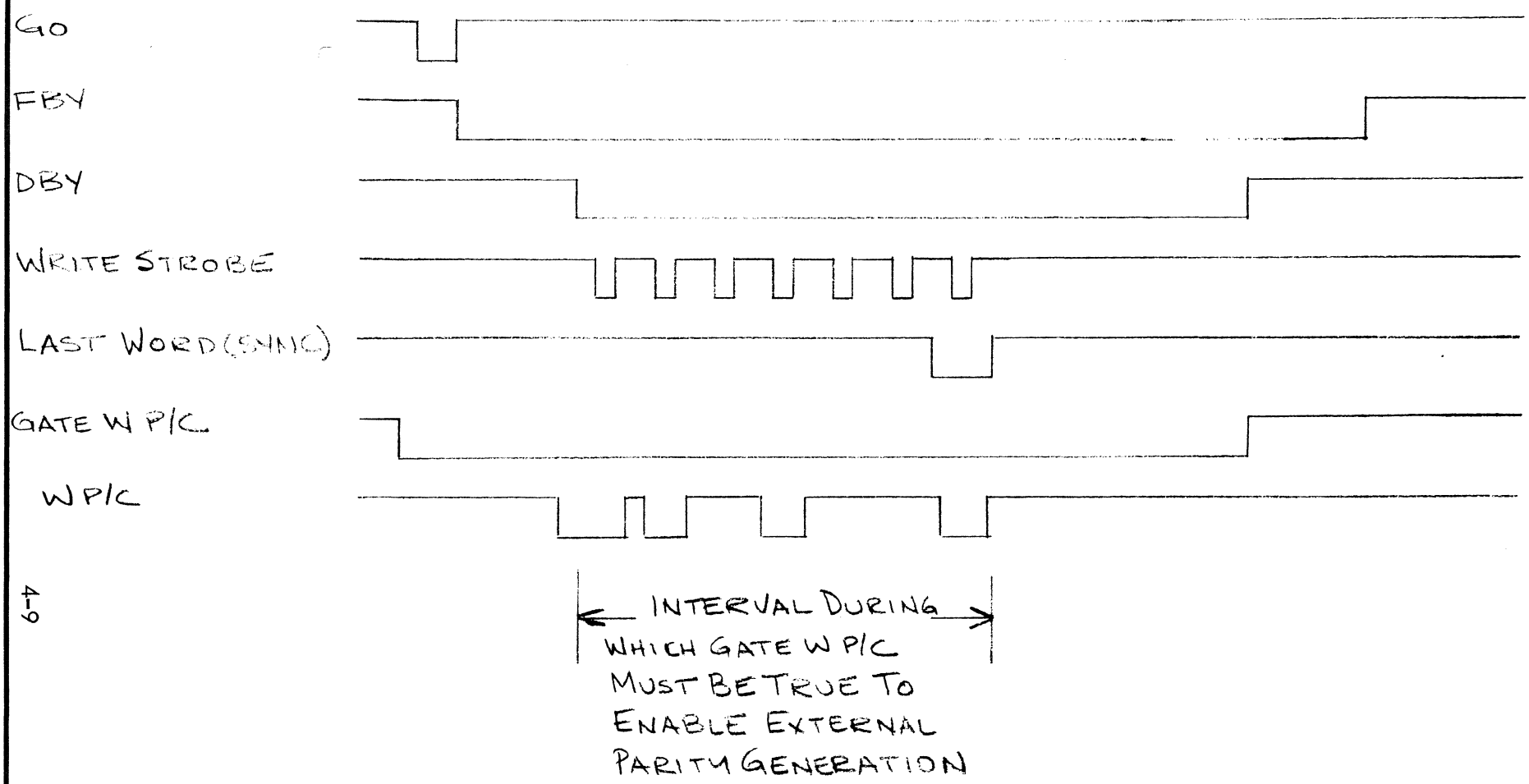


FIG 4-5

TIMING DIAGRAM – EXT PARITY GENERATION	DIGI-DATA CORPORATION
JJ1 1-12-72	SHEET OF

THEORY OF OPERATION
READ ELECTRONICS

READ DATA (Refer to FIG 5-1)

READ DATA STROBE is applied to a DC delay, inverted, and gated with READ DATA STROBE to generate 800 NS READ CLOCK PULSES coincident with the leading edge of READ DATA STROBE. READ DATA LINES are gated by READ DATA STROBE and are utilized to preset a nine-bit latch. READ CLOCK PULSE is utilized to clear the nine-bit latch. The nine-bit read register outputs are buffered and presented to the customer I/O.

3X READ CLOCK (Refer to FIG 5-2)

Prior to the completion of the pre-record delay, AS2 holds a flip-flop (Z75-3, 11) cleared. The output of the flip-flop is gated with/READ CLOCK PULSE via a 5 μs DC delay to form/READ CLOCK DISABLE. Hence, READ CLOCK DISABLE will go false 5 μs after the trailing edge of each READ CLOCK PULSE subsequent to the completion of the pre-record delay and will stay false until the leading edge of a subsequent READ CLOCK PULSE.

With READ CLOCK DISABLE false, a 6-Bit resettable counter is enabled to count TAPE SPEED CLOCKS. For 200/800 BPI operation, the 3X READ CLOCK is generated by dividing the TAPE SPEED CLOCK by 64/16. For 556 BPI tapes, the selected decoder detects a count of 22 and clears the 3X READ CLOCK flip-flop. The flip-flop in turn clears the counter. The next TAPE SPEED CLOCK pulse sets the flip-flop enabling the counter. Hence, one 3X READ CLOCK is generated for every twenty-three TAPE SPEED CLOCKS (556 BPI tapes).

READ FORWARD/REVERSE OPERATION (Refer to FIGS 5-3 and 5-4)

3X READ CLOCKS are applied to a 2 Bit counter which is cleared by READ CLOCK DISABLE. The counter, when enabled, is gated to output the progression Ø-1-2-3-1-2-3..... The counter will be in the Ø state for the duration of each READ DATA STROBE and remain in that state for 5 μs after the trailing edge of said clock (READ CLOCK DISABLE). The counter will then begin to advance and continue to count until the next READ DATA STROBE.

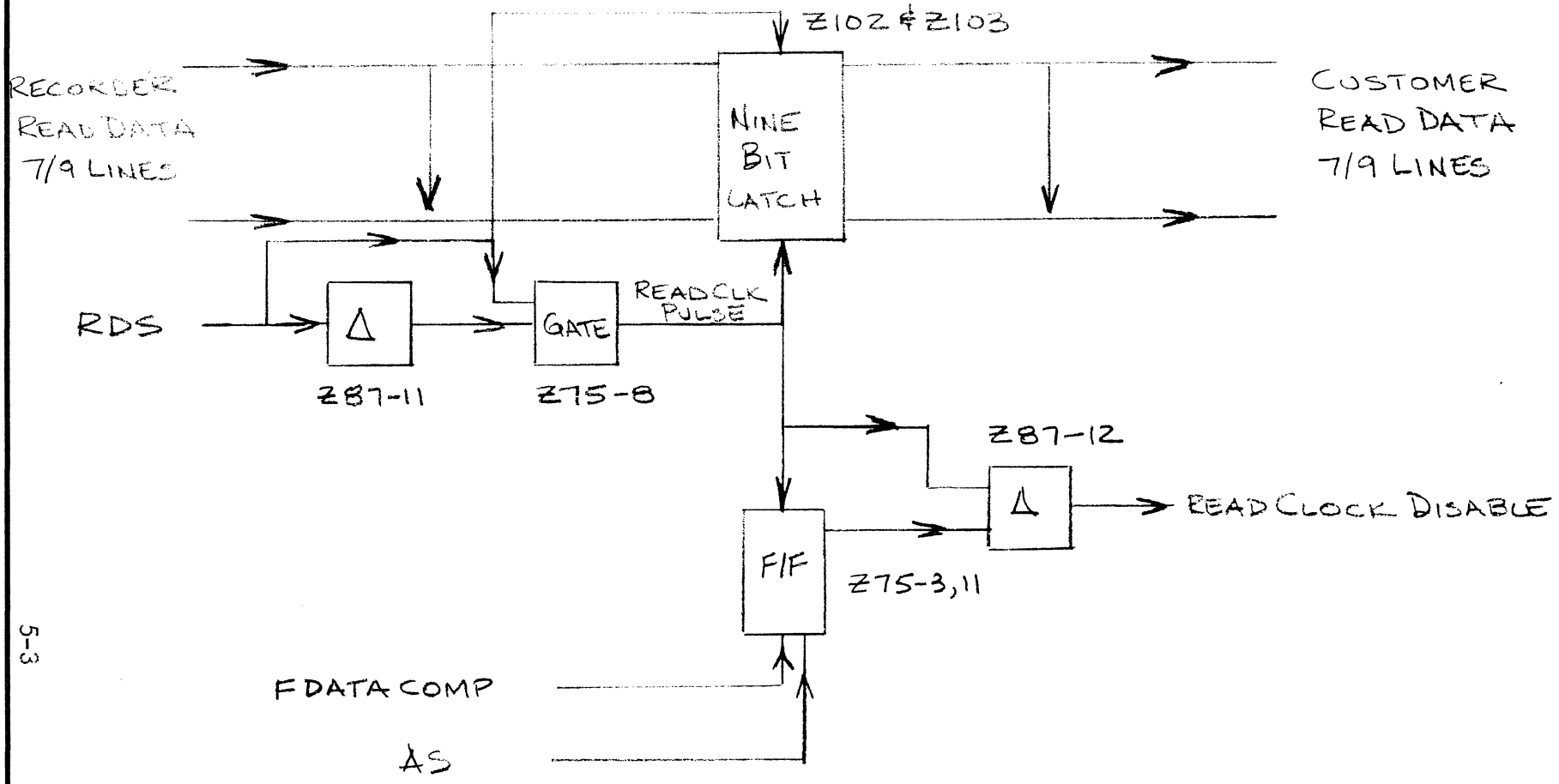
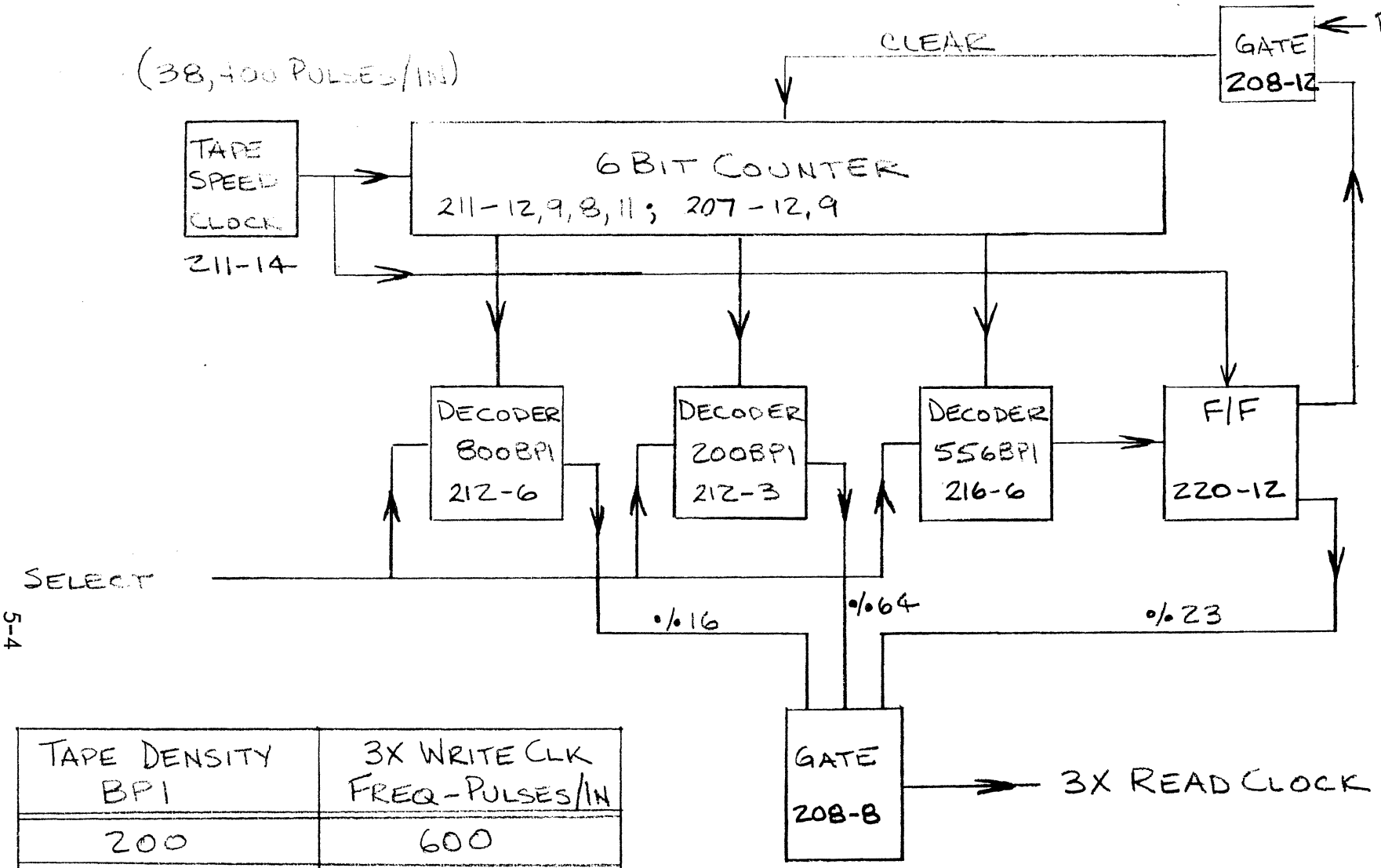


FIG 5-1

A	REF DES. CHANGE JJ1 9-21-72
BLOCK DIAGRAM - READ DATA & READ CLK DISABLE	DIGI-DATA CORPORATION
JJ1 12-27-71	SHEET OF



TAPE DENSITY BPI	3X WRITE CLK FREQ-PULSES/IN
200	600
556	1669
800	2400

FIG 5-2

BLOCK DIAGRAM - 3X READ CLOCK

JJ1 12-21-71

A	REF DES. CHANGE JJ1 9-21-72

DIGI-DATA CORPORATION

SHEET OF

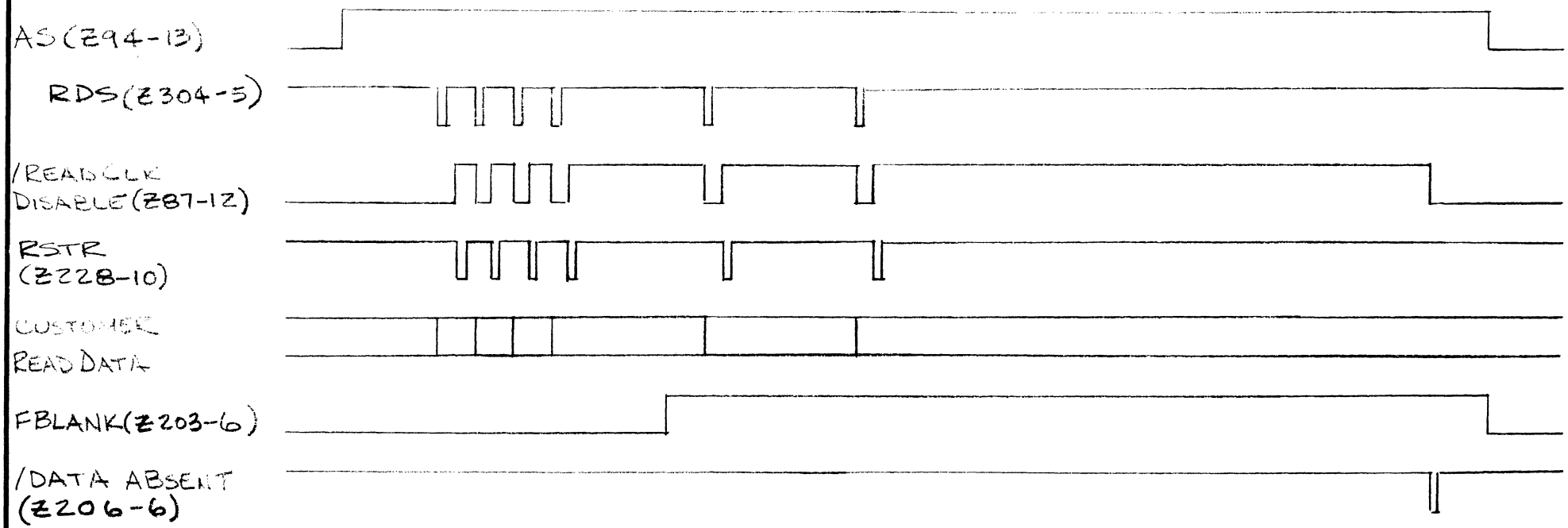


FIG 5-3

TIMING DIAGRAM – READ FORWARD OPERATION	A REF DES. CHANGE JJI 9-21-72
JJI 12-27-71	DIGI-DATA CORPORATION
	SHEET OF

READ FORWARD/REVERSE OPERATION (cont.)

CUSTOMER READ STROBES are generated by gating the Ø state of the counter and READ CLOCK DISABLE false. These clocks, 1/3 character period in width, bear a one-to-one correspondence with READ DATA STROBES.

A gate whose output is true when the 2 Bit counter is between the 2 and 3 states is applied to a 4 bit counter. This counter is held cleared by READ CLOCK DISABLE. Therefore, whenever the tape has advanced one character space without the tape deck issuing a READ DATA STROBE the counter will advance one count (true to false transition of the input). When the 4 bit counter advances to the 3 state (three character periods without a READ DATA STROBE), the BLANK latch is set. The output of this latch may be utilized to gate CUSTOMER READ STROBE (option specified at time of manufacture). This option is normally employed to suppress the CUSTOMER READ STROBES associated with the CR/LR characters when reading in the forward direction. When reading in reverse, the clocks associated with the CR/LR characters will not be suppressed regardless of the option specified.

When the 4-bit counter advances to the count of 15, DATA ABSENT goes true clamping READ CLOCK DISABLE true and initiating the post-record delay.

READ EOF (Refer to FIG 5-5 and TABLE 5-1)

READ CHARACTER CLOCK, generated by gating/READ CLOCK DISABLE and the Ø state of the 2 Bit - 3X READ CLOCK counter, is utilized to clock two J-K flip-flops connected as an electronic "combination lock". Whenever the flip-flops assume the (A-1, B-0) state, they will not change state until they are asynchronously cleared.

Recognition of the file character places the flip-flops in the (A = 1, B = 1) state. Recognition of the LRCC associated with the file character places the flip-flops in the (A = 0, B = 1) state.

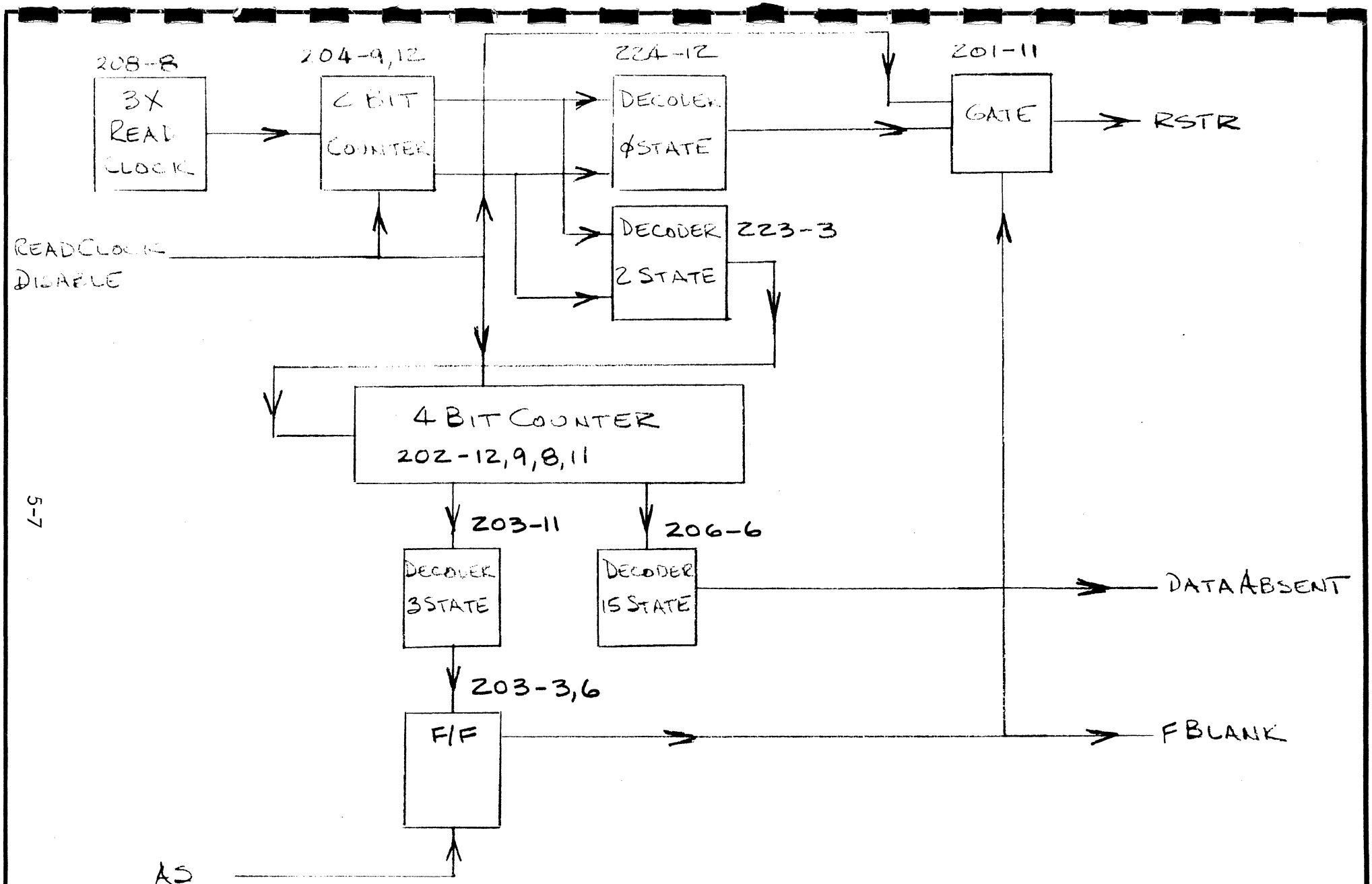


FIG 5-4

A	REF DES. CHANGE JJ 9-21-72
BLOCK DIAGRAM - CUSTOMER READ CLOCK	DIGI-DATA CORPORATION
JJ 12-27-71	SHEET OF

EOF DETECT TRUTH TABLE

B_m	A_m	F Blank	File	JB	KB	JA	KA	Bm+1	Am+1
0	0	0	0	0	X	1	X	0	1
0	0	0	1	1	X	1	X	1	1
0	0	1	0	0	X	1	X	0	1
0	0	1	1	1	X	1	X	1	1
0	1	0	0	0	X	X	0	0	1
0	1	0	1	0	X	X	0	0	1
0	1	1	0	0	X	X	0	0	1
0	1	1	1	0	X	X	0	0	1
1	0	0	0	X	1	1	X	0	1
1	0	0	1	X	1	1	X	0	1
1	0	1	0	X	1	1	X	0	1
1	0	1	1	X	1	1	X	0	1
1	1	0	0	X	1	X	0	0	1
1	1	0	1	X	1	X	0	0	1
1	1	1	0	X	1	X	0	0	1
1	1	1	1	X	0	X	1	1	0

TABLE 5-1

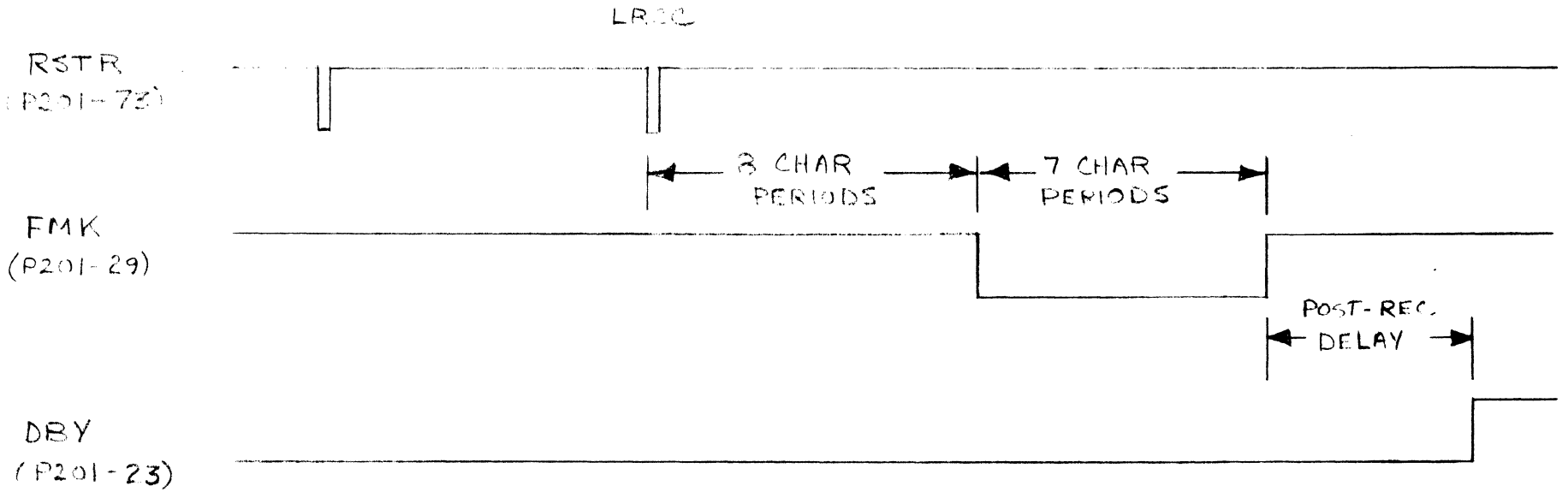


FIG 5-5

TIMING DIAGRAM - FMK	DIGI-DATA CORPORATION
	SHEET OF

LRCC CHECKER (Refer to FIG 5-6)

Nine J-K flip-flops are utilized to check the number of flux reversals per track. For each READ DATA STROBE the flip-flops are clocked with the current status of the READ DATA lines. When the gap is detected (twelve character spaces without a READ DATA STROBE), the contents of the flip-flops are examined. If any flip-flop is in the set state (odd number of flux-reversals for a record) ERROR status is transmitted to the customer I/O.

CHECK CHARACTER GATE

The Check Character Gate is designed to provide an enveloping signal for the Customer READ DATA STROBES associated with the CR and LR characters. F BLANK gates CCG true three character spaces after the RDS associated with the last data character of a record. CCG is set false coincident with the true-false transition of DBY.

CRCC VERTICAL PARITY CHECK (NFM MODELS ONLY)

The following property of the CRCC is utilized for error detection when reading forward with a 9T tape unit:

NUMBER OF DATA CHARACTERS	CRCC VERTICAL PARITY
ODD	EVEN
EVEN	ODD

Whenever an error is detected, HER will be set true coincident with the DATA lines associated with the CRCC RSTR. Additionally, whenever six character spaces have been traversed from the last data character without the transmission of a RDS from the selected drive, the FORMATTER will generate a RSTR (data lines will be false) to the CONTROLLER; error status will be set true if the record contained an even number of data characters.

Note that CRCC vertical parity checking will be suppressed when the CHECK CHAR switch is in the BLANK position.

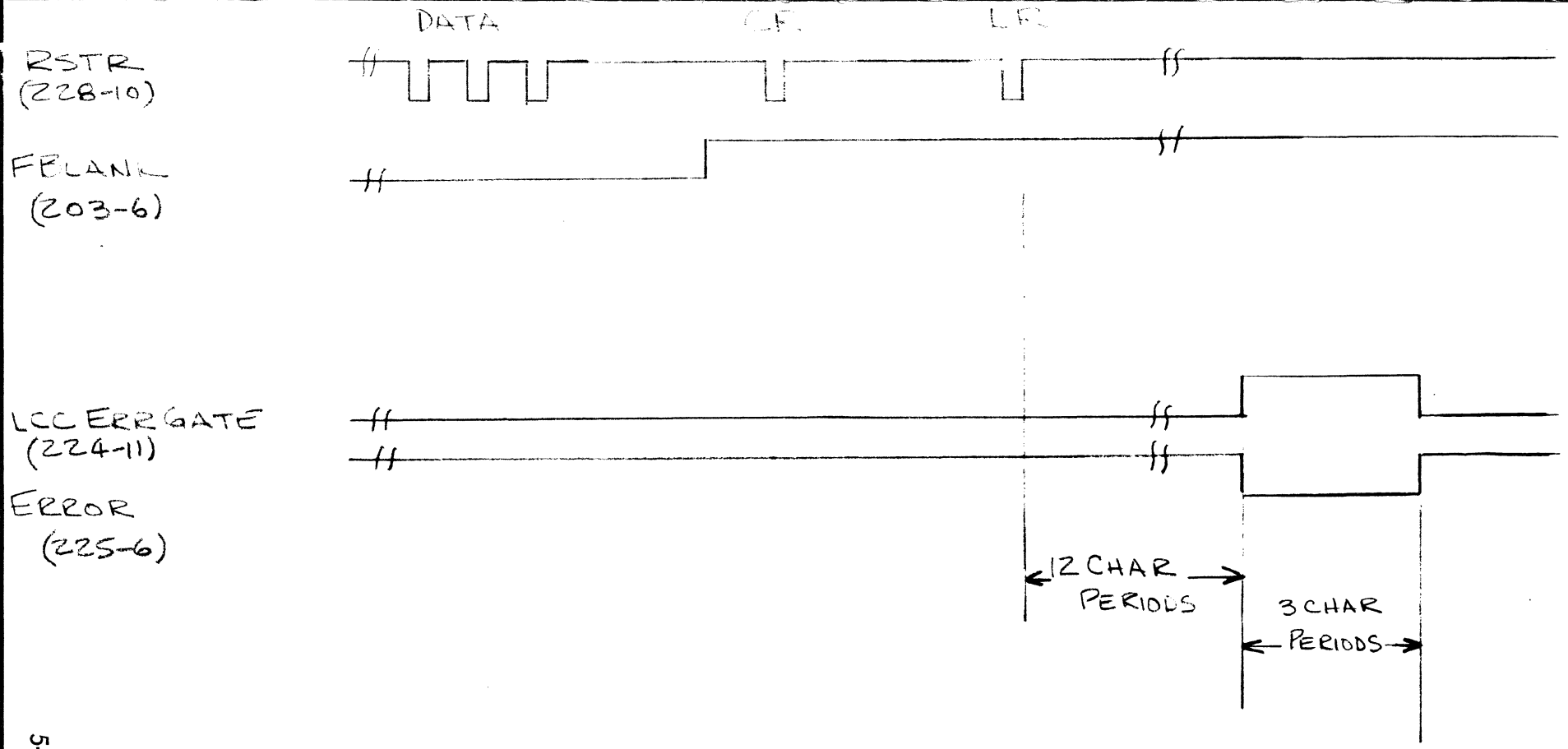


FIG 5-6

TIMING DIAGRAM – LCC CHECKER	A REF DES CHANGE JH 9-21-72
JJ 12-27-71	DIGI-DATA CORPORATION
	SHEET OF

INTERFACE AND APPLICATION SUMMARY FOR DIGI-DATA NRZI/PHASE ENCODED FORMATTERS

CONTENTS
****

LIST OF TABLES

LIST OF FIGURES

1. INTRODUCTION

Digi-Data formatters offer the systems user computer compatibility combined with ease of interfacing. The formatters enable the generation and full read recovery of IBM compatible magnetic tapes in addition to handling the details of interfacing the transport.

2. SPECIFICATIONS

RECORDING MODE	NRZI/PE
DATA DENSITY	7T 200 BPI (NRZI) 7T 556 BPI (NRZI) 7T 800 BPI (NRZI) 9T 800 BPI (NRZI) 9T 1600 BPI (PE)
OPERATING SPEEDS	6.25 to 75 IPS
ELECTRONICS	Solid State, Silicon
ELECTRICAL INTERFACE	DTL/TTL compatible (low true), compatible with many existing controllers.
POWER	105 to 125 VAC (220 VAC optional) 50 to 400 Hz
MOUNTING	Standard 19" rack mount (EIA Standard), (NRZI Formatter also available mounted in tape transport)
OPERATING ENVIRONMENT	40 to 110°F, humidity to 95% relative without condensation
ALTITUDE	0 to 10,000 feet
CONFIGURATIONS	Write only, read only, Write/Read (Single gap head), Read after write (Dual gap head)

3. OPERATOR CONTROLS AND INDICATORS *

POWER	A switch that applies power to the formatter
POWER ON	This indicator is illuminated when power is applied to the formatter

* These not available when NRZI Formatter is mounted in the TAPE UNIT. (TAPE UNIT controls and indicators apply.)

4. ELECTRICAL INTERFACE

All signal inputs should be included in one harness and all outputs in a second harness. The maximum transmission distance is 20 feet. The two harnesses can be run in close proximity. The signals are transmitted by individual twisted pairs to reduce crosstalk. The twisted pairs should have the following characteristics:

(1) Maximum length of 20 feet;

(2) Not less than one twist per inch;

(3) 22 gauge or 24 gauge conductors with minimum insulation thickness of 0.01 inch.

(4) The ground side of each twisted pair to be grounded within 6 inches of the interface circuit to which it is connected.

(5) The pullup and termination resistors should be installed as close as possible to the controller end of the twisted pair interface cable. Power for these resistors should be provided by a heavy twisted pair from the controller power supply and bypass capacitors should be employed near the resistors. The controller should drive all transport inputs with open collector circuits capable of sinking at least 25 milliamps. The controller output driven circuits, especially the WRITE DATA outputs, should be loaded as close as possible to the interface cable and heavily grounded to it.

5. INTERFACE SIGNAL DESCRIPTION

Table 1 lists all formatter input and output signals. Table 3 gives a brief description of the signal functions.

The logic levels on all input/output lines are low true.

TRUE: 0 to +0.4 volt

FALSE: +2.5 to +5.5 volt

Minimum input pulse width: 0.5 usec unless otherwise specified.

CONTROLLER TO FORMATTER		FORMATTER TO CONTROLLER	
Signal Name	Description	Signal Name	Description
TRANSPORT ADDRESS 0 (TAD 0)	Address	FORMATTER BUSY (FBY)	
TRANSPORT ADDRESS 1 (TAD 1)	1 of 4 Transports	DATA BUSY (DBY)	
		HARD ERROR (HER)	FORMATTER STATUS
REVERSE/FORWARD (REV/FWD)		FILE MARK (FMK)	
WRITE/READ (WRT)		**IDENTIFICATION (IDENT)	
EDIT	CONTROLS	**CORRECTED ERROR (CER)	
ERASE	LATCHED BY		
READ THRESHOLD 1 (THR 1)	"GO"	READY (RDY)	
READ THRESHOLD 2 (THR 2)		ON LINE (ONL)	
*PARITY (PAR)		REWINDING (RWD)	
*DENSITY (DEN)		FILE PROTECTED (FPT)	
		LOAD POINT (LPT)	TRANSPORT
REWIND (REW)	DIRECT	END OF TAPE (EOT)	STATUS
OFF LINE (OFL)	COMMANDS	*DENSITY STATUS (DEN STAT)	
		SPEED	
FORMATTER ENABLE (FEN)		SINGLE (SGL)	
GATE W P/C	STATIC CONTROL	*7 TRACK (7 TR)	
FORMATTER ADDRESS (FAD)	LINES	NRZI	
W0 (MSB)		WRITE STROBE (WSTR)	
W1		READ STROBE (RSTR)	TIMING CLOCKS
W2/B		CHECK CHARACTER GATE	
W3/A			
W4/8		R0 (MSB)	
W5/4 (9 TR/7 TR)	WRITE DATA	R1	
W6/2		R2/B (9 TR/7 TR)	
W7/1 (LSB)		R3/A	
WP/C (External)		R4/8	READ DATA
		R5/4	
	WRITE	R6/2	
LAST WORD (LWD)	TERMINATION	R7/1 (LSB)	
	PULSE OR LEVEL	RP/C	
GO	INITIALIZATION PULSE		

* NRZI
** PE

TABLE 1

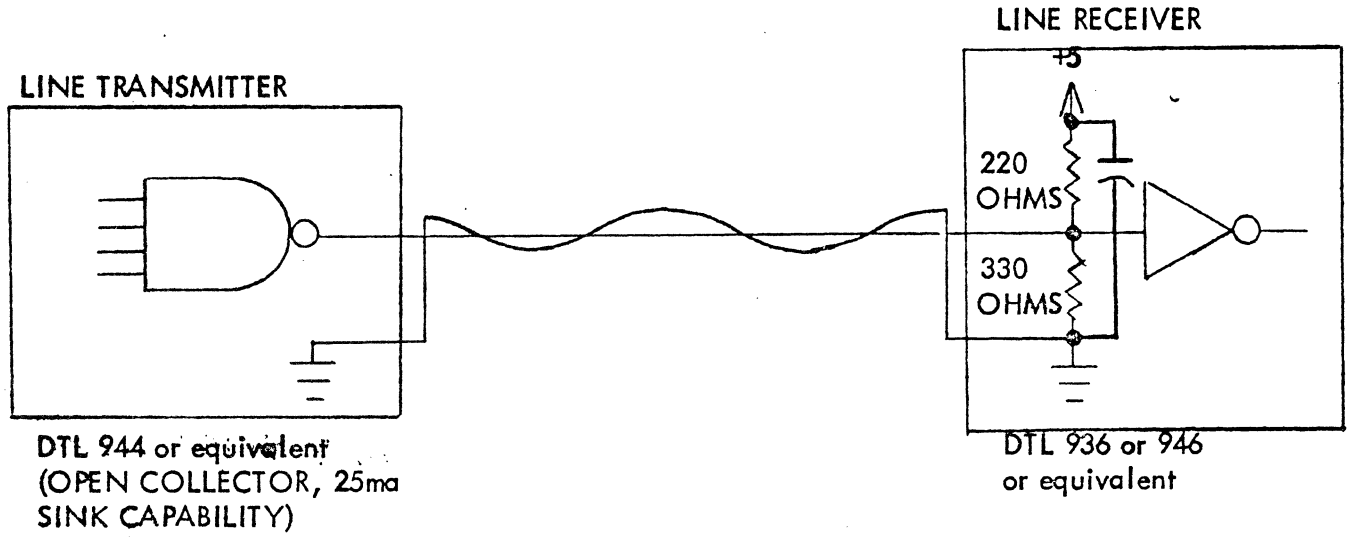


FIGURE I CONTROLLER/FORMATTER INTERFACE CIRCUIT

DIGI-DATA CORPORATION

GROUND PIN	SIGNAL PIN	
4	3	WP/C
6	5	WO (MSB)
8	7	W1
10	9	W2/B
12	11	W3/A
14	13	W4/8
16	15	W5/4
18	17	W6/2
	19	W7/1 (LSB)
	20	GATE WP/C
22	21	FBY
	23	DBY
	24	IDENT (**)
26	25	DEN STAT (*)
	27	HER
	28	CER (**)
30	29	FMK
	31	CCG (*)
	32	7 TR (*)
34	33	RDY
36	35	ONL
38	37	RWD
	39	THR 2
	40	THR 1
42	41	ERASE
	43	EDIT
	44	WFM
46	45	WRT

GROUND PIN	SIGNAL PIN	
48	47	REV/FWD
50	49	OFL
52	51	REW
54	53	TAD 1
56	55	TAD 0
58	57	LWD
60	59	FPT
62	61	LPT
64	63	EOT
66	65	NRZI
68	67	SGL
70	69	SPEED
72	71	WSTR
74	73	RSTR
76	75	RO (MSB)
78	77	R1
80	79	R2/B
82	81	R3/A
84	83	R4/8
86	85	R5/4
88	87	R6/2
90	89	R7/1 (LSB)
92	91	RP/C
94	93	FEN
96	95	FAD
98	97	GO
	99	PAR (*)
	100	DEN (*)

(*) NRZI FORMATTER ONLY (P201)

(**) PE FORMATTER ONLY (P7)

GROUND PIN	SIGNAL PIN	
5	6	SRC
7	8	SFC
9	10	SLT 1
11	12	SLT 0
13	14	SLT 3
15	16	SLT 2
17	18	OVW
19	20	RTH 1
21	22	RTH 2
23	24	WDS
25	26	WARS
27	28	SWS
31	32	NRZ/PE
33	34	EOT
35	36	LDP
37	38	FPT
39	40	RWD
41	42	ONL
43	44	RDY
45	46	SPEED
47	48	SGL
49	50	7 TRK
51	52	DDI
53	54	RDP/C
59	60	RDO (MSB)
61	62	RD 1
63	64	RD 2/B

GROUND PIN	SIGNAL PIN	
65	66	RD3/A
67	68	RD4/8
69	70	RD5/4
71	72	RD6/2
73	74	RD7/1 (LSB)
75	76	RDS
77	78	DDS
79	80	WDP/C
81	82	WDO (MSB)
83	84	WD 1
85	86	WD2/B
87	88	WD3/A
89	90	WD4/8
91	92	WD5/4
93	94	WD6/2
95	96	WD7/1 (LSB)
97	98	OFFC
99	100	RWC

DIGI-DATA CORPORATION

SHEET OF

NRZI FORMATTER/TAPE UNIT
I/O CONNECTOR (P101)

P8

GROUND PIN	SIGNAL PIN	
2		+5 VDC
4		+5 VDC
5	6	SRC
7	8	SFC
9	10	SLT 1
11	12	SLT 0
13	14	SLT 3
15	16	SLT 2
17	18	OVW
19	20	RTH 1
21	22	RTH 2
23	24	WDS
25	26	WARS
27	28	SWS
31	32	NRZ/PE
33	34	EOT
35	36	LDP
37	38	FPT
39	40	RWD
41	42	ONL
43	44	RDY
45	46	SPEED
47	48	SGL
79	80	WD P/C
81	82	WD 0 (MSB)
83	84	WD 1

P8

GROUND PIN	SIGNAL PIN	
85	86	WD 2
87	88	WD 3
89	90	WD 4
91	92	WD 5
93	94	WD 6
95	96	WD 7 (LSB)
97	98	OFFC
99	100	RWC

P3

53	54	RD P
59	60	RD 0 (MSB)
61	62	RD 1
63	64	RD 2
65	66	RD 3
67	68	RD 4
69	70	RD5
71	72	RD 6
73	74	RD 7 (LSB)

TABLE #3

FORMATTER SIGNAL DESCRIPTION

SIGNAL NAME	DESCRIPTION
TRANSPORT ADDRESS 0 TRANSPORT ADDRESS 1	(Input Level) These two lines select one of the four transports which may be bussed onto the formatter. These lines are decoded by the formatter and transmitted to the FORMATTER/TRANSPORT interface as follows: TAD 0 — TAD 1 — TRANSPORT ADDRESS 0 — 0 — 0 0 — 1 — 1 1 — 0 — 2 1 — 1 — 3
REVERSE/FORWARD	(Input Pulse or Level) This line specifies forward or reverse tape motion: TRUE= REVERSE
WRITE/READ	(Input Pulse or Level) This line specifies WRITE or READ mode: TRUE = WRITE
WRITE FILE MARK	(Input Pulse or Level) WFM will specify an END OF FILE to be written on the tape, if WRITE/READ is also TRUE, and ERASE is FALSE.
EDIT	(Input Pulse or Level) This line is used in two ways: (a) Read Reverse. Modifies read reverse post-record delay to optimize head positioning when editing tapes. (b) Write. Activates internal logic such that the associated transport operates in the edit mode.
ERASE	(Input Pulse or Level) If ERASE and WRITE/READ are TRUE the formatter is conditioned to execute a dummy write command. The formatter will go through the motions of a normal write operation except that no data can be recorded. The controller will receive WRITE STROBE and may count the desired length of record to be erased. This operation is terminated by transmitting LAST WORD. Alternatively, if ERASE, WRITE/READ, and WRITE FILE MARK command lines are TRUE, the formatter is conditioned to execute a dummy write file mark command. A fixed length of tape of approximately 3.75 inches will be erased.
READ THRESHOLD 1	(Input Pulse or Level) THR 1 instructs the selected transport to operate in NORMAL or HIGH read threshold mode: TRUE = HIGH THRESHOLD FALSE = NORMAL THRESHOLD (See TAPE UNIT OEM specifications for Dual-Gap considerations)

TABLE #3 (Cont.)

FORMATTER SIGNAL DESCRIPTION

SIGNAL NAME	DESCRIPTION
READ THRESHOLD 2	(Input Pulse or Level) THR 2 is used with transports which have an extra low read threshold capability. TRUE = LOW THRESHOLD FALSE = NORMAL THRESHOLD This input may be made TRUE when it is desired to recover very low amplitude data.
PARITY (NRZI)	(Input Pulse or Level) PAR is used to select EVEN or ODD vertical parity for the formatter parity generation and checking circuitry. TRUE = EVEN PARITY FALSE = ODD PARITY This line is ignored and ODD parity is forced internally if the selected transport is a 9 track unit.
DENSITY (NRZI)	(Input Pulse or Level) DEN is used with 7 track transports which have dual density capabilities. TRUE = HIGH DENSITY FALSE = LOW DENSITY Jumpers on the formatter timing card allow the following choices of densities: LOW DENSITY = 200 or 556 BPI HIGH DENSITY = 556 or 800 BPI Whenever the selected unit is 9 track, the NRZI FORMATTER will operate at 800 BPI regardless of the state of DEN. DEN is also utilized when the NRZI FORMATTER is daisy-chained with a PE FORMATTER to drive DUAL DENSITY 9 track tape units. DEN must be set true when the NRZI FORMATTER is addressed. Failure to do this will result in a format mismatch between the FORMATTER and TAPE UNIT.
REWIND	(Input Pulse) REW causes the selected transport (provided it is READY) to rewind to LOAD POINT. This pulse is routed directly to the transport and does not cause the formatter to become BUSY. Min width 2 usec.
OFF LINE	(Input Pulse) OFL causes the selected transport to go OFF LINE. This pulse is routed directly to the transport and does not cause the formatter to become BUSY. Min width 2 usec.
FORMATTER ENABLE	(Input Level) FEN must be held TRUE during all formatter operation. A FALSE level on this line clears the formatter and holds it in a clear state.
GATE W P/C	(Input Level) This line instructs the formatter to write the data presented on the WRITE DATA P line in the parity track and disables the internal parity generation circuitry. TRUE = EXTERNAL PARITY FALSE = GENERATE INTERNAL PARITY

TABLE #3 (Cont.)

FORMATTER SIGNAL DESCRIPTION

SIGNAL NAME	DESCRIPTION
FORMATTER ADDRESS	(Input Level) FAD informs the formatter that it is to respond to commands on the formatter/controller bus.
WRITE DATA (W0-W7, WP)	(Input Level) These lines transmit write data from the controller to the formatter. WRITE DATA may be changed only during the half character period following the trailing edge of WRITE STROBE, and must be stable at all other times, to ensure fidelity of data written. Processing continues upon WRITE DATA presented until LAST WORD is received by the formatter.
LAST WORD	(Input Pulse or Level) LWD operates in one of two ways to indicate that the last desired character has been transmitted on write operations: (1) Synchronous - In this mode, LAST WORD must be presented to the formatter coincident with the last desired character, spanning the last desired WRITE STROBE in the same manner as specified for WRITE DATA. (2) Asynchronous - In this mode, LAST WORD must be presented AFTER the trailing edge of the last desired WRITE STROBE, but may be presented at any time during the half character period following the trailing edge of the last desired WRITE STROBE. The FORMATTER is conditioned to accept (1) or (2) above by the setting of a PCB switch.
GO	(Input Pulse) This input command initiates the action specified by CONTROL lines, listed in Table 1. These lines are copied into corresponding flip-flops in the FORMATTER, and on the trailing edge of GO, FORMATTER BUSY is set TRUE. The COMMAND lines, as well as the STATIC CONTROL lines and the TAD lines, should be stable at least .5 usec before the leading edge of GO. The COMMAND lines must remain stable for at least .5 usec after the trailing edge of GO. The STATIC CONTROL lines and the TAD lines must be stable throughout the operation.
FORMATTER BUSY	(Output Level) FBY will become TRUE on the trailing edge of GO, and normally remains true until tape motion has ceased after execution of the commanded operation.
DATA BUSY	(Output Level) DBY will become TRUE when the transport has reached operating speed and is about to begin a WRITE or READ data transfer. This line will remain TRUE until the data transfer is

TABLE #3 (Cont.)

FORMATTER SIGNAL DESCRIPTION

SIGNAL NAME	DESCRIPTION
	completed, and the appropriate post-record delay is completed. At this time, when DATA BUSY returns to a FALSE state, a "window" is created, during which a GO pulse may be issued. If a GO pulse is received during this window, the tape remains at operating speed and continues with another data transfer of the same type as the previous one (the same WRITE/READ and REVERSE/FORWARD status). If no GO pulse is received by the end of the window, GO is locked out, and deceleration of the tape begins GO will remain locked out until FORMATTER BUSY goes FALSE.
HARD ERROR (NRZI)	(Output Pulse or Level) This line indicates a read error has been detected. (a) Vertical Parity in error. (b) Longitudinal Parity in error. Vertical parity errors will be indicated by this line coincident with the data of the character(s) in error, and specified exactly as the READ DATA for the character. A READ STROBE will always accompany a character which has been read, and this READ STROBE may be used, in conjunction with HARD ERROR, to store vertical parity error, if desired. Longitudinal Parity errors will be indicated by this line approximatd y 12 character periods after the last READ STROBE has been transmitted. No READ STROBE will accompany the HARD ERROR pulse in the case of longitudinal parity error. This pulse will be approximately 3 character-periods in width, and will return to the FALSE state slightly prior to DATA BUSY going FALSE.
HARD ERROR (PE)	(Output Pulse or Level) HER indicates an uncorrectable read error has been detected by the formatter for one or more of the following reasons: (a) False preamble detection (b) False postamble detection (c) Buffer overflow (d) Multichannel dropout (e) Parity error without associated channel dropouts With the exception of a parity error, the formatter will cease transmission of further read data and search for the IBG. For a parity error only, the erroneous character will be transmitted and labelled by a pulse on HARD ERROR at the READ STROBE.

TABLE #3 (Cont.)

FORMATTER SIGNAL DESCRIPTIONS

SIGNAL NAME	DESCRIPTIONS
CORRECTED ERROR (PE)	(Output Pulse) CER indicates that a single track dropout has been detected and that the formatter is performing error correction. NOTE: When performing a read-after-write operation, to verify that information has been correctly recorded onto tape, the record should be rewritten if either a HARD ERROR or CORRECTED ERROR is detected.
FILE MARK	(Output Pulse) FMK indicates that the formatter read logic has detected a file mark. EOFs are detected in both the forward and reverse directions.
READY	(Output Level) RDY is TRUE only when all of the following conditions exist in the selected transport: the initial load or rewind sequence is complete, and the transport is ON LINE and not rewinding. That is, the transport is ready to receive an external command.
ON LINE	(Output Level) ONL is TRUE if the selected transport is under remote control. When FALSE the transport is off-line and cannot be operated externally.
REWINDING	(Output Level) RWD is TRUE when the selected transport is in a REWIND or advance to LOAD POINT mode.
FILE PROTECT	(Output Level) FPT is TRUE when no write ring has been installed on the supply reel of the selected transport. The transport will not write when this output is true.
LOAD POINT	(Output Level) LDP is TRUE when the selected transport detects the BOT marker.
END OF TAPE	(Output Level) EOT is TRUE when the selected transport detects the END OF TAPE marker.
DENSITY STATUS (NRZI)	(Output Level) DEN STAT is TRUE when the selected transport has responded to a HIGH density command.
SPEED	(Output Level) This line is TRUE when the selected transport is a LOW SPEED unit. For example, if a 12.5 ips transport and a 37.5 ips transport are to be operated by the same formatter, the LOW SPEED jumpers are set to select 12.5 ips, and the HIGH SPEED jumpers are set to select 37.5 ips. The 12.5 ips transport will then be wired to generate LOW SPEED STATUS when selected.

TABLE #3 (Cont.)

FORMATTER SIGNAL DESCRIPTION

SIGNAL NAME	DESCRIPTION
SINGLE	(Output Level) This line indicates whether the selected transport is a single or dual gap device. TRUE = Single Gap FALSE = Dual Gap
NRZ1	(Output Level) This line indicates whether the selected transport is an NRZI transport. TRUE = NRZI
WRITE STROBE	(Output Pulse) WSTR indicates that the information currently presented on the WRITE DATA lines is being written on the tape. The trailing edge may be utilized to initiate data line changes. PULSE WIDTH = 1/3 CHARACTER PERIOD
READ STROBE	(Output Pulse) RSTR should be used to sample the READ DATA lines. Individual pulses will be generally equally-spaced, with some variations due to skew and bit-crowding effects. PULSE WIDTH = 1/3 CHARACTER PERIOD
CHECK CHARACTER GATE (NRZ1)	(Output Pulse). This line will go true three character spaces after the RDS associated with last data character of a record. The line will go false coincident with the true-false transition of DBY. This line is employed as an enveloping signal for the CR and LR characters when they are transmitted from the formatter (ALLOW CHECK CHARACTER option).
7 TRACK	(Output Level) 7 Tr, when true, indicates that the selected tape unit is 7 Track.
READ DATA (NRZI) (R0-R7, RP)	(Output Level) These lines transmit read data from the tape. READ DATA will be stable prior to the leading edge of READ CLOCK and will remain stable for approximately the full character period, ± variations due to skew and bit-crowding effects.
READ DATA (PE) (R0-R7, RP)	(Output Level) These nine lines transmit read data from the formatter to the controller; each character read from tape is available by sampling these lines in parallel by the READ STROBE. Data remains set on the lines for a full character period. The corresponding READ CLOCK is 1/3 character period wide, in the center of the data cell.

TABLE #3 (Cont.)

FORMATTER SIGNAL DESCRIPTION

SIGNAL NAME	DESCRIPTION
IDENTIFICATION (PE)	(Output Pulse) When reading forward from BOT, the formatter inspects the parity channel for the presence or absence of the identification burst which distinguishes PE tapes. If the burst is detected, IDENT is set true for a short time as the BOT marker passes over the read head.

TABLE 4

TYPICAL PE FORMATTER TIME DELAYS AT 12.5 IPS (Time in Milliseconds)

FUNCTION	REFERENCE	TIME
WRITE		
1. Write from BOT	Trailing edge of GO to DATA BUSY going true.	512
2. Write Normal	Trailing edge of GO to DATA BUSY going true.	44.8 (Single Gap) 33.6 (Dual Gap)
3. First WRITE STROBE	DATA BUSY true to first WRITE STROBE.	2.050
4. Data on Line	Data must be on line and stable for one-half a character period before WRITE STROBE.	25 usec
5. Postamble & Post Record Delay	LAST WORD to DATA BUSY going false.	8.8 (single gap) 21.4 (dual gap)
6. Transport Decelerating	DATA BUSY going false to FORMATTER BUSY going false.	38.4
7. WRITE FILE MARK	Trailing edge of GO to DATA BUSY going true.	308
READ		
1. Read from BOT	Trailing edge of GO to DATA BUSY going true.	128
2. Read Normal	Trailing edge of GO to DATA BUSY going true.	25.6
3. Transport Decelerating	DATA BUSY going false to FORMATTER BUSY going false.	38.4

TABLE 4A

TYPICAL NRZI FORMATTER TIME DELAYS AT 12.5 IPS (Time in milliseconds)

FUNCTION	REFERENCE	TIME			
		7 TRACK		9 TRACK	
		Single Gap	Dual Gap	Single Gap	Dual Gap
WRITE					
1. Write from BOT	Trailing edge of GO to DATA BUSY true.	280	280	280	280
2. Write EOF	Trailing edge of GO to DATA BUSY true.	280	280	280	280
3. Write NORMAL	Trailing edge of GO to DATA BUSY true.	56	32	46	34
4. First WRITE CLOCK	DATA BUSY true to first WRITE CLOCK.	5 us	5 μs	5 us	5 μs
5. Data ON LINE	Data must be on line and stable for 1/2 character period before WRITE CLOCK.				
6. Post Record Delay	Last WRITE CLOCK to DATA BUSY going false.	7	31	7	19
7. Stay at speed window	Trailing edge of DATA BUSY.	250 us	250 μs	250 μs	250 μs
8. Transport stopping	Trailing edge of DATA BUSY to trailing edge of FORMATTER BUSY	35	35	35	35
READ					
1. Read from BOT	Trailing edge of GO to DATA BUSY true.	150	150	150	150
2. Read normal	Trailing edge of GO to DATA BUSY true.	24	24	24	24
3. Post Record Delay (FWD)	Last READ CLOCK to DATA BUSY going false.	2.0	2.0	2.5	2.5
REV (NORMAL)		17	17	7.4	7.4
REV (EDIT)		22	22	14	14
4. Stay at speed window	Trailing edge of DATA BUSY.	250μs	250us	250us	250μs
5. Transport Stopping	Trailing edge of DATA BUSY to trailing edge of FORMATTER BUSY.	35	35	35	35

TABLE 4B

TYPICAL NRZI FORMATTER TIME DELAYS AT 18.75 ips (Time in milliseconds)

FUNCTION	REFERENCE	TIME			
		7 TRACK		9 TRACK	
		Single Gap	Dual Gap	Single Gap	Dual Gap
WRITE					
1. Write from BOT	Trailing edge of GO to DATA BUSY true.	185	185	185	185
2. Write EOF	Trailing edge of GO to DATA BUSY true.	185	185	185	185
3. Write NORMAL	Trailing edge of GO to DATA BUSY true.	37.4	21.4	29.9	22.7
4. First WRITE CLOCK	DATA BUSY true to first WRITE CLOCK.	5 us	5 μs	5 μs	5 μs
5. Data ON LINE	Data must be on line and stable for 1/2 character period before WRITE CLOCK.				
6. Post Record Delay	Last WRITE CLOCK to DATA BUSY going false.	4.95	24	4.95	16
7. Stay at speed window	Trailing edge of DATA BUSY.	250 us	250 μs	250 us	250 μs
8. Transport stopping	Trailing edge of DATA BUSY to trailing edge of FORMATTER BUSY.	23	23	23	23
READ					
1. Read from BOT	Trailing edge of GO to DATA BUSY true.	100	100	100	100
2. Read normal	Trailing edge of GO to DATA BUSY true.	15.7	15.7	15.7	15.7
3. Post Record Delay (FWD)	Last READ CLOCK to DATA BUSY going false.	1.3	1.3	1.6	1.6
REV (NORMAL)		11.2	11.2	4.95	4.95
REV (EDIT)		14.7	14.7	9.3	9.3
4. Stay at speed window	Trailing edge of DATA BUSY.	250us	250μs	250us	250μs
5. Transport Stopping	Trailing edge of DATA BUSY to trailing edge of FORMATTER BUSY.	23	23	23	23

TABLE 4C

TYPICAL NRZI FORMATTER TIME DELAYS AT 25 ips (Time in Milliseconds)

FUNCTION	REFERENCE	TIME			
		7 TRACK		9 TRACK	
		Single Gap	Dual Gap	Single Gap	Dual Gap
WRITE					
1. Write from BOT	Trailing edge of GO to DATA BUSY true.	139	139	139	139
2. Write EOF	Trailing edge of GO to DATA BUSY true.	139	139	139	139
3. Write NORMAL	Trailing edge of GO to DATA BUSY true.	28	16	22.5	17
4. First WRITE CLOCK	DATA BUSY true to first WRITE CLOCK.	5 us	5 us	5 us	5 us
5. Data ON LINE	Data must be on line and stable for 1/2 character period before WRITE CLOCK.				
6. Post Record Delay	Last WRITE CLOCK to DATA BUSY going false.	3.7	20	3.7	14
7. Stay at speed window	Trailing edge of DATA BUSY.	250us	250us	250us	250us
8. Transport stopping	Trailing edge of DATA BUSY to trailing edge of FORMATTER BUSY.	17.5	17.5	17.5	17.5
READ					
1. Read from BOT	Trailing edge of GO to DATA BUSY true.	75	75	75	75
2. Read normal	Trailing edge of GO to DATA BUSY true.	11.7	11.7	11.7	11.7
3. Post Record Delay (FWD)	Last READ CLOCK to DATA BUSY going false.	1	1	1.2	1.2
REV (NORMAL)		8.4	8.4	3.7	3.7
REV (EDIT)		11	11	7	7
4. Stay at speed window	Trailing edge of DATA BUSY.	250us	250us	250us	250us
5. Transport Stopping	Trailing edge of DATA BUSY to trailing edge of FORMATTER BUSY.	17.5	17.5	17.5	17.5

TABLE 4D

TYPICAL NRZI FORMATTER TIME DELAYS AT 37.5 ips (Time in Milliseconds)

FUNCTION	REFERENCE	TIME			
		7 TRACK		9 TRACK	
		Single Gap	Dual Gap	Single Gap	Dual Gap
WRITE					
1. Write from BOT	Trailing edge of GO to DATA BUSY true.	93	93	93	93
2. Write EOF	Trailing edge of GO to DATA BUSY true.	93	93	93	93
3. Write NORMAL	Trailing edge of GO to DATA BUSY true.	18.7	18.7	14.9	11.3
4. First WRITE CLOCK	DATA BUSY true to first WRITE CLOCK.	5us	5μs	5μs	5μs
5. Data ON LINE	Data must be on line and stable for 1/2 character period before WRITE CLOCK.				
6. Post Record Delay	Last WRITE CLOCK to DATA BUSY going false.	2.48	16	2.48	12
7. Stay at speed window	Trailing edge of DATA BUSY.	250 μs	250μs	250μs	250μs
8. Transport stopping	Trailing edge of DATA BUSY to trailing edge of FORMATTER BUSY.	11.5	11.5	11.5	11.5
READ					
1. Read from BOT	Trailing edge of GO to DATA BUSY true.	50	50	50	50
2. Read normal	Trailing edge of GO to DATA BUSY true.	7.85	7.85	7.85	7.85
3. Post Record Delay (FWD)	Last READ CLOCK to DATA BUSY going false.	<1	<1	<1	<1
REV (NORMAL)		5.6	5.6	2.48	2.48
REV (EDIT)		7.3	7.3	4.6	4.6
4. Stay at speed window	Trailing edge of DATA BUSY.	250μs	250μs	250μs	250μs
5. Transport Stopping	Trailing edge of DATA BUSY to trailing edge of FORMATTER BUSY.	11.5	11.5	11.5	11.5

TABLE 4E

TYPICAL NRZI FORMATTER TIME DELAYS AT 45 ips (Time in Milliseconds)

FUNCTION	REFERENCE	TIME			
		7 TRACK		9 TRACK	
		Single Gap	Dual Gap	Single Gap	Dual Gap
WRITE					
1. Write from BOT	Trailing edge of GO to DATA BUSY true.	77.5	77.5	77.5	77.5
2. Write EOF	Trailing edge of GO to DATA BUSY true.	77.5	77.5	77.5	77.5
3. Write NORMAL	Trailing edge of GO to DATA BUSY true.	15.5	15.5	12.4	9.5
4. First WRITE CLOCK	DATA BUSY true to first WRITE CLOCK.	5 us	5μs	5μs	5μs
5. Data ON LINE	Data must be on line and stable for 1/2 character period before WRITE CLOCK.				
6. Post Record Delay	Last WRITE CLOCK to DATA BUSY going false.	2	14.7	2	11.3
7. Stay at speed window	Trailing edge of DATA BUSY.	250 μs	250 μs	250 μs	250 μs
8. Transport stopping	Trailing edge of DATA BUSY to trailing edge of FORMATTER BUSY.	10	10	10	10
READ					
1. Read from BOT	Trailing edge of GO to DATA BUSY true.	41.6	41.6	41.6	41.6
2. Read normal	Trailing edge of GO to DATA BUSY true.	6.55	6.55	6.55	6.55
3. Post Record Delay (FWD)	Last READ CLOCK to DATA BUSY going false.	∠1	∠1	∠1	∠1
REV (NORMAL)		4.66	4.66	2	2
REV (EDIT)		6.1	6.1	3.9	3.9
4. Stay at speed window	Trailing edge of DATA BUSY.	250 μs	250μs	250μs	250μs
5. Transport stopping	Trailing edge of DATA BUSY to trailing edge of FORMATTER BUSY.	10	10	10	10

6.0 APPLICATION INFORMATION

6.1 WRITE OPERATION

Writing normally occurs in the forward direction for commands such as Write Record, WRITE FILE MARK, EDIT, or ERASE. It is possible to write in the reverse direction (i.e., reverse erase), but this is not a recommended procedure.

An interface line, WRITE/READ under control of the customer specifies whether a write or read operation is required. This line may be either a pulse or level which envelops the GO command. The interface line, REVERSE/FORWARD, conditioned by the customer, selects the direction of tape travel. This line envelops the command and may either be a pulse or a level.

As a general rule, all interface lines are sampled by GO and latched at the formatter.

The formatter will retain the previously established WRITE/READ and REVERSE/FORWARD function until the next GO command. At that time, new conditions may be established. The formatter will be reset by a false level or pulse on the FORMATTER ENABLE line.

6.2 WRITE FORWARD COMMAND

The following sequence of events will take place when writing a record. Typical waveforms are shown in Figure 2 for the Write operation.

(1) Transport must be READY.

(2) Establish Write conditions.
   (a) Set WRITE/READ true.
   (b) Set REVERSE/FORWARD false.

(3) Initiate GO command. On the trailing edge of this pulse, the write conditions established in Step (2) are initiated. FORMATTER BUSY is set true.

   When writing from Load Point, the PE formatter will automatically write the ID Burst and then proceed with writing the first block. In order to ensure correct positioning of the ID Burst, the tape should be positioned at Load Point through either a Load command or a Rewind command.

(4) (NRZI) Set up data on the WRITE DATA lines. The NRZI formatter allows either internal or external parity generation. DATA BUSY goes true just before the first WRITE STROBE is issued.

Data must be present on these lines a minimum of one-half a character period before the first WRITE STROBE is present. The next character of information must be placed on these lines within one-half of a character period after the trailing edge of the first WRITE STROBE. This sequence is followed until all data characters of the record have been transmitted. A write operation can be abandoned if WRITE DATA is not ready when the first WRITE STROBE is issued by the controller. To abandon a Write operation, LAST WORD is set true. This will write a one-character record. The user should then backspace (Read Reverse) and start Write operation again.

(PE) When DATA BUSY goes true, the PE formatter automatically begins to write the preamble.

Set up data on the WRITE DATA lines. The PE formatter allows either internal or external parity generation. DATA BUSY goes true 41 character periods before the first WRITE STROBE is issued. Data must be present on these lines a minimum of one-half a character period before the first WRITE STROBE is present. The next character of information must be placed on these lines within one-half of a character period after the trailing edge of the first WRITE STROBE. This sequence is followed until all data characters of the record have been transmitted. A Write operation can be abandoned if WRITE DATA is not ready when the first WRITE STROBE is issued by the controller. To abandon a Write operation, LAST WORD is set true. This will write a one-character record. Backspace (Read Reverse) and start Write operation again.

(5) Set LAST WORD true at the same time that the last data character is transmitted to the formatter. When the last character is recorded, the NRZI formatter will automatically generate the check character(s). The PE formatter will automatically generate the postamble.

(6) When the check character(s)/postamble are completed, and after a small postrecord delay, DATA BUSY goes false.

DATA BUSY going false may be used to trigger the next GO command. This can be used for writing "on-the-fly".

(7) This "on-the-fly" operation should only be used when performing the same operation (i.e., writing or reading in the same direction).

(8) FORMATTER BUSY goes false when tape motion has ceased.

(9) When Write Checking for either a single or dual gap system, and a HARD ERROR or CORRECTED ERROR occurs, the record should be re-written. In dual gap systems, data will be sent to the controller while

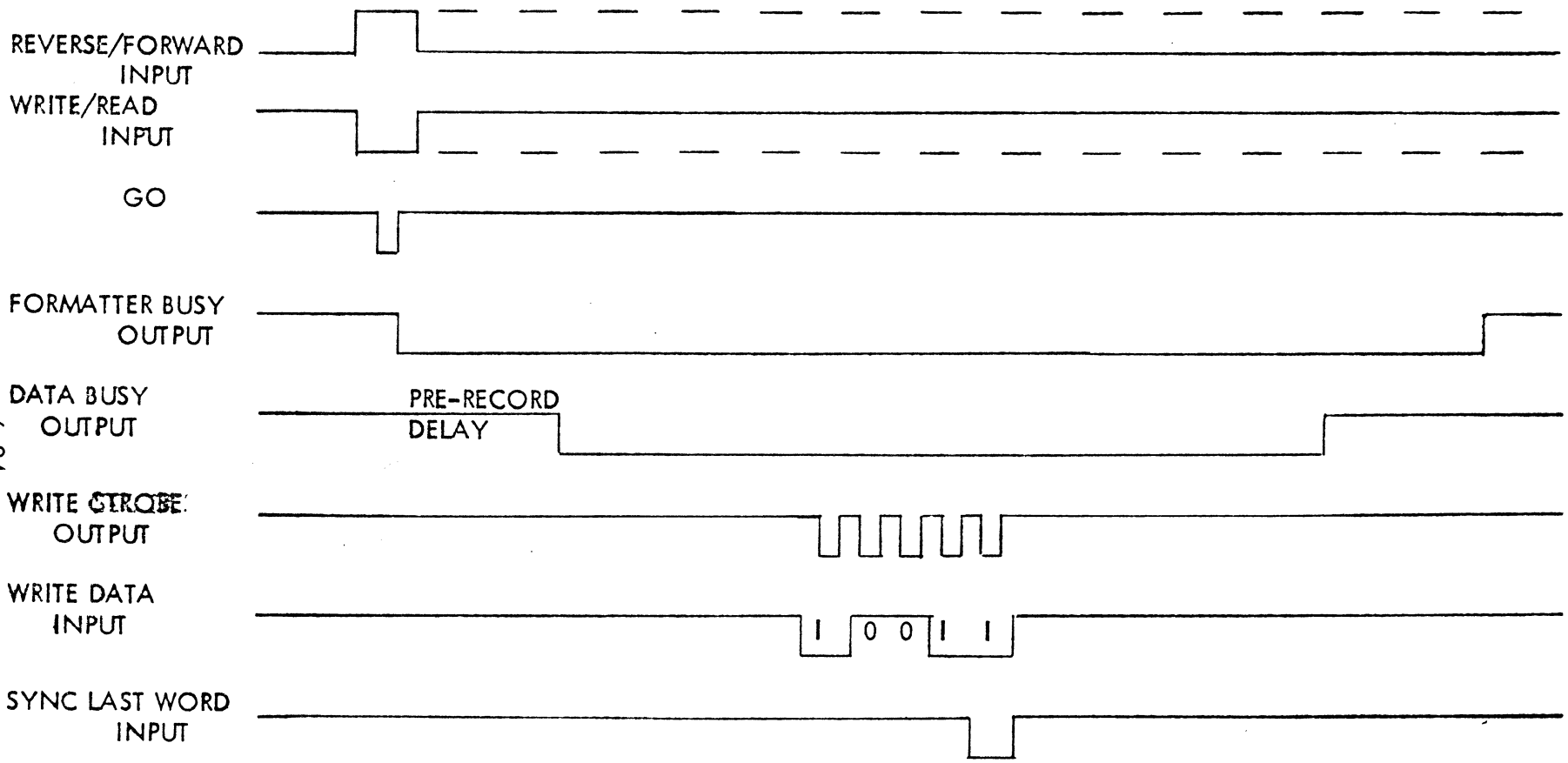


Figure 2 Write Operation Timing Diagram

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6.2 WRITE FORWARD COMMAND (Cont.)

the Write Operation is being performed. To rewrite a record, perform a Reverse Read operation. The system will automatically stop in the proper place for a Rewrite operation.

6.3 VERTICAL PARITY GENERATION

The vertical parity bit recorded in Channel P is generated so that the total number of "1" bits in each data character is always odd for 9 Track and PE transports, and may be selected as odd or even for 7 Track transports.

When EXTERNAL PARITY is selected, the parity may be even or odd as generated externally (7 Track only).

6.4 END OF FILE GENERATION

The following sequence of events will take place when writing an End of File:

(1) Transport must be READY.
(2) Establish WRITE END OF FILE conditions:
  (a) Set WRITE/READ true.
  (b) Set REVERSE/FORWARD false.
  (c) Set WRITE FILE MARK true.
(3) Initiate GO command. On the trailing edge of the pulse, the conditions established in Step 3 are initiated. FORMATTER BUSY is set true.
(4) DATA BUSY goes true, and the FILE MARK is automatically written onto tape. For dual gap Read After Write systems, FMK will also go true during the writing of the END OF FILE record.
(5) DATA BUSY goes false when the writing of the END OF FILE is completed.
(6) Tape motion ceases and FORMATTER BUSY goes false. The next operation may now be performed.

6.5 ERASING

Erasing is required when it is necessary to abandon a specific area of tape after repeated Write errors or to delete a specific record from tape. This can be accomplished by using one of the following methods:

(1) Fixed Length Erase
  (a) Set up interface for END OF FILE.
  (b) Set ERASE True.

6.5 ERASING (Cont.)

(c) Initiate GO. A fixed length of tape of approximately 3.75 inches will be erased.

(2) Variable Length Erase
- (a) Set up conditions for Write Forward.
- (b) Set ERASE true.
- (c) Initiate GO. Determine length to be erased by counting WRITE STROBES (no data will be written when ERASE is true).
- (d) Set LAST WORD true when desired length is reached. Formatter will complete erase function and stop transport.

(3) To delete a specific record on tape, the following sequence should be followed:
- (a) Set EDIT true.
- (b) Read the record in reverse (follow the sequence for Read Reverse) and determine the length of the record by counting READ STROBES (if the record length is not known).
- (c) Set up conditions for Write Forward (EDIT true).
- (d) Set ERASE true.
- (e) Initiate GO. Determine length to be erased by counting WRITE STROBES (no data will be written when ERASE is true).
- (f) Set LAST WORD true when desired length is reached. Formatter will complete erase function and stop transport.

6.6 EDIT

Editing is required when it is desired to change a particular record in the midst of many records. This function is a desirable feature for key-to-tape systems and for primary storage media. The Edit function serves two basic purposes, one of which is correct head positioning in the gap. The second is to slow the write current turn-off/turn-on to prevent a "glich" or noise transient in the gap. When performing an Edit function, the selected record must first be read in the reverse direction. This provides for optimum head positioning for the subsequent Write operation. The new record to be written must be of the same length to ensure maintenance of IBM compatible IBGs.

To perform an EDIT function, the following procedure should be followed:

(1) Read Forward over the record to be edited.

6.6 EDIT (Cont.)

(2) Set EDIT true.
(3) Set WRITE/READ false.
(4) Set REVERSE/FORWARD true.
(5) Initiate GO. Determine the length of the record by counting READ STROBES (if the record length is not known).
(6) Set WRITE/READ and EDIT true (when FORMATTER BUSY goes false).
(7) Set REVERSE/FORWARD false.
(8) Initiate GO.
(9) Set LAST WORD true when the last character of the new record is set up. Formatter will complete function and stop.
(10) Subsequent operations can be performed as desired.

6.7 READ OPERATION

Reading can take place in either the forward or reverse direction. Remotely selectable read thresholds ensure that no write errors have occurred during a previous write operation. As an example, for single gap transports, READ THRESHOLD 1 under the customer's control is used to select the high threshold when it is desired to read a record that has just been written. For dual gap transports, the threshold selection is an automatic function. On all systems, the capability of an extra low read threshold for data recovery is provided through the interface line READ THRESHOLD 2.

Read threshold levels are set to ensure that when data is written on tape, its remanence is above 30 percent nominal amplitude. On subsequent read operations, the threshold or clip level is reduced to 10 percent to ensure data recovery. The extra low threshold for data recovery selects 5 percent as the read level.

The PE formatter provides three-character deskewing capability, automatic data correction for a single track dropout, removal of the preamble and postamble, END OF FILE detection, and forward/reverse Read capability. The data output of the formatter is decoded and is presented in parallel form to the interface. This data is transmitted to the user's equipment on READ DATA interface lines.

Another interface line, READ STROBE samples the READ DATA lines. This waveform consists of a pulse for each data character read from tape.

6.8 READ FORWARD

The following sequence of events will take place when reading a record. Typical waveforms are shown in Figure 3.

(1) Transport must be Ready.

(2) Establish Forward Read conditions.
   (a) Set WRITE/READ false.
   (b) Set REVERSE/FORWARD false.

(3) Initiate GO. Conditions established in Step 2 are initiated on the trailing edge of the GO pulse. FORMATTER BUSY is set true.

(4) DATA BUSY goes true when the tape has reached approximately 80 percent of rated speed. DATA BUSY can be used to gate READ STROBES.

(5) Read data should be sampled by the READ STROBES. HARD ERROR/CORRECTED ERROR indicates that a data error has occurred and normal read recovery techniques should be used (i.e., re-read, change threshold levels, etc.).

(6) DATA BUSY goes false when the check character(s)/postamble is past the read head and the post record delay has been completed.

    DATA BUSY going false can be used to trigger the next GO command and can be used for reading "on-the-fly". This technique should be used only when repeating the same operation (i.e., writing or reading in the same direction).

(7) FORMATTER BUSY goes false when tape motion has ceased.

6.9 READ REVERSE

Read Reverse is implemented in a manner similar to Read Forward. However, the order of the data characters will be reversed. The only difference between Read Forward and Read Reverse operations is that REVERSE/FORWARD is set true.

6.10 FILE MARK DETECTION

The formatter detects file marks in both the forward and reverse directions. The presence of a File Mark is indicated on the status line FMK.

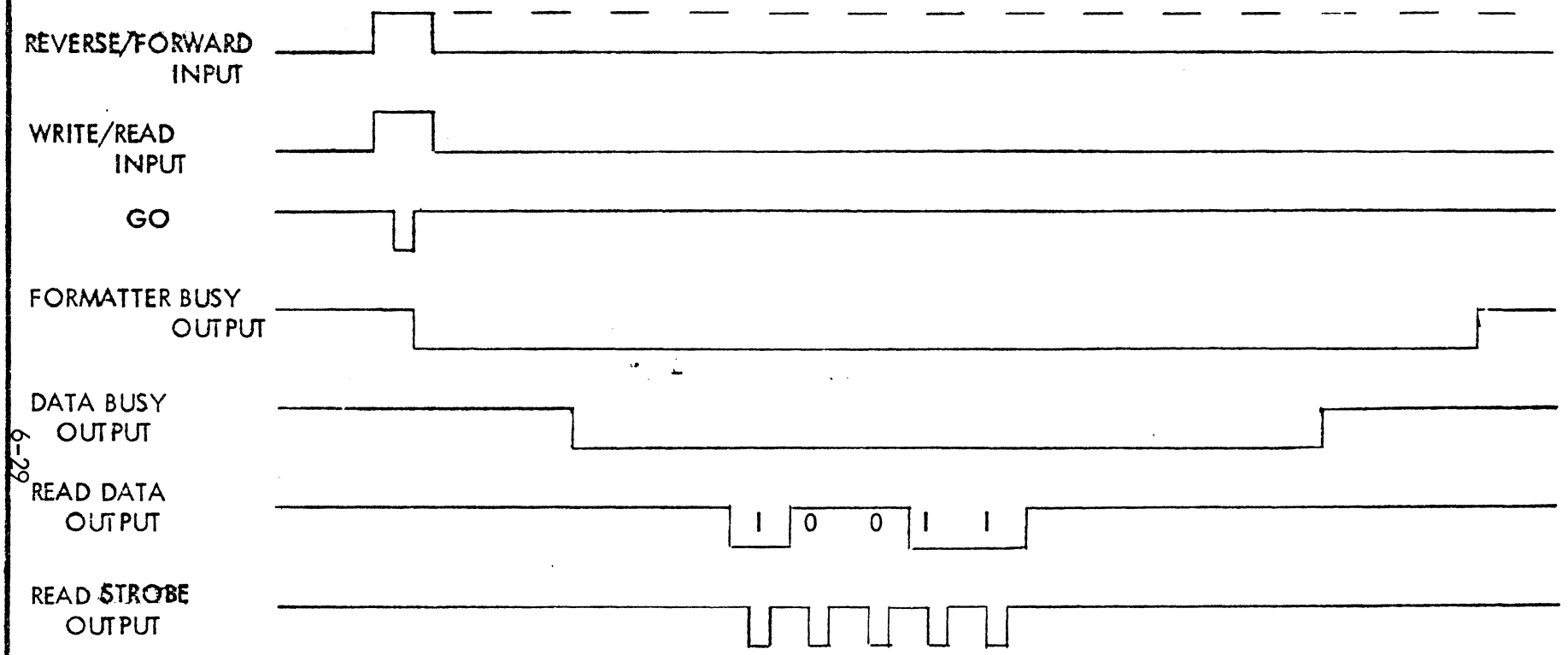

Figure 3 Read Operation Timing Diagram

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OUTRIGGER BOX ADDENDUM

1. GENERAL

The outrigger box (OB) is a 5 1/4"H x 19"W x 22"D rack mountable chassis employed to house and power interface electronics.

2. INPUT POWER REQUIREMENTS

At time of manufacture, the OB is normally configured to satisfy one of the following input requirements:

1. 117VAC, 60Hz
2. 117VAC, 400Hz
3. 230VAC, 50Hz

Input current requirements are a function of the type and number of interfaces powered by the OB. In general, 117VAC machines are fused at 2.5A and 230VAC at 1.25A. The fuse is accessable from the front panel.

3. FRONT PANEL

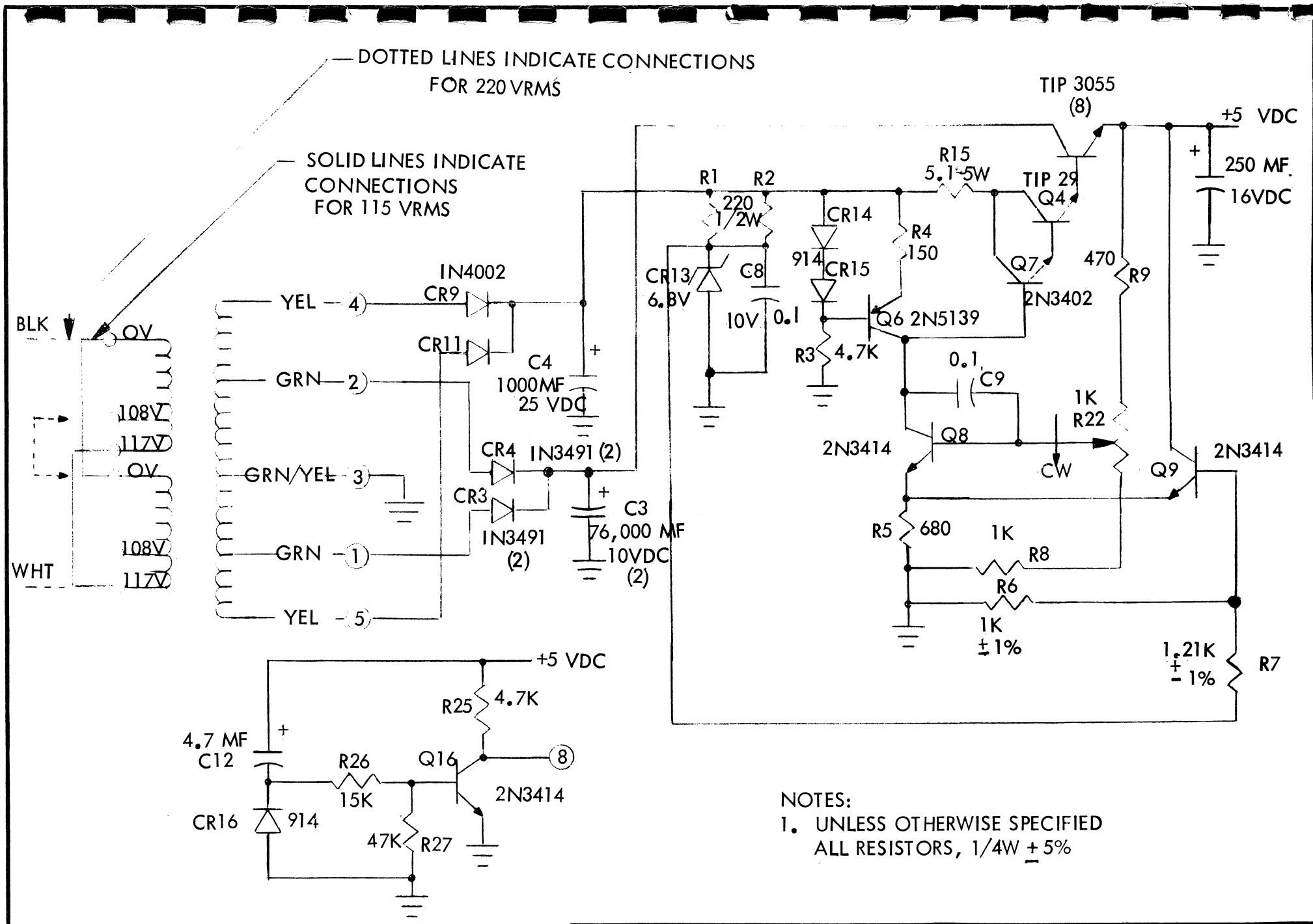
The front panel supplied is a function of the type of interfaces configured within the OB. All panels provide a switch/indicator assembly to power the box and a fuse-holder. Refer to the appropriate interface manual for a description of additional switches/indicators which may be supplied.

4. DC POWER SUPPLIES

Power supply components are located in the area directly behind the front panel. The input AC line is applied to a step down transformer. The transformer drives the rectification, filtering, and voltage regulation circuits which are mounted on the RD-03 printed circuit board. When fully loaded (as dictated by the interface power requirements), +5VDC @ 12A, -5VDC @5A, and -12VDC @ .75A are provided by series pass regulators. A potentiometer is provided in the resistive sampling network of each regulator for adjustment purposes. Additionally, the RD-03 board contains a power-up clear circuit which is utilized to provide a clear signal to interface boards as required.

5. INTERFACE CAGE

Directly behind the power supply assembly is the card cage and cage wiring required to power and interconnect 17"W x 15"D interface assemblies. Cage wiring is a function of the type and number of interfaces within the OB. Refer to MC-0064. Generally, power bussing and interconnection between boards of a multi-board interface are provided. Interconnection between levels of interface are accommodated at the rear of the OB, externally, using cabling supplied at the time of manufacture.



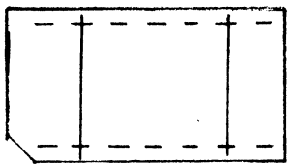
NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS, 1/4W ± 5%

+5VDC SUPPLY	DIGI-DATA CORPORATION
A A	SHEET 1 OF 1

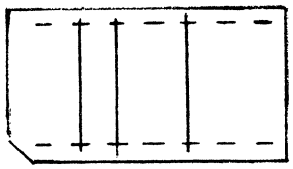
DRAWINGS

SPEED

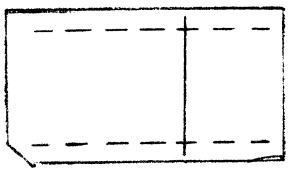
1 2 4 8 16



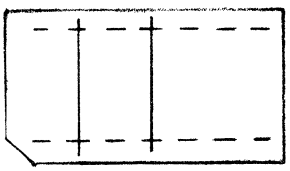
12.5 IPS



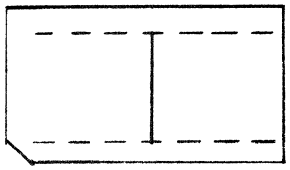
18.75 IPS



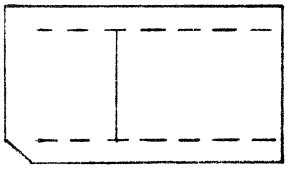
25 IPS



37.5 IPS



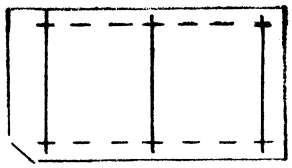
45 IPS



75 IPS

DENSITY

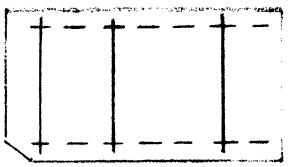
1 2 3 4 5 6 7



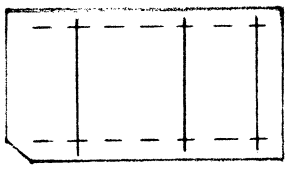
9-TRK

NOTE:
JUMPERS ARE 20 AWG BUSS

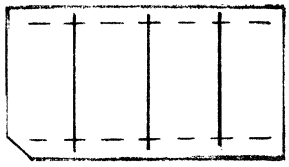
7-TRK



800/556



556/200



800/200

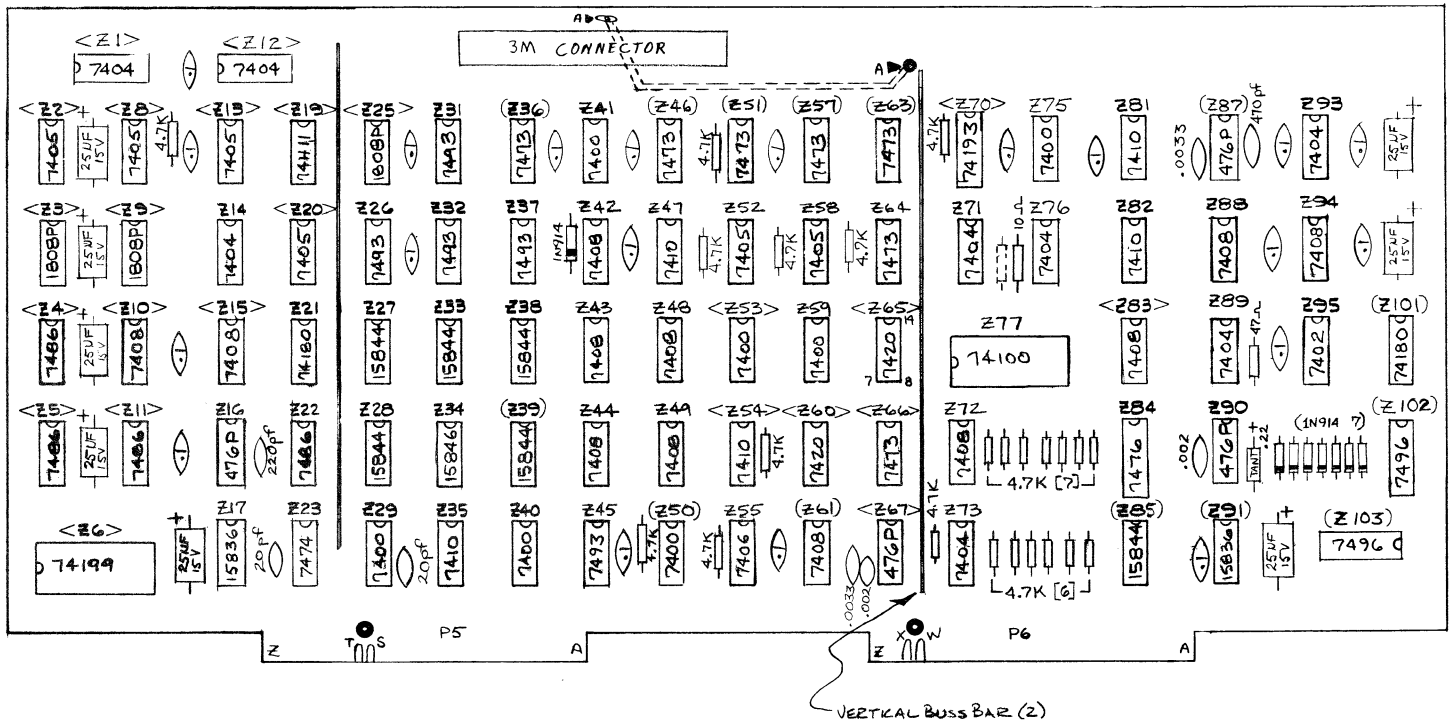
B	JUMPERS CHANGED TO 5V NRZI		
A	75 IPS ADDED JAI 6/18/13		

DIGI-DATA CORPORATION

SHEET 1 OF 1 | CA-0032

NRZI FORMATTER
PLATTER OPTIONS

REV	DATE	INIT.	REMARKS
	2/15/74	ejg	EXTENSION OF OBSOLETE NF-5



UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS IN OHMS, 1/4W, ± 5%.
2. CAPACITORS IN MFD UNLESS OTHERWISE NOTED, ± 10%.
3. INSTALL HORIZONTAL JUMPERS BETWEEN LIKE-NUMBERED HOLES, (1 TO 1, 2 TO 2, 3 TO 3, ETC.) BEFORE INSTALLING VERTICAL BUSS BARS.
4. JUMPERS NUMBERED 1 THROUGH 6 ARE #30 AWG WIRE-WRAP WIRE.
5. JUMPER "A" IS #16 AWG, INSULATED, TO BE INSTALLED AS SHOWN ON THE NON-COMPONENT SIDE OF PC BOARD.
6. SOLDER BUSS BAR PINS ON BOTH SIDES OF PC BOARD.
7. ● = SOLDERED FEEDTHROUGH.

NOTES:

1. FOR READ ONLY UNITS INSERT A 4.7K RESISTOR BETWEEN PINS 10 AND 14 OF POSITION 65.

( ) DELETE FOR WRITE ONLY UNITS.

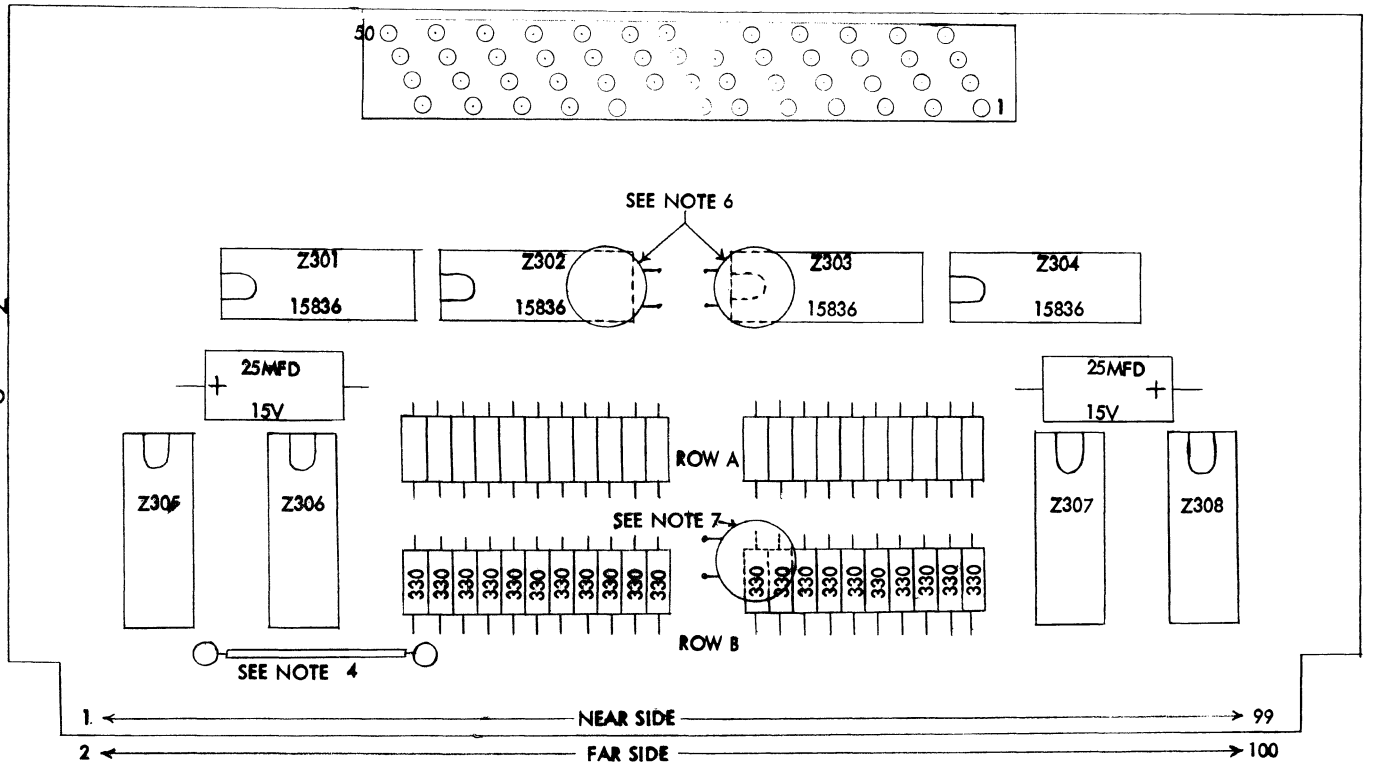
< > DELETE FOR READ ONLY UNITS.

PRINTED CIRCUIT CARD ASSY NF-6	DIGI–DATA CORP.
2/15/74 ejg.	SHEET 1 OF 1 | CC-0150

NOTES:

IN-TRANSPORT	FOR OUTRIGGER
1. Z5-Z8 ARE 7404	1. Z5-Z8 ARE 7406
2. ROW "A" RESISTORS ARE 4.7K	2. ROW "A" RESISTORS ARE 220
3. OMIT ROW "B"	3. INSTALL ROW "B" AS SHOWN
4. INSTALL JUMPER AS SHOWN	4. OMIT JUMPER

5. DWG # LB-0029B SHOWS HOW THE 3M CONNECTOR IS TO BE ASSEMBLED.
6. CAPACITORS (.1 MFD) ARE INSERTED IN THE BOARD AND BENT OVER THE IC'S AS SHOWN IN FIGURE 1.
7. THIS CAPACITOR (.1 MFD) IS PLACE IN THE BOARD AS IN NOTE 6, EXCEPT THAT THE CAPACITOR IS BENT OVER RESISTORS.



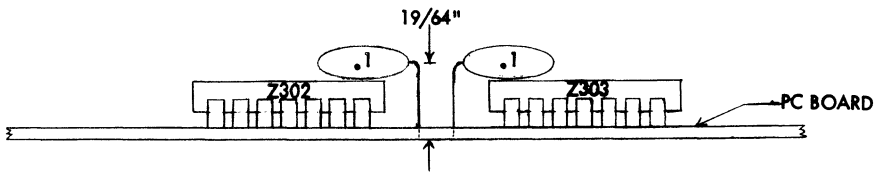
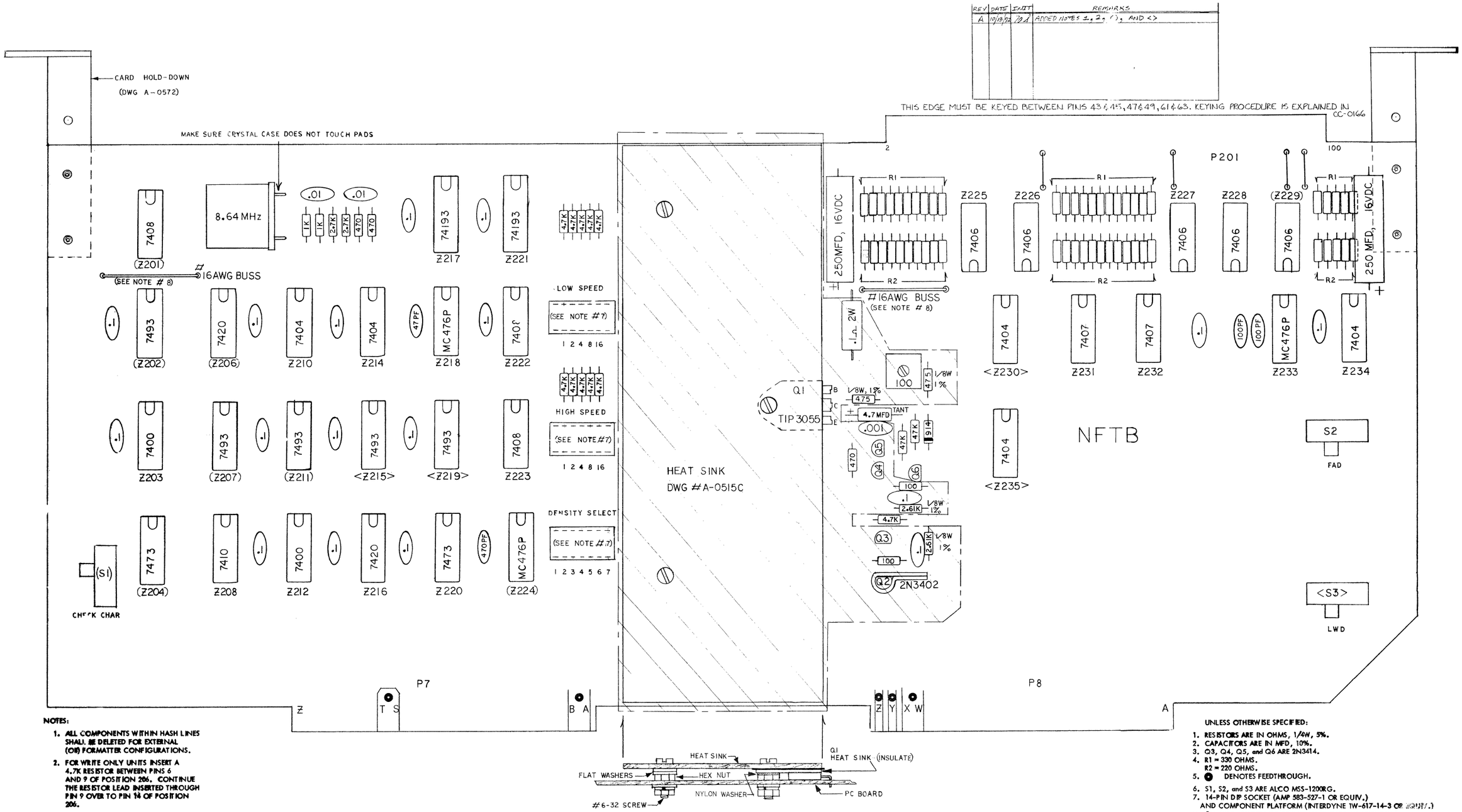


FIGURE 1

ASSEMBLY NFTC-2	DIGI-DATA CORPORATION	
E.J.O.	SHEET 1. OF 1.	CB-00968

REV	DATE	APPT	REMARKS
A	10/18/72	JDA	ADDED NOTES 1, 2, ( ), AND < >



NOTES:

1. ALL COMPONENTS WITHIN HASH LINES SHALL BE DELETED FOR EXTERNAL (OEM) FORMATTER CONFIGURATIONS.
2. FOR WRITE ONLY UNITS INSERT A 4.7K RESISTOR BETWEEN PINS 6 AND 9 OF POSITION 206. CONTINUE THE RESISTOR LEAD INSERTED THROUGH PIN 9 OVER TO PIN 14 OF POSITION 206.

( ) DELETE FOR WRITE ONLY UNITS.

< >, DELETE FOR READ ONLY UNITS.

UNLESS OTHERWISE SPECIFIED:

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. CAPACITORS ARE IN MFD, 10%.
3. Q3, Q4, Q5, and Q6 ARE 2N3414.
4. R1 = 330 OHMS.
   R2 = 220 OHMS.
5. ● DENOTES FEEDTHROUGH.
6. S1, S2, and S3 ARE ALCO MSS-1200RG.
7. 14-PIN DIP SOCKET (AMP 583-527-1 OR EQUIV.) AND COMPONENT PLATFORM (INTERDYNE 1W-617-14-3 OR EQUIV.)
8. #16 AWG JUMPERS TO BE INSTALLED DURING CHECKOUT.
9. DISCRETE COMPONENTS AND JUMPERS TO BE SOLDERED ON BOTH SIDES OF PCB WHERE APPLICABLE.
10. OPTIONS WILL BE SELECTED DURING CHECKOUT.

ASSEMBLY, NFTB-4 REV B	DIGI-DATA CORP.	
9-15-72	SHEET 1 OF 1	CD-0011

A	ARTWORK REVISION	9/15/72
B	ECN 0102	5-30-73
C	NF-6 CHANGE	10-26-73
D	ECN-0170	8/9/73

* JUMPERS ARE 10Ω, LOADED AS FOLLOWS:

12.5 IPS	= 17	(480 KHz)
18.75 IPS	= 11	(720 KHz)
25.0 IPS	= 8	(960 KHz)
37.5 IPS	= 5	(1.44 MHz)
45.0 IPS	= 4	(1.728 MHz)
75.0 IPS	= 2	(2.88 MHz)

DIGI DATA CORP

NRZI FORMATTER CONTROL CKTS

LD-0001 1 OF 3 D

A	ARTWORK REVISION 9/15/72 JJ

TAPE SPEED CLOCK

HI DEN

TTR

200 SELECTED

556 SELECTED

800 SELECTED

F WRITE

ASZ

7-3 5-C

.0033

.002

+5V

4.7K

FEOF

FERASE

RESET F&O

ASYNC

SYNC

LWD

8-M 6-11

8-V 6-18

S3

F WRITE

ASI

AS

WDO

WD1

WD2

WD3

WD4

WD5

WD6

WD7

WP/C

GATE WP/C

ODD

EVEN

WARS

WDS

END CC WRITE

WDP/C

WD7/1

WD6/2

WD5/4

WD4/8

WD FEVEN

WD2/B

WD1

WDO

CRP

CR7

CRO

CR1

CR2

CR3

CR4

CR5

CR6

CR7

FAD

FEOF

TTR

DIGI-DATA CORP.

NRZ I FORMATTER
WRITE CKTS

LD-0001 2OF3

A ARTWORK REVISION 9/15/76

RDS 101-76 +5V 220 330 304 AS2 94 PRESET RREG 87 76 75 470 PF FDATA COMPLETE 93 RCLK PULSE 2 CLR RREG 88 61 75 87 .0033 RCLK PULSE 1 5-L 7-10 210 223 RESET 202 214 225 201 201-29 FMK 224 225 201-27 MER 206 ALLOW 7-8 5-J DATA ABSENT 51 7-6 5-F BLANK 203 7-C 5-3 226 201-31 CCG AS 470PF 228 201-73 RSTR 7-12 5-N

RDP +5V 4.7K 64 58 RCLK PULSE 2 AS2 TAPE SPEED CLOCK 200 SELECTED 556 SELECTED 800 SELECTED 208 211 207 220 212 216 204 52 5-E 7-S

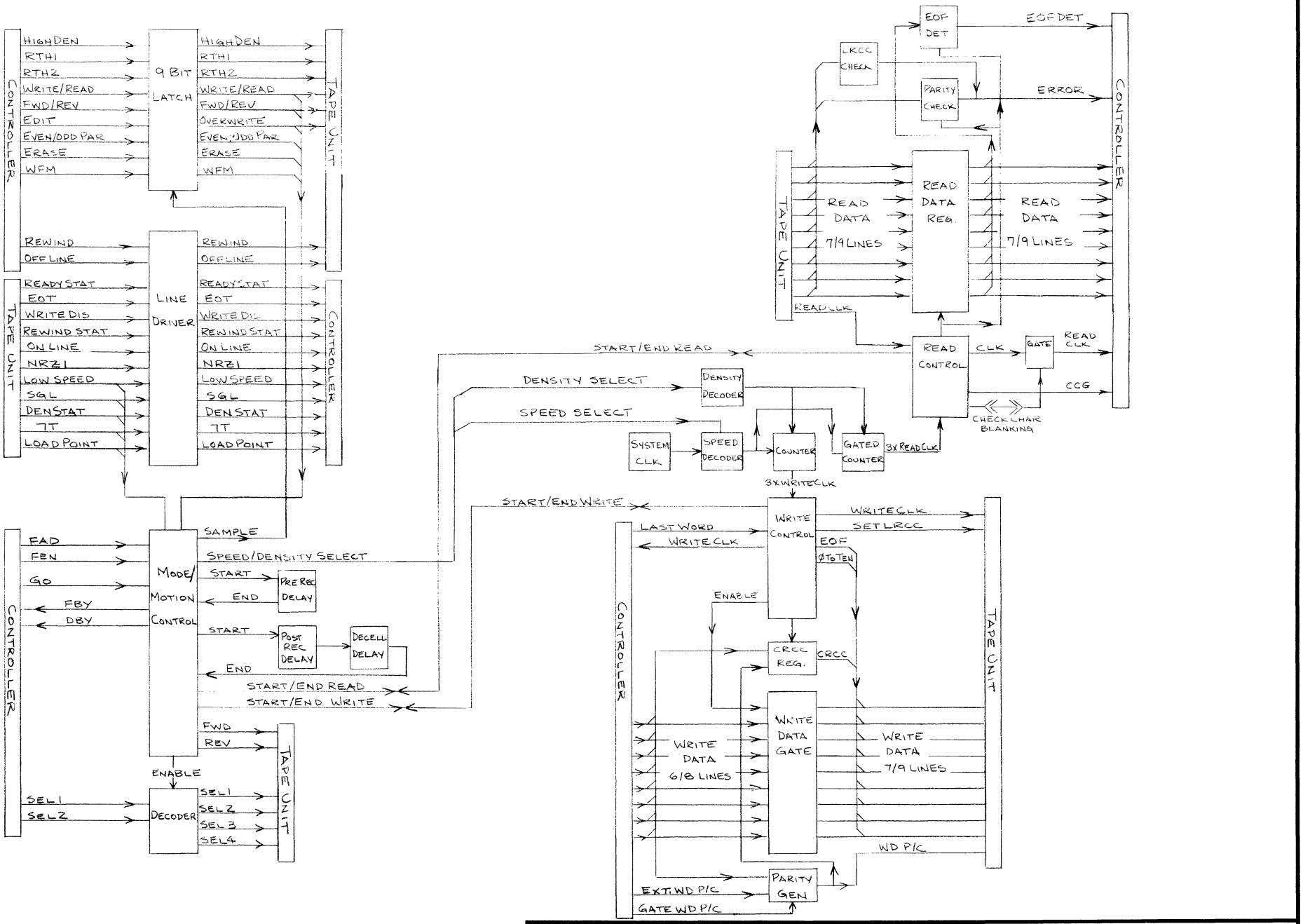
RCLK PULSE 1 AS1 +5V 6-L 8-10 7TR FRD FRDP 89 91 85 IN914 (7PL)

RD P/C 101-54 220 330 303 RDP 103 102 7/1 6/2 5/4 4/8 3/A 2/B 1 0 +5V CLOCK PRESET CLEAR 6-K 8-9 6-J 8-8 6-H 8-7 6-F 8-6 6-E 8-5 6-D 8-4 6-C 8-3 6-B 8-2 6-A 8-1 229 201-91 RP/C R7/1 R6/2 R5/4 R4/8 R3/A R2/B R1 R0

PRESET RREG CLR RREG RDP ∑ ODD 101 EVEN ODD EVEN IN ODD IN 22 50 61 FFORWARD 5-H 7-7

36 41 42 47 73 AS1 5-D 7-4

NRZI FORMATTER
READ CKTS
LD-0001 3 OF 3



BLOCK DIAGRAM
NRZI FORMATTER

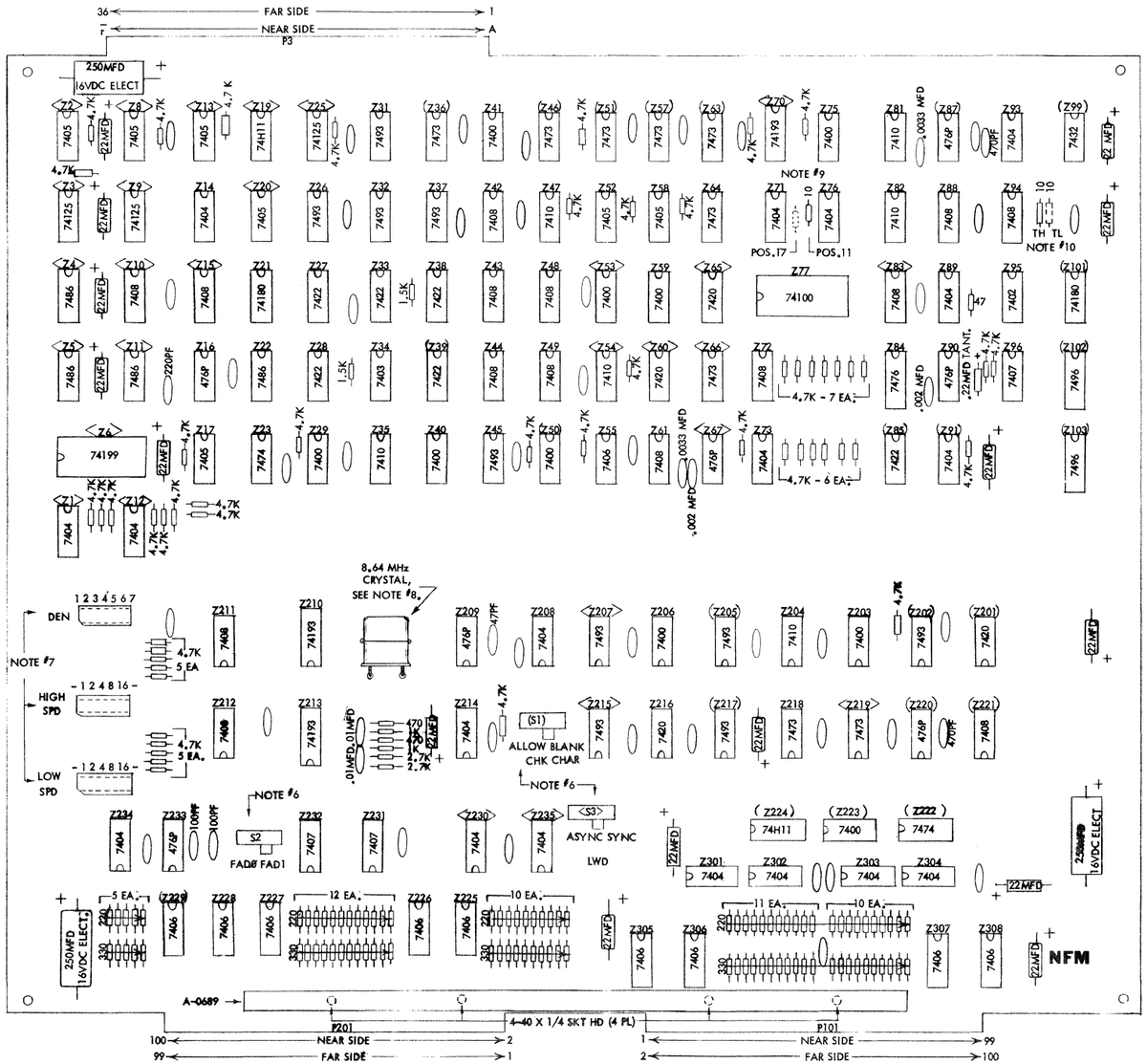
JJ 2-18-72

DIGI–DATA CORP.

SHEET 1 OF 1

LC - 0119

VERSION TABLE
SPEED PLATFORM OPTIONS:
12.5 IPS — 18.75 IPS
25 IPS — 37.5 IPS
45 IPS — 75 IPS
DENSITY PLATFORM OPTIONS:
200/556 BPI — 200/800 BPI
556/800 BPI — 9-TRK ONLY
JUMPERS ARE #20 AWG BUSS



NOTES:
1. ( ) DELETE FOR WRITE-ONLY UNITS.
2. < > DELETE FOR READ-ONLY UNITS.
3. ALL RESISTORS ARE IN OHMS, 1/4W ± 5%.
4. ALL UNSPECIFIED DISC CAPACITORS ARE .1 MFD ± 10%.
5. 22 MFD CAPACITORS ARE ELECTROLYTIC, 16VDC.
6. S1, S2, AND S3 ARE ALCO MSS-1200RG.
7. 14-PIN DIP SOCKET (AMP 583-527-1 OR EQUIV.) AND COMPONENT PLATFORM (INTERDYNE 1W-617-14-3 OR EQUIV.) SEE VERSION TABLE AT FAR LEFT FOR ASSEMBLY OF PLATFORMS.
8. CRYSTAL: BULOVA, HC-33/U, 8.640MHz, ±.005% TO BE SECURED TO THE PC BOARD WITH #22 AWG BUSS AS SHOWN, SOLDERED ON THE FAR SIDE.
9. WITH 10 OHM RESISTOR INSTALLED AS SHOWN IN POSITION 11, THE FORMATTER WILL NOT ACCEPT A "GO" FROM THE CONTROLLER DURING THE DECELERATION DELAY.

   WITH THE 10 OHM RESISTOR INSTALLED IN POSITION 17, THE FORMATTER WILL ACCEPT A "GO" ANYTIME AFTER DBY GOES FALSE.
10. DEN TRUE COMMANDS HIGH DEN WITH TH RESISTOR AND LOW DEN WITH TL RESISTOR.

REVISION		DATE	INIT.
A	PRODUCTION RELEASE	6/7/74	JJI

FINISH 4/10/74	DIGI-DATA CORP.
SCALE 1X	
DRAWN [illegible]	ASSEMBLY — NFM
APPR	SHEET 1 OF 1 PC-D00053

8.640 MH

* JUMPERS ARE LOADED AS FOLLOWS:

12.5 IPS	= 17	(480 KHz)
18.75 IPS	= 11	(720 KHz)
25.0 IPS	= 8	(960 KHz)
37.5 IPS	= 5	(1.44 MHz)
45.0 IPS	= 4	(1.728 MHz)
75.0 IPS	= 2	(2.88 MHz)

TAPE SPEED CLOCK

LOW SPEED

GO

FEN

FAD

EDIT

DEN

THR 1

THR 2

ERASE

PAR

WFM

WRT

REV/FWD

TAD 0

TAD 1

WINDOW

STOP TAPE

GATED GO

FGO

RESET FGO

DELAYED FGO

FORMATTER UP

POWER UP P3-31

NRZI

F DATA COMPLETE

SINGLE GAP

LOAD POINT

DATA ABSENT

END CC WRITE

F FORWARD

F WRITE

FEDIT

7 TR

7 TR 1

REW

NRZI/PE

EOT

LPT

SPEED

DDI

DIGI-DATA CORP.	
NRZI FORMATTER NFM CONTROL CKTS	
LD 0012	1 OF 3

TAPE SPEED CLOCK

HI DEN

7 TR

DENSITY JUMPERS ARE INSTALLED AS FOLLOWS:

DENSITIES	1	2	3	4	5	6	7
800/556, 7T	X		X			X	
556/200, 7T		X			X		X
800/200, 7T		X		X		X	
9T	X			X			X

200 SELECTED
556 SELECTED
800 SELECTED

FWRITE

AS2

.0033

.002

+5V 4.7K

7TR1

101-26 WARS

101-24 WDS

END CC WRITE

FEOF

FERASE

RESET FGD

LWD

ASYNC

SYNC

201-57

220

330

232

FWRITE AS1

201-71 WSTR

W7/1 (LSB)

W6/2

W5/4

W4/8

W3/A

W2/B

W1

W0

201-19

201-17

201-15

201-13

201-11

201-9

201-7

201-5

WD P/C

101-80 WD P/C

96 WD 7/1

94 WD 6/2

92 WD 5/4

90 WD 4/8

88 WD 3/A

86 WD 2/B

84 WD 1

82 WD 0

GATE W P/C

201-20

W P/C

201-3

7TR1

FAD

FEOF

7TR

WD0

WD1

WD2

WD3

WD4

WD5

WD6

WD7

EVEN

ODD

PARITY GEN

AS

CR7

CRP

CRO

CR1

CR2

CR3

CR4

CR5

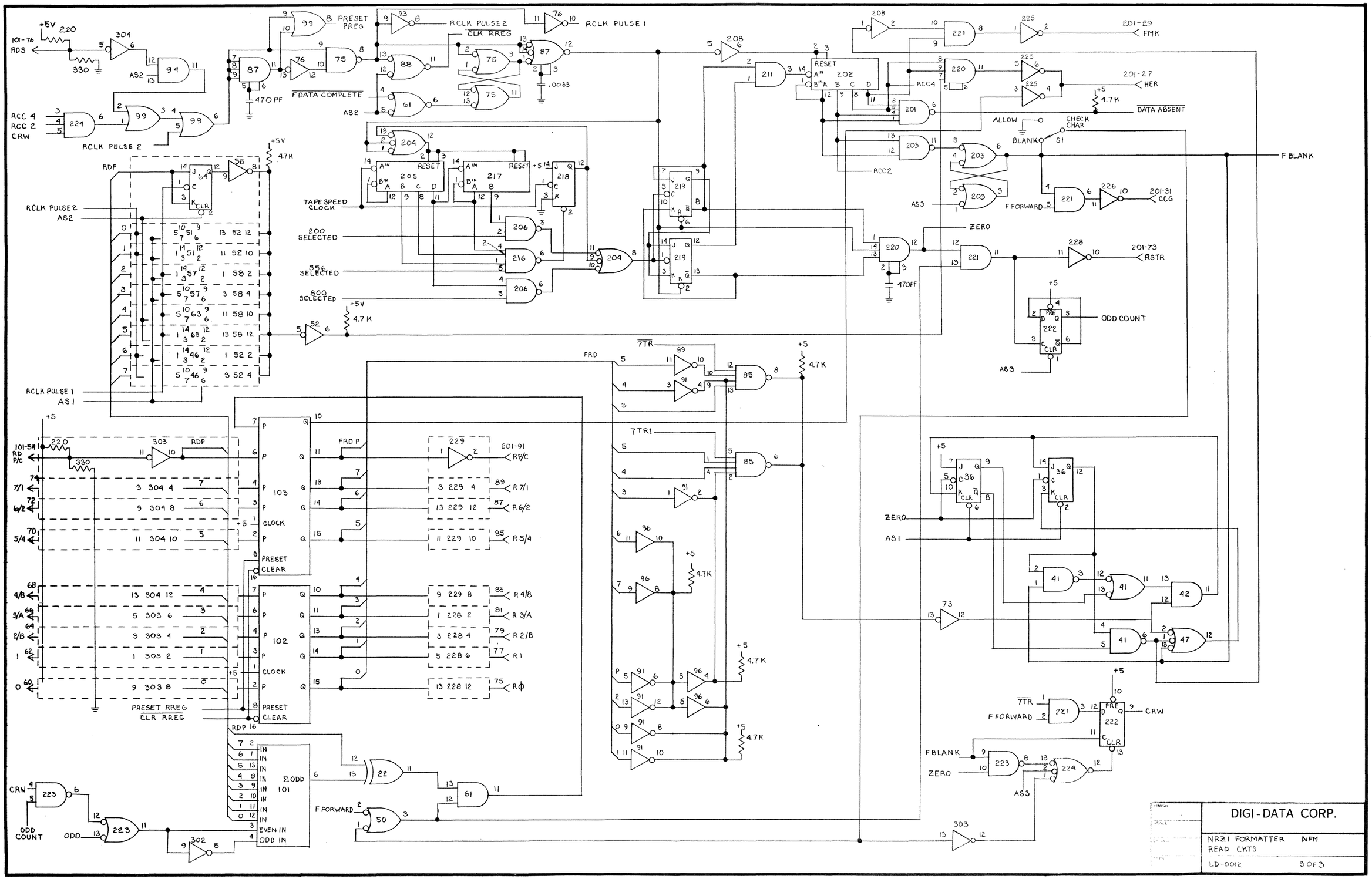
CR6

4.7K

+5

DIGI-DATA CORP.

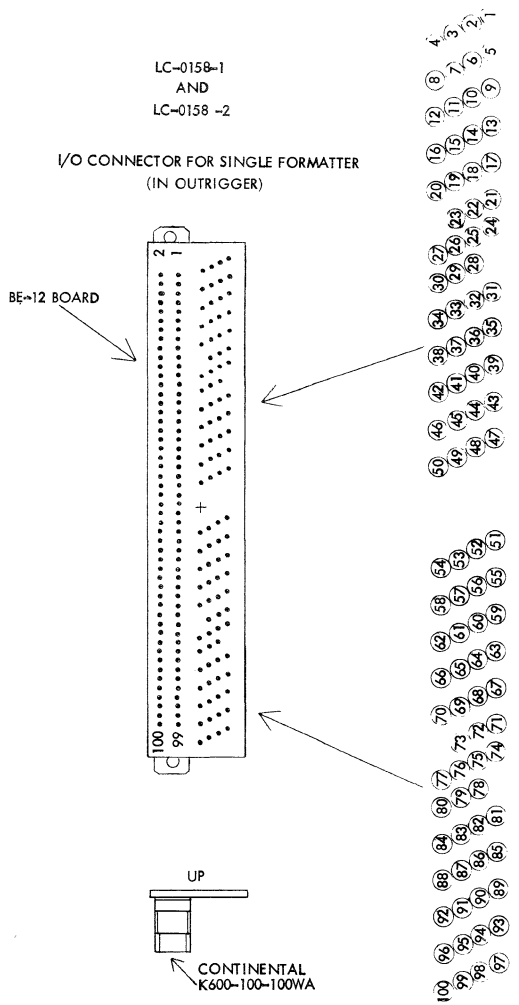
NRZI FORMATTER NFM
WRITE CKTS
LD-0012 2 OF 3



	DIGI-DATA CORP.
	NRZI FORMATTER NFM READ CKTS
	LD-0012 3 OF 3

LC-0158-1
AND
LC-0158 -2

I/O CONNECTOR FOR SINGLE FORMATTER
(IN OUTRIGGER)



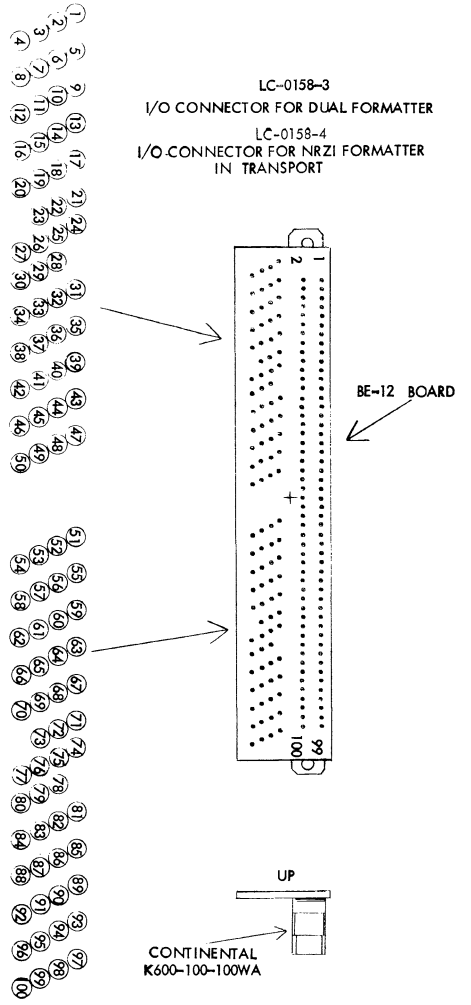
LOCATIONS OF SIGNALS:

1	+5	47	REV/FWD
3	WP/C	49	OFL
5	WØ (MSB)	51	REW
7	W1	53	TAD 1
9	W2/B	55	TAD 0
11	W3/A	57	LWD
13	W4/8	59	FPT
15	W5/4	61	LPT
17	W6/2	63	EOT
19	W7/1 (LSB)	65	NRZI
20	GATE WP/C	67	SGL
21	FBY	69	SPEED
23	DBY	71	WSTR
24	IDENT	73	RSTR
25	DEN STAT	75	RØ (MSB)
27	HER	77	R1
28	CER	79	R2/B
29	FMK	81	R3/A
31	CCG	83	R4/8
32	7 TR	85	R5/4
33	RDY	87	R6/2
35	ONL	89	R7/1 (LSB)
37	RWD	91	RP/C
39	THR2	93	FEN
40	THR1	95	FAD
41	ERASE	97	GO
43	EDIT	99	PAR
44	WFM	100	DEN
45	WRT	ALL OTHER NUMBERS ARE CONNECTED TO GROUND	

KEYING:
K600-100-100WA CONNECTOR MUST BE KEYED IN THREE PLACES. KEYING PROCEDURE IS EXPLAINED IN CC-0166.
LC-0158-1: (FOR NRZI FORMATTER) KEYING IS BETWEEN PINS 43 & 45, 47 & 49, 61 & 63.
LC-0158-2: (FOR PE FORMATTER) KEYING IS BETWEEN PINS 47 & 49, 57 & 59, 61 & 63.

LC-0158-3
I/O CONNECTOR FOR DUAL FORMATTER

LC-0158-4
I/O CONNECTOR FOR NRZI FORMATTER
IN TRANSPORT



KEYING:
K600-100-100WA CONNECTOR MUST BE KEYED IN THREE PLACES KEYING PROCEDURE IS EXPLAINED IN CC-0166.
LC-0158-3: (DUAL FORMATTERS) KEYING IS BETWEEN PINS 39 & 41, 53 & 55, 61 & 63.
LC-0158-4: (NRZI IN TRANSPORT) KEYING IS BETWEEN PINS 43 & 45, 47 & 49, 61 & 63.

FORMATTER CUSTOMER I/O CONNECTORS

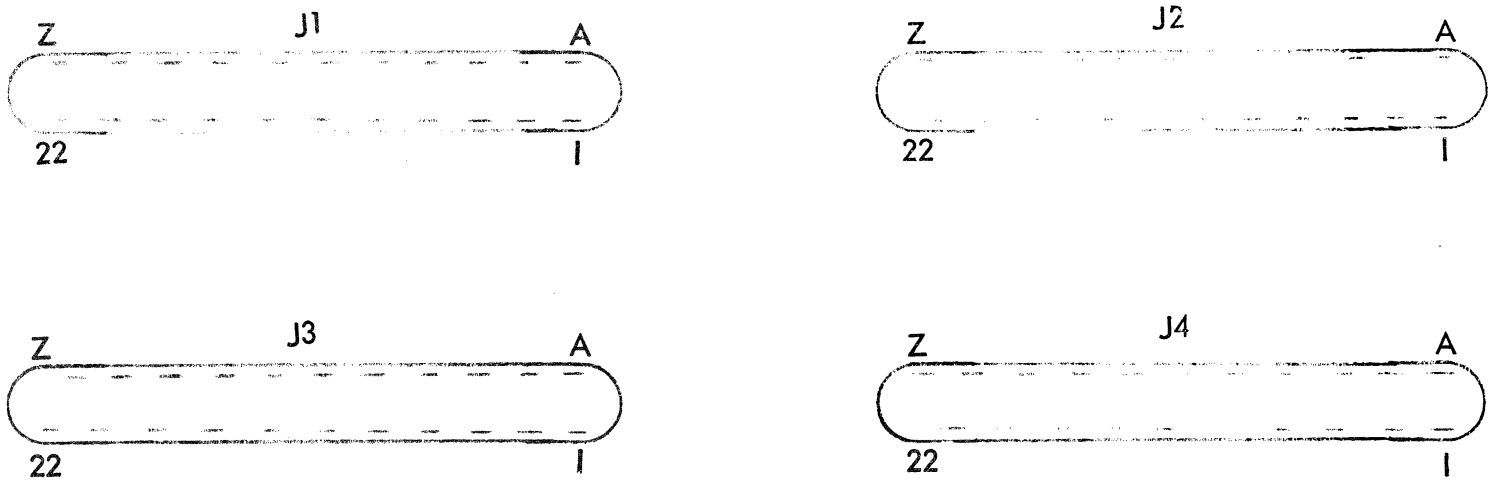
DIGI-DATA CORP.

REVISION B 4/8/74

SHEET 1 OF 1

LC-0158

OCE-ELLIOTT, INC., PGH., PA. REORDER 10-20697A



WIRING SIDE VIEW

ALL CONNECTORS CINCH 5044A30
OR EQUIVALENT

NRZI OUTRIGGER CONNECTOR ORIENTATION	DIGI-DATA CORPORATION
	SHEET 1 OF 3 — Wh-0168

ITEM	FROM	TO	WIRE	ROUTING	REFERENCE
	OR +5	J1 - S, T	#16 AWG	BLU	+5
	OR GND	J2 - W, X		BLK	GND
	J2-W	J2 - 19; J4 - W, 19		BUSS	GND
	J2-X	J2 - 20; J4 - X, 20		BUSS	GND
	J1-S	J1 - 15, J3 - S, 15		BUSS	+5
	J1-T	J1 - 16, J3 - T, 16	#16 AWG	BUSS	+5
	J2-1	J4 - A		BUSS	RO
	2	B			R1
	3	C			R2
	4	D			R3
	5	E			R4
	6	F			R5
	7	H			R6
	8	J			R7
	9	K			RP
	10	L			F P/S ERR
	11	M			FDD
	12	N			TAD 9
	13	P			SG L
	14	R			THR 2
	15	S			DE SEL
	16	T			FAR CYL
	17	U			WFM
	18	V			W R
	J1-3	J3 - C		BUSS	EX WRITE CLK
	4	D			/EOF DET
	5	E			LR REG OUT
	6	F			CC BLANK
	7	H			READ CLK EN
	8	J			/DATA ADJUST
	9	K			TAPE SPEED CL
	10	L			HEAD CLK DL
	11	M			LOAD SPEED
	12	N			HEAD CLK CO
	13	P			
	14	R			WS
	17	U			CFL
	18	V			DM
	19	W			
	20	X			
	21	Y			

NOTES:

EXTERNAL NRZI OUTRIGGER WIRING LIST 8-16

DIGI-DATA CORP.

WA-0168 **WIRING LIST**

REV A

ITEM	FROM	TO	WIRE	ROUTING	REFERENCE
	J1-22	J3-Z		BUSS	WP
	J2-A	J4-1		BUSS	
	B	2			
	C	3			GO
	D	4			LDP
	E	5			RDY
	F	6			ONL
	H	7			RWD
	J	8			EPT
	K	9			EOT
	L	10			NRZ
	M	11			ASYNC
	N	12			THD 1
	P	13			THR 1
	R	14			WRITE
	S	15			EDIT
	T	16			ERASE
	U	17			REVERSE
	V	12			SYNC
	J1-C	J3-3		BUSS	F BLANK
	D	4			7 TRACK
	E	5			
	F	6			
	H	7			
	J	8			
	K	9			
	L	10			
	M	11			
	N	12			
	P	13			HIGH DEN
	R	14			FBY
	U	17			REW
	V	18			GATE WP
	W	19			W6
	X	20			W4
	Y	21			W2
	Z	22			W1

NOTES:

EXTERNAL NRZI OUTRIGGER WIRING LIST

DIGI-DATA CORP.

WH-0168 **WIRING LIST**

REV. A CHANGED J1-S - J3-14 TO J1-R / J3-14 SHEET 3 OF 3

8-17