AEON
SUITE MSB 1855 S. PEARL DENVER , COLORADO
(303) - 777 - AEON 80210

USART
COMMUNICATIONS CARD

THE DIGITAL GROUP USART COMMUNICATIONS CARD

Have you been waiting to interface your micro-computer to remote hardcopy terminals, or to transmit data over telephone and communication lines? Well, your wait is over! The Digital Group adds data communication to the growing list of features of our computer system, with the addition of a USART communications card.

The communications card provides the capabilities of asynchronous and synchronous data transmission with up to four half- or full-duplex double buffered channels. Utilizing LSI programmable USART communication interface chips (8251's) reduces the amount and complexity of processor software overhead as well as increasing communication speeds. The 8251 USART can be programmed by the CPU to operate utilizing virtually any serial data transmission technique presently in use (including IBM Bi-sync). It does not handle SDLC. The USART chip does parallel-to-serial, serial-to-parallel data conversions, data stream formatting, and transmits status and control information between the processor and the peripheral device.

Each communication channel may be individually programmed for transmission rates of up to 9.6K baud (Asynchronous Mode) or up to 56K baud (Synchronous Mode). Sync definition, async baud rates, character lengths, sync or async mode selection, break character generation, and error detection parameters are set by the processor via a command word to an enabled 8251 USART chip. Each 8251 also provides control inputs and outputs for modem control signals, and for those signals used for transmitter and receiver control.

The communications card was designed to plug directly into an I/O slot in a Digital Group system, but may also be used as a port driven card with other system configurations. The card requires +5V, and ±12V DC for operation. Circuitry for port addressing, data buffering to and from the CPU, and crystal-stabilized clocking is provided on the card. The card uses RS-232-to-TTL level conversion chips (1489's) for interfacing modem and terminal signals; RXD, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, and external sync signal SYNDET. TTL-to-RS-232 level conversion chips (1488's) are provided for 8251 output signals; TXD, $\overline{\text{RTS}}$, $\overline{\text{DTR}}$, and internal sync signal SYNDET. One 20ma current loop transmitter circuit is provided on the card for transmitting to a TTY or similar device.

The card uses a 4 MHz crystal, clock signal divided by two for 8251 internal clocking operations. For baud rate clocking signals, an on-board frequency divider network, requiring no tuning, provides eight jumperable baud rate frequencies.

System Description

The communications card may be used with any of the currently available 8-bit microprocessors. The communications card plugs directly into an available I/O bus slot (22-pin and 36-pin dual edge connectors required). Port addressing on the card uses the port address lines on the I/O bus 22-pin connector, and is jumper selectable to any group of eight sequential port addresses. The card uses two output ports and two input ports: one output port for command and mode instructions, one output port for data words, and one input port each for reading status and assembled data words. Voltages of +5V and ±12V are provided by the I/O bus. For non-Digital Group system applications, these must be provided to the 22-pin card connector.

Connections for each channel's output and input signals are made to pins or "fingers" on the 36-pin card connector. Documentation provided includes a technical description of the communications card operation, assembly instructions, a schematic and parts placement diagram, information on programming and operating the communications card, and a guide to cabling and connections to communication devices. A list of publications and reference materials is also included to provide data communication information. The communications card's flexibility allows it to be used in practically all micro-computer data communication applications. If you have a specific application to consider and need additional information, or have problems or questions concerning the card, we suggest that you write or call The Digital Group.

USART Communication Card Specifications

Card Dimensions: 12" x 5.4" vertical, including fingers.

System Requirements:

Power: +5V for TTL, 8251 circuit operation
±12V for RS-232 1488 line drivers
Microcomputer requirements:
Microprocessor: Digital Group system or other supplying 8 bit I/O ports
8 port address lines; group or 8 sequential port addresses used
$\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ strobe lines; 8 data to I/O lines, 8 data from I/O lines

Data Handling Capabilities:

- Full duplex, double buffered, transmitter and receiver
- Error detection — parity, overrun, and framing error
- Transmitter control lines — TXRDY, TXEmpty, $\overline{\text{TXC}}$
- Receiver control line — RXRDY, $\overline{\text{RXC}}$, SYNDET
- Modem control lines — $\overline{\text{RTS}}$, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$
- Asynchronous transmission (DC to 9.6K baud)
  - 5 to 8 bit character lengths
  - Clock rate — software selectable to 1x, 16x, 64x baud rate (1x not recommended for asynchronous receiver mode)
  - Break character generation — 1, 1½, 2 stop bits
  - False start bit detection
- Synchronous transmission (DC to 56K baud)
  - 5 to 8 bit character lengths
  - Internal or external character synchronization
  - Automatic sync character insertion

Card Features

- Port address decoding — jumper selectable for group of 8 port addresses
- Data bus buffers — input and output data lines to and from CPU buffered
- Baud rate — jumper selectable for each 8251 USART utilized, 4 MHz on-board crystal used for clock base and 3 IC frequency divider
- Up to four 8251's per card
- RS-232 to TTL level shifters available:
  - 4 RS-232-to-TTL lines available per USART chip
  - 4 TTL-to-RS-232 lines available per USART chip
  - 1 - 20ma current loop circuit available
- Control lines $\overline{\text{RD}}$, $\overline{\text{WR}}$, C/$\overline{\text{D}}$, $\overline{\text{CS}}$
- TXE, TXRDY, RXRDY, SYNDET available as external I/O pins or as status register bits. Allows either polled I/O operation or interrupt-structured operation.

Technical Description — Communications Card

The communications card is intended to aid interfacing a micro-computer to peripheral devices such as remote CRT and hardcopy terminals, and to format and serialize data for transmission over communication lines. The card itself plugs directly into an available I/O slot of a Digital Group system, using the I/O bus for data and port address lines. Connection to external peripherals or devices are made to pins on the card's 36-pin edge connector.

The card interfaces the CPU's parallel data environment with those lines required by peripheral devices. The card also functions to transmit and receive data, using programmable frame and character generation. Command, status, and control logic are transmitted between the CPU and peripheral device by an 8251 USART interface chip. These logic signals include standard modem and RS-232 level signals used for both status input and control output. Status and data information is input to the CPU via the I/O data bus. Status and control signals between the peripheral and the communications card are transferred via connections to the card's 36-pin dual edge connector. Connections to the card may be made to the peripheral via the CPU backplane connector and adjoining cable, or may be made directly to the peripheral.

The circuitry on the communications card carries out port address decoding, buffering of data to and from the CPU, clocking, and baud rate frequency generation. Four 8251 programmable communication interface chips communicate between peripherals and the CPU, and transmit and receive data. TTL-to-RS-232 level shifting chips (1488's) are used for sending RS-232 level signals. RS-232-to-TTL level shifters (1489's) convert incoming RS-232 level signals to TTL logic levels.

Port address decoding is carried out by using IC26 (74154, 1 of 16 decoder), IC10 (7402, two input NOR gates), and IC25 (7442, 1 of 10 decoder). Eight port address lines are input to the communications card yielding 256 port addresses. Four port address lines, (MSB-3 through MSB), are input to IC26 (74154) and a jumper on one of 74154's outputs designates a group of 16 addresses for the card. A jumper installed on the LSB+3 address line selects either the lower or upper group of eight from the 16 addresses for the card. Two address lines (LSB+1, LSB+2) are input to IC25 (7442) to select one of the four 8251 USART chips on the card. An active low signal from IC26 is gated through IC17 with an active low signal from IC25 and enables one of the 8251s. The LSB is connected to the $C/\overline{D}$ line on each 8251 chip and determines whether the information on the data bus is a control word or a data word.

Data bus lines to and from the CPU are buffered using IC15 and IC16, and IC23 and IC24. An output strobe on pin X of the card's 22-pin connector enables the buffers of IC23 and IC24 and passes data from the CPU to the data lines of the 8251s. Data sent to the CPU from the data lines of the 8251s is gated through IC15 and IC16 with an input strobe accompanying a valid card port address from IC18, and a READ strobe on pin 11 of the I/O bus.
Clocking on the card originates with a 4MHz crystal input to a clock dividing network of IC5, IC6, and IC9. A 2MHz clock is input from IC6 to each 8251 and is used for internal clocking operations. This clock frequency is required to be a minimum of 4.5 times the desired baud rate for asynchronous mode transmission and 30 times a desired baud rate for synchronous mode transmission. The network of IC5, IC6, and IC9, provides jumperable frequencies to control baud rates from 110 baud to 9600 baud. External clock sources optionally may be used in place of the frequency divider network to supply a baud rate clock to each of the 8251's.

Programming the Communications Card

The major activity on the card occurs within the 8251 interface chips. An applications manual from one of the manufacturers (8251s supplied by NEC, INTEL, AMD, NATIONAL) for the 8251 is provided in the documentation. Figures 1 and 2 show the organization of the 8251 and the flow of data between peripherals and the CPU. The 8251 USART is user-programmed to transmit or receive data asynchronously or synchronously, at a baud rate and with a defined frame character selected by the user. Sample programs are included which indicate programming sequences used.

The 8251 has a data bus of eight bits that receives commands and data from the CPU and sends data and status information to the CPU via buffered I/O bus data lines. The card is addressed as an I/O port, using input or output instructions from the processor to read or write data. The LSB address line, making an even or odd I/O address, signals the 8251 as to whether data or control information is being transmitted or received. An odd address (LSB1) is used for transmitting control instructions to the 8251, and reading a status word from the 8251. An even address is used for data input and output (LSB=0).

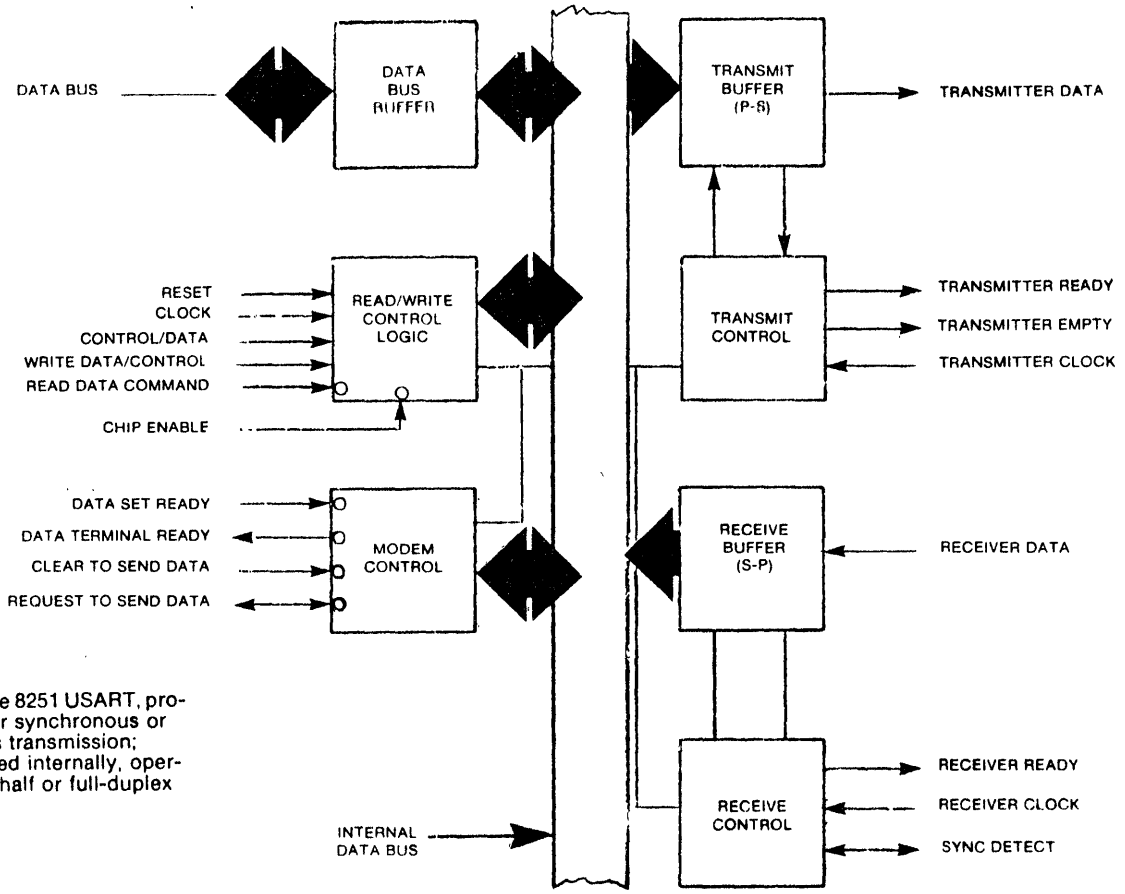


Figure 1 — The 8251 USART, programmable for synchronous or asynchronous transmission; double buffered internally, operates in either half or full-duplex mode.

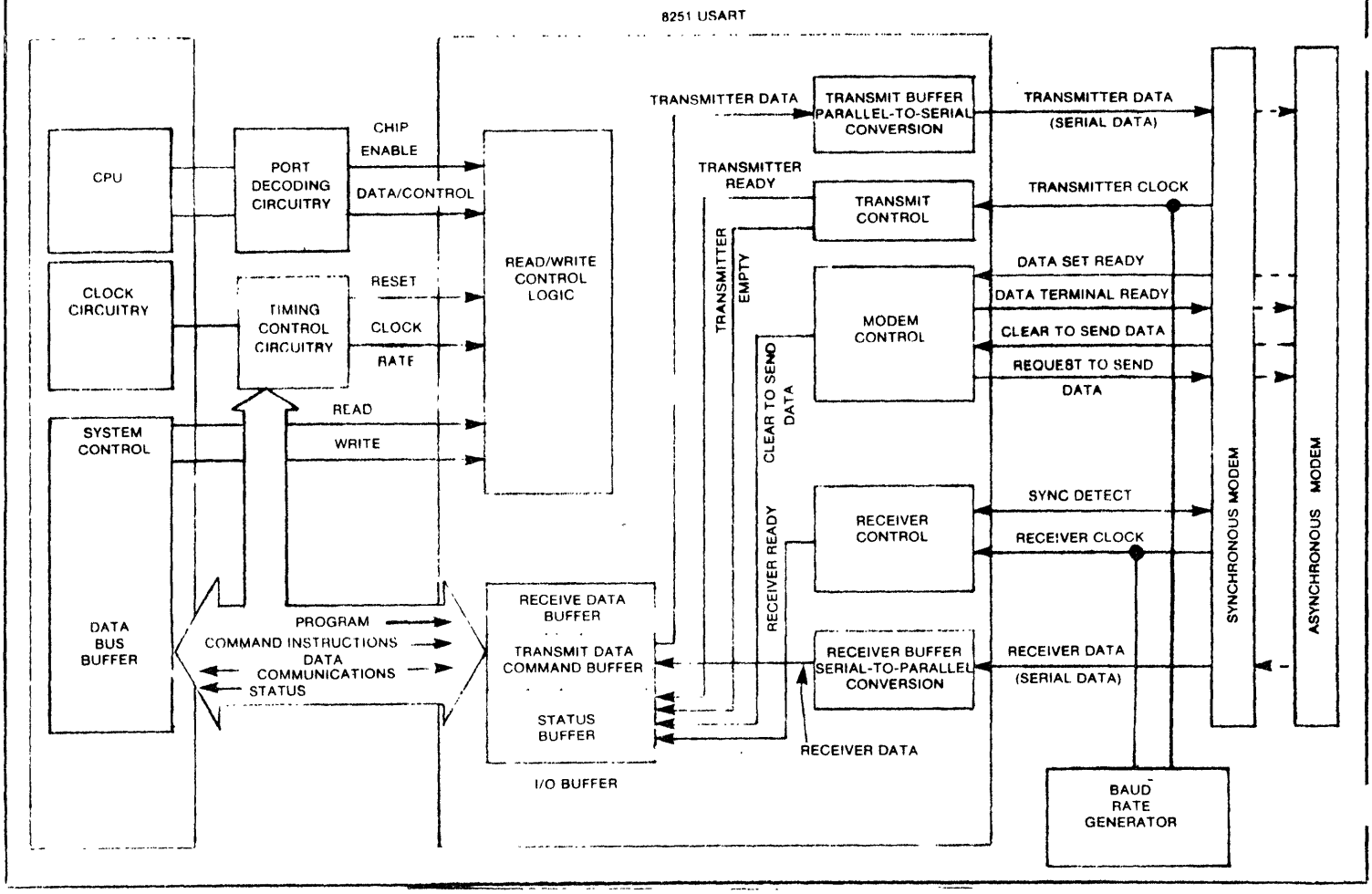


Figure 2 — 8251's implemented in a microcomputer system.

Four "handshaking" signal lines are available from each 8251: two inputs, $\overline{CTS}$ (clear to send) and $\overline{DSR}$ (data set ready), and two outputs, $\overline{RTS}$ (request to send) and $\overline{DTR}$ (data terminal ready).These signal lines are intended for modem control applications. Of the four lines, only one, $\overline{CTS}$, is required for the 8251 to operate. Using RS-232 input levels, a logic "0" RS-232 level (+12V), must be connected to the line receiver input (1489) for each 8251 used. This "low" on the input pin of the 8251 enables the 8251 to transmit data (serial), if the TXEN bit in the command byte is set to a "1". The state of $\overline{RTS}$ and $\overline{DTR}$ can be set from bits in a command word. The state of $\overline{DSR}$ can be checked with a bit from a status read word. In a typical application of the system (8251) with an RS-232 peripheral device or terminal, a request to send signal from the terminal would be connected to the $\overline{CTS}$ input on the 8251, a data terminal ready signal (from peripheral) would connect to the $\overline{DSR}$ input on the 8251. To provide the proper "handshaking" signals for a modem or peripheral device, check the literature supplied with the device for proper sequencing and signal line connections.

Control line logic signals on the 8251 provided are $\overline{RD}$,$\overline{WR}$, C/$\overline{D}$, $\overline{CS}$. The $\overline{RD}$ line is usd to read data from the CPU while the $\overline{WR}$ signal sends data to the CPU. The C/$\overline{D}$ line indicates to the 8251 whether data, control, or status information is on the data bus. The $\overline{CS}$ line of each 8251 is selectively brought low by port decoding logic, so only one device is turned on at a time.

The external reset line on the 8251 is disabled and is tied to ground. An internal reset (setting a bit in a command word) can be used by sending a sequence of four control words (**00**1) followed by a reset command of **10**0 (octal).

Assembly

To build the Digital Group communication card you will need the following tools and equipment:

Fine-tipped low wattage soldering iron (approximately 25 watt)
Solder — 60/40 resin wire solder, 20-30 gauge
Do not use acid core solder!
Diagonal cutters — small micro shear type preferred
Long-nosed pliers
Flux remover or alcohol
Small brush

Before mounting components on the communications card inspect the printed circuit board, comparing it to the component-side layout diagram provided. Identify the component side of the board; the Digital Group label is located on the upper-left corner of the card. Check the areas under sockets to see that adjacent pads or traces are not shorted. Next, identify the components that will be used on the communications card, with the parts list provided. All resistors have standard color code markings bearing the value and tolerance of the resistors. All resistors used are 1/4 watt. Three types of capacitors are used: ceramic disc, tantalum, and silver mica.

Ceramic disc capacitors are flat and disc-shaped and are generally identified by a ceramic casing. There is no polarity or preferred direction. Tantalum capacitors used on this board are "tear-drop" shaped and have a value and polarity marking on the body of the capacitor. These must be installed with the polarity indicated on the layout. The mylar capacitor used on the card is rectangular-shaped, and the value marking is on the capacitor body. The voltage rating for capacitors on the parts list is the minimum rating required; capacitors supplied in the kit may have higher voltage ratings. When soldering components into the board make sure that your soldering iron is hot enough, is kept tinned, and is cleaned periodically with a sponge or similar material.

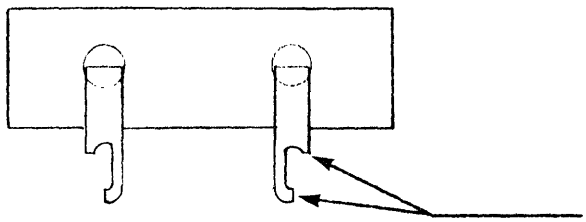
Most problems that occur with newly assembled boards are related to solder shorts or "splashes", improperly soldered connections ("cold" solder) or missed (unsoldered) pins. All IC's are socketed to avoid applying heat to "heat sensitive" IC's, and to aid possible repair. Do not bend IC socket pins excessively before soldering as pins may break underneath the sockets.

STEPS

If you have purchased a COMM-1 card, you will have received all components necessary for one channel. See the schematic and layout diagram to determine placement of components.

- ☐ Install and solder all IC sockets on the component side of the board. Sockets should be mounted as close to the board as possible: IC's 1 through 4 require 28-pin sockets. IC 26 requires a 24-pin socket. IC8, IC9 and IC25 require 16-pin sockets. IC5, IC6, IC7 and IC's 10 through 24 require 14-pin sockets.
- ☐ Next, install and solder R1 - R4 in the positions indicated on the layout diagram. Use the values as indicated in the parts list. Mount the resistors approximately 1/16 inch away from the board.
- ☐ Install and solder D1 with the polarity indicated on the layout diagram. The Diode is installed so the card may request wait states. While not needed with present microprocessors, this feature will accommodate faster CPUs such as the 4MHz Z80.
- ☐ Install and solder C5, C8, C9, C11, 1 mfd tantalum capacitors in positions indicated on the layout diagram, noting their polarity.
- ☐ Install and solder C2, a 50 pfd silver mica capacitor.
- ☐ Install and solder the six .01 mfd ceramic disc capacitors, C1, C3, C4, C6, C7, and C10, in position according to the layout diagram.
- ☐ Install and solder the crystal socket in the position indicated on the layout diagram, without the crystal in the socket. To make the crystal socket leads fit in the holes provided, cut the socket lugs as indicated below.

FIG. 3 - CRYSTAL SOCKET MOUNTING



- ☐ Install the 4 MHz crystal in the crystal socket on the board.
- ☐ Install all IC's in position, noting carefully the IC numbers on the layout diagram. Be careful not to bend any of the IC pins under when installing the IC's.

This completes assembly of the communications card. Check over all components on the card for correct positioning, and check over soldering. Jumpers must still be installed on the card for baud rates and port address selection. Also, depending on the application of the card, jumpers or special wiring must be installed. These are detailed in the operating and testing procedure to follow.

System Planning Steps

1. Designate ports, channels used, interface signal requirements, commands and mode instruction formats

2. Install appropriate jumpers on the communications card
   a. Baud rate jumpers for each 8251 (see Table 1)
   b. Port address jumpering — IC25 and IC26 (see Table 2 and Figures 5 and 6)
   c. Level shifting jumpers or modification to include 20ma current loop
   d. Use of control or status signals (modem control) for "handshaking logic: RXD, $\overline{CTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TXEmpty, TXRDY, RXRDY; polling I/O and interrupts are accommodated by the card. CTS must be used or connected to 12V to allow the 8251 to transmit.

3. Write programming (flow charts and sample listings included)
   a. Initialization routines
      1) Reset 8251 via command word — bit D6 set high
      2) Write a mode instruction
      3) Write sync characters if any (sync mode only)
      4) Write command instruction
   b. Operation routines
      1) Check status word via status register read or interrupt mode processing using external I/O pins on 36-pin edge connector (RXD, SYNDET, TXEMPTY, TXRDY, RXRDY, CTS, DSR)
      2) Input or output data or sync characters
      3) Check status; continue transmission or reset to input new mode or command instructions
   c. Program listings

4. Cabling, diagnostic testing and operation of the communications card

1. Designate ports, channels used, interface signal requirements, command and mode instruction formats.

Before installing jumpers on the communications card, decide on the application for the card, and determine the number of transmission channels that will be used. Refer to the literature supplied with a particular device for specification and requirements of "handshaking" and interface signals. Determine the modem control signals that will be used: $\overline{DTR}$, $\overline{DSR}$, $\overline{RTS}$, and $\overline{CTS}$. Modem control outputs $\overline{DTR}$ and $\overline{RTS}$ may be set via a command instruction. Modem control inputs $\overline{DSR}$ and $\overline{CTS}$ affect bits in the 8251's status register for polled I/O operation.

The user must designate an operating mode via a mode instruction word written into the 8251's. The mode instruction specifies sync or asynchronous operation, frame parameters, clocking rate, and error detection parameters. A command instruction word following a mode instruction controls the actual operation of the selected format. Port addresses must be designated for each 8251 for writing both data and control words to the 8251.

Programming the communications card requires routines to handle initialization of each transmission channel as well as monitoring all data transmissions. Initialization routines must internally reset the 8251 USART in use, and write a mode instruction which defines the operational characteristics of the 8251. Following the mode instruction, the processor must send out a command instruction as well as appropriate sync characters to control the actual operation of a selected format.

2. Install appropriate jumpers on the communications card.

a. Baud rate jumpering

The frequency divider network of IC5, IC6, and IC9 provide connection points for inputs to $\overline{RXC}$ and $\overline{TXC}$ of each 8251. Before installing jumpers for the 8251's calculate which baud rates will be used and the baud rate factor that will be used in the mode instruction. For synchronous transmission baud rate frequencies equal the clocking inputs at $\overline{RXC}$ and $\overline{TXC}$. For asynchronous transmission a choice is available between clock rates, 1x baud rate, 16x baud rate, 64x baud rate. Operating at 300 baud, asynchronously, with a baud rate factor (16x baud), a jumper would be connected to a frequency of 4800 Hz.

Table 1 lists calculated frequencies required for baud rate factors. Figure 4 shows the position of the baud rate frequencies and the connection points to $\overline{TXC}$, $\overline{RXC}$ on each 8251.

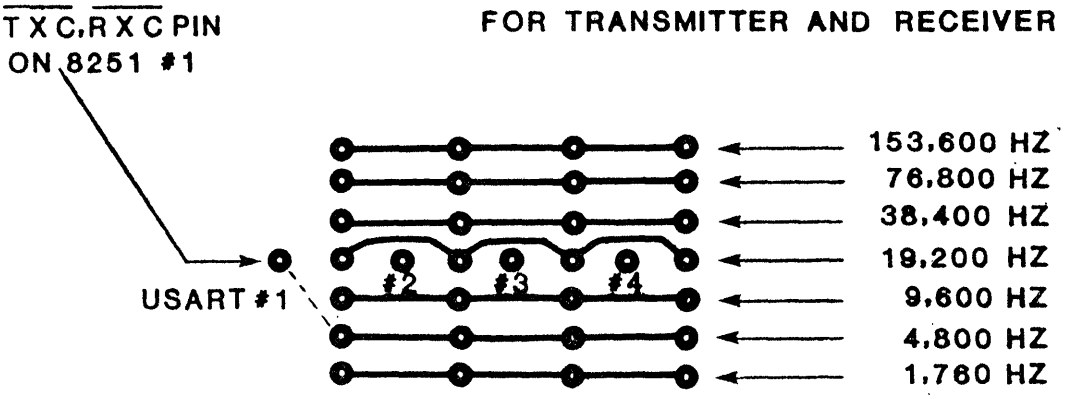
TABLE 1 — Clock Input Required at RXC, TXC for Selected Baud Rates

Baud Rate at TXD	Async Clock Input (TXC, RXC) 1x Baud Rate*	16x Baud Rate	64x Baud Rate	Sync Clock Input 1x Baud Rate
110 baud	—	1760 Hz	7040 Hz	110 Hz
150 baud	—	2400 Hz	9600 Hz	150 Hz
300 baud	—	4800 Hz	19,200 Hz	300 Hz
600 baud	—	9600 Hz	38,400 Hz	600 Hz
1200 baud	—	19,200 Hz	76,800 Hz	1200 Hz
2400 baud	—	38,400 Hz	153,600 Hz	2400 Hz
4800 baud	—	76,800 Hz	207,200 Hz	4800 Hz
9600 baud	—	153,600 Hz	414,400 Hz	9600 Hz

* (1x baud rate). Factor not recommended in asynchronous mode. Operation with 1x baud rate factor is unreliable.

EXAMPLE: $\overline{TXC}$, $\overline{RXC}$ CLOCK INPUT = BAUD RATE x 16 or 4800 Hz = 300 x 16.

FIG. 4 - BAUD RATE JUMPERING FOR TRANSMITTER AND RECEIVER CLOCKS



b. Port address selection

The port address example of Figures 5 and 6 shows the function of each bit of the I/O port address lines. Two jumpers must be installed which set a designation for addressing the communications card. Shown in Figure 5 are bit settings for addressing USART #1. USART #1 would be addressed by ports 16 & 17, USART #2 by ports 18 & 19, USART #3 by 20 & 21, and USART #4 by 22 & 23. See the schematic and layout diagram for jumper location.

With the port address shown, jumper 1 would be connected across the output at pin 2, which is selected output 1. Jumper 2 would be installed on the LSB + 3 address line in a non-inverting position. The LSB + 1 and LSB + 2 positions control which of the four 8251's is enabled. The LSB position selects control or data reading and writing to the 8251.

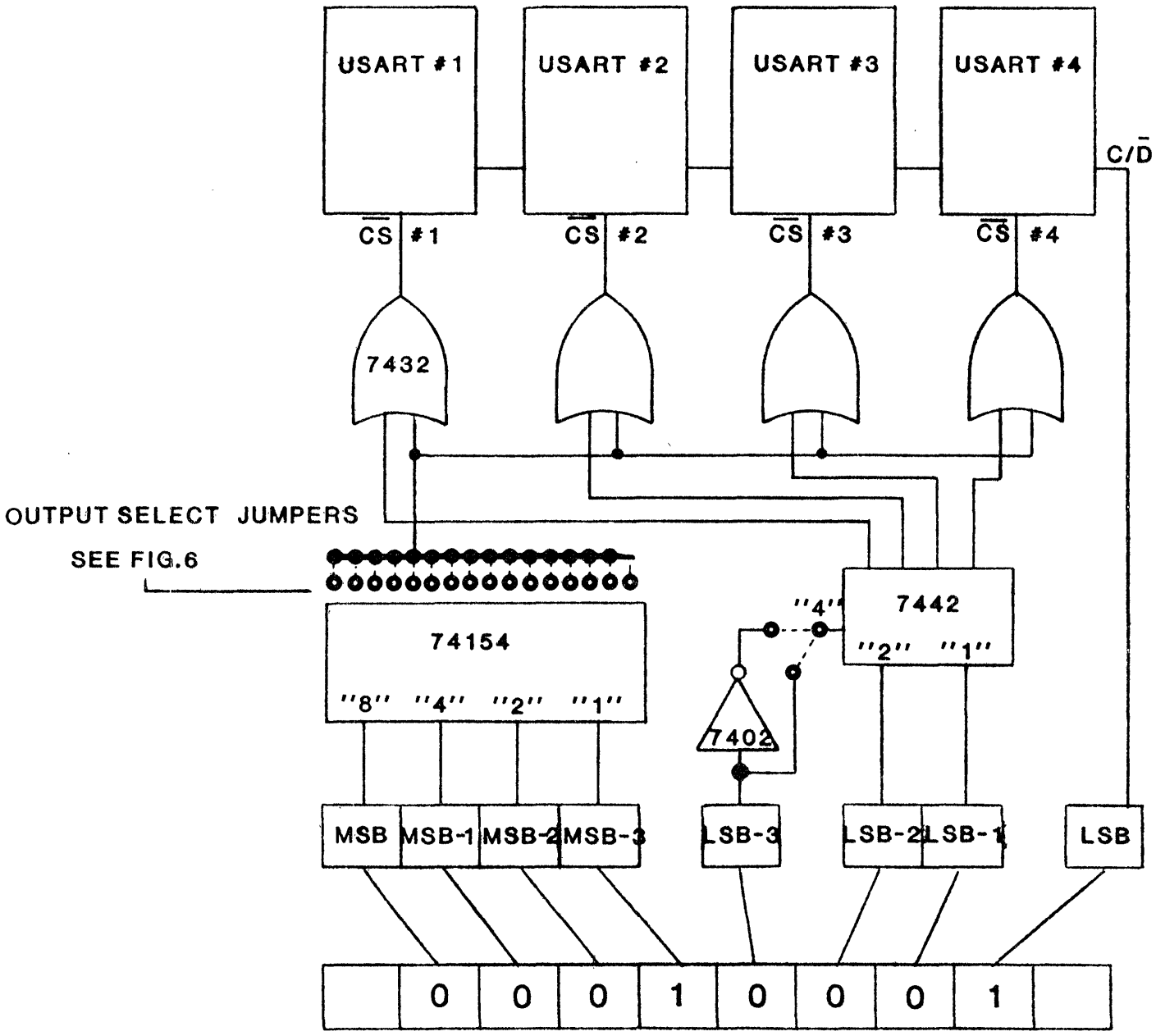


FIG. 5 -PORT ADDRESSING CIRCUITRY

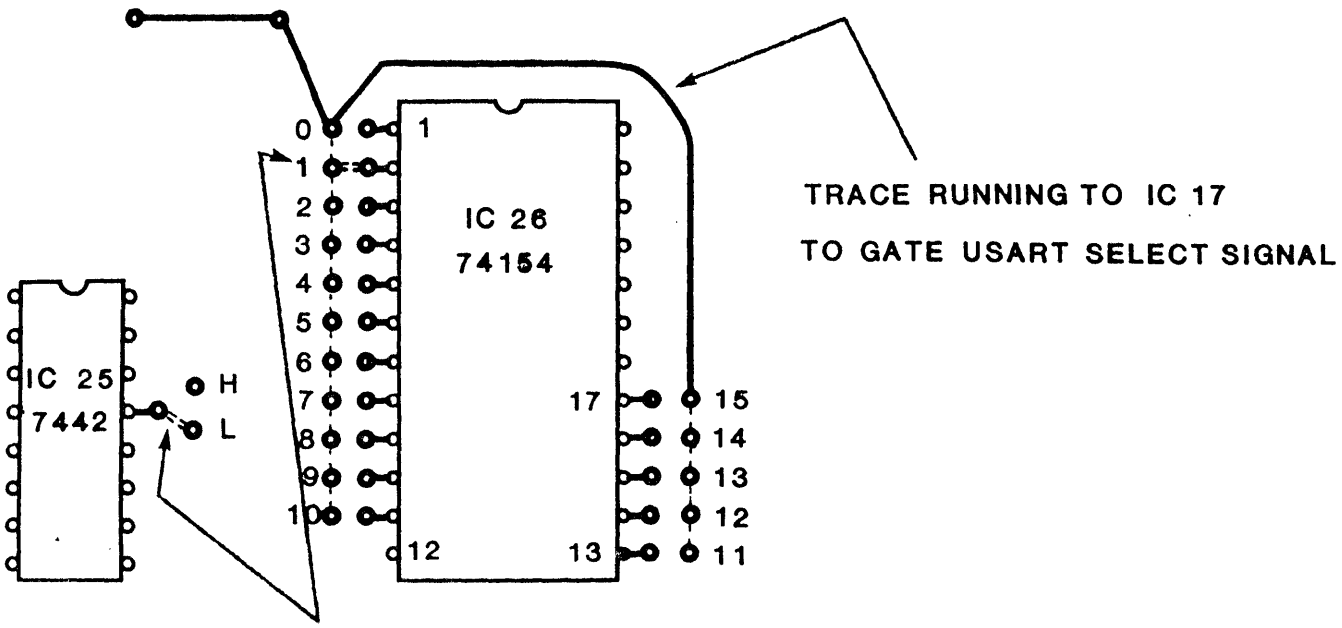


FIG. 6 - PORT SELECT JUMPERING

TABLE 2 — Valid Port Address Selection — Jumpers Installed on Outputs of IC26 and IC10

Card Port Addresses	IC10 Jumpered L	IC10 Jumpered H	IC26 Output Jumpered
0 - 15	0 - 7	8 - 15	0 - pin 1
16 - 31	16 - 23	24 - 31	1 - pin 2
32 - 47	32 - 39	40 - 47	2 - pin 3
48 - 63	48 - 55	56 - 63	3 - pin 4
64 - 79	64 - 71	72 - 79	4 - pin 5
80 - 95	80 - 87	88 - 95	5 - pin 6
96 - 111	96 - 103	104 - 111	6 - pin 7
112 - 127	112 - 119	120 - 127	7 - pin 8
128 - 143	.	.	.
144 - 159	.	.	(Pin 12 is GND)
160 - 175	.	.	.
240 - 255	240 - 247	248 - 255	15 - pin 17

Note: See the schematic diagram for listing of all port pin connections.

c. Level Shifting Line Drivers and Line Receivers

Line drivers used on the communications card are 1488 quad line drivers, IC11, IC13, IC19, and IC21. They require voltages of +5V, +12V and -12V to operate and convert TTL level signals to ±12V. A logic "one" (+5V) on an input is converted to a -12V output (RS-232 logic "one"). A logic "zero" (voltage less than .7V) input is converted to +12V output (RS-232, logic "zero"). The inputs to the 1488's are connected to 8251 signals TXD, $\overline{RTS}$, $\overline{DTR}$, and SYNDET. Outputs of the 1488's are brought out to the card's 36-pin dual edge connector. The pinouts of the 36-pin dual edge connector are shown in Figure 8.

Line receivers used on the communications card are 1489 quad line receivers, IC12, IC14, IC20, and IC22. They require +5V to operate and convert incoming RS-232 signals to TTL levels required by the 8251's. The inputs (from the 36-pin connector) to the 1489's are RXD, $\overline{CTS}$, and $\overline{DSR}$. A fourth line, for external syncing in synchronous mode, may be connected by a jumper connecting the fourth 1489 output to the SYNDET input pin on the USART chips. Jumperable pads are provided on the communications card and are located between the chips of the top row of level shifting chips (1488's and 1489's). These pads are also designated on the layout diagram.

The $\overline{CTS}$ line is of primary importance in using an 8251 for transmission. A +12V input (RS-232 logic "zero") can be tied to pins H, 7, Z, and 22 on the card's 36-pin dual edge connector to enable the $\overline{CTS}$ line of each 8251. Alternately these pins could be tied to the DTR line from a peripheral device. The 1489 converts the incoming +12V RS-232 level to a TTL "zero" on the $\overline{CTS}$ line which is required to enable the transmitter. One 20ma transmitter is available and can be jumpered to the transmitted output (TXD, pin 19) of any of the 8251's as designated on the layout diagram. The jumper pads are located in the center portion of the board. Four jumper pads correspond to the 8251 TXD lines. A jumper should be connected between the pad at R3 and one 8251 TXD line.

NOTE FOR MORE RELIABLE OPERATION USE 8251A

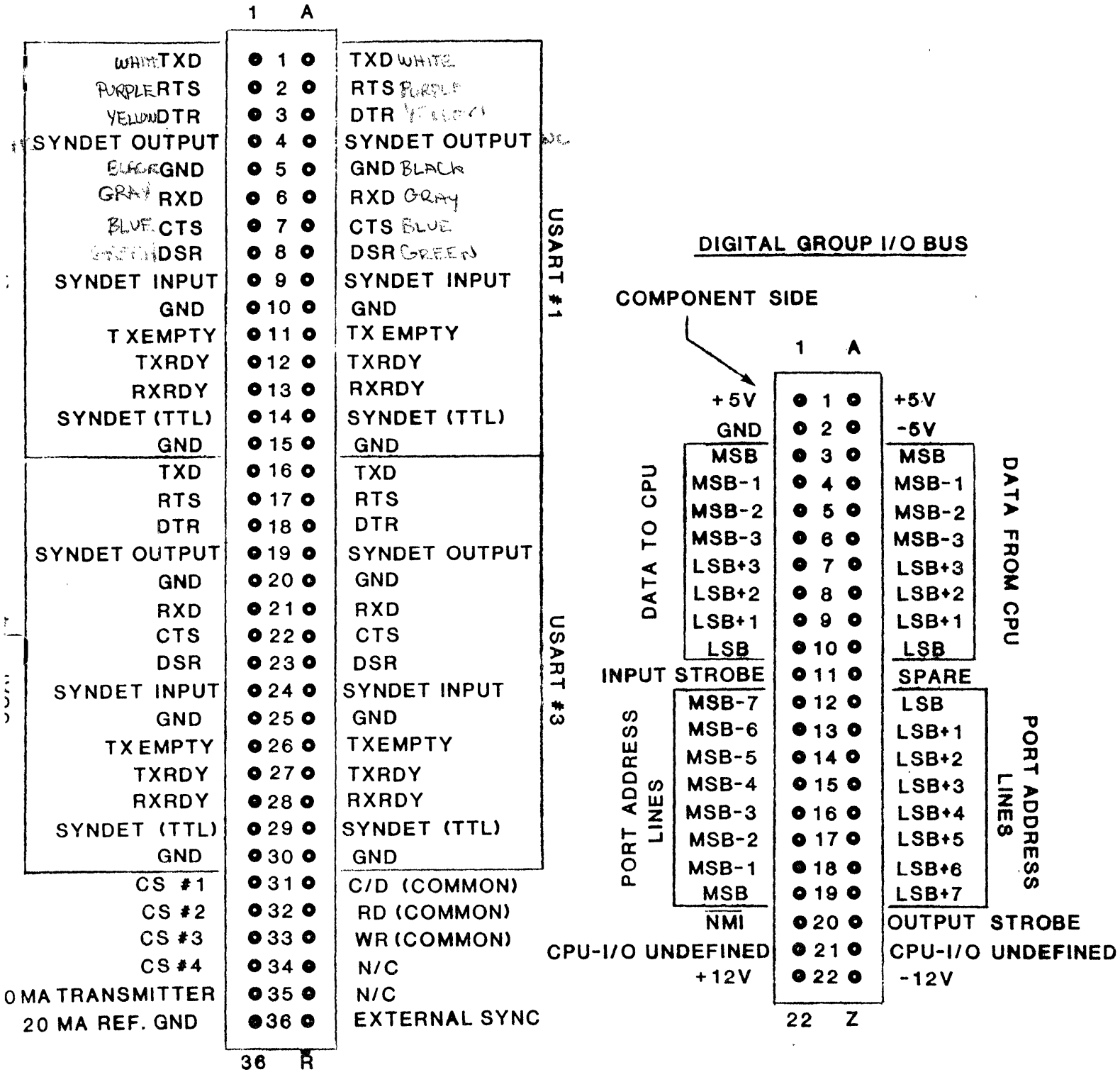


FIG. 8- PINOUT OF COMMUNICATIONS CARD 36 AND 22 PIN DUAL EDGE CONNECTORS. SEE SCHEMATIC DIAGRAM FOR LOGIC (ACTIVE HIGH AND LOW SIGNALS).

d. Control and Status Instructions

Mode Instruction Formats

Following a reset operation, a mode instruction is written into the 8251. The figure below, with a segment from the 8251 applications manual, shows the instruction format that is used and gives an example mode instruction for asynchronous transmission. Synchronous transmission is selected by setting bits D0 and D1 low. See the applications manual for synchronous transmission applications.

A mode instruction of 376 (octal) illustrates how the 8251 mode may be set. Baud rate factors designate clock inputs at $\overline{TXC}$, $\overline{RXC}$ required for asynchronous transmission; 1x baud rate, 16x baud rate, 64x baud rate. In synchronous mode the clock rate is equal to the baud rate (1x baud rate). The 1x baud rate factor for asynchronous transmissions is not recommended as it may not work reliably.

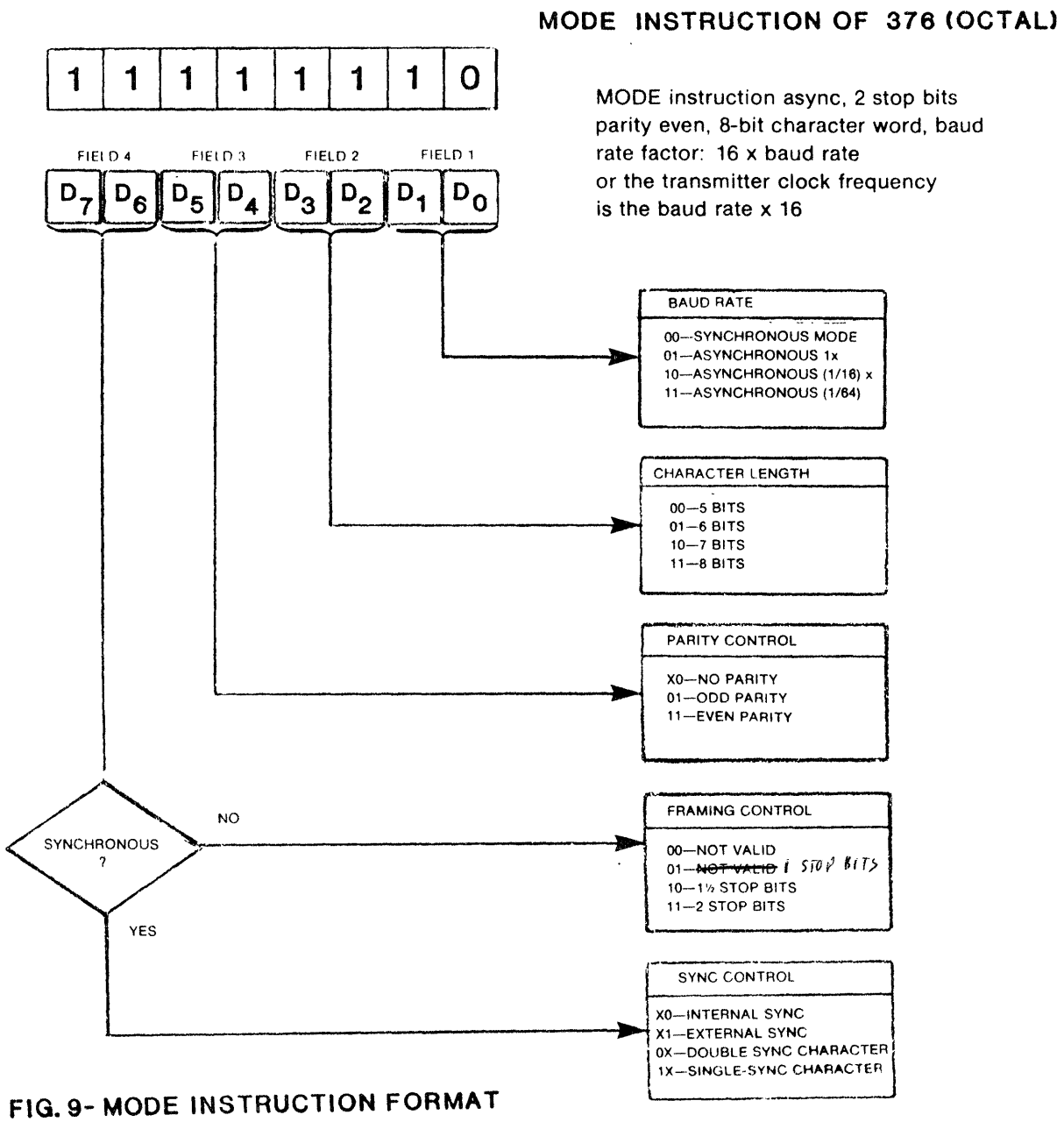


FIG. 9- MODE INSTRUCTION FORMAT

Command Instruction Format

The command instruction controls the actual operation of a selected format, and is written into the 8251's after a mode instruction has been programmed. Once the mode instruction has been written in the 8251, all further control "writes" (C/D = 1) will load the command instruction. A reset operation (internal for application of the card) will return the 8251 to the mode instruction format. Figure 10, from the 8251 applications manual, illustrates the command instruction format.

An example command instruction of 001 (octal), written into the 8251, sets the TXEN bit (D0) "high" which enables the transmitter. To change a command, it is necessary to write another command word (C/D = 1) into the 8251. The mode will remain unchanged (sync-async) until another reset and mode instruction sequence is initiated.

The TXD output remains "high" (marking) until the TXEN bit in the command register is enabled and the $\overline{CTS}$ line goes "low". Data is shifted out on the falling edge of $\overline{TXC}$ in the synchronous mode and in the asynchronous mode on the falling edge of $\overline{TXC}$ at $\overline{TXC}$, $\overline{TXC}/16$ or $\overline{TXC}/64$, as defined by the mode instruction.

Setting bits D1 and D5 (DTR and RTS) "high" forces "low" the $\overline{DTR}$ and $\overline{RTS}$ output pins on the 8251. These lines are generally used for modern "handshaking" lines. Two input pins on the 8251 $\overline{DSR}$ and $\overline{CTS}$ complement DTR and RTS. The $\overline{DSR}$ input signal can be tested by the CPU using a status read to test modem conditions such as data set ready. The $\overline{CTS}$ line enables the 8251 to transmit data (along with TXEN) and must be set accordingly. The 1489's (quad line receivers) convert RS-232 inputs to TTL levels. The 1488's (quad line drivers) convert TTL output levels to RS-232 level signals.

A command of 044 enables the receiver and sets $\overline{RTS}$ low (request to send). The $\overline{RTS}$ line could be connected to a transmitting device $\overline{CTS}$ line. The external pin $\overline{CTS}$ on the 8251 does not affect its operation as a receiver. A falling edge at RXD signals the possible beginning of a START bit and new character. Input bits are sampled at the RXD pin with the edge of $\overline{RXC}$. The 8251 begins assembling a data character, and after a valid stop bit is encountered, loads the input character into the parallel data bus buffer. The RXRDY line is then set "high" to indicate to the processor a character is ready to be fetched. Parity framing errors will be indicated in the status register and may be checked during a status read operation. If the processor fails to fetch a character before a new one is assembled, an overrun flag is set and is indicated in the status register.

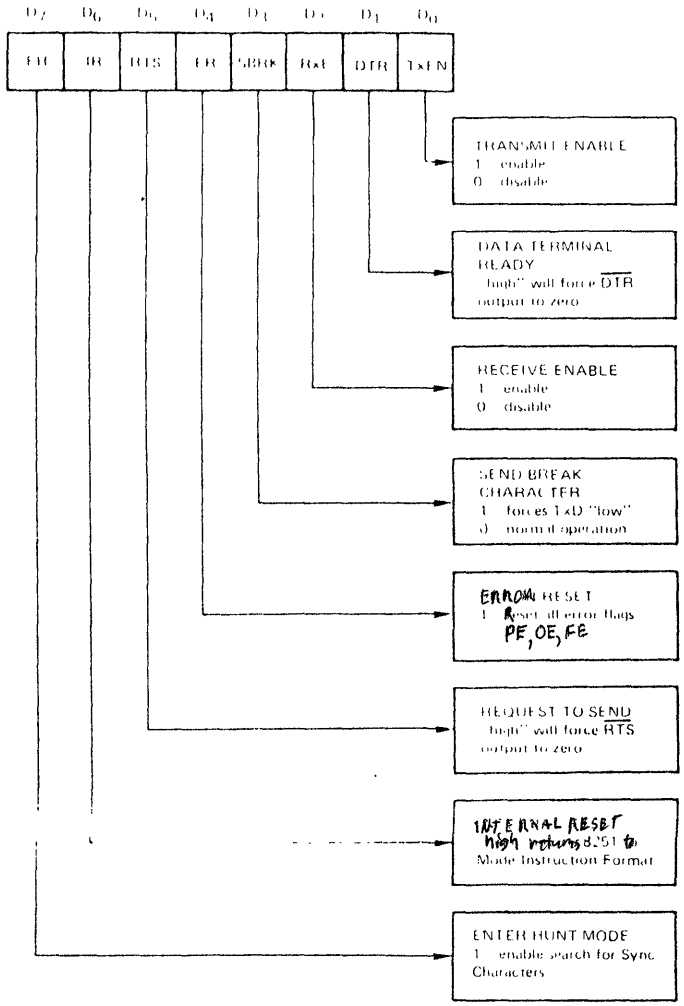
FIG. 10- COMMAND INSTRUCTION FORMAT

001 (OCTAL) -TRANSMIT

0	0	0	0	0	0	0	1

044 (OCTAL) -RECEIVE

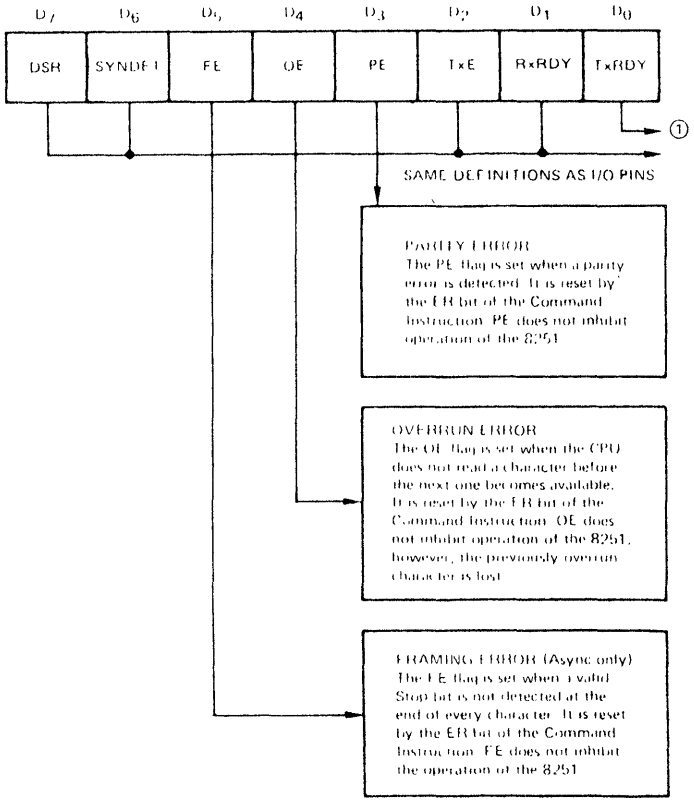
0	0	1	0	0	1	0	0



Status Read Format

The 8251 allows the programmer to "read" the status of the USART at any time during its functional operation (chip select enabled). A normal "read"command (input data from I/O port) is issued by the CPU, with the port address (state of C/$\overline{D}$ line) determining data or status information being read. Some of the bits in the status read format have identical meaning to external I/O pins so that the 8251 can be used in a completely polled environment or in an interrupt driven environment. A figure taken from the applications manual illustrates the status word format that is used. Further information on the usage of status register bits and on using external pins in an interrupt structure can be found in the applications manual provided.

FIG. 11 - STATUS READ FORMAT



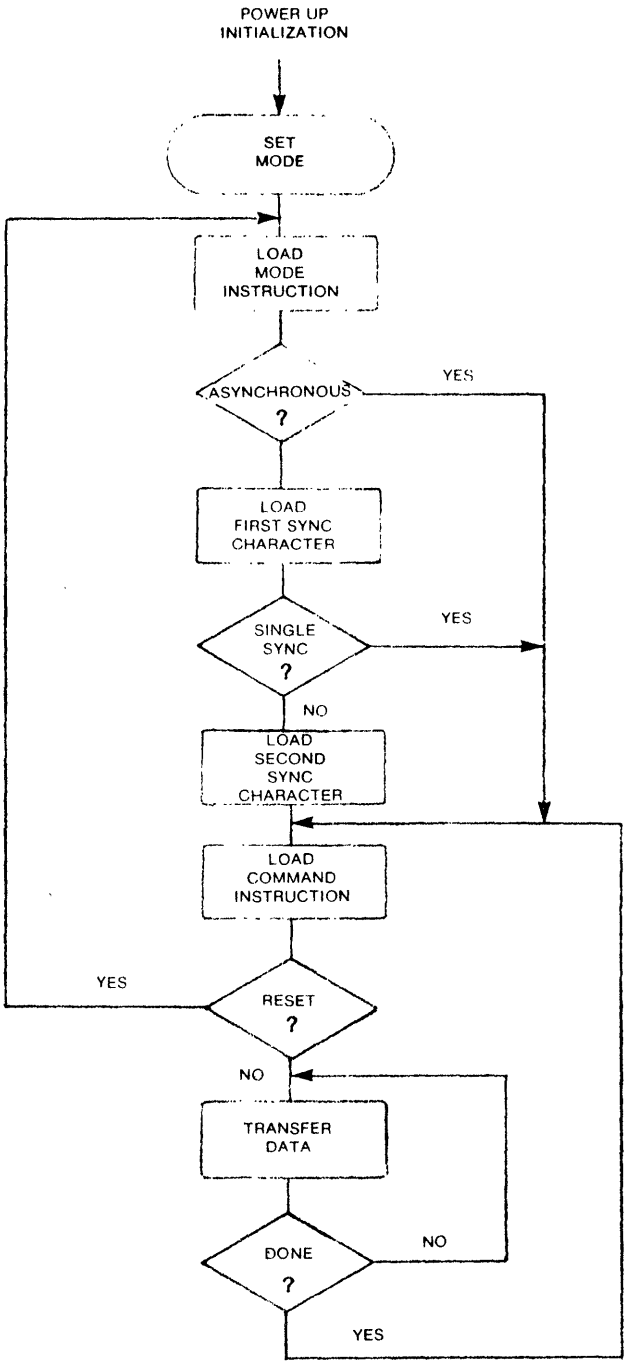
Note ① TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

TxRDY status bit = DB Buffer Empty

TxRDY (pin 15) = DB Buffer Empty • CTS • TxEn

Two sample programs have been written and may be used as operating routines for the communications card. One is used for transmitting data,the other for receiving data. The $\overline{CTS}$ line must be connected to a logic "0" source. The flowchart below shows the sequence of programming steps carried out for either synchronous or asynchronous modes. Figure 12 shows transmitting and receiver data formats for both operating modes. The choice of either mode depends directly on the application; Asynchronous transmission is used generally with man-machine interfaces while synchronous transmission offers higher speeds for machine-machine communication.

Both sample programs use the same reset operation sequence when initially addressing the USART. The user should consult the applications manual for the 8251 USART,particularly the section on initiating software reset.



TYPICAL PROGRAMMING FLOWCHART AFTER POWER-UP RESET

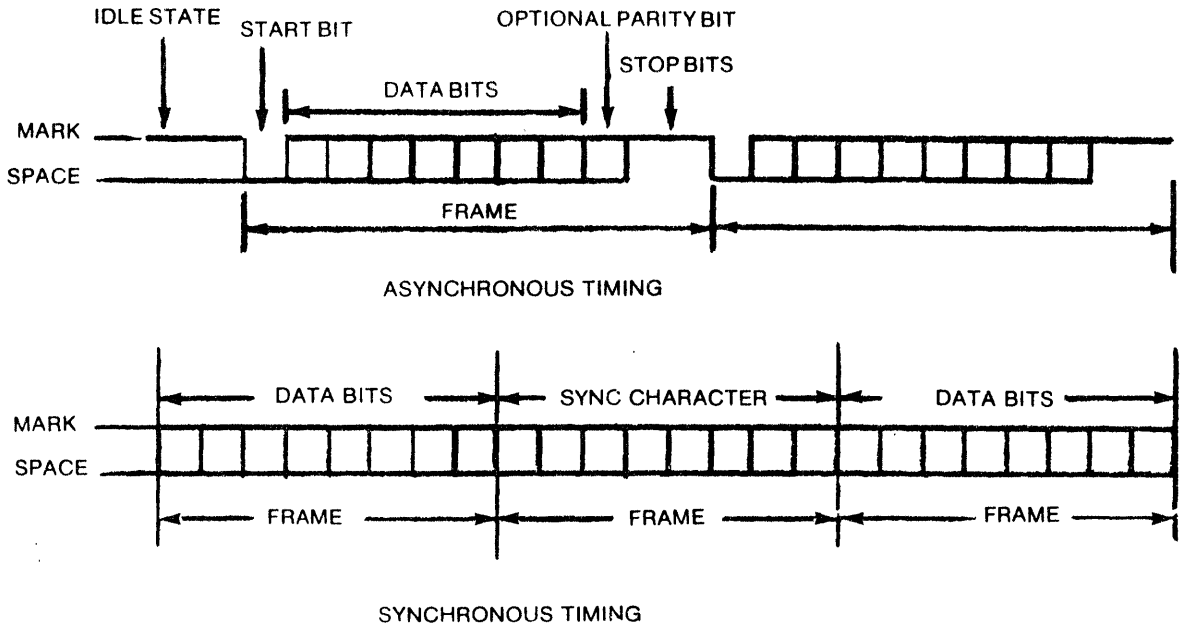


FIG. 12- TRANSMITTER/ RECEIVER FORMATS

USART Communications Card Transmitting Program

This is a sample routine for operating the USART communications card as an asynchronous transmitter.

This routine uses a Digital Group operating system with subroutines HOME ERASE at 000346 (octal), KEYBOARD at 001250 (octal) and TV at 000372.

```
PORT    EQU  17     Decimal     COMMAND DB 001
DPORT   EQU  16     Decimal     MODE DB 376

CALL    HOME ERASE
LD      C, PORT
CALL    INITIALIZE
```

*INITIALIZE carries out a sequence of "out" instructions to the control port which resets the 8251. After resetting the 8251 #1, it sends out a mode instruction which sets the format for transmitted data.

CALL COMMAND

The COMMAND subroutine outputs a command instruction word which enables the transmitter.

To change the mode operation or to send another command, a reset command must be given to the enabled 8251. Once the mode instruction has been written to the 8251, and sync characters (sync mode only) are inserted, all "control writes" to the 8251 (C/D = 1) will load the COMMAND instruction.

CALL KEYBOARD

The KEYBOARD routine waits for a character input from the keyboard or input device.

CALL DATA OUT

The DATA OUT routine saves the contents of the "A" register (the input character) and saves all CPU flags. It does a status read (C/D = 1) which checks to see that the transmitter is ready. This condition will only be true if the data bus buffer of the 8251 is empty, or if the last character transmitted had actually been transmitted.

If the transmitter is ready, the contents of the "C" register are decremented to effect a data port address. The data character is writen out to the 8251 and the 8251 will transmit the character.

Note: The 8251 will only transmit if the TXEN bit of a command word is enabled, and the $\overline{CTS}$ external pin of the 8251 is set low. In the event that neither is true, the status line TXRDY would not go high to request another character to be input from the processor.

TRANSMITTER ROUTINE

THIS ROUTINE EXECUTES AT (OCTAL)

```
066341                  0100 * THIS IS A SAMPLE OUTPUT ROUTINE FOR DG-0022-A
066341 315 346 000      0110         CALL 346
066344                  0120 * CALL HOME ERASE
066344                  0130 PORT    EQU  17D
066344                  0140 * THIS ADDRESS IS THE CONTROL PORT ADDRESS
066344 016 021          0150         LD   C,PORT
066346 315 371 066      0160         CALL INIT
066351                  0170 * THIS STATEMENT CALLS THE INITIALIZE ROUTINE
066351                  0180 * INIT ALSO SENDS THE MODE WORD TO THE 8251
066351 315 015 067      0190         CALL COMAND
066354                  0200 * THIS STATEMENT SENDS A COMAND WORD TO THE 8251
066354 315 250 001      0210 IN      CALL 1250
066357                  0220 * IN GETS A CHARACTER FROM THE KEYBOARD AND TRANSMITS
066357                  0230 * IT TO THE 8251 DATA PORT
066357 016 021          0240         LD   C,PORT
066361 315 023 067      0250         CALL DATAO
066364                  0260 * DATAO IS THE TRANSMIT ROUTINE
066364 315 372 000      0270         CALL 372
066367                  0280 * PRINTS CHARACTER ON TV MONITOR
066367 030 363          0290         JR   IN
066371 076 001          0300 INIT    LD   A,001
066373                  0310 * 001 OCTAL IS AN INVALID MODE INSTRUCTION THIS CAUSES
066373                  0320 * THE 8251 LOOK FOR ANOTHER MODE INSTRUCTION.
066373 355 171          0330         OUT  (C),A
066375 355 171          0340         OUT  (C),A
066377 355 171          0350         OUT  (C),A
067001 355 171          0360         OUT  (C),A
067003 076 100          0370         LD   A,100
067005                  0380 * 100 OCTAL IS A RESET COMAND
067005 355 171          0390         OUT  (C),A
067007 072 040 067      0400         LD   A,(MODE)
067012                  0410 * MODE IS THE MODE INSTRUCTION WORD
067012 355 171          0420         OUT  (C),A
067014 311              0430         RET
067015 072 037 067      0440 COMAND LD   A,(COMND)
067020                  0450 * COMAND IS THE COMAND WORD OUTPUT ROUTINE
067020                  0460 * COMND IS THE COMAND INSTRUCTION WORD
067020 355 171          0470         OUT  (C),A
067022 311              0480         RET
067023 365              0490 DATAO   PUSH AF
067024                  0500 * SAVE THE CONTENTS OF A REGISTER
067024                  0510 * DATAO CHECKS THE STATUS OF THE 8251 FOR TXRDY THEN
067024                  0520 * LOADS IN THE DATA CHARACTER
067024 355 170          0530 STATO   IN   (C),A
067026                  0540 * READ STATUS WORD
067026 313 107          0550         BIT  0,A
067030 050 372          0560         JR   Z,STATO
067032                  0570 * CHECK FOR A 1 IN BIT 0 OF STATUS WORD
067032 361              0580         POP  AF
067033                  0590 * RECALL DATA CHARACTER IN A REGISTER
067033 015              0600         DEC  C
067034                  0610 * CHANGE FROM THE COMAND ADDRESS TO THE DATA ADDRESS
067034 355 171          0620         OUT  (C),A
067036                  0630 * OUTPUT THE DATA CHARACTER
067036 311              0640         RET
067037                  0650 COMND   DB   001
  001
067040                  0660 * COMAND WORD (ENABLE TRANSMITTER)
067040                  0670 MODE    DB   376
  376
067041                  0680 * MODE INSTRUCTION ASYNC, 2 STOP BITS, PARITY EVEN,
067041                  0690 * 8 BIT WORD, BAUD RATE DIVIDED BY 16
```

TRANSMITTER ROUTINE

THIS ROUTINE EXECUTES AT (OCTAL)

```
066341                          0100 * THIS IS A SAMPLE OUTPUT ROUTINE FOR DG-0022-A
066341 315 346 000              0110         CALL 346
066344                          0120 * CALL HOME ERASE
066344                          0130 PORT    EQU  17D
066344                          0140 * THIS ADDRESS IS THE CONTROL PORT ADDRESS
066344 016 021                  0150         LD   C,PORT
066346 315 371 066              0160         CALL INIT
066351                          0170 * THIS STATEMENT CALLS THE INITIALIZE ROUTINE
066351                          0180 * INIT ALSO SENDS THE MODE WORD TO THE 8251
066351 315 015 067              0190         CALL COMAND
066354                          0200 * THIS STATEMENT SENDS A COMAND WORD TO THE 8251
066354 315 250 001              0210 IN      CALL 1250
066357                          0220 * IN GETS A CHARACTER FROM THE KEYBOARD AND TRANSMITS
066357                          0230 * IT TO THE 8251 DATA PORT
066357 016 021                  0240         LD   C,PORT
066361 315 023 067              0250         CALL DATAO
066364                          0260 * DATAO IS THE TRANSMIT ROUTINE
066364 315 372 000              0270         CALL 372
066367                          0280 * PRINTS CHARACTER ON TV MONITOR
066367 030 363                  0290         JR   IN
066371 076 001                  0300 INIT    LD   A,001
066373                          0310 * 001 OCTAL IS AN INVALID MODE INSTRUCTION THIS CAUSES
066373                          0320 * THE 8251 LOOK FOR ANOTHER MODE INSTRUCTION.
066373 355 171                  0330         OUT  (C),A
066375 355 171                  0340         OUT  (C),A
066377 355 171                  0350         OUT  (C),A
067001 355 171                  0360         OUT  (C),A
067003 076 100                  0370         LD   A,100
067005                          0380 * 100 OCTAL IS A RESET COMAND
067005 355 171                  0390         OUT  (C),A
067007 072 040 067              0400         LD   A,(MODE)
067012                          0410 * MODE IS THE MODE INSTRUCTION WORD
067012 355 171                  0420         OUT  (C),A
067014 311                      0430         RET
067015 072 037 067              0440 COMAND  LD   A,(COMND)
067020                          0450 * COMAND IS THE COMAND WORD OUTPUT ROUTINE
067020                          0460 * COMND IS THE COMAND INSTRUCTION WORD
067020 355 171                  0470         OUT  (C),A
067022 311                      0480         RET
067023 365                      0490 DATAO   PUSH AF
067024                          0500 * SAVE THE CONTENTS OF A REGISTER
067024                          0510 * DATAO CHECKS THE STATUS OF THE 8251 FOR TXRDY THEN
067024                          0520 * LOADS IN THE DATA CHARACTER
067024 355 170                  0530 STATO   IN   (C),A
067026                          0540 * READ STATUS WORD
067026 313 107                  0550         BIT  0,A
067030 050 372                  0560         JR   Z,STATO
067032                          0570 * CHECK FOR A 1 IN BIT 0 OF STATUS WORD
067032 361                      0580         POP  AF
067033                          0590 * RECALL DATA CHARACTER IN A REGISTER
067033 015                      0600         DEC  C
067034                          0610 * CHANGE FROM THE COMAND ADDRESS TO THE DATA ADDRESS
067034 355 171                  0620         OUT  (C),A
067036                          0630 * OUTPUT THE DATA CHARACTER
067036 311                      0640         RET
067037                          0650 COMND   DB   001
  001
067040                          0660 * COMAND WORD (ENABLE TRANSMITTER)
067040                          0670 MODE    DB   376
  376
067041                          0680 * MODE INSTRUCTION ASYNC, 2 STOP BITS, PARITY EVEN,
067041                          0690 * 8 BIT WORD, BAUD RATE DIVIDED BY 16
```

USART Communications Card Receiving Program

This is a sample routine for operating the USART communication card as an asynchronous receiver. It uses USART #1 (8251) and ports 16 and 17 for control and data, and reading and writing to the 8251. The "C" register is used for storing the port address used to address the USART.

This routine uses a Digital Group operating system with subroutines HOME ERASE and TV.

The subroutine INITIALIZE carries out a sequence of "out" instructions to the control port address which resets the 8251. After resetting 8251 #1, it sends out a mode instruction which sets the format for transmitted or received data. A mode instruction for setting up the 8251 for transmitting may be the same as that for receiving.

CALL COMMAND

The COMMAND subroutine outputs a command instruction word which sets bit 5 and bit 2 high (octal Ø44). Bit 5, $\overline{RTS}$, is set high (enabled) and sets the external pin $\overline{RTS}$ of the 8251 low. The receiver enable bit (D2) is also set high to allow the receiver to collect serial data and assemble data words.

After enabling the receiver the program monitors transmissions by reading the status word of the enabled 8251. If data has been sent correctly according to the format set up, the RXRDY bit in the staus word will be set high indicating the 8251 has an assembled character for the microprocessor. The port address is then changed to read data (C/$\overline{D}$ = 0) and the processor reads data from the I/O port data lines.

RECEIVER ROUTINE

```
062242                    0000 * THIS IS A SAMPLE INPUT ROUTINE
062242 315 346 000        0100         CALL 346
062245                    0105 * CALL HOME ERASE
062245                    0110 PORT    EQU  17D
062245                    0111 * THIS IS THE CONTROL PORT ADDRESS
062245 016 021            0120         LD   C,PORT
062247 315 267 062        0130 START   CALL INIT
062252                    0133 * CALL THE INITIALIZE ROUTINE
062252 315 313 062        0140         CALL COMAND
062255                    0150 IN      EQU  $
062255 016 021            0160         LD   C,PORT
062257 315 323 062        0170         CALL DATAI
062262 315 372 000        0180         CALL 372
062265 030 366            0190         JR   IN
062267 076 001            0200 INIT    LD   A,001
062271 355 171            0210         OUT  (C),A
062273 355 171            0220         OUT  (C),A
062275 355 171            0230         OUT  (C),A
062277 355 171            0240         OUT  (C),A
062301 076 100            0250         LD   A,100
062303 355 171            0260         OUT  (C),A
062305 072 322 062        0270         LD   A,(MODE)
062310 355 171            0280         OUT  (C),A
062312 311                0290         RET
062313 072 321 062        0300 COMAND  LD   A,(COMND)
062316 355 171            0310         OUT  (C),A
062320 311                0320         RET
062321                    0330 COMND   DB   37D
045
062322                    0340 MODE    DB   376
376
062323                    0350 DATAI   EQU  $
062323 355 170            0360 STATI   IN   A,(C)
062325 313 117            0370         BIT  1,A
062327 050 372            0380         JR   Z,STATI
062331 015                0390         DEC  C
062332 355 170            0400         IN   A,(C)
062334 366 200            0410         OR   200
062336 311                0420         RET
```

Cabling

Figure 8 shows the pinout of the 36 and 22 pin dual edge connector of the communications card. Pins A through S of the 36 pin connector are a block of pins designated for making connection to USART #1. Pins 1 through 15 are designated for USART #2, pins T through J for USART #3, and pins 16 through 30 designated for USART #4. Connections are only made for those pins necessary for interfacing and may be soldered or made with "molex" type connectors.

RS-232 connections are usually made with 25 pin "D" connectors. The typical pinout of a "D" connector is shown below.

Pin	Function
1	Protective ground
2	Transmitted data-output
3	Received data- Input
4	Request to Send-output
5	Clear To Send-input
6	Data Set Ready-input
7	Signal ground(common return)
20	Data Terminal Ready-output

For applications where cable lengths needed is less than 50 feet,or more than 50 feet but at a baud rate of roughly 300 baud or less, the cable used is not critical and need not be shielded. In most cases, it should be use stranded wire,but solid conductors will probably work for short distances. Large diameter wire is not necessary since the devices are not carrying high currents.

Connecting the outputs and their corresponding inputs is accomplished by crossing pairs of wires in the cable itself. E.G.

Pin 1	Pin 1	BLACK
Pin 2 (TXD)	Pin 3 (RXD)	WHITE
Pin 3 (RXD)	Pin 2 (TXD)	GRAY
Pin 4 (RTS)	Pin 5 (CTS)	PURPLE
Pin 5 (CTS)	Pin 4 (RTS)	BLUE
Pin 6 (DSR)	Pin 20 (DTR)	GREEN
Pin 7	Pin 7 (GND)	BLACK
Pin 20 (DTR)	Pin 6 (DSR)	YELLOW

Diagnostic testing and operation of the communications card

The equipment used to test the communications card should use a voltmeter,an oscilloscope, and a frequency counter if available.

Voltage checks can be made at the following pins:

Check for 5V:
Pin 5,IC 5
Pin 5,IC 6
Pin 14,IC 7
Pins 2,9,15,and 16 of IC 8
Pins 5,9,10,15,and 16 of IC 9

Check for GND at:
Pins 2,3,10 of IC 5
Pins 2,3,10 of IC 6
Pin 7 of IC 7
Pins 8,10,and 14 of IC 8
Pins 1,8,14 of IC 9

Pins on the card's 22 pin connector can also be checked:
Pins 1,A at +5V
Pin 2 at Gnd
Pin 22 at +12V
Pin Z at -12V

Clock circuitry testing can be done with an oscilloscope or frequency counter. Checking the frequencies at the following pins will indicate if the frequency divider network is working properly. If one IC in the chain is defective and not outputting a frequency, it will affect all the resulting frequencies relying on that frequency for an input.

Pin 8,IC 7--4MHz square wave

Pin 12,IC 6--2 MHz square wave

On the row of baud selector pads located on the top center portion of the card,frequencies may be checked as follows or according to figure 4.

Row 1---153,600 Hz 153808
Row 2---76,800 Hz 76903
Row 3---38,400 Hz 38452
Row 4---19,200 Hz 19226
Row 5---9,600 Hz 9614
Row 6---4,800 Hz 4807
Row 7---1,760 Hz 1748

These frequencies are typically within .5% If they are not correct,check the circuitry of the frequency divider network.

Operating the USART communications card with USART *1,and the programs listed, the signals on the RXD and TXD pins can be checked, with an oscilloscope or by reading data through the microprocessor. Connecting pin H of the 36 pin connector to 12V,biases $\overline{\text{CTS}}$ on the 8251 and enables the transmitter. The inputs and outputs of the level shifting chips (1488's and 1489's) may be checked with a voltmeter.

The communications card can be set up so that powering up the microcomputer sets up the mode and command words for each 8251 on the card. Once set up, the microprocessor can return to normal operation, with the 8251's monitoring outside communication. If an external device signals one of the 8251's,requesting a data transfer,the corresponding 8251 can signal the microprocessor via either an interrupt request or by setting a bit in the status register when using polled I/O processing.

Reference Materials

1. *NEC uPD8251 Programmable Communication Interface*, January, 1977.
2. *8080 Intel Microcomputer Peripherals User's Manual*, 1976.
3. *EDN*, "Some Do's, Don't's, and How's of Serial Data Transmission", April 20, 1976.
4. *EDN*, "USART, A uP Interface for Serial Data Communication", September 5, 1976.
5. *Computer Design*, "Design Constraints for a USART-based Minicomputer Communications Interface", June 1977.
6. *Kilobaud*, "Who's Afraid of RS-232 — Data Communications Explained!", May, 1977.
7. *Datamation*, "Display Terminal Survey — Alphanumeric Display Terminals", January, 1976.
8. *Computer Data Handling Circuits*, Alfred Corbin.
9. *Minicomputers for Engineers and Scientists*, Granino A. Korn.
10. *TV Typewriter Cookbook*, Don Lancaster.

NOTE FOR MORE RELIABLE OPERATION USE 8251a not 8251

USART Communications Card Parts List

	Label	Description	Qty.	Digital Group Part #
☒	IC1 - IC4	8251, 28-pin, USART interface chip	4 (1)*	073-015
☒	IC12, IC14, IC20, IC22	1489, 14-pin, quad line receiver	4 (2)*	078-007
☒	IC11, IC13, IC19, IC21	1488, 14-pin, quad line driver	4 (2)*	078-008
☒	IC26	74154, 24-pin, 1 of 16 decoder	1	075-053
☒	IC18	7420, 14-pin, dual 4-input nand gate	1	075-011
☒	IC7	74L04, 14-pin, hex inverter	1	075-049
☒	IC25	7442, 16-pin, 1 of 10 decoder	1	075-016
☒	IC10	7402, 14-pin, quad 2-input NOR gate	1	075-002
☒	IC17	7432, 14-pin, quad 2-input OR gate	1	075-013
☒	IC15, IC16	7401, 14-pin, quad 2-input nand gate	2	075-001
☒	IC5, IC6	7493, 14-pin, binary counter	2	075-023
☒	IC8, IC9	74193, 16-pin, synchronous binary counter	2	075-041
☒	IC23, IC24	74125, 14-pin, tri-state quad buffer	2	075-031
☒	Q1	2N5129 npn transistor	1	020-004
☒	D1	1N60 germanium diode	1	040-001
☒	S1 - S4	28-pin socket	4 (1)*	060-005
☒	S26	24-pin socket	1	060-004
☒	S8, S9, S25	16-pin socket	3	060-002
☒	S5 - S7, S10 - S24	14-pin socket	18 (14)*	060-001
☒		PC board	1	090-047
☒		22-pin dual edge connector	1	080-000
☒		36-pin dual edge connector	1	080-001
☒	C5, C8, C9, C11	1 mfd, 15V tantalum capacitor	4	010-001
☐	C2	50 pfd, silver mica capacitor	1	018-002
☒	C1, C3, C4, C6, C7, C10	.01 mfd capacitor, ceramic	6	014-002
☒	Y1	4 MHz crystal	1	030-007
☐ N/A		Crystal socket	1	060-007
☒	R1, R2	1K ohm ¼ watt carbon film resistor	2	001-025
☒	R3	10K ohm ¼ watt carbon film resistor	1	001-037
☒	R4	100 ohm ¼ watt carbon film resistor	1	001-010

* If you have ordered a COMM-1, quantities in parentheses are supplied.

NOTE: FOR MORE RELIABLE OPERATION, USE 8251A

NEC microcomputers, inc.

μPD8251

PROGRAMMABLE COMMUNICATION INTERFACE

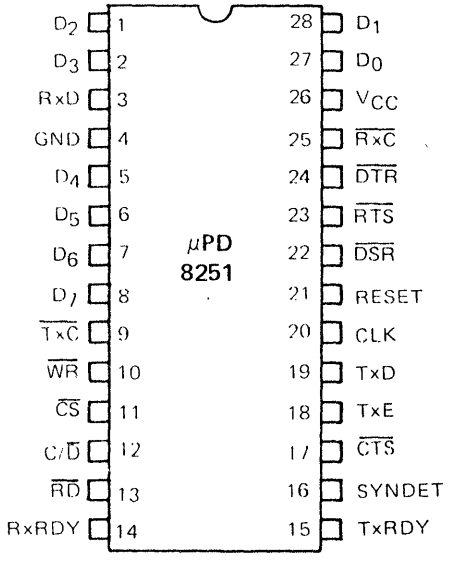
DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the μPD8080 or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART STATUS including data format errors and control signals such as TxE and SYNDET is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate - 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
  - Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate – Synchronous – DC to 56K Baud
  – Asynchronous – DC to 9.6K Baud
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply
- Separate Device, Receive and Transmit TTL Clocks
- 28 Pin Plastic DIP Package
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock (TTL)
TxD	Transmitter Data
RxC	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

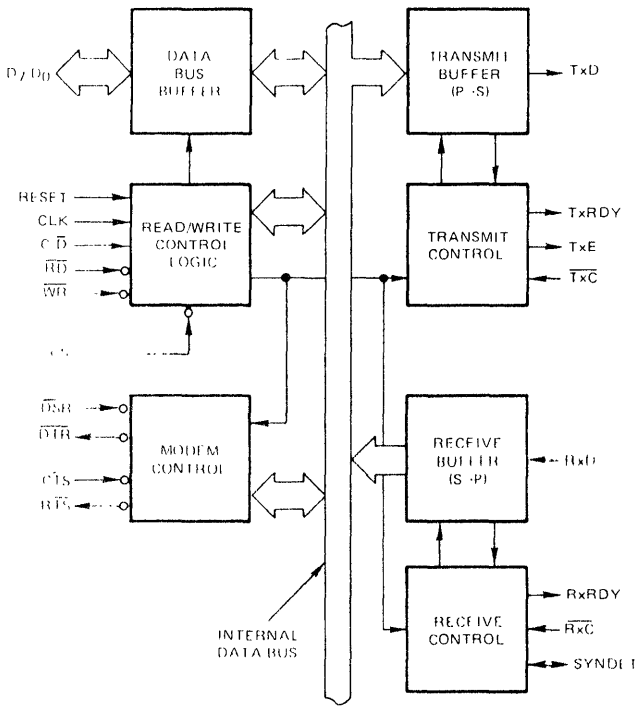
Five Militia Drive/Lexington, Massachusetts 02173 Telephone 617/862-6410 Telex 92-3434 TWX-710-326-6520

FUNCTIONAL DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter is designed specifically for 8080 microcomputer systems but works with most 8-bit processors. Operation of the 8251, like other I/O devices in the 8080 family, is programmed by system software for maximum flexibility.

In the receive mode, a communication interface device must convert incoming serial format data into parallel data and make certain format checks on the data. And in the transmit mode, the device must format data into serial data. The device must also supply or remove characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

BLOCK DIAGRAM



BASIC OPERATION

C/D	RD	WR	CS	
0	0	1	0	8251 → Data Bus
0	1	0	0	Data Bus → 8251
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages	0.5 to +7 Volts
All Input Voltages	0.5 to +7 Volts
Supply Voltages	-0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* $T_a = 25°C$

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V

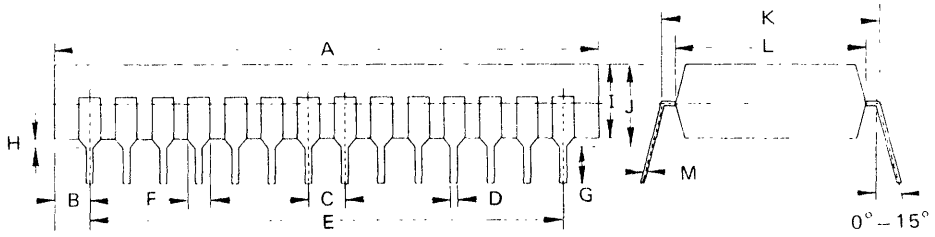
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	GND -.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.7 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −100 μA
Data Bus Leakage	I_{DL}			−50	μA	V_{OUT} = 0.45V
				10		V_{OUT} = V_{CC}
Input Load Current	I_{IL}			10	μA	@5.5V
Power Supply Current	I_{CC}		45	80	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

PACKAGE OUTLINE μPD8251C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN	0.02 MIN.
I	5.22 MAX	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

BUS PARAMETERS (1)

T_a 0°C to 70°C V_{CC} = 5.0V ± 5%, GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Address Stable before $\overline{READ}$, ($\overline{CS}$, C/$\overline{D}$)	t_{AR}	50			ns	
Address Hold Time for $\overline{READ}$, ($\overline{CS}$, C/$\overline{D}$)	t_{RA}	5			ns	
$\overline{READ}$ Pulse Width	t_{RR}	430			ns	
Data Delay from $\overline{READ}$	t_{RD}			350	ns	C_L = 100 pF
$\overline{READ}$ to Data Floating	t_{DF}			200	ns	C_L = 100 pF
		25				C_L = 15 pF
Recovery Time Between WRITES (2)	t_{RV}	6			t_{CY}	
WRITE						
Address Stable before $\overline{WRITE}$	t_{AW}	20			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			ns	
Data Set Up Time for $\overline{WRITE}$	t_{DW}	200			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40			ns	
OTHER TIMING						
Clock Period (3)	t_{CY}	420		1 35	µs	
Clock Pulse Width	$t_{\phi W}$	220		0.7t_{CY}	ns	
Clock Rise and Fall Time	$t_{R/F}$	0		50	ns	
TxD Delay from Falling Edge of $\overline{TxC}$	t_{DTx}			1	µs	C_L = 100 pF
Rx Data Set Up Time to Sampling Pulse	t_{SRx}	2			µs	C_L 100 pF
Rx Data Hold Time to Sampling Pulse	t_{HRx}	2			µs	C_L = 100 pF
Transmitter Input Clock Frequency	f_{Tx}					
1X Baud Rate		DC		56	KHz	
16X and 64X Baud Rate		DC		520	KHz	
Transmitter Input Clock Pulse Width	t_{TPW}					
1X Baud Rate		12			t_{CY}	
16X and 64X Baud Rate		1			t_{CY}	
Transmitter Input Clock Pulse Delay	t_{TPD}					
1X Baud Rate		15			t_{CY}	
16X and 64X Baud Rate		3			t_{CY}	
Receiver Input Clock Frequency	f_{Rx}					
1X Baud Rate		DC		56	KHz	
16X and 64X Baud Rate		DC		520	KHz	
Receiver Input Clock Pulse Width	t_{RPW}					
1X Baud Rate		12			t_{CY}	
16X and 64X Baud Rate		1			t_{CY}	
Receiver Input Clock Pulse Delay	t_{RPD}					
1X Baud Rate		15			t_{CY}	
16X and 64X Baud Rate		3			t_{CY}	
TxRDY Delay from Center of Data Bit	t_{TX}			16	t_{CY}	C_L 50 pF
RxRDY Delay from Center of Data Bit	t_{RX}			20	t_{CY}	
Internal Synder Delay from Center of Data Bit	t_{IS}			25	t_{CY}	
External Synder Set Up Time before Falling Edge of $\overline{Rxc}$	t_{ES}	16		16	t_{CY}	
TxEMPTY Delay from Center of Data Bit	t_{TXE}			16	t_{CY}	C_L 50 pF
Control Delay from Rising Edge of WRITE (TxE, DTR, RTS)	t_{WC}				t_{CY}	
Control to READ Set Up Time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}	16			t_{CY}	

Notes (1) AC timings measured at V_{OH} 2.0, V_{OL} 0.8, and with load circuit of Figure 1

(2) This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1

(3) The TxC and RxC frequencies have the following limitations with respect to CLK
For 1X Baud Rate, f_{Tx} or f_{Rx} ≤ 1/30 t_{CY}
For 16X and 64X Baud Rate, f_{Tx} or f_{Rx} ≤ 1/4.5 t_{CY}

(4) Reset Pulse Width 6 t_{CY} minimum

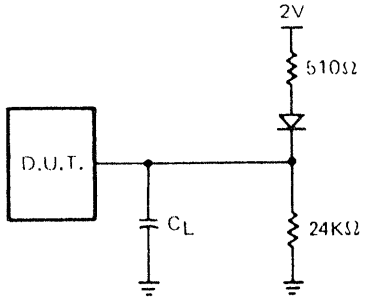
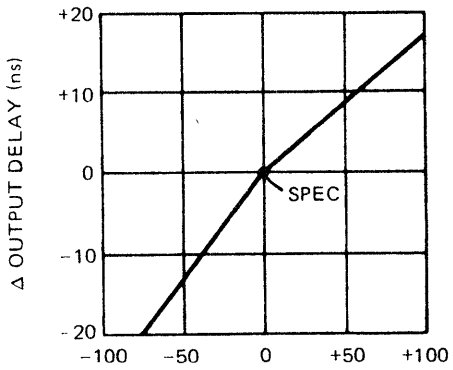


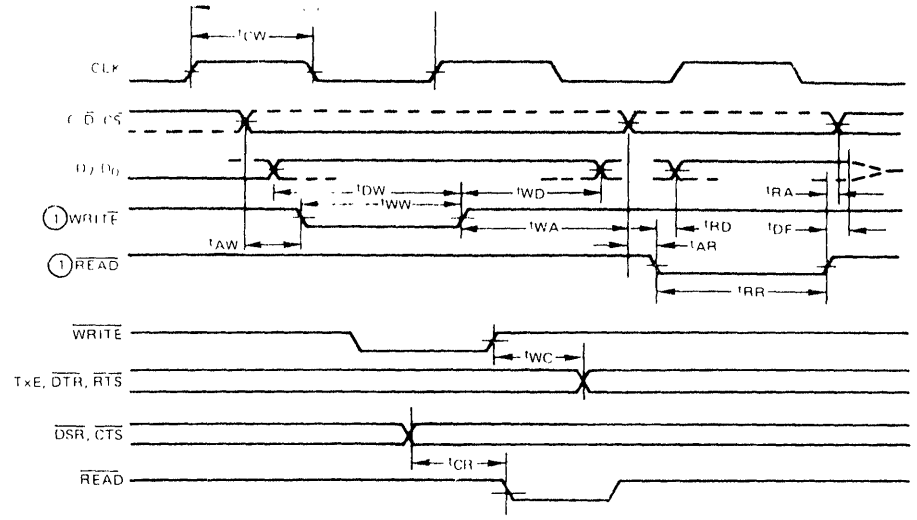
Figure 1.



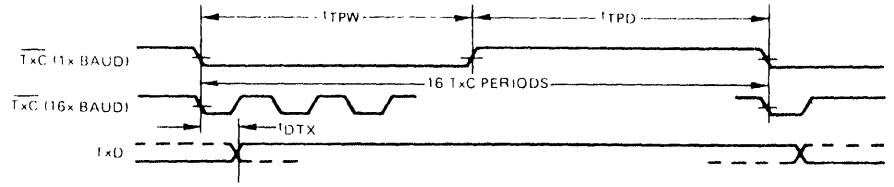
Typical Δ Output
Delay Versus Δ Capacitance (pF)

TEST LOAD CIRCUIT

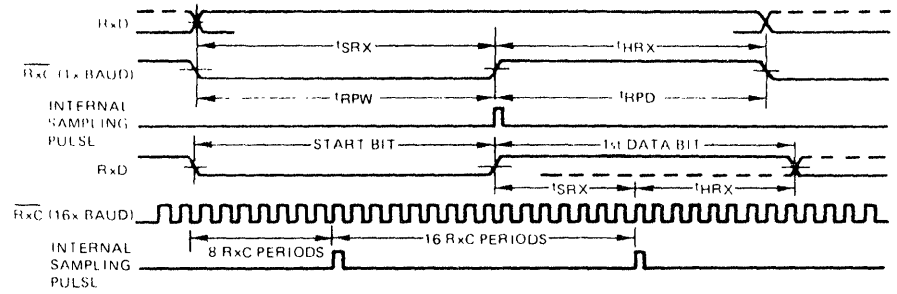
TIMING WAVEFORMS



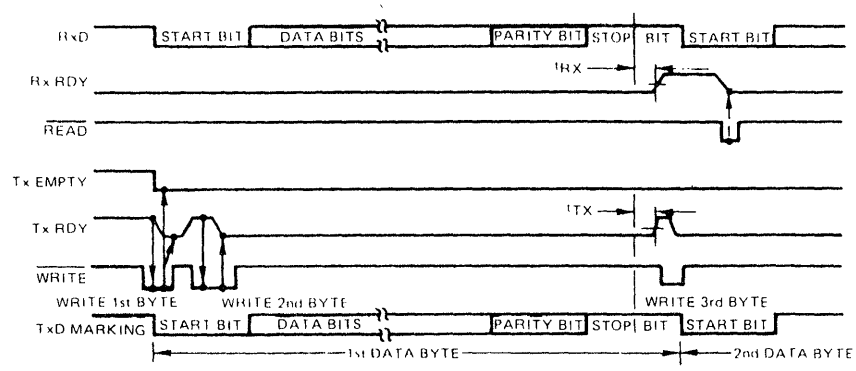
READ AND WRITE TIMING



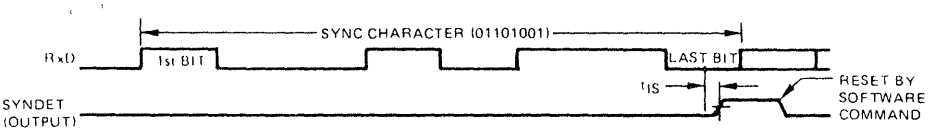
TRASNMITTER CLOCK AND DATA



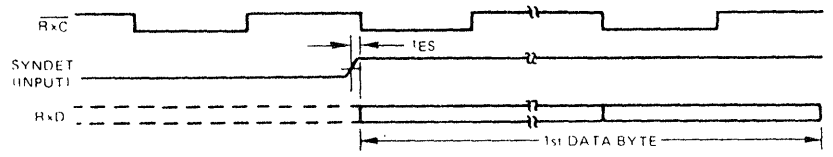
RECEIVER CLOCK AND DATA



TxRDY AND RxRDY TIMING (ASYNC MODE)



INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT

Note: (1) Write and Read pulses have no timing limitation with respect to CLK.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the 8251 to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status.
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation. The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/ Write Control Logic.
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the μPD8251 to accept the data or control word which the processor is writing out to the USART via the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the μPD8251 to place the data or status information onto the Data Bus for the processor to read.
12	C/$\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs USART to accept or provide either a data character, control word or status information via the Data Bus. 0 = Data; 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART for reading and writing to the processor.
Modem Control			The μPD8251 has a set of control inputs and outputs which may be used to simplify the interface to a Modem.
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).

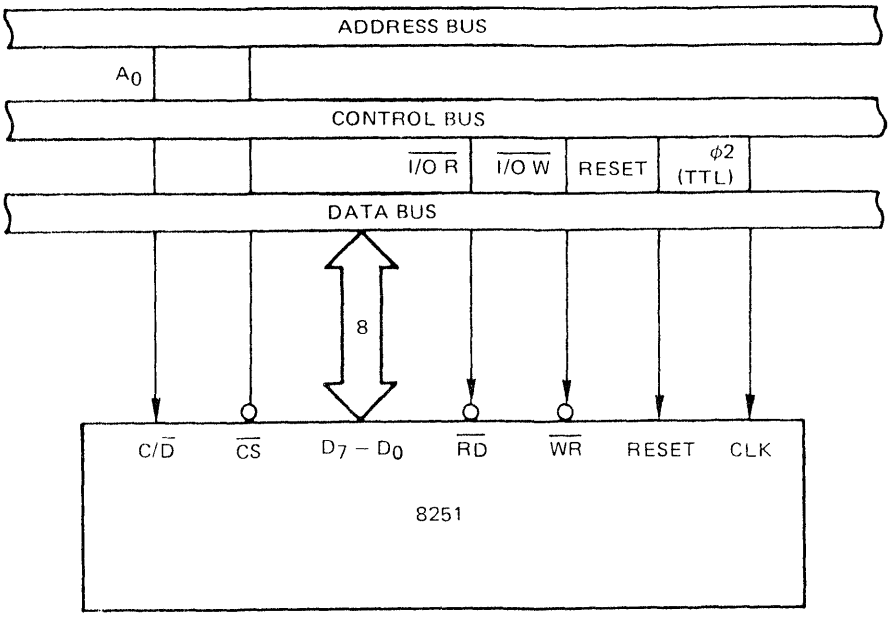
TRANSMIT BUFFER/ CONVERTER

The Transmit Buffer/Converter receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD output.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for Polled operation. Loading a character from the processor automatically resets TxRDY.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{TxC}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

8251 INTERFACE TO 8080 STANDARD SYSTEM BUS



RECEIVER BUFFER

The Receiver Buffer accepts serial data input at the $\overline{RxD}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251 sets the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Receiver Control Logic			This block manages all activities related to incoming data.
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
25	$\overline{RxC}$	Receiver Clock	The Receiver Clock is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1,16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate. Unlike $\overline{TxC}$, data is sampled by the μPD8251 on the rising edge of $\overline{RxC}$. (1)
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin.
16	SYNDET	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251 may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251 has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251 to start assembling data character on the next falling edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the μPD8251 is in SYNC.

Note: (1) Since the μPD8251 will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples:

If the Baud Rate equals 110 (Async):
- $\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)
- $\overline{RxC}$ or $\overline{TxC}$ equals 1.76 KHz (16x)
- $\overline{RxC}$ or $\overline{TxC}$ equals 7.04 KHz (64x)

If the Baud Rate equals 300:
- $\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
- $\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
- $\overline{RxC}$ or $\overline{TxC}$ equals 19.2 KHz (64x) A only

OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251 to define the desired mode and communications format. The control words will specify the BAUD RATE FACTOR (1x, 16x, 64x), CHARACTER LENGTH (5 to 8), NUMBER OF STOP BITS (1, 1-1/2, 2), ASYNCHRONOUS or SYNCHRONOUS MODE, SYNDET (IN or OUT), PARITY, etc.

After receiving the control words, the μPD8251 is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251 may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251 may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251 cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{CTS}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new Command Words.

μPD8251 PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A Reset (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D}$ = 1) followed by a software reset command instruction (40 Hex) can be used to initialize the 8251.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

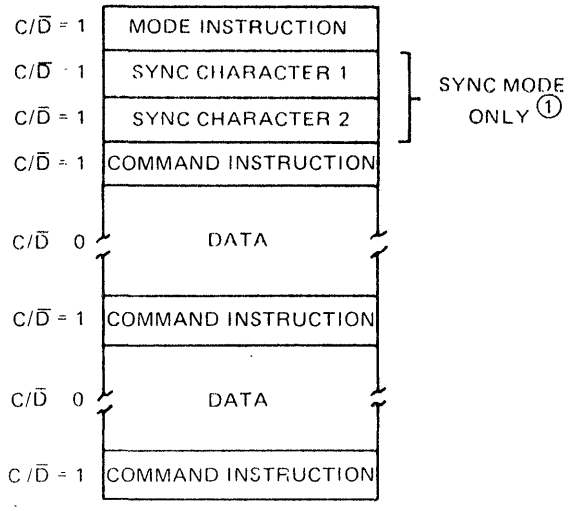
MODE INSTRUCTION

This control word specifies the general characteristics of the interface regarding the SYNCHRONOUS or ASYNCHRONOUS MODE, BAUD RATE FACTOR, CHARACTER LENGTH, PARITY, and NUMBER OF STOP BITS. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all subsequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

TYPICAL DATA BLOCK



NOTE (1) The second SYNC character is skipped if MODE instruction has programmed the 8251 to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251 to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251 can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components, one asynchronous and the other synchronous, which share the same support circuits and package. Although the format definition can be changed at will or "on the fly", the two modes will be explained separately for clarity.

ASYNCHRONOUS TRANSMISSION

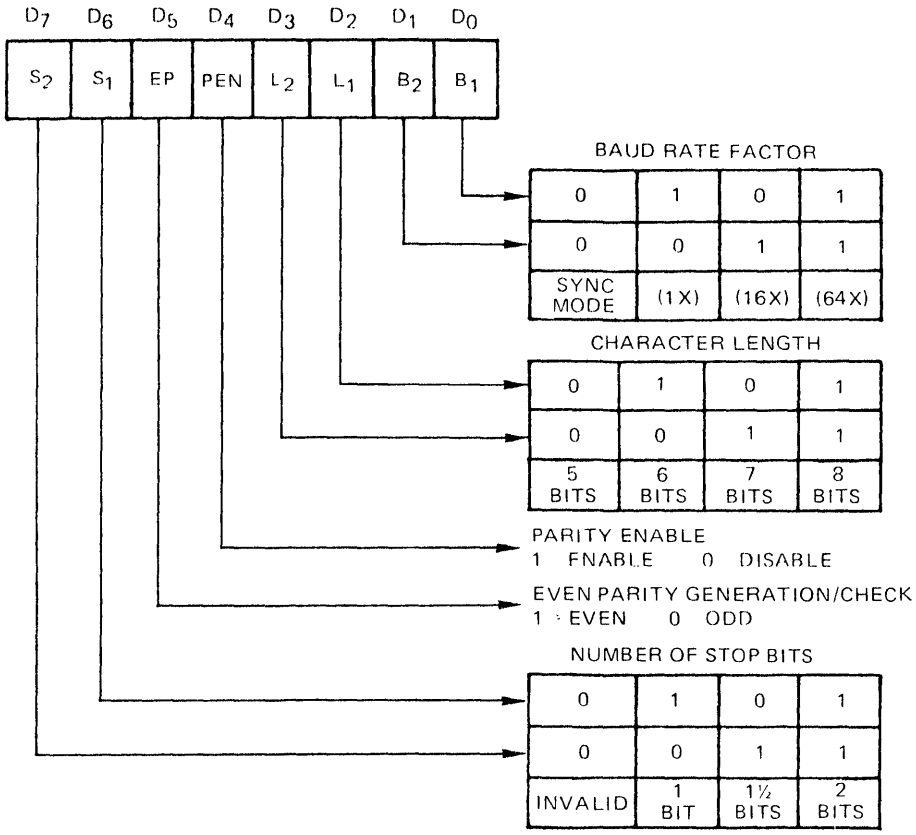
When a data character is written into the μPD8251, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bits(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at $\overline{TxC}$, $\overline{TxC}$/16 or $\overline{TxC}$/64, as defined by the Mode Instruction.

If no data characters have been loaded into the μPD8251, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

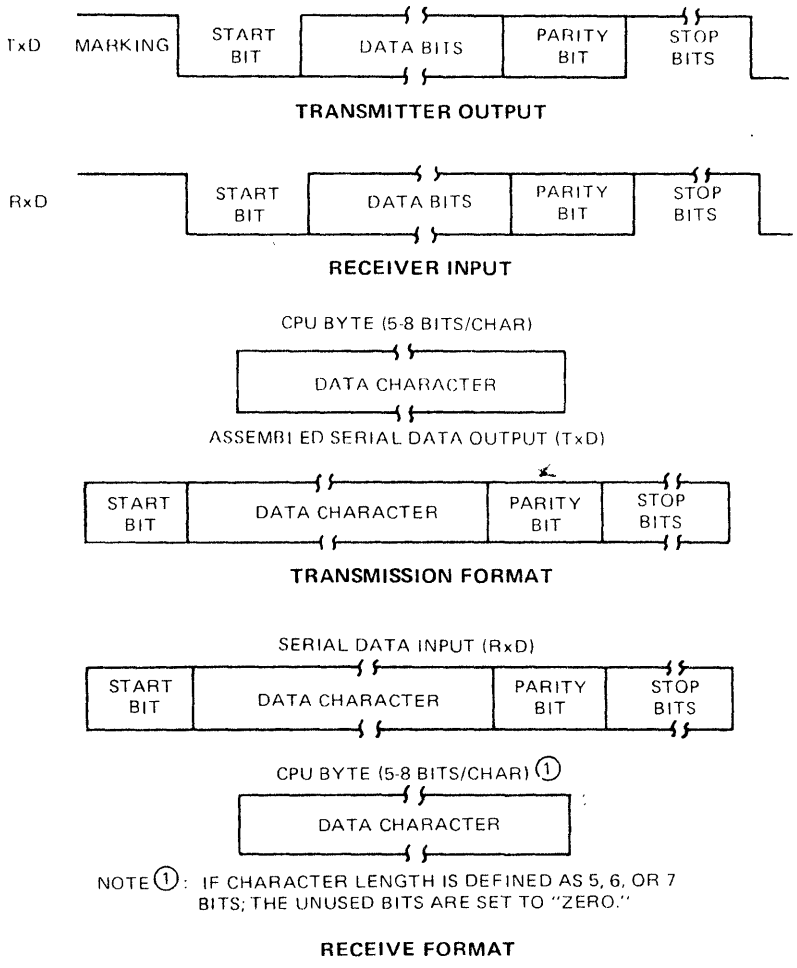
ASYNCHRONOUS RECEIVE

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input character is loaded into the parallel Data Bus Buffer of the μPD8251 and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

MODE INSTRUCTION FORMAT ASYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT ASYNCHRONOUS MODE



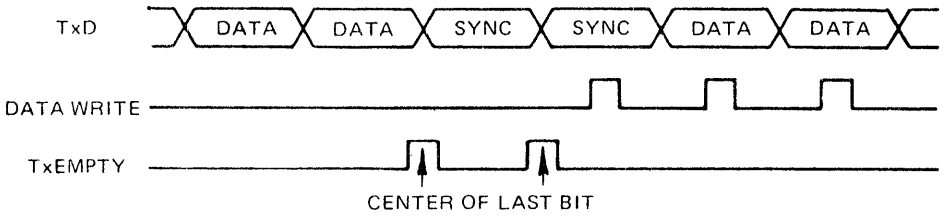
SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251 receives the first character from the processor which is usually a SYNC character. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

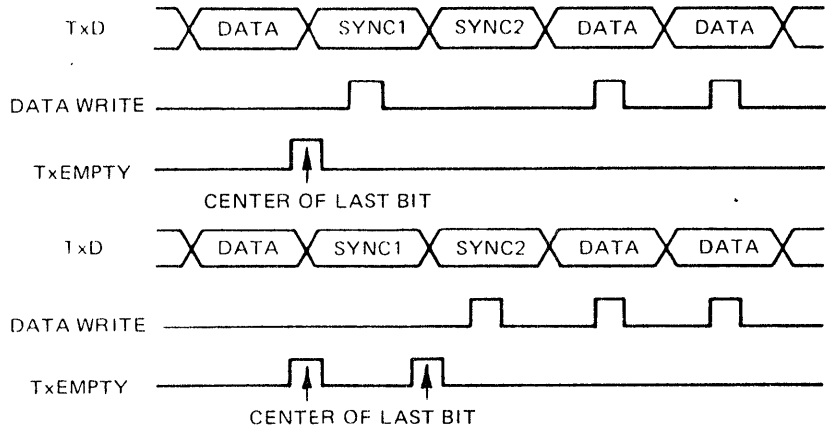
Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251 Transmitter Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251 becomes empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

TxEMPTY go high at the middle of the last data bit when the Transmit Register is EMPTY. TxEMPTY goes low again as sync characters are transmitted. See figure below.

FOR SINGLE SYNC CHARACTER OPERATION



FOR DOUBLE SYNC CHARACTER OPERATION (BISYNC)



SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

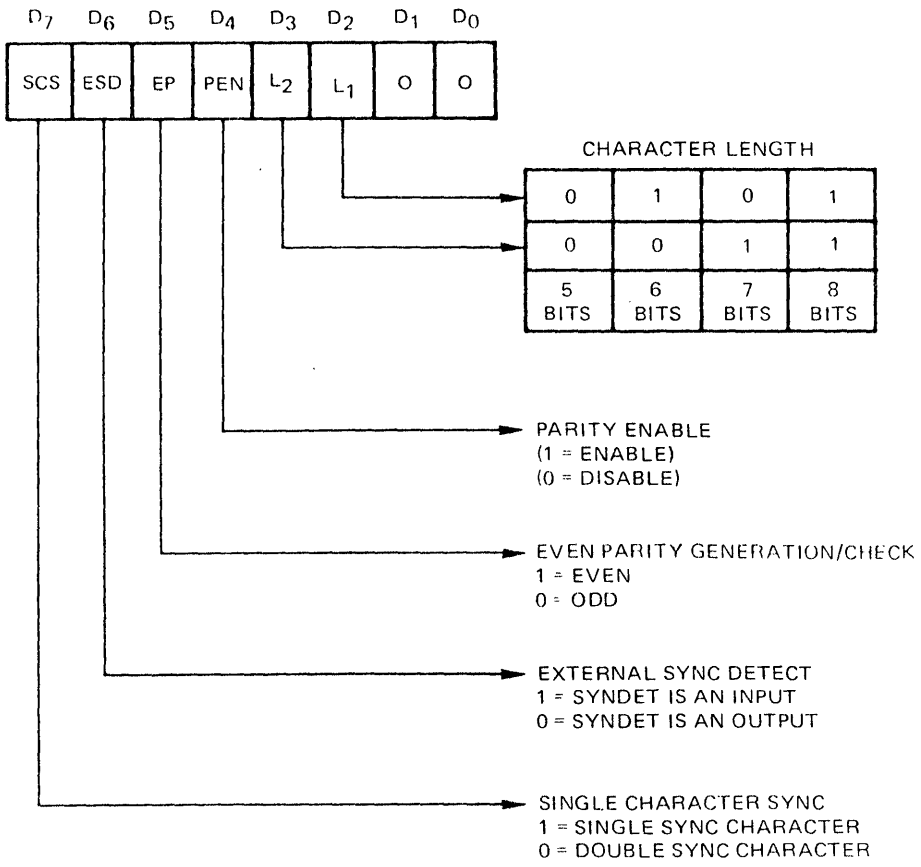
Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receiver Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251 leaves the HUNT mode and is in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

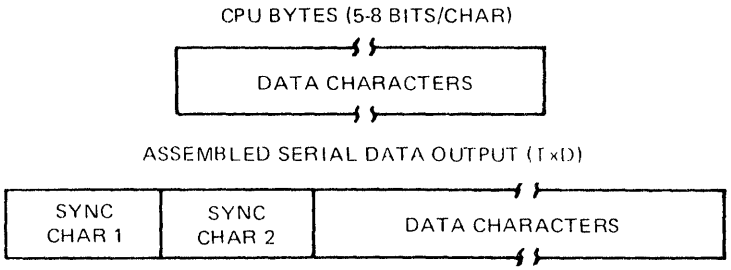
Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

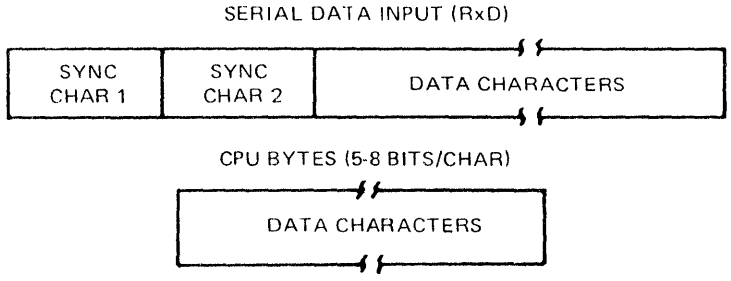
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251 has been specified by the Mode Instruction and the SYNC character(s) have been entered, if in SYNC mode, the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s), as needed, are loaded, all subsequent "control writes" ($C/\overline{D} = 1$) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251 to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the "status" of an active interface device to determine if errors have occurred or to notice other conditions which require a response from the processor. The μPD8251 has features which allow the processor to "read" the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251 to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of a 16 clock period.

PARITY ERROR

When a parity error is detected, the PE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

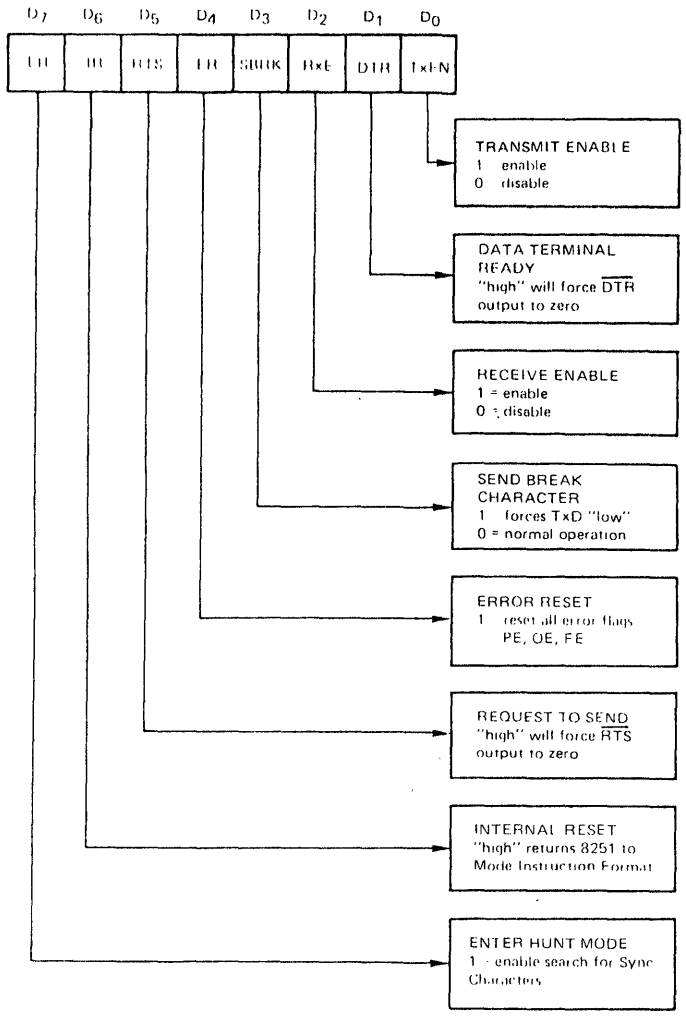
If the processor fails to read a data character before the one following is available, the OE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

FRAMING ERROR ①

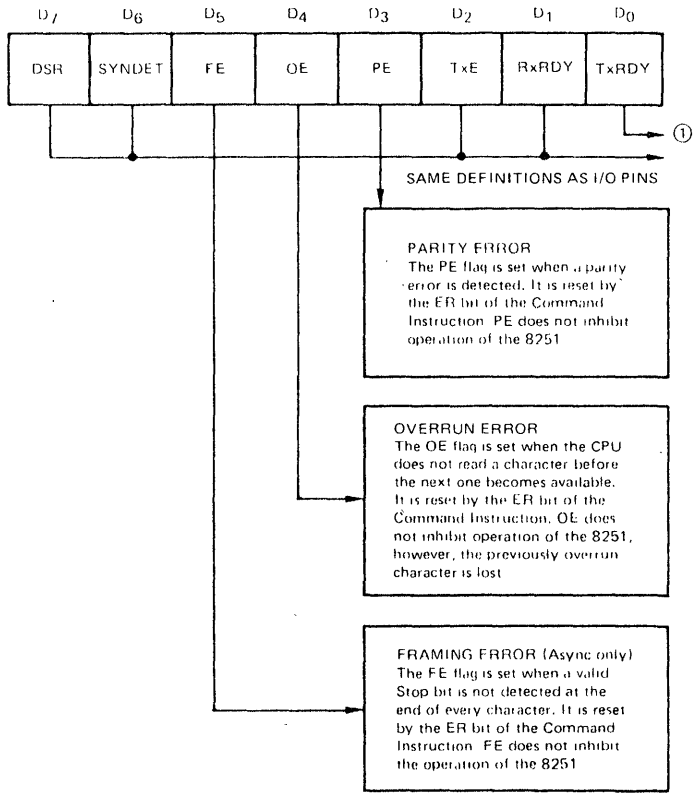
If a valid STOP bit is not detected at the end of a character, the FE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

Note: ① ASYNC mode only.

COMMAND INSTRUCTION FORMAT



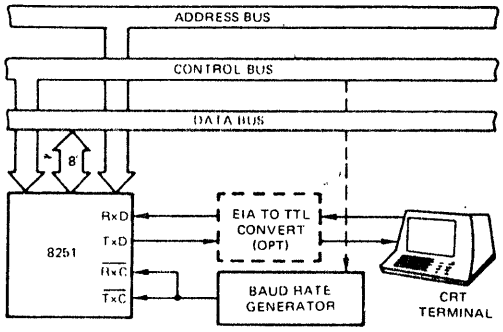
STATUS READ FORMAT



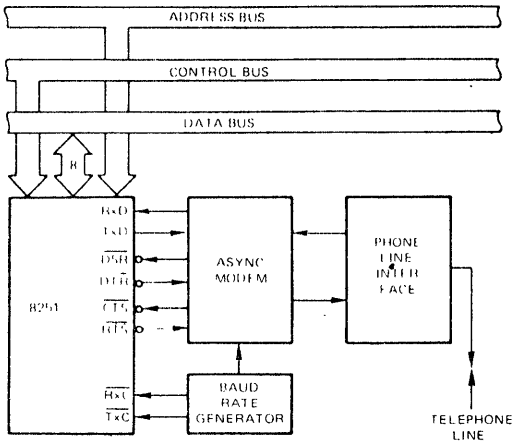
Note. ① TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

TxRDY status bit = DB Buffer Empty

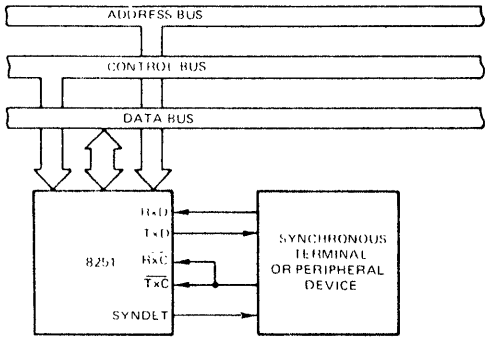
TxRDY (pin 15) = DB Buffer Empty • CTS • TxEn



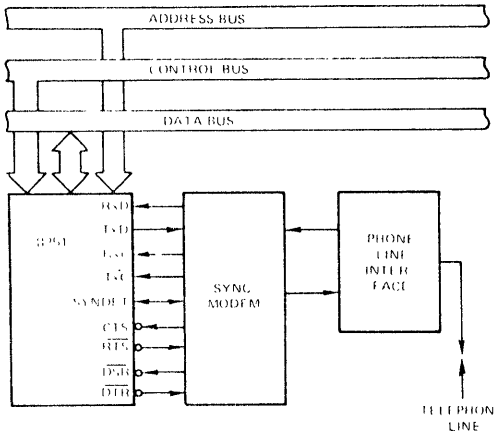
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES

SYSTEM.DEV 14 (COM1)

```
D269
0269: 47F83F0F 05300000 00000000 0000B907 'G.?.............'
0279: B1000000 000096F7 00000000 00000000 '................'
0289: 00000000 00000000 00000000 00000000 '................'
0299: 00000000 00000000 00000000 00000000 '................'
02A9: A7F35038 00000000 00003838 B800EF03 '..P8......88....'
02B9: 00000000 00000000 00000000 00000000 '................'
02C9: 00000000 00000000 00000000 00000000 '................'
02D9: 00000000 00000000 00000000 00000000 '................'
02E9: 00000000 00000000 00000000 00000000 '................'
02F9: 00000000 00000000 00000000 00000000 '................'
0309: A8F25038 00070000 00003800 3800FF00 '..P8......8.8...'
0319: 00000000 00000000 00000000 08000001 '................'
0329: 00000000 00000000 00000000 00000000 '................'
0339: 00000000 00000000 00000000 00000000 '................'
0349: 00000000 00000000 00000000 00000000 '................'
```

```
-LI F2A8 116T
F2A8  C3B7F2   JP   0F2B7      STATUS
F2AB  C343F3   JP   0F343      IN
F2AE  C351F3   JP   0F351      OUT
F2B1  C37BF3   JP   0F37B      INIT
F2B4  C3A2F3   JP   0F3A2      DEINIT
F2B7  DB11     IN   A,(11)     STATUS
 2B9  CB4F     BIT  1,A
F2BB  CADBF2   JP   Z,0F2DB
F2BE  C5       PUSH BC
F2BF  4F       LD   C,A
F2C0  DB10     IN   A,(10)
F2C2  E67F     AND  7F
F2C4  CB59     BIT  3,C
F2C6  2809     JR   Z,0F2D1
F2C8  CD74F3   CALL 0F374
F2CB  3E37     LD   A,37
F2CD  D311     OUT  (11),A
F2CF  3E3F     LD   A,3F
F2D1  C1       POP  BC
F2D2  CF66     SC   66
F2D4  38E1     JR   C,0F2B7
F2D6  CBFF     SET  7,A
F2D8  FD771E   LD   (IY+1E),A
F2DB  DB11     IN   A,(11)
F2DD  CB47     BIT  0,A
F2DF  285B     JR   Z,0F33C
F2E1  FDCB1C46 BIT  0,(IY+1C)
F2E5  200E     JR   NZ,0F2F5
F2E7  FDCB1C4E BIT  1,(IY+1C)
F2EB  200D     JR   NZ,0F2FA
F2ED  FDCB1C56 BIT  2,(IY+1C)
F2F1  202B     JR   NZ,0F31E
F2F3  1844     JR   0F339
F2F5  DB11     IN   A,(11)
 2F7  07       RLCA
F2F8  1843     JR   0F33D
F2FA  FD7E1E   LD   A,(IY+1E)
F2FD  CB7F     BIT  7,A
F2FF  280D     JR   Z,0F30E
F301  E67F     AND  7F
F303  FD771E   LD   (IY+1E),A
F306  FE13     CP   13
F308  280C     JR   Z,0F316
F30A  FE11     CP   11
F30C  280D     JR   Z,0F31B
F30E  FD7E1D   LD   A,(IY+1D)
F311  B7       OR   A
F312  2825     JR   Z,0F339
F314  1826     JR   0F33C
F316  FD771D   LD   (IY+1D),A
 319  18F3     JR   0F30E
 31B  AF       XOR  A
F31C  18F8     JR   0F316
F31E  FD7E1E   LD   A,(IY+1E)
F321  CB7F     BIT  7,A
F323  280D     JR   Z,0F332
F325  E67F     AND  7F
F327  FD771E   LD   (IY+1E),A
F32A  FE06     CP   6
F32C  2004     JR   NZ,0F332
F32E  FD361D00 LD   (IY+1D),0
F332  FD7E1D   LD   A,(IY+1D)
F335  FE80     CP   80
F337  3003     JR   NC,0F33C
F339  37       SCF
F33A  1801     JR   0F33D
F33C  B7       OR   A
F33D  FD7E1E   LD   A,(IY+1E)
F340  CB7F     BIT  7,A
F342  C9       RET
F343  CDB7F2   CALL 0F2B7      INPUT
F346  28FB     JR   Z,0F343
F348  FD7E1E   LD   A,(IY+1E)
F34B  E67F     AND  7F
F34D  FD771E   LD   (IY+1E),A
F350  C9       RET
F351  CDB7F2   CALL 0F2B7      OUTPUT
F354  30FB     JR   NC,0F351
 356  79       LD   A,C
F357  D310     OUT  (10),A
F359  FDCB1C56 BIT  2,(IY+1C)
F35D  C8       RET  Z
F35E  FD341D   INC  (IY+1D)
```

```
F30A  FE11      CP   11
F30C  280D      JR   Z,0F31B
F30E  FD7E1D    LD   A,(IY+1D)
F311  B7        OR   A
F312  2825      JR   Z,0F339
F314  1826      JR   0F33C
F316  FD771D    LD   (IY+1D),A
F319  18F3      JR   0F30E
F31B  AF        XOR  A
F31C  18F8      JR   0F316
F31E  FD7E1E    LD   A,(IY+1E)
F321  CB7F      BIT  7,A
F323  280D      JR   Z,0F332
F325  E67F      AND  7F
F327  FD771E    LD   (IY+1E),A
F32A  FE06      CP   6
F32C  2004      JR   NZ,0F332
F32E  FD361D00  LD   (IY+1D),0
F332  FD7E1D    LD   A,(IY+1D)
F335  FE80      CP   80
F337  3003      JR   NC,0F33C
F339  37        SCF
F33A  1801      JR   0F33D
F33C  B7        OR   A
F33D  FD7E1E    LD   A,(IY+1E)
F340  CB7F      BIT  7,A
F342  C9        RET
F343  CDB7F2    CALL 0F2B7          INPUT
F346  28FB      JR   Z,0F343
F348  FD7E1E    LD   A,(IY+1E)
F34B  E67F      AND  7F
F34D  FD771E    LD   (IY+1E),A
F350  C9        RET
F351  CDB7F2    CALL 0F2B7          OUTPUT
F354  30FB      JR   NC,0F351
F356  79        LD   A,C
F357  D310      OUT  (10),A
F359  FDCB1C56  BIT  2,(IY+1C)
F35D  C8        RET  Z
F35E  FD341D    INC  (IY+1D)
F361  FD7E1D    LD   A,(IY+1D)
F364  FE7F      CP   7F
F366  D8        RET  C
F367  CDB7F2    CALL 0F2B7
F36A  30FB      JR   NC,0F367
F36C  3E03      LD   A,3
F36E  D310      OUT  (10),A
F370  FD341D    INC  (IY+1D)
F373  C9        RET
F374  DB11      IN   A,(11)
F376  CB47      BIT  0,A
F378  28FA      JR   Z,0F374
F37A  C9        RET
F37B  3E8E      LD   A,8E           INIT
F37D  D311      OUT  (11),A
F37F  3E40      LD   A,40
F381  D311      OUT  (11),A
F383  FDCB087E  BIT  7,(IY+8)
F387  280C      JR   Z,0F395
F389  FDCB0876  BIT  6,(IY+8)
F38D  3E7A      LD   A,7A
F38F  2006      JR   NZ,0F397
F391  3E5A      LD   A,5A
F393  1802      JR   0F397
F395  3E4E      LD   A,4E
F397  D311      OUT  (11),A
F399  3E37      LD   A,37
F39B  D311      OUT  (11),A
F39D  FD361D00  LD   (IY+1D),0
F3A1  C9        RET
F3A2  3E40      LD   A,40           DEINIT
F3A4  D311      OUT  (11),A
F3A6  C9        RET
```

```
-B1 F2A8
 LI 0' 116T
 100' C3B7F2    JP   0F'
0003' C343F3    JP   9B'
0006' C351F3    JP   0A9'
0009' C37BF3    JP   0D3'
000C' C3A2F3    JP   0FA'
000F' DB11      IN   A,(11)         STATUS
0011' CB4F      BIT  1,A
0013' CADBF2    JP   Z,33'          ~ RxRDY
0016' C5        PUSH BC
0017' 4F        LD   C,A
0018' DB10      IN   A,(10)
001A' E67F      AND  7F
001C' CB59      BIT  3,C
001E' 2809      JR   Z,29'
0020' CD74F3    CALL 0CC'
0023' 3E37      LD   A,37
0025' D311      OUT  (11),A
0027' 3E3F      LD   A,3F
0029' C1        POP  BC
002A' CF66      SC   66
002C' 38E1      JR   C,0F'
002E' CBFF      SET  7,A
0030' FD771E    LD   (IY+1E),A
0033' DB11      IN   A,(11)
0035' CB47      BIT  0,A
0037' 285B      JR   Z,94'
0039' FDCB1C46  BIT  0,(IY+1C)      TxRDY
003D' 200E      JR   NZ,4D'
003F' FDCB1C4E  BIT  1,(IY+1C)
0043' 200D      JR   NZ,52'
0045' FDCB1C56  BIT  2,(IY+1C)
0049' 202B      JR   NZ,76'
004B' 1844      JR   91'
```

```
-B1 F2A8
LI 0' 116T
0000' C3B7F2    JP    0F'
0003' C343F3    JP    9B'
0006' C351F3    JP    0A9'
0009' C37BF3    JP    0D3'
000C' C3A2F3    JP    0EA'
000F' DB11      IN    A,(11)        STATUS
0011' CB4F      BIT   1,A
0013' CADBF2    JP    Z,33'         R-KBD
0016' C5        PUSH  BC
0017' 4F        LD    C,A
0018' DB10      IN    A,(10)
001A' E67F      AND   7F
001C' CB59      BIT   3,C
001E' 2809      JR    Z,29'
0020' CD74F3    CALL  0CC'
0023' 3E37      LD    A,37
0025' D311      OUT   (11),A
0027' 3E3F      LD    A,3F
0029' C1        POP   BC
002A' CF66      SC    66
002C' 38E1      JR    C,0F'
002E' CBFF      SET   7,A
0030' FD771E    LD    (IY+1E),A
0033' DB11      IN    A,(11)
0035' CB47      BIT   0,A
0037' 285B      JR    Z,94'
0039' FDCB1C46  BIT   0,(IY+1C)     T-KBD
003D' 200E      JR    NZ,4D'
003F' FDCB1C4E  BIT   1,(IY+1C)
0043' 200D      JR    NZ,52'
0045' FDCB1C56  BIT   2,(IY+1C)
0049' 202B      JR    NZ,76'
004B' 1844      JR    91'
004D' DB11      IN    A,(11)
004F' 07        RLCA
0050' 1843      JR    95'
0052' FD7E1E    LD    A,(IY+1E)
0055' CB7F      BIT   7,A
0057' 280D      JR    Z,66'
0059' E67F      AND   7F
005B' FD771E    LD    (IY+1E),A
005E' FE13      CP    13
0060' 280C      JR    Z,6E'
0062' FE11      CP    11
0064' 280D      JR    Z,73'
0066' FD7E1D    LD    A,(IY+1D)
0069' B7        OR    A
006A' 2825      JR    Z,91'
006C' 1826      JR    94'
006E' FD771D    LD    (IY+1D),A
0071' 18F3      JR    66'
0073' AF        XOR   A
0074' 18F8      JR    6E'
0076' FD7E1E    LD    A,(IY+1E)
0079' CB7F      BIT   7,A
007B' 280D      JR    Z,8A'
007D' E67F      AND   7F
007F' FD771E    LD    (IY+1E),A
0082' FE06      CP    6
0084' 2004      JR    NZ,8A'
0086' FD361D00  LD    (IY+1D),0
008A' FD7E1D    LD    A,(IY+1D)
008D' FE80      CP    80
008F' 3003      JR    NC,94'
0091' 01        SCF
0092' 1801      JR    95'
0094' B7        OR    A
0095' FD7E1E    LD    A,(IY+1E)
0098' CB7F      BIT   7,A
009A' C9        RET
009B' CDB7F2    CALL  0F'           INPUT
009E' 28FB      JR    Z,9B'
00A0' FD7E1E    LD    A,(IY+1E)
00A3' E67F      AND   7F
00A5' FD771E    LD    (IY+1E),A
00A8' C9        RET
00A9' CDB7F2    CALL  0F'           OUTPUT
00AC' 30FB      JR    NC,0A9'
00AE' 79        LD    A,C
00AF' D310      OUT   (10),A
00B1' FDCB1C56  BIT   2,(IY+1C)
00B5' C8        RET   Z
00B6' FD341D    INC   (IY+1D)
00B9' FD7E1D    LD    A,(IY+1D)
00BC' FE7F      CP    7F
00BE' D8        RET   C
00BF' CDB7F2    CALL  0F'
00C2' 30FB      JR    NC,0BF'
00C4' 3E03      LD    A,3
00C6' D310      OUT   (10),A
00C8' FD341D    INC   (IY+1D)
00CB' C9        RET
00CC' DB11      IN    A,(11)
00CE' CB47      BIT   0,A
00D0' 28FA      JR    Z,0CC'
00D2' C9        RET
00D3' 3E8E      LD    A,8E          INIT
00D5' D311      OUT   (11),A
00D7' 3E40      LD    A,40
00D9' D311      OUT   (11),A
00DB' FDCB087E  BIT   7,(IY+8)
00DF' 280C      JR    Z,0ED'
00E1' FDCB0876  BIT   6,(IY+8)
00E5' 3E7A      LD    A,7A
00E7' 2006      JR    NZ,0EF'
```

```
0092' 1801      JR   95'
0094' B7        OR   A
0095' FD7E1E    LD   A,(IY+1E)
0098' CB7F      BIT  7,A
009A' C9        RET
009B' CDB7F2    CALL 0F'          INPUT
009E' 28FB      JR   Z,9B'
00A0' FD7E1E    LD   A,(IY+1E)
00A3' E67F      AND  7F
00A5' FD771E    LD   (IY+1E),A
00A8' C9        RET
00A9' CDB7F2    CALL 0F'          OUTPUT
00AC' 30FB      JR   NC,0A9'
00AE' 79        LD   A,C
00AF' D310      OUT  (10),A
00B1' FDCB1C56  BIT  2,(IY+1C)
00B5' C8        RET  Z
00B6' FD341D    INC  (IY+1D)
00B9' FD7E1D    LD   A,(IY+1D)
00BC' FE7F      CP   7F
00BE' D8        RET  C
00BF' CDB7F2    CALL 0F'
00C2' 30FB      JR   NC,0BF'
00C4' 3E03      LD   A,3
00C6' D310      OUT  (10),A
00C8' FD341D    INC  (IY+1D)
00CB' C9        RET
00CC' DB11      IN   A,(11)
00CE' CB47      BIT  0,A
00D0' 28FA      JR   Z,0CC'
00D2' C9        RET
00D3' 3E8E      LD   A,8E         INIT
00D5' D311      OUT  (11),A
00D7' 3E40      LD   A,40
00D9' D311      OUT  (11),A
00DB' FDCB087E  BIT  7,(IY+8)
00DF' 280C      JR   Z,0ED'
00E1' FDCB0876  BIT  6,(IY+8)
00E5' 3E7A      LD   A,7A
00E7' 2006      JR   NZ,0EF'
00E9' 3E5A      LD   A,5A
00EB' 1802      JR   0EF'
00ED' 3E4E      LD   A,4E
00EF' D311      OUT  (11),A
00F1' 3E37      LD   A,37
00F3' D311      OUT  (11),A
00F5' FD361D00  LD   (IY+1D),0
00F9' C9        RET
00FA' 3E40      LD   A,40         DEINIT
00FC' D311      OUT  (11),A
00FE' C9        RET
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