Part Number 30002-3

# MODEL DQ130
# MAGNETIC TAPE COUPLER
# INSTRUCTION MANUAL

January 1984


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# DESCRIPTION

## INTRODUCTION

This manual describes the installation, operation, programming, troubleshooting and theory of operation of Distributed Logic Corporation (DILOG) Model DQ130 Magnetic Tape Coupler. The coupler interfaces DEC* LSI-11 based computer systems to Industry-Standard formatted magnetic tape drives.

The coupler and the drive comprise a complete LSI-11 compatible 9-track magnetic tape subsystem. Magnetic tape drives from manufacturers other than DEC can be used while still retaining software and format compatibility with the DEC TM-11 Tape System. Data transfers are via the DMA facility of the LSI-11. Transfer rates vary, depending upon the density and speed of the drives included in the system, between 10,000 and 200,000 characters per second. The complete coupler occupies one quad module in the backplane.

## COUPLER CHARACTERISTICS

Up to two embedded-formatter tape drives or external stand-alone tape formatters may be connected to the coupler. Each embedded-formatter tape drive is capable of handling an additional three slave drives. All Industry-Standard, external stand-alone formatters are capable of handling up to four drives. The coupler can accommodate up to eight drives. Figures 1-1 and 1-2 illustrate two configurations.

The optimal usage of the coupler is in situations where 9-track, dual density, 800/1600/3200 bpi tape recording capabilities are required; however, the coupler is compatible with single density 800, 1600 or 3200 bpi embedded-formatter tape drives or stand-alone external formatters.

The primary functions of the coupler in a magnetic tape subsystem are to buffer and interlock data and status transfers between the computer I/O bus and the tape formatter, and to translate CPU commands into tape formatter control signals such as Start, Stop, Rewind, Generate IR Gap, Generate EOF Gap. The primary function of the formatter is to control tape motion, establish data format, and perform error checking. The overall tape control function is a combination of the coupler functions, which are related to the LSI-11, and the formatter functions, which are related to the tape drives.

A microprocessor is the sequence and timing center of the coupler. The control information is stored as firmware instructions in Programmable Read-Only Memory (PROM) on the coupler board. One section of the PROM contains a diagnostic program that tests the functional operation of the coupler. This self-test is performed automatically each time power is applied or whenever an INIT command is issued on the CPU I/O bus. A green

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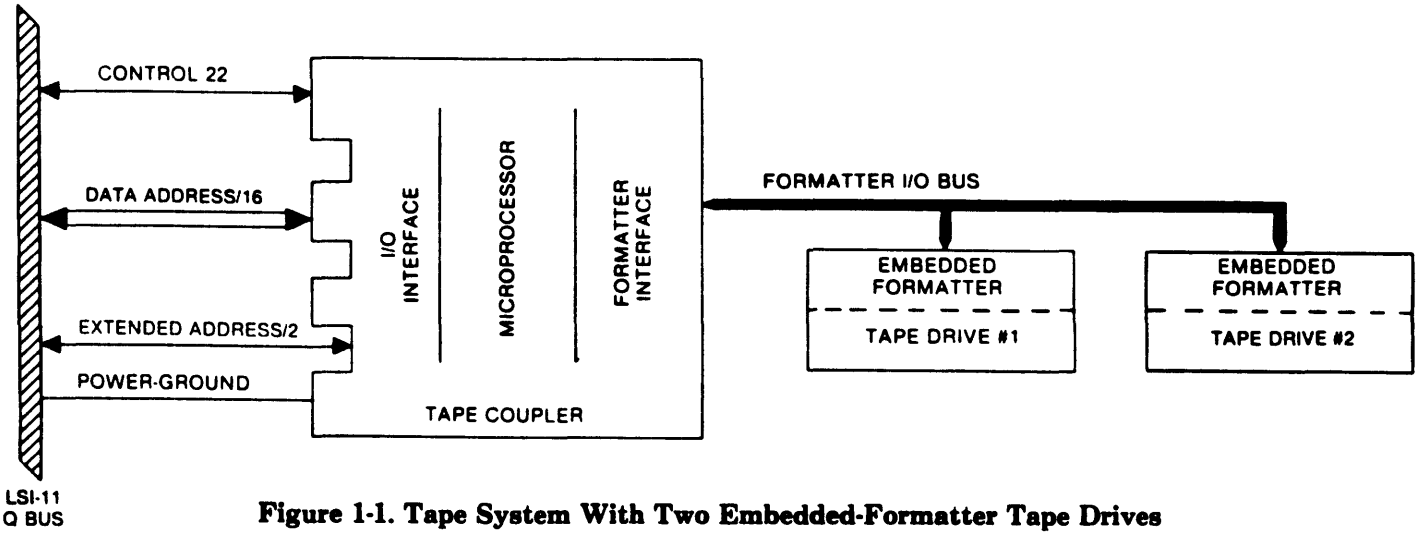



**Figure 1-1. Tape System With Two Embedded-Formatter Tape Drives**

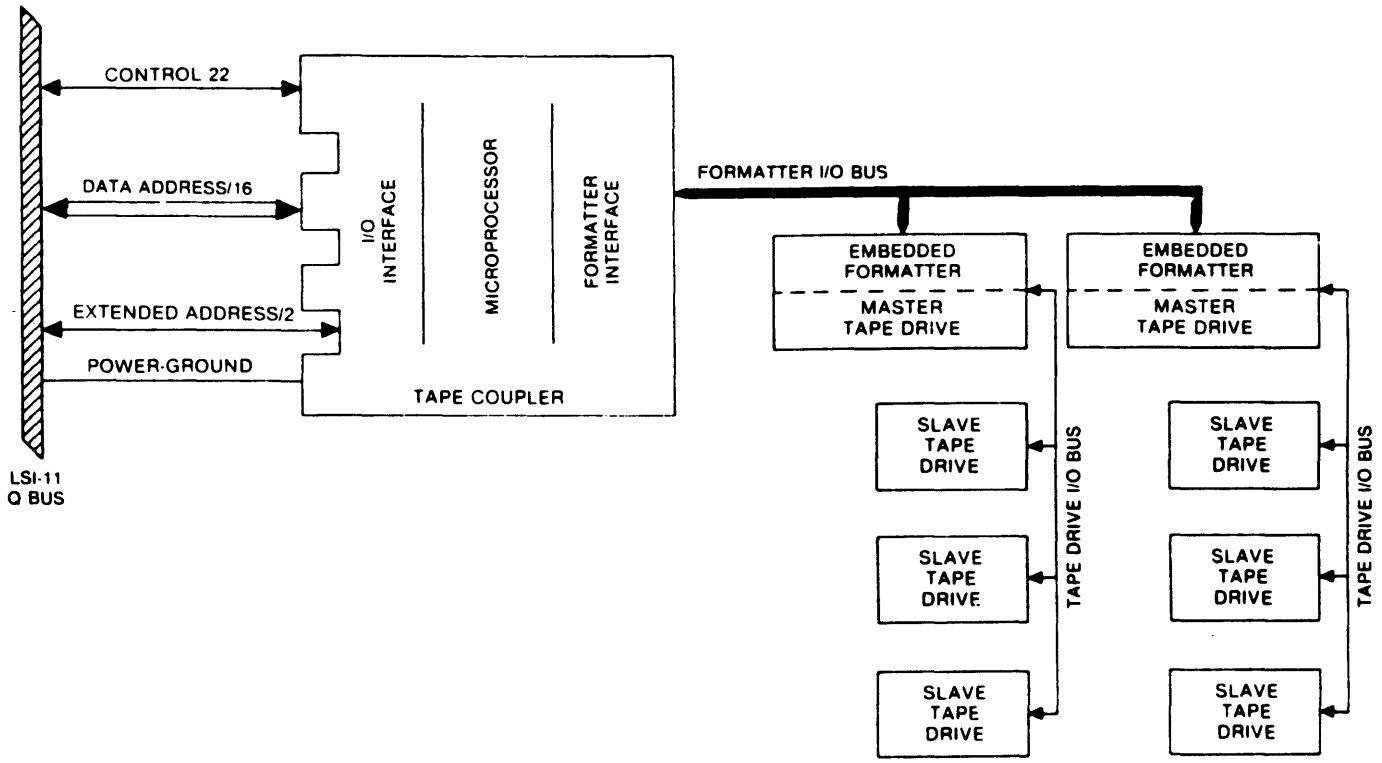



**Figure 1-2. Tape System (Maximum Configuration) Two Embedded-Formatter Tape Drives With Three Slave Tape Drives Each**

diagnostic indicator on the board lights if self-test passes. If self-test fails, the coupler has an automatic data protect feature that stops the CPU from interacting with the tape formatter, and thus prevents writing erroneous information into critical data base areas.

Two additional indicators on the coupler board display dynamic operating conditions to an operator. The conditions displayed are Coupler Busy and Coupler Transferring Data (DMA Busy).

## LSI-11 Q BUS INTERFACE

Commands, data and status transfers between the coupler and the computer are executed via the parallel I/O bus (Q Bus) of the computer directly to memory, via the DMA facility of the Q Bus. Coupler/Q Bus interface signals are listed in Table 1-1.

## FORMATTER INTERFACE

The coupler interfaces with the formatted tape drives through two 50-pin flat cable connectors at the top of the coupler board. The maximum cable length between coupler and formatter is 25 feet. Coupler/formatter interface signals are listed in Tables 1-2 and 1-3.

Table 1-4 lists some manufacturers and connector correlations.

### CAUTION

*Cable connections and interface signals should be checked from the drive manufacturers' manuals to ensure the latest configurations are installed correctly. Incorrect cabling may cause damage to the coupler or the drive.*

## TAPE FORMAT COMPATIBILITY

The coupler can cause the formatter to create a tape in an IBM format. By cutting an etch, the high byte will be written first followed by the low byte. With a jumper (etch) installed, the format will be low byte first followed by the high byte. The tape can be created on the DEC system and run and read on another system.

## INTERRUPT

The interrupt vector address is factory set to address 224, which is compatible with TM-11 software. Interrupts are generated when processor attention is required or when an error occurs.

## Table 1-1. Coupler/Q-Bus Interface Lines

| Bus Pin | Mnemonic | Controller Input/ Output | Description |
|---|---|---|---|
| AJ1, AM1, RT1, BJ1, BM1, BT1, BC2, CJ1, CM1, CT1, CC2, DJ1, DM1, DT1, DC2 | GND | O | Signal Ground and DC return. |
| AN1 | BDMR L | O | Direct Memory Access (DMA) request from coupler: active low. |
| AP1 | BHALT L | N/A | Stops program execution. Refresh and DMA are enabled. Console operation is enabled. |
| AR1 | BREF L | N/A | Memory Refresh. |
| BA1 | BDCOK H | I | DC power OK. All DC voltages are normal. |
| BB1 | BPOK H | N/A | Primary power OK. When low activates power fail trap sequence. |
| BN1 | BSACK L | O | Select Acknowledge. Interlocked with BDMGO indicating coupler is bus master in a DMA sequence. |
| BR1 | BEVNT L | N/A | External Event Interrupt Request. |
| BV1, AA2, BA2, CA2, DA2 | +5 | I | +5 volt system power. |
| AD2, BD2 | +12 | N/A | +12 volt system power. |
| AE2 | BDOUT L | I/O | Data Out. Valid data from bus master is on the bus. Interlocked with BRPLY. |
| AF2 | BRPLY L | I/O | Reply from slave to BDOUT or BDIN and during IAK. |
| AH2 | BDIN L | I/O | Data Input. Input transfer to master (states master is ready for data). Interlocked with BRPLY. |
| AJ2 | BSYNC L | I/O | Synchronize: becomes active when master places address on bus; stays active during transfer. |
| AK2 | BWTBT L | I/O | Write Byte: indicates output sequence to follow (DATO or DATOB) or marks byte address time during a DATOB. |
| AL2 | BIRQ L | O | Interrupt Request. |
| AM2<br>AN2<br>CM2<br>CN2 | BIAK1I L<br>BIAK1O L<br>BIAK2I L<br>BIAK2O L | I<br>O<br>I<br>O | Serial Interrupt Acknowledge input and output lines routed from Q Bus, through devices, and back to processor to establish an interrupt priority chain. |
| AT2 | BINIT L | I | Initialize. Clears devices on I/O bus. |
| AU2, AV2, BE2, BF2, BH2, BJ2, BK2, BL2, BM2, BN2, BP2, BR2, BS2, BT2, BU2, BV2 | BDAL0 L through BDAL15 L | I/O | Data/address lines, 0-15 |
| AR2<br>AS2<br>CR2<br>CS2 | BDMG1I L<br>BDMG1O L<br>BDMG2I L<br>BDMG2O L | I<br>O<br>I<br>O | DMA Grant Input and Output. Serial DMA priority line from computer, through devices and back to computer. |
| AP2 | BBS7 L | I | Bank 7 Select. Asserted by bus master when address in upper 4K bank is placed on the bus. |

**Table 1-2. Coupler Connector J1 Formatter Interface Lines**

| J1 Signal | J1 Return | Mnemonic | Description |
|---|---|---|---|
| 1 | | FRDP | Read Data Parity |
| 2 | | FRD0 | Read Data 0 |
| 3 | | FRD1 | Read Data 1 |
| 4 | | FLDP | Load Point |
| 6 | 5 | FRD4 | Read Data 4 |
| 8 | 7 | FRD7 | Read Data 7 |
| 10 | 9 | FRD6 | Read Data 6 |
| 12 | 11 | FHER | Hard Error |
| 14 | 13 | FFMK | File Mark |
| 16 | 15 | FCCG/ID | CCG/IDENT |
| 18 | 17 | FFEN | Formatter Enable |
| 20 | 19 | FRD5 | Read Data 5 |
| 22 | 21 | FEOT | End of Tape |
| 24 | 23 | FOFL | Off Line |
| 26 | 25 | FNRZ | NRZI |
| 28 | 27 | FRDY | Ready |
| 30 | 29 | FRWD | Rewinding |
| 32 | 31 | FFPT | File Protect |
| 34 | 33 | FRSTR | Read Strobe |
| 36 | 35 | FDWDS | Demand Write Data Strobe |
| 38 | 37 | FDBY | Data Busy |
| 40 | 39 | | Not Used |
| 42 | 41 | FCER | Corrected Error |
| 44 | 43 | FONL | On-Line |
| 46 | 45 | FTAD1 | Transport Address 1 |
| 48 | 47 | FFAD | Formatter Address |
| 50 | 49 | FDEN | Speed/Density Select |

**Table 1-3. Coupler Connector J2 to Formatter Interface Lines**

| J2 Signal | J2 Return | Mnemonic | Description |
|---|---|---|---|
| 2 | 1 | FFBY | Formatter Busy |
| 4 | 3 | FLWD | Last Word |
| 6 | 5 | FWD4 | Write Data 4 |
| 8 | 7 | FGO | Initiate Command |
| 10 | 9 | FWD0 | Write Data 0 |
| 12 | 11 | FWD1 | Write Data 1 |
| 14 | 13 | | Not Used |
| 16 | 15 | FLOL | Load on Line |
| 18 | 17 | FREV | Reverse/Forward |
| 20 | 19 | FREW | Rewind |
| 22 | 21 | FWDP | Not Used |
| 24 | 23 | FWD7 | Write Data 7 |
| 26 | 25 | FWD3 | Write Data 3 |
| 28 | 27 | FWD6 | Write Data 6 |
| 30 | 29 | FWD2 | Write Data 2 |
| 32 | 31 | FWD5 | Write Data 5 |
| 34 | 33 | FWRT | Write/Read |
| 36 | 35 | FRTH2 FLGAP* | Read Threshold 2 |
| 38 | 37 | FEDIT | Edit |
| 40 | 39 | FERASE | Erase |
| 42 | 41 | FWFM | Write File Mark |
| 44 | 43 | FRTH1 (SPARE) | Read Threshold 1 |
| 46 | 45 | FTAD0 | Transport Address 0 |
| 48 | 47 | FRD2 | Read Data 2 |
| 50 | 49 | FRD3 | Read Data 3 |

*Signal applicable to CDC Keystone drives.

**Table 1-4. Coupler to Formatter Connection Correlation**

| Coupler Connector J1 to: | | |
|---|---|---|
| **Manufacturer** | **Model** | **Connector** |
| CDC | 9218X | J5 |
| Cipher | F880 | P2 |
| | F100X, F900X (Adapter required) | P5 |
| Digi-Data | Formatted | JD |
| IDT | 1012 | J2 |
| | 1050 | J125 |
| Kennedy | 6809 Streamer | J2 |
| | Formatted | J1 |
| Pertec | Formatted | P5 |
| | External Formatter (Adapter required) | P5 |

| Coupler Connector J2 to: | | |
|---|---|---|
| **Manufacturer** | **Model** | **Connector** |
| CDC | 9218X | J4 |
| Cipher | F880 | P1 |
| | F100X, F900X (Adapter required) | P4 |
| Digi-Data | Formatted | JC |
| IDT | 1012 | J1 |
| | 1050 | J124 |
| Kennedy | 6809 Streamer | J1 |
| | Formatted | J5 |
| Pertec | Formatted | P4 |
| | External Formatter (Adapter required) | P4 |

## COUPLER SPECIFICATIONS*

Data Format

- Industry-Standard non-return-to-zero (NRZ) or Phase Encoded (PE) recording.
- 9 tracks

Recording densities:

- 800 characters per inch
- 1600 characters per inch
- 3200 characters per inch
- Interrecord gap 0.60 inch min.
- Tape parity marks: LPC, CRC, LRC

Media Characteristics

Type

- ½" wide mylar base, oxide coated, magnetic tape.

Reel Size

- 7", 8½", or 10½" diameter tape reels containing 600, 1,200 and 2,400 feet of tape respectively.

Data Capacity (megabytes)

- Assumes aproximate 80% recording efficiency:

| | | 800 CPI | 1600 CPI | 3200 CPI |
|---|---|---|---|---|
| 600 Ft. | = | 5.75 | 11.5 | 23.0 |
| 1,200 Ft. | = | 11.5 | 23.0 | 46.0 |
| 2,400 Ft. | = | 22.0 | 44.0 | 88.0 |

Data Transfer Rate (Characters/Second)

| | | 800 CPI | 1600 CPI | 3200 CPI |
|---|---|---|---|---|
| 12.5 ips | = | 10,000 | 20,000 | 20,000 |
| 25.0 ips | = | 20,000 | 40,000 | 40,000 |
| 37.5 ips | = | 30,000 | 60,000 | 60,000 |
| 45.0 ips | = | 36,000 | 72,000 | 72,000 |
| 75.0 ips | = | 60,000 | 120,000 | 120,000 |
| 125.0 ips | = | 100,000 | 200,000 | 200,000 |

Register Address
- Status (MTS) 772 520
- Command (MTC) 772 522
- Byte Record Counter (MTBRC) 772 524
- Current Memory Address (MTCMA) 772 526
- Data Buffer (MTD) 772 530
- Tape Read Lines (MTRD) 772 532

Computer Interface
- Interrupt Vector Address 224. DMA data transfer. 1 bus load all lines.

Coupler/Formatter Interface
- Coupler is compatible with formatters manufactured by Pertec, Kennedy, Tandberg, Cipher, CDC, Digi-Data.

Packaging
- The coupler is completely contained on one quad module 10.44 inches wide by 8.88 inches deep.

Documentation
- One instruction manual is supplied with the coupler.

Software
- One diagnostic routine with object listing is supplied with a coupler (or the first of a series of couplers).

Power
- +5, ±0.25 VDC at 3.6 amps, from computer backplane.

Environment
- Operating temperature 40°F to 140°F
- Operating humidity 10% to 95% non-condensing.

**Note**

*The quality of recording and reading information on magnetic tape is affected by temperature and humidity. The area where the tape is used should be maintained within the following limits:*
*Temperature: 60°F to 90°F*
*Humidity: 20% to 80%*

Shipping Weight
- 5 pounds including documentation.

*Specifications subject to change without notice.

# SECTION 2
# INSTALLATION

## INSPECTION

The padded shipping carton that contains the coupler board also contains an instruction manual and cables to the magnetic tape drives (if this option is exercised). The coupler is completely contained on one quad-size printed circuit board. The drive (or drives), if supplied, is contained in a separate shipping carton. Inspect the coupler and cable(s) for damage.

**CAUTION**

*If damage to any of the components is noted, do not install. Immediately inform the carrier and DILOG.*

Installation instructions for the tape drive are contained in the tape drive manual. Before installing any components of the magnetic tape system, read Sections 1, 2 and 3 of this manual. Figure 2-1 illustrates the configuration of the coupler.

## PRE-INSTALLATION CHECKS

There are various LSI-11 configurations for LSI-11 based systems. Certain configurations require minor modifications before operating the magnetic tape system. These modifications are as follows:

A. If the system contains a REV11-C module, it must be placed closer to the processor module (higher priority) than the coupler if the DMA refresh logic on the REV11-C is enabled.

B. If the 4K memory on the DK11-F is not used and the memory in the system does not require external refresh, the DMA refresh logic on the REV11-C should be disabled by removing jumper W2 on the REV11-C module.

C. If the system contains a REV11-A module, the refresh DMA logic must be disabled since the module must be placed at the end of the bus (REV11-A contains bus terminator).

D. If the REV11-C module is installed, cut the etch to pin 12 on circuit D30 (top of board) and add a jumper between pin 12 and pin 13 of D30.

E. If the system requires more than one backplane, place the REV-11 terminator in the last available location in the last backplane.

## INSTALLATION

To install the coupler module, proceed as follows:

**CAUTION**

*Remove DC power from mounting assembly before inserting or removing the coupler module.*

*Damage to the backplane assembly may occur if the coupler module is plugged in backwards.*

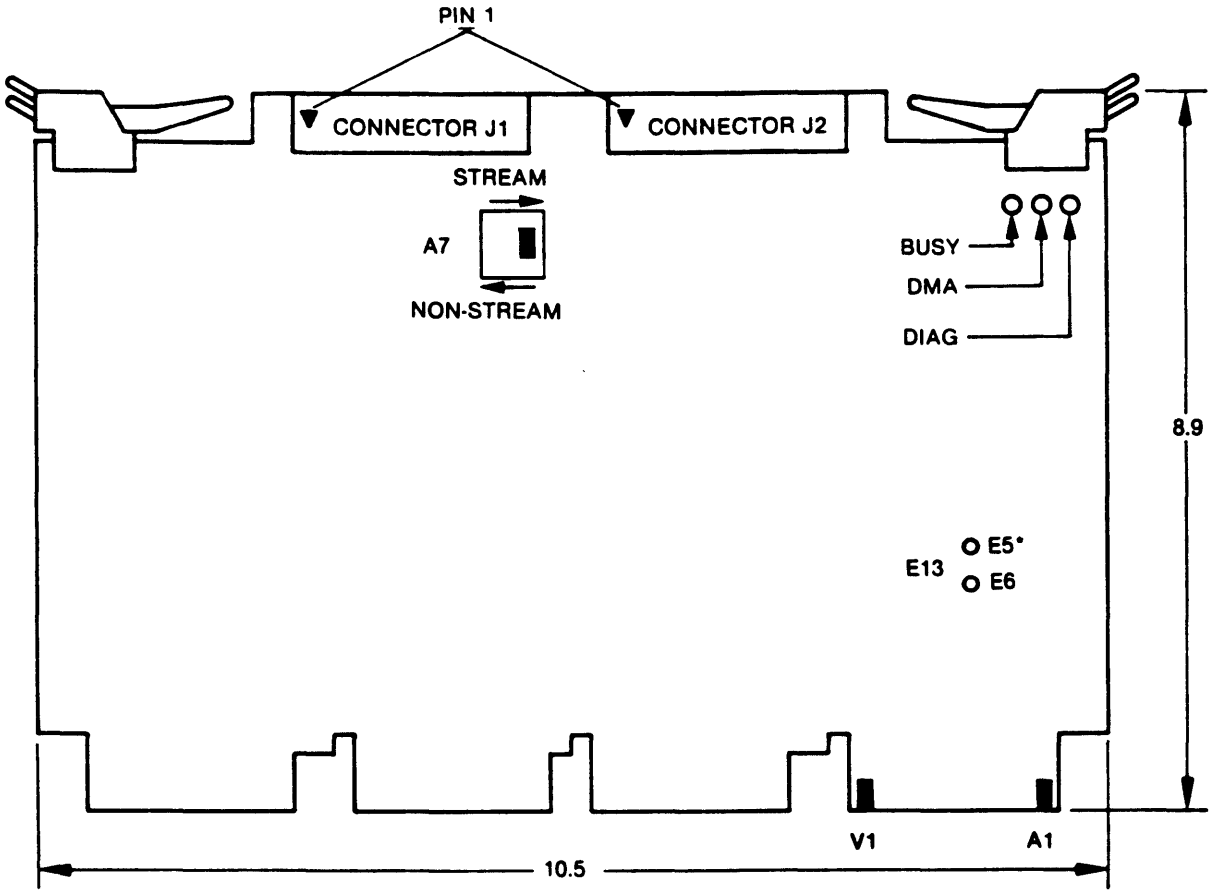
1. Select the backplane location into which the coupler is to be inserted.

   There are several backplane assemblies available from DEC and other manufacturers. Figure 2-2 shows typical backplane configurations. Note that the processor module is always installed in the first location of the backplane or in the first location in the first backplane of multiple backplane systems.

   It is important that all option slots between the processor and the coupler be filled to ensure that the daisy-chained interrupt (BIAK) and DMA (BDMG) signals be complete to the coupler slots. If there must be empty slots between the coupler and any option board, the following backplane jumpers must be installed:

| FROM | TO | SIGNAL |
|---|---|---|
| C0 x NS | C0 x M2 | BIAK1/L0 |
| C0 x S2 | C0 x R2 | BDMG1/L0 |
| ↑ Last Full Option Slot | ↑ Coupler Slot | |

2. Ensure the switch and jumpers are as shown in Figure 2-1.




*When jumper is installed at E13, coupler writes DEC Format (low byte first, high byte second).
When jumper is removed at E13, coupler writes IBM format (high byte first, low byte second).

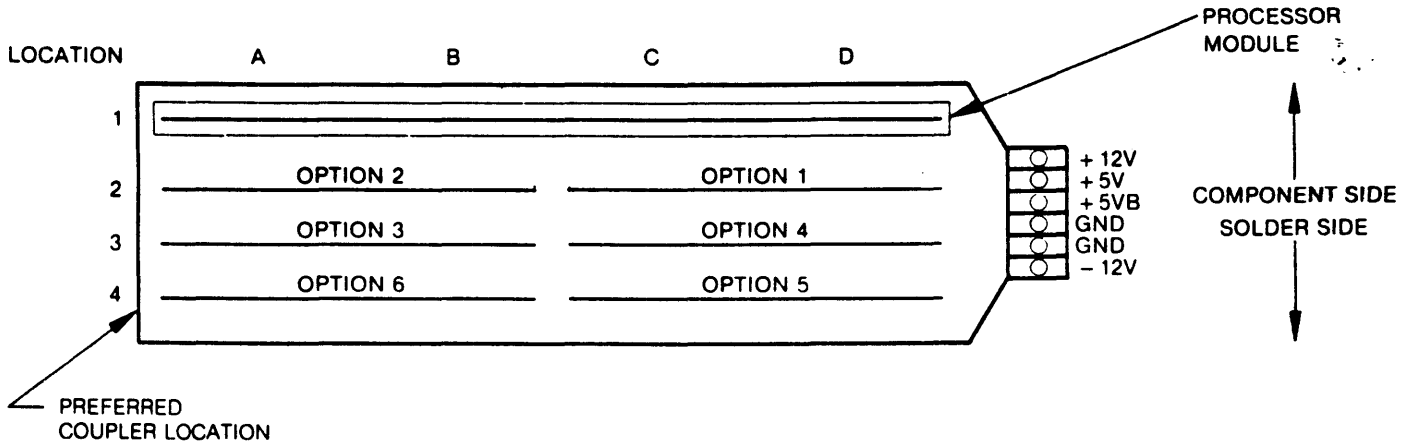
**LOCATION A7**

| Stream Switch OFF | | | Stream Switch ON* | | |
|---|---|---|---|---|---|
| Logical Unit Addressed | Formatter Addressed | Physical Drive Addressed | Logical Unit Addressed | Mode | Physical Drive Addressed |
| 0 | 0 | 0 | 0 | Stop/Start | 0 |
| 1 | 0 | 1 | 1 | Stop/Start | 1 |
| 2 | 0 | 2 | 2 | Stop/Start | 2 |
| 3 | 0 | 3 | 3 | Stop/Start | 3 |
| 4 | 1 | 0 | 4 | Streaming | 0 |
| 5 | 1 | 1 | 5 | Streaming | 1 |
| 6 | 1 | 2 | 6 | Streaming | 2 |
| 7 | 1 | 3 | 7 | Streaming | 3 |

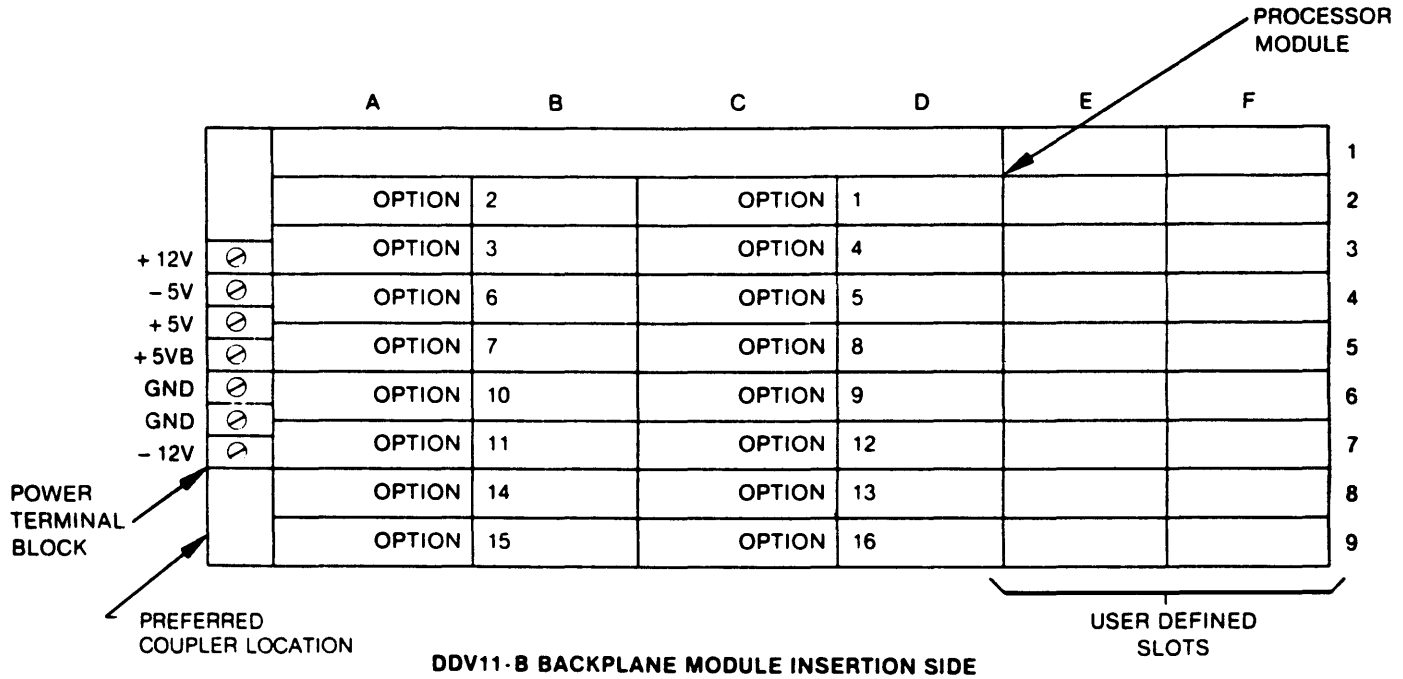
*Formatter Addressed Always 0.

Older coupler boards (Rev. E and earlier) contain Jumpers E1, E2, E3 and E4 at Location A7, rather than the STREAM switch (Rev. F and later). The older boards operated only in an 18-bit addressing mode: the newer ones are capable of 22-bit addressing. For the older boards to operate in the Streamer mode, the following changes must be made:


**Figure 2-1. Coupler Configuration**




H9270 MODULE INSERTION SIDE




DDV11-B BACKPLANE MODULE INSERTION SIDE

**NOTE**

*MEMORY CAN BE INSTALLED IN ANY SLOT; IT IS NOT PRIORITY DEPENDENT AND DOES NOT NEED TO BE ADJACENT TO THE PROCESSOR.*
*CONTROLLERS ARE ALSO COMPATIBLE WITH H9273A MODULES.*

**Figure 2-2. Typical Backplane Configuration**

3. If the formatter is equipped with a 100-pin connector, adapter part number ACC993A must be used to convert the 100-pin connector to two 50-pin connectors. Adapter part number ACC993B is used for 72-pin connectors.

4. Insert the coupler into the selected backplane position. Be sure the coupler is installed with the components facing row one, the processor.

   The coupler module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors into the backplane then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.

5. Feed the module connector end of the tape drive cable(s) into the coupler module connector(s). Install the cable connector(s) into the module connector(s). Verify that the connector(s) are firmly seated.

6. Connect the drive end of the I/O cables to the drive I/O connectors.

7. Apply power to the computer and verify that the green diagnostic LED indicator on the coupler board is lighted. If the DIAG LED is not lighted, either power is not applied to the coupler, the coupler board is bad, or the LED is bad.

8. Refer to the tape drive manual for operating instructions and apply power to the tape drive. Install a known good reel of tape on the tape drive and place the tape drive ON LINE.

9. Place the computer in the HALT mode to enable ODT. Using the computer terminal examine location 772 520. The contents of this location should be 000 141. These are the tape drive status bits signifying: ON LINE, BEGINNING OF TAPE, and TAPE UNIT READY.

10. Using the computer console device, deposit 60007 into location 772 522. The tape should move forward approximately 6 inches and stop. A file mark should have been written on the tape. Examine location 772 520. The contents of this location should be 040 101 signifying that a file mark has been written and detected.

11. Refer to the DILOG software manual and run the diagnostics.

12. The tape system is now ready for data transfer operations.

# SECTION 3
# OPERATION

## INTRODUCTION

Prior to operating the system, the instruction manual sections describing the controls and indicators on the tape drive and procedures for mounting and removing tape reels should be read. To prevent loss of data or damage to the magnetic tape, the following precautions should be observed:

a. Always handle a tape reel by the hub hole. Squeezing the reel flanges can cause damage to the tape edges when winding or unwinding tape.

b. Never touch the portion of tape between the BOT and EOT markers. Oils from fingers attract dust and dirt. Do not allow the end of the tape to drag on the floor.

c. Never use a contaminated reel of tape. This spreads dirt to clean tape reels and can affect tape drive operation.

d. Always store tape reels inside their containers. Keep empty containers closed so dust and dirt cannot get inside.

e. Inspect tapes, reels, and containers for dust and dirt. Replace take-up reels that are old or damaged.

f. Do not smoke near the tape drive or tape storage area. Tobacco smoke and ash are especially damaging to tape.

g. Do not place the tape drive near a line printer or other device that produces paper dust.

h. Clean the tape path frequently.

Note that tape drives permit off-line or on-line operation. The off-line mode is controlled by switches on the tape drive. The on-line mode is controlled by programmed commands from the computer via the coupler and formatter. When system operation is desired, be sure the tape drive ON-LINE indicator is lit. On-line operation is a function of program commands described in Section 4 of this manual.

## TAPE FORMAT

For detailed information on tape format characteristics see formattter and tape drive manuals.

## BOOTING FROM MAGNETIC TAPES

1. Place the tape transport "ON LINE" and position the tape at "Beginning of Tape."
2. Load Register location 772 $522_8$ with $10000_8$.
3. Load Register location 772 $524_8$ with $177777_8$ $(-1)$.
4. Load Register location 772 $522_8$ with $60011_8$. The tape will jump forward and halt.
5. Load Register location 772 $522_8$ with $60003_8$. The tape will jump forward and halt.
6. Load PSW ($S) with $350_8$.
7. Load PC (R7) with 0.
8. Type "P" to start.

## STREAMING TAPE TRANSPORTS

With the STREAMING switch on, the tape drive will function in the low-speed STOP/START mode when addressed as logical unit number 0, when addressed as logical unit number 4, the streamer will function in the high-speed, streaming mode.

# SECTION 4
# PROGRAMMING

## PROGRAMMING DEFINITIONS

*FUNCTION:* The expected activity of the tape system (read, write, rewind).

*COMMAND:* The instruction which initiates a function.

*INSTRUCTION:* One or more orders executed in a prescribed sequence that cause a function to be performed.

*ADDRESS:* The binary code placed on the BDAL0-BDAL21 lines by the bus master to select a register in a slave device. Note that "register" can be either discrete elements (flip flops) or memory elements (core, solid state RAM or ROM). When addressing devices other than computer internal memory, i.e., peripheral device registers, the upper 8K bytes address space is used.

*REGISTER:* An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system.

## TAPE COUPLER FUNCTIONS AND REGISTERS

The tape coupler performs eight functions. A function is initiated by a Go command after the processor has issued a series of instructions that store function-control information into coupler registers. To accept a command, and perform a function, the coupler must be properly addressed and the tape drives must be powered up, at operational speed, and be ready.

All software interaction between the coupler, the processor, and processor memory is accomplished by seven registers in the tape coupler. These registers are assigned memory addresses and can be read or written into (except as noted) by instructions that reference respective register addresses. A summary of the registers, their addresses, mnemonics, and their bit assignments are shown in Figure 4-1.

**Table 4-1. Function Codes**

| BIT 3 | BIT 2 | BIT 1 | BIT 0(60) | Octal | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 00 | Off line |
| 0 | 0 | 1 | 1 | 11 | Read |
| 0 | 1 | 0 | 1 | 05 | Write |
| 0 | 1 | 1 | 1 | 07 | Write EOF |
| 1 | 0 | 0 | 1 | 10 | Space Forward |
| 1 | 0 | 1 | 1 | 13 | Space Reverse |
| 1 | 1 | 0 | 1 | 15 | Write with Extended Interrecord Gap |
| 1 | 1 | 1 | 1 | 17 | Rewind |

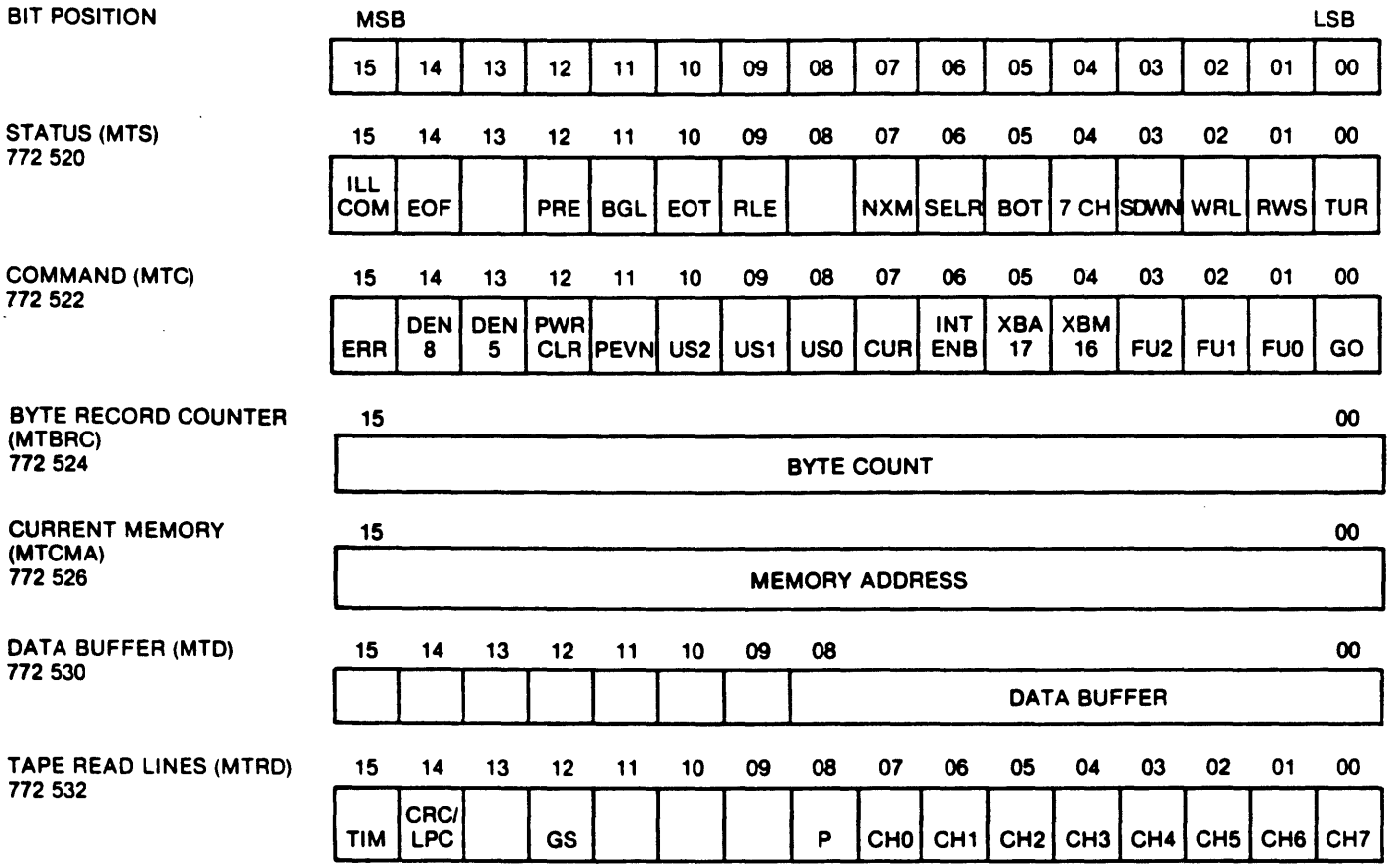
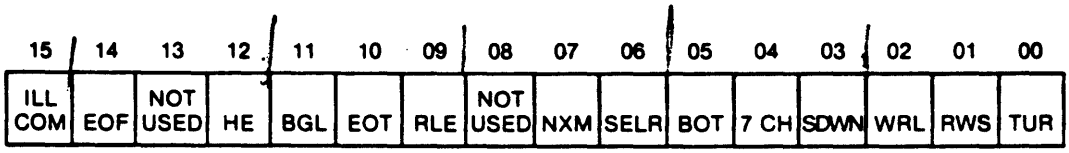



**Figure 4-1. Register Summary**

## STATUS REGISTER (MTS) 772 520




The address of the MTS register is 772 520. MTS is a read-only register. The functions of the bits of this register are as follows:

| BIT(S) | DESCRIPTION |
|---|---|
| 00 | TAPE UNIT READY (TUR): This bit is set when the tape unit is ready and is not rewinding. This bit is cleared when the processor sets the GO bit and the operation defined by the function bit occurs. |
| 01 | REWIND STATUS (RWS): This bit is set by the coupler as soon as it receives a Rewind command from the processor. It is cleared by the coupler as soon as the tape arrives at the BOT marker in the forward direction. (It overshoots BOT in the reverse direction.) |
| 02 | WRITE LOCK (WRL): This bit is set to prevent the control unit from writing information on tape. It is controlled by the presence or absence of the write protect ring on the tape reel. |
| 03 | TAPE SETTLE DOWN (SDWN): This bit is set whenever the tape unit is slowing down. The coupler will accept and execute any new command during the SDWN period except when the new command is to the same tape unit as the one issuing SDWN, and if the direction implied in the new command is opposite to the present direction. |

04 SEVEN CHANNEL (7CH): This bit is set to indicate a 7-channel tape unit; cleared, it indicates a 9-channel unit.

05 BEGINNING OF TAPE (BOT): This bit is set when the BOT marker is read, and cleared when the BOT marker is not read. BOT at a 1 does not produce a 1 in the ERR bit.

06 SELECT REMOTE (SELR): This bit is cleared when the tape unit addressed does not exist, is off-line, or has its power turned off.

07 NON-EXISTENT MEMORY (NXM): This bit is set during DMA operations when the control unit is bus master, and is performing data transfers into and out of the bus, when the control unit does not receive a slave Sync signal within 10 microseconds after it has issued a master Sync signal. The operations which occur when the error is detected are identical to those indicated for the BGL error.

08 BAD TAPE ERROR (BTE): NOT USED.

09 RECORD LENGTH ERROR (RLE): This bit is detected only during a Read operation. It occurs for long records only, and is indicated as soon as MTBRC increments beyond 0, at which time both data transfer into memory and incrementing of the MTCMA and MTBRC stop.

However, the control unit reads the entire record and sets the ERR bit when the LPC character is read. CU Ready remains at 0 until the LPC character is read.

10 END OF TAPE (EOT): This bit is set when the EOT marker is read while the tape is moving in the forward direction. The bit is cleared as soon as the same point is read while the tape is moving in the reverse direction. The ERR bit, as a result of the EOT bit at a 1, sets only in the tape forward direction and coincidentally with the reading of an LPC character.

11 BUS GRANT LATE (BGL): This bit is set when the control unit, after issuing a request for the bus, does not receive a bus grant before the coupler receives the bus request for the following tape character. The condition is tested only for NPR (Non-Processor Request) operations. The ERR bit sets simultaneously with BGL, thus terminating the operation. If the BGL occurred during a Write or Write With Extended IRG operation, the control unit does not send the signal WDS to the master, while the master writes the CRC character (if required) and LPC character onto the tape, terminating the record.

12 HARD ERROR (HE): This bit is set as the result of an error being detected on tape.

For all errors, the ERR bit sets at the end of the record. Both lateral and longitudinal parity errors are detected during Read, Write, Write EOF and Write With Extended IRG operations. The entire record is checked, including the CRC and LPC characters. During a Write operation a correctable error in the PE (1600 bpi) mode will set this bit.

13 NOT USED.

14 END OF FILE (EOF): This bit is set when an EOF character is detected during a Read, Space Forward, or Space Reverse operation. During the Read or Space Forward operation, the EOF bit is set when the LPC (Longitudinal Parity Check) character following the EOF character is read. During a Space Reverse operation, the EOF bit is set when the EOF character following its LPC character is read. The ERR bit sets when the LPC character strobe is generated with the File Mark signal upon EOF detection.

15 ILLEGAL COMMAND (ILL COM): This bit is set by any of the following illegal commands:

1. Any DATO or DATB to the command register during the tape operation period.
2. A Write, Write EOF, or Write With Extended IRG operation when the File Protect bit is a 1.
3. A command to a tape unit whose Select Remote bit is 0.
4. The Select Remote (SELR) bit becomes a 0 during an operation.

In error conditions 1 through 3, the command is loaded into the MTC, but the GO pulse to the tape unit is not generated. In addition, the CU Ready bit remains set.

**COMMAND (MTC)**
**772 522**

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ERR | DEN 8 | DEN 5 | PWR CLR | PEVN | US2 | US1 | US0 | CUR | INT ENB | XBA 17 | XBM 16 | FU2 | FU1 | FU0 | GO |

The address of MTC is 772 522. The functions of the bits of this register are as follows:

| BIT(S) | FUNCTION |
|---|---|
| 00 | GO: When set, this bit begins the operation defined by the function bits. |
| 01-03 | FUNCTION BITS: Selects 1 of 8 functions (programmable commands). |

| BIT 3 | BIT 2 | BIT 1 | |
|---|---|---|---|
| 0 | 0 | 0 | Off-Line/Rewind |
| 0 | 0 | 1 | Read |
| 0 | 1 | 0 | Write |
| 0 | 1 | 1 | Write EOF |
| 1 | 0 | 0 | Space Forward |
| 1 | 0 | 1 | Space Reverse |
| 1 | 1 | 0 | Write With Extended Interrecord Gap |
| 1 | 1 | 1 | Rewind |

| | |
|---|---|
| 04-05 | ADDRESS BITS: These are extended memory bits for an 18-bit bus address. Bit 5 corresponds to XBA17, and bit 4 to XBA16. They are an extension of the MTCMA, and increment during a tape operation if there is a carry-out of MTCMA. |
| 06 | INTERRUPT ENABLE (INT ENB): When this bit is set, an interrupt occurs whenever either the CU Ready bit or the ERR bit changes from 0 to 1, or whenever a tape unit that was set into rewind has arrived at the beginning of the tape. In addition, an interrupt occurs on an instruction that changes the INT ENB from 0 to 1 and does not set the GO bit, i.e., CU READY or ERROR = 1. |
| 07 | CU READY (CUR): This bit is cleared at the start of a tape operation, and set at the end of a tape operation. The control unit accepts as legal, all commands it receives while the CU Ready bit is a 1. |
| 08-09 | UNIT SELECT 1: These bits specify one of the four possible magnetic tape units. All operations defined in the MTC and all status conditions defined in the MTS pertain to the unit indicated by these bits. They are cleared by INIT. |
| 10 | UNIT SELECT 2: This bit specifies one of two possible formatters. When the STREAM switch is OFF (see Section 2), and the bit is 0, the formatter addressed is unit 0; if the bit is 1, the formatter addressed is unit 1. When the STREAM switch is ON and the bit is 0, the mode is START/STOP; if the bit is 1, the mode is STREAMING. If the switch is ON, the formatter addressed is always unit 0. |
| 11 | LATERAL PARITY (PEVN): NOT USED. This bit is not applicable for 9-track tape. |
| 12 | POWER CLEAR (PWRCLR): This bit provides the means for the processor to clear the control unit and tape units without clearing any other device in the system. The PWR CLR bit is always read back by the processor as a 0. |
| 13-14 | DENSITY (DEN 8, DEN 5): NOT USED. These bits are not applicable for 9-track tape. |
| 15 | ERROR (ERR): This bit is set as a function of bits 7-15 of the Status Register MTS. It is cleared by INIT or the GO command to the tape unit. |

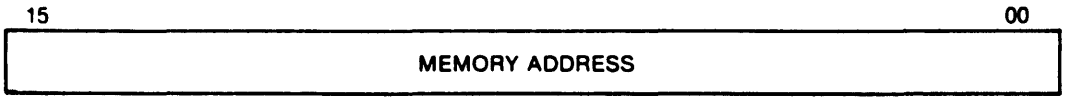
## BYTE RECORD COUNTER (MTBRC)
772 524


The MTBRC is a 15-bit binary counter which is used to count bytes in a Read, Write, or Write With Extended IRG operation, or records in a Space Forward or Space Reverse operation. When used in a Write or Write With Extended IRG operation, the MTBRC is initially set by the program to the 2's complement of the number of bytes to be written on tape. The MTBRC becomes 0 after the last byte of the record has been read from memory. Thus, when the next WDS (Write Data Strobe) signal occurs from the master, the control unit will not send the WDR (Write Data Request) signal to the master, indicating that there are no more data characters in the record.

When the MTBRC is used in a Read operation, it is set to a number equal to or greater than the 2's complement of the number of bytes to be loaded into memory. A Record Length Error (RLE) occurs for long records only, and is indicated when a read pulse for data (RDS occurring when CRC's or LPC's do not occur) occurs when the MTBRC is 0. The MTBRC increments by 1 immediately after each memory access.

When the MTBRC is used in a Space Forward or Space Reverse operation, it is set to the 2's complement of the number of records to be spaced. It is incremented by 1 at LPC time, whether the tape is moving in the forward or reverse direction. A new GO pulse is sent to the tape unit during the SDWN time if the MTBRC is not 0 during that time. When the tape unit is moving in the reverse direction, the LPC character is detected before SDWN, and before the entire record has been traversed. Thus, both SDWN and the LPC character appear to be in different positions on the tape from the positions apparent when the tape unit is moving in a forward direction.

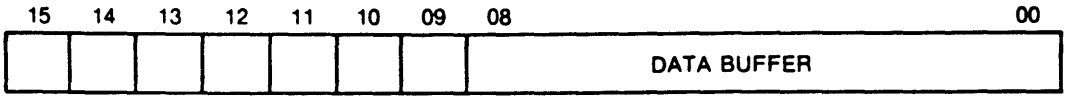
## CURRENT MEMORY ADDRESS (MTCMA)
772 526




The MTCMA contains 16 of the possible 18 memory address bits. It is used in DMA operations to provide the memory address for data transfers in Read, Write, and Write With Extended IRG operations. Before issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a Read operation, or from which the first byte is read in a Write, or Write With Extended IRG operation. The MTCMA is incremented by 2 immediately after each memory access. Thus, at any instant of time, the MTCMA points to the address that is next higher than the one which had been most recently accessed. When the entire record has been transferred, the MTCMA contains the address plus 2 of the last characters in the record. In the error conditions Bus Grant Late (BGL) and Non-Existent Memory (NXM), the MTCMA contains the address of the location in which the failure occurred.

The MTCMA is available to the processor on a DATI, except bit 0 which always reads as a zero under program control. Bit 0 can be asserted during DMA to determine the selected byte. The bits are set or cleared on a processor DATO. INIT clears all bits in the MTCMA.

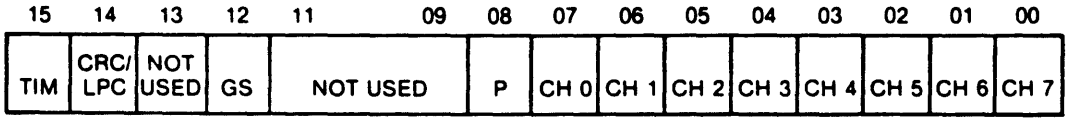
## DATA BUFFER (MTD)
## 772 530




The data buffer is an 8-bit register which is used during a Read, Write, or Write With Extended IRG operation. In a Read operation, the data buffer is a temporary storage register for characters that are read from tape before being stored in memory. In a processor read, all nine bits are stored in memory. Bits 0 through 7 in memory correspond to channels 7 through 0, respectively, from tape, and bit 8 corresponds to the parity bit. In a DMA operation only the data bits are read into memory, and are alternately stored in the low and high bytes. In a Write or Write With Extended IRG operation, the data buffer is a temporary storage register for characters that are read from core memory before they are written on tape.

In a Read operation, the LPC character enters the data buffer when bit 14 of MTRD is a 1, and is inhibited from doing so when bit 14 is a 0. Thus, after reading a nine-channel tape, the data buffer contains the LPC character when bit 14 is a 1, and the CRC character when bit 14 is a 0. After reading an EOF character, the data buffer contains all 0's when bit 14 is a 1, and the LPC character when bit 14 is a 0. The MTD is available to the processor on a DATI. Bits 9 through 15 are read identically to bits 1 through 7, respectively. Bits 0 through 7 are set or cleared on a processor DATA. Bits 8 through 15 are not affected by a processor DATO. INIT clears all bits in the MTD.

## TAPE READ LINES (MTRD)
## 772 532




The memory locations allocated for the tape read lines are:

| BIT(S) | DEFINITION |
|---|---|
| 00-07 | Channels 7-0 respectively. |
| 08 | Parity Bit. |
| 09-11 | NOT USED. |
| 12 | Gap Shutdown Bit. |
| 13 | NOT USED. |
| 14 | CRC, LPC Character Selector. |
| 15 | Timer. |

For correct longitudinal parity, bits 0-8 are 0 after writing a record or reading a record from tape. For a longitudinal parity error, one or more of the bits 0-8 remain 1's, indicating the channel(s) containing the error, which sets the CU Ready bit. Thus, if the pulse is set during a tape operation, CU Ready sets prematurely, producing the gap shutdown period while characters are still being read. Bits 0-8 are set and cleared by the tape unit. Bit 14 is set and cleared by the processor or cleared by INIT. Bit 15 is uniquely controlled by the 100-microsecond timer. The MTRD is available to the processor on a DATO, except that bit 13 reads back as a 0.

TIM (Timer) is a 10-kHz signal with a 50% duty cycle. The signal is used for diagnostic purposes in measuring the time duration of the tape operations. The timer is read as bit 15 in the MTRD.

# SECTION 5
# TROUBLESHOOTING AND THEORY

This section describes troubleshooting procedures at three levels of complexity: basic system, coupler symptoms and detailed analysis. Basic system troubleshooting procedures are visual checks not requiring test equipment and may be performed by the operator. Coupler symptom procedures may require a scope, meter, extender board or diagnostics and should be performed by a technician. Detailed analysis is troubleshooting at the IC level, and is presented for engineers or system analysts for coupler evaluation. The latter method may require the use of test equipment and the material presented here: board layout, term listing, theory of operation and logic diagrams.

**CAUTION**

*Any troubleshooting requires a familiarity with the installation and operation procedures in this manual, the appropriate DEC manual, and the tape drive manufacturer's manual. Ensure power is off when connecting or disconnecting the board or plugs.*

## BASIC SYSTEM TROUBLESHOOTING

The following should be checked before power is applied:

1. Verify that all signal and power cables are properly connected. Ribbon cable connectors are *not* keyed. The arrows on the connectors should be properly aligned.

2. Verify that all modules are properly seated in the computer and are properly oriented.

The following should be checked during or after application of power:

1. Verify that the computer and tape drive generate the proper responses when the system is powered up.

2. Verify that the computer panel switches are set correctly.

3. Verify that the console can be operated in the local mode. If not, the console may be defective.

4. Verify that the green diagnostic, the DMA, and activity lights on the coupler are active.

## COUPLER SYMPTOMS

Coupler symptoms, possible causes and checks/corrective action are described in Table 5-1. Voltage checks should be performed before troubleshooting more complex problems. Check the logics for voltage sources.

## PHYSICAL LAYOUT

The physical layout of the board is shown in Figure 5-1. Column and row numbers on the layout correspond to the numbers on each IC on the logic diagrams.

## TERM LISTING

The input and output terms for each logic diagram are described in Table 5-2. The sources and destinations refer to the sheet numbers on the logic diagrams.

## Table 5-1. Coupler Symptoms

| TROUBLE | POSSIBLE CAUSE | CHECK/REPLACE |
|---|---|---|
| 1. Green DIAGnostic light on coupler is OFF. | 1. Microprocessor section of coupler inoperative. | 1. Coupler. Put board on extender. With scope look at pins of 2901. All pins except power and ground should be switching. Look for "stuck high", or "stuck low", or half-amplitude pulses. If no switching, either power or crystal bad. |
| | a. Crystal not properly seated in socket. | |
| | b. Short or open on board. | |
| | c. Bad integrated circuit. | |
| | d. No DC power. | |
| 2. No communication between console and computer. | 2. I/O section of coupler "hanging up" Q Bus. | 2. Computer interface logic of coupler. |
| | a. $\overline{\text{DEN}}$ always low. | a. Check signal DEN for constant assertion. |
| | b. Shorted bus transceiver IC. | b. Check I/O IC's. Remove coupler board to see if trouble goes away. |
| | c. Bad CPU board. | c. Run CPU diagnostics. |
| 3. No data transfers to/from tape. BSY light never lights. | 3. Tape not ready or bad cable connection. | 3. Check tape switches and cable connector. |
| | a. Improper communication with tape registers on coupler or bad IC in register section of coupler. | a. Load and read tape registers from console with processor halted, i.e., RKDS, RKDA, RKER. Verify bits loaded can be read. |
| 4. Data transferred to/from tape incorrect. DMA and BSY lights blink to indicate transfers. | 4. Bad memory board in backplane. | 4. Run memory diagnostics. |
| | a. Noise or intermittent source of DC power in computer. | a. Check AC and DC power. |
| | b. Bad IC in tape I/O section of coupler. | b. While operating, check lines from coupler to tape with a 'scope for short or open. |
| | c. Run tape diagnostic, set console to make system "Halt On Error." | c. Analyze error halt. |
| | d. Bad area on tape. | d. Errors should always occur in same sector of tape. |
| | e. Head worn. | e. Replace head. |
| | f. Configuration switch not set properly. | f. Check configuration in Installation Section. |

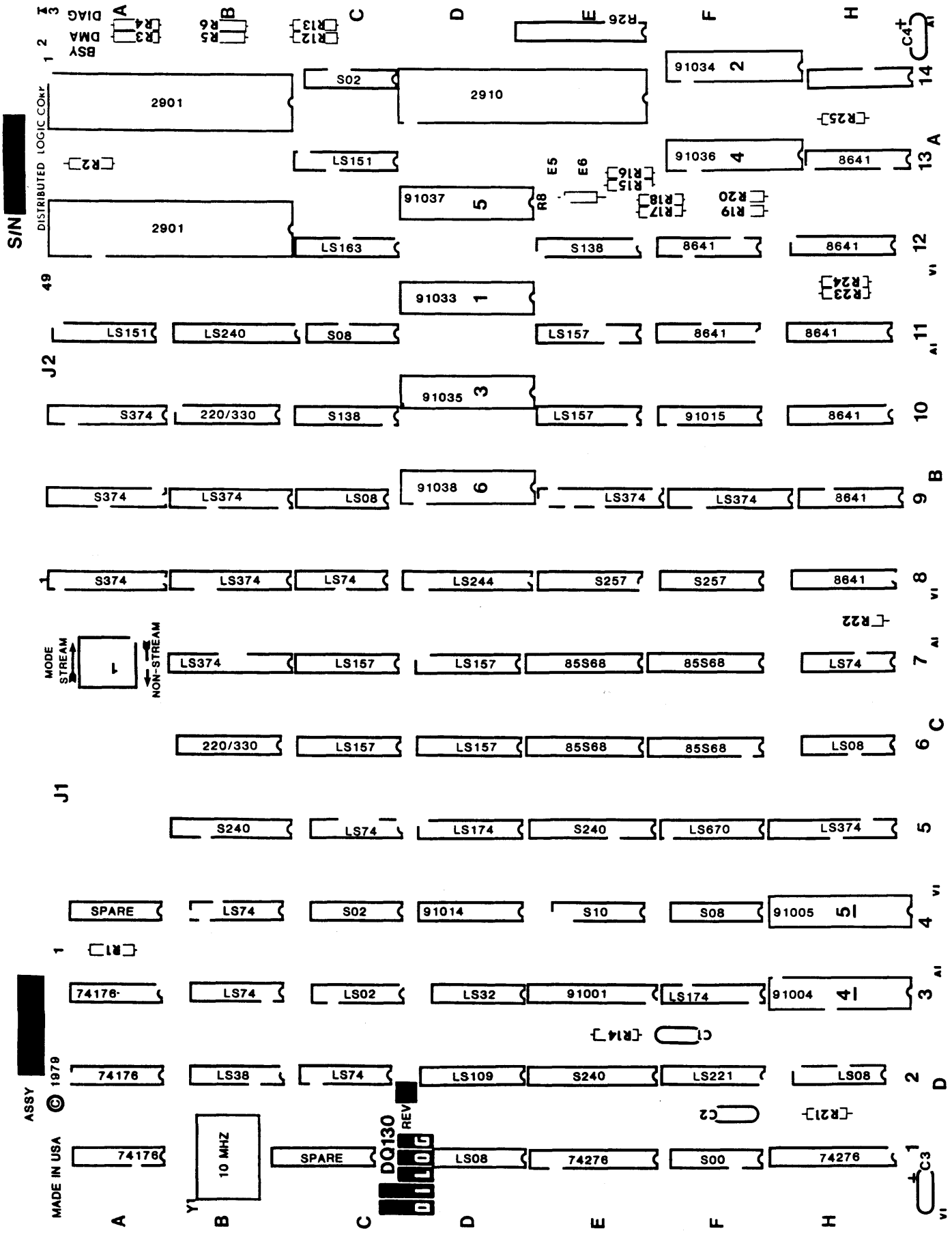



Figure 5-1. Board Layout

## Table 5-2. Term Listing

| Term | Source | Desgination | Description |
|---|---|---|---|
| A00 | 2 | 2 | Bus Address Bit 0, LSB |
| A01-A03 | 2 | 2, 7 | Bus Address Bits 1-3 |
| ACK | 2 | 2 | Acknowledge |
| ACKFF | 2 | 2 | Acknowledge Flip-Flop |
| ADRA | 3 | 7 | Address A |
| ADRB | 3 | 7 | Address B |
| A00FF | 2 | 2 | Address Bit 0 Flip-Flop |
| AS00-AS02 | 2 | 2 | A State Sequencer Bits 0-2 |
| BACTFF | 2 | 2, 7 | Bus Activity Flip-Flop |
| BBS7 | 5 | 2 | Bank Seven Select |
| BBS7L | 5, Bus (AP2) | | Bank Seven Select |
| BDIN | 5 | 2 | Data In |
| BDINL | 5, Bus (AH2) | | Data In From Master |
| BDMGIL | 5, Bus (AR2) | | DMA Grant In |
| BDMRL | 5, Bus (AN1) | | Bus DMA Request |
| BDOUT | 5 | 2 | Bus Data Output |
| BDOUTL | 5, Bus (AE2) | | Data Out From Master |
| BIAKIL | 5, Bus (AM2) | | Interrupt Acknowledge Input |
| BIAKOL | 5, Bus (AU2) | | Interrupt Acknowledge Output |
| BINIT | 5, Bus (AT2) | | Initialize |
| BIRQL | 5, Bus (AL2) | | Interrupt Request |
| BOT | 12 | J1 (4) | Beginning of Tape Mark |
| BRPFF | 2 | 2 | Bus Reply Flip-Flop |
| BRPLY | 5 | 2 | Bus Reply |
| BRPLYL | 5, Bus (AF2) | | Reply From Slave |
| BSACKL | 5, Bus (BN1) | | Select Knowledge |
| BSTCLK | 3 | 3, 7 | Clock |
| BSY | 3 | 3, 9 | Busy |
| BSYNCL | 5, Bus (AJ2) | | Synchronize |
| BUSD00L | 4, Bus (AU2) | | Bus Bit 0 |
| BUSD01L | 4, Bus (AV2) | | Bus Bit 1 |
| BUSD02L | 4, Bus (BE2) | | Bus Bit 2 |
| BUSD03L | 4, Bus (BF2) | | Bus Bit 3 |
| BUSD04L | 4, Bus (BH2) | | Bus Bit 4 |
| BUSD05L | 4, Bus (BJ2) | | Bus Bit 5 |
| BUSD06L | 4, Bus (BK2) | | Bus Bit 6 |
| BUSD07L | 4, Bus (BL2) | | Bus Bit 7 |
| BUSD08L | 4, Bus (BM2) | | Bus Bit 8 |
| BUSD09L | 4, Bus (BN2) | | Bus Bit 9 |
| BUSD10L | 4, Bus (BP2) | | Bus Bit 10 |
| BUSD11L | 4, Bus (BR2) | | Bus Bit 11 |
| BUSD12L | 4, Bus (BS2) | | Bus Bit 12 |
| BUSD13L | 4, Bus (BT2) | | Bus Bit 13 |
| BUSD14L | 4, Bus (BU2) | | Bus Bit 14 |
| BUSD15L | 4, Bus (BV2) | | Bus Bit 15 |
| BWTBT | 5 | 2 | Write Byte |
| BWTBTL | 5, Bus (AK2) | | Write Byte |
| C | 9 | 8 | 2901 Carry |
| CER – | 12 | J1 (42) | Corrected Error |
| CLR | 2 | 3 | Clear |
| CLRB | 3 | 3, 11 | Clear Bus |
| CN + 2 | 8 | 8 | Carry Output of 2901 |
| CR1-00 | 10 | 3, 8, 10 | Control Register One Output Bit 0 |
| CR1-01/ CR1-03 | 10 | 3, 8 | Control Register One Output Bits 1-3 |
| CR1-04 | 10 | 8 | Control Register One Output Bit 4 |
| CR1-05/ CR1-07 | 10 | 8, 10 | Control Register One Output Bits 5-7 |
| CR2-00 | 10 | 3, 8 | Control Register Two Output Bit 0 |
| CR2-01/ CR2-07 | 10 | 8 | Control Register Two Output Bits 1-7 |
| CR3-00/ CR3-01 | 10 | 3 | Control Register Three Output Bits 0-1 |
| CR3-02/ CR3-03 | 10 | 3, 7 | Control Register Three Output Bits 2-3 |
| CR3-04/ CR3-06 | 10 | 8 | Control Register Three Output Bits 4-6 |
| CR3-07 | 10 | 10 | Control Register Three Output Bit 7 |
| CR3-A01 | 3 | 7 | Control and Address Bit 1 |
| CR4-00/ CR4-07 | 10 | 9 | Control Register Four Output Bits 0-7 |

## Table 5-2. Term Listing (Continued)

| Term | Source | Desgination | Description |
|---|---|---|---|
| CR5-00/ CR5-07 | 10 | 9 | Control Register Five Output Bits 0-7 |
| CS | 8 | 9 | Carry Signal Out of Second 2901 |
| CSA-00/ CSA-08 | 9 | 10 | Control Store Address Bits 0-8 |
| D00/D07 | 7, 9, 10, 12 | 8 | 2901 Data Bus Bits 0-7 |
| DA | 2 | 4, 7 | Data Enable |
| DA16/DA17 | 3 | 5 | Data Address Bits 16, 17 |
| DB00 | 4 | 2, 3, 6 | Data Bus Bit 0 From A Bus |
| DB01/DB12 | 4 | 2, 6 | Data Bus Bits 1-12 From A Bus |
| DB08M | 6 | 6 | Data Bus Bit 8 From A Bus |
| DB13/DB15 | 4 | 6 | Data Bus Address Bits 13-15 From A Bus |
| DB15M | 6 | 6 | Data Bus Bit 15 From A Bus (MSB) |
| DB16L | 5, Bus (AC1) | | Data Bus Bit 16 (Address Extension) |
| DB17L | 5, Bus (AD1) | | Data Bus Bit 17 (Address Extension) |
| DBY | 12 | J1 (38) | Data Busy |
| DEN | 2 | 4, 5 | Device Enable |
| DEN – | 13 | J1 (50) | Device Enable |
| DIN | 2 | 2 | Data In |
| DINFF | 2 | 2 | Data In Flip-Flop |
| DMGI | 5 | 2 | Direct Memory Grant In |
| DOUT | 2 | 2 | Data Out |
| DOUTFF | 2 | 2 | Data Out Flip-Flop |
| DMG | 2 | 2 | Direct Memory Grant Delayed |
| DMGFF | 2 | 2 | Direct Memory Grant Flip-Flop |
| DRQFLG | 11 | 9 | Data Request Flag |
| DWDS | 12 | J1 (36) | Demand Write Data |
| DWDS | 12 | 11 | Demand Write Data |
| EDUF | 3 | 7 | Enable Data File |
| EOT | 12 | 12 | End of Tape Mark |
| ERAS | 13 | J2 (40) | Erase |
| FAD | 13 | J1 (48) | Formatter Address |
| FBY | 12 | J2 (2) | Formatter Busy |
| FEN | 13 | J1 (18) | Formatter Enable |
| FI00/FI15 | 6 | 7 | File In Bits 0-15 |
| FLCLK | 3 | 6 | File Lower Byte Clock |
| FL-D | 3 | 3 | File Lower Data |
| FLPT | 12 | J1 (32) | File Protect |
| FMK – | 12 | J1 (14) | File Mark |
| FO00-FO07 | 7 | 4, 7 | File Out Bits 0-7 |
| FO08-FO15 | 7 | 4, 6, 7 | File Out Bits 8-15 |
| FUCLK | 3 | 6 | File Upper Byte Clock |
| FU-D | 3 | 3, 7 | File Upper Data |
| FUNC | 3 | 3 | Function |
| GO | 13 | J2 (8) | Go |
| IAKI | 5 | 2 | Interrupt Acknowledge Input |
| IDENT | 12 | 9 | Formatter ID Burst |
| IDENT – | 12 | J1 (16) | Formatter ID Burst |
| INIT | 5 | 2 | Initialize |
| LD | 4 | 5 | Load Memory Address |
| LDADD | 2 | 3, 4 | Load Address |
| LWD | 13 | J2 (4) | Last Word |
| MMBGOL | 5, Bus (AS2) | | Bus Grant Output |
| MRQA | 3 | 2, 9 | Memory Request A |
| MRQB | 3 | 2, 3, 9 | Memory Request B |
| MRST | 2 | 3, 11 | Master Reset |
| MTC | 2 | 3, 6, 11 | Magnetic Tape Control |
| MTR | 2 | 2, 6 | Magnetic Tape Request |
| MTS | 2 | 2 | Magnetic Tape Status |
| NS | 8 | 9 | Sign of ALU MSB |
| NXM | 3 | 12 | Non Existent Memory |
| OFC | 13 | J1 (24) | Off-Line Status From Tape |
| ONL | 12 | J1 (44) | On-Line Status From Tape |
| PBSY | 3 | 6 | Peripheral Busy |
| PCLK | 3 | 3, 7 | Peripheral Clock |
| PIACLK | 3 | 11, 13 | Peripheral In A Byte Clock |
| PIB01 | 13 | 11 | Peripheral In B |
| PIB05 | 13 | 3 | Peripheral In B |
| PIBCLK | 3 | 13 | Peripheral In B Byte Clock |
| PICCLK | 3 | 13 | Peripheral In C Byte Clock |

**Table 5-2. Term Listing (Continued)**

| Term | Source | Desgination | Description |
|---|---|---|---|
| PIDCLK | 3 | 11 | Peripheral In D Byte Clock |
| POA-D | 2 | 12 | Peripheral Out A Byte Data |
| POB-D | 3 | 12 | Peripheral OUt B Byte Data |
| POC-D | 3 | 12 | Peripheral Out C Byte Data |
| PPCLK | 3 | 2, 3, 7, 11, 12 | Processor Clock |
| PPCLK | 3 | 8, 9, 10 | Processor Clock |
| RD0 | 12 | J1 (2) | Read Data Bit 0 From Tape |
| RD1 | 12 | J1 (3) | Read Data Bit 1 From Tape |
| RD2 | 12 | J2 (48) | Read Data Bit 2 From Tape |
| RD3 | 12 | J2 (50) | Read Data Bit 3 From Tape |
| RD4 | 12 | J1 (6) | Read Data Bit 4 From Tape |
| RD5 | 12 | J1 (20) | Read Data Bit 5 From Tape |
| RD6 | 12 | J1 (10) | Read Data Bit 6 From Tape |
| RD7 | 12 | J1 (8) | Read Data Bit 7 From Tape |
| RDP | 12 | | Read Data Parity From Tape |
| RDP – | 12 | J1 (1) | Read Data Parity From Tape |
| RDP – | 12 | 12 | Read Data Parity From Tape |
| RDQ | 11 | 9 | Request Data From Bus |
| RDS | 12 | J1 (34) | Read Data Strobe From Tape |
| RDS – | 12 | 11 | Read Data Strobe From Tape |
| REV | 13 | J2 (18) | Tape Reverse |
| RSTS | 11 | 3, 9 | Reset |
| RSTS – | 11 | 2, 3 | Reset |
| RSYNC | 2 | 2 | Synchronize |
| RSYNC | 5 | 2 | Synchronize |
| RWC | 13 | J2 (20) | Rewind Command To Tape |
| RWS | 12 | J1 (30) | Rewinding |
| STA | 3 | | Status |
| STORL | 2 | 3 | Store Lower Byte |
| STORU | 2 | 3, 11 | Store Upper Byte |
| TA | 3 | 3 | Tag Clock For Extended Address Bits |
| TAD0 | 13 | J2 (46) | Transport Address 0 |
| TAD1 | 13 | J1 (46) | Transport Address 1 |
| TD07* | 4 | 4, 6 | Transmit Bit 07 |
| TD07 | 6 | 4 | Transmit Bit 07 |
| TD12* | 4 | 4, 6 | Transmit Bit 12 |
| TD12 | 6 | 4 | Transmit Bit 12 |
| TD13* | 4 | 4, 6 | Transmit Bit 13 |
| TD13 | 6 | 4 | Transmit Bit 13 |
| TD14* | 4 | 4 | Transmit Bit 14 |
| TD15* | 4 | 4, 6 | Transmit Bit 15 |
| TD15 | 6 | 4 | Transmit Bit 15 |
| TDIN | 2 | 5 | Transmit D Bus In |
| TDMG | 2 | 5 | Transmit Direct Memory Grant |
| TDMR | 2 | 5 | Transmit Direct Memory Request |
| TD00G | 2 | 4 | Transmit D Bus Bit 0 Gated |
| TDOUT | 2 | 5 | Transmit D Bus Out |
| TEST | 9 | 9 | Test 2901 |
| TIAK | 2 | 5 | Transmit Interrupt Acknowledge |
| TIMER | 11 | 6 | Tape Time Operations |
| TIRQ | 2 | 2 | Transmit Interrupt Request |
| TO | 3 | 3 | Time Out |
| TOD | 3 | 2, 3 | Time Out Delay |
| TRDY | 12 | J1 (28) | Tape Ready From Tape |
| TRPLY | 2 | 5 | Transmit Reply |
| TSACK | 2 | 2, 3, 5 | Transmit Select Acknowledge |
| TSACK – | 2 | 2, 5 | Transmit Select Acknowledge |
| TSYNC | 2 | 3, 5 | Transmit Sync |
| TWTBT | 2 | 2 | Transmit Write Byte |
| WD0 | 13 | J2 (10) | Write Data Line 0 To Tape |
| WD1 | 13 | J2 (12) | Write Data Line 1 To Tape |
| WD2 | 13 | J2 (30) | Write Data Line 2 To Tape |
| WD3 | 13 | J2 (26) | Write Data Line 3 To Tape |
| WD4 | 13 | J2 (6) | Write Data Line 4 To Tape |
| WD5 | 13 | J2 (32) | Write Data Line 5 To Tape |
| WD6 | 13 | J2 (28) | Write Data Line 6 To Tape |
| WD7 | 13 | J2 (24) | Write Data Line 7 To Tape |
| WFM | 13 | J2 (42) | Write File Mark |

**Table 5-2. Term Listing**

| Term | Source | Desgination | Description |
|---|---|---|---|
| WRL | 3 | 7 | Write Load |
| WRT | 13 | 12 | Write/Read Formatter |
| WRT – | 13 | J2 (34) | Write/Read Formatter |
| WRU | 3 | 7 | Write Unload |
| WTBFF | 2 | 2 | Write Byte Flip-Flop |
| Y00/Y02 | 8 | 3, 6, 7, 9, 13 | Write Byte Flip-Flop Y Bus Bits 0-2 |
| Y03/Y05 | 8 | 3, 6, 9, 13 | Write Byte Flip-Flop Y Bus Bits 3-5 |
| Y06/Y07 | 8 | 6, 9, 13 | Write Byte Flip-Flop Y Bus Bits 6-7 |
| ZS | 8 | 9 | ALU Zero |

## THEORY

The coupler may be examined as three functions: computer interface, microprocessor and formatter interface. Signals from and to the computer are described in Section 1, Table 1-1. Signals from and to the formatter are described in Tables 1-2 and 1-3. Figure 5-2 is a simplified block diagram illustrating the interfaces and listing the major functional components. Single lines in the illustration represent serial data and the wide lines represent parallel data. A detailed block diagram of the coupler is shown on Sheet 1 of the logic diagrams. The numbers in the blocks on Sheet 1 refer to the sheet numbers of the other logic diagrams.

### Computer Interface

The purpose of the computer interface is to (1) buffer lines between the Q Bus of the computer and the coupler and (2) synchronize information transfers. There are two major classes of lines connected to the computer interface:

a. Data/address lines

b. Control lines

There are 16 bidirectional data/address lines and six extended address lines. Both device addresses and data are transferred over these lines. Address information is first placed on the lines by a bus master. The bus master then either receives input data from, or outputs data to, the addressed slave device, or memory, over the same lines. During initial control and status-transfer sequences, the coupler is a slave device. During data transfers, the coupler is a bus master and either receives data from, or outputs data to, the processor memory via the DMA facility.

The control lines request information transfers, select the type and direction of transfers, and synchronize the transfers. The control lines are functionally unidirectional and originate either at the processor or at the coupler.

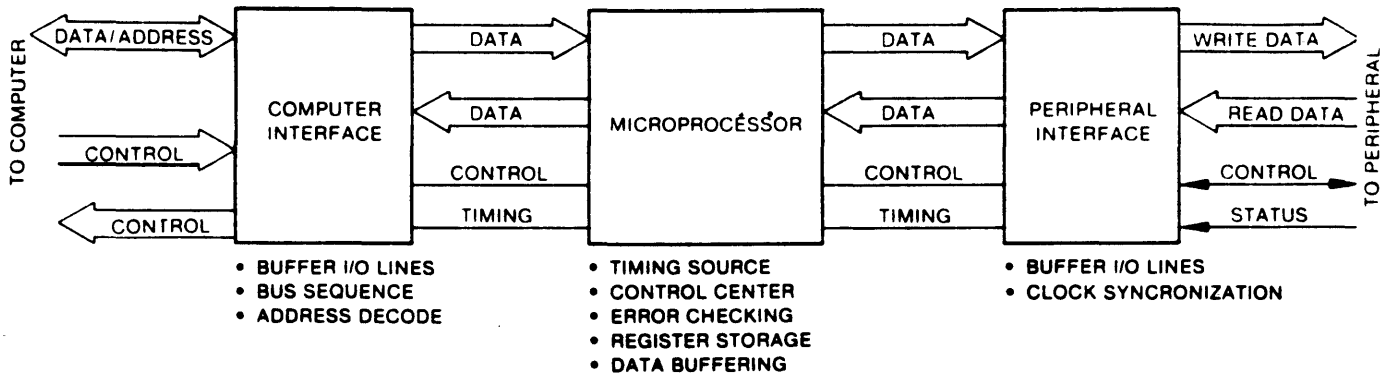



**Figure 5-2. Tape Coupler Simplified Block Diagram**

The computer interface controls the synchronization, or "bus arbitration" sequence. Bus synchronization is done by a separate hardware state processor, rather than by the microprocessor, to minimize bus use by the coupler. This permits many other devices to use the DMA channel efficiently on a time multiplexed basis with the tape coupler.

*Data/Address Receivers*—Both data and device addresses are time multiplexed on a 16 I/O bus line (BDAL00L-BDAL15L). The tri-state receiver/driver circuits H8, H9, H10, and H11, shown on Sheet 4, buffer these lines into the coupler. Once buffered, the received lines are identified as DB00-DB15 and routed to the bus arbitration sequence logic and the RAM data file multiplexer in the microprocessor.

*Control Receiver/Drivers*—The control lines between the I/O bus and the coupler are buffered by circuits F11, F12, H12, and H13, shown on Sheet 5. The receivers are always connected to the bus. Setting circuit pins 7 and 9 low enables the tri-state drivers to the bus. Two of the circuits are permanently enabled; circuit H12 is enabled by Transmit Select Acknowledge (TSACK), and circuit H13 is enabled by Device Enable ($\overline{\text{DEN}}$) and $\overline{\text{TSACK}}$.

*Data/Address Drivers*—The tri-state drivers in circuits H8, H9, H10, and H11 are enabled by Device Enable ($\overline{\text{DEN}}$) to gate addresses and data to the I/O bus. Addresses and data to the I/O bus are temporarily stored by register circuits E9 and F9. Information from the FQ Bus is clocked into the registers either by a Data (DA) signal or by a Load Address (LDADD) signal. The least significant bit (D00) is gated with control term TD00G to the line drivers.

*Bus and Arbitration Sequence (State Processor)*—To ensure the fastest response time, the synchronization of I/O bus transfers is done by hard-wired state logic, illustrated on Sheets 2 and 3. Information transfers are of two kinds; programmed I/O and Direct Memory Access (DMA). During DMA transfers, the coupler is bus master. Distinguishing between the two transfer types is the function of the arbitration logic.

The bus sequence logic synchronizes master/slave transfers over the I/O bus.

Transfers between the I/O bus and the coupler are of two types:

a. Register transfers via programmed I/O.

b. Data transfers via DMA.

During programmed I/O transfers, the seven coupler registers are accessed; initialization information is transferred to the registers; status information is accessed from the registers. The registers are located in the microdata file. Address information from the processor is decoded by circuits D4 and D5. Circuit D4 decodes the 772 52X portion of the address word. Circuit D5 buffers the four least significant bits, which become A00-A03.

The bus and sequence arbitration logic primarily comprises PROM's, used as decoders, and flip flops that temporarily store control information. For example, the storage elements for the DMA light, the Busy light, and the Diagnostic light are contained in this logic. Monostable multivibrators F2-5 and F2-13 monitor bus activity to ensure that responses to the bus master occur within 10 microseconds. Circuits Y1 and E1 establish the crystal-controlled time base for the coupler. The 10 mega-Hertz output of E1 is divided by two to generate 200 nanosecond clock PCLK, buffered to become PPCLK, $\overline{\text{PPCLK}}$, and $\overline{\text{CLK}}$*.

*Bus Transfer Timing*—The two major types of transfers are divided into the following I/O operations and an interrupt sequence:

- Data Input Transfer (DAT1) slave
- Data Output Transfer (DAT0) slave

- Data Input Transfer (DAT1) DMA
- Data Output Transfer (DAT0) DMA
- Interrupt Requests

Programmed I/O transfers are initiated with the coupler when the computer places the device address of the coupler on the BDAL04 through BDAL15 lines, sets the BBS7L signal at a low level, and switches signal BSYNCL low. Within the coupler, BSYNCL converts to RSYNC.

Address decoder D4 monitors the address lines. When the coupler address is decoded and RSYNC is asserted, the Bus Active bit (BACTFF) sets. This sets in motion the transfer sequence.

The sequence for a DATI operation is shown in Figure 5-3. For a DATI sequence, the state processor steps through states 1, 2,, and 7 (see Microprocessor in this section). The coupler responds to input requests by asserting TRPLY within 10 microseconds of a DATI request. DATI operations read status from the coupler.

The sequence for a DATO operation is shown in Figure 5-4. DATO operations transfer commands to the coupler registers. A DATO is similar to a DATI. The principle difference is that during a DATO, the

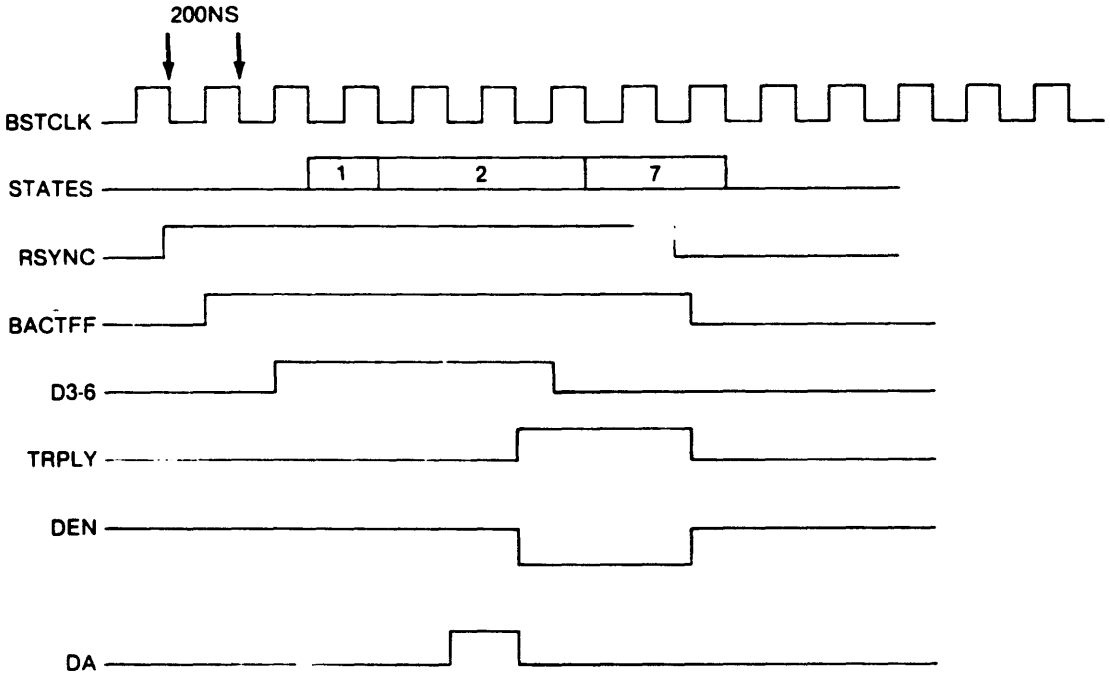



**Figure 5-3. DATI—Slave, Q Bus Transfers**

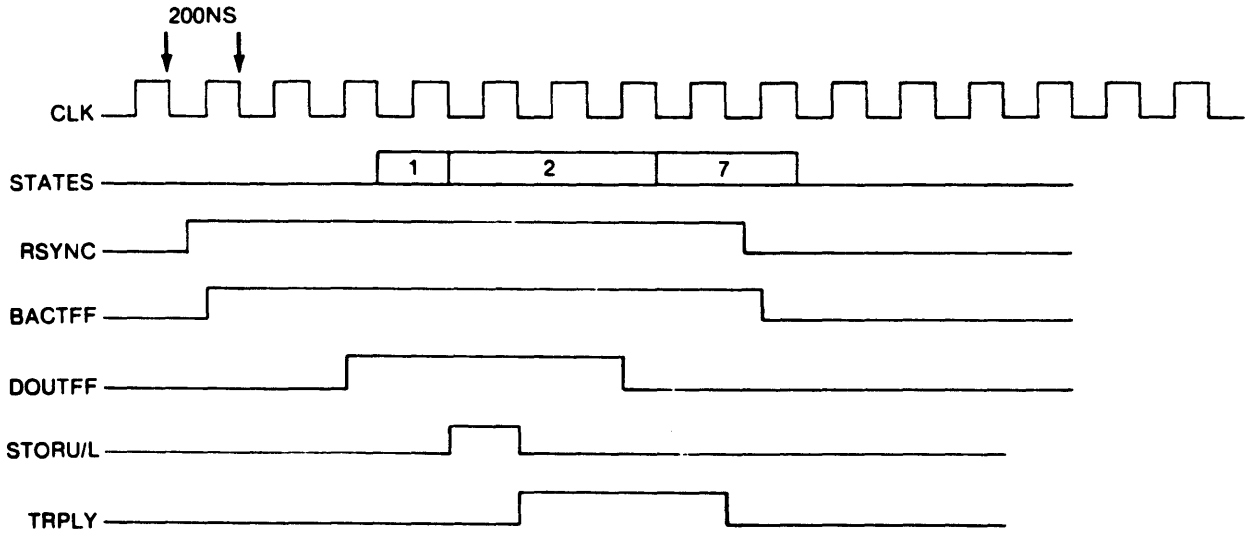



**Figure 5-4. DATO—Slave, Q Bus Transfers**

Data Out FF rather than the Data In FF is set, and the Data Available (DA) signal is not generated.

DMA transfers are between the coupler and computer memory. The coupler is always bus master. There are two transfer types: data in to memory (DATI) and data out of memory (DATO). Once the coupler has been granted DMA bus control, the transfer sequence is similar to I/O bus transfers.

Figure 5-5 illustrates the DMA DATI timing; Figure 5-6 illustrates the DMA DATO timing.

Interrupt request timing is illustrated by Figure 5-7. Interrupt requests are originated by Memory Request A (MRQA), a function of bit Y00 and the FUNC signal. The interrupt vector address is $224_8$.

**Microprocessor**

The microprocessor is the timing and control center of the coupler. The microprocessor is controlled by instructions stored in Programmable Read Only Memory (PROM). These instructions, called firmware, cause the microprocessor to operate in a prescribed manner during each of the computer-selected functions. The functions are established by a series of instructions issued by the computer. The instruction operands are stored in registers within the microprocessor.

When a Go command is issued by the computer, the firmware microinstructions cause the registers

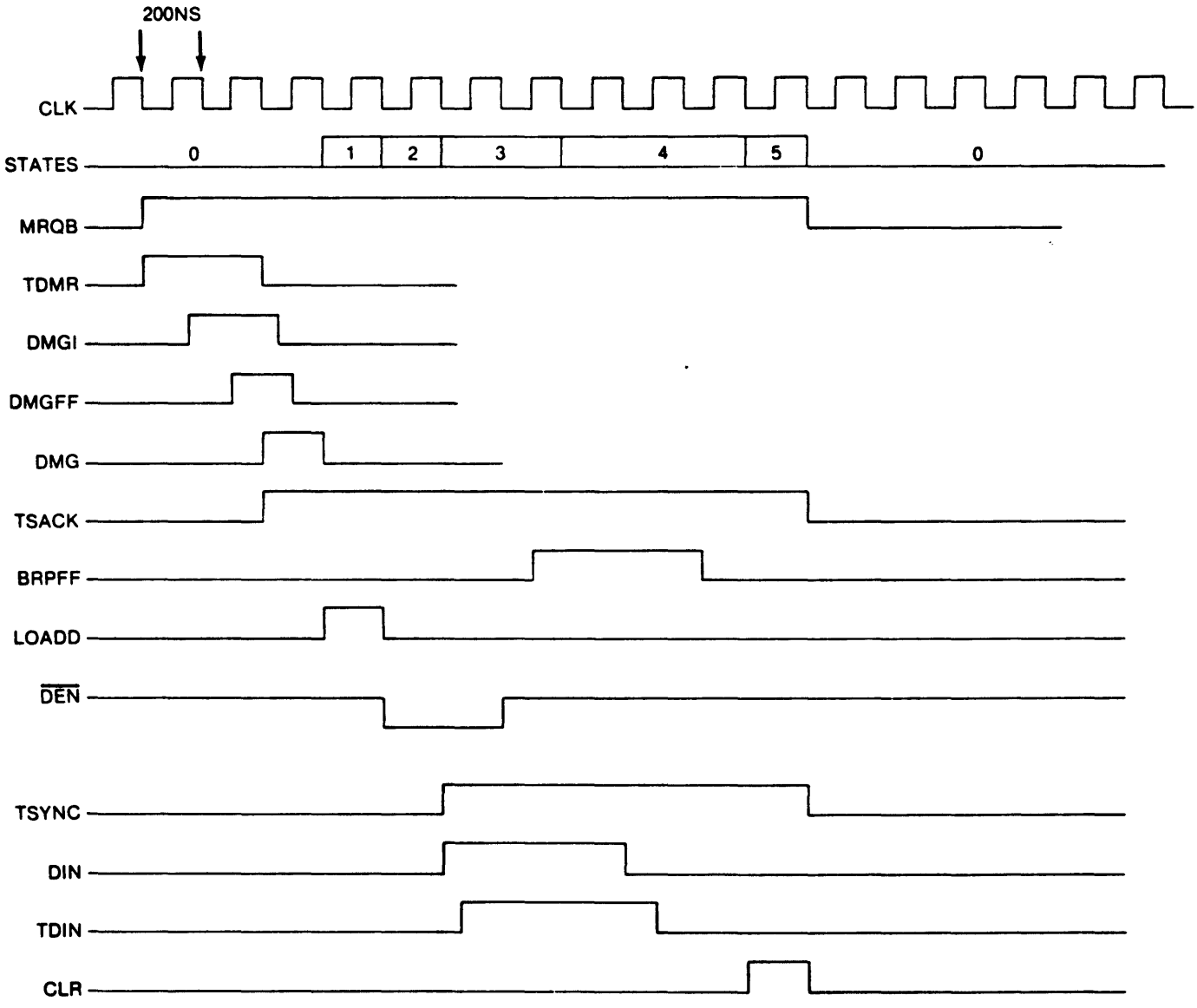



**Figure 5-5. DATI—Q Bus DMA Timing**

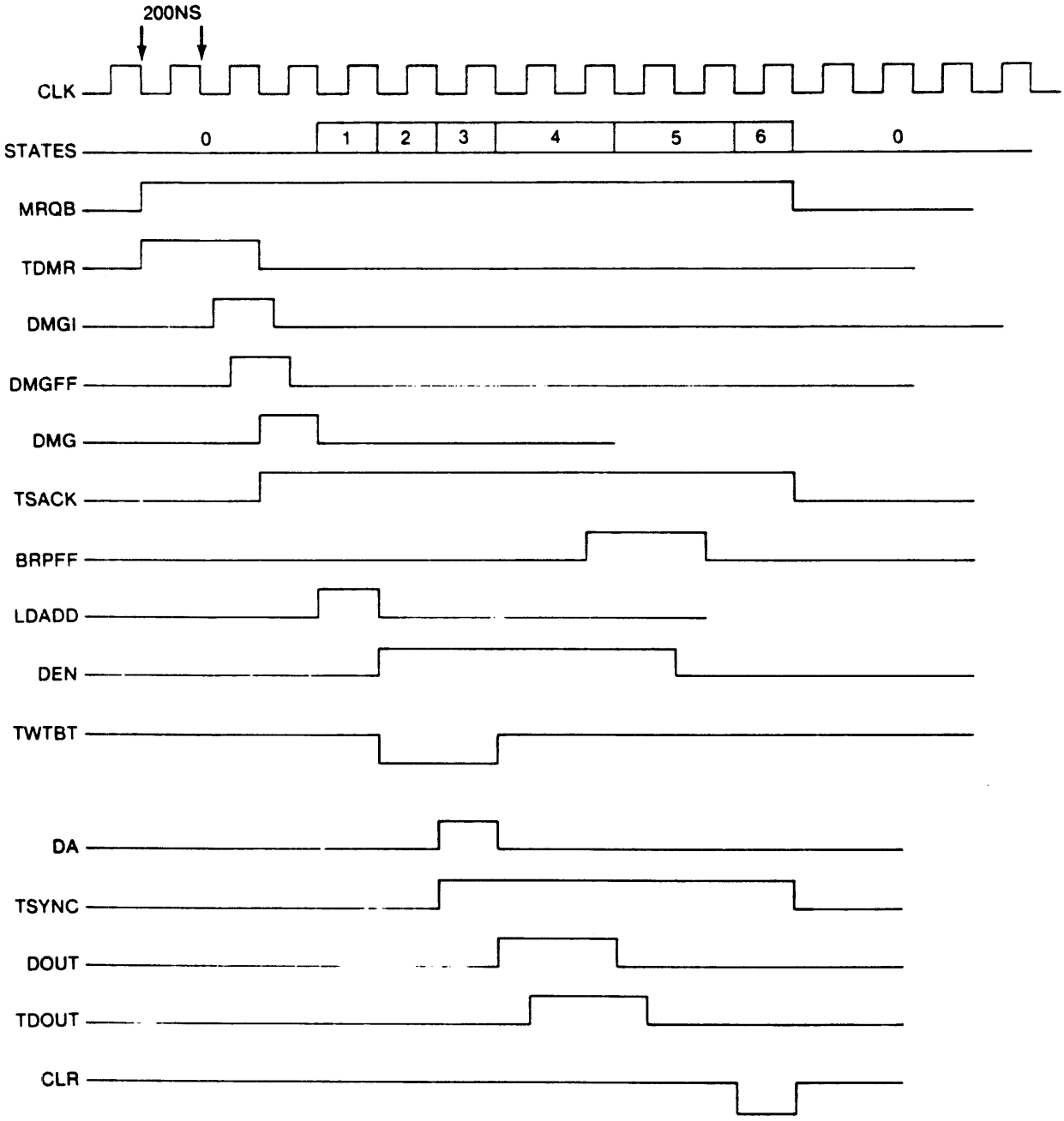



**Figure 5-6. DATO—Q Bus DMA Timing**

to be examined, and either a data transfer sequence or a rewind sequence to be performed.

The microprocessor contains an eight-word Random Access Memory (RAM) dedicated to buffering data between the Q Bus and the microprocessor. This allows several DMA cycle requests to be missed without missing data words being transferred between the tape and computer memory.

The rate and order (format) at which data is transferred to the tape is controlled by the microprocessor. Within the microprocessor, data is handled in 8-bit parallel bytes. Error check bits are calculated (LRCC, CRCC) and supplied to the tape during a write function. During a read function, the microprocessor monitors the error check bits and the data being read. Discrepancies are flagged as errors to the computer. The microprocessor detects other types of errors during the transfer functions (data late, programming error, etc.) and monitors status lines from the tape for malfunctions within this assembly. All errors are assembled into a status word for access by the processor.

The microprocessor comprises the following major elements:

a. Microdata File

b. Microdata File Address Register

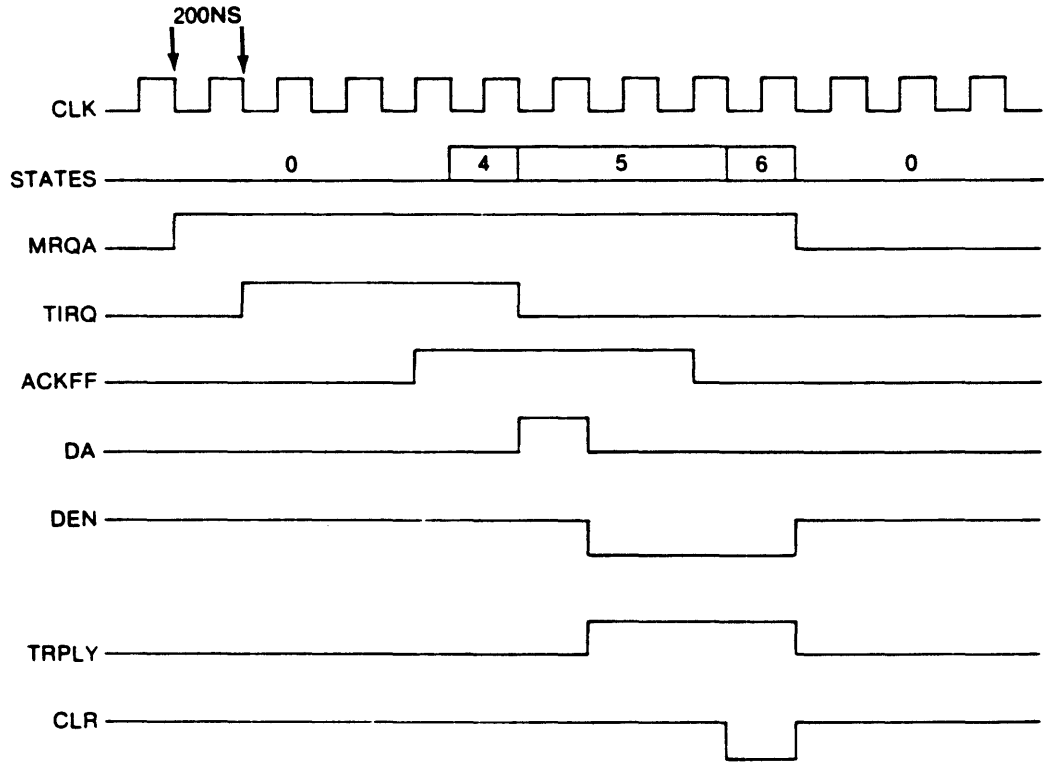



**Figure 5-7. Interrupt Sequence Timing**

c. Microdata File Multiplexer
d. 2901A Array and Status Register
e. Control Memory and Register
f. Control Store Address Programmer and Test Multiplexer
g. D Bus Multiplexer

The preceding elements are interconnected to perform the control, timing, error checking, and data manipulation functions of the coupler. Information is transferred among the elements over internal buses defined in Table 5-3.

To understand the function of a microprocessor, please refer to *The Microprogramming Handbook* from Advanced Micro Devices, Inc. Detailed technical descriptions of the 2901A four-bit bipolar microprocessor slice and of the 2901 microprogram coupler are given in the Advanced Micro Devices *AM2900 Family Data Book*. These two elements are the major components of the coupler.

*Microdata File*—This 16 word, 16-bit-per-word, data file has two functions:

a. Storage for the seven coupler registers in locations $10_{16}$ through $1A_{16}$ shown in Table 5-4.
b. Buffer storage for data words being transferred via DMA between memory and disc (locations 0 through 7).

**Table 5-3. Coupler Buses**

| The following prefixes are used as bus identifiers in the logic diagrams and the tables in Section 1. | |
|---|---|
| **Designation** | **Function** |
| B | LSI-11 I/O bus: Data, Address and Control lines, bidirectional. |
| DB | Data bus from I/O bus receivers into coupler. |
| D | Input Data bus to 2901A. |
| P | Peripheral Bus: Data and Control signals. |
| T | Transmit data or control signals from coupler to LSI-11 I/O bus. |
| Y | Output data bus from 2901A array. |
| FQ | Output of 16 x 16 Microdata file. |

**Table 5-4. Coupler Register Storage**

| Register | File Location (HEX) |
|---|---|
| MTS | 10 |
| MTC | 12 |
| MTBRC | 14 |
| MTCMA | 16 |
| MTD | 18 |
| MTRD | 1A |

Sheet 7 shows the data file. Inputs to the data file are from the data file multiplexer on lines FI00-FI15. Outputs from the data file are on lines FO00-FO15 to the microdata bus. Data file locations are accessed by the address file and by the DS2 portion of the control register word. Note that the data file is separated into 8-bit bytes and that the upper byte (FX08-FX15), the lower byte (FX00-FX07), or both bytes can be written into or read from.

*Microdata File Addressing*—The microdata file address logic is shown on Sheet 7. Two sources address the data file:

a. The bus and arbitration sequence logic (circuit E5).
b. The 4 x 4 address file (circuit F5).

Address control from the bus and arbitration sequence logic is address lines A01-A03, which select specific coupler registers.

The 4 x 4 address file can store up to four addresses. The source of address information to the address file is bit 03 of field three of the control register word (CR3-03), and bits 00, 01, and 03 of the Y Bus. Information can be read from and written into different locations of the address file simultaneously. When addresses are being buffered through circuit E5, circuit F5 is inhibited from supplying addresses. Write and read addresses to the address file are from field three of the control register word directly, and indirectly, via PROM E3 (Sheet 3).

*Microdata File Multiplexer*—The microdata file multiplexer, shown on Sheet 6, switches the input to the microdata file between two sources; the contents of the Y Bus, and the contents of the Data Bus (DB). The contents of field three of the control register word control the selection. Note that data bus bits 8 and 15 to the multiplexer can be selected by circuits E10 and E11 to be either DB8 and 15 or file output bits 8 and 15 restored in the file.

*2901A Array and Status Register*—The 2901A array is shown on Sheet 8. The status register is shown on Sheet 9 (circuit C12). The 2901A array comprises two AM2901A four-bit, bipolar microprocessor slice integrated circuits connected in cascade to perform data manipulation on 8-bit bytes. The major sections of the AM2901A are shown within dashed lines on the block diagram. A description of the operation of this device is given in the *AM2900 Family Data Book*.

The D Bus supplies external data to the 2901A. Data from the 2901A is on the Y Bus. Control inputs to the 2901A are shown in Table 5-5.

The status register is updated on a coupler clock with the ALU status. The register stores the conditions shown in Table 5-6.

**Table 5-5. Control Inputs To 2901A**

| Mnemonic | Signal Source | Definition |
|---|---|---|
| A0-3 | Control Register | Address inputs; selects the A file register contents to be connected to the 2901A, A Bus. (S1) |
| B0-3 | Control Register | Address inputs; selects the A file register contents to be connected to the 2901A, B Bus. (S2) |
| I0-8 | Control Register | Instruction control lines; lines 0-2 select the data sources to be applied to the ALU; lines 6-8 determine the routing of the output of the ALU within the ALU, and the source of data supplied to the Y (output) Bus. |
| CN | Control Register | Carry input of ALU. Used during arithmetic operations. |
| CP | Crystal Oscillator | 200 nanosecond clock to 2901A. |

**Table 5-6. Status Register Bits**

| Mnemonic | Definition |
|---|---|
| $C_S$ | Indicates a "carry out" of ALU |
| $N_S$ | The most significant ALU bit (sign of result). |
| $V_S$ | Overflow has occurred. |

*Control Memory and Register*—The control memory stores the firmware that controls the operation of the coupler. It comprises six 512 x 8 bit Programmable Read-Only Memories (PROMs) identified as D9, D10, D11, D12, F13, and F14, on Sheet 10. The PROMs have a pipeline register at the output identified as the Control Register (CR). The six PROMs produce a 48-bit instruction word divided into six 8-bit fields. Figure 5-8 depicts the instruction word.

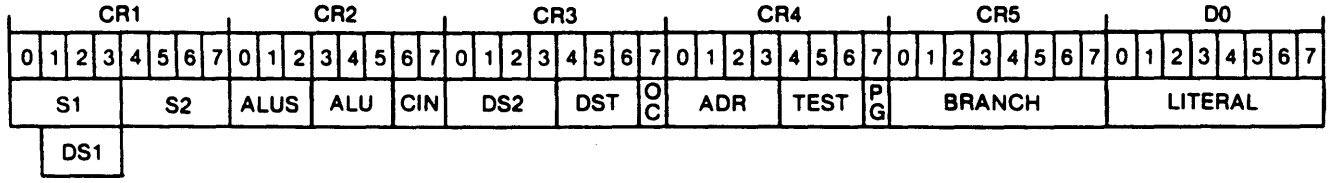



**Figure 5-8. Microinstruction Word**

The contents of the control memory are accessed by the Control Store Address Processor and strobed into the control register by the PPCLK clock. The contents of the control register (CR1-00-07 through CR5-00-07 and literal D00-D07) are routed throughout the logic of the coupler.

*Control Store Address Programmer*—The Control Store Address Programmer (CSAP) is an AM2910 microprogram control circuit and is described in the *AM2900 Family Data Book*. It controls the sequence of execution of microinstructions stored in the control memory. The CSAP is shown on Sheet 9 (circuit DE14).

Control Store output address lines CSA00 through CSA08 select one of 512 locations in control memory. Inputs to the CSAP are primarily from fields four and five of the Control register and the $\overline{\text{TEST}}$ output of Test Conditions Multiplexer C13 (shown on Sheet 9). Bits 00 through 07 (LSB) of field five (CR5) supply branch addresses to the CSAP. Bits 00 through 03 of field four (CR4) supply instruction codes to the CSAP. Any one of 16 instructions can be selected. The instructions can be modified by the state of the $\overline{\text{TEST}}$ input. The instructions select the next source of addresses to the control memory. The primary sources of addresses are as follows:

a. A program counter/register within the CSAP.

b. A five-word stack within the CSAP.

c. Branch addresses directly from bits 00-07 of field five (CR5).

Note that bits 04 through 06 of field four (CR4) control Test Condition Multiplexer C13. This multiplexer connects one of seven selected conditions to the $\overline{\text{TEST}}$ line when specified by the current microinstruction being executed. The conditions tested for are shown in Table 5-7.

**Table 5-7. Address Modification Conditions**

| Mnemonic | Condition |
|---|---|
| C | No carry from 2901A ALU. |
| Z | ALU result is zero. |
| C | Carry from ALU. |
| N | ALU sign bit is logical true. |
| V | ALU has overflowed. |
| INIT | Initiate |

Note that bus signal BDCOKH, if ever low, disables the output of the GSAP and generates a RESET (RST) signal.

*D Bus Multiplexer*—The D-bus multiplexer, shown on Sheets 7, 9, and 12, is the information source to the 2901A array processor. The multiplexer comprises circuits D8 (Sheet 9), E8 and F8 (Sheet 7), and B9 (Sheet 12). Circuits B7, B8, and B9 also function as storage registers. One additional information source for the D Bus is PROM D9, shown on Sheet 10, which supplies the Literal (LIT).

Field one CR1-00-03 and CR2-00 via circuit E12 (Sheet 3) gate the selected source to the D Bus. Information sources to the D Bus are shown in Table 5-8.

**Table 5-8. Information Sources to D Bus**

| Circuit | Sheet | Source |
|---|---|---|
| D9 | 10 | Literal from control memory |
| E8, F8 | 7 | RAM File data bus upper and lower bytes |
| D8 | 9 | Coupler status |
| B7 | 12 | Data from tape |
| B8, B9 | 12 | Tape status |

**Peripheral Interface**

The purpose of the peripheral interface is to match the characteristics of the tape formatter to the characteristics of the microprocessor. The peripheral interface:

a. Contains line drivers and receivers that buffer the information lines between the coupler and the tape drives over cable lengths up to 25 feet.

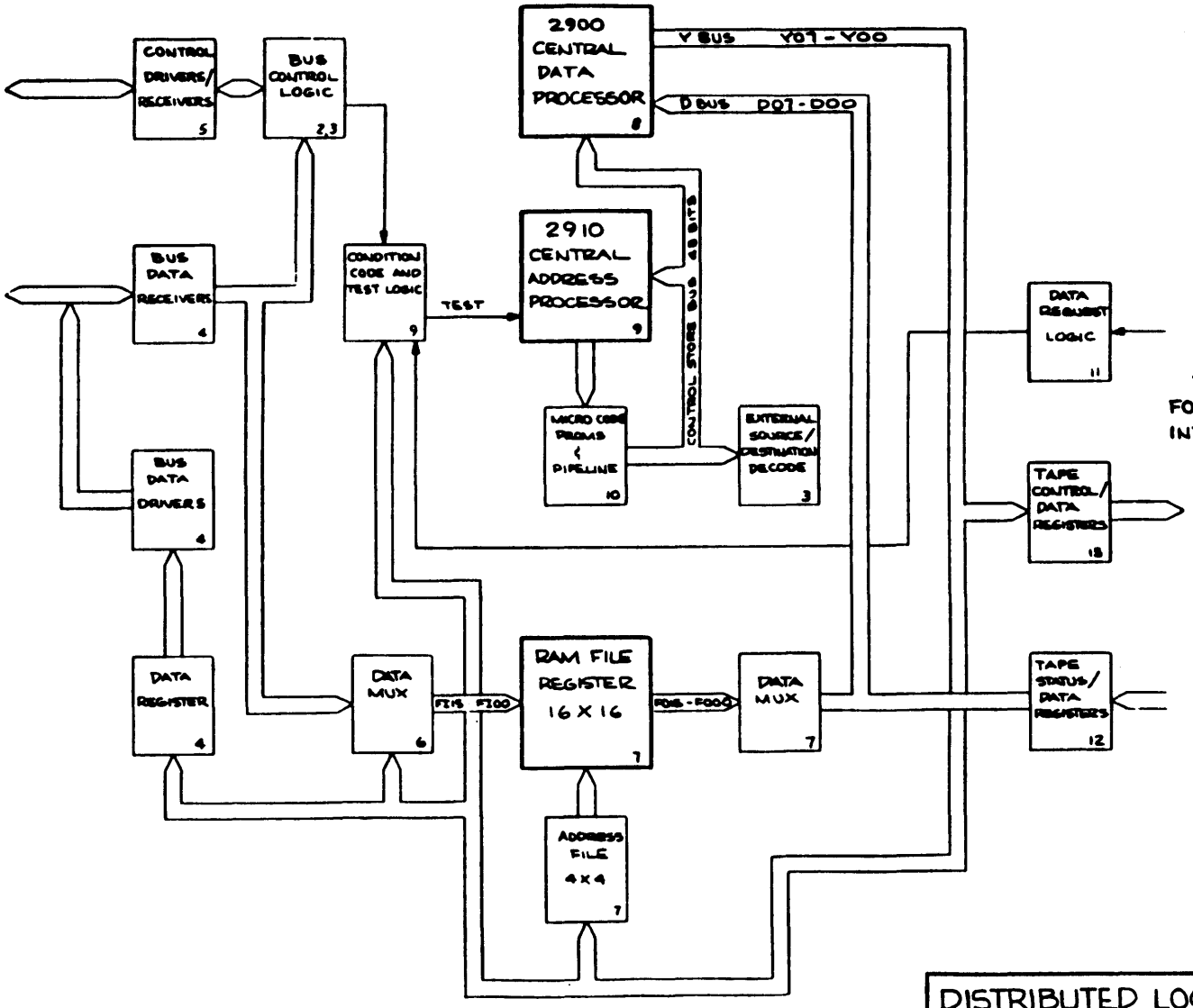
b. Contains the PROM and jumpers that permit configuring the coupler to match the different tape subsystem configurations.

There are two registers which temporarily store information being transferred between the tape and the other elements of the coupler; an input register and an output register. The input register is shown on Sheet 12, and the output register on Sheet 13.

The input register stores status information and data received from the tape and comprises circuits B7, B8, and B9. The outputs of these circuits are gated to the D Bus. The tape status information originates at the line receivers and is stored in circuit B9; the data from the tape is stored in circuit B7.

The output register stores information to be sent to the tape and comprises circuits A8, A9, and A10 on Sheet 13. These circuits make up a 32-bit register that receives information from the Y Bus in 8-bit segments. Y-bus information is stored in the register under control of the PIA, PIB, PIC, and PID clocks. The outputs of the register are routed to the tape formatter.

CPU
INTERFACE




DQ130 BLOCK DIAGRAM

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|---|---|---|
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| LOGIC DIAGRAM DQ130 | | SHT 1 OF 13 |
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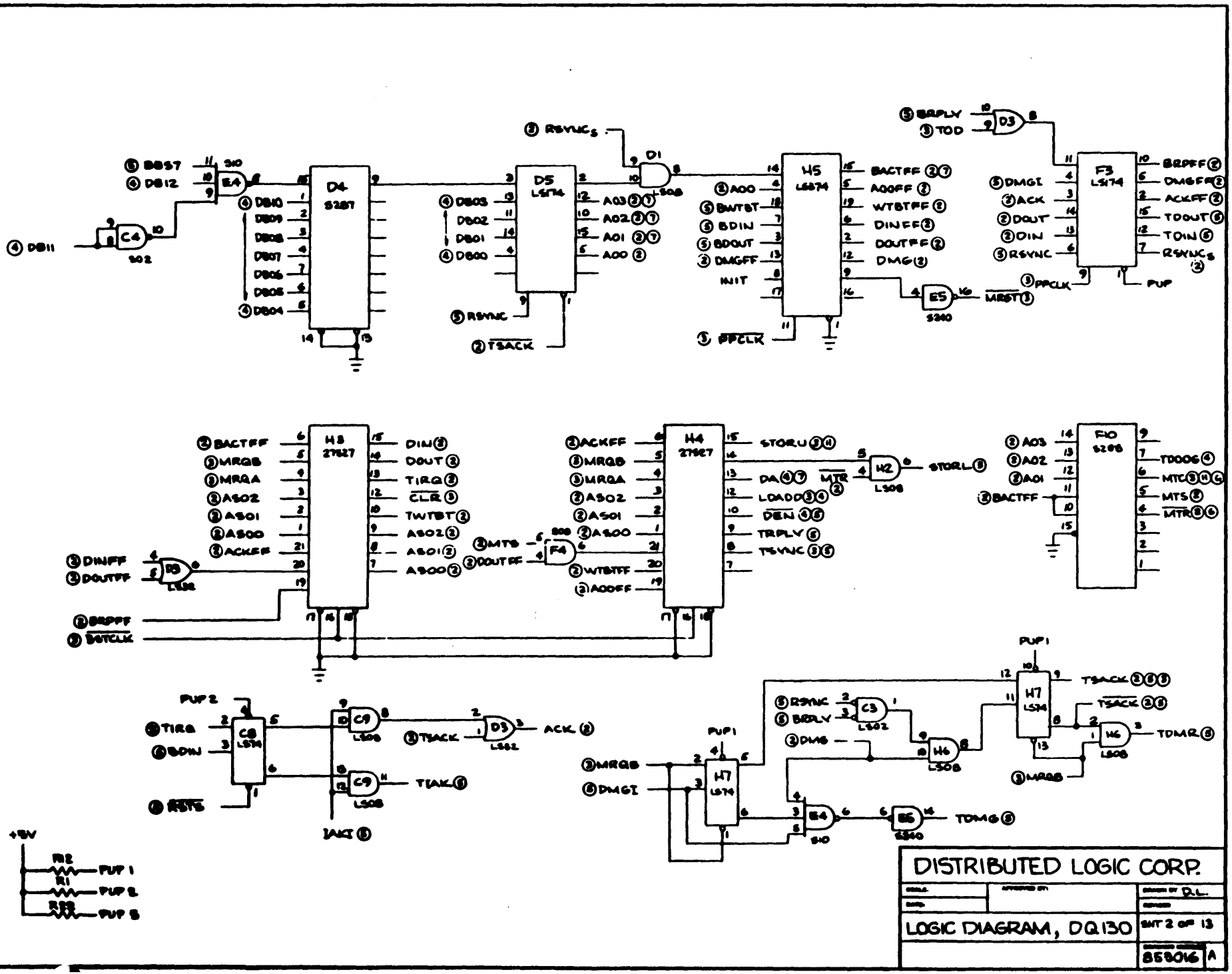
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R2
R1
R33
H1 LS74
H2 LS08
H3 LS74
H4 27S27
H5 LS374
H6 LS08
H7 LS74
H8 27S27
H9 LS32
H10 S298
D1 LS08
D3 LS02
D4 S287
D5 LS374
E3 S240
E4 S10
E5 S240
F3 LS174
F4 S08
C3 LS02
C4 S02
C8 LS74
C9 LS08
DB11
DB12
DB13
DB10
DB09
DB08
DB07
DB06
DB05
DB04
DB03
DB02
DB01
DB00
RSYNCS
TSACK
RSYNC
PPCLK
BRPLY
TOD
DMGI
ACK
DOUT
DIN
PUP
BACTFF
AOOFF
BWTBT
BDIN
BDOUT
DMGFF
INIT
WTBTFF
DINFF
DOUTFF
DMG
MRST
BRPFF
DMGFF
ACKFF
TDOUT
TDIN
RSYNCS
DIN
DOUT
TIRQ
CLR
TWTBT
AS02
AS01
AS00
ACKFF
MRQB
MRQA
AS02
AS01
AS00
MTS
WTBTFF
AOOFF
STORU
DA
LOADD
DEN
TRPLY
TSYNC
STORL
MTR
AO3
AO2
AO1
TDOOG
MTC
MTS
MTR
TIRQ
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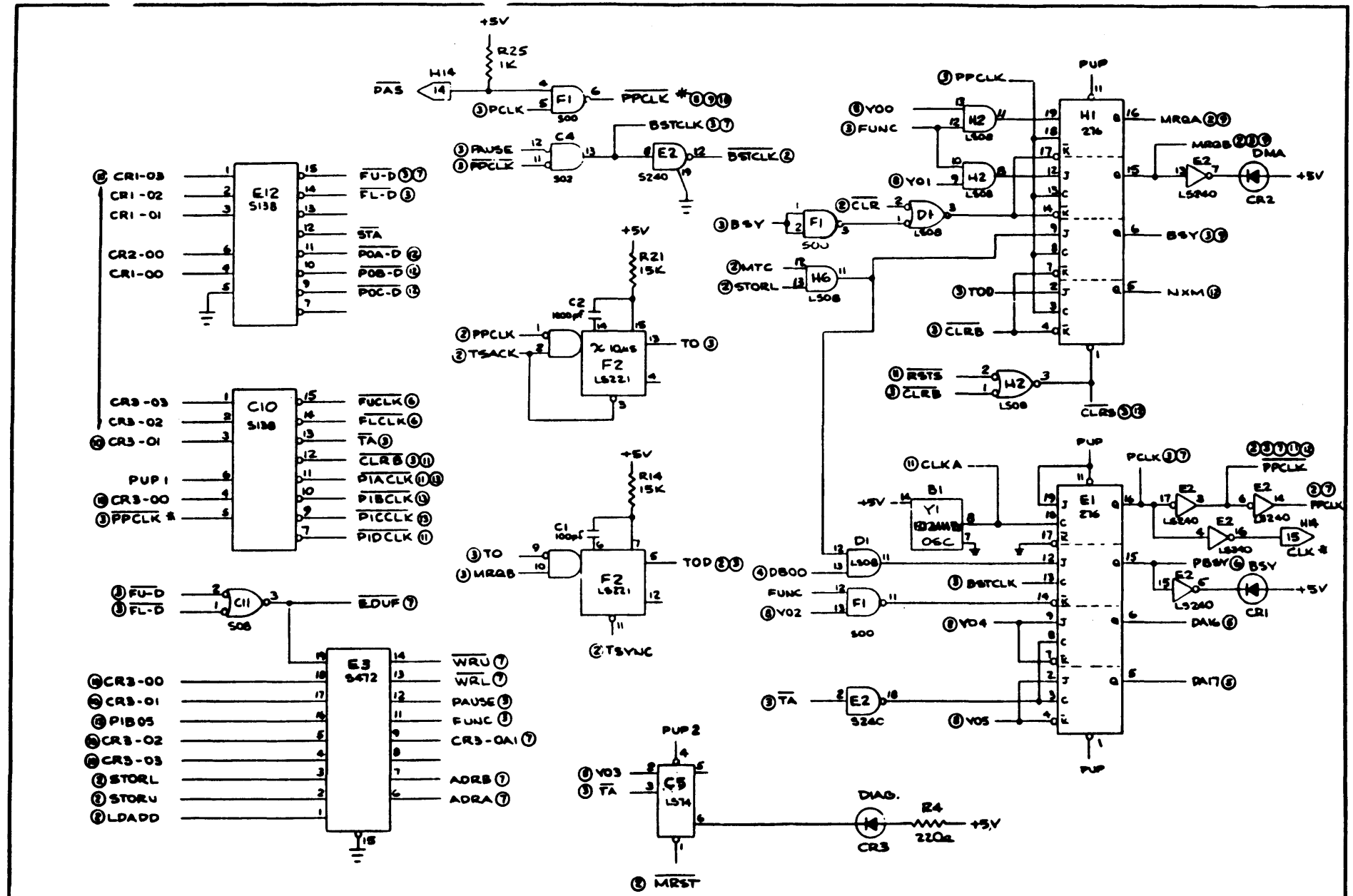
MRQB
TDMG
TDMR




NOTE: SYMBOL ▷ INDICATES 16 PIN DIP CONNECTOR LOCATED AT H14

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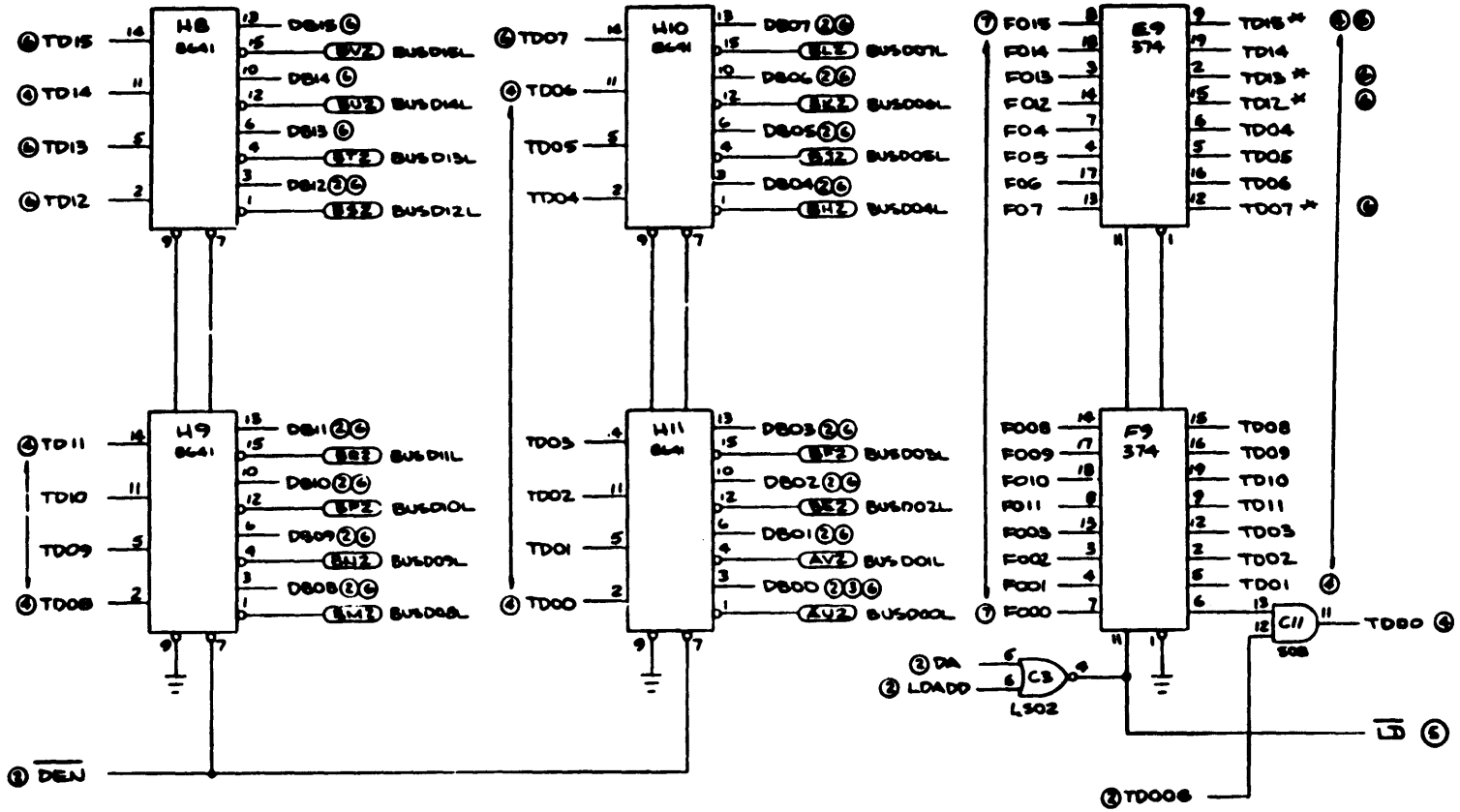
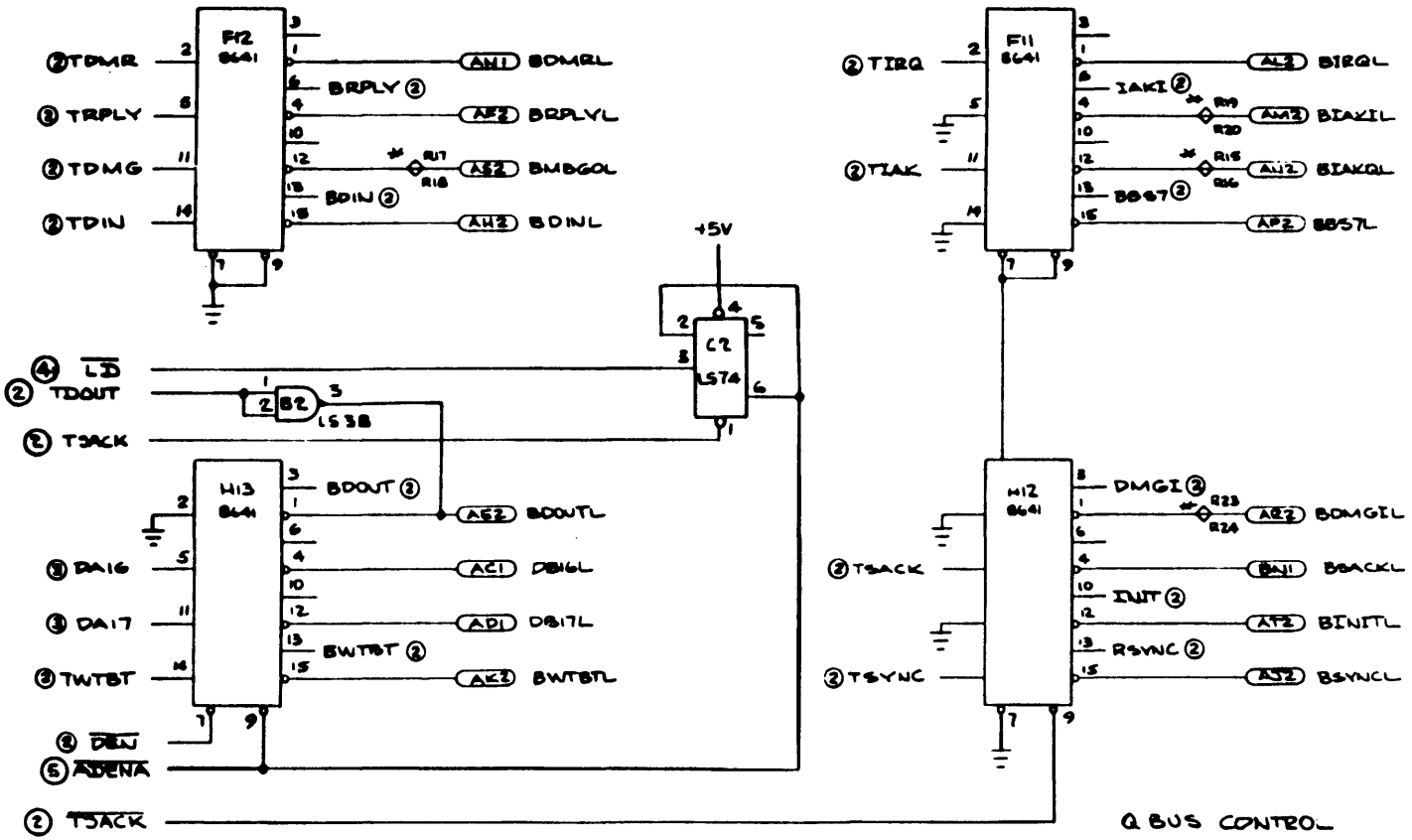
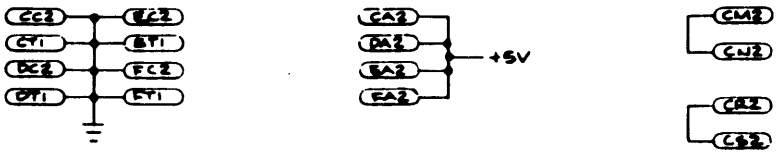
| LOGIC DIAGRAM, DQ130 | | SHT 3 OF 13 |
| | | 859016 A |

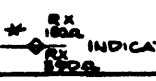



DATA BUS RCVR / DVR

| | | |
|---|---|---|
| DISTRIBUTED LOGIC CORP. | | |
| | | DRAWN BY DL |
| LOGIC DIAGRAM, DQ130 | | SHT 4 OF 13 |
| | | 859016 A |

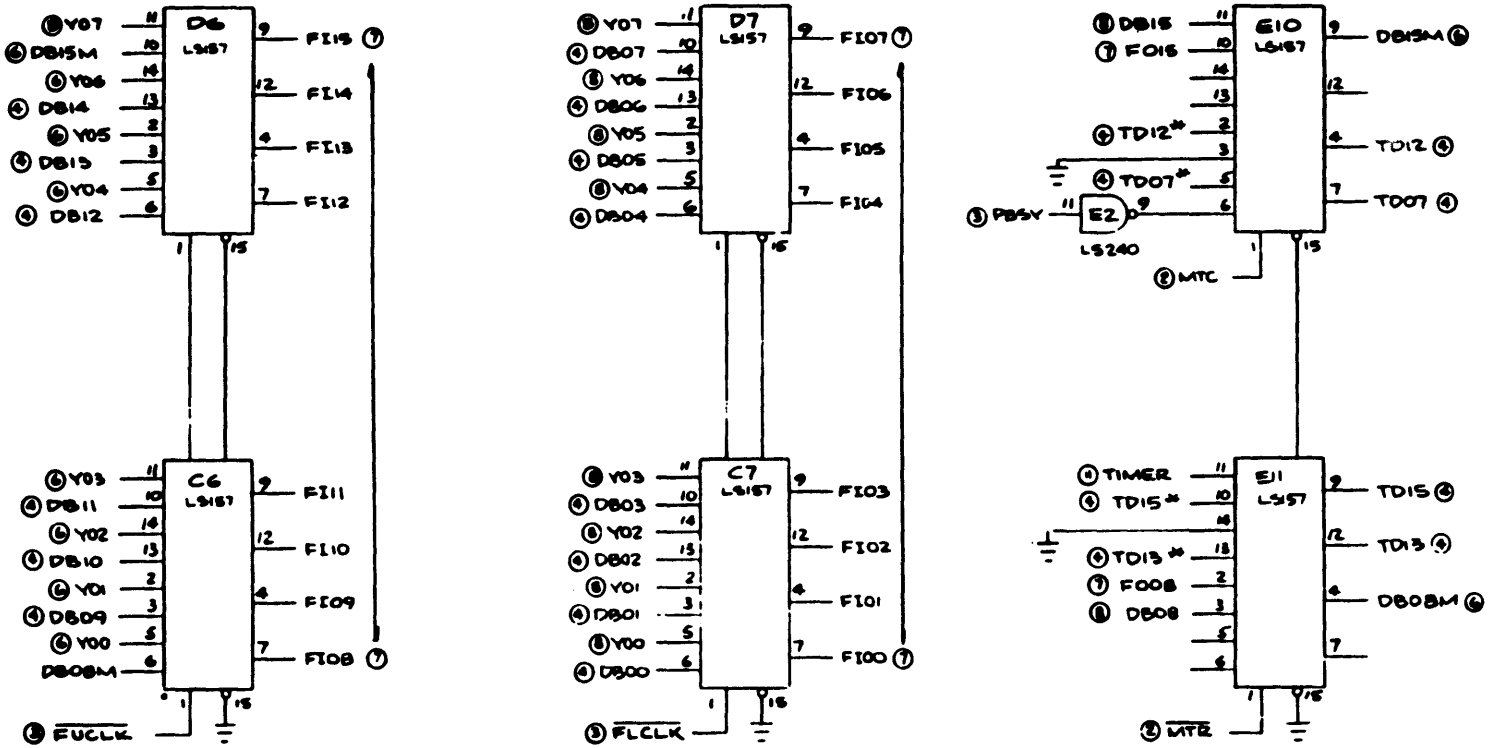



NOTE: SYMBOL  INDICATES "PULL-UP" (180Ω), "PULL DOWN" (390Ω) RESISTORS.

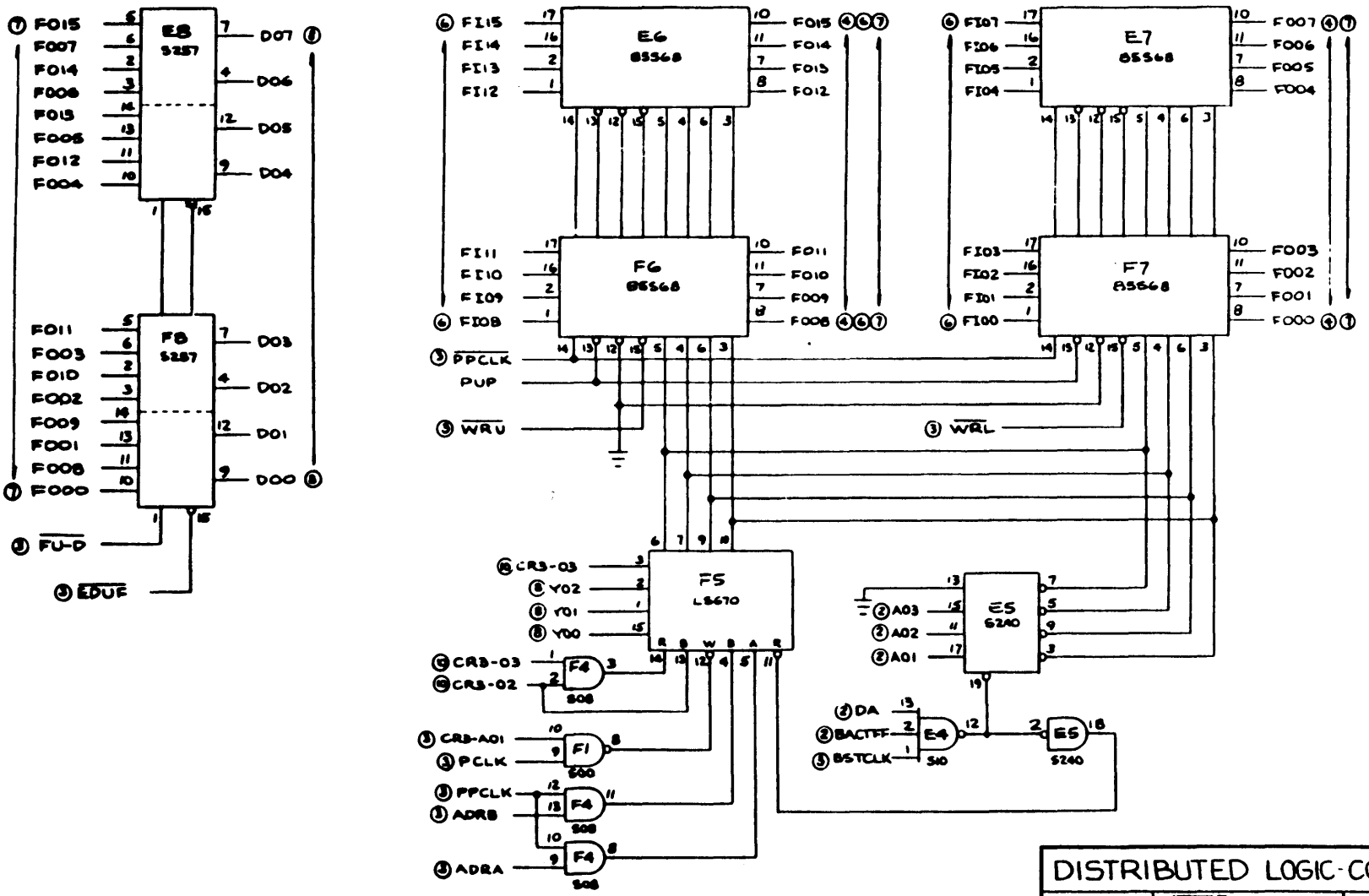
DISTRIBUTED LOGIC CORP.

| | | |
|---|---|---|
| SCALE | APPROVED BY: | DRAWN BY D.L. |
| DATE | | REVISED |
| LOGIC DIAGRAM, DQ130 | | SHT 5 OF 13 |
| | | 859016 A |



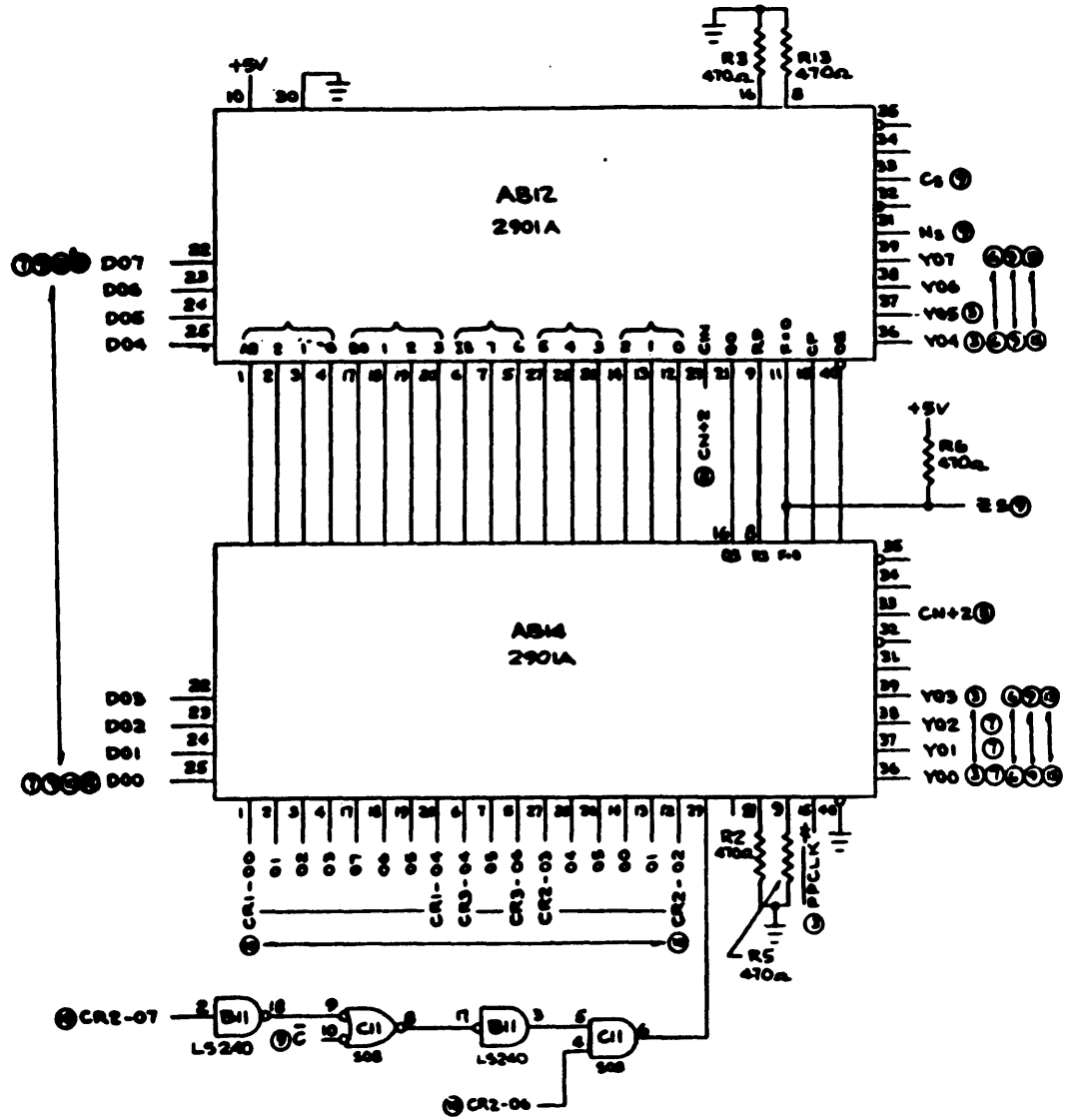

DATA FILE MUX

| DISTRIBUTED LOGIC CORP. | | |
|---|---|---|
| SCALE | APPROVED BY: | DRAWN BY D.L. |
| DATE | | REVISED |
| LOGIC DIAGRAM, DQ130 | | SHT 6 OF 13 |
| | | DRAWING NUMBER 853016 |



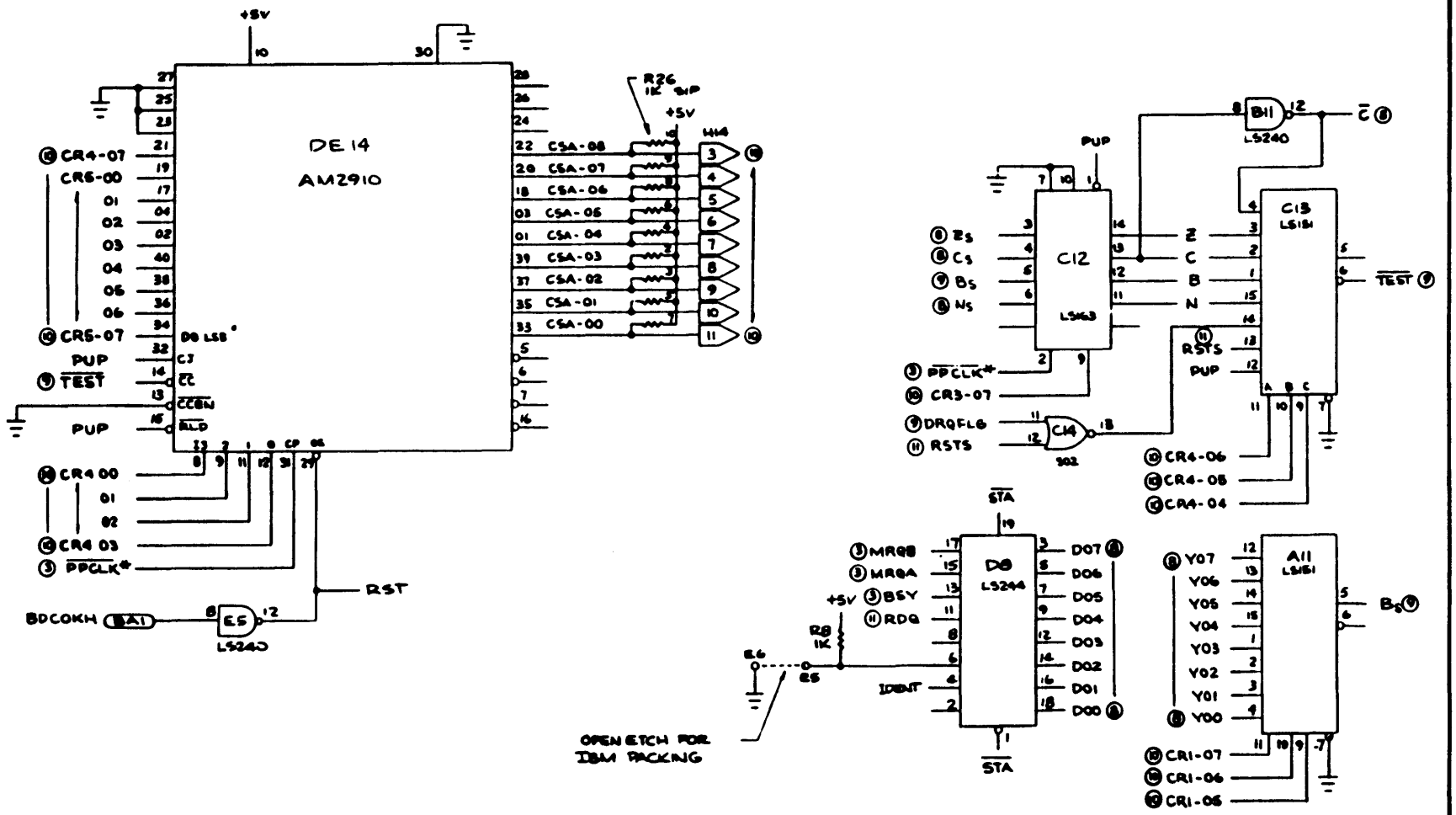

DISTRIBUTED LOGIC CORP.

| | | |
|---|---|---|
| SCALE | APPROVED BY: | DRAWN BY D.L. |
| DATE | | REVISED |
| LOGIC DIAGRAM, DQ130 | | SHT 7 OF 13 |
| | | DRAWING NUMBER 853016 |




1. RESISTORS ARE 470Ω ±5%, ¼W

| DISTRIBUTED LOGIC CORP. | | |
|---|---|---|
| SCALE | APPROVED BY | DRAWN BY D.L. |
| DATE | | REVISED |
| LOGIC DIAGRAM, DQ130 | | SHT 8 OF 13 |
| | | DRAWING NUMBER 853016 |




1. SYMBOL: (X) INDICATES 16 PIN DIP CONNECTOR LOCATED AT H14

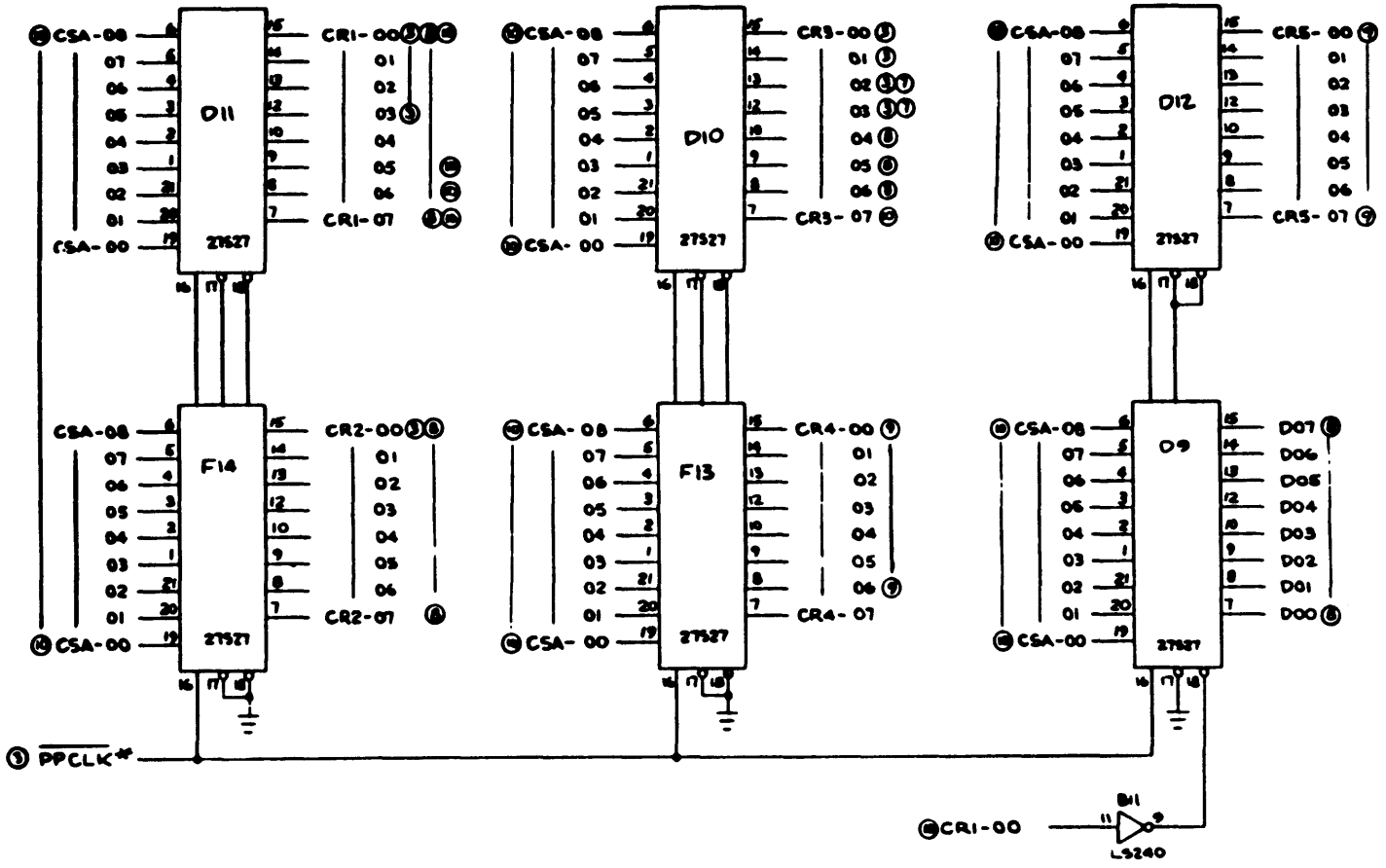
DISTRIBUTED LOGIC CORP.

| | | |
|---|---|---|
| SCALE | APPROVED BY: | DRAWN BY D.L. |
| DATE | | REVISED |

LOGIC DIAGRAM, DQ130

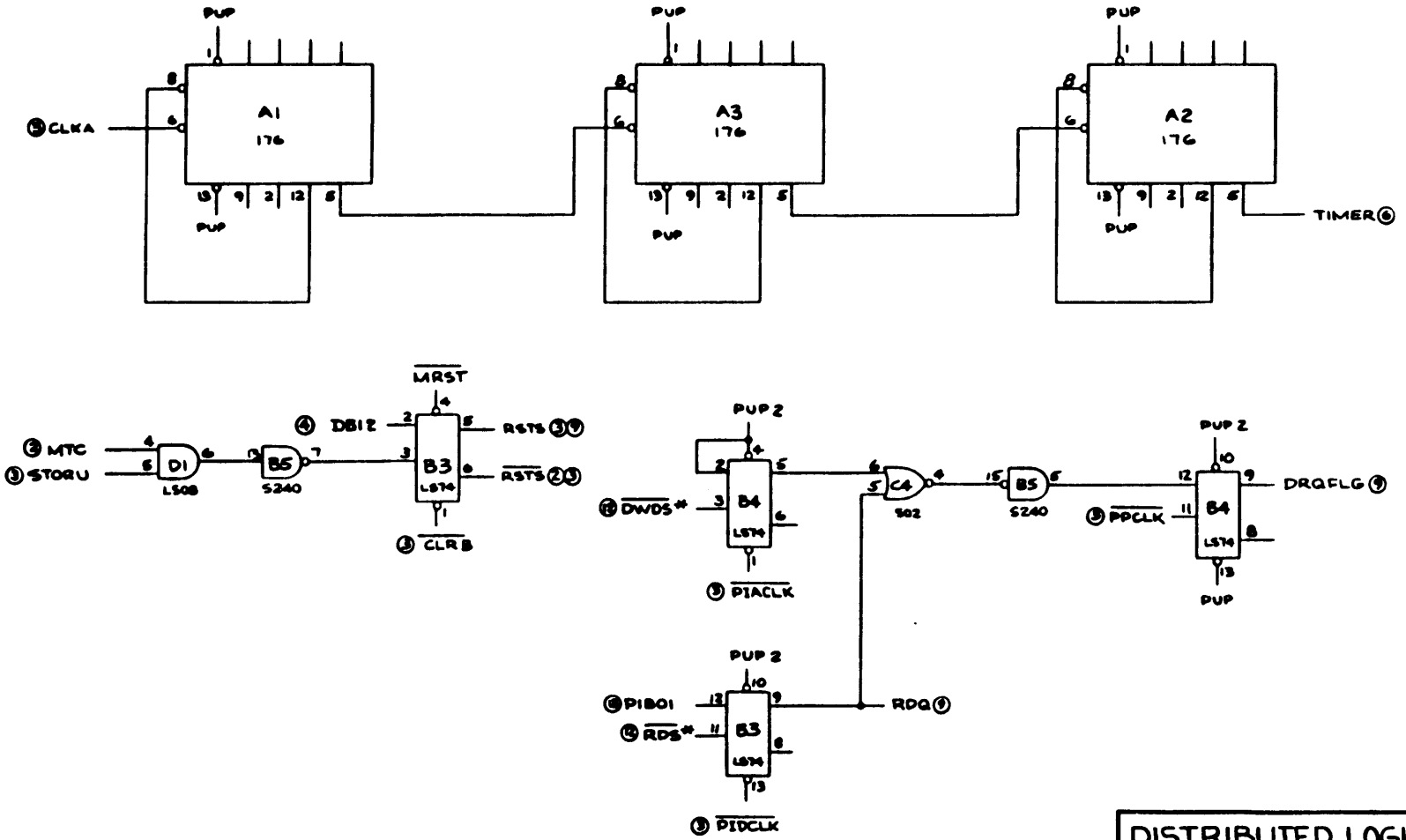
SHT 9 OF 13

863016




CONTROL STORE & PIPELINE

| DISTRIBUTED LOGIC CORP. | | |
|---|---|---|
| SCALE | APPROVED BY: | DRAWN BY D.L. |
| DATE | | REVISED |
| LOGIC DIAGRAM, DQ130 | | SHT 10 OF 13 |
| | | DRAWING NUMBER 853016 |

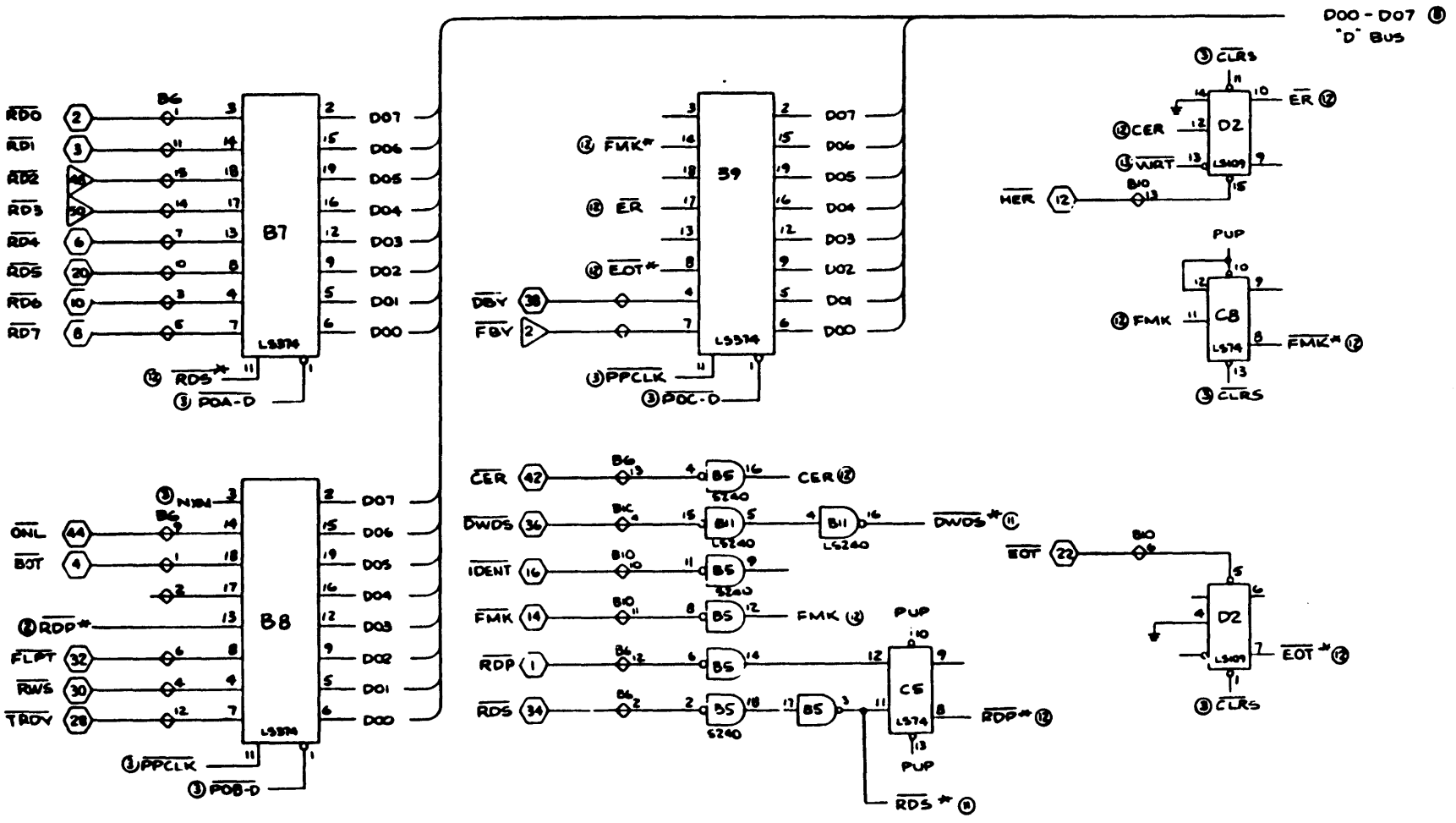



DISTRIBUTED LOGIC CORP.

LOGIC DIAGRAM, DQ130

SHT 11 OF 13

659016 A

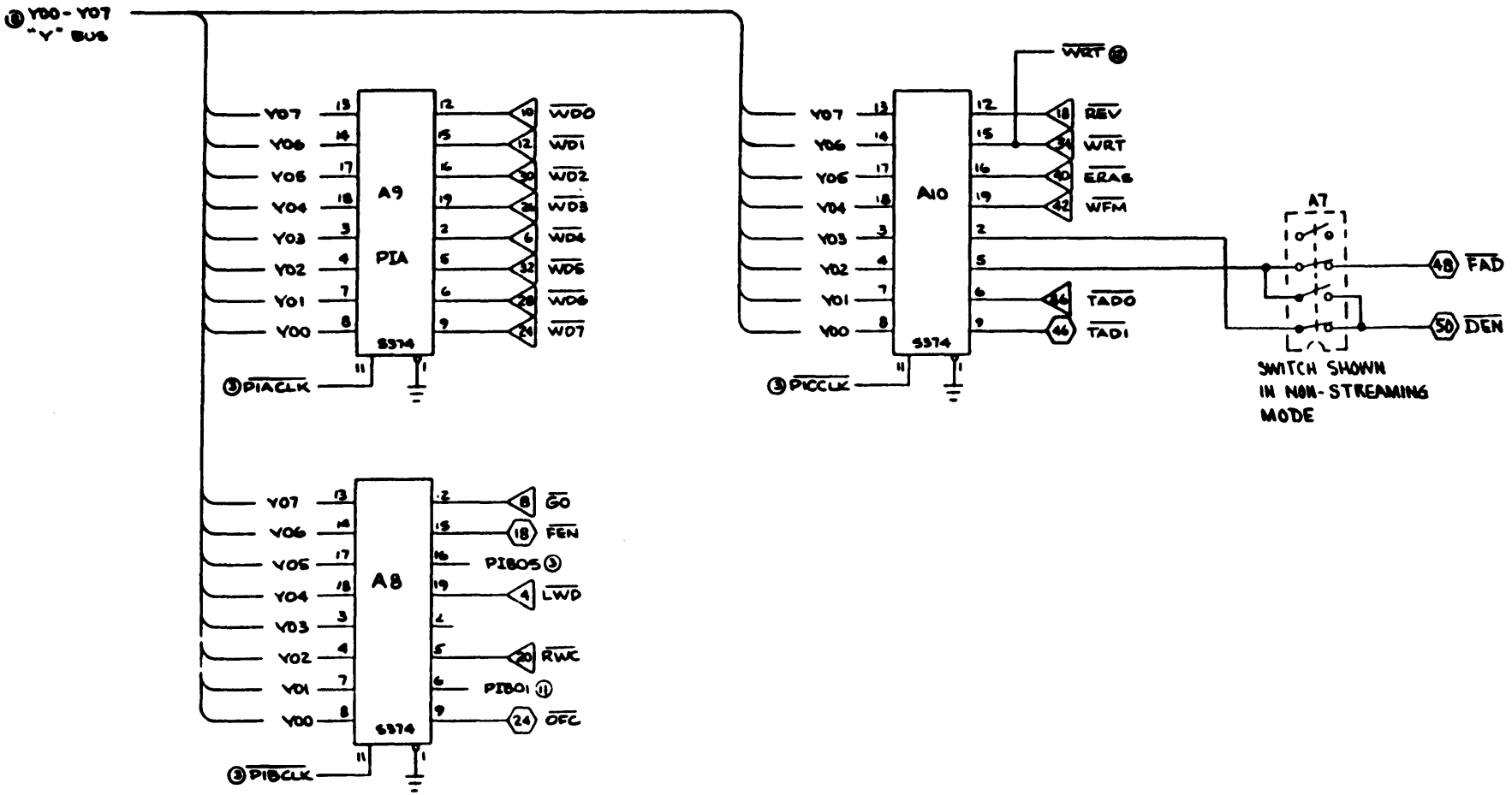



SYMBOL ▷ INDICATES "J2", 60 PIN CONNECTOR (ALL ODD PINS ARE GND.)

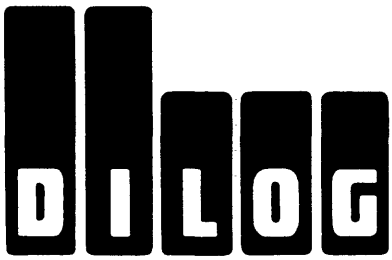
SYMBOL ⬡ INDICATES "J1", 50 PIN CONNECTOR (ODD PINS EXCEPT 1 & 3 ARE GND.)

NOTE: SYMBOL —◇— INDICATES 220Ω/330Ω TERMINATOR

| DISTRIBUTED LOGIC CORP. | | |
|---|---|---|
| SCALE | APPROVED BY | DRAWN BY D.L. |
| DATE | | REVISED |
| LOGIC DIAGRAM, DQ130 | | SHT 2 OF 13 |
| | | DRAWING NUMBER 855016 |




| DISTRIBUTED LOGIC CORP. | | |
|---|---|---|
| SCALE | APPROVED BY: | DRAWN BY D.L. |
| DATE | | REVISED |
| LOGIC DIAGRAM, DQ130 | | SHT 13 OF 13 |
| | | DRAWING NUMBER 853016 B |

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