

**DSD 6214**  
**DSD 6217**

**Multibus Disk Controller**  
**User Guide**

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## Preface

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This manual describes the features, specifications, and programming of the DSD 6214 and 6217 enhanced IEEE-796 (Multibus-compatible) disk drive controllers. The 6217 has a QIC-02 streaming tape drive interface; the 6214 does not. Except for streaming tape drive capability, the two controllers are identical. None of the information in this manual describing tape capability applies to the 6214.

The material in this manual is subject to change without notice. The manufacturer assumes no responsibility for any errors which may appear. Instructions for equipment installation, operation, and elementary troubleshooting are included.

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## 1. General Information

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### 1.1. Introduction

The DSD 6217 and 6214 are enhanced IEEE-796 (Multibus-compatible) disk drive controllers. The 6217 has a QIC-02 streaming tape drive interface; the 6214 does not.

Except for streaming tape drive capability, the two controllers are identical. None of the information in this manual describing tape capability applies to the 6214.

The controllers are compact single-board units for:

- Two (maximum) 5.25-inch Winchester drives.
- Two (maximum) 8-inch floppy drives.
- 6217 Only: Up to four QIC-02 streaming tape drives.

The DSD 6217 emulates the Intel iSBC 215 and iSBX 217/218 controller combination. The 6214 emulates the iSBC 215/iSBX 218 controller combination.

- The Winchester functions emulate the 215.
- The floppy drive functions emulate the 218.
- Some of the tape functions emulate the 217.

These emulated tape functions are referred to in this manual as 217 tape functions.

In addition to the 217 tape functions, the 6217 has a set of DSD tape functions that perform off-line mirror-image backup and restore between Winchester and tape. This is done without accessing the host bus.

Controller operation is compatible with software and operating systems supporting the emulated products. The



controllers offer the convenience of the emulated functions on a single board and, with the 6217, the DSD tape functions.

This manual provides user information for the DSD controller. Covered are: features, specifications, installation, operation, programming, architecture (with block diagram), and user-level maintenance.

## 1.2. Features

Features of the DSD controllers are:

- Support of standard interfaces:
  - For Winchester:
    - ST412;  
SA602, SA604, SA606;  
Tandon 602, 603;  
CDC 9415-21-5;  
CMI CM5206, CM5412.
    - RMS 503, 506, 512.
    - PYXIS 7, 13, 20, 27 (Rodime).
    - PYXIS 4, 8, 12, 16 (Ampex).
    - ST506.
    - Et 5510, 5520, 5530, 5540;  
XT-1065, 1105, 1140;  
V130, V150, V170.
    - 3020, 3033, 3046 (Atasi).
    - Q-500 (Quantum).
  - Floppy:
    - CDC-9406-4  
SA850
    - SA800
  - For streaming tape drives (6217 only):
    - QIC-02 Interface.
- All drives are connected pin-for-pin by flat ribbon cables for easier installation.
- All interfaces plus data separation are on one bus card for best system cost.

- Buffering is provided for noninterleaved operation and off-line mirror-image disk-to-tape backup operations.
- The controllers:
  - Offer built-in high reliability and data integrity.
  - Meet the requirements of the IEEE-796 specifications for the Multibus standard, including 24-bit addressing.
  - Emulate Intel's iSBC-215 and iSBX-217/218 controllers.
  - Are compatible with many operating systems:
    - RMX-86 (supported by Intel)
    - Unix
    - Xenix
    - CP/M
    - CP/M-86

### 1.3. Self-Test and Diagnostics

Resident PROM diagnostics may be used for fault isolation between the controller hardware, disk drives, or bus. Refer to Chapter 5 for detailed fault isolation procedures.

There are two LEDs, labelled CR1 and CR2, mounted on the controller card. These LEDs respond according to the selected options and any error conditions. CR1 blinks when an error is detected. CR2 is on when the controller is ready to accept a new command.

Chapter 2, section 5, details the use of these indicators during initial checkout and acceptance testing. Other information about their use can be found in Chapter 5.

### 1.4. Off-Line Backup Capability (6217 Only)

The quarter-inch streaming tape drives can provide off-line backup for the Winchester drive. The QIC-02 interface is on the 6217. The tape drive controller does not access the host bus. The 6217 controls the tape drive controller directly. This allows data transfer without accessing the host bus.

The DSD tape functions perform full image backup and restore at five megabytes per minute. These functions (codes 80H, 81H, 82H, and 83H: see Chapter 3) are provided in addition to all emulated functions.



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## 2. Hardware Configuration

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### 2.1. Unpacking and Inspection

When the DSD Controller arrives, inspect the shipping container immediately for evidence of mishandling during transit. If the container is damaged, request that the carrier's agent be present when the package is opened. Compare the packing list attached to the shipping container against your purchase order to verify that the shipment is correct.

Unpack the shipping container and inspect each item for external damage. If damage is evident, notify DSD Customer Service. Retain the shipping container and packing materials for examination in the settlement of claims or for future use.

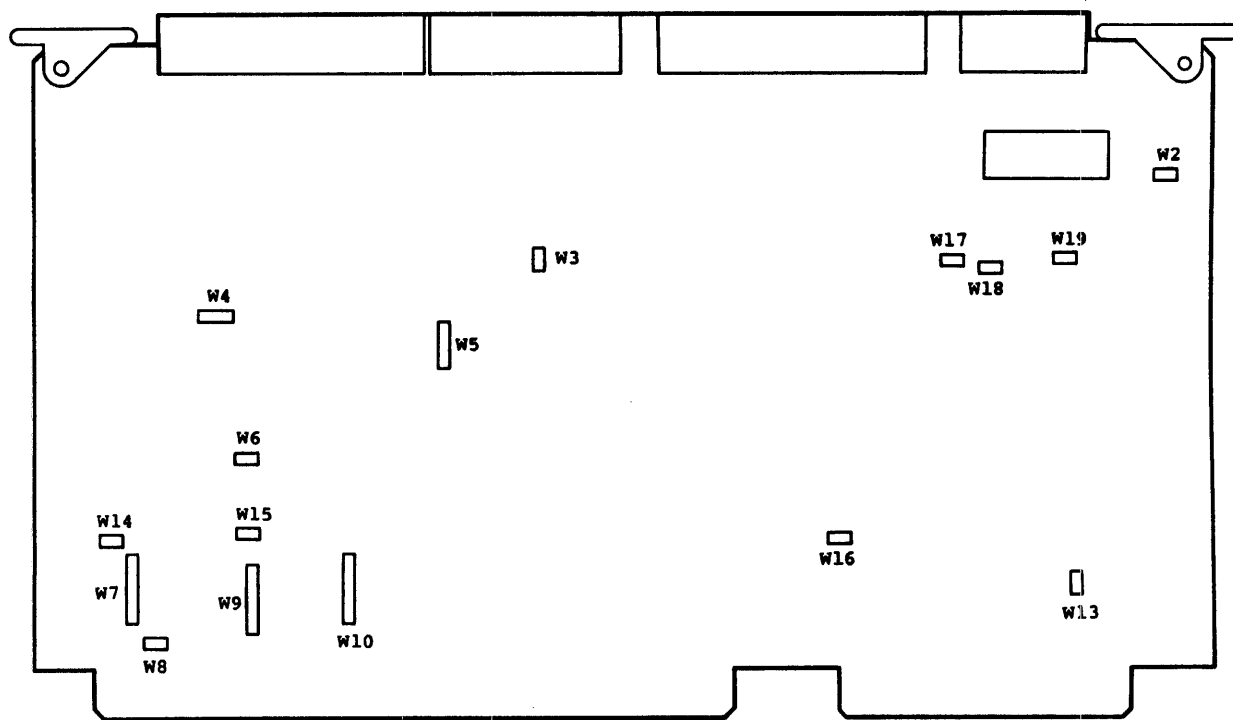
## 2.2. Jumper Options

There are nine selections to be made with the jumper options:

- (1) 8- or 16-bit I/O addressing: jumper W14
- (2) Wake-up address: jumpers W7 and W9.
- (3) 8- or 16-bit data transfers: jumper W3
- (4) Serial or parallel bus priority: jumper W8
- (5) Bus arbitration mode: jumper W5
- (6) Interrupt priority level: jumper W10
- (7) Winchester drive configuration: jumper W6-2, W6-3, W6-4
- (8) Floppy drive configuration: jumper W6-0, W6-1
- (9) Diagnostics: jumper W6-5

Figure 2-1 shows the location and pin configuration of all user-configurable jumpers on the controller board. Jumpers W2, W4, W13, W17, W18, and W19 are for factory use only and should not be changed in the field. It should be noted that there are no jumpers labelled W1, W11, or W12 on the board.

Most of the jumpers are user-configured by placing a Berg mini-jumper on the indicated pins. Jumper W10 is an exception. It is wire-wrapped at the factory because the physical layout of the pins precludes the use of mini-jumpers.



TP 542 84

Figure 2-1. Jumper Locations

### 2.2.1. Select 8- or 16-bit I/O Address

Select with jumper W14. See Figure 2-1 and Table 2-6.

### 2.2.2. Select Wake-Up Address

Jumper groups W7 and W9 select the wake-up address (WUA). See Figure 2-1, Table 2-1, and Table 2-6. The WUA serves as both the address of the I/O port, and the source of the wake-up block (WUB) address. Refer to paragraph 3.3.1 for information about the WUB.

- Jumpers W7 and W9 select (directly) the address of the I/O port used by the host device driver program to give commands to the controller.
- With 8-bit I/O addressing, jumper group W9 selects the WUA; the jumpers of group W7 should be set to zero. For 16-bit I/O addressing, both groups are used.
- The WUB address is computed from the WUA: the WUA is multiplied by 16 (shifted left four bits) to obtain the address of the WUB. Because of this multiplication, the four least significant bits of the computed WUB address are zeros. The WUB must be set up by the host device driver program at this computed address in main memory.
- If only the 16 least significant bits of the computed WUB address are used, the four most significant bits set with jumper group W7 are not used.

Table 2-1. W7 and W9 WUA Address Jumper Groups

Jumper Group:	W 7	W 7	W 7	W 7	W 7	W 7	W 7	W 7	W 9	W 9	W 9	W 9	W 9	W 9	W 9	W 9				
Bits/Pins:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Jumpered Value: n = 1 or 0 X = 0 only	X	X	X	X	X	X	X	X	n	n	n	n	n	n	n	n				
									Value jumpered with W9 Selects an 8-bit I/O address											
Jumpered Value: n = 1 or 0	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n				
	Value jumpered with W7 and W9 selects a 16-bit I/O address																			
	20-bit WUB address computed from jumpered value by multiplying by 16: adds 4 zero bits. -----																			
Pins:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	3	2	1	0
Bits:	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Jumpered Value: n = 1 or 0	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	0	0	0	0
																	Always zero			
	If only 16 bits of computed WUB are used, values set by jumpers W7-12 through W7-15 not used.																			

2.2.3. Select 8- or 16-bit data transfers

Select with jumper W3. See Figure 2-1 and Table 2-6.

2.2.4. Select Serial or Parallel Bus Priority

Select with jumper W8. See Figure 2-1 and Table 2-6.



Table 2-1. W7 and W9 WUA Address Jumper Groups

Jumper Group:	W 7	W 7	W 7	W 7	W 7	W 7	W 7	W 7	W 7	W 9	W 9	W 9	W 9	W 9	W 9	W 9	W 9							
Bits/Pins:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
Jumpered Value: n = 1 or 0 X = 0 only	X	X	X	X	X	X	X	X	n	n	n	n	n	n	n	n	n							
									Value jumpered with W9 Selects an 8-bit I/O address															
Jumpered Value: n = 1 or 0	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n							
	Value jumpered with W7 and W9 selects a 16-bit I/O address																							
	20-bit WUB address computed from jumpered value by multiplying by 16: adds 4 zero bits. -----																							
Pins:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	3	2	1	0				
Bits:	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Jumpered Value: n = 1 or 0	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	0	0	0	0
																	Always zero							
																	If only 16 bits of computed WUB are used, values set by jumpers W7-12 through W7-15 not used.							

2.2.3. Select 8- or 16-bit data transfers

Select with jumper W3. See Figure 2-1 and Table 2-6.

2.2.4. Select Serial or Parallel Bus Priority

Select with jumper W8. See Figure 2-1 and Table 2-6.

### 2.2.5. Select Bus Arbitration Mode

Select with jumper W5. See Figure 2-1 and Table 2-6. The bus arbitration mode options are placed in order of increasing throughput and decreasing bus availability. The bus, acquired on the basis of availability, is always released at the end of burst transfer. Maximum burst length is one full sector per bus grant.

- Single-Transfer: Control of the host bus is acquired before each data transfer and released immediately after. This minimizes controller time on the bus, but compromises maximum throughput capability.
- Yield to Any Request: The bus is released for any request, regardless of priority, through use of the CBRQ/ signal (connector P1, pin 29), or when the transfer of a block of data is completed. This allows maximum throughput capability only when other bus masters do not want to use the bus.
- Yield to Higher Priority: The bus is released only for higher priority requests, or when the transfer of a block of data is completed. This allows maximum throughput capability only when higher priority bus masters do not want to use the bus.
- Override: Higher priority bus master requests are overridden. The bus is released only at the end of data transfer. This guarantees maximum throughput performance. Serial or parallel bus.

### 2.2.6. Select Interrupt priority level

Select with jumper W10. See Figure 2-1 and Table 2-6.

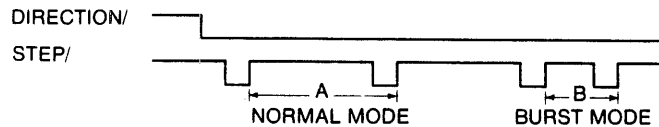
### 2.2.7. Select Winchester Drive Class

Select with jumpers W6-2, W6-3, W6-4. See Figure 2-1, Table 2-2 and Table 2-6. One method of classifying Winchester drives is according to control timing sequences and requirements for reduced write current and precompensation.

Table 2-2 shows some Winchester drives grouped according to the indicated characteristics. All available drives are not listed. The table contains only a representative selection as examples. Use these examples and match characteristics with drives not shown. Contact DSD Customer Service for correct jumper configuration for higher performance Winchester drives not listed.

Table 2-2. Winchester Drive Characteristics

## WINCHESTER CONTROL TIMING/PRECOMP/READ WRITE CURRENT



TP 341 83

Drive Class	STEP/ Normal A	STEP/ Burst B	Precomp 12 ns Cylinders	Reduced Write Current Cylinders
0	3 ms	25.0 us	>= 128	>= 128
1	3 ms	25.0 us	>= 77	>= 77
2	2 ms	25.0 us	>= 0	>= 132
3	3 ms	25.0 us	>= 0	>= 96
4	3 ms	3.0 us	>= 128	>= 128
5	3 ms	10.8 us	none	none
6	3 ms	10.8 us	>= 320	none
7	3 ms	10.8 us	>= 256	none

Table 2-3. Winchester Drive Classes

Drive Class	Typical Drives
0	ST412; SA602, SA604, SA606; Tandon 602, 603; CDC 9415-21-5; CMI CM5206, CM5412.
1	RMS 503, 506, 512.
2	PYXIS 7, 13, 20, 27 (Rodime).
3	PYXIS 4, 8, 12, 16 (Ampex).
4	ST506.
5	Et 5510, 5520, 5530, 5540; XT-1065, 1105, 1140; V130, V150, V170.
6	3020, 3033, 3046 (Atasi).
7	Q-500 (Quantum).

If your drive is listed in Table 2-3, set jumper W6 as shown in Table 2-4. If your drive is not listed, attempt to match it with one of the classes shown in the table, or call DSD Customer Service for assistance.

Table 2-4. W6 Jumper Configuration, Winchester

Supported Winchester Drive Classes	Jumper Group W6			
	W6-5	W6-4	W6-3	W6-2
0	One	One	One	One
1	One	One	One	Zero
2	One	One	Zero	One
3	One	One	Zero	Zero
4	One	Zero	One	One
5	One	Zero	One	Zero
6	One	Zero	Zero	Zero
7 (Reserved)	One	Zero	Zero	Zero

W6-5 (normally One) selects HyperDiagnostics when Zero (see Chapter 5).

#### 2.2.8. Select Floppy Drive Configuration

Select with jumpers W6-0 and W6-1. See Figure 2-1 and Table 2-6. The controller operates floppy drives that are SA850-compatible. Set jumper group W6 as shown in Table 2-5.

Table 2-5. W6 Jumper Configuration, Floppies

Supported Floppy Drives	Jumper Group W6		
	W6-5	W6-1	W6-0
CDC-9406-4, SA850	One	One	One
SA800	One	One	Zero
Future Drive Type*	One	Zero	One
Future Drive Type*	One	Zero	Zero

\* Reserved

W6-5 (normally One) selects HyperDiagnostics when Zero (see Chapter 5).

#### 2.2.9. Select Diagnostic Functions

Selected with jumper W6-5. See Figure 2-1 and Table 2-6. This jumper is normally set to One, to enable drive operation. When this jumper is set to Zero, the HyperDiagnostic routines are performed, rather than drive operations (see Chapter 5).

Table 2-6. Factory Jumper Settings

Jumper	Function	Factory Setting			Options	Remarks
		Pins	One	Zero		
W2	Factory Use Only	1-2	X		None	Leave as set
W3	8- or 16- Bit Data Transfers	1-2		X	8-bit data bus One = 16-bit bus	User option
W4	Factory Use Only	1-2 3-4	X X		None	Leave as set
W5	Bus Arbitration Mode Select	1-2 2-3 2-4 5-6	X  X	 X X	Yield to higher priority One = Yield to any request One = Single-transfers One (with 1-2 One) = Override	User option. Except for override, only one jumper should be One.
W6	Disk and Diagnostic Configuration.	6-0 6-1 ----- 6-2 6-3 6-4 ----- 6-5	X X  X X X  X	 X  X X X  X	Select 8 in Floppy Drive Type  Select 5.25 in Winchester Drive Class  Exercise Diagnostic Functions	User Option
W7	Most Significant Byte of WUA Set at Factory To 0FH	7-15 7-14 7-13 7-12 ----- 7-11 7-10 7-9 7-8	   X  X X X	X X X X     X	Most Significant Bit        For Options, see paragraph 2.2.2	User Option
W9	Least Significant Byte of WUA Set at Factory To 70H	9-7 9-6 9-5 9-4 ----- 9-3 9-2 9-1 9-0	 X X X    X X X X	          X X X X	          Least Significant Bit	
W8	Serial or Parallel Bus Priority Continuity	1-2	X		Serial Zero = Parallel	User option
W10	Interrupt Priority Level Select	C-0 C-1 C-2 C-3 C-4 C-5 C-6 C-7	    X X X X	 X X X X X X X	Priority level 0 (highest) Priority level 1 Priority level 2 Priority level 3 Priority level 4 Priority level 5 (factory) Priority level 6 Priority level 7 (lowest)	User option (wire-wrapped)
W13	Factory Use Only	1-2	X		None	Leave as set
W14	8- or 16- Bit I/O Address Select	1-2 2-3	 X	 X	8-bit I/O address Zero = 16-bit (with 1-2 One)	User option
W15	Factory Use Only	A B	X  X	  X	None	Leave as set
W16	Factory Use Only				None	Leave as set
W17	Factory Use Only				None	Leave as set
W18	Factory Use Only				None	Leave as set
W19	Factory Use Only				None	Leave as set

Jumper groups W6, W7, and W9 are further documented in other tables in this Chapter. Jumpers W1, W11, and W12 are not physically present on the board.

### 2.3. Installation

The controller board may be installed in any IEEE-796, Multibus-compatible backplane that meets the power and cooling requirements specified in Appendix A. Note that power MUST be OFF when installing or removing the controller board.

Up to two floppies, two Winchesters, and four streaming tape drives may be connected to the controller (see Figure 2-2).

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Note  
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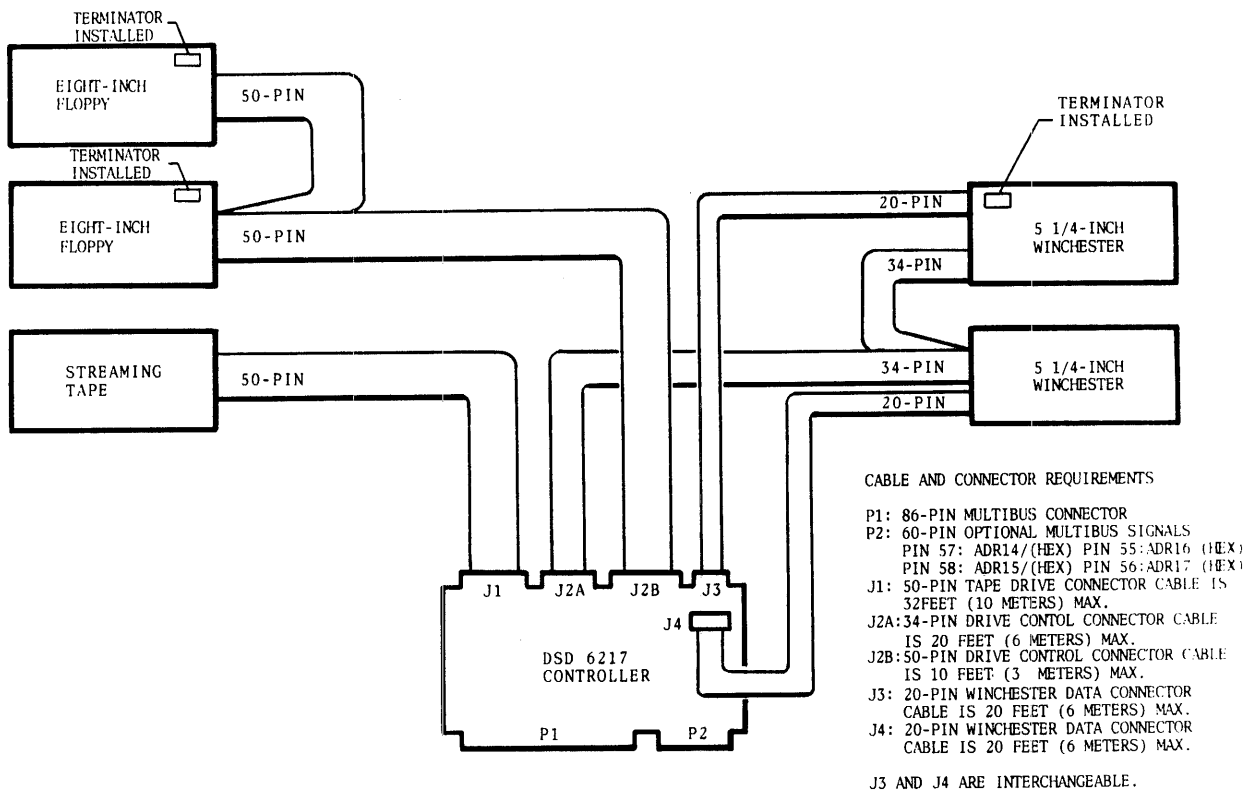
Terminators must be installed in the last Winchester and the last floppy drive. Consult the documentation provided by the drive manufacturer for instructions covering terminating resistor installation.  
 -----

### 2.4. Drive Jumpering

Information concerning jumper options on the disk drive controller cards is contained in Appendix B. All drives must be correctly jumpered to ensure proper operation, and terminators MUST be installed in the last Winchester and last floppy disk drive connected to the controller. Consult the documentation provided by the drive manufacturer for instructions covering terminating resistor installation.

Drive jumper configuration tables are provided for the following type drives:

- Winchester: ST412
- Floppy:
  - SA800/801
  - SA850/851
  - CDC-9406-4



TP 548 84

Figure 2-2. Cables and Connectors

### 2.5. Initial Checkout and Acceptance Tests

Two LEDs, at board positions A1 and A3 (upper left corner), indicate controller status or an error condition. LED CR2 (RDY) indicates whether the board is ready to accept a new command (on), or is busy (off). LED CR1 (ERR) blinks when an error is detected. These indicators, after a reset condition, indicate if the board is performing properly. Indicator sequence is shown in Figure 2-3.

When self-test is complete, CR2 (RDY) will be on. If CR1 (ERR) is off, self-test was successful and the board is ready to receive a new command. If CR1 (ERR) is blinking, a recognized error is indicated. Refer to Chapter 5 for fault analysis procedures.

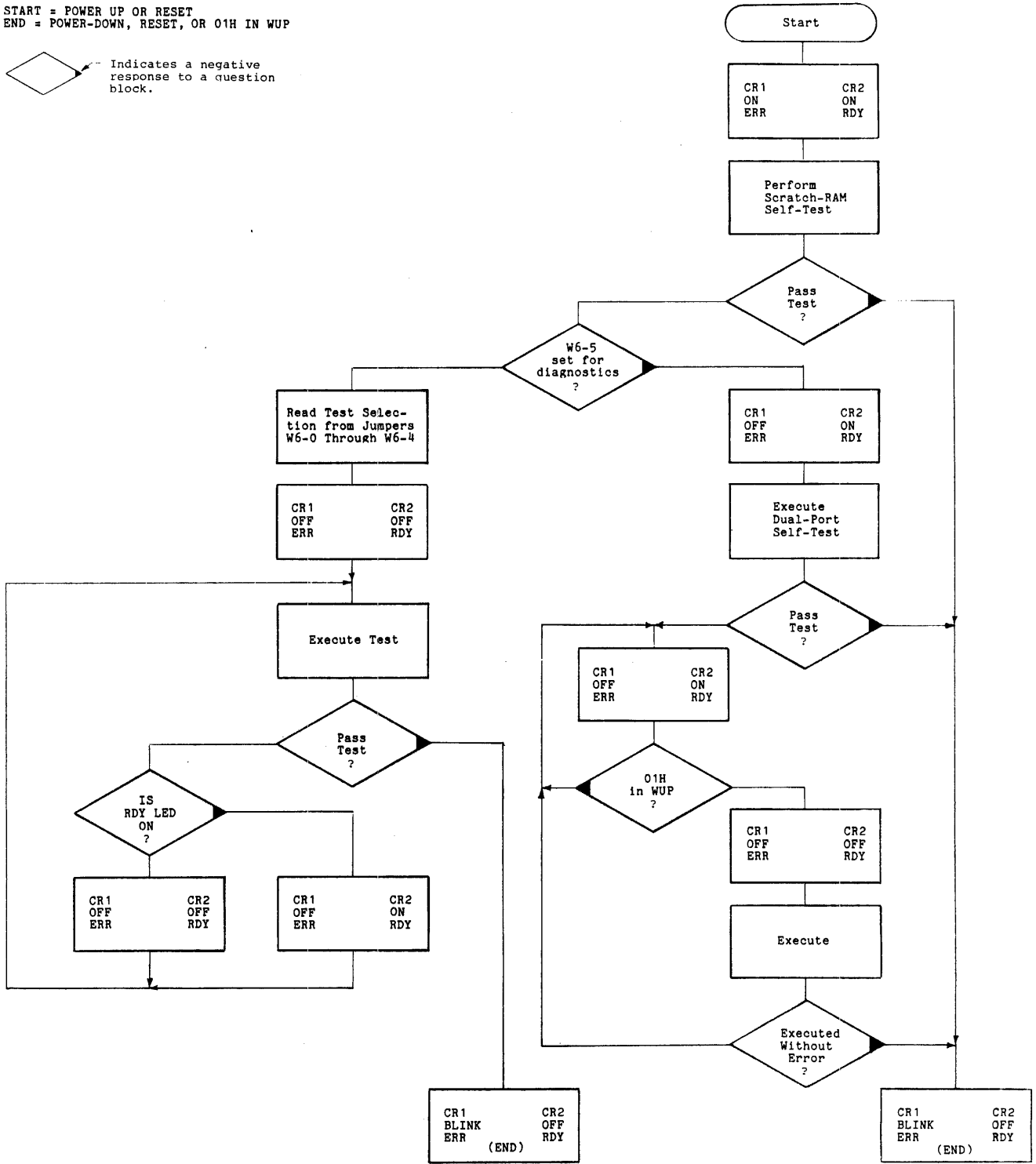
### 2.6. Test and Verification

Up to this point, no other host bus cards have been required, only power. The user may further verify system operation using off-line diagnostics to check that all peripherals are operational. These tests are selected using jumper W6. Refer to Chapter 5 for information on tests and jumper reconfiguration.



START = POWER UP OR RESET  
END = POWER-DOWN, RESET, OR 01H IN WUP

◊ Indicates a negative response to a question block.



TP 541-84

Figure 2-3. Indicator Sequence



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### 3. Programming

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#### 3.1. Introduction

The programmer's task is to write a host device driver program that will operate the controller. This chapter describes what the controller requires of the program.

The program must be able to:

- (1) Initiate controller operation by issuing the program command sequence (detailed in section 3.2) necessary to reset the controller.
- (2) Build a series of control blocks in main memory (detailed in section 3.3).
- (3) Write, in these control blocks, the data required to request the various controller functions (detailed in section 3.6). The function being requested is specified in the function field of the input/output parameter block (IOPB: detailed in paragraph 3.3.4).

Two important definitions are:

- Program Command:

A program command is one issued by the program to regulate the controller (detailed in section 3.2). A program command is issued by executing an I/O write to the address selected by jumpers W7 and W9 (detailed in paragraph 2.2.2). There are three program commands:

- Clear Interrupt/Remove Reset (00H): Detailed in paragraph 3.2.1
- Start (01H): Detailed in paragraph 3.2.2
- Reset Controller (02H): Detailed in paragraph 3.2.3

- Controller Function:

A controller function (detailed in section 3.6) is a task that the controller must execute in response to a program command. There are 28 controller functions (see Table 3-1). It must be remembered that the 6214 has no tape functions.

Table 3-1. Controller Functions

Figure	Function
3-8.	Initialization (00H): 5 1/4-inch Winchester Disk
3-9.	Initialization (00H): 8-Inch Floppy Disk
3-10.	Initialization (00H): 217 Tape Functions
3-11.	217 Tape: Initialization (10H)
3-12.	217 Tape: Reset (1CH)
3-13.	217 Tape: Rewind (11H)
3-14.	Format (02H)
3-16.	Transfer Status (01H)
3-17.	Diagnostics (0FH)
3-18.	Read Data (04H)
3-19.	Write Data (06H)
3-20.	Read Data Into Controller Buffer (05H)
3-21.	Write Data From Controller Buffer (07H)
3-22.	Read Sector ID (03H)
3-23.	Initiate Track Seek (08H)
3-24.	Buffer I/O (0EH)
3-25.	217 Tape: Transfer Status (01H)
3-26.	217 Tape: Read Status (1EH)
3-27.	217 Tape: Read Data (04H)
3-28.	217 Tape: Write Data (06H)
3-29.	217 Tape: Read/Write Terminate (1FH)
3-30.	217 Tape: Move Forward One File (12H)
3-31.	217 Tape: Move Forward One Record (1AH)
3-32.	217 Tape: Write File Mark (14H)
3-33.	217 Tape: Retension Tape (1DH)
3-34.	217 Tape: Erase (17H)
3-35.	DSD Tape: Reset Drive (80H)
3-36.	DSD Tape: Retension Cycle (84H)
3-37.	DSD Tape: Disk-Image Back-up (81H)
3-38.	DSD Tape: Disk-Image Restore (82H)
3-39.	DSD Tape: Read Tape Status (83H)

Program/controller communication is divided into four areas for discussion:

- Program Commands (section 3.2)
- Control Blocks (section 3.3)
- Handshaking (section 3.4)
- Controller Functions (section 3.6)

### 3.2. Program Commands

The three program commands that regulate the controller are:

- Clear Interrupt/Remove Reset (00H): detailed in paragraph 3.2.1
- Start (01H): detailed in paragraph 3.2.2
- Reset Controller (02H): detailed in paragraph 3.2.3

To issue one of these commands, the program must execute an I/O write operation to the I/O port addressed by the WUA jumpers (W7 and W9: detailed in paragraph 2.2.2). The value written must have, as its two least significant bits, the hex value that represents the desired command. When an I/O write is detected by the controller, it evaluates the two least significant bits as the program command.

#### 3.2.1. Clear Interrupt/Remove Reset (00H)

This program command clears the controller-to-host interrupts, and can clear a reset controller (02H) condition. The clear interrupt/remove reset (00H) command is required after:

- a reset controller (02H) program command, or
- an assertion of the host bus INIT/ signal, or
- power-up.

-----  
Note  
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A reset controller (02H) program command must be removed by a clear interrupt/remove reset (00H) command, and then the program command sequence leading to an initialize (00H) controller function (detailed in section 3.6) must be executed before any drive can be accessed.  
 -----

### 3.2.2. Start (01H)

This program command has a special function when used immediately following a clear interrupt/remove reset (00H) command. It causes the controller to fetch the jumpered wake-up address (WUA: detailed in paragraph 2.2.2), compute the address of the wake-up block (WUB), and read through the chain of control blocks (detailed in section 3.3), ending with the controller invocation block (CIB).

Before issuing this first start (01H) command, the program must set the busy 1 field (detailed in paragraph 3.3.2) in the channel control block (CCB) to FFH. Until the busy 1 field is cleared, the program must refrain from interfering with the controller.

When the busy 1 field is cleared after the first start command, it indicates that the controller has the addresses of the CCB, CIB, and input/output parameter block (IOPB); and is ready for the IOPB to be built, with a controller function code in the function field.

Any subsequent start (01H) command causes the controller to access the IOPB, and to begin execution of the specified controller function.

### 3.2.3. Reset Controller (02H)

This program command causes the controller hardware to reset immediately. All operations abort, any data being buffered on board the controller is lost, and no status information is posted in the CIB.

### 3.3. Control Blocks

The control blocks (except for the WUB) can be established anywhere in main memory that is convenient for the user. There are six control blocks:

- Wake-Up Block (WUB): detailed in paragraph 3.3.1
- Channel Control Block (CCB): detailed in paragraph 3.3.2
- Controller Invocation Block (CIB): detailed in paragraph 3.3.3
- Input/Output Parameter Block (IOPB): detailed in paragraph 3.3.4
- Two of the control blocks are used with the IOPB:
  - Data Buffer
  - Tape Parameter Buffer (TPB)



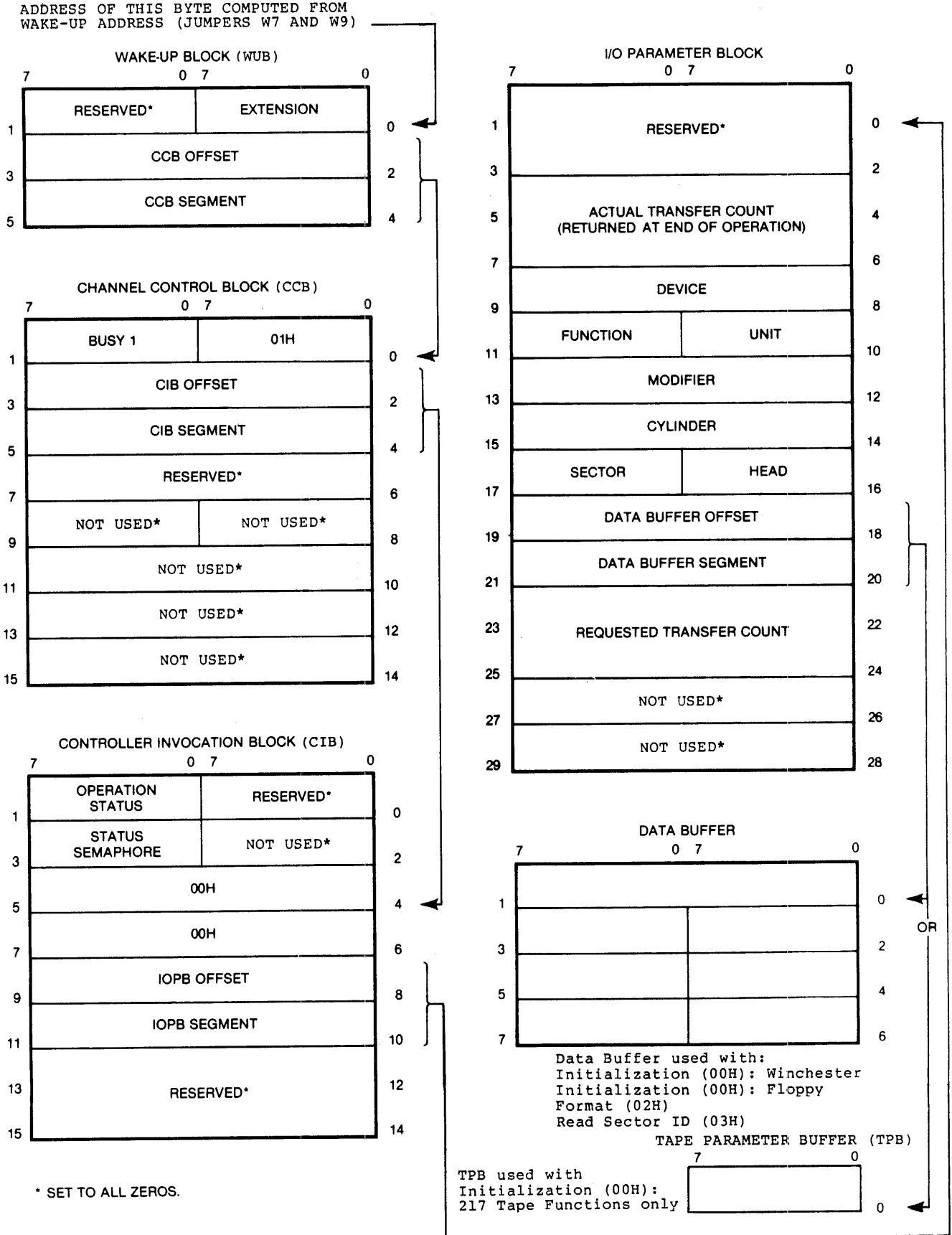


Figure 3-1. Chain of Control Blocks

### 3.3.1. Wake-Up Block (WUB)

The wake-up block is first in the control block chain. The program must set up the WUB in main memory at the WUB address computed from jumpers W7 and W9 (detailed in paragraph 2.2.2). Figure 3-2 shows the layout of the WUB in main memory.

On recognition of the first start (01H) command from the program, the controller computes the address of the WUB from the wake-up address. The controller accesses the WUB and saves the data that was written there by the program.

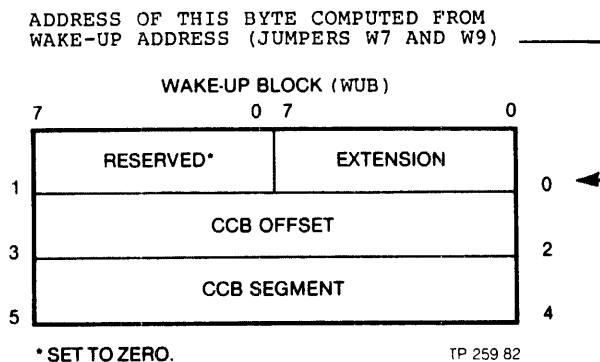


Figure 3-2. Wake-up Block (WUB)

The program must write two values in the WUB for the controller to read:

- (1) The CCB Address Pointers. Bytes 2 through 5 point to the CCB address in main memory.
- (2) The Extension Byte. Byte 0 is the extension byte. It may contain one of four different values:
  - (01H) Segmented (20-bit) addressing enabled (detailed in paragraph 3.3.5).
  - (03H) Linear (24-bit) addressing enabled (detailed in paragraph 3.3.5).
  - (05H) Segmented addressing with extended status (detailed in paragraph 3.6.6) and extended diagnostics (diagnostic (0FH) function: detailed in paragraph 3.6.7) enabled.
  - (07H) Linear addressing with extended status and diagnostics enabled.

The WUB is only accessed by the controller in response to the first start (01H) program command following a reset. Once accessed, the WUB need not be preserved, because the controller saves the WUB data in its internal memory for use in the current operating session, or until a reset occurs.

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Note

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Extended status reporting and the extended form of the diagnostic (0FH) function are enabled by values that the program must write in the WUB. In order to use the extended features, the enabling values must be in the WUB when the controller accesses it in response to the first start (01H) program command following a reset.

Once the WUB has been accessed, extended features cannot be enabled without a complete reset of the controller and drives.

---

3.3.2. Channel Control Block (CCB)

The channel control block is second in the control chain. The program must set up the CCB in main memory at the address pointed to in the WUB. Figure 3-3 shows the layout of the CCB in main memory.

This block is used in handshaking and operation status transfers (detailed in section 3.4) between the program and the controller. The controller does not use the last ten bytes in this block. They are shown for compatibility with iSBC operation only.

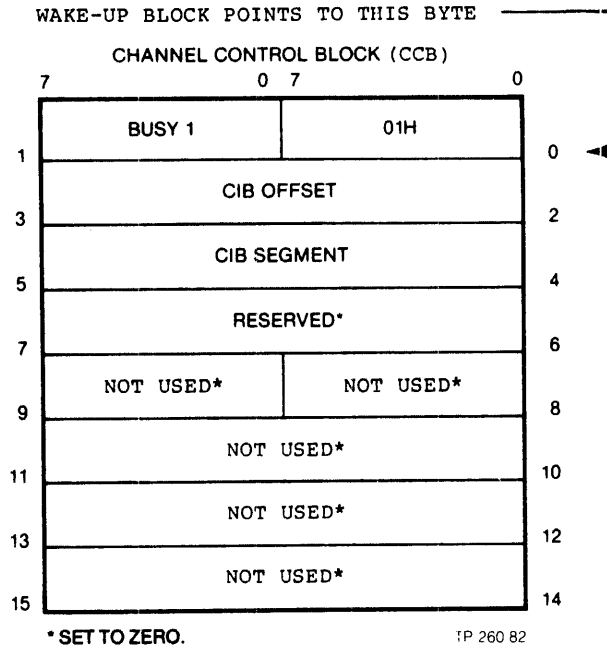


Figure 3-3. Channel Control Block (CCB)

The program must write three values in the CCB for the controller to read:

- (1) Byte 0. The first byte must contain a value of 01H. If it does not contain a value of 01H when accessed by the controller, processing ceases with no status returned, and an error is indicated by LED CR1 (ERR).
- (2) The Busy 1 Field. The second byte (byte 1) contains the busy 1 field. This field is used only with the first start (01H) command. The program must set the busy 1 field to FFH when the CCB is established. The controller will clear busy 1 in response to the first start (01H) command that follows any power up or reset.
- (3) The CIB Address Pointers. Bytes 2 through 5 point to the CIB address in main memory. Note that the pointer in the CCB points to byte 4 of the CIB, not byte zero.

-----  
Note  
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The addresses of the CCB and CIB are retained by the controller until a reset or power-up occurs. During operation, the controller frequently accesses these control blocks, using the stored addresses. Therefore, these control blocks cannot be relocated without a controller reset and initialization sequence.  
-----

### 3.3.3. Controller Invocation Block (CIB)

The controller invocation block is third in the control chain. The program must set up the CIB in main memory at the address pointed to in the CCB. Figure 3-4 shows the layout of the CIB in main memory.

This control block is used in handshaking and operation status transfers (detailed in section 3.4) between the program and the controller.

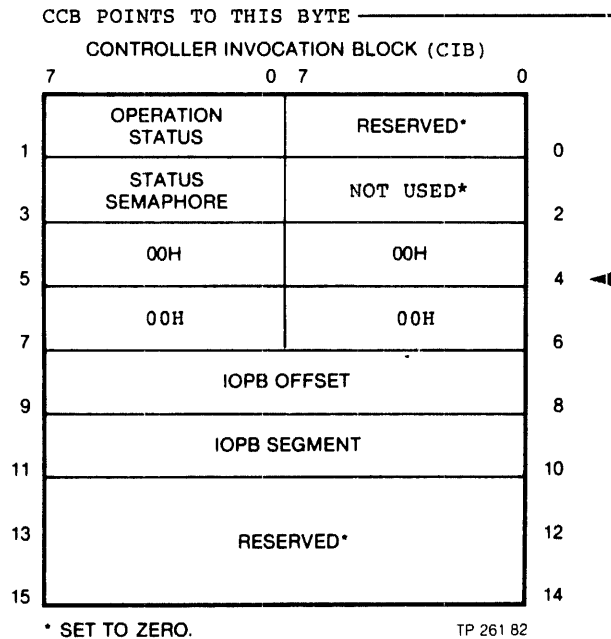


Figure 3-4. Controller Invocation Block (CIB)

The program must write 3 values in the CIB for the controller to read:

- (1) Bytes 4 through 7. These are the first bytes accessed by the controller in the CIB. They must be set to zero.
- (2) Status Semaphore. The program must set this field to 00H when the CIB is set up in main memory. The controller posts new status in its on-board buffer only when this block in main memory is 00H. After posting new status, the controller sets this byte to FFH. After the program reads status, it should reset this byte to 00H.
- (3) The IOPB Address Pointers. Bytes 8 through 11 point to the IOPB address in main memory.



### 3.3.4. I/O Parameter Block (IOPB)

The input/output parameter block is fourth in the control chain. The program must set up the IOPB in main memory at the address pointed to in the CIB. Figure 3-5 shows the layout of the IOPB in main memory.

Except for the actual transfer count, the program must write the specific data required by the controller for each function in the various fields of the IOPB. The controller writes to the actual transfer count field when reporting the number of bytes transferred in the execution of a function.

The program must write up to 9 values in the IOPB for the controller to read, depending on the function being requested. In the section describing each function, the values that must be written to request that function are shaded. The nine possible values are:

- (1) Device. This field (bytes 8 and 9) specifies the device type accessed, or the function set to be used. The possible values for the device field are:

0000H = Winchester Drive  
 0001H = Floppy Disk Drive  
 0004H = Streaming Tape Drive (217 tape function)  
 0010H = Streaming Tape Drive (DSD tape function)

- (2) Function. This field (byte 11) specifies the function to be executed: read, write, format, etc. The functions, and the hex code that appears in the IOPB function field are listed in Table 3-3. The individual functions are detailed in section 3.6.



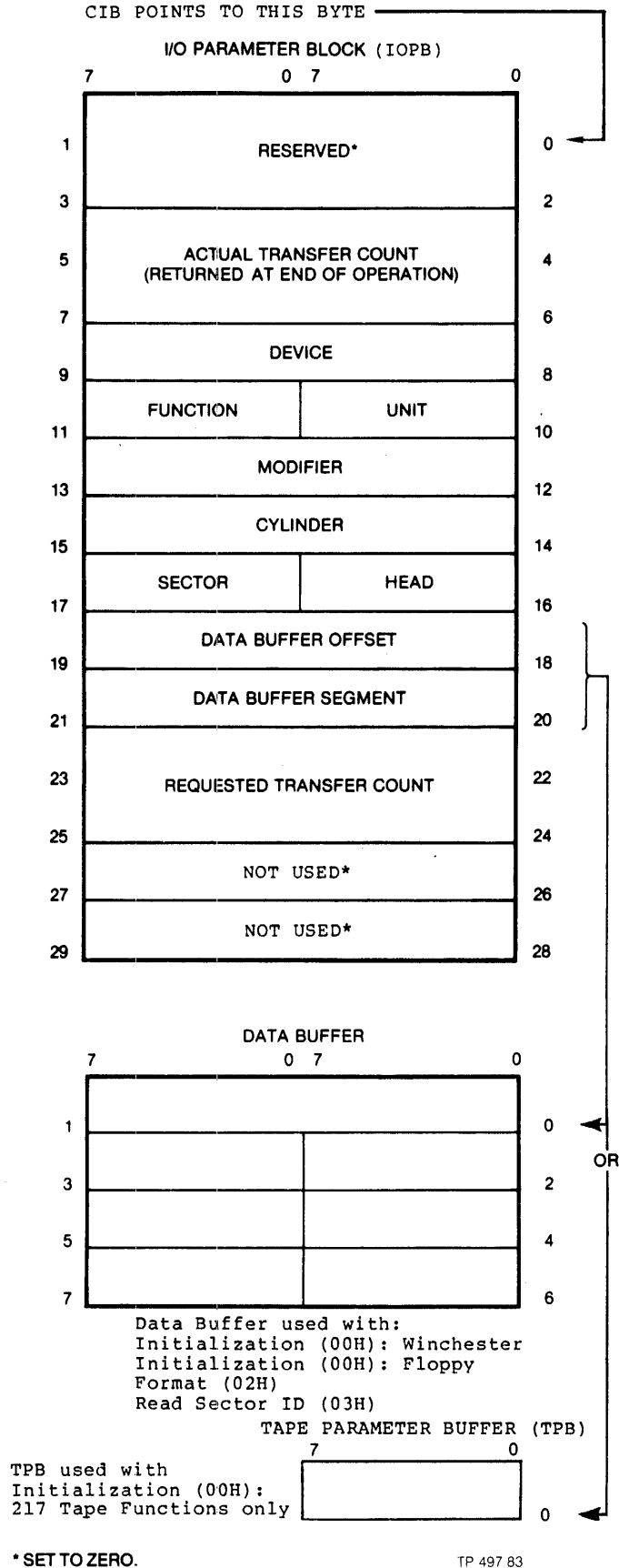


Figure 3-5. Input/Output Parameter Block (IOPB)

Table 3-3. Controller Functions

<u>Figure</u>	<u>Function</u>
3-8.	Initialization (00H): 5 1/4-inch Winchester Disk
3-9.	Initialization (00H): 8-Inch Floppy Disk
3-10.	Initialization (00H): 217 Tape Functions
3-11.	217 Tape: Initialization (10H)
3-12.	217 Tape: Reset (1CH)
3-13.	217 Tape: Rewind (11H)
3-14.	Format (02H)
3-16.	Transfer Status (01H)
3-17.	Diagnostics (0FH)
3-18.	Read Data (04H)
3-19.	Write Data (06H)
3-20.	Read Data Into Controller Buffer (05H)
3-21.	Write Data From Controller Buffer (07H)
3-22.	Read Sector ID (03H)
3-23.	Initiate Track Seek (08H)
3-24.	Buffer I/O (0EH)
3-25.	217 Tape: Transfer Status (01H)
3-26.	217 Tape: Read Status (1EH)
3-27.	217 Tape: Read Data (04H)
3-28.	217 Tape: Write Data (06H)
3-29.	217 Tape: Read/Write Terminate (1FH)
3-30.	217 Tape: Move Forward One File (12H)
3-31.	217 Tape: Move Forward One Record (1AH)
3-32.	217 Tape: Write File Mark (14H)
3-33.	217 Tape: Retension Tape (1DH)
3-34.	217 Tape: Erase (17H)
3-35.	DSD Tape: Reset Drive (80H)
3-36.	DSD Tape: Retension Cycle (84H)
3-37.	DSD Tape: Disk-Image Back-up (81H)
3-38.	DSD Tape: Disk-Image Restore (82H)
3-39.	DSD Tape: Read Tape Status (83H)

- (1) Unit. This field (byte 10), together with the device field, selects the specific drive to be used for the function being requested. Bits 2, 3, 5, 6, and 7 are reserved.

Possible values for the unit field (byte 10) are:

00H: Fixed Volume, Unit 0.  
 01H: Fixed Volume, Unit 1.  
 02H: Fixed Volume, Unit 2.  
 03H: Fixed Volume, Unit 3.  
 10H: Removable Volume, Unit 0.  
 11H: Removable Volume, Unit 1.  
 12H: Removable Volume, Unit 2.  
 13H: Removable Volume, Unit 3.

- (2) Modifier. This field (bytes 12 and 13) contains control flags. The control functions are:

Bit(s)	Function (Enabled when bit = 1)
15-8	For the diagnostic (0FH) function, this byte specifies the test to be executed. <u>For all other functions, this byte must be set to zero.</u>
7	Reserved.
6	For 217 tape function: transfer status (01H) , this bit selects the source of data that the status buffer will contain. There are three choices:  Status of: <ul style="list-style-type: none"> <li>• the last short-term (detailed in 3.6.5) function (modifier bit 6 = 0), or</li> <li>• the last long-term (detailed in 3.6.5) function at the time of the first interrupt (modifier bit 6 = 0), or</li> <li>• current status of the last long-term function (modifier bit 6 = 1).</li> </ul>
5-3	Reserved.
2	Allows deleted data to be accessed with the following functions: <ul style="list-style-type: none"> <li>• read data (04H)</li> <li>• write data (06H)</li> <li>• read data into buffer and verify (05H)</li> <li>• write data from buffer (07H)</li> </ul> bit values: 1 = access deleted data 0 = normal function.
1	Inhibits automatic retries for error recovery.
0	Suppresses generation of an interrupt upon function completion.

- (5) Cylinder. This field (bytes 14 and 15) specifies the starting cylinder (track) number where a read, write, or format function begins. The range of acceptable values depends upon the drive type and drive parameters specified at initialization. The first cylinder number

is always 0. An illegal value causes the selected drive head to go to cylinder 0, and an error to be returned.

- (6) Sector. This field (byte 17) specifies the starting sector number for a disk read or write operation. The range of legal values depends on the drive type and format (number of sectors per track) specified at initialization. The first sector number for a floppy disk is always 1, not 0 as for cylinder and head numbers. The first sector number for a Winchester drive is 0.
- (7) Head. This field (byte 16) specifies the starting head number. The range of legal values depends upon the drive type specified at initialization. Head numbers start at zero. For single-sided floppy disks, the only head number is 0. For double-sided floppy disks, the only values allowed are 0 and 1.
- (8) Data Buffer Address Pointers. These two fields (bytes 18 through 21), depending upon the function to be executed, may point to several different addresses:
- the data buffer
  - the tape parameter buffer
  - other main memory buffer
- (9) Requested Transfer Count. This field (bytes 22 through 25) specifies the number of bytes to be transferred in the process of executing a function. The controller treats the value in this field as a 32-bit positive number. Byte 22 of the IOPB should be written with the least significant byte, and byte 25 the most significant.

The program must read 1 value that the controller writes in the IOPB.

- (1) Actual Transfer Count. This field (bytes 4 through 7) contains the actual transfer count, returned by the controller as a 32-bit positive number. Byte 4 contains the least significant byte, byte seven contains the most significant.

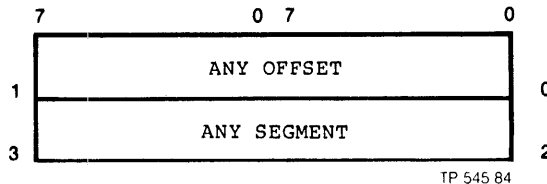
In disk data transfers that occur without error, the actual transfer count will equal the requested transfer count. The controller returns a count of six following a format function and a count of 12 after a status transfer function.

### 3.3.5. Control Block Address Representation

Control block addresses may be represented in two ways. Segmented address representation is compatible with iSBC operation, but is limited to 20 bits. To achieve full 24-bit address compatibility, linear addressing can be specified in the wake-up block. A comparison is shown in Table 3-4.

Table 3-4. Control Block Addressing

In the IOPB block:



Segmented Address:

$$\text{Host Bus Address} = (2^4 * \text{segment}) + \text{offset}$$

Offset:                    byte 1 = 34H    56H = byte 0

Segment:                  byte 3 = 11H    12H = byte 2

As processed to compute host bus address:

Segment x 16:            01H    11H    20H  
(Shift left four bits)

Segment x 16:            01H    11H    20H  
Plus Offset                    34H    56H

-----  
Host Bus                    01H    45H    76H  
Address                    (20 bits)

Linear Address:

$$\text{Host Bus Address} = 24 \text{ least significant bits of:} \\ (2^{16} * \text{segment}) + \text{offset}$$

Offset:                    byte 1 = 34H    56H = byte 0

Segment:                  byte 3 = 11H    12H = byte 2

Host Bus Address:            12H    34H    56H  
(24 bits)

(Most significant byte of segment is ignored)

Segmented address representation is shown in figures throughout the remainder of this manual. Those selecting 24-bit linear addressing must interpret the figures accordingly.

Segmented addressing is one method of specifying an address in two parts. These two parts are called a segment and an offset.

To turn a particular segmented representation into its corresponding 20-bit host bus address, the controller multiplies the segment by 16 (shifts it left four bits), and adds the offset to the result.

### 3.4. Controller/Program Handshaking

Handshaking is used to regulate the transfer of data. Regulation may be done with or without interrupts.

#### 3.4.1. Handshaking with Interrupts

After controller operation has been initiated, the controller can assert an interrupt (if enabled: detailed in IOPB, paragraph 3.3.4) to alert the program to a change in the status of the last function requested. The controller asserts an interrupt on one of host bus interrupt lines INT0/ through INT7/ (detailed in section 2.2.5 and table 2-6). Three events that can cause the controller to assert an interrupt are:

- Completion of any controller function, or
- start of a long-term controller function (detailed in 3.6.1), or
- a media change.

Once an interrupt has been asserted, it can be removed by:

- A clear interrupt/remove reset (00H) program command to the controller, or
- a power-on reset, or
- assertion of the host bus INIT/ signal.

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Note

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The interrupt asserted at the completion of a short-term function and the interrupt asserted at the start of a long-term function may be disabled by setting bit 0 of the IOPB modifier field to zero (detailed in IOPB, 3.3.4). Interrupts asserted by the completion of a long-term function or by a media change may NOT be disabled.

---

#### 3.4.2. Handshaking Without Interrupts (Polling)

The CIB (detailed in 3.3.3) can be used, without reference to interrupts, to regulate the transfer of data between main memory and the controller. The CIB contains both the status semaphore and the operation status byte. The status semaphore is used by the controller to indicate the presence of current status information in the operation status byte, and by the program to acknowledge transfer of the contents of the operation status byte.

When the controller has status information to post, it examines the status semaphore to determine if the program has transferred the last information posted there. If the controller finds a value of zero in the status semaphore, it assumes that the program has transferred the last status posted, and written zero in the field. The controller then posts the new status information in the operation status byte, and writes a non-zero value in the status semaphore.

The program must follow the reverse protocol. When the program finds a non-zero value in the status semaphore, it must assume that there is new status information in the operation status byte. After the program transfers the contents of the operation status byte, the transfer must be acknowledged by writing a value of zero in the status semaphore.

#### 3.4.3. Status Processing

The controller may notify the program that status has been generated by asserting an interrupt, or the program may detect that status has been generated by polling the status semaphore. The program must decide what action to take based on whether or not the status indicates an error.

The controller uses the operation status byte of the CIB (detailed in table 3-2) to indicate that an error occurred in the execution of a function. The controller does this by setting the summary error bit (bit 7 of the operation status byte) to one.

Since status is cleared during the execution of each function except transfer status (IOPB function field = 01H), the program should use this function (detailed in section 3.6) to retrieve status immediately following the completion any other function.

The transfer status (01H) function may transfer data that reports an error. Errors generally fall into three categories:

(1) Operational errors: These can be caused by the program or the operator. They include:

- Illegal sector
- Invalid sector length
- Write protect errors
- Others. Detailed in:

Table 3-7: Status Buffer Definitions (Excluding Tape Functions)

Table 3-8: Extended Status Buffer Definitions (Including DSD Tape Functions)

Table 3-10: 217 Tape Function Status Buffer Definitions

Table 3-11: DSD Tape Function Status Buffer Definitions

(1) Hard errors: Errors caused by flaws in the media.

(2) Soft errors. Those that occur during read functions.

The controller handles most errors without program intervention. If automatic retries are enabled (IOPB modifier field bit 1 = 0: detailed in IOPB, 3.3.4), the controller attempts to recover from errors by simple repetition. Retry information is included in the status: see the status buffer definition tables listed above.

Error correction is attempted during Winchester disk functions using ECC. If, during automatic re-tries, the same error code occurs twice, a correction is performed on error bursts of 11 bits or less. There is no correction attempted on longer error bursts.





### 3.5. Operation Summary

To initiate controller operation, the program must issue a series of commands followed by a series of controller functions (see Figure 3-6):

- (1) Set up the WUB, CCB, and CIB. Set the busy 1 field in the CCB to FFH.
- (2) Issue a reset controller (02H) program command.
- (3) Issue a clear interrupt/remove reset (00H) command to remove the reset condition.
- (4) Issue a start (01H) command. This first start command reads through the chain of control blocks, ending with the CIB. When this first start (01H) command is finished, the controller clears the busy 1 field, and has the address of the IOPB.
- (5) The controller is then ready for initialize (00H) functions for all drives.

After the program builds the IOPB, with the required data in the appropriate fields, another start (01H) command causes the controller to access the IOPB and act upon the data it finds there.

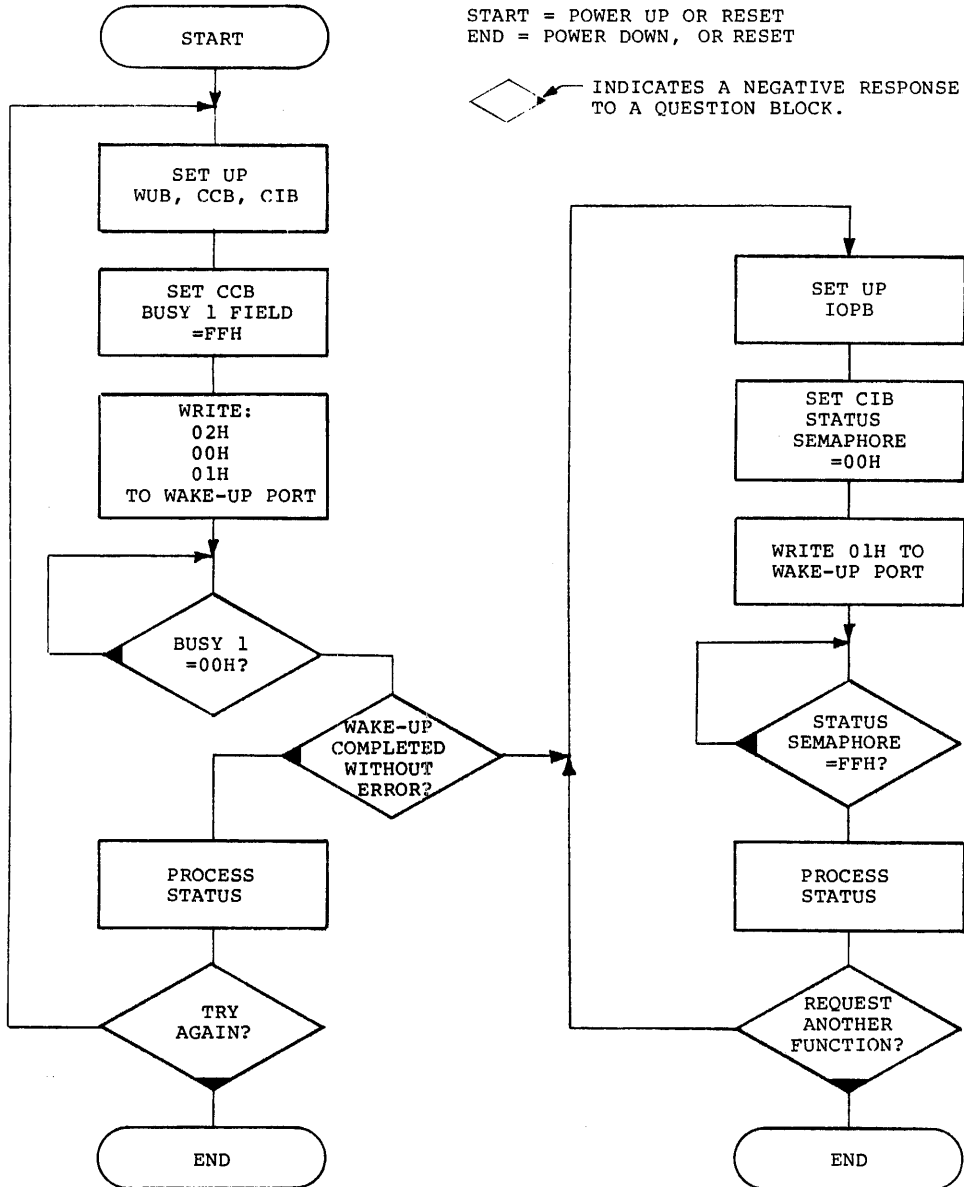
The first controller function must be initialize (00H). This function must be requested for each drive present, to inform the controller of the hardware configuration.

Before any other 217 tape functions are requested, tape initialize (10H) is required. For each tape drive present, tape reset (1CH) and tape rewind (11H) are also required. After any DSD tape functions, these initialization functions must be repeated before requesting any other 217 tape functions.

Before any other DSD tape functions are requested, reset tape drive (80H) is required. After any 217 tape functions, reset tape drive (80H) must be repeated before requesting other DSD tape functions.

When the controller completes a function, if it finds that the program has set the status semaphore to zero, it writes a non-zero value in the status semaphore, and posts status in the operation status-byte of the CIB.

If the program is interrupt-driven, the interrupt generated at the completion of the function may be used as the signal to examine the status semaphore and the operation status-byte in the CIB.



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Figure 3-6. Operation Summary

### 3.6. Controller Functions

A controller function is a task that the controller must carry out, in response to a request by the program. There are 28 controller functions. It must be remembered that the 6214 has no tape functions. The controller functions are presented in the following order:

- Those needed to initiate operation (including 217 tape functions):
  - Initialization (00H): 5 1/4 Winchester Disk
  - Initialization (00H): 8-Inch Floppy Disk
  - Initialization (00H): 217 Tape Functions
  - 217 Tape: Initialization (10H)
  - 217 Tape: Reset (1CH)
  - 217 Tape: Rewind (11H)
- Utility Functions (not including 217 tape functions):
  - Format (02H)
  - Transfer Status (01H)
  - Diagnostics (0FH)
- Disk Drive Read and Write Functions:
  - Read Data (04H)
  - Write Data (06H)
  - Read Data Into Controller Buffer and Verify (05H)
  - Write Data From Controller Buffer (07H)
  - Read Sector ID (03H)
  - Initiate Track Seek (08H)
  - Buffer I/O (0EH)

- 217 Tape Read and Write Functions:
  - Read Data (04H)
  - Write Data (06H)
  - 217 Read/Write Terminate (1FH)
  - Move Forward One Record (1AH)
  - Move Forward One File (12H)
  - Write File Mark (14H)
- 217 Tape Utility Functions:
  - Read Tape Status (1EH)
  - Transfer Status (01H)
  - Retension Tape (1DH)
  - Erase Tape (17H)
- DSD Mirror-Image Tape Functions:
  - Reset Tape Drive (80H)
  - Disk-Image Back-up (81H)
  - Disk-Image Restore (82H)
  - Read Tape Status (83H)
  - Tape Retension Cycle (84H)

### 3.6.1. Short-Term and Long-Term Controller Functions

There are two kinds of controller functions: short-term and long-term. Short-term functions generate one interrupt when complete. This interrupt can be disabled by setting bit 0 of the IOPB modifier field to zero (detailed in IOPB, 3.3.4).

When a short-term function is complete, the controller sets the status semaphore and asserts an interrupt (if enabled). The status available must be processed before any other functions can be requested.

Long-term functions assert two interrupts in the course of execution. The first interrupt can be disabled by setting bit 0 of the IOPB modifier field to zero. The second interrupt cannot be disabled. Table 3-5 is a list of the long-term controller functions.

Table 3-5. Long-Term Controller Functions

---

Initiate Track Seek (08H)  
 217 Tape: Move Forward One File (12H)  
 217 Tape: Retension (1DH)  
 217 Tape: Rewind (11H)  
 217 Tape: Erase (17H)

(All other controller functions are short-term)

---

A long-term function, up to the point of the first interrupt, is essentially the same as a short-term function:

- Up to the point of the first interrupt, the long-term function being processed is the only function being executed.
- The status available at the point of the first interrupt must be processed before any other functions can be requested.

Any error detected at that point will be reflected in the status available when the controller sets the status semaphore and asserts the first interrupt (if enabled). If no error condition was detected, the status information will reflect this.

The program must process the status available when the controller sets the status semaphore and/or asserts the first interrupt before any other controller activity can take place. If the status shows an error, the long-term function is over: no second interrupt will be asserted.

Errors are detected and reported at the time of the first interrupt. There are no errors reported at the time of the second interrupt.

If the status at the time of the first interrupt shows no errors, the long-term function continues. However, once the program clears the status semaphore, the controller can process other functions.

Any other function requested must be for a different drive. If the pending long-term function is 217 tape, any other function requested must be nontape.

If, after the first interrupt status of a long-term function has been processed, the program requests a short-term function, the controller will execute it completely before asserting the second interrupt of the pending long-term function. If the new function is long-term, the controller will process it to the point of the first interrupt, just like a short-term function, before asserting the second interrupt of the pending long-term function.

Since any short-term function requested after the first interrupt of a long-term function must be completely executed including status processing by the program, before the controller will assert the second interrupt of the pending long-term function, there is no possibility of status from one function disrupting the other.

A second long-term function requested after the first interrupt of a previous long-term function will be handled up to the point of its first interrupt as if it were a short-term function.





### 3.6.2. Initialize (00H)

The initialize function, with complete drive information, must be requested for each drive in the system following any:

- power-on,
- host bus INIT/, or
- reset controller (02H) program command.

Other functions, requested for drives not initialized, will not be executed and an error will be returned.

The program must use the initialize function to transfer drive parameters to the controller. This information must be consistent with the format of the drive (see format (02H) function).

#### Winchester Disk Parameters:

In the following discussion, a head is assumed to be associated with a single disk surface. Each surface can have up to 4096 tracks (circular data paths numbered 0 through 4095). The set of tracks on multiple recording surfaces at a given head position is referred to as a cylinder (see Figure 3-7). A drive that has 4096 tracks per surface also has 4096 cylinders.

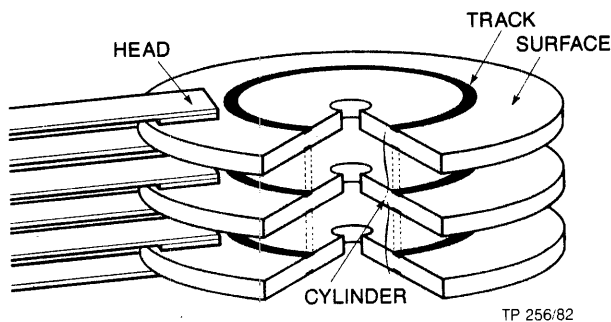


Figure 3-7. Winchester Disk Organization

5 1/4-INCH WINCHESTER

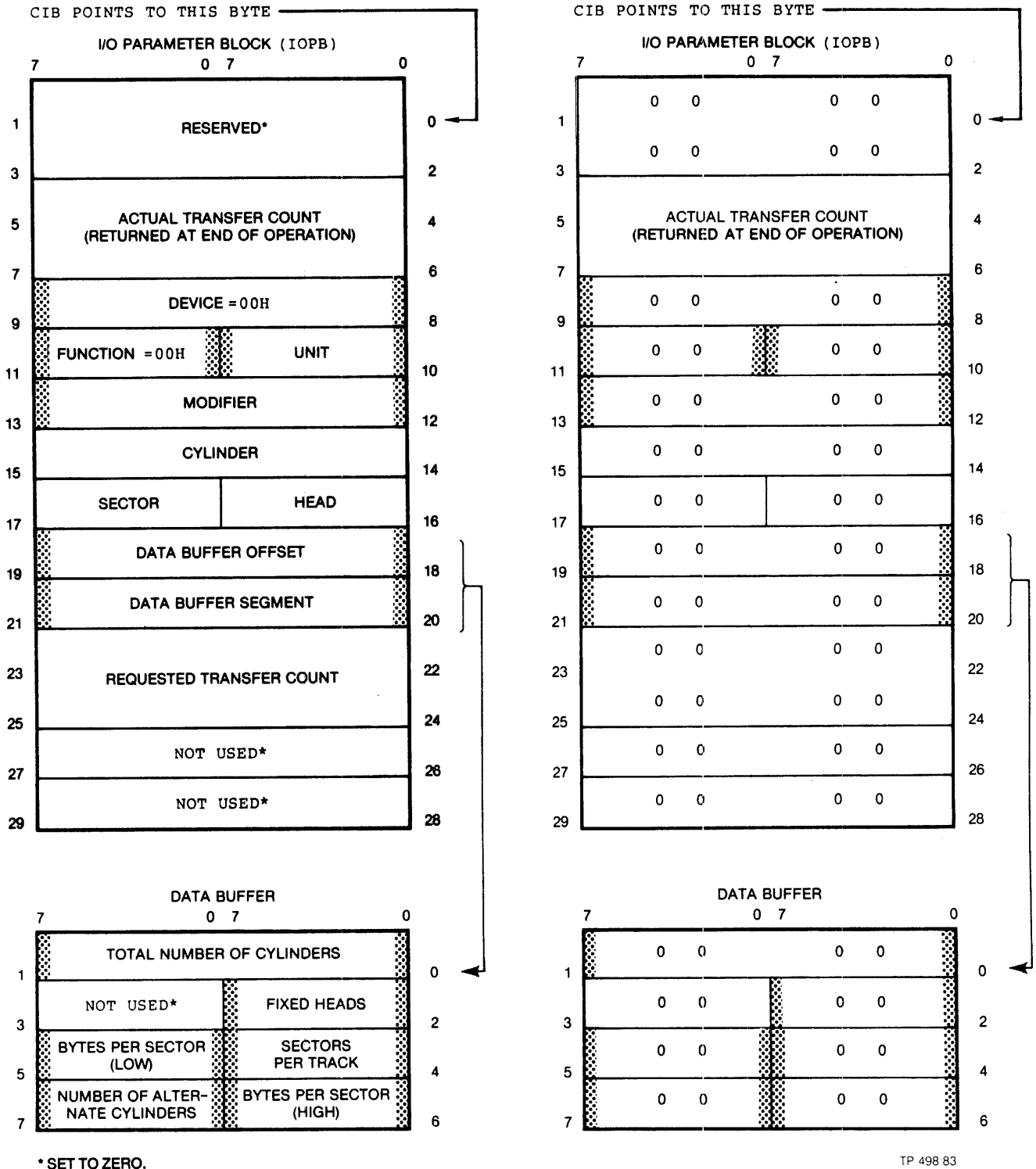


Figure 3-8. Initialization (00H): 5 1/4-inch Winchester Disk

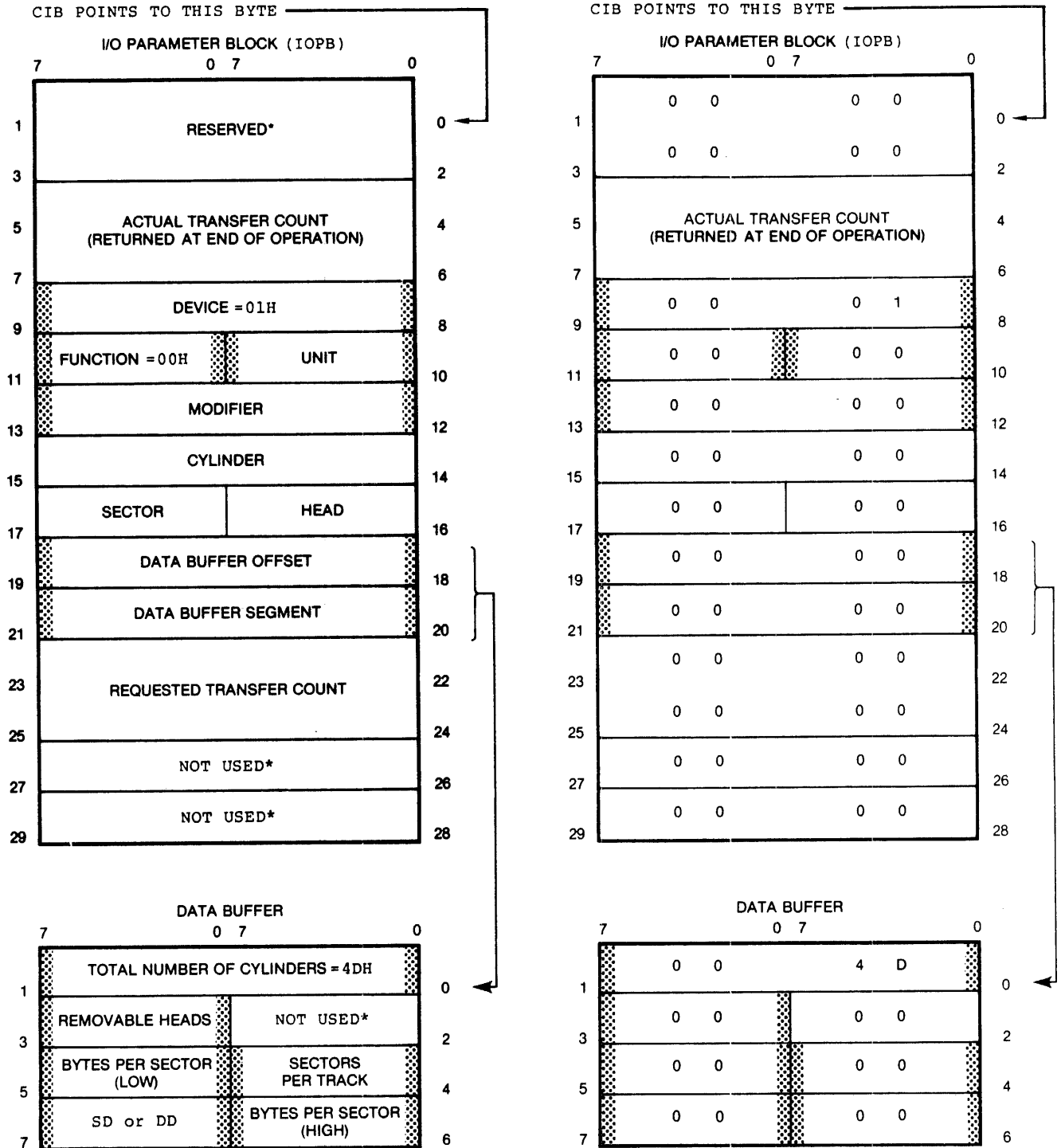
The fields in the IOPB data buffer have the following meaning when a Winchester disk is initialized:

- Number of Cylinders: This two-byte field specifies the number of cylinders available on a disk drive. The value for this field must be obtained from the disk drive manual.

This field can be set to zero to cancel a previous initialization and remove a drive from use.

- Fixed Heads: This field specifies the number of fixed heads on a drive. For example, an ST412 Winchester drive has four.
- Sectors per Track: This field specifies the number of sectors per track for each drive. The value for this field depends on sector size. The possible values are: 9, 17, 31, and 54.
- Bytes per Sector: This two-byte field specifies the number of data-bytes in a disk sector. The sector length, specified each time the initialize function is requested, must match the disk format. The possible values are 128, 256, 512, or 1024.
- Number of Alternate Cylinders: For a Winchester drive, this field specifies the number of cylinders reserved as alternates for defective tracks. The number of alternate cylinders, specified each time the initialize function is requested, must match the disk format.

8-INCH FLOPPY



\* SET TO ZERO.

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Figure 3-9. Initialization (00H): 8-Inch Floppy Disk

### Floppy Disk Parameters:

The floppy disk drives use standard IBM single- or double-sided media. The formats supported are single-density (128 to 1024 data-bytes per sector), and double-density (256 to 1024 data-bytes per sector).

The program must write the floppy disk drive information needed for each initialize function in the data buffer (see Figure 3-9). The fields in the IOPB data buffer have the following meaning when a floppy disk is initialized:

- Number of Cylinders: This two-byte field specifies the number of cylinders available on a disk drive. The value for an 8" floppy is always 77 (4DH).

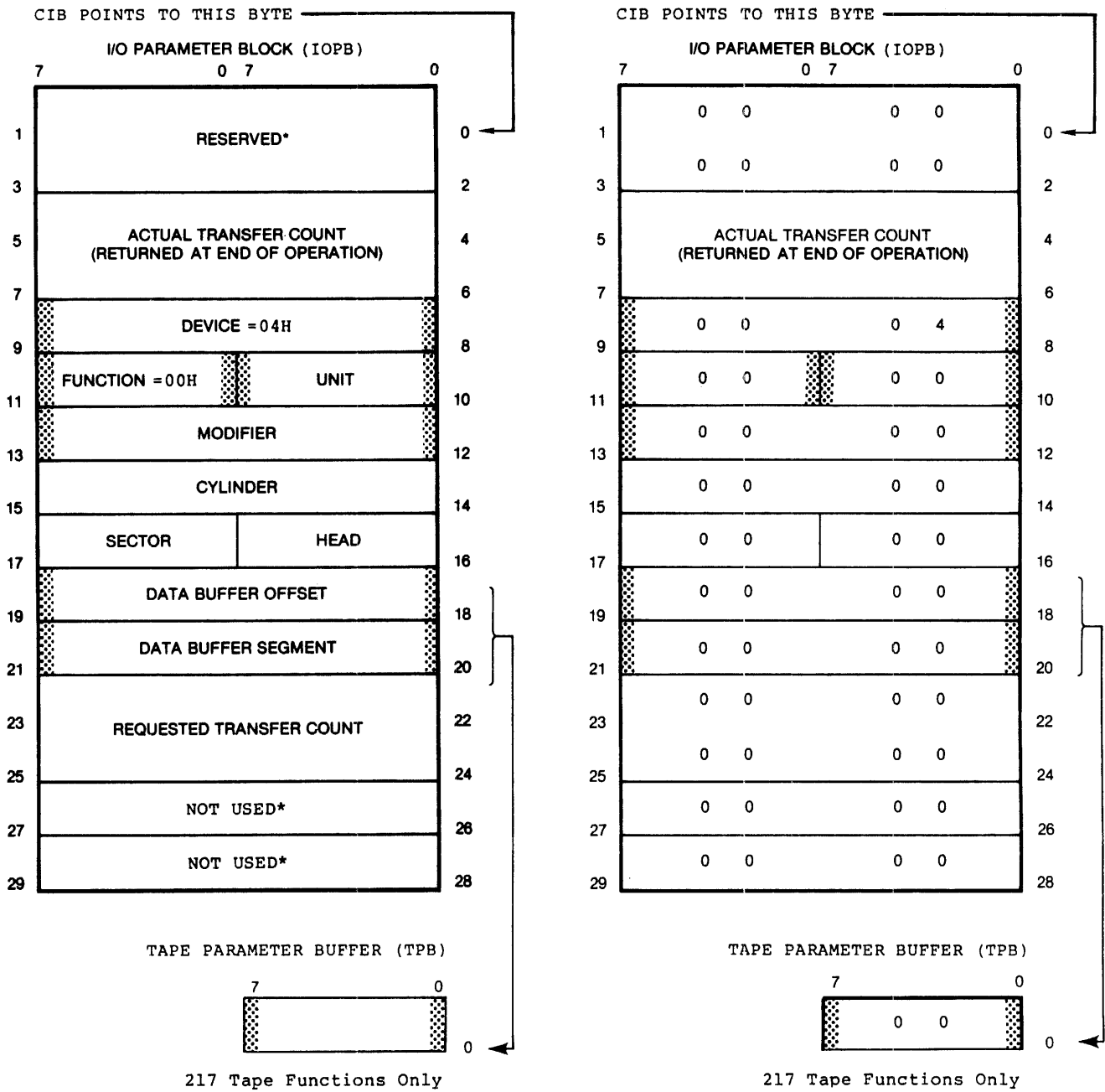
This field can be set to zero to cancel a previous initialization and remove a drive from use.

- Removable Heads: This field specifies the number of heads on a floppy disk drive. For a single-sided floppy drive, the value is one. For a double-sided drive, the value is two.
- Sectors per Track: This field specifies the number of sectors per track for each drive. The value for this field depends on:
  - single-density or double-density
  - bytes per sector.

The possible values are: 4, 8, 15, and 26.

- Bytes per Sector: This two-byte field specifies the number of data-bytes in a disk sector. The sector length, specified each time the initialize function is requested, must match the disk format. The possible values are 128, 256, 512, or 1024.
- Single Density or Double Density Encoding: For a floppy drive, this field specifies the data encoding scheme to be used: 00H for FM, single-density; and 01H for MFM, double-density.

STREAMING TAPE DRIVE: 217 TAPE FUNCTIONS



\* SET TO ZERO.

Figure 3-10. Initialization (00H): 217 Tape Functions

### Streaming Tape Parameters:

Data is recorded on the streaming tape drives in 512-byte blocks (also called records). The track selection is transparent to the program, and is accomplished by the streaming tape drive controller.

Initialization of tape drives is not required to request DSD tape functions. For the DSD tape functions, "present" is the default condition of tape drive 0. Tape drive reset (80H) is required for drive 0, before requesting any DSD tape functions.

For the 217 tape functions, initialize informs the controller that tape drives are present. For 217 functions, "not present" is the default for all tape drives. For each tape drive present, initialize must be followed by the tape initialization (10H) function.

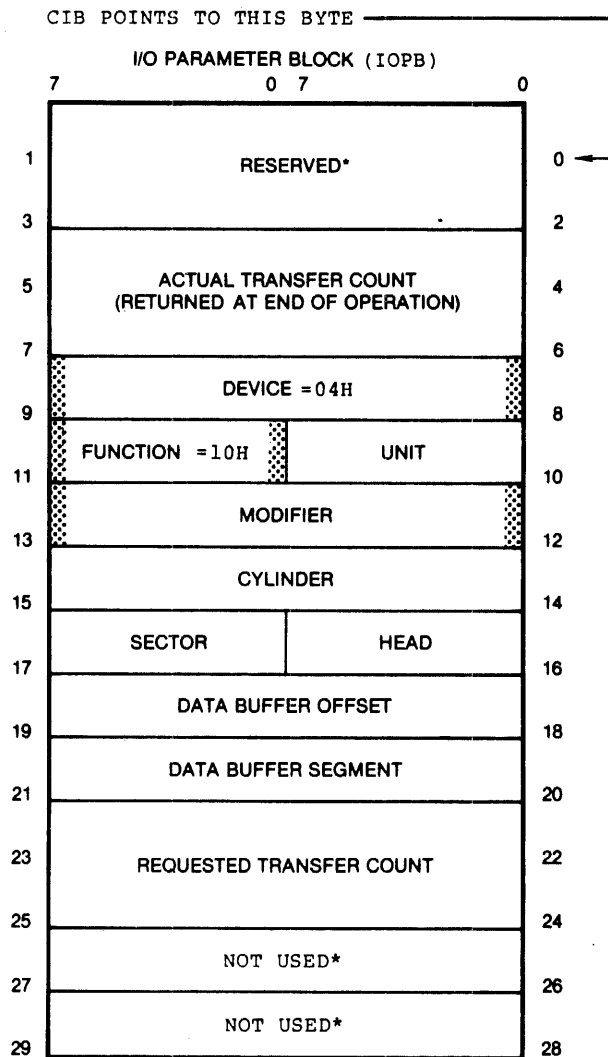
The tape drive information transferred to the controller by this function is stored in an extension to the IOPB called the tape parameter buffer (TPB). The data buffer offset and segment stored in the IOPB are used to address the TPB (see Figure 3-10).

Only bit 0 is used in the TPB. Bits 1 through 7 are not looked at by the controller. PRESENT (bit 0 = 1) must be indicated in the TPB for each drive installed. NOT PRESENT (bit 0 = 0) is the default for all drives.

3.6.3. 217 Tape: Initialization (10H)

217 tape initialization (see Figure 3-11) is required by the streaming tape drive controller in preparation for 217 tape functions.

This function must be invoked immediately after an initialization (00H): 217 tape function, and must be followed by a tape reset (1CH) function. If the tape drive controller cannot complete the 217 tape initialization function, bit 4 of byte 0 in the error status buffer is set.



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Figure 3-11. 217 Tape: Initialization (10H)



### 3.6.4. 217 Tape: Reset (1CH)

217 tape reset (see Figure 3-12) invokes a tape drive reset procedure. This function must follow an initialization (10H): 217 tape function. This function must be followed by a 217 rewind tape (11H) function for each streaming tape drive present.

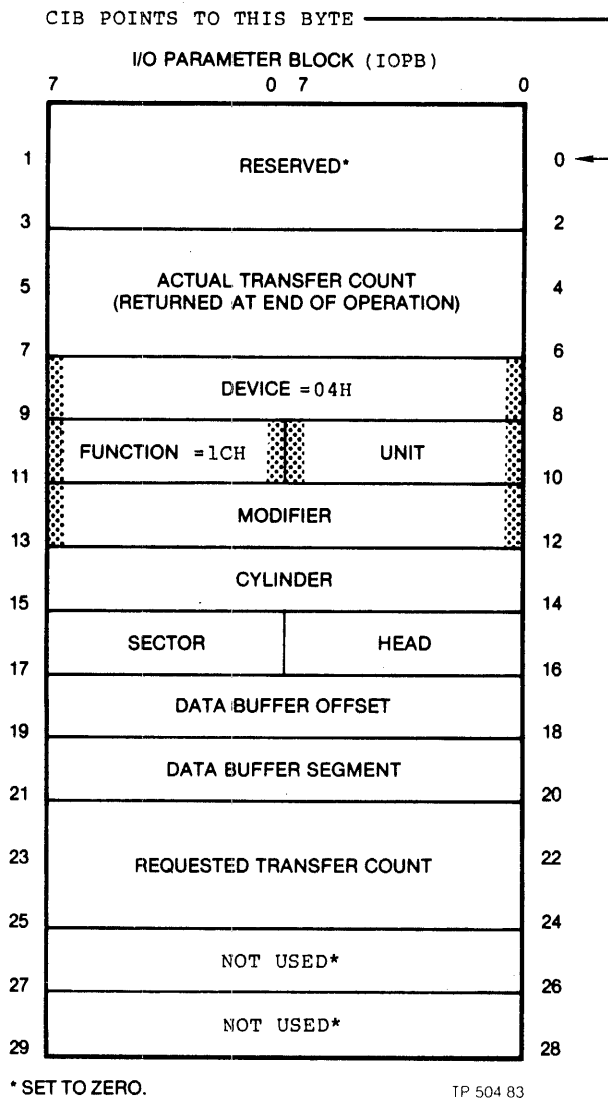


Figure 3-12. 217 Tape: Reset (1CH)

3.6.5. 217 Tape: Rewind (11H)

217 tape rewind (see Figure 3-13) is a long-term function used to place the tape in a known position. This is done by rewinding the tape to BOT and setting the BOT bit in the status buffer.

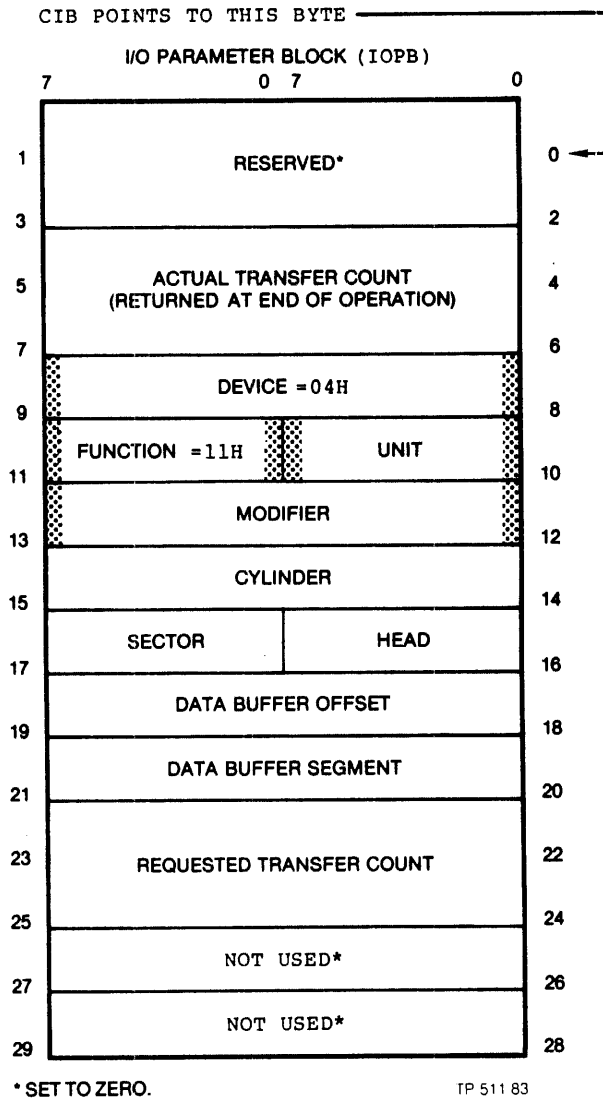


Figure 3-13. 217 Tape: Rewind (11H)

### 3.6.6. Format (02H)

In order for the controller to use a disk drive, the disk must be formatted to the specifications used by the controller. The program must accomplish this with the format function.

The program uses the format function for three operations:

- To format a new disk in preparation for its first use.
- To reformat a disk.
- To format a track on a Winchester drive as defective.

Formatting is accomplished by designating the use of each track and then writing necessary information on the track. A track may be designated as:

- normal data: data buffer  
byte 0 = 00H
- alternate: -for Winchester drives only- data buffer  
byte 0 = 40H
- defective: -for Winchester drives only- data buffer  
byte 0 = 80H

The information written on the disk by the format function is:

- sector ID field (also called sector header)
- data fields (written with a 4-byte user pattern)
- gaps between data fields

When formatting or reformatting a disk, the program must request a format function for each track of each drive. When a track on a Winchester drive is being formatted as defective, only that track need be accessed, if alternate tracks are available. If there are no alternate tracks available, a data track must be reformatted as an alternate.

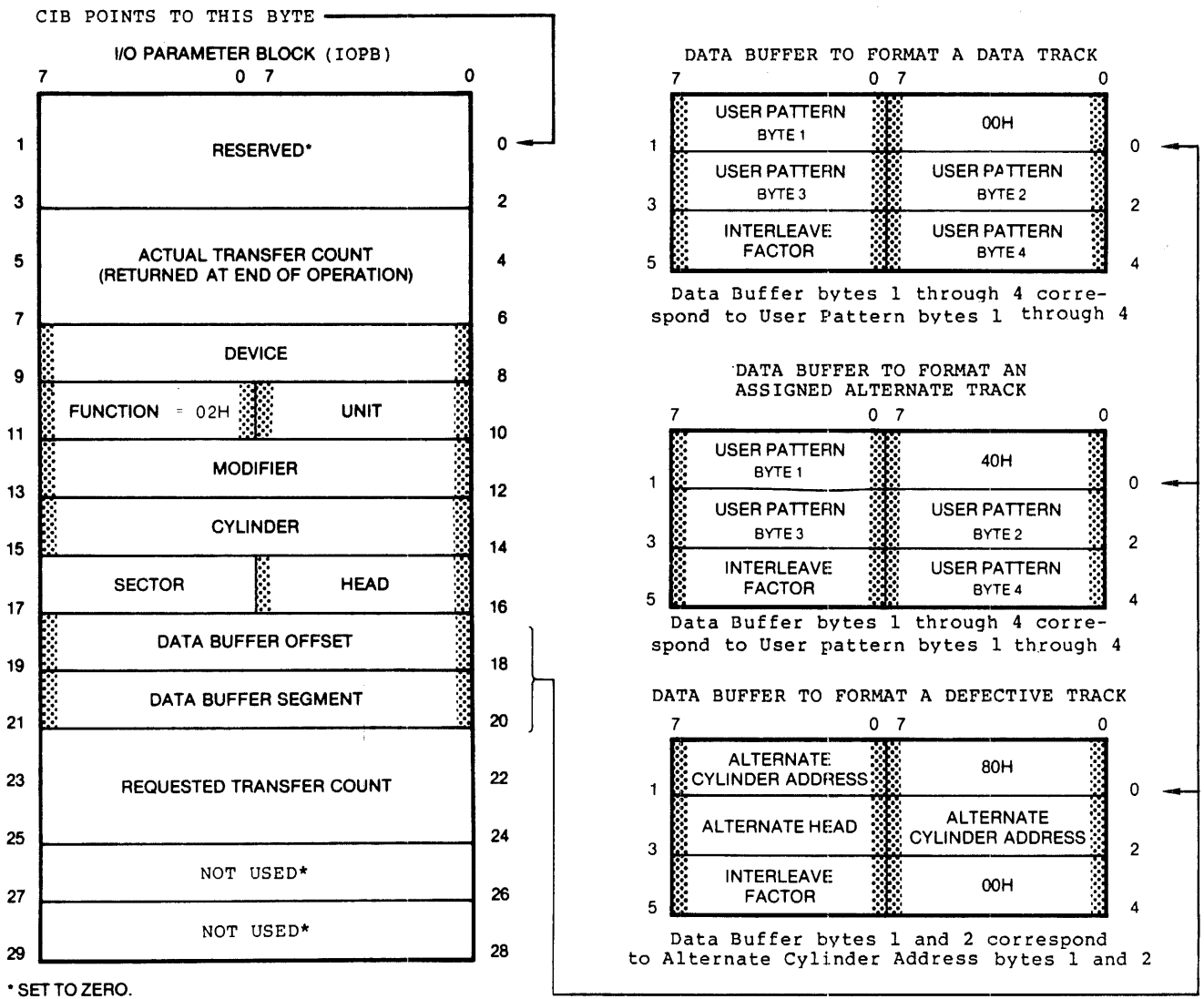


Figure 3-14. Format (02H)

To request a format function, the program builds the IOPB and the 6-byte data buffer in main memory.

- The data buffer specifies:
  - track designation:
    - data: data buffer byte 0 = 00H
    - alternate: -for Winchester drives only-  
data buffer byte 0 = 40H
    - defective: - for Winchesters drives only-  
data buffer byte 0 = 80H
  - either:
    - user pattern (four bytes)
  - or
    - Alternate cylinder address (two bytes) and  
alternate head (one byte).
  - interleave factor

Each Winchester disk surface should be divided into two areas:

- data tracks, and
- alternate tracks.

Two percent is usually an adequate allocation for alternate tracks; however, consult the disk manufacturer's recommendation. Alternates are usually located on the inner tracks of the disk.

-----  
Note  
 -----

In order to reserve the last track at head 0 for the diagnostic program, it must be formatted as a data track.  
 -----

The current state-of-the-art in the production of Winchester recording media makes it impossible to guarantee a flawless recording surface. A certain number of disk defects are expected. Some defects may be present on a new disk, and others may develop with use.

When it has been determined that a defect exists on a track, format the track as defective. The address of the alternate track must be written as the user pattern in the data sectors of the defective track.

When a track that has been formatted as defective is accessed, the controller obtains the address of the assigned alternate track from any data field in the track that remains readable. The controller uses the assigned alternate in place of the defective track. The substitute-use of an assigned alternate track for a track that has been formatted as defective is automatic and transparent to the program.

An alternate track that becomes defective must be removed from service. If a previously defective track points to it, that previously defective track must be reformatted to point to another alternate. A defective alternate track cannot point to another alternate track.

The availability of alternate tracks can be determined by requesting a read ID (03H) function to each track, and decoding the flags posted in byte four of the main memory data buffer.

If a Winchester disk is reformatted, care must be taken to format as defective all tracks known to have defects. The defective tracks should be known before reformatting begins.

The controller generates the format of the sector identification block and the error checking fields of each sector of the disk, one track at a time. Table 3-5 and Figure 3-14 illustrate how the controller organizes this information.

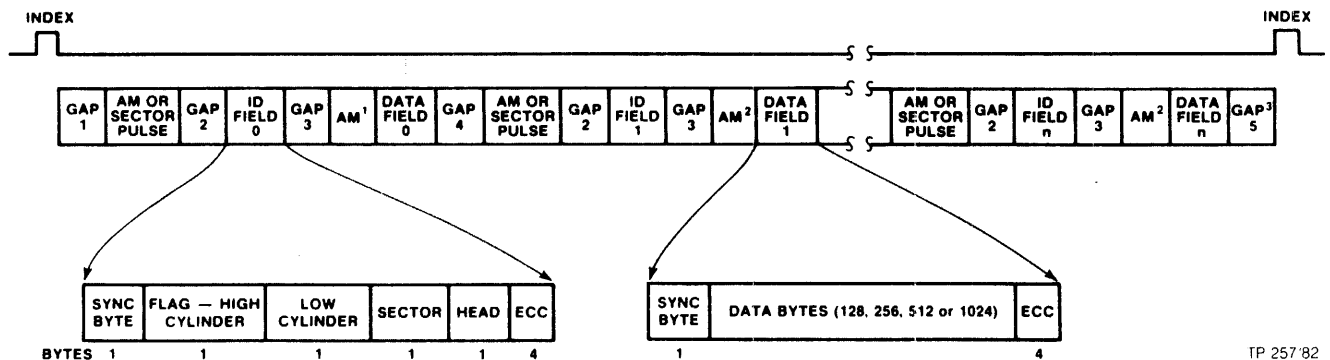


Figure 3-15. Winchester Sector Data Format

Table 3-6. Controller Generated Disk Formatting Data

		physical index													
5,208-bytes/track		G1	P1	IAM	G2	P2	ID	G3	P3	DDAM	DATA	G4	G5		
Single-Density 8" Floppy	Sectors/ Track	Bytes/ Sector	FF	00	FC/DC	FF	00	ID	FF	00	FB/C7 F8/C7	Bytes/ Field	FF	FF	
IAM = FC/D7	26	128	40	6	1	26	6	7	11	6	1	130	27	247	
IDAM = FE/C7	15	256	40	6	1	26	6	7	11	6	1	258	42	170	
DAM = FB/C7	8	512	40	6	1	26	6	7	11	6	1	514	58	311	
DDAM = F8/C7	4	1024	40	6	1	26	6	7	11	6	1	1026	170	227	
Repeated															
		physical index													
10,416-bytes/track		G1	P1	IAM	G2	P2	ID	G3	P3	DDAM	DATA	G4	G5		
Double-Density 8" Floppy	Sectors/ Track	Bytes/ Sector	4E	00	FC/DC	4E	00	ID	4E	00	FB/C7 F8/C7	Bytes/ Field	4E	4E	
IDAM = 3(A1/0A);FE	26	256	80	12	4	50	12	10	22	12	4	258	54	598	
DAM = 3(A1/0A);FB	15	512	80	12	4	50	12	10	22	12	4	514	84	400	
DDAM = 3(A1/0A);F8	8	1024	80	12	4	50	12	10	22	12	4	1026	116	654	
Repeated															
		physical index													
10,416-bytes/track		G1	P1	IAM	G2	P2	ID	G3	P3	DDAM	DATA	G4	G5		
5.25" Winchester	Sectors/ Track	Bytes/ Sector				4E	00	ID	4E	00	FB/C7 F8/C7	Bytes/ Field	4E	4E	
IAM = C2/14;FC	54	128				4	12	10	3	6	2	132	21	368	
IDAM = A1/0A;FE	31	256				4	12	10	3	6	2	260	30	399	
DAM = A1/0A;FB	17	512				4	12	10	3	6	2	516	44	331	
DDAM = A1/0A;F8	9	1024				4	12	10	3	6	2	1028	61	314	
Repeated															

The user pattern is a four-byte sequence repeated throughout all of the data fields. The pattern is written to the drive in numerical order: user pattern one first and user pattern four last. The characters chosen for the pattern have no significance, except when formatting a defective track on a Winchester drive, where the user pattern is the address of the alternate track.

The interleave factor controls the relationship between the numerical order of sectors in a track, and the physical sequence in which the sectors exist on the track.

An interleave factor of one specifies that sectors are to be written in numerical order around the track: Index, Sector 1, Sector 2, etc. This allows the fastest data throughput, and is called noninterleaved operation, since the numerical order and the physical sequence are the same.

Values greater than one may be used to introduce delay between sector accesses. This delay occurs because with values greater than one, the sectors are not physically in numerical order.

Using interleave values greater than one is called interleaved operation. The interleave factor is the minimum number of sector intervals between sectors that are in numerical, but not physical, order.

After a sector has been read, the disk rotates until the next-numbered sector can be accessed. The greater the interleave factor, the farther away the next-numbered sector is, and therefore, the longer the disk must rotate to access it.

The delay introduced by interleaved operation may be necessary if the disk drives are assigned a low bus priority, or if slow main memories are used.

Sector 1 is always physically written immediately after the track index. Table 3-6 assumes eight sectors per track and 1024-bytes per sector, on a single-density floppy disk.

Table 3-7. Interleave Factor

Factor	Order From Index
1	1 2 3 4 5 6 7 8
2	1 5 2 6 3 7 4 8
3	1 4 7 2 5 8 3 6
4	1 3 5 7 2 4 6 8





3.6.7. Transfer Status (01H)

This function (see Figure 3-16) transfers the contents of the on-board status buffer in controller memory to a status buffer in main memory. For disk drives, this function is used by itself to transfer status.

For 217 tape function status, see sections 3.5.14 and 3.5.15. For DSD tape function status, see section 3.5.27.

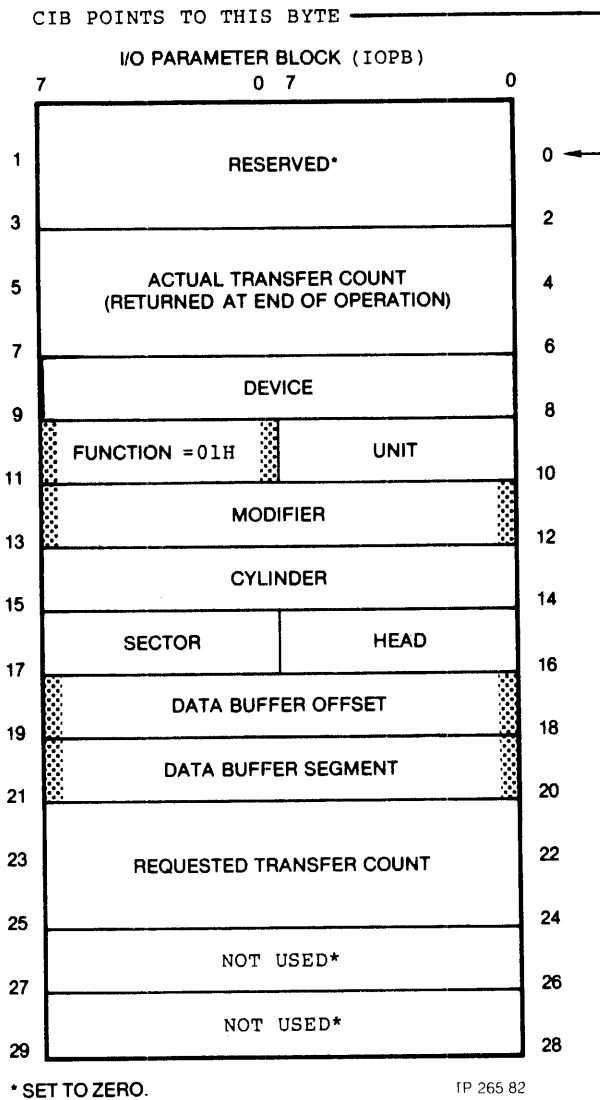


Figure 3-16. Transfer Status (01H)

After each function, the program should examine the summary error bit in the operation status byte of the CIB to obtain function execution status. If detailed status information is required, the transfer status (01H) function should be requested immediately, because the status buffer on-board the controller is cleared during the execution of all other functions.

Executing the transfer status (01H) function causes the current contents of the controller status buffer to be written to the main memory data buffer addressed by the data buffer offset and segment fields of the IOPB.

If extended status was not enabled in the WUB (see paragraph 3.3.1), the status is reported in 12 bytes. Table 3-8 defines the 12 bytes of status data transferred to main memory by the transfer status (01H) function. Bytes 0, 1, and 2 of the status buffer contain the hard and soft error bits. These bits are defined in detail.

If extended status was enabled in the WUB, the status is reported in 13 bytes. Extended status reporting is enabled by setting bit 2 in the extension byte of the WUB at power-up, or following any reset.

-----  
Note  
 -----

Extended status reporting is enabled by a value that the program must write in the WUB (see paragraph 3.3.1). In order to use extended status reporting, the enabling value must be in the WUB when the controller accesses it in response to the first start (01H) program command following a reset.

Once the WUB has been accessed (in response to the first start (01H) program command), extended reporting cannot be enabled without resetting the controller and drives.  
 -----

The thirteenth byte contains the extended error status expressed as a hexadecimal value. Table 3-8 defines the extended error status byte. These status codes are also reported by the blinking patterns of LED CR1 (ERR).

Table 3-8. Status Buffer Definitions for Nontape Functions

<u>Byte #</u>	<u>Definition</u>
0	Hard Error Byte
Bit: 0, 1, 2	<u>Reserved.</u>
3	<u>RAM Error:</u> Controller RAM error detected.
4	<u>ROM Error:</u> Controller ROM error detected.
5	<u>Seek in Progress:</u> Indicates that a seek was already in progress when another disk operation was requested.
6	<u>Illegal Format type:</u> Both alternate track and defective alternate track indications set, signalling either an illegal attempt to create an alternate track for a defective track already formatted as an alternate, or an attempt to access an unassigned alternate track.
7	<u>End of Media:</u> End of media encountered before requested transfer count exhausted.
1	Hard Error Byte
Bit: 8	<u>Illegal Sector Size:</u> Sector size read from sector ID conflicts with sector size specified during initialization.
9	<u>Diagnostic Fault:</u> Micro-diagnostic fault indicated.
A	<u>No Index:</u> Controller did not detect index pulse.
B	<u>Invalid Function:</u> Invalid function code detected.
C	<u>Sector Not Found:</u> Desired sector could not be found on selected track.
D	<u>Invalid Address:</u> Invalid address requested.
E	<u>Selected Unit Not Ready:</u> Selected unit is not ready or not responding to unit connect request.
F	<u>Write Protection Fault:</u> Attempt made to write to a write-protected unit.

(Continued)

Table 3-8. Status Buffer Definitions for Nontape Functions  
 -----(Continued)-----

2	Soft Error Byte
Bit: 0	<u>Reserved.</u>
1	<u>Reserved.</u>
2	<u>Reserved.</u>
3	<u>Data Field ECC Error:</u> Error detected in data field of a sector. If byte 1, bit 6 in the CIB (operation status byte) is set, then error is hard and uncorrectable. If bit 6 is not set, error is not set, error is soft and correctable.
4	<u>ID Field ECC Error:</u> Error detected in ID field of a sector. If bit 6 of CIB operation status byte is set, error is soft and correctable.
5	<u>Drive Fault:</u> Hardware fault detected in selected drive unit. Usually caused by read/write, positioner, power, or speed faults.
6	<u>Cylinder Address Miscompare:</u> ID field contains a cylinder address different from expected.
7	<u>Seek Error:</u> Hardware seek error detected.
3,4	Desired Cylinder
5	Desired Head and Volume
6	Desired Sector
7,8	Actual Cylinder and Flags (Byte 8, Bits 4-7).
9	Actual Head and Volume
10	Actual Sector
11	Number of retries attempted.
12	Extended Error Status, if enabled.

-----

Table 3-9. Extended Status Code (Byte 13) Definitions

Hex Code	Definition	Hex Code	Definition
11-13	Reserved	42	Wrong type of data field
14	RAM error	43	Index too early (drive spinning too fast)
15	ROM error	44	Index too late (drive spinning too slowly)
16	Seek in progress	45	Controller read/write error
17	Illegal format type	46	Bus time out error
18	End of media	47	No drive exists
21	Illegal sector size	51	Tape cartridge not in place (DSD tape function)
22	Diagnostic fault	52	Tape cartridge write-protected (DSD tape function)
23	No index	53	Tape drive not on line (DSD tape function)
24	Invalid Function	54	Tape unrecoverable data error (DSD tape function)
25	Sector not found	55	No data on tape (DSD tape function)
26	Invalid address	56	Data miscompare during diagnostic
27	Selected unit not ready	57	Miscellaneous tape error (DSD tape function)
28	Write protected		
34	Data ECC (or CRC) error		
35	ID ECC (or CRC) error		
36	Drive fault		
37	Cylinder address miscompare		
38	Seek error		
41	Data field not found		



### 3.6.8. Diagnostics (0FH)

The diagnostic function exercises the controller and disk drive system to verify proper operation or to help isolate a malfunction. The diagnostic to be performed is specified in IOPB byte 13 (the second byte of the modifier field). Table 3-10 lists the diagnostic tests and corresponding hex codes.

The number of diagnostic tests available is controlled by the extension byte of the WUB (see 3.3.1). If extended status (bit 2) was enabled at the beginning of the operating session, all the tests listed in Table 3-10 can be selected. If not enabled, only ISBC 215 tests can be selected.

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Note  
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The extended form of the diagnostic (0FH) function is enabled by a value that the program must write in the WUB (see paragraph 3.3.1). In order to use extended diagnostics, the enabling value must be in the WUB when the controller accesses it in response to the first start (01H) program command following a reset.

Once the WUB has been accessed (in response to the first start (01H) program command), extended diagnostics cannot be enabled without resetting the controller and drives.

-----

These tests are similar to off-line HyperDiagnostics except that the on-line diagnostics require that the device and unit number be specified in the IOPB. Each function requested will initiate one pass of the selected diagnostic test.

Diagnostics use the last (highest numbered) track of head 0. When formatting a disk, this track MUST be dedicated to diagnostic program use.

When a diagnostic program begins, the head and cylinder are selected automatically, the user selects the drive unit.



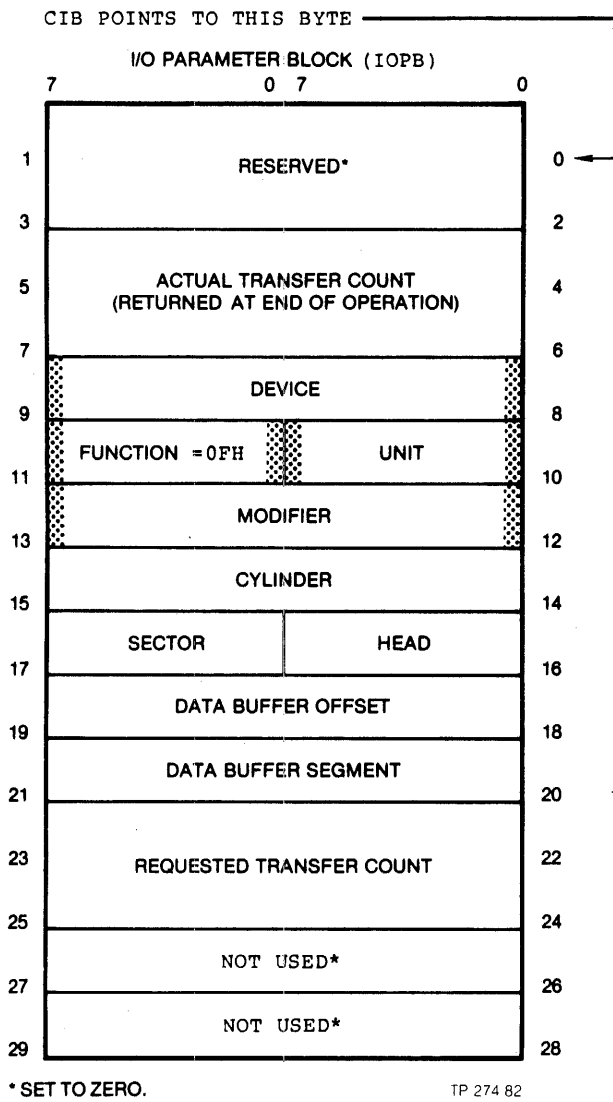


Figure 3-17. Diagnostics (0FH)

Table 3-10. On-Line Diagnostics (0FH)

<u>Extended</u> <u>or</u> <u>Normal</u>	<u>IOPB</u> <u>Byte</u> <u>13</u>	<u>Description</u>
Both	00H	A seek is executed to the last cylinder on the drive. Head 0 is selected and a read ID is performed to verify head position. The first sector is written with a 55AAH pattern and the same sector is read to verify the data and ECC/CRC.
Both	01H	Controller self-test is executed once.
Both	02H	Drive heads are positioned at cylinder 0.
Extended	1FH	<u>8085 self-test.</u> Tests the 8085, PROM, RAM, two-port buffer and DMAC, independent of components in the read/write controller section.
Extended	1BH	<u>Read/write controller self-test.</u> Tests read/write controller without exercising drives. Test 1FH must have been successfully completed prior to this test.
Extended	15H	<u>Tape drive 0 test.</u> Conduct test only if drive 0 is physically present with cartridge installed and write-enabled. Any data on the cartridge is destroyed by the test.  This test first retensions the tape cartridge (this takes about 2 minutes). Next it writes two tracks with an incrementing pattern, and then reads and verifies them. The write and read operations take about two minutes each. Test 1FH must first have been completed without error.

----- (Continued) -----

Table 3-10. On-Line Diagnostics (ØFH)

----- (Continued) -----

Extended 19H Disk drive tests. Tests operation of the drive selected by the device and unit fields of the IOPB:

Floppy drive test. Conduct test only if drive is physically present, media is installed, and write-enabled. Note that previous data on the diskette is destroyed.

This test first homes the heads to track zero, then seeks out 35 tracks and returns to track zero. It then performs a Read ID function, and writes 16 double-density sectors (256-bytes each) with an incrementing pattern.

The pattern for each sector starts at the sector number minus one: for sector one, the pattern starts at Ø. The pattern continues to 255. For sector one, the last byte is written with a value of 255.

For sector two, the pattern starts at 1 and continues to 255. This leaves the last byte still to be written, so the pattern begins again with Ø. For sector two, the last byte is written with a value of Ø.

For sector three, the first byte is 2, and the last two are Ø and 1. Sector four begins with 3, and the last three bytes are Ø through 2.

Sector 16 is the last sector written. It begins with 15, and the last 15 bytes are Ø through 14.

The test then reads and verifies the patterns. Test 1BH must first have been completed without error.

Winchester drive test. This test will fail if the Winchester has not been formatted.

The test first lowers the heads to track zero, then seeks out 128 tracks and returns. It then performs a Read ID function to determine sector size. It then reads sectors Ø through 3 on head zero for three cylinders checking for ECC errors. Test 1BH must first have been completed without error.

### 3.6.9. Read Data (04H)

The read-data function (see Figure 3-18) transfers data from a drive into a main memory buffer.

The IOPB data buffer offset and segment specify the address of the buffer in main memory. The controller clears the actual transfer count field in the IOPB at the beginning of this function. The requested transfer count is placed in the IOPB for the controller to read.

For disk drives, data is read from the drive into the controller buffer one sector at a time and then transferred into the main memory buffer. Bytes are transferred to sequential locations in the buffer until the number of transferred bytes is equal to the requested transfer count, end of media is reached, or an error occurs. The end of media is defined as the last valid sector, head, and track address (not including alternates) specified during initialization.

If the requested transfer count is not exhausted when the last sector on a track has been transferred, the controller automatically continues reading data from sector 1 on the next track. If the count is not exhausted when the last sector of the last track of the cylinder has been transferred, the controller automatically seeks the drive to the next cylinder and continues reading.

If the number of bytes in the requested transfer count does not equal a number of whole sectors, the last sector containing part of the data is read into the on-board buffer in full. Only enough data to exhaust the count is moved to the main memory buffer. The actual transfer count field in the IOPB is updated with the number of bytes written to the memory buffer and status is posted.

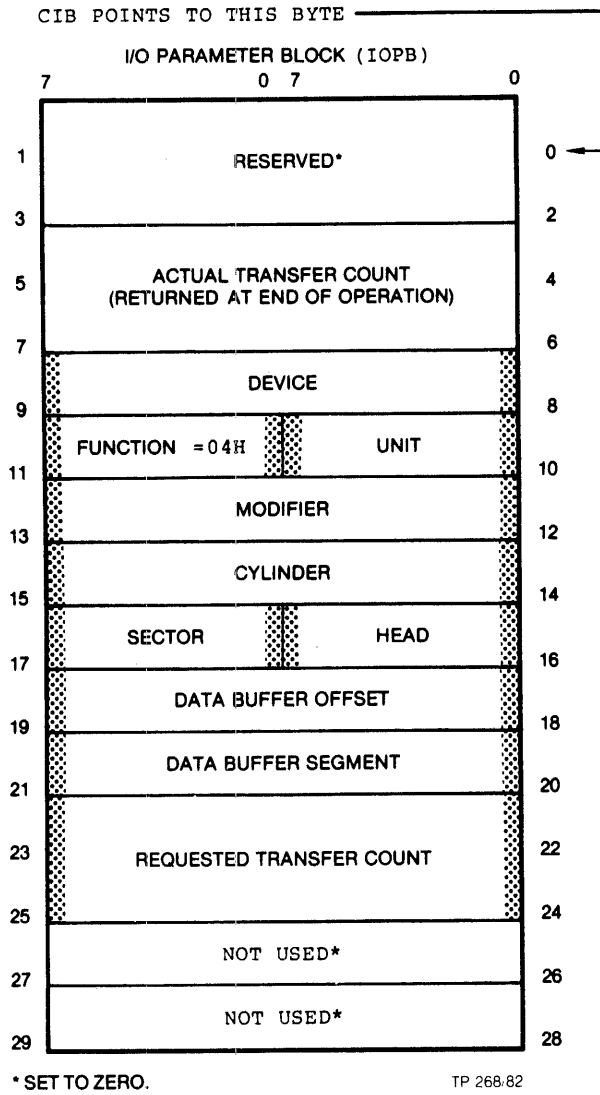


Figure 3-18. Read Data (04H)

### 3.6.10. Write Data (06H)

The write-data function (see Figure 3-19) transfers data from a main memory buffer to a drive. The IOPB unit field specifies the drive to be accessed.

The IOPB data buffer offset and segment specify the address of a buffer in main memory. The main memory is sequentially accessed. Bytes are transferred consecutively into the on-board buffer and then written to the drive.

The controller clears the actual transfer count field in the IOPB at the beginning of this function. The requested transfer count is placed in the IOPB for the controller to read. For disk drives, data is transferred from the main memory buffer into the controller buffer one byte at a time and then whole sectors are written to the drive. Bytes are transferred from sequential locations in the buffer until the number of transferred bytes is equal to the requested transfer count, end of media is reached, or an error occurs. The end of media is defined as the last valid sector, head, and track address (not including alternates) specified during initialization.

If the requested transfer count is not exhausted when the last sector on a track has been written, the controller automatically continues writing data to sector 1 on the next track. If the count is not exhausted when the last sector of the last track of the cylinder has been written, the controller automatically seeks the drive to the next cylinder and continues writing.

If the number of bytes in the requested transfer count does not equal a number of whole sectors, the last sector written with part of the data is finished with zeros. The actual transfer count field in the IOPB is updated with the number of bytes written to the memory buffer and status is posted.

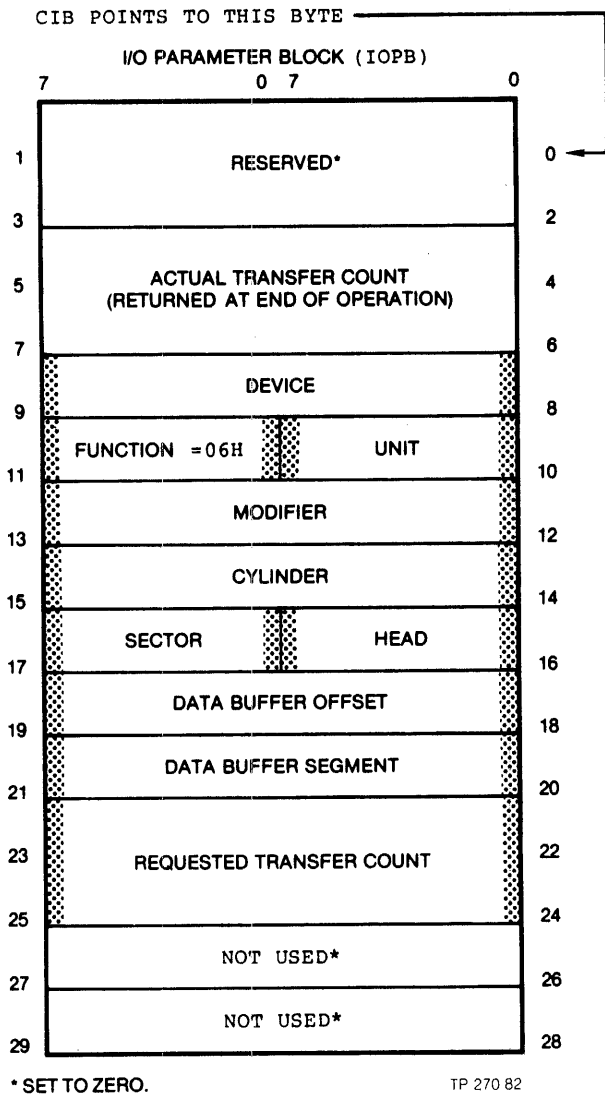


Figure 3-19. Write Data (06H)

### 3.6.11. Read Data Into Controller Buffer and Verify (05H)

This function is similar to the read-data (04H) function except that data is only transferred to the 4K on-board buffer, not into main memory. This function has several uses:

- disk sector ECC/CRC check verification
- data transfer (without using main memory) between drives
- data transfer (without using main memory) between the controller and another peripheral on the host bus.

For data transfer, the write-data from controller buffer (07H) function is required. Read (05H) and then write (07H) must be used alternately because of the 4K limit imposed by the size of the on-board buffer.

Requested transfer counts that are not a multiple of full sectors are rounded up to the nearest full sector count. The requested transfer count should not exceed 4K bytes, or data will be lost, since full sectors are always read into the on-board buffer. If the requested transfer count does exceed 4K bytes, the bytes in excess of 4K overwrite the data already in the buffer, starting with the first address.



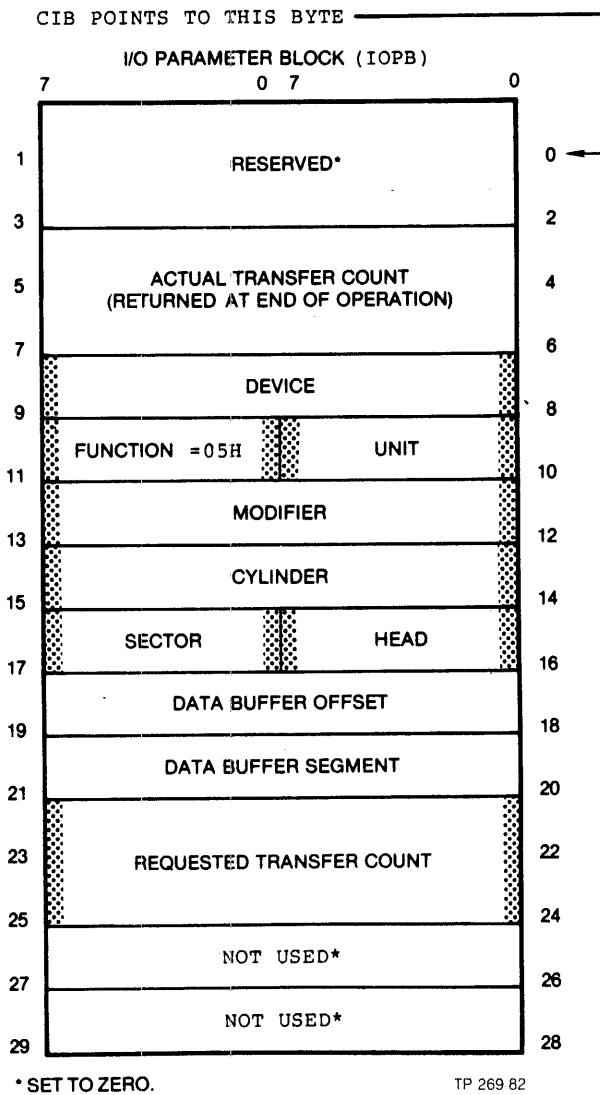


Figure 3-20. Read Data Into Controller Buffer (05H)

### 3.6.12. Write Data From Controller Buffer (07H)

This function is similar to the write-data (06H) function except that data is only transferred from the 4K on-board buffer, not from main memory. This function has several uses:

- repetitively writing the contents of the on-board buffer to sequential disk sectors
- data transfer (using only the on-board buffer) between drives, or
- data transfer (using only the on-board buffer) between the controller and another peripheral.

For data transfer, this function follows read-data into controller buffer (05H) . Read (05H) and then write (07H) must be used alternately because of the 4K limit imposed by the size of the on-board buffer. The requested transfer count must be made with the on-board buffer size in mind. If the requested transfer count is not a multiple of the number of bytes in a sector, the remainder of any sector is written with zeros.

If the requested transfer count exceeds 4k bytes, sequential sectors are written identically with the data in the on-board buffer.

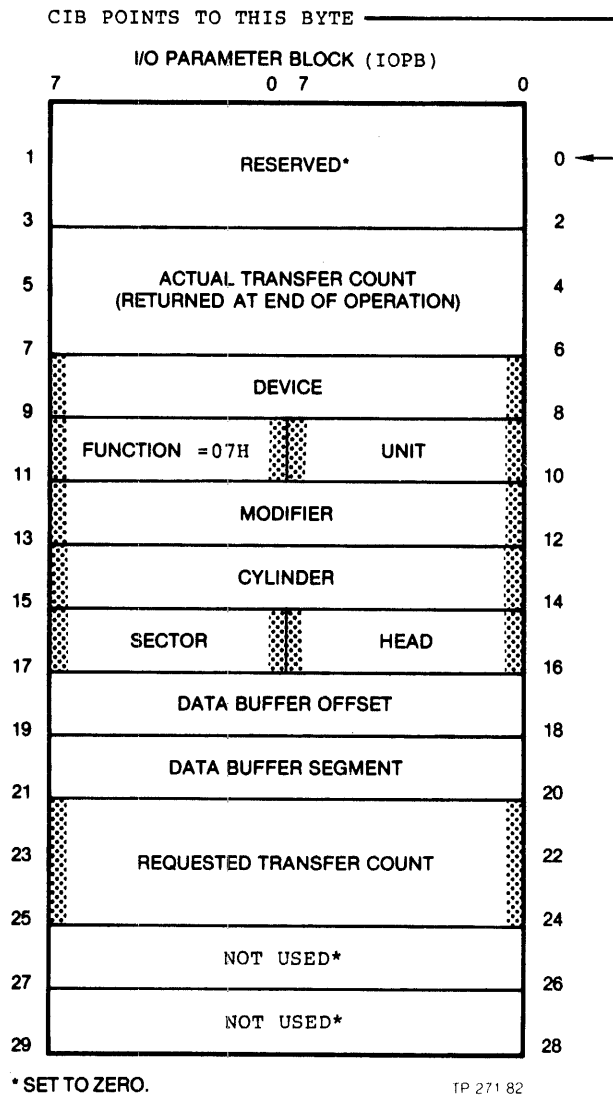


Figure 3-21. Write Data From Controller Buffer (07H)

### 3.6.13. Read Sector ID (03H)

The read sector function reads the contents of the next available sector ID field after the current head position. The data is transferred to the main memory location addressed by the offset and segment in the IOPB (see Figure 3-22).

This information may then be used for a number of purposes; verification of cylinder and head selection, sector length determination, rotational access optimization, etc. Since the function may be used to verify disk position, no implied seek or head selection is performed. The sector ID is read from the last referenced disk track on the drive.

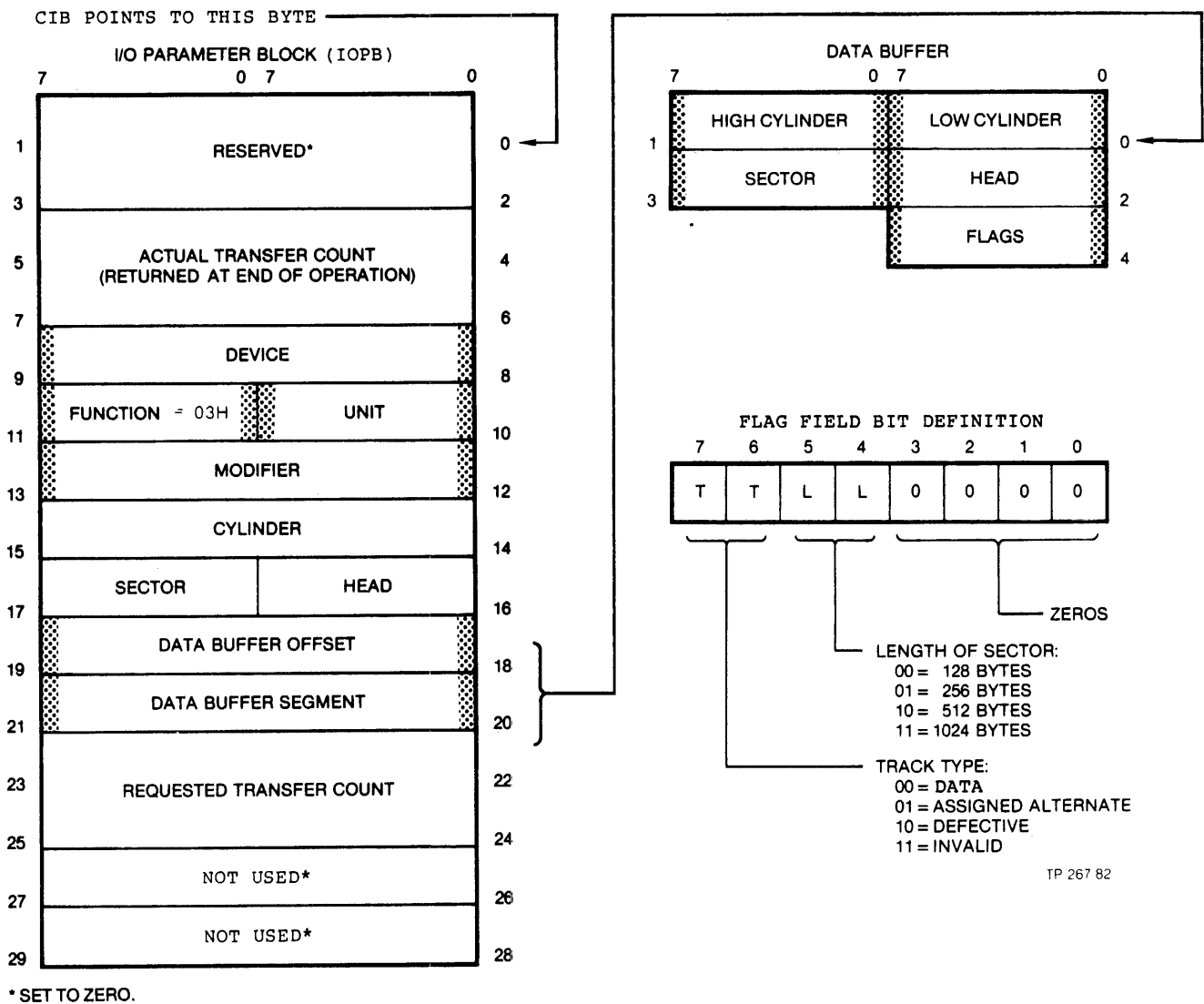


Figure 3-22. Read Sector ID (03H)

#### 3.6.14. Initiate Track Seek (08H)

Initiate track seek (08H) is a long-term function (see section 4.5.1). This function positions disk drive heads as needed. Since each of the data transfer functions include an implied seek, the primary use of this long-term function is to allow the controller to perform other activities on other drives in the system while the heads are being positioned.

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NOTE:  
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An implied seek is one automatically invoked as a part of a short-term function. An implied seek is not a long-term function.  
-----

Errors are detected and reported at the time of the first interrupt. There are no errors reported at the time of the second interrupt.

Once the controller determines that there is no error, the seek is initiated, the status semaphore is set, and an interrupt is asserted (if enabled). When the heads on the drive have reached the specified track, seek-complete status is generated and the second interrupt is asserted.

Because the controller releases the bus when the seek is initiated, several seeks may be in progress on different drives at the same time (overlapped seek). This allows the program to start seeks on multiple drives and use the first drive available.

After the point of the first interrupt, while a seek is in progress on one drive, the controller can accept functions for other drives. A function for the drive where the seek is in progress will generate a seek-in-progress error.

If a seek to a cylinder beyond the end of media, including alternates, is requested, the controller automatically homes the heads and generates an invalid address error.

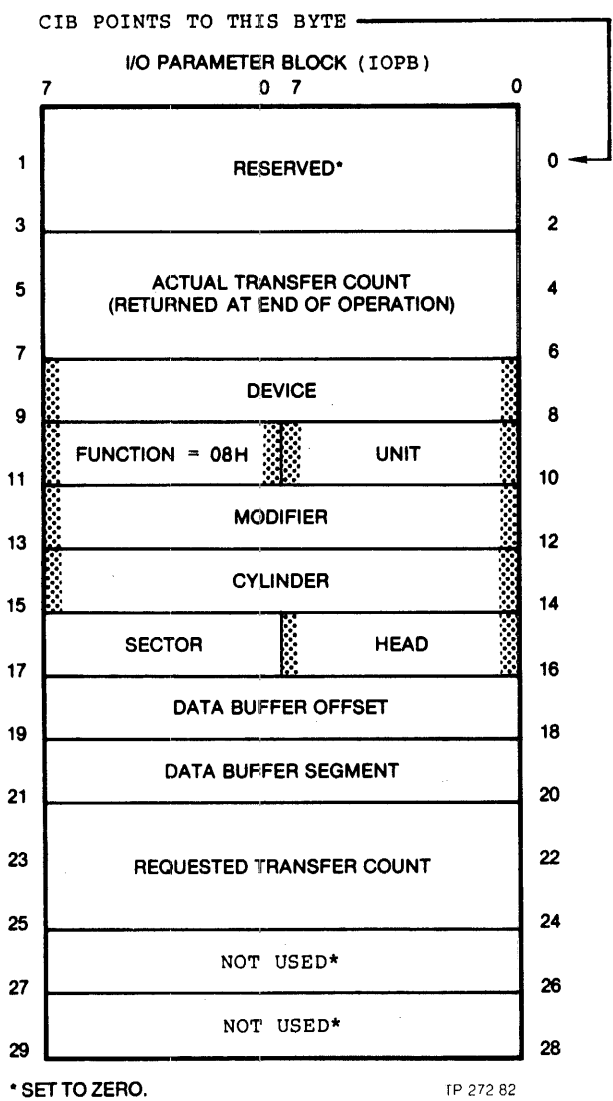


Figure 3-23. Initiate Track Seek (08H)

### 3.6.15. Buffer I/O (0EH)

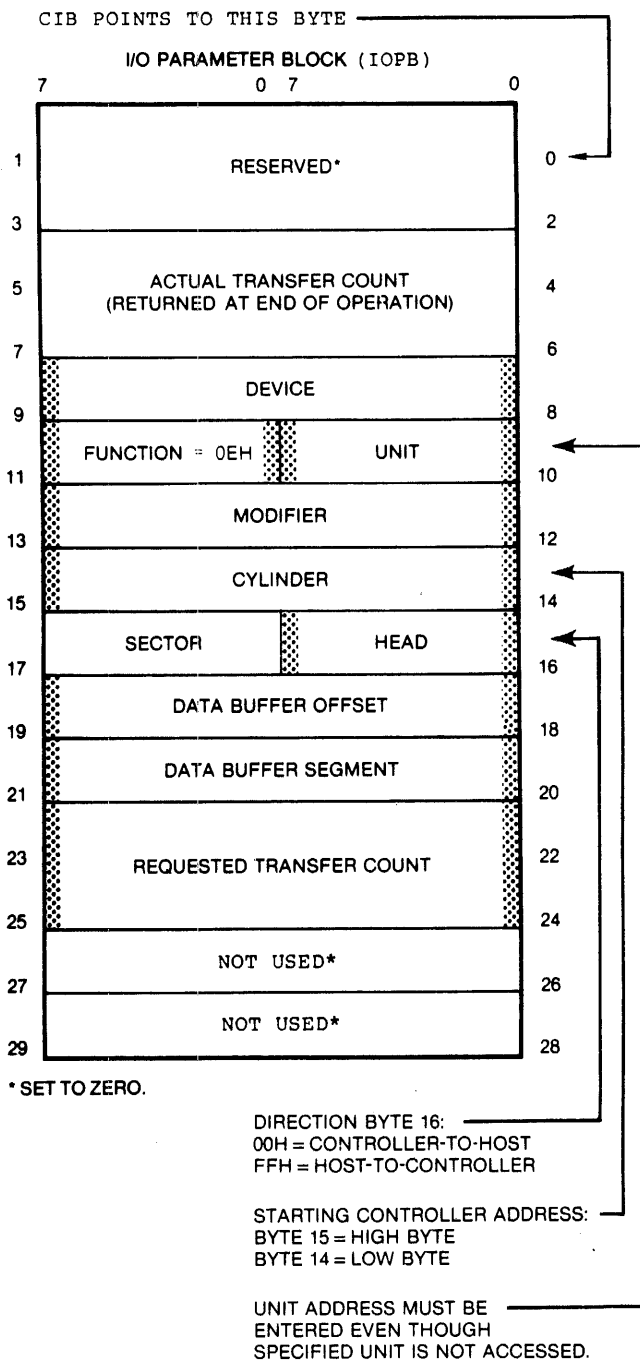
The buffer I/O function allows transfer of data between the on-board buffer and a main memory buffer (See Figure 3-24). No drive access is involved. It is used primarily for diagnostic purposes and for filling the buffer for subsequent write data from buffer (07H) functions.

The main memory buffer is addressed by the data buffer offset and segment fields. The on-board buffer starting address is specified by the cylinder field of the IOPB. For iSBC 215 compatibility, all addresses for the on-board buffer must be between 4000H and 4600H. The head field in the IOPB specifies the direction of data transfer:

- 00H for on-board to main memory (read from the buffer)
- FFH for main memory to on-board (write to the buffer)

The requested transfer count specifies the number of bytes to be transferred.





TP 273 82

Figure 3-24. Buffer I/O (0EH)

### 3.6.16. 217 Tape: Transfer Status (01H)

The program must use this function (see Figure 3-25) to transfer the contents of the on-board status buffer in controller memory to a status buffer in main memory.

After any function has been completed, the program should examine the summary error bit in the operation status byte of the CIB to obtain function execution status. If detailed status information is required, the transfer status function (01H) should be requested immediately, because the controller status buffer is cleared during the execution of all other functions.

Executing the transfer status function causes the current contents of the controller status buffer to be written to the main memory data buffer addressed by the data buffer offset and segment fields of the IOPB.

The 12-byte error status buffer (see Table 3-11) may contain three types of data as selected by the IOPB modifier field. The buffer may contain data about the function or error status of:

- The last short-term function (modifier bit 6 = 0),  
or
- the last long-term function at the time of the first interrupt (modifier bit 6 = 0), or
- current status of the last long-term function (modifier bit 6 = 1).

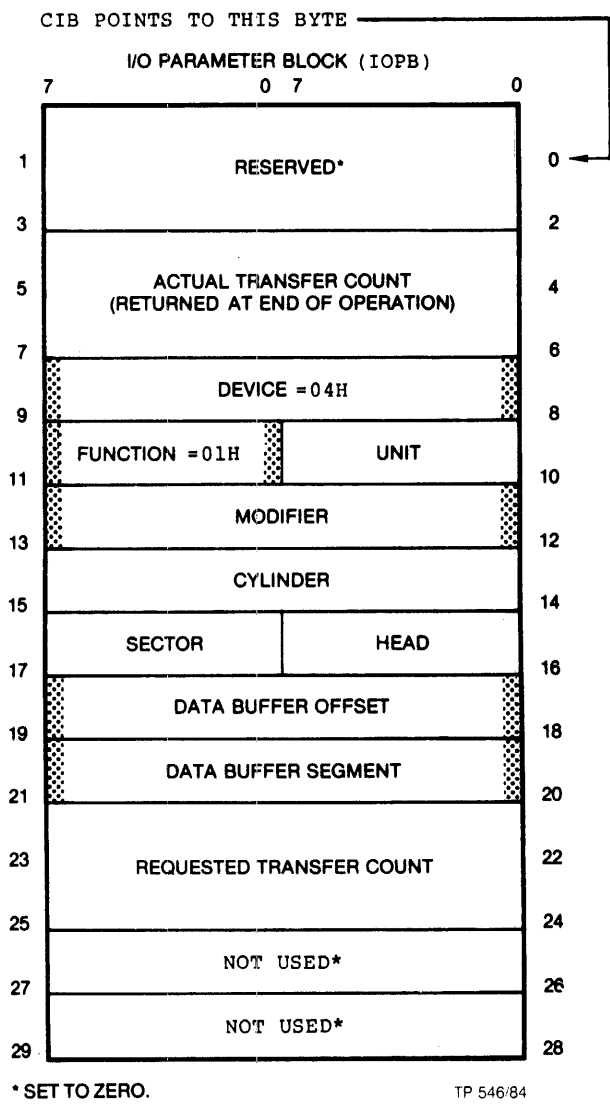


Figure 3-25. 217 Tape: Transfer Status (01H)

Table 3-11. 217 Tape Function Status Buffer Definitions

<u>Byte #</u>	<u>Definition</u>
0	Hard Error Byte
Bit: 7	End of tape (EOT).
6	Illegal format or device code, unit not present, or wrong unit.
5	Long-term function in progress when another function was requested.
4	Failed tape initialization function.
3	Not used.
2	Tape drive function rejected by tape drive controller.
1	217 tape function rejected by 6217.
0	DSD tape function rejected by 6217.
1	Hard Error Byte
Bit: 7	Tape cartridge write-protected.
6	Selected unit not ready.
5	Invalid address.
4	No tape cartridge in selected drive.
3	Invalid function as defined by byte 0, bit 0, 1, or 2.
2	Timeout occurred on tape function.
1	Diagnostic fault.
0	Length error: <ul style="list-style-type: none"> <li>• No transfers requested, or</li> <li>• requested transfer count not divisible by 512, or</li> <li>• read or write function terminated as specified by other bytes.</li> </ul>

(Continued)

Table 3-11. 217 Tape Function Status Buffer Definitions  
 -----(Continued)-----

<u>Byte #</u>	<u>Definition</u>
2	Soft Error Byte
Bit: 7	Not used.
6	Buffer overrun/underrun: no data lost, but drive controller had to stop tape, rewind slightly, and bring tape up to speed before continuing.
5	Broken tape or other drive fault.
4	Not used.
3	Unrecoverable data detected on tape.
2	Not used.
1	Recoverable data error: function completed through the use of retries.
0	Not used.
3	Beginning of tape (BOT), FFH = true.
4	Not used.
5	File mark detected (FMD), FFH = true.
6, 7	Not used.
8	No data detected, FFH = true.
9, 10	Not used.
11	Number of retries. Byte value definitions:
1	Less than 8.
8	Between 8 and 16: indicates probable media wear.
16	Unrecoverable data: indicates media probably worn out.

-----

3.6.17. 217 Tape: Read Status (1EH)

Read 217 tape status (see Figure 3-26) puts current 217 tape status into the status buffer of the DSD controller. This function must be followed by a transfer 217 status function (01H), in order to transfer the data from the controller to main memory.

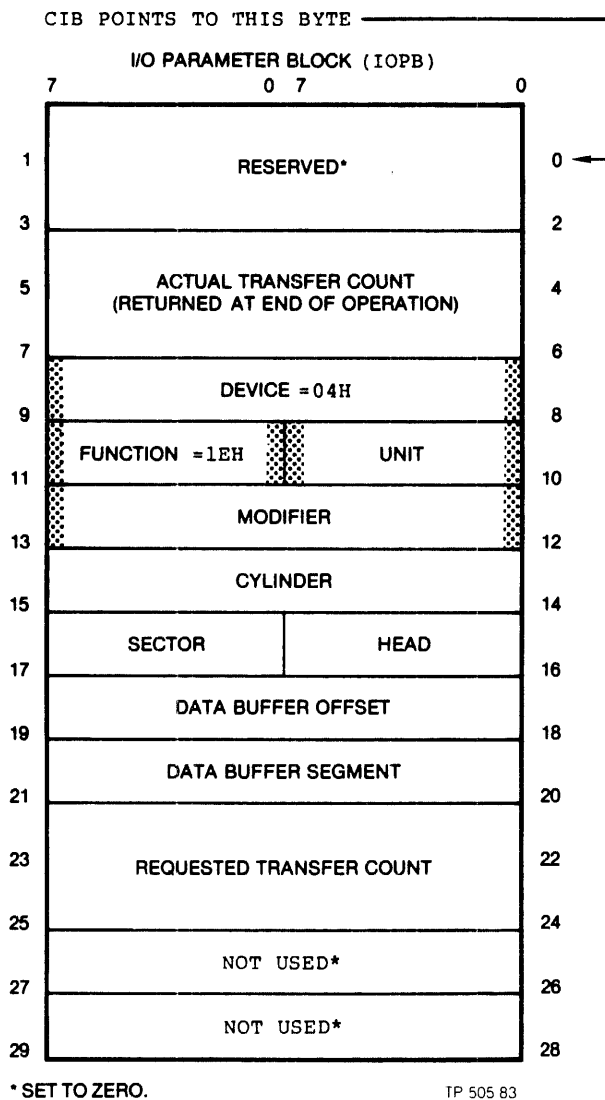


Figure 3-26. 217 Tape: Read Status (1EH)

3.6.18. 217 Tape: Read Data (04H)

For the 217 functions, the requested transfer count must be divisible by 512. Bytes are transferred consecutively from the tape to the on-board buffer, and then to sequentially accessed main memory, as addressed by the data buffer offset and segment fields of the IOPB (see Figure 3-27).

If the data transfer rate falls below 200 Kb/sec during the read-data function, the streaming mode cannot be maintained. In such a case, a buffer overrun/underrun error is posted to indicate that the tape drive controller had to stop and reposition the tape, and then continue the read-data function. This is not an indication of bad data.

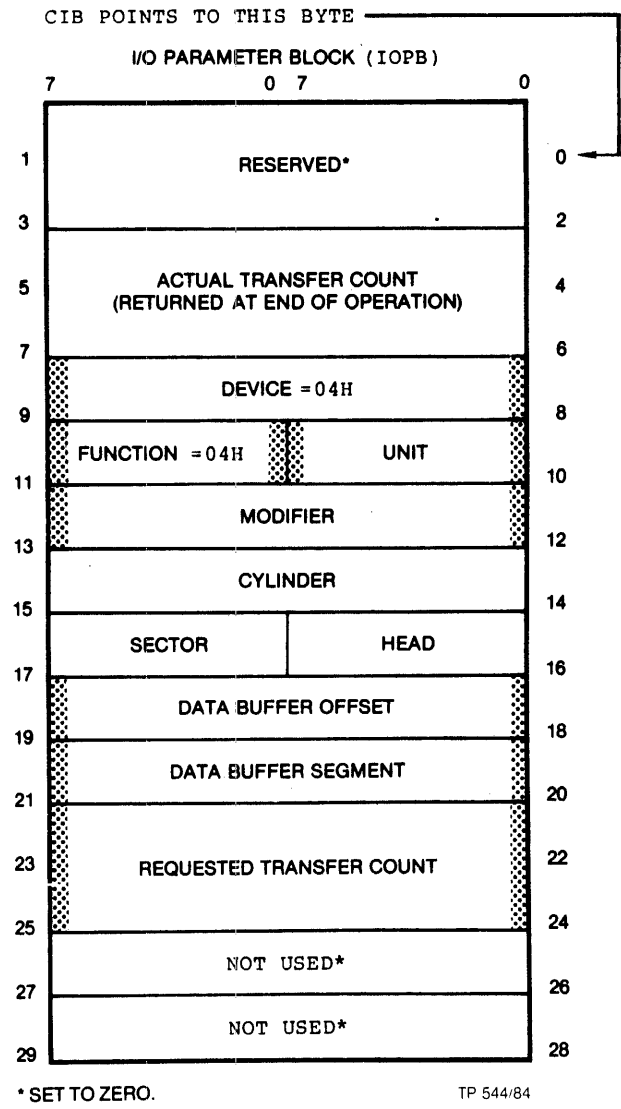


Figure 3-27. 217 Tape: Read Data (04H)

This function continues until one of three conditions is met:

- The actual transfer count equals the requested transfer count, or
- a file mark is encountered on the tape, or
- a 217 r/w terminate function is encountered.

If the buffer area in main memory is too small to accommodate an entire file, it may be necessary to use a series of read-data functions with small transfer counts. If the actual transfer count equals the requested transfer count before a file mark is encountered, then a transfer status function would reveal a buffer overrun/underrun error.

If the actual transfer count equals the requested transfer count shortly before a file mark is encountered, a transfer status function does not return file mark status, because this value is not written until the next read-data function is requested.

When the read-data function continues until it is terminated by a file mark on the tape, the controller writes 89H in the operation status byte of the controller invocation block. 89H in the operation status byte indicates a tape drive summary error, and termination of the function.

If a transfer status function reveals the file mark byte and the length error bit set, this should be interpreted as a successful termination. This is a legal termination procedure, although it does use what are otherwise error messages to indicate a successful completion.

A read-data function still in progress can be terminated by a 217 read/write terminate function. A 217 r/w terminate function is legal only before the read-data function terminates for other reasons.

When a read-data function is terminated by a 217 r/w function, it causes the drive to stop reading data and rewind to the beginning of the tape (BOT). In the error status buffer, this function posts a buffer overrun/underrun error, and sets the BOT-byte. The over/underrun error does not indicate bad data.

If the tape drive controller detects bad data, it makes a maximum of 16 attempts to read the data. This action is transparent to the DSD controller and the program.

If the data is successfully read, byte 11 of the error status buffer indicates that retries were necessary, with an approximation of how many. A byte value of 1 indicates that less than seven retries were necessary. A byte value of 8 indicates that between 8 and 16 retries were necessary.



If the data cannot be read in 16 automatic attempts, an unrecoverable data error is posted. The value 16 is posted to byte 11.

A read-data function requested on a blank tape will terminate after a few inches of tape have been accessed. These errors post:

- Length
- Recoverable data
- Unrecoverable data
- No data detected

### 3.6.19. 217 Tape: Write Data (06H)

This function continues until the actual transfer count equals the requested transfer count, or a 217 r/w terminate function is encountered.

If the buffer area in main memory is too small to accommodate an entire file, it may be necessary to use a series of write-data functions with small transfer counts, until the entire file has been transferred. The series of write-data functions must be terminated by a 217 read/write terminate function. A 217 r/w terminate function is legal only before the write-data function terminates for other reasons.

When a write-data function is terminated by a 217 r/w function, it causes the drive to stop writing data, write a file mark, and then rewind to BOT. In the error status buffer, this function posts a buffer overrun/underrun error, and sets the BOT-byte. The over/underrun error does not indicate bad data.

If the tape drive controller detects bad data, it makes a maximum of 16 attempts to write the data. This action is transparent to the DSD controller and the program.

If the data is successfully written, byte 11 of the error status buffer indicates that retries were necessary, with an approximation of how many. A byte value of 1 indicates that less than seven retries were necessary. A byte value of 8 indicates that between 8 and 16 retries were necessary.

If the data cannot be written in the 16 automatic attempts, an unrecoverable data error is posted. The value 16 is posted to byte 11.

If the data transfer rate falls below 200 Kb/sec during the write function, the streaming mode cannot be maintained. In such a case, a buffer overrun/underrun error is posted to indicate that the tape drive controller had to stop and rewind the tape, and bring it up to speed before continuing the write-data function.

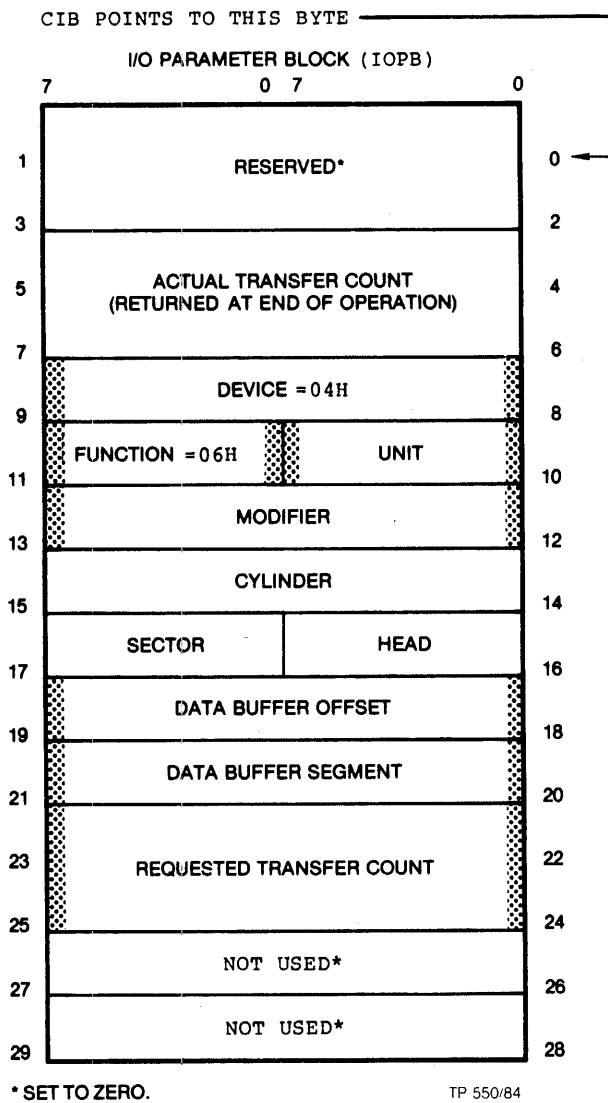


Figure 3-28. 217 Tape: Write Data (06H)

3.6.20. 217 Tape: Read/Write Terminate (1FH)

The 217 r/w terminate (see Figure 3-29) function terminates a read or write function in progress. This function is legal only before a read or write function terminates for other reasons.

This function causes the drive to stop reading data and rewind to BOT. If the function being terminated by the 217 r/w termination was write data (IOPB Function Field = 06H), a filemark is automatically written before the tape rewinds.

In the error status buffer, this function posts a buffer overrun/underrun error and sets the BOT-byte. The overrun/underrun error does not indicate bad data.

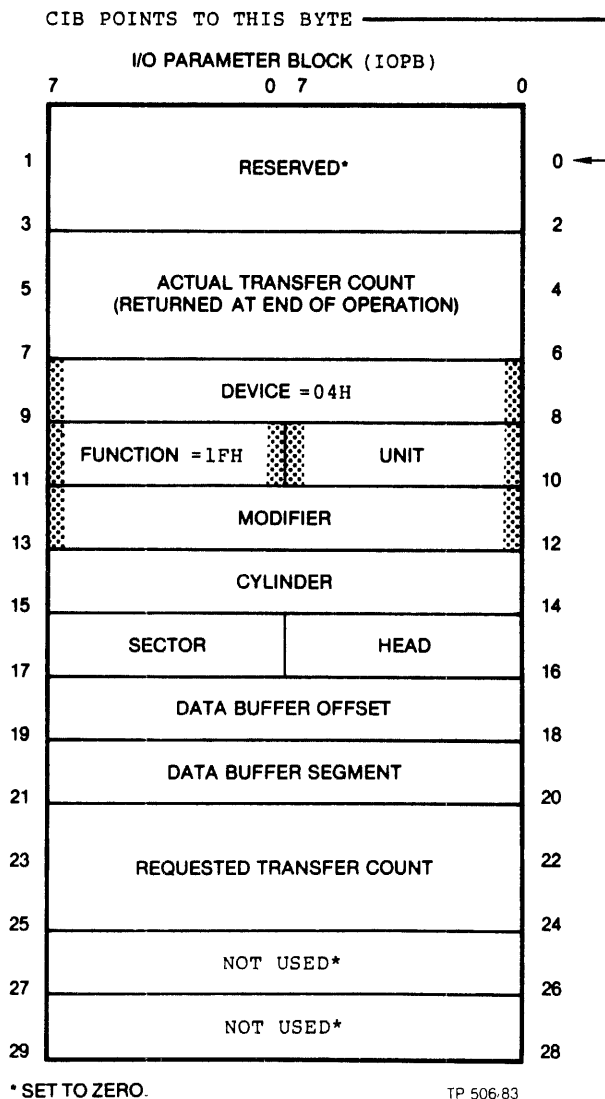


Figure 3-29. 217 Tape: Read/Write Terminate (1FH)

3.6.21. 217 Tape: Move Forward One File (12H)

Move forward one file (see Figure 3-30) is a long-term function that causes the tape to advance until a file mark is encountered, or the end of media is reached. When a file mark has been found, the FMD bit is set in the error status buffer.

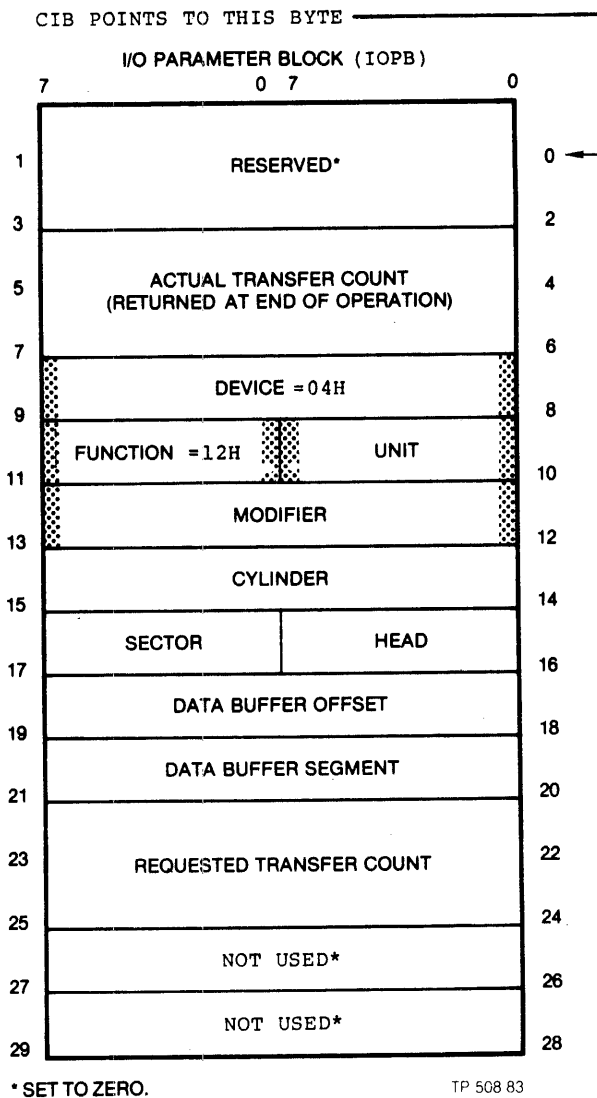


Figure 3-30. 217 Tape: Move Forward One File (12H)

### 3.6.22. 217 Tape: Move Forward One Record (1AH)

Move forward one record (see Figure 3-31) moves the tape forward seeking an interblock gap. The function terminates when one of four conditions is met:

- An interblock gap is encountered, or
- a file mark is detected (FMD bit set in error status buffer), or
- the end of tape is encountered (EOT bit set in error status buffer), or
- the function times out on a blank tape (time-out bit set).

Time out occurs after the time needed for 32 data blocks to pass has elapsed.

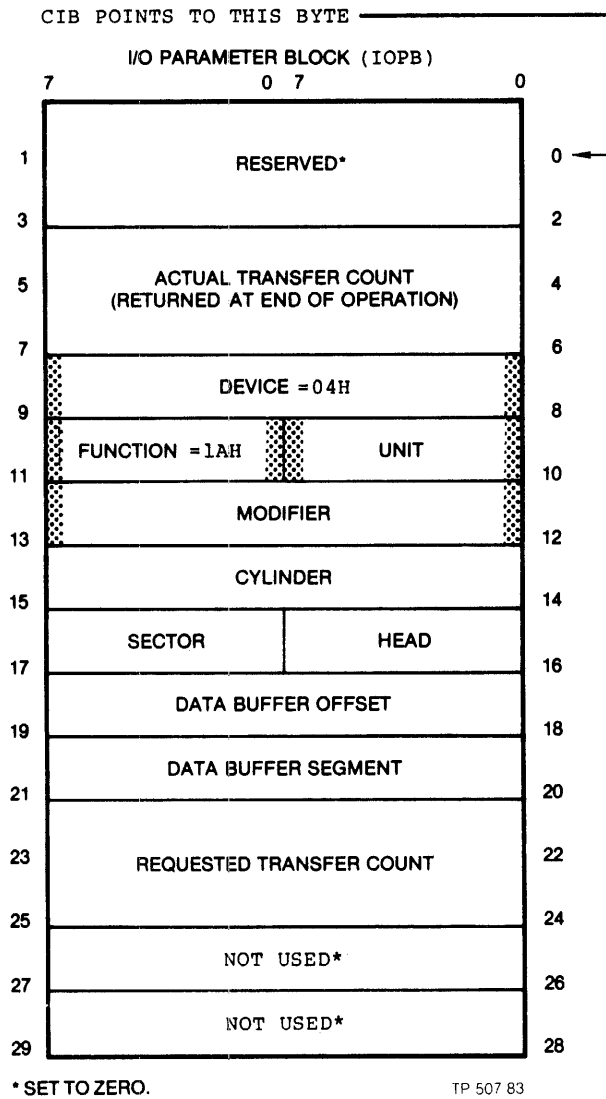


Figure 3-31. 217 Tape: Move Forward One Record (1AH)

3.6.23. 217 Tape: Write File Mark (14H)

Write file mark (see Figure 3-32) can be used to write a file mark on the tape as needed.

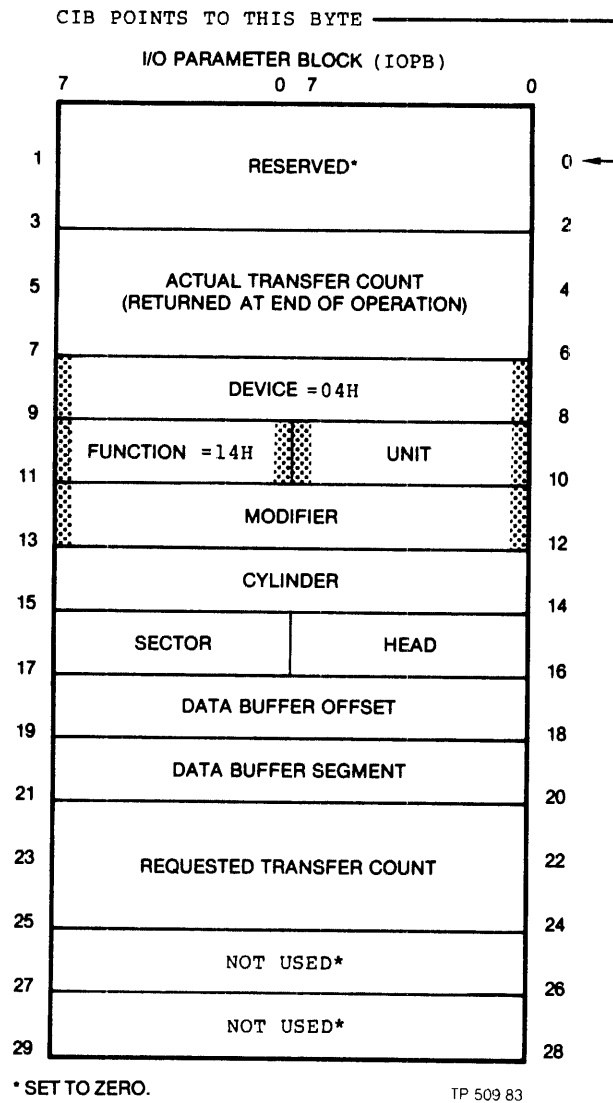


Figure 3-32. 217 Tape: Write File Mark (14H)



### 3.6.24. 217 Tape: Retension Tape (1DH)

Retension tape (see Figure 3-33) is a long-term function that causes the tape to fast-forward to EOT and then rewind to BOT. This function attempts to improve the condition of the tape in the cartridge.

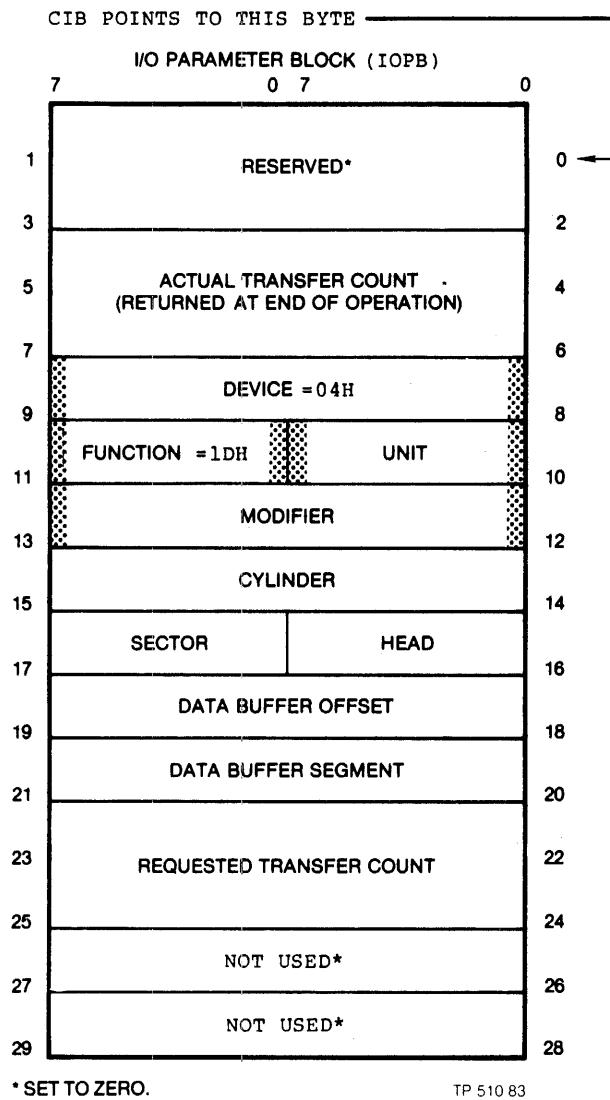


Figure 3-33. 217 Tape: Retension Tape (1DH)

3.6.25. 217 Tape: Erase (17H)

Erase tape (see Figure 3-34) is a long-term function that moves the tape to BOT, erases until EOT is reached, and then rewinds the tape to BOT again.

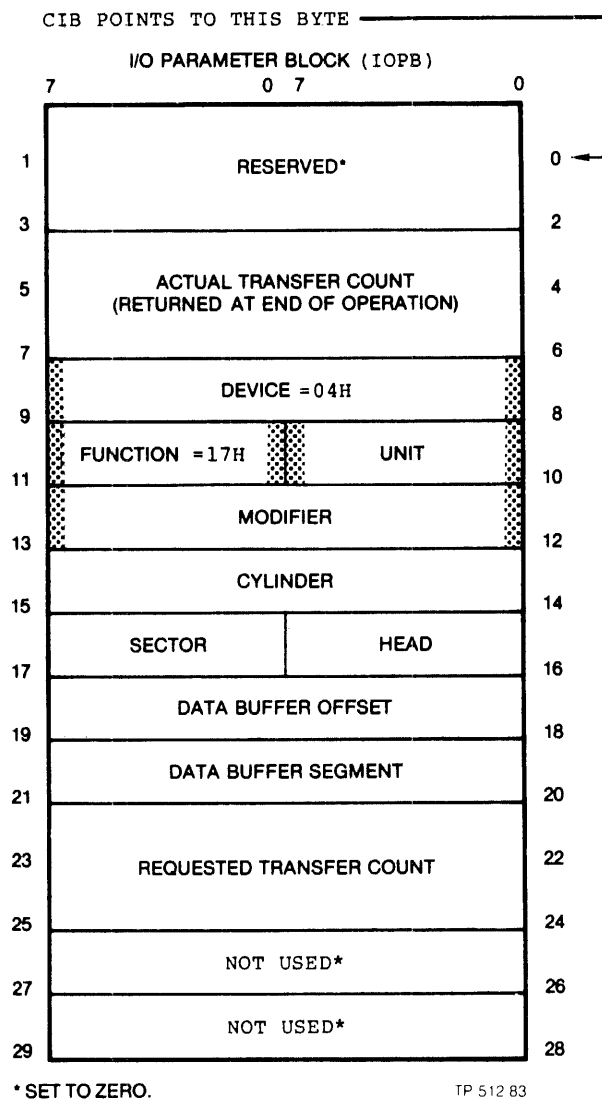


Figure 3-34. 217 Tape: Erase (17H)

### 3.6.26. DSD Tape: Reset Drive (80H)

The reset tape drive function (see Figure 3-35) is required before any DSD tape functions can be invoked. This function resets the tape drive and brings it to a known initial state. requesting this function aborts any other tape operations that may have been in progress.

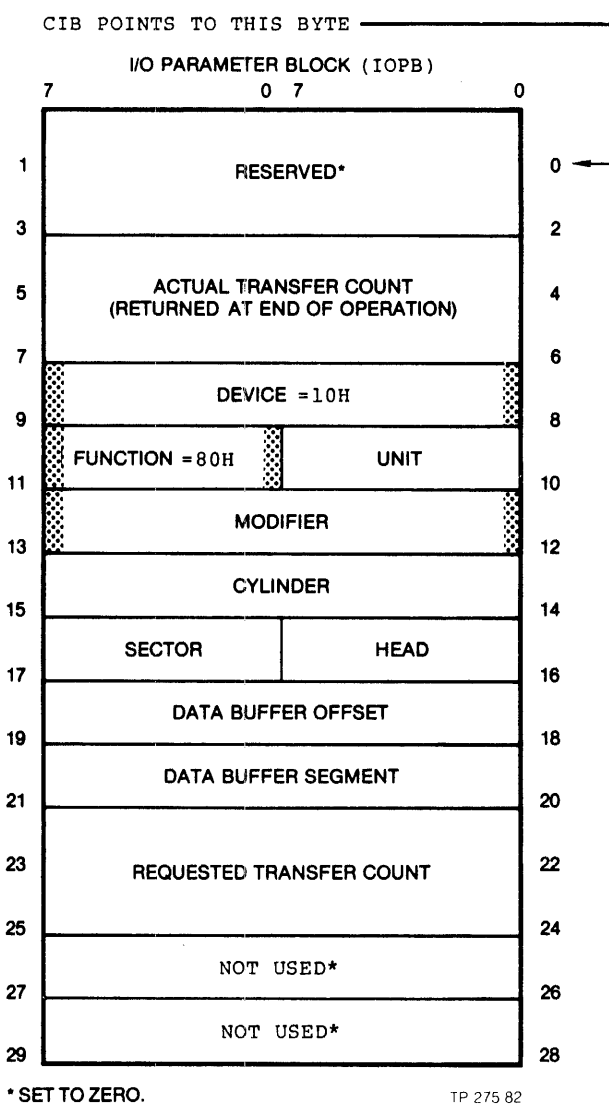


Figure 3-35. DSD Tape: Reset Drive (80H)

### 3.6.27. DSD Tape: Retension Cycle (84H)

This function is recommended for new cartridges or when a cartridge requires an excessive amount of read or write retries.

This function returns an operation complete status when the retension cycle starts. Except for a reset tape drive function (that would abort any function), other functions requested before the retension cycle is complete wait before proceeding.

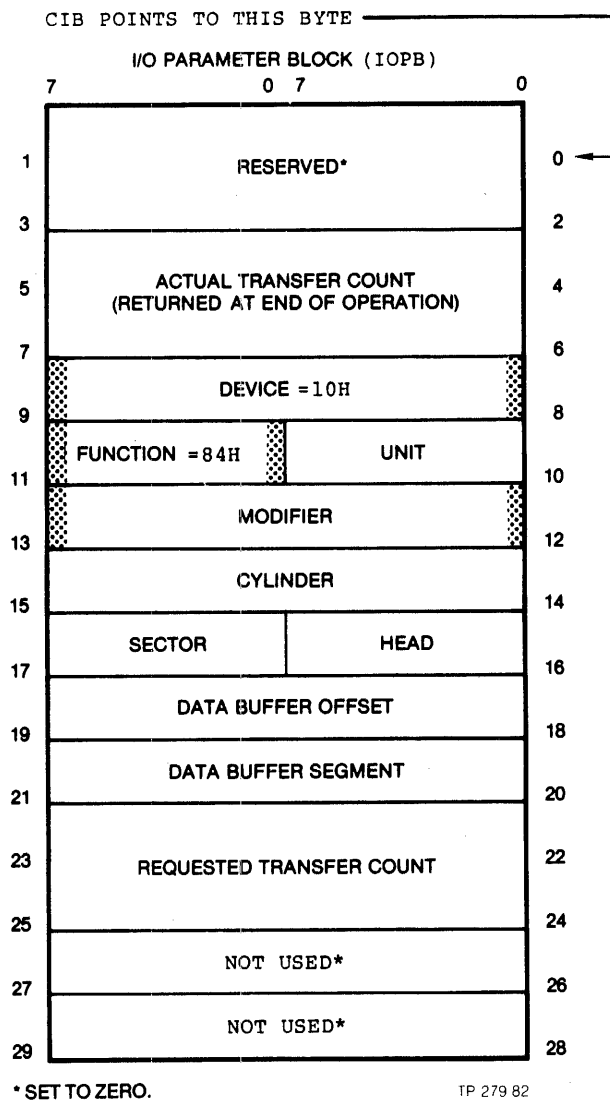


Figure 3-36. DSD Tape: Retension Cycle (84H)

### 3.6.28. DSD Tape: Disk-Image Backup (81H)

The disk-image backup function (see Figure 3-37) provides backup for data stored on Winchester drives. If the data from the Winchester exceeds the capacity of the tape cartridge, backup can be continued onto another cartridge.

The regular power-up function sequence must be observed before mirror-image functions can be carried out. The disk drives must be initialized, and the tape drive reset.

If the end of the tape is reached before the function is complete, the controller posts the status and generates an interrupt (if enabled). The operation status byte contains the following information:

- operation not complete
- media change not detected
- seek not complete
- Winchester drive type
- no error
- Winchester unit number

When a new tape cartridge is inserted, the controller again posts status showing that the media change has been detected.

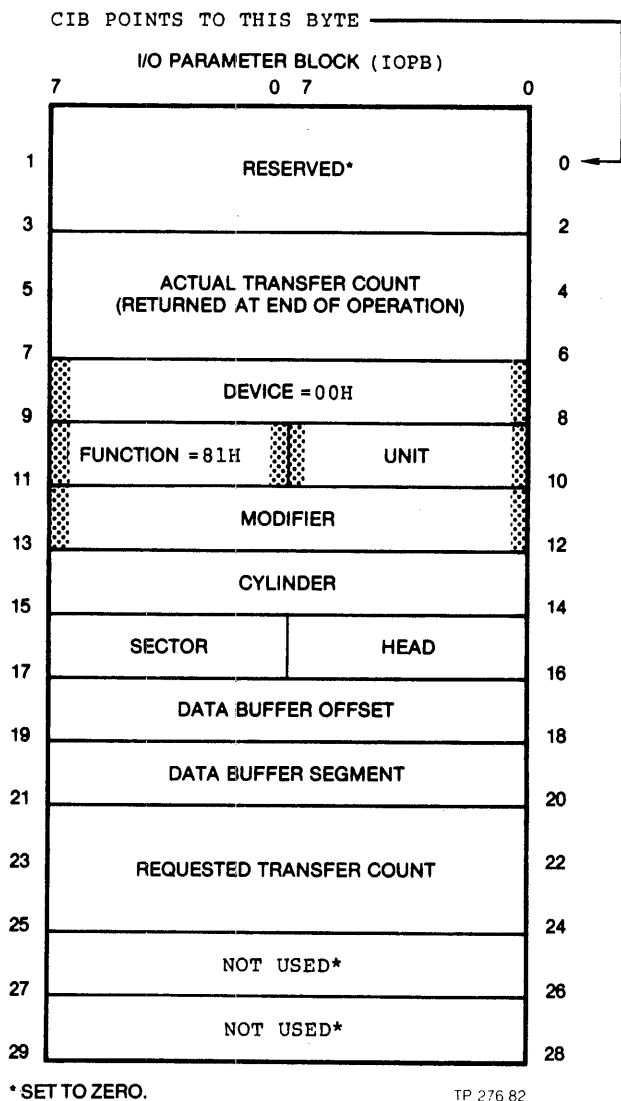


Figure 3-37. DSD Tape: Disk-Image Back-up (81H)

### 3.6.29. DSD Tape: Disk-Image Restore (82H)

The disk-image restore function (see Figure 3-38) writes a disk with an image from tape previously made by the disk-image back-up function. The unit field specifies the Winchester drive to be restored.

The regular power-up function sequence must be observed before mirror-image functions can be carried out. The disk drives must be initialized, and the tape drive reset.

If the end of the tape is reached before the function is complete, the controller posts the status and generates an interrupt (if enabled). The operation status byte contains the following information:

- operation not complete
- media change not detected
- seek not complete
- Winchester drive type
- no error
- Winchester unit number

When a new tape cartridge is inserted, the controller again posts status showing that the media change has been detected.

-----  
Note  
 -----

If the tape cartridge has been in storage, or if additional data has been written to the Winchester since the last backup, a new disk-image backup function (81H) should precede a disk-image restore function. This guards against data loss if the previous backup cartridge is faulty.

To restore the image of one Winchester to another, both drives must be formatted identically.  
 -----



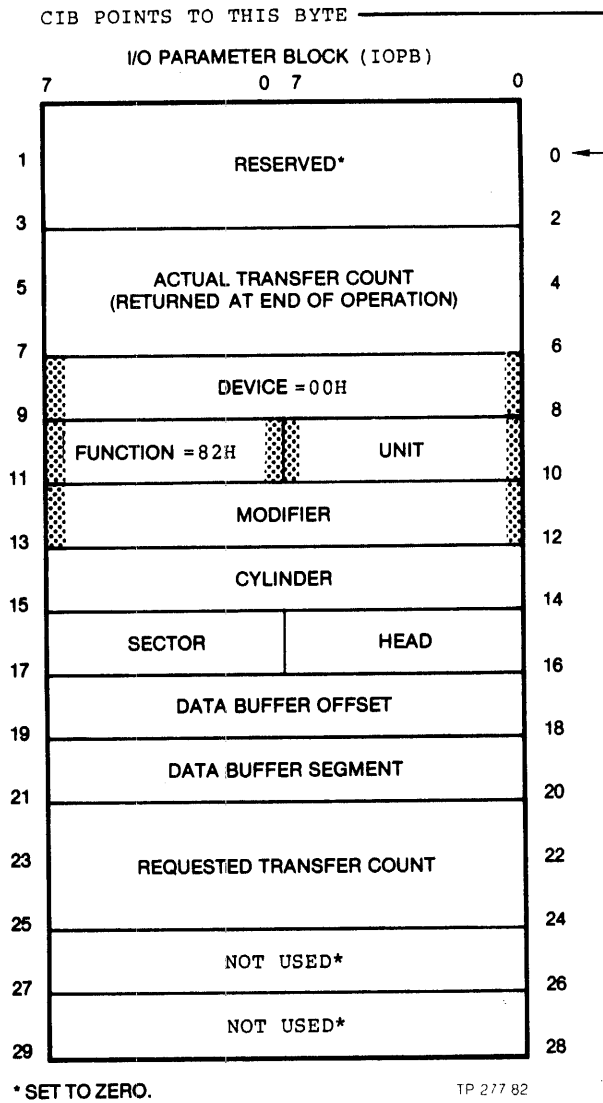


Figure 3-38. DSD Tape: Disk-Image Restore (82H)



3.6.30. DSD Tape: Read Tape Status (83H)

The read tape status function (see Figure 3-39) causes six status bytes to be transferred from the streaming tape drive controller to main memory. Status byte 0 is transferred to the main memory location specified by the data buffer offset and segment fields. The remaining bytes follow in order. See Table 3-12 for status buffer definitions.

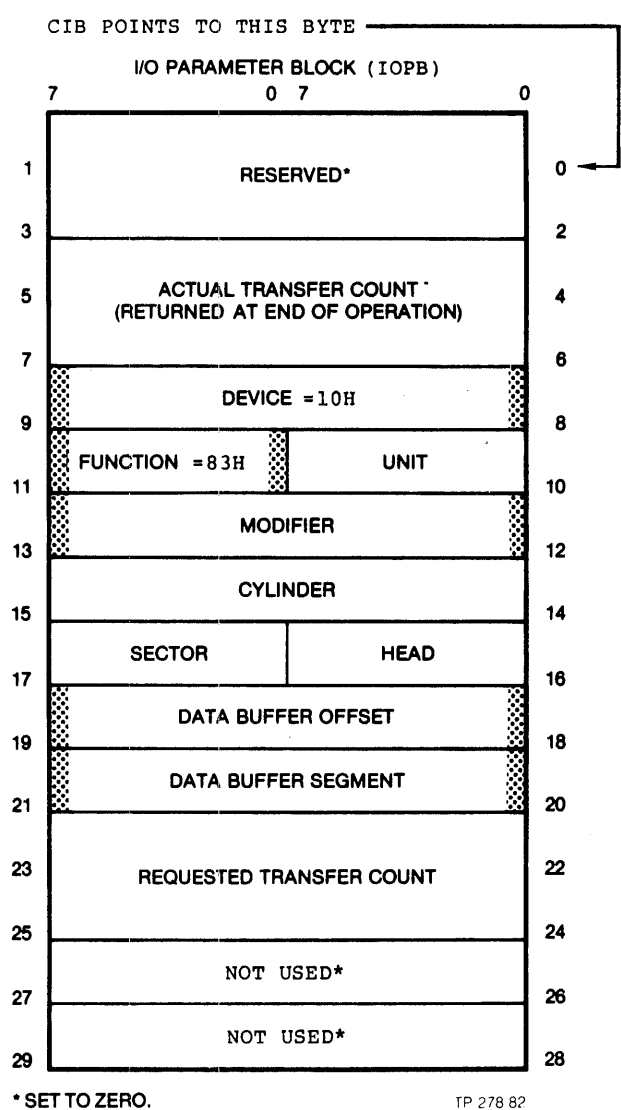


Figure 3-39. DSD Tape: Read Tape Status (83H)

Table 3-12. DSD Tape Function Status Buffer Definitions

<u>Byte</u>	<u>Bit</u>	<u>Description</u>
0	7	There is another bit set in byte 0.
	6	Tape cartridge not inserted, or removed while drive select light was on.
	5	Selected drive was not present when the function was invoked.
	4	Write function invoked on a write-protected cartridge.
	3	End of the last track reached during a read or write operation.
	2	Unrecoverable data error.
	1	Unrecoverable error. The block in error may have been transferred.
	0	File mark detected. (End of image reached during disk-image restore.)
1	7	There is another bit set in byte 0.
	6	Illegal function sent to tape controller.
	5	Drive controller was unable to find data on tape.
	4	Eight or more read retries were required to recover a data block (probably indicative of media wear).
	3	Media is at BOT.
	2	Reserved.
	1	Reserved.
	0	Power-on reset has occurred since the last operation.

----- (Continued) -----

Table 3-12. DSD Tape Function Status Buffer Definitions

----- (Continued) -----		
<u>Byte</u>	<u>Bit</u>	<u>Description</u>
-----		
2,3	0-7	The third and fourth bytes contain a 16-bit binary number that is the count of the number of rewrites that occurred during a write operation, or the number of read retries that occurred during a read operation. Byte 2 contains the high byte, and byte 3 the low.
4,5	0-7	The fifth and sixth bytes contain a 16-bit binary number that is the count of the number of under-runs that occurred during a read or write operation. Byte 4 contains the high-byte, and byte 5 the low.
-----		

A read-tape-status function (83H) resets bits 0 through 3 in byte 0, and bits 0 through 7 in byte 1. It clears the count in bytes 2 through 5. To inform the user of data errors on the tape, bits 0 through 2 of byte 0, and bits 4 and 5 of byte 1 will be set (if they were set on the last read status function).

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## 4. Controller Architecture

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### 4.1. DSD Controller Description

This Chapter contains a block diagram and description of the DSD Controller. The controller consists of a high speed internal bus and data path (pipeline), internal bus masters, and slave interfaces (See figure 4-1). The MPU (microprocessor unit) and DMAC (direct memory access controller) control the bus as masters. The host bus, streaming tape drive, and disk drive interfaces are slaves on the internal bus.

The MPU, which provides all the intelligent controller functions, consists of a 5-Mhz 8085 microprocessor, a pair of 2732 or 2764 EPROMs, and a combination RAM-I/O counter peripheral chip. The 256-byte RAM is a local stack and scratch area that buffers disk commands received from the host bus interface. The I/O ports provide control lines for the slave interfaces and the r/wc (read/write controller). The 8085 controls low speed operations such as buffering commands from the host system, housekeeping chores, executing on-board confidence tests, and initiating off-line backup and restore operations. It supports the iSBC 215 and iSBX 218 emulations. The DMAC, a 5-Mhz 8237 chip, transfers data at high speeds between one port of the dual-port memory and either of two slave interfaces. During backup and restore operations, data are transferred to and from the streaming tape interface. During disk operations, data are transferred to and from the host bus interface.

Disk operations that are too fast for the MPU are performed by the Read/Write Controller (r/wc). Its basic functions are to format the disk tracks, recognize header fields for disk sectors, and to read or write data on the drive, track, and sector specified by the MPU and the disk drive slave interface. The r/wc is a 2910 sequencer clocked at the disk data rate, and is part of the data transfer pipeline. The sequencer uses 1K words of PROM which act as instructions to control other functions including the dual-

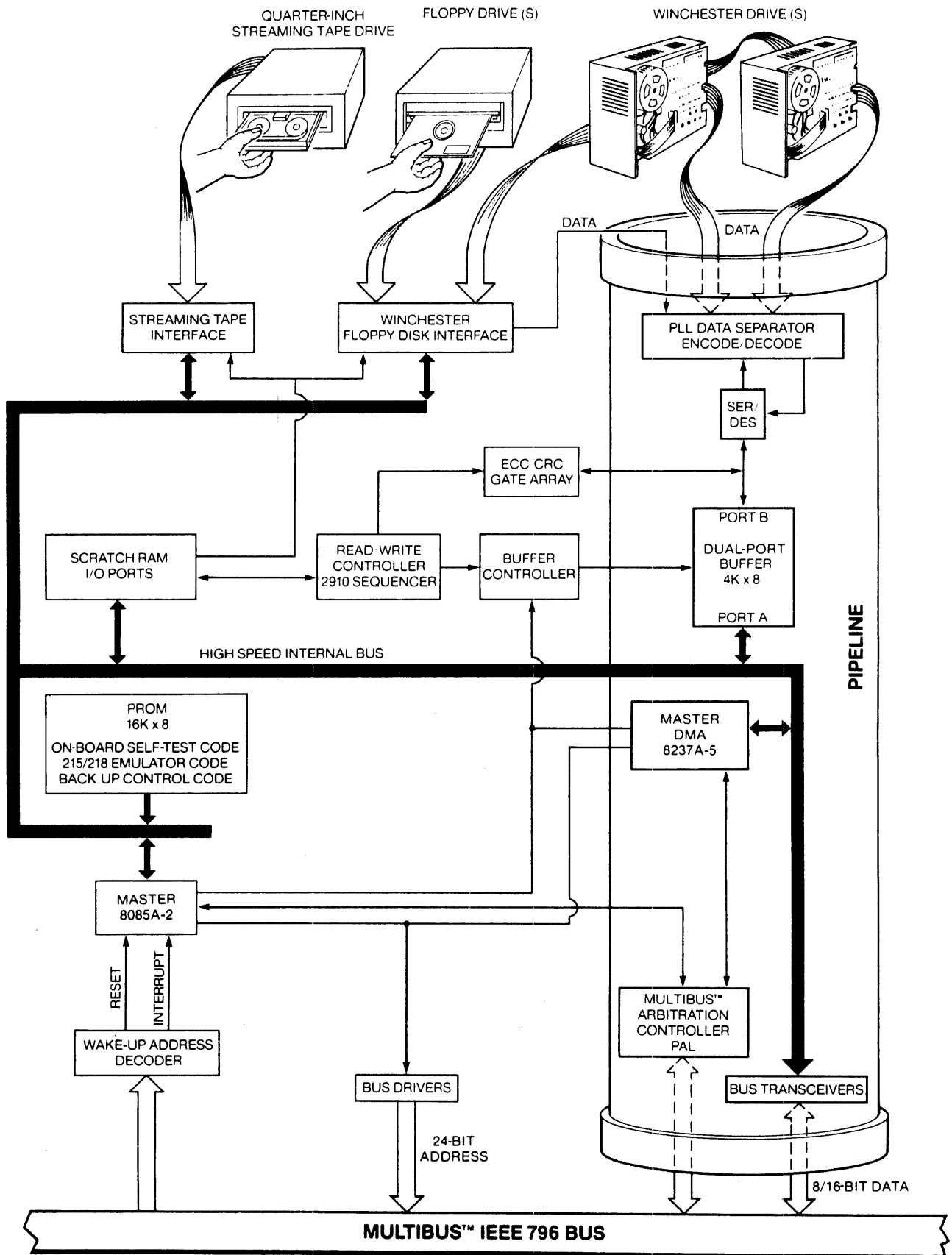


Figure 4-1. Controller Block Diagram

port buffer and ECC/CRC gate array. The sequencer instructions are decoded by one of seven PALs (programmable array logic devices), to reduce chip count. The 2910 permits generation of data streams for direct writing in Winchester drives via the pipeline.

The dual-port buffer consists of a buffer controller (two PAL chips) and four Kbytes of RAM storage. Both ports operate asynchronously with arbitrations provided by the buffer controller. The dual-port buffer anticipates successive transfers to guarantee both the r/wc and the internal bus master always have the next byte of data available when requested.

The host bus interface requests bus access and directs all data transfer operations once bus master control is achieved. Two PAL chips, tailored to the controller architecture, achieve efficient operation and maintain strict host bus compatibility. The Multibus interface transfers data as bytes or words, depending upon the system environment. This is an important feature, as word transfer results in twice the data being handled per host bus access.

Data integrity is a foremost concern of system integrators. The controller incorporates a proprietary error correction chip which handles both Winchester ECC and floppy CRC. A unique computer-generated polynomial for ECC offers improvements in correction accuracy compared with conventional polynomials over a variety of sector sizes.

When data are read, the chip detects errors including error bursts up to 22-bits in length. If an error is detected, the controller automatically tries to re-read the sector. If a correct read ensues, the controller passes the data (via a DMA operation) and reports a soft error (via status registers) to the operating system. If retries cannot correct the error and the error pattern is repeatable, the ECC chip allows up to 11 bits to be corrected. The MPU writes the corrected bits directly into the dual-port buffer. The DMA controller transfers the corrected data to the host bus main memory. Selection of automatic correction is software controlled. Corrections are reported in the same way as soft errors so the operating system can take note.

A high performance PLL (phase-locked-loop) performs data separation for both Winchester and floppy disks. The loop locks the controller onto the serial bit stream so data can be correctly interpreted. The loop has been optimized for the best possible reading margins over a wide range of temperature and voltage variations.

The disk controller uses a PAL to encode and decode the data before writing or during reading. The serializer/deserializer (SERDES) provides parallel-to-serial conversion of data during write operations and vice versa during read operations. Drivers and receivers are installed



as needed to interface with the disk drive control and data signal lines.

The quarter-inch streaming tape drives uses an eight-bit parallel data bus to transfer data and commands. Handshake and status lines control the direction and type of information transmitted over the eight-bit data path. A PAL is programmed to handle transfer protocol while the DMA chip moves data between the tape interface and dual-port buffer during disk backup/restore. The controller is active during this time in handling data transfers between the disk and dual-port buffer.

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## 5. User Level Maintenance

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### 5.1. Introduction

This Chapter provides information on user-level maintenance of the DSD Multibus Disk Controller. Coverage includes troubleshooting and fault analysis, HyperDiagnostic routines, error codes, and customer service assistance.

The DSD Controller requires no adjustment in the field. User level maintenance is limited to the use of HyperDiagnostics to isolate any problem to the subsystem and then swapping the module at fault for a known good one. All subsystem modules can be readily removed and replaced without the need of special tools. Information on returning a product to the factory for repair is covered paragraph 5.4.

### 5.2. Troubleshooting and Fault Analysis

The following list of diagnostic tools is furnished to assist in the isolation of faults that may occur.

- Built-in self-tests
- Activity indicators on the controller module
- On-line or extended diagnostic routines
- Off-line HyperDiagnostics
- DSD Customer Service Hotline

The built-in self-tests, and the use of activity indicators CR1 (ERR), and CR2 (RDY), were described under Initial Checkout and Acceptance Tests, contained in Chapter 2. On-line or extended diagnostics are described under the diagnostic function command (ØFH), contained in Chapter 3.

### 5.3. Off-Line HyperDiagnostics

Jumper group W6, located at coordinate E5, enables and selects the off-line HyperDiagnostic test to be performed. This is a secondary function of W6. The jumper group must be restored to its standard configuration upon completion of testing.

Jumper W6-5 is used to enable the off-line diagnostics. The specific test to be performed is selected by jumpers W6-4 through W6-0. These jumpers represent a hexadecimal value with the least significant bit provided by W6-0 and the most significant bit by W6-4. An inserted jumper represents a value of 1 and an open jumper a value of 0.

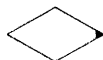
When testing has been enabled and selected by jumper group W6, a power-up, host bus INIT/signal, or a programmed reset and clear command through the wake-up I/O port causes the selected diagnostic to begin execution, see Figure 5-1.

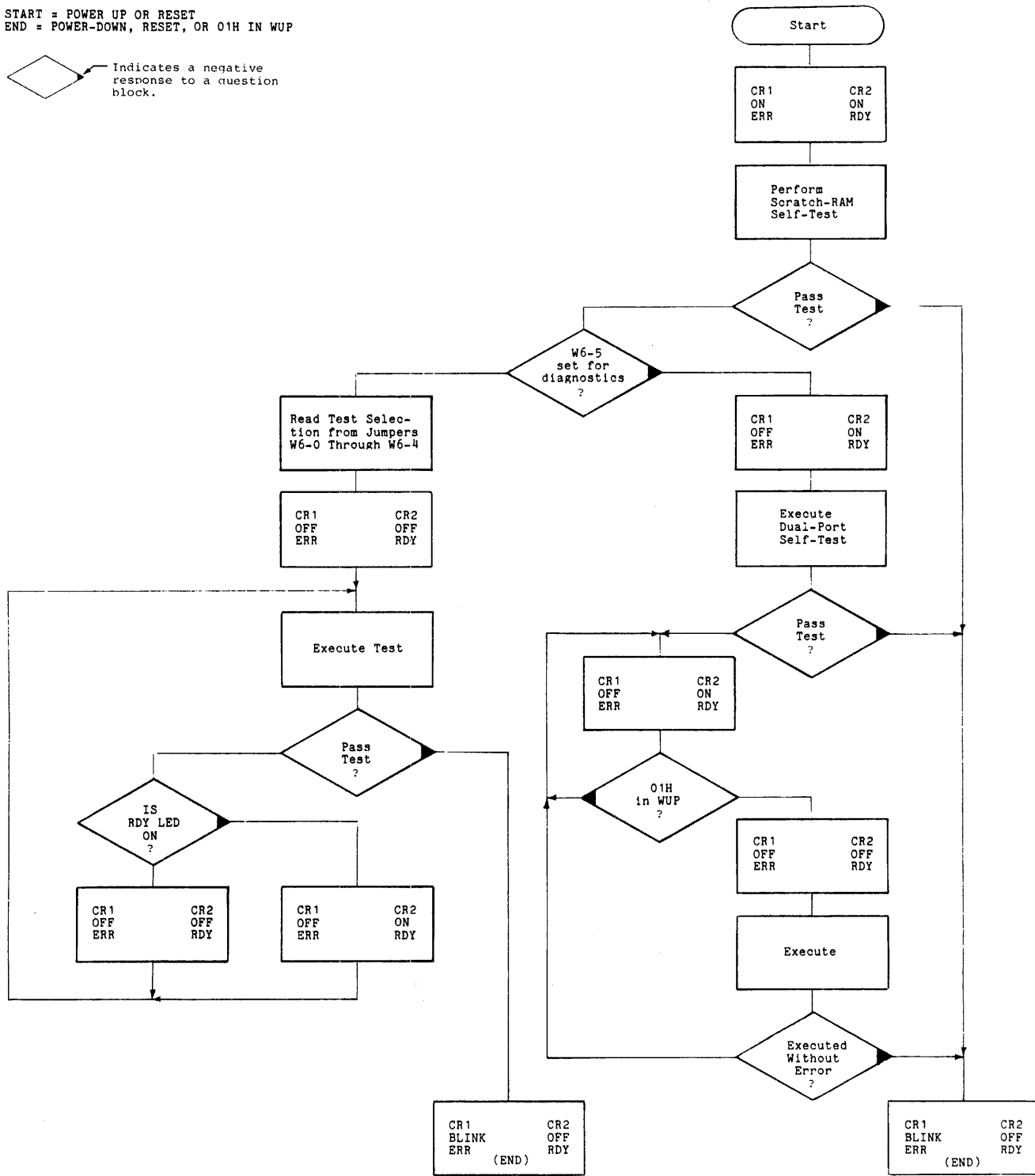
LEDs CR1 (ERR) and CR2 (RDY), mounted in the upper left hand corner on the component side of the controller board, indicate the status of the diagnostic test being performed. After the selected diagnostics begins, CR1 (ERR) and CR2 (RDY) turn OFF. When the test is completed with no errors, CR 2 (RDY) turns OFF. If no error is detected, the test continues indefinitely, with each successful pass of the diagnostic indicated by CR2 (RDY) changing state; OFF to ON, or ON to OFF.

If an error is detected during the execution of a diagnostic, the test halts and CR1 (ERR) blinks the appropriate error code. Refer to paragraph 5.3.1 for detailed information on blinking error codes and their interpretation.

A complete set of tests are provided for use in the off-line HyperDiagnostic mode. A detailed description of the individual test is provided after the table and includes the approximate time required to complete one pass of the selected test.

START = POWER UP OR RESET  
 END = POWER-DOWN, RESET, OR 01H IN WUP

 Indicates a negative response to a question block.



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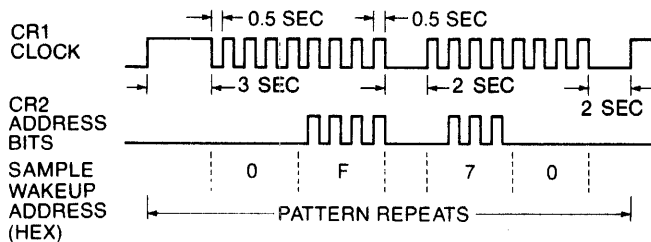
Figure 5-1. LED Indicator Sequence

Table 5-1. Off-Line HyperDiagnostics

Test (Hex)	Description	Jumper Group W6					
		Enable 5	MSB 4	3	2	1	LSB 0
1F	8085 environ- ment self-test	OUT	IN	IN	IN	IN	IN
1E	Factory use only	OUT	IN	IN	IN	IN	OUT
1D	Factory use only	OUT	IN	IN	IN	OUT	IN
1C	Factory use only	OUT	IN	IN	IN	OUT	OUT
1B	Read/write controller self-test	OUT	IN	IN	OUT	IN	IN
1A	CR1,CR2 Blink Wakeup Address Test	OUT	IN	IN	OUT	IN	OUT
19	Floppy Drive 0 Test	OUT	IN	IN	OUT	OUT	IN
18	Floppy Drive 1 Test	OUT	IN	IN	OUT	OUT	OUT
17	Winchester #0 Test	OUT	IN	OUT	IN	IN	IN
16	Winchester #1 test	OUT	IN	OUT	IN	IN	OUT
15	Tape Drive Test	OUT	IN	OUT	IN	OUT	IN
14	Stand-Alone System test	OUT	IN	OUT	IN	OUT	OUT
13	Host Bus Read/ Write test	OUT	IN	OUT	OUT	IN	IN

HyperDiagnostic routines in detail:

- 1F 8085 environment self-test: Tests 8085, PROM, RAM, two-port buffer, and DMAC independent of components in the read/write controller section of the board. Test takes approximately 45 seconds to complete one pass. CR2 (RDY) light toggles ON to OFF or OFF to ON to indicate completion of one pass.
- 1E Winchester PLL alignment: Factory use only.
- 1D Floppy double-density PLL alignment: Factory use only.
- 1C Floppy single-density PLL alignment: Factory use only.
- 1B Read/write controller self-test: Tests the read/write controller hardware without exercising the disk drive. Test 1F must be successfully completed prior to implementing this test. Test takes approximately one millisecond to complete one pass.
- 1A CR1, CR2, blinking wakeup address test: CR1 is the clock and CR2 represents the bits set by each of the 16 wakeup address jumpers settings. The test flashes through an eight-bit cycle, most significant bits first, waits two-seconds and then flashes the remaining eight bits, waits two-seconds and then loops to repeat the test. See timing diagram, Figure 5-2.



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Figure 5-2. CR1/CR2 Timing for Wake-Up Address Test

As shown in Figure 5-2, CR1 (clock) is on for three-seconds before beginning the first series of eight clock pulses. The bit value of CR2 is valid only when the clock (CR1) is high (ON). That is, if CR1 (clock) is ON and CR2 is OFF, the bit value is zero. Conversely, if CR1 and CR2 are both on, the bit value is one. Figure 5-2 shows the timing of a sample wakeup address of 0 F70 Hex. The test takes approximately 23 seconds to complete one pass.

- 19 Floppy drive 0 test: Test only if drive is physically present and media is installed and write-enabled. Operator should note that previous data stored on disk are destroyed during this test.

Test first homes the head to track zero, then seeks out 35 tracks, and returns to track zero. The test then performs a Read ID command, and writes 16 double-density (256-bytes per sector) sectors with a double incrementing pattern. Sector one is written in pattern 0, 1 thru 255. Each successive sector adds one to content of each byte. Therefore, sector two is written as 1, 2 thru 255, 0; sector 16 as 15, 16 thru 255, 1 thru 14. The test then reads and verifies the patterns. The test takes approximately nine seconds to complete one pass. tests 1F and 1B must first have been completed successfully prior to implementing this test.

- 18 Floppy drive 1 test: Exactly the same as test 19, if drive 1 is physically present.

- 17 Winchester drive 0 test: This test will fail if the Winchester has not been formatted.

Test first homes the head to track zero, then seeks out 128 tracks and returns to track zero. The test then performs a Read ID command to determine sector size, and then reads sectors 0 through 3 on head 0 for 3 cylinders and checks for ECC errors. Test takes approximately four seconds to complete one pass. Tests 1F and 1B must first have been completed successfully prior to implementing this test.

- 16 Winchester drive 1 test: Exactly the same as test 17, if second drive is physically present.

- 15 Tape drive test: Test only if drive is physically present and cartridge is installed and write-enabled. Note that any previous data stored on tape are destroyed during this test.

Test first retensions the tape cartridge (approximately two minutes), then writes two tracks with a double incrementing pattern from the buffer (another two minutes) and then reads and verifies the two tracks written (final two minutes of test). Test 1F

must first have been successfully completed prior to implementing this test. Test takes approximately six to eight minutes.

- 14 Standalone system test: Note that this test will destroy any data not previously stored on floppy disks.

Test runs diagnostics 1F, 1B, 19, 18, 17, 16, and 15 sequentially, if all drives are physically present.

Error 47 indicates that the controller recognizes no drives as present, and either the drives are malfunctioning or the cabling between drives and controller is not correct. Time for one complete pass of standalone system test depends upon the number of drives present in the system.

- 13 Host Bus Read/Write Test: Test writes and reads host bus memory 000000 Hex to 000FFF Hex using DMA. Memory must exist from 000000 Hex to 000FFF Hex, and BPRN/(host bus pin P1-15) must be low giving the controller bus priority. No CPU is required. First pass of this test has a three second ready time and then two-second run time. Each successive pass of this test takes two-seconds. Test 1F must first have been completed successfully prior to implementing this test.

### 5.3.1. HyperDiagnostics and Error Code Interpretation

To initiate the off-line HyperDiagnostics proceed as follows:

- (1) With the power OFF, remove the DSD controller board from the host backplane.
- (2) Reconfigure jumper group W6 as shown in table 5-1.
- (3) Reinstall the controller card in the host backplane and apply power in the host computer.
- (4) Selected diagnostic begins with application of power with each successful pass of the test indicated by CR2 (RDY) changing state (OFF to ON, or ON to OFF). The test continues until halted by the user. See Figure 5-3.

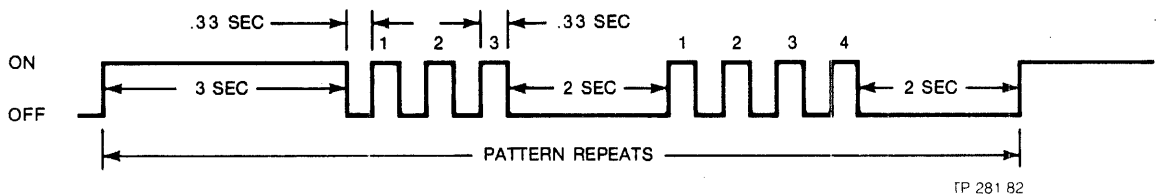
To halt the continuous repeating sequence of the successful diagnostic, remove power from host computer, reconfigure jumper W6 to select drive types used in system (Refer to section 2 for drive type select information), and reinstall controller in backplane.

If an error is encountered during any HyperDiagnostic test, the test will halt, CR2 (RDY) will be OFF, and CR1 (ERR) will begin blinking the error code. Figure



5-3 illustrates the sequence of R1 (ERR) while blinking an error code.

Figure 5-3 shows the on/off sequence of CR1 (ERR) blinking error code 34 Hex. The sequence start is indicated by CR1 (ERR) being on for three-seconds. CR1 then begins a series of short pulses (three in this example) to indicate the first digit of the error code. A two-second off time signals completion of first digit. Then CR1 (ERR) begins a second series of short pulses to indicate the remaining digit and another two-second off time. The pattern then repeats. The sequence can be halted by removing power, or by initiating another diagnostic test. The blinking error codes of CR1 (ERR) are the same error codes reported by the extended status-byte in the error status buffer (Refer to section 4).



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Figure 5-3. CR1 Blinking Error Code

#### 5.4. Maintenance Assistance

Data Systems Design maintains a fully staffed Customer Service Department. If at any time during inspection, installation, or operation of the equipment you encounter a problem, contact one of these offices. Our trained staff can help you diagnose the cause of failure, and, if necessary speed replacement parts to you. Any time you need to return a product to the factory, please contact Customer Service for a Material Return Authorization Number.

#### Data Systems Design Customer Service:

WESTERN REGION  
Sales and Service  
2241 Lundy Avenue  
San Jose, CA 95131  
(408) 946-5800  
TWX: 910-338-0249

CENTRAL REGION  
Sales and Service  
5050 Quorum Drive  
Suite 339  
Dallas, TX 75240  
(214) 980-4884

EASTERN REGION  
Sales and Service  
51 Morgan Drive  
Norwood, MA 02062  
(617) 769-7620  
TWX: 710-336-0120

NORTH CENTRAL REGION  
Sales and Service  
2311 West 22nd St.  
Suite 110  
Oakbrook, IL 60521  
(312) 920-0444

For products sold outside the United States, contact your local DSD distributor for parts and customer service assistance.



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Appendix A: Specifications

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Table A-1. General Specifications

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Mounting: Occupies one card slot in a Multibus-compatible backplane.

Dimensions: 0.6" thick x 12.0" long x 7.1" wide (1.5 cm thick x 30.5 cm long x 18.0 cm wide)

Supply Voltages: + 5 Vdc, + 5% @ 5.1 Amp typical  
+12 Vdc,  $\pm$  5% @ 0.1 Amp typical

Table A-2. Environmental Specifications

---

Operating Temperature: 41 deg. F to 131 deg. F (5 deg. C to 55 deg. C)

Humidity: Up to 90% noncondensing

Cooling: The controller dissipates 24 W of heat (80 BTU/hr). Sufficient air circulation must be maintained to prevent temperatures above 131 deg. F (55 deg. C).

Table A-3. Host Bus Interface Specifications

---

Multibus Compatible  
 Backplane (IEEE P796): Master D16M24  
 Slave D8I16VOEL

I/O Address: 8- or 16-bit (User-Selectable)

Data Transfers: 8- or 16-bit (User-Selectable)

Memory Addressing: 20- or 24-bit (User-Selectable)

Bus Arbitration Modes:
 

- Single Transfer
- Yield to Any Request
- Yield to Higher Priority
- Override

 (Jumper-Selectable)

Interrupts: host bus lines INT0/ to INT7/  
 (Interrupt output jumper-selectable)

Bus Usage During Direct Memory Access

Reading From Bus: 0.9 microseconds plus memory-read  
 access time per word.

Writing to Bus: 0.5 microseconds plus memory-write  
 access time per word.

Table A-4. Drive Interface Specifications

Data Transfer Rates

Winchester:
 

- Within a sector: 625 Kbytes/sec
- Within a cylinder: 529 Kbytes/sec
- Across entire disk: 410 Kbytes/sec

 (Noninterleaved format, 1024-bytes per  
 sector, eight tracks per cylinder).

Floppy: ● 31.25 Kbytes/sec (256-byte sectors)

Error Detection and Correction

Floppy and Tape: CRC checksum

Winchester:
 

- 32-bit ECC polynomial
  - 22-bit burst error detection
  - 11-bit burst error correction

Activity Lights: Two LED indicators  
 (also used by HyperDiagnostics)

Table A-5. Supported Winchester Drive Formats

---

Recording Method:	Modified Frequency Modulation			
Data Bytes per Sector:	128	256	512	1024
Sectors per Track:	54	31	17	9

Table A-6. Supported Floppy Drive Formats

Recording Methods

Single-Density: Frequency Modulation

Double-Density: Modified Frequency Modulation

Sectors per Track

Data Bytes per Sector:	128	256	512	1024
• Single-Density:	26	15	8	4
• Double-Density:	-	26	15	8

Table A-7. Supported Streaming Tape Drive Format (QIC-02)

QIC-02 Recording Format

Tracks: Four (serpentine)

Density: 8,000 bits per inch  
(10,000 flux reversals per inch)

Transfer Rate: 87 Kbytes per second

Bytes per Block: 528.5 (divided into five block fields)

QIC-02 Block Fields

Gap:	13.0-bytes
Sync Mark:	0.5-byte
User Data:	512.0-bytes
Block Address:	1.0-byte
CRC:	2.0-bytes

### A.1. Cables and Connectors

Figure A-1 shows all connector and cabling requirements. The connectors are wired pin-to-pin: a given pin on both connectors always carries the same signal. The female connectors used with J1 through J4 are with 1/10-inch pin spacing. The connectors and cables are summarized in Table A-8.

Table A-8. Controller Connectors and Cables

---

#### Host Bus Connectors

- P1: 86-pin, double-sided, printed circuit edge connector.
- P2: 60-pin, double-sided, printed circuit edge connector; the P2 signals are not used.

#### Tape Drive Connector

- J1 (50-pin):  
Maximum allowable length for the tape drive cable is 32 feet (ten meters).

#### Winchester Drive Connectors

- J2A (34-pin control connector):  
The maximum allowable length for the control cable is 20 feet (six meters).
- J3 and J4 (20-pin data connectors):  
Connectors J3 and J4 are identical and interchangeable. The maximum allowable length for the data cable is 20 feet (six meters).

#### Floppy Drive Connector

- J2B (50-pin):  
The maximum allowable length for the floppy drive cable is 32 feet (ten meters).
-

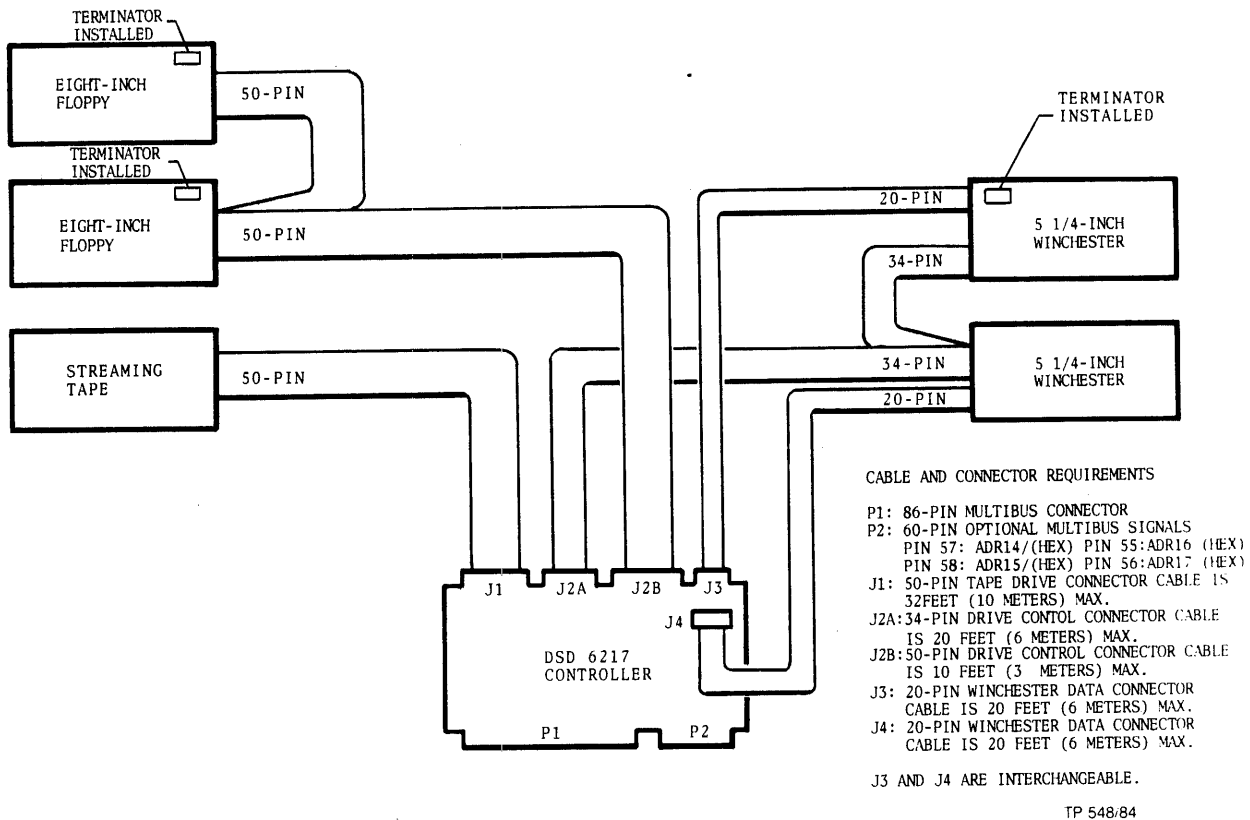


Figure A-1. Cables and Connectors



A.1.1. Host Bus/Controller Interface: Connectors P1 and P2

Table A-9 and A-10 list the host bus connector pin assignments. Table A-11 describes the host bus/controller interface signals on P1. Figure A-2 is a diagram of the host bus/controller interface timing signals with timing requirements. The controller is connected to the host bus interface through connector P1, an 86-pin, double-sided, printed circuit edge connector. Connector P2 provides for optional host bus signals, as listed in Table A-9.

Table A-9. Host Bus P2 Connector Pin Assignment

Pin	Signal Name	Pin	Signal Name
55	ADR16/(Hex)	56	ADR17/(Hex)
57	ADR14/(Hex)	58	ADR15/(Hex)

Connector P2 is not used

Table A-10. Host Bus P1 Connector Pin Assignment

Component Side		Circuit Side	
Pin	Signal	Pin	Signal
<u>Power Supplies</u>			
1	GND	2	GND
3	+ 5Vdc	4	+ 5Vdc
5	+ 5Vdc	6	+ 5Vdc
7	+12Vdc	8	+12Vdc
9	Reserved	10	Reserved
11	GND	12	GND
<u>Bus Controls</u>			
13	BCLK/	14	INIT/
15	BPRN/	16	BPRO/
17	BUSY/	18	BREQ/
19	MRDC/	20	MWTC/
21	IORC/	22	IOWC/
23	XACK/	24	INH1/
25	Reserved	26	Reserved
27	BHEN/		
29	CBRQ/		
31	CCLK/		
<u>Address Bus</u>			
		28	ADR10/
		30	ADR11/
		32	ADR12/
		34	ADR13/

----- (Continued) -----

Table A-10. Host Bus Pl Connector Pin Assignment

Component Side		Circuit Side	
Pin	Signal	Pin	Signal
<u>Interrupts</u>			
33	INTA/		
35	INT6/	36	INT7/
37	INT4/	38	INT5/
39	INT2/	40	INT3/
41	INT0/	42	INT1/
<u>Address Bus</u>			
43	ADR0E/	44	ADR0F/
45	ADR0C/	46	ADR0D/
47	ADR0A/	48	ADR0B/
49	ADR08/	50	ADR09/
51	ADR06/	52	ADR07/
53	ADR04/	54	ADR05/
55	ADR02/	56	ADR03/
57	ADR00/	58	ADR01/
<u>Data Bus</u>			
59	DATE/	60	DATF/
61	DATC/	62	DATD/
63	DATA/	64	DATB/
65	DAT8/	66	DAT9/
67	DAT6/	68	DAT7/
69	DAT4/	70	DAT5/
71	DAT2/	72	DAT3/
73	DAT0/	74	DAT1/
<u>Power Supplies</u>			
75	GND	76	GND
77	Reserved	78	Reserved
79	Reserved	80	Reserved
81	+5Vdc	82	+5Vdc
83	+5Vdc	84	+5Vdc
85	GND	86	GND

Slash ("/") following the signal name indicates an active low.

Table A-11. Host Bus Pl Signals

<u>Signal</u>	<u>Description</u>
ADR00/-ADR0F/ ADR10/-ADR13/	<u>Address</u> . These 20 lines transmit the address of the memory location or I/O port to be accessed. For memory access, ADR00/ (when active) enables the even-byte bank (DAT00/-DAT07/) on the host bus; i.e., ADR00/ is active for all even addresses. ADR13/ is the most significant address bit.
BCLK/	<u>Bus Clock</u> . Used to synchronize the bus contention logic on all bus masters.
BHEN/	<u>Byte High Enable</u> . When active low, enables the odd-byte bank (DAT8/-DATE/) onto the host bus connector.
BPRN/	<u>Bus Priority In</u> . When low, indicates to a particular bus master that no higher priority bus master is requesting use of the bus. BPRN/ is synchronized with BCLK/.
BPRO/	<u>Bus Priority Out</u> . In serial (daisy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	<u>Bus Request</u> . In parallel priority resolution schemes, BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	<u>Bus Busy</u> . Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	<u>Common Bus Request</u> . Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, the requesting bus controller raises the CBRQ/ signal to the inactive high state.

----- (Continued) -----

Table A-11. Host Bus Pl Signals

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(Continued) -----

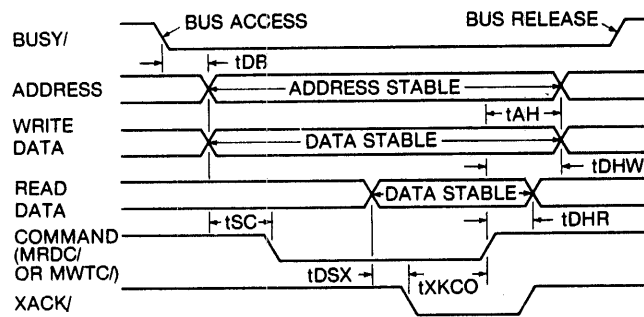
DAT0/-DATF/	<u>Data</u> . These 16 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DATF/ is the most significant bit. For data-byte operations, DAT0/-DAT7/ is the even byte and DAT8/-DATF/ is the odd byte.
INIT/	<u>Initialize</u> . Resets the entire system to known internal state.
INT0/-INT7/	<u>Interrupt Request</u> . These eight lines transmit interrupt requests to the appropriate interrupt handler. INT0/ has the highest priority.
IOWC/	<u>I/O Write Command</u> . Indicates that the address of an I/O port is on the host bus connector address lines and that the contents on the host bus connector data lines are to be accepted by the addressed port.
MRDC/	<u>Memory Read Command</u> . Indicates that the address of a memory location is on the host bus connector address lines and that the contents of the location are to be read (placed) on the host bus connector data lines.
MWTC/	<u>Memory Write Command</u> . Indicates that the address of a memory location is on the host bus connector address lines and that the contents on the host bus connector data lines are to be written into that location.
XACK/	<u>Transfer Acknowledge</u> . Indicates that the address memory location has completed the specified read or write operation. That is, data has been placed onto or accepted from the host bus connector data lines.

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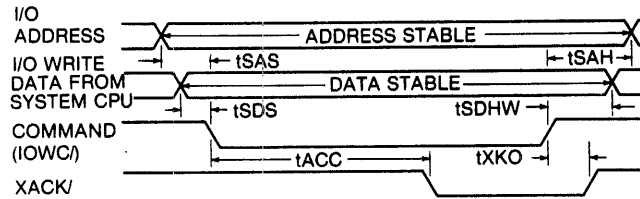
Table A-12. Host Bus Pl Connector Timing Signal Descriptions

Parameter	Nanoseconds		Description
	Min	Max	
tDB		61	Busy-to-address/data delay
tSC	60		Address/data set-up to CMD
tXKCO		500	XACK/ to CMD turn-off
tAH	50		Address hold time
tDHW	50		Data hold time
tDHR	0		Read data hold time
tDSX	0		Data set-up time before XACK/
tSAS	23		Address set-up time to I/O CMD
tSDS	32		Data set-up time to I/O CMD
tSAH	36		Address hold time from I/O CMD
tSDHW	50		Data hold time from I/O CMD
tACC		77	I/O access time
tXKO	10	63	XACK/ hold time from I/O CMD
tBCY	100		Bus clock cycle time
tBL	35	65	Bus clock low
tBH	35	65	Bus clock high
tDRQ		32	Bus request delay
tDBY		48	Bus busy turn on delay
tDBYF		65	Bus busy turn off delay
tDBPN	0		Priority input set-up time
tDBPO		7	BPRO/ serial delay from BPRN/
tWait		Infinity	Requesting master bus access time

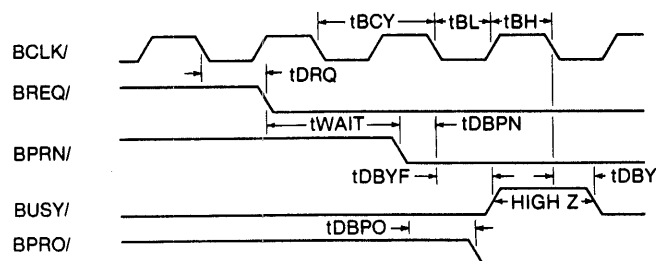
MASTER COMMAND ACCESS TIMING



SLAVE COMMAND TIMING



BUS EXCHANGE TIMING



TP 253/82

Figure A-2. Host Bus Pl Connector Timing Diagrams

### A.1.2. Controller/Drive Interface: Connectors J1 Through J4

Connectors J1, J2A, J2B, J3, and J4 are mounted on the component side of the board. An embossed arrow indicates pin 1. The odd-numbered pins of these connectors are the upper row of pins.

The drive connectors are:

- J1
  - 50-pin
  - Streaming tape drive control and data
  - See Table A-13
- J2A
  - 34-pin
  - Winchester drive control
  - See Table A-14
- J2B
  - 50-pin
  - Floppy drive control and data
  - See Table A-15
- J3 and J4
  - 20-pin
  - Interchangeable Winchester drive data
  - See Table A-16

Table A-13. Tape Drive Control Connector J1

Pin	Signal	Description
2,4,6,8,10		Reserved.
12	HB7/	<u>Host Bus Bit 7.</u> MSB of eight-bit bidirectional data bus.
14	HB6/	<u>Host Bus Bit 6.</u>
16	HB5/	<u>Host Bus Bit 5.</u>
18	HB4/	<u>Host Bus Bit 4.</u>
20	HB3/	<u>Host Bus Bit 3.</u>
22	HB2/	<u>Host Bus Bit 2.</u>
24	HB1/	<u>Host Bus Bit 1.</u>
26	HB0/	<u>Host Bus Bit 0.</u> LSB of eight-bit bidirectional data bus.
28	ONL/	<u>On-Line.</u> Transition to active low terminates a read/write operation and returns tape to BOT.
30	REQ/	<u>Request.</u> Transition to active low informs tape drive controller that a command is on the data bus. Also used to handshake status information from tape drive controller to 6217.
32	RES/	<u>Reset.</u> Transition to active low after power-up initializes tape drive and tape drive controller, and puts the tape cartridge into a known configuration.
34	XFER/	<u>Transfer.</u> Host handshake signal to transfer data to and from tape drive. During read operation, XFER transition to active low means 6217 has received data. During write, XFER transition to active low means 6217 has put data on bus.

(Continued)



Table A-13. Tape Drive Control Connector J1

----- (Continued) -----		
Pin	Signal	Description
-----		
36	ACK/	<u>Acknowledge</u> . Handshake signal to transfer data to and from tape drive. During read, transition to active low means data is available on bus for 6217. During write, transition to active low means data has been received by the tape drive controller.
38	RDY/	<u>Ready</u> . 1. Active low indicates tape drive controller can accept new command. 2. During command transfer, transition to active low means command has been read. 3. Used to signal asynchronous transfer of status information from tape drive controller to 6217. 4. Used to indicate that a block of data is ready to be transferred.
40	EXC/	<u>Exception</u> . Used by tape drive controller to inform the 6217 of a condition which has terminated an operation. Upon transition to active low, the 6217 must respond with a read status function.
42	DIR/	<u>Direction</u> . Used by 6217 to indicate the direction of data flow on the data bus (HB0/ through HB7/). When active low, flow of data is from tape drive controller to 6217.
44,46,48,50		Reserved.

-----  
All odd-numbered pins, 1-49, are at signal ground.

Table A-14. Winchester Drive Control Connector J2A

Pin	Signal	Description
2	RWC/, or HS2 <sup>3</sup> /	This pin carries two signals, determined by whether the drive is in write or read mode.  <u>Reduce Write Current.</u> Active low selects a lower write current value.  <u>Head Select Line (2<sup>3</sup> bit).</u> For class 5 or higher Winchester drives that do not require reduced write current.
4	HS2 <sup>2</sup> /	<u>Head Select Line (2<sup>2</sup> bit).</u>
14	HS2 <sup>0</sup> /	<u>Head Select Line (2<sup>0</sup> bit).</u>
18	HS2 <sup>1</sup> /	<u>Head Select Line (2<sup>1</sup> bit).</u>
6	WG/	<u>Write Gate.</u> When active low, enables write-data to be written to disk. When high, enables transfer of data from drive to 6217, and enables step pulses to reposition head arm.
8	SKCOMP/	<u>Seek Complete.</u> Active low when heads are settled on final track at completion of a seek.
10	TRK000/	<u>Track 000.</u> Active low only when heads are at track zero.

----- (Continued) -----

Table A-14. Winchester Drive Control Connector J2A

Pin	Signal	Description
12	WTFLT/	<u>Write Fault</u> . Indicates that a drive condition exists which could cause improper writing on disk. Occurs when there is write current in the head without write gate active or when multiple heads have been selected.
16		Reserved.
20	INDEX/	<u>Index</u> . Drive provides this signal once per revolution to indicate the beginning of track.
22	RDY/	<u>Ready</u> . When Active low, together with seek-complete, indicates drive is ready to read, write, or seek, and that the signals are valid.
24	STEP/	<u>Step</u> . Causes heads to move as defined by "Direction" (line 34).
26	DS1/	<u>Drive Select 1 and Drive Select 2</u> . When active low, connects the selected drive to the control lines. Only one of these lines may be active at a time.
28	DS2/	
30,32		Reserved.
34	DIRC/	<u>Direction</u> . Active low causes the heads to move toward the center when line 24 (STEP) is pulsed.

-----  
 All odd-numbered pins, 1-33, are at signal ground.

Table A-15. Floppy Drive Control Connector J2B

<u>Pin</u>	<u>Signal</u>	<u>Description</u>
2	RWC/, or ARC/	<p>This pin is used for two signals, selectively enabled by write or read mode.</p> <p><u>Reduce Write Current.</u> Active low selects lower write current during write mode when writing to tracks 43 through 76.</p> <p><u>Active Read Compensation.</u> Active low causes the data to be passed through an active filter network during read mode when reading tracks 60 through 76.</p>
12	DC/	<u>Disk Change.</u> Active low indicates that a media change was detected while the drive was de-selected.
14	SS/	<u>Side Select.</u> Active low selects side 1 on a double-sided drive. Inactive state selects side 0.
18	HL/	<u>Head Load.</u> Active low loads the heads against the diskette if the access door is closed.
20	INDEX/	<u>Index.</u> Active low indicates detection of physical index on diskette. Occurs once per diskette revolution.
22	RDY/	<u>Ready.</u> Active low indicates that two index holes have been detected (three on a double-sided diskette), and that the drive is ready for read or write operations.
26 28	DS1/ DS2/	<u>Drive Select 1 and Drive Select 2.</u> Active low selects a drive. Only one of these lines may be active at a time.
34	DIRC/	<u>Direction Select.</u> Active low causes the heads to move toward the center when pin 36 (STEP) is pulsed.
36	STEP/	<u>Step.</u> Causes heads to move as defined by "Direction" (pin 34).

(Continued)

Table A-15. Floppy Drive Control Connector J2B

----- (Continued) -----		
<u>Pin</u>	<u>Signal</u>	<u>Description</u>
38	WR DATA/	<u>Write-Data</u> . Each transition to active low causes a data bit to be written. Enabled by write gate (pin 40).
40	WG/	<u>Write Gate</u> . Active low enables write-data (pin 38). Inactive state enables read-data (pin 46).
42	TRK00/	<u>Track 00</u> . Active low indicates that the heads are at track 00 (outermost).
44	WP/	<u>Write Protected</u> .
46	RD DATA/	<u>Read-Data</u> . Each transition to active low represents a raw data bit (data read off the disk, unseparated from the clock signal).

Table A-16. Winchester Data Connectors J3 and J4

<u>Pin</u>	<u>Signal</u>	<u>Description</u>
1	DS/	<u>Drive Select</u> . When active low, the selected drive is connected to the I/O lines.
13	+WR DATA/	<u>+Write-Data</u> . Defines bits written to disk.
14	-WR DATA/	<u>-Write-Data</u> . Defines bits written to disk.
17	+RD DATA/	<u>+Read-Data</u> . Data recovered by reading disk.
18	-RD DATA/	<u>-Read-Data</u> . Data recovered by reading disk.

-----  
 J3 and J4 have identical pinouts and are interchangeable. Pins 2, 4, 6, 8, 11, 12, 15, 16, 19, and 20 are at signal ground. Pins 3, 5, 7, 9, and 10 are spares.

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Appendix B: Supported Disk Drive Jumper Configurations

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This Appendix provides drive jumper information for those drives supported by the controller. Each drive type has a table that shows each jumper, its description, and the required configuration for proper disk system operation. Tables included are:

- Table B-1: SA800/801 Floppy Drives (single sided)
- Table B-2: SA850/851 Floppy Drives (double-sided)
- Table B-3: CDC-9406-4 Floppy Drives (double-sided)
- Table B-4: ST412 Winchester Drives
- Table B-5: One and Two Drive System Configurations

Note that there are no drive jumper options for the streaming tape drive. Jumpers are factory set for the tape drive and the user MUST leave them as set for proper operation.

Table B-1. SA800/801 Drive Jumper Configuration

Drive 0 Jumper Settings	Description	Required Setting	
		In	Out
T1	Termination, head load		X
T2	Termination, drive select	X	
T3, T4, T5, T6	Termination, other		X
DS1, DS2, DS4	Drive selects 1, 2, 4		X
DS3	Drive selects 3	X	
RR	Radial ready	X	
R1	Radial index and sector	X	
R, I, S	Radial, index, and sector output	X	
HL	Stepper power from head load		X
DS	Stepper power from drive select	X	
WP	Inhibit write when write-protected	X	
NP	Allow write when write-protected		X
8, 16	SA801 Only		X
32	SA801 Only	X	
D	Alternate input - in use		X
2, 4, 6, 8, 10, 12, 14, 16, 18	Nine alternate I/O pins		X
D1, D2, D4, DDS	Decode drive select options		X
A, B	Head load on drive select	X	
X	Head load on drive select		X
C	Alternate input head load	X	
Z	In use from drive select	X	
Y	In use from head load		X
DC	Alternate output - disk change	X	
Drive 1 Differences			
DS1, DS2, DS3	Drive selects 1, 2, 3		X
DS4	Drive select 4	X	

Table B-2. SA850/851 Drive Jumper Configuration

Drive 0 Jumper Settings	Description	Required Setting	
		In	Out
3H DIP	Termination for standard inputs		X
DS1, DS2, DS4	Drive selects 1, 2, 4		X
DS3	Drive select 3	X	
1B, 2B, 3B, 4A	Side select option using drive select		X
RR	Radial Ready	X	
RI	Radial index and sector	X	
R(4H-7)	Shunt for ready operation	X	
2S	Two-sided status output	X	
850	Sector option enable	X	
851	Sector option enable		X
I(4H-6)	Shunt index output	X	
S(4H-8)	Shunt sector output (cut trace)		X
DC	Disk change	X	
HL(4H-2)	Shunt stepper power from head load (cut trace)		X
DS	Stepper power from drive select	X	
WP	Inhibit write when write-protected	X	
NP	Allow write when write-protected		X
D	Alternate input - in use		X
DD	Standard drive select enable	X	
DL	Door lock latch option	X	
A(4H-3)	Shunt radial head load	X	
B(4H-4)	Shunt radial head load	X	
X(4H-5)	Shunt radial head load (cut trace)		X
C	Alternate input head load	X	
Z(4H-1)	Shunt in-use from drive select	X	
Y	In use from head load		X
S1	Side select option using direction select		X
S2	Standard side selection input	X	
S3	Side select option using drive select		X
TS, FS	Data separation option select		X
IW	Write current switch	X	
RS	Ready standard	X	
RM	Ready modified		X
HLL	Head load latch		X
IT	In use terminator		X
HI	Head load or in use to the in use circuit		X
AF	FM or MFM encoding	X	
NF	M <sup>2</sup> FM encoding		X
Drive 1 Differences			
DS4	Drive select 4	X	
DS1, DS2, DS3	Drive selects 1, 2, 3		X



Table B-3. CDC-9406-4 Drive Jumper Configuration

Switch Number	Function	Required Setting	
		On	Off
S1-1	A	X	
S1-2	B	X	
S1-3	X		X
S1-4	Z	X	
S1-5	RR	X	
S1-6	I	X	
S1-7	R	X	
S1-8	RI	X	
S1-9	WP	X	
S1-10	CC	X	
S2-1	DD	X	
S2-2	HO	X	
S2-3	MM		X
S2-4	S2	X	
S2-5	LC	X	
S2-6	Y		X
S2-7	S2	X	
S2-8	C	X	
S3-1	DL	X	
S3-2	D		X
S3-3	IU		X
S3-4	S1		X
S3-5	S3		X
S3-6	DC	X	
S3-7	DR		X
S3-8	--	-	-
S4-1	DS1		X
S4-2	DS2		X
S4-3	DS3	On for Drive 0	
S4-4	DS4	On for Drive 1	
S5-1	4B		X
S5-2	3B		X
S5-3	2B		X
S5-4	1B		X

Table B-4. ST412 Winchester Drive Jumper Configuration

Trace Designator	Description	Required Setting	
		In	Out
R	Radial option		X
DS1, 2, 3, 4	Drive select	Table B-3	
6F DIP	Terminator for Standard Inputs	Table B-3	

An Option Shunt Block is provided at IC position 6E on the ST412 (terminator block is adjacent at location 6F). The 14-pin shunt block (16-pin socket) is plugged in pins 2 through 15, leaving pins 1 and 16 open.

--U--		
1	R	16
2	NC	15
3	NC	14
4	NC	13
5	DS4	12
6	DS3	11
7	DS2	10
8	DS1	9

Table B-5. One and Two Drive System Configurations

	Drive Select				Terminator
	1	2	3	4	
One Drive Systems:					
	IN	OUT	OUT	OUT	IN
Two Drive Systems:					
Drive 1	IN	OUT	OUT	OUT	OUT
Drive 2	OUT	IN	OUT	OUT	IN