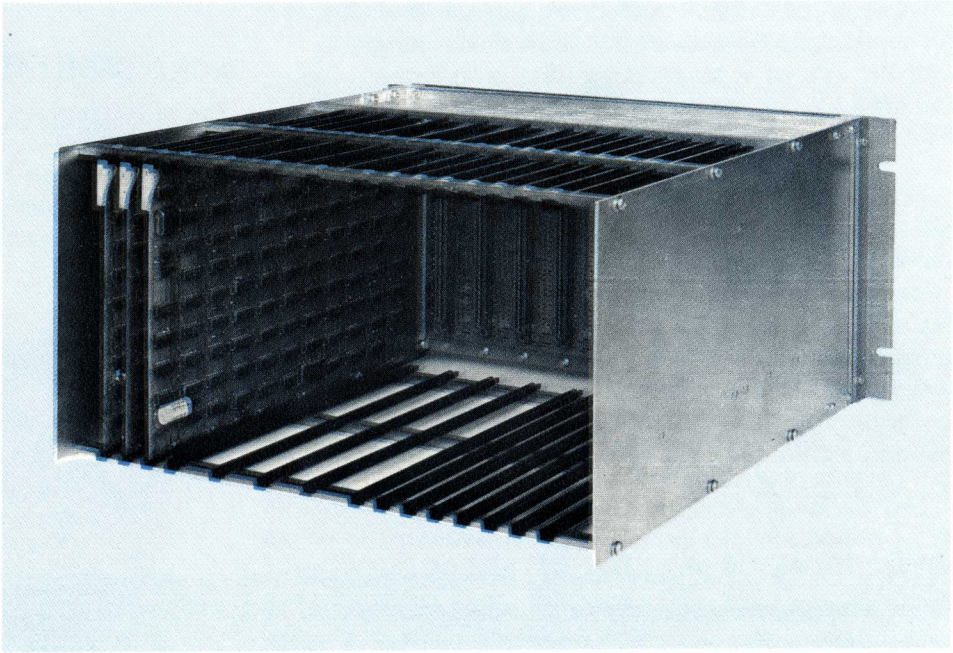
MODEL ee200

Easily Expandable

A VIEW FROM THE BACK OF THE BUS

Of course you could put the rack ears on the other end and then you would have a view from the front of the bus. We just wanted to choose a view which would show some of the advanced thinking which went into the ee 200 as exemplified by:



ELDORADO'S ANSWER TO BUSSING—A UNIVERSAL BUS

The universal bus is utopia to a systems integrater. It allows him to intermix memories, peripherals or read only memory with no thought about neighborhood or which device is next door. The peripherals can communicate indiscriminately with memory and each other without consulting the CPU since all are on the same bus. Therefore, all 12 slots that you see in the picture are for your specific needs. The minute you need it, you can plug in additional memory and I/O controllers without regard to sequence or location. This means easy expandability.

VERTICAL RUNNING BOARDS

Sounds like a little thing, but it isn't. Vertical mounting lets convection do the cooling and it's lots quieter and less expensive than a fan. And cooler components mean longer life—since all components operate at derated levels, we mean much longer life. In addition, the board size allows the average interface to have approximately 100 integrated circuits on one board which minimizes interconnections between peripherals and the computer. This means ready reliability.

THE BUS DRIVER

See those three boards seated on the left? They comprise the complete central processing unit and bus controller. And what a CPU it is! It's faster than a greyhound, with a 5MHz clock and 8, 16 and 24 bit instructions. And it responds quickly and automatically with 16 levels of priority interrupt; each level has 8 general purpose 16-bit registers—which allows real time and multiprocessing through one computer. Further, a stack pointer allows complete re-entry according to subroutine during interrupts. Because the CPU is controlled by memory for I/O speeds, asynchronous memories and peripherals can be used. Therefore, memory can range from microsecond core to nanosecond bi-polar and these memories can be interchanged and field alternated with no programming changes. This means valuable versatility.

LOADING THE BUS

An automatic bootstrap loader and a serial interface for an ASR-33/35 teletypewriter are included in the standard ee 200. The basic bootstrap and teletype loader routines are built into the ee 200 hardware. At long last, something for nothing.

PROJECT HEADSTART—TEACHING THE ee 200

The ee 200 features the most extensive address modification capability of any mini. The machine accepts relative addressing, 65k direct addressing, indexed addressing, indexed addressing plus displacement, and indexed with displacement at an automatic increment and decrement index register. There are 69 basic commands and thousands of permutations of each. All peripheral devices are assigned addresses and any peripheral device can input and output any one of the above addressing modes. In a real time environment, the hardware automatically keeps track of your interrupt level and automatically switches from one interrupt level to another, via a single instruction. And that's saying a lot.

THE FLUENTLY MULTILINGUAL MACHINES

The ee 200 understands a large number of languages. Several assemblers are available. Some are written in Fortran, the Eldorado String Processor and a standard Basic interpreter. There is a comprehensive debugging and diagnostic set. Whatever your language background, the ee 200 will feel like home. Now that's the end of the rap gap.

IN FACT, THAT'S THE END OF THE RAP.

Please turn the page for full specifications on the remarkable ee 200.

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The ee 200 Computer

The ee 200 presents a concept in computer architecture—a concept so flexible, so versatile that the user has unmatched advantages in his ability to tailor a computer to his individual requirements, in the ease of modifying the computer in the field and—last, but not least—in the significant cost savings.

UNIVERSAL BUS CONSTRUCTION

Keystone of the ee 200's organization is its Universal Bus construction. This results in a basic, simple, powerful computer without an ounce of unnecessary hardware. You don't pay for options—or the circuitry to support them—until you actually need them.

The "basic" ee 200 consists of an enclosure (ready for rack mounting) with an operating console, three circuit boards containing the entire central processor, 12 positions for memory and input/output device controllers. The Universal Bus concept is so straightforward that additional memory and peripheral controllers, on the same size circuit boards, and using the same size connectors, can be plugged into any position without regard to sequence or combinations.

ASYNCHRONOUS MEMORY INTERFACE

An asynchronous memory interface allows you to select various combinations of memory size and speed. For example, intermixing of high speed register files with 400 nanosecond MOS memory modules, a 1.2 microsecond core memory and read-only memories of any capacities. Since instruction execution time is directly related to memory cycle time, desired processor speed can be achieved by the memory selection. Thus, a 16-bit add operation can range from 9.6 microseconds using core memory to 2.0 microseconds using a 200 nanosecond file memory.

The asynchronous nature of the memory interface also means that newer and/or faster types of memories which may be available in the future can be used by simply mounting them on a standard ee 200 circuit board.

DYNAMIC REGISTER ALLOCATION

Handling a real-time environment involves rapid context switching; e.g., moving from one process to another with a minimum of overhead in time and instructions.

Multiple sets of registers provide unusually efficient interrupt processing, eliminating saving and restoring. There are eight 16-bit registers in each register set and there are 16 sets . . . One set is allocated to normal background processing and 15 sets are dedicated to 15 levels of interrupt processing.

MEMORY SELECTION

Core . . . . . 4K and 16K bytes

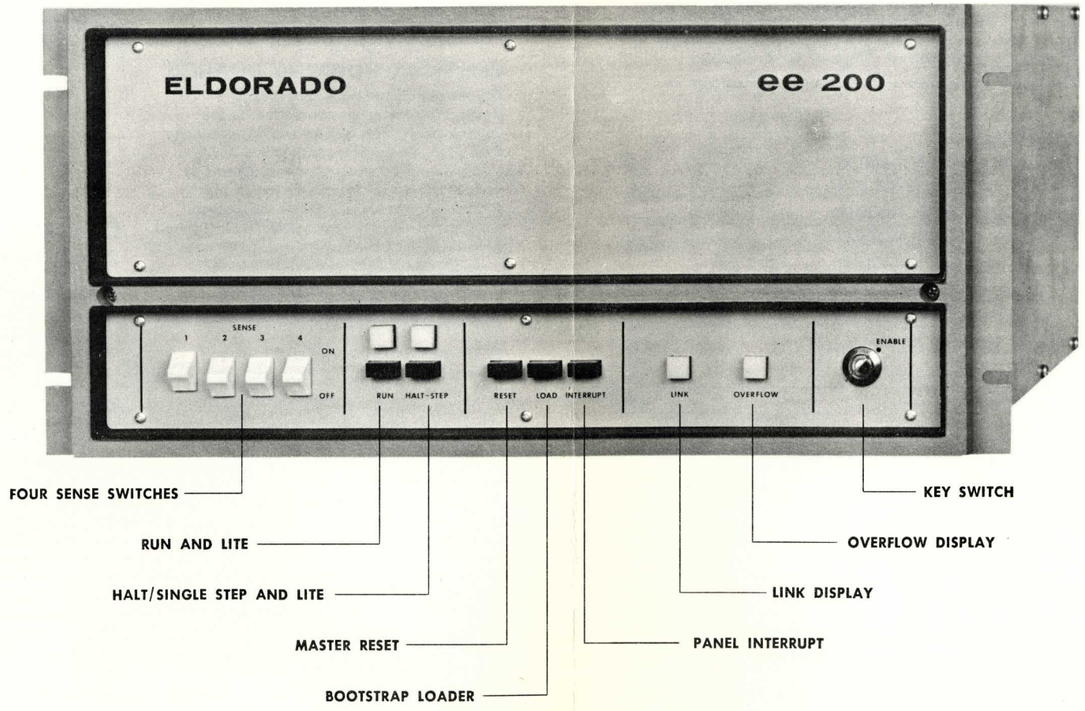
High Speed IC . . . . . 16, 32, 64, 128 bytes

Read-Only . . . . . 64 bytes

Up to 65K bytes of memory are available with the ee 200, with all 65K directly addressable.

WORD LENGTH AND INSTRUCTIONS

The ee 200 operates with parallel arithmetic capability, 2's complement, on either 8-bit bytes or 16-bit words. The instruction list includes 8, 16 and some 24-bit commands. There are 69 basic commands and hundreds of permutations.



ADDRESS MODIFICATION

Address modification of the ee 200 is unusually versatile and powerful. Modes include:

1. Direct addressing of any I/O device or up to 65K memory.
2. Fully extended indirect addressing.
3. Relative addressing.
4. Relative indirect addressing.
5. One and two-byte literals.

INDEXING

Any of the eight general purpose registers can be used as index registers. Indexing modes are:

1. Straight Indexing—with and without displacement
2. Automatic Incrementing—with and without displacement
3. Automatic Decrementing—with and without displacement

(All modes can also be used for Indirect Indexing.)

Software

The ee 200 basic software philosophy is to minimize time and cost needed for customers to write their own programs. All utility programs and general application subroutines are written for minimum memory configurations. Subroutines are re-entrant and relocatable.

UTILITY AND APPLICATION SOFTWARE

Additional software includes:

LOADERS—Binary Loader—Bootstrap Loader—Linkage Editor

ASSEMBLERS—Resident Absolute Assembler—Relocatable Assembler—Cross Assembler For Batch Processing

COMPLIERS—ESP String Processor Complier—Dartmuth Basic

UTILITIES—Debug Package Including Traps—Math Package—Peripheral Software Drivers, Text Editor

All software is dedicated to being operationally efficient and to using the smallest possible memory.

INPUT/OUTPUT CAPABILITY

The Universal Bus provides the same wide dimensions of input/output capability that it brings to memory make-up. For example, all external devices can directly access memory without going through the central processor. Peripheral devices can communicate directly with each other. Transfer rates between memory and external devices or between external devices can be more than 1 million bytes/second.

Serial interface for an ASR 33/35 teletypewriter is included in the basic ee 200. The basic teletypewriter bootstrap routine is built into the ee 200 hardware. All other peripherals are put on-line with the simple plug-in of a controller into one of the available card positions.

RELIABILITY

Because the ee 200 is designed for demanding on-line, real time systems work, the goal of reliable, dependable operation received design attention far beyond what is normally expected in a computer of this class. For example, circuit boards are mounted vertically for maximum cooling without the need for a cooling fan. Large connector fingers are used for maximum reliability.

A 0.8 inch space between circuit boards provides ample convection cooling for components, sharply decreasing heat build up and adding substantially to component life. The ee 200 circuit boards, including central processor, memory modules and I/O controllers, use connectors with low density MIL-spec spacing of .156 inch between centers, making all plug-in connections simpler, less costly and more reliable.

As another step toward reliability, the core memory, basically an 850-nanosecond design, operates on a 1.2 microsecond cycle to further decrease heat build-up. The only wiring within the ee 200 enclosure, besides the power supply cable, runs a short distance between front panel and motherboard. Processor is made of TTL logic elements with extensive use of MSI devices.

ee 200 Instructions

MNEMONIC NAME

Control (1 Byte)

WAIT . . . . . Wait for Interrupt (Halt)
NOP . . . . . No Operation
SF . . . . . Set Fault
RF . . . . . Reset Fault
EI . . . . . Enable Interrupt System
DI . . . . . Disable Interrupt System
SL . . . . . Set Link
RL . . . . . Reset Link
CL . . . . . Complement Link
RSR . . . . . Return from Subroutine
RI . . . . . Return from Interrupt
RIM . . . . . Return from Interrupt Modified
ELO . . . . . Enable Link Out
PCX . . . . . Transfer PC to X
DLY . . . . . Delay 4.55 milliseconds

Conditional Branches (2 Bytes)

BL . . . . . Branch if Link Set
BNL . . . . . Branch if Link Not Set
BF . . . . . Branch if Fault Set
BNF . . . . . Branch if Fault Not Set
BZ . . . . . Branch if Equal to Zero
BNZ . . . . . Branch if Not Equal to Zero
BM . . . . . Branch if Minus Set
BP . . . . . Branch on Plus
BGZ . . . . . Branch if Greater than Zero
BLE . . . . . Branch if Less Than or Equal to Zero
BS1 . . . . . Branch if Sense Switch 1 Set
BS2 . . . . . Branch if Sense Switch 2 Set
BS3 . . . . . Branch if Sense Switch 3 Set
BS4 . . . . . Branch if Sense Switch 4 Set
BTM . . . . . Branch on Teletype MARK
BRU . . . . . Unconditional Branch

Single Register Operations (1 or 2 Bytes)

INR(B) . . . . . Increment Register
DCR(B) . . . . . Decrement Register
CLR(B) . . . . . Clear Register
IVR(B) . . . . . Invert Register (1's complement)

MNEMONIC NAME

Single Register Operations (continued)

SRR(B) . . . . . Shift Right
SLR(B) . . . . . Shift Left
RRR(B) . . . . . Rotate Right
RLR(B) . . . . . Rotate Left
INA(B) . . . . . Increment A by 1
DCA(B) . . . . . Decrement A by 1
CLA(B) . . . . . Clear A
IVA(B) . . . . . Invert A
SRA(B) . . . . . Shift Right A
SLA(B) . . . . . Shift Left A
INX . . . . . Increment X (Word) by 1
DCX . . . . . Decrement X (Word) by 1

Double Register Operations

ADD(B) . . . . . Add
SUB(B) . . . . . Subtract
AND(B) . . . . . AND
OR(B) . . . . . OR Inclusive
ORE(B) . . . . . OR Exclusive
XFR(B) . . . . . Transfer
AAB(B) . . . . . Add A Register and B Register
SAB(B) . . . . . Subtract A Register and B Register
NAB(B) . . . . . AND A Register and B Register
XAX(B) . . . . . Transfer A Register to X Register
XAY(B) . . . . . Transfer A Register to Y Register
XAB(B) . . . . . Transfer A Register to B Register
XAZ(B) . . . . . Transfer A Register to Z Register
XAS(B) . . . . . Transfer A Register to S Register

Memory Reference

LDA(B) . . . . . Load A Register
STA(B) . . . . . Store A Register
LDB(B) . . . . . Load B Register
STB(B) . . . . . Store B Register
LDX . . . . . Load X Register
STX . . . . . Store X Register
JMP . . . . . Jump
JSR . . . . . Jump to Subroutine

PHYSICAL SPECIFICATIONS

MECHANICAL: SIZE: Nominal 8¾" x 17" x 19¼" (HxWxD). With Rack Ears Attached, Conforms to Standard 8¾" Rack Mounting Height

WEIGHT: (Basic CPU, Enclosure, Control Panel) 17 Lbs., Shipping 27 Lbs.

ENVIRONMENTAL: OPERATING TEMPERATURE: 0°C to +50°C

STORAGE TEMPERATURE: −55°C to +80°C

HUMIDITY: 0 to 95% RH Non-Condensing

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MODEL ee200

Easily Expandable

OEM PRICES AND PERIPHERAL INTERFACES

ee 200 Model No.	DESCRIPTION	Pre-requisite	PRICE 1-5	6-10	11-20	21-50	51-100		CURRENT REQD. (Amperes) +5V	−10V	+10V
A	CPU, ENCLOSURE, BASIC CONTROL PANEL	----	$1,765	$1,610	$1,460	$1,310	$1,160		4.85		
B	4096 BYTES (8 BITS) CORE MEMORY 1.0 μs FULL CYCLE TIME	A	$ 900	$ 865	$ 830	$ 795	$ 755	Standby Operate	0.68 1.45	0.07 1.70	
BB	8192 BYTES (8 BITS) CORE MEMORY 1.2μS FULL CYCLE TIME	A	$1,500	$1,405	$1,245	$1,115	$ 985	Standby Operate	2.50 2.50	0.15 5.00	0.1 0.5
C	16384 BYTES (8 BITS) CORE MEMORY 1.2 μs FULL CYCLE TIME	A	$2,000	$1,825	$1,660	$1,485	$1,315	Standby Operate	2.50 2.50	0.15 5.00	0.1 0.5
D	CARD READER INTERFACE FOR DOCUMATION MODEL 200	A, 1-B	$ 495	$ 450	$ 410	$ 370	$ 325		0.63		
E	ROM MEMORY 64 BYTES FOR READER	D	$ 295	$ 270	$ 245	$ 220	$ 195		0.50		
F	LINE PRINTER INTERFACE FOR DATAPRINTER V132	A, 1-B	$ 495	$ 450	$ 410	$ 370	$ 325		0.72		
G	SYNCHRONOUS MODEM INTERFACE	A, 1-B	$ 495	$ 450	$ 410	$ 370	$ 325		1.0		
H	ASYNCHRONOUS MODEM INTERFACE 110, 300, 1200 BAUD	A, 1-B	$ 495	$ 450	$ 410	$ 370	$ 325		1.12		
I	TYPEWRITER INTERFACE FOR IBM SELECTRIC 735	A, 1-B	$ 600	$ 550	$ 500	$ 445	$ 395		0.8		
J	CASSETTE INTERFACE FOR 1 TO 3 SYKES TT 100	A, 1-B	$ 650	$ 595	$ 540	$ 480	$ 425		2.55		
K	ROM MEMORY 64 BYTES FOR CASSETTE	J	$ 250	$ 225	$ 205	$ 185	$ 165		0.5		
L	DISC INTERFACE FOR IOMEC 2002 OR 2012	A, 1-C	$1,900	$1,250	$1,145	$1,020	$ 900		2.0		
M	MAGNETIC TAPE INTERFACE FOR PERTEC 6000 & 7000 SERIES	A, 2-B (or 1-C)	$1,900	$1,250	$1,145	$1,020	$ 900		1.7		
N	PARALLEL TELETYPE INTERFACE FOR ASR 33/35	A, 1-B	$ 495	$ 450	$ 410	$ 370	$ 325		0.8		
O	ROM MEMORY 64 BYTES TO CUSTOMER SPECIFICATION	----	$ 325	$ 295	$ 270	$ 240	$ 215		0.5		
P	POWER SUPPLY, REMOTE SENSE +5V @ 10A, −10V @ 5A, +10V @ 2A	A	$ 250	$ 250	$ 250	$ 250	$ 250				
Q	AUGMENTED POWER SUPPLY, REMOTE SENSE +5V @ 20A, −10V @ 5A, +10V @ 2A	A	$ 375	$ 375	$ 375	$ 375	$ 375				
R	EXTENDER BOARD, CPU	A	$ 75	$ 70	$ 65	$ 55	$ 50				
S	EXTENDER BOARD, I/O	A	$ 75	$ 70	$ 65	$ 55	$ 50				
T	UNIVERSAL INTERFACE BOARD. FRONT WITH BUS LOGIC AND REAR FOR CUSTOMER WIRE WRAP	A	$ 325	$ 295	$ 270	$ 240	$ 215				
U	PAPER TAPE READER 300 CPS (DIGITRONICS)	A	$ 495	$ 450	$ 410	$ 370	$ 325		0.7		
V	LINE PRINTER INTERFACE FOR PRINTEC 100	A, 1-B	$ 495	$ 450	$ 410	$ 370	$ 325		0.72		

Prices and Specifications are subject to change without notice. Prices are F.O.B. Concord, California. Terms are N30.

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