CS23/E1 COMMUNICATIONS SUBSYSTEM

(DHU11 COMPATIBLE)

TECHNICAL MANUAL

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CS2351001 Rev B
September, 1986

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This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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Printed in U.S.A.

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EMULEX PRODUCT WARRANTY

WARRANTY: Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex CS23/E1 Communications Subsystem supplied shall be free from defects in material and workmanship.

During the warranty period, if the customer experiences difficulties with an Emulex controller and is unable to resolve the problem via the phone with Emulex Technical Support, a Return Authorization will be issued. Following receipt of a Return Authorization, the customer is responsible for returning the product to Emulex, freight prepaid. Emulex, upon verification of warranty will, at its option, repair or replace the component in question, and return to the customer freight prepaid.

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1.1 INTRODUCTION

This manual is designed to help you install and use your CS23/E1 Communications Subsystem in the most efficient and straightforward manner possible. The contents of the seven sections and six appendices are described briefly below.

Section 1 **General Description** This section contains an overview of the CS23/E1 Communications Subsystem.

Section 2 **Subsystem Specification** This section contains general, electrical, environmental, and physical specifications for each component of the subsystem.

Section 3 **Planning the Installation** This section contains the information necessary to plan your installation.

Section 4 **Installation** This section contains the information needed to set up and physically install the subsystem.

Section 5 **Troubleshooting** This section describes fault isolation procedures that can be used to pinpoint trouble spots.

Section 6 **Controller Registers and Programming** This section contains a description of the subsystem's DHU11-type registers. This section also describes the controller architecture.

Section 7 **Interfaces** This section describes the subsystem UNIBUS interface.

Appendix A **DEC Autoconfigure Algorithm** This appendix contains an explanation of the autoconfigure algorithm for UNIBUS address assignment.

Appendix B **PROM Removal and Replacement** This appendix contains instructions for PROM removal and replacement.

Appendix C **PDP-11 Diagnostics** This appendix contains instruction for loading and starting the DEC PDP-11 diagnostics run by the CS23/E1.

Appendix D **VAX-11 Diagnostics** This appendix contains instruction for loading and starting the DEC VAX-11 diagnostics run by the CS23/E1.

Appendix E **Code Conversion Tables** This appendix provides ASCII and decimal/hexadecimal/octal code conversion tables.

Glossary This glossary contains definitions of words or phrases that do not have generally accepted meanings or that have a different connotation in this manual.

1.1.1 RELATED DOCUMENTATION

This manual is the main piece of documentation for the CS23/E1 Communication Subsystem. Two other manuals come with the subsystem: a distribution panel technical manual and a diagnostic manual (if the Emulex VAX diagnostic IVC23E was ordered). The Emulex part number for the VAX Installation Diagnostics User's Guide is VX9950902.

These other manuals are used only during specific parts of the installation procedure and this manual will clearly reference the other manuals any time you need them.

1.2 SUBSYSTEM OVERVIEW

The CC23/E1 Communications Subsystem connects, via a single UNIBUS small peripheral controller (SPC) slot, up to 32 asynchronous data channels to PDP-11 or VAX-11 minicomputers manufactured by Digital Equipment Corporation (DEC).

To provide software transparency, the CS23/E1 emulates one or two DEC DHU11 communications multiplexers.

The CS23/E1 subsystem components consist of the CC23 Controller, one or two distribution panels, and cables to connect the controller to the distribution panels.

The CS23/E1 incorporates several advanced features for communications multiplexers. These features include direct memory access (DMA) on transmit, 256-character receive silos with fill alarm for each sixteen-channel emulation, programmable channel parameters, and data rates up to 38400 bits per second (bps).

The CS23/E1 Communications Subsystem is shown in Figure 1-1.

CS2301-0995

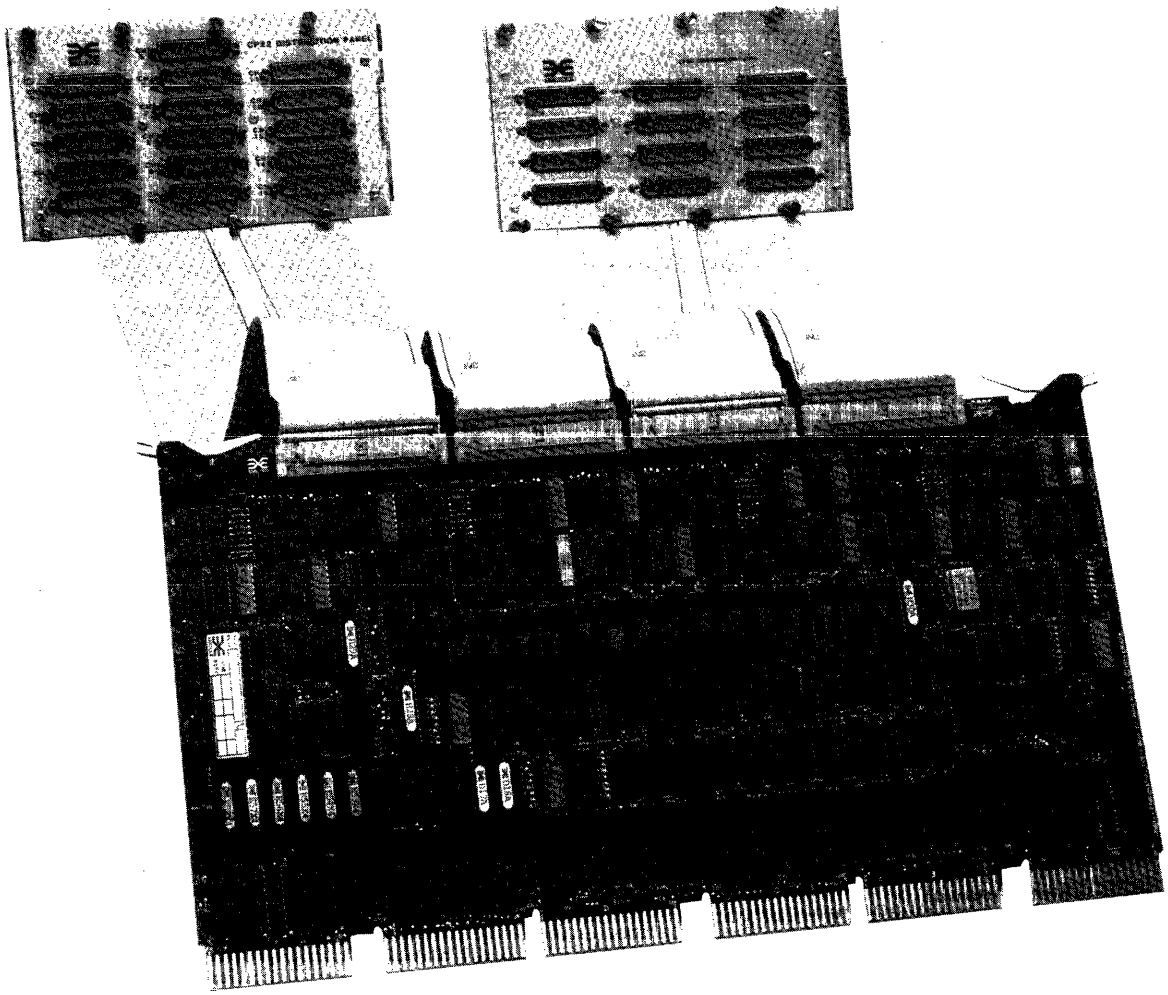


Figure 1-1. CS23/E1 Communications Subsystem

1.3 PHYSICAL ORGANIZATION OVERVIEW

The CS23/E1 Communications Subsystem consists of two components: the CC23 Controller and a distribution panel. Figure 1-2 shows the relationship of each component to the other. These relationships are explained in the following subsections.

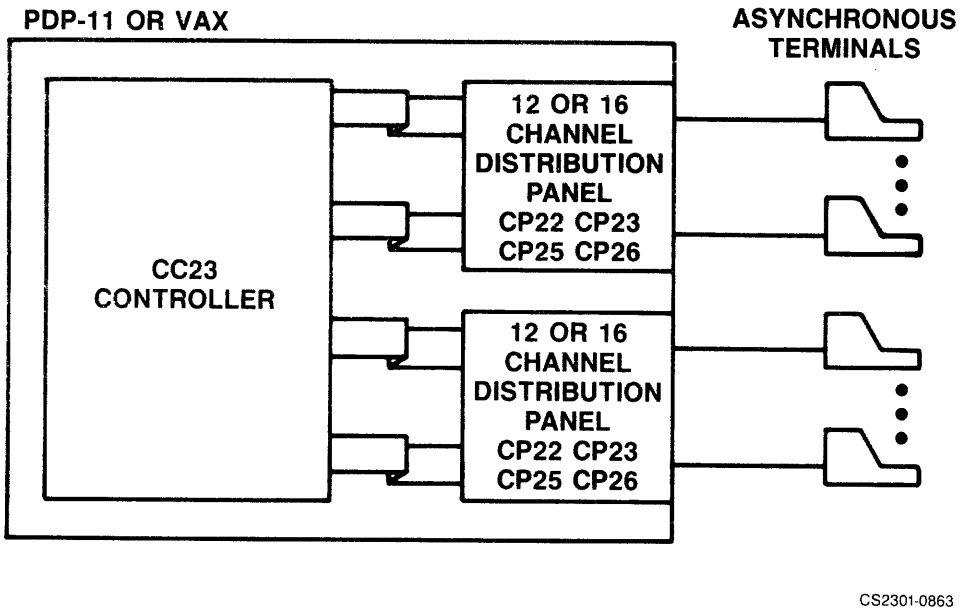


Figure 1-2. CS23/E1 Subsystem Configuration

1.3.1 CC23 CONTROLLER

The CC23 Controller is a single hex-wide printed circuit board assembly (PCBA) that plugs directly into a UNIBUS SPC backplane slot. The CC23's firmware-driven microprocessor performs the DHU11 emulation and multiplexes/de-multiplexes data from the asynchronous channels.

The CC23 Controller is connected to the distribution panel(s) using two 50-pin flat cables for each panel.

1.3.2 DISTRIBUTION PANEL

The CS23/E1 comes with one or two of the following distribution panels:

- CP22 (RS-232-C, 16 channels, partial modem control)
- CP23 (20 mA/RS-232-C, 16 channels, partial modem control)
- CP25 (RS-232-C/RS-422-A, 16 channels, partial modem control)
- CP26 (RS-232-C, 12 channels, full modem control on 8 channels, partial modem control on 4 channels))

All of the distribution panels are FCC compliant. All panels are the same size as DEC's DMF32 distribution panel. They can be mounted directly in place of a DMF32 panel in CPU cabinets that are DMF32 compatible, or in a DEC-FCC cabinet, or in a rack that mounts on RETMA rails.

The CP22 and CP23 can be ordered with EMI filters installed on each 25-pin connector. This is a special order item, however, and is not generally required.

1.4 ORDERING INFORMATION

The CS23/E1 Communications Subsystem is ordered using model numbers. The models available are:

- CS23/CP22
- CS23/CP23
- CS23/CP25
- CS23/CP26
- CS23/CP22/CP22
- CS23/CP22/CP23
- CS23/CP22/CP25
- CS23/CP22/CP26
- CS23/CP23/CP23
- CS23/CP23/CP25
- CS23/CP23/CP26
- CS23/CP25/CP25
- CS23/CP25/CP26
- CS23/CP26/CP26

The basic contents of the models is contained in Table 1-1. Table 1-2 contains a list of all CS23/E1 items that can be ordered separately.

Table 1-1. CS23/E1 Basic Model

Emulex Part	Coments
CC23 Controller	
CPXX Distribution Panel	One or two, depending on model ordered
8 foot 50-wire ribbon cable	Two per distribution panel
CS23 Technical Manual	
CPXX Technical Manual	One for each distribution panel ordered

Table 1-2. CS23/E1 Accessories

Model Number	Part Number	Description
CC23/E1	CS2310202-E1X	CC23 Controller
CP22-02	CP2210202-02	RS-232-C distribution panel
CP23-02	CP2310201-02	20 mA current loop/RS-232-C distribution panel
CP25	CP2510202	RS-422-A/RS-232-C distribution panel
CP26	CP2610201-00	RS-232-C distribution panel
NA	CU2111201-02	8 foot 50-wire ribbon cable, CC23 Controller to distribution panel
NA[1]	NA	Optional Address Range Decode PROM
NA	CU0411202	Staggered Loopback Connector
NA	CU0411203	Wrap-Around Connector
NA	CS2351001	CS23/E1 Technical Manual
NA	CP2251001	CP22 Technical Manual
NA	CP2351001	CP23 Technical Manual
NA	CP2551001	CP25 Technical Manual
NA	CP2651001	CP26 Technical Manual

[1]Special order item.

Note: Distribution panel installation hardware and most cables are not listed. The need for these will vary by application. See your distribution panel manual to determine your requirements.

1.5 FEATURES

1.5.1 MICROPROCESSOR DESIGN

The CC23 design incorporates an eight-bit, high-performance bipolar microprocessor to perform all controller functions. The microprocessor approach provides a reduced component count, high reliability, easy maintainability, and the ability to perform an emulation of the equivalent DEC controller.

1.5.2 FCC COMPLIANCE

The CC23/E1 Communications Subsystem complies with the appropriate Federal Communications Commission (FCC) standards that limit EMI radiation from computing devices. All models, if operated within Class A compliant cabinets, comply with the limits for FCC Class A.

1.5.3 SELF-TEST

The controller incorporates an internal self-test routine that is executed upon power-up. This test exercises all parts of the microprocessor and the on-board memory. Although this test does not completely test all circuitry, successful execution indicates a very high probability that the controller and the UNIBUS interface are operational. Failure of the self-test is indicated by Fault LEDs on the edge of the controller board. In addition, if the failure is in the controller electronics, the controller cannot be addressed from the central processing unit (CPU).

1.5.4 PROGRAMMABLE CHANNEL PARAMETERS

Parameters on all 32 channels provided by the CS23/E1 Communications Subsystem can be set individually under program control.

Parameters for all channels include:

- Data rates from 50 to 38,400 bps
- The number of stop bits per character
- Parity (odd, even, or none)
- The number of data bits per character
- Independently programmable transmit and receive data rates per channel

1.5.5 DMA ON TRANSMIT

The subsystem performs full-word direct memory access (DMA) on transmit. This feature considerably reduces the CPU overhead associated with data communications, especially when the host system is running terminal-I/O intensive software.

1.6 COMPATIBILITY

1.6.1 WITH DEC DIAGNOSTICS

The CS23/E1 Communications Subsystem executes the following DEC DHU11 PDP-11 diagnostics:

- ZDHU
- ZDHV
- ZDHW
- ZDHX
- XDHU

The CS23/E1 executes the following DEC DHU11 VAX-11 diagnostics:

- EVDAI
- EVDAH
- UETP

The diagnostics EVDAH and UETP are run error-free by the CS23/E1. Diagnostic EVDAI runs with some errors. See subsection D.3 for a list of the tests that run with errors. Instructions for loading and starting the diagnostics are contained in Appendix C, PDP-11 Diagnostics, and Appendix D, VAX-11 Diagnostics.

1.6.2 EIA SIGNALS

The EIA signals supported vary for each distribution panel type. For a list of the signals supported, consult your distribution panel manual.

1.6.3 OPERATING SYSTEMS

The CS23/E1 Communications Subsystem is compatible with the following operating systems without modification:

- RSX-11M, V4.1 update level D or above (PDP-11)
- RSX-11M-PLUS, V2.1 update level D or above (PDP-11)
- RSTS/E, V8.0-07 or above (PDP-11)
- VMS, V4.0 or above (VAX-11)
- Ultrix-11, V2.0 or above
- Ultrix-32, V1.1 or above

1.6.4 EXTERNAL DEVICE INTERFACES

Distribution panels available for use with the CS23/E1 Communications Subsystem are compatible with the following interfaces:

- RS-232-C
- RS-422-A
- 20 mA current loop

Details of distribution panel compatibility and functionality are contained in the distribution panel technical manual that came with your communications subsystem.

2.1 OVERVIEW

This section contains the general, electrical, environmental, and physical specifications for the CS23/E1 Communications Subsystem.

Specifications are contained in tables as listed below:

Subsection	Title
2.1	Overview
2.2	General Specification
2.3	Electrical Specification
2.4	Environmental Specification
2.5	Physical Specification

2.2 GENERAL SPECIFICATION

A general specification for the CS23/E1 Communications Subsystem is contained in Table 2-1.

Table 2-1. General Specifications

Parameter	Description
FUNCTION	Communications multiplexer providing up to 32 asynchronous channels
EMULATION	Complete functional emulation of one or two DEC DHU11 multiplexers
Number of emulations	1 or 2
Number of channels	Up to 32
Diagnostic Compatibility	
PDP-11	ZDHU, ZDHV, ZDHW, ZDHX, XDHU
VAX-11	EVDAI[1], EVDAH, UETP

[1]Runs with some errors. See subsection D.3.

continued on next page

Table 2-1. General Specifications (continued)

Parameter	Description
Operating System Compatibility	
PDP-11	RSX-11M, V4.1 update level D or above RSX-11M-PLUS, V2.1 update level D or above RSTS/E, V8.0-07 or above Ultrix-11, V2.0 or above
VAX-11	VMS, V4.0 or above Ultrix-32, V1.1 or above
CPU I/O TECHNIQUE	
Transmission	Interrupt driven DMA, or programmed I/O with transmit silo
Reception	Interrupt driven, programmed I/O with receive silo
Transmission Modes	Full-duplex, half-duplex
Programmable Data Format	
Character Lengths	5 to 8 bit data
Stop Bits	1, 1.5, or 2
Parity	Odd, even, or none
Data Rates	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 4800, 7200, 9600, 19200, 38400; split speed capability[1]
Throughput Rate	50,000 characters/second total
EMULEX DISTRIBUTION PANELS SUPPORTED	CP22 (16 channels) CP23 (16 channels) CP25 (16 channels) CP26 (12 channels)

[1]See Table 6-1

continued on next page

Table 2-1. General Specifications (continued)

Parameter	Description
INTERFACES	
CPU	Standard UNIBUS SPC interface
Device Address	All possible DHU11 assignments (switch selectable) (change of PROMs needed for some addresses)
Vector Address	All possible DHU11 assignments (switch selectable)
Priority Level	Switch Selectable, BR5 or BR6
EIA	
Asynchronous ports	Serial, low order bit first, asynchronous
Connectors	25-Pin Male
Configuration	Data Terminal Equipment (DTE)
Modem Status Signals	
16 Channel Panel All channels	DCD, RI
12 Channel Panel Channels 0-3 Channels 4-7* Channels 8-11*	 DCD, RI, CTS, DSR DCD, RI, CTS DCD, RI
Modem Control Signals	
16 Channel Panel All channels	DTR
12 Channel Panel Channels 0-3 Channels 4-7 Channels 8-11	 DTR, RTS DTR, RTS DTR
Modems Supported	Bell-Compatible: 103, 113, 212 CCITT: V.22

*See subsection 6.2.7.

2.3 ELECTRICAL SPECIFICATION

Table 2-2 lists and describes the electrical specification for the CC23 Controller.

Table 2-2. CC23 Electrical Specifications

Parameter	Description
UNIBUS LOAD	One
ELECTRICAL REQUIREMENTS	+5 volts DC ± 5% at 8 amperes +15 volts DC ± 4% at 1 ampere (with all channels connected) -15 volts DC ± 4% at 1 ampere (with all channels connected)

2.4 ENVIRONMENTAL SPECIFICATION

Table 2-3 contains the environmental specifications for the CC23 Controller.

Table 2-3. CC23 Environmental Specifications

Parameter	Description
STORAGE TEMPERATURE	-40°C (°F) to 66°C (°F)
OPERATING TEMPERATURE	0°C (50°F) to 45°C (104°F) Where maximum temperature is reduced 1.8°C per 1000 meters (1°F per 1000 feet) altitude
RELATIVE HUMIDITY	10% to 90% with a maximum wet bulb of 28°C (82°F) and a minimum dewpoint of 2°C (3.6°F)
COOLING	11 cubic feet per minute required

2.5 PHYSICAL SPECIFICATION

Table 2-4 contains the physical specifications for the CC23 Controller. The dimensions of the CC23 are shown in Figure 2-1.

Table 2-4. CC23 Physical Specifications

Parameter	Description
PACKAGING	Single, hex-size, six-layer PCBA
Dimensions	8.4 inches high by 15.7 inches wide by .625 inches deep
Shipping Weight	5 pounds

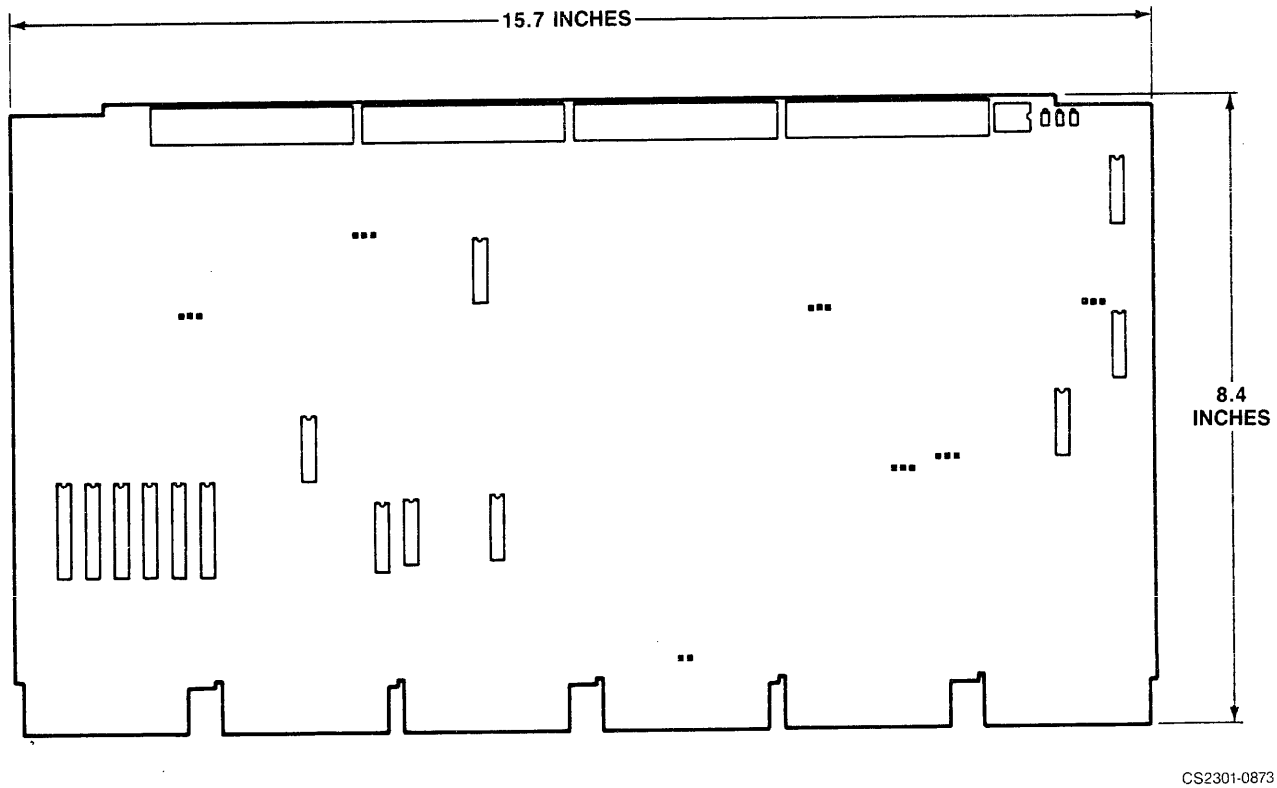


Figure 2-1. CC23 Controller Dimensions

3.1 OVERVIEW

This section is designed to help you plan the installation of your CS23/E1 Communications Subsystem. Taking time to plan the configuration of your subsystem before beginning its installation will result in a smoother installation with less system down time. As a planning tool, this section explains some of the practical matters that need to be considered before you begin your installation.

This section contains examples and explanations of configuration options. The subsections are listed in the following table:

Subsection	Title
3.1	Overview
3.2	Configurations
3.3	Modem Signals
3.4	Data Flow Control
3.5	Hardware Level Flow Control
3.6	Channel Numbering
3.7	Installing the CS23/E1 on the PDP-11
3.8	Installing the CS23/E1 on the VAX/VMS

3.2 CONFIGURATIONS

The CS23/E1 is designed to provide up to 32 channels on a PDP-11 or on a VAX-11. These channels are carried to external devices via distribution panels. The CS23/E1 can use any mix of two distribution panels from the following group:

- CP22
- CP23
- CP25
- CP26

This subsection discusses each panel in detail to help you determine which panels best suit your application.

3.2.1 CP22 DISTRIBUTION PANEL

The CP22 is a 16-channel passive distribution panel. It can be mounted directly in DMF32-compatible CPU cabinets, a DEC FCC cabinet, or rack-mounted in a chassis on RETMA rails. The panel provides an RS-232-C compatible interface on all ports.

3.2.2 CP23 DISTRIBUTION PANEL

The CP23 is a 16-channel active distribution panel. It can be mounted directly in DMF32-compatible CPU cabinets, a DEC FCC cabinet, or rack-mounted in a chassis on RETMA rails. Each port can be configured as either an RS-232-C or a 20 mA current loop interface.

3.2.3 CP25 DISTRIBUTION PANEL

The CP25 is a 16-channel active distribution panel. It can be mounted directly in DMF32-compatible CPU cabinets, a DEC FCC cabinet, or rack-mounted in a chassis on RETMA rails. Each port can be configured as either an RS-232-C or an RS-422-A interface.

3.2.4 CP26 DISTRIBUTION PANEL

The CP26 is a 12-channel passive distribution panel. It can be mounted directly in DMF32-compatible CPU cabinets, a DEC FCC cabinet, or rack-mounted in a chassis on RETMA rails. The panel provides an RS-232-C compatible interface on all ports.

The CP26 provides additional modem control signals for eight of the 12 ports.

3.3 MODEM SIGNALS

The supported modem signals vary for each distribution panel. Because of this, careful consideration should be given to which devices will be connected to which ports.

3.4 DATA FLOW CONTROL

There are two common methods used to control the flow of data between the host CPU and external devices (such as terminals and printers):

- **XON/XOFF Flow Control.** With this method, XON/XOFF characters are used to start and stop the data flow. If the external device is receiving data too fast for it to keep up, it sends an XOFF character to the host and the host stops transmission. When it is able to accept more data, it transmits an XON character to the host.

- **Hardware Level Flow Control.** A device that uses this method drops a modem control signal (usually Data Terminal Ready) to signal the host that it cannot accept more data. The DTR pin on the device is cabled to one of the modem status pins on the distribution panel (usually Clear To Send or Carrier Detect), which is monitored by the host. When the device is able to accept more data, it raises its DTR signal.

There are advantages to both methods. XON/XOFF flow control allows devices to be attached to the distribution panel with only four wires and is the method used by DEC. For this reason, Emulex recommends using devices that are capable of XON/XOFF flow control.

However, many devices (especially printers) are receive-only devices and are incapable of transmitting XON/XOFF characters. For this reason, the CS23/E1 supports three switch-selectable versions of level flow control on a per-channel basis. The discussion in subsection 3.5 describes each version of hardware level flow control. The switch settings necessary to choose hardware level flow control are described in Section 4.

To preserve emulation transparency, in all three modes, all modem status signal changes are reported to the host operating system via the appropriate status register and receive FIFO.

In the Basic Level Flow Control and in the XON/XOFF Flow Control, the DTR bit in the Line Control Register always reflects what was last written to it, regardless of what the EIA DTR signal is. Also, channels enabled for both of these types of flow control have DTR deasserted at reset, then reasserted automatically.

The term congested is used in the following subsections to describe the state of certain silos. Congested means that the silo has been at least three-quarters full and has not yet dropped below one-half full.

3.5 HARDWARE LEVEL FLOW CONTROL

When the hardware level flow control option is enabled, the CC23 controls transmitted data flow by monitoring the Carrier Detect (DCD) or Clear to Send (CTS) input at the distribution panel. The signal monitored (DCD or CTS) depends on which signal is selected using switches SW6-1 through SW6-5.

When DCD (or CTS if selected) is negated, the CC23 generates an XOFF character for transmission to the host. When DCD (or CTS if selected) is asserted, the CC23 generates an XON character for transmission to the host. An XOFF from the host negates Data Terminal Ready (DTR). An XON from the host asserts DTR.

This feature can be enabled only for the first of the two distribution panels connected to the CC23 (the panel connected to J1 and J2 on the CC23). If the panel is a 16 channel panel, channels one through fifteen in single channel increments can be enabled to use this feature. If the panel is a 12 channel panel, channels zero through eleven in single channel increments can be enabled to use this feature.

When enabled, the panel uses DCD (or CTS) for control of outbound data, and DTR for control of incoming data. DCD is converted to XON/XOFF characters for transmission to the host. XON/XOFF characters coming from the host are converted to DTR.

When switch SW6-5 is ON (closed), CTS is used instead of DCD on channels zero through eight of a twelve-channel panel in single channel increments.

3.5.1 BASIC LEVEL FLOW CONTROL

This is the simplest method. Transmission of outbound data stops within two character times if DCD (or CTS) drops, and restarts when DCD or CTS is raised.

3.5.1.1 Programming Notes for Basic Level Flow Control

After the CC23 receive silo is congested, inbound data reception of a character on any line results in the deassertion of DTR. DTR is reasserted when the receive silo drops to less than one-half full.

This version of flow control has limited application. VMS, for example, times output operations and will post a transmit timeout if the controller halts transmission for too long.

3.5.2 LEVEL FLOW CONTROL WITH XON/XOFF CONVERSION

In this mode, the controller converts changes in modem signals into XON/XOFF characters for the benefit of the operating system.

Outbound transmission of data stops within two character times if DCD (CTS) changes to a deasserted condition. An XOFF character is passed to the host.

3.5.2.1 Programming Notes for Level Flow Control With XON/XOFF Conversion

If the OAUTO bit in the Line Control Register is set the TX.ENA bit in Transmit Buffer Address Register Number 2 is cleared when the silo becomes congested or DCD (CTS) is deasserted. See Section 6, Device Registers and Programming for bit descriptions.

Data transmission resumes when DCD (CTS) returns to an asserted condition. An XON character is passed to the host. If the OAUTO bit in the Line Control Register is set the TX.ENA bit in Transmit Buffer Address Register Number 2 is set.

If DCD is deasserted and the host operating system sets TX.ENA while in OAUTO mode, an XOFF is passed to the host and TX.ENA is cleared again within 30 ms.

After the receive silo has become congested, or after an XOFF is sent by the host operating system, or if the FORCE.XOFF in the Line Control Register is set, **inbound** data reception of characters on any channel results in the deassertion of DTR. An XOFF is not passed to the peripheral device.

DTR is reasserted when the receive silo becomes decongested and the FORCE.XOFF bit is cleared, or when the receive silo becomes decongested and the host operating system has sent an XON character. An XON character is not passed to the peripheral device.

This is the most useful mode of level flow control, because it allows standard DEC software to run transparently.

3.5.3 SOFTWARE ASSISTED LEVEL FLOW CONTROL

This version of level flow control is used to improve response time with host operating software that already has the capability of using level flow control. Response time is improved for both transmitted data and received data.

This type of level flow control differs from Basic Level Flow Control in the ability of the host's control. With Software Assisted Level Flow Control the host has the ability to control DTR so that it can inhibit transmission from the external device. With Basic Level Flow Control the host cannot control DTR; the CC23 retains control of that function.

Transmission of outbound data stops within two character times if DCD (or CTS) drops, and restarts when DCD (CTS) is raised.

3.5.3.1 Programming Notes for Software Assisted Level Flow Control

Reception of inbound data is controlled if the receive silo is congested, or if the host operating system writes a zero to the DTR bit in the Line Control Register. Upon the happening of either event (congestion of the silo or writing to the DTR bit), the EIA DTR signal is deasserted. The EIA DTR signal is reasserted when the receive silo is decongested **and** when the host operating system writes a one to the DTR bit in the Line Control Register.

Channels enabled for Software Assisted Level Flow Control have DTR deasserted at reset. These channels will wait for the host to set the DTR bit in the Line Control Register before asserting DTR.

With this method, the host is still in control, but data flow is started and stopped more quickly because the controller "anticipates" the need for flow control.

3.6 CHANNEL NUMBERING

The CS23/E1 emulates one or two 16-channel controllers. Thus, the CS23/E1 can accommodate up to 32 channels.

There are four distribution panels that can be used with the CS23/E1. The CP22, CP23, and CP25 are 16-channel panels with ports 0-15. The CP26 is a 12-channel panel with ports 0-11. The DHU11 channels correspond to the distribution panel ports in the way you would expect; that is, the DHU11 with the lowest starting address controls ports 0 through 15, the next DHU11 controls ports 16 through 31.

The distribution panel connected to CC23 connectors J1 and J2 is the first distribution panel, and the distribution panel connected to CC23 connectors J3 and J4 is the second distribution panel. Connectors J1 and J3 on the CC23 correspond to the first DHU11 emulation, and connectors J2 and J4 correspond to the second DHU11 emulation.

3.7 INSTALLING THE CS23/E1 ON THE PDP-11

This subsection includes information you will need during the SYSGEN process when you add the CS23/E1 to your system. Information is included for RSTS/E, RSX-11M, RSX-11M-PLUS, and Ultrix-11.

3.7.1 ADDING A NEW DEVICE TO RSTS/E

All device drivers are an integral part of the RSTS/E monitor. Therefore, when you add a new device to your system, you must generate an entirely new RSTS/E monitor. You do not need to generate a new monitor if:

- You are merely replacing an existing device with an Emulex emulation of the same device. That is, if you already have two DEC DHU11s and you are replacing them with a single CS23/E1, there is no need to regenerate the RSTS/E monitor.
- Your present RSTS/E monitor already includes support for two DHU11s but they have been disabled. To enable them, simply type HARDWR at the INIT.SYS option prompt and answer ENABLE at the HARDWR suboption prompt. When it asks Controller to Enable, answer DHU0 (the DEC mnemonic for DHU11). Repeat this for DHU1. To end, type Exit.

Other options (modem controls, etc.) are explained in subsection C.2.3.

3.7.1.1 Generating a New Monitor With SYSGEN

If your RSTS/E monitor does not include support for DHU11s, you must generate a new RSTS/E monitor which includes DHU11 support. To do this, you must generate a new monitor as described in the DEC RSTS/E System Generation Manual. If the only change you are making to your system is to add the CS23/E1, then most of your answers to the SYSGEN questions will not change. The only changes will be made during the Terminal Interface Configuration stage. The questions relating to the CS23/E1 are the following:

- DHU11's?
  Answer: This depends on the number of emulations you have programmed with switch SW4-8.

- DHU11 unit 00 lines enabled?
  Answer: 16. This question will be repeated once more for the second emulation. Answer 16 again.

- Dataset support for DHU11's?
  Answer: yes

When you have finished the questions, you must generate your new monitor from the configuration files created with the system program. Complete the monitor building as described in the DEC RSTS/E manual.

3.7.1.2 Modem Controls

After the RSTS/E monitor is complete, you must configure each CS23/E1 line as either local or remote. To enable modem controls for one or more lines:

- At the INIT.SYS Option prompt, type SET.

- At the SET suboption prompt, type LIST.

- At the Device prompt, type KB. The computer's response will be a list of all DHU11 lines and the keyboard numbers associated with each line. Note down the keyboard numbers of all lines which will require modem support. For an explanation of how DHU11 lines are numbered, see subsection 3.6.

- At the SET suboption prompt, type MODEM.

- At the KB prompt, type the keyboard numbers you noted down above. If you are constantly switching modems from line to line, you may enable modem controls for all lines by typing a range. If you do this, be sure to follow the external device cabling instructions in your distribution panel technical manual.

3.7.2 ADDING A NEW DEVICE TO RSX-11M

In general, when a new device is added to the RSX-11M operating system, a completely new operating system must be generated. You do not need to do this if you already have two DEC DHU11s installed and are merely replacing them with a CS23/E1.

If you are making no other changes to your system, then most of your answers to the SYSGEN questions will remain the same. The SYSGEN Phase I questions which relate to the CS23/E1 are the following:

- Autoconfigure the host system?
  Answer: Yes, if you wish to use autoconfigure.

- Devices
  Answer: SYSGEN will print a list of the devices it found during the autoconfigure process. If it is correct, simply type a period. The RSX-11M mnemonic for a DHU11 is YV, so autoconfigure should include YVA and YVB in its listing if you are emulating two DHU11's. Note down the bus and vector addresses; you will need them later.

- Loadable device drivers?
  Answer: Yes. The DHU11 requires a loadable driver.

- Terminal driver desired
  Answer: Full-duplex

- YV controller 0
  Answer: This question asks for the vector and bus addresses for the DHU11, the number of lines on the DHU11, and the default baud rate for remote lines. Autoconfigure should provide the correct responses already, which will look something like this:

  ```
  340,760260,16,300
  ```

  If the listed values are not correct, enter the correct values. Note that the default baud rate can be changed after SYSGEN is completed if you wish. If you do not want modem support, enter a default baud rate of zero. The CS23/E1 emulates up to two DHU11s, and this question will repeat for each emulation. YV0 corresponds to the first 16 channels of the CS23/E1, and YV1 to the second set of 16 channels.

After you have finished the Phase I questions, you must complete Phases II and III as described in the DEC RSX-11M manual.

3.7.2.1 Modem Controls

The MCR command SET can be used to change a terminal's status from remote to local and vice versa. It can also be used to change the baud rate of an individual channel. The command

```
SET /REMOTE
```

lists all remote channels. The command

```
SET /REMOTE=TT5:1200
```

sets the terminal line corresponding to TT5 as a remote dial-up line with a baud rate of 1200. Similarly, the command

```
SET /NOREMOTE
```

lists all local channels, and the command

```
SET /NOREMOTE=TT5:
```

sets the terminal line corresponding to TT5 as a local line. To find out which DHU11 line corresponds to TTn, you must check your hardware to see which terminals are connected to which ports on the distribution panel. See subsection 3.6 for an explanation of DHU11 channel numbering. Any user may use the SET command to change his own characteristics, but only a privileged user may change a channel characteristic of another.

Some users enable modem controls for all channels because they are constantly switching modems from channel to channel. If you do this, be sure to follow the external device cabling instructions in your distribution panel technical manual.

3.7.3 ADDING A NEW DEVICE TO RSX-11M-PLUS

To add a new device to the RSX-11M-Plus operating system, the appropriate device driver must be added to the RSX-11M-Plus kernel. Most devices can be added to RSX-11M-Plus without doing a new SYSGEN. However, this is not the case with communications equipment. When you add the CS23/E1, you will need to generate a completely new operating system.

If you are making no other changes to your system, most of your answers to the SYSGEN questions will remain the same. The SYSGEN questions which relate to the CS23/E1 are the following:

- Enter number of DHU11 multiplexers
  Answer: This depends on the number of emulations you have selected with switch SW4-8.

- Enter number of DHU11 dial-up lines
  Answer: List the number of lines which will require modem support. These lines will be the first lines on your system (i.e., the lowest numbered channels).

- At which baud rate do you want to answer?
  Answer: This question is asked only if you specified one or more dial-up lines. Answer with the baud rate of the modems you are using.

- Enter total number of DHU11 local lines
  Answer: All lines are either local or dial-up. So, if you specified any dial-up lines, specify the rest as local lines. For example, if you specified 12 dial-up lines, channels DHU0,0 through DHU0,11 would be, dial-up lines and channels DHU0,12, through DHU1,15 would be local lines. See subsection 3.6 for an explanation of DHU11 channel numbering.

- Enter vector address of YVA
  Answer: this is the interrupt vector address programmed into the CS23/E1 (see subsection 4.4.4). YV is the RSX-11M-Plus mnemonic for DHU11.

- What is its bus address?
  Answer: this is the bus address programmed into the CS23/E1 (see subsection 4.4.3).

  The bus and vector addresses must be entered for each DHU11 emulation. Enter the bus and vector for each emulation when the question appears.

- Enter terminal type for YVA
  Answer: respond with the terminal types you are using. This can be changed later without doing a new SYSGEN, so choose the default answer if you are not sure what terminal types you will be using.

3.7.4 ADDING A NEW DEVICE TO ULTRIX-11 (V2.0)

Support for new devices MUST be included in a monitor at SYSGEN time. A configuration file is generated (and a monitor is built) with the 'sysgen' program. The following is an example of the dialog form the 'sysgen' program that specifies a CS23/E1 controller:

```
Communications devices:

< dz dzv dzq dh dhu dhv dhdm du dn kl dl > ? dhu

Number of units <1> ? 1

CSR address for unit 1 <160020> ? 160440

Vector address for unit 1 <300> ? 300

Communications devices:

< dz dzv dzq dh dhu dhv dhdm du dn kl dl > ?
```

For more information on configuring a new monitor with the 'sysgen' program, see Appendix C of the Ultrix-11 System Installation Guide.

3.7.4.1 Autoconfigure

At boot time, Ultrix-11 attempts to auto-configure the devices included in the booted monitor's configuration file. If the device was not included in the configuration file, it will not be configured into the running system. If the device was included, but is not present, Ultrix-11 will skip it.

3.7.4.2 Enabling Terminals

To enable terminals, there must be a special file created for each line of the CS23/E1. Also the files 'ttys' and 'ttytype' must be edited to reflect the number, availability, and terminal types for each line.

3.7.4.2.1 /dev/ttyxx

The special files can be created with the supplied command file 'msf' in the /dev account. It will create the special files for the devices specified. For example:

```
# msf dhv11 0 tty00
```

will create the 16 special files for the CS23/E1 (beginning at tty00 through tty15).

3.7.4.2.2 /etc/ttys

The 'ttys' file is used by the 'init' program to determine which terminals to create the login process for (and allow logins). The format for each line is: nctty##

where n: 0 = Disabled
1 = Remote (enabled for dialup access)
2 = Local (enabled for local access)
3 = No Login

and c: 0 = cycles thru 300-1200-150-110 bits/sec
2 = 9600 bits/sec
3 = 1200 cycles back to 300 bits/sec
6 = 2400 bits/sec
7 = 4800 bits/sec
f = 1200 bits/sec

The remainder of the line is the terminal's entry in the device directory, /dev. An example of this file is as follows:

```
22console
22tty00
22tty01
22tty02
22tty03
22tty04
22tty05
22tty06
22tty07
22tty08
22tty09
22tty10
22tty11
22tty12
22tty13
22tty14
22tty15
```

3.7.4.2.3 /etc/ttytype

The 'ttytype' file is used by the 'login' program to initialize TERM variables at login time. An example of this file is:

```
vtl00 console
vtl00 tty00
vtl00 tty01
vtl00 tty02
vtl00 tty03
vtl00 tty04
vtl00 tty05
vtl00 tty06
vtl00 tty07
vtl00 tty08
vtl00 tty09
vtl00 tty10
vtl00 tty11
vtl00 tty12
vtl00 tty13
vtl00 tty14
vtl00 tty15
```

For more information on configuring terminals, see Chapter 4.7 "Enabling User Terminals" in the Ultrix-11 System Management Guide.

3.8 INSTALLING THE CS23/E1 ON THE VAX-11

The CS23/E1 Communication Subsystem is fully compatible with the DHU11 and consequently, it is supported on any VAX UNIBUS under VMS or Ultrix-32.

3.8.1 ADDING A NEW DEVICE TO VMS

You can use autoconfigure to automatically connect the CS23/E1 on power-up. Autoconfigure requires that specific device-types be installed at specific UNIBUS addresses so that it can identify the devices that it finds. VMS has a software utility called SYSGEN that can be used to determine the UNIBUS address and interrupt vector address for any I/O devices to be installed on the computer's UNIBUS. A running VAX/VMS computer system is required to use this utility. If you do not have access to a running system, you will have to determine the UNIBUS addresses and vector addresses manually (although autoconfigure can still be used to automatically connect the devices to the computer on power up). See Appendix A for a description of the algorithm used by SYSGEN to determine UNIBUS addresses.

The following procedure tells how to use SYSGEN to determine UNIBUS CSR addresses and interrupt vectors as well as how to use autoconfigure to connect the CS23/E1.

1. Login to the system manager's account. Set your default to SYS$SYSROOT:[SYSEXE].

2. Run the SYSGEN utility:

```
$ RUN SYSGEN<cr>
SYSGEN>
```

   The SYSGEN> prompt indicates that the utility is ready to accept commands.

3. Obtain a list of devices already installed on the VAX UNIBUS by typing:

```
SYSGEN> SHOW/CONFIGURATION<cr>
```

   SYSGEN will list the devices already installed in the UNIBUS by logical name. Make a note of the devices with floating addresses (greater than 760000_8) or floating vectors (greater than 300_8) that you plan to re-install with your CS23/E1.

4. To determine the UNIBUS addresses and vectors that autoconfigure will expect for that device type, execute the CONFIGURE command:

```
SYSGEN> CONFIGURE<cr>
DEVICE>
```

   Specify the UNIBUS devices to be installed by typing their UNIBUS names at the DEVICE prompt:

```
DEVICE> DHU11,2<cr>
```

   A comma separates the device name from the number of devices of that type to be installed. The number of devices is specified in decimal.

   For the installation of the CS23/E1, you need only specify devices that have floating addresses or vectors. Devices with fixed addresses or vectors will not affect the address or vector assignments of devices with floating addresses and vectors.

5. Indicate that all devices have been entered by pressing the CTRL and Z keys simultaneously:

```
DEVICE> ^Z
```

SYSGEN will list the addresses and vectors of the devices entered in the format shown in Figure 3-1.

```
SYSGEN>  CONFIGURE
DEVICE> DZ11
DEVICE> DMC11
DEVICE> DHU11,2
DEVICE> ^Z
Device: DMC11   Name: XMA    CSR: 760070*   Vector: 300*   Support: yes
Device: DZ11    Name: TTA    CSR: 760110*   Vector: 310*   Support: yes
Device: DHU11   Name: COMB   CSR: 760500*   Vector: 320*   Support: yes
Device: DHU11   Name: COMB   CSR: 760520*   Vector: 330*   Support: yes

*Floating address or vector.
```

Figure 3-1. CONFIGURE Device Listing

6. Note the CSR addresses listed for the UNIBUS devices in floating address space. Program the listed addresses into non-Emulex devices as instructed by that manufacturer's documentation. For the CS23/E1, program the address given for the first device (lowest numerical address) into the CC23 Controller as described in subsection 4.4.3.

7. A command to initiate autoconfigure during power-up must be included in one of several start up command files on the system. As shipped from DEC, this command is included in SYS$SYSTEM:STARTUP.COM file. See Figure 3-2 for an example of the command.

8. Emulex recommends setting the default line parameters as shown in Figure 3-2.

```
$!
$!       TXA0: IS NOW CONNECTED TO A DIAL UP LINE AND A MODEM
$!
$SET TERMINAL TXA0:/SPEED=1200/MODEM/HANGUP/VT100/PERM
$!
$SET TERMINAL TXA1:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA2:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA2:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA3:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA4:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA5:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA6:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA7:/SPEED=9600/PERM/VT100
$SET TERMINAL TXB0:/SPEED=9600/PERM/VT100
$SET TERMINAL TXB1:/SPEED=9600/PERM/VT100
$SET TERMINAL TXB2:/SPEED=9600/PERM/VT100
$SET TERMINAL TXB3:/SPEED=9600/PERM/VT100
$SET TERMINAL TXB4:/SPEED=9600/PERM/VT100
$SET TERMINAL TXB5:/SPEED=9600/PERM/VT100
$SET TERMINAL TXB6:/SPEED=9600/PERM/VT100
$SET TERMINAL TXB7:/SPEED=9600/PERM/VT100
```

Figure 3-2. DHU11 Autoconfigure Command File

3.8.2 ADDING A NEW DEVICE TO ULTRIX-32 (V1.1)

Support for new devices MUST be included in a monitor at SYSGEN time. The configuration file is edited to reflect the number of controllers and devices connected to each controller.

The following example is from a configuration file that specifies a single CS23/E1 controller:

```
device dhu0 at uba0 csr 0160440 flags 0xff vector dhurint dhuxint
```

The flag value is a binary value that specifies which terminals are 'hard wired', where bit zero corresponds to therminal line 0, etc.

3.8.2.1 Autoconfigure

At boot time, Ultrix-32 attempts to auto-configure the devices included in the booted monitor's configuration file. If the device was not included in the configuration file, it will not be configured into the running system. If the device was included, but is not present, Ultrix-32 will skip it.

When Ultrix-32 finds a device at autoconfigure time it prints a message as follows:

```
dhu0 at uba0 at csr 160440 vec 300, ipl 15
```

The CSR addresses were set in the configuration file. The vectors are set with the switches on the controller board. The operating system 'pokes' the device and records it's interrupt vector address. If the CSR doesn't match the configuration file, the device will be skipped (and no message will be printed).

3.8.2.2 Enabling Terminals

To enable terminals, there must be a special file created for each line of each emulation of the CS23/E1. Also the files 'ttys' and 'ttytype' must be edited to reflect the number, availability, and terminal types for each line.

3.8.2.2.1 /dev/ttyxx

The special files can be created with the supplied command file 'MAKEDEV' in the /dev account. It will create the special files for the devices specified. For example:

```
# MAKEDEV dhu0
```

will create the 16 special files for the CS23/E1.

3.8.2.2.2 /etc/ttys

The 'ttys' file is used by the 'init' program to determine which terminals to create the login process for (and allow logins). The first digit is either '0' or '1'. If the first character is a a zero (0), the 'init' program ignores that line. If the first character is a one (1), the 'init' program creates a login process for that line. The second character is an argument to the 'getty' program. It determines the autobaud speed detection pattern. The remainder of the line is the terminal's entry in the device directory, /dev. An example of this file follows:

```
l2console
l2ttyA0
l2ttyA1
l2ttyA2
l2ttyA3
l2ttyA4
l2ttyA5
l2ttyA6
l2ttyA7
l2ttyA8
l2ttyA9
l2ttyAa
l2ttyAb
l2ttyAc
l2ttyAd
l2ttyAe
l2ttyAf
```

3.8.2.2.3 /etc/ttytype

The 'ttytype' file is used by the 'login' program to initialize TERM variables at login time. An example of this file is:

```
vtl00 console
vtl00 ttyA0
vtl00 ttyA1
vtl00 ttyA2
vtl00 ttyA3
vtl00 ttyA4
vtl00 ttyA5
vtl00 ttyA6
vtl00 ttyA7
vtl00 ttyA8
vtl00 ttyA9
vtl00 ttyAa
vtl00 ttyAb
vtl00 ttyAc
vtl00 ttyAd
vtl00 ttyAe
vtl00 ttyAf
```

For more information on configuring terminals, see PART 5 "Installing and operating 4.2BSD on the VAX" in the Ultrix-32 Supplementary Documents, Volume III, System Managers manual.

4.1 OVERVIEW

This section describes the procedures for installing and checking the CS23/E1 Communications Subsystem. The subsection titles are listed below to serve as an outline of the procedure.

Subsection	Title
4.1	Overview
4.2	Inspection
4.3	Subsystem Configurations
4.4	CC23 Controller Setup
4.5	Distribution Panel Setup
4.6	CC23 Controller Installation
4.7	Distribution panel Installation
4.8	Subsystem Cabling
4.9	Subsystem Power-Up and Verification

The information contained in this section is limited to switch setting data and physical installation instructions. No attempt is made to describe the many subsystem configurations that are possible. **If you are not familiar with the possible configurations, we strongly recommend reading Section 3, Planning the Installation, before attempting to install this subsystem.**

4.1.1 MAINTAINING FCC CLASS A COMPLIANCE

The CC23 Controller and the distribution panels are designed to be embedded in a shielded cabinet. Emulex has tested the CS23/E1 Communications Subsystem with DEC computers that comply with FCC Class A limits for radiated and conducted interference. When properly installed, the CS23/E1 does not cause compliant computers to exceed Class A limits.

The CC23 Controller and the distribution panels can be installed two ways:

- Both mounted in the same CPU cabinet, or
- With the CC23 mounted in the CPU cabinet and the distribution panels mounted in a separate expansion cabinet.

To limit radiated interference, DEC completely encloses the components of their computers that generate or could conduct radio frequency interference (RFI) with a grounded metal shield (earth ground). When installing these embedded components, nothing must be

done that would reduce this shield's effectiveness. That is, when the installation is complete, no gap in the shield that would allow RFI to escape can be allowed.

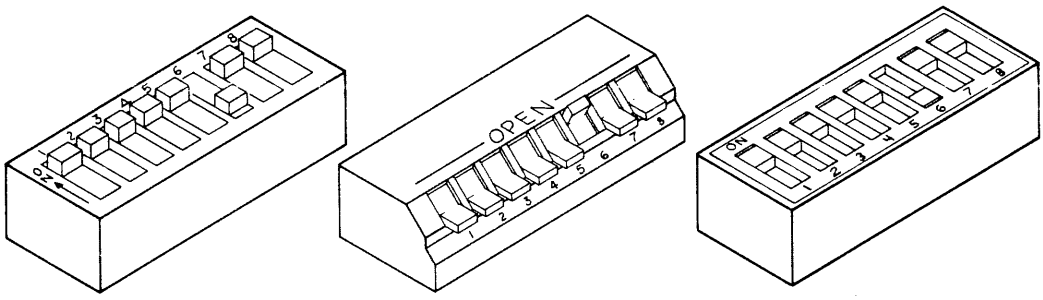
Conducted interference is generally prevented by installing a filter in the ac line between the computer and the ac outlet. Most power distribution panels that are of current manufacture contain suitable filters.

Details on mounting the distribution panel to maintain FCC Class A compliance are in the installation section of your distribution panel technical manual. Note that special cabling and hardware are needed if the distribution panel is mounted in a separate cabinet.

4.1.2 DIP SWITCH TYPES

Switch-setting tables in this manual use the numeral one (1) to indicate the ON (closed) position and the numeral zero (0) to indicate the OFF (open) position.

The two DIP switch types used in this product are shown in Figure 4-1. All switches are set to the code shown in the switch setting example.



CS2301-0034

----------SW1----------							
1	2	3	4	5	6	7	8
1	1	1	1	1	0	1	1

Figure 4-1. Switch Setting Example

4.1.3 INSTALLATION CHECKLIST

The Installation Checklist, Table 4-1 is designed to provide a condensed version of the installation procedure. It contains as few details as possible; the entire Installation Section should be used to actually install your CS23/E1.

Table 4-1. Installation Checklist

____	1.	Unpack the equipment you have received and check it against the shipping list. Inspect the equipment for damage.
____	2.	Determine your subsystem configuration. Fill out the Configuration Record Sheet (Figure 4-2).
____	3.	Set the switches and jumpers on the CC23 Controller to comply with the Configuration Reference Sheet.
____	4.	Set the remaining controller switches for number of emulations, bus request level, UNIBUS address, etc.
____	5.	Set any jumpers on each distribution panel (using the distribution panel technical manual).
____	6.	Install the CC23 Controller in the UNIBUS backplane.
____	7.	Install the distribution panel(s) in the CPU or expansion cabinet (using the distribution panel technical manual).
____	8.	Connect the two 50-pin cables to each distribution panel (using the distribution panel technical manual).
____	9.	Power up the CPU.
____	10.	Check the LEDs on the CC23 Controller to verify proper installation.

4.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal shipping conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

Unpack the CC23/E1 Communications Subsystem and, using the shipping invoice, verify that all equipment is present. Verify also that model or part number (P/N) designation, revision level, and serial numbers agree with those on the shipping invoice. Subsection 1.4 explains model numbers and details kit contents. These verifications are important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately. If the equipment must be returned to Emulex, it should be shipped in the original container.

Visually inspect all components after unpacking. Check for such items as bent or broken connector pins, damaged components or any other evidence of physical damage.

Examine all socketed components carefully to ensure they are properly seated.

4.3 SUBSYSTEM CONFIGURATIONS

Before installing your subsystem, determine the subsystem configuration you want and fill out the Configuration Record Sheet provided in Figure 4-2. If you are not familiar with the possible configurations, please read Section 3, Planning the Installation.

GENERAL INFORMATION

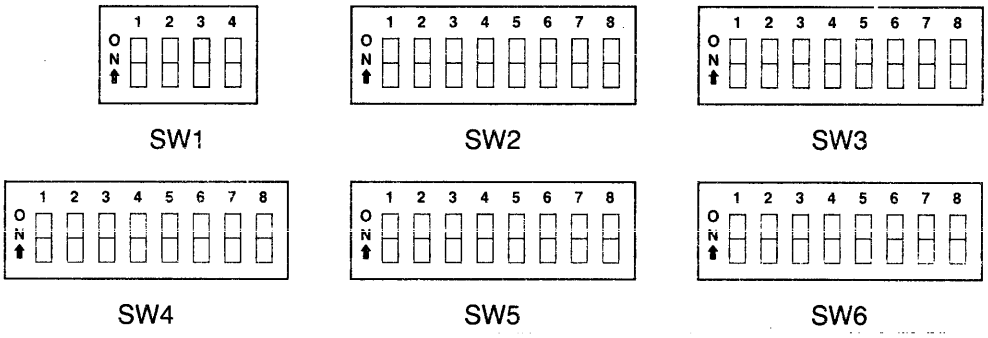
1. Host computer type _____
2. Host computer operating system _____
3. Type of memory _____
4. Amount of memory _____
5. Number of emulations (circle one) 1 2

CS23/E1 COMMUNICATIONS SUBSYSTEM

1. Distribution panel #1 _____
2. Distribution panel #2 _____
3. DIP header (circle if installed) U49 U65

CC23/E1 CONTROLLER

1. Emulation PROM numbers range from _____ to _____
2. Address Range Decode PROM number _____
3. Warranty expiration date _____
4. Top assembly number _____
5. Serial number _____
6. Switch settings:



7. Unibus addresses _____ and _____
8. Interrupt vector addresses _____ and _____

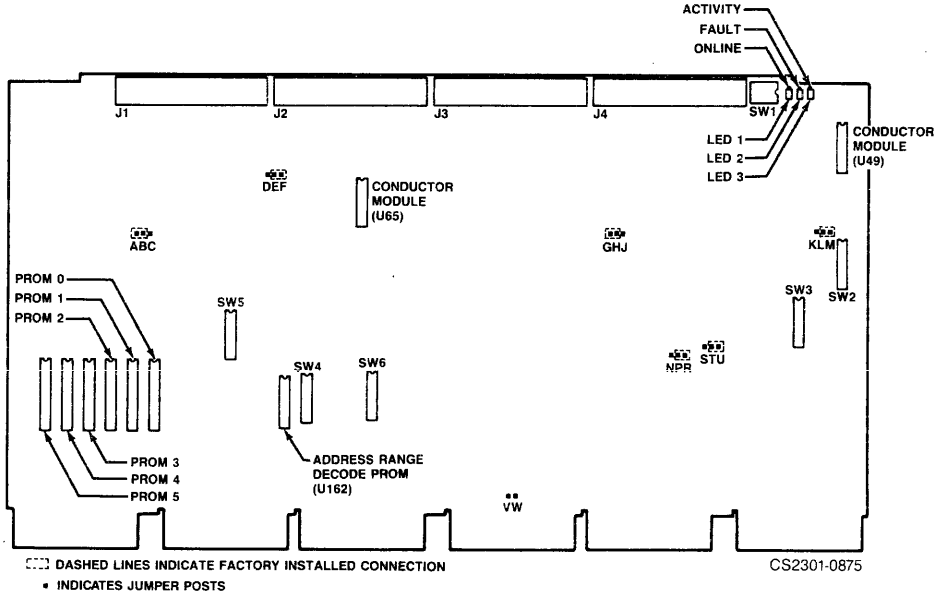


Figure 4-2. CS23/E1 Configuration Reference Sheet

CS2301-0991

4.4 CC23 CONTROLLER SETUP

Figure 4-3 shows the locations of the configuration switches and jumpers referenced in the subsections below. Set the configuration switches before the unit is installed in the CPU card cage because they are not accessible after installation.

NOTE

If any switch position is changed on the CC23 Controller, the unit must be reset either by using switch SW1-1 or removing and restoring the unit's power. This reset is required because the switches are read by an initialization routine in the unit's firmware.

Table 4-2 defines the function and factory configuration of all switches on the CC23 Controller. Table 4-3 defines the functions and factory configuration of all jumpers on the CC23 Controller.

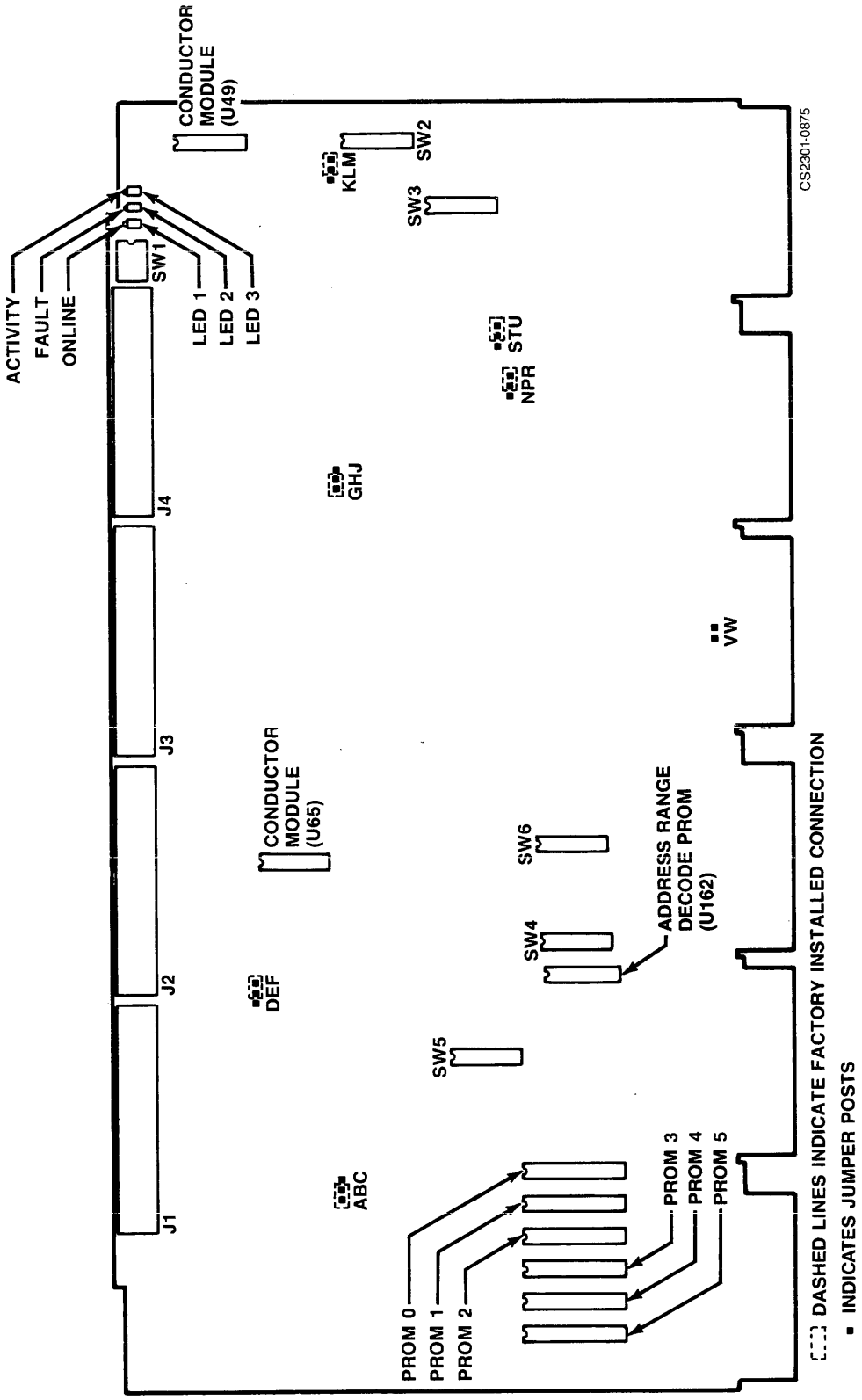


Figure 4-3. CC23 Controller Component Locations

Table 4-2. CC23 Controller Switch Definitions and Factory Configuration

SWITCH	OFF(0)	ON(1)	Factory	Function	Section
SW1-1	Run	Halt-Reset	OFF(0)	Controller Run vs. Halt	4.4.5.1
SW1-2	-	Int Test	OFF(0)	Internal Test Select	4.4.5.2
SW1-3	-	Int Test	OFF(0)	Internal Test Select	4.4.5.2
SW1-4	-	Int Test	OFF(0)	Internal Test Select	4.4.5.2
SW2-1	-	-	OFF(0)*	Factory Configuration	
SW2-2	Disable	Enable	OFF(0)*	38,400 Baud vs. 2000 Baud	4.4.5.3
SW2-3	Disable	Enable	OFF(0)	Force Two Stop Bits	4.4.5.4
SW2-4	Disable	Enable	OFF(0)	Multi-Word DMA Transfer	4.4.5.5
SW2-5	-	-	OFF(0)*	Factory Configuration	
SW2-6	-	-	OFF(0)*	Factory Configuration	
SW2-7	-	-	OFF(0)*	Factory Configuration	
SW2-8	-	-	OFF(0)*	Factory Configuration	
SW3-1	-	-	OFF(0)*	Factory Configuration	
SW3-2	-	-	OFF(0)*	Factory Configuration	
SW3-3	-	-	OFF(0)*	Factory Configuration	
SW3-4	-	-	OFF(0)*	Factory Configuration	
SW3-5	-	-	OFF(0)*	Factory Configuration	
SW3-6	-	-	OFF(0)*	Factory Configuration	
SW3-7	Enable	Disable	ON(1)	Steal Grant[1]	4.4.5.6
SW3-8	BR6/BG6	BR5/BG5	ON(1)	Bus Request/Bus Grant	4.4.4.2
SW4-1	-	-	NS	DHU11 UNIBUS Address	4.4.3
SW4-2	-	-	NS	DHU11 UNIBUS Address	4.4.3
SW4-3	-	-	NS	DHU11 UNIBUS Address	4.4.3
SW4-4	-	-	NS	DHU11 UNIBUS Address	4.4.3
SW4-5	-	-	NS	DHU11 UNIBUS Address	4.4.3
SW4-6	-	-	NS	DHU11 UNIBUS Address	4.4.3
SW4-7	-	-	NS	DHU11 UNIBUS Address	4.4.3
SW4-8	One	Two	ON(1)	Number of DHU11 Emulations	4.4.2
SW5-1	-	-	NS	DHU11 Vector Address	4.4.4.1
SW5-2	-	-	NS	DHU11 Vector Address	4.4.4.1
SW5-3	-	-	NS	DHU11 Vector Address	4.4.4.1
SW5-4	-	-	NS	DHU11 Vector Address	4.4.4.1
SW5-5	-	-	NS	DHU11 Vector Address	4.4.4.1
SW5-6	-	-	NS	DHU11 Vector Address	4.4.4.1
SW5-7	-	-	OFF(0)*	Factory Configuration	
SW5-8	-	-	OFF(0)*	Factory Configuration	

[1]Does not function on Rev A PWBs. See subsection 4.4.5.6.

continued on next page

Table 4-2. CC23 Controller Switch Definitions and Factory Configuration (continued)

SWITCH	OFF(0)	ON(1)	Factory	Function	Section
SW6-1	-	-	OFF(0)*	Hardware Flow Control	4.4.5.7
SW6-2	-	-	OFF(0)*	Hardware Flow Control	4.4.5.7
SW6-3	-	-	OFF(0)*	Hardware Flow Control	4.4.5.7
SW6-4	-	-	OFF(0)*	Hardware Flow Control	4.4.5.7
SW6-5	-	-	OFF(0)*	Hardware Flow Control	4.4.5.7
SW6-6	-	-	OFF(0)*	Level Flow Control Mode	4.4.5.8
SW6-7	-	-	OFF(0)*	Level Flow Control Mode	4.4.5.8
SW6-8	-	-	OFF(0)*	Factory Configuration	

ON(1) = Closed
OFF(0) = Open
* = Switch **must** be in factory setting
NS = no standard
DMA = Direct Memory Access

Table 4-3. CC23 Controller Jumper Definition/Factory Configuration

Jumper	Factory Setting	Function (when connected)
A to B	Jumpered	DCD biased OFF for first distribution panel. CTS biased OFF for channels 0 through 3 of a 12-channel panel.
B to C	Not connected	DCD biased ON for first distribution panel. CTS biased ON for channels 0 through 3 of a 12-channel panel.
D to E	Not connected	RI biased ON for first distribution panel. DSR biased ON for channels 0 through 3 of a 12-channel panel.
E to F	Jumpered	RI biased OFF for first distribution panel. DSR biased OFF for channels 0 through 3 of a 12-channel panel.
G to H	Jumpered	DCD biased OFF for second distribution panel. CTS biased OFF for channels 0 through 3 of a 12-channel panel.
H to J	Not connected	DCD biased ON for second distribution panel. CTS biased ON for channels 0 through 3 of a 12-channel panel.
K to L	Not connected	RI biased ON for second distribution panel. DSR biased ON for channels 0 through 3 of a 12-channel panel.
L to M	Jumpered	RI biased OFF for second distribution panel. DSR biased OFF for channels 0 through 3 of a 12-channel panel.
N to P	Not connected	Factory test
P to R	Jumpered	Hardware configuration - leave out for normal operation
S to T	Not connected	Not used
T to U	In etch	RAM size select
V to W	Not connected	Factory test - leave out for normal operation

4.4.1 DIP HEADER CONFIGURATION

When the CC23 is used with CP23 or CP25 Distribution Panels, DIP headers must be inserted in the CC23 Controller to provide power. Those two panels require power (+5V and -15V); power is not required to operate the CP22 or the CP26 Distribution Panels. The DIP headers are shipped with the CP23 and CP25 panels.

The CC23 Controller is shipped with conductor modules (also known as zero-ohm packs) installed in locations U49 and U65. When using the CP23 and CP25 panels, the conductor modules must be replaced with the DIP headers. One conductor module corresponds to the first distribution panel (the panel connected to J1 and J2 on the CC23), and the other corresponds to the second distribution panel (the panel connected to J3 and J4 on the CC23). If a CP22 or a CP26 is used, the conductor module for that panel **must** be left on the CC23.

The DIP header can be inserted in two different directions. Only one direction will allow the header to supply the necessary power. Use Figure 4-4 to determine the proper orientation of the DIP headers. Use the table below to determine which conductor modules to replace.

WARNING

If the DIP header is installed in the orientation shown in Figure 4-4 and a CP22 or CP26 panel is installed, the fuse on the DIP header will blow. Therefore, if installing a CP22 or CP26, reverse the orientation of the DIP header or replace it with conductor modules.

Socket Location	CC23 PCBA Connectors	Distribution Panel
U65	J1 and J2	First
U49	J3 and J4	Second

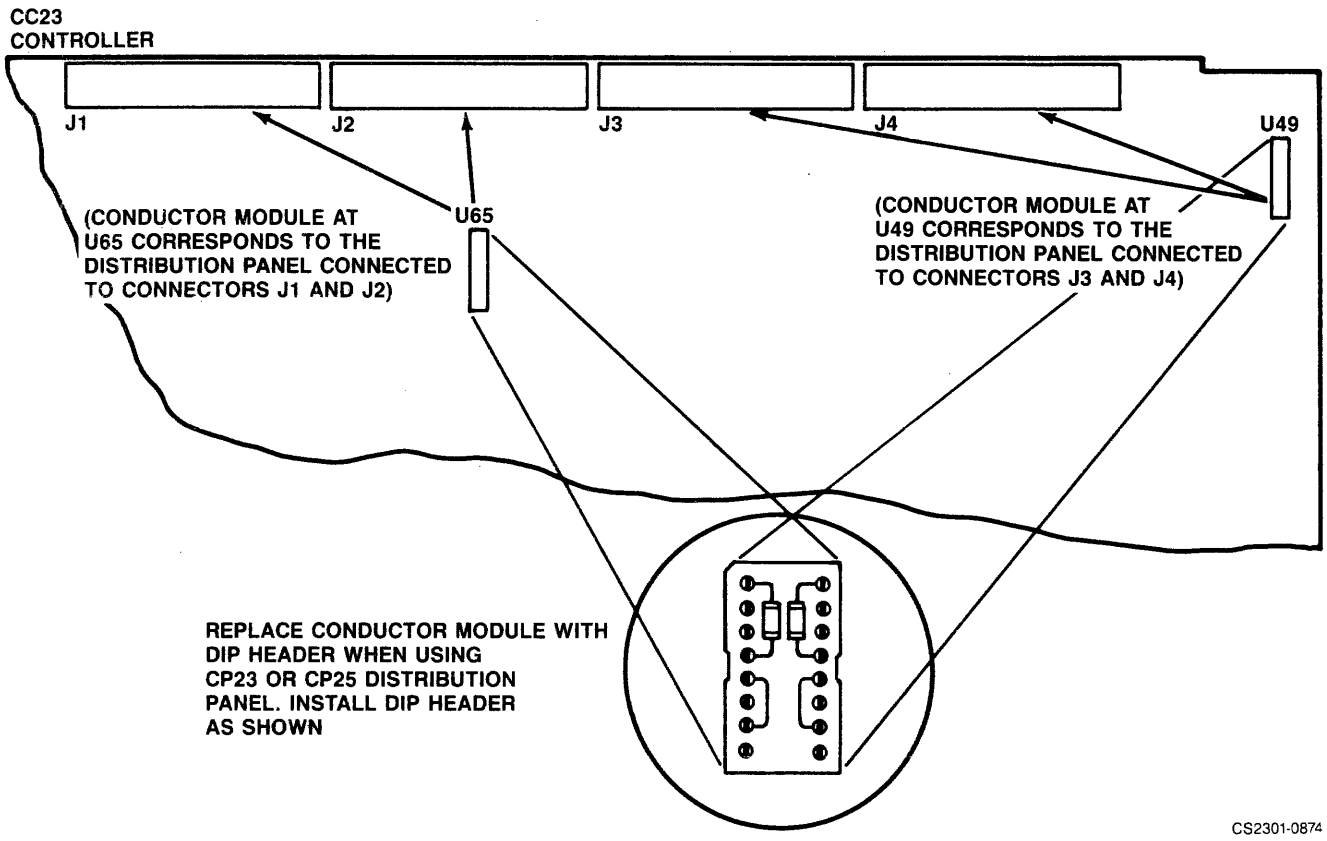


Figure 4-4. CC23 DIP Header Orientation

4.4.2 NUMBER OF DHU11 EMULATIONS

The number of asynchronous 16-line DHU11 emulations performed by the CS23/E1 and seen by the operating system is determined by the setting of switch SW4-8. The CS23/E1 can perform one or two DHU11 emulations. See subsection 3.6 for an explanation of channel numbering.

Switch	OFF	ON	Factory
SW4-8	One	Two	ON

4.4.3 DHU11 DEVICE REGISTER ADDRESSES

DHU11-type devices are assigned UNIBUS addresses from the floating address section of the UNIBUS I/O page. See Appendix A for a detailed discussion of the autoconfigure algorithm.

When you have determined the proper address for the first CSR of the first DHU11 emulation, set CC23 Controller switches SW4-1 through SW4-7 according to Table 4-4. The CS23/E1 will calculate the other register addresses for the first emulation, as well as the register addresses for the subsequent emulation. The CSR addresses of the subsequent emulation is located consecutively on modulo-20_8 boundaries. That is, if the switches are set to select an address of 760340_8 for the first DHU11 emulation, the second emulation responds to addresses beginning at 760360_8.

NOTE

Address Range Decode PROMs that provide address ranges in addition to those listed in Table 4-4 are available by special order from Emulex. Contact your local Emulex sales representative, or:

Emulex In-House Sales
3545 Harbor Boulevard
Costa Mesa CA 92626
(800) EMULEX3
or
(714)662-5600
or
TWX 910-595-2521

1st CSR 160440
VEC 300

2nd CSR 160500
VEC 320

Table 4-4. CC23 Controller UNIBUS Address Selection

CC23 Address in octal	SW4 1	2	3	4	5	6	7	CC23 Address in octal	SW4 1	2	3	4	5	6	7
760000[1]	0	0	0	0	1	0	1	762000	0	0	0	0	0	1	1
760020	1	0	0	0	1	0	1	762020	1	0	0	0	0	1	1
760040	0	1	0	0	1	0	1	762040	0	1	0	0	0	1	1
760060	1	1	0	0	1	0	1	762060	1	1	0	0	0	1	1
760100	0	0	1	0	1	0	1	762100	0	0	1	0	0	1	1
760120	1	0	1	0	1	0	1	762120	1	0	1	0	0	1	1
760140	0	1	1	0	1	0	1	762140	0	1	1	0	0	1	1
760160	1	1	1	0	1	0	1	762160	1	1	1	0	0	1	1
760200	0	0	0	1	1	0	1	762200	0	0	0	1	0	1	1
760220	1	0	0	1	1	0	1	762220	1	0	0	1	0	1	1
760240	0	1	0	1	1	0	1	762240	0	1	0	1	0	1	1
760260	1	1	0	1	1	0	1	762260	1	1	0	1	0	1	1
760300	0	0	1	1	1	0	1	762300	0	0	1	1	0	1	1
760320	1	0	1	1	1	0	1	762320	1	0	1	1	0	1	1
760340	0	1	1	1	1	0	1	762340	0	1	1	1	0	1	1
760360[2]	1	1	1	1	1	0	1	762360[2]	1	1	1	1	0	1	1
760400	0	0	0	0	1	0	0	762400	0	0	0	0	0	1	0
760420	1	0	0	0	1	0	0	762420	1	0	0	0	0	1	0
760440	0	1	0	0	1	0	0	762440	0	1	0	0	0	1	0
760460	1	1	0	0	1	0	0	762460	1	1	0	0	0	1	0
760500	0	0	1	0	1	0	0	762500	0	0	1	0	0	1	0
760520	1	0	1	0	1	0	0	762520	1	0	1	0	0	1	0
760540	0	1	1	0	1	0	0	762540	0	1	1	0	0	1	0
760560	1	1	1	0	1	0	0	762560	1	1	1	0	0	1	0
760600	0	0	0	1	1	0	0	762600	0	0	0	1	0	1	0
760620	1	0	0	1	1	0	0	762620	1	0	0	1	0	1	0
760640	0	1	0	1	1	0	0	762640	0	1	0	1	0	1	0
760660	1	1	0	1	1	0	0	762660	1	1	0	1	0	1	0
760700	0	0	1	1	1	0	0	762700	0	0	1	1	0	1	0
760720	1	0	1	1	1	0	0	762720	1	0	1	1	0	1	0
760740	0	1	1	1	1	0	0	762740	0	1	1	1	0	1	0
760760[2]	1	1	1	1	1	0	0	762760[2]	1	1	1	1	0	1	0

[1]Illegal for use with VMS
[2]Do not use if two emulations are enabled

0 = OFF (open) 1 = ON (closed)

Example 4-1: CS23/E1 performing two DHU11 emulations. Address of first DHU11 emulation set to 760260_8 using SW4.

Emulation Number	CS23/E1 Address	SW4 1	2	3	4	5	6	7
1	760260_8	1	1	0	1	1	0	1
2	760300_8							

0 = OFF (open) 1 = ON (closed)

4.4.4 INTERRUPT SETUP

4.4.4.1 Interrupt Vector Address Selection

A floating vector convention is used to select vectors for DHU11-type devices. These vector addresses are assigned from the floating vector block that starts at address 300_8 and proceeds upwards to 777_8. See Appendix A for a detailed description of the vector selection algorithm.

Table 4-5. DHU11 Vector Address Selection

Octal Address	SW5 1	2	3	4	5	6	Octal Address	SW5 1	2	3	4	5	6
300	1	1	1	0	0	1	540	1	1	0	0	1	0
310	0	1	1	0	0	1	550	0	1	0	0	1	0
320	1	0	1	0	0	1	560	1	0	0	0	1	0
330	0	0	1	0	0	1	570	0	0	0	0	1	0
340	1	1	0	0	0	1	600	1	1	1	1	0	0
350	0	1	0	0	0	1	610	0	1	1	1	0	0
360	1	0	0	0	0	1	620	1	0	1	1	0	0
370	0	0	0	0	0	1	630	0	0	1	1	0	0
400	1	1	1	1	1	0	640	1	1	0	1	0	0
410	0	1	1	1	1	0	650	0	1	0	1	0	0
420	1	0	1	1	1	0	660	1	0	0	1	0	0
430	0	0	1	1	1	0	670	0	0	0	1	0	0
440	1	1	0	1	1	0	700	1	1	1	0	0	0
450	0	1	0	1	1	0	710	0	1	1	0	0	0
460	1	0	0	1	1	0	720	1	0	1	0	0	0
470	0	0	0	1	1	0	730	0	0	1	0	0	0
500	1	1	1	0	1	0	740	1	1	0	0	0	0
510	0	1	1	0	1	0	750	0	1	0	0	0	0
520	1	0	1	0	1	0	760	1	0	0	0	0	0
530	0	0	1	0	1	0	770	0	0	0	0	0	0

0 = OFF (open) 1 = ON (closed)

Each DHUl1 emulation requires two interrupt vector addresses, one for the receive function and one for the transmit function. The receive vector is first, and it is always on a modulo-10 boundary (XX0). It is followed consecutively by the transmit vector on a modulo-four boundary (XX4). The DHUl1 interrupt vector addresses are set using six switches as specified in Table 4-5. Only the receive vector of the first emulation is selected using Table 4-5. The transmit vector follows the receive vector, and is automatically assigned by the firmware. The interrupt vectors for the second emulation follow the transmit and receive vectors for the first emulation.

Example 4-2. Two DHUl1 emulations. Using Table 4-5, switch SW5 is set to select a receive vector address of 340_8 for the first DHUl1.

	DHUl1 Emulation Number	DHUl1 Vector	-------- SW5 -------- 1 2 3 4 5 6
Receive	1	340_8	1 1 0 0 0 1
Transmit		344_8	
Receive	2	350_8	
Transmit		354_8	
0 = OFF (open) 1 = ON (closed)			

4.4.4.2 Bus Request/Grant Level Selection

Switch SW3-8 selects bus priority level five or six for the CS23/El. The standard setting is for level 5.

Switch	OFF	ON	Factory
SW3-8	BR6/BG6	BR5/BG5	ON

4.4.5 OPTION SWITCHES

Other switches are used to select various options. This subsection explains those switch functions and options.

4.4.5.1 CC23 Run vs Halt/Reset (SW1-1)

When placed in the ON (closed) position, switch SW1-1 halts and resets the CC23 microprocessor. Upon placing the switch back in the OFF (open) position, the CC23 Controller executes its power-up self-diagnostic and its initialization routine.

When left ON, this switch effectively places CC23/E1 offline without having to actually remove it from the UNIBUS. Bus grant continuity is provided in this condition.

CAUTION

Toggling the reset switch (SW1-1) should always be done when the system is offline. On many operating systems, toggling this CC23 Controller switch causes a system crash.

Switch	OFF	ON	Factory
SW1-1	Normal	Halt/Reset	OFF

4.4.5.2 Internal Test Select (SW1-2 through SW1-4)

Switches SW1-2 through SW1-4 select one of four internal micro tests. The available selections are briefly described in Table 4-6 (see Section 5 for further details). To activate these tests, set the switches to the desired mode, then toggle the Reset switch (SW1-1).

NOTE

Switches SW1-2 through SW1-4 must be OFF (open) for normal operation of the controller. Test modes three and four (see Table 4-6) are used for off-line testing only.

Table 4-6. CC23 Internal Micro Test

Test Mode	Test Mode Description	--SW1-- 2	3	4
1	Normal Run Mode - LED2 (Fault LED) blinks if any channel fails internal loopback test.	0	0	0
2	Override Mode - LED2 (Fault LED) blinks only if no channels pass internal loopback test. Controller will run with lines that pass.	0	0	1
3	Continuous External Loopback Mode - LED2 (Fault LED) blinks if any error is detected on any channel.	0	1	0
4	Search Mode - LED2 (Fault LED) goes off if at least one channel is good. If no channels are good, the Fault LED blinks.	0	1	1
5	Echo Mode - Characters received from any terminal will be echoed.	1	0	0
0 = OFF (open) 1 = ON (closed)				

4.4.5.3 38,400 Baud vs. 2000 Baud (SW2-2)

When this option is enabled (ON) and the operating system attempts to set the data rate to 2000 bps (see Table 6-1), the rate is actually set to 38,400 bps. When this option is disabled (OFF) and the operating system attempts to set the data rate to 2000 bps, the attempt is successful.

Switch	OFF	ON	Factory
SW2-2	Disable	Enable	OFF

4.4.5.4 CC23 Force Two Stop Bits (SW2-3)

This option overrides operating system control of the number of stop bits per character. This option is useful in situations where a continuous stream of asynchronous characters are being transmitted and the transmit station's data rate is slightly faster than the receive station's rate. In some cases one stop bit between characters does not allow enough time for the receiving device to synchronize on the start bit that immediately follows the single stop

bit. Two stop bits simply allow more time between characters to ensure that the receiving device has enough time to internally set up to sense the next start bit.

Switch	OFF	ON	Factory
SW2-3	Disable	Enable	OFF

4.4.5.5 Multi-Word DMA Transfer (SW2-4)

When this option is enabled the CC23 performs DMA transfers in eight-byte (four word) increments at a time. When this option is disabled, the CC23 performs DMA transfers in two-byte increments.

Switch	OFF	ON	Factory
SW2-4	Disable	Enable	OFF

4.4.5.6 Steal Grant (SW3-7)

This option is designed to improve UNIBUS latency by 'stealing' a bus grant that is intended for a lower priority device. If the CC23 receives a bus grant while bus non-processor request (BNPR) is asserted, the CC23 will passively release the UNIBUS, and the device that raised the NPR will not be delayed.

Switch	OFF	ON	Factory
SW3-7	Enable	Disable	ON

NOTES

This option functions only on CC23 boards that are Rev B and above. The rev level of the PWB is printed in etch adjacent to the PWB part number on the solder side of the board.

Some Q-Bus-to-UNIBUS converters cannot operate with a Steal Grant option enabled. When using the CC23 on a Q-Bus-to-UNIBUS converter check the documentation for the converter to determine if such a restriction is noted before enabling this option.

4.4.5.7 Hardware Level Flow Control (SW6-1 through SW6-6)

Switches SW6-1 through SW6-6 control which channels are enabled for hardware level flow control. These switches also control whether the DCD or CTS signals are used to control inbound data. This option is explained in greater detail in subsection 3.4. Table 4-7 shows the switch settings for the hardware flow control feature.

NOTE

Switches SW6-1 through SW6-7 must be OFF (open) for the DEC PDP-11 and VAX-11 Diagnostics to run without unpredictable errors.

Table 4-7. Hardware Flow Control Switch Settings

Channels Selected		Signals	SW6				
12 Channel Panel	16 Channel Panel	Enabled	5	4	3	2	1
none	none	none	0	0	0	0	0
11	15	DCD/DTR	0	0	0	0	1
11-10	15-14	DCD/DTR	0	0	0	1	0
11-9	15-13	DCD/DTR	0	0	0	1	1
11-8	15-12	DCD/DTR	0	0	1	0	0
11-7	15-11	DCD/DTR	0	0	1	0	1
11-6	15-10	DCD/DTR	0	0	1	1	0
11-5	15-9	DCD/DTR	0	0	1	1	1
11-4	15-8	DCD/DTR	0	1	0	0	0
11-3	15-7	DCD/DTR	0	1	0	0	1
11-2	15-6	DCD/DTR	0	1	0	1	0
11-1	15-5	DCD/DTR	0	1	0	1	1
11-0	15-4	DCD/DTR	0	1	1	0	0
11-0	15-3	DCD/DTR	0	1	1	0	1
11-0	15-2	DCD/DTR	0	1	1	1	0
11-0	15-1	DCD/DTR	0	1	1	1	1
none	none	none	1	0	0	0	0
7	none	CTS/DTR	1	0	0	0	1
7-6	none	CTS/DTR	1	0	0	1	0
7-5	none	CTS/DTR	1	0	0	1	1
7-4	none	CTS/DTR	1	0	1	0	0
7-3	none	CTS/DTR	1	0	1	0	1
7-2	none	CTS/DTR	1	0	1	1	0
7-1	none	CTS/DTR	1	0	1	1	1
7-0	none	CTS/DTR	1	1	0	0	0
7-0	none	CTS/DTR	1	1	0	0	1
7-0	none	CTS/DTR	1	1	0	1	0
7-0	none	CTS/DTR	1	1	0	1	1
7-0	none	CTS/DTR	1	1	1	0	0
7-0	none	CTS/DTR	1	1	1	0	1
7-0	none	CTS/DTR	1	1	1	1	0
7-0	none	CTS/DTR	1	1	1	1	1

0 = OFF (open) 1 = ON (closed)

4.4.5.8 Level Flow Control Mode

Three types of level flow control are available for the CS23/E1:

- Mode 1 - Basic Level Flow Control
- Mode 2 - Software Assisted Level Flow Control
- Mode 3 - XON/XOFF Conversion Level Flow Control

Each type is described in detail in subsection 3.5. Table 3-8 lists the switch settings for each mode.

NOTE

Switches SW6-1 through SW6-7 must be OFF for the DEC PDP-11 and VAX-11 Diagnostics to run without unpredictable errors.

Table 4-8. Level Flow Control Mode Selection

Mode	-SW6- 6	7	Factory
1 - Basic Level Flow Control	0	0	√
2 - Software Assisted Level Flow Control	1	0	
3 - XON/XOFF Conversion Level Flow Control	0	1	
0 = OFF (open) 1 = ON (closed)			

4.4.6 MODEM SIGNAL BIAS JUMPERS OPTION

The bias levels for unconnected incoming modem signals DCD (Data Carrier Detected), RI (Ring Indicator), CTS (Clear To Send), and DSR (Data Set Ready), are controlled by jumper options. When an incoming modem signal is not being driven by a modem or other device, these jumpers will control whether the operating system interprets this unconnected signal as ON (Asserted) or OFF (Unasserted). When an incoming modem signal is connected to a modem or other device, the position of the jumpers has no effect on how the operating system interprets the signal.

If the operating system is set to work with modem signals on a particular line, and the incoming modem signals are not being driven by the connected device, **one** of the following three things must be done:

- The operating system configuration for that line must be changed to non-modem operation
- Those modem signals must be physically connected to another asserted modem signal within the 25 pin connector
- The bias jumpers must be set to the asserted condition

Table 4-3 describes which jumpers control biasing. Please note that changing a jumper will change the biasing for all other similar unconnected modem signals on a particular panel. All of the incoming modem signals are biased OFF in the factory jumper settings. To change

a bias from the factory setting, a jumper must be removed, and another one installed in a different position. For example, to bias DCD ON for the first panel, the wire between jumpers A and B must be removed, and a wire must be wrapped between jumper posts B and C. If this panel is a 12 channel panel, CTS of channels 0 through 3 will also be biased ON now. CTS for channels 4 through 7 of a 12 channel panel cannot be biased ON, and will always be biased OFF when left unconnected.

4.5 DISTRIBUTION PANEL SETUP

Before you begin the installation of the CS23/E1 Subsystem, you may need to set certain jumpers on the distribution panel(s). See the setup section of your distribution panel manual for details.

When you are finished setting up the distribution panel(s), return to this manual for instructions on installing the CC23 in the UNIBUS backplane.

4.6 CC23 CONTROLLER INSTALLATION

4.6.1 SYSTEM PREPARATION

Power down the system and switch OFF the main AC breaker. Remove the side covers from the CPU cabinet and make the UNIBUS accessible.

4.6.2 SPC SLOT SELECTION

The CC23 Controller can be inserted into any PDP-11 or VAX-11 UNIBUS SPC slot. The closer a module is to the CPU the higher its interrupt priority. The CC23 Controller should be placed fairly close to the CPU to provide a higher priority than other devices.

Each UNIBUS slot should contain a module. Card slots that would otherwise remain unoccupied should contain Bus Grant modules to provide interrupt acknowledge continuity.

NOTE

The Nonprocessor Grant (NPG) jumper on the SPC card slot in which the controller is being installed MUST BE REMOVED to allow the controller to trap the NPG signal during DMA requests.

4.6.3 NPG SIGNAL JUMPER

The Nonprocessor Grant (NPG) string on the SPC card slot must be opened to allow the trapping of the NPG signal during DMA requests. Therefore, remove the NPG signal jumper between pins CA1 and CB1 on the backplane so that the NPG signal passes through the CC23 Controller.

Figure 4-5 shows a DD11-DK nine-slot backplane, with the enlargement depicting the layout of a typical socket as seen from the rear. (The enlargement is valid for each of the sockets on the backplane.) The figure of the backplane includes letters and numbers that are not actually on the backplane; they are included to help identify pin locations. Also, the numbers shown in the enlargement do not appear in the same location on the backplane; rather, they are located in about the center of the backplane.

Jumper locations are defined by a series of numbers and letters that show pin locations by socket, column and row. To find the NPG signal jumper on the DD11-DK backplane, use the following procedure:

1. Find the appropriate socket (in this case C). The sockets of pins are lettered sequentially, beginning with A at one end, and proceeding to F at the other end.

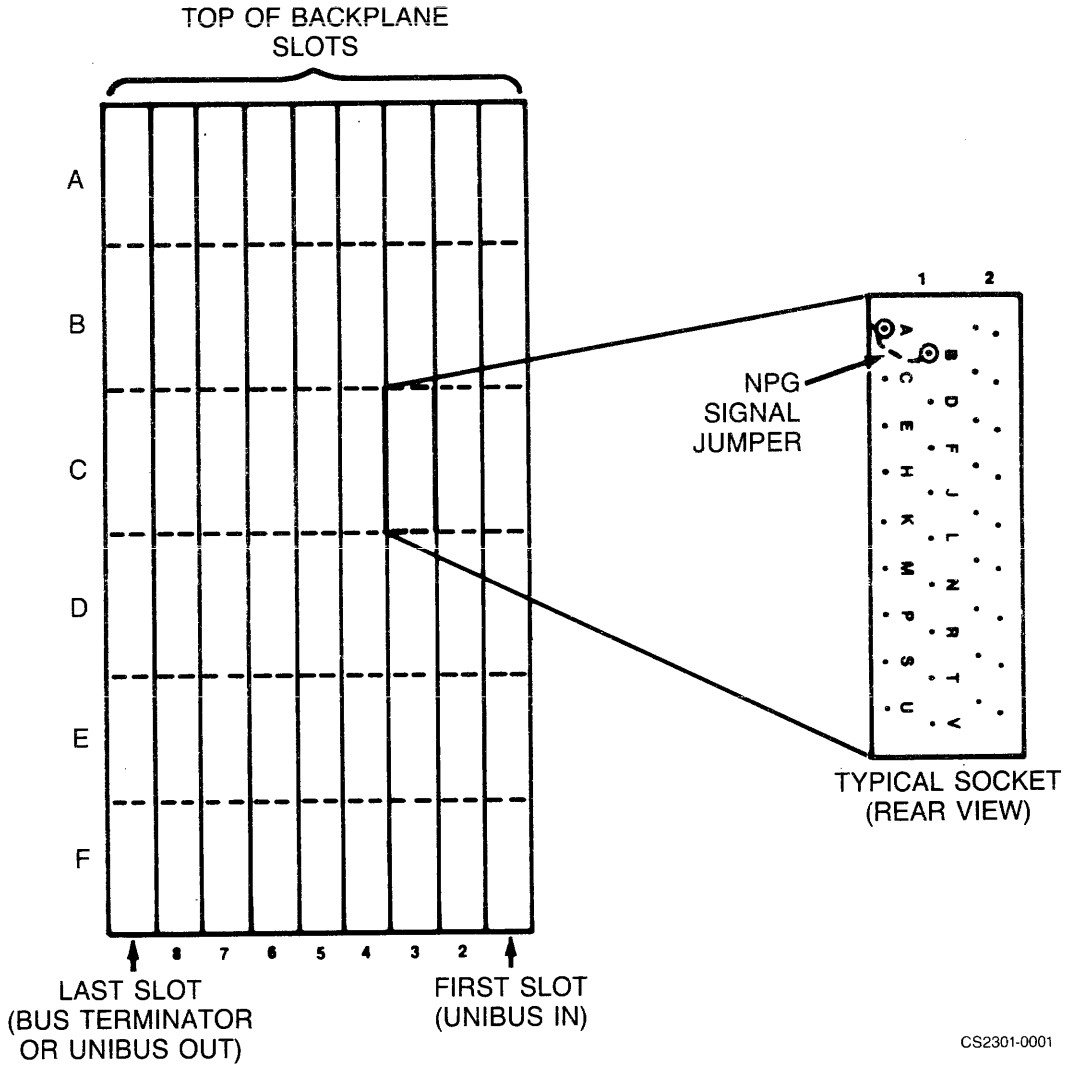


Figure 4-5. NPG Jumper Location

2. Find the appropriate card slot. In Figure 4-5, the card slots are numbered 1 through 9, from right to left. The column of pins shown in the socket enlargement corresponds to card slot 7. Note that each card slot is four pins wide, as the enlargement shows.

3. Find the appropriate row of pins. As the enlargement shows, each pin is labeled A through V, excluding G, I, O and Q. Also, each row of pins is offset from the row on either side.

4. Find the appropriate number corresponding to the desired pin. As the enlargement shows, each number differentiates between two pins on the same row that correspond to the same card slot. A number 1 indicates the left pin of that column in a particular row; a number 2 indicates the right.

In summary: for the seventh card slot, pin CA1 refers to the fourth socket from the top of the backplane (C), the top pin of the left-hand set (A1). CB1 is one pin to the left and slightly up. An arrow shows the wire between the two pins.

The wire-wrap jumper between CA1-CB1 is the bottom-most wrap on the pair. Once located, remove the jumper.

If the CC23 Controller is removed from the backplane, either reconnect the NPG jumper and insert a single-width grant continuity module (DEC part number 5008691) into connector D, or insert a dual-width grant continuity module into connectors C and D, of the slot vacated by the module. The dual-width grant continuity module (DEC part number G7273) jumpers all grant signals (interrupt grants and nonprocessor grants). It can be ordered from Emulex using part number ZU1110812.

4.6.4 CONTROLLER MOUNTING

The controller PCBA should be plugged into the UNIBUS backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the PCBA with the computer power OFF to avoid possible damage to the circuitry. Be sure that the PCBA is properly seated in the throat of the connector before attempting to seat the PCBA by means of the extractor handles.

NOTE

Older UNIBUS systems use a smaller grant card that is difficult to notice when it is plugged into the backplane. **Be sure to look directly into the slot and check to see if one of these smaller grant cards is present.** If there is one present, remove it before plugging in the controller board.

4.7 DISTRIBUTION PANEL INSTALLATION

The CP22, CP23, CP25, and CP26 distribution panels can be mounted directly in DMF32-compatible CPU cabinets, a DEC FCC cabinet, or rack-mounted in a chassis on RETMA rails. Installation instructions for these distribution panels are contained in their respective technical manuals. When you have completed the physical installation of the panel(s), continue using the distribution panel manual and proceed with the cabling.

4.8 SUBSYSTEM CABLING

Use the distribution panel technical manual for instruction on subsystem cabling. When you have completed the cabling procedure return to subsection 4.9 of this manual (Subsystem Power-Up and Verification) to complete the installation.

4.9 SUBSYSTEM POWER-UP AND VERIFICATION

When you have finished configuring and installing your CS23/E1 Communications Subsystem, you need to confirm that it is indeed installed and functioning properly. This subsection is designed to help you to verify proper subsystem operation quickly and efficiently.

When power is applied to the CPU, or when SW1-1 on the edge of the CC23 Controller is turned ON and then OFF again (close/open), the controller automatically executes a built-in self-test. The test is not executed with every Bus INIT, but only on power-up (i.e., DCLO).

As power is applied to the system, watch the LED indicators. All indicators should go to normal operating condition after a few seconds. The normal operating condition of all LEDs is defined in Table 4-9. If any LEDs fail to indicate "normal operating condition" after a few seconds, please see Section 5, Troubleshooting, for a detailed fault isolation procedure.

Table 4-9. CC23 Controller LED Indications

LED	Normal Operating Condition	Indication When Lit
LED 1 (Green - Online)	ON	Indicates the CC23 Controller is in normal operating mode. It is on line to the host computer.
LED 2 (Red - Fault)	OFF	Indicates a fault has been detected during power-up self-test
LED 3 (Yellow - Activity)	FLICKERING or OFF	Indicates controller activity

5.1 OVERVIEW

This section describes the several diagnostic features with which the CC23 is equipped, and outlines fault isolation procedures that use these diagnostic features. This section contains the following subsections:

Subsection	Title
5.1	Overview
5.2	Service
5.3	Test Connector
5.4	Fault Isolation Procedures
5.5	Power-Up Self-Tests
5.6	CC23 Operator Initiated Self-Diagnostics

5.2 SERVICE

The components of your Emulex CS23/E1 Communications Subsystem have been designed to give years of trouble-free service, and they were thoroughly tested before leaving the factory.

Should one of these fault isolation procedures indicate that a component is not working properly, the component must be returned to the factory or one of Emulex's authorized repair centers for service. Emulex products are not designed to be repaired in the field.

Before returning the component to Emulex, whether the product is under warranty or not, you must contact the factory or the factory's representative for instructions and a Return Materials Authorization (RMA) number.

Do not return a component to Emulex without authorization. A component returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii contact:

Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714)662-5600 TWX 910-595-2521

Outside of the United States, contact the distributer from whom the subsystem was initially purchased.

To help you efficiently, Emulex or its representative requires certain information about our product and the environment in which it is installed. During installation a record of the switch settings should have been made on the Configuration Reference Sheets. These sheets are contained in the Installation Section.

After you have contacted Emulex and received an RMA, package the component (preferably using the original packing material) and send the the component **POSTAGE PAID** to the address given you by the Emulex representative. The sender must also insure the package.

5.3 TEST CONNECTOR

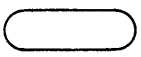
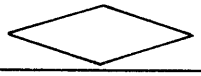
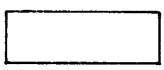
The external loop tests described in subsections 5.6.3 and 5.6.4 require a wrap-around connector. One connector or a full set of 16 can be ordered from Emulex. You can build your own test connector for any of the Emulex distribution panels by strapping a DB25S connector. The type of wrap-around depends the type of interface (RS-232, RS-422, or 20 mA current loop), and the model of distribution panel. Instructions for building wrap-around connectors are contained in the distribution panel technical manuals.

5.4 FAULT ISOLATION PROCEDURES

A fault isolation procedure is provided in flow chart format. The procedure is based on the self-tests incorporated into the subsystem. The procedure is designed to isolate and identify bad lines.

The chart symbols are defined in Table 5-1. The three- and four-digit numbers in the process boxes (for example, 5.6.4) are the numbers of the subsections that describe the test specified as the process.

Table 5-1. Flow Chart Symbol Definitions

Symbol	Description
	Start point, ending point.
	Decision, go ahead according with YES or NO.
	Connector, go to same-numbered symbol on another sheet.
	Process.

CS2301-0106

When the fault isolation procedure indicates a problem, see subsection 5.2 for service instructions.

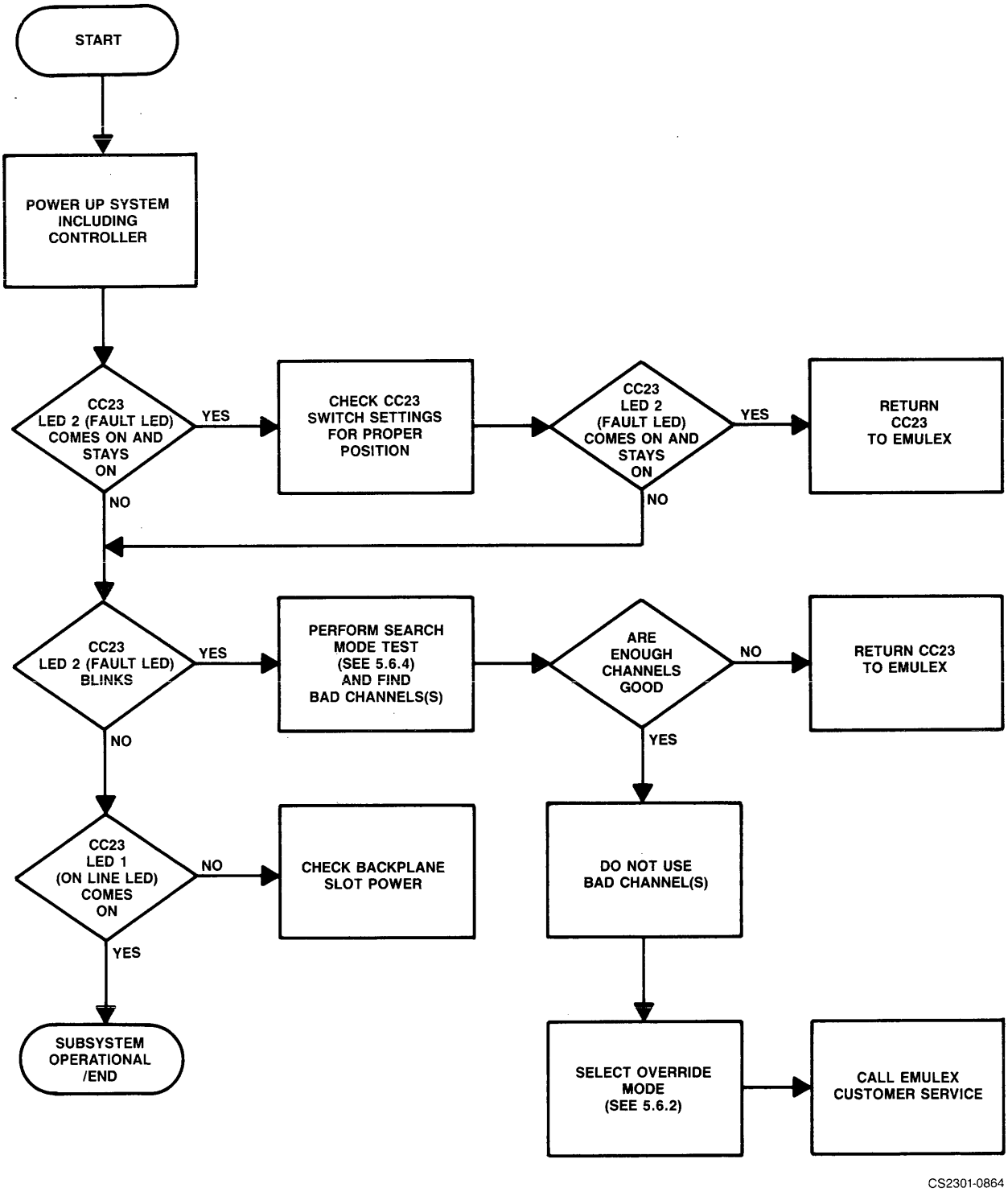


Figure 5-1. Self-Test Failure Fault Isolation Chart

5.4.1 SELF-TEST FAILURE FAULT ISOLATION

The flow chart shown in Figure 5-1 is a representation of the subsystem verification procedure recommended in subsection 4.9 with fault isolation techniques added. The isolation techniques are designed to pinpoint the cause of most self-test failures.

The starting point is the initial power-up of the subsystem which, of course, causes all power-up self-tests to be performed. Each power-up self-test is represented by one or more decision diamonds in the chart. If a self-test fails, the failure branch of the decision diamond indicates additional operator-initiated self-diagnostics that can be performed to isolate the fault.

Aside from a wrap-around connector, no special test equipment is required. Subsystem cables can be checked by substitution or with the aid of a multimeter. All subsystem cables are shown schematically in each distribution panel manual.

5.5 POWER-UP SELF-TESTS

The following subsections describe the self-tests performed on the major components of the subsystem. If any of these components completely fail their self-tests, you do not need to proceed with further tests. Package the units as described in subsection 5.2 and return them to the factory for repair. The major subsystem components are not designed to be serviced in the field.

5.5.1 CC23 CONTROLLER SELF-TEST

This power up self-test is a very thorough check of the CC23's functional integrity. Three functional areas are checked:

1. The on-board PROM and RAM memories
2. The on-board DUARTs (with the exception of the EIA drivers)
3. The microprocessor itself.

NOTE

Switches SW1-2 through SW1-4 must be OFF when the tests described are executed.

When power is applied to the CPU, or when switch SW1-1 on edge of the CC23 Controller PCBA is turned ON and then OFF again (close/open), the controller automatically executes a built-in self-test. The test is not executed with every Bus INIT but only on power-up (i.e., DCLO asserted).

During the self-test LED2 (the Fault LED) on the top edge of the CC23 control module is ON. If the self-test is completed successfully, the on-board microprocessor turns the LED2 OFF. If the LED goes ON when power is applied and stays ON, a complete failure of the self-test is indicated. When LED2 is ON, the CC23 cannot be addressed by the CPU.

5.6 CC23 OPERATOR-INITIATED SELF-DIAGNOSTICS

There are several CC23 self-diagnostics that can be selected by the operator using switches SW1-2 through SW1-4 on the CC23 Controller PCBA. The combinations of switch positions and the test modes that they produce are summarized in Table 5-2, below. The operation of the various test modes is detailed in subsections 5.6.2 through 5.6.5.

Table 5-2. Self-Test Modes

Test Mode	Test Mode Description	--SW1-- 2	3	4
1	Normal Run Mode - LED2 (Fault LED) blinks if any channel fails internal loopback test.	0	0	0
2	Override Mode - LED2 (Fault LED) blinks only if no channels pass internal loopback test. Controller will run with lines that pass.	0	0	1
3	Continuous External Loopback Mode - LED2 (Fault LED) blinks if any error is detected on any channel.	0	1	0
4	Search Mode - LED2 (Fault LED) goes off if at least one channel is good. If no channels are good, the Fault LED blinks.	0	1	1
5	Echo Mode - Characters received from any terminal will be echoed.	1	0	0
0 = OFF (open) 1 = ON (closed)				

5.6.1 NORMAL RUN MODE

The CC23 Controller is placed in this mode for normal operation. In the Normal Run mode, the controller executes its standard self-test on power-up or when SW1-1 is closed and then opened (ON/OFF) (see subsection 5.5).

5.6.2 OVERRIDE MODE

All power-up diagnostic routines are performed in the Override mode, but the CC23 operates if at least one good serial port is detected. All of the serial ports that have passed the Internal Loopback test should function normally.

5.6.3 CONTINUOUS EXTERNAL LOOPBACK MODE

In this mode, the controller executes an External Loopback test continuously. For the controller to pass this test, all ports must be externally looped back. This loopback can be accomplished by placing loopback connectors on every port. If a port fails this test, the LED blinks. The bad port can then be isolated using the Search mode.

5.6.4 SEARCH MODE

In the Search mode, the controller executes a continuous external loopback test. If NO ports pass the test, CC23 LED2 (the Fault LED) blinks. If ONE port passes the test, the CC23 LED2 goes out. This allows a faulty port to be isolated by plugging a loopback connector (see subsection 5.3) in each port, one port at a time. If the CC23 LED2 goes out, that port is good. If it continues to blink, that port is bad.

5.6.5 ECHO MODE

In the echo mode, characters received from any terminal will be echoed back to that terminal. The terminal can be set for any baud rate.

6.1 OVERVIEW

This section contains a detailed description of the device registers that are accessible to the UNIBUS, and that are used to monitor and control the CS23/E1 Communications Subsystem. The registers are functionally compatible with those of the asynchronous portion of a DEC DHU11 communications multiplexer.

This section also includes some general programming notes designed to aid the programmer who writes software to operate the CS23/E1.

The following table outlines the contents of this section.

Subsection	Title
6.1	Overview
6.2	Controller Registers
6.3	Programming Features
6.4	CC23 Controller Architecture

6.2 CONTROLLER REGISTERS

DHU11 registers occupy eight words (16 bytes) of UNIBUS memory-mapped I/O space. However, by indexing, this is expanded internally to 115 words.

The position of the eight words within the I/O page is switch-selected on the CS23/E1. In order to access the module, bits <12:04> of an I/O address must match the address switch coding.

Figure 6-1 depicts all of the DHU11 registers and the offset from the base address is given for each register in hexadecimal and in octal. The suffix "M" (after the base offset) means that there are 16 of these registers, one for each channel. When an "M" register is accessed, the channel is selected by the contents of the Control-and-Status Register <03:00>.

The term "base" means the lowest I/O address on the module, that is to say, when the four low-order address bits equal zero.

Registers are accessed by instructions that use "base + n" as a source or destination. However, before multiple "M" registers are accessed, the channel number must be written to the CSR. The following example explains this.

For example, to read the line-control register of Channel 3, the following PDP-11 instructions are executed:

```
MOVB #CHAN,@#BASE   ;WRITE CHANNEL NUMBER (SEE BELOW) TO CSR
MOV@#BASE+10,R0     ;READ THE LINE-CONTROL REGISTER.
```

In the example:

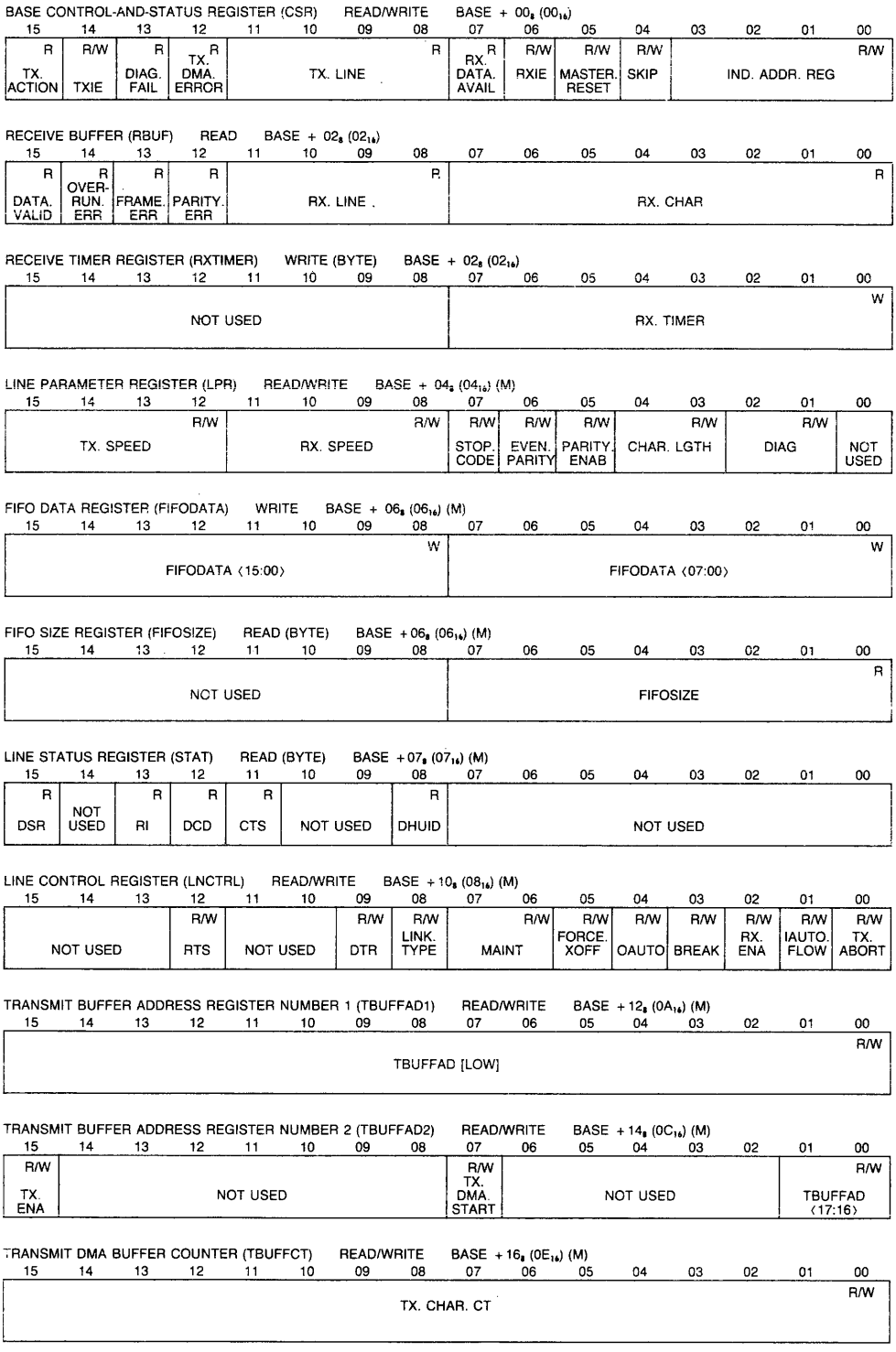
CHAN = $0er0011_2$

Where e = the RXIE bit
and r = the MRST bit (would be 0)
and 0011 = channel number 3

NOTES

Not all register bits are specified. During a write, all unspecified bits must be written as zeros. During a read, unspecified bits are undefined.

The exception to the above rule is that a bit can be written as logical one or zero if it is read as logical one. That is to say, read-modify-write instructions work correctly. Read-modify-write instructions should not be used on the base address or base plus two.



R = READ ONLY
W = WRITE ONLY
R/W = READ/WRITE
(M) = THERE IS ONE OF THESE REGISTERS FOR EACH CHANNEL

CS2301-0992

Figure 6-1. Asynchronous Register Summary

6.2.1 BASE CONTROL-AND-STATUS REGISTER (CSR) Base + 00_8 (00_{16})

15	14	13	12	11	10	09	08
TX. ACTION	TXIE	DIAG. FAIL	TX.DMA ERROR	TX.LINE			

07	06	05	04	03	02	01	00
RX.DATA AVAIL	RXIE	MASTER. RESET	SKIP	IND.ADDR.REG			

Read/Write

Transmit Action (TX.ACTION) CSR<15>

Read-only

Cleared by MASTER.RESET

This bit is set by the CC23 when:

1. The last character of a DMA buffer has been transmitted and the TX FIFO becomes empty.
2. An abort sequence has been completed.
3. A DMA transfer has been terminated by the controller because nonexistent memory has been addressed, or because of a memory parity error.
4. A TX FIFO becomes empty during a TX FIFO output sequence.

This bit is cleared if the host reads the CSR after the TX Action FIFO has become empty. To avoid losing TX Action reports, the host must not let more than 16 reports accumulate. It is advisable to read the CSR until TX.ACTION becomes clear, otherwise, a TX interrupt will not be generated when further reports are loaded.

NOTE

CSR contents should only be changed by a PDP-11 MOV or MOVB instruction, or the VAX equivalent (MOVW or MOVB). Other instructions can lose the state of the TX.ACTION bit (CSR<15>).

Transmit Interrupt Enable (TXIE) CSR<14>

Read/Write

Cleared by BINIT but not by MASTER.RESET

When set, allows the CC23 to interrupt the host when CSR<15> (TX.ACTION) becomes set.

Diagnostic Fail (DIAG.FAIL) CSR<13>

Read-only

When set, DIAG.FAIL indicates that the CC23 internal diagnostics have detected an error. The error may have been detected by the self-test diagnostic or by the BMP. (Background Monitor Program).

This bit is associated with the diagnostic-passed LED. When it is set, the LED will be off. When it is cleared, the LED will be on.

This bit is valid only after MASTER.RESET (CSR<5>) has been cleared. It is cleared after the internal diagnostic programs have been run successfully.

Transmit DMA Error (TX.DMA.ERROR) CSR<12>

Read-only

If set with TX.ACTION also set, means that the channel indicated by CSR<11:08> has failed to transfer DMA data within 21.3 microseconds of the bus request being acknowledged, or that there is a memory parity error.

The TBUFFAD1 and TBUFFAD2 registers will contain the address of the memory location which would not be accessed. TBUFFCT will be cleared.

Transmit Line Number (TX.LINE) CSR<11:08>

Read-only

If TX.ACTION is set, these bits hold the binary number of the channel on which one of the following has just occurred:

1. The TX FIFO has become empty.
2. A DMA transfer has been completed normally.
3. A DMA abort sequence has been completed.

If TX.DMA.ERROR is also set, these bits contain the binary number of channel that has failed during a DMA transfer.

Received Data Available (RX.DATA.AVAIL) CSR<07>

Read-only

When set, indicates that a received character is available. This bit is clear when the RX FIFO is empty. It is used to request an RX interrupt.

Set after MASTER.RESET because the RX FIFO contains diagnostic information.

Receiver Interrupt Enable (RXIE) CSR<06>

Read/Write

Cleared by BINIT but not by MASTER.RESET.

When set, this bit allows the controller to interrupt the host when RX.DATA.AVAIL is set. An interrupt is generated under the following conditions:

1. RXIE is set and a character is placed into the empty RX FIFO.
2. The RX FIFO is not empty and RXIE is changed from zero to one.

The receive interrupt can be delayed by use of the RXTIMER register (See subsection 6.2.3).

Master Reset (MASTER.RESET) CSR<05>

Read/Write

Set by the Host; in order to reset the controller to a known state. Stays set while the controller runs a self-test diagnostic and then performs an initialization sequence. The bit is then cleared to tell the Host that the process is complete.

This bit is set by BINIT (bus initialization signal), or by the Host processor setting CSR<05>.

The Host must not write to any register, or read RBUF, while this bit is set, except during a "skip self-test" operation.

Skip Self-Test (SKIP) CSR<04>

Read/Write

This bit must only be set at the same time as MASTER.RESET (write 60 to CSR). It must be cleared not less than 20 microseconds after it is set.

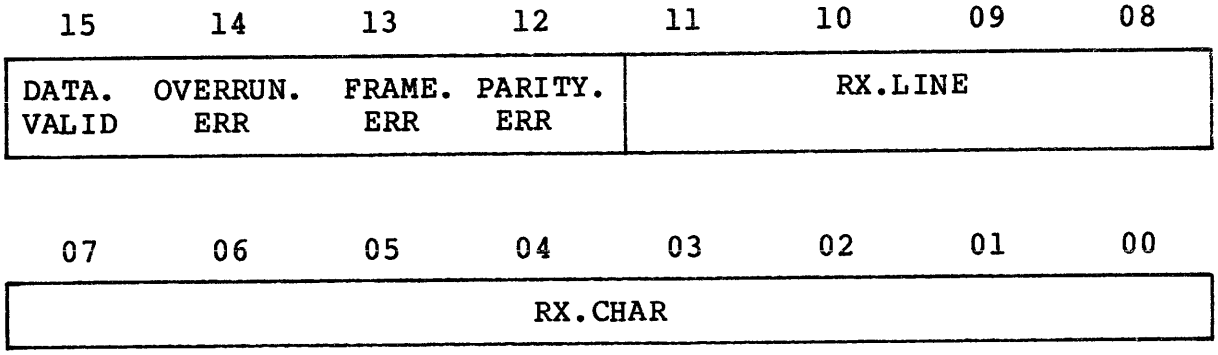
This bit is used to make the controller skip the self-test operation. This will shorten the reset/initialization sequence to about 25 milliseconds.

Indirect Address Register (IND.ADDR.REG) CSR<03:00>

Read/Write

These bits are used to select the channel when accessing a block of indexed "M" registers. They form the binary number of the channel that is to be accessed.

6.2.2 RECEIVE BUFFER (RBUF) Base + 02_8 (00_{16})



Read-only

This is a read-only register at address base + 2_8. Reading the register accesses the oldest word in the 256-word RX FIFO. The least-significant bit (LSB) of the character is in Bit 0.

Data Valid (DATA.VALID) RBUF<15>

Read-only

Cleared by MASTER.RESET or by the FIFO becoming empty.

After self-test, diagnostic information is loaded into the RX FIFO. Therefore, this bit is always set after a successful master-reset sequence.

This bit is set if the FIFO is not empty.

Overrun Error (OVERRUN.ERR) RBUF<14>

Read-only

Set if one or more previous characters of the channel indicated by bits <11:8> were lost because of a full FIFO, or failure to service the DUARTs (also see RX.CHAR).

NOTE

The "all ones" code for bits <14:12> is reserved. This code indicates that modem status or diagnostic information is held in RBUF<07:00>.

Framing Error (FRAME.ERR) RBUF<13>

Read-only

Set if the first stop bit of the received character was not detected (Also see RX.CHAR).

Parity Error (PARITY.ERR) RBUF<12>

Read-Only

Set if this character has a parity error and parity is enabled for the channel indicated by bits <11:08> (also see RX.CHAR).

Receive Line Number (RX.LINE) RBUF<11:08>

Read-only

These bits hold the binary number of the channel on which the character of RBUF<07:00> was received or on which a data-set change was reported.

Received Character (RX.CHAR) RBUF<07:00>

Read-only

If RBUF<14:12> equals 00, these eight bits contain the oldest character in the FIFO. The character is good.

If RBUF<14:12> equals 001, 010, or 011, these eight bits contain the oldest character in the FIFO. The character is bad.

If RBUF<14:12> equals 111, these eight bits contain diagnostic or modem status information in this case, RBUF<00> has the following meanings:

0 = Modem status in RBUF<07:01> (See subsection 6.2.7)
1 = Diagnostic information in RBUF<07:01> (See subsection 6.3.10).

If there is an overrun condition, the DUART data buffer for that channel will be cleared. A null character with RBUF<14> set (4000_8) will be placed in the RX FIFO. The cleared data will be lost.

The controller does not have a read-detect bit. A line break is indicated to the program as a null character with the FRAME.ERR set (2000_8).

6.2.3 RECEIVE TIMER REGISTER (RXTIMER) Base + 02_8 (02_{16})

15	14	13	12	11	10	09	08
0	0	0	0	0	0	0	0

07	06	05	04	03	02	01	00
RX.TIMER							

Write (byte)

The indirect address register (CSR<03:00>) must = 0000 in order to access the receive timer. It can be used by the host to delay the receive interrupt.

Receive Timer (RX.TIMER) RXTIMER<07:00>

Write-only

Set to 1 by MASTER RESET.

The receive interrupt is normally raised when a received character is loaded into the previously empty RX FIFO. The binary number loaded into RX.TIMER modifies this procedure as follows.

0 = Infinite timeout. This timeout will be overridden by the conditions below.

1 = No timeout. The interrupt will be raised immediately.

2 to 255 = Timer delay in milliseconds.

The timer is overridden when the FIFO becomes three-quarters full (critical) or when a modem status change is written to the FIFO.

6.2.4 LINE PARAMETER REGISTER (LPR) Base + 04_8 (04_{16}) (M)

15	14	13	12	11	10	09	08
TX.SPEED				RX.SPEED			

07	06	05	04	03	02	01	00
STOP. CODE	EVEN. PARITY	PARITY. ENAB	CHAR.LGTH		DIAG		0

Read/Write

This register is used to configure its associated channel.

Transmitted Data Rate (TX.SPEED) LPR<15:12>

Read/Write

Set to 1101 by MASTER.RESET. (9600 bits/s).

This bit defines the transmit data rate (See Table 6-1).

Received Data Rate (RX.SPEED) LPR<11:08>

Read/Write

Set to 1101 by MASTER.RESET. (9600 bits/s).

This bit defines the receive data rate (See Table 6-1).

Table 6-1. Data Rates

Code	Data Rate (Bits/s)	Maximum Error(%)	Groups
0000	50	0.01	A
0001	75	0.01	B
0010	110	0.08	A and B
0011	134.5	0.07	A and B
0100	150	0.01	B
0101	300	0.01	A and B
0110	600	0.01	A and B
0111	1200	0.01	A and B
1000	1800	0.01	B
1001	2000	0.19	B
1010	2400	0.01	A and B
1011	4800	0.01	A and B
1100	7200	0.01	A
1101	9600	0.01	A and B
1110	19200	0.01	B
1111	38400	0.01	A

NOTES

Each DHU11 16-channel interface uses eight dual-channel ICs. Channels 0/1, 2/3, 4/5, 6/7, 8/9, 10/11, 12/13, and 14/15 are paired. It is the responsibility of the user to select, transmit and receive data rates of the same group (A or B), for any pair of channels

If channels within the same DUART are configured in different groups, the resulting data rates are undefined.

Stop Code (STOP.CODE) LPR<07>

Read/Write

Cleared by MASTER.RESET

This bit defines the length of the transmitted stop bit.

0 = 1 stop bit for 5-, 6-, 7- or 8-bit characters

1 = 2 stop bits for 6-, 7-, or 8-bit characters
or
1.5 stop bits for 5-bit characters.

Even Parity (EVEN.PARITY) LPR<06>

Read/Write

Cleared by MASTER.RESET.

If LPR<05> is set, this bit defines the type of parity.

1 = Even parity
0 = Odd parity

Parity Enable (PARITY.ENAB) LPR<05>

Read/Write

Cleared by MASTER.RESET.

This bit causes a parity bit to be generated on transmit, and checked and stripped on receive.

1 = Parity Enable
0 = Parity disabled

Character Length (CHAR.LGTH) LPR<04:03>

Read/Write

Set to 11 by MASTER.RESET.

Defines the length of characters. Does not include start, stop, and parity bits.

00 = 5 bits
01 = 6 bits
10 = 7 bits
11 = 8 bits

Diagnostic Code (DIAG) LPR<02:01>

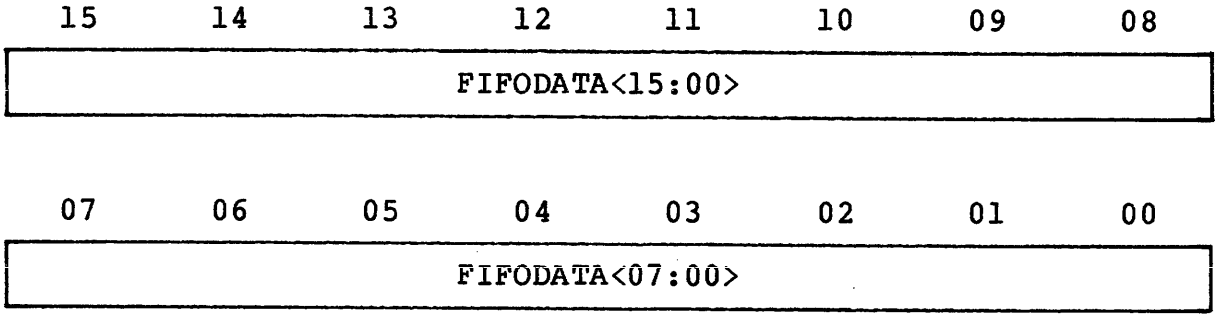
Read/Write

Set to 00 by MASTER.RESET

These bits are diagnostic control codes. They are used by the host as follows:

00 = Normal operation
01 = Causes the background monitor program (BMP) to report the CC23 status via the RX FIFO.BMP reports are covered in subsection 6.3.10.

6.2.5 FIFO DATA REGISTER (FIFODATA) Base + 06_8 (06_{16}) (M)



Write-Only

A write to FIFODATA is interpreted as a write to a TX FIFO. To send a character or characters via a TX FIFO, the host writes the character(s) to the FIFO data register of the appropriate channel. To make sure that there is room in the TX FIFO, the host should first read the associated FIFO size register (See subsection 6.2.6). If single characters are sent, they must be written to the low byte of FIFODATA.

FIFO Data Register FIFODATA<15:00>

Write

Cleared by MASTER.RESET.

These bits contain two characters for transfer via the TX FIFO. After a write-word action to this register, FIFODATA<07:00> and then FIFODATA<15:08> are transferred to the FIFO.

The least-significant bits of the characters are in FIFODATA, bits 00 and 08. Unused bits must be cleared.

FIFO Data Byte Register FIFODATA<07:00>

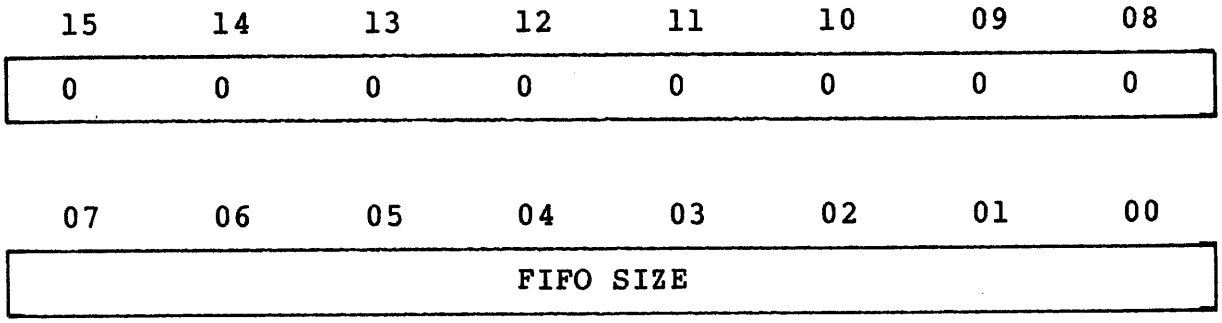
Write Byte

Cleared by MASTER.RESET.

These bits contain a single character for transfer via the TX FIFO. After a write-byte action to this register, FIFODATA<07:00> is transferred to the FIFO.

The least-significant bit of the character is in FIFODATA bit 00. Unused bits must be cleared.

6.2.6 FIFO SIZE REGISTER (FIFOSIZE) Base + 06_8 (06_{16}) (M)



Read Byte

This low-byte register holds a number that indicates the space available in the TX FIFO.

FIFO Size (FIFOSIZE) FIFOSIZE<07:00>

Read Byte

Set to 100_8 by MASTER.RESET.

These bits indicate the available space (in characters) in the TX FIFO. The range is 000_8 (0_{10}) to 100_8 (64_{10}). This register should be read before sending a character, or a sequence of characters, to the FIFO data register.

NOTE

This register can be read (RD WORD) at the same time as the STAT register.

6.2.7 LINE STATUS REGISTER (STAT) Base + 07_8 (07_{16}) (M)

15	14	13	12	11	10	09	08
DSR	0	RI	DCD	CTS	0	0	DHUID

07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0

Read (byte)

This high-byte register holds modem status information.

Data Set Ready (DSR) STAT<15>

Read-only

This bit gives the present status of the Data Set Ready (DSR) signal from the modem.

1 = ON
0 = OFF

NOTE

On a 16 channel distribution panel and on ports 4 through 11 of a 12 channel distribution panel, this bit reflects the state of DTR in the Line Control Register.

Ring Indicator (RI) STAT<13>

Read-only

This bit gives the present status of the Ring Indicator (RI) signal from the modem.

1 = ON
0 = OFF

Data Carrier Detect (DCD) STAT<12>

Read-only

This bit give the present status of the Data Carrier Detect (DCD) signal from the modem.

1 = ON
0 = OFF

Clear to Send (CTS) STAT<11>

Read-only

This bit give the present status of the Clear To Send (CTS) signal from the modem.

1 = ON
0 = OFF

NOTE

On a 16 channel distribution panel and on ports 8 through 11 of a 12 channel distribution panel, this bit reflects the state of DTR in the Line Control Register.

DHU11 Identifier (DHUID) STAT<08>

Read-only

This bit tells the host whether a DHU11 or a DHV11 is installed. This bit is not valid while MASTER.RESET is set.

Always 1 on DHU11 (0 on DHV11).

NOTES

In order to report a change of modem status, the CC23 writes the contents of STAT<15:09> into RBUF<07:01>. RBUF<00> will be clear. RBUF<14:12> equals 111 to tell the host that RBUF<07:00> does not hold a receive character (See subsection 6.3.8, Modem Control).

This register can be read (RD WORD) at the same time as the FIFO size register.

6.2.8 LINE CONTROL REGISTER (LNCTRL) Base + 10_8 (08_{16}) (M)

15	14	13	12	11	10	09	08
0	0	0	RTS	0	0	DTR	LINK. TYPE

07	06	05	04	03	02	01	00
MAINT		FORCE. XOFF	OAUTO	BREAK	RX.ENA	IAUTO. FLOW	TX. ABORT

Read/Write

The main function of this register is to control the line interface.

Request to Send (RTS) LNCTRL<12>

Read/Write

Cleared by MASTER.RESET.

This bit controls the Request To Send (RTS) signal to the modem.

1 = ON
0 = OFF

Data Terminal Ready (DTR) LNCTRL<09>

Read/Write

Cleared by MASTER.RESET

This bit controls the Data Terminal Ready (DTR) signal to the modem.

1 = ON
0 = OFF

Link Type (LINK.TYPE) LNCTRL<08>

Read/Write

Cleared by MASTER.RESET.

This bit must be set if the channel is to be connected to a modem. When the bit is set, any change in modem status will be reported via the RX FIFO as well as the STAT register.

If this bit is reset, this channel becomes a 'data leads only' channel. Modem status information is loaded in the high byte of STAT but is not placed in the FIFO.

Maintenance Mode (MAINT) LNCTRL<07:06>

Read/Write

Cleared to 00 by MASTER.RESET.

These bits can be written by the driver or test programs, in order to test the channel. The coding is as follows:

00 = Normal operation.

01 = Automatic Echo Mode - Received data is retransmitted (regardless of the state of TX.ENA) **at the data rate selected for the receiver.** The received characters are processed normally and placed in the RX FIFO. In this mode, the controller will not transmit any characters (this includes internally generated flow-control characters). The RX.ENA bit must be set when operating in this mode.

10 = Local loopback - The DUART channel output is internally connected to the input. Normal received data is ignored and the transmit data line is held marking. In this mode, flow-control characters will be looped back instead of being transmitted. The data rate selected for the transmitter is used for both transmission and reception. The TX.ENA bit still controls transmission in this mode. RX.ENA is ignored.

11 = Remote loopback - In this mode received data is retransmitted at a clock rate equal to the received clock rate. The data is not placed in the RX FIFO. The state of TX.ENA is ignored but RX.ENA must be set.

Force XOFF (FORCE.XOFF) LNCTRL<05>

Read/Write

Cleared by MASTER.RESET.

This bit can be set by the program to indicate that this channel is congested at the Host system (for example, if the typehead buffer is full). When it sees this bit set, the CC23 will send an XOFF code. Until the bit is reset, XOFFs will be sent after every alternate character received on that channel. When the bit is reset, and XON will be sent unless IAUTO is set and the RX FIFO is critical. See subsection 6.3.6, Auto XON and XOFF.

Outgoing Auto Flow (OAUTO) LNCTRL<04>

Read/Write

Cleared by MASTER.RESET

This bit is the auto-flow control bit for outgoing characters. When OAUTO and RX.ENA are both set, the CC23 will automatically respond to XON and XOFF codes received from a channel. The controller uses the TX.ENA bit in TBUFFAD2 to stop and start the flow. See subsection 6.3.6, Auto XON and XOFF.

Break Control (BREAK) LNCTRL<03>

Read/Write

Cleared by MASTER.RESET.

If set, this bit forces the transmitter of this channel to the spacing state.

Transmission is restarted when the bit is cleared.

NOTE

There is a short delay between writing the bit and the channel changing state. The delay is dependent on the amount of controller activity. Because of the normal length of a BREAK signal, this should not cause problems.

Receiver Enable (RX.ENA) LNCTRL<02>

Read/Write

Cleared by MASTER.RESET.

If this bit is set, this receiver channel is enabled.

If this bit is reset when this DUART channel is assembling a character, that character can be lost.

Incoming Auto Flow (IAUTO.FLOW) LNCTRL<01>

Read/Write

Cleared by MASTER.RESET.

This is the auto-flow control bit for incoming characters. If this bit is set, the CC23 will control incoming characters by transmitting XON and XOFF codes.

If the RX FIFO becomes congested, the CC23 will send an XOFF code to channels with this bit set. An XON will be sent when the congestion is reduced. See subsection 6.3.6, Auto XON and XOFF.

NOTE

An XON code = 21_8 = DC1 = CTRL/Q.
An XOFF code = 23_8 = DC3 = CTRL/S.
No other codes are specified for the interface.

Transmitter Abort (TS.ABORT) LNCTRL<00>

Read/Write

Cleared by MASTER.RESET.

Set by the host to halt the transfer of data.

If a DMA transfer was in progress, the DMA address and count registers (TBUFFAD1, TBUFFAD2, and TBUFFCT) will be updated to reflect the number of characters that have been transmitted. The transfer can be continued by clearing TX.ABORT, and then setting TX.DMA.START in TBUFFAD2. No characters will be lost.

The program must make sure that TX.ABORT is clear before setting TX.DMA.START. Otherwise, the transfer will be aborted before any characters are transmitted.

If a programmed transfer was in progress, characters in the TX FIFO will be discarded. Because of firmware delays, it is possible to transmit a few characters before the abort is actioned. Therefore, the Host cannot determine how many characters have been lost.

When an abort sequence has been completed, the CC23 will set the TX.ACTION bit in the CSR. If the transmitter interrupt is enabled, the program will be interrupted at the transmit vector.

See subsection 6.3.3.1, DMA Transfers, for the use of TX.ABORT.

6.2.9 TRANSMIT BUFFER ADDRESS REGISTER NUMBER 1 (TBUFFAD1)

Base + 12_8 ($0A_{16}$) (M)

15	14	13	12	11	10	09	08
TBUFFAD<15:00>							

07	06	05	04	03	02	01	00
TBUFFAD<15:00>							

Read/Write

Transmit Buffer Address [LOW] (TBUFFAD<15:00>) TBUFFAD1<15:00>

Read/Write

Cleared by MASTER.RESET.

Bits <15:00> of the DMA address (also see subsection 6.2.10).

6.2.10 TRANSMIT BUFFER ADDRESS REGISTER NUMBER 2 (TBUFFAD2)

Base + 14_8 ($0C_{16}$) (M)

15	14	13	12	11	10	09	08
TX.ENA	0	0	0	0	0	0	0

07	06	05	04	03	02	01	00
TX.DMA. START	0	0	0	0	0	TBUFFAD<17:16>	

Read/Write

Transmitter Enable (TX.ENA) TBUFFAD2<15>

Read/Write

Set by MASTER.RESET.

When this bit is set, the controller will transmit all characters.

When this bit is cleared, the controller will only transmit internally generated flow-control characters.

In the OAUTO mode, this bit is used by the CC23 to control outgoing characters. See subsection 6.3.6, Auto XON and XOFF.

Transmit DMA Start (TX.DMA.START) TBUFFAD2<07>

Read/Write

Cleared by MASTER.RESET.

Set by the host to start a DMA transfer. The CC23 will reset the bit before returning TX.ACTION.

NOTE

After setting this bit, the host must **not** write to TBUFFCT, TBUFFAD1, TBUFFAD2 <07:00>, or FIFODATA until the TX.ACTION report has been returned.

Transmit Buffer Address [HIGH] (TBUFFAD<17:16>) TBUFFAD2<01:00>

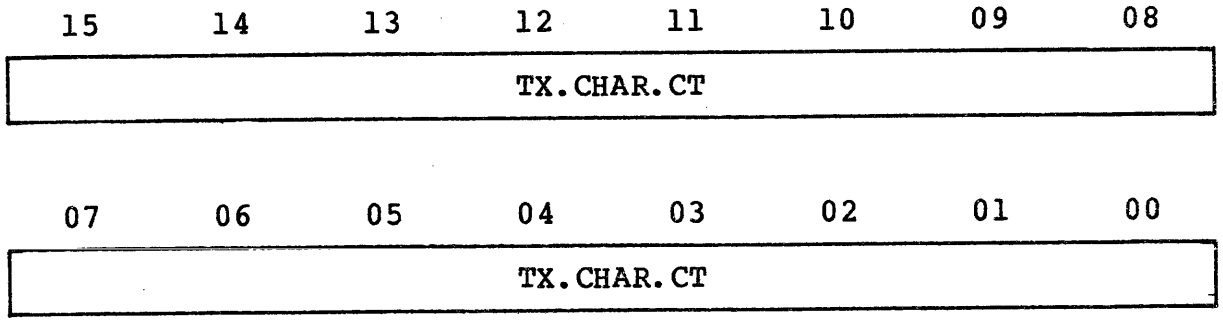
Read/Write

Cleared by MASTER.RESET

Bits <17:16> of the DMA address.

Before a DMA transfer, TBUFFAD1 and the low byte of TBUFFAD2 are loaded with the start address of the DMA buffer. This address is not valid during a DMA transfer. When TX.ACTION is returned, the address will be valid.

6.2.11 TRANSMIT DMA BUFFER COUNTER (TBUFFCT) Base + 16_8 ($0E_{16}$) (M)



Read/Write

Transmit Character Count (TX.CHAR.CT) TBUFFCT<15:00>

Read/Write

Cleared by MASTER.RESET.

Loaded with the number of characters to be transferred by DMA.

The number of characters is specified as a 16-bit unsigned integer.

After a DMA transfer has been aborted this location will hold the number of characters still to be transferred.

See also the previous note (subsection 6.2.10, TX.DMA.START).

6.3 PROGRAMMING FEATURES

6.3.1 INITIALIZATION

The CC23 Controller is initialized by its on-board firmware.

Initialization takes place after a bus-reset sequence, or when the host sets CSR<05> (MASTER.RESET).

Before starting initialization, the on-board diagnostics run a self-test program. These results of this test are reported by eight diagnostic bytes in the RX FIFO.

NOTE

This self-test diagnostic can be skipped on command from the program. This is covered in subsection 6.3.10.3.

The CC23 state, after a successful self-test, is as follows:

1. Eight diagnostic codes are placed in the RX FIFO.
2. The diagnostic fail bit (CSR<13>) is reset.
3. All channels set for:
   a. Send and receive 9600 bits/s
   b. Eight data bits
   c. One stop bit
   d. No parity
   e. parity odd
   f. Auto-flow off
   g. RX disabled
   h. TX enabled
   i. No break on line
   j. No loopback
   k. No modem control
   l. DTR and RTS off
   m. DMA character count zero
   n. DMA start address zero
   o. TX.DMA.START cleared
   p. TX.DMA.ABORT cleared
   q. FIFO SIZE set to 100_8

The CC23 Controller clears the MASTER.RESET bit (CSR<05>) when initialization and self-test are complete.

6.3.2 CONFIGURATION

After CC23 Controller self-initialization, the driver program can configure the module as needed. This is done via the LPR and LNCTRL registers.

By writing to the associated LPR and LNCTRL, the program can select data rate, character length, parity, and number of stop bits for each channel. Individual receivers and transmitters can be enabled and auto-flow selected.

For operation with any device that uses modem control signals, LINK.TYPE of the associated LNCTRL register should be set.

6.3.3 TRANSMITTING

Data can be transferred to the serial interface by two methods. Blocks of characters can be transferred under DMA control, or the Host can write one or two characters at a time to the FIFO data register. Such transfers are covered in the following subsections.

6.3.3.1 DMA Transfers

Before setting up the transfer of a DMA buffer, the program should make sure that TX.DMA.START is not set. TBUFFCT, TBUFFAD1, and FIFODATA should not be written unless TX.DMA.START is clear.

Transmission will start when the program sets TX.DMA.START.

The size of the DMA buffer, and its start address, can be written to TBUFFCT, TBUFFAD1, and TBUFFAD2 in any order. However, TBUFFAD2 contains TX.ENA and TX.DMA.START, so it is simpler to write TBUFFAD2 last. By using byte operations on this register, TX.ENA and TX.DMA.START can be separated.

The CC23 will perform the transfer, and set TX.ACTION when it is complete. If TXIE is set, the program will be interrupted at the transmit vector. Otherwise, TX.ACTION must be polled to detect the end of the DMA operation.

To abort a DMA transfer, the program must set TX.ABORT. The controller will stop transmission, and update TBUFFCT, TBUFFAD1, and TBUFFAD2<07:00> to reflect the number of characters that have been transmitted. TX.DMA.START will be cleared. If the interrupt is enabled, TX.ACTION will interrupt the program at the transmit vector. If the program clears TX.ABORT and sets TX.DMA.START, the transfer can be resumed without loss of characters.

If a DMA transfer fails because of a memory error, the transmission will be terminated. TBUFFAD1 and TBUFFAD2 will point to the failing location. TBUFFCT will be cleared, and TX.DMA.ERROR and TX.ACTION will be set. If TXIE is set, the TX interrupt will be raised.

6.3.3.2 Programmed Transfers

Before writing a character or a sequence of characters to the FIFO data register (FIFODATA), the program should read the FIFO size register (FIFOSIZE) to check that there is space in the TX FIFO.

If there is space for characters, they can be written as bytes (one character) or words (two characters) to FIFODATA. After a low-byte write, FIFODATA<07:00> will be transferred to the FIFO. After a word write, FIFODATA<07:00> and then FIFODATA<15:08> will be transferred to the FIFO. High-byte writes to FIFODATA are not allowed.

The CC23 returns TX.ACTION when the TX FIFO becomes empty. As with DMA transfers, this bit can be sensed via interrupt or by polling the CSR.

In programmed-transfer FIFO mode, TX.ACTION is returned when the CC23 transfers the last character from the RX FIFO to the DUART, not when it has been transmitted. Each channel has a two-character buffer. Thus, if modem status bits or line parameters are changed immediately after the last TX.ACTION of a message, the end of the message could

be lost. The program can avoid loss by adding two null characters to the end of each programmed-transfer FIFO message.

To abort a programmed transfer, the program must set TX.ABORT. The CC23 will terminate the transfer and then set TX.ACTION. If TXIE is set, the TX interrupt will be raised. Characters in the TX FIFO will be discarded, but because of firmware delays the Host cannot determine how many characters have been lost.

6.3.4 RECEIVING

Received characters, tagged with the channel number and DATA.VALID, are placed in the RX FIFO buffer (RBUF). If a character is put in an empty RBUF, the CC23 sets RX.DATA.AVAIL. It remains set while there is valid data in there. If RXIE is set, the program will be interrupted at the receive vector. The program's interrupt routine should read RBUF until DATA.VALID is reset.

NOTE

Subject to the RX timer, a receive interrupt is generated when RX.DATA.AVAIL and RXIE both become set. If the interrupt routine does not empty the FIFO, RXIE must be toggled to raise another interrupt.

If RXIE is not set, the program must poll RBUF often enough to prevent data loss.

6.3.5 INTERRUPT CONTROL

An interrupt priority level of 5 or 6 is selected by switches on the module. During an interrupt sequence, the CC23 Controller will provide one of two vectors.

1. A "base" vector set on the interrupt vector switches, or
2. A "base + 4" vector

Subject to the value in RXTIMER (subsection 6.2.3), the base vector is supplied whenever data is put into an empty RX FIFO.

The "base + 4" vector is supplied when:

1. A TX FIFO has become empty. This may be because all characters have been transmitted, or because the program has aborted the transfer.
2. A complete DMA block has been transferred, or
3. A DMA transfer has been aborted, or terminated due to a memory error.

At the two vectors, the host must provide the addresses of suitable routines to deal with the above conditions.

6.3.6 AUTO XON AND XOFF

XON and XOFF codes are commonly used to control data flow on communications channels. To use this facility, interfaces must have suitable decoding hardware or software.

A channel that receives an XOFF stops sending characters until it receives an XON. A channel that is becoming overrun by received data sends an XOFF. It sends an XON when the congestion is relieved.

If the CC23 is programmed for automatic flow control (auto-flow), it can automatically regulate the flow of characters. Three bits of the Line Control Register (see subsection 6.2.8) control this function:

1. IAUTO - LNCTRL<01>
2. FORCE.XOFF - LNCTRL<05>
3. OAUTO - LNCTRL<04>

IAUTO and FORCE.XOFF both control incoming characters. IAUTO is an enable bit that allows the state of the RX FIFO counters to control the generation of XOFF and XON codes. The FORCE.XOFF bit is a direct command from the program.

1. The CC23 hardware recognizes when the FIFO is three-quarters full and half full. The firmware uses these states for auto flow control.

   If the program sets a channel's IAUTO bit, the CC23 will send the channel an XOFF if it receives a character after the FIFO becomes three-quarters full. If the channel does not respond to XOFF, the CC23 will send an XOFF in reply to every alternate character received. An XON will be sent when the FIFO becomes less than half full, unless FORCE.XOFF for that channel is set. XONs are only sent to channels to which an XOFF has been sent.

   By inserting XON and XOFF characters into the data stream, the program can perform flow control directly. However, if the CC23 is in the IAUTO or FORCE.XOFF mode, the results will be unpredictable.

   These internally generated XONs and XOFFs will be transmitted even if TX.ENA is cleared.

2. When FORCE.XOFF is set, the CC23 sends an XOFF and then acts as if IAUTO is set and the FIFO is critical (was three-quarters full, not yet less than half full). When FORCE.XOFF is reset, and XON will be sent unless the FIFO is critical and IAUTO is set (See 1, IAUTO).

NOTE

If both FORCE.XOFF and IAUTO become clear after XOFF has been sent, an XON will be sent immediately.

3. If the program sets OAUTO, the CC23 will automatically respond to XON and XOFF characters from the channel. It does this by setting and clearing the TX.ENA bit.

   The program can also control the TX.ENA bit. In this case it is important to keep track of received XON and XOFF characters.

   Received XON and XOFF characters will always be reported via the FIFO. It is possible during read/modify/write operations by the program, for the CC23 to change the TX.ENA bit between the read and the write action. For this reason, if DMA transfers are started while OAUTO is set, it is advisable to write to the low byte of TBUFFAD2 only.

NOTES

The CC23 can change the state of TX.ENA for up to 20 microseconds after OAUTO is cleared by the program.

When checking for flow-control characters, the CC23 only checks characters that do not contain transmission errors. The parity bit is stripped and the remaining bits are checked for XON (21_8) and XOFF (23_8) codes.

6.3.7 ERROR INDICATION

The program is informed of transmission and reception errors by means of four bits.

1. TX.DMA.ERR - CSR<12>. See subsection 6.2.1
2. PARITY.ERR - RBUF<12>. See subsection 6.2.2
3. FRAME.ERR - RBUF<13>. See subsection 6.2.2
4. OVERRUN.ERR - RBUF<14>. See subsection 6.2.2

RBUF<14:12> are also used to identify a diagnostic or modem status code.

6.3.8 MODEM CONTROL

This subsection discusses the use of modem signals. The ability to use some modem signals is dependant on the distribution panel. See your distribution panel manual for a list of signals supported by that panel.

Each channel of the module provides modem control bits for RTS and DTR. Modem status inputs CTS, DSR, RI, and DCD are also provided on each channel. These bits can be used for modem control or as general-purpose outputs and inputs (see subsection 6.2.7, STAT Register).

CTS, DSR and DCD are sampled every 10 ms. Therefore, to make sure that a change is detected, these bits must stay steady for at least 10 ms after a change. RI is also sampled every 10 ms, but a change is not reported unless the new state is held for three consecutive samples. There are no hardware controls between the modem control logic and the receiver and transmitter logic. Any coordination should be done under program control. Modem-status-change reports are placed in the RX FIFO at the correct position relative to the received characters.

NOTES

On a 16 channel distribution panel and on ports 8 through 11 of a 12 channel distribution panel, CTS reflects the state of DTR in the Line Control Register.

On a 16 channel distribution panel and on ports 4 through 11 of a 12 channel distribution panel, DSR reflects the state of DTR in the Line Control Register.

By setting LINK.TYPE(LNCTRL<08>), a channel can be selected for modem operation. Any change of the modem status inputs will be reported to the program via the RX FIFO. Modem control bits must be driven by the program's communication routines. Control bits are written to the LNCTRL register.

By clearing LINK.TYPE the channel is selected as a "data line only" channel. Modem control and status bits can still be managed by the program, but status bits must be polled at the line status register. Changes of modem status will not be reported to the program.

NOTE

When transmitting by the programmed transfer method, up to two characters can be buffered in CC23 hardware. If modem control bits are to be changed at the end of a transmission, two null characters should be added. When TX.ACTION is set after the second null character, the last genuine character has left the DUART.

Status change reporting is done via the RX FIFO as follows:

- When OVERRUN.ERR, FRAME.ERR, and PARITY.ERR are all set, the eight low-order bits contain either status change or diagnostic information. In this case:
- If RBUF<00> =, RBUF<07:01> hold STAT<15:09> (see subsection 6.2.7).
- If RBUF<00> =, RBUF<07:01> hold diagnostic information (see subsection 6.3.10).

6.3.9 MAINTENANCE PROGRAMMING

As well as using on-board and external diagnostic programs,the LNCTRL register allows each channel to be configured in normal, automatic-echo, local-loopback, and remote-loopback modes (see subsection 6.2.8, LNCTRL).

6.3.10 DIAGNOSTIC CODES

6.3.10.1 Self-Test Diagnostic Codes

After bus reset or master reset, the CC23 Controller executes an initialization sequence. At the end of the sequence, eight diagnostic codes are put in the RX FIFO. RX.DATA.AVAIL is set and MASTER.RESET is cleared.

After an error-free test, DIAG.FAIL will be reset. The "diagnostic passed" LED will be on. If an error is detected, DIAG.FAIL will be set and the LED will be off.

6.3.10.2 Interpretation of Self-Test Codes

All self-test codes in RBUF will have the top four bits set. Bits<11:08> indicate the sequence of the diagnostic byte. That is to say, 0 equals first byte, 1 equals second byte, and so on.

Figure 6-2 shows how the diagnostic code in the low byte of RBUF should be interpreted. Table 6-2 gives the meaning of each implemented diagnostic byte.

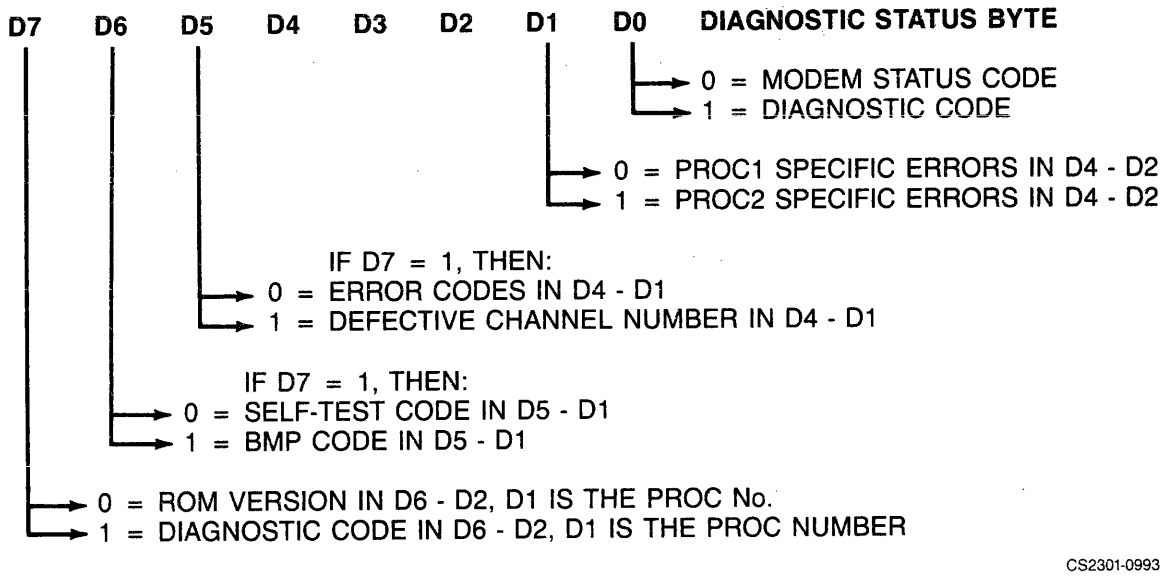


Figure 6-2. Diagnostic Code Interpretation

Table 6-2. CC23 Self Test Error Codes

Code (Octal)	Test
201	Self-Test null code (used as a filler)
203	Self-Test skipped
213	Undefined DUART error
215	Transmit-character-FIFO logic error
217	Received-character-FIFO logic error
231	Microprocessor internal RAM error
235	Microprocessor ROM CRC error

The odd numbers from 241_8 to 277_8 indicate a DUART access or function error on the channel indicated by D4 to D1.

If D7 = 0, the ROM version number is in D6 to D2.

D1 = PROC number (0 = PROC1, 1 = PROC2).

NOTE

Codes not shown in this table indicate undefined errors.

After self-test, the eight codes in the RX FIFO will consist of six diagnostic codes and two ROM version codes.

After an error-free test, six 201 codes and two ROM version codes will be returned.

If self-test is skipped (see next section), six 203 codes and two ROM version codes will be returned.

6.3.10.3 Skipping Self-Test

Self-test takes up to 2.5 seconds to complete. Depending on system software, this can cause a 2.5 second hand-up. The "skip self-test" facility allows the program to bypass the self-test diagnostic.

There are two methods of skipping self-test.

- DHV11 compatible method
- DHU11 (direct) method

The DHV11 compatible method is as follows:

1. The program resets the controller.
2. The diagnostic firmware writes 125252_8 throughout the common RAM within eight milliseconds of reset.
3. The program waits 10 ms (+or-1ms) after issuing reset. It then writes 052525_8 throughout the control register (LPR, LNCRTL, TBUFFAD1, TBUFFAD2, and TBUFFCT) for lines 0 to 7, within the next 4 ms.
4. The diagnostic firmware waits until 16 ms after reset. It then checks for a 052525_8 code in common RAM.

   It finds the code, self-test is skipped. The DIAG.FAIL bit is cleared and control is passed to the communications firmware that begins initialization.

   If the code is not found, self-test begins.

NOTE

The program must not write to the CSR or the control registers during the period starting 15 ms after reset and ending when the MASTER.RESET bit is cleared. This could cause a diagnostic fail condition.

The direct method is to set SKIP (CSR<04>) and MASTER.RESET (CSR<05>) at the same time. That is to say, write 60_8 to the base CSR. SKIP must not be cleared until at least 20 microseconds after it is set. SKIP must be cleared by the Host to enable the communications firmware to complete the master reset sequence.

6.3.10.4 Backround Monitor Program (BMP)

Normally, no BMP reports will occur. However, if the host suspects that the controller is dead, it can obtain a BMP report at any time. This is done by setting DIAG (LPR<02:01>) of any channel to 01. One of two codes is loaded into the RX FIFO:

- 305_8 - CC23 running
- 307_8 - CC23 defective

A single diagnostic word is returned via the FIFO. The low byte contains the diagnostic code. In the high byte OVERRUN.ERR, FRAME.ERR, and PARITY.ERR are all set to indicate that bits <07:00> do not hold a normal character. The line number returned is that of the LPR used to request the report.

On completion of the check, the BMP will clear the 01 code in DIAG. The host should not write to the LPR of that channel until DIAG has been cleared.

6.4 CC23 CONTROLLER ARCHITECTURE

The CC23 Controller is organized around an eight-bit high-speed bipolar microprocessor that performs all controller functions. The ALU and register file portion of the microprocessor are implemented with two 2901 bit-slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with six 2K X 8-bit PROMs.

A 4K x 8-bit high-speed random access memory (RAM) holds the contents of device registers, silo buffer and working storage for the microprocessor. The RAM is both a source and destination to the internal data bus and is addressed directly and indirectly by the microprocessor.

The UNIBUS interface consists of a 16-bit bidirectional set of data lines and an 18-bit set of address lines. The UNIBUS interface is used for programmed I/O, CPU interrupts and NPR data transfers. The microprocessor responds to all programmed I/O, and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all NPR read operations and transfers data between the UNIBUS data lines and the distribution panels.

The CC23 Controller Module is connected to each distribution panel by two 50-conductor cables.

6.4.1 RECEIVER OPERATION

Reception on each channel is by means of Dual Universal Asynchronous Receiver/Transmitters (DUARTs). These MOS/LSI devices perform all the functions of quadruple-buffered asynchronous character assembly. The receiver section of the DUART samples the channel at 16 times the bit rate of the signals to be received on the channel. Upon detection of a mark-to-space transition, the DUART counts eight clock pulses and checks the state of the channel again. This sampling occurs in the center of the normal start bit. If the sample is a mark, the receiver returns to its idling state, ready to detect another mark-to-space transition. If the sample is a space, the receiver enters the data entry condition and samples the state of the channel at subsequent sample points spaced at multiples of 16 clock pulses from the center of the start bit. The number of samples taken is determined by the character length information and parity enable programmed in the device registers. If parity checking is enabled for the channel, the receiver computes the parity of the character received and compares it with the parity sense specified for reception on that channel. If the parity does not check, the parity error bit is set.

The character length, parity, and number of stop bits that are used by the DUART to perform the above operations are stored in each DUART from information received from the device register controlling the line parameters for the associated channel in the DUART.

6.4.2 TRANSMITTER OPERATION

Transmission on each channel is also performed by DUARTs. These MOS/LSI devices perform all the necessary functions for double buffered asynchronous character transmission. The transmitter section of the DUART holds the serial output at a marking state when idle. When a character has been loaded into the transmitter-holding buffer, the DUART generates a start bit within 1/16 of the bit time. The start space is followed by five, six, seven, or eight data bits and the parity bit if parity is selected. Control of the DUART is performed by the device register controlling the line parameters. Data bits are presented to the channel with the least significant bit first.

If the transmitter's holding register has been loaded while a character is being transmitted, the the start bit of the second character is transmitted immediately at the end of the preceding character's stop bits.

7.1 OVERVIEW

This section describes the interfaces that the CS23/E1 Communication Subsystem incorporates. This section is divided into the following subsections:

Subsection	Title
7.1	Overview
7.2	UNIBUS
7.3	CC23 Controller to Distribution Panel
7.4	EIA

7.2 UNIBUS

The controller interfaces to the VAX UNIBUS via a Small Peripheral Controller (SPC) connector. The UNIBUS consists of 18 address channels and 16 bi-directional data channels, plus control signals for data and interrupt vector address transfer and for becoming bus master. The signal connections of the controller to the UNIBUS are shown in Table 7-1.

Table 7-1. SPC UNIBUS Connections

Column	C		D		E		F	
Pin	1	2	1	2	1	2	1	2
A	NPG IN	+5V		+5V		+5V		+5V
B	NPG OUT					-15V		-15V
C	PA	GND		GND	A12	GND		GND
D		D15		BR7	A17	A15	BBSY	
E		D14		BR6	MSYN	A16		
F		D13		BR5	A02	C1		
H	D11	D12		BR4	A01	A00		
J		D10			SSYN	C0	NPR	
K		D09		BG7 IN	A14	A13		
L		D08	INIT	BG7 OUT	A11			
M		D07		BG6 IN			INTR	
N	DCLO	D04		BG6 OUT	A08			
P		D05		BG5 IN	A10	A07		
R		D01		BG5 OUT	A09			
S	PB	D00		BG4 IN				
T	GND	D03	GND	BG4 OUT	GND		GND	SACK
U		D02			A06	A04		
V	ACLO	D06			A05	A03		

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7.3 CC23 CONTROLLER TO DISTRIBUTION PANEL

The CC23 Controller interfaces with the distribution panels via two 50-wire cables that connect to J1 and J2, or J3 and J4 on the edge of the CC23. The pinning assignments for this interface are shown in Table 7-2.

NOTE

When using Table 7-2 it is important to remember that connectors J1 and J3 on the CC23 correspond to the first DHU11 emulation, and connectors J2 and J4 correspond to the second DHU11 emulation.

7.4 EIA

The distribution panels interface with external devices such as terminals, printers, and modems. This interface is the EIA interface. The EIA interface differs from distribution panel to distribution panel. See the manual for the distribution panel for a table of the pin/signal assignments supported by that panel.

Table 7-2. CC23 Controller to Distribution Panel Interface

CONNECTIONS FOR 16 CHANNEL DISTRIBUTION PANEL

CC23 Connector J1 or J3				CC23 Connector J2 or J4			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	DTR 00	2	DCD 00	1	DTR 08	2	DCD 08
3	DTR 01	4	DCD 01	3	DTR 09	4	DCD 09
5	DTR 02	6	DCD 02	5	DTR 10	6	DCD 10
7	DTR 03	8	DCD 03	7	DTR 11	8	DCD 11
9	DTR 04	10	DCD 04	9	DTR 12	10	DCD 12
11	DTR 05	12	DCD 05	11	DTR 13	12	DCD 13
13	DTR 06	14	DCD 06	13	DTR 14	14	DCD 14
15	DTR 07	16	DCD 07	15	DTR 15	16	DCD 15
17	0V	18	0V	17	MUST BE GROUND	18	0V
19	TDX 00	20	RI 00	19	TDX 08	20	RI 08
21	RXD 00	22	0V	21	RXD 08	22	0V
23	TXD 01	24	RI 01	23	TXD 09	24	RI 09
25	RXD 01	26	0V	25	RXD 09	26	0V
27	TXD 02	28	RI 02	27	TXD 10	28	RI 10
29	RXD 02	30	0V	29	RXD 10	30	0V
31	TXD 03	32	RI 03	31	TXD 11	32	RI 11
33	RXD 03	34	0V	33	RXD 11	34	0V
35	TXD 04	36	RI 04	35	TXD 12	36	RI 12
37	RXD 04	38	0V (−15V)	37	RXD 12	38	0V (−15V)
39	TXD 05	40	RI 05	39	TXD 13	40	RI 13
41	RXD 05	42	0V (+5V)	41	RXD 13	42	0V (+5V)
43	TXD 06	44	RI 06	43	TXD 14	44	RI 14
45	RXD 06	46	0V (+5V)	45	RXD 14	46	0V (+5V)
47	TXD 07	48	RI 07	47	TXD 15	48	RI 15
49	RXD 07	50	0V	49	RXD 15	50	0V

CONNECTIONS FOR 12 CHANNEL DISTRIBUTION PANEL

CC23 Connector J1 or J3				CC23 Connector J2 or J4			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	DTR 00	2	DCD 00	1	DTR 08	2	DCD 08
3	DTR 01	4	DCD 01	3	DTR 09	4	DCD 09
5	DTR 02	6	DCD 02	5	DTR 10	6	DCD 10
7	DTR 03	8	DCD 03	7	DTR 11	8	DCD 11
9	DTR 04	10	DCD 04	9	RTS 00	10	CTS 00
11	DTR 05	12	DCD 05	11	RTS 01	12	CTS 01
13	DTR 06	14	DCD 06	13	RTS 02	14	CTS 02
15	DTR 07	16	DCD 07	15	RTS 03	16	CTS 03
17	0V	18	0V	17	MUST BE OPEN	18	0V
19	TDX 00	20	RI 00	19	TDX 08	20	RI 08
21	RXD 00	22	0V	21	RXD 08	22	0V
23	TXD 01	24	RI 01	23	TXD 09	24	RI 09
25	RXD 01	26	0V	25	RXD 09	26	0V
27	TXD 02	28	RI 02	27	TXD 10	28	RI 10
29	RXD 02	30	0V	29	RXD 10	30	0V
31	TXD 03	32	RI 03	31	TXD 11	32	RI 11
33	RXD 03	34	0V	33	RXD 11	34	0V
35	TXD 04	36	RI 04	35	RTS 04	36	DSR 00
37	RXD 04	38	0V (−15V)	37	CTS 04	38	0V (−15V)
39	TXD 05	40	RI 05	39	RTS 05	40	DSR 01
41	RXD 05	42	0V (+5V)	41	CTS 05	42	0V (+5V)
43	TXD 06	44	RI 06	43	RTS 06	44	DSR 02
45	RXD 06	46	0V (+5V)	45	CTS 06	46	0V (+5V)
47	TXD 07	48	RI 07	47	RTS 07	48	DSR 03
49	RXD 07	50	0V	49	CTS 07	50	0V

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Appendix A
AUTOCONFIGURE ALGORITHM

A.1 OVERVIEW

The following discussion presents the algorithm for assignment of floating addresses and vectors for VAX-VMS.

This appendix is divided into the following subsections:

Section	Title
A.1	Determining the CSR Address for Use With Autoconfigure
A.2	Determining the Vector Address for Use With Autoconfigure
A.3	A System Configuration Example

A.2 DETERMINING THE CSR ADDRESS FOR USE WITH AUTOCONFIGURE

The term Autoconfigure refers to a software utility that is run when the computer is bootstrapped. This utility finds and identifies I/O devices in the I/O page of system memory.

Some devices (like the DM11) have fixed addresses reserved for them. Autoconfigure detects their presence by simply testing their standard address for a response. Specifically, the control/status register (CSR) address, which is usually the first register of the block, is tested.

Addresses for those devices not assigned fixed numbers are selected from the floating CSR address space (760010_8 - 763776_8) of the UNIBUS input/output (I/O) page. This means that the presence or absence of floating devices will affect the assignment of addresses to other floating-address devices. Similarly, many devices have floating interrupt vector addresses. According to the DEC standard, vectors must be assigned in a specific sequence and the presence of one type of device will affect the correct assignment of vectors for other devices.

The CSR address for a floating-address device is selected according to the algorithm used during autoconfigure. The algorithm is used in conjunction with a SYSGEN Device Table, Table A-1.

Essentially, Autoconfigure checks each valid CSR address in the floating CSR address space for the presence of a device. Autoconfigure expects any devices installed in that space to be in the order specified by the SYSGEN Device Table. Also, the utility expects an eight-byte block to be reserved for each device that is not installed in the system. Each empty block tells Autoconfigure to look at the next valid address for the next device on the list.

Determining the CSR Address For Use With Autoconfigure

When a device is detected, a block of addresses is reserved for the device according to the number of registers it employs. The utility then looks at the next CSR for that device type. If there is a device there, it is assumed to be of the same type as the one before it and a block is reserved for that device. If there is no response at the next address, that space is reserved to indicate that there are no more devices of that type. Then the utility checks the CSR address (at the appropriate boundary) for the next device in the table.

Table A-1. SYSGEN Device Table

Rank	Device	Number of Registers	Octal Modulus	Rank	Device	Number of Registers	Octal Modulus
1	DJ11	4	10	17	Reserved	4	10
2	DH11	8	20	18	RX11[2]	4	10
3	DQ11	4	10	18	RX211[2]	4	10
4	DU11,DUV11	4	10	18	RXV11[2]	4	10
5	DUP11	4	10	18	RXV21[2]	4	10
6	LK11A	4	10	19	DR11-W	4	10
7	DMC11	4	10	20	DR11-B[3]	4	10
7	DMR11	4	10	21	DMP11	4	10
8	DZ11[1]	4	10	22	DPV11	4	10
8	DZV11	4	10	23	ISB11	4	10
8	DZS11	4	10	24	DMV11	8	20
8	DZ32	4	10	25	DEUNA[2]	4	10
9	KMC11	4	10	26	UDA50[2]	2	4
10	LPP11	4	10	27	DMF32	16	40
11	VMV21	4	10	28	KMS11	6	20
12	VMV31	8	20	29	VS100	8	20
13	DWR70	4	10	30	TU81	2	4
14	RL11[2]	4	10	31	KMV11	8	20
14	RLV11[2]	4	10	**32**	**DHV11,DHU11**	**8**	**20**
15	LPA11-K[2]	8	20	33	DMZ32	16	40
16	KW11-C	4	10	34	CP132	16	40

[1] DZ11-E and DZ11-F are treated as two DZ11s.

[2] The first device of this type has a fixed address. Any extra devices have a floating address.

[3] The first two devices of this type have a fixed address. Any extra devices have a floating address.

In summary, there are four rules that pertain to the assignment of device addresses in floating address space:

1. Devices with floating addresses must be attached in the order in which they are listed in the SYSGEN Device Table, Table A-1. That is, a device higher on the list will always have a higher bus address.

2. The CSR address for a given device type is assigned on word boundaries according to the number of UNIBUS-accessible registers that the device has. The boundaries are shown in the Octal Modulus column of Table A-1. The following table relates the number of device registers to possible word boundaries.

Device Registers	Possible Boundaries
1	Any Word
2	XXXXX0, XXXXX4
3,4	XXXXX0
5,6,7,8	XXXX00,XXXX20,XXXX40,XXXX60
9 through 16	XXXX00,XXXX40

   The Autoconfigure utility inspects for a given device type only at one of the possible boundaries for that device. That is, the utility does not look for a DMF32 (16 registers) at an address that ends in 20_8.

3. A gap must follow the register block of any installed device to indicate that there are no more of that type of device. This gap must start on the proper CSR address boundary for that type of device.

4. An eight-byte gap must be reserved in floating address space for each device type that is not installed in the current system. The gap must start on the proper word boundary for the type of device the gap represents. That is, a single DJ11 installed at 760010_8 would be followed by a gap starting at 760020_8 to show a change of device types. A gap to show that there are none of the next device on the list, a DH11, would begin at 760040_8, the next legal boundary for a DH11-type device.

An example of calculating bus and vector addresses is contained in subsection A.4.

A.3 DETERMINING THE VECTOR ADDRESS FOR USE WITH AUTOCONFIGURE

There is a floating vector address convention that is used for communications and other devices that interface with the UNIBUS. These vector addresses are assigned in order starting at 300_8 and proceeding upwards to 777_8. Table A-2 shows the assignment sequence. For a given system configuration, the device with the highest

floating vector rank would be assigned to vector address 300_8. Additional devices of the same type would be assigned subsequent vector addresses according to the number of vectors required per device, and according to the starting boundary assigned to that device type.

Vector addresses are assigned on the boundaries indicated in the modulus column of Table A-2. That is, if the modulus is 10_8, then the first vector address for that device must end with zero (XX0). If the modulus is 4_8, then the first vector address can end with zero or 4 (XX0, XX4).

Vector addresses always fall on modulo 4_8 boundaries (XX0, XX4). That is, a vector address never ends in any number but four or zero. Consequently, if a device has two vectors and the first must start on a modulo 10_8 boundary, then, using 350_8 as a starting point, the vectors will be 350_8 and 354_8.

Table A-2. Priority Ranking for Floating Vector Addresses (starting at 300_8 and proceeding upwards

Rank	Device	Number of Vectors	Octal Modulus
1	DC11	2	10
1	TU58	2	10
2	KL11[1]	2	10
2	DL11-A[1]	2	10
2	DL11-B[1]	2	10
2	DLV11-J[1]	8	40
2	DLV11,DLV11-F[1]	2	10
3	DP11	2	10
4	DM11-A	2	10
5	DN11	1	4
6	DM11-BB/BA	1	4
7	DH11 modem control	1	4
8	DR11-A, DRV11-B	2	10
9	DR11-C, DRV11	2	10
10	PA611 (reader+punch)	4	20
11	LPD11	2	10
12	DT07	2	10
13	DX11	2	10
14	DL11-C to DLV11-F	2	10
15	DJ11	2	10
16	DH11	2	10
17	VT40	4	20
17	VSV11	4	10
18	LPS11	6	40
19	DQ11	2	10
20	KW11-W, KWV11	2	10
21	DU11, DUV11	2	10
22	DUP11	2	10
23	DV11 + modem control	3	20
24	LK11-A	2	10
25	DWUN	2	10
26	DMC11	2	10
26	DMR11	2	10
27	DZ11/DZS11/DZV11	2	10
27	DZ32	2	10
28	KMC11	2	10
29	LPP11	2	10

continued on next page

Table A-2. Priority Ranking for Floating Vectors Addresses (starting at 300_8 and proceeding upwards) (continued)

Rank	Device	Number of Vectors	Octal Modulus
30	VMV21	2	10
31	VMV31	2	10
32	VTV01	2	10
33	DWR70	2	10
34	RL11/RLV11[2]	1	4
35	TS11[2], TU80[2]	1	4
36	LPA11-K	2	10
37	IP11/IP300[2]	1	4
38	KW11-C	2	10
39	RX11[2]	1	4
39	RX211[2]	1	4
39	RXV11[2]	1	4
39	RXV21[2]	1	4
40	DR11-W	1	4
41	DR11-B[2]	1	4
42	DMP11	2	10
43	DPV11	2	10
44	ML11[3]	1	4
45	ISB11	2	10
46	DMV11	2	10
47	DEUNA[2]	1	4
48	UDA50[2]	1	4
49	DMF32	8	40
50	KMS11	3	20
51	PCL11-B	2	10
52	VS100	1	4
53	Reserved	1	4
54	KMV11	2	10
55	Reserved	2	10
56	IEX	2	10
57	DHV11	2	10
57	**DHU11**	**2**	**10**
58	DMZ32	6	20
59	CP132	6	20

[1] A KL11 or DL11 used as a console, has a fixed vector.

[2] The first device of this type has a fixed vector. Any extra devices have a floating vector.

[3] ML11 is a Massbus device which can connect to a UNIBUS via a bus adapter.

A.4 A SYSTEM CONFIGURATION EXAMPLE

Below is an example of a system configuration that includes the following devices:

- 2 DV11s
- 1 DMC11
- 2 DZ11s
- 1 KMC11
- 2 RL11s
- 1 DR11-W
- 2 DHU11s

Table A-3 shows how the CSR addresses were calculated. Note that the DV11 has a fixed bus addresses, so no floating bus address was assigned to it. Table A-4 shows how the vector addresses were assigned when two emulations are enabled.

Table A-3. SYSGEN Floating CSR Address Assignment Example

Installed	Device		Octal Address
	DJ11	Gap	760010
	DH11	Gap	760020
	DQ11	Gap	760030
	DU11	Gap	760040
	DUP11	Gap	760050
---->	DV11		775000[1]
---->	DV11		775040
	LK11A	Gap	760060
---->	DMC11		760070
		Gap	760100
---->	DZ11		760110
---->	DZ11		760120
		Gap	760130
---->	KMC11		760140
		Gap	760150
	LPP11	Gap	760160
	VMV21	Gap	760170
	VMV31	Gap	760200
	DWR70	Gap	760210
---->	RL11		760220
		Gap	760230
	LPA11-K	Gap	760240
	KW11-C	Gap	760250
	Reserved	Gap	760260
	RX11	Gap	760270
---->	DR11-W		760300
		Gap	760310
	DR11-B	Gap	760320
	DMP11	Gap	760330
	DPV11	Gap	760340
	ISB11	Gap	760350
	DMV11	Gap	760360
	DEUNA	Gap	760370
	UDA50	Gap	760400
	DMF32	Gap	760440
	KMS11	Gap	760460
	VS100	Gap	760500
	TU81	Gap	760510
	KMV11	Gap	760520
---->	DHU11		760540
---->	DHU11		760560
		Gap	760600
	DMZ32	Gap	760640
	CP132	Gap	760700

[1]Fixed address

Table A-4. Interrupt Vector Floating Address Assignment Example

Number of Devices Installed	Devices	Octal Vector Address
2	DV11	300
		320
		340
		360
		400
		420
1	DMC11	430
		440
2	DZ11	450
		460
		470
		500
1	KMC11	510
		520
2	RL11	524
		530
1	DR11-W	534
2	DHU11 (CS23/E1)	540
		544
		550
		554

Appendix B
PROM REMOVAL AND REPLACEMENT

B.1 OVERVIEW

It may be necessary, either for maintenance reasons or because you wish to change your Emulex controller from one emulation to another, to remove and replace the CS23/E1's firmware PROM set.

B.1.1 EXCHANGING EMULATION PROMS

The six existing emulation PROMs are located in sockets labeled PROM 0 through PROM 5. Pry the existing PROMs from their sockets using an IC puller or an equivalent tool.

The CS23/E1 PROM set is identified by the part numbers on top of the PROMs (E53-E58). Place the new PROMs in numerical order beginning with the socket labeled PROM 0 (see Table B-1). Make certain that the PROMs are firmly seated and that no pins are bent or misaligned. (If the two rows of PROM pins are too far apart to fit in the socket, grasp the PROM at its ends using your thumb and forefinger and bend one of the pin rows inward by pressing it against a table top or other flat surface.

Table B-1. Emulation PROM Locations

PROM Number	Socket	PCBA Location
E53	PROM 0	U156
E54	PROM 1	U155
E55	PROM 2	U154
E56	PROM 3	U153
E57	PROM 4	U152
E58	PROM 5	U151

B.1.2 ADDRESS RANGE DECODE PROM

In order to access UNIBUS device addresses not listed in Table 4-4, an optional address range decode PROM must be installed on the CC23 Controller. The address decode PROM that is shipped in the controller at location U162 must be replaced with the optional PROM to access the optional set of addresses.

The optional address range decode PROM is available by special order from Emulex.

Appendix C
PDP-11 DIAGNOSTICS

C.1 OVERVIEW

This appendix describes the DEC DHU11 PDP-11 diagnostics. It includes procedures and commands for running the DHU11 diagnostic programs with the Diagnostic Runtime Services (DRS) supervisor.

The instructions in the appendix explain how to run the diagnostics with the DRS supervisor. The DRS supervisor provides the interface between the operator and the diagnostic programs, allowing the operator to modify the execution of the diagnostic programs.

The PDP-11 diagnostic programs are combined to form a Functional Verification Test (FVT) which, when run, tests various controller functions. The diagnostic programs that make up the FVT are ZDHU??, ZDHV??, ZDHW??, AND ZDHX??. The symbol ? at the end of the diagnostic program names indicates the revision level of the diagnostic, and the patch level of the diagnostic.

NOTE

Before running the DEC PDP-11 Diagnostics, check the settings of switches SW6-1 through SW6-7. All of these switches must be OFF (open) for the diagnostics to run without unpredictable errors.

The minimum system requirements to use the DHU11 diagnostic programs are:

- UNIBUS CPU
- 32K bytes of memory
- Console terminal
- XXDP+ load device with Diagnostic Runtime Services supervisor
- CS23/E1 Communications Subsystem

In order to test the full DMA address capability of the controller, the FVT uses the following address patterns. If the high address lines are to be tested, the host must have memory at the following locations as well as the 32K bytes defined above:

Address Bits	17	16	15	14	13	-	-
Memory Address (High bank)	1	0	1	X	X	X	X
Memory Address (Low bank)	0	1	0	X	X	X	X

If memory is not available at these locations some high DMA address bits will not be tested. This will not be considered as an error. The operator, by answering a prompt, can display information specifying the bits that were tested.

C.2 TEST CONNECTORS

Diagnostics ZDHV, ZDHW, and ZDHX require wrap-around connectors and staggered loopback connectors.

The schematic for the DHUll wrap-around connector is shown in Figure C-1. This connector is identical to the DEC H325 connector.

The schematic for the loopback connector is shown in Figure C-2. Placement of the connector is shown in Figure C-3.

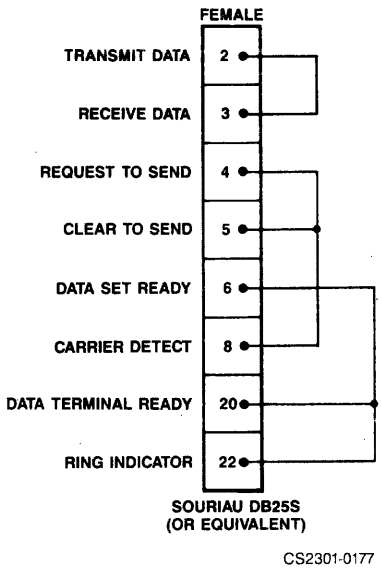

Figure C-1. DHUll Wrap-Around Connector

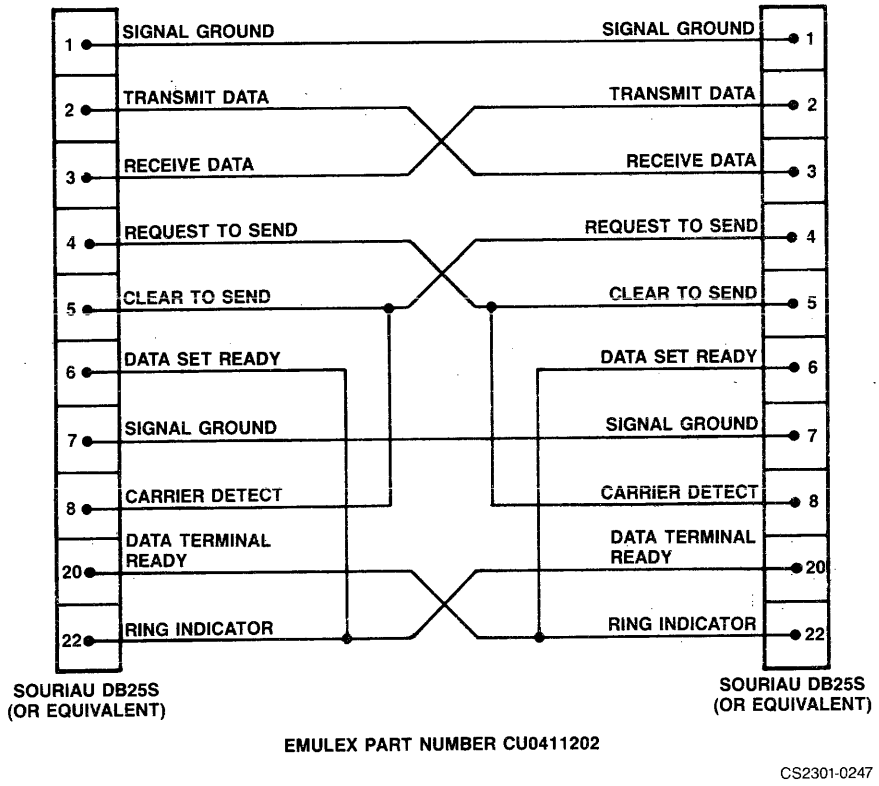

Figure C-2. DHUll Staggered Loopback Connector Schematic

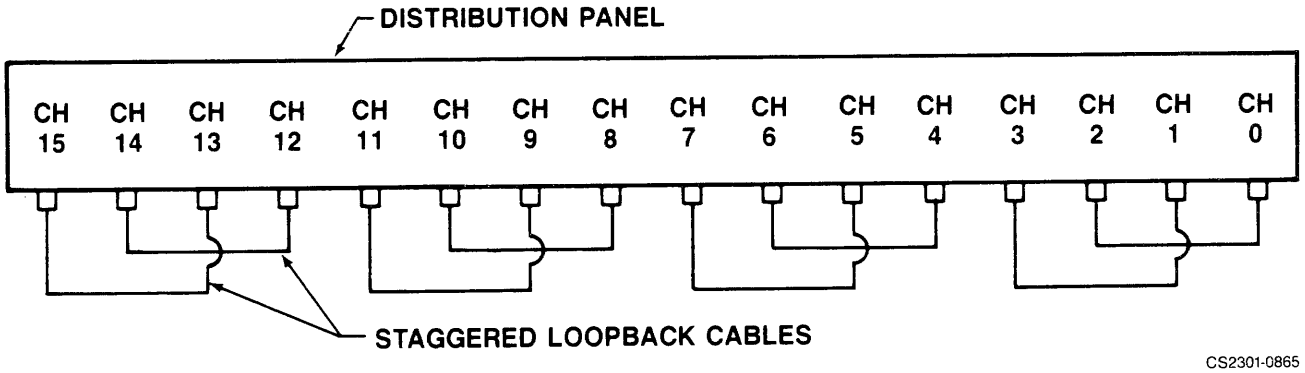

Figure C-3. DHUll Staggered Loopback Connector Placement

C.3 DIAGNOSTIC TEST FUNCTIONS

In addition to the functions described below, each diagnostic test verifies that the handshake between the controller and the host is operating correctly.

C.3.1 ZDHU

This program checks the reset and register access functions, and checks reports from the self-test. This diagnostic test does not require the use of loopback connectors.

C.3.2 ZDHV

This program checks the operation of the receive interrupt timer. It also checks the register bits that control the flow of data and the operation of the FIFOs. Some of these diagnostic tests require the use of a loopback connector.

C.3.3 ZDHW

This program verifies correct operation of the modem control and status lines, and checks that that there is no unwanted interaction between them. One of the external loopback modes must be selected for this test to run.

NOTE

Because not all channels on the distribution panels have all modem signals available, some ZDHW tests will not pass. The tests that will **not** pass are:

Test 3 - Staggered Mode; channels 8-11 on 12 channel panel, all channels on 16 channel panel.

Test 3 - Loopback Mode; channels 8-11 on 12 channel panel, all channels on 16 channel panel.

Test 4 - Staggered Mode; channels 4-7 and 8-11 on 12 channel panel, all channels on 16 channel panel.

Test 6 - Staggered Mode; channels 8-11 on 12 channel panel and all channels on 16 channel panel.

Test 6 - Loopback Mode; channels 8-11 on 12 channel panel and all channels on 16 channel panel.

Test 7 - Staggered Mode; channels 8-11 on 12 channel panel and all channels on 16 channel panel.

Test 7 - Loopback Mode; channels 8-11 on 12 channel panel and all channels on 16 channel panel.

Test 8 - Staggered Mode; channels 4-7 and 8-11 on 12 channel panel and all channels on 16 channel panel.

Test 8 - Loopback Mode; channels 8-11 on 12 channel panel and all channels on 16 channel panel.

C.3.4 ZDHX

This program checks DMA transfers and addressing, split-speed operation, and the reporting of data errors. Modem loopback and keyboard echo tests can be selected. When using the modem-loopback mode the modem must be set up manually. The diagnostic will test up to the point where the line is looped back. One of the external loopback modes must be selected for this test to run.

NOTE

Several tests of ZDHXA0 will fail if the extended monitor (XXDPXM) of the XXDP V2 diagnostic monitor is used. This is due to a bug in the DEC diagnostic. (The DEC DHU11 also fails under the same diagnostic.) Either these tests should not be run or your system should be reconfigured to load the small monitor (XXDPSM).

C.4 DECX/11 EXERECISER (XDHU)

The DECX/11 Exerciser, XDHU must be run any time a DHU11-type emulation (such as the CS23/E1) is installed. Instructions for loading and running the DECX/11 Exerciser are contained in the DECX/11 User's Manual (DEC part number AC-F035B-MC) and in DECX/11 Cross-Reference (DEC part number AC-F055C-MC).

The Exerciser should not be run until all phases of the FVT have been passed.

C.5 STARTING THE DIAGNOSTIC PROGRAM

Use the DRS Supervisor to start the diagnostic program. The start procedure has four steps. The start command is issued, hardware parameter questions are answered, software parameter questions are answered, and the diagnostic is executed. These steps are presented in greater detail below.

1. At the prompt DR> type:

   STA/PASS:1/FLAGS:HOE<CR>

   The switches and flags are optional

2. The program prompts with:

   CHANGE HW?

   You must answer Y to this prompt to change the hardware parameter tables.

NOTE

Some versions of the diagnostic supervisor do not ask if you would like to alter the hardware parameter tables. Instead, they begin with the hardware parameter question sequence.

The answers to the questions are used to build hardware parameter tables in memory. A series of questions is presented for each device to be tested, and a table is built for each device.

3. When all of the hardware parameter tables have been built, the program presents the prompt for the software parameter tables. This prompt is as follows:

   CHANG SW?

   If parameters other than the default parameters are desired, type Y. If you wish to use the default parameters, type N.

   If you type Y, a series of questions will be asked which prompt you to enter desired software parameters. These parameters will be entered in the software parameter table in memory. Unlike the hardware questions, the software questions will be asked only once, regardless of the number of units being tested.

4. After the software parameter tables have been built, the diagnostic begins to run.

   The program printouts and actions on error detection are determined by the switch options selected with the start command.

C.6 LOADING PROCEDURES

There are several different methods for loading the DHU11 diagnostics under the control of the XXDP+ diagnostic monitor. The following procedure is common to many DEC systems and similar to others.

1. Mount the appropriate medium (Dectape, disk, etc.) containing the XXDP+ monitor and the Functional Verification Test.

2. Boot the system to load the monitor.

3. Once loaded, the XXDP+ monitor prints an introductory message and displays a period (.) to indicate that it is ready to accept commands.

4. To display a list of the diagnostic programs contained on the tape (or disk), type DIR at a period prompt.

5. The diagnostic can now be loaded. There are two different ways to load the diagnostic. The two methods are described below. The diagnostic ZDHUA0 (where the A0 at the end of the name indicates the revision level and the patch level of the diagnostic) is used as an example in both of the methods.

   a. To load the diagnostic ZDHUA0, type:

      ```
      L ZDHUA0
      ```

      The DRS supervisor can now be started. At the prompt, type:

      ```
      S 200
      ```

   or

   b. To load the diagnostic and start the DRS supervisor, type:

      ```
      R ZDHUA0
      ```

6. The diagnostic and the DRS supervisor will be loaded. The following message is then displayed:

   ```
   DRS LOADED
   DIAG. RUN-TIME SERVICES REV. D APR-79
   ZDHUA0
   DHU-11 FUNC TST PART1
   UNIT IS DHU-11
   DR>
   ```

DR> is the prompt for the DRS supervisor routine. At this point a DRS supervisor command (such as START) must be entered. The DRS supervisor commands are listed in subsection C.7.

C.7 DRS SUPERVISOR COMMANDS

The following DRS supervisor commands can be issued in response to the DR> prompt:

COMMAND	FUNCTION
START	Starts a diagnostic program
RESTART	When a diagnostic has stopped and control is returned to the supervisor, this command restarts the program from the beginning
CONTINUE	Allows a diagnostic to continue running from the point where it was stopping point
PROCEED	Causes the diagnostic to resume with the next test after the one it halted in
EXIT	Transfers control to the XXDP+ monitor
DROP	Drops units specified until an ADD or START command is given
ADD	Adds specified units. These units must have been previously dropped
PRINT	Prints out statistics if available
FLAGS	Used to change flags
ZFLAGS	Clears flags

All of the DRS supervisor commands except EXIT, PRINT, FLAGS and ZFLAGS can be used with switch options.

C.7.1 COMMAND SWITCHES

Switch options can be used with most DRS supervisor commands. The commands and their functions and some examples are listed below.

COMMAND	FUNCTION
/TESTS:	Used to specify the tests to be run (the default is all tests). An example of the tests switch used with the start command to run tests 1 to 10, 20 and 30 to 35 would be: DR> START/TESTS:1-10:20:30-35<CR>
/PASS:	Used to specify the number of passes for the diagnostic to run. An example of the tests switch used with the start command to make two passes would be: DR> START/PASS:2
/EOP:	Used to specify how many passes of the diagnostic will occur before the end of pass message is printed (the default is one). An example of the tests switch used with the start command to prompt the program to report the end of a pass after every third pass would be: DR> START/EOP:3
/UNITS:	Used to specify the units to be run. This switch is valid only if N was entered in response to the CHANGE HW? question.

/FLAGS: Used to check for conditions and modify program execution accordingly. It is possible to enable multiple flags at the same time. An example of the format to do this is as follows:

```
DR> START/FLAGS:HOE:PNT
```

The conditions checked for are as follows:

:HOE	Halt on error (transfers control back to the supervisor)
:LOE	Loop on error
:IER	Inhibit error reports
:IBE	Inhibit basic error information
:IXE	Inhibit extended error information
:PRI	Print errors on line printer
:PNT	Print the number of the test being executed before execution
:BOE	Ring bell on error
:UAM	Run in unattended mode, bypass manual intervention tests
:ISR	Inhibit statistical reports
:IOU	Inhibit dropping of units by program

C.7.2 CONTROL/ESCAPE CHARACTERS SUPPORTED

The keyboard functions supported by the DRS supervisor are as follows:

COMMAND	FUNCTION
CTRL C	Returns control to the supervisor. The DR> prompt would be typed in response to CTRL C. This command can be typed at any time.
CTRL Z	Used during hardware or software dialogue to terminate the dialogue and select default values.
CTRL O	Disables all printouts. This is valid only during a printout.
CTRL S	Used during a printout to temporarily freeze the printout.
CTRL Q	Resumes a printout after a CTRL S.

Appendix D
VAX-11 DIAGNOSTICS

D.1 OVERVIEW

The following VAX diagnostics can be run for the CS23/E1:

- EVDAI - Standalone VAX diagnostic (Runs with some errors. See subsection D.3)
- EVDAH - Online VAX diagnostic
- UETP - User Environmental Test Program

EVDAI is a group of functional verification tests that can be used as installation tests, for troubleshooting, and as a confidence check.

EVDAH is an online diagnostic that provides a confidence check of the CS23/E1. Channels that have not been allocated to a process can be checked while the system is running application programs.

UETP is an exerciser package that checks to make sure there is no unwanted interaction between options connected to the system.

NOTE

Before running the DEC VAX-11 Diagnostics, check the settings of switches SW6-1 through SW6-7. All of these switches must be OFF (open) for the diagnostics to run without unpredictable errors.

D.2 TEST CONNECTORS

The VAX diagnostics require wrap-around connectors and staggered loopback connectors.

The schematic for the DHU11 wrap-around connector is shown in Figure D-1. This connector is identical to the DEC H325 connector.

The schematic for the loopback connector is shown in Figure D-2. Placement of the connector is shown in Figure D-3.

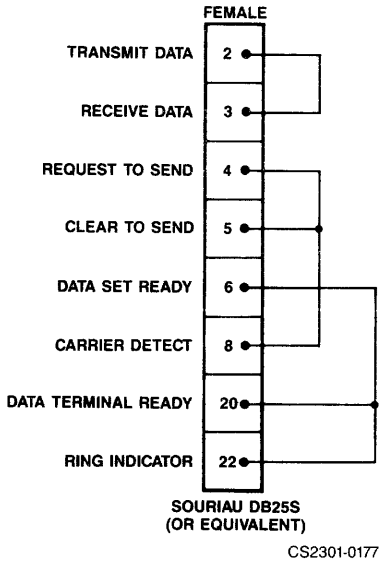

Figure D-1. DHU11 Wrap-Around Connector

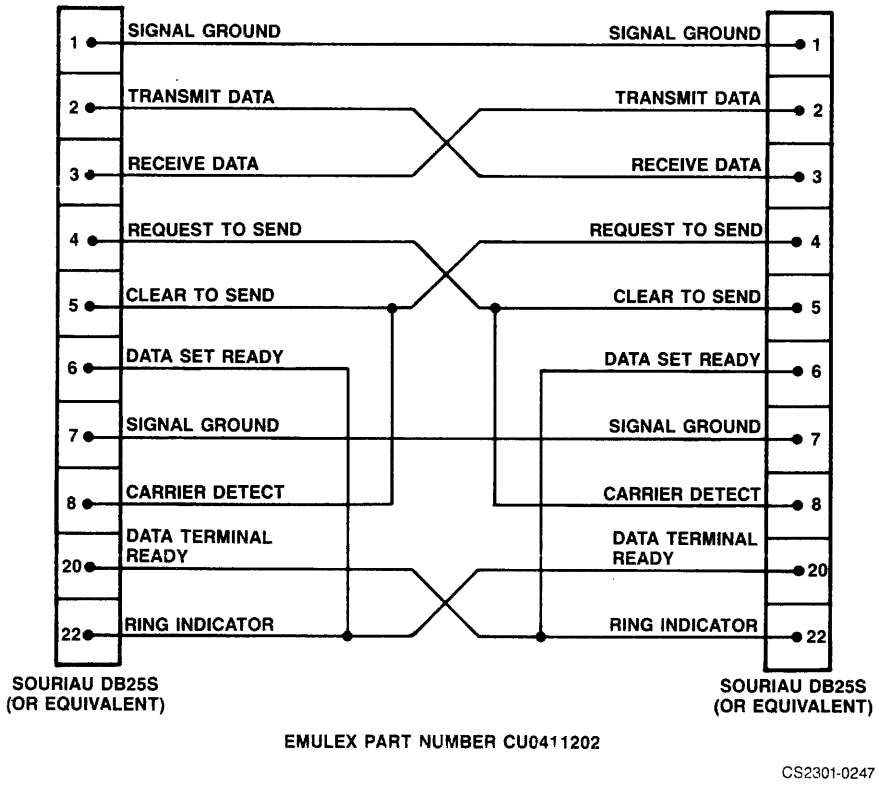

Figure D-2. DHU11 Staggered Loopback Connector Schematic

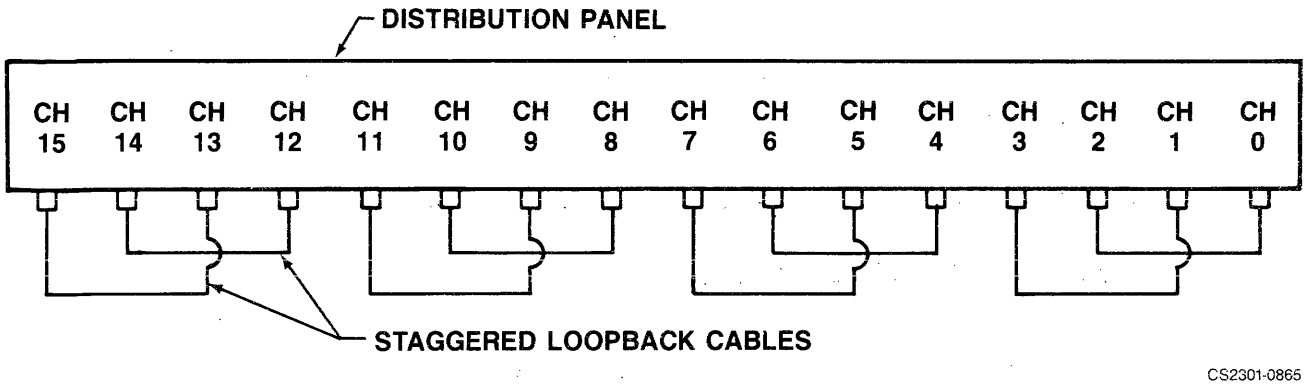

Figure D-3. DHU11 Staggered Loopback Connector Placement

D.3 EVDAI STANDALONE DIAGNOSTIC

EVDAI runs under the VAX Diagnostic Supervisor (VDS) V6.13 or later. The diagnostic has five modes of operation:

- internal loopback
- external loopback
- staggered loopback
- modem loopback
- terminal echo

The format of the START command (see subsection D.3.1.2) determines which tests are performed.

Unless individual channel problems are indicated, tests should start with the staggered loopback mode.

NOTE

Because not all channels on the distribution panels have all modem signals available, some EVDAI tests will not pass. The tests that will **not** pass are:

16 Channel Panels:

Internal Loopback Mode;

Test 19
Test 20 only if run immediately after Test 19

External Loopback Mode;

Test 19
Test 20 only if run immediately after Test 19
Test 22

Staggered Loopback Mode;

Test 19
Test 20 only if run immediately after Test 19
Test 22

12 Channel Panels: (select lines 0-11 only)

Internal Loopback Mode;

Test 12
Test 20 only if run immediately after Test 19

External Loopback Mode;

Test 12
Test 20 only if run immediately after Test 19
Test 22 on channels 8-11

Staggered Loopback Mode;

Test 12
Test 20 only if run immediately after Test 19
Test 22 on channels 4-11

D.3.1 RUNNING EVDAI

The minimum requirements to run EVDAI are:

- a VAX system with a UNIBUS
- a console terminal
- a CS23/E1
- an extra terminal if the terminal echo test will be run

Instructions for loading and running programs under VDS are provided in the VAX Diagnostic System User's Guide (DEC part number EK-DS780-UG). Details of the standalone test can be found in the diagnostic listing ZZ-EVDAI.

D.3.1.1 Starting EVDAI

After the diagnostic supervisor is booted:

1. Load EVDAI
2. Attach the CS23/E1
3. Select the device(s) to be tested
4. Start the diagnostic

The following is an example of what is entered to perform the above steps:

```
DS>  LOAD EVDAI                                  (loads the program)
DS>  SET TR,H                                    (sets trace and halt on
                                                 error)
DS>  ATTACH DHU11 DW0 TYA 760460 310 5
       |      |    |   |    |     |  |
       |      |    |   |    |     |  |--BR interrupt level
       |      |    |   |    |     |-----vector address
       |      |    |   |    |-----------CSR address
       |      |    |   |----------------name unit
       |      |    |--------------------linking the option to UBA
       |      |-------------------------device to be ATTACHed
       |------------------------------ATTACH command

DS>  SET TYA                                     (selects the device for
                                                 test)
DS>  ST                                          (starts the diagnostic)
```

D.3.1.2 Options

Once the program starts the user is prompted to select the following options:

- lines to be tested
- line speed
- type of loopback

The default selection of tests is to run tests 1 through 26. Specific tests can be selected at the START command. Also, the number of passes for each test can be selected at the START command.

The following example shows how to run tests 7 through 10 with 3 passes:

```
DS>  START/PASS:3/TEST:7:10
```

D.3.1.3 Event Flags

Event flag 1 can be used to disable the ROM version number message. It is used as follows:

```
DS>  SET EVENT 1
```

D.3.1.4 Sections

The SECTION command used at the START command allows selection of test types. Modem loopback tests or terminal echo tests can be selected. The SECTION command is used as follows:

```
DS>  ST/SE:MODEM                    (selects modem loopback
                                     tests)

or

DS>  ST/SEC:ECHO                    (selects terminal echo
                                     tests)
```

The test will run until either an error or CTRL Y is detected.

Pressing the break key during the terminal echo test halts the test and causes a framing error which generates an error message.

D.4 EVDAH ONLINE DIAGNSOTIC

The EVDAH Online Diagnostic runs in the online mode under VMS V4.0 or later. The operator interface is via the VAX Diagnostic Supervisor (VDS), V6.13 or later. The EVDAH diagnostic is supported by the online help facility EVDAH.HLP.

EVDAH consists of five tests:

- internal data-loopback test on selected channels in sequence
- internal DMA data-loopback test on selected channels in sequence
- internal data-loopback on selected channels at the same time
- external loopback test of modem control signals
- external data-loopback via a modem or wrap-around connector. If a modem is used it must be set up manually.

Before running EVDAH be aware of the following:

1. The tests are online; therefore it is essential to select the channels to be tested. If a channel is allocated to a process, it will not be run if selected for testing. Channel allocations can be checked using the SHOW DEVICE command: SH DEV/FULL TYA (where TYA is the name unit).

2. If test 4 is to be run, a DHU11 wrap-around connector (Emulex part number CU0411203) must be used on the selected channel. By setting Event Flag 20, the program will be halted between channel tests to allow the wrap-around connector to be moved to another channel. Event Flag 21 causes the program to halt after each DHU11 is tested.

3. If test 5 is run, a modem or a DHU11 wrap-around connector must be installed on the selected channel. The event flags also function in this test.

4. If tests 4 or 5 are run without a loopback connector installed, error messages are generated.

5. In the CS23/E1 hardware adjacent channels are paired (see subsection 6.2.4). An attempt to change a baud rate that will change the group of an allocated channel generates error messages, and the baud rate is not changed.

D.4.1 RUNNING EVDAH ONLINE

The minimum hardware requirements for running EVDAH are:

- a VAX system with a UNIBUS
- a console terminal
- a CS23/E1

Instructions for loading and running programs under VDS are provided in the VAX Diagnostic System User's Guide (DEC part number EK-DS780-UG). Details of the online tests can be found in the diagnostic listing ZZ-EVDAH.

D.4.1.1 Starting EVDAH

After VMS is booted:

1. Log into the system maintenance account
2. Allocate the lines to be tested
3. Load the diagnostic supervisor
4. Attach the CS23/E1
5. Select the device(s) for test
6. Start the diagnostic

The following is an example of what is entered to perform steps 2 through 6:

```
$  ALL TYA0                                  (allocates lines to be
                                              tested)
$  ALL TYA1
$  ALL TYA2

$  RUN ESSAA                                 (for VAX-11/780,
                                              Supervisor
   or

$  RUN ECSAA                                 (for VAX-11/750)

   or

$  RUN ENSAA                                 (for VAX-11/730)

DIAGNOSTIC SUPERVISOR ZZ-ENSAA-Y6. 13-510 10-JAN-1986 12:00: 00.00

DS>  ATT DW780 SBI DW0 3 4                   (for VAX-11/780 ATTACH the
                                              UBA on the SBI)

     or

DS>  ATT DW750 HUB DW0                       (for VAX-11/750)

     or

DS>  ATT DW730 HUB DW0                       (for VAX-11/730)

DS>  LOAD EVDAH                              (loads the diagnostic)
DS>  ATT DHU11                               (ATTACHes the DHU11)
DEVICE LINK? DW0                             (the option is linked to
                                              the UBA)
DEVICE NAME? TYA                             (the option named unit;
                                              range from A-F)
CSR? 760460                                  (CSR address)
VECTOR? 300                                  (vector address)
BR? 5                                        (BR interrupt level)

DS>  SEL TYA:                                (select unit under test)
DS>  START                                   (start diagnostic
                                              execution)
```

The program should now be running.

If preferred, the ATTACH command and parameters can be input as one statement:

```
DS>  ATTACH DHU11 DW0 TYA 760460 310 5
       |      |    |   |    |     |  |
       |      |    |   |    |     |  |--BR interrupt level
       |      |    |   |    |     |-----vector address
       |      |    |   |    |-----------CSR address
       |      |    |   |----------------name unit
       |      |    |--------------------linking the option to UBA
       |      |-------------------------device to be ATTACHed
       |--------------------------------ATTACH command
```

D.4.1.2 Options

Once the program starts, the user is asked to select a number of options:

- lines which are to be tested
- baud rate
- type of loopback

LINES TO BE TESTED

The following question will be displayed:

```
Lines to test [(ALL),REV,EVE,ODD,0,1,2,3,4,5,6,7,8, 9,10,11,12,
13,14,15]
```

The possible responses are:

ALL - Test all lines in ascending order. This is the default.

REV - Test all lines in descending order.

EVE - Test lines 0, 2, 4, 6, 8, 10, 12, and 14.

ODD - Test lines 1, 3, 5, 7, 9, 11, 13, and 15.

n - Test line line (where n can be any number).

n,m - Test lines n,m (where n,m can be any combination of line numbers; for example; 0,15,3,7,1). The lines will be tested in the sequence entered.

Any invalid entry will display the following error message:

```
?? Invalid response
```

followed by a reprompt of the input request.

BAUD RATE

The following question will be displayed:

```
Baud Rate [(9600),50,75,110,134,150,300,600,1200,1800,2000,2400,
4800,7200,19200,38400]
```

One of two responses can be given:

n - A specific value

<CR> - The default rate (9600 bits/s)

An invalid entry will display the following error message:

?? Invalid response

followed by a reprompt of the input request.

TYPE OF LOOPBACK

The following question will be displayed:

```
Loop Type [(INTERNAL),MODEM,H325]
```

The H325 is the wrap-around connector (Emulex part number CU0411203).

The possible responses that can be given are:

INTERNAL - Internal loopback will be used in the test. This is the default response.

MODEM - A modem preset to loopback.

H325 - External wrap-around connector is to be used.

An invalid entry will display the following error message:

?? Invalid response

followed by a reprompt of the input request.

D.4.1.3 Event Flags

Event flags are used to control multichannel or multi-DHU11 tests. Flags are set by the Set Event Command.

FLAG 20 - Functions in tests 4 and 5 only. When flag 20 is set, the program is suspended after each channel is tested. A supervisor message invites the operator to transfer the wrap-around connector or modem to the next channel to be tested.

FLAG 21 - Functions in all tests. This flag is useful when more than one DHU11 emulation is being tested. This event flag has different functions in internal and external loopback tests.

INTERNAL TEST FUNCTIONS -

Flag 21 = 0 Only the first DHU11 emulation is selected.

Flag 21 = 1 All DHU11 emulations are tested in the selected order. Console messages indicate the module under test. For example:

```
INTERNAL LOOPBACK ON UNIT 000
INTERNAL LOOPBACK ON UNIT 001
INTERNAL LOOPBACK ON UNIT 002
INTERNAL LOOPBACK ON UNIT 003
```

EXTERNAL TEST FUNCTIONS -

Flag 21 = 0 Only the first DHU11 emulation is selected.

Flag 21 = 1 The program is suspended before each module is tested. Console messages warn the user to transfer the wrap-around connector or modem.

D.4.1.4 Sections

The SECTION command is part of the START command. The SECTION command allows the user to select a specific set of tests to be run. The default for tests to be run is tests 1, 2, and 3. If SECTION is specified as MANUAL, tests 4 and 5 are run. The following is an example of the SECTION and MANUAL command:

```
DS>  START                          (runs tests 1, 2, and 3)
DS>  START/SEC=MANUAL               (runs tests 4 and 5)
```

D.4.1.5 Error Messages

If an error is detected during a test, the program will output an error message. This indicates that the option is defective or that an illegal parameter has been selected. Error numbers are listed in the diagnostic listing ZZ-EVDAH.

Appendix E
ASCII CODE CONVERSION

Table E-1. ASCII Seven-Bit Code

Octal	Hex	Decimal	Mnemonic	Description
000	00	000	NUL	Blank
001	01	001	SOH	Start of Header
002	02	002	STX	Start of Text
003	03	003	ETX	End of Text
004	04	004	EOT	End of Transmission
005	05	005	ENQ	Enquiry
006	06	006	ACK	Acknowledge (Positive)
007	07	007	BEL	Bell
010	08	008	BS	Backspace
011	09	009	HT	Horizontal Tabulation
012	0A	010	LF	Line Feed
013	0B	011	VT	Vertical Tabulation
014	0C	012	FF	Form Feed
015	0D	013	CR	Carriage Return
016	0E	014	SO	Shift Out
017	0F	015	SI	Shift In
020	10	016	DLE	Data Link Escape
021	11	017	DC1	Device Control 1 (X-ON)
022	12	018	DC2	Device Control 2
023	13	019	DC3	Device Control 3 (X-OFF)
024	14	020	DC4	Device Control 4--Stop
025	15	021	NAK	Negative Acknowledge
026	16	022	SYN	Synchronization
027	17	023	ETB	End of Text Block
030	18	024	CAN	Cancel
031	19	025	EM	End of Medium
032	1A	026	SUB	Substitute
033	1B	027	ESC	Escape
034	1C	028	FS	File Separator
035	1D	029	GS	Group Separator
036	1E	030	RS	Record Separator
037	1F	031	US	Unit Separator
040	20	032	SP	Space
041	21	033	!	
042	22	034	"	
043	23	035	#	
044	24	036	$	
045	25	037	%	
046	26	038	&	
047	27	039	'	Closing Single Quote
050	28	040	(	
051	29	041	)	
052	2A	042	*	
053	2B	043	+	
054	2C	044	,	Comma
055	2D	045	-	Hyphen
056	2E	046	.	Period
057	2F	047	/	
060	30	048	0	
061	31	049	1	
062	32	050	2	
063	33	051	3	
064	34	052	4	
065	35	053	5	
066	36	054	6	
067	37	055	7	
070	38	056	8	
071	39	057	9	
072	3A	058	:	
073	3B	059	;	
074	3C	060	<	Less Than
075	3D	061	=	
076	3E	062	>	Greater Than
077	3F	063	?	
100	40	064	@	
101	41	065	A	
102	42	066	B	
103	43	067	C	
104	44	068	D	
105	45	069	E	
106	46	070	F	
107	47	071	G	
110	48	072	H	
111	49	073	I	
112	4A	074	J	
113	4B	075	K	
114	4C	076	L	
115	4D	077	M	
116	4E	078	N	
117	4F	079	O	
120	50	080	P	
121	51	081	Q	
122	52	082	R	
123	53	083	S	
124	54	084	T	
125	55	085	U	
126	56	086	V	
127	57	087	W	
130	58	088	X	
131	59	089	Y	
132	5A	090	Z	
133	5B	091	[	Opening Bracket
134	5C	092	\	Reverse Slant
135	5D	093	]	Closing Bracket
136	5E	094	^	Circumflex
137	5F	095	_	Underline
140	60	096	`	Opening Single Quote
141	61	097	a	
142	62	098	b	
143	63	099	c	
144	64	100	d	
145	65	101	e	
146	66	102	f	
147	67	103	g	
150	68	104	h	
151	69	105	i	
152	6A	106	j	
153	6B	107	k	
154	6C	108	l	
155	6D	109	m	
156	6E	110	n	
157	6F	111	o	
160	70	112	p	
161	71	113	q	
162	72	114	r	
163	73	115	s	
164	74	116	t	
165	75	117	u	
166	76	118	v	
167	77	119	w	
170	78	120	x	
171	79	121	y	
172	7A	122	z	
173	7B	123	{	Opening Brace
174	7C	124	|	Vertical Line
175	7D	125	}	Closing Brace
176	7E	126	~	Overline (Tilde)
177	7F	127	DEL	Delete/Rubout

CS2301-0125

The following definitions are made within the context of the communications subsystem that is described in this manual. Consequently, the definitions are not generally applicable to the field of data communications, and they contain specific references to the Emulex equipment in question.

Analog signals: Information presented by continuous and smoothly varying signal amplitude or frequency over a certain range. (See also digital signals.)

ASCII: American Standard Code for Information Interchange. This is a seven-bit-plus-parity code established by the American National Standards Institute to achieve compatibility between data services.

Asynchronous transmission: Transmission in which time intervals between transmitted characters may be of unequal length. Transmission is controlled by start and stop elements at the beginning and end of each character. Also called Start-Stop transmission.

Baud: A unit of signaling speed equal to the number of discrete conditions or signal events per second. In asynchronous transmission, the unit of signaling speed corresponds to one unit interval per second. Thus, if the duration of the unit interval is 20 milliseconds, the signaling speed is 50 baud. Baud is the same as "bits per second" (bps) only if each signal event represents exactly one bit. A baud is the reciprocal of the unit interval (see unit interval).

bps: See baud.

Buffer: A storage device used to compensate for a difference in the rate of data flow when transmitting data from one device to another.

Busy: A signal associated with modem control. The ON condition on this circuit indicates that the modem is currently in use.

DCD: Data Carrier detect. A signal associated with modem control. The ON condition on this circuit is present when the data communication equipment is receiving a signal which meets its suitability criteria. These criteria are established by the data communication equipment manufacturer.

Channel: An individual, non-multiplexed data communications link between the data terminal equipment (DTE) and the data communication equipment (DCE).

Common Carrier: A company that provides telecommunications intended mainly, in a public correspondence service, for the transmission, emission, or reception of signals, written images, and sounds. The transmission is via wire, radio, optical, or other electromagnetic systems between specific points subject to appropriate remuneration.

Communications Multiplexer: A microprocessor-based control module that provides a structured interface between the host computer's operating system (via the bus) and remote and local data communications channels.

Under microprocessor control, the control module multiplexes inbound data from a number of external communications channels on to the host computer's internal data bus. In the outbound direction, it demultiplexes data from the bus and distributes the data to the appropriate channels.

In the CS23/E1, statistically multiplexed data from the remote link is converted to a form acceptable to the operating system's data communications protocol. The CS23/E1 also places outbound data in the statistically multiplexed format.

Configuration: The physical and logical arrangement of a system as defined by the nature, number, and the chief characteristics of its functional units.

CSR: Control Status Register. One of the CS23/E1's directly addressable registers.

CTS: Clear to send. A signal associated with modem control. Signals on this circuit are generated by the data communication equipment to indicate whether or not the data set is ready to transmit data.

Data Communication Equipment (DCE): The equipment that provides the functions required to establish, maintain, and terminate a connection, the signal conversion, and coding required for communication between data terminal equipment and data circuit. With reference to the RS-232-C interface, the equipment with the female connector; transmitted data is on pin 3 and received data is on pin 2.

Data Terminal Equipment (DTE): The equipment comprising the data source, the data destination, or both. That is, either a computer or a terminal. With respect to the RS-232-C interface, the equipment with the male connector; transmitted data is on pin 2 and received data is on pin 3.

Digital signals: Information presented using only two different levels of voltage or current. These types of signals are often used in communications because they are simple to generate, detect, and use. (see also analog signals)

DMA: Direct memory access. A facility that permits I/O transfers directly into or out of memory without passing through the CPU's general registers. The transfers are either performed independently, or on a cycle-stealing basis.

DSR: Data set ready. A signal associated with modem control. Signals on this circuit are used to indicate the status of the local set.

DTR: Data terminal ready. A signal associated with modem control. Signals on this circuit are used to control switching of the data communication equipment to the communication channel.

Duplex: See full-duplex.

EIA: Electronic Industries Association. A standards organization specializing in the electrical and functional characteristics of interface equipment.

FCC: Federal Communications Commission.

Full-Duplex: Simultaneous two-way independent transmission in both directions. Also called duplex.

Half-Duplex: A circuit designed for transmission in either direction but not in both directions simultaneously.

Marking Condition: The state of a line when the voltage on the line is more negative than -3 V with respect to the signal ground. For the CS23/E1, an idle line is in the marking condition. Also, although lines are generally considered to be in a marking or spacing condition, modem lines are considered OFF when in the marking condition.

NXM: Non-Existent Memory.

RI: Ring. A signal associated with modem control. The ON condition of this circuit indicates that a ringing signal is being received on the communication channel.

RS-232-C: A standard for the interface between Data Terminal Equipment and Data Communications Equipment employing serial binary exchange.

RTS: Request to Send. A signal associated with modem control. This signal is used to condition the local data communication equipment for data transmission and, on a half-duplex channel, to control the direction of data transmission of the local communication equipment.

Spacing Condition: The state of a line when the voltage on the line is more positive than +3 V with respect to the signal ground. For the CS23/E1, a line bring sent a break is in the spacing condition. Also, although lines are generally considered to be in a marking or spacing condition, modem lines are considered ON when in the spacing condition.

SPC: Small Peripheral Controller.

Statistical Multiplexing: A time division multiplexing technique used to combine several individual channels which have low overall activity (if not low absolute speed) onto a single composite data link. This technique is predicated upon the statistical likelihood that none of the multiplexed channels will be receiving or transmitting data continually. However, buffering is generally provided to absorb peak load conditions. For example, several dumb asynchronous terminals configured to operate at 9600 bps will have an aggregate data rate of considerably less than 9600 bps. Using statistical multiplexing, all of the several channels can be carried over a single composite link with no noticeable loss in response time except during peak loads (if all the CRTs were being repainted at once, for example).

Synchronous Transmission: Transmission in which the data characters and bits are transmitted at a fixed rate with the transmitter and receiver synchronized. This method of transmission eliminates the need for start and stop elements at the beginning and end of each character, thus providing greater efficiency.

UBA: UNIBUS Adapter.

Unit interval: The duration of the shortest nominal signal element. It is the longest interval of time such that the nominal durations of the signal elements in a synchronous system or the start and information elements in a start-stop system are whole multiples of this interval. The duration of the unit interval (in seconds) is the reciprocal of the telegraph speed expressed in baud.

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