SC02/A

(RP02/RP03 COMPATIBLE)

DISK CONTROLLER

TECHNICAL MANUAL

EMULEX

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1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC02/A Disk Controller. In addition, this manual provides diagnostics and application information.

1.2 OVERVIEW

1.2.1 General Description

The SC02/A Disk Controller is a single board imbedded controller for LSI-11 computers manufactured by Digital Equipment Corporation (DEC). This controller can be used to interface any large disk having a Storage Module Drive (SMD) interface. The SC02/A controller emulates the RP11-E disk controller manufactured by DEC for use with RP02 and RP03 disk drives.

1.2.2 SC02/A Emulation of RP11-E

The RP11-E provides a convenient controller architecture for a wide variety of modern technology type disks. It is supported by all DEC operating systems and is easy to program.

In mapping RP02 or RP03 logical disk(s) onto the physical drive, all aspects of the RP02/03 disk organization stay the same except for the number of cylinders. The number of logical tracks per cylinder is always 20. In patching the DEC operating systems for non-standard capacity RP02 or RP03, it is necessary to change only the maximum block size parameter. A summary of the RP02/03 characteristics is found in Table 1-1.

The SC02/A controller can handle two disk drives of the same or different capacities. Each drive is configured from information in a configuration PROM. This technique permits up to 64 different switch selectable combinations of disk drive configurations on the two controller ports.

1.3 FEATURES

1.3.1 Microprocessor Design

The SC02/A design incorporates a unique 8-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The

of 64 possible combinations of disk characteristics for the two drives which can be handled by the controller, including mixtures of disk sizes and drive type codes.

1.3.7 Dual Port Capability

The SC02/A controller does not support programmable dual port capability. Those disk drives that have dual port hardware may be used in a dual port configuration if the port select switch is in the Channel I only or Channel II only position. The middle (programmable) position creates errors.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Media Compatibility

In all cases, the headers written on the drives are not standard RP02/RP03 headers. In addition, a 3-to-1 sector interleave is generated by the hardware formatter. DEC does not provide the software to hardware format RP02/RP03 systems. The necessary program is available from Emulex (part number SXAX0), or see paragraph 3.7.3 for hardware formatting instructions. Disk packs formatted with an SC02/A controller are not media compatible with models SC01/A or SC11/A Emulex controllers.

1.4.2 Disk Mapping

Depending upon the type and size of the disk drive, one to eight logical units may be mapped on it. The mapping is done in a straightforward manner with only the number of heads and/or number of cylinders being varied. An option switch also allows selection of a nonmapped mode so that the logical address is the physical address.

1.4.3 Diagnostics

See Appendix C for patches to the standard DEC RP02/RP03 diagnostics. Emulex Corporation provides a set of diagnostics specifically designed to test the SC02/A controller.

1.4.4 Operating Systems

When emulating standard size RP02/RP03 disk subsystems the SC02/A is compatible with all DEC operating systems, and no modifications to the operating systems are required. When a non-standard capacity RP02/RP03 is emulated, the disk driver's maximum block count must be patched to reflect the different capacity. Patch documentation is available from Emulex (SCXX Disk Capacity Patches, part number PD9951002).

Table 1-1
RP11/RP02/RP03 Disk Subsystem Characteristics

Characteristics	Specifications	
	RP02	RP03
Platters/Drive	11	11
MBytes/Logical Unit	20.8	41.6
Blocks/Drive	40600	81200
Tracks/Cylinder	20	20
Cylinders/Drive	203	406
Sectors/Track	10	10
Data Bytes/Sector	512	512
Drives/Controller,Max	8	8
Speed, RPM	2400	2400
Bit Density, (BPI)	2020	2020
Data Rate, (KBYTES/SEC)	204.8	204.8

Table 1-2
General Specification

Functional

Emulation	DEC RP02 and RP03
Media Format	3-to-1 sector interlace
Drive Interface	SMD
Drive Ports	2
Error Control	32-bit ECC for data and 32-bit CRC for headers. Correction of single data error burst of up to 11 bits.
Sector Size	256 words (512 bytes)
Sectors/Track	Selectable for each drive
Tracks/Cylinder	Selectable for each drive
Cylinders/Drive	Selectable for each drive
Drive Type Code	Selectable for each drive (RP02 or RP03)
Computer Interface	LSI-11 Q-Bus
Vector Address	254 Standard,150,370,374 Optional
Priority Level	Level 5
Data Bufferring	1 Sector (256 words)
Data Transfer	High speed DMA operation
Self-Test	Extensive internal self-test on powering up

Table 1-2 (Cont.)
General Specification

Functional

    Indicator   Activity/Error/Status LED

    Options   512 word bootstrap/Q-Bus terminators/BDV11 compatible line time clock (LTC) control

    Q-Bus Addresses   Controller registers: 776700-776736
                          Bootstrap PROM: 773000-773776 and
                                  765000-765776
                          LTC register: 777546

    Design   High-speed bipolar microprocessor using 2901 bit-slice components

Physical

    Mounting   Any LSI-11 Quad slot in CPU or expansion box

    Connectors   One 60-pin A Cable flat connector and two 26-pin B Cable connectors. (Flat cable type.)

Electrical

    Q-Bus Interface   DEC approved line drivers and receivers

    Drive Interface   Differential line drivers and receivers. A Cable cumulative length to 35 feet. B Cable length to 25 feet.

    Power   +5V, 5%, 5.5 Amp.

2.1 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC02/A controller is shown in Figure 2-1. The SC02/A controller is organized around an 8-bit high-speed bipolar microprocessor. The arithmetic and logic unit (ALU) and register file portions of the microprocessor are implemented with two 2901 bit-slice components. The microinstruction is 48 bits in length and the control memory of 1K words is implemented with twelve 1K x 4 PROMs.

The controller incorporates a 1K x 8 high-speed RAM buffer which is used to store the controller's device registers and one sector (512 bytes) of data buffering.

The A Cable Register (ACR) provides the storage of all A Cable signals going to the disk drives. The inputs from the selected drive are testable by the microprocessor.

Serial data from the drive is converted into 8-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data accessed from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC Shift Register is used to generate and check the ECC for the data field. The same register is also used in a 32-bit CRC mode for the headers. The actual ECC polynomial operation is done independent of the microprocessor, but the determination of the error position and error pattern is done under the control of the microprocessor.

The Q-Bus interface consists of 36 bidirectional and 2 unidirectional signal lines. The Q-Bus interface is used for programmed input/output (I/O), CPU interrupts, and Data Transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all direct memory access (DMA) operations and transfers data between the Q-Bus data lines and the buffer.

2.2 PHYSICAL DESCRIPTION

The SC02/A controller consists of a single quad-size board which plugs directly into a LSI-11 chassis. Figure 2-2 shows the board.

2.2.1 Connectors

2.2.1.1 A Cable Connector

The 60-pin flat cable connector labeled J3 at the top edge of the board is for the A Cable which daisy-chains to all the drives for

Data Bus

8-Bit ALU and Register File	1K x 8 RAM Buffer	A Cable Register

A Cable

Q-Bus Address and Data	Control Memory (PROMs)	Shift Register

Q-Bus

Write
Data

B Cable

Read
Data

Address Decode	Se- quencer	Switches	ECC Logic

**Test
Mux**
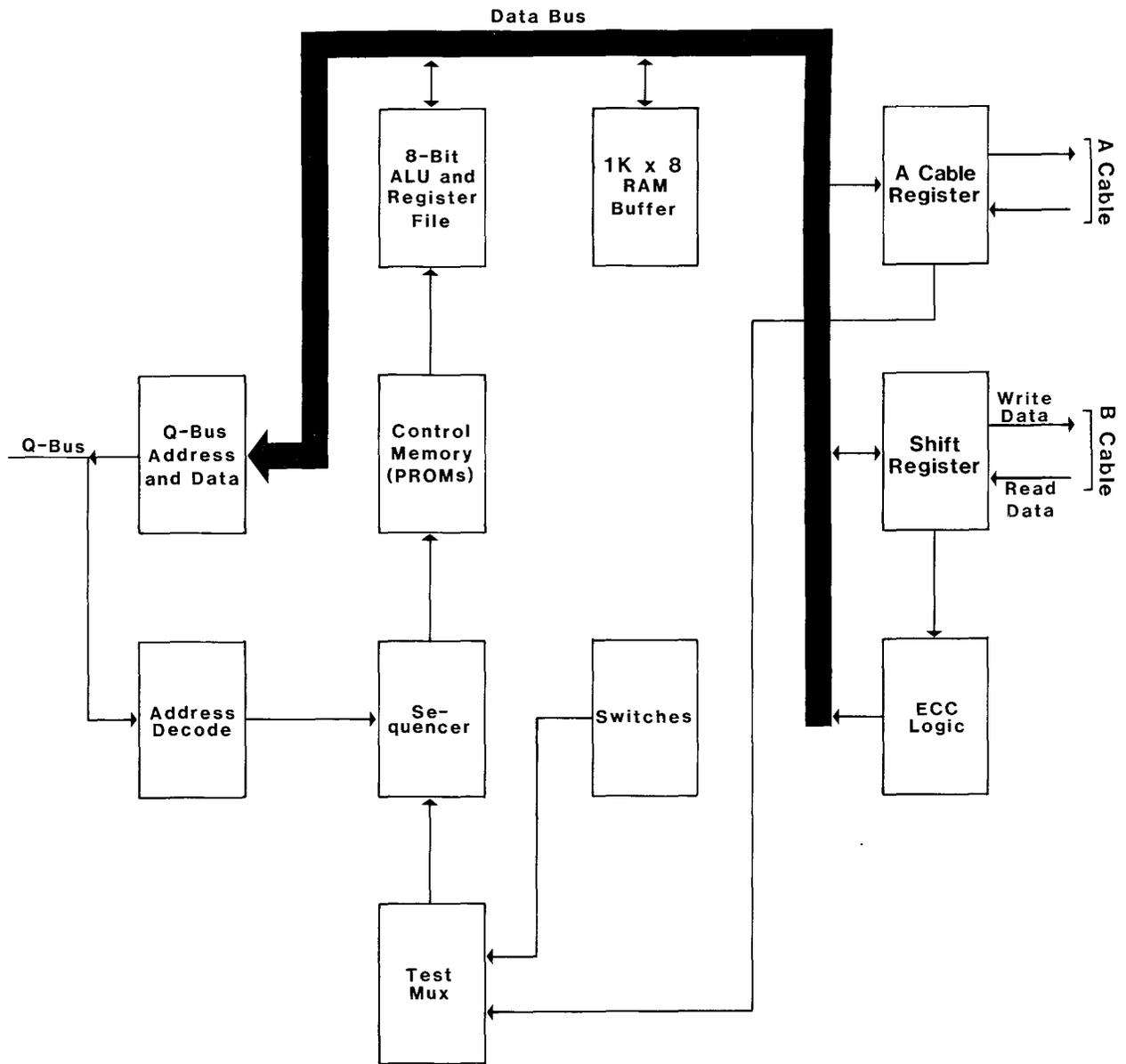
Figure 2-1 SC02 Block Diagram
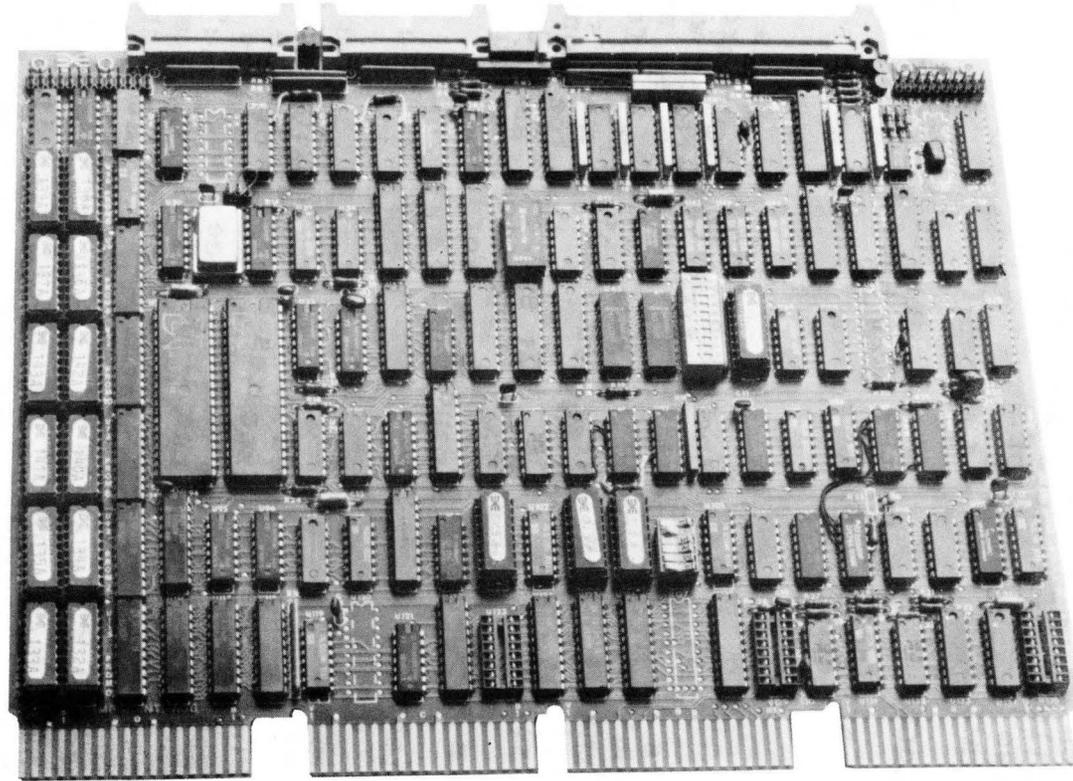
Figure 2-2 SC02 Controller Board

SC0201-0029

control and status. Pin 1 is located on the left side of the connector.

2.2.1.2 B Cable Connector

The two 26-pin flat cable connectors labeled J1 and J2 are for the radial B Cables to each of two physical drives which may be attached to the controller. Pin 1 is located on the left side of the connector. The two B Cable ports are all identical and any drive may be plugged into any connector.

2.2.1.3 Test Connectors

Connectors J4 and J5 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.2 Switches

There are three sets of switches labeled SW1-SW3. SW1 is a four pole DIP 'piano-type' switch accessible from the PC board edge. Locating SW1 such that it is accessible to the operator while the controller is imbedded in a LSI type chassis, makes the selection of common options such as hardware format simpler to perform.

The other two sets of switches SW2 and SW3 provide controller address decoding selection, option selection and drive configuration selection. See Appendix A for detailed switch settings.

2.2.3 LED Indicator

There is an LED indicator mounted between the connectors at the top of the board. The controller executes an extensive self-test when powering up. The microprogrammed organization of the controller permits most logic other than the interface circuitry to the disk to be validated before the controller becomes ready. The LED lamp is turned on as the controller starts its self-test and is turned off only when the controller successfully completes the test. If a malfunction is detected by the built-in diagnostics, the LED remains ON and the controller will not respond to program I/O. The LED blinks at approximately a one second rate if the self-test is successful but no drive is seen on-line. The LED also functions as an activity indicator during read and write operations.

2.2.4 Firmware PROMs

There are twelve PROM sockets, used for the control memory, located along the left edge of the board. The sockets are labeled PROM 0 through PROM 11 in a discontinuous physical order. The numbers on the top of the PROM ICs are Emulex part numbers, which identify the unique pattern of the PROM. When inserting PROMs in the board, the ID numbers are placed in the same sequence as the PROM numbers on the board beside each socket.

2.2.5 Bootstrap PROMs

There are two sockets provided for the installation of optional bootstrap PROMs. The socket in location U101 receives P/N 015x and the socket in location U103 receives P/N 014x.

2.3.1 Disk Interface

The controllers' disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD interface and is compatible with these drives electrically and in timing.

The following defines the electrical interface and the recommended cables.

2.3.1.1 A Cable

The 60-conductor A Cable is daisy-chained to all drives and terminated at the last drive. The signals in this cable, along with their function when the control tag (Tag 3) is asserted, are listed in Table 2-1. The A Cable should be 30 twisted pair flat cable with an impedance of 100 ohms and an cumulative length of no greater than 35 feet.

Spectra-Strip P/N 455-248-60 flat cable or its equivalent is recommended. It is possible to order A-Cable assemblies from Emulex that are made up in one of four lengths:

EMULEX P/N	LENGTH (FT.)
SU1111201	8.0
SU1111203	15.0
SU1111205	25.0
SU1111207	35.0

2.3.1.2 B Cable

The 26-conductor B Cable is radial to all drives and contains the data and clock signals. The signals and grounds in this cable are listed in Table 2-1. The B Cable should be 26 conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length must not be greater than 25 feet.

3M-P/N 3476/26 flat cable or its equivalent is recommended. It is possible to order B Cable assemblies from Emulex that are made up in one of three lengths:

```
EMULEX P/N          LENGTH (FT.)
------------------------------------
SU1111202           8.0
SU1111204           15.0
SU1111206           25.0
------------------------------------
```

2.3.2   Q-Bus Interface

The LSI-11 Bus consists of 36 bidirectional and 2 unidirectional signal lines. These form the lines along which the processor, memory and I/O devices communicate with each other.

Addresses, data, and control information are sent along these signal lines, some of which contain time-multiplexed information. The lines are divided as follows:

    18 Data/address lines-BDAL00-BDAL17

    6 Data Transfer control lines - BBS7, BDIN, BDOUT, BRPLY, BSYNC, BWTBT

    3 Direct memory access control lines - BDMG, BDMR, BSACK

    6 Interrupt control lines - BEVNT, BIAK, BIRQ4, BIRQ5, BIRQ6, BIRQ7

    5 System control lines - BDCOK, BHALT, BINIT, BPOK, BREF

2.3.2.1   Interrupt Priority Level

The controller is hardwired to issue level 4 and level 5 interrupt requests. The level 4 request is necessary to allow compatibility with either a LSI-11 or LSI-11/2 processor.

2.3.2.2   Register Address

The register address and the number of registers assigned to the controller are decoded by a PROM at U104. The selections available are determined by configuration switch SW1 as discussed in Section 3.

2.3.2.3   DCOK and INIT Signals

The DCOK and INIT signals both perform a controller clear. The self-test is performed only when DC power is initially applied.

Table 2-1
Disk Drive Connections

Pins Lo/Hi	Signal	(Tag 3 Function)	From/To
A Cable:			
22,52	Unit Select Tag		To
23,53	Unit Select bit 0		To
24,54	Unit Select bit 1		To
26,56	Unit Select bit 2		To
27,57	Unit Select bit 3		To
1,31	Tag 1		To
2,32	Tag 2		To
3,33	Tag 3		To
4,34	Bit 0	(Write Gate)	To
5,35	Bit 1	(Read Gate)	To
6,36	Bit 2	(Servo Offset Plus)	To
7,37	Bit 3	(Servo Offset Minus)	To
8,38	Bit 4	(Fault Clear)	To
9,39	Bit 5	(AM Enable)	To
10,40	Bit 6	(Return to Zero)	To
11,41	Bit 7	(Data Strobe Early)	To
12,42	Bit 8	(Data Strobe Late)	To
13,43	Bit 9	(Release)	To
30,60	Bit 10		To
14,44	Open Cable Detect		To
15,45	Fault		From
16,46	Seek Error		From
17,47	On Cylinder		From
18,48	Index		From
19,49	Unit Ready		From
20,50	NOT USED		From
21,51	Busy (dual port only)		From
25,55	Sector		From
28,58	Write Protected		From
29	Power Sequence Hold		To
59	Power Sequence Pick		To
B Cable:			
8,20	Write Data		To
6,19	Write Clock		To
2,14	Servo Clock		From
3,16	Read Data		From
5,17	Read Clock		From
10,23	NOT USED		From
22,9	Unit Selected		From
12,24	NOT USED		From
13,26	NOT USED		From

Table 2-2
Q-Bus Connections

| | A | | B | |
	1	2	1	2
A	BIRQ5	+5V	BDCOK	+5V
B	BIRQ6		BPOK	
C	BAD16	GND		GND
D	BAD17			
E		BDOUT		BDAL02
F		BRPLY		BDAL03
H		BDIN		BDAL04
J	GND	BSYNC	GND	BDAL05
K		BWTBT		BDAL06
L		BIRQ4		BDAL07
M	GND	BIAKI	GND	BDAL08
N	BDMR	BIAKO	BSACK	BDAL09
P	BHALT	BBS7	BIRQ7	BDAL10
R	BREF	BDMGI	BEVNT	BDAL11
S		BDMGO		BDAL12
T	GND	BINIT	GND	BDAL13
U		BDAL00		BDAL14
V		BDAL01		BDAL15

2.4 DISK FORMAT

2.4.1 Disk Pack Organization

The formatting of a disk pack and the mapping of one or more logical drives onto a physical drive varies with the drive size. Some of this information is supplied by the configuration PROM. The rest is computed based upon configuration PROM information. In all cases, the headers actually written on the drives are not standard RP02/RP03 headers. In addition, a 3-to-1 sector interleave is generated by the hardware formatter. There is no software formatting possible with this controller. Disk packs formatted with an SC02/A controller are not media compatible with models SC11/A or SC01/A Emulex controllers.

2.4.2 Mapping

Depending upon the type and size of the disk drive, one to eight logical units may be mapped onto it. The controller can handle a maximum of eight logical units distributed across a maximum of two physical disk drives. Some drives are mapped by cylinders, i.e., "X" number of physical cylinders equals one logical unit. Some drives are mapped by tracks, i.e., "X" number of physical tracks equals one logical unit ("X" can be one, as would be the case with a CMD). The number of physical sectors per physical track is determined by the following three requirements:

1. A minimum of 570 bytes/sector is required.

2. There can be no sectors of less than 570 bytes unless the sector pulse for the "runt" sector can be suppressed in the drive.

3. Removable media drives require a 574 bytes/sector minimum. For a typical SMD or CMD drive with 20160 bytes/track, 576 bytes/sector gives 35 sectors/track, all of equal size.

2.4.3 Sector Format

Each sector contains a detached two-word header and a 256 word data field. The header field is terminated with a 32-bit CRC and the data field is terminated with a 32-bit ECC. The controller attempts corrections only on the data field, never on the header. Each field is preceded by at least 11 bytes of zeros and an 8-bit SYNC byte.

In detail, each sector is organized as follows:

    4+   Sector pulse postamble zero bytes (varies by drive
            type)
    13   Header preamble zero bytes
    1   Sync byte
    4   Header bytes
    4   Header CRC bytes
    2   Header postamble zero bytes

    13   Data field preamble zero bytes
    1   Sync byte
    512   Data bytes
    4   Data ECC bytes
    2   Data postamble zero bytes
    10+   Recovery area (varies by drive type and number of
            sectors/tracks

    570+   Total Bytes

2.4.3.1 Header Field

The header preamble is used to synchronize the Phase Locked
Oscillator (PLO) in the drive to the data on the pack. The SYNC
byte is used by the controller to synchronize to the data bytes and
their boundaries, and by the drive to synchronize to the phase of
the data stream. The two header data words are organized as
follows:

    Word #1 - Logical cylinder address, right justified.

    Word #2 - Logical track and sector addresses, right justified;
              sector in low byte, track in high byte.

Neither the two data words nor the two CRC words for the header are
available to the user (see Read Header command, paragraph 5.9).
The header format is the same as the format followed by the
cylinder address (RPCA) and disk address (RPDA) registers.

2.4.3.2 Data Field

The data field preamble and SYNC bytes have the same functions as
the header preamble and SYNC bytes. The data field itself is
always 256 words long. Any unused portion of the sector will be
terminated with zero bytes during a write operation. The 32-bit
ECC is generated during a write, and is used during a read to check
the validity of the data. Any single error burst anywhere in the
data field of 11 bits or less can be corrected. Correction is
transparent, and is done before the data is sent to memory.

2.4.3.3 Postambles

The postambles provide areas for turning off the write amplifiers, for turning on read amplifiers, and for switching from read-to-write. Write splices will exist within all of these areas. The sector pulse postamble will also include a head-scatter area on removable media drives.

2.4.3.4 Recovery Area

The recovery area is used for housekeeping operations during a format. A minimum of eight microseconds (ten bytes @ 9.67 MHZ data rate) is required.

2.5 GENERAL PROGRAMMING INFORMATION

2.5.1 Clearing the Controller

A RESET is generated when the GO bit in RPCS is set with the function code bits all reset. A Controller RESET can be executed at any time, regardless of the state of the RDY bit in RPCS. No interrupt is generated at the completion of the reset operation.

A RESET clears the following registers:

- All bits in RPER, RPWC, RPBA, RPCA and RPDA.

- RPDS bits <07:00> (ATA bits).

- RPCS bits <06:00>, <15:08>. The RDY bit (bit 07) is set.

A Bus INIT executes a RESET.

During Data Transfer operations (Read, Write, Write Check, Format), any Write to any controller register results in the execution of RESET. During those operations the CPU may not write to any controller register while RDY equals zero. The user must either wait for an interrupt to be generated (which can't happen as long as RDY equals zero), or monitor the status of RDY with read-only instructions.

2.5.2 Interrupt Conditions

The controller generates an interrupt in the CPU due to the following conditions:

1. Upon termination of Data Transfer if Interrupt Done Enable (IDE) is set when the controller becomes ready (i.e., if IDE is set when RDY goes from zero to one).

2. Upon assertion of any attention bit while the controller is ready (RDY equals one), and the Attention Interrupt Enable (AIE) is set.

3. Upon termination of the initiate phase of a Seek or Home command if the Interrupt on Done Enable (IDE) is set when the controller becomes ready. This type of interrupt is usually used in overlapped seek drivers to initiate seeks in interrupt mode on two or more units.

4. When the program writes a one into IDE while RDY is set and IDE is reset. Writing a one into IDE when it is already set has no effect.

2.5.3 Termination of Data Transfers

A Data Transfer may terminate in any one of the following ways:

1. Normal Termination - Word count overflows to zero and the controller becomes ready at the end of the current sector.

2. Controller Error - An error occurs during a Data Transfer operation. The controller sets the appropriate error bit(s), terminates the Data Transfer immediately, and makes the controller ready.

3. Drive Error - An error occurs during a Seek or Data Transfer operation. The controller sets the appropriate error bit(s), terminates any Data Transfer that may be in progress, and makes the controller ready.

4. Program-Caused Abort - By performing a Controller Reset operation, the program can cause an abort of any operation. Status and error information are lost when this is done, and the controller becomes ready immediately.

2.5.4 Error Correction

The 32-bit ECC appended to every sector's data field allows the controller to detect read errors of any length, and correct single error bursts of one to 11 bits in length. However, not all read errors are corrected. The controller does not correct initial read errors, but flags the error instead to allow software logging. The next read error encountered after the first will result in a correction attempt. If the correction attempt is successful, then the corrected data is sent to the CPU and the controller continues as if no error existed. The Read Error Flag is also reset so that the next read error is seen as an initial read error. If the correction attempt is unsuccessful, then the error is flagged again. The Read Error Flag remains set so that the next attempted read of the bad sector also results in a correction attempt. INIT and RESET functions do not alter this flag. The user may manually reset the flag by writing (any data) into RPDB. Note that the ECH bit in RPER determines whether a read error correction was not attempted (ECH equals zero) or was unsuccessful (ECH equals one).

The Data Check (DCK) bit in RPER will be set in either case. See paragraph 4.3, Error Register. No correction is ever attempted during a Write Check. A Write operation will reset the Read Error Flag.

2.5.5 Line Time Clock (LTC)

The Line Time Clock is a 60 Hz clock generated by the power supply and distributed on the backplane as the BEVNT signal. A high to low transition of this signal interrupts the processor. BEVNT has the highest external interrupt priority; only processor interrupts have higher priorities. If external interrupts are enabled (PS bit 07 equals zero), the processor PC (R7) and PS words are pushed onto the processor stack. The LTC (or external event device) service routine is entered by vector address 100; the usual interrupt vector address input operation by the processor is not required since vector 100 is generated by the processor.

The LTC can be software controlled by using the Line Clock Register on the SC02/C. The Line Clock Register has a bus address of 777546. It is a one-bit, write-only register. Reads to this register return unspecified data. Bit 06 is the only bit implemented. A write to this register with bit 06 equals one enables the line clock. A write to this register with bit 06 equals zero disables the line clock. The enable bit need not be set again after an interrupt has been processed. The clock will continue to interrupt until bit 06 is reset or an INIT is generated.

See paragraph 3.4.5.3 for information on how to configure the processor for use with the LTC.

2.5.6 Bootstrap Routines

Installing the Emulex bootstrap option kit (number SC0213001) makes available two bootstrap routines: the standard console bootstrap and auto-boot sequence. See paragraph 3.4.5.2 for installation instructions.

NOTE: Be sure to disable any other boot options prior to use of the Emulex boot option.

2.5.6.1 Standard Console Bootstrap

The CPU enters the standard console bootstrap routine at location 773000. The CPU board can be jumpered to start at location 773000 automatically on power-up (or external DCLO set-reset). See paragraph 3.4.5.2.

After performing several CPU tests, the bootstrap program will prompt the operator with a dollar sign ($) on the standard terminal (bus addresses 777560-777564). At this point the bootstrap routine expects terminal input. If no $ is printed, then the boot program failed one of the CPU tests it executed prior to entering terminal input mode.

When the $ prompt has been printed, the boot program is ready for
input from the terminal. The user should enter one of the
two-character codes from the Table 2-3 (plus a single octal number
if one is required and the unit number to be booted is not zero)
followed by a carriage return. The two-character codes represent
bootstrap routine for specific device types. When the code is
entered, the routine that the code represents will be executed. If
the code is not recognized, a question mark (?) is printed,
followed by the $. The code to use for the SC02/C is "DM".

If the code selected represents a peripheral device boot routine,
then the controller will execute three more CPU tests and two
memory tests prior to executing the actual boot. The two memory
tests will check all available memory, but they require a minimum
of 8K bytes (0-17776) to operate.

Table 2-3
Bootstrap Routines

```
--------------------------------------------------------------------
XC   =   Execute CPU tests 7-9 only.
XM   =   Execute memory tests only.
OD   =   ODT Halt.  No routines executed.  A proceed (P)
         returns the program to the terminal input mode.
MTn  =   TM11 mag tape boot.  Can boot units 0-7.
DXn  =   RXV11 floppy disk boot.  Can boot units 0-1.
DKn  =   RK05 disk boot.  Can boot units 0-7.
RPn  =   RP02/3 disk boot.  Can boot units 0-7.
DMn  =   RK06/7 disk boot.  Can boot units 0-7.
DBn  =   RM02/3/5 disk boot.  Can boot units 0-7.
DRn  =   RP04/5/6 disk boot.  Can boot units 0-7.
DYn  =   RX211/RX02 disk boot.  Can boot units 0-7.
DLn  =   RL01/02 disk boot. Can boot units 0-7.
--------------------------------------------------------------------
Note:    If "n" is not entered, a default unit number of 0 is
         assumed.
```

The following is a list of halt locations which the PROM program will execute should the boot be unsuccessful.

HALT Address	Reason for HALT
765320	Non-existent unit, unit not on-line and ready, controller ready equals zero
765612	Read Error, Disk Error aborted read
765674	Read failed to complete within time limit
773434	Failure in CPU test #7
773530	Failure in CPU test #8
773550, 773556, or 773604	Failure in CPU test #9
773730	Failure in Memory test #1
773760	Failure in Memory test #2

2.5.6.2 Auto-boot Sequence

The auto-boot sequence will automatically bootstrap the system without operator intervention when the system is powered up or when an external DCLO signal is generated.

The CPU enters the auto-boot sequence at location 765000. The LSI-11/23 CPU can be jumpered to start at location 765000 automatically. See paragraph 3.4.5.2.

After performing a memory test, the auto-boot program will first attempt to boot the system from an RK06/07. If none is present, it will look for an RP02/03. If there is no RP02/03, it will attempt to find an RL01/02. In all cases, the auto-boot program will only attempt to boot from drive zero.

If none of the above drives is present, the program will print the $ prompt and expect the operator to enter a device code as described in paragraph 2.5.6.1, above.

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This section describes the step-by-step procedure for installation of the SC02/A Disk Controller in an LSI-11 system. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the SC02, is covered in paragraph 3.1).

Emulex recommends that Section 3 be read in its entirety before installation is begun.

1. Inspect the SC02.

2. Prepare the disk drives.

3. Prepare the LSI-11.

4. Route the drive I/O cables.

5. Configure the SC02.

6. Install the SC02.

7. Run the diagnostics.

3.1 INSPECTION

A visual inspection of the board is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROMs should be examined carefully to ensure that they are firmly and completely seated in the sockets.

3.2 DISK DRIVE PREPARATION

3.2.1 Drive Placement

Uncrate and install the disk drives according to the manufacturer's instructions. Position and level the disk drives in their final places before beginning the installation of the SC02. This allows the I/O cable routing and length to be accurately judged. Place the drives side by side to make installation of the daisy-chained A Cable simpler.

3.2.2 Local/Remote

The LOCAL/REMOTE switch controls whether the drive can be powered up from the drive (local) or the controller (remote). Place the switch in the REMOTE position. With the LSI-11 powered down, press the START switch on the front panel of each of the drives (the START LED will light, but the drive will not spin up and

become ready). When the LSI-11 is powered up, the drives will spin up sequentially. This prevents the heavy current draw that would be caused if all of the drives were powered up at once. When in the remote mode the drives will power down when the LSI-11 is powered down. While the LSI-11 is powered ON, the drives may be powered up and down individually (to change disk media, for example) using the drive START switch.

3.2.3 Sectoring

See Appendix A, Configuration Selection, for the correct sector count settings for the disk drives in use. The exact method of entering the sector count differs from one drive manufacturer to another and the particular drive manual should be consulted for the exact procedure. A minimum of 576 bytes per sector are required for proper operation.

3.2.4 Address Selection

An ID plug in the range of 0-1 should be placed in the drive. Be careful that the drives do not have the same number. Some drives have their address selected by means of switches on one of the logic cards and do not use an ID plug.

3.3 SYSTEM PREPARATION

3.3.1 Powering Down the System

Power down the system and switch OFF the main AC breaker at the rear of the cabinet (the AC power indicator will remain lit). Slide the CPU out of the cabinet and remove the top cover. Tilt the card cage up to obtain access to the CPU and other modules.

3.4 CONTROLLER SETUP

Several configuration setups must be made on the controller before inserting it into the chassis. These are made by SW1, SW2 and SW3.

3.4.1 Controller Address Selection

All Q-Bus controllers have a block of several command and status registers through which the system can command and monitor the controller. The registers are addressed sequentially from a starting address assigned to that device type, in this case a disk controller.

The starting address for the controller's Q-Bus registers is selected by DIP switch SW3. A normal starting address of 776700 is obtained by placing switch SW3-3 in the ON position. An alternate address of 777440 is available by closing SW3-2. Both SW3-3 and SW3-2 should not be closed at the same time.

Fault/Activity
LED

SW1

J1   J2   J3

SW2   Configuration PROM

Emulation
PROMs

Bootstrap PROMs   Address PROM

$400/

SW3

22-Bit Addressing DIP

Jumpers ▪

Bus Terminator DIPs
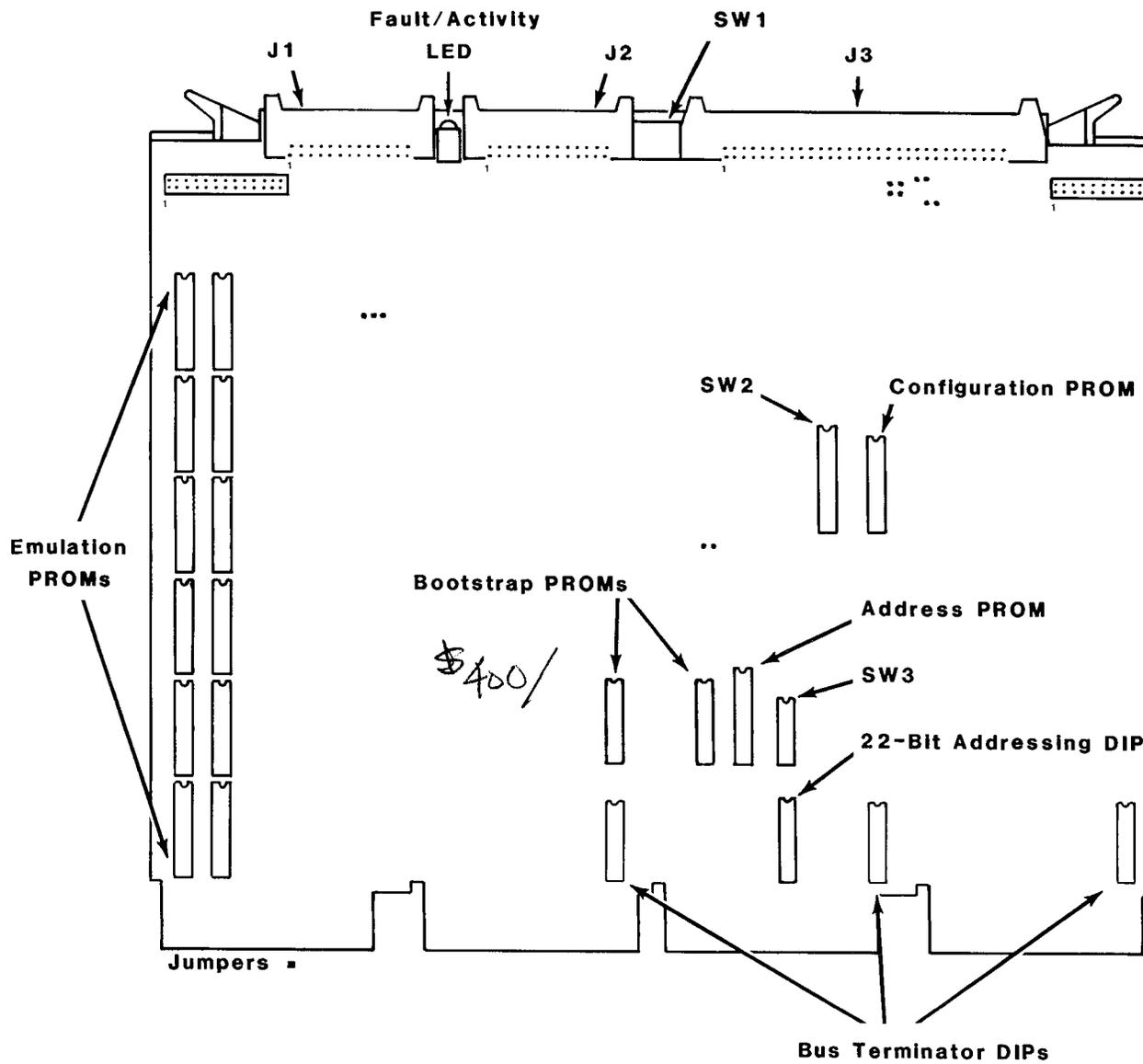
SC0201-0030

Figure 3-1 SC02 Controller Assembly

3.4.2 Interrupt Vector Address

Switches SW2-9 and SW2-10 allow the selection of one of four interrupt vectors. The normal interrupt vector of 254 is obtained by having both switches OFF. Other vectors are possible as shown in Table 3-1 below:

Table 3-1
Interrupt Vector Address Selection

SW2-10	SW2-9	VECTOR
OFF	OFF	254
OFF	ON	150
ON	OFF	370
ON	ON	374

3.4.3 Index and Sector Pulse Selection

The SC02 controller is designed to have the Index and Sector signals on the B Cable. The presence of the signals on the B Cable is not required.

3.4.4 Drive Configuration Selection

The phrase "drive configuration selection" describes the process that is used to configure the SC02 to use a particular type of physical disk drive to perform the RP02/03 emulation. That is, you have a particular set of physical disk drives. You must tell the controller what kind of physical disk drive you are going to use. On the SC02, switches SW2-1 through SW2-6 are used for that purpose.

For ease of manual maintenance the configuration table for the SC02 is contained in Appendix A.

3.4.5 Option Installation

There are a number of other SC02 options that can be selected by the user. These features are selected using the various switches and wire wrap jumpers located on the PCBA.

3.4.5.1 Q-Bus Terminator Option

To provide the equivalent of 120 ohms electrical termination to the

Q-Bus, DIP resistor networks are installed in U123, U129, and U135. These resistor packs provide a 180 ohm resistor connection to +5 volts and a 390 ohm resistor connection to ground on each Q-Bus line.

These three resistor networks may be ordered from Emulex or the customer may provide his own terminating resistor networks by using an equivalent part such as BOURNS P/N 4116R-003-181/391, or BECKMAN 898-5-r180/390, or CTS 761-5-R181/391.

WARNING

Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing an SC02 with the Q-Bus Terminator Option in such a system will damage the option ICs. Before installing the option confirm that there is neither positive or negative potential between lines BC1, BD1, BE1, BF1 and logic ground. If there is power on any of the above lines and you wish to use the terminator option, cut pins 1, 4, 5 and 14 of the IC in socket U129. An SC02 without the option will not be damaged if power is present on those lines.

3.4.5.2 Bootstrap PROM Option

The Bootstrap Option is a firmware routine executed by the CPU that loads the system memory with software that is stored on disk or tape. The option kit consists of two PROMs. Its Emulex part number is SC021301. See paragraph 2.5.6 for operating information.

To install the option, place the PROM labeled 015x in socket U101 and the PROM labeled 014x in socket U103.

The bootstrap option has two sections, standard console bootstrap and auto-boot. The standard console bootstrap routine is entered by the CPU at address 773000, DEC's conventional starting address. The auto boot sequence is entered at address 765000.

The LSI-11 and LSI-11/02 both require that power-up mode 2 be selected to take advantage of the standard console bootstrap option. This is done by installing jumper W6 and removing jumper W5 on the CPU PCBA. The configuration for both the LSI-11 and the LSI-11/02 is the same. The auto-boot routine is not available for these units.

The LSI-11/23 may be configured to take advantage of either the standard console boot or the auto-boot routines. This CPU also requires that power-up mode 2 be selected (install jumper W6 and remove jumper W5 on the CPU PCBA). The bootstrap starting address, however, is selected using jumpers W8 through W15. To select the standard console bootstrap routine install W8. This will cause the processor to default to starting address 773000. To use the auto-boot option, remove W8, W10 and W12; install W9, W11, W13, W14 and W15.

NOTE: Be sure to disable any other boot options prior to use of the Emulex boot option.

3.4.5.3 Line Time Clock Option

The Line Time Clock Option allows program control of the Line Time
Clock. This feature is enabled by closing (ON) SW3-5 on the SC02
PCBA. See paragraph 2.5.5 for programming instructions.

Before the LTC can be used, the CPU must be configured to enable
that feature. On the LSI-11 and LSI-11/02, remove jumper W3 (BEVNT
Line Enable). On the LSI-11/23, remove jumper W4 (BEVNT Line
Enable). The LTC switch on the front panel must also be ON.

When using the SC02 with the RSTS operating system, the Line Time
Clock Option must be OFF (SW3-5 = open). The CPU should be
configured to enable the option, however.

3.5 PHYSICAL INSTALLATION

3.5.1 Slot Selection

If the three optional Q-Bus terminator resistor networks are
installed, the SC02 should be installed in a quad slot such that it
provides the termination required at the end of the bus.

If the optional Q-Bus terminators are not installed, the SC02 may
be assigned to any desired slot since it uses the LSI four-level
interrupt scheme to perform distributed interrupt arbitration.

3.5.2 Mounting

The controller board should be plugged into the LSI-11 backplane
with components oriented in the same direction as the CPU and other
modules. Always insert and remove the boards with the computer
power OFF to avoid possible damage to the circuitry. Be sure that
the board is properly in the throat of the connector before
attempting to seat the board by means of the extractor handles.

3.6 CABLING

The subsystem cabling of the drives and controller is shown in
Figure 3-2.

3.6.1 A Cable

The 60-wire A cable should be plugged into J3 on the controller and
wired to the first drive. If more than one drive is used, it is
then daisy-chained to the other drives. The last drive on the A
cable must have a terminator installed. This part is available
from the drive manufacturer. The terminator is generally plugged
into one of two A cable connectors on the drive. In some cases, a
ground wire emerging from the terminator assembly will have to be
connected to the drive to provide a ground return for the resistors
in the terminator. Pin 1 of the board connector is on the left.
Pin 1 of the cable connector has a notch on the connector body to
identify it. Twist and flat cable will have brown-brown twist

DAISY CHAINED SYSTEM

Figure 3-2 Cabling Diagram
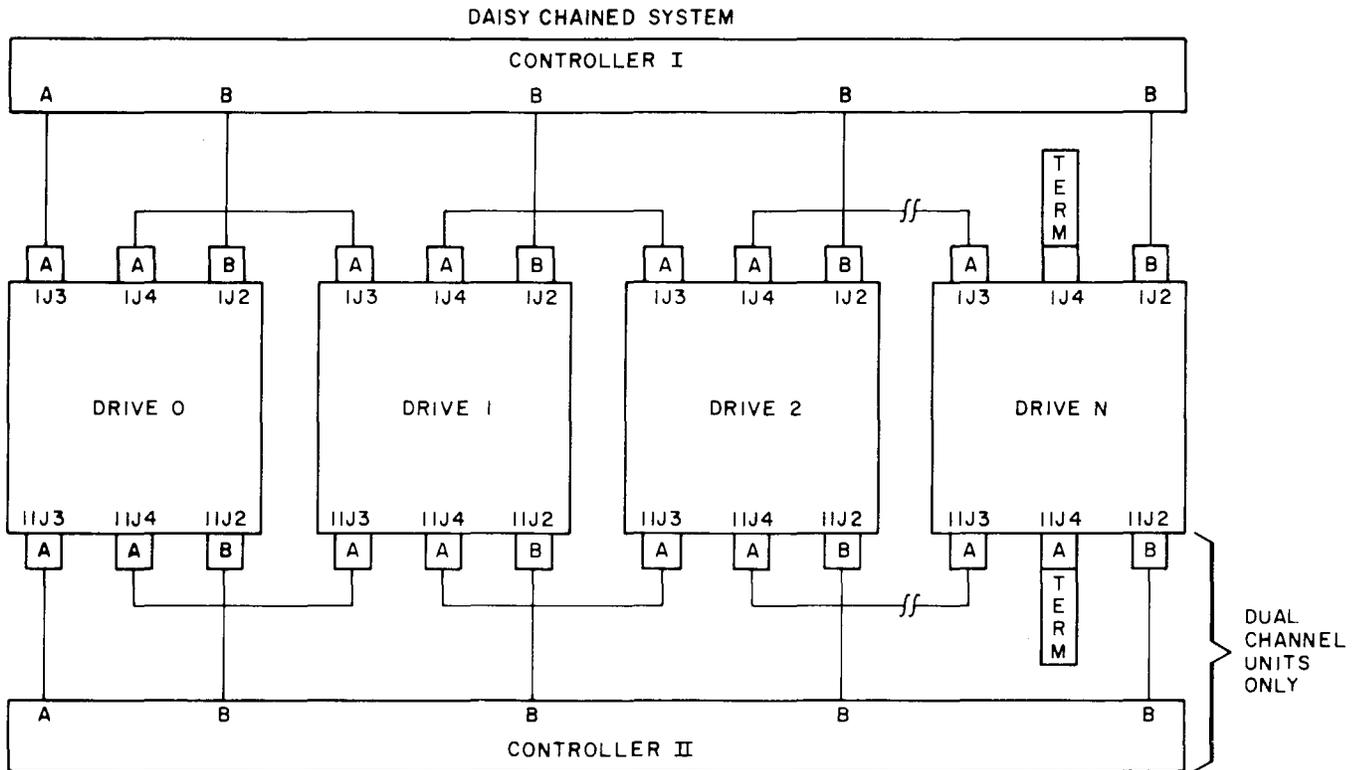
NOTES:
   1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
   2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET

SC0201-0000

followed by red-brown twist on the pin 1 edge of the cable. The cable will normally egress to the rear of the controller.

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.

3.6.2 B Cable

Each drive must have a 26-wire B Cable wired from the drive to one of the B ports of the controller. It makes no difference which B port connection is used by a drive. No external terminators are used with the B Cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe.

NOTE: Observe the same caution on connector reversal given in paragraph 3.6.1.

3.6.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

3.7 TESTING

3.7.1 Self-Test

When power is applied to the CPU, the controller automatically executes a built-in self test. This self test is not executed with every bus INIT but only on powering up. If the self test has been executed successfully, the LED on the top edge of the controller board will be OFF or flashing. The LED flashes when the controller cannot properly address at least one drive after successfully executing its self test. This will occur if the A and B Cables are not properly plugged in, a drive is not powered up with a code plug, or two drives have an identical code plug. If the LED is ON steadily the controller did not pass its self test and the controller cannot be addressed from the CPU.

3.7.2 Register Examination

After powering up the CPU and noting that the LED indicator is not ON steadily, a quick check should be made to ensure that the controller registers can be read from the computer console. The Control Status Register (RPCS) 776714 will contain 000200 if the controller is ready. To determine the on line status of the selected drive check the Device Status Register (RPDS) 776710 (see paragraph 4.2). If the CPU has a console emulator all the registers of the controller should be examined.

3.7.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing headers and zero data in all sectors of the disk. This format does not verify the data or headers and does not write a Bad Sector File on the last track of the last cylinder.

If the drive is on line, the formatting is carried out as follows:

1. Turn ON the hardware format enable switch SW1-4.

OR:

Format enable can also be done by writing a 177777 into
RPSH (776702) after Step 2 and before Step 3 instead of
turning ON SW1-4. This procedure sets a temporary flag.
The Write Header command (see Step 3) must be given
immediately after setting the enable flag.

2. Perform a controller clear by depositing 000001 into the
   Control Status Register (RPCS 776714).

3. To initiate a format, it is necessary to set the Mode bit
   (12) and the Header bit (11) to one in the RPCS. In
   addition, the desired logical drive number must be placed
   in bits 8, 9 and 10 of the RPCS and the Write function
   (bits 1, 2 and 3) plus the Go bit (0) must also be
   deposited in RPCS. The appropriate numbers to deposit for
   each logical drive are listed below.

LOGICAL DR.	DEPOSIT
0	014003
1	014403
2	015003
3	015403
4	016003
5	016403
6	017003
7	017403

3.7.4 Diagnostics

See Appendix C for patches to existing DEC RP02/RP03 diagnostics.
Emulex Corporation provides a diagnostic set that is specifically
designed to test the SC02/A controller.

BLANK

Table 4-1 summarizes the Controller's Register Set. A detailed description of each of the registers follows the table. The bus addresses that are listed are the standard addresses. Alternate addresses can be selected.

Table 4-1
Summary of SC02/A Registers

Bus Address	Register
776700	# Sectors Read Counter Low (RPSL)
776702	# Sectors Read Counter High (RPSH)
777704	# Sectors Corrected Counter (RPSC)
776706	# Sectors Uncorrected Counter (RPSU)
776710	Device Status Register (RPDS)
776712	Error Register (RPER)
776714	Control Status Register (RPCS)
776716	Word Count (RPWC)
776720	Bus Address (RPBA)
776722	Cylinder Address (RPCA)
776724	Disk Address (RPDA)
776726	Physical Address 1 (RPA1)
776730	Physical Address 2 (RPA2)
776732	Physical Address 3 (RPA3)
776734	Current Cylinder Address (RPCC)
776736	Data Buffer (RPDB)

4.1 SECTOR READ COUNTERS 776700-776706

RPSL - 776700: Contains the low order 16 bits of the number-of-sectors-read counter.

RPSH - 776702: Contains the high order 16 bits of the number-of-sectors-read counter.

RPSC - 776704: Contains the number of sectors read that were in error and corrected.

RPSU - 776706: Contains the number of sectors read that were in error and either not corrected or uncorrectable.

All four counters are read-write registers. None are reset by INIT or the RESET function. In addition, if a 177777 is written into RPSH, the write is ignored and a software "format enable" flag is set instead. If the next instruction executed is a Write Header

command, the entire disk pack will be formatted. (See Section 5 for further details.) These registers may be written into with both word and byte ops.

4.2 DEVICE STATUS REGISTER (RPDS) 776710

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OCYL	ONL	T3	HNF	SKE	SIP	FLT	WPT	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

The Device Status Register (RPDS) holds the current state of the selected drive and the Attention signals from each of the eight logical drives. The Attention bits are read/clear and, as such, can be selectively cleared by writing a one in the desired bit location(s). The other bits of RPDS are read-only. A drive is selected via bits <10:08> of RPCS.

On-Cylinder (OCYL) - Bit 15

This bit is set after a successful head load (on cylinder). It is reset during any Seek operation and set again after the Seek is completed if no Seek Error exists.

On-Line (ONL) - Bit 14

The selected drive exists and is up to speed.

T03 (T3) - Bit 13

This bit is a one if the selected drive is an RP03. This bit is a zero for RP02 emulations.

Header Not Found (HNF) - Bit 12

The selected drive has completed three full revolutions without locating the addressed sector. This bit is reset at the start of any operation.

Seek Error (SKE) - Bit 11

This bit is set if a Seek Error is detected at the completion of Seek for the selected unit.

Seek in Progress (SIP) - Bit 10

Set if the selected unit is currently executing a Seek or Home. This bit is reset at the completion of the Seek or Home.

Fault (FLT) - Bit 09

The selected unit has detected a fault condition within the drive and is prohibiting all operations. This bit is reset manually in the drive, and by a Home command (if possible).

Write Protected (WPT) - Bit 08

This bit is set when the Write Protect switch on the selected drive is set.

Attention Active 7-0 (ATA7-ATA0) - Bits <07:00>

Attention is set by a drive when a Seek or Home is completed. OCYL will be set after a successful Seek, and SKE will be set after an incomplete Seek. All Attention bits are cleared by INIT or the RESET function. Implied and mid-transfer Seeks do not set Attention bits.

4.3 ERROR REGISTER (RPER)   776712

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WPV	FUV	NXC	NXT	NXS	PGE	HRE	MER	MPE	ECH	DCK	TME	WCE	NXM	EPE	DKE

The Error Register (RPER) contains all error conditions generated within the controller. RPER is a read-only register. This register is cleared at the writing of the GO bit in RPCS, by INIT or by a RESET function.

Write Protect Violation (WPV) - Bit 15

Disk Write operation was attempted when WPT was true.

File Unsafe Violation (FUV) - Bit 14

Disk operation was attempted when FLT was true.

Non-Existent Cylinder (NXC) - Bit 13

Disk operation was attempted when the content of the Cylinder Address Register was not within range.

Non-Existent Track (NXT) - Bit 12

Disk operation was attempted when the content of the Track Address portion of the RPDA Register was not within range.

Non-Existent Sector (NXS) - Bit 11

Disk operation was attempted when the content of the Sector Address portion of the RPDA Register was not within range.

Program Error (PGE) - Bit 10

A Data Transfer operation was attempted with the content of RPWC equal to zero; an operation was attempted on an off-line drive or

while another instruction was still in progress (RDY equals zero).
Also set if a Write Header command is attempted with the format
enable flag/switch OFF.

Header Read Error (HRE) - Bit 09

CRC error was detected in a sector's header.

Mode Error (MER) - Bit 08

A header operation was attempted while the MDE bit in RPCS is
reset. Both HDR and MDE must be set.

Memory Parity Error (MPE) - Bit 07

A Parity Error was detected during a DMA read from memory.

ECC Hard Error (ECH) - Bit 06

Used in conjunction with bit 05 to indicate that the data read was
not correctable and a correction attempt was made.

Data Check (DCK) - Bit 05

Calculated ECC does not compare with that read from the disk, and
either the data was not correctable or no correction was attempted.

Timing Error (TME) - Bit 04

Data field sync character not found or 256 data words not found.

Write Check Error (WCE) - Bit 03

Data read from the disk pack does not compare with data read from
memory during a Write Check operation.

Non-Existent Memory (NXM) - Bit 02

More than 10 us was required to complete a DMA operation.

End of Pack Error (EPE) - Bit 01

Data Transfer (read or write) was attempted across the end of the
last sector of the pack.

Disk Error (DKE) - Bit 00

OR condition of Header Not Found (HNF) and Seek Error (SKE).

4.4 CONTROL STATUS REGISTER (RPCS) 776714

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	HE	AIE	MDE	HDR	US2	US1	US0	RDY	IDE	A17	A16	F2	F1	F0	GO

Error (ERR) - Bit 15

OR of all errors. This is a read-only bit.

Hard Error (HE) - Bit 14

OR of all errors except data errors. This is a read-only bit.

Attention Interrupt Enable (AIE) - Bit 13

Causes the controller to set an interrupt request whenever any
logical unit sets its ATA bit. This bit is cleared at the
completion of the interrupt. Also cleared by INIT or RESET
function; this is a read/write bit.

Mode (MDE) - Bit 12

Not used except that if bit 11 is set, this bit must also be set
for diagnostic compatibility. This is a read/write bit; cleared by
INIT or RESET function.

Header (HDR) - Bit 11

The function in the Function Field is a Header operation. This is
a read/write bit; cleared by INIT or RESET function.

Unit Select (US2-US0) - Bits <10:08>

Specify the logical drive which is to be the subject of any
controller action. These are read/write bits; cleared by INIT or
RESET function. Note that the number of units that can be operated
upon varies by drive types and number.

Ready (RDY) - Bit 07

When set indicates that the controller is in a condition to accept
and execute a new operation.

Interrupt On Done (Error) Enable (IDE) - Bit 06

Causes the controller to raise an interrupt request when a disk
operation is complete or if an error occurs. This is a read/write
bit; cleared by INIT or RESET function. Not cleared at the
completion of an interrupt.

Memory Extended Address (A17, A16) - Bits <05:04>

Specifies the 32K-word bank of memory used during Data Transfers. These are read/write bits; cleared by INIT or RESET function.

Function Bits (F2-F0) - Bits <03:01>

Specify the operation to be performed. These functions are described in detail in Section 5. These are read/write bits; cleared by INIT or RESET function.

GO (GO) - Bit 00

Set from the bus, causes the controller to initiate the operation encoded in bits <03:01> of the RPCS. This write-only bit always reads as a zero.

4.5 WORD COUNT REGISTER (RPWC) 776716

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Two's Complement Word Count															
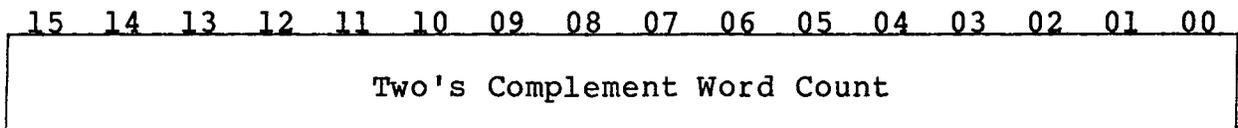
This register holds the two's complement of the number of data words to be transferred. This register is incremented by one after each transfer. Data Transfers are terminated when RPWC increments to zero. RPWC must be non-zero when a Data Transfer is initiated or a Programming Error (PGE) will be generated and no data will be transferred. RPWC can be written into with both word and byte ops.

4.6 BUS ADDRESS REGISTER (RPBA) 776720

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Bus Address															
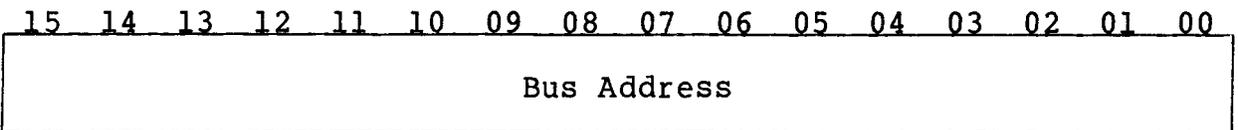
The Bus Address Register (RPBA) is loaded from the bus and specifies the bus address for Data Transfers during Read, Write, or Write Check operations. Transfers are always on a word basis; therefore, RPBA must be an even value. Incrementation by two takes place after a memory transaction has occurred. RPBA, therefore, is loaded with the address of the first location to be read from or written into. RPBA overflows into the extended address bits (bits 04 and 05) of RPCS. RPBA is a read/write register. The register is cleared by INIT or the RESET function. RPBA can be written into with both word and bytes ops.

4.7 CYLINDER ADDRESS REGISTER (RPCA) 776722

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Cylinder Address															
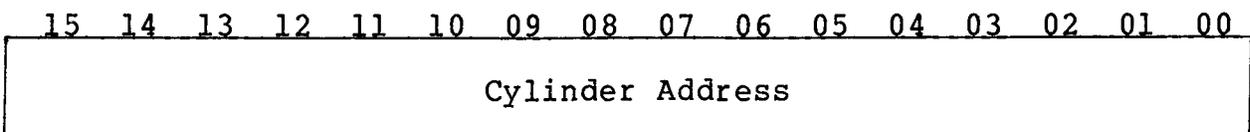
Bits <15:00> of the Cylinder Address Register (RPCA) are loaded from the bus and specify the disk cylinder for any disk operation. RPCA is a read/write register. It is cleared by INIT or the RESET function. RPCA can be written into with both word and byte ops.

4.8 DISK ADDRESS REGISTER (RPDA) 776724

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	Track Address				0	0	0	0	Sector Address			
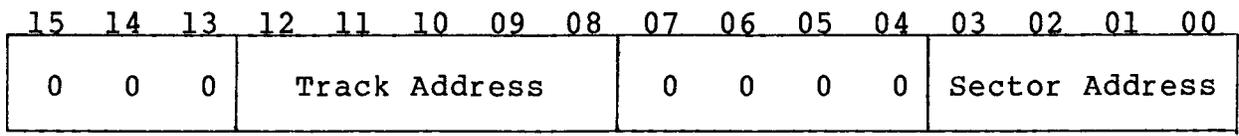
If logical-to-physical mapping is in effect, then bits <03:00> of the Disk Address Register (RPDA) are loaded from the bus and specify the disk sector address for any operation other than Seek or Home. Bits <03:00> are read/write bits and are cleared by INIT or the RESET function. Bits <07:04> are read-only bits which are read as zeros. Bits <12:08> are loaded from the bus to specify the track address for any disk operation. Bits <12:08> are read/write bits and are cleared by INIT or the RESET function. Bits <15:13> are read-only bits which are read as zeros.

If logical-to-physical mapping is not in effect, then bits <07:00> specify the sector address and <15:08> specify the track address. All bits are read/write bits, and all bits are cleared by INIT or the RESET function.

RPDA can be written into with both word and byte ops.

4.9 PHYSICAL ADDRESSES (RPA1-RPA3) 776726-776732

Whenever a seek is executed the physical address is saved in these three registers as follows:

        RPA1 - 776726:   Contains the physical cylinder number
        RPA2 - 776730:   Contains the physical track number
        RPA3 - 776732:   Contains the physical sector number

During multi-sector Data Transfers, RPA3 is incremented once after each sector is transferred. When this register increments past the maximum physical sector number for the drive, RPA2 and RPA1 are updated, RPA3 is cleared to zero, and a mid-transfer seek is executed.

RPA3 is a read-only register. RPA1 and RPA2 are also read-only registers with one qualification: attempting to write into RPA1 (any data) will replace the data currently in RPA1 with the maximum logical cylinder number for the selected unit. Similarly, any write into RPA2 will replace the data currently in RPA2 with the maximum track number (upper byte) and sector number (lower byte). These will be a 19 and a 9 respectively if logical-to-physical mapping is enabled. They will be actual limits per the configuration PROM if logical-to-physical mapping is disabled (in that case, RPM1 would also contain a physical address).

4.10 CURRENT CYLINDER ADDRESS (RPCC) 776734

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
						Current Cylinder Address									
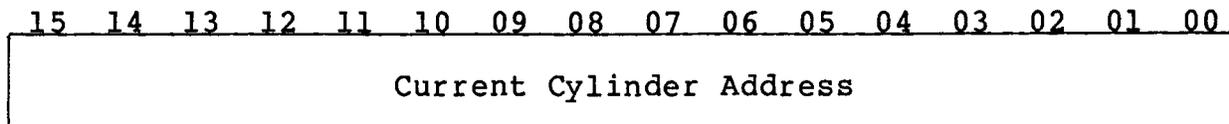
The Current Cylinder Address (RPCC) register stores the contents of the selected logical unit's current logical cylinder address. This is a Read-Only register.

4.11 DATA BUFFER (RPDB) 776736

This is a Read-Only register. If a write check error occurs it contains the data word from the disk that caused the error. A write to this register (any data) will reset the read error flag. See paragraph 2.5.4, Error Correction.

The controller provides the hardware for the execution of the eight
different functions. Home Seek and Seek are designated initiate
functions because their execution requires less than 30 us of
controller time after the command is issued. For this period, the
controller is busy. Initiate type commands require that the target
unit be selected. Although a Seek may require 500 ms. for
completion, a new unit number can be loaded into RPCS immediately.
Reset requires only ten microseconds of time. Execute
instructions, however, use all the time the controller requires for
completing the function. The controller, therefore, is busy for
the entire operation. Also, the target unit must be selected for
the entire operation and cannot be deselected for beginning
initiate-type functions.

Table 5-1
Function Codes

Function	Code	Type	Code + Go
Reset	0	Initiate	1
Seek	4	Initiate	11
Home Seek	6	Initiate	15
Write	1	Execute	3
Read	2	Execute	5
Write Check	3	Execute	7
Write	5	Execute	13
Read	7	Execute	17

Functions are selected by loading a three-bit field (F2-F0), of the
Controller Status Register (RPCS) with an octal number equal to the
function code. The function code and the GO bit may be written at
the same time. GO must be set before any action takes place.

5.1   INITIATE FUNCTIONS

5.1.1   Reset (1)

The Reset function is a controller clear operation. This function
is entered when the controller is initially cleared, or when the
Function field contents equal zero and the GO is set. This
operation requires ten microseconds of controller time and no
interrupt is generated upon completion. The RESET command can be
executed even if the controller is in the NOT READY state. (See
paragraph 2.5.1, Clearing the Controller)

5.1.2 Seek (11)

The Seek function can be executed by loading its octal code (4) into the Function field and setting GO. The Seek operation positions the heads of the selected unit as specified by the contents of the Cylinder Address and Disk Address registers. The unit Attention line, if it had been cleared previously, is raised when the Seek is completed. If the Seek is unsuccessful, the Seek Error status bit is set. At the successful completion of a Seek function, the on-cylinder status bit is set. While the Seek is in progress, the SIP bit (seek in progress) is set.

The Seek function allows the program to preposition the drive heads for the first block of data to be transferred. This prepositioning then results in a zero-cylinder seek (which usually takes less than 100 us) when the implied seek inherent within the Read, Write, and Write-Check functions occur.

On a multi-drive system, it is possible to initiate simultaneous Seek operations on several drives. The first drive to complete the Seek operation and respond by raising the Attention signal will cause an interrupt only if the Attention Interrupt Enable (AIE) bit has been set.

The programmer usually expects to be interrupted at the completion of any Seek operation, and sets the AIE bit accordingly. Because the Attention bits for each of the drives are effectively ORed, when any drive raises the Attention signal, an interrupt is generated. At the completion of the interrupt, the AIE bit is cleared by the controller, thus inhibiting further interrupts during the Data Transfer which normally follows. When the AIE bit is enabled again by the program, any remaining or new Attention bits initiate another interrupt and again clear AIE. In this way, each Attention can be handled individually or they can be handled collectively.

5.1.3 Home Seek (15)

The Home Seek function is executed by loading its function code (6) into the Function field and setting GO. The Home Seek function recovers the head position after a Seek Error. When this function is completed, the heads are placed at cylinder zero and Unit Attention is set along with ON-CYLINDER. This command does not alter RPCA or RPDA. A Home Seek should never cause a Seek Error. If it does, the drive requires maintenance. A fault clear is also issued to the drive. While the Home is in progress, the SIP bit is set.

5.2 EXECUTE FUNCTIONS

5.2.1 Write (3)

The Write function includes a Seek to the starting disk address (cylinder and track). This function is executed by loading its

octal code (1) into the Function field and setting GO. WRITE transfers data from the CPU memory to the disk drive beginning with the memory location specified by the Bus Address Register. Each data word transferred increments the Bus address by two and Word Count by one. The content of the RPWC at the beginning of the transfer determines the number of data words to be transferred. When the RPWC overflows, Data Transfers cease on the Q-Bus and the remainder of the present sector (if any) is filled with zeros. If RPWC is equal to zero when this function is executed, the write is aborted and a programming error (PGE) is indicated.

When this operation is performed, if the Data Transfer is sufficiently large enough to cause the heads to reposition to the next cylinder, the controller executes a mid-transfer Seek before continuing with the operation.

5.2.2 Read (5)

The Read function includes a Seek to the starting disk address (cylinder and track). This function is executed by loading its octal code (2) into the Function field and setting GO. READ transfers data from the disk drive to the CPU beginning with the memory location specified by the Bus Address register. Each data word transferred increments the Bus Address by two and Word Count by one. The content of the RPWC at the beginning of the transfer determines the number of data words to be transferred. When the RPWC overflows, Data Transfers stop. The remainder of the present sector is retrieved and the ECC checked before RDY is set. If RPWC equals zero when this function is executed, the read is aborted and a programming error (PGE) is indicated.

When this operation is performed, if the Data Transfer is sufficiently large enough to cause the heads to reposition to the next cylinder, the controller executes a mid-transfer Seek before continuing with the operation.

5.2.3 Write Check (7)

The Write Check function includes a Seek to the starting disk address (cylinder and track). This function is executed by loading its octal code (3) into the Function Field and setting GO. The Write Check command is a combination of the Write and Read functions. Data words are transferred from CPU memory to the controller and simultaneously read from the disk drive and transferred to the controller. In the controller, the two words are compared. Discrepancies set the WCE error status bit and terminate the operation. Data remains unchanged both in memory and on the disk. If an error occurs, RPBA points to the memory location that follows the one that caused the error, and the RPDB register contains the disk data that caused the error. RPDA points to the sector that caused the error. If RPWC equals zero when this function is executed, the function is aborted and a programming error (PGE) is indicated.

When this operation is performed, if the Data Transfer is sufficiently large enough to cause the heads to reposition to the next cylinder, the controller executes a mid-transfer Seek before continuing the operation.

5.2.4 Write (13)

This Write function is identical to the other (Function equals one).

5.2.5 Read (17)

This Read function is identical to the other (Function equals two).

5.3 READ HEADER

This is a dummy command that is included for diagnostic compatibility only. A Read Header command consists of a Read command with bits HDR and MDE in RPCS set. Headers are not actually read from the disk, but are created by microcode in RP02/RP03 format. Note that the controller uses a different, more efficient, format for the disk headers. An RP02/RP03 header consists of three words with the following format:

    Word #1 = All zeros

    Word #2 = Cylinder address in bits <15:06>, track address in
                bits <05:01>, and a zero in bit 00.

    Word #3 = Sector address in bits <03:00>.

Note that in an unmapped system with track addresses of six bits or more, the track address overflows into the cylinder address. Nothing is done to prevent this. If the contents of RPWC indicates more than 255 words are to be read by this function, then the read is aborted and a programming error (PGE) is indicated.

There is no method provided within this controller to read actual disk headers. The user's software must include a method for bypassing unusable sectors in non-error free media.

5.4 WRITE HEADER

With one exception, this command is illegal and results in a programming error (PGE). A Write Header command consists of a Write command with bits HDR and MDE in RPCS set. The exception is a pack format. The controller contains a formatting routine within the microcode. This format routine is executed via a Write Header command with the Format Enable flag set. The flag is set in one of two ways: first, by having the Format Enable switch ON (SW1-4) when the Write Header command is issued, and second, by writing a 177777 into RPSH (see paragraph 4.1) just prior to issuing the Write Header command. The second method of setting the flag is temporary. The flag is reset when RDY goes from zero to one.

The actual format operation is done on the entire logical unit selected via RPCS bits <10:08>. Headers are created and written, and data fields of all zeros are created and written. Sectors are interleaved in a 3-to-1 organization to optimize system throughput. In mapped mode, any unused sectors on the last physical track are formatted with illegal headers and zero data fields so that they are not accidentally used during Read or Write operations.

5.5 Data Transfer ERRORS

If any error occurs which terminates a Data Transfer operation, then RPCA and RPDA contains the address of the sector that caused the error. During a Read operation, the data from the sector that caused the Read error is transferred to memory regardless of whether the data is correctable or not. Data Transfer errors include all DMA errors and all disk Read/Write errors.

Since Data Transfer errors result in RPCA and RPDA addressing the sector that caused the error, and since a Home Seek does not affect either RPCA or RPDA, error recovery routines do not have to reload either RPCA or RPDA. Note that a Read error that occurs during a Write Check results in a status that shows both a Read error and a Write Check error.

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APPENDIX A

SC02/A CONFIGURATION AND OPTION SELECTION

A.1 INTRODUCTION

To allow the user of the SC02/A the greatest amount of flexibility
in selecting disk drives for his system, the SC02/A supports a wide
variety of disk types and offers a number of other user selectable
options. This appendix is designed as a quick reference to the
various switches and jumpers which make this flexibility possible.
For more detailed information about user selectable options see the
Installation chapter in this manual.

A.2 DRIVE CONFIGURATION

The SC02/A unit is capable of controlling a wide variety of disk
drives of various sizes and types. The various drives that are
supported are defined by the Configuration PROM. Table A-1 is a
list of the drive types and sizes that are supported. The user may
choose between the available options by means of configuration
switch SW2. The correct switch settings for each of the various
configurations are given in Table A-2.

A.2.1 Single Drive Installations

To find the configuration setting that is suitable for your single
disk drive installation, use the following process. Note that all
configurations require that the drive be hard sectored as noted in
the Sec column of Table A-1. See the manufacturer's drive
installation manual for instructions.

      1. Locate your drive type and size in Table A-1. Note down
          the configuration code(s) assigned to your drive. Note
          also the cylinder (Cyl), track (Trk) and sector (Sec)
          figures for the drive.

      2. Find the configuration number for your drive in the CONF
          NO. column of Table A-2. If there is more than one number
          for an individual drive, start with the smallest. Note
          that for each configuration row, specifications are given
          for two physical drives, Unit 0 and 1.

      3. When you find the proper row, compare the Physical Drive
          cylinder, track and sector figures for Unit 0 in Table A-2
          with the numbers you noted down from Table A-1. They must
          match. If they do not, go on to the next higher
          configuration number, etc, until you find a match.

A-1

4. When you find a match, set the Configuration Switches (SW2) as indicated in Table A-2. (Generally, there is more than one match. In such cases, look at the Logical Unit and Drive Type column for each configuration where a match was found. Choose the Logical configuration you like best, and set the Configurations Switches accordingly.)

A.2.2 Dual Drive Installations (same type drive)

To find the configuration setting that is suitable for your dual disk drive installation (drives same size and type), use the following process. Note that all configurations require that the drives both be hard sectored as noted in the Sec column of Table A-1. See the manufacturer's drive installation manual for instructions.

1. Locate your drive type and size in Table A-1. Note down the configuration code(s) assigned to your drives. Note also the cylinder (Cyl), track (Trk) and sector (Sec) figures for the drives.

2. Find the configuration number for your drives in the CONF NO. column of Table A-2. If more than one number was given for the drives, start with the smallest. Note that for each configuration row, specifications are given for two physical drives, Unit 0 and 1. The physical cylinder, track and sector numbers for Unit 0 and 1 in that row must match. If they do not, go on to the next configuration number.

3. When you find the proper row, compare the Physical Drive cylinder, track and sector figures for both Unit 0 and Unit 1 in Table A-2 with the numbers you noted down from Table A-1. They must match. If they do not, go on to the next higher configuration number, etc, until you find a match.

4. When you find a match, set the Configuration Switches (SW2) as indicated in Table A-2. (Generally, there is more than one match. In such cases, look at the Logical Unit and Drive Type column for each configuration where a match was found. Choose the Logical configuration you like best, and set the Configuration Switches accordingly.)

A.2.3 Dual Drive Installations (different drive types)

To find the configuration settings that are suitable for your dual disk drive installation (different drive size and type), use the following process. Note that all configurations require that the drives both be hard sectored as noted in the Sec column of Table A-1. See the manufacturer's drive installation manual for instructions.

1. Locate your drive types and sizes in Table A-1. Note down the configuration code(s) assigned to each drive. Note also the cylinder (Cyl), track (Trk) and sector (Sec) figures for each drive.

2. Once you have located and noted your drive configuration codes, compare the codes for each drive to one another. There must be at least one match if that drive combination is supported. Note that for all configurations that support different drive sizes, the configuration code does not have a letter suffix.

3. Consult Table A-2. Find the configuration number that both drives have in common in the CONF NO. column. If more than one number was given for the drive, start with the smallest.

4. For each configuration row, specifications are given for two physical drives, Unit 0 and 1. The two sets of numbers will be different. Compare the physical cylinder, track and sector numbers for each unit with the corresponding numbers from Table A-1. The physical drive that matches the numbers for physical unit 0 becomes unit 0. The physical drive whose numbers match physical unit 1's becomes unit 1.

5. If there is more than one configuration supported, look at the Logical Unit and Drive Type column for each configuration where a match was found. Choose the Logical configuration you like best, and set the Configuration Switches (SW2) accordingly.

TABLE A-1
DRIVES SUPPORTED

Mfg. - Model		Cyl	Trk	Sec	Configurations
AMPEX	940	411	5	32	52
AMPEX	93160	1645	5	35	13
BALL	BD160	1645	5	35	13
BASF	6172	614	3	23	23
BASF	6173	614	5	23	24
CENTURY	T82	815	5	35	4,5,44
CENTURY	T82RM	823	5	35	4,5,6,11,44
CDC	9448-32	823	2	35	0,2
CDC	9448-64	823	4	35	1
CDC	9448-96	823	6	35	0
CDC	9448-96	823	6	32	3
CDC	9455	206	4	32	20
CDC	9762	823	5	35	4,5,6,11,44
CDC	9730-12	320	2	35	35

Mfg. -	Model	Cyl	Trk	Sec	Configurations
CDC	9730-24	320	4	35	34
CDC	9730-80	823	5	35	4,5,6,11,44
CDC	9730-160	823	10	35	7,10,11
FUJITSU	2311	589	4	34	25
FUJITSU	2312	589	7	34	26
FUJITSU	2284	823	10	34	41,42,43
KENNEDY	5300-70	700	5	35	4
KENNEDY	5300-70	700	5	32	36,40
KENNEDY	5300-80	823	5	35	4,5,6,11,44
MEMOREX	612-84	350	12	35	15
NISSEI	NP30-40	370	5	35	31
NISSEI	NP30-80	370	11	35	32
NISSEI	NP30-120	568	11	35	33
OKIDATA	3306	339	12	32	37,40
PRIAM	3350	561	3	32	12
PRIAM	3350	561	3	35	14
PRIAM	6650	1122	3	35	16
PRIAM	15450	1122	7	35	17
PRIAM	2050	525	3	23	21
PRIAM	3450	525	5	23	22
PRIAM	7050	1049	5	23	45,46
SLI	Sheyenne 3	656	5	19	27
SLI	Sheyenne 4	656	7	19	30

TABLE A-2
SC02/AX CONFIGURATION PROM 195   REV K[1]

CONF NO.	SW2- 6 5 4 3 2 1	Unit	Physical Cyl	Trk	Sec	Unit(s)	=	Dr Type	Cyl	Cap	Rev
0	O O O O O O	0	823	6	35	0,1,2,3,4,5	=	RP02	144	14.7	A
		1	823	2	35	6,7	=	RP02	144	14.7	A
1	O O O O O C	0	823	4	35	0,1,2,3	=	RP02	144	14.7	A
		1	823	4	35	4,5,6,7	=	RP02	144	14.7	A
2	O O O O C O	0	823	2	35	0,1	=	RP02	144	14.7	A
		1	823	2	35	2,3	=	RP02	144	14.7	A
3	O O O O C C	0	823	6	32	0,1,2,3,4,5	=	RP02	131	13.4	A
		1	823	2	32	6,7	=	RP02	131	13.4	A
4	O O O C O O	0	700	5	35	0,1,2	=	RP02	203	Std	A
		1	700	5	35	3,4,5	=	RP02	203	Std	A
5	O O O C O C	0	815	5	35	0,1,2	=	RP02	237	24.2	A
		1	815	5	35	3,4,5	=	RP02	237	24.2	A
6	O O O C C O	0	823	5	35	0	=	RP03	720	73.7	A
		1	823	5	35	1	=	RP03	720	73.7	A

[1]Must be used with SC02/A firmware Rev. B or above.

CONF NO.	SW2- 6	5	4	3	2	1	Unit	Physical Cyl	Trk	Sec	Unit(s)	=	Dr Type	Cyl	Cap	Rev
7	O	O	O	C	C	C	0	823	10	35	0,1,2	=	RP03	406	Std	A
							1	823	10	35	3,4,5	=	RP03	406	Std	A
10	O	O	C	O	O	O	0	823	10	35	0,1	=	RP03	720	73.7	A
							1	823	5	35	7	=	RP03	720	73.7	A
11	O	O	C	O	O	C	0	823	10	35	0,1,2,3,4,5,6	=	RP02	203	Std	F
							1	823	5	35	7	=	RP03	720	73.7	A
12	O	O	C	O	C	O	0	561	3	35	0	=	RP02	203	Std	A
							1	561	3	35	1	=	RP02	203	Std	A
13	O	O	C	O	C	C	0	1645	5	35	0,1,2,3,4,5,6	=	RP02	203	Std	A
							1	1645	5	35	7	=	RP03	1312	134	A
14	O	O	C	C	O	O	0	561	3	35	0	=	RP02	294	30.1	A
							1	561	3	35	1	=	RP02	294	30.1	A
15	O	O	C	C	O	C	0	350	12	35	0,1,2	=	RP02	245	25.0	A
							1	350	12	35	3,4,5	=	RP02	245	25.0	A
16	O	O	C	C	C	O	0	1122	3	35	0	=	RP03	589	60.3	A
							1	1122	3	35	1	=	RP03	589	60.3	A
17	O	O	C	C	C	C	0	1122	7	35	0	=	RP03	1312	134	B
							1	1122	7	35	1	=	RP03	1312	134	B
20	O	C	O	O	O	O	0	206	4	32	0,1	=	RP02	65	6.6	B
							1	206	4	32	2,3	=	RP02	65	6.6	B
21	O	C	O	O	O	C	0	525	3	23	0	=	RP02	181	18.5	A
							1	525	3	23	1	=	RP02	181	18.5	A
22	O	C	O	O	C	O	0	525	5	23	0	=	RP02	301	30.8	D
							1	525	5	23	1	=	RP02	301	30.8	D
23	O	C	O	O	C	C	0	614	3	23	0	=	RP02	211	21.6	A
							1	614	3	23	1	=	RP02	211	21.6	A
24	O	C	O	C	O	O	0	614	5	23	0	=	RP02	353	36.1	A
							1	614	5	23	1	=	RP02	353	36.1	A
25	O	C	O	C	O	C	0	589	4	34	0	=	RP02	400	40.9	B
							1	589	4	34	1	=	RP02	400	40.9	B
26	O	C	O	C	C	O	0	589	7	34	0	=	RP03	700	71.6	B
							1	589	7	34	1	=	RP03	700	71.6	B
27	O	C	O	C	C	C	0	656	5	19	0	=	RP02	311	31.8	A
							1	656	5	19	1	=	RP02	311	31.8	A
30	O	C	C	O	O	O	0	656	7	19	0	=	RP03	436	44.6	A
							1	656	7	19	1	=	RP03	436	44.6	A
31	O	C	C	O	O	C	0	370	5	35	0	=	RP02	323	33.0	B
							1	370	5	35	1	=	RP02	323	33.0	B
32	O	C	C	O	C	O	0	370	11	35	0,1,2	=	RP02	203	Std	D
							1	370	11	35	3,4,5	=	RP02	203	Std	D
33	O	C	C	O	C	C	0	568	11	35	0,1	=	RP03	497	50.8	D
							1	568	11	35	2,3	=	RP03	497	50.8	D
34	O	C	C	C	O	O	0	320	4	35	0	=	RP02	224	22.9	C
							1	320	4	35	0	=	RP02	224	22.9	C
35	O	C	C	C	O	C	0	320	2	35	0	=	RP02	112	11.4	C
							1	320	2	35	0	=	RP02	112	11.4	C
36	O	C	C	C	C	O	0	700	5	32	0	=	RP03	560	57.3	C
							1	700	5	32	0	=	RP03	560	57.3	C

CONF NO.	SW2- 6 5 4 3 2 1	Unit	Physical Cyl	Trk	Sec	Unit(s)	=	Dr Type	Cyl	Cap	Rev
37	O C C C C C	0	339	12	32	0,1,2	=	RP02	203	Std	E
		1	339	12	32	3,4,5	=	RP02	203	Std	E
40	C O O O O O	0	339	12	32	0,1,2	=	RP02	203	Std	E
		1	700	5	35	3,4,5	=	RP02	203	Std	E
41	C O O O O C	0	823	10	34	0,1	=	RP03	699	71.5	F
		1	823	10	34	6,7	=	RP03	699	71.5	F
42	C O O O C O	0	823	10	34	0,1,2	=	RP03	406	Std	F
		1	823	10	34	3,4,5	=	RP03	406	Std	F
43	C O O O C C	0	823	10	34	0,1,2,3,4,5	=	RP02	203	Std	F
		1	823	10	34	6,7	=	RP03	699	71.5	F
44	C O O C O O	0	823	5	35	0	=	RP03	406	Std	G
		1	823	5	35	1	=	RP03	406	Std	G
45	C O O C O C	0	525	5	23	0	=	RP03	602	61.6	G
		1	525	5	23	1	=	RP03	602	61.6	G
46	C O O C C O	0	525	5	23	0,1	=	RP02	301	30.8	G
		1	525	5	23	2,3	=	RP02	301	30.8	G
47	C O O C C C	0	624	4	32	0,1	=	RP02	199	20.4	K
		1	624	4	32	2,3	=	RP02	199	20.4	K
50	C O C O O O	0	1645	5	35	0	=	RP03	1439	147.3	H
		1	1645	5	35	1	=	RP03	1439	147.3	H
51	C O C O O C	0	823	10	35	0,1,2,3,4,5	=	RP02	203	Std	J
		1	823	5	35	6	=	RP03	720	73.7	J
52	C O C O C O	0	411	5	32	0	=	RP02	328	33.5	K
		1	411	5	32	1	=	RP02	328	33.5	K

NOTES: C = Closed (ON), O = Open (OFF)

A.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC02/A can be user selected. The functions of the switches that select those options are defined in Tables A-3, A-4 and A-5, below.

TABLE A-3
OPTION SWITCH SETTINGS

Option Sw	Open	Closed	Function
SW1-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW1-2			Not used[1]
SW1-3	Enable	Disable	ECC correction
SW1-4	Disable	Enable	Hardware disk format operation[2]

[1] All unused switches MUST BE OFF.

[2] See paragraph 3.7.3.

TABLE A-4
CONFIGURATION SWITCH SETTINGS

Config Sw	Open	Closed	Function
SW2-1			Drive Configuration[2]
SW2-2			Drive Configuration[2]
SW2-3			Drive Configuration[2]
SW2-4			Drive Configuration[2]
SW2-5			Drive Configuration[2]
SW2-6			Drive Configuration[2]
SW2-7	Enable	Disable	Physical to Logical Mapping
SW2-8			Not used[1]
SW2-9			Interrupt Vector Select[3]
SW2-10			Interrupt Vector Select[3]

[1]All unused switches MUST BE OFF.

[2]See TABLE A-2 for settings.

[3]See Table 3-1 for settings.

TABLE A-5
ADDRESS SWITCH SETTINGS

Address Sw	Open	Closed	Function
SW3-1			Not used[1]
SW3-2		777440	Alternate Unibus Address[3]
SW3-3		776700	Standard Unibus Address[3]
SW3-4	Disable	Enable	Boot PROM Option
SW3-5	Disable	Enable	Line Clock Option
SW3-6	Disable	Enable	1k Microcode Address Range (normally closed)

[1]All unused switches MUST BE OFF.

[3]Only one address may be selected. All other address
switches MUST BE OFF.

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APPENDIX B
Modifications to DEC Diagnostics

The following modifications to the existing DEC RP02/RP03 diagnostics will allow those diagnostics to be run on an Emulex SC02/A controller. The tests require logical unit 0 to be present before they will run.

A. MAINDEC-11-DZRPZ-C-D
   RP11E Drive Positioning Test   Sept 1977

Item	Location(s)	From	To
1.	3026-3046	12737, 312, 1236 5737, 1240, 1403 12737, 625, 1236	13700, 1266, 5060 4, 5060, 16 16037, 16, 1236
2.	3150-3166	12737, 200, 1676 5737, 1240, 1403 12737, 400, 1676	13700, 1266, 5060 4, 5060, 16, 16037 16, 1676
3.	6040	1002	240
4.	6314	1002	240
5.	6626	1002	240

Item	Explanation
1.	Self-sizes the test to the size of logical unit 0.
2.	Self-sizes one of the sub tests to the size of logical unit 0.
3.	Removes timing test 10.
4.	Removes timing test 11.
5.	Removes timing test 12.

Users who are running on an LSI or an LSI 11/2 must make the following patches to alter explicit PSW references.

Item	Location	From	To
1.	2742-2744	5037, 177776	106427, 0
2.	14040-14040	137, 1272, 177776	106437, 1272, 240
3.	14152-14154	5037, 177776	106427, 0
4.	14314-14316	5037, 177776	106427, 0
5.	14746-14750	5037, 177776	106427, 0
6.	15026-15030	5037, 177776	106427, 0
7.	15304-15306	5037, 177776	106427, 0
8.	15376-15400	5037, 177776	106427, 0
9.	15534-15536	5037, 177776	106427, 0
10.	16656-16660	5037, 177776	106427, 0
11.	17074-17076	5037, 177776	106427, 0

B. MAINDEC-11-DZRPY-C-D
    RP11E Functional Logic & Read/Write Test   Sept 1977

Item	Location(s)	From	To
1.	23050 23054-23056	24000, 5337, 23060	1000, 240, 5327
2.	4374-4404	12737, 312, 1210 5737, 1304, 1403	4, 5064, 16, 16437 16, 1210
3.	7210-7212 7222	112737, 5, 12737	12737, 14005, 404
4.	7316	1002	240
5.	10170 10234-10240 10252 10256 10320 10340	300 52737, 14000, 2502 23546 23240 14000 1366	40 52764, 14000, 4 23240 23546 4000 1011
6.	10376	1002	240

7.	10750	4737	424
	11254	1004	405
8.	14636	1002	240
9.	15400	1002	240
10.	15632	1002	240
11.	22324	20	0
12.	24004-24046	12737, 117230, 1244	5037, 1244, 5037
		5037, 1246, 5000	1246, 12700, 310
		113700, 2500	63737, 1210, 1244
		13607	
		1360, 1304, 1404	5537, 1246, 5300
		6337, 1244, 6137	1371, 402
		1246	

Item   Explanation

 1.   Corrects a programming error and shortens a stall
       subroutine to speed up the test.

 2.   Self-sizes the test to the size of logical unit 0.

 3.   Alters a "PGE" error test.

 4.   Removes a write header test.

 5.   Changes a seek test to use cylinder 32 instead of 192, and
       corrects two programming errors.

 6.   Removes a non-existent memory test which will not run on
       an LSI 11/23.

 7.   Alters a sector addressing test to remove the write header
       command and the SOT counter check.

 8.   Removes power fail test 15.

 9.   Removes head alignment test 16.

10.   Removes control panel switch test 17.

11.   Disables memory management 22-bit mode.

12.   Self-sizes test 14 to the size of logical unit 0.

Users who are running on an LSI-11 or an LSI-11/2 must make the following patches to alter explicit PSW references.

Item	Locations	From	To
1.	4276-4300	5037, 177776	106427. 0
2.	4360-4362	5037, 177776	106427, 0
3.	15342-15344	5037, 177776	106427, 0

C. MAINDEC-11-DZRP2-B-D
    RP11E Disk Pack Formatter   May 1976

Item	Location(s)	From	To
1.	206	1314	1304
2.	212	1324	1304
3.	216	1334	1304
4.	2256-2270	104401, 11435 4737, 10242 4737, 7642	4737, 7642 12764, 177777 177772, 240
5.	2364 2402 2424	740 7266 2450	732 2236 2236
6.	7664	5	20

Item	Explanation
1.	Changes a 204 start to a 200 start.
2.	Changes a 210 start to a 200 start.
3.	Changes a 214 start to a 200 start.
4.	Removes a switch-enable question/response from the hardware format portion of the test.
5.	Removes the header check portion of the test, and loops back to the hardware format portion of the test.
6.	Increases a "home" command stall timer to accommodate slower drives.

Users who are running on an LSI-11 or an LSI-11/2 must make the following patches to alter explicit PSW references.

Item	Locations	From	To
1.	2242-2244	5037, 177776	106427, 0
2.	2330-2332	5037, 177776	106427, 0
3.	2434-2436	5037, 177776	106427, 0
4.	2450-2456	12737, 340, 177776	106427, 200, 240

D. MAINDEC-11-DZRP1-B-D
    RP11E Multi-Drive Exerciser Programer   May 1976

Item	Location(s)	From	To
1.	4316	1010	240
2.	4352	1414	1421
3.	2766-3006	12737, 312, 1256 5737, 21122, 1403 12737, 625, 1256	13704, 1216, 5064 4, 5064, 16 16437, 16, 1256
4.	21746 23066	112764 112764	152764 152764
5.	22746 22756	1430 1024	1431 1025

Item	Explanation
1.	A modification per a DEC "MAINDEC Change Notice".
2.	A modification per a DEC "MAINDEC Change Notice", but altered to the correct value.
3.	Self-sizes the test to the size of logical unit 0.
4.	Alters a "MOVB" op code to a "BISB" of code so that an error printout will show the drive number loaded into RPCS.
5.	Programming errors. Fixes two incorrect branch addresses.

Users who are running on an LSI-11 or an LSI-11/2 must make the following patches to alter explicit PSW references.

Item	Location(s)	From	To
1.	2234-2236	5037, 177776	106427, 0
2.	2360-2362	5037, 177776	106427, 0
3.	2666-2670	5037, 177776	106427, 0
4.	2700-2702	5037, 177776	106427, 0
5.	3500-3504	12737, 200, 177776	106427, 0, 240
6.	3526-3530	5037, 177776	106427, 0
7.	10152	200	0
8.	21316-21320	13746, 177776	106746, 240
9.	21322-21326	13737, 1222, 177776	106437, 1222, 240
10.	21424-21426	5037, 177776	106427, 0
11.	21434-21436	12637, 177776	106426, 240
12.	21566-21570	13746, 177776	1067