SC21/B1 SC21/V1

SC21/BE SC21/BF SC21/BM

(RM02/RM03/RM05 COMPATIBLE)

DISK CONTROLLER

TECHNICAL MANUAL

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INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC21/B1, SC21/BF, SC21/BE, SC21/BM and SC21/V1 Disk Controllers. In addition, this manual provides diagnostic and application information.

1.2 OVERVIEW

1.2.1 General Description

The SC21/B Disk Controller is a one-board imbedded controller for PDP-11 and VAX-11 computers manufactured by Digital Equipment Corporation. This controller can be used to interface any large disk having a Storage Module Drive (SMD) interface. The SC21/B series of controllers is capable of emulating the DEC Massbus disk subsystems. The SC21/B1 emulates the DEC RJM02 disk subsystem while the SC21/B2 emulates the DEC RJP06 disk subsystem. These controllers are capable of operating with disk drives having different characteristics from those used in the DEC disk subsystems. The SC21/B controllers provide the capability of operating with a mixture of disks having storage capacity of 5-600 megabytes. The SC21/B controllers provide capabilities beyond those of the companion two-board SC11/B controllers.

1.2.2 Controller Models

The various SC21 models performing RM02/RM03/RM05 emulations are described below. They can be identified by their top level assembly numbers, located on the IC at location U117.

SC21/B1 - Basic RM emulation with dual port and single logical drive per physical drive. Top level assembly number SC2110201-B1X (X is the revision level of the firmware)

SC21/BE - Same as SC21/B1 except that it provides sector interleaving, transparent ECC correction and expanded transfer counts. Top level assembly number SC2110201-BEX (X is the revision level of the firmware).

SC21/BF - Same as SC21/B1 except that it provides for fixed head support for Winchester type disk drives. Top level assemply number SC2110201-BFX (X is the revision level of the firmware).

SC21/BM - Same as SC21/B1 except that it allows for two logical drives per physical drive. Top level assembly number SC2110201-BMX (X is the revision level of the firmware).

SC21/V1 - Same as SC21/B1 except that it performs four word NPR bursts optimized for the Unibus Adapter (UBA) of the VAX-11/780. Top level assembly number SC2110101-V1X (X is the revision level of the firmware).

1.3 FEATURES

1.3.1 Microprocessor Design

The SC21/B design incorporates a unique 16-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various sizes.

1.3.2 Packaging

The SC21/B is constructed on a single hex-size multi-layer PC board which is designed to plug directly into a PDP-11, VAX-11 chassis or an expansion chassis. No cabling is required between the computer and the disk controller. The controller obtains its power from the chassis in which it is mounted.

1.3.3 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk data logic. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is operational. If the controller fails the self-test, it leaves the Fault LED on and the controller cannot be addressed from the CPU.

1.3.4 Buffering

The controller contains a 1K x 16 high-speed RAM buffer used to store the device registers of the controller and drive being emulated and three or two sectors of data buffering. Because of the buffering and the strategies used to employ it, data late situations on the Unibus are not possible.

1.3.5 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) capable of correcting single error bursts of up to 11 bits in length and detecting bursts of longer length. The controller determines the location of the error and the error pattern and then passes this information back to the PDP-11 or VAX-11 which actually performs the correction of the erroneous data. The SC21/BE performs the correction of the data in the controller before the data is sent to memory. A 16-bit CRC is employed with the header of every sector.

1.3.6 Option and Configuration Switches

Two ten-pole DIP switches are used to configure the controller for various disk sizes, Unibus addresses and certain firmware options. It is possible to select one of 32 possible combinations of disk characteristics for the four drives which can be handled by the controller, including mixtures of disk sizes and drive type codes.

1.3.7 Get Characteristics Capability

Since the SC21/B1 series of controllers can handle a number of different drive sizes, a capability has been provided to read out the maximum cylinder, maximum track, and maximum sector address, as well as the selected drive type code. This is useful for self configuring software such as used with the Emulex supplied driver for VAX/VMS.

1.3.8 Dual Port Capability

The controller can operate with disk drives having dual port capability which allows a second controller to have access to the drive on a priority basis.

1.3.9 Bootstrap PROM

A bootstrap PROM is supplied with the SC21/V1. This PROM is for use in the VAX-11/750. The PROM is designated UM boot (EMULEX #287B).

1.4 FUNCTIONAL COMPATABILITY

1.4.1 Media Compatability

The SC21/B1 is media compatible with the DEC RM02/RM03 packs when using a CDC 9762 drive or equivalent and with the DEC RM05 when using a CDC 9766 drive or equivalent.

1.4.2 Disk Mapping

For an 80 MB disk drive, the mapping is the same as the DEC RM02. When drives of different sizes are used, the mapping is done in a straightforward manner with only the number of heads and/or number of cylinders being varied. In all cases, the disk drive is configured for 32 sectors.

1.4.3 Diagnostics

The controller executes the following standard DEC RM02/RM03 diagnostics on PDP-11 computers:

ZRMA - Formatter
ZRMB - Performance Exerciser
ZRMC - Functional Controller, Part I *
ZRMD - Functional Controller, Part II
ZRME - Functional Controller, Part III *
ZRMF - Extended Drive Test
ZRMI - Drive Compatibility Test

The diagnostics marked with an asterisk require certain patches to bypass unsupported maintenance functions. All diagnostics require patches to run with drive sizes other than that of a standard RM02/RM03.

DEC supports the RM02, RM03 or RM05 disk subsystems on the VAX line of computers through RH750 or RH780 Massbus Adaptors. Consequently, there are no DEC diagnostics for the support of the SC21/V1 which does not provide a Massbus emulation. Emulex provides diagnostics support for the SC21/V1. The part numbers for the Emulex diagnostics are VX9960401 (750) and VX9960501 (780). See the literature supplied with the diagnostic for installation and operation instructions.

1.4.4 Operating Systems

The SC21/B1 series of controllers are compatible with DEC operating systems without modification when operating with an 80 MB disk drive having 823 cylinders and 5 tracks. Patches are required to the operating system when operating with other than standard size disks. These patches numerically redefine the logical drive capacity to the operating system and generally do not involve modification to program instructions.

The RM02 disk drives are not supported by all DEC operating systems, in particular, RT11.

The VAX/VMS Operating System supports the RM02, RM03 or RM05 disk subsystems through RH750 or RH780 Massbus Adaptors. Consequently, VMS does not support the SC21/V1 which is not a Massbus emulation. Emulex provides a VMS software driver that allows the SC21/V1 to be used on both the VAX 750 and 780. The Emulex part numbers are VD9960401 (750) and VD9960501 (780). The software is supplied with its own operation and installation manual.

Table 1-1

GENERAL SPECIFICATIONS

FUNCTIONAL	
Emulation	DEC RM02, RM03, and RM05
Media Compatability	DEC RM02, RM03, and RM05 when using appropriate disk drives.
Drive Interface	SMD
Drive Ports	4
Error Control	32-bit ECC for data and 16-bit CRC for headers. Correction of single data error burst of up to 11 bits.
Sector Size	256 words (512 bytes)
Sectors/Track	32
Tracks/Cylinder	Selectable for each drive.
Cylinders/Drive	Selectable for each drive.
Drive Type Code	Selectable for each drive.
Computer Interface	SPC Unibus
Unibus Address	
Standard	776700 (20 Registers)
Alternates	776600 (20 Registers) 776300 (20 Registers) 776100 (20 Registers) 775300 (20 Registers)
Vector Address	
Standard	254
Alternates	150, 370, 374
/BM Alternates	150, 370, 374, 354, 224, 270, 274
Priority Level	BR5
Data Buffering	3 Sectors (768 words) for SC21/B1, SC21/V1 and SC21/BE 2 Sectors (512 words) for SC21/BF and SC21/BM
Data Transfer	High speed NPR operation.

Table 1-1 (cont'd)

Self-Test	Extensive internal self-test on powering up.
Indicators	Activity and Fault LEDs
DESIGN	High-speed bipolar microprocessor using 2901-bit-slice components.
PHYSICAL	
Packaging	One DEC hex-size board.
Mounting	Any SPC slot in CPU or expansion box.
Connectors	One 60-pin A cable flat connector and four 26-pin B cable connectors. (Flat cable type.)
Electrical	
Unibus Interface	DEC approved line drivers and receivers.
Drive Interfaces	Differential line drivers and receivers. A cable accumulative length to 100 feet. B cable length to 50 feet.
Power	+5 v, 8 Amp. max. -15 v, 1 Amp. max.

2.1 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC21/B1 controller is shown in Figure 2-1. The controller is organized around a 16-bit high-speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with four 2901-bit slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with twelve 2K x 4 PROMs.

The controller incorporates a 1K x 16 high-speed RAM buffer which is used to store the controller's device registers and three sectors (768 words) of data buffering.

The A Cable Register (ACR) provides the storage of all A cable signals going to the disk drives. Status inputs from the selected drive are testable by the microprocessor.

Serial data from the drive is converted into 16-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data access from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC Shift Register is used to generate and check the ECC for the data field. The same register is also used in a 16-bit CRC mode for the headers. The actual ECC polynomial operation is done independently of the microprocessor, but the determination of the error position and error pattern is done under the control of the microprocessor.

A configuration PROM is a source to the data bus. This PROM configures the maximum cylinder address, maximum track address and drive type code for each of the logical drives.

The Unibus interface consists of a 16-bit bi-directional set of data lines and an 18-bit set of address lines. The Unibus interface is used for programmed I/O, CPU interrupts, and data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all NPR operations and transfers data between the Unibus data lines and the buffer.

2.2 PHYSICAL DESCRIPTION

The SC21/B1 controller consists of a single hex-size board which plugs directly into a PDP-11 chassis. Figure 2-2 shows the board.

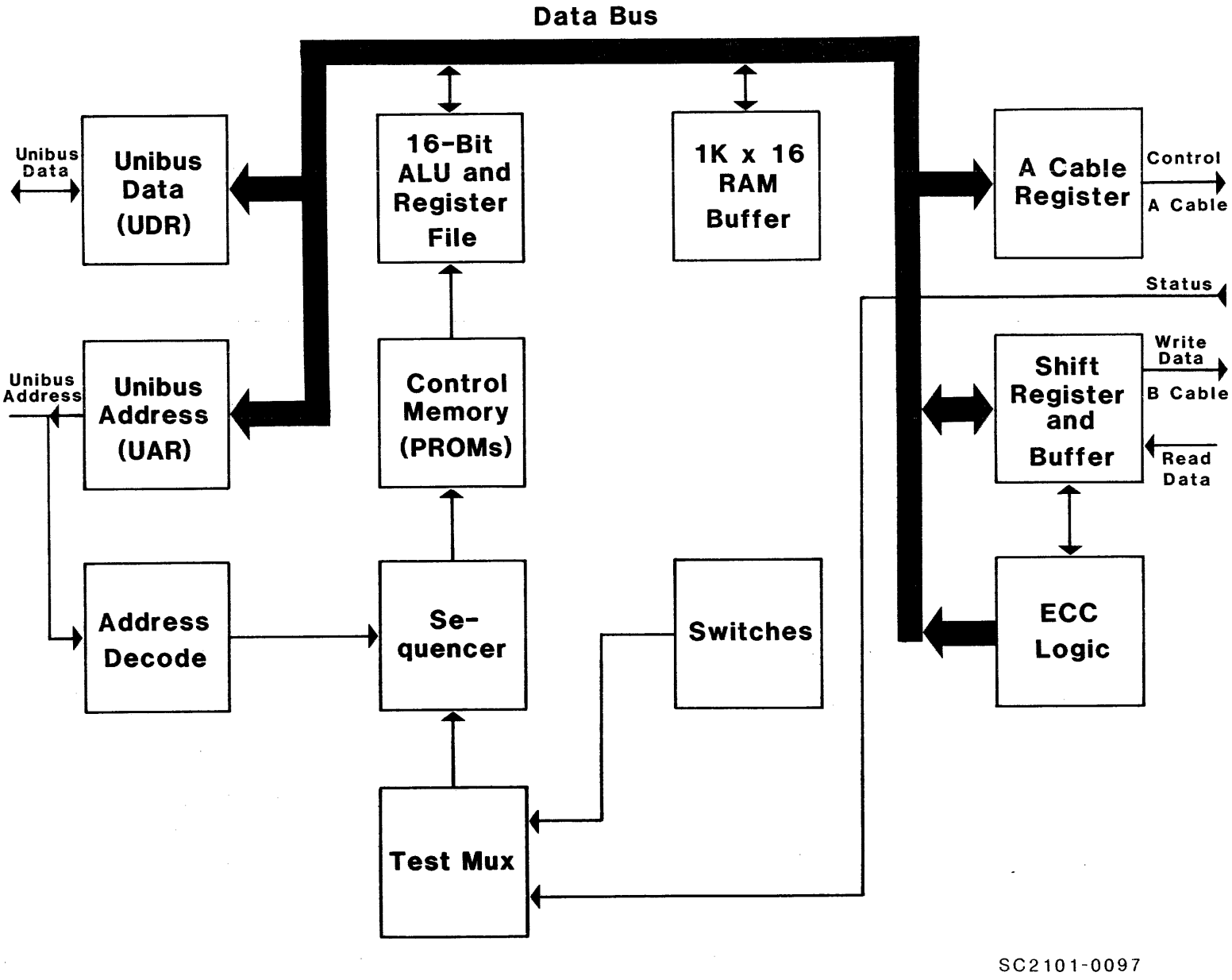
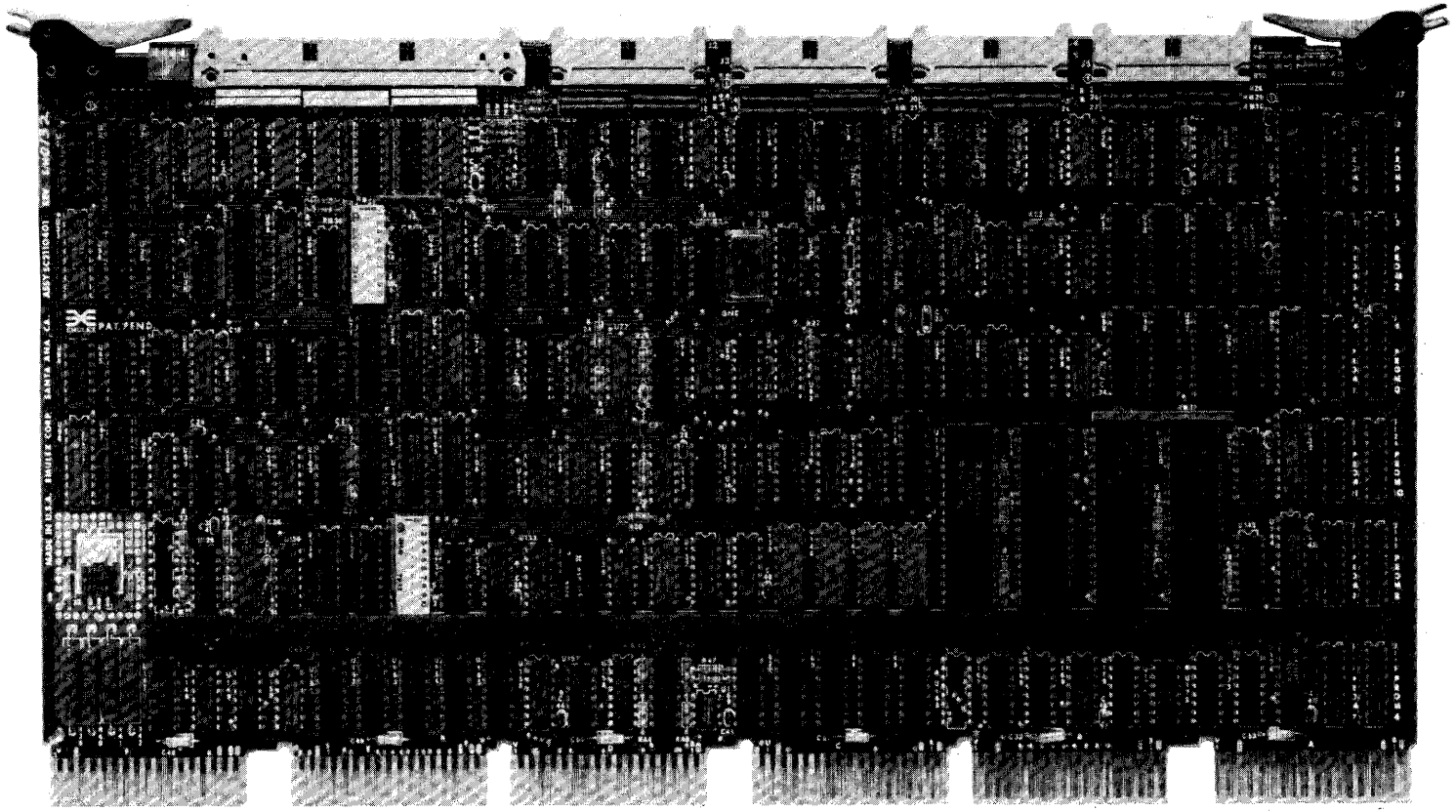


Figure 2-1 SC21 Block Diagram



SC2101-0098

Figure 2-2. SC21 Disk Controller

2.2.1 Connectors

2.2.1.1 A Cable Connector

The 60-pin flat cable connector labeled J1 at the top edge of the board is for the A cable which daisy-chains to all the drives for control and status. Pin 1 is located on the left side of the connector.

2.2.1.2 B Cable Connector

The four 26-pin flat cable connectors labeled J2, J3, J4, and J5 are for the radial B cables to each of four physical drives which may be attached to the controller. Pin 1 is located on the left side of the connector. The four B cable ports are all identical and any drive may be plugged into any connector.

2.2.1.3 Test Connectors

Connectors J6 and J7 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.2 Switches

The two ten-pole DIP switches labeled SW1 and SW2 are used to configure the controller. SW1 provides firmware options, while SW2 provides selection of controller address and drive configurations.

2.2.3 Indicators

There are two LED indicators mounted between the connectors at the top of the board. They have the following use:

Fault - Indicates unsuccessful self-test execution. A flashing LED indicates successful self-test, but unable to find any drive connected and/or powered-up.

Activity - Indicates disk read or write activity.

2.2.4 PROMs

There are twelve PROM sockets, used for the control memory, located along the right edge of the board. The sockets are labeled PROM 0 through PROM 11 in a discontinuous physical order. The numbers on the top of the PROM ICs are Emulex part numbers, which identify the unique pattern of the PROM. When inserting PROMs in the board, the ID numbers are placed in the same sequence as the PROM numbers on the board beside each socket.

There are two more PROMs in the lower left portion of the board at U129 and U130. The socket at U129 is for the drive configuration PROM. The socket at U130 is for the address PROM.

2.3 INTERFACES

2.3.1 Disk Interface

The controller's disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD interface and is compatible with the electrical and timing characteristics of such disk drives.

The following paragraphs define the electrical interface and the recommended cables.

2.3.1.1 Drivers and Receivers

The drivers for the A and B cables are MC3453, which are equivalent to the 75110A. The receivers are MC3450 quad differential receivers, which are equivalent to 75108 receivers. The lines of the A cable are terminated with 82 ohms to ground. The lines of the B cable are terminated with 56 ohms to ground.

2.3.1.2 A Cable

The 60-conductor A cable is daisy-chained to all drives and terminated at the last drive. The signals in this cable, along with their function when the control tag (Tag 3) is asserted, are listed in Table 2-1. The A cable should be 30 twisted pair flat cable with an impedance of 100 ohms and an accumulative length of no greater than 100 feet.

2.3.1.3 B Cable

The 26-conductor B cable is radial to all drives and contains the data and clock signals. The signals and grounds in this cable are listed in Table 2-1. The B cable should be 26 conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length must not be greater than 50 feet.

2.3.2 Unibus Interface

The controller interfaces to the PDP-11 or VAX-11/780 Unibus via a Small Peripheral Controller (SPC) connector. The Unibus consists of 18 address lines and 16 bi-directional data lines, plus control signals for data and interrupt vector address transfer and for becoming bus master. The signal connections of the controller to the Unibus are shown in Table 2-2.

2.3.2.1 BR (Interrupt) Priority Level

The controller is hardwired for BR5. The other three Bus Grant signals are jumpered through.

Table 2-1
Disk Drive Connections

Pins Lo/Hi	Signal	(Tag 3 Function)	From/To
A Cable:			
22,52	Unit Select Tag		To
23,53	Unit Select bit 0		To
24,54	Unit Select bit 1		To
26,56	Unit Select bit 2		To
27,57	Unit Select bit 3		To
1,31	Tag 1		To
2,32	Tag 2		To
3,33	Tag 3		To
4,34	Bit 0	(Write Gate)	To
5,35	Bit 1	(Read Gate)	To
6,36	Bit 2	(Servo Offset Plus)	To
7,37	Bit 3	(Servo Offset Minus)	To
8,38	Bit 4	(Fault Clear)	To
9,39	Bit 5	(AM Enable)	To
10,40	Bit 6	(Return to Zero)	To
11,41	Bit 7	(Data Strobe Early)	To
12,42	Bit 8	(Data Strobe Late)	To
13,43	Bit 9	(Release)	To
30,60	Bit 10		To
14,44	Open Cable Detect		To
15,45	Fault		From
16,46	Seek Error		From
17,47	On Cylinder		From
18,48	Index		From
19,49	Unit Ready		From
20,50	Address Mark Found		From
21,51	Busy (dual port only)		From
25,55	Sector		From
28,58	Write Protected		From
29	Power Sequence Hold		To
59	Power Sequence Pick		To
B Cable:			
8,20	Write Data		To
6,19	Write Clock		To
2,14	Servo Clock		From
3,16	Read Data		From
5,17	Read Clock		From
10,23	Seek End		From
22,9	Unit Selected		From
12,24	Index		From
13,26	Sector		From

Table 2-2
SPC Unibus Connections

Column	C		D		E		F	
Pin	1	2	1	2	1	2	1	2
A	NPGIN	+5V		+5V		+5V		+5V
B	NPGOUT					-15V		-15V
C	PA	GND		GND	A12	GND		GND
D		D15		BR7	A17	A15	BBSY	
E		D14		BR6	MSYN	A16		
F		D13		BR5	A02	C1		
H	D11	D12		BR4	A01	A00		
J		D10			SSYN	C0	NPR	
K		D09		BG7IN	A14	A13		
L		D08	INIT	BG7OUT	A11			
M		D07		BG6IN			INTR	
N	DCLO	D04		BG6OUT		A08		
P		D05		BG5IN	A10	A07		
R		D01		BG5OUT	A09			
S	PB	D00		BG4IN				
T	GND	D03	GND	BG4OUT	GND		GND	SACK
U		D02			A06	A04		
V	ACLO	D06			A05	A03		

2.3.2.2 Register Address

The register address and the number of registers assigned to the controller are decoded by a PROM at U130. The selections available are determined by configuration switch SW2 as discussed in paragraph 3.4.3.

2.3.2.3 DCLO and INIT Signals

The DCLO and INIT signals both perform a controller clear. The self-test is performed only if DCLO has been asserted.

2.4 DISK FORMAT

2.4.1 Disk Organization

The SC21/B1 handles only one logical RM drive per physical drive. The number of cylinders and tracks for each drive can be configured by the Configuration PROM. The number of sectors is always 32. The SC21/BF handles two logical RM drives per physical drive: one on the moving-head portion of the drive and one on the fixed-head portion of the drive. The number of sectors and tracks is the same for both. Only the number of cylinders differs. See Section 2.7 for.

Each of the four physical disk drives on the SC21/BM may have up to two logical drives mapped on them. The size of the emulated disk drive is proportional to the size of the drive being emulated.

2.4.2 Sector Organization

Figure 2-3 shows the sector format used by the controller. Each track of 20,160 bytes is divided into 32 sectors of 630 bytes. The four byte header is preceeded by a preamble of 30 bytes ending in the sync byte and is followed by a two byte CRC. The 256-word data field is preceded by a preamble of 20 bytes ending in the sync byte, and is followed by four bytes of ECC. This format is compatible with that of the DEC RM02/RM03.

If the actual size of the useful data information is less than 256 words, the remainder of the data field will be filled with 0's until 256 words have been written. During disk formatting procedures, each data track is located and recorded with header information by means of the Write Header and Data command. A disk pack should be formatted and the format verified before any real data is written on it. Once formatted, individual or groups of sectors should not be reformatted unless absolutely necessary.

2.4.3 Header

2.4.3.1 Header Description

Figure 2-4 shows the header format, which consists of the following three words:

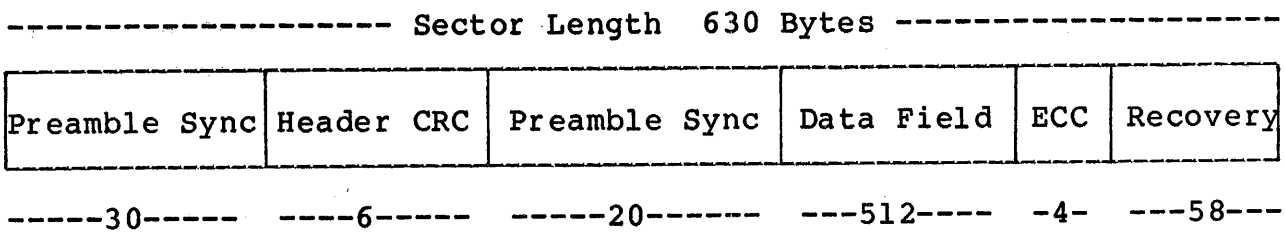
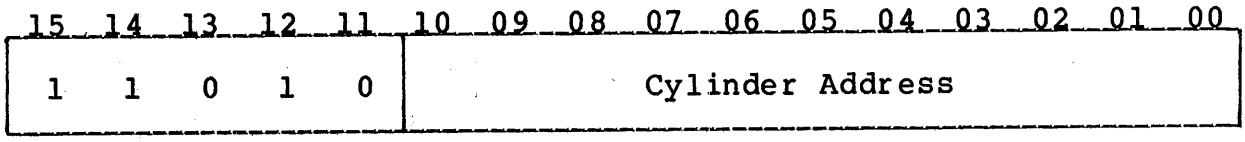
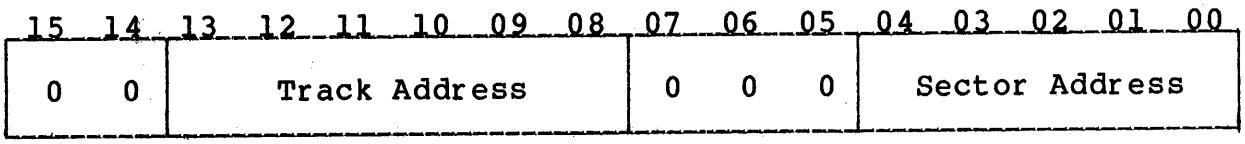


Figure 2-3 Sector Format

Header Word 1:



Header Word 2:



Header Word 3:

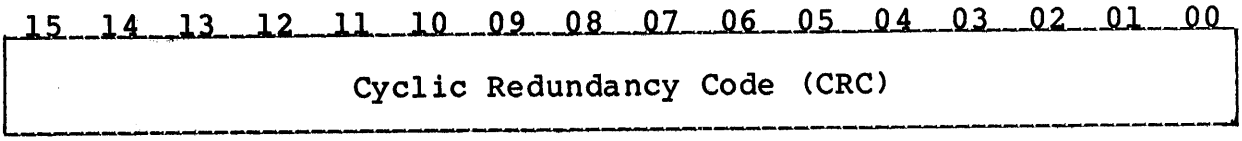


Figure 2-4 Header Format

Word One -

This word contains the cylinder address. It contains a 1 in bit 12 to identify 16-bit format to the software and 1-bits in bit positions 14 and 15 to identify a good sector.

Word Two -

The low-order five bits of this word contain the sector address. Each track on the drive contains 32 sectors. The least significant six bits of the upper byte of this word contain the track address.

Word Three -

This is the CRC word which is generated and checked by the controller logic. This word is not available to the software.

2.4.3.2 Header Field Handling

After the drive reports that it is on cylinder, the controller locates the desired sector by means of the sector counters. The sector counters for each drive are maintained in the controller. The controller compares the first two words of the header against the desired track, sector and cylinder and then checks the CRC word for errors. An error in the header field is indicated by turning on the appropriate error bit in the error register (format error, header compare error, bad sector error or CRC error). A header error is only valid when the sector count field of the RMLA register and the sector field of the RMDA have already matched. It is immaterial where a CRC error occurs in the header field since the controller cannot determine its location in the field. However, software may read the header to memory by means of a Read Header and Data command. The header compare may be inhibited by setting the HCI bit in the RMOF register.

2.5 GENERAL PROGRAMMING INFORMATION

2.5.1 Clearing the Controller

The controller has the following clearing methods:

a. Controller Clear - Controller Clear is performed by writing a 1-bit into the CLR bit (bit 05 of RMCS2) or Unibus INIT. This causes the following to be cleared:

- RMCS1 bits <00:06>, <08:09>, <12:15>; RMCS2 bits <00:05>, <07:15>; RMBA bits <00:15>. Sets RMCS2 bit 06 and RMCS1 bit 07.

- In all drives: RMER1; RMER2; RMDA; RMAS ATA bit; RMEC2; RMDS ATA, ERR and LST bits; RMMR1 bits <00:02>, <04:15>. Sets bit 03 of RMMR1.

b. Error Clear - The Error Clear is performed by writing a 1-bit into the TRE bit (bit 14 of RMCS1). This causes a clearing of RMCS1 bits 13 and 14, and bits <08:15> of RMCS2. Clears the SC bit (bit 15 of RMCS1) if RMAS=0.

c. Drive Clear - The Drive Clear is a command. (Code 11.) This causes the following registers in the drive selected by U2-U0 to be cleared:

- RMER1; RMER2; RMAS ATA bit; RMEC2; RMDS ATA and ERR bits; RMMR1 bits <00:02>, <04:15>. Sets bit 03 of RMMR1.

2.5.2 Interrupt Conditions

The controller generates an interrupt on the following conditions:

a. Upon termination of data transfer if interrupt enable is set when the controller becomes ready.

b. Upon assertion of attention or occurrence of a controller error (SC being set) while the controller is not busy and the interrupt enable is set.

c. When the program writes 1 into IE and RDY at the same time. Note that this can be done by Read-Modify-Write instructions (BIS, BIC, etc.) which set the IE bit.

2.5.3 Termination of Data Transfers

A data transfer which has been successfully started may terminate in the following ways:

a. Normal Termination - Word count overflows to 0 and the controller becomes ready at the end of the current sector.

b. Controller Error - An error occurs in the RMCS2 register bits <08:15>. Any of these errors sets TRE which terminates the data transfer immediately and makes the controller ready.

c. Drive Error - The ERR bit in the RMDS register and at least one bit in an RMER1 or RMER2 register are set. TRE is also set and the controller becomes ready. The ATA for the drive doing the data transfer becomes asserted.

d. Program-Caused Abort - By performing a Controller Clear or a RESET instruction, the program can cause an abort of any operation. Status and error information is lost when this is done, and the controller and drive become ready immediately.

2.5.4 Ready Bits

RDY is the ready indicator for the controller. When RDY = 1, the controller is ready to accept a data transfer command. RDY is reset when the controller is doing a data transfer command. DRY is the ready indicator for the selected drive and is the complement of the drive's GO bit. To successfully initiate a data transfer command, both of these bits must be asserted. However, a non-data transfer command (Search, Drive Clear) may be issued to a drive at any time DRY is asserted regardless of the state of the RDY bit.

When a data transfer command is successfully initiated, both RDY and DRY become negated. When a non-data transfer command is successfully initiated, only DRY bit becomes negated.

The assertion of RDY after the execution of a data transfer command will not occur until the DRY bit is set and the controller is done. RDY is asserted on the completion of the last memory cycle (or at the time of an abort condition) and the last disk transfer.

If any command other than Drive Clear is issued to a drive which has ERR asserted, the command is ignored by the drive. If a Data Transfer command is issued to a drive which has ERR asserted, the drive does not execute the command and the missed transfer error (MXF, bit 09 in RMCS2 register) is set.

2.5.5 SC21/BE Special Features

Revisions B and above of the SC21/BE emulation incorporate the following three special features: transparent ECC correction, RMWC equals sector count and sector interleave mode. General information on these features is contained in the paragraphs below. See Section 5 for more information.

2.5.5.1 Transparent ECC Correction

When this feature is enabled, correctable ECC errors are fixed within the controller before the data is transferred to the memory on a Read or Read Header and Data operation.

2.5.5.2 RMWC Equals Sector Count

When this feature is enabled, the contents of RMWC contain the number of sectors to be transferred, rather than the number of words. It is valid for all operations except Write Checks.

2.5.5.3 Sector Interleave Mode

The SC21/BE emulation has an option switch (SW3-4) which allows the user to run in sector interleave mode. The interleave mode is not automatic; to enable this feature the user must enable (CLOSE) SW3-4 and write a formatter program which interleaves sectors in the sequence the user desires.

The sector interleave mode causes some commands to be treated in a different manner. The following two paragraphs describe the manner in which the altered commands function in the interleave mode.

The controller will ignore the sector counter when searching for a sector's header. If within three revolutions no match is found, a header compare error (HCE bit 07 in RMER1) is flagged, and no data is transferred. This causes a Read Header and Data Command to be treated like a Read Data Command (see paragraph 5.1.5) and a Write Check Header and Data to be treated like a Write Check Data (see paragraph 5.1.1).

If the user attempts a Read Command or a Write Data operation with the header compare inhibit bit (HCI bit 10 in RMOF) set, the controller will commence reading with sector zero if the low byte of RMDA is zero, or any other sector if the low byte of RMDA is not a zero. Sectors are read in sequence as long as the controller is not required to wait for a buffer to become available. If the controller is required to wait for a buffer, the next sector transferred will be whichever one rotates into position as soon as a buffer becomes available.

2.6 DUAL CONTROLLER OPERATION

SMD drives may be equipped with a dual port option which provides the capability for two controllers (generally on separate computers) to access the drive. The SC21/B controller supports this type of operation as a standard feature. Most of the dual port functions of the DEC controller being emulated are supported, and those which are not should be transparent to a properly written dual port driver.

2.6.1 Dual Port Drives

The two drive ports are known as Channel I and Channel II. Each channel has a disable switch which disables the port and prevents the computer from having access to it. Access to the drive in dual port operation is switched back and forth between the two controllers under program control of the two computers involved in a manner described in the following sections. Table 2-3 summarizes the register responses in dual port operation.

2.6.2 Unseized State

The unseized state is when the drive is not connected to either controller. The CPU must issue a request for the controller to seize the drive. This request is done in one of the following ways:

a. Writing into any drive register, including read-only registers.

b. Writing a one-bit into the drive's ATA bit in RMAS. The bit does not have to be set.

2.6.3 Seized State

The drive is seized when it is logically connected to one of the controllers. At that time the DVA (RMCS1, bit 11) is set indicating that the drive is ready to communicate with the controller which has seized it. If the drive is seized by the other controller, then the DVA bit is reset, all the drive registers read as 0's and any write to a register is ignored. Any attempt to seize a drive which is busy with the other port will cause the request to be remembered and acted upon when the drive is released by the other controller.

2.6.4 Returning to the Unseized State

The drive is released and returned to the unseized state by issuing a release command. In addition, a one second timer in the controller will timeout and release the drive if one of the events listed in section 2.6.2 for seizing the drive is not performed periodically to keep resetting the timeout timer. Reading the RMCS1 register will also reset the timeout timer if the drive is currently seized.

When the controller sees a previously busy drive becoming unseized, it checks its request flag. If the drive had been previously requested while busy on the other port, the controller will seize the drive, set the DVA bit and set the ATA causing an interrupt to the CPU if the IE bit is set. If the CPU does not respond to the attention within one second the drive will be released, but the ATA remains set.

2.6.5 DEC Compatibility

The SC21/B controller differs from the equivalent DEC controller in three important areas. First, there is no neutral state. Since the controller does not have instantaneous access to all drives at the same time (a limitation of the daisy-chained A cable and the microprocessor organization of the controller), the controller assumes a drive is busy on the other port if the controller has not already seized it. The DEC controllers can switch from neutral to seized state within the time required to do a single read or write of a drive register. In that case no ATA is set and the drive would appear to have been already seized.

Second, the release command is not instantaneous since the controller takes a few microseconds to execute the command. During this time the drive will appear to be unseized.

Third, during a data transfer the timeout timers will not operate and the drives can not be polled to see if they are not busy.

Therefore no drives are seized or released during the execution of a data transfer.

The software driver should not issue a Release command and then attempt to save the current status of a drive, since the Release command will immediately show the drive in the unseized state, thus returning zero data for the drive registers. In order to allow the other controller time to poll the drive, the CPU should not communicate with any of the released drive's registers until required to seize the drive again.

2.6.6 Dual Port Drives in Single Port Mode

When using an operating system which does not have dual port drive software support, it may still be advantageous to use dual port drives while operating in the controller in single port mode. This will allow for a non-dynamic type of operation between two CPUs. In this type of operation the controller does not unseize the drive and, in effect, it is seized by both controllers all the time.

The one second timer and the release command for this mode operate the same as those described in Paragraph 2.6.4. Even when released a drive will still appear to be seized to the releasing controller. No attention is generated when the other controller finds the drive not busy. Should a command be issued to a controller while a drive is busy on the other port, the controller will wait until the drive becomes unbusy before executing the command. No timer exists in this case.

This mode of operation eliminates the need for manually switching the drive from one controller to another.

2.6.7 Dual Access Mode

In order to provide compatability with RSX-11M Plus when it is configured for dual access, the dual access mode is supported on the SC21/BM model controller. This mode is currently not supported on VMS.

The mode is enabled by setting SW1-9 to ON (closed). When in this mode, the controller sets Dual Port Mode (Drive Type Register) and Programmable (Drive Status Register) to imitate the DEC neutral state.

When DPM and PGM are set, the operating system will attempt to seize a drive by simply writing a command to it. If the drive is unbusy the command is executed. The operating system will not issue a command to a drive when that drive is busy.

The first time the SC21 sees a drive, it is ignored for one second. This one-second stall occurs once for each drive on the controller. It prevents the controller from seeing erroneous status information when power is applied to the drive after the controller has been powered-up. For a drive in dual port mode the stall will prevent

the other CPU from accessing the drive until the stall completes. The dual access option switch bypasses the stall in all cases. For proper system operation with the dual access switch option ON, all drives must have power applied before either controller is powered-up.

The operating system's choice of controller depends on whether or not a controller is currently executing a command, and what type of command it is. A controller executing a data transfer command can not accept any other command. A controller executing a positioning or a housekeeping command may be given another command.

Setting the Dual Port Option switch overrides the Dual Access Option.

2.7 FIXED HEAD OPERATION

Certain Winchester type non-removal disks have an optional one or two megabytes of fixed head storage. This is useful for special applications such as swapping storage, since the zero seek time means quicker access time to the fixed head storage. This fixed head option is supported by the SC21/BF model controller.

2.7.1 Drive Numbering

Drives having the fixed head option will have two logical RM disks per physical drive. The movable head portion will have unit numbers 0 to 3 and the corresponding fixed head portion will have unit numbers 4 to 7. Unit 4 is on the same drive as unit 0 and has an A cable address of 0.

2.7.2 Drive Characteristics

The fixed head drive usually has the same number of tracks (heads) as the movable head drive. The number of cylinders will depend on the size of the fixed head option. In some configurations the last cylinder may not have a full number of heads.

Table 2-3
Register Access on Dual Controller Operation

Controller Action / Drive State:	Response With Respect To Action On Ch. I
Read RMCS1	
Drive Not Seized:	Reads the controller portion of the RMCS1 only. The drive's portion is read as all zeros. No request flag is set.
Drive Seized by Ch. I:	DVA = 1; reads the register and resets the timer.
Drive Seized by Ch. II:	DVA = 0; reads all zeros for the drive's portion of the register. No flag set.
Write RMCS1	
Drive Not Seized:	The function code is attempted if GO = 1 and a port request flag is set.
Drive Seized by Ch. I:	Loads the function code. (Switches to unseized if the function is a Release).
Drive Seized by Ch. II:	The function code is attempted if GO = 1 and a port request flag is set.
Read RMDS	
Drive Not Seized:	Reads all zeros.
Drive Seized by Ch. I:	Reads the status bits; PGM = 1; DPR = 1.
Drive Seized by Ch. II:	Reads all zeros.
Read any other drive register	
Drive Not Seized:	Reads all zeros.
Drive Seized by Ch. I:	Reads the register.
Drive Seized by Ch. II:	Reads all zeros.
Write any drive register	
Drive Not Seized:	The write is ignored, and a port request flag is set.
Drive Seized by Ch. I:	Loads the register. Resets timer.
Drive Seized by Ch. II:	The write is ignored, and a port request flag is set.

BLANK

Section 3
INSTALLATION

This section describes the step-by-step procedure for installation of the SC21/B Disk Controller in a PDP-11 system. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the SC21/B, is covered in paragraph 3.1 Appendix I contains an installation checklist.

Emulex recommends that Section 3 be read in its entirety before installation is begun.

1. Inspect the SC21/B.
2. Prepare the disk drives.
3. Install the bootstrap PROM if necessary.
4. Configure the SC21/B.
5. Install the SC21/B.
6. Route the drive I/O cables.
7. Test the controller.
8. Patch the operating system if required.

3.1 INSPECTION

Before unpacking the SC21/B, examine the packaging for any signs of damage. Notify the carrier if any damage is noted.

Make a visual inspection of the board after unpacking. Check specifically for bent or broken connector pins, damaged components or any other evidence of physical damage. Examine the PROMs to insure that they are firmly and completely seated in their sockets.

3.2 DISK DRIVE PREPARATION

The disk drive must be configured for the proper number of sectors, and have an ID plug or address selection switches properly configured.

3.2.1 Drive Placement

Uncrate and install the disk drives according to the manufacturer's instructions. Position and level the disk drives in their final places before beginning the installation of the SC21/B. This allows the I/O cable routing and length to be accurately judged. Place the drives side-by-side to make installation of the daisy-chained A cable simpler.

3.2.2 Local/Remote

The LOCAL/REMOTE switch controls whether the drive can be powered up from the drive (local) or the controller (remote). Place the switch in the REMOTE position. With the PDP-11 powered down, press the start switch on the front panel of each of the drives (the Start LED will light, but the drive will not spin up and become ready). When the PDP-11 is powered up, the drives will spin up sequentially. This prevents the heavy current draw that would be caused if all of the drives were powered up at once. When in the remote mode the drives will power down when the PDP is powered down. While the PDP is powered on, the drives may be powered up and down individually (to change disk media, for example) using the drive START switch.

3.2.3 Sectoring

The disk drive must be configured for 32 sectors which is equivalent to a sector size of 420 dibits. The exact method of entering this 420 count into the logic of the drive will differ from one drive manufacturer to another and the particular drive manual should be consulted for the exact procedure.

For CDC drives, a value of 419 should be entered into the sector length switches by closing switches 0, 1, 5, 7, and 8.

3.2.4 Drive Numbering

An address from 0 to 3 must be selected for each drive. Be careful that no two drives are assigned the same number. CDC drive addresses are selected by means of an ID plug. Drives by other manufacturers have their addresses selected by switches on one of the logic cards. Consult the particular drive manual for the exact procedure.

3.2.5 Sector and Index Modifications

It may be necessary to move the sector and index signals from the A cable to the B cable. See Section 3.4.5. Instructions for doing this for commonly used drives is included in Appendix F.

3.3 BOOTSTRAP PROM INSTALLATION

The VAX-11/750 bootstrap PROMs are located on the memory controller module. The PROMs are plugged into sockets so that you can remove and/or replace them. Table 3-1 shows the DEC factory placement of the bootstrap PROMs.

When installing a SC21 disk system, you need to install a UM boot PROM (EMULEX #287B) on the memory controller module. Installation of the PROM allows the user to boot the operating system from a system disk on the Unibus. The PROM is shipped in a PROM box. Carefully remove the PROM and plug it into the memory module. You may plug this boot PROM in the location that corresponds to switch

Table 3-1
DEC Placement of the Bootstrap PROMs

Boots Switch Position	Device Type
A	TU58
B	RL02
C	RK07
D	EMPTY

position D, or you can rearrange the bootstrap PROMs to correspond to any boot switch position configuration. The only requirement is that the TU58 bootstrap PROM remain on the memory controller module, preferably in either socket position A or D (see Figure 3-1). Note that the physical location of the bootstram PROM sockets on older L0011 memory boards may be different.

The Emulex boot PROM is limited to booting unit 0 on the SC21/V1 controller. If you wish to boot off a non-zero unit, you must boot from the console media, BOOT58. The console media can be updated to boot non-zero units via the Emulex UM driver installation procedure.

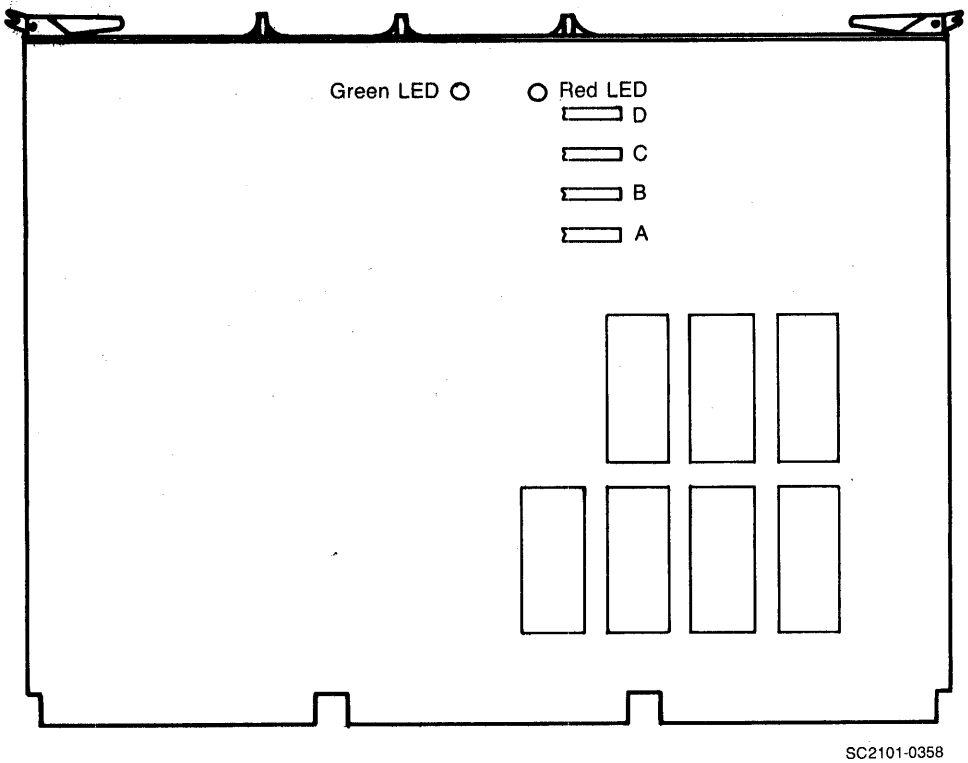


Figure 3-1 L0016 Memory Controller

3.4 CONTROLLER SETUP

Several configuration setups must be made on the controller before inserting it into the chassis. These are made by SW1, SW2 and SW3.

Figure 3-2 shows an assembly diagram of the SC21 Controller Board.

For the functions assigned to the configuration switches not discussed below, consult the appendix that specifically covers your controller emulation:

SC21/B1	Appendix A
SC21/V1	Appendix B
SC21/BE	Appendix C
SC21/BF	Appendix D
SC21/BM	Appendix E

3.4.1 Controller Address Selection

All Unibus controllers have a block of several command and status registers through which the system can command and monitor the controller. The blocks contain 20 registers, and are addressed sequentially from a starting address assigned to that device type, in this case a disk controller.

Register addressing for all emulations except the /BM is decoded by decode PROM #192, located at U130. The SC21/BM uses address decode PROM #793. See Table 3-2 for the available addresses and the necessary switch settings for all address decode PROMs.

Appendix B contains information on octal to hex conversion for addressing the SC21/V1.

3.4.1.1 Alternate Address Option Kits

Two alternate address option kits for the SC21/B emulations are available from Emulex. Option kit SC2113001 contains decode PROM #597. Option kit SC2113002 contains decode PROM #793. All SC21/B emulations will accept any option kit PROM. Table 3-2 shows the switch settings for the starting addresses of the controller registers for each optional PROM.

Table 3-2
Controller Addresses and Switch Settings

Switch SW2							
-9	-8	-7	-6	PROM #192	PROM #597	PROM #793	
O	O	C	O	776700	776700	776700	Standard
C	O	O	O	776300	776300	776300	Alternate
O	O	O	C	Not used[1]	776100	776600	Alternate
O	C	O	O	Not used[1]	775300	Not used[1]	Alternate

[1]All unused switches MUST BE OFF.

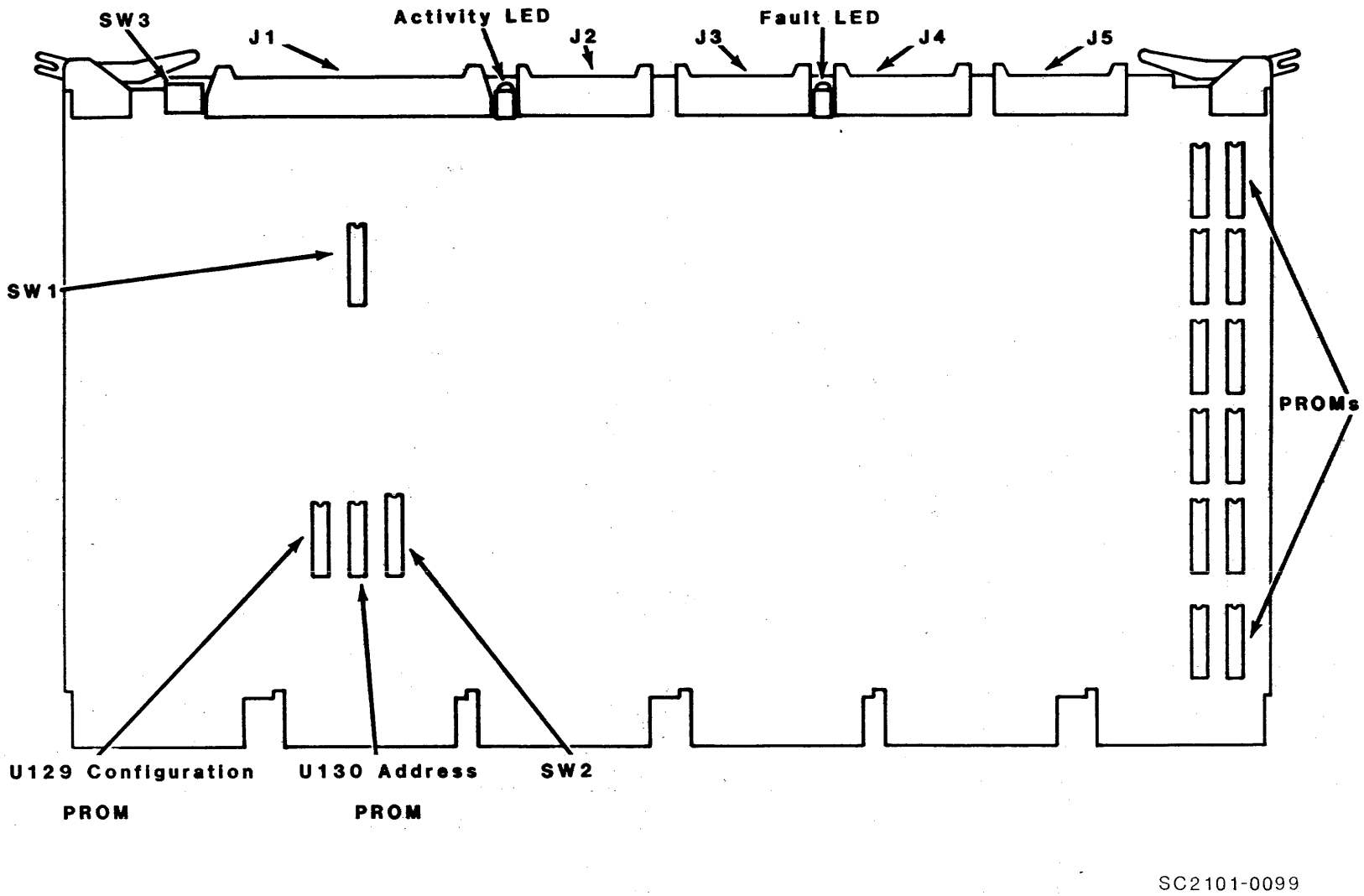


Figure 3-2 SC21 Controller Assembly

3.4.1.2 SC21/BM Address Selection

Register addressing for the /BM emulation is decoded by address decode PROM #793 (Emulex part number SC211717). Prior to the availability of this PROM, the /BM emulation was decoded by decode PROM 192, which currently decodes the remaining emulations. Table 3-2 shows the switch settings and addresses for PROM #793.

3.4.2 Interrupt Vector Address

The interrupt vector address is selected by means of SW1-1 and SW1-2. The standard vector address is 254. The alternates are 150, 370 and 374. Listed below are the switch settings for the standard and alternate interrupt vector addresses.

SW1-2	SW1-1	Vector
O	O	254 (Standard)
O	C	150 (Alternate)
C	O	370 (Alternate)
C	C	374 (Alternate)

3.4.2.1 SC21/BM Interrupt Vector Address

Revisions G and above of the SC21/BM emulation have increased interrupt vector addressing. An additional switch (SW3-4) is used to set vector addresses, increasing the number of possibilities for the /BM emulation to eight. The interrupt vector addresses and switch settings for the SC21/BM are listed below.

SW3-4	SW1-2	SW1-1	Vector
O	O	O	254 (Standard)
O	O	C	150 (Alternate)
O	C	O	370 (Alternate)
O	C	C	374 (Alternate)
C	O	O	354 (Alternate)
C	O	C	224 (Alternate)
C	C	O	270 (Alternate)
C	C	C	274 (Alternate)

3.4.3 Drive Configuration Selection

The phrase "drive configuration selection" describes the process that is used to select the logical disk drives that will be emulated by the SC21/B controllers using a given set of physical disk drives. That is, you have a particular set of physical disk drives. Using those disk drives and the SC21/B, you wish to emulate a specific type and arrangement of DEC subsystems. (The emulated subsystem is referred to as a logical disk drive.) Setting SW2-1 through SW2-5 on the controller allows you to select

the logical disk drive configuration (limited, of course, by the physical disk drives available).

Because the five emulations covered by this manual each offer different configurations, the configuration tables and instructions for using them are contained in Appendixes A through E.

SC21/Bl	Appendix A
SC21/Vl	Appendix B
SC21/BE	Appendix C
SC21/BF	Appendix D
SC21/BM	Appendix E

3.4.3.1 Alternate Configuration PROMs

An alternate configuration PROM is supplied with the SC21/Bl, SC21/BE, SC21/Vl and SC21/BM emulations. The PROM is shipped in the socket at location Ul25. This alternate configuration PROM replaces the standard configuration PROM at Ul29. To use the PROM, remove it from its shipping location and plug it into the socket at location Ul29. The table below shows the PROM number which each emulation receives.

Emulation	PROM Number
SC21/Bl	898
SC21/BE	898
SC21/Vl	986
SC21/BM	987

3.4.4 Dual Access Mode

In order to provide compatibility with RSX-llM Plus when it is configured for dual access, the dual access mode is provided on the SC21/BM. The dual access mode is enabled by setting SWl-9 to ON (closed). This mode should only be selected when the disk drive has dual ports and is configured for dual port operation. This feature was added to the SC21/BM at revision level "F".

See paragraph 2.6.7 for programming information.

3.4.5 Index and Sector Pulse Selection

The SC21/B controllers are designed to have the Index and Sector signals on the B cable from each physical drive. The signals are necessary for proper operation of the sector counters associated with each drive. The RM emulation requires an updated sector counter which can be read by the PDP-11. Failure to have a valid sector counter may cause incorrect operation of the rotational position sensing software.

Depending on the disk drive, the index and sector pulse signals may be carried on the A instead of the B cable. For example, standard CDC drives provide the index and sector signals on the A cable; however, they may be moved to the B cable by minor rewiring of the drive backplane, or this configuration may be ordered from the factory. The procedure for making this modification to several of the more common drives is described Appendix F. If the procedure for the drive in question is not covered there, it is generally described in the drive manual.

It is possible to operate with the index and sector signals on the A cable by placing switch SW1-8 in the ON position. When operating in this manner there is some loss of capabilities and performance including: the Search command operates as a Seek; the sector counter in RMLA will be incorrect; and each transfer must wait for an index pulse to sync-up the sector counter. Also, some of the lower level diagnostics will produce some errors.

3.5 PHYSICAL INSTALLATION

3.5.1 SPC Slot Selection

The controller may be placed in any SPC slot along the Unibus without regard to NPR priority. The controller contains adequate buffering to prevent data lates and will automatically get off the bus if any other device is waiting for the Unibus. If the system contains a Unibus repeater, the controller will not give priority to devices which are on the CPU side of the repeater when the controller is on the far side of the repeater. This may require that the controller be placed on the CPU side of the repeater or that all DMA devices be on the far side of the repeater.

3.5.2 NPG Signal Jumper

The NPG signal jumper between pins CA1 and CB1 on the backplane must be removed so that the NPG signal passes through the controller. See Figure 3-3.

3.5.3 Mounting

The controller board should be plugged into the PDP backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the board with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly in the throat of the connector before attempting to seat the board by means of the extractor handles.

3.6 CABLING

The subsystem cabling of the drives and controller is shown in Figure 3-4.

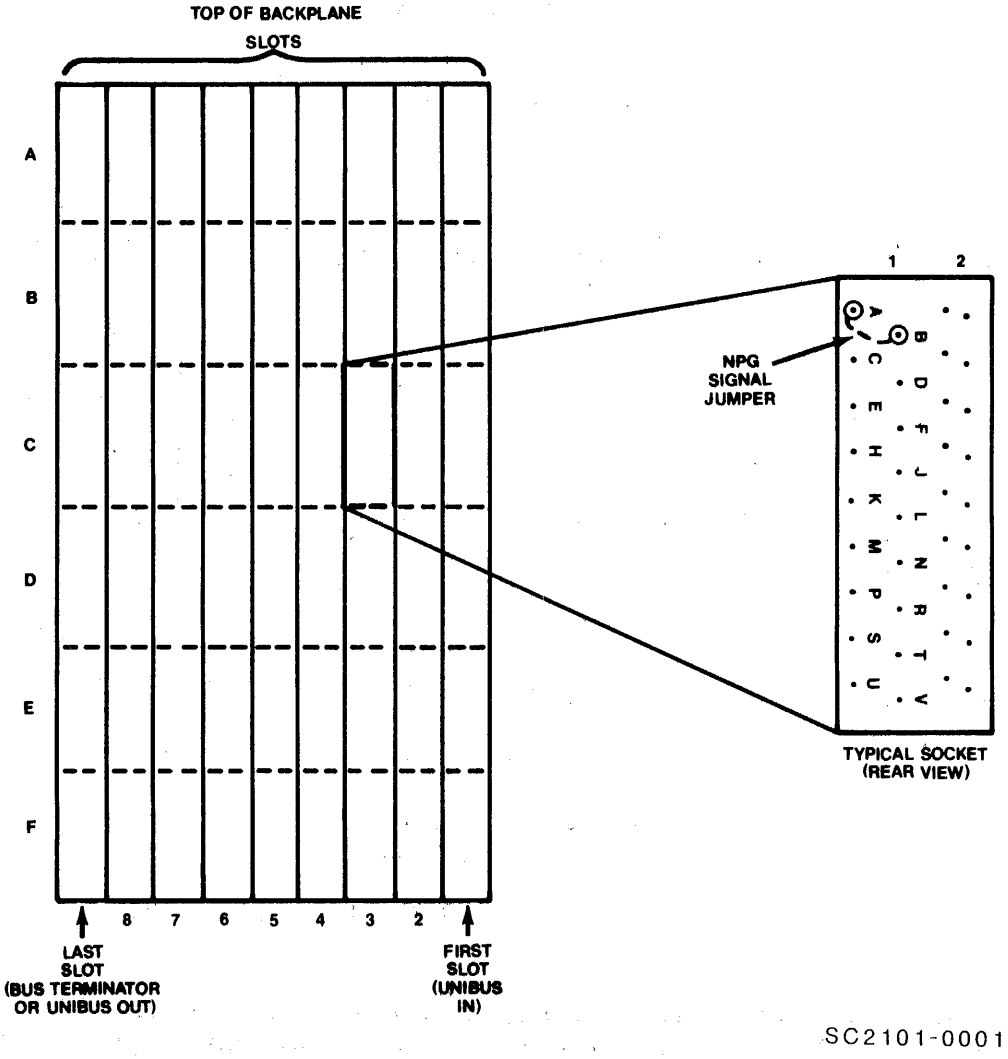
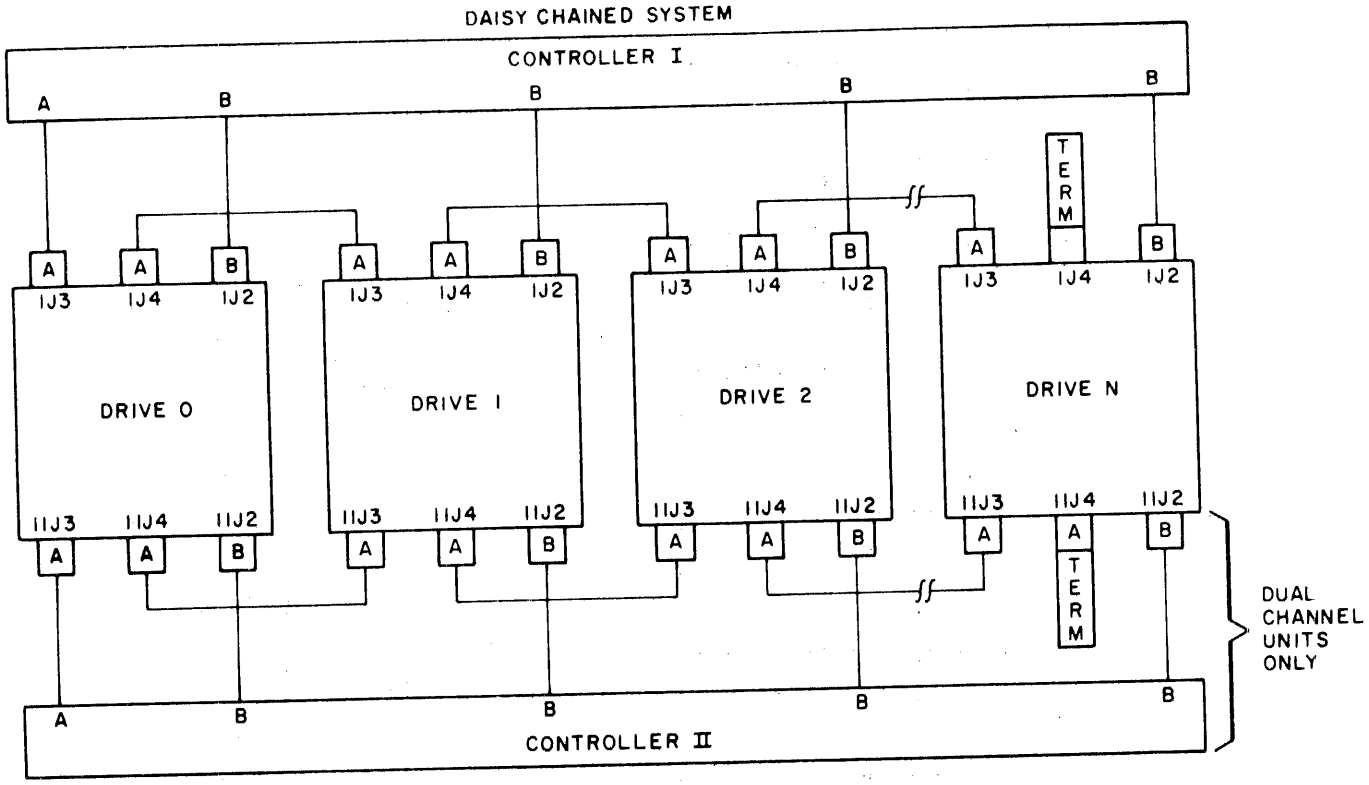


Figure 3-3 NPG Signal Jumper Location

3.6.1 A Cable

The 60-wire A cable should be plugged into the connector on the A board of the controller and wired to the first drive. If more than one drive is used, it is then daisy-chained to the other drives. The last drive on the A cable must have a terminator installed. This part is available from the drive manufacturer. The terminator is generally plugged into one of two A cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin 1 of the board connector is on the left. Pin 1 of the cable connector has a notch on the connector body to identify it. Twist and flat cable will have brown-brown twist followed by red-brown twist on the pin 1 edge of the cable. The cable will normally egress to the rear of the controller.



NOTES:

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET

SC2101-0000

Figure 3-4 Drive Cabling Diagram

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.

3.6.2 B Cable

Each drive must have a 26-wire B cable wired from the drive to one of the B ports of the controller. It makes no difference which B port connection is used by a drive. No external terminators are used with the B cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe.

NOTE: Observe the same caution on connector reversal given in paragraph 3.6.1.

3.6.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic

ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

3.7 TESTING

3.7.1 Self-Test

When power is applied to the CPU, the controller will automatically execute a built-in self-test. This self-test is not executed with every bus INIT but only on powering-up. If the self-test has been executed successfully, the Fault LED on the top edge of the controller board will be OFF or flashing. The Fault LED flashes when the controller cannot properly address at least one drive after successfully executing its self-test. This will occur if the A and B cables are not properly plugged in, a drive is not powered-up with a code plug, or two drives have an identical code plug. Appendix I contains a troubleshooting guide. If the Fault LED is ON steadily the controller did not pass its self-test and the controller cannot be addressed from the CPU.

3.7.2 Register Examination

After powering-up the CPU and noting that the Fault indicator is not ON steadily, a quick check should be made to ensure that the controller registers can be read from the computer console. The RMCS1 register will contain 004200 if the drive is available and 000200 if it is not. If the CPU has a console emulator all the registers of the controller should be examined.

3.7.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing headers and zero data in all sectors of the disk. This format does not verify the data or headers and does not write a Bad Sector File on the last track of the last cylinder. The following instructions are valid only for the PDP-11. All numbers are in octal.

Formatting is carried out from the CPU front panel as follows:

1) Halt the CPU by placing the HALT/ENABLE switch in the down position. With the CPU HALT switch down, press the START switch (causes an INIT).

2) Install a scratch pack on Drive 0 and make ready.

3) Deposit the drive number (if other than 0) in RMCS2 at 176710 (176310 if alternate address range is selected).

4) Deposit a 177777 in RMHR at 176736 (176336) to enable the optional Format Command.

5) Deposit a 000021 (Read-in Preset Command) in RMCS1 at 176700 (176300). This sets Volume Valid.

6) Deposit a 000077 (Format command) in RMCS1 at 176700 (176300). The WRITE activity indicator near the bottom of the board will flash as long as the formatting is underway. Wait until this LED goes off.

7) Examine RMDS at 176712 (176312) to see if the drive's ERR (bit 14) is set indicating an error. If there is an error resulting from the format operation, RMER1 and RMER2 should be examined to determine the cause of the error, and RMDA and RMDC should be examined to see how far the formatting progressed.

8) Run the software format program or run the Emulex S1B18X format program.

3.7.4 Diagnostics

The DEC RM02/RM03 diagnostics should be run. Generally it will be necessary to run only the Formatter and the Performance Exerciser. If the drive is other than an 80 megabyte with 823 cylinders and 5 tracks it will be necessary to patch the diagnostics as shown in Section 6.

It is recommended that the user run the Emulex self-sizing diagnostics rather the DEC supplied diagnostics. The Emulex diagnostics do not require patching.

If the Formatter diagnostic is run on an unformatted disk, it will report five errors in trying to read the Bad Sector File before it will proceed.

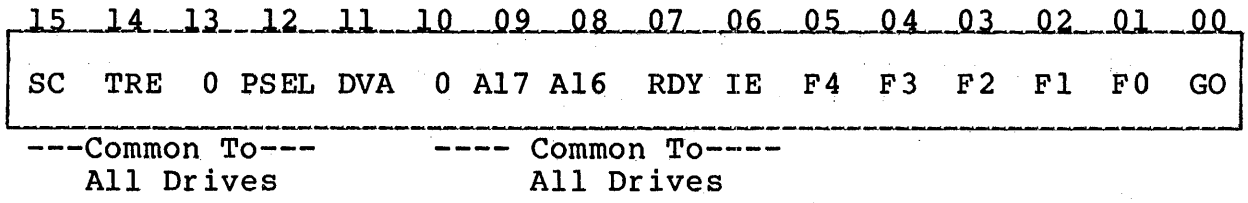
3.8 OPERATING SYSTEM PATCHES

If the disk drive is a size different than that of the DEC disk for the selected Drive Type Code, it will be necessary to patch the operating system. Patches for RSX-11M and RSTS/E can be found in the Emulex Patch Document (P/N PD9951002)

There are 20 device registers in the SC21/B. These are used to interface the controller to the drives and the computer. The registers are loaded and/or read under program control in order to initiate selected disk commands and monitor status and error conditions. Most registers can be written into with word or byte operations.

The RMWC, RMBA, RMCS2, RMDB and bits <15:12> and <10:06> of RMCS1 are common to all drives. Loading and reading of these registers is independent of the unit selected. A separate set of the other registers and bits 11 and <05:00> of RMCS1 exists for each of the drives. Loading and reading of these registers is dependent on the drive selected by the unit number in RMCS2. In addition, the eight ATA bits in RMAS are each associated with an individual drive. Any attempt to write into the drive registers (except RMAS) while the drive's GO bit is asserted will cause a register modification refused error and the register is not modified.

4.1 CONTROLLER/STATUS REGISTER 1 (RMCS1) 776700



The RMCS1 register can be read or written by program control, and is used to store the current disk command function code and operational status of the controller. Setting the GO bit will cause the controller to recognize the function code in the register and initiate the operation for the corresponding drive. The actual start of execution of the command does not begin when the function code is loaded into the control register but commences when the controller has finished any previous operation and polls through the drive RMCS1's in search of a command needing initiation.

Special Condition (SC) - Bit 15

This read only bit is set as long as TRE in RMCS1 or any of the drive's ATA bits are set. This bit causes a CPU interrupt if IE is also set.

Transfer Error (TRE) - Bit 14

This read/write bit is set by DLT, WCE, UPE, NED, NEM, PGE, MXF, or a drive error during a data transfer. Writing a 1 into the bit causes the controller error bits in RMCS2 to be cleared. They are also cleared at the start of every data transfer operation.

Port Select (PSEL) - Bit 12

This is a read/write bit that has no effect on any controller operations. (For diagnostic compatability.)

Drive Available (DVA) - Bit 11

This read-only bit is set when the drive is seized by the controller. When not in dual port mode, the drive is seized as long as it is powered-up.

Extended Bus Address (A16, A17) - Bits 08, 09

Upper extension of the RMBA register. This two-bit counter is incremented by one every time RMBA overflows. These bits cannot be altered if RDY = 0 and no error results when attempted.

Ready (RDY) - Bit 07

This read-only bit is reset when the controller starts a Data Transfer Command (codes 51 - 77) and is set at the termination of the data transfer.

Interrupt Enable (IE) - Bit 06

When IE is set an interrupt can be generated when RDY is asserted at the end of a data transfer or by any ATA being asserted. It is reset automatically when the interrupt is accepted by the CPU. When a zero is written into IE by the program, any pending interrupts are cancelled. An interrupt is generated by writing 1's into IE and RDY at the same time.

Function Code (F4-F0) - Bits <05:01>

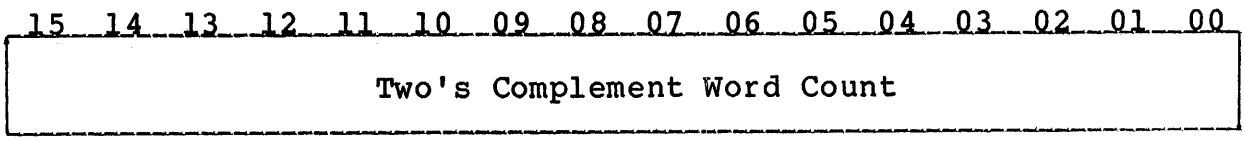
F4-F0 and the GO bit make up the function (command) code which determine the action to be performed by the controller and drive as shown below:

01	No Operation	37	Transparent ECC Correction
05	Seek Command	41	RMWC Equals Sector Count
07	Recalibrate	51	Write Check Data
11	Drive Clear	53	Write Check Header and Data
13	Release	61	Write Data
15	Offset Command	63	Write Header and Data
17	Return to Centerline	71	Read Data
21	Read-In Preset	73	Read Header and Data
23	Pack Acknowledge	75	Boot (Optional)
25	DMA Bandwidth Set (Optional)	77	Format (Optional)
31	Search Command		

GO (GO) - Bit 00

The GO bit must be set to cause the controller to respond to a command. The GO bit is reset after command termination.

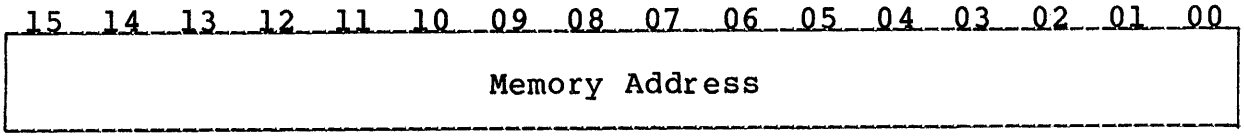
4.2 WORD COUNT REGISTER (RMWC) 776702



The RMWC register is loaded with the two's complement of the number of data words to be transferred to or from main memory. The register is incremented by 1 after each word transferred, and accommodates a maximum transfer of 65,536 words. The RMWC register is not cleared by INIT or controller clear.

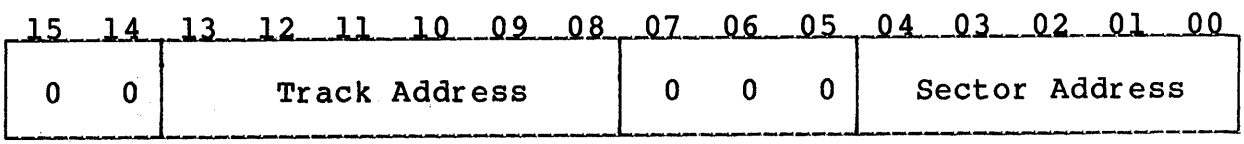
When the special feature RMWC equals sector count is enabled for the SC21/BE, the contents of this register contain the number of sectors to be transferred, rather than the number of words.

4.3 UNIBUS ADDRESS REGISTER (RMBA) 776704



The RMBA register is initially loaded with the low-order 16 bits of the memory address for a data transfer. The low-order bit (00) is always forced to a 0. The RMBA register is incremented by 2 after transfer of a word to or from memory, unless the BAI bit is set.

4.4 DISK ADDRESS REGISTER (RMDA) 776706



This register is used to address the sector and track on the disk to or from which a transfer is desired. It can only be loaded as a word. The RMDA is incremented each time a sector of data is transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred. At the end of a transfer, RMDA contains the address of the sector following the last one involved in data transfer.

The RMDA contains a 5-bit sector counter providing 32 sectors per track. The register also contains a 6-bit track counter which is incremented by one every time the sector counter overflows. When the sector address and the track address reach their maximum counts, they are reset to 0 and the RMDC is incremented by one. The invalid address error (IAE, RMER1, bit 10) is set if the address in the RMDA is invalid when a data transfer, Seek, or Search function is initiated. The maximum track address is obtained from the selected configuration.

4.5 CONTROL/STATUS REGISTER 2 (RMCS2) 776710

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0

The RMCS2 register can be read or written under program control and is used to store the current drive select code and controller operational status. In addition, the register can initiate a controller clear operation. It is recommended that writes to the unit select bits be done with byte-writes since two of the error bits in the upper byte and read/write.

Data Late (DLT) - Bit 15

This bit cannot normally be set because of the three sector buffer in the controller. It can be set by accessing RMDB without the appropriate status bit (06 or 07) in RMCS2 set to a 1. This is a read-only bit.

Write Check Error (WCE) - Bit 14

Set when the controller is performing a write check operation and a word from the disk does not match the corresponding word in memory. When the mismatch occurs, the reading of the disk terminates and the WCE bit is set. The memory address displayed in RMBA is the address of the word following the one which did not match (if BAI is not set). The mismatched data word on the disk is displayed in the data buffer (RMDB). This is a read-only bit.

Unibus Parity Error (UPE) - Bit 13

Set if a parity error occurs in the Unibus memory while the controller is performing a write or write check command. When the error occurs, the RMBA register contains the address of the word following the word with the parity error (if BAI is not set). This is a read/write bit.

Nonexistent Drive (NED) - Bit 12

Set when the program reads or writes a device register associated with a drive (selected by U2-U0) which is not recognized because of a wrong code plug, not powered up, or is non-existent. This is a read-only bit.

Nonexistent Memory (NEM) - Bit 11

Set when the controller is performing an NPR transfer and the memory does not respond within 10 microseconds. The memory address contained in RMBA is the address of the word following the memory location causing the error. This is a read-only bit.

Program Error (PGE) - Bit 10

Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. This is a read-only bit.

Missed Transfer (MXF) - Bit 09

Set if a data transfer cannot be executed (RMDS ERR bit = 1). This is a read/write bit.

Massbus Data Bus Parity (MDPE) - Bit 08

This read-only bit is always a zero.

Output Ready (OR) - Bit 07

Set when a word is present in RMDB and can be read by the program. Cleared by reading RMDB. Any attempt to read RMDB register before OR is asserted will cause a DLT error. This is a read-only bit.

Input Ready (IR) - Bit 06

This read-only bit is always a 1.

Controller Clear (CLR) - Bit 05

When a 1-bit is written into this bit position, the controller is initialized (Paragraph 2.6.1). This is a write-only bit. It is always read as a zero.

Parity Test (PAT) - Bit 04

This read-write bit has no effect on any controller operation. (For diagnostic compatability.)

Unibus Address Increment Inhibit (BAI) - Bit 03

When BAI is set, the controller will not increment the RMBA register during data transfer, causing all data words to be read from or written into the same memory location. This is a read/write bit.

Unit Select (U2-U0) - Bits <02:00>

These bits select one of eight logical units for communicating with the CPU. The unit select bits can be changed at any time without interfering with the current operations. These are read/write bits.

4.6 DRIVE STATUS REGISTER (RMDS) 776712

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0	OFM

This register contains various status indicators for the drive selected by the unit number in RMCS2. The register is a read-only register.

Attention Active (ATA) - Bit 15

An attention condition will set the ATA bit in this register and the Attention Summary register (RMAS). It is cleared by INIT, controller clear, loading a command with the GO bit set or loading a 1-bit in RMAS register corresponding to the drive's unit number. The last method of clearing the ATA bit will not clear the error indicators.

An attention condition is caused by: an error in the error registers; the completion of a positioning operation; the change of state of the MOL bit; dual port operation with the drive presently available if previously not available; correct sector identification for the Search command.

Error (ERR) - Bit 14

Set when one or more of the errors in the error registers (RMER1 or RMER2) for a selected drive is set. While ERR is asserted, commands other than Drive Clear are not accepted.

Positioning in Progress (PIP) - Bit 13

Set when a positioning command is accepted. These commands are: Seek, Recalibrate, and Search. Cleared when the moving function is completed at the time the DRY and ATA bits are set. Also set if MOL is reset.

Medium On-Line (MOL) - Bit 12

Set when the unit ready line from the drive is asserted indicating that the drive is up to speed, the heads are positioned over the recording tracks and no fault condition exists within the drive. Cleared when the spindle is powered down or the drive is off-line. Whenever the MOL bit changes state, the ATA bit is set.

Write-Lock (WRL) - Bit 11

Set when the write protected line from the drive is asserted as enabled by a switch located on the drive. A write command on a write-locked drive will cause the write-lock error (WLE, bit 11 of RMER1) to be set.

Last Sector Transfer (LST) - Bit 10

Set when the last addressable sector on the disk pack has been read or written. Cleared when a new write to RMDA is received.

At the time LST is set, the RMDA register is reset to 0 and the RMDC register increments by 1 to the first illegal cylinder address. If the RMWC register is not 0, a mid transfer seek is aborted which will cause the AOE status bit (RMER1, bit 09) to be set indicating that the desired cylinder register overflowed during a read or write.

Programmable (PGM) - Bit 09

This bit is set when dual port or dual access operation is enabled.

Drive Present (DPR) - Bit 08

This bit is set if the controller has seized the drive and is reset when the other controller has seized the drive. This bit is a reflection of the DVA bit in RMCS1.

Drive Ready (DRY) - Bit 07

Set at the completion of every command and cleared at the initiation of a command. When set, this bit indicates the readiness of the drive to accept a command. If a mechanical movement command was initiated, the ATA bit will also be set when DRY is set. This bit is the complement of the drive's GO bit.

Volume Valid (VV) - Bit 06

Set by the Pack Acknowledge or Read-In Present commands. Cleared whenever the drive cycles up from the OFF state. When reset, this bit indicates that the drive has been off-line and a disk pack may have been changed.

Offset Mode (OFM) - Bit 00

Set by the offset command to indicate that a read will be done with the heads in the offset position as determined by RMOF bit 07. Cleared by a Read-in Preset, Return-to-Centerline, Recalibrate or write command, or a mid-transfer seek.

4.7 ERROR REGISTER 1 (RMER1) · 776714

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF

The RMER1 register is a read/write register that is used to store the error status of the drive whose unit number is in RMCS2. The

RMER1 register can only be written as a word. Any attempt to write a byte will cause an entire word to be written. If the program attempts to write into this register while the drive is busy, an RMR (RMER1 register, bit 02) error is set, and the contents of the register are not otherwise modified. Writing 0's into this register should not be used as the normal way of clearing errors. The Drive Clear command should be used instead.

Data Check (DCK) - Bit 15

Set during a read operation when the ECC hardware detects an ECC error. The data transfer terminates with the current sector. If the Error Correction Inhibit (ECI) bit is off, the controller will go into the error correction process, and the RDY bit will not be set until the end of the process. If ECI bit is on, the error correction process is inhibited, and the RDY bit is set.

Unsafe (UNS) - Bit 14

This bit is a composite error bit of the unsafe and seek incomplete error conditions in the RMER2 register. With UNS set, correct results on any operation cannot be guaranteed. Some faults must be cleared by manual intervention at the drive.

Operation Incomplete (OPI) - Bit 13

Set when a read or write command involving header search cannot find the physical sector within three index pulses. Also set during a search operation where a sector count match is not made within three index pulses. When OPI is set, the GO bit is cleared and the RDY bit is set.

Drive Timing Error (DTE) - Bit 12

Set when either the header or data sync pattern is not found. When DTE is set, the GO bit will be cleared and the RDY bit set. Also set if a sector pulse occurs before the end of a sector's data field.

Write Lock Error (WLE) - Bit 11

Set when a write command is issued to a write-locked drive.

Invalid Address Error (IAE) - Bit 10

Set when the address in RMDC or RMDA is invalid and a Seek, Search or data transfer command is initiated.

Address Overflow Error (AOE) - Bit 09

Set when the RMDC register overflows during a read or write operation indicating that the address has exceeded the cylinder

address limit. With AOE set, the controller will terminate the operation when the last sector of the last cylinder has been read or written.

Header CRC Error (HCRC) - Bit 08

Set by a CRC error in the header. If a CRC error is detected during a read or write command, the controller will not make any data transfer. In the event of a CRC error during a read/write-check header and data command, the entire sector will be transferred with the HCRC bit set.

Header Compare Error (HCE) - Bit 07

Set when the first two words of the header read at the sector whose count is equal to the desired sector field of RMDA do not match the contents of RMDC and RMDA. If the HCE bit is set during a read or write command, the controller will not perform any data transfer. In the event of a read/write-check header and data command, the entire sector will be transferred with the HCE bit set.

ECC Hard Error (ECH) - Bit 06

Set when the error correction procedure indicates that the error was a non-correctable ECC error. DCK (Bit 15) is also set. This bit will never be set if ECI is on.

Write Clock Fail (WCF) - Bit 05

This bit is normally a zero unless written into.

Format Error (FER) - Bit 04

Set if the FMT16 bit in RMOF does not match bit 12 in word 1 of a sector's header. Although the controller implements both 30 and 32 sector formats, all sectors contain 256 16-bit words in either format. If FER is set, then HCE may not be set.

Parity Error (PAR) - Bit 03

Set if the optional checksum feature is enabled and a bad checksum compare is found during a write operation.

Register Modification Refused (RMR) - Bit 02

Set when a write is attempted to any drive register (except RMAS) with DRY=0. The drive will continue to execute the command in progress.

Illegal Register (ILR) - Bit 01

This bit is normally a zero unless written into.

Illegal Function (ILF) - Bit 00

Set when the function code in RMCS1 is illegal and the GO bit is set.

4.8 ATTENTION SUMMARY REGISTER (RMAS) 776716

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

The RMAS register allows the program to examine the attention status of all drives with only one register read operation. It also provides a means of resetting the attention logic in a selected group of drives. The eight low-order bits of this register correspond to the ATA bits in the RMDS of the drive having the same unit number as the bit position of this register.

A drive's ATA bit can be reset by loading a 1 into the bit position corresponding to the drive's unit number. Loading a 0 has no effect. For a program to use the RMAS without losing status information, the program must use MOV instructions for all writes to this register. An instruction that does a read-restore (such as BIS) may cause bits that became asserted just prior to the read to be lost. This register can be read or written at any time.

A persistent error, just like any error condition, will cause the ATA bit to be reasserted. Attempts by the controller to clear the error will not work in this case.

4.9 LOOK-AHEAD REGISTER (RMLA) 776720

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Sector Counter					0	0	0	0	0	0

The RMLA register contains the drive sector counter and is used to present the angular position of the disk relative to the read/write heads for the disk whose unit number appears in RMCS2. The purpose of this register is to provide the programmer with a means of optimizing disk accesses by minimizing rotational delays. The counter counts from 0 to 31.

4.10 DATA BUFFER (RMDB) 776722

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Data Buffer															

The RMDB register provides a maintenance tool to check the controller data paths. The IR (input ready) and OR (output ready) status indicators in RMCS2 registers are provided so that the programmer can determine when words can be read from or written into RMDB.

RMDB is used as an access to the Silo Buffer for an RM02. This controller has no Silo Buffer. All writes to this register are ignored. If a write-check error occurs, the data word as read from the disk is placed in RMDB and the OR bit in RMCS2 is set. Reading RMDB resets OR. Any further attempts to read RMDB will create a DLT error.

4.11 MAINTENANCE REGISTER 1 (RMMR1) 776724

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	MUR	MOC	MSER	MDF	0	0	MWP	0	0	DMD

RMMR1 is a read/write register that allows a program to simulate various signals from the disk for diagnostic testing of the controller. The DMD bit must be set before any other bit has an effect on the controller. This register may be written into as a word or a byte. Writing to RMMR1 can occur at any time regardless of the status of the drive. A drive or controller clear resets this register except for bit 3, which is set.

Maintenance Unit Ready (MUR) - Bit 09

Set by a diagnostic program to simulate the Unit Ready signal from the drive.

Maintenance On Cylinder (MOC) - Bit 08

Set by a diagnostic program to simulate the On Cylinder signal from the drive.

Maintenance Seek Error (MSER) - Bit 07

Set by a diagnostic program to simulate the Seek Error signal from the drive.

Maintenance Drive Fault (MDF) - Bit 06

Set by a diagnostic program to simulate the Fault signal from the drive.

Maintenance Write Protect (MWP) - Bit 03

Set by a diagnostic program to simulate the Write Protect signal from the drive.

Diagnostic Mode (DMD) - Bit 00

Set by the diagnostic program to reconfigure the drive into maintenance mode. None of the other bits in this register have any effect on the controller unless DMD is 1. Before a drive can be set to maintenance mode, it must first be ready and not busy. No positioner motion is initiated for a Seek, Home, Search or Implied Seek and all data transfer commands are ignored.

4.12 DRIVE TYPE REGISTER (RMDT) 776726

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DPM	0	0	0	Drive Type Code							

Moving-Head (MOH) - Bit 13

This bit is always a 1 indicating that the drive is a moving head device.

Dual Port Mode (DPM) - Bit 11

This bit signifies that the drive is operating in dual port mode as enabled by SW1-6, or in dual access mode as enabled by SW1-9.

Drive Type Code - Bits <07:00>

This code specifies the type of drive as follows:
24 - RM03, 25 - RM02, 27 - RM05.

4.13 SERIAL NUMBER REGISTER (RMSN) 776730

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SW1 -8	SW1 -7	SW1 -6	SW1 -5	SW1 -4	SW1 -3	SW1 -2	SW1 -1	Firmware Rev.				Port No.			

The purpose of the RMSN register was to distinguish a drive from similar drives attached to the controller by means of a four decade serial number. Here it consists of the controller port number for which the drive is attached, the firmware revision level, and the eight SW1 switch settings.

4.14 OFFSET REGISTER (RMOF) 776732

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	FMT 16	ECI	HCI	0	0	OFS 7	0	0	0	0	0	0	0

The RMOF register contains two inhibit bits and the drive offset direction bit. The offset direction bit determines if a read will be done with the heads advanced or retarded from normal centerline position. The actual offset determination is done by the status of RMDS bit 00. All bits of this register are cleared by Read-in Preset command.

Format Bit (FMT 16) - Bit 12

Set for 32 sector (16 bit) mode and reset for 30 sector (18 bit) mode. Since the controller only handles 16 bits/word format, this bit should always be a 1.

Error Correction Code Inhibit (ECI) - Bit 11

Set to inhibit error correction when an ECC error is detected. See paragraph 4.7, bit 15.

Header Compare Inhibit (HCI) - Bit 10

Set to inhibit header compare and CRC check. With HCI set, the controller depends only on the sector count for sector identification. It is recommended that the HCI bit be reset during a write operation.

Offset Direction (OFS7) - Bit 07

Set under software control to select the direction of positioner offset. A one retards the heads and a zero advances the heads.

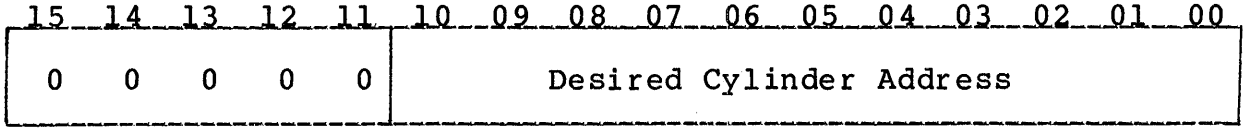
Transparent ECC Correction Status (TEC) - Bit 02

During normal operation, remains a zero. If enabled with SC21/BE emulation indicates that transparent ECC correction is enabled. See paragraph 5.4.4.1 for more information.

Word Count Register Function (WCR) - Bit 01

During normal operation, remains a zero. If enabled with SC21/BE emulation indicates that RMWC equals sector count is enabled. See paragraph 5.4.4.2 for more information.

4.15 DESIRED CYLINDER REGISTER (RMDC) 776734



The RMDC register contains the address of the cylinder to which the positioner is to move. The RMDC register will be cleared by the Read-in Preset command. Following an initial load, the value in the RMDC register will be incremented by 1 whenever the RMDA register is reset to 0 during a data transfer. When the RMDC

register is incremented and the RMWC register is not equal to 0, a mid-transfer seek is initiated by the controller.

The Invalid Address Error (IAE) bit will be set when, upon asserting the GO bit, the RMDC register contains an address greater than the largest addressable cylinder.

4.16 HOLDING REGISTER (RMHR) 776736

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RMHR is a read-only register that always returns a zero when read except as follows: If the register is written into with one of the values listed below, it is possible to read out the configured size of the selected disk from the same register.

100027 - Maximum cylinder address
100030 - Maximum track address
100031 - Maximum sector address

Writing a 177777 into the register enables the optional Boot and Format commands to be executed when loaded into RMCS1. The enable is cleared when any data transfer command terminates.

4.17 MAINTENANCE REGISTER 2 (RMMR2) 776740

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
11777_8															

RMMR2 is a read-only register. It will return 11777_8 when read with drive connected and selected via RMCS2. With drive not connected and up to speed or not selected through RMCS2, this register will return zeros.

4.18 ERROR REGISTER 2 (RMER2) 776742

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	OPE	IVC	LSC	LBC	MDS	DCU	DVC	ACU	0	0	DPE	0	0	0

Error Register 2 is a read/write register that contains status information relating to the electromechanical performance of the drive whose unit number is in RMCS2. This register may be written as either a word or a byte. If any bit is set in this register, then the ERR bit in RMDS is also set. In some cases, the UNS bit in RMER1 will also be set. Writing zeros into this register should not be used as the normal way of clearing errors. A drive clear or a controller clear should be used instead. If the program attempts

to write into this register while the drive is busy, the RMR bit in RMER1 will be set and the write will be ignored.

Bad Sector Error (BSE) - Bit 15

Set whenever the controller detects a zero in bit 14 or 15 of the first header word and the HCI bit in RMOF = 0. HCE in RMER1 may also be set.

Seek Incomplete (SKI) - Bit 14

Set whenever a Seek Error is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if a Seek Error is detected.

Operator Plug Error (OPE) - Bit 13

Set whenever the drive's address plug is removed and then reinstalled. This bit can be cleared by issuing a drive clear.

Invalid Command (IVC) - Bit 12

Set whenever any command is issued to a drive with MOL = 0. Set whenever any command except a Read-in Preset or a Pack Acknowledge is issued to a drive with VV = 0.

Loss of Sector Clock (LSC) - Bit 11

Set when the controller detects more than 63 Sector pulses without an Index pulse, with Sector and Index on B cable.

Loss of Bit Clock (LBC) - Bit 10

Set if the controller does not detect at least 16 servo clocks within 3.0 microseconds.

Multiple Drive Select (MDS) - Bit 09

Set when more than one drive responds to a logical address on the A cable. This bit cannot be set by a program.

D.C. Power Unsafe (DCU) - Bit 08

Set if the -5 VDC power supply to the cable drivers and receivers is not proper. This bit cannot be set by a program.

Device Check (DVC) - Bit 07

Set if a Fault indication is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if a Fault is detected.

AC Power Unsafe (ACU) - Bit 06

Set if an ACLO indication is received from the Unibus.

Data Parity Error (DPE) - Bit 03

This bit is normally a zero unless written into.

4.19 ECC POSITION REGISTER (RMEC1) 776744

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	ECC Position												

The Error Correction Code (ECC) Position register is a read-only register that contains the position of the error pattern as determined by the ECC correction procedure. The error position is the number of bit positions from the beginning of the sector's data field to (and including) the right most bit position of the error pattern stored in RMEC2. If the detected error is not correctable using ECC, the ECH error bit in RMER1 will be set.

4.20 ECC PATTERN REGISTER (RMEC2) 776746

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Error Pattern										

The Error Correction Code (ECC) Pattern register is a read-only register that contains the 11-bit error correction pattern obtained from the ECC correction procedure. A 1 in the error pattern indicates a bit of the data in memory from the last read sector which is in error. The error pattern may straddle two 16-bit words in memory. The bit displacement to the right most bit of the pattern is determined by the bit count in RMEC1. The actual correction is done by an exclusive-OR of the error pattern and the data in memory.

Operations are initiated on the drive selected by the unit select bits in RMCS2 by loading the function code and GO bit into RMCS1. The function code specifies a specific command. The commands can be divided into three categories: data transfer commands, positioning commands, and housekeeping commands. Commands and their corresponding function codes (always odd since the GO bit must be asserted to execute the command) are described below:

5.1 DATA TRANSFER COMMANDS

These commands involve data transfers to or from the disk and are designated by function codes 51 through 77.

All data transfer commands have seek and sector search functions implied. When the desired cylinder does not equal the current cylinder during the execution of the data transfer, a seek will be issued to the desired cylinder. The controller will then search the desired track for the desired sector and, when found, will start the data transfer. On all commands except the Write Header and Data command (which is the format operation) and Read/Write-Check Header and Data command, a match of the sector header must be made before the data transfer is started. If the header compare inhibit (HCI bit 10 in RMOF) is set, the header will not be compared or checked and, like the Write Header and Data command, the transfer will be started based on the pre-recorded sector pulses. With the HCI bit set, header errors will not be reported. With the HCI bit cleared, the transfer will be aborted if a header error is detected. The Read/Write-Check Header and Data command aborts only the transfers following the sector that caused the error.

The desired sector, track and cylinder addresses are updated after the transfer of a sector. Therefore, at the end of a transfer, the disk is set up to transfer the next sequential sector. This allows multiple sector transfers and spiral transfers across tracks and cylinders. When the desired cylinder address changes during a transfer, the implied seek is performed and is termed a mid-transfer seek.

The data transfer commands are described below:

5.1.1 Write Check Data (51)

This command reads data from the selected drive and compares it on a word by word basis with that obtained from memory. If the data fails to compare, the WCE status bit is set and the command is terminated immediately. For additional information on write check errors see Section 4.10 and the WCE bit in Section 4.5.

5.1.2 Write Check Header and Data (53)

This command reads the header field and data field from the selected drive and compares it on a word by word basis with data obtained from memory. If the header and data fail to compare, the WCE status bit is set and the command is terminated immediately.

5.1.3 Write Data (61)

This command writes the 256-word data field of the selected sector with words obtained from memory. A two word ECC is appended to each sector. If the word count in RMWC goes to zero during the sector, the rest of the sector is zero filled. After a sector transfer the word count in RMWC is checked, and if not zero, the data transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit.

5.1.4 Write Header and Data (format operation) (63)

This command writes the 2-word header field and the 256-word data field of the selected sector with words obtained from memory. A one word CRC is appended to each header field, and a two word ECC is appended to each data field. After a sector transfer the word count in RMWC is checked, and if not zero, the data transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit. If RMWC goes to zero during the sector, the rest of the sector is zero filled.

5.1.5 Read Data (71)

This command reads the 256-word data field from the selected sector and transfers the data to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RMOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RMWC is checked; if not zero, the data transfer operation is repeated with the next sector. If RMWC goes to zero during the sector, the rest of the sector is not transferred.

5.1.6 Read Header and Data (73)

This command transfers the 2-word sector header field and the 256-word data field from the selected sector to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RMOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RMWC is checked; if not zero the data transfer operation is repeated with the next sector.

5.2 POSITIONING COMMANDS

Positioning commands are mechanical movement commands used to position the heads over the disk pack and take milliseconds to complete. Upon initiating the positioning commands, the controller will set the PIP bit and reset the DRY bit. Upon completion of the positioning operation, the controller resets the PIP and GO bits, sets the DRY bit and sets the ATA bit. The positioning commands are described below:

5.2.1 Seek Command (5)

This command causes the heads to be moved to the cylinder address specified by the contents of RMDC. When the controller sees the Seek command with the GO bit set, it sends the cylinder address to the corresponding drive. Any attempt to write into RMDC while the seek is in progress will cause the RMR bit to be set and RMDC will not be modified. Upon completion of the seek operation, the ATA and DRY bits in RMDS are set, and the GO bit is reset. If the drive is unable to complete a move within 500 milliseconds or if it has moved the carriage to a position outside the recording field, the drive asserts the seek error signal and the controller sets the SKI error bit in RMER2 and the ERR, ATA and DRY bits in RMDS. The controller will automatically issue a Fault Clear and a Return-to-Zero to the drive so that a Drive Clear command can clear the error.

5.2.2 Recalibrate (7)

This command will cause the drive positioner to position the heads over cylinder 0. A Return-to-Zero is automatically performed with each head load sequence, and whenever a Fault or Seek Error is detected. This command clears the OFM bit in RMDS.

5.2.3 Offset Command (15)

This command causes the OFM bit in RMDS to be set. Subsequent reads will be done with the heads offset from track centerline in the direction specified by RMOF bit 07. This operation offers additional data recovery attempts over that provided by the ECC capability when an ECC error is detected. If an ECC hard error occurs, two offset positions should be used. At the completion of the offset command, the ATA bit is set indicating that a read command should be issued to the cylinder and track in order to recover data.

The OFM bit in RMDS will be cleared by any one of the following:

a. Seek to another cylinder by means of implied or mid-transfer seek.
b. Write command.
c. Return-to-centerline command.
d. Recalibrate command.
e. Read-in preset command.

5.2.4 Return-to-Centerline Command (17)

This command is used to clear the OFM bit and set the ATA bit in RMDS.

5.2.5. Search Command (31)

The search command causes the controller to first perform a seek to the desired cylinder and then compare the sector counter with the desired sector in the RMDA register. When they match, it sets the ATA bit causing an interrupt to the computer if IE in RMCS1 is set. An unsuccessful completion of a search command occurs when a sector count and desired sector address match is not made during the interval of three index pulses, in which case the OPI bit is set.

5.3 HOUSEKEEPING COMMANDS

Housekeeping commands are used to place drive logic into a known or initialized state and usually take only a few microseconds to execute. The housekeeping commands are listed below.

5.3.1 NO OP (1)

This command does not perform any operation, except to clear the ATA bit.

5.3.2 Drive Clear (11)

This command causes the following registers and conditions associated with the drive selected by the unit select bits in RMCS2 to be cleared: ATA and ERR in RMDS, RMER1, RMER2, RMEC2, RMMR1 (except bit 03 which is set) and ATA bit in RMAS.

5.3.3 Release Command (13)

This command performs a drive clear function, and then releases the drive for use by the other port when in dual port mode of operation.

5.3.4 Read-In Preset (21)

This command sets the VV (volume valid) bit, clears the RMDC and RMDA registers, clears the RMOF register, and clears the OFM bit in the RMDS register.

5.3.5 Pack Acknowledge (23)

This command sets the VV bit for the command controller. This command or a Read-in Preset command must be issued before any data transfer or positioning command can be given if the pack has gone off-line and then on-line (i.e., MOL change of state). It is primarily intended to avoid unknown pack changes.

5.4 OPTIONAL COMMANDS

The Format, Transparent ECC Correction and RMWC Equals Sector Count commands can be executed only after writing a 1777777 into RMHR.

5.4.1 Boot (75)

This command executes a Return-to-Zero; clears RMDC and RMDA; sets the FMT16 bit in RMOF; set the Volume Valid bit in RMDS; and reads sector 0 (sectors 0 and 1 with firmware Revision G and above) of track 0 and cylinder 0 into memory starting at location 0. The bank of memory that the data is to be read into is determined from the memory extension bits.

The boot command is executed as follows:

1. Select a drive if one other than drive zero is to be used.
2. Execute a Pack Acknowledge by depositing a 23 into RMCS1.
3. Deposit a 1777777 into RMHR.
4. Deposit a 75 into RMCS1 to load the command into the controller.
5. Deposit a zero into R7.
6. Enter "Continue".

5.4.2 Format (77)

This command executes a Return-to-Zero; clears RMDC, and RMDA; and formats the entire pack in standard format. Each sector has bits 15, 14, and the FMT16 bit set in Header Word 1 and an all 0's data field. RMDC will be set to the last cylinder number plus one at completion, the LST bit in RMDS will be set, and the FMT16 bit in RMOF will be set.

5.4.3 DMA Bandwidth Set (25)

This command requires option switch SW1-7 to be ON. The switch has a dual purpose: it activates the DMA bandwidth control during DMA transfers, and it makes this command code legal. This command allows the program to alter the amount of delay time between DMA bursts on a drive-by-drive basis and is in addition to the standard delay. If ERR = 0 and DRY = 1 for the drive selected via RMCS2, then this op code takes the contents of RMWC, treats it as an unsigned 16-bit positive number, and saves it for use during subsequent data transfer operations. Each count equals a delay of 0.6 microseconds with a count of 0 = 1.5 microseconds. Any number in the range 0-65535(10) is legal. This results in a delay range of 1.5 microseconds to 39.33 milliseconds in 0.6 microsecond increments. Each drive is individually programmable, and a default count of nine (6.9 microseconds) is preset at power-up time. This feature is not available on the SC21/V1.

5.4.4 SC21/BE Special Features

Revisions B and above of the SC21/BE emulation incorporate the following special features: transparent ECC correction and RMWC equals sector count. Information on enabling and clearing these features is contained in the paragraphs below.

5.4.4.1 Transparent ECC Correction (37)

When this feature is enabled correctable ECC errors are fixed within the controller before the data is transferred to the memory on a Read, or Read Header and Data operation. Reading continues with the next sector if the data is ECC correctable. If the data is not ECC correctable, data transfers terminate with the bad sector, and an uncorrectable read error is flagged in the normal manner. Upon completion of the read, RMEC2 will contain the number of correctable ECC errors for the current command. It is preset to zero at the start of a read.

When disabled, read errors are handled in the normal manner and RMEC2 is not precleared. A cumulative corrected error count is maintained for each drive and may be read out of RMHR by writing a 100023 into RMHR. It is cleared only upon power up.

This feature may be enabled only when the controller has been conditioned for extended operations. Once this has been done, the transparent ECC correction may be enabled by executing op code 37. Because a separate flag exists in RMOF for each drive, the op code enables this feature only for the drive selected in RMCS2. Bit 2 of RMOF reflects the status of transparent ECC mode. A one indicates that the function is enabled.

5.4.4.2 RMWC Equals Sector Count (41)

When this feature is enabled, the contents of RMWC contain the number of sectors to be transferred, rather than the number of words. It is valid for Read, or Read Header and Data operation and for Write or Write Header and Data operation. Partial sector transfers cannot be done in this mode.

When disabled, RMWC contains a word count. The count is negative in both cases.

Once enabled, this command remains enabled until a controller clear or termination of any data transfer operation. Once this has been done, the RMWC equals sector count may be enabled by executing op code 41. Because a separate flag exists in RMOF for each drive, the op code enables this feature only for the drive selected in RMCS2. Bit 1 of RMOF reflects the status of RMWC equals sector count. A one indicates that the function is enabled.

5.4.4.3 Clearing the Special Features

The function flag is cleared under the following circumstances:

A. Selected drive only

1. Termination of a data transfer operation (regardless of its success).

2. Initiation of a Write Check operation (not valid for these modes).

3. Execution of a Read-In Preset command.

B. For all drives

1. Bus Init.

2. Controller clear.

3. Power up.

NOTE: A write to RMOF does not affect the two flags. Either of these two functions may be used separately or combined with one another. The flags may be set any time prior to a Read or Write operation for all drives on the system. Providing there is no occurrence of an intervening data transfer operation for a specific drive, the enabling of extended operations need be done only once. Because Write Check and Clear operations automatically reset the flags, the method of enabling the special features allows the user to use a common subroutine within his driver.

BLANK

6.1 INTRODUCTION

This section describes the modifications required in the Digital Equipment Corporation RM02/RM03 diagnostics to run on the Emulex SC21/B1 and other controllers in self-sizing mode. Once modified, these diagnostics will run on any current and future configurations generated for the following Emulex controllers:

Part one includes all known programming errors, and all modifications required to bypass unsupported portions of the DEC maintenance mode. Part two are the self-sizing modifications.

6.2 CZRMJB0 RM03/RM02 Diskless Diagnostic

Product Code: AC-B018B-MC

This diagnostic runs exclusively in maintenance mode. Since only a subset of the RM02 maintenance mode features are emulated in the Emulex controller, this diagnostic is not run.

6.3 CZRMCB0 RM03/RM02 Functional Test - Part 1

Product Code: AC-A9997B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	25024, 25026	4737, 43216	137,25622
2.	10730	40001	0
3.	13062	1012	412
4.	26600	1007	407
5.	27014	1011	411
6.	35570	1406	406
7.	45152	4	10
8.	60000	7	1405
9.	66074	13746	12746
10.	10356-10362	5007, 110102, 1	11102, 105002, 240

Item — Explanation

1. This modification bypasses an OPI test to comply with DEC hardware ECOs #7684-0004, 7684-0007, 7684-0009.

2. This modification is only required on very fast processors. It changes a Drive Clear test to run in normal mode instead of maintenance mode.

3. This modification bypasses a "lost of bit clock" test which is run in maintenance mode.

4. This modification bypasses an "RMR" test which, as written, can only be run in maintenance mode.

5. This modification bypasses a Massbus Parity Error test. Since there is no massbus on the Emulex controller, there is no massbus parity to test.

6. This modification bypasses a test of the RMLA register that is done in 18-bit mode.

7-10. Unidentified program bugs.

MODIFICATIONS (Part 2)

*Note: Required on SC21/BF only. Limits test to units 0-3.

Location	From	To
6116	7	3*
6706	67	63*
6746	377	17*
7634	24024	20024
7654	24025	20027
7732-7734	12706, 1100	4737, 104106
27500-27502	12737, 1466	13737, 104400
30522-30524	22726, 1000	23726, 104400
31372-31374	12737, 1466	13737, 104400
32022-32024	12737, 1466	13737, 104400
32240-32242	22737, 1466	23737, 104400
32730-32732	12737, 2400	13737, 104410
33224	3400	37400
33250-33252	12737, 2400	13737, 104410
33344-33346	12737, 1467	13737, 104402
33636	2000	4000
33662-33664	12737, 1467	13737, 104402
36364	633	40
36370	634	41
36754	634	40
36760	633	41
37436-37440	12737, 2400	13737, 104410
37700	4000	40000
37724-37726	12737, 2400	13737, 104410
40032-40034	12737, 1467	13737, 104402
40304	2000	4000
40330-40332	12737, 1467	13737, 104402
51114	177770	177700
51134-51140	23727, 51702, 240	23737, 51702, 104412
51150-51152	162737, 5	163737, 104412

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51224-51226	22737, 1467	23737, 104402
51340-51342	22737, 1467	23737, 104402
51600	176000	170000
52236-52242	23727, 1432, 1466	23737, 1432, 104400
52304-52310	123727, 1405, 4	123737, 1405, 104404
57730-57736	23727, 1432, 1466	23737, 1432, 104400
57776-60002	123727, 7, 4	123737, 1405, 104404

The following subroutine must be inserted where indicated. The previous contents of the locations should all be zeros.

Locations: 104106-104174

Contents: 13700, 1276, 062700, 36, 12701, 104400, 12710, 100027, 11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221, 105021, 116121, 177775, 12710, 100036, 16100, 177776, 6200, 6200, 6200, 10011, 207.

6.4 CZRMDB0 RM03/RM02 Functional Test - Part 2

Product Code: AC-B000B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	40452	4	10
2.	63360	13746	12746

Both of the above modifications correct unidentified program bugs.

MODIFICATIONS (Part 2)

*Note: Required on SC21/BF only. Limits test to units 0-3.

Location	From	To
6134	7	3*
6724	67	63*
6764	377	17*
7656	24024	20024
7674	24025	20027
7732-7734	12700, 1100	4737, 101550
17514-17516	12737, 2037	13737, 102514
20374-20376	12737, 1466	13737, 102500
22272-22274	22737, 2000	23737, 102506
22300	103402	101402
23014-23016	22737, 1466	23737, 102500
23076-23100	12737, 1466	13737, 102500
23104-23106	12737, 2037	13737, 102514
23374-23376	12737, 1466	13737, 102500
23402-23404	12737, 2037	13737, 102514

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24406-24410	12737, 2400	13737, 102510
25066	3400	37400
25126-25130	12737, 1467	13737, 102502
25614	1777	3777
34714	5737	0
36766-36770	122763, 4	123763, 102504
44414	177770	177700
44434-44440	23727, 45202, 240	23737, 45202, 102512
44450-44452	162737, 240	163737, 102512
44474-44500	23727, 45200, 5	23737, 45200, 102506
44510-44512	162737, 5	163737, 102506
44524-44526	22737, 1467	23737, 102502
44640-44642	22737, 1467	23737, 102502
45100	176000	170000
45536-45542	23727, 1434, 1466	23737, 1434, 102500
45604-45610	123727, 1407, 4	123737, 1407, 102506
53764-53766	22737, 1466	23737, 102500
54002-54004	122737, 4	123737, 102504

The following subroutine must be inserted where indicated. The previous contents of the locations should be all zeros.

Location: 101550-10646

Contents: 13700, 1276, 62700, 36, 12701, 102500, 12710, 100027, 11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221, 105021, 116121, 177775, 12710, 100036, 16100, 177776, 6200, 6200, 6200, 10021, 112721, 37, 116111, 177767, 207.

6.5 CZRMEB0 RM03/RM02 Functional Test - Part 3

Product Code: AC-B003B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	31032	42702	52702
2.	30070, 30072	404, 240	402, 0
	30076,30100	137, 30470	5237, 1336
3.	30416, 30420,	404, 240	402, 0
	30424, 30426	137, 30470	5237, 1336
4.	44472	4	10
5.	67364	13746	12746

Item — Explanation

1. This modification reverses a DEC patch that eliminated bus-address-increment-inhibit mode in a write test. The DEC controller gets Data Late errors in this mode. The Emulex controllers do not.

2. This modification increments the saved contents of RMDA after attempting a write with the ERR bit in RMDS set. The DEC controller increments RMDA during the illegal attempt. Emulex controllers do not. The modification allows a subroutine to pass the test.

3. Same as Item 2, except that this is for an attempted read with ERR set.

4-5. Unidentified program bugs.

MODIFICATIONS (Part 2)

*Note: Required on SC21/BF only. Limits test to units 0-3.

Location	From	To
6110	7	3*
6700	67	63*
6740	377	17*
7632	24024	20024
7652	24025	20027
7706-7710	12706, 1100	4737, 111760
20040-20042	12737, 1466	13737, 112100
20444-20442	12737, 1466	13737, 112100
22076-22100	12737, 2037	13737, 112114
32604-32610	23727, 1434, 1400	23737, 1434, 112100
32710-32712	12737, 2037	13737, 112114
36722-36724	22737, 2037	23737, 112114
41000-41002	12737, 2000	13737, 112116
41006-41010	12737, 1466	13737, 112100
42012-42014	12737, 2012	13737, 112120
42426-42430	112737, 4	123737, 112104
42446-42450	22737, 1466	23737, 112100
42516-42520	122737, 4	123737, 112104
42536-42540	22737, 1466	23737, 112100
43006-43010	122763, 4	123763, 112104
50434	177770	177700
50454-50460	23727, 51222, 240	23737, 51222, 112112
50470-50472	162737, 240	163737, 112112
50514-50520	23727, 51220, 5	23737, 51220, 112106
50530-50532	162737, 5	163737, 112106
50544-50546	22737, 1467	23737, 112102
50660-50662	22737, 1467	23737, 112102
51120	176000	170000
51556-51562	23727, 1434, 1466	23737, 1434, 112100
51624-51630	123727, 1407, 4	123737, 1407, 112104
60004-60006	22737, 1466	23737, 112100
60022-60024	122737, 4	123737, 112104

The following subroutine must be added to the test at:

Locations: 111760-112052

Contents: 13700, 1276, 62700, 36, 12701, 112100, 12710, 100027, 11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221, 105021, 116121, 177775, 12710, 100036, 16100, 177776, 6200, 6200, 6200, 10021, 112721, 37, 116121, 177767, 105021, 116121, 177776, 112721, 12, 116111, 177776, 207.

6.6 CZRMFB0 RM03/RM02 Extended Drive Test

Product Code: AC-B0006B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	21464	13746	12746
2.	27722-27726	5737, 4322, 1011	32737, 100000, 4350
	27730-27734	32737, 100000, 4350	1405, 12737, 177777
	27736-27742	1405, 12737, 177777	1446, 137, 30370
	27744-27750	1446, 137, 30370	5737, 4322, 1401
3.	37246	1750	1503
4.	37604	10164	110164
5.	41674	10164	110164
6.	43064-43066	5702, 1426	4737, 44770
	43070-43072	4737, 44770	5702, 1424

All of the above are unidentified program bugs.

MODIFICATIONS (Part 2)

*Note: Required on SC21/BF only. Limits test to units 0-3.

**Note: Required on drives of less than 100 logical cylinders only

Location	From	To
1774	400	1466
2040	400	1466
2176	144	100**
37116	177770	177774*
37124	7	3*
37270-37272	22705, 20024	122705, 24
37276-37300	22705, 24024	122705, 27
37312-37314	22705, 20025	122705, 25
37320-37322	22705, 24025	122705, 25
5714	10	4*
17574-17576	20127, 1466	20137, 1574
17602-17604	20227, 4	20237, 1602
17022-17026	22700, 5, 3365	23700, 1602, 2365

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17222-17224	122737, 4	123737, 1602
20312-20314	122737, 5	123737, 1602
20320	3370	2370
33530-33534	122702, 5, 3003	123702, 1602, 2003

The following subroutine must be inserted where indicated. It replaces an existing subroutine of similar function that is no longer needed. The contents of the existing routine are not shown.

Locations: 26632-27004

Contents: 104412, 113704, 1102, 6304, 16401, 1620, 13704, 1450, 62704, 36, 12702, 1566, 5003, 12122, 6237, 1566, 103002, 12122, 401, 5022, 5203, 20327, 14, 1405, 20327, 3, 1363, 24242, 761, 12714, 100027, 11405, 12703, 1574, 5713, 1412, 21327, 1466, 1407, 21327, 1465, 1002, 5305, 402, 20513, 2001, 10513, 12714, 100030, 11437, 1602, 104413, 207.

6.7 CZRMIB0 RM03/RM02 Drive Compatibility Test

Product Code: AC-B015B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	21000	13746	12746

The above item is an unidentified program bug.

There are no Part 2 modifications to this test. It is impractical to rewrite this test. To do so would require allocating an indeterminate amount of buffer space near the beginning of the test. The test uses cylinders 0-800 (but not all of them), and tracks 0-4. Any configuration with 801 or more cylinders and 5 or more tracks is compatible with this test.

6.8 CZRMAC0 RM03/RM02 Formatter

Product Code: AC-9252C-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	12632	10011	1
2.	23630	13746	12746
3.	27154	1750	1503
4.	27512	10164	110164
5.	31602	10164	110164
6.	32772-32774	5702, 1426	4737, 34676
	32776-33000	4737, 34676	5702, 1424

Item	Explanation
1.	This modification alters the number of tracks that must be formatted before a bad sector file can be written. Since the format OP code does not write a bad sector file, and since the Performance Exerciser will not run without one, this modification allows any size format or verify to create a bad sector file. If the number is not altered, then the entire pack must be formatted before a bad sector file can be written.
2-6.	Unidentified program bugs.

MODIFICATIONS (Part 2)

Location	From	To
30044	4037	406
11260-11262	112737, 4	113737, 31472
11266-11270	12737, 1466	13737, 31470
11510-11512	22737, 151466	23737, 31466
11520-11522	22737, 2000	23737, 31464
12530-12532	12702, 1466	13702, 31470
12560-12562	12737, 5	13737, 5660
12612-12614	62737, 5	63737, 5660
15200-15202	22737, 1466	23737, 31470
15210-15212	122737, 4	123737, 31472
15402-15404	12737, 1466	12737, 31470
15410-15412	112737, 4	113737, 31472
16410-16412	22737, 4	23737, 31472
16430-16432	22737, 1466	23737, 31470
16440-16442	122737, 4	123737, 31472
16502-16504	22737, 1467	23737, 5652
20070-20072	12737, 1466	13737, 31470
20076-20100	12737, 4	13737, 31472
27176-27200	22705, 20024	122705, 24
27204-27206	22705, 24024	122705, 27
27220-27222	22705, 20025	122705, 25
27226-27230	22705, 24025	122705, 25
10734-10740	12737, 1466, 1320	104412, 13703, 26644
10742-10746	132762, 3, 26526	13702, 1220, 10263
10750-10752	1003, 12737	10, 4737
10754-10756	1466, 1320	31320, 104413

The following subroutine must be inserted where indicated. It replaces a rotational position sensing routine that the formatter does not need since it only formats one drive at a time. The contents of the existing routine are not shown.

Locations: 31320-31452

Contents: 62703, 36, 12713, 100027, 11304, 12713, 100030, 11305, 12713, 100036, 10437, 1320, 10537, 1324, 12703, 31464, 105023, 110523, 10413, 52723, 150000, 10423, 10523, 5204, 5205, 10437, 5652, 10537, 5660, 10437, 5666, 10537, 5674, 10437, 5704, 10537, 5712, 10437, 5730, 10537, 5736, 10437, 5754, 10537, 5762, 207.

6.9 CZRMBB0 RM03/RM02 Performance Exerciser

Product Code: AC-A994B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	11134-11136	400, 46116	100000, 46144
2.	32144	13746	12746
3.	35130	1750	1503
4.	35466	10164	110164
5.	37556	10164	110164
6.	41036-41040	5702, 1426	4737, 34676
	41042-41044	4737, 34676	5702, 1424

All of the above items are unidentified program bugs.

MODIFICATIONS (Part 2)

Location	From	To
4440	57512	60410
4472	57512	60410
6364-6366	22760, 1465	26060, 106
13534-13540	123727, 1415, 5	240, 4737, 60304
13554-13560	23727, 1412, 151466	240, 4737, 60230
16654-16656	62705, 5	66005, 112
16672-16676	20527, 4, 101402	26005, 112, 3002
16700-16702	162705, 5	16005, 112
22614-22616	112766, 4	116066, 112
25442-25446	10004, 62704, 2	10046, 4737, 60064
25664	12737	402
25762-25764	16403, 55252	4737, 60206
26214-26220	12737, 1466, 40674	240, 4737, 60262
26222-26226	112737, 4, 46073	240, 4737, 60326
35152-35154	22705, 20024	122705, 24
35160-35162	22705, 24024	122705, 27
35174-35176	22705, 20025	122705, 25
35202-35204	22705, 24025	122705, 25

The following subroutine must be added to the end of the program at the indicated locations.

Locations: 60064-60204

Contents: 10146, 111001, 13704, 34620, 4037, 35050, 401, 403, 105761, 34512, 1375, 105761, 34472, 3424, 62704, 36, 6301, 6301, 62701, 60350, 12714, 100027, 11421, 11400, 5300, 10037, 1446, 12714, 100030, 11421, 11437, 1444, 12714, 100036, 12601, 16604, 2, 12600, 62704, 2, 200.

Locations: 60206-60346

Contents: 16403, 55252, 13763, 1444, 16, 13763, 1444, 24, 207, 5046, 111016, 6316, 6316, 67716, 60350, 13646, 52716, 150000, 5216, 22637, 1412, 207, 5046, 111016, 6316, 6316, 62716, 60350, 13637, 46074, 207, 5046, 111016, 6316, 6316, 62716, 60352, 123637, 1415, 207, 5046, 111016, 6316, 6316, 62716, 60352, 113637, 46073, 207.

Those users running on drives with more than 80 MB capacity will require the following patches. The Performance Exerciser limits the number of allowable bad sectors on any drive to 16, even though the Bad Sector File can handle 126. The following patches allow the program to run with 126 bad sectors or less. The first two patches move the base address of the buffer. These locations have already been patched, and the "from" column reflects those patches.

Location	From	To
4440	60410	70410
4472	60410	70410
17202	20	176
17206	62702	16002
20274	12701	16001
20300	60001	240
20304	20	176
25504	14	22
25510	162	154
25716	122	126
26166	62701	16001
26174	40	400
26344	62701	16001
26352	40	400
43146	0	60410
43452	0	61410
43756	0	62410
44262	0	63410
44566	0	64410
45072	0	65410
45376	0	66410
45702	0	67410

6.10 CZRMGB0 RM03/RM02 Dual Port Logic Test - Part 1

Product Code: AC-B009B-MC

See note under Dual Port Logic Test - Part II.

6.11 CZRMHB0 RM03/RM02 Dual Port Logic Test - Part 2

Product Code: AC-B012B-MC

Neither Dual Port Logic Test can be run. They require that the drive under test be tied to a single controller via a special cable from the second port, and that the drive have a "neutral" position. The neutral position allows any asynchronous request via either port to immediately seize the drive without having to wait for it. This controller does not have the ability to examine any drive at any given moment since only one drive can be addressed at a time via the A cable. Therefore, with this controller a "neutral" position must appear as a "busy" to both controllers. The lack of an immediately seizable state will cause errors in almost all of the sub-tests in each of the dual controller logic diagnostics.

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APPENDIX A

SC21/B1 CONFIGURATION AND OPTION SELECTION

A.1 INTRODUCTION

To allow the user of the SC21/B1 the greatest amount of flexibility in selecting disk drives for his system, the SC21/B1 supports a wide variety of disk types and offers a number of other user selectable options. This appendix is designed as a quick reference to the various switches which make this flexibility possible.

A.2 CONTROLLER CONFIGURATION

The SC21/B1 unit is capable of controlling a wide variety of disk drives of various sizes and types. The various drives that are supported are defined by the Configuration PROM. Table A-1 is a list of the drive types and sizes that are supported. The user may choose between the available options by means of configuration switch SW2. The correct switch settings for each of the various configurations are given in Table A-2.

A.2.1 Physical vs Logical Disk Numbering

There is no mapping of logical disks onto physical disks of different numbers. That is, logical unit zero corresponds to physical unit zero, and so on. In cases where the capacity of the physical unit is greater than the standard capacity of the disk subsystem that is being emulated the operating system drivers must be patched to reflect the increased block counts. See the Emulex Patch Document (P/N PD9951002) for patch instructions.

A.2.2 Drive Configuration Selection

The SC21/B1 emulates three different DEC disk subsystems, the RM02, the RM03 and the RM05. Both the RM02 and the RM03 subsystems have an unformatted capacity of 80 Mb. The RM05 has an unformatted capacity of 300 Mb.

Each subsystem type is represented by a drive type code in Table A-2. The number 25 represents an RM02, 24 represents an RM03, and 27 an RM05. These numbers are preceded in Table A-2 by a configuration key that represents the make and size of the physical drive that is used to emulate the DEC subsystem. The configuration key is taken from Table A-1. For example, an 80 Mb CDC 9762 is often used as a standard RM02 and would be represented in Table A-2 like this: 80C/25. An 300 Mb CDC 9766 with a RM05 assigned to it would be represented like this: 300C/27.

If the drive type code for an RM02 is paired with a drive that has a greater capacity than does a normal RM02 (80 Mb), the emulation is said to be expanded. That is, an expanded RM02 emulation would have an unformatted capacity of 300 Mb if assigned to a 300 Mb CDC 9300. Such a configuration would be represented in Table A-2 as 300A/25. Because this is a non-standard size for that particular drive type code, the host's operating system must be patched with the larger maximum block count for the expanded RM02. Instructions for patching the software are included in the Emulex Patch Document (P/N PD9951002).

There are several standard configurations offered that require no software patching to operate. These configurations emulate RM02, RM03 or RM05 disk subsystems, either by themselves or in combination. The standard RM02, RM03 or RM03 configurations are marked in Table A-2.

To find the configuration switch setting that is suitable for your disk installation, use the following process. Note that all configurations require that the drives be set with 32 hard sectors. See the drive manufacturer's installation manual for instructions. Note also that use of a Trident type drive requires that SW1-9 be closed.

1. Locate your drive type and size in Table A-1. Note down the configuration key assigned to your drive. If you intend to use more than one type of drive, note down their assigned keys as well.

2. Find the configuration number for the type of drive you wish to use as logical unit zero in the Drive 0 column of Table A-2. If you wish to avoid patching the software, then only use the configurations marked with a super scripted one (00^1, for example). The marked settings are standard emulations.

3. When you find a suitable match for Drive 0, check the drive key and type for Drives 1, 2 and 3 for that configuration row. You do not need to use all four drive ports.

4. When you find a suitable configuration, set the Configuration Switches (SW2) as indicated in Table A-2.

TABLE A-1
DRIVES SUPPORTED

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
80C	823	5	32	9762, 9730-80, 980, T82RM
160C	823	10	32	9730-160
160CM	1646	5	32	9730-160 - mapped
160A	1645	5	32	9160
300C	823	19	32	9766, 9300, T302RM

TABLE A-1, cont.

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
500T	1348	19	32	T602
600C	842	40	32	9775
600CM	1684	19	32	9775-mapped
84FJ	589	7	32	M2312
40C	411	5	32	9760
150C	411	19	32	9764
300A	815	19	32	9300
160T	700	12	32	SAPPHIRE 160
330A	1024	16	32	330

TABLE A-2
DRIVE CONFIGURATION PROM NO. 012

	SW2-					Logical-Physical[2]				
Octal	5	4	3	2	1	Drive 0	Drive 1	Drive 2	Drive 3	Rev.
00[1]	O	O	O	O	O	80C/25	80C/25	80C/25	80C/25	A
01	O	O	O	O	C	160C/25	160C/25	160C/25	160C/25	A
02	O	O	O	C	O	160A/25	160A/25	160A/25	160A/25	A
03	O	O	O	C	C	500T/25	500T/25	500T/25	500T/25	A
04	O	O	C	O	O	300C/25	300C/25	300C/25	300C/25	A
05[1]	O	O	C	O	C	300C/27	300C/27	300C/27	300C/27	A
06	O	O	C	C	O	600C/25	600C/25	600C/25	600C/25	A
07	O	O	C	C	C	300A/25	300A/25	300A/25	300A/25	C
10	O	C	O	O	O	80C/25	80C/25	160CM/24	160CM/24	B
11[1]	O	C	O	O	C	80C/25	80C/25	300C/27	300C/27	B
12	O	C	O	C	O	80C/25	80C/25	600CM/27	600CM/27	B
13[3]	O	C	O	C	C	300C/25	300C/25	600CM/24	600CM/24	B
14	O	C	C	O	O	300C/27	300C/27	600C/25	600C/25	B
15[3]	O	C	C	O	C	80C/25	80C/25	300C/27	600C/24	E
16[1]	O	C	C	C	O	300C/27	80C/25	80C/25	80C/25	G
17[1]	O	C	C	C	C	300C/27	300C/27	80C/25	80C/25	G
20	C	O	O	O	O	80C/25	160CM/24	160CM/24	160CM/24	B
21[1]	C	O	O	O	C	80C/25	300C/27	300C/27	300C/27	B
22	C	O	O	C	O	80C/25	600CM/27	600CM/27	600CM/27	B
23	C	O	O	C	C	300C/25	600CM/24	600CM/24	600CM/24	B
24	C	O	C	O	O	300C/27	600C/25	600C/25	600C/25	B
25[3]	C	O	C	O	C	300A/25	600C/24	600C/24	600C/24	F
26	C	O	C	C	O	300A/27	330A/25	300A/27	330A/25	G
27	C	O	C	C	C	160CM/25	160CM/25	300C/27	300C/27	G
30[1]	C	C	O	O	O	80C/25	80C/25	80C/25	300C/27	G
31	C	C	O	O	C	84FJ/25	84FJ/25	84FJ/25	84FJ/25	C
32	C	C	O	C	O	40C/25	40C/25	40C/25	40C/25	C
33	C	C	O	C	C	150C/25	150C/25	150C/25	150C/25	C

TABLE A-2, cont.

Octal	SW2-5	4	3	2	1	Logical-Physical[2] Drive 0	Drive 1	Drive 2	Drive 3	Rev.
34[3]	C	C	C	O	O	84FJ/24	84FJ/24	84FJ/24	80C/25	H
35[3]	C	C	C	O	C	84FJ/24	84FJ/24	84FJ/24	80C/25	J
36	C	C	C	C	O	330A/25	330A/25	330A/25	330A/25	F
37	C	C	C	C	C	160T/25	160T/25	160T/25	160T/25	F

[1]Standard configurations; no software patching required.

[2]Table entries: Drive Key/Drive Type Code.

[3]Configurations cannot be used with RSTS/E operating system.

C = sw. closed; O = sw. open.

TABLE A-3
DRIVES SUPPORTED BY ALTERNATE CONFIGURATION PROM (#898)

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
80C	823	05	32	Ampex 9380, Century T82RM, CDC 9730-80, CDC9762
160C	823	10	32	CDC 9730-160, Fujitsu 2284
330A	1024	16	32	Ampex 330, Fujitsu 2294

TABLE A-4
DRIVE CONFIGURATIONS FOR
ALTERNATE CONFIGURATION PROM (#898)

Octal	SW2-5	4	3	2	1	Logical-Physical[1] Drive 0	Drive 1	Drive 2	Drive 3	Rev.
00	O	O	O	O	O	160C/24	160C/24	160C/24	330A/25	A
01	O	O	O	O	C	160C/25	160C/25	330A/27	330A/27	B
02	O	O	O	C	O	80C/25	80C/25	160C/25	160C/25	C

[1]Table entries: Drive Key/Drive Type Code.

C = Closed (ON), O = Open (OFF)

A.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC21/B1 can be user selected. The functions of the switches that select those options are defined in Tables A-5, A-6, A-7, and A-8 below.

TABLE A-5
OPTION SWITCH SW1 SETTINGS

Option Sw	Open	Closed	Function
SW1-1			Interrupt vector address select[2]
SW1-2			Interrupt vector address select[2]
SW1-3	0-3	4-7	Select logical units (Rev. D and above)
SW1-4			Not used[1]
SW1-5	Disable	Enable	Checksum enable for data transfers
SW1-6	Disable	Enable	Dual port mode
SW1-7	Disable	Enable	DMA Bandwidth Control
SW1-8	B Cable	A Cable	Sector and Index signals
SW1-9	Disable	Enable	CDS Trident drive compatability
SW1-10			Not used[1]

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.4.2.

TABLE A-6
OPTION SWITCH SW2 SETTINGS

Option Sw	Open	Closed	Function
SW2-1			Drive configuration[2]
SW2-2			Drive configuration[2]
SW2-3			Drive configuration[2]
SW2-4			Drive configuration[2]
SW2-5			Drive configuration[2]
SW2-6			Register address selection[3]
SW2-7			Register address selection[3]
SW2-8			Register address selection[3]
SW2-9			Register address selection[3]
SW2-10			Not used[1]

[1]All unused switches MUST BE OFF.

[2]See TABLES A-2 and A-4.

[3]See TABLE A-7.

TABLE A-7
ADDRESS SWITCH SETTINGS

SWITCH SW2 -9	-8	-7	-6	PROM #192 (Standard)	PROM #597 (Optional)	PROM #793 (Optional)	
O	O	C	O	776700[2]	776700[3]	776700[3]	Standard
C	O	O	O	776300[2]	776300[3]	776300[3]	Alternate
O	O	O	C	Not used[1]	776100[3]	776600[3]	Alternate
O	C	O	O	Not used[1]	775300[3]	Not used[1]	Alternate

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.4.1.

[3]This address available with option kit. See paragraph 3.4.1.1.

TABLE A-8
OPTION SWITCH SW3 SETTINGS

Option Sw	Open	Closed	Function
SW3-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW3-2			Not used[1]
SW3-3	5.1 usec.	20.4 usec.	Delay time if DMA burst suspended (Rev. E and above)
SW3-4			Not used[1]

[1]All unused switches MUST BE OFF.

APPENDIX B

SC21/V1 CONFIGURATION AND OPTION SELECTION

B.1 INTRODUCTION

To allow the user of the SC21/V1 the greatest amount of flexibility in selecting disk drives for his system, the SC21/V1 supports a wide variety of disk types and offers a number of other user selectable options. This appendix is designed as a quick reference to the various switches and jumpers which make this flexibility possible. For more detailed information about user selectable options see the Installation chapter in this manual.

B.2 CONTROLLER CONFIGURATION

The SC21/V1 unit is capable of controlling a wide variety of disk drives of various sizes and types. The various drives that are supported are defined by the Configuration PROM. Table B-1 is a list of the drive types and sizes that are supported. The user may choose between the available options by means of configuration switch SW2. The correct switch settings for each of the various configurations are given in Table B-2.

B.2.1 Physical vs Logical Disk Numbering

There is no mapping of logical disks onto physical disks of different numbers. That is, logical unit zero corresponds to physical unit zero, and so on. In cases where the capacity of the physical unit is greater than the standard capacity of the disk subsystem that is being emulated the operating system drivers must be patched to reflect the increased block counts. See the Emulex Patch Document (P/N PD9951002) for patch instructions.

B.2.2 Drive Configuration Selection

The SC21/V1 emulates three different DEC disk subsystems, the RM02, the RM03 and the RM05. Both the RM02 and the RM03 subsystems have an unformatted capacity of 80 Mb. The RM05 has an unformatted capacity of 300 Mb.

Each subsystem type is represented by a drive type code in Table B-2. The number 25 represents an RM02, 24 represents an RM03, and 27 an RM05. These numbers are preceded in Table B-2 by a configuration key that represents the make and size of the physical drive that is used to emulate the DEC subsystem. The configuration key is taken from Table B-1. For example, an 80 Mb CDC 9762 is often used as a standard RM02 and would be represented in Table B-2 like this: 80C/25. An 300 Mb CDC 9766 with a RM05 assigned to it would be represented like this: 300C/27.

If the drive type code for an RM02 is paired with a drive that has a greater capacity than does a normal RM02 (80 Mb), the emulation is said to be expanded. That is, an expanded RM02 emulation would have an unformatted capacity of 300 Mb if assigned to a 300 Mb Ampex 9300. Such a configuration would be represented in Table B-2 as 300A/25. Because this is a non-standard size for that particular drive type code, the host's operating system must be patched with the larger maximum block count for the expanded RM02. Instructions for patching the software are included in the Emulex Patch Document (P/N PD9951002).

There are several standard configurations offered that require no software patching to operate. These configurations emulate RM02, RM03 or RM05 disk subsystems, either by themselves or in combination. The standard RM02, RM03 or RM03 configurations are marked in Table B-2.

To find the configuration switch setting that is suitable for your disk installation, use the following process. Note that all configurations require that the drives be set with 32 hard sectors. See the drive manufacturer's installation manual for instructions. Note also that use of a Trident type drive requires that SW1-9 be closed.

1. Locate your drive type and size in Table B-1. Note down the configuration key assigned to your drive. If you intend to use more than one type of drive, note down their assigned keys as well.

2. Find the configuration number for the type of drive you wish to use as logical unit zero in the Drive 0 column of Table B-2. If you wish to avoid patching the software, then only use the configurations marked with a super scripted one (00^1, for example). The marked settings are standard emulations.

3. When you find a suitable match for Drive 0, check the drive key and type for Drives 1, 2 and 3 for that configuration row. You do not need to use all four drive ports.

4. When you find a suitable configuration, set the Configuration Switches (SW2) as indicated in Table B-2.

TABLE B-1
DRIVES SUPPORTED

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
80C	823	5	32	9762, 9730-80, 980, T82RM
160C	823	10	32	9730-160
160CM	1646	5	32	9730-160 - mapped
160A	1645	5	32	9160
300C	823	19	32	9766, 9300, T302RM

TABLE B-1, cont.

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
500T	1348	19	32	T602
600C	842	40	32	9775
600CM	1684	19	32	9775-mapped
84FJ	589	7	32	M2312
40C	411	5	32	9760
150C	411	19	32	9764
300A	815	19	32	9300
160T	700	12	32	SAPPHIRE 160
330A	1024	16	32	330

TABLE B-2
DRIVE CONFIGURATION PROM NO. 012

	SW2-					Logical-Physical[2]				
Octal	5	4	3	2	1	Drive 0	Drive 1	Drive 2	Drive 3	Rev.
00[1]	O	O	O	O	O	80C/25	80C/25	80C/25	80C/25	A
01	O	O	O	O	C	160C/25	160C/25	160C/25	160C/25	A
02	O	O	O	C	O	160A/25	160A/25	160A/25	160A/25	A
03	O	O	O	C	C	500T/25	500T/25	500T/25	500T/25	A
04[1]	O	O	C	O	O	300C/25	300C/25	300C/25	300C/25	A
05[1]	O	O	C	O	C	300C/27	300C/27	300C/27	300C/27	A
06	O	O	C	C	O	600C/25	600C/25	600C/25	600C/25	A
07	O	O	C	C	C	300A/25	300A/25	300A/25	300A/25	C
10[1]	O	C	O	O	O	80C/25	80C/25	160CM/24	160CM/24	B
11[1]	O	C	O	O	C	80C/25	80C/25	300C/27	300C/27	B
12	O	C	O	C	O	80C/25	80C/25	600CM/27	600CM/27	B
13	O	C	O	C	C	300C/25	300C/25	600CM/24	600CM/24	B
14	O	C	C	O	O	300C/27	300C/27	600C/25	600C/25	B
15[1]	O	C	C	O	C	80C/25	80C/25	300C/27	600C/24	E
16[1]	O	C	C	C	O	300C/27	80C/25	80C/25	80C/25	G
17[1]	O	C	C	C	C	300C/27	300C/27	80C/25	80C/25	G
20[1]	C	O	O	O	O	80C/25	160CM/24	160CM/24	160CM/24	B
21[1]	C	O	O	O	C	80C/25	300C/27	300C/27	300C/27	B
22	C	O	O	C	O	80C/25	600CM/27	600CM/27	600CM/27	B
23	C	O	O	C	C	300C/25	600CM/24	600CM/24	600CM/24	B
24	C	O	C	O	O	300C/27	600C/25	600C/25	600C/25	B
25	C	O	C	O	C	300A/25	600C/24	600C/24	600C/24	F
26	C	O	C	C	O	300A/27	330A/25	300A/27	330A/25	G
27[1]	C	O	C	C	C	160CM/25	160CM/25	300C/27	300C/27	G
30[1]	C	C	O	O	O	80C/25	80C/25	80C/25	300C/27	G
31	C	C	O	O	C	84FJ/25	84FJ/25	84FJ/25	84FJ/25	C
32	C	C	O	C	O	40C/25	40C/25	40C/25	40C/25	C
33	C	C	O	C	C	150C/25	150C/25	150C/25	150C/25	C

TABLE B-2, cont.

Octal	SW2- 5	4	3	2	1	Logical-Physical[2] Drive 0	Drive 1	Drive 2	Drive 3	Rev.
34	C	C	C	O	O	84FJ/24	84FJ/24	84FJ/24	80C/25	H
35	C	C	C	O	C	84FJ/24	84FJ/24	84FJ/24	80C/25	J
36	C	C	C	C	O	330A/25	330A/25	330A/25	330A/25	F
37	C	C	C	C	C	160T/25	160T/25	160T/25	160T/25	F

[1]Standard configurations; no software patching required.

[2]Table entries: Drive Key/Drive Type Code.

C = sw. closed; O = sw. open.

TABLE B-3
DRIVES SUPPORTED BY ALTERNATE CONFIGURATION PROM (#986)

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
80C	823	5	32	Ampex 9380, CDC 9730-80, Century T82RM, CDC 9762
81C	815	5	32	Century T82F
129	1121	7	32	Priam 15450
160C	823	10	32	CDC 9730-160, Fujitsu 2284
300A	815	19	32	Ampex 9300
300C	823	19	32	Century T302RM, CDC 9766
330A	1024	16	32	Ampex 330, Fujitsu 2294
340	711	24	32	CDC 9715-340
600C	842	40	32	CDC 9775

TABLE B-4
DRIVE CONFIGURATIONS FOR
ALTERNATE CONFIGURATION PROM (#986)

	SW2-					Logical-Physical[1]				
Octal	5	4	3	2	1	Drive 0	Drive 1	Drive 2	Drive 3	Rev.
00	O	O	O	O	O	160C/24	160C/24	160C/24	330A/25	A
01	O	O	O	O	C	80C/25	160C/24	160C/24	160C/24	A
02	O	O	O	C	O	80C/25	80C/25	160C/24	160C/24	A
03	O	O	O	C	C	160C/25	160C/25	300C/27	300C/27	A
04	O	O	C	O	O	160C/25	600C/25	600C/25	600C/25	A
05	O	O	C	O	C	300A/27	80C/25	80C/25	80C/25	B
06	O	O	C	C	O	80C/25	80C/25	80C/25	160C/25	C
07	O	O	C	C	C	80C/25	330A/27	330A/27	330A/27	D
10	O	C	O	O	O	330A/27	330A/27	80C/25	80C/25	E
11	O	C	O	O	C	340/27	340/27	160C/24	80C/24	F
12	O	C	O	C	O	340/27	340/27	300C/27	300C/27	F
13	O	C	O	C	C	160C/25	81C/25	160C/25	300C/27	G
14	O	C	C	O	O	300C/27	300C/27	160C/25	160C/25	G
15	0	C	C	0	C	129/24	129/24	129/24	129/24	G

[1]Table entries: Drive Key/Drive Type Code.

C = Closed (ON), O = Open (OFF)

B.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC21/V1 can be user selected. The functions of the switches that select those options are defined in Tables B-5, B-6, B-7 and B-8 below.

TABLE B-5
OPTION SWITCH SW1 SETTINGS

Option Sw	Open	Closed	Function
SW1-1			Interrupt vector address select[2]
SW1-2			Interrupt vector address select[2]
SW1-3	0-3	4-7	Select logical units (Rev. C and above)
SW1-4	Disable	Enable	Hardware 2-1 sector interleave (Rev. D and above)
SW1-5			Not used[1]
SW1-6	Disable	Enable	Dual port mode
SW1-7			Not used[1]
SW1-8	B Cable	A Cable	Sector and Index signals
SW1-9	Disable	Enable	CDS Trident drive compatability
SW1-10			Not used[1]

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.4.2.

TABLE B-6
OPTION SWITCH SW2 SETTINGS

Option Sw	Open	Closed	Function
SW2-1			Drive configuration[2]
SW2-2			Drive configuration[2]
SW2-3			Drive configuration[2]
SW2-4			Drive configuration[2]
SW2-5			Drive configuration[2]
SW2-6			Register address selection[3]
SW2-7			Register address selection[3]
SW2-8			Register address selection[3]
SW2-9			Register address selection[3]
SW2-10			Not used[1]

[1]All unused switches MUST BE OFF.

[2]See TABLES B-2 and B-4.

[3]See TABLE B-7.

TABLE B-7
ADDRESS SWITCH SETTINGS

SWITCH SW2 -9	-8	-7	-6	PROM #192 (Standard)	PROM #597 (Optional)	PROM #793 (Optional)	
O	O	C	O	776700[2]	776700[3]	776700[3]	Standard
C	O	O	O	776300[2]	776300[3]	776300[3]	Alternate
O	O	O	C	Not used[1]	776100[3]	776600[3]	Alternate
O	C	O	O	Not used[1]	775300[3]	Not used[1]	Alternate

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.4.1.

[3]This address available with option kit. See paragraph 3.4.1.1.

TABLE B-8
OPTION SWITCH SW3 SETTINGS

Option Sw	Open	Closed	Function
SW3-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW3-2			Not used[1]
SW3-3			Not used[1]
SW3-4			Not used[1]

[1]All unused switches MUST BE OFF.

B.4 ADDRESS CONVERSION FOR VAX-11

To derive the VAX-11 address take the SC21 base address (in hex) and add the Unibus Adaptor (UBA) offset (also in hex). The conversion of the SC21 addresses from octal to hex is as follows:

Octal	Hex
776700	3FDC0
776300	3FCC0
776100	3FC40
775300	3FAC0

The following is a list of the UBA offsets for the VAX-11/780, 750 and 730.

UBA Number	730/750 Offset	780 Offset
0	FC0000	2013E000
1	F80000	2017E000
2		201BE000
3		201FE000

Thus, to derive the CSR register address for the first controller on UBA0 on the 780, take the SC21 base address of 3FDC0 (776700 in octal) and add the offset of 2013E000. The CSR register address is 2017DDC0.

APPENDIX C

SC21/BE CONFIGURATION AND OPTION SELECTION

C.1 INTRODUCTION

To allow the user of the SC21/BE the greatest amount of flexibility in selecting disk drives for his system, the SC21/BE supports a wide variety of disk types and offers a number of other user selectable options. This appendix is designed as a quick reference to the various switches and jumpers which make this flexibility possible. For more detailed information about user selectable options see the Installation chapter in this manual.

C.2 CONTROLLER CONFIGURATION

The SC21/BE unit is capable of controlling a wide variety of disk drives of various sizes and types. The various drives that are supported are defined by the Configuration PROM. Table C-1 is a list of the drive types and sizes that are supported. The user may choose between the available options by means of configuration switch SW2. The correct switch settings for each of the various configurations are given in Table C-2.

C.2.1 Physical vs Logical Disk Numbering

There is no mapping of logical disks onto physical disks of different numbers. That is, logical unit zero corresponds to physical unit zero, and so on. In cases where the capacity of the physical unit is greater than the standard capacity of the disk subsystem that is being emulated the operating system drivers must be patched to reflect the increased block counts. See the Emulex Patch Document (P/N PD9951002) for patch instructions.

C.2.2 Drive Configuration Selection

The SC21/BE emulates three different DEC disk subsystems, the RM02, the RM03 and the RM05. Both the RM02 and the RM03 subsystems have an unformatted capacity of 80 Mb. The RM05 has an unformatted capacity of 300 Mb.

Each subsystem type is represented by a drive type code in Table C-2. The number 25 represents an RM02, 24 represents an RM03, and 27 an RM05. These numbers are preceded in Table C-2 by a configuration key that represents the make and size of the physical drive that is used to emulate the DEC subsystem. The configuration key is taken from Table C-1. For example, an 80 Mb CDC 9762 is often used as a standard RM02 and would be represented in Table C-2 like this: 80C/25. An 300 Mb CDC 9766 with a RM05 assigned to it would be represented like this: 300C/27.

If the drive type code for an RM02 is paired with a drive that has a greater capacity than does a normal RM02 (80 Mb), the emulation is said to be expanded. That is, an expanded RM02 emulation would have an unformatted capacity of 300 Mb if assigned to a 300 Mb CDC 9300. Such a configuration would be represented in Table C-2 as 300A/25. Because this is a non-standard size for that particular drive type code, the host's operating system must be patched with the larger maximum block count for the expanded RM02. Instructions for patching the software are included in Appendix G.

There are several standard configurations offered that require no software patching to operate. These configurations emulate RM02, RM03 or RM05 disk subsystems, either by themselves or in combination. The standard RM02, RM03 or RM03 configurations are marked in Table C-2.

To find the configuration switch setting that is suitable for your disk installation, use the following process. Note that all configurations require that the drives be set with 32 hard sectors. See the drive manufacturer's installation manual for instructions. Note also that use of a Trident type drive requires that SW1-9 be closed.

1. Locate your drive type and size in Table C-1. Note down the configuration key assigned to your drive. If you intend to use more than one type of drive, note down their assigned keys as well.

2. Find the configuration number for the type of drive you wish to use as logical unit zero in the Drive 0 column of Table C-2. If you wish to avoid patching the software, then only use the configurations marked with a super scripted one (00^1, for example). The marked settings are standard emulations.

3. When you find a suitable match for Drive 0, check the drive key and type for Drives 1, 2 and 3 for that configuration row. You do not need to use all four drive ports.

4. When you find a suitable configuration, set the Configuration Switches (SW2) as indicated in Table C-2.

TABLE C-1
DRIVES SUPPORTED

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
80C	823	5	32	9762, 9730-80, 980, T82RM
160C	823	10	32	9730-160
160CM	1646	5	32	9730-160 - mapped
160A	1645	5	32	9160
300C	823	19	32	9766, 9300, T302RM

TABLE C-1, cont.

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
500T	1348	19	32	T602
600C	842	40	32	9775
600CM	1684	19	32	9775-mapped
84FJ	589	7	32	M2312
40C	411	5	32	9760
150C	411	19	32	9764
300A	815	19	32	9300
160T	700	12	32	SAPPHIRE 160
330A	1024	16	32	330

TABLE C-2
DRIVE CONFIGURATION PROM NO. 012

	SW2-					Logical-Physical[2]				
Octal	5	4	3	2	1	Drive 0	Drive 1	Drive 2	Drive 3	Rev.
00[1]	O	O	O	O	O	80C/25	80C/25	80C/25	80C/25	A
01	O	O	O	O	C	160C/25	160C/25	160C/25	160C/25	A
02	O	O	O	C	O	160A/25	160A/25	160A/25	160A/25	A
03	O	O	O	C	C	500T/25	500T/25	500T/25	500T/25	A
04	O	O	C	O	O	300C/25	300C/25	300C/25	300C/25	A
05[1]	O	O	C	O	C	300C/27	300C/27	300C/27	300C/27	A
06	O	O	C	C	O	600C/25	600C/25	600C/25	600C/25	A
07	O	O	C	C	C	300A/25	300A/25	300A/25	300A/25	C
10	O	C	O	O	O	80C/25	80C/25	160CM/24	160CM/24	B
11[1]	O	C	O	O	C	80C/25	80C/25	300C/27	300C/27	B
12	O	C	O	C	O	80C/25	80C/25	600CM/27	600CM/27	B
13[3]	O	C	O	C	C	300C/25	300C/25	600CM/24	600CM/24	B
14	O	C	C	O	O	300C/27	300C/27	600C/25	600C/25	B
15[3]	O	C	C	O	C	80C/25	80C/25	300C/27	600C/24	E
16[1]	O	C	C	C	O	300C/27	80C/25	80C/25	80C/25	G
17[1]	O	C	C	C	C	300C/27	300C/27	80C/25	80C/25	G
20	C	O	O	O	O	80C/25	160CM/24	160CM/24	160CM/24	B
21[1]	C	O	O	O	C	80C/25	300C/27	300C/27	300C/27	B
22	C	O	O	C	O	80C/25	600CM/27	600CM/27	600CM/27	B
23	C	O	O	C	C	300C/25	600CM/24	600CM/24	600CM/24	B
24	C	O	C	O	O	300C/27	600C/25	600C/25	600C/25	B
25[3]	C	O	C	O	C	300A/25	600C/24	600C/24	600C/24	F
26	C	O	C	C	O	300A/27	330A/25	300A/27	330A/25	G
27	C	O	C	C	C	160CM/25	160CM/25	300C/27	300C/27	G
30[1]	C	C	O	O	O	80C/25	80C/25	80C/25	300C/27	G
31	C	C	O	O	C	84FJ/25	84FJ/25	84FJ/25	84FJ/25	C
32	C	C	O	C	O	40C/25	40C/25	40C/25	40C/25	C
33	C	C	O	C	C	150C/25	150C/25	150C/25	150C/25	C

TABLE C-2, cont.

Octal	SW2- 5	4	3	2	1	Logical-Physical[2] Drive 0	Drive 1	Drive 2	Drive 3	Rev.
34[3]	C	C	C	O	O	84FJ/24	84FJ/24	84FJ/24	80C/25	H
35[3]	C	C	C	O	C	84FJ/24	84FJ/24	84FJ/24	80C/25	J
36	C	C	C	C	O	330A/25	330A/25	330A/25	330A/25	F
37	C	C	C	C	C	160T/25	160T/25	160T/25	160T/25	F

[1]Standard configurations; no software patching required.

[2]Table entries: Drive Key/Drive Type Code.

[3]Configurations cannot be used with RSTS/E operating system.

C = sw. closed; O = sw. open.

TABLE C-3
DRIVES SUPPORTED BY ALTERNATE CONFIGURATION PROM (#898)

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
80C	823	05	32	Ampex 9380, Century T82RM, CDC 9730-80, CDC9762
160C	823	10	32	CDC 9730-160, Fujitsu 2284
330A	1024	16	32	Ampex 330, Fujitsu 2294

TABLE C-4
DRIVE CONFIGURATIONS FOR
ALTERNATE CONFIGURATION PROM (#898)

Octal	SW2- 5	4	3	2	1	Logical-Physical[1] Drive 0	Drive 1	Drive 2	Drive 3	Rev.
00	O	O	O	O	O	160C/24	160C/24	160C/24	330A/25	A
01	O	O	O	O	C	160C/25	160C/25	330A/27	330A/27	B
02	O	O	O	C	O	80C/25	80C/25	160C/25	160C/25	C

[1]Table entries: Drive Key/Drive Type Code.

C = Closed (ON), O = Open (OFF)

C.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC21/BE can be user selected. The functions of the switches that select those options are defined in Tables C-5, C-6, C-7 and C-8 below.

TABLE C-5
OPTION SWITCH SW1 SETTINGS

Option Sw	Open	Closed	Function
SW1-1			Interrupt vector address select[2]
SW1-2			Interrupt vector address select[2]
SW1-3	0-3	4-7	Select logical units (Rev. C and above)
SW1-4			Not used[1]
SW1-5			Not used[1]
SW1-6	Disable	Enable	Dual port mode
SW1-7	Disable	Enable	DMA Bandwidth Control
SW1-8	B Cable	A Cable	Sector and Index signals
SW1-9	Disable	Enable	CDS Trident drive compatability
SW1-10			Not used[1]

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.4.2.

TABLE C-6
OPTION SWITCH SW2 SETTINGS

Option Sw	Open	Closed	Function
SW2-1			Drive configuration[2]
SW2-2			Drive configuration[2]
SW2-3			Drive configuration[2]
SW2-4			Drive configuration[2]
SW2-5			Drive configuration[2]
SW2-6			Register address selection[3]
SW2-7			Register address selection[3]
SW2-8			Register address selection[3]
SW2-9			Register address selection[3]
SW2-10			Not used[1]

[1]All unused switches MUST BE OFF.

[2]See TABLES C-2 and C-4.

[3]See TABLE C-7.

TABLE C-7
ADDRESS SWITCH SETTINGS

SWITCH SW2 -9	-8	-7	-6	PROM #192 (Standard)	PROM #597 (Optional)	PROM #793 (Optional)	
O	O	C	O	776700[2]	776700[3]	776700[3]	Standard
C	O	O	O	776300[2]	776300[3]	776300[3]	Alternate
O	O	O	C	Not used[1]	776100[3]	776600[3]	Alternate
O	C	O	O	Not used[1]	775300[3]	Not used[1]	Alternate

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.4.1.

[3]This address available with option kit. See paragraph 3.4.1.1.

TABLE C-8
OPTION SWITCH SW3 SETTINGS

Option Sw	Open	Closed	Function
SW3-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW3-2			Not used[1]
SW3-3			Not used[1]
SW3-4	Disable	Enable	Software sector interleaving

[1]All unused switches MUST BE OFF.

APPENDIX D

SC21/BF CONFIGURATION AND OPTION SELECTION

D.1 INTRODUCTION

The SC21/BF supports the two fixed-head options of the CDC 9730 disk drives. One option provides .96 Mb of fixed-head storage, and the other provides 1.92 Mb. The fixed-head options are offered on both the 80 Mb and 160 Mb 9730s. Using these drives in combination with several non-fixed-head drives, the SC21/BF is able to offer the user a variety of logical disk drives and types. This appendix is designed as a quick reference to the various switches and jumpers which make this flexibility possible. For more detailed information about user selectable options see the Installation chapter in this manual.

D.2 CONTROLLER CONFIGURATION

The SC21/BF unit is capable of controlling several disk drives of various sizes and types. The various drives that are supported are defined by the Configuration PROM. Table D-1 is a list of the drive types and sizes that are supported. The user may choose between the available options by means of configuration switch SW2. The correct switch settings for each of the various configurations are given in Table D-2.

D.2.1 Physical vs Logical Disk Numbering

Each 9730 with the fixed-head option acts like two completely different disk drives--an 80 Mb or 160 Mb moving head unit and a .96 Mb or 1.92 Mb fixed-head unit. The SC21/BF maps a standard RM02 onto the moving heads (an expanded RM02 on the 160 Mb version) and it maps a contracted .96 or 1.92 Mb RM03 onto the fixed-heads. This arrangement allows eight logical disk drives to be mapped on four physical disk drives. The table below shows the logical number assignments per physical disk drive.

Physical Drives	Logical Drives (Moving)	(Fixed)
0	0	4
1	1	5
2	2	6
3	3	7

The configurations listed in Table D-2 offer several variations on this theme.

D.2.2 Drive Configuration Selection

The SC21/BF emulates two different DEC disk subsystems, the RM02 and the RM03. Both the RM02 and the RM03 subsystems have an unformatted capacity of 80 Mb.

The various subsystem types are represented by a drive type code in the Logical Drive columns of Table D-2. The number 25 represents an RM02 and 24 represents an RM03. These numbers are preceded in Table D-2 by a configuration key that represents the make and size of the physical drive that is used to emulate the DEC subsystem. The configuration key is taken from Table D-1.

If the drive type code for an RM02 is paired with one of the 160 Mb drives, the emulation is said to be expanded. That is, an expanded RM02 emulation has an unformatted capacity of 160 Mb when assigned to a 160 Mb CDC 9730. Such a configuration is represented in Table D-2 as 160x/25. Because this is a non-standard size for that particular drive type code, the host's operating system must be patched with the larger maximum block count for the expanded RM02. Instructions for patching the software are included in the Emulex Patch Document (P/N PD9951002).

All of the RM03 emulations are mapped onto the fixed head portions for the disk drives. Because the fixed head portion of the drive has a capacity of only .96 Mb or 1.92 Mb (depending on the drive), the RM03 emulation must be contracted. Because this is a non-standard size for that particular drive type code, the host's operating system must be patched with the smaller maximum block count for the contracted RM03. Instructions for patching the software are included in the Emulex Patch Document (P/N PD9951002).

To find the configuration switch setting that is suitable for your disk installation, use the following process. Note that all configurations require that the drives be set with 32 hard sectors. See the drive manufacturer's installation manual for instructions. Note that use of Fujitsu M2286-M2288 drives requires that SW1-3 be closed.

1. Locate your drive type and size in Table D-1. Note down the configuration key assigned to your drive. If you intend to use more than one type of drive, note down their assigned keys as well.

2. Scan down the Physical Unit and Type columns of Table D-2 until you find the configuration key for the type of drive you wish to use as logical unit zero in a row marked unit zero.

3. When you find a suitable match for Drive 0, check the drive key and type for Drives 1, 2 and 3 for that configuration row. Also look at the arrangement of the logical units for that configuration. You do not need to use all four drive ports. If that configuration does not

suit your needs, continue to scan down the list until you find another match for drive zero, etc.

4. When you find a suitable configuration, set the Configuration Switches (SW2) as indicated in Table D-2.

TABLE D-1
DRIVES SUPPORTED

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
80C	823	5	32	9762, 9730-80, 980, T82RM
80F	19	5	32	9730-80F - 1.92 mb. fixed-head opt.
80E	9	5	32	9730-80F - 0.96 mb. fixed-head opt.
160C	823	10	32	9730-160, M2284
160F	9	10	32	9730-160F - 1.92 mb. fixed-head opt.
160E	4	10	32	9730-160F - 0.96 mb. fixed-head opt.

TABLE D-2
DRIVE CONFIGURATION PROM NO. 1145

	SW2-					Physical		Logical		
Octal	5	4	3	2	1	Unit	Key	Unit	Type (Code)	Rev.
00	O	O	O	O	O	0	80E	0/4	RM02 (25)/RM03 (24)	
						1	80E	1/5	RM02 (25)/RM03 (24)	
						2	80E	2/6	RM02 (25)/RM03 (24)	
						3	80E	3/7	RM02 (25)/RM03 (24)	
01*	O	O	O	O	C	0	80E	0/4	RM02 (25)/RM03 (24)	
						1	80E	1/5	RM02 (25)/RM03 (24)	
						2	80E	2/6	RM02 (25)/RM03 (24)	
						3	80E	3/7	RM02 (25)/RM03 (24)	
02	O	O	O	C	O	0	80F	0/4	RM02 (25)/RM03 (24)	
						1	80F	1/5	RM02 (25)/RM03 (24)	
						2	80F	2/6	RM02 (25)/RM03 (24)	
						3	80F	3/7	RM02 (25)/RM03 (24)	
03	O	O	O	C	C	0	80C	0	RM02 (25)	
						1	80C	1	RM02 (25)	
						2	80E	2/6	RM02 (25)/RM03 (24)	
						3	80E	3/7	RM02 (25)/RM03 (24)	
04*	O	O	C	O	O	0	80C	0	RM02 (25)	
						1	80C	1	RM02 (25)	
						2	80E	2/6	RM02 (25)/RM03 (24)	
						3	80E	3/7	RM02 (25)/RM03 (24)	
05	O	O	C	O	C	0	80C	0	RM02 (25)	
						1	80C	1	RM02 (25)	
						2	80F	2/6	RM02 (25)/RM03 (24)	
						3	80F	3/7	RM02 (25)/RM03 (24)	

TABLE D-2, cont.

Octal	SW2- 5	4	3	2	1	Physical Unit	Key	Logical Unit	Type (Code)	Rev.
06	O	O	C	C	O	0	160E	0/4	RM02 (25)/RM03 (24)	
						1	160E	1/5	RM02 (25)/RM03 (24)	
						2	160E	2/6	RM02 (25)/RM03 (24)	
						3	160E	3/7	RM02 (25)/RM03 (24)	
07*	O	O	C	C	C	0	160E	0/4	RM02 (25)/RM03 (24)	
						1	160E	1/5	RM02 (25)/RM03 (24)	
						2	160E	2/6	RM02 (25)/RM03 (24)	
						3	160E	3/7	RM02 (25)/RM03 (24)	
10	O	C	O	O	O	0	160F	0/4	RM02 (25)/RM03 (24)	
						1	160F	1/5	RM02 (25)/RM03 (24)	
						2	160F	2/6	RM02 (25)/RM03 (24)	
						3	160F	3/7	RM02 (25)/RM03 (24)	
11*	O	C	O	O	C	0	160F	0/4	RM02 (25)/RM03 (24)	
						1	160F	1/5	RM02 (25)/RM03 (24)	
						2	160F	2/6	RM02 (25)/RM03 (24)	
						3	160F	3/7	RM02 (25)/RM03 (24)	
12	O	C	O	C	O	0	160C	0	RM02 (25)	
						1	160C	1	RM02 (25)	
						2	160E	2/6	RM02 (25)/RM03 (24)	
						3	160E	3/7	RM02 (25)/RM03 (24)	
13*	O	C	O	C	C	0	160C	0	RM02 (25)	
						1	160C	1	RM02 (25)	
						2	160E	2/6	RM02 (25)/RM03 (24)	
						3	160E	3/7	RM02 (25)/RM03 (24)	
14	O	C	C	O	O	0	160C	0	RM02 (25)	
						1	160C	1	RM02 (25)	
						2	160F	2/6	RM02 (25)/RM03 (24)	
						3	160F	3/7	RM02 (25)/RM03 (24)	
15*	O	C	C	O	C	0	160C	0	RM02 (25)	
						1	160C	1	RM02 (25)	
						2	160F	2/6	RM02 (25)/RM03 (24)	
						3	160F	3/7	RM02 (25)/RM03 (24)	

[1]C = sw. closed; O = sw. open
*See below.

Configurations marked with an asterisk allow users with the ability to modify their software access to the maximum number of fixed-head tracks. The software must be modified because the last track does not have a full complement of heads in these configurations. The following table gives the number of tracks, heads and sectors for the fixed-head portion of the drive.

Octal	Tracks	Heads	Sectors	Heads, Last Track	Fixed Drive Size (Mb)
01	10	05	32	3	0.96
04	10	05	32	3	0.96
07	05	10	32	8	0.96
11	10	10	32	6	1.92
13	05	10	32	8	0.96
17	10	10	32	6	1.92

Because the last track of each of these configurations does not contain a full complement of heads, standard DEC software cannot be adapted to use them. Also, neither DEC or Emulex diagnostics will work on these configurations.

All of the other configurations will work with standard DEC drivers after the drivers have been patched with the appropriate block counts as described in the Emulex Patch Document (P/N PD9951002).

D.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC21/BF can be user selected. The functions of the switches that select those options are defined in Tables D-3, D-4, D-5 and D-6 below.

TABLE D-3
OPTION SWITCH SW1 SETTINGS

Option Sw	Open	Closed	Function
SW1-1			Interrupt vector address select[2]
SW1-2			Interrupt vector address select[2]
SW1-3	Disable	Enable	Fujitsu M2286-M2288 (Rev. C and above)
SW1-4	Disable	Enable	Drive type 27 for logical units 4-7 (Rev. C and above)
SW1-5			Not used[1]
SW1-6	Disable	Enable	Dual port mode
SW1-7	Disable	Enable	DMA Bandwidth Control
SW1-8	B Cable	A Cable	Sector and Index signals
SW1-9	Disable	Enable	CDS Trident drive compatability
SW1-10			Not used[1]

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.4.2.

TABLE D-4
OPTION SWITCH SW2 SETTINGS

Option Sw	Open	Closed	Function
SW2-1			Drive configuration[2]
SW2-2			Drive configuration[2]
SW2-3			Drive configuration[2]
SW2-4			Drive configuration[2]
SW2-5			Drive configuration[2]
SW2-6			Register address selection[3]
SW2-7			Register address selection[3]
SW2-8			Register address selection[3]
SW2-9			Register address selection[3]
SW2-10			Not used[1]

[1]All unused switches MUST BE OFF.

[2]See TABLE D-1.

[3]See TABLE D-5.

TABLE D-5
ADDRESS SWITCH SETTINGS

SWITCH SW2 -9	-8	-7	-6	PROM #192 (Standard)	PROM #597 (Optional)	PROM #793 (Optional)	
O	O	C	O	776700[2]	776700[3]	776700[3]	Standard
C	O	O	O	776300[2]	776300[3]	776300[3]	Alternate
O	O	O	C	Not used[1]	776100[3]	776600[3]	Alternate
O	C	O	O	Not used[1]	775300[3]	Not used[1]	Alternate

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.4.1.

[3]This address available with option kit. See paragraph 3.4.1.1.

TABLE D-6
OPTION SWITCH SW3 SETTINGS

Option Sw	Open	Closed	Function
SW3-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW3-2			Not used[1]
SW3-3	5.1 usec.	20.4 usec.	Delay time for suspended DMA burst (Rev C and above)
SW3-4			Not used[1]

[1]All unused switches MUST BE OFF.

APPENDIX E

SC21/BM CONFIGURATION SWITCHES

E.1 INTRODUCTION

The SC21/BM emulates three different DEC disk subsystems, the RM02, the RM03 and the RM05. Both the RM02 and the RM03 subsystems have an unformatted capacity of 80 Mb. The RM05 has an unformatted capacity of 300 Mb. To allow the user to take advantage of large capacity disk drives and their lower cost per bit, the SC21/BM maps up to eight logical disk drives onto four physical drives. For example, eight RM02 emulations would be mapped onto four 160 Mb CDC 9730 disk drives. This appendix is designed as a quick reference to the various switches and jumpers which make this flexibility possible. For more detailed information about user selectable options see the Installation chapter in this manual.

E.2 CONTROLLER CONFIGURATION

The SC21/BM unit is capable of controlling several disk drives of various sizes and types. The various drives that are supported are defined by the Configuration PROM. Table E-1 is a list of the drive types and sizes that are supported. The user may choose between the available options by means of configuration switch SW2. The correct switch settings for each of the various configurations are given in Table E-2.

E.2.1 Physical vs Logical Disk Numbering

The SC21/BM allows eight logical RM02, RM03 or RM05 disk drives to be mapped on four physical disk drives. The table below shows the logical number assignments per physical disk drive.

Physical Drives	Logical Drives (Moving)	(Fixed)
0	0	4
1	1	5
2	2	6
3	3	7

The configurations listed in Table E-2 offer several variations on this theme.

E.2.2 Drive Configuration Selection

The various subsystem types emulated by the SC21/BM (the RM02, RM03 and RM05) are represented by a drive type code in the Logical Drive columns of Table E-2. The number 25 represents an RM02, 24

represents an RM03 and 27 an RM05. These numbers are preceded in Table E-2 by a configuration key that represents the make and size of the physical drive that is used to emulate the DEC subsystem. The configuration key is taken from Table E-1.

Except for configurations 20 and 20R, all of the configurations supported by the SC21/BM are standard emulations and require no software modifications. The RM03 emulations in configurations 20 and 20R are 164 cylinder drives mapped onto the cartridges of the CDC 9748s. See the Emulex Patch Document (P/N PD9951002) for instructions on how to patch the operating system to accommodate those two configurations.

To find the configuration switch setting that is suitable for your disk installation, use the following process. Note that all configurations require that the drives be set with 32 hard sectors. See the drive manufacturer's installation manual for instructions. Note also that for Lark drive compatibility SW1-5 must be set according to the SC21/BM firmware revision and that use of a CMD type drive requires that SW1-3 be closed.

1. Locate your drive type and size in Table E-1. Note down the configuration key assigned to your drive. If you intend to use more than one type of drive, note down their assigned keys as well.

2. Scan down the Physical Unit and Type columns of Table E-2 until you find the configuration key for the type of drive you wish to use as logical unit zero in a row marked unit zero.

3. When you find a suitable match for Drive 0, check the drive key and type for Drives 1, 2 and 3 for that configuration row. Also look at the arrangement of the logical units for that configuration. You do not need to use all four drive ports. If that configuration does not suit your needs, continue to scan down the list until you find another match for drive zero, etc.

4. When you find a suitable configuration, set the Configuration Switches (SW2) as indicated in Table E-2.

TABLE E-1
DRIVES SUPPORTED

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
80	823	5	32	9762, 9730-80/CDC, T82RM/Century
84	589	7	32	M2312/Fujitsu
96	823	6	32	9448-96/CDC
160	823	10	32	9730-160/CDC, M2284/Fujitsu
161	1646	5	32	9160/Ampex modified for 1646 cyl.
162	1645	5	32	9160/Ampex

TABLE E-1, cont.

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
300	823	19	32	9766/CDC
330	1024	16	32	330/Ampex
673	1124	30	32	8775/STC
675	842	40	32	9775/CDC
13	203	4	32	9455/CDC

TABLE E-2
DRIVE CONFIGURATION PROM NO. 286 REV. E

Octal	SW2- 5	4	3	2	1	Physical Unit	Key	Logical Unit	Type (Code)	Rev.
00	O	O	O	O	O	0	80	0	RM02 (25)	A
						1	80	1	RM02 (25)	
						2	80	2	RM02 (25)	
						3	80	3	RM02 (25)	
01	O	O	O	O	C	0	80	0	RM02 (25)	A
						1	80	1	RM02 (25)	
						2	160	2/6	RM02 (25)/RM02 (25)	
						3	160	3/7	RM02 (25)/RM02 (25)	
02	O	O	O	C	O	0	80	0	RM02 (25)	A
						1	160	1/5	RM02 (25)/RM02 (25)	
						2	160	2/6	RM02 (25)/RM02 (25)	
						3	160	3/7	RM02 (25)/RM02 (25)	
03	O	O	O	C	C	0	160	0/4	RM02 (25)/RM02 (25)	A
						1	160	1/5	RM02 (25)/RM02 (25)	
						2	160	2/6	RM02 (25)/RM02 (25)	
						3	160	3/7	RM02 (25)/RM02 (25)	
04	O	O	C	O	O	0	300	0	RM05 (27)	A
						1	300	1	RMO5 (27)	
						2	675	2/6	RM05 (27)/RM05 (27)	
						3	675	3/7	RM05 (27)/RM05 (27)	
05	O	O	C	O	C	0	300	0	RM05 (27)	A
						1	675	1/5	RM05 (27)/RM05 (27)	
						2	675	2/6	RM05 (27)/RM05 (27)	
						3	675	3/7	RM05 (27)/RM05 (27)	
06	O	O	C	C	O	0	675	0/4	RM05 (27)/RM05 (27)	A
						1	675	1/5	RM05 (27)/RM05 (27)	
						2	675	2/6	RM05 (27)/RM05 (27)	
						3	675	3/7	RM05 (27)/RM05 (27)	
07	O	O	C	C	C	0	80	0	RM02 (25)	A
						1	160	1/5	RM02 (25)/RM02 (25)	
						2	300	2	RM05 (27)	
						3	675	3/7	RM05 (27)/RM05 (27)	
10	O	C	O	O	O	0	160	0/4	RM02 (25)/RM02 (25)	C
						1	160	1/5	RM02 (25)/RM02 (25)	
						2	160	2/6	RM02 (25)/RM02 (25)	
						3	80	3	RM02 (25)	

TABLE E-2, cont.

Octal	SW2-5	SW2-4	SW2-3	SW2-2	SW2-1	Physical Unit	Physical Key	Logical Unit	Logical Type (Code)	Rev.
11	O	C	O	O	C	0	675	0/4	RM05 (27)/RM05 (27)	C
						1	675	1/5	RM05 (27)/RM05 (27)	
						2	675	2/6	RM05 (27)/RM05 (27)	
						3	300	3	RM05 (27)	
12	O	C	O	C	O	0	300	0	RM05 (27)	C
						1	300	1	RM05 (27)	
						2	300	2	RM05 (27)	
						3	300	3	RM05 (27)	
13	O	C	O	C	C	0	80	0	RM02 (25)	C
						1	80	1	RM02 (25)	
						2	80	2	RM02 (25)	
						3	300	3	RM05 (27)	
14	O	C	C	O	O	0	80	0	RM02 (25)	C
						1	80	1	RM02 (25)	
						2	300	2	RM05 (27)	
						3	300	3	RM05 (27)	
15	O	C	C	O	C	0	300	0	RM05 (27)	C
						1	300	1	RM05 (27)	
						2	300	2	RM05 (27)	
						3	80	3	RM02 (25)	
16	O	C	C	C	O	0	330	0	RM05 (27)	C
						1	330	1	RM05 (27)	
						2	330	2	RM05 (27)	
						3	330	3	RM05 (27)	
17	O	C	C	C	C	0	330	0	RM05 (27)	C
						1	330	1	RM05 (27)	
						2	330	2	RM05 (27)	
						3	300	3	RM05 (27)	
20	C	O	O	O	O	0	96	0/4	RM03 (24)[2]/RM02 (25)	C
						1	96	1/5	RM03 (24)[2]/RM02 (25)	
						2	96	2/6	RM03 (24)[2]/RM02 (25)	
						3	300	3	RM05 (27)	
20R[1]	C	O	O	O	O	0	96	0/4	RM02 (25)/RM03 (24)[2]	C
						1	96	1/5	RM02 (25)/RM03 (25)[2]	
						2	96	2/6	RM02 (25)/RM03 (24)[2]	
						3	300	3	RM05 (27)	
21	C	O	O	O	C	0	13	0/4	RM03 (24)[3]/RM03 (24)[3]	B
						1	13	1/5	RM03 (24)[3]/RM03 (24)[3]	
						2	80	2	RM02 (25)	
						3	80	3	RM02 (25)	
21R[1]	C	O	O	O	C	0	13	0/4	RM03 (24)[3]/RM03 (24)[3]	B
						1	13	1/5	RM03 (24)[3]/RM03 (24)[3]	
						2	80	6	RM02 (25)	
						3	80	7	RM02 (25)	
22	C	O	O	C	O	0	300	0	RM05 (27)	C
						1	96	1/5	RM03 (24)[2]/RM02 (25)	
						2	96	2/6	RM03 (24)[2]/RM02 (25)	
						3	300	3	RM05 (27)	

TABLE E-2, cont.

Octal	SW2- 5	4	3	2	1	Physical Unit	Key	Logical Unit	Type (Code)	Rev.
22R[1]	C	O	O	C	O	0	300	0	RM05 (27)	C
						1	96	1/5	RM02 (25)/RM03 (24)[2]	
						2	96	2/6	RM02 (25)/RM03 (24)[2]	
						3	300	3	RM05 (27)	
23	C	O	O	C	C	0	300	0	RM05 (27)	C
						1	160	1/5	RM02 (25)/RM02 (25)	
						2	160	2/6	RM02 (25)/RM02 (25)	
						3	160	3/7	RM02 (25)/RM02 (25)	
24	C	O	C	O	O	0	84	0	RM02 (25)	A
						1	84	1	RM02 (25)	
						2	84	2	RM02 (25)	
						3	84	3	RM02 (25)	
25	C	O	C	O	C	0	160	0/4	RM02 (25)/RM02 (25)	D[4]
						1	160	1/5	RM02 (25)/RM02 (25)	
						2	161	2/6	RM02 (25)/RM02 (25)	
						3	160	3/7	RM02 (25)/RM02 (25)	
26	C	O	C	C	O	0	84	0	RM02 (25)	D
						1	84	1	RM02 (25)	
						2	84	2	RM02 (25)	
						3	80	3	RM02 (25)	
27	C	O	C	C	C	0	162	0	RM02 (25)[6]	E
						1	162	1	RM02 (25)[6]	
						2	330	2/6	RM02 (25)[6]	
						3	330	3/7	RM02 (25)[6]	
30	C	C	O	O	O	0	673	0	RM05 (27)[7]	E
						1	673	1	RM05 (27)[7]	
						2	673	2	RM05 (27)[7]	
						3	673	3	RM05 (27)[7]	
31	C	C	O	O	C	0	673	0/4	RM05 (27)/RM05 (27)	A
						1	673	1/5	RM05 (27)/RM05 (27)	
						2	673	2/6	RM05 (27)/RM05 (27)	
						3	673	3/7	RM05 (27)/RM05 (27)	
32	C	C	O	C	O	0	673	0/4	RM05 (27)/RM05 (27)	C
						1	673	1/5	RM05 (27)/RM05 (27)	
						2	673	2/6	RM05 (27)/RM05 (27)	
						3	300	3	RM05 (27)	
33	C	C	O	C	C	0	300	0	RM02 (25)[5]	D
						1	300	1	RM02 (25)[5]	
						2	300	2	RM02 (25)[5]	
						3	300	3	RM02 (25)[5]	
34	C	C	C	O	O	0	84	0	RM02 (25)	F
						1	84	1	RM02 (25)	
						2	80	2	RM02 (25)	
						3	80	3	RM02 (25)	
35	C	C	C	O	C	0	330	0	RM05 (27)	G
						1	330	1	RM05 (27)	
						2	300	2	RM05 (27)	
						3	300	3	RM05 (27)	

TABLE E-2, cont.

Octal	SW2-5	4	3	2	1	Physical Unit	Key	Logical Unit	Type (Code)	Rev.
36	C	C	C	C	O	0	80	0	RM02 (25)	G
						1	300	1	RM05 (27)	
						2	300	2	RM05 (27)	
						3	300	3	RM05 (27)	
37	C	C	C	C	C	0	80	0	RM02 (25)	G
						1	330	1	RM05 (27)	
						2	84	2	RM02 (25)	
						3	84	3	RM02 (25)	

[1]Configuration Reverse is obtained by closing SW1-4.

[2]This RM03 emulation is a 164 cylinder drive mapped onto the 9448 cartridge. SW1-3 must be closed to enable this emulation. The host operating system must be patched to accommodate this configuration. See the Emulex Patch Document (P/N PD9951002).

[3]This RM03 emulation is a 81 cylinder drive mapped onto the 9455 cartridge. Note the instructions in Table E-5 for setting SW1-5 when using this configuration. The host operating system must be patched to accommodate this configuration. See the Emulex Patch Document (P/N PD9951002).

[4]SC21/BM firmware must be revision E or above for this config.

[5]This RM02 has 19 heads and 823 cylinders.

[6]This RM02 has 5 heads and 1638 cylinders.

[7]This RM05 has 30 heads and 1124 cylinders.

C = sw. closed; O = sw. open

TABLE E-3
DRIVES SUPPORTED BY ALTERNATE CONFIGURATION PROM (#987)

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
13	203	4	32	9455/CDC
80	823	5	32	9762, 9710, 9730-80/CDC, T82RM/Century
84	589	7	32	M2312/Fujitsu
96	823	6	32	9448-96/CDC
160	823	10	32	9715, 9730-160/CDC, M2284/Fujitsu

continued on next page

TABLE E-3, continued

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
161	1646	5	32	9160/Ampex modified for 1646 cylinders.
162	1645	5	32	9160/Ampex
300	823	19	32	9766/CDC
330	1024	16	32	330/Ampex, 2294/Fujitsu
340	711	24	32	9715-340/CDC
673	1124	30	32	8775/STC
675	842	40	32	9775/CDC

TABLE E-4
DRIVE CONFIGURATIONS FOR
ALTERNATE CONFIGURATION PROM (#987)

	SW2-					SW1	Physical			
Logical Octal	5	4	3	2	1	3	Unit	Key	Unit	Type (Code)	Rev
00	O	O	O	O	O	O	0	330	0	RM05 (27)	A
							1	80	1	RM03 (24)	A
							2	330	2	RM05 (27)	A
							3	330	3	RM05 (27)	A
01	O	O	O	C	O	O	0	160	0/4	RM02 (25)/RM02 (25)	B
							1	160	1/5	RM02 (25)/RM02 (25)	B
							2	330	2	RM05 (27)	B
							3	330	3	RM05 (27)	B
02	O	O	C	O	O	O	0	160	0/4	RM02 (25)/RM02 (25)	B
							1	80	1	RM02 (25)	B
							2	330	2	RM05 (27)	B
							3	330	3	RM05 (27)	B
03	O	O	O	C	C	O	0	300	0	RM05 (27)	C
							1	300	1	RM05 (27)	C
							2	160	2/6	RM02 (25)/RM02 (25)	C
							3	160	3/7	RM02 (25)/RM02 (25)	C
04	O	O	C	O	O	O	0	330	0	RM05 (27)	D
							1	330	1	RM05 (27)	D
							2	330	2	RM05 (27)	D
							3	80	3	RM02 (25)	D
05	O	O	C	O	C	O	0	340	0	RM05 (27)	E
							1	340	1	RM05 (27)	E
							2	340	2	RM05 (27)	E
							3	340	3	RM05 (27)	E
06	O	O	C	C	O	O	0	340	0	RM05 (27)	E
							1	340	1	RM05 (27)	E
							2	340	2	RM05 (27)	E
							3	300	3	RM05 (27)	E

C = Closed (ON), O = Open (OFF)

TABLE E-4, continued

Logical Octal	SW2-5	4	3	2	1	SW1-3	Physical Unit	Key	Unit	Type (Code)	Rev
07	O	O	C	C	C	O	0	80	0	RM03 (27)	F
							1	330	1	RM05 (27)	F
							2	330	2	RM05 (27)	F
							3	330	3	RM05 (27)	F
10	O	C	O	O	O	O	0	300	0	RM05 (27)	F
							1	300	1	RM05 (27)	F
							2	300	2	RM05 (27)	F
							3	675	3,7	RM05 (27)/RM05 (27)	F
11	O	C	O	O	C	O	0	675	0,4	RM05 (27)/RM05 (27)	F
							1	300	1	RM05 (27)	F
							2	300	2	RM05 (27)	F
							3	300	3	RM05 (27)	F
12	O	C	O	C	O	O	0	330	0	RM05 (27)	H
							1	330	1	RM05 (27)	H
							2	80	2	RM03 (24)	H
							3	80	3	RM03 (24)	H
13	O	C	O	C	C	O	0	330	0	RM05 (27)	J
							1	330	1	RM05 (27)	J
							2	80	2	RM02 (25)	J
							3	80	3	RM02 (25)	J

E.3 USER SELECTABLE OPTIONS

Other options including the register starting address for the SC21/BM can be user selected. The functions of the switches that select those options are defined in Tables E-5, E-6, E-7 and E-8 below.

TABLE E-5
OPTION SWITCH SW1 SETTINGS

Option Sw	Open	Closed	Function
SW1-1			Interrupt vector address select[2]
SW1-2			Interrupt vector address select[2]
SW1-3	Disable	Enable	Select CMD-type disk drives
SW1-4	0-3	4-7	Select logical units
SW1-5			Not used[4]
SW1-6	Disable	Enable	Dual port mode (Rev. C and above)
SW1-7	Disable	Enable	DMA Bandwidth Control
SW1-8	B Cable	A Cable	Sector and Index signals
SW1-9	Disable	Enable	Dual access mode enable (Rev. F and above)[3]
SW1-10			Not used[1]

Notes on next page

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.4.2.1.

[3]See paragraph 2.6.7.

[4]Revisions B through G of SC21/BM firmware require this switch to be ON (closed) for Lark drive compatibility. For Lark drive compatibility with SC21/BM firmware Revisions H and above, this switch must be OFF (open), and the Seek-On-Head-Select switch on the Lark drive must be ON.

TABLE E-6
OPTION SWITCH SW2 SETTINGS

Option Sw	Open	Closed	Function
SW2-1			Drive configuration[2]
SW2-2			Drive configuration[2]
SW2-3			Drive configuration[2]
SW2-4			Drive configuration[2]
SW2-5			Drive configuration[2]
SW2-6			Register address selection[3]
SW2-7			Register address selection[3]
SW2-8			Not used[1]
SW2-9			Register address selection[3]
SW2-10			Not used[1]

[1]All unused switches MUST BE OFF.

[2]See TABLES E-2 and E-4.

[3]See TABLE E-7.

TABLE E-7
ADDRESS SWITCH SETTINGS

SWITCH 2-6	2-7	2-8	2-9	PROM #793 (Standard)	PROM #597 (Optional)	
O	O	O	C	776300[2]	776300[3]	(Alternate)
O	O	C	O	Not used[1]	775300[3]	(Alternate)
O	C	O	O	776700[2]	776700[3]	(Standard)
C	O	O	O	776600[2]	776100[3]	(Alternate)

[1]All unused switches must be OFF.

[2]See paragraph 3.4.1.2.

[3]This address available with option kit. See paragraph 3.4.1.1.

TABLE E-8
OPTION SWITCH SW3 SETTINGS

Option Sw	Open	Closed	Function
SW3-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW3-2			Not used[1]
SW3-3	5.1 us	20.4 us	Extend delay on suspended DMA (Revisions B and above)
SW3-4			Interrupt vector address select[2] (Revisions G and above)

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.4.2.1.

APPENDIX F

DRIVE MODIFICATIONS

This appendix provides modifications to commonly used drives for moving the Sector and Index signals from the A cable to the B cable.

F.1 CDC 9762

Remove (Ch. I)	Add (Ch. I)
B01-06B to JA82-18B	B01-06B to JA82-43B
B01-06A to JA82-18A	B01-06A to JA82-44A
B01-05B to JA82-25B	B01-05B to JA82-45B
B01-05A to JA82-25A	B01-05A to JA82-45A

Remove (Ch. II)	Add (Ch. II)
B03-06B to JA83-18B	B03-06B to JA83-43B
B03-06A to JA83-18A	B03-06A to JA83-44A
B03-05B to JA83-25B	B03-05B to JA83-45B
B03-05A to JA83-25A	B03-05A to JA83-45A

Rework transmitter card FTVV in location B01 (Ch. I) and B03 (Ch. II). Locate jumper at center bottom of board (as viewed with connector on the right). Remove jumper and reinsert one set of holes lower (i.e., from center hole to hole below original jumper). Remove the letter "F" from the card type designation FTVV and mark a "G" in its place so that the card type becomes GTVV.

NOTE - On later models of the 9762, CDC will ship units with an enhancement feature which will allow easy switchover to the B cable as follows: Remove the jumper plug on (B07) of the logic chassis backpanel.

F.2 CDC 9730

Rework transmitter-receiver card CFAX in location A04 (Ch. I) and B04 (Ch. II). When viewing card with connector on the right, locate four jumpers to the left of the I/O connectors and above the terminator ground lug. The bottom end of the jumpers must be removed from the holes to which they are soldered and moved to the holes immediately above. Next, find the small jumper to the right of the third IC from the connector edge of the board on the bottom row of ICs. This jumper must be removed and reinserted so that it connects the top and middle holes rather than the original connection of the bottom and middle. This connection ungates the sector and index driver.

Remove the letter "C" from the card type designation CFAX and mark a "D" in its place so that the card type becomes DFAX.

F.3 CDC 9766

Remove (Ch. I)		Remove (Ch. II)	
Sector +	J4-55	Sector +	J4-55
Sector -	J4-25	Sector -	J4-25
Index +	J4-48	Index +	J4-48
Index -	J4-18	Index -	J4-18

Move Wire (Ch. I)	Orgin	From	To
Sector +	PA01-5B	J3-55	J2-26
Sector -	PA01-5A	J3-25	J2-13
Index +	PA01-6B	J3-48	J2-24
Index -	PA01-6A	J3-18	J2-12

Move Wire (Ch. II)	Orgin	From	To
Sector +	PA03-5B	J3-55	J2-26
Sector -	PA03-5A	J3-25	J2-13
Index +	PA03-6B	J3-48	J2-24
Index -	PA03-6A	J3-18	J2-12

Rework transmitter card FTVV in location A01 (Ch. I) and A03 (Ch. II). Locate the jumper at center bottom of board (as viewed with connector on the right). Remove jumper and reinsert one set of holes lower (i.e., from center hole to hole below original jumper). Remove the letter "F" from the card type designation FTVV and mark "G" in its place so that the card type becomes GTVV.

NOTE - On later models of the 9766, CDC will ship units with an enhancement feature which will allow easy switchover to the B cable as follows: Cut the cable tie securing PD90 to the I/O cable and plug PD90 into JD90 pins 13 and 14 (Ch. I) and pins 11 and 12 (Ch. II) as indicated on the top of the connector.

F.4 CDC 9448

Sector and Index are on both the A and B cables.

F.5 TRIDENT DRIVES

Sector and Index are on both the A and B cables.

F.6 FUJITSU DRIVES

Sector and Index are on both the A and B cables.

APPENDIX G

INSTALLATION AND TROUBLESHOOTING

H.1 SC21/B1 INSTALLATION CHECKLIST

Use the following as an installation checklist for the SC21/B1 controller. Verify that every step is successfully completed before proceeding to the next one.

H.1.1 Controller Preparation

1. Visually inspect the controller for any sign of damage or defect.

2. Switch setting verification. See Appendix A.

3. Check CSR address_____

4. Check vector address_____

5. Controller serial number:_____

H.1.2 Drive Preparation

1. Determine a configuration from the Configuration Table on page A-3. Configuration selected:_____

2. Sector/Index signal must be on B cable. See appendix F.

3. Sector count: the SC21/B1 requires that the drive have 32 sectors. Refer to your drive manual for 32 sector setting.

4. Install the A cable (60-conductor, multicolor, flat ribbon) on the A cable connector on your drive.

   Install the B cable (26-conductor, gray, flat ribbon) on the B cable connector on your drive.

5. Install a drive terminator on the drive.

6. Unlock all head and spindle locking mechanism.

H.1.3 CPU Preparation

1. Select a Unibus slot in which to install the controller. Slot number chosen:_____

2. Remove the NPG jumper from CA1 to CB1 on the slot selected in step 1.

3. Remove the bus grant card from the selected slot.

4. Carefully install the SC21/B1 controller in the selected slot.

5. Connect the free ends of the A and B cables to the connectors on the controller.

H.1.4 Testing

1. Power up the CPU, verify that the Fault LED on the controller is blinking.

2. Power up the drive and verify that the Fault LED stops blinking.

3. Examine the controller registers and verify that there are no bus errors.

4. Verify that the drive is ready.

5. Hardware format: see subsection 3.7.3

6. Software format: see subsection 6.8

7. Performance Exerciser: see subsection 6.9

8. This completes the installation of the SC21/B1.

H.2 TROUBLESHOOTING

Use the following as a guide to troubleshooting the SC21 disk controller.

Sympton	Probably Cause	Action
Fault LED stays lit	Wrong switch setting	Check switch setting
	Cable installed backwards	Check cable orientation
	CPU power sequence	Power down CPU, then power up
	PROMs not well seated in sockets	Inspect PROMs for bent pins, or any pin out of its socket
	PROMs installed out of sequence	Verify PROM sequence as installed on controller
	Bad SPC slot	Try another SPC slot
	SW3 (red piano type) inadvertantly set	Reset all switches in this switch pack

	Hard failure	Contact Emulex technical support
Fault LED stays blinking when drive is ready	Bad cables	Replace cable or check for open connection
	No address plug or two identical plugs are installed	Install an address plug and make sure address is unique. Check address switch setting on drive
	Cables not properly connected	Reseat and reconnect all cables
		Cables on drive side must be connected on the selected channel is the dual port option is enabled
	Hard failure	Contact Emulex technical support
Cannot hardware format	Sector/Index signal on wrong cable	Verify that sector/index signal is on B cable and sector/index is ungated
	Bad cables	Replace cables
	Wrong instruction for hardware format command	Verify proper instruction and sequence of entry in subsection 3.7.3
	Wrong switch settings	Verify switch settings
	Drive problem	Contact drive manufacturer
	Hard failure	Contact Emulex technical support
Bus errors	NPG jumper not removed	Remove NPG jumper
	NPG jumper removed from wrong slot	Make sure correct NPG jumper has been removed
Fails Diag-nostics	Hard failure	Contact Emulex technical support

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