VT01 9-TRACK
TAPE DRIVE INTERFACE
TECHNICAL MANUAL

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VT0151001-00 Rev. A
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WARNING

This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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In all cases where equipment is to be returned to Emulex, a "Return Authorization" must be issued by the "Repair Center," (714) 662-5600.

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Section 1
GENERAL DESCRIPTION

1.1 Introduction

This manual contains information and applications data for the Emulex VT01 9-Track Tape Drive Interface. It is designed to be used for setup, installation, cabling, and programming of the VT01 interface. Installation and usage of software is described in the *Emulex VMEbus UNIX Software Installation and User's Guide*.

The contents of the manual are as follows:

Section 1	**General Description**
Section 2	**Specifications**
Section 3	**Installation**
Section 4	**Programming the VT01**
Section 5	**Theory of Operation**
Appendix A	**Cable Pin Assignments**

1.2 Overview

The VT01 is designed to interface a VMEbus based computer system with 9-track tape drives which use the Cipher-Pertec formatter interface. This double-height Eurocard is fully compatible with Revision C VMEbus Specifications.

Up to eight tape drives may be connected in daisy-chain fashion to the VT01 using 50-conductor ribbon cables. The VT01 supports tape densities up to 6250 bits-per-inch (bpi) at 100 inches-per-second (ips).

Data is transferred on both read and write by DMA using 16-bit or 32-bit data paths and 24- or 32-bit addressing. Data transfers are buffered by a 1024-byte FIFO which prevents overruns if DMA is delayed by bus latency.

1.2.1 Part Numbers

Table 1-1 lists the part numbers for the VT01 9-Track Tape Drive Interface and accessories.

Table 1-1. VT01 Part Numbers

Model	Part Number	Qty	Description
VT01	VT0110501-00	1	VT01 Controller Board
-----	-----	-	See Table 1-1 for ribbon cables
-----	VT0151001-00	1	*VT01 9-Track Tape Drive Interface Technical Manual*
-----	VS9951801-XX	1	Emulex Diagnostics and Driver; media on 9-track tape (-01)
-----			Emulex Diagnostics and Driver; media on 5.25 inch floppy disk, 360K bytes (-02)
-----			Emulex Diagnostics and Driver; media on 5.25 inch floppy disk, 1.2M bytes (-03)
-----	VS9950901	1	*Emulex VMEbus UNIX Software Installation and User's Guide*

1.3 Features

- Supports tape densities up to 6250 bpi.
- Buffered data transfers.
- Selectable response to VMEbus address modifiers.
- Selectable bus request and grant level.
- Selectable interrupt level.
- Selectable base I/O and vector address.

1.4 Compatibility

Note the following details about compatibility and restrictions on VT01 use:

- All NRZI tape drives used with the VT01 must be able to disable transmission of LRC and CRC data reliability bytes.
- DMA requests to the VT01 must be made one command at a time (no overlap is allowed).
- On the VT01, transfers of even byte counts that are less than 65,535 bytes must be made from even addresses only.

Section 2
SPECIFICATIONS

2.1 Specifications

Table 2-1 lists the specifications for the VT01 Interface.

Table 2-1. VT01 Specifications

Parameter	Description
Master Data Transfer Options	A32 - 31 address lines. D16 or D32 data lines. D16 - 16 data lines.
Address Modifiers	Any; loaded from host CPU.
Slave Data Transfer Options	A16 - 15 address lines. D16 - 16 data lines.
Address Modifiers	2D (short supervisory) or 29 (user supervisory)
Requester Options	RWD - release when done. Any one of R(0), R(1), R(2), or R(3) (STAT) - static selection of request line.
Interrupter Options	Any one of I(1), I(2), I(3), I(4), I(5), I(6), or I(7) (STAT) - static selection of interrupt request line.
Environmental Options	
Operating Temperature	0-70 degrees C
Maximum Relative Operating Humidity	90%
Power Options	3.0 A max (2.4 A typ) at +5 VDC
Physical Configuration	EXP (expanded) - double-height Eurocard (160mm x 233mm).

Section 3
INSTALLATION

3.1 Overview

This section describes the procedures for installing and checking the VT01 interface. The subsection titles are listed below to serve as an outline of the procedure.

Subsection	Title
3.1	Overview
3.2	Inspection
3.3	Setup
3.4	Installing the VT01 in a Backplane
3.5	Cabling
3.6	Power-Up and System Verification

3.1.1 Maintaining FCC Class A Compliance

Emulex has tested the VT01 interface for FCC compliance. The VT01 complies with FCC Class A limits for radiated and conducted interference.

3.2 Inspection

Emulex products are shipped in special containers designed to provide full protection under normal shipping conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

Unpack the VT01 interface and, using the shipping invoice, verify that all equipment is present. Verify also that model or part number (P/N) designation, revision level, and serial numbers agree with those on shipping invoice. Subsection 1.2 explains model numbers. These verifications are important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately. If the equipment must be returned to Emulex, it should be shipped in the original container.

Visually inspect all components after unpacking. Check for such items as bent or broken connector pins, damaged components or any other evidence of physical damage.

Examine all socketed components carefully to ensure they are properly seated.

3.3 Setup

Use Figure 3-1 as a reference for switch, jumper, and connector locations on the VT01 Interface board.

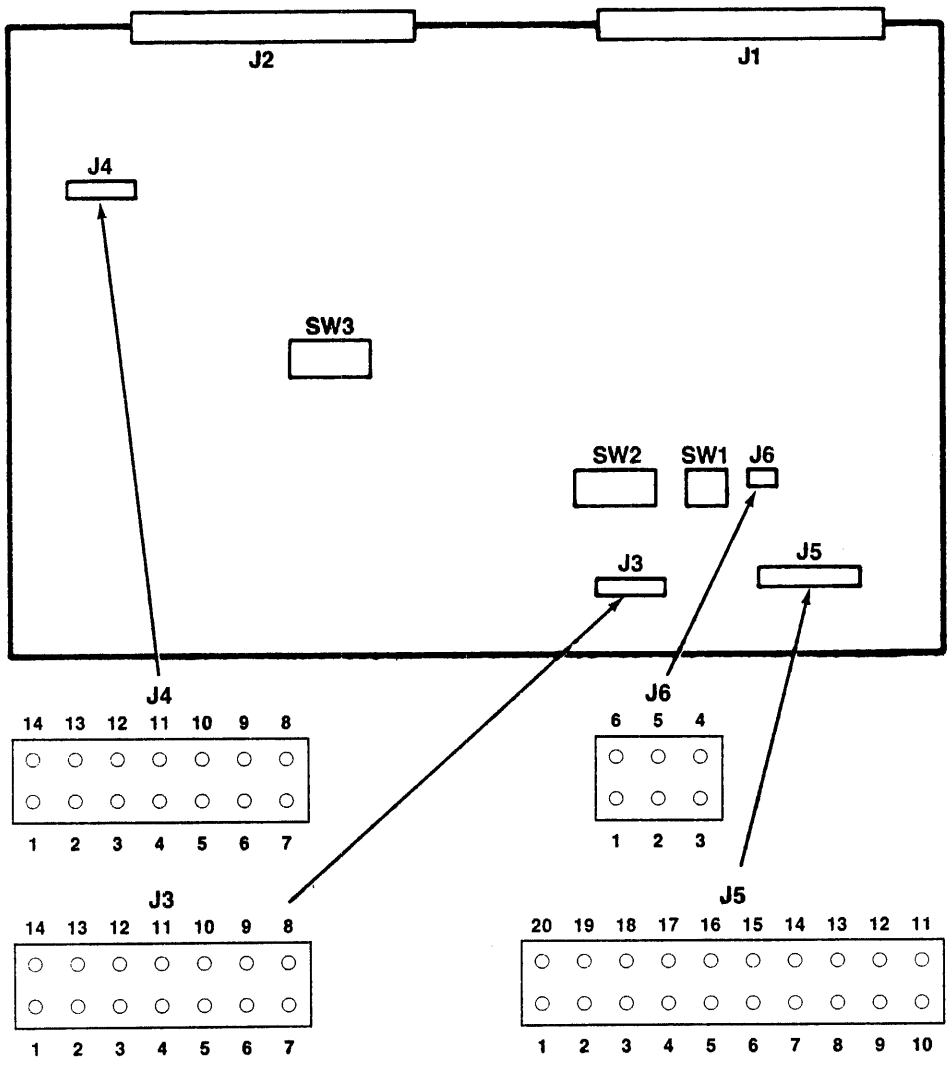


Figure 3-1. VT01 Board Component Locations

3.3.1 Jumper Settings

The jumper functions are as follows:

Bus Request/Grant:	J5
I/O Address Modifier:	J6
Interrupt Request and Acknowledge:	J3 and J4

3.3.1.1 Bus Request/Grant - J5

Jumpers on J5 (Figure 3-2) select the VMEbus request and bus grant levels that are to be used by the DMA circuitry.

All VMEbus masters must request the VMEbus prior to use by means of one of the BR0-3 lines. Only one of these lines may be used by a master. A request line is selected by jumpering across the jumper area from BRX to the desired request level.

If your system's arbiter is configured for "option one" bus arbitration, it will respond only to requests which occur on BR3. This is the simplest form of VMEbus arbitration. If your arbiter supports Round Robin or Priority arbitration, any of the lines BR0-3 may be selected.

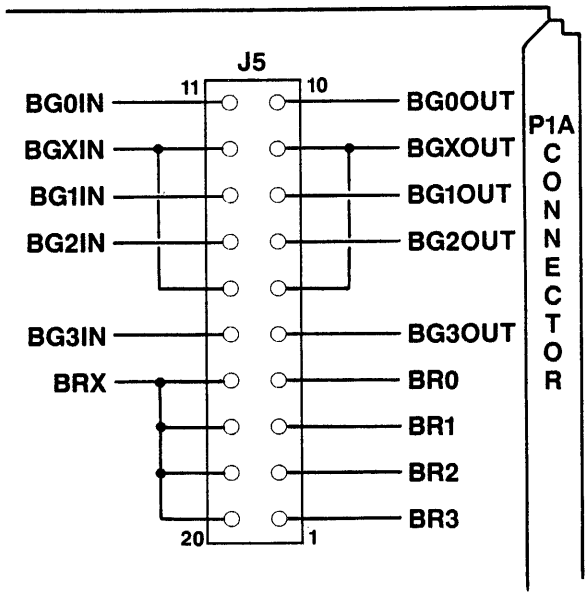


Figure 3-2. VMEbus Request/Grant Jumper Area

Once a master has requested the VMEbus via one of the BR lines, the system arbiter responds by issuing a bus grant on the corresponding BG line. If the request is on BR2, for example, the arbiter in the system will issue the grant on the BG2 line. Therefore, the levels selected for request and grant must be the same.

Grant-in is selected by jumpering from one of the BGXIN posts to the desired level. Grant-out is selected by jumpering from one of the BGXOUT posts to the desired level. The three unused grant levels must be jumpered across from grant-in to grant-out on each level to maintain the continuity of the unused grant daisy-chains. The four valid jumper settings for VMEbus request/grant are shown in Figure 3-3 with the VT01 board positioned so that the P3 and P4 connectors are on the right and the front panel is on the left.

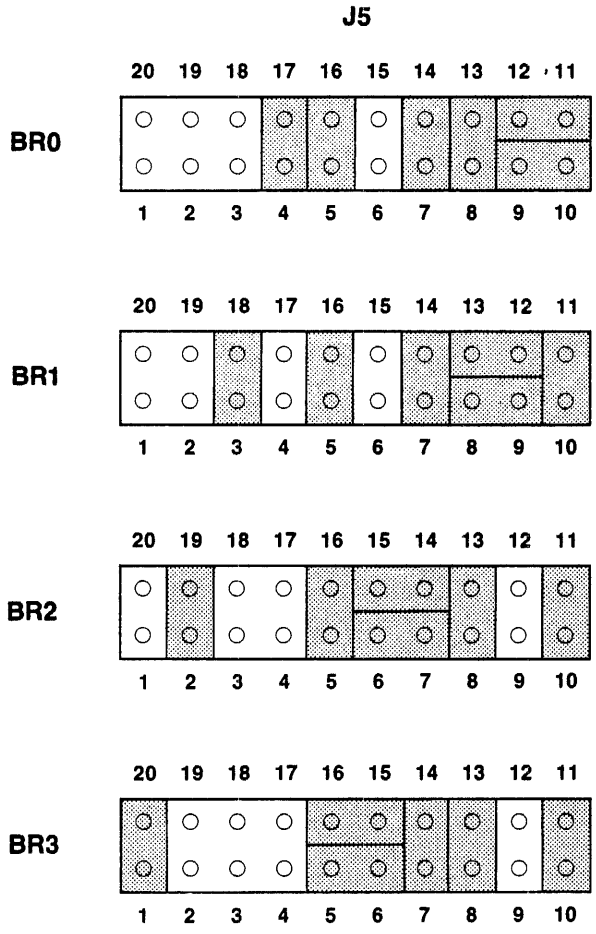


Figure 3-3. VMEbus Request/Grant Jumper Settings

3.3.1.2 I/O Address Modifier - J6

Jumpers in J6 (Figure 3-4) select the type of address modifier that the board, as a slave, will respond to on Input/Output accesses. Address modifier types may be user-short, supervisory-short, or both. Normally, I/O access is performed by the operating system which requires the supervisory address modifier. Address length is short; that is, 15 address lines, A01 through A15.

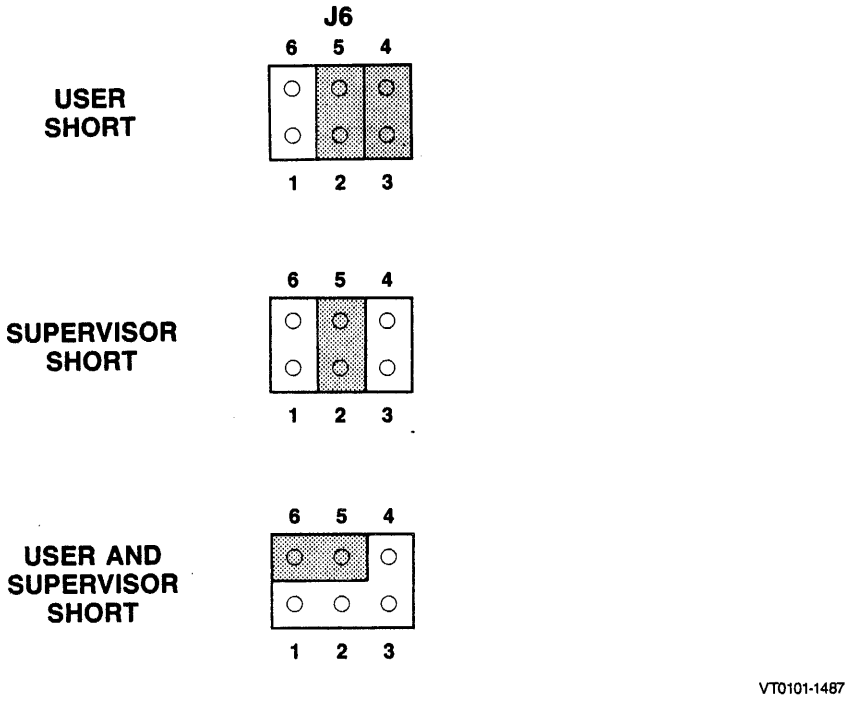
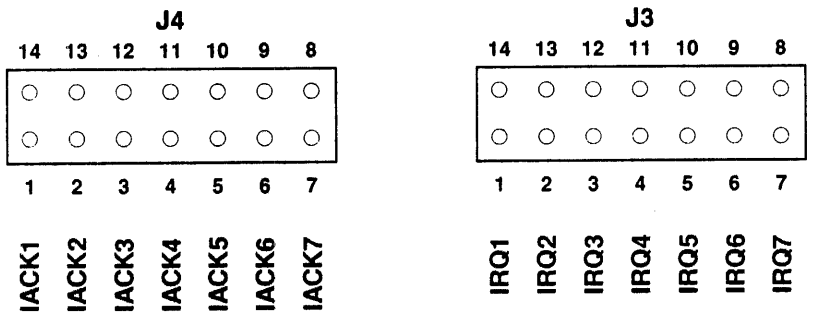


Figure 3-4. I/O Address Modifier Selection

3.3.1.3 Interrupt Request and Acknowledge - J3, J4

The interrupt request level is selected by a jumper in J3. The interrupt acknowledge level is selected by a jumper in J4. See Figure 3-5. The interrupt acknowledge level is used in the decoding of the lower three address lines in the interrupt-acknowledge cycle. For the board to function properly J3 and J4 must be jumpered at the same level.



NOTE: J4 AND J3 MUST BE JUMPERED AT THE SAME LEVEL

VT0101-1488

Figure 3-5. Interrupt Request Jumpers

3.3.2 Switch Settings

The switch functions are as follows:

Base I/O Address:	SW1 and SW2
Interrupt Vector:	SW3

3.3.2.1 Base I/O Address - SW1, SW2

The settings of switches SW1 and SW2 (Figure 3-6) determine the base I/O address for eight 16-bit I/O ports which are used to control the VT01. Input/Output ports are discussed further in Section 4, Programming.

Switch settings for a base I/O address of E000H are shown in Figure 3-7.

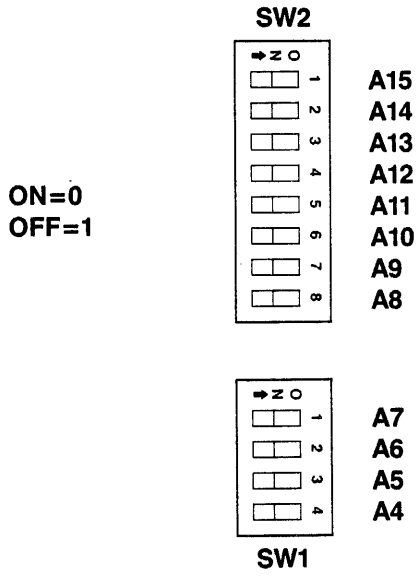


Figure 3-6. I/O Address Switches

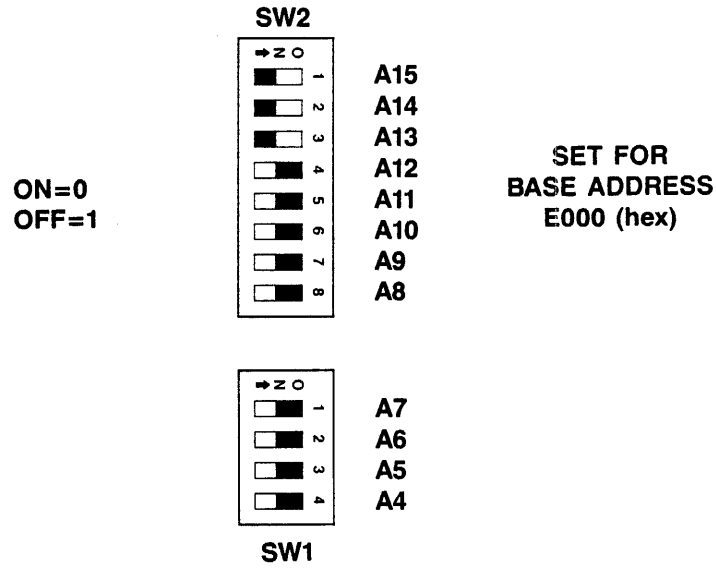


Figure 3-7. Base I/O Address - Sample Setting

3.3.2.2 Interrupt Vector - SW3

DIP switch SW3 (Figure 3-8) is used to set the vector number which is issued by the board during an interrupt-acknowledge cycle.

Figure 3-9 depicts a sample interrupt vector address setting of 85H.

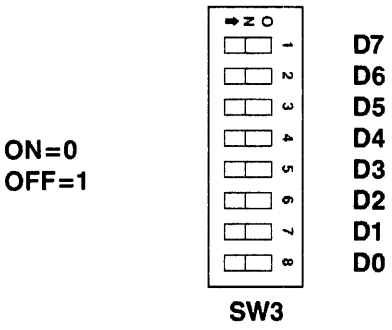


Figure 3-8. Interrupt Vector Switch

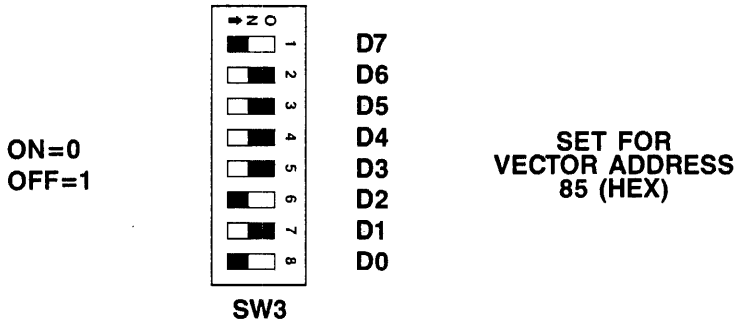


Figure 3-9. Interrupt Vector Switch - Sample Setting

3.4 VT01 Installation in a Backplane

Use the procedure below to install the VT01 in a backplane.

1. Shut down the operating system and **remove the AC power.**

2. Remove the side (or top) covers from the CPU cabinet to make the VMEbus accessible.

3. Select a card slot for the VT01. **If switch and jumpers settings on the VT01 give it a low priority on the VMEbus, then the VT01 should be given a high-priority slot in the backplane.**

4. Remove any jumpers (look especially for NPR and IRQ) already located in the selected slot.

5. Install the VT01 board by firmly plugging it into the backplane. Orient the components on the board in the same direction as the CPU and other modules.

   Be sure that the board is properly seated in the throat of the connector before attempting to seat the board using the extractor handles.

6. Connect cables using the information in subsection 3.5.

3.5 Cabling

After installing the VT01 in a VMEbus computer card cage, connect the VT01 to a 9-track tape drive with two 50-conductor ribbon cables. Use Figure 3-10 and the procedure below. Emulex part numbers for the cables are listed in Table 3-1. Pin-out information for VT01 J1 and J2 connectors is contained in Appendix A.

1. The cable labeled P1, connects connector P1 (or P4) on the tape drive to connector J1 on the VT01.

   Similarly, the P2 cable connects connector P2 (or P5) on the tape drive to connector J2 on the VT01.

2. Pin 1 of each connector on the VT01 is designated by an arrow. Be sure to align the pin-1 edge of each cable with the pin-1 marking beside the connector.

NOTE

When using a streaming tape drive **and** a start/stop tape drive, place each at a different formatter address.

Unformatted tape drives are connected to a formatted tape drive via special connectors (not P1, P2, or P4, P5). See the tape drive documentation for details.

CAUTION

Do not add or remove cables to tape drive while UNIX system is running. This causes unpredictable controller actions (NXM accesses, spurious interrupts, etc.)

Table 3-1. Emulex Cable Part Numbers

Item	Part Number	Description
1	TU1211201-03	8-foot 50-Pin Unshielded Cable
2	TU1211201-04	15-foot 50-Pin Unshielded Cable
3	TU1211201-05	25-foot 50-Pin Unshielded Cable
4	TU1211201-06	35-foot 50-Pin Unshielded Cable
5	TU1210402-00	Daisy-Chain Adapter
Note: Cables connect the VT01 to a tape drive, or connect one tape drive to another via the daisy-chain adapter.		

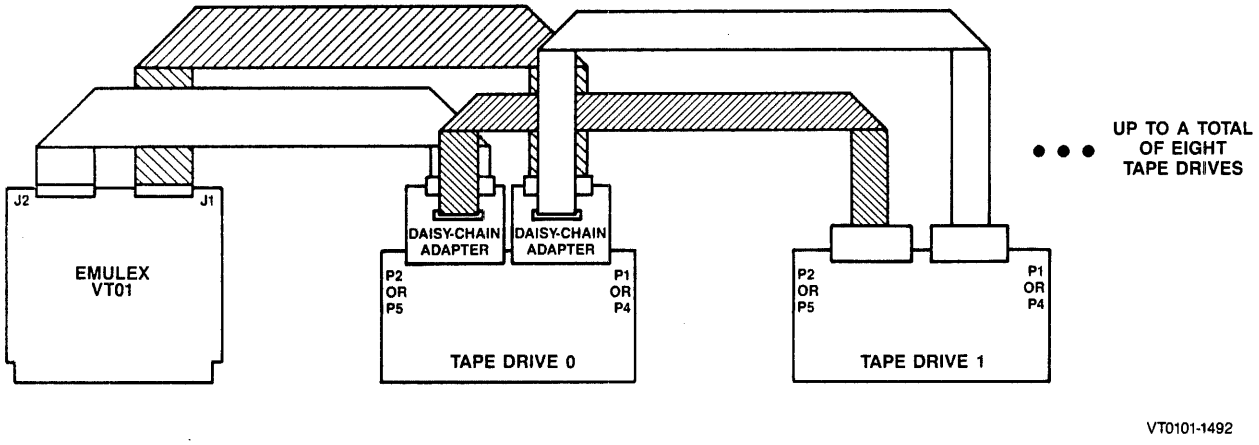


Figure 3-10. VT01 Cabling

4.1 Overview

The information contained in this section is based on the assumption that the user has a basic understanding of the Cipher-Pertec tape format and of VMEbus specifications. This section contains the following subsections:

Subsection	Title
4.1	Overview
4.2	Address Offsets
4.3	DMA Address
4.4	Byte Count
4.5	Control Word
4.6	Status Word
4.7	Interrupt Read and Interrupt Write
4.8	Address Modifier

4.2 Address Offsets

Eight I/O ports (Table 4-1) are used to control the VT01. Each port is 16-bits wide and can be accessed either one byte at a time or one word at a time.

Table 4-1. Address Offsets

Offset	Read Port	Write Port
0x0	-	DMA Address
0x2	Byte Count	Byte Count
0x4	Status Word	Control Word
0x6	Interrupt Read	Interrupt Write
0x8	-	Address Modifier
0xA	-	-
0xC	-	-
0xE	-	-

4.3 DMA Address - Offset 0 (Write Only)

The DMA address must be loaded into Port 0 before a command is issued (excluding rewind and off-line commands). The most significant word of the 32-bit address is loaded first followed by the least significant word. The most significant word is shifted up 16 bits automatically to position it for addressing memory. The least-significant bit of the least-significant word is ignored. If 24-bit addressing is used the most-significant byte of the 32-bit address is ignored. The address must fall on a word boundary.

4.4 Byte Count - Offset 2 (Read/Write)

Before a command is issued (excluding rewind and off-line commands), a byte count must be loaded into Port 1. The byte count is 16-bits wide. Reading this port returns the byte count after a command has been performed. The byte count must be an even number.

4.5 Control Word - Offset 4 (Write Only)

Port 2 is used to select the tape drive and to issue commands to it.

15	14	13	12	11	10	9	8
32 BIT	OFL	RWD	DEN	FEN	FAD	TAD1	TAD0

7	6	5	4	3	2	1	0
GO	GO TOGGLE	X	ERASE	EDIT	WFM	WRT	REV

Bit 15, 32-Bit (32 BIT) - should be set to use longword DMA transfers between the VT01 and VMEbus memory. The default is word (16-bit) DMA transfers.

Bit 14, Off Line (OFL) - must be set to zero before being set to one. Upon being set to one, this bit causes the tape drive to go off line. On some tape drives, setting this bit to one causes the tape to be rewound before the drive goes off line.

Bit 13, Rewind (RWD) - must be set to zero before being set to one. Upon being set to one this bit causes the tape to be rewound.

Bit 12, Density (DEN) - is used in multiple density drives to select high or low density. In other drives, such as the Cipher F880, this bit is used to select high or low tape speed.

Bit 11, Formatter Enable (FEN) - may be used to terminate runaway read, write, and search commands.

Bits 10-8, Formatter Address (FAD) and Transport Address (TAD) - are used to address one of eight possible drives.

Bit 7 - is the pulsed GO line which is normally used to initiate a command. This bit must be set to a 0 before issuing a 1 to initiate a command.

Bit 6 - controls the GO line directly and can be used to produce extended interrecord gaps on some drives. It should be left at 0, if bit 7 is used. Bit 7 must always be used to initiate a command.

Bits 4, 3, 2, 1, and 0 - encode the command to be issued to the formatter. See the tape drive manual for the codes generated by various combinations of Erase, Edit, Write File Mark, Write, and Reverse.

4.6 Status Word - Offset 4 (Read Only)

This port is normally read after a command has been executed to give error conditions and interface status information.

15	14	13	12	11	10	9	8
IDENT	FPT	REWD	NRZ	NTC	RLE	CER	HER

7	6	5	4	3	2	1	0
RDY	DBY	FBY	LP	EOT	ONL	FMK	ERROR

Bit 15, Identification (IDENT) - identifies phase-encoded tapes.

Bit 14, File Protect (FPT) - indicates the absence of a write-enable ring in the tape reel.

Bit 13, Rewinding (REWD) - indicates that the tape is rewinding.

Bit 12, Non-Return to Zero (NRZ) - is ignored in drives that use phase encoding.

Bit 11, No Terminal Count (NTC) - indicates that the terminal count (see section 4.2 I/O Port 1, Byte Count) was not zero at the completion of a command requesting DMA. **NTC is an error indication.**

Bit 10, Record Length Error (RLE) - indicates more data was waiting in the FIFO to be transferred when the command completed. This data cannot be recovered directly from the FIFO.

The data must be flushed with a non-DMA command prior to another DMA command or the data will be written randomly to memory.

Bits 9 through 1 - are standard status outputs for a nine-track tape drive. The status ouput bits are defined as follows:

CER	Corrected error
HER	Hard error detected
RDY	Tape ready
DBY	Data busy active
FBY	Formatter busy
LP	Load point
EOT	End of tape
ONL	On-line status
FMK	Filemark detected

Bit 0, Error - indicates that **any one of the three error conditions reported in the Interrupt Read port has occurred.**

4.7 Interrupt Read and Interrupt Write - Offset 6 (Read/Write)

This port controls interrupts and returns error conditions.

15	14	13	12	11	10	9	8
FIFO OVER-FLOW	FIFO UNDER-FLOW	BERR	X	X	X	X	X

7	6	5	4	3	2	1	0
X	X	X	X	X	X	INT ENABLE FBY	INT ENABLE DBY

Bit 15 - is read only and indicates an attempt to write to a full FIFO.

Bit 14 - is read only and indicates an attempt to read from an empty FIFO.

Bit 13 - is read only and indicates that a Bus Error (BERR) was received at least once from memory during a command.

Bits 1 and 0 - control interrupts at the end of a command when Formatter Busy (FBY) or Data Busy (DBY) go false. If bit 1 is set, the VT01 will request an interrupt on the VMEbus as soon as the FBY signal goes false. Similarly, bit 0 set, causes the VT01 to request an interrupt as soon as the DBY signal goes false.

4.8 Address Modifier - Offset 8 (Write Only)

Bits 0 to 5 can be written with the address modifiers that are to be used by the VT01 when it accesses memory via a DMA cycle. These bits are latched on the board and need not be issued with every command. They must, however, be set before issuing the first command.

See the VMEbus Specifications manual (Revision C) for more information on address modifiers.

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
X	X	AM5	AM4	AM3	AM2	AM1	AM0

Section 5
THEORY OF OPERATION

5.1 Overview

The VT01 acts as both a bus slave and a bus master. The slave portion consists of eight contiguous I/O ports, 16 bits wide, that allow commands to be set up and executed. Once a command has begun, the master portion of VT01 takes over and transfers the data via DMA. DMA cycles take place on the bus one word or longword at a time. Arbitration for the bus takes place between each cycle.

Every 16-bit transfer must have an even numbered byte count and a DMA address falling on a word boundary. Every 32-bit (longword) transfer must start on a longword boundary and have a byte count that is a multiple of four. In 32-bit mode, the I/O port may not be accessed while DMA transfers are in progress. Completion of an operation must therefore be monitored by using interrupts (this does not include rewinds).

Two 512-byte FIFOs buffer the data on the VMEbus bus to the tape interface in both directions. On a read-from-tape, for example, byte-wide data from the tape interface is written alternately to the two FIFOs. A signal from the FIFOs indicating they are not empty initiates DMA cycles that read a byte from each FIFO to form a 16-bit word for transfer to memory. This memory transfer continues until both FIFOs are empty. If DMA is delayed by bus latency, the FIFO will continue to receive data from the tape interface to be transferred later when the bus becomes available.

On a write-to-tape, DMA cycles write 16-bit data into the two FIFOs until the byte count is zero or the FIFOs are full. The tape interface reads byte-wide data from the two FIFOs alternately until they are empty.

When a command terminates, an interrupt is issued and status information regarding errors and formatter status can be read from the slave portion of the board. Interrupt-enables allow the selection of an interrupt when either FBY or DBY go inactive at the end of a command. Any error conditions reported are cleared when a new command is issued.

Appendix A
CABLE PIN ASSIGNMENTS

Table A-1. Connector P1 Pin Identification

Pin	Signal	Name
2	FBY	Formatter Busy
4	LWD	Last Word
6	W4	Write Data 4
8	GO	Initiate Command
10	W0	Write Data 0
12	W1	Write Data 1
14	-	-
16	-	-
18	REV	Reverse
20	REW	Rewind
22	-	-
24	W7	Write Data 7
26	W3	Write Data 3
28	W6	Write Data 6
30	W2	Write Data 2
32	W5	Write Data 5
34	WRT	Write
36	-	-
38	EDIT	Edit
40	ERASE	Erase
42	WFM	Write File Mark
44	-	-
46	TAD0	Transport Address 0
48	-	-
50	RD3	Read Data 3

Table A-2. Connector P2 Pin Identification

Pin	Signal	Name
1	-	-
2	RD0	Read Data 0
3	RD1	Read Data 1
4	LP	Load Point
6	RD4	Read Data 4
8	RD7	Read Data 7
10	RD6	Read Data 6
12	HER	Hard Error
14	FMK	File Mark
16	IDENT	Identification
18	FEN	Formatter Enable
20	RD5	Read Data 5
22	EOT	End of Tape
24	OFL	Offline
26	NRZ	Non-Return to Zero
28	RDY	Ready
30	REWD	Rewinding
32	FPT	File Protect
34	RSTR	Read Strobe
36	WSTR	Write Strobe
38	DBY	Data Busy
40	-	-
42	CER	Corrected Error
44	ONL	Online
46	TAD1	Transport Address 1
48	FAD	Formatter Address
50	DEN	Density

VT01 PROGRAMMING REFERENCE CARD

ADDRESS OFFSETS

Offset	Read Port	Write Port
0×0	—	DMA Address
0×2	Byte Count	Byte Count
0×4	Status Word	Control Word
0×6	Interrupt Read	Interrupt Write
0×8	—	Address Modifier

DMA Address — Offset 0 (Write Only)

The 32-bit DMA address must be loaded into Port 0 before a command is issued (excluding rewind and off-line commands). The most significant word is loaded first followed by the least significant word. The least-significant address bit is ignored. If 24-bit addressing is used, the most-significant byte is ignored. The address must fall on a word boundary.

Byte Count — Offset 2 (Read/Write)

Before a command is issued (excluding rewind and off-line commands), a 16-bit byte count must be loaded into Port 1. This port returns the byte count after a command has been performed. The byte count must be an even number.

Control Word — Offset 4 (Write Only)

Port 2 is used to select the tape drive and to issue commands to it.

15	14	13	12	11	10	9	8
32 BIT	OFL	RWD	DEN	FEN	FAD	TAD1	TAD0

7	6	5	4	3	2	1	0
GO	GO TOGGLE	X	ERASE	EDIT	WFM	WRT	REV

Bit 15, 32-Bit — Set to use longword DMA transfers. The default is word transfers.

Bit 14, Off Line — Set to zero then one to cause the tape drive to go off line. On some tape drives, this will cause the tape to rewind before going off line.

Bit 13, Rewind — Set to zero then one to rewind the tape.

Bit 12, Density — Used in multiple density drives to select high or low density. In other drives, such as the Cipher F880, this bit selects high or low tape speed.

Bit 11, Formatter Enable — Terminates runaway read, write, and search commands.

Bits 10–8, Formatter Address (FAD) and Transport Address (TAD) — Address one of eight possible drives.

Bit 7 — Pulsed GO line. This bit must be set to 0 then 1 to initiate a command.

Bit 6 — Controls the GO line directly and can be used to produce extended interrecord gaps on some drives. It should be left at 0 if bit 7 is used.

Bits 4, 3, 2, 1, and 0 encode the formatter command. See the tape drive manual for the code combinations of Erase, Edit, Write File Mark, Write, and Reverse.

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VT01 PROGRAMMING REFERENCE CARD

ADDRESS OFFSETS

Offset	Read Port	Write Port
0×0	—	DMA Address
0×2	Byte Count	Byte Count
0×4	Status Word	Control Word
0×6	Interrupt Read	Interrupt Write
0×8	—	Address Modifier

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The 32-bit DMA address must be loaded into Port 0 before a command is issued (excluding rewind and off-line commands). The most significant word is loaded first followed by the least significant word. The least-significant address bit is ignored. If 24-bit addressing is used, the most-significant byte is ignored. The address must fall on a word boundary.

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GO	GO TOGGLE	X	ERASE	EDIT	WFM	WRT	REV

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Bits 4, 3, 2, 1, and 0 encode the formatter command. See the tape drive manual for the code combinations of Erase, Edit, Write File Mark, Write, and Reverse.

VT0101-1798

Status Word — Offset 4 (Read Only)

This port hold error and interface status information after a command has executed.

15	14	13	12	11	10	9	8
IDENT	FPT	REWD	NRZ	NTC	RLE	CER	HER
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	DBY	FBY	LP	EOT	ONL	FMK	ERROR

Bit 15, Identification — Identifies phase-encoded tapes.

Bit 14, File Protect — Indicates the absence of a write-enable ring in the tape reel.

Bit 13, Rewinding — Indicates that the tape is rewinding.

Bit 12, Non-Return to Zero — Is ignored in drives that use phase encoding.

Bit 11, No Terminal Count — An error indication that the terminal count was not zero at the completion of a command requesting DMA.

Bit 10, Record Length Error — Indicates more data waiting in the FIFO to be transferred after the command completed.

Bits 9 through 1 — Standard status outputs for a nine-track tape drive, as follows:

CER	Corrected error	DBY	Data Busy Active	EOT	End of tape
HER	Hard error detected	FBY	Formatter Busy	ONL	ON-line status
RDY	Tape Ready	LP	Load Point	FMK	Filemark detected

Bit 0, Error — An error condition reported in the Interrupt Read port has occurred.

Interrupt Read and Interrupt Write — Offset 6 (Read/Write)

This port controls interrupts and returns error conditions.

15	14	13	12	11	10	9	8
FIFO OVER-FLOW	FIFO UNDER-FLOW	BERR	X	X	X	X	X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X	X	X	X	X	X	INT ENABLE FBY	INT ENABLE DBY

Bit 15 — Read only, indicates an attempt to write to a full FIFO.

Bit 14 — Read only, indicates an attempt to read from an empty FIFO.

Bit 13 — Read only, indicates that a Bus Error (BERR) was received during a command.

Bits 1 and 0 — These bits control interrupts at the end of command when FBY or DBY go false. Set bit 1 to request a VMEbus interrupt when the FBY signal goes false. Set bit 0 to request and interrupt when the DBY signal goes false.

Address Modifier — Offset 8 (Write Only)

Bits 0 to 5 hold the address modifiers for the VT01 when it uses DMA. They must be set before issuing the first command. These bits are latched on the board and need not be issued with every command.

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X	X	AM5	AM4	AM3	AM2	AM1	AM0

Status Word — Offset 4 (Read Only)

This port hold error and interface status information after a command has executed.

15	14	13	12	11	10	9	8
IDENT	FPT	REWD	NRZ	NTC	RLE	CER	HER
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDY	DBY	FBY	LP	EOT	ONL	FMK	ERROR

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7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X	X	X	X	X	X	INT ENABLE FBY	INT ENABLE DBY

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Bit 14 — Read only, indicates an attempt to read from an empty FIFO.

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15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X	X	AM5	AM4	AM3	AM2	AM1	AM0

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