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# American National Standard

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for information systems –

## intelligent peripheral interface – physical level

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American National Standard  
for Information Systems –  
**Intelligent Peripheral Interface –  
Physical Level**

Secretariat

**Computer and Business Equipment Manufacturers Association**

Approved April 24, 1986

**American National Standards Institute, Inc**

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# Foreword

(This Foreword is not part of American National Standard X3.129-1986.)

This standard is a definition of the physical portion of a family of standards called the Intelligent Peripheral Interface (IPI). It is a new high-performance, general-purpose parallel peripheral interface. This standard responds to an industry market need (expressed both by users and manufacturers) to limit the increasing costs in hosts associated with changes in peripherals. The intent of the IPI is to isolate the host (CPU), both hardware and software, from changes in peripherals by providing a "function-generic" command set to allow the connection of multiple types of peripherals (disks, printers, tapes, communications). To smooth the transition from the current methods to the generic approach, the IPI also supports device-specific command sets to aid in bridging the gap between the two approaches.

To accomplish this set of goals, the design of the IPI includes device-specific and device-generic command sets, both utilizing a common physical bus. The device-specific command set provides:

- (1) Device-oriented control
- (2) Physical Data Addressing
- (3) Timing Critical Operations
- (4) Lower Device Cost

The device-generic command set provides a higher level of functionality and portability. It includes:

- (1) Host/Device Independence
- (2) Logical Data Addressing
- (3) Timing Independence
- (4) Command Queuing Capability

A system is not restricted to the use of one level of command set or the other. It is possible that both levels of command sets will be utilized with a given system's architecture to balance such parameters as system performance, cost, and peripheral availability. It is also possible for the host to provide for migration from device-specific to device-generic levels while still retaining the same physical interface.

The development of an Intelligent Peripheral Interface (IPI) was begun after a preliminary investigation had been completed. The earliest proposals were made by participants of Task Group X3T9.3 in late 1978. At that time, the Task Group decided generic-oriented peripheral interfaces were not yet ready for standardization and that the group should concentrate on device-oriented interfaces and the system-oriented, high-speed serial interfaces. The group acknowledged the desirability of higher level intelligent commands by reserving code fields in American National Standard for Interface between Rigid Disk Drives and Their Host(s), ANSI X3.101-1983, during its April 1980 meeting.

The basic architecture of the resultant IPI was first proposed at the X3T9.3 August 1980 meeting. In addition to the 1978 proposal, complete company implementations were proposed by several manufacturers from August 1980 to August 1981. These proposals resulted from the initiative of the contributors and from wide-spread solicitation by the task group.

X3T9.3 agreed upon preliminary functional requirements during the October 1980 meeting, which included the following:

- (1) Parallel transfer
- (2) Command and Data Handshaking
- (3) Allowance for high-speed transfers without Handshaking
- (4) Minimum transfer rate to 5 Megaoctets per second

X3T9.3 began work on the IPI in 1981 in response to an emerging need for a higher performance peripheral interface. Coincidental with the need for higher performance was the availability of low-cost VLSI circuit technologies, allowing increased intelligence in the peripheral device. These needs were confirmed by large and active participation from all areas of the computer industry.

The fundamental characteristics that the group achieved included the following:

- (1) Single or dual octet transfers
- (2) Data rates of at least 10 megabytes per second
- (3) Cable lengths extending from 5 to 125 meters depending upon type of transmitter and cable type
- (4) Low-cost, commonly available components
- (5) High level of maintainability and availability
- (6) A multilevel command structure allowing different levels of intelligence in the peripherals
- (7) A definition that facilitates evolutionary changes in the levels with minimal impact on software and hardware components
- (8) Definitions supporting an extensive group of peripheral devices including disks, tape, communications equipment, printers, and the like, with a common choice of interface hardware and commands

Suggestions for improvement of this standard will be welcome. They should be sent to the Computer and Business Equipment Manufacturers Association, 311 First Street, NW, Suite 500, Washington, D.C. 20001.

This standard was processed and approved for submittal to ANSI by Accredited Standards Committee on Information Processing Systems, X3. Committee approval of the standard does not imply that all committee members voted for approval. At the time it approved this standard, the X3 Committee had the following members:

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# American National Standard for Information Systems – Intelligent Peripheral Interface – Physical Level

## 1. Scope and Purpose

**1.1 Scope.** This American National Standard provides the mechanical, electrical and bus protocol requirements for a high-performance interface for peripheral devices attached to powerful computers.

The physical interface described in this document can be operated at rates up to 10 megabytes per second and over distances of up to 125 meters, depending upon circuit and cable implementation choices.

**1.2 Purpose.** The purpose of this standard is to facilitate the development and utilization of computer systems by providing a common interface at the physical level that provides for connection of peripherals (disks, tapes, printers, terminals, and the like) with diverse characteristics.

### 1.3 Description of Sections

Section 1 contains the introductory material.

Section 2 lists the publications referenced in this standard.

Section 3 provides a glossary.

Section 4 specifies the classes of electrical and mechanical connections defined by this standard. These specifications cover drivers, receivers, line termination, connectors, and cable parameters

Section 5 specifies control sequences required to implement master/slave interactions.

Section 6 describes the relationship between this standard and its companion standard, which covers logical use of the interface.

Section 7 provides detailed timing information.

**1.4 Editorial Conventions.** Certain terms used in this standard that are proper names of signals, state mnemonics, or similar terms are printed in

uppercase to avoid possible confusion with other uses of the same words; e.g., BUS A, SLAVE IN, SYNC OUT, DESEL, SLAVEND. Any lowercase uses of these words have the normal English meaning.

A number of conditions, sequence parameters, events, English text, states or similar terms are printed with the first letter of each word in uppercase and the rest lowercase; e.g., In, Out, Selective Reset, Bidirectional, Bus Control, Operation Response. Any lowercase uses of these words have the normal English meaning.

## 1.5 Physical Interface

**1.5.1 Purpose.** The purpose of the interface is to exchange information between connected machines, and meet the criteria of:

(1) *Content Independence.* The operation of the interface is not affected by the contents of Information Transfers.

(2) *Speed Independence.* The control of the interface is not timing critical in handling of the interface protocol.

(3) *Protocol Integrity.* The integrity of the protocol sequences is ensured by requiring that each signal change be handshaked. No more than one signal is permitted to change at any time, except during optional Data Streaming transfers.

**1.5.2 Characteristics.** The characteristics of the physical interface are as follows:

(1) Master/slave mode of execution is used.

(2) There is one master only.

(3) Master selects slave.

(4) A daisy-chained cable consisting of 24 signals is used.

(5) Up to 8 slaves are allowed, with up to 16 facilities per slave.

(6) Bus Exchanges are used to frame Information Transfers and are executed only as interlocked and unidirectional.

(7) Information Transfers occur using either the unidirectional configuration or in a 16-bit bidirectional configuration. The two can coexist on the same cable.

(8) Information Transfers can be terminated in either direction by either the master or the slave.

(9) Information Transfers are asynchronous and interlocked except during Data Streaming.

(10) Except for Selection, a master can allocate control of interface functions to a dominant slave.

**1.6 Configuration Characteristics.** The IPI has been designed to operate with three defined elements of a computer system; master, slave and facility.

**1.6.1 Master.** The master manages the slaves and is responsible for control of the interface. It is the master's responsibility to operate the slaves according to their capabilities.

**1.6.2 Slave.** The slave is managed by the master and may or may not have intelligence, depending on the command set it is capable of executing. In an intelligent configuration, it can support a master that is oriented to generic device characteristics, such as a disk with 22 000 blocks of data, each 512 bytes long. In a device-oriented configuration, it can support a master oriented to specific device characteristics; e.g., a disk with 10 000 bytes/track, 7 tracks/cylinder, 500 cylinders/actuator. A facility is addressable through the slave.

**1.6.3 Facility.** The facility is addressable through the slave. It is the responsibility of the slave to manage the facility. A facility may or may not have generic functionality and may or may not be a device.

**1.6.4 Multi-tier Structure.** Configurations of the IPI can be tiered in a hierarchical manner to provide a measure of compatibility between the different functional requirements of system utilization.

Figure 1 illustrates a mainframe configuration in which a Storage Director is both slave to the CPU and master to the String Control. The CPU can directly address the String Controls through the Storage Director.

The String Control is both slave to the Storage Director and master to the Devices. The Storage Director can directly address devices through the String Control.

Figure 2 illustrates a minicomputer configuration in which the Controller is both

slave to the CPU and master to the Devices. The CPU can directly address devices through the Controller.

NOTE: The interface between slave and facility need not be IPI, but if it is, two separate IPI interfaces are needed to obtain 16 addresses.

**1.7 Signal Nomenclature.** The nomenclature used to define voltage levels, signal states, logical states, and their correlation to each other is defined in Table 1.

## 2. Referenced Publications

**2.1 American National Standards.** This standard is intended to be used in conjunction with the following American National Standards. When these standards are superseded by revisions approved by the American National Standards Institute, Inc, the revisions shall apply.

ANSI X3.130-1986, Information Systems — Intelligent Peripheral Interface — Device-Specific Command Sets for Magnetic Disk Drives

ANSI X3.132<sup>1</sup>, Information Systems — Intelligent Peripheral Interface — Device-Generic Command Set for Magnetic and Optical Disk

ANSI X3.147<sup>1</sup>, Information Systems — Intelligent Peripheral Interface — Device-Generic Command Set for Magnetic Tapes

**2.2 Other Standards.** This standard is also intended to be used in conjunction with EIA Standard for Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems, EIA RS-485-1983.

## 3. Definitions

**bidirectional.** This term refers to the use of signal lines that may be asserted by either the master or a slave, but not concurrently.

**bus acknowledge.** In the optional configuration, where the master permits the slave to define the type of Information Transfer to be executed, Bus Acknowledge is the BUS B equivalent of Bus Control.

<sup>1</sup> These standards are currently under development. Contact the Secretariat for the most recent information on the status and availability of these standards.

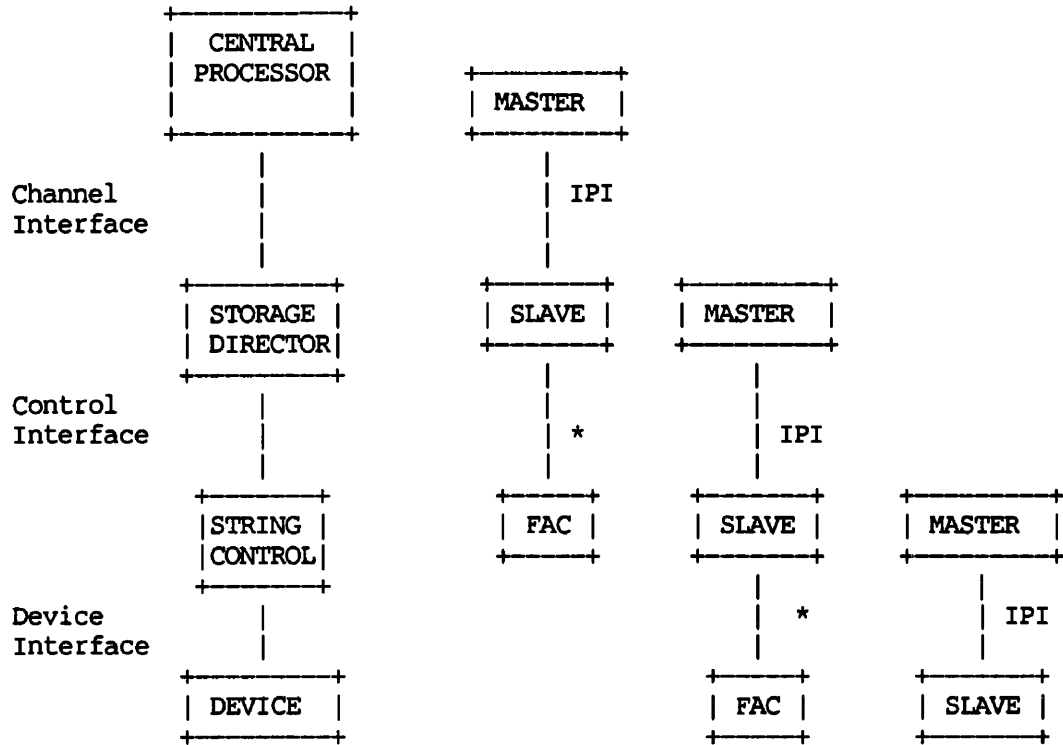
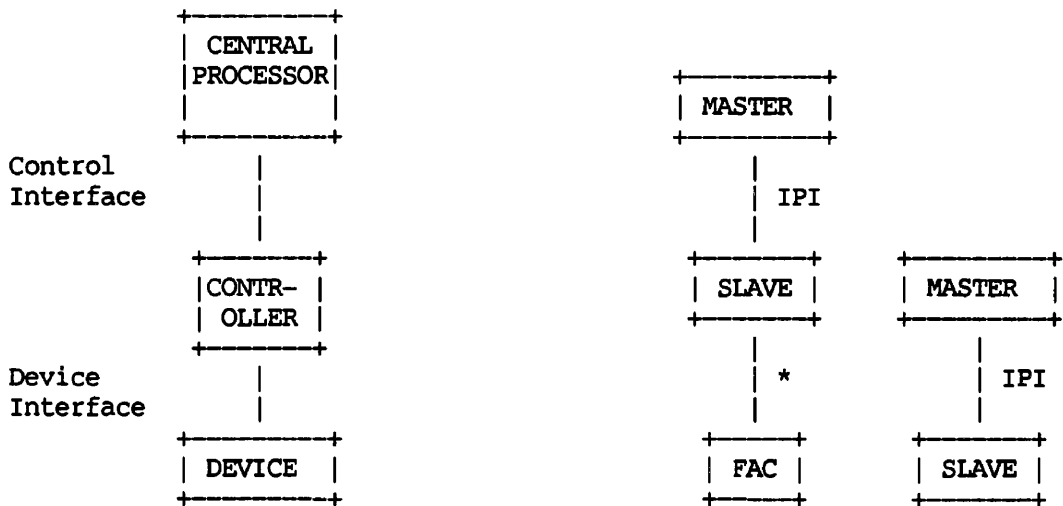


FIGURE 1

MAINFRAME CONFIGURATION EXAMPLE



\* This interface may or may not be IPI, but if it is, then the master/slave relationship is valid at that tier.

FIGURE 2

MINICOMPUTER CONFIGURATION EXAMPLE

**TABLE 1**  
**SIGNAL NOMENCLATURE**

TYPE OF DRIVER	VOLTAGE LEVEL	INTERFACE			
		SIGNAL CONDITION	LOGICAL TRANSITION	LOGICAL CONDITION	
THREE STATE	LOW	ACTIVE	ASSERT	1	ONE
	HIGH	INACTIVE	NEGATE	0	ZERO
	RELEASED	INACTIVE	DEGATE	0	ZERO
DIFFERENTIAL (Odd pin relative to Even pin)	HIGH	ACTIVE	ASSERT	1	ONE
	LOW	INACTIVE	NEGATE	0	ZERO
	RELEASED	INACTIVE	DEGATE	0	ZERO
OPEN EMITTER	HIGH	ACTIVE	ASSERT	1	ONE
	LOW	INACTIVE	NEGATE	0	ZERO
	RELEASED	INACTIVE	DEGATE	0	ZERO

NOTE: GATE is the action of ASSERTing or NEGATEing

**bus control.** This term refers to the Physical Interface Bus Control octet asserted on BUS A by the master during the Bus Control sequence. It is used to define the bus configuration for the subsequent Information Transfer.

**bus exchange.** This term refers to the Bus Control sequence (initiated by the master) and the Ending Status sequence (initiated by the slave), that are used to frame an Information Transfer (which may or may not have occurred). For every Bus Control sequence, there shall be an Ending Status sequence.

**busy.** This term describes a slave that is currently unable to process Bus Exchanges or Information Transfers.

**data.** This term refers to information transferred over the Physical Interface, other than that defined as Operation Commands and Operation Responses by the Logical Interface.

**data streaming.** This term refers to the transfer of information in a noninterlocked manner in order to achieve faster transfer rates.

**dominant slave.** This term describes a slave capable of assuming the role of the master for slave — slave Information Transfers.

**double octet mode (DOM).** This term refers to a mode of Information Transfer that uses BUS A and BUS B in parallel in a bidirectional manner to transfer 16 bits concurrently.

**ending status.** This term refers to the Physical Interface status octets presented by the master (optional) and the slave (mandatory) immediately following an Information Transfer.

**facility.** This term refers to the entity addressable by the master through the slave.

**information transfer.** This term refers to interchanges on the interface associated with the Logical Interface (i.e., Operation Commands, Operation Responses, and Data).

**interlocked.** This term refers to the handshake between master and slave of signals on the interface.

**level 0.** This term refers to the electrical and

mechanical characteristics of the Physical Interface.

**level 1.** This term refers to the bus states, sequences, and other rules (excepting electrical and mechanical characteristics of Level 0) that govern the use of the Physical Interface.

**logical interface.** This term refers collectively to all protocols higher than the Physical Interface specified in this standard.

**maintenance mode.** This term refers to the capability for a master to initiate analysis of the interface and restore operation after a failure condition.

**mandatory.** The functions labeled *mandatory* shall be included in all masters and slaves. They shall be implemented as defined in this standard.

**master.** This term refers to the entity in control of the interface.

**master status.** In the optional configuration, where the master permits the slave to define the type of Information Transfer to be executed, Master Status is the BUS A equivalent of Slave Status.

**operation command.** This term refers to a command issued by the master to initiate some specific operation that is outside the Physical Interface and is associated with a Logical Interface function.

**operation response.** This term refers to the response of a slave to an Operation Command. It is associated with the Logical Interface.

**optional.** This term describes features that are not required by the standard. However, if any feature defined by the standard is implemented, it shall be done as defined by the standard.

**physical interface.** This term denotes the mechanical, electrical, and interface protocols specified in this standard. In use, this term is the opposite of Logical Interface.

**sequence.** This term refers to a series of states that follow each other in a definite order to accomplish a function.



**single octet mode (SOM).** This term refers to a mode of Information Transfer that uses BUS A in a unidirectional manner to transfer 8 bits of information from master to slave, and BUS B in a unidirectional manner to transfer 8 bits of information from slave to master.

**slave.** This term refers to the addressable entity under control of, and directly connected to, the master.

**slave status.** This is the status asserted on BUS B by the slave at the completion of an Information Transfer (which may or may not have occurred).

**state.** This term is used to define the immediate condition of the interface, excluding transitions, as indicated by the control signals.

**unidirectional.** This term refers to the use of signal lines that are not asserted by both the master and slave (either concurrently or successively).

**vendor unique.** This term defines those features that can be defined as required by a vendor in a specific implementation. Caution should be exercised in defining and using such features since they are not necessarily standard between vendors.

## 4. Physical Characteristics

This interface specification defines the configuration classes that cover all of the cable types and line driver/receiver types permitted by the proposed standard. The classes are defined in response to perceived market requirements for the wide range of applications within which this interface is expected to be used. The protocol and timing differences between classes are expected to be either absent or so small as to permit inexpensive, simple interconnection of different classes within a single system environment.

Table 2 represents the mechanical and electrical characteristics of all of the configuration alternatives, which are chosen by an implementor on the basis of required performance, cost considerations, or both. The connectors for each type of cable are specified

in 4.2 for both shielded and unshielded applications.

**4.1 Configuration.** A maximum of eight slaves shall be connected to the master. Typically, this would be by a daisy-chain signal cable configuration, but radial connection is permitted. Some precautions shall be taken to properly handle interface features, such as dominant slaves, if radial connections are used.

**4.1.1 Alternatives.** The configurations permitted by this standard are intended to permit selection of the most cost-effective alternative for different market environments.

### 4.1.2 Intermix of Configurations

#### 4.1.2.1 Same Driver/Receiver Types.

The interconnection of different cable types using the same driver type is permitted within the restrictions of Table 6, provided that suitable techniques are used to maintain signal quality.

#### 4.1.2.2 Different Driver/Receiver Types.

The interconnection of configurations using different driver types requires that the master either be capable of operating with both, or there be an adapter that will exchange the signal types at the respective interfaces. The adapter, if any, is not defined in this standard.

**4.1.3 Extension of Distance Limitations.** The use of repeaters/converters is not defined in this standard.

**4.2 Connector Specification.** Three connector types shall be used with this interface. They are as follows:

- (1) A 2 · 25 pin header, plug-receptacle
- (2) A 50-pin connector
- (3) A 48-pin connector

**4.2.1 2 · 25 Pin Header, Plug-Receptacle.** A 2 · 25 pin header assembly shall be used. See Figures 3 and 4 for the connector physical specifications. See Table 3 for the pin assignments and signal nomenclature.

**4.2.2 50-Pin Shielded Bulkhead Connector.** A three-row 50-pin shielded bulkhead subminiature "D" connector shall be used. See Figures 5 through 7 for the connector physical specifications. Refer to Table 3 for the pin assignments and signal nomenclature.

NOTE: Cables with 50-pin connectors allow cables to be joined if a slave has to be removed from the interface for any reason (this is the rationale for requiring alternating retention hardware on opposite ends of the cable). However, it should be recognized that such abutments need to be limited in number so as to minimize signal degradation.

**4.2.3 48-Pin Shielded Bulkhead Connector.** A 48-pin shielded bulkhead coaxial connector shall be used. See Figures 8 through 10 for the connector physical specifications. See Table 4 for the pin assignments and signal nomenclature.

**4.2.4 Connector Shells.** The shells of the shielded connectors shall be plated with conductive material to ensure the integrity of the cable shield to chassis current path. The resistance of the cable shield to equipment chassis shall not exceed 5 milliohms, after a minimum of 500 cycles of mating and unmating.

**4.2.5 Terminators.** The terminators shall fit within the same dimensions as the cable end connectors, and shall be secured by the same retention method as are the cable connectors.

**4.3 Cable Characteristics**

**4.3.1 50-Conductor, 28-AWG Flat Cable.** The cable shall consist of 50 conductors of 28 AWG capable of mass termination to all standard 50 mil insulation displacement connectors (IDC). The following electrical characteristics apply to the individual wires within the flat cable assembly:

Characteristic impedance:	100 ohms ± 10%
Signal attenuation:	0.029 db max/ft at 5 MHz
Propagation delay:	1.4 ns/ft ± 10%
dc Resistance:	70 ohm max/1000 ft at 20°C

**4.3.2 50-Conductor, 28-AWG, Twisted-Pair Cable.** The cable shall consist of 25 twisted pairs of conductors of 28 AWG. The cable may have an overall shield, suitable for terminating in a metal-shielded connector (see 4.2.2). The overall shield serves the purpose of a signal shield. The two wires of a pair shall be connected to the same signal, one to the positive and the other to the negative signal pin. The following electrical characteristics apply to the twisted pairs within the bulk cable assembly:

Characteristic impedance:	105 ohms +6 ohms/−4 ohms 120 ohms ± 12 ohms (Voltage mode differential only)
Signal attenuation:	0.029 db max/ft at 5 MHz
Propagation delay:	1.7 ns/ft ± 10%
dc Resistance:	70 ohms max/1000 ft at 20°C

NOTE: See 4.3.3 for conductor-to-conductor capacitance, pair-to-shield delta capacitance, and pair-to-pair propagation delay delta.

**4.3.3 50-Conductor, 26-AWG, Twisted-Pair Cable.** The cable shall consist of 25 twisted pairs of conductors of 26 AWG. The cable may have an overall shield, suitable for terminating in a metal-shielded connector (see 4.2.2). The overall shield serves the purpose of a signal shield. The two wires of a pair shall be connected to the same signal, one to the positive and the other to the negative signal pin. The following electrical characteristics apply to the twisted pairs within the bulk cable assembly:

Characteristic impedance:	106 ohms ± 10 ohms 120 ohms ± 12 ohms (Voltage mode differential only)
Signal attenuation:	0.029 db max/ft at 5 MHz
Propagation delay:	1.65 ns/ft ± 10%
dc Resistance:	43 ohms max/ft at 20°C
Conductor-to-conductor capacitance:	17 pf/ft max
Pair-to-shield delta capacitance:	0.8 pf/ft max
Pair-to-pair propagation delay delta:	0.15 ns/ft max

**4.3.4 24-Conductor Coaxial Cable.** The cable shall be a special-purpose, twin, parallel electrical cable. Each of these twin cables shall consist of 12 coaxial cables of 26-AWG signal wire and an associated shield and an overall shield. The overall shield shall be suitable for terminating in a metal-shielded connector (see 4.2.3). The following electrical characteristics apply to individual coaxial cables:

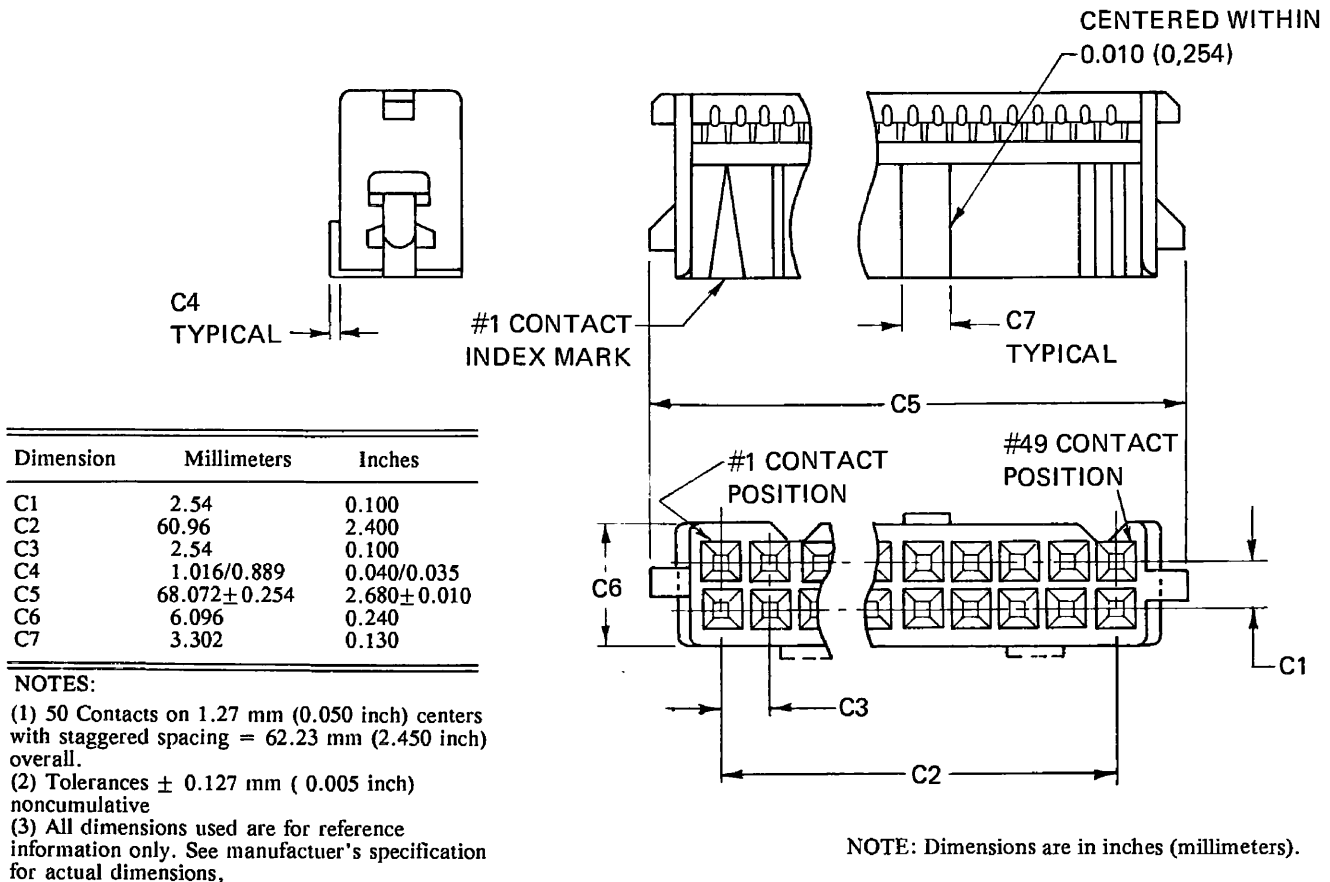
Characteristic impedance:	95 ohms +6 ohms / −4 ohms
Signal attenuation (Increase in rise time measured between the 20% and 80% points of the leading edge):	0.025 ns max/ft
Propagation delay (Measured at the 50% point of the leading edge):	1.22 < tPD < 1.27ns/ft
dc Resistance:	45 ohms max/1000 ft at 20°C

**TABLE 2**  
**MECHANICAL AND ELECTRICAL CHARACTERISTICS**

DRIVERS AND RECEIVERS	CABLE		MAX LENGTH	MIN CCD (PERIOD) *	MAX STREAMING TRANSFER RATE**	
	TYPE	ELECT CHAR			SOM	DOM
THREE-STATE DRIVERS and TTL RECEIVERS w/ HYSTERESIS	FLAT	4.4.1	5M	200ns	5MBs	10MBs
DIFFERENTIAL	TWISTED PAIR	4.4.2	50M			
		4.4.3	75M			
OPEN EMITTER	COAX CABLE	4.4.4	65M	290ns	3.3MBs	6.7MBs

\* See timing in Section 7 for a definition of CCD

\*\* Interlocked transfer rates may exceed these rates over short distances



**FIGURE 3**  
**2 x 25 PIN HEADER - PLUG**

**TABLE 3  
PIN ASSIGNMENTS FOR THREE STATE AND DIFFERENTIAL**

SIGNAL PIN	GROUND PIN	THREE STATE DRIVERS/RECEIVERS	SIGNAL PIN	GROUND PIN
SIGNAL PIN +	SIGNAL PIN -	DIFFERENTIAL DRIVERS/RECEIVERS	SIGNAL PIN +	SIGNAL PIN -
		SIGNAL NAME	SIGNAL SOURCE	
1	2	DC GROUND	1	34
9	10	ATTENTION IN	20	4
23	24	SYNC OUT	41	25
17	18	SLAVE IN	39	23
43	44	SYNC IN	15	48
35	36	MASTER OUT	45	29
29	30	SELECT OUT	43	27
45	46	BUS B - BIT 0	32	16
47	48	1	49	33
7	8	2	3	36
19	20	3	7	40
21	22	4	24	8
25	26	5	9	42
3	4	6	18	2
5	6	7	35	19
49	50	BUS B - PARITY	17	50
37	38	BUS A - BIT 0	13	46
39	40	1	30	14
15	16	2	22	6
27	28	3	26	10
31	32	4	11	44
33	34	5	28	12
11	12	6	37	21
13	14	7	5	38
41	42	BUS A - PARITY	47	31
+-----+			+-----+	
Header Pin Designation (See Figure 3)			IEC 48B Connector Pin Designation (See Figure 6)	

**NOTES:**

- (1) The outer shield of the 50-conductor shielded cable is used to tie to the frame via the connector.
- (2) When using the shielded bulkhead connector in a daisy-chain configuration, the master shall have a female panel connector per port, and each slave shall have both a female and a male panel connector per port. Line termination shall be provided at both ends of the cable.
- (3) Each cable shall be manufactured with a male cable connector on one end and a female connector on the other end.

TABLE 4

## PIN ASSIGNMENTS FOR OPEN EMITTER WITH 48 PIN COAXIAL CONNECTOR

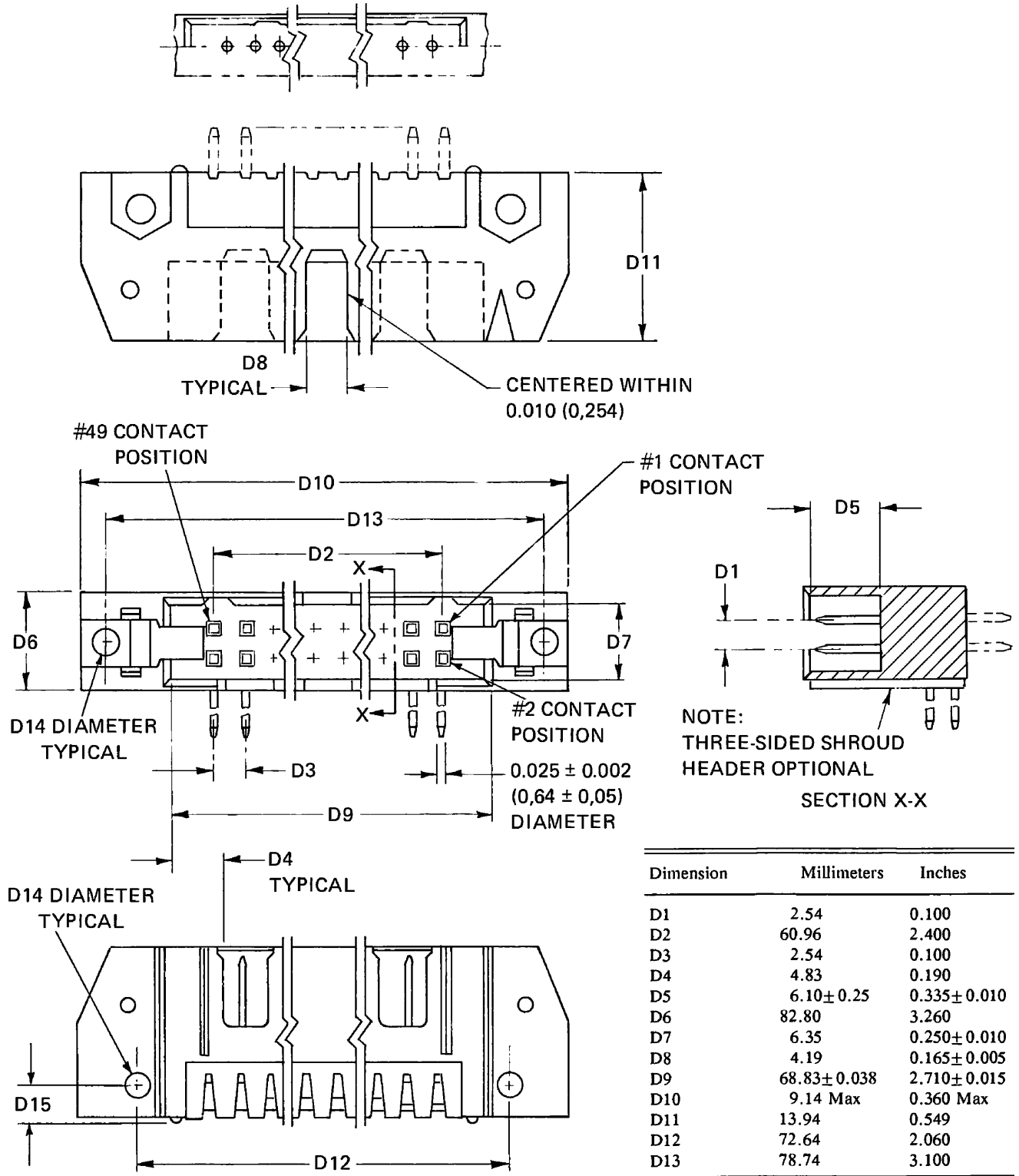
SIGNAL PIN	DRAIN WIRE	SIGNAL NAME	SIGNAL SOURCE
G06	G11	ATTENTION IN	SLAVE
D13	D12	SYNC OUT	MASTER
J02	J03	SLAVE IN	SLAVE
J13	J12	SYNC IN	SLAVE
B06	B11	MASTER OUT	MASTER
D02	D03	SELECT OUT	MASTER
J04	J05	BUS B BIT 0	SLAVE(MASTER)
G05	G04	1	
J06	J07	2	
G08	G07	3	
J09	J08	4	
G10	G09	5	
J11	J10	6	
G12	G13	7	
G03	G02	BUS B PARITY	SLAVE(MASTER)
D04	D05	BUS A BIT 0	MASTER(SLAVE)
B05	B04	1	
D06	D07	2	
B08	B07	3	
D09	D08	4	
B10	B09	5	
D11	D10	6	
B12	B13	7	
B03	B02	BUS A PARITY	MASTER(SLAVE)

## NOTES:

(1) The outer shield of the cable specified is used to tie to frame via the connector, and so provide the equivalent of the shield signal specified in Table 3.

(2) When used in a daisy-chain configuration, each slave shall have panel connectors for a signal-In cable and a signal-Out cable per port. Each extreme end shall have line termination at the panel connectors. A master that has only a signal-Out connector shall have internal provision for line termination.

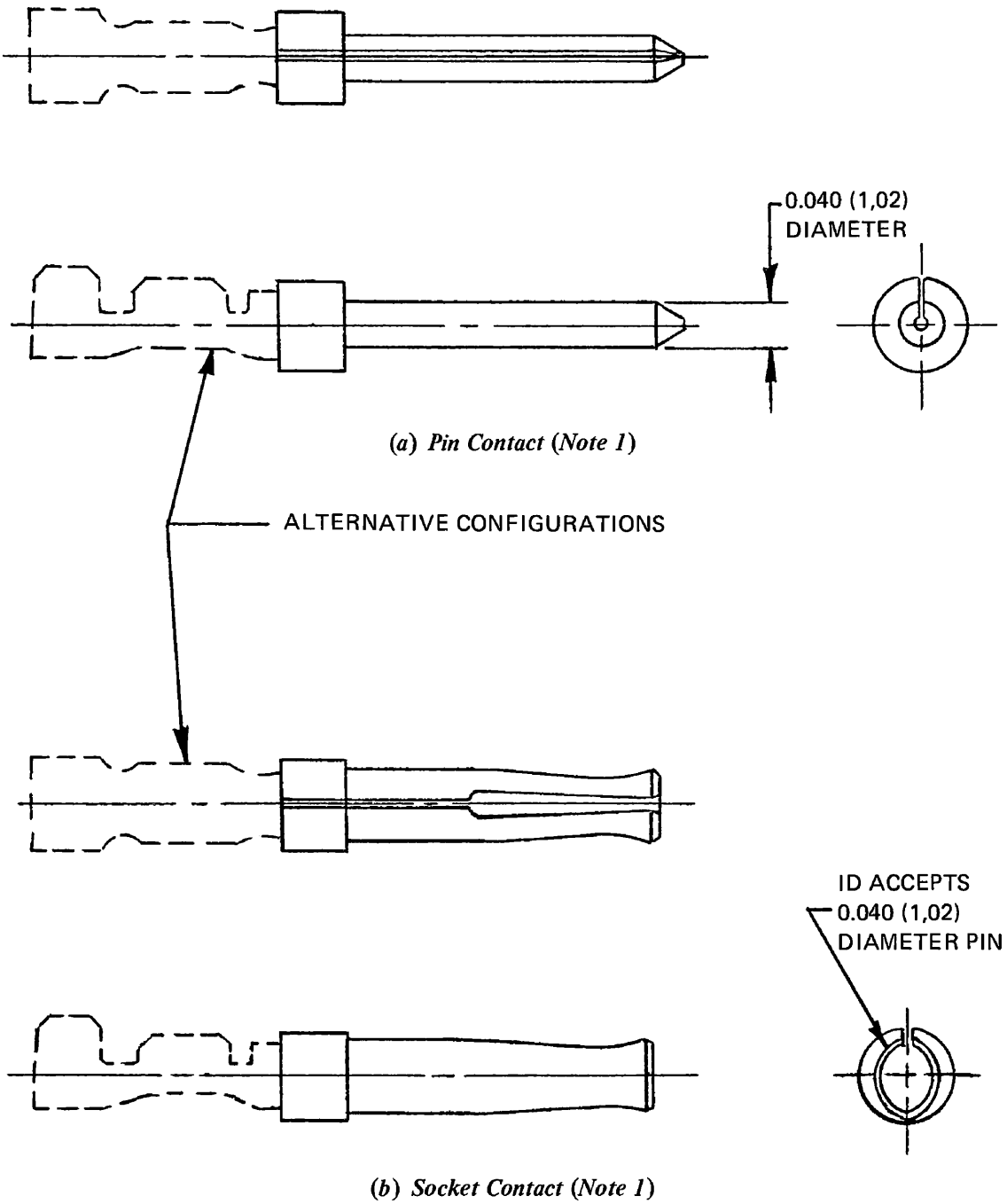
(3) The connectors are hermaphroditic. The signal-In cable connector and the signal-Out panel (bulkhead) connector shall be light-colored. The signal-Out cable connector and the signal-In panel connector shall be dark-colored. Each cable shall be manufactured with a light-colored signal-In cable connector on one end and a dark-colored signal-Out cable connector on the other. Proper mating, including cable to cable shall be light to dark.



NOTE: Dimensions are in inches (millimeters).

NOTES:  
 (1) 50 Contacts on 2.54 mm (0.100 inch) centers with staggered spacing = 60.96 mm (2.40 inch) overall.  
 (2) Tolerances ± 0.127 mm ( 0.005 inch) noncumulative  
 (3) All dimensions used are for reference information only. See manufacturer's specification for actual dimensions.

**FIGURE 4**  
**2 x 25 PIN HEADER – RECEPTACLE**

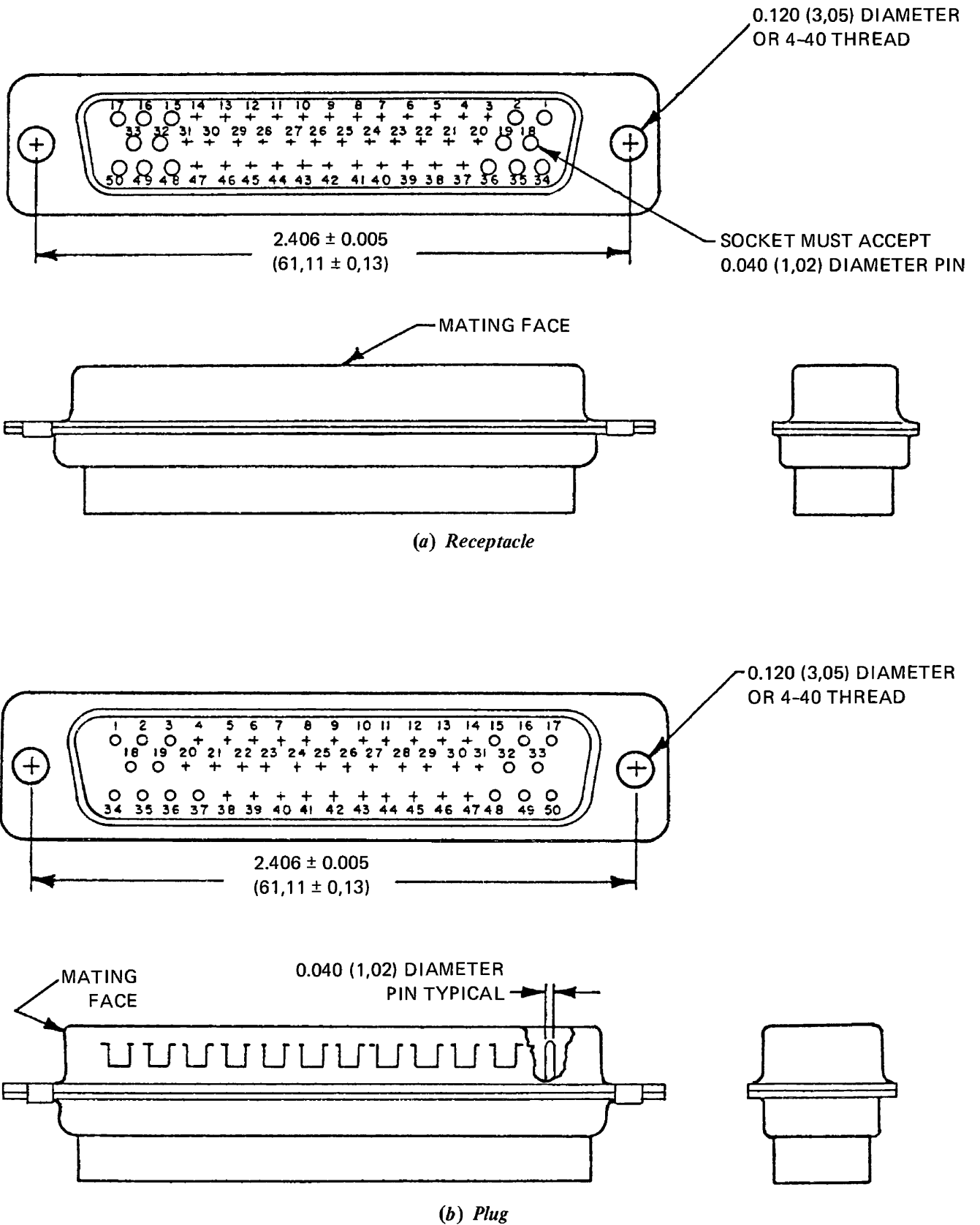


NOTES:

- (1) Contact pictorials for reference only.
- (2) Dimensions are in inches (millimeters).

FIGURE 5

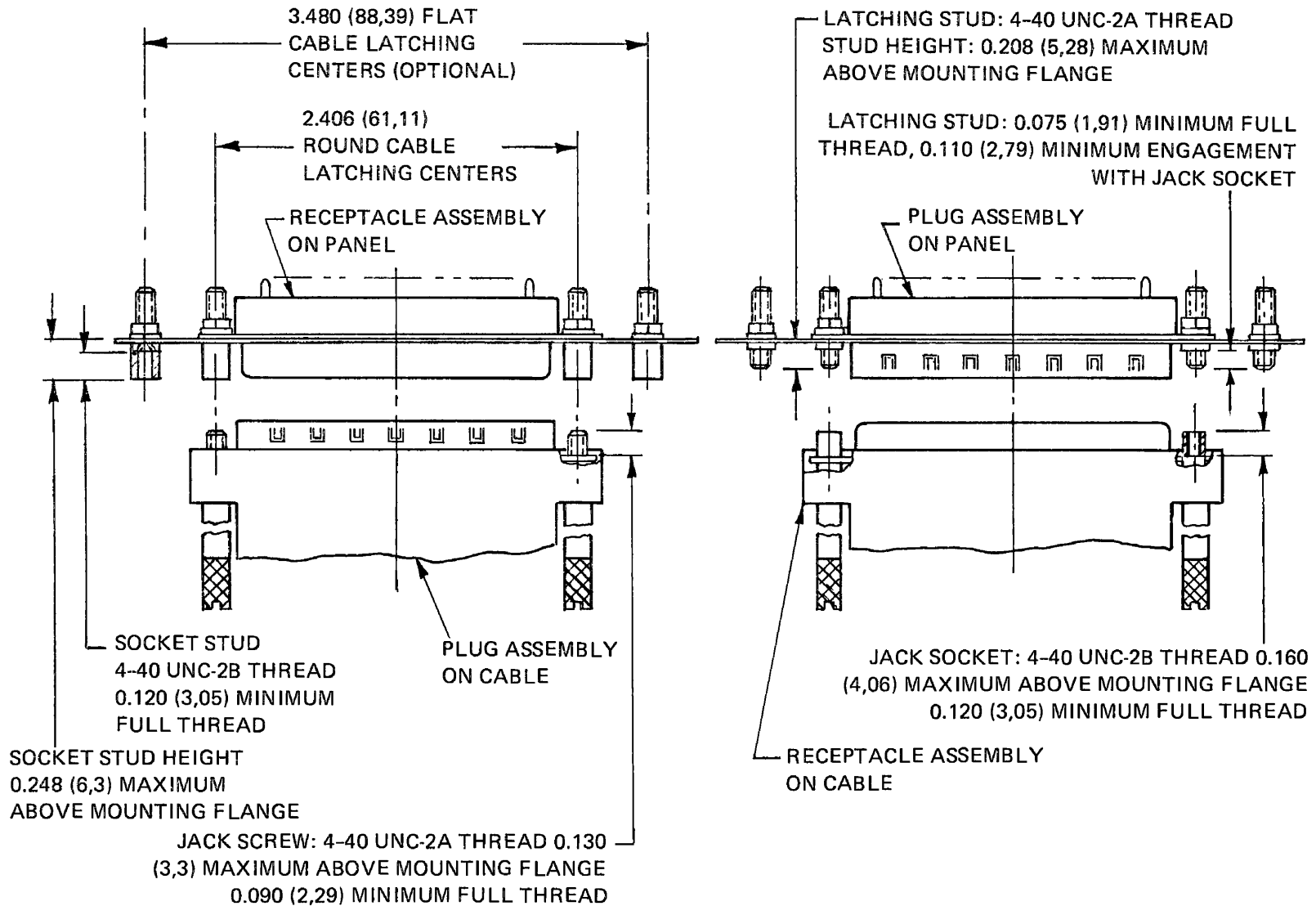
50-POSITION SUBMINIATURE "D" PIN/SOCKET CONTACT



NOTE: Dimensions are in inches (millimeters).

FIGURE 6  
50-POSITION SUBMINIATURE "D" RECEPTACLE/PLUG

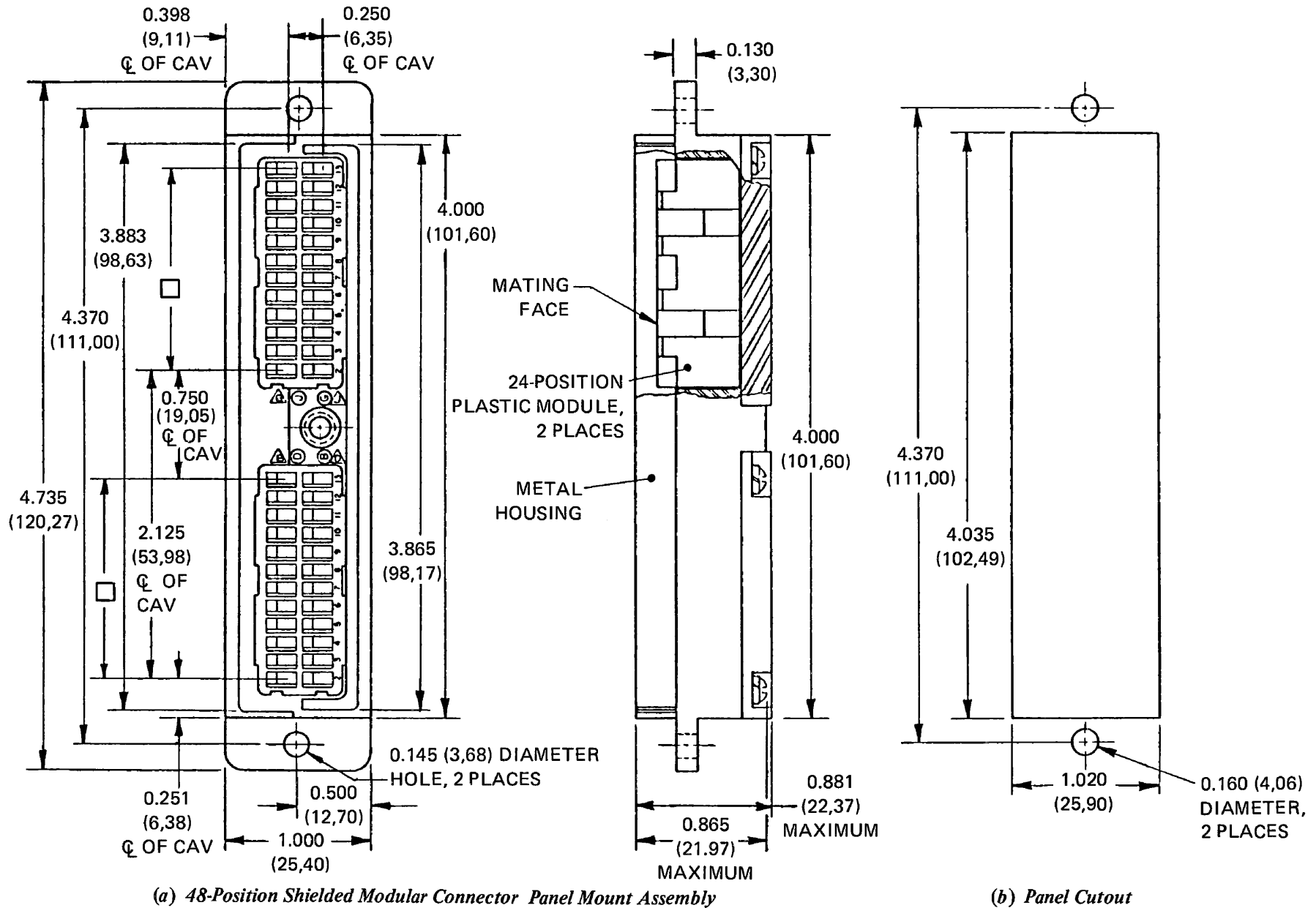




NOTES:

- (1) Recommended mounting clearance shall be in accordance with EIA 449-1983.
- (2) Receptacle assembly should have a conductive metal front shell.
- (3) Plug assembly should have a conductive metal front shell with grounding indents.
- (4) Cable end assembly should have a shielded strain relief system.
- (5) Connector assembly, on the panel side, can be rear or front mounted. Rear mounting shown for illustration only. Dimensions apply to rear or front mounting.
- (6) Dimensions are in inches (millimeters).

FIGURE 7 50-POSITION SUBMINIATURE "D" CONNECTOR



- NOTES: (1)  $\circ$  denotes pin assignments for signal-in (dark) panel-mounted connector.  
 (2)  $\triangle$  denotes pin assignments for signal-out (light) panel-mounted connector.  
 (3)  $\square$  = 11 equal spaces at 0.125–1.375 (3.18–34.93).  
 (4) All dimensions are in inches (millimeters). CAV = cavity.

FIGURE 8 48-POSITION SHIELDED MODULAR CONNECTOR - PANEL MOUNT



**4.4 Electrical Characteristics.** Bidirectional line transceivers are permitted on all signals; but when lines are used unidirectionally, transceivers shall be wired as unidirectional.

Upon completion of a Power On Reset, Slaves shall enable all drivers.

NOTE: If Slave-to-Slave Information Transfers are supported, MASTER OUT and SYNC OUT shall be bidirectional (see 5.4.9).

In all electrical configurations, the receiver as well as the driver shall tolerate, without damage, the situation in which up to nine drivers are active simultaneously in the same direction as well as the situation in which a line is shorted to dc ground. In the case of the ATTENTION IN signal, it is possible that up to eight slaves may be simultaneously signaling an Attention condition. The receiver output shall remain at logical active when any combination of the eight slaves is signaling attention. The ATTENTION IN signal shall not be driven to inactive.

See Figure 11 for the configuration of bidirectional signal lines. See Figures 12 and 13 for the configuration of the unidirectional signal lines.

#### **4.4.1 Three State Logic Drivers and Receivers with Hysteresis**

**4.4.1.1 Line Transceivers.** The maximum Low-level output voltage shall be 0.5 volts. The minimum High-level output voltage shall be 2.4 volts. At the Low-level output voltage, the driver shall be capable of sinking 48 milliamperes, minimum. At the High-level output voltage, the driver shall be capable of sourcing 15 milliamperes, minimum. The maximum three-state output current with the line at the Low-level voltage shall be  $-1$  milliamperes. Line drivers shall not be driven during power sequencing.

The maximum Low-level input voltage shall be 0.8 volts. The minimum High-level input voltage shall be 2.0 volts. At Low level, the input current shall be  $-1$  milliamperes maximum. At High level, the input current shall be 80 microamperes, maximum. The hysteresis at the receiver inputs shall be 0.2 volts, minimum.

**4.4.1.2 Line Drivers.** The maximum Low-level output voltage shall be 0.5 volts. The minimum High-level output voltage shall be 2.4 volts. At the Low-level output voltage, the driver shall be capable of sinking 48 milliamperes, minimum. At the High-level output voltage, the driver shall be capable of sourcing 15 milliamperes, minimum. The maximum three-state output current

with the line at the Low-level voltage shall be  $-400$  microamperes. Line drivers shall not be driven during power sequencing.

**4.4.1.3 Line Receivers.** The maximum Low-level input voltage shall be 0.8 volts. The minimum High-level input voltage shall be 2.0 volts. At Low level, the input current shall be  $-600$  microamperes, maximum. At High level, the input current shall be 80 microamperes, maximum. The hysteresis at the receiver inputs shall be 0.2 volts, minimum.

**4.4.1.4 Bus Terminators.** Each signal line shall be terminated at both ends of the cable by installing a 220-ohm resistor  $\pm 2\%$  from signal to  $+ 5$  volts and a 330-ohm resistor  $\pm 2\%$  from signal to ground.

**4.4.1.5 Stubs.** A maximum stub length of 7 centimeters is allowed off of the mainline within any connected equipment. The mainline is defined as the continuous path between the terminators at each extreme end of the interface. The stub signals on the Printed Circuit Board shall maintain a characteristic impedance of 100-ohms  $\pm 20\%$ .

**4.4.1.6 ATTENTION IN Signal.** The ATTENTION IN signal shall not be driven to inactive.

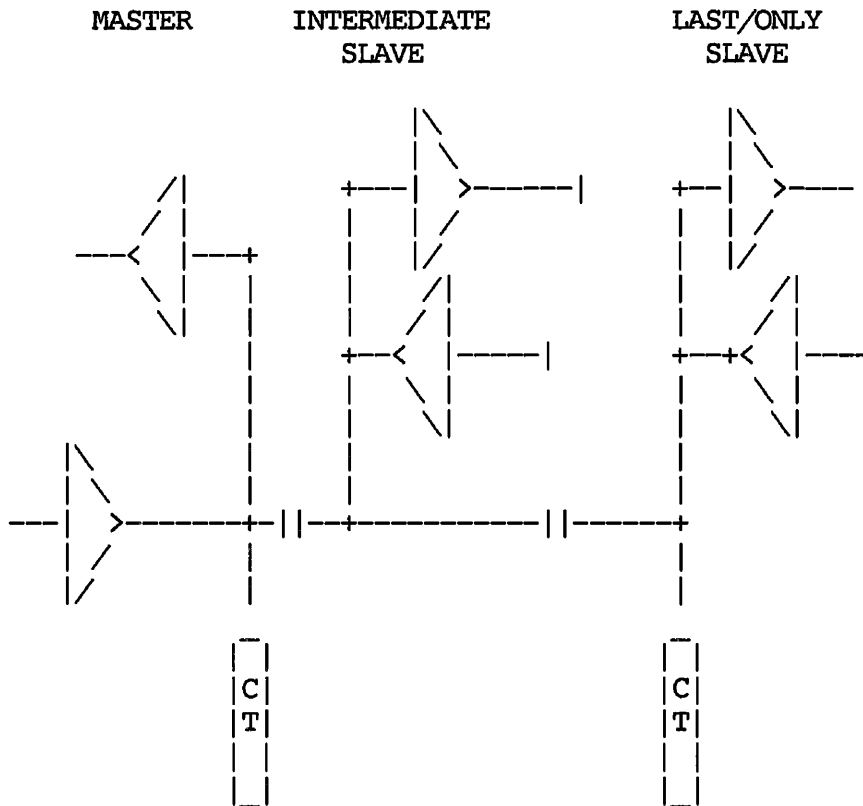
**4.4.2 Voltage Mode Differential Drivers/Receivers.** This class can support data transmission rates up to 10 Mbytes/s at up to 50 meters. The total length of all cable segments between master and slaves, all effective cable segments within the connected master and slaves, and all stubs shall be less than or equal to 50 meters.

The twisted pair leads always attach to an adjacent pair of connector pins as noted in Table 3.

**4.4.2.1 Line Drivers.** The differential driver shall meet the requirements of EIA RS-485-1983, which specifies the electrical characteristics of generators (drivers) and receivers for use in a balanced digital multipoint system.

**4.4.2.2 Line Receivers.** The differential receiver shall meet the requirements of EIA RS-485-1983, which specifies the electrical characteristics of generators (drivers) and receivers for use in a balanced digital multipoint system.

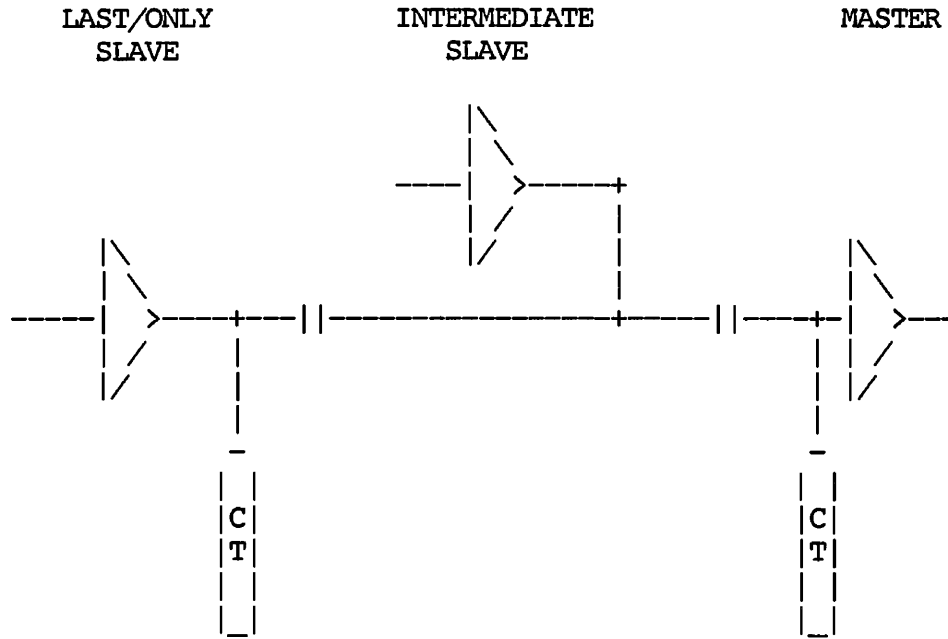
If the (+) signal lead is positive with respect to the (−) signal lead, the receiver output shall be logically active. The receiver output shall be inactive if the input differential signal is reversed.



Note: Terminator CT shall be at extreme ends of the cable.

FIGURE 11

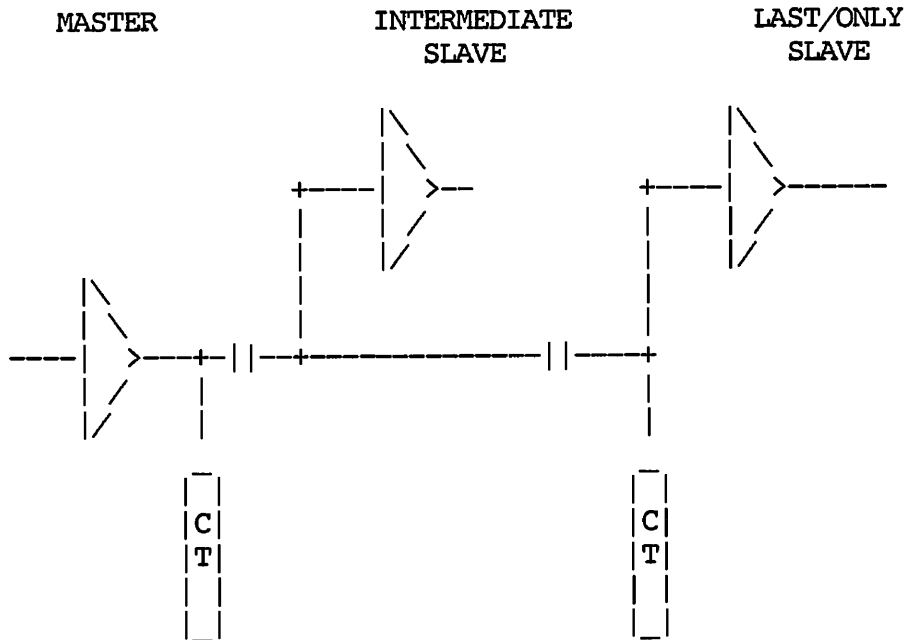
CONFIGURATION FOR BIDIRECTIONAL BUS SIGNALS



Note: Terminator CT shall be at extreme ends of the cable.

FIGURE 12

CONFIGURATION FOR UNIDIRECTIONAL SINGLE-ENDED LINES FROM SLAVE



Note: Terminator CT shall be at extreme ends of the cable.

FIGURE 13

CONFIGURATION FOR UNIDIRECTIONAL SINGLE-ENDED LINES FROM MASTER

**4.4.2.3 Line Terminators.** Each signal line pair shall be terminated at both ends of the cable by installing a 150-ohm ( $\pm 2\%$ ) resistor from signal pin (+) to signal pin (−).

**4.4.2.4 Stubs.** A maximum stub length of 60 centimeters is allowed off of the mainline within any connected equipment. The mainline is defined as the continuous path between the terminators at each extreme end of the interface.

**4.4.2.5 Line Bias.** Each signal line pair shall be biased so as to establish a minimum 250-millivolt quiescent differential voltage. This is done in order to enforce an inactive state (zero) when the signal pair is released. The biasing network shall be of sufficiently high impedance to minimize disturbance of signal transmission.

**4.4.2.6 Signal Level.** The minimum signal available to any master or slave differential receiver attached to the cabling system shall be at least 400 millivolts.

**4.4.2.7 ATTENTION IN Signal.** The ATTENTION IN signal shall not be driven to inactive.

**4.4.3 Current Mode Differential Drivers/Receivers.** The driver approximates a constant current source. The current is steered to the leads of the twisted-pair transmission line by the appropriate logic levels at the input terminals. The output current can be switched off (released) for multidriver operation. The driver can either be a single current source that is steered into one or the other of the twisted-pair leads or a dual current source to ensure nearly equal and opposite currents in the twisted-pair leads. Either type can be intermixed on the interface, provided that they individually meet the criteria outlined in this standard.

The twisted-pair leads always attach to adjacent connector pins (as noted in Table 3).

**4.4.3.1 Line Drivers.** When all other drivers are inhibited, a driver's constant current source shall be capable of developing a differential signal across the twisted-pair leads of between 125 millivolts and 1.1 volts at a receiver that is separated from the driver by the maximum allowable cable resistance. The differential signal value should apply with the duty cycle between 30 percent and 60 percent at 5 megahertz and with the lines properly terminated. If the data input becomes inactive, the output signal is reversed resulting in a minimum of −125 millivolts as measured from the

(+) signal relative to the (−) signal twisted-pair lead. When the driver is inhibited, the current source is disconnected from the outputs so that the output current and voltage will allow the receiver to detect signals from the other drivers on the line. The common mode range of the driver shall be at least +3 volts or at least −3 volts.

**4.4.3.2 Line Receivers.** The two receiver are connected to the twisted-pair (+) and (−) signal leads; so that the receiver may sense signals on the interface line pair. The receiver sensitivity shall be such that the receiver output is stable with a differential signal of 25 millivolts or more. Common mode range of the receiver shall be at least +3 volts or at least −3 volts.

If the (+) signal lead is positive with respect to the (−) signal lead, the receiver output shall be logically active. The receiver output shall be inactive if the input differential signal is reversed.

**4.4.3.3 Line Termination.** Each twisted-pair conductor line is terminated to DC ground at both extreme ends of the twisted-pair transmission line with a 51-ohm ( $\pm 2\%$ ) resistor. The lines are biased at the master to ensure that the case in which the lines are undriven can be reliably interpreted and also to prevent receiver oscillation.

If the drivers used require two voltage supplies, the biasing network shall consist of a resistor from the (−) signal lead to a positive supply and a resistor from the (+) signal lead to a negative supply. If a single voltage supply driver is used, a single resistor will suffice. If the resistors are used, the resistor values shall be small enough to place the (−) signal a minimum of 60 millivolts above DC ground and the (+) signal at least 60 millivolts below ground. If a single resistor is used its value shall ensure that the (+) signal is a minimum of 120 millivolts more negative than the (−) signal with all drivers inhibited.

NOTE: Since the biasing subtracts from the operating noise margins, the resistor values shall also be large enough so that the normal operating differential signal does not fall below the 125-millivolt minimum specified in 4.4.3.1. This range shall be ensured regardless of where on the cable the measurement is taken, including the extreme end, which is separated from the biasing network by the maximum cable resistance. The values apply after the lines fully stabilize.

**4.4.3.4 Stub/Interconnect Lengths.** A maximum stub length of 12 centimeters is allowed

off of the mainline within any connected equipment. The mainline is defined as the continuous path between the terminators at each extreme end of the interface.

A maximum etched mainline interconnect length of 12 centimeters is allowed at any one place within any connected equipment. The etched interconnects and stubs are controlled so that the two conductors associated with a twisted pair are routed together. The interconnect and stubs shall maintain an effective resistance of no greater than the 28 AWG wire specified in 4.3.2. It is recommended that etched interconnects be avoided whenever possible, especially at intermediate points on the interface where the cable goes through a slave. Etched interconnects add significantly to differential noise as well as increasing the exposure to losing the entire interface whenever a connector fault occurs within a slave.

**4.4.3.5 ATTENTION IN Signal.** The ATTENTION IN signal shall not be driven to inactive.

#### **4.4.4 Open Emitter Drivers/Receivers**

**4.4.4.1 Line Drivers.** The maximum Low-level output voltage shall be 0.15 volts. The minimum High-level output voltage shall be 2.4 volts. At High level, the driver output shall source 100 milliamperes, minimum. Line driver outputs shall be Low or released during power sequencing, except for ATTENTION IN, which shall be released.

**4.4.4.2 Line Receivers.** The maximum Low-level input voltage shall be 0.7 volts. The minimum High-level input voltage shall be 1.7 volts. At Low level, the input current shall be  $-400$  microamperes, maximum. At High level (5.0 volts), the input current shall be 420 microamperes, maximum.

**4.4.4.3 Line Termination.** Each signal shall be terminated by installing a 95-ohm ( $\pm 2\%$ ) resistor from signal to ground at the extreme ends of the cable.

**4.4.4.4 Stub Lengths.** A signal In bulkhead connector shall be used with an interconnection to a signal Out bulkhead connector. A maximum stub length of 15 centimeters is allowed off of the mainline within any connected equipment. The mainline is defined as the continuous path between the terminators at each extreme end of the interface. The interconnection shall maintain an effective 26 AWG with an impedance of 95 ohms,  $+6$  ohms,  $-4$  ohms.

**4.4.4.5 Intermixed Cable Configurations.** It is allowable to intermix twisted-pair cables and coaxial cables in the same daisy chain. Twisted pair may be used internal to a slave to complete the signal path between the signal In connector and the signal Out connector. The internal length of this path shall be kept to a minimum and shall be included in the calculation of maximum cable length.

**4.4.4.6 ATTENTION IN Signal.** The ATTENTION IN signal shall not be driven to inactive.

#### **4.5 Cable Interconnections**

**4.5.1 Stub Lengths.** Table 5 represents the valid stub lengths for electrical and cable combinations.

**4.5.2 Maximum Cable Lengths and Allowable Cable/Driver Combinations.** The maximum cable lengths with the various cabling/driver configuration choices are shown in Table 6.

**4.5.3 Cable and Connector Configurations.** The cable and connector combinations permitted by the standard are described in Table 7.

**4.5.4 Configurations.** Figures 11 through 13 illustrate cabling alternatives for configurations that have a master at one end of the cable, a slave at the other, with intermediate slaves. Other electrically valid configurations may be used, even if they are not shown in the figures.



TABLE 5

## STUB LENGTHS (Centimeters) FOR ELECTRICAL/CABLE COMBINATIONS

	4.3.1 FLAT CABLE	4.3.2 28 AWG TWISTED PR CABLE	4.3.3 26 AWG TWISTED PR CABLE	4.3.4 COAXIAL CABLE
4.4.1 Three State	7	N/A	N/A	N/A
4.4.2 Differential (Voltage Mode Class)	N/A	60	60	N/A
4.4.3 Differential (Current Mode Class)	N/A	12	12	N/A
4.4.4 Open Emitter	N/A	N/A	15	15

**TABLE 6**  
**MAXIMUM CABLE LENGTHS (Meters) FOR VARIOUS DRIVER OPTIONS**

	4.3.1	4.3.2	4.3.3	4.3.4
	FLAT CABLE	28 AWG TWISTED PR CABLE	26 AWG TWISTED PR CABLE	COAXIAL CABLE
4.4.1 Three State	5	N/A	N/A	N/A
4.4.2 Differential (Voltage Mode Class)	N/A	50	50 less length of 4.3.2	N/A
4.4.3 Differential (Current Mode Class)	N/A	50	75 less 1.5*(length of 4.3.2)	N/A
4.4.4 Open Emitter	N/A	N/A	65	125 less 2*(length of 4.3.3)

NOTE: The values shown in this table represent the maximum accumulated length that is valid with a particular electrical class. An implementation may permit two cable types to coexist, for example, an internal cable that interconnects multiple devices within a cabinet and an external cable that exits the cabinet. The formula shown is used to calculate the total for one type, less the actual sum of the lengths in the other type referenced, for example, the maximum length for an installation of Open Emitter and Coaxial Cable is 125 meters, less twice the actual length of the twisted-pair cable internal to the cabinet.

**TABLE 7**  
**CABLE AND CONNECTOR COMBINATIONS**

	4.3.1	4.3.2	4.3.3	4.3.4
	FLAT CABLE	28-AWG TWISTED PR CABLE	26-AWG TWISTED PR CABLE	COAXIAL CABLE
4.4.1 50 Pin Header	X	X	X	N/A
4.4.2 50 Pin Shielded Bulkhead Connector	N/A	X	X	N/A
4.4.3 48 Pin Shielded Bulkhead Connector	N/A	N/A	N/A	X

## 5. Protocol

This section provides signal definitions, state, sequence, octet, and Maintenance Mode descriptions. The terms "In" and "Out" are always used in reference to the master. Relative signal timing and tolerance is defined in Section 7.

### 5.1 Interface Description

**5.1.1 Bus Usage.** The following apply to the use of BUS A and BUS B

(1) The uses of BUS A and BUS B are structured to optimize operations between Bus Exchanges and Information Transfers.

(2) The Bus Control sequence is initiated by the master and is associated with control of the Physical Interface. The Ending Status sequence is initiated by the slave and is associated with reporting the status of the Bus Exchange or the preceding Information Transfer.

(3) During Bus Exchanges BUS A is unidirectional Out from the master for Bus Control and Master Status (optional), and BUS B is unidirectional In to the master for Bus Acknowledge (optional) and Slave Status.

(4) Information Transfer is the term used to indicate the various types of information (Data, Operation Command, or Operation Response) that are transparently transferred across the Physical Interface.

(5) Bus Exchanges are defined as framing (bracketing) Information Transfers. The differentiation between Bus Exchanges and Information Transfers allows a simple state machine to control Bus Exchanges; for example, the timing-independent Bus Exchanges can be interpreted by a general-purpose microprocessor.

(6) Only one control signal shall change at a time between master and slave. An In control signal change shall be interleaved with an Out control signal change such that the source of control signal changes is alternated between them, thus effectively interlocking all control functions. Optional Data Streaming transfers are not required to comply with this requirement.

(7) Operation Commands are issued by the master and are associated with operation of the Logical Interface. Operation Responses are returned by the slave. Both occur as Information Transfers.

(8) During Information Transfers there can be two modes:

(a) In Single Octet Mode, Information Transfers are 8-bit unidirectional modes (that is, BUS A Out, BUS B In).

(b) In Double Octet Mode, BUS A and BUS B are used to transfer 16 bits in parallel either In or Out as required.

(9) If unused bits are listed as Reserved, they shall be set to zero. The sender is responsible for ensuring zeros. The receiver may choose whether or not to verify that the zeros are present.

(10) If unused bits are listed as undefined then there is no requirement for either sender or receiver to care about content. Octet parity shall still be maintained.

(11) In states in which the bus contents are bit-significant addresses, octet parity need not be correct.

(12) Parity shall be generated by the originator and checked by the receiver, except where noted.

**5.1.2 Maintenance Mode.** Maintenance Mode provides a communication path for error recovery and fault isolation when a failure exists in the interface or within an attached slave.

Utilizing the Master Reset sequence, the master forces the interface into a mode (see 5.6) that allows various levels of communication and control while normal functional usage of the interface is blocked.

Normal interface function is blocked as a result of failure modes such as:

(1) An interface line being open  
 (2) An interface line being stuck-on (for example, a slave's driver continually asserting SYNC IN)

(3) An attached slave malfunctioning in a manner that results in improper and irrational interface usage (for example, a microprocessor in a slave not recognizing or responding correctly to master sequences)

Such failure modes prevent the master/slave communication necessary to collect fault isolation information, to implement real-time error recovery procedures, or to do both.

The Maintenance Mode permits using the interface for some basic functions during most failure modes that have been predicted (except for those that block the master from asserting SYNC OUT and negating SELECT OUT and MASTER OUT in order to enter the MAINT state).

**5.2 Usage of Signals.** The interface signals are summarized in Figure 14.

**5.2.1 BUS A.** BUS A consists of nine lines (bits 7 — 0 plus parity). Bit 7 is the most significant bit (MSB). Parity is odd.

BUS A is used by the master for all control sequences. For Information Transfers in Single-Octet Mode, all information is passed from the master to the slave on BUS A.

In Double-Octet Mode, information is passed from the master to the slave or from the slave to the master on BUS A. BUS A is considered to be the first octet in a double octet of information. BUS A shall be released by all slaves when SELECT OUT is negated.

**5.2.2 BUS B.** BUS B consists of nine lines (bits 7 — 0 plus parity). Bit 7 is the most significant bit. Parity is odd.

BUS B is used by the slave for all control sequences. For Information Transfers in Single-Octet Mode, all information is passed from the slave to the master on BUS B.

In Double-Octet Mode, information is passed from the slave to the master or from the master to the slave on BUS B. BUS B is the other octet in a double octet of information.

**5.2.3 SELECT OUT.** SELECT OUT is sent from the master to the slaves to select a slave and maintain selection. When SELECT OUT is inactive, all slaves shall release BUS A. Dominant slaves shall release MASTER OUT and SYNC OUT drivers upon sensing the negation of SELECT OUT by the master.

**5.2.4 SLAVE IN.** SLAVE IN is used by the slave to either indicate acknowledgment of master-initiated control sequences or to terminate Information Transfers.

**5.2.5 MASTER OUT.** MASTER OUT is used by the master to initiate or terminate Information Transfers, Request Interrupts, Request Transfer Mode, or Reset slaves.

**5.2.6 SYNC IN.** When SYNC IN is asserted during transfers In, information is valid on the bus or buses. When SYNC IN is asserted during transfers Out, the slave is ready to accept information.

NOTE: To deskew, the information In is asserted on the bus or buses a minimum time before SYNC IN is asserted (see Section 7). SYNC IN is asserted to acknowledge the Bus Control octet during the Bus Control sequence.

**5.2.7 SYNC OUT.** When SYNC OUT is asserted transfers In, the information has been accepted by the master. When SYNC OUT is asserted during transfers Out, the information is valid on the bus or buses.

NOTE: To deskew, the information Out is asserted on the bus or buses a minimum time before SYNC OUT is asserted (see Section 7). SYNC OUT is asserted to initiate the Bus Control sequence.

During reset, SYNC OUT is asserted without response for a minimum time (see Figures 48 and 49.)

**5.2.8 ATTENTION IN.** ATTENTION IN is a wired-OR signal for all slaves to inform the master that service is requested. The master has the responsibility to service the interrupts (or class of interrupts) as required.

NOTE: This signal does not contribute to determining the state of the interface. It can be asserted by any slave until a selection of that slave is acknowledged, at which time the selected slave shall release this line. The slave can again assert ATTENTION IN after entering the IDLE state. Nonselected slaves can continue to assert ATTENTION IN.

This line shall not be driven inactive.

**5.3 States.** The states of the interface are defined by the condition of the control signals: SELECT OUT, SLAVE IN, MASTER OUT, SYNC OUT, and SYNC IN. With the exception of Data Streaming transfers (optional), these signals are interlocked between the master and the slave. (See Figures 14 and 15 and Tables 8 and 9).

NOTE: ATTENTION IN is not considered a control signal.

**5.3.1 IDLE.** When all the control signals are inactive, the interface is in the IDLE state. Abnormal entries to this state shall occur whenever the master and slaves recognize an undefined state or state transition. The buses are released prior to entering the IDLE state except during the Request Interrupts and Master Reset sequences.

**5.3.2 MAINT (Maintenance Mode).** The master shall negate MASTER OUT, SYNC OUT, and then SELECT OUT. Then the master shall release BUS B, negate BUS A, and then assert SYNC OUT to enter the MAINT state.

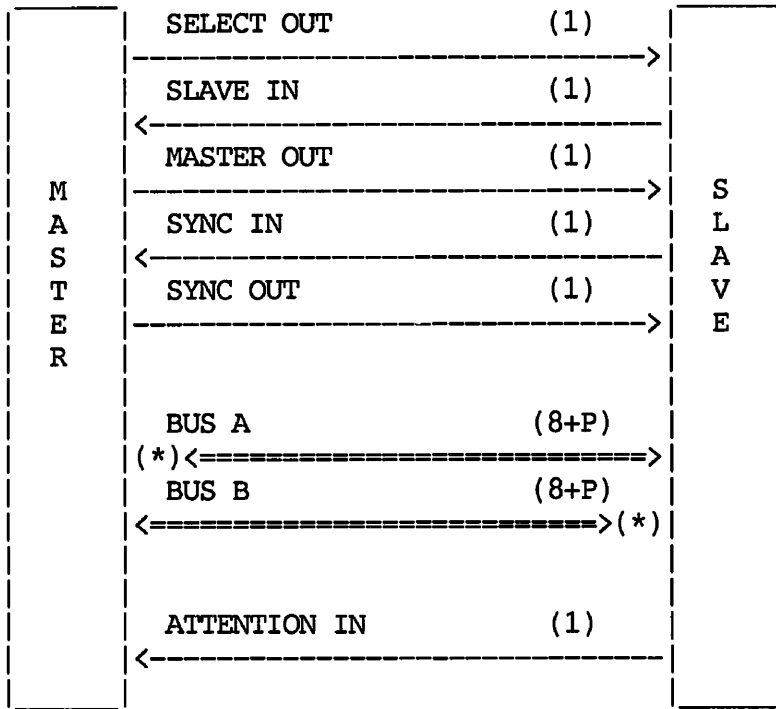
This state initiates Maintenance Mode on all slaves.

**5.3.3 REQUEST.** While in IDLE, the master shall set the Request Modifier octet on BUS A, then assert MASTER OUT to enter the REQUEST state.

This state causes the slaves to respond with either the Address octet or the Transfer Settings octet, or to initiate Selective Reset (see 5.3.4).

**5.3.4 RESETSEL1 (Selective Reset 1).** While in REQUEST, the master shall assert SYNC OUT to enter the RESETSEL1 state.

This state initiates a reset of the slave identified by the Selective Reset Control octet on BUS A and terminates MAINT.



\* Bi-directional in Double Octet Mode (optional)

FIGURE 14

INTERFACE SIGNAL SUMMARY

**5.3.5 REQUACK (Request Acknowledge).** While in REQUEST, the slave shall set the requested response on BUS B, then assert SLAVE IN to enter the REQUACK state.

**5.3.6 RESETSEL2 (Selective Reset 2).** The slave entered REQUACK state in response to REQUEST. While in REQUACK, the master shall assert SYNC OUT to enter the RESETSEL2 state. The slave shall release or negate all interface lines upon recognition of this state, which then causes an entry to RESETSEL1.

**5.3.7 DESEL (Deselect).** While in REQUACK, the master shall negate MASTER OUT to enter the DESEL state.

While in SLAVACK (see 5.3.9), the master shall negate SELECT OUT to enter the DESEL state.

This state initiates the deselection of the slave by the master.

**5.3.8 SELECT.** While in IDLE, the master shall set the Selection octet on BUS A, then assert SELECT OUT to enter the SELECT state.

This state initiates the Selection Sequence.

While in SLAVEND (see 5.3.17), the master shall set the Master Status octet on BUS A and negate MASTER OUT to enter the SELECT state.

NOTE: In the SELECT state, it is necessary to know the previous transition in order to respond correctly. When entered from IDLE, it is a true Selection (and the slave responds with Select Status on BUS B). When entered from SLAVEND, SELECT is an intermediate state following an Information Transfer between the master and the selected slave.

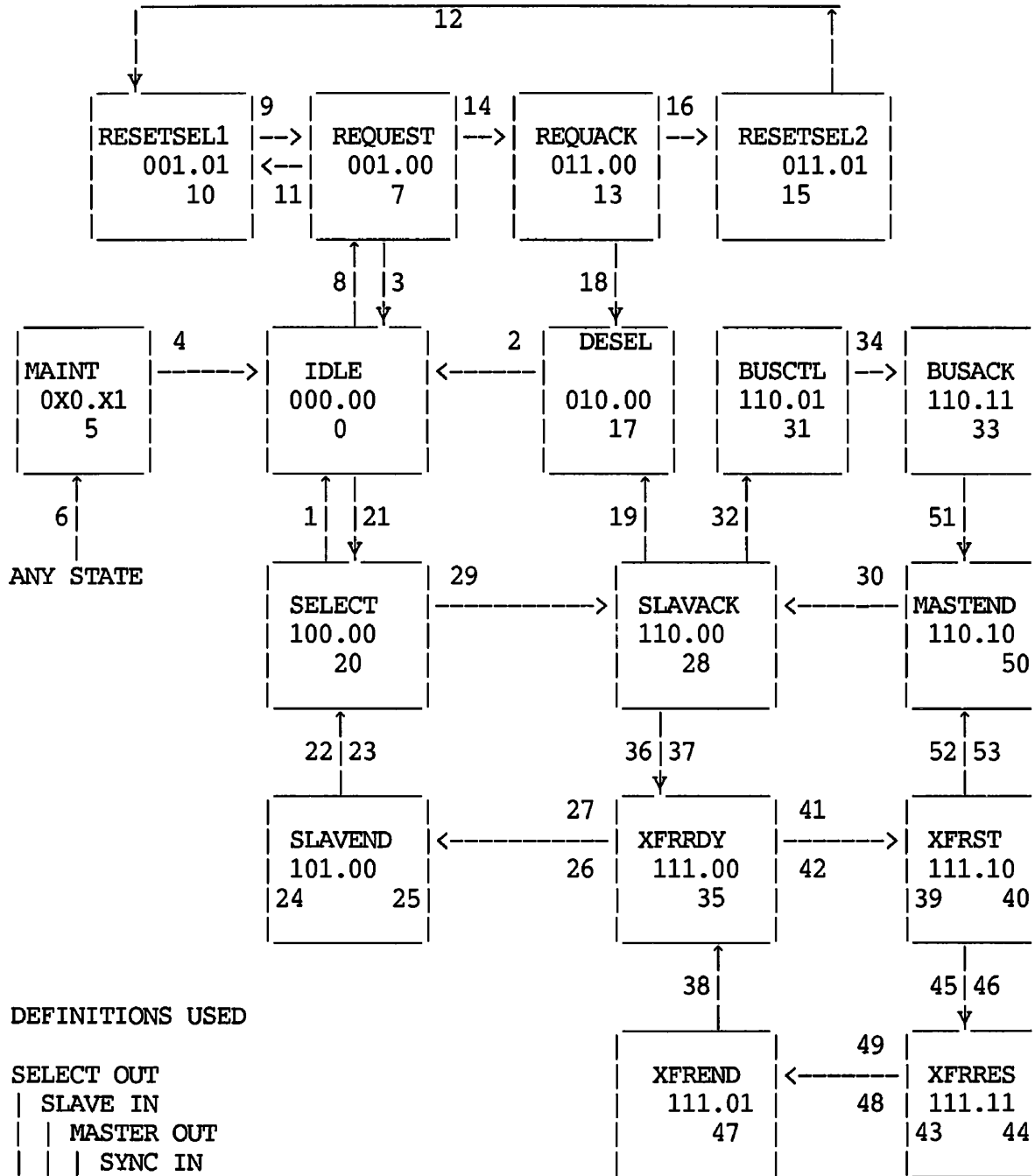
**5.3.9 SLAVACK (Slave Acknowledge).** While in SELECT following IDLE, the addressed slave shall set its Select Status on BUS B, then assert SLAVE IN to enter the SLAVACK state.

While in SELECT following SLAVEND, the selected slave shall set the Slave Status octet on BUS B, then assert SLAVE IN to enter the SLAVACK state.

While in MASTEND (see 5.3.12), the selected slave shall negate SYNC IN to enter the SLAVACK state. BUS B is not valid during this transition.

This state acknowledges either selection, the end of a Bus Control sequence, or the end of an Information Transfer.

NOTE: In the SLAVACK state, it is necessary to know the previous transition because BUS B contains different contents depending upon the state from which SLAVACK was entered.



NOTES:

- (1) This figure represents all of the defined states and possible paths between them. Not all sequences are necessarily valid. The valid sequences are described in 5.4.
- (2) The numbers are shown as cross reference to Table 9, which defines the contents of the buses during all valid states.

FIGURE 15

BUS STATE DIAGRAM



**TABLE 9**  
**STATES AND TRANSITIONS**

#	FROM STATE	TO STATE	XFR	BUS A	BUS B	ASSERT/NEGATE
0	IDLE	IDLE		RELEASED /MASTER REL	RELEASED /SLAVE REL	
1	SELECT	IDLE		SELECT OCT	RELEASED	
2	DESEL	IDLE		RELEASED	RELEASED	SLAVE IN
3	REQUEST	IDLE		REQ/SEL/SET	ADDRESS	MASTER OUT
4	MAINT	IDLE		RELEASED	RELEASED	SYNC OUT
5	MAINT	MAINT		RELEASED	SLAVE REL	
6	ANY STATE	MAINT		RELEASED	*	SYNC OUT SELECT OUT MASTER OUT
7	REQUEST	REQUEST		REQ/SEL/SET	ADDRESS/*	
8	IDLE	REQUEST		REQ/SEL/SET	RELEASED	MASTER OUT
9	RESETSEL1	REQUEST		SEL RESET	*	SYNC OUT
10	RESETSEL1	RESETSEL1		SEL RESET	*	
11	REQUEST	RESETSEL1		SEL RESET	*	SYNC OUT
12	RESETSEL2	RESETSEL1		SEL RESET	*	SLAVE IN
13	REQUACK	REQUACK		REQ/SEL/SET	ADDRESS /XFR SET	
14	REQUEST	REQUACK		REQ/SEL/SET	ADDRESS /XFR SET	SLAVE IN
15	RESETSEL2	RESETSEL2		SEL RESET	*	
16	REQUACK	RESETSEL2		SEL RESET	ADDRESS /XFR SET	SYNC OUT



**TABLE 9**  
**STATES AND TRANSITIONS (CONTINUED)**

#	FROM STATE	TO STATE	XFR	BUS A	BUS B	ASSERT/NEGATE
17	DESEL	DESEL		MASTER REL	SLAVE REL	
18	REQUACK	DESEL		REQ/SEL/SET	ADDRESS /XFR SET	MASTER OUT
19	SLAVACK	DESEL		*	SAME PREC	SELECT OUT
20	SELECT	SELECT		SAME PREC	*	
21	IDLE	SELECT		SELECT OCT	RELEASED	SELECT OUT
22	SLAVEND	SELECT	IN	MSTR STATUS	*	MASTER OUT
23	SLAVEND	SELECT	OUT	MSTR STATUS	MASTER REL DOM	MASTER OUT
24	SLAVEND	SLAVEND	IN	RELEASED DOM	*	
25	SLAVEND	SLAVEND	OUT	*	*	
26	XFRRDY	SLAVEND	IN	SLAVE REL DOM	*	SLAVE IN
27	XFRRDY	SLAVEND	OUT	*	*	SLAVE IN
28	SLAVACK	SLAVACK		SAME PREC/*	SAME PREC	
29	SELECT	SLAVACK		SAME PREC	SELECT STAT /SLAVE STAT	SLAVE IN
30	MASTEND	SLAVACK		*	SLAVE REL DOM /*	SYNC IN
31	BUSCTL	BUSCTL		BUS CTL	*	
32	SLAVACK	BUSCTL		BUS CTL	SAME PREC	SYNC OUT
33	BUSACK	BUSACK		*	BUS ACK	
34	BUSCTL	BUSACK		BUS CTL	BUS ACK	SYNC IN

TABLE 9

STATES AND TRANSITIONS (CONTINUED)

#	FROM STATE	TO STATE	XFR	BUS A	BUS B	ASSERT/NEGATE
35	XFRRDY	XFRRDY		*	*	
36	SLAVACK	XFRRDY	IN	MASTER REL DOM /*	*	MASTER OUT
37	SLAVACK	XFRRDY	OUT	*	*	MASTER OUT
38	XFREND	XFRRDY		*	*	SYNC OUT
39	XFRST	XFRST	IN	IN DOM	IN SOM	
40	XFRST	XFRST	OUT	*	*	
41	XFRRDY	XFRST	IN	IN DOM	IN SOM	SYNC IN
42	XFRRDY	XFRST	OUT	*	*	SYNC IN
43	XFRRES	XFRRES	IN	*	*	
44	XFRRES	XFRRES	OUT	OUT SOM	OUT DOM	
45	XFRST	XFRRES	IN	IN DOM	IN SOM	SYNC OUT
46	XFRST	XFRRES	OUT	OUT SOM	OUT DOM	SYNC OUT
47	XFREND	XFREND		*	*	
48	XFRRES	XFREND	IN	*	*	SYNC IN
49	XFRRES	XFREND	OUT	OUT SOM	OUT DOM	SYNC IN
50	MASTEND	MASTEND		*	*	
51	BUSACK	MASTEND		*	BUS ACK	SYNC OUT
52	XFRST	MASTEND	IN	IN DOM	IN SOM	MASTER OUT
53	XFRST	MASTEND	OUT	*	*	MASTER OUT

Note: In SOM configurations it is not necessary for the master or selected slave to release the buses.

**5.3.10 BUSCTL (Bus Control).** While in SLAVACK, the master shall set the Bus Control octet on BUS A, then assert SYNC OUT to enter the BUSCTL state.

This state initiates control of the subsequent Information Transfer.

**5.3.11 BUSACK (Bus Acknowledge).** While in BUSCTL, the slave shall set the Bus Acknowledge octet on BUS B, then assert SYNC IN to enter the BUSACK state.

This state is complementary to BUSCTL to acknowledge that the Bus Control octet has been accepted.

**5.3.12 MASTEND (Master End).** While in BUSACK, the master shall negate SYNC OUT to enter the MASTEND state.

While in XFRST (see 5.3.14), the master shall negate MASTER OUT to enter the MASTEND state.

This state either acknowledges that the Bus Acknowledge octet has been accepted, or it initiates termination of an Information Transfer by the master.

**5.3.13 XFRRDY (Ready to Transfer).** While in SLAVACK, the master shall assert MASTER OUT to enter XFRRDY state.

When beginning transfers In, the assertion of MASTER OUT shall indicate to a slave operating in Double-Octet Mode that the master has released BUS A.

When beginning transfers Out, the assertion of MASTER OUT shall direct a slave operating in Double-Octet Mode to release BUS B.

While in XFREND (see 5.3.16), the master shall negate SYNC OUT to enter the XFRRDY state.

This state is initiated by the master to transfer each octet (or double octet) of an Information Transfer.

**5.3.14 XFRST (Start to Transfer).** While in XFRRDY for transfers In, the slave shall set information on the buses, then assert SYNC IN to enter the XFRST state.

While in XFRRDY for Transfers Out, the slave shall assert SYNC IN to enter the XFRST state. The master shall maintain control of the buses.

This state is initiated by the slave to acknowledge the start of Information Transfer. For transfers Out, it shall indicate that the slave is ready to accept information, and for transfers In, it shall be used to validate that the buses have stable information.

**5.3.15 XFRRES (Respond to Transfer).** While in XFRST for transfers Out, the master shall set information on the buses, then assert SYNC OUT to enter the XFRRES state.

While in XFRST for transfers In, the master shall accept information on the buses, then assert SYNC OUT to enter the XFRRES state. The slave shall maintain control of the buses.

This state is initiated by the master to acknowledge the acceptance of information on the buses for transfers In, or to validate that the buses have stable information on transfers Out.

**5.3.16 XFREND (End of Transfer).** While in XFRRES the slave shall negate SYNC IN to enter the XFREND state. For transfers Out, the master shall maintain control of the buses. For transfers In, the slave shall maintain control of the buses.

This state is initiated by the slave to acknowledge the acceptance of information on transfers Out, and to complete the transferring of each octet (or double octet) of an Information Transfer.

**5.3.17 SLAVEND (Slave End).** While in XFRRDY the slave shall negate SLAVE IN to enter the SLAVEND state. When in Double-Octet Mode for transfers Out, the master shall release control of BUS B; for transfers In during Double-Octet Mode, this state acknowledges the release of BUS A by the slave.

This state is initiated by the slave to terminate an Information Transfer.

**5.3.18 State Summary.** The states are summarized in Table 8 and are schematically shown in Figure 15.

Table 9 defines BUS A and BUS B for every valid state transition for both input and output. It also notes the interface signals.

The determination of bus contents requires remembering the previous state transition in two states. The two states that have defined bus contents only when entered from a particular previous state are: (1) SLAVACK, when entered from SELECT or MASTEND, and (2) SELECT, when entered from IDLE or SLAVEND.

**5.3.19 Undefined State Recovery.** An undefined state or state transition induced by a slave shall cause the master to begin abnormal deselection by releasing the buses and negating all OUT signals. SELECT OUT shall be the last signal line negated, unless Slave-to-Slave Information Transfers are in progress (see 5.4.9.2). When the slave is deselected, it shall release the buses it may be driving, then negate SYNC IN and SLAVE IN. The interface is thus returned to the IDLE state, and the master can resume operations.

An undefined state or state transition induced

by a master shall cause the slave to release the buses it may be driving, then negate SYNC IN and SLAVE IN. When the master recognizes the negation of SLAVE IN outside of a valid sequence, it shall release the buses and negate all OUT signals. SELECT OUT shall be the last signal line negated. The interface is thus returned to the IDLE state, and the master can resume operations.

NOTE: The negation of SLAVE IN and SYNC IN is valid during defined sequences such as SLAVEND from XFRRDY. SLAVE IN and SYNC IN are not active during REQUEST, SELECT, and SLAVEND.

Since ATTENTION IN does not affect the state sequences, its use does not have to be specified here.

**5.3.20 Sequences without Information Transfer.**

There is no requirement that an Information Transfer has to occur between Bus Control and Slave Status. The following subsections refer to sequences in which an Information Transfer is expected to occur.

**5.3.20.1 SLAVEND without Information Transfer.** If a slave senses a parity error or illegal Bus Control octet on BUS A during a Bus Control Sequence, it shall terminate the sequence normally. When the master attempts the subsequent information transfer, the slave shall negate SLAVE IN upon sensing the assertion of MASTER OUT, and enter SLAVEND from XFRRDY.

Entering SLAVEND without an Information Transfer shall indicate to the master that the slave did not accept the Bus Control octet. The cause of the slave rejection of the Bus Control shall be reported to the master in the Slave Status Octet during the SLAVACK state. See Figure 50.

**5.3.20.2 MASTEND without Information Transfer.** During a slave-controlled Information Transfer (optional), if the master detects a parity error or an illegal Bus Acknowledge octet on BUS B during the Bus Control sequence, it shall terminate the sequence normally. The sequence shall proceed normally from BUSACK through MASTEND to SLAVACK. While in SLAVACK, the master can either assert SYNC OUT to enter BUSCTL and restart the Bus Control sequence, or negate SELECT OUT to enter DESEL and deselect the slave.

The deselection sequence, or the restarting of the Bus Control sequence shall indicate to the slave that the master did not accept the Bus Acknowledge octet.

**5.3.21 Slave Action on BUS A Parity Errors**

**5.3.21.1 Selection Octet.** If the slave detects a parity error on BUS A during SELECT, it shall not respond to the contents of the octet for selection purposes. If the master fails to receive a response from the addressed slave within a time-out period, it shall retry the SELECT sequence.

**5.3.21.2 Request Modifier Octet.** If the slave detects a parity error on BUS A during REQUEST, it shall not respond to the contents of the octet. If the master fails to receive a response from at least one slave within a time-out period, it shall retry the REQUEST sequence.

**5.3.21.3 Master Status Octet.** If the slave detects a parity error on BUS A during the SELECT state of the Ending Status sequence, it shall not interpret the contents of the octet. It shall assume the Information Transfer, if any, was unsuccessful and post accordingly in the Slave Status octet.

**5.3.21.4 Bus Control Octet.** If the slave detects a parity error on BUS A during BUSCTL, it shall not interpret the contents of the octet and shall post the parity error in the Slave Status octet.

**5.3.22 State and Transition Table.** Table 9 supplements the timing diagrams in Section 7. Its purpose is to provide a snapshot at two points in time, from the perspective of the initiator and the resposdee.

*Initiator.* The table identifies the responsibility of the initiator for bus contents at the time it changes a signal to begin transition to a new state.

*Resposdee.* The table identifies the bus contents at the time that the resposdee recognizes the state signaled by the initiator.

Wherever DOM is referenced, it identifies that there is a special requirement to release the bus other than that used in SOM and control functions. It is also implied in the table that the bus is undefined (\*) in SOM.

The following abbreviations are used in Table 9:

*	Bus Undefined — not necessarily released or
BUS ACK	Bus Acknowledge Octet
BUS CTL	Bus Control Octet
DOM	Double Octet Mode
MASTER REL	Master releases bus
MSTR STATUS	Master Status Octet

ADDRESS	Address Octet (bit significant)
SELECT STAT	Select Status Octet (bit significant)
REQ/SEL/SET	Request Modifier Octet or Selective Reset Control Octet or Request Transfer Settings Octet
SAME PREC	Same contents as in preceding transition
SELECT OCT	BUS A Selection Octet
SEL RESET	Selective Reset Control
SLAVE REL	Slave releases bus
SLAVE STAT	Slave Status Octet
SOM	Single Octet Mode
XFR	Transfer
XFR SET	Transfer Settings Octet

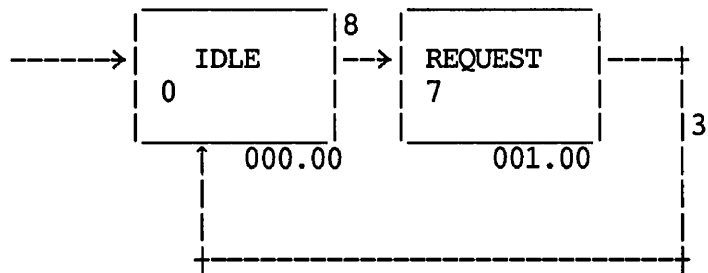


FIGURE 16

**REQUEST INTERRUPTS SEQUENCE**

**5.4 Sequences.** The Bus State diagram in Figure 15 summarizes the possible state transitions. The condition of the buses during all of the states and transitions is shown in Table 9. The numbers of the entries in Table 9 are shown on Figure 15, and those in the following subsections provide a cross-reference.

**5.4.1 Request Sequences**

**5.4.1.1 Request Interrupts Sequence.** This sequence (Figure 16) allows the master to interrogate the slaves to determine the service (or class of service) desired.

The master initiates the sequence by setting the Request Modifier on BUS A and asserting MASTER OUT. Slaves with interrupts meeting the required Request Modifier conditions (see 5.5.7.1) shall place their bit-significant address in the Address octet on BUS B. Appropriate latching may be required at the master because interrupts from the slaves can change dynamically. Parity on BUS B shall not be checked by the master. The master shall negate MASTER OUT to return to IDLE state.

NOTE: The response of the slaves is not synchronous, and the master must wait until the slowest, the furthest, or the slowest and furthest slave responds before latching or sampling BUS B. In addition, the master must wait until the slowest, the furthest, or the slowest and furthest slave detects the IDLE state and releases its bit-significant address on BUS B before starting another sequence.

See Figure 44 for timing details.

**5.4.1.2 Request Transfer Settings Sequence.**

This sequence (Figure 17) allows the master to interrogate the specified slave as to its Information Transfer characteristics.

The master initiates the sequence by placing the Request Transfer Settings octet on BUS A

(see 5.5.7.3) and asserting MASTER OUT. The addressed slave shall respond by setting the Transfer Settings Response octet on BUS B and asserting SLAVE IN. Then the master shall negate MASTER OUT to reach the Deselection State, and SLAVE IN is negated to return to IDLE State.

See Figure 45 for timing details.

**5.4.1.3 Request Facility Interrupts Sequence (Optional).**

This sequence allows the master to interrogate the facilities of the specified slave to determine the service (or class of service) desired. The sequence is the same as that for Request Transfer Settings. The contents of the Request Modifier octet affect the slave's octet response. The master initiates the sequence by placing the Request Facility Interrupts octet on BUS A (see 5.5.7.2) and asserting MASTER OUT. Facilities on the specified slave that have interrupts meeting the required Request Modifiers conditions set the Address octet on BUS B, and the slave shall assert SLAVE IN. Appropriate latching may be required at the master because interrupts from the facilities can change dynamically. Parity shall not be checked on BUS B by the master. The master shall then negate MASTER OUT to reach the DESEL state, and SLAVE IN is negated to return to IDLE state.

See Figure 45 for timing details.

**5.4.1.4 Request Slave Interrupts Sequence (Optional).**

This sequence allows the master to obtain status and interrupt information from a specified slave. The sequence is the same as that for Request Transfer Settings. The master initiates the sequence by placing the Request Slave Interrupts octet on BUS A (see 5.5.7.4) and asserting MASTER OUT. The specified slave sets the Slave Interrupts octet on Bus B asserts SLAVE IN. Appropriate latching may be required

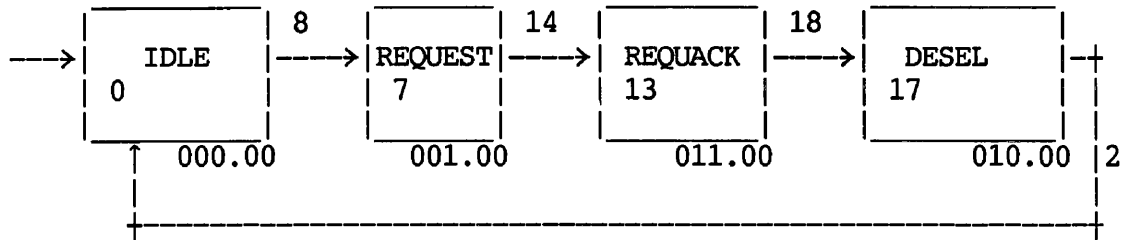


FIGURE 17  
REQUEST TRANSFER SETTINGS SEQUENCE

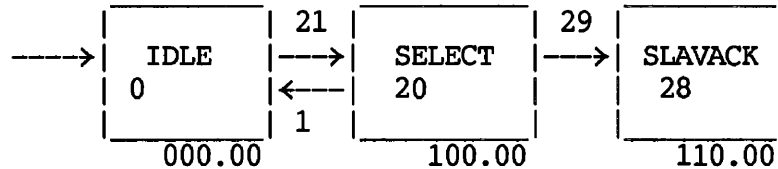


FIGURE 18  
SELECTION SEQUENCE

at the master because interrupts from the slaves can change dynamically. Parity shall not be checked on BUS B by the master. The master shall then negate MASTER OUT to reach the DESEL state, and SLAVE IN is negated to return to IDLE state.

See Figure 45 for timing details.

**5.4.2 Selection Sequence.** The Selection sequence (Figure 18) occurs when the master addresses a slave (or a slave and its facilities).

The master shall place the Selection octet containing the slave address, and optionally the facility address, on BUS A, then assert SELECT OUT to enter the SELECT state.

If the slave can process Bus Exchanges or Information Transfers, the slave shall place its (the slave's) bit-significant Select Status in the Address octet on BUS B and then assert SLAVE IN to enter the SLAVACK state.

If the slave cannot process Bus Exchanges or Information Transfers, but is otherwise functioning normally, the slave shall assert only SLAVE IN to report the Busy condition by entering the SLAVACK state. This Busy condition reflects only the current condition of the slave and does not necessarily reflect the current condition of the addressed facility when the facility address is optionally placed on BUS A.

When the Slave responds to the master as Busy

(i.e., no bit-significant address), the master shall return to IDLE via the DESEL state.

If there is a parity error on BUS A, none of the slaves are selected, and SLAVE IN is not asserted.

See Figure 46 for timing details.

**5.4.3 Normal Deselect Sequence.** Selection is maintained while SELECT OUT remains active. When SELECT OUT is negated, the addressee shall be deselected (see Figure 19).

See Figure 47 for timing details.

**5.4.4 Master Reset Sequence (Maintenance Mode).** The Master Reset sequence (Figure 20) allows the master to initiate Maintenance Mode.

The master initiates the sequence by ensuring that SELECT OUT and MASTER OUT are not active, and then asserting SYNC OUT for a minimum of 10 microseconds.

Recognition of the MAINT state shall be independent of normal state processing logic. The slave shall not enter Maintenance Mode until the MAINT state has been active for at least 2 microseconds.

See Figure 48 for timing details. See 5.6 for details on Maintenance Mode.

**5.4.5 Selective Reset Sequence.** The Selective Reset sequence (Figure 21) allows the master to reset a single slave and terminate the Maintenance Mode.

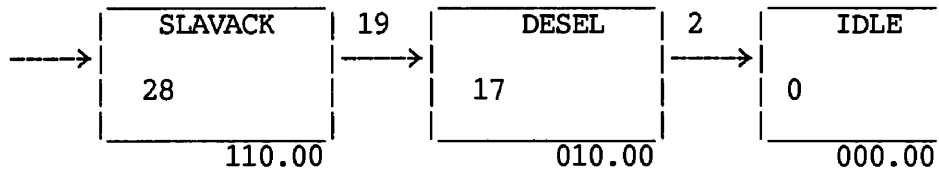


FIGURE 19  
NORMAL DESELECTION SEQUENCE

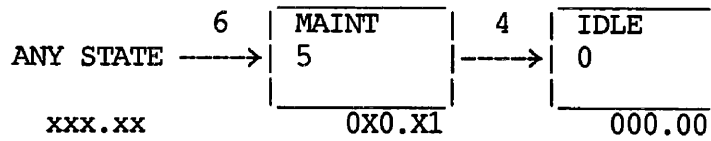


FIGURE 20  
MASTER RESET SEQUENCE

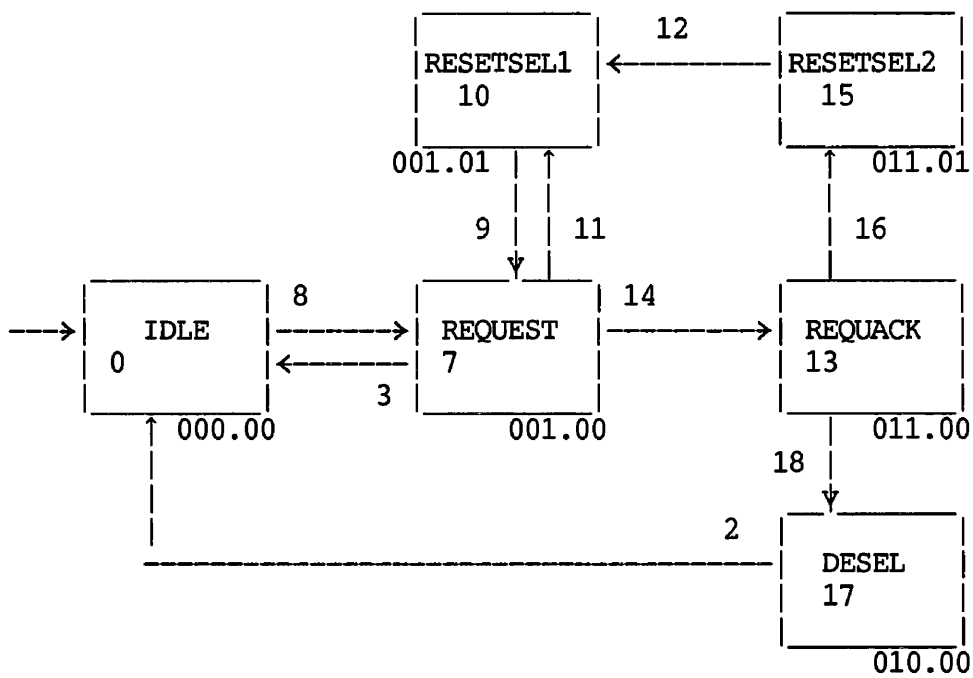


FIGURE 21  
SELECTIVE RESET SEQUENCE

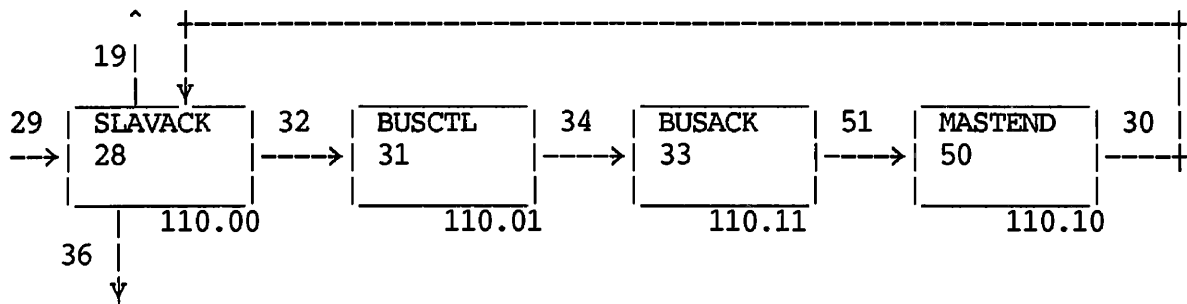


FIGURE 22

**BUS CONTROL SEQUENCE**

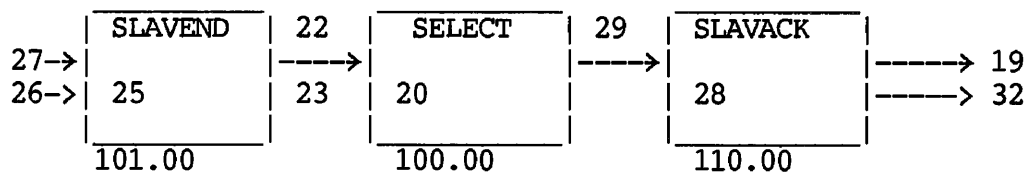


FIGURE 23

**ENDING STATUS SEQUENCE**

The master initiates the sequence by placing the Selective Reset Control octet on BUS A and asserting MASTER OUT. The master shall then allow the slave time to respond by asserting SLAVE IN, but shall disregard SLAVE IN and the contents of BUS B if asserted by the slave. The master shall then assert SYNC OUT for a minimum of 10 microseconds during which time the slave shall negate SLAVE IN if previously asserted, before negating SYNC OUT and returning to the REQUEST state. The slave shall neither initiate its reset action nor release its interface lines until RESETSEL1 has been active for at least 2 microseconds. The master shall then allow the slave time to respond by asserting SLAVE IN. Whether the slave responds or not, the master shall complete the sequence by negating MASTER OUT and monitoring the interface to ensure that the slave completes the sequence by negating SLAVE IN.

Recognition of Selective Reset shall be independent of normal state processing logic. See Figure 49 for timing details.

**5.4.6 Bus Exchange.** The Bus Exchange is started by the master, with a Bus Control sequence to set up an Information Transfer, and

completed by the slave, with an Ending Status sequence when the transfer is ended.

**5.4.6.1 Bus Control Sequence.** The Bus Control sequence (Figure 22) allows the master (or, optionally, the slave) to establish the bus configuration for the subsequent Information Transfer.

The Bus Control sequence is initiated by the master after either Select Status (following selection) or Slave Status (following an Information Transfer) has been accepted. The master shall set the Bus Control octet on BUS A and assert SYNC OUT. The slave shall respond by setting the Bus Acknowledge octet on BUS B and asserting SYNC IN. The master shall end the sequence by negating SYNC OUT.

NOTE: Although the interface returns to SLAVACK when the slave responds by negating SYNC IN, there is no Slave Status octet on BUS B because SLAVACK is simply an intermediate state on the way to beginning an Information Transfer. See Figures 51 and 52.

**5.4.6.2 Ending Status Sequence.** The Ending Status sequence (Figure 23) allows the slave (or, optionally, the master and the slave) to present the status of the previous Information Transfer (if any).



To enter SLAVEND, the slave terminates the Information Transfer by releasing BUS A (Double-Octet Mode, transfers In) and negating SLAVE IN. The master shall respond by releasing BUS B (Double-Octet Mode, transfers Out), setting the Master Status octet on BUS A, and negating MASTER OUT. The slave shall then set the Slave Status octet on BUS B and reassert SLAVE IN to enter the SLAVACK state. See Figures 50 and 53 through 60.

**5.4.7 Information Transfer Sequence.** Figures 24 and 25 represent the sequence of states necessary for Information Transfers. Each horizontal line is labeled (A – E, corresponding to the description below) to illustrate the separate parts of the sequence. An Information Transfer is framed by a Bus Exchange as shown in Figure 26.

An Information Transfer sequence differs depending on whether the ending of a transfer is initiated by the master or by the slave. The slave may terminate a sequence without the transfer of information, as shown in Figure 50. See Figures 52 through 60 for the timing charts with transfer of information.

**5.4.7.1 Operation Command Transfer**

A Condition Bus for transfers Out	Bus Control sequence Information Transfer sequence
B Request transfer Out	
C Transfers Out	
D Master-initiated termination (if any)	
E Ending Status	Ending Status sequence

**5.4.7.2 Operation Response Transfer**

A Condition Bus for transfers In	Bus Control sequence Information Transfer sequence
B First transfer In	
C Additional transfers In	
E Ending Status	Ending Status sequence

**5.4.7.3 Data Transfer Out**

A Condition Bus for transfers Out	Bus Control sequence Information Transfer sequence
B Request transfer Out	
C Transfers Out	
D Master-initiated termination (if any)	
E Ending Status	Ending Status sequence

**5.4.7.4 Data Transfer In**

A Condition Bus for transfers In	Bus Control sequence Information Transfer sequence
B First transfer In	
C Additional transfers In	
D Master-initiated termination (if any)	
E Ending Status	Ending Status sequence

**5.4.7.5 Termination of Information Transfer.** The slave shall terminate an Information Transfer sequence with the Ending Status Sequence. The master may initiate the end of the Information Transfer, and the slave then terminate the sequence with the Ending Status sequence.

**5.4.8 Data Streaming (optional).** Data streaming is the technique that allows high transfer rates over long cable lengths by not interlocking SYNC IN and SYNC OUT, which eliminates a round trip cable delay. This method allows cable delay to be eliminated in determining transfer rate. Data streaming shall only be used during Information Transfers. All control and status sequences shall be interlocked.

NOTE: Normal state sequences do not apply during Data Streaming, since fully interlocked operation is not required.

Request Transfer Settings sequence is used to ascertain what modes of transfer are possible. Slave attributes may be interlocked only, Data Streaming only, or both. In the latter case, the master shall select the mode to be used during slave selection.

**5.4.8.1 Transfer Technique.** The transfer begins with the slave asserting SYNC IN and then negating it to generate a pulse. The period between successive pulses is defined by the transfer rate. Upon recognizing the SYNC IN pulse, the master shall generate a complementary SYNC OUT pulse. The master shall "answer" every SYNC IN pulse with a complementary SYNC OUT pulse.

The SYNC OUT pulse may be generated by the master in two ways:

- (1) Mirror the SYNC IN pulse by detection of leading and trailing edges
- (2) Use a clock value to create a pulse

NOTE: The CCD (Cable Configuration Dependent) value that a slave can recognize at the interface is at least equal to, but may be faster than, the rate at which it can transfer data.

The transmitter shall ensure the proper set-up and hold times with respect to the active edge of its sync pulse.

If the hold time is greater than the one-way cable delay plus set-up times, then the transfers shall appear interlocked.

See Figures 57 through 60.

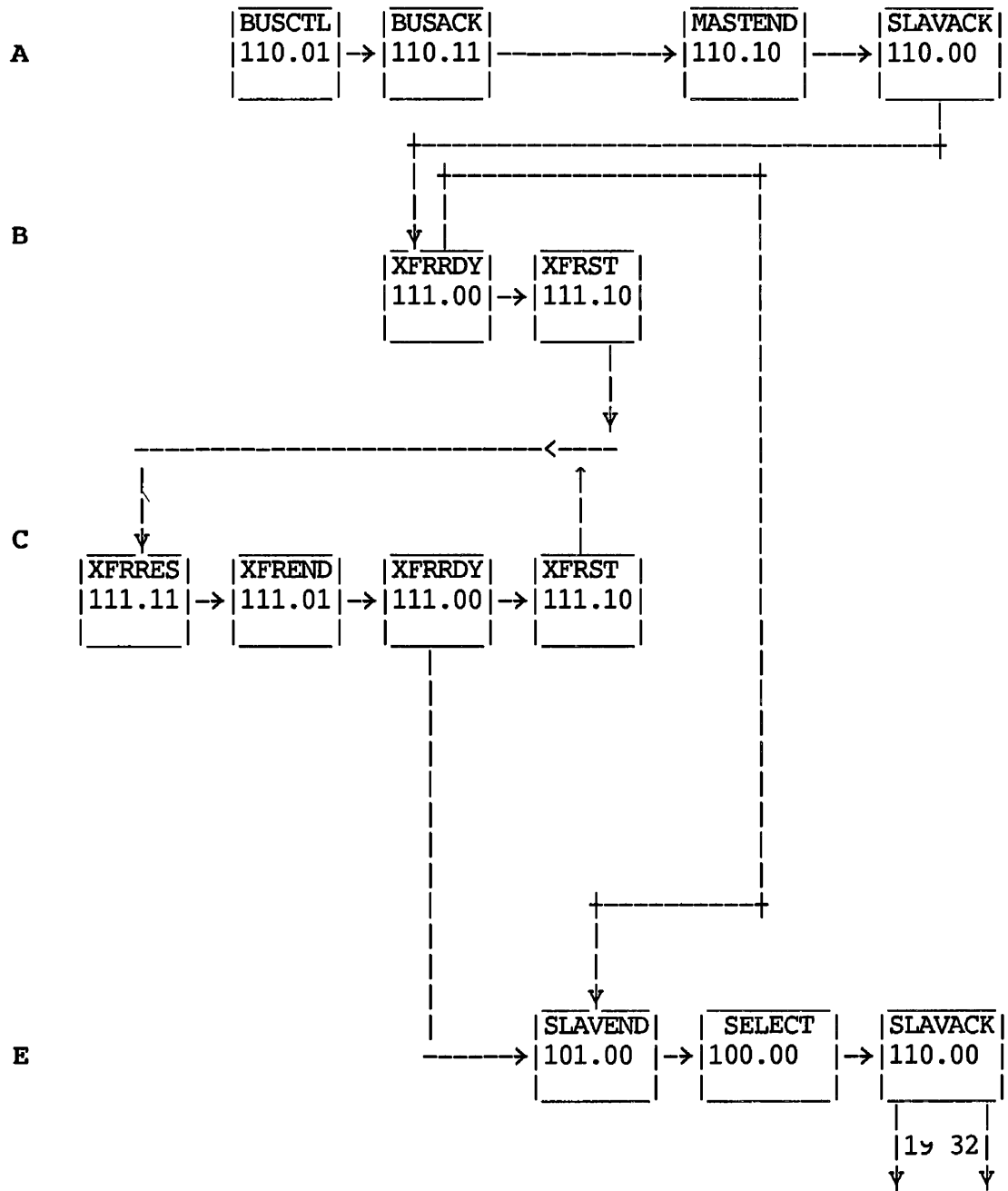


FIGURE 24

SLAVE-INITIATED ENDING OF INFORMATION TRANSFER

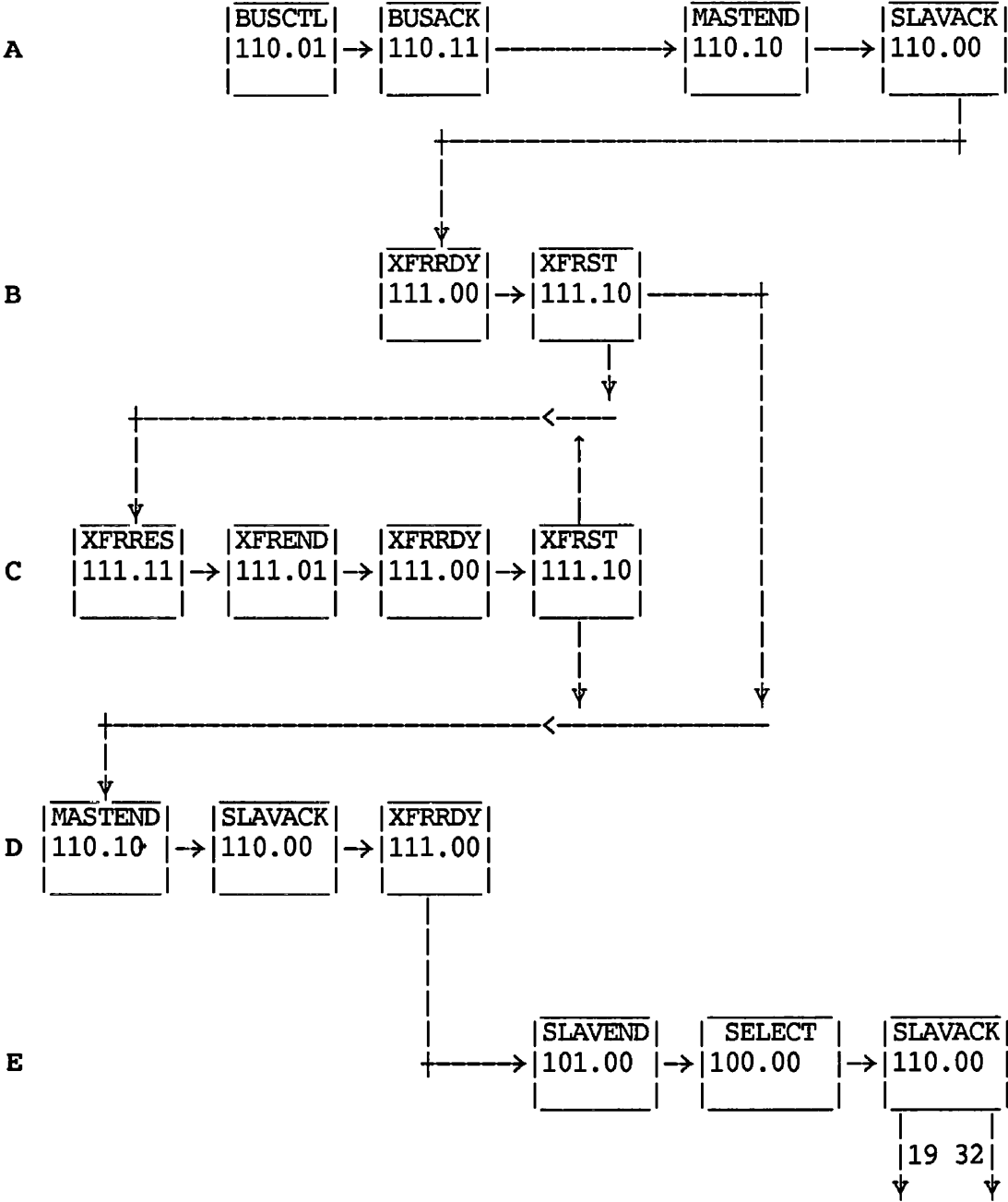


FIGURE 25

MASTER-INITIATED ENDING OF INFORMATION TRANSFER

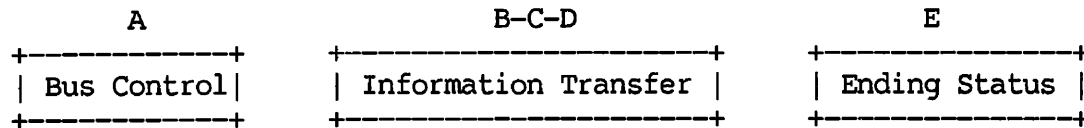


FIGURE 26

## INFORMATION TRANSFER SEQUENCE

**5.4.8.2 Throttling Transfers (optional).** A slave transferring from a buffer may be able to permit the master to stop and start the transfer stream.

If at any point in the transfer the slave has transmitted  $X$  unanswered SYNC IN pulses, it shall wait a minimum of 25 milliseconds for a complementary SYNC OUT pulse. If a SYNC OUT pulse is received, operations shall continue normally. If a SYNC OUT pulse is not received, the slave shall end the transfer sequence.

NOTE: In this transaction,  $X = 8$ , unless the number of pulses ( $X$ ) is vendor dependent or the number is specified by the master via the Logical Interface.

The effect is that after the first  $X$  SYNC IN pulses are transmitted by the slave at its chosen transfer rate, all successive SYNC IN pulses shall only be generated upon receipt of a SYNC OUT pulse, thus allowing the master to dictate the period between SYNC IN pulses and throttling the speed at which the slave can transfer.

**5.4.8.3 Slave Termination of Data Streaming.** To terminate a Data Streaming transfer, the slave shall first stop transmitting SYNC IN pulses. Then it shall wait until it has received an equal number of SYNC OUT pulses from the master, or a minimum of 25 milliseconds has expired without pulses, after which it shall terminate the transfer by negating SLAVE IN and following the normal interlocked Ending Status Sequence.

See Figures 57 and 58.

**5.4.8.4 Master-Initiated Termination of Data Streaming.** To terminate a Data Streaming transfer, the master shall substitute a SYNC OUT pulse with an inactive pulse on the MASTER OUT line having the same pulse width and period requirements of the SYNC OUT pulse. The master shall then continue to "answer" every SYNC IN pulse with complementary SYNC OUT pulses.

For transfers Out, the master shall not transmit information with the MASTER OUT pulse or subsequent SYNC OUT pulses.

For transfers In, the master shall accept information with up to 7 SYNC IN pulses, following generation of the MASTER OUT pulse. This allows all information transmitted by the slave before its recognition of the MASTER OUT pulse to be received by the master, thus maintaining the capability for data integrity.

NOTE: If master-initiated termination of Data Streaming is used when the master does not require a precise match between the number of octets transferred by the master and the slave, the master is not required to accept information after generation of the MASTER OUT pulse.

When the slave senses the MASTER OUT pulse, it shall stop transmitting SYNC IN pulses and wait until it has received an equal number of SYNC OUT pulses, including the MASTER OUT pulse. For transfers Out, the slave shall not latch any information on the MASTER OUT pulse and subsequent SYNC OUT pulses.

After the slave detects the number of SYNC OUT pulses including the MASTER OUT pulse, equaling the number of SYNC IN pulses, or a minimum of 25 milliseconds has expired without pulses, it shall negate SLAVE IN and the normal interlocked Ending Status Sequence is followed.

See Figures 59 and 60.

**5.4.9 Slave-to-Slave Information Transfers (optional).** The master can permit transfers to occur between any two slaves on the interface by defining a dominant slave that shall control MASTER OUT and SYNC OUT. The master remains master of the interface because it retains control of SELECT OUT.

**5.4.9.1 Information Transfers.** It is possible to set up transfers between slaves so that data movement can be accomplished external to the master. This requires the designation of a dominant slave and a subservient slave. The

following is a description of how the two are required to operate:

First, the master shall designate the slave that is to be the dominant slave.

Then, using Operation Commands/Operation Responses, the master shall supply the identity of the subservient slave to the dominant slave. The dominant slave shall monitor the interface and be prepared to assume control after the master selects the subservient slave. The subservient slave shall have its Select Status octet on BUS B during the SLAVACK state.

If the subservient slave is not busy, the master shall release BUS A and the dominant slave shall assume control of MASTER OUT and SYNC OUT (thus assuming the role of the master on the interface). The master thus permits the dominant slave to initiate Information Transfers with the subservient slave (which is operating normally), but retains, through SELECT OUT, the ability to abort the operation.

Each time the intermediate SELECT state is entered, the dominant slave shall set the Master Status octet on BUS A. The master shall monitor this octet to detect the Slave — Slave Operation Completed bit.

The dominant slave shall relinquish control to the master by posting the Slave — Slave Operation Completed bit in the Master Status octet. The subservient slave shall proceed normally to enter SLAVACK.

The dominant slave is responsible to ensure that operations with the subservient slave have been completed. This typically requires that a null transfer be executed after the last required one because Slave Status is presented after Master Status and the dominant slave would not know if the last required transfer was successful until after posting the Slave — Slave Operation Completed bit.

The master shall terminate the Slave — Slave Information Transfer by deselecting the subservient slave. The master shall reselect the dominant slave to obtain the Operation Response.

**5.4.9.2 Error Recovery Considerations.** If the subservient slave is busy during initial selection, the master can continue to retry until successful or reselect the dominant slave to terminate the process.

If the master must regain control of the bus during the process, it shall do so by deselecting the subservient slave. The dominant slave shall detect the deselection as an abnormal termination and prepare Operation Response for pre-

sentation to the master when it is next selected. The subservient Slave shall proceed through normal deselection, if it was in the SLAVACK state when SELECT OUT was negated.

NOTE: The implementation described in 5.4.9 requires the use of features in the interface that are defined as optional. In addition, a master that intends to support Slave — Slave Information Transfers must be able to monitor the MASTER OUT and SYNC OUT lines that are under control of the dominant slave.

**5.5 Bus Octet Definitions.** Table 9 defines the usage of bus octets for each state and transition. The following section specifies the BUS A octets, followed by the associated BUS B response octets.

NOTE: The optional functions defined within each octet are identified by the bits being enclosed in parentheses.

If the octet itself is optional, required bits within it do not have parentheses. Only optional bits in an optional octet have parentheses.

**5.5.1 BUS A Selection Octet Bit Definitions Presented during the SELECT state.** During the selection sequence, BUS A contains the addressing information for the selection.

**5.5.1.1 BUS A Selection Octet** (See Figure 27). When Bit 7 = 0, the addressed slave shall respond on BUS B to the Selection octet on BUS A (see 5.3.2).

**5.5.1.1.1 Slave Address.** Bit 4 is the least significant bit (LSB) of the slave address.

**5.5.1.1.2 Change Transfer Mode.** When Bit 3 = 1, the addressed slave shall change its current mode of transfer (Interlocked or Data Streaming). See 5.5.8.3.

**5.5.1.1.3 Change Octet Mode.** When Bit 2 = 1, the addressed slave shall change its current mode of octet operation (SOM or DOM). See 5.5.8.3.

**5.5.1.1.4 Priority Hold.** When Bit 1 = 1 and a selection is established, the slave shall maintain an explicit allegiance after deselection to this port until:

(1) A subsequent selection is established without the Priority Hold bit set in the Selection octet or

(2) A selection by another port is established with both the Priority Hold and Priority Select bits set in the Selection octet or

(3) An appropriate Reset is executed by the slave

**5.5.1.1.5 Priority Select.** When Bit 0 = 1, the specified slave shall release the current

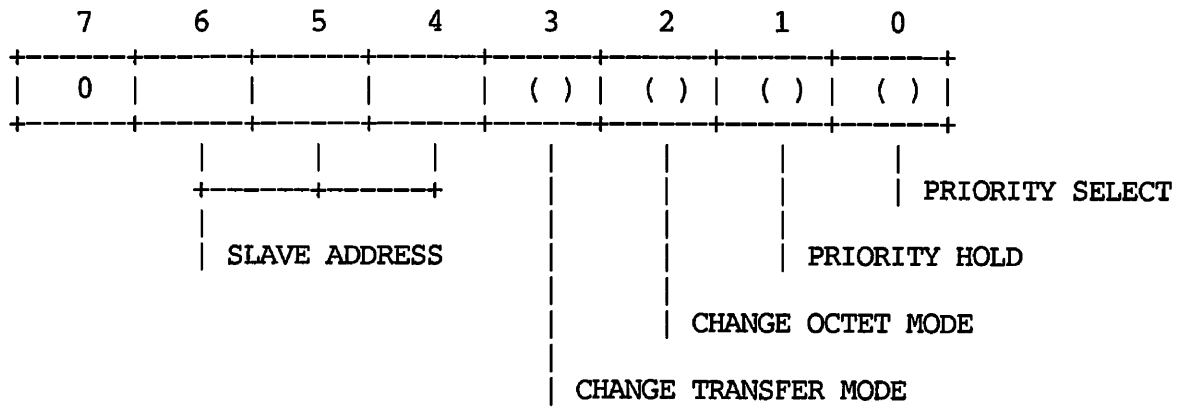


FIGURE 27

## BUS A SELECTION OCTET

port to which it is dedicated, provided that an alternate port does not have a Priority Hold in effect, and shall respond to the requesting master.

If two or more ports of a given slave are in the SELECT state at the same time with the Priority Select bit set in the Selection octet, and the slave does not have a Priority Hold in effect for any port not attempting a selection, the slave shall connect to one and only one of the ports. The other ports shall receive a Busy indication.

A successful selection with the Priority Select bit set in the Selection octet shall cause any other port with a selection established and not in the SELECT state during a Selection sequence to terminate its selection. The termination may be orderly or abrupt depending on the slave's implementation.

**5.5.1.1.6 Priority Hold and Priority Select.** When both Bit 1 = 1 and Bit 0 = 1, the specified slave shall release the current port to which it is dedicated, regardless of its previous condition, provided that another port had not previously established selection with both of the bits set.

The specified slave shall maintain allegiance to the selected post after deselection until

(1) A subsequent selection is established without the Priority Hold and Priority Select bits set or

(2) An appropriate reset is executed by the slave (see Table 10).

If any of the optional bits (bits 0 – 3) set are not supported by the slave, the addressed

slave shall not acknowledge selection; i.e., the slave shall not assert SLAVE IN.

**5.5.1.2 BUS A Facility Selection Octet** (optional) (See Figure 28). The master has the ability to select any of 8 slaves and indirectly address up to 16 facilities. The slave shall select facilities on behalf of the master.

**5.5.1.2.1 Slave Address.** Bit 4 is the least significant bit (LSB) of the slave address.

**5.5.1.2.2 Facility Address.** Bit 0 is the LSB of the facility address.

If this option is not supported, the slave identified in Bits 4 – 6 shall not acknowledge selection; i.e., the slave shall not assert SLAVE IN.

If it is supported and the facility address is not valid, then the Slave Status octet shall be used to indicate an invalid selection address.

**5.5.2 BUS B Select Status Octet Presented during the SLAVACK state** (See Figure 29). The slave responds to selection by driving its bit-significant address and releasing all other bus bits to provide Select Status, which is defined as follows:

If the addressed slave is not present on the interface or does not recognize its address, SLAVE IN will not be asserted and no address bits shall be asserted.

The master can detect invalid selection conditions by analysis of Select Status, for example, incorrect selection will have the wrong address bit posted, multiple selection will have more than one address bit posted.

TABLE 10

PRIORITY HOLD AND PRIORITY SELECT

	Port B									
	PH	PS	PH	PS	PH	PS	PH	PS		
			0	0	0	1	1	0	1	1
Port A not Selected	0	0	B		B		B		B	
	0	1	B		B		B		B	
	1	0	A		A		A		B	
	1	1	A		A		A		A	
Port A Selected	0	0	A		B		A		B	
	0	1	A		B		A		B	
	1	0	A		A		A		B	
	1	1	A		A		A		A	

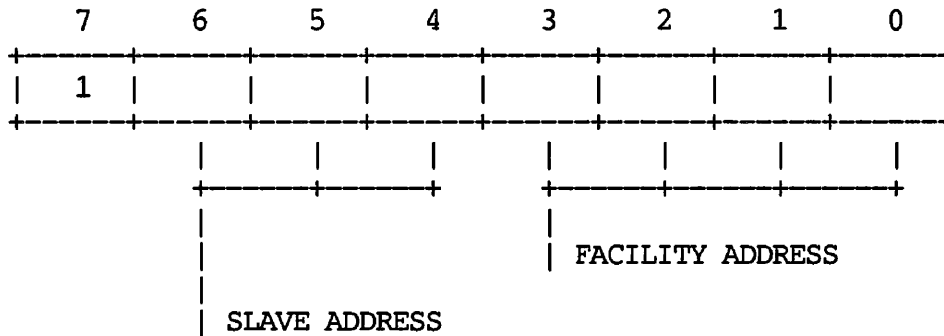


FIGURE 28

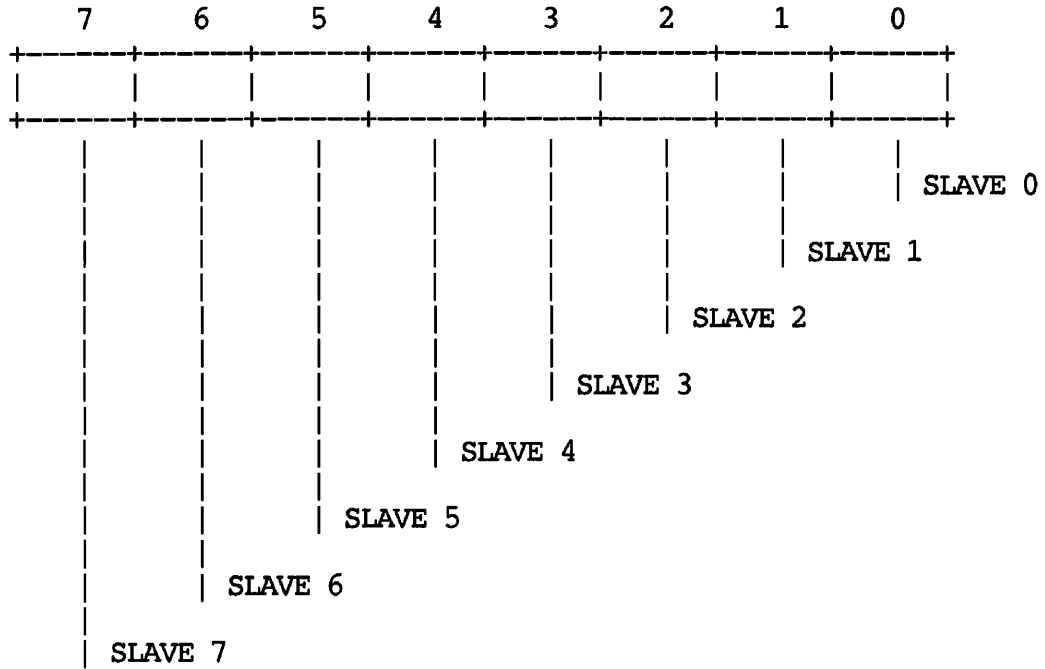
BUS A FACILITY SELECTION OCTET

To detect multiple selection, the master shall wait until all slaves have had enough time to respond.

**5.5.3 BUS A Bus Control Octet Presented during the BUSCTL state.** The Bus Control octet (Figure 30) describes the subsequent Information Transfer and bus configuration. If the master sets up a Bus Control that is not recognizable at the slave, the slave shall end the subsequent Information Transfer sequence without an Information Transfer (see Figure 50).

The Bus Control octet is defined as follows:  
The use of Bits 0 – 5 may be Vendor Unique if not defined by the Logical Interface. The use of these bits shall not affect the Physical Interface hardware.

**5.5.4 BUS B Bus Acknowledge Octet Presented during the BUSACK State** (See Figure 31). The contents of this octet are optional. If none are supported, the slave shall ensure that the bus contents are stable with correct parity during the BUSACK state, and that zero is posted.



NOTE: The parity line shall be released by the slave and parity shall not be checked by the master.

FIGURE 29

BUS B SELECT STATUS OCTET

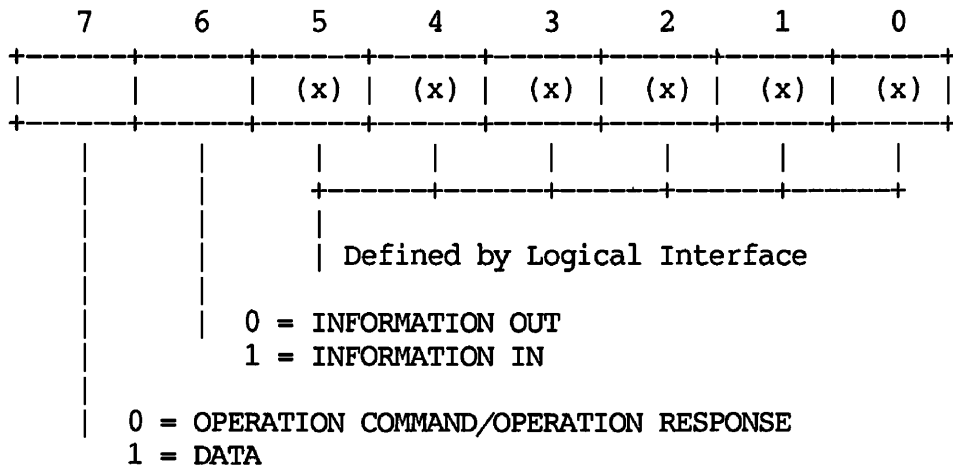


FIGURE 30

BUS A CONTROL OCTET



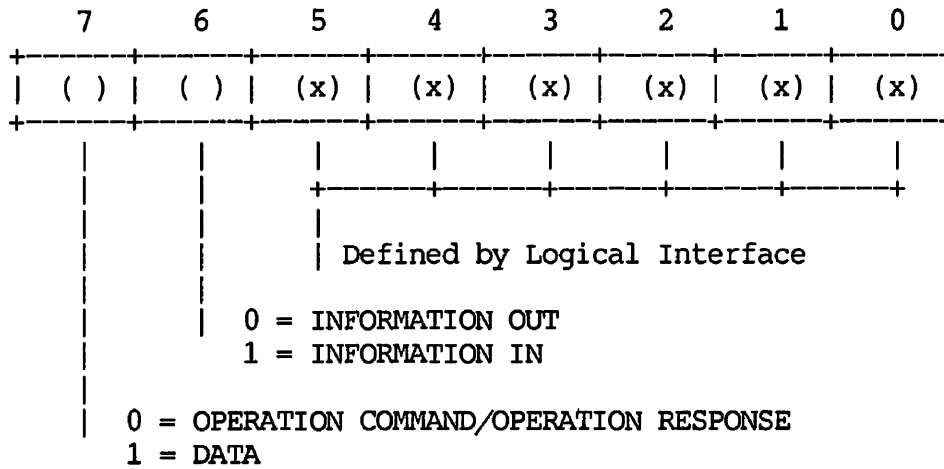


FIGURE 31

**BUS B BUS ACKNOWLEDGE OCTET**

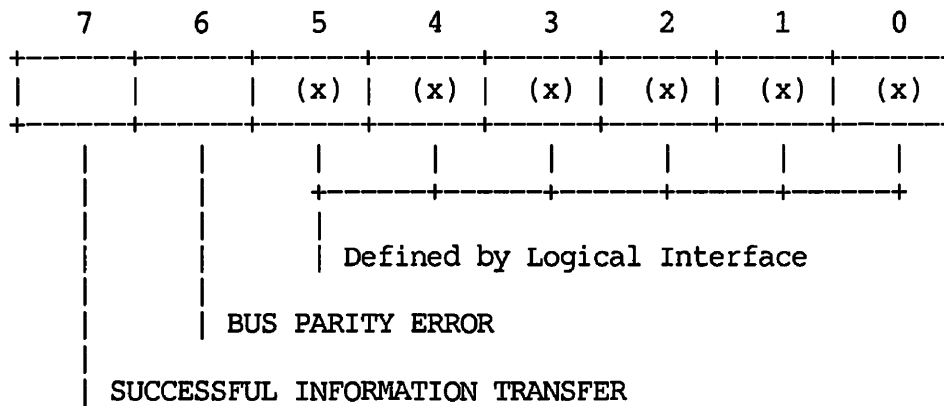


FIGURE 32

**BUS A MASTER STATUS OCTET**

In an intelligent subsystem there may be a need for the master to receive responses from the slave immediately after Bus Control.

The use of Bits 0 – 5 may be Vendor Unique if not defined by the Logical Interface. The use of these bits shall not affect the Physical Interface hardware.

**5.5.5 BUS A Master Status Octet Presented during the SELECT state.** The Master Status octet (Figure 32) is used by the master to inform the slave whether or not the previous Information Transfer was successful, and if a bus parity error had been detected.

**5.5.5.1 Successful Information Transfer.**

When Bit 7 = 1, the previous Information Transfer as viewed by the master completed successfully.

**5.5.5.2 Bus Parity Error.** When Bit 6 = 1, the master detected a bus parity error on the Bus Acknowledge octet or the Information Transfer In.

The use of Bits 0 – 5 may be Vendor Unique if not defined by the Logical Interface. The use of these bits shall not affect the Physical Interface hardware.

**5.5.6 BUS B Slave Status Octet Presented during the SLAVACK state.** The Slave Status octet (Figure 33) describes the slave-determined ending status of the previous Information Transfer, if any.

**5.5.6.1 Successful Information Transfer.**

When Bit 7 = 1, the previous Information Transfer completed successfully.

**5.5.6.2 Bus Parity Error.** When Bit 6 = 1, the slave detected a parity error in the Bus Control octet, the Information Transfer Out, or the Master Status octet.

The use of Bits 0 – 5 may be Vendor Unique if not defined by the Logical Interface. The use of these bits shall not affect the Physical Interface hardware.

**5.5.7 BUS A Request Modifier Octet Presented during the REQUEST state.** The Request Modifier octet is presented during the REQUEST state and is used by the master in various forms to request interrupt classes, status, or transfer settings, and is also used to initiate Selective Reset.

**5.5.7.1 Request Interrupts Octet** (See Figure 34). When Bit 7 = 0, all slaves on the interface shall respond on BUS B (see 5.5.8.1) based on the settings of Bits 0 – 6.

**5.5.7.1.1 Report Busy.** When Bit 6 = 1, all slaves that are Busy shall place their bit-significant address on BUS B.

**5.5.7.1.2 Report Ready Status.** When Bit 5 = 1, all slaves that are Ready for use shall place their bit-significant address on BUS B.

**5.5.7.1.3 Power Fail Alert.** When Bit 4 = 1, the master is informing the slaves that it has detected that power is failing. The slaves shall acknowledge by placing their address on BUS B after they have taken the appropriate action to permit a graceful termination of activity.

**5.5.7.1.4 Power On Status Request.** When Bit 3 = 1, all slaves with power on (but not necessarily ready) shall place their bit-significant address on BUS B.

**5.5.7.1.5 Interrupt Class.** Slaves with interrupts pending shall respond by placing their bit-significant address on BUS B. The definition of interrupts within a class may vary between different implementations of the interface; however, they shall always be ranked between Class 3 (most important) and Class 1 (least important).

The vendor shall define the type of interrupts within each class.

When Bit 2 = 1, slaves with Class 3 Interrupts pending shall respond. Class 3 Interrupts would typically be asynchronous and critical, and deserving of immediate attention from the master.

When Bit 1 = 1, slaves with Class 2 Interrupts pending shall respond. Class 2 Interrupts would typically be associated with a data transfer.

When Bit 0 = 1, slaves with Class 1 Interrupts pending shall respond. Class 1 Interrupts would typically be status associated with the completion of operations, but may also be asynchronous and noncritical.

NOTE: If more than one status or interrupt request is set by the master, the slaves shall respond to the logical OR of the conditions.

**5.5.7.2 Request Facility Interrupts Octet** (Optional). If all the Interrupt Class bits are zero, this octet (Figure 35) is interpreted as either Request Transfer Settings (see 5.5.7.3) or Request Slave Interrupts (see 5.5.7.4).

When Bit 7 = 1 and bits 0 – 3 are not zero, the slave specified by the address in Bits 6 – 4 shall decode the Request Facility Interrupts octet.

**5.5.7.2.1 Slave Address.** Bit 4 is the least significant bit (LSB) of the slave address.

**5.5.7.2.2 Facility Range.** Bit 3 is used to identify the range of addresses to respond on BUS B.

0: addresses 0 – 7 respond

1: addresses 8 – F respond

**5.5.7.2.3 Interrupt Class.** See 5.5.7.1.5

NOTE: If more than one interrupt request is set by the master, the facilities shall respond to the logical OR of the conditions.

**5.5.7.3 Request Transfer Settings Octet** (See Figure 36)

**5.5.7.3.1 Slave Address.** Bit 4 is the least significant bit (LSB) of the slave address.

**5.5.7.3.2 Request Transfer Settings.** When Bits 0 – 3 are set to zero, the selected slave shall respond with the Transfer Settings octet (see 5.5.8.3).

**5.5.7.4 Request Slave Interrupts Octet** (Optional). This request (Figure 37) allows the master to obtain status and all the interrupts from the slave.

**5.5.7.4.1 Slave Address.** Bit 4 is the least significant bit (LSB) of the slave address.



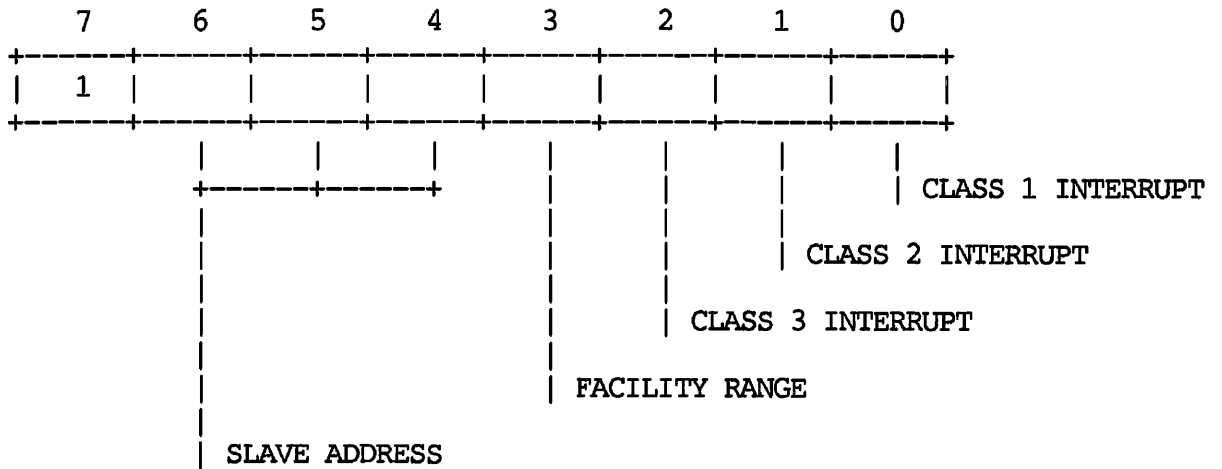


FIGURE 35

REQUEST FACILITY INTERRUPTS OCTET

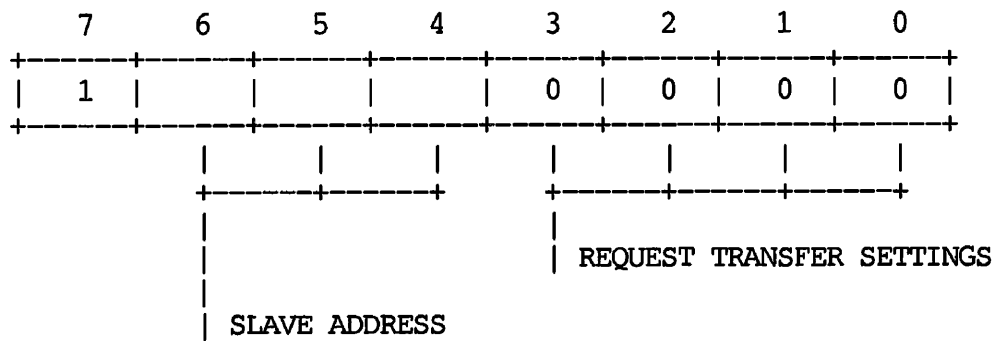


FIGURE 36

REQUEST TRANSFER SETTINGS OCTET

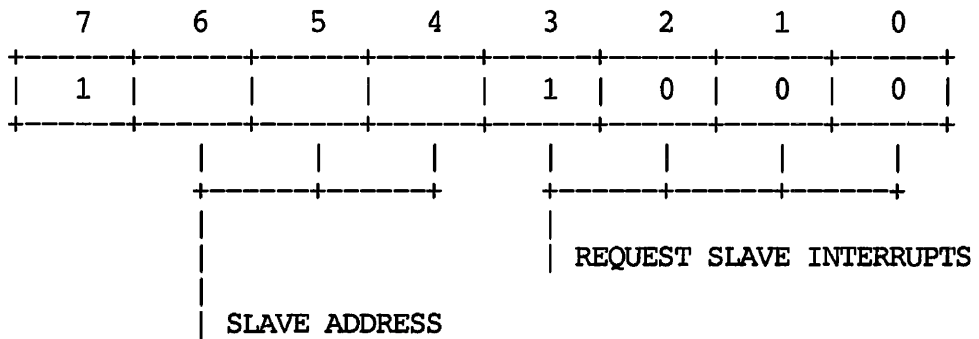


FIGURE 37

REQUEST SLAVE INTERRUPTS OCTET

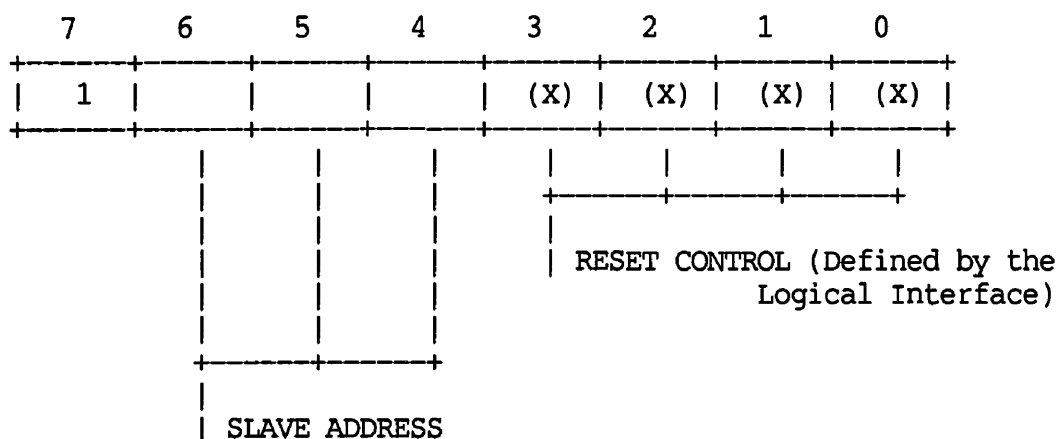


FIGURE 38

## SELECTIVE RESET CONTROL OCTET

**5.5.7.4.2 Request Slave Interrupts.** When Bit 3 is set to 1 and Bits 2 – 0 are set to zero, the selected slave shall respond with the Slave Interrupts octet (see 5.5.8.4).

**5.5.7.5 Selective Reset Control Octet Interpreted during the RESETSEL1 and RESETSEL2 States.** The Selective Reset Control octet (Figure 38) is used to perform Selective Reset (see 5.4.5) of the addressed slave. This octet is first presented during the REQUEST state, and acquires its specific meaning when in RESETSEL1 or RESETSEL2.

**5.5.7.5.1 Slave Address.** Bit 4 is the least significant bit (LSB) of the slave address.

**5.5.7.5.2 Reset Control.** Bits 0 – 3 shall be used to define the type of Selective Reset to be executed by the slave. The use of Bits 0 – 3 is established by the master and the slave at the Logical Interface or may be Vendor Unique. The use of these bits shall not affect the Physical Interface hardware.

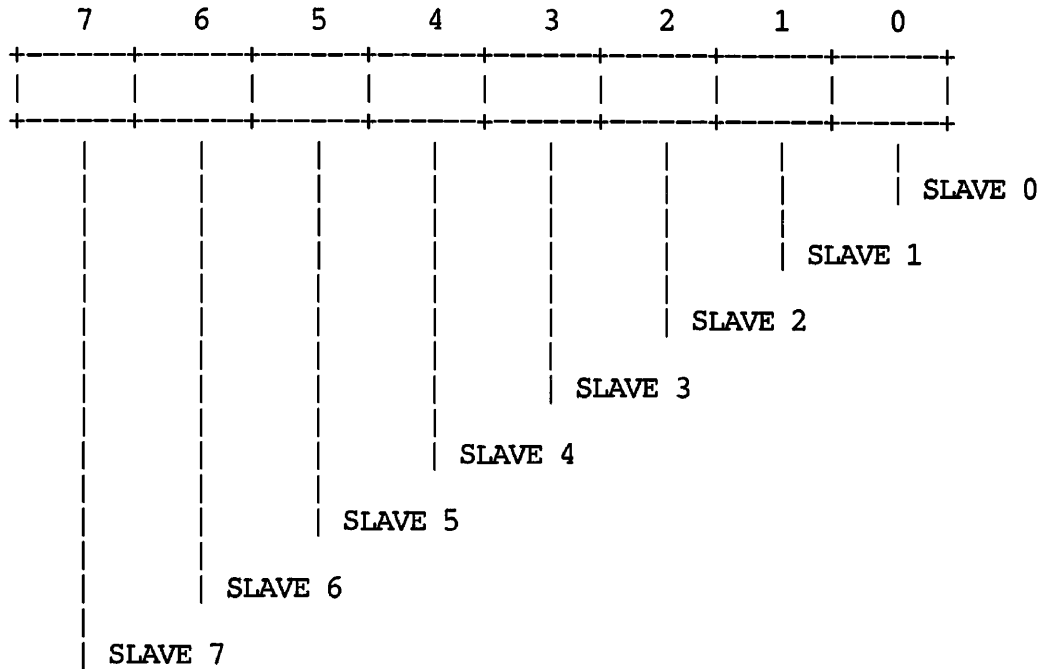
NOTE: There is no BUS B response to Selective Reset. If a slave interprets the octet and responds during a Selective Reset sequence, the response is ignored by the master. The slave shall interpret this octet as a Selective Reset octet during the RESETSEL1 and RESETSEL2 states.

**5.5.8 BUS B Responses to Request Modifier Octet Presented during the REQUEST or REQUACK states**

**5.5.8.1 Address Octet Response to Request Interrupts Presented during the REQUEST State.** If there is an interrupt or status that satisfies the requirements of the Request Interrupts octet on BUS A, the slave shall respond by driving only its address bit (and shall ensure that all other bits are released) to provide the Address octet, which is defined as shown in Figure 39.

The slave shall make no control signal response to the "polling" of interrupts. This octet shall be presented by the slave on BUS B during the REQUEST state. The master is responsible to ensure that sufficient time has elapsed for all slaves to respond.

**5.5.8.2 Address Octet Response to Request Facility Interrupts Presented during the REQUACK State (Optional).** The address bits shall be set on BUS B by the slave if there are any interrupts that satisfy the requirements in the facility range specified. Table 11 summarizes the bit-significant address mapping.



NOTE: The parity line shall be released by the slave and parity shall not be checked by the master.

FIGURE 39

ADDRESS OCTET RESPONSE TO REQUEST INTERRUPTS

TABLE 11

FACILITY ADDRESS MAPPING

BUS B BIT	RANGE 0-7 ADDRESSES	RANGE 8-F ADDRESSES
7	ADDRESS 7	ADDRESS F
6	" 6	" E
5	" 5	" D
4	" 4	" C
3	" 3	" B
2	" 2	" A
1	" 1	" 9
0	" 0	" 8

NOTE: Parity may or may not be valid.  
Parity shall not be checked by the master.

### 5.5.8.3 Transfer Settings Octet Presented during the REQUACK State (See Figure 40)

**5.5.8.3.1 Maintenance Mode.** This mode shall be used by the slave to indicate its Maintenance Mode setting to the master:

Bit 6: 0 = Maintenance Mode 1 capability only  
1 = Maintenance Modes 1 and 2 capability

**5.5.8.3.2 Current Setting.** This mode shall be used by the slave to identify to the master whose modes are currently set:

Bit 5: 0 = Single Octet Mode  
1 = Double Octet Mode

Bit 4: 0 = Interlocked Transfer  
1 = Data Streaming Transfer

**5.5.8.3.3 Transfer Mode Capability.** When Bit 3 = 1, the slave can transfer in Data Streaming Mode. When Bit 2 = 1, the slave can transfer in Interlocked Mode. When both bits are set, the slave is capable of operating in either mode.

**5.5.8.3.4 Octet Capability.** When Bit 1 = 1, the slave is capable of operating in Double-Octet Mode. When Bit 0 = 1, the slave is capable of operating in Single-Octet Mode. When both bits are set, the slave is capable of operating in either mode.

If a slave is capable of supporting more than one type of octet mode or more than one type of transfer mode, it shall be able to change the current mode under control of the master (see 5.5.1.1).

**5.5.8.4 Slave Interrupts Octet (Optional) Presented during the REQUACK State (See Figure 41)**

**5.5.8.4.1 Busy Status.** When Bit 6 = 1, the slave is Busy.

**5.5.8.4.2 Ready Status.** When Bit 5 = 1, the slave is Ready for use.

**5.5.8.4.3 Priority Hold Status.** When Bit 4 = 1, the slave has a Priority Hold established at one of its ports.

**5.5.8.4.4 Priority Select Status.** When Bit 3 = 1, the slave is Priority Selected at another port.

**5.5.8.4.5 Interrupt Class.** When Bit 2 = 1, the slave has a Class 3 Interrupt pending. When Bit 1 = 1, the slave has a Class 2 Interrupt pending. When Bit 0 = 1, the slave has a Class 1 Interrupt pending.

The use of Bit 7 may be Vendor Unique if not defined by the Logical Interface. The use of this bit shall not affect the Physical Interface hardware.

**5.6 Maintenance Mode.** To enter Maintenance Mode, the master shall initiate the Master Reset sequence (see 5.4.4). When in MAINT state, the master may select one of two maintenance modes, hereafter referred to as Maintenance Mode 1 (MM1) and Maintenance Mode 2 (MM2). Slaves shall support at least one of these two modes. Maintenance Mode offers capabilities to the master when normal methods of interface communications are not operational (failure) or may be inappropriate (diagnostics). The maintenance logic shall have the ability to take over the interface drivers in the slave and, optionally, to communicate with the master.

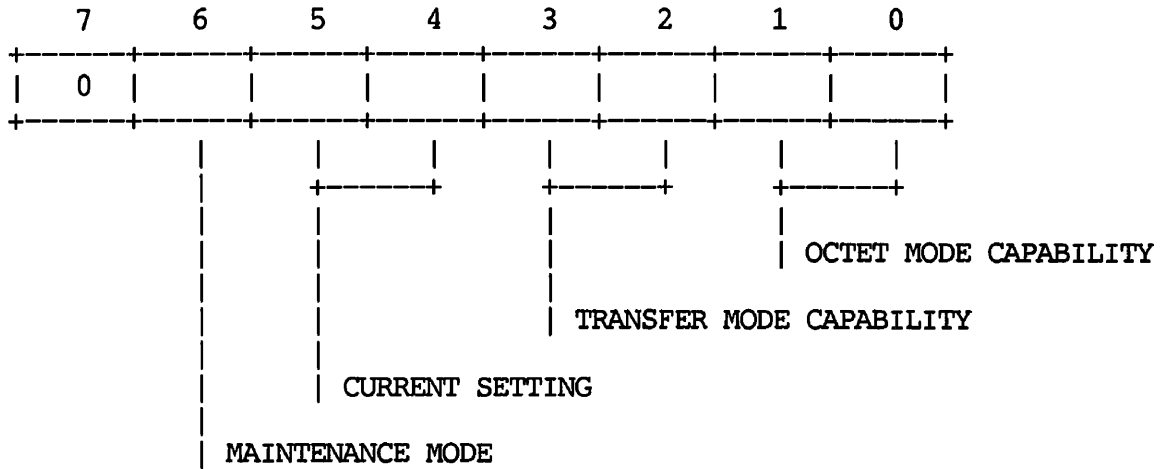
The actions of a Master Reset are defined by the logical interface.

MM1 is a simple technique to provide a degree of isolation that improves the serviceability and availability of the interface. MM2 is an alternative protocol that provides a serial, fault-tolerant method of communication using the same signal lines. The master adapts to the capabilities of Maintenance Mode provided by the slaves.

Figure 42 illustrates a slave implementation including the maintenance logic. Normal operations are directed from the drivers and receivers into the functional circuits. When communication with the maintenance logic is required, the signals are disconnected from the functional circuits and diverted to the maintenance circuits.

Both of the defined modes require that the slave provide logic that is independent (as far as is practical) of the logic associated with normal functions. MM1 is a very limited subset of MM2 that provides a mechanism for resetting the MM1 slave and for releasing of the interface drivers. The master may selectively restore use of a slave's drivers, if released by the MM1 circuits, by using the Selective Reset sequence. The MM2 circuits extend the capabilities beyond those available with MM1.

MM1 and MM2 circuits can coexist on the same Physical Interface. A slave that has incorporated MM2 and that is connected to a master that is only capable of supporting the MM1 functions responds in the same manner as a slave with MM1 circuits. A dominant slave cannot



MAINTENANCE MODE

FIGURE 40  
TRANSFER SETTINGS OCTET

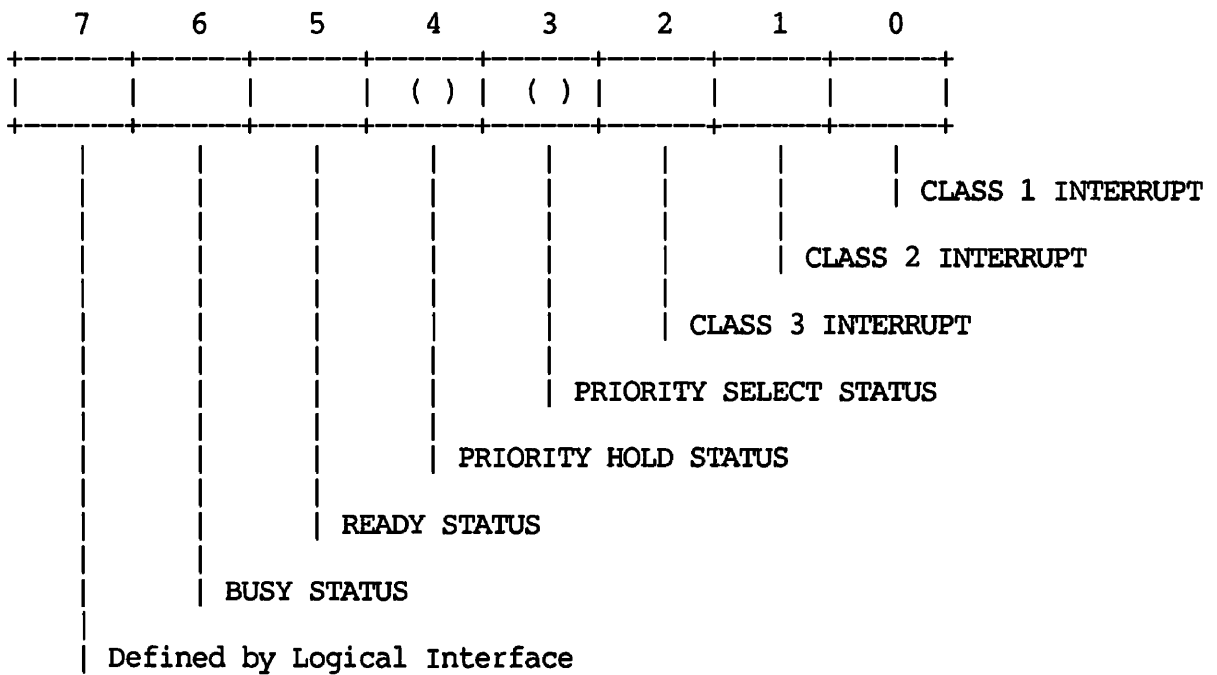


FIGURE 41  
SLAVE INTERRUPTS OCTET



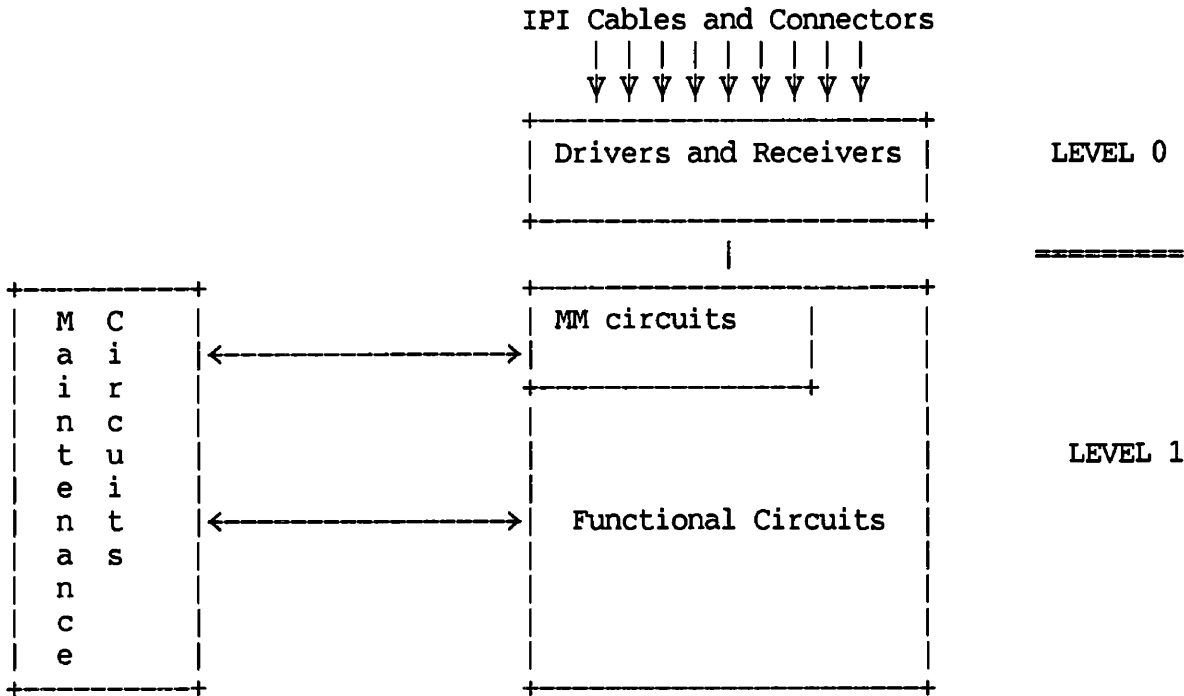


FIGURE 42

**BLOCK DIAGRAM OF MAINTENANCE MODE**

assume the role of the master when in maintenance mode. (See Figure 61.)

MM1 and MM2 are compatible with slaves which support Single Octet Mode, Double Octet Mode, or both.

MM control signals are developed by voting on triplicated lines. This technique provides fault tolerance. Voting shall be done on the static condition of the triplicated lines (i.e., the condition of the lines is not edge sensitive).

**5.6.1 Maintenance Mode 1**

**5.6.1.1 MM1 Capabilities.** MM1 enables releasing the slave's drivers from the interface. This capability, in conjunction with the Selective Reset state, can be used to isolate a slave that is holding a driver active on the interface. This may allow the master to continue using the remaining operational slaves on the interface when otherwise this would be impossible.

MM1 provides a reset capability.

The master may invoke MM1 at any time by placing the control Out lines into the MAINT state. The MM logic associated with each slave shall release the drivers from the interface after it is recognized that the master has placed the Control Out lines into the MAINT state.

**5.6.1.2 MM1 Scenario.** Table 12 outlines the MM1 scenario. As can be seen, the MM1 scenario is separated into three phases. Each of these phases are described more fully in 5.6.1.2.1 through 5.6.1.2.3. Table 13 provides the signal line assignments during the first two phases of the MM1 scenario.

**5.6.1.2.1 First Phase (MM1) — Assert Master Reset Sequence.** The MM1 circuits shall release all the drivers from the interface after the master places the control out lines into the MAINT state.

**5.6.1.2.2 Second Phase (MM1) — Enter IDLE State, Begin Reset.** Whether or not a reset and permanent releasing of the interface drivers occurs depends upon the state of three BUS A lines, referred hereafter as the DATA OUT lines, at the time SYNC OUT is negated. If at least two of these three lines are active at the trailing edge of SYNC OUT, the slave shall be reset and the drivers shall remain released until a Selective Reset sequence is issued. The reset shall persist as long as DATA OUT remains active. If at least two of the DATA OUT lines are not active at the trailing edge of SYNC OUT, the drivers shall be restored and no reset shall be issued. This latter sequence enables MM2

operations to be performed without disrupting MM1 slaves.

NOTE: To reset and release any attached MM2 slaves in addition to MM1 slaves, both the DATA OUT and the ENABLE OUT signals shall be activated by an MM1 master before negating SYNC OUT (see 5.6.2.2).

**5.6.1.2.3 Third Phase (MM1) — Selective Reset of Slaves.** The master may selectively restore a slave's interface drivers by use of the Selective Reset sequence. The response to the Selective Reset sequence is delayed until the MM1 circuits release the control In line drivers during RESETSEL1.

**5.6.2 Maintenance Mode 2.** This alternative to MM1 provides a fault-tolerant serial protocol.

**5.6.2.1 MM2 Capabilities.** MM2 performs all the functions of MM1 when DATA OUT and ENABLE OUT are active.

The master may use MM2 to obtain a description of faults that may or may not otherwise preclude normal sequences.

NOTE: To assist in the description of this capability, terms such as Fault Descriptor Shift Register (FDSR) are used (see 5.6.2.4.4.1). These connotations of registers do not denote a requirement of any implementation technique.

The MM2 circuits within a specific slave can be selected, thereby minimizing unnecessary disruptions to any other slaves on the interface.

Expanded functionality is available with the use of Extended Orders (see 5.6.2.6.3).

As is the case with MM1, the master invokes MM2 by placing the three control Out lines into MAINT state.

**5.6.2.2 MM2 Scenario.** Table 14 outlines the MM2 scenario. The MM2 scenario is broken up into the three phases shown in Table 14 and more fully described in 5.6.2.2.1 through 5.6.2.2.3. Table 13 provides the signal line assignments used during the first two phases of the MM2 scenario.

**5.6.2.2.1 First Phase (MM2) — Enter MAINT State.** After entering MAINT state, all MM2 slaves shall release their interface drivers.

While MAINT state is active, the master may transfer an MM2 address into each attached MM2 slave (see MM2 Write sequence, 5.6.2.4). The MM2 circuits with an address match shall become selected and enable the drivers, thus becoming capable of executing subsequent MM2 orders.

**5.6.2.2.2 Second Phase (MM2) — Enter IDLE State and Begin Reset.** A decision to reset

and continue isolating the drivers occurs when SYNC OUT is negated to enter the IDLE state. In this mode (unlike MM1), both the DATA OUT and the ENABLE OUT signals shall be active at the trailing edge of SYNC OUT before the reset is generated and the drivers shall be kept released. The reset shall persist until either the DATA OUT or the ENABLE OUT signal is deactivated.

An MM2 slave shall appear the same as an MM1 slave when connected to a master that does not support MM2 sequences, as long as the master ensures that ENABLE OUT, as well as DATA OUT, is active at the trailing edge of SYNC OUT.

**5.6.2.2.3 Third Phase (MM2) — Selective Reset of Slaves.** The master may either use the Selective Reset sequence (see MM1 third phase, 5.6.1.2) or re-enter Phase 1 of the MM2 scenario and issue the appropriate order to restore a slave's interface drivers, should they be released by the MM2 circuits.

NOTE: MM2 allows slaves to be selectively released by issuing certain selective MM2 orders, which eliminates the need to use the Selective Reset sequence to restore an MM2 slave.

**5.6.2.3 MM2 Line Usage with SYNC OUT Asserted (Table 14, First Phase).** All the MM2 signals described in 5.6.2.3.1 and 5.6.2.3.2 are developed by taking a majority vote on the three signal lines assigned to each MM2 signal. This technique assures the master of the use of the MM2 slave even when faults, such as an open interface wire, occur.

#### 5.6.2.3.1 Outbound MM2 Signals

(1) **ENABLE OUT.** The ENABLE OUT signal is primarily used by the MM2 circuits to determine that MM2 Write sequence is completed and that the order in the deserialization register can be interrogated. In a sense, then, this line is a "framing" line that tells the slave when the orders and address information sent it are properly aligned and can be sampled.

A secondary use of the ENABLE OUT signal in conjunction with the CLOCK OUT and DATA OUT signals is to establish whether or not a subsequent serial data transfer is to be from or to the slave. This secondary usage of the ENABLE OUT is described more completely in 5.6.2.4.

(2) **CLOCK OUT.** The primary use of the CLOCK OUT signal is to shift data either into or out of the MM2 circuits during the MM2 write or read sequences.

TABLE 12  
MM1 SCENARIO SUMMARY

MAINTENANCE MODE 1	MASTER ACTION	SLAVE ACTION
FIRST PHASE	Enter MAINT State	Upon recognition of MAINT state the MM1 slave shall release the interface drivers
SECOND PHASE	Assert the DATA OUT (and ENABLE OUT)* signals and then enter IDLE state	If DATA OUT is active when SYNC OUT is negated a reset shall be activated
THIRD PHASE	Negate the DATA OUT (and ENABLE OUT)* to enter RESETSEL1 and attempt communication with a specific slave  * For any attached MM2 slaves	When the DATA OUT signal is negated the reset shall be deactivated. The interface drivers shall be left released until RESETSEL1 is entered. Upon recognition of RESETSEL1 the slave shall re-activate its drivers

TABLE 13

MM SIGNAL LINE ASSIGNMENTS

Line Name	MM1 Usage	MM2 Usage
SELECT OUT (0)	MAINT state (0x0.x1) invokes MM circuits	
SLAVE IN (x)		
MASTER OUT (0)		
SYNC IN (x)		
SYNC OUT (1)		
BUS B (bit 7)	not used	DATA IN (bit 2)
BUS B (bit 6)	not used	CLOCK IN (bit 2)
BUS B (bit 5)	not used	RESPONSE IN (bit 1)
BUS B (bit 4)	not used	DATA IN (bit 1)
BUS B (bit 3)	not used	CLOCK IN (bit 1)
BUS B (bit 2)	not used	RESPONSE IN (bit 0)
BUS B (bit 1)	not used	DATA IN (bit 0)
BUS B (bit 0)	not used	CLOCK IN (bit 0)
BUS B Parity	not used	RESPONSE IN (bit 2)
BUS A (bit 7)	DATA OUT (bit 2)	DATA OUT (bit 2)
BUS A (bit 6)	ENABLE OUT (bit 2)*	ENABLE OUT (bit 2)
BUS A (bit 5)	not used	CLOCK OUT (bit 1)
BUS A (bit 4)	DATA OUT (bit 1)	DATA OUT (bit 1)
BUS A (bit 3)	ENABLE OUT (bit 1)*	ENABLE OUT (bit 1)
BUS A (bit 2)	not used	CLOCK OUT (bit 0)
BUS A (bit 1)	DATA OUT (bit 0)	DATA OUT (bit 0)
BUS A (bit 0)	ENABLE OUT (bit 0)*	ENABLE OUT (bit 0)
BUS A Parity	not used	CLOCK OUT (bit 2)

\* An MM1 Master must use both ENABLE OUT and DATA OUT to reset and release any attached MM2 slaves.

TABLE 14

## MM2 SCENARIO SUMMARY

MAINTENANCE MODE 2	MASTER ACTION	SLAVE ACTION
FIRST PHASE	Enter MAINT state	Upon recognition of MAINT state the MM2 slave shall release the interface drivers and respond to Maintenance Mode orders (selection, reset, etc.)
SECOND PHASE	Activate the DATA OUT and or ENABLE OUT signals and enter IDLE state	If DATA OUT and ENABLE OUT are active when the MAINT state is removed a reset shall be activated and the drivers shall be left released
THIRD PHASE	Deactivate the DATA OUT and ENABLE OUT signals. Optionally enter Selective Reset to attempt communication with a specific slave	When either the DATA OUT or ENABLE OUT signal is dropped the reset shall be deactivated. The interface drivers shall be left released until the RESETSEL1 state is entered or certain selective MM2 orders are issued.

This signal is also used in conjunction with the DATA OUT and ENABLE OUT signals to determine whether or not the subsequent serial data is to be shifted into the MM2 master (Write) or from the MM2 slave (Read). This sequence is described in 5.6.2.4 and is illustrated on the MM2 Timing Chart (see Figure 62).

(3) DATA OUT. The DATA OUT lines are used by the master to transmit serial data to the MM2 deserialization register during the MM2 write sequence. The CLOCK OUT signal is used to clock the data into the deserialization register while the ENABLE OUT signal is active. The data is loaded into the deserialization register regardless of whether or not the MM2 was selected earlier.

The DATA OUT signal, along with the ENABLE OUT signal, is also used at the trailing edge of SYNC OUT to specify that the MM2 slave is to perform the reset and release functions. This enables MM2 circuits to act just like MM1 circuits when intermixed on the same interface, except that ENABLE OUT, as well as DATA OUT, shall be active at the trailing edge of SYNC OUT before drivers are enabled.

#### 5.6.2.3.2 Inbound MM2 Signals

(1) CLOCK IN. The CLOCK IN lines are simply the CLOCK OUT lines returned (after voting) by the selected MM2 circuits. The DATA IN lines shall be stable and may be sampled by the master 250 ns after CLOCK IN is detected at the master, provided that CLOCK OUT also remains asserted.

(2) DATA IN. These lines contain the serial data returned to the master from the MM2 slave during the MM2 read sequence. Normally, this data is a description of detected faults that may prevent normal communications. However, the option is provided for the use of this path to send the master any information that cannot be reliably communicated any other way.

The information transferred on the DATA IN lines shall be specified by a previous order as described in 5.6.2.6.

(3) RESPONSE IN. The master performs a majority vote on the three RESPONSE IN lines to indicate initial MM2 selection. This signal is also used to determine whether or not the FDSR shift has completed. This enables the master to simply deal with differing FDSR lengths.

The use of RESPONSE IN to signal completion of the FDSR shifting is described in 5.6.2.4.5. The use of this signal to indicate successful selection is described in 5.6.2.4.2.

**5.6.2.4 MM2 Write/Read Sequences.** MM2 write data are serially shifted into all MM2 slaves or MM2 read data are shifted from a selected MM2 slave by the CLOCK OUT signal when the ENABLE OUT signal is active. Whether or not the shift is to the MM2 circuits (Write) or from the MM2 circuits (Read) shall be established before the ENABLE OUT signal becomes active. This is done by testing the DATA OUT signal with the CLOCK OUT signal prior to activating ENABLE OUT. If DATA OUT is found to be active, the subsequent shift operation shall be to the MM2 circuits (Write) and, of course, if DATA OUT is inactive when sampled, the subsequent shift shall be from the MM2 slave (Read) (see the MM2 Timing Chart, Figure 62).

**5.6.2.4.1. MM2 Write Sequence.** The MM2 Write sequence provides the master with the capability of transmitting data serially to the MM2 circuits. The initial write sequence shall be received by all MM2 slaves and shall contain the slave address. Subsequent writes shall contain encoded orders for the selected MM2 circuits. However, the write data is not limited to addresses or orders and can be any type of data that may make sense transferring across this fault-tolerant path.

All data, regardless of which MM2 slave it is intended for, shall be shifted into all slaves with MM2 circuits, and at least the last four bits of DATA OUT shall be retained until ENABLE OUT goes inactive.

The last bit of write data shifted to the MM2 circuits, before ENABLE OUT drops, shall specify whether the previous three bits contain an address to be used to select a specific MM2 or an encoded order to a previously selected MM2 slave. The meaning of any additional write data shall be specified by the four required bits as is described in 5.6.2.5.

**5.6.2.4.2 MM2 Selection Sequence.** If, upon interrogating the last bit of serial write data, once ENABLE OUT becomes inactive, an MM2 slave finds the bit active, it shall check whether its address corresponds to the address sent in the previous three bits of write data. The next to the last bit of data shifted to the MM2 circuits shall contain the high-order bit of the slave address. If the address in the deserialization register corresponds to the slave address, the MM2 circuits shall be selected and shall remain so until either:

(1) The MAINT state is removed from the three control out lines, or

(2) A subsequent write sequence specifies that a different MM2 slave has been selected

When the MM2 circuits are selected, RESPONSE IN shall be asserted to signal to the master that the MM2 slave has been selected. The RESPONSE IN lines shall remain active until the master activates the CLOCK OUT lines or drops SYNC OUT. Activating the RESPONSE IN lines when an MM2 initially becomes selected provides the master with a quick way of determining that the MM2 circuits are powered on and capable of carrying on an MM2 dialog.

**5.6.2.4.3 MM2 Order Sequence.** The last bit of serial write data that was shifted to the MM2 slaves underneath MM2 ENABLE OUT may be inactive. If so, an MM2 slave selected by a prior write sequence shall decode and execute the order contained in the previous three bits of write data. The orders are described in 5.6.2.5.

**5.6.2.4.4 MM2 Read Sequence.** The MM2 Read sequence provides the master the capability to extract serial data from a selected MM2 slave. The default data is the contents of the FDSR. The FDSR contains a description of faults that may preclude normal communications. Optionally, this path can be used to send the master any data that makes sense being transferred across this fault-tolerant path, such as wrap data. The source of this data may be set to be something other than the FDSR contents by an optional Set Source/Sink order (see 5.6.2.5).

When the contents of the FDSR are being read, the entire register shall be shifted out. If the sequence is truncated early, the contents of the FDSR cannot be guaranteed the next time the FDSR is accessed.

**5.6.2.4.4.1 Fault Descriptor Shift Register (FDSR) Description.** Whenever a slave's MM2 circuits are selected by the master, all error circuitry that could change the contents of the register containing the basic fault descriptors (FDSR) shall be released. Accessing the contents of the FDSR shall be accomplished by the master initiating an MM2 Read sequence.

Once begun, the MM2 read sequence access should be completed or the FDSR may contain misleading information. The Fault Descriptor Shift Register (FDSR) in each MM2 slave is effectively an extendable shift register. There are a basic number of entries in this shift register that shall be supported. The required entries include the first two bits (0 and 1) and

the last two bits ( $n - 1 = 1$  and  $n = 0$ ) as shown in Table 15. The RESPONSE IN lines shall be asserted when the shift is completed, and released when either ENABLE OUT is negated or MAINT state is deactivated.

The FDSR shall always have a zero placed in bit position  $n$  while shifting so that the entire register will end up reset after completion of the FDSR read sequence. The FDSR is also reset whenever a reset is generated at the trailing edge of SYNC OUT.

The fixed one and zero that are the last FDSR bits shifted out before RESPONSE IN is activated may be used to verify that the FDSR shifted properly.

The FDSR contents during MM2 shall be defined as follows, with Bit 0 being the first bit shifted to the master during a read sequence.

**5.6.2.5 Description of MM2 Orders.** The three-bit encoded orders sent to a selected MM2 slave via the Write sequence shall be as summarized in Table 16 and as detailed in 5.6.2.5.1 through 5.6.2.5.4. Note that certain orders that are issued to the selected MM2 circuits do not take effect until SYNC OUT is negated, e.g., the MM2 reset order. If more than one slave with MM2 circuitry is selected during the MAINT state and are issued such orders, these orders shall be held and performed after SYNC OUT is negated (assuming that all other prerequisites are met).

**5.6.2.5.1 ENABLE DRIVERS Order.** The ENABLE DRIVERS order shall cause the selected slave MM2 circuits to restore the interface drivers after SYNC OUT is negated, if they had been previously released from the interface. The drivers may have been released earlier either by a previous order or after detection of a fault that may prevent normal communication (see 5.7). All the drivers shall be released from the interface whenever MAINT state is active, except those BUS B drivers that must be used during MM2 sequences by the selected MM2 circuits. The ENABLE DRIVERS order shall reset the logic that causes the selected slave's MM2 circuits to continue releasing the drivers after SYNC OUT is negated.

**5.6.2.5.2 DISABLE DRIVERS Order.** The DISABLE DRIVERS order shall cause the selected slave MM2 circuits to continue releasing the drivers after SYNC OUT is negated. The drivers shall remain released until either

(1) An MM2 ENABLE DRIVERS order is received or

**TABLE 15**  
**DESCRIPTION OF MM2 FDSR**

---

Bit	Description
0	Control Out sequence check
1	IPI Bus Out Parity error
2	
3	(optional fault
4	descriptors defined
5	by each slave's
n-2	manufacturer)
n-1	(always a one)
n	clear bit (always a zero)

---

Bit 0=1 - Control Out sequence check indicates the Slave has detected an invalid sequence on the Control Out lines.

Bit 1=1 - IPI Bus Out Parity error indicates the Slave has detected a parity error on BUS A and/or BUS B.



**TABLE 16**  
**ENCODED MM2 ORDERS**

DATA OUT				MM2 ORDER
bits				
n-3	n-2	n-1	n	
0	0	0	*	Enable Drivers
0	0	1	*	Disable Drivers
0	1	0	*	MM2 Reset
0	1	1	*	MM2 Reset and Disable Drivers
1	0	0	*	vendor unique
1	0	1	*	reserved for optional MM2 Data Transfer order
1	1	0	*	reserved for optional Set Source/Sink order
1	1	1	*	reserved for Additional Orders option

\* Bit n is the last bit shifted into the deserialization register before ENABLE OUT is dropped. Bit n - 1 is the next to the last bit of MM2 serial read data sent to the MM2 slave during a Read sequence and so on. Note that Bit n remains inactive in this case to signify that the deserialization register contains an order.

(2) A Selective Reset sequence is issued to the slave

Releasing the drivers shall only affect the drivers when SYNC OUT is negated. The drivers not used for MM2 communications shall always be released while MAINT is active.

**5.6.2.5.3 MM2 RESET Order.** The MM2 RESET order shall result in a reset being issued to the slave when SYNC OUT is negated providing that at that time the ENABLE OUT signal is active and DATA OUT is inactive. The reset shall persist until ENABLE OUT signal becomes inactive.

NOTE: The MM2 RESET order becomes void when ENABLE OUT is not activated at the trailing edge of SYNC OUT.

Other orders may be issued after the MM2 RESET order has been given and before SYNC OUT is negated.

**5.6.2.5.4 MM2 RESET AND DISABLE DRIVERS Order.** The MM2 RESET AND DISABLE DRIVERS order shall perform the same result as would a paired sequence of MM2 RESET followed by a DISABLE DRIVERS order sent separately. This order is provided as a convenience to allow setting the logic that will keep the interface drivers released after SYNC OUT is negated and to generate an MM2 reset with one order.

#### **5.6.2.6 Description of Optional MM2 Orders**

**5.6.2.6.1 MM2 DATA TRANSFER Order.** This order indicates that the write sequence was intended to move data (exclusive of Bits  $n$  through  $n - 3$ ) to an alternate destination within the MM2 circuits set up by a prior SET SOURCE/SINK order. No other action shall be performed.

**5.6.2.6.2 SET SOURCE/SINK Order.** The SET SOURCE/ SINK order specifies alternate sources of read data or alternate destinations of write data within the MM2 circuits.

This order shall allow for extending the MM2 circuits to transfer any serial data that cannot be reliably sent any other way to or from the MM2 circuits. The default source for read data is the FDSR. The SET SOURCE/SINK order only applies to the subsequent Read or Write sequence.

For example, the Source/Sink for a subsequent Read/Write sequence may be specified by additional deserialization register bits implemented as Vendor Unique (i.e., beyond the four required bits).

**5.6.2.6.3 Additional Orders.** This order indicates that the additional write data bits

beyond the four required bits shall be regarded as additional MM2 vendor unique orders.

For example, additions might be for power control of remote equipment cabinets or loading and reading back any diagnostic data within the slave.

**5.7 Other Maintenance Considerations.** The MM circuits may release the slave's drivers from the interface outside of MAINT if a fault is detected by the slave which may prevent normal communications. Once the master recognizes that a slave has isolated itself from the interface, it may attempt to restore communications via the Selective Reset sequence or via selective orders if MM2 is supported. If the problem persists, the slave may be left isolated from the interface until repairs can be made. If the slave that isolated itself from the interface supports MM2, it may be possible to obtain a description of the fault, before attempting to restore normal communication, by using the MM2 sequences described in 5.6.2.

NOTE: If the MM circuits release the slave's drivers from the interface, undefined states may result. When the Selective Reset sequence is initiated to restore the slave, the normal response to the Selective Reset state shall be delayed until the drivers are restored.

Multiported slaves shall react to the Maintenance Mode considerations on the port over which the MAINT state was recognized. The slave shall not induce error conditions on the other ports that are attached to the slave. However, during Maintenance Mode, the slave may be dedicated to the port initiating the reset, and may be Busy to all others.

## **6. Logical Interface Environment**

**6.1 General.** The IPI operates in a layered environment. The Logical Interface uses the Physical Interface to transfer information between the master and the slave.

Logical Interface operates independently of the Physical Interface (except as noted in the 5.5, Bus Octet Definitions), and consists of a repertoire of Operation Commands and Operation Responses that control various types of slaves and facilities.

Variations possible within the command definitions of the Logical Interface include



TABLE 17

LEVEL CHARACTERISTICS

	DATA SPACE	ACCESS TIMING	DATA ADDRESS	CONTROL COMMAND	BLOCK LENGTH	DATA TYPE	OTHER CHARACT
LEVEL 2	facility defined	dependent independ	physical	device	static	raw	
LEVEL 3	facility defined	independ dependent	logical	facility	static	raw perfect	
LEVEL 4	facility independ	independ	logical	data	static	raw perfect	
LEVELS ABOVE	data dependent	independ	record, field	record, field	dynamic	perfect	file-name

The Logical Interface represents all the levels above the Physical Interface; Level 2 will be described in ANSI X3.130 and Level 3 will be described ANSI X3.132. Other levels have been established that incorporate different degrees of functionality and intelligence.

All of the levels offer a migration path from one environment to another. Multiple logical levels may coexist on the same Physical Interface, but only one may be active at any one instant.

Table 17 summarizes the characteristics of the logical levels.

**6.2.1 Level 2 - Device Specific.** Level 2 is oriented to devices and is not covered in this document (see ANSI X3.130, when available). The master shall be aware of the unique attributes of the device under its control. Some of the characteristics that define Level 2 are:

- (1) Operations are executed with the use of encoded commands imbedded in the Bus Control of Bus Exchanges at the Physical Interface.
- (2) The data area is defined by device addressability to the media.
- (3) The Transfer of data may or may not be timing critical, and typically is unbuffered.
- (4) Data is addressed by the PhysicalBlock address.

(5) Data typically is transferred as "raw," i.e., as read from the device with no correction of errors (if any).

(6) The commands are device unique.

(7) PhysicalBlock lengths may or may not be fixed over the addressable media.

(8) Positioning is requested explicitly, but may also be implicit.

**6.2.2 Level 3 - Device Generic.** Level 3 is oriented to the generic components of devices (disk, tape, printer, and the like), and typically not the device-unique components (e.g., cylinders, heads). Level 3 uses a packet structure that provides independence of the command repertoire from the Physical Interface. Some of the Level 3 characteristics are:

- (1) Operations may be Individual or Queued.
- (2) The data area is defined by the facility addressability to the media.
- (3) The Transfer of data may or may not be timing critical, and typically is buffered.
- (4) Data is addressed by DataBlock address, but PhysicalBlock addresses may also be used.
- (5) DataBlock lengths typically are fixed over an addressable data area, and can vary between different addressable areas on the media as well as varying between medias.

(6) Data is normally requested as "perfect" (data errors, if any, corrected), or may be requested as "raw" (data errors, if any, not corrected).

(7) Positioning is requested implicitly, but may be explicit.

(8) Media defect handling is transparent to the master, but may be managed by the master.

(9) Error correction is transparent to the master, but may be managed by the master.

(10) Error retry is transparent to the master, but may be managed by the master.

**6.2.3 Level 4 - Data Specific.** Level 4 concepts are oriented to the characteristics of data and its attributes (e.g., random or sequential, input or output). The characteristics defined in the following list are neither complete nor exclusive. They are shown here to provide some perspective on what extensions in functionality and intelligence are envisaged as being appropriate at Level 4.

(1) Operations may be Individual or Queued.

(2) Logical slaves make the data area both slave independent and facility independent.

(3) Logical volumes make the addressing structure device independent.

(4) Buffers are used to gain access to data.

(5) Data availability can be controlled by the Mount/Dismount of volumes.

(6) DataBlock sizes are fixed within a volume.

(7) Data is normally requested as "perfect" (data errors, if any, corrected), but may be requested as "raw" (data errors, if any, not corrected).

(8) The master does not participate in defect management, error retry, or error correction.

**6.2.4 Level 5 and Above.** These levels are expected to embody concepts that require file structures and file organization be imbedded in the slave. The characteristics defined in the following list are neither complete nor exclusive. They are shown here to provide some perspective on what extensions in functionality and intelligence are envisaged as being appropriate at the upper levels.

(1) Operations may be Individual or Queued.

(2) The data area is data dependent, i.e., files.

(3) Availability of data is timing independent, e.g., Open/Close File.

(4) Addressing of data is at the level of the application, e.g., records or fields.

(5) Data lengths may vary within a volume (variable length records).

(6) Only perfect data is available, i.e., no errors.

(7) Data location is by implicit addresses, e.g., Filename.

## 7. Timing

**7.1 Terms.** The master shall provide for cable deskewing for all signals originating from the master. The slave shall provide for cable deskewing for all signals originating in the slave. The following terms are used in place of actual numbers so that timing may be determined separately for different slaves and their supported cable types.

**SDE (Slave-Dependent Exchange).** This term, the value of which is supplied by the slave manufacturer, specifies both the maximum BUS B setup time and the maximum response delay for the slave during a Bus Exchange when the slave is functioning properly.

**SYD (System Dependent).** This term, the value of which is supplied by the slave manufacturer, specifies the time the master shall wait during a Bus Exchange until it can conclude that the slave is not functioning properly. This value should be used by the master as a time-out for interlocked slave responses during a Bus Exchange.

**IRT (Interrupt Response Time).** This term, the value of which is supplied by the slave manufacturer, specifies the maximum slave response time to a Request Interrupts Sequence.

**SDR (Slave Dependent-Reset).** This term, the value of which is supplied by the slave manufacturer, specifies the maximum time the master shall wait for the slave to recover from a reset sequence (which may include a reset of the slave microprocessor if specified by Bits 0 — 3 of the Selective Reset octet).

**CCD (Cable Configuration Dependent).** This term, the value of which is limited by the electrical class, is defined in Table 2. It is used to establish minimum values such as set-up times and pulse widths as shown in the timing diagrams. The actual CCD value shall be defined by an individual product. The actual value shall

be determined by the product's implementation, and shall define the minimum timings (maximum rates) that can be utilized.

**CMX (Maximum Cable Propagation Delay).** This term specifies the cable propagation delay based on the maximum length of cable in the configuration in which this interface is used.

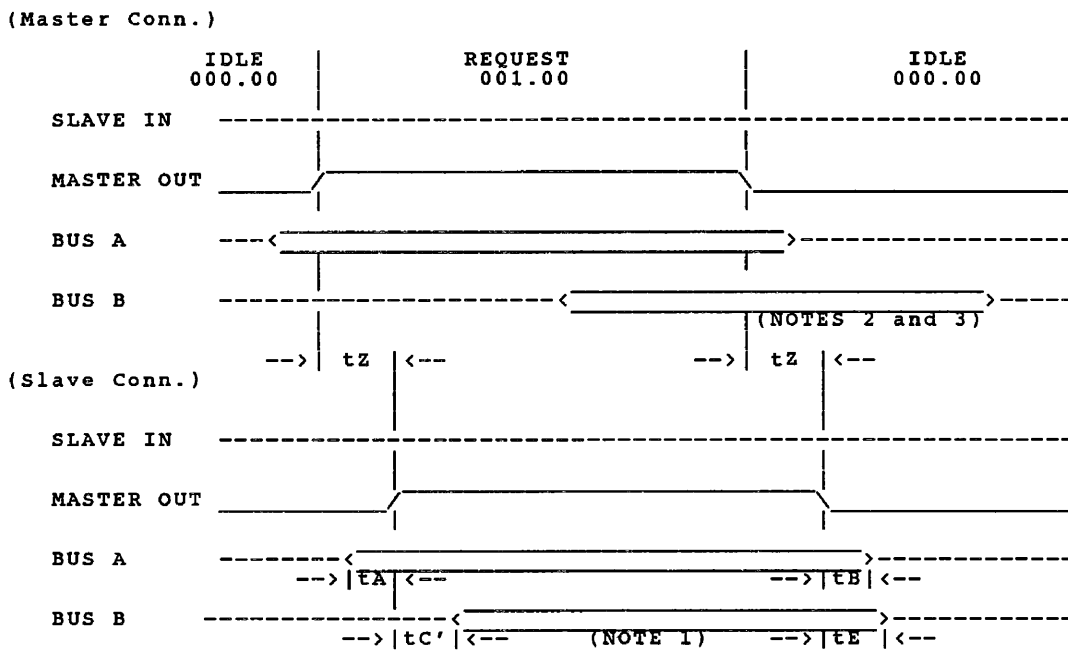
**7.2 Data Streaming SYNC OUT Pulse Width.** When the slave is executing transfers that cannot be throttled, e.g., direct data transmittal between the master and a disc drive, the values 1.1(tH), tH' Max, and tY' Min and Max shall be applicable.

The value of tH' shall always be met by the master.

See Figures 57 through 60.

**7.3. Symbols.** Certain symbols are used in the timing diagrams. These symbols and their respective definitions shall be as shown in the following table.

&	- Abbreviated state notation, e.g., 7.2 = 111.10
/ or \	- Signal transition
< or >	- Bus transition
-----	- Released
XXXXXX	- Undefined but not necessarily released
.....	- The bus may or may not be driven



SELECT OUT, SYNC OUT = Inactive  
(Master and Slave Conn.)

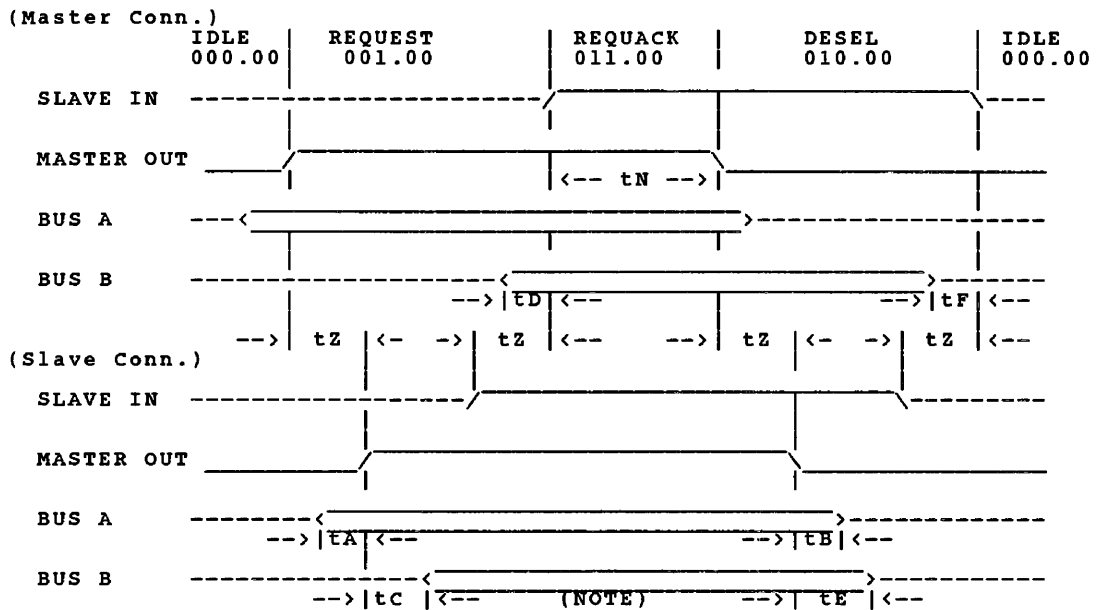
SYNC IN = Released  
(Master and Slave Conn.)  
Label Description

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.
tB	Master bus release from MASTER OUT	0.025	-	usecs.
tC'	Slave Interrupt Response Delay	0	IRT	usecs.
tE	Slave bus release	0	SDE	usecs.
tZ	Cable delay	0	CMX	usecs.

NOTES:

- (1) The slave sets only the line corresponding to its bit-significant address.
- (2) The master receives valid interrupts only for the bit positions corresponding to the responding slaves on the bus.
- (3) The response of the slaves is not synchronous, and the master shall wait a time equal to that of the slowest, furthest, or slowest and furthest slave to respond before latching or sampling BUS B. In addition, the master shall wait for a time equal to that of the slowest, furthest, or slowest and furthest slave to detect the IDLE state, and release its bit-significant address on BUS B, before starting another sequence.

FIGURE 44  
REQUEST INTERRUPTS SEQUENCE



SELECT OUT, SYNC OUT = Inactive  
(Master and Slave Conn.)

SYNC IN = Released  
(Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.
tB	Master bus release from MASTER OUT	0.025	-	usecs.
tC	Slave turnaround	0	SDE	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.
tE	Slave bus release	0	SDE	usecs.
tF	Slave bus release set-up	0.025	SDE	usecs.
tN	Master interlock delay	0	-	usecs.
tZ	Cable delay	0	CMX	usecs.

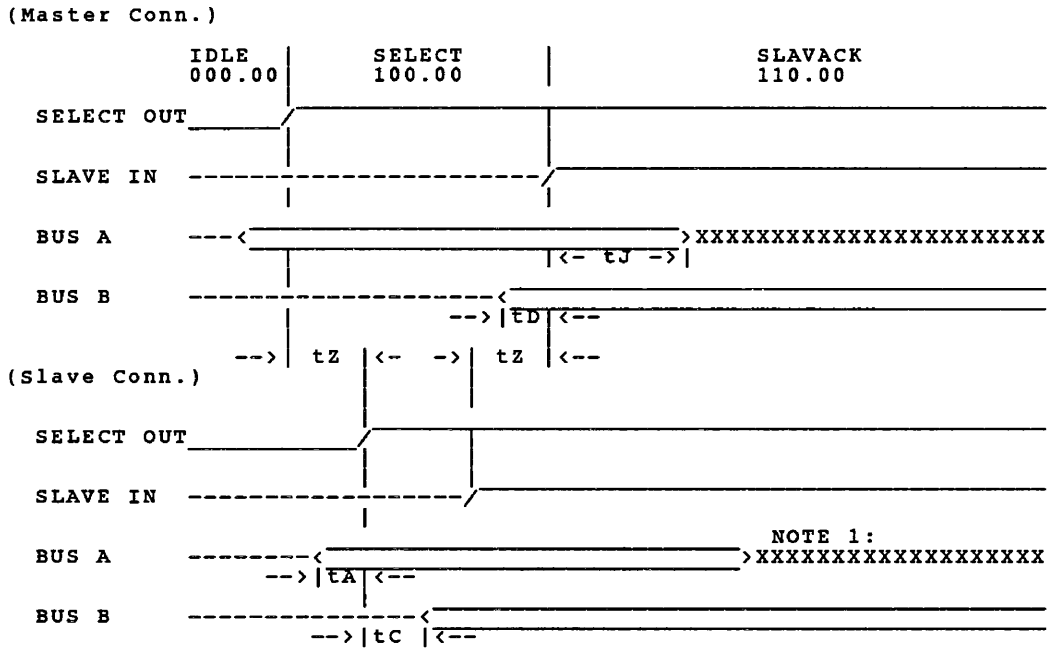
NOTES:

- (1) For a Request Transfer Settings sequence, the addressed slave sets its Transfer Settings octet on BUS B.
- (2) For a Request Facility Interrupts sequence, the addressed slave sets only the lines corresponding to the facilities under its control requesting attention, subject to the Request Modifier on BUS A. Note that the contents of BUS B may change after the assertion of SLAVE IN due to interrupts changing dynamically at the facilities.
- (3) For a Request Slave Interrupts sequence, the addressed slave sets its Slave Interrupts octet on BUS B. Note that the contents of BUS B may change after the assertion of SLAVE IN due to interrupts changing dynamically at the slave.

FIGURE 45

REQUEST TRANSFER SETTINGS/SLAVE INTERRUPTS (Optional)/  
FACILITY INTERRUPTS (Optional) SEQUENCE





(Slave Conn.)

NOTE 1:

MASTER OUT, SYNC OUT = Inactive  
(Master and Slave Conn.)

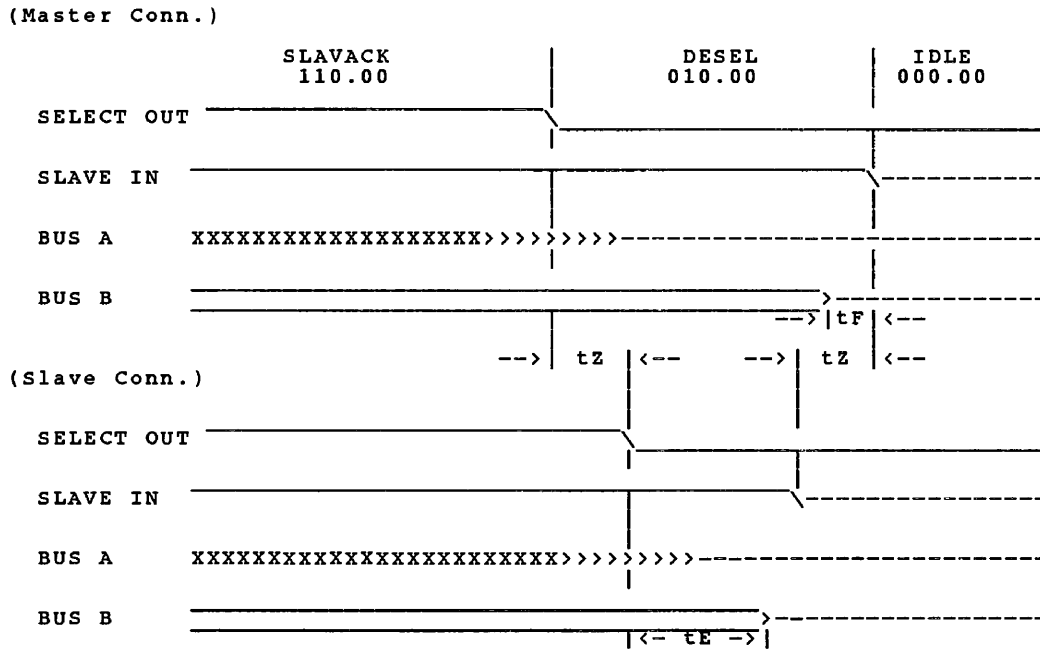
SYNC IN = Released  
(Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.
tC	Slave turnaround	0	SDE	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.
tJ	Master bus hold	0	-	usecs.
tZ	Cable delay	0	CMX	usecs.

NOTES:

(1) When Slave-to-Slave Information Transfers are supported, the maximum  $t_J$  should not exceed 1 usec.

**FIGURE 46**  
**SELECTION SEQUENCE**



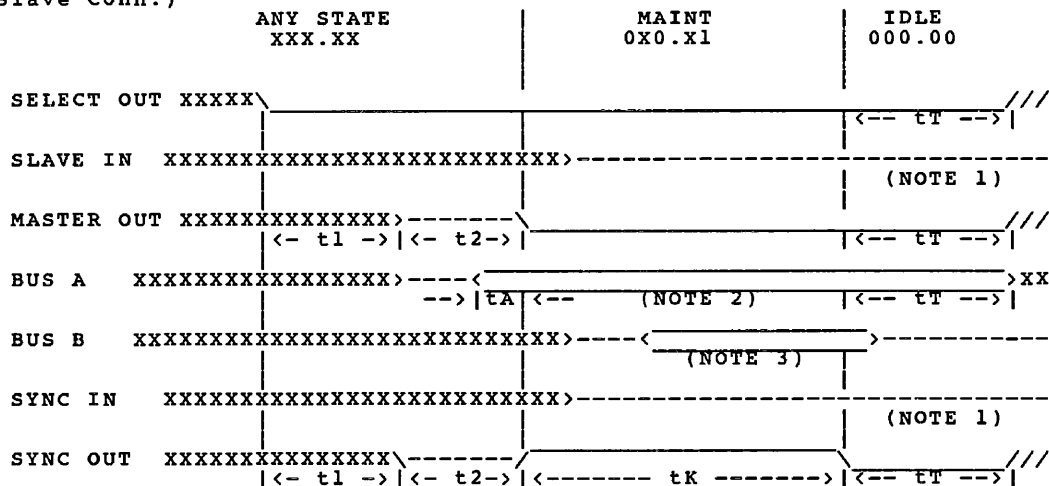
MASTER OUT, SYNC OUT = Inactive (Master and Slave Conn.)

SYNC IN = Released (Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tE	Slave bus release	0	SDE	usecs.
tF	Slave bus release set-up	0.025	SDE	usecs.
tZ	Cable delay	0	CMX	usecs.

**FIGURE 47**  
**NORMAL DESELECTION SEQUENCE**

(Slave Conn.)

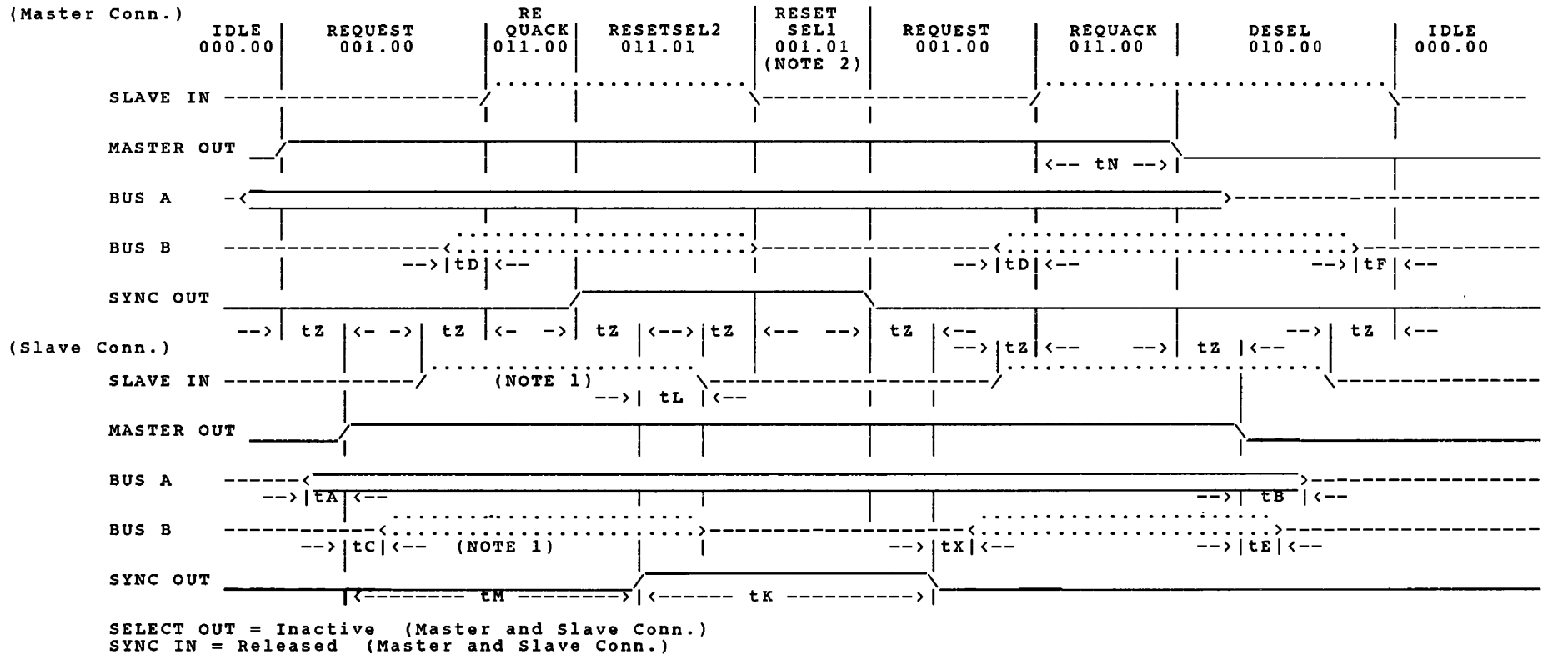


Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.
tK	SYNC OUT pulse width for MAINT (see NOTE 4)	10	-	usecs.
tT	IDLE following MAINT (see NOTE 5)	6	-	usecs.
t1	Dominant Slave MASTER OUT, SYNC OUT and BUS A release from SELECT OUT negation (see NOTE 6)	0	1	usecs.
t2	Master SYNC OUT assertion, MASTER OUT negation from MASTER OUT, SYNC OUT release (see NOTE 6)	1	-	usecs.

NOTES:

- (1) Signal In lines may or may not be released after MAINT (see 5.6).
- (2) BUS A is used for maintenance actions (see 5.6).
- (3) BUS B is optionally used for maintenance actions (see 5.6).
- (4) The slave shall not enter Maintenance Mode until the MAINT state has been active for at least 2 microseconds.
- (5) The slave shall not reset until IDLE has been active after MAINT for at least 2 microseconds.
- (6) If there are no slaves on the cable that implement slave-to-slave information transfers, the master shall hold all control Out signals inactive for a period of at least 1 microsecond (t2) before asserting SYNC OUT to enter the MAINT state.

**FIGURE 48**  
**MASTER RESET SEQUENCE**



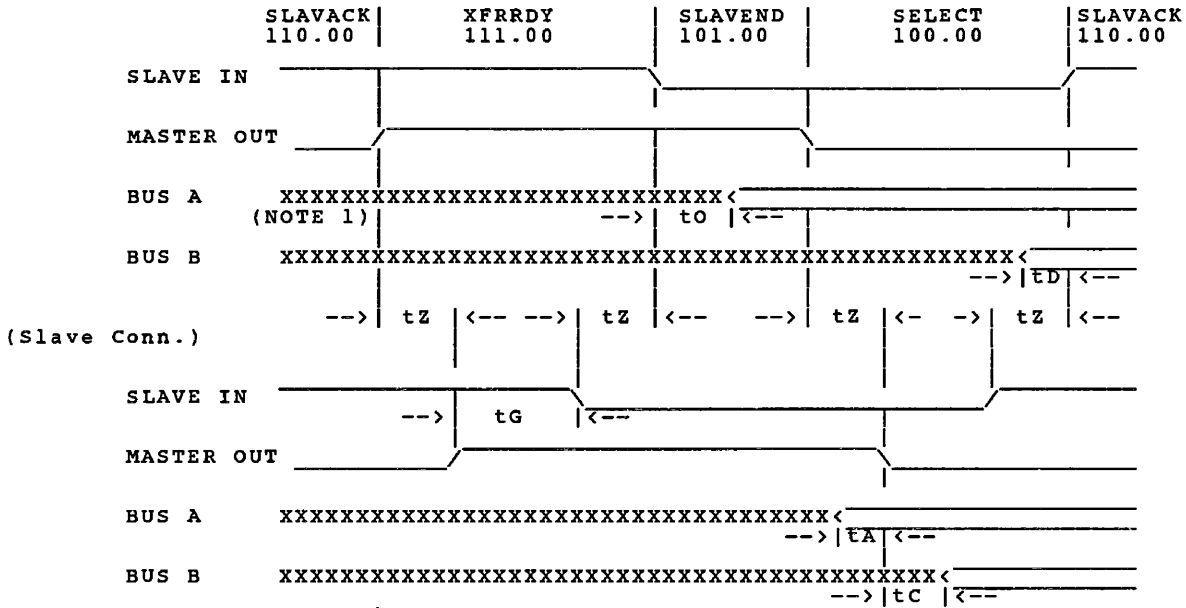
Label	Description	Min.	Max.	Units	Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.	tK	SYNC OUT pulse width for reset	10	-	usecs.
tB	Master bus release from MASTER OUT	0.025	-	usecs.	tL	Slave reset response	0	SDE	usecs.
tC	Slave turnaround	0	SDE	usecs.	tM	MASTER OUT to SYNC OUT set-up	SDE	-	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.	tN	Master interlock delay	0	-	usecs.
tE	Slave bus release	0	SDE	usecs.	tX	Slave reset delay	0	SDR	usecs.
tF	Slave bus release set-up	0.25	SDE	usecs.	tZ	Cable delay	0	CMX	usecs.

## NOTES:

- (1) Slave may or may not respond at this point, e.g., a slave that does not support Request Facilities Interrupts.  
 (2) The slave shall not reset unless the RESESEL1 state has been active for at least 2 microseconds.

FIGURE 49  
 SELECTIVE RESET SEQUENCE

(Master Conn.)



SELECT OUT = Active  
(Master and Slave Conn.)

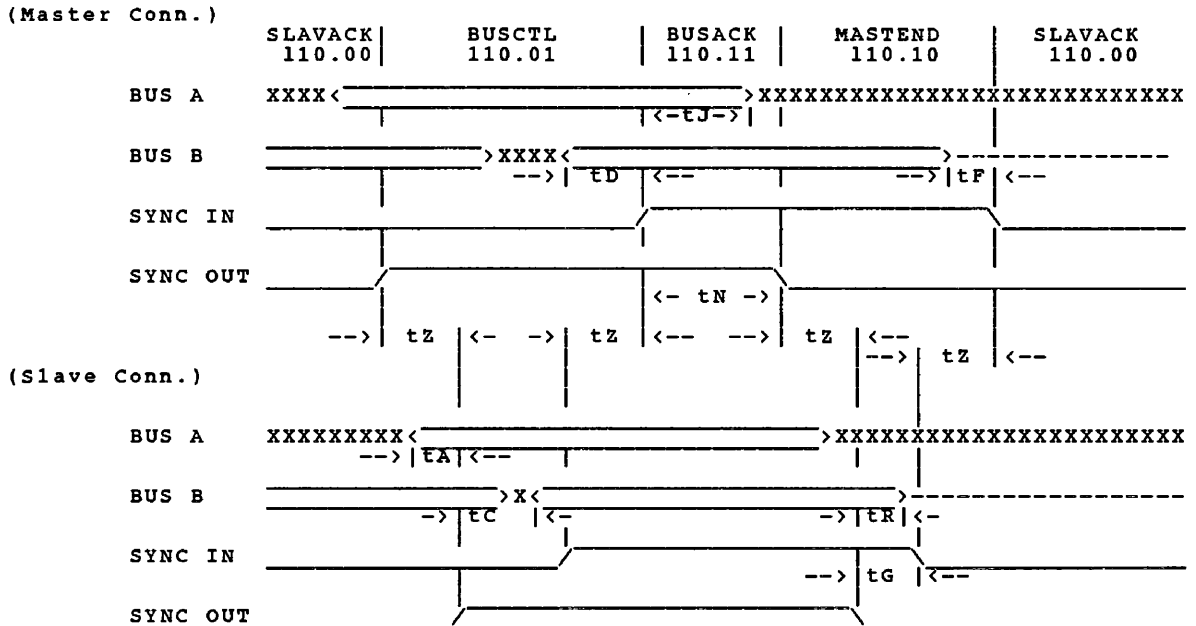
SYNC IN, SYNC OUT = Inactive  
(Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.
tC	Slave turnaround	0	SDE	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.
tG	Slave interlock delay	0	SDE	usecs.
tO	Master turnaround	0	-	usecs.
tZ	Cable delay	0	CMX	usecs.

NOTES:

- (1) For DOM transfers In, BUS A shall be released before the XFRRDY state is entered (see Figure 53).
- (2) This sequence is used if an unrecognizable Bus Control Octet is received at the slave (possibly due to a parity error).
- (3) This sequence is used if there is no required Information Transfer during a Bus Exchange.

FIGURE 50  
SLAVE END WITHOUT INFORMATION TRANSFER SEQUENCE



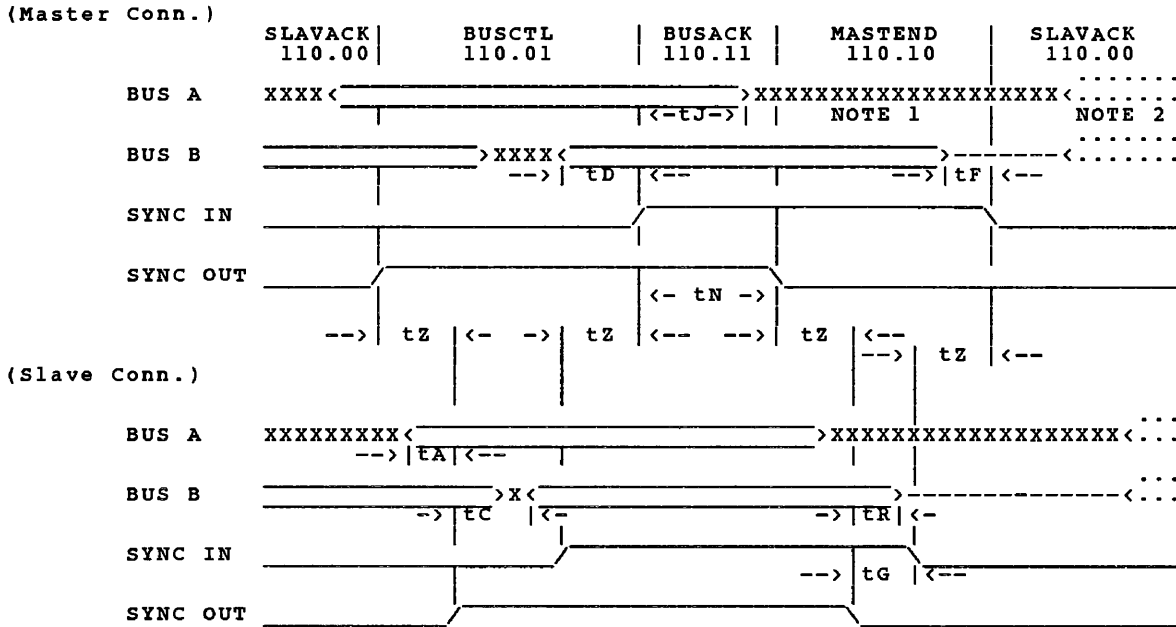
SELECT OUT, SLAVE IN = Active (Master and Slave Conn.)

MASTER OUT = Inactive (Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.
tC	Slave turnaround	0	SDE	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.
tF	Slave bus release set-up	0.025	SDE	usecs.
tG	Slave interlock delay	0	SDE	usecs.
tJ	Master bus hold	0	-	usecs.
tN	Master interlock delay	0	-	usecs.
tR	Slave bus hold	0	-	usecs.
tZ	Cable delay	0	CMX	usecs.

FIGURE 51

BUS CONTROL SEQUENCE (Preceding Transfers In)



SELECT OUT, SLAVE IN = Active (Master and Slave Conn.)

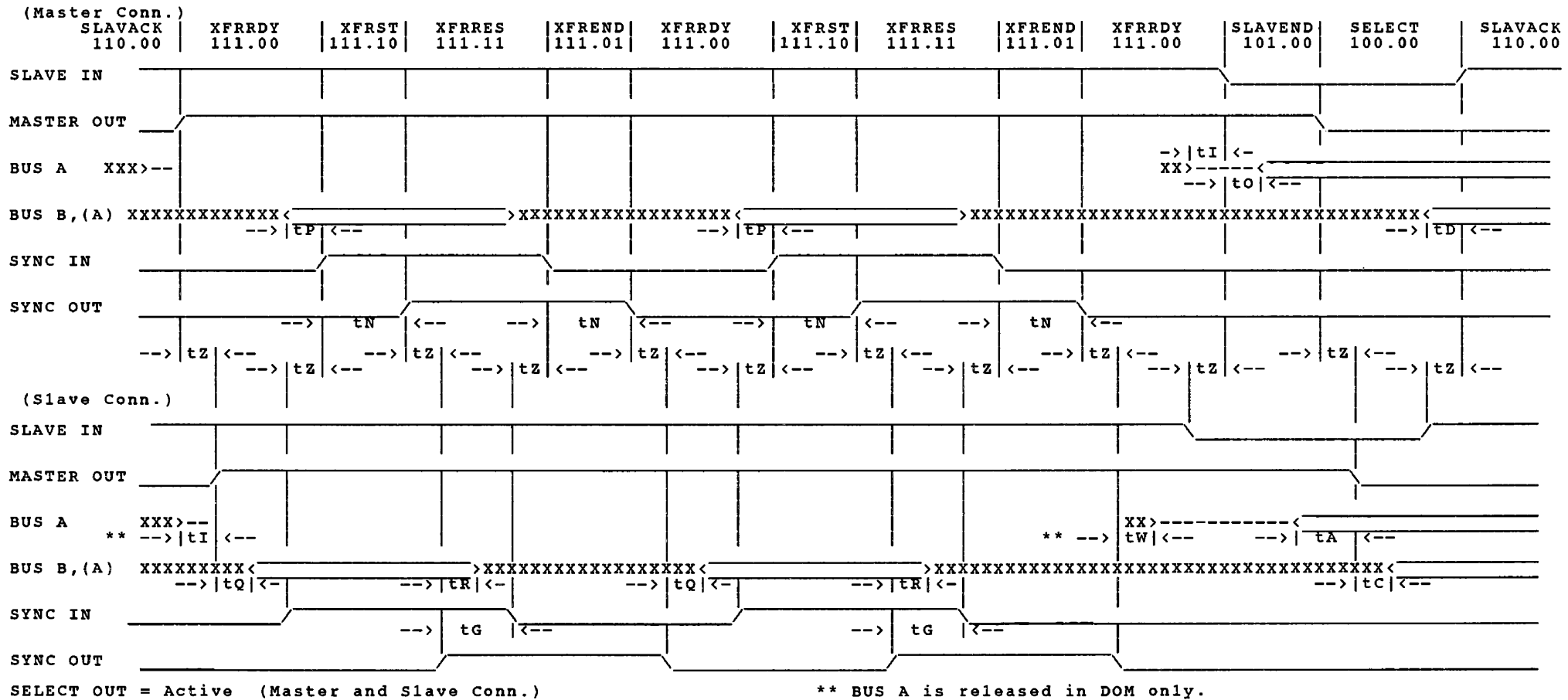
MASTER OUT = Inactive (Master and Slave Conn.)

Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.
tC	Slave turnaround	0	SDE	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.
tF	Slave bus release set-up	0.025	SDE	usecs.
tG	Slave interlock delay	0	SDE	usecs.
tJ	Master bus hold	0	-	usecs.
tN	Master interlock delay	0	-	usecs.
tR	Slave bus hold	0	-	usecs.
tZ	Cable delay	0	CMX	usecs.

NOTES:

- (1) The Slave shall release BUS B prior to entry to the SLAVACK state so that a Master implementation that wraps SYNC IN to produce SYNC OUT may meet the setup time requirements for the first SYNC IN pulse during DOM streaming.
- (2) The master may or may not be driving the buses.

FIGURE 52  
BUS CONTROL SEQUENCE (Preceding Transfer Out)

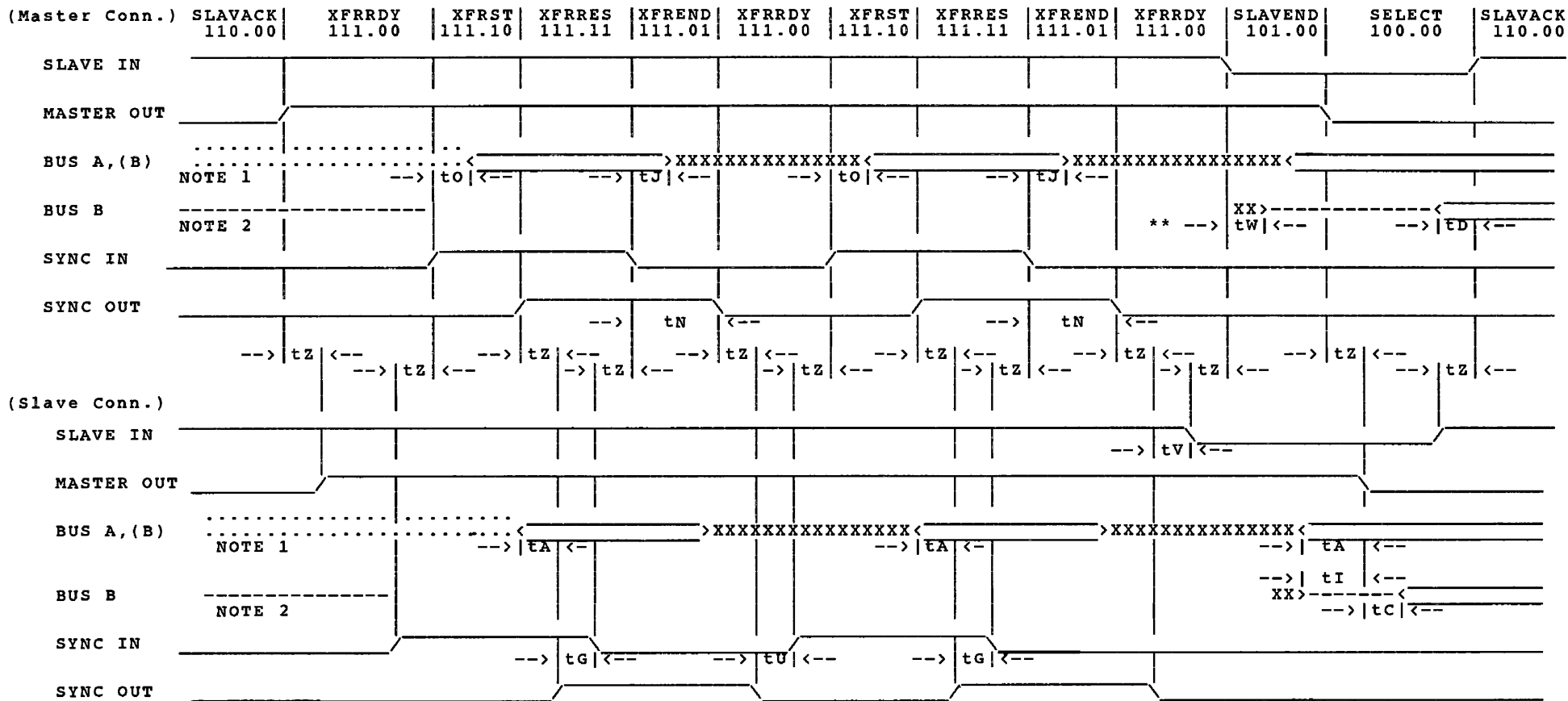


Label	Description	Min.	Max.	Units	Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.	tC	Slave turnaround	0	SDE	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.	tG	Slave interlock delay	0	SDE	usecs.
tI	Bus release set-up	0.025	-	usecs.	tN	Master interlock delay	0	-	usecs.
tO	Master turnaround	0	-	usecs.	tP	Slave data set-up	0.025	-	usecs.
tQ	Slave data turnaround	0	-	usecs.	tR	Slave bus hold	0	-	usecs.
tW	Transfer Bus Release	0	-	usecs.	tZ	Cable delay	0	CMX	usecs.

FIGURE 53

INTERLOCKED INPUT SEQUENCE - SLAVE END





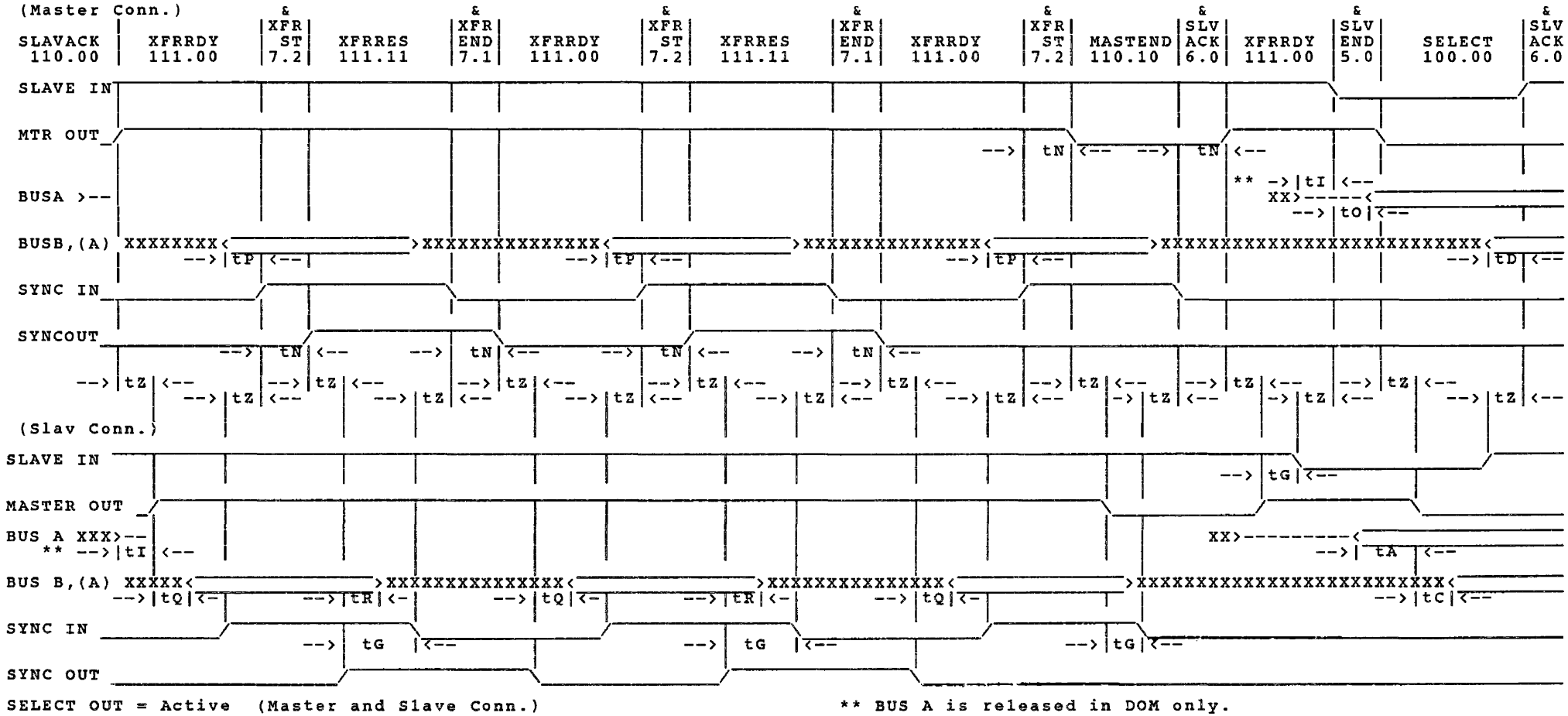
SELECT OUT = Active (Master and Slave Conn.)

Label	Description	Min.	Max.	Units	Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.	tC	Slave turnaround	0	SDE	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.	tG	Slave interlock delay	0	SDE	usecs.
tI	Bus release set-up	0.025	-	usecs.	tJ	Master bus hold	0	-	usecs.
tN	Master interlock delay	0	-	usecs.	tO	Master turnaround	0	-	usecs.
tU	Slave SYNC IN delay	0	-	usecs.	tV	Slave end delay	0	-	usecs.
tW	Transfer bus release	0	-	usecs.	tZ	Cable delay	0	CMX	usecs.

NOTES:

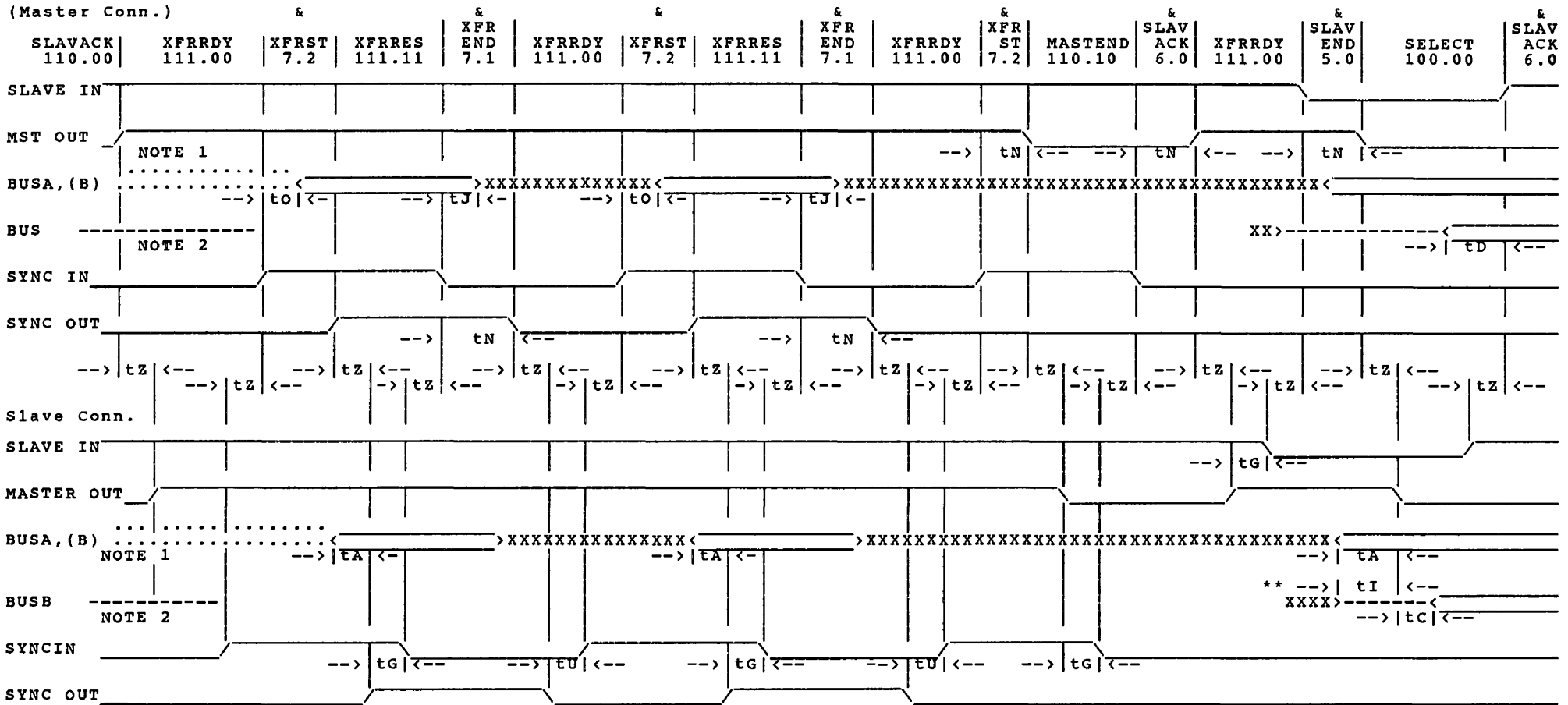
- (1) The master may or may not be driving the buses.
- (2) This represents the slave's drivers in DOM only.

FIGURE 54  
INTERLOCKED OUTPUT SEQUENCE - SLAVE END



Label	Description	Min.	Max.	Units	Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.	tC	Slave turnaround	0	SDE	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.	tG	Slave interlock delay	0	SDE	usecs.
tI	Bus release set-up	0.025	-	usecs.	tN	Master interlock delay	0	-	usecs.
tO	Master turnaround	0	-	usecs.	tP	Slave data set-up	0.025	-	usecs.
tQ	Slave data turnaround	0	-	usecs.	tR	Slave bus hold	0	-	usecs.
tZ	Cable delay	0	CMX	usecs.					

FIGURE 55  
INTERLOCKED INPUT SEQUENCE - MASTER END



SELECT OUT = Active (Master and Slave Conn.)

Label	Description	Min.	Max.	Units	Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.	tC	Slave turnaround	0	SDE	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.	tG	Slave interlock delay	0	SDE	usecs.
tI	Bus release set-up	0.025	-	usecs.	tJ	Master bus hold	0	-	usecs.
tN	Master interlock delay	0	-	usecs.	tO	Master turnaround	0	-	usecs.
tU	Slave SYNC IN delay	0	-	usecs.	tW	Transfer bus release	0	-	usecs.
tZ	Cable delay	0	CMX	usecs.					

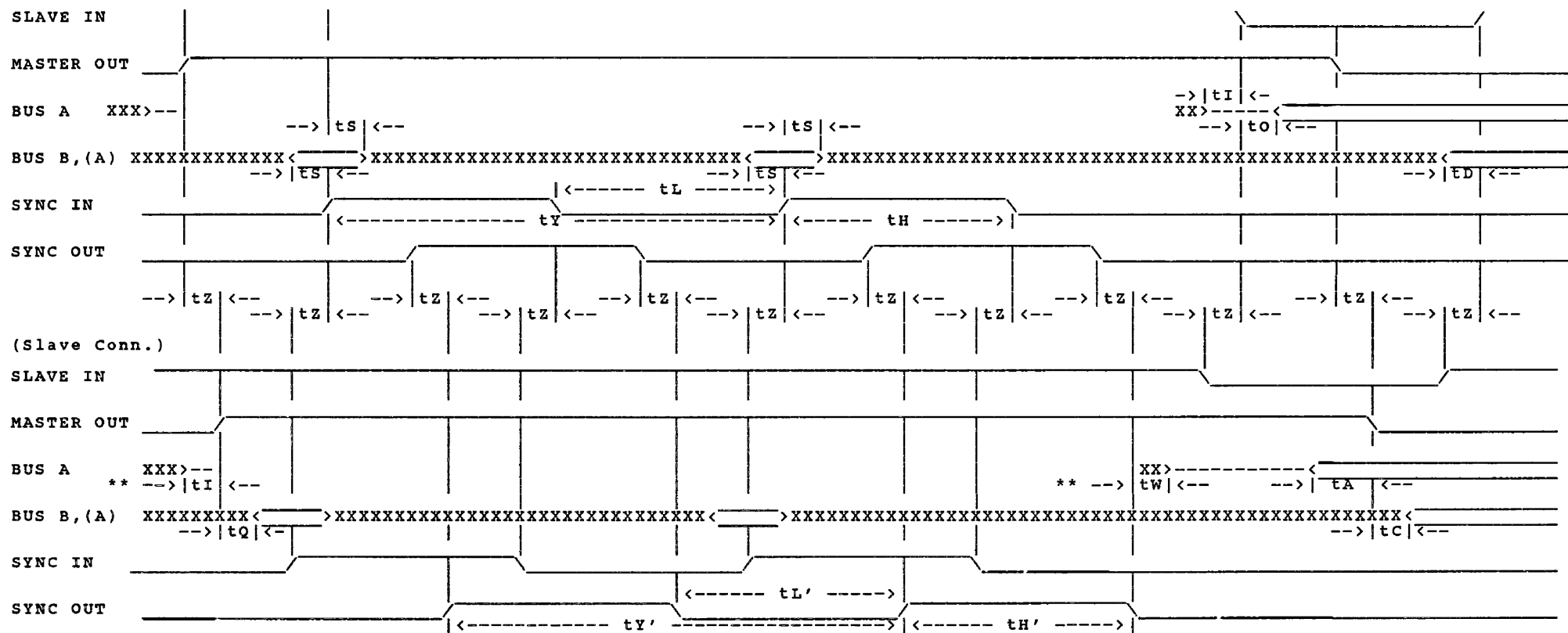
NOTES:

- (1) The master may or may not be driving the buses.
- (2) This represents the slave's drivers in DOM only.

FIGURE 56

INTERLOCKED OUTPUT SEQUENCE - MASTER END

SLAVACK | XFRRDY | | SELECT | SLAVACK  
 110.00 | 111.00 | | STATE SEQUENCES NOT VALID | 100.00 | 110.00



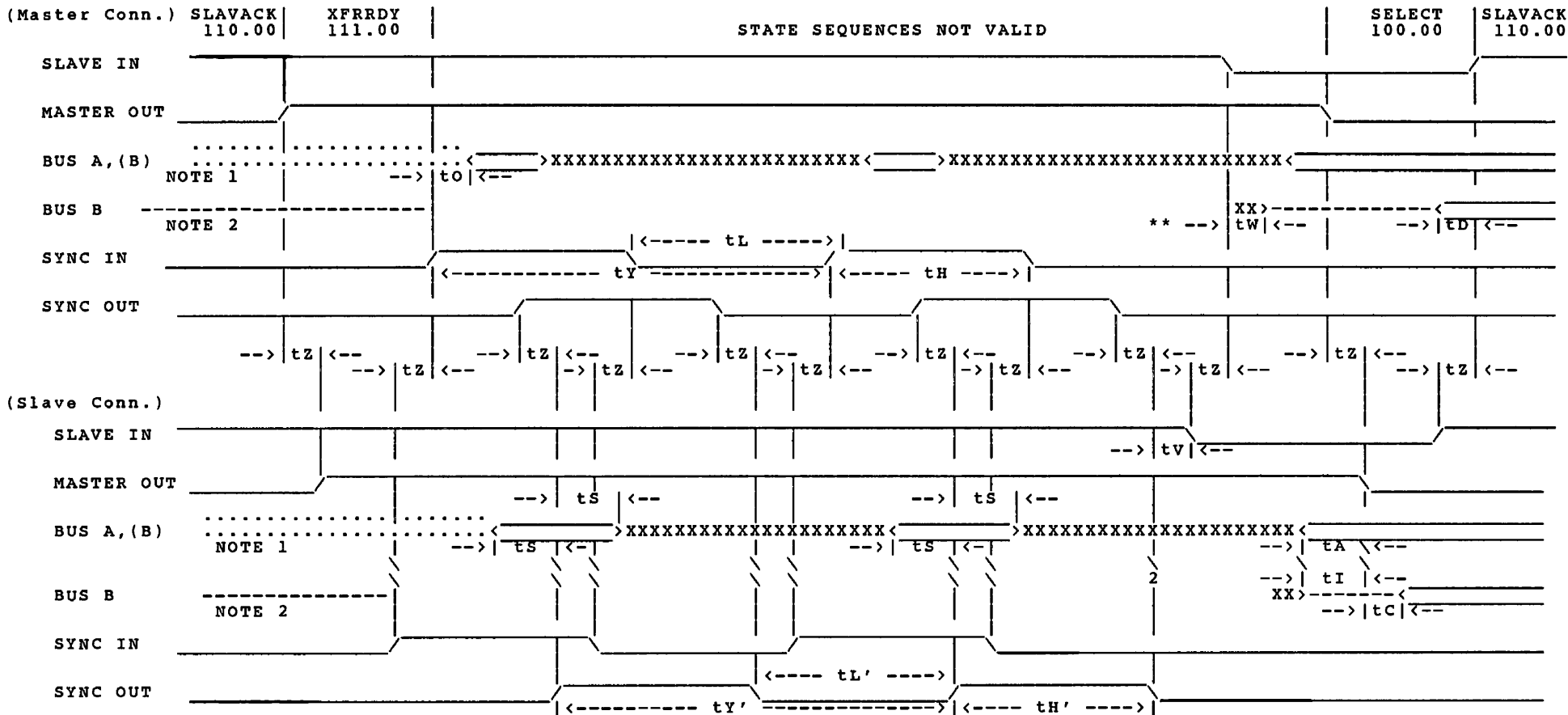
SELECT OUT = Active (Master and Slave Conn.)

\*\* BUS A is released in DOM only.

Label	Description	Min.	Max.	Units	Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.	tO	Master turnaround	0	-	usecs.
tC	Slave turnaround	0	SDE	usecs.	tQ	Slave data turnaround	0	-	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.	tS	Stream. set-up/hold	0.030	-	usecs.
tH	SYNC IN pulse active	0.4*(CCD)	-	usecs.	tW	Transfer bus release	0	-	usecs.
tH'	SYNC OUT pulse active	0.32*(CCD)	-	usecs.	tY	SYNC IN period	CCD	-	usecs.
tI	Bus release set-up	0.025	-	usecs.	tY'	SYNC OUT period	CCD	-	usecs.
tL	SYNC IN pulse inactive	0.4*(CCD)	-	usecs.	tZ	Cable delay	0	CMX	usecs.
tL'	SYNC OUT pulse inactive	0.32*(CCD)	-	usecs.					

FIGURE 57

DATA STREAMING INPUT SEQUENCE - SLAVE END



SELECT OUT = Active (Master and Slave Conn.)

Label	Description	Min.	Max.	Units	Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.	tO	Master turnaround	0	-	usecs.
tC	Slave turnaround	0	SDE	usecs.	tS	Streaming set-up/hold	0.030	-	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.	tV	Slave end delay	0	-	usecs.
tH	SYNC IN pulse active	0.4*(CCD)	-	usecs.	tW	Transfer bus release	0	-	usecs.
tH'	SYNC OUT pulse active	0.32*(CCD)	-	usecs.	tY	SYNC IN period	CCD	-	usecs.
tI	Bus release set-up	0.025	-	usecs.	tY'	SYNC OUT period	CCD	-	usecs.
tL	SYNC IN pulse inactive	0.4*(CCD)	-	usecs.	tZ	Cable delay	0	CMX	usecs.
tL'	SYNC OUT pulse inactive	0.32*(CCD)	-	usecs.					

NOTES:

- (1) The master may or may not be driving the buses.
- (2) This represents the slave's drivers in DOM only.

FIGURE 58

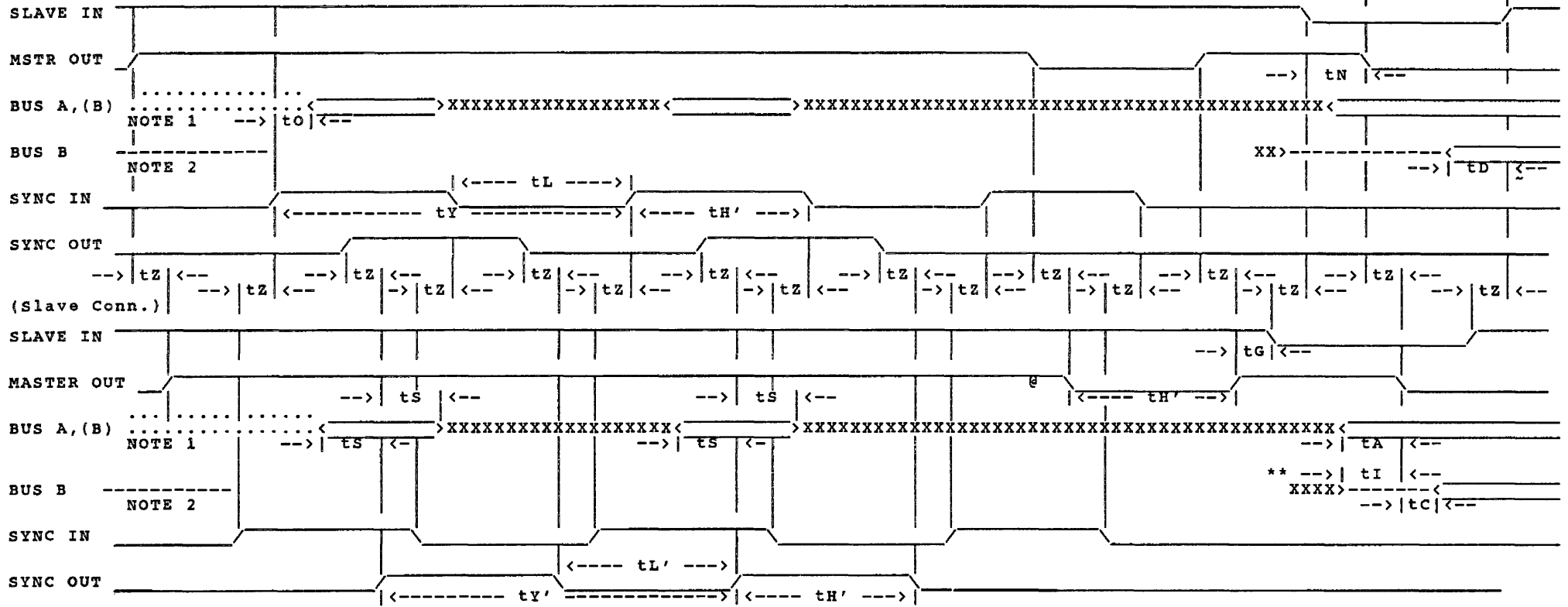
DATA STREAMING OUTPUT SEQUENCE - SLAVE END



(Master Conn.)  
 SLAVACK | XFRRDY  
 110.00 | 111.00

STATE SEQUENCES NOT VALID

SELECT | SLAV  
 100.00 | ACK  
 6.0

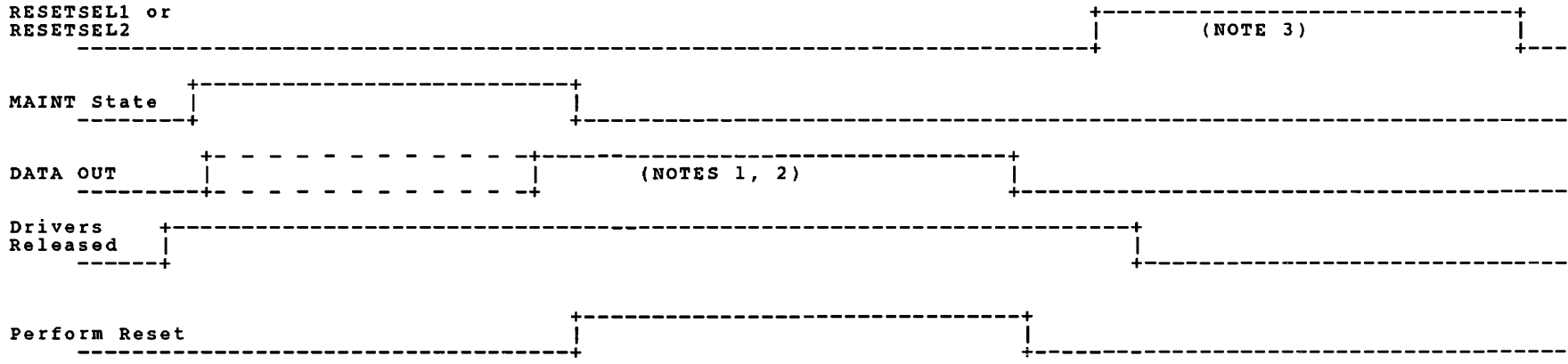


SELECT OUT = Active (Master and Slave Conn.) \*\* BUS B released in DOM only @ The slave does not latch the bus contents here.

Label	Description	Min.	Max.	Units	Label	Description	Min.	Max.	Units
tA	Master bus set-up	0.025	-	usecs.	tL'	SYNC OUT pulse inactive	0.32	-	usecs.
tC	Slave turnaround	0	SDE	usecs.	tN	Master interlock delay	0	-	usecs.
tD	Slave bus set-up	0.025	SDE	usecs.	tO	Master turnaround	0	-	usecs.
tG	Slave interlock delay	0	SDE	usecs.	tS	Stream. set-up/hold	0.030	-	usecs.
tH	SYNC IN pulse active	0.4*(CCD)	-	usecs.	tW	Transfer bus release	0	-	usecs.
tH'	SYNC OUT pulse active	0.32*(CCD)	-	usecs.	tY	SYNC IN period	CCD	-	usecs.
tI	Bus release set-up	0.025	-	usecs.	tY'	SYNC OUT period	CCD	-	usecs.
tL	SYNC IN pulse inactive	0.4*(CCD)	-	usecs.	tZ	Cable delay	0	CMX	usecs.

- NOTES:  
 (1) The master may or may not be driving the buses.  
 (2) This represents the slave's drivers in DOM only.

FIGURE 60  
 DATA STREAMING OUTPUT SEQUENCE - MASTER END

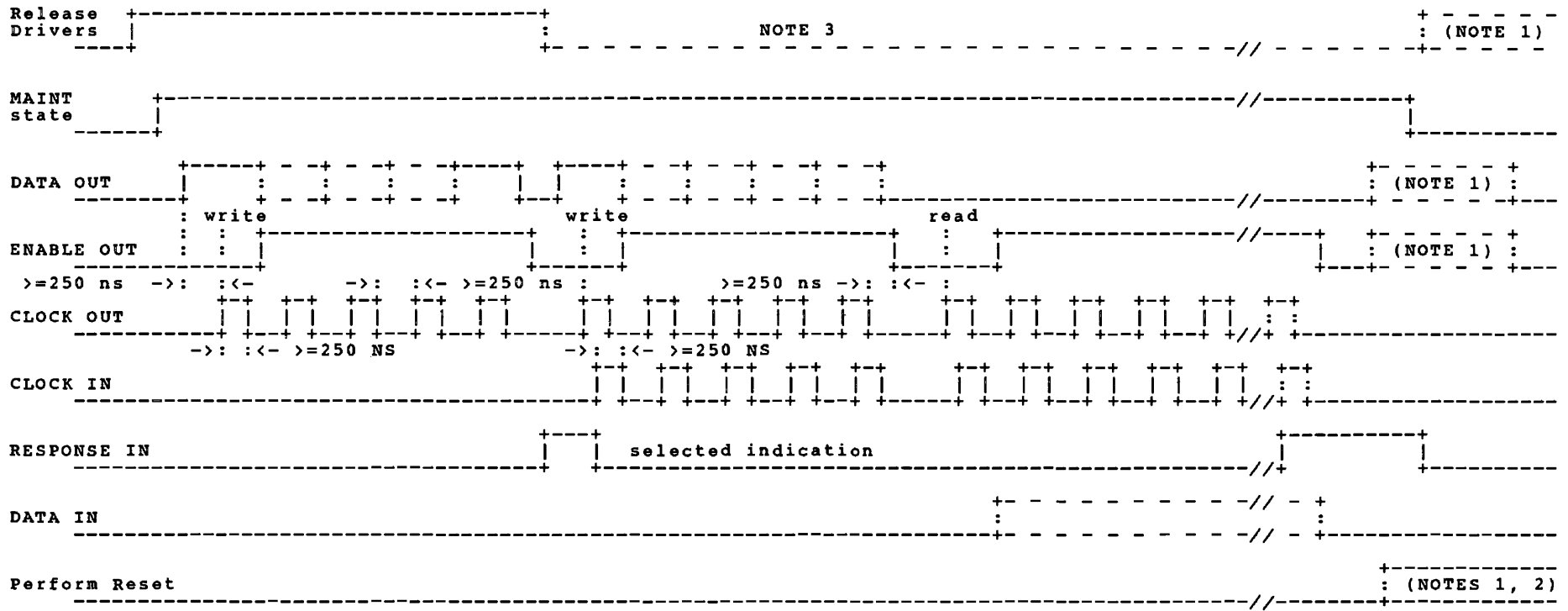


NOTES:

- (1) For MM1 slaves if DATA OUT is active when the MAINT state is negated, a reset shall be generated that will persist until DATA OUT is negated for a minimum of 10 microseconds. The drivers shall be left released if this situation occurs.
- (2) For MM2 slaves, if DATA OUT and ENABLE OUT are active when the MAINT state is negated, a reset shall be generated that will persist until DATA OUT or ENABLE OUT is negated for a minimum of 10 microseconds. The drivers shall be left released if this situation occurs.
- (3) The BUS A Selective Reset Control octet is assumed to contain the slave's address while the RESETSEL1 or RESETSEL2 state is active.

**FIGURE 61**  
**MAINTENANCE MODE 1**





**NOTES:**

- (1) If DATA OUT and ENABLE OUT are active when MAINT is negated, then a reset shall be generated that will persist until DATA OUT or ENABLE OUT is negated. The Reset shall persist for a minimum of 10 microseconds. The drivers shall be left released if this situation occurs.
- (2) If ENABLE OUT is active (and DATA OUT is not active) when MAINT state is negated, and if an MM2 Reset Order was issued while MAINT was active, a reset shall be generated that shall persist until ENABLE OUT is negated. The reset shall persist for a minimum of 10 microseconds.
- (3) Only the BUS B drivers used for MM2 sequences are enabled while a slave's MM2 circuits are selected.

**FIGURE 62**  
**MAINTENANCE MODE 2**

# Appendixes (These Appendixes are not part of American National Standard X3.129-1986, but are included for information only.)

## Appendix A

### Example of State Sequences for Information Transfer

Figure A1 is a simple example of use of the IPI to poll, select a slave, issue an Operation Command to read data, receive Operation Response, and Deselect.

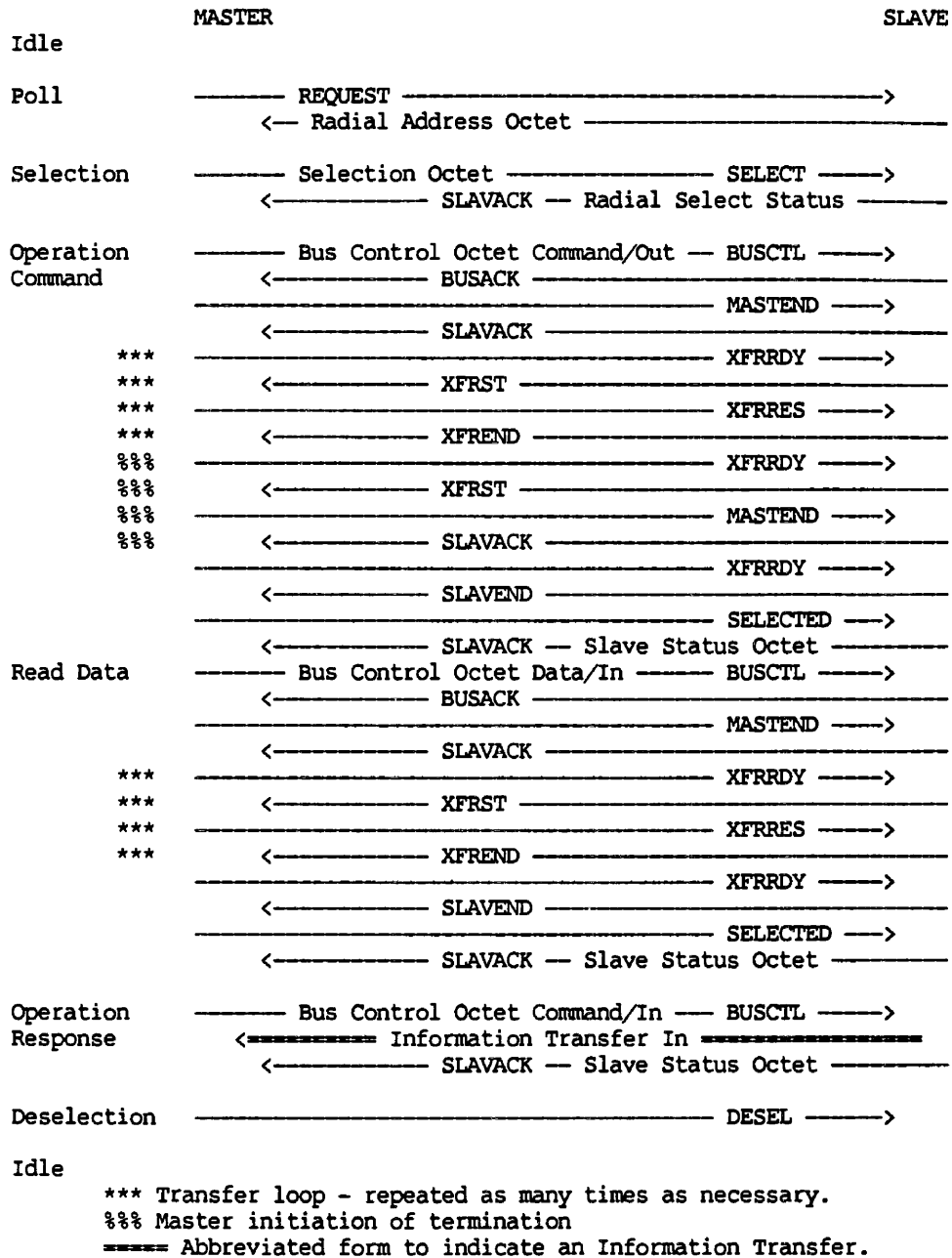


FIGURE A1  
 State Sequences for Information Transfer

## Appendix B

### Specifications for 24-Conductor Shielded Cable

The shielded 24-conductor (overall) coaxial cable is formed from two core assemblies, each consisting of 12 individual coaxial cables. Each core assembly should be covered with an overall shield and jacket. These two cables may be bonded together. If so, any such bond should allow the cables to be easily separated without reduction in their respective jacket thicknesses below the specified minimum at any point.

Inner Conductor diameter	0.0159, +0.0004, -0.0002 (26 AWG)
Diameter over primary insulation	0.100 min, 0.106 max
Outer conductor strand diameter	0.0040, +0.0003, -0.0001 (38 AWG)
Overall diameter	0.160 max

#### B1. Individual Coaxial Cables

The characteristics of these cables are as follows:

(1) *Inner Conductor.* 26-AWG solid, tinned copper or silver-plated copper alloy.

(2) *Primary Insulation.* Semi-solid, consisting of a filament of flame-retardant polyethylene spiraled around the inner conductor and covered with an extruded tube of the same material.

(3) *Outer Conductor.* Single-braid, tinned, soft-annealed copper, to provide a minimum coverage of 90%.

(4) *Jacket.* Polyvinyl chloride (PVC), UL recognized.

(5) *Dimensions and Tolerances.* The dimensions and tolerances (in inches) are as follows:

#### B2. Overall Cable Assembly

The following recommendations should be considered in the assembly of cables for the IPI.

(1) *Length.* Individual cables — continuous. All coaxial cables should be of equal length.

(2) *Shield.* Aluminum/"mylar" tape, with 25% overlap. The aluminum side should be outward. This tape should be covered with a braid of tinned copper wire with a 65% minimum coverage.

(3) *Jacket.* Polyvinyl chloride (PVC), 80 durometer maximum, UL recognized.

(4) *Flammability Rating.* UL recognized.

(5) *Marking.* In a manner required by UL or other regulating agencies.

(6) *Physical Ratings.* 60°C minimum, 150 volts minimum.

## Appendix C

### Specifications for 50-Conductor, Flat, Twisted-Pair Cable

#### C1. Introduction

This cable allows for mass termination of twisted pairs to all standard 50-mil insulation displacement connectors (IDC).

The flat, twisted-pair cable consists of 50 conductors twisted into pairs. Primary insulation should be Polyvinyl Chloride (PVC). The twist in adjacent pairs is reversed to reduce crosstalk. The cable allows mass termination of twisted pairs to all standard 50-mil insulation displacement connectors (IDC). The cable should allow for alternating twisted-pair sections with flat sections (in which the conductors are parallel) to enable installation of an IDC connector. The spacing of the flat sections is on 18-inch centers, (nominal).

The twisted-pair cable is primarily intended for attaching slaves within the same equipment cabinet that utilizes a differential driver/receiver system. However, if shielding techniques similar to those utilized on the jacketed and shielded, twisted-pair cable (see Appendix D) are applied, there is no reason why the cable cannot exit the cabinet.

#### C2. Component Wire Description

The wire should conform to the following recommendations:

(1) *Materials and Construction.* Tinned copper, 28AWG, 7/36 strand.

(2) *Component Wire Insulation.* Polyvinyl chloride (PVC).

(3) *Dimensions and Tolerances.* For walls of conductor insulation, 0.010 in nominal.

(4) *Conductor Insulation.* 0.010 nominal wall

#### C3. Cable Description

The cable should conform to the following recommendations:

(1) *Length.* Individual cables — continuous. Conductors — same length.

(2) *Conductor Spacing.* Centers for twisted-pair cables, 0.100 inch, nominal. Centers for conductor in flat regions,  $0.050 \pm 0.005$  inch.

(3) *Thickness.* 0.042 inch, nominal (flat sections), 0.080 inch, nominal (twisted sections).

(4) *Flammability Rating.* UL recognized.

(5) *Insulation.* Polyvinyl chloride (PVC).

(6) *Physical Ratings.* 80°C minimum, 150 volts minimum.

(7) *Distance between Flats.* The flat sections will contribute significantly to differential noise, so care should be taken to use flat sections only where required for connector termination.

## Appendix D

### Specifications for 50-Conductor, Shielded, Twisted-Pair Cable

#### D1. Introduction

The shielded twisted-pair cable assembly consists of 25 twisted pairs with an overall shield and jacket. The cable connectors are Subminiature "D" connectors with a metal shell and 360° shield termination (see Figure 6).

The jacketed and shielded twisted-pair cable is primarily intended for attaching slaves that are in separate cabinets and that utilize a differential driver/receiver system.

#### D2. Inner Conductors

Inner conductors of the shielded twisted-pair cable assembly should have the following characteristics:

- (1) *Materials and Construction.* Tinned copper, 26 AWG, 7/34 Strand Tinned copper, 28 AWG, 7/36 Strand
- (2) *Insulation.* High-density polyethylene
- (3) *Dimensions and Tolerances.* The dimensions and tolerances (in inches) are as follows:

Insulation thickness	0.011
Overall diameter	0.043 max
Pair lay	3/4 to 1.5 staggered left hand lay

#### D3. Cable

The cables used for the shielded twisted-pair cable assembly should have the following characteristics:

- (1) *Length.* Individual cables — continuous. Conductors — same length.
- (2) *Shield.* Braided, 36-AWG, tinned copper wire, to provide 85% minimum coverage.
- (3) *Jacket.* Polyvinyl chloride (PVC), UL recognized.
- (4) *Insulation Thickness.* 0.040 inch, minimum.
- (5) *Flammability Rating.* UL recognized.
- (6) *Marking.* In a manner required by UL or other regulating agencies.
- (7) *Physical Ratings.* 60°C minimum, 150 volts minimum.
- (8) *Outer Diameter.* 0.505 inch  $\pm$  0.020 inch
- (9) *Binder.* 0.002-inch Mylar tape, spiral wrapped, 25% lap

## Appendix E

### 75-Meter Differential Driver/Receiver System

The following is an example of one differential driver/receiver system that meets the requirements outlined in 4.4.3:

If the 75112/75107B driver/receiver is used, an 1800-ohm( $\pm 2\%$ ) biasing resistor from the odd lead to the negative voltage supply as well as from the even lead to the positive voltage supply will meet the requirements of 4.4.3. Note that the 75112/75107B requires a 5-volt ( $\pm 5\%$ ) positive supply and a 5-volt ( $\pm 5\%$ ) negative supply.

#### NOTES:

(1) In order to prevent the 75112 driver from causing errors, the interface must be quiesced prior to powering on or off the driver voltage supplies. After powering on or off any attached master or slave, all slaves must be reset since false errors may have been detected due to glitches that occur at that time.

(2) If the biasing network is in the master, and the master is powered off, the 75107 receiver or the 75108 receiver tend to oscillate. Either precautions must be taken in the slaves to prevent this oscillation from causing errors, or the master must consider powering the bias network in such a way that the biasing voltage can be maintained even with the master powered off.

(3) To reduce common mode noise in the master, the 75112 driver modules and terminator/biasing resistors should be placed as physically close together as possible on the same printed circuit card.

(4) When groups of 75112 drivers are released, common mode noise is generated. Shielding the IPI cable within slaves containing 75112 drivers is very effective in reducing the magnitude of such common mode noise.

(5) The amplitude of the noise within the slave is proportional to the number of drivers released at the same time. Limiting the number of slave 75112 drivers that can be released (inhibited) within a 2-microsecond window to no more than 9 reduces the amplitude of the common mode noise. The noise associated with going from released to operational is less, but it is recommended that the same constraint be applied.

## Appendix F

### Voltage Mode Differential Driver/Receiver System

#### F1. General

The drivers and receivers that conform to EIA RS-485-1983 are intended for balanced transmission-line applications employing multiple drivers and receivers in a bus configuration. They are protected against shorts and bus contention even with a ground difference of 7 volts between any two devices. Disabled drivers will maintain the high impedance state over a common mode range of  $-7\text{ V} < V_{cm} < 12\text{ V}$ , and as such will not interfere with the signal quality of the active driver even in the presence of ground transients up to  $\pm 7\text{ V}$ .

Meeting the requirements of EIA RS-485-1983 is a necessary condition for IPI, but it may not be sufficient. The ac performance of the drivers/receivers should be good enough to meet the specifications for jitter and distortion while driving 50 meters of cable loaded to satisfy the biasing and termination requirements of the IPI.

Distortion and jitter are caused mainly by the rise-time degradation due to the distributed low-pass-filter characteristics of the cable, and the effect of this degradation upon any signal imbalance or receiver threshold offset. As the signal travels down the cable, its rise time increases, causing increased jitter and distortion. For a given rise time (i.e., at a given length and quality of cable), a tighter receiver threshold and a better signal balance will give superior jitter and distortion numbers.

IPI lines require biasing to hold a "0" state when all drivers are off/disabled. This will introduce some signal imbalance and increase jitter. The driver must have drive, transient, and skew characteristics that will meet the jitter and distortion requirements in spite of this imbalance. Since ground differences are a fact of life, the jitter performance must also be maintained over a reasonable common-mode range.

The DS3695/DS3696 family will meet the IPI requirements with 50 meters of appropriate cable (see cable specs). The IPI bias network, with the Master either at the end of the cable or not, is shown in Figure F1.

Using the following suggested values will hold a bias voltage of at least 247 mV at any part (minimum bias occurs farthest from the Master) of the line, with the following assumptions:

- (1) Connector contact resistances are negligible.
- (2) Cable resistance is nominal (24 ohms) if maximum length (50 meters) is used.

(NOTE: The cable line resistance is in fact distributed along both sides of the pair, but in the figures it is shown as a single resistor.)

- (3) The input impedance and resistance (ac and dc) of the receivers used is high enough to be ignored, as is that of the driver when deselected or powered down. For the voltage to be at this minimum, the terminators, bias resistors, and power supply would all have to be at their tolerance limits in the worst direction at the same time. Nearly all conditions will result in minimum bias above 250 mV, but even the worst-case condition yields 247 mV.

These suggested resistor values were chosen to optimize the performance trade-offs among minimum and maximum bias levels, holding a "0" with no active driver while allowing normal signaling to overcome the bias without excessive skew and noise-margin deterioration. In addition, these values:

- (1) Are normal, low-cost standard values, available in discrettes, SIPs, and DIPs from most vendors, with standard tolerance of 2% or better, and

- (2) Use the same value for the external plug-in terminator and the equivalent-function on-board R2, for equipment designers who may want the option of operating either way (e.g., the same master configuration operating optimally at the cable end or not).

A tolerance specification of 2% is no additional cost in SIP/DIP resistors (see above), and 5% is easily obtained in power supplies and is required by many electronic components, including the DS3695/DS3696 series. These tolerances allow better system performance (e.g., lower error rate) by allowing a higher-impedance design, meeting the desired minimum bias with less maximum bias for the drivers to overcome. The termination value of

150 ohms is well in line with the design rule of slightly under-terminating transmission lines. It ensures positive reflections and faster transitions, optimizing receiver performance, especially with hysteresis receivers. This value has been carefully tested and its performance is verified. For those designers who may wish to consider other values in the bias network, there is available a noncopyrighted, suitable computer program to aid in evaluating combinations and other tolerance limits.

R1 = R3	=	510 (± 2%)	ohms
at Vcc	=	5 (± 5%)	volts
R2	=	150 (± 2%)	ohms
Terminator	=	150 (± 2%)	ohms

yielding bias voltages at

Master and Cable-End Terminator:

287 mV	247 mV (Minimum)
314 mV	271 mV (Nominal)
367 mV	295 mV (Maximum)

and equivalent termination resistance at Master (Nominal): 132 ohms.

EIA RS-485-1983 stipulates that the receiver respond to a 200-mV signal. This network is designed to cause any receiver on the line that conforms to EIA RS-485-1983 to switch to a "0" when all the drivers are off/disabled. Once the receiver has switched, it will have a noise immunity of at least 47 mV (plus the hysteresis and short-pulse rejection of the chosen receiver).

## F2. Calculating Resistor Values for the Bias Network

The formulas may be derived in the following manner. Figure F1(b) shows the worst-case configuration that provides the lowest bias voltage (at the cable end opposite the master). This occurs when the supply voltage and the termination-resistance values are low, and the bias resistor values are high:

$$\begin{aligned} V_{cc} &= V_{cc} \text{ (nominal)} \cdot (100 - t(V))/100 \\ R1 = R3 &= R1 \text{ (nominal)} \cdot (100 + t(R))/100 \\ R2 &= R2 \text{ (nominal)} \cdot (100 - t(R))/100 \\ RT2 &= RT2 \text{ (nominal)} \cdot (100 - t(R))/100 \end{aligned}$$

where

t(R) is the percentage resistor tolerance, and t(V) is the percentage power supply tolerance.

NOTE: The worst-case jitter and distortion occur with highest bias when the resistor and supply variations are opposite those given previously. The worst high bias occurs in the Master, when at the center of the cable.

In Figure F1(b), the bias voltage at the Master (VBiasM) is given by:

$$V_{BiasM} = \frac{R2 // (RT2 + RL2)}{R1 + R3 + (R2 // (RT2 + RL2))} V_{cc}$$

$$V_{BiasM} = \frac{R2 \cdot (RT2 + RL2)}{(R1 + R3) \cdot (R2 + RT2 + RL2) + R2 \cdot (RT2 + RL2)} V_{cc}$$

The bias voltage at the far-end terminator, VBias2, is given by:

$$V_{Bias2} = \frac{RT2}{RT2 + RL2} V_{BiasM}$$

$$= \frac{R2 \cdot RT2}{(R1 + R3) \cdot (R2 + RT2 + RL2) + R2 \cdot (RT2 + RL2)} V_{cc}$$

Hence, using R1 = R3 and therefore in the above (R1 + R3) = 2R1:

$$R1 = R3 = \frac{R2 \cdot RT2 \cdot (V_{cc} - V_{Bias2}) - RL2 \cdot R2 \cdot V_{Bias2}}{2 \cdot V_{Bias2} \cdot (R2 + RT2 + RL2)} \quad \text{(Eq F1)}$$

and the equivalent termination of the Bias/Term network is given by:

$$R_{TEq} = 2R1 // R2 = \frac{2R1 \cdot R2}{2R1 + R2},$$

from which

$$R2 = \frac{2R1 \cdot R_{TEq}}{2R1 - R_{TEq}} \quad \text{(Eq F2)}$$

Rearranging the terms in Eq F1:

$$R2 = \frac{2R1 \cdot V_{Bias2} \cdot (RT2 + RL2)}{RT2 \cdot (V_{cc} - V_{Bias2}) - RL2 \cdot V_{Bias2} - 2R1 \cdot V_{Bias2}} \quad \text{(Eq F3)}$$



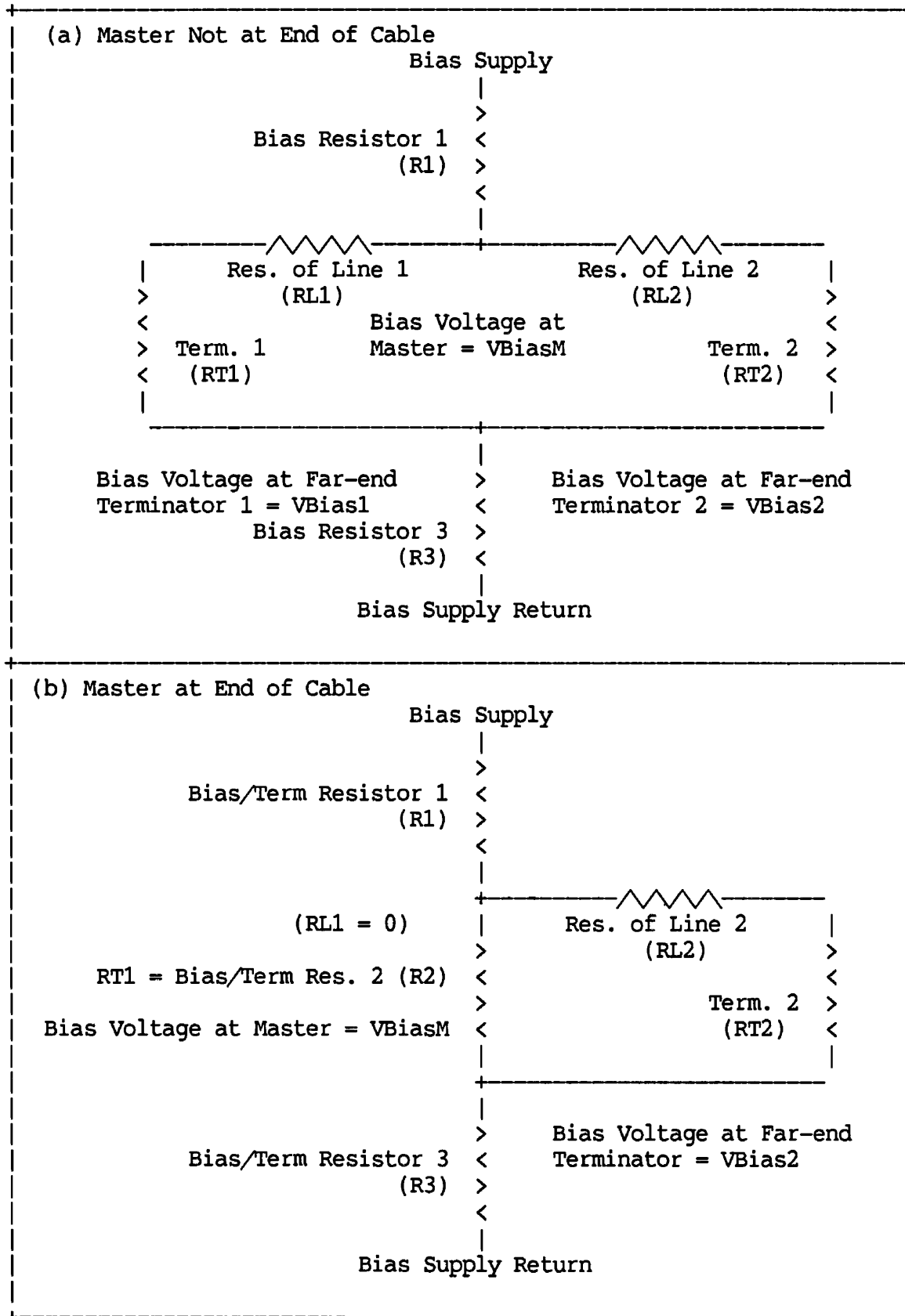


FIGURE F1  
THE TWO SUBSYSTEM ARRANGEMENTS WITH PARAMETER LABELS



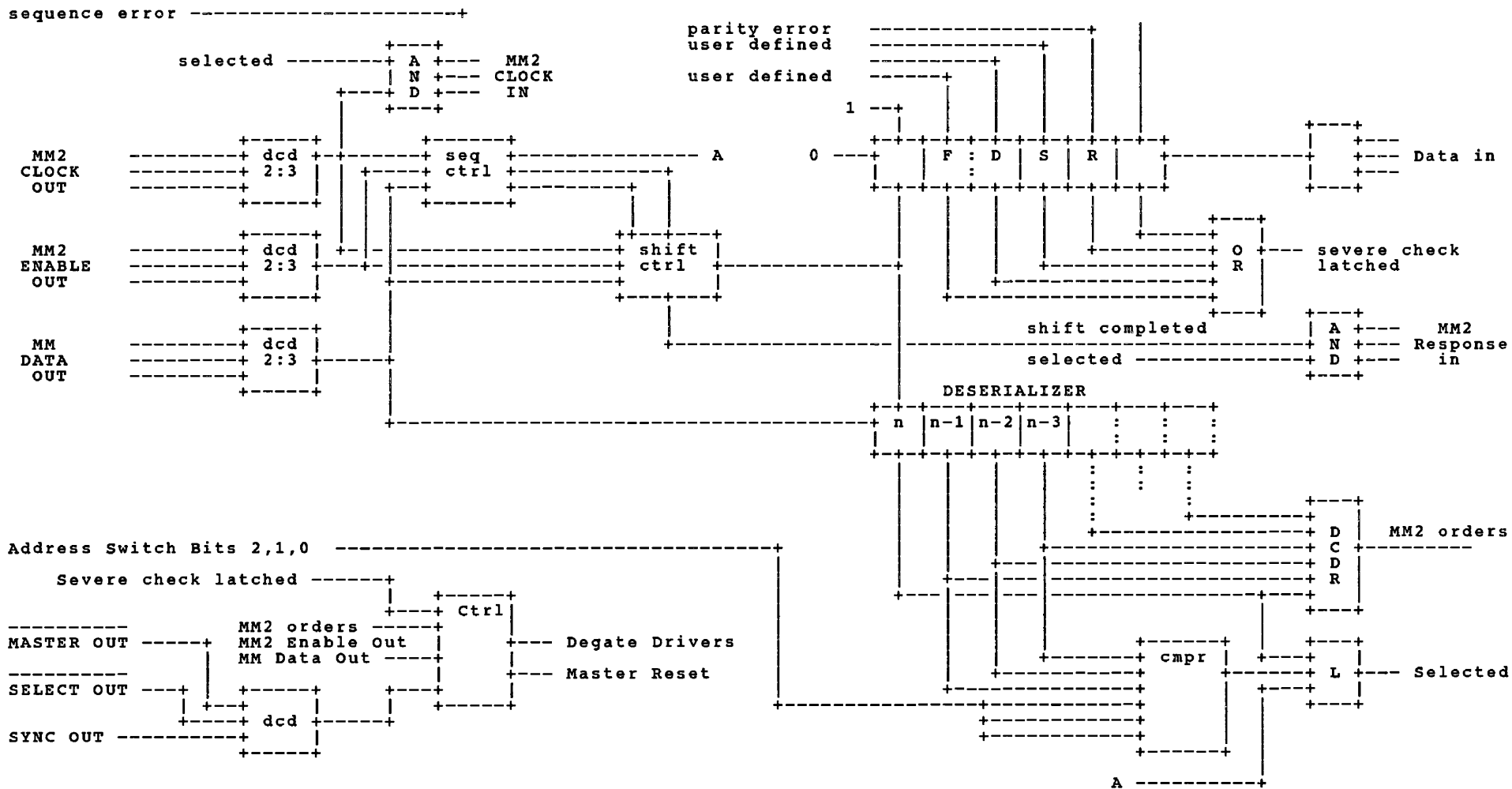
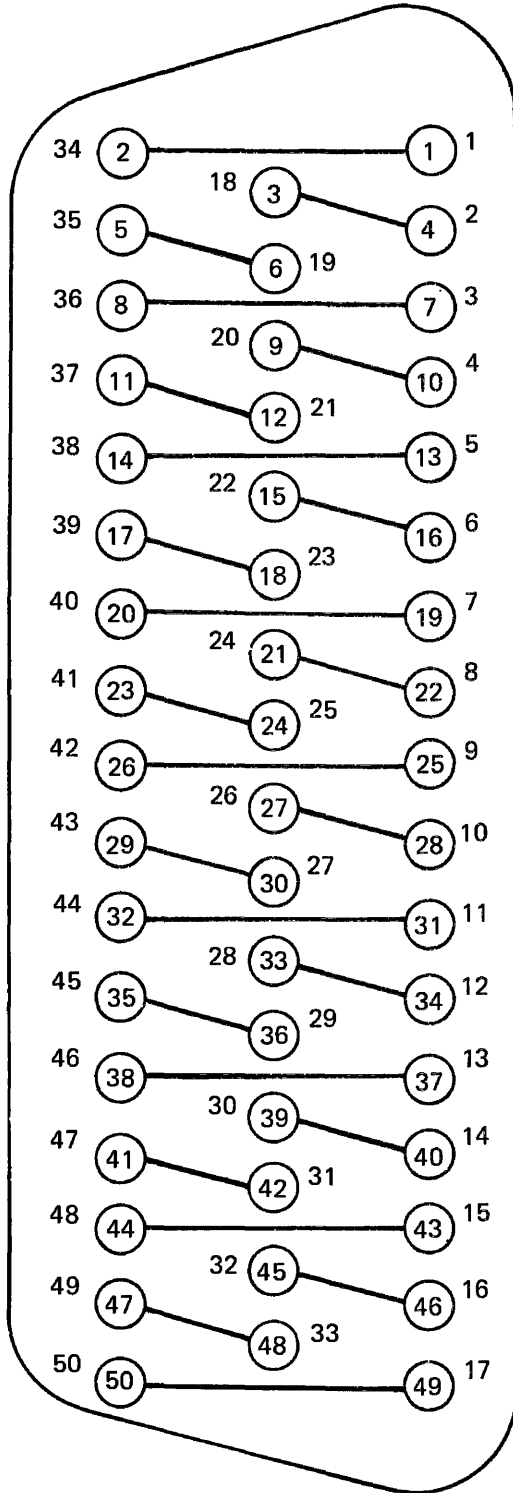


FIGURE G2  
MM2 Block Diagram

## Appendix H

### Flat Cable Conductor/Subminiature "D" Connector Pin Identification

Figure H1 illustrates the correspondence of flat cable conductor numbers to the IEC 48B pin numbering system.



NOTE: Conductor numbers noted in circles are the conductor numbers of flat cable. The numbers outside the circles are the corresponding pin numbers on the IEC48B connector. The lines connecting the pin numbers indicate signal pair assignments, and not direct connections.

FIGURE H1  
CORRESPONDENCE BETWEEN CONDUCTOR  
NUMBERS AND PIN NUMBERS





**X3.115-1984** Unformatted 80 Megabyte Trident Pack for Use at 370 tpi and 6000 bpi (General, Physical, and Magnetic Characteristics)

**X3.116-1986** Recorded Magnetic Tape Cartridge, 4-Track, Serial 0.250 Inch (6.30 mm) 6400 bpi (252 bpmm), Inverted Modified Frequency Modulation Encoded

**X3.117-1984** Printable/Image Areas for Text and Facsimile Communication Equipment

**X3.118-1984** Financial Services — Personal Identification Number — PIN Pad

**X3.119-1984** Contact Start/Stop Storage Disk, 158361 Flux Transitions per Track, 8.268 Inch (210 mm) Outer Diameter and 3.937 inch (100 mm) Inner Diameter

**X3.120-1984** Contact Start/Stop Storage Disk

**X3.121-1984** Two-Sided, Unformatted, 8-Inch (200-mm), 48-tpi, Double-Density, Flexible Disk Cartridge for 13 262 fpr Two-Headed Application

**X3.122-1986** Computer Graphics Metafile for the Storage and Transfer of Picture Description Information

**X3.124-1985** Graphical Kernel System (GKS) Functional Description

**X3.124.1-1985** Graphical Kernel System (GKS) FORTRAN Binding

**X3.125-1985** Two-Sided, Double-Density, Unformatted 5.25-inch (130-mm), 48-tpi (1,9-tpmm), Flexible Disk Cartridge for 7958 bpr Use

**X3.126-1986** One- or Two-Sided Double-Density Unformatted 5.25-inch (130-mm), 96 Tracks per Inch, Flexible Disk Cartridge

**X3.127-1987** Unrecorded Magnetic Tape Cartridge for Information Interchange

**X3.128-1986** Contact Start-Stop Storage Disk — 83 000 Flux Transitions per Track, 130-mm (5.118-in) Outer Diameter and 40-mm (1.575-in) Inner Diameter

**X3.129-1986** Intelligent Peripheral Interface, Physical Level

**X3.130-1986** Intelligent Peripheral Interface, Logical Device Specific Command Sets for Magnetic Disk Drive

**X3.131-1986** Small Computer Systems Interface

**X3.132-1987** Intelligent Peripheral Interface — Logical Device Generic Command Set for Optical and Magnetic Disks

**X3.133-1986** Database Language —NDL

**X3.135-1986** Database Language — SQL

**X3.136-1986** Serial Recorded Magnetic Tape Cartridge for Information Interchange, Four and Nine Track

**X3.139-1987** Fiber Distributed Data Interface (FDDI) Token Ring Media Access Control (MAC)

**X3.140-1986** Open Systems Interconnection — Connection Oriented Transport Layer Protocol Specification

**X3.141-1987** Data Communication Systems and Services — Measurement Methods for User-Oriented Performance Evaluation

**X3.146-1987** Device Level Interface for Streaming Cartridge and Cassette Tape Drives

**X3.147-1987** Intelligent Peripheral Interface — Logical Device Generic Command Set for Magnetic Tapes

**X3.153-1987** Open Systems Interconnection — Basic Connection Oriented Session Protocol Specification

**X3.156-1987** Nominal 8-Inch Rigid Disk Removable Cartridge

**X3.157-1987** Recorded Magnetic Tape for Information Interchange, 3200 CPI

**X3.158-1987** Serial Recorded Magnetic Tape Cassette for Information Interchange, 0.150 Inch (3.81 mm), 8000 bpi (315 bpmm), Group Code Recording.

**X11.1-1977** Programming Language MUMPS

**IEEE 416-1978** Abbreviated Test Language for All Systems (ATLAS)

**IEEE 716-1982** Standard C/ATLAS Language

**IEEE 717-1982** Standard C/ATLAS Syntax

**IEEE 770X3.97-1983** Programming Language PASCAL

**IEEE 771-1980** Guide to the Use of ATLAS

**ISO 8211-1986** Specifications for a Data Descriptive File for Information Interchange

**MIL-STD-1815A-1983** Reference Manual for the Ada Programming Language

**NBS-ICST 1-1986** Fingerprint Identification — Data Format for Information Interchange

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**X3/TRI-82** Dictionary for Information Processing Systems (Technical Report)

# American National Standards for Information Processing

- X3.1-1987** Synchronous Signaling Rates for Data Transmission  
**X3.2-1970** Print Specifications for Magnetic Ink Character Recognition  
**X3.4-1986** Coded Character Sets — 7-Bit ASCII  
**X3.5-1970** Flowchart Symbols and Their Usage  
**X3.6-1965** Perforated Tape Code  
**X3.9-1978** Programming Language FORTRAN  
**X3.11-1969** General Purpose Paper Cards  
**X3.14-1983** Recorded Magnetic Tape (200 CPI, NRZI)  
**X3.15-1976** Bit Sequencing of the American National Standard Code for Information Interchange in Serial-by-Bit Data Transmission  
**X3.16-1976** Character Structure and Character Parity Sense for Serial-by-Bit Data Communication in the American National Standard Code for Information Interchange  
**X3.17-1981** Character Set for Optical Character Recognition (OCR-A)  
**X3.18-1974** One-Inch Perforated Paper Tape  
**X3.19-1974** Eleven-Sixteenths-Inch Perforated Paper Tape  
**X3.20-1967** Take-Up Reels for One-Inch Perforated Tape  
**X3.21-1967** Rectangular Holes in Twelve-Row Punched Cards  
**X3.22-1983** Recorded Magnetic Tape (800 CPI, NRZI)  
**X3.23-1985** Programming Language COBOL  
**X3.25-1976** Character Structure and Character Parity Sense for Parallel-by-Bit Data Communication in the American National Standard Code for Information Interchange  
**X3.26-1980** Hollerith Punched Card Code  
**X3.27-1987** Magnetic Tape Labels and File Structure  
**X3.28-1976** Procedures for the Use of the Communication Control Characters of American National Standard Code for Information Interchange in Specified Data Communication Links  
**X3.29-1971** Specifications for Properties of Unpunched Oiled Paper Perforator Tape  
**X3.30-1986** Representation for Calendar Date and Ordinal Date  
**X3.31-1973** Structure for the Identification of the Counties of the United States  
**X3.32-1973** Graphic Representation of the Control Characters of American National Standard Code for Information Interchange  
**X3.34-1972** Interchange Rolls of Perforated Tape  
**X3.37-1987** Programming Language APT  
**X3.38-1972** Identification of States of the United States (Including the District of Columbia)  
**X3.39-1986** Recorded Magnetic Tape (1600 CPI, PE)  
**X3.40-1983** Unrecorded Magnetic Tape (9-Track 800 CPI, NRZI; 1600 CPI, PE; and 6250 CPI, GCR)  
**X3.41-1974** Code Extension Techniques for Use with the 7-Bit Coded Character Set of American National Standard Code for Information Interchange  
**X3.42-1975** Representation of Numeric Values in Character Strings  
**X3.43-1986** Representations of Local Time of Day  
**X3.44-1974** Determination of the Performance of Data Communication Systems  
**X3.45-1982** Character Set for Handprinting  
**X3.46-1974** Unrecorded Magnetic Six-Disk Pack (General, Physical, and Magnetic Characteristics)  
**X3.47-1977** Structure for the Identification of Named Populated Places and Related Entities of the States of the United States for Information Interchange  
**X3.48-1986** Magnetic Tape Cassettes (3.81-mm [0.150-Inch] Tape at 32 b/mm [800 bpi], PE)  
**X3.49-1975** Character Set for Optical Character Recognition (OCR-B)  
**X3.50-1986** Representations for U.S. Customary, SI, and Other Units to Be Used in Systems with Limited Character Sets  
**X3.51-1986** Representations of Universal Time, Local Time Differentials, and United States Time Zone References  
**X3.52-1976** Unrecorded Single-Disk Cartridge (Front Loading, 2200 BPI) (General, Physical, and Magnetic Requirements)  
**X3.53-1976** Programming Language PL/I  
**X3.54-1986** Recorded Magnetic Tape (6250 CPI, Group Coded Recording)  
**X3.55-1982** Unrecorded Magnetic Tape Cartridge, 0.250 Inch (6.30 mm), 1600 bpi (63 b/mm), Phase encoded  
**X3.56-1986** Recorded Magnetic Tape Cartridge, 4 Track, 0.250 Inch (6.30 mm), 1600 bpi (63 b/mm), Phase Encoded  
**X3.57-1977** Structure for Formatting Message Headings Using the American National Standard Code for Information Interchange for Data Communication Systems Control  
**X3.58-1977** Unrecorded Eleven-Disk Pack (General, Physical, and Magnetic Requirements)  
**X3.60-1978** Programming Language Minimal BASIC  
**X3.61-1986** Representation of Geographic Point Locations  
**X3.62-1987** Paper Used in Optical Character Recognition (OCR) Systems  
**X3.63-1981** Unrecorded Twelve-Disk Pack (100 Megabytes) (General, Physical, and Magnetic Requirements)  
**X3.64-1979** Additional Controls for Use with American National Standard Code for Information Interchange  
**X3.66-1979** Advanced Data Communication Control Procedures (ADCCP)  
**X3.72-1981** Parallel Recorded Magnetic Tape Cartridge, 4 Track, 0.250 Inch (6.30 mm), 1600 bpi (63 b/mm), Phase Encoded  
**X3.73-1980** Single-Sided Unformatted Flexible Disk Cartridge (for 6631-BPR Use)  
**X3.74-1987** Programming Language PL/I, General-Purpose Subset  
**X3.76-1981** Unformatted Single-Disk Cartridge (Top Loading 200 tpi 4400 bpi) (General, Physical, and Magnetic Requirements)  
**X3.77-1980** Representation of Pocket Select Characters  
**X3.78-1981** Representation of Vertical Carriage Positioning Characters in Information Interchange  
**X3.79-1981** Determination of Performance of Data Communications Systems That Use Bit-Oriented Communication Procedures  
**X3.80-1981** Interfaces between Flexible Disk Cartridge Drives and Their Host Controllers  
**X3.82-1980** One-Sided Single-Density Unformatted 5.25-Inch Flexible Disk Cartridge (for 3979-BPR Use)  
**X3.83-1980** ANSI Sponsorship Procedures for ISO Registration According to ISO 2375  
**X3.84-1981** Unformatted Twelve-Disk Pack (200 Megabytes) (General, Physical, and Magnetic Requirements)  
**X3.85-1981** 1/2-Inch Magnetic Tape Interchange Using a Self Loading Cartridge  
**X3.86-1980** Optical Character Recognition (OCR) Inks  
**X3.88-1981** Computer Program Abstracts  
**X3.89-1981** Unrecorded Single-Disk, Double-Density Cartridge (Front Loading, 2200 bpi, 200 tpi) (General, Physical, and Magnetic Requirements)  
**X3.91M-1987** Storage Module Interfaces  
**X3.92-1981** Data Encryption Algorithm  
**X3.93M-1981** OCR Character Positioning  
**X3.94-1985** Programming Language PANCM  
**X3.95-1982** Microprocessors — Hexadecimal Input/Output, Using 5-Bit and 7-Bit Teleprinters  
**X3.96-1983** Continuous Business Forms (Single-Part)  
**X3.98-1983** Text Information Interchange in Page Image Format (PIF)  
**X3.99-1983** Print Quality Guideline for Optical Character Recognition (OCR)  
**X3.100-1983** Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment for Packet Mode Operation with Packet Switched Data Communications Network  
**X3.101-1984** Interfaces Between Rigid Disk Drive(s) and Host(s)  
**X3.102-1983** Data Communication Systems and Services — User-Oriented Performance Parameters  
**X3.103-1983** Unrecorded Magnetic Tape Minicassette for Information Interchange, Coplanar 3.81 mm (0.150 in)  
**X3.104-1983** Recorded Magnetic Tape Minicassette for Information Interchange, Coplanar 3.81 mm (0.150 in), Phase Encoded  
**X3.105-1983** Data Link Encryption  
**X3.106-1983** Modes of Operation for the Data Encryption Algorithm  
**X3.110-1983** Videotex/Teletext Presentation Level Protocol Syntax  
**X3.111-1986** Optical Character Recognition (OCR) Matrix Character Sets for OCR-M  
**X3.112-1984** 14-in (356-mm) Diameter Low-Surface-Friction Magnetic Storage Disk  
**X3.113-1987** Programming Language FULL BASIC  
**X3.114-1984** Alphanumeric Machines; Coded Character Sets for Keyboard Arrangements in ANSI X4.23-1982 and X4.22-1983

(Continued on reverse)



NIST-772  
(REV. 10-88)

U.S. DEPARTMENT OF COMMERCE  
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY

CHANGE NUMBER 2 - FIPS 60-2 & 62  
1-FIPS 61-1,63-1,97,111,130&131

## FIPS PUBLICATION CHANGE NOTICE

DATE OF CHANGE  
1990 December 26

FIPS PUBLICATION NUMBER  
See above.

**PUBLICATION TITLE** FIPS 60-2, I/O Channel Interface; 62, Operational Specifications for Magnetic Tape Subsystems; 61-1, Channel Level Power Control Interface; 63-1, Operational Specifications for Variable Block Rotating Mass Storage Subsystems; 97, Operational Specifications for Fixed Block Rotating Mass Storage Subsystems; 111, Storage Module Interfaces (w/extens. for enhanced storage module interface); 130, Intelligent Peripheral Interface (IPI); 131, Small Computer System Interface (SCSI).

**THIS OFFICE HAS A RECORD OF YOUR INTEREST IN RECEIVING CHANGES TO THE ABOVE FIPS PUBLICATION. THE CHANGE(S) INDICATED BELOW HAVE BEEN PROVIDED BY THE MAINTENANCE AGENCY FOR THIS PUBLICATION AND WILL BE INCLUDED IN THE NEXT PUBLISHED REVISION TO THIS FIPS PUBLICATION. QUESTIONS OR REQUESTS FOR ADDITIONAL INFORMATION SHOULD BE ADDRESSED TO THE MAINTENANCE AGENCY:**

Department of Commerce  
National Institute of Standards and Technology  
National Computer Systems Laboratory  
Gaithersburg, MD 20899

### CHANGE ITEM(S)

Attached is a reprint from the December 18, 1990, FEDERAL REGISTER (55 FR 51941) which provides approved revisions by the Secretary of Commerce to the FIPS family of input/output interface standards, and the approved discontinuation of the Exclusion and Verification Lists for these standards.

These approved revisions became effective on December 18, 1990, and become an integral part of FIPS 60-2, 61-1, 62, 63-1, 97, 111, 130 and 131, and, as such, are considered to be included whenever reference is made to them.

These approved revisions should be filed with each FIPS listed above.

Attachment ..

Copies of FIPS are available from:

National Technical Information Service (NTIS)  
ATTN: Sales Office, Sills Building  
5285 Port Royal Road  
Springfield, Virginia 22161

Phone - 703/487-4650 Office Hours - 7:45 a.m. to 4:15 p.m.



Tuesday  
December 18, 1990

National Institute of Standards and Technology  
NOTICES  
Information processing standards. Federal:  
Family of input/output interface standards, 51941

National Institute of Standards and  
Technology

[Docket No. 900101-0219]

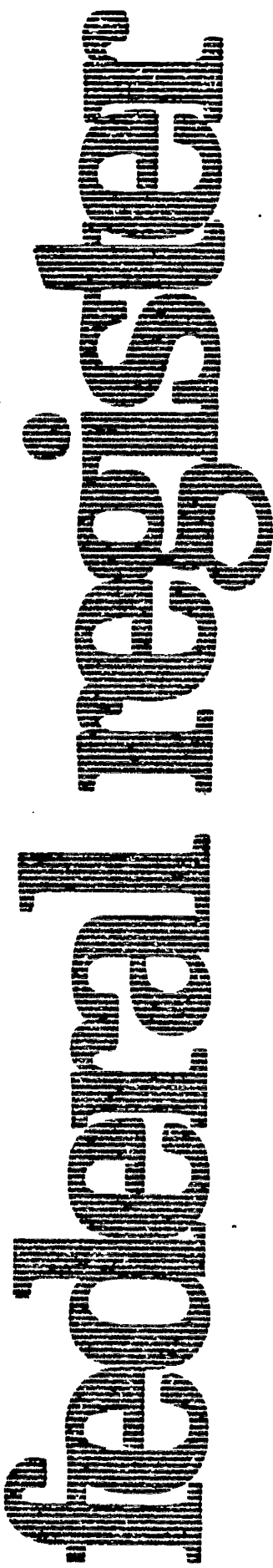
RIN 0693-AA59

**Approval of Revisions to Federal  
Information Processing Standards  
(FIPS) Family of Input/Output Interface  
Standards**

**AGENCY:** National Institute of Standards  
and Technology (NIST), Commerce.

**ACTION:** The purpose of this notice is to  
announce that the Secretary of  
Commerce has approved revisions to the  
Federal Information Processing  
Standards (FIPS) family of input/output  
interface standards, and has approved  
discontinuation of the exclusion and  
verification lists for these standards.

**SUMMARY:** On March 20, 1990, notice  
was published in the Federal Register  
(55 FR 10272) proposing revision of  
Federal Information Processing  
Standards (FIPS) 60-2, 61-1, 62, 63-1, 97,  
111, 130, and 131 to make them non-  
mandatory, and discontinue the  
exclusion and verification lists for these  
standards. This proposal superseded the  
proposal for revision of these standards  
announced in the Federal Register (52  
FR 44462) of November 19, 1987.  
Procedures for the Exclusion List for  
FIPS 60, 61, 62, 63, and 97 were  
published in the Federal Register on





September 3, 1982 (47 FR 38959-38960). Procedures for the Verification List for FIPS 60, 61, 62, 63, and 97 were published in the **Federal Register** on December 11, 1979 (44 FR 71444-71445) and on April 7, 1981 (46 FR 20719-20720).

The written comments submitted by interested parties and other material available to the Department relevant to these proposed revisions were reviewed by NIST. On the basis of this review, NIST recommended that the Secretary approve revisions to the input/output family of standards and approve discontinuation of the exclusion and verification lists for these standards. NIST prepared a detailed justification document for the Secretary's review in support of those recommendations.

This notice provides only the changes to the revised standards.

**EFFECTIVE DATE:** These revisions are effective December 18, 1990.

**ADDRESSES:** Interested parties may obtain copies of FIPS PUBS 60-2, 61-1, 62, 63-1, 97, 111, 130, and 131 from the National Technical Information Service, U.S. Department of Commerce, Springfield, VA 22161.

**FOR FURTHER INFORMATION CONTACT:** Ms. Shirley Radack, National Institute of Standards and Technology, Gaithersburg, MD 20899, telephone (301) 975-2833.

**SUPPLEMENTARY INFORMATION:** Under the provisions of 40 U.S.C. 759(d), the Secretary of Commerce is authorized to promulgate standards and guidelines for Federal computer systems, and to make such standards compulsory and binding to the extent to which the Secretary determines necessary to improve the efficiency of operation, or security and privacy of Federal computer systems.

The family of I/O interface standards currently includes:

- a. FIPS 60-2, I/O Channel Interface, revised July 29, 1983.
- b. FIPS 61-1, Channel Level Power Control Interface, revised July 13, 1982.
- c. FIPS 62, Operational Specifications for Magnetic Tape Subsystems, revised December 30, 1980.
- d. FIPS 63-1, Operational Specifications for Variable Block Rotating Mass Storage Subsystems, revised April 14, 1983; Supplement to FIPS PUB. 63-1, Additional Operational Specifications for Variable Block Rotating Mass Storage Subsystems, April 14, 1983.
- e. FIPS 97, Operational Specifications for Fixed Block Rotating Mass Storage Subsystems, February 4, 1983.
- f. FIPS 111, Storage Module Interfaces (with extensions for enhanced storage module interfaces), April 18, 1985.

g. FIPS 130, Intelligent Peripheral Interface (IPI), July 16, 1987.

h. FIPS 131, Small Computer System Interface (SCSI) July 16, 1987.

The following revisions are being made effective immediately upon publication. A delayed effective date is not required because these standards are exempt from the Administrative Procedure Act by U.S.C. 553(a)(2).

Revisions to Federal Information Processing Standards 60-2, 61-1, 62, 63-1, 97, 111, 130, and 131.

FIPS 60-2, I/O Channel Interface, is revised as follows:

**Applicability.** This standard addresses the interconnection of computer peripheral equipment as a part of ADP systems for the following types of peripherals: (1) Magnetic tape equipment employing open reel-to-reel magnetic tape storage devices, specifically excluding magnetic tape cassette and tape cartridge storage devices, (2) magnetic disk storage equipment employing disk drives each having a capacity greater than 7 megabytes per storage module, excluding flexible disk and disk cartridge devices having a smaller storage capacity per device, and (3) other peripheral equipment employing peripheral device types for which operational specifications standards have been issued as Federal Information Processing Standards. This standard is recommended for use in the acquisition of peripheral equipment for ADP systems with input/output channel interfaces as specified in the technical specifications, when it is determined that interchange of equipment between different systems is likely.

**Implementation.** The original version of this standard became effective December 13, 1979. The first revision became effective June 23, 1980, and the second revision became effective July 29, 1983. This revision becomes effective December 18, 1990.

**Waivers.** This standard is non-mandatory. No waivers are required.

FIPS 61-1, Channel Level Power Control Interface, is revised as follows:

**Applicability.** This standard addresses the power control interface in connecting computer peripheral equipment to ADP systems. It is recommended for use when FIPS 60-2 is used, when it is determined that interchange of equipment between different systems is likely.

**Implementation.** The original version of this standard became effective June 23, 1980, and the first revision became effective July 13, 1982. This revision becomes effective December 18, 1990.

**Waivers.** This standard is non-mandatory. No waivers are required.

FIPS 62, Operational Specifications for Magnetic Tape Subsystems, is revised as follows:

**Applicability.** This standard addresses magnetic tape equipment connected to ADP systems through FIPS 60 interfaces. It is recommended for use in the acquisition of such equipment, when it is determined that interchange of equipment between different systems is likely.

**Implementation.** The original version of this standard became effective June 23, 1980. This revision becomes effective December 18, 1990.

**Waivers.** This standard is non-mandatory. No waivers are required.

FIPS 63-1, Operational Specifications for Variable Block Rotating Mass Storage Subsystems, is revised as follows:

**Applicability.** This standard addresses peripheral device dependent operational interfaces for connecting variable block rotating mass storage equipment to ADP systems through FIPS 60 interfaces. It is recommended for use in the acquisition of such variable block rotating mass storage equipment for connection to ADP systems, when it is determined that interchange of equipment between different systems is likely.

**Implementation.** This standard became effective June 23, 1980, and the first revision became effective April 14, 1983. This revision becomes effective December 18, 1990.

**Waivers.** This standard is non-mandatory. No waivers are required.

FIPS 97, Operational Specifications for Fixed Block Rotating Mass Storage Subsystems, is revised as follows:

**Applicability.** This standard addresses the peripheral device dependent operational interface specifications for connecting fixed block rotating mass storage equipment to ADP systems through FIPS 60 interfaces. It is recommended for use in the acquisition of such fixed block rotating mass storage equipment for connection to ADP systems, when it is determined that interchange of equipment between different systems is likely.

**Implementation.** The original version of this standard became effective February 4, 1983. This revision becomes effective December 18, 1990.

**Waivers.** This standard is non-mandatory. No waivers are required.

FIPS 111, Storage Module Interfaces, is revised as follows:

**Applicability.** This standard addresses connection of a disk drive to a controller as part of an ADP system. This standard is recommended for use in the acquisition of disk systems that are



connected to small and medium sized computer systems, when it is determined that interchange of equipment between different systems is likely.

**Implementation.** This standard became effective May 18, 1985. This revision becomes effective December 18, 1990.

**Waivers.** This standard is non-mandatory. No waivers are required.

**FIPS 130, Intelligent Peripheral Interface (IPI), is revised as follows:**

**Section 8, Applicability.** This standard applies to the connection of computers to storage peripheral device controllers. This standard is recommended for use in the acquisition of magnetic disk drives, optical disk drives, and tape drives to be connected to minicomputer systems, when it is determined that interchange of equipment between different systems is likely.

**Section 10, Implementation.** This standard became effective December 16, 1987. This revision becomes effective December 18, 1990.

**Section 11, Waivers.** This standard is non-mandatory. No waivers are required.

**FIPS 131, Small Computer System Interface (SCSI) is revised as follows:**

**Section 8, Applicability.** This standard addresses the connection of small computers to peripheral devices with integral controllers. This standard is recommended for use in the acquisition of storage peripherals and small computer systems for office or laboratory use, when it is determined that interchange of equipment between different systems is likely.

**Section 10, Implementation.** This standard became effective December 16, 1987. This revision becomes effective December 18, 1990.

**Section 11, Waivers.** This standard is non-mandatory. No waivers are required.

Dated: December 12, 1990.

John W. Lyons,  
*Director.*

[FR Doc. 90-29563 Filed 12-17-90; 8:45 am]

BILLING CODE 3510-CN-M

