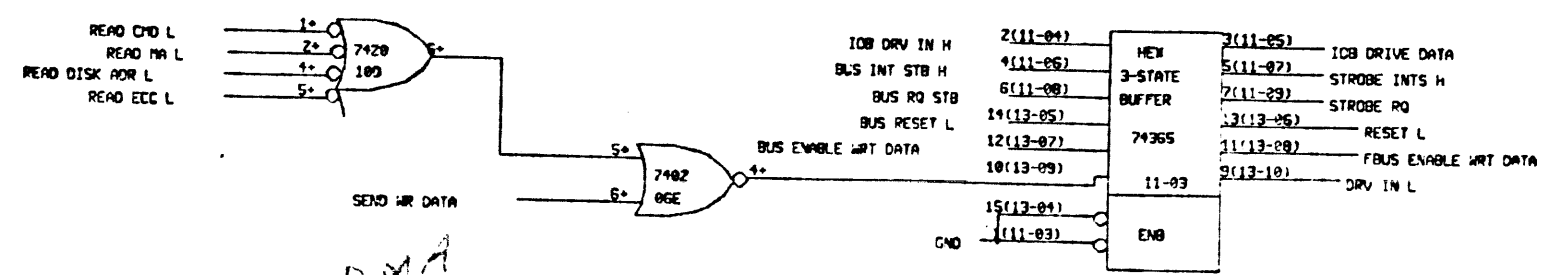
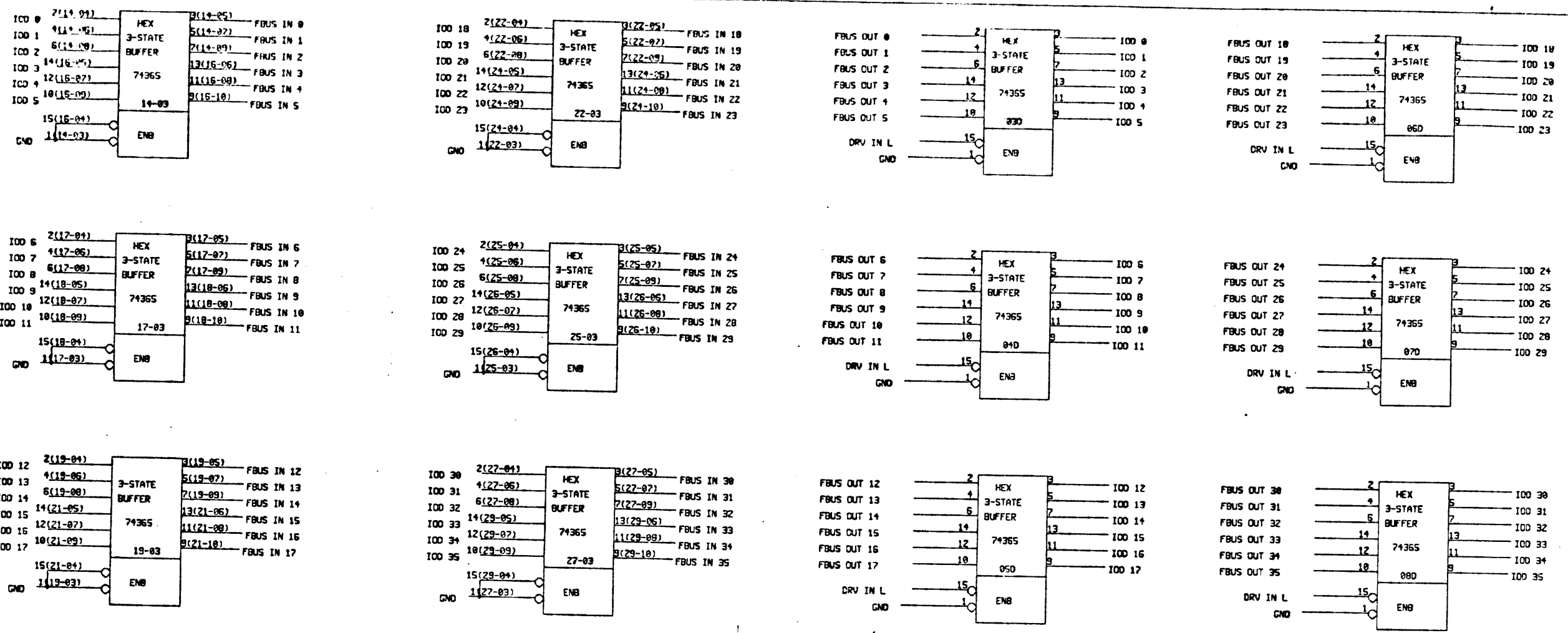
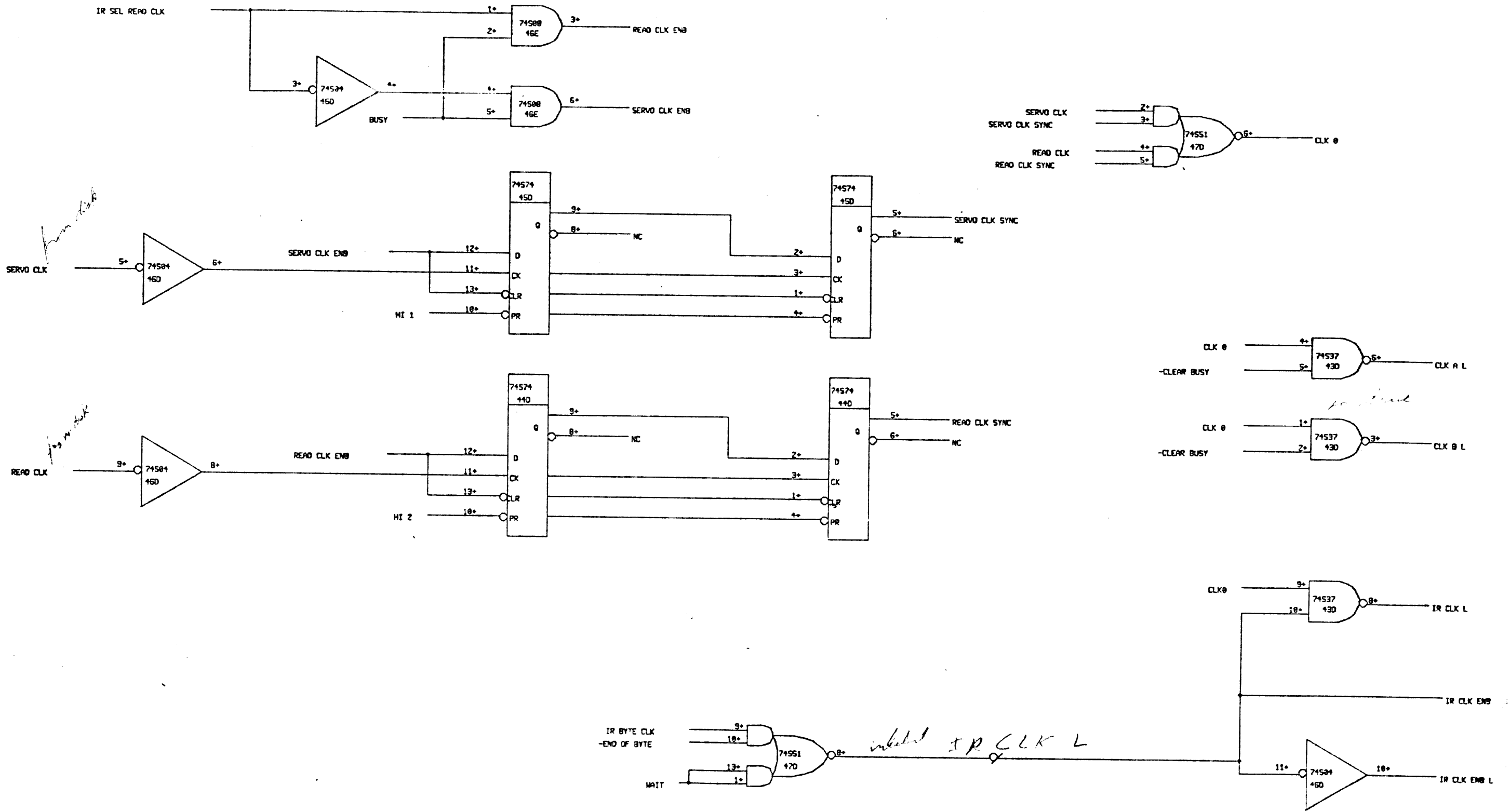


FOONLY, INC.		23-DEC-79 15:01	
		CFDACN.DRW (4,41)	
DRAWN BY:	PAGE	OF	NUMBER /
APPROVED BY:	PROJECT:		REV.

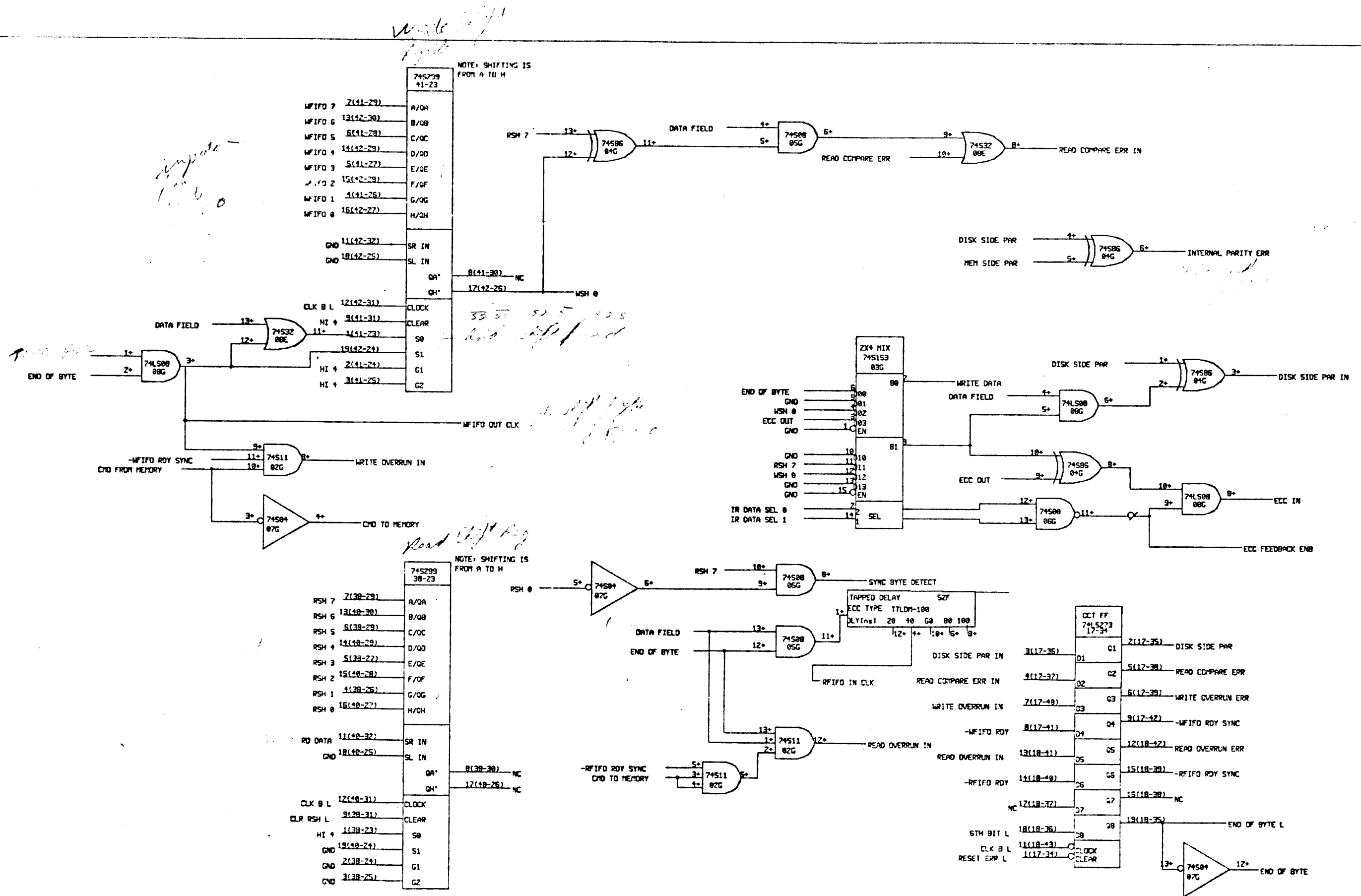
SNL



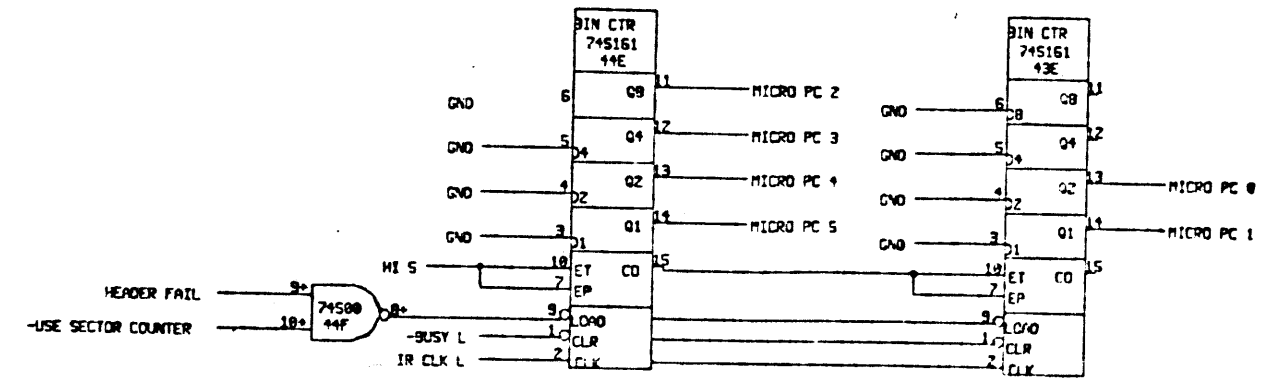
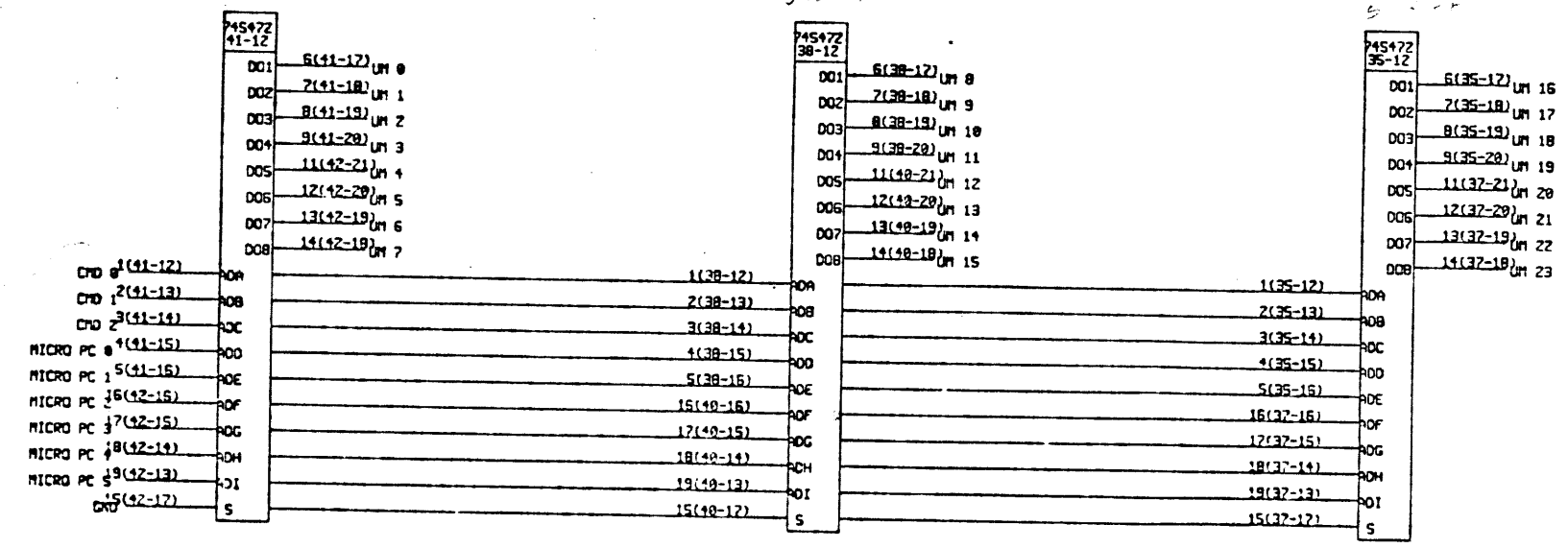
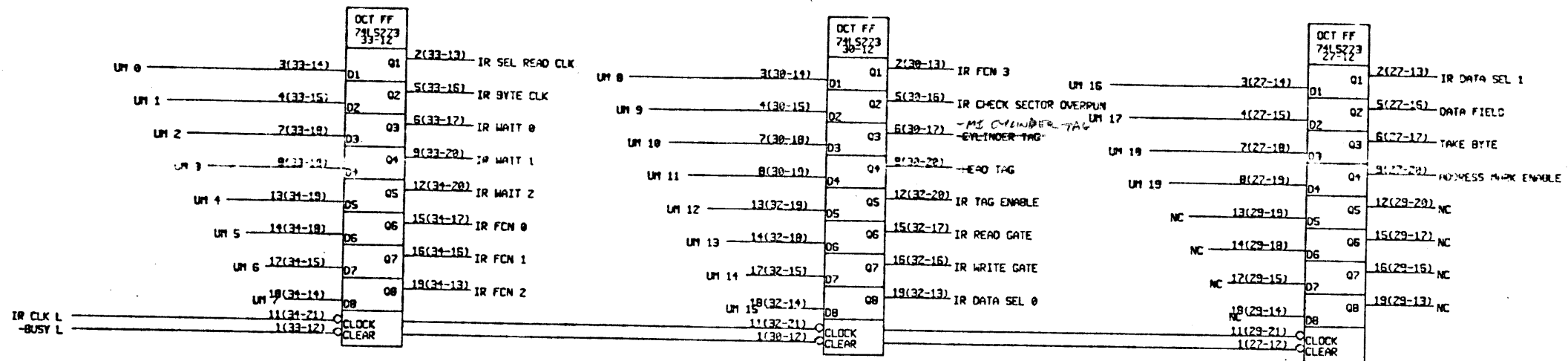
FOONLY, INC.		28-DEC-79 05:47	
DRAWN BY:	PAGE / OF	NUMBER	REV.
APPROVED BY:	PROJECT:		



FOONLY INCORPORATED		20-DEC-79 05:48	
DRAWN BY:		CLKSYN.DRW (4,41)	
APPROVED BY:		PAGE 1 OF 1	NUMBER 3
PROJECT:			REV.

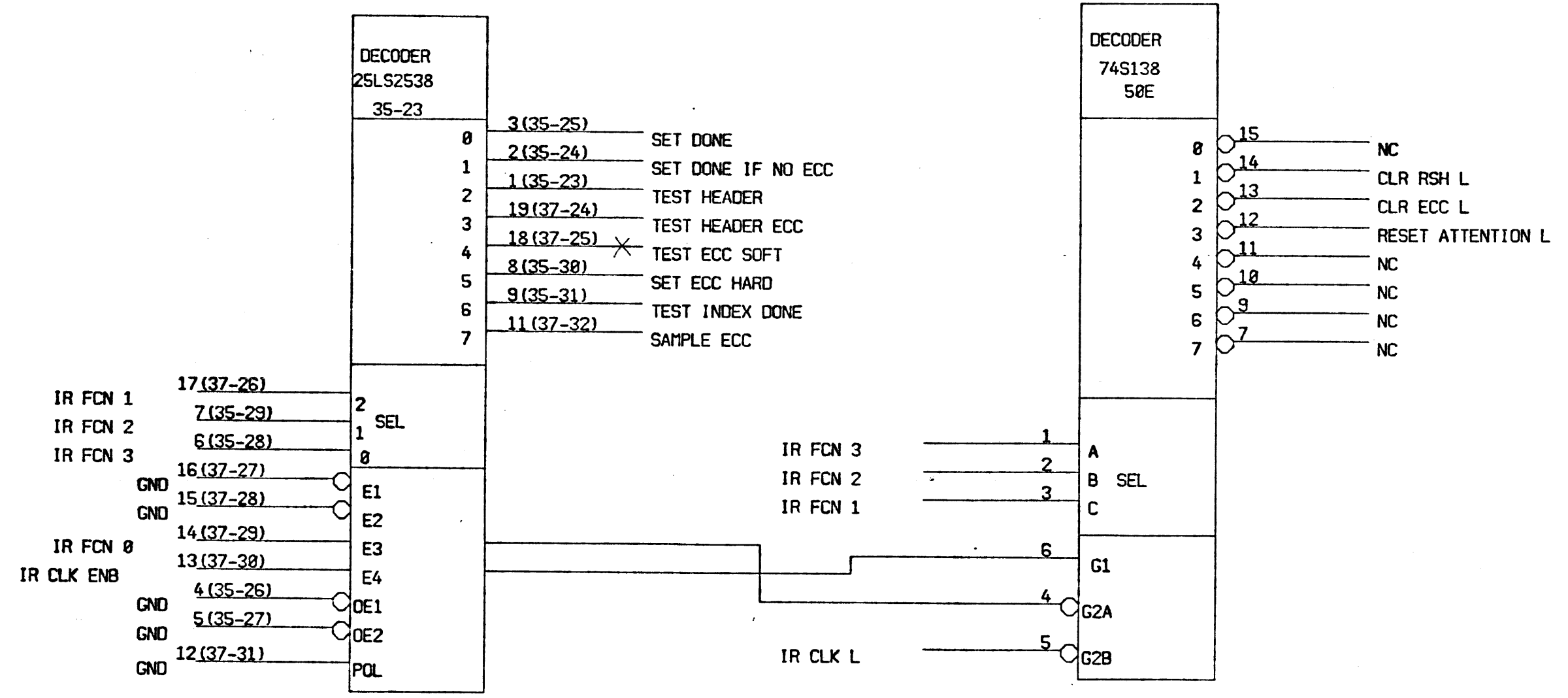
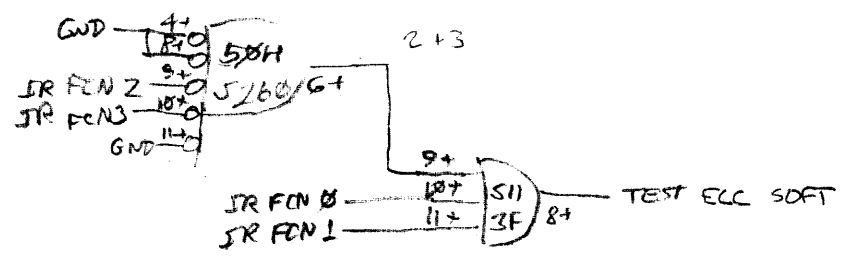


FOONLY INCORPORATED		23-DEC-79 15:31	
DRAWN BY:		RWLOG.DRW(4,41)	
APPROVED BY:		PAGE 1 OF 1	NUMBER REV.
PROJECT:			

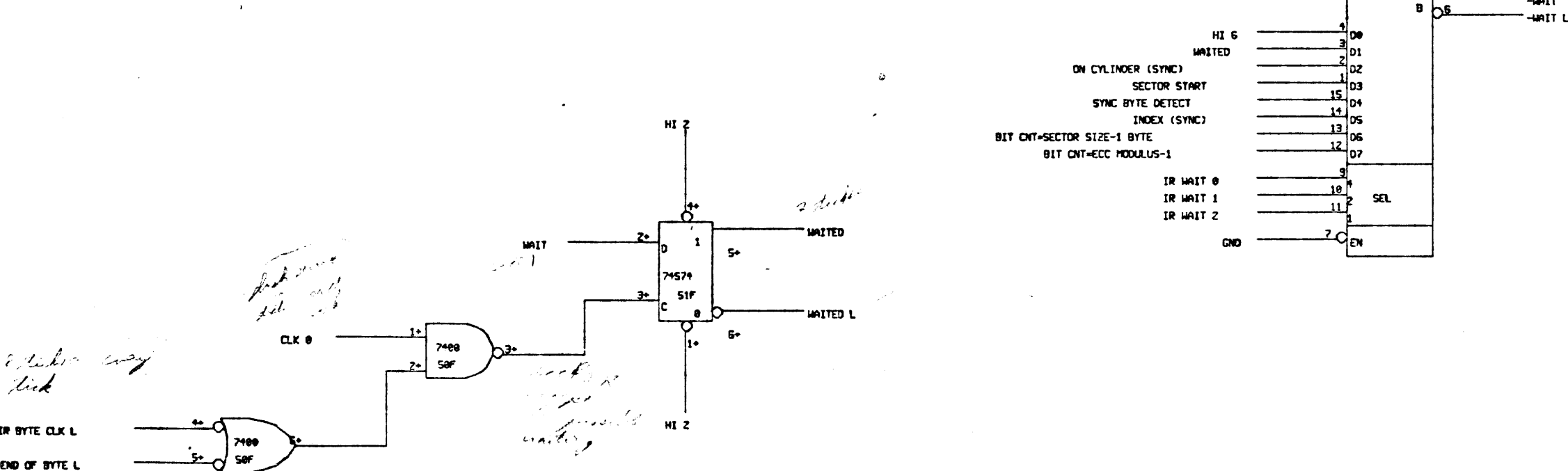
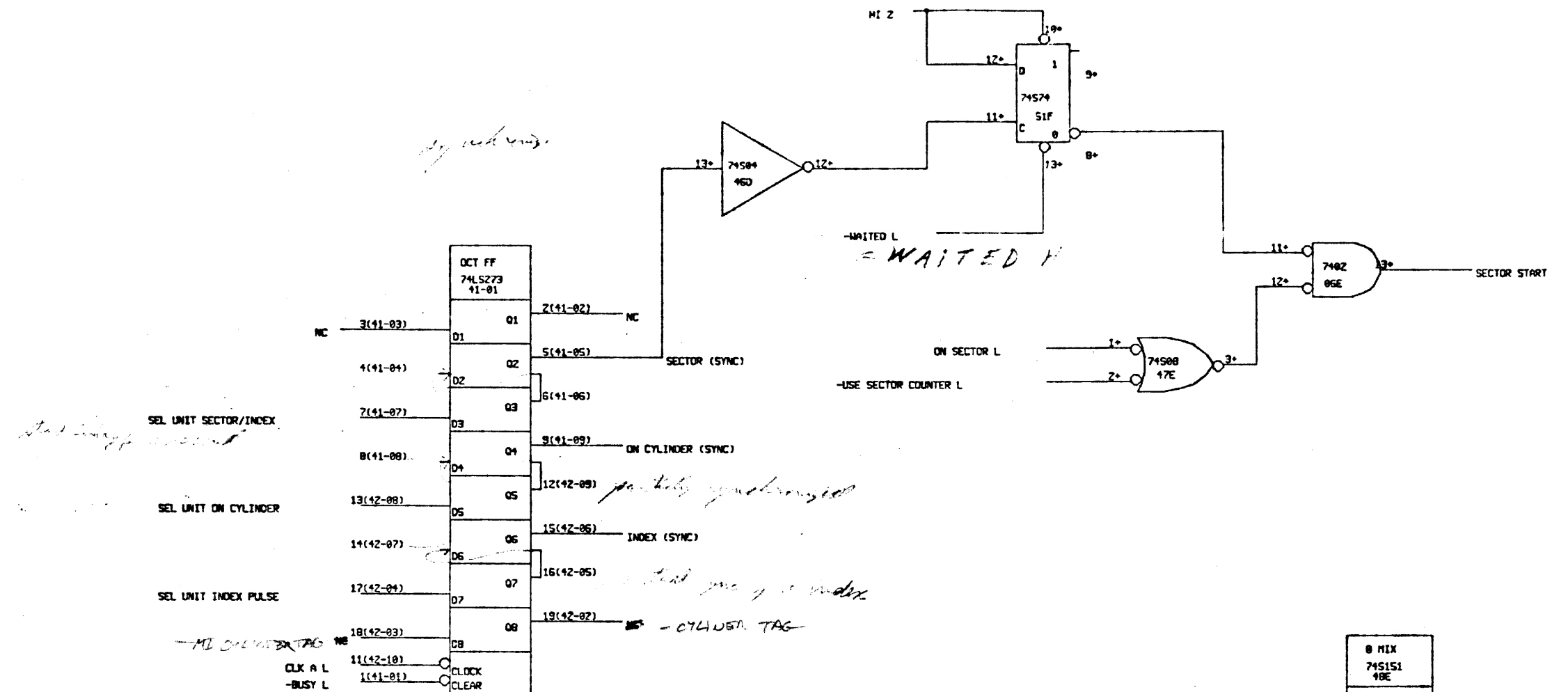


wait while

FOONLY INCORPORATED		<i>These instructions testing micro memory (part 1) 2/1/79</i>		28-DEC-79 05:48	
DRAWN BY:		PAGE 1 OF 1		NUMBER /	
APPROVED BY:		PROJECT:		UFSM.DRW(4,41)	
				REV.	



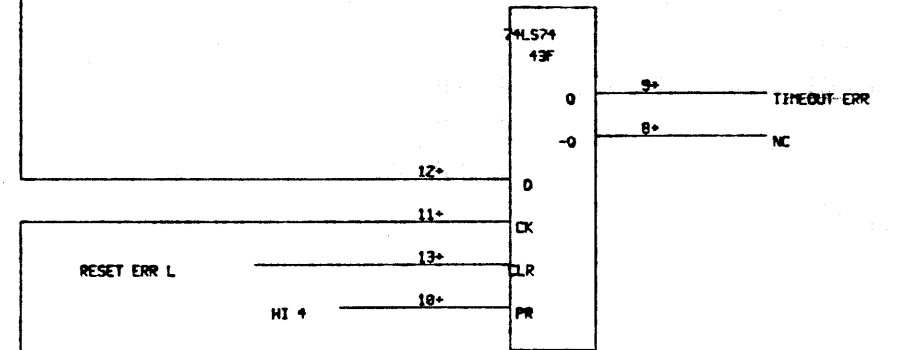
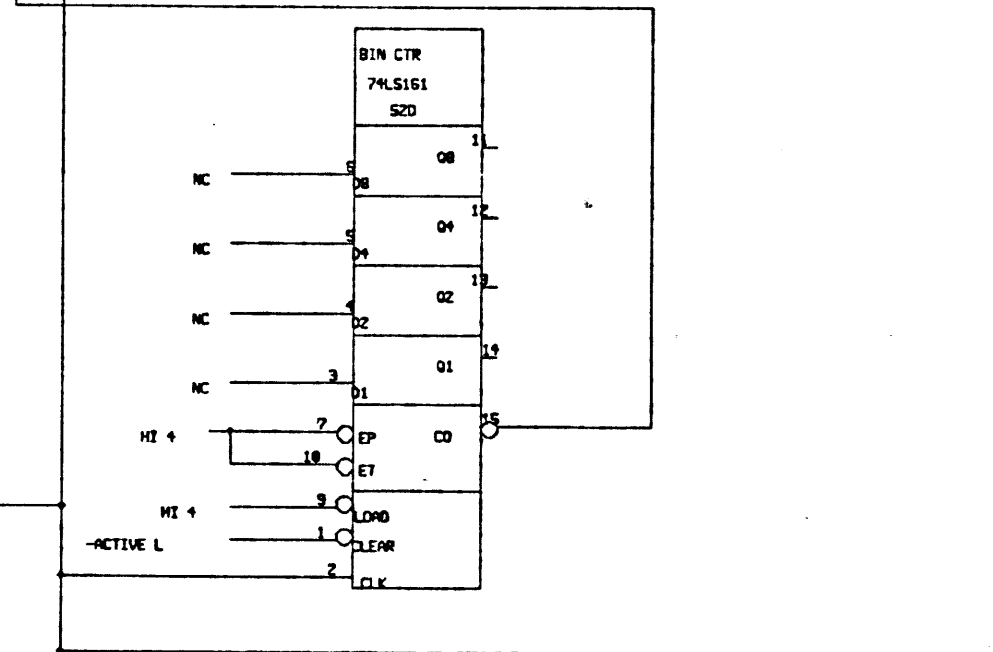
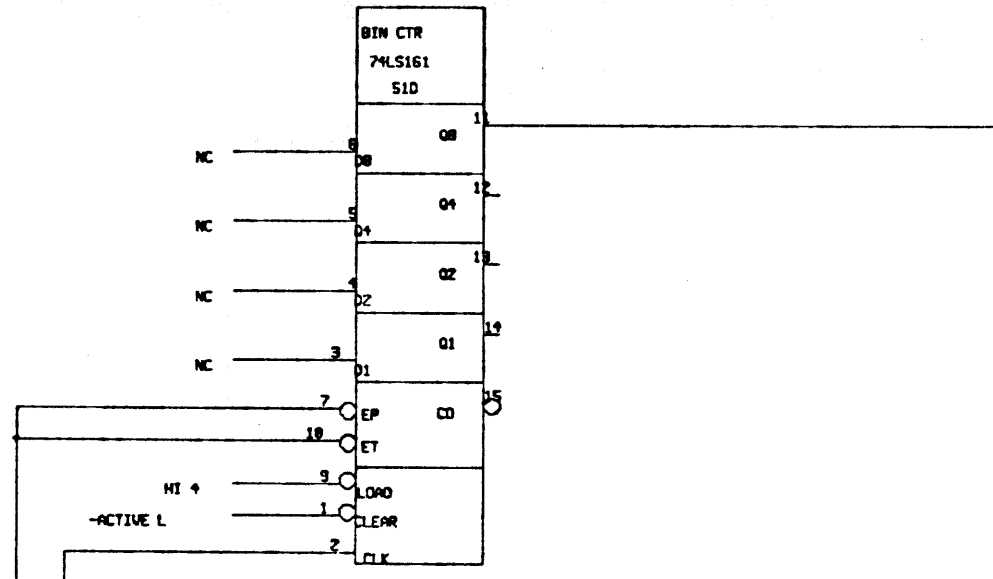
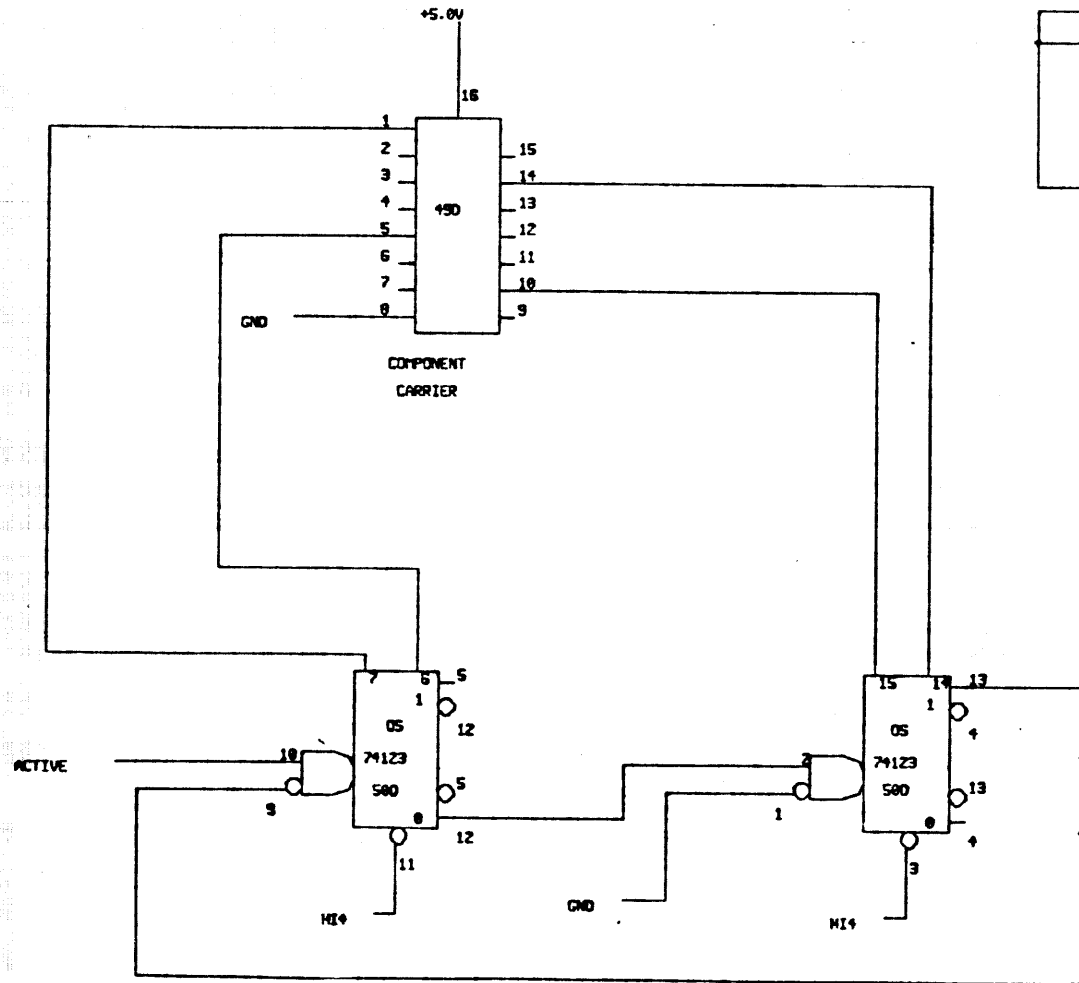
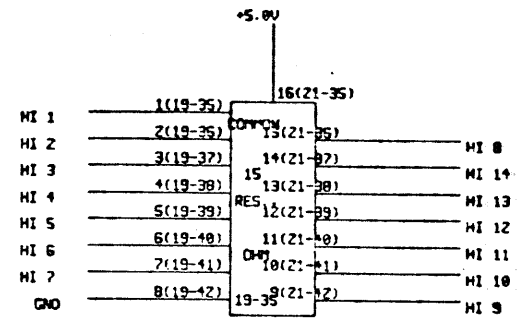
FOONLY INCORPORATED		20-DEC-79 05:48	
		UFUN.DRW (4,41)	
DRAWN BY:	PAGE 1 OF 1	NUMBER 9	REV.
APPROVED BY:	PROJECT:		



Handwritten notes:

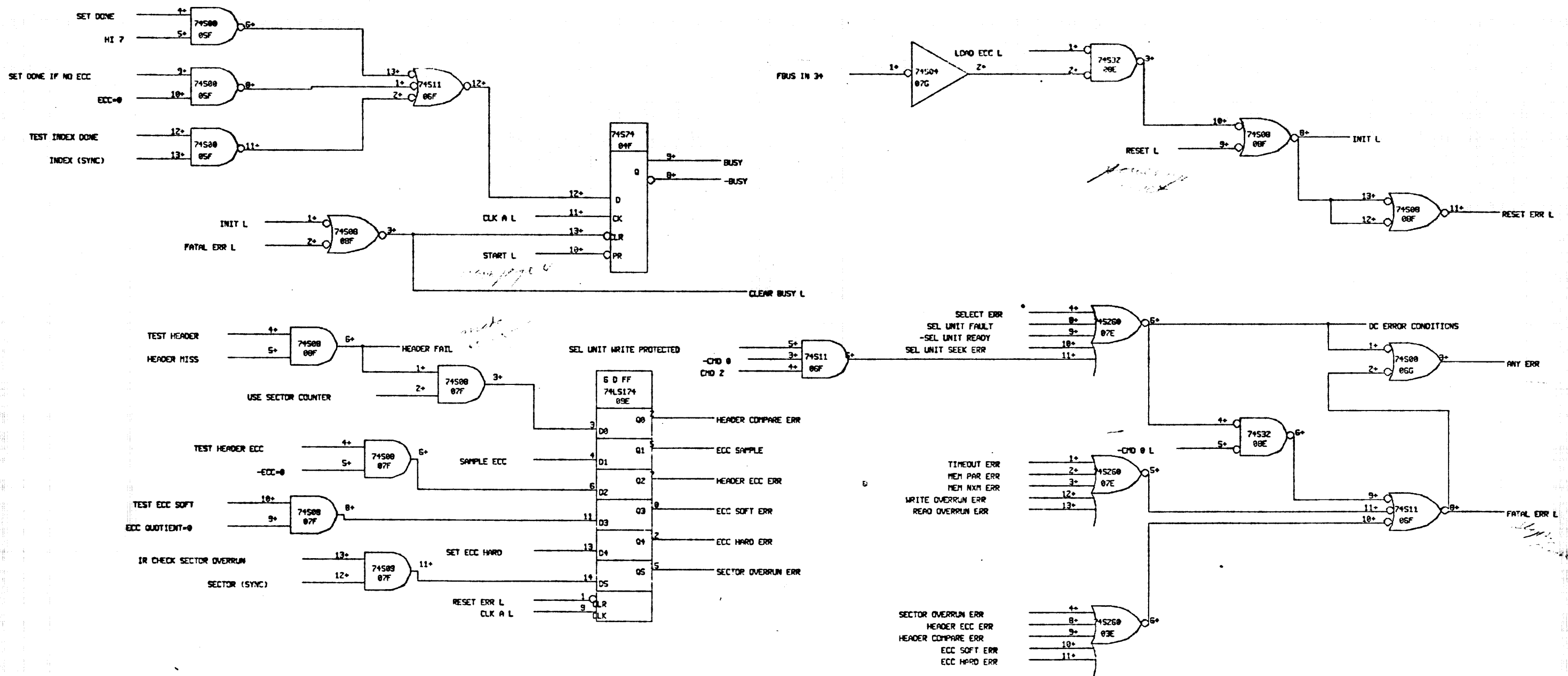
- Top center: *sync*
- Left side: *Start timing circuit*
- Right side: *partially unacknowledged*
- Right side: *used for index*
- Right side: *- CYLINDER TAG*
- Bottom left: *Handwritten note about CLK 0 and END OF BYTE L*
- Bottom center: *Handwritten note about WAIT and WAITED L*

FOONLY INCORPORATED		23-DEC-79 15:27	
DRAWN BY:		UWAIT.DRW (4, 41)	
APPROVED BY:		PAGE 1 OF 1	NUMBER 8
PROJECT:		REV.	



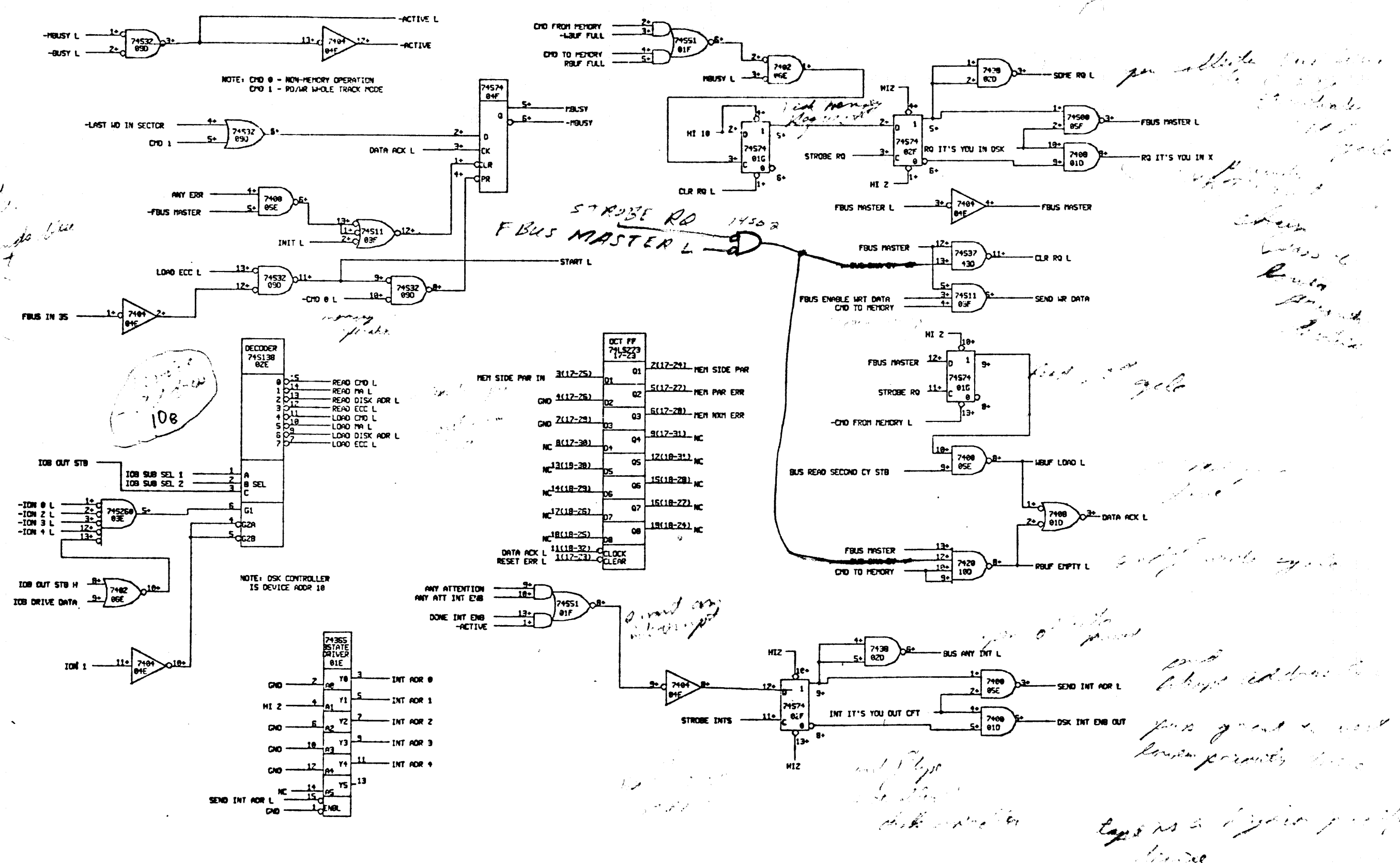
not implemented
look out step 10 in 101
the output is available on the
many options etc.

FOONLY INCORPORATED		23-DEC-79 15:21	
		TIMOUT.DRW [4, 41]	
DRAWN BY:	PAGE 1 / OF 1	NUMBER 12	REV.
APPROVED BY:	PROJECT:		



Handwritten note: The error codes are all from the 74511.

FOONLY INCORPORATED		28-DEC-79 05:49	
		ERRORS.DRW (4, 41)	
DRAWN BY:	PAGE 1 OF 1	NUMBER 6	REV.
APPROVED BY:	PROJECT:		



LOAD ECC
 Memory Load
 just need to
 read back
 from disk
 CPU control line

108

STROBE RD
 FBUS MASTER L

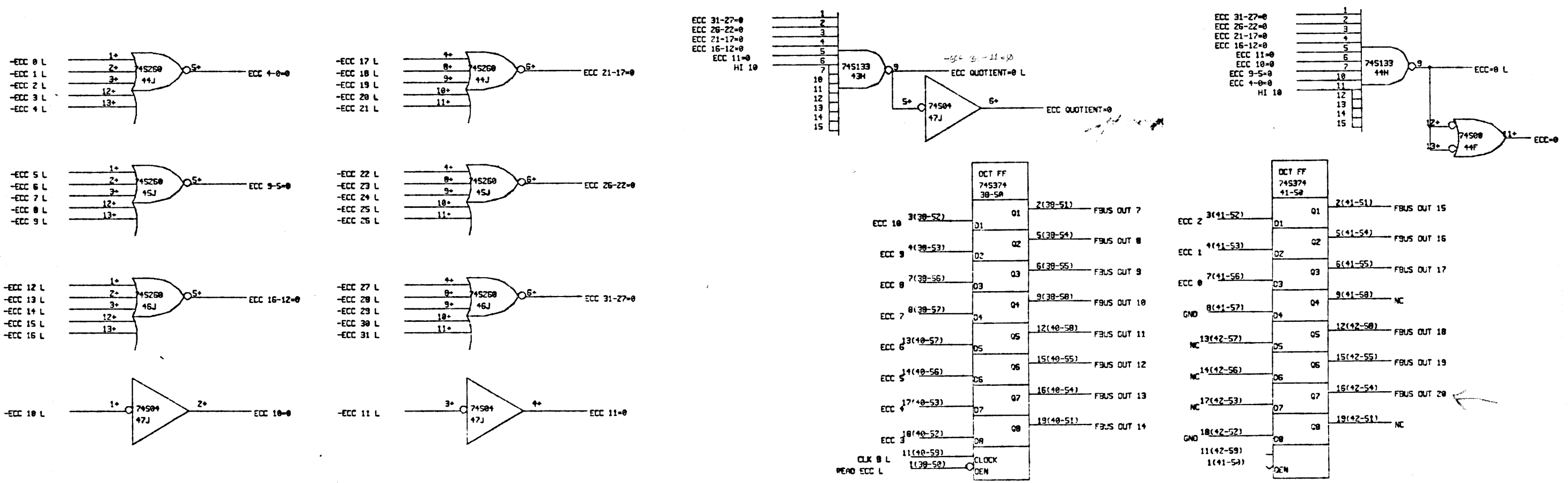
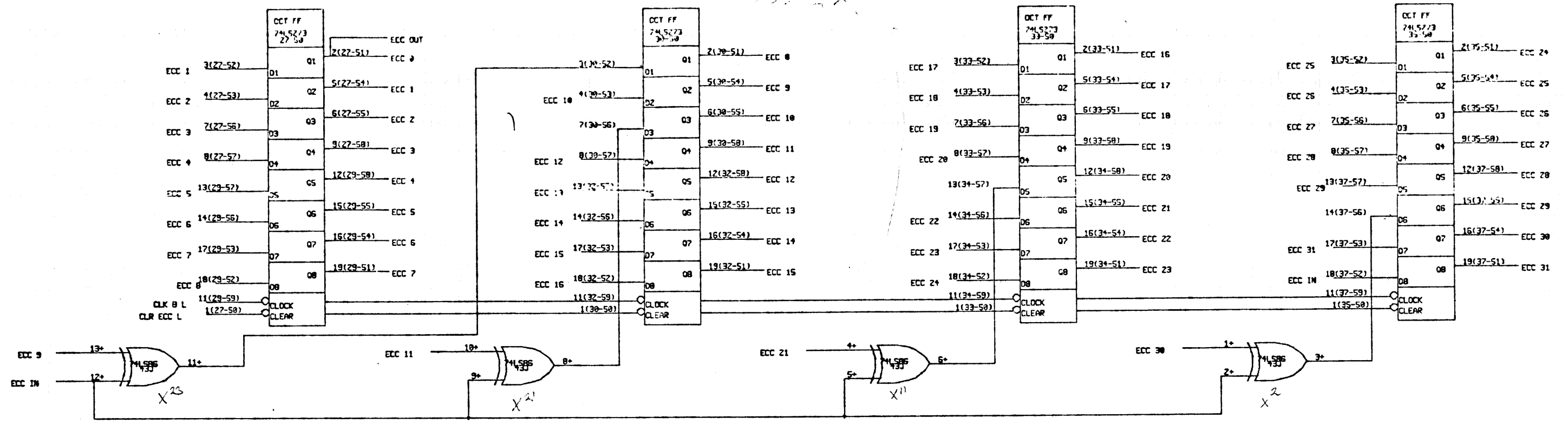
MEM SIDE PAR IN 3(12-25)		OCT FF 74579 17-23	
01	2(12-24)	01	MEM SIDE PAR
02	5(12-27)	02	MEM PAR ERR
03	6(12-28)	03	MEM NRM ERR
04	9(12-31)	04	NC
05	12(18-34)	05	NC
06	15(18-37)	06	NC
07	16(18-38)	07	NC
08	18(18-40)	08	NC
09	11(18-32)	09	CLOCK CLEAR
10	11(18-32)	10	DATA ACK L
11	11(18-32)	11	RESET ERR L

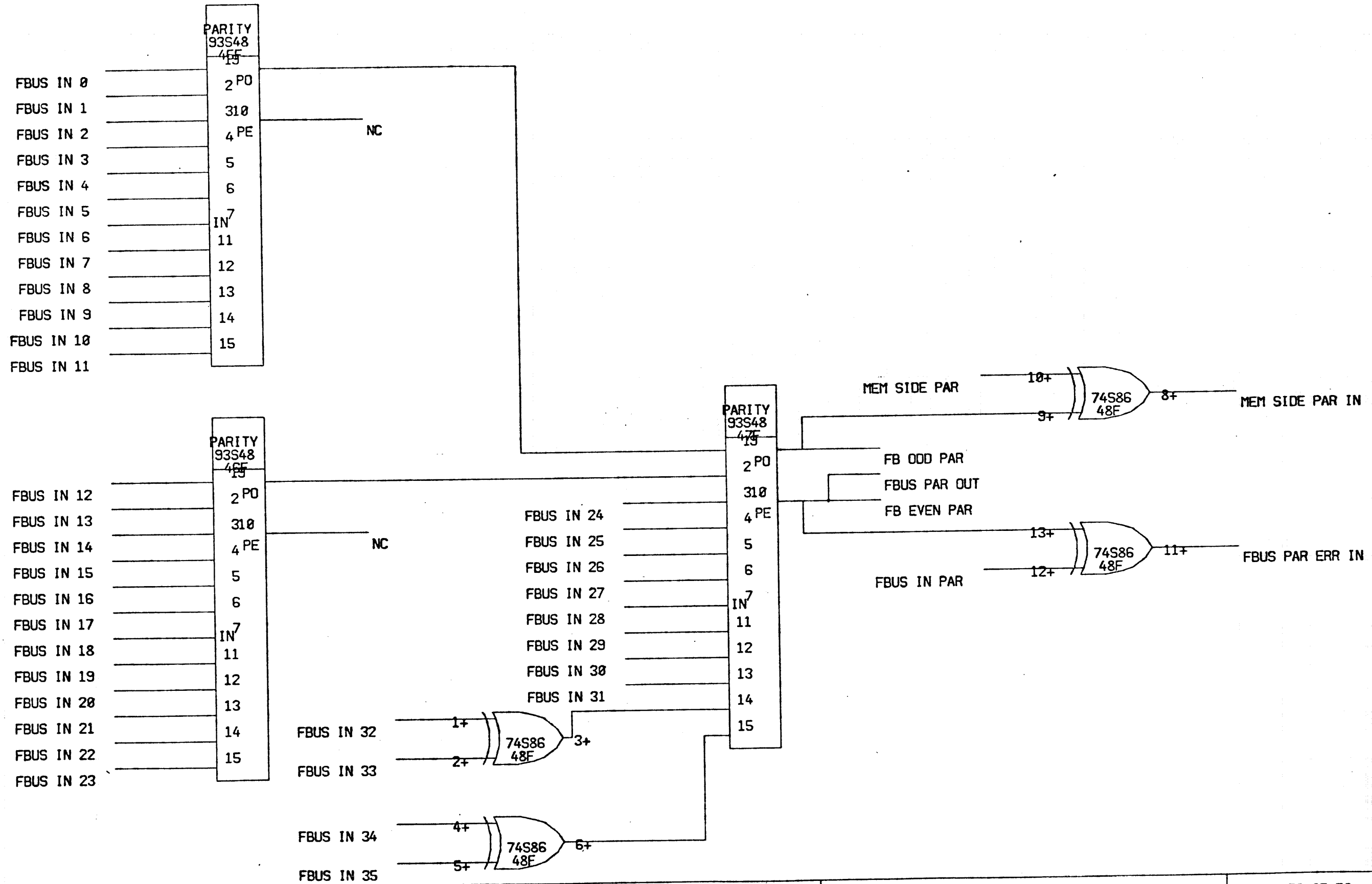
NOTE: DISK CONTROLLER IS DEVICE ADDR 18

ANY ATTENTION
 ANY ATT INT ENB
 DONE INT ENB
 -ACTIVE

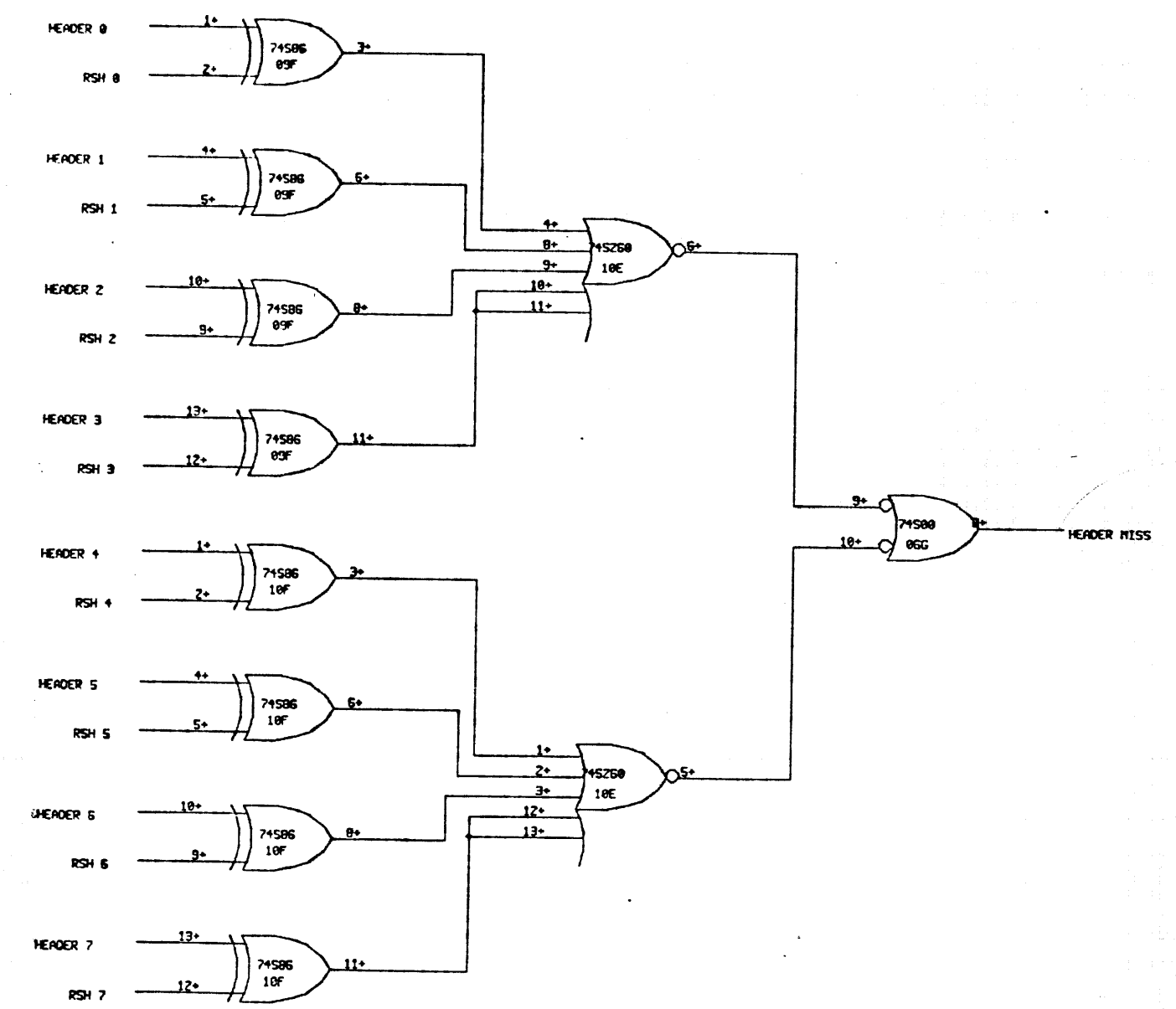
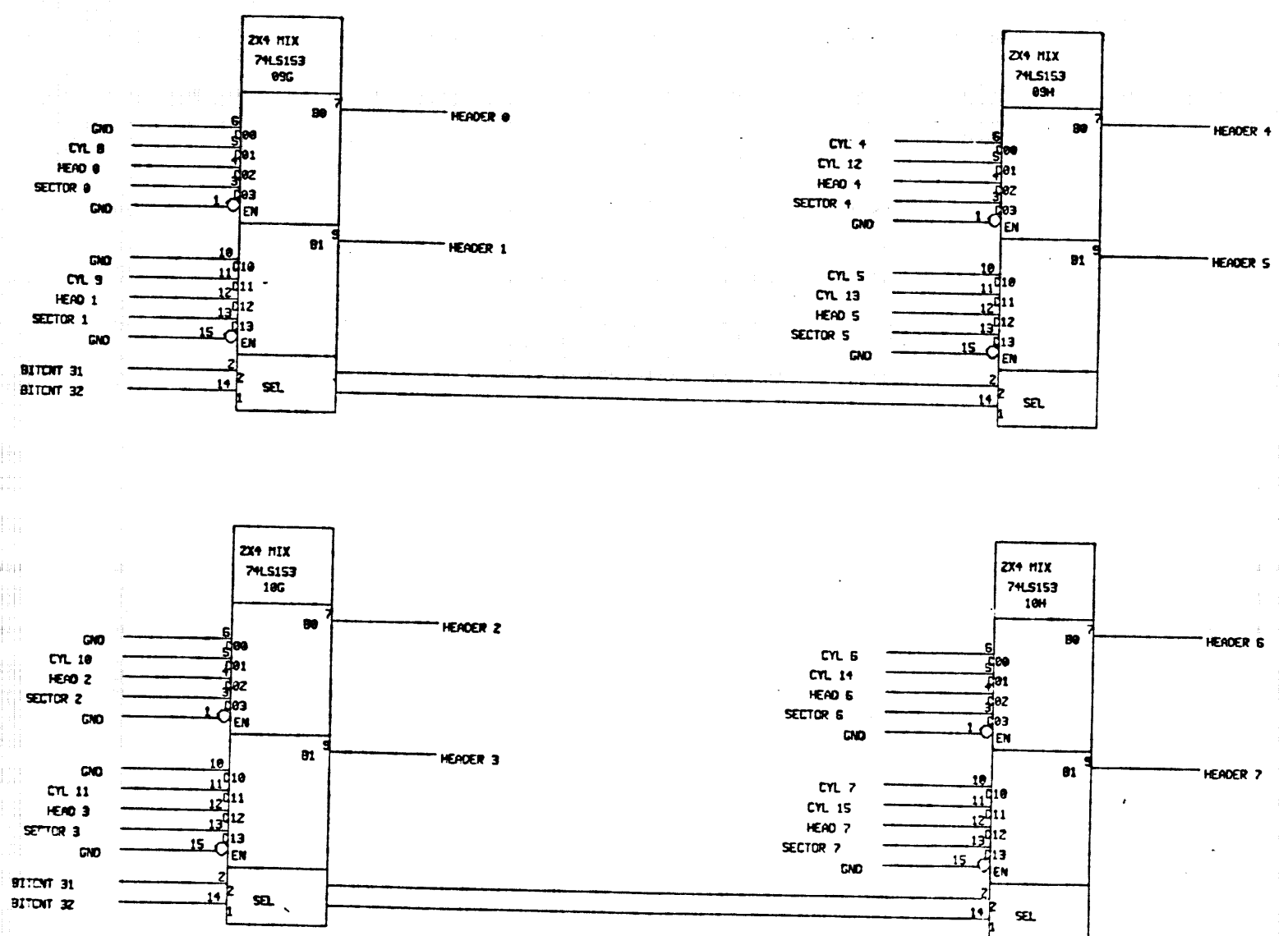
74365 BISTATE DRIVER 01E	
2	Y0
4	Y1
6	Y2
10	Y3
12	Y4
14	Y5
15	ENL

you should have done
 this
 check
 bus read second cycle
 and about address
 bus grant to read
 lower priority data
 tape is a higher priority
 line

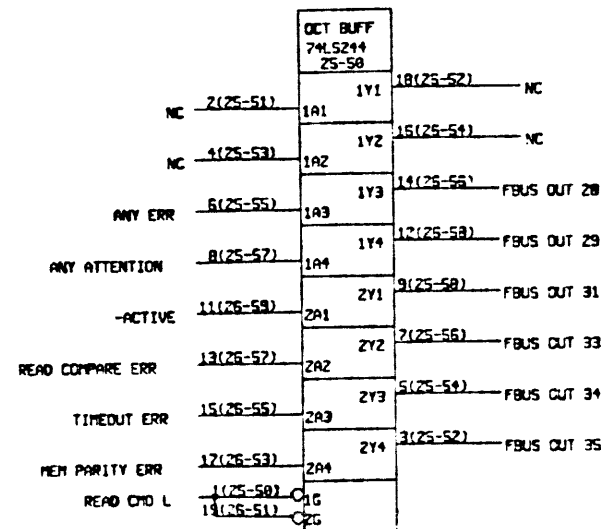
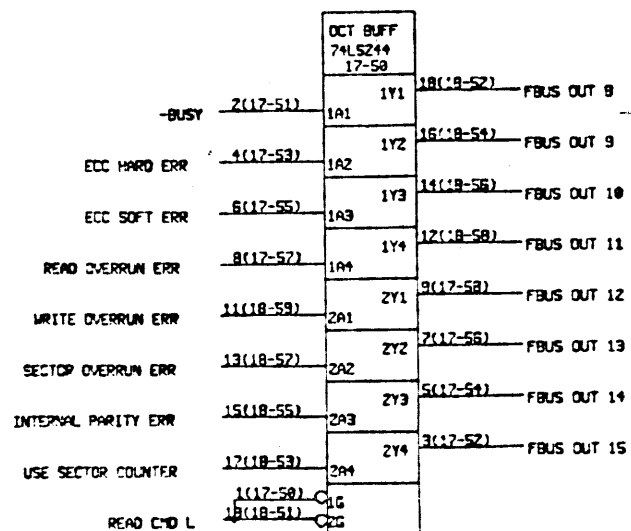
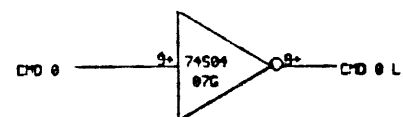
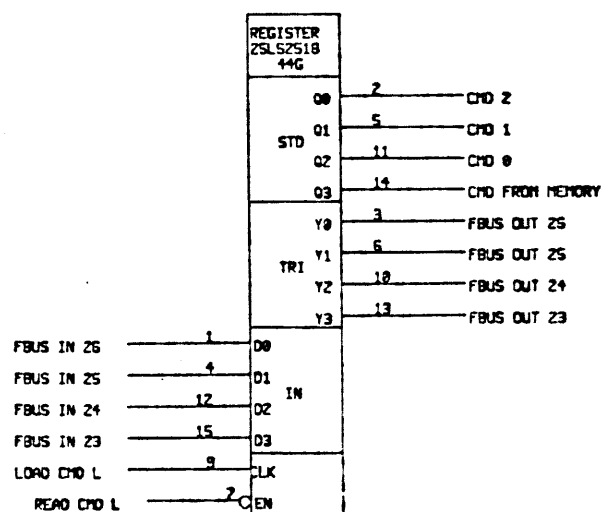
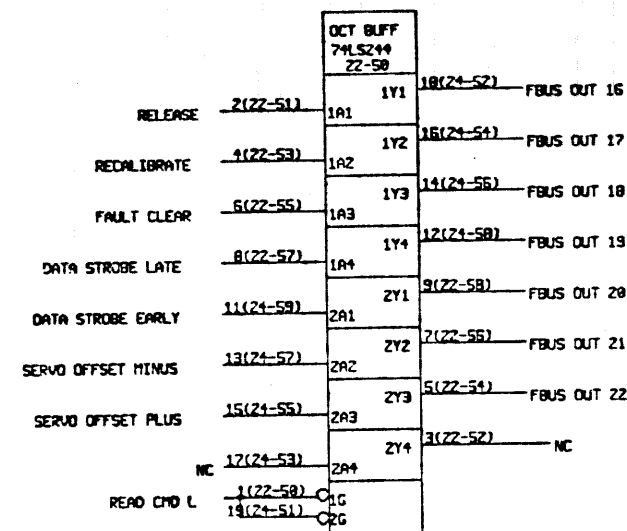
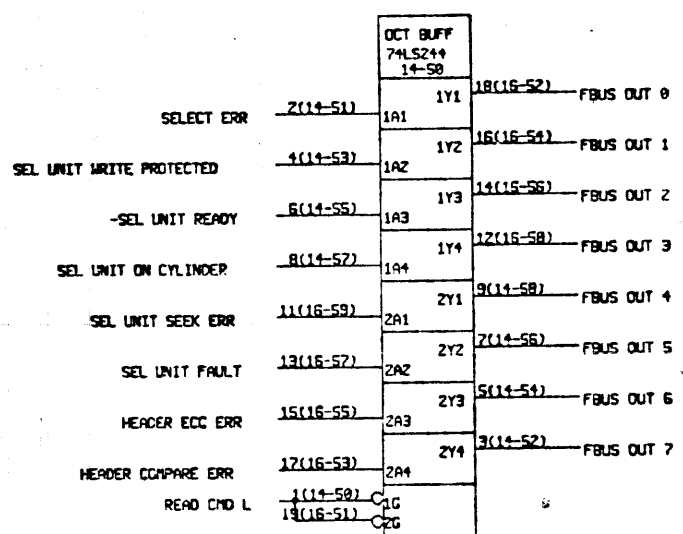
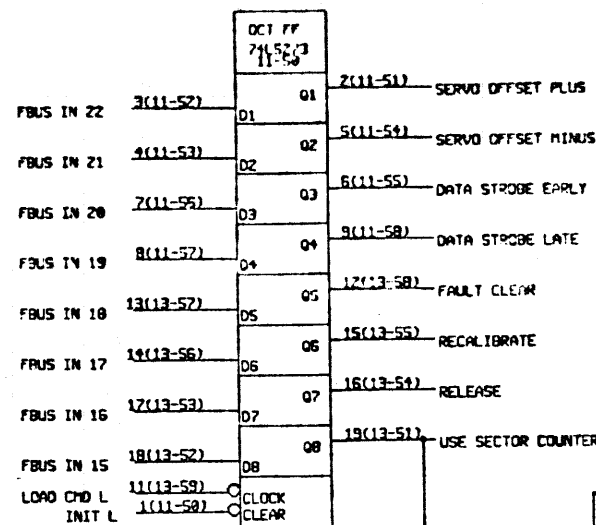
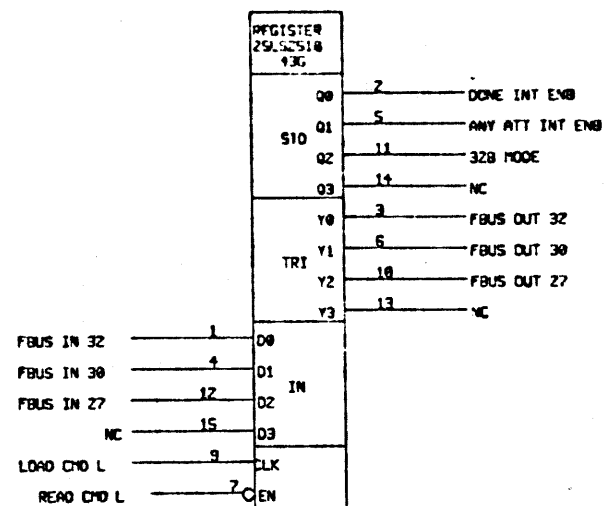




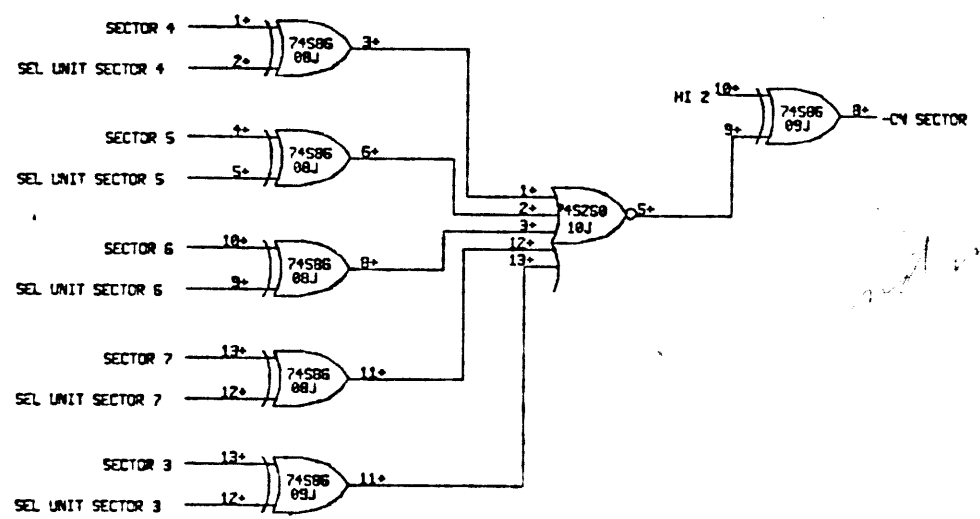
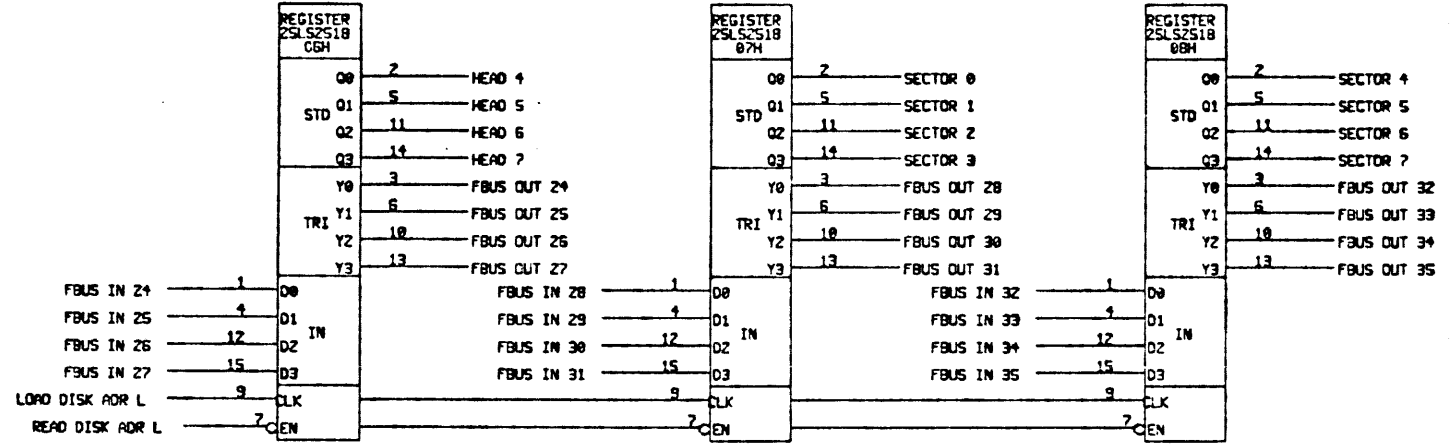
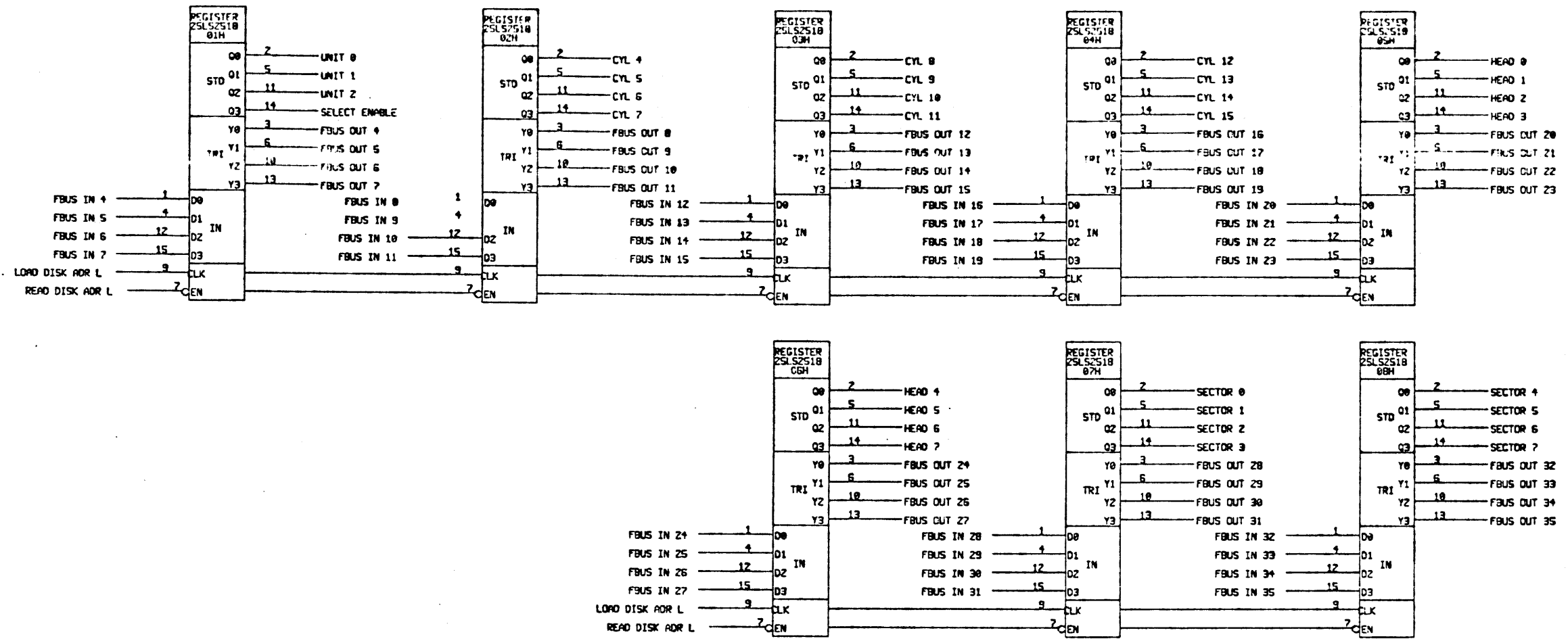
FOONLY INCORPORATED		20-DEC-79 05:50	
		PARITY.DRW(4,41)	
DRAWN BY:	PAGE 1 OF 1	NUMBER 2	REV.
APPROVED BY:	PROJECT:		0



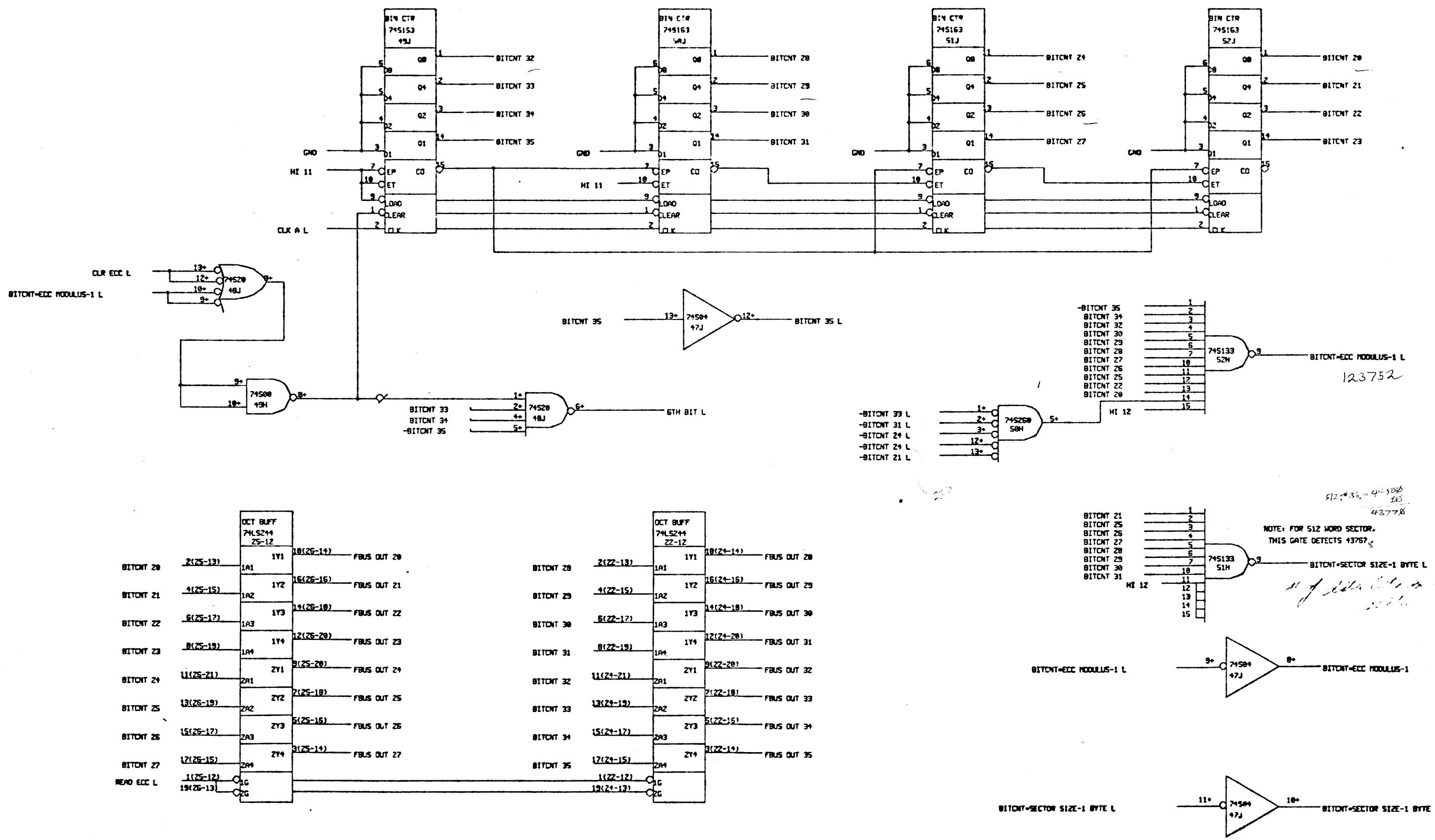
FOONLY INCORPORATED		28-DEC-79 05:50	
		HDCOMP.DRW(4,41)	
DRAWN BY:	PAGE 1 OF 1	NUMBER	REV.
APPROVED BY:	PROJECT:		



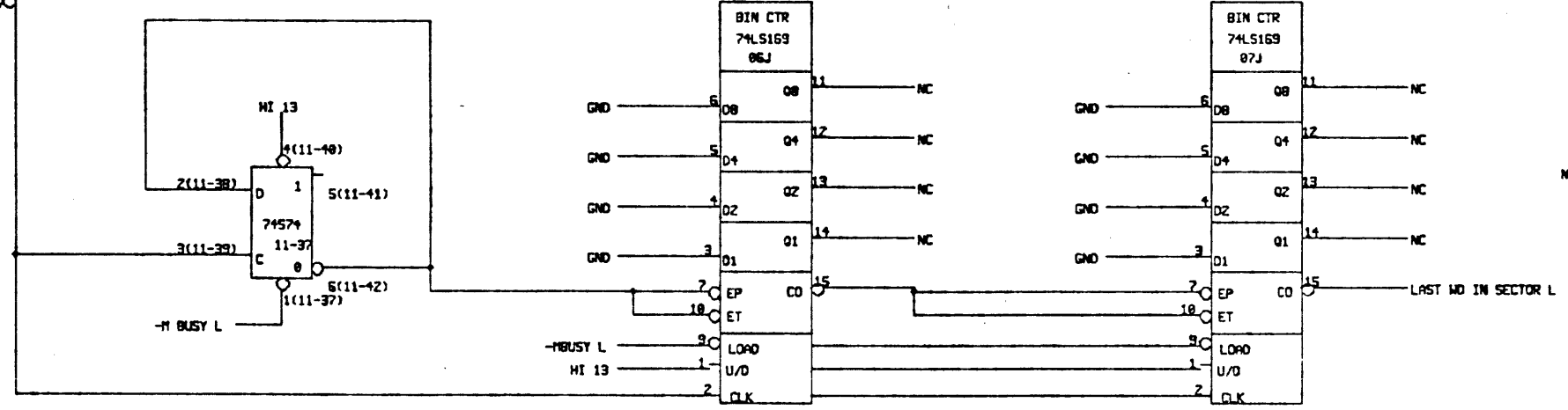
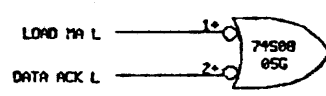
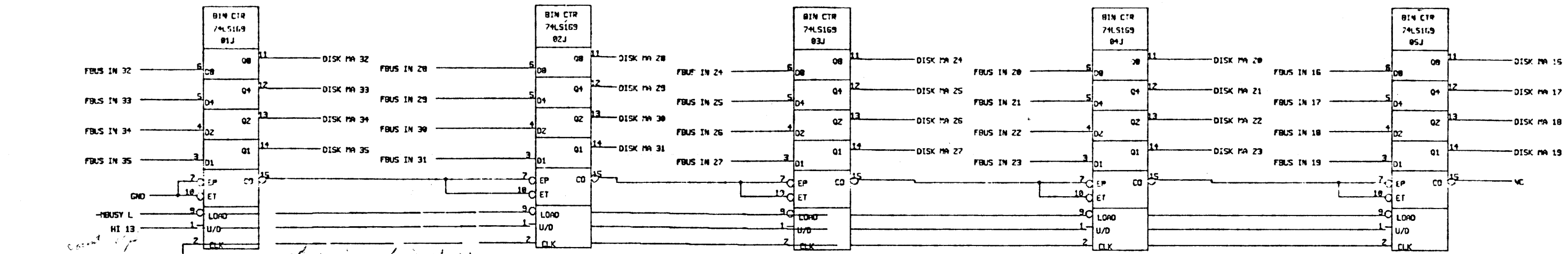
FOONLY INCORPORATED		23-DEC-79 15:32	
DRAWN BY:		CSREG.DRW(4,41)	
APPROVED BY:		PAGE 1 OF 1	NUMBER 5
		PROJECT:	REV. 0



FOONLY INCORPORATED		<i>Disk Address Register</i>		20-DEC-79 05:51
DRAWN BY:		PAGE 1 OF 1	NUMBER	REV.
APPROVED BY:		PROJECT:	OSKADR.DRW (4,41)	

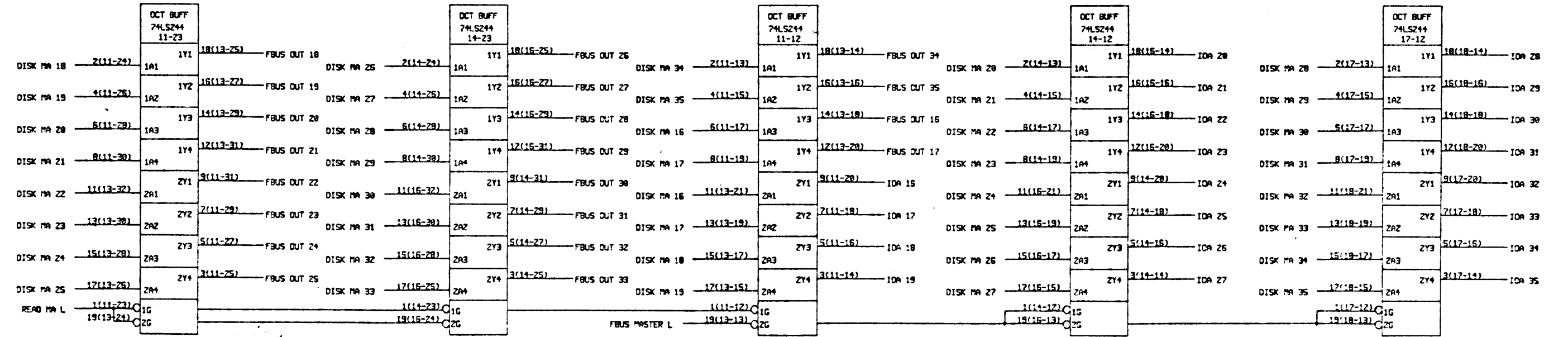


FOONLY INCORPORATED		23-DEC-79 15:34	
		BITCNT.DRW(4,41)	
DRAWN BY:	PAGE 1 OF 1	NUMBER	REV.
APPROVED BY:	PROJECT:		



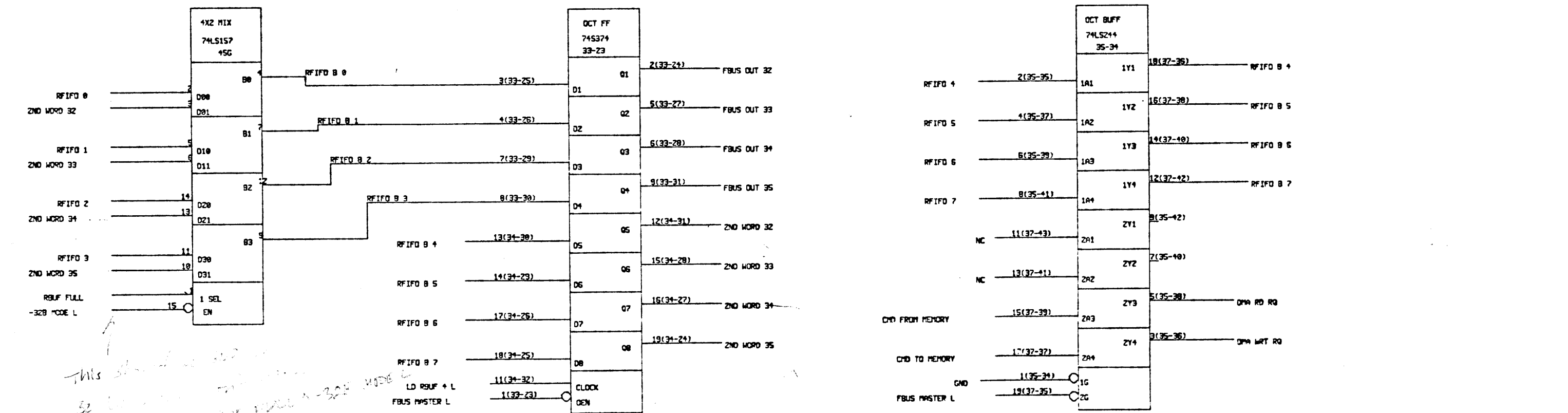
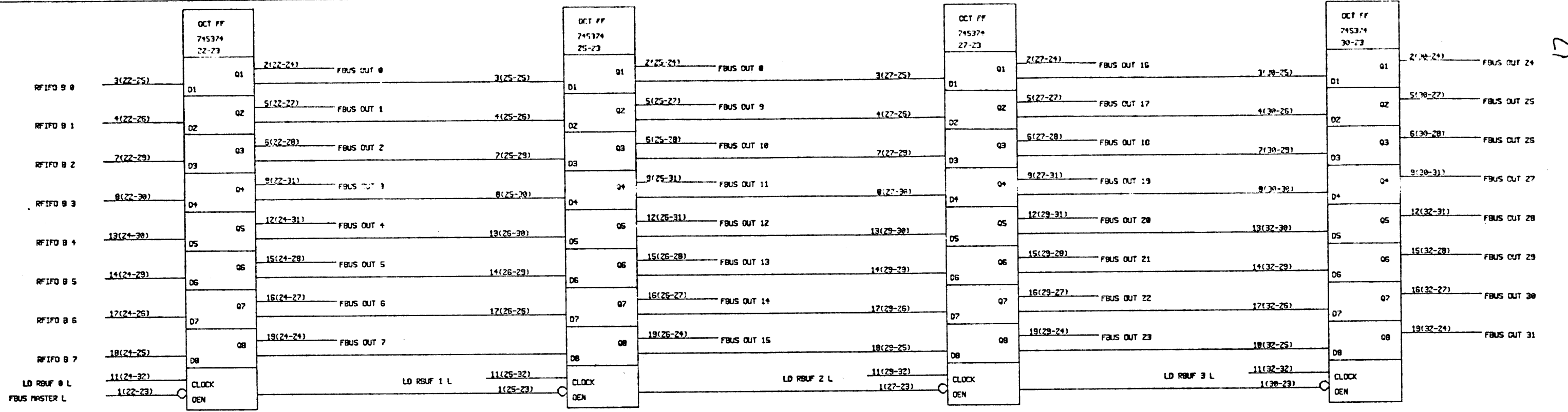
NOTE: COUNTS TO 511 FOR A 512 MD SECTOR SIZE

Handwritten notes: and to clear the 10 8 4 2 1



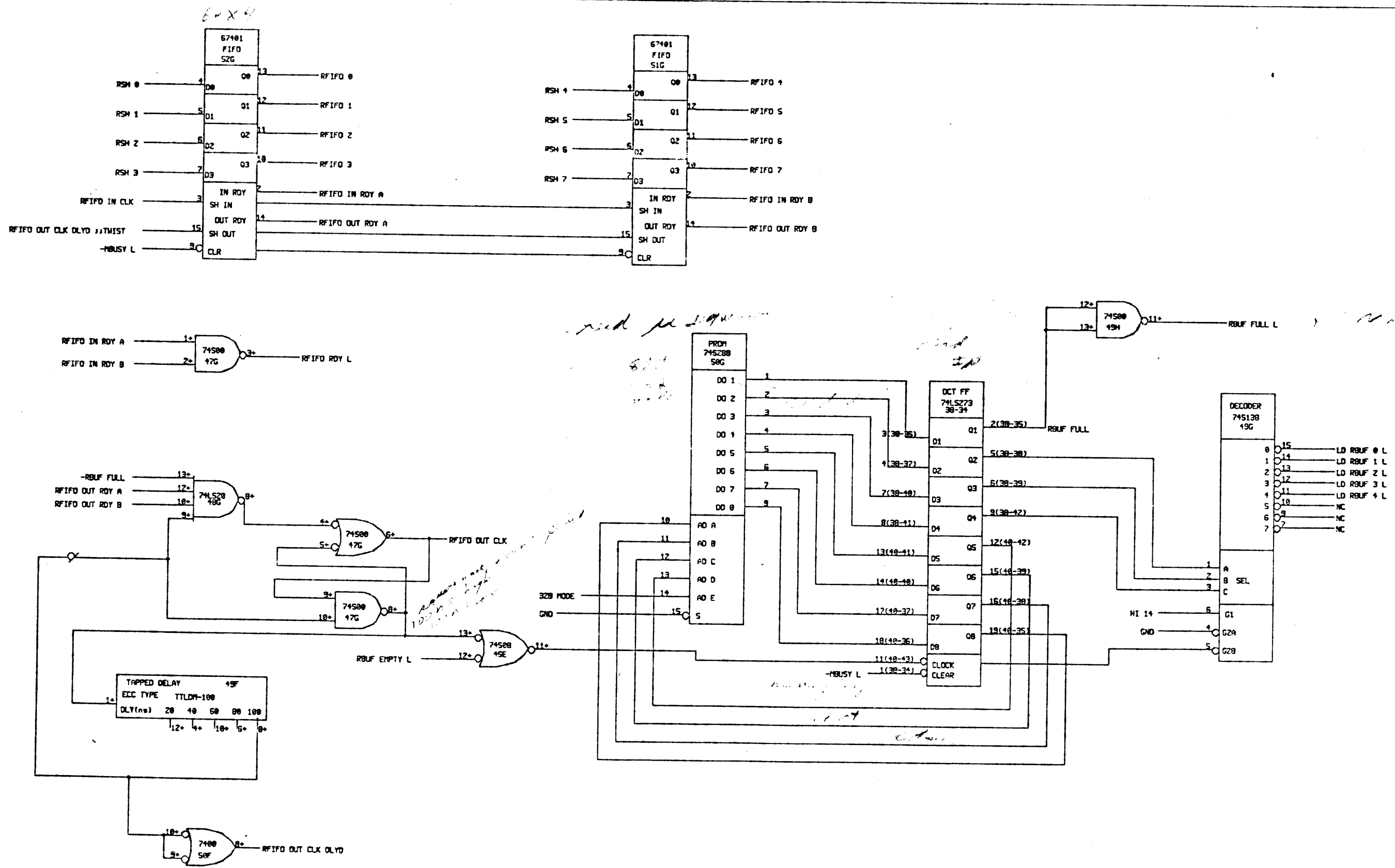
Handwritten note: do not

FOONLY INCORPORATED		20-DEC-79 05:51	
		DSKMA.DRW [4, 41]	
DRAWN BY:	PAGE 1 OF 1	NUMBER	REV.
APPROVED BY:	PROJECT:		

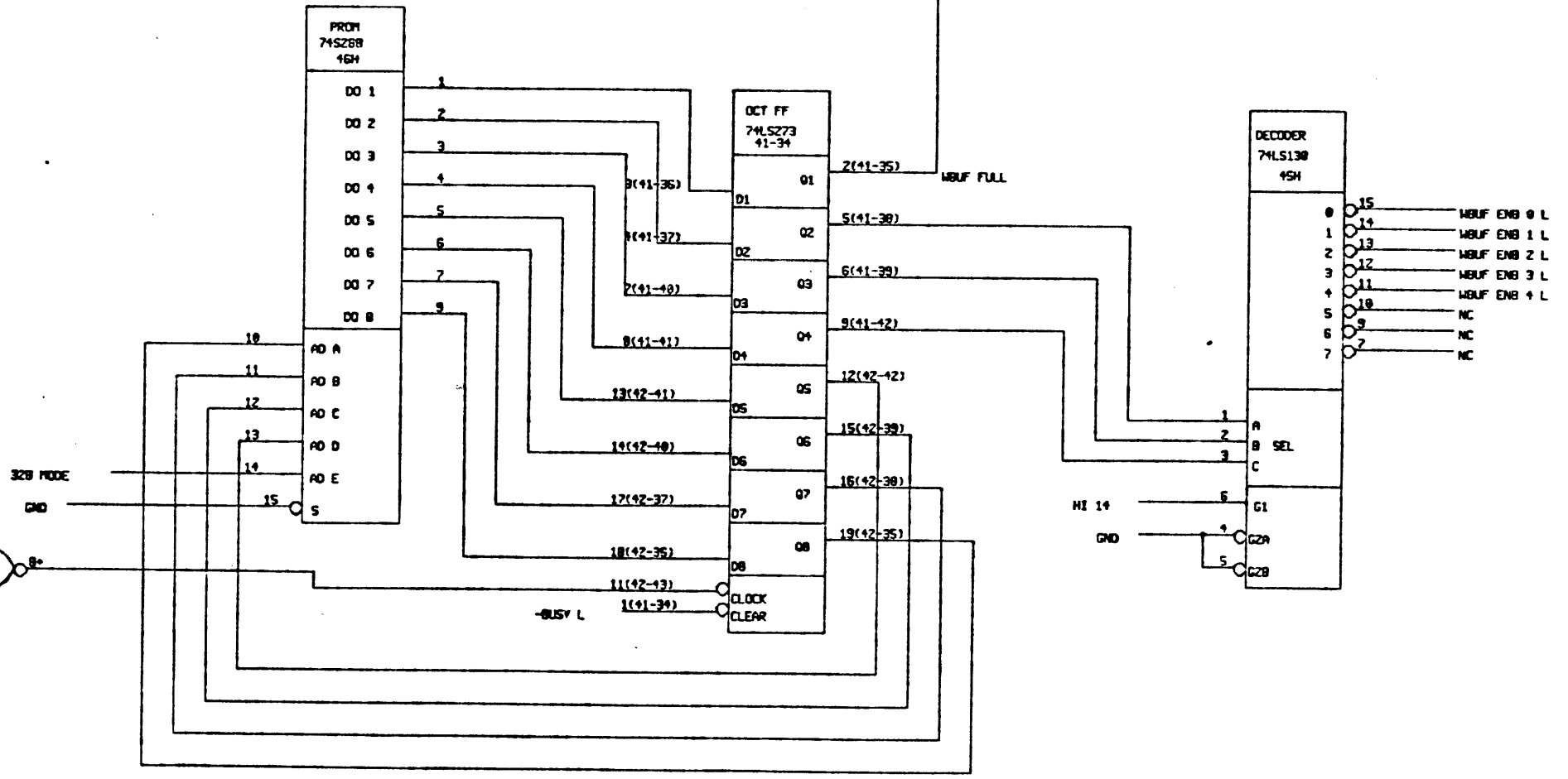
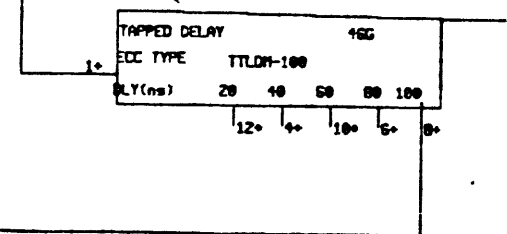
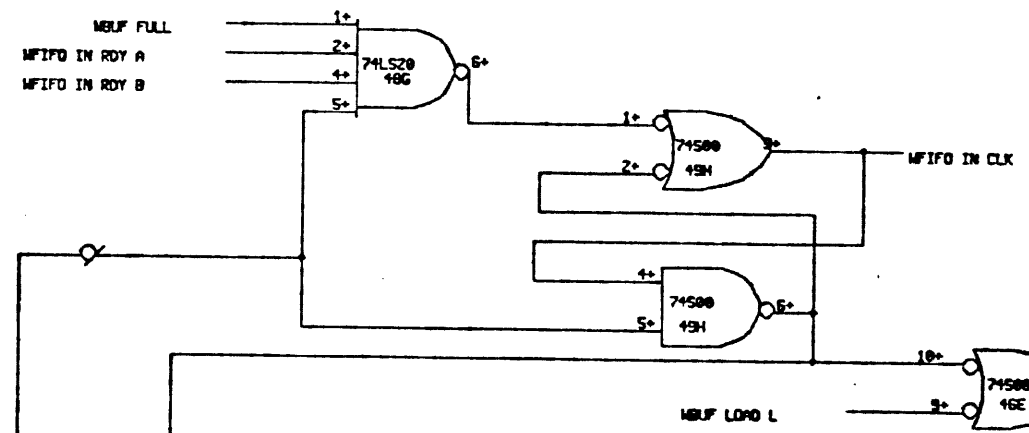
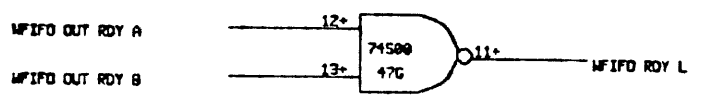
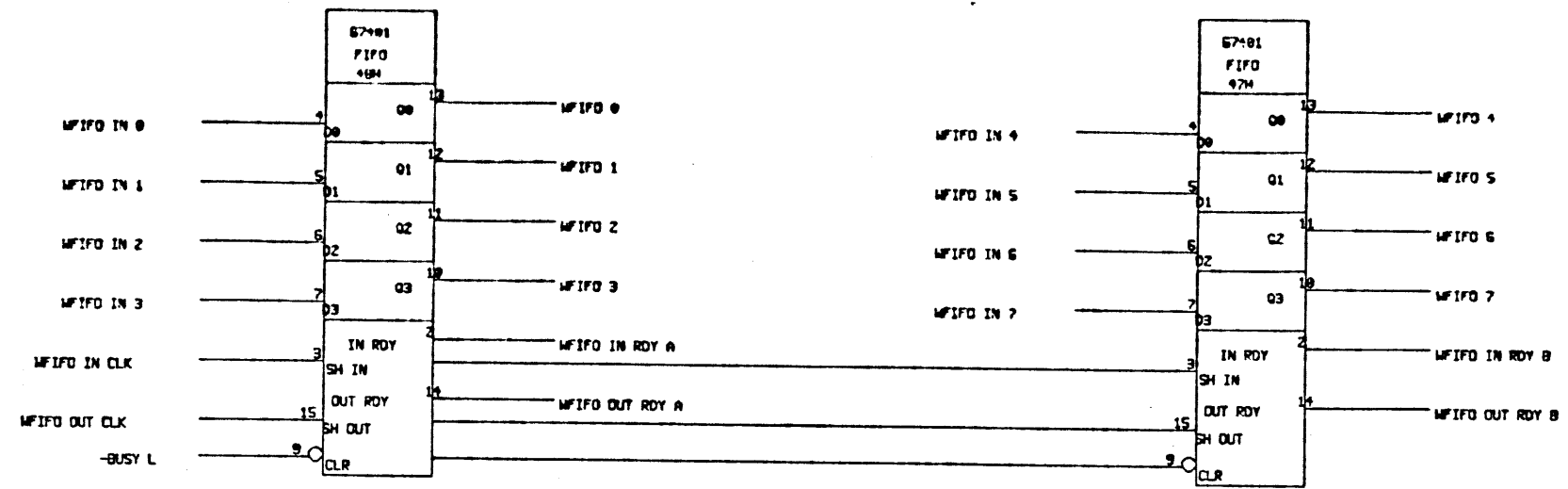


THIS should be 100%
 32 MODE L
 see also to RBUF FULL -32B MODE L

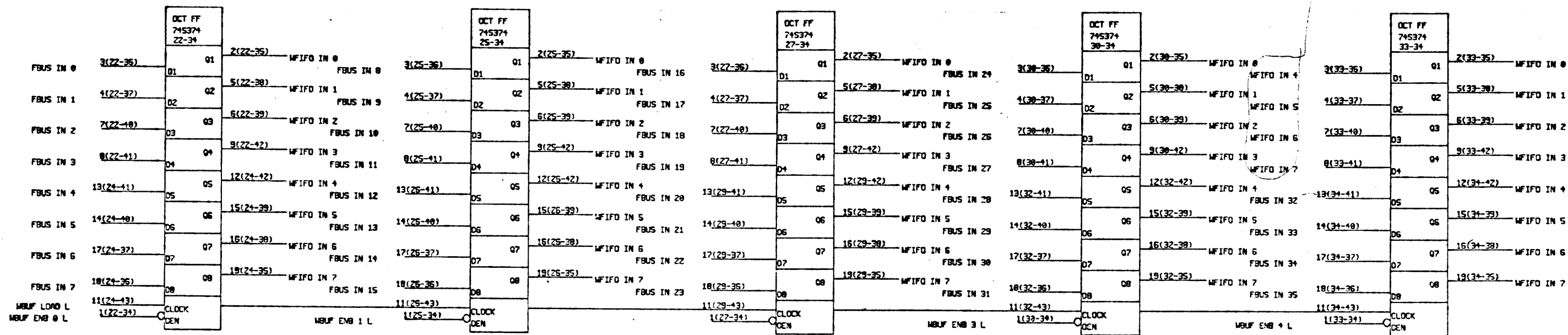
FOONLY INCORPORATED		20-DEC-79 05:52	
		RBUF.DRW [4,41]	
DRAWN BY:	PAGE 1 OF 1	NUMBER 1	REV.
APPROVED BY:	PROJECT:		0



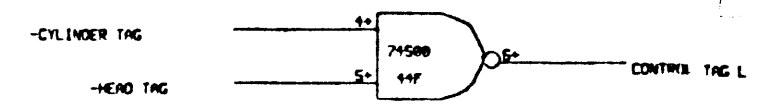
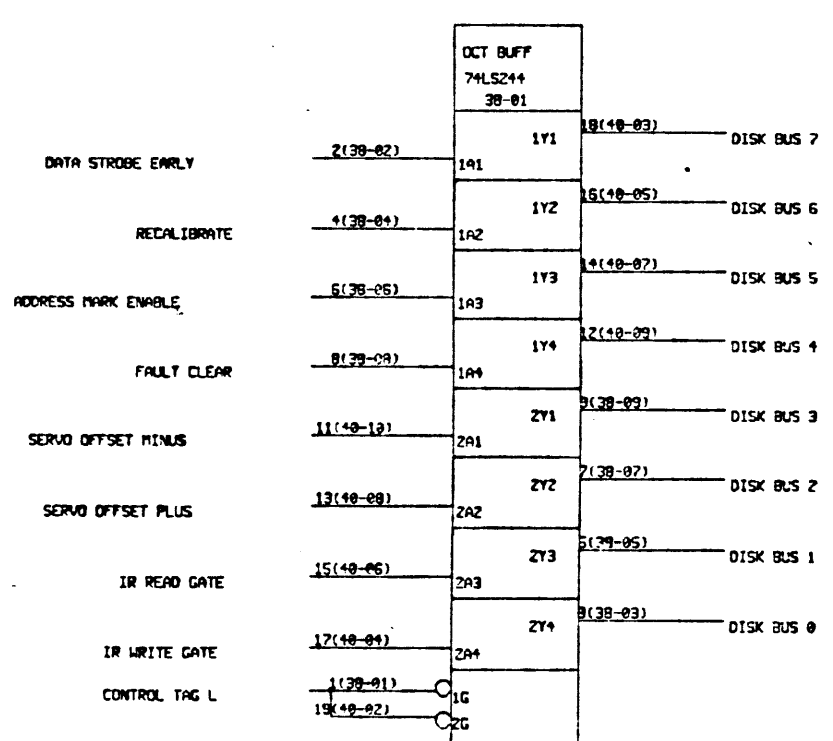
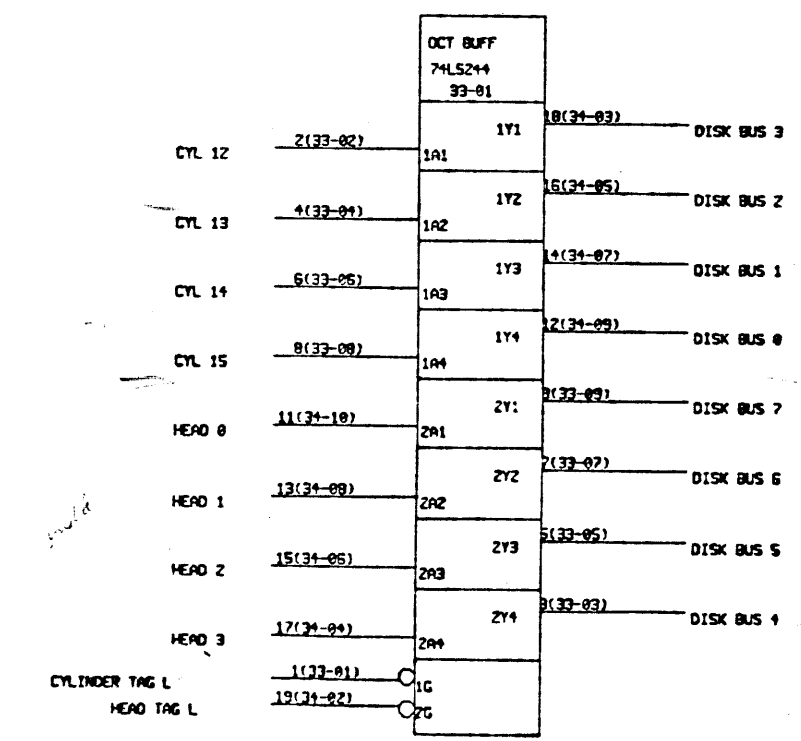
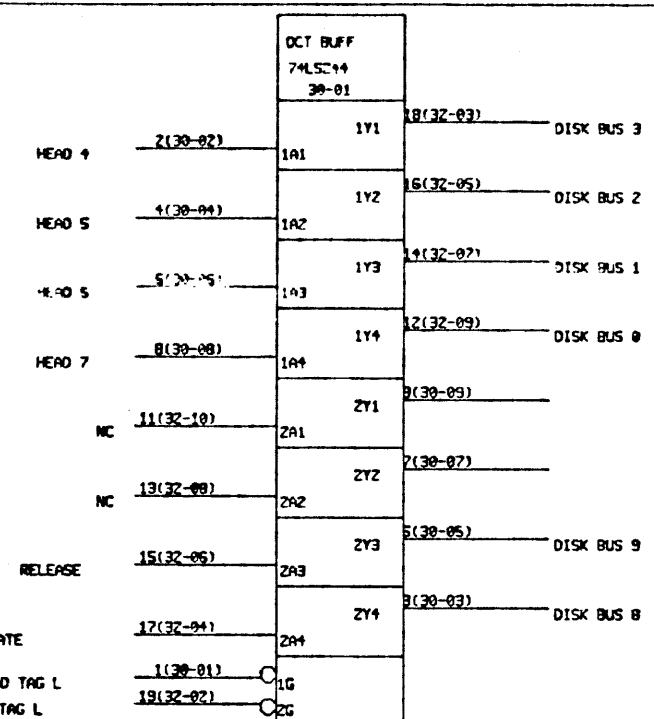
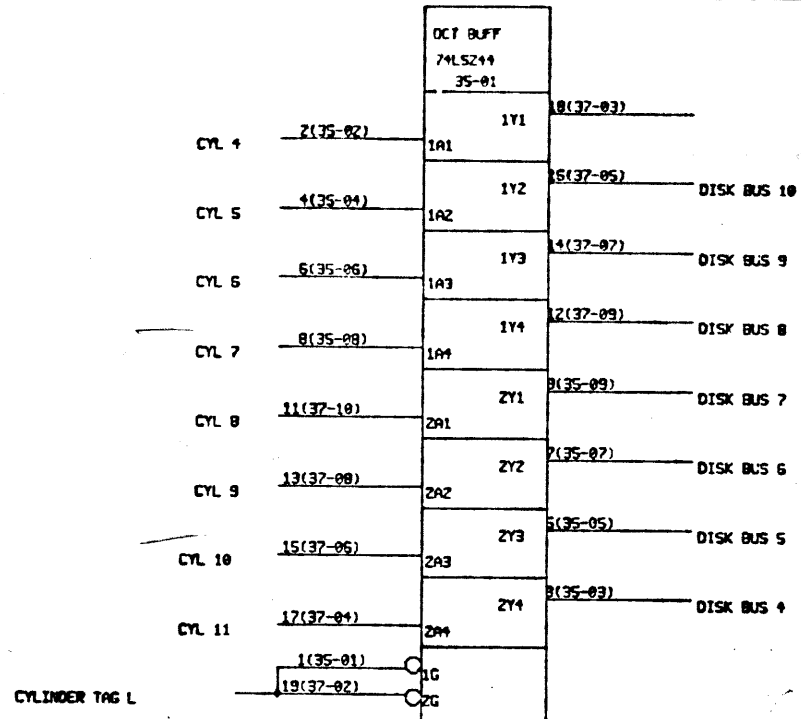
FOONLY INCORPORATED		20-DEC-79 05:52	
DRAWN BY:		RFCTRL.DRW (4, 41)	
APPROVED BY:		PAGE 1 OF 1	NUMBER
		PROJECT:	REV.



FOONLY INCORPORATED		28-DEC-79 05:52	
		WFCTRL.DRW (4, 41)	
DRAWN BY:	PAGE 1 / OF 1	NUMBER 17	REV.
APPROVED BY:	PROJECT:		



FOONLY INCORPORATED		28-DEC-79 05:52	
DRAWN BY:		PAGE 1 OF 1	NUMBER
APPROVED BY:		PROJECT:	REV.

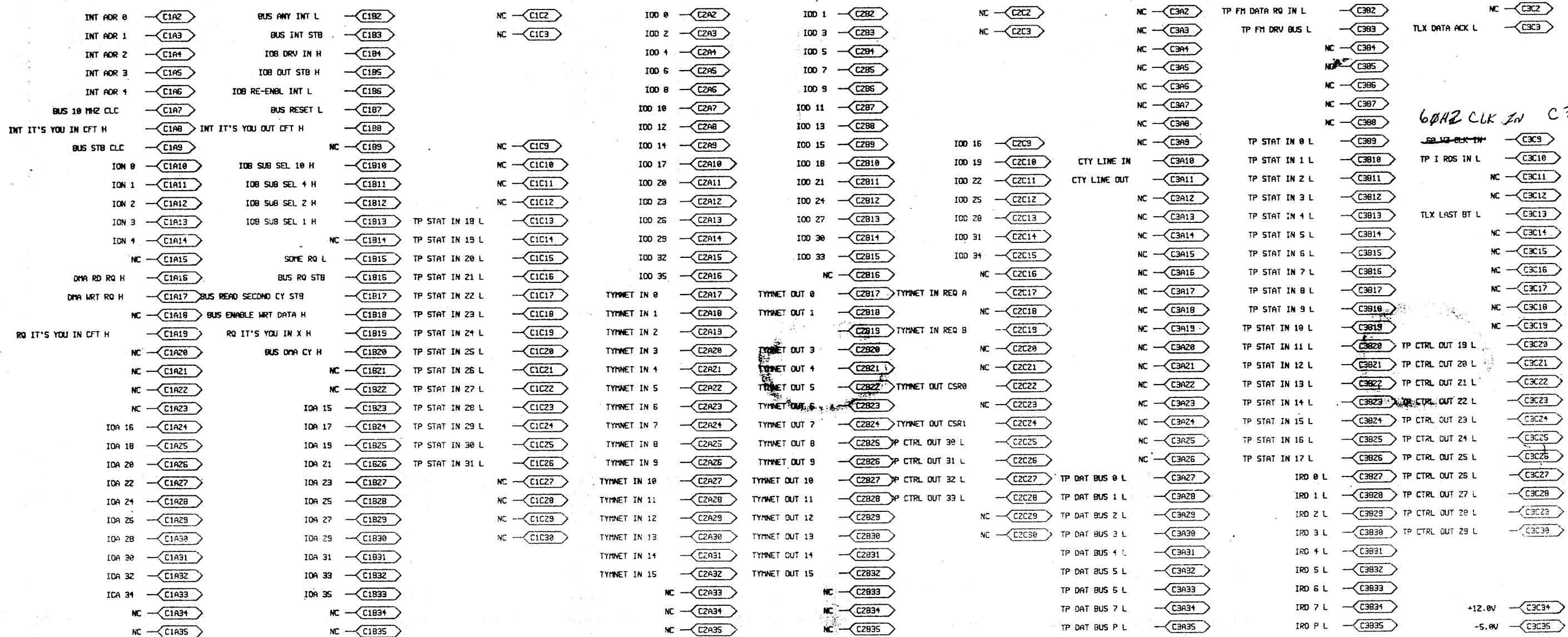


FOONLY INCORPORATED		20-DEC-79 05:53	
DRAWN BY:		DSKBUS.DRW [4,41]	
APPROVED BY:		NUMBER	REV.
PROJECT:		PAGE 1 OF 1	

CFTA-4
BUG FIXES: (shown in red)
CFTCMA
CFT FCT
CFT I1

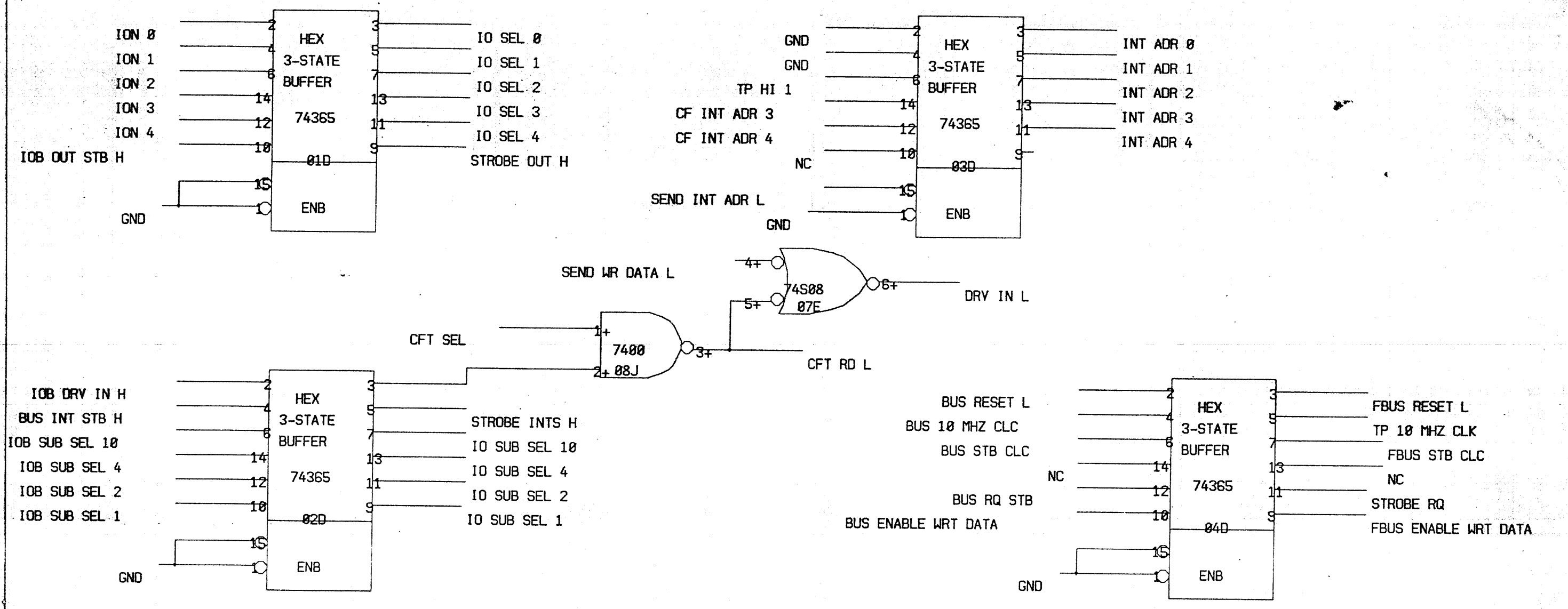
also add:
11-8 to 11-10 (sh 2 wire)
11-19 to 11-21
13-19 to 14-21
C3C35 to 503-2

NOTE !!! SIGNALS "INT IT'S YOU" AND "RO IT'S YOU" ARE NOT BUSSED !!!! -- THEY ARE DAISY-CHAINED (IN TO OUT) !!!!!



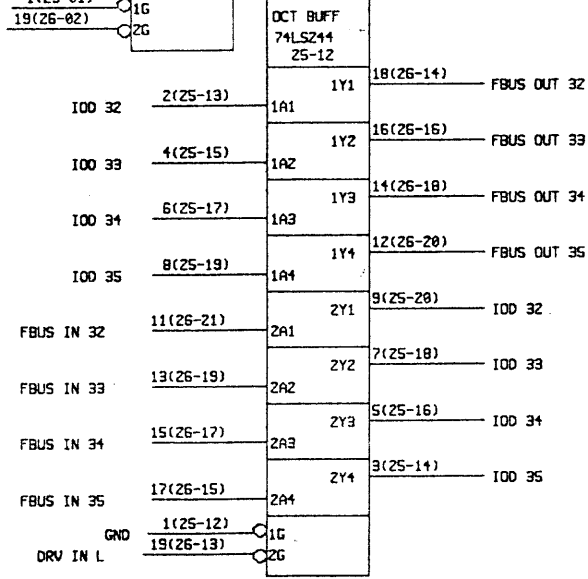
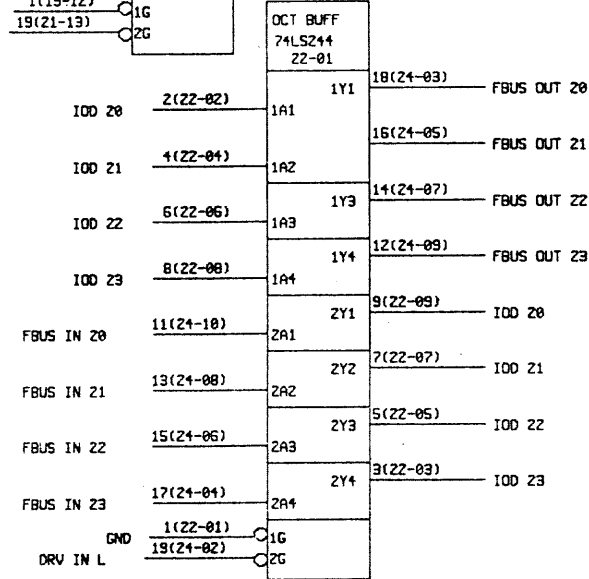
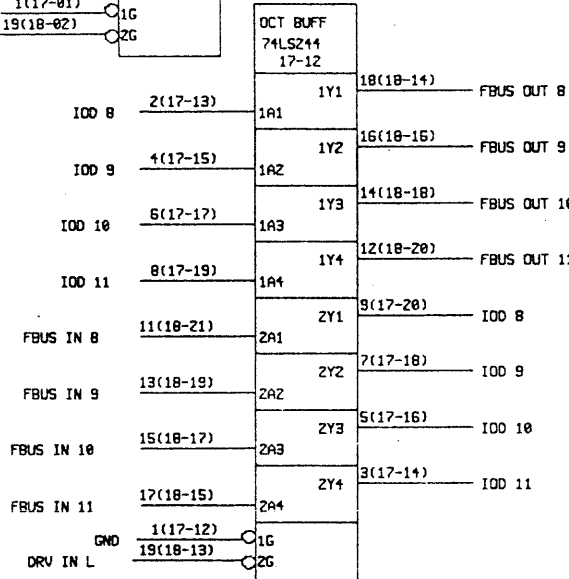
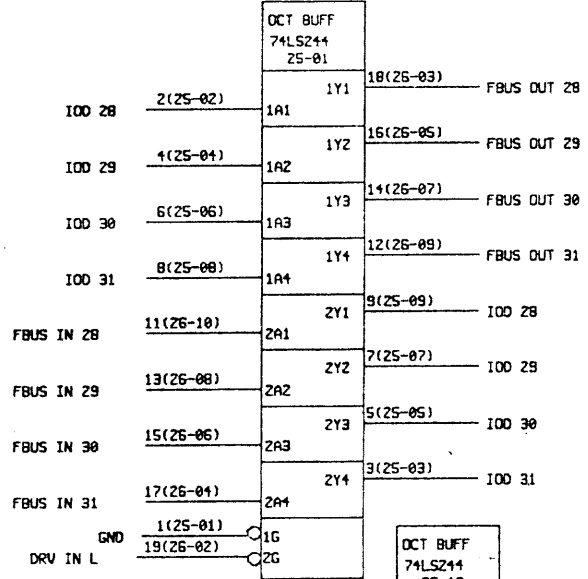
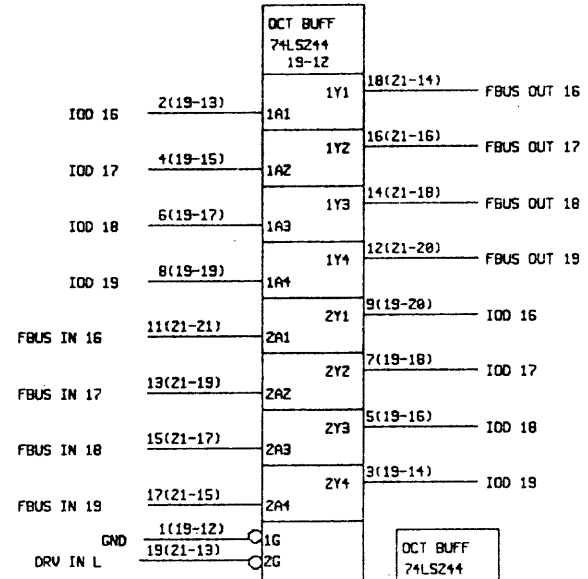
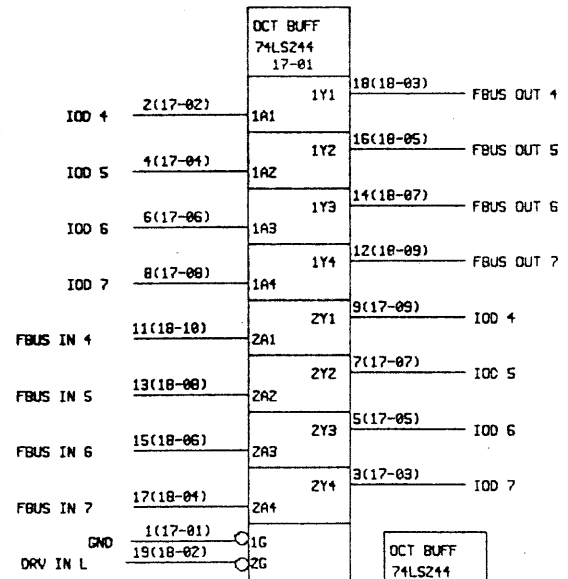
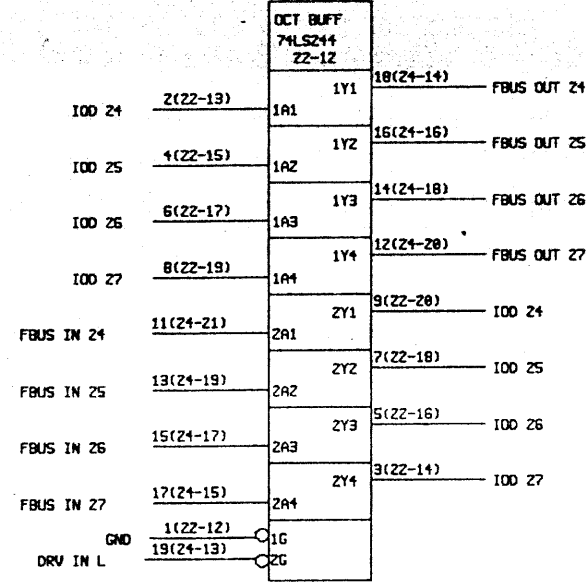
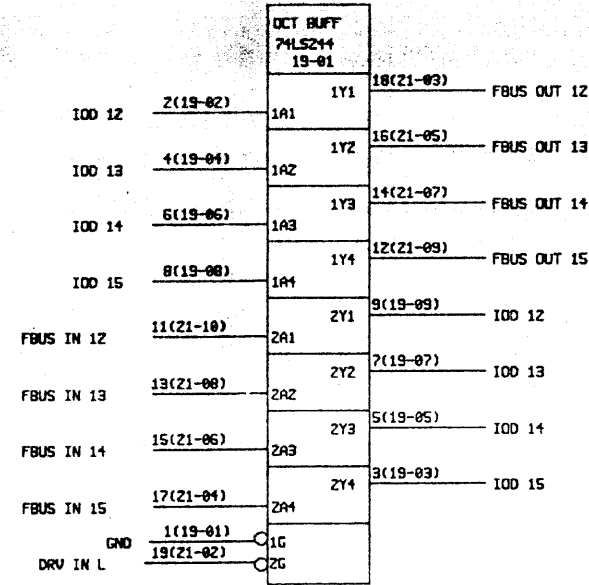
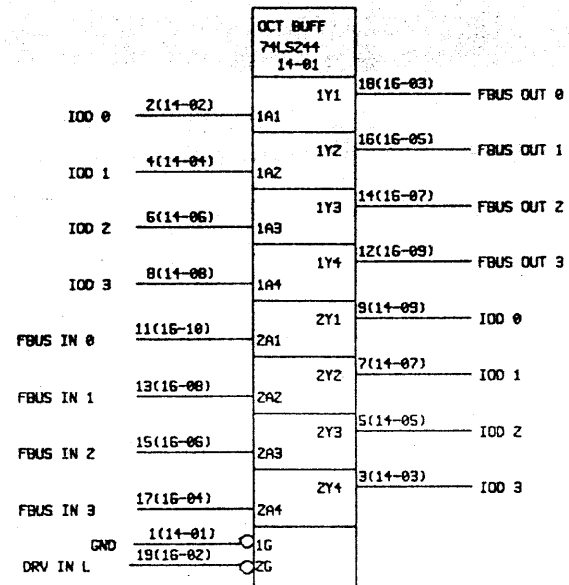
6042 CLK IN C3C8

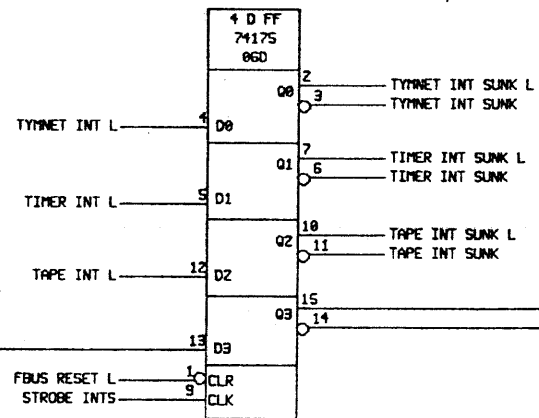
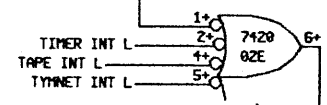
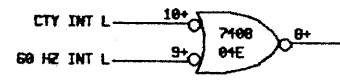
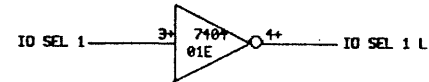
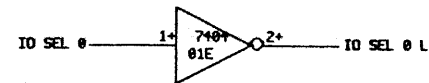
FOONLY, INC.		16-MAY-80 02:15	
DRAWN BY:		CFTACN.DRW (5157,4622)	
APPROVED BY:		REV.	
PAGE	OF	NUMBER	
PROJECT:		<i>CFTA-4</i>	
		<i>MASTER COPY</i>	



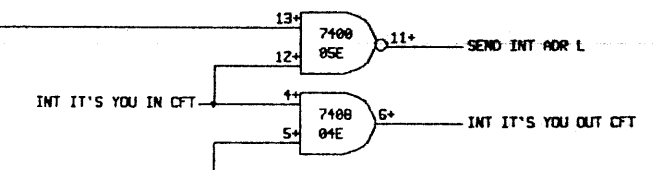
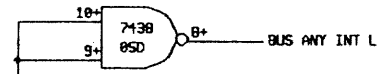
FOONLY, INC.		19-MAY-80 02:37	
DRAWN BY:		PAGE	OF
APPROVED BY:		PROJECT:	CFTA
		NUMBER	REV.

CFTBF.DRW (5157,4622)



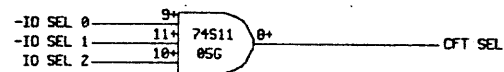
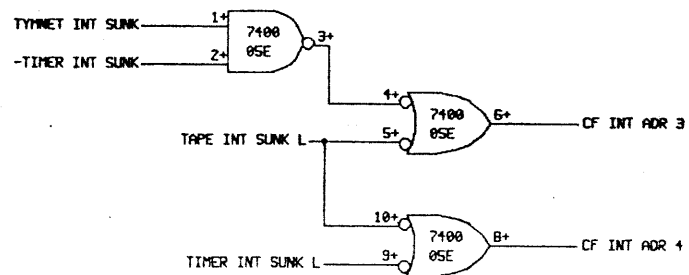


*interrupt
synchronizer*



DEVICE ADDRESSES

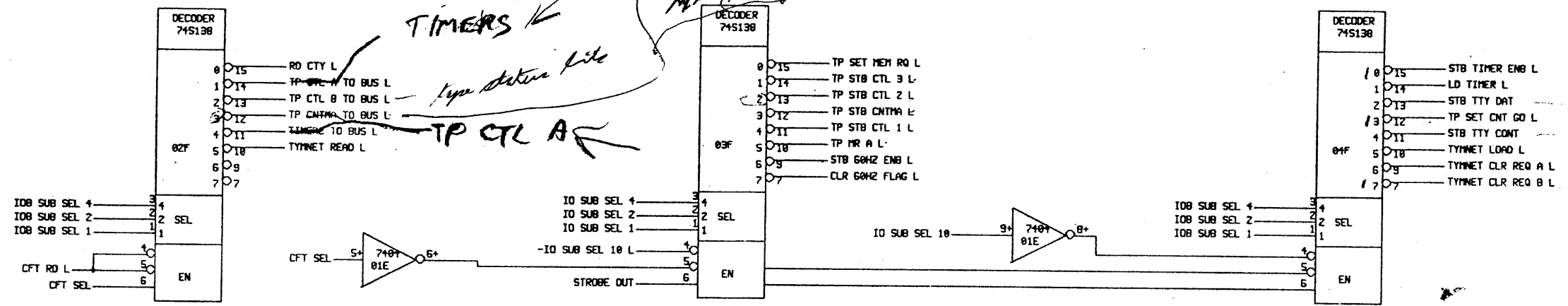
- CTY, 60 HZ CLK 4
- TIMER 5
- TYMNET 6
- TAPE 7



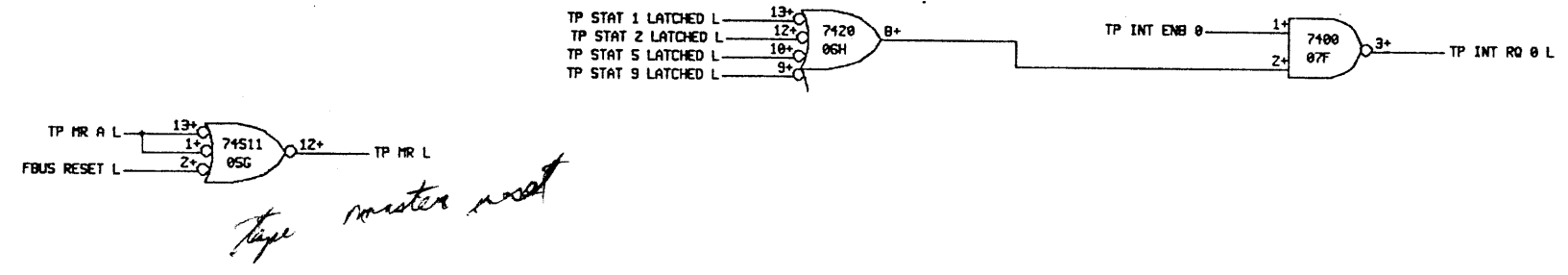
*high order
ROM address
into*

[Handwritten signature]

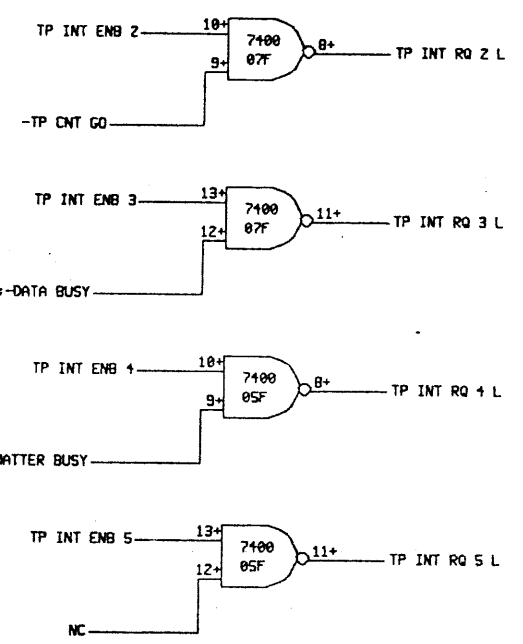
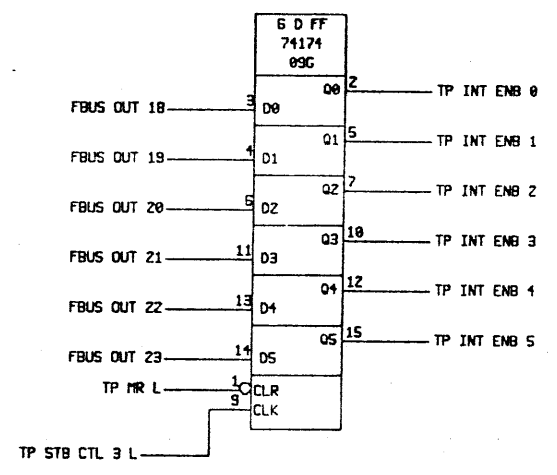
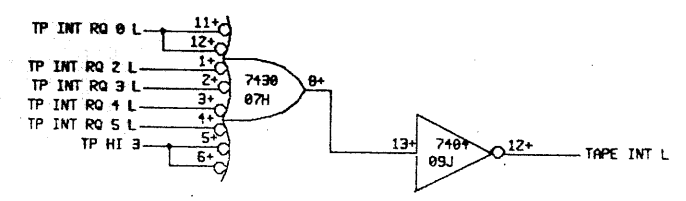
FOONLY, INC.		19-MAY-80 02:41	
DRAWN BY:		PAGE OF	NUMBER
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		CFTA	CFT INT. DRW (5157, 4622)



*tape status
(end of tape, parity error etc.)*



tape master reset

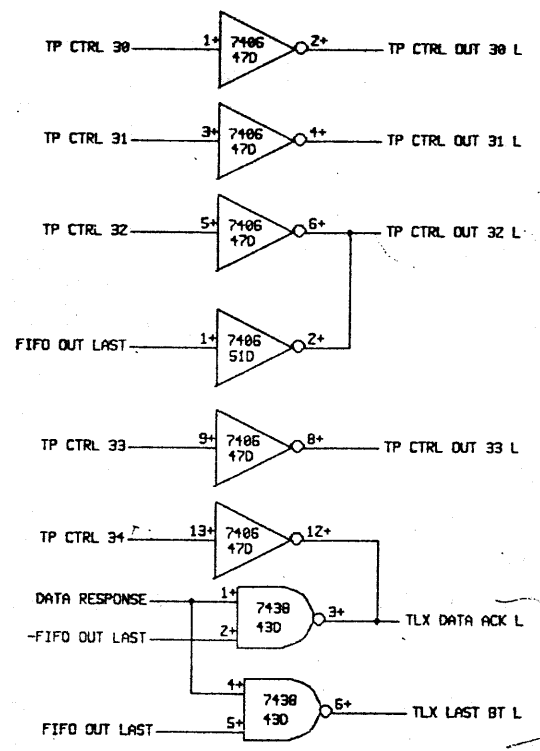
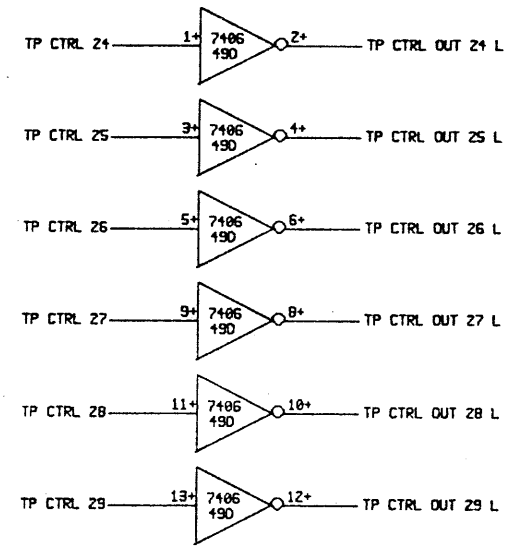
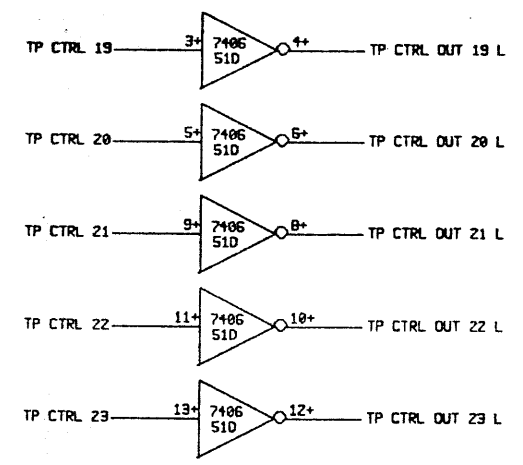
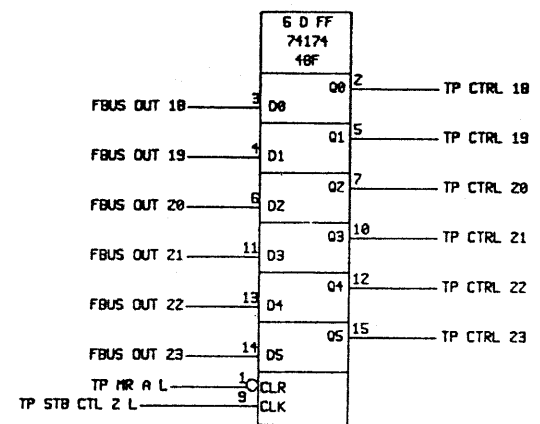
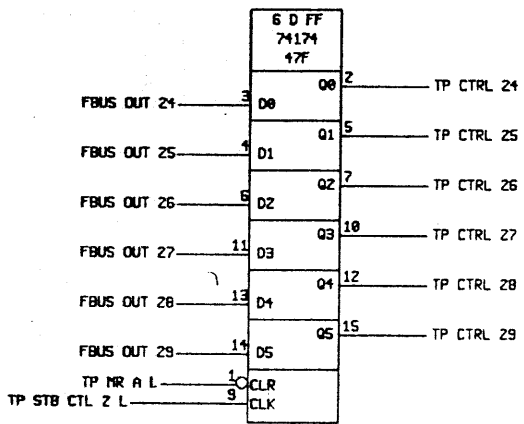
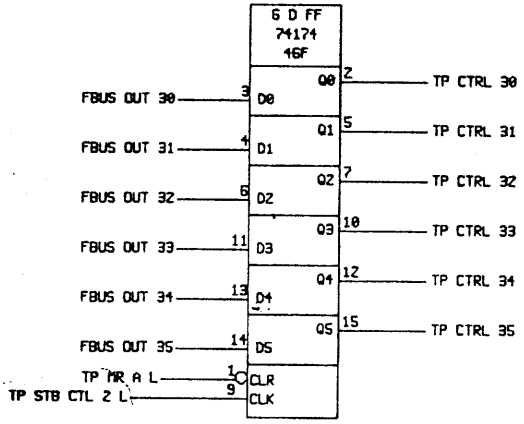
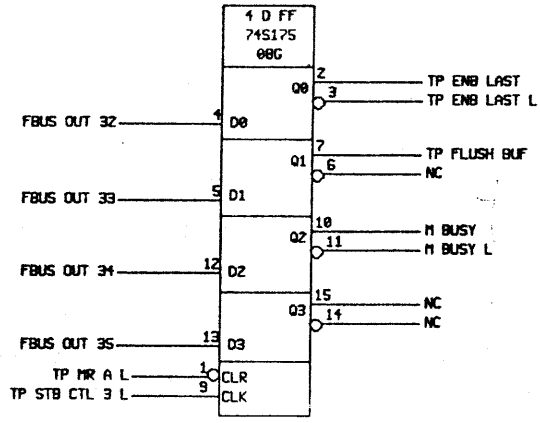
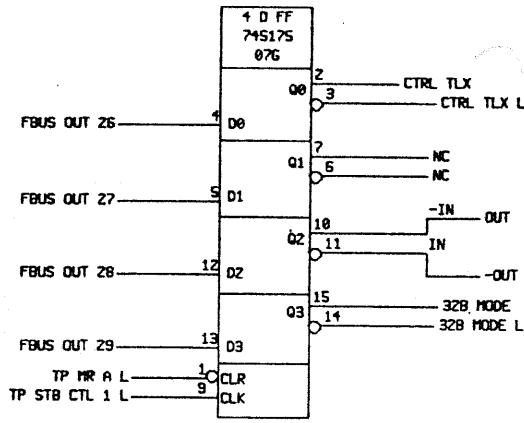


tape interrupt

correct

FOONLY, INC.		22-MAY-80 08:48	
DRAWN BY:		PAGE OF	NUMBER
APPROVED BY:		PROJECT: FOONLY	REV.
		CFTA	CFTCT1.DRW(5157,4622)

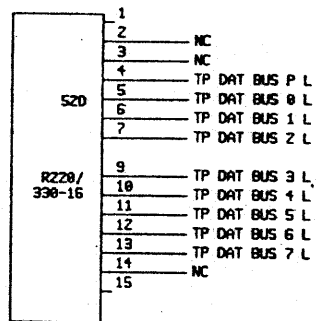
always false (if not talks to a Telecon formatter)



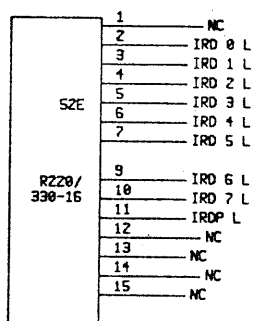
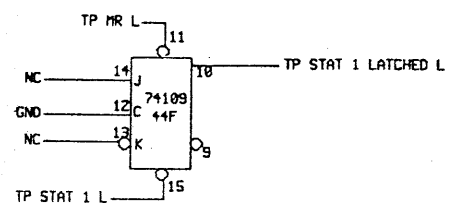
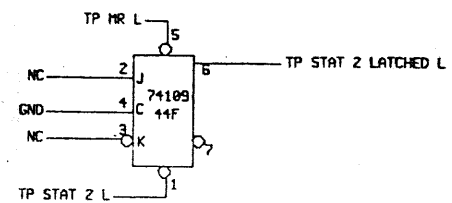
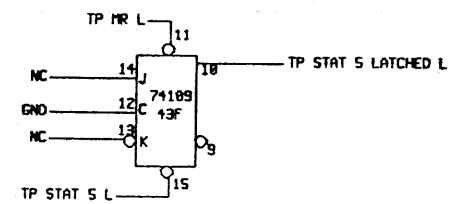
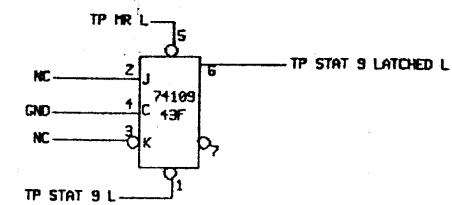
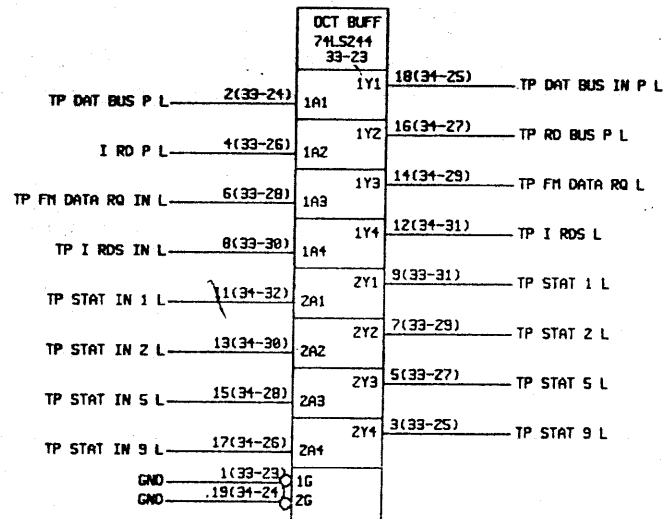
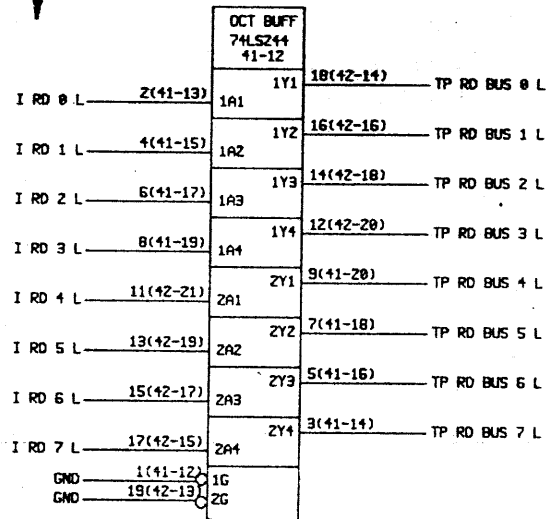
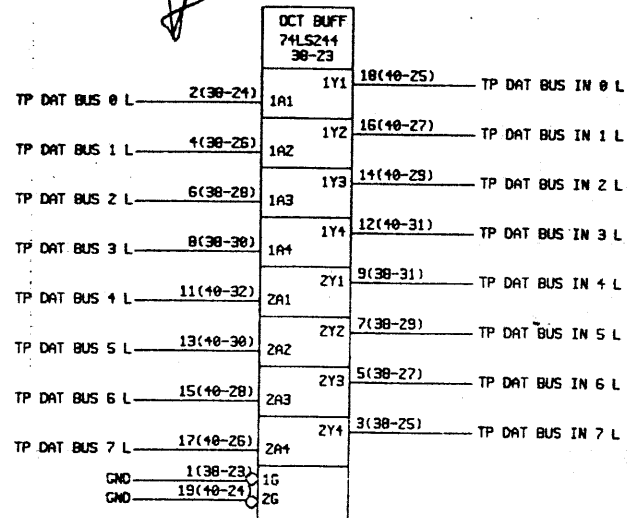
open collector drivers to traps

FOONLY, INC.		22-MAY-80 02:58	
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			REV.
CFTCT3.DRW (5157,4622)			

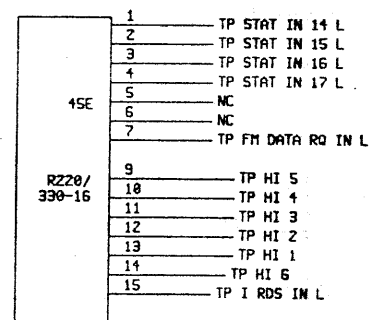
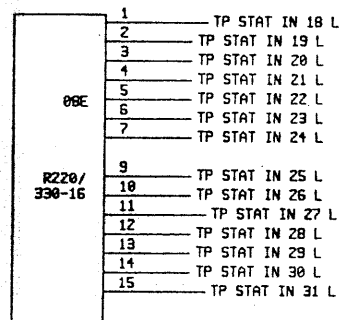
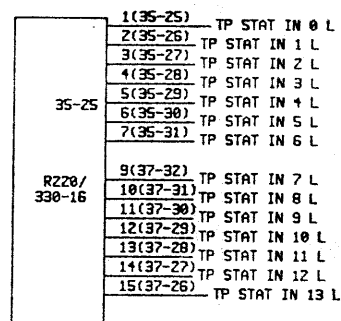
TLX only



Red Data



+5
1202
3302



FOONLY, INC.

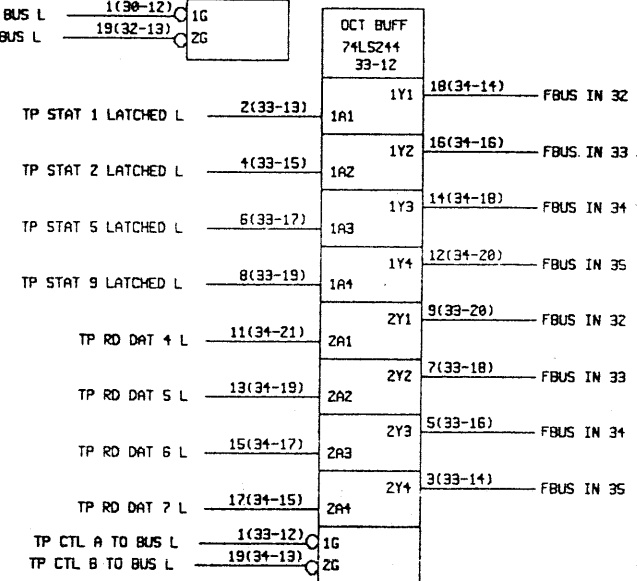
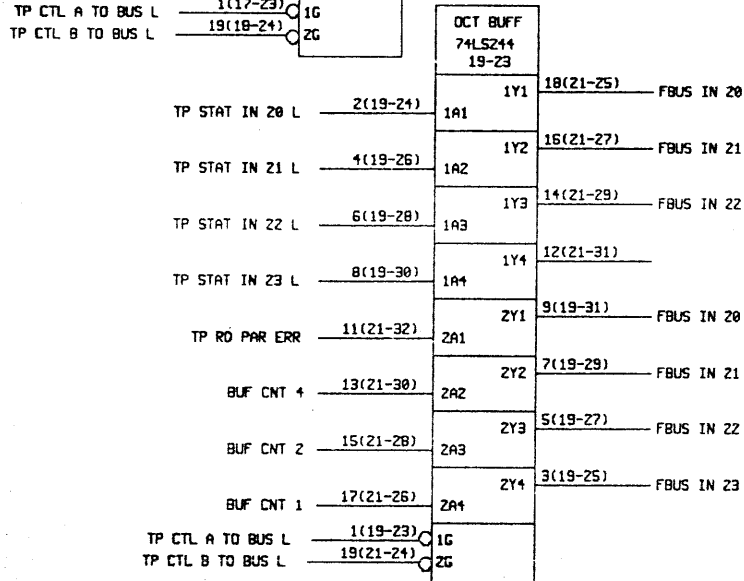
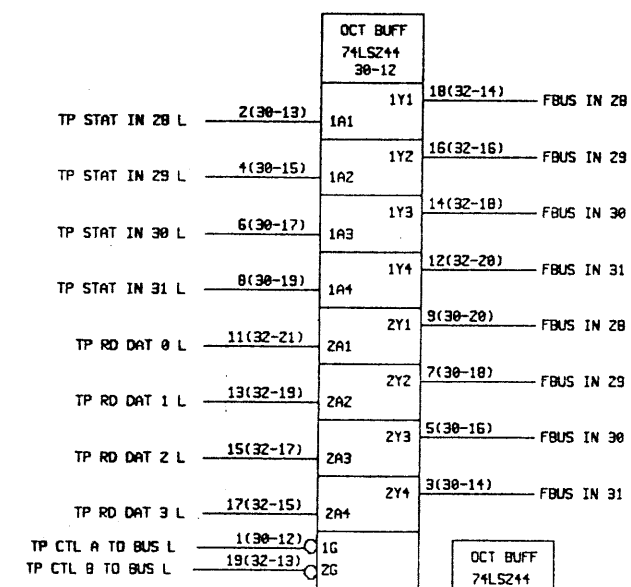
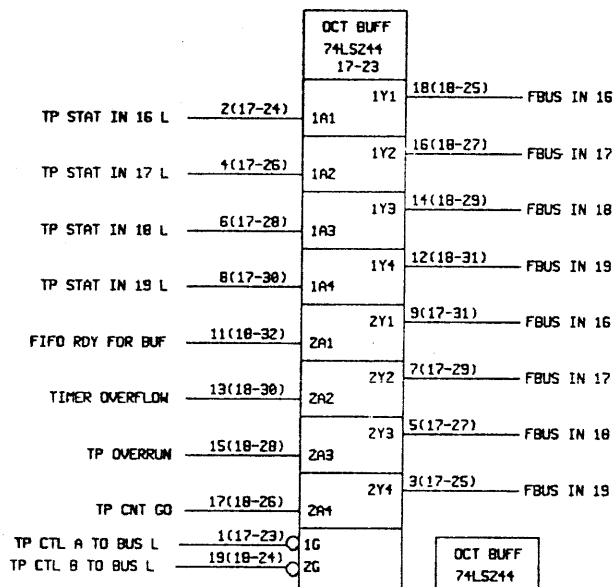
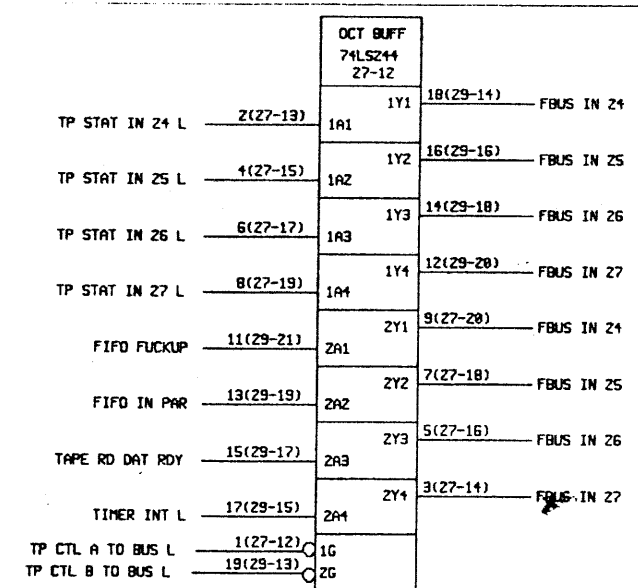
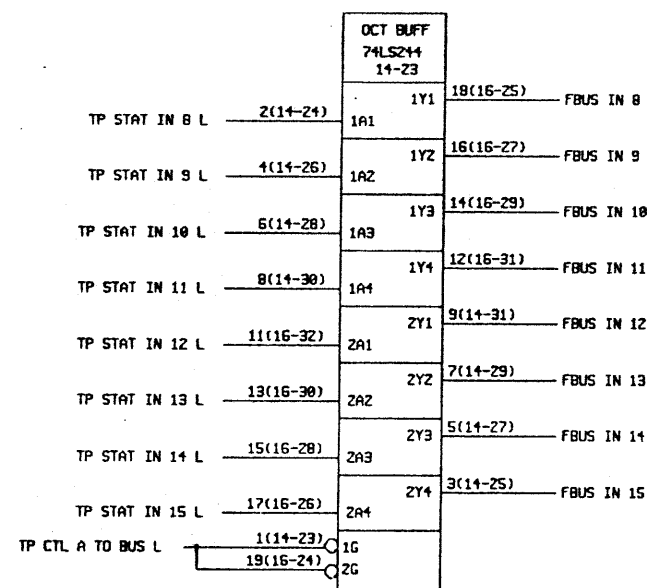
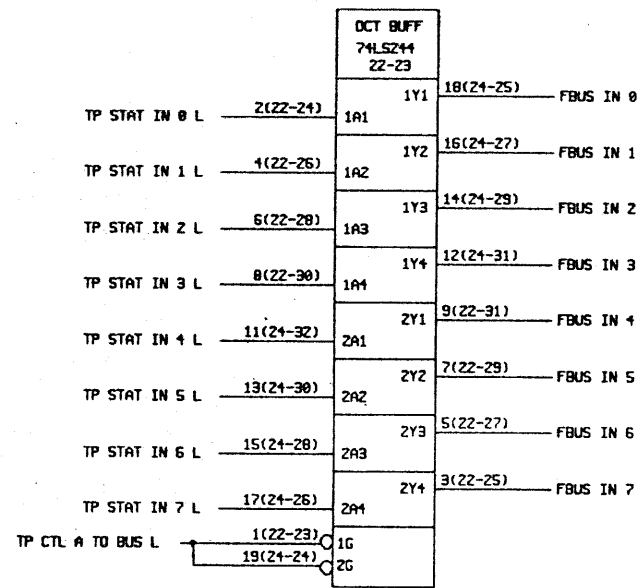
22-MAY-80 00:46

CFTCT4.DRW (5157, 4622)

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APPROVED BY:

PAGE OF
PROJECT: FOONLY CFTA

NUMBER REV.

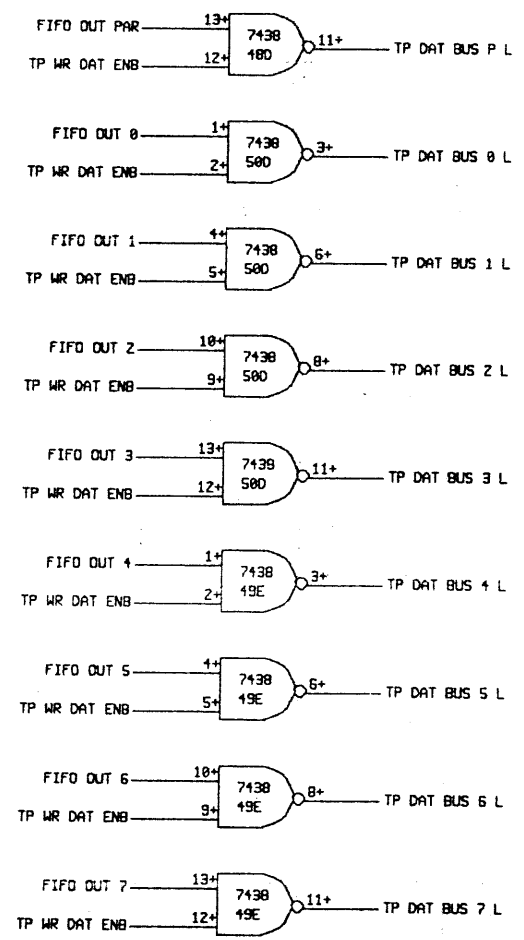
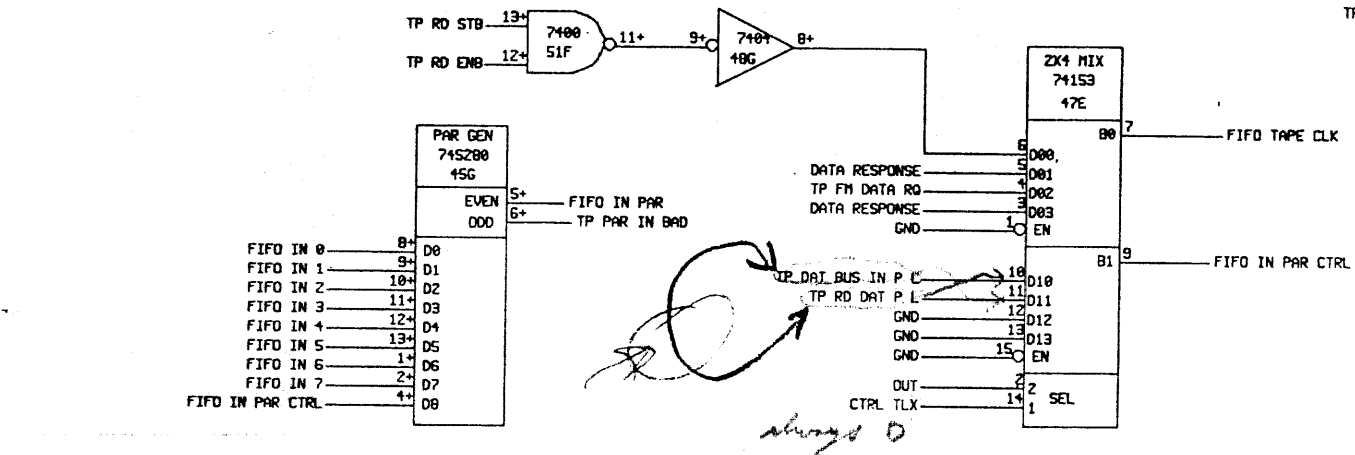
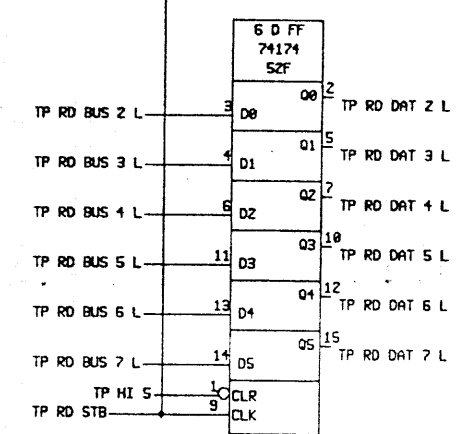
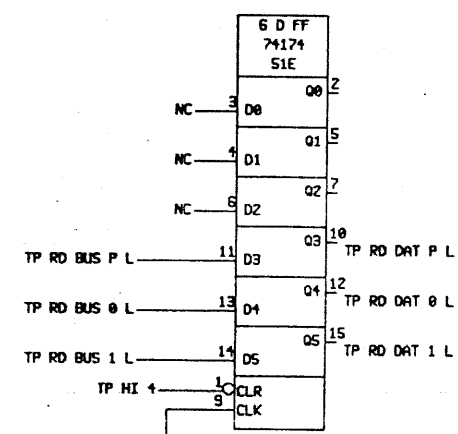
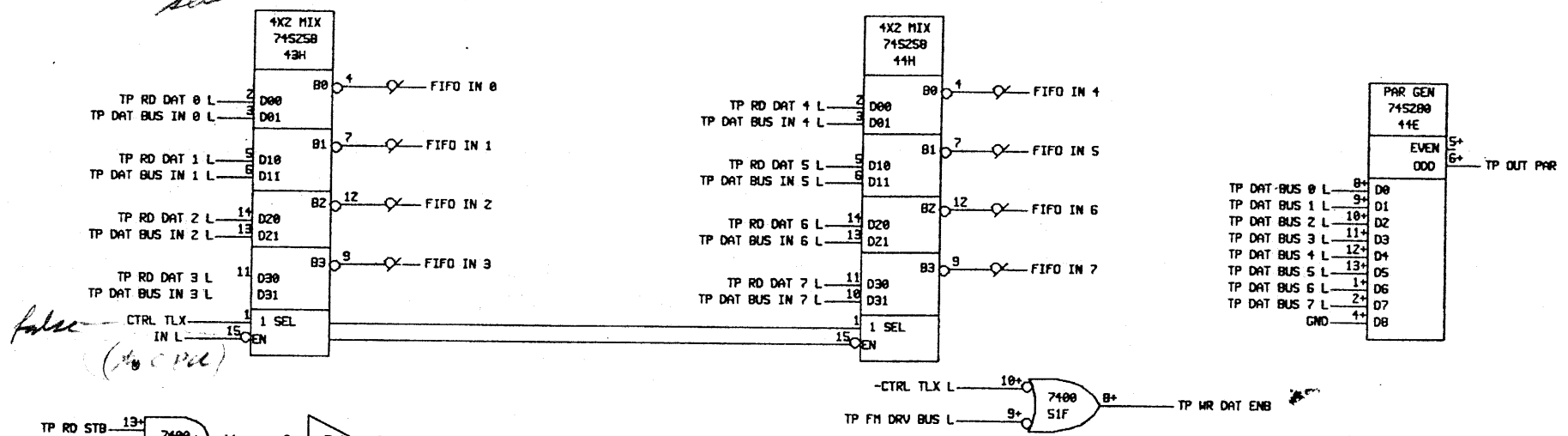
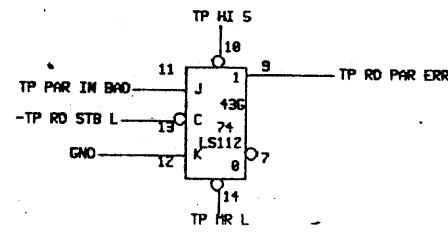


*for
direct
read to FBUS
without
using
data
panel*

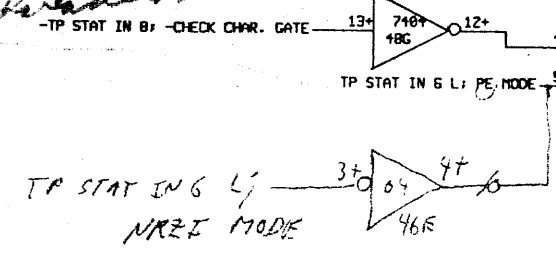
FOONLY, INC.		22-MAY-80 00:48	
DRAWN BY:	PAGE	OF	NUMBER
APPROVED BY:	PROJECT:	CFTA	
			REV.

CFTCT5.DRW(5157,4622)

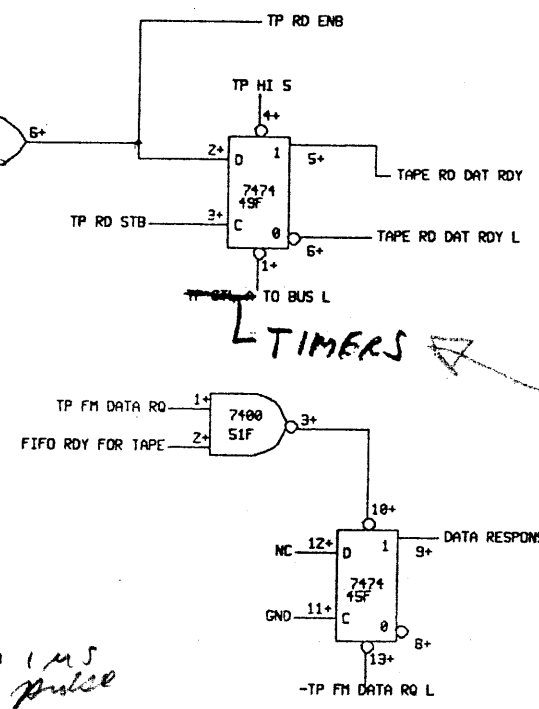
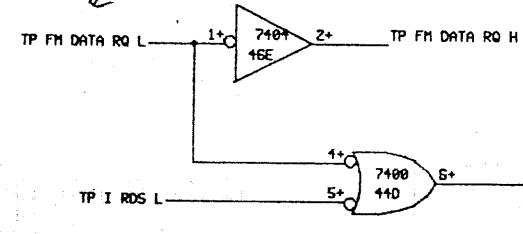
select TP RD DAT #



Ignore check read mode
Parameters in NR23

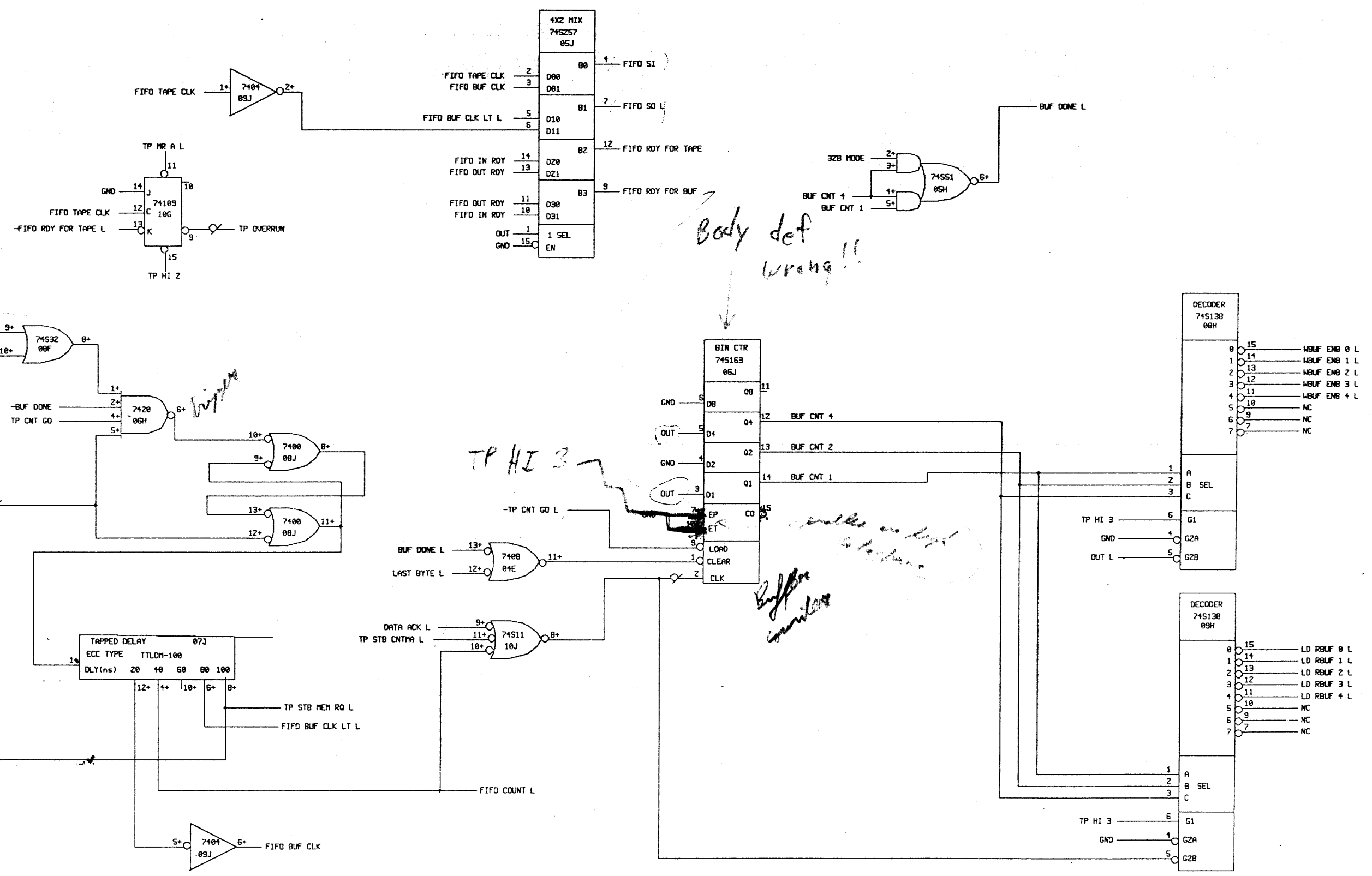


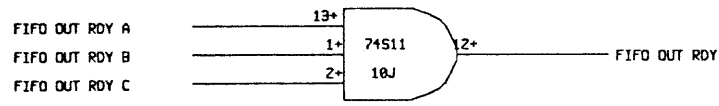
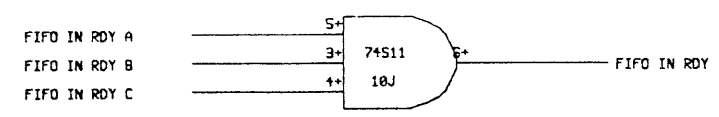
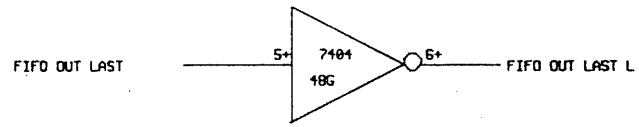
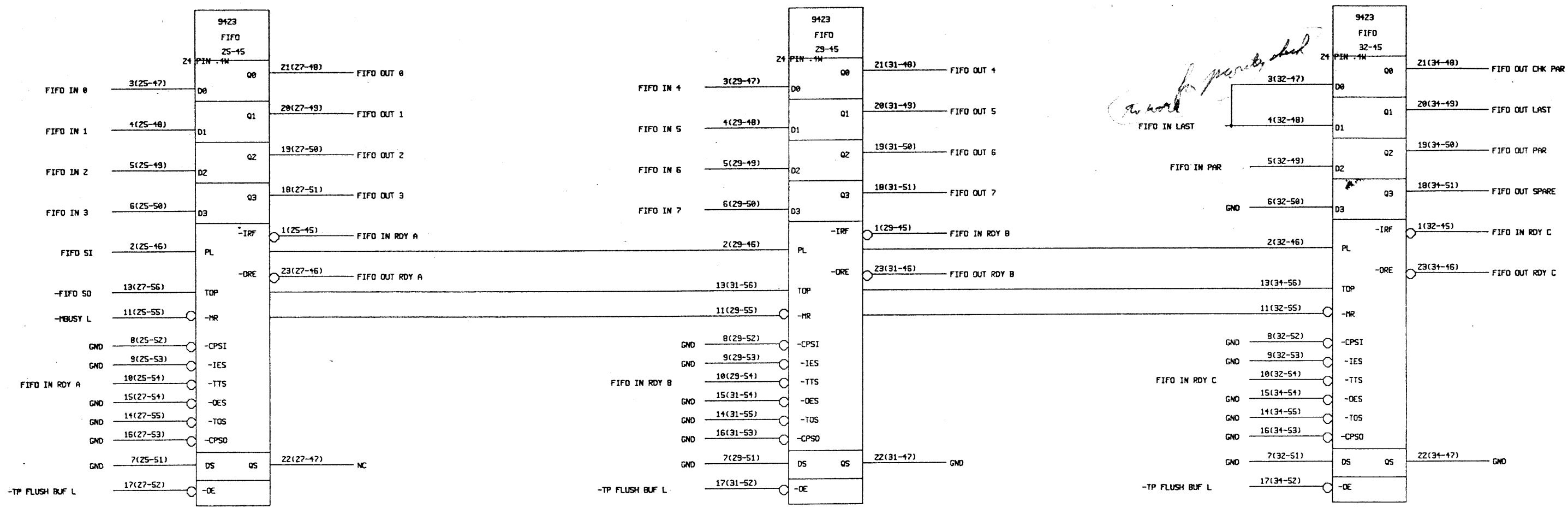
write only



TO BUS L
TIMERS

FOONLY, INC.		19-MAY-80 02:59	
DRAWN BY:	PAGE	OF	NUMBER
APPROVED BY:	PROJECT:	FOONLY	REV.
		CFT11.DRW (5157, 4622)	

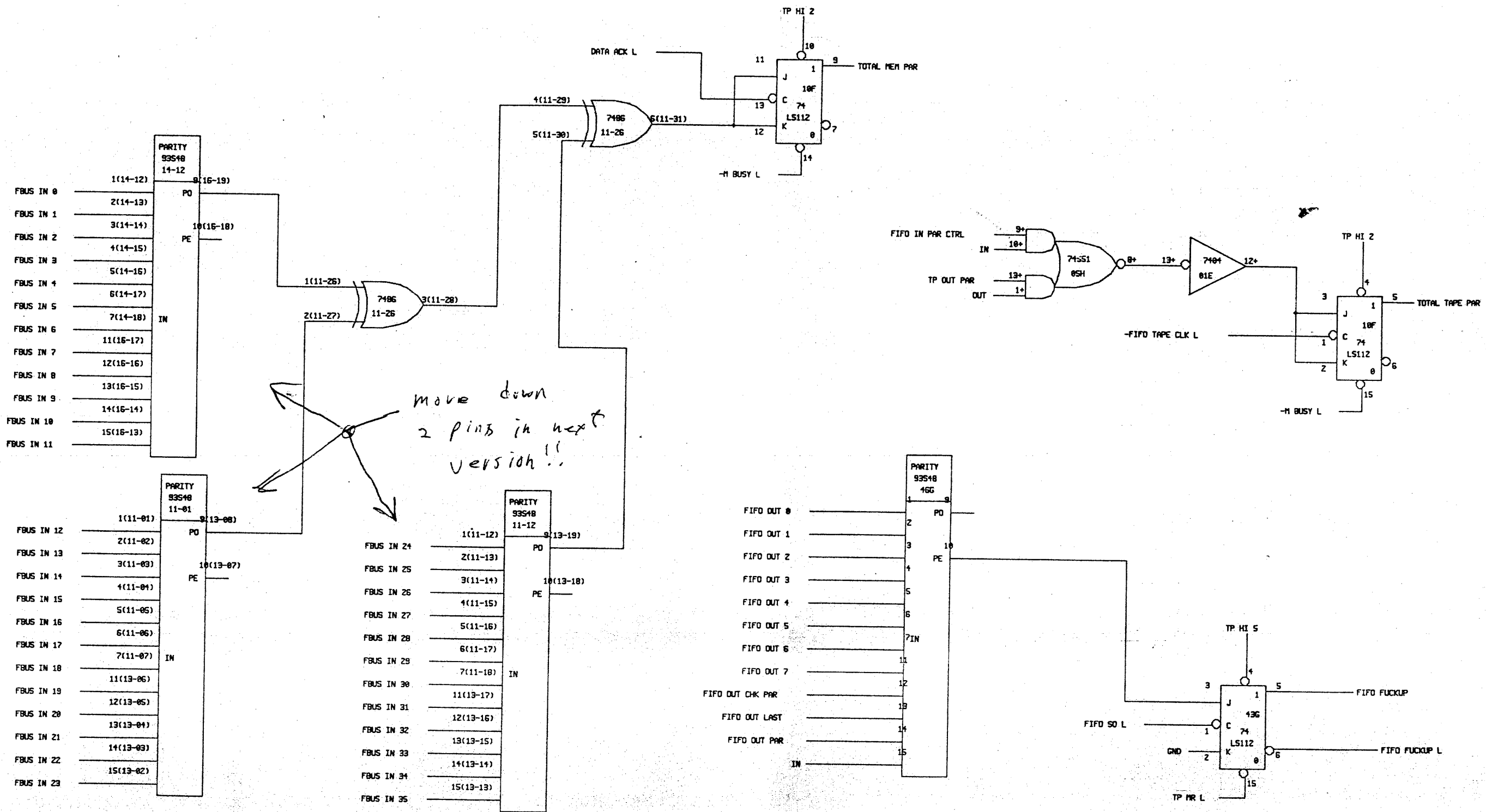




use same FIFO for in and out

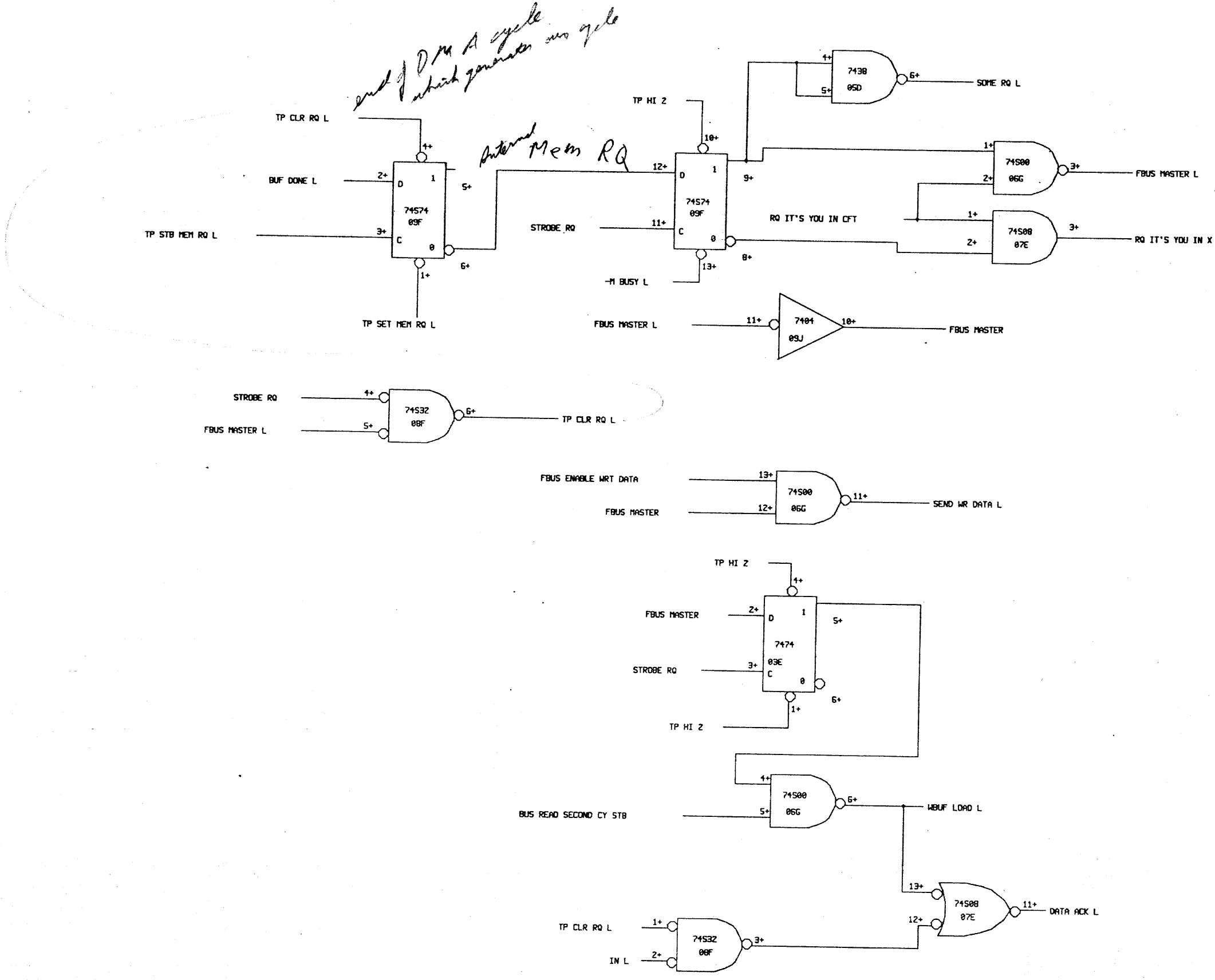
FOONLY INCORPORATED		19-MAY-80 03:05	
DRAWN BY:		PAGE 1 OF 1	NUMBER
APPROVED BY:		PROJECT: CFTA	REV. 0

CFTTIF.DRW (5157, 4622)

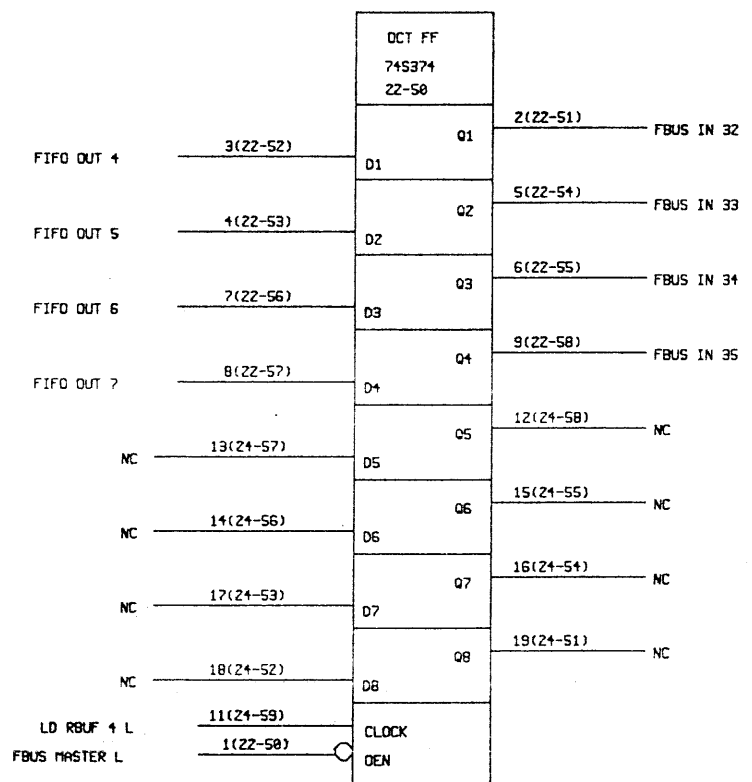
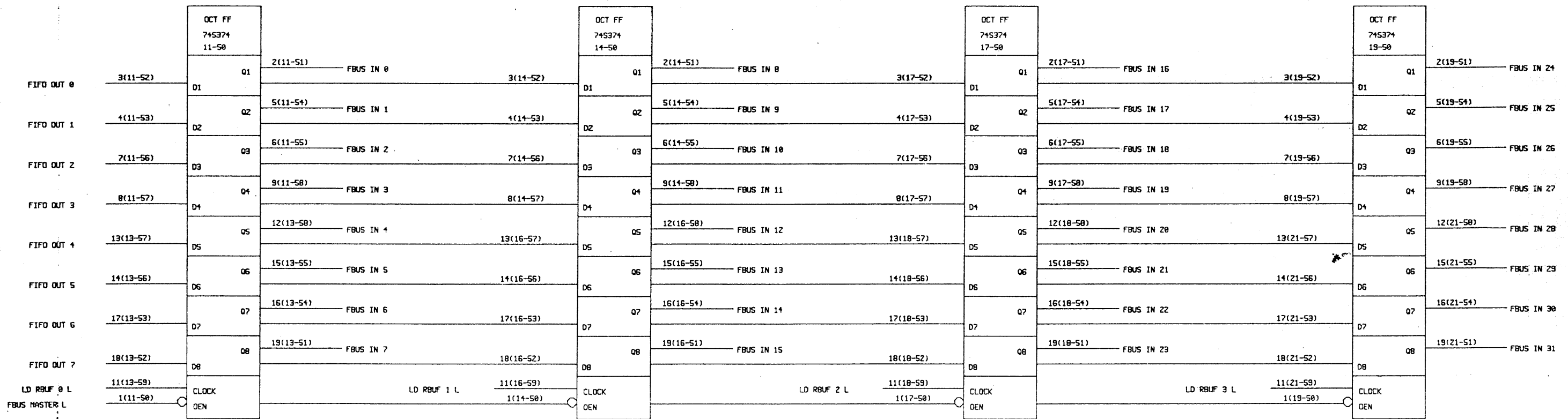


FOONLY INCORPORATED		22-MAY-80 01:50	
DRAWN BY:	PAGE 1 OF 1	NUMBER	REV.
APPROVED BY:	PROJECT: CFTA		

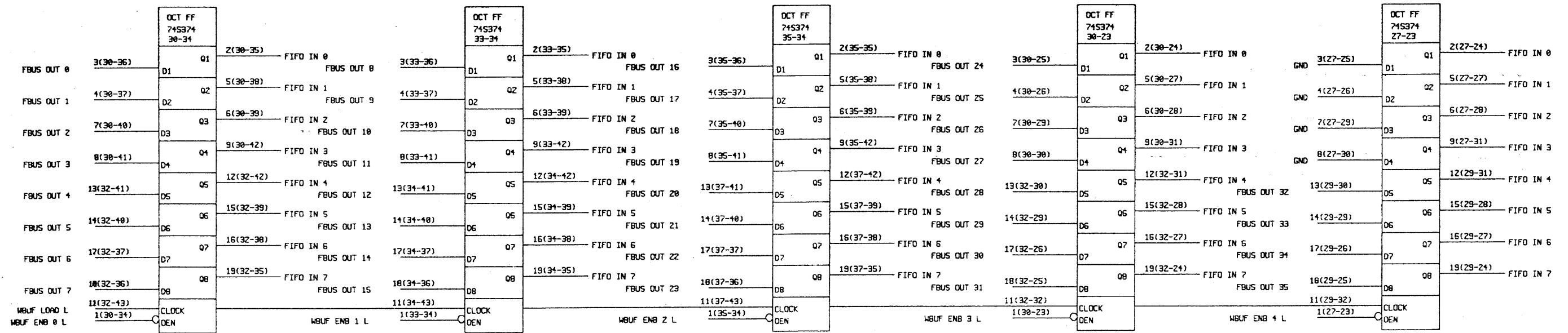
CFTF11.DRW (5157,4622)



FOONLY INCORPORATED		19-MAY-80 03:17	
DRAWN BY:	PAGE 1 OF 1	NUMBER	REV.
APPROVED BY:	PROJECT:	CFTFBC.DRW (5157, 4622)	



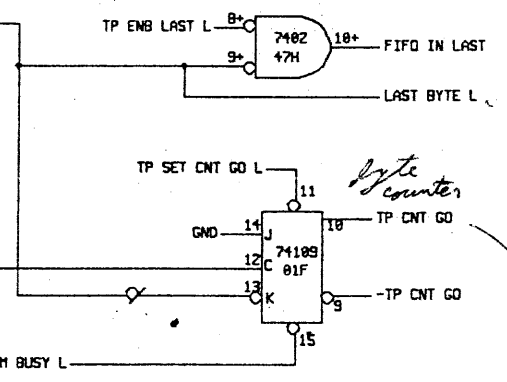
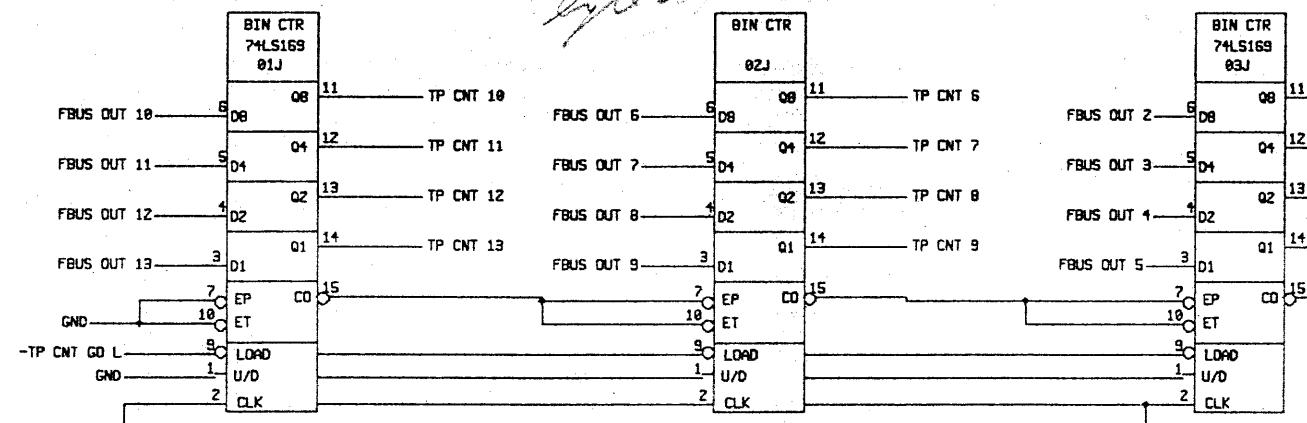
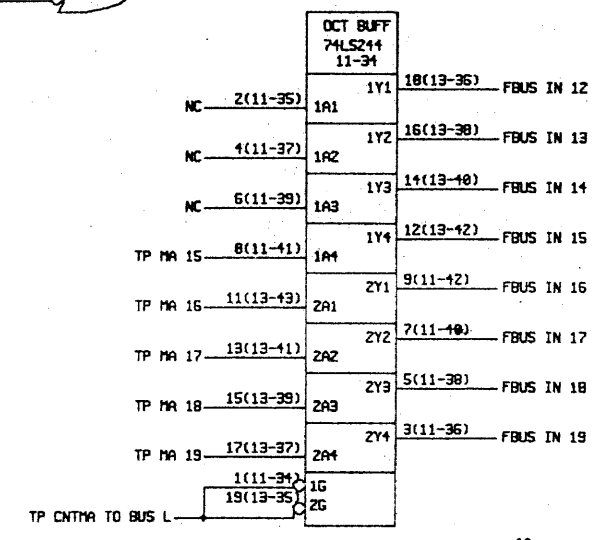
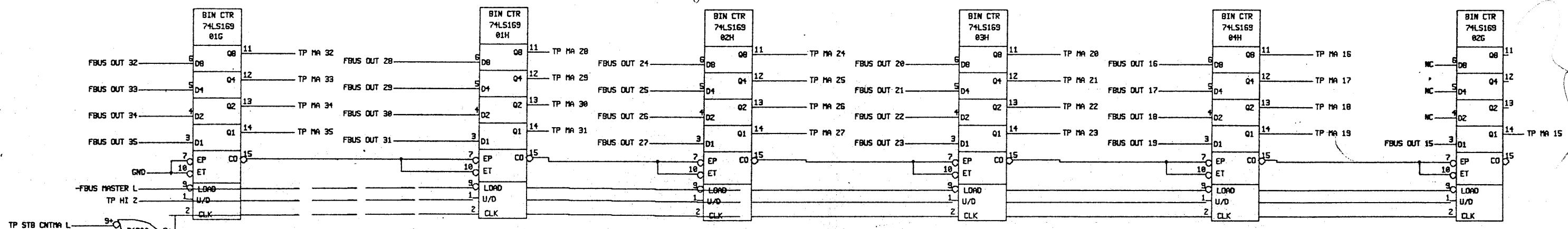
FOONLY INCORPORATED		18-MAY-80 23:51	
DRAWN BY:		PAGE 1 OF 1	CF TRDF.DRW (5157,4622)
APPROVED BY:		NUMBER	REV.
			8



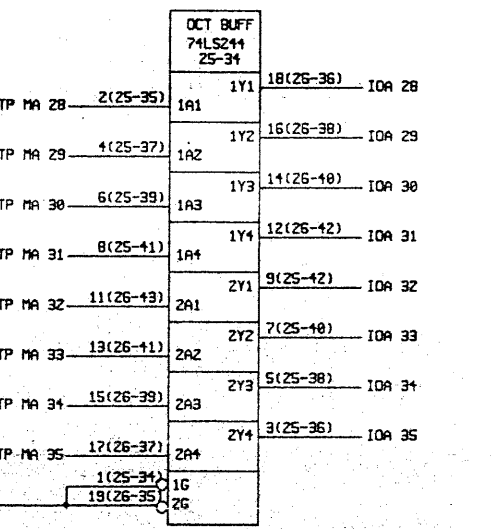
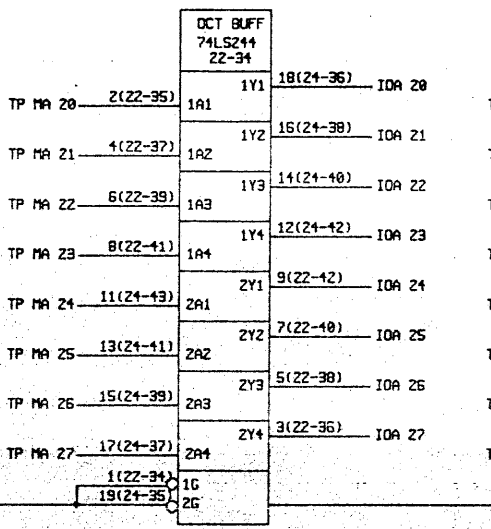
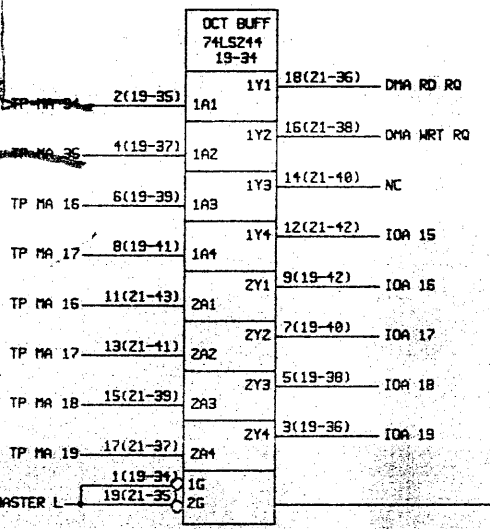
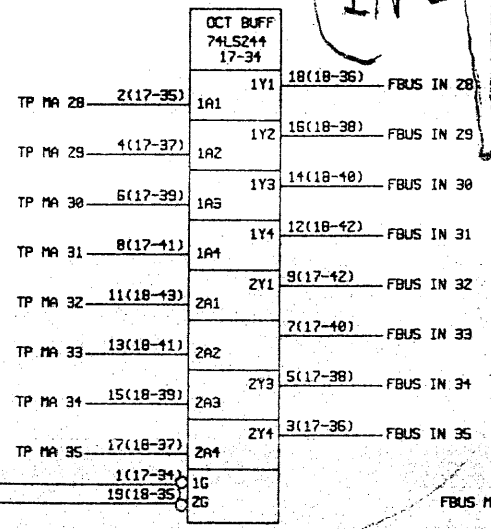
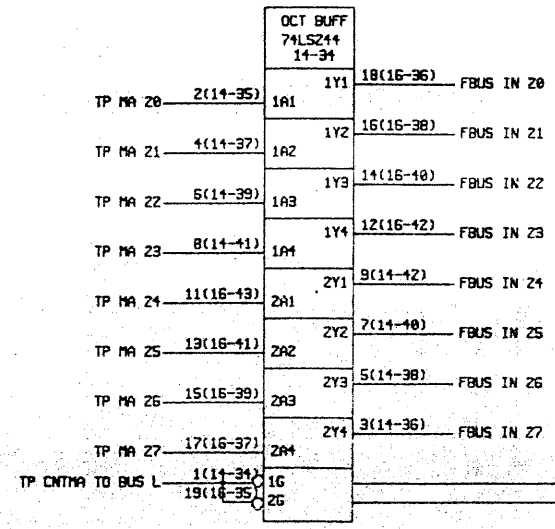
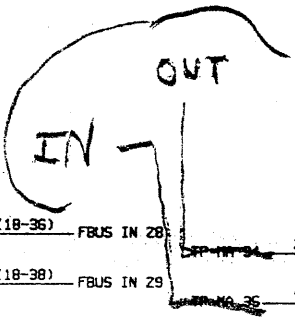
FOONLY INCORPORATED		19-MAY-88 03:09	
		CF TWBF. DRW (5157, 4622)	
DRAWN BY:	PAGE 1 OF 1	NUMBER	REV.
APPROVED BY:	PROJECT:		8

counts at end of tape operation

16



code in CPU starts counter with N-1 to do a byte transfer



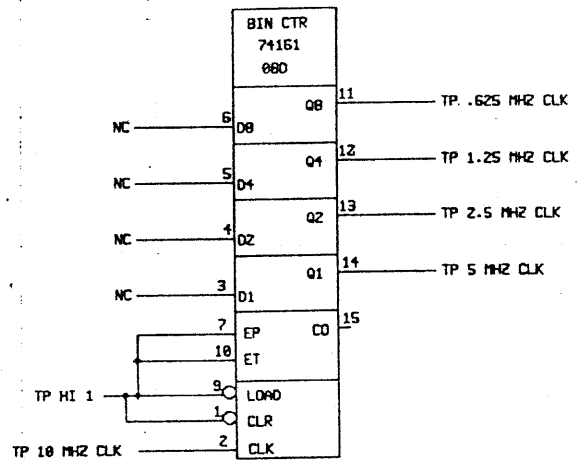
near end of count data channel is running

FOONLY INCORPORATED		19-MAY-80 03:30	
DRAWN BY:		PAGE 1 OF 1	NUMBER
APPROVED BY:		PROJECT:	REV.

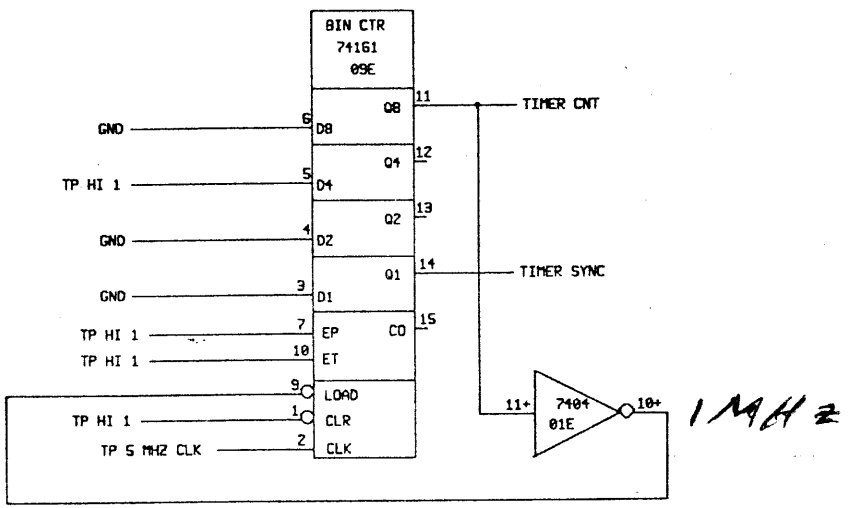
LAST BYTE

3 2 1 0 - 1

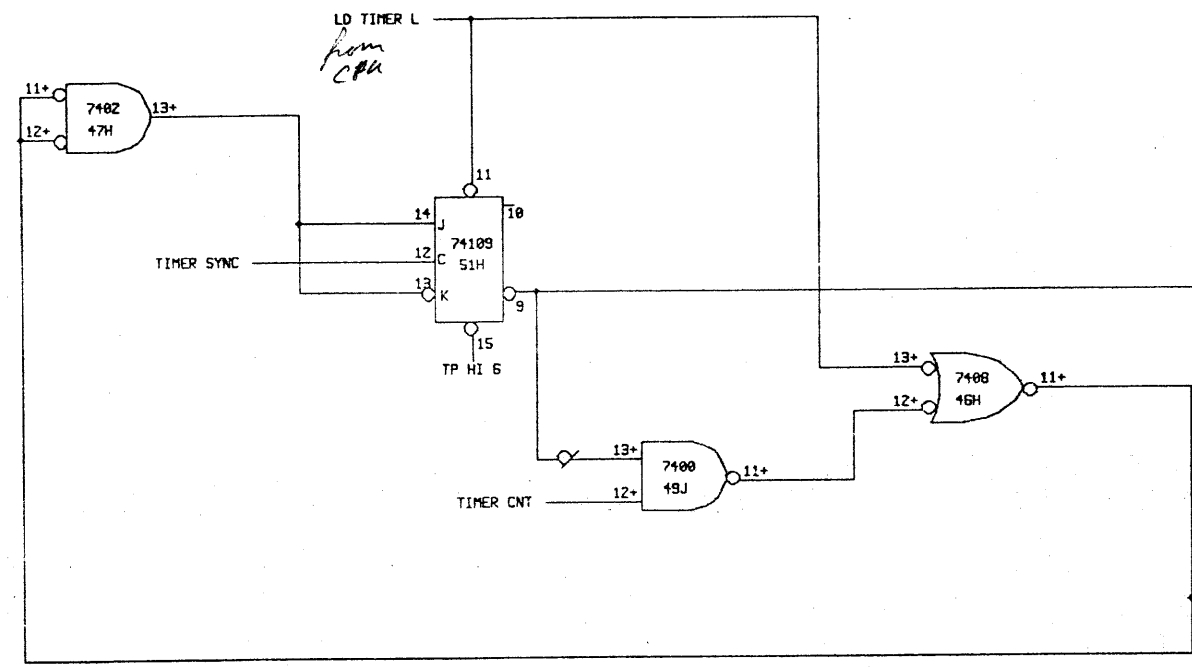
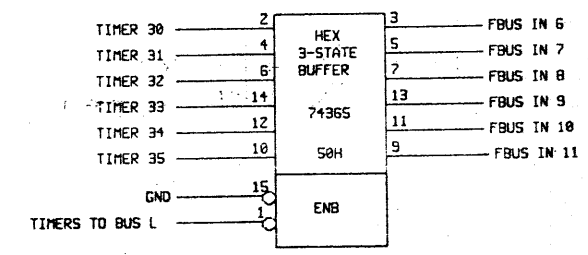
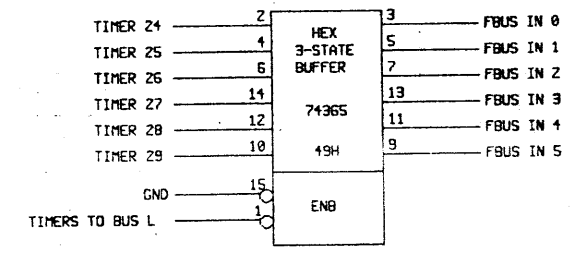
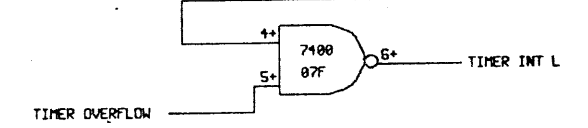
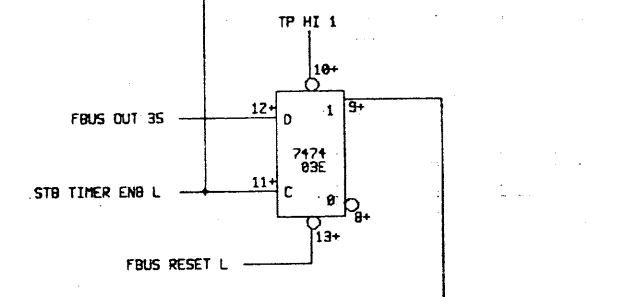
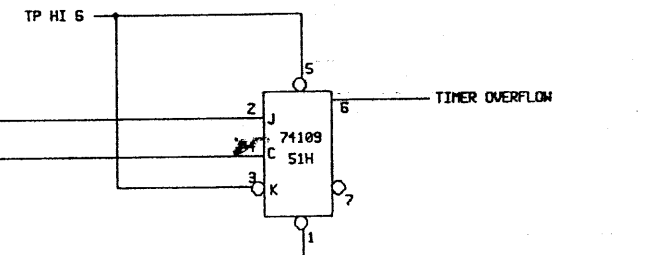
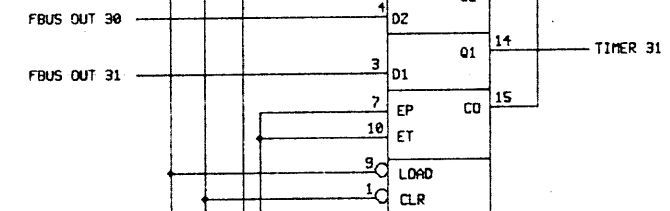
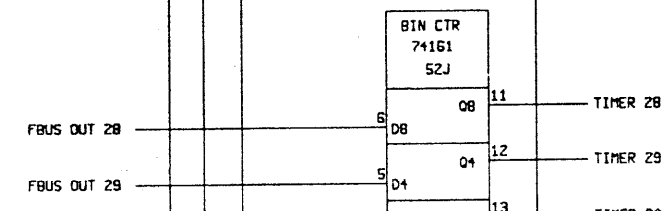
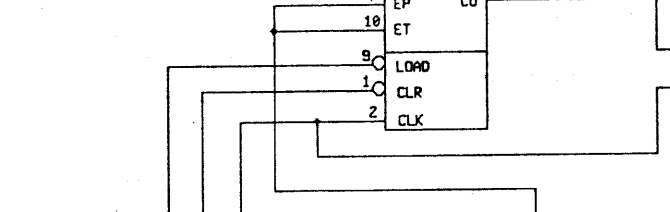
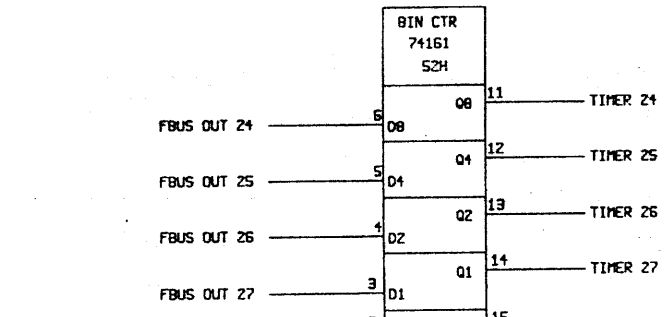
CNT GO



NOTE: COUNTING SEQUENCE IS 4 5 6 7 10
DIVIDES BY 5, GIVING 1 MHz OUT



from FBUS
from CPU
clock



FOONLY, INC.

22-MAY-80 02:34

CFTTIM.DRW(5157,4622)

DRAWN BY:
APPROVED BY:

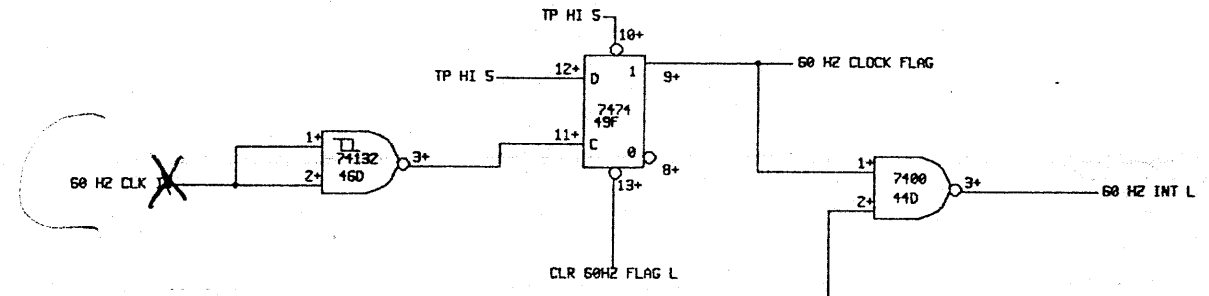
PAGE
PROJECT:

OF

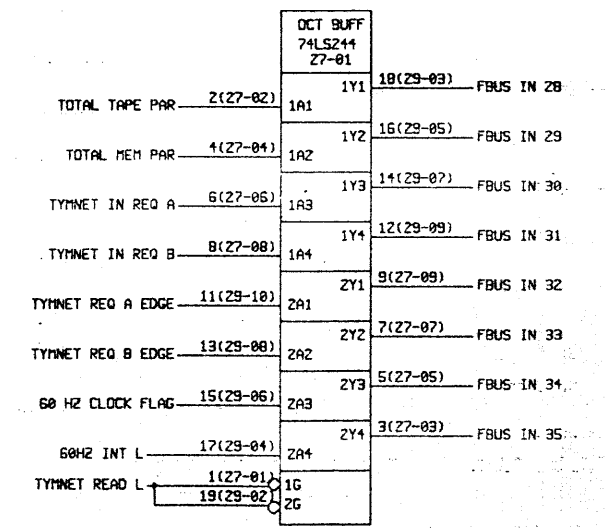
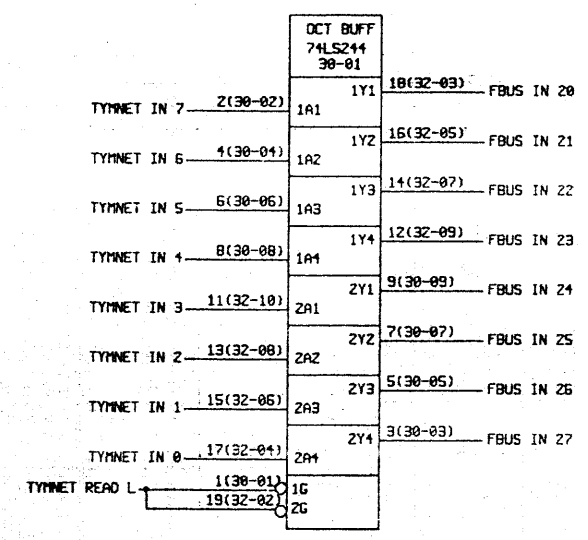
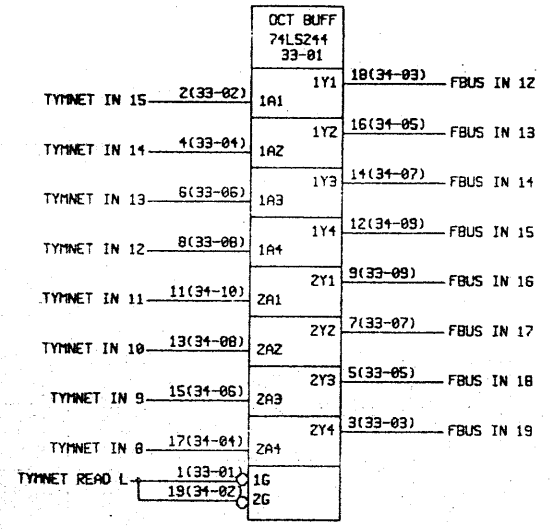
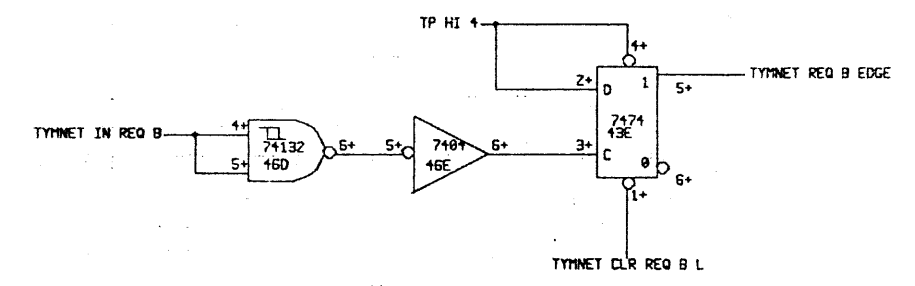
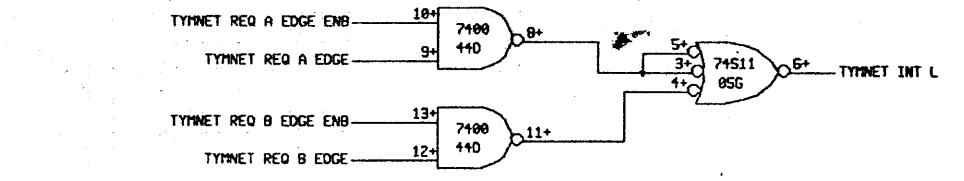
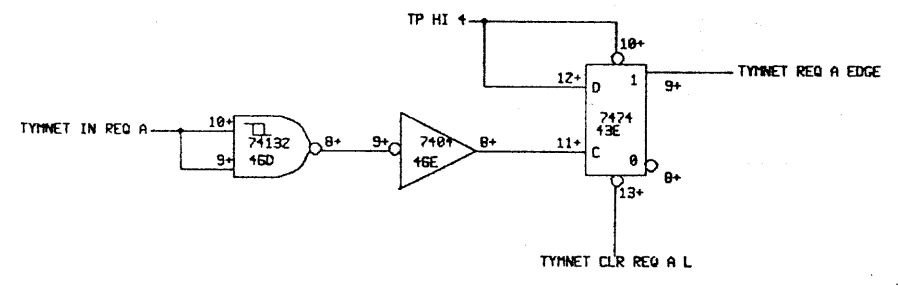
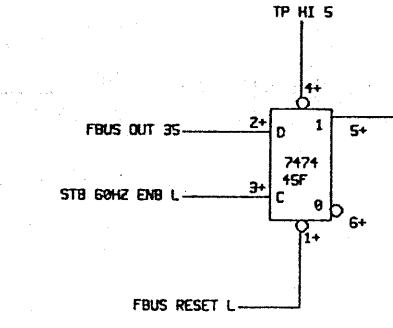
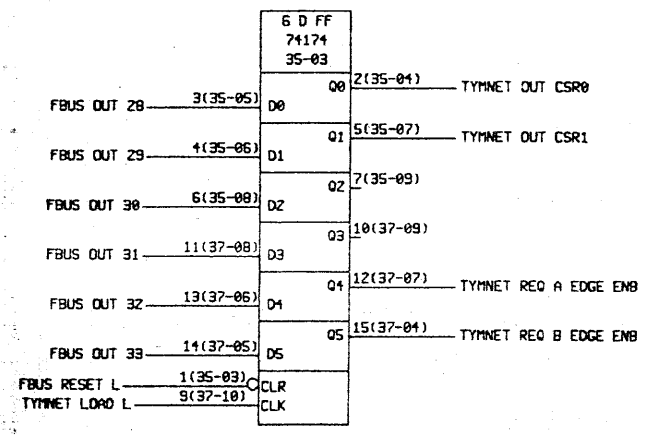
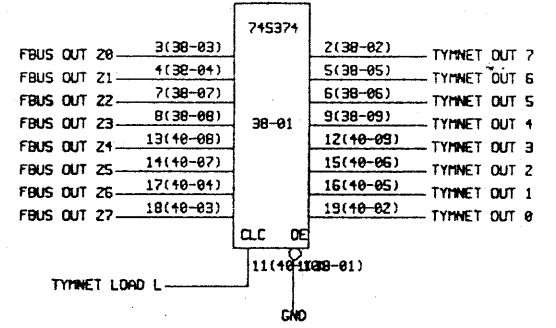
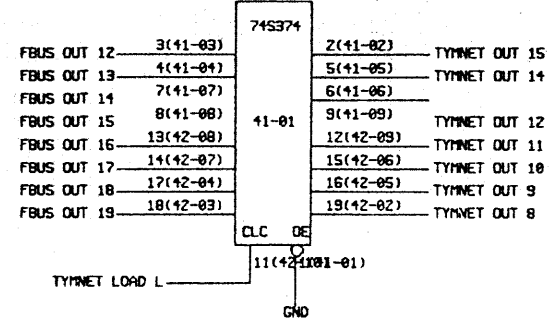
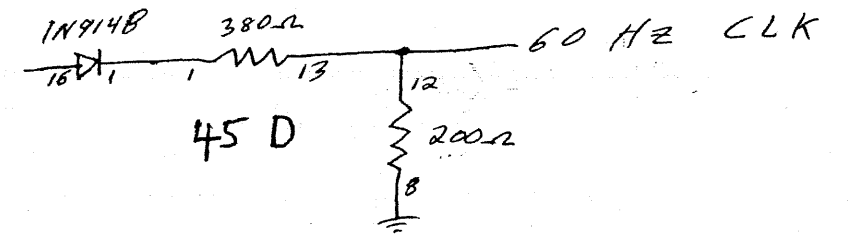
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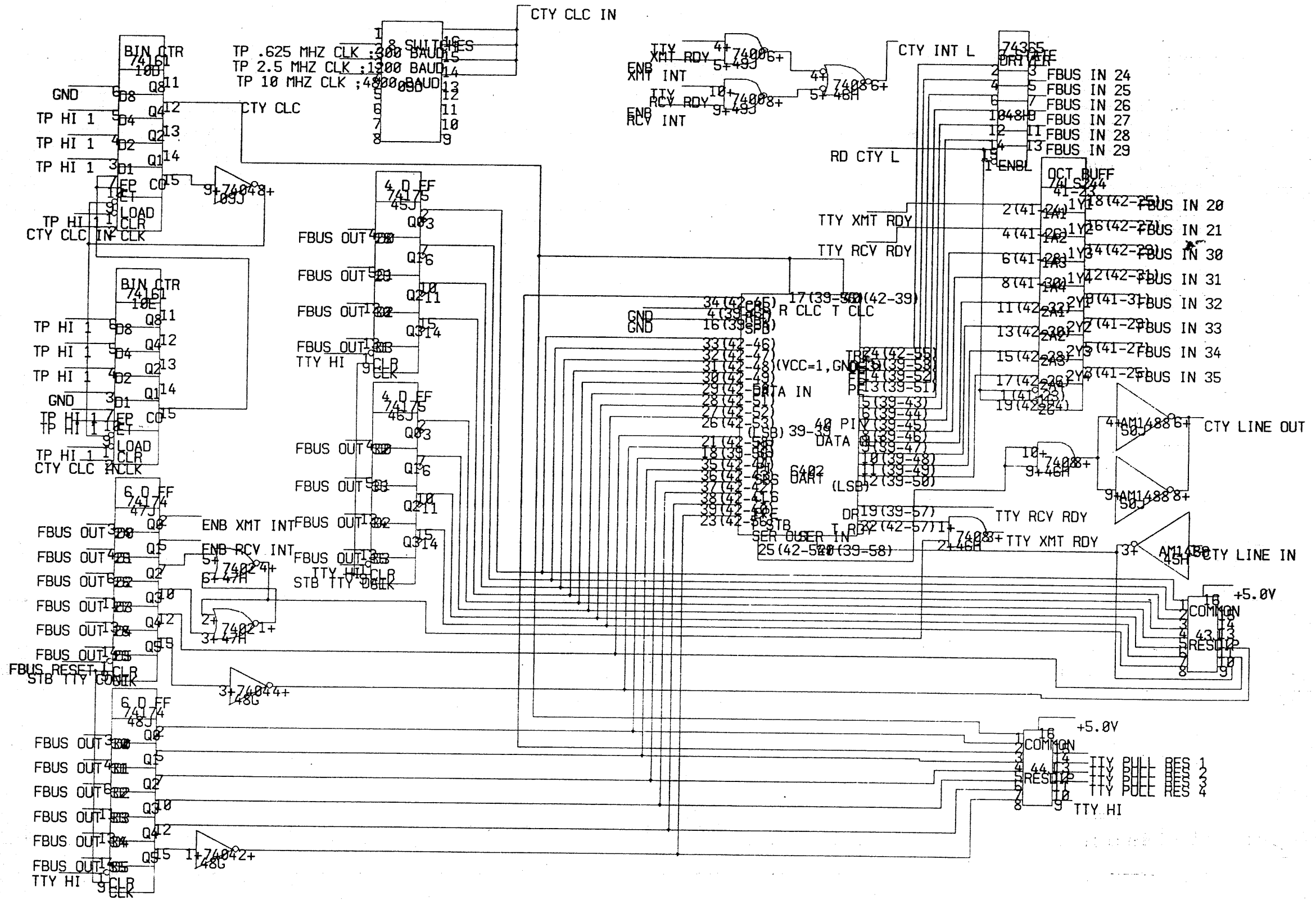
REV.



(C3C8)
60 HZ
CLK IN

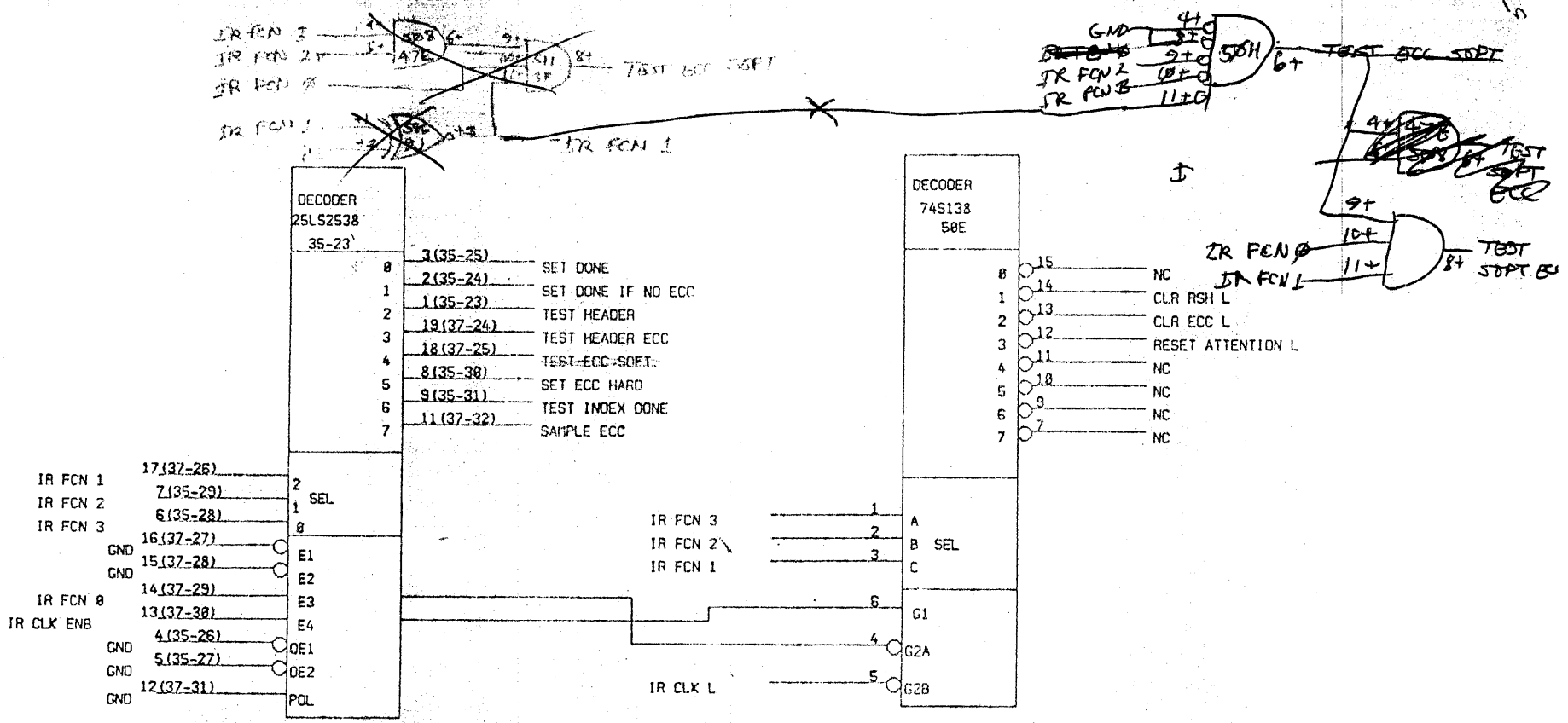


FOONLY, INC.		22-MAY-80 02:38	
DRAWN BY:		CFTNET.DRW (5157,4622)	
APPROVED BY:		NUMBER	REV.
PROJECT:		CFTA	



FOONLY, INC.		22-MAY-80 02:48	
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APPROVED BY:		PROJECT: FOONLY	NUMBER _____ REV. _____
		CFTA	

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FOONLY INCORPORATED		28-DEC-79 05:48	
DRAWN BY:		PAGE 1 OF 1	NUMBER
APPROVED BY:		PROJECT:	REV.
		UFUN, DRW (4, 41)	

removed :	(37-25)	-	7F10+	TEST ECC SOFT
added :	3F8+	-	7F10+	TEST ECC SOFT
	3F10+	-	(37-29)	IR FCN 0
	3F11+	-	(37-26)	IR FCN 1
	3F9+	-	50H6+	2+3
	50H-8+		50H-4+	GND
	50H-11+		50H-9G	GND
	50H-11+	-	50H-4+	GND
	(35-29)		50H-9+	IR FCN 2
	(35-28)		50H-10+	IR FCN 3