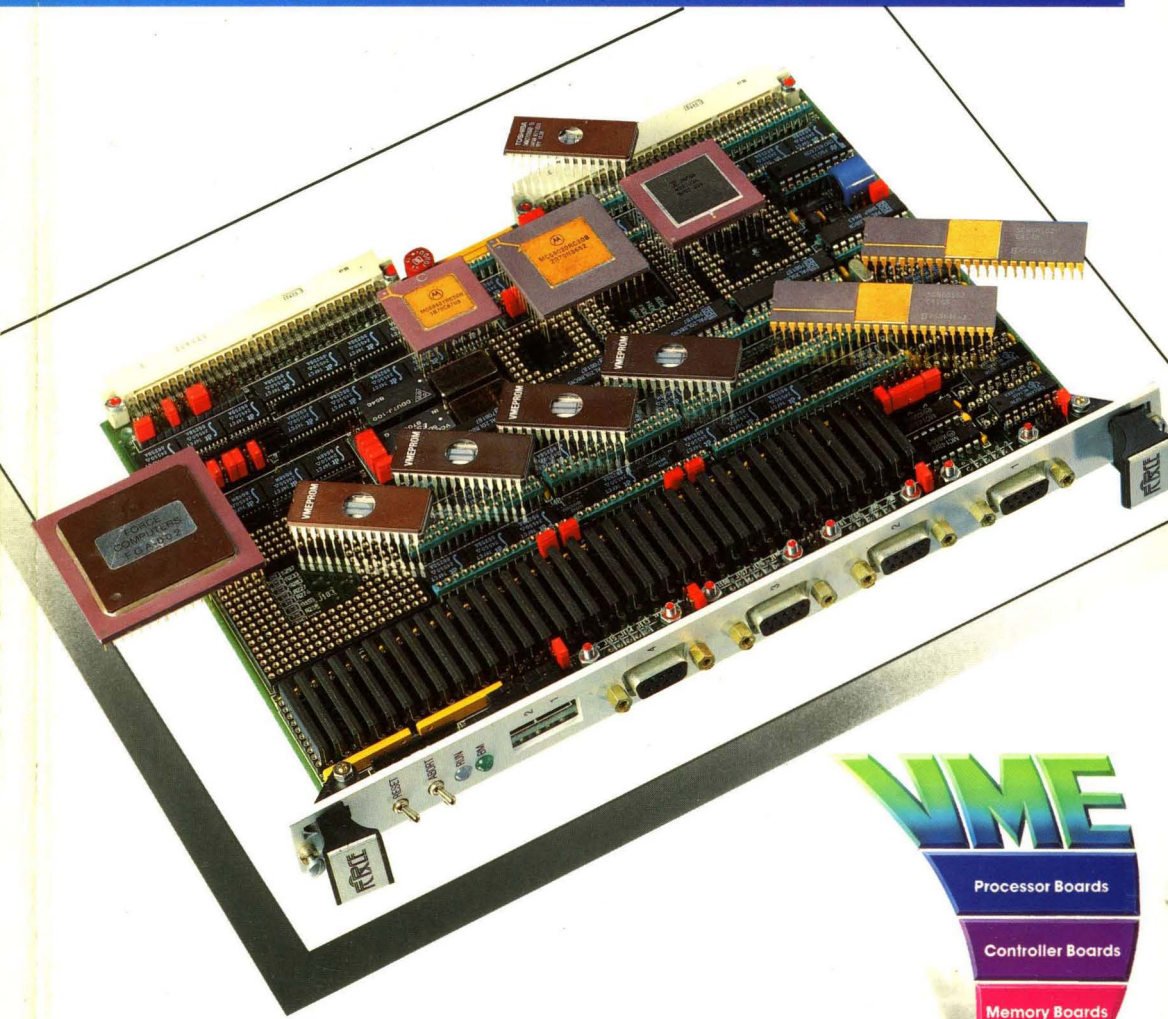
DATA BOOK 1988



VME

Processor Boards

Controller Boards

Memory Boards

I/O Boards

Systems

FORCE COMPUTERS®

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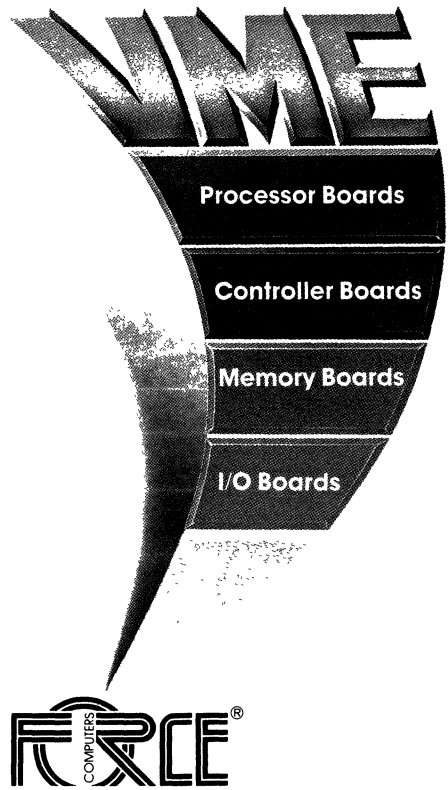
First Edition November 1986
Second Edition October 1987

DATA BOOK 1988

VMEbus Products



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Introduction to FORCE COMPUTERS Product Guide

Listed here you will find the FORCE COMPUTERS 1988 product guide. As you will see, in addition to the name of the product and the page on which information can be found, there are two additional columns.
These two additional columns signify that some of FORCE COMPUTERS' older products are not recommended for new designs. This means that if a product is not recommended for new design, you should consider using the suggested alternative in order to guarantee increased performance and functionality. FORCE COMPUTERS will continue to produce products that are not recommended for new designs for existing customers of those products. You will note that the products offered as suggested alternatives offer the same functionality and are often compatible. This ensures that you as a valued FORCE COMPUTERS customer are guaranteed product compatibility growth paths.

Part No.	Product	Description	Recommended for new Designs	Suggested Alternative	Details on Page
		16 bit CPU Boards			
100100	SYS68K/CPU-1B	68000/ 8.0 MHz/ 128 KB	No	CPU-6	69
100101	SYS68K/CPU-1C	68000/10.0 MHz/ 128 KB	No	CPU-6	69
100102	SYS68K/CPU-1D	68000/10.0 MHz/ 512 KB	No	CPU-6	69
100200	SYS68K/CPU-2	68000/ 8.0 MHz/ 256 KB	No	CPU-2B	37
100201	SYS68K/CPU-2A	68000/10.0 MHz/ 256 KB	No	CPU-2B	37
100202	SYS68K/CPU-2B	68000/10.0 MHz/ 512 KB	Yes		
100220	SYS68K/CPU-2D	68000/ 8.0 MHz/ 128 KB	No	CPU-2B	37
100205	SYS68K/CPU-2F	68000/10.0 MHz/1024 KB	Yes		
100211	SYS68K/CPU-2VA	68010/10.0 MHz/ 256 KB	No	CPU-2VB	37
100212	SYS68K/CPU-2VB	68010/10.0 MHz/ 512 KB	Yes		
100213	SYS68K/CPU-2VC	68010/10.0 MHz/1024 KB	Yes		
100300	SYS68K/CPU-3	68000/ 8.0 MHz/ 32 KB	No	CPU-3VB	45
100310	SYS68K/CPU-3V	68010/ 8.0 MHz/ 32 KB	No	CPU-3VB	45
100311	SYS68K/CPU-3VA	68010/10.0 MHz/ 32 KB	No	CPU-3VB	45
100312	SYS68K/CPU-3VB	68010/10.0 MHz/ 128 KB	Yes		
100401	SYS68K/CPU-4A	68000/12.5 MHz/ 32 KB	No	CPU-4VC	53
100410	SYS68K/CPU-4V	68010/10.0 MHz/ 32 KB	No	CPU-4VC	53
100411	SYS68K/CPU-4VA	68010/12.5 MHz/ 32 KB	No	CPU-4VC	53
100412	SYS68K/CPU-4VB	68010/12.5 MHz/ 128 KB	No	CPU-4VC	53
100413	SYS68K/CPU-4VC	68010/12.5 MHz/ 128 KB/BBU	Yes		
100501	SYS68K/CPU-5A	68000/16.7 MHz/ 128 KB/FPU	Yes		
100502	SYS68K/CPU-5V	68010/12.5 MHz/ 128 KB/FPU	No	CPU-5A	61
100601	SYS68K/CPU-6	68000/ 8.0 MHz/ 512 KB	Yes		
100602	SYS68K/CPU-6A	68000/12.5 MHz/ 512 KB	Yes		
100610	SYS68K/CPU-6VA	68010/12.5 MHz/ 512 KB	Yes		
100611	SYS68K/CPU-6VB	68010/12.5 MHz/ 512 KB/FPU	Yes		
		32 bit CPU Boards			
101041	SYS68K/CPU-21S	68020/12.5 MHz/ 512 KB/FPU	Yes		
101001	SYS68K/CPU-21	68020/16.7 MHz/ 512 KB/FPU	Yes		
101011	SYS68K/CPU-21A	68020/20.0 MHz/ 512 KB/FPU	Yes		
101021	SYS68K/CPU-21B	68020/25.0 MHz/ 512 KB/FPU	Yes		
101100	SYS68K/CPU-22	68020/16.7 MHz/ 256 KB/FGA-002	Yes		
101101	SYS68K/CPU-22A	68020/20.0 MHz/ 256 KB/FGA-002	Yes		
101102	SYS68K/CPU-22XA	68020/20.0 MHz/ 1 MB/FGA-002	Yes		
101210	SYS68K/CPU-25	68020/16.7 MHz/ 512 KB/MMU/FPU	Yes		
101130	SYS68K/CPU-26X	68020/16.7 MHz/ 256 KB/SCSI/FGA-002	Yes		
101131	SYS68K/CPU-26XA	68020/20.0 MHz/ 256 KB/SCSI/FGA-002	Yes		
101132	SYS68K/CPU-26ZA	68020/20.0 MHz/ 1 MB/SCSI/FGA-002	Yes		
101150	SYS68K/CPU-29XS	68020/12.5 MHz/ 1 MB/FPU/FGA-001	Yes		
101152	SYS68K/CPU-29X	68020/16.7 MHz/ 1 MB/FPU/FGA-001	Yes		
101153	SYS68K/CPU-29XB	68020/25.0 MHz/ 1 MB/FPU/FGA-001	Yes		
101154	SYS68K/CPU-29XC	68020/30.0 MHz/ 1 MB/FPU/FGA-001	Yes		
101323	SYS68K/CPU-32XS	68030/12.5 MHz/ 1 MB/FPU/FGA-001	Yes		
101324	SYS68K/CPU-32X	68030/16.7 MHz/ 1 MB/FPU/FGA-001	Yes		
101321	SYS68K/CPU-32XA	68030/20.0 MHz/ 1 MB/FPU/FGA-001	Yes		
101322	SYS68K/CPU-32XB	68030/25.0 MHz/ 1 MB/FPU/FGA-001	Yes		
101333	SYS68K/CPU-32XC	68030/30.0 MHz/ 1 MB/FPU/FGA-001	Yes		
105000	SYS80K/CPU-386-1	80386/16.0 MHz/ 2 MB	Yes		
105001	SYS80K/CPU-386-1A	80386/16.0 MHz/ 2 MB/FPU	Yes		
		16 bit Memory Board Products			
200000	SYS68K/DRAM-1	512 KB DRAM A24 : D16	Yes		
200001	SYS68K/DRAM-2	2 MB DRAM A24 : D16	Yes		
200010	SYS68K/RR-1	NAKED ROM/PROM/EPROM/SRAM	Yes		
200011	SYS68K/RR-1S	128 KB SRAM A24 : D16	Yes		
200020	SYS68K/SRAM-1	128 KB SRAM A24 : D16	No	SRAM-5	265
200021	SYS68K/SRAM-2	512 KB SRAM A24 : D16	No	SRAM-5	265

Part No.	Product	Description	Recommended for new Designs	Suggested Alternative	Details on Page
		32 bit Memory Board Products			
200004	SYS68K/DRAM-E-3M1	1 MB DRAM A32 : D32 MASTER	Yes		
200103	SYS68K/DRAM-E-3S3	3 MB DRAM EXTENSION SLAVE	Yes		
200110	SYS68K/DRAM-E4M4	4 MB DRAM A32 : D32 MASTER	Yes		
200113	SYS68K/DRAM-E4S12	12 MB DRAM EXTENSION SLAVE	Yes		
200130	SYS68K/DRAM-6	2 MB DRAM A32 · D32 VERY FAST	Yes		
200300	SYS68K/RR-2	NAKED PROM/EPROM/EEPROM	Yes		
200600	SYS68K/RR-3	NAKED PROM/EPROM/EEPROM	Yes		
200401	SYS68K/SRAM-3A	512 KB SRAM A32 : D32 VME/VMX	No	SRAM-5	265
200402	SYS68K/SRAM-3B	1 MB SRAM A32 : D32 VME/VMX	Yes		
200501	SYS68K/SRAM-4A	512 KB SRAM A32 : D32 VME	No	SRAM-5	265
200502	SYS68K/SRAM-4B	1 MB SRAM A32 : D32 VME	Yes		
200504	SYS68K/SRAM-5	512 KB SRAM A32 : D32 VME	Yes		
201000	SYS68K/SRAM-22	512 KB MEM. EXP. CPU-21/25	Yes		
201040	SYS68K/SRAM-22S	512 KB MEM. EXP. CPU-21S	Yes		
201010	SYS68K/SRAM-22A	512 KB MEM. EXP. CPU-21A	Yes		
201020	SYS68K/SRAM-22B	512 KB MEM. EXP. CPU-21B	Yes		
		Controller Boards			
300000	SYS68K/SASI-1	SASIBUS HOST CONTR.	No	ISCSI-1	301
300001	SYS68K/WFC-1	WINCH/FLOPPY CONTR.	Yes		
300020	SYS68K/ISCSI-1	INTELL. SCSI CONTR., 128 KB SRAM	Yes		
300023	SYS68K/ISCSI-1A	INTELL. SCSI CONTR., 512 KB SRAM	Yes		
400010	SYS68K/CMC-1	COLOR MONITOR CONTR.	No	AGC-2	331
400004	SYS68K/GDC-1M+1S	GRAPH. MASTER CONTR. + GDC-1S	No	AGC-2	331
400007	SYS68K/GDC-1S2	GRAPH. SLAVE POS. 2	No	AGC-2	331
400008	SYS68K/GDC-1S3	GRAPH. SLAVE POS. 3	No	AGC-2	331
400020	SYS68K/AGC-1	ADVANCED GRAPHICS CONTR.	Yes		
400022	SYS68K/AGC-1X	ADVANCED GRAPHICS CONTR. EXT.	Yes		
400023	SYS68K/AGC-2	GRAPHICS CONTROLLER	Yes		
700006	SYS68K/ASCU-1	ADVANCED SYS. CONT. UNIT	Yes		
700007	SYS68K/ASCU-2	ADVANCED SYS. CONT. W GPIB	Yes		
300100	SYS68K/ILANC-1	INTELLIGENT ETHERNET CONTROLLER	Yes		
		INPUT/OUTPUT Boards			
310000	SYS68K/SIO-1	6 CHANNEL SER. I/O	No	SIO-2	379
310004	SYS68K/SIO-2	6 CHANNEL SER. I/O	Yes		
310005	SYS68K/SIO-2A	6 CHANNEL SER. I/O, OPTICAL LINKS	Yes		
310030	SYS68K/ISIO-1	8 CHANNEL SER. I/O, 128 KB SRAM	Yes		
310035	SYS68K/ISIO-1A	8 CHANNEL SER. I/O, 512 KB SRAM	Yes		
310031	SYS68K/ISIO-2	8 CHANNEL SER. I/O, 128 KB SRAM	Yes		
310036	SYS68K/ISIO-2A	8 CHANNEL SER. I/O, 512 KB SRAM	Yes		
310011	SYS68K/OPIO-1	PAR. I/O : OPTO. COUP.	Yes		
310010	SYS68K/PIO-1	PARALLEL I/O : TTL	Yes		
320002	SYS68K/AD-10A	12 BIT A/D CONV., 20 MICROSEC.	Yes		
320003	SYS68K/AD-10B	12 BIT A/D CONV., 4 MICROSEC.	Yes		
320004	SYS68K/AD-10C	14 BIT A/D CONV., 35 MICROSEC.	Yes		
320006	SYS68K/AD-10D	16 BIT A/D CONV., 400 MICROSEC.	Yes		
320007	SYS68K/AD-11A	12 BIT A/D CONV., 20 MICROSEC., 2 D/A	Yes		
320008	SYS68K/AD-11B	12 BIT A/D CONV., 4 MICROSEC., 2 D/A	Yes		
320009	SYS68K/AD-11C	14 BIT A/D CONV., 35 MICROSEC., 2 D/A	Yes		
320010	SYS68K/AD-11D	16 BIT A/D CONV., 400 MICROSEC., 2 D/A	Yes		
320011	SYS68K/AD-12	16 CHANNEL S/H EXPANS. FOR AD-10/11	Yes		
320012	SYS68K/AD-13H	8 CHANNEL HIGH VOLTAGE EXP. FOR AD-10/11	Yes		
320013	SYS68K/AD-14	32 CHANNEL HIGH LEVEL INPUT EXP. FOR AD-10/11	Yes		
320014	SYS68K/DA-1A	8 CHANNEL D/A CONV., 12 BIT	Yes		
320015	SYS68K/DA-1B	8 CHANNEL D/A CONV., 12 BIT, CURRENT LOOP OUTPUT	Yes		
320016	SYS68K/DA-2A	6 CHANNEL D/A CONV., 16 BIT	Yes		
320017	SYS68K/DA-2B	6 CHANNEL D/A CONV., 16 BIT	Yes		

Part No.	Product	Description	Recommended for new Designs	Suggested Alternative	Details on Page
		System Products			
620510	miniFORCE 1P1	PDOS SYSTEM/CPU-1D/3U	No	miniFORCE 1P6	433
620550	miniFORCE 1P5	PDOS SYSTEM/CPU-5V/3U	No	miniFORCE 2P5	435
620560	miniFORCE 1P6	PDOS SYSTEM/CPU-6/3U	Yes		
620610	miniFORCE 2P1	PDOS SYSTEM/CPU-1D/7U	No	miniFORCE 2P6	435
620620	miniFORCE 2P2	PDOS SYSTEM/CPU-2VC/7U	Yes		
620640	miniFORCE 2P4	PDOS SYSTEM/CPU-4VC/7U	Yes		
620650	miniFORCE 2P5	PDOS SYSTEM/CPU-5A/7U	Yes		
620660	miniFORCE 2P6	PDOS SYSTEM/CPU-6VB/7U, WFC	Yes		
620662	miniFORCE 2P6I	PDOS SYSTEM/CPU-6VB/7U, ISCSI	Yes		
620700	miniFORCE 2P21	PDOS SYSTEM/CPU-21/7U	Yes		
620710	miniFORCE 2P21S	PDOS SYSTEM/CPU-21S/7U	Yes		
620720	miniFORCE 2P21A	PDOS SYSTEM/CPU-21A/7U, WFC	Yes		
620722	miniFORCE 2P21AI	PDOS SYSTEM/CPU-21A/7U, ISCSI	Yes		
630005	microFORCE 1A	UNIX SYSTEM/CPU-3VB/3U	Yes		
630010	microFORCE 2	UNIX SYSTEM/CPU-3VB/7U	Yes		
640021	FORCE FOCUS 32 PDOS SYSTEM 21A	PDOS SYSTEM/CPU-21A	Yes		
640022	FORCE FOCUS 32 PDOS SYSTEM 21B	PDOS SYSTEM/CPU-21B	Yes		
641025	FORCE FOCUS 32 SYSTEM 25U	UNIX SYSTEM/CPU-25	Yes		
		Software Products			
140020	SYS68K/PDOS-PAS	PDOS PASCAL	Yes		
140021	SYS68K/PDOS-PAS020	PDOS PASCAL FOR 68020	Yes		
140040	SYS68K/PDOS-FOR	PDOS FORTRAN-77	Yes		
140041	SYS68K/PDOS-FOR020	PDOS FORTRAN-77 FOR 68020	Yes		
140030	SYS68K/PDOS-C	PDOS "C" COMPILER	Yes		
140031	SYS68K/PDOS-C020	PDOS "C" COMPILER FOR 68020	Yes		
140044	SYS68K/PDOS-BAS	PDOS BASIC FOR 68000/68010	Yes		
140045	SYS68K/PDOS-BAS020	PDOS BASIC FOR 68020	Yes		
150005	SYS68K/UNIX-PAS	UNIX PASCAL	Yes		
150006	SYS68K/UNIX-PAS020	UNIX PASCAL	Yes		
160000	SYS68K/GKSGRAL-P2B1	GKS SOFTWARE FOR PDOS	Yes		
160001	SYS68K/GKSGRAL-P2B1	GKS SOFTWARE FOR UNIX	Yes		
		Accessory Products			
500005	SYS68K/MOTH-05A	5 SLOT MOTHERBOARD	Yes		
500011	SYS68K/MOTH-09A	9 SLOT MOTHERBOARD	Yes		
500006	SYS68K/MOTH-12A	12 SLOT MOTHERBOARD	Yes		
500013	SYS68K/MOTH-20A	20 SLOT MOTHERBOARD	Yes		
500007	SYS68K/MOTH-21A	21 SLOT MOTHERBOARD	Yes		
500008	SYS68K/MOTH-E05A	5 SLOT 32 BIT EXTENSION	Yes		
500012	SYS68K/MOTH-E09A	9 SLOT 32 BIT EXTENSION	Yes		
500009	SYS68K/MOTH-E12A	12 SLOT 32 BIT EXTENSION	Yes		
500014	SYS68K/MOTH-E20A	20 SLOT 32 BIT EXTENSION	Yes		
500010	SYS68K/MOTH-E21A	21 SLOT 32 BIT EXTENSION	Yes		
610101	SYS68K/CHAS 19-09E/7HE	CHAS 19-09/7HE PLUS P2 MOTH	Yes		
610105	SYS68K/CHAS 19-21E/7HE	CHAS 19-21/7HE PLUS P2 MOTH	Yes		
610191	SYS68K/CHAS 19-21E/12HE	12HE CHASSIS W 21 SLOTS	Yes		
610005	SYS68K/RACK 19-09A	19" RACK WITH 9 SLOT MOTH	Yes		
610025	SYS68K/RACK 19-21A	19" RACK WITH 21 SLOT MOTH	Yes		
700008	SYS68K/PWR-09A	280 W PWR SUPPLY	Yes		
700018	SYS68K/PWR-09AC	PWR-09A POWER CABLE	Yes		
700009	SYS68K/PWR-20	750 W PWR SUPPLY	Yes		
700030	SYS68K/PWR-20C	PWR-20 POWER CABLE	Yes		
700040	SYS68K/STR-120	120 MB STREAMER FOR FOCUS 32	Yes		
700002	SYS68K/WFMOD-20	20 MB WIN/1 MB FLOPPY	Yes		
700020	SYS68K/WFMOD-50	50 MB WIN/1 MB FLOPPY	Yes		
700012	SYS68K/WFMOD-85	80 MB WIN/1 MB FLOPPY	Yes		
700022	SYS68K/WFMOD-175	175 MB WIN/1 MB FLOPPY	Yes		

Manufacturing

The task of the Manufacturing Department is to convert the high-tech designs developed by the Engineering Department into top-quality, long-lived products. The manufacturing system at each working location is defined by considerations of "integrated quality" (see the Q.A. section of the Data Book). Capacity shortages caused by a large backlog or by machine down times must be absorbed by overtime and may not lead to any degradation of production quality.

Production Planning

The major elements of production planning are to ensure a timely delivery of the backlog and to provide a sufficient number of products for the activities of the Sales Organization. This is based on the sales forecast and the sales volume of the past months. Additional customer orders which are very urgent should be shipped from a specified minimum stock acting as a buffer.
The production schedule must always be adjusted to the limited manufacturing capacities of the various steps in a simultaneous planning action. The capacities of the Testing and Manufacturing Departments are continuously expanded with the growth of the company. This results in a timely reaction to the steadily increasing manufacturing volume. Therefore, it is easier to allow for short-time utilization peaks and urgent OEM orders in the production environment.

Component Purchasing

In every design, the manufacturers for the components used are approved by the Engineering Department. Only components of leading suppliers will be approved. If the Manufacturing or Purchasing Department suggests additional suppliers for specific components, a very strict approval procedure is applied under Q.A. control.
The demand for each component is determined by the MRP Computer System (Manufacturing Requirement Planning) based on the current Production Schedule. Generally, OEM delivery contracts are made with large and renowned manufacturers to ensure that the end products can be manufactured and sold at a low cost. The secured delivery due to the long-term delivery dates is an additional feature of these contracts. With the exception of "sole-source products", a risk spreading results from the availability of strategically important products from different suppliers. A lot of emphasis is put on the purchasing procedures, as this element accounts for a major part of the company's profits.

Component Receiving Quality Control

The Component Receiving Department utilizes its own quality control regulations. Apart from the outward appearance of the incoming products, the internal manufacturer approval, the date codes, the mask revisions etc. will be checked. Special emphasis is put on PCB control, as any inadequate quality which is not detected at this point may lead to major problems in the production flow. Thus, significant time is dedicated to this task.
The component storage is exactly defined and controlled (e.g. the tested printed circuit boards must be hermetically sealed).

Pick Generation

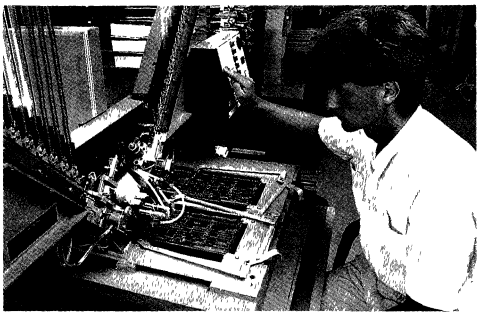
The production lots are approved by the Manufacturing Planning according to the production plan so that the picks may be generated in the component warehouse. First, the PALs and EPROMs are transferred to the production floor to be programmed in parallel to the pick generation. Thus, completed picks will leave the warehouse.
If any parts are missing, the Purchasing Department intervenes in order to identify the whereabouts of the respective products. A second warehouse employee will check the completed pick for 100% completeness before it is transferred to the production area. Thus, production delays due to missing parts have been reduced to a minimum.

Manufacturing Planning Tracking

Here, the production documents are generated, updated and checked in coordination with the Product Engineering. Based on detailed, controlled procedures, this department implements the Engineering Change Orders (ECO's) in order to ensure a maximum degree of transparency as far as board and product revision is concerned. The implementation of ECO's is organized worldwide and is monitored by Q.A. At the individual levels, the material and product flow is controlled by Manufacturing Planning based on deadlines and lot sizes.

Board Assembly

Assembly is carried out according to strict quality regulations for insertion. Depending on the complexity, manual, semi-automatic or automatic insertion is used. All Q.A. measures which are a standard in advanced insertion companies are implemented in the production floors.
A detailed Quality Report is submitted to each assembly area at the end of each month in order to maintain and improve the quality level.
Initial products for SMT (Surface Mount Technology) have been integrated into the production on a mixed-insertion basis. Future designs will signifcantly expand this production area, and the production floors are well prepared for these enhancements.



Incircuit Test

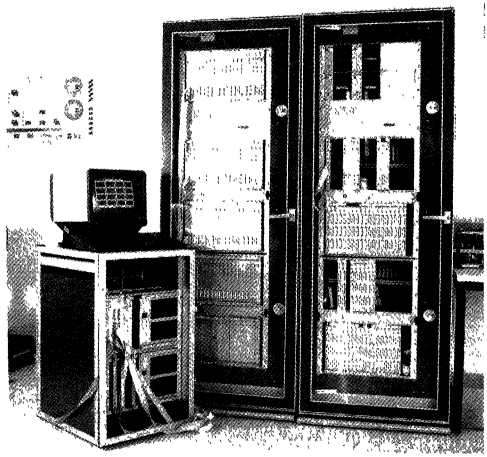
Currently, all boards are tested in-circuit using Genrad testing equipment. The bed of nails and the test program for each product are generated, modified and improved at the Design Center which developed the product. All other in-circuit test facilities are supplied with adapters and programs from one central source. Thus, uniform testing is ensured at FORCE Computers facilities all over the world.
Dedicated software in the test computer generates test reports at the product and component levels. Among others, this information is available to the Q.A. or the Purchasing Department. Hence, specific component suppliers may be excluded from further delivery if any inadequate quality should be detected.
If a proprietary customer-specific production lot cannot be tested with the ICT Program of the standard FORCE product, the ICT program (and the test adapter sometimes even) will be modified. An electrically tested product is to be delivered to the customer.

Functional Test

In this section, the on-board functions are checked under real-time conditions and in an operating environment the board will typically be exposed to. These test programs are also generated, modified and expanded in Design Centers in a centralized manner, so that identical functional tests will be used for a specific product all over the world. For newly introduced products, a team of programmers is constantly developing new program modules which are integrated into the functional-test programs. In addition, the test programs are also maintained, expanded and improved with respect to their test depth.

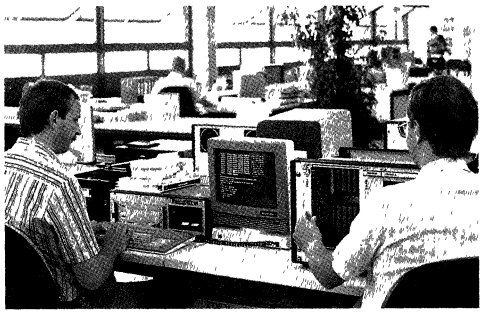
Burn-in Test

Burn-in tests are carried out for at least 48hrs. at a minimum of 50° C. For this purpose, test racks have been developed which provide a VME operating environment for the boards under test. A high-performance control system operating in a real-time, multi-tasking mode controls and monitors the test racks and the testing tasks.
All burn-in test departments all over the world are equipped with these test racks along with the control unit.
After passing the burn-in test, the board is provided with its default setting and submitted to the Q.A. Outgoing Inspection.



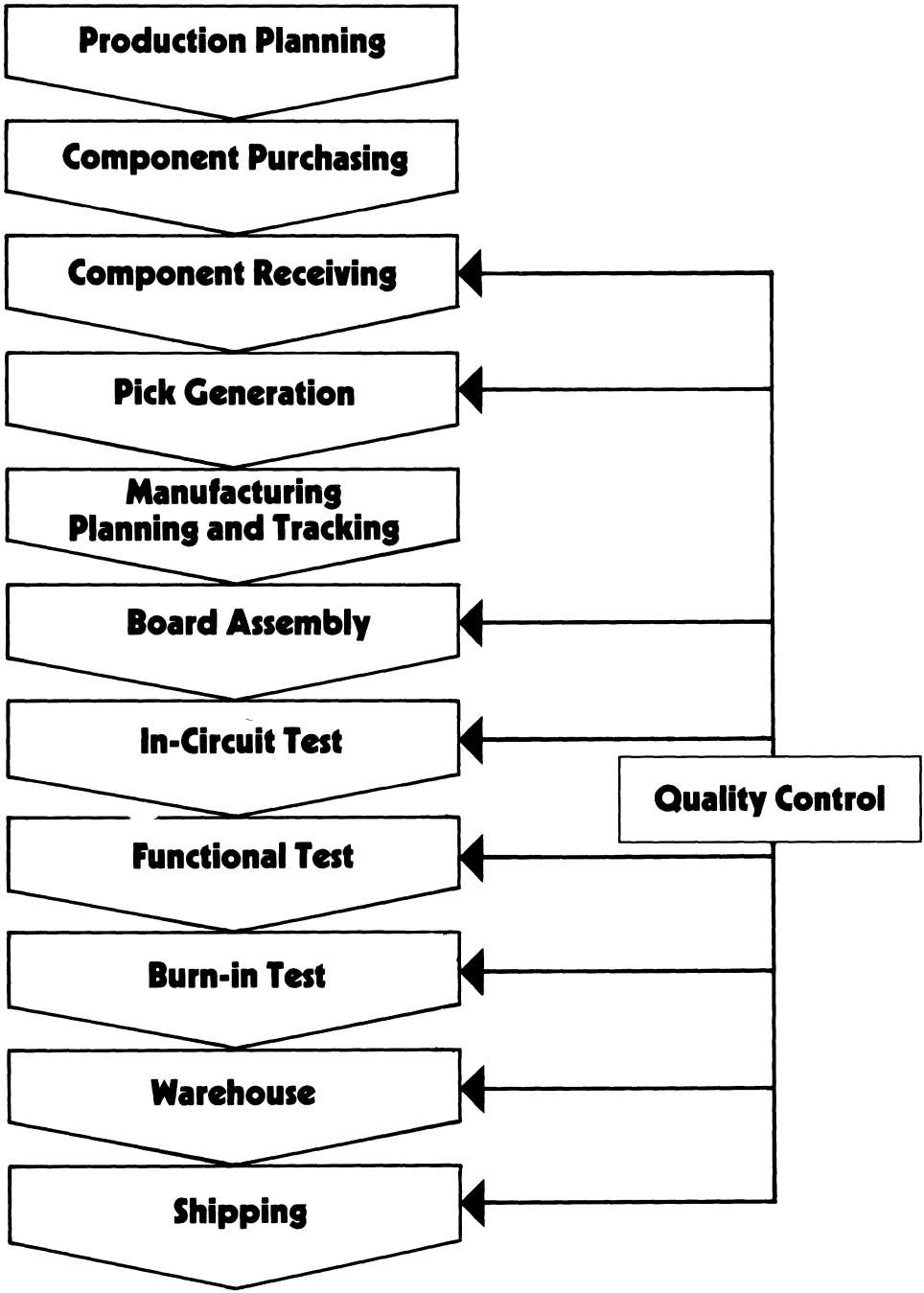
System Generation

Apart from board-level products, FORCE also offers entire control and development systems.
In the System Generation Department, Systems are mounted in standard configurations or according to the customer's specifications. In addition, the software is loaded (the user has the choice among several operating systems), tested and approved by the Q.A. Each system passes a functional test and a burn-in test of at least 16hrs. As the FORCE boards for these systems are taken from the Finished Goods Warehouse, only entirely tested products are used.
The System Generation Department is expanding rapidly, not least as a result of the new System Generation. Thus, it is especially in this department that methods are sought which promise to increase productivity (improved material flow, use of production components, standardizations, etc). In spite of the dramatic increase in the system-level business, FORCE Computers is still a company which sees itself as a board-level supplier in the first instance.



Warehouse Shipping

Following the outgoing inspection carried out by the Q.A., the boards and systems are transferred to the Finished Goods Warehouse, where the products are stored in antistatic and dust-proof packages.
The backlog determines when the goods are prepared for shipping, when the documentation is included and when they are put into the shipping boxes.
Generally, the customer will specify the shipment procedure. However, in case of very urgent orders, FORCE provides its expertise and connections to the optimum means of transportation in order to ensure a timely delivery. For this purpose, FORCE has set up a special customs service.
Practical packaging, professional documentation and fast delivery are additional features which give the final touch to FORCE Computer's high-tech products.


Production Planning
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Quality Control

Quality Assurance

FORCE Computers' quality system incorporates a total quality assurance concept encompassing management, design, purchasing, manufacturing, test, inspection, and documentation. The quality control program established and maintained insures that products conform to published specifications and customer quality requirements. Records demonstrating the effective operation of the quality system are available for review at FORCE Computers by designated purchasing authorities and source inspectors.

I. Organization
Quality is the responsibility of management and it is the policy of management that quality needs to be controlled. A quality assurance organisation must be independent of other organisations in order to function effectively.
FORCE Computers' quality assurance manager reports directly to the general manager and has the authority to resolve matters pertaining to quality.
Responsibility and authority is delegated to those personnel performing quality functions in order to identify and evaluate quality problems, and to iniate, recommend, or provide solutions. Management regularly reviews the status and adequacy of the quality program.

II. Records
Records are one of the prinicipal forms of objective evidence of quality. FORCE Computers maintains and uses records for inspection and test, corrective actions, and calibration.
Test and inspection records are maintained indicating the nature or type of observation, the number of observations made, and number and type of deficiencies found. Corrective action records detail the nature of the action and effective dates of correction. Records showing calibration history and status are maintained for test and measurement equipment.

III. Documentation and Change Control
In industries where innovation, redesign, and product improvement are continuously practiced, control of documentation is of critical importance to product quality and reliability.
FORCE Computers maintains control of all documentation relating to the design and manufacture of its products. Current issues of appropriate documents are available at all locations where operations essential to the effective functioning of the quality system are performed. All changes to documentation are in writing and records of changes made are maintained.

IV. Statistical Quality Control and Analysis
FORCE Computers utilizes statistical analysis and tests to maintain the required control of quality. Sampling inspection is performed in accordance with MIL-STD-105D, table II-A.
Acceptable quality levels (AQL) are applied at receiving inspection and final electrial and mechanical/visual inspection.
Utilizing modern test equipment, data is generated and analyzed pertaining to yields and product quality trends. As a result, causes of defects or significant variations in manufacturing operations can be identified and the necessary corrective actions implemented in a timely manner.

V. Control of Inspection, Measuring, and Test Equipment.
All test and measurement equipment is maintained and controlled to insure product conformance to specifications and required quality levels. Calibration records are maintained and equipments are labeled showing calibration intervals and status. The calibration system conforms with »Nato Measurement and Calibration System Requirements for Industry« (AQAP-6).

VI. Test Programs and Procedures
FORCE Computers has developed sophisticated test programs utilizing state-of-the-art test and measurement equipment for its board level and system products.
Board level products are subjected to 100 percent in-circuit test using a GENRAD 2276E or equivalent automatic tester (bed of nails). Data related to yields and product quality trends is collected, analysed, and used as a basis for product improvement programs. Defect data feedback is used to initiate corrective actions.
Utilizing proprietary test programs in imbedded software, all board level products are tested for functionality in a VME System environment simulating the end use of the product. Processor, memory, and controller chips, for example are exercised to test performance in the intended application. In order to screen out infant mortalities all CPU I/O and RAM boards are subjected to a dynamic burn-in for 48 hours at 50 degrees centigrade, minimum.
Real-time software driven test programs have been developed enabling board level products to be tested in functional environments at elevated ambient temperatures.
A post test electrical and visual sample inspection is performed on all finished products to verify that all tests have been completed as specified.
All systems are functionally tested and a minimum 24 hour duration test is performed at room ambient temperatures. Prior to shipment a final q.c. electional and visual inspection is performed on all systems.

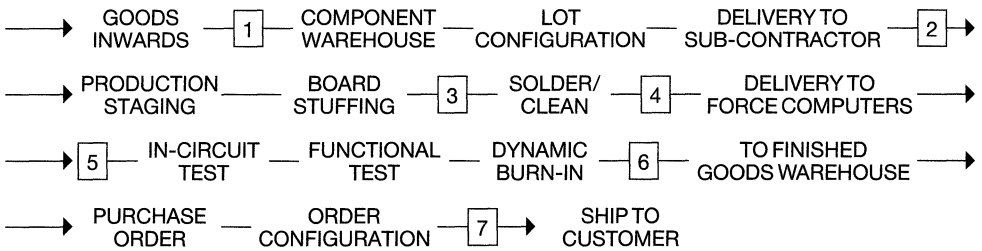
VII. Standards and Specifications

The quality system implemented at FORCE Computers conforms with and applies the following standards and specifications.

BS5750 – Part 1	Specification for design, manufacture and installation.
MIL-Q-9858A	Quality program requirements.
AQAP-1	NATO Quality Control System Requirements for Industry.
AQAP-6	NATO Measurement and Calibration System Requirements for Industry.
IPC-SM-840	Qualification and performance of permanent polymer coatings.
MIL-P-55110C	Military specification printed wiring boards.
IPC-A-600C	Acceptability of printed wiring boards.
IPC-ML-910A	Design and end production spec. for rigid multi-layer boards.
MIL-STD-275D	Printed wiring for electronic equipment.

Workmanship standards as published by Martin Marietta Aerospace.

VIII. Material Flow Chart



Q.C. INSPECTION POINTS

1. Sample Visual AQL 1.0
2. Sample Visual AQL 1.0
3. Sample Visual AQL 1.0
4. 100% Visual
5. Sample Visual AQL 1.0
6. Sample Electrical AQL 1.0/100% Visual
7. Purchase Order, Documentation, Packaging

A comprehensive description of the quality system implemented by FORCE Computers is available in handbook form:

Quality Assurance and Reliability Handbook
First Edition, June 1987

Part No. 800450

16 Bit CPU Boards

FORCE Computers 16 bit CPU Board Introduction

There are six basic designs in the FORCE family of 16 bit CPU boards. All the designs are available with a variety of options, which makes this family of boards one of the broadest and most comprehensive available in today's 16 bit CPU marketplace.

General Feature Overview

For general purpose flexibility and functionality, the SYS68K/CPU-6 and the SYS68K/CPU-1 families provide all the features that the user could ever need. The CPU-6 family was designed as a functional update for the extremely popular CPU-1 family. The CPU-1 family was designed to rev. B of the VMEbus specification and provides ample RAM and EPROM areas for most small to medium sized applications. The family also includes 3 serial I/O ports as standard. The CPU-6 was designed to provide complete S/W compatibility to the CPU-1 family, provides all the same features, whilst conforming fully to the IEEE 1014 standard (Rev C. specification). In addition an optional 68881 floating point co-processor was included. The CPU-1 and CPU-6 families are the general purpose solution.

If you require a standalone CPU board with sufficient memory and I/O capability to manage small applications without the need for extra boards, then the SYS68K/CPU-2 family of boards may suit your requirements. The board has up to 512 Kbyte of memory, optional floppy disk controller, 32 Kbyte EPROM and serial and parallel I/O capabilities. The CPU-2 is the single board solution.

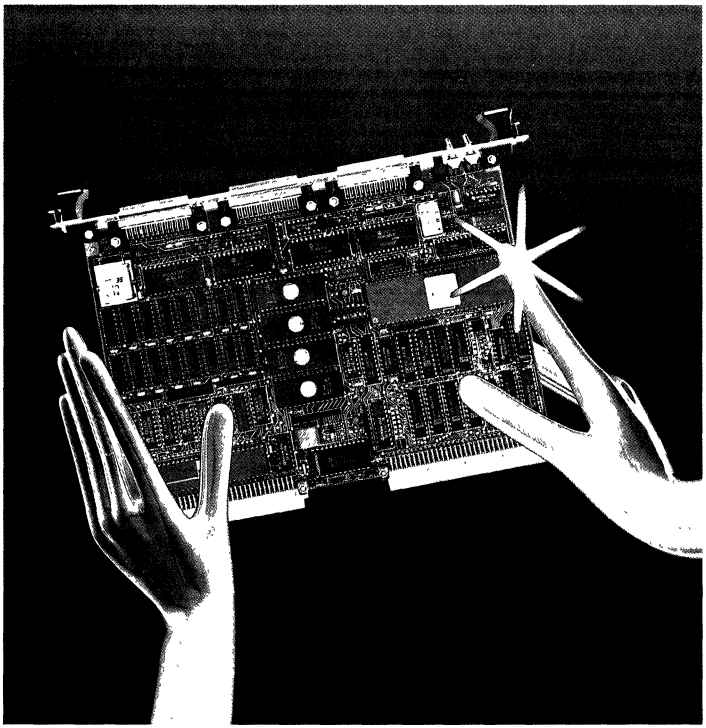
If memory management and data protection is in your specification, then the SYS68K/CPU-3 family is the product for you. The 68010 CPU coupled with the 68451 memory management unit (MMU) and the 68450 DMA controller means that this board is ideally suited to UNIX type environments. The CPU-3 family is the memory managed solution.

If your application requires that small to medium sized applications be committed to EPROM, then the SYS68K/CPU-4 family is designed especially for you. With 8 JEDEC compatible sockets, the user is provided with a potential 512 Kbyte of EPROM space. Coupled with the powerful 68010 microprocessor, DMA controller with optional floppy dosk controller and serial and parallel I/O, the CPU-4 family is the standalone solution.

For true raw performance, the SYS68K/CPU-5 family provides the maximum computing power available with a 16 bit 68000 microprocessor. With the local CPU and floating point co-processor running at a blistering 16.67MHz and with the 128 Kbyte of local RAM inducing no wait states on the CPU, the CPU-5A is the 68000 performance standard.

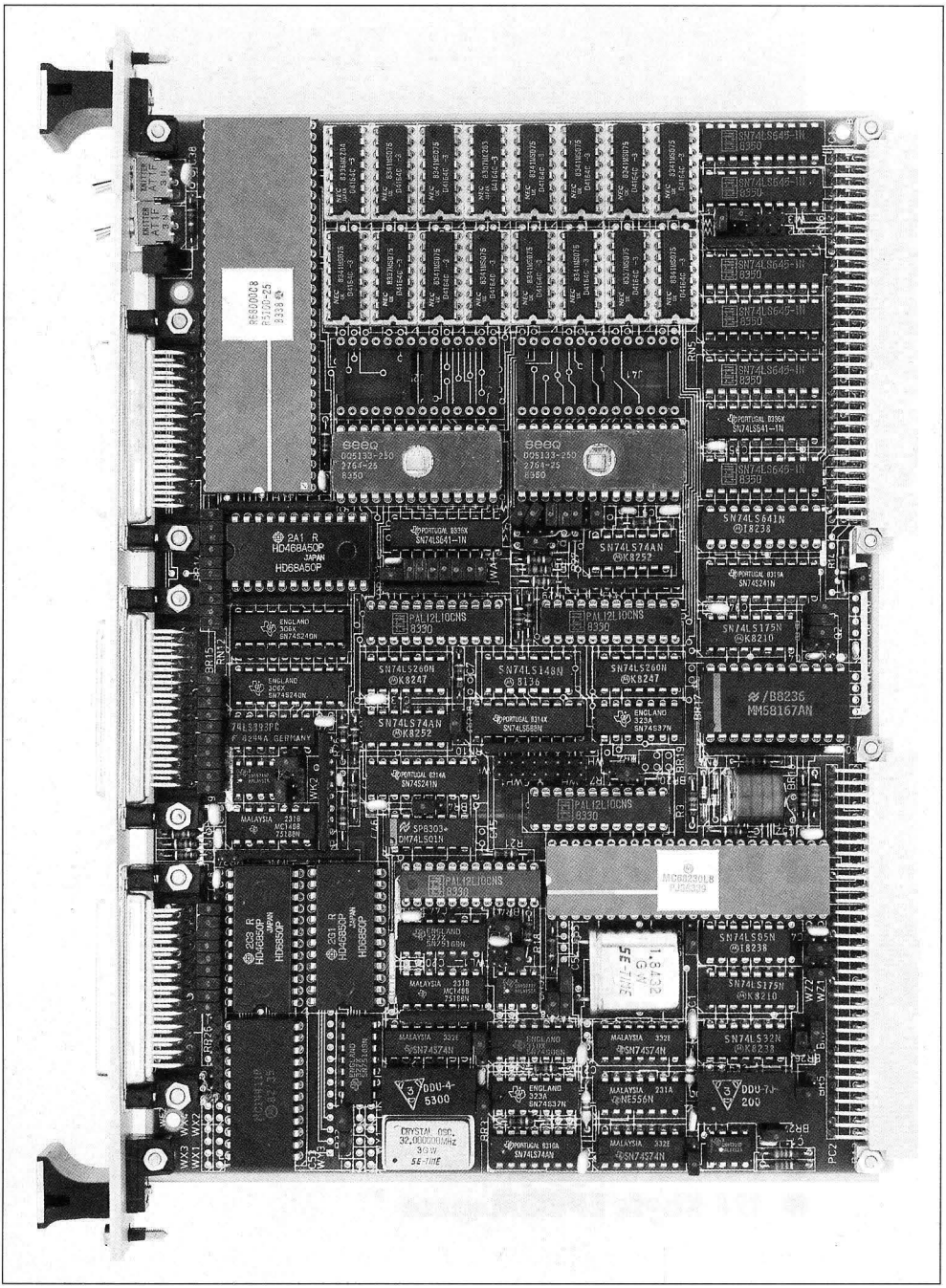
All the 16 bit CPU boards are available in system configurations which take full advantage of all their features. These configurations may be found in the systems pages towards the end of this data book.

FAMILY	CPU-1	CPU-2	CPU-2V	CPU-3V	CPU-4VC	CPU-5A	CPU-6	CPU-6V
Processor Type Frequency min. max.	68000 8 MHz 10 MHz	68000 10 MHz 10 MHz	68010 10 MHz 10 MHz	68010 10 MHz 10 MHz	68010 12.5 MHz 12.5 MHz	68000 16.7 MHz 16.7 MHz	68000 8 MHz 12.5 MHz	68010 12.5 MHz 12.5 MHz
FPCP Type Frequency	– –	– –	– –	– –	– –	68881 16.7 MHz	– –	68881 12.5 MHz
DMAC Type Frequency	– –	– –	– –	68450 10 MHz	68450 8 MHz	68450 8 MHz	– –	– –
MMU Type Frequency	– –	– –	– –	68451 10 MHz	– –	– –	– –	– –
DRAM on Board min. max.	128 Kbyte 512 Kbyte	512 Kbyte 1 Mbyte	512 Kbyte 1 Mbyte	– –	– –	– –	512 Kbyte 512 Kbyte	512 Kbyte 512 Kbyte
SRAM on Board min. max.	– –	16 Kbyte 16 Kbyte	16 Kbyte 16 Kbyte	128 Kbyte 128 Kbyte	128 Kbyte 128 Kbyte	128 Kbyte 512 Kbyte	– –	– –
Sockets for EPROMs/SRAMs	4	4	4	4	8	4	4	4
Debugger	X	X	X	X	–	–	–	–
VMEPROM	–	–	–	–	X	X	X	X
Serial Ports (RS232)	3 (ACIA)	1 (MPCC)	1 (MPCC)	1 (MPCC)	1 (MPCC)	2 (MPCC)	3 (ACIA)	3 (ACIA)
Parallel Interface	2 x 8 bit	2 x 8 bit	2 x 8 bit	–	2 x 8 bit	–	2 x 8 bit	2 x 8 bit
Timer	1 x 24 bit	1 x 24 bit	1 x 24 bit	1 x 24 bit	2 x 24 bit	1 x 24 bit	1 x 24 bit	1 x 24 bit
RTC	X	X	X	X	X	–	X	X
Floppy Disk Controller Bus Arbiter	– Single Level	X Single Level	X Single Level	– Four Level	(optional) Four Level	– Single Level	– Single Level	– Single Level
Watch Dog Timer	X	X	X	X	X	X	X	X
VMXbus Interface	–	–	–	–	–	X	–	–
Detailed Description on Page:	29	39	39	45	53	61	69	69



System 68000 VME
SYS68K/CPU-1B/D
Universal CPU-Board

- 68000 CPU
- 512 Kbyte DRAM
- 3 Serial I/O Interfaces
- Real Time Clock
- Parallel I/O Interface
- 128 Kbyte EPROM space



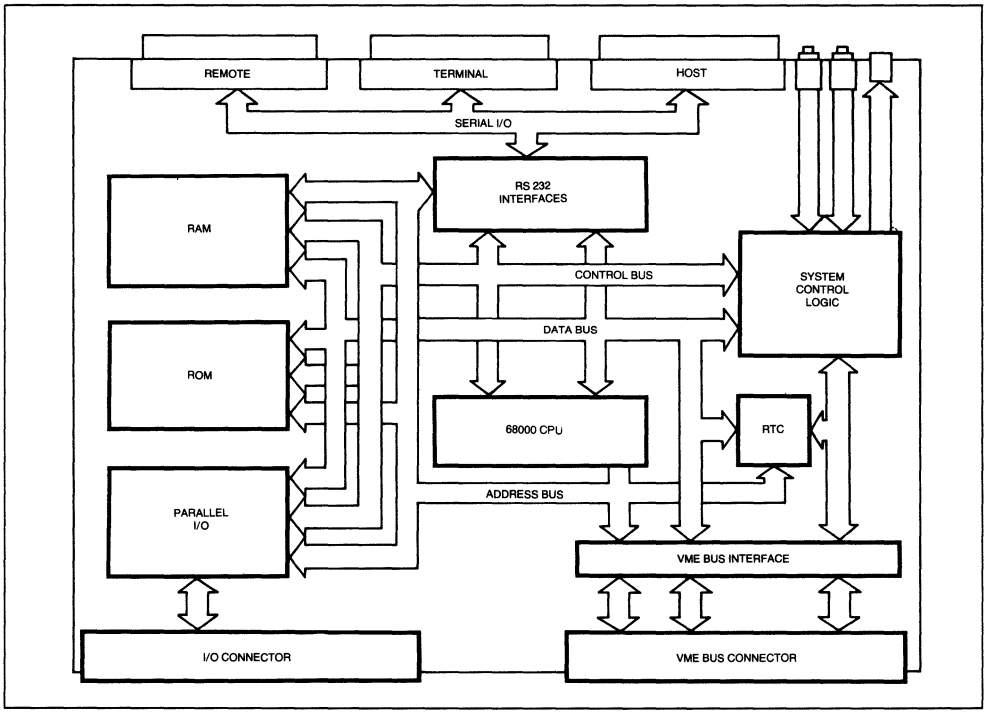
General Description SYS68K/CPU-1B

The SYS68K/CPU-1B Board is a high performance, low-cost system computer board based on the 68000 CPU and the VMEbus for high speed real time applications.
It contains 128 Kbyte of DRAM, up to 128 Kbyte of EPROM/ROM, parallel I/O, a real-time clock, 3 serial communications interfaces and the system monitor.
The implemented VMEbus interface is VMEbus Rev. B compatible and includes the slave bus arbitration as well as a single level bus arbiter.

SYS68K/CPU-1B Features

- 68000 CPU (8 MHz) on CPU-1B
- 128 Kbyte of dynamic RAM with distributed refresh every 15μsec.
- 16 Kbyte of firmware in ROM/EPROM expandable to 64 Kbyte
- 64 Kbyte of USER EPROM area or 16 Kbyte of USER SRAM area
- Memory access times
  PROM 200 – 500 ns (jumper selectable)
  DRAM 280 ns (typ.)
- Three serial communication ports with RS232 compatible interface
- Strap selectable I/O signal assignment
- Parallel I/O with 2 ports 8 bit each
- 24 bit Timer with 5 bit prescaler
- Real Time Clock with on-board battery back-up
- Auto Interrupt Vectoring for all on-board devices (6 different interrupt levels and vectors)
- Fully VMEbus compatible (Rev. B)
- 7 interrupt levels from the VMEbus
- Slave bus arbitration
- Single level bus arbiter
- RESET and ABORT function switches
- HALT mode indication LED
- Indirect connection on all connectors
- Double Eurocard form factor with front panel
- Self contained operating firmware that provides monitor, debug, one-line assembly/disassembly, and I/O control functions.
- Operating system software for different applications available.

BLOCK DIAGRAM OF THE SYS68K/CPU-1B



Features of the SYS68K/CPU-1D

- The CPU-1D contains the same features as the CPU-1B
- The dynamic memory capacity is increased to 512 Kbyte

Functional Description

Memory, real time clock, serial and parallel I/O communicate with the MPU via their common internal system bus.
Table 1. shows the global memory layout. The various functional areas of the board are described briefly in the following paragraphs.

Address	
000 000 000 007	Initialisation vectors from system EPROM
000 008 01F FFF	Dynamic RAM on CPU-1B
000 008 07F FFF	Dynamic RAM on CPU-1D
080 008 09F FFF	SYSTEM EPROM Area
0A0 000 0BF FFF	USER EPROM Area
0E0 000 0FF FFF	I/O Interfaces
100 000 FEF FFF	VMEbus addresses (A24)
FF0 000 FFF FFF	VMEbus Short I/O (A16)

1. 68000 CPU (8 or 10 MHz)

The 68000 CPU has a 16-bit data bus and a 23-bit address bus. The address bus provides a direct memory addressing range of 16 Mbytes. The processor has eight 32-bit data registers, seven 32-bit address registers, two 32-bit stack-pointers, a 32-bit program counter, and a 16-bit status register. Seven interrupt levels allow an auto- and a non-auto-interrupt vector mode (192 vectors). The 68000 Data Sheet and the User's Manual describe the device in detail.

2. The Dynamic RAM

The local addresses space consists of 128 Kbyte with a typical access time of 280 ns. With the use of 256K x 1 oriented DRAM's the memory capacity is increased to 512 Kbyte (on CPU-1D).

For critical real time applications the distributed »RAS only« refresh can delay every 15 micro sec a pending access for a maximum of 290 ns. The refresh works totally asynchronous to the CPU. Therefore, no time delay is required if the CPU accesses other memory areas.

3. The SYSTEM Area

The SYSTEM area contains two sockets (28 pins) with a JEDEC compatible pin-out. This allows the use of different ROM's and EPROM's with a maximum capacity of 64 Kbyte. The access time of the SYSTEM area and of the USER area is jumper selectable from 150 to 500 ns.
Table 2. shows the list of usable devices.
The SYS68K DEBUGGER firmware package resides in two 2764 EPROM's (included in the shipment).

Table 2		EPROM
2K x 16	4 Kbyte	2716
4K x 16	8 Kbyte	2732
8K x 16	16 Kbyte	2764
16K x 16	32 Kbyte	27128
32K x 16	64 Kbyte	27256

4. The USER Area

The USER area contains two 28 pin sockets with JEDEC compatible pin out. To allow the usage of static RAM's, the access to the USER area is byte oriented.
Table 3. lists the usable device types.

Table 3		EPROM	SRAM
2K x 16	4 Kbyte	2716	6116
4K x 16	8 Kbyte	2732	–
8K x 16	16 Kbyte	2764	6264
16K x 16	32 Kbyte	27128	–
32K x 16	64 Kbyte	27256	–

5. Serial Communication Ports

Three asynchronous serial communication ports, designated Port 1 for the terminal, Port 2 for the host, and Port 3 for user applications, are provided on the board. All of these ports are RS232C compatible (E.I.A. standard). The terminal acts as a user interface and works in conjunction with the monitor. Port 2 interfaces to a modem or directly to a host computer. The host computer may be used to provide more powerful software capabilities, such as program assembly and downloading of programs. Also an operational transparent mode condition is callable via the system monitor. This transparent mode effectively bypasses the board and

allows the terminal to communicate directly with the host. The third serial communication port interfaces either to a printer or acts as a remote link to another computer. All serial ports are jumper selectable for various data transmission rates (110-9600 or 600-19200 baud).
For each serial port the I/O signals can be assigned to one of the 25 pins of the D-sub female connector on the front panel.

6. Parallel I/O
The board contains a Parallel Interface and Timer chip PI/T 68230 with a clock frequency of 8 MHz.
The PI/T operates in uni- or bi-directional mode either 8 or 16 bits wide.
Each of the 24 I/O lines may be configured as an input or as an output.
For asynchronous software control the third 8 bit port can be configured to drive two interrupts on level 5, one for the handshake interface and one as a timer output.

7. Programmable Timer
The PI/T 68230 (Parallel Interface and Timer) includes a 24-bit programmable timer. The timer is a synchronous counter to be used for generating or measuring time delays and various frequencies. The timer is either clocked by a 5-bit prescaler or directly, and the clock source can either be the 8 MHz CPU clock or an external clock.

8. Programmable Real Time Clock
The on-board Real Time Clock (RTC) allows various applications, such as time scheduling, time comparison, time-out counter, etc. Additionally, the real time clock may act as an actual time base providing month, day of month and day of week. An on-board battery ensures time base operation during power down times.

9. On-Board Interrupt Handling
All on-board devices are able to force interrupts on different levels to the CPU. In this case the auto-interrupt vector of the 68000 will be forced and each device has its own interrupt vector.
Table 4. shows the interrupt structure of the CPU-1B/D.

Description	Device	Level	Vector No.
ABORT	Switch	7	31
Real Time Clock	58167A	6	30
Parallel Interface and Timer Chip	68230	5	29
Terminal ACIA	6850	4	28
Remote ACIA	6850	3	27
Host ACIA	6850	2	26

10. The VMEbus
The implemented VMEbus Interface includes 24 address, 16 data, 6 address modifier and the asynchronous control signals.
A single level bus arbiter is provided to build multi master systems. In addition to the bus arbiter, a separate slave bus arbitration allows selection of the arbitration level (0-3).
The address modifier range »Short I/O Access« can be selected via a jumper for variable system generation.
The 7 interrupt request levels of the VMEbus are fully supported from the SYS68K/CPU-1B/D. For multi-processing, each IRQ signal can be enabled/disabled via a jumper field.
Additionally, the SYS68K/CPU-1B/D supports the ACFAIL, SYSRESET, SYSFAIL and SYSCLK signal (16 MHz).

11. The DEBUGGER Firmware
The SYS68K/CPU-1 series of boards operate under control of the DEBUGGER firmware. This 32 Kbyte software package provides an easy interface to the SYS68K family hardware and offers excellent functionality. The DEBUGGER is a system monitor which controls communication with the terminal and exercises other elements of the system. It provides debug capability, one-line assembly/disassembly, and I/O control.
For program development and debug, a dynamic line-by-line editor/assembler function is used. Each instruction is translated into the proper opcode and stored in the memory.
In order to display an instruction, the firmware disassembles the opcode and displays the instruction mnemonic and operands.
Data and programs can be uploaded and downloaded via a serial port (HOST INTERFACE).

The DEBUGGER has the following features:

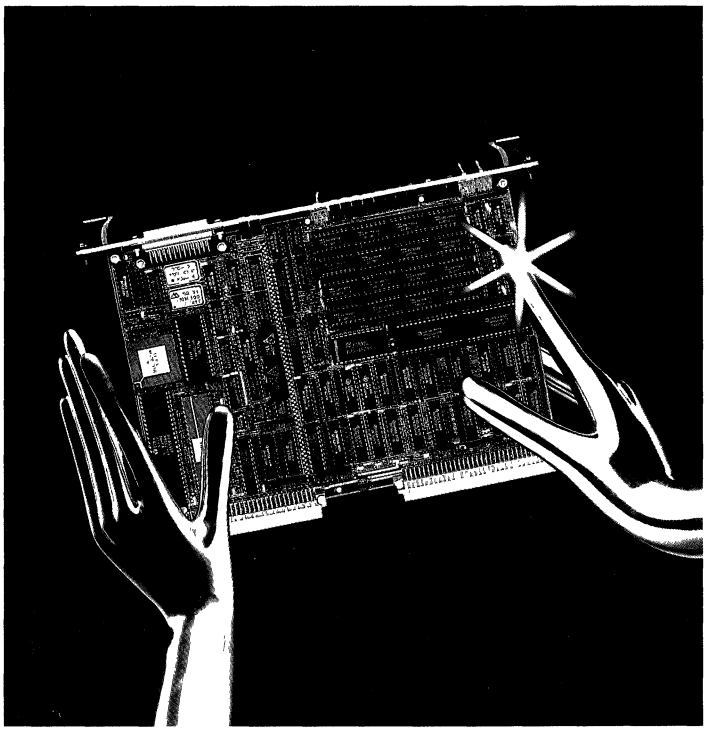
COMMAND SUMMARY	DESCRIPTION
BF <address1> <address2> <data> <CR>	Block Fill memory – from addr1 through addr2 with data
BM <address1> <address2> <address 3> <CR>	Block Move – move from addr1 through addr2 to addr3
BR [<address> [; <count>]...] <CR>	Set/display Breakpoint
BS <address1> <address2> <data> <CR>	Block Search – search addr1 through addr2 for data
BT <address1> <address2> <CR>	Block Test of memory
DC <expression> <CR>	Data Conversion
DF <CR>	Display Formatted registers
DU [n] <address1> <address2> [<string>] <CR>	Dump memory to object file
GO [<address>] <CR>	Execute program
GD [<address>] <CR>	Go direct
GT <address> <CR>	Exec prog: temporary breakpoint
HE <CR>	Help; display monitor commands
LO [n] [;<options>] <CR>	Load Object file
MD <address> [<count>] <CR>	Memory Display
MM <address> [<data>] [;<options>] <CR>	Memory Modify
MS <address> <data1> <data2> <... <CR>	Memory Set – starting at addr with data 1, data 2,..
NOBR [<address> ...] <CR>	Remove Breakpoint
NOPA <CR>	Printer Detach
OF <CR>	Offset
PA <CR>	Printer Attach
PF [n] <CR>	Set/display Port Format
RM <CR>	Register Modify
TM [<exit character>] <CR>	Transparent Mode
TR [<count>] <CR>	Trace
TT <address> <CR>	Trace: temporary breakpoint
VE [n] [<string>] <CR>	Verify memory/object file
.AO – .A7 [<expression>] <CR>	Display/set address register
.DO – .D7 [<expression>] <CR>	Display/set data register
.RO – .R6 [<expression>] <CR>	Display/set offset register
.PC [<expression>] <CR>	Display/set program counter
.SR [<expression>] <CR>	Display/set status register
.SS [<expression>] <CR>	Display/set supervisor stack
.US [<expression>] <CR>	Display/set user stack
MD <address> [<count>];DI <CR>	Disassemble memory location
MM <address>;DI <CR>	Disassemble/Assemble memory location

Specification of the SYS68K/CPU-1B/D

Microprocessor	68000 (8 MHz on CPU-1B and 10 MHz on CPU-1D
Parallel I/O	68230 PI/T, 16 data lines and 8 control lines configurable as a Centronics parallel interface
Serial I/O	3 RS232C interfaces, strap selectable baud rate from 110-9600 or 600-19200 baud
Timer	One 24-bit timer with a 5-bit prescaler,
Real Time Clock	Programmable real time clock with on-board battery back-up
Memory	128 Kbyte of RAM,on CPU-1B, 512 Kbyte of RAM on CPU-1D 64 Kbyte of SYSTEM area, 64 Kbyte of USER area.
Firmware	32 Kbyte of monitor called DEBUGGER including a one-line assembler/disassembler
Power Requirements	+5V/2.8A, +12V/200mA -12V/200mA
Operating Temp.	0 to +60 degrees C
Storage Temp.	-50 to +85 degrees C
Relative Humidity	0-95% (non-condensing)
Board Dimensions	Double Eurocard 234 x 160 mm (9.2 x 6.3")

Ordering Information:

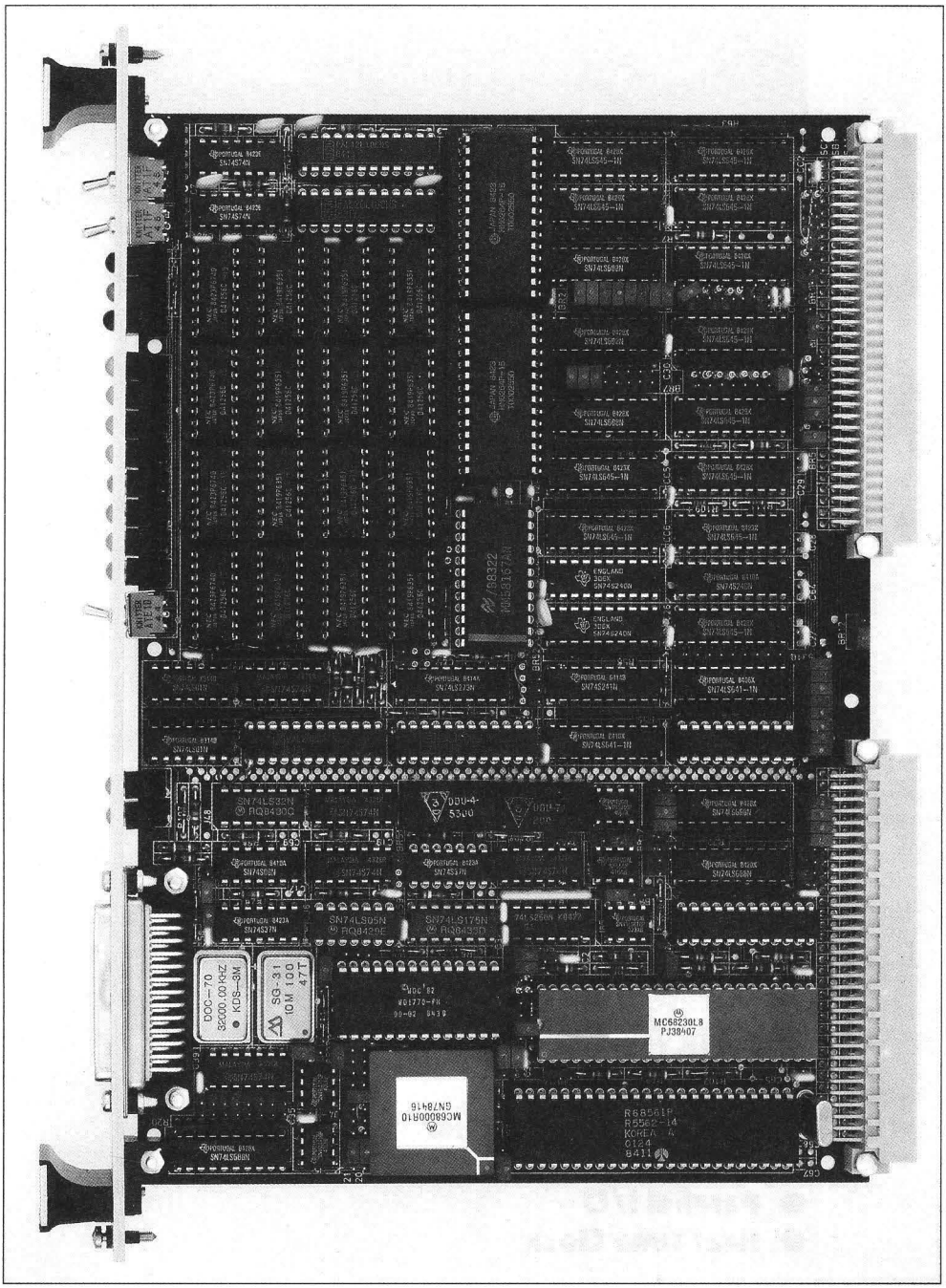
SYS68K/CPU-1B Part No. 100100	68000 CPU Board including User's Manual (8MHz clock frequency/128 Kbyte RAM)
SYS68K/CPU-1D Part No. 100102	68000 CPU Board including User's Manual (10MHz clock frequency/512 Kbyte RAM)
SYS68K/CPU-1B/UM Part No. 800100	User's Manual for all CPU-1 Products



System 68000 VME
SYS68K/CPU-2

High Performance CPU-Board with Dual Ported RAM

- Up to 1 Mbyte of DPR
- 10 MHz CPU Clock
- Floppy Disk Controller
- RS232 Interface
- Parallel I/O
- Real Time Clock


DOC—70
32000.00 KHz
KDS—8M
SG-31
10M 100
47T
MC68230L8
PJ3840?
MC68000FN10
6N7041G
R6856P
R5562-14
KOREA
0124
8411

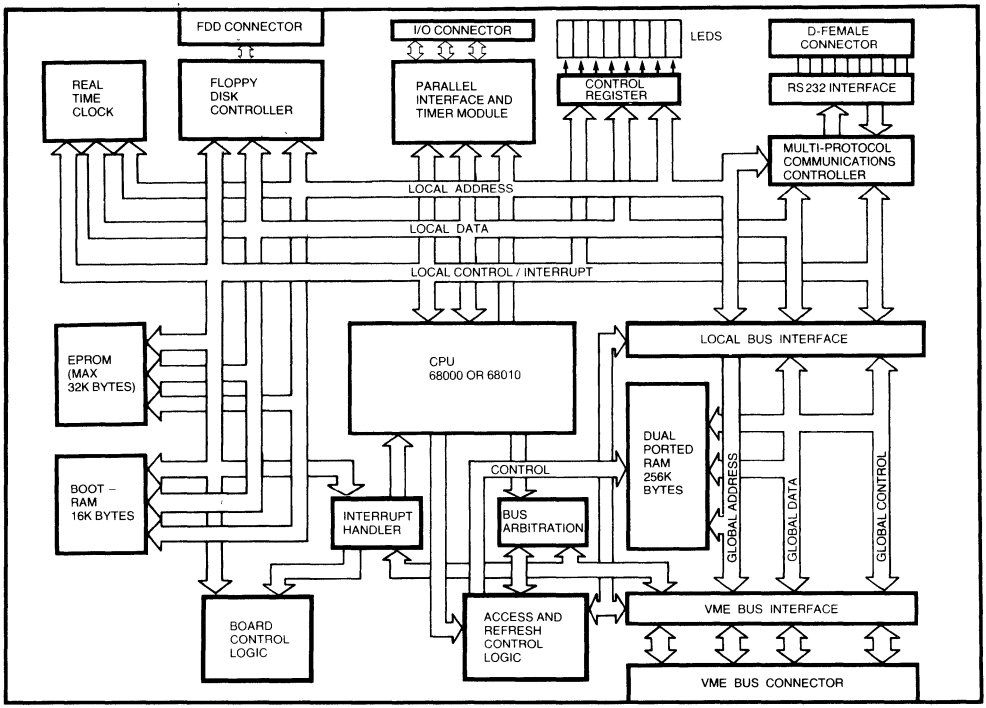
General Description CPU-2

The SYS68K/CPU-2 board can be used as a single board computer, as well as in high performance multi-processor environments.
The CPU-2 board is available with a 68010 CPU (10 MHz), which is software compatible to the standard 68000, and offers additional features, such as virtual memory management and enhanced error exception handling.
The CPU-2 offers either 512 Kbyte or 1 Mbyte of dual ported dynamic memory. The parallel interface and timer device 68230 contains 24 bidirectional I/O lines and a 24 bit timer. For real time applications the Real Time Clock 58167A with date and time of day is used.
In addition, the Floppy Disk Controller WD 1770 can control up to four different Floppy Drives with a Shugart compatible interface.

Features of the SYS68K/CPU-2

- Processor 68000 (68010 optional) with 10 MHz clock frequency
- Dual Ported Memory with 512 Kbyte and 1 Mbyte versions
- Parallel Interface with 24 bidirectional I/O lines
- 24 bit Timer with 5 bit prescaler
- Real Time Clock with date and time of day
- 8 bit output register with 8 control/indicator LEDs on the front panel
- Floppy Disk Controller for up to 4 Floppy Disk Drives (Shugart compatible interface)
- All I/O interface devices are able to force interrupts

BLOCK DIAGRAM OF THE SYS68K/CPU-2



Functional Description
The EPROM array and the I/O devices communicate with the CPU via their 23 bit address bus and 16 bit data bus. The functional areas are briefly described in the following paragraphs.

68000 CPU
The CPU packed in a Pin Grid Array with 68 pins contains eight 32 bit data registers, seven 32 bit address registers, two 32 bit stack pointers, a 32 bit program counter, and a 16 bit status register. The processor is able to react on 7 different interrupts from the local and from the VMEbus. Processor clock frequency is 10 MHz.

Virtual Processor 68010
The 68010 CPU is a virtual machine, software compatible to the standard 68000. Error exception handling is optimized. On occurrence of an error the program counter and the access address are stored on the stack for easy handling and diagnostics. Therefore the system software is able to correct even catastrophic failures, thus preventing system crashes. The processor clock frequency is 10 MHz.

EPROM Area
The SYS68K/CPU-2 contains two 28 pin sockets for JEDEC compatible EPROM's. The base address of the EPROM area is selectable and easy to change via plug-in jumpers. Maximum EPROM space is 32 Kbyte when using 27128 devices.

RS232 Interface
The board contains a RS232 compatible interface to transfer information to/from other Data Communication Equipment (DCE). The interface chip used is a Multi-Protocol Communications Controller (MPCC) 68561. This device allows the use of all standard byte or bit oriented protocols in synchronous, or asynchronous modes.
The following protocols may be selected:
- Binary Synchronus Communications (BSC)
  IBM ASCII and IBM EBCDIC
- Character Oriented Protocols (COP)
  BSC, DDCMP, X3.28, X.21, ECMA-16
- Bit Oriented Protocols (BOP)
  SDLC, HDLC/ADCCP, X.25

The internal clock for the modem handshake interface is software programmable from 50 to 38400 baud.
The MPCC is able to force an interrupt in a fully asynchronous software handling mode. (Three different software programmable interrupt vectors are available.)
A wire wrap configuration area allows various signal assignments to the 25 pin D-sub-connector on the front panel. The base address of the MPCC is jumper selectable for easy system configuration.

Dual Ported RAM (DPR)
The on-board CPU communicates with the dynamic RAM storage area via a special bus system. Transfers to/from the DRAM area are controlled by special arbitration logic. The base address and the address modifier code of the DPR is jumper selectable to be at any global address in the system environment.
The DPR storage array is accessible from the VMEbus and also from the on board CPU under the same access address and the same address modifier code. A special mode can be selected so that the DPR array works only as local memory (not accessible from the VMEbus).
Storage capacity is 512 Kbyte or 1 Mbyte of DRAM with access times of 340ns on a READ and WRITE with no access from the 2nd bus.
The on-board auto refresh for the DRAM's forces a maximum delay of 290ns and works transparent to other accesses.

Parallel I/O (PI/T)
The board contains a special I/O interface (PI/T 68230) with 24 bidirectional I/O lines which are accessible via the second 96 pin male connector. A special jumper can enable the 24 bit timer to drive an interrupt to the local bus. Clock frequency of the PI/T is 8 MHz to provide high data throughputs for critical real time applications.

Real Time Clock (RTC)
The on-board RTC includes a calendar indicating month, day of the month, day of the week, hours, minutes, seconds, 1/100 seconds and 1/1000 seconds.
An interrupt control register enables or disables the interrupt output of the RTC. A special jumper enables the interrupt signal to the local interrupt bus. The RTC can be connected to the +5V standby power line of the VMEbus or to a special line of the I/O connector. Therefore all the data patterns are stored during power failures or in power down mode.

Control Register (CR)
The board contains an 8 bit buffered latch which is used to define the Floppy Disk Drive to be enabled and serves as a general purpose output port.
The levels of the output lines are indicated by 8 LED's on the front panel. These LED's may be used as status and test indicators.

Floppy Disk Controller / Formatter (FDC)
The on-board FDC with its fully buffered output (48mA sink) contains an SA450 compatible interface for direct connection to Floppy Disk Drives. With the specially buffered output the drive (1–4) can be selected and controlled. The on-board controller WD1770 is able to control double and single sided drives in both double and single density modes.

For asynchronous handling, the FDC can force an interrupt to the local bus.
The interface lines are accessible via the I/O connector (flat cable 1:1 to the Floppy Drive Edge Connector).

Control Logic
On the board there are three switches for control. The RESET button resets the CPU and all I/O devices. Pushing the ABORT button generates an interrupt on level 7. The RUN/HALT switch sets the CPU into HALT mode and is indicated with a red LED, otherwise the green RUN LED is lit when the CPU is in RUN mode.
For easy indication that the board is the current VMEbus master, a BUS MASTER LED indicator is provided on the front panel.
To abort invalid address accesses, a time-out counter is provided on the board. It generates a time-out from 8μs up to 2 ms (jumper selectable).

VMEbus Interface
The SYS68K/CPU-2 board is completely VMEbus compatible and drives/receives the address modifier (AM) signals. A special address modifier encoder is used to provide the short supervisor I/O access and the short non privileged I/O access (AM4 active).
The bus control signals Address Strobe (AS), Data Strobe 0,1 (DS0, DS1), and Write (WR) have drive capability of 64 mA in accordance to the VMEbus specification.
Each interrupt signal of the VMEbus can be enabled or disabled on the board so that in a multiprocessor environment several interrupt signals may be reserved for each CPU board individually.
The on-board interrupt sources are handled individually offering transparent handling and self test capabilities.
For multi-master environments the board contains full slave bus arbitration on one of the four selectable daisy chain levels.
The board works completely asynchronous to the VMEbus and the bus master state so that on-board transfers to/from the I/O from the EPROM area and to/from the Dual Ported RAM can be initiated if another VMEbus board is the current bus master.
To provide full address decoding, all addresses which are not on-board (DPR, EPROM, I/O) are decoded as off-board addresses. This allows configuration of contiguous memory space of RAM on a selected address range by means of an additional RAM board.

Features of the resident DEBUGGER package:
- EPROM resident system monitor/debugger
- More than 30 commands for debug, up/down-line load
- One-line assembler/disassembler for assembly language program development
- Full speed execution of system and user programs operating in the VMEbus oriented monoboard microcomputer system
- Terminal capability for up/downline load from another development system or any host computer
- Powerful software and system debug command set allowing access to all VME modules plus the full 16 Mbyte direct address range of the VME system bus
- Includes all required installation and operation documentation
- Access to monitor resources via vectorized entries and the TRAP 14 calling sequence
- Start of a user application program or optional software by command

The CPU-2 DEBUGGER is an EPROM based resident package ready for immediate use with the VME monoboard CPU-2.
It provides a powerful evaluation and system debugging tool for VME based CPU systems. The EPROM resident package operates in 32 Kbyte of ROM space. CPU-2 DEBUGGER uses the first 1024 words of RAM storage for interrupt vectors and temporary storage. The EPROM resident package is delivered in two EPROM's.
The package permits full speed execution of system and user developed programs operated in a VME based CPU system environment under complete operator control.
Access to monitor resources and configuration control is given by vectorized system entries and a TRAP 14 calling sequence. The DEBUGGER may be utilized with the VME based CPU monoboard microcomputer SYS68K/CPU-2 in a standalone environment with only a user provided standard asynchronous ASCII terminal.

Assembler/Disassembler Capability
The on-board assembler does not allow line numbers and labels; however, it is a powerful tool for creating, modifying, and debugging 68000 code. The on-board assembler processes each line of a program as an individual unit.
- In order to read back a program after it has been entered, the machine code is disassembled and then displayed as mnemonic and operands.
- The one-line assembler shows a question mark (?) under the portion of the source statement where an error probably occurred, or displays a short error message.
- One directive (DC.W) is accepted.

The symbolic language used to code source programs for processing by the assembler is called 68000 assembly language. This language is a collection of mnemonics representing:

- Operations
  - 68000/68010 machine instruction operation codes
  - Directive (pseudo-op)
- Operators
- Special symbols

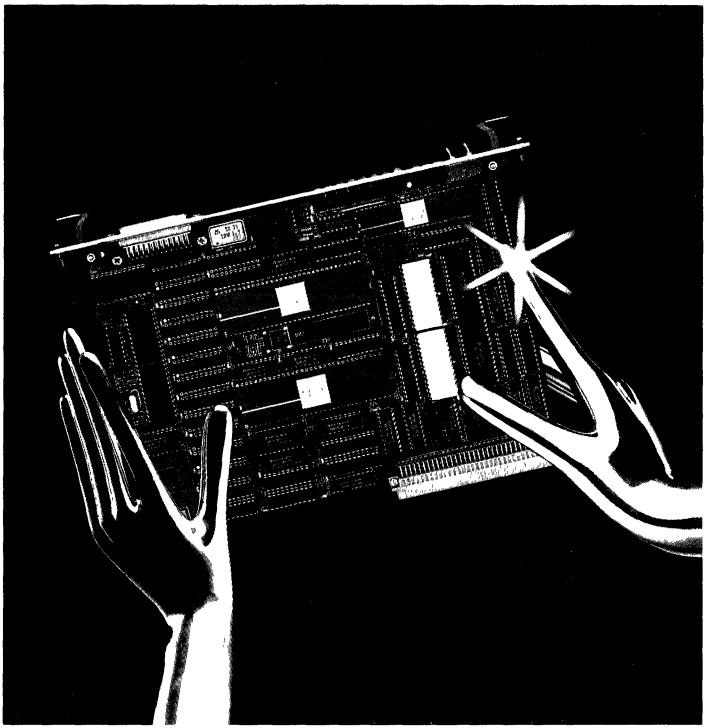
A source program is a sequence of source statements arranged in a logical way to perform a predetermined task. Each source statement occupies a line and must be either an executable instruction or a DC.W assembler directive. Each source statement follows a consistent source line format.

Specification

	CPU-2
Microprocessor	68000/10 MHz 68010/10 MHz (virtual processor)
JEDEC Sockets	2 EPROM sockets for 2764 or 27128 devices (8K x 8 or 16K x 8) 2 Static RAM's 6264 (16 Kbyte)
I/O	Multi-Protocol Communications Controller with RS232 compatible interface Parallel Interface (68230) with 24 bidirectional I/O lines and a 24 bit timer Real Time Clock Floppy Disk Controller WD1770 with Shugart compatible interface Status is signaled by 8 LED's on the front panel
Dual Ported RAM	256 Kbyte of DPR 340ns (typ) write 340ns (typ) read 512 Kbyte of DPR optional 1 Mbyte of DPR optional
Bus Interface	VMEbus Interface implemented A16 : D8, D16 and A24 : D8, D16 mode Slave bus arbitration Release on request Release after Time-out One Level Bus Arbiter Full interrupt handling
Included Firmware	DEBUGGER firmware with line by line assembler/disassembler
Power Requirements	+5V/3.2A (max) +12V/200mA (max) −12V/200mA (max)
Operating Temperature	0 to + 50 degrees C
Storage Temperature	−50 to + 85 degrees C
Relative Humidity	0−95% (non condensing)
Board Dimensions	Double Eurocard 234 x 160 mm (9.2 x 6.3 inch)

Ordering Information:

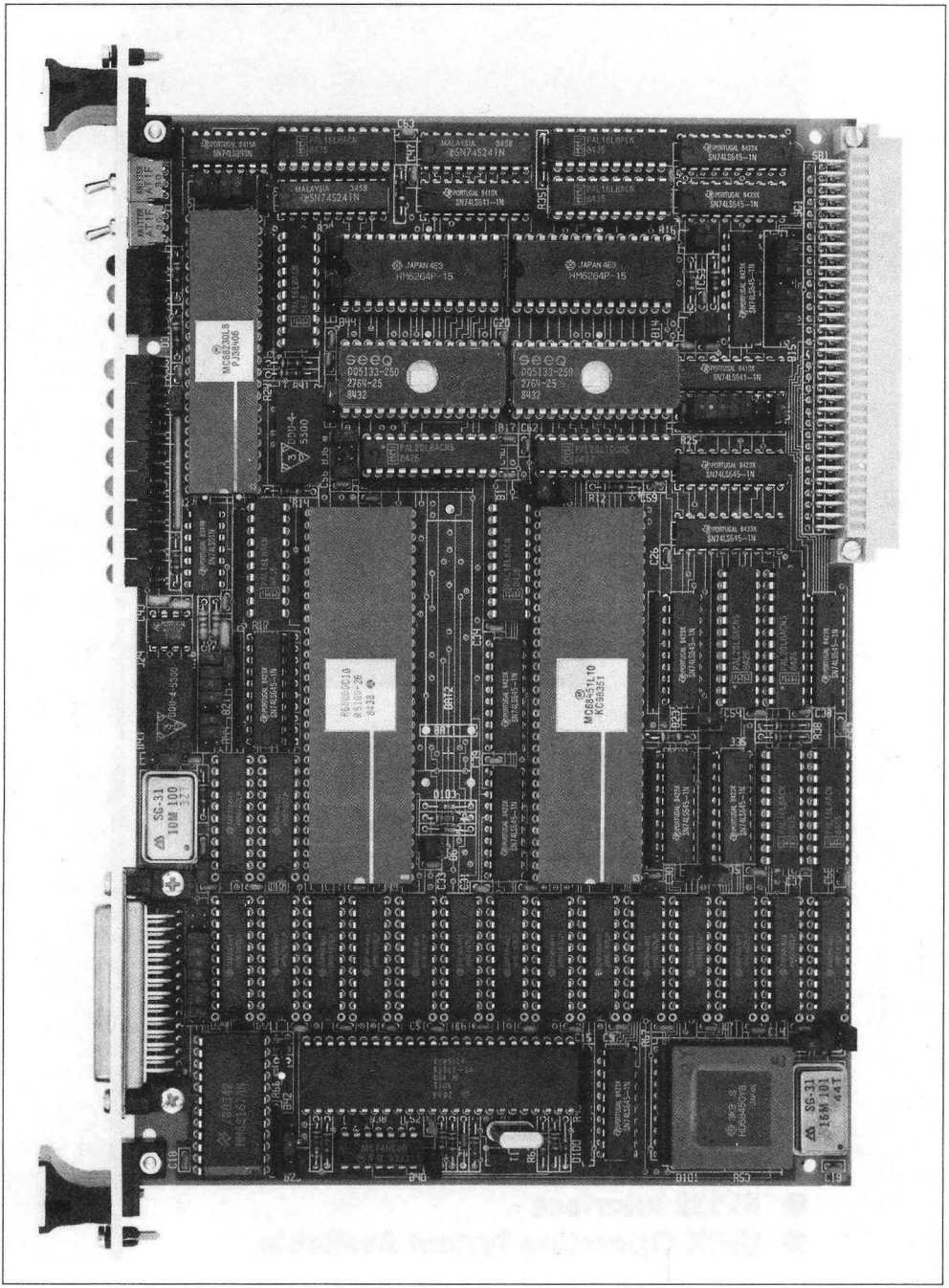
SYS68K/CPU-2B Part No. 100202	68000, 10 MHz, 512 Kbyte DPR, including User's Manual
SYS68K/CPU-2F Part No. 100205	68000, 10 MHz, 1 Mbyte DPR, including User's Manual
SYS68K/CPU-2VB Part No. 100212	68010, 10 MHz, 512 Kbyte DPR, including User's Manual
SYS68K/CPU-2VC Part No. 100213	68010, 10 MHz, 1 Mbyte DPR, including User's Manual
SYS68K/CPU-2/UM Part No. 800136	User's Manual for all CPU-2 Board versions



System 68000 VME
SYS68K/CPU-3VB

CPU Board
with Memory Management

- 68010 with 10 MHz Clock
- 68451 MMU with 10 MHz Clock
- 68450 DMAC with 10 MHz Clock
- 128 Kbyte No Wait State SRAM
- RS232 Interface
- UNIX Operating System Available



General Description SYS68K/CPU-3VB
The SYS68K/CPU-3VB board is a high performance multi-processor computer board built around the virtual 68010 CPU and the VMEbus.
It contains a Memory Management Unit, Direct Memory Access Controller, 128 Kbyte SRAM, 128 Kbyte EPROM and powerful control functions. The implemented VMEbus interface is fully VMEbus-compatible and includes a slave bus arbitration as well as a four level prioritized arbiter.

SYS68K/CPU-3VB Features
- 68010, 10 MHz
- 68450 Direct Memory Access Controller with 10 MHz
- 68451 Memory Management Unit with 10 MHz
- 68561 Multi-Protocol Communications Controller with an RS232-compatible interface
- 68230 Parallel Interface and Timer Module for local control
- 58167 Real Time Clock with battery back-up
- 128 Kbyte high-speed static RAM
- 4 EPROM sockets for system and/or User programs (max 128 Kbyte)
- All on-board devices are able to interrupt the onboard CPU (vector or auto-vector)
- 4 level Bus Arbiter (prioritized)
- Slave bus arbitration on a jumper selectable level (0-3)
- RESET and ABORT function switches
- 8 status LEDs
- Self-contained operating firmware providing monitor, debug, on-line assembly/disassembly and I/O control functions
- UNIX Operating system available

Functional Description
The DMA Controller, Multi-Protocol Communication Controller and the Memory Management communicate with the CPU via the unbuffered physical address and data bus. The EPROM areas, static RAM, Real Time Clock, Parallel Interface and Timer Module as well as the VMEbus interface communicate with the CPU via the buffered physical address and data bus.

BLOCK DIAGRAM OF THE SYS68K/CPU-3VB

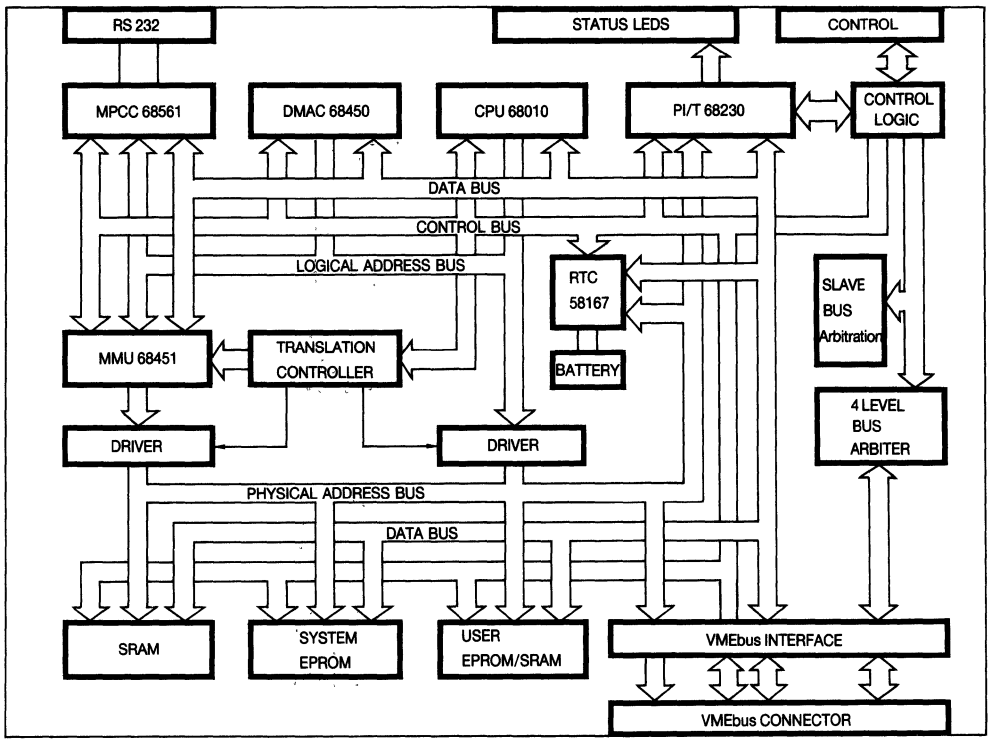


Table 1 – CPU-3VB Memory Layout

Address	Description
000000 to 000007	Start Vectors from System EPROM
000008 to 01FFFF	Static RAM (128 Kbyte)
008000 or 020000 to EFFFFF	VMEbus Addresses
F00000 to F3FFFF	SYSTEM and USER EPROM Area
F40000 to F4FFFF	LOCAL I/O Devices
FF0000 to FFFFFF	Short I/O VMEbus Addresses

1. 68010 Central Processing Unit
The high performance 68010 CPU with its upgraded 68000 instruction set and virtual memory support offers a total of 16 Mbyte of addressable memory through its 23 address signals. The fully asynchronous 16 bit data bus allows high speed data transfers to/from the on-board or VMEbus memory and I/O areas.
The SYS68K/CPU-3VB uses an 10 MHz 68010 processor. To provide fault tolerant systems, the CPU provides excellent exception handling if an error or interrupt occurs. The status and all addresses, as well as the fault address are stored on the stack to provide diagnostic and correction as well as rerun functions.

2. 68450 Direct Memory Access Controller
A high-speed DMA Controller is used on the board to move data to and from the VMEbus. Its four channels can be used from the operating system and/or shared with user programs.
The DMAC has a maximum data transfer speed of 4 Mbyte per second. Time-critical programs can be loaded into the local RAM via the DMAC, giving number cruncher applications no time overhead through the VMEbus. This also results in a lower VMEbus load.

3. 68451 Memory Management Unit (10 MHz)
The powerful 68451 MMU is used on the SYS68K/CPU-3VB to provide memory allocation, paging and segmentation, as well as write protection of allocated memory areas.
When special bits are programmed through the Parallel Interface and Timer Module, the logical address of the CPU and the DMAC can be translated through the MMU into the physical address where the memory, I/O devices, and the VMEbus are connected. If these bits are not activated, no MMU translation is performed and the access speed is faster (default condition).
The two PI/T signals define whether an MMU operation has been initiated or not. The detailed diagram of the physical and logical address bus is shown in Figure 1.
The MMU can be enabled and disabled for each device seperately (CPU and DMAC). This offers maximum flexibility for operating systems and application programs. Table 2 shows how much time overhead must be added if an MMU operation is enabled.

Table 2 – Address Translation Times

	MMU Translation	No MMU Translation
CPU	235ns	15ns
DMAC	235ns	15ns

4. The Static RAM
The SYS68K/CPU-3VB contains 128 Kbyte of static RAM. The access time of the static RAM is 70ns for both reads and writes.
This allows the CPU to run with only wait state trough the MMU.

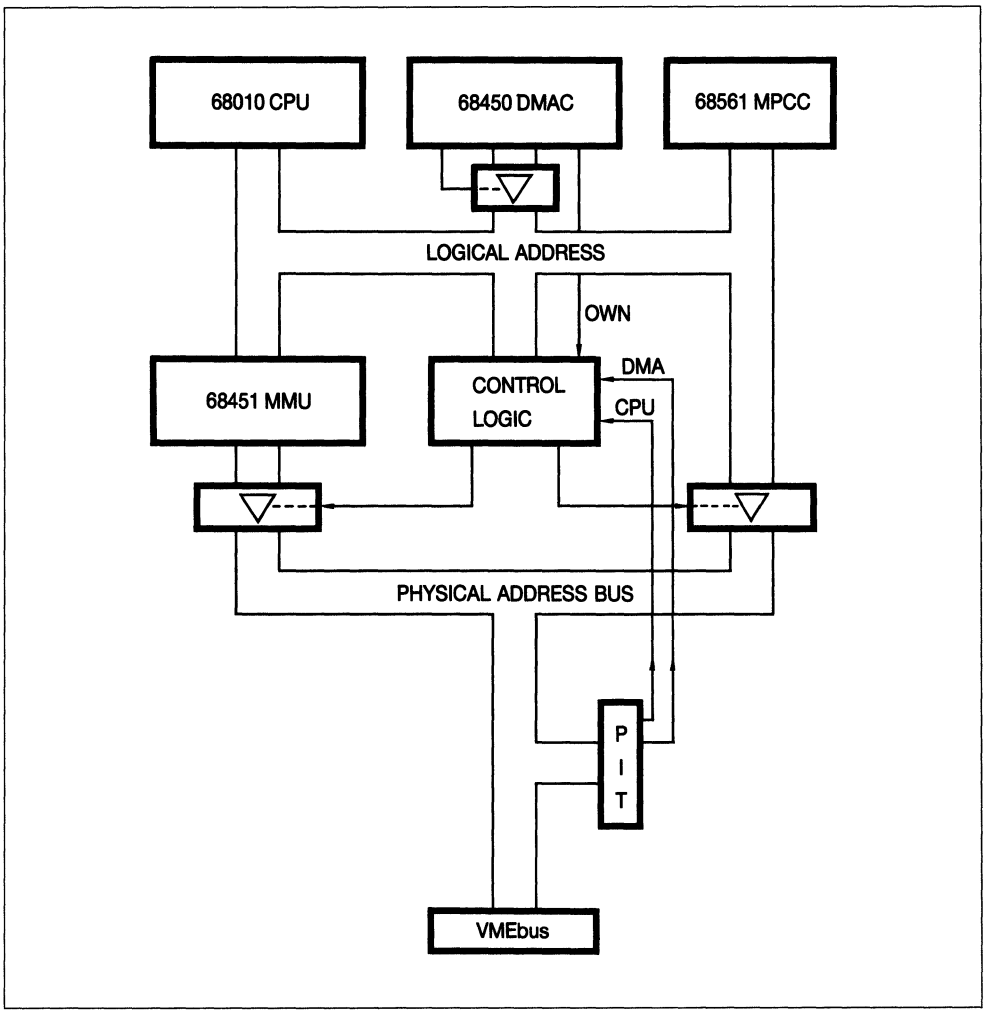
5. The SYSTEM and USER Area
The SYSTEM area consists of two sockets for JEDEC-compatible EPROM devices. The SYS68K/CPU-3VB DEBUGGER firmware resides with its boot-up and I/O control functions in two devices (included in the shipment).
The USER area is provided for the use of EPROMs or SRAMs (JEDEC compatible pin-out).

Table 3 – lists the usable device type for each area.

Device	Type	Organisation	User Area	System Area	Total Capacity
2764	EPROM	8K x 8	X	X	32 Kbyte
27128	EPROM	16K x 8	X	X	64 Kbyte
27256	EPROM	32K x 8	X	X	128 Kbyte
6264	SRAM	8K x 8	X		16 Kbyte

The access times for the SYSTEM and for the USER areas are jumper-selectable from 100ns to 400ns.

Figure 1 – The CPU-3VB Address Translation Handling



6. 68561 Multi-Protocol Communication Controller

The MPCC contains different protocols to communicate via the RS232-compatible interface to a user-supplied serial communication device.

Protocols: IBM binary synchronous (ASCII or EBCDIC)
Character oriented protocols (BSC, DDCMP, X3.28, X.21, ECMA16)
Synchronous Bit oriented protocols (SDLC, HDLC, ADCCP, X.25)

A software-programmable baud rate from 110 to 38400 baud and a local loop-back mode provide maximum flexibility.
The I/O signal assignment of the 4 input and 4 output signals to the 25 pin D-Sub connector on the front panel is jumper selectable.
The MPCC is able to force an interrupt to the CPU.

7. 68230 Parallel Interface and Timer Module

The PI/T with its 8 MHz clock frequency allows an optical status display through the eight yellow status LEDs on the front panel.
Interrupts are controlled through the 2nd port.
Each interrupt request level can be enabled or disabled through a CPU command. The exception signals ACFAIL and SYSFAIL are monitored through the 3rd port. Additionally, both the MMU translation for the CPU and the DMAC and the bus release functions are software programmable through this port.
The PI/T I/O ports are used for local control only and include a 24-bit programmable timer. This timer may be used for generating or measuring time delays, or as a watchdog timer. The PI/T timer interrupt request signal is used to force an interrupt to the CPU.

8. 58167 Programmable Real Time Clock

The on-board RTC allows various applications such as time scheduling, time comparison, time-out counter etc.
Additionally, the RTC may act as an actual time base independent from the main power, providing month, day of month, and day of week. An on-board battery ensures time base operation during power-down.

9. On-Board Exception Handling

The board contains two switches – a RESET and an ABORT switch. During an activated RESET, all on-board devices along with the CPU are reset.
Additionally, the reset can be forced to the VMEbus if this card is used as the master controller (slot 1 function).
During a pushed ABORT switch, an interrupt is forced on level 7 (non-maskable).
The 16 MHz SYSCLK signal can be forced to the VMEbus if the jumper setting has been set.

10. On-Board Interrupt Handling

All on-board devices are able to force interrupts to the CPU on different levels. Table 4 shows the interrupt structure of the SYS68K/CPU-3VB:

Table 4

Device	Name	IRQ Level	Interrupt Auto Vector	Software Prog. Interrupt Vector
SWITCH	ABORT	7	X	
58167A	RTC	6	X	
68230	PI/T	5	X	
68451	MMU	4		X
68561	MPCC	3		X
68450	DMAC	2		X

11. The VMEbus Interface

The implemented VMEbus interface includes 23 address, 16 data, 6 address modifier and different control signals.
A 4 level Bus Arbiter with a prioritized scheme provides fast bus arbitration (if required).
A seperate slave bus arbitration on a jumper selectable level (0-3) provides the bus request/bus busy handshake to the used bus arbiter. 7 VMEbus interrupt request levels may be enabled/disabled via jumpers to provide a multi-processing environment.

12. The DEBUGGER Firmware Features

- EPROM resident system monitor/debugger
- More than 30 commands for debug, up/down-line load
- One-line assembler/disassembler for assembly language program development
- Full speed execution of system and user programs operating in the VMEbus oriented microcomputer system
- Terminal capability for up/downline load from another development system or any host computer
- Powerful software and system debug command set allowing access to all VME modules plus the full 16 Mbyte direct address range of the VME system bus
- Includes all required installation and operation documentation
- Access to monitor resources via vectored entries and a TRAP 14 calling sequence
- Start of user application program or optional software by command

The CPU-3VB DEBUGGER is an EPROM based resident package ready for immediate use with the VME monoboard CPU-3VB as well as for VME-based microcomputer products. It provides a powerful evaluation and system debugging tool for VME-based CPU systems. The EPROM resident package will operate in 16 Kbyte of ROM space. The CPU-3VB Monitor uses the first 1024 words of RAM storage for interrupt vectors and temporary storage.

The package permits full speed execution of system and user developed programs operated in a VME-based CPU system environment under complete operator control. Access to monitor resources and configuration control is given by vectored system entries and a TRAP 14 calling sequence.

13. Assembler/Disassembler Capability

The on-board assembler does not allow line numbers and labels; however, it is a powerful tool for creating, modifying, and debugging 68010 code. The on-board assembler processes each line of a program as an individual unit.

- In order to read back a program after it has been entered, the machine code is disassembled and then displayed as mnemonic and operands.
- The one-line assembler shows a question mark (?) under the portion of the source statement where an error probably occurred, or display a short error message.
- Only one directive (DC.W) is accepted.

The symbolic language used to code source programs for processing by the assembler is called 68010 assembly language. This language is a collection of mnemonics representing:

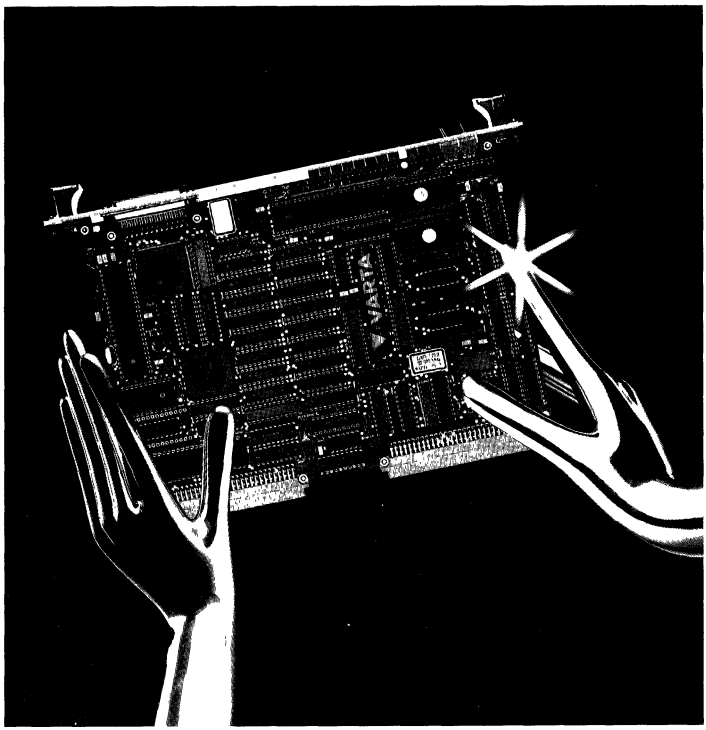
- Operations: 68010 machine instruction operation codes Directive (pseudo-op)
- Operators
- Special symbols

Specification of the SYS68K/CPU-3VB

Microprocessor	68010 CPU 10 MHz
DMA Controller	68450 DMAC 10 MHz
Memory Management Unit	68451 MMU 10MHz with software programmable address translation, paging and address range protection
Serial I/O	68561 Multi-Protocol Communication Controller with a software-selectable baud rate from 110 to 38400 baud and variable I/O signal assignment
Control	68230 PI/T for local control and timer function
Real Time Clock	58167 RTC with Calendar and on-board battery back-up
SRAM	128 Kbyte
EPROM	128 Kbyte of EPROM (max) (JEDEC compatible devices)
VMEbus	Full VMEbus compatible interface with a slave bus arbitration. Slot 1 Control functions.
Arbiter	4-level prioritized bus arbiter with bus clear generation.
Firmware	32 Kbyte of monitor called DEBUGGER
Power Requirements	+5V/3.9A (max) +12V/200mA (max) −12V/200mA (max)
Operating Temp	0 to +50 degrees C
Storage Temp	−50 to +85 degrees C
Relative Humidity	0 – 95% (non-condensing)
Board Dimensions	Double Eurocard 234 x 160 mm (9.2 x 6.3")

Ordering Information

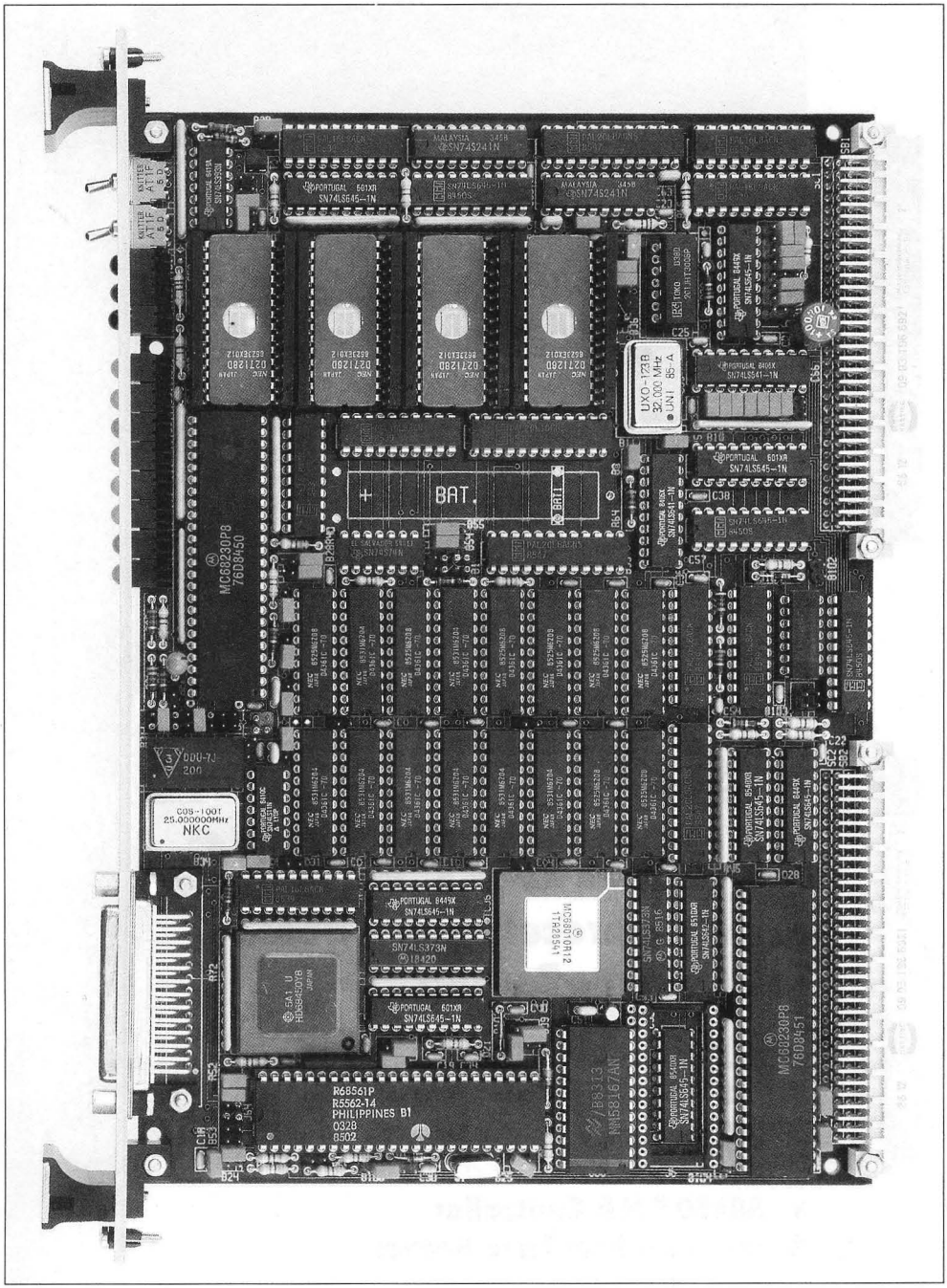
SYS68K/CPU-3VB Part No. 100312	68010 CPU Board with 10 MHz CPU and DMAC clock frequency, 128 Kbyte SRAM. HUM and SUM included.
SYS68K/CPU-3VB/HUM Part No. 800003	Hardware User's Manual
SYS68K/CPU-3VB/SUM Part No. 800038	Software User's Manual



System 68000 VME
SYS68K/CPU-4VC

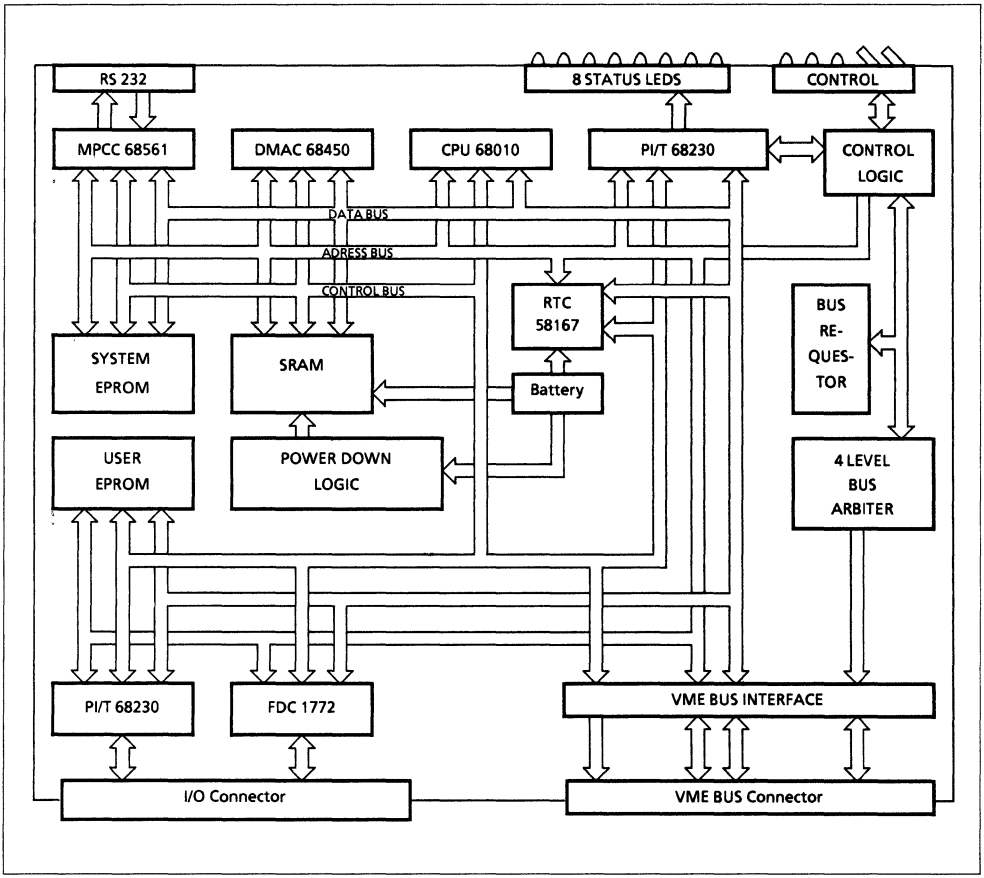
Fast Multiprocessor CPU Board with Battery-Backup

- 12.5 MHz 68010 CPU
- 128 Kbyte No Wait State SRAM
- 512 Kbyte EPROM capacity
- Real Time Clock
- 68450 DMA Controller
- Installed Real Time Kernel


BAT.
UXO-123B
32.000 MHz
R68561P
R5562-14
PHILIPPINES B1
0328
0502
MC68020PB
76DB451
SN74LS373N
SN74LS645-1N

General Description SYS68K/CPU-4VC
The SYS68K/CPU-4VC board is a high performance multi-processor computer board built around the virtual 68010 CPU and the VMEbus.
It contains a Direct Memory Access Controller, 32 or 128 Kbyte SRAM, up to 512 Kbyte EPROM and powerful control functions.
The implemented VMEbus interface is fully VMEbus and IEEE 1014 standard compatible and includes a slave bus arbitration as well as a four level prioritized Arbiter.
The block diagram shows the SYS68K/CPU-4VC board structure in detail.

BLOCK DIAGRAM OF THE SYS68K/CPU-4VC



SYS68K/CPU-4VC Features

- 68010 CPU with 12.5MHz clock frequency
- 68450 Direct Memory Access Controller with 8MHz clock frequency
- 68561 Multi-Protocol Communications Controller with an RS232-compatible interface
- 68230 Parallel Interface and Timer Module with 8MHz clock frequency for local control and status display
- 68230 PIT with 8MHz clock frequency for parallel I/O on P2 connector
- 58167 Real Time Clock with battery backup
- 128 Kbyte of high-speed static RAM with on-board battery backup
- 8 EPROM sockets for system and/or user programs (max. 512 Kbyte)
- All on-board devices are able to interrupt the on-board CPU (vector or auto-vector)
- 4 level Bus Arbiter (prioritized scheme)
- Bus Requester on a jumper selectable level (0-3)
- RESET and ABORT function switches
- 8 status LEDs
- Powerful Real Rime Monitor/Debugger VME-PROM on board
- High level Real Time Operating Systems are available for different applications
- Optionally available:
  1772 Floppy Disk Controller for up to four 3", $3^1/_2$", $5^1/_4$" Drives

Functional Description

The DMA Controller and Multi-Protocol Communication Controller communicate with the CPU via the unbuffered address and data bus. The EPROM areas, static RAM, Real Time Clock, Parallel Interface and Timer Module as well as the VMEbus interface communicate with the CPU via the buffered address bus.
Table 1 shows the global memory layout, and the various functional areas of the board are described briefly in the following paragraphs.

1. 68010 Central Processing Unit

The high performance 68010 CPU with its up-graded 68000 instruction set and virtual memory support offers a total of 16 Mbyte of addressable memory through its 23 address signals. The fully asynchronous 16 bit data bus allows high speed data transfers to/from the on-board or VMEbus memory and I/O areas.
The SYS68K/CPU-4VC series uses a 12.5 MHz 68010 processor. To provide for fault tolerant systems, the CPU provides excellent exception handling if an error or interrupt occurs. The state and all addresses, as well as the fault address are stored on the stack to provide diagnostic and correction as well as re-run functions.

Table 1 CPU-4VC Memory Layout

Address	Description
000000 to 000007	Start Vectors from System EPROM
000008 to 01FFFF	Static RAM
008000 or 020000 to EFFFFF	VMEbus Addresses
F00000 to F7FFFF	SYSTEM and USER EPROM Area
F80000 to F8FFFF	LOCAL I/O Devices
F90000 to FEFFFF	VMEbus Addresses
FF0000 to FFFFFF	Short I/O VMEbus Addresses

2. 68450 Direct Memory Access Controller

A high-speed DMA Controller with 8 MHz clock frequency is used on the board to move data to and from the VMEbus. Its four channels can be used from the operating system and/or shared with user programs.
The DMAC has a maximum data transfer speed of 4 Mbyte per second. Time-critical programs can thus be loaded into the local RAM via the DMAC, giving number cruncher applications no time overhead through the VMEbus. This also results in a lower VMEbus load.

3. The Static RAM

The SYS68K/CPU-4VC contains a static memory of 128 Kbyte with a maximum access time of 70ns.
A separate power-down logic on every board is used to disable the SRAM chips when the main power is out of spec. The on-board battery is used for the standby power of the SRAM chips (approx. 1000h data retention).
Each static RAM access (read and write) of the processor runs without any wait states at 12.5MHz clock frequency.

4. The SYSTEM and USER Area

The SYSTEM area consists of two sockets for JEDEC-compatible EPROM devices. The VME-PROM firmware resides with its boot-up and I/O control functions in two EPROM devices (included in the shipment).
The USER area (6 sockets) is provided for the use of EPROMs or SRAMs (JEDEC compatible pin-out).

Table 3 lists the usable device type for each area.

Device	Type	Organi-zation	System Area	User Area 1-3	Total Capacity
2764	EPROM	8 Kx8	X	X	64 KBYTE
27128	EPROM	16 Kx8	X	X	128 KBYTE
27256	EPROM	32 Kx8	X	X	256 KBYTE
27512	EPROM	64 Kx8	X	X	512 KBYTE
6264	SRAM	8 Kx8		X	32 KBYTE

The access speeds for the SYSTEM and for the USER areas are jumper-selectable from 100ns to 400ns.

5. 68561 Multi-Protocol Communication Controller

The MPCC contains different protocols to communicate via the RS232-compatible interface to a user-supplied serial communication device.
Protocols:
- IBM binary synchronous (ASCII or EBCDIC)
- Character oriented protocols (BSC, DDCMP, X3.28, X.21,ECMA16 etc.)
- Synchronous Bit oriented protocols (SDLC, HDLC, ADCCP, X.25)

A software-programmable baud rate from 110 to 38400 baud and a local loop-back mode provide maximum flexibility.
The I/O signal assignment of the 4 input and 4 output signals to the 25 pin D-Sub connector on the front panel is jumper selectable.
The MPCC is able to force an interrupt with 3 different software programmable vectors to the CPU.

6. The Local Control

The Parallel Interface and Timer Module (PI/T) with its 8MHz clock frequency allows an optical status display through eight yellow status LED's on the front panel.
Each interrupt request level (0-7) can be enabled or disabled independent from each other through the CPU. The exception signals ACFAIL and SYSFAIL are monitored through the 3rd PI/T port.
The bus release functions are also software programmable through the 3rd port.
The PI/T includes a 24-bit programmable timer with a 5 bit prescaler. This timer may be used for measuring time delays or as a watchdog timer.
The PI/T timer interrupt request signal is used to force an auto-vectored interrupt to the CPU.

7. The Parallel I/O Port

A second PI/T is used on the board to provide parallel I/O via the P2 connector. Two 8 bit bidirectional ports can be used for bit I/O or special control functions via 4 handshake interface signals.
The port interrupt causes an interrupt request to the on-board CPU on level 4. The 4 different software programmable IRQ vectors offer maximum flexibility for program handling.

8. 58167 Programmable Real Time Clock

The on-board RTC with its RAM array allows various applications such as time scheduling, time measurement and time-out counters.
Additionally, the RTC may act as an actual time base independent from the main power, providing month, day of month, and day of week. An onboard battery ensures time base operation during power-down.

9. 1772 Floppy Disk Controller Option

The optionally available Single Chip Floppy Disk Controller (FDC) offers the capability of using the SYS68K/CPU-4VC board versions in process control applications without any other mass memory controllers.
The FDC controls up to 4 different drives (3", 3 1/2" or 5 1/4") either single or double sided with single or double density (software programmable). Additionally, the step-rate is software programmable from 1ms to 6ms.
All drive select signals and status lines from the disk interface are controlled via the PI/T. Easy interface is provided through the P2 I/O pins, which fit into a 1:1 connection via a flat cable to the floppy drive edge connector.
An interrupt after operation completion can be generated to the CPU via the PI/T. For high asynchronous use of the floppy, the FDC is connected to the DMAC via its data request signal. The DMA is provided on the board to use the FDC in critical real-time applications. The CPU and the DMAC/FDC work fully asynchronous.
The FDC must be ordered separately for every CPU-4 board version.

10. On-Board Exception Handling

The board contains two switches, one for RESET and one for ABORT. During an activated RESET, all on-board devices along with the CPU are reset. Additionally, the reset (SYSRESET*) can be forced to the VMEbus if this card is used as the system controller (slot 1 functions).
During a pushed ABORT switch, an interrupt (non-maskable) is forced to the CPU.
The 16MHz SYSCLK signal can be forced to the VMEbus if a jumper setting has been provided.

11. On-Board Interrupt Handling

All on-board devices are able to force interrupts to the CPU on different levels. Table 4 shows the interrupt structure of the SYS68K/CPU-4VC.

Table 4

Device	Name	IRQ Level	Interrupt Auto Vector	Software Prog. Interrupt Vector
SWITCH	ABORT	7	X	
58167A	RTC	6	X	
68230	PI/T1	5	X	
68230	PI/T2 (FDC)	4		X
68561	MPCC	3		X
68450	DMAC	2		X

12. The VMEbus Interface

The implemented VMEbus interface includes 23 address, 16 data, 6 address modifier and different control signals.
A 4 level Bus Arbiter with a prioritized scheme provides fast bus arbitration (if required).
A separate bus arbitration on a jumper selectable level (0-3) provides the bus request/bus busy handshake to the used bus arbiter. Each VMEbus interrupt request level may be enabled or disabled via a jumper to provide multiprocessing capabilities.
The board supports the Release When Done (RWD), Release on Bus Clear (ROBCLR) as well as the Release after Time-out (RAT) function (all software programmable).

13. Software Description

VMEPROM is an EPROM based real-time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM.
VMEPROM is composed of the powerful PDOS real-time kernel and the PDOS file manager. Thus the package provides support of a highly sophisticated real-time kernel and an interface to floppy and hard disk drives.
The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition it includes a powerful line assembler and disassembler for the 68000/68010.

VMEPROM features:

- Real-Time Multitasking Kernel supporting up to 64 tasks.
- File Management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Line assembler/disassembler with full support of all 68000/68010 instructions.
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify.
- S-record up-/downloading from any port defined in the system.
- Disk support for RAM-disk, floppy and winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. VMEPROM also allows disk formatting and initialisation.
- Serial I/O support for up to two SIO-2 or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full Screen Editor.
- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.

13.1 Description of the User Interface of VMEPROM

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple command lines may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The Command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

13.2 Description of the Kernel Functions

The kernel of VMEPROM is written in 680 x 0 assembly language for fast and efficient execution. It provides multitasking, system clock, event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously.
Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

13.3 Description of the File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

13.4 Supported VMEbus Hardware

Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards and one disk controller.
In addition, EPROM programming is supported by VMEPROM utilising the SYS68K/RR-2/3 board family.

13.5 Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VME-PROM kernel and file manager is about 40 Kbytes. Small romable applications can be put in EPROMS easily without the overhead of the user interface.

13.6 Development Systems

Currently either one of the FORCE PDOS* or UNIX System V* development stations may be used for software development for VMEPROM.
Compilers, Assemblers, and Libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.

13.7 Licensing

No license is required for VMEPROM. VMEPROM is delivered free of charge and is already installed on every CPU-4 board.
VMEPROM will be available on the CPU-4VC in Q4/87.

14. Available Software

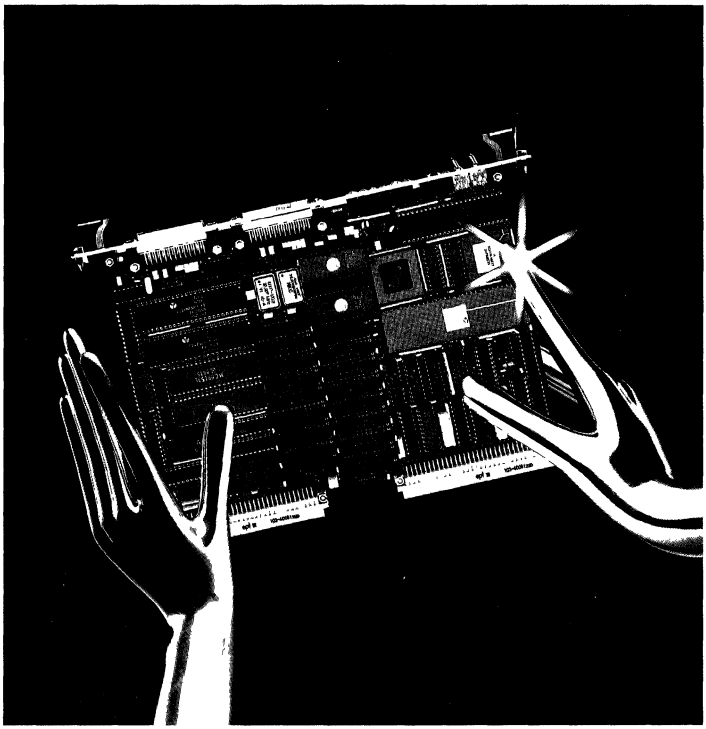
The multiuser multitasking disk operating system PDOS is available for each of the SYS68K/CPU-4V products. PASCAL,C,FORTRAN 77 and a powerful macro assembler supports the various applications. Please refer to the SYS68K/PDOS data sheet for further information.

Specification of the SYS68K/CPU-4VC Boards

Microprocessor	68010 CPU 12.5 MHz
DMA Controller	68450 DMAC 8 MHz
Serial I/O	68561 Multi-Protocol Communication Controller with a software-selectable baud rate from 110 to 38400 baud and variable I/O signal assignment
Parallel I/O	Two 8 bit ports and 4 handshake signals are available on the P2 connector through a PI/T device
Control	68230 PI/T for local control and timer function
Real Time Clock	58167 RTC with Calendar and on-board battery backup
SRAM	128 Kbyte (with battery backup)
EPROM	512 Kbyte of EPROM (max) (JEDEC compatible devices)
VMEbus	Full VMEbus compatible interface with bus arbitration. Slot 1 Control functions.
Arbiter	4-level prioritized bus arbiter with bus clear generation.
Firmware	128 Kbyte of firmware (VMEPROM)
Power Requirements	+5V/3.9A (max) +12V/200mA (max) -12V/200mA (max)
Operating Temperature	0 to +50 degrees C
Storage Temperature	−50 to +85 degrees C
Relative Humidity	0−95% (non-condensing)
Board Dimensions	Double Eurocard 234 x 160 mm (9.2 x 6.3")
Optionally Available:	
Floppy Controller	WD1772 Single Chip Floppy Controller for up to four 5 1/4" drives

Ordering Information

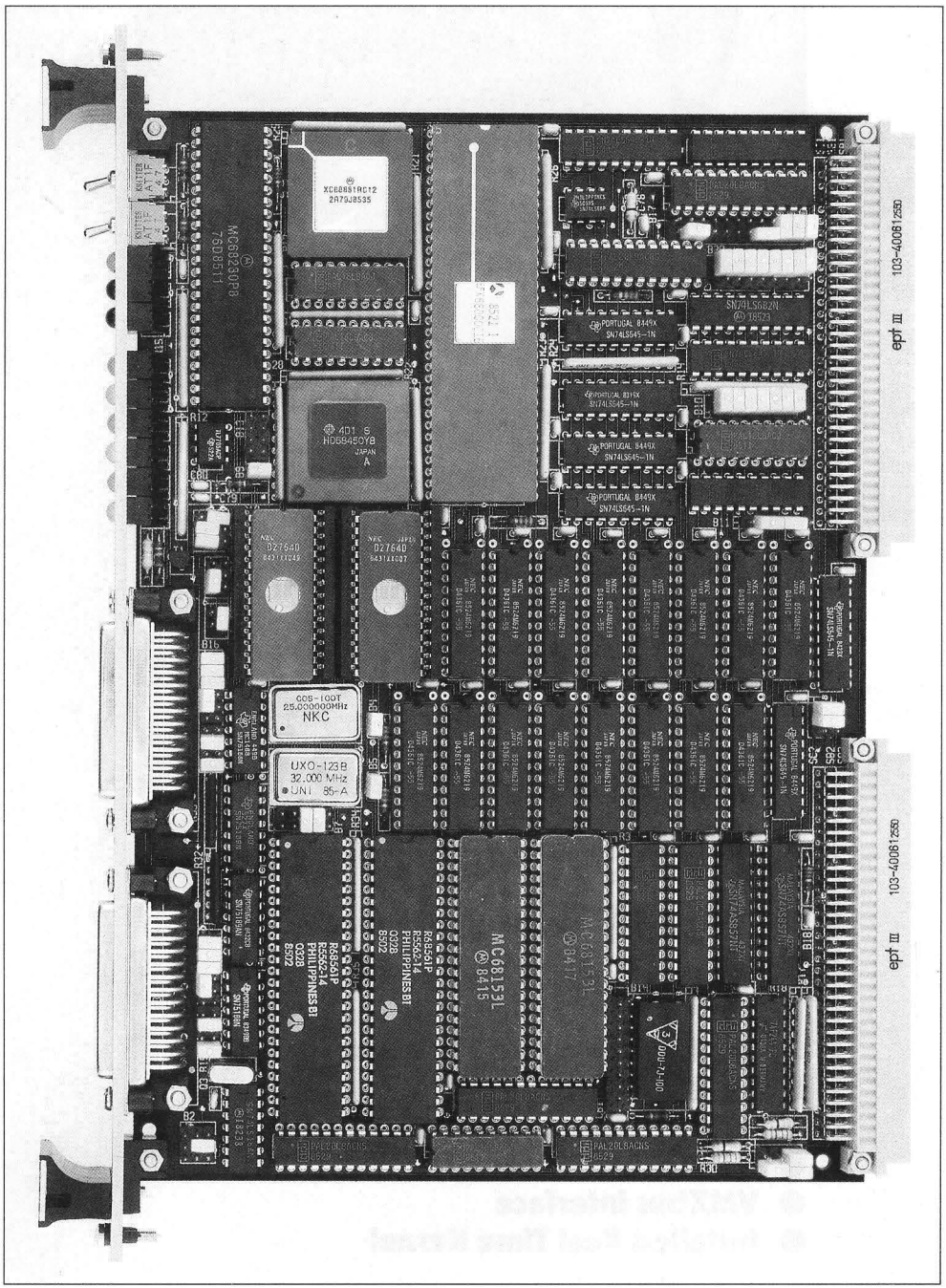
SYS68K/CPU-4VC Part No. 100413	68010 CPU Board with 12,5MHz CPU and 128 Kbyte SRAM. (with battery backup) Debugger software and User's Manual included.
SYS68K/CPU-4FDC Part No. 110040	Floppy Disk Controller option (1772) supporting up to four drives (3", 3 1/2", or 5 1/4")
SYS68K/CPU-4VC/UM Part No. 800102	User's Manual for CPU-4VC
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM User's Manual



System 68000 VME SYS68K/CPU-5A

16MHz CPU Board with Floating Point Co-Processor

- 128 Kbyte No Wait State SRAM
- 68881 FPCP
- 68450 DMA Controller
- 2 RS232 Interfaces
- VMXbus Interface
- Installed Real Time Kernel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HD68450CB
JAPAN
D27640
D27640
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NKC
UXO-123B
32.000 MHz
UNI 85-A
MC68153L
MC68153L
R6856IP
R6856IP
R6856IP
R6856IP
PAL20L8ACNS
PAL20L8ACNS
SN74LS682N
SN74LS645-1N
SN74LS645-1N
SN74LS645-1N
SN74LS645-1N

General Description

The SYS68K/CPU-5A boards are high speed computer boards built around the 68000/68010 CPU and the ultra fast Floating Point Co-Processor 68881.

Zero wait state operation is performed at 16,7 MHz CPU clock frequency by accessing the 128 Kbyte high speed static RAM.

The installed four channel DMA Controller is capable of transferring data from memory to memory or from the two serial interfaces to memory.

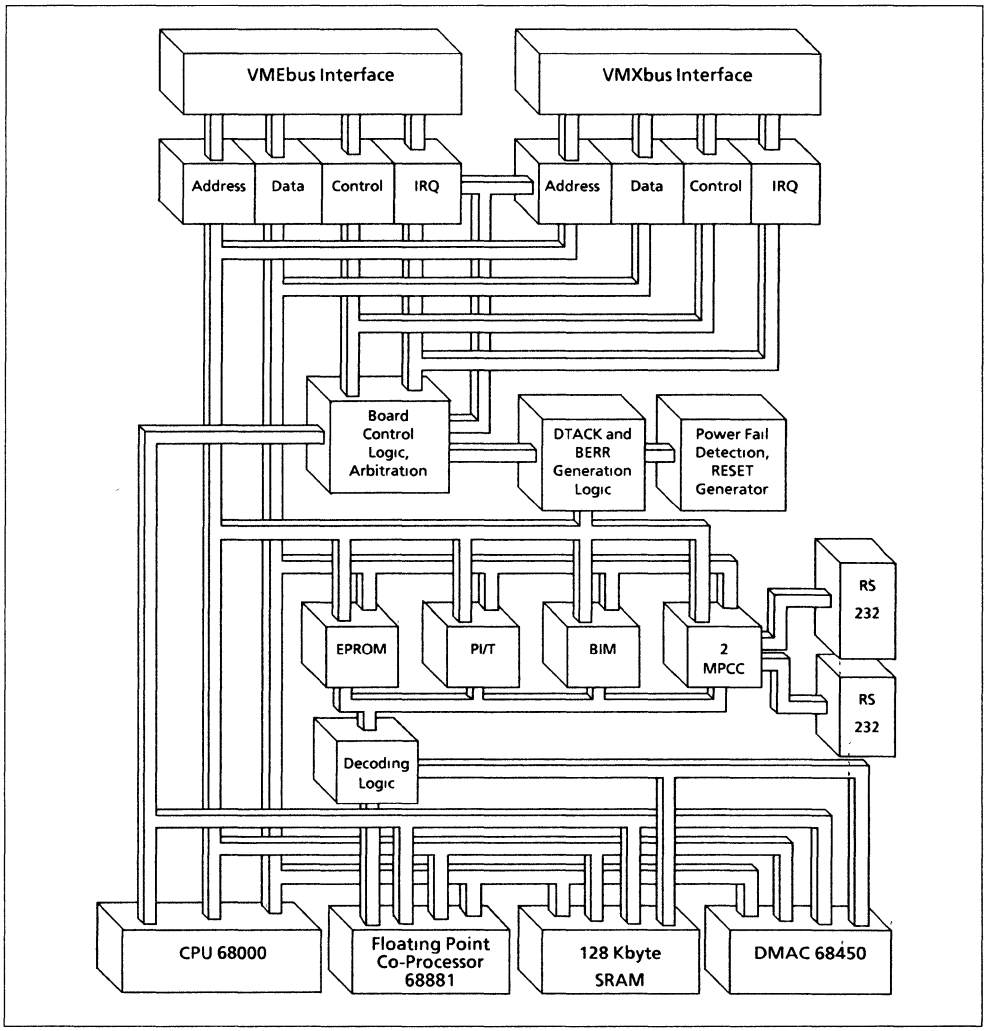
One Parallel Interface and Timer Module offers a software programmable timer as well as VMEbus exception signal handling.

The implemented VMEbus interface is fully VMEbus and IEEE 1014 standard compatible and includes a one level arbiter.

The primary VMXbus interface completes the board and offers optimized multiprocessing support.

The block diagram shows the board structure of the CPU-5 in detail.

BLOCK DIAGRAM OF THE SYS68K/CPU-5A



SYS68K/CPU-5A Features

- 68000 CPU with 16.7 MHz clock frequency.
- 68881 Floating Point Co-Processor with 16.7 MHz clock frequency.
- 68450 DMA Controller with 8MHz clock frequency.
- 68561 Multi Protocol Communications Controllers with two RS232 compatible interfaces.
- 68230 Parallel Interface and Timer Module with 8 MHz clock frequency.
- 128 Kbyte of zero wait state static RAM.
- 4 EPROM sockets for system and/or user programs.
- All on-board interrupt requests are software programmable (level and vector).
- Each VMEbus IRQ (1-7) can be enabled or disabled via software through the PI/T.
- Single level arbiter.
- VMEbus interface (A24:D8,D16;A16:D8,D16).
- VMXbus primary master interface (A24:D16).
- Powerful real time Monitor/Debugger VME-PROM on board.
- 9 Status LED's, RESET and ABORT function switch.

1. 68000/68010 Central Processing Unit

The high performance 68010 CPU with its upgraded 68000 instruction set and virtual memory support offers a total of 16 Mbyte of addressable memory through its 24 address signals. The fully asynchronous 16 bit data bus allows high speed data transfer to/from the on-board, VME- or VMXbus memory and I/O areas.
The SYS68K/CPU-5A uses a 16.7 MHz 68000 processor and runs constantly without wait states from the 128 Kbyte of static RAM.

The following table shows the global memory layout of the CPU-5A board:

Address	Description
000000 to 000007	Start Vectors from System EPROM
000008 to 01FFFF	Static RAM on CPU-5A (128 Kbyte)
020000 to xxxxxx	VME or VMXbus Addresses
xxxxxx to EFFFFF	VMX or VMEbus Addresses
F00000 to F3FFFF	SYSTEM and USER EPROM Area
F80000 to F8FFFF	LOCAL I/O Devices
F90000 to FEFFFF	VMEbus Addresses
FF0000 to FFFFFF	Short I/O VMEbus Addresses

2. The Floating Point Co-Processor:

The 68881 Floating Point Co-Processor is a full implementation of the IEEE Standard P754 for Floating Point Arithmetic (Draft 10.0).
A set of 8 general Floating Point Data Registers, supporting full 80 bit extended precision are available for arithmetic operations such as:

Add	Sine, cosine, hyperbolic sine and cosine
Subtract	Tangent, cotangent, hyperbolic tangent and cotangent
Multiply	e EXP(x)
Divide	e EXP(x−1)
Compare	E EXP(xtract (4))
Scale Exponent	ln (x), ln (x+1)
Modulo	log 10 (x), log 2 (x)
Conditional branches	2 EXP(x), 10 EXP (x)
Absolute value	Square root
	Conditional Trap (32)

The FPCP supports the following data types:
Byte, Word and Long Integers
Single, Double and Extended Precision Real Numbers
Packed BCD String Real Numbers
The SYS68K/CPU-5A is fitted with a 16,7MHz FPCP.

3. The Static RAM

Zero wait state operation for the CPU and the DMAC at 12,5 or 16,7MHz clock frequency is provided by using the 16 static RAM's.
128 Kbyte of SRAM with a maximum access time of 55ns is provided on each CPU-5A board for program and/or data storage.

4. The SYSTEM and the USER Area

The CPU-5A contains four sockets for JEDEC compatible EPROM devices. Two 27128 devices are used for VMEPROM (included in the shipment).
The following table lists the usable EPROM types for each area:

Device	Organization	TOTAL Capacity
2764	8 K x 8	32 Kbyte
27128	16 K x 8	64 Kbyte
27256	32 K x 8	128 Kbyte
27512	64 K x 8	256 Kbyte

The access time for both areas is jumper selectable in the range of 100-400ns to adapt different EPROM access times.

5. 68450 Direct Memory Access Controller

A high-speed DMA Controller with 8MHz clock frequency is used on the board to move data on the local, VMX- and the VMEbus. Its four channels can be used from the operating system and/or shared with user programs.
The DMAC has a maximum data transfer speed of 4 MBytes per second. Time critical programs can thus be loaded into the local RAM via the DMAC, which allows number cruncher applications to run without the time overhead through the VME/VMXbus. This also results in a lower bus load.
The 68450 is connected to the two serial interface channels to optimise serial communication (if required).

6. 68561 Multi-Protocol Communication Controllers

The CPU-5A board contains two serial interfaces for communication to a terminal and/or printer/host computer.
The MPCC offers different protocols to communicate via the RS232-compatible interface to a user-supplied serial communication device.
Protocols:

- IBM binary synchronous (ASCII or EBCDIC).
- Character oriented protocols (BSC, DDCMP, X3.28, X.21, ECMA 16 etc.)
- Synchronous Bit oriented protocols (SDLC, HDLC, ADCCP, X.25).

A software-programmable baud rate from 110 to 38400 baud and a local loop-back mode provide maximum flexibility.
The I/O signal assignment of the 4 input and 4 output signals per channel to the 25 pin D-Sub-connectors on the front panel is jumper selectable.
The MPCC is able to force an interrupt with 3 different software programmable vectors to the CPU.

7. The Local Control

The Parallel Interface and Timer Module (PI/T) with its 8MHz clock frequency allows an optical status display through six yellow status LEDs mounted on the front panel.
Each interrupt request level from the VMEbus can be enabled or disabled independent from each other through the CPU (dynamically). The VMEbus signals ACFAIL and SYSFAIL are monitored through the 3rd PI/T port.
The bus release functions described in the VMEbus section are also software programmable.
The PI/T includes a 24-bit programmable timer with a 5 bit prescaler. This timer may be used for measuring time delays or as a watchdog timer.

8. The Interrupt Structure

The CPU-5A contains two Bus Interrupter Modules to provide a flexible interrupt structure for multiprocessor applications.
Each on-board interrupt request is software programmable to one of the IRQ levels of the CPU. The vector is also free software programmable.

The following table lists all the on-board interrupt sources:

Interrupt	Device
ABORT	SWITCH
TIMER	PI/T
Serial I/O 1	MPCC 1
Serial I/O 2	MPCC 2
DMAC	DMAC
ACFAIL	VMEbus
SYSFAIL	VMEbus
IRQVMX	VMXbus

The VMXbus interrupt request is routed into the on-board IRQ structure to offer maximum flexibility (software programmable level and vector).
The VMEbus interrupt requests can be dynamically enabled or disabled to the CPU through the PI/T device. This allows dynamic adaption for high end multi-processor environments because each of the IRQ's (1-7) can be selected separately under run time of the CPU (no jumper settings are required).

9. The VMXbus Interface
The CPU-5A board contains a primary VMXbus interface with a jumper selectable access address range in the whole address space of 16 Mbyte.
24 address lines and 16 data lines are supported from the VMXbus interface. The early DTACK option can be used to speed up the access cycles.

10. The VMEbus Interface
The implemented interface supports 24 address, 16 data, 6 address modifiers and all the control signals.
The transfer of 8 and 16 bit (A24: D8, D16) is supported.
Software programmable bus release functions allow flexible adjustment to the various application dependent requirements.

ROR	Release on Request
RBCLR	Release on Bus Clear
RAT	Release after Time-Out
RWD	Release when Done

The single level arbiter included on the board simplifies installation of the CPU-5A into a VMEbus environment.

11. Software Description
VMEPROM is an EPROM based real-time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM.
VMEPROM is composed of the powerful PDOS real-time kernel and the PDOS file manager. Thus the package provides support of a highly sophisticated real-time kernel and an interface to floppy and hard disk drives.
The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition it includes a powerful line assembler and disassembler for the 68000/68010.

VMEPROM features:
- Real-Time Multitasking Kernel supporting up to 64 tasks.
- File Management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Line assembler/disassembler with full support of all 68000/68010 instructions.
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify.
- S-record up-/downloading from any port defined in the system.
- Disk support for RAM-disk, floppy and winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. VMEPROM also allows disk formatting and initialisation.
- Serial I/O support for up to two SIO-2 or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full Screen Editor.
- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.

11.1 Description of the User Interface of VMEPROM

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple command lines may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The Command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

11.2 Description of the Kernel Functions

The kernel of VMEPROM is written in 680 x 0 assembly language for fast and efficient execution. It provides multitasking, system clock, event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously.
Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

11.3 Description of the File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

11.4 Supported VMEbus Hardware

Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards and one disk controller.
In addition, EPROM programming is supported by VMEPROM utilising the SYS68K/RR-2/3 board family.

11.5 Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 40 Kbytes. Small romable applications can be put in EPROMS easily without the overhead of the user interface.

11.6 Development Systems

Currently either one of the FORCE PDOS* or UNIX System V* development stations may be used for software development for VMEPROM.
Compilers, Assemblers, and Libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.

11.7 Licensing

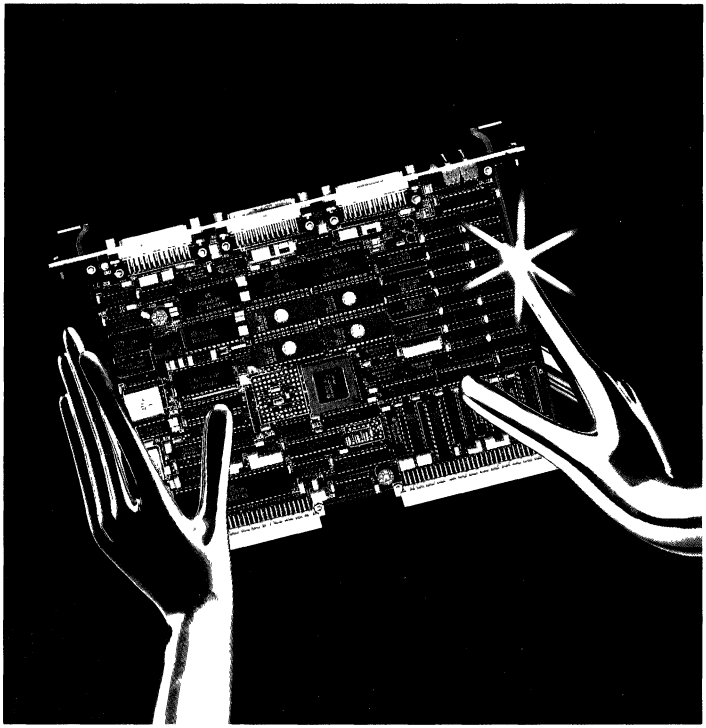
No license is required for VMEPROM. VMEPROM is delivered free of charge and is already installed on every CPU-5A board.
VMEPROM will be available on the CPU-5A in Q4/87.

Specifications of the SYS68K/CPU-5A Boards

Microprocessors	68000 CPU 16.7MHz on CPU-5A
Floating Point, Co-Processor	68881 FPCP 16,7MHz on CPU-5A
SRAM	128 Kbyte of zero wait state static RAM (16,7MHz operation)
EPROM	4 Sockets for JEDEC compatible EPROM's (256 Kbyte max)
CONTROL	68230 PI/T for interrupt control and timer function
DMA Controller	68450 DMAC (8MHz)
Serial I/O	68561 MPCC with software programmable protocolls and baud rate 2 serial interfaces RS232 compatible
Interrupts	All on-board interrupts are software programmable on level and vector. Off-board interrupts can be enabled/disabled via software (dynamically)
VMXbus	Primary VMXbus interface: A24:D8, D16, early DTACK option
VMEbus	VMEbus interface A24: D8, D16 A16: D8, D16 IRQ handler (1-7 dynamically) Single level arbiter Requester (0-3 static)
Firmware	128 Kbyte of firmware (VMEPROM)
Power Requirements	+ 5V/5.0A(max) +12V/200mA(max) −12V/200mA(max)
Operating Temperature	0 to +50 degrees C
Storage Temperature	−50 to +85 degrees C
Relative Humidity	0–95% (non-condensing)
Board Dimensions	Double Eurocard 234x160mm (9.2x6.3")

Ordering Information

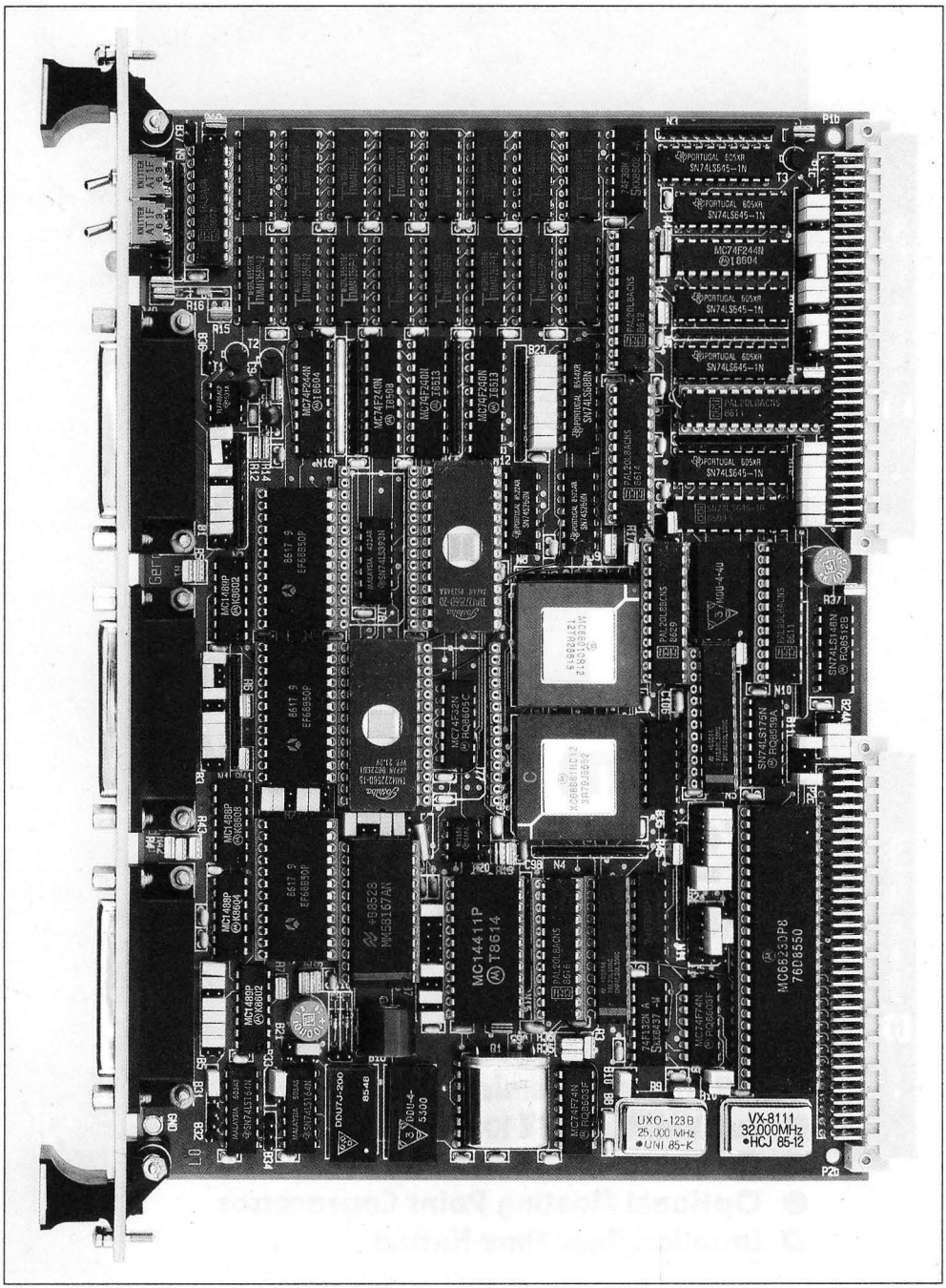
SYS68K/CPU-5A Part No. 100501	16,7MHz 68000 CPU board with Floating Point Co-Processor (16.7MHz) and VMEPROM, UM included.
SYS68K/CPU-5 UM Part No. 800078	User's Manual for CPU-5A
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM User's Manual



System 68000 VME SYS68K/CPU-6

Flexible CPU with Floating Point Support

- 68000/68010 CPU board
- 512 Kbyte dynamic RAM
- Full VMEbus IEEE 1014 standard compatible
- Flexible I/O structure
- Optional Floating Point Coprocessor
- Installed Real Time Kernel

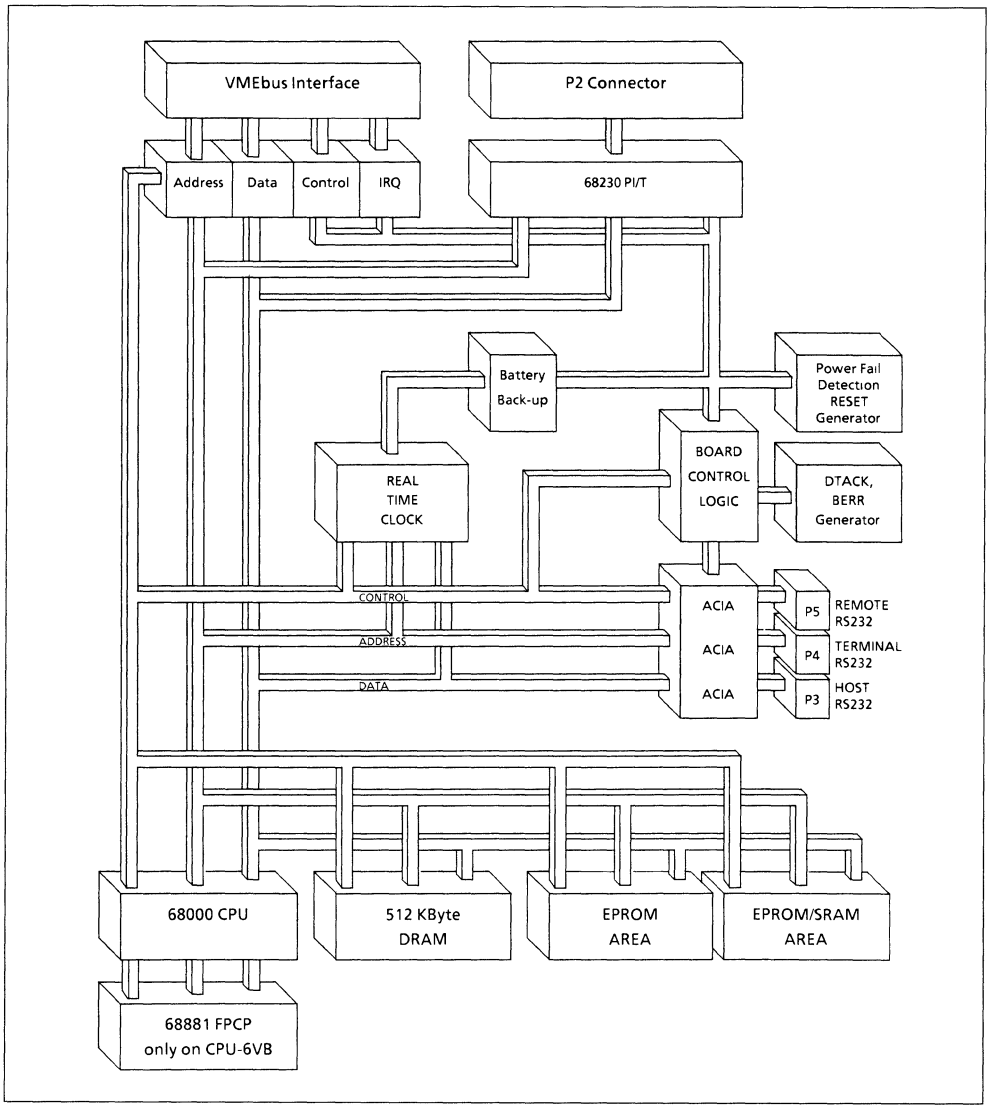

MC144111P
T8614
UXO-123B
25.000 MHz
•UNI 85-K
VX-8111
32.000MHz
•HCJ 85-12

General Description

The general purpose SYS68K/CPU-6 board is a high speed VMEbus board based on a 68000/68010 processor. It contains 512 Kbyte of dynamic RAM, 3 serial I/O interfaces, up to 256 Kbyte of EPROM and a parallel I/O interface as well as a Real Time Clock.

The implemented VMEbus interface is IEEE 1014 standard compatible, and features a single level arbiter, a SYSCLK-driver and a power monitor/RESET generator.
Details of the structure of CPU-6 are shown in the block diagram.

BLOCK DIAGRAM OF THE SYS68K/CPU-6



SYS68K/CPU-6 Features

- 68000 CPU (8,0MHz) on CPU-6
  68000 CPU (12,5MHz) on CPU-6A
  68010 CPU (12,5MHz) on CPU-6VA/6VB
- 512 Kbyte of dynamic RAM
  0 Wait States at 8MHz
  1 Wait State at 12,5MHz
  Distributed hardware refresh every 15us
- 4 EPROM sockets provide 256 Kbyte space
- 3 serial communication ports
  (RS232 compatible)
- Parallel I/O interface to P2 connector
- Real Time Clock with on-board battery back-up
- 24-bit timer with 5-bit prescaler
- Local interrupt service via auto-vectoring
- Fully VMEbus IEEE 1014 standard compatible
- RESET and ABORT function switches
- Double Eurocard from factor
- Powerful real time Monitor/Debugger VME-PROM on board
- PDOS* Real Time Operating System optionally available
- Fully software and I/O signal compatible to the SYS68K/CPU-1B series

Additional Features of CPU-6VB

- 68881 Floating Point Co-Processor with 12,5 MHz clock frequency

Functional Description

Memory, Real Time Clock, serial and parallel I/O communicate to the CPU via their internal system bus.
The global memory layout and the I/O address assignment are outlined below:

START Address	END Address	
000000	000007	Initialisation vectors from system EPROM
000008	07FFFF	Dynamic RAM
080008	09FFFF	SYSTEM EPROM
0A0000	0BFFFF	USER EPROM
0E0000	0FFFFF	I/O interfaces
100000	FEFFFF	VMEbus standard addressing (A24:)
FF0000	FFFFFF	VMEbus short I/O addressing (A16:)

1. 68000/68010 Central Processing Unit

The high performance 68010 CPU with its upgraded 68000 instruction set and virtual memory support offers a total of 16 Mbyte of addressable memory through its 23 address signals. The fully asynchronous 16-bit data bus allows high speed data transfer to/from the on-board and VMEbus memory.

2. The Dynamic RAM

512 Kbyte DRAM is provided on all CPU-6 versions. Zero Wait State operation at 8MHZ CPU clock frequency is provided to optimize data throughput on CPU-6.
CPU-6A, 6VA and 6VB are equipped with a 12.5 MHz processor and need only 1 wait state to read data from the local DRAM.
For critical real time applications the distributed "RAS only" refresh can delay every 15 microseconds a pending access for a maximum of 290ns. The refresh works asynchronous to the CPU and guarantees refreshing of the DRAMs independent of the processor state.

3. The EPROM Memory

The SYS68K/CPU-6 consists of two different memory banks, both 16 bits wide and 128 Kbyte deep. The SYSTEM Area and the USER Area can be configured for the following devices:

Device	Type	Organisation	System Area	User Area
2764	EPROM	8 K x 8	x	x
27128	EPROM	16 K x 8	x	x
27256	EPROM	32 K x 8	x	x
27512	EPROM	64 K x 8	x	x
6264	SRAM	8 K x 8		x
62256	SRAM	32 K x 8		x

The total capacity of both areas is 256 Kbyte using four 27512 devices. Access time selection between 150 and 350ns for both areas allows the use of a wide variety of chips.

4. Serial Communication Ports

Three asynchronous serial communication ports (using a 68B50 ACIA chip) designated for the terminal, for the host, and for user applications are provided on the board. All of these ports are RS232-compatible. The terminal acts as a user interface and works in conjunction with FORCEbug. An operational transparent mode condition is callable via the system monitor. This transparent mode effectively bypasses the board and allows the terminal to communicate directly with the host. The third serial communication port interfaces either to a printer, or acts as a remote link to another computer. Each serial port has a jumper selectable data transmission rate (110-9600 or 600-19200 baud).
For each serial port, each of the I/O signals can be assigned to one of the 25 pin D-sub female connectors on the front panel.

5. Parallel I/O
The board contains a Parallel Interface and Timer chip (PI/T 68230) with a clock frequency of 8MHz.
The PI/T operates in uni- or bi-directional mode either 8 or 16 bits wide.
Each of the I/O lines can be configured as an input or as an output by programming the PI/T.
For asynchronous software control, the third 8-bit port can be configured to drive an interrupt on level 5 to the CPU.

6. Programmable Timer
The PI/T includes a 24-bit programmable timer. The timer is a synchronous counter to be used for generating or measuring time delays and various frequencies. The timer is either clocked by a 5-bit prescaler or directly, and the clock source can either be the 8MHz system clock or an external clock.

7. Programmable Real Time Clock
The on-board Real Time Clock (58167A RTC) allows various applications, such as time scheduling, time comparsion, time-out counter, etc. Additionally, the RTC may act as an actual time base providing month, day of month and day of week. An on-board battery back-up ensures time base operation during power down times.

8. On-Board Interrupt Handling
All on-board devices are able force interrupts on different levels to the CPU. In this case the auto-interrupt vector of the 68000 will be forced and each device has its own interrupt vector. Each service of a local interrupt does not cause a VMEbus request.
The following table shows the interrupt structure of CPU-6.

Description	Device	Level	Vector No.
ABORT	Switch	7	31
Real Time Clock	58167A	6	30
Parallel Interface and Timer	68230	5	29
Terminal ACIA	6850	4	28
Remote ACIA	6850	3	27
Host ACIA	6850	2	26

9. The VMEbus Interrupts
Each of the 7 defined VMEbus IRQs can be separately enabled or disabled for servicing through the local CPU. Only a jumper setting is required to enable the corresponding VMEbus IRQ.

10. The VMEbus Interface
The implemented VMEbus interface supports 23 address, 16 data, 6 address modifier and all the control signals defined in the IEEE 1014 standard.
All the electrical, mechanical and timing specifications are realized on the CPU-6 series of boards.
The following address and data transfer types are supported:
A16: D8, D16
A24: D8, D16
To support single processor and multi-master applications, CPU-6 includes a Single Level Arbiter and a SYSCLK driver. Both functions can be disabled for multi-processor applications.
Bus mastership is only requested if the VMEbus is addressed. The level is jumper selectable (0, 1, 2 or 3). A time-out counter for bus mastership (RAT) and the Release on Bus Clear (RBCLR) options are installed on the board to allow the use of CPU-6 in high end multi-processor environments.
A RESET generator, a power monitor and a time out counter for local and VMEbus accesses completes the board.

11. The Floating Point Co-Processor
The 68881 Floating Point Co-Processor (installed only on CPU-6VB) is a full implementation of the IEEE Standard 754 for Floating Point Arithmetic (Draft 10.0).
A set of 8 general Floating Point Data Registers, supporting full 80-bit extended precision are available for arithmetic operations such as:
- Add
- Subtract
- Multiply
- Divide
- Compare
- Scale Exponent
- Modulo
- Conditional branches
- Absolute value
- Sine, cosine, hyperbolic sine and cosine
- Tangent, cotangent, hyperbolic tangent and contangent
- eEXP (x)
- eEXP (x-1)
- eEXP (xtract (4))
- 1n (x), 1n (x+1)
- log 10 (x), log 2 (x)
- 2 EXP (x), 10 EXP (x)
- Square root
- Conditional Trap (32)

The FPCP supports the following data types:
- Byte, Word and Long Integers
- Single, Double and Extended Precision Real Numbers
- Packed BCD String Real Numbers

12. Software Description
VMEPROM is an EPROM based real-time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM. VMEPROM is composed of the powerful PDOS real-time kernel and the PDOS file manager. Thus the package provides support of a highly sophisticated real-time kernel and an interface to floppy and hard disk drives.
The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition it includes a powerful line assembler and disassembler for the 68000/68010.

VMEPROM features:
- Real-Time Multitasking Kernel supporting up to 64 tasks.
- File Management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Line assembler/disassembler with full support of all 68000/68010 instructions.
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify.
- S-record up-/downloading from any port defined in the system.
- Disk support for RAM-disk, floppy and winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. VMEPROM also allows disk formatting and initialisation.
- Serial I/O support for up to two SIO-2 or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full Screen Editor.
- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.

12.1 Description of the User Interface of VMEPROM
The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple command lines may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The Command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

12.2 Description of the Kernel Functions
The kernel of VMEPROM is written in 680 x 0 assembly language for fast and efficient execution. It provides multitasking, system clock, event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously.
Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

12.3 Description of the File Manager Functions
The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

12.4 Supported VMEbus Hardware
Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards and one disk controller.
In addition, EPROM programming is supported by VMEPROM utilising the SYS68K/RR-2/3 board family.

12.5 Target System Support
VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 40 Kbytes. Small romable applications can be put in EPROMS easily without the overhead of the user interface.

12.6 Development Systems
Currently either one of the FORCE PDOS* or UNIX System V* development stations may be used for software development for VMEPROM.
Compilers, Assemblers, and Libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.

12.7 Licensing
No license is required for VMEPROM. VMEPROM is delivered free of charge and is already installed on every CPU-6 board.
VMEPROM will be available on the CPU-6 family in Q4/87.

Specification of the SYS68K/CPU-6 Products

Microprocessor:	68000, 8,0MHz CPU-6 68000, 12,5MHz CPU-6A 68010, 12,5MHz CPU-6VA 68010, 12,5MHz CPU-6VB
Floating Point Support:	68881 FPCP (12,5MHz) installed only on CPU-6VB
DRAM:	512 Kbyte dynamic RAM 0 Wait State at 8MHz 1 Wait State at 12,5MHz Distributed Hardware Refresh
EPROM:	256 Kbyte for the SYSTEM Area 32 – 512 Kbyte for the USER Area
Serial I/O:	3 RS232 interfaces built with 6850 devices (ACIA) Strap selectable baud rate from 110-19200 baud Strap selectable I/O signal assignment to the 3 25-pin D-Sub Connectors.
Parallel I/O:	68230 PI/T with 24 I/O signals connected to P2 connector
Timer:	24-bit timer included in the PI/T
Real Time Clock:	58167 RTC with on-board battery back-up
Interrupts:	All on-board devices are capable of generating interrupts to the CPU on a fixed IRQ level. Local interrupts do not cause a VMEbus request.
VMEbus Interface:	Jumper selectable VMEbus request level (0-3) Transfer Modes A16: D8, D16 A24: D8, D16 Interrupt Handler (1-7 stat.) Single Level Arbiter SYSCLK Driver Power Monitor RESET Generator Bus Release Options: ROBCLR, RAT
Firmware:	128 Kbyte of firmware (VMEPROM)
Power Requirements:	+ 5V/2.9A +12V/0.2A –12V/0.2A
Operating Temp. Storage Temp. Relative Humidity Board Dimensions	0 to 60 Degrees C –50 to +85 Degrees C 0–95 % (non-condensing) Double Eurocard 234 x 160mm (9.2 x 6.3")

Ordering Information

SYS 68K/CPU-6 Part No. 100601	68000 CPU Board (8MHz), 512 Kbyte DRAM including User's Manual
SYS68/CPU-6A Part No. 100602	68000 CPU Board (12,5MHz), 512 Kbyte DRAM including User's Manual
SYS68K/CPU-6VA Part No. 100610	68010 CPU Board (12,5MHz), 512 Kbyte DRAM including User's Manual
SYS68K/CPU-6VB Part No. 100611	68010 CPU Board (12,5MHz), 512 Kbyte DRAM including 68881 FPCP and User's Manual
SYS68K/CPU-6UM Part No. 800094	User's Manual for all CPU-6 products
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM User's Manual

32 Bit CPU Boards

FORCE Computers 32 bit CPU Board Introduction

The range of FORCE Computers 32 bit CPU boards is one of the most comprehensive and complete available today. Products for all your top end performance and versatile functionality needs are offered. State of the art technology enabling multiprocessing features. True continuous 68020 zero wait state performance at all commercially available frequencies. The cross pollination of the Intel World to the to the VMEbus with the CPU-386. Plus the ability to deliver as promissed with a relentless eye for quality. All these are features that have made FORCE Computers the market leaders in high performance CPU boards.

General Feature Overview

If you are considering a 32 bit CPU board, then it is clear that performance is of importance. When FORCE designed their family of 32 bit CPU boards then maximum performance was crucial in the specification of the product. No tradeoffs were made at the expense of performance.
The SYS68K/CPU-21 board is the first example of this design philosophy. The product is available as a two board set, one board containing the VMEbus interface, CPU and control logic and the second board containing the high speed static RAM. The two boards are connected via the FLME interface. The board set is available with 12.5 MHz, 16.67 MHz, 20 MHz and 25 MHz CPUs and with the 68881 floating point co-processor up to 20 MHz. The board supports continuous no wait state operation at all frequencies up to 25 MHz from up to 4 Mbyte of local static RAM. The board is also provided with a real time kernel installed as standard. Additionally, newly available is the SYS68K/CPU-29 which is totally software and hardware compatible with the CPU-21, with the exception that the maximum memory capacity is only 1 Mbyte. The CPU-29 is available on one board. For S/W compatible upgrades to the memory managed 68030 environment , FORCE Computers has again shown its commitment to their customers by producing the SYS68K/CPU-32. The board is fully s/w ompatible to the CPU-21 and the CPU-29. The CPU-21, the CPU-29 and the CPU-32 are the 32 bit performance standard.
The SYS68K/CPU-22 provides a complete multiprocessing package. The CPU-22 family has a VMX interface to provide the systems integrator with access a subsystem bus for local memory and peripheral extension. Features of the family include the 68020 processor running continuously without the insertion of wait states from the on board dual ported static RAM. Revolutionary inter processor communication facilities such as programmable single or group processor interrupts with automatic programmable vector generation. Intelligent programmable interrupt prioritisation. 30 Mbyte/sec DMA controller. Two serial I/O channels. On board real time kernel in EPROM. All provided as standard. The CPU-22 is the 32 bit multiprocessor solution.
SYS68K/CPU-25 offer a 32 bit memory managed environment that sets new standards in the microcomputer world. Running with a single wait state from up to 4 Mbyte of local memory through the PMMU (68851), the board provides the perfect base for performace applications that need memory protection. Application areas are multi user workstations and UNIX environments. The CPU-25 are the performance memory management solution.
If it's general purpose features that you want with your 32 bit processor board, then look no further than the SYS68K/CPU-26 family. The boards come with up to 4 Mbyte of dynamic RAM inducing only 1 wait state on the 68020 at 20 MHz. The boards also come with 4 serial I/O channels and a SCSIbus interface and a floppy interface. In addition, all the comprehensive multprocessing and DMA features offered by the CPU-22 are also offered by the CPU-26 family. The CPU-26 is the versatile solution.
For those systems integrators who have investments in Intel S/W and experience in Intel environments, FORCE Computers has the answer. The SYS80K/CPU-386 is the first implementation of the 80386 processor on the VMEbus. The board provides as standard 2 Mbyte of DRAM, 3 serial I/O channels, a full VMEbus interface with slot 1 functions and the facility for the insertion of the 80387 floating point co-processor. This board is the VMEbus-Intel solution.

32 Bit CPU Boards

FAMILY	CPU-20	CPU-21	CPU-22	CPU-24	CPU-25	CPU-26	CPU-29
Processor Type	Not recommended for new designs.	68020	68020	Not recommended for new designs.	68020	68020	68020
Frequency min.		12.5 MHz	16.7 MHz		16.7 MHz	16.7 MHz	12.5 MHz
Frequency max.		25.0 MHz	20.0 MHz		20.0 MHz	20.0 MHz	30.0 MHz
FPCP Type		68881	68882		68881	68882	68882
Frequency min.		12.5 MHz	16.7 MHz		16.7 MHz	16.7 MHz	12.5 MHz
Frequency max.		20.0 MHz	20.0 MHz		20.0 MHz	20.0 MHz	25.0 MHz
DMAC Frequency min.		–	16.7 MHz		–	16.7 MHz	–
DMAC Frequency max.		–	20.0 MHz		–	20.0 MHz	–
MMU Type		–	–		68851	–	–
RAM Type		SRAM	SRAM		SRAM	DRAM	SRAM
RAM Capacity min.		512 Kbyte	256 Kbyte		512 Kbyte	1 Mbyte	1 Mbyte
RAM Capacity max.		2 Mbyte	1 Mbyte		2 Mbyte	4 Mbyte	1 Mbyte
No. of Wait States		0	0		0	1	0
RAM Function		local	DPR		local	DPR	local
No. of EPROM Sockets		8	4		1	4	4
28 Pin Support		X	X		X	X	X
32 Pin Support		–	X		–	X	X
Max. Capacity		512 Kbyte	4 Mbyte		64 Kbyte	4 Mbyte	4 Mbyte
VMEPROM		X	X		–	X	X

FAMILY	CPU-20	CPU-21	CPU-22	CPU-24	CPU-25	CPU-26	CPU-29
Battery Backup-SRAM	Not recommended for new designs.	–	32 Kbyte	Not recommended for new designs.	–	32 Kbyte	–
Serial I/Os RS232 RS232 & RS422 Used Controller Chip		1 1 2 x 68561	1 1 68562		1 1 2 x 68561	1 3 2 x 68562	2 – 2 x 68561
Floppy Disk Interface SCSI Interface SCSI Transfer Speed		– – –	– – –		– – –	X X 4 Mbyte/s	– – –
FORCE Message Passing Channels		–	2		–	2	–
Location Monitors Single Level Arbiter		– X	16 X		– X	16 X	– X
FORCE Gate Array		–	FGA002		–	FGA002	FGA001
Timer 24 bit Timer 8 bit		1 –	2 4		1 –	2 4	2 –
VMXbus Interface VSB Interface		X –	X –		– –	– –	– X
No. of Used Slots		2	1		2	1	1
Operating Temp. min. max.		0°C 50°C	0°C 50°C		0°C 50°C	0°C 50°C	0°C 50°C
Detailed Description on Page:		93	105		123	131	149

32 Bit CPU Boards

FAMILY		CPU-30	CPU-31	CPU-32	CPU-386	CPU-386A
Processor Type		68030	68030	68030	80386	80386
Frequency	min.	16.7 MHz	16.7 MHz	12.5 MHz	16.7 MHz	16.7 MHz
	max.	20.0 MHz	20.0 MHz	33.0 MHz	16.7 MHz	16.7 MHz
FPCP Type		68882	68882	68882	–	80387
Frequency	min.	16.7 MHz	16.7 MHz	12.5 MHz	–	16.7 MHz
	max.	20.0 MHz	20.0 MHz	25.0 MHz	–	16.7 MHz
DMAC Frequency	min.	16.7 MHz	16.7 MHz	–	–	–
	max.	20.0 MHz	20.0 MHz	–	–	–
On Chip MMU		X	X	X	X	X
RAM Type		DRAM	SRAM	SRAM	DRAM	DRAM
RAM Capacity	min.	1 Mbyte	1 Mbyte	1 Mbyte	2 Mbyte	2 Mbyte
	max.	4 Mbyte	1 Mbyte	1 Mbyte	8 Mbyte	8 Mbyte
No. of Wait States		1	0	0	0	0
RAM Function		DPR	DPR	local	local	local
No. of EPROM Sockets		4	4	4	4	4
28 Pin Support		X	X	X	X	X
32 Pin Support		X	X	X	–	–
Max. Capacity		4 Mbyte	4 Mbyte	4 Mbyte	256 Kbyte	256 Kbyte
FORCEbug		–	–	–	X	X
VMEPROM		X	X	X	–	–

FAMILY	CPU-30	CPU-31	CPU-32	CPU-386	CPU-386A
Battery Backup SRAM	32 Kbyte	32 Kbyte	–	–	–
Serial I/Os RS232 RS232 & RS422 Used Controller Chip	1 3 68562	1 1 68562	2 – 2 x 68561	3 – 68562	3 – 68562
Floppy Disk Interface SCSI Interface SCSI Transfer Speed	X X 4 Mbyte/s	– – –	– – –	– – –	– – –
FORCE Message Passing Channels	2	2	–	–	–
Location Monitors Single Level Arbiter	16 X	16 X	– X	– X	– X
FORCE Gate Array	FGA002	FGA002	FGA001	–	–
Timer 24 bit Timer 8 bit	2 4	2 4	2 –	– 3 + 2	– 3 + 2
VMXbus Interface VSB Interface	– –	– X	– X	– –	– –
No. of Used Slots	1	1	1	1	1
Operating Temp. min. max.	0°C 50°C	0°C 50°C	0°C 50°C	0°C 50°C	0°C 50°C
Detailed Description on Page:	161	179	197	209	209

System 68000
SYS68K/FMB

Force Message Broadcast on the VMEbus

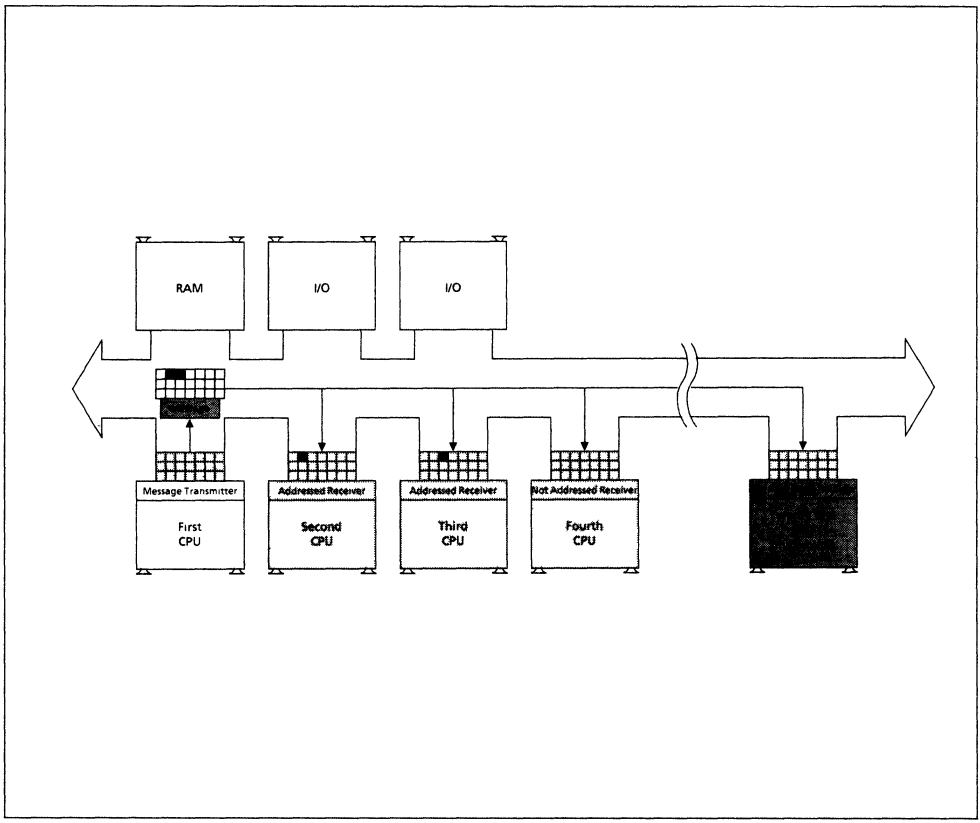
1. General Description

The FORCE Message Broadcast (FMB) is a message broadcasting utility on the VMEbus allowing messages to be sent across the VMEbus to any CPU board or to intelligent controllers.
A message of 8 bit can be sent to each of the participating slaves on the VMEbus.

1.1 The FMB Implementation

The FMB allows a user to send user defined 8 bit wide messages to any board which supports the FMB function in a single standard VMEbus write cycle.
The FMB receiver contains at minimum an 8 byte deep FIFO to store these messages. The FMB receiver is capable of interrupting the local CPU on a software programmable level and supplying a unique interrupt vector. Two fully independent FMB channels offer different prioritized messages across the VMEbus.
The initiator defines to which slave boards the message is sent via the access address. A unique access address for each VMEbus slot (21) assures that the message can be sent to each of the installed boards in a single cycle.
The FMB is installed in the FORCE Gate Array FGA-002 assuring compatibility to all FORCE Computers products.
A typical multiprocesor configuration is outlined in the following figure describing how the FMB can be used to distribute different messages to the various installed boards.

BLOCK DIAGRAM FORCE MESSAGE BROADCAST



2. The Message Broadcast Concept

Message broadcasting is necessary in multiprocessor configurations to synchronize multiple CPUs and to exchange/share status information.
A multiprocessor configuration consisting of for example 10 CPU boards each working on a dedicated task needs to be controlled and triggered if data is coming in. This data has to be processed and all CPU boards have to signal completion to all other boards.
The VMEbus specification does not define a standardized way of synchronizing these multiple CPUs so that for each application, a system design engineer has to define a message broadcasting technique typically using the VMEbus interrupt structure. The FMB provides an installed mechanism to allow message broadcasting without VMEbus interrupt overhead.
With the availability of FMB, there now exist three possible methods for multiple CPUs to communicate effectively in a multiprocessing VMEbus environment. VMEbus interrupts, location monitors and FMB. The merits and drawbacks of each method is described below.

2.1 The VMEbus IRQ Structure

Seven different Interrupt Request signals are defined in the VMEbus specification. Each of these seven IRQs can interrupt one interrupt handler. An interrupt handler can be an intelligent I/O controller or a CPU board.
Normally, one or more IRQ level(s) per interrupt handler can be assigned (static IRQ handler).
This allows the interruption of a maximum of 7 different CPU boards at a time.
Each interrupt handler needed to fetch the interrupt vector from the VMEbus requires the request of bus mastership. For 7 interrupt requests being asserted at the same time 7 IRQ vectors need to be fetched. Typically the IRQ daisy chain needs around 200 to 800 ns per cycle to be completed. The bus request/bus grant daisy chain takes approximately 100 ns per IACK cycle and the time overhead to perform the cycle on each CPU board requires additional 100 ns. Adding all these together (700 ns as an average) and multiplying by 7 results in a minimum time of 7,9 us to send all of these 7 boards an interrupt.
These are ideal conditions while the "real" time required to interrupt all CPU boards is also influenced by the application. This means that for example each CPU board does not release bus mastership after fetching the interrupt vector because transactions on the VMEbus are required. This application depended overhead may result in a much longer synchronization time, maybe up to 10 to 20 us.
This means that the time between the first CPU getting its IRQ vector and the 7th CPU may reach 20 us. This may result in a timing problem of the Real Time Synchronization capability of the whole system.

2.2 The Location Monitor

A different technique to synchronize multiple CPU boards is the usage of location monitors on each CPU board to be synchronized. The location monitor has a unique global VMEbus address and decodes the access address of VMEbus cycles and interrupts the local CPU on the defined IRQ level, when an address match occurs.
This technique allows the interruption of more than 7 different CPU boards on the VMEbus if each of the CPU boards contains an independent location monitor.
To synchronize for example 10 different CPU boards on the VMEbus, 10 VMEbus access cycles have to be performed as each location monitor has to be addressed separately. Assuming that each VMEbus access cycle takes approximately 300 ns including the response time of the slave board and adding 200ns for fetching and executing the next instruction then 500 ns per cycle are needed. This results in a minimum time of 5.0 us required to interrupt 10 different CPU boards.
This is the ideal timing assuming that the board which triggers all other boards does not give up VMEbus mastership.
The maximum time between the first and tenth interrupted CPU board may reach 5 to 10 us depending on the application.
In high end multiprocessor applications this time may reach 20 to 30 us using 16 or more CPU boards.

2.3 The FORCE Message Broadcast

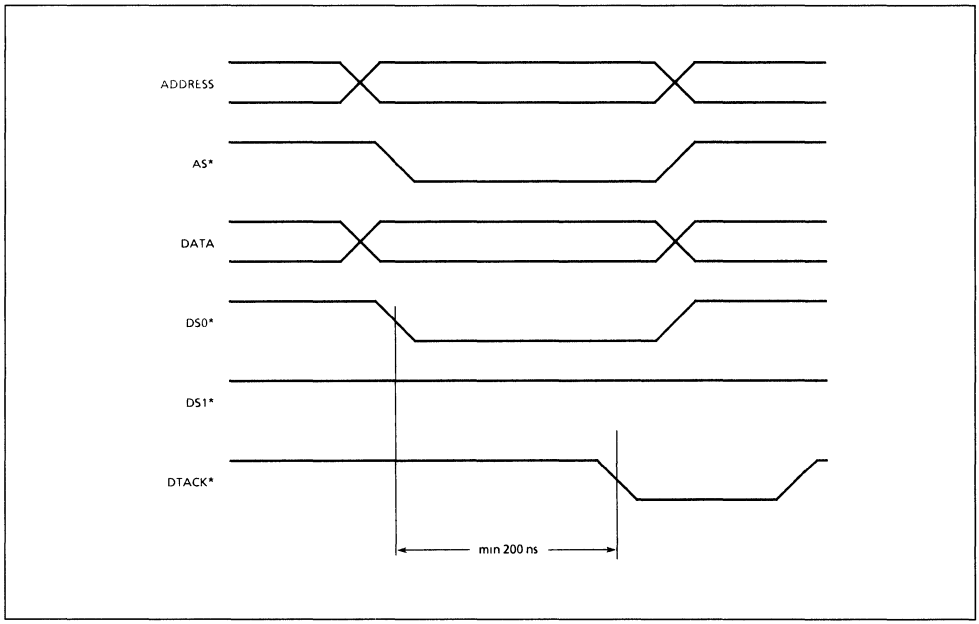
The FORCE Message Broadcast (FMB) allows the interrupt of all, some or only one CPU board supporting of the FMB feature in only one cycle which is performed in less than 330 ns including the VMEbus protocol.
Using the location monitor technique is at a minimum 10 times slower in synchronizing the different CPUs in a system not using the FMB mechanism.
In addition, the FMB allows the storage of an 8 bit message in an 8 byte deep FIFO. This information is user defined and therefore adaptable to the application needs. The location monitors normally do not store any information.
If a message should be stored using the Location Monitor technique a Dual Ported Memory is required resulting in a doubled amount of time needed to sychronize the CPU boards.

3. The VMEbus Interface

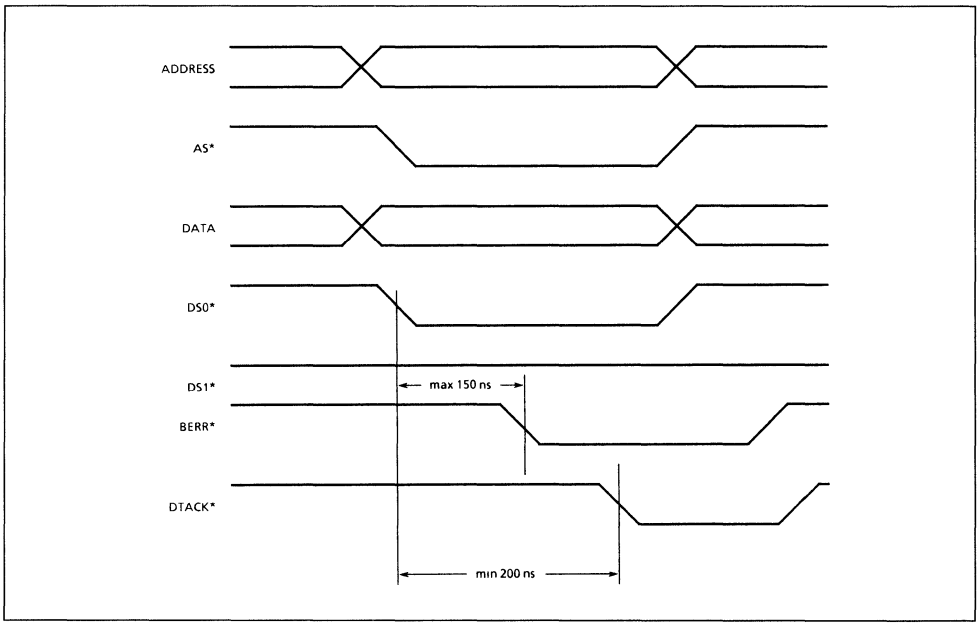
The specification of the VMEbus defines two modules, the master and the slave. A master holding bus mastership can initiate data transfers on the VMEbus by reading or writing data from/to the slave module.
The current revision of the VMEbus specification does not forbid write cycles to multiple slave modules because of its fully asynchronous structure and lack of handshake signals. FORCE Computers defines such a cycle by synchronizing all participating slave modules on the falling edges of the Data and Address Strobe signals.
The principal data transfer is a standard write transfer which is terminated by asserting a DTACK* or BERR* to the master board.
In the case when the BERR* signal is asserted before DTACK*, the cycle was not performed correctly.
If the DTACK* signal is asserted before BERR*, the cycle has been performed correctly.
The timing diagram of the different cycles shows the principal of operation.

The slave which detects that the cycle cannot be performed has to drive BERR* to the VMEbus to signal the master that the cycle has not been successfully executed. All other participating slaves which perform the cycle have to drive the DTACK* signal to the VMEbus informing the master CPU that the data pattern sent to the slave module has been stored correctly.
The slave module(s) detecting that the cycle cannot be performed correctly must assert BERR* at latest 150 ns after the data strobe has been driven active to insure that the master receives the BERR* before DTACK* from another participating slave.
The participating slave(s) MUST NOT drive their DTACK*s valid before 200 ns after the data strobe has been asserted. This timing insures compatibility with the current available CPUs like the 68000, 68010, 68020 and 68030.
This assures that the master receives BERR* before DTACK*. Indeed 3 participating slave modules may drive DTACK* active while one module may drive BERR*.
The initiator of a FMB cycle can be each standard VMEbus board capable of driving extended accesses (A32 mode) independent of the FMB slave function.

Timing Diagram A: Correct Operation



Timing Diagram B: Incorrect Operation



4. The Local Bus Interface

The two fully independent FMB channels installed in FGA-002 are able to interrupt the local CPU on a software programmable level. The interrupt vector is supplied on a local interrupt acknowledge cycle from the Gate Array to the local CPU without requesting or using the VMEbus.
The message stored in the 8 byte deep FIFOs can be read from the local CPU out of the Gate Array through two fully independent data registers.
A status register shows if messages are stored in the FIFO or if no message is received.
In case that the FIFO has an overflow, an error bit is set in the status register.
To recover from FIFO overflow, the control register allows the reset of the FIFO and operations may be started again.

5. Usage of the FMB

This paragraph lists some typical applications where the FMB is useful.

5.1 Multiprocessor Synchronization

If a high end multiprocessor system has a need for synchronization of time critical tasks, the FMB may be used to interrupt all CPU boards or only a few of them at the same time.
This allows a reduction in the time between different CPU boards being interrupted and therefore eliminates run time differences.

Example: A20 processor system not using the FMB technique for synchronization may have a time gap between the first and last interrupt acknowledge cycle of the different interrupted CPU boards of at least 30 us. These 30 us can be saved by using the FMB.

5.2 Multiprocessor Status Exchange

A standard multiprocessor system has to have a control mechanism to detect if a board does not perform well or if the board is halted.
Normally, status bits in global memory are set and one board has to poll this function bit. After reading this bit it has to be reset to ensure that the CPU to be checked is able to and has changed that bit. This technique uses a significant amount of the VMEbus bandwidth, because both the board which is observed and the observer have to check and modify the bits in global memory.
The FMB allows reduction of overhead because only the observed board has to initiate an FMB cycle and store in the observer's FMB FIFO the message that board X is functioning correctly. This function allows the observer(s) to wait a defined time period and set a watchdog timer to initiate a local interrupt if the observed board(s) has not/ have not sent a message within the time period.
The observer is no longer limited to only one CPU board because this message can be sent to all CPU boards installed in the system to make them aware that the sender is active.
This allows easy installation of a fully virtual watchdog function.

5.3 Fault Tolerant Configurations

The FMB may be used for message broadcasting in a fault tolerant system built with VMEbus based boards. The FMB can inform each CPU board about the current status of each other board to detect failures on non responding and/or on responding but not current functioning modules.

5.4 Triggering of Dedicated Processors

The FMB allows the user to send a start or a stop message to a multiple CPU board to control their program flow. The message or data pattern can inform these CPUs to, for example, abort the current task and start execution of the next task.

5.5 Enhanced Real Time Capabilities

The FMB allows a significant increase in the Real Time capability of a multiprocessor system because the time between the interrupts being acknowledged by the different CPUs can be reduced to almost 1 us (in reality). This allows the user to, for example, send 10 installed CPU boards the same message (first byte) and than a number of data bytes which are needed to perform an action.

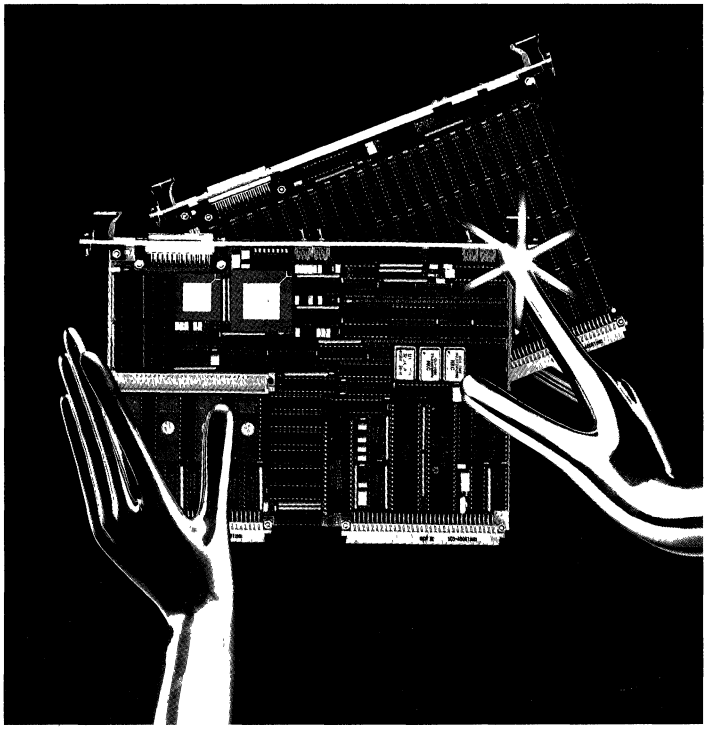
6. Installation of the FMB

The FMB is installed on various FORCE Computers CPU boards as listed below. These boards may both be FMB slaves and/or FMB masters.

SYS68K/CPU-22	68020 CPU board with FPCP, constant zero wait state Dual Ported RAM and DMA
SYS68K/CPU-26	68020 CPU board with FPCP, 4 Mbyte Dual Ported DRAM, DMA, SCSI, FDC and 4 serial I/Os
SYS68K/CPU-30	68030 CPU board with FPCP, 4 Mbyte Dual Ported DRAM, DMA, SCSI, FDC and 4 serial I/Os
SYS68K/CPU-31	68030 CPU board with FPCP, constant zero wait state Dual Ported RAM, DMA and VSB interface

CPU boards as listed below can only initiate a FMB cycle as a master.

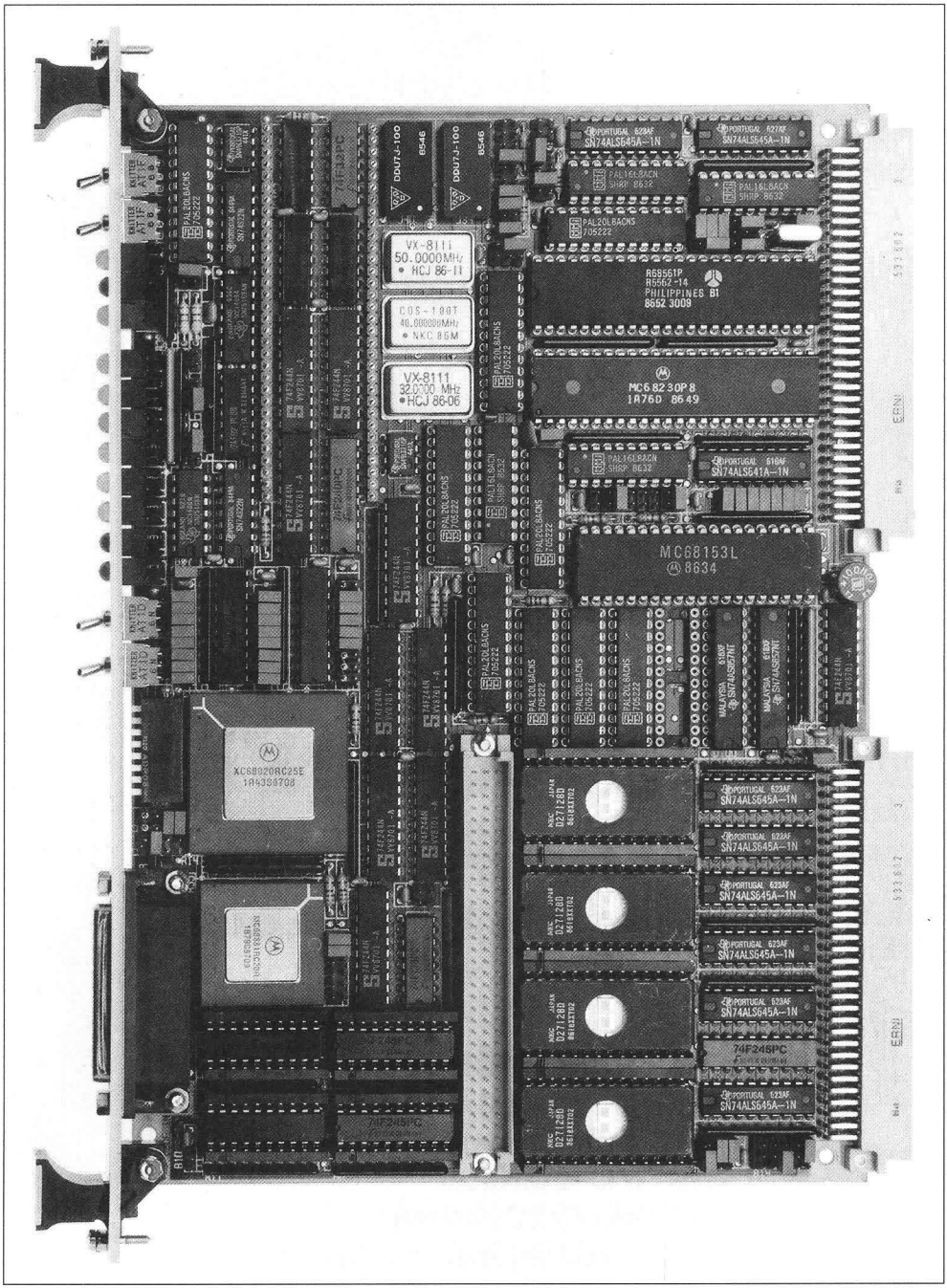
SYS68K/CPU-21	68020 CPU board with FPCP, constant zero wait state SRAM up to 25 MHz clock frequency
SYS68K/CPU-25	68020 CPU board with FPCP, Memory Management (68851 PMMU) and 512 Kbyte static RAM
SYS68K/CPU-29	68020 CPU board with up to 30 MHz clock frequency, FPCP, 1 Mbyte zero wait state SRAM and VSB interface
SYS68K/CPU-32	68030 CPU board with up to 30 MHz clock frequency, FPCP 1 Mbyte zero wait state SRAM and VSB interface



System 68000 VME SYS68K/CPU-21

68020 Real Time Multi Processor CPU Board

- No Wait State 25 MHz 68020
- 512 K/2 Mbyte Static RAM
- 68881 Floating Point Co-Processor
- 2 Serial I/O Interfaces
- 32 bit wide EPROM Areas
- VMEbus and VMXbus Interface

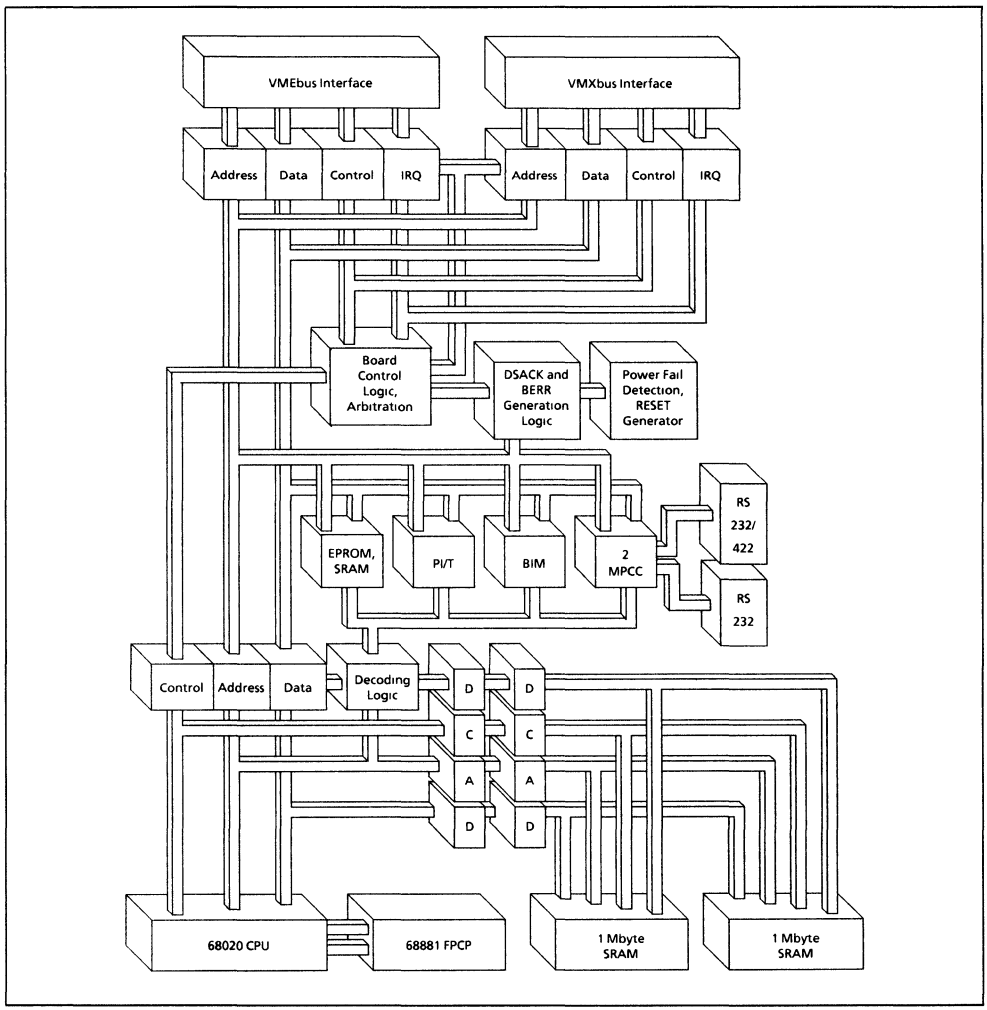

VX-8111
50.0000MHz
• HCJ 86-11
COS-100T
40.000000MHz
• NKC 86M
VX-8111
32.0000 MHz
•HCJ 86-06
R65561P
R5562-14
PHILIPPINES B1
8652 3009
MC68230P8
1A76D 8649
MC68153L
8634
XC68020RC25E
1A4338703
SN74ALS645A-1N
74F245PC

General Description

The SYS68K/CPU-21 is an ultra high speed CPU board designed around the true 32 bit 68020 CPU. The board is built for the VMEbus/IEEE 1014 standard environment and offers 8 sockets for JEDEC compatible devices (EPROMs or SRAMs), two serial ports, a local control device as well as the advanced floating point co-processor 68881 (CPU-21).
A static RAM (512 Kbyte) is installed on the CPU-21 to provide zero wait state operation at 12.5 to 25 MHz on read and write cycles.

The SYS68K/CPU-21A with its 20 MHz CPU runs without the insertion of wait states out of 512 Kbyte SRAM and the SYS68K/CPU-21B with its 25 MHz CPU runs also without the insertion of wait states out of 512 Kbyte SRAM.
A powerful real time multitasking monitor called VMEPROM is included. It features over 50 commands for debugging, task management, file management 68020/68881 line assembler/disassembler.
A photo of the SYS68K/CPU-21 is shown on the left page while the block diagram of the SYS68K/CPU-21Y is shown below.

BLOCK DIAGRAM OF THE SYS68K/CPU-21Y



Features of the SYS68K/CPU-21

- 68020 CPU (12.5 MHz) on CPU-21S
  68020 CPU (16.7 MHz) on CPU-21
  68020 CPU (20.0 MHz) on CPU-21A
  68020 CPU (25.0 MHz) on CPU-21B
- 68881 Floating Point Co-Processor
- 68561 Multi-Protocol Communications Controllers for Serial I/O (one RS232 and one RS232/RS422 compatible interface)
- 68230 Parallel Interface and Timer for local control, interrupt level control and timer function
- 68153 Bus Interrupter Module for all local interrupts
- 512 Kbyte or 2 Mbyte of zero wait state static RAM via the FLME interface (jumper selectable access address)
- 4 Sockets for EPROMs (32 bit wide) for 8K x 8 to 64K x 8 organized devices
- 4 stacked DIP sockets for EPROMs/SRAMs (32 bit wide) for 8K to 64K x 8/8K x 8 to 32K x 8 devices. The maximum EPROM capacity is 512 Kbyte by using eight 27512 devices, the maximum SRAM capacity is 128 Kbyte by using four 32K x 8 SRAMs
- Fully buffered local address and data bus
- VMX Primary Master Interface (32 bit)
- VME IEEE 1014 interface (VMEbus) supporting unaligned transfers (32 bit)
- Single level bus arbiter
- Software selectable bus release functions (6)
- Interrupt handler (1-7 static)
- Bus Timer for BERR generation on local bus, VME IEEE 1014 bus and VMXbus
- Power Fail Detector and RESET generator
- RESET and TEST switch
- RUN/HALT switch
- CACHE enable/disable switch
- RUN/HALT/Bus Master/SRAM Access and Wait State indication LEDs
- Powerful real time monitor/debugger, called VMEPROM, included.

1.0 Hardware Description

1.1 The 68020 CPU

The 68020 with its 32 bit address and data bus is implemented on the board to take full advantage of the 32 bit VME IEEE 1014 bus structure.
A cache of 256 words is installed on the CPU to reduce bus overhead by eliminating op-code fetches. A CACHE switch is installed on the front panel to provide easy software debugging through enabled or disabled CACHE via hardware (the switch overrides the software commands).

The 68020 offers additional instructions to the 68010 such as string manipulations, extended branches over the whole 4 Gbyte addressing space, check and set instructions as well as enhanced exception handling (3rd stack pointer for interrupts) etc.
Dynamic bus sizing (8, 16 or 32 bit ports are defined) and the 32 bit structure offers maximum throughput in conjunction with the 32 bit wide memory such as the connectable static RAM boards which provide zero wait state operation on read and write cycles (CPU clock frequency is 16.7 MHz). In this case 2-3 MIPs computing power are available.
The CPU communicates to the local I/O and memory through a full buffered address and data bus.

1.2 The Floating Point Co-Processor

The SYS68K/CPU-21 is fitted with a 68881 FPCP. The clock frequency of the CPU and the FPCP are identical. The FPCP conforms to the IEEE Floating Point standard 10.0.
Easy Floating Point operation control to the Co-Processor is provided because the intercommunication between the CPU and the FPCP is built in silicon.
An internal register set of 8 general purpose registers (80 bit wide) yields fast execution times.
The performance of the FPCP can be easily upgraded by changing the quartz oscillator frequency (as faster versions become available).

Features of the FPCP:

- 8 General purpose Registers (80 bit, 64 bit Mantissa, 15 bit Exponent and one Sign bit)
- 67 bit on chip ALU
- 67 bit barrel shifter
- 46 Instruction Types including 35 Arithmetic Operations
- IEEE P754 standard (draft 10.0)
- Full support of trigonometrical and logarithmic functions such as:
  sine and cosine
  tangent and cotangent
  Hyperbolic functions (tangent, arc tangent, sine and cosine)
  Logarithmic functions (4)
  Square Root and Exponential functions (4)

1.3 The Serial I/O Channels

The SYS68K/CPU-21 board contains two Multi Protocol Communications Controllers (68561 MPCC) which support the following protocols:

- Character Oriented Protocols
  BSC, DDCMP, X3.28, X.21
  ECMA16
- Synchronous Bit Oriented Protocols
  SDLC, HDLC, X.25
- Even, Odd or no Parity check
- CRC check selectable
- Eight character receiver and buffer register
- Software Programmable Baud Rate from 110 to 38400 Baud
- DC data Rate up to 4 Mbit/s

An RS232 compatible interface (first port) is installed on the board to provide direct connection to standard terminals. The user can select between a RS232 and a RS422 compatible interface on the 2nd serial port.
The I/O signal assignment of the 4 input and output signals per port to the two 25 pin D-sub connectors on the front panel is jumper selectable.
Each MPCC is able to issue an interrupt on a software programmable level to the CPU. The interrupt vectors are also software programmable.

1.4 The Local Control PI/T

A Parallel Interface and Timer Module (68230 PI/T) with 8 MHz clock frequency is installed on the board to provide timer function as well as local control.
All interrupt levels of the CPU (1 to 7) can be separately enabled or disabled via port B of the PI/T.
Eight DIP-switches for data input and configuration selection (memory size, baud rate etc.) are installed on the front panel and readable via port A of the PI/T.
The SYSFAIL and ACFAIL signal of the VMEbus is routed to the handshake pins of the PI/T to generate an interrupt or exception. The interrupt request signal of the VMXbus is also routed to one handshake input to generate an interrupt to the 68020.
The availability of the Floating Point Co-Processor can be sensed through the PI/T.
The bus release functions of the VMEbus (ROR, RAT, RATAR, RATBCLR, RORAT, RORRAT) are SOFTWARE selectable through port C of the PI/T.
The PI/T includes a 24 bit programmable timer with 5 bit prescaler. The Timer can be used for time measurement or as a time base for operating systems. The Timer as well as the signals, connected to the handshake port can issue an interrupt to the CPU on a software programmable level. The interrupt vector is also software programmable.

1.5 The Local Interrupt Handler

A Bus Interrupter Module (68153 BIM) is installed on the board to provide a software programmable interrupt level for each of the on-board interrupt sources.

Local Interrupt Sources

Interrupter	Device
TEST SWITCH	Switch
Serial Channels	MPCC
Timer	PI/T
ACFAIL	PI/T
SYSFAIL	PI/T
VMX-IRQ	PI/T

The CPU-21 will only request VMEbus mastership if the access address is within the VMEbus range or if a VMEbus interrupt has to be acknowledged.

1.6 Local Memory

The local memory consists of 8 sockets for JEDEC compatible devices, 4 SYSTEM EPROM sockets as well as 4 USER sockets. The memory organization is 32 bit wide for the SYSTEM and the USER area to provide maximum throughput of the 68020 CPU.

The following device types are supported:

Device Type	Organization	SYSTEM Area capacity	USER Area capacity	TOTAL capacity
2764	8K x 8	32 Kbyte	32 Kbyte	64 Kbyte
27128	16K x 8	64 Kbyte	64 Kbyte	128 Kbyte
27256	32K x 8	128 Kbyte	128 Kbyte	256 Kbyte
27512	64K x 8	256 Kbyte	256 Kbyte	512 Kbyte
6264	8K x 8	–	32 Kbyte	32 Kbyte
62256	32K x 8	–	128 Kbyte	128Kbyte

The board is fitted with the VMEPROM (in 4 EPROMs 27256) and 4 SRAMs 6264 for standalone operations. If the exception vectors can be stored in another address (i.e. $0) the USER area can be used for additional EPROMs.
The access time of the SYSTEM and the USER area are independently jumper selectable between 100 and 400 ns.

1.7 The Local Memory Extension

The CPU-21 contains a local extension (FLME) interface (32 bit wide) for ultra high speed static RAM connection. This fully buffered local memory extension bus is connected to the 3rd 96 pin DIN connector in the middle of the board.
The access address and the capacity of the RAM area is jumper selectable in the whole 4 Gbyte address space. All of the decoding and driver/receiver logic is installed on the CPU-21 board.
512 Kbyte of SRAMs is installed on the CPU-21 and 2 Mbyte is installed on the SYS68K/CPU-21Y series of boards.
The access time of 35ns allows to operate at 25 MHz CPU clock frequency without insertion of any wait states. The FLME Memory can be extended by using a SRAM-22 board.
CPU-21A memory extention is supported by the SRAM-22A and for CPU-21B memory extension is supported by the SRAM-22B.

1.8 The Local Control

A local RESET generator is installed on the board to provide a RESET to all of the on-board devices. The RESET is generated, if the Power Fail detector detects a supply voltage of lower than 4.75V, if the RESET switch on the front panel is pushed or if the SYSRESET from the VMEbus is active.
A TEST switch is installed to provide self test or application dependent interrupt handling. The DEBUGGER of the CPU-21 supports the TEST switch as level 7 interrupt (Software Abort).
Additionally a RUN/HALT function switch is installed for easy multi-processor software debugging.
RUN/HALT, VME Bus Master, Local RAM extension access and EPROM access are shown on the front panel through LEDs.
6 LEDs on the front panel show the number of wait states inserted by the 68020 CPU.

1.9 The VMEbus Interface

A full 32 bit VMEbus/IEEE 1014 standard interface is implemented on the CPU-21 to communicate to global RAM – and I/O cards.
The 4 Gbyte address space of the 68020 is fully decoded and 8, 16, 24 and 32 bit data transfers are supported as listed below:

Transfer Type	D31 – D24	D23 – D16	D15 – D8	D7 – D0	Note
Byte			x		
				x	
Word			x	x	
Long-Word	x	x	x	x	
Unaligned	x	x	x		1
Transfers		x	x		1
		x	x	x	1
Read Modify Write				x	1
			x	x	1
	x	x	x	x	1

Note 1: According to the VMEbus specification Rev.C and the IEEE 1014 specification.

The support of the unaligned transfer allows the 68020 CPU to operate with its maximum throughput because a 16 bit transfer to an odd address is now legal and needs only 1 bus cycle. If the unaligned transfer is not supported, 2 bus cycles are needed because the single transfer has to be split into 2 cycles.
To enable the support of 16 bit memory boards, the size of the VMEbus address space is programmable (16 or 32 bit wide) via the PI/T.
A single level arbiter is installed on the CPU-20/21 to build small environments without the need for a special system controller. The arbitration level on which the board requests the VMEbus mastership is jumper selectable to level 0, 1, 2, and 3.
Powerful software programmable bus release functions are installed on the board such as:

a) RAT	Release after Time-Out
b) RATAR	Release after Time-Out if Request is pending
c) RATBCLR	Release after Time-Out if bus clear is active
d) ROR	Release on Request
e) RORAT	Release on Request after Time-Out
f) RORRAT	Release on Request and Release after Time-Out

The VMEbus Interrupt Request Signals (IRQ 1-7) are jumper selectable to provide full multiprocessing.
A bus timer for BERR generation during VMEbus accesses is installed. Additionally a Power FAIL detector and a SYSRESET generator is provided on the board.

1.10 The VMXbus Interface

A full 32 bit VMX Interface is installed to allow high end configurations for multi-processing applications as shown below:
The Primary Master Interface allows the connection of up to 5 other VMXbus boards which may be RAM boards, special I/O boards as well as proprietary boards (i.e. Graphics Controller).
The 32 bit data path (D32NA) allows the following transfer types:

WRT	Write Cycles
RD	Read Cycles
RMW	Read Modify Write Cycles
ADDR	Address Only Cycles

Aligned and Non-Aligned Transfers are supported from the CPU-21.
The Slave Boards may respond to the CPU as follows:

SD	Standard Data
SDE	Standard Data Error Response
LD	Late Data Response
LDE	Late Data Error Response

The VMXbus Interrupt request is supported and handled through the on board PI/T. The IRQ level and the IRQ vector are software programmable.

2.0 Software Description

VMEPROM is an EPROM based real-time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM. VMEPROM is composed of the powerful PDOS real-time kernel and the PDOS file manager. Thus the package provides support of a highly sophisticated real-time kernel and an interface to floppy and hard disk drives.
The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition it includes a powerful line assembler and disassembler for the 68020 and the 68881.

2.1 Features of the VMEPROM

- Real-Time Multitasking Kernel supporting up to 64 tasks.
- File Management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Line assembler/disassembler with full support of all 68020/68881 instructions.
- Over 20 commands for program bedugging, including breakpoints, tracing, processor register display and modify.
- S-record up/downloading from any port defined in the system.
- Disk support for RAM-disk, floppy and winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. VMEPROM also allows disk formatting and initialisation.
- Serial I/O support for up to two SIO-2 or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full Screen Editor.
- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.

2.2 Description of the User Interface of VMEPROM

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple command lines may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The Command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

2.3 Description of the Kernel Functions

The kernel of VMEPROM is written in 680 x 0 assembly language for fast and efficient execution. It provides multitasking, system clock, event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously.
Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

2.4 Description of the File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

2.5 Supported VMEbus Hardware

Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards, and one disk controller.
In addition, EPROM programming is supported by VMEPROM utilising the SYS68K/RR-2/3 board family.

2.6 Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 40 Kbytes. Small romable applications can be put in EPROMS easily without the overhead of the user interface.

2.7 Development Systems

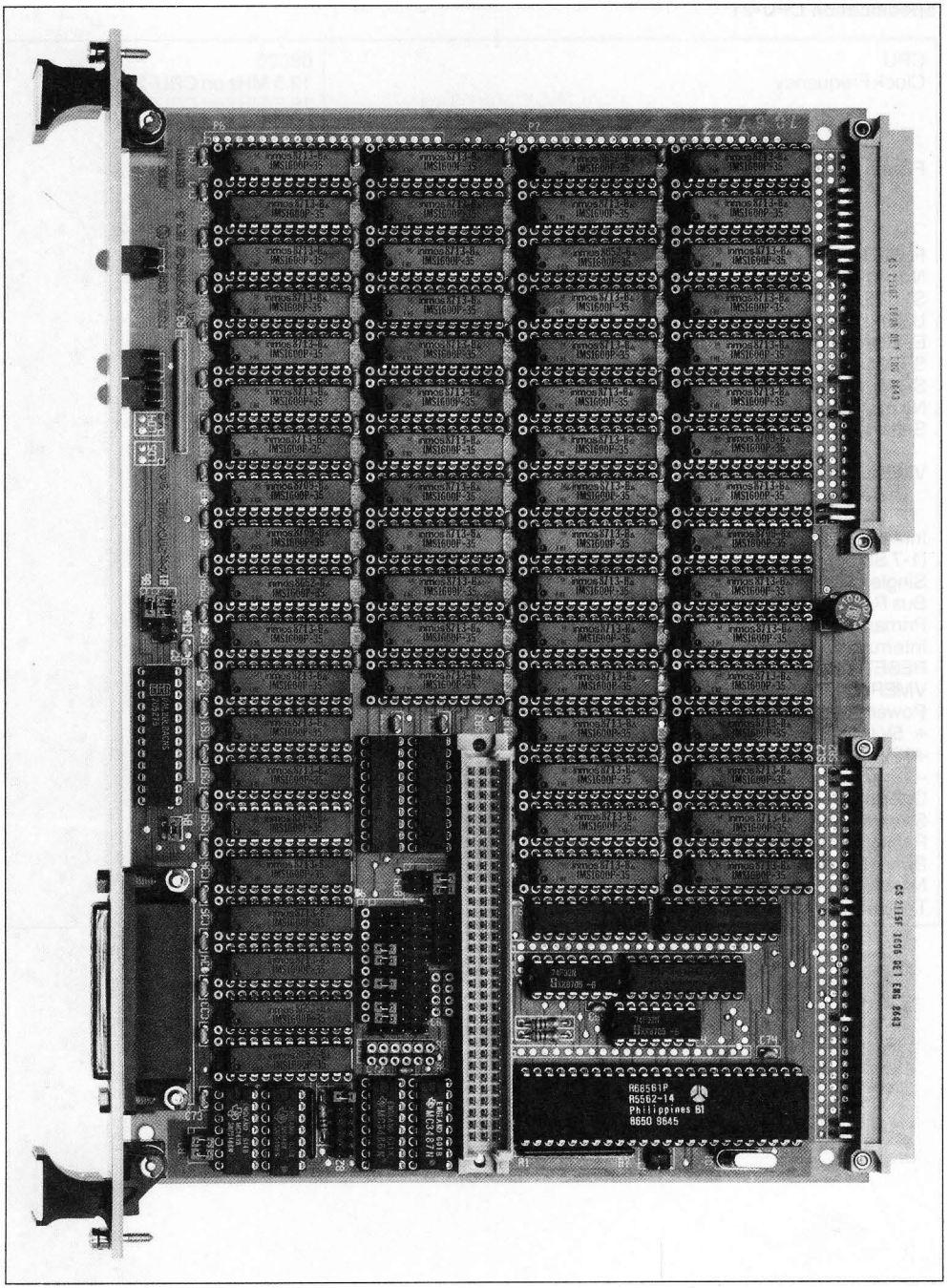
Currently either one of the FORCE PDOS* or UNIX System V* development stations may be used for software development for VMEPROM.
Compilers, Assemblers, and Libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.

2.8 Licensing

No license is required for VMEPROM. VMEPROM is delivered free of charge with every CPU-21 board.

Specification CPU-21

CPU	68020
Clock Frequency	12.5 MHz on CPU-21S 16.7 MHz on CPU-21 20.0 MHz on CPU-21A 25.0 MHz on CPU-21B
Floating Point Co-processor	12.5 MHz on CPU-21S 16.7 MHz on CPU-21 20.0 MHz on CPU-21A 20.0 MHz on CPU-21B
FLME Memory	512 Kbyte
No of Wait States	0
SYSTEM EPROM sockets	4
USER EPROM sockets	4
EPROM capacity (max)	512 Kbyte
SRAM capacity (max)	128 Kbyte
SRAM capacity at delivery for VMEPROM	32 Kbyte
No of Wait States	2
Serial I/O Interfaces	1 RS232 1 RS232/RS422
VMEbus Interface IEEE 1014	
A32, A24, A16	x
D32, D24, D16, D8	x
Interrupt Handler	
(1-7 Stat)	x
Single Level Arbiter	x
Bus Release Functions	6
Primary VMXbus Interface (D32NA)	x
Interrupt Handler	x
RESET, TEST, RUN and CACHE switch	x
VMEPROM Firmware	128 Kbyte
Power Requirements	
+ 5V (max)	5.3A (2x)
+12V (max)	0.2A (1x)
−12V (max)	0.2A (1x)
Operating Temperature (degree C)	0 to 50
Storage Temperature (degree C)	−40 to 85
Relative Humidity (Non-condensing)	0 to 95 %
Board Dimensions 234 x 160 mm (9.2 x 6.3")	x
No. of Slots used	2
Thickness	38 mm (1.39")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General Description
The SYS68K/SRAM-22 is an ultra high speed static RAM board designed for the 68020 processor board, CPU-21.
The static memories are 64K x 1 oriented and have an access time of as low as 45ns. This allows operation of the 68020 at a clock frequency of up to 20MHz without any wait states. Therefore, maximum throughput is provided using the SRAM-22 board.

1.0 Hardware Description

1.1 The Static RAM
The memory organisation is 32 bit wide (512 Kbyte in total) to allow maximum throughput for the 68020. Aligned and unaligned transfers are supported because each byte strobe is separately controlled via a decoding logic on the local memory expansion. Zero Wait State operation of 16.7 MHz processor clock frequency is provided using 55ns devices.

Two banks (32 chips each) are associated with one SRAM board. 2 LEDs show if an access is pending to one of the two memory banks.
To support the higher clock frequency of CPU-21A, the SRAM-22A is equipped with 45ns devices.
The RAM extension for CPU-21A can only be made with SRAM-22A.

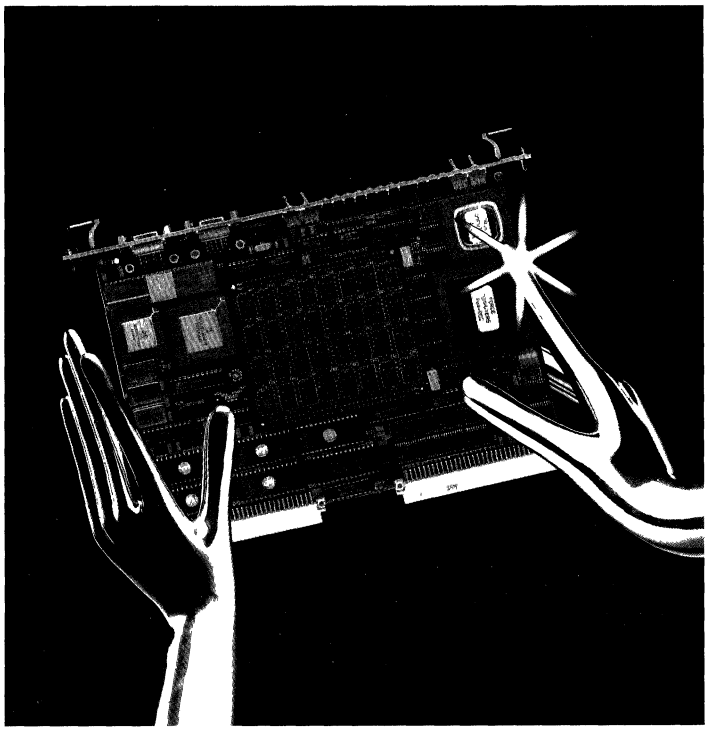
1.2 Serial I/O Interface
A Multi Protocol Communications Controller (68561 MPCC) is installed on the SRAM-22 to provide an additional serial communication channel. The interface type is jumper selectable between RS232 and RS422 driver/receiver circuits.
A jumperfield offers flexible I/O signal assignment to the 25 pin D-sub connector on the front panel.

Specification SRAM-22

Memory Capacity	512 Kbyte
Access Time of SRAMs	70ns on SRAM-22S 55ns on SRAM-22 45ns on SRAM-22A 35ns on SRAM-22B
No. of SRAMs	64 (64K x 1)
Serial I/O Channel	1
RS232 interface	x
RS422 interface	x
Power Requirements	
+ 5V (max)	2.8A
+12V (max)	0.1A
−12V (max)	0.1A
Operating Temperature (degree C)	0 to 50
Storage Temperature (degree C)	−40 to 85
Relative Humidity (non-condensing)	0 – 95 %
Board Dimensions	
234 x 160 x 18 mm (9.2 x 6.3 x 0.71")	x

Ordering Information

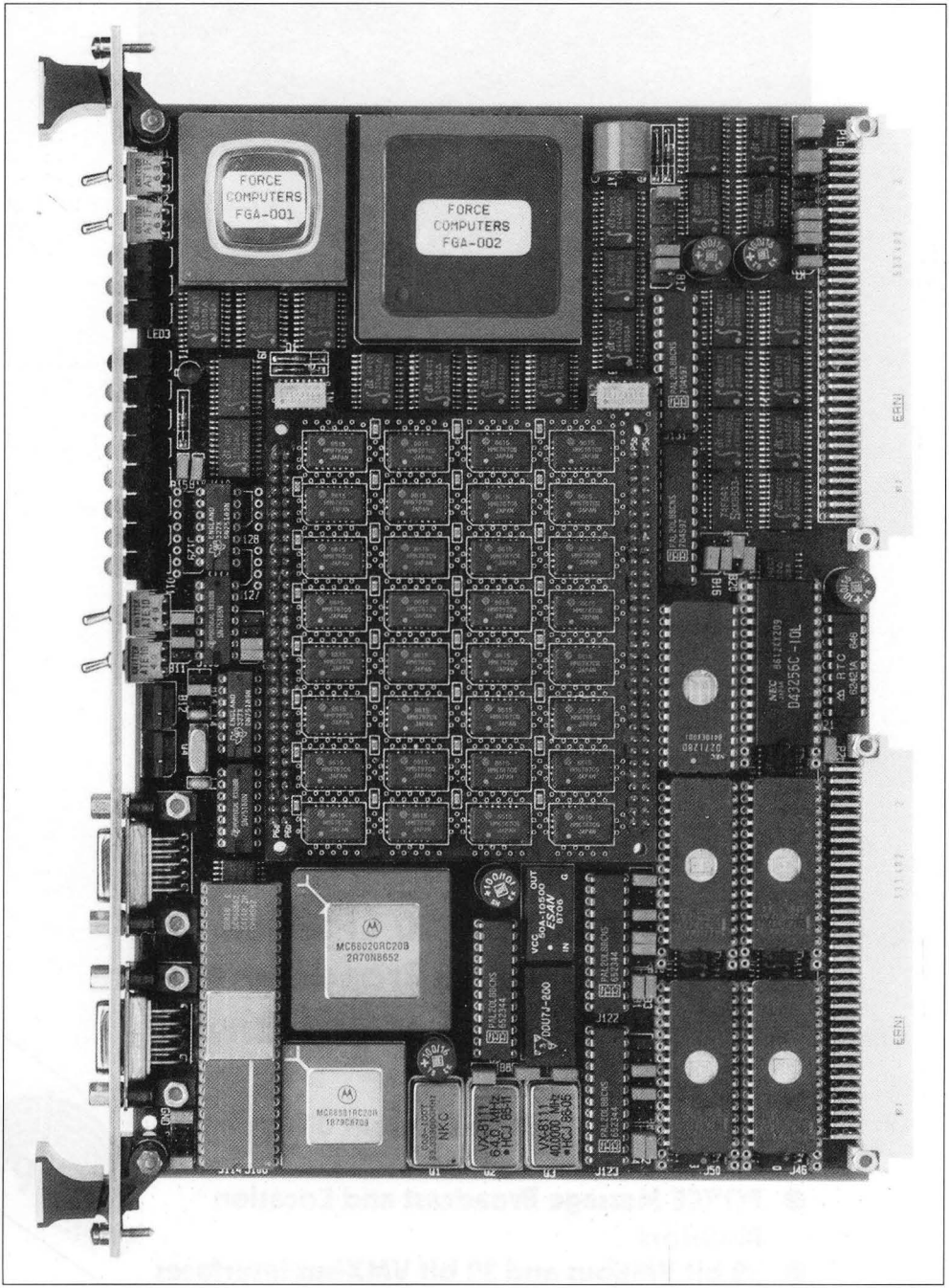
SYS68K/CPU-21S Part No. 101041	68020 CPU board including Floating Point Co-processor 68881 with 12.5 MHz clock frequency and 512 Kbyte of zero wait state RAM including documentation and VMEPROM
SYS68K/SRAM-22S Part No. 201040	512 Kbyte Static Memory board with an additional serial I/O interface supporting CPU-21S
SYS68K/CPU-21 Part No. 101001	68020 CPU board (CPU-20) including Floating Point Co-processor 68881 with 16.7 MHz clock frequency and 512 Kbyte of zero wait state RAM including documentation and VMEPROM
SYS68K/SRAM-22 Part No. 201000	512 Kbyte Static Memory board with an additional serial I/O interface supporting CPU-21
SYS68K/CPU-21A Part No. 101011	68020 CPU board with 20.0 MHz clock frequency, 68881 FPCP and 512 Kbyte of zero wait state RAM including documentation and VMEPROM
SYS68K/CPU-21YA Part No. 101061	68020 CPU board with 20 MHz clock frequency, 68881 FPCP and 2 Mbyte of zero wait state RAM including documentation and VMEPROM
SYS68K/SRAM-22A Part No. 201010	512 Kbyte Static Memory board with an additional serial I/O interface supporting CPU-21A
SYS68K/CPU-21B Part No. 101021	68020 CPU board with 25.0 MHz clock frequency, 68881 FPCP and 512 Kbyte of zero wait state RAM including documentation and VMEPROM
SYS68K/CPU-21YB Part No. 101071	68020 CPU board with 25.0 MHz clock frequency, 68881 FPCP and 2 Mbyte of zero wait state RAM including documentation and VMEPROM
SYS68K/SRAM-22B Part No. 201020	512 Kbyte Static Memory board with an additional serial I/O interface supporting CPU-21B
SYS68K/CPU-21 UM Part No. 800073	Hard- and Software User's Manual for CPU-21 and SRAM-22
SYS68K/VMEPROM UM Part No. 800140	VMEPROM User's Manual



System 68000 VME SYS68K/CPU-22

Multiprocessor 68020 CPU Board with DMA, Message Broadcast and the Supreme Dual Ported Memory

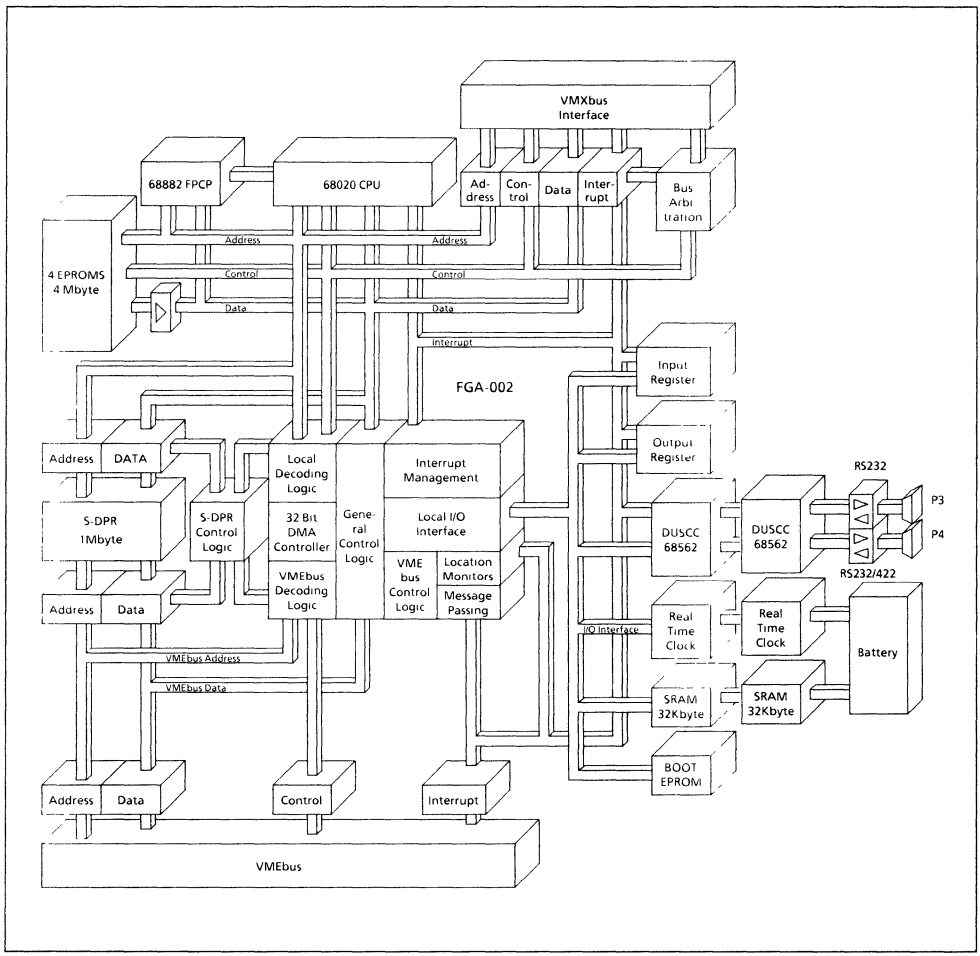
- 16.7 or 20.0 MHz
- 256 Kbyte or 1 Mbyte constant 0 Wait State SRAM
- FORCE Message Broadcast and Location Monitors
- 32 bit VMEbus and 32 bit VMXbus Interfaces


FORCE
COMPUTERS
FGA-001
FORCE
COMPUTERS
FGA-002
MC68020RC20B
2R70N8652
D43256C-10L
VX6111
64.0 MHz
VX6111
40.000 MHz

1. General Description

The SYS68K/CPU-22 is a 68020 based CPU-board especially designed for multiprocessor applications. The Supreme Dual Ported RAM supports constant zero wait state access of the 68020 CPU to the S-DPR while the RAM is also accessed from the VMEbus side. The high speed fully dual ported and dual buffered static RAM with a capacity of 256 Kbyte or 1 Mbyte also supports read and write protection for three individual memory areas from the VMEbus side.
The SYS68K/CPU-22 also includes the 68882 enhanced Floating Point Coprocessor and a full 32 bit DMA Controller which is built inside the 280 pin FORCE specific Gate Array. The DMA Controller can transfer data fully independant from the operation of the local CPU.
Special multiprocessor functions are the 2 independent 8 bit wide Message Broadcast FIFOs, and the 16 location monitors. Each supports the interruption of the local CPU on a software programmable level.
Additional features include the up to 4 Mbyte EPROM capacity (32 bit wide), the 2 multi-protocol serial I/O links, the 32 Kbyte battery backed up SRAM, the Real Time Clock/Calender and the VMXbus interface.

BLOCK DIAGRAM OF THE SYS68K/CPU-22



2. Features of the SYS68K/CPU-22 Boards:

- 68020 CPU with 16.7 or 20.0 MHz clock frequency.
- 68882 Floating Point Coprocessor with 16.7 or 20.0 MHz clock frequency.
- 32 bit DMA Controller supporting data transfer speeds of up to 30 Mbyte/s (memory to memory). 32 byte internal FIFO for burst DMA.
- 256 Kbyte or 1 Mbyte constant zero wait state static RAM dual ported to the VMEbus with three fully independent software programmable access address ranges and write/read protection.
- Four user EPROM sockets for up to 4 Mbyte EPROM capacity supporting the 28 and 32 pin JEDEC standard-one wait state operation from EPROMs by using 100 ns devices.
- One system EPROM socket for local booting and initialization of the I/O and the Gate Array.
- 32 Kbyte of static RAM with on-board battery backup and power fail detection logic.
- Real Time Clock/Calender with battery backup.
- Two multi-protocol serial I/O channels with SDLC, HDLC and asynchronous protocols – RS232 compatible (one RS422 configurable).
- Two 24 bit timers with 5 bit prescaler – each timer may interrupt the 68020 CPU on a software programmable level (1 to 7).
- Three 8 bit timers with an 8 bit prescaler also supporting interrupts to the 68020 CPU on a software programmable level (1 to 7).
- One 8 bit timer with an 8 bit prescaler used as a watchdog timer to force a SYSFAIL to the VMEbus (software selectable).
- BERR handling fully under software control via different counters for local, VMEbus and secondary bus accesses.
- Full 32 bit VMEbus master interface supporting the following data transfer types:
  A32, A24, A16 : D8, D16, D32
  UAT, RMW and address only cycles.
- Full 32 bit VMEbus slave interface to the Dual Ported RAM supporting the following data transfer types:
  A32, A24 : D8, D16, D32
  UAT, and address only cycles
- Single level bus arbiter
- SYSCLK driver
- VMEbus Interrupt Handler (IH 1 to 7 dynamic)
- Two independent Message Broadcast FIFOs for simultaneous access of up to 20 CPU boards installed in one RACK.
- 16 software programmable location monitors supporting 16 different interrupt vectors on individual software programmable levels (1 to 7).
- Support for ACFAIL and SYSFAIL via software programmable IRQ-levels.
- Timeout counter (3 seconds), if the board does not receive VMEbus mastership. Software selectable in parallel to the standard bus error counters.
- VMXbus interface supporting 8, 16 and 32 bit data transfers.
- VMEPROM the real time monitor with file manager and Real Time Kernel (PDOS compatible) is installed on each board version.

3. Hardware Description

3.1 The 68020 CPU

The 68020 with its 32 bit address and data paths is installed on the SYS68K/CPU-22 board.
The CPU includes a 256 byte instruction cache which significantly reduces the number of bus cycles needed for program fetches. A CACHE switch on the front panel allows the user to enable or disable the on-chip cache for software debugging purposes.
To achieve maximum performance, the 68020 CPU accesses the Dual Ported Memory constantly without the insertion of wait states.
Communication with the local I/O interfaces, local SRAM, and the VMEbus interface is provided through the specially designed 280 pin Gate Array.
The EPROM area, the Floating Point Coprocessor, the Dual Ported RAM and the VMXbus interface are directly connected to the CPU data and address bus interface (as shown in the block diagram of the SYS68K/CPU-22).
The clock frequency of the CPU is 16.7 or 20.0 MHz. This offers, in combination with the Dual Ported RAM, a real computing rate of 2-4 MIPs.

3.2 The Floating Point Coprocessor

The SYS68K/CPU-22 is fitted with the enhanced 68882 Floating Point Coprocessor (FPCP). The clock frequency of the CPU and the FPCP is identical. The FPCP conforms to the IEEE Floating Point standard 754 (draft 10.0).
Easy floating point operation control to the coprocessor is provided because the intercommunication between the CPU and the FPCP is built in silicon.
An internal register set inside the FPCP of 8 general purpose registers (80 bit wide) yields fast execution times.

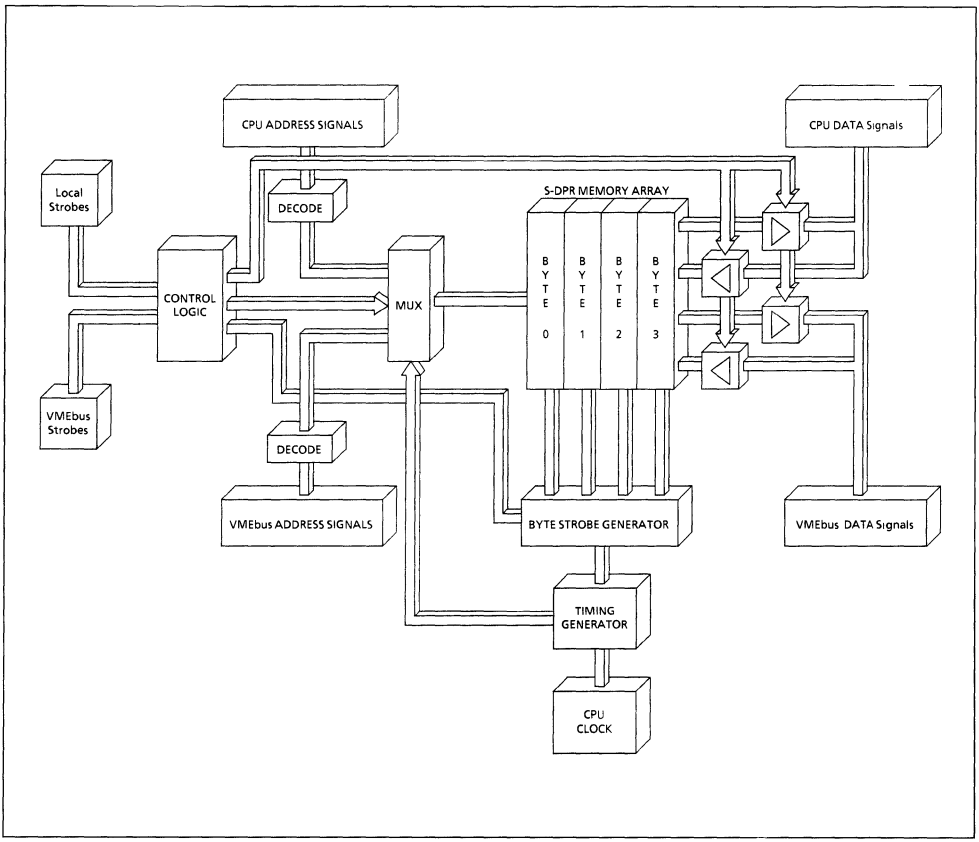
Features of the FPCP

- 8 general purpose registers (80 bit, 64 bit Mantissa, 15 bit exponent and one sign bit)
- 67 bit on-chip ALU
- 67 bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 standard (draft 10.0)
- Full support of trigonometrical and logarithmic functions such as:
  SINE and COSINE
  TANGENT and COTANGENT
  Hyperbolic functions (TANGENT,
  ARC TANGENT, SINE and COSINE)
  Logarithmic functions (4)
  Square root and exponential functions (4)
- The 68882 is fully software compatible to the 68881 FPCP

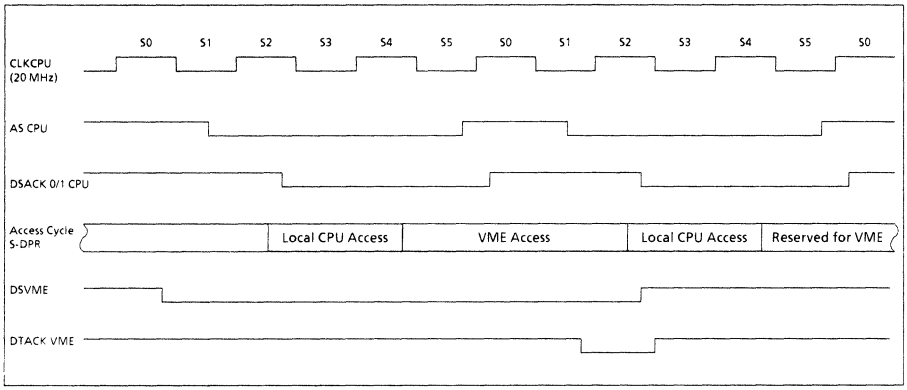
3.3 The Dual Ported RAM

The SYS68K/CPU-22 contains a Supreme Dual Ported static RAM design called S-DPR, which constantly supports zero wait state accesses of the local CPU. All accesses of the 68020 CPU to the S-DPR are immediately serviced while the VMEbus accesses are forced to the S-DPR between the 68020 access cycles.
This technique allows the SYS68K/CPU-22 to guarantee a constant run time of all programs regardless of whether an access to the S-DPR from another VMEbus board is forced or not.
The bandwidth of the S-DPR for the local CPU is 25 Mbyte/sec plus 15 Mbyte/sec for the VMEbus. This results in a total S-DPR bandwidth of 40 Mbyte/sec.
A detailed block diagram of the S-DPR control mechanism and a global timing diagram are outlined below.

BLOCK DIAGRAM OF THE S-DPR

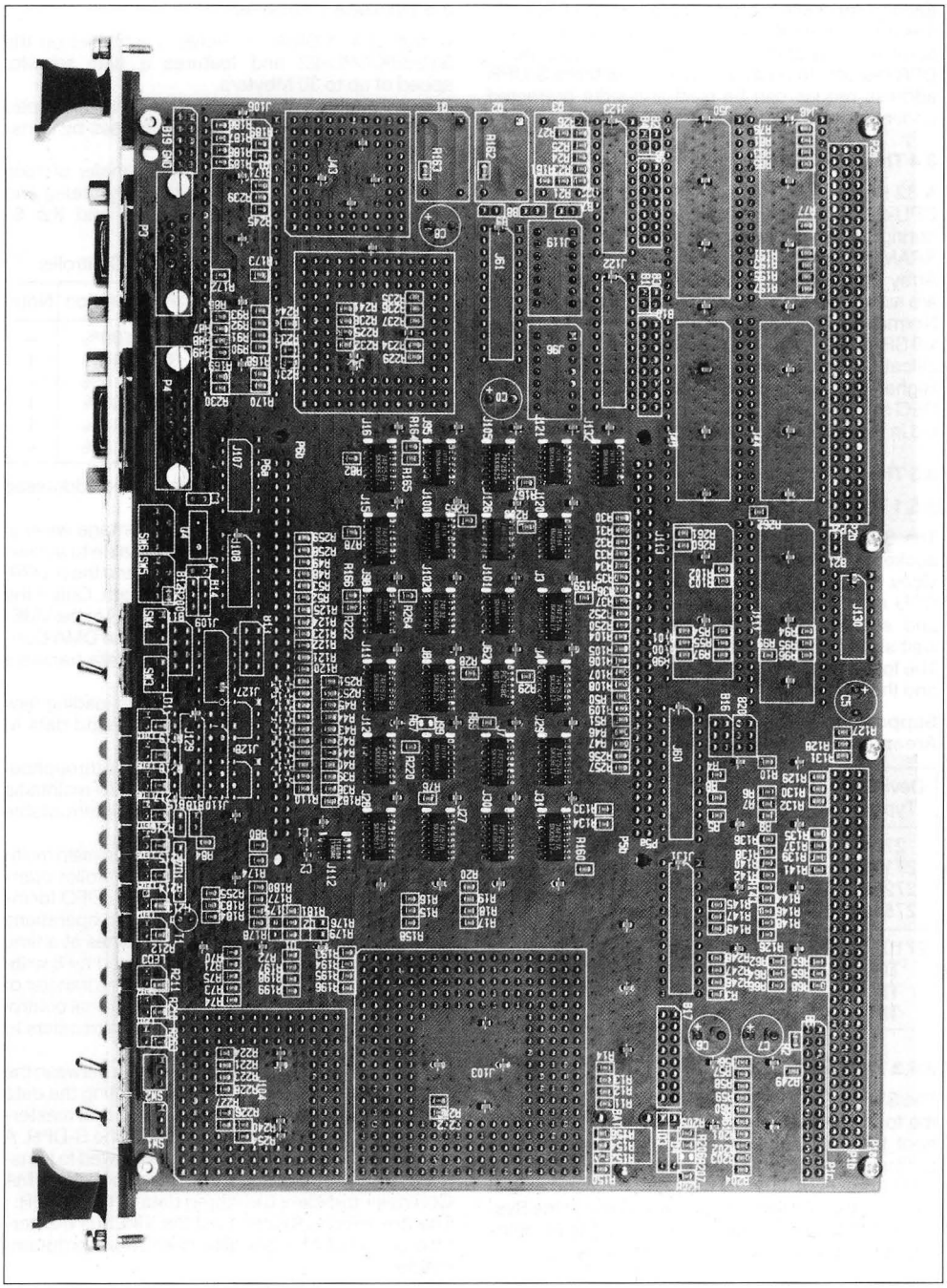


TIMING DIAGRAM OF THE S-DPR



A key advantage of the S-DPR technology is that the SYS68K/CPU-22 can be used in critical real-time applications without loosing the real-time capabilities through external accesses to the S-DPR. Alternative technologies such as the dual gated mechanism (the CPU is halted during the VMEbus accesses), or the dual buffered function (alternative access to the DPR while one requester is waiting until the RAM is unused) cannot guarantee constant zero wait state operation. In non – S-DPR configurations the CPU normally waits or is halted during a VMEbus access cycle which results in a decreased CPU throughput.
The SYS68K/CPU-22 indeed combines the highest possible throughput (zero wait state accesses) with the Dual Ported RAM structure without decreasing performance at a CPU clock frequency of 16.7 or 20.0 MHz.
The memory capacity is 256 Kbyte, or 1 Mbyte depending on the board version.

Increasing the memory capacity from 256K to 1 Mbyte is possible by exchanging the SYS68K/SMDP-05 memory module with a SYS68K/SMDP-06 module. The SYS68K/SMDP-06 board holds 1 Mbyte RAM. The SMDP-06 board has the same dimensions as the SMDP-05 and can easily be installed.
Underneath the SYS68K/SMDP-05/06 boards only passive components such as resistors and capacitors are installed to guarantee correct operation for an ambient temperature range of 0 to +50 degrees C.
The access address of the S-DPR is fully software programmable through the installed Gate Array within the 4Gbyte address range.
Address and address modifier decoding for the VMEbus accesses is software programmable through the Gate Array. Three independent areas, in 4 Kbyte increments, can be defined by the on-board CPU.



Each of the three independent memory areas forces a data transfer cycle to the S-DPR under the software programmed address range where the S-DPR resides. In addition, each of the three S-DPR address ranges can be read and write protected under software control during run time.

3.4 The Local SRAM

A 32 Kbyte static RAM is installed on all SYS68K/CPU-22 board versions and supports data storage during power down phases for up to 1 year. The SRAM is directly connected to the FORCE Gate Array I/O interface. Long, word and byte transfers are automatically controlled via the Gate Array.
Normal read and write operations to the single 32K x 8 SRAM are allowed if the power is within the specification detected by a separate power sensor. Higher organized devices compatible to the JEDEC standard (i.e. 128K x 8 devices) can be installed in the 32 pin socket.

3.5 The EPROM Areas

3.5.1 The USER EPROMs

The SYS68K/CPU-22 contains four user EPROM sockets supporting four 28 or 32 pin EPROM devices. Maximum data throughput to the 68020 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation if 100 ns devices are installed. The following table lists the supported device types and the memory capacity.

Supported Device Types in the User EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
2764	28	8K x 8	32 Kbyte
27128	28	16K x 8	64 Kbyte
27256	28	32K x 8	128 Kbyte
27512	28	64K x 8	256 Kbyte
271024	32	128K x 8	512 Kbyte
TBD	32	256K x 8	1 Mbyte
TBD	32	512K x 8	2 Mbyte
TBD	32	1M x 8	4 Mbyte

3.5.2 The SYSTEM EPROM

The SYS68K/CPU-22 board contains in addition to the four user EPROMs a single system EPROM to boot the local CPU, initialize all I/O devices and program the board dependent functions of the Gate Array FGA-002. All the presetting and initialization of the I/O devices are made through the System EPROM to ease the adaptation of the complex board functions to the application needs.

3.6 The DMA Controller

A high speed DMA Controller is installed on the SYS68K/CPU-22 and features a data transfer speed of up to 30 Mbyte/s.
This throughput is the effective transfer speed which assumes zero wait state accesses by transferring 32 bit of data.
The SYS68K/CPU-22 allows the transfer of data between memory (2 different memory areas) and between VMXbus/VMEbus memory and the S-DPR, as listed below.

Possible Data Transfers for the DMA Controller

Area 1		Area 2	CPU operation	Note
VMEbus	⟷	VMEbus	100%	–
VMEbus	⟷	S-DPR	60 – 40%	1
VMXbus	⟷	VMXbus	0%	–
VMXbus	⟷	S-DPR	60 – 40%	1
VMXbus	⟷	VMEbus	60 – 40%	1
S-DPR	⟷	S-DPR	0%	–

Note 1: Dependent on the speed of the addressed boards

The center row lists the time (percentage wise) in which the local CPU is operable and able to access the local I/O devices, EPROM areas and the S-DPR, while the DMA Controller transfers data. Only if the local CPU wants to access the VMXbus or the VMEbus does the CPU have to wait until the DMA Controller has finished the maximum 8 data transfers from its FIFO.
This allows a program to be run while loading new data into the S-DPR or writing processed data to global RAM or I/O controller boards.
This feature significantly increases data throughput and functionality because the local CPU maintains the real-time capabilities by being interruptable during DMA transfers.
To increase the data throughput and maintain multiprocessor functionality, the DMA Controller operates in burst mode by using its 32 byte FIFO for internal data storage. The read and write operations are executed in 8 cycles fetching 4 bytes at a time which result into 8 read cycles followed by 8 write cycles. The DMA Controller supports the transfer of data on unaligned addresses, as an internal control mechanism is installed to align the data transfers to 32 bit accesses if possible.
This technology allows to transfer data between the S-DPR and the VMEbus by first collecting the data from the VMXbus/VMEbus, giving up bus mastership and then transferring the data to the S-DPR. A second VMXbus/VMEbus board is allowed to transfer data on the VMXbus/VMEbus while the DMA Controller transfers the stored data to the S-DPR.
The bus release functions of the VMEbus mastership of the DMA Controller is software programmable.

The DMA Controller is installed inside the 280 pin Gate Array supporting 32 data and address signals. All addressing modes of the VMEbus are fully software programmable (AM-Codes) for the source and destination address.
The data transfer speed between the S-DPR and the VMXbus/VMEbus depends on the access time of the addressed VMXbus/VMEbus module.
The following register set shows the structure of the DMA Controller in more detail.

Register Set of the DMA Controller

4	DMA Interrupt Control Registers. Normal Termination.
4	DMA Interrupt Control Registers. ERROR Termination.
8	DMA General Control Register.
8	DMA Mode Control Register.
8	DMA Destination Attributes and AM-Code.
8	DMA Source Attributes and AM-Code.
32	Source Address Register.
32	Destination Address Register.
32	Transfer Count Register.

3.7 The Local I/O Devices

The Gate Array installed on the SYS68K/CPU-22 includes an 8 bit local I/O bus interface.
The Real Time Clock, the serial I/O controller and the port read/write functions are directly connected to this I/O interface.

3.7.1 The Serial I/O Interfaces

A Dual Universal Serial Communication Controller (DUSCC 68562) is installed on the SYS68K/CPU-22 to communicate via two serial interfaces to terminals, printers, computers or other equipment.

Features of the DUSCC

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multi-protocol operation consisting of:
  BOP: HDLC/ADCCP, SDLC, SDLC Loop, X.25 or X.75 link level
  COP: BISYNC, DDCMP, X.21
  ASYNC: 5-8 bit plus optional parity
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1,Manchester
- 4 character receiver and transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter
- Digital phase locked loop
- User programmable counter/timer
- Programmable channel modes full/half duplex, auto echo, local loopback
- Modem control signals for each channel: RTS, CTS, DCD
- CTS and DCD programmable auto enables for Receiver (RX) and Transmitter (TX)
- Programmable interrupt on change of CTS or DCD

The I/O signal assignment of each of the two channels is listed in the following table:

Signal	Input	Output	9 Pin DSUB Connector	Description
DCD	x		1	Data Carrier Detect
RXD	x		2	Receive Data
TXD		x	3	Transmit Data
DTR		x	4	Data Terminal Ready
GND			5	Signal GND
DSR	x	x	6	Data Set Ready
RTS		x	7	Request to Send
CTS	x		8	Clear to Send
–	–	–	9	Not Connected

The first channel is assigned to connect a terminal via the RS232 compatible interface.
The second channel can be configured to work as a RS232 or as a RS422 compatible interface. R/C components can be installed to adapt to various cable lengths and reduce reflections if the RS422 compatible interface is selected.
The DUSCC is able to interrupt the local CPU on a software programmable IRQ-level (1-7) by supplying its own software programmable IRQ vectors (6 in total) to the local CPU.

3.7.2 The Real Time Clock

A software programmable Real Time Clock (RTC-62421) with on-board battery backup is installed on the SYS68K/CPU-22 boards. The features of the Real Time Clock are listed below.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12hr/24hr clock switchover
- Automatic leap year setting
- Interrupt masking
- C-MOS design provides low power consumption during power down mode.

The Real Time Clock is able to interrupt the local CPU on a software programmable level (1 to 7).

3.7.3 The Input/Output Register

A total of three input and one 8 bit output port is available on the SYS68K/CPU-22.
The first 8 bit input port is connected to the two 4 bit HEX rotary switches available on the front panel for configuration purposes.
The second 8 bit input port allows the jumper settings to be read (1 or 0) on a jumperfield installed on the PCB. This jumperfield can be used to define the slot number or to define application dependent pre-settings.
The third 8 bit input port allows the memory capacity of the S-DPR to be read. Each SYS68K/SMDP board has three readable status bits describing the memory capacity. In addition, the CPU board type can be read via the remaining 5 bits.
Four LEDs are controlled via the 8 bit output port. The remaining 4 bits are used for board specific control functions.

3.7.4 The Timers

A total of 6 independent timers are available for the user. These timers offer maximum flexibility because each timer can be used to force an interrupt to the CPU on a software programmable IRQ-level.
The first two timers each provide a 24 bit timer with an individual 5 bit prescaler.
The next three timers are 8 bit wide and include an 8 bit prescaler.
The sixth timer is used to generate the SYSFAIL signal to the VMEbus. SYSFAIL can be used in multiprocessor systems to signal that one board has detected a failure. This 6th timer is used as a watchdog timer which needs to be triggered after a software programmed time before signalling SYSFAIL.
All installed timers can be used as a watchdog timer or can generate interrupts on a periodical basis.

4. The VMEbus Interface

The SYS68K/CPU-22 includes a full 32 bit VMEbus interface, thereby taking full advantage of the VMEbus specification.
The address modifier codes for A16, A24 and A32 addressing are fully supported in master and slave mode.
In slave mode the Gate Array decodes the AM-codes and the address signals of the VMEbus and signals the on-board control logic if one of the three independent decoding ranges are addressed correctly and if the access cycle has to be executed (read/write protection).
The Gate Array forces the access cycle to the S-DPR and controls/adapts the data flow (8, 16, 24 or 32 bit of data) automatically.

The following data transfer types are supported in master and slave mode:

Transfer Type	D31-D24	D23-D16	D15-D8	D7-D0
Byte			x	x
Word			x	x
Long Word	x	x	x	x
Unaligned Transfers	x	x x x	x x x	x
Read Modify Write*	x	x	x x	x x x

* Read modify write cycles are split into separate read and write cycles only in the slave mode while multiprocessor synchronization is provided via the Gate Array.

The access times to access the S-DPR from the VMEbus are listed in the following table:

Access Times	Min	Type	Max
Read	120 ns	215 ns	330 ns
Write	110 ns	195 ns	310 ns

The SYS68K/CPU-22 includes a DMA Controller supporting high speed data transfer through the on-board Gate Array. DMA transfers can be performed between the S-DPR and VMEbus memory while the 68020 CPU is operating.
The SYS68K/CPU-22 includes the following bus arbitration modes:

RWD	Release when done
ROR	Release on request
ROBCLR	Release on Bus Clear
RAT	Release after Timeout

In addition, the board is able to request bus mastership if no other board requests bus mastership (Request on No Request-RNR).
Each of the listed modes is software programmable inside the Gate Array. The bus request level of the SYS68K/CPU-22 is jumper selectable (BR0-3). A single level arbiter, a power monitor, a SYSRESET generator and support for ACFAIL and SYSFAIL complete the VMEbus interface.
The installed location monitor and the Message Passing on VME are briefly described in the next two sections.

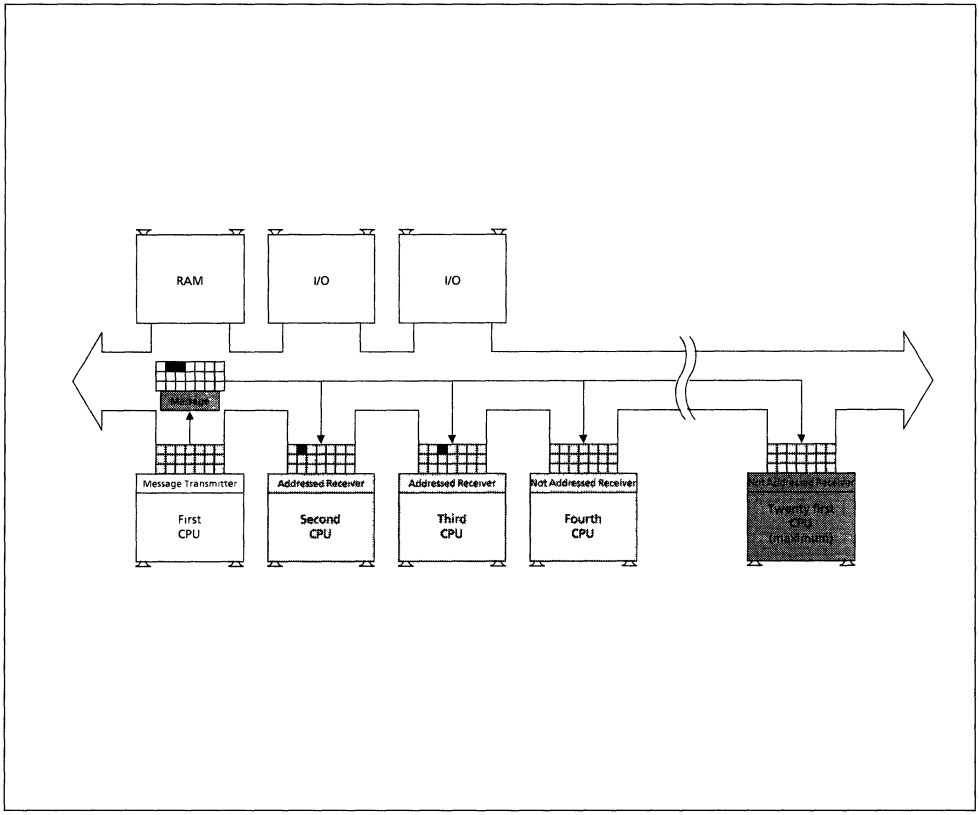
5. The Location Monitors

The SYS68K/CPU-22 includes 16 location monitors. Each of these location monitors allows an interrupt to be forced to the local 68020 CPU. The interrupt level of each location monitor is software programmable and an individual interrupt vector for each location monitor is forced to the CPU.
This function allows the triggering of multiple CPU boards via one master by only fetching an interrupt vector on the local bus and leaving the VMEbus free for data transfers.
In addition, the location monitor bits can be used to synchronize multiple CPUs via standard read cycles by internally forcing a read-modify-write cycle. This allows various CPUs on the VMEbus to be synchronized (for example a 68020 and a 80386 CPU-board).

6. The Message Broadcast

The SYS68K/CPU-22 board provides two fully independent unique Message Broadcast functions which are implemented within the Gate Array.
The FORCE Message Broadcast (FMB) allows the simultaneous addressing and interrupting of all CPU boards installed in a VMEbus environment. It stores a 8 bit message in a 8 stage deep FIFO.
The Message Broadcast complies fully to the VMEbus specification and minimizes the time overhead required to interrupt all installed CPU boards in a system.
If, for example, 16 boards are installed in a system without FMB, the minimum time required to interrupt all of them is 16 times an access cycle to each of their location monitors. If no location monitors are available then the IRQ signals of the VMEbus have to be used. This results in a maximum number of 7 boards to be synchronized (7 VMEbus IRQ levels). The time required to interrupt all of them is enormous because each board has to request bus mastership and initiate an interrupt acknowledge cycle. This results in a big timing gap between the different CPU boards being interrupted.
The FMB allows each of the maximum 21 defined boards in the system to be addressed and to interrupt one, some or all of them, sending the addressed boards an 8 bit message.
The FMB therefore allows any board(s) to be triggered at the same time by fetching the interrupt vector on the local bus leaving the VMEbus free for activities of other bus masters.
Each participant of the FMB stores the single byte message in its 8 byte deep FIFO (inside the Gate Array) and at the same time interrupts their local CPU on a software programmable level (1 to 7).
Each of the two, fully independent FIFOs is designed to allow as many as 8 messages to be sent to multiple participants within a short time frame. The messages can be read from the local CPU after the interrupt has been acknowledged.
The FMB byte is user defined to allow maximum flexibility and to adapt the various requirements to the user needs.
The most important feature of the FMB is that any 32 bit VMEbus based CPU available on the market can send this message byte to a FORCE board supporting the FMB function.
No special motherboard or extended address modifier capabilities are needed because only the defined signals, timings and data transfer types are used to perform the FMB.
Each master can define the board(s) which have to receive the FMB byte on an individual base. The hardware inside the Gate Array decodes the information from the used address and performs the cycle.
The data transfer of the FMB is completed in less than 330 ns for all CPU boards which results into a maximum data bandwidth (theoretical) of 20 x 3 Mbyte/s = 60 Mbyte/s.
A patent on the FMB is pending.
The FORCE Message Broadcast is described in detail in the SYS68K/FMB Data Sheet while the general block diagram is shown below.

BLOCK DIAGRAM OF THE FORCE MESSAGE BROADCAST



7. The Interrupt Structure

The Gate Array installed on the SYS68K/CPU-22 handles all the local, VMEbus and secondary bus interrupts. Each interrupt request from the local bus through the DUSCC, RTC and the two timers, as well as the Gate Array specific interrupt requests, are combined with the 7 VMEbus interrupt requests.
Each IRQ source including the 7 VMEbus IRQs can be programmed to interrupt the CPU on an individual programmable level (1 to 7).
The Gate Array supports the vector, or initiates an interrupt vector fetch from the local I/O devices or from the VMEbus.
In addition to the local interrupts, the ACFAIL and SYSFAIL signals can be used to interrupt the CPU on a software programmable level.
This results in a total of 40 individual IRQs handled through the Gate Array on the SYS68K/CPU-22 board.
The Gate Array supplied interrupt vectors have a basic vector and fixed increments for each source. The basic vector is software programmable.

8. The VMXbus Interface

A VMXbus primary master interface is installed on each SYS68K/CPU-22 version.
Maximum data throughput is provided on the VMXbus interface by supporting 32 bit of data in the 16 Mbyte address range. The VMXbus address range is decoded out of the 4 Gbyte address space of the 68020.
The following data transfer types are supported:

A24 : D8, D16, D32
Unaligned Transfers
Address Only Cycles
Read Modify Write Transfers

9. The Memory Map

The memory map of the SYS68K/CPU-22 is listed in the following table:

Start Address	End Address	Type
00000000	000FFFFF	Dual Ported Memory (1 Mbyte)
00100000	F9FFFFFF	VMEbus Addresses A32: D32, D24, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area (Slave and Master Mode)
FB000000	FBFEFFFF	VMEbus A24: D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus A16: D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus A24: D16, D8
FCFF0000	FCFFFFFF	VMEbus A16: D16, D8
FD000000	FDFFFFFF	VMXbus A24: D32, D24, D16, D8
FE000000	FEFFFFFF	VMXbus A24: D16, D8

Start Address	End Address	Capacity	Type
FF000000	FF7FFFFF	8 Mbyte	USER–EPROM
FF800000	FFBFFFFF	1 Mbyte	Local I/O
FFC00000	FFCFFFFF	1 Mbyte	LOCAL SRAM
FFD00000	FFDFFFFF	1 Mbyte	Registers of FGA-002
FFE00000	FFEFFFFF	1 Mbyte	SYSTEM EPROM
FFF00000	FFFFFFFF	1 Mbyte	Reserved

10. The VMEPROM

10.1. General Description

VMEPROM is an EPROM based real time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM. VMEPROM is composed of the powerful PDOS Real Time Kernel and the PDOS file manager. Thus the package provides support of a highly sophisticated Real Time Kernel and an interface to floppy and hard disk drives.

The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition, it includes a powerful line assembler and disassembler for the 68020 and the 68882.

VMEPROM features:

- Real Time Multitasking Kernel supporting up to 64 tasks.
- File management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Line assembler/disassembler with full support of all 68020/68882 instructions.
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify.
- S-record up/downloading from any port defined in the system.
- Disk support for RAM-disk, floppy and Winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. VMEPROM also allows disk formatting and initialization.
- Serial I/O support for up to two SIO-2 or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full screen editor.
- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.

10.2. Description of the User Interface of VMEPROM

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple command lines may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

10.3. Description of the Kernel Functions

The kernel of VMEPROM is written in 68020 assembly language for fast and efficient execution. It provides multitasking, system clock,event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously. Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

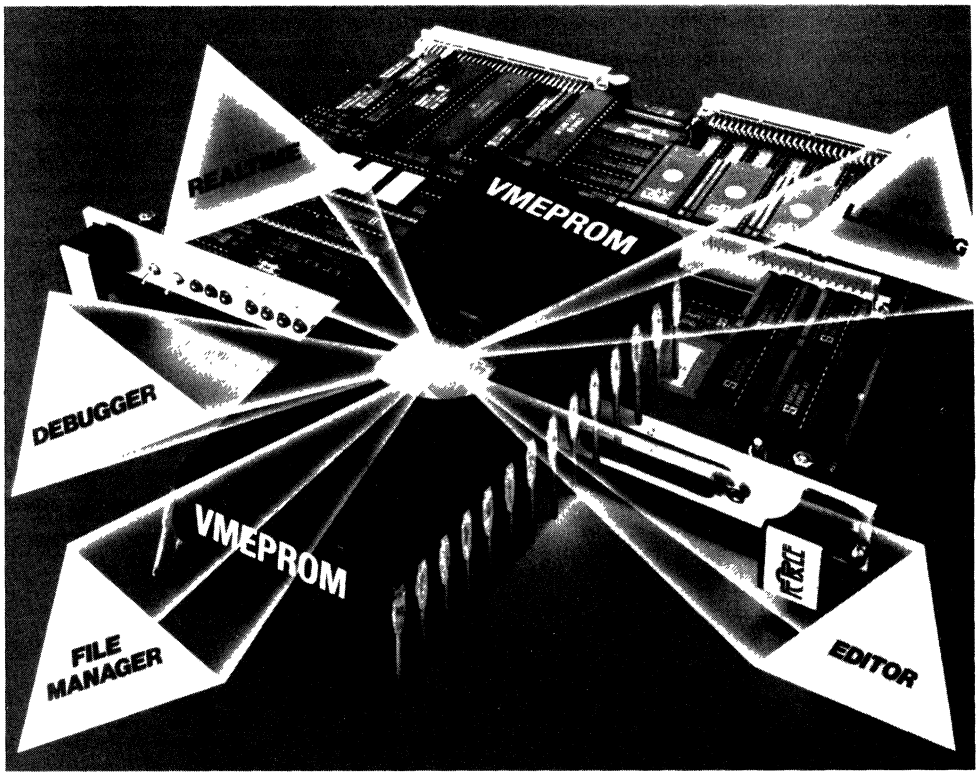
10.4. Description of the File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

10.5. Supported VMEbus Hardware

Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards, and one disk controller.
In addition, EPROM programming is supported by VMEPROM utilizing the SYS68K/RR-2/3 board family.

VMEPROM



10.6. Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 40 Kbyte. Small romable applications can be put in EPROMS easily without the overhead of the user interface.

10.7. Development Systems

Currently either one of the FORCE PDOS* or UNIX* System V development stations may be used for software development for VMEPROM.
Compilers, assemblers, and libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.
The support of VMEPROM through other development systems like the IBM-AT or the VAX is under development. These cross-software development packages will include C-compiler, assemblers for the 68020 and libraries to generate code to run under control of VMEPROM.

10.8. Licensing

No license is required for VMEPROM. VMEPROM is delivered free of charge with every CPU-22 board. For more detailed information please refer to the SYS68K/VMEPROM Data Sheet.

Specification

Function	
68020 CPU Clock Frequency on: CPU-22 CPU-22A/-22XA	 16.7 MHz 20.0 MHz
68882 FPCP Clock Frequency on: CPU-22 CPU-22A/-22XA	 16.7 MHz 20.0 MHz
DMA Controller: CPU-22 CPU-22A/-22XA Internal FIFO Max. Data Transfer Throughput	16.7 MHz 20.0 MHz 32 byte 30 Mbyte/s
S-DPR Type S-DPR Capacity: CPU-22/-22A CPU-22XA No. of Wait States for all CPU and DMA Access Cycles	SRAM 256 Kbyte 1 Mbyte 0
SRAM Capacity On-Board Battery Backup	32 Kbyte yes
No. of EPROM Sockets Data Paths Max. Capacity No. of Wait States (min/max)	4 32 bit 4 Mbyte 1/6
Serial I/O Interfaces (total) Used Controller RS232 compatible RS232/RS422 compatible	2 68562 1 1
Real Time Clock (Type) On-Board Battery Backup	62421 yes
VMEbus Interface Master: A32, A24, A16:D8, D16, D32, D(0), UAT Slave: A32, A24, A16:D8, D16, D32, D(0), UAT Software programmable Access Address and Address Modifier Code No. of different Areas for S-DPR Accesses S-DPR Read Access Time (typ) Write Access Time (typ) Single Level Bus Arbiter SYSCLK Driver 16 Location Monitors	 yes yes yes 3 215 ns 195 ns yes yes yes
FORCE Message Broadcast FMB-FIFO 1 FMB-FIFO 2	 8 byte 8 byte
VMEbus Interrupt Handler Local Bus Interrupt Handler All Sources can be routed to a Software programmable IRQ Level Total Number of IRQ Sources	1 to 7 1 to 7 yes 40

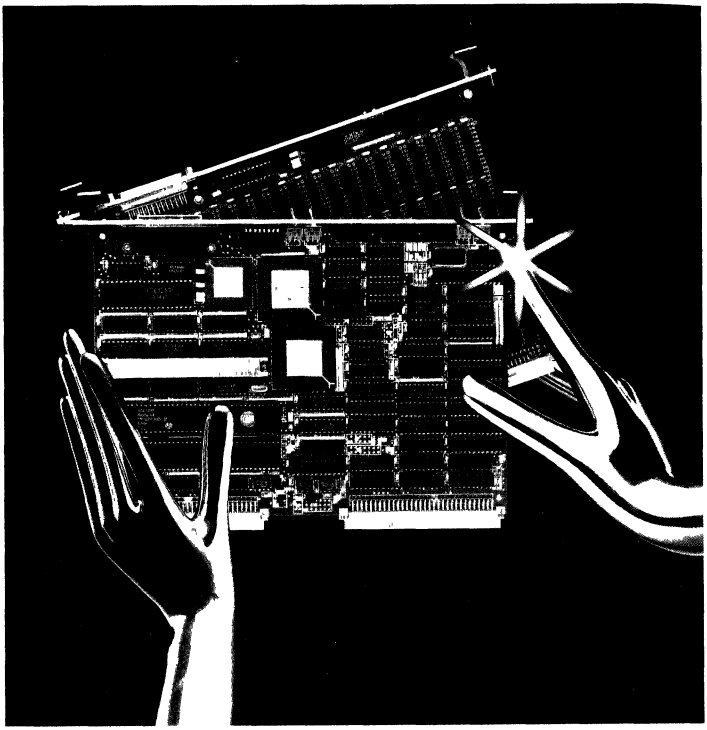
Specification (cont'd)

Function		
Timers 24 bit with 5 bit Prescaler 8 bit with 8 bit Prescaler 8 bit with 8 bit Prescaler (Watchdog Timer for SYSFAIL)		 2 3 1
VMXbus Primary Master Interface A24: D8, D16, D32, D(0), UAT, RMW Interrupt Handler		 yes yes
RESET, TEST, RUN and CACHE Switch		yes
VMEPROM Firmware on all Board Versions		128 Kbyte
Power Requirements + 5V min/max +12V min/max −12V min/max		 4.3/5.9A 0.1/0.2A 0.1/0.2A
Operating Temperature Storage Temperature Relative Humidity	(Degrees C) (Degrees C) (non-condensing in %)	0 to 50 −40 to 85 0 to 95
Board Dimensions	(mm) (in)	234 x 160 9.2 x 6.3
No. of Slots used		1

Ordering Information

SYS68K/CPU-22 Part No. 101100	16.7 MHz 68020 based CPU board with 68882 FPCP, DMAC, 256 Kbyte S-DPR capacity, VMXbus interface and VMEPROM. Documentation included.
SYS68K/CPU-22A Part No. 101101	20.0 MHz 68020 based CPU board with 68882 FPCP, DMAC, 256 Kbyte S-DPR capacity, VMXbus interface and VMEPROM. Documentation included.
SYS68K/CPU-22XA Part No. 101102	20.0 MHz 68020 based CPU board with 68882 FPCP, DMAC, 1 Mbyte S-DPR capacity, VMXbus interface and VMEPROM. Documentation included.
SYS68K/SMDP-06 Part No. 101104	1 Mbyte static RAM board replacing the 256 Kbyte SMDP-05 board installed on the CPU-22 and CPU-22A.
SYS68K/VMEPROM/UM Part. No. 800140	VMEPROM User's Manual
SYS68K/CPU-22/UM Part No. 800138	User's Manual for the SYS68K/CPU-22 products, including VMEPROM User's Manual.

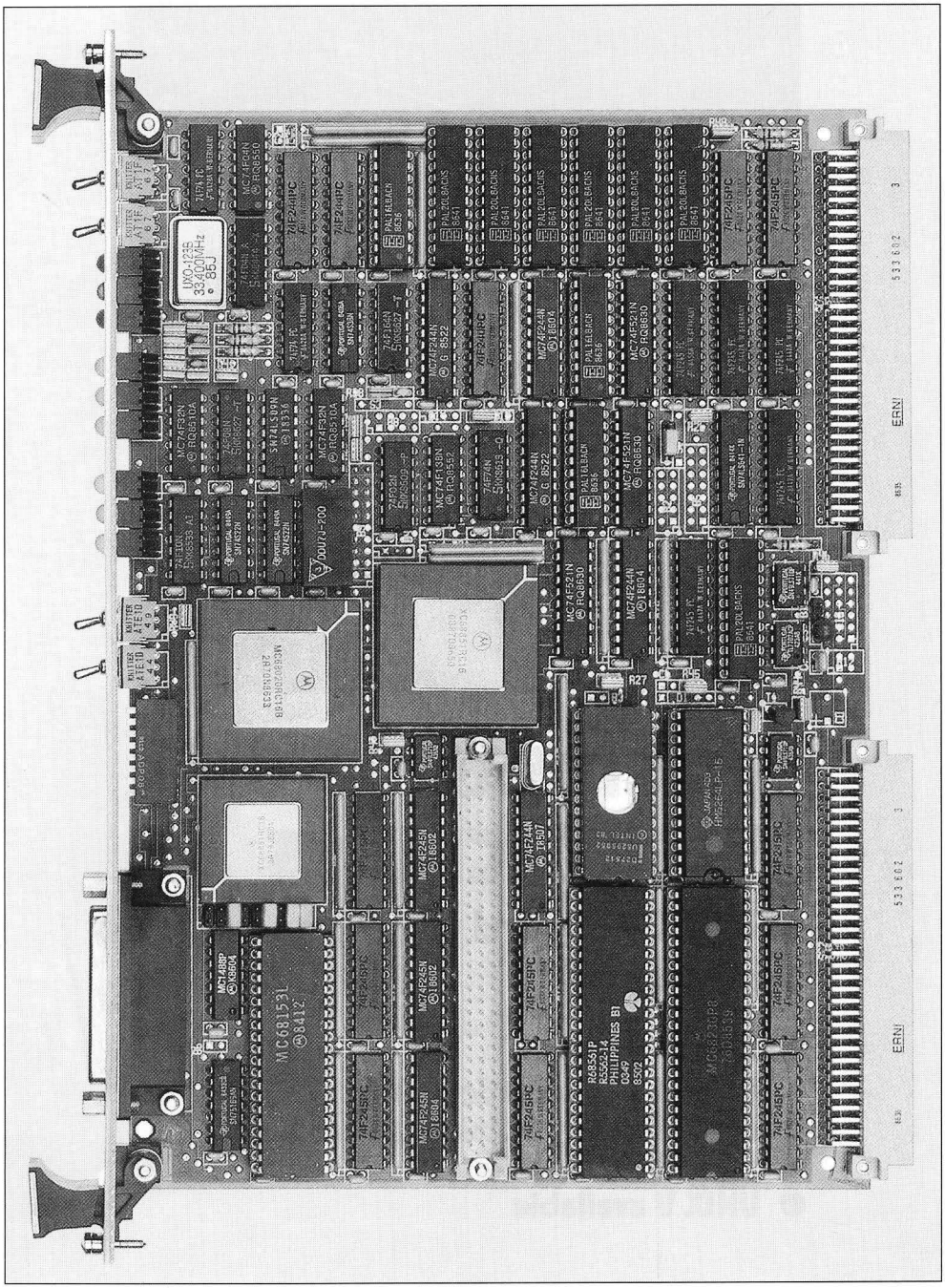
Note: SYS68K/CPU-22 board versions without the 68882 FPCP are available upon special request.



System 68000 VME SYS68K/CPU-25

68020 CPU Board with Memory Management

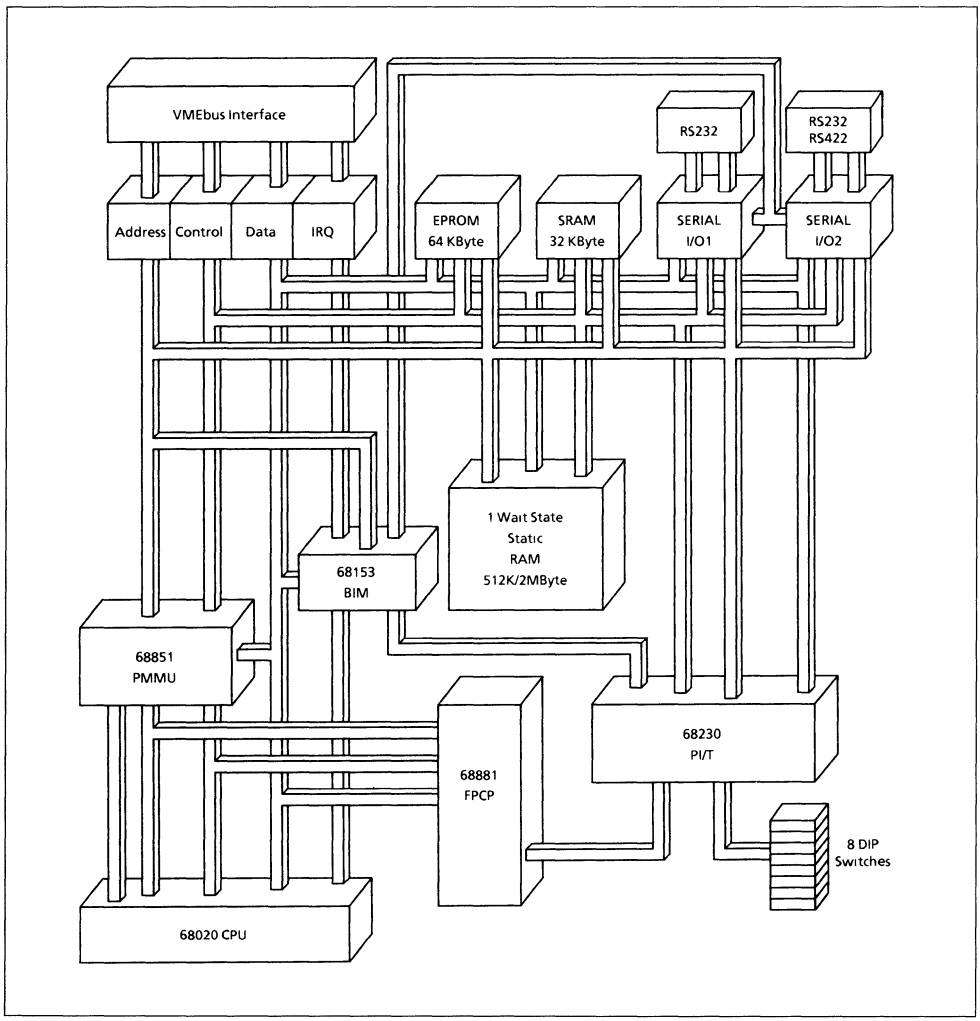
- 68851 Page MMU
- Up to 4 Mbyte static RAM
- 68881 Floating Point Coprocessor
- Serial I/O Interfaces
- UNIX V available



General Description

The SYS68K/CPU-25 is a high speed CPU board with memory management built around the 32 bit 68020 CPU. The board contains a VMEbus/IEEE 1014 compatible bus interface and offers 512 Kbyte of static RAM accessible through the Paged Memory Management Unit (PMMU 68851) with only one wait state.
CPU-25 features in addition a Floating Point Co-Processor (FPCP 68881) for complex arithmetic floating point operations.
The clock frequency of the CPU, PMMU and FPCP is always 16.7MHz.
Two serial I/O interfaces, a timer, a static RAM (32Kbyte) for vector storage for the powerful monitor firmware FORCEbug and 64Kbyte of EPROM space complete the board.
A photo of the SYS68K/CPU-25 is shown on the left page while the block diagram is shown below.

BLOCK DIAGRAM OF THE SYS68K/CPU-25



Features of the SYS68K/CPU-25

- 68020 CPU (16.7MHz)
- 68851 PMMU (16.7MHz)
- 68881 FPCP (16.7MHz)
- 512Kbyte static RAM - 1 Wait State via the FLME interface
- 68561 MPCC serial I/O interface (RS232 compatible)
- 68561 MPCC serial I/O interface (RS232 and RS422 compatible)
- 68230 PI/T for local control
- 68153 BIM for local interrupt management
- Fully buffered local address, data and control bus
- 64Kbyte of EPROM space (27512)
- 32Kbyte of SRAM space (62256) independent from the FLME memory
- VMEbus/IEEE 1014 standard interface supporting Read-Modify-Write and unaligned transfers
- RUN/HALT, RESET, ABORT and CACHE switches
- 12 LEDs for status monitoring
- 68020 Monitor with Macro facility and single line assembler and disassembler
- The SYS68K/CPU-25 is fully soft- and hardware compatible to the SYS68K/CPU-21

1.0 Hardware Description

1.1 The 68020 CPU

The 68020 CPU with its 32 address and data lines is implemented on the SYS68K/CPU-25. An on-chip cache with 256 byte capacity reduces the number of bus cycles to be executed.
The real computing rate ranges from 1.5 to 3 MIPS depending on the used instructions.
Additional instructions on the 68020 compared to the 68010 such as string manipulations, extended branches over the whole 4Gbyte addressing space offers at minimum two times the performance of 68010 CPU.

1.2 The 68851 PMMU

The logical to physical address translation is provided via the on-board PMMU supporting 4Gbyte of physical memory. Address translation is completed in one clock period which is equivalent to 60 ns at 16.7MHz clock frequency. The on-chip 64 entry address translation cache allows to build fully virtual systems in conjunction with the table search mechanism.
Hierarchical protection mechanism and Breakpoint support complete the PMMU.

1.3 The 68881 FPCP

The SYS68K/CPU-25 includes a 16.7MHz Floating Point Co-Processor. The FPCP conforms to the IEEE 754 standard and includes 8 general purpose registers (80 bit, 64 bit Mantissa, 15 bit Exponent and 1 sign bit). The 46 instruction types including trigonometrical and logarithmic functions such as sine, cosine, tangent, cotangent, hyperbolic functions, square root and exponential functions allow effective code development with standard commands.

1.4 The Serial I/O Interfaces

The SYS68K/CPU-25 contains two serial I/O interfaces built with 68561 Multi Protocol Communication Controllers supporting character oriented protocols such as BSC, DDCMP, X3.28, X.21 and ECMA16, synchronous bit oriented protocols (SDLC, HDLC, X.25) and other special protocols. CRC check, the baud/bit rate as well as the hardware handshake are software selectable. On the main board, a RS232 compatible interface available on the front panel via a 25 pin female D-sub connector is installed. The slave board offers a RS232 and RS 422 compatible interface also available via a 25 pin D-sub connector.
Each MPCC contains an 8 character receiver and transmitter buffer register to effectively support real time and non-real time system architectures.

1.5 The Local Control Device

A Parallel Interface and Timer chip (PI/T 68230) with 8MHz clock frequency is installed on the board to provide the local timer function as well as local control.
Eight DIP switches available on the front panel are readable via the PI/T to provide user defined process manipulations or presettings in the application program.
All interrupt levels of the CPU (IRQ 1 to 7) can be separately enabled or disabled via the PI/T.
The local 24 bit timer with its 5 bit prescaler can be used for time measurements or as the time base for the operating system.

1.6 The Local Interrupt Handler

A Bus Interrupter Module (BIM 68153) is installed on the board to provide a software programmable interrupt level and interrupt vector for each of the on-board interrupt sources.

1.7 The EPROM Area

A single boot EPROM is installed on the SYS68K/CPU-25 providing 64Kbyte of EPROM space by using a 27512 device.

1.8 The SRAM Area

For vector storage a static RAM with a capacity of 32Kbyte is installed on the board. FORCEbug, the macro Monitor, installed in the 27512 EPROM uses the SRAM for vector storage and for its temporary buffers.

1.9 The Local Main Memory

The SYS68K/CPU-25 contains a high speed static memory which operates 32 bit wide with only one wait state including PMMU logical to physical address translation.
The fully buffered local memory expansion interface is installed in the middle of the board via a 3rd 96 pin DIN connector to leave the P2 connector free for I/O expansion.
The memory capacity is 512Kbyte for the SYS68K/CPU-25 and 2 Mbyte for the SYS68K/CPU-25Y versions.
Memory expansion is provided by using the SYS68K/SRAM-22/22Y boards offering 512 Kbyte or 2 Mbyte additional capacity to the SYS68K/CPU-25 or CPU-25Y.
An additional RS232/422 compatible I/O interface is installed on the SYS68K/SRAM-22/22Y to allow serial communication on the local bus without using the VMEbus for this purpose.
Only the SYS68K/CPU-25 and the SYS68K/SRAM-22 operate together while the SYS68K/CPU-25Y and the SYS68K/SRAM-22Y can be combined.

1.10 The VMEbus Interface

A full 32 bit wide VMEbus interface compatible to the VMEbus, IEEE 1014 standard is installed on the SYS68K/CPU-25 products.
The 4 Gbyte address space of the 68020 is fully decoded and 8, 16, 24 and 32 bit data transfers are supported.
The support of the unaligned data transfers across the VMEbus allows the 68020 CPU to operate with its maximum throughput. To enable the support of 16 bit memory boards, the bus size of the VMEbus address space is software programmable (16 or 32 bit wide) via the PI/T.
A single level bus arbiter is installed on the SYS68K/CPU-25 to build single or small multi-processor environments without the need for a special system controller unit.
Powerful software programmable bus release functions are installed on the board to take maximum advantage of the multi-processor features defined in the VMEbus specification.
A bus driver for BERR generation during local and VMEbus accesses which are not completed within 60 to 80 us is installed on the SYS68K/CPU-25.

2.0 Software Description

2.1 Features of the FORCEbug

- Powerful Command Set including:
  - Test facilities
  - Debugging tools
  - Up/down load utilities
- Line assembler/disassembler fully supporting all 68020/68851/68881 opcodes and addressing modes
- Full support of the Co-Processors 68881 FPCP and 68851 PMMU
- Macro facility for FORCEbug commands
- Recall of last input line using Control A
- System timer with 10msec clock tics

2.2 General Description

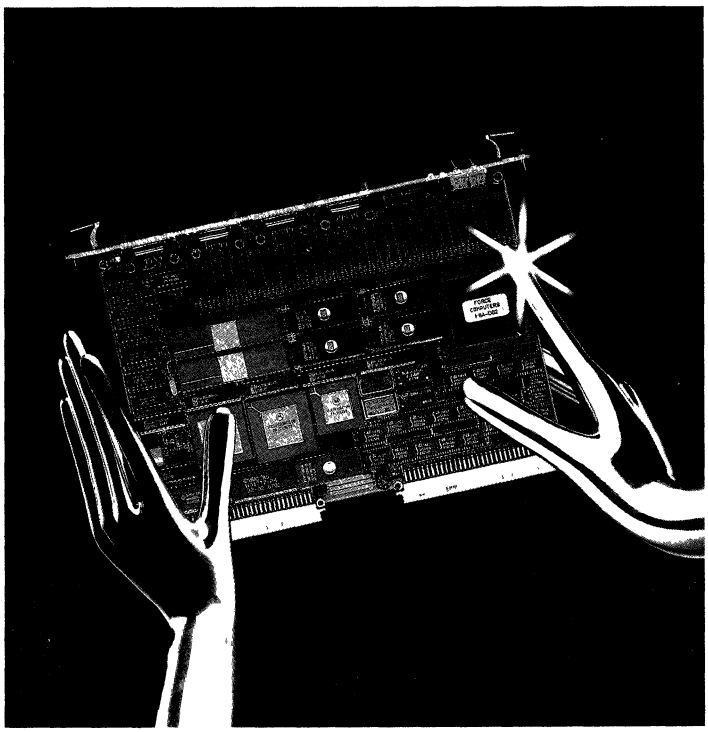
FORCEbug is an EPROM resident debugging package for the SYS68K/CPU-25. It features test facilities, debugging tools, a powerful line assembler/disassembler for the 68020 as well as for use with all FORCEbug commands.
The test facilities allow the user to test and debug hardware on the external bus as well as to prove functionality of all on-board devices.
The debugging tools are well suited to download programs from a host computer and debug them on the board. Included is breakpoint setting, single stepping, tracing if flow is changed, continuous tracing, display and change of all processor registers and memory contents.
With the macro facility, several FORCEbug commands can be combined in one command name and then executed together. It also allows parameter substitution for up to eight parameters.
FORCEbug takes approximately 40Kbyte of EPROM space and resides in a single 27512 EPROM. Additionally, approximately 4Kbyte of read/write memory are used by FORCEbug for vector and parameter storage.

Specifications

		CPU-25	SRAM-22	CPU-25Y	SRAM-22Y
CPU		68020	–	68020	–
Clock Frequency	(MHz)	16.7	–	16.7	–
PMMU		68851	–	68851	–
Clock Frequency	(MHz)	16.7	–	16.7	–
FPCP		68881	–	68881	–
Clock Frequency	(MHz)	16.7	–	16.7	–
FLME Memory Capacity	(Mbyte)	0.5	0.5	2.0	2.0
No. of Wait States		1	1	1	1
EPROM Space	(Kbyte)	64	–	64	–
SRAM Space (main board)	(Kbyte)	32	–	32	–
Serial I/O Interfaces					
RS232		1	–	1	–
RS232/RS422		1	1	1	1
VMEbus Interface		x	–	x	–
A32, A24, A16 : D32, D16, D8, UAT		x	–	x	–
Single Level Arbiter		x	–	x	–
Interrupt Handler (IRQ1-7)		x	–	x	–
68020 FORCEbug Firmware		x	–	x	–
Maximum Power Requirements					
	+ 5V (A)	5.2 (2x)	5.2	5.2 (2x)	5.2
	+12V (A)	0.2	0.1	0.2	0.1
	−12V (A)	0.2	0.1	0.2	0.1
Operating Temperature	(°C) min	0	0	0	0
	(°C) max	50	50	50	50
Storage Temperature	(°C) min	−20	−20	−20	−20
(non-operating)	(°C) max	+85	+85	+85	+85
Relative Humidity	(%) min	10	10	10	10
(non-condensing)	(%) max	90	90	90	90
No. of Used Slots		2	1	2	1

Ordering Information

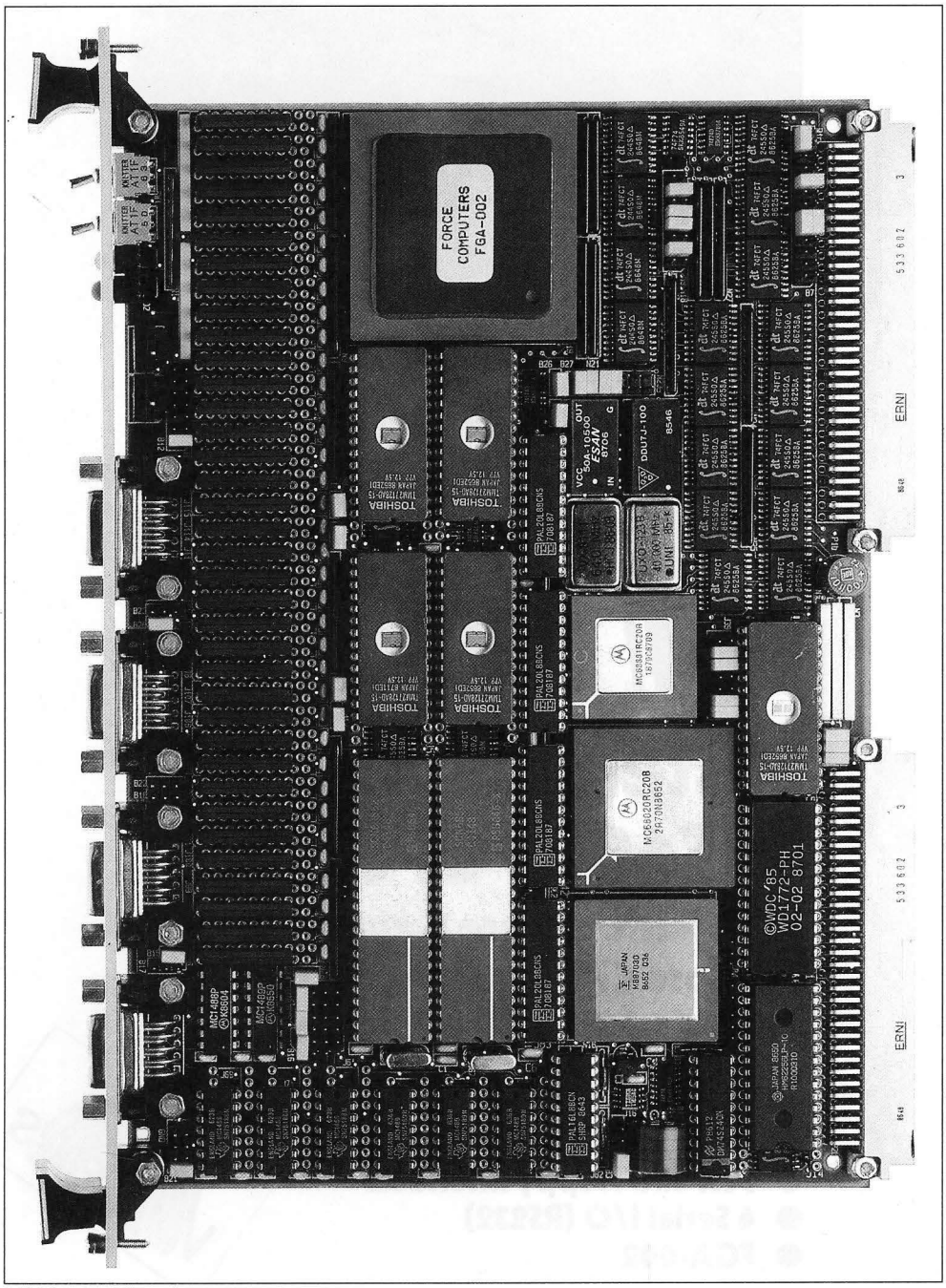
SYS68K/CPU-25 Part no. 101210	68020 CPU board with PMMU, FPCP and 512Kbyte SRAM including documentation
SYS68K/SRAM-22 Part No. 201000	512Kbyte SRAM expansion only for the CPU-25
SYS68K/CPU-25Y Part No. 101211	68020 CPU board with PMMU, FPCP and 2Mbyte SRAM including documentation
SYS68K/SRAM-22Y Part No. 201100	2Mbyte SRAM expansion only for the CPU-25Y
SYS68K/CPU-25 UM Part No. 800126	User's Manual for the CPU25(Y) and SRAM-22(Y) products.



System 68000 VME SYS68K/CPU-26

High Performance General Purpose CPU Board with DPR DMA and Mass Memory Control

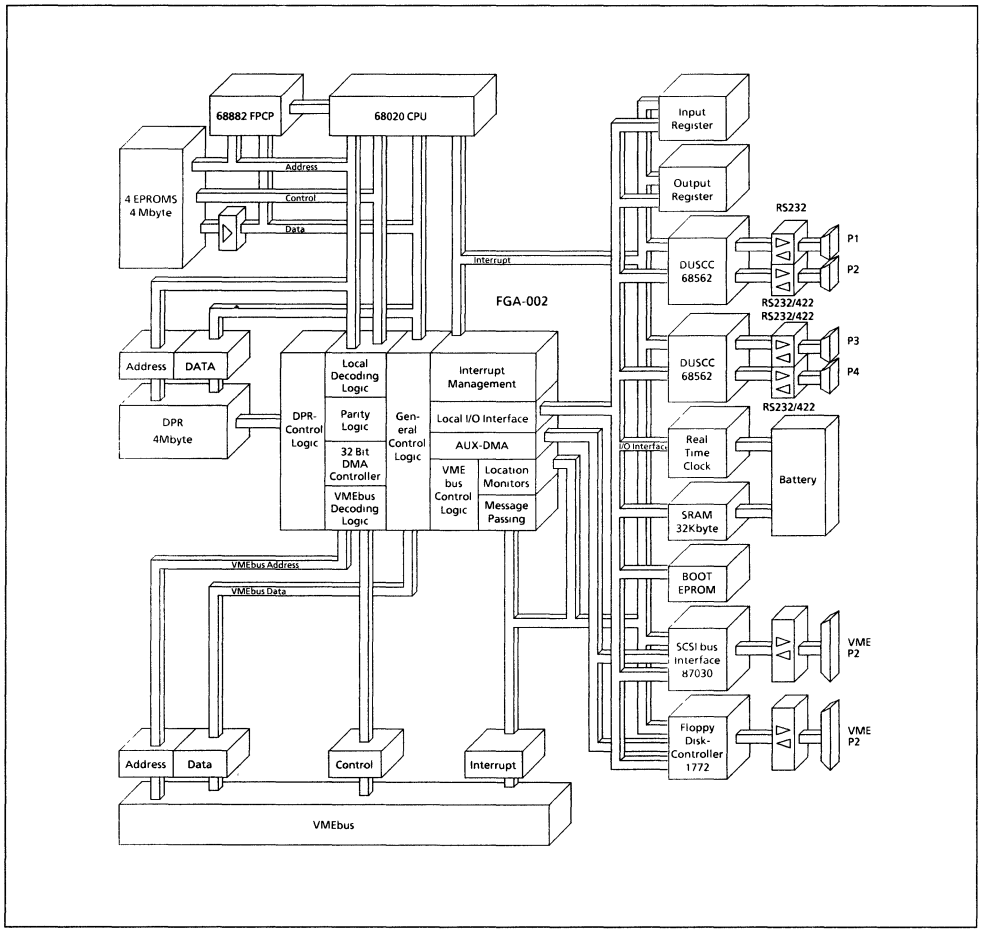
- 16.7 or 20.0 MHz 68020 CPU
- 1 or 4 Mbyte Dual Ported RAM
- SCSI and Floppy Interfaces
- 4 Serial I/O (RS232)
- FGA-002


FORCE
COMPUTERS
FGA-002
TOSHIBA
WD1772-PH
02-02 8701

1. General Description

The SYS68K/CPU-26 is a 68020 based CPU board providing as much as 4 Mbyte of Dual Ported Memory.
A full 32 bit DMA Controller supporting data transfers to/from VMEbus memory as well as to/from local system RAM is provided by a FORCE specific 280 pin Gate Array installed on the board.
The SYS68K/CPU-26 also includes the enhanced Floating Point Co-processor 68882.
Mass memory control is provided through the SCSI Controller and the single chip floppy disk controller. Both are connected to the 32 bit DMA Controller providing highest data throughput to connected mass memory devices.
Serial communication is provided through four fully independent synchronous/asynchronous Multi Protocol Communication Channels.
Additional features include up to 4 Mbyte EPROM capacity (32 bit wide), 32 Kbyte static RAM and a Real Time Clock.
The two independent 8 bit wide VMEbus FORCE Message Broadcast FIFOs and the 16 VMEbus location monitors complete the board.

BLOCK DIAGRAM OF THE SYS68K/CPU-26



2. Features of the SYS68K/CPU-26 Boards:

- 68020 CPU with 16.7 or 20.0 MHz clock frequency.
- 68882 FPCP with 16.7 or 20.0 MHz clock frequency.
- 32 bit high speed DMA Controller for data transfers to/from the Dual Ported RAM and/or to/from the VMEbus memory.
  32 byte internal FIFO for burst DMA.
- 1 or 4 Mbyte of dual gated dynamic RAM accessed from the local CPU with 1 wait state including byte parity generation/check.
- The DRAM is accessible from the VMEbus side via the Gate Array (FGA-002).
- 4 Serial I/O interfaces built with two Dual Universal Serial Communication Controllers.
  1 channel is RS232 and 3 channels are RS232/RS422 compatible.
- Four user EPROM devices providing up to 4 Mbyte capacity using a 32 bit data path.
  1 wait state access possible by using 100 ns devices.
- 1 system EPROM for local booting and initialization of the I/O interface chips and the Gate Array.
- 32 Kbyte of static RAM with on-board battery backup (8 bit data path).
- Real Time Clock with calendar and on-board battery backup.
- SCSI-interface with 2.0/4.0 Mbyte/s data transfer rate using the on-board DMA Controller.
- Floppy disk interface (SA460 compatible) for connection of 3, 3 1/2 and 5 1/4 inch drives.
- Two 24 bit timers with 5 bit prescaler.
- Four 8 bit timers with 8 bit prescaler.
- All local I/O devices are able to interrupt the local CPU on a software programmable level.
- BERR handling fully under software control via different counters for local and VMEbus accesses.
- Full 32 bit VMEbus master/slave interface supporting the following data transfer types:
  Master: A32, A24, A16: D8, D16, D32
  Slave: A32, A24, A16: D8, D16, D32
  Address only
  UAT and read-modify-write cycles are also supported.
- Single level VMEbus arbiter
- SYSCLK driver
- VMEbus Interrupt Handler (IH 1 to 7 dynamic)
- Two independent Message Broadcast FIFOs for simultaneous access of up to 20 CPU boards installed in one rack.
- Support for ACFAIL and SYSFAIL via software programmable IRQ levels.
- Timeout counter (3 seconds), if the board does not receive bus mastership.
- Bus timeout counters for local and VMEbus accesses (15 us).
- VMEPROM, the real time monitor with file manager and Real Time Kernel (PDOS compatible) is installed on each board version.

3. Hardware Description

3.1. The 68020 CPU

The 68020 with its 32 bit address and data paths is installed on the SYS68K/CPU-26 board.
The CPU includes a 256 byte instruction cache which significantly reduces the number of bus cycles needed for program fetches. A CACHE switch on the front panel allows the user to enable or disable the on-chip cache for software debugging purposes.
The 68020 CPU accesses the Dual Ported Memory constantly with the insertion of only one wait state.
Communication of the local I/O interfaces, local SRAM, and the VMEbus interface to the 68020 CPU is provided through the specially designed 280 pin Gate Array called FGA-002.
The EPROM area, the Floating Point Coprocessor, and the dual gated RAM are directly connected to the CPU data and address bus interface (as shown in the block diagram of the SYS68K/CPU-26).
The clock frequency of the 68020 CPU is 16.7 or 20.0 MHz. This offers, in combination with the Dual Ported RAM, a real computing rate of 1.5-4 MIPs.

3.2 The Floating Point Coprocessor

The SYS68K/CPU-26 is fitted with the enhanced 68882 Floating Point Coprocessor (FPCP). The clock frequency of the CPU and the FPCP is identical. The FPCP conforms to the IEEE Floating Point standard 754 (draft 10.0).
Easy floating point operation control to the coprocessor is provided because the intercommunication between the CPU and the FPCP is built in silicon.
An internal register set inside the FPCP of 8 general purpose registers (80 bit wide) yields fast execution times.

Features of the FPCP

- 8 general purpose registers (80 bit, 64 bit Mantissa, 15 bit exponent and one sign bit)
- 67 bit on-chip ALU
- 67 bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 standard (draft 10.0)

- Full support of trigonometrical and logarithmic functions such as:
  SINE and COSINE
  TANGENT and COTANGENT
  Hyperbolic functions (TANGENT, ARC TANGENT, SINE and COSINE)
  Logarithmic functions (4)
  Square root and exponential functions (4)
- The 68882 is fully software compatible to the 68881 FPCP

3.3 The Dual Ported RAM

The SYS68K/CPU-26 contains a dynamic RAM area with a capacity of 1 or 4 Mbyte. The local control logic allows to extend the Dual Ported RAM capacity to 16 Mbyte if the 4 Mbit DRAMs become available. The local CPU and the installed DMA Controller can access the DRAM constantly with only one wait state. RAS and CAS pre-charge times and the clock synchronized control logic allow accesses of the RAM every 200 ns which results in a 4 clock access period for the CPU and the DMA Controller at 20.0 MHz. The bandwidth of the DRAM is therefore 20 Mbyte/s.
Distributed asynchronous refresh is provided every 15 µs and each access cycle is delayed by the insertion of only 4 additional clocks.
The DRAM is also accessible from the VMEbus through the installed FORCE specific Gate Array (FGA-002). Three fully independent access address ranges and address modifier codes are programmable from the local CPU.
The smallest RAM area for a dual gated RAM segment is 4 Kbyte which allows partitioning of the dual gated RAM under software control because the access address ranges can be modified under run time in steps of 4 Kbyte.
The DRAM is accessed from the VMEbus side by requesting local bus mastership from the local CPU via the FGA-002. After the CPU has granted local bus mastership to FGA-002 the access cycle is executed and all data are latched on read cycles, while a normal write cycle is executed and terminated after storing data into the DRAM cells. The read and the write cycle is terminated on the local bus side and FGA-002 immediately releases bus mastership to the CPU while completing the fully asynchronous VMEbus access cycle.
The early completion of the read and write cycle from the VMEbus side to the DRAMs is twice as fast as to wait for the completion of the VMEbus cycle. This allows the local CPU to run with a minimum of overhead.
The SYS68K/CPU-26 includes Byte Parity Check for the local and for the VMEbus accesses. If a parity error is detected on a VMEbus cycle, a BERR is forced to the VMEbus to inform the requestor about the parity error. On all local accesses a normal DSACK will be generated and an interrupt on a software programmable level is also generated if a parity error was detected. For easy software controlled detection of the cycle which caused the parity error the access address is stored inside FGA-002.

3.4 The Local SRAM

A 32 Kbyte static RAM is installed on all SYS68K/CPU-26 board versions and supports data storage during power down phases for up to 1 year. The SRAM is directly connected to the FORCE Gate Array I/O interface. Long, word and byte transfers are automatically controlled via the Gate Array.
Normal read and write operations to the single 32K x 8 SRAM are allowed if the power is within the specification detected by a separate power sensor. Higher density devices (e.g. future 128K x 8 devices) may be inserted as the 32 pin socket allows the use of all JEDEC compatible devices.

3.5 The EPROM Areas

3.5.1 The USER EPROMs

The SYS68K/CPU-26 contains four user EPROM sockets supporting four 28 and/or 32 pin EPROM devices. Maximum data throughput to the 68020 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation if 100 ns devices are installed. The following table lists the supported device types and the memory capacities.

Supported Device Types in the User EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
2764	28	8K x 8	32 Kbyte
27128	28	16K x 8	64 Kbyte
27256	28	32K x 8	128 Kbyte
27512	28	64K x 8	256 Kbyte
271024	32	128K x 8	512 Kbyte
TBD	32	256K x 8	1 Mbyte
TBD	32	512K x 8	2 Mbyte
TBD	32	1M x 8	4 Mbyte

3.5.2 The SYSTEM EPROM

The SYS68K/CPU-26 board contains in addition to the four user EPROMs a single system EPROM to boot the local CPU and initialize all I/O devices and program the board dependent functions of the Gate Array FGA-002. All the presetting and initialization of the I/O devices are made through the system EPROM to ease the adaptation of the complex board functions to the application needs.

3.6 The DMA Controller

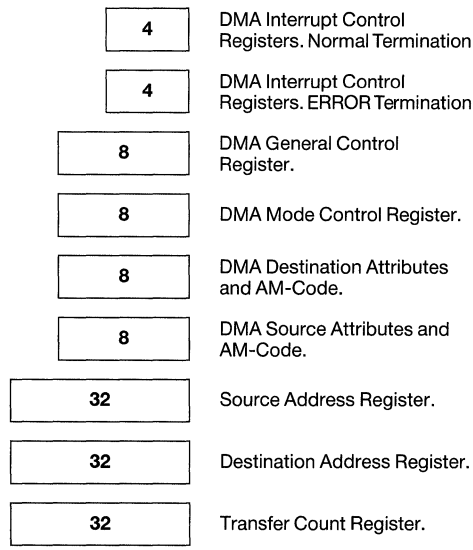
A high speed DMA Controller is installed on the SYS68K/CPU-26. It features a data transfer speed of up to 30 Mbyte/sec on the VMEbus while the data transfer speed to the Dual Ported RAM is 20 Mbyte/sec.
This throughput is the effective transfer speed by transferring 32 bit of data.
The SYS68K/CPU-26 allows the transfer of data between VMEbus memory (2 different memory areas), or between VMEbus memory and the Dual Ported RAM.
DMA execution on the VMEbus is performed without any determination of performance for the local CPU. This allows a program to be run while loading new data into the Dual Ported RAM or writing processed data to global RAM or I/O controller boards. If the data has to be stored or read to/from the Dual Ported RAM the DMA Controller requests bus mastership from the local CPU.
To increase the data throughput and maintain multiprocessor functionality, the DMA Controller operates in burst mode by using its 32 byte FIFO for internal data storage. The read and write operations are executed in 8 cycles fetching 4 byte at a time which result in 8 read cycles followed by 8 write cycles.
This feature significantly increases data throughput and functionality because the local CPU maintains the real-time capabilities by being interruptable during DMA transfers on the VMEbus.
This technology allows data transfer between the Dual Ported RAM and the VMEbus by first collecting the data from the VMEbus, giving up bus mastership and then transferring the data to the Dual Ported RAM. A second VMEbus board is allowed to transfer data on the VMEbus while the DMA Controller transfers the stored data to the Dual Ported RAM.
The bus release functions of the VMEbus mastership for the DMA Controller are software programmable.
The following table shows the DMA data transfer capabilities of the SYS68K/CPU-26 board.

Area 1		Area 2	CPU operation	Note
VMEbus	⟷	VMEbus	100%	–
VMEbus	⟷	DPR	40 – 50%	1
VMEbus	⟷	SCSI	100%	–
VMEbus	⟷	FDC	100%	–
DPR	⟷	SCSI	60 – 80%	2
DPR	⟷	FDC	90%	–

Note 1: CPU operation depends on the transfer speed of the addressed VMEbus board.
Note 2: CPU operation depends on the transfer speed of the SCSI device.

The CPU can operate in parallel to the DMA Controller data transfers because of the 32 byte FIFO and structure of the SYS68K/CPU-26.
CPU operation means that the CPU can access all local I/O devices, the EPROM area as well as the Dual Ported RAM. Only if the CPU wants to access the VMEbus the CPU has to wait until the DMA Controller has finished its data transfers out of its FIFO (max 8 data transfers).
Additionally, the DMA Controller is connected to the on-board SCSI and floppy disk controller allowing data transfer between mass memory devices and the Dual Ported RAM or the VMEbus memory.
The DMA Controller is installed inside the 280 pin Gate Array supporting 32 data and address signals. All addressing modes of the VMEbus are fully software programmable (AM-Codes) for the source and destination address.
The DMA Controller supports aligned and unaligned data transfers to odd and even addresses. The internal control logic first aligns the data transfers to take full advantage of the 32 bit bus structure.
The data transfer speed to the VMEbus depends on the access time of the addressed VMEbus module. The effective transfer speed reaches 15 to 20 Mbyte/s using dynamic memory boards. The maximum speed of 30 Mbyte/s can be achieved if high speed static RAM boards are used.
The following register set shows the structure of the DMA Controller in more detail.

Register Set of the DMA Controller



3.7 The Local I/O Devices

The SYS68K/CPU-26 contains a Gate Array (FGA-002) which builds an 8 bit local I/O interface used to interconnect the CPU and the I/O devices.
The Real Time Clock, serial I/O controllers, control and status registers, SCSI and the floppy disk controller are connected to this local I/O interface.

3.7.1. The Serial I/O Interfaces

Two Dual Universal Serial Communication Controllers (DUSCC 68562) are installed on the SYS68K/CPU-26 to communicate to terminals, computers or other equipment.

Features of the DUSCC

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multi-protocol operation consisting of:
  BOP: HDLC/ADCCP, SDLC, SDLC Loop, X.25 or X.75 link level
  COP: BISYNC, DDCMP, X.21
  ASYNC: 5-8 bit plus optional parity
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1,Manchester
- 4 character receiver and transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter
- Digital phase locked loop
- User programmable counter/timer
- Programmable channel modes full/half duplex, auto echo, local loopback
- Modem control signals for each channel: RTS, CTS, DCD
- CTS and DCD programmable auto enables for Receiver (RX) and Transmitter (TX)
- Programmable interrupt on change of CTS or DCD

The I/O signal assignment of each of the four channels is listed in the following table:

Signal	Input	Output	9 Pin DSUB Connector	Description
DCD	x		1	Data Carrier Detect
RXD	x		2	Receive Data
TXD		x	3	Transmit Data
DTR		x	4	Data Terminal Ready
GND			5	Signal GND
DSR	x	x	6	Data Set Ready
RTS		x	7	Request to Send
CTS	x		8	Clear to Send
–	–	–	9	Not Connected

The first channel is assigned to connect a terminal via the RS232 compatible interface.

The remaining three channels can be configured to work as an RS232 or as an RS422 compatible interface. R/C components can be installed to adopt the various cable lengths and reduce the reflections if the RS422 compatible interface is selected.
The two DUSCCs are able to interrupt the local CPU on a software programmable IRQ-level (1-7) by supplying their own software programmable IRQ vectors (12 in total) to the local CPU.

3.7.2 The Real Time Clock

A software programmable Real Time Clock (RTC-62421) with on-board battery backup is installed on the SYS68K/CPU-26 boards. The features of the Real Time Clock are listed below.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12hr/24hr clock switchover
- Automatic leap year setting
- Interrupt masking
- C-MOS design provides low power consumption during power down mode.

The Real Time Clock is able to interrupt the local CPU on a software programmable level (1 to 7).

3.7.3 The Input/Output Register

A total of three 8 bit input ports and one 8 bit output port are available on the SYS68K/CPU-26.
The first 8 bit input port is connected to the two 4 bit HEX rotary switches provided on the front panel for application dependent settings.
The second 8 bit input port allows the jumper settings to be read (1 or 0) on a jumperfield installed on the PCB. This jumperfield can be used to define the slot number or to define application dependent pre-settings.
The third 8 bit input port allows the memory capacity of the DPR to be read. Each SYS68K/CPU-26 board has three readable status bits describing the memory capacity. In addition, the CPU board type can be read via the remaining 5 bits.
Four LEDs are controlled via the 8 bit output port. The remaining 4 bits are used for board specific control functions.

3.7.4 The Timers

A total of 6 independent timers are available for the user. These timers offer maximum flexibility because each timer can be used to force an interrupt to the CPU on a software programmable IRQ-level (1 to 7).
The first two timers each provide a 24 bit timer with an individual 5 bit prescaler.

The next three timers are 8 bit wide and include an 8 bit prescaler.
The sixth timer is used to generate the SYSFAIL signal to the VMEbus. SYSFAIL can be used in multiprocessor systems to signal that one board has detected a failure. This 6th timer is used as a watchdog timer which needs to be triggered after a software programmed time before signalling SYSFAIL. All installed timers can be used as a watchdog timer or can generate interrupts on a periodical basis.

3.7.5. The Floppy Disk Interface

The SYS68K/CPU-26 contains a single chip floppy controller, the WD1772. The installed driver/receiver circuits allow direct connection of 3, 3 1/2 and 5 1/4 inch floppy drives. All I/O signals are available on the user defined pins of the P2 connector. The I/O signal assignment is compatible to the SYS68K/ISCSI-1 Controller which allows the use of the ISCSI-1BP for inter-connection to mass memory devices.

Features of the WD1772 Controller:

- Built-in data separator
- Built-in write precompensation
- 128, 256, 512 or 1024 byte sector lengths
- 5 1/4" single and double density
- Programmable stepping rate (2 to 6 ms)

The WD1772 Controller is connected via an 8 bit DMAbus to the DMA Controller which allows the transfer of data fully asynchronous to the operation of the CPU.
The floppy disk controller is fully supported from the on-board real time monitor debugger VMEPROM.

3.7.6 The SCSI Interface

The MB87030 SCSI Controller with its up to 4 Mbyte/s data transfer rate is installed on the SYS68K/CPU-26 to interface directly to SCSI Winchester disks, optical drives or tape streamers.

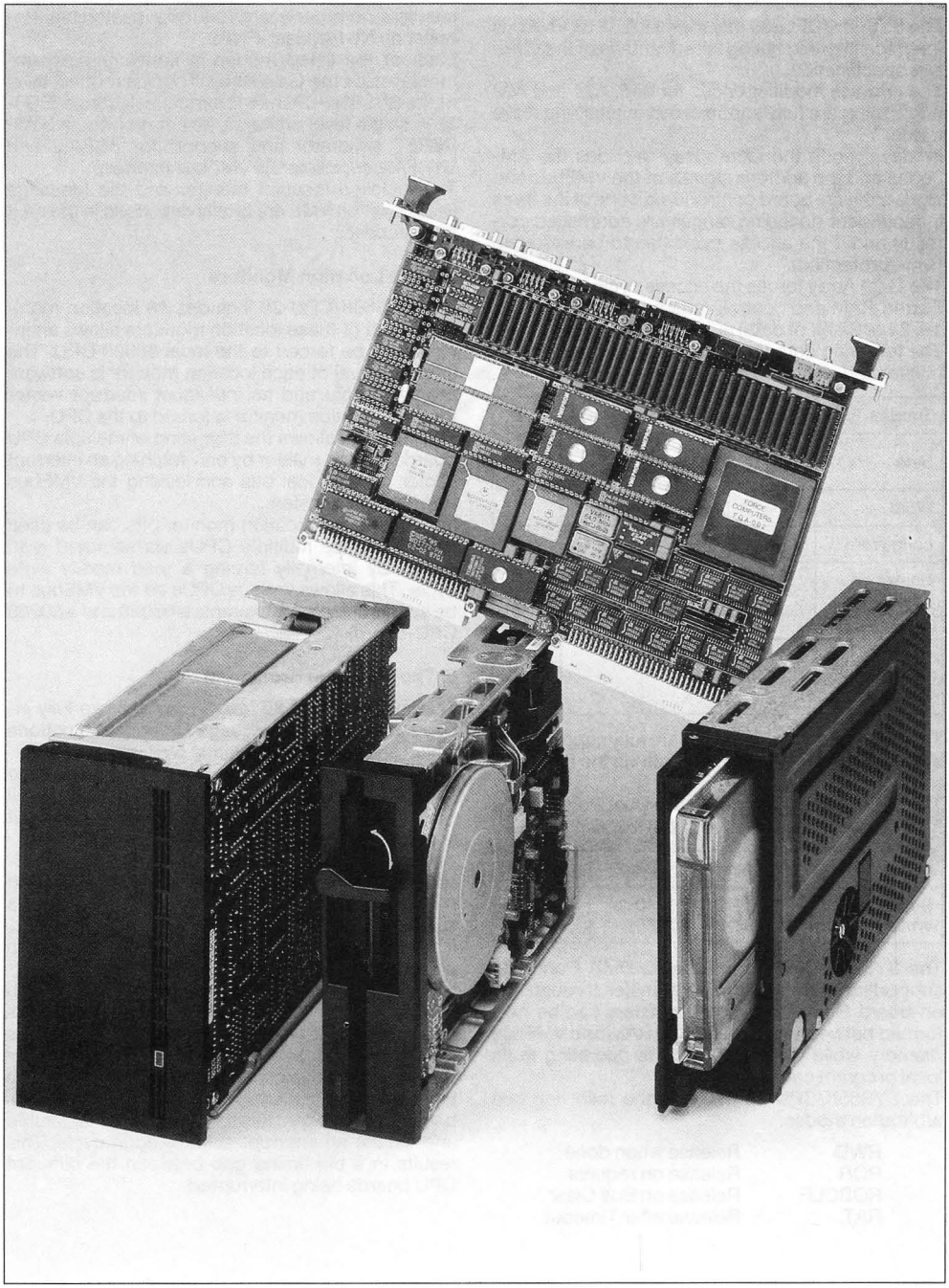
Features of the 87030 SCSI Controller:

- Full support for SCSI control
- Service of either initiator or target device
- Eight byte data buffer register incorporated
- Transfer byte counter (24 bit)
- Independent control and data transfer bus
- Asynchronous data transfer speed 2.0 Mbyte/sec.
- Synchronous data transfer speed up to 4.0 Mbyte/sec.

The SCSI Controller with its 8 bit DMA channel is directly connected to the installed DMA Controller (inside FGA-002) and allows the transfer of data with a maximum speed of 4 Mbyte/s.

The installed DMA Controller includes a 32 byte FIFO which is able to wait until the 32 bytes are filled and then to request local bus mastership to transfer the data in only 8 cycles (32 bit in parallel).
In addition to the 32 byte DMA FIFO, the DMA channel includes a 2nd FIFO (8 byte deep) to fill the DMA FIFO if the DMA transfer to the main memory is taking place. This allows to transfer data on the local DMA bus continuously with a data rate of 4 Mbyte/s without any timing gaps in between.
This technique permits the CPU to perform all real-time capabilities, because the ratio between CPU and DMA operation at the maximum SCSI data transfer rate of 4 Mbyte/s is 63% for the CPU, 20% for the DMA Controller and 7% for the overhead (BR, BG, BGACK handshake). If the data transfer rate is less than 4 Mbyte/s the percentage range of CPU operation increases and the DMAC range decreases while the overhead of 7% remains unchanged.
The I/O signal assignment of the single ended SCSI interface is fully compatible to the assignment of the SYS68K/ISCSI-1/1A board.
The SCSI Controller on the SYS68K/CPU-26 is fully supported from the installed real time monitor debugger VMEPROM.

Picture of the SYS68K/CPU-26 with Mass Memory Drives



4.0 The VMEbus Interface

The SYS68K/CPU-26 includes a full 32 bit VMEbus interface, thereby taking full advantage of the VMEbus specification.
The address modifier codes for A16, A24 and A32 addressing are fully supported in master and slave mode.
In slave mode the Gate Array decodes the AM-codes and the address signals of the VMEbus and signals the on-board control logic if one of the three independent decoding ranges are addressed correctly and if the access cycle has to be executed (write protection).
The Gate Array forces the access cycle to the Dual Ported RAM and controls/adapts the data flow (8, 16, 24 or 32 bit of data) automatically.
The following data transfer types are supported in master and slave Mode:

Transfer Type	D31-D24	D23-D16	D15-D8	D7-D0
Byte			x	x
Word			x	x
Long Word	x	x	x	x
Unaligned Transfers	x	x x x	x x x	x
Read Modify Write	x	x	x x	x x x

The read-modify-write cycles are fully supported to synchronize multiple CPU boards via the Dual Ported RAM.
The access times to access the Dual Ported RAM from the VMEbus are listed in the following table:

Access Times	Min	Type	Max
Read	280 ns	340 ns	440 ns
Write	280 ns	330 ns	430 ns

The SYS68K/CPU-26 includes a DMA Controller supporting high speed data transfer through the on-board Gate Array. DMA transfers can be performed between the Dual Ported RAM and VMEbus memory while the 68020 CPU is operating in its local program cache.
The SYS68K/CPU-26 includes the following bus arbitration modes:

RWD	Release when done
ROR	Release on request
ROBCLR	Release on Bus Clear
RAT	Release after Timeout

In addition the board is able to request bus mastership if no other board requests mastership (Request on No Request-RNR).
Each of the listed modes is software programmable inside the Gate Array. The bus request level of the SYS68K/CPU-26 is jumper selectable (BR0-3). A single level arbiter, a power monitor, a SYSRESET generator and support for ACFAIL and SYSFAIL complete the VMEbus interface.
The installed location monitor and the Message Broadcast on VME are briefly described in the next two sections.

5.0 The Location Monitors

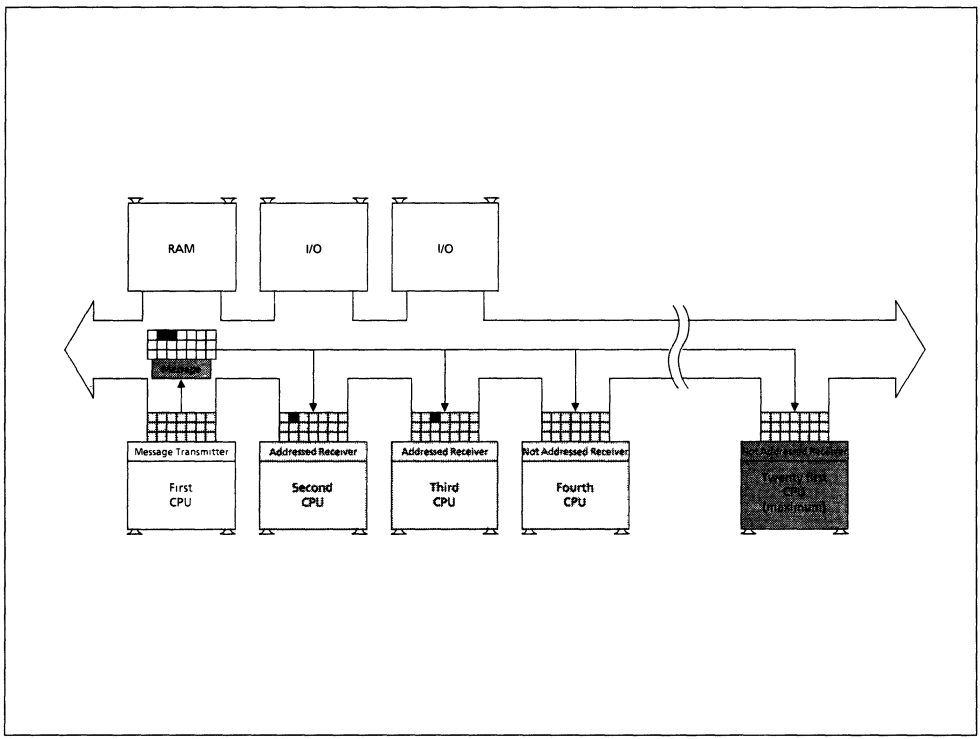
The SYS68K/CPU-26 includes 16 location monitors. Each of these location monitors allows an interrupt to be forced to the local 68020 CPU. The interrupt level of each location monitor is software programmable and an individual interrupt vector for each location monitor is forced to the CPU.
This function allows the triggering of multiple CPU boards via one master by only fetching an interrupt vector on the local bus and leaving the VMEbus free for data transfers.
In addition, the location monitor bits can be used to synchronize multiple CPUs via standard read cycles by internally forcing a read modify write cycle. This allows various CPUs on the VMEbus to be synchronized (for example a 68020 and a 80386 CPU-board).

6. The Message Broadcast

The SYS68K/CPU-26 board provides two fully independent Unique Message Broadcast functions which are implemented within the Gate Array.
The FORCE Message Broadcast (FMB) allows the simultaneous addressing and interrupting of all CPU boards installed in a VMEbus environment. It stores an 8 bit message in an 8 stage deep FIFO.
The Message Broadcast complies fully to the VMEbus specification and minimizes the time overhead required to interrupt all installed CPU boards in a system.
If, for example, 16 boards are installed in a system without FMB, the minimum time required to interrupt all of them is 16 times an access cycle to each of their location monitors. If no location monitors are available then the IRQ signals of the VMEbus have to be used. This results in a maximum number of 7 boards to be synchronized (7 IRQ levels). The time required to interrupt all of them is enormous because each board has to request bus mastership and initiate an interrupt acknowledge cycle. This results in a big timing gap between the different CPU boards being interrupted.

The FMB allows each of the maximum 21 defined boards in the system to be addressed, and to interrupt one, some or all of them, sending the addressed boards an 8 bit message.
The FMB therefore allows any board(s) to be triggered at the same time by fetching the interrupt vector on the local bus leaving the VMEbus free for activities of other bus masters.
Each participant of the FMB stores the single byte message in its 8 byte deep FIFO (inside the Gate Array) and at the same time interrupts the local CPU on a software programmable level (1 to 7).
Each of the two, fully independent FIFOs is designed to allow as many as 8 messages to be sent to multiple participants within a short time frame. The messages can be read from the local CPU after the interrupt has been acknowledged.
The FMB byte is user defined to allow maximum flexibility and to adapt the various requirements to the user needs.
The most important feature of the FMB is that each 32 bit VMEbus based CPU available on the market can send this message byte to a FORCE board supporting the FMB function.
No special motherboard or extended address modifier capabilities are needed because only the defined signals, timings and data transfer types are used to perform the FMB.
Each master can define the board(s) which are to receive the FMB byte on an individual base. The hardware inside the Gate Array decodes the information from the used address and performs the cycle.
The data transfer of the FMB is completed in less than 330 ns for all CPU boards which results in a maximum data bandwidth (theoretical) of 20 x 3 Mbyte/s = 60 Mbyte/s.
A patent on the FMB is pending.
The FORCE Message Broadcast is described in detail in the SYS68K/FMB Data Sheet while the general block diagram is shown below.

BLOCK DIAGRAM OF THE FORCE MESSAGE BROADCAST



7. The Interrupt Structure

The Gate Array installed on the SYS68K/CPU-26 handles all local and VMEbus interrupts. Each interrupt request from the local bus through the SCSI and floppy disk controller, the DUSCC, RTC and the two timers, as well as the Gate Array specific interrupt requests, are combined with the 7 VMEbus interrupt requests.
Each IRQ source including the VMEbus IRQs can be programmed to interrupt the CPU on an individual programmable level (1 to 7).
The Gate Array supports the vector, or initiates an interrupt vector fetch from the I/O device or from the VMEbus.
In addition to the local interrupts, the ACFAIL and SYSFAIL signals can be used to interrupt the CPU on a software programmable level.
This results in a total of 42 individual IRQs handled through the Gate Array on the SYS68K/CPU-26 board.
The Gate Array supplied interrupt vectors have a basic vector and fixed increments for each source. The basic vector is software programmable.

8. The Memory Map

The memory map of the SYS68K/CPU-26 is listed in the following table:

Start Address	End Address	Type
00000000	003FFFFF	Dual Ported Memory (4 Mbyte)
00400000	F9FFFFFF	VMEbus Addresses A32: D32, D24, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area (Slave and Master Mode)
FB000000	FBFEFFFF	VMEbus A24: D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus A16: D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus A24: D16, D8
FCFF0000	FCFFFFFF	VMEbus A16: D16, D8
FD000000	FDFFFFFF	Reserved
FE000000	FEFFFFFF	Reserved

Start Address	End Address	Capacity	Type
FF000000	FF7FFFFF	8 Mbyte	USER – EPROM
FF800000	FFBFFFFF	1 Mbyte	Local I/O
FFC00000	FFCFFFFF	1 Mbyte	LOCAL SRAM
FFD00000	FFDFFFFF	1 Mbyte	Registers of FGA-002
FFE00000	FFEFFFFF	1 Mbyte	SYSTEM EPROM
FFF00000	FFFFFFFF	1 Mbyte	Reserved

9. The VMEPROM

9.1. General Description

VMEPROM is an EPROM based real time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM.
VMEPROM is composed of the powerful PDOS Real Time Kernel and the PDOS file manager. Thus the package provides support of a highly sophisticated Real Time Kernel and an interface to floppy and hard disk drives.
The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition, it includes a powerful line assembler and disassembler for the 68020 and the 68882.

VMEPROM features:

- Real Time Multitasking Kernel supporting up to 64 tasks.
- File management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Line assembler/disassembler with full support of all 68020/68882 instructions.
- Over 20 commands for program debugging, including break-points, tracing, processor register display and modify.
- S-record up/downloading from any port defined in the system.
- Disk support for RAM-disk, floppy and Winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. The local SCSI and floppy disk controller are also supported. VMEPROM also allows disk formatting and initialization.
- Serial I/O support for up to two SIO-2 or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full screen editor.

- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.

9.2. Description of the User Interface of VMEPROM

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple command lines may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

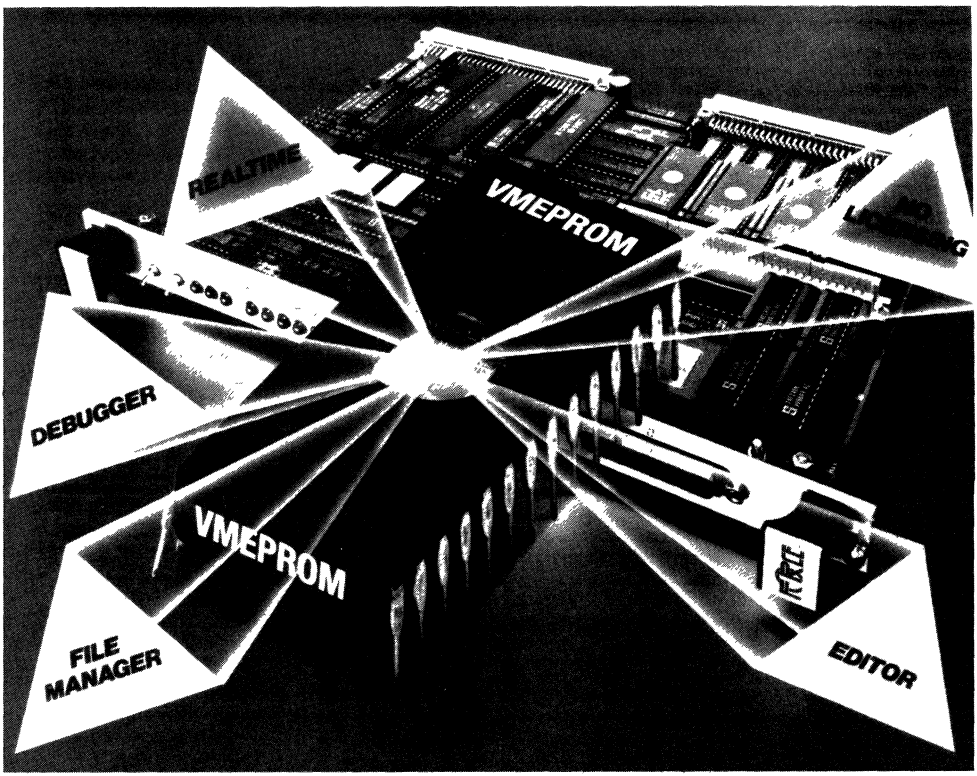
9.3. Description of the Kernel Functions

The kernel of VMEPROM is written in 68020 assembly language for fast and efficient execution. It provides multitasking, system clock,event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously.
Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

9.4. Description of the File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

VMEPROM



9.5. Supported VMEbus Hardware

Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards, and one disk controller.
In addition, EPROM programming is supported by VMEPROM utilizing the SYS68K/RR-2/3 board family.

9.6. Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 40 Kbyte. Small romable applications can be put in EPROMS easily without the overhead of the user interface.

9.7. Development Systems

Currently either one of the FORCE PDOS* or UNIX* System V development stations may be used for software development for VMEPROM.
Compilers, assemblers, and libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.
The support of VMEPROM through other development systems like the IBM-AT or the VAX is under development. These cross-software development packages will include C-compiler, assemblers for the 68020 and libraries to generate codes to run under control of VMEPROM.

9.8. Licensing

No license is required for VMEPROM. VMEPROM is delivered free of charge with every CPU-26 board. For more detailed information please refer to the SYS68K/VMEPROM Data Sheet.

Specification

Function	
68020 CPU Frequency on: CPU-26X CPU-26XA	 16.7 MHz 20.0 MHz
68882 FPCP Frequency on: CPU-26X CPU-26XA/-26ZA	 16.7 MHZ 20.0 MHz
DMA Controller: CPU-26X CPU-26XA/-26ZA Internal FIFO Max. Data Transfer Throughput	16.7 MHz 20.0 MHz 32 byte 30 Mbyte/s
Dual Ported RAM Type Byte Parity DPR Capacity: CPU-26X/-26XA CPU-26ZA No. of Wait States for all CPU and DMA Cycles	DRAM yes 1 Mbyte 4 Mbyte 1
SRAM Capacity On-Board Battery Backup	32 Kbyte yes
No. of EPROM Sockets Data Paths Max. Capacity No. of Wait States (min/max)	4 32 bit 4 Mbyte 1/6
Serial I/O Interfaces (total) Used Controller RS232 compatible RS232/RS422 compatible	4 2 x 68562 1 3
Real Time Clock (Typ) On-Board Battery Backup	62421 yes
SCSI Controller Chip SCSI Interface Data Transfer Rate asynchronous synchronous Connection to DMA Controller I/O Signals routed to	87030 Single ended 2 Mbyte/s 4 Mbyte/s yes P2
Floppy Disk Controller Chip Interface Connection to DMA Controller I/O Signals routed to	1772 SA 460 yes P2

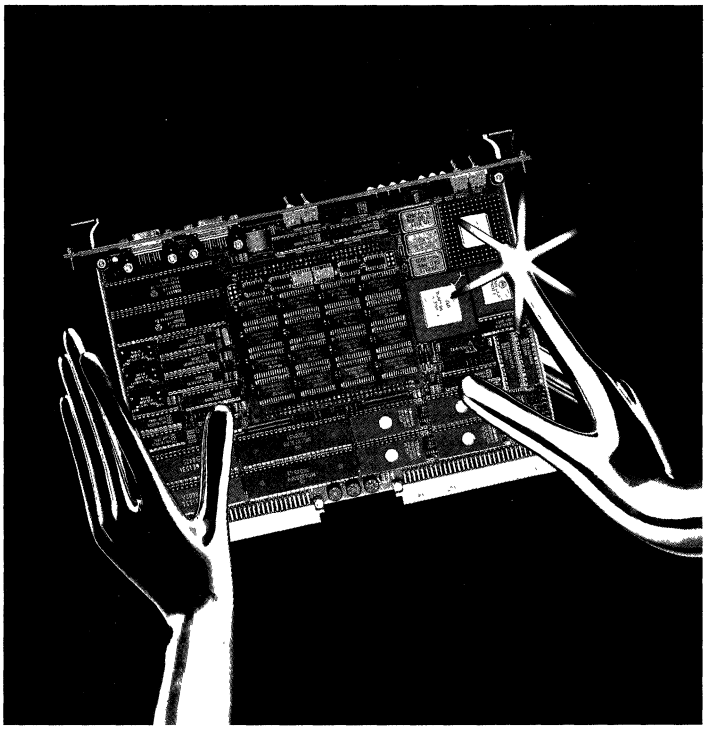
Specification (cont'd)

Function		
VMEbus Interface		
Master: A32, A24, A16:D8, D16, D32, D(0), UAT		yes
Slave: A32, A24, A16:D8, D16, D32, D(0), UAT		yes
Software Programmable Access Address and Address Modifier Code		yes
No. of different Areas for Dual Ported RAM		3
DPR Read Access Time (Typ)		340 ns
Write Access Time (Typ)		330 ns
Single Level Bus Arbiter		yes
SYSCLK Driver		yes
16 Location Monitors		yes
FORCE Message Broadcast		
FMB-FIFO 1		8 byte
FMB-FIFO 2		8 byte
Timers		
24 bit with 5 bit Prescaler		2
8 bit with 8 bit Prescaler		3
8 bit with 8 bit Prescaler (Watchdog Timer for SYSFAIL)		1
VMEbus Interrupt Handler		1 to 7
Local Bus Interrupt Handler		1 to 7
All Sources can be routed to a Software programmable IRQ Level		yes
Total Number of IRQ Sources		42
RESET, TEST, RUN and CACHE Switch		yes
VMEPROM Firmware installed on all Board Versions		128 Kbyte
Power Requirements		
+ 5V min/max		4.2/5.9A
+12V min/max		0.1/0.3A
−12V min/max		0.1/0.3A
Operating Temperature	(Degrees C)	0 to 50
Storage Temperature	(Degrees C)	−40 to 85
Relative Humidity	(non-condensing in %)	0 to 95
Board Dimensions	(mm)	234 x 160
	(in)	9.2 x 6.3
No. of Slots used		1

Ordering Information

SYS68K/CPU-26X Part No. 101130	16.7 MHz 68020 based CPU board with 68882 FPCP, DMAC, 1 Mbyte Dual Ported RAM capacity and VMEPROM. Documentation included.
SYS68K/CPU-26XA Part No. 101131	20.0 MHz 68020 based CPU board with 68882 FPCP, DMAC, 1 Mbyte Dual Ported RAM capacity and VMEPROM. Documentation included.
SYS68K/CPU-26ZA Part No. 101132	20.0 MHz 68020 based CPU board with 68882 FPCP, DMAC, 4 Mbyte Dual Ported RAM capacity and VMEPROM. Documentation included.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM User's Manual excluding the SYS68K/CPU-26 description.
SYS68K/CPU-26/UM Part No. 800141	User's Manual for the SYS68K/CPU-26 products, including VMEPROM User's Manual.

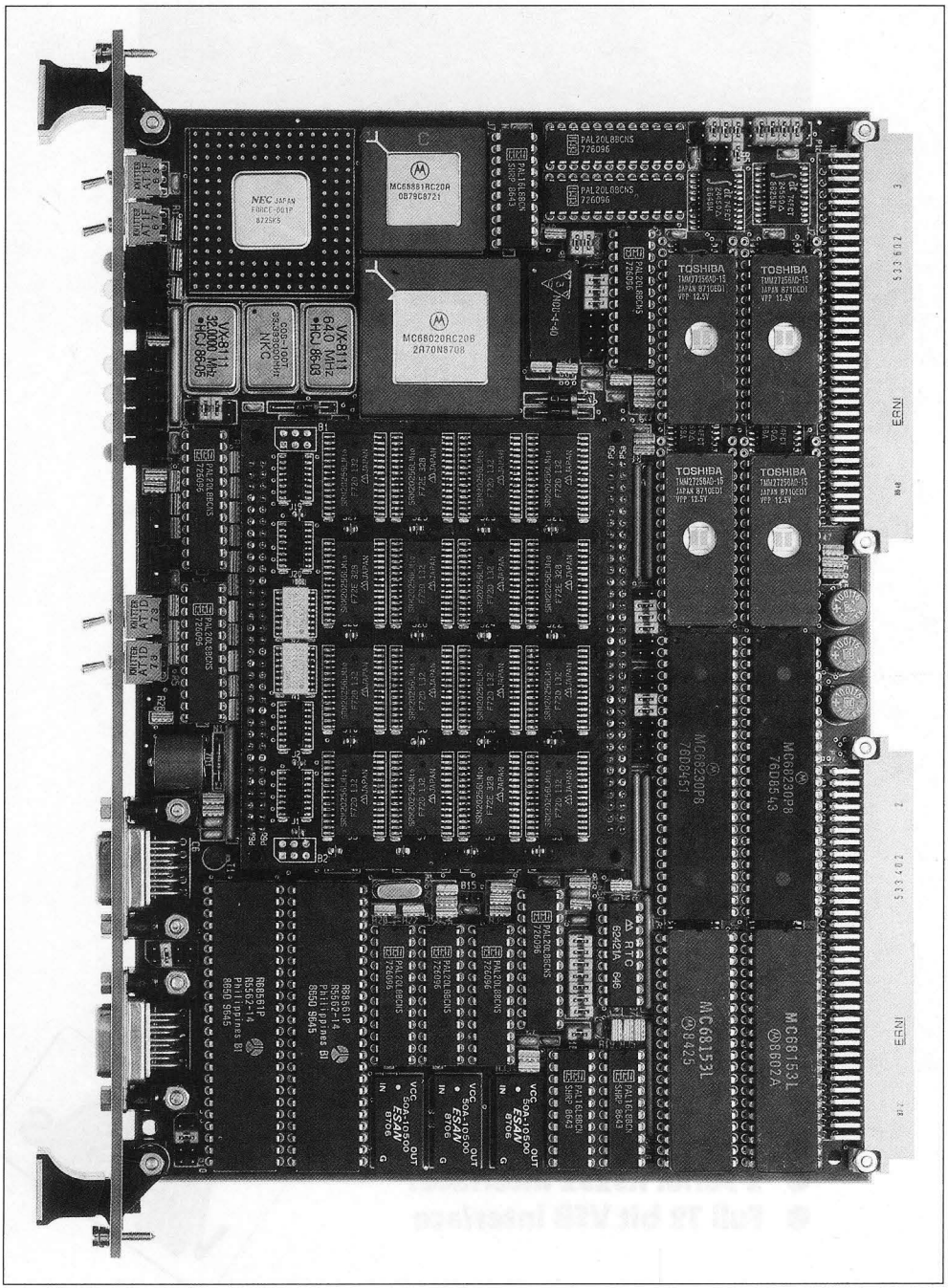
Note: SYS68K/CPU-26 board versions without the 68882 FPCP are available upon special request.



System 68000 VME SYS68K/CPU-29

High Performance 68020 Multiprocessor CPU Board with VSB Interface

- 12.5 MHz to 30 MHz 68020 CPU
- 1 Mbyte 0 Wait State SRAM
- 2 Serial RS232 Interfaces
- Full 32 bit VSB Interface

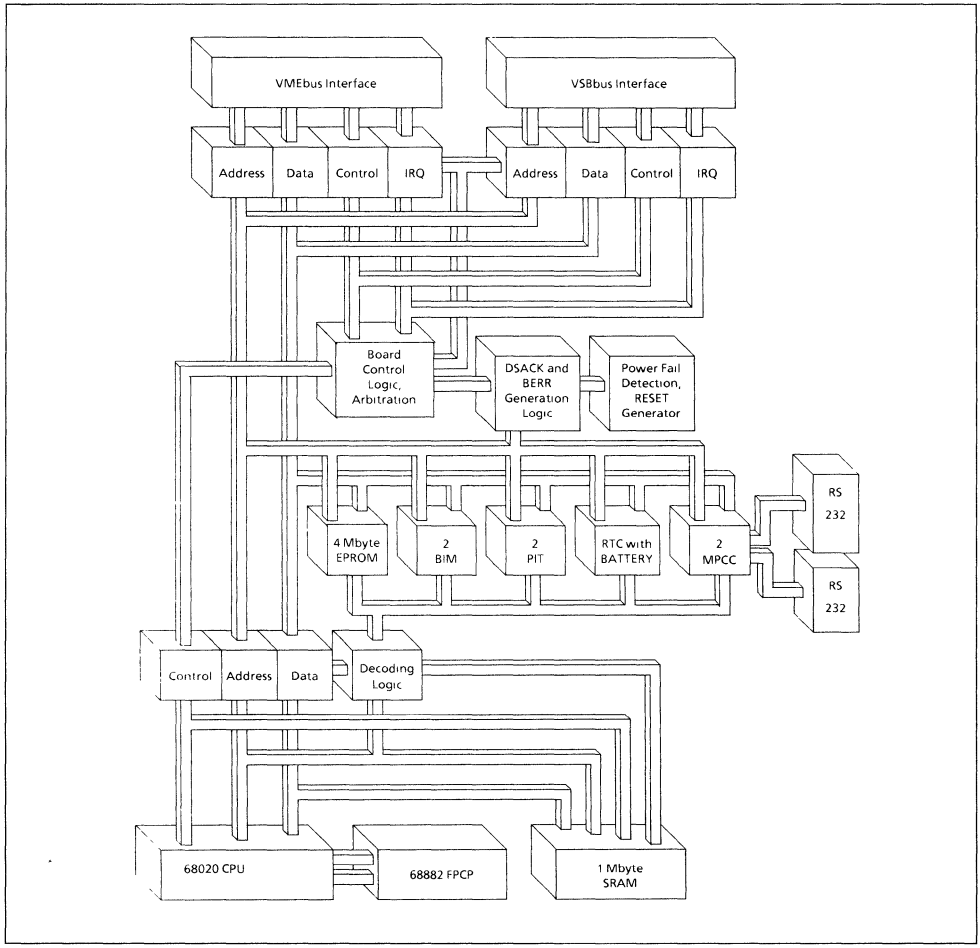


1. General Description

The SYS68K/CPU-29 is an ultra high speed CPU board using a 68020 with a clock frequency of up to 30 MHz. The SYS68K/CPU-29 is fully software compatible to the SYS68K/CPU-21 board. The SYS68K/CPU-29 uses only a single VMEbus slot while the SYS68K/CPU-21 uses 2 to 3 slots.
A static RAM of up to 1 Mbyte capacity can be accessed from the CPU (30 MHz clock frequency) without the insertion of wait states for all read and write cycles. A full 32 bit VSB interface including bus arbitration and interrupt handling is installed on all CPU-29 board versions.

Two serial I/O interfaces (RS232 compatible) provide asynchronous and synchronous data transfer rates of up to 38400 baud or 2 Mbit/sec.
The EPROM area consists of 4 devices supporting the 28 and 32 pin JEDEC standard providing a maximum capacity of 4 Mbyte.
Two fully independent 24 bit timers, a Real Time Clock with an on-board battery backup and the full 32 bit VMEbus master interface complete the board.
In addition, VMEPROM, the PDOS* compatible multi-user real time monitor/debugger is installed on the SYS68K/CPU-29 boards.

BLOCK DIAGRAM OF THE SYS68K/CPU-29XC.



2. Features of the SYS68K/CPU-29

- 68020 CPU (12.5 MHz) on CPU-29XS
  (16.7 MHz) on CPU-29X
  (25.0 MHz) on CPU-29XB
  (30.0 MHz) on CPU-29XC
- 68882 FPCP (12.5 MHz) on CPU-29XS
  (16.7 MHz) on CPU-29X
  (20.0 MHz) on CPU-29XB
  (25.0 MHz) on CPU-29XC
- 68561 Multi Protocol Communication Controllers (2x) for serial I/O data transfers (RS232 compatible)
- 68230 Parallel Interface and Timer devices (2x) for local control and timer function
- 68153 Bus Interrupter Modules (2x) for all local interrupt management
- 1 Mbyte of constant zero wait state static RAM
- Up to 4 Mbyte of EPROM using 4 EPROMs (28 and 32 pin JEDEC standard) building a 32 bit data path
- VSB interface (full 32 bit) with single level arbiter
  A32, A24, A16: D(0), D8, D16, D32
  Unaligned transfers
  Read-modify-write transfers
  Interrupt Handler
- VMEbus interface (full 32 bit) with single level arbiter
  A32, A24, A16: D(0), D8, D16, D32
  Unaligned transfers
  Read-modify-write transfers
- Bus timer
- Power monitor
- SYSRESET generator
- RUN/HALT/CACHE and TEST function switches
- Status indication LEDs
- 2 HEX rotary switches
- Fully software compatible to the SYS68K/CPU-21 CPU board
- VMEPROM installed

3. Hardware Description

3.1 The 68020 CPU

The 68020 with its 32 bit address and data paths is installed on the SYS68K/CPU-29 board.
The CPU includes a 256 byte instruction cache which significantly reduces the number of bus cycles needed for program fetches. A CACHE switch on the front panel allows the user to enable or disable the on-chip cache for software debugging purposes.
The 68020 CPU accesses the static RAM with 30 MHz clock frequency constantly without the insertion of wait states. This allows the design to take full advantage of the throughput of the CPU.

The EPROM area, the Floating Point Coprocessor, the SRAM and the VSB interface are directly connected to the CPU data and address bus interface (as shown in the block diagram of the SYS68K/CPU-29). The clock frequency of the CPU ranges from 12.5 to 30 MHz. This offers, in combination with the SRAM, a real computing rate of 2-6 MIPs.

3.2 The Floating Point Coprocessor

The SYS68K/CPU-29 is fitted with the enhanced 68882 Floating Point Coprocessor (FPCP). The clock frequency of the CPU and the FPCP is identical. The FPCP conforms to the IEEE Floating Point standard 754 (draft 10.0).
Easy floating point operation control to the coprocessor is provided because the intercommunication between the CPU and the FPCP is built in silicon.
An internal register set inside the FPCP of 8 general purpose registers (80 bit wide) yields fast execution times.

Features of the FPCP

- 8 general purpose registers (80 bit, 64 bit Mantissa, 15 bit exponent and one sign bit)
- 67 bit on-chip ALU
- 67 bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 standard (draft 10.0)
- Full support of trigonometrical and logarithmic functions such as:
  SINE and COSINE
  TANGENT and COTANGENT
  Hyperbolic functions (TANGENT, ARC TANGENT, SINE and COSINE)
  Logarithmic functions (4)
  Square root and exponential functions (4)
- The 68882 is fully software compatible to the 68881 FPCP

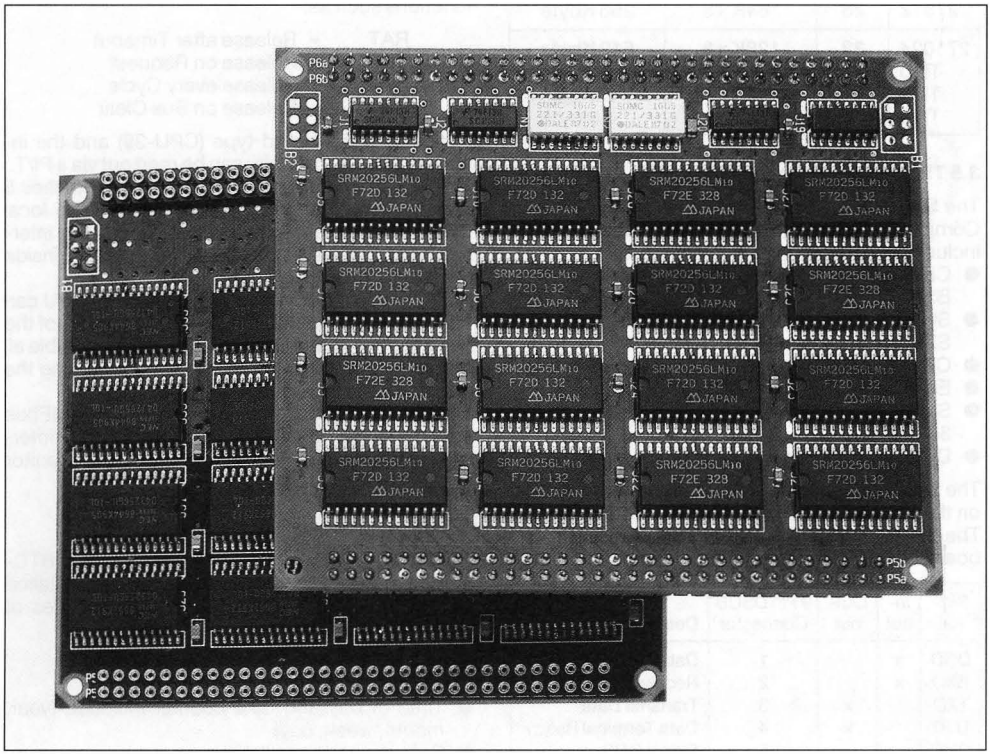
3.3 The Static RAM

The SYS68K/CPU-29 contains a high speed static RAM offering constant no wait state access of all CPU access cycles. This 32 bit wide memory allows to take full advantage of the CPU execution speed. An upgrade to 4 Mbyte RAM is possible, as the RAM is located on a memory module which can easily be replaced if higher density modules become available.
The memory bandwidth of the SYS68K/CPU-29 reaches 40 Mbyte/sec in the 30 MHz version without any need for refresh because static RAMs are used.

The low cost 12.5 and 16.7 MHz versions (SYS68K/CPU-29XS and -29X) access the static RAM (1 M-byte) constantly without the insertion of wait states. On the 25.0 MHz version (SYS68K/CPU-29XB) 100 ns devices (32 K x 8) are installed providing a constant one wait state access to the RAM.
The 30 MHz board version uses 256 K x 1 oriented devices with an access time of 35 ns to guarantee the constant zero wait state operation of the CPU.
The following table lists the CPU board type, the memory capacity as well as the required number of wait states for accessing the SRAM area. In addition, the memory module with the 32 K x 8 oriented devices, together with the on-board control logic, supports a battery backup through the +5V STDBY line.

Board Type	CPU Clock Frequency (MHz)	SRAM Capacity (byte)	No. of Wait States	External Battery Backup Supported
CPU-29XS	12.5	1 M	0	Yes
CPU-29X	16.7	1 M	0	Yes
CPU-29XB	25.0	1 M	1	Yes
CPU-29XC	30.0	1 M	0	No

PHOTO OF THE MEMORY MODULE



3.4 The EPROM Area

The SYS68K/CPU-29 contains four user EPROM sockets supporting 28 or 32 pin EPROM devices. Maximum data throughput to the 68020 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation if 100 ns devices are used. The following table lists the supported device types and the memory capacity.

Supported Device Types in the User EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
2764	28	8K x 8	32 Kbyte
27128	28	16K x 8	64 Kbyte
27256	28	32K x 8	128 Kbyte
27512	28	64K x 8	256 Kbyte
271024	32	128K x 8	512 Kbyte
TBD	32	256K x 8	1 Mbyte
TBD	32	512K x 8	2 Mbyte
TBD	32	1M x 8	4 Mbyte

3.5 The Serial I/O Channels

The SYS68K/CPU-29 contains two Multi Protocol Communication Controllers (MPCC 68561) which include the following protocol features:

- Character oriented protocols
  BSC, DDCMP, X3.28, X.21, ECMA16
- Synchronous bit oriented protocols
  SDLC, HDLC, X.25
- CRC check selectable
- Eight character receiver and buffer registers
- Software programmable baud rate from 110 to 38400 baud
- DC data rate of up to 2 Mbit/s

The two RS232 compatible interfaces are installed on the front panel via two 9 pin D-Sub connectors. The following I/O signals are supported with on-board driver/receiver circuits:

Signal	Input	Output	9 Pin DSUB Connector	Description
DCD	x		1	Data Carrier Detect
RXD	x		2	Receive Data
TXD		x	3	Transmit Data
DTR		x	4	Data Terminal Ready
GND			5	Signal GND
DSR	x	x	6	Data Set Ready
RTS		x	7	Request to Send
CTS	x		8	Clear to Send
–	–	–	9	Not Connected

Each MPCC is able to interrupt the local CPU on a software programmable level. The interrupt vector is also software programmable.

3.6 The Local Control Devices

The SYS68K/CPU-29 contains two independent Parallel Interface and Timer devices (PI/T 68230), for local control and status display.
The clock frequency of each PI/T is 8.064 MHz on all different board versions. Eight control bits can be read via the PI/T port A. These control bits can be set via two HEX rotary switches available on the front panel for manipulation. In addition, 8 status bits can be read out via the second PI/T. The status bits can be used for setting different configurations, defining the slot number in a VMEbus multiprocessor system etc.
The PI/T also allows to program the bus release functions such as:

RAT = Release after Timeout
ROR = Release on Request
REC = Release every Cycle
RBCLR = Release on Bus Clear

In addition, the board type (CPU-29) and the installed memory capacity can be read out via a PI/T.
The two fully independent 24 bit timers with their 5 bit pre-scaler can be used to interrupt the local CPU on a software programmable level. The interrupt vector is also software programmable inside the Bus Interrupter Module.
All of the 7 interrupt request levels of the CPU can be separately enabled or disabled via port B of the first PI/T. For example, this allows you to disable all interrupts on a certain IRQ level by debugging the application software.
The SYSFAIL and ACFAIL signals of the VMEbus are connected to the first PI/T to eventually interrupt the local CPU (if programmed) or to monitor the status of these signals.

3.7 The Real Time Clock

A software programmable Real Time Clock (RTC-62421) with on-board battery backup is installed on the SYS68K/CPU-29 boards. The features of the Real Time Clock are listed below.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12hr/24hr clock switchover
- Automatic leap year setting
- Interrupt masking
- C-MOS design provides low power consumption during power down mode.

The Real Time Clock is able to interrupt the local CPU on a software programmable level (1 to 7).

3.8 The Local Interrupt Sources

Two Bus Interrupter Modules (BIM 68153) are installed on the SYS68K/CPU-29 to manage all the local interrupts.
Each local interrupt source can be routed to one of the seven different IRQ levels of the CPU. The interrupt vector is also software programmable.

Local Interrupt Sources:

1) Test Switch
2) MPCC 1
3) MPCC 2
4) PI/T 1 Timer
5) PI/T 2 Timer
6) RTC
7) VSB-IRQ
8) ACFAIL
9) SYSFAIL

The SYS68K/CPU-29 will only request bus mastership for interrupt acknowledge cycles if the interrupt request was a VMEbus IRQ.

4. The VSB Interface

The SYS68K/CPU-29 board is delivered with a full 32 bit VSB master interface.
Maximum data throughput is provided on the VSB interface by supporting 32 bit of data via the 4 Gbyte address range. The VSB address range is decoded out of the 4 Gbyte address space of the 68020.
The following data transfer types are supported:

A32 : D8, D16, D32
Unaligned Transfers
Address Only Cycles
Read Modify Write Transfers

The VSB interface allows to build contiguous memory beyond the local SRAM. The local control logic provides an access cycle to the VSB interface before addressing the VMEbus. This technique allows an increase of the overall throughput of systems using the secondary bus. If the VSB interface is not required, a jumper setting allows to disable it and forces VMEbus accesses if there is no on-board access cycle detected.
The serial arbiter and the IHP Interrupt Handler complete the VSB interface.

5. The VMEbus Interface

The SYS68K/CPU-29 includes a full 32 bit VMEbus interface, thereby taking full advantage of the VMEbus specification.
The address modifier codes for A16, A24 and A32 addressing are fully supported.

The following data transfer types are supported:

Transfer Type	D31-D24	D23-D16	D15-D8	D7-D0
Byte			x	x
Word			x	x
Long Word	x	x	x	x
Unaligned Transfers	x 	x x x	x x x	 x
Read Modify Write	 x	 x	x x	x x x

The SYS68K/CPU-29 includes the following bus arbitration modes:

RWD	Release when done
ROR	Release on request
RBCLR	Release on Bus Clear
RAT	Release after Timeout

Each of the listed modes is software programmable inside the Gate Array. The bus request level of the SYS68K/CPU-29 is jumper selectable (BR0-3). A single level arbiter, a power monitor, a SYSRESET generator and support for ACFAIL and SYSFAIL complete the VMEbus interface.

6. The VMEPROM

6.1 General Description

VMEPROM is an EPROM based real time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM.
VMEPROM is composed of the powerful PDOS Real Time Kernel and the PDOS file manager. Thus the package provides support of a highly sophisticated Real Time Kernel and an interface to floppy and hard disk drives.
The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition, it includes a powerful line assembler and disassembler for the 68020 and the 68881.

VMEPROM features:

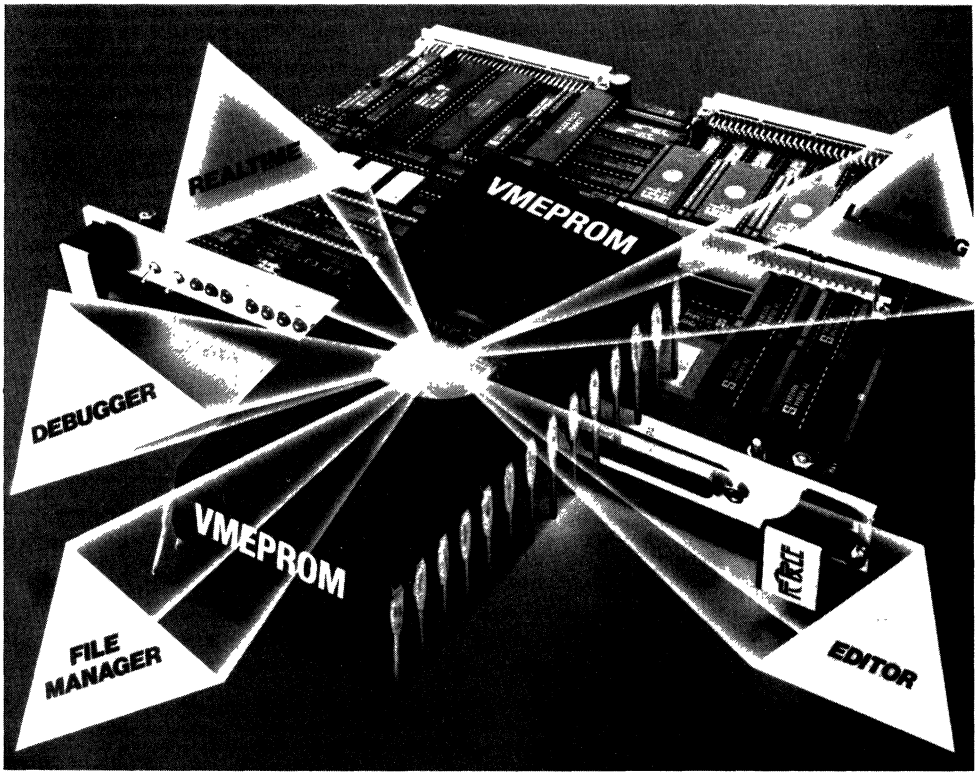
- Real Time Multitasking Kernel supporting up to 64 tasks.
- File management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Line assembler/disassembler with full support of all 68020/68882 instructions.

- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify.
- S-record up/downloading from any port defined in the system.
- Disk support for RAM disk, floppy and Winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. VMEPROM also allows disk formatting and initialization.
- Serial I/O support for up to two SIO or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full screen editor.
- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.

6.2 Description of the User Interface of VMEPROM

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple command lines may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

VMEPROM



6.3 Description of the Kernel Functions

The kernel of VMEPROM is written in 68020 assembly language for fast and efficient execution. It provides multitasking, system clock,event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously.
Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

6.4 Description of the File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

6.5 Supported VMEbus Hardware

Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards and one disk controller.
In addition, EPROM programming is supported by VMEPROM utilizing the SYS68K/RR-2/3 board family.

6.6 Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 40 Kbyte. Small romable applications can be put in EPROMS easily without the overhead of the user interface.

6.7 Development Systems

Currently either one of the FORCE PDOS* or UNIX* System V development stations may be used for software development for VMEPROM.
Compilers, assemblers, and libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.
The support of VMEPROM through other development systems like the IBM-AT or the VAX is under development. These cross-software development packages will include C-compiler, assemblers for the 68020 and libraries to generate codes to run under control of VMEPROM.

6.8 Licensing

No license is required for VMEPROM. VMEPROM is delivered free of charge with every CPU-29 board. For more detailed information please refer to the SYS68K/VMEPROM Data Sheet.

Specifications of the SYS68K/CPU-29

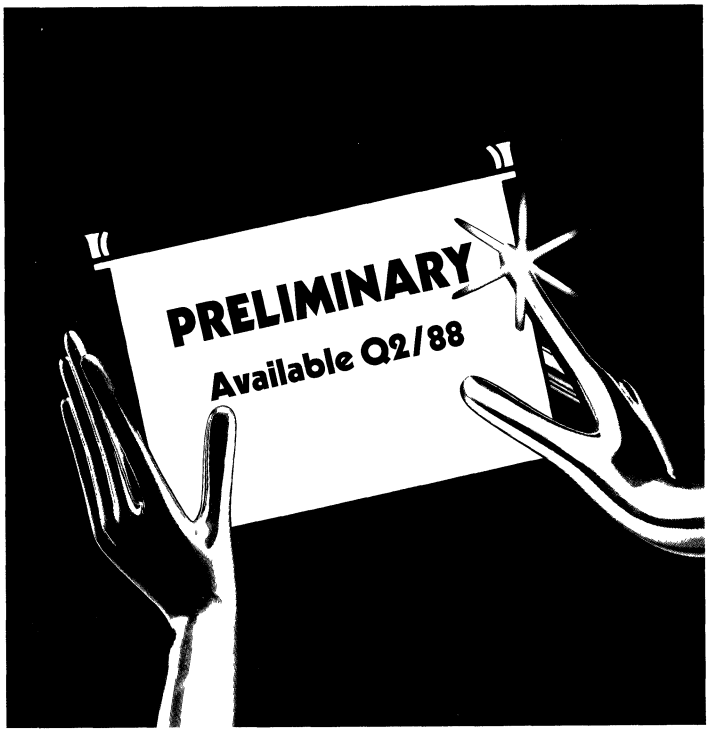
Functions	
68020 CPU Frequency on: CPU-29XS CPU-29X CPU-29XB CPU-29XC	 12.5 MHz 16.7 MHz 25.0 MHz 30.0 MHz
68881/2 FPCP Clock Frequency on: CPU-29XS CPU-29X CPU-29XB CPU-29XC	 12.5 MHz 16.7 MHz 20.0 MHz 25.0 MHz
Local RAM Type Data Path Memory Capacity External Battery backup for SRAMs No. of Wait States – CPU-29XA No. of Wait States – all others	SRAM 32 bit 1 Mbyte Yes (+5V STDBY) 1 (all cycles) 0 (all cycles)
No. of EPROM Sockets Data Path Max. Capacity No. of Wait States (min/max)	4 32 bit 4 Mbyte 1/8
Serial I/O Interfaces Used Controller RS232 compatible	2 2 x 68561 Yes
Real Time Clock (Typ) On-Board Battery Backup	62421 Yes
24 bit Timer	2
VSB Master Interface A32 : D(0), D8, D16, D32 Arbiter Interrupt Handler	Yes Yes Serial IHP
VMEbus Master Interface A32, A24, A16: D(0), D8, D16, D32 Unaligned Data Transfers Read-Modify-Write Cycles Single Level Bus Arbiter VMEbus Interrupt Handler	 Yes Yes Yes Yes IH 1 to 7
RESET, TEST, CACHE, HALT Function Switches	Yes
VMEPROM Firmware on all Board Versions	128 Kbyte
Power Requirements + 5V typ/max +12V typ/max -12V typ/max	 4.3/5.7A 0.1/0.2A 0.1/0.2A

Specification (cont'd)

Function		
Operating Temperature	(Degrees C)	0 to 50
Storage Temperature	(DegreesC)	−40 to 85
Relative Humidity	(noncondensing %)	0 to 95
Board Dimensions	(mm) (in)	234 x 160 9.2 x 6.3
No. of Slots used		1

Ordering Information

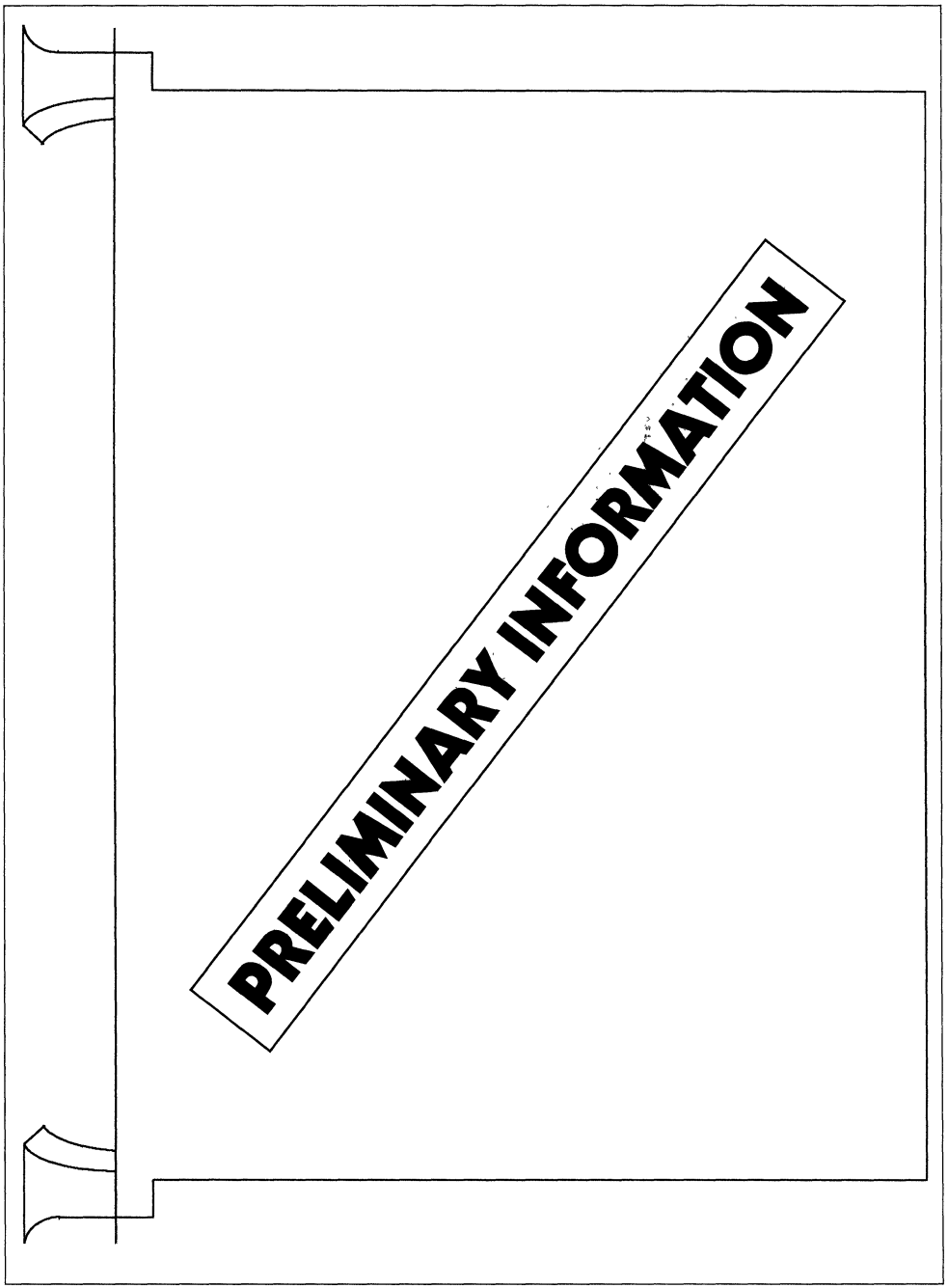
SYS68K/CPU-29XS Part No. 101150	12.5 MHz 68020 CPU board with 1 Mbyte zero wait state SRAM, FPCP and VMEPROM. Documentation included.
SYS68K/CPU-29X Part No. 101152	16.7 MHz 68020 CPU board with 1 Mbyte zero wait state SRAM, FPCP and VMEPROM. Documentation included.
SYS68K/CPU-29XB Part No. 101153	25.0 MHz 68020 CPU board with 1 Mbyte one wait state SRAM, FPCP and VMEPROM. Documentation included.
SYS68K/CPU-29XC Part No. 101154	30.0 MHz 68020 CPU board with 1 Mbyte zero wait state SRAM, FPCP and VMEPROM. Documentation included.
SYS68K/VMEPROM/UM Part No. 800140	User's Manual of VMEPROM
SYS68K/CPU-29/UM Part No. 800145	User's Manual for all SYS68K/CPU-29 board versions. VMEPROM documentation included.



System 68000 VME SYS68K/CPU-30

High Performance General Purpose 68030 CPU Board with DPR DMA and Mass Memory Control

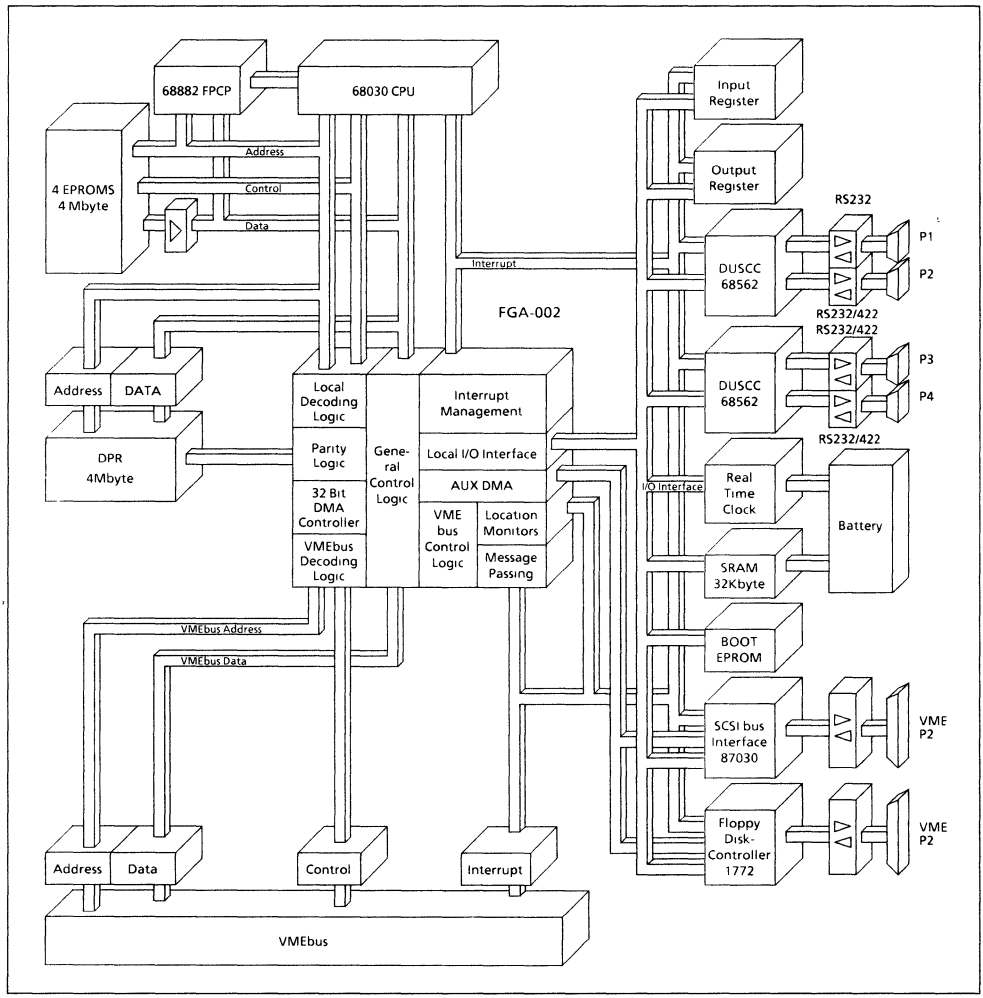
- Up to 4 Mbyte DPR
- SCSI and Floppy Interface
- 4 Serial I/O Interfaces
- 32 bit DMA
- Message Broadcast and Location Monitors


PRELIMINARY INFORMATION

1. General Description

The SYS68K/CPU-30 is a 68030 based CPU board providing as much as 4 Mbyte of Dual Ported Memory.
A full 32 bit DMA Controller supporting data transfers to/from VMEbus memory as well as to/from local system RAM is provided by a FORCE specific 280 pin Gate Array installed on the board.
The SYS68K/CPU-30 also includes the enhanced Floating Point Coprocessor 68882.
Mass memory control is provided through the SCSI Controller and the single chip floppy disk controller. Both are connected to the 32 bit DMA Controller providing highest data throughput to connected mass memory devices.
Serial communication is provided through four fully independent synchronous/asynchronous Multi Protocol Communication Channels.
Additional features include up to 4 Mbyte EPROM capacity (32 bit wide), 32 Kbyte static RAM and a Real Time Clock.
The two independent 8 bit wide VMEbus FORCE Message Broadcast FIFOs and the 16 VMEbus location monitors complete the board.

BLOCK DIAGRAM OF THE SYS68K/CPU-30



2. Features of the SYS68K/CPU-30 Boards:

- 68030 CPU with 16.7 or 20.0 MHz clock frequency.
- 68882 FPCP with 16.7 or 20.0 MHz clock frequency.
- 32 bit high speed DMA Controller for data transfers to/from the Dual Ported RAM and/or to/from the VMEbus memory. 32 byte internal FIFO for burst DMA.
- 1 or 4 Mbyte of dual gated dynamic RAM accessed from the local CPU with 1 wait state including byte parity generation/check.
- The DRAM is accessible from the VMEbus side via the Gate Array (FGA-002).
- 4 Serial I/O interfaces built with two Dual Universal Serial Communication Controllers.
  1 channel is RS232 and 3 channels are RS232/RS422 compatible.
- Four user EPROM devices providing up to 4 Mbyte capacity using a 32 bit data path.
  1 wait state access possible by using 100 ns devices.
- 1 system EPROM for local booting and initialization of the I/O interface chips and the Gate Array.
- 32 Kbyte of static RAM with on-board battery backup (8 bit data path).
- Real Time Clock with calendar and on-board battery backup.
- SCSI-interface with 2.0/4.0 Mbyte/s data transfer rate using the on-board DMA Controller.
- Floppy disk interface (SA460 compatible) for connection of 3, 3 1/2 and 5 1/4 inch drives.
- Two 24 bit timers with 5 bit prescaler.
- Four 8 bit timers with 8 bit prescaler.
- All local I/O devices are able to interrupt the local CPU on a software programmable level.
- BERR handling fully under software control via different counters for local and VMEbus accesses.
- Full 32 bit VMEbus master/slave interface supporting the following data transfer types:
  Master: A32, A24, A16: D8, D16, D32
  Slave: A32, A24, A16: D8, D16, D32
  Address only
  UAT and read-modify-write cycles are also supported.
- Single level VMEbus arbiter
- SYSCLK driver
- VMEbus Interrupt Handler (IH 1 to 7 dynamic)
- Two independent Message Broadcast FIFOs for simultaneous access of up to 20 CPU boards installed in one rack.
- Support for ACFAIL and SYSFAIL via software programmable IRQ levels.
- Timeout counter (3 seconds), if the board does not receive bus mastership.
- Bus timeout counters for local and VMEbus accesses (15 us).
- VMEPROM, the real time monitor with file manager and Real Time Kernel (PDOS compatible) is installed on each board version.

3. Hardware Description

3.1. The 68030 CPU

The 68030 with its 32 bit address and data paths is installed on the SYS68K/CPU-30 board.
The CPU includes a 256 byte instruction- and a 256 byte datacache which significantly reduces the number of bus cycles needed for program fetches. A CACHE switch on the front panel allows the user to enable or disable the on-chip cache for software debugging purposes.
The 68030 CPU accesses the Dual Ported Memory constantly with the insertion of only one wait state through the on chip MMU.
Communication of the local I/O interfaces, local SRAM, and the VMEbus interface to the 68030 CPU is provided through the specially designed 280 pin Gate Array called FGA-002.
The EPROM area, the Floating Point Coprocessor, and the dual gated RAM are directly connected to the CPU data and address bus interface (as shown in the block diagram of the SYS68K/CPU30).
The clock frequency of the 68030 CPU is 16.7 or 20.0 MHz. This offers, in combination with the Dual Ported RAM, a real computing rate of 3 – 7 MIPs.

3.2 The Floating Point Coprocessor

The SYS68K/CPU-30 is fitted with the enhanced 68882 Floating Point Coprocessor (FPCP). The clock frequency of the CPU and the FPCP is identical. The FPCP conforms to the IEEE Floating Point standard 754 (draft 10.0).
Easy floating point operation control to the coprocessor is provided because the intercommunication between the CPU and the FPCP is built in silicon.
An internal register set inside the FPCP of 8 general purpose registers (80 bit wide) yields fast execution times.

Features of the FPCP

- 8 general purpose registers (80 bit, 64 bit Mantissa, 15 bit exponent and one sign bit)
- 67 bit on-chip ALU
- 67 bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 standard (draft 10.0)
- Full support of trigonometrical and logarithmic functions such as:
  SINE and COSINE
  TANGENT and COTANGENT
  Hyperbolic functions (tangent, arc tangent, sine and cosine)
  Logarithmic functions (4)
  Square root and exponential functions (4)

- The 68882 is fully software compatible to the 68881 FPCP

3.3 The Dual Ported RAM

The SYS68K/CPU-30 contains a dynamic RAM area with a capacity of 1 or 4 Mbyte. The local control logic allows to extend the Dual Ported RAM capacity to 16 Mbyte if the 4 Mbit DRAMs become available. The local CPU and the installed DMA Controller can access the DRAM constantly with only one wait state. RAS and CAS pre-charge times and the clock synchronized control logic allow accesses of the RAM every 200 ns which results in a 4 clock access period for the CPU and the DMA Controller at 20.0 MHz. The bandwidth of the DRAM is therefore 20 Mbyte/s.
Distributed asynchronous refresh is provided every 15 us and each access cycle is delayed by the insertion of only 4 additional clocks.
The DRAM is also accessible from the VMEbus through the installed FORCE specific Gate Array (FGA-002). Three fully independent access address ranges and address modifier codes are programmable from the local CPU.
The smallest RAM area for a dual gated RAM segment is 4 Kbyte which allows partitioning of the dual gated RAM under software control because the access address ranges can be modified under run time in steps of 4 Kbyte.
The DRAM is accessed from the VMEbus side by requesting local bus mastership from the local CPU via the FGA-002. After the CPU has granted local bus mastership to FGA-002 the access cycle is executed and all data are latched on read cycles, while a normal write cycle is executed and terminated after storing data into the DRAM cells. The read and the write cycle is terminated on the local bus side and FGA-002 immediately releases bus mastership to the CPU while completing the fully asynchronous VMEbus access cycle.
The early completion of the read and write cycle from the VMEbus side to the DRAMs is twice as fast as to wait for the completion of the VMEbus cycle. This allows the local CPU to run with a minimum of overhead.
The SYS68K/CPU-30 includes byte parity check for the local and for the VMEbus accesses. If a parity error is detected on a VMEbus cycle, a BERR is forced to the VMEbus to inform the requestor about the parity error. On all local accesses a normal DSACK will be generated and an interrupt on a software programmable level is also generated if a parity error was detected. For easy software controlled detection of the cycle which caused the parity error the access address is stored inside FGA-002.

3.4 The Local SRAM

A 32 Kbyte static RAM is installed on all SYS68K/CPU-30 board versions and supports data storage during power down phases for up to 1 year. The SRAM is directly connected to the FORCE Gate Array I/O interface. Long, word and byte transfers are automatically controlled via the Gate Array.
Normal read and write operations to the single 32K x 8 SRAM are allowed if the power is within the specification detected by a separate power sensor.
Higher density devices (e.g. future 128K x 8 devices) may be inserted as the 32 pin socket allows the use of all JEDEC compatible devices.

3.5 The EPROM Areas

3.5.1 The USER EPROMs

The SYS68K/CPU-30 contains four user EPROM sockets supporting four 28 and/or 32 pin EPROM devices. Maximum data throughput to the 68030 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation if 100 ns devices are installed. The following table lists the supported device types and the memory capacities.

Supported Device Types in the User EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
2764	28	8K x 8	32 Kbyte
27128	28	16K x 8	64 Kbyte
27256	28	32K x 8	128 Kbyte
27512	28	64K x 8	256 Kbyte
271024	32	128K x 8	512 Kbyte
TBD	32	256K x 8	1 Mbyte
TBD	32	512K x 8	2 Mbyte
TBD	32	1M x 8	4 Mbyte

3.5.2 The SYSTEM EPROM

The SYS68K/CPU-30 board contains in addition to the four user EPROMs a single system EPROM to boot the local CPU and initialize all I/O devices and program the board dependent functions of the Gate Array FGA-002. All the presetting and initialization of the I/O devices are made through the system EPROM to ease the adaptation of the complex board functions to the application needs.

3.6 The DMA Controller

A high speed DMA Controller is installed on the SYS68K/CPU-30. It features a data transfer speed of up to 30 Mbyte/sec on the VMEbus while the data transfer speed to the Dual Ported RAM is 20 Mbyte/sec.

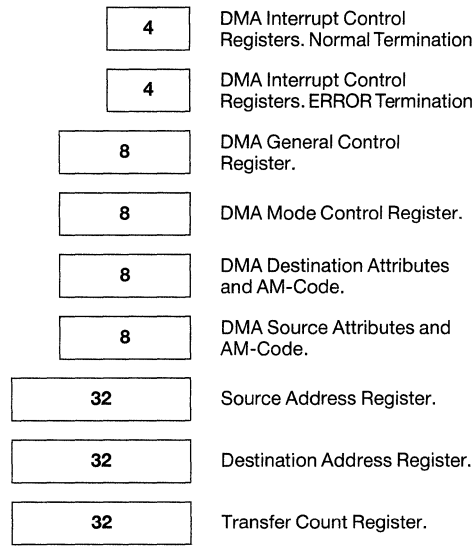
This throughput is the effective transfer speed by transferring 32 bit of data.
The SYS68K/CPU-30 allows the transfer of data between VMEbus memory (2 different memory areas), or between VMEbus memory and the Dual Ported RAM.
DMA execution on the VMEbus is performed without any degredation of performance for the local CPU. This allows a program to be run while loading new data into the Dual Ported RAM or writing processed data to global RAM or I/O controller boards.
If the data has to be stored or read to/from the Dual Ported RAM the DMA Controller requests bus mastership from the local CPU.
To increase the data throughput and maintain multiprocessor functionality, the DMA Controller operates in burst mode by using its 32 byte FIFO for internal data storage. The read and write operations are executed in 8 cycles fetching 4 byte at a time which result in 8 read cycles followed by 8 write cycles.
This feature significantly increases data throughput and functionality because the local CPU maintains the real-time capabilities by being interruptable during DMA transfers on the VMEbus.
This technology allows data transfer between the Dual Ported RAM and the VMEbus by first collecting the data from the VMEbus, giving up bus mastership and then transferring the data to the Dual Ported RAM. A second VMEbus board is allowed to transfer data on the VMEbus while the DMA Controller transfers the stored data to the Dual Ported RAM.
The bus release functions of the VMEbus mastership for the DMA Controller are software programmable.
The following table shows the DMA data transfer capabilities of the SYS68K/CPU-30 board.

Area 1		Area 2	CPU operation	Note
VMEbus	⟷	VMEbus	100%	–
VMEbus	⟷	DPR	40 – 50%	1
VMEbus	⟷	SCSI	100%	–
VMEbus	⟷	FDC	100%	–
DPR	⟷	SCSI	60 – 80%	2
DPR	⟷	FDC	90%	–

Note 1: CPU operation depends on the transfer speed of the addressed VMEbus board.
Note 2: CPU operation depends on the transfer speed of the SCSI device.

The CPU can operate in parallel to the DMA Controller data transfers because of the 32 byte FIFO and structure of the SYS68K/CPU-30.
CPU operation means that the CPU can access all local I/O devices, the EPROM area as well as the Dual Ported RAM. Only if the CPU wants to access the VMEbus the CPU has to wait until the DMA Controller has finished its data transfers out of its FIFO (max 8 data transfers).
Additionally, the DMA Controller is connected to the on-board SCSI and floppy disk controller allowing data transfer between mass memory devices and the dual ported RAM or the VMEbus memory.
The DMA Controller is installed inside the 280 pin Gate Array supporting 32 data and address signals. All addressing modes of the VMEbus are fully software programmable (AM-Codes) for the source and destination address.
The DMA Controller supports aligned and unaligned data transfers to odd and even addresses. The internal control logic first aligns the data transfers to take full advantage of the 32 bit bus structure.
The data transfer speed to the VMEbus depends on the access time of the addressed VMEbus module. The effective transfer speed reaches 15 to 20 Mbyte/s using dynamic memory boards. The maximum speed of 30 Mbyte/s can be achieved if high speed static RAM boards are used.
The following register set shows the structure of the DMA Controller in more detail.

Register Set of the DMA Controller



3.7 The Local I/O Devices

The SYS68K/CPU-30 contains a Gate Array (FGA-002) which builds an 8 bit local I/O interface used to interconnect the CPU and the I/O devices.
The Real Time Clock, serial I/O controllers, control and status registers, SCSI and the floppy disk controller are connected to this local I/O interface.

3.7.1 The Serial I/O Interfaces

Two Dual Universal Serial Communication Controllers (DUSCC 68562) are installed on the SYS68K/CPU-30 to communicate to terminals, computers or other equipment.

Features of the DUSCC

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multi-protocol operation consisting of:
  BOP: HDLC/ADCCP, SDLC, SDLC Loop, X.25 or X.75 link level
  COP: BISYNC, DDCMP, X.21
  ASYNC: 5-8 bit plus optional parity
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1, Manchester
- 4 character receiver and transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter
- Digital phase locked loop
- User programmable counter/timer
- Programmable channel modes full/half duplex, auto echo, local loopback
- Modem control signals for each channel: RTS, CTS, DCD
- CTS and DCD programmable auto enables for Receiver (RX) and Transmitter (TX)
- Programmable interrupt on change of CTS or DCD

The I/O signal assignment of each of the four channels is listed in the following table:

Signal	Input	Output	9 Pin DSUB Connector	Description
DCD	x		1	Data Carrier Detect
RXD	x		2	Receive Data
TXD		x	3	Transmit Data
DTR		x	4	Data Terminal Ready
GND			5	Signal GND
DSR	x	x	6	Data Set Ready
RTS		x	7	Request to Send
CTS	x		8	Clear to Send
–	–	–	9	Not Connected

The first channel is assigned to connect a terminal via the RS232 compatible interface.
The remaining three channels can be configured to work as an RS232 or as an RS422 compatible interface. R/C components can be installed to adopt the various cable lengths and reduce the reflections if the RS422 compatible interface is selected.
The two DUSCCs are able to interrupt the local CPU on a software programmable IRQ-level (1 – 7) by supplying their own software programmable IRQ vectors (12 in total) to the local CPU.

3.7.2 The Real Time Clock

A software programmable Real Time Clock (RTC-62421) with onboard battery backup is installed on the SYS68K/CPU-30 boards. The features of the Real Time Clock are listed below.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12hr/24hr clock switchover
- Automatic leap year setting
- Interrupt masking
- C-MOS design provides low power consumption during power down mode.

The Real Time Clock is able to interrupt the local CPU on a software programmable level (1 to 7).

3.7.3 The Input/Output Register

A total of three 8 bit input ports and one 8 bit output port are available on the SYS68K/CPU-30.
The first 8 bit input port is connected to the two 4 bit HEX rotary switches provided on the front panel for application dependent settings.
The second 8 bit input port allows the jumper settings to be read (1 or 0) on a jumperfield installed on the PCB. This jumperfield can be used to define the slot number or to define application dependent presettings.
The third 8 bit input port allows the memory capacity of the DPR to be read. Each SYS68K/CPU-30 board has three readable status bits describing the memory capacity. In addition, the CPU board type can be read via the remaining 5 bits.
Four LEDs are controlled via the 8 bit output port. The remaining 4 bits are used for board specific control functions.

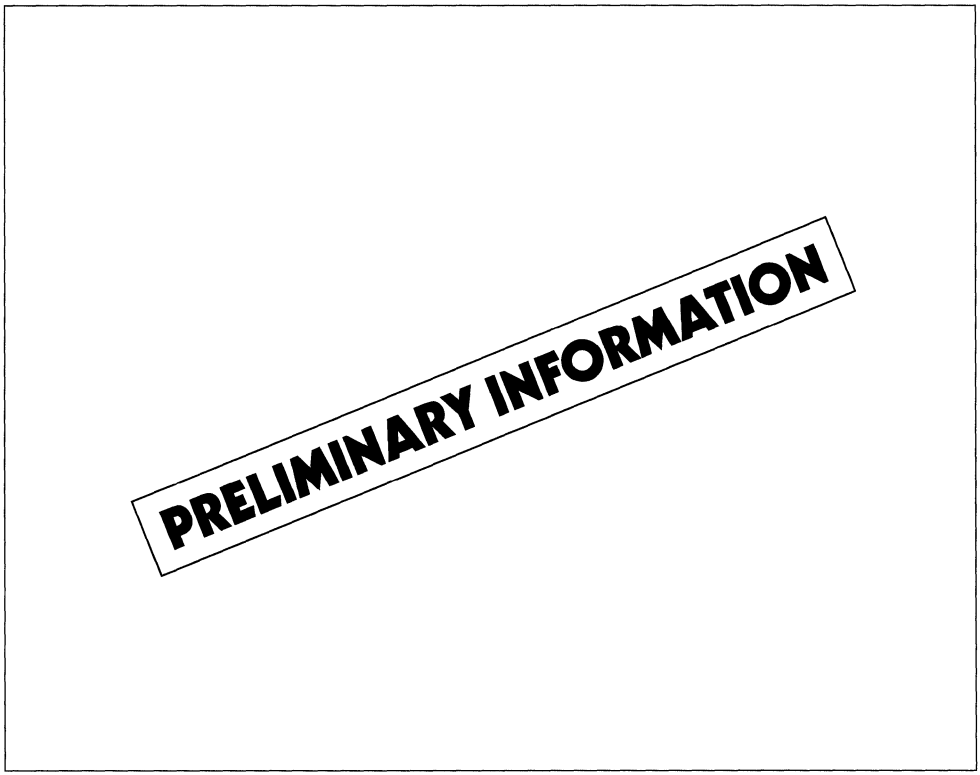
3.7.4 The Timers

A total of 6 independent timers are available for the user. These timers offer maximum flexibility because each timer can be used to force an interrupt to the CPU on a software programmable IRQ-level (1 to 7).
The first two timers each provide a 24 bit timer with an individual 5 bit prescaler.
The next three timers are 8 bit wide and include an 8 bit prescaler.
The sixth timer is used to generate the SYSFAIL signal to the VMEbus. SYSFAIL can be used in multiprocessor systems to signal that one board has detected a failure. This 6th timer is used as a watchdog timer which needs to be triggered after a software programmed time before signalling SYSFAIL.
All installed timers can be used as a watchdog timer or can generate interrupts on a periodical basis.

3.7.5. The Floppy Disk Interface

The SYS68K/CPU-30 contains a single chip floppy controller, the WD1772. The installed driver/receiver circuits allow direct connection of 3, 3 1/2 and 5 1/4 inch floppy drives. All I/O signals are available on the user defined pins of the P2 connector. The I/O signal assignment is compatible to the SYS68K/ISCSI-1 Controller which allows the use of the ISCSI-1BP for inter-connection to mass memory devices shown in the following picture.

Picture of the SYS68K/CPU-30 and Mass Memory Drives



Features of the WD1772 Controller:

- Built-in data separator
- Built-in write precompensation
- 128, 256, 512 or 1024 byte sector lengths
- 5 1/4" single and double density
- Programmable stepping rate (2 to 6 ms)

The WD1772 Controller is connected via an 8 bit DMAbus to the DMA Controller which allows the transfer of data fully asynchronous to the operation of the CPU.
The floppy disk controller is fully supported from the on-board real time monitor debugger VMEPROM.

3.7.6 The SCSI Interface

The **MB87030** SCSI Controller with its up to 4 Mbyte/s data transfer rate is installed on the SYS68K/CPU-30 to interface directly to SCSI Winchester disks, optical drives or tape streamers.

Features of the 87030 SCSI Controller:

- Full support for SCSI control
- Service of either initiator or target device
- Eight byte data buffer register incorporated
- Transfer byte counter (24 bit)
- Independent control and data transfer bus
- Asynchronous data transfer speed 2.0 Mbyte/sec.
- Synchronous data transfer speed up to 4.0 Mbyte/sec.

The SCSI Controller with its 8 bit DMA channel is directly connected to the installed DMA Controller (inside FGA-002) and allows the transfer of data with a maximum speed of 4 Mbyte/s.
The installed DMA Controller includes a 32 byte FIFO which is able to wait until the 32 bytes are filled and then to request local bus mastership to transfer the data in only 8 cycles (32 bit in parallel).
In addition to the 32 byte DMA FIFO, the DMA channel includes a 2nd FIFO (8 byte deep) to fill the DMA FIFO if the DMA transfer to the main memory is taking place. This allows to transfer data on the local DMA bus continuously with a data rate of 4 Mbyte/s without any timing gaps in between.
This technique permits the CPU to perform all real-time capabilities, because the ratio between CPU and DMA operation at the maximum SCSI data transfer rate of 4 Mbyte/s is 63% for the CPU, 20% for the DMA Controller and 7% for the overhead (BR, BG, BGACK handshake). If the data transfer rate is less than 4 Mbyte/s the percentage range of CPU operation increases and the DMAC range decreases while the overhead of 7% remains unchanged.
The I/O signal assignment of the single ended SCSI interface is fully compatible to the assignment of the SYS68K/ISCSI-1/1A board.

The SCSI Controller on the SYS68K/CPU-30 is fully supported from the installed real time monitor debugger VMEPROM.

4. The VMEbus Interface

The SYS68K/CPU-30 includes a full 32 bit VMEbus interface, thereby taking full advantage of the VMEbus specification.
The address modifier codes for A16, A24 and A32 addressing are fully supported in master and slave mode.
In slave mode the Gate Array decodes the AM-codes and the address signals of the VMEbus and signals the on-board control logic if one of the three independent decoding ranges are addressed correctly and if the access cycle has to be executed (write protection).
The Gate Array forces the access cycle to the Dual Ported RAM and controls/adapts the data flow (8, 16, 24 or 32 bit of data) automatically.
The following data transfer types are supported in master and slave Mode:

Transfer Type	D31-D24	D23-D16	D15-D8	D7-D0
Byte			x	x
Word			x	x
Long Word	x	x	x	x
Unaligned Transfers	x	x x x	x x x	x
Read Modify Write	x	x	x x	x x x

The read-modify-write cycles are fully supported to synchronize multiple CPU boards via the Dual Ported RAM.
The access times to access the Dual Ported RAM from the VMEbus are listed in the following table:

Access Times	Min	Type	Max
Read Write	280 ns 280 ns	340 ns 330 ns	440 ns 430 ns

The SYS68K/CPU-30 includes a DMA Controller supporting high speed data transfer through the on-board Gate Array. DMA transfers can be performed between the Dual Ported RAM and VMEbus memory while the 68030 CPU is operating in its local program cache.

The SYS68K/CPU-30 includes the following bus arbitration modes:

RWD	Release when done
ROR	Release on request
ROBCLR	Release on Bus Clear
RAT	Release after Timeout

In addition the board is able to request bus mastership if no other board requests mastership (Request on No Request-RNR).
Each of the listed modes is software programmable inside the Gate Array. The bus request level of the SYS68K/CPU-30 is jumper selectable (BR0-3). A single level arbiter, a power monitor, a SYSRESET generator and support for ACFAIL and SYSFAIL complete the VMEbus interface.
The installed location monitor and the Message Broadcast on VME are briefly described in the next two sections.

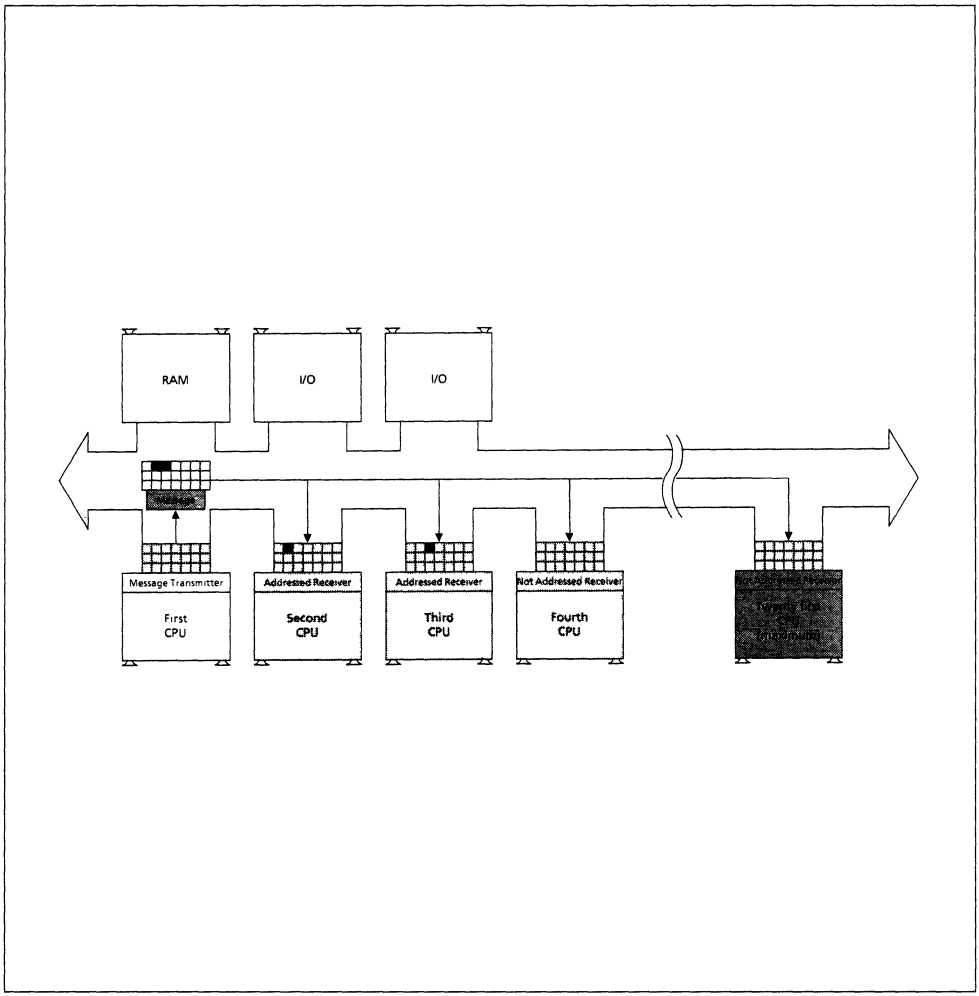
5. The Location Monitors

The SYS68K/CPU-30 includes 16 location monitors. Each of these location monitors allows an interrupt to be forced to the local 68030 CPU. The interrupt level of each location monitor is software programmable and an individual interrupt vector for each location monitor is forced to the CPU.
This function allows the triggering of multiple CPU boards via one master by only fetching an interrupt vector on the local bus and leaving the VMEbus free for data transfers.
In addition, the location monitor bits can be used to synchronize multiple CPUs via standard read cycles by internally forcing a read modify write cycle. This allows various CPUs on the VMEbus to be synchronized (for example a 68030 and a 80386 CPU-board).

6. The Message Broadcast

The SYS68K/CPU-30 board provides two fully independent Unique Message Broadcast functions which are implemented within the Gate Array.
The FORCE Message Broadcast (FMB) allows the simultaneous addressing and interrupting of all CPU boards installed in a VMEbus environment. It stores an 8 bit message in an 8 stage deep FIFO.
The Message Broadcast complies fully to the VMEbus specification and minimizes the time overhead required to interrupt all installed CPU boards in a system.
If, for example, 16 boards are installed in a system without FMB, the minimum time required to interrupt all of them is 16 times an access cycle to each of their location monitors. If no location monitors are available then the IRQ signals of the VMEbus have to be used. This results in a maximum number of 7 boards to be synchronized (7 IRQ levels). The time required to interrupt all of them is enormous because each board has to request bus mastership and initiate an interrupt acknowledge cycle. This results in a big timing gap between the different CPU boards being interrupted.
The FMB allows each of the maximum 21 defined boards in the system to be addressed, and to interrupt one, some or all of them, sending the addressed boards an 8 bit message.
The FMB therefore allows any board(s) to be triggered at the same time by fetching the interrupt vector on the local bus leaving the VMEbus free for activities of other bus masters.
Each participant of the FMB stores the single byte message in its 8 byte deep FIFO (inside the Gate Array) and at the same time interrupts the local CPU on a software programmable level (1 to 7).
Each of the two, fully independent FIFOs is designed to allow as many as 8 messages to be sent to multiple participants within a short time frame. The messages can be read by the local CPU after the interrupt has been acknowledged.
The FMB byte is user defined to allow maximum flexibility and to adapt the various requirements to the user needs.
The most important feature of the FMB is that each 32 bit VMEbus based CPU available on the market can send this message byte to a FORCE board supporting the FMB function.
No special motherboard or extended address modifier capabilities are needed because only the defined signals, timings and data transfer types are used to perform the FMB.
Each master can define the board(s) which are to receive the FMB byte on an individual basis. The hardware inside the Gate Array decodes the information from the used address and performs the cycle.
The data transfer of the FMB is completed in less than 330 ns for all CPU boards which results in a maximum data bandwidth (theoretical) of 20 x 3 Mbyte/s = 60 Mbyte/s.
A patent on the FMB is pending.
The FORCE Message Broadcast is described in detail in the SYS68K/FMB Data Sheet while the general block diagram is shown below.

BLOCK DIAGRAM OF THE FORCE MESSAGE BROADCAST



7. The Interrupt Structure

The Gate Array installed on the SYS68K/CPU-30 handles all local and VMEbus interrupts. Each interrupt request from the local bus through the SCSI and floppy disk controller, the DUSCC, RTC and the two timers, as well as the Gate Array specific interrupt requests, are combined with the 7 VMEbus interrupt requests.
Each IRQ source including the VMEbus IRQs can be programmed to interrupt the CPU on an individual programmable level (1 to 7).

The Gate Array supports the vector, or initiates an interrupt vector fetch from the I/O device or from the VMEbus.
In addition to the local interrupts, the ACFAIL and SYSFAIL signals can be used to interrupt the CPU on a software programmable level.
This results in a total of 42 individual IRQs handled through the Gate Array on the SYS68K/CPU-30 board.
The Gate Array supplied interrupt vectors have a basic vector and fixed increments for each source. The basic vector is software programmable.

8. The Memory Map

The memory map of the SYS68K/CPU-30 is listed in the following table:

Start Address	End Address	Type
00000000	003FFFFF	Dual Ported Memory (4 Mbyte)
00400000	F9FFFFFF	VMEbus Addresses A32: D32, D24, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area (Slave and Master Mode)
FB000000	FBFEFFFF	VMEbus A24: D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus A16: D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus A24: D16, D8
FCFF0000	FCFFFFFF	VMEbus A16: D16, D8
FD000000	FDFFFFFF	Reserved
FE000000	FEFFFFFF	Reserved

Start Address	End Address	Capacity	Type
FF000000	FF7FFFFF	8 Mbyte	USER–EPROM
FF800000	FFBFFFFF	1 Mbyte	Local I/O
FFC00000	FFCFFFFF	1 Mbyte	LOCAL SRAM
FFD00000	FFDFFFFF	1 Mbyte	Registers of FGA-002
FFE00000	FFEFFFFF	1 Mbyte	SYSTEM EPROM
FFF00000	FFFFFFFF	1 Mbyte	Reserved

9. The VMEPROM

9.1. General Description

VMEPROM is an EPROM based real time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM. VMEPROM is composed of the powerful PDOS Real Time Kernel and the PDOS file manager. Thus the package provides support of a highly sophisticated Real Time Kernel and an interface to floppy and hard disk drives.

The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition, it includes a powerful line assembler and disassembler for the 68030 and the 68882.

VMEPROM features:

- Real Time Multitasking Kernel supporting up to 64 tasks.
- File management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Line assembler/disassembler with full support of all 68030/68882 instructions.
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify.
- S-record up/downloading from any port defined in the system.
- Disk support for RAM-disk, floppy and Winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. The local SCSI and floppy disk controller are also supported. VMEPROM also allows disk formatting and initialization.
- Serial I/O support for up to two SIO or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full screen editor.
- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.

9.2. Description of the User Interface of VMEPROM

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple command lines may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

9.3. Description of the Kernel Functions

The kernel of VMEPROM is written in 68030 assembly language for fast and efficient execution. It provides multitasking, system clock,event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously.
Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

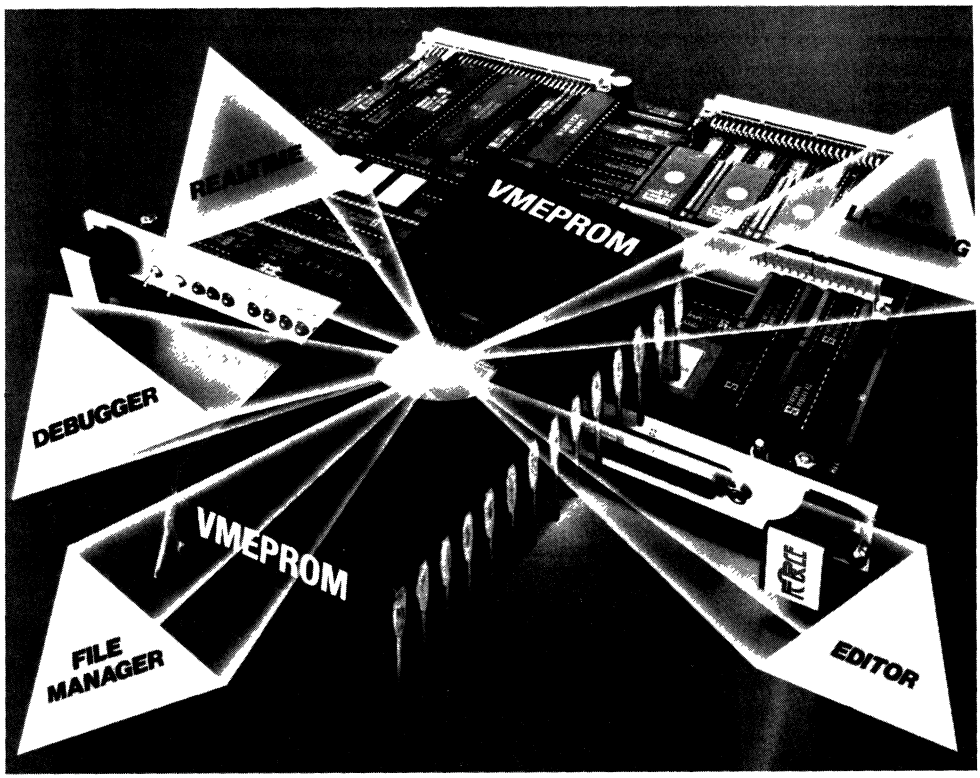
9.4. Description of the File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

9.5. Supported VMEbus Hardware

Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards, and one disk controller.
In addition, EPROM programming is supported by VMEPROM utilizing the SYS68K/RR-2/3 board family.

VMEPROM



9.6. Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 40 Kbyte. Small romable applications can be put in EPROMS easily without the overhead of the user interface.

9.7. Development Systems

Currently either one of the FORCE PDOS* or UNIX* System V development stations may be used for software development for VMEPROM.
Compilers, assemblers, and libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.
The support of VMEPROM through other development systems like the IBM-AT or the VAX is under development. These crosssoftware development packages will include C-compiler, assemblers for the 68030 and libraries to generate code to run under control of VMEPROM.

9.8. Licensing

No license is required for VMEPROM. VMEPROM is delivered free of charge with every CPU-30 board. For more detailed information please refer to the SYS68K/VMEPROM Data Sheet.

10. Specification

Function	
68030 CPU Frequency on: CPU-30X CPU-30XA/-30ZA	 16.7 MHz 20.0 MHz
68882 FPCP Frequency on: CPU-30X CPU-30XA/-30ZA	 16.7 MHZ 20.0 MHz
DMA Controller: CPU-30X CPU-30XA/-30ZA Internal FIFO Max. Data Transfer Throughput	16.7 MHz 20.0 MHz 32 byte 30 Mbyte/s
Dual Ported RAM Type Byte Parity DPR Capacity: CPU-30X/-30XA CPU-30ZA No. of Wait States for all CPU and DMA Cycles	DRAM yes 1 Mbyte 4 Mbyte 1
SRAM Capacity On-Board Battery Backup	32 Kbyte yes
No. of EPROM Sockets Data Paths Max. Capacity No. of Wait States (min/max)	4 32 bit 4 Mbyte 1/6
Serial I/O Interfaces (total) Used Controller RS232 compatible RS232/RS422 compatible	4 2 x 68562 1 3
Real Time Clock (Typ) On-Board Battery Backup	62421 yes
SCSI Controller Chip SCSI Interface Data Transfer Rate asynchronous synchronous Connection to DMA Controller I/O Signals routed to	87030 Single ended 2 Mbyte/s 4 Mbyte/s yes P2
Floppy Disk Controller Chip Interface Connection to DMA Controller I/O Signals routed to	1772 SA 460 yes P2

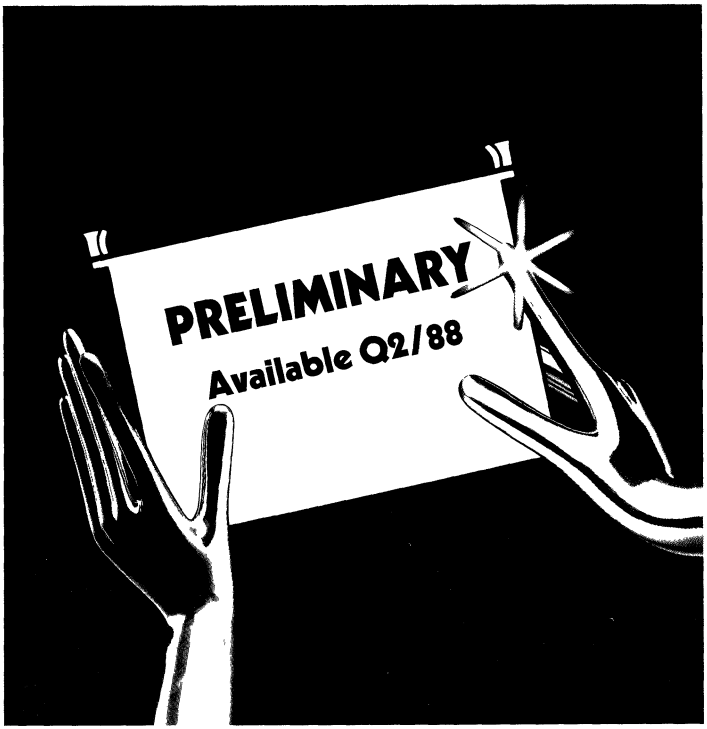
10. Specification (cont'd)

Function		
VMEbus Interface		
Master: A32, A24, A16:D8, D16, D32, D(0), UAT		yes
Slave: A32, A24, A16:D8, D16, D32, D(0), UAT		yes
Software Programmable Access Address and Address Modifier Code		yes
No. of different Areas for Dual Ported RAM		3
DPR Read Access Time (Typ)		340 ns
Write Access Time (Typ)		330 ns
Single Level Bus Arbiter		yes
SYSCLK Driver		yes
16 Location Monitors		yes
FORCE Message Broadcast		
FMB-FIFO 1		8 byte
FMB-FIFO 2		8 byte
Timers		
24 bit with 5 bit Prescaler		2
8 bit with 8 bit Prescaler		3
8 bit with 8 bit Prescaler (Watchdog Timer for SYSFAIL)		1
VMEbus Interrupt Handler		1 to 7
Local Bus Interrupt Handler		1 to 7
All Sources can be routed to a Software programmable IRQ Level		yes
Total Number of IRQ Sources		42
RESET, TEST, RUN and CACHE Switch		yes
VMEPROM Firmware installed on all Board Versions		128 Kbyte
Power Requirements		
+ 5V min/max		4.2/5.9A
+12V min/max		0.1/0.3A
−12V min/max		0.1/0.3A
Operating Temperature	(Degrees C)	0 to 50
Storage Temperature	(Degrees C)	−40 to 85
Relative Humidity	(non-condensing in %)	0 to 95
Board Dimensions	(mm)	234 x 160
	(in)	9.2 x 6.3
No. of Slots used		1

Ordering Information

SYS68K/CPU-30X Part No. 101300	16.7 MHz 68030 based CPU board with 68882 FPCP, DMAC, 1 Mbyte Dual Ported RAM capacity and VMEPROM. Documentation included.
SYS68K/CPU-30XA Part No. 101301	20.0 MHz 68030 based CPU board with 68882 FPCP, DMAC, 1 Mbyte Dual Ported RAM capacity and VMEPROM. Documentation included.
SYS68K/CPU-30ZA Part No. 101302	20.0 MHz 68030 based CPU board with 68882 FPCP, DMAC, 4 Mbyte Dual Ported RAM capacity and VMEPROM. Documentation included.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM User's Manual
SYS68K/CPU-30/UM Part No. 800146	User's Manual for the SYS68K/CPU-30 products, including VMEPROM User's Manual.

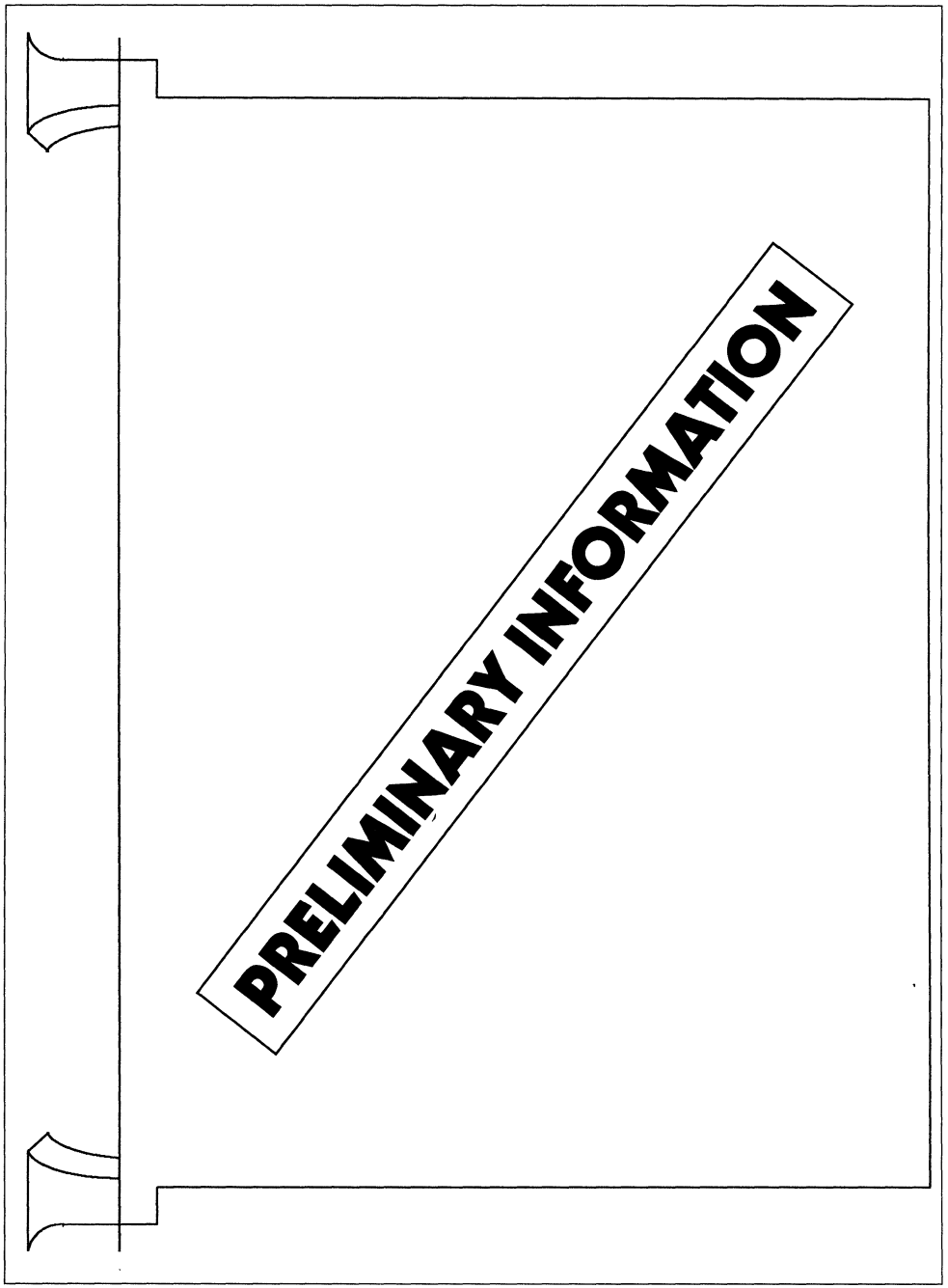
Note: SYS68K/CPU-30 board versions without the 68882 FPCP are available upon special request.



System 68000 VME
SYS68K/CPU-31

Multiprocessor
68030 based CPU board

- 16.67 or 20.0 MHz 68030 CPU
- On board Memory Management Unit
- DMA, Message Passing, Location Monitors
- 256 Kbyte/1 Mbyte Dual Ported RAM
- VSB Interface


PRELIMINARY INFORMATION

1. General Description

The SYS68K/CPU-31 is a 68030 based CPU-board especially designed for multiprocessor applications. The Supreme Dual Ported RAM supports constant zero wait state access of the 68030 CPU to the S-DPR while the RAM is also accessed from the VMEbus side. The high speed fully dual ported and dual buffered static RAM with a capacity of 256 Kbyte or 1 Mbyte also supports read and write protection for three individual memory areas from the VMEbus side.

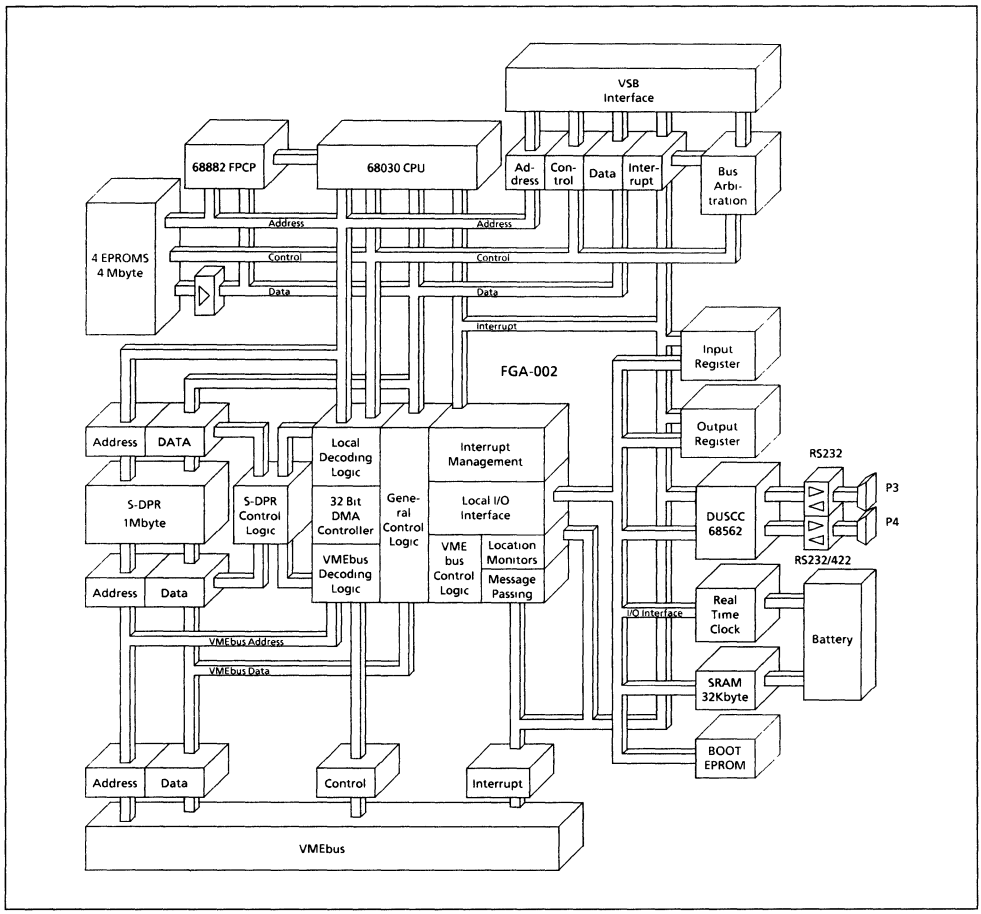
The SYS68K/CPU-31 also includes the 68882 enhanced Floating Point Coprocessor and a full 32 bit DMA Controller which is built inside the 280 pin FORCE specific Gate Array. The DMA Controller can transfer data fully independant from the operation of the local CPU.

Special multiprocessor functions are the 2 independent 8 bit wide Message Broadcast FIFOs, and the 16 location monitors. Each supports the interruption of the local CPU on a software programmable level.

Additional features include the up to 4 Mbyte EPROM capacity (32 bit wide), the 2 multi-protocol serial I/O links, the 32 Kbyte battery backed up SRAM and the Real Time Clock/Calender.

The 32 bit VSB interface with its 4 Gbyte address range completes the board.

BLOCK DIAGRAM OF THE SYS68K/CPU-31



2. Features of the SYS68K/CPU-31 boards:

- 68030 CPU with 16.7 or 20.0 MHz clock frequency.
- 68882 Floating Point Coprocessor with 16.7 or 20.0 MHz clock frequency.
- 32 bit DMA Controller supporting data transfer speeds of up to 30 Mbyte/s (memory to memory). 32 byte internal FIFO for burst DMA.
- 256 Kbyte or 1 Mbyte constant zero wait state static RAM dual ported to the VMEbus with three fully independent software programmable access address ranges and Write/Read protection.
- Four user EPROM sockets for up to 4 Mbyte EPROM capacity supporting the 28 and 32 pin JEDEC standard-one wait state operation from EPROMs by using 100 ns devices.
- One system EPROM socket for local booting and initialization of the I/O and the Gate Array.
- 32 Kbyte of static RAM with on-board battery backup and power fail detection logic.
- Real Time Clock/Calender with battery backup.
- Two multi-protocol serial I/O channels with SDLC, HDLC and asynchronous protocols – RS232 compatible (one RS422 configurable).
- Two 24 bit timers with 5 bit prescaler – each timer may interrupt the 68030 CPU on a software programmable level (1 to 7).
- Three 8 bit timers with an 8 bit prescaler also supporting interrupts to the 68030 CPU on a software programmable level (1 to 7).
- One 8 bit timer with an 8 bit prescaler used as a watchdog timer to force a SYSFAIL to the VMEbus (software selectable).
- BERR handling fully under software control via different counters for local, VMEbus and secondary bus accesses.
- Full 32 bit VMEbus master interface supporting the following data transfer types:
  A32, A24, A16 : D8, D16, D32
  UAT, RMW and address only cycles.
- Full 32 bit VMEbus slave interface to the Dual Ported RAM supporting the following data transfer types:
  A32, A24 : D8, D16, D32
  UAT, and address only cycles
- Single level bus arbiter
- SYSCLK driver
- VMEbus Interrupt Handler (IH 1 to 7 dynamic)
- Two independent Message Broadcast FIFOs for simultaneous access of up to 20 CPU boards installed in one RACK.
- 16 software programmable location monitors supporting 16 different interrupt vectors on individual software programmable levels (1 to 7).
- Support for ACFAIL and SYSFAIL via software programmable IRQ-levels.
- Timeout counter (3 seconds), if the board does not receive VMEbus mastership. Software selectable in parallel to the standard bus error counters.
- VSB interface supporting 8, 16 and 32 bit data transfers is installed on the board.
- VMEPROM the real time monitor with file manager and Real Time Kernel (PDOS compatible) is installed on each board version.

3. HARDWARE DESCRIPTION

3.1 The 68030 CPU

The 68030 with its 32 bit address and data paths is installed on the SYS68K/CPU-31 board.
The CPU includes a 256 byte instruction- and a 256 byte datacache which significantly reduces the number of bus cycles needed for program fetches. A CACHE switch on the front panel allows the user to enable or disable the on-chip cache for software debugging purposes.
To achieve maximum performance, the 68030 CPU accesses the Dual Ported Memory constantly without the insertion of wait states, through the on chip MMU.
Communication with the local I/O interfaces, local SRAM, and the VMEbus interface is provided through the specially designed 280 pin Gate Array.
The EPROM area, the Floating Point Coprocessor, the Dual Ported RAM and the VSBbus interface are directly connected to the CPU data and address bus interface (as shown in the block diagram of the SYS68K/CPU-31).
The clock frequency of the CPU is 16.7 or 20.0 MHz. This offers, in combination with the Dual Ported RAM, a real computing rate of 3-8 MIPs.

3.2 The Floating Point Coprocessor

The SYS68K/CPU-31 is fitted with the enhanced 68882 Floating Point Coprocessor (FPCP). The clock frequency of the CPU and the FPCP is identical. The FPCP conforms to the IEEE Floating Point standard 754 (draft 10.0).
Easy floating point operation control to the coprocessor is provided because the intercommunication between the CPU and the FPCP is built in silicon.
An internal register set inside the FPCP of 8 general purpose registers (80 bit wide) yields fast execution times.

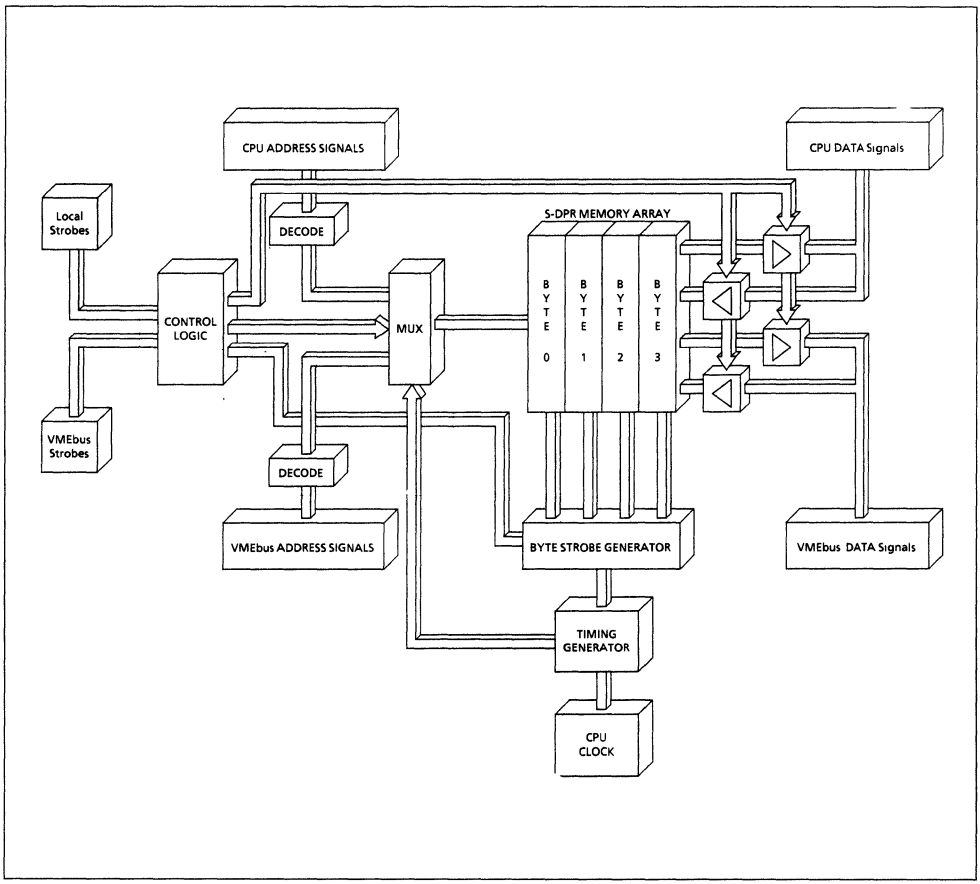
Features of the FPCP

- 8 general purpose registers (80 bit, 64 bit Mantissa, 15 bit exponent and one sign bit)
- 67 bit on-chip ALU
- 67 bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 standard (draft 10.0)
- Full support of trigonometrical and logarithmic functions such as:
  - SINE and COSINE
  - TANGENT and COTANGENT
  - Hyperbolic functions (TANGENT, ARC TANGENT, SINE and COSINE)
  - Logarithmic functions (4)
  - Square root and exponential functions (4)
- The 68882 is fully software compatible to the 68881 FPCP

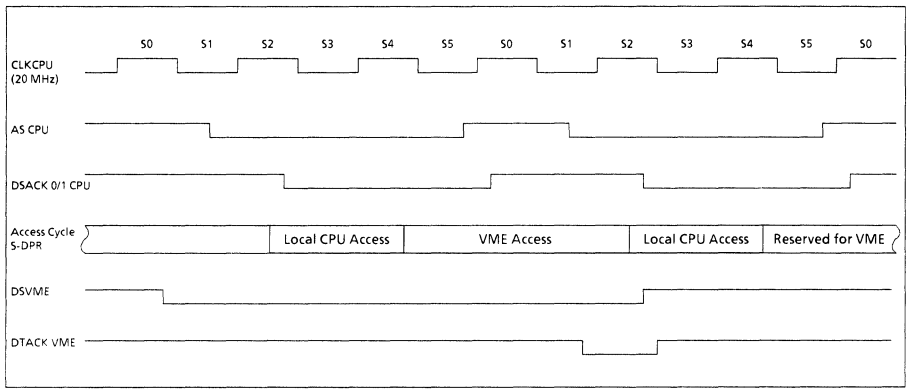
3.3 The Dual Ported RAM

The SYS68K/CPU-31 contains a Supreme Dual Ported static RAM design called S-DPR, which constantly supports zero wait state accesses of the local CPU. All accesses of the 68030 CPU to the S-DPR are immediately serviced while the VMEbus accesses are forced to the S-DPR between the 68030 access cycles.
This technique allows the SYS68K/CPU-31 to guarantee a constant run time of all programs regardless of whether an access to the S-DPR from another VMEbus board is forced or not.
The bandwidth of the S-DPR for the local CPU is 25 Mbyte/sec plus 15 Mbyte/sec for the VMEbus. This results in a total S-DPR bandwidth of 40 Mbyte/sec.
A detailed block diagram of the S-DPR control mechanism and a global timing diagram are outlined below.

BLOCK DIAGRAM OF THE S-DPR



Timing Diagram of the S-DPR



A key advantage of the S-DPR technology is that the SYS68K/CPU31 can be used in critical real-time applications without loosing the real-time capabilities through external accesses to the S-DPR. Alternative technologies such as the dual gated mechanism (the CPU is halted during the VMEbus accesses) or the dual buffered function (alternative access to the DPR while one requester is waiting until the RAM is unused) cannot guarantee constant zero wait state operation. In non – S-DPR configurations the CPU normally waits or is halted during a VMEbus access cycle which results in a decreased CPU throughput.
The SYS68K/CPU-31 indeed combines the highest possible throughput (zero wait state accesses) with the Dual Ported RAM structure without decreasing performance at a CPU clock frequency of 16.7 or 20.0 MHz.
The memory capacity is 256 Kbyte, or 1 Mbyte depending on the board version.

Increasing the memory capacity from 256K to 1 Mbyte is possible by exchanging the SYS68K/SMDP-05 memory module with a SYS68K/SMDP-06 module. The SYS68K/SMDP-06 board holds 1 Mbyte RAM. The SMDP-06 board has the same dimensions as the SMDP-05 and can easily be installed.
Underneath the SYS68K/SMDP-05/06 boards only passive components such as resistors and capacitors are installed to guarantee correct operation for an ambient temperature range of 0 to +50 degrees C.
The access address of the S-DPR is fully software programmable through the installed Gate Array within the 4 Gbyte address range.
Address and address modifier decoding for the VMEbus accesses is software programmable through the Gate Array. Three independent areas, in 4 Kbyte increments, can be defined by the onboard CPU.

Each of the three independent memory areas forces a data transfer cycle to the S-DPR under the software programmed address range where the S-DPR resides. In addition, each of the three S-DPR address ranges can be read and write protected under software control during run time.

3.4 The Local SRAM

A 32 Kbyte static RAM is installed on all SYS68K/CPU-31 board versions and supports data storage during power down phases for up to 1 year. The SRAM is directly connected to the FORCE Gate Array I/O interface. Long, word and byte transfers are automatically controlled via the Gate Array.
Normal read and write operations to the single 32Kx8 SRAM are allowed if the power is within the specification detected by a separate power sensor. Higher organized devices compatible to the JEDEC standard (i.e. 128Kx8 devices) can be installed in the 32 pin socket.

3.5 The EPROM Areas

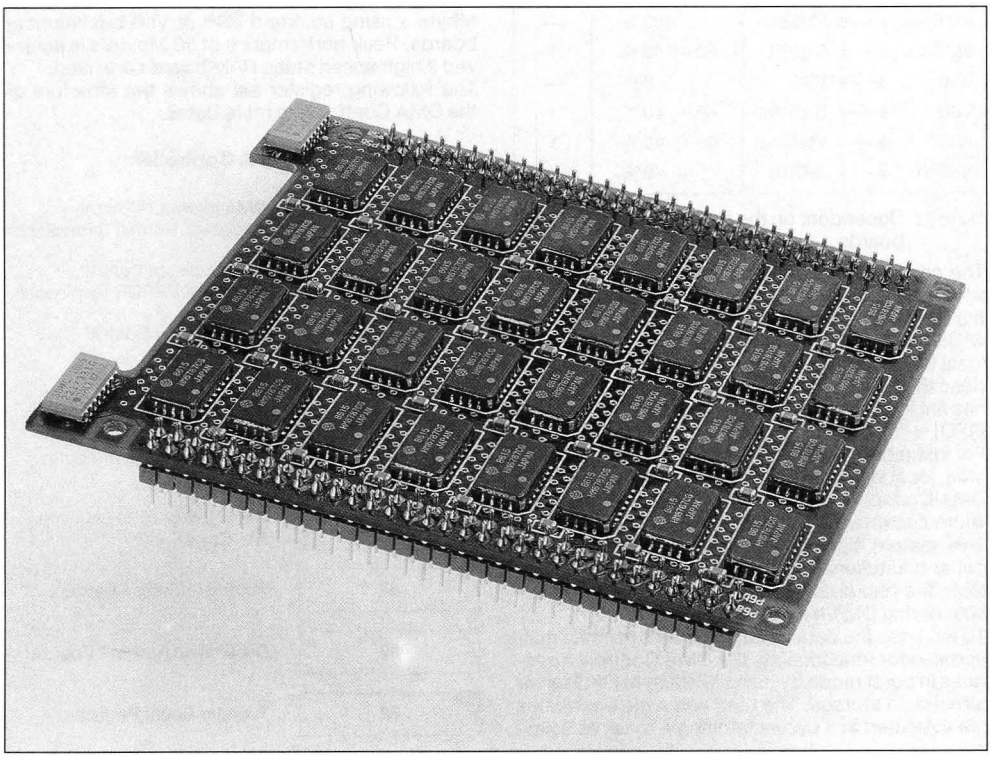
3.5.1 The USER EPROMs

The SYS68K/CPU-31 contains four user EPROM sockets supporting four 28 or 32 pin EPROM devices. Maximum data throughput to the 68030 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation if 100 ns devices are installed. The following table lists the supported device types and the memory capacity.

Supported Device Types in the User EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
2764	28	8K x 8	32 Kbyte
27128	28	16K x 8	64 Kbyte
27256	28	32K x 8	128 Kbyte
27512	28	64K x 8	256 Kbyte
271024	32	128K x 8	512 Kbyte
TBD	32	256K x 8	1 Mbyte
TBD	32	512K x 8	2 Mbyte
TBD	32	1M x 8	4 Mbyte

PHOTO OF THE SMDP-05 BOARD



3.5.2 The SYSTEM EPROM

The SYS68K/CPU-31 board contains in addition to the four user EPROMs a single system EPROM to boot the local CPU, initialize all I/O devices and program the board dependent functions of the Gate Array FGA-002. All the presetting and initialization of the I/O devices are made through the system EPROM to ease the adaptation of the complex board functions to the application needs.

3.6 The DMA Controller

A high speed DMA Controller is installed on the SYS68K/CPU-31 and features a data transfer speed of up to 30 Mbyte/s.
This throughput is the effective transfer speed which assumes zero wait state accesses by transferring 32 bit of data.
The SYS68K/CPU-31 allows the transfer of data between memory (2 different memory areas) and between VSB/VMEbus memory and the S-DPR, as listed below.

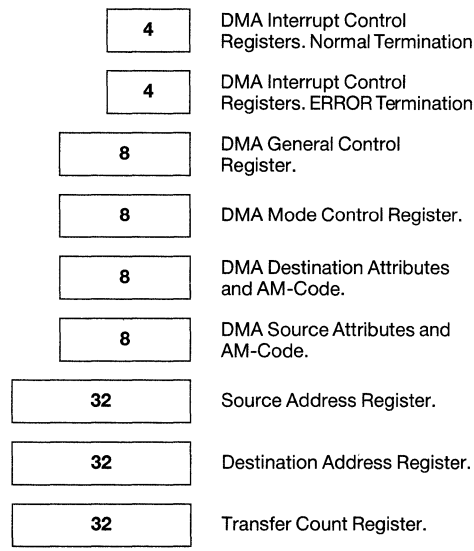
Possible Data Transfers for the DMA Controller.

Area 1		Area 2	CPU Operation	Note
VMEbus	⟷	VMEbus	100%	—
VMEbus	⟷	S-DPR	60 – 40%	1
VSB	⟷	VSB	0%	—
VSB	⟷	S-DPR	60 – 40%	1
VSB	⟷	VMEbus	60 – 40%	1
S-DPR	⟷	S-DPR	0%	—

Note 1: Dependent on the speed of the addressed boards

The center row lists the time (percentage wise) in which the local CPU is operable and able to access the local I/O devices, EPROM areas and the S-DPR, while the DMA Controller transfers data. Only if the local CPU wants to access the VSB or the VMEbus does the CPU have to wait until the DMA Controller has finished the maximum 8 data transfers from it's FIFO.
For instance, the local CPU can access the EPROM area, local system RAM and all I/O devices while the DMA Controller is transferring data on the VMEbus without interfering with the activities of the CPU.
This feature significantly increases data throughput and functionality because the local CPU maintains the real-time capabilities by being interruptable during DMA transfers.
To increase the data throughput and maintain multiprocessor functionality, the DMA Controller operates in burst mode by using its 32 byte FIFO for internal data storage. The read and write operations are executed in 8 cycles fetching 4 bytes at a time which result into 8 read cycles followed by 8 write cycles. The DMA Controller supports the transfer of data on unaligned addresses, as an internal control mechanism is installed to align the data transfers to 32 bit accesses if possible.
This technology allows to transfer data between the S-DPR and the VSB or VMEbus by first collecting the data from the VSB or VMEbus, giving up bus mastership and then transferring the data to the S-DPR. A second VSB or VMEbus board is allowed to transfer data on the VSB or VMEbus while the DMA Controller transfers the stored data to the S-DPR.
The bus release functions of the VMEbus mastership of the DMA Controller is software programmable.
The DMA Controller is installed inside the 280 pin Gate Array supporting 32 data and address signals. All addressing modes of the VMEbus are fully software programmable (AM-Codes) for the source and destination address.
The data transfer speed between the S-DPR and the VSB/VMEbus depends on the access time of the addressed VSB/VMEbus module.
The effective transfer speed reaches 15 to 20 Mbyte/s using standard VSB or VMEbus memory boards. Peak performance of 30 Mbyte/s is achieved if high speed static RAM boards are used.
The following register set shows the structure of the DMA Controller in more detail.

Register Set of the DMA Controller



3.7 The Local I/O Devices

The Gate Array installed on the SYS68K/CPU-31 includes an 8 bit local I/O bus interface.
The Real Time Clock, the serial I/O controller and the port read/write functions are directly connected to this I/O interface.

3.7.1 The Serial I/O Interfaces

A Dual Universal Serial Communication Controller (DUSCC 68562) is installed on the SYS68K/CPU-31 to communicate via two serial interfaces to terminals, printers, computers or other equipment.

Features of the DUSCC

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multi-protocol operation consisting of:
  BOP: HDLC/ADCCP, SDLC, SDLC Loop, X.25 or X.75 link level
  COP: BISYNC, DDCMP, X.21
  ASYNC: 5–8 bit plus optional parity
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1, Manchester
- 4 character receiver and transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter
- Digital phase locked loop
- User programmable counter/timer
- Programmable channel modes full/half duplex, auto echo, local loopback
- Modem control signals for each channel: RTS, CTS, DCD
- CTS and DCD programmable auto enables for Receiver (RX) and Transmitter (TX)
- Programmable interrupt on change of CTS or DCD

The I/O signal assignment of each of the two channels is listed in the following table:

Signal	Input	Output	9 Pin DSUB Connector	Description
DCD	x		1	Data Carrier Detect
RXD	x		2	Receive Data
TXD		x	3	Transmit Data
DTR		x	4	Data Terminal Ready
GND			5	Signal GND
DSR	x	x	6	Data Set Ready
RTS		x	7	Request to Send
CTS	x		8	Clear to Send
–	–	–	9	Not Connected

The first channel is assigned to connect a terminal via the RS232 compatible interface.
The second channel can be configured to work as a RS232 or as a RS422 compatible interface. R/C components can be installed to adapt to various cable lengths and reduce reflections if the RS422 compatible interface is selected.

The DUSCC is able to interrupt the local CPU on a software programmable IRQ-level (1-7) by supplying its own software programmable IRQ vectors (6 in total) to the local CPU.

3.7.2 The Real Time Clock

A software programmable Real Time Clock (RTC-62421) with onboard battery backup is installed on the SYS68K/CPU-31 boards. The features of the Real Time Clock are listed below.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12hr/24hr clock switchover
- Automatic leap year setting
- Interrupt masking
- C-MOS design provides low power consumption during power down mode.

The Real Time Clock is able to interrupt the local CPU on a software programmable level (1 to 7).

3.7.3 The Input/Output Register

A total of three input and one 8 bit output port is available on the SYS68K/CPU-31.
The first 8 bit input port is connected to the two 4 bit HEX rotary switches available on the front panel for configuration purposes.
The second 8 bit input port allows the jumper settings to be read (1 or 0) on a jumperfield installed on the PCB. This jumperfield can be used to define the slot number or to define application dependent pre-settings.
The third 8 bit input port allows the memory capacity of the S-DPR to be read. Each SYS68K/SMDP board has three readable status bits describing the memory capacity. In addition, the CPU board type can be read via the remaining 5 bits.
Four LEDs are controlled via the 8 bit output port. The remaining 4 bits are used for board specific control functions.

3.7.4 The Timers

A total of 6 independent timers are available for the user. These timers offer maximum flexibility because each timer can be used to force an interrupt to the CPU on a software programmable IRQ-level.
The first two timers each provide a 24 bit timer with an individual 5 bit prescaler.The next three timers are 8 bit wide and include an 8 bit prescaler.
The sixth timer is used to generate the SYSFAIL signal to the VMEbus. SYSFAIL can be used in multiprocessor systems to signal that one board has detected a failure. This 6th timer is used as a watchdog timer which needs to be triggered after a software programmed time before signalling SYSFAIL.
All installed timers can be used as a watchdog timer or can generate interrupts on a periodical basis.

4. The VMEbus Interface

The SYS68K/CPU-31 includes a full 32 bit VMEbus interface, thereby taking full advantage of the VMEbus specification.
The address modifier codes for A16, A24 and A32 addressing are fully supported in master and slave mode. In slave mode the Gate Array decodes the AM-codes and the address signals of the VMEbus and signals the on-board control logic if one of the three independent decoding ranges are addressed correctly and if the access cycle has to be executed (read/write protection).
The Gate Array forces the access cycle to the S-DPR and controls/adapts the data flow (8, 16, 24 or 32 bit of data) automatically.
The following data transfer types are supported in master and slave mode:

Transfer Type	D31-D24	D23-D16	D15-D8	D7-D0
Byte			x	x
Word			x	x
Long Word	x	x	x	x
Unaligned	x	x	x	
Transfers		x	x	
		x	x	x
Read Modify				x
Write*			x	x
	x	x	x	x

*Read modify write cycles are split into separate read and write cycles only in the slave mode while multiprocessor synchronization is provided via the Gate Array.

The access time to access the S-DPR from the VMEbus are listed in the following table:

Access Times	Min	Type	Max
Read	120ns	215ns	330ns
Write	110ns	195ns	310ns

The SYS68K/CPU-31 includes a DMA Controller supporting high speed data transfer through the on-board Gate Array. DMA transfers can be performed between the S-DPR and VMEbus memory while the 68030 CPU is operating.
The SYS68K/CPU-31 includes the following bus arbitration modes:

RWD	Release when done
ROR	Release on request
ROBCLR	Release on Bus Clear
RAT	Release after Timeout

In addition, the board is able to request bus mastership if no other board requests bus mastership (Request on No Request RNR).

Each of the listed modes is software programmable inside the Gate Array. The bus request level of the SYS68K/CPU-31 is jumper selectable (BR0-3). A single level arbiter, a power monitor, a SYSRESET generator and support for ACFAIL and SYSFAIL complete the VMEbus interface.
The installed location monitor and the Message Broadcast on VME are briefly described in the next two sections.

5. The Location Monitors

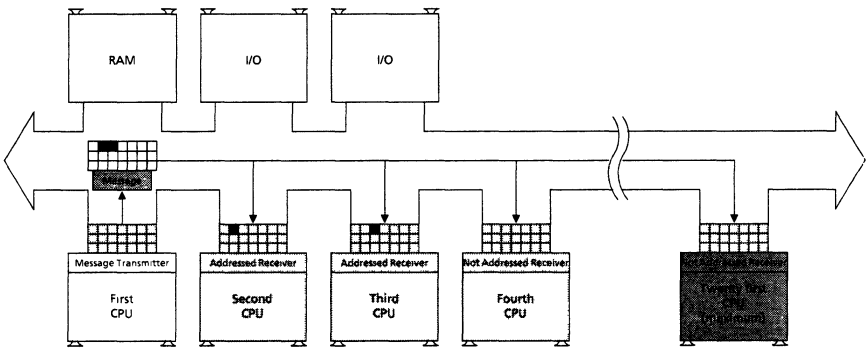
The SYS68K/CPU-31 includes 16 location monitors. Each of these location monitors allows an interrupt to be forced to the local 68030 CPU. The interrupt level of each location monitor is software programmable and an individual interrupt vector for each location monitor is forced to the CPU.
This function allows the triggering of multiple CPU boards via one master by only fetching an interrupt vector on the local bus and leaving the VMEbus free for data transfers.
In addition, the location monitor bits can be used to synchronize multiple CPUs via standard read cycles by internally forcing a read modify write cycle. This allows various CPUs on the VMEbus to be synchronized (for example a 68030 and a 80386 CPU-board).

6. The Message Broadcast

The SYS68K/CPU-31 board provides two fully independent unique Message Broadcast functions which are implemented within the Gate Array.
The FORCE Message Broadcast (FMB) allows the simultaneous addressing and interrupting of all CPU boards installed in a VMEbus environment. It stores an 8 bit message in an 8 stage deep FIFO.
The Message Broadcast complies fully to the VMEbus specification and minimizes the time overhead required to interrupt all installed CPU boards in a system.
Without FMB, the following problems occur when synchronousing multiple CPUs in a VMEbus environment.
If, for example, 16 boards are installed in a system, without FMB, the minimum time required to interrupt all of them is 16 times an access cycle to each of their location monitors. If no location monitors are available then the IRQ signals of the VMEbus have to be used. This results in a maximum number of 7 boards to be synchronized (7 VMEbus IRQ levels). The time required to interrupt all of them is enormous because each board has to request bus mastership and initiate an interrupt acknowledge cycle. This results in a big timing gap between the different CPU boards being interrupted.
The FMB allows each of the maximum 21 defined boards in the system to be addressed and to interrupt one, some or all of them, sending the addressed boards an 8 bit message.

The FMB therefore allows any board(s) to be triggered at the same time by fetching the interrupt vector on the local bus leaving the VMEbus free for activities of other bus masters.
Each participant of the FMB stores the single byte message in its 8 byte deep FIFO (inside the Gate Array) and at the same time interrupts their local CPU on a software programmable level (1 to 7).
Each of the two, fully independent FIFOs is designed to allow as many as 8 messages to be sent to multiple participants within a short time frame. The messages can be read from the local CPU after the interrupt has been acknowledged.
The FMB byte is user defined to allow maximum flexibility and to adapt the various requirements to the user needs.
The most important feature of the FMB is that any 32 bit VMEbus based CPU available on the market can send this message byte to a FORCE board supporting the FMB function.
No special motherboard or extended address modifier capabilities are needed because only the defined signals, timings and data transfer types are used to perform the FMB.
Each master can define the board(s) which have to receive the FMB byte on an individual basis. The hardware inside the Gate Array decodes the information from the used address and performs the cycle.
The data transfer of the FMB is completed in less than 330 ns for all CPU boards which results in a maximum data bandwidth (theoretical) of 20x3 Mbyte/s = 60 Mbyte/s.
A patent on the FMB is pending.
The FORCE Message Broadcast is described in detail in the SYS68K/FMP Data Sheet while the general block diagram is shown below.

BLOCK DIAGRAM OF THE FORCE MESSAGE BROADCAST



7. The Interrupt Structure

The Gate Array installed on the SYS68K/CPU-31 handles all the local, VMEbus and secondary bus interrupts. Each interrupt request from the local bus through the DUSCC, RTC and the two timers, as well as the Gate Array specific interrupt requests, are combined with the 7 VMEbus interrupt requests.
Each IRQ source including the 7 VMEbus IRQs can be programmed to interrupt the CPU on an individual programmable level (1 to 7).
The Gate Array supports the vector or initiates an interrupt vector fetch from the local I/O devices or from the VMEbus.
In addition to the local interrupts, the ACFAIL and SYSFAIL signals can be used to interrupt the CPU on a software programmable level.
This results in a total of 40 individual IRQs handled through the Gate Array on the SYS68K/CPU-31 board.
The Gate Array supplied interrupt vectors have a basic vector and fixed increments for each source. The basic vector is software programmable.

8. The VSB Interface

The SYS68K/CPU-31 board is delivered with a full 32 bit VSB master interface.
Maximum data throughput is provided on the VSB interface by supporting 8, 16, 24 and 32 bit data transfers in the 4 Gbyte address range. The VSB address range is decoded out of the 4 Gbyte address space of the 68030.

The following data transfer types are supported:

- A32 : D8, D16, D32
- Unaligned Transfers
- Address Only Cycles
- Read Modify Write Transfers

The VSB interface allows to build contiguous memory together with the S-DPR. The local control logic provides an access cycle to the VSB before accessing the VMEbus. This technique allows to deload the VMEbus interface by using dual ported memories between the VMEbus and the VSB by accessing the memory through the VSB interface. A jumper setting allows to deselect the VSB interface if no VSB board is connected. The VSB interface also includes a serial arbiter as well as an IHP Interrupt Handler.

9. The Memory Map

The memory map of the SYS68K/CPU-31 is listed in the following table:

Start Address	End Address	Type
00000000	000FFFFF	Dual Ported Memory (1 Mbyte)
00100000	F9FFFFFF	VMEbus Addresses or VSB Addresses A32: D32, D24, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area (Slave and Master Mode)
FB000000	FBFEFFFF	VMEbus A24: D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus A16: D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus A24: D16, D8
FCFF0000	FCFFFFFF	VMEbus A16: D16, D8
FD000000	FDFFFFFF	Reserved
FE000000	FEFFFFFF	Reserved

Start Address	End Address	Capacity	Type
FF000000	FF7FFFFF	8 Mbyte	USER–EPROM
FF800000	FFBFFFFF	1 Mbyte	Local I/O
FFC00000	FFCFFFFF	1 Mbyte	LOCAL SRAM
FFD00000	FFDFFFFF	1 Mbyte	Registers of FGA-002
FFE00000	FFEFFFFF	1 Mbyte	SYSTEM EPROM
FFF00000	FFFFFFFF	1 Mbyte	Reserved

10.0 The VMEPROM

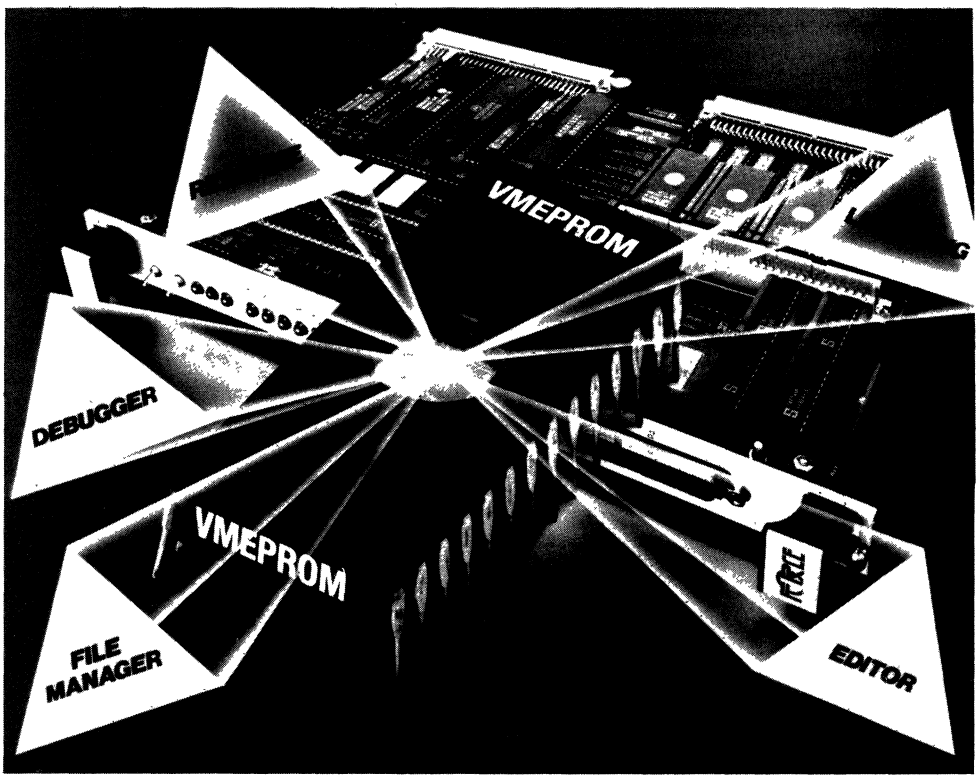
10.1 General Description

VMEPROM is an EPROM based real time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM. VMEPROM is composed of the powerful PDOS Real Time Kernel and the PDOS file manager. Thus the package provides support of a highly sophisticated Real Time Kernel and an interface to floppy and hard disk drives.
The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition, it includes a powerful line assembler and disassembler for the 68030 and the 68882.

VMEPROM features:

- Real Time Multitasking Kernel supporting up to 64 tasks.
- File management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Line assembler/disassembler with full support of all 68030/68882 instructions.
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify.
- S-record up/downloading from any port defined in the system.
- Disk support for RAM-disk, floppy and Winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. VMEPROM also allows disk formatting and initialization.
- Serial I/O support for up to two SIO-2 or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full screen editor.
- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.

VMEPROM



10.2. Description of the User Interface of VMEPROM

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple command lines may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

10.3 Description of the Kernel Functions

The kernel of VMEPROM is written in 68030 assembly language for fast and efficient execution. It provides multitasking, system clock,event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously. Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

10.4 Description of the File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

10.5 Supported VMEbus Hardware

Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards, and one disk controller.
In addition, EPROM programming is supported by VMEPROM utilizing the SYS68K/RR-2/3 board family.

10.6. Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 40 Kbyte. Small romable applications can be put in EPROMs easily without the overhead of the user interface.

10.7. Development Systems

Currently either one of the FORCE PDOS* or UNIX* System V development stations may be used for software development for VMEPROM.
Compilers, assemblers, and libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.
The support of VMEPROM through other development systems like the IBM-AT or the VAX is under development. These crosssoftware development packages will include C-compiler, assemblers for the 68030 and libraries to generate codes to run under control of VMEPROM.

10.8. Licensing

No license is required for VMEPROM. VMEPROM is delivered free of charge with every CPU-31 board.
For more detailed information please refer to the SYS68K/VMEPROM Data Sheet.

Specification

Function	
68030 CPU Clock Frequency on: CPU-31 CPU-31A/-31XA	 16.7 MHz 20.0 MHz
68882 FPCP Clock Frequency on: CPU-31 CPU-31A/-31XA	 16.7 MHZ 20.0 MHz
DMA Controller: CPU-31 CPU-31A/-31XA Internal FIFO Max. Data Transfer Throughput	16.7 MHz 20.0 MHz 32 byte 30 Mbyte/s
S-DPR Type S-DPR Capacity: CPU-31/-31A CPU-31XA No. of Wait States for all CPU and DMA Cycles	SRAM 256 Kbyte 1 Mbyte 0
SRAM Capacity On-Board Battery Backup	32 Kbyte yes
No. of EPROM Sockets Data Paths Max Capacity No. of Wait States (min/max)	4 32 bit 4 Mbyte 1/6
Serial I/O Interfaces (total) Used Controller RS232 compatible RS232/RS422 compatible	2 68562 1 1
Real Time Clock (Type) On-Board Battery Backup	62421 yes
VMEbus Interface Master: A32, A24, A16:D8, D16, D32, D(0), UAT Slave: A32, A24, A16:D8, D16, D32, D(0), UAT Software Programmable Access Address and Address Modifier Code No. of different Areas for S-DPR Accesses S-DPR Read Access Time (Typ) Write Access Time (Typ) Single Level Bus Arbiter SYSCLK Driver 16 Location Monitors	 yes yes yes 3 215ns 195ns yes yes yes

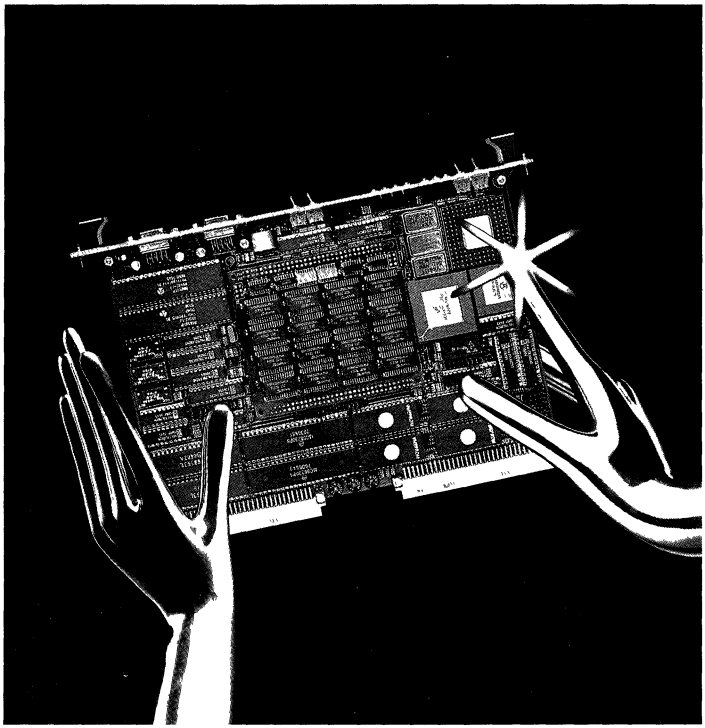
Specification

Function	
FORCE Message Broadcast FMB-FIFO 1 FMB-FIFO 2	 8 byte 8 byte
VMEbus Interrupt Handler Local Bus Interrupt Handler All Sources can be routed to a Software programmable IRQ Level Total Number of IRQ Sources	1 to 7 1 to 7 yes 40
Timers 24 bit with 5 bit Prescaler 8 bit with 8 bit Prescaler 8 bit with 8 bit Prescaler (Watchdog Timer for SYSFAIL)	 2 3 1
VSB Master Interface A32: D8, D16, D32, D(0), UAT, RMW Bus Arbiter Interrupt Handler	yes yes Serial IHP
RESET, TEST, RUN and CACHE Switch	yes
VMEPROM Firmware on all Board Versions	128 Kbyte
Power Requirements + 5V min/max +12V min/max −12V min/max	 4.3/5.9A 0.1/0.2A 0.1/0.2A
Operating Temperature (Degrees C) Storage Temperature (Degrees C) Relative Humidity (non-condensing in %)	0 to 50 −40 to 85 0 to 95
Board Dimensions (mm) (in)	234 x 160 9.2 x 6.3
No. of Slots used	1

Ordering Information

SYS68K/CPU-31 Part No. 101310	16.7 MHz 68030 based CPU board with VSB interface 68882 FPCP, DMAC, 256 Kbyte S-DPR capacity and VMEPROM. Documentation included.
SYS68K/CPU-31A Part No. 101311	20.0 MHz 68030 based CPU board with VSB interface 68882 FPCP, DMAC, 256 Kbyte S-DPR capacity and VMEPROM. Documentation included.
SYS68K/CPU-31XA Part No. 101312	20.0 MHz 68030 based CPU board with VSB interface 68882 FPCP, DMAC, 1 Mbyte S-DPR capacity and VMEPROM. Documentation included.
SYS68K/SMDP-06 Part No. 101104	1 Mbyte static RAM board replacing the 256 Kbyte SMDP-05 board installed on the CPU-31 and CPU-31A.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM User's Manual
SYS68K/CPU-31/UM Part No. 800147	User's Manual for the SYS68K/CPU-31 products, including VMEPROM User's Manual.

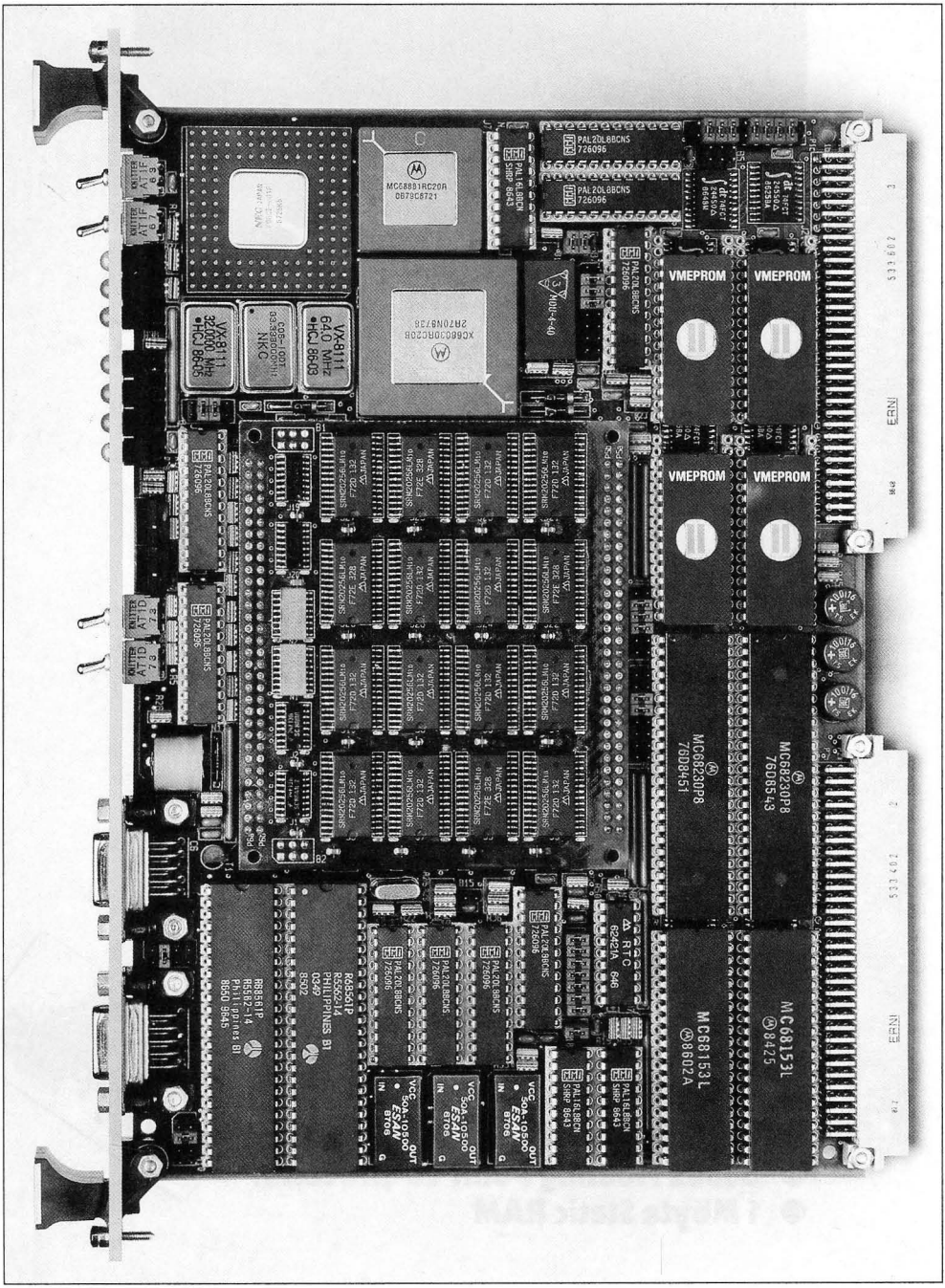
Note: SYS68K/CPU-31 board versions without the 68882 FPCP are available upon special request.



System 68000 VME SYS68K/CPU-32

High Performance 68030 Multiprocessor CPU Board with VSB Interface

- No Wait State 68030
- On Chip PMMU
- 68882 Floating Point Co-processor
- 1 Mbyte Static RAM


VMEPROM
VMEPROM
VMEPROM
VMEPROM
MC68230P8
MC68230P8
MC68153L
MC68153L
MC68881RC20R
PAL20L8BCNS
PAL16L8BCN
RTC
VX8111
32.000 MHz
VX8111
64.000 MHz

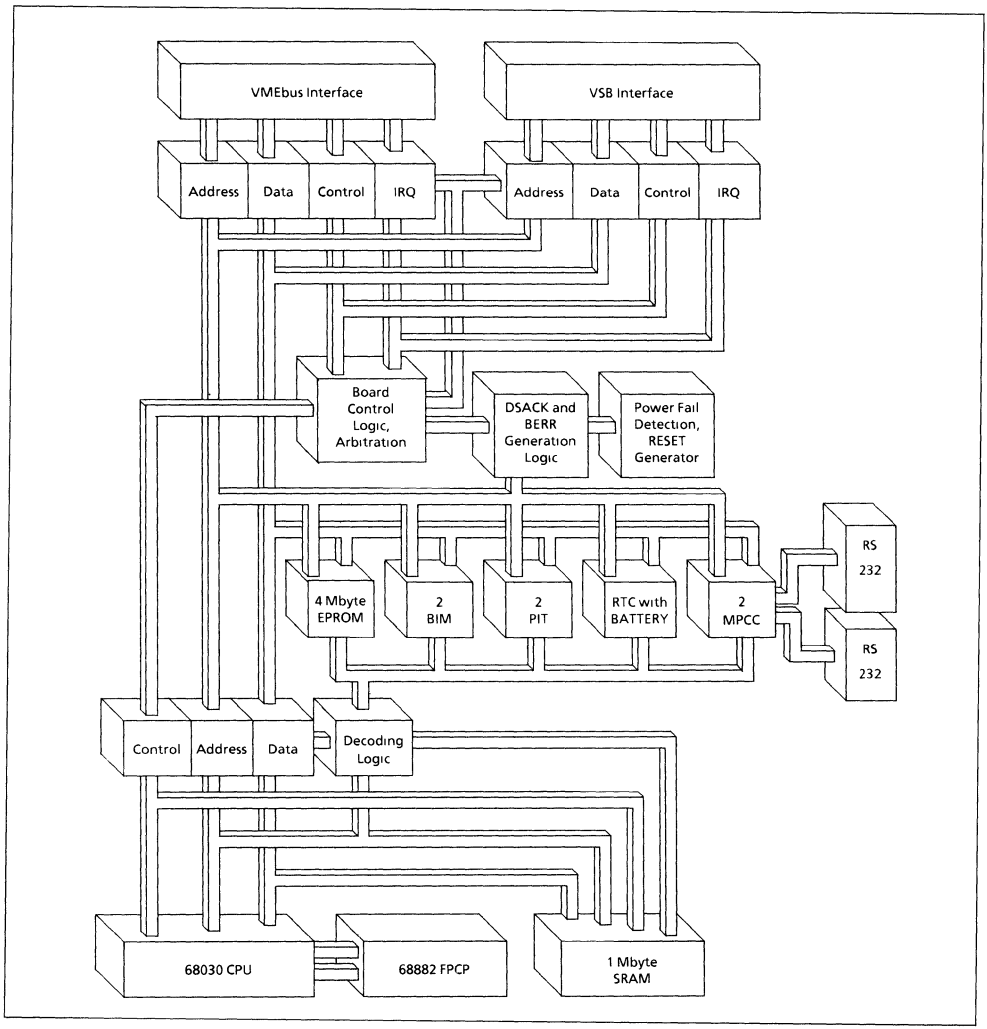
1. General Description

The SYS68K/CPU-32 is an ultra high speed CPU board using a 68030 with a clock frequency of up to 30 MHz. The SYS68K/CPU-32 is fully software compatible to the SYS68K/CPU-29 board. The SYS68K/CPU-32 uses only a single VMEbus slot. A static RAM of up to 1 Mbyte capacity can be accessed from the CPU (30 MHz clock frequency) without the insertion of wait states for all read and write cycles. A full 32 bit VSB interface including bus arbitration and Interrupt Handling is installed on all CPU-32 board versions. Two serial I/O interfaces (RS232 compatible) provide asynchronous and synchronous data transfer rates of up to 38400 baud/2 Mbit/sec.

The EPROM area consists of 4 devices supporting the 28 and 32 pin JEDEC standard providing a maximum capacity of 4 Mbyte. Two fully independent 24 bit timers, a Real Time Clock with an on-board battery backup and the full 32 bit VMEbus master interface complete the board.

In addition, VMEPROM, the PDOS* compatible multi-user real time monitor/debugger is installed on the SYS68K/CPU-32 boards.

BLOCK DIAGRAM OF THE CPU-32XC



2. Features of the SYS68K/CPU-32

- 68030 CPU (16.7 MHz) on CPU-32X
  (20.0 MHz) on CPU-32XA
  (25.0 MHz) on CPU-32B, -32XB
  (30.0 MHz) on CPU-32XC
- 68882 FPCP (16.7 MHz) on CPU-32X
  (20.0 MHz) on CPU-32XA, -32XB
  (25.0 MHz) on CPU-32XC
- 68561 Multi Protocol Communication Controllers (2x) for serial I/O data transfers (RS232 compatible)
- 68230 Parallel Interface and Timer devices (2x) for local control and timer function
- 68153 Bus Interrupter Modules (2x) for all local interrupt management

256 Kbyte or 1 Mbyte of constant zero wait state static RAM

- Up to 4 Mbyte of EPROM using 4 EPROMs (28 and 32 pin JEDEC standard) building a 32 bit data path
- VSB interface (full 32 bit) with single level arbiter A32, A24, A16 : D(0), D8, D16, D32
  Unaligned transfers
  Read-modify-write transfers
  Interrupt Handler
- VMEbus interface (full 32 bit) with single level arbiter A32, A24, A16 : D(0), D8, D16, D32
  Unaligned transfers
  Read-modify-write transfers
- Bus timer
- Power monitor
- SYSRESET generator
- RUN/HALT/CACHE and TEST function switches
- Status indication LEDs
- 2 HEX rotary switches
- Fully software compatible to the SYS68K/CPU-21 series of boards
- VMEPROM installed

3. Hardware Description

3.1 The 68030 CPU

The 68030 with its 32 bit address and data paths is installed on the SYS68K/CPU-32 board.
The CPU includes a 256 byte instruction and 256 byte data cache which significantly reduces the number of bus cycles needed for program fetches. A CACHE switch on the front panel allows the user to enable or disable the on-chip cache for software debugging purposes.
The 68030 CPU accesses the static RAM with 30 MHz clock frequency constantly without the insertion of wait states. This allows the design to take full advantage of the throughput of the CPU.
The EPROM area, the Floating Point Coprocessor, the RAM and the VSB interface are directly connected to the CPU data and address bus interface (as shown in the block diagram of the SYS68K/CPU-32).
The clock frequency of the CPU ranges from 12.5 to 30 MHz. This offers, in combination with the RAM, a real computing rate of 4-10 MIPs.

3.2 The Floating Point Coprocessor

The SYS68K/CPU-32 is fitted with the enhanced 68882 Floating Point Coprocessor (FPCP). The FPCP conforms to the IEEE Floating Point standard 754 (draft 10.0).
Easy floating point operation control to the coprocessor is provided because the intercommunication between the CPU and the FPCP is built in silicon.
An internal register set inside the FPCP of 8 general purpose registers (80 bit wide) yields fast execution times.

Features of the FPCP

- 8 general purpose registers (80 bit, 64 bit Mantissa, 15 bit exponent and one sign bit)
- 67 bit on-chip ALU
- 67 bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 standard (draft 10.0)
- Full support of trigonometrical and logarithmic functions such as:
  SINE and COSINE
  TANGENT and COTANGENT
  Hyperbolic functions (tangent, arc tangent, sine and cosine)
  Logarithmic functions (4)
  Square root and exponential functions (4)
- The 68882 is fully software compatible to the 68881 FPCP

3.3 The Static RAM

The SYS68K/CPU-32 contains a high speed static RAM offering constant no wait state access for CPU access cycles. This 32 bit wide memory allows to take full advantage of the CPU execution speed. An upgrade to 4 Mbyte RAM is possible, as the RAM is located on a memory module which can easily be replaced if higher density modules become available.
The memory bandwidth of the SYS68K/CPU-32 reaches 40 Mbyte/sec in the 30 MHz version without any need for refresh because static RAMs are used.
The low cost 16.7 MHz versions (SYS68K/CPU-32X) access the static RAM (1 Mbyte) constantly without the insertion of wait states.

On the 20.0 MHz and 25.0 MHz version (SYS68K/CPU-32XA/-32XB) 100ns devices (32 K x 8) are installed providing a constant one wait state access to the RAM.
The 30 MHz board version (CPU-32XC) uses 256 K x 1 oriented devices with an access time of 35 ns to guarantee the constant zero wait state operation of the CPU.
The following table lists the CPU board type, the memory capacity as well as the required number of wait states for accessing the SRAM area. External battery backup is supported through the +5V STDBY line of the VMEbus on all CPU-32 boards excluding the CPU-32XC.

Board Type	CPU Clock Frequency (MHz)	SRAM Capacity (byte)	No. of Wait States
CPU-32X	16.7	1 M	0
CPU-32XA	20.0	1 M	1
CPU-32XB	25.0	1 M	1
CPU-32XC	30.0	1 M	0

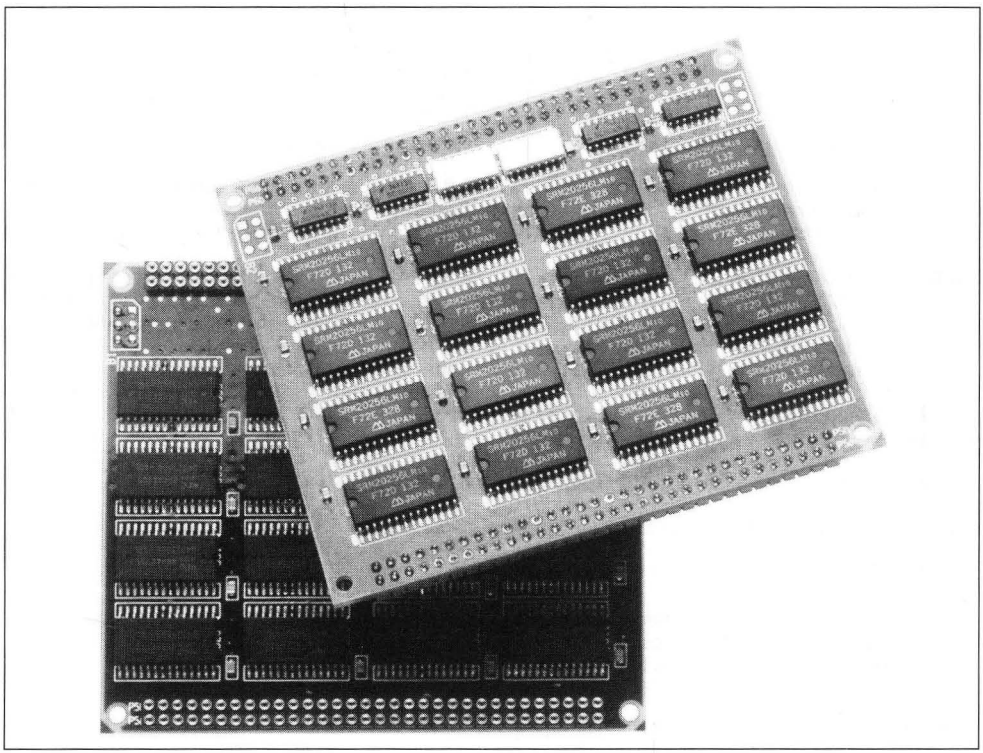
3.4 The EPROM Area

The SYS68K/CPU-32 contains four user EPROM sockets supporting 28 or 32 pin EPROM devices. Maximum data throughput to the 68030 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation if 100 ns devices are used. The following table lists the supported device types and the memory capacity.

Supported Device Types in the User EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
2764	28	8K x 8	32 Kbyte
27128	28	16K x 8	64 Kbyte
27256	28	32K x 8	128 Kbyte
27512	28	64K x 8	256 Kbyte
271024	32	128K x 8	512 Kbyte
TBD	32	256K x 8	1 Mbyte
TBD	32	512K x 8	2 Mbyte
TBD	32	1M x 8	4 Mbyte

PHOTO OF THE MEMORY MODULE



3.5 The Serial I/O Channels

The SYS68K/CPU-32 contains two Multi Protocol Communication Controllers (MPCC 68561) which include the following protocol features:

- Character oriented protocols BSC, DDCMP, X3.28, X.21, ECMA16
- Synchronous bit oriented protocols SDLC, HDLC, X.25
- CRC check selectable
- Eight character receiver and buffer registers
- Software programmable baud rate from 110 to 38400 baud
- DC data rate of up to 2 Mbit/s

The two RS232 compatible interfaces are installed on the front panel via two 9 pin D-Sub connectors. The following I/O signals are supported with onboard driver/receiver circuits:

Signal	Input	Output	9 Pin DSUB Connector	Description
DCD	X		1	Data Carrier Detect
RXD	X		2	Receive Data
TXD		X	3	Transmit Data
DTR		X	4	Data Terminal Data
GND			5	Signal GND
DSR	X	X	6	Data Set Ready
RTS		X	7	Request to Send
CTS	X		8	Clear to Send
–	–	–	9	Not Connected

Each MPCC is able to interrupt the local CPU on a software programmable level. The interrupt vector is also software programmable.

3.6 The Local Control Devices

The SYS68K/CPU-32 contains two independent Parallel Interface and Timer devices (PI/T 68230), for local control and status display.
The clock frequency of each PI/T is 8.064 MHz on all different board versions. Eight control bits can be read via the PI/T port A. These control bits can be set via two HEX rotary switches available on the front panel for manipulation. In addition, 8 status bits can be read out via the second PI/T. The status bits can be used for setting different configurations, defining the slot number in a VMEbus multiprocessor system etc.
The PI/T also allows to program the bus release functions such as:

RAT = Release after Timeout
ROR = Release on Request
REC = Release every Cycle
RBCLR = Release on Bus Clear

In addition, the board type (CPU-32) and the installed memory capacity can be read out via a PI/T.

The two fully independent 24 bit timers with their 5 bit prescaler can be used to interrupt the local CPU on a software programmable level. The interrupt vector is also software programmable inside the Bus Interrupter Module.
All of the 7 interrupt request levels of the CPU can be separately enabled or disabled via port B of the first PI/T. For example, this allows you to disable all interrupts on a certain IRQ level by debugging the application software.
The SYSFAIL and ACFAIL signals of the VMEbus are connected to the first PI/T to eventually interrupt the local CPU (if programmed) or to monitor the status of these signals.

3.7 The Real Time Clock

A software programmable Real Time Clock (RTC-62421) with onboard battery backup is installed on the SYS68K/CPU-32 boards. The features of the Real Time Clock are listed below.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12hr/24hr clock switchover
- Automatic leap year setting
- Interrupt masking
- C-MOS design provides low power consumption during power down mode.

The Real Time Clock is able to interrupt the local CPU on a software programmable level (1 to 7).

3.8 The Local Interrupt Sources

Two Bus Interrupter Modules (BIM 68153) are installed on the SYS68K/CPU-32 to manage all the local interrupts.
Each local interrupt source can be routed to one of the seven different IRQ levels of the CPU. The interrupt vector is also software programmable.

Local Interrupt Sources:

1) Test Switch
2) MPCC 1
3) MPCC 2
4) PI/T 1 Timer
5) PI/T 2 Timer
6) RTC
7) VSB-IRQ
8) ACFAIL
9) SYSFAIL

4. The VSB Interface

The SYS68K/CPU-32 board is delivered with a full 32 bit VSB master interface.
Maximum data throughput is provided on the VSB interface by supporting 32 bit of data via the 4 Gbyte address range. the VSB address range is decoded out of the 4 Gbyte address space of the 68030.
The following data transfer types are supported:

A32:D8, D16, D32
Unaligned Transfers
Address Only Cycles
Read Modify Write Transfers

The VSB interface allows to build contiguous memory beyond the local SRAM. The local control logic provides an access cycle to the VSB interface before addressing the VMEbus. This technique allows an increase of the overall throughput of systems using the secondary bus. If the VSB interface is not required, a jumper setting allows to disable it and forces VMEbus accesses if there is no on-board access cycle detected.
The serial arbiter and the IHP Interrupt Handler complete the VSB interface.

5. The VMEbus Interface

The SYS68K/CPU-32 includes a full 32 bit VMEbus interface, thereby taking full advantage of the VMEbus specification.
The Address Modifier codes for A16, A24 and A32 addressing are fully supported.

The following data transfer types are supported:

Transfer Type	D31-D24	D23-D16	D15-D8	D7-D0
Byte				X
			X	
Word			X	X
Long Word	X	X	X	X
Unaligned Transfers	X	X	X	
		X	X	
		X	X	X
Read Modify Write				X
			X	X
	X	X	X	X

The SYS68K/CPU-32 includes the following bus arbitration modes:

RWD	Release when done
ROR	Release on request
RBCLR	Release on Bus Clear
RAT	Release after Timeout

Each of the listed modes is software programmable inside the Gate Array. The bus request level of the SYS68K/CPU-32 is jumper selectable (BR0-3). A single level arbiter, a power monitor, a SYSRESET generator and support for ACFAIL and SYSFAIL complete the VMEbus interface.

6. The VMEPROM

6.1 General Description

VMEPROM is an EPROM based real time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM.
VMEPROM is composed of the powerful PDOS Real Time Kernel and the PDOS file manager. Thus the package provides support of a highly sophisticated Real Time Kernel and an interface to floppy and hard disk drives.
The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition, it includes a powerful line assembler and disassembler for the 68030 and the 68882.

VMEPROM features:

- Real-Time Multitasking Kernel supporting up to 64 tasks.
- File management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Line assembler/disassembler with full support of all 68030/68882 instructions.
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify.
- S-record up/downloading from any port defined in the system.
- Disk support for RAM-disk, floppy and Winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. VMEPROM also allows disk formatting and initialization.
- Serial I/O support for up to two SIO-2 or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full screen editor.
- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.

6.2 Description of the User Interface of VMEPROM

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple command lines may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

6.3 Description of the Kernel Functions

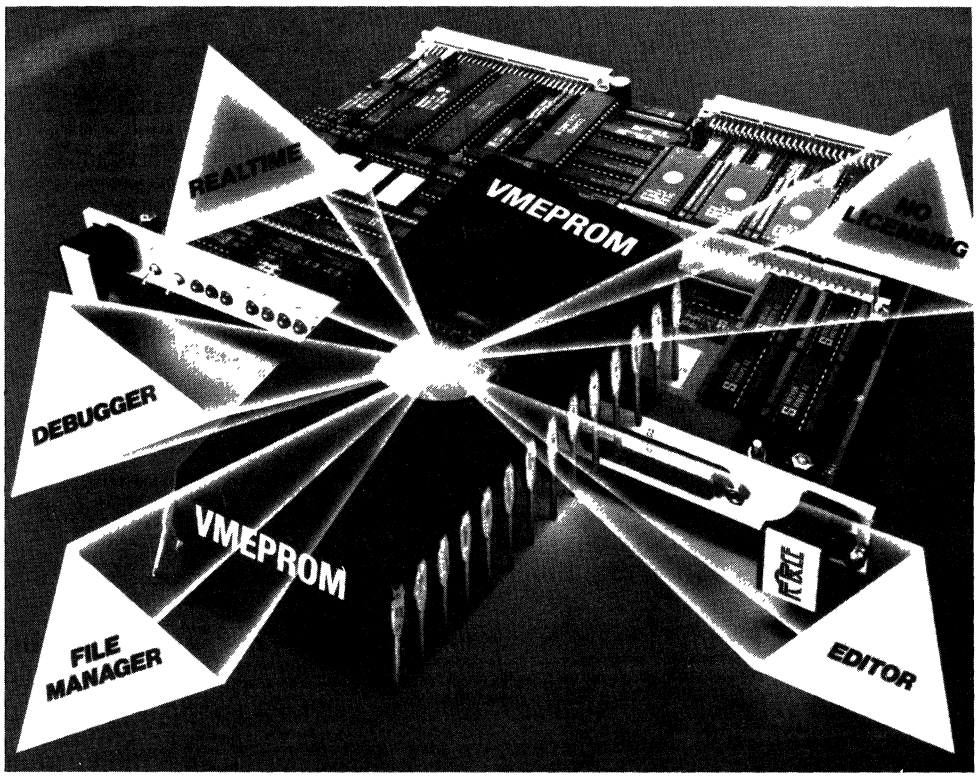
The kernel of VMEPROM is written in 68030 assembly language for fast and efficient execution. It provides multitasking, system clock,event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously.
Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

6.4 Description of the File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

6.5 Supported VMEbus Hardware

Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards and one disk controller.
In addition, EPROM programming is supported by VMEPROM utilizing the SYS68K/RR-2/3 board family.



6.6 Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 40 Kbyte. Small romable applications can be put in EPROMS easily without the overhead of the user interface.

6.7 Development Systems

Currently either one of the FORCE PDOS* or UNIX* System V development stations may be used for software development for VMEPROM.
Compilers, assemblers, and libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.
The support of VMEPROM through other development systems like the IBM-AT or the VAX is under development. These crosssoftware development packages will include C-compiler, assemblers for the 68030 and libraries to generate codes to run under control of VMEPROM.

6.8 Licensing

No license is required for VMEPROM. VMEPROM is delivered free of charge with every CPU-32 board. For more detailed information please refer to the SYS68K/VMEPROM Data Sheet.

7. Specifications of the SYS68K/CPU-32

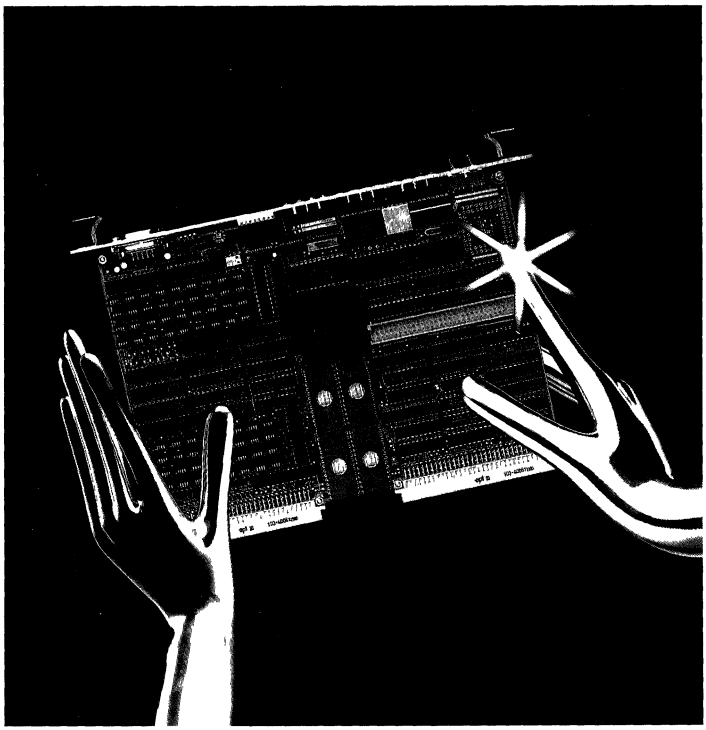
Functions

68030 CPU Clock Frequency on:	
CPU-32X	16.7 MHz
CPU-32XA	20.0 MHz
CPU-32XB	25.0 MHz
CPU-32XC	30.0 MHz
68881 FPCP Clock Frequency on:	
CPU-32X	16.7 MHz
CPU-32XA/-32XB	20.0 MHz
CPU-32XC	25.0 MHz
Local RAM Type	SRAM
Data Path	32 bit
Memory Capacity	1 Mbyte
No.of Wait States – CPU-32XA/-32XB	1 (all cycles)
No.of Wait States – all others	0 (all cycles)
No. of EPROM Sockets	4
Data Path	32 bit
Max. Capacity	4 Mbyte
No. of Wait States (min/max)	1/8
Serial I/O Interfaces	2
Used Controller	2 x 68561
RS232 compatible	Yes
Real Time Clock	62421
On-Board Battery Backup	Yes
24 bit Timer	2

VSB Master Interface A32 : D(0), D8, D16, D32 Arbiter Interrupt Handler	Yes Yes Serial IHP
VMEbus Master Interface A32, A24, A16: D(0), D8, D16, D32 Unaligned Data Transfers Read-Modify-Write Cycles Single Level Bus Arbiter VMEbus Interrupt Handler	 Yes Yes Yes Yes IH 1 to 7
RESET, TEST, CACHE, HALT Function Switches	Yes
VMEPROM Firmware on all Board Versions	128 Kbyte
Power Requirements + 5V typ/max +12V typ/max −12V typ/max	 4.9/5.9A 0.1/0.2A 0.1/0.2A
Operating Temperature (Degrees C)	0 to 50
Storage Temperature (Degrees C)	−40 to 85
Relative Humidity (noncondensing %)	0 to 95
Board Dimensions (mm) (in)	234 x 160 9.2 x 6.3
No. of Slots used	1

Ordering Information

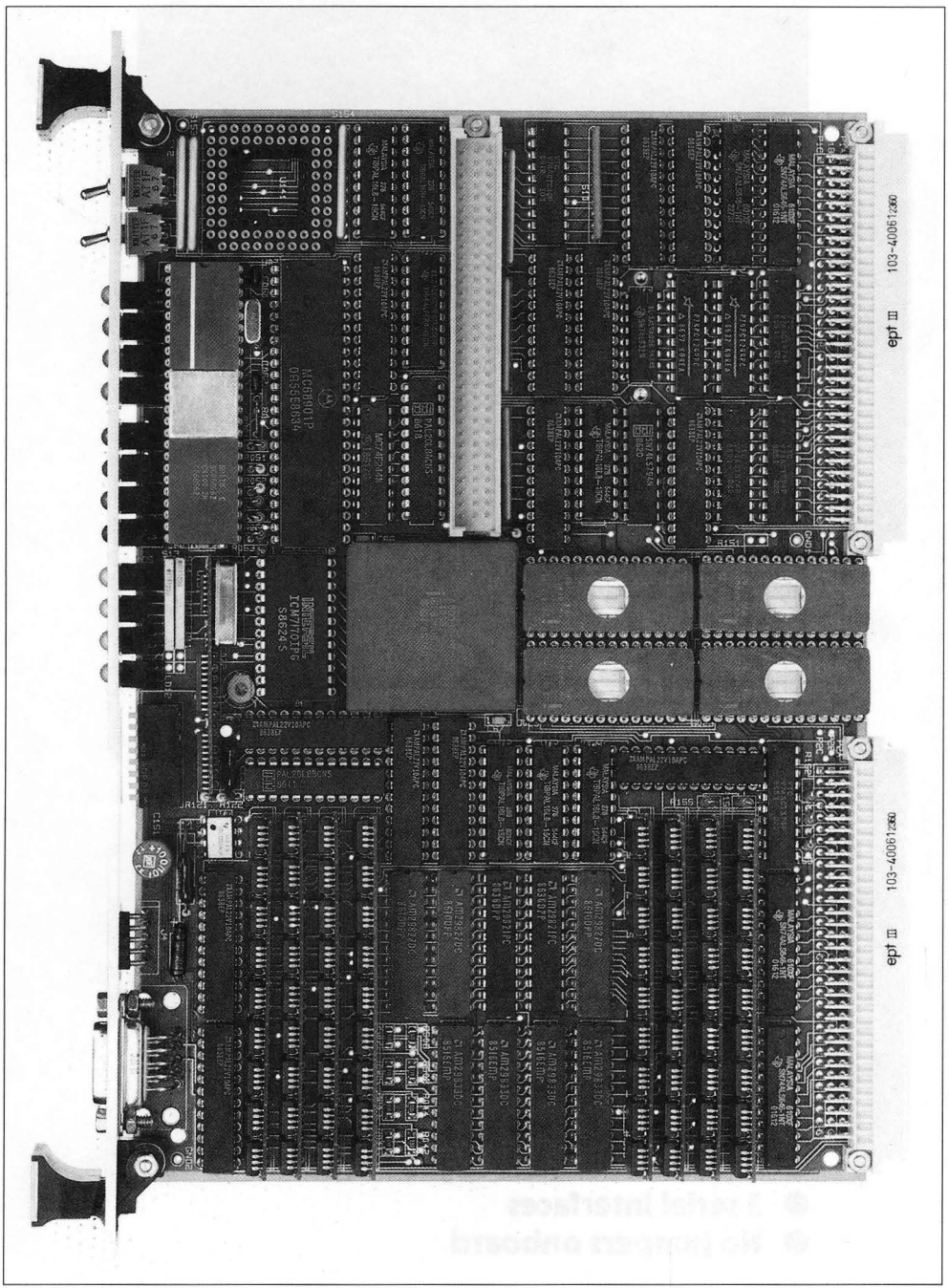
SYS68K/CPU-32X Part No. 101324	16.7 MHz 68030 CPU board with 1 Mbyte zero wait state SRAM, FPCP and VMEPROM. Documentation included.
SYS68K/CPU-32XA Part No. 101321	20.0 MHz 68030 CPU board with 1 Mbyte one wait state SRAM, FPCP and VMEPROM. Documentation included.
SYS68K/CPU-32XB Part No. 101322	25.0 MHz 68030 CPU board with 1 Mbyte zero wait state SRAM, FPCP and VMEPROM. Documentation included.
SYS68K/CPU-32XC Part No. 101333	30.0 MHz 68030 CPU board with 1 Mbyte zero wait state SRAM, FPCP and VMEPROM. Documentation included.
SYS68K/VMEPROM/UM Part No. 800140	User's Manual of VMEPROM excluding documentation of the SYS68K/CPU-32.
SYS68K/CPU-32/UM Part No. 800148	User's Manual for all SYS68K/CPU-32 board versions. VMEPROM documentation included.



System 80386 VME SYS80K/CPU-386

80386 High Performance 32-Bit CPU Board

- 80386 processor running at 16 MHz without insertion of wait states
- 2 (8) Mbyte of onboard DRAM
- Optional numeric coprocessor
- 3 serial Interfaces
- No jumpers onboard

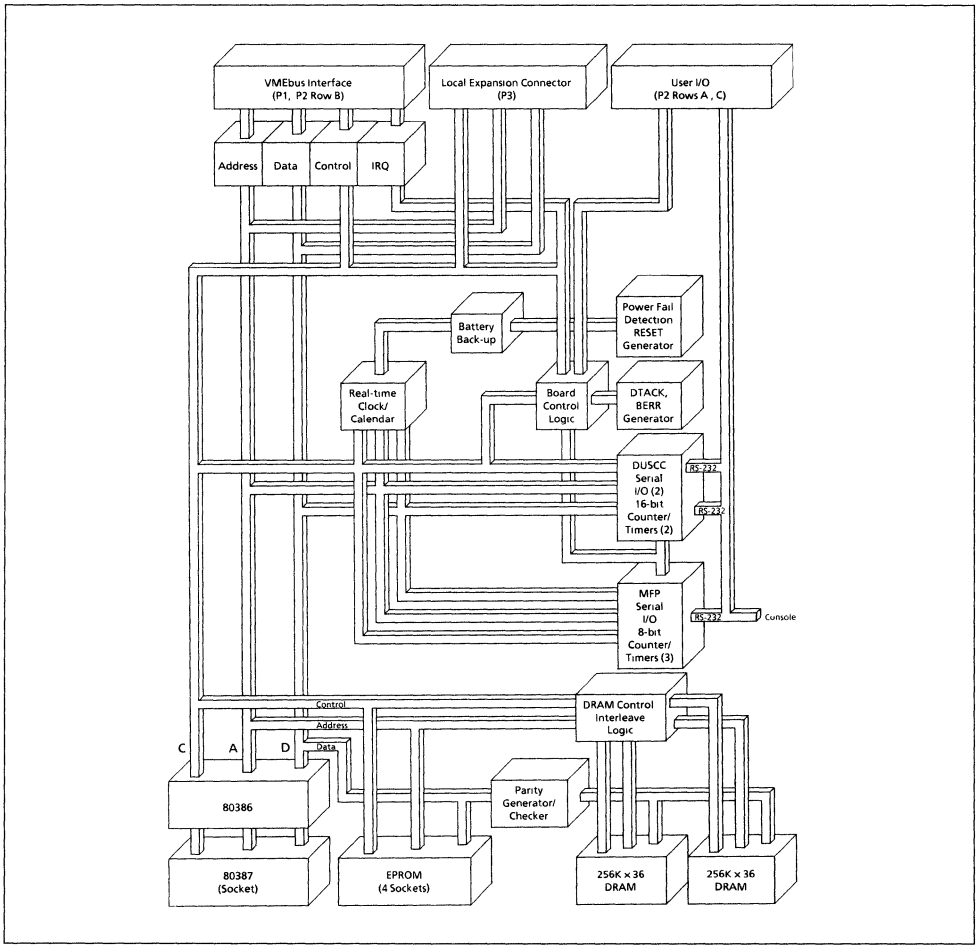


General Description

The SYS80K/CPU-386 is a high-performance CPU board designed using an 80386 32 bit microprocessor. The board is built for the VMEbus IEEE 1014 system environment and provides four sockets for JEDEC compatible memory devices (EPROMs, EEPROMS), 3 serial I/O ports, time-of-day/real-time clock/calendar, two 16-bit and three 8-bit counters/timers, and a socket for installation of an 80387 numeric coprocessor.
The SYS80K/CPU-386 is available with 2 or 8 Mbyte of parity-checked dynamic RAM. This local memory has been configured to provide zero wait state operation at 16 MHz for read and write cycles.

A powerful debugging package with full 80386 and 80387 line assembler/disassembler capabilities called FORCEbug/386 is included. FORCEbug/386 also features test facilities, floating point coprocessor support, benchmark routines, and macro facilities.
A photo of the CPU-386 is shown on the preceding page, and a block diagram is presented below.

BLOCK DIAGRAM OF THE SYS80K/CPU-386



Features of the CPU-386

- 80386 Processor with a clock frequency of 16 MHz
- Optional 80387 Numeric Coprocessor (CPU-386A, CPU-386C)
- 68901 Multi-Function Peripheral with Serial I/O (RS-232C used for console and debugging port), interrupt support, and three user-programmable 8 bit timers
- 68562 Dual Universal Serial Communications Controller with two multi-mode serial channels (RS-232C) each with 4-character input and output FIFOs and two 16 bit timers
- 7170 Real Time Clock with alarm and program-accessible year, month, date, day, hours, minutes, seconds and hundredths of seconds, and settable alarm
- 2 or 8 Mbyte of zero wait state, dynamic RAM with parity, in an interleaved configuration supported by look-ahead logic to minimize wait states (if any) for consecutive accesses to the same bank
- 4 sockets for 8 K x 8 to 64 K x 8 EPROMs, EEPROMs and page-mode byte-wide devices
- Fully buffered 32 bit local address and data buses
- Full VMEbus interface
  - A16, A24, and A32 address modes
  - D8, D16, and D32 data modes
  - User/supervisor and program/data address modifier code support
  - Unaligned transfers
  - 16 MHz system clock
  - Address pipelining
- 4-level Bus arbitration supporting "Round Robin", "Prioritized" and "single-level" algorithms
- Interrupt handler (Local, VME IRQ1-IRQ7, optional Autovectors, & 2 non-maskable interrupts)
- VMEbus system controller
  - 16 MHz system clock
  - Bus timer
  - Arbiter
- Bus Timer for BERR generation
- RESET generator
- Front Panel LED Indicators
  GREEN: EPROM, RAM, I/O & VMEbus accesses
  RED: HALT, SHUTDOWN, PARITY & BERR
  YELLOW: 4 User-definable indicators
- Front Panel Switches (momentary contact): RESET & ABORT
- "Smart" jumpers set under program control
- Custom geographical addressing simplifies configuration
- Electronic Tag Module Socket for providing user-defined configuration information
- Four debug registers and programmable single-step flag for simplified program debugging
- FORCEbug/386 Debugger Firmware with 80387 Numeric Coprocessor support, Macro facilities and Assembler/Disassembler

1.0 Hardware Description

1.1 The 80386 CPU

The 80386 processor is a highly-integrated device containing a central processing unit, memory management unit and bus interface unit. This processor features 32 bit wide internal and external data buses, and is implemented on board to take full advantage of the 32 bit VMEbus structure.
The clock speed of the 80386 is set at 16 MHz. Coupled with a pipelined architecture, zero wait state, 32 bit wide dynamic RAM, and a 16 byte prefetch instruction queue that reduces bus overhead, the 80386 operates with 3 to 4 MIPs of effective computing power.
An extensive instruction set which includes eleven addressing modes has been incorporated into the 80386. All instructions are orthogonal supporting 8, 16, 24, and 32 bit data structures. The 80386 can address 4 gigabytes of physical memory and the on-chip memory management unit fully supports virtual addressing. Additionally, the 80386, in emulation mode, will execute programs written for the 8086/8088/80286/80386 family.
A fully buffered address and data bus has been implemented for the CPU to communicate to local I/O and memory.

1.2 The 80387 Numeric Coprocessor

The 80387 is a high-performance floating point coprocessor designed to improve the throughput of 80386 mathematical and trigonometric calculations. The 80387 implements the IEEE754 floating point standard, with high-precision 80 bit architecture and full support for single, double, and extended precision operations.
An 809387 Numeric Coprocessor is installed on the CPU-386A and CPU-386C only.

1.3 The Serial I/O Channels

The CPU-386 board contains three serial communication channels. The 68562 Dual Universal Serial Communications Controller (DUSCC) provides two of the three channels. Input/Output using the DUSCC supports the following protocols:

- Character-Oriented Protocols
  BISYNC, DDCMP, X.21
- Synchronous Bit-Oriented Protocols
  SDLC, HDLC, X.25
- Even, Odd or no Parity check
- CRC check selectable
- Four character receiver and four character transmitter FIFOs
- Software Programmable Standard Baud Rates from 110 to 38,400 Baud
- DC data rate to 4 Mbit/sec

RS-232 compatible interfaces (both ports) are installed on the board to provide direct connection to standard terminals. User connection has been configured such that a standard flat cable terminated in a 9-pin D connector provides an IBM PC/AT style interface (both ports). The second port also supports modem control signals. Both serial ports are accessible through the VMEbus P2 connector.
A 68901 Multi-Function Peripheral Controller (MFP) provides a third serial communication channel. This port is normally programmed to 9600 baud by FORCEbug/386 at power-up, and an IBM AT style 9-pin D connector on the front panel enables this channel to be used as console and debugging port with the following features:

- Full duplex operation
- Asynchronous to 19,200 bits/sec
- Synchronous to 1 Mbit/sec

Each of the three serial I/O channels (DUSCC and MFP) is capable of issuing an interrupt to the processor. The interrupt vector values are programmable.

1.4 Real Time Clock

An ICM7170 Real Time Clock, with 10-year battery backup, provides a user-accessible clock/calendar. Year, month, date, day, hours, minutes, seconds, and hundredths of a second may be read and written under program control. An alarm function can also be programmed and enabled to generate an interrupt.
The real time clock can be used to output a periodic interrupt at any one of six different rates from 100 Hz to once per day.

1.5 Programmable Counter/Timers

Four programmable counter/timers available to applications are provided on the CPU-386 board. Three of the counter/timers are 8 bits wide (68901: A, B, C) and the remaining counter/timer is 16 bits wide (68562: A, B).
Eight-bit counter A may be programmed to operate in delay, count, or pulse-width mode. Counter C functions primarily as a rate generator. Prescale selection of 4 to 200 extends the dynamic range of these three counters. Additionally, counters A and B have their auxiliary inputs, used in pulse-width mode, connected to the user I/O pins on the VMEbus P2 connector. Interrupts for counters A, B, and C may be enabled/disabled under program control.
Sixteen-bit counter A may be programmed to perform delay generation, automatic bit-length measurement, count received or transmitted characters, event counter, or non-standard bit-rate generator. This counter can be prescaled by 16, 32, or 64. Interrupt for counter A may be enabled/disabled under program control.

1.6 Interrupt Handling

The 80386 processor provides vector-defined interrupt support. Two interrupt lines, one maskable, the other non-maskable, are used to inform the 80386 of interrupt requests. All interrupts generated by IRQ1*-IRQ6* from the VMEbus, as well all local (on-board) devices, are routed to the maskable interrupt input of the 80386. The VMEbus IRQ1*-IRQ6* interrupts are individually maskable through bits programmatically set and reset in the Board Interrupt Mask Register. Interrupts IRQ1*, IRQ3*, and IRQ5* may also be implemented using Autovectoring.
The non-maskable interrupt input of the 80386 supports two functions; VMEbus IRQ7* and the ABORT switch on the front panel of the CPU-386.

1.7 Local Read/Write Memory

Two megabytes configured as two banks of 256 K x 36 bits or 8 Mbyte configured as 1 Mbyte x 36 bits of dynamic read/write, pipelined zero wait state memory are provided on the CPU-386 board. Dividing the on-board memory into two logical banks and using look-ahead logic for interleave access improves memory response time for transfer speeds to 32 Mbyte/sec. Parity checking is also provided.
The refresh algorithm for the on-board RAM further improves memory access speed by minimizing interference with processor memory accesses. Under normal conditions, a refresh cycle occurs only when both banks of memory are idle. Memory integrity is ensured by an on-board timer that converts memory refresh to a high priority request. A 16 byte pre-fetch instruction queue on the 80386 further eliminates most processor hold-offs due to refresh activity. The 80386 transfers opcodes to the queue in bursts of memory accesses, and then executes instructions from this queue. Memory refreshes can then occur while the 80386 is executing opcodes from its on-chip resources. In this way, the majority of refresh cycles are transparent.

1.8 Local EPROM Support

The CPU-386 contains four sockets for 28-pin JEDEC compatible EPROM devices: 2764 through 27512 or equivalent. Configuration of these sockets for devices is accomplished with "smart jumpering". EPROM, as well as EEPROM, type, size, and speed is conveniently selected by the front panel DIP switch. EPROM capacity is from 32 Kbyte to 256 Kbyte, and switch-selectable support of page mode devices increases capacity to 512 Kbyte. EPROM access is 32 bit wide, and access times down to 100 nsec (1 wait state) are supported.

Interrupt Source	Interrupt Generator
ABORT SWITCH	Direct (NMI)
VMEbus IRQ7*	Direct (NMI)
DUSCC Serial I/O (2)	DUSCC (MI)
MFP Serial I/O (1)	MFP (MI)
Real Time Clock	MFP (MI)
MFP 8 bit Counter/Timer (A, B, C)	MFP (MI)
DUSCC 16-bit Counter/Timer (A, B)	DUSCC (MI)
VMEbus ACFAIL	MFP (MI)
VMEbus SYSFAIL MFP	(MI)
DRAM Memory Parity Error	MFP (MI)
VMEbus IRQ1*-IRQ6*	BIMR (MI)
VMEbus IRQ1*, IRQ3*, IRQ5* Autovector	MFP (MI)

NOTE: DUSCC = 68562 Dual Universal Serial Communications Controller
MFP = 68901 Multi-Function Peripheral
MI = Maskable Interrupt
NMI = Non-Maskable Interrupt
BIMR = Board Interrupt Mask Register

Device Type	Organization	Total Capacity
2764	8 K x 8	32 Kbyte
27128	16 K x 8	64 Kbyte
27256	32 K x 8	128 Kbyte
27512	64 K x 8	256 Kbyte

1.9 The VMEbus Interface

A full 32 bit VMEbus interface is implemented on the CPU-386 to communicate with global memory, I/O, and other functions.
The 4 Gbyte physical address space of the 80386 processor is fully decoded. 8, 16, 24, and 32 bit data transfers are supported.
As an example, the support of unaligned transfers allows the 80386 CPU to operate with efficient throughput because a 16 bit transfer to an odd address needs only one bus cycle. Without unaligned transfer support, two bus cycles are needed because the single transfer must be split into 2 cycles, thereby impeding performance of the processor.
The CPU-386 board is designed to support fully the VMEbus address pipelining function. During normal VMEbus operation, a master completes all handshaking requirements of the current bus cycle prior to initiating the next one. Support of address pipelining enables the CPU-386 to begin subsequent cycles as soon as DTACK* (slave acknowledge) is returned. This capability reduces bus transaction overhead by overlapping address broadcasting with data transfers, and thereby improves throughput of data on the VMEbus.

Further improvement in VMEbus performance is provided by two VMEbus-related features of the CPU-386. The CPU-386 determines VMEbus access requests in advance of when a normal VMEbus cycle begins. This enables the CPU-386 to gain control of the system immediately following a release by the current master. On the completing end of the cycle, the CPU-386 is capable of "early BBSY* (Bus Busy) release", informing other masters that the VMEbus will be available. This enables the completion of arbitration by the next VMEbus master, and control of the bus is transferred immediately following release by the CPU-386. In addition, if the VMEbus is required for the next cycle, the CPU-386 will continue to assert BBSY*, prohibiting another master from arbitrating for the VMEbus. This allows the CPU-386 to retain control without arbitration. Both of these features improve the overall performance of the VMEbus by minimizing unnecessary wait time due to arbitration.
A VMEbus system controller and bus arbiter is installed on the CPU-386 for multiple CPU board configurations. The four-level VMEbus arbiter may be programmed to operate in one of three modes: "round robin", prioritized, and single-level, providing flexibility in implementing a system for highest performance.

1.10 Expansion Connector (P3)

A 96-pin local bus connector is provided on the CPU-386 board to support memory and I/O enhancements. Address, data, and controls are brought directly from the 80386 to the connector. This connector is reserved for future use by FORCE Computers.

1.11 VMEbus User I/O Connector (P2A, P2C)

The P2 connector of the CPU-386 board enables access to user I/O signals on the VMEbus backplane. Serial I/O, parallel I/O, interrupts, counter/timer inputs and outputs, and board and user status lines (LEDs) are available at rows A and C on the P2 connector. See P2 connector pin assignment.

2.0 Software Description

2.1 Features of FORCEbus/386

- Powerful command set including:
  - Test facilities
  - Debugging tools
  - Program upload/download facilities
  - Benchmark programs
- Line assembler/disassembler fully supporting all 80386 and 80387 opcodes/mnemonics and addressing modes
- Macro facility for FORCEbug/386 commands
- Recall of previous input lines using Control A
- Program execution timer with 10 msec resolution

2.2 General Description

FORCEbug/386 is an EPROM-resident debugging package for the CPU-386 board. It features test facilities, debugging tools, a powerful line assembler/disassembler for the 80386 processor, and a macro facility for use with all FORCEbug/386 commands.

The test facilities allow the user to test and debug hardware on the external bus as well as to prove functionality of all on-board devices.

The debugging tools are well suited to download programs from a host computer and debug them on the board. Included is breakpoint setting, single-stepping, continuous tracing, display and modify all processor registers and memory contents.

With the macro facility, several FORCEbug/386 commands can be combined in one command name and then executed together.

Upload and download of user application programs supports both Intel hex or Motorola S-records. The upload/download facilities of FORCEbug/386 may then be used to transfer binary program and data between a CPU-386 serial I/O port and a host system serial I/O port.

FORCEbug/386 requires 64 Kbyte of EPROM space, and resides in four 27128 EPROMS. Additionally, approximately 8 Kbyte of read/write memory are used by FORCEbug/386 for vector, parameter and macro storage.

2.3 Command Summary

1. Block Commands:

BF	Fill block of memory with constant value
BM	Move block of memory
BS	Search a block of memory for a constant value
BT	Test a block of memory
BV	Compare two blocks of memory
BX	Block translate memory

2. Memory Commands:

MM	Display/change memory including line assembly/disassembly
MD	Display memory contents in Hex and ASCII
MS	Set memory to an ASCII string
TOUCH	Set parity for all on-board RAM

3. Input/Output Commands:

PF	Change serial Input/Output port parameters
IN	Read contents of I/O location
OUT	Change contents of I/O location

4. System Commands:

BENCH	Select/execute benchmarks
TIME	Enable/disable run-time report of user programs
DATE	Set/display real-time clock
TM	Transparent Mode via Port B
HELP	Display brief summary of available FORCEbug/386 commands
VERSION	Display current version number and release date of FORCEbug/386
SELFTEST	Perform selftest of CPU-386
STATUS	Display status of on-board control registers
INTERRUPT	Enable/disable interrupt servicing
HALT	Halt CPU

5. Debugging Commands:

ASM	Assemble 80386/80387 instructions
DIS	Disassemble 80386/80387 object code
BP	Set/remove/display breakpoints
SBP	Set/remove/display software (secondary) breakpoints
RD	Display formatted 80386/80387 registers
GO	Start user program at specified address
RM	Modify 80386 registers
RL	Set register list to be displayed by RD command
T	Trace in single-step mode
TC	Set trace count

6. Macro Commands:

DIR	Display list of defined Macros
KILL	Delete defined Macro
LIST	List Macro contents
MACRO	Define a new Macro
MLOAD	Load Macros from memory
MSAVE	Save Macros to memory

7. Upload/Download Commands:

LOAD	Load serial code/data from port to memory
SEND	Save serial code/data from memory to port

8. Electronic Tag Commands:

TAG <option>	
No Option	Print list of available Tag commands
L(oad)	Loads tag data into memory
S(tore)	Stores tag data from memory
D(isplay)	Displays tag data from tag module
M(odify)	Edits tag data
E(xecute)	Executes tag configuration data

9. MMU Commands:

CD	Create segment descriptor
DD	Delete segment descriptor
DGDT	Display Global Descriptor Table
DLDT	Display Local Descriptor Table
DIDT	Display Interrupt Descriptor Table

P2 Connector Pin Assignment

P2A-1	N.C.	P2C-1	N.C.
P2A-2	+12 VDC Pullup	P2C-2	Console R x D
P2A-3	N.C.	P2C-3	Console T x D
P2A-4	+12 VDC Pullup	P2C-4	+12 VDC Pullup
P2A-5	N.C.	P2C-5	N.C.
P2A-6	Gnd	P2C-6	R x D (Ch. A)
P2A-7	N.C.	P2C-7	T x D (Ch. A)
P2A-8	Gnd	P2C-8	+12 VDC Pullup
P2A-9	N.C.	P2C-9	N.C.
P2A-10	RTS (Ch. B)	P2C-10	R x D (Ch. B)
P2A-11	CTS (Ch. B)	P2C-11	T x D (Ch. B)
P2A-12	Gnd	P2C-12	+12 VDC Pullup
P2A-13	68901 Timer A Input	P2C-13	Transmit Clock (Ch. A)
P2A-14	68901 Timer A Output	P2C-14	LC (Ch. A)
P2A-15	68901 Timer B Input	P2C-15	RTS (Ch. A)
P2A-16	68901 Timer B Output	P2C-16	Transmit Clock (Ch. B)
P2A-17	68901 Timer C Output	P2C-17	68562 I1A (Input)
P2A-18	68901 IRQ	P2C-18	68562 I1B (Input)
P2A-19	RTC IRQ	P2C-19	68562 I2A (Input)
P2A-20	N.C.	P2C-20	68562 I2B (Input)
P2A-21	Status Line (HALT)	P2C-21	68562 O1A (Output)
P2A-22	Status Line (SHUTDOWN)	P2C-22	68562 O1B (Output)
P2A-23	Status Line (Parity Error)	P2C-23	68562 O2A (Output)
P2A-24	Status Line (Bus Error)	P2C-24	68562 O2B (Output)
P2A-25	N.C.	P2C-25	N.C.
P2A-26	Status Line (User 1)	P2C-26	Status Line (EPROM)
P2A-27	Status Line (User 2)	P2C-27	Status Line (DRAM)
P2A-28	Status Line (User 3)	P2C-28	Status Line (I/O)
P2A-29	Status Line (User 4)	P2C-29	Status Line (VME)
P2A-30	User Switch No. 8	P2C-30	+5 VDC Pullup
P2A-31	VMEbus Pipeline Inhibit	P2C-31	Slot 1 Disable
P2A-32	Gnd	P2C-32	Gnd

Note: N.C. = Not Connected

Specification for CPU-386

CPU	80386
Clock Frequency	16 MHz
80387 Numeric Co-Processor	
CPU-386A, CPU-386C	Yes
CPU-386, CPU-386-B	No
On-Board DRAM	
CPU-386, CPU-386A	2 Mbyte
CPU-386B, CPU-386C	8 Mbyte
No. of Wait States	0
Byte Parity	x
User EPROM Sockets	Four 28-pin JEDEC
EPROM Capacity (Max)	512 Kbyte
Serial I/O Interfaces	3 RS-232 (2 Multi-mode)
VMEbus Interface IEEE 1014	
A32, A24, A16	x
D32, D24, D16, D08 (EO), UAT, RMW	x
VMEbus Interrupts (Software selectable)	
Maskable	IRQ1-IRQ6
Non-Maskable	IRQ7
Autovector option for	IRQ1, IRQ3, IRQ5
Arbitration (Software selectable)	
Round Robin	x
Prioritized	x
Single Level	x
RESET & ABORT Switches	x
FORCEbug/80386 Firmware	32 Kbyte
Power Requirements	
+ 5V (max)	6.0 Amps
+12V (max)	0.2 Amps
−12V (max)	0.2 Amps
Operating Temperature	0 to 50 (degrees C)
Storage Temperature	−40 to 85 (degrees C)
Relative Humidity	10 to 95% (non-condensing)
Board Dimensions (L x W)	233.35 x 160 mm (9.2 x 6.3 in)
Board Height	19.20 mm (0.72 in)
Board Pitch	20.33 mm (0.80 in)
No. of VMEbus Slots required	1

Ordering Information

SYS80K/CPU-386 Part No. 105000	80386 CPU board with 16 MHz clock frequency and 2 Mbytes of zero wait-state RAM including documentation and FORCEbug/386 debugger firmware.
SYS80K/CPU-386A Part No. 105001	80386 CPU board with 80387 Numeric Coprocessor at 16 MHz clock frequency and 2 Mbytes of zero wait-state RAM including documentation and FORCEbug/386 debugger firmware.
SYS80K/CPU-386B Part No. 105002	80386 CPU board with 16 MHz clock frequency and 8 Mbytes of zero wait-state RAM including documentation and FORCEbug/386 debugger firmware.
SYS80K/CPU-386C Part No. 105003	80386 CPU board with 80387 Numeric Coprocessor at 16 MHz clock frequency and 8 Mbytes of zero wait-state RAM including documentation and FORCEbug/386 debugger firmware.
SYS80K/CPU-386/UM Part No. 800500	User Manual for all CPU-386 versions.

Memory Boards

FORCE Computers Memory Board Introduction

With this family of boards FORCE Computers has provided a solution to all your memory needs. Whether you need very large memory arrays on the VMEbus or very fast access to large arrays or maybe you need to be able to program EPROMs on the bus, FORCE Computers has the answer. This family is designed to compliment the other 32 bit designs detailed in this data book and 16 bit.

General Feature Overview

General purpose 16 bit dynamic RAM requirements are satisfied by the SYS68K/DRAM-1 and the SYS68K/DRAM-2 boards. These two boards, basically the same design, povide either 512 Kbyte (DRAM-1) or 2 Mbyte (DRAM-2) of dynamic RAM. Refresh control and a complete VMEbus interface are included in the designs. In addition, full parity protection is provided on both boards for data security.

For large memory arrays, FORCE Computers has designed the SYS68K/DRAM-E3M/S family and the SYS68K/DRAM-E4M/S family. These two designs use the concept of the FLME (Force Local Memory Expansion) interface to enable the user to expand the total memory capacity of the board to meet the requirements of the application. The DRAM-E3M1 supports 1 Mbyte of DRAM and can be expanded up to 13 Mbyte though the use of the slave modules DRAM-E3Sx. These slave boards do not have any direct interface to the VMEbus and may only be accessed through the master (DRAM-E3M1). With the use of one of the available slave boards, the capacity of the DRAM-E3M1 board will appear to be 1 Mbyte plus the capacity of the slave board. The slave boards for the DRAM-E3M1 are available in 1 Mbyte, 3 Mbyte and 6 Mbyte capacities. The DRAM-E4M4 supports 4 Mbyte of DRAM and can be expanded up to 28 Mbyte through the use of the DRAM-E4Sx modules in the same manner as describer above for the DRAM-E3M1. This family provides the solution to mass memory requirements.

The SYS68K/DRAM-6 provides a high speed dynamic RAM array for the VMEbus. The board supports data write access times of less than 90 ns. Read accesses may be achieved in less than 200ns. Data throughput of up to 30 Mbyte per second can be achieved with this board. These boards provide the dynamic RAM performance standard.

The SYS68K/RR-1 board provides the maximum flexibility with regard to the choice of memory devices that the user may wish to use. The board is shipped, either unpopulated (SYS68K/RR-1) or which may be populated with EPROM devices providing 128 Kbyte of EPROM space, or it may be shipped with 8 Kbyte SRAM devices providing 128 Kbyte of static RAM. In the static RAM configuration, battery back up is also provided for power down data retention.

If it's an EPROM board on the VMEbus that you require, then look no further than the SYS68K/RR-2 and SYS68K/RR-3. These boards offer the unique feature of being able to test your application in SRAM and then program your EPROM in a VMEbus environment without the need for expensive EPROM programmers. The board may then be used as a standard memory card. These boards provide the solution to EPROM resident applications.

The SYS68K/SRAM-3 and SYS68K/SRAM-4 boards are similar designs to the RR-2 and RR-3 boards discussed above, the SRAM-3 provides a VMEbus and a VMXbus interface, while the SRAM-4 provides only the VMEbus interface. Both boards are provided with a battery back up facility to guarantee data retention during power down situations.

If howver raw performance with the added benefit of the security offered by SRAM devices is required then the SYS68K/SRAM-5 static RAM board may be the answer. This board contains 512 Kbyte of high speed static RAM that offers access times of less than 55ns for both read and for write cycles. This board is the static RAM performance standard.

16 Bit Memory Boards

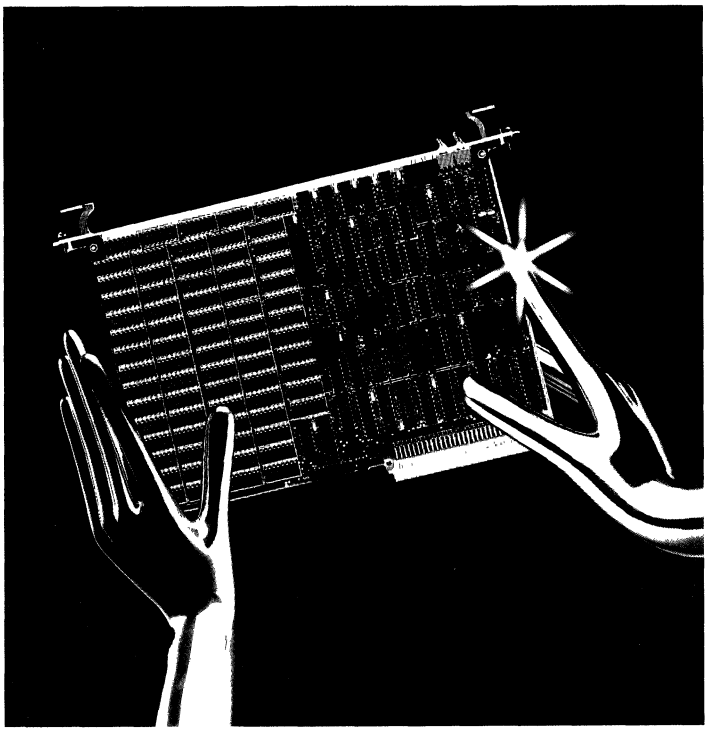
FAMILY	DRAM		SRAM		PROM/EPROM	
BOARD	DRAM-1	DRAM-2	SRAM-1	SRAM-2	RR-1	RR-1S
Capacity No. of Memory Areas Byte, Parity	512 Kbyte 2 X	2 Mbyte 2 X	Not recommended for new designs	Not recommended for new designs	max. 512 Kbyte 8 –	128 Kbyte 8 –
No. of JEDEC Sockets	–	–			16	16
Battery Back-up Board	–	–			X	X
VMEbus Interface Decoding Data Transfer Size	A24 D8, D16	A24 D8, D16			A24 D8, D16	A24 D8, D16
Read Access Time Write Access Time	320 ns 190 ns	320 ns 190 ns			Selectable Selectable	230 ns 230 ns
Detailed Description on Page:	227	227			271	271

32 Bit General Purpose Memory Boards

FAMILY	SRAM						SRAM/ROM/EPROM	
BOARD	SRAM-3A	SRAM-3B	SRAM-4A	SRAM-4B	SRAM-5	SRAM-6	RR-2	RR-3
Capacity Device Organization	Not recommended for new designs.	1 Mbyte 32K x 8	Not recommended for new designs.	1 Mbyte 32K x 8	512 Kbyte 64K x 1	2 Mbyte 256K x 1	up to 16 Mbyte Various	up to 16 Mbyte Various
Memory Areas		2		2	1	1	2	2
On Board Battery Backup (Calculated)		6000h		6000h	10000h	6000h	Device dependent	Device dependent
VMEbus Interface Decoding Decoding Boundary Data Transfer Size		A24, A32 512 Kbyte D8, D16, D32		A24, A32 512 Kbyte D8, D16, D32	A24, A32 512 Kbyte D8, D16, D32	A24, A32 2 Mbyte D8, D16, D32	A24, A32 Various D8, D16, D32	A24, A32 Various D8, D16, D32
Unaligned Transfer Read Modify Write		X X		X X	X X	X X	X X	X X
Read Access Time max. Write Access Time max.		210 ns 80 ns		210 ns 80 ns	55 ns 55 ns	55 ns 55 ns	Selectable Selectable	Selectable Selectable
VMXbus Interface Decoding Decoding Boundary Data Transfer Size		A24 512 Kbyte D8, D16, D32		– – –	– – –	– – –	A24 Various D8, D16, D32	– – –
Unaligned Transfer Ready Modify Write		X X		– –	– –	– –	X X	– –
Read Access Time max. Write Access Time max.		210 ns 70 ns		– –	– –	– –	Selectable Selectable	– –
Detailed Description on Page:		253		259	265	265	277	285

32 Bit Dynamic Memory Boards

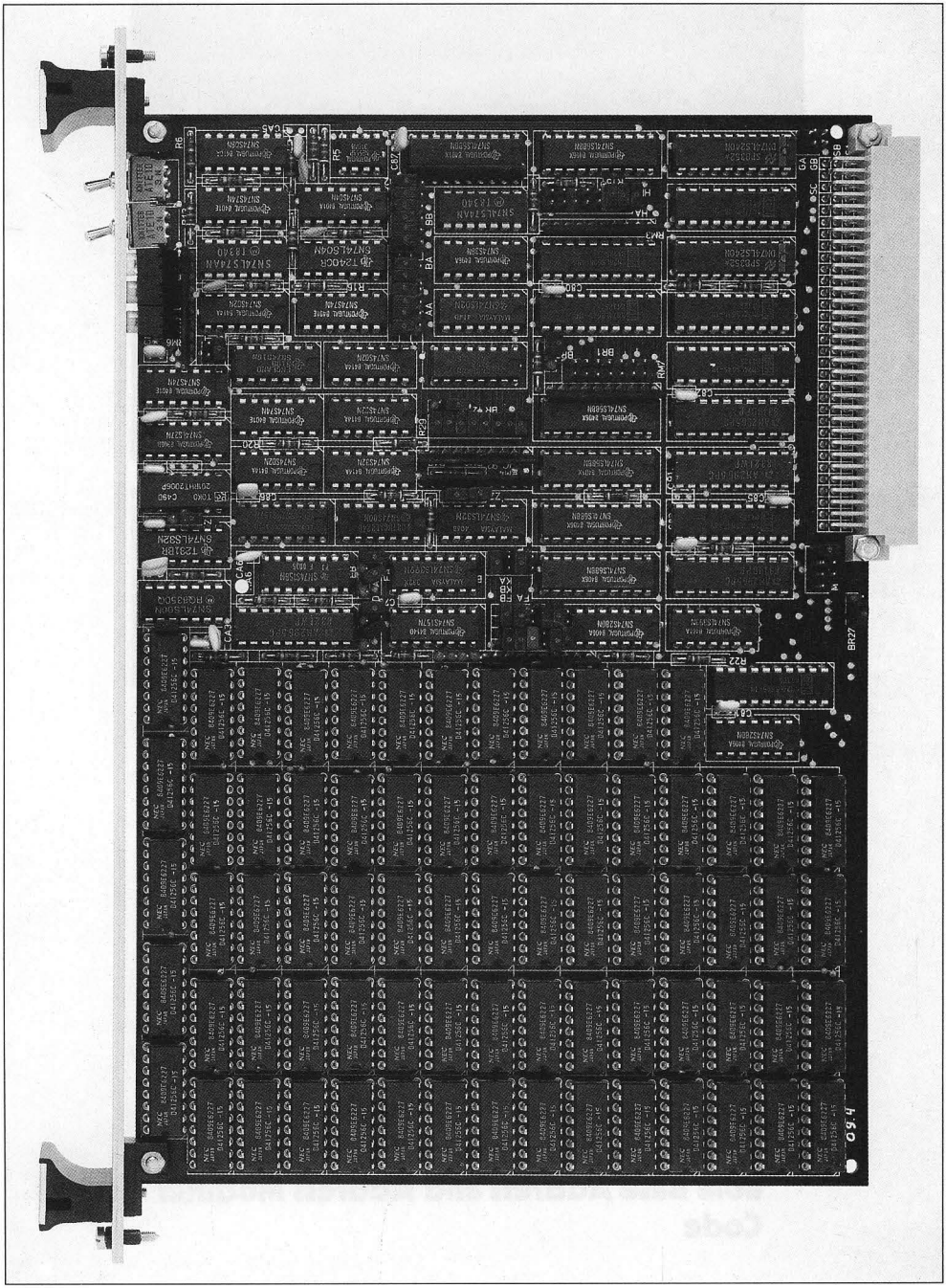
FAMILY	DRAM-E3 Series		DRAM-4 Series		DRAM-5	DRAM-6
BOARD	DRAM-E3M1	DRAM-E3S3	DRAM-E4M4	DRAM-E4S12		
Capacity Device Organization	1 Mbyte 256K x 1	3 Mbyte 256K x 1	4 Mbyte 1M x 1	12 Mbyte 1M x 1	Not recommended for new designs.	2 Mbyte 256K x 1
Byte Parity	X	X	X	X		X
Off Board Battery Back-up	X	X	X	X		–
VMEbus Interface Decoding Decoding Boundary Data Transfer Size	A24, A32 256 Kbyte D8, D16, D32	– – –	A24, A32 256 Kbyte D8, D16, D32	– – –		A24, A32 1 Mbyte D8, D16, D32
Unaligned Transfer Support Read Modify Write Support	X X	X X	X X	X X		X X
Read Access Time max. Pre-Read Access Time max. Write Access Time max.	245 ns – 65 ns	245 ns – 65 ns	225 ns – 65 ns	225 ns – 65 ns		215 ns – 105 ns
Read Ahead Logic	–	–	–	–		X
Max. No. of Board(s) No. of Slots Used	– 1	2 with 1x-E3M1 1	– 1	2 with 1x-E4M4 1		– 1
Detailed Description on Page:	231	231	239	239		247



System 68000 VME SYS68K/DRAM-1/2

16 Bit Dynamic RAM Board

- **Storage Capacity: 512 Kbyte (DRAM-1)**
  2 Mbyte (DRAM-2)
- **Byte Parity Checking**
- **A24 Addressing**
- **2 Memory Areas each with Jumper Selectable Base Address and Address Modifier Code**

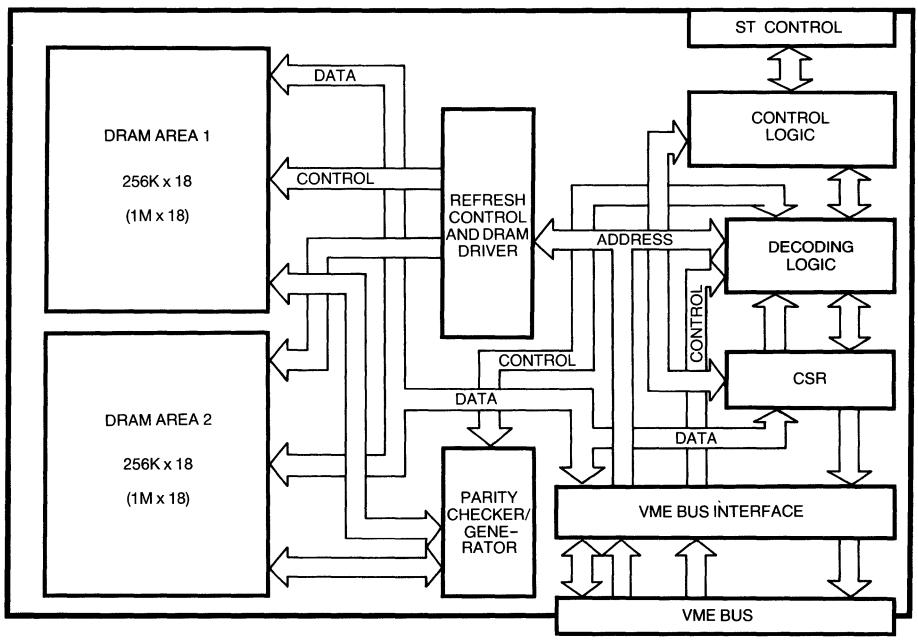


General Description
This board provides additional global RAM capacity in a VMEbus based microcomputer system. The module is available with 64 Kbit devices for a total capacity of 512 Kbyte with byte parity. The memory map of the SYS68K/DRAM-1 is organized in two areas of 256 Kbyte each with two banks of 128 Kbyte. The base address of each area is jumper selectable in 256 Kbyte increments.

Memory
The four memory banks consist of 72 dynamic RAM's with an access time of 150 ns. For maximum reliability and safety, a byte parity check is provided for each byte or word transfer.
The base address of both areas may be jumper selected. Each address modifier signal of the VMEbus can be enabled or disabled for the base address decoding via a special jumper selection. Access to memory for a read or write operation can either be obtained in single byte mode, determined the upper or lower data strobe signal, or in double byte (word) mode if both data strobes are active.
The access time of an ordinary write is 200 ns and for a read 310 ns. The maximum transfer speed to/from the SYS68K/DRAM-1 board is 4 Mbyte/s.
Refresh circuitry is provided on the board. A complete refresh is performed every 2 milliseconds. Every access to the board is delayed by pending refresh for 110 ns. This feature allows the board's use in high speed real time applications because the maximum access time is 460 ns when refresh is in progress.

Control
The SYS68K/DRAM-1 has two switches and three LED's on the front panel for control and maintenance proposes. Switch S1 sets the board in RUN or LOCAL mode. In the RUN mode normal accesses from the bus may be performed. In the LOCAL mode no read or write transfer can occur to the DRAM areas. The RUN/LOCAL mode is indicated by LED3 on the front panel and a flag bit is set in the Control/Status Register (CSR).
LED2 turns on upon a parity error indicating that an error has occurred. LED2 can only be reset by a system reset or a write to the CSR. A parity error can be forced by a write to the CSR to test the different error exception features of the board. The parity error may be used to generate either a Bus Error, SYSFAIL or an interrupt on one of the levels 4-7 (free selectable).
In the interrupt exception mode an auto interrupt vector number can be jumper selected and the master CPU can handle the error with a special recovery routine. This feature allows the master CPU to check the memory byte under test by performing a write/read cycle. If this test is success-

BLOCK DIAGRAM OF THE SYS68K/DRAM-1/2



ful, the previous error is assumed to be a soft error. If a multiple error occurs, it is considered to be a hardware error. For maintenance and error correction the CSR includes a special software selectable mode in which the parity check can be disabled.
The CSR includes, in addition, a special control mode for read/write protection. Therefore, each area may be set separately by software into a read only mode like double bank write and one bank read may be used for saving important data (memory duplication). The front panel switch selects either the default jumpered hardware condition or the software programmable mode using the CSR. The base address of the CSR is free jumper selectable in 256 byte steps.

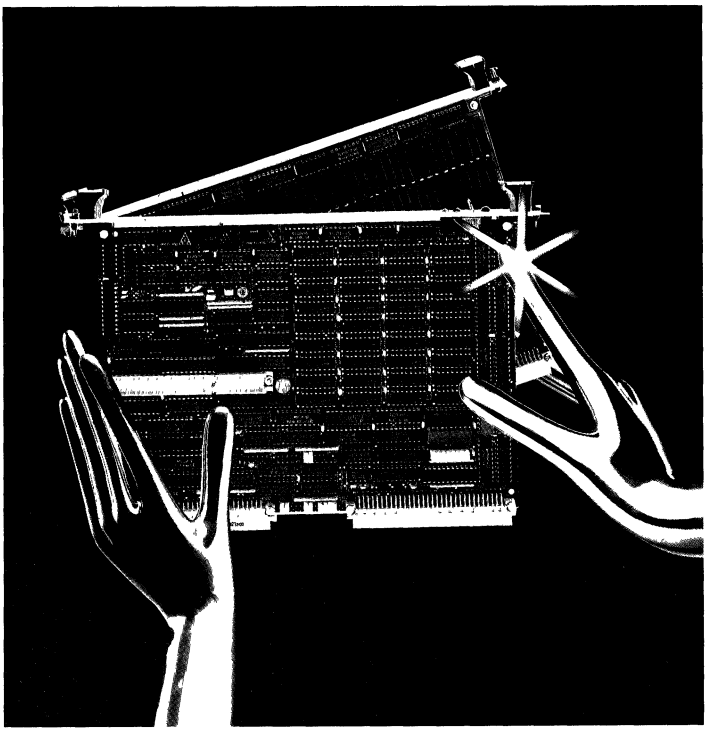
General Description SYS68K/DRAM-2
The SYS68K/DRAM-2 contains the same features as the SYS68K/DRAM-1, like control and status register and byte parity. Memory capacity is increased to 2 Mbyte, 1 Mbyte for each area. This allows cost reduction using the 256K*1 oriented DRAM's.

Specification

Storage Capacity	512 Kbyte (SYS68K/DRAM-1) 2 Mbyte (SYS68K/DRAM-2)
Word Length	8 Bit with 1 Parity Bit 16 Bit with 2 Parity Bits
Page Boundaries	Free jumper selectable base address (256KB/1MB Pages) Address Modifier decoding
Control	Control and Status Register for Multi Mode Control
Access Times	Write Access 190 ns (min) Write Access 210 ns (max) Read Access 320 ns (min) Read Access 350 ns (max) Write Cycle 355 ns (max) Read Cycle 400 ns (max)
Operating Modes	Write (Word or Byte) Read (Word or Byte) Read-Modify-Write (Word or Byte) Read/Write Protection jumper Selectable or Software Programmable
Power Requirements	+5V/2.0 A (max) Operating Mode +5V/1.8 A (typ)
Operating Temperature	0 to +50 degrees C
Storage Temperature	−50 to +85 degrees C
Relative Humidity	0-95% (non-condensing)
Front Panel	6 HE/4 TE
Board Dimensions	Double Eurocard 234 x 160 mm (9.2 x 6.3 inch)

Ordering Information

SYS68K/DRAM-1 Part No. 200000	512 Kbyte dynamic RAM Board with Byte Parity incl. User's Manual
SYS68K/DRAM-2 Part No. 200001	2 Mbyte dynamic RAM Board with Byte Parity incl. User's Manual
SYS68K/DRAM-1/2-UM Part No. 800004	User's Manual for DRAM-1/2

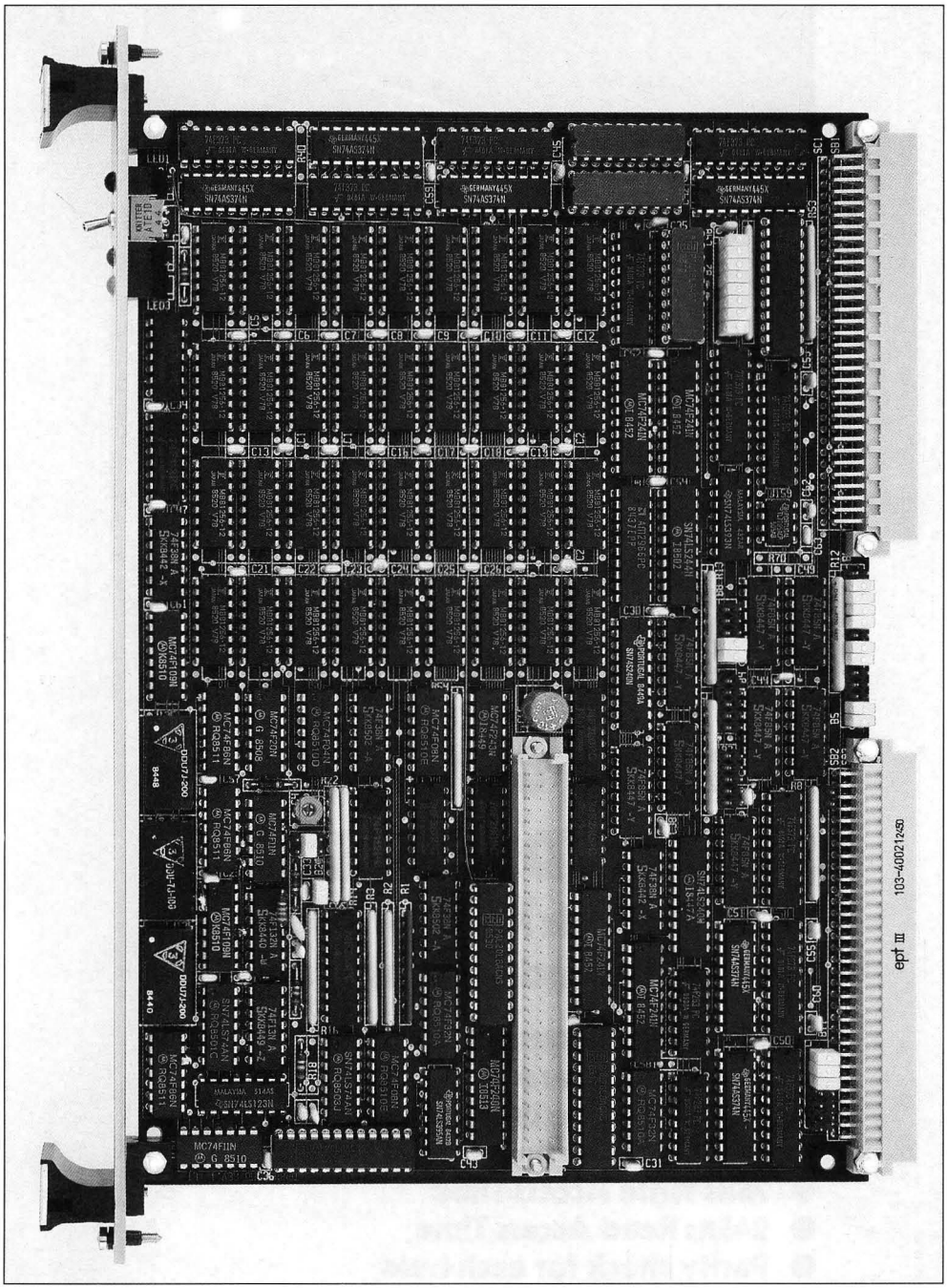


System 68000 VME

SYS68K/DRAM-E3M/S

32 Bit Dynamic Memory Board with Byte Parity and FME Interface

- 32 Address Lines are supported
- 32 Data Lines are supported
- Support of the Unaligned Transfer UAT (IEEE 1014 standard)
- 75ns Write Access Time
- 245ns Read Access Time
- Parity check for each byte



General Description
SYS68K/DRAM-E3M1

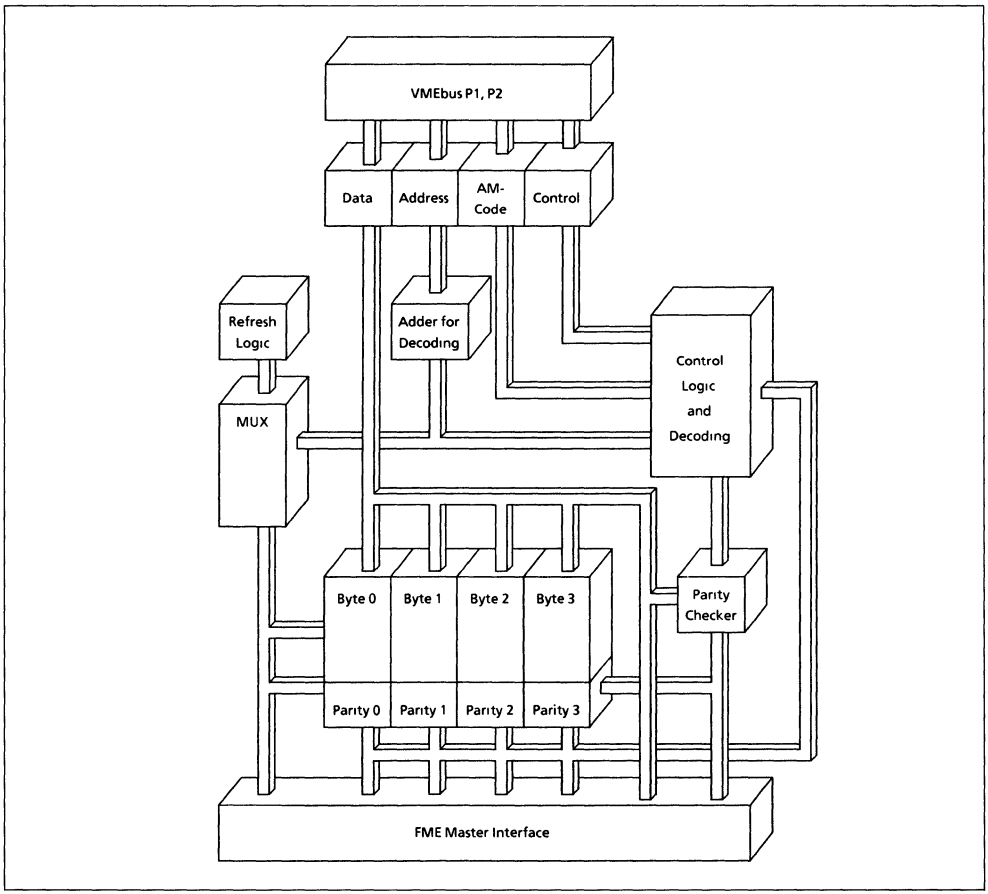
The SYS68K/DRAM-E3M1 board is a high speed dynamic memory board supporting 32 address and data lines, including byte parity check. The address modifier codes are free jumper selectable. The memory capacity of 1 Mbyte can be expanded via FME* slave boards to a maximum capacity of 13 Mbyte.
The block diagram of the DRAM-E3M1 board shows the building blocks in detail.

SYS68K/DRAM-E3M1 Features

- 1 Mbyte dynamic RAM
- 75ns Write Access Time
- 245ns Read Access Time
- Parity check for each byte
- 32 Address Lines are supported
- 32 Data Lines are supported
- Support of the Unaligned Transfer UAT (IEEE 1014**)
- Read Modify Write is supported (8, 16, 24 and 32 bit)
- Address Modifier Code and Access Address free jumper selectable
- Refresh Interleave
- FME Interface
- Battery Backup through P2
- RUN/LOCAL function switch
- RUN/LOCAL/ACCESS and ERROR indication LEDs

FME* Force Memory Expansion
IEEE 1014** Bus standard (VMEbus) of the IEEE Computer Society TC

BLOCK DIAGRAM OF THE SYS68K/DRAM-E3M1



Functional Description
All of the technical features of the DRAM-E3M1 board are briefly described in the following paragraphs:

1. Memory Capacity and Organization
The DRAM-E3M1 board consists of 36 dynamic RAM chips with an internal organization of 256K by 1 bit. 32 chips are used for data storage and 4 chips contain the parity information.
The total capacity of the DRAM-E3M1 board is 1 Mbyte.
The selected address modifier code (A32 or A24) defines the decoding range of the memory. Automatic adjustment to the VMEbus transfer type (8, 16, 24 or 32 bit) is provided.
The IEEE 1014 unaligned transfers (Read, Write and Read-Modify-Write) for the 68020 are supported.

Data Transfer Types Read/Write and Read-Modify-Write	D24-D31	D16-D23	D8-D15	D0-D7
Single Byte Even			x	
Single Byte Odd				x
Double Byte			x	x
Quad Byte	x	x	x	x
Unaligned Transfer	x	x x x	x x x	x

2. The Parity Check
A byte parity check is installed on the board to provide error checking. The parity check can be enabled or disabled via jumper settings. The timing to the RAM chips is identical in both modes, but the access time for a Read cycle is 30ns faster if the parity check is disabled.
If a parity error occurs, the red FAIL LED on the front panel turns on, and a BERR is forced to the VMEbus. The latched ERROR status can be reset via a switch on the front panel.

3. Access Times
The DRAM-E3M1 contains address and data latches to provide maximum throughput to the VMEbus.
If an access is performed on the DRAM-E3M1 board, the yellow SELECT LED on the front panel turns on.

Access Times	Typ	max
WRITE	65ns	75ns
READ with Parity Check READ without Parity Check	260ns 230ns	275ns 245ns
Overhead time for Refresh	120ns	450ns

4. The Refresh
The refresh for the dynamic RAMs is distributed over 4ms and provision is made to minimize the overhead and delay to the VMEbus accesses.
After the internal read cycle of the DRAMs is finished and the data on a read cycle has been stored in the output data latches, a pending refresh request (every 15us) is executed independent from all VMEbus activities. Therefore the overhead time for the VMEbus protocol is used to refresh the RAMs. In addition to the refresh interleave, a refresh to the DRAMs is forced if no on-board access is detected between 11 and 15us after the execution of the last refresh.
The refresh control logic for the FME slave modules (memory expansion) is included on the DRAM-E3M1 board.

5. Battery Backup
All of the DRAMs and the control logic can be powered through the P2 connector. The typical power consumption of the DRAM-E3M1 board in the battery backup mode is 1.0A if refresh is not active, and 2.4A if a refresh cycle is executed (peak current). Due to the limitation of the power consumption of 1.2A per DIN connector pin, 3 pins on the P2 connector are used to provide the battery backup. For special purposes the P1 STDBY line can be used to power the board.

6. The Address Selection
Easy address and address modifier code selection is provided through jumper fields. The access address is jumper selectable in 256 Kbyte increments over the whole range of 16 Mbyte or 4 Gbyte. The start and end address selection is not memory capacity dependent including FME memory expansion.
Twelve different address modifier codes are jumper selectable. Each of the AM-codes can be enabled seperately via jumper settings.
24 and/or 32 address lines are supported on the DRAM-E3M1 to provide maximum flexibility for 16 and 32 bit microprocessors.

Usable Address Modifier Codes:

No	HEX Code	Address Modifier	Function
1	3E	HHHHHL	Standard Supervisory Program Access
2	3D	HHHHLH	Standard Supervisory Data Access
3	3A	HHHLHL	Standard Non-priviledged Program Access
4	39	HHHLLH	Standard Non-priviledged Data Access
5	0E	LLHHHL	Extended Supervisory Program Access
6	0D	LLHHLH	Extended Supervisory Data Access
7	0A	LLHLHL	Extended Non-priviledged Program Access
8	09	LLHLLH	Extended Non-priviledged Data Access
9	XX	XXXXXX	Respond Always
10	1E	LHHHHL	User defined
11	10	LHHHLH	User defined
12	19	LHHLLH	User defined

7. RUN/LOCAL Switch

A RUN/LOCAL switch can be used to isolate the DRAM-E3M1 from the VMEbus during maintenance or for test purposes. The state is shown on two LEDs available on the front panel.

8. The FME

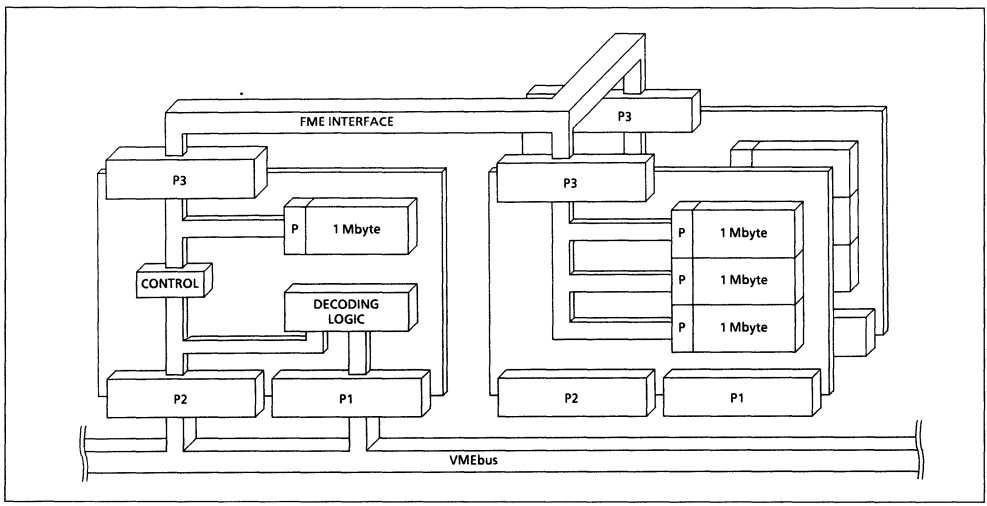
The SYS68K/DRAM-E3M1 supports the FME (FORCE Memory Expansion) to provide cost effective memory expansion through FME slave boards. The FME master interface on the DRAM-E3M1 supports a maximum of 2 FME slave boards which can be connected directly to the DRAM-E3M1 via a 96 pin DIN connector (P3). No time overhead is incurred through the FME expansion slave modules. The access times listed in paragraph 3 are valid for the onboard RAM as well as for the FME slave modules.

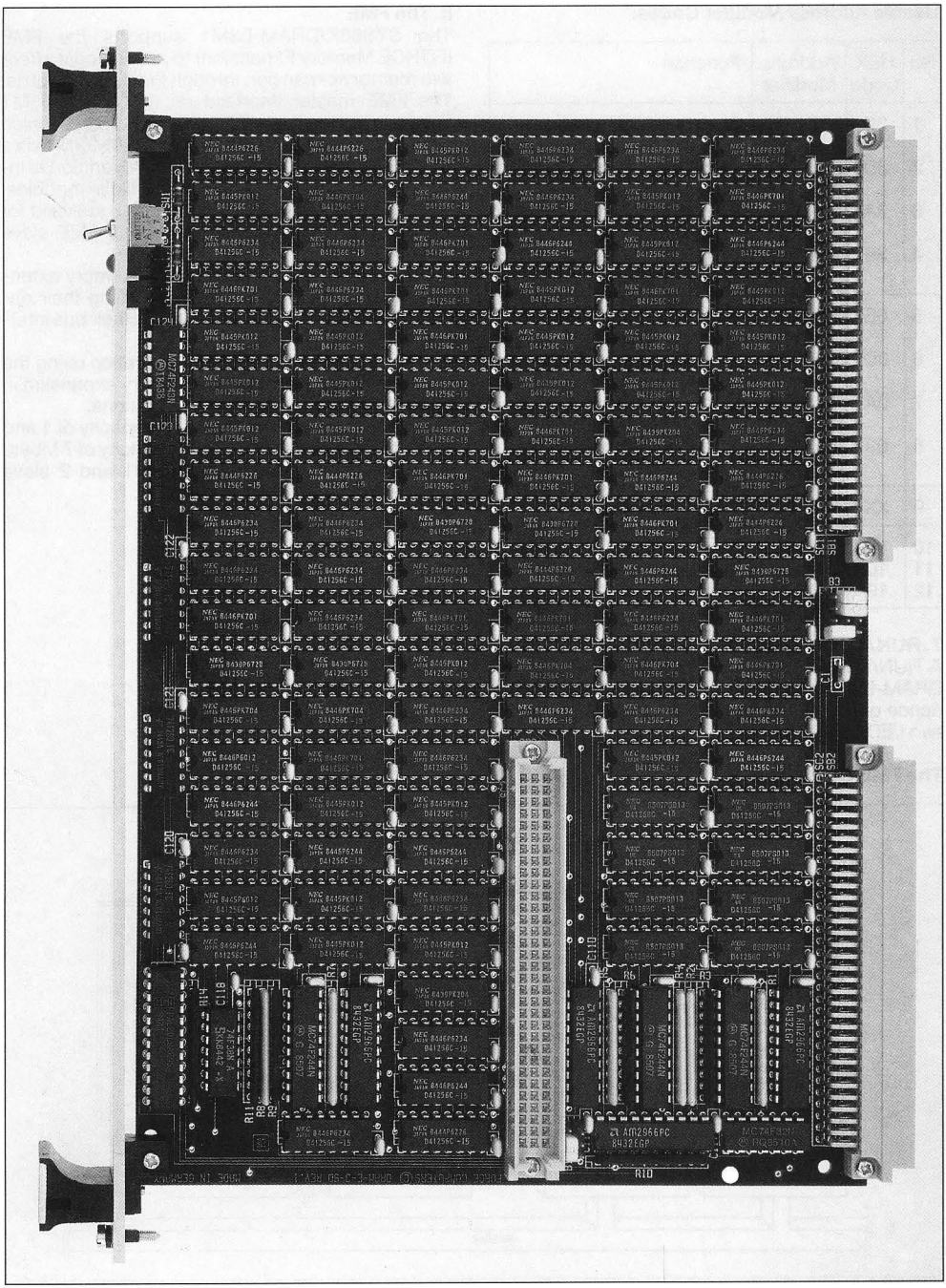
The FME concept allows the local memory extention of RAM and CPU boards by using their onboard DRAM control logic as well as their bus interfaces.

The FME allows easy system integration using the VMEbus and/or VMXbus for memory expansion in high performance system configurations.

Slave boards are available with a capacity of 1 and 3 Mbyte. Therefore a maximum capacity of 7 Mbyte is provided using the DRAM-E3M1 and 2 slave boards, both with 3 Mbyte capacity.

The FME Concept





General Description
SYS68K/DRAM-E3SX

The SYS68K/DRAM-E3SX boards are high speed dynamic memory boards based on the FME. Each of the slave boards contains 32-bit data and 4 parity bits as well as the complete decoding logic for the FME. Two different memory boards with a capacity of 1 and 3 Mbyte are available.

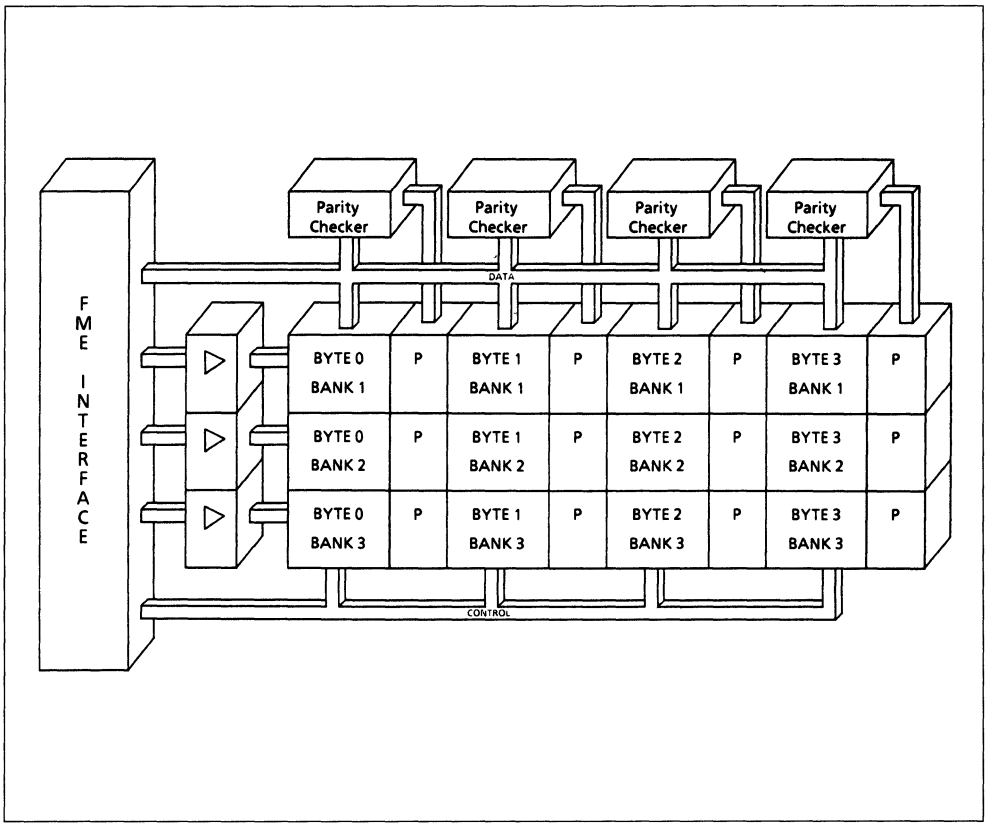
SYS68K/DRAM-E3SX Features

- FME Slave board
- 32 data lines are supported
- 4 parity bits
- 4 strobes control every byte seperately
- Read Modify Write is supported
- Parity Error LED
- Access LED
- Refresh Interleave Support
- DRAM-E3S1 : 1 Mbyte RAM
  DRAM-E3S3 : 3 Mbyte RAM

Functional Description

The FME boards DRAM-E3S1/3 are designed to interface any FME master board as a memory expansion. FME master board (DRAM-E3M1) controls the access as well as the refresh function of the DRAMs on the slave boards. The FME master board has to achieve timing and control to the slave modules for optimized throughput.
All the memory range decoding and bank selection is made on the master board to allow the use of every slave board in 8, 16 or 32 bit environments. Each of the DRAM-E3SX boards uses 256Kx1 oriented DRAMs with an access time of 120ns. The DRAM-E3S1 and E3S3 boards use Dual Inline packages.
To avoid power consumption peaks, the DRAM-E3SX boards can refresh the memory cells for each memory bank seperately. The FME master board controls this function.

BLOCK DIAGRAM OF THE SYS68K/DRAM-E3S3

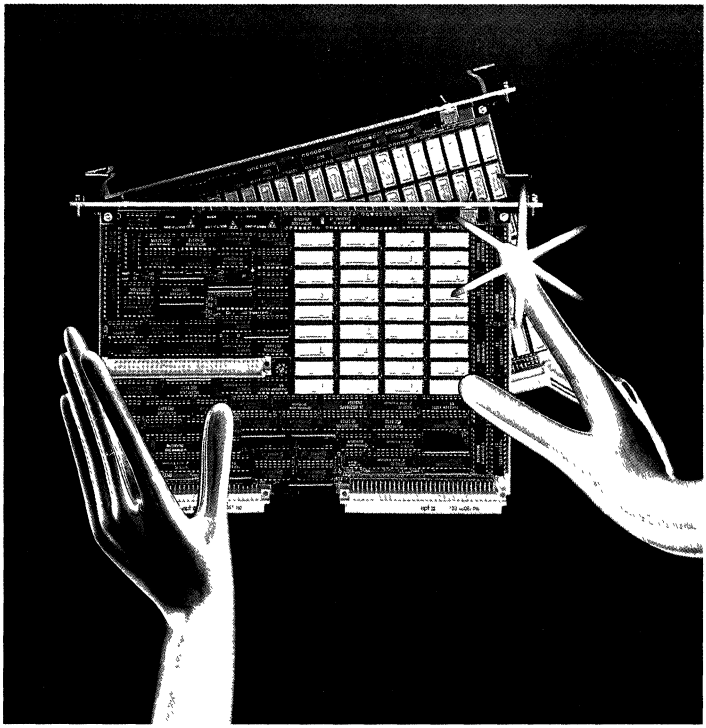


Specification SYS68K/DRAM-E3M/S

	E3M1	E3S1	E3S3
Memory Capacity	1 Mbyte	1 Mbyte	3 Mbyte
Organization	32+4 Bit	32+4 Bit	32+4 Bit
Data Transfer Mode any of 4 bytes	Yes	Yes	Yes
Used DRAM Organization	256Kx1	256Kx1	256Kx1
DRAM Chips	36pcs	36pcs	108pcs
RAS DRAM Access Time	120ns	120ns	120ns
Interface	FME (master) VMEbus	FME (slave)	FME (slave)
Access Times Write	65	65	65
With Parity Check Read	260	260	260
Without Parity Check Read	210	210	210
Power Requirements			
+5V (Refresh Peak)	5.9A	2.8A	3.5A
+5V (Average Max)	4.3A	2.1A	2.9A
+5V (Average Typ)	3.2A	1.4A	1.5A
+5V BATTERY	0.9-2.1A	0.4-2.1A	0.8-2.9A
Operating Temperature (degrees C)	0 to +60	0 to +60	0 to +60
Storage Temperature (degrees C)	−55 to +85	−55 to +85	−55 to +85
Relative Humidity (non-condensing)	0−95%	0−95%	0−95%
Double Eurocard 233x160mm (9.2x6.3")	Yes	Yes	Yes

Ordering Information

SYS68K/DRAM-E3M1 Part No1. 200004	1 Mbyte DRAM card for 32 bit including the FME master interface and E3M1/HUM.
SYS68K/DRAM-E3S1 Part No. 200101	1 Mbyte DRAM card for memory expansion. HUM included.
SYS68K/DRAM-E3S3 Part No. 200103	3 Mbyte DRAM card for memory expansion. HUM included.
SYS68K/DRAM-E3M/E3S/HUM Part No. 800043	Hardware User's Manual for the SYS68K/DRAM-E3 boards

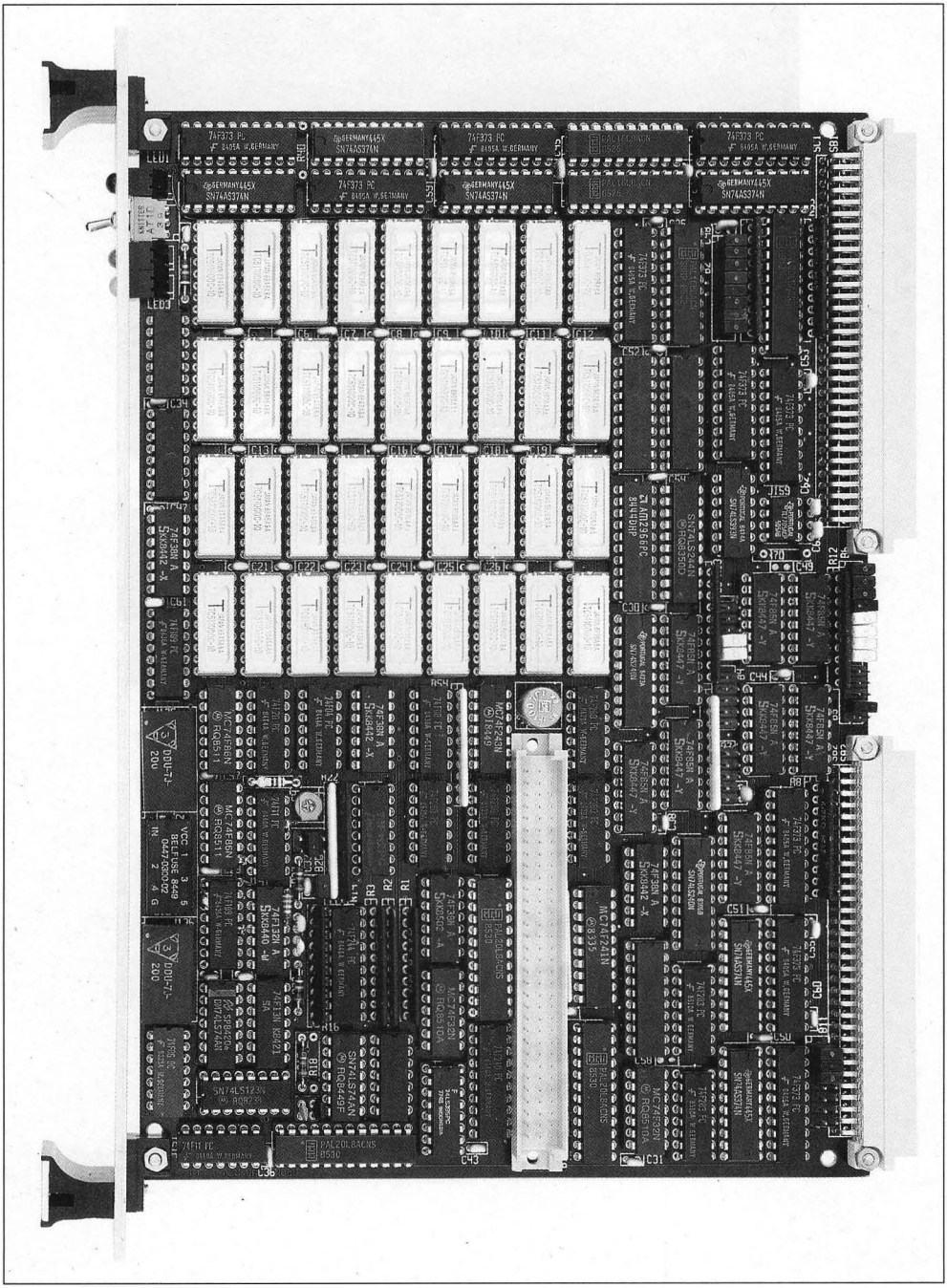


System 68000 VME

SYS68K/DRAM-E4M/S

32 Bit Dynamic Memory Board with Byte Parity and FME Interface

- 32 Address and Data Lines are supported
- Support of the Unaligned Transfer UAT
- 75 ns Write Access Time
- 225 ns Read Access Time



General Description
SYS68K/DRAM-E4M4

The SYS68K/DRAM-E4M4 board is a high speed dynamic memory board supporting 32 address and data lines, including byte parity check. The address modifier codes are free jumper selectable.

The memory capacity of 4 Mbyte can be expanded via FME* slave boards to a maximum capacity of 28 Mbyte.

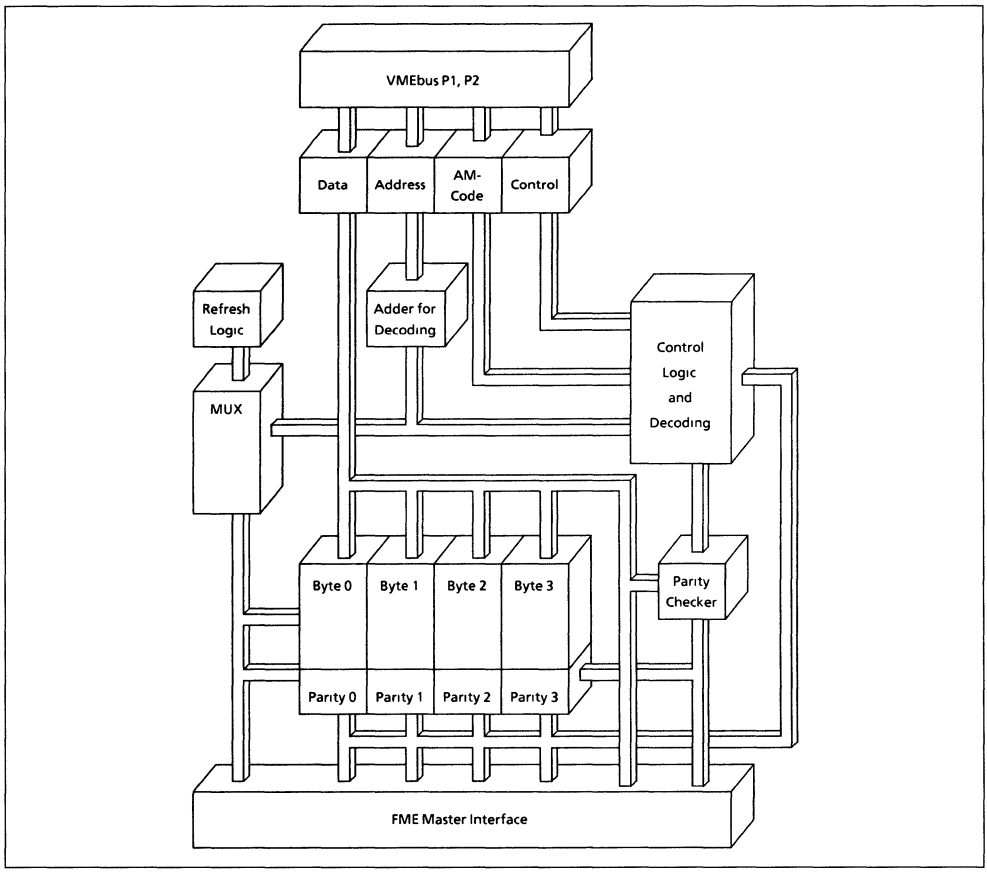
The block diagram of the DRAM-E4M4 board shows the building blocks in detail.

SYS68K/DRAM-E4M4 Features

- 4 Mbyte dynamic RAM
- 75ns Write access time
- 225ns Read access time
- Parity check for each byte
- 32 address lines are supported
- 32 data lines are supported
- Support of the Unaligned Transfers UAT (IEEE 1014**)
- Read-Modify-Write is supported (8, 16, 24 and 32 bit)
- Address Modifier code and access address free jumper selectable
- Refresh interleave
- FME interface
- Battery backup through P2
- RUN/LOCAL function switch
- RUN/LOCAL/ACCESS and ERROR indication LEDs

FME* Force Memory Expansion
IEEE 1014** Bus standard (VMEbus) of the IEEE Computer Society TC.

BLOCK DIAGRAM OF THE SYS68K/DRAM-E4M4



Functional Description
All of the technical features of the DRAM-E4M4 board are briefly described in the following paragraphs:

1.1 Memory Capacity and Organization
The DRAM-E4M4 board consists of 36 dynamic RAM chips with an internal organization of 1 M x 1 bit. 32 chips are used for data storage and 4 chips contain the parity information.
The total capacity of the DRAM-E4M4 board is 4 Mbyte.
The selected address modifier code (A32 or A24) defines the decoding range of the memory. Automatic adjustment to the VMEbus transfer type (8, 16, 24 or 32 bit) is provided.
The IEEE 1014 Unaligned Transfers (Read, Write and Read-Modify-Write) for the 68020 are supported.

Data transfer types Read/Write and Read-Modify-Write	D24-31	D16-23	D8-D15	D0-D7
Single byte even			x	
Single byte odd				x
Double byte			x	x
Quad byte	x	x	x	x
Unaligned Transfer	x	x x x	x x x	x

1.2 The Parity Check
A byte parity check is installed on the board to provide error checking. The parity check can be enabled or disabled via jumper settings. The timing to the RAM chips is identical in both modes, but the access time for a read cycle is 30ns faster if the parity check is disabled.
If a parity error occurs, the red FAIL LED on the front panel turns on, and a BERR is forced to the VMEbus. The latched ERROR status can be reset via a switch on the front panel.

1.3 Access Times
The DRAM-E4M4 contains address and data latches to provide maximum throughput to the VMEbus.
If an access is performed on the DRAM-E4M4 board, the yellow SELECT LED on the front panel turns on.

Access Times	Typ	Max
WRITE	65ns	75ns
READ with parity check READ without parity check	225ns 195ns	245ns 215ns
Overhead time for refresh	120ns	450ns

1.4 The Refresh
The refresh for the dynamic RAMs is distributed over 4ms and provision is made to minimize the overhead and delay to the VMEbus accesses.
After the internal read cycle of the DRAMs is finished and the data on a read cycle has been stored in the output data latches, a pending refresh request (every 15us) is executed independent from all VMEbus activities. Therefore the overhead time for the VMEbus protocol is used to refresh the RAMs. In addition to the refresh interleave, a refresh to the DRAMs is forced if no on-board access is detected between 11 and 15us after the execution of the last refresh.
The refresh control logic for the FME slave modules (memory expansion) is included on the DRAM-E4M4 board.

1.5 Battery Backup
All of the DRAMs and the control logic can be powered through the P2 connector. The typical power consumption of the DRAM-E4M4 board in the battery backup mode is 1.0A if refresh is not active, and 2.4A if a refresh cycle is executed (peak current). Due to the limitation of the power consumption of 1.2A per DIN connector pin, 3 pins on the P2 connector are used to provide the battery backup. For special purposes the P1 STDBY line can be used to power the board.

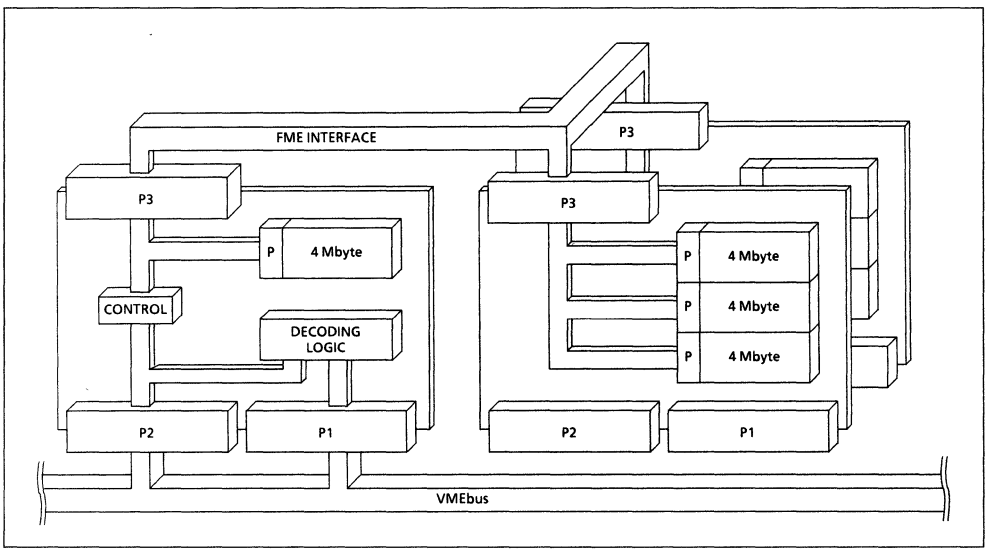
1.6 The Address Selection
Easy address and Address Modifier code selection is provided through jumper fields. The access address is jumper selectable in 256 Kbyte increments over the whole range of 16 Mbyte or 4 Gbyte. The start and end address selection is not memory capacity dependent including FME memory expansion.
Twelve different Address Modifier codes are jumper selectable. Each of the AM-codes can be enabled separately via jumper setting.

Usable Address Modifier Codes:

No	HEX Code	Address Modifier	Function
1	3E	HHHHHL	Standard supervisory program access
2	3D	HHHHLH	Standard supervisory data access
3	3A	HHHLHL	Standard non-privileged program access
4	39	HHHLLH	Standard non-privileged data access
5	0E	LLHHHL	Extended supervisory program access
6	0D	LLHHLH	Extended supervisory data access
7	0A	LLHLHL	Extended non-privileged program access
8	09	LLHLLH	Extended non-privileged data access
9	XX	XXXXXX	Respond Always
10	1E	LHHHHL	User defined
11	10	LHHHLH	User defined
12	19	LHHLLH	User defined

24 and/or 32 address lines are supported on the DRAM-E4M4 to provide maximum flexibility for 16 and 32 bit microprocessors.

The FME Concept



1.7 RUN/LOCAL Switch

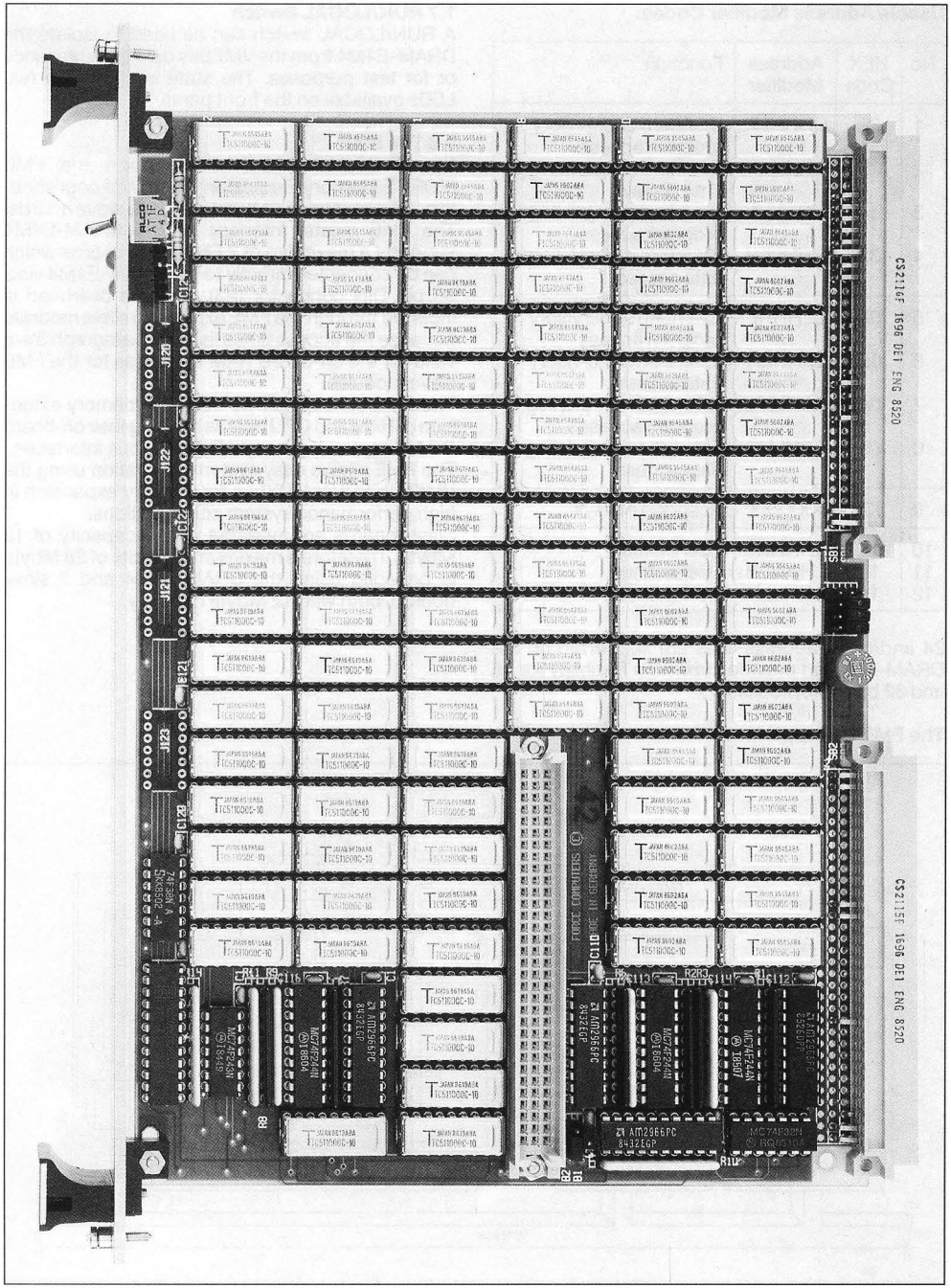
A RUN/LOCAL switch can be used to isolate the DRAM-E4M4 from the VMEbus during maintenance or for test purposes. The state is shown on two LEDs available on the front panel.

1.8 The FME

The SYS68K/DRAM-E4M4 supports the FME (FORCE Memory Expansion) to provide cost effective memory expansion through FME slave boards. The FME master interface on the DRAM-E4M4 supports a maximum of 2 FME slave boards which can be connected directly to the DRAM-E4M4 via a 96 pin DIN connector (P3). No time overhead is incurred through the FME expansion slave modules because the access times listed in paragraph 3 are valid for the on-board RAM as well as for the FME slave modules.

The FME concept allows the local memory extension of RAM and CPU boards by using their on-board DRAM control logic as well as their bus interfaces. The FME allows easy system integration using the VMEbus and/or VMXbus for memory expansion in high performance system configurations.

Slave boards are available with a capacity of 12 Mbyte. Therefore a maximum capacity of 28 Mbyte is provided using the DRAM-E4M4 and 2 slave boards, both with 12 Mbyte capacity.


CS2216F 1696 DE1 ENG 8520
CS2215F 1696 DE1 ENG 8520
FORCE COMPUTERS © 2
MADE IN GERMANY

General Description
SYS68K/DRAM-E4S12

The SYS68K/DRAM-E4S12 board is a high speed dynamic memory board based on the FME. Each slave board contains 32-bit data and 4 parity bits as well as the complete decoding logic for the FME. A memory board with a capacity of 12 Mbyte is available.

SYS68K/DRAM-E4S12 Features

- FME slave card
- 32 data lines are supported
- 4 parity bits
- 4 strobes control every byte separately
- Read-Modify-Write is supported
- Parity error LED
- Access LED
- Refresh interleave support
- DRAM-E4S12 : 12 Mbyte RAM

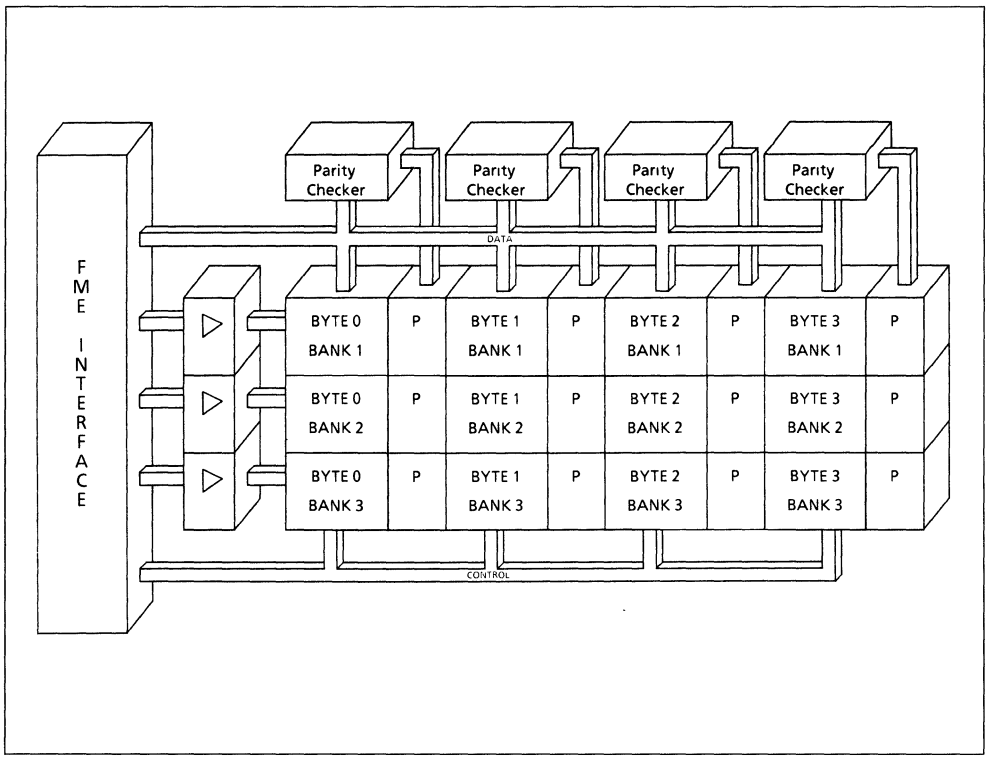
Functional Description

The FME board DRAM-E4S12 is designed to interface any FME master board as a memory expansion. FME master boards (i.e. DRAM-E4M4) control the access as well as the refresh function of the DRAMs on the slave boards. The FME master board has to achieve timing and control to the slave modules for optimized throughput.

All the memory range decoding and bank selection is made on the master board to allow every slave board to be used in 8, 16 or 32 bit environments. The DRAM-E4S12 board uses 1Mx1 oriented DRAMs with an access time of 100 ns.

To avoid power consumption peaks, the DRAM-E4S12 board can refresh the memory cells for each memory bank separately. The FME master board controls this function.

BLOCK DIAGRAM OF THE SYS68K/DRAM-E4S12

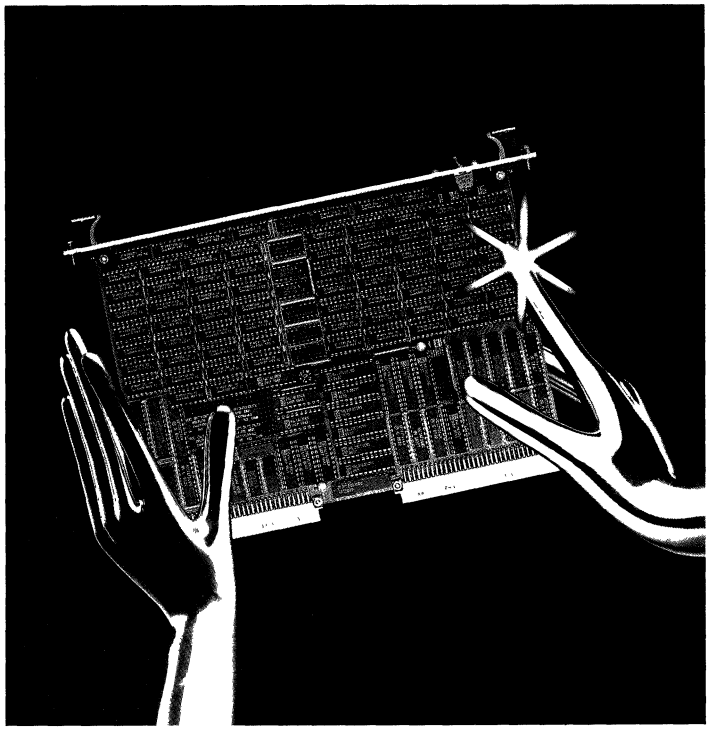


Specification SYS68K/DRAM-E4M/S

	E4M4	E4S12
Memory Capacity	4 Mbyte	12 Mbyte
Organization	32+4 bit	32+4 bit
Data Transfer Mode	Yes	Yes
any of 4 byte		
Used DRAM Organization	1 M x 1	1 M x 1
DRAM Chips	36pcs	108pcs
RAS DRAM Access Time	100 ns	100 ns
Interface	FME (master) VMEbus	FME (slave)
Access Times Write	65	65
With Parity Check Read	225	225
Without Parity Check Read	195	195
Power Requirements:		
+5V (Refresh Peak)	5.9A	5.0A
+5V (Average Max)	4.3A	4.8A
+5V (Average Typ)	3.2A	4.6A
+5V BATTERY	2.4A	
Operating Temperature (degrees C)	0 to +60	0 to +60
Storage Temperature (degrees C)	−55 to +85	−55 to +85
Relative Humidity (non-condensing)	0 – 95%	0 – 95%
Double Eurocard 233 x 160mm (9.2 x 6.3")	Yes	Yes

Ordering Information

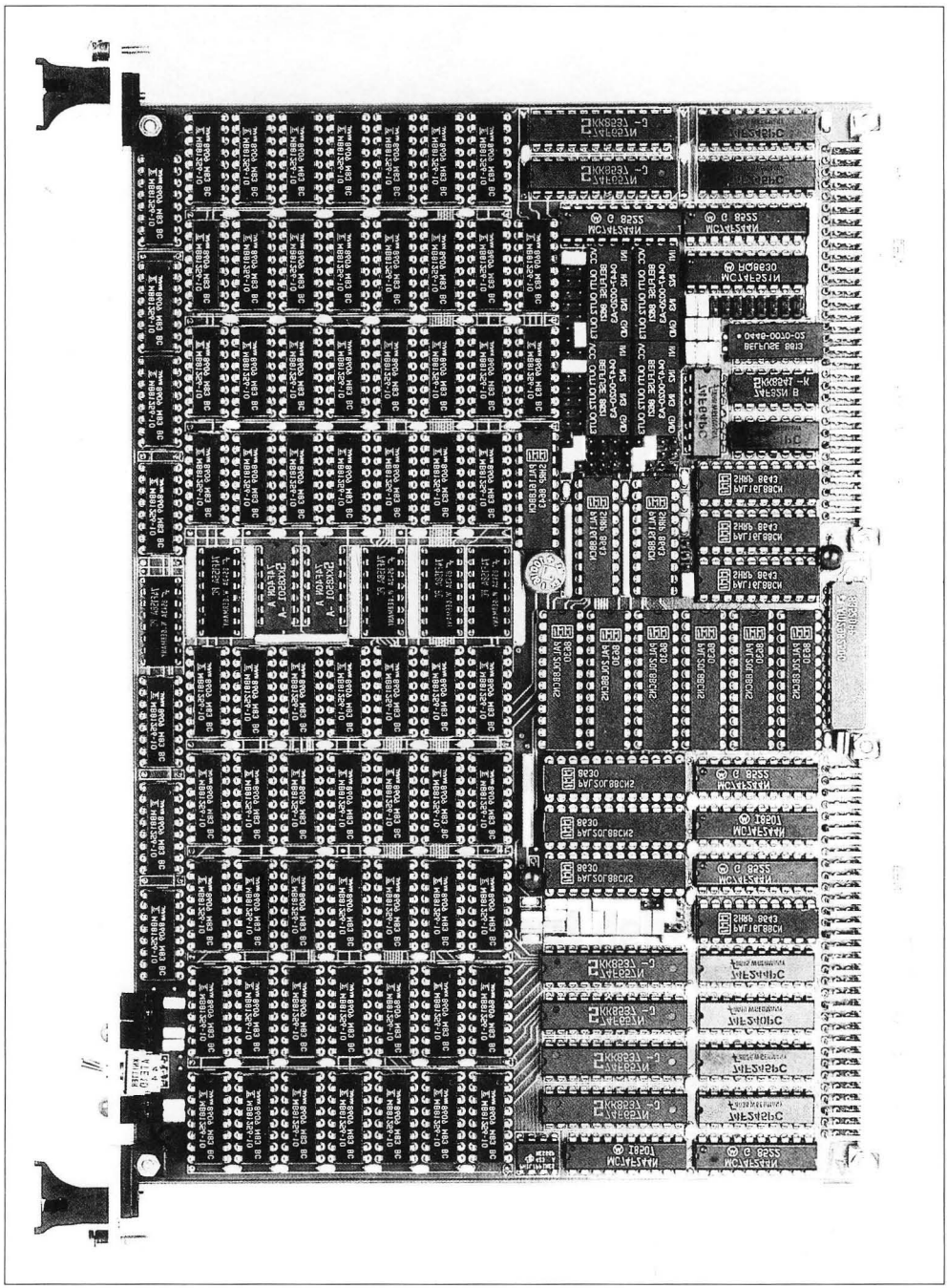
SYS68K/DRAM-E4M4 Part No. 200110	4M byte DRAM card for 16 and 32 bit environments. FME master interface and user's manual included.
SYS68K/DRAM-E4S12 Part No. 200113	12M byte DRAM card for FME memory expansion. User's manual included.
SYS68K/DRAM-E4M/E4S/UM Part No. 800105	User's manual for the SYS68K/DRAM-E4 board series.



System 68000 VME SYS68K/DRAM-6

32 Bit High Speed Dynamic RAM Board

- 2 Mbyte Memory Capacity
- 95/200 ns Access Time
- IEEE 1014 VMEbus Interface



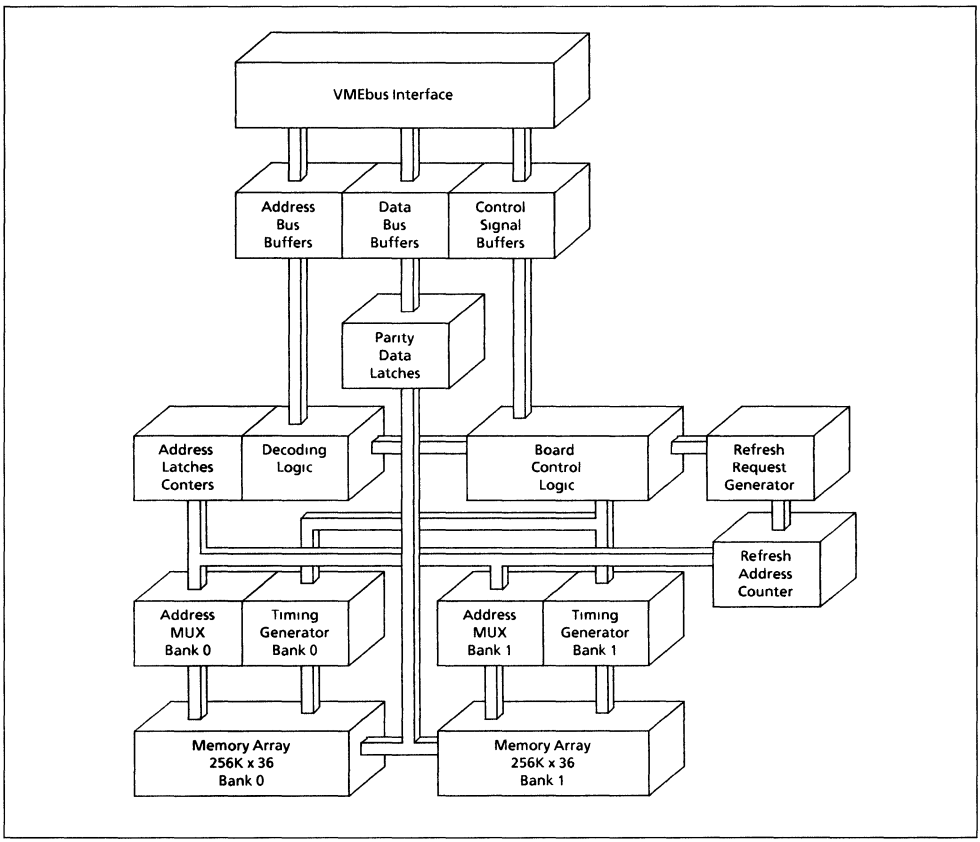
General Description SYS68K/DRAM-6

The SYS68K/DRAM-6 board is an ultra high speed memory board using dynamic RAMs. It provides 2 Mbyte of RAM including byte parity generation/check, supporting all 32 address and 32 data lines as defined in the IEEE 1014 Standard (VMEbus Rev. C).
Maximum data throughput on the VMEbus is provided by the on-board logic which allows read access times of 200 ns and write access times of 95 ns.
The early write operation provides a 95 ns write operation by latching all data internally and executing the write operation to the DRAMs fully asynchronous to the VMEbus activities.
Easy installation is provided because the access address of the DRAM-6 board is jumper selectable in 1 Mbyte increments and each of the defined address modifier codes is jumper selectable.

Features of the SYS68K/DRAM-6

- 2 Mbyte dynamic RAM on DRAM-6
  Access Times: Read: 200 ns (typ.)
  Write: 95 ns (typ.)
- 32 Address and Data Signals supported
- Byte Parity Generation/Check
- Interleaved Refresh every 15 us
- VMEbus Interface:
  A32: D32, D16, D8, D(0), UAT, RMW
  A24: D32, D16, D8, D(0), UAT, RMW
- RUN/LOCAL Switch
- Access Indicator
- FAIL Indicator

BLOCK DIAGRAM OF THE SYS68K/DRAM-6



Functional Description
All of the technical features of the DRAM-6 board are briefly described in the following paragraphs:

1. Memory Capacity and Organization
The DRAM-6 board consists of 72 dynamic RAM chips with an internal organization of 256 K x 1 bit. 64 chips are used for data storage and 8 devices contain the parity information.
The total capacity of the DRAM-6 board is 2 Mbyte.
The selected address modifier code (A32 or A24) defines the decoding range of the memory. Automatic adjustment to the VMEbus transfer type (8,16,24 or 32 bit) is provided.
The IEEE 1014 unaligned transfers (Read, Write and Read Modify Write) for the 68020 are supported.

Data Transfer Types Read/Write and Read Modify Write	D24-31	D16-23	D8-D15	D0-D7
Single Byte Even			x	
Single Byte Odd				x
Double Byte (Word)			x	x
Quad Byte (Long Word)	x	x	x	x
Unaligned Transfer	x	x	x	
		x	x	x
		x	x	

2. The Parity Check
A byte parity check is installed on the board to provide error checking.
If a parity error occurs, the red FAIL LED on the front panel turns on, and a BERR is forced to the VMEbus. The latched ERROR status can be reset via a system reset.

3. Access Times
The DRAM-6 contains address and data latches to provide maximum throughput to the VMEbus.

Access Times	Typ	Max
WRITE	95 ns	105 ns
READ	200 ns	215 ns
Overhead Time for Refresh		270 ns

If an access is performed on the DRAM-6 board, the yellow SELECT LED on the front panel turns on.

4. The Refresh
The refresh for the dynamic RAMs is distributed over 4 ms and provision is made to minimize the overhead and delay to the VMEbus accesses.
After the internal read cycle of the DRAMs is finished and the data on a read cycle has been stored in the output data latches, a pending refresh request (every 15 us) is executed independent from all VMEbus activities. Therefore the overhead time for the VMEbus protocol is used to refresh the RAMs. In addition to the refresh interleave, a refresh to the DRAMs is forced if a not on-board access is detected between 11 and 15 us after the execution of the last refresh.

5. The Address Selection
Easy address and address modifier code selection is provided through jumper fields. The access address is jumper selectable in 1 Mbyte increments over the whole range of 16 Mbyte or 4 Gbyte.
All defined address modifier codes are jumper selectable. Each of the AM-codes can be enabled separately via jumper setting.
24 and/or 32 address lines are supported on the DRAM-6 to provide maximum flexibility for 16 and 32 bit microprocessors.

Usable Address Modifier Codes:

No	HEX Code	Address Modifier	Function
1	3E	HHHHHL	Standard Supervisory Program Access
2	3D	HHHHLH	Standard Supervisory Data Access
3	3A	HHHLHL	Standard Non-privileged Program Access
4	39	HHHLLH	Standard Non-privileged Data Access
5	0E	LLHHHL	Extended Supervisory Program Access
6	0D	LLHHLH	Extended Supervisory Data Access
7	0A	LLHLHL	Extended Non-privileged Program Access
8	09	LLHLLH	Extended Non-privileged Data Access
9	XX	XXXXXX	Respond Always
10	1E	LHHHHL	User defined
11	10	LHHHLH	User defined
12	19	LHHLLH	User defined

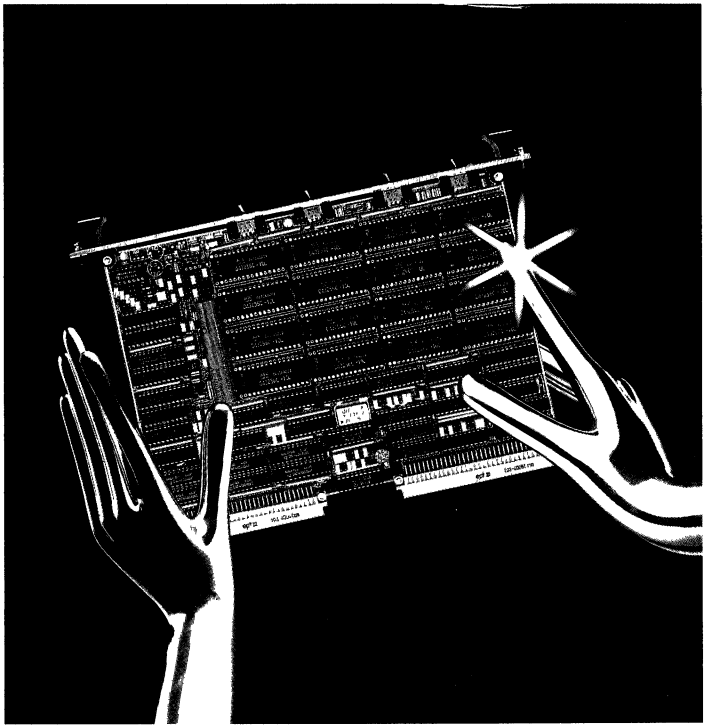
7. RUN/LOCAL Switch
A RUN/LOCAL switch can be used to isolate the DRAM-6 board from the VMEbus during maintenance or for test purposes. The state is shown on two LEDs available on the front panel.

Specifications of the SYS68K/DRAM-6

	DRAM-6
Memory Capacity	2 Mbyte
Organization	64 + 8 Bit
Used DRAM Organization	256 K x 1
DRAM Chips	72 pcs
RAS DRAM Access Time	100 ns
IEEE 1014 (VMEbus Rev.C) Interface	Yes
A32: D32, D16, D8, D(0), UAT, RMW	Yes
A24: D32, D16, D8, D(0), UAT, RMW	Yes
Access Times: Read Access Time Write Access Time	Typ Max 200 ns 215 ns 95 ns 105 ns
Power Requirements:	
+5V (Refresh Peak) +5V (Average Max) +5V (Average Typ)	5.9A 5.3A 4.8A
Operating Temperature (Degrees C)	0 to +60
Storage Temperature (Degrees C)	−55 to +85
Relative Humidity (non-condensing)	0 − 95 %
Double Eurocard 233 x 160 mm (9.2 x 6.3")	Yes

Ordering Information

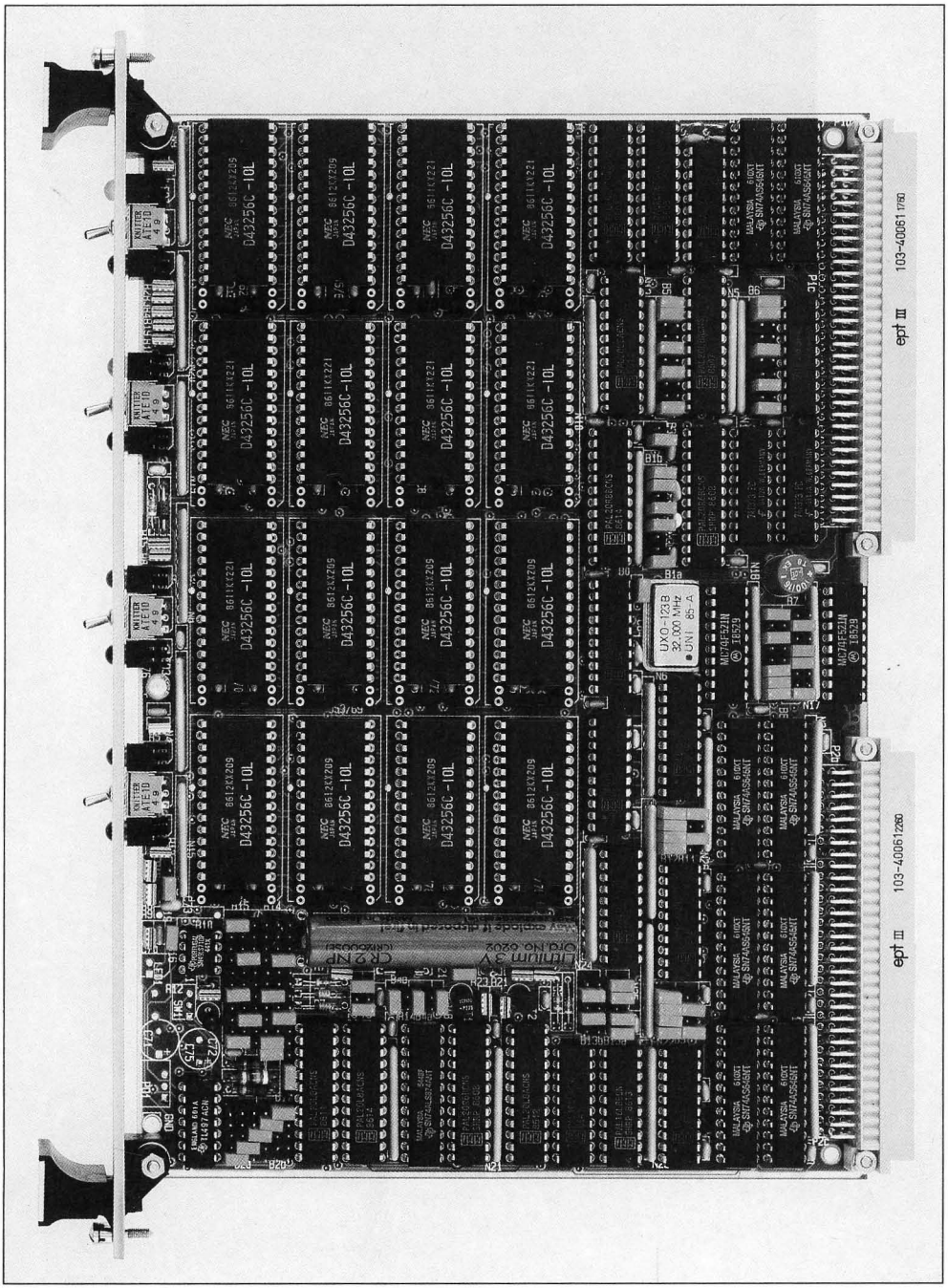
SYS68K/DRAM-6 Part No. 200130	2 Mbyte DRAM card for 32 bit address and data including documentation.
SYS68K/DRAM-6/UM Part No. 800134	Hardware User's Manual for the SYS68K/DRAM-6 board.



System 68000 VME SYS68K/SRAM-3B

32 Bit Static RAM Board with VMEbus and VMXbus Interface

- 1 Mbyte static RAM
- On-board battery backup
- 80/210ns Write/Read access time
- Jumper selectable access address


eptm 103-A00612260
eptm 103-A00612260

General Description

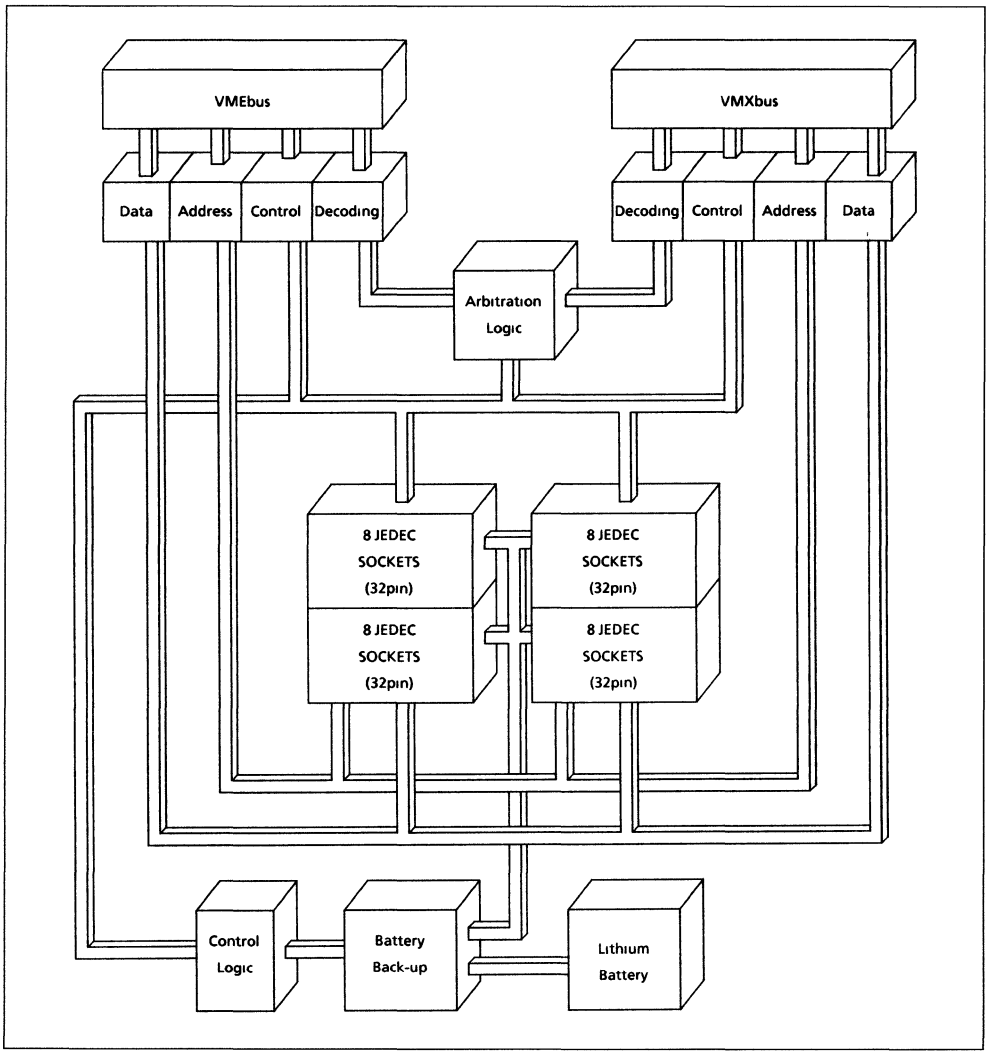
The SYS68K/SRAM-3B board provide full static memory with an on-board battery back-up accessible from the VMEbus as well as from the VMXbus. The 32 bit address and data support in conjunction with the fast static RAMs, offers high data throughput with maximum reliability. Access Address and Address Modifier code of the two memory areas are jumper selectable.

The SRAM-3B provides 1 Mbyte of dual ported high speed static RAM.

The two memory areas, both holding half of the memory capacity can be assigned to respond to VMEbus only, VMXbus only, or VMEbus and VMXbus transfers.

An on-board voltage sensor detects if the main power is out of specification and enables the on-board battery back up for the SRAMs realized with a lithium battery.

BLOCK DIAGRAM OF THE SYS68K/SRAM-3B



Features of the SYS68K/SRAM-3B

- 1024 Kbyte SRAM on SRAM-3B
- VMEbus Interface supporting the following data transfer modes:
  A24: D32, D32NA, D16, D8
  A32: D32, D32NA, D16, D8
  Read-Modify-Write cycles are supported for multi-processor synchronization with the VMXbus.
- VMXbus interface supporting the following data transfer modes:
  A24: D32, D32NA, D16, D8
  Read-Modify-Write cycles are supported for multi-processor synchronization with the VMEbus.
- 2 memory areas which each have separate jumper selectable access addresses and address modifier codes.

Typical Access Times:

	VMEbus	VMXbus
Write	80 ns	70 ns
Read	210 ns	210 ns

- On-board battery back-up provides data retention for up to 1 year.

1.0 Functional Description

The SRAM-3B static RAM board provides 1 Mbyte of dual ported memory.
VMXbus and VMEbus accesses are supported and a fast arbitration logic provides only 35ns overhead when switching from one bus interface to the other.
The fully latched address and data bus provide an interleaved Write operation to minimize bus overhead and support a maximum transfer rate on the VMEbus of 4M transfer/sec which results in a 16 Mbyte/s data throughput using 32 bit of data.
Installation in 16 or 32 bit environments is provided through the address modifier decoding (A24 or A32 mode) which defines the address range to be decoded.
Automatic data bus sizing and adaptation to 16 or 32 bit environments is provided through the on-board hardware logic.
The functional details of the VMEbus and VMXbus interface, the battery back-up and the decoding are described in the following paragraphs.

1.1 The VMEbus Interface

A full IEEE 1014 standard compatible interface which supports the unaligned transfers is installed on the SRAM-3B boards.
32 bit of data and address are supported to take full advantage of 16 and 32 bit processor boards and DMA Controllers.

The following table lists the supported data transfer modes:

Transfer Type	D31–D24	D23–D16	D15–D8	D7–D0
Byte			x	x
Word			x	x
Word (unaligned)		x	x	
3 Byte		x	x	x
(unaligned)	x	x	x	
Long Word	x	x	x	x

The address and data transfer modes supported on the SRAM-3B board is:
A24: D32, D32NA, D16, D8
A32: D32, D32NA, D16, D8
Installation in 16 and 32 bit environments is possible using the address modifier selection. Each of the two fully independent memory areas, each consisting of half of the memory size, contains its own decoding logic, which allows the separation and assignment of different data/program segments.
A RUN/LOCAL switch to enable or disable accesses from the VMEbus is installed on the SRAM-3B board. This switch allows the assignment of the board to the VMXbus or as a dual ported memory if the corresponding switch for the VMXbus interface is set to enable VMXbus transfers. If the corresponding switch is set to disable the VMXbus interface, only VMEbus transfers are allowed.
For multi-processor synchronization, all defined Read-Modify-Write cycles are supported. A VMEbus Read and the following Write transfer cannot be interrupted by a VMXbus data transfer modifying the same memory location.
The maximum data throughput of the SRAM-3B is 16 Mbyte/s without any concurrent VMXbus data transfers.

1.2 The VMXbus Interface

A VMXbus revision B compatible interface supporting 32 bit data transfers is installed on the SRAM-3B. The supported data transfer modes are identical to the listed transfer modes in the VMEbus description.
Data Transfer Modes: D32, D32NA, D16, D8
The 23 address lines of the VMXbus are decoded and the access address for each of the two memory areas are jumper selectable within the A24 address range.
The access address of the VMEbus (A24 mode) and the VMXbus are identical to maintain linear addressing.
In conjunction with the RUN/LOCAL switch of the VMEbus interface, the SRAM-3B can be set into the following modes:

Mode A:	VMEbus access only
Mode B:	VMXbus access only
Mode C:	VMEbus and VMXbus accesses
Mode D:	Disable of the VMEbus and VMXbus interface

The Read-Modify-Write cycles defined in the VMXbus specification are supported to synchronize multiple CPU boards if the VMEbus and the VMXbus interface is enabled.
The real data throughput on the VMXbus interface without concurrent transfers on the VMEbus side is 13 Mbyte/s using 32 bit data transfers.

VMXbus Access Times:

Write:	70 ns	No concurrent
Read:	210 ns	VMEbus accesses

1.3 Address Decoding

Unique address decoding logic providing a jumper selectable access address is installed on the SRAM-3B. The address lines A31 to A24 of the VMEbus are only decoded if the Extended Address Modifier code is selected. Otherwise, only the address signals up to A23 of the VMEbus and the VMXbus are used to detect if the board is addressed or not. The two independent memory areas can be placed in the 4 Gbyte address range in 512 Kbyte steps, depending on the memory capacity. This allows the adaption of the SRAM-3B to various applications without mirroring memory and losing capacity.
The memory capacity of the SRAM-3B board is split into two memory areas, each consisting of exactly half the total capacity as listed below:

SRAM-3B: 1 Mbyte capacity

The SRAM-3B contains 32 sockets supporting 32 devices with a 32K x 8 organization.

1.4 Battery Back-Up

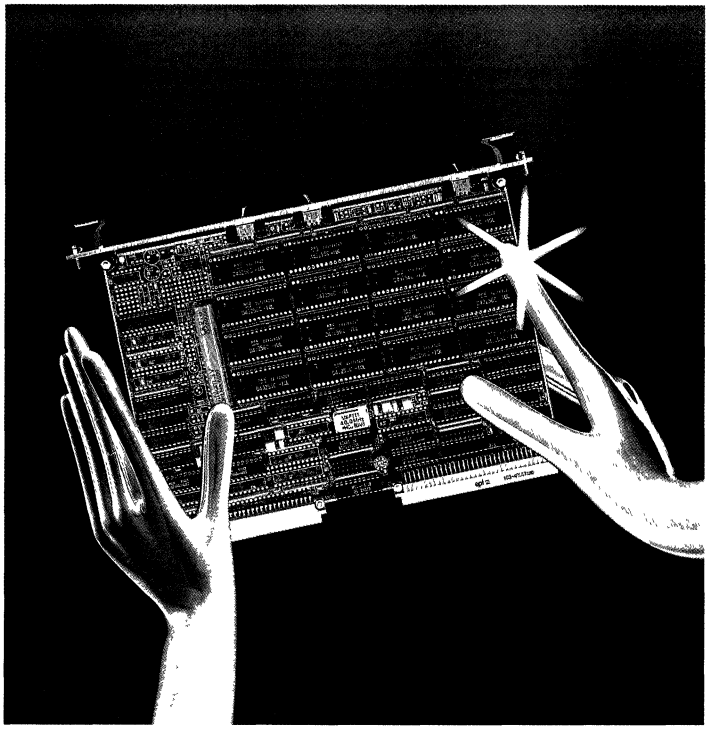
The SRAM-3B includes power fail detection circuitry and a lithium battery to guarantee data retention of the static RAMs for up to 1 year (calculated).
Data retention time can be extended if the +5V STDBY line is powered while +5V main is not active.
The board automatically detects when the +5V power drops below 4.65V and does not respond to the VMEbus and the VMXbus. In this case all the chip enable and select signals are driven inactive and the power down mode is activated.

Specification

Memory Memory Capacity VMEbus Interface VMXbus Interface	Static RAM organized in 2 Memory Areas 1 Mbyte on SRAM-3B IEEE 1014 standard compatible A32: D32, D32NA, D16, D8 A24: D32, D32NA, D16, D8 Read-Modify-Write and Unaligned Transfers supported Rev.B compatible A24: D32, D32NA, D16, D8 Read-Modify-Write and Unaligned Transfers supported			
Maximum Access Times	1st Cycle	VMEbus	VMXbus	Mode
	Write Read	80 ns 210 ns	70 ns 210 ns	no concurrent access
	1st Cycle	VMEbus	VMXbus	Mode
	Write Read	240 ns 370 ns	250 ns 380 ns	with concurrent access
Data Retention Time Special Hardware Functions Maximum Power Requirements	6000 h (calculated) Onboard voltage sensor supporting the battery back-up of the SRAMs RUN/LOCAL switch for each bus interface (VMEbus and VMXbus) Write protection switch for each of the two memory areas. Status and Access Control LEDs on the front panel. +5V: 5.6 A (P2 Backplane or power connection on P2 recommended)			
Operating Temperature Storage Temperature Relative Humidity Dimensions	0 to 50 degrees C –50 to +85 degrees C (non operating) 0–90% (non condensing) Double Eurocard 233 x 160 mm 9.2 x 6.3 inch			

Ordering Information

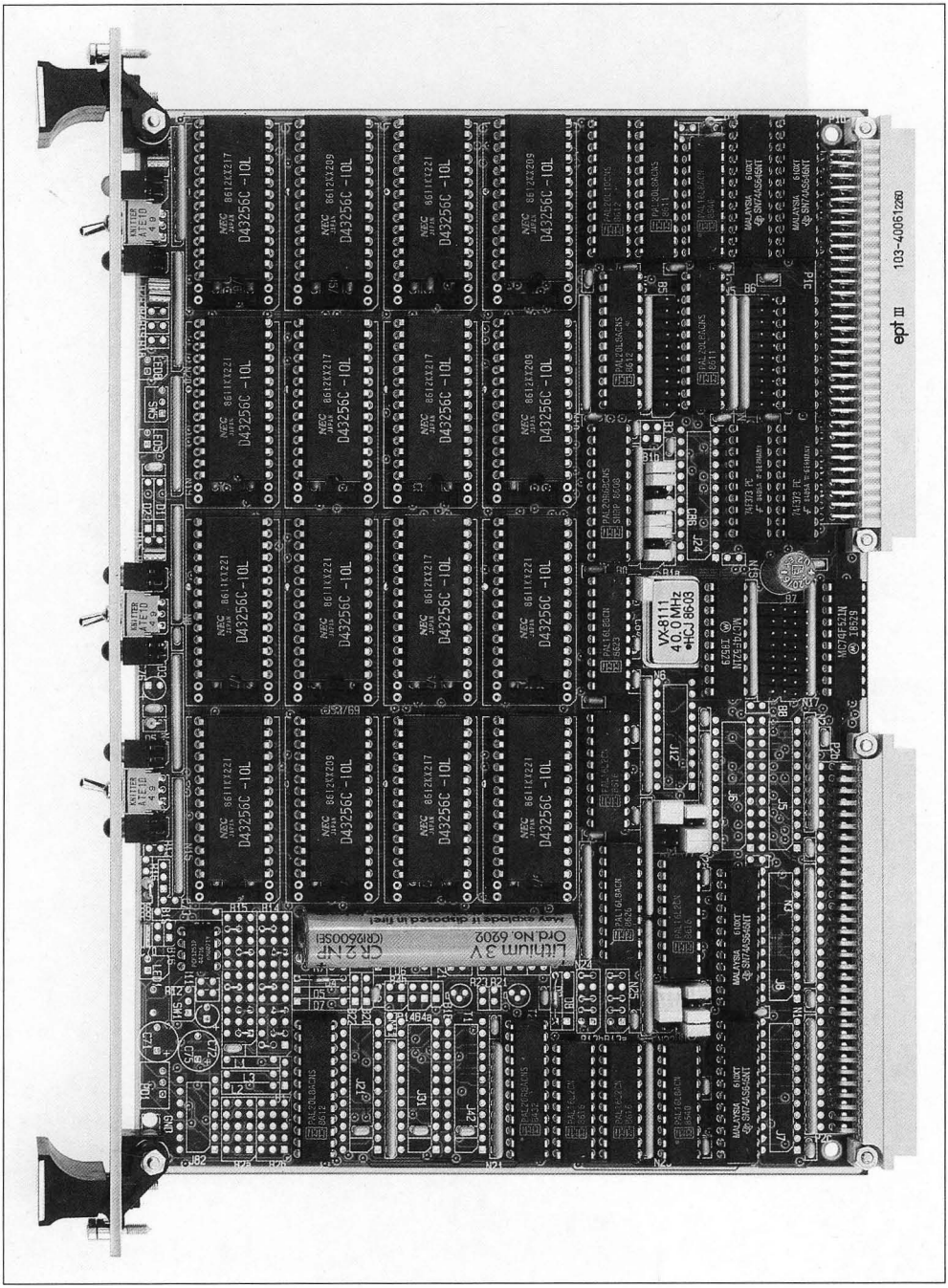
SYS68K/SRAM-3B Part No. 200402	1 Mbyte static RAM board with VMEbus and VMXbus interface including documentation.
SYS68K/SRAM-3B/UM Part No. 800104	User's Manual for the SYS68K/SRAM-3B board.



System 68000 VME SYS68K/SRAM-4B

32 Bit Static RAM Board

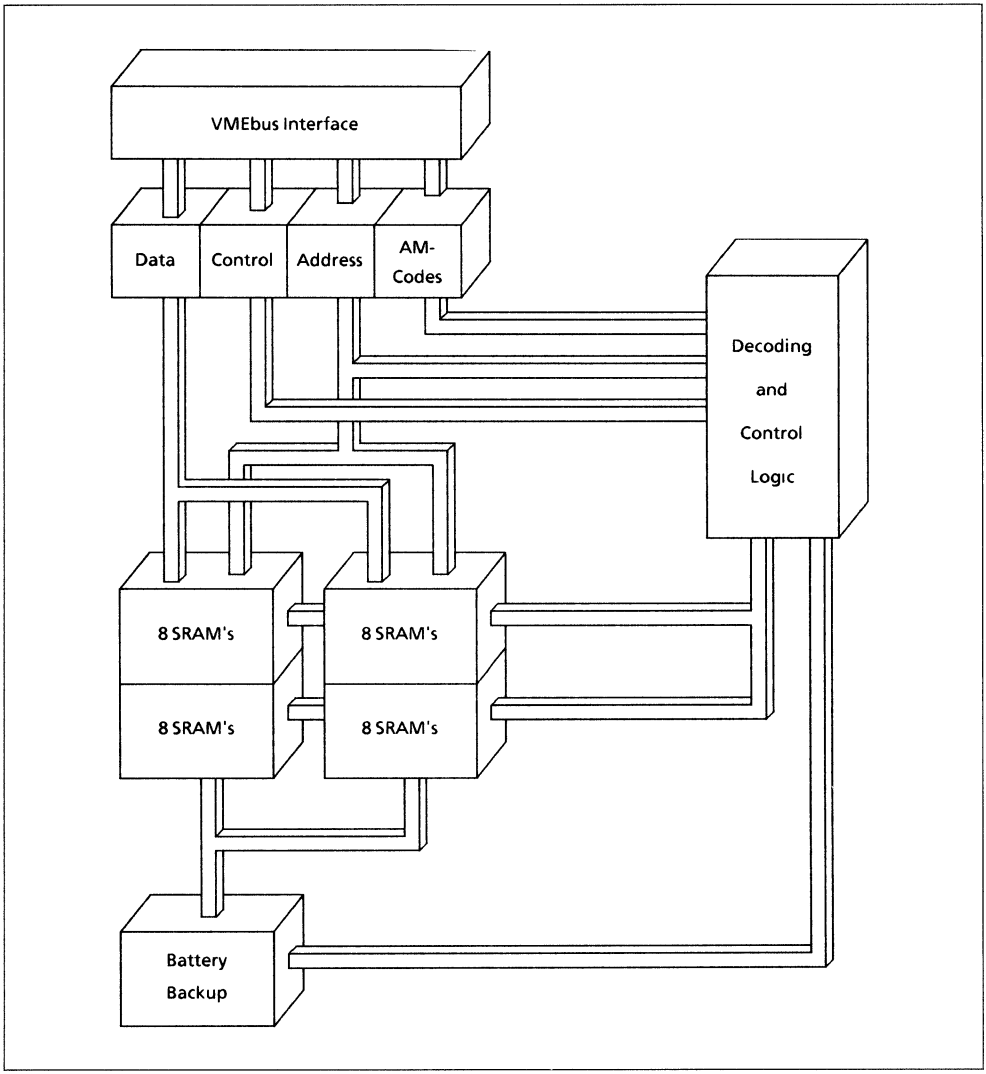
- VMEbus Interface (A32:D32)
- 1 Mbyte static RAM
- On-board battery backup
- 80/210ns Write/Read access time
- Jumper selectable access address


eptm 103-40061269

General Description
The SYS68K/SRAM-4B provides full static memory with an on-board battery back-up accessible via the VMEbus.
The 32 bit address and data support in conjunction with the fast static RAMs, offers high data throughput with maximum reliability. Access Address and Address Modifier code of the two memory areas are jumper selectable.

The SRAM-4B provides 1 Mbyte of high speed static RAM.
An on-board voltage sensor detects if the main power is out of specification and enables the on-board battery back up for the SRAMs realized with a lithium battery.

BLOCK DIAGRAM OF THE SYS68K/SRAM-4B



Features of the SYS68K/SRAM-4B

- 1024 Kbyte SRAM on SRAM-4B
- VMEbus Interface supporting the following data transfer modes:
  A24: D32, D32NA, D16, D8
  A32: D32, D32NA, D16, D8
  Read-Modify-Write cycles are supported.
- 2 memory areas which each have separate jumper selectable access addresses and address modifier codes.
  Write Access Time 80 ns
  Read Access Time 210 ns
- On-board battery back-up provides data retention for up to 1 year.

1.0 Functional Description

The SRAM-4B provides 1 Mbyte of static memory. The fully latched address and data bus provide an interleaved Write operation to minimize bus overhead and support a maximum transfer rate on the VMEbus of 4M transfer/s which results in a 16 Mbyte/s data throughput using 32 bit of data.
Installation in 16 or 32 bit environments is provided through the address modifier decoding (A24 or A32 mode) which defines the address range to be decoded.
Automatic data bus sizing and adaptation to 16 or 32 bit environments is provided through the on-board hardware logic.

1.1 The VMEbus Interface

A full IEEE 1014 standard compatible interface which supports the unaligned transfers is installed on the SRAM-4B.
32 bit of data and address are supported to take full advantage of 16 and 32 bit processor boards and DMA Controllers.

The following table lists the supported data transfer modes:

Transfer Type	D31–D24	D23–D16	D15–D8	D7–D0
Byte			x	x
Word Word (unaligned)		x	x x	x
3 Byte (unaligned)	x	x x	x x	x
Long Word	x	x	x	x

The address and data transfer modes supported on the SRAM-4B is:
A24: D32, D32NA, D16, D8
A32: D32, D32NA, D16, D8
Installation in 16 and 32 bit environments is possible using the address modifier selection. Each of the two fully independent memory areas, each consisting of half of the memory size, contains its own decoding logic, which allows the separation and assignment of different data/program segments.
A RUN/LOCAL switch to enable or disable accesses from the VMEbus is installed on the SRAM-4B.
For multi-processor synchronization, all defined Read-Modify-Write cycles are supported. A VMEbus Read and the following Write transfer cannot be interrupted.
The maximum data throughput of the SRAM-4B is 16 Mbyte/s.

VMEbus Access Times:

Write	80 ns
Read	210 ns

1.2 Address Decoding

Unique address decoding logic providing a jumper selectable access address is installed on the SRAM-4B. The address lines A31 to A24 of the VMEbus are only decoded if the Extended Address Modifier code is selected. Otherwise, only the address signals up to A23 of the VMEbus are used to detect if the board is addressed or not. The two independent memory areas can be placed into the 4 Gbyte address range in 512 Kbyte steps. This allows the adaption of the SRAM-4 boards to various applications without mirroring memory and losing capacity.
The memory capacity of the SRAM-4B board is split into two memory areas, each consisting of exactly half the total capacity as listed below:
SRAM-4B: 1 Mbyte capacity
The SRAM-4B contains 32 sockets supporting 32 devices with 32K x 8 organization.

1.3 Battery Back-Up

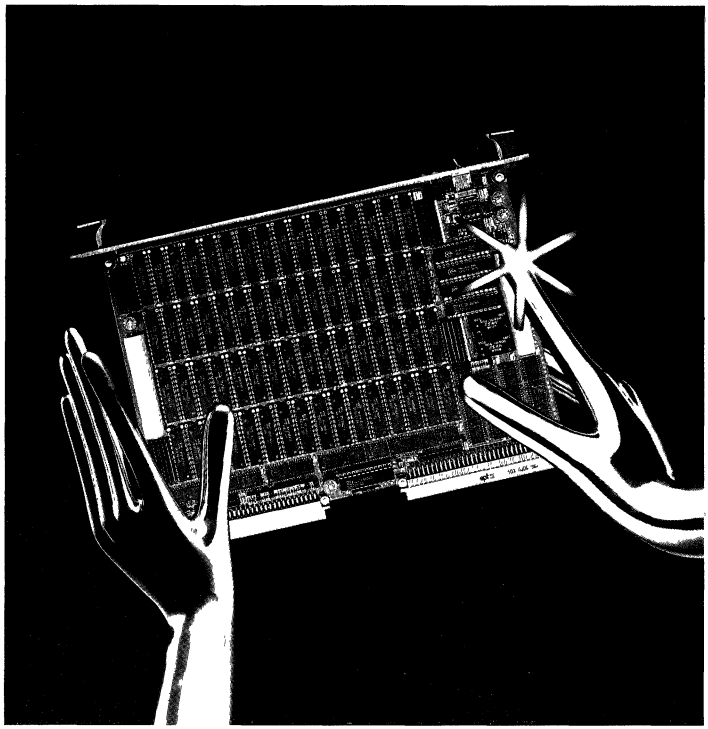
The SRAM-4B includes power fail detection circuitry and a lithium battery to guarantee data retention of the static RAMs of up to 1 year (calculated). Data retention time can be extended if the +5V STDBY line is powered while main +5V is not active.
The board automatically detects when the +5V power drops below 4.65V and does not respond to the VMEbus. In this case all the chip enable and select signals are driven inactive and the power down mode is activated.

Specification of the SYS68K/SRAM-4B

Memory Memory Capacity VMEbus Interface	Static RAM organized in 2 Memory Areas 1 Mbyte IEEE 1014 standard compatible A32: D32, D32NA, D16, D8 A24: D32, D32NA, D16, D8 Read-Modify-Write and Unaligned Transfers supported
Maximum Access Times	Write 80 ns Read 210 ns
Data Retention Time Special Hardware Functions Maximum Power Requirements	6000 h (calculated) Onboard voltage sensor supporting the battery back-up of the SRAMs RUN/LOCAL switch Write protection switch for each of the two memory areas. Status and Access Control LEDs on the front panel. (P2 Backplane or power +5V: 5.6 A connection on P2 recommended)
Operating Temperature Storage Temperature Relative Humidity Dimensions	0 to 50 degrees C –50 to +85 degrees C (non operating) 0–90% (non condensing) Double Eurocard 233 x 160 mm 9.2 x 6.3 inch

Ordering Information

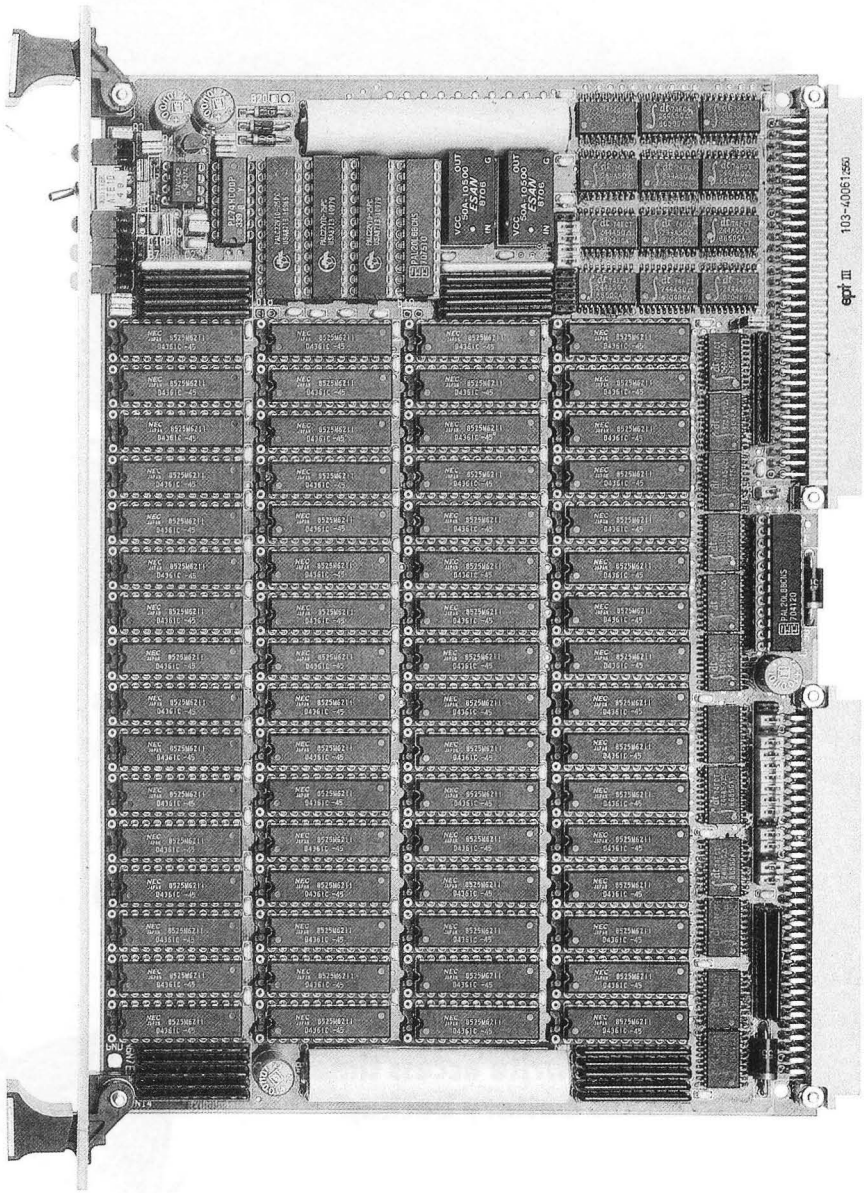
SYS68K/SRAM-4B Part No. 200502	1 Mbyte static RAM board with VMEbus interface including documentation.
SYS68K/SRAM-4/UM Part No. 800116	User's Manual for the SYS68K/SRAM-4B board.



System 68000 VME
SYS68K/SRAM-5/6

32 Bit High Speed Static RAM Board

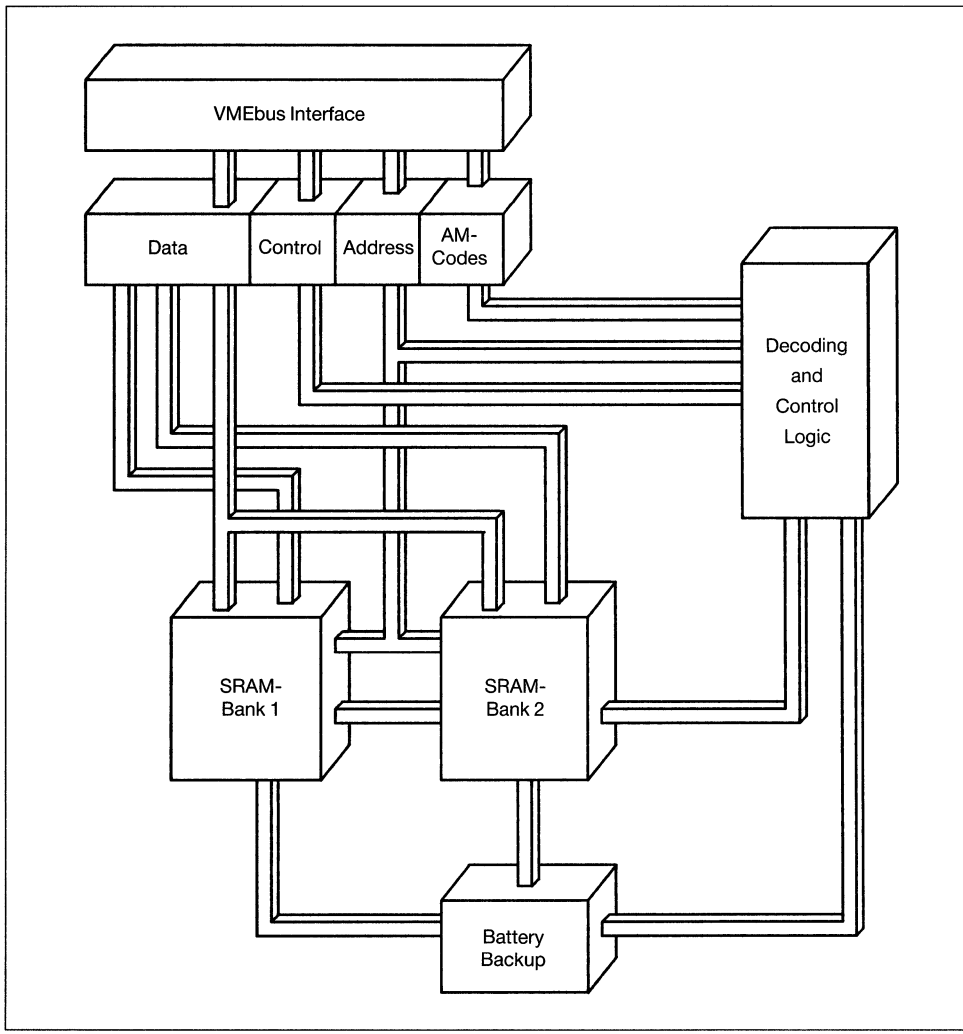
- 512 Kbyte or 2 Mbyte SRAM
- 32 bit VMEbus Interface
- 55 ns read/write access times
- On board battery backup



General Description

The SYS68K/SRAM-5/6 boards provide fast static memory which is accessible via the VMEbus, taking full advantage of the VMEbus bandwidth. The 32 bit address and data support, in conjunction with the fast static RAMs, offers high data throughput with maximum reliability. The Access Address and Address Modifier codes of the two memory areas are jumper selectable. The SRAM-5 features 512 Kbyte memory capacity built with high speed static RAM, while the SRAM-6 provides 2 Mbyte capacity. An on-board voltage sensor detects if the supply voltage is out of specification, and enables the on-board battery backup (two lithium batteries) for the SRAMs.

BLOCK DIAGRAM OF THE SYS68K/SRAM-5/6



Features of the SYS68K/SRAM-5/6 Boards

- SRAM-5: 512 Kbyte SRAM
- SRAM-6: 2048 Kbyte SRAM
- VMEbus Interface supports the following data transfer modes:
  A24: D32,D32NA,D16,D8
  A32: D32,D32NA,D16,D8
  Read-Modify-Write cycles are supported.
- 2 memory areas with high speed static CMOS RAMs.
  Write Access Time 55 ns (max), 50 ns (typ)
  Read Access Time 55 ns (max), 50 ns (typ)
- On-board battery backup provides data retention for up to 1 year.

1.0 Functional Description

The fully latched address and data bus provide interleaved Read and Write operation to minimize bus overhead and to support a maximum transfer rate on the VMEbus of 9M transfer/s. This results in a 36 Mbyte data throughput using 32 bit data. Installation in 16 or 32 bit environments is provided through the address modifier decoding (A24 or A32 mode) which defines the address range to be decoded. Automatic data bus sizing, and adaptation to 16 or 32 bit environments, are provided through on-board hardware logic.

1.1 The VMEbus Interface

A full VMEbus IEEE 1014 (Rev C.) compatible interface which supports the unaligned transfers is installed on the SRAM-5/6 boards. 32 bit of data and address are supported to take full advantage of 16 and 32 bit processor boards and DMA Controllers. The following table lists the supported data transfer modes:

Transfer Type	D31-D24	D23-D16	D15-D8	D7-D0
Byte Byte			 x	x
Word Word (unaligned)		 x	x x	x
3 Byte (unaligned)	 x	x x	x x	x
Long Word	x	x	x	x

The addressing and data transfer modes supported on the SRAM-5/6 boards are:

A24: D32, D32NA, D16, D8
A32: D32, D32NA, D16, D8

Installation in 16 and 32 bit environments is possible using the Address Modifier selection. Each of the two fully independent memory areas, which consist of half of the memory size, contain their own decoding logic. This allows the separation and assignment of different data/program segments. A RUN/LOCAL switch to enable or disable accesses from the VMEbus is installed on each of the SRAM-5/6 boards. For multi-processor synchronization, all defined Read-Modify-Write cycles are supported. The maximum data throughput of the SRAM-5/6 boards is 36 Mbyte/sec. VMEbus Worst Case Access Times:

Write 55 ns
Read 55 ns

1.2 Address Decoding

A unique address decoding logic which provides a jumper selectable access address, is installed on the SRAM-5/6 boards. The address lines A31 to A24 of the VMEbus are only decoded if the Extended Address Modifier code is selected; otherwise, only the address signals up to A23 of the VMEbus are used in order to detect whether or not the board is addressed. The independent memory areas can be placed anywhere in the 4 Gbyte address range in 512 Kbyte/2 Mbyte steps, depending on the memory capacity. This allows the adaption of the SRAM-5/6 boards to various applications without mirroring memory and losing capacity.

The memory capacity of each SRAM-5/6 board version is as follows:

SRAM-5: 2 x 256 Kbyte total capacity
SRAM-6: 2 x 1 Mbyte total capacity

1.3 Battery Backup

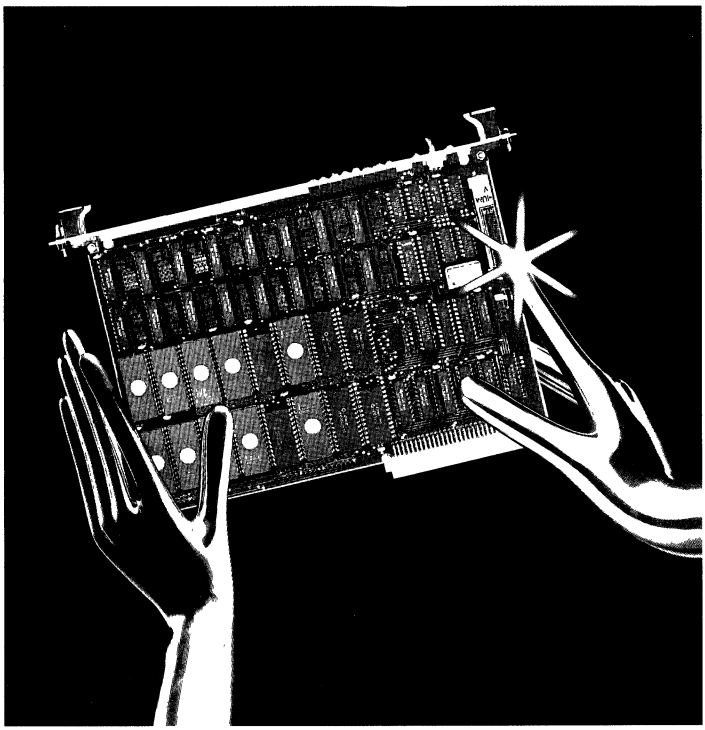
The SRAM-5/6 boards include power fail detection circuitry and two lithium batteries to guarantee data retention of the static RAMs for up to 1 year (calculated). Data retention time can be extended if the +5V STDBY line is powered while +5V mains are not active. The board automatically detects when the +5V supply voltage drops below 4.65V and does not respond to the VMEbus. In this case all the chip enable and select signals are driven inactive and the power down mode is activated.

Specifications of the SYS68K/SRAM-5/6

Memory	Static RAM organized in 2 Memory Areas
Memory Capacity	SRAM-5: 512 Kbyte SRAM-6: 2 Mbyte
VMEbus Interface	IEEE 1014 (Rev C.) compatible A32: D32, D32NA, D16, D8 A24: D32, D32NA, D16, D8 Read-Modify-Write and Unaligned Transfers are supported
Maximum Access Times	Write 55 ns Read 55 ns
Data Retention Times	SRAM-5 10000 h (typical) SRAM-6 6000 h (typical) (all times are calculated)
Special Hardware Functions	On-board voltage sensor supporting the battery backup of the SRAMs RUN/LOCAL switch Status and Access Control LEDs on the front panel.
Power Requirements	typ max +5V 3,5A 6A
Operating Temperature	0 to 50 degrees C
Storage Temperature	−50 to +85 degrees C (non operating)
Relative Humidity	0 to 90 % (non condensing)
Dimensions	Double Eurocard 243 x 160 mm 9.2 x 6.3 in.

Ordering Information

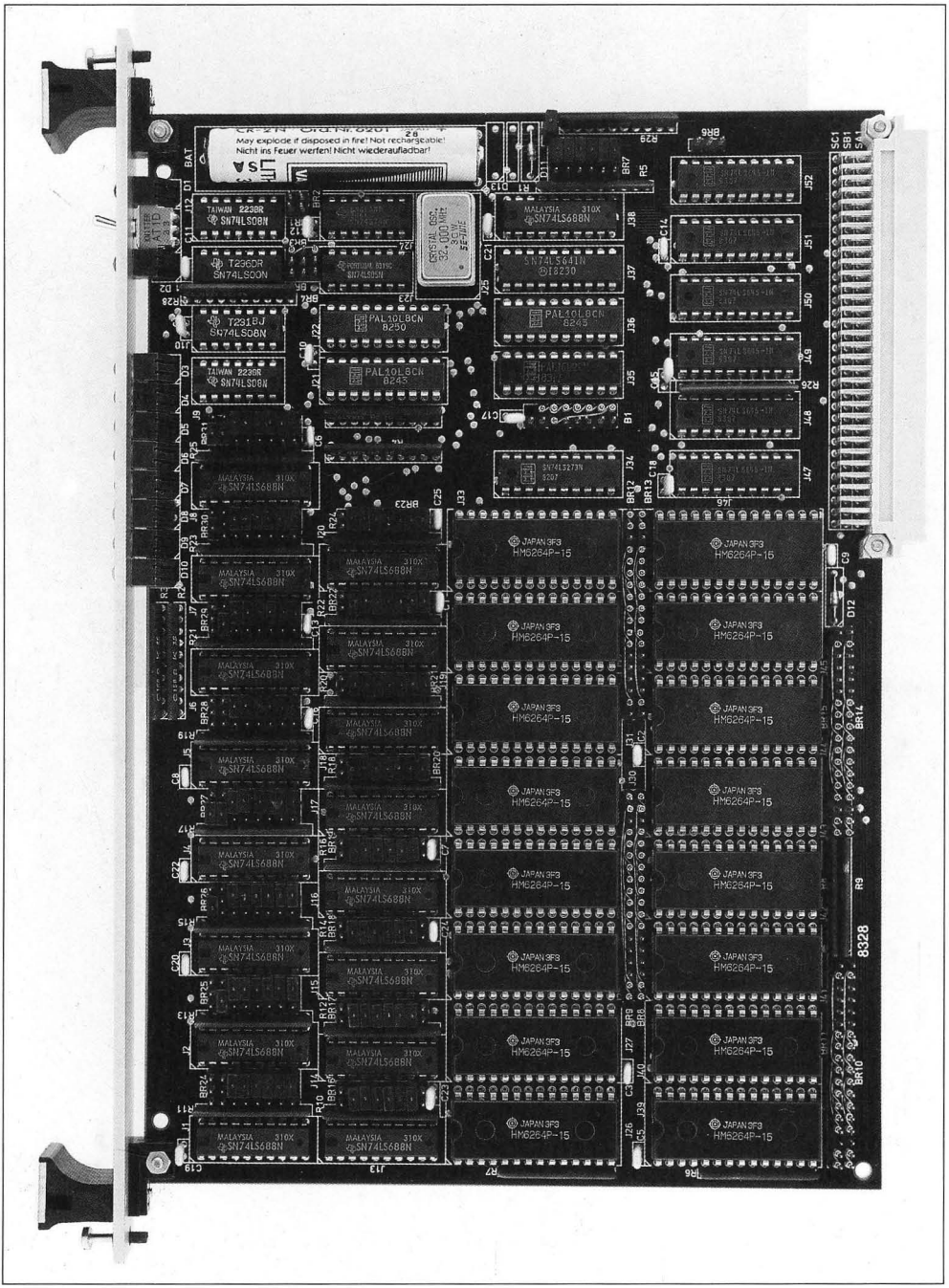
SYS68K/SRAM-5 Part No. 200504	512 Kbyte static RAM board with VMEbus Interface including documentation.
SYS68K/SRAM-6 Part No. 200505	2 Mbyte static RAM board with VMEbus Interface including documentation.
SYS68K/SRAM-5/6/UM Part No. 800137	User's Manual for all SYS68K/SRAM-5/6 board versions.



System 68000 VME SYS68K/RR-1

Static RAM/ROM/EPROM Board

- 16 sockets up to 512 Kbyte EPROM
- Selectable access time
- Battery backup for SRAM
- For wide range of EPROM/ROM/SRAM devices


May explode if disposed in fire! Not rechargeable!
Nicht ins Feuer werfen! Nicht wiederaufladbar!
8328

General Description

This board provides additional global SRAM, ROM or EPROM capacity in a VME bus based microcomputer system. The 28 pin sockets can contain Static Random Access Memories (SRAM's), Read Only Memories (ROM's) or Erasable and Programmable Read Only Memories (EPROM's). The maximum capacity of EPROM/ROM space using 32 Kx8 organized devices like 27256 is 512 Kbyte.

Eight banks are separately configurable for the different device types which offer a variety of applications. The battery option allows data storage in Power Fail or Power Down modes, furthermore a LOCAL/RUN function switch performs the isolation of the SYS68K/RR-1 from the VMEbus. Two LED's indicate the selected modes and additional 8 LED's indicate an access to one of the eight areas.

The base address of each area may be selected separately via jumper. The address modifier decoding can be used in addition to the base address for each area (jumper selectable).

Usable Device Types

The base address decoding includes a jumper field which allows free selectable decoding for each area in 4, 8, 16, 32 or 64 Kbyte steps. Therefore continuous memory space can be generated for SRAM's, PROM's or EPROM's with different memory sizes.

Each area contains two 28 pin sockets, one for the lower 8 data bits (D0-D7) and one for the upper data bits (D8-D15). The socket select lines are address dependent and strobed by the DS0 and DS1 signals of the VMEbus. Therefore word transfers (16 bit) or byte transfers (8 bit) can be forced.

The memory space of the board is device dependent and a maximum capacity of 512 Kbyte can be obtained by using 32 Kbyte devices and 128 Kbyte by using 8 Kbyte devices. Table 1 lists some of the supported device types which can be inserted in the 28 pin sockets. Access speed for each area may be set separately from 62.5 ns to 500 ns in increments of 62.5 ns. Therefore, for critical real time applications, slow ROM/EPROM devices and high speed SRAM's may be mixed on the same board.

The WRITE signal of the VME bus may be used as read/write protection line for the SRAM area.

Separately for each area a battery back-up is provided (when SRAM's are used) to save data during power down or power fail.

Shipment includes the SYS68K/RR-1/UM and 100 jumpers for address selection and address modifier decoding.

BLOCK DIAGRAM OF THE SYS68K/RR-1

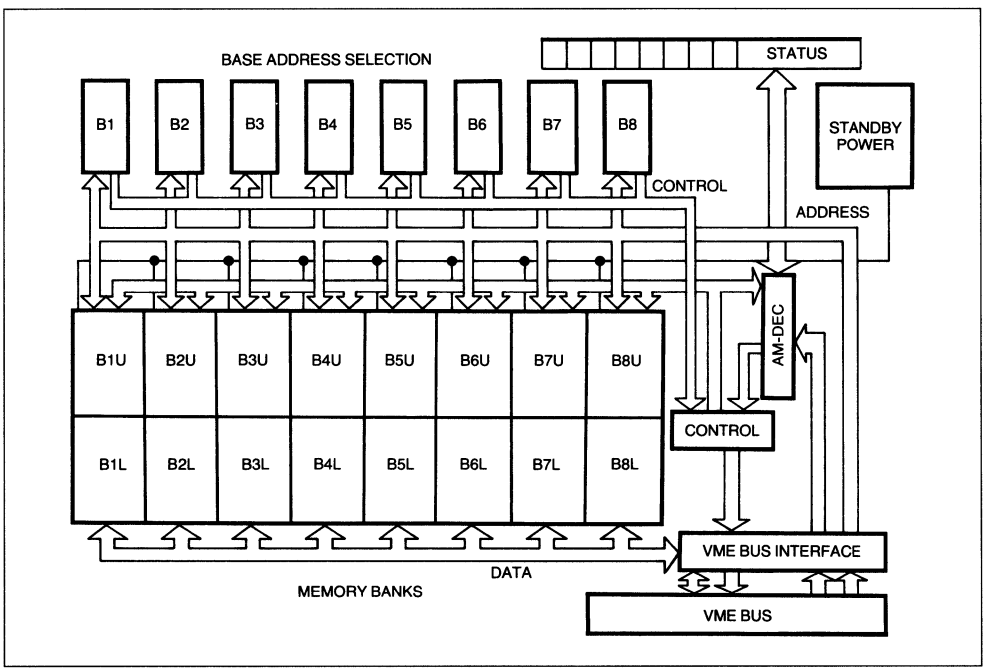


Table 1 Usable Device Types

	EPROM	ROM	SRAM	SIZE
DEVICES	2716		8416	2 Kx8
	2516		8128	
	2732	58735		4 Kx8
	2532	46332		
	2764	37000	6264	8 Kx8
		48364		
	27128	613128		16 Kx8
	27256	38000		32 Kx8

SYS68K/RR-1S

This version of the SYS68K/RR-1 includes 16 static CMOS RAM's with 8 Kbyte each. Therefore the SRAM memory size is 128 Kbyte in a continuous block as default set during manufacturing.
High speed SRAM's have an access time of 100 ns and the access through the VMEbus to the SRAM's takes less than 180 ns.
The on-board battery guarantees data retention for more than 1000 hours during power fail or main power down in accordance with the VMEbus specification.

SYS68K/RR-1 Specification

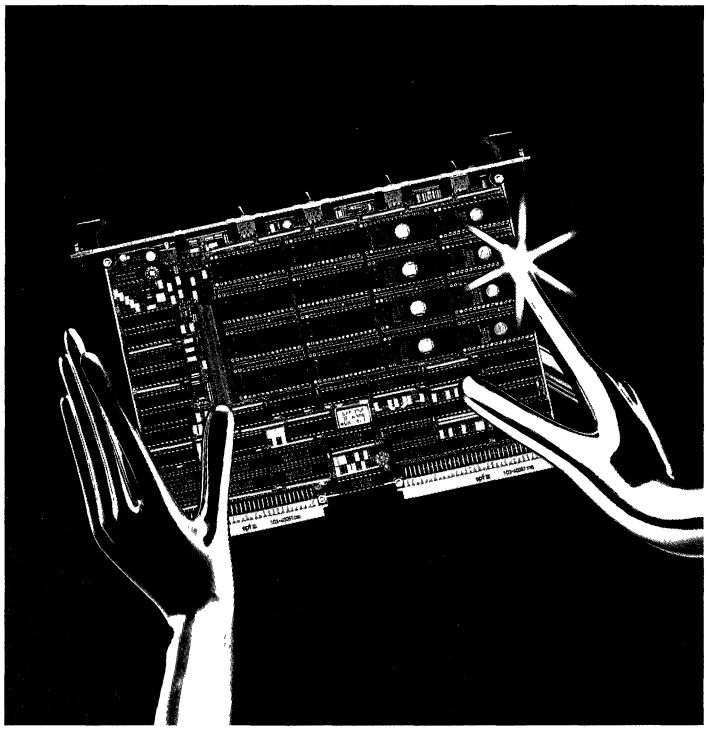
Memory Space	512 Kbyte (max.) 16 sockets for user supplied devices. Free selectable base address for each area Free selectable access time (62.5 to 500 ns) for each area Address Modifier decoding Battery back-up for SRAM's
Control	RUN/LOCAL switch for bus isolation 2 Status LED's 8 Access LED's for control
Bus	VME bus interface
Transfer	Byte (8 bit) and Word (16 bit) transfers as well as Read/Write or Read-Modify-Write cycles can be forced Access time is device selectable
Power Requirements	+5V/1.2 A (max)
Operating Temperature	0 to +70 degrees C
Storage Temperature	−50 to +85 degrees C
Relative Humidity	0–95% (non-condensing)
Front Panel	6HE/4TE
Board Dimensions	Double Eurocard 234x160 mm (9.2x6.3 inch)

SYS68K/RR-1S Specification

Memory	128 Kbyte of SRAM
Transfer	Read/Write in Byte or Word Mode Access time 250 ns (max)
Data Retention	1000 hours (min) at power down
Power Requirements	+5V/1.8 A (max) +5V STDBY/80 mA (Power Down Mode)

Ordering Information

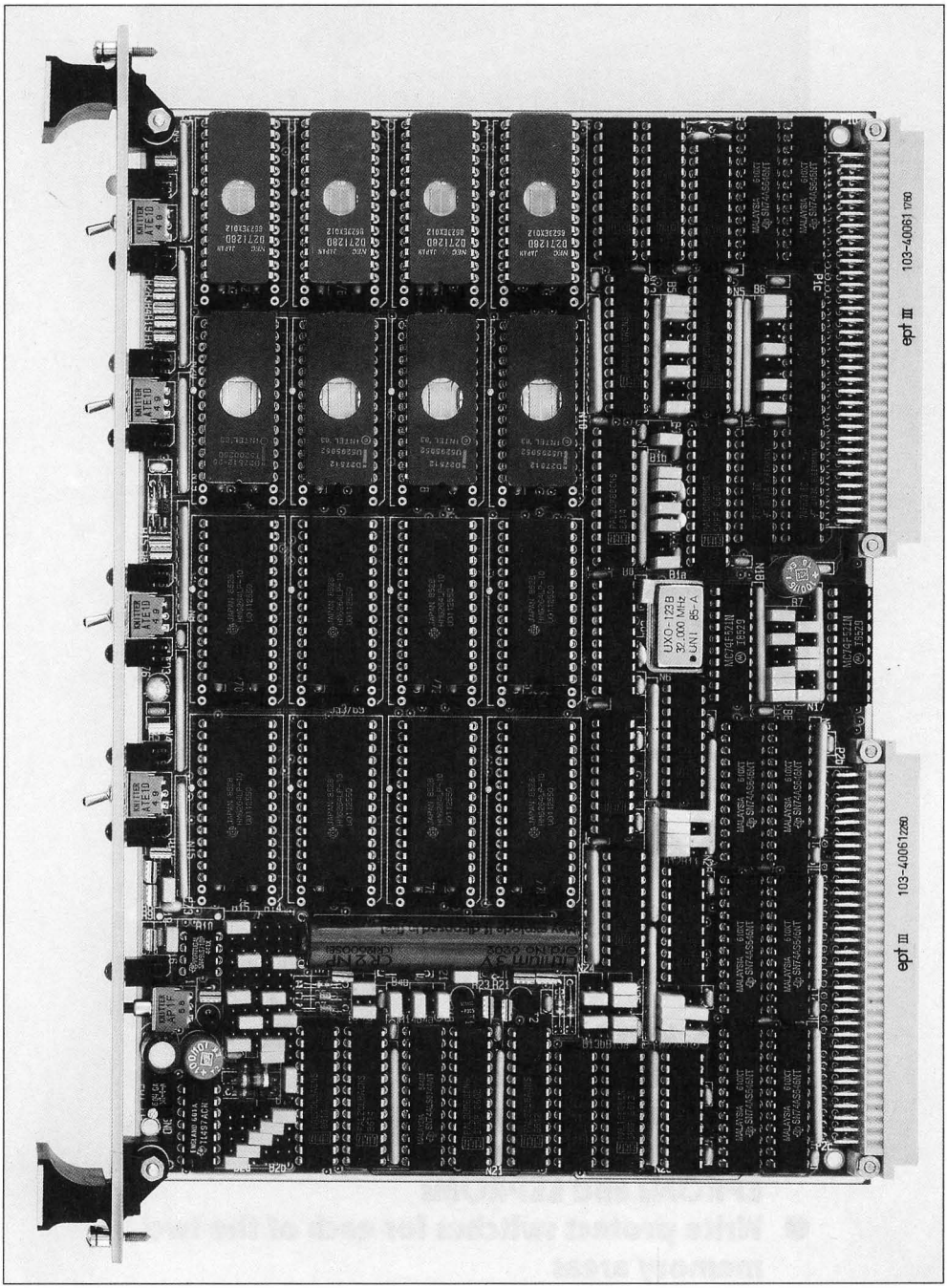
SYS68K/RR-1 Part No. 200010	SRAM/ROM/EPROM Board including User's Manual
SYS68K/RR-1S Part No. 200011	128 Kbyte SRAM Board including User's Manual
SYS68K/RR-1/UM Part No. 800005	User's Manual for the SRAM/ROM/EPROM Board



System 68000 VME SYS68K/RR-2

32 Bit RAM/ROM Board with VMEbus and VMXbus Interface

- **16 sockets for 28 and 32 pin JEDEC compatible devices**
- **On-board battery backup for static RAMs**
- **On-board programming logic for EPROMs and EEPROMs**
- **Write protect switches for each of the two memory areas**


epi III 103-40061280
epi III 103-40061780
UXO-123B
32.000 MHz
UN1 85-A

General Description

The SYS68K/RR-2 board is a high speed 32 bit memory board using up to 16 JEDEC compatible devices. The VMEbus interface is capable of transferring 8, 16, 24 and 32 bit of data according to the VMEbus IEEE 1014 standard.

In addition to the 32 bit VMEbus interface, a full 32 bit VMXbus interface is installed on the RR-2. It supports unaligned transfers from the VMEbus as well as from the VMXbus. Read-Modify-Write cycles for multi-processor synchronisation are also supported. The VMEbus and the VMXbus interface can separately be enabled or disabled via two switches installed on the front panel.

A dual port control logic is installed on the RR-2 to control the accesses of the two independent asynchronous buses.

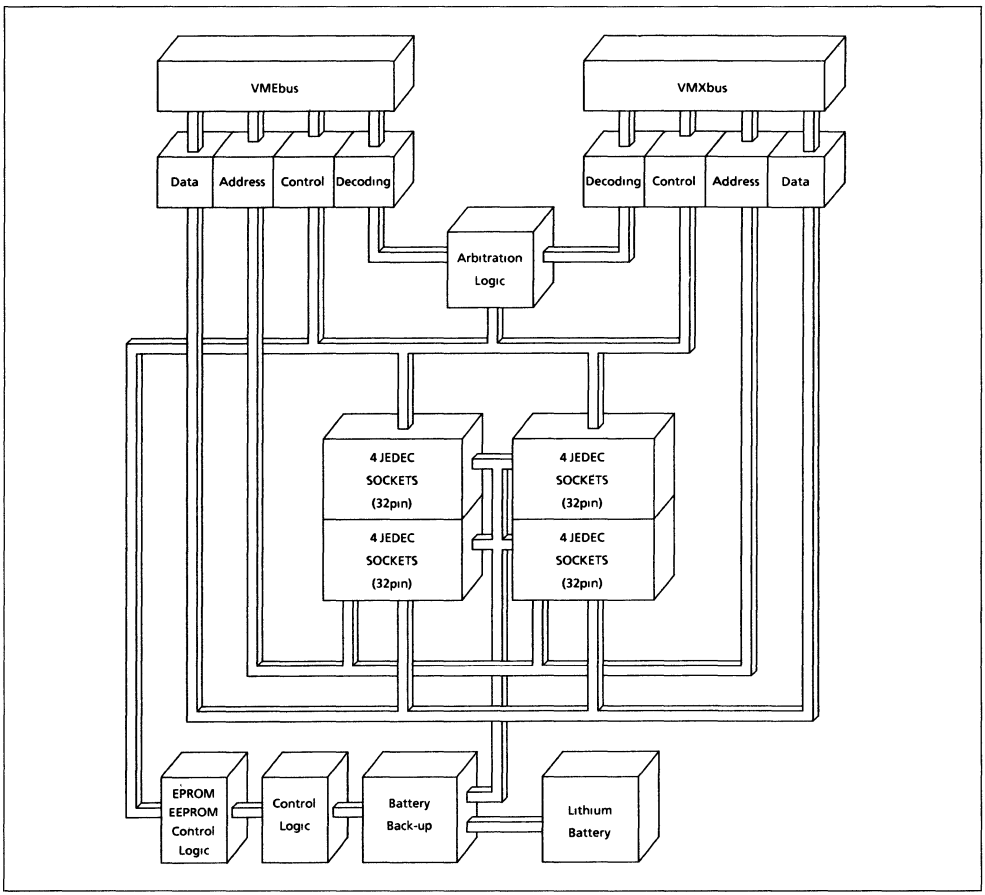
Both the 28 pin and the 32 pin standard for SRAMs, EPROMs and EEPROMs are supported to offer a maximum EPROM capacity of 2 Mbyte if 128 K x 8 devices are used. Two different memory areas, each consisting of 8 sockets are installed on the board to allow mixing of device types (i.e. one SRAM and one EPROM area).

Each memory area has a jumper selectable access address in device dependent boundaries and a set of selectable address modifier codes. The access speed for each memory area is jumper selectable to adapt the access times of the used devices.

A battery back-up with a voltage sensor is installed on the RR-2 to allow data retention for SRAM devices for up to 1 year.

To maintain reprogramming of data in special applications, the RR-2 contains hardware logic to program EPROMs and EEPROMs.

BLOCK DIAGRAM OF THE SYS68K/RR-2



Features of the SYS68K/RR-2

- IEEE 1014 interface supporting 32 data and 32 address lines.
- Jumper selectable access address and address modifier code.
- 16 sockets for JEDEC compatible devices using the 28 or 32 pin standard.
- VMXbus interface (Rev.B compatible) supporting 32 data and 23 address lines.
- Arbitration mechanism between VMXbus and VMEbus accesses supporting Read, Write and Read-Modify-Write cycles.
- 2 independent memory areas each consisting of 8 devices.
- Typical Access Times using 100ns devices:

	VMEbus	VMXbus	Conditions
Write Read	70ns 200ns	70ns 180ns	No concurrent Accesses

- Battery back-up for static RAMs.
- Programming of EEPROMs and Chip Erase function switch.
- Programming of EPROMs (21V and 12V types).
- Write protection switch for each of the two memory areas.
- RUN/LOCAL switch for the VMEbus and VMXbus interface.
- Jumper selectable access address and address modifier code for each of the two memory areas.
- Status and Access indication LEDs.

1.0 Functional Description

The two different memory areas, each consisting of 8 sockets are accessible via the VMEbus or VMXbus interface and provide global memory such as static RAM, EPROM or EEPROM.
The two bus interfaces allow the use of the RR-2 board as a global Dual Ported Memory accessible through the VMXbus interface for the host CPU and accessible through the VMEbus interface from other CPU-boards for multi-processing or from an intelligent controller board featuring DMA.
The Read-Modify-Write cycles from both bus interfaces are supported to provide multi-processor synchronisation as well as shared memory resources.
A Write Protect switch for each memory area installed on the front panel allows the protection of the memory area against non privileged modification.
EPROMs and EEPROMs can be programmed via special on-board hardware logic which makes a PROM programmer obsolete for most of the rommable software development packages. The EPROM programming feature of the RR-2 is supported under the Real Time Multi User Multitasking Operating System PDOS*.
Further details of the board features are described in the following paragraphs.

1.1 The VMEbus Interface

The RR-2 contains a full 32 bit interface providing highest data throughput. A RUN/LOCAL switch can disable the VMEbus interface to allow use of the board as a VMXbus board.
On Write cycles, the 32 bit data and address are latched and a DTACK will be generated immediately if this operation is completed, and if the Write Protection is not activated for the addressed memory area.
The internal Write cycle starts in parallel and will be executed depending on the selected access time of the used devices.
The access times on Read and Write cycles depends on the load from the VMXbus interface as well as on Read cycles on the access time of the installed devices.

Write: 80 ns
Read: 210 ns (using 100ns SRAMs)
310 ns (using 200ns EPROMs)

All listed times are the maximum response times measured without accessing the RR-2 board from the VMXbus interface.
The access address of the two independent memory areas is jumper selectable in device dependent steps.
The unaligned transfers, defined in the VMEbus specification are fully supported to take advantage of the 68020 data bus handling.
Data Transfer Modes:

A32: D32, D32NA, D16, D8
A24: D32, D32NA, D16, D8

The maximum data transfer speed over the VMEbus without concurring accesses via the VMXbus is 16 Mbyte/s using 100ns SRAM devices.

1.2 The VMXbus Interface

A 32 bit VMXbus interface is installed on the RR-2 to offer a dual port function together with the VMEbus. The access address for the two memory areas is identical to the decoding of the lower address lines of the VMEbus (A24 Mode). A RUN/LOCAL switch for the two memory banks is used to disable accesses to the board from the VMXbus side if only VMEbus transfers need to be supported.
The following data transfer modes are supported:

A24: D32, D32NA, D16, D8

The Unaligned and the Read-Modify-Write cycles are supported on the VMEbus and VMXbus for multi-processor synchronisation.
The Read and Write access times of the VMXbus interface depend on the load from the VMEbus interface (number of initiated transfers) and on the access times of the installed devices. The time values listed below are measured without any load from the VMEbus.

Write	80 ns (independent of the device access time)
Read	190 ns (using 100ns SRAM and no VME access)

Times are measured between a driven data strobe and a driven DTACK on the VMXbus. The early DTACK option of the VMXbus is not used for measurement.

1.3 Access Address Selection

Each of the two memory areas provides an individual selectable access address which is device capacity dependent. The address modifier code can also be selected for each memory area.
The access address which is compared depends on the selected address modifier code. The hardware logic of the RR-2 automatically detects if A24 or A32 decoding is selected (Extended or Standard addressing).
Each of the 8 defined AM-codes can be separately enabled or disabled via jumper settings.
The VMXbus access address decoding is identical to the A24 address set-up of the VMEbus interface to guarantee linear addressing.

1.4 Use of EPROM Devices

The RR-2 is designed to support 28 and 32 pin JEDEC compatible devices. The pin-out of both standards is outlined below.
16 sockets each consisting of 32 pins are installed on the RR-2 to support the following device types:

Device	Organisation	No of PINs Used	Total Capacity
2764	8 K x 8	28	128 Kbyte
27128	16 K x 8	28	256 Kbyte
27256	32 K x 8	28	512 Kbyte
27512	64 K x 8	28	1 Mbyte
271024	128 K x 8	32	2 Mbyte
TBD	256 K x 8	32	4 Mbyte
TBD	512 K x 8	32	8 Mbyte
TBD	1 M x 8	32	16 Mbyte

The remaining 3 pins of the 32 pin socket can be adapted to accept EPROMs with a capacity of up to 1 Mbyte per chip which then results into a total capacity of 16 Mbyte if the chips become available.

Each memory area can be equipped with different device types allowing the insertion of SRAMs, EPROMs and EEPROMs at the user's discretion.
A Write Protect switch on the front panel protects SRAM, EPROM and EEPROM devices from writing because the RR-2 contains a hardware logic to program EPROMs which have a programming voltage of 12.5 or 21V. The programming time (standard or intelligent algorithm) per cycle can be adapted to the used devices.

1.5 Use of EEPROM Devices

The RR-2 accepts EEPROM devices with at least 64K bit capacity (8K x 8 organisation). Logic to program EEPROMs is installed on the board to allow the modification of parameters during run time without exchanging the devices.
A chip erase switch is installed on the board to erase a maximum of 4 chips at a time (depending on the initiated data transfer which enables the chip erase function for the selected devices).
A Write Protect switch allows each memory bank to be protected against overwriting.
The following table lists all supported devices and the total capacity if all sockets are fitted with identical devices.

Device Type	Organisation	No of PINs Used	Total Capacity
58064,2864, 5233	8 K x 8	28	128 Kbyte
TBD	32 K x 8	28	512 Kbyte
TBD	64 K x 8	32	1 Mbyte
TBD	128 K x 8	32	2 Mbyte
TBD	256 K x 8	32	4 Mbyte
TBD	512 K x 8	32	8 Mbyte

1.6 Use of SRAM Devices

The RR-2 contains 16 sockets which may be used for static RAM insertion. The standard pin assignments for 8 K x 8 and 32 K x 8 devices is supported, resulting into a capacity of 128 or 512 Kbyte.
Expansion of the memory capacity is provided by using 32 pin devices.
The following table lists the supported devices and the future extention:

Device Type	Organisation	No of PINs Used	Total Capacity
6264	8 K x 8	28	128 Kbyte
62256	32 K x 8	28	512 Kbyte
TBD	128 K x 8	32	2 Mbyte
TBD	512 K x 8	32	8 Mbyte

An on-board lithium battery and a voltage sensor provide battery back-up of "low power" specified SRAMs (CMOS) of up to 1 year (SRAM dependent).

The on-board logic can be adjusted to the access time of the SRAMs to support various devices and optimize data throughput to the VMEbus and VMXbus interface.

Specification of the SYS68K/RR-2

VMEbus Interface:	VMEbus IEEE 1014 standard compatible. Read-Modify-Write and Unaligned transfers supported. A32: D32, D32NA, D16, D8 A24: D32, D32NA, D16, D8 Independent Address and Address Modifier Decoding for each of the 2 memory areas. RUN/LOCAL switch disabling VMEbus accesses.
VMXbus Interface:	VMXbus Rev.B compatible. Read-Modify-Write and Unaligned transfers supported A24: D32, D32NA, D16,D8 RUN/LOCAL switch disabling VMXbus accesses. Independent address and decoding for each of the 2 memory areas.
Sockets:	16 sockets for 28 or 32 pin devices (JEDEC Compatible pin out)
Memory Space:	EPROM: 28 pin devices 1 Mbyte (max) 32 pin devices 16 Mbyte (max) EEPROM: 28 pin devices 512 Kbyte (max) 32 pin devices 8 Mbyte (max) SRAM: 28 pin devices 512 Kbyte (max) 32 pin devices 8 Mbyte (max)
Access Times:	The access time of the board can be adapted to the speed of the used devices between 75 and 475ns in 25ns steps.

Access Times without concurrent transfers:

	VMEbus	VMXbus	Type
Write	50 ns 80 ns	50 ns 80 ns	MIN MAX
Read	180 ns 210 ns	170 ns 190 ns	MIN MAX

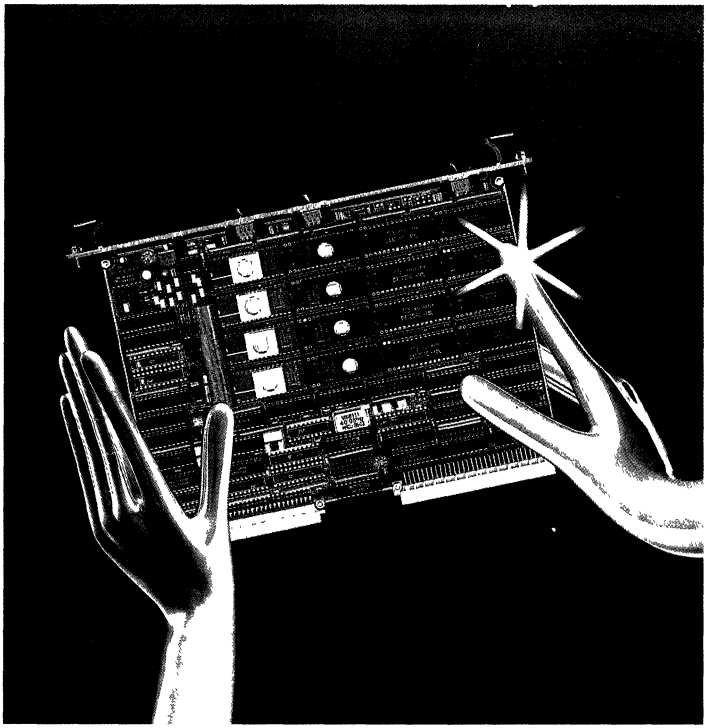
Access Times with concurrent transfer:

	VMEbus	VMXbus	Type
Write	210 ns 240 ns	220 ns 250 ns	MIN MAX
Read	340 ns 370 ns	350 ns 380 ns	MIN MAX

Special Functions:	EPROM programming function for +12V and +21V devices included. EEPROM programming function for +5V devices included. Chip Erase switch for EEPROMs included. SRAM battery back up for up to 1 year data retention with onboard lithium battery. Write Protect switches for each of the two independent memory areas. RUN/LOCAL switches for the VMEbus and VMXbus interface RUN/LOCAL, Access Protect and Chip Erase control LEDs for status monitoring installed on the front panel.
Power Requirements:	+ 5V : 3.4A (P2 Backplane or power connection +12V : 0.2A on P2 recommended)
Operating Temperature:	0 to 50 degrees C
Storage:	−50 to +85 degrees C (non operating)
Relative Humidity:	0–90% (non condensing)
Board Dimensions:	Double Eurocard 233 x 160 mm 9.2 x6.3 inch

Ordering Information:

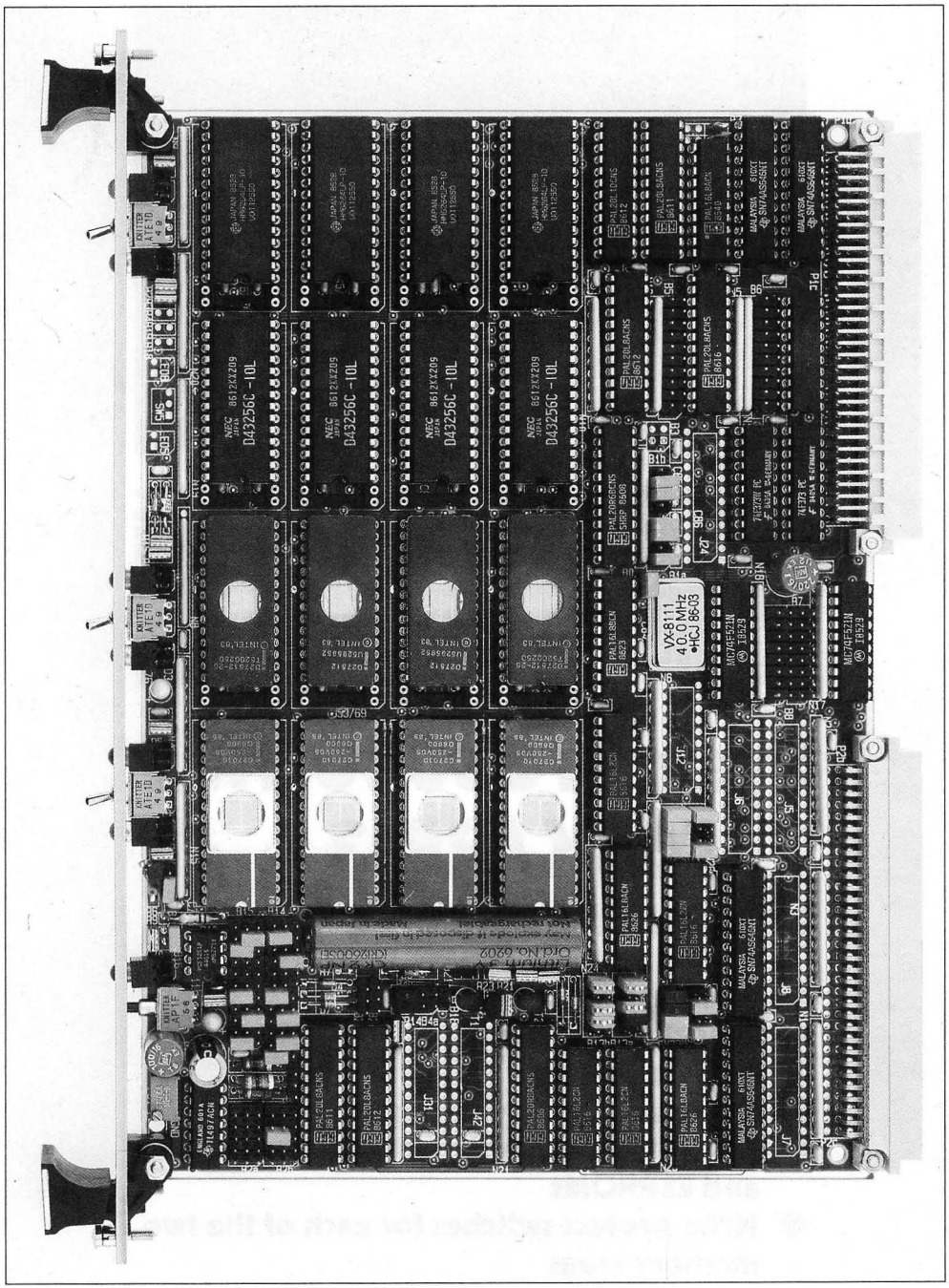
SYS68K/RR-2 Part No.200200	32 Bit RAM/ROM Board with VMEbus and VMXbus interface. Documentation included.
SYS68K/RR-2/UM Part No.800103	User's Manual of the SYS68K/RR-2



System 68000 VME SYS68K/RR-3

32 Bit RAM/ROM Board

- VMEbus Interface (A32:D32)
- 16 sockets for 28 and 32 pin JEDEC compatible devices
- On-board battery backup for static RAMs
- On-board programming logic for EPROMs and EEPROMs
- Write protect switches for each of the two memory areas



General Description

The SYS68K/RR-3 board is a high speed 32 bit memory board using up to 16 JEDEC compatible devices. The VMEbus interface is capable of transferring 8, 16, 24 and 32 bit data according to the IEEE 1014 standard.

The RR-3 supports 8, 16, 32 bit and unaligned transfers from the VMEbus. Read-Modify-Write cycles for multi-processor synchronisation are also supported. The VMEbus interface can be enabled or disabled via a switch installed on the front panel.

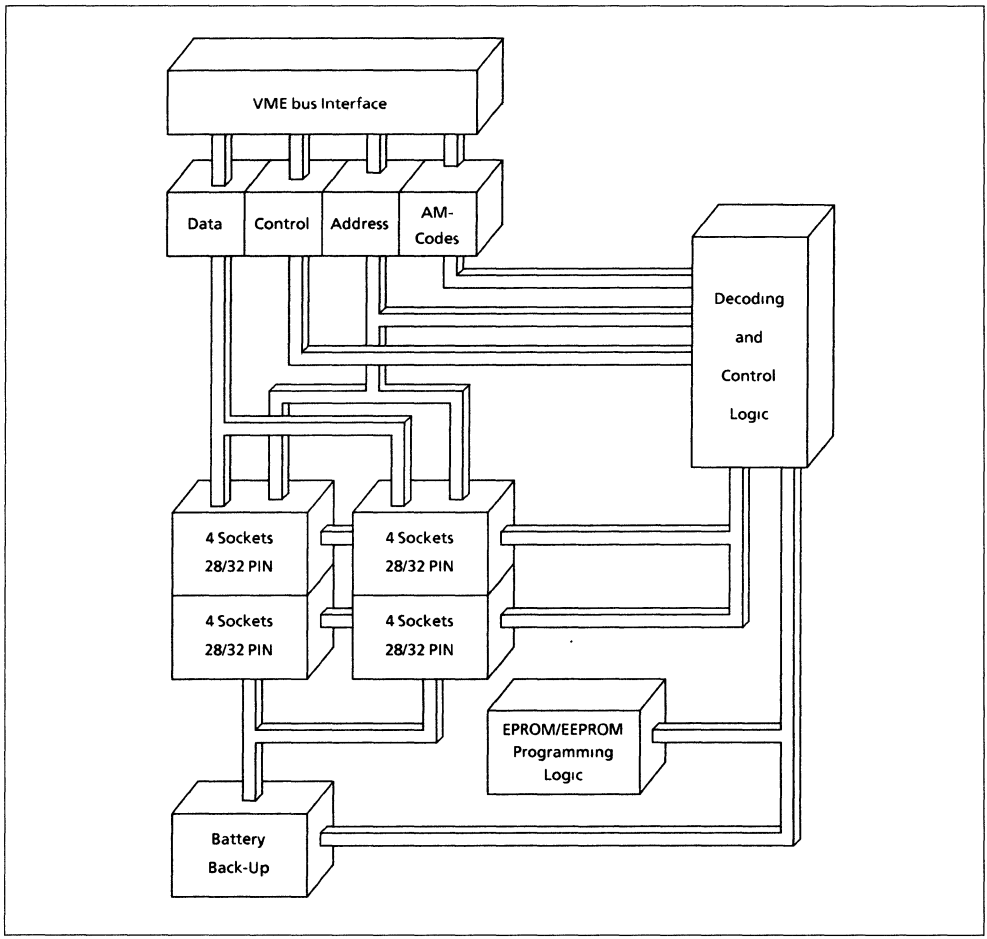
Both the 28 pin and the 32 pin standard for SRAMs, EPROMs and EEPROMs are supported to offer a maximum EPROM capacity of 2 Mbyte if the 128K x 8 devices are used. Two different memory areas, each consisting of 8 sockets are installed on the board to allow mixing of device types (i.e. one SRAM and one EPROM area).

Each memory area has a jumper selectable access address in device dependent boundaries and a set of selectable address modifier codes. The access time for each memory area is jumper selectable to adapt to the access times of the used devices.

A battery back-up with a voltage sensor is installed on the RR-3 to allow data retention for SRAM devices for up to 1 year.

To maintain reprogramming of data in special applications, the RR-3 contains hardware logic to program EPROMs and EEPROMs.

BLOCK DIAGRAM OF THE SYS68K/RR-3



Features of the SYS68K/RR-3

- IEEE 1014 interface supporting 32 data and 32 address lines.
- Jumper selectable access address and address modifier code.
- 16 sockets for JEDEC compatible devices using the 28 or 32 pin standard.
- 2 independent memory areas each consisting of 8 devices.
- Typical Access Times using 100ns devices: Write 70 ns, Read 200 ns
- Battery back-up for static RAMs.
- Programming of EEPROMs and Chip Erase function switch.
- Programming of EPROMs (21V and 12V types).
- Write protect switch for each of the two memory areas.
- RUN/LOCAL switch for the VMEbus.
- Jumper selectable access address and address modifier code for each of the two memory areas.
- Status and Access indication LEDs.

1.0 Functional Description

Two different memory areas, each consisting of 8 sockets are accessible via the VMEbus interface. Each provides for global memory such as static RAM, EPROM or EEPROM.
The Read-Modify-Write cycles from the VMEbus interface are supported to provide multi-processor synchronisation.
A Write Protection switch for each memory area installed on the front panel allows the protection of the memory area against non privileged modification.
EPROMs and EEPROMs can be programmed via special on-board hardware logic which makes a PROM programmer obsolete for most of the rommable software development packages. The EPROM programming feature of the RR-2 is supported under the Real Time Multi User Multitasking Operating System PDOS*.
Further details of the board features are described in the following paragraphs.

1.1 The VMEbus Interface

The RR-3 contains a full 32 bit interface providing highest data throughput. A RUN/LOCAL switch can disable the VMEbus interface.
On Write cycles, the 32 bit data and address are latched and a DTACK will be generated immediately if this operation is completed, and if the Write Protection is not activated for the addressed memory area.
The internal Write cycle starts in parallel and will be executed depending on the selected access time of the used devices.

Write:	80 ns
Read:	210 ns (using 100ns SRAMs)
	310 ns (using 200ns EPROMs)

All listed times are the maximum response times.
The access address of the two independent memory areas is jumper selectable in device dependent steps.
The unaligned transfers, defined in the VMEbus specification are fully supported to take advantage of the 68020 data bus handling.
Data Transfer Modes:

A32:	D32, D32NA, D16, D8
A24:	D32, D32NA, D16, D8

The maximum data transfer speed over the VMEbus is 16 Mbyte/s using 100ns SRAM devices.

1.2 Access Address Selection

Each of the two memory areas provides an individual selectable access address which is device capacity dependent. The address modifier code can also be selected for each memory area.
The access address which is compared depends on the selected address modifier code. The hardware logic of the RR-2 automatically detects if A24 or A32 decoding is selected (Extended or Standard addressing).
Each of the 8 defined AM-codes can be separately enabled or disabled via jumper settings.

1.3 Use of EPROM Devices

The RR-3 is designed to support 28 and 32 pin JEDEC compatible devices.
16 sockets each consisting of 32 pins are installed on the RR-3 to support the following device types:

Device	Organisation	No of PINs Used	Total Capacity
2764	8 K x 8	28	128 Kbyte
27128	16 K x 8	28	256 Kbyte
27256	32 K x 8	28	512 Kbyte
27512	64 K x 8	28	1 Mbyte
271024	128 K x 8	32	2 Mbyte
TBD	256 K x 8	32	4 Mbyte
TBD	512 K x 8	32	8 Mbyte
TBD	1 M x 8	32	16 Mbyte

The remaining 3 pins of the 32 pin socket can be adapted to accept EPROMs with a capacity of up to 1 Mbyte per chip which then results into a total capacity of 16 Mbyte if the chips become available.
Each memory area can be equipped with different device types allowing the insertion of SRAMs, EPROMs and EEPROMs at the user's discretion.
A Write Protect switch on the front panel protects SRAM, EPROM and EEPROM devices from writing because the RR-3 contains hardware logic to program EPROMs which have a programming voltage of 12.5 or 21V. The programming time (standard or intelligent algorithm) per cycle can be adapted to the used devices.

1.4 Use of EEPROM Devices

The RR-3 accepts EEPROM devices with at least 64K bit capacity (8K x 8 organisation). Logic to program EEPROMs is installed on the board to allow the modification of parameters during run time without exchanging the devices.
A chip erase switch is installed on the board to erase a maximum of 4 chips at a time (depending on the initiated data transfer which enables the chip erase function for the selected devices).
A Write Protect switch allows each memory bank to be protected against overwriting.
The following table lists all supported devices and the total capacity if all sockets are fitted with identical devices.

Device Type	Organisation	No of PINs Used	Total Capacity
58064,2864, 5233	8 K x 8	28	128 Kbyte
TBD	32 K x 8	28	512 Kbyte
TBD	64 K x 8	32	1 Mbyte
TBD	128 K x 8	32	2 Mbyte
TBD	256 K x 8	32	4 Mbyte
TBD	512 K x 8	32	8 Mbyte

1.5 Use of SRAM Devices

The RR-3 contains 16 sockets which may be used for static RAM insertion. The standard pin assignments for 8K x 8 and 32K x 8 devices is supported, resulting into a capacity of 128 or 512 Kbyte.
Expansion of the memory capacity is provided by using 32 pin devices.
The following table lists the supported devices and the future extention:

Device Type	Organisation	No of PINs Used	Total Capacity
6264	8 K x 8	28	128 Kbyte
62256	32 K x 8	28	512 Kbyte
TBD	128 K x 8	32	2 Mbyte
TBD	512 K x 8	32	8 Mbyte

An on-board lithium battery and a voltage sensor provide battery back-up of "low power" specified SRAMs (CMOS) of up to 1 year (SRAM dependent).
The on-board logic can be adjusted to the access time of the SRAMs to support various devices and optimize data throughput to the VMEbus and VMXbus interface.

Specification of the SYS68K/RR-3

VMEbus Interface:	IEEE 1014 standard compatible. Read-Modify-Write and Unaligned transfers supported. A32: D32, D32NA, D16, D8 A24: D32, D32NA, D16, D8 Independent Address and Address Modifier Decoding for each of the 2 memory areas. RUN/LOCAL switch disabling VMEbus accesses.
Sockets:	16 sockets for 28 or 32 pin devices (JEDEC Compatible pin out)
Memory Space:	EPROM: 28 pin devices 1 Mbyte (max) 32 pin devices 16 Mbyte (max) EEPROM: 28 pin devices 512 Kbyte (max) 32 pin devices 8 Mbyte (max) SRAM: 28 pin devices 512 Kbyte (max) 32 pin devices 8 Mbyte (max)
Access Times:	The access time of the board can be adapted to the speed of the used devices between 75 and 475ns in 25ns steps. Write 50 ns MIN 80 ns MAX Read 180 ns MIN 210 ns MAX
Special Functions:	EPROM programming function for +12V and +21V devices included. EEPROM programming function for +5V devices included. Chip Erase switch for EEPROMs included. SRAM battery back up for up to 1 year data retention with onboard lithium battery. Write Protect switches for each of the two independent memory areas. RUN/LOCAL switches for the VMEbus interface RUN/LOCAL, Access Protect and Chip Erase control LEDs for status monitoring installed on the front panel.
Power Requirements:	+ 5V : 2.9A +12V : 0.2A
Operating Temperature:	0 to 50 degrees C
Storage:	−50 to +85 degrees C (non operating)
Relative Humidity:	0–90% (non condensing)
Board Dimensions:	Double Eurocard 233 x 160 mm 9.2 x 6.3 inch

Ordering Information:

SYS68K/RR-3 Part No. 200600	RAM/ROM Board with 32 Bit VMEbus interface Documentation included.
SYS68K/RR-3/UM Part No. 800108	User's Manual of the SYS68K/RR-3

Controller Boards

FORCE Computers Mass Memory Controller Board Introduction

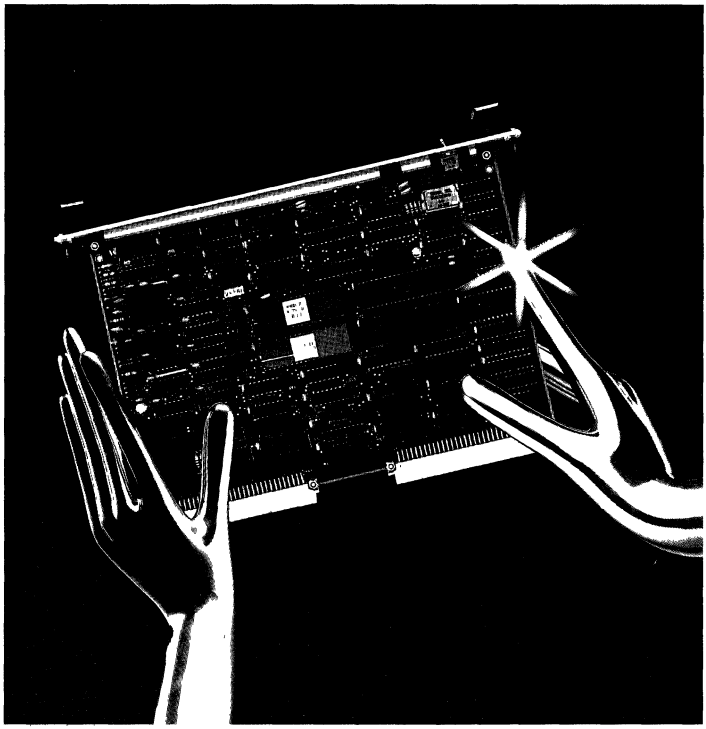
FORCE Computers range of VMEbus based boards includes a comprehensive selection of boards designed to match system requirements for mass (magnetic media) memory control. The family ranges from the non intelligent to the intelligent controller, controlling interfaces from ST506 to SCSI.

General Feature Overview

For medium performance and flexibility, the SYS68K/WFC-1 card provides direct access to ST506 compatible winchester disk drives. Additionally an SA460 interface is provided to allow the direct connection of Shugart compatible floppy disk drives. Five connectors are provided for the connection of up to three Winchester drives and four floppy drives. The board additionally provides the facility for ECC buffer control via the WD1014 in order to ensure data integrity. The WFC-1 is the low cost performance solution.
If top end performance is required without employing specialist product, then the SYS68K/ISCSI-1 or the SYS68K/ISCSI-1A controller card may be the solution to your application needs. This family of boards provides an intelligent interface to the high speed SCSI bus. Intelligence is provided via the on board 68010 (10 MHz) CPU and the installed firmware which supports not only the user interface but also hashing and cashing algorithms to increase performance. Data rates of up to 1.5 Mbyte per second are supported across the SCSI bus under the control of the on board DMA controller. Maximum performance is guaranteed from the 68010 due to 0 wait state access to the on-board dual ported RAM, 128 Kbyte on the ISCSI-1 and 512 Kbyte on the ISCSI-1A. The ISCSI-1(A) is the general purpose high performance mass media interface standard.

Mass Memory Controllers

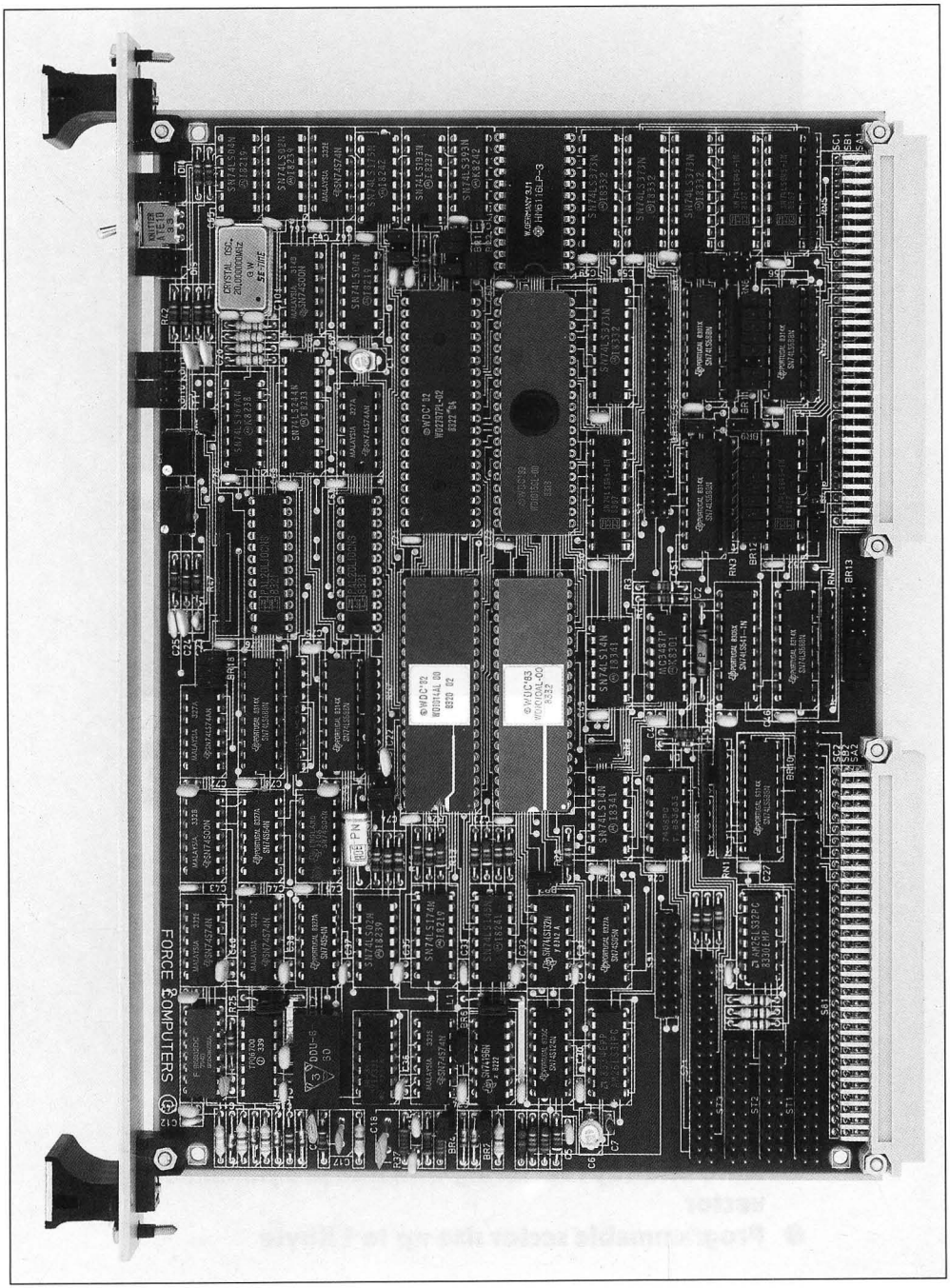
FAMILY	SASI-1	WFC-1	ISCSI-1	ISCSI-1A
Mass Memory Interface	Not recommended for new designs.	ST 506/SA 460	SCSI/SA 460	SCSI/SA 460
Maximum Disk Data Transfer Rate Synchronous Asyhchronous		ST 506 0.62 Mbyte/s –	SCSI – 1.5 Mbyte/s	SCSI – 1.5 Mbyte/s
VMEbus Interface		8 bit	16 bit	16 bit
Dual Ported RAM Capacity		– –	yes 128 Kbyte	yes 512 Kbyte
DMA to VMEbus Transfer Rate		no –	no –	no –
Local Processor Frequency		– –	68010 10 MHz	68010 10 MHz
No. of Supported Disks		3 x Winchester 4 x Floppy	8 (SCSI) 4 x Floppy	8 (SCSI) 4 x Floppy
Driver/Receiver Circuits on Board		yes	yes	yes
No. of different Interrupts to VMEbus		2	4	4
Detailed Description on Page:		295	301	301



System 68000 VME SYS68K/WFC-1

Winchester/Floppy Controller

- Controls up to three $5^1/_4$" Winchesters
- Controls up to four $5^1/_4$" Floppies
- Fully VMEbus compatible (A32:D16/A24:D16)
- Generation of two different interrupts with free jumper selectable interrupt level (1–7)
- Auto interrupt vectoring with free programmable vector
- Programmable sector size up to 1 Kbyte


FORCE COMPUTERS

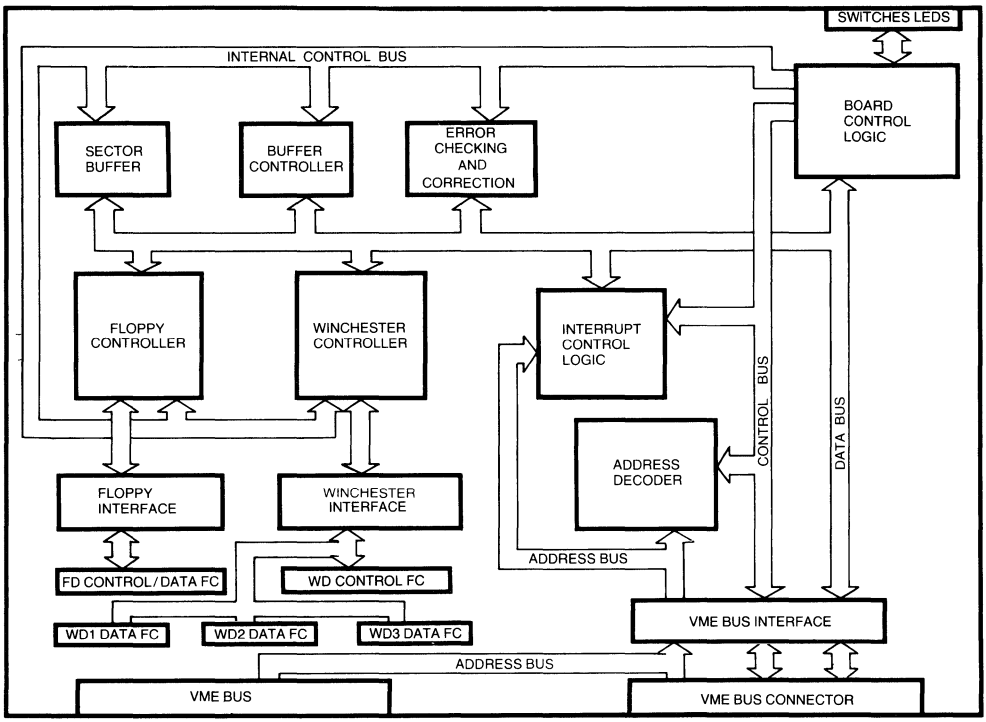
General Description

The SYS68K/WFC-1 board is a low cost controller board based on the VMEbus. It contains a Winchester controller, a Floppy controller, a sector buffer (1 Kbyte), and an ECC diagnostic processor. The SYS68K/WFC-1 board is able to generate an interrupt to the VME bus (levels 1-7) and to drive two different software programmable auto interrupt vectors.
The interface to the Floppies is Shugart compatible and the interface to the Winchester is ST506 compatible.

SYS68K/WFC-1 Features

- Controls up to three 5 1/4" Winchesters
- Controls up to four 5 1/4" Floppies
- Fully VME bus compatible (A32:D16/A24:D16)
- Generation of two different interrupts with free jumper selectable interrupt level (1-7)
- Auto interrupt vectoring with free programmable vector
- Free selectable access address including address modifier
- Programmable sector size up to 1 Kbyte
- Automatic track formatting on hard disk
- Up to 5M bit/sec data transfer rate
- 5 bit single burst error correction
- Five easy to use macro commands
- RUN/LOCAL switch
- LED indicators for RUN/LOCAL, ERROR and BUSY information

BLOCK DIAGRAM OF THE SYS68K/WFC-1



Functional Description

The SYS68K/WFC-1 board can control Floppies and Winchesters depending on the loaded command register and on several other powerful registers. The SYS68K/WFC-1 contains 8 registers and a FIFO buffer (First In First Out) for stored data. An interrupt can be generated by the SYS68K/WFC-1 at the end of command or at data request depending on the loaded command in this case, the interrupt vector has to be loaded before entering a command. The SYS68K/WFC-1 executes five easy to use macro commands:

- Restore
- Seek
- Read Sector
- Write Sector
- Format Track

Commands are executed by loading the command byte into the command register while the controller is not busy.

The RUN/LOCAL switch isolates the board from the bus during failures or maintenance. This mode is indicated by two LED's on the front panel.

The interface for the Winchesters is ST506 compatible (Seagate) and the interface for Floppies is Shugart compatible. All necessary drivers/receivers and buffers are on-board.

All I/O signals of the Floppy and Winchester interface are also connected to the P2 connector. The optionally available SYS68K/WFC-1BP board can be used to connect all the interface cables on the back of the motherboard.

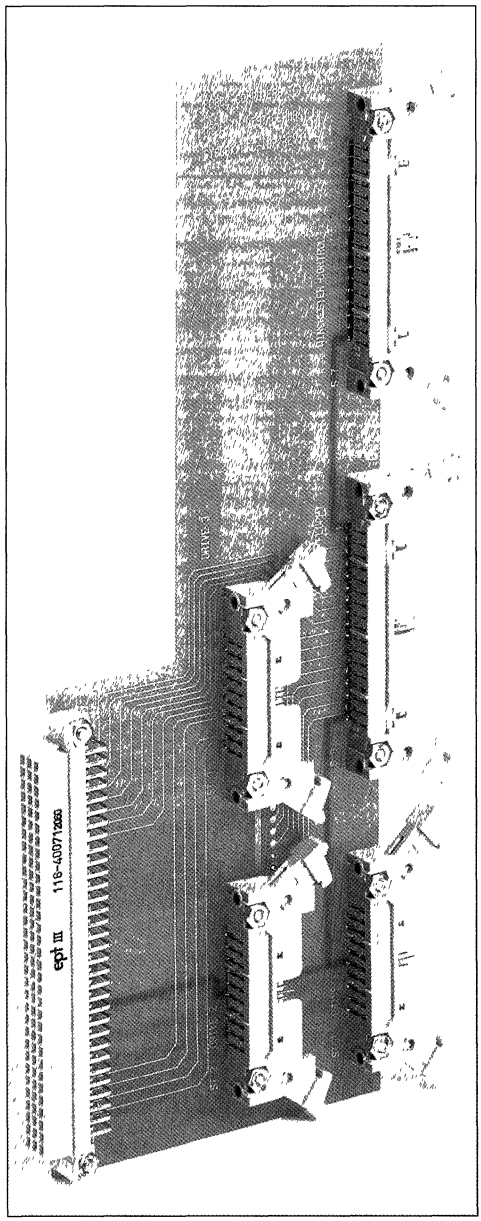
The WFC-1BP board fits directly into the P2 I/O connector of the motherboard and contains two 34 pin and three 20 pin connectors with ejectors. Therefore the WFC-1 board can be removed without disconnecting the interface cables of the disk drives.

Five connectors are provided for connection of up to three Winchester and four Floppy drives. All signals to the Floppies are placed on one 34 pin male connector where a flat cable can be plugged in and all signals are daisy chained.

The Winchester control lines are available on one 34 pin male connector. They are also daisy chained and require similar termination.

The data cables on the Winchester are radially connected to each drive via three 20 pin flat cables.

Photo of the SYS68K/WFC-1BP



Specification

Interface	ST506 for 51/4" Winchester drives SA460 for 5 1/4" Floppy drives
Devices	Floppy controller Winchester controller ECC/Buffer controller
Interrupt	Free selectable interrupt level Two differnt interrupt vectors
Bus	VME bus compatible (A32:D16/A24:D16) Free selectable board base address and address modifier code (AM0–AM5)
Power Requirements	+5V/3.0A max.
Operating Temperature	0 to +50 degrees C
Storage Temperature	−50 to +90 degrees C
Drive Cable Length	3 meters max.
Board Dimensions	Double Eurocard 234 x 160 mm (9.2x6.3 inch)

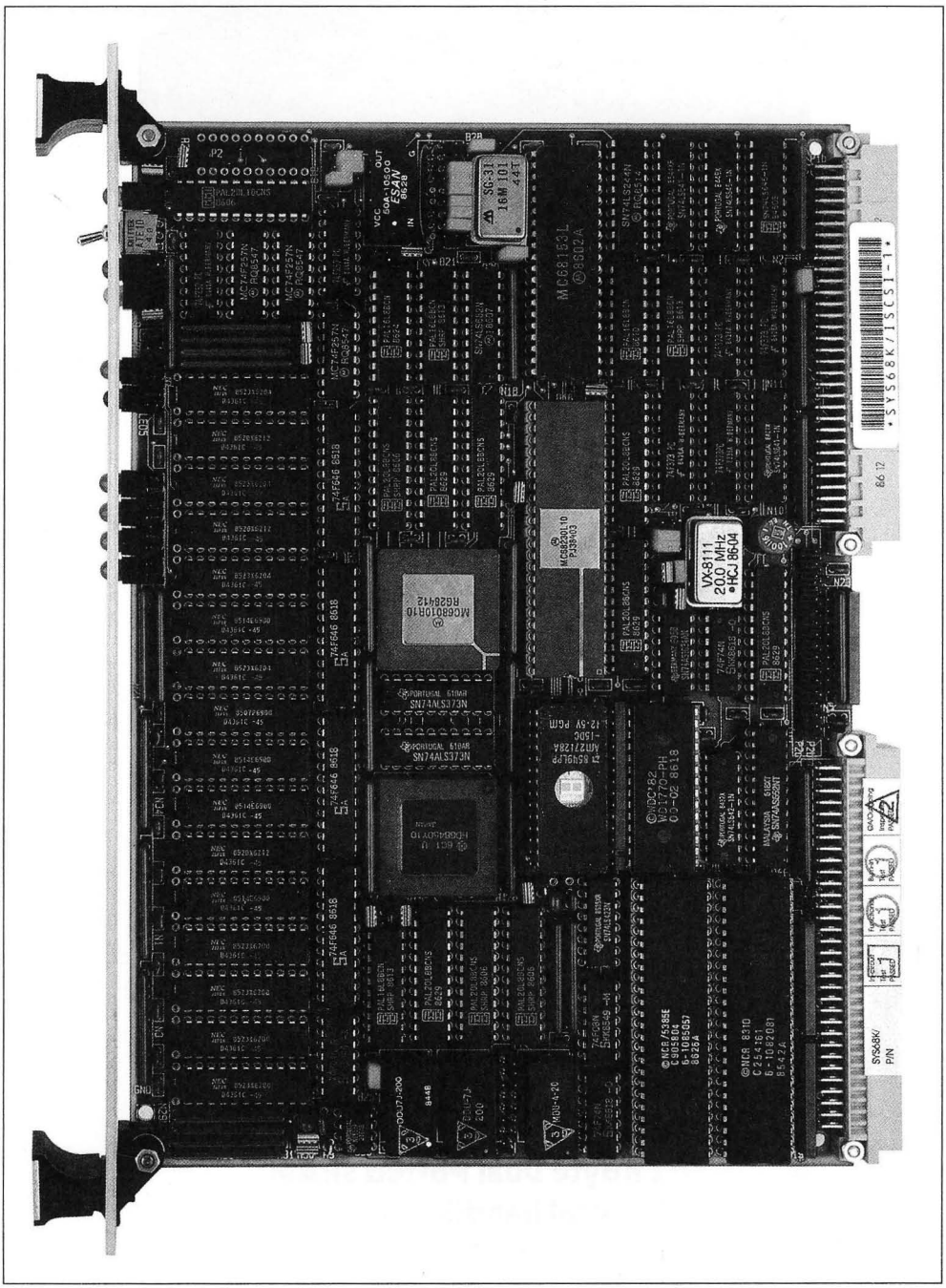
Ordering Information:

SYS68K/WFC-1 Part No. 300001	Winchester Floppy Controller Board including documentation
SYS68K/WFC-1BP Part No. 300002	Back Panel for the WFC-1 Controller Board
SYS68K/WFC-1/UM Part No. 800009	User's Manual for the WFC-1 and WFC-1BP Board

System 68000 VME SYS68K/ISCSI-1/1A

Intelligent Mass Memory Controller Board

- SCSI and Floppy Controller
- Fully SCSIbus and VMEbus IEEE 1014 compatible
- 128/512 Kbyte Dual Ported SRAM
- 68010 for local handling and control
- Powerful handling firmware

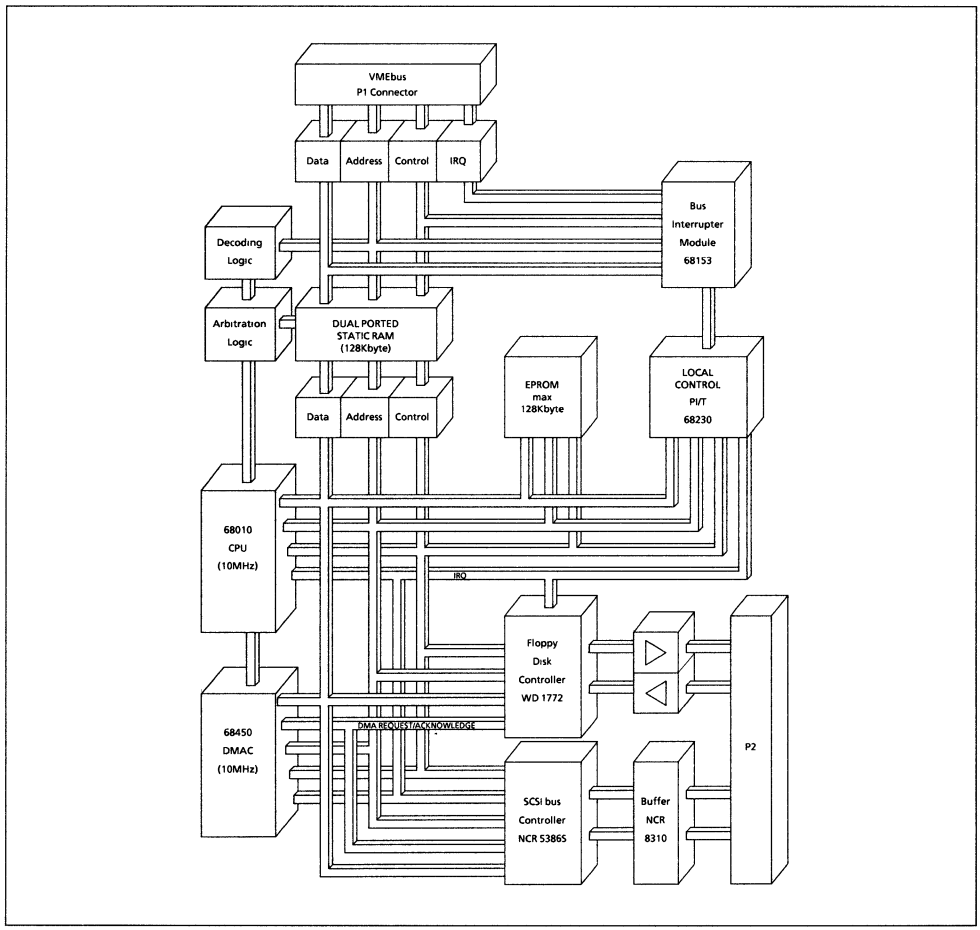

SYS68K/ISCSI-1*
SYS68K/
P/N

General Description

The SYS68K/ISCSI-1/1A is a high performance intelligent mass memory controller board, providing local intelligence with a 68010 CPU and a high speed DMA Controller. The DMA Controller is coupled with the ISCSI controller and the on-board floppy disk controller to optimize data throughput to/from the ISCSI bus and the floppy disk.
512 Kbyte of Dual Ported RAM on the ISCSI-1A or 128 Kbyte of Dual Ported RAM on the ISCSI-1 are used to store commands and data. Highest throughput in the 68010 CPU and 68450 DMA Controller by using 10MHz clock frequency is provided by the arbitration mechanism of the Dual Ported RAM.

The DMA Controller and the CPU access the DPR constantly without any wait states, independent from all VMEbus accesses.
The ISCSI-1/1A controller board contains an NCR 5386S controller chip and an 8310 SCSI bus driver transceiver circuitry. The maximum asynchronous data transfer rate is 1.5 Mbyte per second to/from the SCSI bus via the DMA Controller.
The initiator and the target mode are supported on the ISCSI-1/1A board to offer a wide variety of applications. All the driver and receiver circuitries are installed on the board to provide direct P2 interfacing and easy installation into VMEbus environments.

BLOCK DIAGRAM OF THE SYS68K/ISCSI-1/1A



The on-board floppy disk controller (WD 1772) allows the connection of up to four 3", 3 1/2" and 5 1/4" drives.
The ISCSI-1/1A contains a VMEbus IEEE 1014 compatible interface to communicate to the host CPUs via the Dual Ported Memory. The access address and the address modifier code is jumper selectable. A Bus Interrupter Module (BIM 68153) is installed on the board to support fully asynchronous operation with the four different software programmable interrupt request channels.
The firmware of the ISCSI-1/1A board handles all activities to/from the SCSI bus and the floppy disk drives. A data hashing and cashing mechanism built into the on-board firmware allows effective transfers of data to/from the mass memory devices. The firmware includes copy commands, which allow effective data transfers to/from connected devices without using the VMEbus for the data transfers. For example, a copy from a Winchester disk to a connected streamer is handled fully locally without any interaction from the host CPU.

2.0 Features of the SYS68K/ISCSI-1/1A

- 68010 CPU for local control (10MHz).
- 68450 DMA Controller (10MHz) connected to the SCSI bus controller and the floppy disk controller.
- Dual Ported 512 Kbyte 0 wait state static RAM between the VMEbus and the local CPU/DMA Controller. (ISCSI-1A)
- Dual Ported 128 Kbyte 0 wait state static RAM between the VMEbus and the local CPU/DMA Controller. (ISCSI-1)
- SCSI bus interface built with the NCR 5386S SCSI bus controller programmable as initiator or target. Data transfer rate on the SCSI bus is as high as 1.5 Mbyte per second.
- Shugart compatible floppy interface with a WD 1772 floppy disk controller for connection of up to 4 floppy disk drives.
- All SCSI bus interface and floppy disk interface signals are available on the P2 connector.
- Four different interrupt request channels to the VMEbus. Each channel contains a software programmable IRQ level (1-7) and vector.
- Local parallel interface for controlling and monitoring board functions.
- VMEbus IEEE 1014 compatible slave interface (A24:D16, D8).
- Watchdog timer controlling correct functions of on-board hardware and software.
- Status and control LEDs for monitoring local activities.
- High level handling firmware for communication, selftest, data cashing/hashing and control.

3.0 The Hardware Functions

The local CPU reacts on the commands and initialization parameters within the Dual Ported RAM. Constant run times are guaranteed through the special hardware logic, providing zero wait state operation from the Dual Ported RAM, independent from the accesses from the VMEbus to the Dual Ported RAM.
The ISCSI-1/1A consists of selftest functions as well as of a hardware watchdog timer which controls the activities of the 68010 CPU and the 68450 DMA Controller running with 10MHz clock frequency.
User-supplied programs can be loaded into the Dual Ported RAM and executed from the local CPU to adapt and extend board functionality. The local CPU controls the DMA Controller, SCSI bus controller and the floppy disk controller via local interrupts and communicates to the host CPU via the DPR and/or via interrupt requests to the VMEbus generated by a Bus Interrupt Module.
All I/O signals of the SCSI bus controller and the floppy disk controller are buffered and are available at the P2 connector of the board.

3.1 The Local 68010 CPU

A 10MHz 68010 CPU is installed on the ISCSI-1/1A to control the data traffic between the SCSI bus controller, floppy disk controller and the VMEbus for the host CPU(s). 2 EPROMs with a maximum capacity of 128 Kbyte are installed on the ISCSI-1 to contain the handling firmware. Constant zero wait state operation from the EPROM guarantees maximum CPU throughput and a fixed program run time. The 128 Kbyte of Dual Ported RAM is also accessible without the insertion of wait states by using a CPU clock synchronized arbitration mechanism. The accesses from the CPU to the DPR are not delayed if a VMEbus access is pending or being executed. A local timer included in the PI/T is used to interrupt the CPU for task scheduling, command interpretation and execution.
The CPU and all I/O devices can be reset through a system reset via the SYSRESET* signal of the VMEbus, or by accessing a dedicated location within the DPR reserved for this function.

3.2 The 68450 DMAC

The ISCSI-1/1A contains a 4 channel DMA Controller (68450) with a clock frequency of 10 MHz. The DMA Controller is connected to the floppy disk controller and the SCSI bus controller to offer maximum data throughput to/from the mass memory devices.
The DMA Controller accesses the Dual Ported RAM constantly without the insertion of wait states. The DMA Controller transfers data from the device directly to the memory in a single cycle mode.

Special hardware logic on the board collects 2 x 8 bit of data and forces one 16 bit transfer to the Dual Ported RAM to enhance and optimize data throughput. This results in a maximum data throughput for the SCSI bus data transfers of 1.5 Mbyte per second.
The minimum guaranteed data transfer rate, including handshaking on the SCSI bus is 1.25 Mbyte per second if an appropriate SCSI bus data transfer rate of the mass memory device is provided.

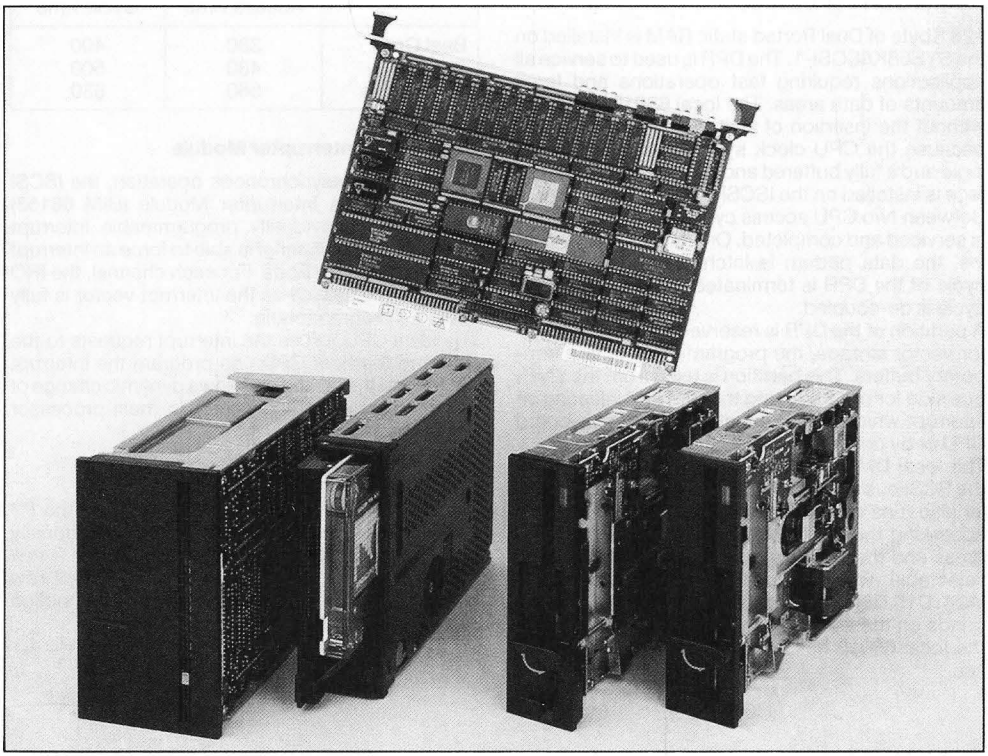
3.3 The SCSI Bus Controller

The SYS68K/ISCSI-1/1A contains an NCR 5386S SCSI bus controller chip and an NCR 5310 SCSI bus driver/transceiver. The 8386S controller is directly connected to the on-board DMA Controller to transport the incoming/outgoing data via the DMA Controller to/from the Dual Ported RAM. The data transfer rate through the DMA Controller on the SCSI bus is 1.5 Mbyte per second.
The initiator and the target mode of the SCSI bus specification are fully supported with the controller and the on-board firmware. Parity generation and check are automatically handled inside the controller, to guarantee maximum data integrity.

The installation of the 8310 SCSI bus driver/receiver circuitry allows easy adaption and installation in a VMEbus rack because all I/O signals are available on the P2 connector and fully buffered with 48 mA drivers (single ended version).

3.4 The Floppy Disk Controller

The ISCSI-1/1A board contains a WD 1772 floppy disk controller to directly control 3", 3 1/2" and 5 1/4" floppy disk drives. All the driver and receiver circuitries are installed on the board and the I/O signals are available on the P2 connector for easy interfacing.
The floppy disk controller data bus is directly connected to the DMA Controller allowing highest throughput from the floppy disk to the Dual Ported Memory. The single chip floppy disk controller includes all the phase locked loop and data separation without the need for adjustments and adaptions.
The floppy disk controller WD 1772 is able to control single and double density floppy disk drives (single or double sided). The selection of each mode is made via the local PI/T.



3.5 The PI/T 68230

A 68230 Parallel Interface and Timer chip is installed on the SYS68K/ISCSI-1/1A to control and display the status of all on-board activities. The PI/T is also used to force and monitor the interrupt request lines to the Bus Interrupter Module which initiates the interrupts to the VMEbus under control of the host CPU.
One handshake pin is used to interrupt the local CPU if the host CPU accesses a defined location within the DPR. One output signal is used to force a SYSFAIL signal to the VMEbus if an on-board failure has been detected or if the board initializes the DPR after RESET or power up. The timer also included in the PI/T is the time base for the on-board handling firmware and the scheduler for handling the macro commands.
A watchdog timer for processor control is installed on the board to detect software or hardware errors independent from the on-board CPU. The SCSI bus RESET signal is controlled from the local PI/T. One input of the PI/T indicates the state of the SCSI bus RESET and one output can be used to force an SCSI bus reset.

3.6 The Dual Ported RAM

128 Kbyte of Dual Ported static RAM is installed on the SYS68K/ISCSI-1. The DPR is used to service all applications requiring fast operations and large amounts of data areas. The local 68010 CPU runs without the insertion of wait states from the DPR because the CPU clock synchronized arbitration logic and a fully buffered and latched VMEbus interface is installed on the ISCSI-1/1A.
Between two CPU access cycles, a VMEbus cycle is serviced and completed. On VMEbus READ cycles, the data pattern is latched and the internal cycle of the DPR is terminated while the VMEbus cycle is de-coupled.
A partition of the DPR is reserved for the local CPU for vector storage, the program counter and temporary buffers. This partition is used from the VMEbus side for programming the BIM and initiating an interrupt which will be handled from the on-board CPU or by driving a local RESET.
The local DMA Controller, which is connected to the SCSI bus controller and the floppy disk controller also runs without the insertion of wait states by accessing the Dual Ported RAM. The access address and the Address Modifier codes are jumper selectable within the standard address range (A24:D16,D8). The access times of the DPR depends on the accesses made by the local CPU as the local 68010 has priority over VMEbus accesses.

3.7 The VMEbus Interface

A fully VMEbus IEEE 1014 compatible interface is installed on the SYS68K/ISCSI-1/1A to allow an access to the DPR and the Bus Interrupter Module. The 16-bit data width (D16, D8) of the DPR and the decoding of the standard address range (A24) allows easy installation in all VMEbus environments.
During power up and after RESET has been executed from the local CPU, the ISCSI drives the VMEbus signal SYSFAIL active to signal each board in the VMEbus environment that the board is not ready or has detected a malfunction.
A RESET for the local CPU can be initiated by accessing a dedicated address within the DPR. All local devices as well as the CPU will be reset through this access.
An interrupt to the local CPU can be forced by accessing another location within the DPR, signalling the on-board processor that a command has been given, or that an exception has to be taken.
The Dual Ported RAM can be accessed at least every 640ns because this is the worst case cycle time. The data transfer rate to/from the ISCSI-1/1A is 3 to 4 Mbyte/s including the VMEbus protocol.

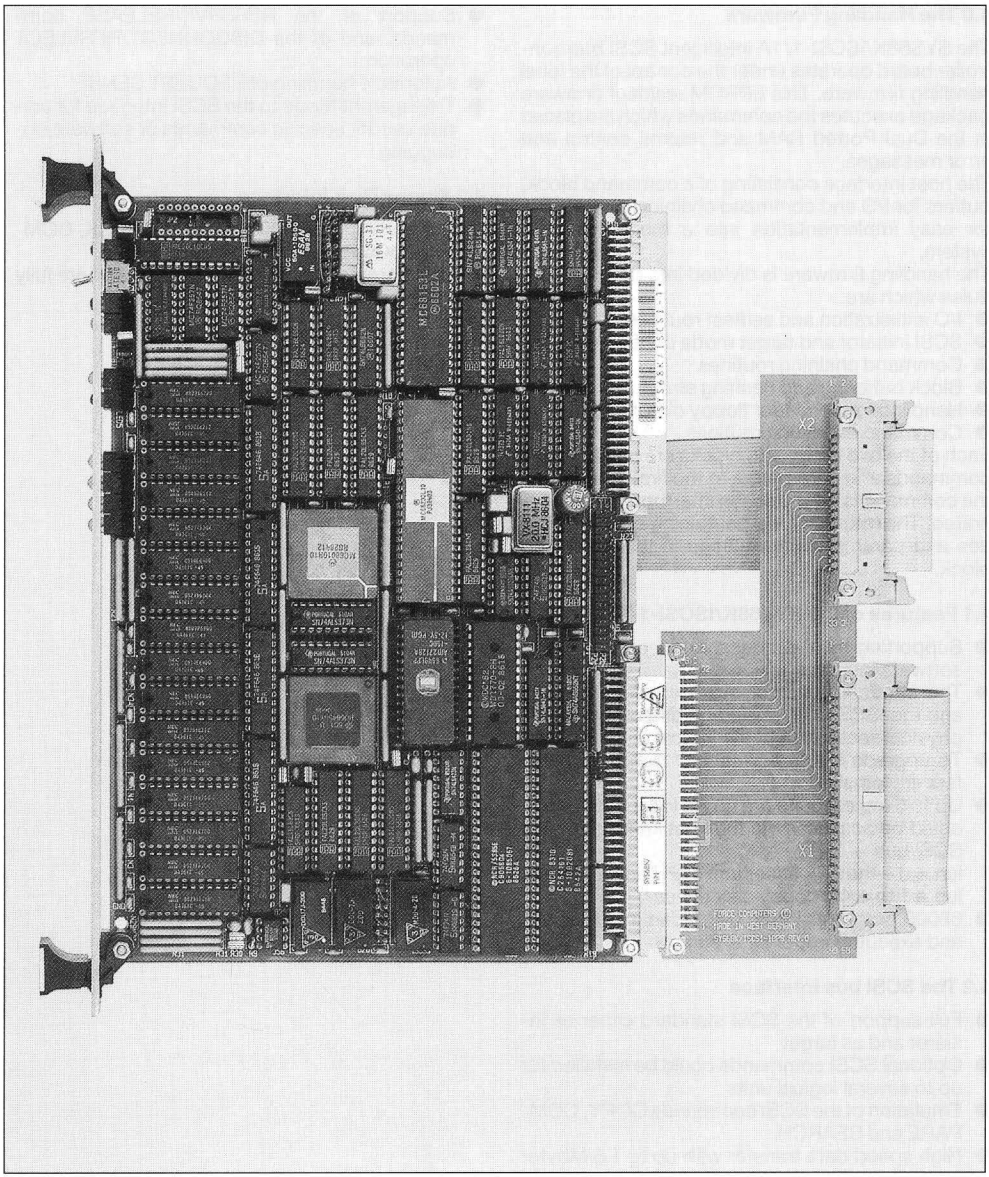
	Access Time	Cycle Time
Best Case	330	400
Average	430	500
Worst Case	560	630

3.8 The Bus Interrupter Module

To allow fully asynchronous operation, the ISCSI contains a Bus Interrupter Module (BIM 68153) providing 4 individually programmable interrupt channels. Each channel is able to force an interrupt request to the VMEbus. For each channel, the IRQ level (1 to 7) as well as the interrupt vector is fully software programmable.
The local CPU forces the interrupt requests to the BIM and the host CPU can program the interrupt vector and the level. This allows dynamic change of the interrupt level and vector in multi-processor environments.

3.9 The Optional Back Panel

A back panel which can be plugged into the P2 connector of the ISCSI-1/1A board is optionally available. Included on this board is a 50-pin 2-row connector for the SCSI bus and a 34-pin 2-row connector for the floppy disk for direct connection of a flat cable.


X2
X1

4.0 The Handling Firmware

The SYS68K/ISCSI-1/1A intelligent SCSI bus controller board operates under the control of the local handling firmware. This EPROM resident firmware package executes the commands which are placed in the Dual Ported RAM and returns control and error messages.
The host interface consisting of a command block, buffers for I/O and command chaining exists twice for easy implementation into a multi-processor system.
The handling firmware is divided into different modules which are:

- I/O initialization and selftest routines
- SCSI initiator and target mode control
- Command chaining routines
- Block buffering and hashing structures
- Handling for up to four floppy disk drives
- Command execution routines

Each of the two command blocks are used to pass commands and parameters to the firmware. When the command is executed, an interrupt can be generated. The return values, containing complete codes and parameters are placed in the command block.

4.1 Features of the SYS68K/ISCSI-1/1A

- Supporting multi-processor access via double software interface
- The interfacing sector size between the host and the ISCSI-1/1A could be different from the physical sector size of the logical units
- To upgrade the performance, 16 hashing buffers are installed
- Up to 5 logical units are under local control and could be accessed via the host interface or the SCSI bus
  lun #0 + the processor unit (CPU and DMAC)
  lun #1 to #4 = floppy disk drives
- 68000 programs could be loaded into the DPR and executed under local control

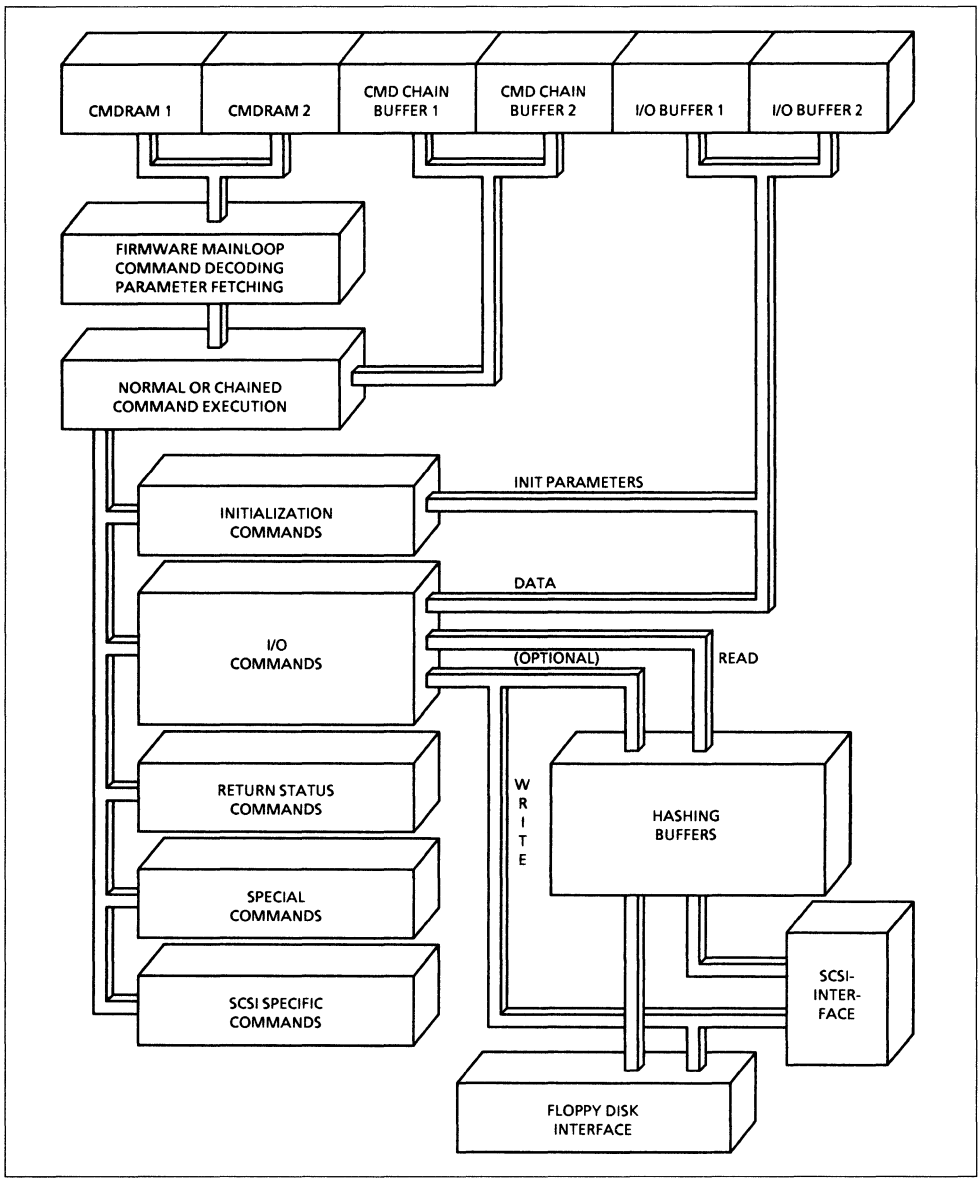
4.2 The SCSI bus Interface

- Full support of the SCSI standard either as initiator and as target
- Optional SCSI commands could be installed for up to several logical units
- Emulation of the SCSI commands COPY, COMPARE and SEARCH
- High speed data transfer with up to 1.5 Mbyte/second
- BACKUP command and automatic run time backup to a secondary unit
- Support of the RESERVE/RELEASE commands, and of the DISCONNECT/RESELECT operation
- Automatic handling of REQUEST SENSE
- Transparent Mode to the SCSI interface for unique vendor specific commands or software debugging

4.3 Floppy Disk Interface

- Supporting FORMAT, FORMAT TRACK, COMPARE, COPY and BACKUP commands
- Disk parameters and format interleaves are fully installable and changeable

LOGICAL BLOCK DIAGRAM OF THE ISCSI-1/1A FIRMWARE



5.0 The Command Set of the ISCSI-1/1A

5.1 Initialization Commands

- Setup of SCSI bus ID
- Configuration of the interfacing sector size between the ISCSI-1 and the host
- Installation of a logical unit (SCSI unit or a local floppy disk)
- Enable/disable block buffering for write operations
- Enable/disable routine backup to parallel logical unit
- Setup of address offset
- Software reset with selftest

5.2 I/O Commands

- Get one byte from logical block
- Write one byte to a logical block
- Read blocks from a logical unit
- Write blocks to a logical unit
- Get a delimited string from a logical block
- Write a delimited string to a logical block
- Get a counted string from a logical block
- Write a counted string to a logical block

5.3 Status Commands

- Return the current state of the controller board
- Check SCSI targets for existence and device type
- Return units parameter

5.4 Special Commands

- Execute user program within the DPR
- Execute command queue (chain mode)
- Backup a logical unit
- Flush all modified buffers
- Format a logical unit
- Format a track on a floppy disk
- Compare data between two logical units
- Lock local units against SCSI bus access
- Free local units for SCSI bus access
- Copy data from a logical unit to another or on the same unit
- Enter command chaining mode

5.5 SCSI Specific Commands

- Send a command to SCSI target (transparent mode)
- Enable/disable SCSI target mode
- Enable/disable automatic RESERVE/RELEASE unit

Specification of the SYS68K/ISCSI-1/1A

Local CPU	68010 CPU with 10 MHz Clock Frequency
Local DMA Controller	68450 DMAC with 10 MHz Clock Frequency
EPROM	128 Kbyte maximum capacity Constant No Wait State operation
Dual Ported RAM	512/128 Kbyte capacity using static RAMs No Wait State operation from local CPU and DMA Controller VMEbus access time best case – 330 ns VMEbus access time average case – 430 ns VMEbus access time worst case – 560 ns
SCSI bus	NCR 5386S SCSI bus controller and NCR 8310 SCSI bus driver/transceiver Initiator and Target Modes Supported All SCSI bus signals are available on the P2 connector
Floppy Disk Controller	WD 1772 Floppy Disk Controller supporting 3", 3.5", 5 1/4" disk drives on-board phase lock loop and data separation SA450 compatible interface available on the P2 connector
VMEbus Interface	Fully IEEE 1014 compatible slave interface A24:D16, D8 mode 4 IRQs with software programmable level (1-7) and vector Access address jumper selectable SYSFAIL supported
Handling Firmware	In EPROM with macro commands for all mass memory control
Power Requirements	+5V: 5.6A (max) (P2 backplane or power connection on P2 recommended)
Operating Temperature	0 to 50 Degrees C
Storage Temperature	–50 to +85 Degrees C (non-operating)
Relative Humidity	0 to 90% (non-condensing)
Dimensions	233 x 160mm 9.3" x 6.3"

Ordering Information

SYS68K/ISCSI-1 Part No. 300020	Intelligent SCSI/Floppy Disk Controller, 128 Kbyte Dual Ported RAM, with local DMA controller, including firmware and documentation.
SYS68K/ISCSI-1A Part No. 300023	Intelligent SCSI/Floppy Disk Controller, 512 Kbyte Dual Ported RAM, with DMA controller, including firmware and documentation.
SYS68K/ISCSI-1BPS Part No. 300021	Back panel for the ISCSI-1/1A board providing SCSI and floppy disk controller connectors.
SYS68K/ISCSI-1/UM Part No. 800114	User's Manual for the ISCSI-1/1A.

Graphics Controller Boards

FORCE Computers Graphics Controller Board Introduction

The family of FORCE Computers graphics cards covers all needs from low cost, medium performance graphics solutions to powerful high resolution graphics cards capable of simultaneously displaying 256 different colours.

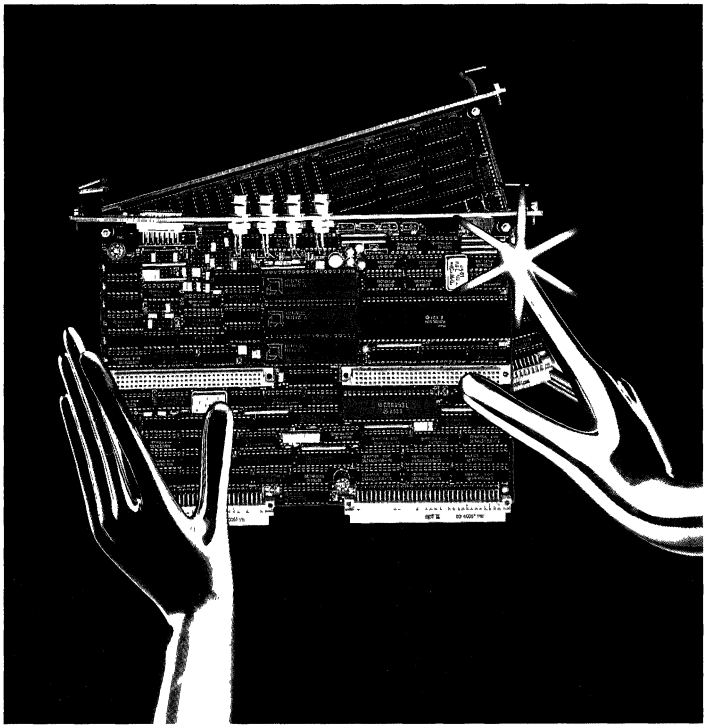
General Feature Overview

For top end graphics applications, the SYS68K/AGC-1 board offers all the advanced features that are made available with the 63484 ACRTC Advanced Colour Raster Tube Controller chip. The hardware fully implements the dual access mode of the chip which allows the fastest flicker free drawing. 2 Mbyte of dual ported RAM is installed on the board set as standard allowing resolutions of up to 1600 x 1280 to be displayed with 16 colours in interlaced mode. The optional SYS68K/AGC-1X board may also be installed in the subsystem. This provides a character generator, 4 serial ports and a full VMXbus interface. The SYS68K/AGC-1 board set is the high level graphics solution.
If you need the high level graphic solutions offered by the 63484 ACRTC but the comprehensive features offered by the AGC-1 family are more than you need, then maybe the SYS68K/AGC-2 will fit your specification. The board offers 1 Mbyte of video memory and the 63484 offering 4 bit/pixel graphical display at up to 1160 x 876 resolution. The AGC-2 is the low cost performance solution.

Graphics Controllers

FAMILY		CMC-1	GDC-1	AGC-1	AGC-1X	AGC-2
Resolution	50 Hz interlaced 50 Hz non-interlaced 60 Hz interlaced 60 Hz non-interlaced	Not recommended for new designs.	Not recommended for new designs.	1600 x 1280 1140 x 870 1280 x 1024 1024 x 800	– – – –	1160 x 870 800 x 600 1024 x 800 720 x 560
No. of different simultaneous displayable Colors Total No. of Colors				16 or 256 16 million	16 or 256 16 million	16 256 K
Used Controller Chip				63484	–	63484
Video RAM Capacity Local Intelligence via				2 Mbyte –	– –	1 Mbyte –
Interfaces:	Light Pen Serial I/O (RS232) Centronics			yes 0 no	no 4 no	yes 0 no
Smooth Scroll:	Horizontal Vertical Zoom			yes yes yes	yes yes yes	yes yes yes
Cursor:	Software Programmable Cross Hair Grid			yes no no	yes no no	yes yes yes
No. of different Screens Window Screens				3 1	– –	3 1
Character Generator:	RAM EPROM			– –	128 Kbyte 128 Kbyte	– –
No. of Boards				2	1	1
Special Features				– –	VMXbus DMAC	– –
Detailed Description on Page:				317	317	331

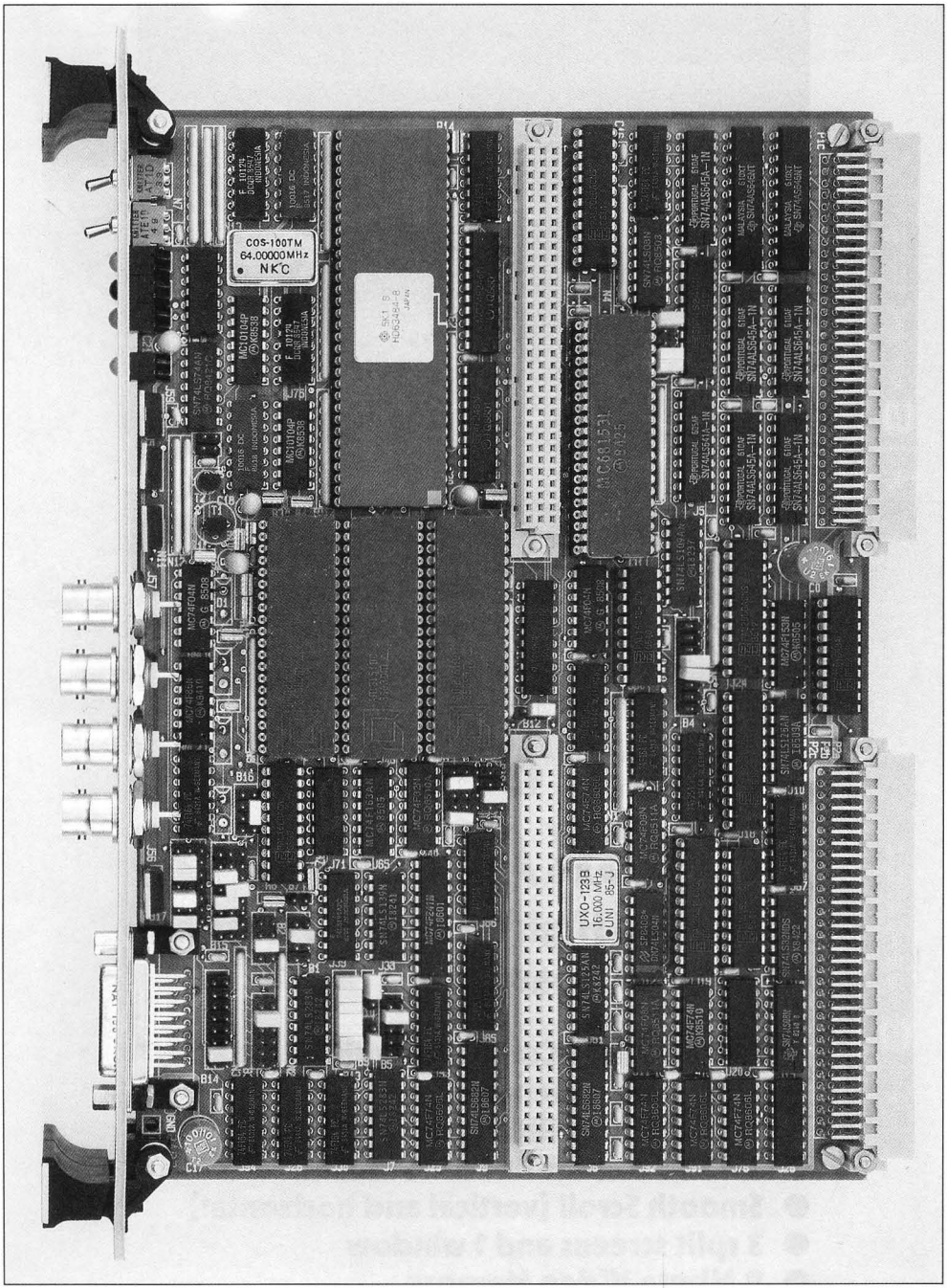
Note: The AGC-1X board can only be used in conjunction with the AGC-1



System 68000 VME SYS68K/AGC-1/1X

Advanced High Resolution Graphic Controller Board

- 63484 ACRTC Controller with Dual Access Mode implemented
- 1600x1280x4 Bit interlaced display format
- 16/256 colours out of 16 million
- Smooth Scroll (vertical and horizontal)
- 3 split screens and 1 window
- 2 Mbyte Video Memory


COS-100TM
64.00000MHz
NKC
UXO-129B
16.000 MHz
UNI 85-J

General Description

The SYS68K/AGC-1 is a high performance graphic system consisting of two double eurocard boards. It is based on the Advanced Colour Raster Tube Controller ACRTC-63484 and the VMEbus.

The maximum resolution to be displayed at 50 Hz is 1600 by 1280 pixel with 4 bit/pixel colour information and interlaced display mode.

Flicker-free display in the non-interlaced mode is provided by using the 1024 by 800 display format which provides 50 to 60 Hz frequency and 4 bit/pixel colour information. The pixel frequency of the RGB outputs is 32 MHz or 64 MHz depending on the colour information per pixel.

To provide maximum flexibility, 256 different colours out of 16 million can simultaneously be displayed at the maximum format of 800 by 600 pixels using the 50 Hz non-interlaced display mode.

The 2 Mbyte dual ported video RAM is accessible from the ACRTC and the VMEbus. The Dual Access Mode of the ACRTC is implemented for all display formats to enhance drawing speed.

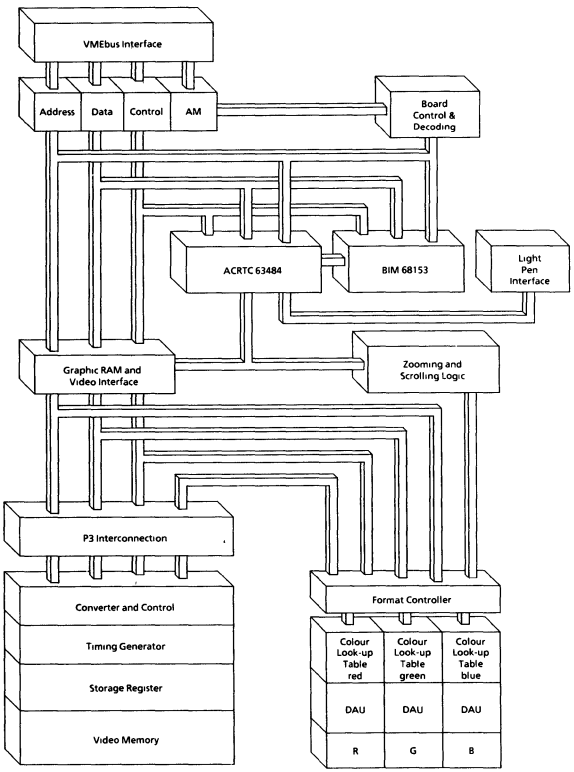
The VMEbus interface (IEEE 1014) contains a jumper selectable access address for the ACRTC and the Bus Interrupter Module (BIM 68153) as well as for the 2 Mbyte video RAM.

Three Advanced Graphic Colour Palettes (AM8151) are installed on the AGC-1 board set to select the 16 or 256 simultaneously displayable colours out of the whole set of 16 million colours.

Hardware zoom, vertical and horizontal smooth scroll, clipping, hitting, blinking and conditional blinking are additional features of the AGC-1 board set. These features are described briefly in the next paragraphs.

The world-wide Graphic Standard GKS is optionally available for the AGC-1 board set. Detailed information is outlined in the GKSGRAL datasheet in the software chapter of this data book.

BLOCK DIAGRAM OF THE SYS68K/AGC-1 BOARD SET



Features of the SYS68K/AGC-1

- ACRTC 63484 with a clock frequency of 8 MHz and 23 high level commands. Dual Access Mode implemented.
- High level graphic commands, such as LINE, RECTANGLE, POLYLINE, POLYGON, CIRCLE, ELLIPSE, PAINT, COPY etc.
- 2 Mbyte of dual ported RAM directly accessible from the VMEbus and through the ACRTC. Hardware refresh for the DRAMs implemented.
- R-G-B and composite SYNC outputs.
- Display formats:

Horizontal x vertical	Bit/ Pixel	Pixel Frequency	Frame Period	Mode
1600x1280	4	64 MHz	50 Hz	interlaced
800x 600	8	32 MHz	50 Hz	non-interlaced

- No "flashing" screen during draw cycles due to the implemented dual access mode.
- Pixelwise softscrolls (horizontal and vertical).
- 3 different screens with software programmable positions.
- 3 Graphic Colour Palettes provide 16 or 256 simultaneously displayable colours out of a palette of 16 million.
- Lightpen interface.
- VMEbus/IEEE 1014 standard
  A24: D16, D8
  A16: D16, D8
- Interrupter to VMEbus with software programmable IRQ level and vector.
- RUN/LOCAL switch to disable VMEbus accesses.
- Fully buffered local bus.
- Extension interface to the SYS68K/AGC-1X board.

1.0 Functional Description

The ACRTC 63484 receives the drawing commands from a CPU-board through the VMEbus interface. All address calculations to the video RAM are made internally to offload the CPU-board programs by using only x- and y-coordinates.
The controller chip automatically generates the timing to the screen after initialisation.
4 or 8 bit per pixel can be selected as display modes to provide 16 or 256 different colours to be displayed out of the complete range of 16 million colours.

A local interface connector between the AGC-1A and -1B board is installed in the middle of the boards to offload the P2 connector and leave it free for other bus interfaces.
Board A contains the ACRTC chip, the VMEbus interface and the colour lookup table including the D/A converters. All timing and control functions are installed on the A board, while the B board houses the dynamic RAMs and the shift registers.
The following paragraphs describe different functions on the AGC-1 board set.

1.1 The ACRTC 63484

The Advanced CRT Controller 63484 provides 38 commands including 23 graphic drawing commands. A 16 byte on-chip Read/Write FIFO reduces communication overhead of the CPU-board. Automatic conversion of the x-y coordinates to physical frame buffer addresses is provided through the on-chip drawing processor.
All timing parameters of the used monitor are software programmable and the ACRTC generates all the necessary timings to the R-G-B and SYNC outputs.
The controller also allows the use of up to 3 different screens (upper, lower and the base screen) plus one window screen.
The size and the position as well as the smooth scroll for each screen is software programmable. Special hardware logic is implemented on the AGC-1 to support the horizontal and vertical smooth scroll function. In addition, hardware logic provides the correct attributes for zooming (1..16).
The lightpen interface of the ACRTC is supported via the 15 pin D-sub connector available on the front panel.
The drawing speed of the ARCTC is at minimum 2 Mpixel/s because of implementation of the Dual Access Mode.
With the implementation of the Dual Access Mode, the ACRTC display and drawing accesses are interlaced, so the ACRTC reaches its maximum drawing speed without a "flashing" display during draw and read accesses.

1.2 The Video RAM

2 Mbyte of video RAM are installed on the AGC-1 board B supporting the whole addressing capability of the ACRTC chip. The video RAM enables the usage of multiple pictures to be held in the video memory (depending on the display size and the zoom factor).
Direct access from the VMEbus is provided through the VMEbus/IEEE 1014 interface. The transfers to/from the video memory cause no interference on the display.

The Dual Access Mode of the ACRTC chip is implemented on the AGC-1 to offer maximum drawing speed at 64 MHz pixel clock frequency. In the dual access mode, the ACRTC displays the pattern in the video RAM on the screen in the first cycle and draws in the next cycle. The 4 or 8 bits per cycle are modified in each draw cycle which minimizes drawing time.
The ACRTC chip provides the hardware refresh for the dynamic RAMs which uses 64 K x 4 organization.

1.3 The Colour Lookup Table

The AGC-1 board set contains 3 colour lookup tables (AM8151) including the digital to analogue converters to provide a total set of 16 million different colours. The two different display modes (4 or 8 bit per pixel) allow the display of 16 or 256 colours at one time, respectively.
The colour lookup tables are accessible through the VMEbus/IEEE 1014 interface and all entries are also readable.
The timing and control functions as well as the ECL voltage converters are installed on the AGC-1 board A so that no additional power supply for the –5V is needed.

1.6 Display Formats

The resolution to be displayed depends on the monitor parameters as well as on the AGC-1 hardware setups. The following table lists standard display formats which are supported from the AGC-1 hardware and which are tested with various monitors.
All display parameters as well as the number of bits per pixel are software programmable to offer maximum flexibility and minimize software overhead. An initialisation routine in menu technique (under PDOS), a programming example and a PDOS driver are optionally available.

1.7 The VMEbus Interface

A VMEbus IEEE 1014 standard compatible interface is installed on the AGC-1 board set. The access address and the address modifier code of the video RAM (2 Mbyte) are jumper selectable within the standard address range (A24:D16, D8). The ACRTC, the Bus Interrupter Module BIM 68153 as well as the colour lookup table are also accessible under the same address and AM-codes.
All address, data and control signals are latched and buffered the local bus.

Horizontal x vertical	Bit/Pixel	No. of Colours	Pixel Frequency	Frame Period	Mode
1600 x 1280	4	16	64 MHz	50 Hz	interlaced
1280 x 1024	4	16	64 MHz	60 Hz	interlaced
1140 x 870	4	16	64 MHz	50 Hz	non-interlaced
1024 x 800	4	16	64 MHz	60 Hz	non-interlaced
1160 x 870	8	256	32 MHz	50 Hz	interlaced
1024 x 800	8	256	32 MHz	60 Hz	interlaced
800 x 600	8	256	32 MHz	50 Hz	non-interlaced
720 x 560	8	256	32 MHz	60 Hz	non-interlaced

An interrupt in the V-sync phase can be generated to load the colour lookup table without any flicker on the monitor.

1.4 The Video Outputs

Four BNC connectors for connection of a colour monitor are provided on the front panel of the AGC-1 board A. The R-G-B outputs have the following characteristics:

–1V to +1V analogue voltage at 75 Ohm
64 MHz maximum pixel frequency

A composite SYNC output is also available on the front panel.

1.5 Light Pen Interface

The light pen input of the ACRTC chip is supported via a standard lightpen interface and the 15 pin D-sub connector available on the front panel.

1.8 Bus Interrupter Function

A Bus Interrupter Module BIM 68153 is installed on the AGC-1 board set supporting the ACRTC-IRQ output and an IRQ on vertical SYNC. The BIM includes 4 channels each providing interrupt request generation on a software programmable level (IRQ 1 to 7) with a programmable interrupt vector.

2.0 Special Functions

The AGC-1 board set contains special hardware logic for zoom and scroll which are extensions to the functions of the ACRTC chip.

2.1 Zoom

A hardware zoom for zoom factors 1 to 16 is installed to provide a flicker-free display supporting the three different split screens. The zoom can be used in conjunction with the smooth scroll. The X and the Y zoom factors are independently programmable.

2.2 Smooth Scroll

Vertical and horizontal smooth scroll is implemented on the AGC-1 board set providing pixel-wise scrolling.
Both the vertical and the horizontal scroll factors are software programmable for the 3 different split screens.

2.3 Blinking

The AGC-1 board set can be used in a wide variety of applications and the blink function of the ACRTC chip is installed on the board set as follows:

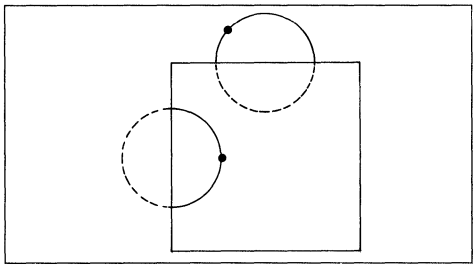
4 Bit Mode:	
4 Pixel	+ 1 Blink Attribute
4 Pixel	+ 1 Blink Attribute + 1 Blink Overlay
4 Pixel	+ 2 Blink Overlays

8 Bit Mode:	
8 Pixel	+ 1 Blink Attribute
7 Pixel	+ 1 Blink Attribute + 1 Blink Overlay
6 Pixel	+ 2 Blink Overlays

2.4 Clipping and Hitting

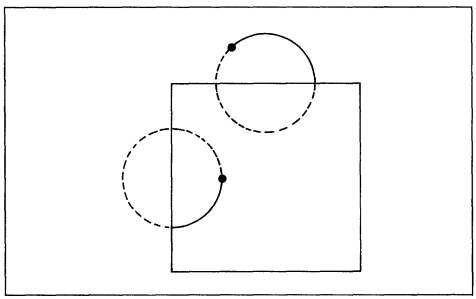
The ACRTC provides the clipping function which allows figures to be drawn within/outside a defined drawing area without destroying information outside/within the specified drawing area.

Example
Clipping:



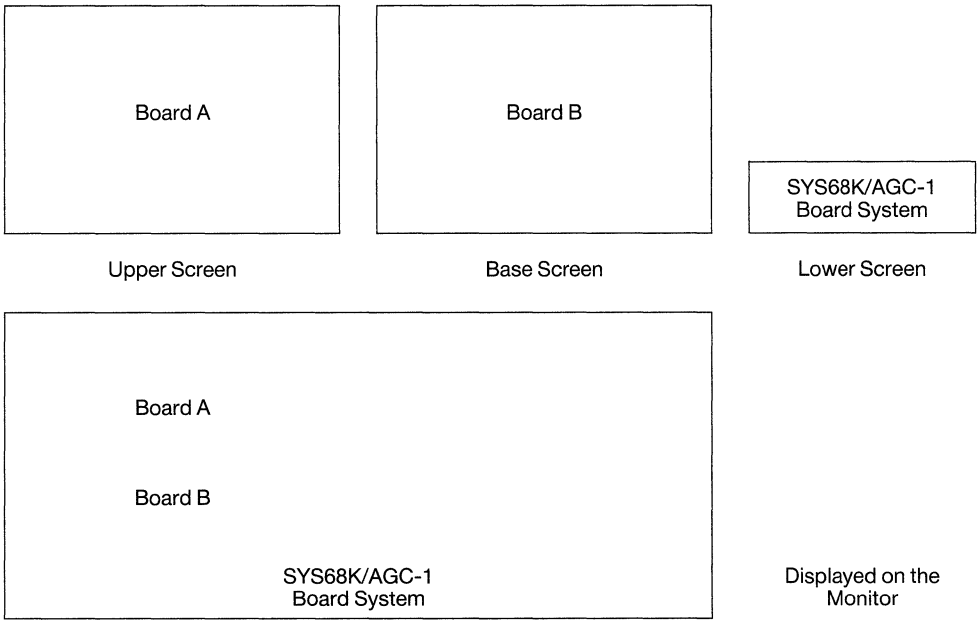
The hitting function allows a figure to be draw inside/outside the specified drawing area. Concurrent to the clipping function, all pixels inside/outside the specified drawing area will be set. The clipping function sets all pixels inside/outside the drawing area until the drawing area is left/reached. If the figure returns into the drawing area, clipping will not modify the pixels because hitting modifies this pixel.

Example
Hitting:



2.5 The Split Screens

The ACRTC offers as many as 4 different screens to be displayed, the upper-, lower- and base screen as well as the window. The position where the screens have to be displayed is fully software programmable (independent from each other).
Parts of figures can be drawn separately and displayed together without any flicker on the screen.
An example for three split screens is outlined below:



Each of the split screens as well as the window have separate attributes for scrolling and zooming, built with separate hardware logic, controlled by the ACRTC chip.

2.6 The Cursor

The ACRTC chip provides a software controlled cursor which is implemented on the AGC-1. The two hardware cursors are not implemented because the ACRTC-1 chip does not allow the positioning of the cursor on a pixel base, which creates incorrect display information if zoom and/or the smooth scroll is active. A copy of a 16 by 16 pixel field included in the video memory is usable in building the cursor. The pattern in the RAM cells is programmable so that the cursor displays the user defined figure.

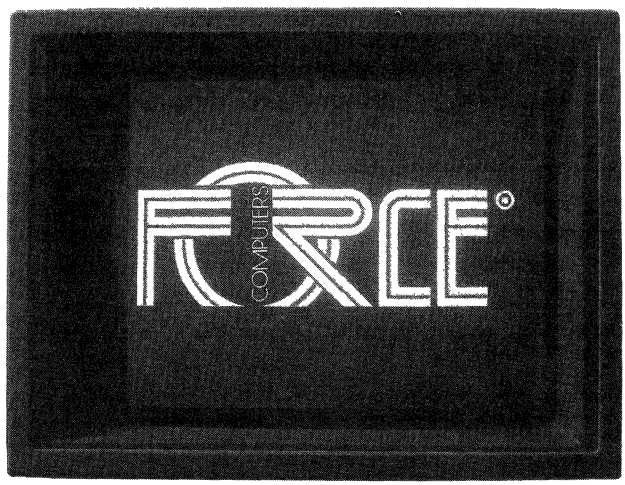
3.0 The ACRTC Command Set

The ACRTC chip contains a set of 38 commands dedicated to three groups, Register Access, Data Transfer, and Graphic Drawing commands. The five Register Access commands allow access to the pattern RAM and the drawing parameter registers. Ten Data Transfer commands are used to move data between the video memory and the VMEbus host or within the video memory.

The 23 Graphic Drawing commands cause the ACRTC to perform drawing separations. The parameters for these commands are specified using logical x-y coordinates. All 38 commands, parameters and data are transferred via the ACRTC read and write FIFOs.

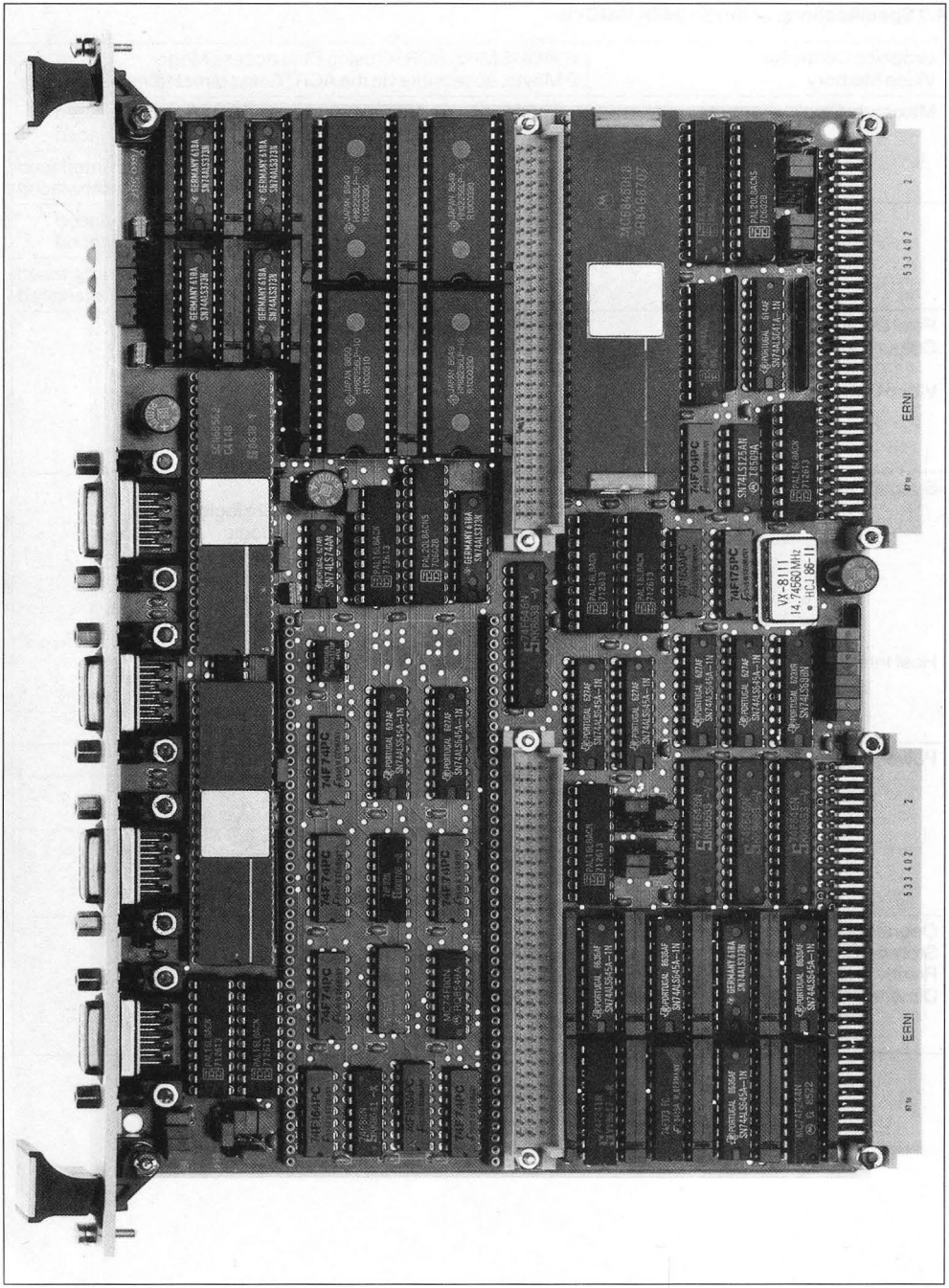
The following table lists all commands installed on the ACRTC chip.

Type	Mnemonic	Function
Register Access Commands	ORG	Set Origin Point
	RPR,WPR	Read/Write Parameter Registers
	RPTN,WPTN	Read/Write Pattern RAM
Data Transfer Commands	DRD,DWT,DMOD	DMA Read/Write/Modify
	RD,WT,MOD	Read/Write/Modify
	CLR,SCLR	Clear
	CPY,SCPY	Copy
Drawing Commands	AMOVE,RMOVE	Move
	ALINE,RLINE	Line
	ARCT,RRCT	Rectangle
	APLL,RPLL	Polyline
	APLG,RPLG	Polygon
	CRCL	Circle
	ELPS	Ellipse
	AARC,RARC	Arc
	AEARC,REARC	Ellipse Arc
	AFRTC,RFRTC	Filled Rectangle
	PAINT	Paint
	DOT	Dot
	PTN	Pattern
	AGCPY,RGCPY	Graphic Copy



4.0 Specifications of the SYS68K/AGC-1:

Graphics Controller Video Memory	63484 (8 MHz) ACRTC using Dual Access Mode 2 Mbyte, accessible via the ACRTC and direct from the VMEbus			
Maximum Display Formats	4 bit Mode	1600 x 1200 1280 x 1024	50 Hz 60 Hz	interlaced interlaced
		1140 x 860 1024 x 800	50 Hz 60 Hz	non interlaced non interlaced
	8 bit Mode	1140 x 860 1024 x 800	50 Hz 60 Hz	interlaced interlaced
		800 x 600 720 x 560	50 Hz 60 Hz	non interlaced non interlaced
Pixel Depth Colour Selection Video Outputs	4 or 8 bit, depending on the display format 16 or 256 colours out of a set of 16 million colours (software programmable) 32 or 64 MHz pixel frequency 1.0 Vss R, G, and B on 75 Ohm load TTL compatible composite SYNC on 75 Ohm load 4 BNC connectors installed on the front panel			
Special Functions Host Interface	Hardware Zoom (1 to 16) Horizontal smooth scroll via hardware logic Vertical smooth scroll via hardware logic 3 different screens 1 window Software cursor Hitting and clipping functions Lightpen interface VMEbus IEEE 1014 compatible A24 : D16, D8 or A16 : D16, D8 Interrupter to VMEbus 4 IRQs on level 1 to 7			
Power Requirements		+5V	+12V	−12V
	Board A Board B	5.8A 5.6A	0.1A –	0.7A 0.7A
	Because of the power requirements, the AGC-1 board has to be powered on the P1 and P2 connectors.			
Operating Temperature Storage Temperature Relative Humidity Dimensions	0 to 50 Degrees C −50 to 85 Degrees C (non-operating) 0–90% (non-condensing) Double Eurocard 234 x 160 mm 9.2" x 6.3"			


VX-8111
14.74560 MHz
HCJ 86-11
ERNI
ERNI

5.0 General Description

The SYS68K/AGC-1X is a very sophisticated extension for the SYS68K/AGC-1 graphics system. It adds a list of very useful features to the AGC-1 boardset to give them maximum performance in all graphic applications.
The 128 Kbyte character RAM provides a powerful character overlay using the window features of the AGC-1. Characters could be displayed with 8 colours out of 16 million in normal and in inversed mode. The blink feature of the ACRTC 63484 is also supported. There is a great variety of displaying character oriented information with the SYS68K/AGC-1.
The 256 Kbyte character generator consists of 128 Kbyte EPROM and 128 Kbyte RAM and allows the user to generate up to 4096 characters or graphic symbols at one time. The character size is programmable and can vary between 8, 16 or 32 pixels in width and up to 32 lines in height.
Four serial I/O channels with V24/RS232 interface using the DUSCC 68562 with data rates up to 4 Mbit/s ease the adoption of mainframe links as well as the interfacing of graphic tableaus, plotters, printers, keyboards and mice.
The four channel DMA controller 68450 DMAC enhances the access to the SYS68K/AGC-1 by supporting memory to/from video RAM transfers as well as single access transfer to/from the 63484 ACRTC. The DMAC also supports two of the four serial I/O channels. The 68450 DMAC is fully transparent to the VMEbus and can speed up memory to memory transfers from any location to any location on the VMEbus.
A VMXbus interface is also available on the board which gives the opportunity to implement local graphic functions in VMEbus environments.

6.0 Features of the SYS68K/AGC-1X

- 128 Kbyte of character RAM supporting the character feature of the 63484 ACRTC.
  8 colours out of 16 million (for the character display) invers, blink attributes
  max. 4096 different characters accessible
- 256 Kbyte of character generator RAM/EPROM supports the generation of characters with 8, 16 or 32 columns width and up to 32 lines height. Depending on the column mode the character generator stores up to 4096 different characters or graphic symbols.

column mode (columns/character)	no. of characters (available in the generator)
8	4096
16	2048
32	1024

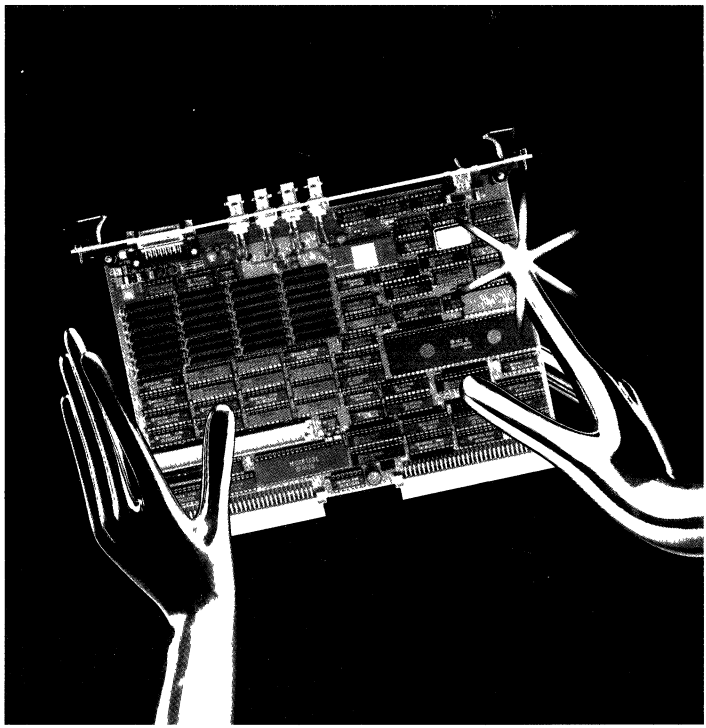
- Two DUSCC 68562 (Dual Universal Serial Communications Controller) provide four serial I/O channels.
  data rates up to 4 Mbit/second
  synchronous and asynchronous protocols
  V24/RS232 Interface via 9 pin DSUB female connectors
  DMA support for two channels
- The four channel DMA controller (DMAC 68450) supports data transfers on the VMEbus, directly interfacing the 63484 ACRTC on the SYS68K/AGC-1 board and one DUSCC 68562.
  DMA transfers from/to the video memory.
  DMA transfers from/to the DUSCC 68562.
  DMA transfers from/to the 63484 ACRTC using single access transfers.
  Four level BUS ARBITER.
  Release-When-Done, Release-On-Request function.
  Retry, Relinquish an Retry function on BERR.
  Bus master indication LED.
  DMA transfers from any to any location on the VMEbus (A24, A16).
  Fully compatible with VMEbus/IEEE 1014 standard.
- The VMXbus interface supports the following data transfer modes for accesses to all devices on the SYS68K/AGC-1 and the SYS68K/AGC-1X:
  A24 : D16, D8
  The access address from the VMEbus (Standard Memory) and the VMXbus are identical.
  DMA transfers on the VMEbus using the 68450 DMAC on the SYS68K/AGC-1X can be initiated via the VMXbus.

7.0 Specifications of the AGC-1X

Function	Description
Character RAM	128 Kbyte RAM using overlay and window in conjuction with the AGC-1
Character Colours	8 colors usable at one time out of a selection of 16 million
Character Blinking	Is supported in conjuction with the AGC-1
Character Generator	128 Kbyte on RAM 128 Kbyte on EPROM
Character Size	8, 16 or 32 pixels width, up to 32 lines height in 1 line steps
Serial Interfaces	Four RS232/V24 for graphic devices (Tableau, Printer, Plotter, Keyboard and Mouse)
Other Interfaces	VMXbus slave interface which allows access to the AGC-1 and AGC-1X
Other Devices on Board	68450 DMAC for high speed transfers on the VMEbus
Power Requirements	+5V 4.5V +12V 0.03A −12V 0.03A
Operating Temperature Relative Humidity Dimensions	0 to 50 Degrees C −50 to 85 Degrees C (nonoperating) 0 to 90% (non-condensing) Double Eurocard (2x) 234 x 160 mm 9.2" x 6.3"

Ordering Information

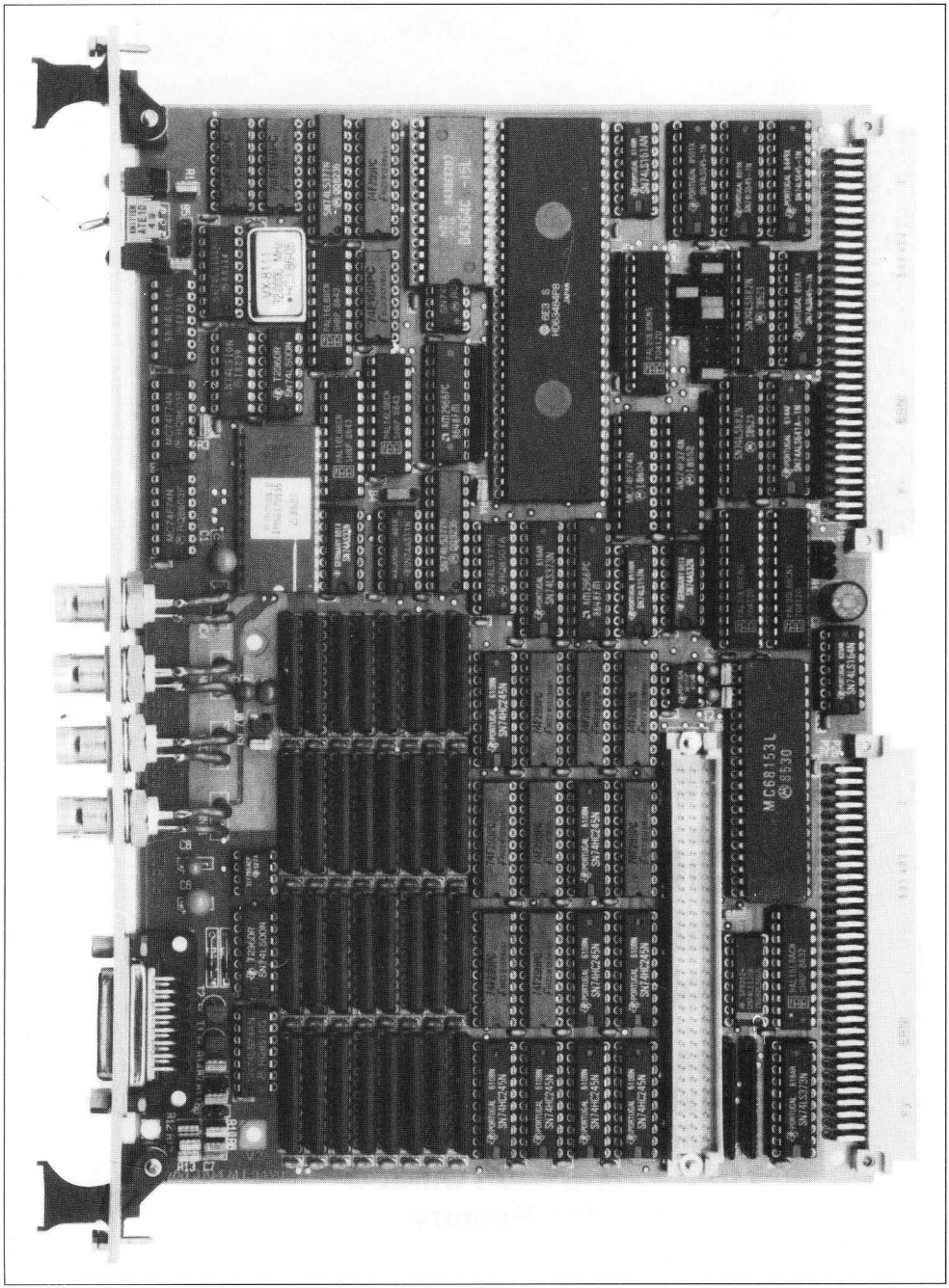
SYS68K/AGC-1 Part No. 400020	Advanced Graphic Controller Board Set consisting of the A and B Board. Documentation included.
SYS68K/AGC-1/UM Part No. 800106	User's Manual for the SYS68K/AGC-1 Board Set.
SYS68K/AGC-1X Part No. 400022	Advanced Graphic Controller extension board to the AGC-1. Documentation included.
SYS68/AGC-1X/UM Part No. 800107	User's Manual for the AGC-1X board.



System 68000 VME SYS68K/AGC-2

Advanced Colour Graphic Controller Board

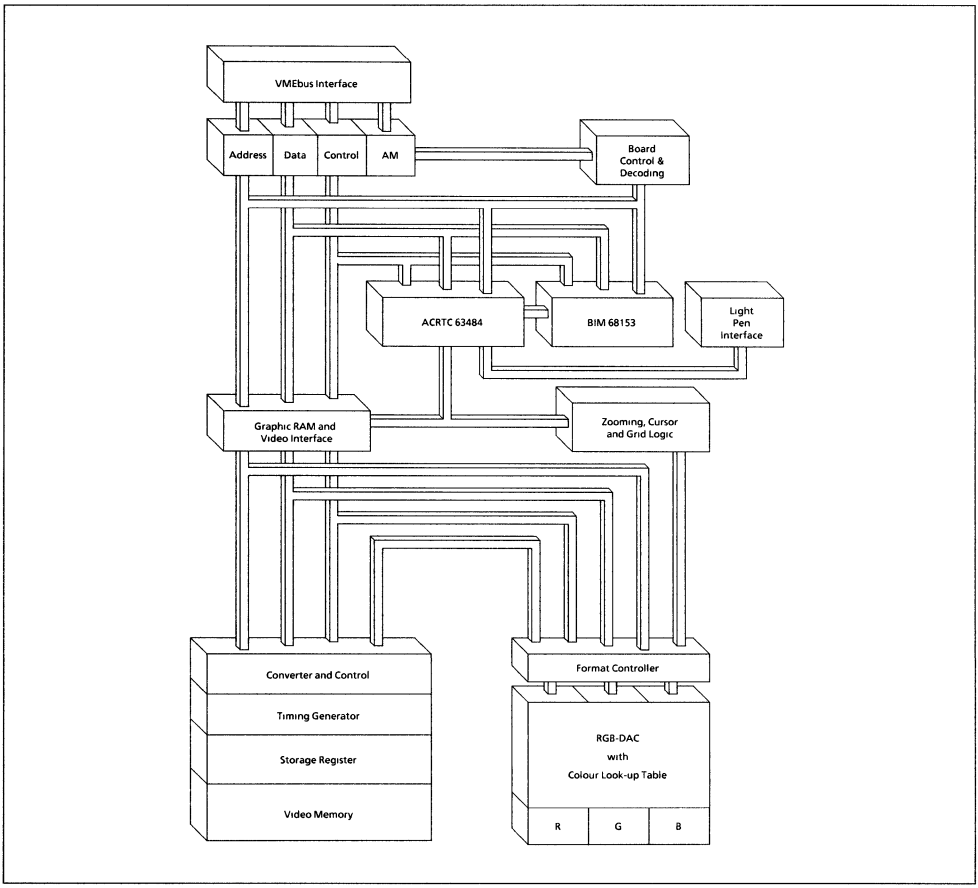
- 63484 ACRTC Controller
- 1160x870x4 Bit interlaced display format
- 16 colours out of 262144 colours
- 3 split screens and 1 window
- 1 Mbyte Video Memory


MC68153L
8930

General Description

The SYS68K/AGC-2 is a high performance graphic board which combines a powerful graphic processor, the 63484 ACRTC, with 1 Mbyte video RAM and a digital-to-analogue convertor, the IMS G170, with a colour look-up table.
The maximum resolution to be displayed at 50 Hz is 1160 x 870 pixel with 4 bit/pixel colour information and interlaced display mode.
Flicker-free display in the non-interlaced mode is provided by using the 800 x 600 display format which provides 50 Hz frequency and 4 bit/pixel colour information. The pixel frequency of the RGB output is 32 MHz, or 16 MHz to allow the connection of a lower resolution monitor also.
To provide maximum flexibility, 16 different colours, out of 262144, can be simultaneously displayed at the maximum format of 1160 x 870 pixels using the 50 Hz interlaced display mode.
The 1 Mbyte video RAM is accessible via the ACRTC by using its powerful command set.
The local control, which consists of a Bus Interrupter Module (BIM), offers software control for programming the ACRTC and updating the frame buffer of the colour look-up table during vertical retrace period.
The AGC-2 also provides a standard light pen interface which is accessible through the front panel.
The VMEbus interface is Rev.C and IEEE 1014 compatible and contains a jumper selectable access address and address modifier for the on-board devices.
A free programmable cursor and a grid, which can be filled in, are additional features of the AGC-2.

BLOCK DIAGRAM OF THE SYS68K/AGC-2 BOARD



Features of the SYS68K/AGC-2

- ACRTC 63484 with a clock frequency of 4 MHz.
- 23 High level graphic commands, such as LINE, RECTANGLE, POLYLINE, POLYGON, CIRCLE, ELLIPSE, PAINT, COPY etc.
- 1 MB video RAM accessible via the ACRTC.
- Free programmable cursor independent from zoom and window limits.
- Grid logic in combination with zooming.
- R-G-B and composite SYNC output.
- 3 different screens with software programmable positions.
- 1 graphic colour RGB-DAC with colour look-up table providing 16 simultaneously displayable colours out of a palette of 262144 colours.
- Light pen interface.
- VMEbus/IEEE 1014 interface
  A24 : D16, D8
  A16 : D16, D8
- Interrupter to VMEbus with software programmable IRQ level and vector.
- RUN/LOCAL switch to disable VMEbus accesses.
- Full decoding of the address modifiers.

1.0 Functional Description

The ACRTC 63484 receives the drawing commands from a CPU-board through the VMEbus interface. All address calculations to the video RAM are made internally to deload the CPU-board programs by using only x- and y-coordinates.
The controller chip automatically generates the timing to the screen after initialization.
4 bits/pixel provide 16 colours to be displayed out of the complete range of 262144 colours.

1.1 The ACRTC 63484

The advance CRT Controller 63484 provides 38 commands including 23 graphic drawing commands. A 16 byte on-chip Read/Write FIFO reduces communication overhead of the CPU-board. Automatic conversion of the x-y coordinates to physical frame buffer addresses is provided through the on-chip drawing processor.
All timing parameters for the used monitor are software programmable, and the ACRTC generates all the necessary timings to the R-G-B and SYNC outputs.
The controller also allows the usage of up to 3 different screens (upper, lower and base screen), plus one window screen.
The size and the position, as well as the smooth scroll for each screen, is software programmable.
The light pen interface of the ACRTC is supported via the 15 pin D-sub connector available on the front panel.

1.2 The Video RAM

1 MB of video RAM is installed on the AGC-2 board.
The video RAM enables the usage of multiple pictures to be held in the video memory (depending on the display size and the zoom factor).
The video RAM can be accessed via the ACRTC using its data transfer commands.

1.3 The Colour Look-up Table

The AGC-2 contains the IMS G170 RGB-DAC with colour look-up table, 4 bits/pixel provide 16 colours to be displayed out of the complete range of 262144 colours.
The colour look-up table is accessible through the VMEbus/IEEE 1014 interface.
An interrupt in the V-sync phase can be generated to load the colour look-up table without any flicker on the monitor.

1.4 The Video Outputs

Four BNC connectors for the connection of a colour monitor are provided on the front panel of the AGC-2 board. The R-G-B outputs have the following characteristics:
0 to 1V (analogue) at 75 Ohm
32 MHz maximum pixel frequency
A composite SYNC output is also available on the front panel.

1.5 Light Pen Interface

The light pen input of the ACRTC chip is supported via a standard light pen interface and the 15 pin D-sub connector available on the front panel.

1.6 Display Formats

The resolution to be displayed depends on the monitor parameters as well as on the AGC-2 hardware setups. The following table lists standard display formats which are supported from the AGC-2 hardware and which are tested with various monitors.

Horizontal x Vertical	Bit/Pixel	No. of Colours	Pixel Frequency	Frame Period	Mode
1160 x 870	4	16	32 MHz	50 Hz	Interlaced
1024 x 800	4	16	32 MHz	60 Hz	Interlaced
800 x 600	4	16	32 MHz	50 Hz	non-Interlaced
720 x 560	4	16	32 MHz	60 Hz	non-Interlaced
690 x 520	4	16	16 MHz	50 Hz	Interlaced
640 x 480	4	16	16 MHz	60 Hz	Interlaced

All display parameters are software programmable to offer maximum flexibility and minimize software overhead.

1.7 The VMEbus Interface

A full VMEbus IEEE 1014 standard interface is installed on the AGC-2 board. The access address and the address modifier code of the board are jumper selectable within the standard address range (A24: D16, D8) and short I/O range (A16: D16, D8). The ACRTC, the Bus Interrupter Module BIM 68153, the RGB-DAC IMS G170 and the cursor RAM are accessible under the same AM-codes.
All address, data and control signals are latched and buffered to build the local bus.

1.8 Bus Interrupter Function

A Bus Interrupter Module, BIM 68153, is installed on the AGC-2 board supporting the ACRTC-IRQ output as well as an IRQ on vertical and horizontal SYNC. The BIM includes 4 channels, each providing interrupt request generation on a software programmable level (IRQ 1 to 7) with a programmable interrupt vector.

2.0 Special Functions

The AGC-2 board contains special hardware logic for zoom, a cursor (independent from zooming and windows) and grid logic (combined with zooming).

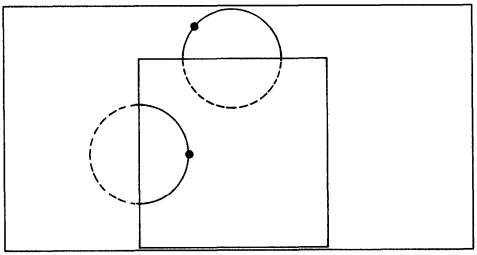
2.1 Zoom

A hardware zoom for zoom factors 1 to 16 is installed to provide a flicker-free display supporting the base screen. The x and y zoom factors are independently programmable.

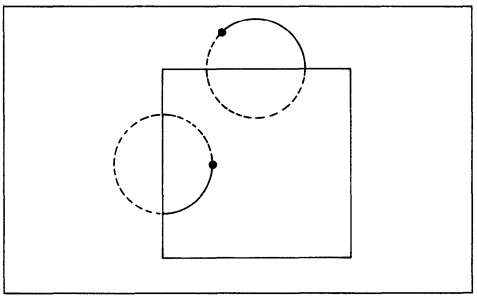
2.2 Clipping and Hitting

The ACRTC provides the clipping function which allows figures to be drawn within/outside a defined drawing area without destroying information outside/within the specified drawing area.

Example of Clipping:



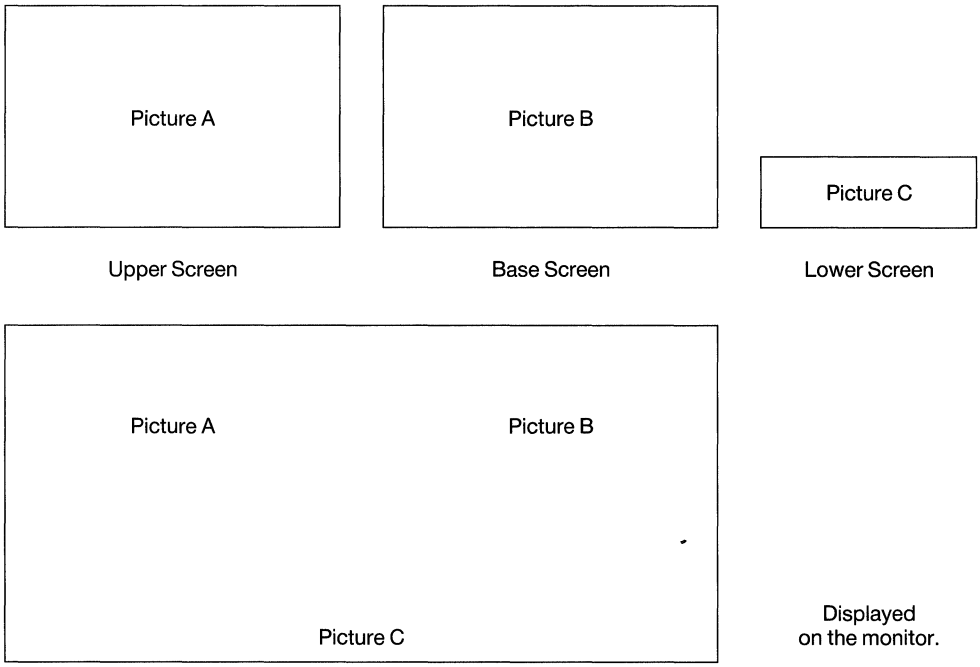
Example of Hitting:



2.3 The Split Screens

The ACRTC offers as many as 4 different screens to be displayed: the upper-, lower- and base screen as well as the window. The position where the screens have to be displayed is fully software programmable (the screens being independent from each other).
Parts of figures can be drawn separately and displayed together without any flicker on the screen.

An example for three split screens is outlined below:



2.4 The Cursor

The ACRTC chip provides a software controlled cursor which is implemented in hardware on the AGC-2.
8 Kbyte static RAM, accessible via the VMEbus interface and independent from the video RAM, provides a cursor with free programmable colour and form in a maximum size of 128 x 128 pixels. The position is independent from zoom and window limits, and is programmable in 1 pixel steps in both horizontal and vertical directions.

2.5 The Grid

A grid with 1 pixel width and the distance of the actual zoom factor can be filled in. The colour of the grid is free programmable.

3.0 The ACRTC Command Set

The ACRTC chip contains a set of 38 commands dedicated to three groups, Register Access, Data Transfer and Graphic Drawing commands. The five register access commands allow access to the pattern RAM and to the drawing parameter registers. Ten data transfer commands are used to move data between the video memory and the VMEbus host, or within the video memory.

The 23 graphic drawing commands cause the ACRTC to perform drawing separations. The parameters for these commands are specified using logical x-y coordinates. All 38 commands' parameters and data are transferred via the ACRTC read and write FIFOs.
The following table lists all commands installed on the ACRTC chip:

Type	Mnemonic	Function
Register Access Commands	ORG	Set Origin Point
	RPR,WPR	Read/Write Parameter Registers
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Data Transfer Commands	RD,WT,MOD	Read/Write/Modify
	CLR,SCLR,	Clear
	CPY, SCPY	Copy
Drawing Commands	AMOVE,RMOVE	Move
	ALINE,RLINE	Line
	ARCT,RRCT	Rectangle
	APLL,RPLL	Polyline
	APLG,RPLG	Polygon
	CRCL	Circle
	ELPS	Ellipse
	AARC,RARC	Arc
	AEARC,REARC	Ellipse Arc
	AFRTC,RFRTC	Filled Rectangle
	PAINT	Paint
	DOT	Dot
	PTN	Pattern
	AGCPY,RGCPY	Graphic Copy

Specifications of the SYS68K/AGC-2:

Graphics Controller Video Memory	63484 (4 MHz) ACRTC 1 Mbyte, accessible via the ACRTC		
Maximum Display Formats	1160 x 870 1024 x 800	50 Hz 60 Hz	Interlaced Interlaced
	800 x 600 720 x 560	50 Hz 60 Hz	non-Interlaced non-Interlaced
Pixel Depth Colour Selection Video Outputs	4 bit 16 colours out of a set of 262144 (software programmable) 16 or 32 MHz pixel frequency 1.0Vss R, G, and B on 75 Ohm load TTL compatible composite SYNC on 75 Ohm load 4 BNC connectors installed on the front panel		
Special Functions	Hardware Zoom (1 to 16) 3 different screens 1 window Software cursor Hardware cursor Grid Logic Hitting and clipping function Light Pen interface		
Host Interface	VMEbus Rev.C and IEEE 1014 compatible A24:D16, D8 or A16:D16, D8 Interrupter to VMEbus 4 IRQs on level 1 to 7 (software programmable)		
Power Requirements	+5V 3.2A	+12V 0.1A	−12V 0.2A
Operating Temperature Storage Temperature Relative Humidity Dimensions	0 to 50 Degrees C −50 to 85 Degrees C (non-operating) 0 to 90% (non-condensing) Double Eurocard 234 x 160 mm 9.2 x 6.3 inch		

Ordering Information

SYS68K/AGC-2 Part No. 400023	Advanced Graphic Controller Board Including Documentation.
SYS68K/AGC-2/UM Part No. 800139	User's Manual for the SYS68K/AGC-2 Board.

General Controller Boards

FORCE Computers General Controller Board Introduction

The family of VMEbus based products offered by FORCE Computers includes a family of controller cards which cover application needs for system control and networking.

General Feature Overview

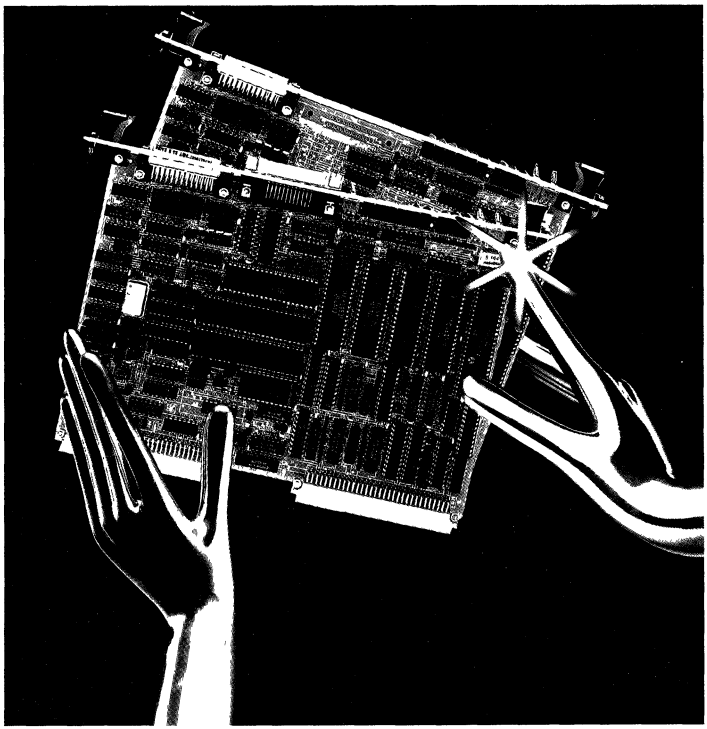
If your application requires multi-level bus arbitration, additional I/O and specialist multiprocessing features, then look no further than the SYS68K/ASCU-1/2 system controller boards. Both boards support the full IEEE 1014 standard 4 level bus arbitration options, Centronics printer interface, serial I/O interface and a Real Time Clock. Additionally, the ASCU-2 also supports an IEEE-488 (GPIB) interface and the facility to trigger H/W interrupts on the VMEbus from software. This added feature makes the ASCU-2 the ideal choice for multiprocessing applications. The ASCU-1/2 are the IEEE 1014 standard system controller modules.
The SYS68K/ILANC-1 card offered by FORCE Computers provides the systems integrator with an interface to the most commonly used networking architecture in the market today. The ILANC-1 card is also available with TCP/IP firmware on the board and will be fully supported by the UNIX V.3 port on the FOCUS system with remote file serving. This product is due for availability early in 1988.

System Controllers

FAMILY	ASCU-1	ASCU-2
Bus Arbiter	4 level Round Robin 4 level Prioritized 4 level Prioritized Round Robin	4 level Round Robin 4 level Prioritized 4 level Prioritized Round Robin
SYSCLOCK Driver SYSRESET Switch and Generator Power Monitor VMEbus Time Out Generator VMEbus Arbitration Timeout Generator	yes yes yes yes yes	yes yes yes yes yes
Interrupt Generator to VMEbus No. of Channels Total No. of Different Interrupts to VMEbus	– – 8	yes 8 16
Serial I/O Interface (RS232/RS422) Parallel I/O Interface Real Time Clock with Battery Backup IEEE 488 (GPIB/HPIB) Interface Timer	1 Centronics yes – 1 x 24 bit	1 Centronics yes yes 2 x 24 bit
Detailed Description on Page:	347	347

Network Controller

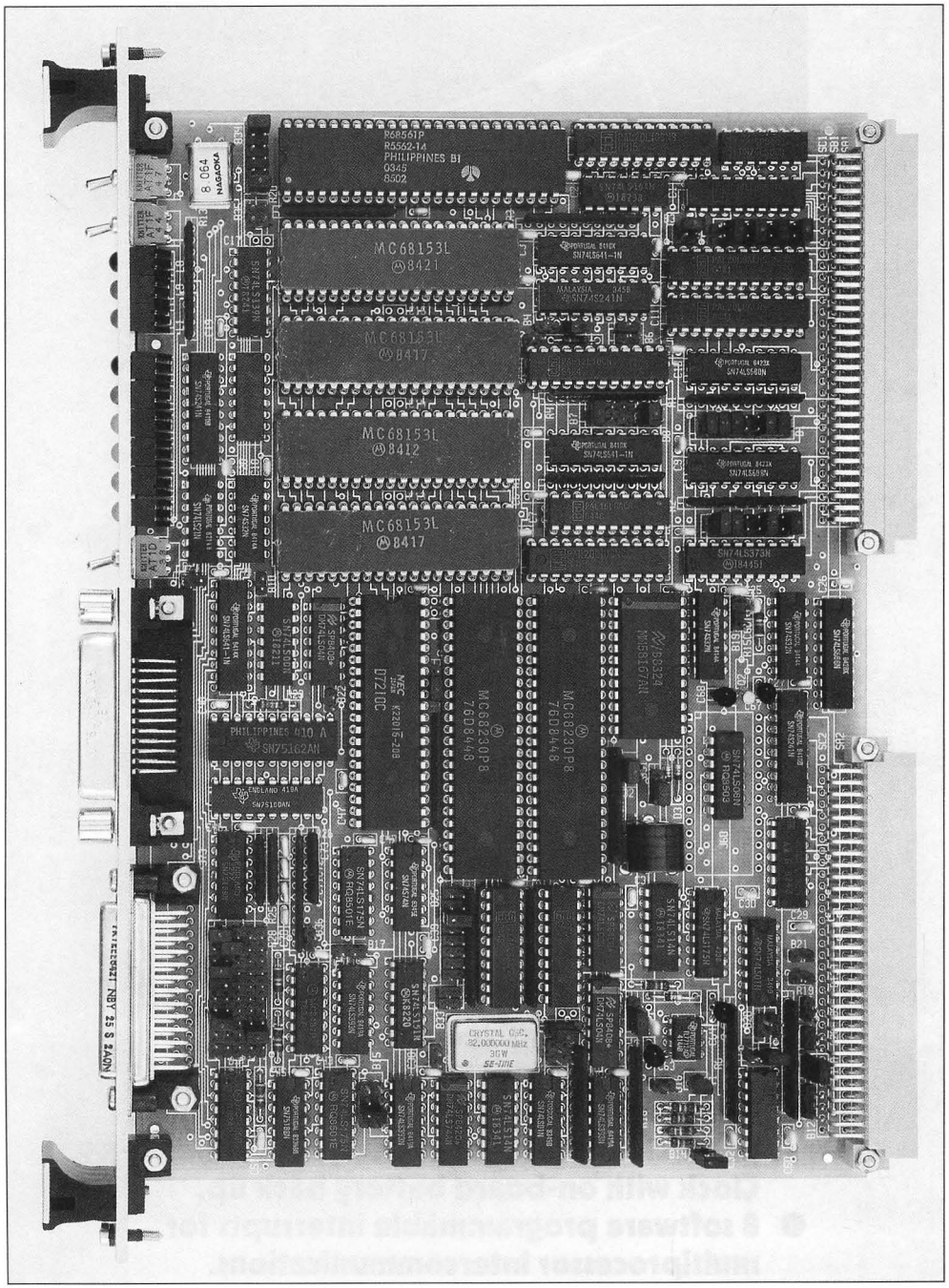
	ILANC-1
Used CPU	68010
Used Controller Chips	AM 7990 LANCE AM 7992 SIA
EPROM Capacity	64 Kbyte
On Board RAM RAM Capacity Bitrate	Dual Access DRAM 512 Kbyte 10 Mbit/s
VMEbus Interface	A24: D16
Ethernet Compatibility	Ethernet 1.0, 2.0 IEEE 802.3
Detailed Description on Page:	355



System 68000 VME
SYS68K/ASCU-1/2

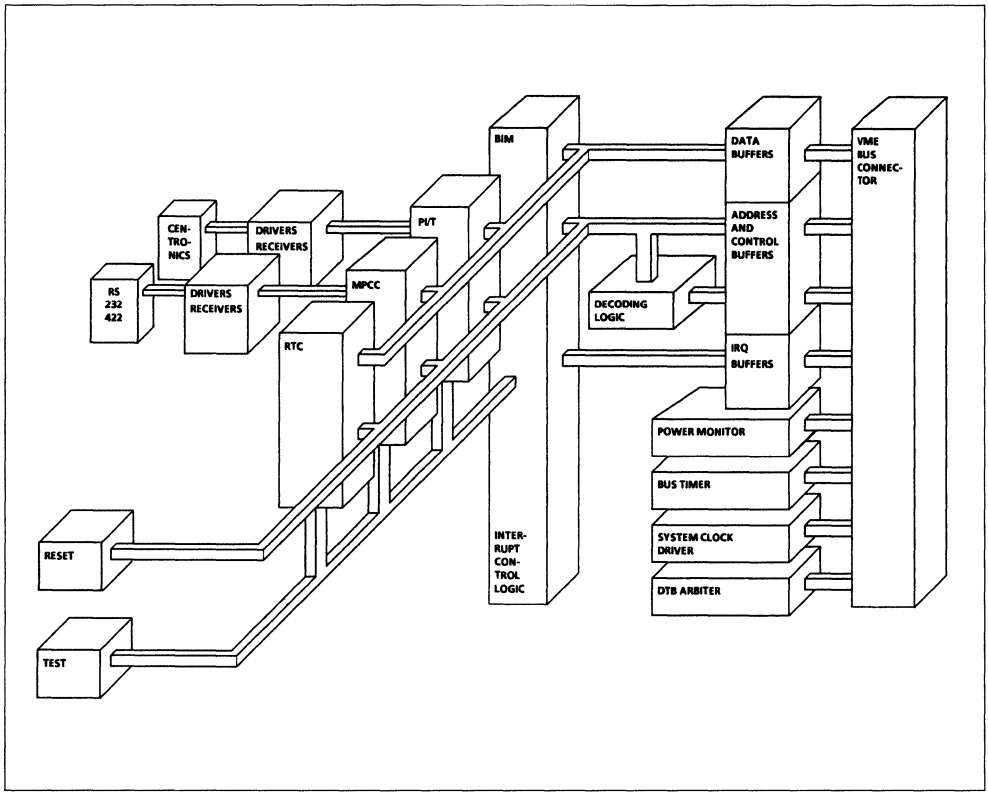
Advanced System Control Unit

- **4 level bus arbiter with prioritized, round robin and prioritized round robin operating mode.**
- **High speed serial I/O channel, Centronics parallel interface for printer, Real Time Clock with on-board battery back up.**
- **8 software programmable interrupts for multiprocessor intercommunications.**


MC68153L
8421
MC68153L
8417
MC68153L
8412
MC68153L
8417
MC68230P8
76D8448
MC68230P8
76D8448
PHILIPPINES 410 A
SN75162AN
CRYSTAL OSC.
32.0XXXX MHz
3GW
SE-TIME

General Description SYS68K/ASCU-1
The SYS68K/ASCU-1 board is a high performance system controller which handles all exception signals on the VMEbus and contains powerful I/O devices such as a serial interface (RS232 and RS422 compatible), a centronics parallel interface, a real time clock with battery backup, and a 4 level bus arbiter.
The block diagram shows the different building blocks in detail.

BLOCK DIAGRAM OF THE SYS68K/ASCU-1



SYS68K/ASCU-1 Features

- 4 level Bus ARBITER with prioritized, round robin, and prioritized round robin operating mode
- LEDs show the current bus master level (0-3)
- High speed serial I/O channel with built-in 68561 Multi-Protocol Communications Controller, RS232 and RS422 driver/receiver circuitries
- Centronics Parallel Interface for printer connection
- 58167A Real Time Clock with on-board battery back-up
- POWER MONITOR provides automatic power up/power-down and ACFAIL/SYSRESET handling through power fail detection. A Reset function switch generates a SYSRESET to the VMEbus
- SYSTEM CLOCK DRIVER (16MHz)
- BUS TIMER with software selectable timeouts for Bus Error generation
- Timer Interrupt can be used for time measurements or as a watch dog
- Software selectable option for generating an interrupt on ACFAIL detection
- TEST function switch generates an interrupt to the VMEbus on a software programmable level
- Every I/O device interrupt can be programmed to one of the 7 IRQ levels on the Priority Interrupt Bus
- Jumper selectable access address and address modifier codes
- DTB slave bus interface

Functional Description

All of the I/O and control devices are accessible and programmable via the VMEbus interface. The ASCU is compatible to the VMEbus spec as well as to the IEEE 1014 standard.
The various functional areas of the board are described briefly in the following paragraphs.

1. The Serial I/O Interface

A Multi-Protocol Communications Controller (MPCC 68561) with an 8/16 bit data path is used on the ASCU-1 to provide maximum flexibility for serial communications.
Protocols:
- IBM synchronous (ASCII or EBCDIC)
- Character oriented protocols (BSC, DDCMP, X3.28, X.21, ECMA16 etc.)
- Synchronous bit oriented protocols (SDLC, HDLC, ADCCP, X.25)
- Standard asynchronous protocol

A software programmable baud rate generator (from 110 to 38400 baud) and the local loop-back provide maximum flexibility. The pin assignments to the 25 pin D-sub connector on the front panel of the two interfaces (one RS232 and one RS422 compatible interface) are jumper selectable.

The MPCC can initiate an interrupt to the VMEbus on a software programmable level; 3 different interrupt vectors are programmable.

2. The Centronics Interface

A Parallel Interface and Timer Module (68230 PI/T) is used on the SYS68K/ASCU-1 to provide a centronics parallel interface. All of the interface signals are fully buffered in both directions, and are connected to the user I/O pins of connector P2. The following signals of the Centronics Interface are supported:

D1-D8
DATA STROBE
ACKNOWLEDGE
BUSY
PAPER END
SELECT
ERROR

Interrupts on a software programmable level and vector can be generated through the on-board Bus Interrupter Modules (68153 BIM).

3. The Real Time Clock

The Real Time Clock (58167A RTC) allows various applications such as time scheduling, time measurement, counting and simple calendar functions. The RTC may act as an actual time base independent from the main power through the on-board lithium battery.
The RTC provides the following features:

MONTH
DAY OF MONTH
DAY OF WEEK
HOURS
MINUTES
SECONDS
1/1000 SECONDS

The RTC is able to generate an interrupt to the VMEbus on a software programmable interrupt level. The interrupt vector is also software programmable.

4. Local Control and the Bus Timer
The PI/T is used on the SYS68K/ASCU-1 to provide the centronics parallel interface and its additional I/O lines are used to control the bus error time-out values.
The ASCU-1 contains 8 different software programmable Bus Time values for a wide range of applications.
One of the 8 possible time-outs can be selected to generate a BERR signal on the VMEbus (1, 2, 4, 8, 16, 32, 64 or 8000us). To avoid the problem that the IACK daisy chain may take between 1 and 10us more time than a normal cycle, a separate BERR time-out mechanism is included for IACK cycles on the VMEbus. Time-out is selectable (30 or 120us), independent from the normal Bus Time Value.

5. The TEST Switch
The ASCU-1 board contains a TEST switch which generates an interrupt to the VMEbus on a software programmable level and vector.
The P2 connector is used in parallel to connect an external switch for the interrupt generation.

6. The ACFAIL Handling
If an ACFAIL is detected on the VMEbus ACFAIL line or on an additional input on connector P2, a SYSRESET is generated after a defined time (please refer to paragraph 7). The signal can be jumpered to be active on positive or negative state. An interrupt on a software programmable level can be generated via one bus interrupter module. The interrupt vector is programmable.

7. The RESET Handling
The SYS68K/ASCU-1 handles the power-up/power-down mechanism on the VMEbus.
The ASCU-1 contains a Power Monitor Module as well as a counter for the ACFAIL time to generate a SYSRESET (jumper selectable from 1 to 16ms).
A RESET of the whole system may be programmed through the PI/T. Additionally, a switch on the front panel can generate a SYSRESET. Provision is made on the P2 connector to use an additional RESET switch (all the logic for the switch is included).

8. The 4 Level Bus Arbiter
A special bus arbiter is built on the ASCU-1 card to provide maximum flexibility for multi-processor environments.
Three modes are jumper selectable for the arbiter
a) prioritized scheme
b) round robin scheme
c) prioritized round robin scheme
Mode c) offers bus mastership to a master on level 3 every 2nd arbitration cycle. Therefore, level 3 has priority but levels 0, 1 and 2 are built in a round robin mode.
In all modes the bus clear signal (BCLR) can be generated if a higher prioritized request is pending.
Additionally, a local arbitration RESET is provided if a potential bus master has requested the bus but has not responded to the arbiter with a BBSY within a time frame. This avoids system crashes through incorrect arbitration cycles because the arbiter starts arbitration again.
The current DTB master level and the activities on the Bus Clear line are shown on 5 LEDs on the front panel.

9. The Access Selection
The SYS68K/ASCU-1 can be accessed under a jumper selectable access address and address modifier code.
The following modes are automatically assigned through an enabled AM-code:
A24 : D8/D16
A16 : D8/D16
The following AM-codes are jumper selectable (independent from each other)

No	AM-Code	Decode	HEX Code
1)	Standard Supervisory Data Access	A24	3D
2)	Standard Non-privileged Data Access	A24	39
3)	Short Supervisory I/O Access	A16	2D
4)	Short Non-privileged I/O Access	A16	29
5)	Ignore all AM Codes	A24	—

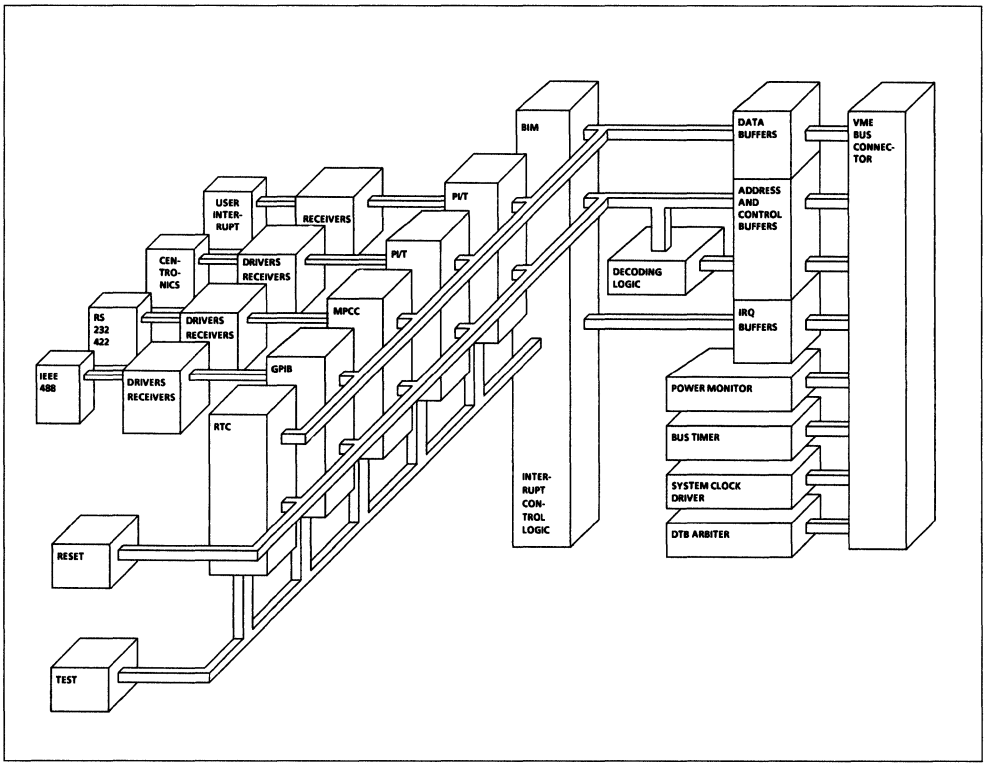
General Description SYS68K/ASCU-2

The SYS68K/ASCU-2 board incorporates the features of the ASCU-1 board plus additional powerful functions such as GPIB interface and interrupt capabilities for multiprocessor environments.
The block diagram shows the different building blocks.

SYS68K/ASCU-2 Features

- All the features contained in the SYS68K/ASCU-1 description
- General Purpose Interface Bus (IEEE488–1978) Talker, Listener, and Controller functions
- 8 different interrupts to the VMEbus (level and vector programmable)
- 4 user interrupts (buffered inputs through P2 connector)

BLOCK DIAGRAM OF THE SYS68K/ASCU-2



Functional Description
The additional I/O and control functions are described briefly in the following paragraphs:

1. The GPIB Interface
The board contains an IEEE488–1978 interface with a 24 pin "microribbon" connector available on the front panel. The advanced controller (NEC 7210) offers full software handling of the different modes.
Each of the Talker, Listener, and Controller functions are software programmable. The Talker and the Listener address is jumper selectable and readable via Port B of the additional Parallel Interface and Timer Module (PIT 68230).

2. The Interrupt Generator
The ASCU-2 contains four Bus Interrupter Modules (BIM 68153) for a complete set of 16 different interrupts.
Two BIM devices are added on the ASCU-2 to provide, in conjunction with Port A of the additional PI/T, 8 software programmable interrupts to the VMEbus. This feature allows easy multiprocessor communication because the level and the vector of each IRQ is separately software programmable. Each interrupt is automatically released if a register access was provided (RORA option).

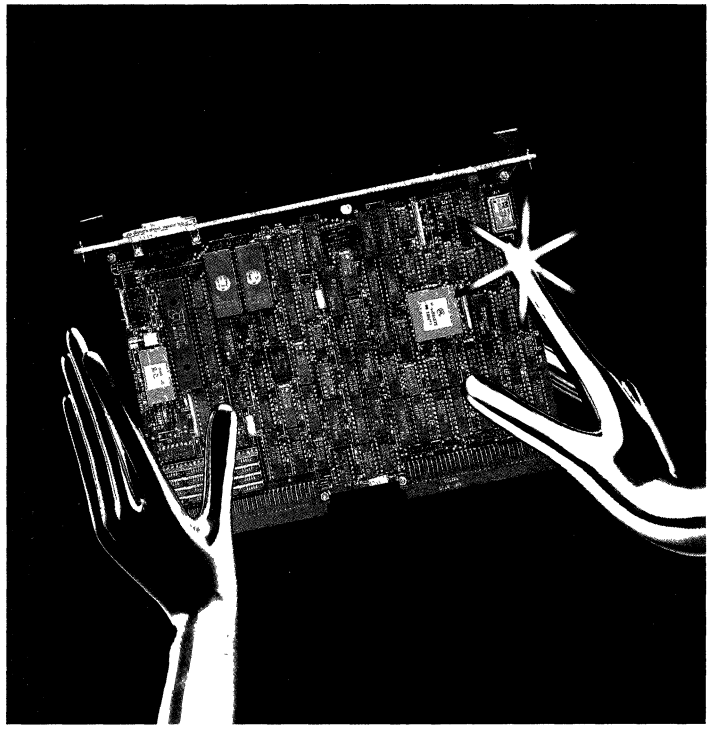
3. The User Interrupts
Five different interrupt sources can be connected to the P2 connector to provide external exception setting. This feature allows external devices or other systems to issue interrupts to a VMEbus system.
The input signals are fully buffered with Schmitt Trigger devices 74LS14.

Specification

Description	ASCU-1	ASCU-2
IEEE488 (GPIB) Interface	–	x
Serial I/O Interface RS422	x	x
RS232	x	x
Centronics Parallel Interface	x	x
Real Time Clock with Battery backup	x	x
SW-Programmable Bus Timer (2 to 12000us)	x	x
ACFAIL Handling	x	x
SYSFAIL Handling	x	x
TEST/RESET Switches	x	x
IACK Daisy Chain Driver	x	x
Interrupts to Priority Interrupt Bus	7	16
SW-Programmable Interrupts	–	8
User Interrupts on P2	1	5
RORA/ROAK Interrupt Release	x	x
4 Level Bus Arbiter	x	x
Address Selection A24:D16 / A16:D16	x	x
Power Requirements +5V (max)	3.0A	3.6A
+12V (max)	200mA	200mA
–12V (max)	200mA	200mA
Operating Temperature 0 to 60 degrees C	x	x
Storage Temperature –55 to +85 degrees C	x	x
Relative Humidity 0 – 95% (non-condensing)	x	x
Dimensions Double Eurocard 233x160mm (9.2x6.3")	x	x

Ordering Information

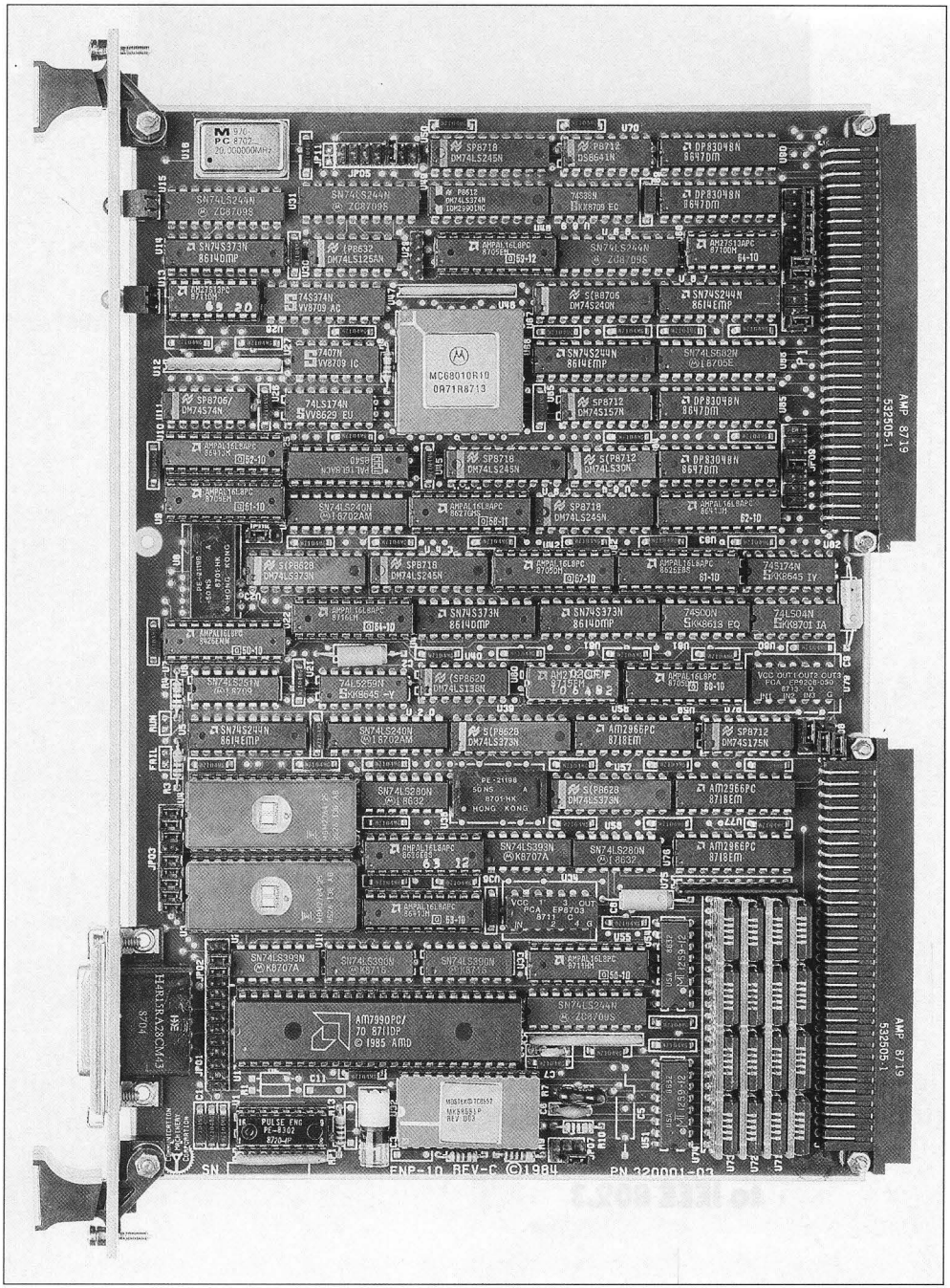
SYS68K/ASCU-1 Part No. 700006	System Control Unit including HUM
SYS68K/ASCU-2 Part No. 700007	System Control Unit with IEEE 488 Interface and Interrupt Generator for 8 independent interrupts. HUM included.
SYS68K/ASCU-1/2 HUM Part No. 800047	Hardware User's Manual for ASCU-1 and ASCU-2.



System 68000 VME SYS68K/ILANC-1

Intelligent Ethernet Controller

- 68010 CPU (10 MHz)
- 512 Kbyte of Dual Access DRAM
- Local Area Network Controller for Ethernet (LANCE)
- Ethernet Compatibility, Conforming to IEEE 802.3


AMP 8719
532505-1
AM7990PC/
70 8711DP
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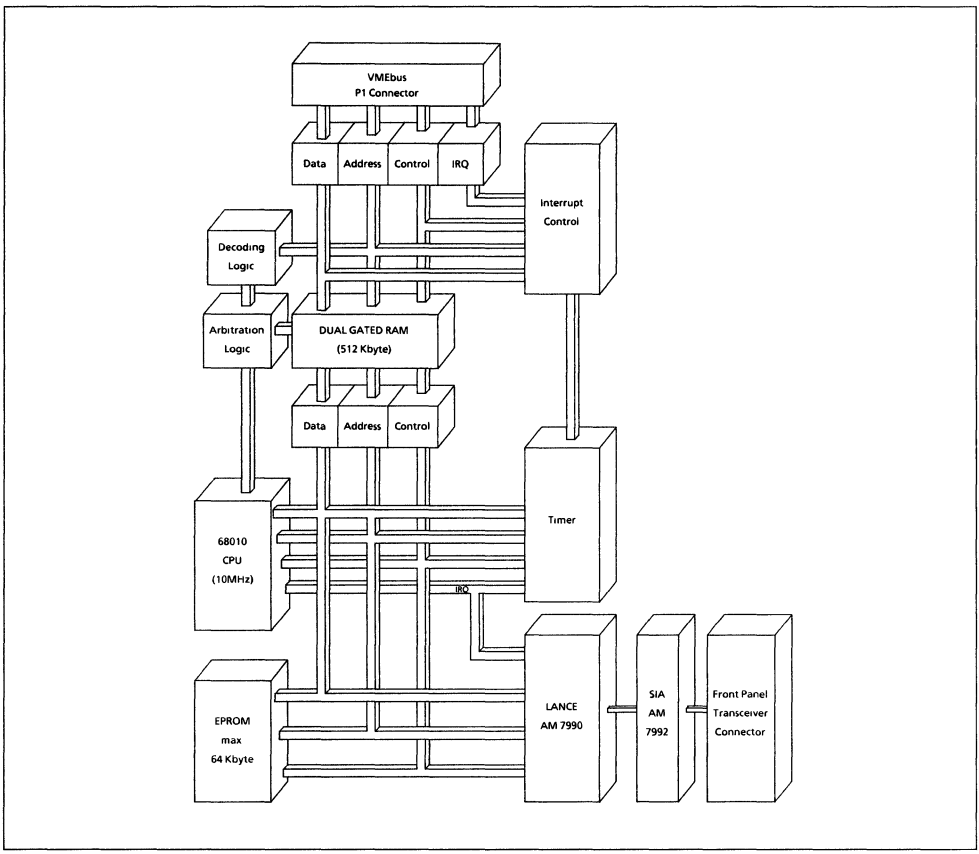
PN 320001-03

1.0 General Description

The SYS68K/ILANC-1 is a high performance communications processor which provides a physical electrical interface to 10 Mbit CSMA/CD network conforming to IEEE 802.3 or Ethernet and a VMEbus based computer system. The SYS68K/ILANC-1 is a complete single card microprocessor subsystem with a VLSI network interface, PROM and DRAM for protocol processing code and a data buffering and a VMEbus interface.

BLOCK DIAGRAM OF THE SYS68K/ILANC-1



2.0 Features:

- 10 MHz MC68010 Microprocessor Unit
- 512 Kbyte dual access DRAM with parity and no wait states to MPU
- Up to 64 Kbyte EPROM (2 sockets)
- VMEbus (IEEE 1014) A24:D16 master, slave and interrupter interface for host to ILANC-1 communications
  - Memory mapped RWD requestor access to VMEbus allows MPU to move data to or from host
  - VMEbus mapped slave access to ILANC-1 DRAM allows host to move data or access software control structures
  - VMEbus interrupter with programmable vector
  - Host signalling interrupt to MPU via a host access to ILANC-1
- Node address PROM contains a world wide unique Ethernet address issued by the Xerox Corporation
- A 2 ms timer interrupts the MPU for protocol software timing
- Local Area Network Controller for Ethernet (LANCE)
  - Descriptor ring buffer management
  - DMA to shared local DRAM
  - Line access protocol (CSMA/CD)
  - Extensive diagnostics and error reporting to MPU
- Serial Interface adaptor
  - Manchester encoding/decoding
  - Transceiver cable interface
- Ethernet compatibility, conforming to Ethernet 1.0, 2.0 or IEEE 802.3

3.0 The Hardware Functions

The local CPU reacts to commands and parameters within the 512 Kbyte of dual access DRAM, it moves the data, processes network protocols and performs DMA transfers across the bus. The SYS68K/ILANC-1 appears as memory to the host operating system, where communication is handled by a standard I/O driver. Compatibility is enhanced by strict conformance to Ethernet 1.0, 2.0 or IEEE 802.3.
Ethernet interfacing is accomplished by cable interconnections between the ILANC-1 transceiver connector and the associated Ethernet transceiver equipment.

3.1 The Local 68010 CPU

The on-board processor is a 10 MHz 68010 CPU. The CPU is responsible for the command and data transfer to and from the on-board memory, response to and generation of bus interrupts, execution of the network communications protocol upper layers, timer functions and running self-diagnostics on power up or initialization. In order to do this, the CPU has access to two 28 pin EPROMs with capacity for a maximum of 64 Kbyte of firmware.

3.2 The Dual Access DRAM

The SYS68K/ILANC-1, in its standard configuration, includes 512 Kbyte of dual access DRAM with parity causing no wait state when accessed from on-board CPU. The DRAM is accessible from the CPU, the LANCE and from the VMEbus. The VMEbus access has the highest priority, followed by the LANCE and the on-board CPU with the lowest priority. Because of the speed of the Ethernet data rate (10 Mbit/sec) the memory buffers accessed by the LANCE have to reside on the ILANC-1 DRAM area. The LANCE performs eight word data bursts when writing received Ethernet data to memory or reading data from memory to send on to Ethernet.

3.3 The Local Area Network Controller for Ethernet

The Local Area Network Controller for Ethernet (LANCE) chip set consists of a DMA-oriented link layer controller (Am 7990) and a Serial Interface Adapter (SIA), the Am 7992. The SIA provides proper IEEE 802.3 or Ethernet 1.0 transceiver interface levels and signalling and the TTL signals to the LANCE. It performs Manchester encoding/decoding necessary for interfacing LANCE to Ethernet. The LANCE features the Ethernet 10 Mbit/sec data rate, a DMA Controller with 24 bit addressing, a sophisticated buffer management structure, the CSMA/CD (Carrier Sense Multiple Access/Collision Detect) network access algorithm and extensive error reporting. The LANCE implements the full CSMA/CD network access algorithm. Upon detection of a collision, it sends a jam signal, followed by a back off algorithm, before attempting to transmit again.

3.4 The VMEbus Interface

A fully VMEbus Rev. C/IEEE 1014 compatible interface is installed on the SYS68K/ILANC-1 to allow an access to the dual access DRAM.
The 16 bit data width (D16, D8) of the DRAM and the decoding of the standard address range (A24) allows easy installation in all VMEbus environments.
During power up and after RESET has been executed the SYS68K/ILANC-1 first executes a selftest and initializes all on-board devices.
Special registers on the SYS68K/ILANC-1 enable a host CPU to send interrupts to the ILANC-1.

4.0 The Handling Firmware

The SYS68K/ILANC-1 intelligent Ethernet Controller board operates under the control of the local handling firmware.
The firmware allows down-loading directly over the VMEbus from the host, and gathers running statistics on all conditions reported by LANCE. In addition, the firmware manages the LANCE status registers and and descriptor rings, performs timer functions and manages interrupts, allowing protocol software to be written in a high level language such as C or PASCAL.

Specifications of the SYS68K/ILANC-1

Local CPU	68010 CPU with 10 MHz clock frequency
Ethernet Interface	Am 7990 LANCE and AM 7992 Serial Interface Adaptor
EPROM Interface	64 Kbyte maximum capacity
Dual Access DRAM	512 Kbyte capacity using DRAMs, no wait state operation from local CPU
VMEbus Interface	Fully Rev. C/IEEE 1014 compatible slave interface A:24D16 mode
Handling Firmware	In EPROM with support for LANCE and SIA
Power Requirements	+ 5V : 4.4A typ +12V : 0.6A typ
Operating Temperature	5 to 50 Degrees C
Storage Temperature	−40 to 85 Degrees C
Relative Humidity	5 to 95% (non condensing)
Dimensions	233 x 160 mm 9.3 x 6.3 in

Ordering Information

SYS68K/ILANC-1 Part No. 300100	Intelligent Ethernet Controller, including firmware and documentation
SYS68K/ILANC-1/UM Part No. 800149	User's Manual for the ILANC-1

I/O Boards

FORCE Computers Serial and Parallel I/O Board Introduction

FORCE Computers offers a full selection of general purpose I/O boards that satisfies most general purpose application needs for both serial and parallel I/O. The family includes not only dumb serial I/O boards but also considerable intelligence and the obvious performance advantages offered by the ISIO family.

General Feature Overview

For general purpose parallel I/O, look no further than the SYS68K/PIO-1. This board offers four 8 bit interface channels provided by the four 68230 parallel interface and timer chips installed on the board. The board offers four 8 bit parallel output ports and four opto-coupled 8 bit parallel input ports. Both the input and the output ports offer two handshake signals each. The PIO-1 is the general purpose parallel I/O solution.

If your application also requires a DMA controller on your parallel I/O board or the facility of being totally opto-isolated from the interface, then the SYS68K/OPIO-1 board may be the board for you. This board also offers four 8 bit parallel interfaces via four 68230 parallel interface and timer chips. The board additionally offers full opto isolation (1000V) on both the input and the output channels. As an added feature, a 4 channel DMA controller is installed on the board to allow high speed data transfers to/from VMEbus memory and the 68230 PI/T chips.

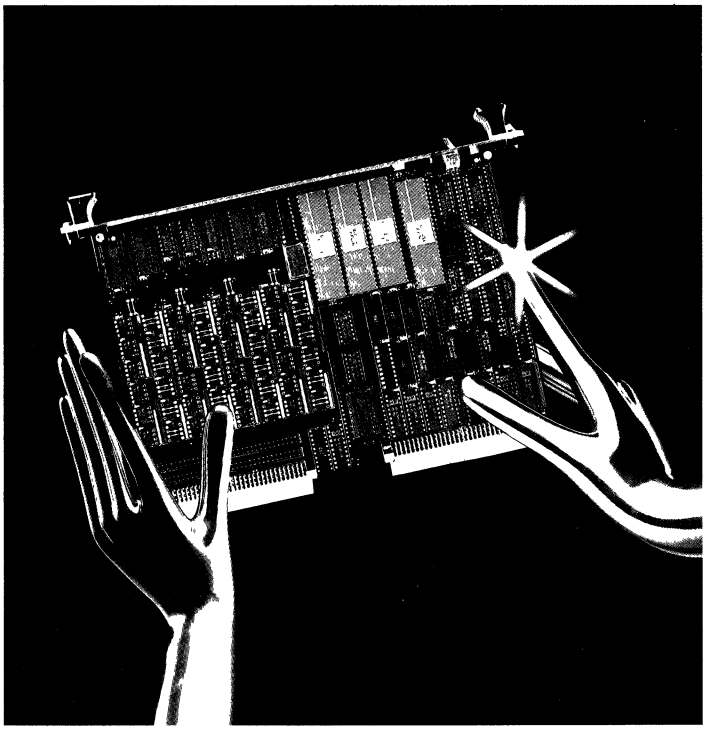
For general purpose serial I/O applications, the SYS68K/SIO-2 board offers 6 channels, configurable for either RS232 or RS422 communication. Available baud rates are from 110-38.4K and all synchronous and asynchronous protocols are supported. If serial optical links are required, then the SYS68K/SIO-2A board provides two interfaces to optical fibre serial links as an extra feature for two of the serial channels. These interfaces provide high security, high reliability and data integrity over a serial interface.

For intelligent serial I/O interfaces, the SYS68K/ISIO-1 and the SYS68K/ISIO-2 boards provide no wait state performance. This family of boards provides high performance serial I/O specifications using the 68010 (10 MHz) to provide the on board intelligence. The processor in both designs runs constantly without inserting wait states from the on board RAM. The ISIO-1 and the ISIO-2 have 128 Kbyte of on board memory while the ISIO-1A and the ISIO-2A have 512 Kbyte of on board memory. The ISIO-2 family may be configured to communicate using the RS232 or the RS422 communication standards while the ISIO-1 family only supports the RS232 standard. The ISIO-1/2 family are the intelligent serial communication solution.

Parallel I/O Boards

FAMILY	PIO-1	OPIO-1
No. of Output Signals Interface Type Isolation Voltage Propagation Delay (max.)	32 TTL (64 mA) 5V 10 ns	32 Opto Coupled (30 mA) 1000V 50 ns
No. of Input Signals Interface Type Isolation Voltage Propagation Delay (max.)	32 Opto Coupled 1000V 50 ns	32 Opto Coupled 1000V 50 ns
No. of Parallel Ports Input Output No. of Handshake Signals per Port	4 x 8 bit 4 x 8 bit 2	4 x 8 bit 4 x 8 bit 2
No. of Timers (24 bit + 5 bit Prescaler)	4	4
Used Parallel Interface Chips	68230 (4 x)	68230 (4 x)
No. of Different IRQs No. of Different IRQ Vectors IRQ-Level to the VMEbus	8 8 1 (fixed)	8 8 1-7 (SW Programmable)
DMA Controller Clock Frequency Data Transfer Capability	– – –	68450 8 MHz 8, 16 bit
Detailed Description on Page:	367	373

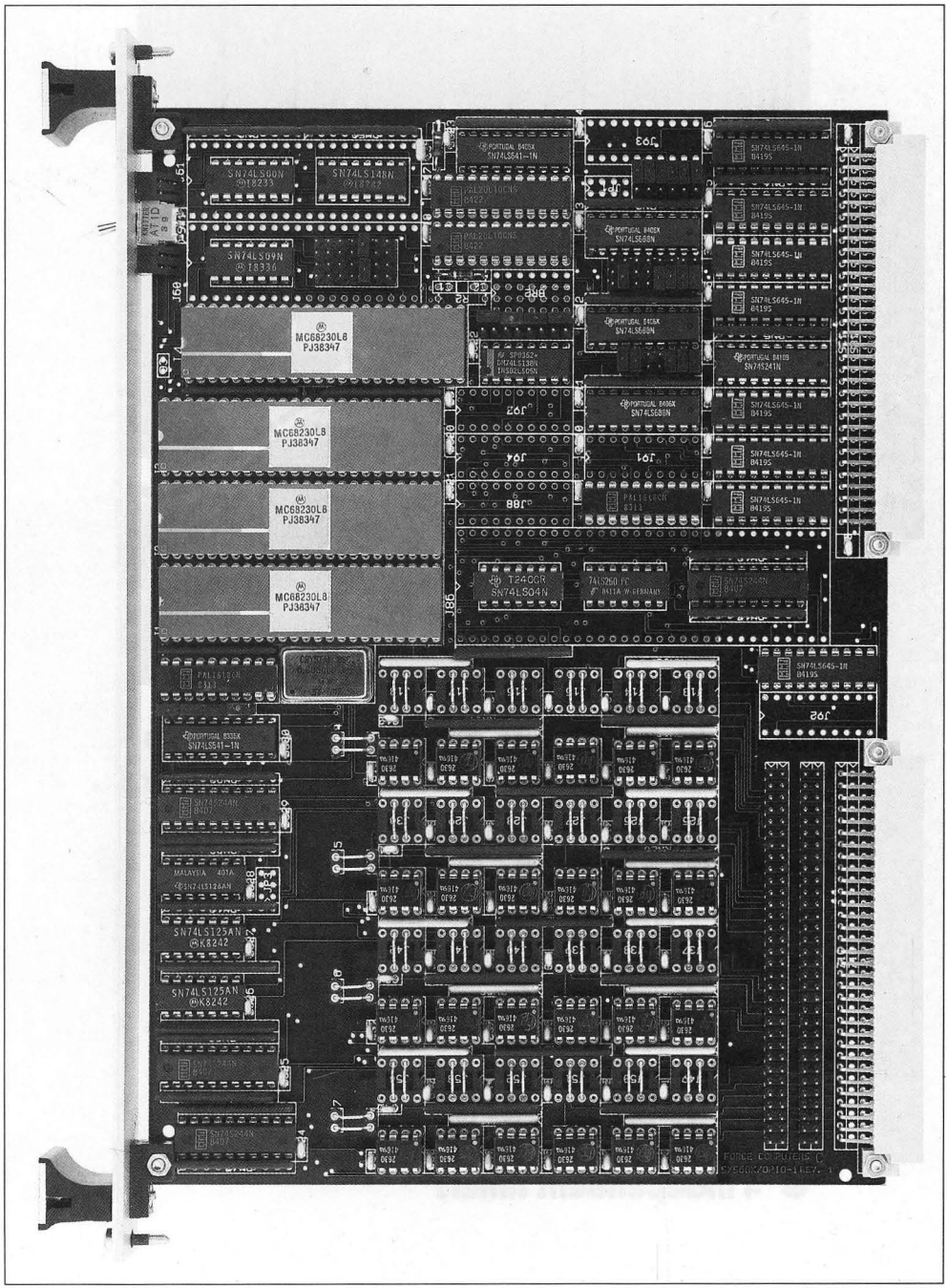
FAMILY	SIO-1	SIO-2	SIO-2A	ISIO-1	ISIO-1A	ISIO-2	ISIO-2A
No. of Ports Synchronous/Asynchronous RS232 RS422 Baud Rate	Not recommended for new designs.	6 yes 6 6 110-38K	6 yes 6 6 110-38K	8 yes 8 – 110-38K	8 yes 8 – 110-38K	8 yes 8 8 110-38K	8 yes 8 8 110-38K
Used Controller Chips		68561 (6x)	68561 (6x)	68562 (4x)	68562 (4x)	68562 (4x)	68562 (4x)
No. of different Interrupt Vectors to VME			18	4	4	4	4
Processor Type Frequency		– –	– –	68010 10 MHz	68010 10 MHz	68010 10 MHz	68010 10 MHz
RAM Type RAM Capacity No. of Wait States Dual Ported RAM Capacity		– – – –	– – – –	SRAM 128 Kbyte 0 128 Kbyte	SRAM 512 Kbyte 0 512 Kbyte	SRAM 128 Kbyte 0 128 Kbyte	SRAM 512 Kbyte 0 512 Kbyte
EPROM Capacity		–	–	128 Kbyte	128 Kbyte	128 Kbyte	128 Kbyte
Intelligent Spooler Capability		no	no	yes (64 Kbyte)	yes (64 Kbyte)	yes (256 Kbyte)	yes (256 Kbyte)
Optical Links		–	yes (2)	–	–	–	–
Detailed Description on Page:		379	379	385	385	395	395



System 68000 VME
SYS68K/PIO-1

Multi Channel Parallel I/O Board

- 4 independent input ports (8 bit each)
- 4 independent output ports
  (8 bit each, 64mA max. drive current)
- TTL compatible ports
- 2 handshake signals per port
- 4 independent timers


SN74LS00N
SN74LS14N
SN74LS09N
MC68230L8
PJ38347
MC68230L8
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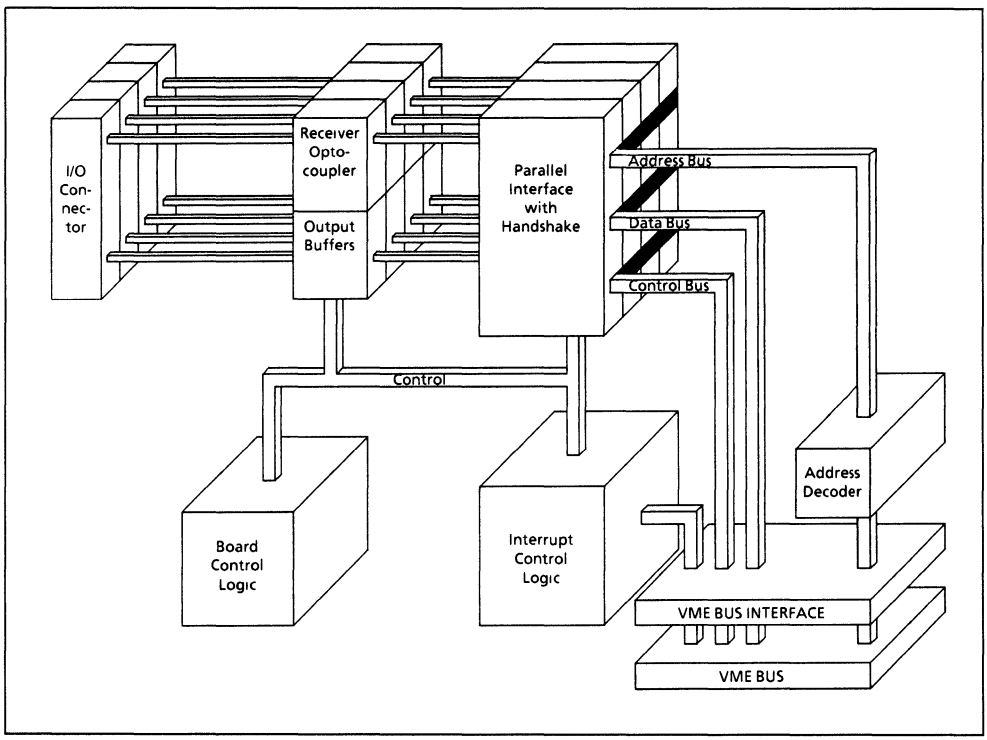
MC68230L8
PJ38347
SN74LS541-1N
SN74LS645-1N
SN74LS08N
SN74LS241N
T240CR
SN74LS04N
74LS260 FC
SN74LS125AN
SN74LS125AN
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10

General Description
The SYS68K/PIO-1 is a high performance interface board based on the VMEbus. Four interface units provide four input and four output channels, each 8 bit wide.
Each input signal is opto coupled, providing current sensing. Each output signal is driven by TTL buffers.

To allow fully asynchronous operation of the SYS68K/PIO-1, each parallel interface and timer module (PI/T) can force handshake or timer interrupts to the VMEbus. The interrupt vectors are software programmable, the level is jumper selectable.

FEATURES OF THE SYS68K/PIO-1
- 4 TTL buffered 8 bit parallel output ports with 2 handshake signals per port.
- 4 opto-coupled 8 bit parallel input ports with 2 handshake signals per port.
- 4 timers (24bit).
- Interrupt capabilities:
  4 timer interrupts
  4 I/O handshake interrupts
  Each interrupt has a software programmable vector.
- Jumper selectable Access Address and Address Modifier Code.
- Fully VMEbus compatible.
- RUN/LOCAL function switch.
- RUN/LOCAL indicators.

BLOCK DIAGRAM OF THE SYS68K/PIO-1



Global Operation
The SYS68K/PIO-1 is a parallel I/O board designed to communicate fully asynchrounus from the VMEbus to the outside world.
Four 8 bit input and four 8 bit output ports are provided on the board.

1. The Parallel Ports
The parallel I/O is designed with Parallel Interface and Timer modules (PI/T 68230). The clock frequency is 8 MHz.
Each PI/T includes the following features:
- All registers are Read/Write and directly addressable
- Special port interrupt service request
- 4 different interrupt vectors for the port interrupts
- 8 bit output port
- 8 bit input port
- Selectable handshaking modes

All input and handshake input signals are routed to high speed opto coupler (HCPL2630) to provide current sensing. The typical propagation delay of each opto coupler is 50ns.
Each I/O channel with the 2 ports contains a separate power supply input where the opto coupler supply voltage can be connected.
In addition, the standard power fo the VMEbus (+5V) can be used to drive the opto coupler.
Each I/O signal is available through two 64 pin I/O connectors or through the 64 pin DIN connector (P2).
The SYS68K/PIO-1 can operate in a 16 bit parallel mode because two PI/T devices are on the lower data bus (D0-D7) and two devices are connected to the upper data bus (D8-D15). This allows a parallel transfer of 16 bit data with a common handshake.

2. The Timer Operation
Each PI/T device contains a 24 bit timer capable of generating an interrupt. Therefore 4 different timer interrupts can be generated from the SYS68K/PIO-1.

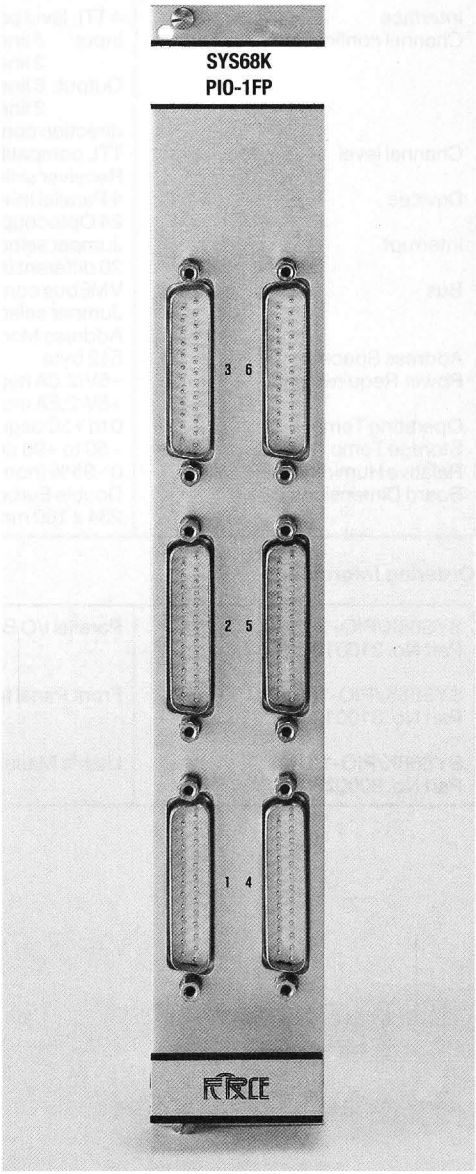
3. The Interrupt Structure
The four PI/T port service request and timer interrupt request outputs are gated to drive one jumper selectable request level on the VMEbus. The port service request interrupt has four software programmable vectors, and the timer interrupt has one software programmable vector per PI/T. 20 software programmable interrupt vectors are provided for by the SYS68K/PIO-1.

4. The Addressing
The SYS68K/PIO-1 contains a flexible address and address modifier decoding logic. The access address and the address modifier code are jumper selectable (A24 or A16 mode). Therefore, both standard and the Short I/O addressing modes are supported.

SYS68K/PIO-1FP

Front Panel with 6 I/O Connectors

The SYS68K/PIO-1FP is a double-wide (12HE/8TE) front panel, providing six 25-pin D SUB male connectors, each with flat cable and connectors to the SYS68K/PIO-1 I/O-channel ports.
The connectors 1, 2, 3 and 4 are each supplied with two 14-pin connectors on the other end of the flat cable, for the bidirectional channel configuration. The connectors 5 and 6 are each mounted with one 14-pin connector. The assignment of the connector to the I/O channels is user selectable, as well as the individual configuration of the bidirectional I/O ports or separate input and output ports.

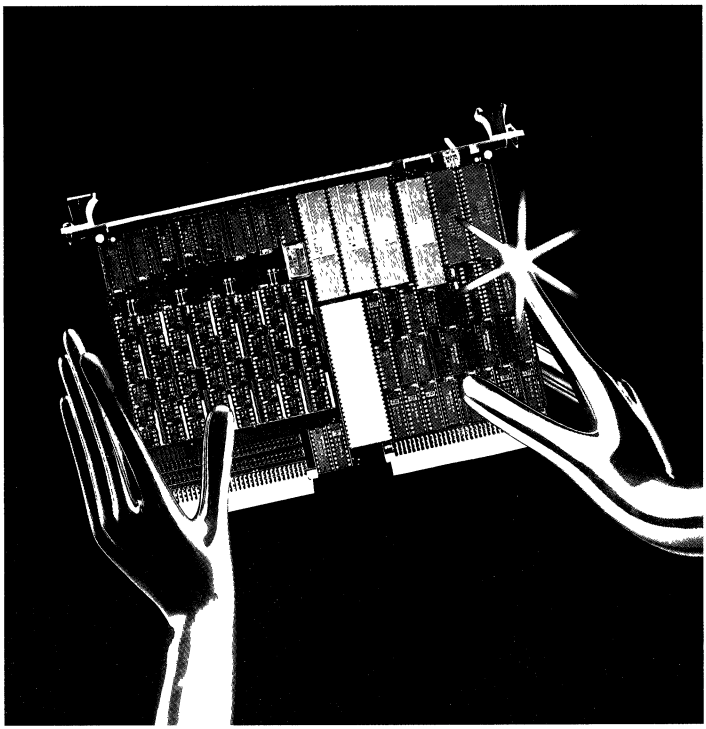


SYS68K/PIO-1 Specifications

Interface	4 TTL level parallel I/O channels
Channel config.	Input: 8 lines data 2 lines handshake Output: 8 lines data (64 mA sink) 2 lines handshake direction control
Channel level	TTL compatible voltage Receiver sinks 8mA for logic 0
Devices	4 Parallel Interface/Timer (68230) 24 Optocouplers (HCPL2630)
Interrupt	Jumper selectable interrupt request level 20 different interrupt vectors possible
Bus	VMEbus compatible (A24:D16/A16:D16) Jumper selectable board base address Address Modifier decoding
Address Space	512 byte
Power Requirements	+5V/2.0A (typ) +5V/2.5A (max)
Operating Temp.	0 to +50 degrees C
Storage Temp.	−50 to +90 degrees C
Relative Humidity	0−95 % (non-condensing)
Board Dimensions	Double Eurocard 234 x 160 mm (9.2 x 6.3")

Ordering Information

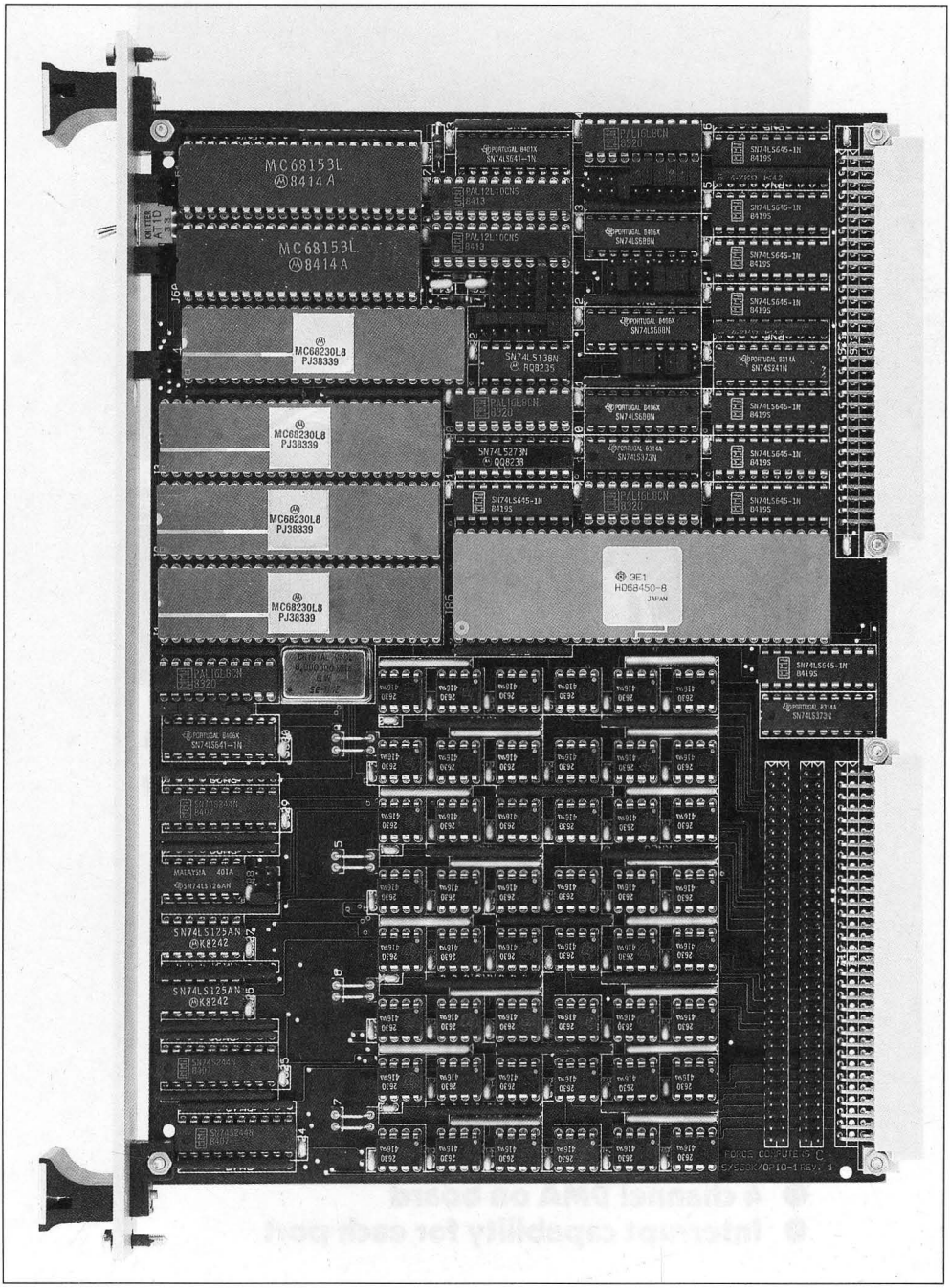
SYS68K/PIO-1 Part No. 310010	Parallel I/O Board including User's Manual.
SYS68K/PIO-1FP Part No. 310012	Front Panel for the Parallel I/O Signals
SYS68K/PIO-1/UM Part No. 800028	User's Manual for the SYS68K/PIO-1 Board.



System 68000 VME SYS68K/OPIO-1

Multi Channel Opto Isolated Parallel I/O Board

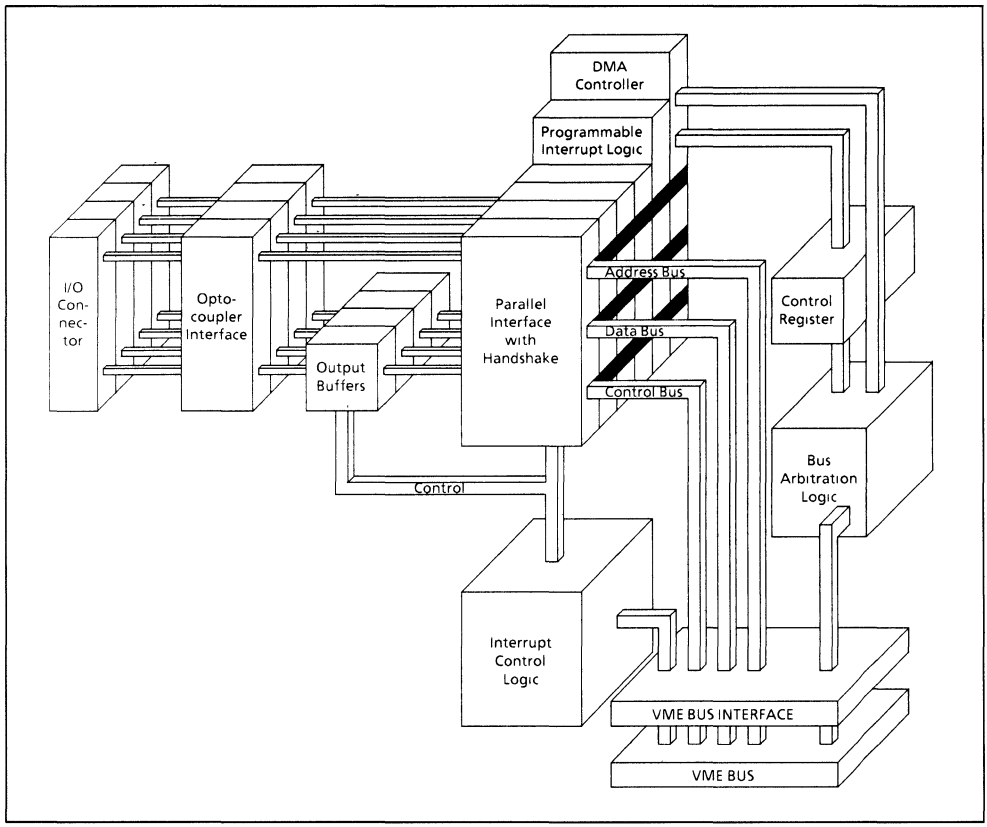
- 4 opto isolated (1000V) input ports (8 bit each)
- 4 opto isolated (1000V) output ports (8 bit each)
- 4 channel DMA on board
- Interrupt capability for each port


MC68153L
8414A
MC68153L
8414A
MC68230L8
PJ38339
MC68230L8
PJ38339
MC68230L8
PJ38339
MC68230L8
PJ38339
SN74LS138N
SN74LS273N
SN74LS125AN
SN74LS125AN
SN74LS645-1N
SN74LS373N
SN74LS241N
PAL16L8CN
PAL12L10CNS
SYS68K/OPIO-1 REV 1

General Description
The SYS68K/OPIO-1 is a high performance interface board based on the VMEbus. Four interface units provide four input and four output channels, each 8 bit wide.
Each input and output signal is opto coupled to provide maximum flexibility. For high speed data transfers, a four channel DMA controller is provided on the board.
To allow fully asynchronous operation of the SYS68K/OPIO-1, each parallel interface and timer module (PI/T) can force handshake or timer interrupts to the VMEbus. The interrupt vector and the level are both software programmable.

FEATURES OF THE SYS68K/OPIO-1
- 4 opto isolated 8 bit parallel output ports with 2 handshake signals per port (opto isolated).
- 4 opto isolated 8 bit parallel input ports with 2 handshake signals per port (opto isolated).
- 4 different opto-isolated areas for the parallel ports (1000V).
- Direct Memory Access Controller for high speed DMA transfers. Directly coupled to the I/O ports.
- Full VME Slave bus arbitration for the DMAC.
- 4 Timers (24 bit).
- Interrupt capabilities:
  4 timer interrupts
  4 I/O handshake interrupts
  1 DMA controller interrupt
  Each interrupt has a software programmable vector and level (1-7).
- Control Register, performs flexible Bus Release functions (RWD, ROR, RAT).
- Jumper selectable Access Address and Address Modifier Code.
- Fully VMEbus compatible.
- RUN/LOCAL function switch.
- RUN/LOCAL and DMA Busy indicators.

BLOCK DIAGRAM OF THE SYS68K/OPIO-1



Global Operation
The SYS68K/OPIO-1 is a high-speed parallel I/O board designed to communicate fully asynchronous from the VMEbus to the outside world.
Four 8bit input and four 8bit output ports are provided on the board.

1. The Parallel Ports
The parallel I/O is designed with Parallel Interface and Timer modules (PI/T 68230). The clock frequency is 8 MHz.
Each PI/T includes the following features:
- All registers are Read/Write and directly addressable
- Special port interrupt service request
- 4 different interrupt vectors for the port interrupts
- 8 bit output port
- 8 bit input port
- Selectable handshaking modes

All I/O and handshake signals are routed to high speed opto coupler (HCPL 2630) to provide maximum flexibility of the voltage ranges. The typical propagation delay of each opto coupler is 50 ns.
Each I/O channel with the 2 ports contains a separate power supply input where the opto coupler supply voltage can be connected.
In addition, the standby power of the VMEbus (+5V) can be used to drive the opto coupler.
Each I/O signal is available through two 64 pin I/O connectors or through the 64 pin DIN connector (P2).
The SYS68K/OPIO-1 can operate in a 16bit parallel mode because two PI/T devices are on the lower data bus (D0-D7) and two devices are connected to the upper data bus (D8-D15). This allows a parallel transfer of 16bit data with a common handshake.

2. The DMA Controller
The 4 channel DMA Controller (68450) has a clock frequency of 8 MHz. The maximum data transfer rate is 4 Mbyte/second.
Each PI/T device is connected to a request input of the DMA Controller. Therefore, a maximum of flexibility for the parallel I/O is provided through the internal DMA Controller structure.
Features of the DMAC:
- 4 independent DMA channels
- Array-Chained and Linked-Array-Chained Operations
- 72 Registers for complete software control
- Interface Lines that provide for Requesting and Acknowledging
- Programmable channel prioritization
- 2 vectored interrupts for each channel
- Auto-Request and External-Request Transfer Mode
- Up to 2 Mbyte/second transfer rate

For easy installation of the SYS68K/OPIO-1 into a system, the board contains different bus release functions:
Release When Done (RWD)
Release on Request (ROR)
Release after Time-out (RAT)
The RAT function and the ROR function are software programmable through the on-board Control-Register.
The RAT function contains eight different time-out values (6 μs to 800 μs) wich are software programmable.
The DMA Controller can operate on the VMEbus in the following transfer modes:
- OPIO to Memory
- Memory to OPIO
- Memory to Memory

For the DTB mastership, the board contains a full slave bus arbitration with a strap selectable level (0-3).

3. The Timer Operation
Each PI/T device contains a 24 bit timer capable of generating an interrupt. Therefore 4 different timer interrupts can be generated from the SYS68K/OPIO-1.

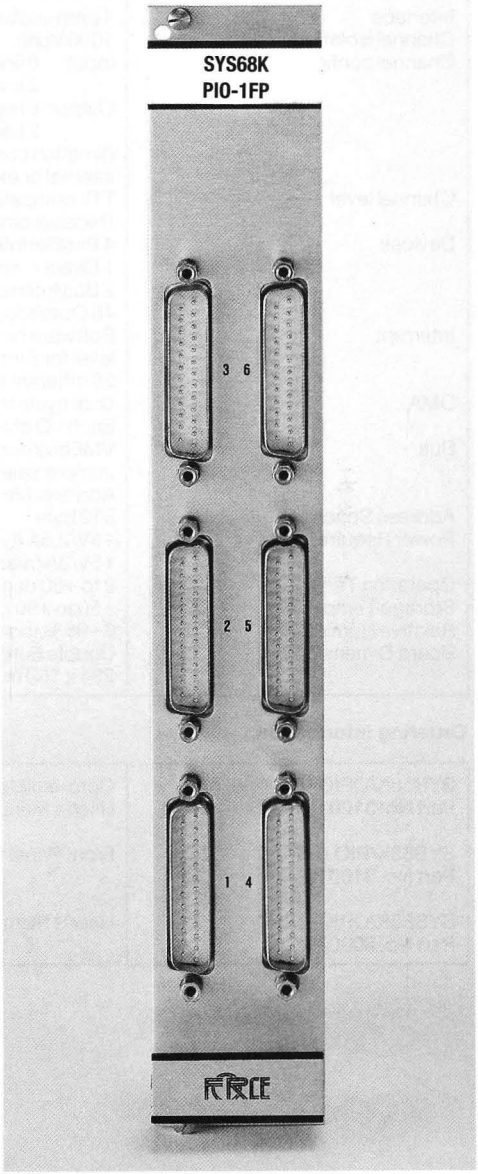
4. The Interrupt Structure
The PI/T devices and the DMA Controller can generate interrupts. These interrupt request signals are used as an input for the two Bus Interrupter Modules (BIM 68153). The BIM contains different registers. These registers are Read/Writeable and describe which interrupt request levels are assigned to the IRQ inputs.
This structure allows for each PI/T port service request and timer interrupt request, a variable interrupt level definition, and vector generation.

5. The Addressing
The SYS68K/OPIO-1 contains a flexible address and address modifier decoding logic. The access address and the address modifier code are jumper selectable (A24 or A16 mode). Therefore, both standard and the Short I/O addressing modes are supported.
For DMA transfers on the VMEbus, the board contains a register set which contains all possible address modifier combinations (A24 and A16).

SYS68K/PIO-1FP

Front Panel with 6 I/O Connectors

The SYS68K/PIO-1FP is a double-wide (12HE/8TE) front panel, providing six 25-pin D SUB male connectors, each with flat cable and connectors to the SYS68K/PIO-1 I/O-channel ports.
The connectors 1, 2, 3 and 4 are each supplied with two 14-pin connectors on the other end of the flat cable, for the bidirectional channel configuration. The connectors 5 and 6 are each mounted with one 14-pin connector. The assignment of the connector to the I/O channels is user selectable, as well as the individual configuration of the bidirectional I/O ports or separate input and output ports.

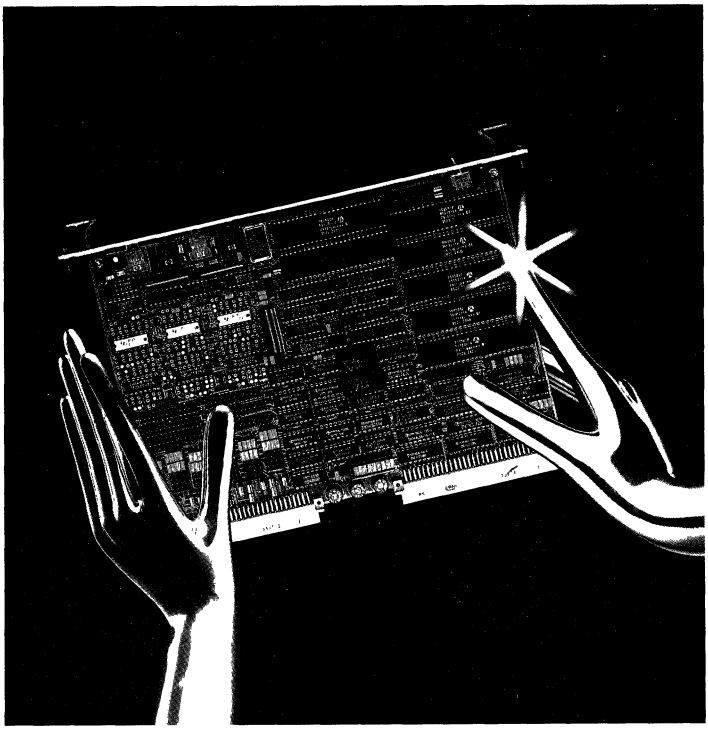


SYS68K/OPIO-1 Specifications

Interface	4 opto-isolated TTL level parallel I/O channels.
Channel isolation	1000 Volts.
Channel config.	Input: 8 lines data 2 lines handshake Output: 8 lines data 2 lines handshake direction control internal or external GND and VCC (+5V)
Channel level	TTL compatible voltage Receiver sinks 8mA for logic 0.
Devices	4 Parallel Interface/Timer (68230) 1 Direct Memory Access Controller (68450) 2 Bus Interrupter Module (68153) 48 Optocouplers (HCPL2630)
Interrupt	Software programmable interrupt request level for 8 interrupts individually. 28 different interrupt vectors possible
DMA	Dual cycle transfers as bus master. Each I/O channel can request the DMAC
Bus	VMEbus compatible (A24:D16/A16:D16) Jumper selectable board base address Address Modifier decoding
Address Space	512 byte
Power Requirements	+5V/2.5A (typ) +5V/3A (max)
Operating Temp.	0 to +50 degrees C
Storage Temp.	−50 to +90 degrees C
Relative Humidity	0−95 % (non-condensing)
Board Dimensions	Double Eurocard 234 x 160 mm (9.2 x 6.3 inch)

Ordering Information

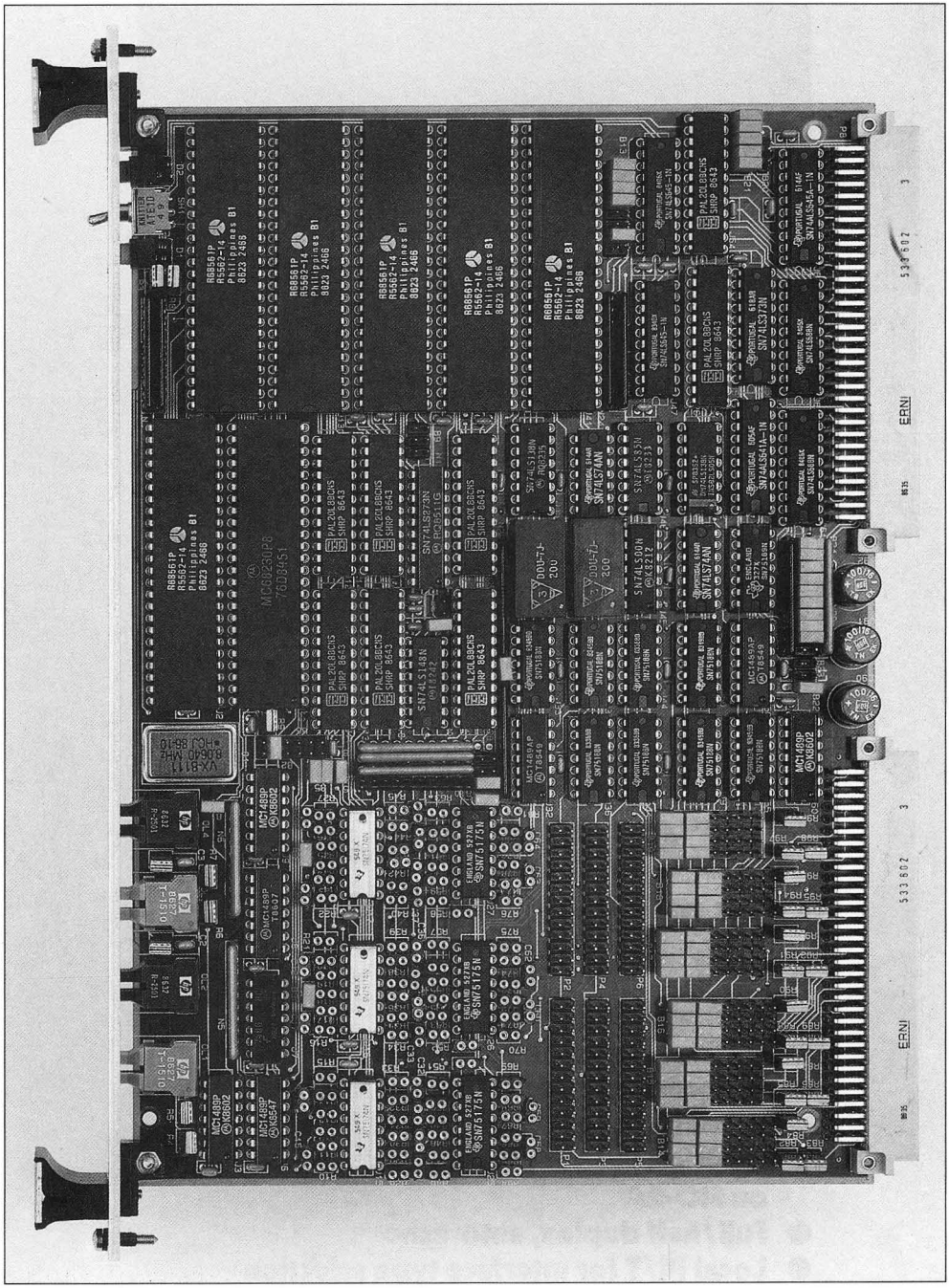
SYS68K/OPIO-1 Part No. 310011	Opto-isolated paralell I/O Board including User's Manual.
SYS68K/PIO-1FP Part No. 310012	Front Panel for the Parallel I/O Signals
SYS68K/OPIO-1/UM Part No. 800029	User's Manual for the SYS68K/OPIO-1 Board.



System 68000 VME SYS68K/SIO-2/2A

Multi Protocol Serial I/O Controller Board

- 6 serial I/O channels
- Software programmable baud rate
- Asynchronous/synchronous receiver/ transmitter functions (RS-232/RS422)
- 2 optical links for serial transmission on SIO-2A
- Full/half duplex, auto-echo
- Local PI/T for interface type selection



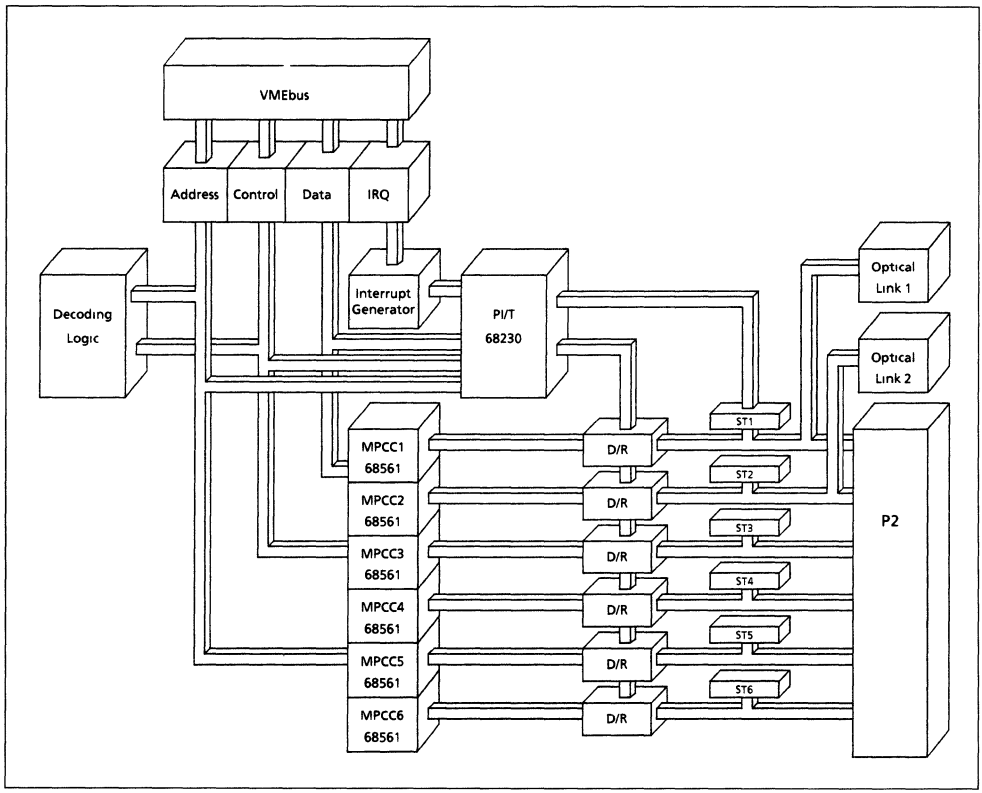
General Description

The SYS68K/SIO-2 board contains six serial I/O channels based on the Multi-Protocol Communications Controllers (MPCC) used for each channel, with its asynchronous or synchronous protocols and the 8 character receiver and transmitter buffer register.
Each MPCC is able to generate an interrupt to the VMEbus (levels 1–7) and to drive three different interrupt vectors.
The interface to the communication equipment is RS232 or RS422 compatible (free selectable). The SYS68K/SIO-2A offers in addition to the listed hardware protocols, two optical links channels (HFBR-0500).

Features of the SYS68K/SIO-2

- 6 serial I/O channels
- Fully IEEE 1014, VMEbus Rev. C compatible
- Multi-Protocol Communications Controller (68561) for each channel allows:
  - Asynchronous/synchronous receiver/transmitter functions
  - Full/half duplex, auto-echo and local loopback modes
- Protocols:
  - IBM binary synchronous communications in ASCII or EBCDIC format
  - Character Oriented Protocols (COP) BSC, DDCMP, X3.28, X.21, ISO IS1745, ECMA 16, etc.
  - Synchronous Bit-Oriented Protocols (BOP) SDLC, HDLC/ADCCP, X.25 etc.
  - Asynchronous or isochronous mode

BLOCK DIAGRAM OF THE SYS68K/SIO-2A



- Modem handshake interface
- Selectable Parity (enable odd, even) and CRC (control field enable, CRC-16, CCITT, V.41, VRC/LRC)
- 22 directly addressable registers for flexible option selection, complete status reporting and data transfer
- Eight character receiver and transmitter buffer register
- Three separate programmable and maskable interrupt vector numbers for the receiver, transmitter, and serial interface
- Software programmable baud rate from 110 to 38400 baud
- 8 and 16 bit data bus
- A24 and A16 decoding
- Free configurable I/O interface signal assignment through wire wrap areas for each channel.
  5 Drivers (RS232 compatible)
  6 Receivers (RS232 compatible)
  2 Drivers (RS422 compatible)
  2 Receivers (RS422 compatible)
- All I/O signals are routed to the P2 connector
- Local PI/T for interface type selection and deselection of the MPCCs during initialization
- 2 optical links for Transmit and Receive data available on the SYS68K/SIO-2A (up to 50m cable length).
- Free selectable access address and address modifier code of the 6 MPCCs and the PI/T in common
- RUN/LOCAL mode indicated by LEDs

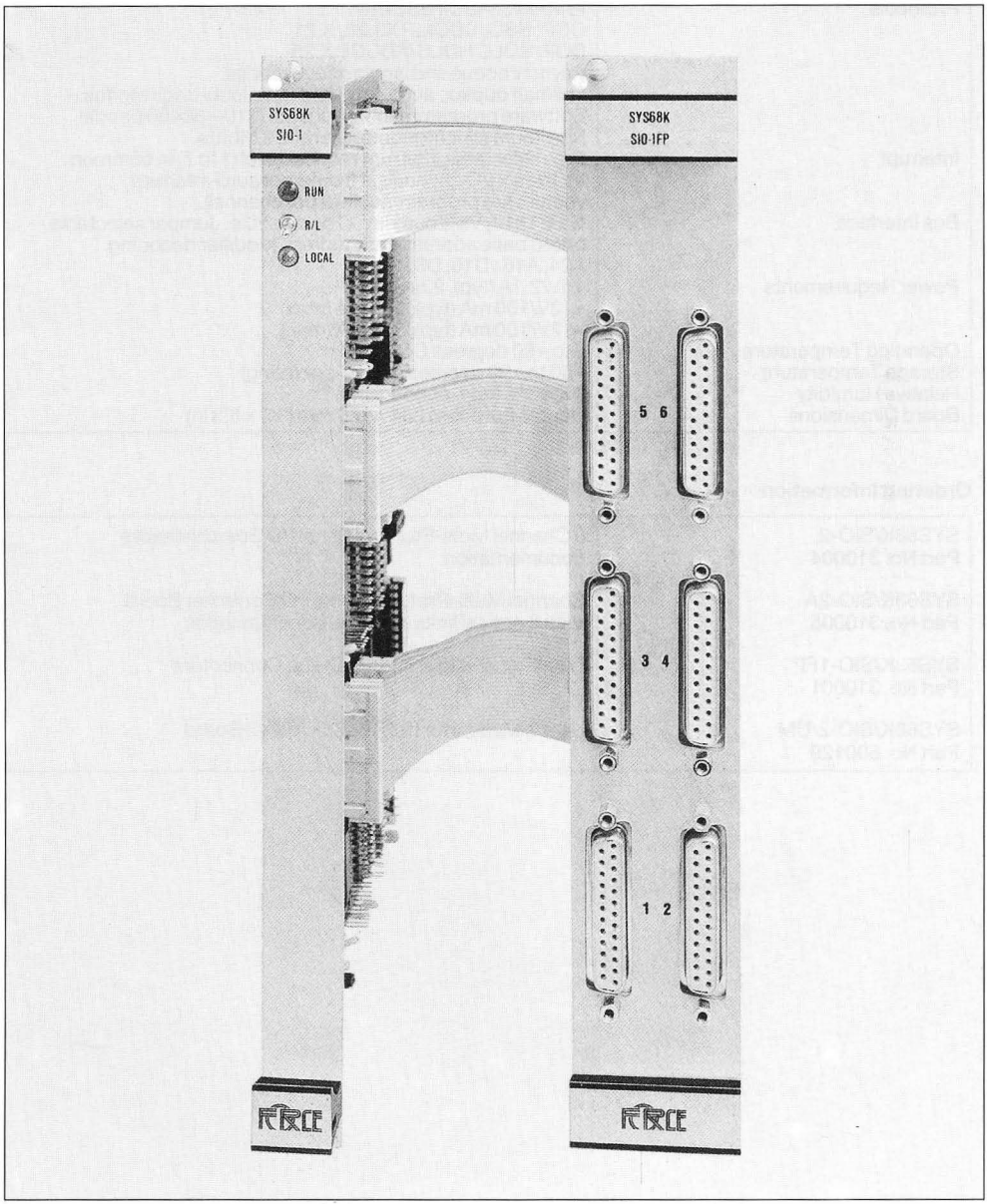
Each MPCC is able to use the listed protocols and communicates with its 8 or 16 bit data bus to the controller module. The internal 8 character receiver/transmitter buffer register (FIFO) reduces the software handling in accordance to the three separate maskable interrupt vector numbers (transmitter, receiver, or handshake interface).
All the MPCCs on the board work fully asynchronous to the VMEbus and respond to the handling CPU on the free jumper selectable access address and address modifier code.

The RUN/LOCAL switch isolates the board from the bus during failures or maintenance. This mode is indicated by two LEDs on the front panel.
Each serial I/O channel contains RS232/RS422 driver (5/2) and receiver (6/2) circuits. Each of the I/O signals is connected to the 26 pin male connector installed on the board to allow the connection of a flat cable. The SYS68K/SIO-1FP offers the connection of six 25 pin D-Sub connectors on a standard front panel as shown on the next page.
In addition to the 26 pin male connectors, all I/O signals are available on a wire wrap area where the user can select the I/O signals to be connected to the P2 connector.
The I/O signal assignment on the P2 connector is compatible to the I/O signal assignment of the SYS68K/ISIO-1/2 boards.

SYS68K/SIO-1FP Description

The SYS68K/SIO-1FP is a doublewide front panel containing six 25-pin D-sub connectors with flat wire cables to be used in conjunction with the SYS68K/SIO-2 multi-protocol serial I/O controller board.

The SYS68K/SIO-1FP allows easy plug-in of the serial I/O ports relieving the user from individual wiring problems in systems applications.

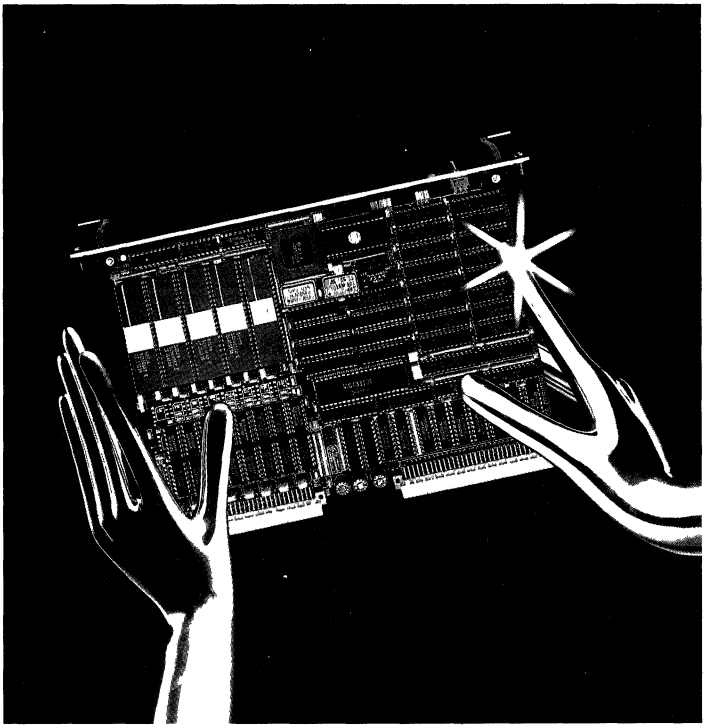


Specification

Interface	6 independent serial I/O channels RS232 or RS422 compatible (jumper selectable)
Optical Link	2 HFBR-0500 data links available on the front panel (only on the SYS68K/SIO-2A)
Communications Controller	6 Multi-Protocol Communications Controller (68561 MPCC)
Protocols	IBM BSC: ASCII EBCDIC COP: BSC, DDCMP X3.28, X.21 BOP: SDLC HDLC/ADCCP X.25 Asynchronous and isochronous modes. Full/half duplex, auto-echo and local loop-back modes. Software programmable baud rate (110 – 38400 baud). Maximum synchronous data rate: 2 Mbit/s
Interrupt	Free selectable interrupt request level (1 to 7) in common for the six I/O channels. 18 different auto-interrupt vectors are programmable (3 per channel).
Bus Interface	IEEE 1014, VMEbus Rev. C compatible. Jumper selectable board base address and Address Modifier decoding. A24, A16 : D16, D8
Power Requirements	+5V/2.1A (typ), 2.5A (max) +12V/100 mA (typ), 300 mA (max) –12V/100 mA (typ), 300 mA (max)
Operating Temperature	0 to +60 degrees CNNL
Storage Temperature	–50 to +90 degrees C (non-operating)
Relative Humidity	0 to 95% (non-condensing)
Board Dimensions	Double Eurocard 234 x 160 mm (9.2 x 6.3 in)

Ordering Information

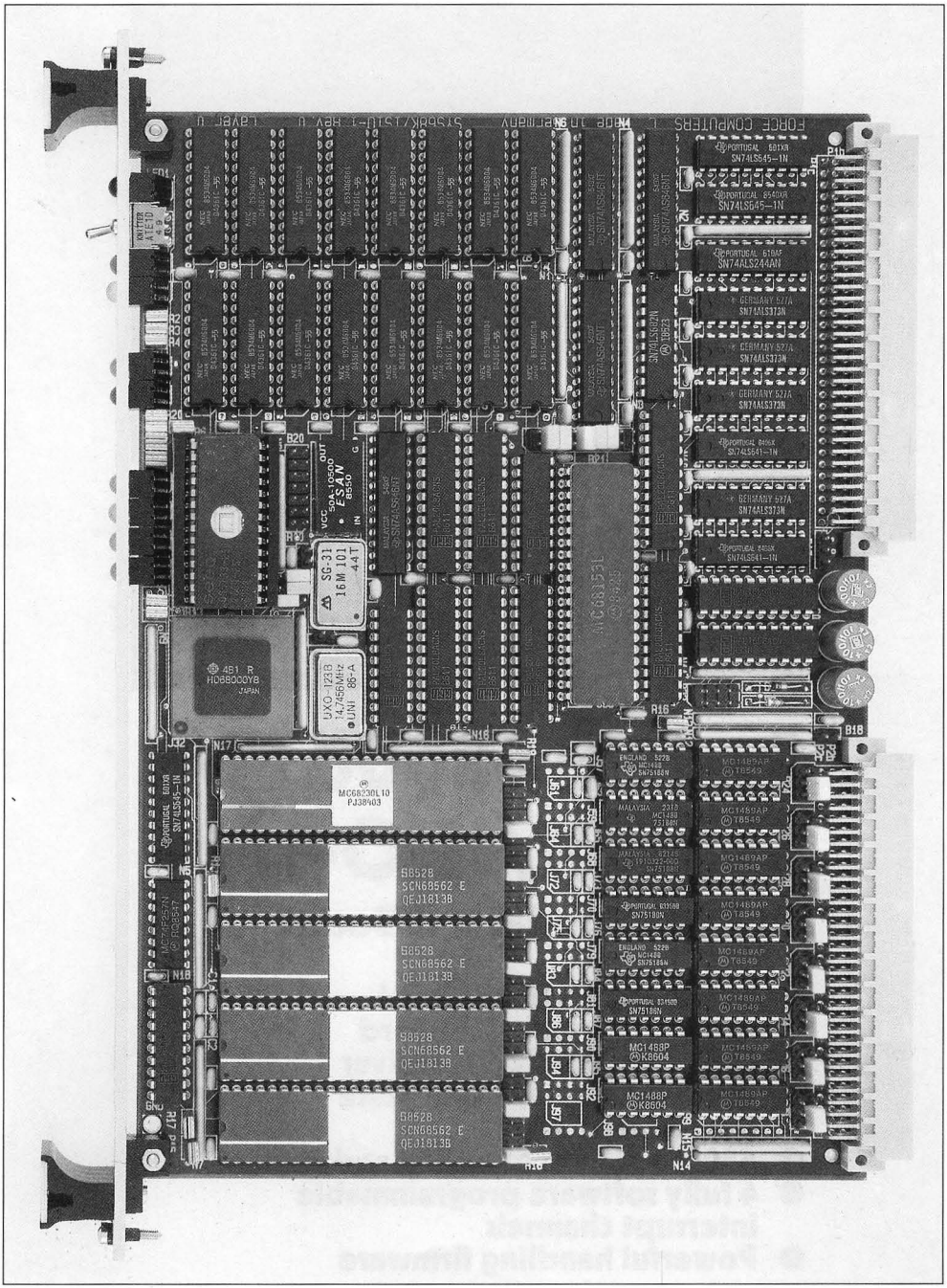
SYS68K/SIO-2 Part No. 310004	6 Channel Multi-Protocol Serial I/O Board inclusive documentation
SYS68K/SIO-2A Part No. 310005	Channel Multi-Protocol Serial I/O Controller Board with 2 optical links inclusive documentation
SYS68K/SIO-1FP Part No. 310001	Front Panel with six 25 pin D-sub Connectors
SYS68K/SIO-2/UM Part No. 800129	User's Manual for the SYS68K/SIO-2 Board



System 68000 VME
SYS68K/ISIO-1/1A

Intelligent Serial I/O Board

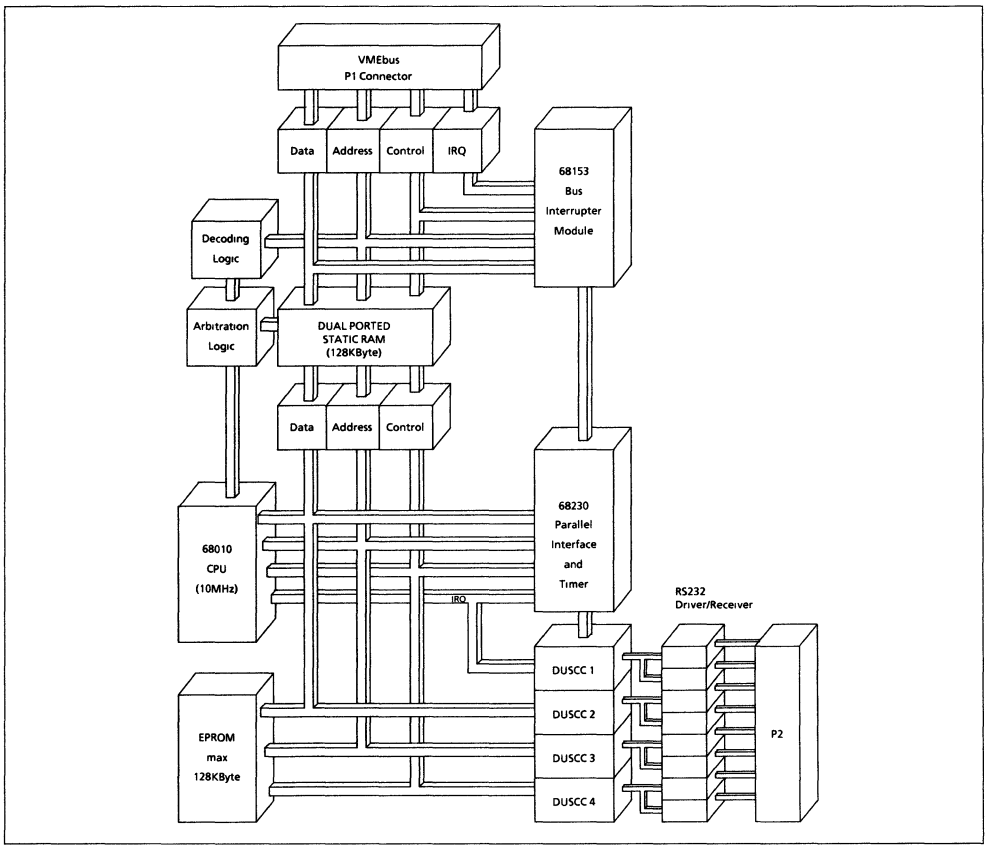
- 8 channel, multi-protocol serial I/O controller board
- On-board RS232 transceiver
- 128/512 Kbyte No Wait State Dual Ported RAM
- 68010 for local handling and control
- 4 fully software programmable interrupt channels
- Powerful handling firmware



1. General Description

The SYS68K/ISIO-1/1A is a high performance intelligent serial I/O board providing local intelligence with a 68010 CPU and 8 serial I/O channels with onboard RS232-compatible driver/receiver circuits.
128 Kbyte (ISIO-1) or 512 Kbyte (ISIO-1A) of Dual Ported RAM are used to store commands and data. Highest throughput is guaranteed by using a 10MHz 68010 CPU running constantly without the insertion of wait states out of the 128 Kbyte EPROM area or out of the DPR (independent of VMEbus accesses).
Four Dual Universal Serial Communication Controllers DUSCC 68562 are used to interface to as many as 8 serial channels.
The RS232 driver and receiver circuitries are installed on the ISIO-1/1A to make adaptation boards unnecessary.
To enable easy system design, all I/O signals are routed to the P2 connector which results in 7 I/O signals per channel being supported.
The ISIO-1/1A contains a VMEbus IEEE 1014 compatible interface to communicate to the host CPUs via its DPR. The access address and the address modifier code is jumper selectable. A Bus Interrupter Module – BIM 68153 – is installed on the board to support fully asynchronous operation with the 4 different software programmable interrupt request channels.
The firmware of the ISIO-1/1A handles all activities to/from the serial I/O channels including code conversion, search and copy functions.

BLOCK DIAGRAM OF THE SYS68K/ISIO-1/1A



Features of the SYS68K/ISIO-1/1A

- 68010 CPU for local control (10MHz)
- Dual Ported 512 Kbyte 0 wait state Static RAM between the VMEbus and the local CPU on ISIO-1A.
- Dual Ported 128 Kbyte 0 wait state Static RAM between the VMEbus and the local CPU on ISIO-1.
- 8 serial I/O channels built with four 68562 DUSCC chips. HDLC and SDLC protocols supported. Independently software programmable baud rate for each channel from 50 to 38400 baud. Data rate in synchronous mode up to 4 Mbit/s.
- RS232 driver and receiver circuits on board.
- All I/O signals available on P2 connector.
- 4 different interrupt request signals to the VMEbus. Each channel contains a software programmable IRQ level (1 to 7) and vector.
- Local parallel interface for controlling and monitoring all board functions.
- Local timer used as watchdog.
- VMEbus IEEE 1014 compatible interface A24 : D16, D8
- Watchdog timer controlling correct functions of onboard hard- and software.
- Status and control LEDs for monitoring of local activities.
- High level handling firmware for communication, selftest and control.

1. The Hardware Functions

The local CPU reacts on the commands and initialisation parameters within the DPR. Constant program run times are guaranteed through the special hardware logic providing Zero Wait State operation from the DPR, independent of the accesses from the VMEbus to the DPR.
The ISIO-1/1A consists of self-test functions as well as of a hardware watchdog timer which controls the activities of the 68010 CPU running with 10MHz.
User supplied programs can be loaded into the DPR and executed from the local CPU to adapt and extend board functionality.
A time scheduler and a prioritisation mechanism are installed in the firmware to adapt the ISIO-1/1A to a wide variety of applications such as terminal controller, print spooler, interacting network controller etc.
The local CPU controls all 8 serial I/O channels via local interrupts and communicates to the host CPU via the DPR or via interrupt requests to the VMEbus generated by a Bus Interrupter Module. The I/O signals to be supported through the DUSCC chips are jumper selectable which allows the individual adaptation to each application on a channel by channel basis.

1.1 The Local 68010 CPU

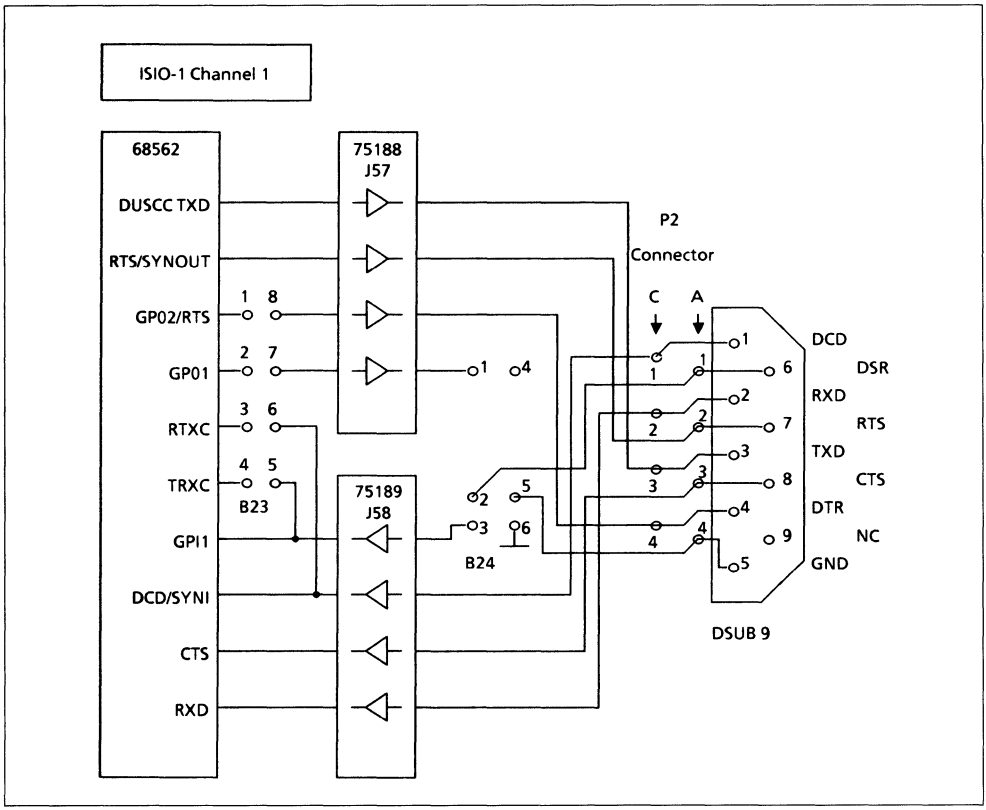
A 10MHz 68010 CPU is installed on the ISIO-1/1A to control the data traffic between the serial I/O channels and the VMEbus host CPU(s).
Two EPROMs with a maximum capacity of 128 Kbyte are installed on the ISIO-1/1A to contain the handling firmware. Constant Zero Wait State operation from the EPROM guarantees maximum CPU throughput and a fixed program run time.
The Dual Ported RAM is also accessible without the insertion of wait states by using a CPU clock synchronized arbitration mechanism. The accesses from the CPU to the DPR are not delayed if a VMEbus access is pending or being executed.
A local timer, included in the PI/T, is used to interrupt the CPU for task scheduling, command interpretation and execution.
The CPU and all I/O devices can be RESET through a SYSTEM reset via the SYSRESET signal of the VMEbus or by accessing a dedicated location within the DPR reserved for this function.

1.2 The Serial I/O Interfaces

The ISIO-1/1A contains 4 Dual Universal Serial Communication Controllers - DUSCC 68562. Each of the DUSCC chips provides the following features:

- Dual full-duplex synchronous/asynchronous receiver and transmitter.
- Multi-protocol operation consisting of:
  BOP: HDLC/ADCCP, SDLC, SDLC Loop,
  X.25 or X.75 link level
  COP: BISYNC, DDCMP, X.21
  ASYNC: 5-8 bits plus optional parity
- Programmable data encoding formats
  NRZ, NRZI, FM0, FM1, Manchester
- 4 character receiver and transmitter FIFO's
- Programmable baud rate for each receiver and transmitter
  50 to 38400 Baud (asynchronous)
  Special data rate ranging from 0 to 4MHz
  Digital phase locked loop
  User programmable counter/timer
- Programmable channel modes
  full/half duplex
  auto echo
  local loopback
- Modem control signals for each channel
  RTS, CTS, DCD
  CTS and DCD programmable auto enables for Receiver (RX) and Transmitter (TX)
  Programmable interrupt on change of CTS or DCD

A set of 7 I/O signals is supported on each channel providing maximum flexibility for the use of the I/O pins as shown in the following figure.

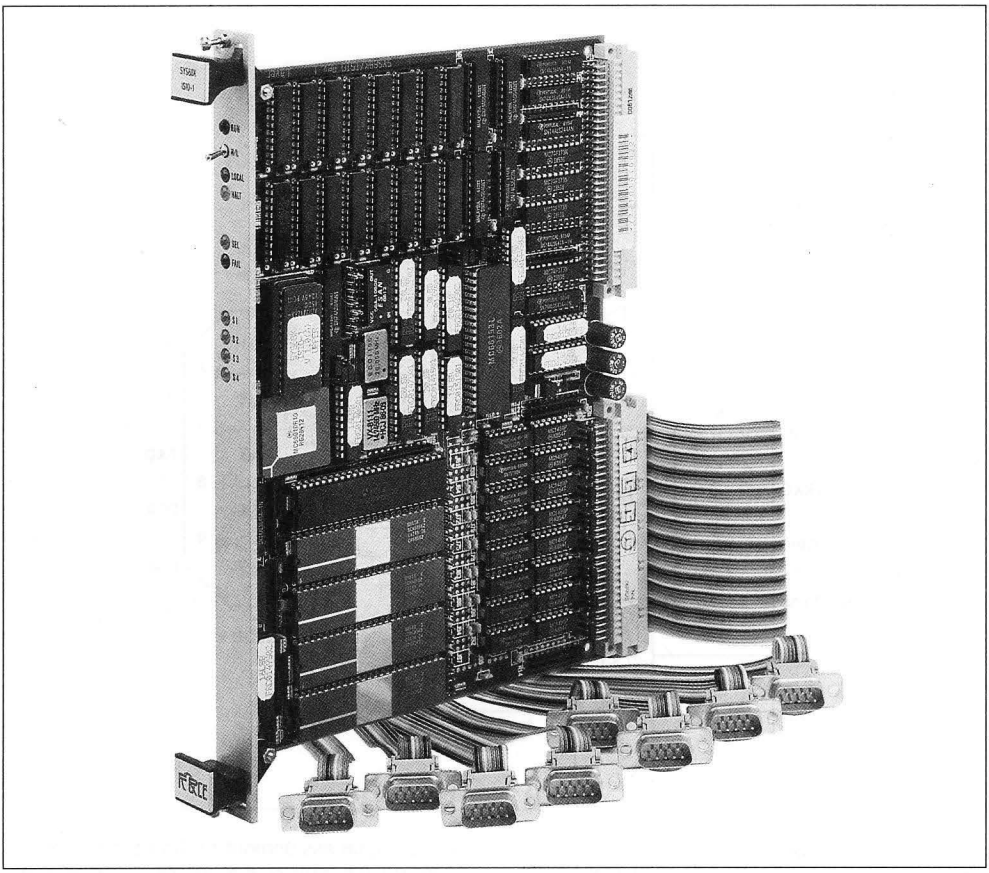


All RS232 compatible driver and receiver circuits are installed on the ISIO-1/1A to allow easy installation and adaptation of the board into VMEbus environments.

The I/O signal assignment to the P2 connector is organised in 8 groups of 8 signals as shown in the following table:

Signal	Input	Output	P2-PIN	9 PIN DSUB Connector	Description
DCD	x		c1	1	Data Carrier Detect
RXD	x		c2	2	Receive Data
TXD		x	c3	3	Transmit Data
DTR		x	c4	4	Data Terminal Ready
GND			a4	5	Signal GND
DSR	x	x	a1	6	Data Set Ready
RTS		x	a2	7	Request to Send
CTS	x		a3	8	Clear to Send
–	–	–	–	9	Not Connected

The 64 I/O pins of the P2 connector can be connected with a flat cable allowing the splitting into 8 flat cables. Each of these cables can be connected to a 9-PIN D-Sub connector as shown in the following figure.



1.3 The PI/T 68230

A 68230 Parallel Interface and Timer chip is installed on the ISIO-1/1A to control and display the status of all on-board activities. The PI/T is also used to issue and monitor the interrupt request lines to the Bus Interrupter Module, which initiates the interrupts to the VMEbus (under control of the host CPU).
One handshake pin is used to interrupt the local CPU if the host CPU accesses a defined location within the DPR. One output signal is used to activate the SYSFAIL signal of the VMEbus if an onboard error has been detected or if the board initializes the DPR after RESET or power up.
The timer, also included in the PI/T, is the time base for the onboard handling firmware and the scheduler for the macro commands.
A watchdog timer, for processor control, is installed on the board to detect software or hardware errors independent from the onboard CPU. For this purpose, one output of the PI/T is used to retrigger the watchdog timer within defined time frames.
If the onboard CPU does not work properly, or if the hardware isn't working correctly, the timer will not be retriggered, and the SYSFAIL signal of the VMEbus will be activated. The host CPU then can initiate a software controlled RESET for the ISIO, or start other maintenance activities.

1.4 The Dual Ported RAM

512 Kbyte of Dual Ported Static RAM with 45ns access time is installed on the ISIO-1A and 128 Kbyte is installed on the ISIO-1. The Dual Ported RAM is used to service all applications requiring fast operations and large data areas.
The local 68010 CPU runs without the insertion of wait states out of the DPR, because a CPU clock synchronized arbitration logic and a full buffered and latched VMEbus interface is installed on the ISIO-1/1A. Between two CPU access cycles, a VMEbus cycle is serviced and completed. On VMEbus Read cycles, the data pattern is latched, and the internal cycle of the DPR is aborted while the VMEbus cycle is decoupled.
A partition of the DPR is reserved for the local CPU for vector storage, the program counter, and temporary buffers. This partition is used from the VMEbus side for programming the BIM and initiating an interrupt, which will be handled from the onboard CPU, or driving a local RESET.
The access address and the address modifier code(s) are jumper selectable within the standard address range (A24:D16,D8). The access times of the DPR depend on the accesses made by the local CPU, as the local 68010 has priority over VMEbus accesses.

1.5 The VMEbus Interface

A full VMEbus IEEE 1014 standard compatible interface is installed on the ISIO-1/1A to allow an access to the DPR and the Bus Interrupter Module.
The 16-bit data width (D16,D8) of the DPR and the decoding of the standard address range (A24) allows easy installation in all VMEbus environments.
During power-up and after a RESET has been executed from the local CPU, the ISIO-1/1A drives the VMEbus signal SYSFAIL active to signal each board in the VMEbus environment that the board is not ready or has detected a malfunction.
A RESET for the local CPU can be initiated by accessing a dedicated address within the DPR. All local devices as well as the CPU will be reset through this access.
An interrupt to the local CPU can be forced by accessing another location within the DPR, signalling the on-board processor that a command has been given, or that an exception has to be taken.
The Dual Ported RAM can be accessed at least every 560ns because this is the worst case access time and also the longest cycle time. The data transfer rate to/from the ISIO-1/1A is 2 to 4 Mbyte/s including the VMEbus protocol.

best case	330 ns
average	430 ns
worst case	560 ns

1.6 The Bus Interrupter Module

To allow fully asynchronous operation, the ISIO-1/1A contains a Bus Interrupter Module – BIM 68153 – providing 4 individually programmable interrupt channels. Each channel is able to force an interrupt request to the VMEbus. For each channel, the IRQ level (1 to 7) as well as the interrupt vector is fully software programmable.
The local CPU forces the requests to the BIM and the host CPU can program the interrupt vector and the level at its direction. This allows dynamic change of the interrupt level and vector in multiprocessor environments.

Memory Layout of the Dual Ported RAM

Offset to Base Address	Description
$000000 – $0007FF	BIM providing 4 programmable interrupt levels and vectors on VME.
$000800 – $000FFF	Status register, read only.
$001000 – $0017FF	Local interrupt, reading this address generates a local interrupt.
$001800 – $001FFF	Local reset, reading this address generates a local reset.
$002000 – $007FFF	This part of the dual ported RAM is used by the local firmware and must not be modified from the VMEbus.
$008000 – $0080FF	16 command channels to program the 8 input and 8 output channels.
$008100 – $01FFFF	16 data arrays for the I/O channels.

2.0 The Handling Firmware

The SYS68K/ISIO-1/1A intelligent serial I/O board operates under the control of the local handling firmware. This EPROM resident firmware package executes the commands which are placed in the Dual Ported RAM and returns control and error messages. All commands are executed under the supervision of a local real time kernel which coordinates the 8 input and 8 output tasks.

Each of the 16 command blocks are used to pass commands and parameters to the corresponding channel. When the command is executed an interrupt can be generated. The return value containing end codes and parameters is placed in the command block.

Command Set of the ISIO-1/1A

2.1 Initialisation Commands:

- Global RAM Configuration
- Terminal Configuration
- I/O Chip Configuration
- Setup of Address Offset
- Load Translation Table
- Setup of Handshake Modes
- Asynchronous Initialisation
- Software Reset with Selftest
- Return RAM Configuration

2.2 Input Commands:

- Get one byte from input channel with/without autoecho
- Get all available bytes from input channel with/without autoecho
- Get block with fixed length from input channel with/without autoecho
- Get string with/without autoecho
- Get counted string with/without autoecho
- Get edited line
- Get input channel status

2.3 Output Commands:

- Output byte or word
- Output block with fixed length
- Output string
- Output counted string
- Return output channel status

2.4 Copy Commands:

- Copy byte from input channel to output channel(s)
- Copy block with fixed length from input channel to output channel(s)
- Copy string from input channel to output channel(s)
- Copy counted string from input channel to output(s)

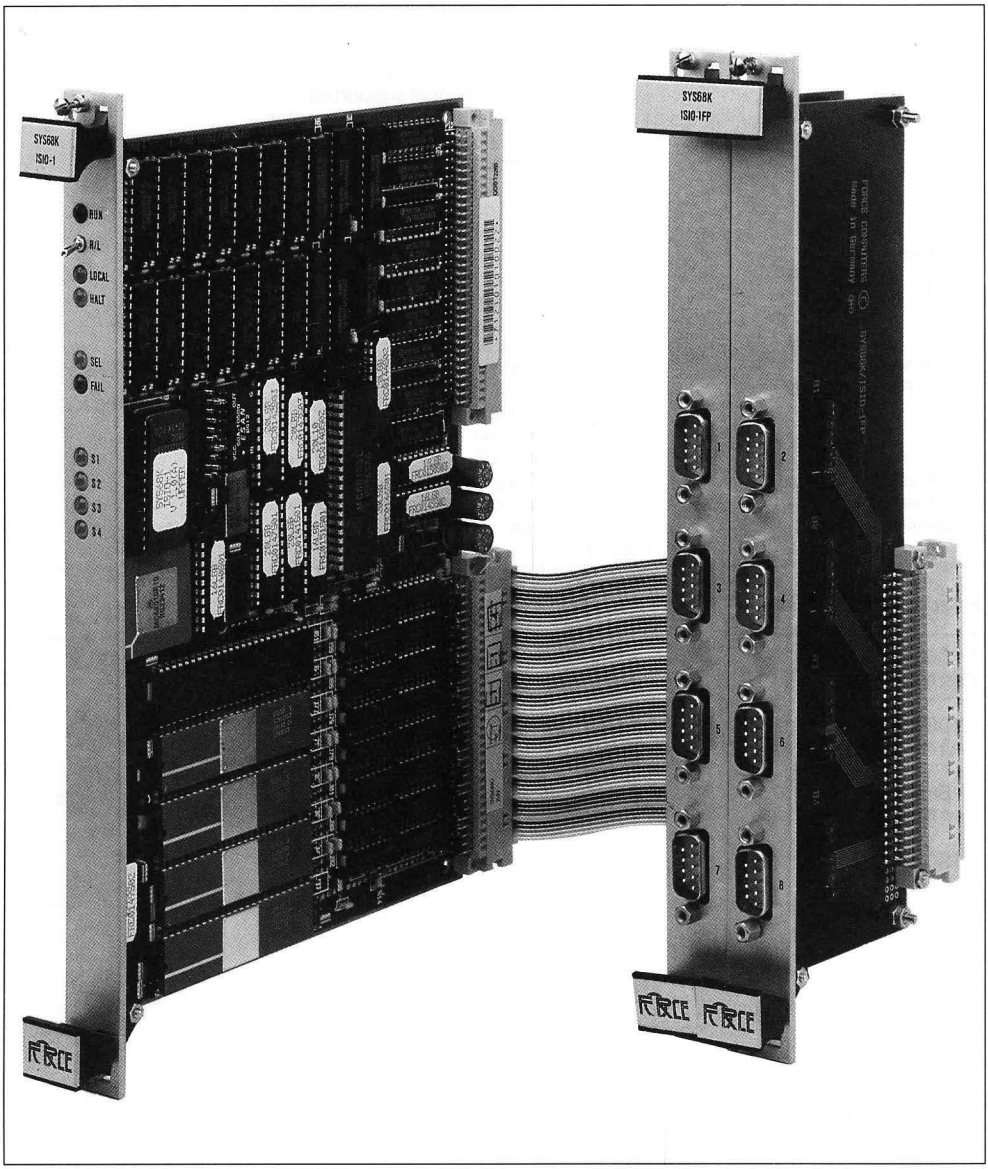
2.5 Special Commands:

- Execute user program in the DPR

3.0 The Optional Front Panel

A front panel consisting of eight 9-pin D-sub connectors is optionally available to allow direct connection to the 8 serial I/O channels of the ISIO-1/1A board.
The pin-out for each of the 8 D-sub connectors is adjustable on the ISIO-1/1A board.

The following figure shows the SYS68K/ISIO-1FP and the interconnection to the ISIO-1/1A board in detail.
Each of the 7 I/O signals is connected to a jumperfield on the ISIO-1FP board to allow adaptition of the I/O signals to the various applications.

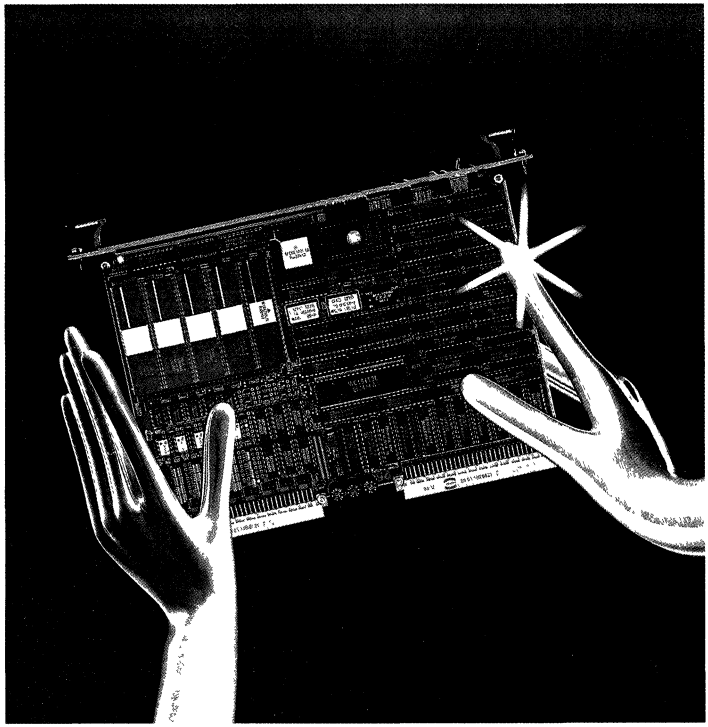


Specification of the SYS68K/ISIO-1/1A

Local CPU	68010 with 10MHz clock frequency
EPROM	128 Kbyte maximum capacity 0 Wait State operation
Dual Ported RAM	128/512 Kbyte capacity using static RAMs 0 Wait State operation from local CPU 330 ns best case VMEbus access time 430 ns average VMEbus access time 560 ns worst case VMEbus access time
Serial I/O Interfaces	8 channels (RS232 compatible) 7 I/O signals per channel supported All I/O signals available on P2 connector
Serial I/O Controller	68562 DUSCC providing SW-programmable baud rate (50 to 38400 Baud) HDLC and SDLC protocols DC data rate of up to 4 MBit/second Automatic hardware handshake programmable
VMEbus Interface	Full IEEE 1014 standard compatible A24:D16,D8 mode 4 IRQs with SW programmable level (1 to 7) and vector Access address jumper selectable SYSFAIL* supported
Handling Firmware	in EPROM with macro commands for all I/O channels installed
Power Requirements	+ 5V : 5.4 A (max) +12V : 0.6 A (max) −12V : 0.6 A (max) (P2 Backplane or power connection on P2 recommended)
Operating Temperature	0 to 50 Degrees C
Storage Temperature	−50 to +85 Degrees C (non-operating)
Relative Humidity	0 to 90% (non-condensing)
Dimensions	233 x 160 mm 9.2" x 6.3"

Ordering Information

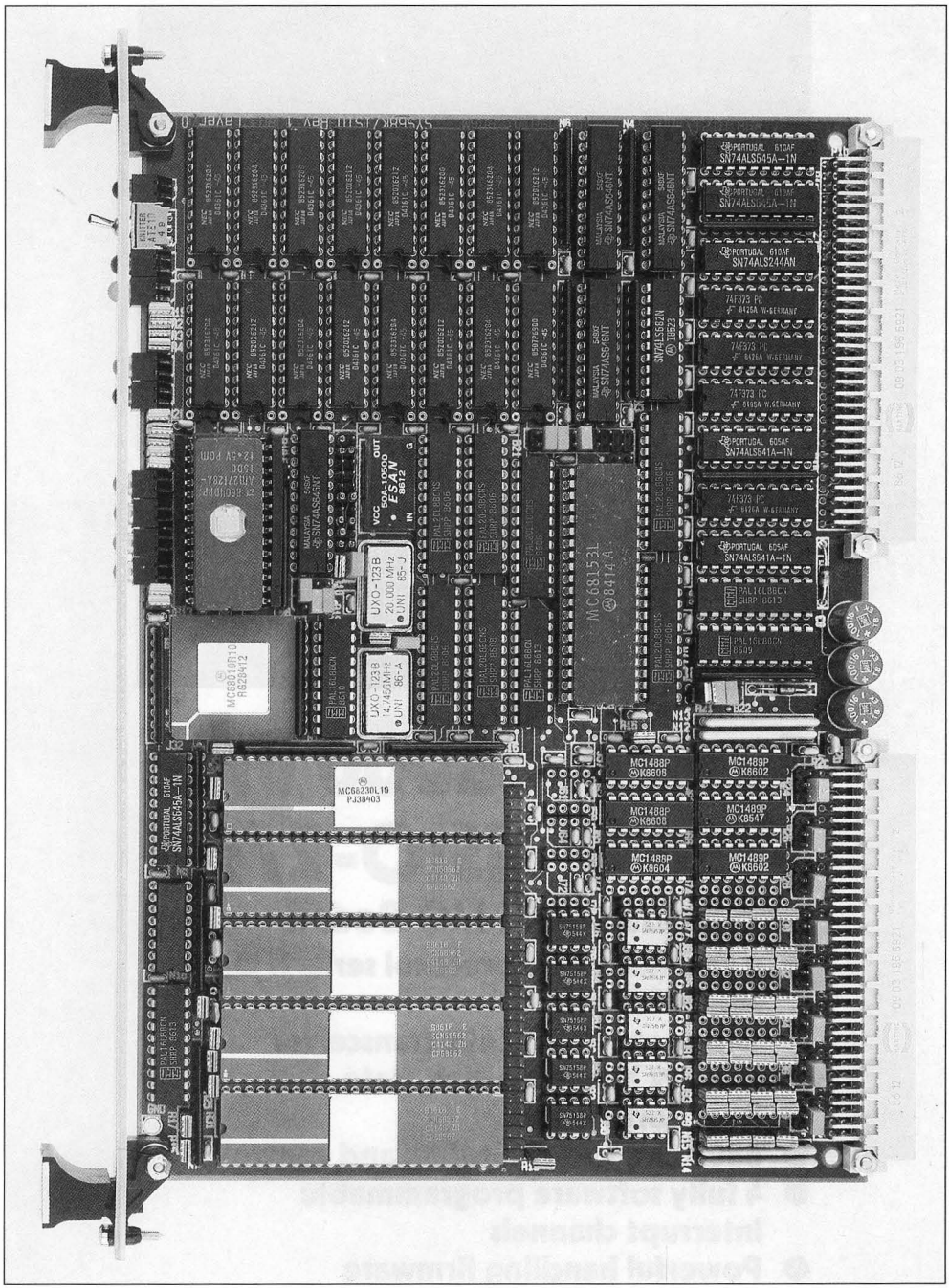
SYS68K/ISIO-1 Part No. 310030	8 Channel Intelligent Serial I/O Controller board with 128 Kbyte of DPR, including firmware and documentation.
SYS68K/ISIO-1A Part No. 310035	8 Channel Intelligent Serial I/O Controller board with 512 Kbyte of DPR, including firmware and documentation.
SYS68K/ISIO-1FP Part No. 310034	Front Panel for the ISIO-1/1A board providing eight 9-pin D-sub connectors.
SYS68K/ISIO-1/UM Part No. 800109	User's Manual for the ISIO-1/1A.



System 68000 VME
SYS68K/ISIO-2/2A

Intelligent Serial I/O Board

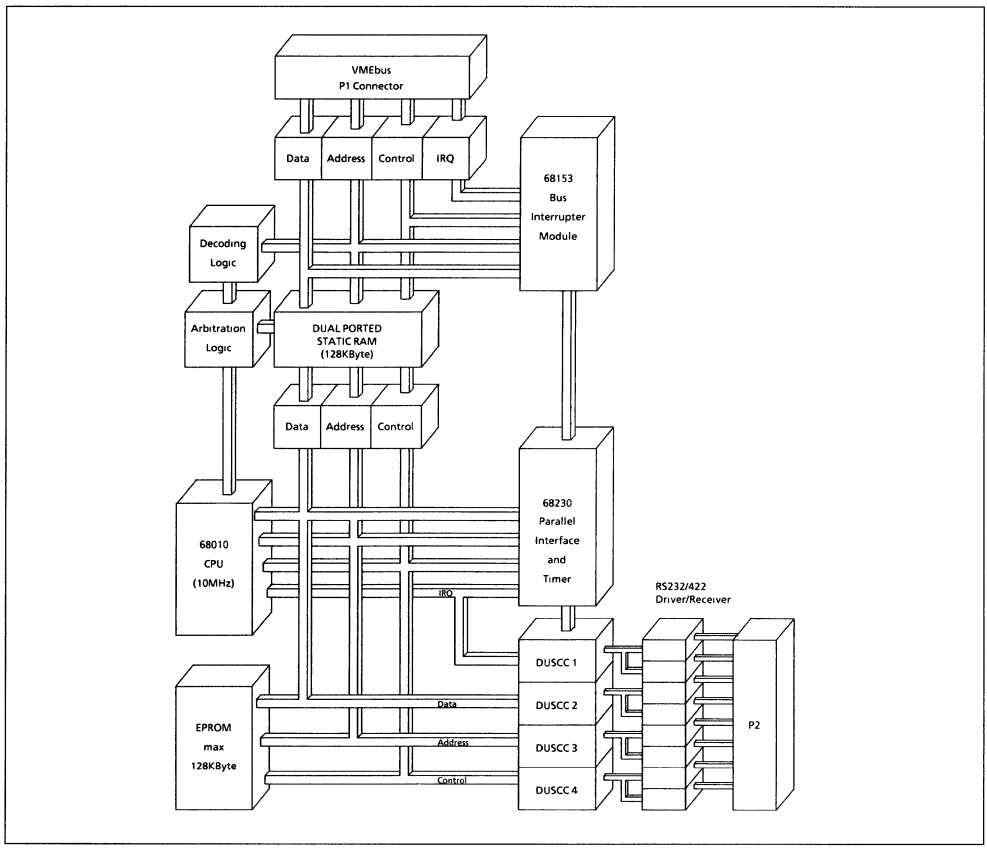
- 8 channel, multi-protocol serial I/O controller board
- On-board RS232/422 transceiver
- 128/512 Kbyte No Wait State Dual Ported RAM
- 68010 for local handling and control
- 4 fully software programmable interrupt channels
- Powerful handling firmware



1. General Description

The SYS68K/ISIO-2/2A is a high performance intelligent serial I/O board providing local intelligence with a 68010 CPU and 8 serial I/O channels with onboard RS232-compatible driver/receiver circuits.
512 Kbyte (ISIO-2A) or 128 Kbyte (ISIO-2) of Dual Ported RAM used are to store commands and data. Highest throughput is guaranteed by using a 10MHz 68010 CPU running constantly without the insertion of wait states out of the 128 Kbyte EPROM area or out of the DPR (independent of VMEbus accesses).
Four Dual Universal Serial Communication Controllers DUSCC 68562 are used to interface to as many as 8 serial channels.
The RS232/422 driver and receiver circuitries are installed on the ISIO-2/2A to make adaptation boards unnecessary.
To enable easy system design, all I/O signals are routed to the P2 connector which results in 8 I/O signals per channel being supported.
The ISIO-2/2A contains a VMEbus IEEE 1014 compatible interface to communicate to the host CPUs via its DPR. The access address and the address modifier code is jumper selectable. A Bus Interrupter Module – BIM 68153 – is installed on the board to support fully asynchronous operation with the 4 different software programmable interrupt request channels.
The firmware of the ISIO-2/2A handles all activities to/from the serial I/O channels including code conversion, search and copy functions. For special applications, the source code of the firmware is optionally available.

BLOCK DIAGRAM OF THE SYS68K/ISIO-2/2A



Features of the SYS68K/ISIO-2/2A

- 68010 CPU for local control (10MHz)
- Dual Ported 512 Kbyte 0 wait state Static RAM between the VMEbus and the local CPU on ISIO-2A.
- Dual Ported 128 Kbyte 0 wait state Static RAM between the VMEbus and the local CPU on ISIO-2.
- 8 serial I/O channels built with four 68562 DUSCC chips. HDLC and SDLC protocols supported. Independently software programmable baud rate for each channel from 50 to 38400 baud. Data rate in synchronous mode up to 4Mbit/s.
- RS232/422 driver and receiver circuits on board.
- All I/O signals available on P2 connector.
- 4 different interrupt request signals to the VMEbus. Each channel contains a software programmable IRQ level (1 to 7) and vector.
- Local parallel interface for controlling and monitoring all board functions.
- Local timer used as watchdog.
- VMEbus IEEE 1014 compatible interface A24:D16, D8
- Watchdog timer controlling correct functions of onboard hard- and software.
- Status and control LEDs for monitoring of local activities.
- High level handling firmware for communication, selftest and control.

1. The Hardware Functions

The local CPU reacts on the commands and initialisation parameters within the DPR. Constant program run times are guaranteed through the special hardware logic providing Zero Wait State operation from the DPR, independent to the accesses from the VMEbus to the DPR.
The ISIO-2/2A consists of self-test functions as well as of a hardware watchdog timer which controls the activities of the 68010 CPU running with 10MHz.
User supplied programs can be loaded into the DPR and executed from the local CPU to adapt and extend board functionality.
A time scheduler and a prioritisation mechanism are installed in the firmware to adapt the ISIO-2/2A to a wide variety of applications such as terminal controller, print spooler, interacting network controller etc.
The local CPU controls all 8 serial I/O channels via local interrupts and communicates to the host CPU via the DPR or via interrupt requests to the VMEbus generated by a Bus Interrupter Module. The I/O signals to be supported through the DUSCC chips are jumper selectable which allows the individual adaptation to each application on a channel by channel basis.

1.1 The Local 68010 CPU

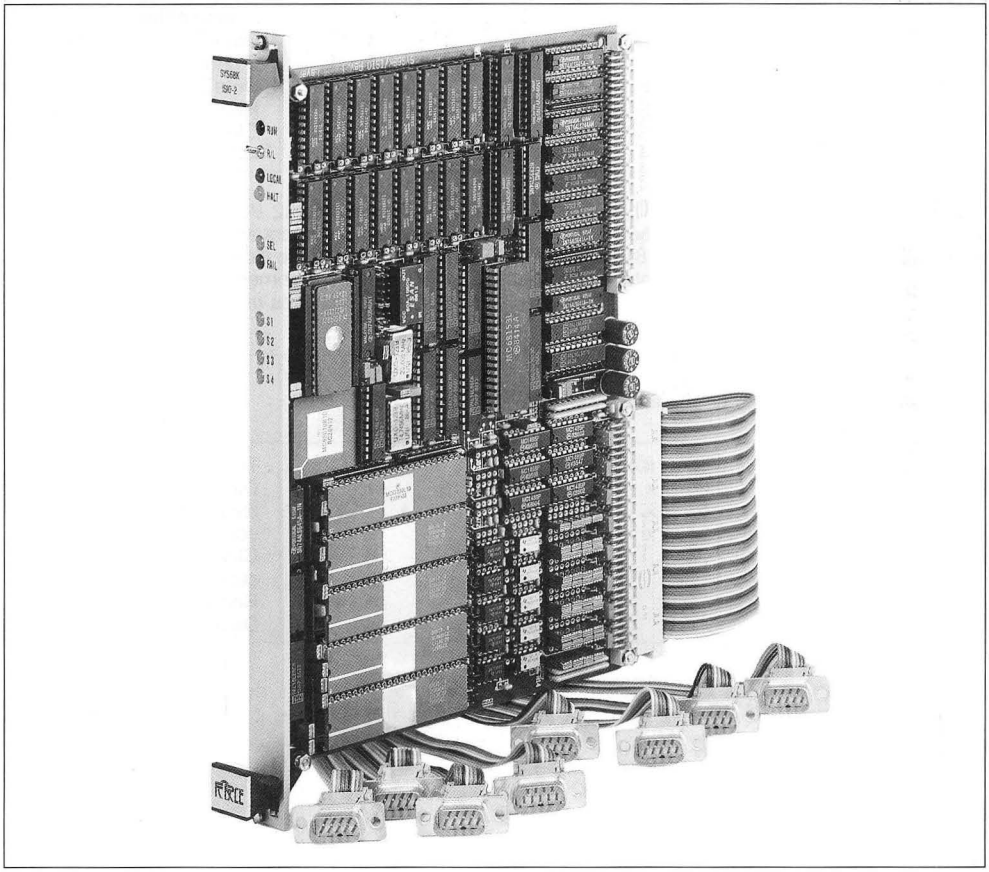
A 10MHz 68010 CPU is installed on the ISIO-2/2A to control the data traffic between the serial I/O channels and the VMEbus host CPU(s).
Two EPROMs with a maximum capacity of 128 Kbyte are installed on the ISIO-2/2A to contain the handling firmware. Constant Zero Wait State operation from the EPROM guarantees maximum CPU throughput and a fixed program run time.
The Dual Ported RAM is also accessible without the insertion of wait states by using a CPU clock synchronized arbitration mechanism. The accesses from the CPU to the DPR are not delayed if a VMEbus access is pending or being executed.
A local timer, included in the PI/T, is used to interrupt the CPU for task scheduling, command interpretation and execution.
The CPU and all I/O devices can be RESET through a SYSTEM reset via the SYSRESET signal of the VMEbus or by accessing a dedicated location within the DPR reserved for this function.

1.2 The Serial I/O Interfaces

The ISIO-2/2A contains 4 Dual Universal Serial Communication Controllers - DUSCC 68562. Each of the DUSCC chips provides the following features:

- Dual full-duplex synchronous/asynchronous receiver and transmitter.
- Multi-protocol operation consisting of:
  BOP: HDLC/ADCCP, SDLC, SDLC Loop, X.25 or X.75 link level
  COP: BISYNC, DDCMP, X.21
  ASYNC: 5-8 bits plus optional parity
- Programmable data encoding formats
  NRZ, NRZI, FM0, FM1, Manchester
- 4 character receiver and transmitter FIFO's
- Programmable baud rate for each receiver and transmitter
  50 to 38400 Baud (asynchronous)
  Special data rate ranging from 0 to 4MHz
  Digital phase locked loop
  User programmable counter/timer
- Programmable channel modes
  full/half duplex
  auto echo
  local loopback
- Modem control signals for each channel
  RTS, CTS, DCD
  CTS and DCD programmable auto enables for Receiver (RX) and Transmitter (TX)
  Programmable interrupt on change of CTS or DCD

A set of 8 I/O signals is supported on each channel providing maximum flexibility for the use of the I/O pins.
The ISIO-2/2A board offers two different interface types for each channel. The board is equipped by default with RS232 driver and receiver circuits supporting 7 I/O signals as listed in paragraph 1.2.1.
Each of the 8 channels can be reconfigured to meet the RS422 standard. Both of the driver and receiver circuits reside on the sockets and can easily be removed or exchanged. By having one basic version, the application needs with user's direction are easier to reconfigurate. Maximum flexibility is guaranteed because the number of RS232 and RS422 interfaces are user defined without any limitation.
Resistors and capacitors can be installed in the RS422 mode to adapt the various cable length. A detailed description of the RS422 interface is shown in paragraph 1.2.2.



1.2.1 The RS232 Interface

All RS232 compatible driver and receiver circuits are installed on the ISIO-2/2A to allow easy installation and adaptation of the board into VMEbus environments.

The I/O signal assignment to the P2 connector is organised in 8 groups of 8 signals as shown in the following table:

Signal	Input	Output	P2-PIN	9 PIN DSUB Connector	Description
DCD	x		c1	1	Data Carrier Detect
RXD	x		c2	2	Receive Data
TXD		x	c3	3	Transmit Data
DTR		x	c4	4	Data Terminal Ready
GND			a4	5	Signal GND
DSR	x	x	a1	6	Data Set Ready
RTS		x	a2	7	Request to Send
CTS	x		a3	8	Clear to Send
–	–	–	–	9	Not Connected

1.2.2 The RS422 Interface

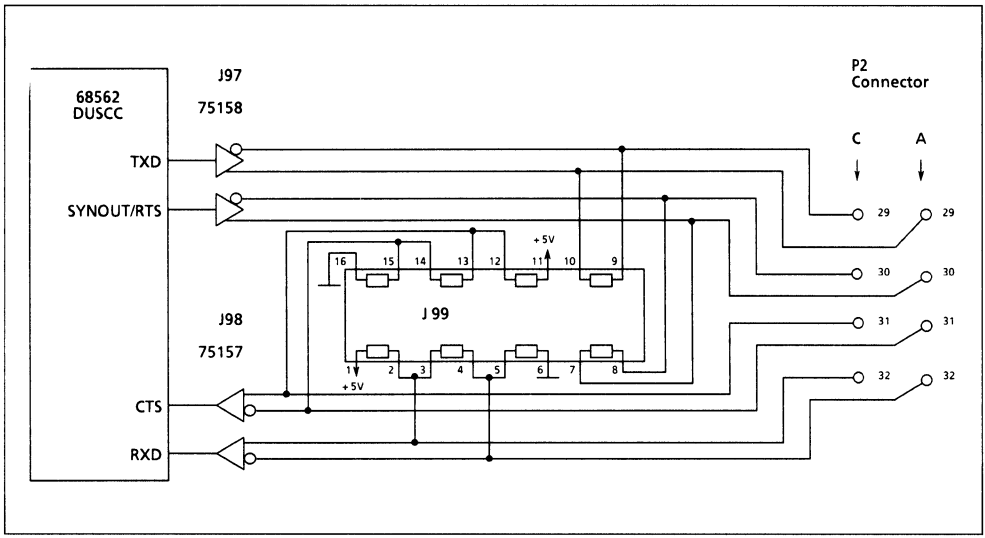
By default the RS232 driver and receiver circuits are installed on the board. Each of the 8 I/O channels can be reconfigured by using other interface chips to the RS422 standard.

Each of the 4 RS422 I/O signals contain socket places where resistors and capacitors can be installed to adapt to the various cable lengths.
The I/O signal assignment to the P2 connector is organized in 8 groups of 4 signals as listed in the following table:

Signal	Input	Output	P2-PIN	9 PIN DSUB Connector	Description
TXD-A		x	a1	6	Transmit
TXD-B		x	c1	1	Data
RTS-A		x	a2	7	Request to
RTS-B		x	c2	2	send
CTS-A	x		a3	8	Clear to
CTS-B	x		c3	3	send
RXD-A	x		a4	5	Receive
RXD-B	x		c4	4	Data

1.2.3 The I/O Signal Assignment

The 64 I/O pins of the P2 connector can be connected with a flat cable allowing the splitting into 8 flat cables. Each of these cables can be connected to a 9-PIN D-Sub connector as shown in the following figure.



1.3 The PI/T 68230

A 68230 Parallel Interface and Timer chip is installed on the ISIO-2/2A to control and display the status of all on-board activities. The PI/T is also used to issue and monitor the interrupt request lines to the Bus Interrupter Module, which initiates the interrupts to the VMEbus (under control of the host CPU).

One handshake pin is used to interrupt the local CPU if the host CPU accesses a defined location within the DPR. One output signal is used to activate the SYSFAIL signal of the VMEbus if an onboard error has been detected or if the board initializes the DPR after RESET or power up.

The timer, also included in the PI/T, is the time base for the onboard handling firmware and the scheduler for the macro commands.

A watchdog timer, for processor control, is installed on the board to detect software or hardware errors independent from the onboard CPU. For this purpose, one output of the PI/T is used to retrigger the watchdog timer within defined time frames.

If the onboard CPU does not work properly, or if the hardware isn't working correctly, the timer will not be retriggered, and the SYSFAIL signal of the VMEbus will be activated. The host CPU then can initiate a software controlled RESET for the ISIO, or start other maintenance activities.

1.4 The Dual Ported RAM

512 Kbyte of Dual Ported Static RAM with 45ns access time is installed on the ISIO-2A and 128 Kbyte is installed on the ISIO-2. The Dual Ported RAM is used to service all applications requiring fast operations and large data areas.
The local 68010 CPU runs without the insertion of wait states out of the DPR, because a CPU clock synchronized arbitration logic and a full buffered and latched VMEbus interface is installed on the ISIO-2/2A. Between two CPU access cycles, a VMEbus cycle is serviced and completed. On VMEbus Read cycles, the data pattern is latched, and the internal cycle of the DPR is aborted while the VMEbus cycle is decoupled.
A partition of the DPR is reserved for the local CPU for vector storage, the program counter, and temporary buffers. This partition is used from the VMEbus side for programming the BIM and initiating an interrupt, which will be handled from the onboard CPU, or driving a local RESET.
The access address and the address modifier code(s) are jumper selectable within the standard address range (A24:D16,D8). The access times of the DPR depend on the accesses made by the local CPU as the local 68010 has priority over VMEbus accesses.

1.5 The VMEbus Interface

A full VMEbus IEEE 1014 standard compatible interface is installed on the ISIO-2/2A to allow an access to the DPR and the Bus Interrupter Module.
The 16-bit data width (D16,D8) of the DPR and the decoding of the standard address range (A24) allows easy installation in all VMEbus environments.
During power-up and after a RESET has been executed from the local CPU, the ISIO-2/2A drives the VMEbus signal SYSFAIL active to signal each board in the VMEbus environment that the board is not ready or has detected a malfunction.
A RESET for the local CPU can be initiated by accessing a dedicated address within of the DPR. All local devices as well as the CPU will be reset through this access.
An interrupt to the local CPU can be forced by accessing another location within the DPR, signalling the on-board processor that a command has been given, or that an exception has to be taken.
The Dual Ported RAM can be accessed at least every 560ns because this is the worst case access time and also the longest cycle time. The data transfer rate to/from the ISIO-2/2A is 2 to 4 Mbyte/s including the VMEbus protocol.

best case	330 ns
average	430 ns
worst case	560 ns

1.6 The Bus Interrupter Module

To allow fully asynchronous operation, the ISIO-2/2A contains a Bus Interrupter Module - BIM 68153 - providing 4 individually programmable interrupt channels. Each channel is able to force an interrupt request to the VMEbus. For each channel, the IRQ level (1 to 7) as well as the interrupt vector is fully software programmable.
The local CPU forces the requests to the BIM and the host CPU can program the interrupt vector and the level at its direction. This allows dynamic change of the interrupt level and vector in multiprocessor environments.

Memory Layout of the Dual Ported RAM

Offset to Base Address	Description
$000000 – $0007FF	BIM providing 4 programmable interrupt levels and vectors on VME.
$000800 – $000FFF	Status register, read only.
$001000 – $0017FF	Local interrupt, reading this address generates a local interrupt.
$001800 – $001FFF	Local reset, reading this address generates a local reset.
$002000 – $007FFF	This part of the dual ported RAM is used by the local firmware and must not be modified from the VMEbus.
$008000 – $0080FF	16 command channels to program the 8 input and 8 output channels.
$008100 – $01FFFF	16 data arrays for the I/O channels.

2.0 The Handling Firmware

The SYS68K/ISIO-2/2A intelligent serial I/O board operates under the control of the local handling firmware. This EPROM resident firmware package executes the commands which are placed in the Dual Ported RAM and returns control and error messages. All commands are executed under the supervision of a local real time kernel which coordinates the 8 input and 8 output tasks.

Each of the 16 command blocks are used to pass commands and parameters to the corresponding channel. When the command is executed an interrupt can be generated. The return value containing end codes and parameters is placed in the command block.

Command Set of the ISIO-2/2A

2.1 Initialisation Commands:

- Global RAM Configuration
- Terminal Configuration
- I/O Chip Configuration
- Setup of Address Offset
- Load Translation Table
- Setup of Handshake Modes
- Asynchronous Initialisation
- Software Reset with Selftest
- Return RAM Configuration

2.2 Input Commands:

- Get one byte from input channel with/without autoecho
- Get all available bytes from input channel with/without autoecho
- Get block with fixed length from input channel with/without autoecho
- Get string with/without autoecho
- Get counted string with/without autoecho
- Get edited line
- Get input channel status

2.3 Output Commands:

- Output byte or word
- Output block with fixed length
- Output string
- Output counted string
- Return output channel status

2.4 Copy Commands:

- Copy byte from input channel to output channel(s)
- Copy block with fixed length from input channel to output channel(s)
- Copy string from input channel to output channel(s)
- Copy counted string from input channel to output(s)

2.5 Special Commands:

- Execute user program in the DPR

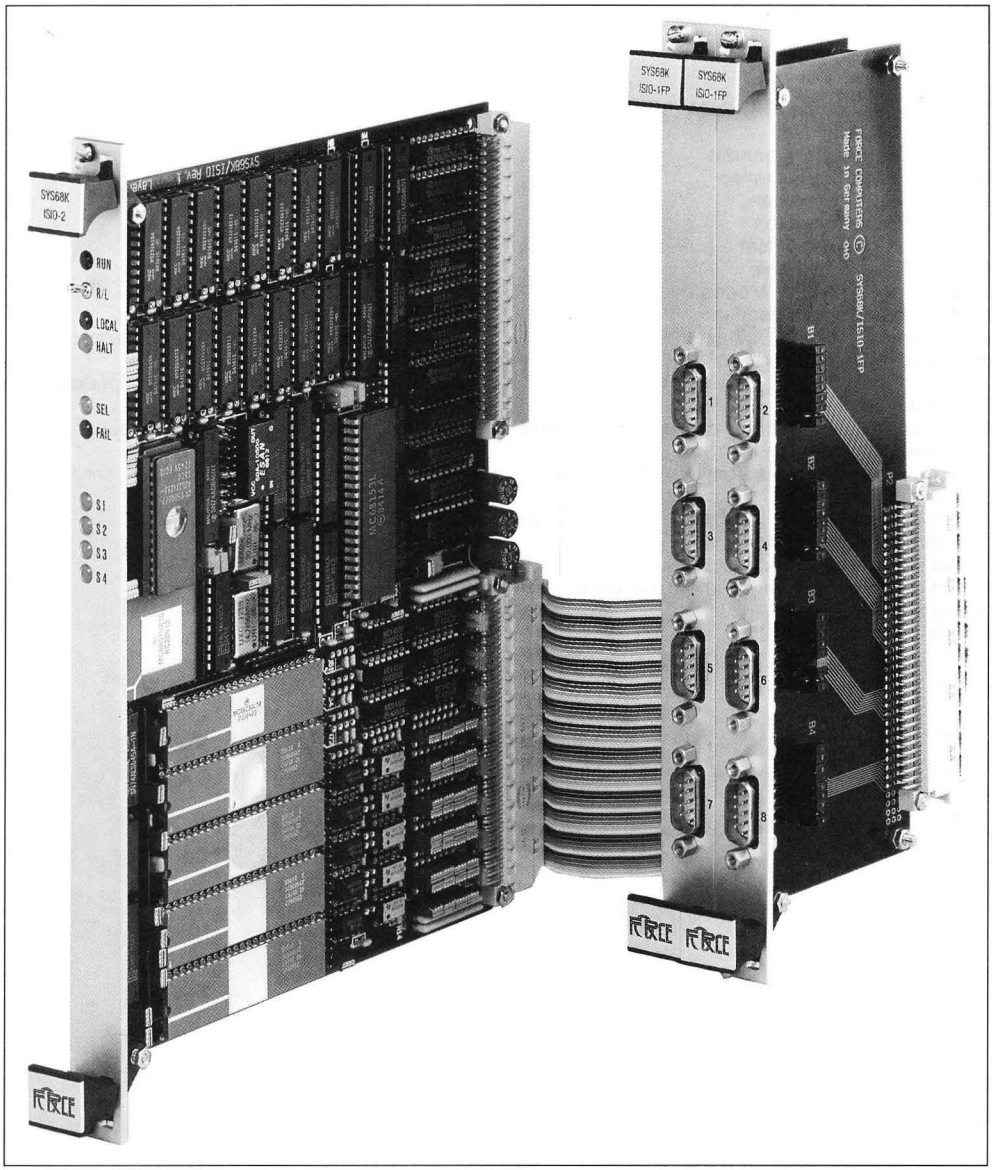
3.0 The Optional Front Panel

A front panel consisting of eight 9-pin D-sub connectors is optionally available to allow direct connection to the 8 serial I/O channels of the ISIO-2/2A board.

The pin-out for each of the 8 D-sub connectors is adjustable on the ISIO-2/2A board.

The following figure shows the SYS68K/ISIO-1FP and the interconnection to the ISIO-2/2A board in detail.

Each of the 7 I/O signals is connected to a jumperfield on the ISIO-1FP board to allow adaptition of the I/O signals to the various applications.



Specification of the SYS68K/ISIO-2/2A

Local CPU	68010 with 10MHz clock frequency
EPROM	128 Kbyte maximum capacity 0 Wait State operation
Dual Ported RAM	128/512 Kbyte capacity using static RAMs 0 Wait State operation from local CPU 330 ns best case VMEbus access time 430 ns average VMEbus access time 560 ns worst case VMEbus access time
Serial I/O Interfaces	8 channels 7 I/O signals per channel (RS232 compatible) or 8 I/O signals per channel (RS422 compatible) All I/O signals available on P2 connector
Serial I/O Controller	68562 DUSCC providing SW-programmable baud rate (50 to 38400 Baud) HDLC and SDLC protocols DC data rate of up to 4 MBit/second Automatic hardware handshake programmable
VMEbus Interface	Full IEEE 1014 standard compatible A24:D16,D8 mode 4 IRQs with SW programmable level (1 to 7) and vector Access address jumper selectable SYSFAIL* supported
Handling Firmware	in EPROM with macro commands for all I/O channels installed
Power Requirements	+ 5V : 5.4 A (max) +12V : 0.6 A (max) −12V : 0.6 A (max) (P2 Backplane or power connection on P2 recommended)
Operating Temperature	0 to 50 Degrees C
Storage Temperature	−50 to +85 Degrees C (non-operating)
Relative Humidity	0 to 90% (non-condensing)
Dimensions	233 x 160 mm 9.2" x 6.3"

Ordering Information

SYS68K/ISIO-2 Part No. 310031	8 Channel Intelligent Serial I/O Controller board with 128 Kbyte DPR, including firmware and documentation.
SYS68K/ISIO-2A Part No. 310036	8 Channel Intelligent Serial I/O Controller board with 512 Kbyte of DPR including firmware and documentation.
SYS68K/ISIO-1FP Part No. 310034	Front Panel for the ISIO-2/2A board providing eight 9-pin D-sub connectors.
SYS68K/ISIO-2/UM Part No. 800110	User's Manual for the ISIO-2/2A.

Analog I/O Boards

FORCE Computers Analog I/O Boards

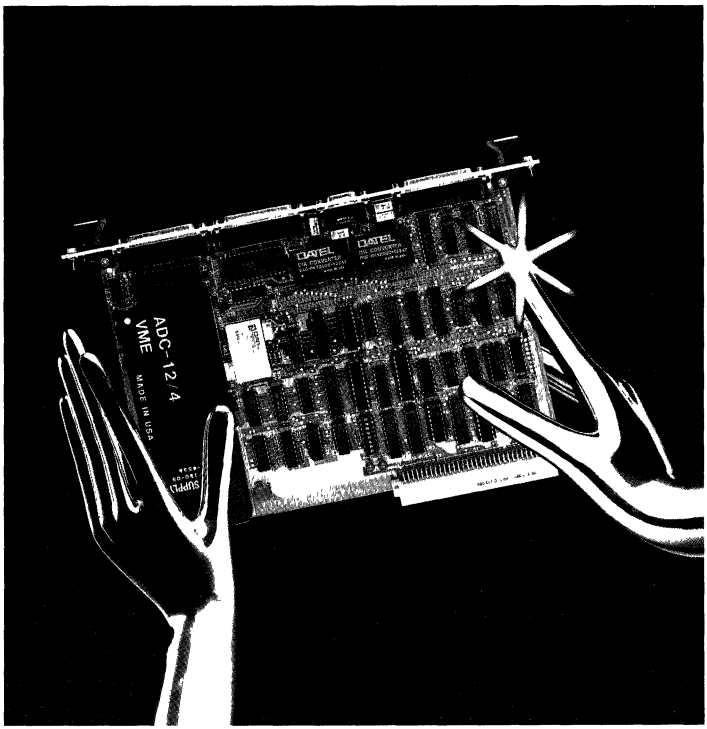
The family of VMEbus based products offered by FORCE Computers includes a family of controller cards which cover analog interfacing application areas. The analog interfacing cards cover virtually all common analog input and output application areas.

General Feature Overview

The family of analog input boards offered by FORCE Computers is as comprehensive as any in today's marketplace. The SYS68K/AD-10/11 boards are analog to digital converter boards offering up to 16 bit resolution. The boards feature either 32 single ended of 16 differential analog input channels. Additionally, the AD-11 offers two additional analog output channels. The AD-10/11 family of boards may be expanded through the use of the auxilliary boards which provide additional functionality to the input channels of the board. Extra features which may be added include sample and hold circuits, isolated input channels and high level expansion. The SYS68K/AD-10/11 family provides solutions to all analog input applications.
For your analog output needs, the SYS68K/DA-1/2 boards offer high resolution and a high level of stability over a wide temperature range. The DA-1 offers 8 digital to analog conversion channels and the DA-2 offers 6 channels. Additionally, curent loop output options are available (4 to 20ma) to complete the functionality of the family. The DA-1/2 are the analog output options.

Analog Controllers

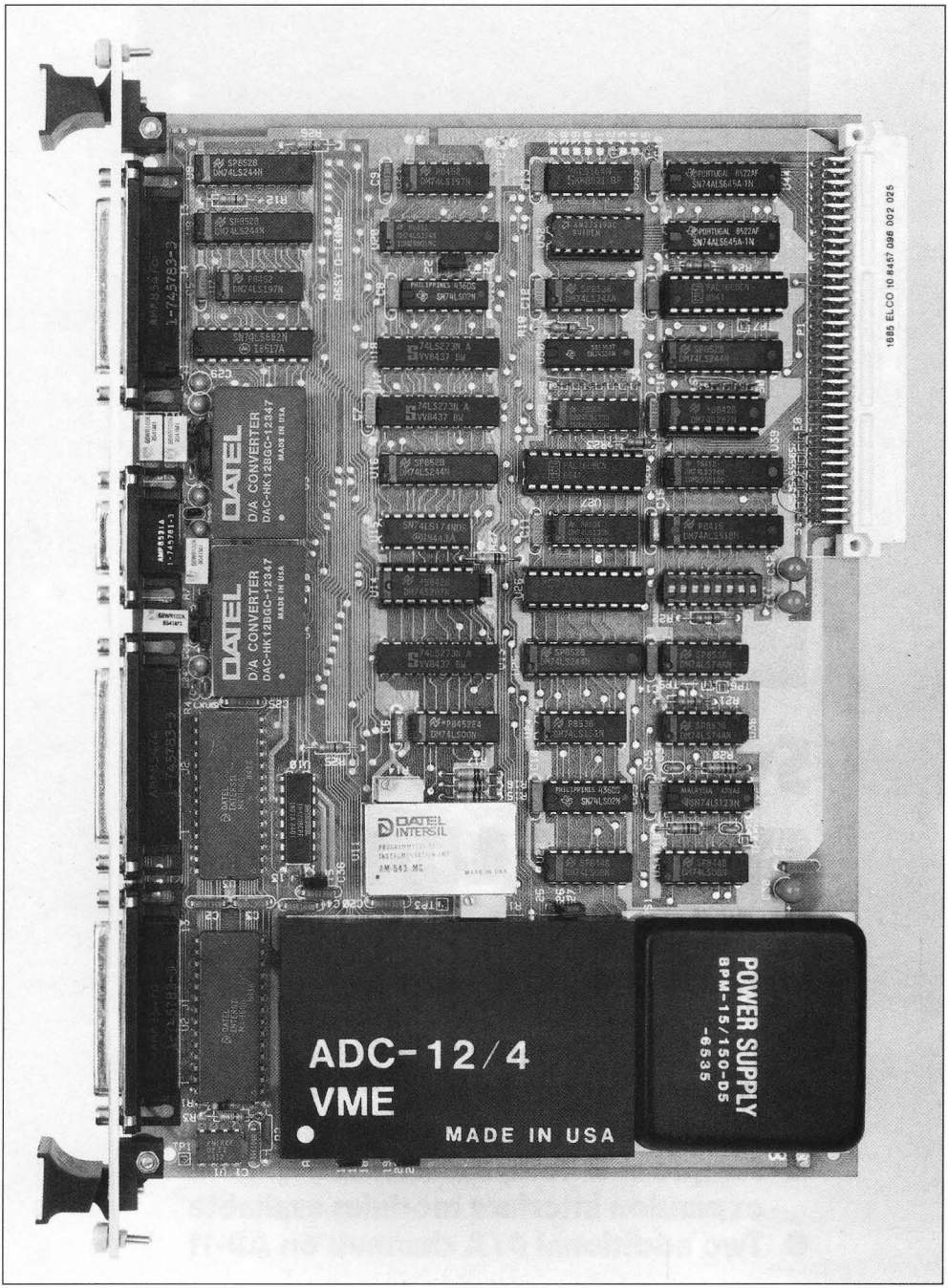
FAMILY	DA-1	DA-2	AD-10	AD-11
Analog O/P Channels	8	6	–	2
Analog I/P Channels	–	–	32/16	32/16
Resolution min.	12 bit	16 bit	12 bit	12 bit
Resolution max.	12 bit	16 bit	16 bit	16 bit
Conversion Time min.	–	–	4 μs	4 μs
Conversion Time max.	6 μs	15 μs	400 ms	400 ms
VMEbus Interface	A16: D16, D8	A16: D16, D8	A16: D16, D8	A16: D16, D8
Detailed Description on Page:	421	421	411	411



System 68000 VME SYS68K/AD-10/11

High Speed Analog to Digital Converter Board Family

- 32/16 A/D channels
- 12/14/16 bit resolution
- Conversion times down to 4 μs
- Sample and hold, isolated and channel expansion interface modules available
- Two additional D/A channels on AD-11

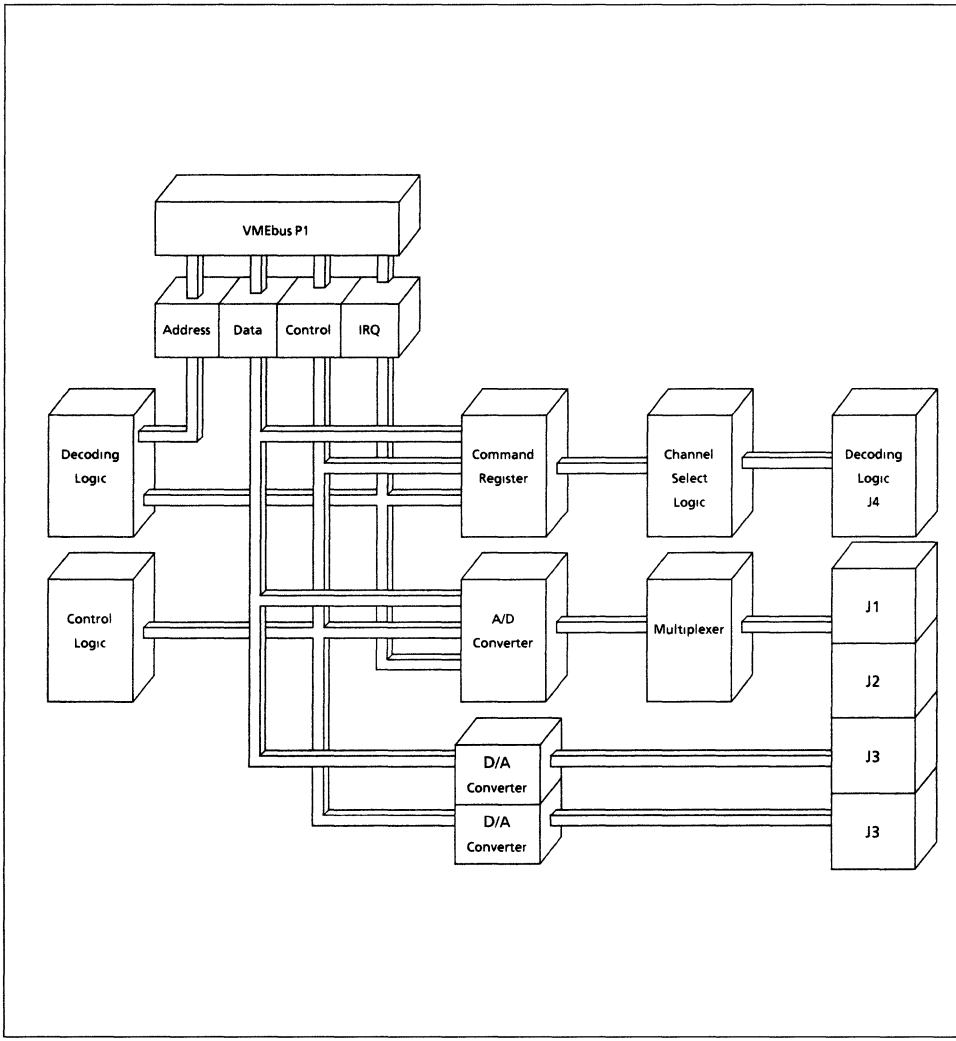

DATEL
D/A CONVERTER
DAC-HK12BGC-12347
MADE IN USA
DATEL
INTERSIL
ADC-12/4
VME
MADE IN USA
POWER SUPPLY
BPM-15/150-D5
-6535

General Description

The SYS68K/AD-10/11 series of products are Analog to Digital converter boards supporting highest conversion rates (up to 16 bit resolution), as well cost effective solutions to the application needs.
The SYS68K/AD-10 board features 32 single ended or 16 differential analog input channels with 12 to 16 bit resolution. To provide analog output control functions, the SYS68K/AD-11 board features two additional output channels.

The SYS68K/AD-10/11 auxiliary boards provide sample and hold (SYS68K/AD-12), isolated input channels (SYS68K/AD-13) and 32 high level expansion channels (SYS68K/AD-14).
The SYS68K/AD-10/11 concept offers modularity and expansion to service the various application needs with the best price/performance ratio.

BLOCK DIAGRAM OF THE SYS68K/AD-10/11



Features of the SYS68K/AD-10

- 32 single ended or 16 differential A/D channels
- Four levels of resolutions are available:
  SYS68K/AD-10A : 12bit/20us
  SYS68K/AD-10B : 12bit/4us
  SYS68K/AD-10C : 14bit/35us
  SYS68K/AD-10D : 16bit/400ms
- Four different input voltage ranges are supported:
  −10V to +10V
  − 5V to + 5V
  0V to 0V
  0V to +10V
- Programmable gain amplifier (PGA)
- 80dB CMRR at a gain of 128
- Up to 0.0063% full-scale range accuracy
  ±1/2 LSB linearity error
- Channel Expansion interface for connection of the
  SYS68K/AD-12 Sample and Hold
  SYS68K/AD-13 Isolated Inputs
  SYS68K/AD-14 32 Channel Expansion
- VMEbus Interface:
  A16 : D16, D8
  Interrupter (IRQ 1-7), with software programmable IRQ vector.

Features of the SYS68K/AD-11

- The SYS68K/AD-11 contains exactly the same features as the SYS68K/AD-10 plus
- 2 Digital to Analog converter channels

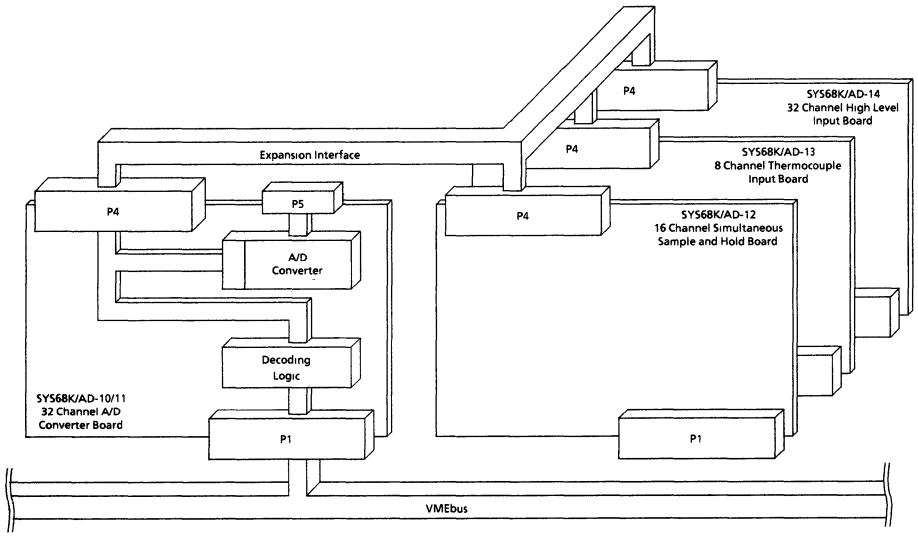
General Description

The SYS68K/AD-10/11 boards consist of a programmable gain amplifier (PGA), multiplexer, an A/D converter and storage registers. The PGA is programmable for gains from 1 to 128 in binary increments. Both the SYS68K/AD-10 and AD-11 boards are available in four models (12, 14 and 16 bit resolution) depending on the used A/D converter module. All boards, except the SYS68K/AD-10D and 11D contain a sample and hold amplifier.
The SYS68K/AD-10/11 boards contain 16 data channels built with differential inputs or up to 32 single ended data channels. The number of channels can be expanded by using the on-board expansion capabilities for connection of other input boards. The channel and control information from the channel select logic is connected to the P4 expansion connector as well as all control signals for steering the SYS68K/AD-12, -13 and -14 boards are included.
On-board jumpers allow coding of the data to be output in bipolar 2's complement, offset binary, or unipolar binary format. The analog output section on the SYS68K/AD-11 offers +1/2 LSB differential nonlinearity and operates at ±0.05 of full scale range accuracy.
All I/O signals are made available on the front panel via a 25 pin D-Sub connector.
The SYS68K/AD-10 and 11 boards consist of a 16 bit VMEbus interface using the short I/O address space for decoding.
On-board switches select the base address of the board and the access time of the SYS68K/AD-10/11 boards is jumper selectable in the range between 125 to 1000 us.
An interrupt ID register is installed on the board allowing to interrupt the host CPU if a conversion is finished. The IRQ level is jumper selectable to one of the 7 defined IRQ levels (IRQ1-7).

The Expansion Interface

The interfacing to the expansion boards is made via low cost expansion boards such as the 8 channel isolated input board, the 32 channel high level input board or the 16 channel simultaneous sample and hold board.
The interfacing to the expansion boards is made via the 25 Pin D-Sub connector available on the front panel of each board. The data to be transferred is routed only through the SYS68K/AD-10 or -11 board to minimize the overhead logic and reduce the cost for the complete system.
The expansion bus extends the number of input channels to 256.
All expansion boards are described in detail in the following pages while the principal block diagram of the expansion interface is outlined below.

BLOCK DIAGRAM OF THE EXPANSION INTERFACE



Specification of the SYS68K/AD-10

Number of Input Channels	32 single ended 16 differential
Input Voltage Range	-10V to +10V - 5V to + 5V 0V to + 5V 0V to +10V (jumper selectable)
Channel Expansion	Up to 256 single ended or differential channels with SYS68K/AD-12, -13 or -14 boards
Programmable Gain Amplifier	1, 2, 4, 8, 16, 32, 64, 128
PGA plus max. settling time	8 us at a gain of 1 12 us at a gain of 12 40 us at a gain of 64 100 us at a gain of 128
Common Mode Voltage	±10Vdc, maximum
Input Bias Current	8nA, maximum
Overvoltage Protection	±35Vdc, maximum
Input Independence	10M ohm, minimum (Differential to GND)
Common Mode Rejection	75dB at a gain of 2 80dB at a gain of 128 (±10V input signal at 60Hz minimum)
VMEbus Interface	A16 : D16, D8
AM-Codes	29, 2D, 39, 3D
Interrupts	Software Programmable IRQ vector, Jumper selectable IRQ-level

	Resolution	Maximum Conversion Time	Throughput per sec.
SYS68K/AD-10A/-12A	12	25 us	40320
SYS68K/AD-10B/-11B	12	5 us	160000
SYS68K/AD-10C/-11C	14	45 us	18667
SYS68K/AD-10D/-11D	16	400 ms	2.5

	Gain Temperature coefficient + (ppm/°C)	Zero Temperature Drift (ppm/°C)	Linearity Error (max.)
SYS68K/AD-10A/-11A	20	20	0.5 LSB
SYS68K/AD-10B/-12B	20	20	0.5 LSB
SYS68K/AD-10C/-12C	20	20	0.5 LSB
SYS68K/AD-10D/-12D	10	10	2.0 LSB

Power Requirements	+5V : 2.5A On-board DC – DC Converter generates the ±15V for the logic circuits
Operating Temperature	0 to +60 °C
Storage Temperature	–20 to +80 °C (non operational)
Relative Humidity	0 to 90% (non condensing)
Dimensions	233.5 x 160 mm (9.2 x 6.3 in.)

Additional Features of the SYS68K/AD-11

Analog Output Channels	2
Output Range	–10V to +10V 0V to + 5V 0V to +10V
Digital Coding	Bipolar 2's complement bipolar offset binary unipolar binary
Resolution, Accuracy	12bit, 0.05% minimum
Differential Non-linearity	0.5 LSB, minimum
Zero Temperature Drift	5ppm/°C, maximum
Offset Temperature Drift	20ppm/°C, maximum
Gain Temperature Drift	20ppm/°C, maximum
Setting Time	10 us, maximum
Output Current	5mA, typical
Output Independence	50mOhm, typical

Ordering Information

SYS68K/AD-10A Part No. 320002	12 Bit Analog to Digital Converter Board including documentation
SYS68K/AD-10B Part No. 320003	12 Bit Analog to Digital Converter Board (4 us data conversion time) including documentation
SYS68K/AD-10C Part No. 320004	14 Bit Analog to Digital Converter Board including documentation
SYS68K/AD-10D Part No. 320005	16 Bit Analog to Digital Converter Board including documentation
SYS68K/AD-11A Part No. 320006	12 Bit Analog to Digital Converter Board plus 2 Analog Output Channels including documentation
SYS68K/AD-11B Part No. 320007	12 Bit Analog to Digital Converter Board (4 us data conversion time) plus 2 Analog Output Channels including documentation
SYS68K/AD-11C Part No. 320008	14 Bit Analog to Digital Converter Board plus 2 Analog Output Channels including documentation
SYS68K/AD-11D Part No. 320009	16 Bit Analog to Digital Converter Board plus 2 Analog Output Channels including documentation
SYS68K/AD-10/UM Part No. 800119	Documentation for the SYS68K/AD-10 board versions
SYS68K/AD-11/UM Part No. 800120	Documentation for the SYS68K/AD-11 board versions

General Description of the SYS68K/AD-12

The SYS68K/AD-12 board is a 16 channel simultaneous sample and hold expansion board to the SYS68K/AD-10/11 board versions.
A sample and hold circuit holds or freezes a changing analog input signal for up to a few milliseconds. With 16 on-board amplifiers, the SYS68K/AD-10/11 boards may scan and convert the samples stored. The digital data represents the analog input signal values at an instant of time from all the 16 channels. This allows to measure high speed transients and spikes during a specified window of time.
For applications requiring sampling at rates up to 8M sample/s all 16 channels may be connected to a single measuring point. The sample and hold circuits may then sequentially acquire the analog input signal. In this application the SYS68K/AD-12 functions as a very low cost 8MHz storage device.
The inputs may either be single ended (up to 16) or differential (up to 8).
The specification of the SYS68K/AD-12 board is outlined together with the SYS68K/AD-13 and -14 boards.

General Description of the SYS68K/AD-13

The SYS68K/AD-13 boards is a 8 channel input board which offers 1000V peak isolation as well as thermocouple and low level inputs.
Designed specially for applications requiring multiple channel data acquisition, the SYS68K/AD-13 board expands the analog input capability of the SYS68K/AD-10/11 boards.
The SYS68K/AD-13 board is offered in two versions:
The SYS68K/AD-13T providing isolation and signal conditioning for thermocouple and low level inputs allowing to mix thermocouple and low level signals (±25.6, 51.2 and 102.4mV) on the same board.
The SYS68K/AD-13M accepting high level voltage inputs and 4 to 20mA current loop inputs.
The specification of the SYS68K/AD-13 board versions are listed together with the specification of the SYS68K/AD-12 and -14 boards.

General Description of the SYS68K/AD-14

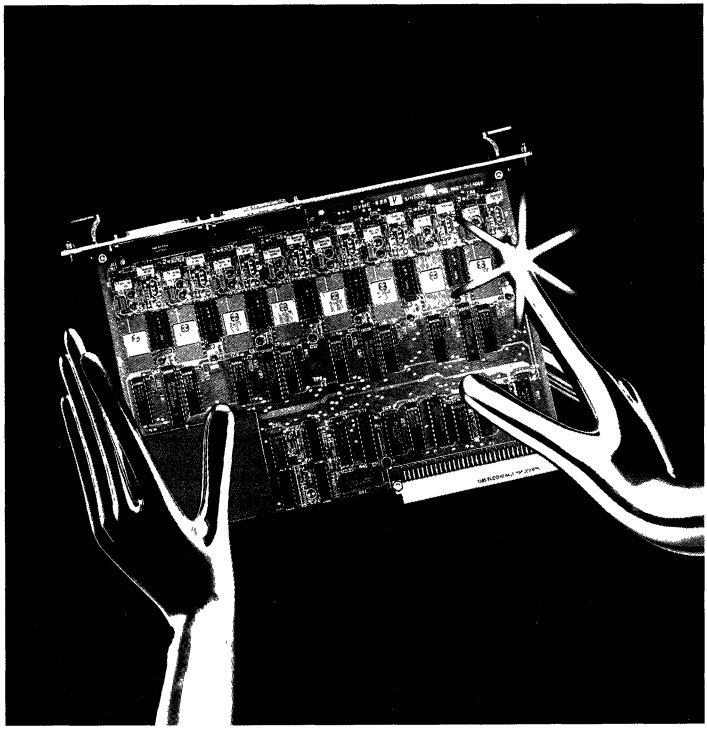
The SYS68K/AD-14 board is a 32 channel high level expansion board to the SYS68K/AD-10/11 boards.
The SYS68K/AD-14 provides 32 single ended or 16 differential expansion channels directly accepting high level inputs.
The settling time is less than 6 us with a full range accuracy of better than 0.01%.
The board externally multiplexes up to 32 input channels at the lowest cost. If more than 32 input channels are needed multiple SYS68K/AD-14 boards can be connected together supporting up to 256 different channels.

Specification

		AD-12	AD-13T	AD-13H	AD-14
Number of channels	(single)	16			32
	(differential)	8	8	8	16
Channel expansion up to		256	256	256	256
DC Input range	±(V), max.	10	0.026.6 0.051.2 0.102.4	5	10
Analog expansion interface to the SYS68K/AD-10/11 boards		yes	yes	yes	yes
VME Interface		no	no	no	no
External Trigger for Sample and Hold		yes	no	no	no
Common Mode Voltage (maximum)		±10Vdc	750V RMS 1000V peak/AC	750V RMS 1000V peak/AC	±10Vdc
DC Overvoltage Protection (V)		±35	130	130	±35
Input Independence (M Ohm)		1	–	–	100
Sample and Hold Droop Rate	(uv/us), max	2	–	–	–
Sample and Hold Pedestal	(mv), typ	1.0	–	–	–
	(mv), max	2.5	–	–	–
Output Independence	(k Ohm), max	0.5	–	–	–
Input offset Voltage	(mv), max	1	–	–	–
Input offset Voltage drift	(mV/°C) max	20			
Common Mode Rejection Ratio f=0.01 to 100MHz, (dB), min		–	120	110	–
Normal Mode Rejection 50 or 60MHz, (dB), min		–	55	55	–
Setting Time (ms), typ		–	2.5	2.5	–
DC Gain Accuracy (%FSR), min		–	0.03	0.05	0.01
Gain Drift (ppm/°C), max		–	35	35	–
Offset Drift (uV/°C), max		–	3	60	–
CJC Error (°C), max		–	1.5	1.5	–
Output Setting time (us), max (0 to 10V step)		6	–	–	6
Leakage current on channel	(nA), typ	–	–	–	0.03
on channel	(nA), max	–	–	–	60
off channel	(nA), typ	–	–	–	0.1
on channel	(nA), max	–	–	–	300
Power Consumption at 5V	(A), max	3.0	1.5	1.5	0.6
Operating Temperature	(°C), min	0	0	0	0
	(°C), max	+60	+60	+60	+60
Storage Temperature	(°C), min	–20	–20	–20	–20
	(°C), max	+85	+85	+85	+85
Relative Humidity (non condensing)	(%), min	0	0	0	0
	(%), max	90	90	90	90

Ordering Information

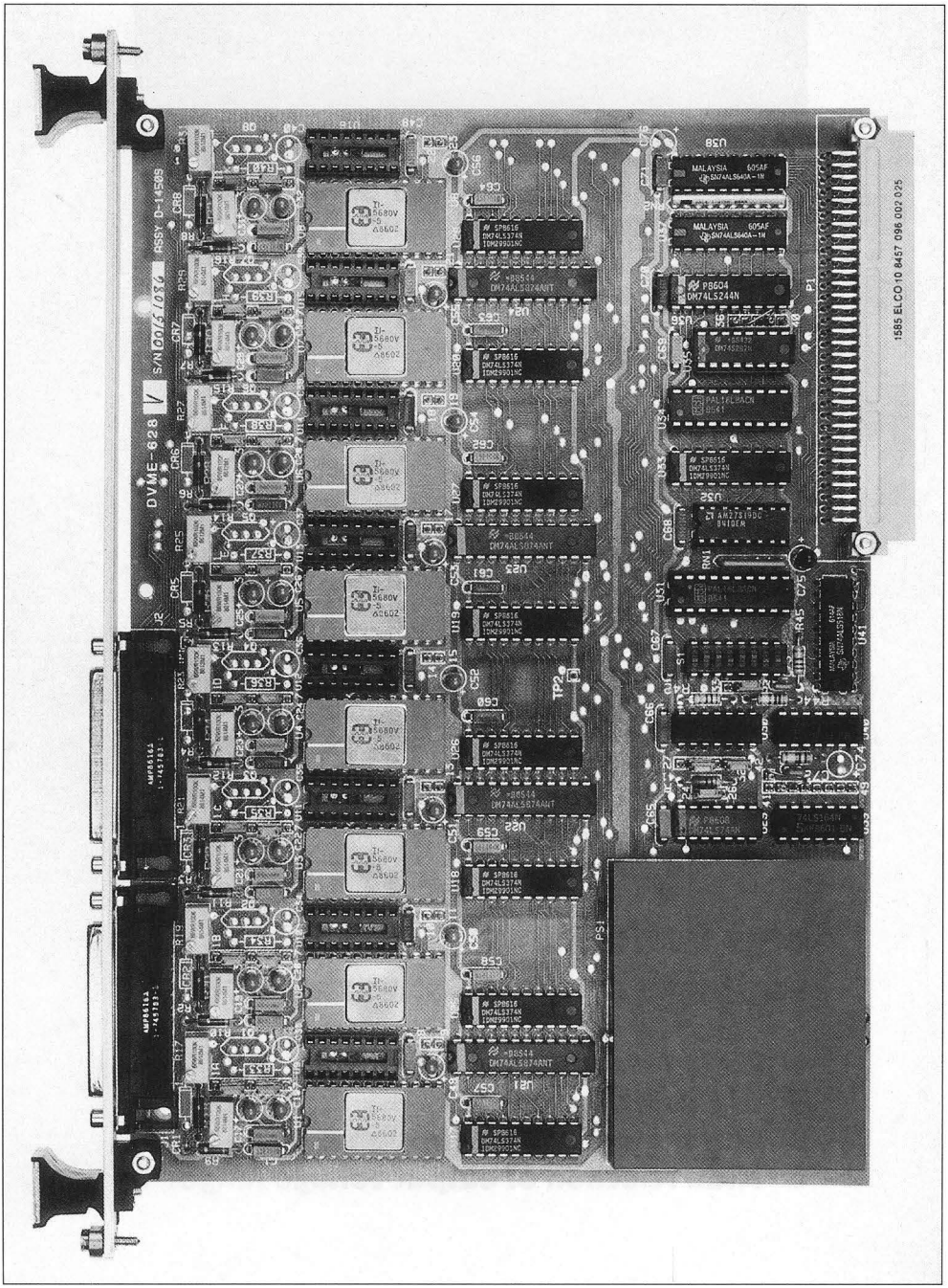
SYS68K/AD-12 Part No. 320010	16 channel Sample and Hold expansion board for the SYS68K/AD-10/11 boards. Documentation included.
SYS68K/AD-13T Part No. 320011	8 channel thermocouple input expansion board for the SYS68K/AD-10/11 boards. Documentation included.
SYS68K/AD13H Part No. 320012	8 channel high voltage and current loop expansion board for the SYS68K/AD-10/11 boards. Documentation included.
SYS68K/AD-14 Part No. 320013	32 channel high level input board for the SYS68K/AD-10/11 boards. Documentation included.
SYS68K/AD-12/UM Part No. 800121	User's Manual for the SYS68K/AD-12 board.
SYS68K/AD-13/UM Part No. 800122	User's Manual for the SYS68K/AD-13 board.
SYS68K/AD-14/UM Part No. 800123	User's Manual for the SYS68K/AD-14 board.



System 68000 VME
SYS68K/DA-1/2

High Performance
Digital to Analog Converter Boards

- **12/16 bit resolution**
- **6/8 D/A channels**
- **Current loop output optional**
- **Wide selection of output voltage ranges**

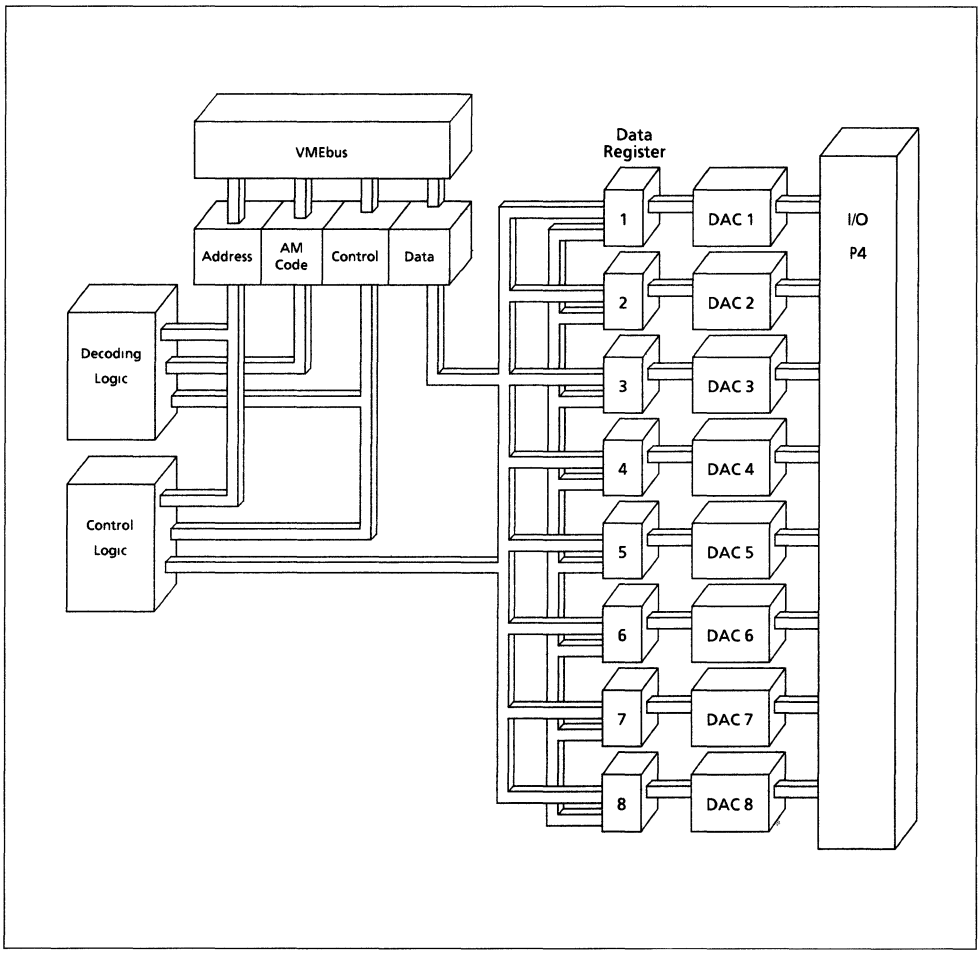

DVME-828
1585 ELCO 10 8457 096 002 025

General Description

The SYS68K/DA-1/2 boards are high speed digital to analog converter boards supporting 16 bit resolution at a maximum of 8 channels. On-board hardware resources provide 8 or 6 digital to analog conversion channels (SYS68K/DA-1 or DA-2) with a resolution of 12 or 16 bit. Both boards provide five output voltage ranges (up to +10V). The on-board dc/dc converter guarantees a full scale range accuracy of 0.05% on the SYS68K/DA-1 and 0.005% on the SYS68K/DA-2 board.
The input data format (16 bit) for the conversion can be digital data, coded bipolar's 2's complement, bipolar offset binary, or unipolar straight binary.

Functionally the SYS68K/DA-1/2 boards consist of a VMEbus interface and a digital to analog converter for each channel. A special function on the SYS68K/DA-1/2 allows to force each DAC output to 0.000V during reset regardless of whether unipolar or bipolar outputs are selected. The SYS68K/DA-1B board offers the selection between the standard voltage and current loop outputs (4 to 20 mA). The functional block diagram of the SYS68K/DA-1/2 shows the functional modules in detail.

BLOCK DIAGRAM OF THE SYS68K/DA-1



Specifications

		SYS68K/ DA-1A, 1B	SYS68K/ DA-2A	SYS68K/ DA-2B
Analog Output Channels		8	6	6
Output Voltage Range		0 to + 5V 0 to +10V ± 2.5V ± 5.0V ±10.0V	±10.0V	±5.0V
Digital Input Coding				
Bipolar 2's complement		yes	yes	yes
Bipolar offset binary		yes	yes	yes
Unipolar straight binary		yes	yes	yes
Resolution		12 Bit	16 Bit	16 Bit
Monotonicity		–	14 Bit	14 Bit
Accuracy Differential	(FSR), min.	0.05%	0.005%	0.005%
Nonlinearity	(FSR), min.	0.5LSB	0.005%	0.005%
Zero temperature drift	(ppm/°C), typ.	3	5	5
Offset temperature drift	(ppm/°C), typ.	5	8	8
Gain temperature drift	(ppm/°C), typ.	15	20	20
Settling time	(us), max.	6	15	15
Output current	(mA), typ.	±5	±5	±5
Output impedance	(mOhm), typ.	50	50	50
Current Loop				
(only on SYS68K/DA-1B) conforming to ISA standard 550.1, type 4, class U.		4 to 20	–	–
Accuracy	(FSR), min.	0.1%	–	–
Excitation	(Vdc), min.	+15	–	–
	(Vdc), typ.	+ 4	–	–
	(Vdc), max.	+36	–	–
Load resistance	(Ohm), min.	100	–	–
	(Ohm), max.	1000	–	–
VMEbus Interface				
A16 : D16, D8		x	x	x
Access time	(ns), min.	125	125	125
Access time	(ns), max.	1000	1000	1000
AM Codes supported	(HEX)	29,2D 39,3D	29,2D 39,3D	29,2D 39,3D
Power requirements	5V, max.	2.3A	3.5A	3.5A
Operating temperature	(°C)	0 to +60	0 to +60	0 to +60
Storage temperature	(°C)	–20 to +80	–20 to +80	–20 to +80
Relative humidity (non-condensing)		0 to 90%	0 to 90%	0 to 90%

Ordering Information

SYS68K/DA-1A Part No. 320014	8 channel digital to analog converter board (12 bit), inclusive documentation.
SYS68K/DA-1B Part No. 320015	8 channel digital to analog converter board (12 bit) with current loop outputs. Documentation included.
SYS68K/DA-2A Part No. 320016	6 channel digital to analog converter board (16 bit/±10V) inclusive documentation.
SYS68K/DA-2B Part No. 320017	6 channel digital to analog converter board (16 bit/0 to 10V) inclusive documentation.
SYS68K/DA-1/UM Part No. 800124	User's Manual for the SYS68K/DA-1 boards.
SYS68K/DA-2/UM Part No. 800125	User's Manual for the SYS68K/DA-2 boards.

Development Systems

FORCE Computers Systems Introduction

With the broad range of VMEbus based products currently being offered by FORCE Computers, it is clearly possible to build an enormous variety of systems. Within the standard product line, FORCE is currently offering some commonly requested configurations of boards in the form of systems. These systems are configured in one of three chassis. The top end performance systems are offered in the FORCE FOCUS 32 chassis, this chassis provides a full 32 bit, 12 slot VME environment complete with power supply and magnetic storage media. The mid range systems are offered in the 7HE, 19„ chassis complete with 9 VMEbus slots, power supply and magnetic storage media. Finally the low cost end of the system product line is realised in the 5 slot, 3HE chassis also complete with power supply and magnetic storage media.
The systems offered by FORCE Computers are complimented in software by either the PDOS real time, multitasking operating system or by the industry standard time sharing UNIX operating system.

General Feature Overview

The FORCE FOCUS 32 system is available with either UNIX (FORCE FOCUS UNIX System 25) with the SYS68K/CPU-25 or with PDOS (FORCE FOCUS PDOS System 21) with the SYS68K/CPU-21. Both systems come fully configured with SYS68K/ISIO-1, SYS68K/ISCSI-1, SYS68K/ASCU-2 and sufficient memory for the operating system. Additionally, 170 Mbyte hard disk and 1 Mbyte floppy disk drive are also provided. Also available as standard on the UNIX system and as an option on the PDOS system is a 120 Mbyte streaming tape drive.
The miniFORCE systems are all configured with the PDOS operating system and are available with a member of each of FORCE Computer's CPU board families with the exception of the CPU-3 and the CPU-24/25 families (as these two families are installed with a memory management unit, not supported by PDOS). All systems are fully configured with disk controller, magnetic media and serial I/O capability.
The microFORCE systems are all UNIX based systems, the microFORCE 2 is a 9 slot, 7 user system and the microFORCE 1A is a 5 slot, 4 user system both are configured with 2 Mbyte of DRAM and a 1 Mbyte floppy disk and a hard disk. Both systems come with UNIX reconfiguration rights.

16 Bit Development Systems

FAMILY	microFORCE		miniFORCE								
SYSTEM TYPE	–1A	–2	–1P1	–1P5	–1P6	–2P1	–2P2	–2P4	–2P5	–2P6	–2P6I
Used CPU Board Processor Type Frequency	CPU-3VB 68010 10 MHz	CPU-3VB 68010 10 MHz	CPU-1D	CPU-5V	CPU-6 68000 8 MHz	CPU-1D	CPU-2VC 68010 10 MHz	CPU-4VB 68010 12 MHz	CPU-5A 68000 16.7 MHz	CPU-6VB 68010 12 MHz	CPU-6VB 68010 12 MHz
FPCP Type	–	–			–		–	–	68881	68881	68881
Memory DRAM SRAM ROM	2 Mbyte 128 Kbyte 128 Kbyte	2 Mbyte 128 Kbyte 128 Kbyte			512 Kbyte – 256 Kbyte		1 Mbyte – 32 Kbyte	2 Mbyte 128 Kbyte 512 Kbyte	2 Mbyte 128 Kbyte 256 Kbyte	1 Mbyte – 256 Kbyte	1 Mbyte – 256 Kbyte
Storage Hard Disk Floppy Disk	50 Mbyte 1 Mbyte	85 Mbyte 1 Mbyte	Not recommended for new developments.	Not recommended for new developments.	– 2x1 Mbyte	Not recommended for new developments.	50 Mbyte 1 Mbyte	50 Mbyte 1 Mbyte	50 Mbyte 1 Mbyte	50 Mbyte 1 Mbyte	170 Mbyte 1 Mbyte
No. of Slots No. of Installed Boards No. of Free Slots	5 4 1	9 4 3*			5 2 3		9 3 4*	9 4 3*	9 4 3*	9 3 6	9 3 6
I/O Ports Serial Parallel	4 –	7 –			3 2x8 bit		7 2x8 bit	7 2x8 bit	8 –	3 2x8 bit	3 2x8 bit
VMXbus Interface	–	–			–		–	–	X	–	–
Operating System	UNIX	UNIX			PDOS		PDOS	PDOS	PDOS	PDOS	PDOS
Optional Software	◇	◇			◇◇		◇◇	◇◇	◇◇	◇◇	◇◇
Chassis	3U	7U			3U		7U	7U	7U	7U	7U
Detailed Description on Page:	453	461			433		435	435	435	435	435

Software Notes: ◇ = PASCAL, GKS
◇◇ = C, FORTRAN, PASCAL, BASIC, GKS

*With SIO-1FP removed 2 more slots are available

FAMILY	miniFORCE			
SYSTEM TYPE	–2P21S	–2P21	–2P21A	–2P21AI
Used CPU Board(s) No. of CPU Boards Processor Type Frequency	CPU-21S 1 68020 12.5 MHz	CPU-21 1 68020 16.7 MHz	CPU-21A 1 68020 20.0 MHz	CPU-21A 1 68020 20.0 MHz
FPCP Type	68881	68881	68881	68881
Memory DRAM SRAM ROM	– 512 Kbyte 512 Kbyte	– 512 Kbyte 512 Kbyte	– 512 Kbyte 512 Kbyte	– 512 Kbyte 512 Kbyte
Storage Hard Disk Floppy Disk Streamer	25 Mbyte 1 Mbyte –	50 Mbyte 1 Mbyte –	50 Mbyte 1 Mbyte –	170 Mbyte 1 Mbyte Option
No. of Slots No. of Installed Boards No. of Free Slots	9 3 6	9 3 6	9 3 6	9 3 6
I/O Ports Serial Parallel	2 –	2 –	2 –	2 –
Additional Bus Interface	VMX	VMX	VMX	VMX
Operating System	PDOS	PDOS	PDOS	PDOS
Optional Software	◇◇◇	◇◇◇	◇◇◇	◇◇◇
Chassis	7U	7U	7U	7U
Availability:	Now	Now	Now	Now
Detailed Description on Page:	445	445	445	445

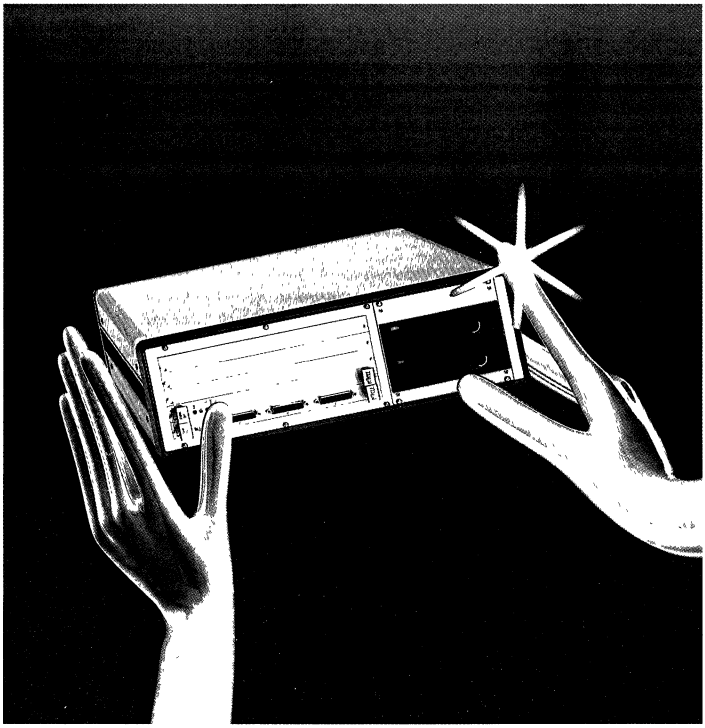
Software Notes: ◇◇◇ = C, FORTRAN, PASCAL, GKS.

32 Bit FOCUS Development Systems

FAMILY	FOCUS 32			
SYSTEM TYPE	PDOS System 21A	PDOS System 21B	System 25U	System 25A U
Used CPU Board(s) No. of CPU Boards Processor Type Frequency	CPU-21A 1 68020 20.0 MHz	CPU-21B 1 68020 25.0 MHz	CPU-25U 1 68020 16.7 MHz	CPU-25A 1 68020 20.0 MHz
FPCP Type	68881	68881	68881	68881
Memory DRAM SRAM ROM	– 1 Mbyte 512 Kbyte	– 1 Mbyte 512 Kbyte	4 Mbyte 1 Mbyte 64 Kbyte	4 Mbyte 1 Mbyte 64 Kbyte
Storage Hard Disk Floppy Disk Streamer	170 Mbyte 1 Mbyte Option	170 Mbyte 1 Mbyte Option	170 Mbyte 1 Mbyte 125 Mbyte	170 Mbyte 1 Mbyte 125 Mbyte
No. of Slots No. of Installed Boards No. of Free Slots	12 6 6	12 6 6	12 7 5	12 7 5
I/O Ports Serial Parallel	12 1	12 1	12 1	12 1
Additional Bus Interface	VMX	VMX	–	–
Operating System	PDOS	PDOS	UNIX	UNIX
Optional Software	◇◇◇	◇◇◇	◇◇◇◇	◇◇◇◇
Chassis	FOCUS 32	FOCUS 32	FOCUS 32	FOCUS 32
Availability:	Now	Now	Now	Now
Detailed Description on Page:	461	461	473	473

Software Notes: ◇◇◇ = C, FORTRAN, PASCAL, GKS
◇◇◇◇ = PASCAL, COBOL, GKS

**= Multi-processing is supported



System 68000 VME miniFORCE 1P6

- PDOS Real Time Operating System
- 3 serial and 1 parallel I/O interface
- Real Time Clock with battery back-up
- Three user application slots
- Most flexible I/O-structure
- Universal system solution

General Description

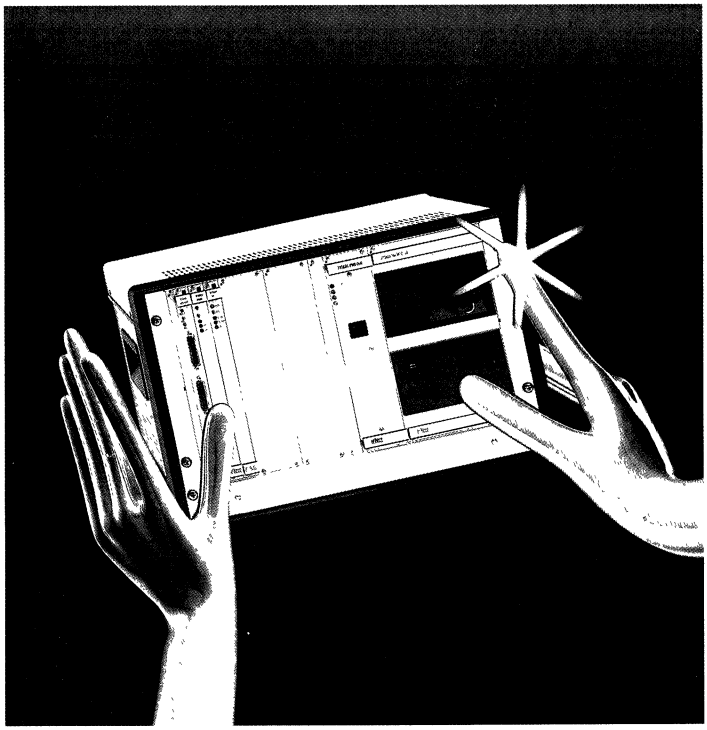
The miniFORCE 1P6 system is a universal development tool. Due to its flexible I/O structure (3 serial and 1 parallel interface) and its battery back-up Real Time Clock it is ideally suited for a wide variety of industrial applications. Two users are supported from the PDOS Real Time Operating System. PDOS offers various compilers (C, Pascal, Fortran 77) and powerful debugging tools to ease application software development.

System Configuration

- Processor 68000 (8MHz)
- Local DRAM 512 Kbyte
- 3 serial I/O ports
- Two 1 Mbyte Floppy Disks
- Real Time Clock with battery back-up
- VMEbus boards used:
  - CPU-6
  - WFC-1
  - MOTH-05A
- 3HE chassis including 160W power supply
- Operating temperature +10 to +40 degree C
- Storage temperature −10 to +50 degree C
- Humidity 0-85% non condensing

Ordering Information

miniFORCE 1P6 Part No. 620560	PDOS system with CPU-6 including documentation
SYS68K/PDOS-PAS Part No. 140020	PDOS PASCAL compiler including documentation
SYS68K/PDOS-C Part No. 140030	PDOS C compiler including documentation
SYS68K/PDOS-FOR Part No. 140040	PDOS FORTRAN 77 compiler including documentation

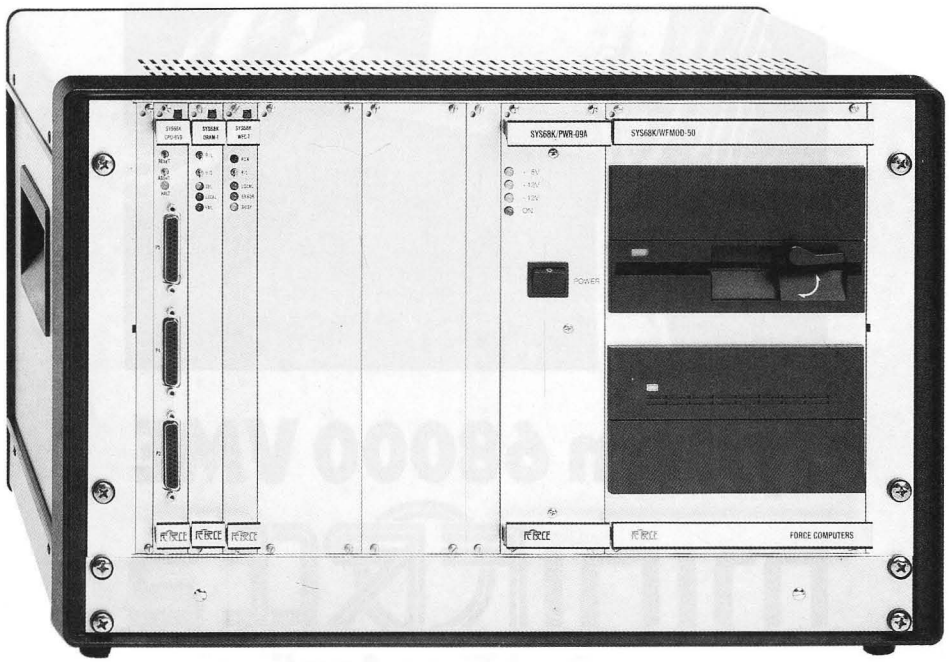


System 68000 VME

miniFORCE 2

Systems for Real Time Applications

- PDOS Real Time Operating System
- Advanced VMEbus architecture
- Wide selection of VMEbus CPU boards
- Fast realisation of complex applications
- Development = Target system
- Expandable system configuration


SYS68K/PWR-09A
SYS68K/WFMOD-50
POWER
FORCE COMPUTERS

General Description
The FORCE Computers' multi-user development systems for real time applications are low cost, high performance systems based on the VMEbus. Four different CPUs offer flexible adjustment to a wide variety of applications around the 68000/68010 CPU.
The applications of the hardware configurations include software development systems, intelligent workstations, graphics applications and numeric control systems.
The powerful real time operating system PDOS and the flexible real time kernel allow software development and test of the hard- and software in the same environment without the overhead of an emulator and a host computer.
The compilers for FORTRAN 77, C, and PASCAL allow efficient software development in conjunction with the 68000/68010 macro assembler. A system (miniFORCE 2P4) is shown on the previous page.

1.0 Hardware
The miniFORCE 2 systems are housed in a 19" enclosure which includes two quiet fans for cooling and a noise filter (RFI filter) for the fan and the power supply.
For easy installation in 19" cabinets, the complete hardware consisting of power supply, motherboard and mass storage drives, is mounted in a 19" rack. The major functions of the different hardware parts are described below:

1.1 Power Supply PWR-09A
The PWR-09A is used to power the motherboard, VME boards, as well as the disk drives. The 280W power supply drives up to 9 VME boards and offers a maximum of 36 Amps at +5V.

1.2 Motherboard MOTH-09A/09E
The VMEbus motherboard allows the interconnection of up to 9 VMEbus-based boards with a power consumption of 6A each.

1.3 Mass Memory WFMOD-50
The Winchester Floppy module includes a high speed winchester (35 ms average access time) as well as half height 1 Mbyte floppy disk. All drives (5 1/4") are included in a cassette which is mounted in the 19" rack near the power supply.

The following table lists the features of the WFMOD-50 module:

	WFMOD-50
Winchester capacity	
unformatted	51 Mbyte
formatted	39.2 Mbyte
Average Access Time including head settling Time	35 ms
MTBF	11000 h
Floppy capacity	
unformatted	1.0 Mbyte
formatted	0.8 Mbyte
Average Access Time	94 ms
MTBF	10000 h

1.3.1 Mass Memory WFMOD-175
The Winchester Floppy module includes a high speed winchester (30 ms average access time) as well as half height 1 Mbyte floppy disk. All drives (5 1/4") are included in a cassette which is mounted in the 19" rack near the power supply.
The following table lists the WFMOD-175 module:

	WFMOD-175
Winchester capacity	
unformatted	175 Mbyte
formatted (256 byte/sector)	133 Mbyte
Average Access Time	28 ms
MTBF	20000 h
Floppy capacity	
unformatted	1.0 Mbyte
formatted	0.8 Mbyte
Average Access Time	94 ms
MTBF	10000 h

1.4 VMEbus Boards
The miniFORCE-2 systems include a CPU board and various interface boards for serial I/O and winchester/floppy control. Dynamic RAM boards with byte parity check are also available to increase workspace for the operating system and/or user programs.

1.4.1 Mass Memory Interface WFC-1
The WFC-1 board controls the Winchester as well as the floppy disk drive. It contains an error detection and correction circuit as well as a 2 Kbyte sector buffer. The sector buffer allows the use of the system as a real time target system because data can't be lost during transfers to/from the WFC-1. Full asynchronous operation is performed through the flexible interrupt scheme on the board.

1.4.1.1 Mass Memory Interface ISCSI-1

The ISCSI-1 is a VMEbus based intelligent controller board. It supports a Winchester, floppy drives and each type of SCSI-bus based devices. The interfaces to the Mass Memory devices are the SCSI bus and the SA460 interface. The connected Winchester must have a SCSI Interface and the floppy a SA460 compatible interface. The board contains hashing buffers which are included on the 128 Kbyte dual ported RAM.
Intelligent commands control the Mass Memory devices. The on-board 68010 and the handling firmware control the SCSI interface and the SA460 interface after the host command is given.
The ISCSI-1 board is included on the miniFORCE-2P6I system configuration by default. All other configurations contain the WFC-1, but they can be built with the ISCSI-1 on request.

1.4.2 Serial I/O Interface SIO-2

Interconnection to terminals, printer or to host computer(s) is provided through the six channel serial I/O board. All channels are RS232 compatible and offer a strap selectable I/O signal assignment to each of the 6 D-Sub connectors mounted on the front side of the system. The front panel SIO-1FP requires two slots in the system. If more than the 3(4) remaining slots are required for application dependent boards, this front panel can be eliminated by strapping all the flat cables to the back of the system.
The multi protocol controllers (6) offer various protocols (HDLC, SDLC, X.25 etc.) as well as a software programmable baud rate (110 to 38400 Baud).

1.4.3 RAM Extension DRAM-1/2

All miniFORCE 2 systems have an additional RAM storage array on the VMEbus. 512 Kbyte or 2 Mbyte of RAM capacity (DRAM-1 or -2) are installed and offer 200 ns/300ns access time on write/read cycles. Byte parity on both boards is installed for error detection. Each system can easily be expanded by using additional RAM boards such as the DRAM-1/-2 and DRAM-E3M1/S3 (32 bit memory boards with 70ns/245ns access time).

1.5 The CPU Boards

Four different CPU boards are available for the real time development systems. Each of the boards offers different features to adapt the development system to the real time application (target system) without the need to change the CPU board for the software development.
The different features of the CPU boards are described below and are combined in Table 2.

1.5.1 CPU-6VB

This universal CPU board with 68010 processor runs out of the 512 Kbyte dynamic RAM and offers 3 serial I/O channels (asynchronous protocol with strap selectable baud rate), a parallel interface and a Real Time Clock with battery backup. Four EPROM sockets are usable on the board for various software packages (128 Kbyte). An additional 68881 Floating Point Coprocessor is implented on the CPU-6VB.

1.5.2 CPU-2VC

1 Mbyte of dual ported, dual bused dynamic RAM are installed on the CPU-2VC which contains a 68010 with 10MHz clock frequency. One serial I/O interface (RS232 with software programmable baud rate), a Real Time Clock, a parallel interface, a Floppy Disk Controller and up to 32 Kbyte of EPROM capacity complete the board.

1.5.3 CPU-4VC

A 12.5MHz 68010 running at 0 wait states out of the 128 Kbyte of static RAM with on-board battery backup, installed on the CPU-4VC. 8 sockets for JEDEC compatible devices offer a maximum of 512 Kbyte of EPROM capacity. A 4-channel DMA controller, a serial I/O channel (RS232 compatible with X.25, HDLC and SDLC protocols), a Real Time Clock (with battery backup), a parallel interface, a socket for an additional Floppy Disk Controller and the four-level VMEbus arbiter are installed the board.

1.5.4 CPU-5A

A 16.7MHz 68000 CPU is installed on the CPU-5A. Zero wait state operation at 16.7MHz is provided using the 128 Kbyte on-board static RAM. Fast Floating Point operation is performed using the 68881 Co-Processor (16.7MHz). The four-channel DMA Controller is connected to the two serial I/O channels which are built with two Multi Protocol Communications Controllers offering various protocols (X.25,SDLC, HDLC, IBM format etc.) and a software programmable baud rate (110 to 38400 Baud, 4MHz transfer rate in synchronous mode).
The primary VMXbus interface enables the board to be used in high end multiprocessor applications.

CPU Board Comparisons

	CPU-2VC	CPU-4VC	CPU-5A	CPU-6VB
CPU	68010	68010	68000	68010
Clock Frequency	10 MHz	12.5 MH	16.7 MHz	12.5 MHz
Floating Point	—	—	68881	68881
Clock Frequency	—	—	16.7 MHz	12.5 MHz
DMA Controller	—	68450	68450	—
Clock Frequency	—	8 MHz	8 MHz	—
Memory	DRAM (DPR)	SRAM	SRAM	DRAM
Capacity	1 Mbyte	128 Kbyte	128 Kbyte	512Kbyte
No. of Wait States	3	0	0	1
Serial I/O Device(s)	68561	68561	68561	6850
No. of Channels	1	1	2	3
EPROM Capacity	32 Kbyte	512 Kbyte	256 Kbyte	256 Kbyte
Parallel Interface/Timer	68230	68230	68230	68230
Real Time Clock	58167	58167	—	58167
Battery Backup	No	Yes	—	Yes
Floppy Disk Controller	WD1770	—	—	—
Status LEDs	8	8	6	—
Software Programmable IRQ Level	No	No	Yes	No
IRQ Vectors	No	Yes	Yes	No

The choice of the CPU used in the system depends on the application of the target system or on the requirements in the system's use. Benchmarks between the different hardware configurations are listed in the next chapter.

2.0 PDOS* Operating System Overview

The SYS68K/PDOS* is a powerful multi-user, multi-tasking, Real Time Operating System. PDOS* consists of a small real time kernel (6 Kbyte) which provides synchronisation and control of events occurring from the hardware using semaphores, events, messages, mailboxes and suspension primitives. The file management module supports named file access with sequential, random and shared accesses. The details of the PDOS functions are listed below:

2.1 PDOS Kernel

PDOS is written in assembly language for fast, efficient execution. The small kernel provides multi-tasking, Real-Time Clock, event processing, and memory management functions. Ready tasks are scheduled using a prioritized, round-robin method. The line A exception vector is used to interface over 74 system primitives to a user task.
Multi-Tasking Execution Environment: Tasks are the components comprising a real-time application. Each task is an independent program that shares the processor with other tasks in the system. Tasks provide a mechanism that allows a complicated application to be subdivided into several independent, understandable, and manageable modules. Real-time, concurrent tasks are allocated in 2 Kbyte increments. The task system overhead is 1.25 Kbyte.

2.2 Intertask Communication & Synchronization

Semaphores and events provide a low overhead facility for one task to signal another. Events can be used to indicate availability of a shared resource, timing pulses, or hardware interrupt occurrences. Messages and mailboxes are used in conjunction with system lock, unlock, suspend, and event primitives. PDOS* provides timing events that can be used in conjunction with desired events to prevent system lockouts. Other special system events signal character inputs and outputs.

2.3 Memory Requirements

PDOS* is very memory efficient. The PDOS* kernel, file manager, and user monitor utilities require only 16 Kbytes of memory plus an additional 4 Kbytes for system buffers and stacks. Further memory reduction can be achieved by linking the user application to a 4 Kbyte PDOS* kernel for a small, ROMable, standalone, multi-tasking module. A fast, 16 Kbyte scientific oriented BASIC interpreter with real-time primitives provides interactive high level language support as well.

2.4 File Management

The PDOS* file management module provides sequential, random, read only, and shared access to named files on a secondary storage device. These low overhead file primitives use a linked, random access file structure and a logical sector bit map for allocation of secondary storage. No file compaction is ever required. Files are time stamped with date of creation and last update. Up to 32 files can be simultaneously opened. Complete device independence is achieved through read and write logical sector primitives.

2.5 Command Line Interpreter

A resident command line interpreter allows multiple commands to be entered on a single line. Command utilities such as append, define, delete, copy, rename, and show file are also resident and can be executed without destroying current memory programs. Other functions resident in the monitor included setting the baud rate of a port, checksumming memory, creating tasks, listing tasks, files and open file status, asking for help, setting file level, file attributes, interrupt mask, and system disk, and directing console output.

2.6 Interrupt Management

The PDOS* kernel handles user console, system clock, and other designated hardware interrupts. User consoles have interrupt driven character I/O with type ahead. A task can be suspended pending a hardware or software event. PDOS* will switch control to a task suspended on an external event within 100 microseconds after the occurrence of the event (provided the system mask in high enough). Otherwise, a prioritized round-robin scheduling of ready tasks occurs at 10 millisecond intervals.

2.7 Support Tools

Numerous support utilities including virtual screen editors, assembler, linker, macroprocessor, disk diagnostics, link, and recovery, disk cataloging are standard. Single stepping, multiple break points, memory snap shots, save and restore task commands, and error trapping primitives are provided in all languages to aid in program debugging.

2.8 Language Support

The following languages are available under PDOS*:

Assembler:	A macro assembler with the full 68000/68010/68020 instruction set is included in the PDOS* system.
BASIC:	The Standard Dartmouth Basic (Interpreter) with several enhancements such as program debugging, inter-task communication and real time support are included.
C:	A complete implementation of the C-language as defined by Kernighan and Ritchie. Extensions include most of the PDOS primitives to support the real time features of PDOS.
FORTRAN 77:	Full 1977 ANSI Version of the FORTRAN language.
PASCAL:	Superset of the ISO Pascal Standard. The standard Pascal is enhanced with parallel processing capabilities from Modula.

3.0 System Configurations

Five different development systems built around the four CPU boards are available as standard configurations.
The following list of the systems shows all the differences, and the benchmarks of the PDOS running on these configurations are intended to select between the development systems.

Special configurations such as systems with expanded winchester capacity are available on request.
The miniFORCE 2 series consists of as much as 6 free VME slots for application dependent I/O boards or for memory expansion.

	miniFORCE 2P2	miniFORCE 2P4	miniFORCE 2P5	miniFORCE 2P6	miniFORCE 2P6I
Processor	68010	68010	68000	68010	68010
Frequency	10 MHz	12.5 MHz	16.7 MHz	12.5 MHz	12.5 MHz
68881 FPCP	No	No	Yes	Yes	Yes
68450 DMAC	No	Yes	Yes	No	No
Local RAM Type	DRAM	SRAM	SRAM	DRAM	DRAM
Battery Back-up	No	Yes	No	No	No
Capacity	1 Mbyte	128 Kbyte	128 Kbyte	512 Kbyte	512 Kbyte
No. of Wait States	3	0	0	1	1
VMEbus DRAM Capacity	DPR of CPU-2VC	2 Mbyte	2 Mbyte	512 Kbyte	512 Kbyte
Serial I/O Channels	7	7	8	3	3
Winchester Disk (unformatted)	51 Mbyte	51 Mbyte	51 Mbyte	51 Mbyte	175 Mbyte
Floppy Disk (unformatted)	1 Mbyte	1 Mbyte	1 Mbyte	1 Mbyte	1 Mbyte
Real Time Clock	Yes	Yes	No	Yes	Yes
Battery Back-up	No	Yes	No	Yes	Yes
Parallel Interface	Yes	Yes	No	Yes	Yes
Primary VMXbus Interface	No	No	Yes	No	No
Used VME Boards	CPU-2VC SIO-1 WFC-1 MOTH-09A/E	CPU-4VC DRAM-2 SIO-1 WFC-1 MOTH-09A/E	CPU-5A DRAM-2 SIO-1 WFC-1 MOTH-09A/E	CPU-6VB DRAM-1 WFC-1 MOTH-09A/E	CPU-6VB DRAM-1 ISCSI-1 MOTH-09A/E
No. of Free Slots	4/6**	3/5*	3/5*	6	6
Power Supply	PWR-09A	PWR-09A	PWR-09A	PWR-09A	PWR-09A
Mass Memory	WFMOD-50	WFMOD-50	WFMOD-50	WFMOD-50	
Housing	CHAS 19-09/7U	CHAS 19-09/7U	CHAS 19-09/7U	CHAS 19-09/7U	CHAS 19-09/7U
Weight	max 23 kg (51 lbs)				
Dimensions	344 mm x 520 mm x 400 mm				

3/5* 3 slots are free if the SIO front panel is installed and 5 slots are unused if the SIO cables are connected to the back of the system (user supplied option).

4/6** 4 slots are free if the SIO front panel is installed and 6 slots are unused if the SIO cables are connected to the back of the system (user supplied option).

Benchmark

	miniFORCE 2P2	miniFORCE 2P4	miniFORCE 2P5	miniFORCE 2P6
10.000.000 Nops	23.31 s	10.50 s	8.18 s	12.70 s
100.000 Context Switches	16.32 s	6.85 s	5.32 s	9.00 s
100.000 Read time of day	30.69 s	14.38 s	11.72 s	17.97 s
100.000 Set System event	20.01 s	8.47 s	6.62 s	11.03 s
100.000 Test System event	11.47 s	4.81 s	3.73 s	6.33 s
100.000 Resource allocations	42.33 s	17.86 s	14.11 s	23.25 s
100.000 Send and Receive 64 bytes	81.10 s	36.50 s	34.76 s	46.58 s
100.000 Task Synchronisations	86.63 s	36.39 s	28.83 s	47.57 s
100.000 Lock and Unlock file	70.90 s	30.34 s	23.91 s	40.00 s
100.000 10-byte record rereads	83.49 s	36.23 s	28.71 s	47.41 s
Overall Performance	0.97 s	2.24 s	2.73 s	1.75 s

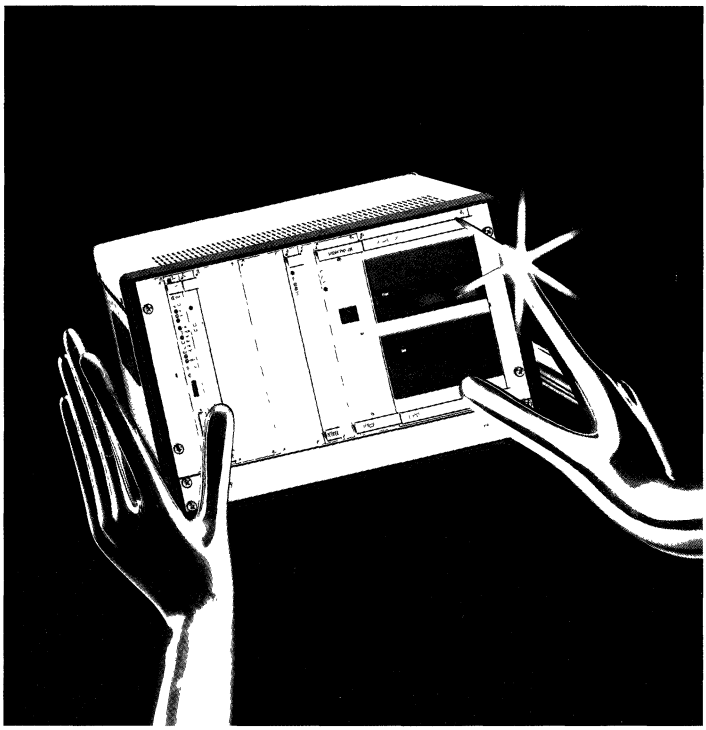
Ordering Information

System Configuration including PDOS

miniFORCE 2P2 Part No. 620620	PDOS* system with CPU-2VC and documentation
miniFORCE 2P4 Part No. 620640	PDOS* system with CPU-4VC and documentation
miniFORCE 2P5 Part No. 620650	PDOS* system with CPU-5A and documentation
miniFORCE 2P6 Part No. 620660	PDOS* system with CPU-6VB and documentation
miniFORCE 2P6I Part No. 620662	PDOS* system with CPU-6VB, 170 Mbyte SCSI disk and
SYS68K/PDOS-UM Part No. 800031	Software User's Manual for the PDOS Operating System including BASIC Documentation
SYS68K/SIO-1LC Part No. 310014	Long cable set (6pcs a 50cm) for connection of the 6 SIO channels to the back of the system

Language Support for PDOS

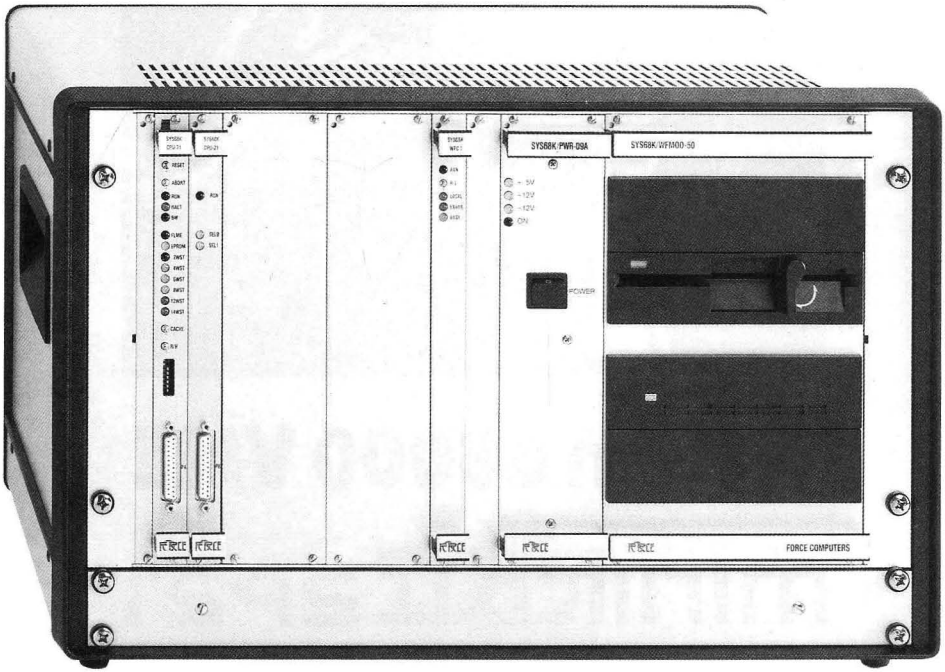
SYS68K/PDOS-PAS Part No. 140 020	PASCAL-Compiler for PDOS inclusive documentation
SYS68K/PDOS-C Part No. 140030	C-Compiler for PDOS inclusive documentation
SYS68K/PDOS-FOR Part No. 140040	FORTRAN-77 Compiler for PDOS inclusive documentation



System 68000 VME

miniFORCE 2P21

- **PDOS Real Time Operating System**
- **Advanced VMEbus architecture**
- **Fast realisation of complex applications**
- **32 bit Development/Target system**
- **Up to 3.5 MIPS system performance**


SYS68K/PWR-09A
SYS68K/VFM00-50
FORCE COMPUTERS

General Description
The miniFORCE 2P21 multi-user development/target system for realtime applications is a high performance system at low cost based on the VMEbus. A 16,7 MHz 68020 CPU is used on the SYS68K/CPU-21 offering a real computing power of 2.5 to 3.5 MIPS running without wait states out of the 512 Kbyte on board static RAM.
The powerful multi-tasking real time operating system PDOS* allows efficient and fast software development, as well as the testing of the used hard and software in the same environment without the overhead of an emulator and a host computer. The FORTRAN 77 and the C-compiler allow easy software development in conjunction with the macro assembler.

1.0 Hardware
The miniFORCE 2P21 is housed in a 19″ enclosure which includes three quiet fans for cooling and a noise filter (RFI filter) for the fans and the power supply.
For easy installation in 19″ cabinets, the complete hardware consisting of power supply, motherboards and mass storage drives, is mounted in a 19″ rack. The major functions of the different hardware parts are described below:

1.1 Power Supply PWR-09A
The PWR-09A is used to power the VME boards, as well as the disk drives. The 280W power supply drives up to 9 VME boards and offers a maximum drive capacity of 36 Amps at +5V.

1.2 Motherboard MOTH-09A and MOTH-E09A
The VMEbus motherboard allows the interconnection of up to 9 VMEbus-based boards 8, 16 and 32 bit data transfers are supported.

1.3 Mass Memory WFMOD-50
The Winchester Floppy module includes a high speed, half height winchester (35 ms average access time) as well as half height 1 Mbyte floppy disk. All drives (5 1/4″) are included in a cassette which is mounted in the 19″ rack near to the power supply.
The following table lists the features of the WFMOD-50 module used in the miniFORCE 2P21 and 2P21A. The disk capacity of the 2P21S configuration is 25 Mbyte.

	WFMOD-50
Winchester capacity	
unformatted	51.0 Mbyte
formatted	39.2 Mbyte
Average Access Time including head settling Time	35 ms
MTBF	11000 h
Floppy capacity	
unformatted	1.0 Mbyte
formatted	0.8 Mbyte
MTBF	10000 h

1.3.1 Mass Memory WFMOD-175
The Winchester Floppy module includes a high speed Winchester (30 ms average access time) as well as half height 1 Mbyte floppy disk. All drives (5 1/4″) are included in a cassette which is mounted in the 19″ rack near the power supply.
The following table lists the WFMOD-175 module:

	WFMOD-175
Winchester capacity	
unformatted	175.0 Mbyte
formatted (256 byte/sector)	133.0 Mbyte
Average Access Time	28 ms
MTBF	20000 h
Floppy capacity	
unformatted	1.0 Mbyte
formatted	0.8 Mbyte
Average Access Time	94 ms
MTBF	10000 h

1.4 The CPU-board CPU-21
The powerful SYS68K/CPU-21 is used as the processor board in the miniFORCE 2P21. Zero wait state operation at 16.7 MHz is performed using the 512 Kbyte static RAM. The computing power is in the range of 2.5 to 3.5 MIPS.
The on-chip cache of the 68020 CPU is fully supported in the real time operating system and peaks the throughput at cache only cycles to as much as 5 MIPS.
A Floating Point Co-Processor with 16.7 MHz clock frequency is provided on the board to allow efficient execution of user supplied programs.
On the miniFORCE 2P21S the SYS68K/CPU-21S running at 12.5 MHz with zero wait state is used. The most powerful system the miniFORCE 2P21A uses the SYS68K/CPU-21A working at 20MHz in zero wait state operation.

Features of the SYS68K/CPU-21
- 68020 CPU with a clock frequency of 16.7 MHz
- 68881 Floating Point Co-Processor (16.7 MHz)
- Two 68561 Multi-Protocol Communication Controllers for Serial I/O (one RS232 and one RS232/RS422 compatible interface)
- 68230 Parallel Interface and Timer for local control, interrupt level control and timer function
- 68153 Bus Interrupter Module for all local interrupts
- 512 Kbyte of zero wait state static RAM via the FLME interface (jumper selectable access address)
- 4 Sockets for EPROMs (32-bit wide) for 8K x 8 to 64K x 8 organised devices.
- 4 Sockets for EPROMs/SRAMs (32-bit wide) for 8K x 8 to 64K x 8 organized devices.
- Maximum capacity:

EPROM	SRAM	Comment
512 Kbyte	0	only EPROM
256 Kbyte	128 Kbyte	EPROM and SRAM

- Fully buffered local address data and control bus
- VMX Primary Master Interface (32-bit wide)
- IEEE 1014 interface supporting unaligned transfer (32-bit)
- Single level bus arbiter
- Software selectable bus release functions (6)
- Interrupt handler (1-7 static)
- Bus Timer for BERR generation on local bus, VME/P1014 bus and VMXbus
- Power Fail Detector and RESET generator
- RESET and ABORT switch
- RUN/HALT switch
- CACHE enable/disable switch
- RUN/HALT/Bus Master/SRAM Access and Wait State indication LEDs
- VMEPROM is included

Different features of the SYS68K/CPU-21S
- 68020 CPU with a clock frequency of 12.5 MHz
- 68881 Floating Point Coprocessor (12.5 MHz)

Different features of the SYS68K/CPU-21A
- 68020 CPU with a clock frequency of 20 MHz
- 68881 Floating Point Coprocessor of 20 MHz

1.5 Mass Memory Interface WFC-1

The WFC-1 board controls the winchester as well as the floppy disk drive (5 1/4 ″). It contains an error detection and correction circuit as well as a 2 Kbyte sector buffer. The sector buffer allows the usage of the system as a real time target system because data can not be lost during transfers to/from the WFC-1. Full asynchronous operation is performed through the flexible interrupt scheme on the board.

1.5.1 Mass Memory Interface ISCSI-1

The ISCSI-1 is a VMEbus based intelligent controller board. It supports Winchester, floppy drives and each type of SCSI-bus based devices. The interfaces to the Mass Memory devices are the SCSI bus and the SA460 inteface. The connected Winchester must have a SCSI Interface and the floppy a SA460 compatible interface. The board contains hashing buffers which are included on the 128 Kbyte dual ported RAM.
Intelligent commands control the Mass Memory devices. The on-board 68010 and the handling firmware control the SCSI interface and the SA460 interface after the host command is given.
The ISCSI-1 board is included on the miniFORCE-2P21AI system configuration by default. All other configurations contain the WFC-1 but they can be delivered with the ISCSI-1 on request.

2.0 Preferred VMEbus Boards for system extension

The miniFORCE 2P21 is a full 32 bit VMEbus based system and provides the maximum throughput if the processor runs within the local SRAM. A memory extention of the 512 Kbyte RAM can be made via a SRAM-22 board or via global memory boards on the VMEbus.
For systems where global memory has to be used, a 32 bit memory board is the best solution to improve throughput and execution speed.
Additional memory is automatically detected and used by the PDOS operating system if it is continuous to the local memory.
Additional I/O channels are supported through the SIO-2 board as well as through the advanced system control unit ASCU-1/2.

3.0 PDOS* Operating System Overview

The SYS68K/PDOS* is a powerful multi-user, multi-tasking, Real Time Operating System. PDOS* consists of a small real time kernel (6 Kbyte) which provides synchronisation and control of events occurring from the hardware using semaphores, events, messages, mailboxes and suspension primitives.
The file management module supports named file access with sequential, random and shared accesses.

3.1 PDOS Kernel

PDOS* is written in assembly language for fast, efficient execution. The small kernel provides multitasking, Real-Time Clock, event processing, and memory management functions. Ready tasks are scheduled using a prioritized, round-robin method. The line A exception vector is used to interface over 74 system primitives to a user task.
Multi-Tasking execution environment: Tasks are the components comprising a real-time application. Each task is an independent program that shares the processor with other tasks in the system. Tasks provide a mechanism that allows a complicated application to be subdivided into several independent, understandable, and manageable modules. Real-time, concurrent tasks are allocated in 2 Kbyte increments. The task system overhead for each task is only 1.25 Kbyte.

3.2 Intertask Communication & Synchronization

Semaphores and events provide a low overhead facility for one task to signal another. Events can be used to indicate availability of a shared resource, timing pulses, or hardware interrupt occurrences. Messages and mailboxes are used in conjunction with system lock, unlock, suspend, and event primitives. PDOS* provides timing events that can be used in conjunction with desired events to prevent system lockouts. Other special system events signal character inputs and outputs.

3.3 Memory Requirements

PDOS* is very memory efficient. The PDOS* kernel, file manager, and user monitor utilities require only 16 Kbyte of memory plus an additional 6 Kbyte for system buffers and stacks. Further memory reduction can be achieved by linking the user application to a 6 Kbyte PDOS* kernel for a small, ROMable, standalone, multi-tasking module.

3.4 File Management

The PDOS* file management module provides sequential, random, read only, and shared access to named files on a secondary storage device. These low overhead file primitives use a linked, random access file structure and a logical sector bit map for allocation of secondary storage. No file compaction is ever required. Files are time stamped with date of creation and last update. Up to 32 files can be simultaneously opened. Complete device independence is achieved through read and write logical sector primitives.

3.5 Command Line Interpreter

A resident command line interpreter allows multiple commands to be entered on a single line. Command utilities such as append, define, delete, copy, rename, and show file are also resident and can be executed without destroying current memory programs. Other functions resident in the PDOS* monitor include setting the baud rate of a port, checksumming memory, creating tasks, listing tasks, files and open file status, asking for help, setting file level, file attributes, interrupt mask, and system disk, and directing console output.

3.6 Interrupt Management

The PDOS* kernel handles user console, system clock, and other designated hardware interrupts. User consoles have interrupt driven character I/O with type ahead. A task can be suspended pending a hardware or software event. PDOS* will switch control to a task suspended on an external event within 100 microseconds after the occurrence of the event (provided the system mask is high enough). Otherwise, a prioritized round-robin scheduling of ready tasks occurs in 10 millisecond intervals.

3.7 Support Tools

Numerous support utilities including virtual screen editors, assembler, linker, macroprocessor, disk diagnostics, link, and recovery, disk cataloging are additional standard functions in the PDOS*. Single stepping, multiple break points, memory snap shots, save and restore task commands, and error trapping primitives are provided for program debugging.

3.8 Language Support

The following languages are available under PDOS*:

Assembler:	A macro assembler with the full 68020 instruction set is included in the PDOS* system.
C:	A complete implementation of the C-language as defined by Kernighan and Ritchie is available as an option. Extensions include most of the PDOS primitives to support the real time features of PDOS.
FORTRAN77:	Full ANSI 77 Version of the FORTRAN language is available as an option.
PASCAL:	Full Jensen/Wirth implementation of the ISO PASCAL standard is under development.

4.0 System Configuration

The basic configuration of a 32 bit development system is realised in the miniFORCE 2P21 Real Time System.
The miniFORCE 2P21 consists of 6 unused VME slots for application dependent I/O boards or memory expansion.
All 6 unused slots are supported from the included power supply.
Special configurations including additional boards are available on request.

System Configurations

	miniFORCE 2P21	miniFORCE 2P21S	miniFORCE 2P21A	miniFORCE 2P21AI
Processor	68020	68020	68020	68020
Frequency	16,7MHz	12,5MHz	20MHz	20MHz
Floating Point CoProcessor	68881	68881	68881	68881
Frequency	16,7MHz	12,5MHz	20MHz	20MHz
Local RAM Type	SRAM	SRAM	SRAM	SRAM
Capacity	512 Kbyte	512 Kbyte	512 Kbyte	512 Kbyte
No. of Wait States	0	0	0	0
Data Transfer Size	8, 16, 24 and 32 Bit	8, 16, 24 and 32 Bit	8, 16, 24 and 32 Bit	8, 16, 24 and 32 Bit
Serial I/O Channels	2	2	2	2
RS232	1 + 1	1 + 1	1 + 1	1 + 1
RS422	1	1	1	1
Winchester Disk unformatted	51 Mbyte	25 Mbyte	51 Mbyte	175 Mbyte
Floppy Disk unformatted	1 Mbyte	1 Mbyte	1 Mbyte	1 Mbyte
VMEbus Interrupt Handler	1-7 dyn.	1-7 dyn.	1-7 dyn.	1-7 dyn.
Single Level Arbiter	Yes	Yes	Yes	Yes
Primary VMXbus Interface	A24:D8,D16, D24,D32	A24:D8,D16, D24,D32	A24:D8,D16, D24,D32	A24:D8,D16, D24,D32
VMEbus Interface	A32:D8,D16, D24,D32 A24:D8,D16, D24,D32 A16:D8,D16, D24,D32	A32:D8,D16, D24,D32 A24:D8,D16, D24,D32 A16:D8,D16, D24,D32	A32:D8,D16, D24,D32 A24:D8,D16, D24,D32 A16:D8,D16, D24,D32	A32:D8,D16, D24,D32 A24:D8,D16, D24,D32 A16:D8,D16, D24,D32
Used VME Boards	CPU-21 WFC-1 MOTH-09A MOTH-E09A	CPU-21S WFC-1 MOTH-09A MOTH-E09A	CPU-21A WFC-1 MOTH-09A MOTH-E09A	CPU-21A ISCSI-1 MOTH-09A MOTH-E09A
No of Free Slots	6	6	6	6
Power Supply	PWR-09A 36A at 5V	PWR-09A 36A at 5V	PWR-09A 36A at 5V	PWR-09A 36A at 5V
Mass Memory	WFMOD-50	WFMOD-20	WFMOD-50	WFMOD-175
Housing	19″	19″	19″	19″
Weight	max 23kg (51 lbs)			
Dimensions	344 mm x 520 mm x 400 mm			
Operating Temperature	5–45°C			
Relative Humidity	5–85 % (non condensing)			

System Benchmarks

	miniFORCE 2P21	miniFORCE 2P21S	miniFORCE 2P21A
100.000 Bench BIAS	0.05 s	0.06 s	0.04 s
100.000 Task Rescheduling	3.68 s	4.94 s	3.15 s
100.000 Set System Event	1.88 s	2.56 s	1.62 s
100.000 Set Event w/Rescheduling	4.38 s	5.88 s	3.78 s
100.000 Change Task Priority	2.99 s	3.86 s	2.47 s
100.000 Read Time of Day	1.87 s	2.32 s	1.63 s
100.000 Send and Receive 64 Bytes	17.39 s	23.46 s	14.86 s
100.000 Send and Receive 4 Bytes	4.96 s	6.97 s	4.35 s
100.000 Resources Allocutions	6.71 s	9.01 s	5.74 s
100.000 Task Synchronisations	19.66 s	26.49 s	16.86 s

The benchmarks are performed with CPU-21/CPU-21S/CPU-21A at 16,7/12,5/20MHz processor clock frequency and cache enabled. In addition one background task is running by default in the PDOS system.

Ordering Information

System Configuration

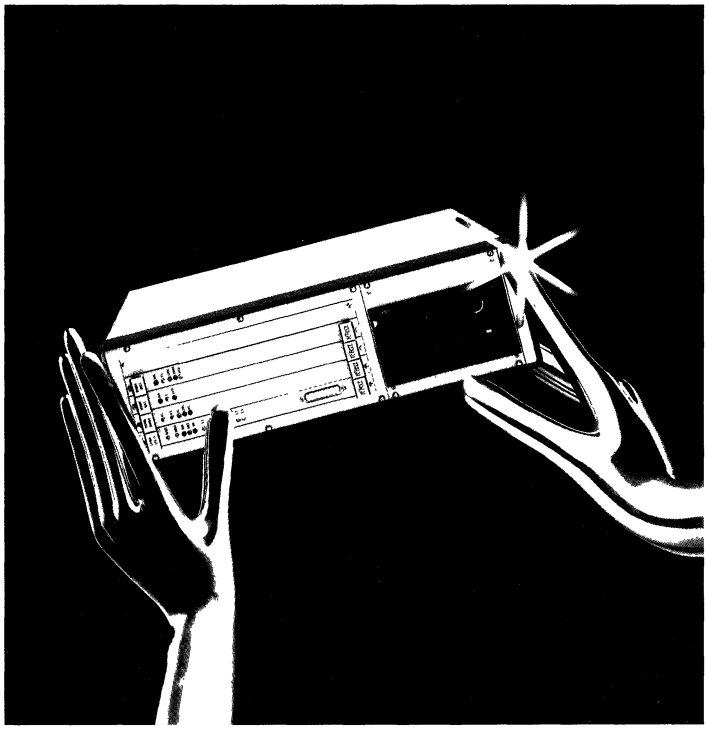
miniFORCE 2P21 Part No. 620700	PDOS System with CPU-21 and documentation
miniFORCE 2P21S Part No. 620710	PDOS System with CPU-21S and documentation
miniFORCE 2P21A Part No. 620720	PDOS System with CPU-21A and documentation
miniFORCE 2P21AI Part No. 620722	PDOS System with CPU-21A, ISCSI-1 and documentation
SYS68K/PDOS-UM/21 Part No. 800031	Software Users Manual for the PDOS Operating System

Language support

SYS68K/PDOS-C020 Part No. 140031	C-Compiler for PDOS inclusive documentation
SYS68K/PDOS-FOR020 Part No. 140041	FORTRAN-77 Compiler for PDOS inclusive documentation
SYS68K/PDOS-PAS020 Part No. 140021	PASCAL Compiler for PDOS inclusive Documentation

Extensions

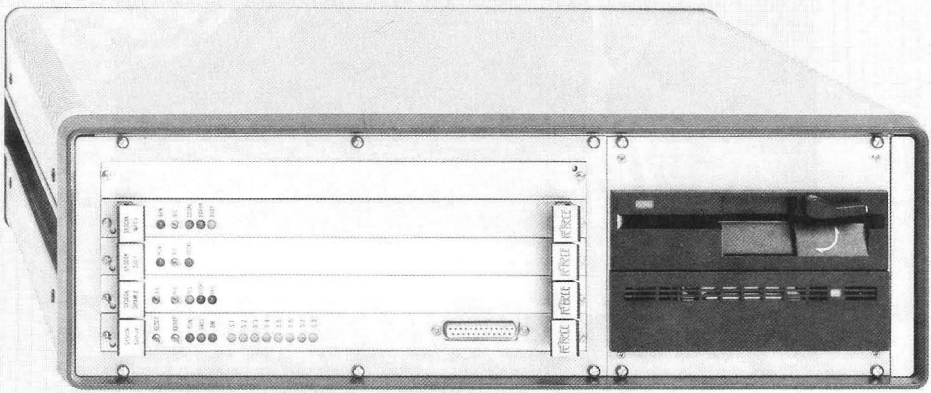
SYS68K/SRAM-22 Part No. 201000	Zero Wait State 512 Kbyte static RAM extention for CPU-21
SYS68K/SRAM-22S Part No. 201040	Zero Wait State 512 Kbyte static RAM extention for CPU-21S
SYS68K/SRAM-22A Part No. 201010	Zero Wait State 512 Kbyte static RAM extention for CPU-21A
SYS68K/DRAM-E3M1 Part No. 200004	1 Mbyte 32-bit VMEbus dynamic RAM board including documentation
SYS68K/SIO-2 Part No. 310004	6 channel serial I/O board including documentation
SYS68K/ASCU-2 Part No. 700007	System Control Unit including IEEE488, 1 serial I/O and one Parallel Interface. Documentation included



System 68000 VME

microFORCE 1A

- **Compact UNIX development system**
- **Flexible configuration**
- **VMEbus based**



General Description

The microFORCE 1A series is a low cost VMEbus-based configuration which incorporates all the nessary hardware components including mass memory drives for the powerful UNIX* SYSTEM V operating system.
All VME modules which are required to run the multiuser, timesharing, multitasking, powerful UNIX* SYSTEM V are housed in a 3HE 19" rack enclosure.
The microFORCE 1A is an open system and the reconfiguration rights are included. Therefore, the free slot can be used for the implementation of additional controllers.

The Hardware

microFORCE 1A

- 68010 (10MHz) based CPU
- Global memory 2 Mbyte
- 128 Kbyte on CPU board
  no-wait-state static RAM
- Four serial I/O channels
  - two users ports
  - printer port
  - communication port
- Winchester Disk 51 Mbyte
  35ms average access time
- Floppy Disk 1 Mbyte
- One free VMEbus slot
- 160W power supply which
  supports fully populated system

The Software

1. UNIX* System V Release 2

The popular multiuser timesharing multi-tasking operating system UNIX* V is implemented. Both systems offer all the features known to UNIX* and include the C-compiler, 68000 assembler, F77 compiler, and screen editor. Additional high level languages such as Pascal are optional.
The systems contain sufficient memory and disk memory capacity (2/51 Mbyte) to allow efficient multiuser operation.

Comparisons
The following table of benchmarks running under UNIX* shows the microFORCE 1A.

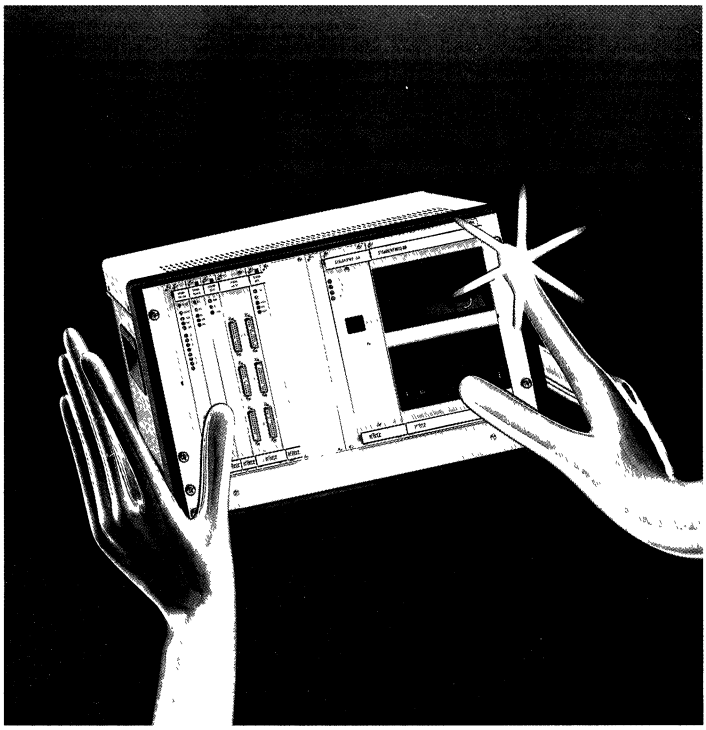
Benchmark	microFORCE-1A		
	Real	User	System
Pipes	4.9s	0s	2.2s
System Call	6.2s	0.5s	5.6s
C-compile of pipes, C	20.8s	6.7s	8.8s
Multishell	15.2s	3.9s	8.1s

Specifications

	microFORCE 1A
CPU (68010):	10MHz
MMU (68451):	10MHz
DMA (68450):	10MHz
Serial I/O (RS232):	4 channels
Real Time clock with battery back-up:	Yes
Cache (no wait states)	128 Kbyte
Global Memory with parity:	2 Mbyte
Floppy (SA450):	1 Mbyte
Winchester (ST506):	51 Mbyte
Case:	19" enclosure with 5-slot VMEbus motherboard
Power supply:	160W for up to 5 VMEbus boards
Power requirements:	110/220V at 50-60 Hz
Cooling:	2 low noise fans on the backside
Overall dimensions:	W/H/D: 471mm x 147mm x 462mm
Operating Temperature	5–40 degr. C
Relative Humidity	5–85% (non condensing)

Ordering Information

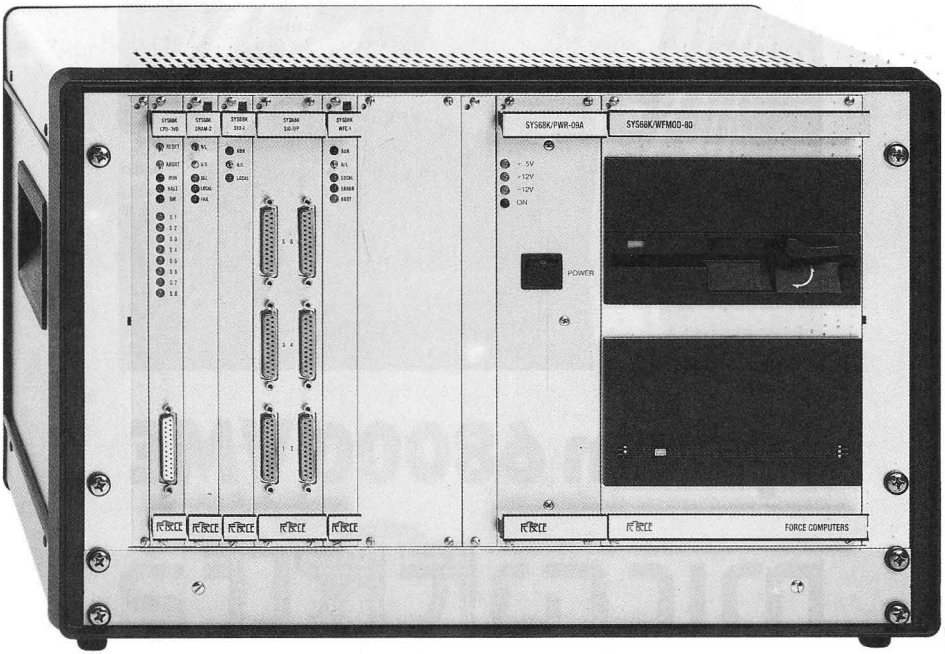
microFORCE 1A Part No. 630005	VMEbus-based system UNIX* System V operating system including FORTRAN 77 Compiler and appropriate documentation
microFORCE 1A/2/UM Part No. 800113	User's Manual for microFORCE 1A
SYS68K/UNIX-PAS Part No. 150005	PASCAL Compiler including documentation



System 68000 VME

microFORCE 2

- **Flexible, expandable VMEbus system**
- **UNIX SYSTEM V operating system**
- **Multiuser configuration**
- **85 Mbyte Winchester**


SYS68K/PWR-09A
SYS68K/WFMOD-80
+ 5V
+12V
-12V
ON
POWER
FORCE COMPUTERS

General Description
The microFORCE 2 is a VMEbus-based computer system which incorporates the hardware and software to perform efficient software development under UNIX* for 68000-based applications.
The application field of the microFORCE 2 includes software development systems, intelligent workstations, and emulation workstations for VMEbus target systems.

The Hardware
The microFORCE 2 system is housed in a 19" rack and cabinet including 9 VMEbus slots and all utilities such as power supply, power cable and switches, fans and noise filter (RFI filter).
The hardware features of the microFORCE 2 include:

- Powerful 68010-based CPU
- 128 Kbyte of no-wait-state static RAM
- Main memory with 2 Mbyte and parity check
- 7 RS232C-compatible serial I/O ports
- Winchester disk with 85 Mbyte capacity
- Floppy disk with 1 Mbyte capacity
- 3/4 free VMEbus slots
- 280W power supply which supports fully populated systems

The Software

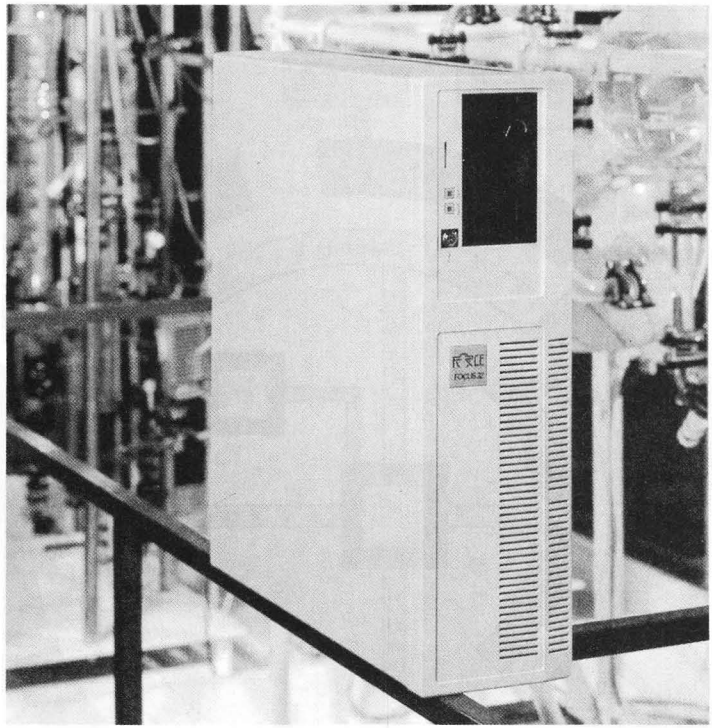
UNIX* System V Release 2:
The popular timesharing multiuser multitasking operating system UNIX SYSTEM V is used on the microFORCE 2. This system offers all the features known from UNIX and the standard system includes the FORTRAN 77 and C-compiler, 68000 assembler, reconfiguration rights and screen editor. Additional high level languages, such as Pascal are optionally available.
The system contains fast memory and 85 Mbyte disk capacity to allow efficient multiuser operation for up to 6 users.

Specifications

CPU:	68010 (10 MHz)
MMU:	68451 (10 MHz)
DMA:	68450 (10 MHz)
Serial I/O:	7 channels (RS232-compatible)
Real Time Clock	58167 with battery backup
Cache:	128 Kbyte (no-wait-state operation)
Global Memory:	2 Mbyte (with byte parity)
Floppy:	1 Mbyte (5 1/4") slim line
Winchester:	85 Mbyte (5 1/4") 25ms average access time
Case:	19" enclosure with 9-slot VMEbus motherboard
Power Supply:	280W for up to 9 VMEbus boards
Power Requirements:	110/220V at 50-60Hz
Cooling:	2 low noise fans on the back side
Overall Dimensions:	W/H/D 520mm x 340mm x 400mm
System Configuration:	SYS68K/CPU-3VB, SYS68K/DRAM-2, SYS68K/SIO-1, SYS68K/WFC-1
Operating Temperature	5–40 deg. C
Relative Humidity	5–85% (non condensing)

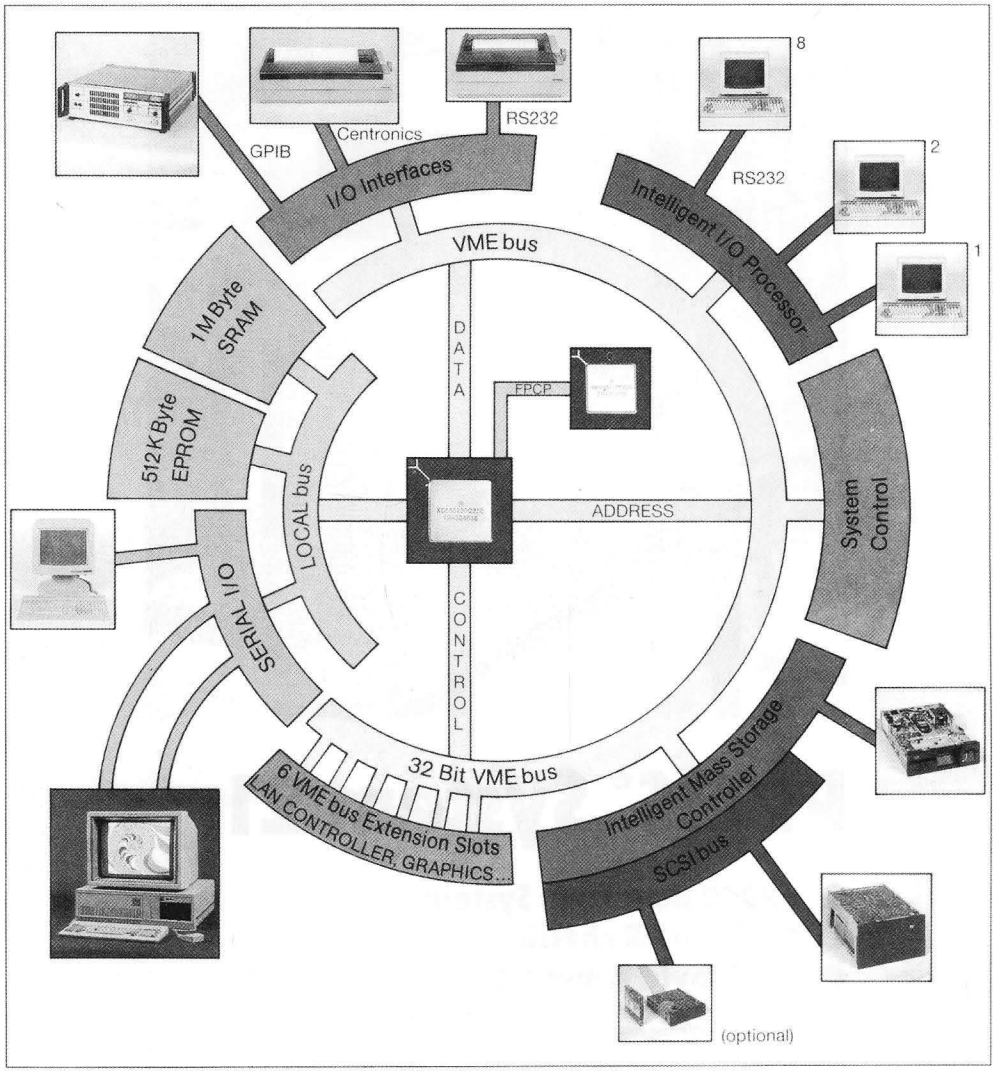
Ordering Information

microFORCE 2 Part No. 630010	VMEbus-based system with UNIX* SYSTEM V operating system including documentation
microFORCE-1A/2/UM Part No. 800113	User's Manual for the microFORCE 2
SYS68K/UNIX-PAS Part No. 150005	PASCAL Compiler including documentation



PDOS* System 21

- 68020 Real Time System
- 12 slot VME chassis
- 175 Mbyte Winchester

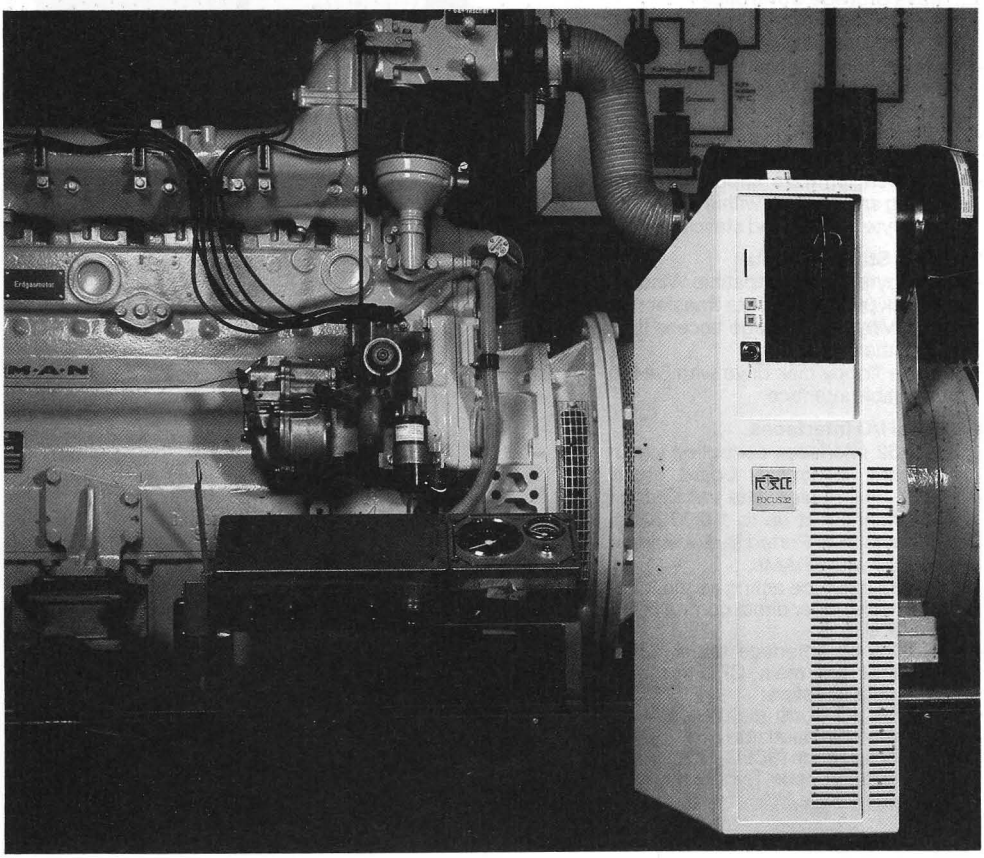


PDOS* is a trademark of Eyring Research Institute

General Description

The FOCUS 32 series of products are full 32 bit target and development systems based on the VMEbus.
All the serial I/O communications to the terminals or host computers as well as the mass memory device control are made via intelligent controller boards.
The PDOS* System 21 consists of a high speed processor board featuring a 68020 CPU (20 or 25 MHz) running constantly without the insertion of wait states out of 1 Mbyte static RAM.
Floating point operations are supported via the Floating Point Co-Processor 68881 (20 MHz) increasing the throughput of the system.
A constant computing rate of 3 to 5 million instructions per second is available for the user of the Real Time Operating System PDOS*.
The multi-user multi-tasking operating system features lowest overhead for task switching in combination with an ultra fast exception/interrupt handling.
A Centronics parallel and a RS232 serial printer interface as well as a GBIP (IEEE 488) interface are installed and supported by the operating system.
The 8 serial I/O channels for connection of user terminals are controlled by a separate 68010 processor exonerating the Main Central Processing Unit from I/O handling.
Maximum data throughput to the hard disk and the floppy disk drive is provided through the Intelligent SCSI controller board featuring a 128 Kbyte data puffer for hashing and caching. A local 68010 CPU and a DMA controller offer a data throughput of 1.5 Mbyte per second to the installed 170 Mbyte hard disk.
The PDOS* System 21 offers 12 double-height VMEbus slots where 6 slots are used and 6 slots are left open for application dependent extensions.

Photo of the PDOS* System 21



1. Features of the PDOS* System 21

1.1 Main Processor
- 20MHz 68020 (PDOS* System 21A) or 25 MHz 68020 (PDOS* System 21B)
- 8 EPROM sockets providing a maximum capacity of 512 Kbyte
- Full 32 bit address and data path for all memory accesses (SRAM, EPROM and global RAM)

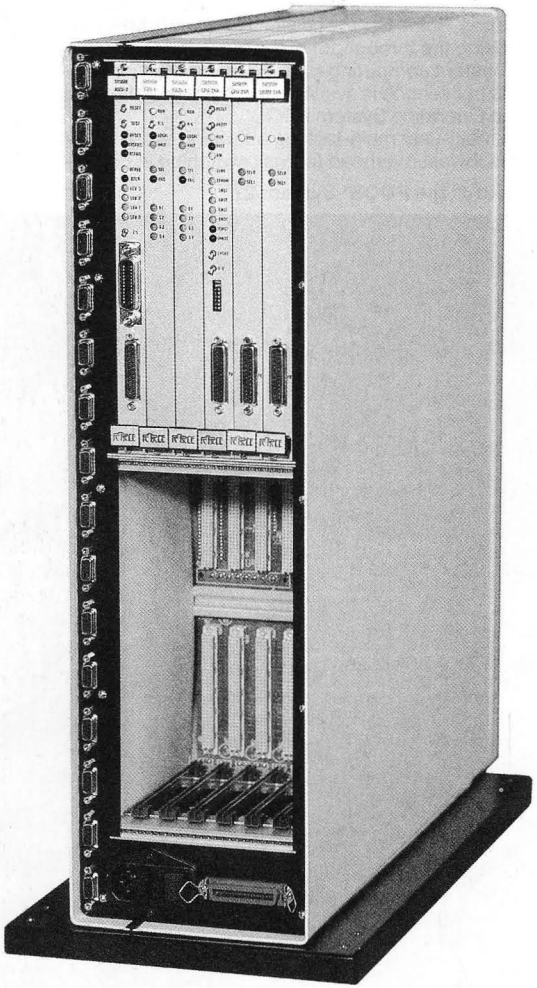
1.2 Floating Point Arithmetic
- Full IEEE P754 draft 10.0 compatible Floating Point Co-Processor installed (FPCP 68881 with 20 MHz)

1.3 Main Memory
- 1 Mbyte of high reliable static RAM
- Zero Wait State operation for all read and write transfers of the CPU (20 and 25 MHz) to the static RAM

1.4 Mass Storage Controller
- Intelligent controller built with a 68010 CPU and a 68450 DMA controller
- Full SCSI compatible interface providing data transfer rates of up to 1.5 Mbyte/s
- Floppy disk interface (SA460 compatible)
- Enhanced firmware supporting data hashing and caching within the 128 Kbyte Dual Ported static RAM

1.5 Mass Storage Media
- 170 Mbyte SCSI compatible Winchester disk providing a data transfer rate of 1.5 Mbyte/s. Average access time of less than 23 ms
- 1Mbyte floppy disk drive with SA460 compatible interface

1.6 Serial I/O Interfaces
- 8 RS232 interfaces controlled via an intelligent controller board (local 68010). Full duplex data transfers on all 8 channels at up to 19200 baud. 128 Kbyte Dual Ported Buffer storage area built with SRAMs.
- 1 RS232 interface acting as the Master Console under direct control of the main CPU.
- 1 RS232/422 interface under direct control of the main CPU for high speed data transfers.
- All serial I/O ports feature software programmable baud rate and protocol selection (SDLC, HDLC, X.25, Asynchronous, Synchronous).



1.7 Dedicated I/O Interfaces

- 1 serial printer interface (RS232 compatible) with software selectable baud rate.
- 1 Centronics printer interface (parallel).
- 1 GPIB/IEEE488 interface with talker/listener and controller function.
- 1 RS232/422 link to other computers for up/down-loading of data/programs.

1.8 System Control Functions

- 4 level bus arbiter
  - Round Robin mode
  - Prioritized mode
  - Prioritized Round Robin mode
- Software programmable real-time clock with on-board battery backup.
- Watchdog timers for
  - Arbitration
  - Interrupt Acknowledge cycles
  - Standard Read/Write cycles
- Power monitor and handling of SYSRESET and ACFAIL.
- Software controlled shutdown of the system.
- Front panel switches for system RESET and ABORT.
- Front panel indicators for
  POWER ON
  VME ACCESS
  USER MODE
  MASS STORAGE ACCESS
  SYSFAIL
- Key switch for main power, removable in ON and OFF position.

1.9 VMEbus Functions

- 32 address signals
- 32 data signals
- 7 interrupt Request signals
- 4 Level Bus Arbitration
- 40 Mbyte/s maximum data transfer rate
- 16 Layer motherboard

1.10 System Environment

- 460W power supply
- 110/220V Input Voltage
- 2 independent cooling fans
- 6 VMEbus boards installed
- 6 VMEbus slots for extensions
- Dimensions Height 170mm
  Depth 540mm
  Breadth 600mm

2. PDOS* Operating System Overview

The SYS68K/PDOS* is a powerful multi-user, multi-tasking, Real Time Operating System (RTOS). PDOS* consists of a small real time kernel (6 Kbyte) which provides synchronization and control of events occuring from the hardware using semaphores, events, messages, mailboxes and suspension primitives.
The file management module supports named file access with sequential, random and shared accesses. The details of the PDOS* functions are listed below:

2.1 PDOS* Kernel

PDOS* is written in assembly language for fast, efficient execution. The small kernel provides multitasking Real-Time Clock, event processing, and memory management functions. Ready tasks are scheduled using a prioritized, round-robin method. The line A execution vector is used to interface over 74 system primitives to a user task.
Multi-Tasking execution environment: Tasks are the components comprising a real-time application. Each task is an independent program that shares the processor with other tasks in the system. Tasks provide a mechanism that allows a complicated application to be subdivided into several independent, understandable, and manageable modules. Real-time, concurrent tasks are allocated in 2 Kbyte increments. The task system overhead for each task is only 1.25 Kbyte.

2.2 Intertask Communication & Synchronisation

Semaphores and events provide a low overhead facility for one task to signal another. Events can be used to indicate availability of a shared resource, timing pulses, or hardware interrupt occurrences. Messages and mailboxes are used in conjunction with system lock, unlock, suspend, and event primitives. PDOS* provides timing events that can be used in conjunction with desired events to prevent system outlocks. Other special system events signal character inputs and outputs.

2.3 Memory Requirements

PDOS* is very memory efficient. The PDOS* kernel, file manager, and user monitor utilities require only 24 Kbytes of memory plus an additional 4 Kbytes for system buffers and stacks. The hardware dependent part takes an additional 8 Kbyte of memory. Further memory reduction can be achieved by linking the user application to a 6 Kbyte PDOS* kernel for a small, ROMable, standalone, multitasking module.

2.4 File Management

The PDOS* file management module provides sequential, random, read only, and shared access to named files on a secondary storage device. These low overhead file primitives use a linked, random access file structure and a logical sector bit map for allocation of secondary storage. No file compaction is ever required. Files are time stamped with date of creation and last update. Up to 32 files can be simultaneously opened. Complete device independence is achieved through read and write logical sector primitives.

2.5 Command Line Interpreter

A resident command line interpreter allows multiple commands to be entered on a single line. Command utilities such as append, define, delete, copy, rename, and show file are also resident and can be executed without destroying current memory programs. Other functions resident in the PDOS* monitor include setting the baud rate of a port, checksumming memory, creating tasks, listing tasks, files and open file status, asking for help, setting file level, file attributes, interrupt mask, and system disk, and directing console output.

2.6 Interrupt Management

The PDOS* kernel handles user console, system clock, and other designated hardware interrupts. User consoles have interrupt driven character I/O with type ahead. A task can be suspended pending a hardware or software event. PDOS* will switch control to a task suspended on an external event within 100 microseconds after the occurrence of the event (provided the system mask is high enough). Otherwise, a prioritized round-robin scheduling of ready tasks occurs in 10 millisecond intervals.

2.7 Support Tools

Numerous support utilities including virtual screen editors, assembler, linker, macroprocessor, disk diagnostics, link, recovery and disk cataloging are additional standard functions in the PDOS*. Single stepping, multiple break points, memory snap shots, save and restore task commands, and error trapping primitives are provided for program debugging.

2.8 Language Support

The following languages are available under PDOS*:

Assembler: A macro assembler with the full 68020 and 68881 instruction set is included in the PDOS* system.

C: A complete implementation of the C-language as defined by Kenigham and Ritchie is available as an option. Extensions include most of the PDOS* primitives to support the real time features of PDOS*. The compiler supports 68020 as well as the Floating Point Co-Processor 68881.

FORTRAN77: Full 1977 ANSI Version of the FORTRAN language is available as an option. The FORTRAN compiler can generate code for the 68000/68010 or the 68020 with support of the 68881.

PASCAL: Full Jensen/Wirth implementation of the ISO PASCAL standard is available as an option.

2.9 Benchmarks of the PDOS* System 21B

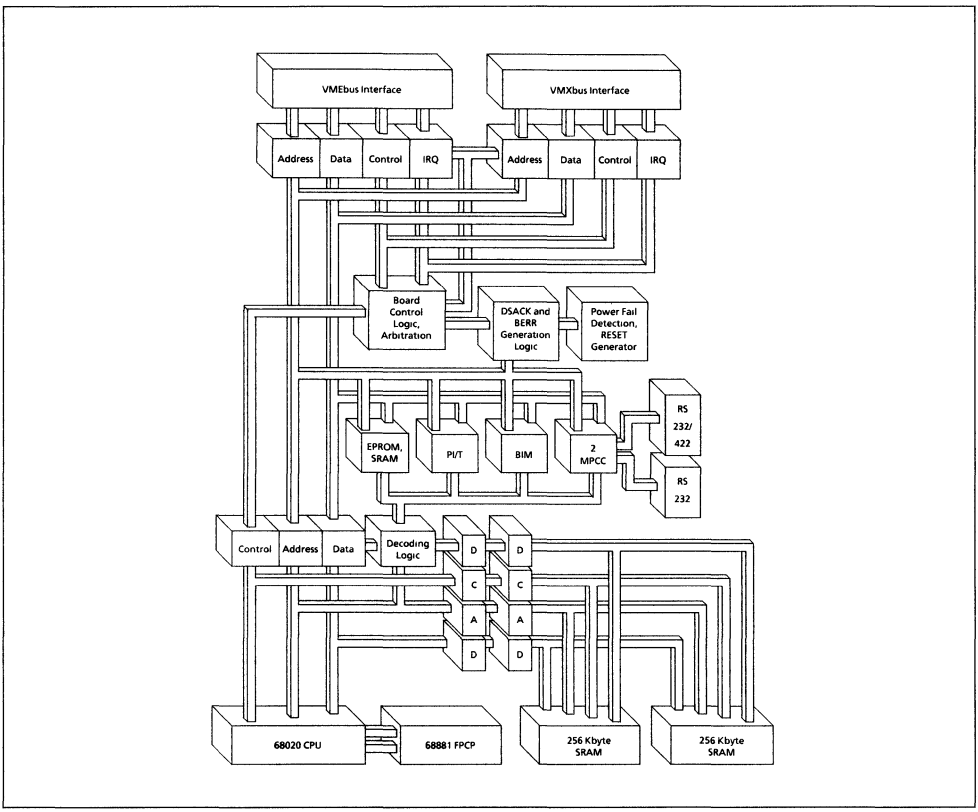
Type	Time	Type	Time
Sieve 100 iterations	2.77 s	Set system event with context switch	25.2 μs
Ackermann 100 loops	13.98 s	Change task priority	18.8 μs
Fibonacci 100 loops Floating point	6.7 s 19.18 s	Read time	13.0 μs
Context switch time	20.6 μs	Send and receive 4 bytes	35.8 μs
Set system event	12.9 μs	Send and receive 64 bytes Task Synchronization	117.0 μs 116.1 μs

3. Hardware Description

3.1 Main Processor Board

The 68020 CPU is installed as the main CPU of the PDOS* System 21. The 68020 is a full 32 bit processor offering a computing power of 2-4 MIPS (20 MHz) respectively 3-5 MIPS at 25 MHz.
A high speed static RAM (1 Mbyte) guarantees this throughput, because all bus cycles to the RAM of the 68020 are executed without the insertion of wait states. The 1 Mbyte static RAM guarantees highest reliability, data security and throughput through the 32 bit data path. 8 EPROM sockets, also with a 32 bit data path, allow the storage of application dependent programs with a maximum size of 512 Kbyte.
A Floating Point Co-Processor (FPCP 68881) supports all floating point instructions with single, standard, double and extended precision (80 bit) defined in the IEEE P754 draft 10.0. In addition, the 20 MHz Co-Processor offers 35 arithmetic, trigonometrical and logarithmic instructions.
A local timer, included in the PI/T (68230) is used as the time base of the operating system. The local interrupts coming from the 3 serial I/O interfaces and the PI/T can be routed to a free software programmable level via a special on-board hardware.
One RS232 compatible serial I/O interface built with the multiprotocol communication controller (MPCC 68561) is used as the master console for the PDOS* based system.
The second serial interface (RS232/422 compatible) is configured for communication to a host computer and/or other FORCE systems. Up- and down-load programs are installed under the operating system to ease installation and usage.
The third serial I/O interface (RS232 or RS422) can be used for high speed data communication to other machines using HDLC, SDLC or asynchronous protocols (38400 baud or synchronous data rate of up to 2 Mbit/s).
The block diagram of the SYS68K/CPU-21B shows the structure of the board.

BLOCK DIAGRAM OF THE SYS68K/CPU-21B



3.2 Mass Storage Devices

The PDOS* System 21 contains an intelligent mass memory controller board, the SYS68K/ISCSI-1. It is built around the 16/32 bit 68010 CPU and the 68450 four channel DMA controller. Both, the DMA controller and the CPU access the 128 Kbyte Dual Ported static RAM without the insertion of wait states, which guarantee maximum performance. The CPU executes the firmware housed in two EPROMs constantly without the insertion of wait states and provides hashing and caching of data.
The SCSI bus controller (NCR 5386) and the bus driver/receiver chip (NCR 8310) provide a constant data transfer rate of 1.5 Mbyte/s together with the DMA controller.
A 5 1/4" Winchester disk with an unformatted capacity of 170 Mbyte is installed inside the system. The data transfer rate of 1.5 Mbyte per second of the Winchester and the controller board offers together with the average access time of 23 ms, maximum system performance.
The Floppy Disk Controller (WD1772) installed on the ISCSI-1 board controls the 5 1/4" floppy disk drive (half height) available on the front side of the system.
The on-board handling firmware allows copying of data from the floppy disk to the Winchester disk or to the optionally available streamer without interfering the activities of the main CPU.

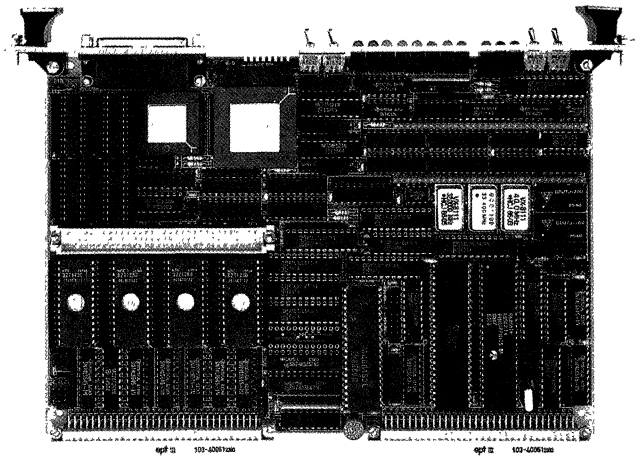
3.3 The Serial I/O Controller

To reduce the overhead of the main CPU handling the terminals or other RS232 devices, an intelligent serial I/O controller board, the SYS68K/ISIO-1 is installed in the PDOS* System 21.

The board is built around the 68010 CPU, running constantly without any wait states out of the EPROM (128 Kbyte capacity) and out of the Dual Buffered Dual Ported RAM. This allows to run on all 8 serial I/O channels, full duplex at a baud rate of 19200 baud without loosing any data. Hardware or software handshake, various synchronous and asynchronous protocols as well as the baud rate of each channel are software programmable.
The 128 Kbyte Dual Ported static RAM allows to store the line buffers on the board for each channel which reduces the overhead of the VMEbus activities.
Single character, a line editor, block moves and data conversions are available as standard commands within the firmware of the ISIO-1 board.
The eight RS232 compatible I/O channels are available on the rear side of the system via 9 pin D-sub connectors.
The following table lists all the supported signals per channel:

PIN	Input	Output	Signal	Description
1	x		DCD	Data Carrier Detect
2	x		RXD	Receiver Data
3		x	TXD	Transmit Data
4		x	DTR	Data Terminal Ready
5	x	x	GND	Signal GND
6	x	x	DSR	Data Set Ready
7		x	RTS	Request to Send
8	x		CTS	Clear to Send
9	–	–	–	Not Connected

PHOTO OF THE SYS658K/CPU-21B



3.4 The System Control Functions

All system control functions as well as dedicated interfaces are installed on the SYS68K/ASCU-2 at slot 1 of the PDOS* System 21.
A serial and a parallel printer interface are installed to support Centronics as well as RS232 compatible printers.
The IEEE488 interface allows controlling of industrial measurement machines. The Talker, Listener as well as the Controller mode are supported via the included software driver and the used 7210 chip.
Time and date are stored within the on-board Real Time Clock (58167). The battery guarantees correct operation for more than two years.
A 4 level bus arbiter provide efficient bus arbitration for the main CPU and optional VMEbus boards. To avoid system failures, a watchdog timer for bus arbitration, interrupt acknowledge and standard access cycles are installed on the board.

3.5 System Environment

All VMEbus boards are connected via a specially designed motherboard providing interconnection to the power supply, the mass memory storage devices and the front panel switches/indicators.
The 16 layer motherboard uses special shielding mechanism to reduce cross talking and to reduce the noise level of each signal trace. The J1 and J2 functions of the VMEbus motherboard are combined in the single backplane providing optimised power distribution through 4 separate power layers. The interconnection between the VMEbus based controller boards and the I/O interfaces as well as the mass memory drives is made via indirect connectors. The supply voltage of the mass memory drives is also made on the motherboard to guarantee lowest noise levels on the supply voltage.
A total of 16 serial I/O channels with 9 pin D-sub connectors are available on the rear side of the system where 8 of them are supported through the installed ISIO-1 board and 8 of them are preconfigured to be used in conjunction with an optional ISIO-1 board (to be installed at slot 12).
A 25 pin D-sub connector for the serial printer and the Centronics connector for a parallel printer are also available on the rear side of the system.
Control of the system is provided on the front side using the key switch for the main power and the RESET as well as the TEST switch. Visual control is provided through the 5 indicators which are also available on the front side of the system.
Two independent metal enclosures assure mechanical stability as well as lowest scattered radiation. There are two independent fans, one for the VMEbus boards and one for the mass memory storage devices as well as for the power supply assuring proper cooling. A temperature sensor is installed between the VMEbus boards to switch off the DC power if the temperature is higher than 60 degrees C to avoid damage of the components.
The power supply installed in the system provides a supply current of 64A at +5V, 10A at +12V and 2A at -12V. The main voltage is 110V or 220V with a range of $\pm 10\%$.
The PDOS* System 21 consists of 12 slots where 6 are left open for application dependent extensions.

4. Extensions

The PDOS* System 21 can be upgraded by adding application dependent modules such as a graphic board set and a graphic software package (GKS) or a streamer providing a fast system backup. Global memory using dynamic or static RAMs, additional I/O interfaces or network controllers can also be installed using the VMEbus for interfacing.

4.1 Streamer

A 120 Mbyte SCSIbus compatible streamer can be installed on the front side of the system without the need for an additional controller board. The handling software for the streamer is installed on each system. The system is preconfigured with the mounting equipment and cable assembly for easy installation and usage of the streamer.

4.2 Graphics

High resolution graphics are supported via the graphics option which includes the SYS68K/AGC-1 board and the GKS package. The SYS68K/AGC-1 board set supporting display formats of up to 1600 x 1280 pixels (64 MHz pixel frequency). 16 different colours can be selected out of a palette of 16 million colours using this resolution.
The Advanced CRT Controller 63484 using the dual access mode to the 2 Mbyte video memory provides a maximum drawing speed of 2M pixel/s. Using 256 different colours out of 16 million, the maximum display format of the AGC-1 board set is 1024 x 800 (32 MHz pixel frequency).
The GKS level 2b running under PDOS* conforms to the DIN 66252 and the ISO 7942 standard. The GKS package can be interfaced from the FORTRAN 77 as well as from the C programming language. Device drivers for colour printers, a mouse, digitizer and keyboard are included in source code form to adapt the software to the application dependent needs.

4.3 Memory Extension

Dynamic memory can be added using the DRAM-E3M1 or DRAM-E4M4 boards providing 1 Mbyte, respectively 4 Mbyte of global memory. The access time on read/write cycles is 245/65 ns.
Static memory with battery backup of up to 1 year can be added by using the SRAM-4, 4A or 4B boards. The memory capacity is 256 K, 512 K or 1 Mbyte at a read/write access time of 210/80 ns.

All memory boards have a full 32 bit data and address path conforming to the VMEbus specification. Read Modify Write as well as aligned and unaligned transfers are supported.

4.4 Tower Extension

Mounting equipment for the FOCUS series of products and an additional module allows the usage of the system as a "Tower" as shown in the data sheet.

PHOTO OF THE DESK TOP VERSION

Specifications

Main CPU of PDOS* System 21A Main CPU of PDOS* System 21B	68020 68020	20MHz 25MHz
Floating Point Co-Processor	68881	20MHz
Main Memory	SRAM	1Mbyte
No of Wait States	0	Constantly
EPROM	8 sockets/32 bit	512Kbyte
Serial I/O Interfaces Master Console Host Computer High speed Data Link Terminal Interfaces via ISIO-1 9 pin D-sub connectors	 1 1 1 8 16	 RS232 RS232/422 RS232/422 RS232 Pre-Configured
Mass Memory		
Winchester Capacity Transfer Speed Average Access Time	170Mbyte 130Mbyte 1.5Mbyte/s 23ms	unformatted formatted 5ms Track-to-Track
Floppy Disk	1Mbyte	unformatted
Intelligent Controller board Interfaces	SCSIbus	SA460
Real Time Clock with battery backup	58167	
Printer Interface	RS232 Centronics	Serial Parallel
GPIB Interface	IEEE 488	
Bus System Total No. of slots Used VMEbus Boards No of free slots	VMEbus 12 ASCU-2 ISIO-1 ISCSI-1 6	A32:D32 6+6 CPU-21A/B CPU-21A/B SRAM-22A/B
Power Requirements	110 220	6.5 A (avg) 3.2 A (avg)
Spurious Radiation conforms to	VDE 0871/Class B	
Security Level conforms to	VDE 0806/IEC 380	
DC Power Specification	+5V +12V −12V	64A (max.) 10A (max.) 2A (max.)
Surge Current	12A at 220V 22A at 110V	
Main Voltage	100 – 120V 200 – 240V	690W 192 KJ/h
Enclosure Dimensions	Height 170 mm Depth 540 mm Breadth 600 mm	6.7 inch 21.3 inch 23.7 inch
Weight	40kg	88lbs
Operating Temperature	5–45 degrees C	
Storage Temperature	5–95 degrees C	non-operation
Relative Humidity	10–70%	non-condensing

Ordering Information

PDOS* System 21A Part No. 640021	FORCE FOCUS 32 with 20 MHz 68020 CPU Board and PDOS*
PDOS* System 21B Part No. 640022	FORCE FOCUS 32 with 25 MHz 68020 CPU Board and PDOS*
PDOS* System 21/UM Part No. 800118	User Manual of the PDOS* System 21

Hardware Extensions

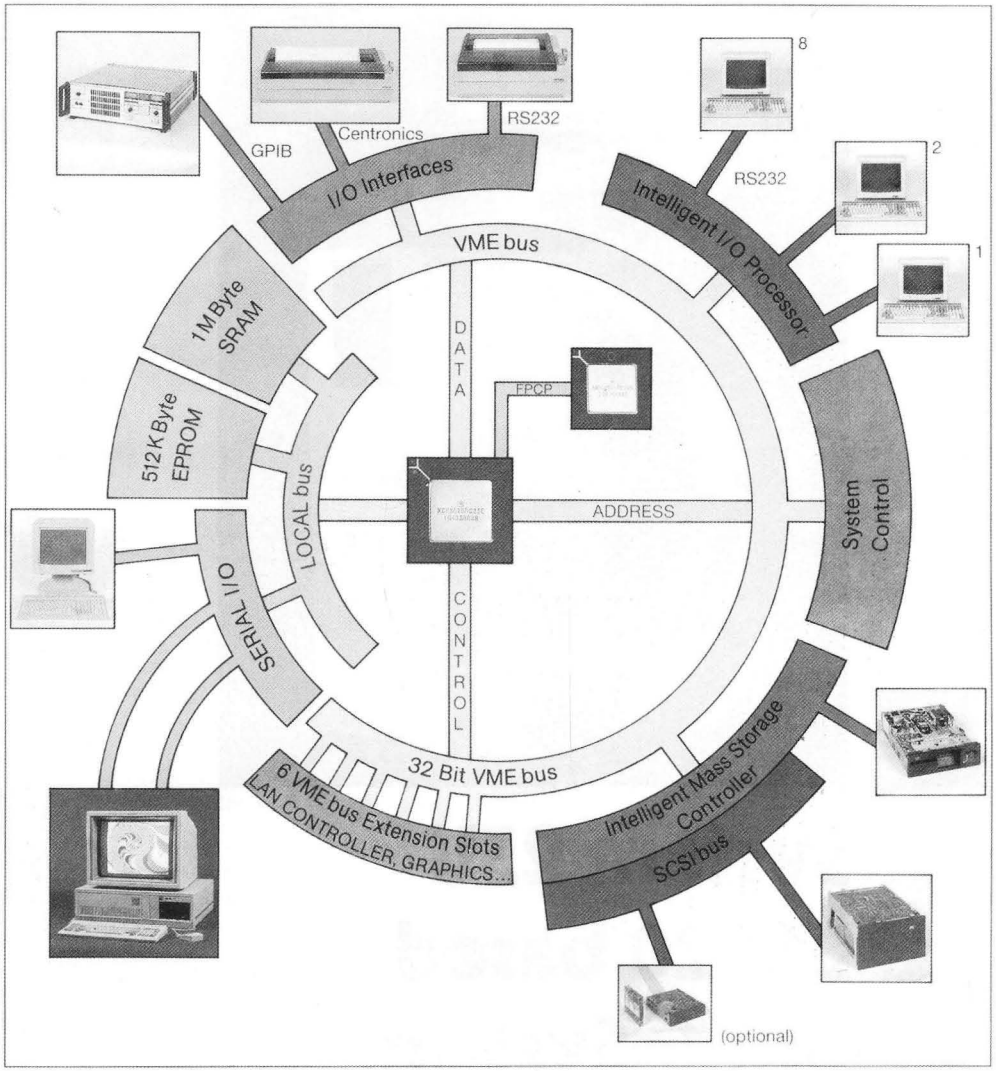
SYS68K/STR-120 Part No. 700040	120 Mbyte SCSIbus compatible streamer
SYS68K/AGC-1 Part No. 400020	High Resolution Graphics Board Set (2 slots)
SYS68K/ISIO-1 Part No. 310030	Additional 8 channel serial I/O controller board to be installed at slot 12
SYS68K/DRAM-E3M1 Part No. 200004	1 Mbyte dynamic RAM board with byte parity check
SYS68K/DRAM-E4M4 Part No. 200110	4 Mbyte dynamic RAM board with byte parity
SYS68K/SRAM-4B Part No. 200502	1 Mbyte static RAM board including battery backup
SYS68K/CABLE-9/25 Part No. 700031	8 cable adaptors from 9 pin D-sub connector to 25 pin D-sub connector
FOCUS 32 TOWER Part No. 700041	Mounting equipment for usage of the FOCUS systems as a tower

Software Extensions

SYS68K/PDOS*-C020 Part No. 140031	C Compiler for PDOS*
SYS68K/PDOS*-FOR020 Part No. 140041	FORTRAN-77 Compiler for PDOS*
SYS68K/PDOS*-PAS020 Part No. 140021	PASCAL Compiler for PDOS*
SYS68K/GKSGRAL-P2B1 Part No. 160000	GKS level 2b for FORTRAN 77 and C under PDOS*

System 25U 68020 based UNIX* System

- Fully configured 32 bit Unix
- 175 Mbyte Winchester, 120 Mbyte Streamer
- 5 free expansion slots



UNIX* is a trademark of Bell Laboratories

General Description

The FOCUS 32 series of products are full 32 bit target and development systems based on the VMEbus.
All the serial I/O communication channels to the terminals or host computers, as well as the mass memory device interfaces, are controlled via intelligent controller boards.
The System 25U consists of a high speed processor board which features a 68020 CPU (16.7 or 20.0 MHz) that runs constantly with one wait state out of 1 Mbyte local static RAM.
Floating point operations are supported via the Floating Point Coprocessor 68881 (16.7 or 20.0 MHz) increasing the throughput of the system.
A constant computing rate of 1.5 to 3 million instructions per second is available for the user of the UNIX* operating system.
The implemented Paged Memory Management Unit (PMMU 68851) provides logical-to-physical address translation to monitor and enforce the protection/privilege mechanism, and to support the breakpoint operations.
A Centronics parallel printer, an RS232 serial printer interface and a GBIP (IEEE 488) interface are installed and supported by the operating system.
The 8 serial I/O channels for connection of user terminals are controlled by a separate 68010 processor exonerating the main Central Processing Unit from I/O handling.
Maximum data throughput to the hard disk and the floppy disk drive is provided through the Intelligent SCSI controller board featuring a 128 Kbyte data buffer for hashing and caching. A local 68010 CPU and a DMA controller offer a data throughput of 1.5 Mbyte per second to the installed 170 Mbyte hard disk.
The System 25U offers 12 double-height VMEbus slots. Seven of these slots are used, while five slots are left open for application dependent extensions.

PHOTO OF THE SYSTEM 25U

1. Features of the UNIX* System 25

1.1 Main Processor

- 16.7 or 20.0 MHz 68020
- Full 32 bit address and data path for all memory accesses (SRAM and global RAM).

1.2 Memory Management

- 68851 PMMU for fast logical to physical address translation (causing one wait state at local SRAM access).

1.3 Floating Point Arithmetic

- Full IEEE P754 draft 10.0 compatible Floating Point Coprocessor installed (FPCP 68881 with 16.7 or 20.0 MHz).

1.4 Main Memory

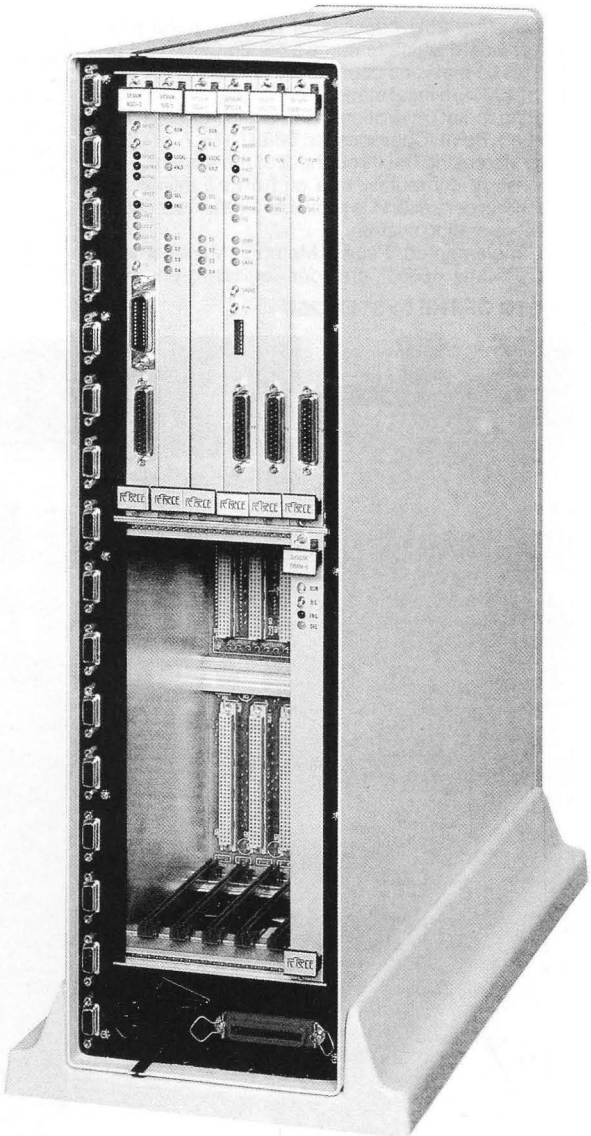
- 1 Mbyte of high reliable static RAM operating constantly with one wait state for all read and write transfers of the CPU at 16.7 or 20.0 MHz because of the PMMU.
- 4 Mbyte of DRAM including byte parity check (VMEbus).

1.5 Mass Storage Controller

- Intelligent controller built with a 68010 CPU and a 68450 DMA controller.
- Full SCSI compatible interface providing data transfer rates of up to 1.5 Mbyte/s.
- Floppy disk interface (SA460 compatible).
- Enhanced firmware supporting data hashing and caching within the 128 Kbyte dual ported static RAM.

1.6 Mass Storage Media

- 170 Mbyte SCSI compatible Winchester disk providing a data transfer rate of 1.25 Mbyte/s. Average access time of less than 23 ms.
- 1 Mbyte floppy disk drive with SA460 compatible interface.
- 120 Mbyte 5 1/4 inch cartridge tape drive with SCSI compatible interface.



1.7 Serial I/O Interfaces

- 8 RS232 interfaces controlled via an intelligent controller board (local 68010). Full duplex data transfers on all 8 channels at up to 19200 baud. 128 Kbyte dual ported buffer storage area built with SRAMs.
- 1 RS232 interface acting as the master console under direct control of the main CPU.
- All serial I/O ports feature software programmable baud rate and protocol selection (SDLC, HDLC, X.25, asynchronous, synchronous).

1.8 Dedicated I/O Interfaces

- 1 serial printer interface (RS232 compatible) with software selectable baud rate.
- 1 Centronics printer interface (parallel).
- 1 GPIB/IEEE488 interface with talker/listener and controller function.
- 2 RS232/422 links to other computers for up/down-loading of data/programs.

1.9 System Control Functions

- 4 Level Bus Arbiter
  - Round Robin mode
  - Prioritized mode
  - Prioritized Round Robin mode
- Software programmable real-time clock with on-board battery backup.
- Watchdog timers for
  - Arbitration
  - Interrupt Acknowledge cycles
  - Standard Read/Write cycles
- Power monitor and handling of SYSRESET and ACFAIL.
- Software controlled shutdown of the system.
- Front panel switches for system RESET and ABORT.
- Front panel indicators for POWER ON
  VME ACCESS
  USER MODE
  MASS STORAGE ACCESS
  SYSFAIL
- Key switch for main power, removable in ON and OFF position.

1.10 VMEbus Functions

- 32 address signals
- 32 data signals
- 7 Interrupt Request signals
- 4 Level Bus Arbitration
- 40 Mbyte/s maximum data transfer rate
- 16 layer motherboard

1.11 System Environment

- 460W power supply
- 110/220V input voltage
- 2 independent cooling fans
- 7 VMEbus boards installed
- 5 VMEbus slots for extensions
- Dimensions
  - Height 170 mm
  - Length 540 mm
  - Width 600 mm

2.0 UNIX* Operating System Overview

The UNIX* System V Release 3(2), which is implemented in the FOCUS 32 series, is a multi-user, timesharing, multi-tasking operating system. The UNIX* operating system software includes:

- the UNIX* operating system kernel
- the "shell" command interpreter
- a file system
- various user and system commands

The UNIX* operating system oversees the execution of many user programs or commands. These programs seem to execute simultaneously because of the systems' ability to time-share the processor among all the programs.
Actually, each program is scheduled to use the processor for a short period of time until the execution of all other programs.
Therefore, in addition to providing a multi-user system, the UNIX* operating system provides the capability for each user to run several programs at once (multi-tasking).

2.1 The UNIX* Kernel

The kernel, comprising from 5 to 10 percent of the operating system software, is the basic resident software on which the entire system relies. It is the only permanently resident part of the system. The kernel controls user processes and manages system resources.

2.2 The Command Interpreter (shell)

The shell command interpreter allows the user to communicate with the UNIX* operating system. The shell, besides providing the user interface to the kernel and interpreting operating system commands, can also be used as a programming language.
The user can quickly write custom shell procedures to perform very simple to very complex tasks. The shell allows users to enhance and build upon UNIX* system capabilities and adapt the operating system to a wide variety of user applications.

2.3 The File System

The file system of the UNIX* operating system consists of a set of directories and files which are arranged in a tree-like structure.
The file system is built up from the root directory. Although the operating system does not require the file system to be structured in any particular way, the root directory normally contains certain standard subdirectories. The function they perform is necessary for the operation of the system. Additional subdirectories may be generated for several user needs.

2.4 Support Tools

Additional functions in the system are tools which support the handling of the operating system, the development of programs and the installation of FORCE VMEbus application boards.
The following tools are included in the standard configuration:

- A driver for the high resolution colour controller SYS68K/AGC-1 board. The source code of the driver named "agc.c" is included in the system.
- The driver for the RAM-ROM SYS68K/RR-2 board and an EPROM programming utility is included in the system.
- The visual editor "vi".
- The assembler.
- The C-shell (csh) which is a command interpreter and which can run as an alternative to the bourne shell. This is a tool for those people who are familiar with the "csh".
- The "VMEPROM-LINK" is a software package which allows the user to develop programs under UNIX* and to transfer these programs to a real-time environment which runs under VMEPROM control.
  VMEPROM is the ROM resident, PDOS compatible, Real-Time Kernel, plus file manager to support multi-tasking.

2.5 Programming Languages

Besides the inherent programming capability of the shell, the operating system supports many programming languages in common use such as C, Fortran 77, Assembler and Snobol. These are included in the system without extra cost.
Other Compilers (e.g. Pascal, Cobol...) are available as options on the System 25U.

2.6 Benchmarks of the System 25U

BENCHMARK TYPE	REAL (sec)	TIME USER (sec)	SYS (sec)
Shell – fork a child shell and execute sort	0.9	0.0	0.4
Multitasking with 6 processes – fork 6 child shells and execute sort	5.5	0.5	2.0
Disk write – write 1000 blocks to filesystem	8.6	0.0	1.0
Disk read – read 1000 blocks to filesystem	1.3	0.0	0.8
Function call – 50,000 dummy function calls	0.1	0.0	0.0
Function call – 50,000 assign variables	0.2	0.2	0.0
Fibonacci – 10 iterations	5.2	5.2	0.0
Float – 70,000 multiply and 70,000 divide	1.2	1.2	0.0
iofile – 500 random read and write	1.0	0.0	0.9
loop – count of 1000000	1.4	1.4	0.0
pipes – 1024, 512 byte blocks	1.4	0.0	0.7
system calls – 25,000 get pid ( )	2.9	0.1	2.8
sieve from Eratosthenes – 10 iterations	0.6	0.6	0.0
Bytesort – sort 1000 byte buffer 10 times	5.5	5.4	0.1
iocall – 1000 writes to disk file	2.7	0.0	2.6
dhrystone with register	3476/S		
dhrystone with no register	3363/S		

3. Hardware Description

3.1 Main Processor Board

The 68020 CPU is installed as the main CPU of the System 25U. The 68020 is a full 32 bit processor which offers a computing power of 1.5-3 MIPs at 16.7 MHz. As many as 4 MIPs are provided on the 20 MHz version.
A high speed static RAM (1 Mbyte) guarantees this throughput, because all bus cycles to the RAM of the 68020 are executed with the insertion of only one wait state. The 1 Mbyte static RAM guarantees highest reliability, data security and throughput through the 32 bit data path. 1 EPROM socket allows the storage of application dependent programs with a maximum size of 64 Kbyte.
A Floating Point Coprocessor (FPCP 68881) supports all floating point instructions with single, standard, double and extended precision (80 bit) as defined in the IEEE P754 draft 10.0. In addition, the 16.7 MHz Coprocessor offers 35 arithmetic, trigonometrical and logarithmic instructions.
The Paged Memory Management Unit (PMMU 68851) offers logical to physical address translation in less than 60 ns.
A local timer, included in the PI/T (68230), is used as the time base of the operating system. The local interrupts coming from the 3 serial I/O interfaces and the PI/T can be routed to a free software programmable level via a special on-board hardware.
One RS232 compatible serial I/O interface, built with the Multi Protocol Communication Controller (MPCC 68561), is used as the master console for the UNIX* based system.
The second and third serial I/O interface (RS232 or RS422) can be used for high speed data communication to other machines using HDLC, SDLC or asynchronous protocols (38400 baud or synchronous data rate of up to 2 Mbit/s).
The block diagram of the SYS68K/CPU-25 shows the structure of the board.

BLOCK DIAGRAM OF THE SYS68K/CPU-25

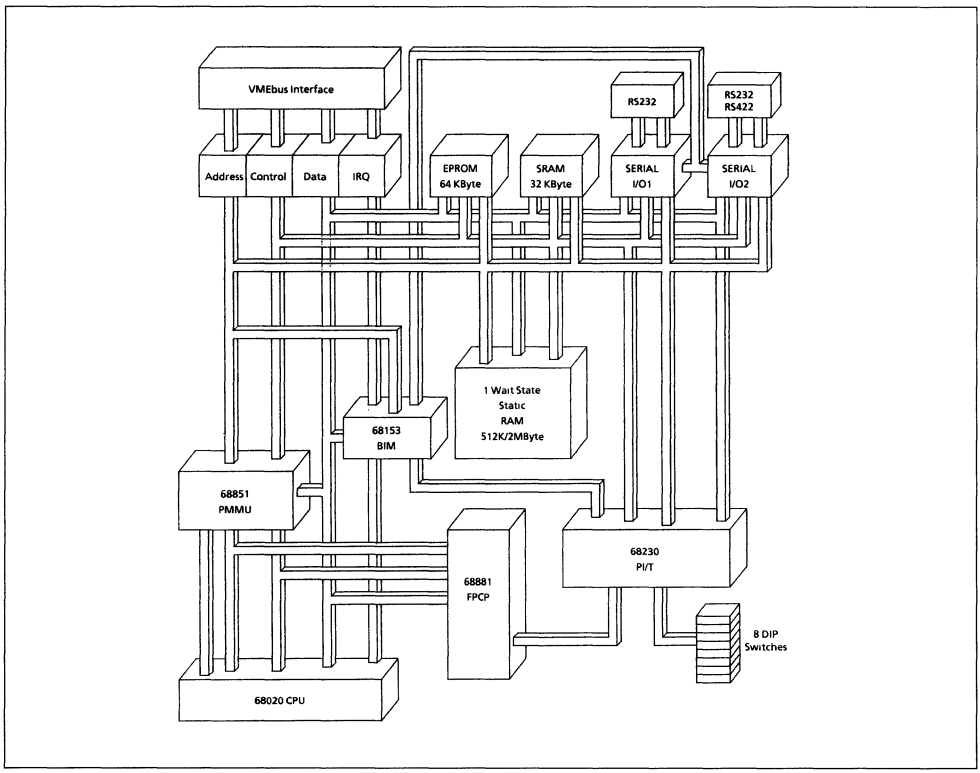
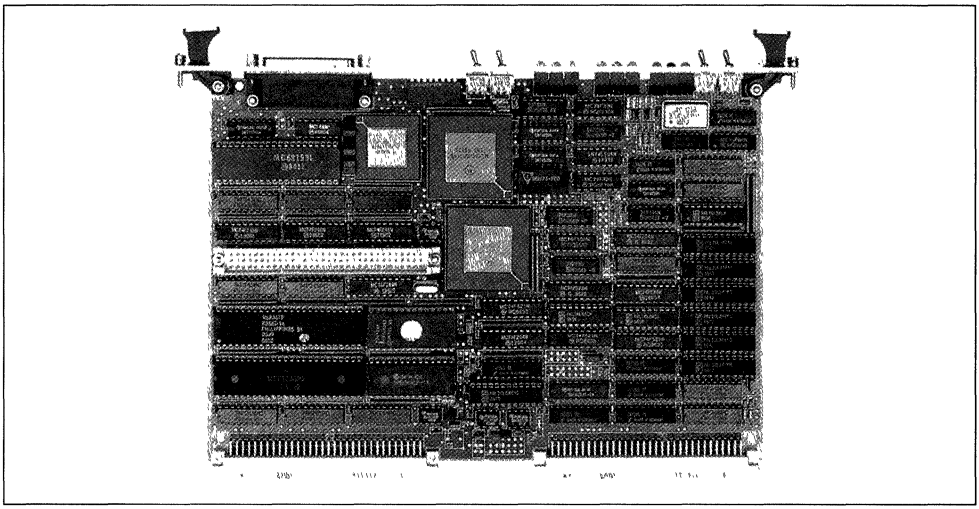


PHOTO OF THE SYS68K/CPU-25



3.2 Mass Storage Devices

The System 25U contains an intelligent mass memory controller board, the SYS68K/ISCSI-1. It is built around the 16/32 bit 68010 CPU and the 68450 four channel DMA controller. Both the DMA controller, and the CPU, access the 128 Kbyte Dual Ported static RAM without the insertion of wait states, which guarantees maximum performance. The CPU executes the firmware housed in two EPROMs constantly without the insertion of wait states and provides hashing and caching of data.
The SCSI bus controller (NCR 5386) and the bus driver/receiver chip (NCR 8310) provide a constant data transfer rate of 1.5 Mbyte/s together with the DMA controller.
A 5 1/4 inch Winchester disk with an unformatted capacity of 170 Mbyte is installed inside the system. The data transfer rate of 1.5 Mbyte per second of the Winchester and the controller board offers, together with the average access time of 23 ms, maximum system performance.
A 5 1/4 inch cartridge tape drive with a capacity of 120 Mbyte is installed in the system available on the front side. The data transfer rate of 1.25 Mbyte per second offers a maximum back-up and restore performance.
The Floppy Disk Controller (WD1772) installed on the ISCSI-1 board controls the 5 1/4 inch floppy disk drive (half height) available on the front side of the system.
The on-board handling firmware allows copying of data from the floppy disk to the Winchester disk or to the streamer without interfering with the activities of the main CPU.

3.3 The Serial I/O Controller

To reduce the overhead of the main CPU handling the terminals or other RS232 devices, an intelligent serial I/O controller board, the SYS68K/ISIO-1, is installed in the System 25U.
The board is built around the 68010 CPU, running constantly without any wait states out of the EPROM (128 Kbyte capacity) and out of the Dual Buffered Dual Ported RAM. This allows the board to run on all 8 serial I/O channels, full duplex, at a baud rate of 19200 baud, without loosing any data. Hardware or software handshake, various synchronous and asynchronous protocols as well as the baud rate of each channel are software programmable.
The 128 Kbyte Dual Ported static RAM allows the board to store the line buffers on the board for each channel. This reduces the overhead of the VMEbus activities.
Single character, a line editor, block moves and data conversions are available as standard commands within the firmware of the ISIO-1 board.
The eight RS232 compatible I/O channels are available on the rear side of the system via 9 pin D-sub connectors.
The following table lists all the supported signals per channel:

PIN	Input	Output	Signal	Description
1	x		DCD	Data Carrier Detect
2	x		RXD	Receiver Data
3		x	TXD	Transmit Data
4		x	DTR	Data Terminal Ready
5	x	x	GND	Signal GND
6	x	x	DSR	Data Set Ready
7		x	RTS	Request to Send
8	x		CTS	Clear to Send
9	–	–	–	Not Connected

3.4 The System Control Functions

All system control functions as well as dedicated interfaces are installed on the SYS68K/ASCU-2 at slot 1 of the System 25U.
A serial and a parallel printer interface are installed to support Centronics as well as RS232 compatible printers.
The IEEE488 interface allows controlling of industrial measurement machines. The Talker, Listener as well as the Controller mode are supported via the included software driver and the used 7210 chip.
Time and date are stored within the on-board Real-Time Clock (58167). The battery guarantees correct operation for more than two years.
A 4 level bus arbiter provides efficient bus arbitration for the main CPU and optional VMEbus boards. To avoid system failures, a watchdog timer for bus arbitration, interrupt acknowledge and standard access cycles are installed on the board.

3.5 System Environment

All VMEbus boards are connected via a specially designed motherboard which provides interconnection to the power supply, the mass memory storage devices and the front panel switches/indicators.
The 16 layer motherboard uses a special shielding mechanism to reduce cross talking and to reduce the noise level of each signal trace. The J1 and J2 functions of the VMEbus motherboard are combined in the single backplane which provides optimized power distribution through 4 separate power layers.
The interconnection between the VMEbus based controller boards and the I/O interfaces as well as the mass memory drives is made via indirect connectors. The supply voltage of the mass memory drives is also made on the motherboard in order to guarantee lowest noise levels on the supply voltage.
A total of 16 serial I/O channels with 9 pin D-sub connectors are available on the rear side of the system where 8 of them are supported through the installed ISIO-1 board and the other 8 are preconfigured to be used in conjunction with an optional ISIO-1 board (to be installed at slot 12).
A 25 pin D-sub connector for the serial printer and the Centronics connector for a parallel printer are also available on the rear side of the system.
Control of the system is provided on the front side and includes the key switch for the main power, the RESET and the TEST switch. Visual control is provided through the 5 indicators which are also available on the front side of the system.
Two independent metal enclosures assure mechanical stability as well as lowest scattered radiation. There are two independent fans: one for the VMEbus boards, and one for the mass memory storage devices as well as for the power supply to assure proper cooling. A temperature sensor is installed between the VMEbus boards which switches off the DC power if the temperature is higher than 60 degrees C and thus avoids damage to the components.
The power supply installed in the system provides a supply current of 64A at +5V, 10A at +12V and 2A at −12V. The main voltage is 110V or 220V with a range of +10%.
The System 25U consists of 12 slots with 5 left open for application dependent extensions.

4. Extensions

The System 25U can be upgraded by adding application dependent modules such as a graphic board set and a graphic software package (GKS). Global memory using dynamic or static RAMs, additional I/O interfaces or network controllers can also be installed using the VMEbus for interfacing.

4.1 Graphics Extension

High resolution graphics are supported via the graphics option which includes the SYS68K/AGC-1 board and the GKS package. The SYS68K/AGC-1 board set supports display formats of up to 1600 x 1280 pixels (64 MHz pixel frequency). 16 different colours can be selected out of a palette of 16 million colours using this resolution.
The Advanced CRT Controller 63484, using the dual access mode to the 2 Mbyte video memory, provides a maximum drawing speed of 2M pixel/s. Using 256 different colours out of 16 million, the maximum display format of the AGC-1 board set is 1024 x 800 (32 MHz pixel frequency).
The GKS level 2b running under UNIX* conforms to the DIN 66252 and the ISO 7942 standard. The GKS package can be interfaced from the FORTRAN 77 as well as from the C programming language. Device drivers for colour printers, a mouse, digitizer and keyboard are included in source code form to adapt the software to the application dependent needs.

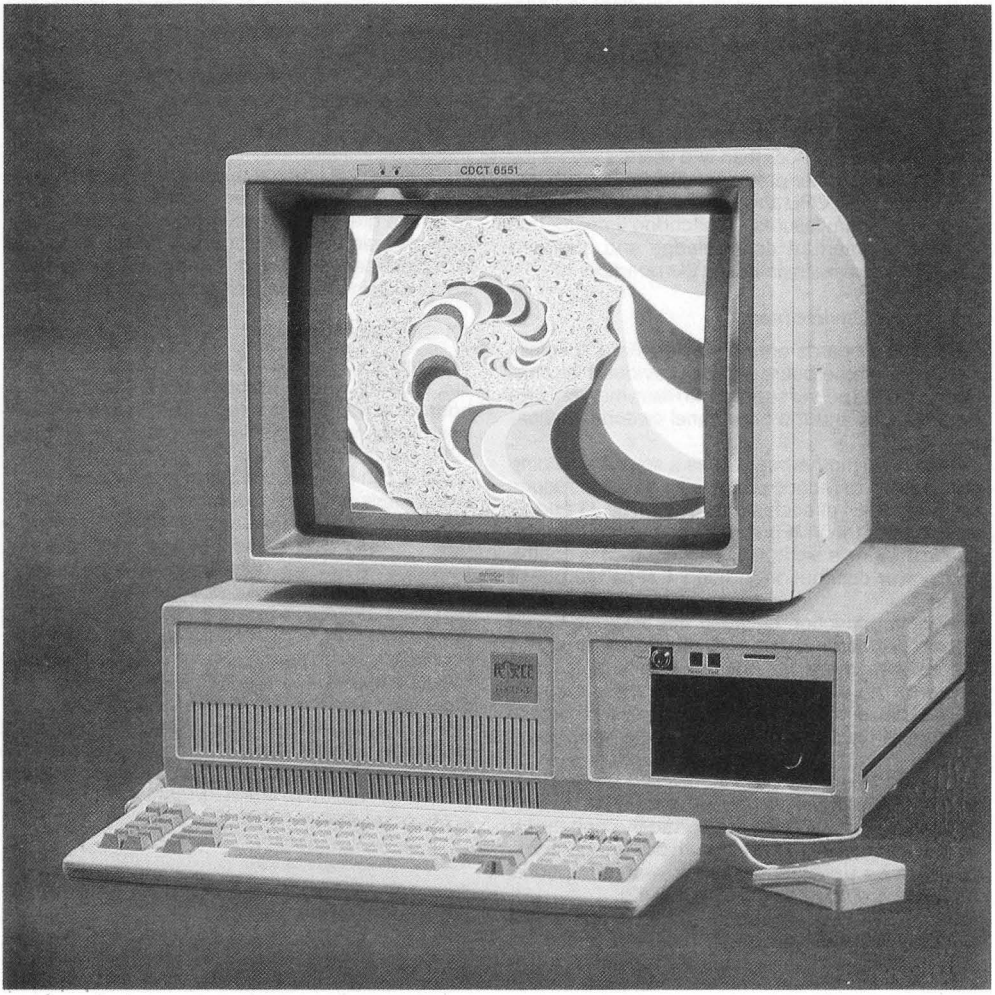
4.2 Memory Extension

Dynamic memory on the VMEbus can be added using the DRAM-6 or DRAM-7 boards providing 2 Mbyte or 8 Mbyte respectively, of global memory. The access time on read/write cycles is 170/70 ns.
Static memory with battery backup of up to 1 year can be added by using the SRAM-5 or the SRAM-6 boards. The memory capacity is 512 Kbyte or 2 Mbyte, at a read/write access time of 50/50 ns.
All memory boards have a full 32 bit data and address path conforming to the VMEbus specification. Read-Modify-Write as well as aligned and unaligned transfers are supported.

4.3 Tower Extension

Mounting equipment for the FOCUS series of products and an additional module allows the usage of the system as a "Tower" (as shown on page 3).

PHOTO OF THE DESK TOP VERSION



Specifications

Main CPU of the System 25U	68020	16.7 MHz
Main CPU of the System 25AU	68020	20.0 MHz
Floating Point Coprocessor	68881	16.7/20.0 MHz
Paged Memory Management Unit	68851	16.7/20.0 MHz
Local Main Memory	SRAM	1 Mbyte
No. of Wait States	1	Constantly
VME Main Memory	DRAM	4 Mbyte
Total Memory Capacity	RAM	5 Mbyte
EPROM	1 Socket	64 Kbyte
Serial I/O Interfaces		
Master Console	1	RS232
Host Computer	1	RS232/422
High Speed Data Link	1	RS232/422
Terminal Interfaces via Intelligent Controller	8	RS232
9 Pin D-sub Connectors	16	Preconfigured
Mass Memory		
Winchester Capacity	170 Mbyte	Unformatted
	130 Mbyte	Formatted
Transfer Speed	1.5 Mbyte/s	
Average Access Time	23 ms	5 ms track-to-track
Track-to-Track Access Time	5 ms	
Cartridge Tape Drive	125 Mbyte	SCSI compatible
Floppy Disk	1 Mbyte	Unformatted
Intelligent Controller Board Interfaces	SCSIbus, SA460	
Real-Time Clock with Battery Backup	58167	
Printer Interfaces	RS232	Serial
	Centronics	Parallel
GPIB Interface	IEEE 488	
Bus System	VMEbus	A32 : D32
Total No. of Slots	12	6 + 6
Used VMEbus Boards	ASCU-2, CPU-25(A)	
	ISIO-1, CPU-25(B)	
	ISCSI-1, SRAM-22	
	DRAM-E4M4	
No. of Free Slots	5	
Power Requirements	110V	6.5A (avg)
	220V	3.2A (avg)
Spurious Radiation conforms to	VDE 0871/Class B	
Security Level conforms to	VDE 0806/IEC 380	
DC Power Specification	+ 5V	64A (max)
	+12V	10A (max)
	−12V	2A (max)
Surge Current	12A at 220V	
	22A at 110V	
Main Voltage	100 – 120V	
	200 – 240V	
Power Consumption	690W	
Thermal Dissipation	192 KJ/h	
Enclosure Dimensions	Height 170 mm	6.7 in.
	Depth 540 mm	21.3 in.
	Width 600 mm	23.7 in.
Weight	40 kg	88 lb
Operating Temperature	5-45 degrees C	
Storage Temperature	5-95 degrees C	non-operation
Relative Humidity	10 – 70%	non-condensing

Ordering Information

System 25U Part No. 641025	FORCE FOCUS 32 with 16.7 MHz 68020, 68851, 68881 CPU Board and UNIX* System V Release 3(2).
System 25U/UM Part No. 800128	User's Manual of the System 25U/25AU
System 25AU Part No. 641027	FORCE FOCUS 32 with 20.0 MHz 68020, 68851, 68881 CPU Board and UNIX* System V Release 3(2).

Hardware Extensions:

SYS68K/AGC-1 Part No. 400020	High Resolution Graphics Board Set (2 slots)
SYS68K/ISIO-1 Part No. 310030	Additional 8 channel serial I/O controller board to be installed at slot 12
SYS68K/DRAM-E4S4 Part No. 200111	4 Mbyte dynamic RAM board with byte parity check
SYS68K/DRAM-7 Part No. 200131	8 Mbyte dynamic RAM board with byte parity check
SYS68K/SRAM-4B Part No. 200502	1 Mbyte static RAM board including battery backup
SYS68K/CABLE-9/25 Part No. 700031	8 cable adaptors from 9 pin D-sub connector to 25 pin D-sub connector
FOCUS 32 TOWER Part No. 700041	Mounting equipment for usage of the FOCUS systems as a tower

Software Extensions:

SYS68K/UNIX*-PAS020 Part No. 150006	PASCAL Compiler under UNIX* for 68020
SYS68K/GKSGRAL-U2B1 Part No. 160001	GKS level 2b for FORTRAN 77 and C under UNIX*

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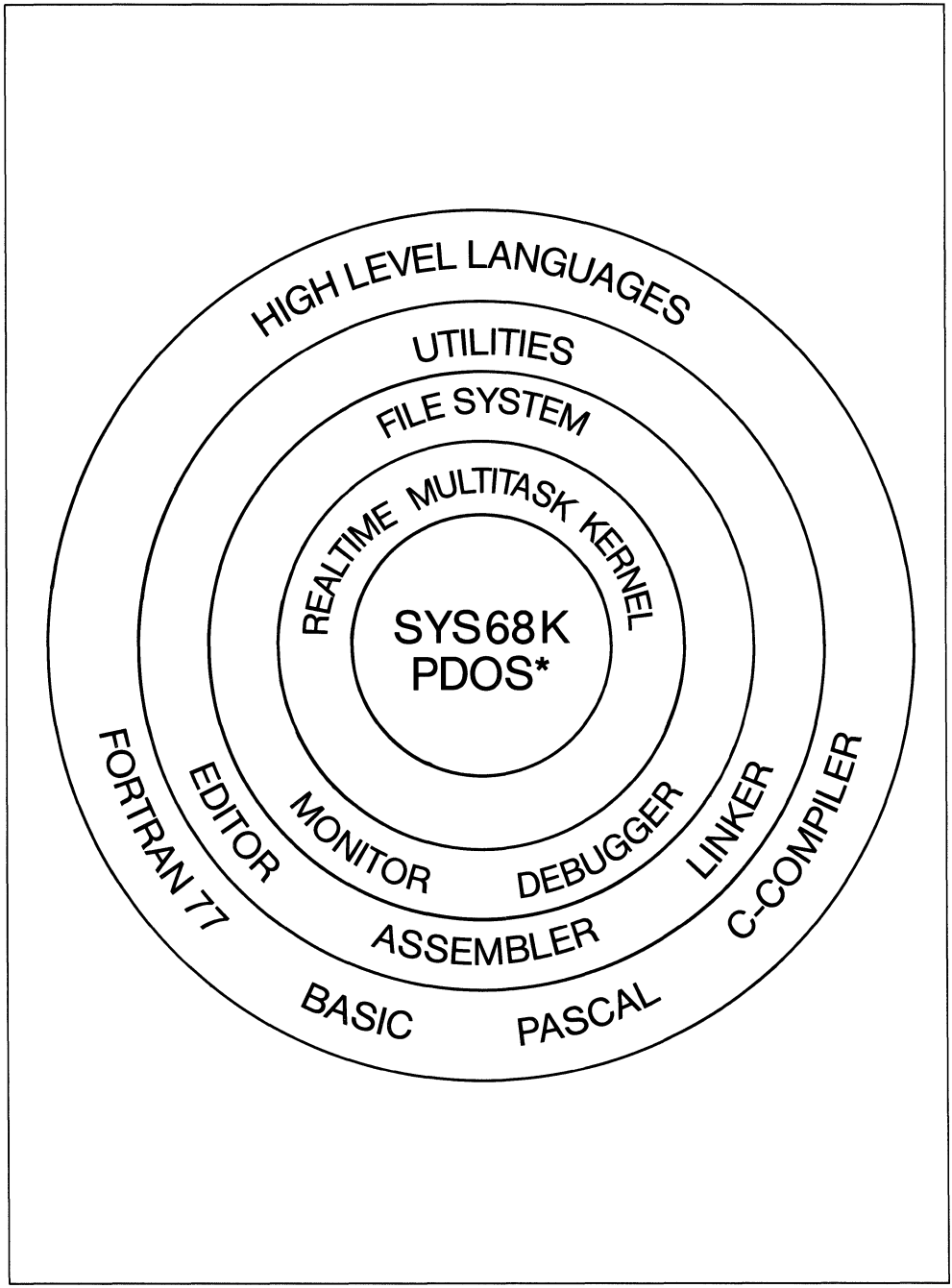
Software

System 68000 VME SYS68K/PDOS*

Operating System

- Real Time, Multi-User, Multi-Tasking
- Configurable, romable
- Full 68000/68020 support
- Real Time Compilers


HIGH LEVEL LANGUAGES
UTILITIES
FILE SYSTEM
REALTIME MULTITASK KERNEL
SYS68K
PDOS*
FORTRAN 77
EDITOR
MONITOR
DEBUGGER
LINKER
C-COMPILER
ASSEMBLER
BASIC
PASCAL

1. DESCRIPTION:

PDOS* is a powerful multi-user, multi-tasking operating system developed for the 32-bit Motorola 68000 processor family. This development software is designed for scientific, educational, industrial, and business applications. PDOS* consists of a small, real time, multi-tasking kernel layered by file management, floating point, and user monitor modules. The 8 Kbyte kernel provides synchronization and control of events occurring in a real-time environment using semaphores, events, messages, mailboxes, and suspension primitives. All user console I/O as well as other useful conversion and housekeeping routines are included in the PDOS* kernel. The file management module supports named files with sequential, random, and shared access. Mass storage device independance is achieved through read and write logical sector primitives. The designer is relieved of real-time and task management problems as well as user console interaction and file manipulation so that efforts can be concentrated on the application.

2. FUNCTIONAL DESCRIPTION:

2.1 PDOS* KERNEL.

PDOS* is written in 68000/68020 assembly language for fast, efficient execution. The small kernel provides multi-tasking, real-time clock, event processing, and memory management functions. Ready tasks are scheduled using a prioritized, round-robin method. The A-line emulation exception is used to interface over 100 system primitives to a user task.

2.2 MULTI-TASKING EXECUTION ENVIRONMENT.

Tasks are the components comprising a real-time application. Each task is an independant program that shares the processor with other tasks in the system. Tasks provide a mechanism that allows a complicated application to be subdivided into several independant, understandable, and manageable modules. Real-time, concurrent tasks are allocated in 2 Kbyte increments. Task system overhead is less than 1.25 Kbyte.

2.3 INTERTASK COMMUNICATION & SYNCHRONIZATION.

Semaphores and events provide a low overhead facility for one task to signal another. Events can be used to indicate availability of a shared resource, timing pulses, or hardware interrupt occurrences. Messages and mailboxes are used in conjunction with system lock, unlock, suspend, and event primitives. PDOS* provides timing events that can be used in conjunction with desired events to prevent system lockouts. Other special system events signal character inputs and outputs.

2.4 MEMORY REQUIREMENTS.

PDOS* is very memory efficient. The PDOS* kernel, floating point module, file manager, and user monitor utilities require only 24 Kbyte of memory plus an additional 4 Kbyte for system buffers and stacks. Applications memory reduction can be achieved by linking the user application to a 8 Kbyte PDOS* kernel for a small, ROMable, standalone, multi-tasking module. A fast, 16 Kbyte scientific orientated BASIC interpreter with real-time primitives provides interactive high level language support as well. For large system configurations, PDOS* effectively addresses up to a 32 bit address space.

2.5 FILE MANAGEMENT.

The PDOS* file management module provides sequential, random, read only, and shared access to named files on a secondary storage device. These low overhead file primitives use a linked, random access file structure and a logical sector bit map for allocation of secondary storage. No file compaction is ever required. Files are time stamped with date of creation and last update. Up to 128 files can be simultaneously opened. Complete device independence is achieved through read and write logical sector primitives.

2.6 COMMAND LINE INTERPRETER.

A resident command line interpreter allows multiple commands to be entered on a single line. Command utilities such as append, define, delete, copy, rename, and show file are also resident and can be executed without destroying current memory programs. Other functions resident in the monitor include setting the baud rate of a port, checksumming memory, creating tasks, listing tasks, files and open file status, asking for help, setting file level, file attributes, interrupt mask, and system disk, and directing console output.

2.7 INTERRUPT MANAGEMENT.

The PDOS* kernel handles user console, system clock, and other designated hardware interrupts. User consoles have interrupt driven character I/O with type ahead. A task can be suspended pending a hardware or software event. PDOS* will switch control to a task suspended on an external event within 30 microseconds after the occurrence of the event (provided the system mask is high enough). Otherwise, a prioritized, round-robin scheduling of ready tasks occurs at 10 millisecond intervals.

2.8 PORTABILITY.

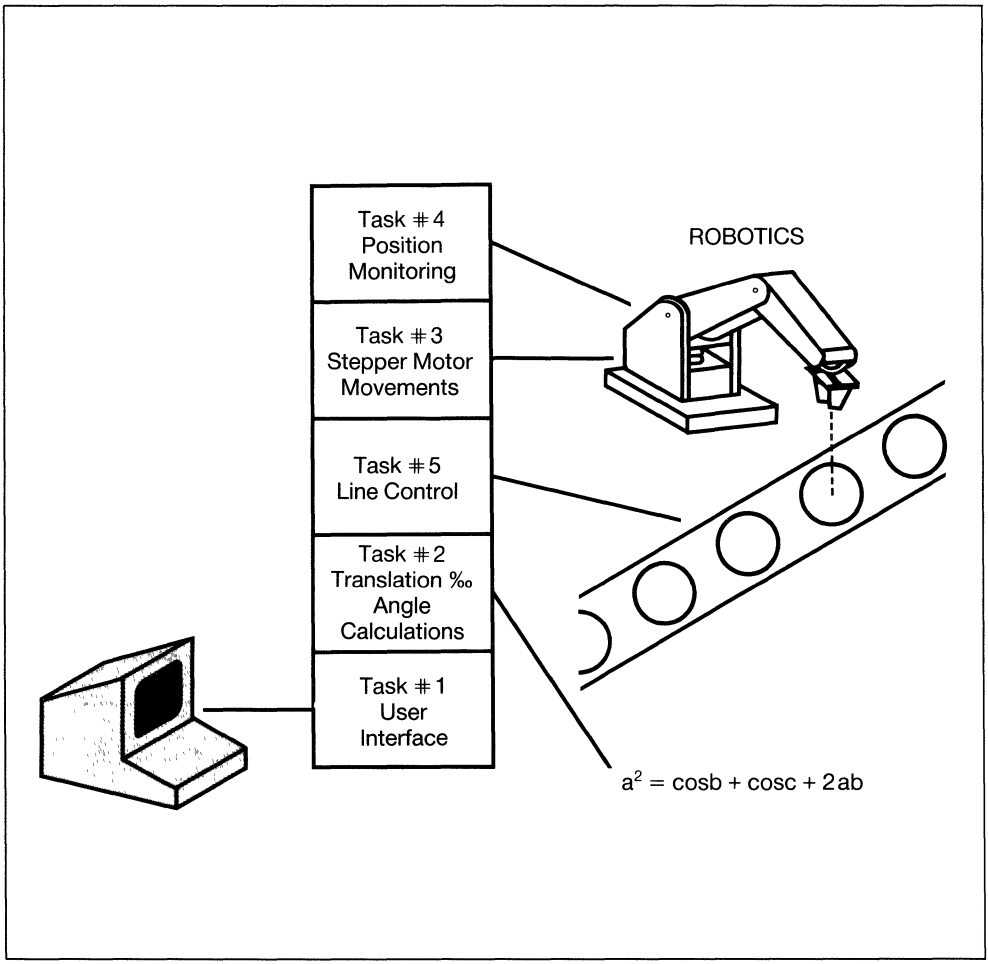
PDOS* gives software portability through hardware independance of read/write logicial sector primitives. All other hardware functions such as clocks, mappers, and UARTS are conveniently isolated for minimal customization to new 68000 based systems.

2.9 CUSTOMER SUPPORT.

Numerous support utilities including virtual screen editors, assembler, linker, macroprocessor, disk diagnostics, link, and recovery, disk cataloging are standard. Single stepping, multi break points, memory snap shots, save and restore task commands, and error trapping primitives are provided in all languages to aid in program debugging.

PDOS* DISK OPERATING SYSTEM

FEATURES:
- Real Time, Multi-User, Multi-Tasking
- Multiprocessing support
- Prioritized, Round-Robin scheduling
- Intertask Communication and synchronisation
- Task memory map control for program security
- Full exception processing
- Sequential, Random, and shared file management
- Hardware independence
- Kernel, file Manager and Monitor are written in 68000/68020 assembly language.
- Configurable, modular, Romable standalone support



3. LANGUAGE SUPPORT:

- Basic — Standard Dartmouth Basic with enhancements, such as program debugging, intertask communication and real-time support.
- Pascal — multi-pass, optimizing compiler that generates assembler text for the 68000 microprocessor. The PDOS* Pascal compiler implements a superset of the Pascal language defined by Jensen and Wirth.
- Fortran 77 — compiler, supporting the full ANSI Fortran 77 standard
- C — Compiler for the C language

PDOS* SYSTEM CALLS

Append file
Baud console port
Build file directory list
Chain command
Check for break character
Check for break or pause
Clear screen
Close file
Close file w/attribute
Conditional get character
Convert ASCII to binary
Convert binary to decimal
Convert binary to hex
Convert binary to hex in buffer
Convert to dec w/message
Convert to decimal in buffer
Copy file
Create task block
Debug call
Define file
Define trap vectors
Delay set/reset event
Delete file
Dump memory from stack
Dump registers
Enter supervisor mode
Enter supervisor mode
Execute PDOS call to D7.W
Exit to monitor
Exit to monitor w/command
File altered check
Fix file name
Fix time and date
Flush buffers
Free user memory
Get character
Get character conditional
Get disk size
Get line buffer
Get line in monitor buffer
Get line in user buffer
Get memory limits
Get message pointer
Get next Parameter
Get port character
Get task message
Get user memory
Initialize sector
Kill task
Kill task message
List file directory
Load error register
Load file
Load status register
Lock file

Lock task
Look for name in file slots
Open non-exclusive random
Open random
Open random read only
Open sequential
Pack ASCII date
Position cursor
Position file
Push command to buffer
Put buffer to console
Put character raw
Put character(s) to console
Put CRLF to console
Put data to console
Put encoded line to console
Put encoded message to console
Put line to console
Put message to console
Put space to console
Read bytes from file
Read date
Read directory entry by name
Read file attributes
Read file from position
Read line from file
Read next directory entry
Read port cursor position
Read port status
Read sector
Read sector zero
Read status register
Read task status
Read time
Rename file
Reset console inputs
Reset disk
Return error Do to monitor
Return from interrupt
Return to user mode
Rewind file
Send message pointer
Send task message
Set event flag w/swap
Set event flag
Set port flag
Set/read task priority
Suspend until interrupt
Swap to next task
Tab to column
Test event flag
Unlock file
Unlock task
Unpack ASCII date
Unpack date
Unpack time
Write bytes to file
Write date
Write file attributes
Write file parameter
Write line to file
Write sector
Write time
Zero file

PDOS* UTILITIES

FxFRMT	Format logical unit
FxLDGO	Load and execute operating system
FxPARK	Flush buffers and park Winchester heads
MABORT	Task aborter
MASM	68000/68010 Macro assembler
MASM20	68020 Macro assembler
MBACK	Disk Backup
MCHATLE	Change file attributes and levels
MDCOMP	Disk file compare
MDDMAP	Disk Map, read files by link
MDDUMP	Disk dump and alter by sector
MDDISK	Disk name list
MDLOOK	Disk look, look at disk sector contents
MDNAME	Rename disk
MDSAVE	Disk file recovery
MEDIT	Configurable screen edit
MFDUMP	File dump in hex and ASCII
MFFIND	Multiple disk search for file
MFSAVE	File recovery
MINIT	Disk initialization
MINST	Additional memory installation
MLDIR	Directory list
MLEVEL	Directory list by level
MLIB	Library file manager
MLIBGEN	Library generator
MMKBT	Install PDOS Boot on Disk
MORDIR	Alphabetize Directory
MPATCH	Apply a program upgrade patch
MSREC	Build S-record
MSYFL	Build SY object file
MSYOB	Build object from SY file
MTERM	Set task terminal characteristics
MTIME	Read/Set clock calendar (if applicable)
MTRANS	Multiple file transfer
MUNDL	Undelete file
QLINK	PDOS linker
WIND1	Create virtual porting task
WKILL	Disable virtual ports
WLOOK	View virtual port parameters
WTERM	Set terminal type for virtual ports

PDOS* MONITOR COMMANDS

Append file	Free memory	RAM disk
Assign console review	Get memory	Rename file
Baud port	Goto	Reset console
Console unit	Help	Reset disk
Copy file	If altered	Save to file
Create task	If processor	Send message
Date and time	If processor	Set file attributes
Define file	Kill message	Set system date/time
Delete file	Kill task	Set/reset event
Delete multiple file	List directory	Show file
Directory level	List error	Spool unit
Disk space	List level	System disk
Download file to port	List tasks	Task priority
Enable/disable echo	Load file	Transfer files
Execute	Make file	Transparent mode
File slot usage	PDOS BASIC	Upload file from port
For every	PDOS debugger	Zero memory

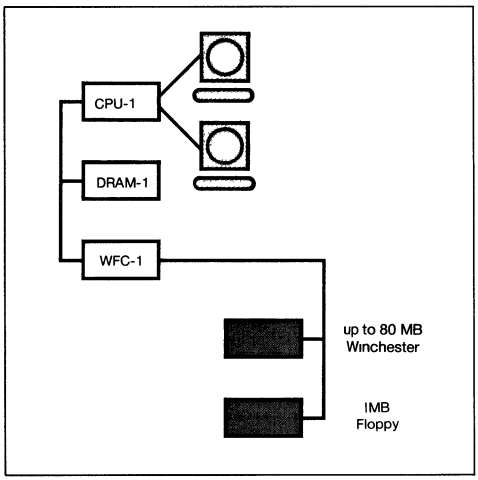
4. HARDWARE CONFIGURATION:

The SYS68K/PDOS* Operating System is implemented on the following hardware:

CPU boards
CPU-1, CPU-2, CPU-4, CPU-5, CPU-6, CPU-21, CPU-22, CPU-26, CPU-29

Memory boards
DRAM-1, DRAM-2, DRAM-E3M1, DRAM-E3S3, DRAM-E4M4, DRAM-E4S12, DRAM-6

Controller boards
WFC-1, SIO-2, ISIO-1/1A, ISIO-2/2A, ISCSI-1/1A, AGC-1, ASCU-1/2, AGC-2



5. DELIVERY MEDIA:
SYS68K/PDOS* is shipped on 5 1/4 inch Floppies.
The package includes two boot EPROMS and documentation.

ORDERING INFORMATION

SYS68K/PDOS	Operating System on 5 1/4 inch Floppies, boot EPROMS and documentation. PDOS CPU-1 PDOS CPU-2 PDOS CPU-4 PDOS CPU-5 PDOS CPU-6 PDOS CPU-21 PDOS CPU-22 PDOS CPU-26 PDOS CPU-29
SYS68K/PDOS/UM Part No. 800031	User's documentation.
SYS68K/PDOS/PASCAL Part No. 140020 Part No. 140021	Pascal Compiler and documentation For all 68000/68010 CPUs For all 68020 CPUs
SYS68K/PDOS-PAS/UM Part No. 800032	Pascal User's documentation.
SYS68K/PDOS/FORTRAN Part No. 140040 Part No. 140041	FORTRAN 77 Compiler and documentation For all 68000/68010 CPUs For all 68020 CPUs
SYS68K/PDOS-FOR/UM Part No. 800040	FORTRAN User's documentation
SYS68K/PDOS/C Part No. 140030 Part No. 140031	C compiler and documentation For all 68000/68010 CPUs For all 68020 CPUs
SYS68K/PDOS-C/UM Part No. 800041	C compiler User's documentation

System 68000
SYS68K/VMEPROM

PDOS* Based Real Time Operating Monitor

- **Real Time, Multi-Tasking Kernel**
- **Full Debugging Facilities**
- **68000/020 Support**

1. General Description

VMEPROM is an EPROM based real-time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM. VMEPROM is composed of the powerful PDOS* Real Time Kernel and the PDOS* file manager. Thus the package provides support of a highly sophisticated Real Time Kernel and an interface to floppy and hard disk drives.
The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition, it includes a powerful line assembler and disassembler for the 68020/68881 or the 68000/68010.

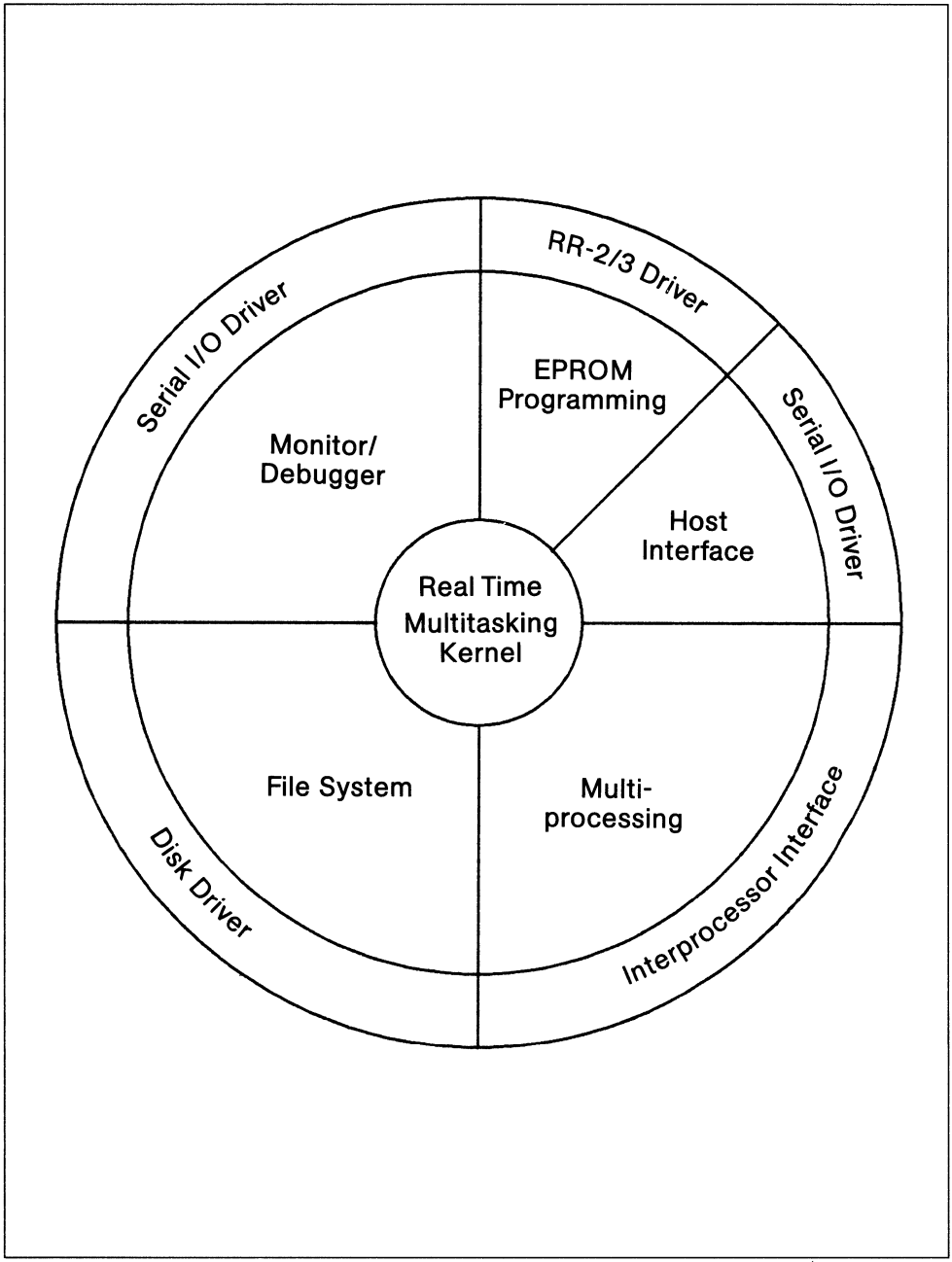
VMEPROM features:

- Real Time Multitasking Kernel supporting up to 64 tasks.
- File management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Task management system calls.
- Line assembler/disassembler with full support of all 68000/68010 or 68020/68881 instructions.
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify.
- Display and modify floating point data registers of the 68881 (68020 version only).
- S-record up/downloading from any port defined in the system.
- Time stamping of user programs.
- Built-in benchmarks
- Disk support for RAM-disk, floppy and Winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. VMEPROM also allows disk formatting and initialization.
- Serial I/O support for up to two SIO-1/2 or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full screen editor.
- More than 30 commands to control the PDOS* kernel and file manager.
- Complete task management.
- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.
- Data conversion system calls.
- Terminal I/O functions.

2. Description of the User Interface of VMEPROM

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple commands may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

BLOCK DIAGRAM OF THE SYS68K/VMEPROM



Command set summary

#	Name processor
AF	Append file
ARB	Set Arbiter
AS	Line assembler
ASSIGN	Set port number
BASE	Set base
BENCH	Benchmarks
BF	Fill memory
BM	Move date
BP	Baud port
BR	Breakpoints
BS	Search value
BT	Test memory
BV	Compare memory
CF	Copy file(s)
CT	Create task
COLD	Coldstart VMEPROM
CONFIG	Configure VMEbus
DD	Disk Dump
DI	Disassembler
DF	Define file
DL	Delete file(s)
DN	Rename disk
DR	Display registers
DRF	Display 68881 regs
DT	Show date/time
DU	Dump S-record
ED	Screen editor
ER	Display Error
EV	Events
FD	File Dump
FM	Free memory
FRMT	Format disk
FS	File slot usage
G	Execute program
GO	Alias for G
GD	GO direct
GM	Get memory
GOTO	Goto string
GT	GO w/temp. break
IA	File altered
ID	Set date and time
INIT	Init disk
KM	Kill message
KT	Kill task
LC	Directory
LD	Load file to mem
LO	Load S-record
LS	Directory
LT	List tasks
LV	Directory level
M	Modify memory
MM	Alias for M
MD	Dump memory
MEM	Set bus width
MF	Make file
MS	Preset memory
RC	Reset console
RD	Set RAM disk
RM	Modify registers
RN	Rename file(s)
RR2	Program EPROMs
RS	Reset disk
SA	Set attribute
SF	Show file
SM	Send message
SP	Disk usage
ST	Set terminal type
SV	Save to file
SY	Set system disk
T	Trace program
TC	Set trace count
TIME	Measure run time
TJ	Trace on jumps
TM	Transparent mode
TP	Set task priority
TT	Alias for T
UN	Set unit mask
ZM	Zero memory

VMEPROM Benchmarks

The following benchmarks are contained in VMEPROM. The given execution times are measured with a CPU-21B (68020 with 25 MHz, 68881 with 20 MHz).

Bench #	Benchmark type	Time (sec)
1	Decrement long word in memory, 100.000 times	04.83
2	Pseudo DMA 1 Kbyte, 50.000 times	06.23
3	Substring character search, 100.000 times (taken from EDN, 08/08/85)	06.06
4	Bit Test/Set/Reset, 100.000 times (taken from EDN, 08/08/85)	01.84
5	Bit Matrix Transposition 100.000 times (taken from EDN, 08/08/85)	06.81
6	Cache test (executes 128 Kbyte program 1000 times)	14.54
7	1.000.000 Additions (extended precision)	01.48
8	1.000.000 Sines (extended precision)	17.30
9	1.000.000 Multiplications (extended precision)	03.22
10	100.000 Context switches	02.83
11	100.000 Set system event	01.97
12	100.000 Change task priority	02.40
13	100.000 Send and Receive task message	15.15
14	100.000 Read system time	01.82

3. Description of the Kernel functions

The kernel of VMEPROM is written in 680x0 assembly language for fast and efficient execution. It provides multitasking, system clock, event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously. Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.
VMEPROM handles user console, system clock and other hardware interrupts.
A task can be suspended pending a hardware or software event. Control is switched to a suspended task within 28 microseconds (68020, 25 MHz) after the occurrence of the event.

Kernel system calls

X881 – SAVE 68881 ENABLE
XBCP – BAUD CONSOLE PORT
XCBC – CHECK FOR BREAK CHARACTER
XCBD – CONVERT BINARY TO DECIMAL
XCBH – CONVERT BINARY TO HEX
XCBM – CONVERT TO DECIMAL W/MESSAGE
XCBP – CHECK FOR BREAK OR PAUSE
XCBX – CONVERT TO DECIMAL IN BUFFER
XCDB – CONVERT ASCII TO BINARY
XCFA – CLOSE FILE W/ATTRIBUTE
XCHX – CONVERT BINARY TO HEX IN BUF.
XCLS – CLEAR SCREEN
XCPY – COPY FILE
XCTB – CREATE TASK BLOCK
XDEV – DELAY SET/RESET EVENT
XDMP – DUMP MEMORY FROM STACK
XDTV – DEFINE TRAP VECTORS
XERR – RETURN ERROR D0 TO MONITOR
XEXC – EXECUTE PDOS* CALL D7
XEXT – EXIT TO MONITOR
XFTD – FIX TIME & DATE
XFUM – FREE USER MEMORY
XGCB – CONDITIONAL GET CHARACTER
XGCC – GET CHARACTER CONDITIONAL
XGCP – GET PORT CHARACTER
XGCR – GET CHARACTER
XGLB – GET LINE IN BUFFER
XGLM – GET LINE IN MONITOR BUFFER
XGLU – GET LINE IN USER BUFFER
XGML – GET MEMORY LIMITS
XGMP – GET MESSAGE POINTER
XGNP – GET NEXT PARAMETER
XGTM – GET TASK MESSAGE
XGUM – GET USER MEMORY
XKTB – KILL TASK
XKTM – KILL TASK MESSAGE
XLER – LOAD ERROR REGISTER
XLKT – LOCK TASK
XLSR – LOAD STATUS REGISTER
XPAD – PACK ASCII DATE
XPBC – PUT BUFFER TO CONSOLE
XPCC – PUT CHARACTER(S) TO CONSOLE
XPCL – PUT CRLF TO CONSOLE
XPCR – PUT CHARACTER RAW
XPDC – PUT DATA TO CONSOL
XPEL – PUT ENCODED LINE TO CONSOLE
XPEM – PUT ENCODED MESSAGE TO CONSOLE
XPLC – PUT LINE TO CONSOLE
XPMC – PUT MESSAGE TO CONSOLE
XPSC – POSITION CURSOR
XPSP – PUT SPACE TO CONSOLE
XRCP – READ PORT CURSOR POSITION
XRDM – DUMP REGISTERSN
XRDT – READ DATE
XRPS – READ PORT STATUS
XRSR – READ STATUS REGISTER
XRTE – RETURN FROM INTERRUPT
XRTM – READ TIME
XRTP – READ TIME PARAMETERS
XRTS – READ TASK STATUS
XSEF – SET EVENT FLAG W/SWAP
XSEV – SET EVENT FLAG
XSMP – SEND MESSAGE POINTER
XSPF – SET PORT FLAG
XSTM – SEND TASK MESSAGE
XSTP – SET/READ TASK PRIORITY
XSUI – SUSPEND UNTIL INTERRUPT
XSUP – ENTER SUPERVISOR MODE
XSWP – SWAP TO NEXT TASK
XTAB – TAB TO COLUMN
XTEF – TEST EVENT FLAG
XUAD – UNPACK ASCII DATE
XUDT – UNPACK DATE
XULT – UNLOCK TASK
XUSP – RETURN TO USER MODE
XUTM – UNPACK TIME
XWDT – WRITE DATE
XWTM – WRITE TIME

4. Description of the File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

These low overhead file primitives use a linked, random access file structure and a logical sector bit map for storage allocation. Files are time stamped with the date and time of creation and last update. Up to 64 files may be open at the same time.

File manager system calls

XAPF – APPEND FILE
XCFA – CLOSE FILE W/ATTRIBUTE
XCLF – CLOSE FILE
XCPY – COPY FILE
XDFL – DEFINE FILE
XDLF – DELETE FILE
XFAC – FILE ALTERED CHECK
XFBF – FLUSH BUFFERS
XFFN – FIX FILE NAME
XISE – INITIALIZE SECTOR
XLDF – LOAD FILE
XLFN – LOOK FOR NAME IN FILE SLOTS
XLKF – LOCK FILE
XNOP – OPEN SHARED RANDOM FILE
XPSF – POSITION FILE
XRBF – READ BYTES FROM FILE
XRCN – RESET CONSOLE INPUTS
XRDE – READ NEXT DIRECTORY ENTRY
XRDN – READ DIRECTORY ENTRY BY NAME
XRFA – READ FILE ATTRIBUTES
XRFP – READ FILE POSITION
XRLF – READ LINE FROM FILE
XRNF – RENAME FILE
XROO – OPEN RANDOM READ ONLY FILE
XROP – OPEN RANDOM
XRSE – READ SECTOR
XRST – RESET DISK
XRSZ – READ SECTOR ZERO
XRWF – REWIND FILE
XSOP – OPEN SEQUENTIAL FILE
XSZF – GET DISK SIZE
XULF – UNLOCK FILE
XWBF – WRITE BYTES TO FILE
XWFA – WRITE FILE ATTRIBUTES
XWFP – WRITE FILE PARAMETERS
XWLF – WRITE LINE TO FILE
XWSE – WRITE SECTOR
XZFL – ZERO FILE

5. Supported VMEbus Hardware

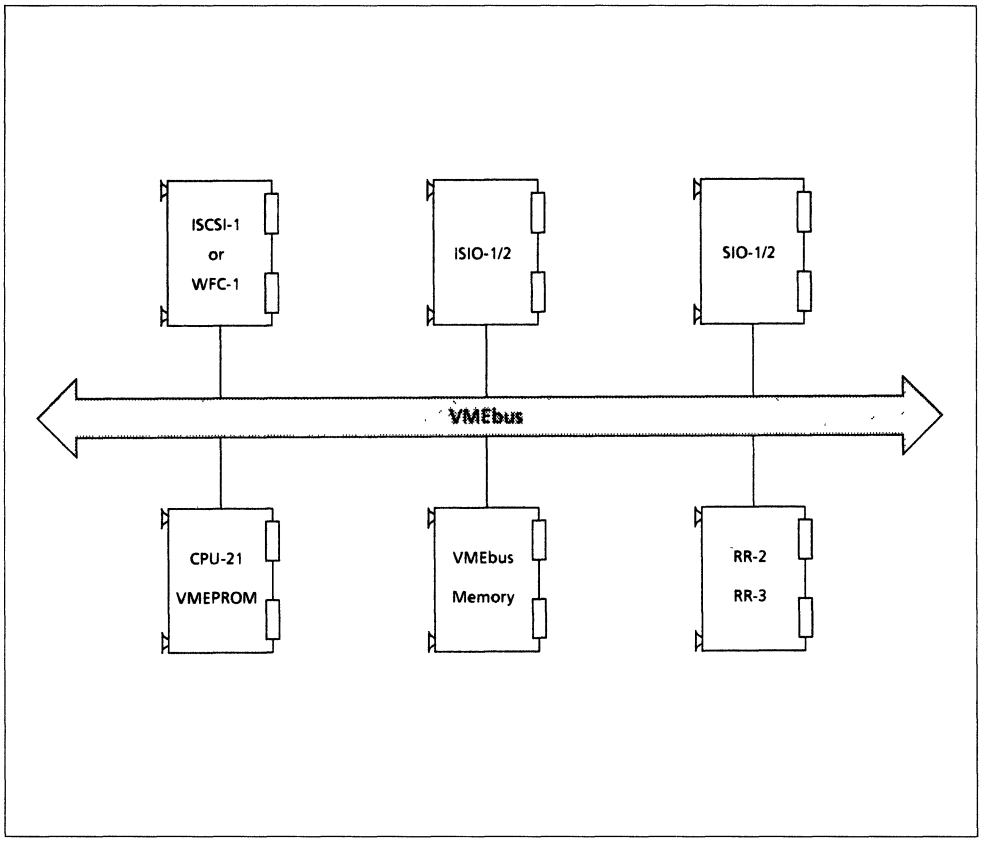
Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards, which may be the SYS68K/SIO-2 or the SYS68K/ISIO-1/2.
In addition, one disk controller is supported by VMEPROM. This can be either a SYS68K/ISCSI-1 or a SYS68K/WFC-1.
Both the serial I/O controllers and the disk controllers are interrupt driven.
EPROM programming is supported by VMEPROM utilizing the SYS68K/RR-2/3 board family. Two commands are available to program EPROMs directly from the VMEPROM command line. The code to be programmed may reside in memory, on RAM disk or an external mass storage device such as a floppy disk or a Winchester disk.

6. Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 40 Kbyte. Small romable applications can be put in EPROMS easily without the overhead of the user interface.

7.0 Development Systems

Currently either one of the FORCE PDOS* or UNIX* System V development stations may be used for software development for VMEPROM.
Compilers, assemblers, and libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.



7.1 UNIX System V Development Systems

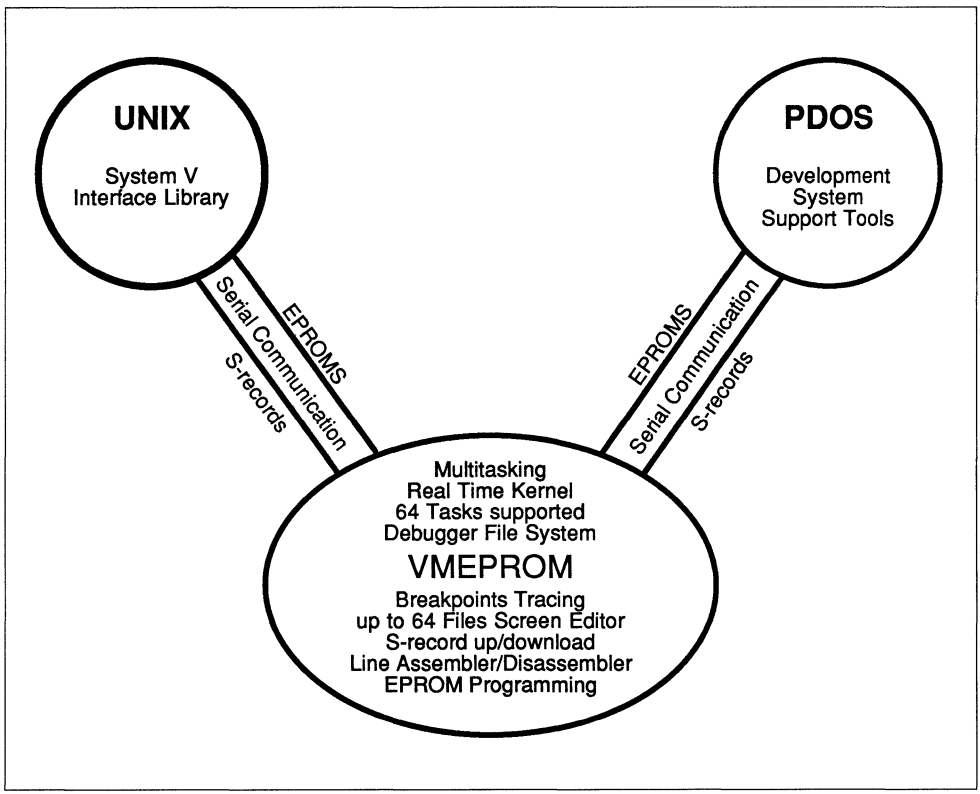
The FORCE FOCUS UNIX* System V family of development systems contains the UNIX* to VMEPROM link. This package is available free of charge on every UNIX* system. It consists of C – libraries and utilities making the software development for VMEPROM under UNIX* an easy task.
Also supported under UNIX* are EPROM programming as well as program downloading to the target system using S-records.
A transparent mode is also available thus allowing to debug or execute VMEPROM tasks from the UNIX* console.

7.2 PDOS* Development Systems

As VMEPROM is based on the powerful PDOS* Real Time Kernel, the PDOS* operating system is best suited for software development for VMEPROM. The PDOS* operating system supports EPROM programming and code downloading to VMEPROM via S-records. The transparent mode is also supported under PDOS* to allow program debugging from the PDOS* terminal.
No additional tools or utilities are required when using the PDOS* operating system for software development for VMEPROM.

7.3 IBM-AT Development Systems

VMEPROM is also supported by the family of IBM-AT or true compatible development systems.
The link is based on a special version of the Alcyon C-compiler,a cross assembler for the 680x0 processor family and utilities to download the code to the target systems for debugging.



7.4 Other Development Systems

The support of VMEPROM through other development systems like the HP systems or the VAX is under development. These cross-software development packages will be available by begin of 1988 and will include compilers, cross-assemblers and libraries to fully support program development for VMEPROM based target systems.

8. Licensing

No license is required for VMEPROM. VMEPROM is delivered free of charge and is currently implemented on the following FORCE CPU-boards:

- SYS68K/CPU-4*
- SYS68K/CPU-5*
- SYS68K/CPU-6*
- SYS68K/CPU-20
- SYS68K/CPU-21
- SYS68K/CPU-22
- SYS68K/CPU-26
- SYS68K/CPU-29
- SYS68K/CPU-32

*VMEPROM is available on these boards starting Q4/87.

This gives full software compatibility and portability between the above listed CPU-boards.

NOTE: VMEPROM will be supplied free of charge on future 32 bit CPU board designs from FORCE Computers.

Ordering Information

SYS68K/VMEPROM/UM Part No. 800140	VMEPROM User's Manual
SYS68K/VMEPROM Link-1 Part No. 140110	SW link from the IBM-AT to VMEPROM including documentation

PDOS* is a trademark of Eyring Research Institute
UNIX* is a trademark of Bell Laboratories

System 68000 VME SYS68K/UNIX*

Operating System

- **UNIX System V Release 2 (3)**
- **Full 68000/68010/68020 support**
- **C and FORTRAN Compiler inclusive**

1.0 General Information

The UNIX* operating system implemented on the 68010/68020 microprocessor is derived from the original AT&T UNIX System V. FORCE Computers has implemented the UNIX System V for the 68010 on its own hardware. The UNIX operating system is implemented on several microprocessors and mainframes. Each of these UNIX operating system versions differs mainly in the features, capabilities and application packages supported by the system. However, the basic operating system software functions in each case in the same way.

The UNIX Operating System oversees the execution of many user programs and commands. It seems to execute programs simultaneously because of the system's ability to time-share the processor among all of the programs. In actual fact, each program will be scheduled to use the processor for a short period of time to the exclusion of all other programs.

Therefore, in addition to providing a multiuser system, the UNIX operating system provides the capability for each user to run several programs at once. This is called multitasking.

The UNIX System V for 68K includes:

- the operating system kernel
- the "shell" command interpreter
- the file system
- various standard user and system commands.

The kernel is the basic resident software on which the entire system relies. It is the only permanently resident part of the system. The shell command interpreter allows the user to communicate with the UNIX operating system. The shell, besides providing the user interface to the kernel, and interpreting operating system commands, also can be used as a programming language.

2.0 Features:

Some of the major features of the UNIX operating system are:

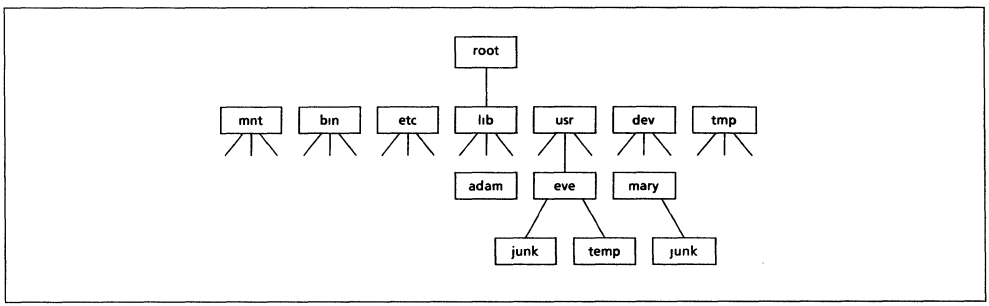
- a flexible, easy to use command language
- a wide variety of supported applications
- access to the facilities of other computer systems
- a practical file system structure
- many high-level programming languages (FORTRAN 77, PASCAL, C)
- system programming and debugging tools
- a package of terminal routines that allow user programs to produce output on many different types of terminals
- Easy implementation of different terminals
- on-line help facilities which are useful to both beginners and experienced users
- Tree-like structure of the file system (hierarchical file system)

3.0 File System

The file system of the UNIX operating system consists of a set of directories and files arranged in a tree-like structure.The file system is built up from the root (/) directory (see Figure 1-1). Although the operating system does not require the file system to be structured a certain way, the root directory normally contains certain standard subdirectories:

mnt	Used to mount a backup file system for file restoring.
bin	Most user commands are kept here. There are also many commands in /usr/bin.
dev	The standard location for special files associated with physical devices. All input/output is done by accessing the files in this directory.
etc	Administrative programs and data tables are kept here. The /usr/adm directory is also used for system administration.
lib	A library of subroutines. Also contains programs associated with the assembler and C compiler. The subroutines perform a wide variety of functions and are accessible by all system software.
tmp	Used for temporary files.
usr	This is where the user's file system is mounted onto the file structure.

Figure: The Hierarchical File System



There may be other subdirectories, but those listed are a standard part of the UNIX software. The functions they perform are necessary for the operation of the system. Even though the file system may be reorganized, the directories listed must exist somewhere in the file system. For example, there must be a directory to contain special files. Some of the features of the file structure are:

- Simple and consistent naming conventions; file names can be fully qualified or relative to any directory in the file system hierarchy.
- Automatic file space allocation and deallocation that is invisible to users.
- A complete set of flexible directory and file protection modes that allows all combinations of read, write, and execute access, independently for the owner of each file or directory, for a group of users (such as all members of a project), and for all other users. The file protection modes can be set dynamically.
- Facilities for creating, accessing, moving, and processing files, directories, or sets of these in a simple, uniform, and natural way.
- Each physical input/output device from interactive terminals to main memory is treated like a file, allowing uniform file and device input and output.
- Mountable and unmountable file systems and volumes.
- File linking across directories.

4.0 Programming

Besides the inherent programming capability of the shell, the operating system will support many programming languages in common use. Some of these – C, Assembler, and Snobol to be specific – are standard. Others such as Basic, Cobol, and Pascal are add-on features. A C-language compiler is included as a standard part of the UNIX system software. Thus, users can write and compiler their own C-language programs.

The user interface to the file system is extremely convenient from a programming stand-point. The lowest possible interface level is designed to eliminate distinctions between the various devices and files and between direct and sequential access. No large "access method" routines are required to insulate the programmer from the system calls. Another convenience is that there are no complicated "control blocks" maintained or required by the file system or other system calls.

The programming environment is enhanced by the availability of many support tools. These support tools are either standard commands or are add-on packages as listed in following pages. For example, the Source Code Control System and the MAKE command both help in maintaining source code. Other languages such as LEX, YACC, and AWK make it easier for the user to create programs.

5.0 Basic Software

The basic software consists of user commands, programs, and utilities that provide all the facilities needed to use the operating system. The basic commands provide users with system access control, the ability to manipulate files and directories, system status information, inter-user communication, and various other utility functions. All of the commands in the following lists are a standard part of the UNIX software.

5.1 Operating System

/unix — This is the basic resident code, known as the kernel, which everything else depends upon. The kernel executes the system calls, maintains the file system, and manages the system's resources; it contains device drivers, I/O buffers, and other system information. Further capabilities include:
- Automatically-supported reentrant code
- Separation of instruction and data spaces (machine dependent)
- Timer-interrupt sampling and interprocess monitoring for debugging and measurement

5.2 User Access Control

LOGIN — Identifies and signs on a new user:
- Adapts to characteristics of terminal
- Verifies password and establishes user's individual and group (project) identity
- Establishes working directory
- Publishes message of the day
- Announces presence of mail
- Lists unseen news items
- Executes an optional user-specified profile
- Starts command interpreter (shell) or other user-specified program

PASSWD — Changes a password:
- User can change own password
- Passwords are kept encrypted for security

SU — Assume the permissions and privileges of another user or root (super-user) provided the proper password is supplied.

NEWGRP — Changes working group (project ID). This provides access with protection for groups of related users.

STTY Sets up options for optimal control of a terminal. In so far as they are deducible from the input, these options are set automatically by LOGIN:
- Speed
- Parity
- Mapping of upper-case characters to lower case
- Carriage-return plus line-feed versus new-line
- Interpretation of tab characters
- Delays for tab, new-line, and carriage-return characters
- Raw versus edited input

TABS Sets terminal's hardware tab stops. The TABS command allows several standard formats. Also, it is compatible with many terminal types.

5.3 Manipulation of Files and Directories

ED Interactive line-oriented text editor. The ED command can:
- Randomly access all lines of a file
- Find lines by number or pattern (regular expressions). Patterns can include specified characters, "don't card" characters, choices among characters, (specified numbers of) repetitions of these constructs, beginning of line, end of line.
- Add, delete, change, copy, or move lines
- Permute contents of a line
- Replace one or more instances of a pattern within a line
- Combine or split lines
- Combine or split files
- Do any of above operations on every line (in a given range) that matches a pattern
- Escape to the shell (UNIX system command interpreter) during editing

EX The base program of a family of editors including VI. It has all the features of ED and implements the line-oriented commands for VI. There are three modes to EX:

command The initial mode; the line-oriented portion of EX.

insert Arbitrary text can be entered anywhere in the file.

visual Entered with the VI command; the display editing portion of EX.

SED A stream (one-pass) editor with features similar to those of ED.

VI A screen-oriented display editor. All the features of the ED and EX editors are available in VI. There are many other features available, such as:
- cursor positions itself at the actual position within the file
- text can be inserted and deleted at any point on a line
- full cursor control using single keystroke commands
- windows of text can be scrolled forward or backward
- movement forward and backward through the text by words, sentences, paragraphs, sections, etc.
- macros and shorthand versions of most commands
- automatic breaking of long lines
- automatic indent option when creating text
- recovery of up to 9 blocks of lost text
- buffers to temporarily hold pieces of text to be moved and copied to various places
- several files can be edited simultaneously
- portions of the buffer can be filtered through standard UNIX system commands
- usable on a wide variety of terminals including CRT, hardcopy, and other undefined terminals
- most commands can be given repetition factors

CAT Concatenates one or more files and lists them on standard output.

PR Prints files with title, date, and page number on every page:
- variable page length
- multi-column output
- parallel column merge of several files

TAIL Prints the ending of a file. The user can specify how many lines back in the file to start.

SPLIT Splits a large file into more manageable pieces. Splitting is controlled by the number of lines to be put in each output file. Another command similar to SPLIT, CSPLIT, controls splitting by context.

PACK Compresses a file using Huffman codes on a byte-by-byte basis. Files are typically reduced 60-75% of their original size. The new file is renamed to indicate it is a packed version. The UNPACK command restores the file.

DD Physical file format translator, for exchanging data with non-UNIX systems. DD is also good at making physical copies of a file system.

OD Dumps any file:
- output options include: octal or decimal by words, octal by bytes, ASCII, operation codes, hexadecimal, or any combination thereof
- range of dumping is controllable

CP Copies one file to another or many files to a directory.

CPIO Copies a sub-tree of the file system (directories, links, and all) to another place in the file system (often used with the FIND command). The CPIO command can also copy a sub-tree onto a tape and later recreate it from tape.

LN Links another name (alias) to an existing file.

MV Moves one or more files. The MV command is usually used for renaming files or directories.

RM Removes one or more files. If any names are linked to the file, only the name being removed goes away.

CHMOD Change access permissions on a file(s). Executable by the owner of the file(s) or by the super-user.

CHOWN Changes owner of a file(s). Only the owner of a file can do this.

MKDIR Makes one or more new directories.

RMDIR Removes one or more (empty directories).

CD Changes working (that is, current) directory.

FIND Searches the directory hierarchy for, and performs specified commands on, every file that meets given criteria (starting at any directory node):
- filename matches a given pattern
- modification date in given range
- date of last use in given range
- given permissions
- given owner
- given special file characteristics
- any logical combination of the above

5.4 Execution of Programs

SH The shell, or command language interpreter, understands a set of constructs which constitute a full programming language. The shell allows a user or a command procedure to:
- supply arguments to and run any executable program
- redirect standard input, standard output, and standard error files
- "Pipe" the output of one process directly to the input of another process with simultaneous execution
- compose compound commands using:
  - if...then...else,
  - case switches,
  - while loops,
  - for loops over lists,
  - break, continue, and exit,
  - parentheses for grouping
- initiate background processes
- perform shell procedures (that is, command scripts with substitute arguments)
- construct argument lists from all file names matching specified patterns
- take user-specified action on traps and interrupts
- specify a search path for finding commands
- automatically create a user-specific environment (upon log in)
- optionally announce presence of mail as it arrives
- provide variables and parameters with default settings

RSH — Restricts a user to a subset of the UNIX system commands (restricted shell). The system administrator may construct different levels of restriction.

TEST — Tests argument values in shell conditional constructs:
- string comparison
- file nature and accessibility
- boolean combinations of the above

EXPR — Calculates command arguments input in the form of expressions. The EXPR command can perform:
- integer arithmetic
- pattern matching
- conditional side-effect calculations (similar to the TEST command) can be used for conditional side-effect

TEE — Passes data between processes (like a "pipe"), but also diverts copies into one or more files.

ECHO — Prints its arguments on the standard output. The ECHO command is useful for diagnostics or prompts in shell procedures, or for inserting data into a "pipe".

SLEEP — Suspends execution of a process for a specified time.

WAIT — Waits for termination of a specific or all processes that are running in the background.

NOHUP — Runs a command immune to interruption from "hanging up" the terminal.

NICE — Runs a command at low (or high) priority.

KILL — Terminates the named process(es).

CRON — Performs actions at specified times (usually is run by the initialization process using instructions stored in a "job" file):
- actions are arbitrary shell procedures or executable programs
- times are conjunctions of month, day of month, day of week, hour, and minute. Ranges are specifiable for each.

DOC — An on-line version of the UNIX System User Reference Manual. Will format output to print on many types of terminals and printers.

5.5 Status Inquires

LS — Lists the names of one, several, or all files in one or more directories.
- alphabetic or chronological sorting, up or down
- optional information: size, owner, group, date last modified, date last accessed, permissions

FILE — Tries to determine what kind of information is in a file by consulting the file system index and by reading the file itself.

SUM — Computes and prints the checksum of a file.

WHAT — Prints informational lines found in files usually inserted by SCCS.

DATE — Prints current date and time. DATE has considerable knowledge of calendrical and horologic peculiarities and can be used to set the UNIX operating system's idea of date and time. (As yet, cannot cope with Daylight Saving Time in the Southern Hemisphere.)

DF — Reports the amount of free space in a file system.

DU — Prints a summary of the total space occupied by all files in a hierarchy.

TTY — Prints the "name" of the user's terminal (that is, the name of the port to which the user's terminal is connected).

WHO — WHO Tells which users are logged onto the system.
- lists logged-in users, their ports, and the time when they logged in
- provides optional history of all log ins and log outs
- optionally indicates boot time, current run level, and other system information
- tells the user his login name

PS — Reports on active processes:
- lists the user's processes or everybody's processes
- tells what commands are being executed at the moment
- provides optional status information: state and scheduling information, priority, attached terminal, what the process is waiting for, its size, etc.

ACCTCOM Reports a chronological history of all processes that have terminated. Information includes:
- times and sizes of user and system processes
- start and end real times
- owner and terminal line associated with each process
- system exit status

PWD Prints the name of the user's working (that is, current) directory.

RJESTAT Reports on the status of the Remote Job Entry (RJE) interface(s) to an IBM host machine.

UUSTAT Reports status of files queued for transmission to other UNIX systems (both current and past requests) via UUCP command. Also provides an option to cancel a job.

LPSTAT Reports current status of the lp spooling system. There are various options, such as:
- report status of certain jobs
- specify certain user's jobs
- print status of the scheduler
- indicate status of all jobs on a particular printer

5.6 Inter-User Communication

MAIL Mails a message to one or more users. Also used to read and display of incoming mail. The presence of mail is announced by the LOGIN command.

NEWS Prints out current general information and announcement files.

CALENDAR Automatically checks a "calendar" file for entries with tomorrow's date and sends them to MAIL (that is, a reminder service).

WRITE Establishes direct, interactive terminal-to-terminal communication with another user.

WALL Broadcasts a message to all users who are logged in.

MESG Inhibits or permits receipt of messages from WRITE and WALL.

5.7 Utilities

CXREF Makes a cross-reference listing of a set of C source files. The listing contains all symbols in each file (separately or, optionally, in combination). An asterisk appears before a symbol's declaration.

SORT Merges and/or sorts ASCII files line-by-line:
- in ascending or descending order
- lexicographically or on numeric key
- on multiple keys located by delimiters or by position
- in dictionary order, with upper-case and lower-case characters folded together

UNIQ Deletes successive duplicate lines in a file.
- prints lines that were originally unique, duplicated, or both
- can give redundancy count for each line

TR Performs character translation according to an arbitrary code.
- can "squeeze out" repetitions of selected characters
- can delete selected characters

DIFF Reports line changed, additions, and deletions necessary to bring two files into agreement.

COMM Identifies common lines in two sorted files. Output in up to 3 columns shows lines present in first file only, present in second file only, and/or present in both.

CMP Compares two files and reports disagreeing bytes.

GREP Prints all lines in one or more files that match a specified pattern. GREP patterns are similar to ED patterns.
- can print all lines that fail to match
- can print count of "hits"

CUT Lets the user "cut out" certain columns from a table or file by field number.

PASTE Puts together columns side-by-side. Often used with GREP and CUT to reorganize data in the given files.

WC Counts lines and "words" (strings separated by blanks or tab characters) in a file.

TIME Runs a command and provides timing information on it.

5.8 Normal Daily Administration

MOUNT — Attaches a device containing a file system to the tree of directories.

UMOUNT — Removes the file system contained on a device from the tree of directories. Protects against removing a busy device.

MKFS — Makes a new file system on a device.

MKNOD — Makes a file system entry for a special file. Special files are physical devices, virtual devices, physical memory, etc.

FSCK — Used to check the consistency of file systems and directories and make interactive repairs.
- print statistics: number of files, space used, free space
- report duplicate use of space
- retrieve lost space
- report inaccessible files
- check consistency of directories
- reorganize free disk space for maximum operating efficiency

SYNC — Forces all outstanding I/O on the system to completion. Normally used prior to shutting down the system.

CONFIG — Tailors device-dependent system code to a specific hardware configuration.

CRASH — Prints out tables and structures in the operating system. CRASH is useful for examining operating system core dumps after a system "crash".

5.9 System Monitoring Facilities

Accounting — The process accounting package covers time accounting, command usage, command frequency, disk utilization, and line usage. All of these are summarized by user and by command on a daily, monthly, and fiscal basis. The system lends itself to local needs and modification.

Error logging — The UNIX operating system incorporates continuous logging hardware error detection and reporting.

SAR — The System Activity Report package is a body of programs for sampling the behavior of the operating system. The sampling consists of several time counters, I/O activity counters, context-switching counters, system-call counters, and file-access counters. Reports can be generated on a daily basis or as desired.

Profiler — The Profiler is another group of commands for studying the activity of the operating system. It reports the percentage of time that the operating system spends on user tasks, on system functions, and in being idle.

6.0 Releases:

The performance and features of the UNIX System V Release 1.0 shell have been improved in Release 2.0 (3.0) with various features such as:
- functions (saved parsed shell scripts)
- command hashing and faster directory reads
- automatic lowering of background process priority
- more built-in commands
- greater flexibility by programming
- faster debugging
- improvements for speed-up program compilation and execution
- Remote File System (RFS) and Network File System (NFS) support.

The "UNIX SYSTEM Release 2.0 (3.0) for 68K" is also available from FORCE Computers in conjunction with the microFORCE and FOCUS 32 system configurations.

7.0 Application Programs
The following application programs are implemented on the FORCE hardware running under UNIX:

SYS68K/UNIX*-PAS020 Part No. 150006	Pascal compiler for UNIX* including documentation
SYS68K/AGC-1GKSGRALU2B1 Part No. 160001	GKS Level 2b implemented under UNIX* for the Graphic Controller Board SYS68K/AGC-1
SYS68K/AGC-2GKSGRALU2B2 Part No. 160003	GKS Level 2b implemented under UNIX for the Graphic Controller Board SYS68K/AGC-2

System 68000 VME
SYS68K/GKSGRAL
Graphical Kernel System

1. General Information

The Graphical Kernel System (GKS) has been developed over a long process since 1976 and has evolved as an international standard. More than 100 scientists from all over the world invested probably more than 50 man years to make GKS the consistent and complete graphics standard it is today.

2. GKSGRAL Introduction

GKSGRAL is a full implementation of the Graphical Kernel System GKS, which is both an international ISO standard (ISO DIS 7942) /1/ and is accepted for several national standards, e.g., DIN, ANSI, BSI, AFNOR, NNI.
This first international standard offers the capability to create and represent two-dimensional pictures, handle input from graphical workstations, structure and manipulate pictures, and also to store and retrieve the pictures.
The main objectives of the standard were:

- Portability of application programs between different GKS installations on varying computing environments
- Unifying the concepts of graphics programming, therefore easing the programmer's training
- Guiding hardware and system manufacturers when providing graphics capabilities

2.1 The GKSGRAL System Structure

The GKSGRAL implementation is a modular subroutine package with a well-defined internal structure and a set of interfaces that can be used for many configuration possibilities.
The Graphical Kernel System (GKS) provides a set of functions for computer graphics programming. GKS is a basic graphics system that can be used by the majority of applications that produce computer generated two-dimensional pictures on line graphics or raster graphics output devices. The main reasons for introducing the GKS standard are:

a. To allow application programs involving graphics to be easily portable between different installations;
b. To aid the understanding and use of graphics methods by application programs;
c. To serve manufacturers of graphics equipment as a guideline in providing useful combinations of graphics capabilities in a device.

In order to reach these objectives, the GKS design was based on the following requirements:

a. GKS shall include all the capabilities that are essential for the whole spectrum of graphics, from simple passive output to highly interactive applications;
b. The whole range of graphics devices, including vector and raster devices, microfilm recorders, storage tube displays, refresh displays and colour displays shall be controllable by GKS in a uniform way.
c. GKS shall provide all the capabilities required by a majority of applications without becoming unduly large.

The GKSGRAL system can be subdivided into three layers:

- The GKSGRAL kernel:
  a. Provides the standard FORTRAN interface to application programs. Other language interfaces as well as communication interfaces in distributed systems sit on top of the FORTRAN interface.
  b. Keeps the GKS state list, handles most of the GKS error conditions and distributes commands to the single workstations.
  c. Interprets the GKS metafile input, by associating, copying and inserting segments out of the segment storage workstation.
  d. Redraws segments on workstations which have no own segment storage or cannot fulfill all of the GKS dynamic modifications functions.
- The GKSGRAL Workstation Layer:
  The main task of the GKSGRAL workstation layer is to map the logical GKS workstation functions onto the existing peripheral device functions. For real graphical devices, this is a set of graphics commands. To ease the writing of new graphics device drivers, we separated the device-specific command coding from algorithmic computations. The latter ones, e.g. coordinate transformations, clipping and high quality text, are performed within the workstation layer, the coding of a coordinate into characters is done within a device drive.
  For metafiles, the workstation layer maps the GKS functions to standard codings on sequential files with fixed record lengths and vice versa. For the WISS, an optimized portable solution is implemented which stores and retrieves GKS picture descriptions (with the help of a memory resident working set and a direct access file).
- The GKSGRAL Device Driver Layer:
  As already mentioned, GKSGRAL device drivers are intended to perform the device specific command and data coding and to communicate with the operator via the hardware. All device drivers must fulfill a certain set of functions and may contain an optional set of functions. The minimal required set of functions comprises the GKS output primitives in device coordinates, the according direct attributes and a set of INQUIRY functions.

2.2 GKSGRAL Interface

The GKSGRAL system provides a set of interfaces which either correspond to certain ISO standards or are defined by GTS/GRAL in order to support well-defined exchangeable subsystems and system components.

These interfaces are:
- the language interfaces
- the metafile interfaces
- the graphics device interface
- symbol interfaces

2.3 GKSGRAL Input

The input part of GKSGRAL is divided into three modules above the device interface and one module below it. The three modules above are:

a. The Request Input Module:
This module comprises the INITIALIZE, the SET MODE, the corresponding INQUIRE and the REQUEST functions. These functions perform the error handling, data conversions such as unpacking the data record, string into integer con version, etc. and the simulation of non-supported logical input devices like calculating a segment name from a position for a PICK device, or transforming points from DC into WC for LOCATOR and STROKE devices. All data is passed over GKDDLK to the device drivers.

b. The Sample Input Module:
This module only contains the SAMPLE functions. Error checking is performed, the input data is sampled via the device interface and transformed (or mapped) to the world coordinate level.

c. The Event Input Module:
This module implements the GET function, the AWAIT and FLUSH functions and one INQUIRE function. It also contains the current event report. The event queue is kept in the device input handler. When calling the AWAIT function, the DCV event reports are acquired via the device interface and transformed (or mapped) to the world coordinate level, and stored as current event report.

d. The Device Input Handler Module:
This set of routines is situated below the GKDDLK interface. It keeps the current logical DC input device measure values and the DC input queue (one for all connected device). It is also responsible for mapping the physical input values into logical DC values and for performing the echo, if this is not done by the input handler of the physical input devices.

The input handler can be realized in three ways, depending on the operating system facilities:

1. It can be called asynchronously by an interrupt routine
2. It can run as a separate task together with the device drivers
3. It performs only when an AWAIT function or a REQUEST function is pending, i.e., only when the application program waits for any input. This realization allows for the handling of several input devices at the same time (if the application program enables a number of input devices and waits for the input from any one of these). However, it does not implement true asynchronous input handling, i.e., input devices can only be handled and echo is only performed when the application program calls REQUEST or AWAIT – EVENT functions.

3. The Implemented GKSGRAL

The GKSGRAL Level 2b is implemented on the FORCE COMPUTERS Systems.
This level 2b contains the following features:
- Segmentation including segment-handling and storing on separate memory areas
- Update control
- Multiple workstations support
- Metafile support
- Duplication and transfer to other workstations
- Request Input including Pick

4. Supporting Operating Systems

The GKSGRAL level 2b is implemented under the UNIX* 5.2 and under the PDOS* operating system. It is available for all system configurations of FORCE COMPUTERS. The user interface and the internal structure of GKS are remaining the same and therefore the GKS standard is fully protected.

4.1 GKSGRAL Implementation for UNIX* 5.2

Minimum requirements:
- 1-2 free slots
- 80 Mbyte Winchester
- 4 Mbyte system memory
- UNIX* operating system Version 5.2 or later 68010 or 68020 based
- Fortran 77 and C-compiler
- Language supported:
  - Fortran 77
  - C

4.2 GKSGRAL Implementation for PDOS*

Minimum requirements:
- 1-2 free slots
- 1 Mbyte available memory
- 20 Mbyte Winchester
- PDOS* operating system, Version 3.2a or later 68000/68010/68020 based
- PDOS* Fortran 77 Compiler, Version 3.2a or later
- Language supported:
  - Fortran 77

*UNIX is a Trademark of Bell Laboratories
*PDOS is a Trademark of Eyring Research Inst.

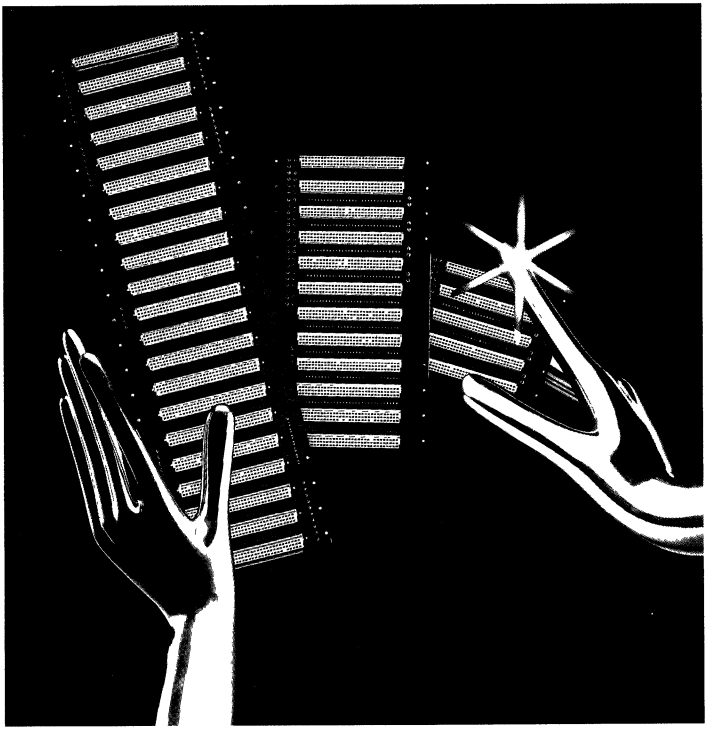
5. Supported Hardware

The graphic boards which are supported under GKSGRAL are the SYS68K/AGC-1 and the SYS68K/AGC-2. For both VMEbus based graphic boards a driver is developed and all GKSGRAL functions are supported by these drivers. Additionally, the input functions for mouse, keyboard or tableau are implemented on serial I/O boards of FORCE COMPUTERS. Therefore a graphic workstation building with input and output devices is possible.

Ordering Information

SYS68K/GKSGRAL-U2B1 Part No. 160001	GKS level 2b under UNIX* forAGC-1 including documentation
SYS68K/GKSGRAL-P2B1 Part No. 160000	GKS level 2b under PDOS* for AGC-1 including documentation
SYS68K/GKSGRAL-U2B2 Part No. 160003	GKS level 2b under UNIX* for AGC-2 including documentation
SYS68K/GKSGRAL-P2B2 Part No. 160002	GKS level 2b under PDOS* for AGC-2 including documentation
SYS68K/GKSGRAL-2B1/UM Part No. 800111	GKS User's Manual

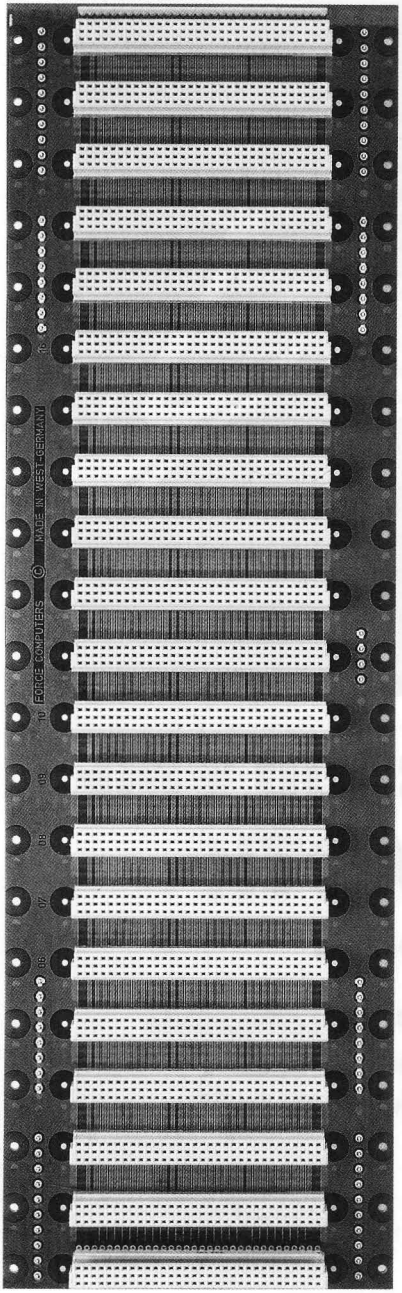
Accessories

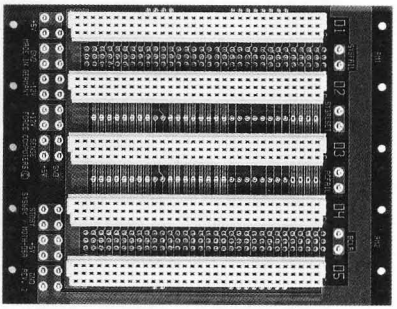


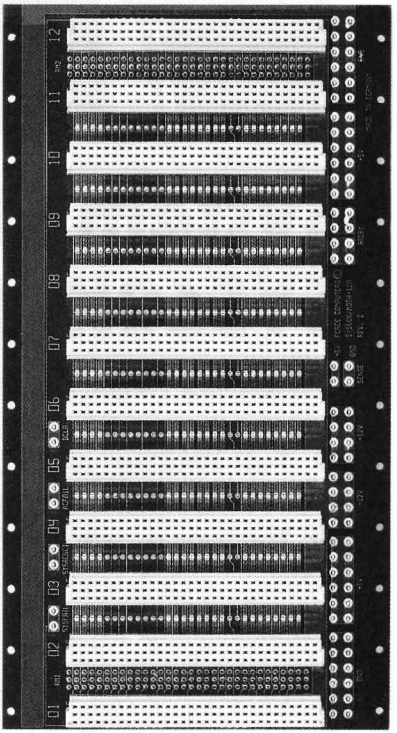
System 68000 VME SYS68K/MOTH

VMEbus Motherboards

- **Full VMEbus Rev.C/P1014 compatible**
- **J1 and J2 motherboards available**
- **Various number of slots 5 up to 21**


FORGE COMPUTERS
MADE IN WEST-GERMANY





General Information
All Motherboards of the SYS68K/MOTH family are VMEbus (IEEE 1014 standard) compatible. The transfer speed is 20 MHz (minimum) and 5, 9, 12, 20 or 21 VME modules can be plugged in via the 96 pin connectors (DIN 41612C).
Two different backplane versions are defined in the IEEE 1014 standard specification, the J1 and J2 backplane. The J1 backplane offers operations with 24 address and 16 data lines which are primarily used for 16 bit processors. The J2 backplane offers an extension for the 32 bit processors because it adds 8 address and 16 data lines to fully support 32 bit address and data together with the J1 backplane. It also provides additionally power driving capabilities for 16 bit environments (i.e. SYS68K/DRAM-E3).
A 5 slot backplane (SYS68K/MOTH-05A), a 12 slot backplane (SYS68K/MOTH-12A) and a 21 slot J2 backplane (SYS68K/MOTH-E21A) are shown on the previous page.

Board Assembly
The SYS68K/MOTH Motherboard is produced with gold plated fast-on connectors for power connections. Additionally, the Motherboard (J1 backplane) contains 4 connectors for the VMEbus, IEEE 1014 bus exception signals:
BERR*
ACFAIL*
SYSFAIL* and
SYSRESET*
Each signal line is terminated according to the specification with 330/470 Ohm resistors to guarantee the high level voltage of 2.94V. The J1 backplane contains 6 resistor networks (B2 pins) and the J2 backplane contains 2 resistor networks for termination.
All IACK and Bus-Grant daisy chain signals on the J1 backplane can be jumpered directly to the next slot to establish the daisy chain. All jumpers for the daisy chain are included.

Electrical Environment
Power is supplied to the backplanes (J1 and J2) through gold plated fast-on connectors.
A supply current of maximum 25A per connector may be drawn.
For a reduction of the contact resistance, the Motherboard contains more power connections than needed only for the maximum allowed value (4.5A per slot). To connect the sense signals of the power supply to the Motherboard, 2 sense signals (+5V SENSE and GND SENSE) are installed in the middle of each backplane. The following table lists the number of power points for each supply voltage for each Motherboard.

Type		No. of Slots	No. of Connectors				
			+5V	+12V	−12V	+5VSTDBY	GND
MOTH-05A	J1	5	4	2	2	2	4
MOTH-09A	J1	9	8	2	2	2	8
MOTH-12A	J1	12	12	4	4	4	12
MOTH-20A	J1	20	16	8	8	4	20
MOTH-21A	J1	21	16	8	8	4	20
MOTH-E05A	J2	5	4	–	–	–	4
MOTH-E09A	J2	9	8	–	–	–	8
MOTH-E12A	J2	12	12	–	–	–	12
MOTH-E20A	J2	20	16	–	–	–	20
MOTH-E21A	J2	21	16	–	–	–	20

Mechanical Environment
All of the mechanics are VMEbus/IEEE 1014 standard compatible and each of the J1 backplanes can be used together with each of the J2 backplanes.
The J2 backplanes have wire wrap type connector pins on the backside to interconnect to a user supplied I/O or to a VMXbus backplane.

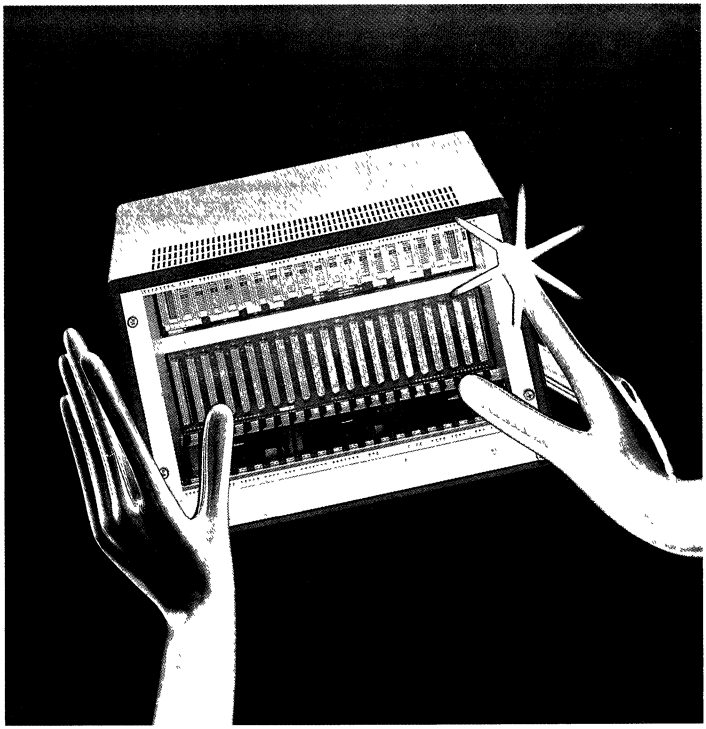
Dimensions	Length (mm)	Length (inch)
J1/J2 5 slot	100	39
J1/J2 9 slot	181	71
J1/J2 12 slot	242	95
J1/J2 20 slot	405	159
J1/J2 21 slot	425	167

Specification

Backplane Wiring	Utilises all specified signal and power supply lines of the VMEbus specification
Construction	All connectors are supplied in press fit technique J1 Backplane 6 layers J2 Backplane 2 layers
Connectors	DIN 41612C female connector Gold plated Fast-On connectors for power supply connection and exception signals (4)
Daisy Chain	All daisy chain signals can be jumpered from the backside of the Motherboard
Bus Terminators	All specified signal lines have termination networks at both ends of the Motherboards (330 Ohm / 470 Ohm)
Power Requirements	5.5W (typ) 5V / 1.1 A (typ) J1 Backplane 5.5W (typ) 5V / 0.34 A (typ) J2 Backplane
Dimensions	Both Motherboard types are equipped to be mounted in a standard 19" card cage
Temperature Range	Operating Temperature: 0 to 70 deg. C Storage Temperature: −25 to 90 deg. C
Humidity	Operating Humidity: 0 to 95 % (non-condensing)

Ordering Information
All Motherboards are shipped together with a hardware user's manual describing the usage of the board in detail and the daisy chain jumpers (J1 backplane only).

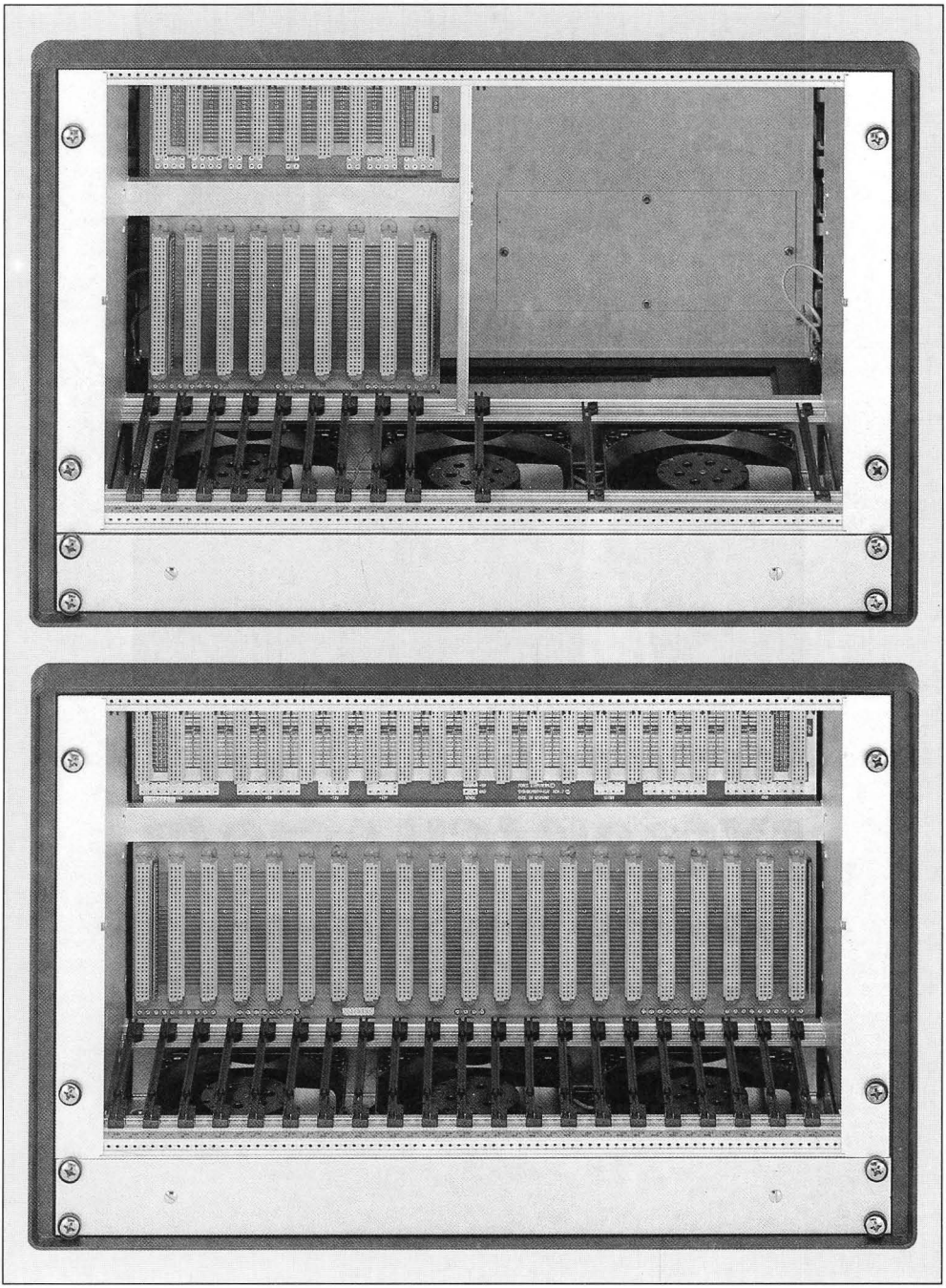
SYS68K/MOTH-05A Part No. 500005	5 slot J1 Motherboard
SYS68K/MOTH-09A Part No. 500011	9 slot J1 Motherboard
SYS68K/MOTH-12A Part No. 500006	12 slot J1 Motherboard
SYS68K/MOTH-20A Part No. 500013	20 slot J1 Motherboard
SYS68K/MOTH-21A Part No. 500007	21 slot J1 Motherboard
SYS68K/MOTH-E05A Part No. 500008	5 slot J2 Motherboard
SYS68K/MOTH-E09A Part No. 500012	9 slot J2 Motherboard
SYS68K/MOTH-E12A Part No. 500009	12 slot J2 Motherboard
SYS68K/MOTH-E20A Part No. 500014	20 slot J2 Motherboard
SYS68K/MOTH-E21A Part No. 500010	21 slot J2 Motherboard
SYS68K/MOTH-A/HUM Part No. 800072	Hardware User's Manual for all backplanes



System 68000 VME
SYS68K/CHAS19/7

Industrial VMEbus Enclosures

- 19 inch chassis including card cage
- Low noise fans underneath of the card cage
- 9 or 21 slot P1 VMEbus motherboard
- 9 or 21 slot P1 and P2 VMEbus motherboard



1. General Information

The SYS68K/CHAS19 is an industrial 19" rack of steel-reinforced aluminium, with a baked lacquer exterior finish. It features side grips for easy transportation and has mains switch, power connector and cooling fans already integrated.

2. Features

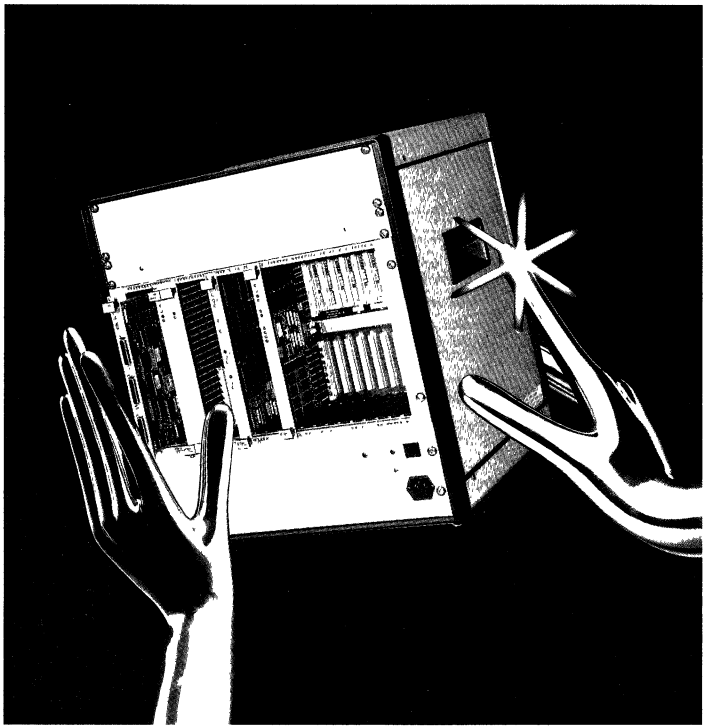
- The SYS68K/CHAS19-09/7HE contains a 9-slot motherboard designed to interconnect VME modules (see photo on opposite page and data sheet for the SYS68K/MOTH series).
- The SYS68K/CHAS19-21/7HE contains a 21-slot motherboard for the interconnection of VME modules.
- The SYS68K/CHAS19-09E/7HE and the SYS68K/CHAS19-21E/7HE provide an additional P2 motherboard for the VME 32-bit expansion.
- Three PAPST 4800/4850 standard fans or equivalent, mains switch, power connector and interface cables are always integrated.

3. Construction

The SYS68K/CHAS19 is constructed of two cast aluminium sections and four aluminium connecting supports.
The interconnecting formed elements and locking screws provide good stability. Special grounding clips are used when attaching the sheet metal panels to the aluminium frame. Central grounding can be in various locations, preferably on the backside of the enclosure.

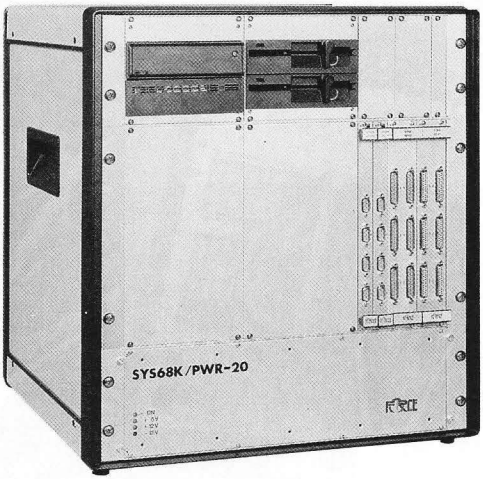
Ordering Information

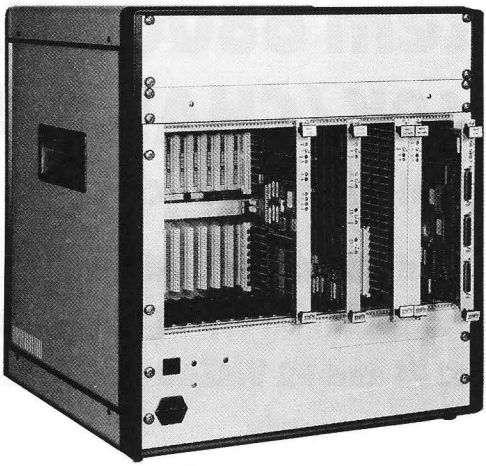
SYS68K/CHAS19-09/7HE Part No. 610100	7HE Chassis with 9-slot VME motherboard including fans, mains switch, cabling.
SYS68K/CHAS19-21/7HE Part No. 610104	7HE Chassis with 21-slot VME motherboard including fans, mains switch, cabling.
SYS68K/CHAS19-09E/7HE Part No. 610101	7HE Chassis with 9-slot VME motherboard and 32-bit expansion motherboard, including fans, mains switch, cabling.
SYS68K/CHAS19-21E/7HE Part No. 610105	7HE Chassis with 21-slot VME motherboard and 32-bit expansion motherboard, including fans, mains switch, cabling.



System 68000 VME
SYS68K/CHAS-19/12
Industrial VMEbus Enclosure

- 19" chassis, including card cage
- Low noise fans on top of the card cage
- 21-slot P1 and P2 VMEbus motherboard
- 90A power supply
- Mounting equipment for up to 4 drives


SYS68K/PWR-20



1.0 General Information

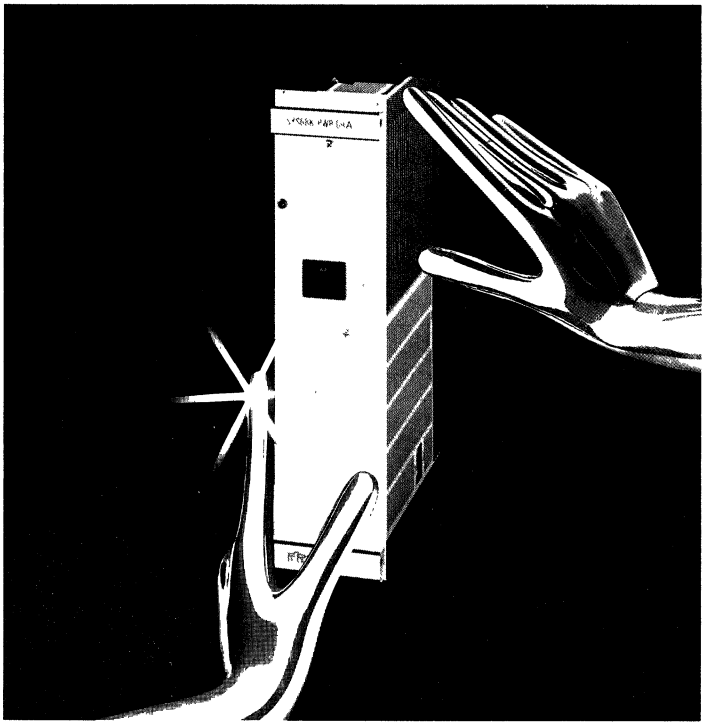
The SYS68K/CHAS-19/12 is an industrial 19" rack of steel-reinforced aluminium. It features a 19" 6HE rack, including a J1 and J2 VMEbus motherboard as well as cooling fans on top of the 12HE enclosure. A 90A power supply is installed in order to support the 21 VMEbus slots, as well as the up to 4 mountable Winchester/floppy disk drives.

2.0 Features

- 21-slot VMEbus backplane (J1 and J2)
- 90A at +5V power supply, mounted in a 3HE card cage (+12V : 20A, 12V : 5A)
- Mounting places for up to 4 Winchester/floppy drives in a 3HE enclosure
- 3 quiet fans on top of the card cage for the VMEbus boards
- All the cabling needed for the interconnection of the power supply to the VMEbus motherboards as well as to the Winchester/floppy drives is included
- Special grounding clips are used when attaching the sheet metal panels to the aluminium frame

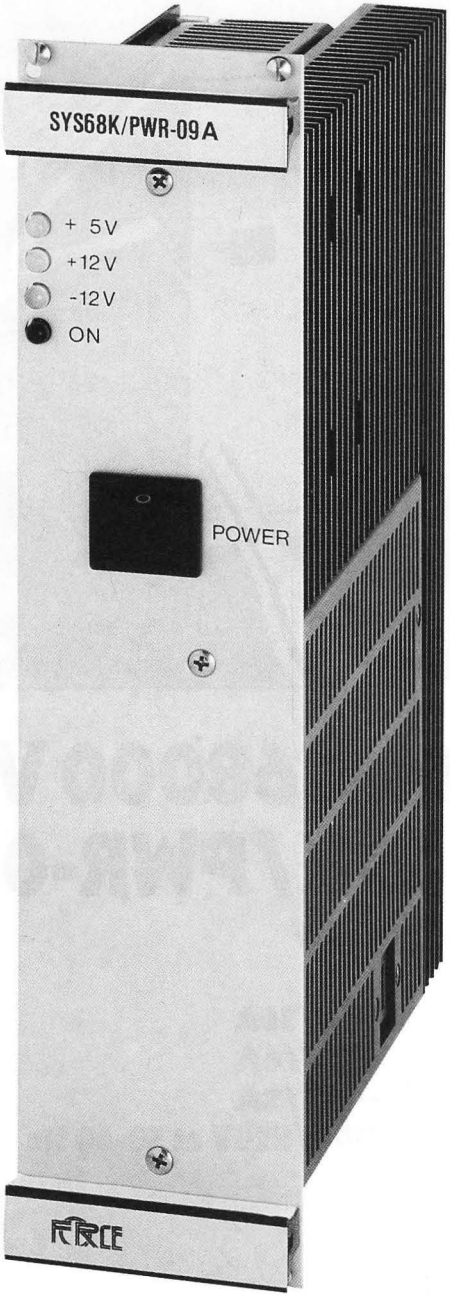
3.0 Ordering Information

SYS68K/CHAS-19/12 Part No. 610190	12HE chassis with J1 and J2 VMEbus motherboard (21 slots), including fans, main switch, cabling and 90A power supply.



System 68000 VME
SYS68K/PWR-09A
Power Supply

- **Outputs** +5V/36A
  +12V/6A
  −12V/2A
- **Inputs** 110V/220V at 50-60 Hz


SYS68K/PWR-09A
+ 5V
+12V
-12V
ON
POWER
FORCE

General Description

The SYS68K/PWR-09A is a high performance power supply especially designed for VMEbus based systems. Easy installation is provided through two DIN 41612 connectors and the cable subassembly which allows the direct connection to a Floppy/Winchester combination and a VMEbus motherboard.
A main power switch with control LED's for each supply voltage (+5V, +12V, −12V) is available on the front panel. The power supply can be used with 110V/220V at 50 to 60 Hz.

Features

- High reliability
- VMEbus Spec compatible SYSRESET and ACFAIL signal
- Compact dimensions
- Outputs: +5V/36A
  +12V/6A
  −12V/2A
- Inputs 110V/220V at 50−60 Hz.

Specifications

Input Voltage	UE = 110V/220V AC +/−10% user selectable via fuse
Input Frequency	f = 50−60 Hz
Input Current	220V AC: IE = 2.5A (typ) IE = 50A (max) input peak 110V AC: IE = 5A (typ) IE = 50A (max) input peak
Output Voltage	DC OUTPUT
	Nom. / Voltage Settl. Range / Current 50°C forced cooling
	+ 5V — 5...5.5V — 36A +12V — 12V — 6A −12V — 12V — 2A
Efficiency	>75% (5V)
Pard (periodic ripple)	<50mVpp (30 MHz bandwidth)
(random noise)	<30mVr.m.s (10 MHz) bandwidth)
Dynamic Behavior	For instantaneous load changes (dIo/dt = 0.5A/us) the transient recovery time to settle within 1.5% of output voltage: 2 ms for Io = 30% − 80% IA nominal For transient voltage changes (overshoot) which could exceed the regulation limits: 200mV for IA nom. = 30% − 80% or 80% − 30%
Regulation	for +/−10% main input variations +5V stat +/−1%
Turn-on Delay Time	<800 ms to reach load specification at 25 degree C
Turn-off Decay Time	>10 ms at nom. load and nom. mains
Output Protection	Full overload protection of all outputs short approx. 0,66 x IA nom. OVP (5V) approx. 1.3 x UA nom.
Specials	Power fail signal (TTL compatible), 5V Sense line
M.T.B.F.	80.000 operating hours at 25 degrees C
Cooling	Free convection or forced cooling (3 m/s)
Operating Temp.	0 to +50 degrees C
Storage Temp.	−25 to +85 degrees C
Relative Humidity	10% to 90% (non condensing)
Safety Class	Conforms to Class I VDE 0804
RFI	VDE 0871 class B
Connectors	two H15 DIN 41612
Dimensions	Full metal cassette 6HE/12TE, depth 210 mm/8.26 inch
Weight	3.0 kg

Ordering Information

SYS68K/PWR-09A Part No. 700008	Power Supply PWR-09A including User's Manual
SYS68K/PWR-09A/CA Part No. 700018	Cable Assembly for the PWR-09A
SYS68K/PWR-09A/UM Part No. 800060	User's Manual for SYS68K/PWR-09A

System 68000 VME
SYS68K/PWR-20
Power Supply

- **Outputs** +5V/90A
  +12V/20A
  −12V/5A
- **Inputs** 110V/220V at 50-60 Hz


SYS68K/PWR-20
+5V
+12V
-12V
ON
FORCE

General Description

The SYS68K/PWR-20 is a high performance primary switching power supply. This power supply is especially designed for high integrated systems and includes VMEbus compatible signals (SYSRESET and ACFAIL). An inhibit switch signal is also supported for the control of the output voltages. The control LED's for each supply voltage (+5V, +12V, −12V) are available on the front panel. The +12V, −12V connections, sense lines for +5V, +12V, GND and the VMEbus compatible signals are available on the backside via a H15 DIN 41812 connector. The +5V and GND load connections are placed on to the cupreous flange special connector for the 90A power.

Features

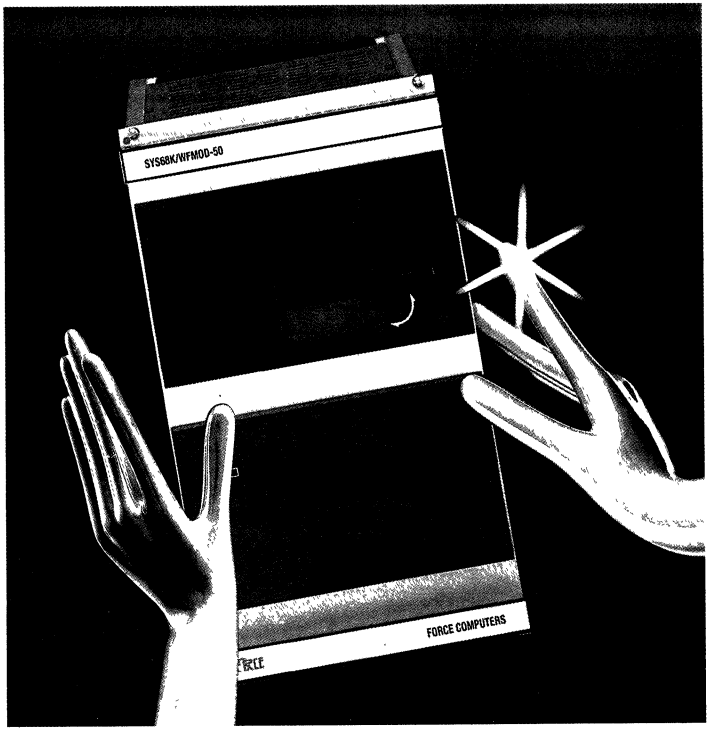
- High Reliability
- Outputs: + 5V/90A
  +12V/20A
  −12V/5A
- Compact Dimensions 3HE/84TE and 200 mm depth
- VMEbus compatible SYSRESET, ACFAIL signals
- Inputs: 110V/220V at 50-60Hz
- Fan is included on the Power Supply
- Sense Lines for +5V, +12V and GND
- Inhibit switch signal

Specifications

Input Voltage	UE = 110V AC +/−20% user selectable via fuse 220V AC +20%, −10% user selectable via fuse		
Input Frequency	f = 50−60 Hz		
Input Current	220V AC: IE = 8A (typ) IE = 100A (max) input peak 110V AC: IE = 16A (typ) IE = 100A (max) input peak		
Output Voltage		DC OUTPUT	
	Nom.	Voltage Settl. Range	Current 50DegC forced
	+ 5V	5...5.5V	90A
	+12V	12V	20A
	−12V	12V	5A
Efficiency	>75% (5V)		
Pard (periodic ripple)	<50mVpp (30 MHz bandwidth)		
(random noise)	<30mVr.m.s (10 MHz bandwidth)		
Dynamic Behaviour	For instantaneous load changes (dIo/dt = 0.5A/us) the transient recovery time to settle within 1.5% of output voltage: 2 ms for Io = 30% − 80% IA nominal For transient voltage changes (overshoot) which could exceed the regulation limits: 200mV for IA nom. = 30% − 80% or 80% − 30%		
Regulation	for +/−10% main input variations +5V stat +/−1%		
Turn-on Delay Time	<800ms to reach load specification at 25 degree C		
Turn-off Decay Time	>10ms at nom.load and nom.mains		
Output Protection	Full overload protection of all outputs Ishort approx. 0.66 x IA nom. OVP (5V) approx. 1.3 x UAnom.		
Specials	ACFAIL SYSRESET (TTL compatible), 5V, +12V and GND sense lines		
M.T.B.F.	50.000 operating hours at 25 degrees C		
Cooling	Free convection or forced cooling (3m/s)		
Operating Temp.	0 to +50 degrees C		
Storage Temp.	−25 to +85 degrees C		
Relative Humidity	10% to 90% (non condensing)		
Safety Class	Conforms to Class I VDE 0804		
RFI	VDE 0871 class B		
Connectors	One H15 DIN 41612 and two Cupreous Flanges		
Dimensions	Full metal cassette 3HE/84TE, depth 200 mm/7.86 inch		
Weight	10.5 kg		

Ordering Information

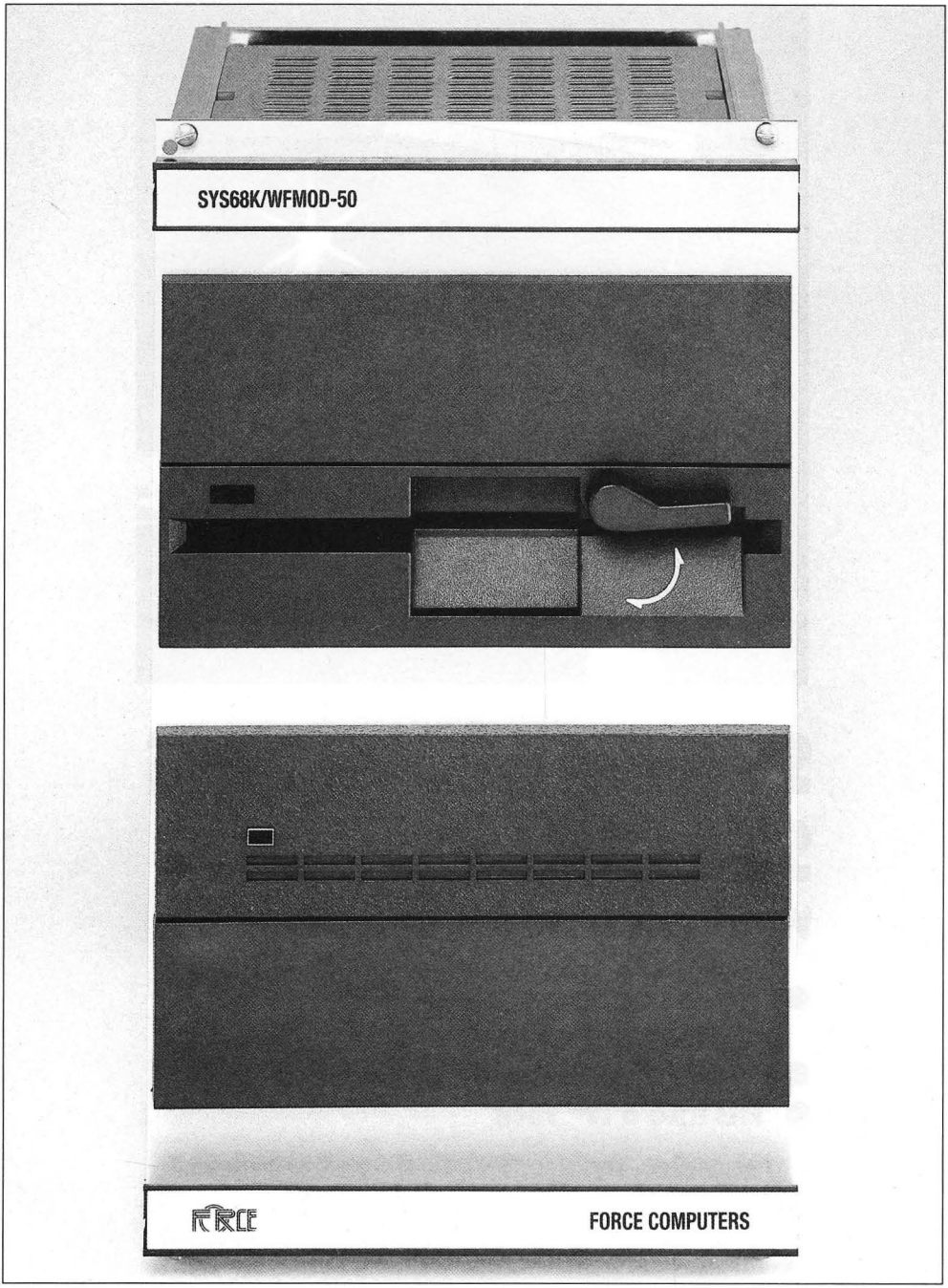
SYS68K/PWR-20 Part No. 700009	Power Supply SYS68K/PWR-20 including User's Manual
SYS68K/PWR-20/CA Part No. 700030	Cable Assembly for the PWR-20
SYS68K/PWR-20/UM Part No. 800070	User's Manual for SYS68K/PWR-20



System 68000 VME
SYS68K/WFMOD

Winchester/Floppy Drive Module

- **Three Configurations with 20/50/ 80/175 Mbyte Winchester**
- **Additional 1 Mbyte Floppy Drive**
- **Fits into a 19" rack**


SYS68K/WFMOD-50
FORCE COMPUTERS

General Description
The SYS68K/WFMOD is a universal mass memory module for VMEbus systems. Each of the three configurations contains a floppy and a Winchester drive with different capacities. All power and control signal connectors are located on the back side for easy integration. The SYS68K/WFMOD can be installed in a 19" rack of appropriate depth and height.

Configurations
SYS68K/WFMOD-20
The SYS68K/WFMOD-20 is configured as follows: Chassis 6HE/30TE with a 20 Mbyte Winchester and a 1 Mbyte slim line Floppy Drive.

SYS68K/WFMOD-50
The SYS68K/WFMOD-50 is configured as follows: Chassis 6HE/30TE with a 50 Mbyte Winchester and a 1 Mbyte slim line Floppy Drive.

SYS68K/WFMOD-80
The SYS68K/WFMOD-80 is configured as follows: Chassis 6HE/30TE with a 80 Mbyte Winchester and a 1 Mbyte slim line Floppy Drive.

SYS68K/WFMOD-175
The SYS68K/WFMOD-175 is configured as follows: Chassis 6HE/30TE with a 175 Mbyte Winchester and a 1 Mbyte slim line Floppy Drive.

Specifications

	WFMOD-20	WFMOD-50	WFMOD-80	WFMOD-175
Winchester capacity (unformatted)	20 Mbyte	50 Mbyte	80 Mbyte	175 Mbyte
Floppy capacity	1 Mbyte	1 Mbyte	1 Mbyte	1 Mbyte
Winchester Interface	ST506/412	ST506/412	ST506/412	SCSI
Floppy Interface	SA 460	SA 460	SA 460	SA 460
Power	+ 5V(A) +12V(A)	+ 5V(A) +12V(A)	+ 5V(A) +12V(A)	+ 5V(A) +12V(A)
Chassis	6HE/30TE 19"compatible	6HE/30TE 19"compatible	6HE/30TE 19"compatible	6HE/30TE 19" compatible
Depth	230 mm	230 mm	230 mm	230 mm
Operating Temp.	10°C–46°C	10°C–46°C	10°C–46°C	10°C–46°
Relative Humidity	10%–80%	10%–80%	10%–80%	10%–80%
Power Connectors	AMP PIN 480424–0	AMP PIN 480424–0	AMP PIN 480424–0	AMP PIN 480424–0
Control Connectors	34 pin edge Connectors	34 pin edge Connectors	34 pin edge Connectors	34 pin edge Connectors
Connectors	20 pin edge Connectors	20 pin edge Connectors	20 pin edge Connectors	50 pin IDC

Ordering Information

SYS68K/WFMOD-20 Part No. 700002	Winchester Floppy Module with 20 Mbyte Winchester, including OEM Manuals
SYS68K/WFMOD-50 Part No. 700020	Winchester Floppy Module with 50 Mbyte Winchester, including OEM Manuals
SYS68K/WFMOD-80 Part No. 700012	Winchester Floppy Module with 80 Mbyte Winchester, including OEM Manuals
SYS68K/WFMOD-175 Part No. 700022	Winchester Floppy Module with 175 Mbyte Winchester, including OEM Manuals

Direct Offices, Distributors and Representatives

CORPORATE HEADQUARTERS

FORCE COMPUTERS INC.
3165 Winchester Blvd.
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Tel.: (408) 370-6300
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Fax: (408) 374 1146

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SOUTH CAROLINA
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301/574-7777

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3700 Koppers St., Ste 109
Baltimore, MD 21227
301/574-7777

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Canada L4W 2S7
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1–800 BEST VME
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(inside CA)

EUROPEAN HEADQUARTERS
FORCE COMPUTERS GmbH
Daimlerstraße 9
D-8012 Ottobrunn/München
Tel.: (089) 60091-0
Tlx.: 524190 forc d
Fax: (089) 6097793

EUROPEAN SALES OFFICES

GERMANY
FORCE COMPUTERS GmbH
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D-8012 Ottobrunn/München
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Tel. (01) 242 52 04
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SWEDEN
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Box 8314
Stormbyvägen
S-163 08 Spånga
Tel. (08) 761 78 20
Tlx. 15511 scancop s

SWITZERLAND
W. MOOR AG
Bahnstrasse 58/60
CH-8105 Regensdorf
Tel. (01) 843 31 11
Tlx. 825840 moor ch

TAIWAN
NEW RABBIT ASSOCIATES
4F No. 400 Keelung Road
Section 1
Taipei
Tel. 705 21 78
Tlx. 13078 gregtang

UNITED KINGDOM
MICROSYSTEM SERVICES
P.O. Box No. 37
Lincoln Road
Cressex Industrial Estate
High Wycombe
Bucks, HP1 23XJ
Tel. (0494) 416 61
Tlx. 837187 micsys g

Corporate Headquarters

FORCE COMPUTERS INC.
3165 Winchester Blvd.
Campbell, CA 95008
UNITED STATES OF AMERICA

European Headquarters

FORCE COMPUTERS GmbH
Daimlerstraße 9
8012 Ottobrunn/Munich
W.-GERMANY