SYS68K/DRAM-E3M1

HARDWARE USER'S MANUAL

32 BIT DYNAMIC MEMORY BOARD WITH FME INTERFACE

2nd Edition
September 1985

PART NO. 800043

FORCE COMPUTERS Inc./GmbH

P/N 999530

N O T E

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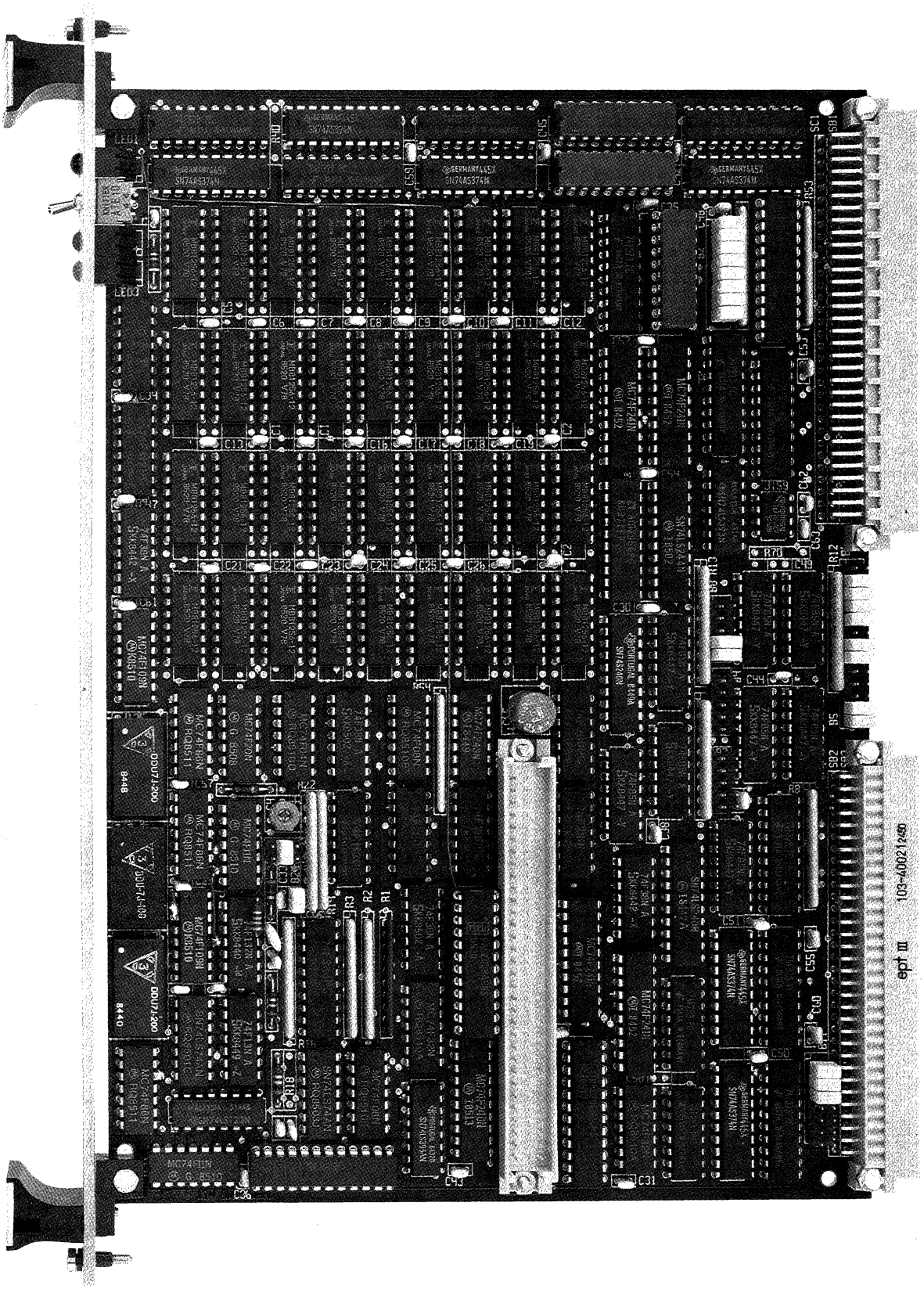
Figure 1: Photo of the SYS68K/DRAM-E3M1



1.Ø General Information

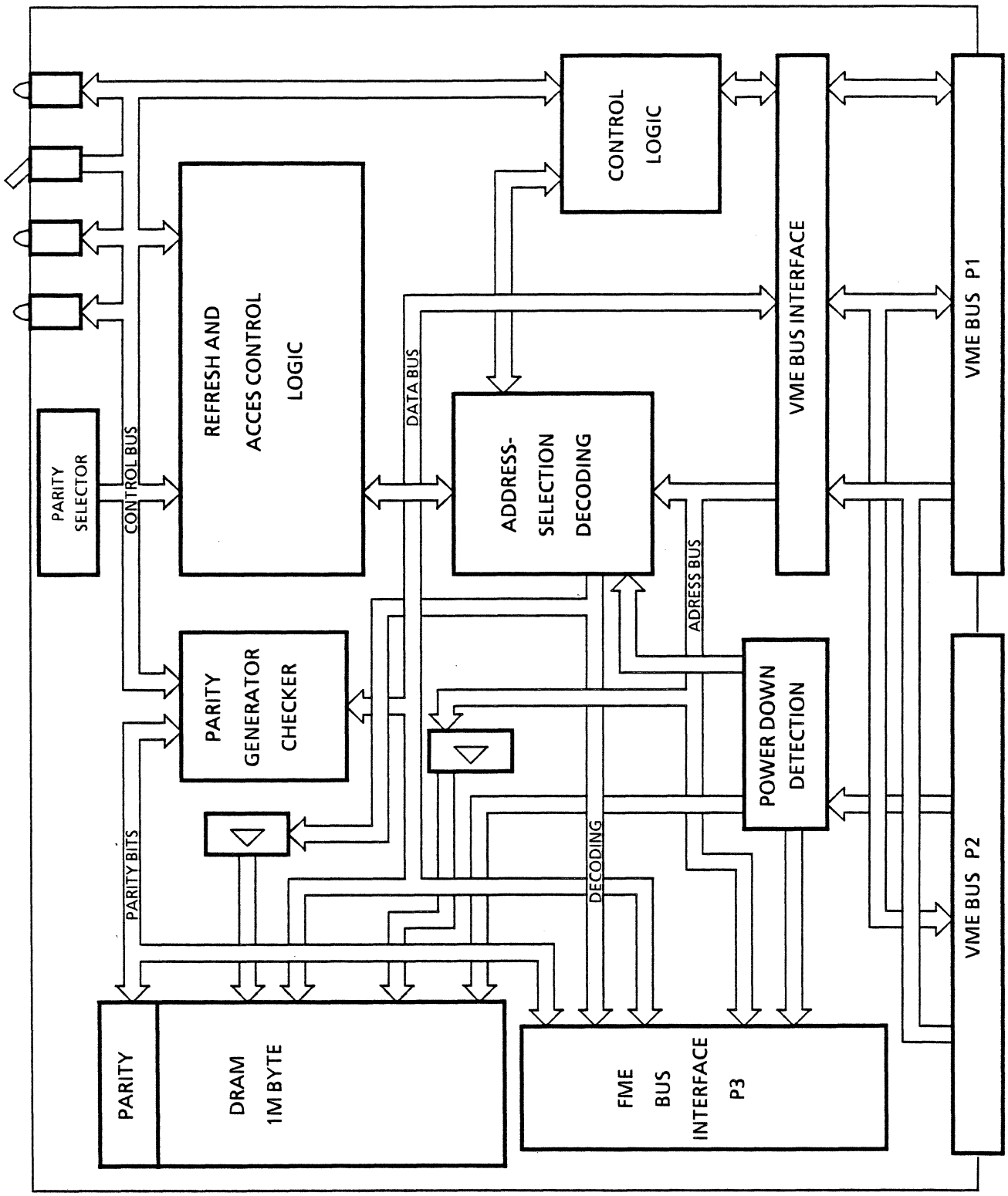
The SYS68K/DRAM-E3M1 high speed dynamic memory board designed for VMEbus/P1Ø14* environments offers 1M byte of RAM capacity.

The board is able to transfer 8, 16, 24 or 32 bits of data in the whole address range of 16M byte or 4G Byte because all 32 address lines of the VME/P1Ø14* bus are supported. Additionally, an FMEbus master interface for memory expansion is included. Battery backup is provided through a connection on P2.

Three LEDs for status display and a RUN/LOCAL switch allow easy handling of the board.

IEEE P1Ø14* Bus specification (VMEbus) of the IEEE Computer Society TC.

Figure 2: Block Diagram SYS68K/DRAM-E3M1



2.Ø General Operation

The SYS68K/DRAM-E3M1 (see Figure 1) contains the VMEbus interface, timing and control logic, refresh circuitry and the RAM storage array (1M byte). The board also contains circuitry to generate and check parity and to generate a bus error if a Parity Error is detected.

Easy access address selection in 256K byte increments is provided through jumper fields. The FMEbus master interface allows easy memory expansion through SYS68K/DRAM-E3SX boards.

If a Parity Error is detected, a BERR* is driven to the VMEbus as long as the parity check is enabled.

A RUN/LOCAL switch can separate the board from the VMEbus without loss of data. This mode is displayed by an LED. An access LED is required on the front panel to inform the user that an access to a DRAM area is pending.

A general block diagram of the SYS68K/DRAM-E3M1 is shown in Figure 2.

3.Ø Hardware Description

The address selection, VMEbus response timing diagram, functional description and the jumper settings are described in the following sections.

3.1 Supported Transfer Types

The SYS68K/DRAM-E3M1 is capable of transferring 8, 16, 24 or 32 bits of data. The VMEbus/PlØ14* spec defines the transfer type as well as the number of bytes to be transferred.

Table 1 lists all transfer types supported by the DRAM-E3M1 and the DRAM-E3SX boards connected to the DRAM-E3M1.

The VME/PlØ14 specification defines the relationship between the control signals and the transfer type. Please refer to the specification for further details.

Table 1: Supported Data Transfer Types

Data Transfer Type		D24-D31	D16-D23	D8-D15	DØ-D7	Note
Address Only						
Single Byte (8 bit)	EVEN			x		
	ODD				x	
Double Byte (16 bit)				x	x	
Quad Byte (32 bit)		x	x	x	x	
Single Byte Read Modify Write (8 bit RMW)	EVEN			x		
	ODD				x	
Double Byte Read Modify Write (16 bit RMW)				x	x	
Quad Byte Read Modify Write (32 bit RMW)		x	x	x	x	
Unaligned Transfers			x	x		
		x	x	x		
			x	x	x	
Unaligned RMW Transfers			x	x		
		x	x	x		
			x	x	x	

3.2 Access to the DRAM-E3M1 Board

Easy access address and address modifier code selection to the DRAM-E3M1 board is provided through jumperfields. The access address is jumper selectable in 256K byte steps to allow contiguous memory configuration to other VME/P1Ø14 bus based boards.

3.2.1 The Access Address Selection of the DRAM-E3M1 Board

This chapter describes the address selection of the DRAM-E3M1 board excluding slave boards (DRAM-E3SX) because the access address selection of the board including the slave boards is described in chapter 4.1. The memory capacity of the DRAM-E3M1 board is 1M byte.

The comparator ICs J118 to J125 decode the address range out of the whole range of 16M byte (A24 mode) or 4G byte (A32 mode).

The least significant address signal which can be modified is A18.

A24 decoding:

23	22	21	2Ø	19	18	17	16
y	y	y	y	y	y	x	x

y = set to logical Ø or 1
x = don't care

To allow a flexible lay-out, the DRAM-E3M1 board allows the access address selection in 256K byte boundaries by jumper settings in jumper areas (3 jumperfields each).

One jumper area defines the start address at which the board can be accessed.

The other jumper area defines the first address at which the board cannot be accessed. The address range at which the board responds to is set by default from $FF1Ø ØØØØ to $FF1F FFFF.

In a standard environment (68ØØØ or 68Ø1Ø processor) the address lines A24 to A31 are not driven (A24 mode). The decoding logic of the DRAM-E3M1 board provides the A32 mode and offers a full 32 bit decoding. For this purpose the address lines A24 to A31 are decoded every time. In an A24 environment, the upper address lines A24 to A31 have to be ignored from the decoding logic. This is provided through internal pull-up resistor networks which pull the upper address lines to high state. This results in the need to jumper the start address to $FF1Ø ØØØØ for parallel decoding in the A24 and A32 mode.

Figure 3 outlines the decoding logic in a general block diagram and Table 2 lists the relation between the jumperfields and the address range to be selected.

Jumperfields B4, B5 and B6 define the start address because B7, B8 and B9 define the first address which is not on the DRAM-E3M1.

Figure 4 outlines the location diagram of the access address selection jumperfields.

Table 3 lists the default connection of the DRAM-E3M1 board during manufacturing (delivery version).

Figure 3: The Decoding Logic Block Diagram

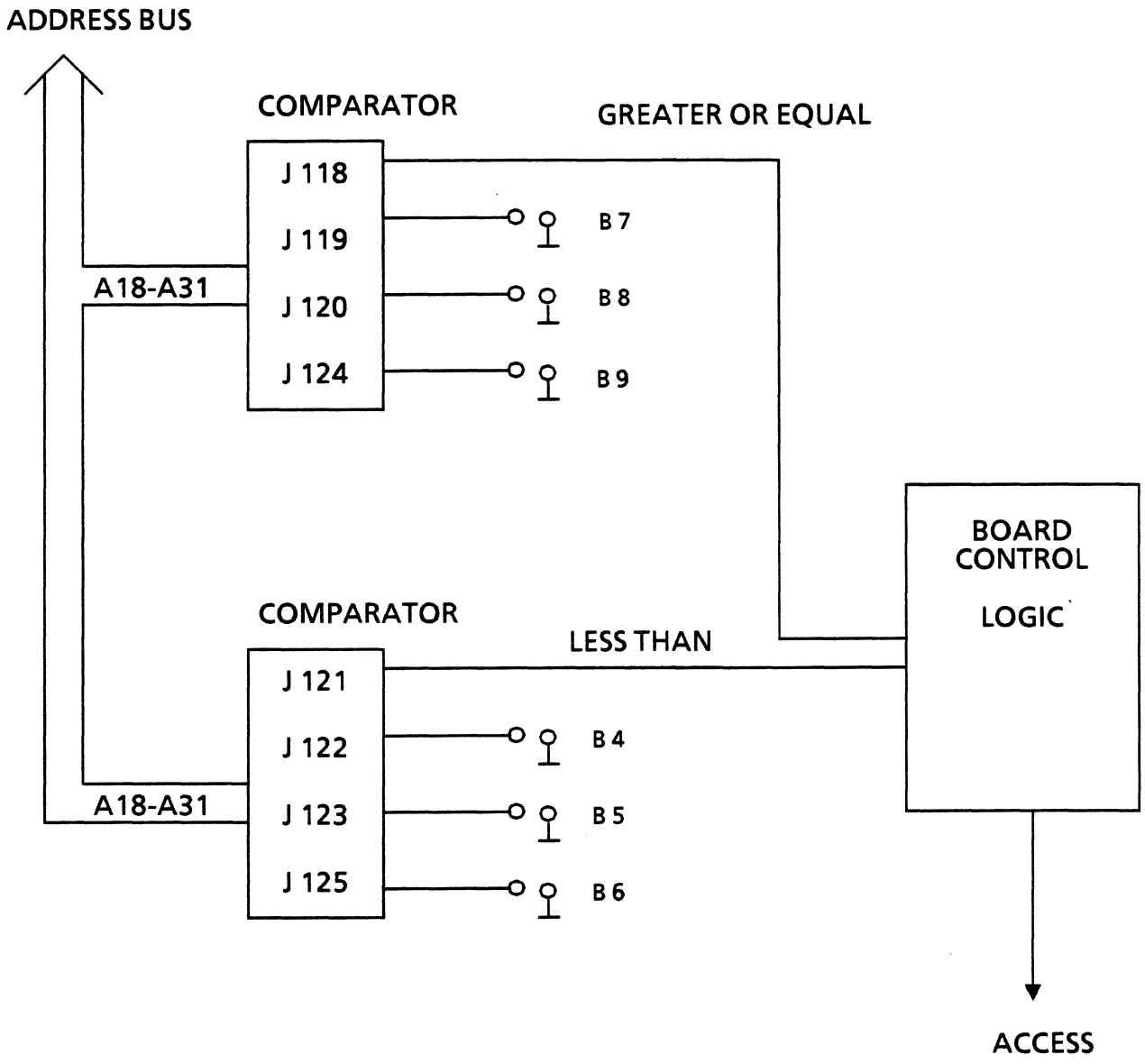


Figure 4: Location Diagram of the Access Address Selection Jumperfields

Please see Appendix C for the complete location diagram.

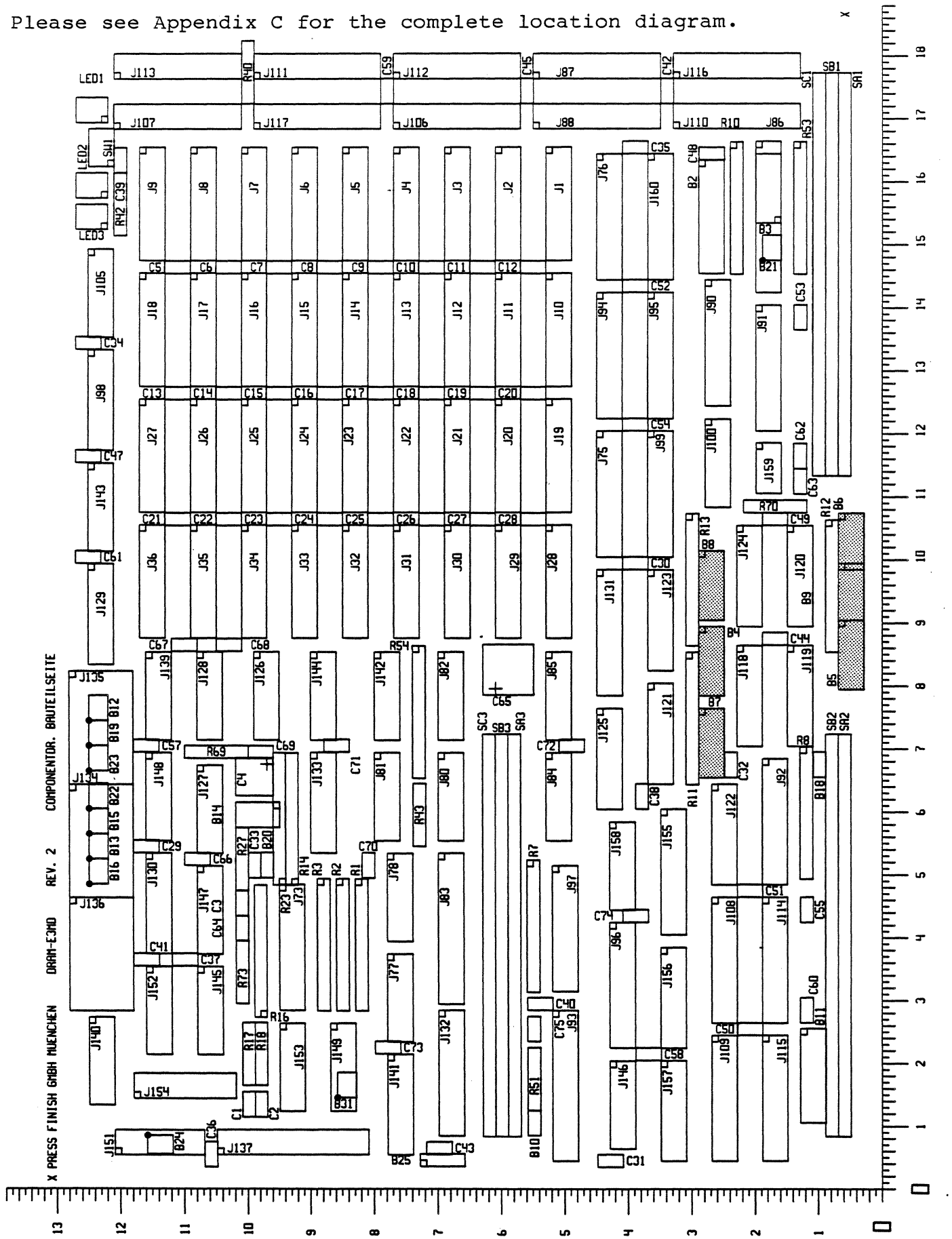


Table 2: Jumperfield Assignment to Access Address Selection

START Address Selection				Selection of 1st not on-board Addr		
Jumperfield			Corresponding Bus Address Signal	Jumperfield		
B7	B8	B9		B4	B5	B6
1-10			A31	1-10		
2-9			A30	2-9		
3-8			A29	3-8		
4-7			A28	4-7		
5-6			A27	5-6		
	1-10		A26		1-10	
	2-9		A25		2-9	
	3-8		A24		3-8	
	4-7		A23		4-7	
	5-6		A22		5-6	
		1-8	A21			1-8
		2-7	A20			2-7
		3-6	A19			3-6
		4-5	A18			4-5

Table 3: Default Access Address Selection

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6			5-6		A22
		1-8				A21
					2-7	A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF1F FFFF	$1F FFFF
First not on-board Address:	$FF20 0000	$20 0000
Boundary:	$0010 0000	$10 0000
	1M byte	1M byte

3.2.2 Modification of the Access Address of the DRAM-E3M1

Due to the full decoding of the 21 address signals, the DRAM-E3M1 can be jumpered to react on different access address ranges. Tables 4, 5 and 6 outline 3 examples of the DRAM-E3M1 configuration for different memory ranges.

To adapt the board access address range to the appropriate range, please follow the following rules:

1) Calculate the start address of the board and list the address line value A31 to A18 in binary form (Ø or 1)

2) Calculate the first not on-board address by adding the boundary and list the address line value A31 to A18 in binary form (Ø or 1)

3) Install or remove the jumpers in the jumperfields B4 to B9 in the following way:

   a Ø on the corresponding address signal is equivalent to an inserted jumper,

   a 1 on the corresponding address signal is equivalent to a removed jumper.

Table 7 gives an empty form for installation of the used setup.

Note:1) If the A32 and the A24 mode is used, the address signals A24 to A31 must be high for a valid A24 decoding. If not, the A24 decoding is disabled.

2) If only the A32 mode is used, there are no limitations regarding address selection.

3a) If only the A24 mode is used, A24 to A31 must be high (provided through on-board pull-up register networks) if not disabled (see 3b).

3b) If only the A24 mode is used, A24 to A31 can be disabled by removing the jumper at jumperfield B18.

Caution: In the default configuration B18 is not inserted (A24 mode is enabled!)

Table 4: Access Address Selection Example 1

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		0 A23 0
	5-6			5-6		0 A22 0
		1-8			1-8	0 A21 0
		2-7				0 A20 1
						1 A19 1
		4-5			4-5	0 A18 0

	A32	A24
Start Address:	$FF08 0000	$08 0000
End Address:	$FF17 FFFF	$17 FFFF
First not on-board Address:	$FF18 0000	$18 0000
Boundary:	$0010 0000	$10 0000
	1M byte	1M byte

Table 5: Access Address Selection Example 2

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
						A22
						A21
		2-7				A20
		3-6			3-6	A19
						A18

	A32	A24
Start Address:	$FF64 0000	$64 0000
End Address:	$FF73 FFFF	$73 FFFF
First not on-board Address:	$FF74 0000	$74 0000
Boundary:	$0010 0000	$10 0000
	1M byte	1M byte

Table 6: Access Address Selection Example 3

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
1-10			1-10			A31
2-9			2-9			A30
						A29
						A28
5-6			5-6			A27
						A26
						A25
	3-8			3-8		A24
	4-7			4-7		A23
						A22
		1-8			1-8	A21
		2-7				A20
		3-6			3-6	A19
						A18

	A32	A24
Start Address:	$3644 0000	
End Address:	$3653 FFFF	NOT
First not on-board Address:	$3654 0000	DECODED
Boundary:	$0010 0000	
	1M byte	1M byte

Table 7: Access Address Selection

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
						A23
						A22
						A21
						A20
						A19
						A18

	A32	A24
Start Address:	$	$
End Address:	$	$
First not on-board Address:	$	$
Boundary:	$	$
	1M byte	1M byte

3.3 The Address Modifier Decoding

The VME/P1Ø14 specification defines address modifier (AM-) codes which are decoded in parallel to the address signals. The 6 AM Code signals are routed directly into a PAL and a total number of 1Ø different codes can be separately enabled via jumper settings. Table 8 lists the AM-Codes which are defined in the VME/P1Ø14 specification.

A short I/O access to the DRAM-E3M is not necessary because the memory range of the board is greater than the range for this AM-Code.

Additionally, the block transfer is not supported through the DRAM-E3M1 board. Therefore, the AM codes, listed in Table 9 are allowed. To enable each of the AM-Codes separately, the jumperfields B2, B3 and B21 are installed on the board. Figure 5 outlines the location diagram of the AM-Code jumperfields.

Figure 5: The AM-Code Jumperfields

Please see Appendix C for the complete location diagram.

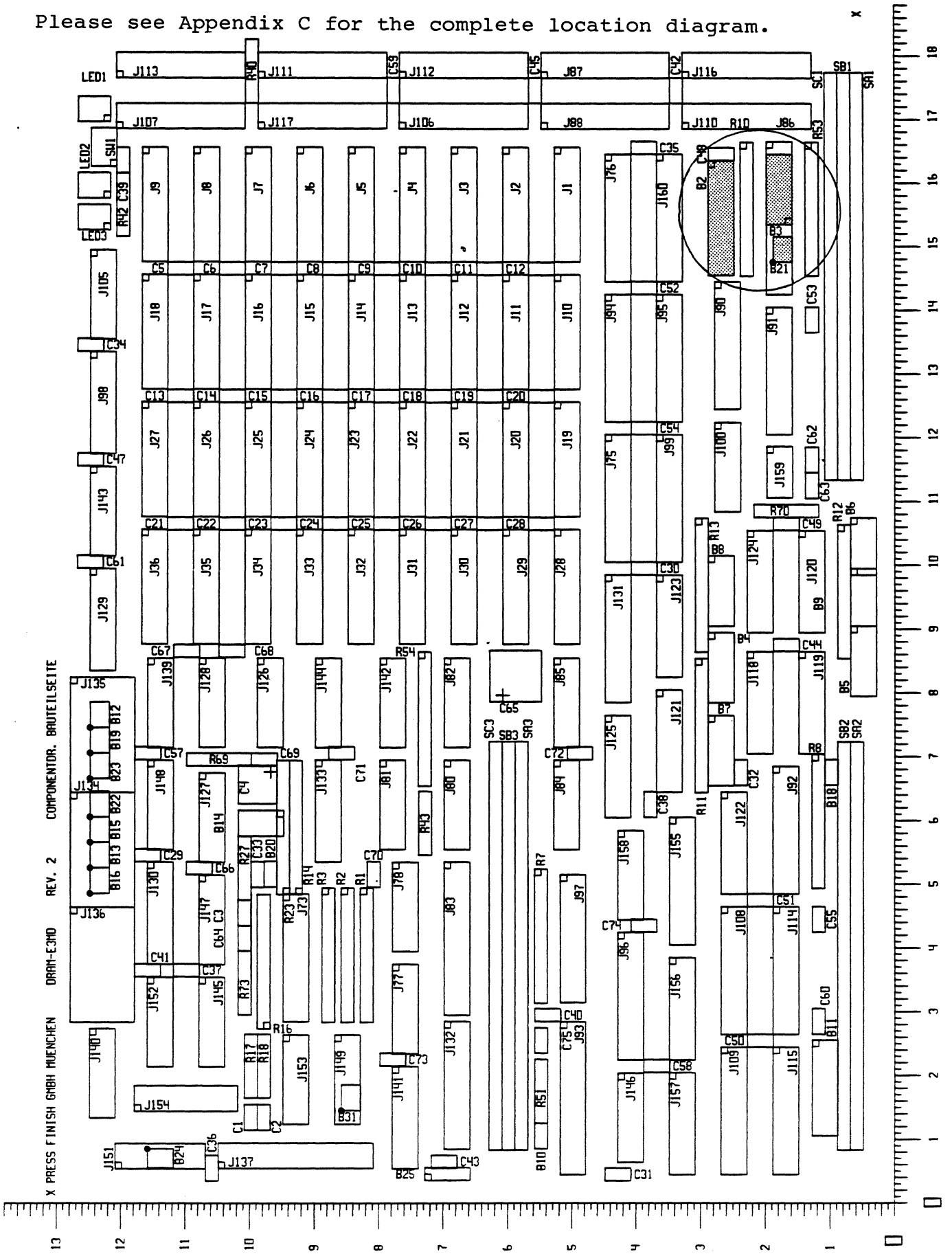


Table 8: The Address Modifier Codes

HEX CODE	Address Modifier 5	4	3	2	1	Ø	Function
3F	H	H	H	H	H	H	Standard Supervisory Block Transfer
3E	H	H	H	H	H	L	Standard Supervisory Program Access
3D	H	H	H	H	L	H	Standard Supervisory Data Access
3C	H	H	H	H	L	L	Reserved
3B	H	H	H	L	H	H	Standard Non-Privileged Block Transfer
3A	H	H	H	L	H	L	Standard Non-Privileged Program Access
39	H	H	H	L	L	H	Standard Non-Privileged Data Access
38	H	H	H	L	L	L	Reserved
37	H	H	L	H	H	H	Reserved
36	H	H	L	H	H	L	Reserved
35	H	H	L	H	L	H	Reserved
34	H	H	L	H	L	L	Reserved
33	H	H	L	L	H	H	Reserved
32	H	H	L	L	H	L	Reserved
31	H	H	L	L	L	H	Reserved
3Ø	H	H	L	L	L	L	Reserved
2F	H	L	H	H	H	H	Reserved
2E	H	L	H	H	H	L	Reserved
2D	H	L	H	H	L	H	Short Supervisory Access
2C	H	L	H	H	L	L	Reserved
2B	H	L	H	L	H	H	Reserved
2A	H	L	H	L	H	L	Reserved
29	H	L	H	L	L	H	Short Non-Privileged Access
28	H	L	H	L	L	L	Reserved
27	H	L	L	H	H	H	Reserved
26	H	L	L	H	H	L	Reserved
25	H	L	L	H	L	H	Reserved
24	H	L	L	H	L	L	Reserved
23	H	L	L	L	H	H	Reserved
22	H	L	L	L	H	L	Reserved
21	H	L	L	L	L	H	Reserved
2Ø	H	L	L	L	L	L	Reserved

L = low signal level
H = high signal level

Table 8 cont'd

HEX CODE	Address Modifier 5	4	3	2	1	Ø	Function
1F	L	H	H	H	H	H	User defined
1E	L	H	H	H	H	L	User defined
1D	L	H	H	H	L	H	User defined
1C	L	H	H	H	L	L	User defined
1B	L	H	H	L	H	H	User defined
1A	L	H	H	L	H	L	User defined
19	L	H	H	L	L	H	User defined
18	L	H	H	L	L	L	User defined
17	L	H	L	H	H	H	User defined
16	L	H	L	H	H	L	User defined
15	L	H	L	H	L	H	User defined
14	L	H	L	H	L	L	User defined
13	L	H	L	L	H	H	User defined
12	L	H	L	L	H	L	User defined
11	L	H	L	L	L	H	User defined
1Ø	L	H	L	L	L	L	User defined
ØF	L	L	H	H	H	H	Extended Supervisory Block Transfer
ØE	L	L	H	H	H	L	Extended Supervisory Program Access
ØD	L	L	H	H	L	H	Extended Supervisory Data Access
ØC	L	L	H	H	L	L	Reserved
ØB	L	L	H	L	H	H	Extended Non-Privileged Block Transfer
ØA	L	L	H	L	H	L	Extended Non-Privileged Program Access
Ø9	L	L	H	L	L	H	Extended Non-Privileged Data Access
Ø8	L	L	H	L	L	L	Reserved
Ø7	L	L	L	H	H	H	Reserved
Ø6	L	L	L	H	H	L	Reserved
Ø5	L	L	L	H	L	H	Reserved
Ø4	L	L	L	H	L	L	Reserved
Ø3	L	L	L	L	H	H	Reserved
Ø2	L	L	L	L	H	L	Reserved
Ø1	L	L	L	L	L	H	Reserved
ØØ	L	L	L	L	L	L	Reserved

L = low signal level
H = high signal level

Table 9 lists the selectable AM-Codes.

Table 9: The AM-Code Selection

Jumperfield B2	Jumperfield B3	HEX Code	Function
1-16		3E	Standard Supervisor Program Access
2-15		3D	Standard Supervisor Data Access
3-14		3A	Standard Non-Privileged Program Access
4-13		39	Standard Non-Privileged Data Access
5-12		ØE	Extended Supervisor Program Access
6-11		ØD	Extended Supervisor Data Access
7-1Ø		ØA	Extended Non-Privileged Program Access
8-9		Ø9	Extended Non-Privileged Data Access
	1-1Ø	1Ø	USER defined
	3-8	11	USER defined
	4-7		*
	5-6		*
	2-9		Respond always *

* for test purposes only.

Caution: Jumperfield B21 is for in-circuit test purposes only and has to be disconnected during normal operation.

Each of the AM-Codes may be used in the environment. To enable an AM-Code, the corresponding connection has to be provided.

Table 1Ø lists the default condition during manufacturing. If the default set-up is not usable and a special set-up has to made, please follow the following 2 rules:

1) Define the AM-Codes for the DRAM-E3M1 board.

2) Insert or remove the jumpers in jumperfield B2 and/or install or remove a wire on the jumperfield B3 in the following way:

   An inserted jumper/wire enables the corresponding AM-Code (as listed in Table 9) because a removed jumper/wire will disable the corresponding AM-Code.

Tables 11 to 13 list examples for AM-Code combinations. Table 14 is an empty form.

Table 1Ø: Default AM-Code Selection

Jumperfield Connections		AM-Code	Enabled AM-Code (x)
B2	B3		
1-16		3E	Y
2-15		3D	Y
3-14		3A	Y
4-13		39	Y
5-12		ØE	Y
6-11		ØD	Y
7-1Ø		ØA	Y
8-9		Ø9	Y
		1Ø	N
		11	N

Table 11: AM-Code Selection Example 1

Jumperfield Connections		AM-Code	Enabled AM-Code (x)
B2	B3		
1-16		3E	Y
2-15		3D	Y
		3A	N
		39	N
5-12		ØE	Y
6-11		ØD	Y
		ØA	N
		Ø9	N
		1Ø	N
		11	N

Example 1: The DRAM-E3M1 responds to 24 bit and 32 bit addressing (A24 and A32 mode) only under Supervisor mode. All non-privileged accesses are ignored.

Table 12: AM-Code Selection Example 2

Jumperfield Connections		AM-Code	Enabled AM-Code (x)
B2	B3		
1-16		3E	Y
2-15		3D	Y
3-14		3A	Y
4-13		39	Y
		ØE	N
		ØD	N
		ØA	N
		Ø9	N
		1Ø	N
		11	N

Example 2: All A32 mode accesses are ignored by the DRAM-E3M1 board. Only A24 mode accesses are supported.

Table 13: AM-Code Selection Example 3

Jumperfield Connections		AM-Code	Enabled AM-Code (x)
B2	B3		
		3E	N
		3D	N
		3A	N
		39	N
5-12		ØE	Y
6-11		ØD	Y
7-1Ø		ØA	Y
8-9		Ø9	Y
	1-1Ø	1Ø	Y
	3-8	11	Y

Example 3: A32 mode accesses as well as the user defined AM-Codes 1Ø and 11 are supported. All other AM-Codes (i.e. the A24 mode) are ignored.

Table 14: AM-Code Selection

Jumperfield Connection		AM-Code	Enabled AM-Code (x)
B2	B3		
		3E	
		3D	
		3A	
		39	
		ØE	
		ØD	
		ØA	
		Ø9	
		1Ø	
		11	

3.4 The Parity Check

The DRAM-E3M1 board contains 36 memory chips (256K * 1 bit); 32 bits for data storage and 4 bits for byte parity information.

The board supports 8, 16, 24 and 32 bit data transfers. Each of the 4 bytes which may be read or written at the same time, has a separately controlled parity checker/generator.

The parity generator is activated on every write access only for the selected bytes (up to 4) which are transferred.

On read accesses the parity checker for the selected byte(s) is activated by default during manufacturing.

If a parity error is detected and if the parity check is enabled, the DRAM-E3M1 board drives the BERR signal instead of the DTACK* signal. On occurrence of a parity error, the red FAIL LED on the front panel lights up.

The byte parity check can easily be disabled by following the rules listed below:

1) Remove jumper at jumperfield B2Ø

2) Remove jumper between pin 2 and pin 5 at jumperfield B14

3) Install a jumper between pin 1 and pin 6 at jumperfield B14.

The default connections during manufacturing for the enabled parity check are listed below:

Table 15: Parity Check Jumper Fields

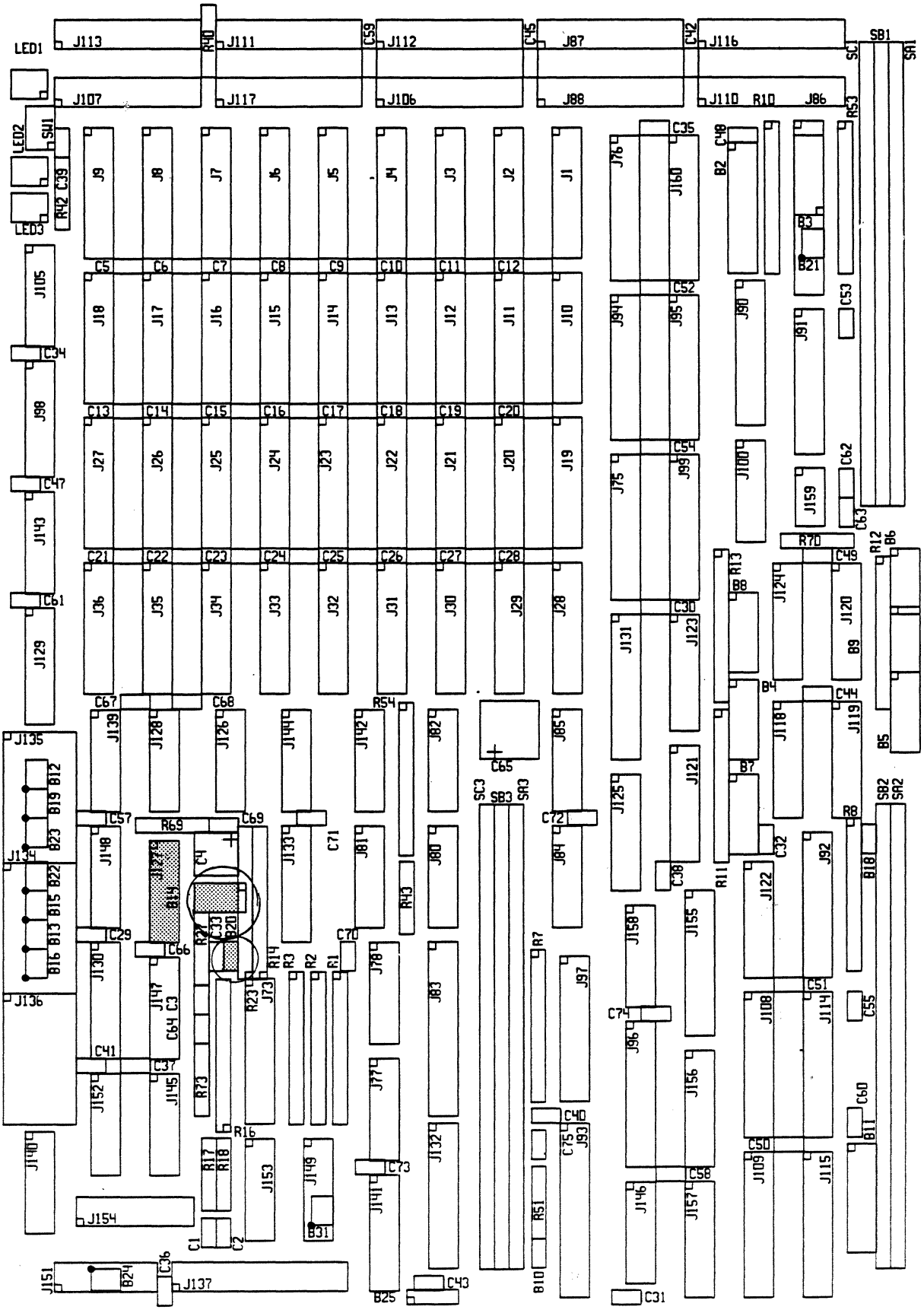
B2Ø	B14	Mode	Note
IN	2 - 5	Parity Error Check enabled	*
OUT	1 - 6	Parity Error Check Disabled	

* Default condition

Figure 6 outlines the location diagram of the parity check jumperfields.

Figure 6: Parity Check Jumperfield Locations

Please see Appendix C for the complete location diagram.



3.5 The Access Times

The DRAM-E3M1 board is a high speed dynamic RAM board which provides the following access times:

Table 16: Access Times of the DRAM-E3M1

Access Times	Type	Max
WRITE with Parity Generation	70ns	80ns
READ with Parity Check	245ns	265ns
READ without Parity Check	210ns	225ns

The access time is measured from the falling edge of one of the two data strobes to the falling edge of DTACK* generated from the DRAM-E3M1 board.

The cycle time from the beginning of a cycle is 315ns typ / 335ns max.

Due to the interleave structure of the board (decoding and next access are interleaved), a high throughput is provided. If an access was forced, the next access can occur within the following time frames:

Next Access after	TYP	MAX
WRITE	250ns	270ns
READ	70ns	90ns

Therefore, the following transfer capacity is provided on the VME/P1014 bus (if the transfer device has an ideal VME/P1014 timing).

Cycle	TYP	MIN
WRITE	12.0M byte/s	11.0M byte/s
READ	12.0M byte/s	11.0M byte/s

3.6 The Refresh

The refresh for the dynamic RAMs is distributed over 4ms and provision is made to minimize the overhead and delay to the VMEbus accesses.

After the internal read cycle of the DRAMs is finished and the data on a read cycle has been stored in the output data latches, a pending refresh request (every 15us) is executed independent from all VMEbus activities. Therefore, the overhead time for the VMEbus protocol is used to refresh the RAMs. In addition to the refresh interleave, a refresh to the DRAMs is forced if a not on-board access is detected between 11 and 15us after the execution of the last refresh.

A 68Ø1Ø processor with a clock frequency of 1ØMHz can access the DRAM-E3M1 board without extra wait states for the DRAM refresh if the used program runs on the DRAM-E3M1 or DRAM-E3SX.

The refresh control logic for the FMEbus slave modules (memory expansion) is included on the DRAM-E3M1 board.

	TYP	MAX
Overhead time for refresh	12Øns	45Øns

An access can stay for a longer time than the refresh period (15us) because every access cycle on the board is aborted if the correct data is stored on the RAMs or in the output latches to the VMEbus.

Therefore, correct refresh is provided if a system hang-up occurs or if a bus master holds an access for a long time.

If the board is jumpered to work from the standby power, refresh for the dynamic RAMs is provided during main power down.

3.7 The Battery Backup Option

The DRAM-E3M1 board can be powered from the +5V main power or from the +5VBAT pins of P2 connector (SA-30/31/32).

The default condition during manufacturing is the connection to the +5V Main Power.

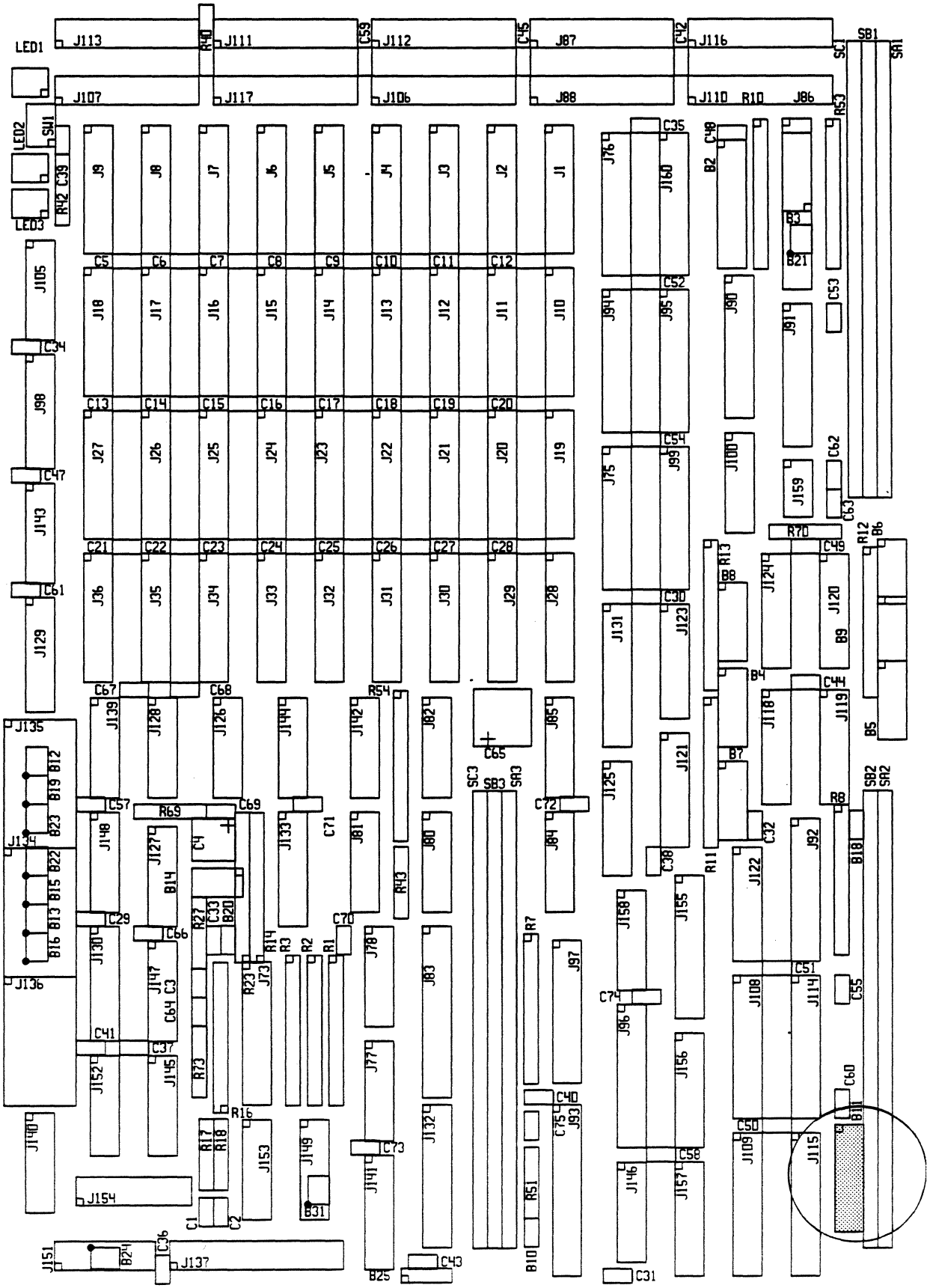
Table 17 lists the jumper settings which have to be made for the different modes, and Figure 7 outlines the location diagram of the jumperfields.

Table 17: The Battery Backup Option

Option	B11
Battery Backup	5-10 6-9 7-8
5V STDBY (optional)	4-11
+5V MAIN	1-14 2-13 3-12

Figure 7: Location Diagram of the Battery Backup Jumperfields

Please see Appendix C for the complete location diagram.



3.8 The Front Panel

The DRAM-E3M1 board contains a RUN/LOCAL switch which disables the board from the VME/P1Ø14 bus if set to LOCAL. In RUN position, the green "RUN" LED on the front panel turns on, and the red "FAIL" LED lights up if the board is in LOCAL mode.

During normal operation the "FAIL" LED may turn on if a parity error is detected. The parity error is latched and only reset if the board is reset through the SYSRESET* signal from the VMEbus or through a RUN-LOCAL-RUN change of the RUN/LOCAL switch.

Additionally, a yellow SELect LED is installed. The LED turns on if the board is selected (an access is pending).

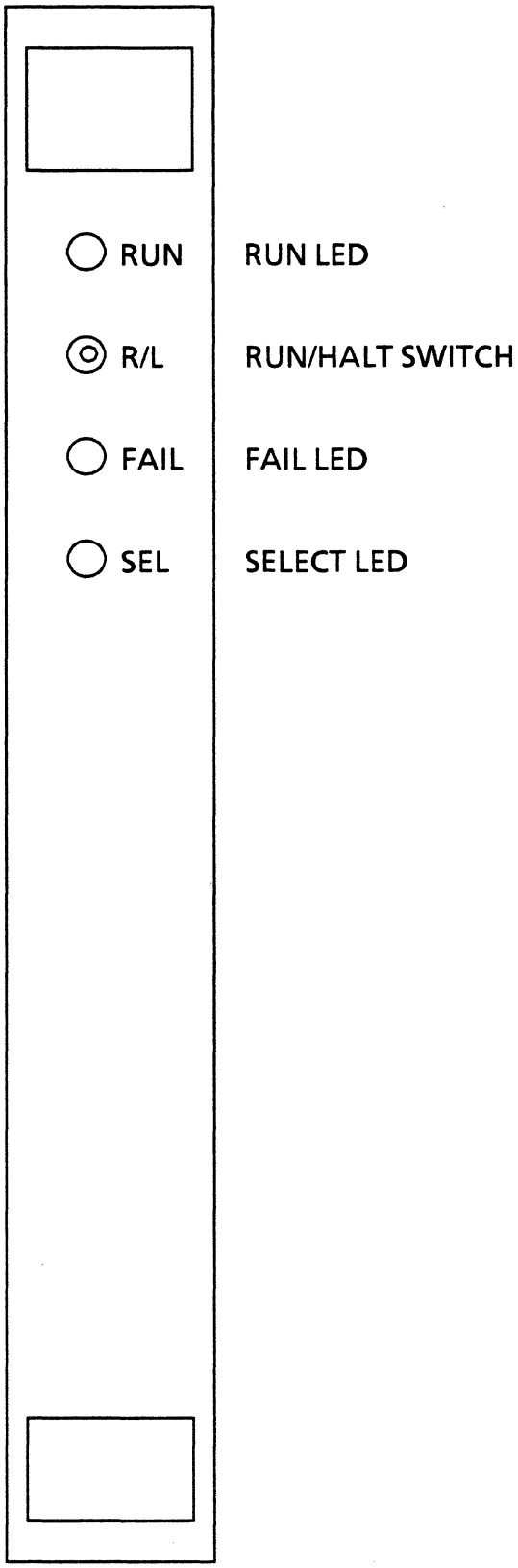
Figure 8 shows the front panel lay-out in detail.

RUN	FAIL	Function
-	X	Board in LOCAL mode
X	-	Board in RUN mode
X	X	Board in FAIL mode

Note: All other combinations are not possible.

X = LED active.

Figure 8: The Front Panel of the SYS68K/DRAM-E3M1



4.Ø The FMEbus Interface

The DRAM-E3M1 board contains an FMEbus interface for memory expansion. All the control logic for access and refresh is included on the DRAM-E3M1 board to allow cost effective memory expansions.

The general block diagram of the FME concept is shown in Figure 9.

Cost and space intensive ICs are spent only on the master interface (DRAM-E3M1) and only driver circuitries are included on the DRAM-E3SX boards. This allows easy memory expansion through 1 or 2 slave boards.

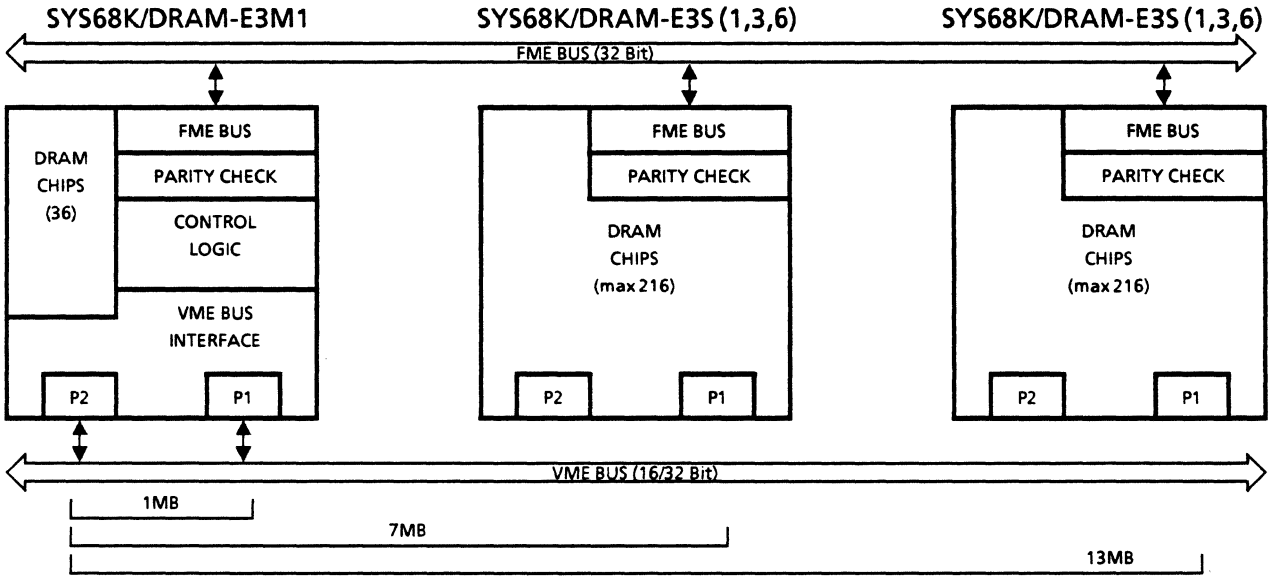
The following slave boards are now available to interconnect the DRAM-E3M1:

Board	Capacity
DRAM-E3S1	1Mbyte
DRAM-E3S3	3Mbyte
DRAM-E3S6	6Mbyte

A maximum of 13M byte DRAM is provided using a DRAM-E3M1 and two DRAM-E3S6 boards.

Easy installation of the slave boards is provided through the 3rd 96 pin DIN connector.

Figure 9: The FME Concept



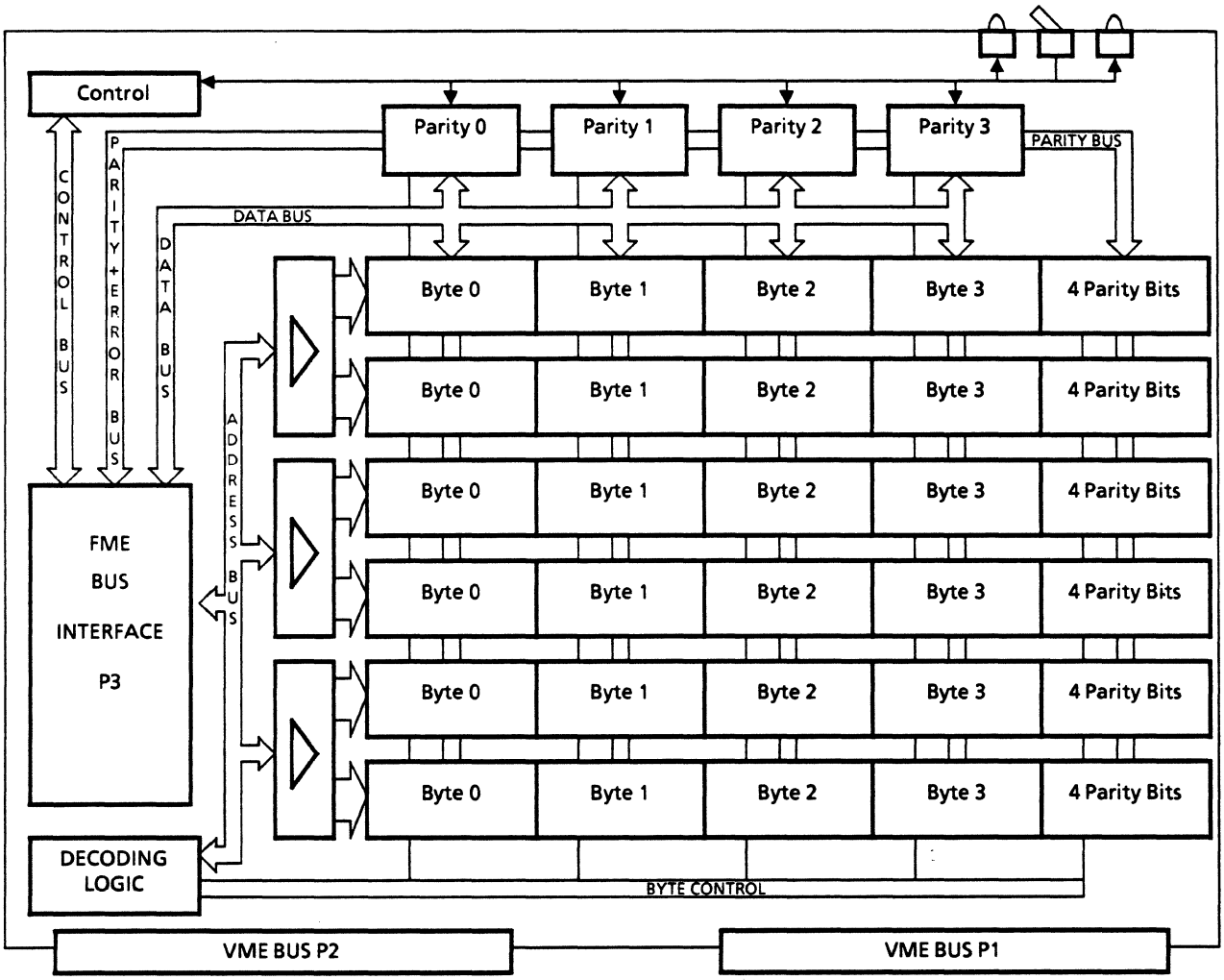
The connection as a second slave board requires a fulfilled first slave board (boards may be exchanged in order of position). Please follow the installation rules in the DRAM-E3SX manual.

Table 18: Usable Slave Board Combinations

	1st Slave	2nd Slave	Total Memory Capacity
E3M1			1M byte
E3M1	E3S1	--	2M byte
E3M1	E3S3		4M byte
E3M1	E3S3	E3S1	5M byte
E3M1	E3S3	E3S3	7M byte
E3M1	E3S6		7M byte
E3M1	E3S6	E3S1	8M byte
E3M1	E3S6	E3S3	10M byte
E3M1	E3S6	E3S6	13M byte

A general block diagram of the DRAM-E3S6 board is shown in Figure 10.

Figure 1Ø: Block Diagram of the SYS68K/DRAM-E3S6



4.1 Access Address Selection using FME Slave Boards

Due to the fact that the memory capacity is expanded using DRAM-E3SX boards (see Table 18), the access address selection has to be changed. The general calculation rules, outlined in chapter 3.2.2, are usable to reconfigure the default setup of the board.

The default access address selection of each DRAM-E3M1 board is outlined in chapter 3.2.1.

Table 19 lists the extension of the default access address selection using a DRAM-E3S1 board. Table 2Ø lists the extension using a DRAM-E3S3 board while Table 21 lists the extension with a DRAM-E3S6 board. All other modifications are similar to the listed examples.

Table 19: Access Address Selection using one DRAM-E3S1

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6			5-6		A22
		1-8				A21
						A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF2F FFFF	$2F FFFF
First not on-board Address:	$FF30 0000	$30 0000
Boundary:	$0020 0000	$20 0000
	2M byte	2M byte

Table 20: Access Address Selection using one DRAM-E3S3

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6					A22
		1-8			1-8	A21
						A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF4F FFFF	$4F FFFF
First not on-board Address:	$FF50 0000	$50 0000
Boundary:	$0040 0000	$40 0000
	4M byte	4M byte

Table 21: Access Address Selection using one DRAM-E3S6

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7					A23
	5-6			5-6		A22
		1-8			1-8	A21
					2-7	A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF7F FFFF	$7F FFFF
First not on-board Address:	$FF80 0000	$80 0000
Boundary:	$0070 0000	$70 0000
	7M byte	7M byte

Table 22: Access Address Selection using two DRAM-E3S6

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7					A23
	5-6					A22
		1-8				A21
					2-7	A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FFDF FFFF	$DF FFFF
First not on-board Address:	$FFE0 0000	$E0 0000
Boundary:	$00D0 0000	$D00 000
	13M byte	13M byte

5.Ø Preparation for Use

a) Please read the complete manual for easy and correct board handling.

b) Make optical check of the multi-layer board and the components for eventual damages prior to mounting the board.

c) Use adequate electrical outlets for check.

d) Use adequate equipment for electrical check (i.e. volt meter).

e) Use power supply with sufficient drive capacity within the VMEbus tolerances.

f) To initialize the DRAM-E3M1 and its connected slave boards an initialization routine has to be installed before reading from the board.

The following program example (subroutine) is useful for initialization:

```
STARTADR    =    first on-board address
ENDADR      =    last on-board address


START   LEA.L    STARTADR,AØ
        LEA.L    ENDADR,A1
LOOP    MOVE.L   #Ø,(AØ)+
        CMPA.L   A1,AØ
        BLT.S    LOOP
        RTS
```

Note: The initialization of the DRAM cells has to be done with long-word moves.

5.1 Power On

When the board is mounted in a VMEbus environment and the power is stable, transfers to and from the board can be forced.

Caution: If the board has not been initialized, parity errors may occur during read cycle because the data bits of the DRAMs are not in a definite state after power up.

Normal access can be forced to the default set address ranges if the following items are provided:

a) RUN/LOCAL switch is in RUN mode.

b) The current bus master can force an access to this board under the default access address range and AM code.

Access Address Range:	$FF1ØØ ØØØ	Start A32 Mode
	$FF1FF FFF	End A32 Mode
	$1ØØ ØØØ	Start A24 Mode
	$1FF FFF	End A24 Mode

Selected AM Codes:	Ø9,	ØA,	ØD,	ØE
	39,	3A,	3D,	3E

APPENDIX A

Specification SYS68K/DRAM-E3M1

Capacity:	1M byte dynamic RAM including Byte Parity Check
Organisation:	36 bit internally including 4 parity bits
Data Transfer Modes:	A24:D8 ; A24:D16 ; A24:D24 ; A24:D32 A32:D8 ; A32:D16 ; A32:D24 ; A32:D32
Access Times:	Write: 70ns (typ) with Parity generation Read: 245ns (typ) with Parity check 210ns (typ) without Parity check
Refresh:	Interleave every 15us
Decoding:	Jumper selectable Access Address in 256K byte increments and Address Modifier Code (any combination of 10 AM codes)
Specials:	Through FMEbus (up to 13M bytes)
Memory Expansion:	Battery backup through P2 RUN/LOCAL switch RUN/LOCAL & ERROR/ACCESS LEDs

Power Requirements:			
	+5V	5.9A	(refresh peak)
	+5V	4.3A	(average max)
	+5V	3.2A	(average typ)
	+5V STDBY	3.9A	(refresh peak)
	+5V STDBY	1.9A	(average max)
	+5V STDBY	1.7A	(average typ)

Operating Temperature:	0 to +60 degrees C
Storage Temperature:	-55 to +85 degrees C
Relative Humidity:	0-95% (non-condensing)
Dimensions:	Double Eurocard 233x160mm (9.2x6.3")

APPENDIX B

COMPONENT PART LIST

ICs

Location	Type	Manufacturer
J1 - J36	41256-12	NEC,HIT,FUJ
J73	74F244	MOT,F,VALVO
J75	AM2966	AMD
J76	74F373	MOT,F,VALVO
J77	74F32	MOT,F,VALVO
J78	74F38	MOT,F,VALVO
J8Ø	74F28ØA	MOT,F,VALVO
J81	74F28ØA	MOT,F,VALVO
J82	74F243	MOT,F,VALVO
J83	FRC 82	FORCE PAL 2ØL8A
J84	74F28ØA	MOT,F,VALVO
J85	74F28ØA	MOT,F,VALVO
J86	FRC 79	FORCE PAL 2ØL8A
J87	FRC 77	FORCE PAL 16L8A
J88	FRC 78	FORCE PAL 16L8A
J9Ø	74F373	MOT,F,VALVO
J91	74F373	MOT,F,VALVO
J92	74F373	MOT,F,VALVO
J93	FRC 8Ø	FORCE PAL 2ØL8A
J94	74F241	MOT,F,VALVO
J95	74F241	MOT,F,VALVO

APPENDIX B

COMPONENT PART LIST

ICs

Location	Type	Manufacturer
J96	74F241	MOT,F,VALVO
J97	74F241	MOT,F,VALVO
J98	74F112	MOT,F,VALVO
J99	74LS244	MOT,F,VALVO
J1ØØ	74LS393	MOT,F,VALVO
J1Ø5	74F74	MOT,F,VALVO
J1Ø6	74AS374	TI
J1Ø7	74AS374	TI
J1Ø8	74AS374	TI
J1Ø9	74AS374	TI
J11Ø	74AS374	TI
J111	74AS374	TI
J112	74F373	MOT,F,VAVLO
J113	74F373	MOT,F,VALVO
J114	74F373	MOT,F,VALVO
J115	74F373	MOT,F,VALVO
J116	74F373	MOT,F,VALVO
J117	74F373	MOT,F,VALVO
J118	74F85	MOT,F,VALVO
J119	74F85	MOT,F,VALVO

APPENDIX B

COMPONENT PART LIST

ICs

Location	Type	Manufacturer
J12Ø	74F85	MOT,F,VALVO
J121	74F85	MOT,F,VALVO
J122	74F85	MOT,F,VALVO
J123	74F85	MOT,F,VALVO
J124	74F85	MOT,F,VALVO
J125	74F85	MOT,F,VALVO
J126	74FØ4	MOT,F,VALVO
J127	74F11	MOT,F,VALVO
J128	74F2Ø	MOT,F,VALVO
J129	74F1Ø9	MOT,F,VALVO
J13Ø	74F1Ø9	MOT,F,VALVO
J131	74S24Ø	TI,MOT
J132	74F24Ø	MOT,F,VALVO
J133	74F112	MOT,F,VALVO
J134	DDU-7J-1ØØ	TOKO
J135	DDU-7J-2ØØ	TOKO
J136	DDU-7J-2ØØ	TOKO
J137	FRC 76	FORCE PAL 2ØL8A
J139	74F86	MOT,F,VALVO
J14Ø	74F86	MOT,F,VALVO

APPENDIX B

COMPONENT PART LIST

ICs

Location	Type	Manufacturer
J141	74LS395	MOT,F,VALVO
J142	74FØ8	MOT,F,VALVO
J143	74F38	MOT,F,VALVO
J144	74F38	MOT,F,VALVO
J145	74F13	MOT,F,VALVO
J146	74F32	MOT,F,VALVO
J147	74F132	MOT,F,VALVO
J148	74F86	MOT,F,VALVO
J149	74FØ8	MOT,F,VALVO
J151	74F11	MOT,F,VALVO
J152	74LS74AN	MOT,F,VALVO
J153	74LS74AN	MOT,F,VALVO
J154	74LS123	MOT,F,VALVO
J155	75LS24Ø	MOT,F,VALVO
J156	74F283	MOT,F,VALVO
J157	74F283	MOT,F,VALVO
J158	74F38	MOT,F,VALVO
J159	TL77Ø5	TI
J16Ø	FRC 81	FORCE PAL 16L8A

APPENDIX B

COMPONENT PART LIST

DIODES

Location	Type	Manufacturer
LD1	22Ø6	DIALIGHT GREEN
LD2	24Ø6	DIALIGHT RED
LD3	23Ø6	DIALIGHT YELLOW

APPENDIX B

COMPONENT PART LIST

RESISTORS, NETWORKS

Location	Type	Manufacturer
R1	5*33 1Ø PIN	VARIOUS
R2	5*47 1Ø PIN	VARIOUS
R3	9*4.7K 1Ø PIN	VARIOUS
R7	9*68Ø 1Ø PIN	VARIOUS
R8	9*4.7K 1Ø PIN	VARIOUS
R1Ø	9*4.7K 1Ø PIN	VARIOUS
R11	9*4.7K 1Ø PIN	VARIOUS
R12	9*4.7K 1Ø PIN	VARIOUS
R13	9*4.7K 1Ø PIN	VARIOUS
R14	9*4.7K 1Ø PIN	VARIOUS
R16	9*4.7K 1Ø PIN	VARIOUS
R17	1ØK	VARIOUS
R18	---	---
R23	5*1ØØ 1Ø PIN	VARIOUS
R27	1ØØ	VARIOUS
R4Ø	1ØØ	VARIOUS
R42	27	VARIOUS
R51	4.7K	VARIOUS
R53	9*4.7K 1Ø PIN	VARIOUS
R54	9*68Ø 1Ø PIN	VARIOUS
R69	56	VARIOUS
R7Ø	---	---
R73	5.6K Ohm	VARIOUS

APPENDIX B

COMPONENT PART LIST

CAPACITORS

Location	Type	Manufacturer
C1	10nF	VARIOUS
C2	1.8nF	VARIOUS
C3	390pF	VARIOUS
C4	10.5-60pF	VARIOUS
C5-C60	100nF	Panasonic KERAMIK
C61	100nF	VARIOUS
C62	100nF	VARIOUS
C63	100nF	VARIOUS
C64	1n	VARIOUS
C65	100uF	VARIOUS

APPENDIX B

COMPONENT PART LIST

MECHANICAL PARTS

Location	Type	Manufacturer
B2	DW16	VARIOUS
B4	DW1Ø	VARIOUS
B5	DW1Ø	VARIOUS
B6+B9	DW16	VARIOUS
B7	DW1Ø	VARIOUS
B8	DW1Ø	VARIOUS
B1Ø	EW2	VARIOUS
B11	DW14	VARIOUS
B14	DW6	VARIOUS
B18	EW2	VARIOUS
B2Ø	EW2	VARIOUS
SW1	AT-1D SWITCH	KNITTER
P1	VG CONNEC 96	VARIOUS
P2	VG1Ø3-4ØØ21	VARIOUS
P3	VG115-4ØØ62	VARIOUS
J83	24 PIN SOCKET	VARIOUS
J86	24 PIN SOCKET	VARIOUS
J87	2Ø PIN SOCKET	VARIOUS
J88	2Ø PIN SOCKET	VARIOUS
J93	24 PIN SOCKET	VARIOUS
J137	24 PIN SOCKET	VARIOUS
J16Ø	2Ø PIN SOCKET	VARIOUS

APPENDIX B

COMPONENT PART LIST

MECHANICAL PARTS

	ATTACHED PARTS
1)	SYS68K/DRAM-E3M1/HUM Hardware User's Manual
2)	Product Release Note

APPENDIX C

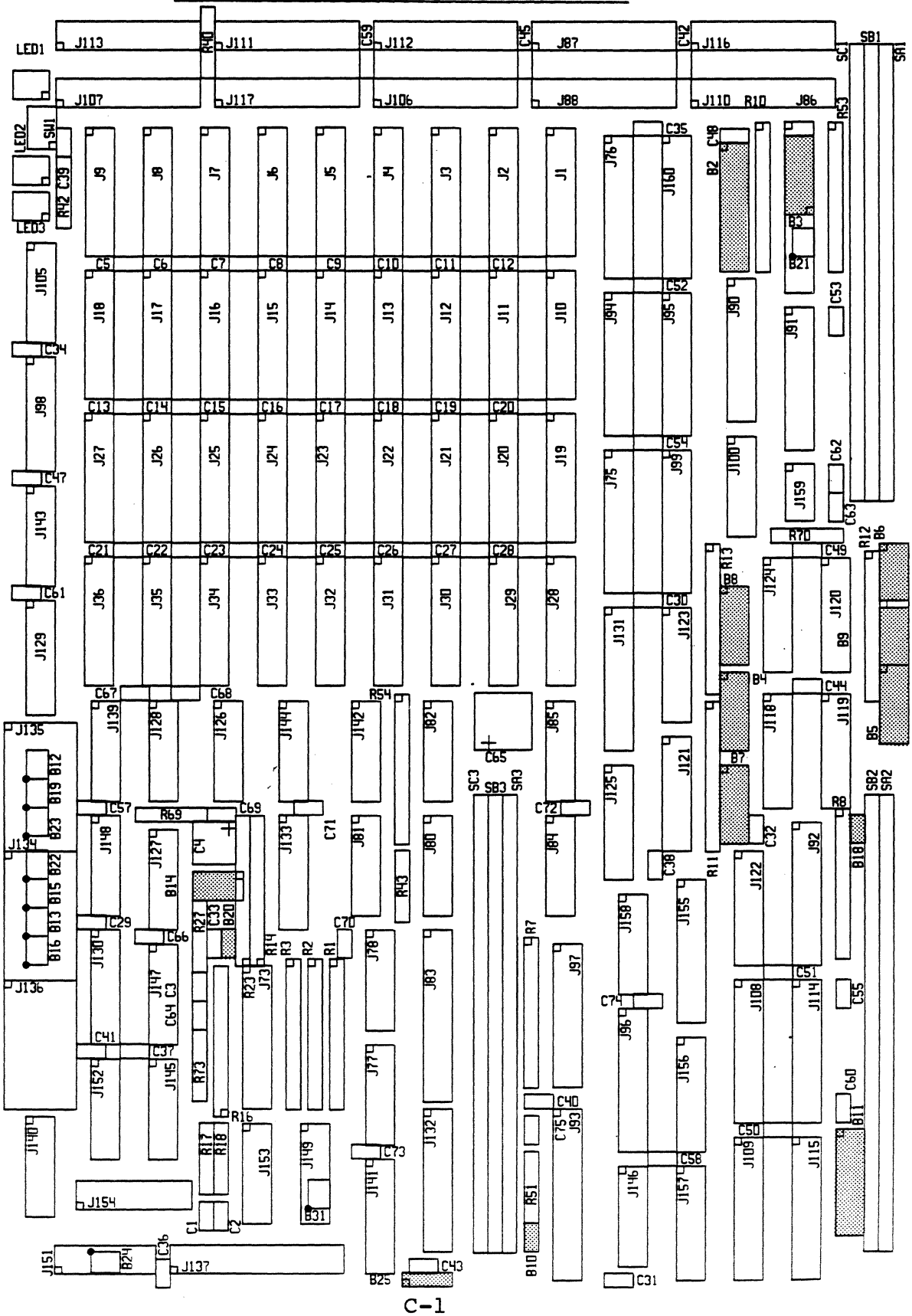
Description of the Jumperfields

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x y	see pg.
B2	Address Modifier Code Selection	1-16 2-15 3-14 4-13	6-Ø1	162/29	28
B3	Address Modifier Code Selection	5-12 6-11 7-1Ø 8-9		152/16	28
B4 +B5 +B6	Access Address Selection First not on board Address (MAD)	4-7 5-6 2-7 3-6 4-5	5-A1	89/29 9Ø/6 1Ø7/6	17
B7 +B8 +B9	Access Address Selection First on board address Start address (LAD)	4-7 5-6 1-8 3-6 4-7	5-A3	75/29 1Ø5/29 95/6	17
B1Ø	Bank Select Modes	-	3-A2	14/55	-
B11	Battery Backup Option	1-14 2-13 3-12	2-B4	25/12	4Ø
B12	RAM Timing	2-3	7-B4	76/124	-
B13	RAM Timing	2-3	7-B3	54/124	-
B14	Read Access Select	2-5	7-A4	6Ø/94	36

- for internal use only.

APPENDIX C

Description of the Jumperfields



APPENDIX C

Description of the Jumperfields

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B2	Address Modifier Code Selection	1-16 2-15 3-14 4-13 5-12 6-11 7-10 8- 9	6-01	162/29		28

Default: B2 all Jumpers IN

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B3	Address Modifier Code Selection	-	6-01	162/29		28

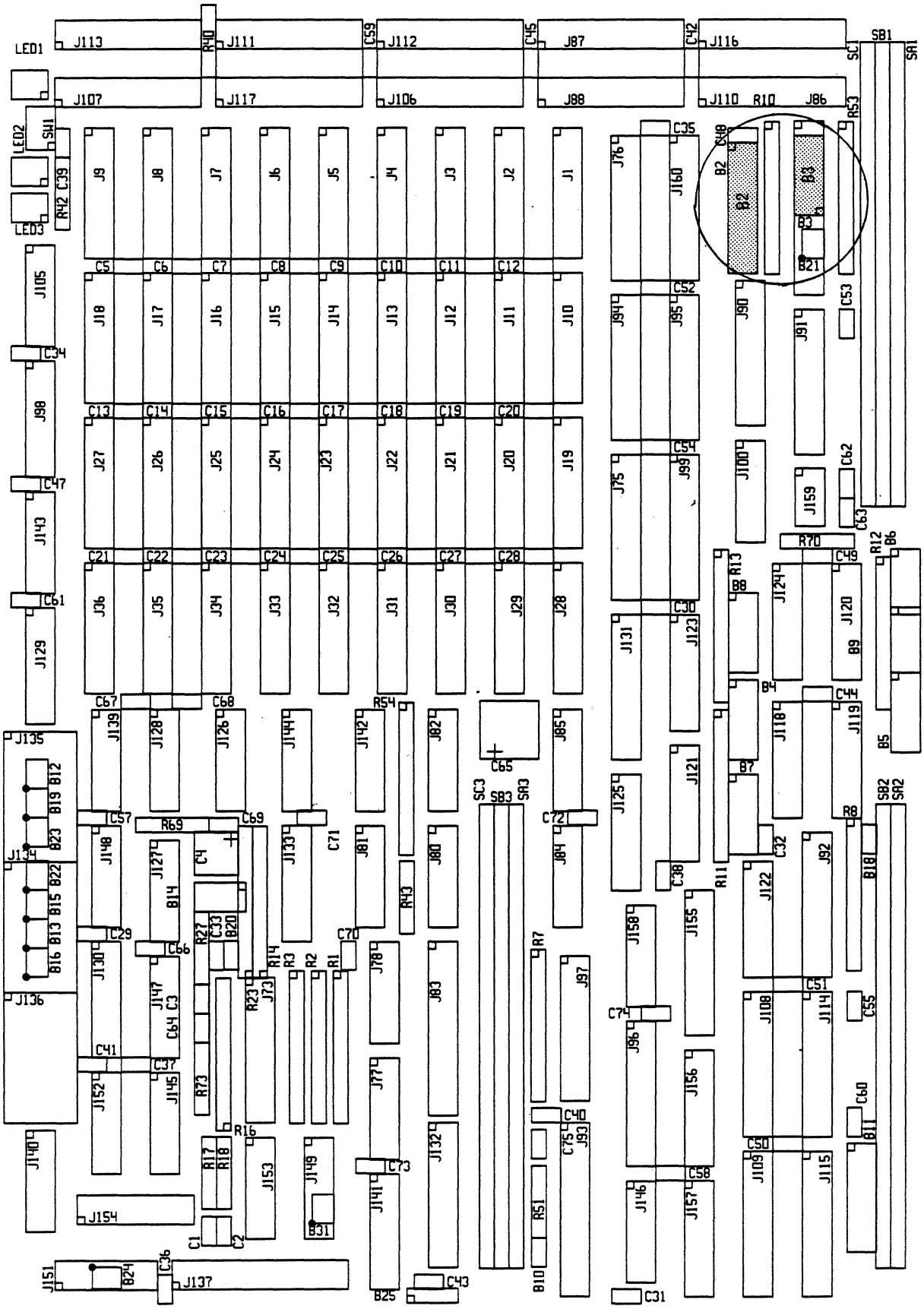
Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B21	Address Modifier Code	-	6-C2	147/18		-

- for internal use only.

B3 and B21 are only connected with soldering bridges.

APPENDIX C

Description of the Jumperfields



APPENDIX C

Description of the Jumperfields

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B4		-				
+B5	Access Address Selection First not on board Address (MAD)	4-7 5-6	5-A1	89/29 90/6 107/6		17
+B6		2-7 3-6 4-7				
B7		-				
+B8	Access Address Selection First on board address Start address (LAD)	4-7 5-6	5-A3	75/29 105/29 95/6		17
+B9		1-8 3-6 4-7				

Default Address: For 24 Bit B18 OUT

First not on board	$	XX10	0000
First not on board	$	XX20	0000

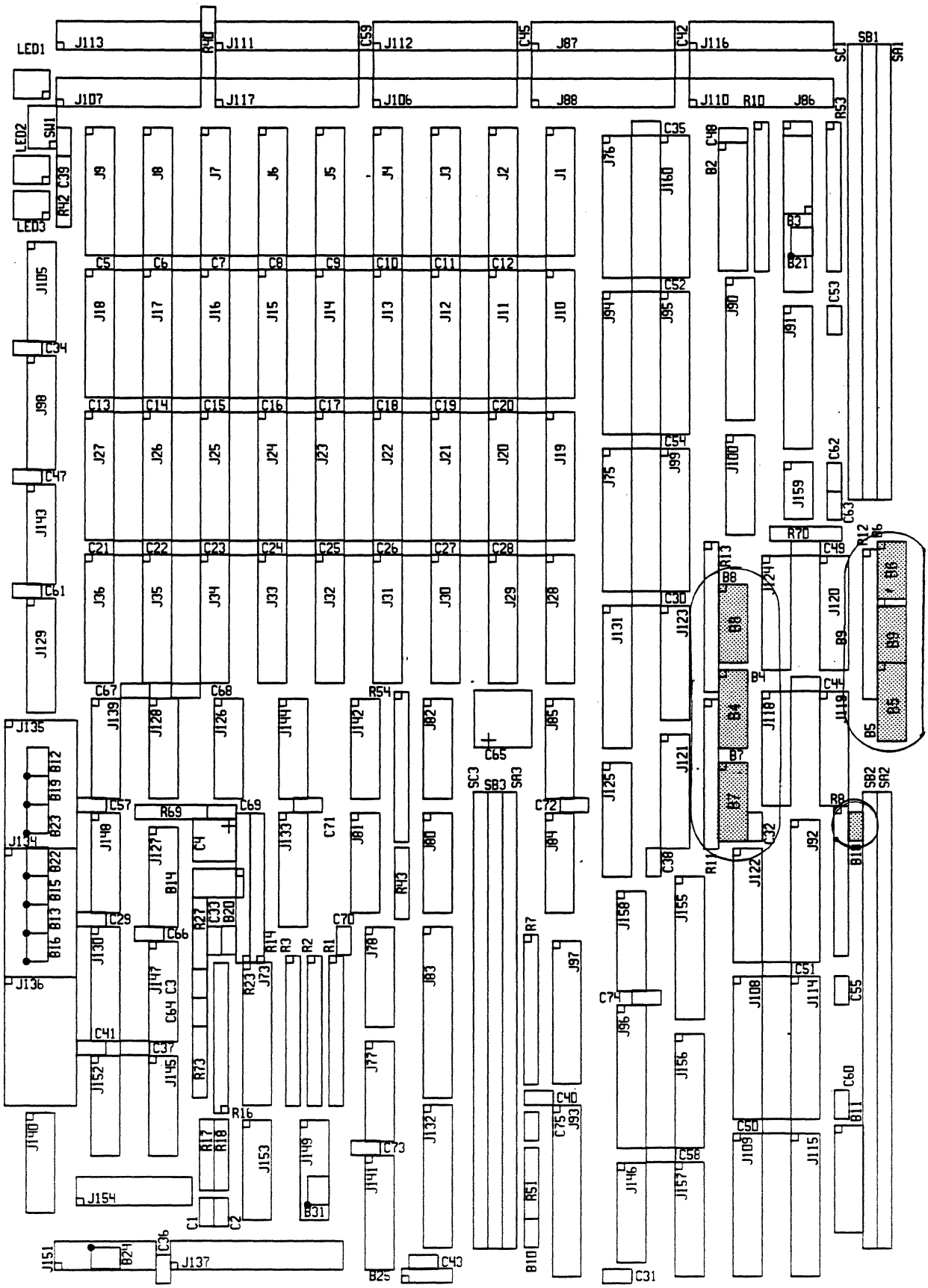
For 32 Bit B18 IN

First not on board	$	FF10	0000
First on board	$	FF20	0000

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B18	Disable/Enable Address Lines A24-A31	-	3-B2	69/10		19

APPENDIX C

Description of the Jumperfields



APPENDIX C

Description of the Jumperfields

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B1Ø	Bank Select Modes	-	3-A2	14/55		-
B11	Battery Backup Option	-	2-B4	25/12		4Ø

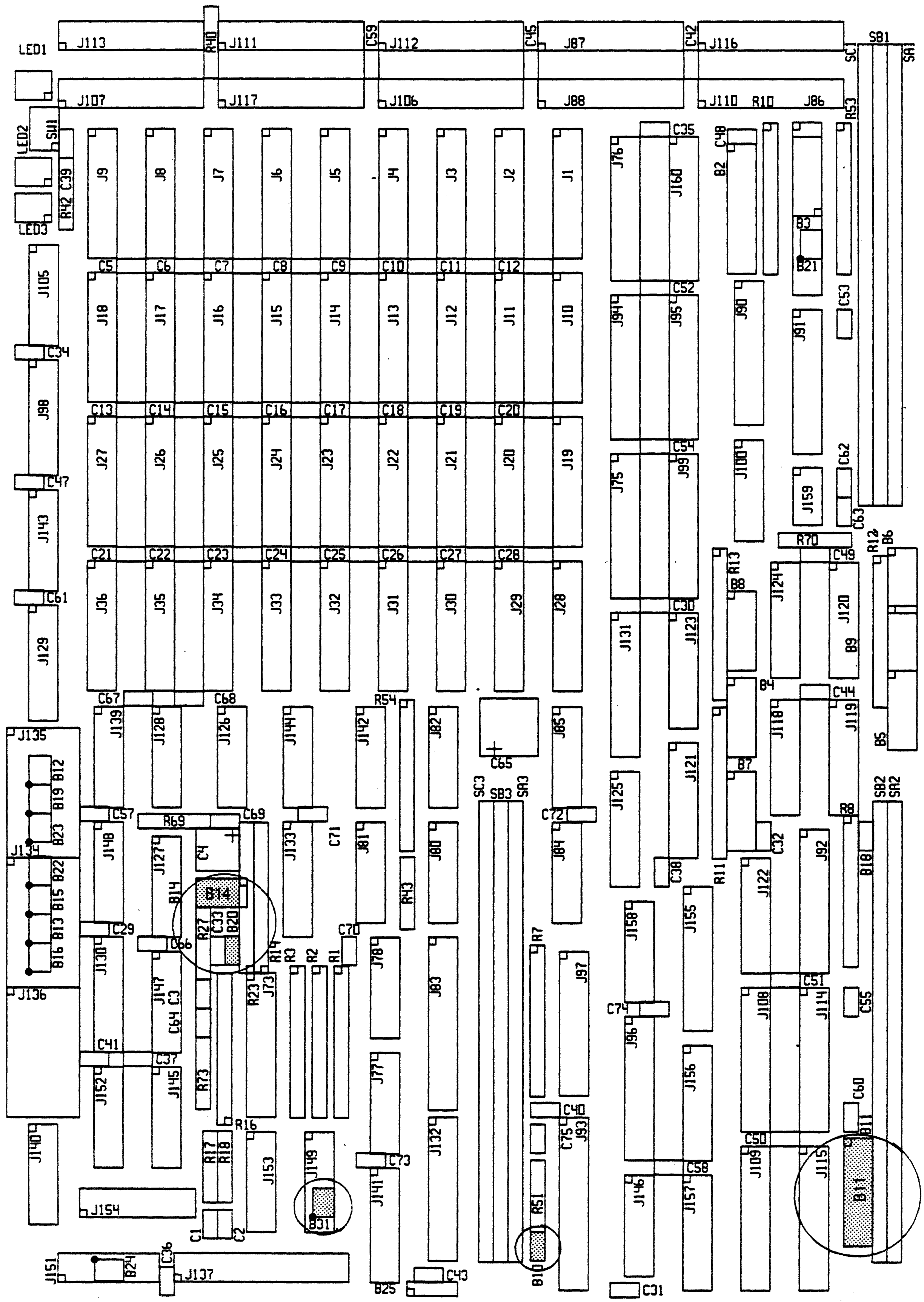
Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B14	Read Access Select	1 6 2-5 3-4	7-A4	6Ø/94		36
B2Ø	Parity Error to BERR	1-2	2C-3	54/96		36

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B25	AS*	1 O	2-C1	15/86		-
	Start	2 O |				
	AS* and DSO* or DS1	3 O				

- for internal use only.

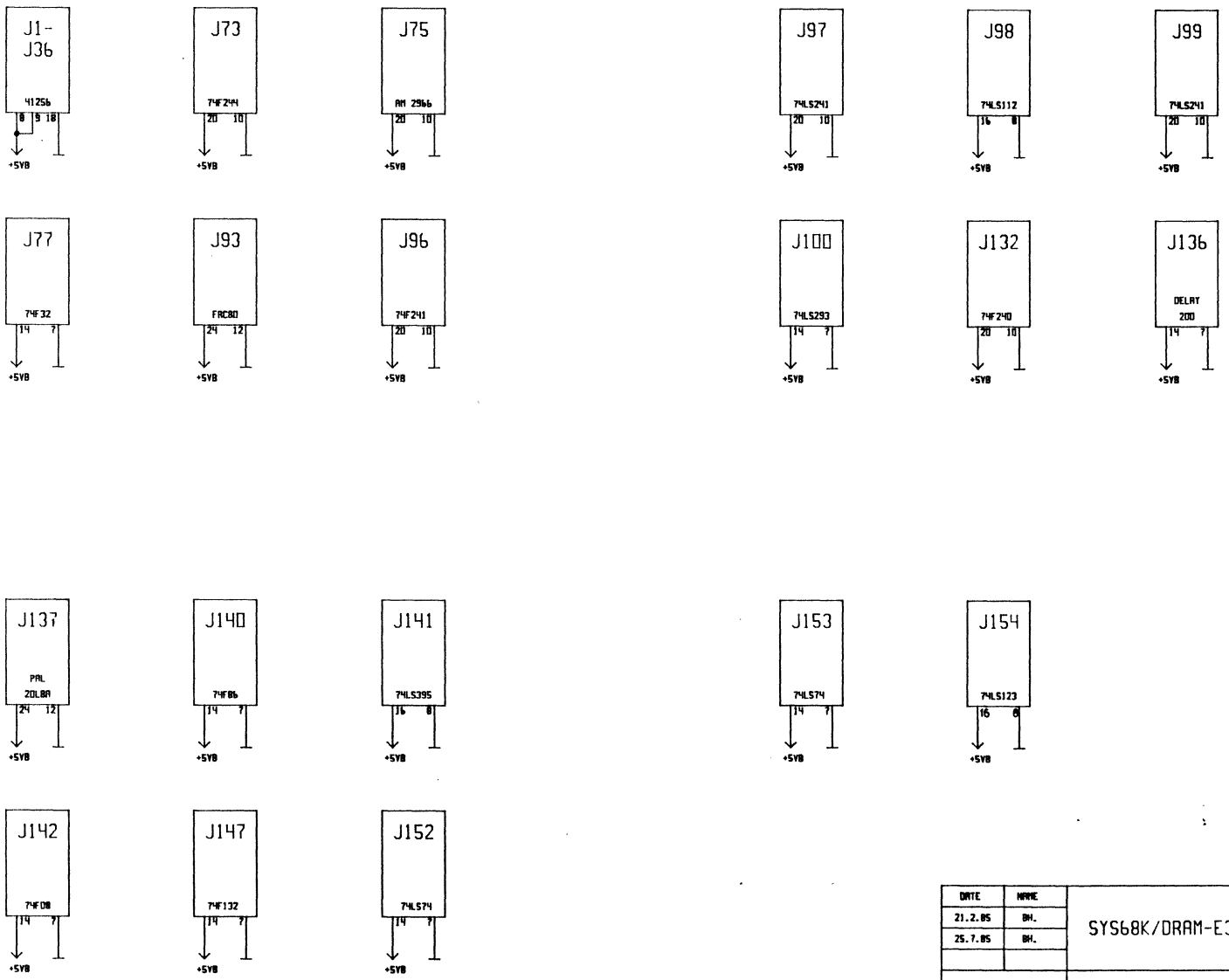
APPENDIX C

Description of the Jumperfields

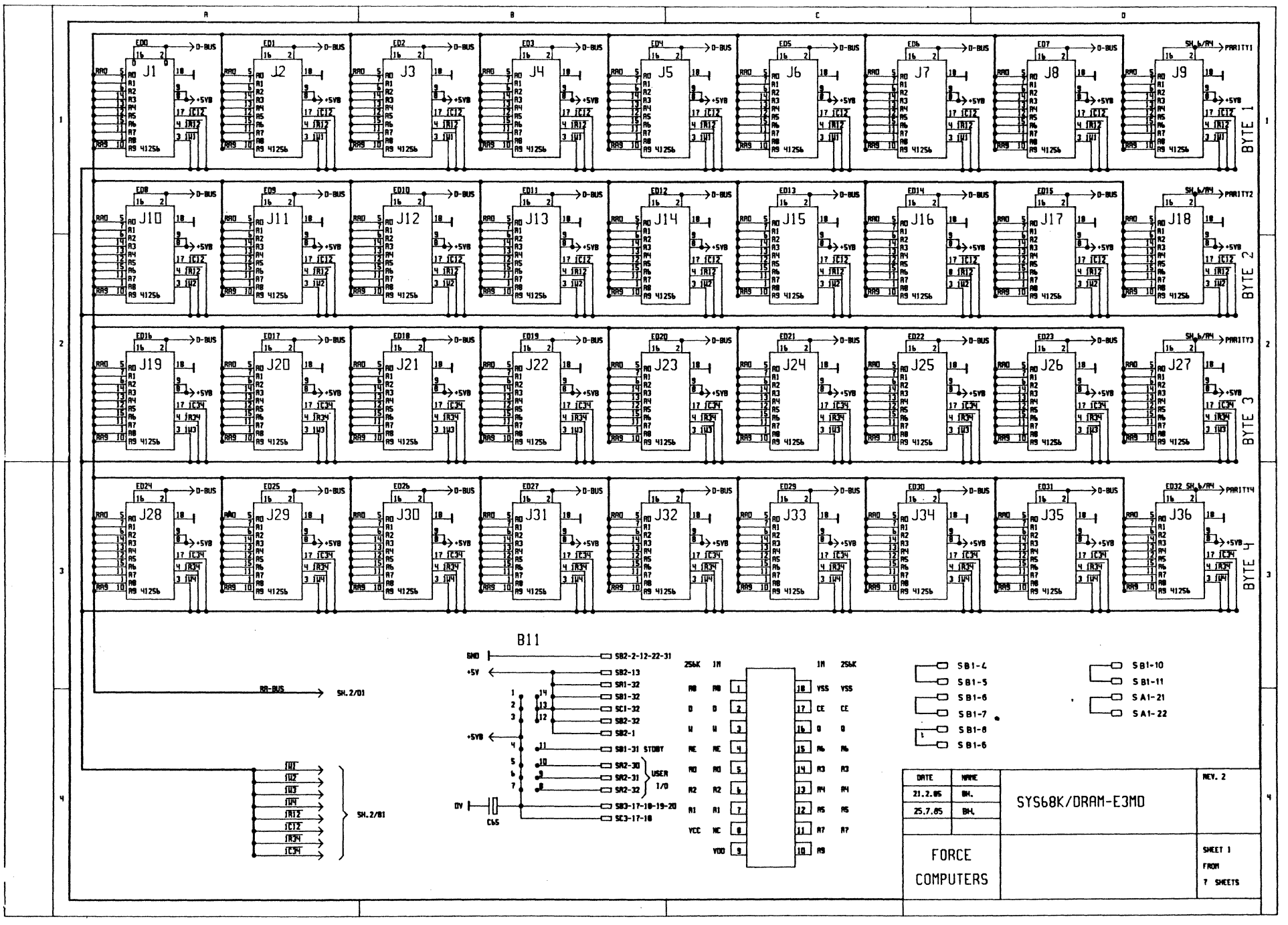


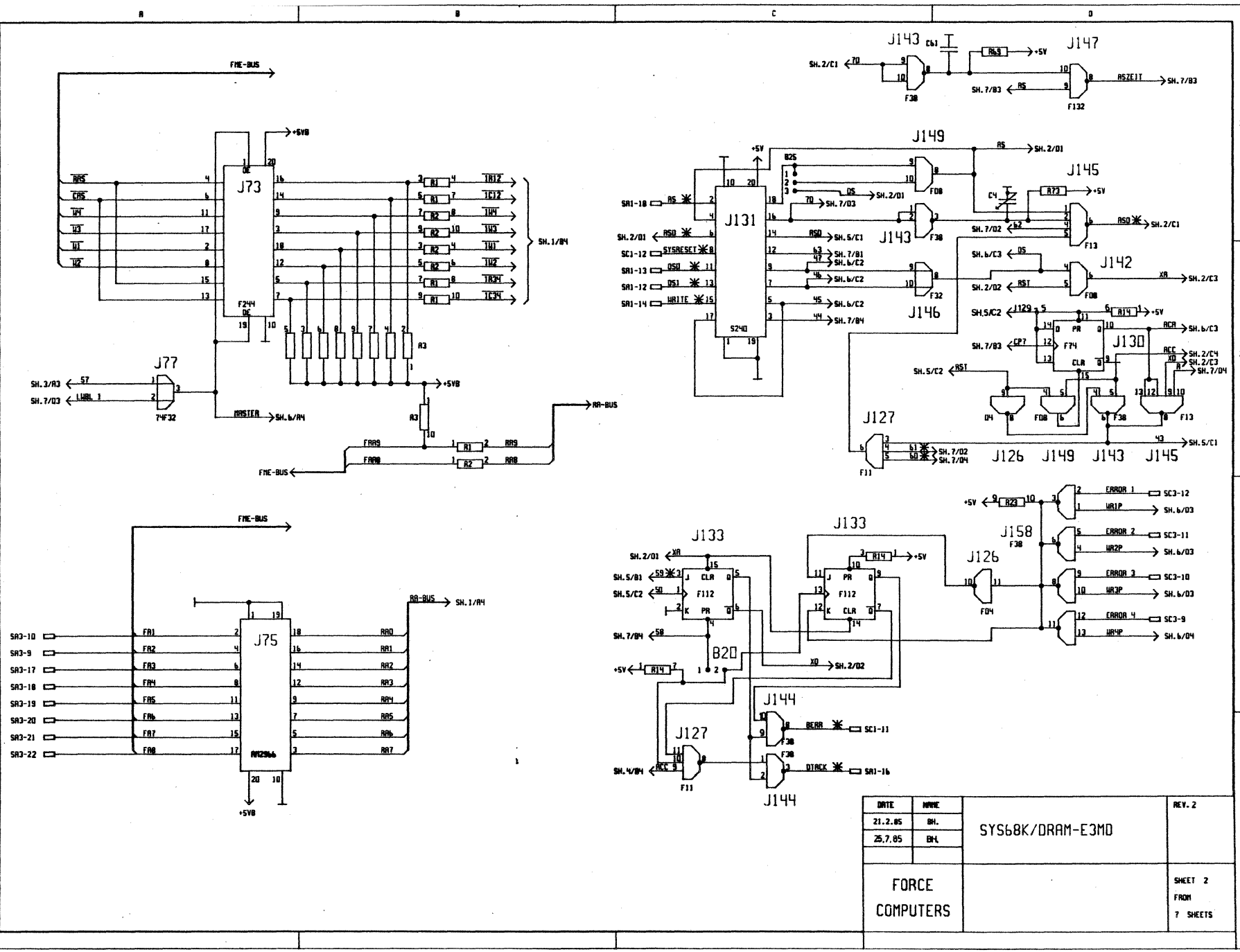
APPENDIX D

Circuit Schematics

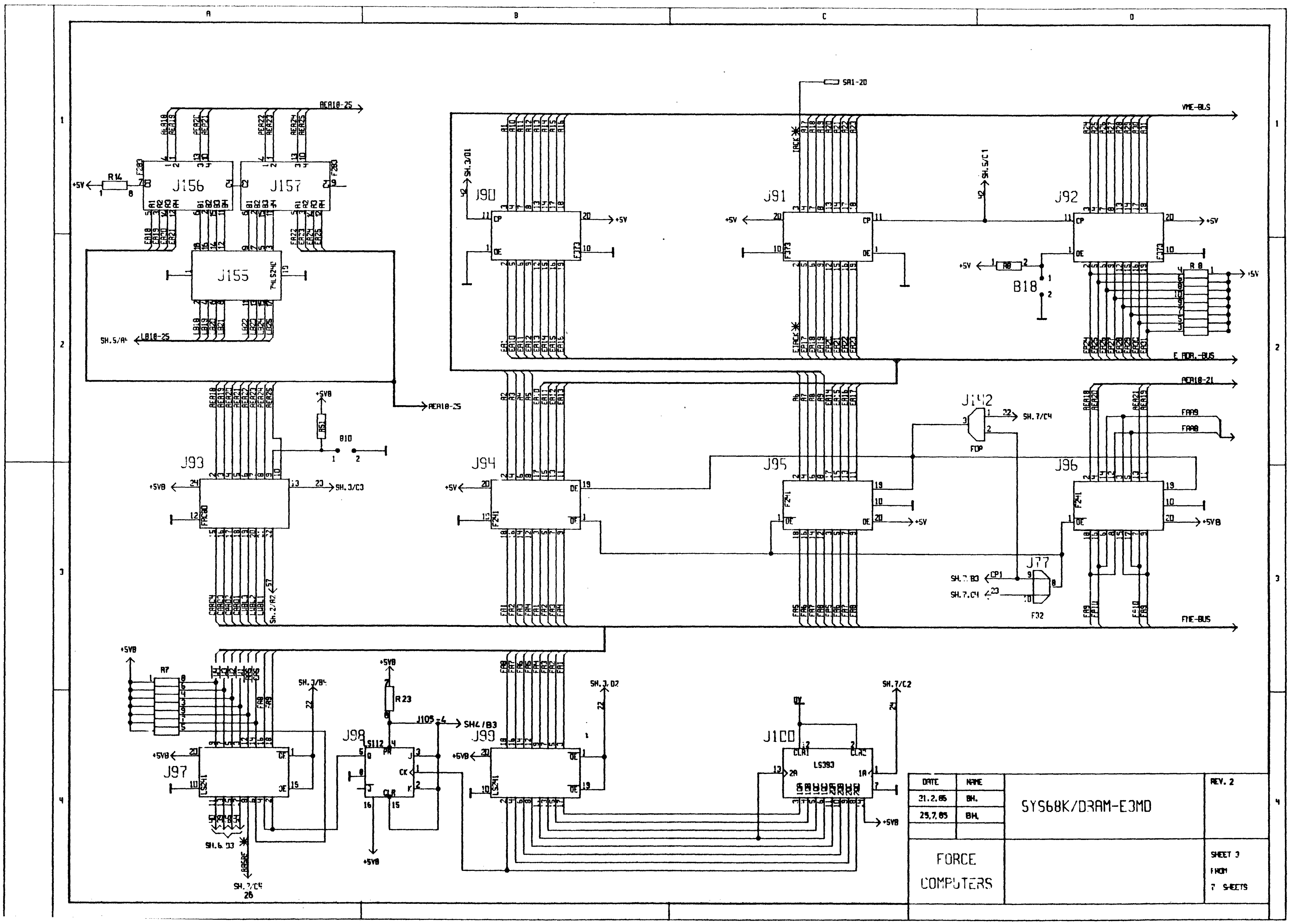


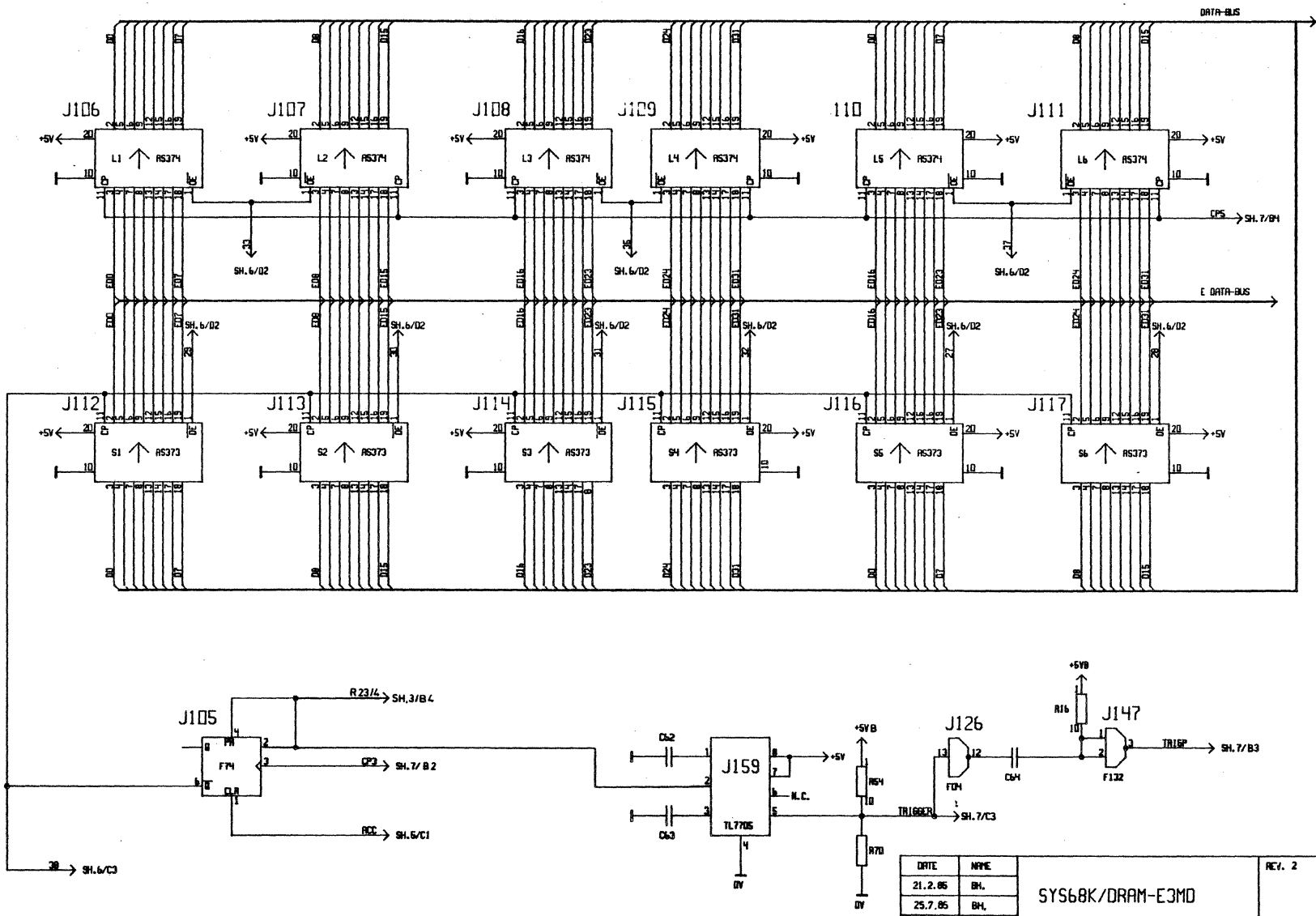
DATE	NAME		REV. 2
21.2.85	BH.	SYS68K/DRAM-E3MD	
25.7.85	BH.		
FORCE COMPUTERS			SHEET 1 FROM 1 SHEETS


ED0 D-BUS J1 +5VB BYTE 1
ED8 D-BUS J10 +5VB BYTE 2
ED16 D-BUS J19 +5VB BYTE 3
ED24 D-BUS J28 +5VB BYTE 4
SH.2/01
SH.2/B1
B11
GND
+5V
SB2-2-12-22-31
SB2-13
SR1-32
SB1-32
SC1-32
SB2-32
SB2-1
SB1-31 STDBY
SR2-30
SR2-31
SR2-32
USER I/O
SB3-17-18-19-20
SC3-17-18
C65
SB1-4
SB1-5
SB1-6
SB1-7
SB1-8
SB1-9
SB1-10
SB1-11
SA1-21
SA1-22
SYS68K/DRAM-E3MD
REV. 2
DATE
NAME
21.2.05
BH.
25.7.05
BH.
FORCE COMPUTERS
SHEET 1 FROM 7 SHEETS

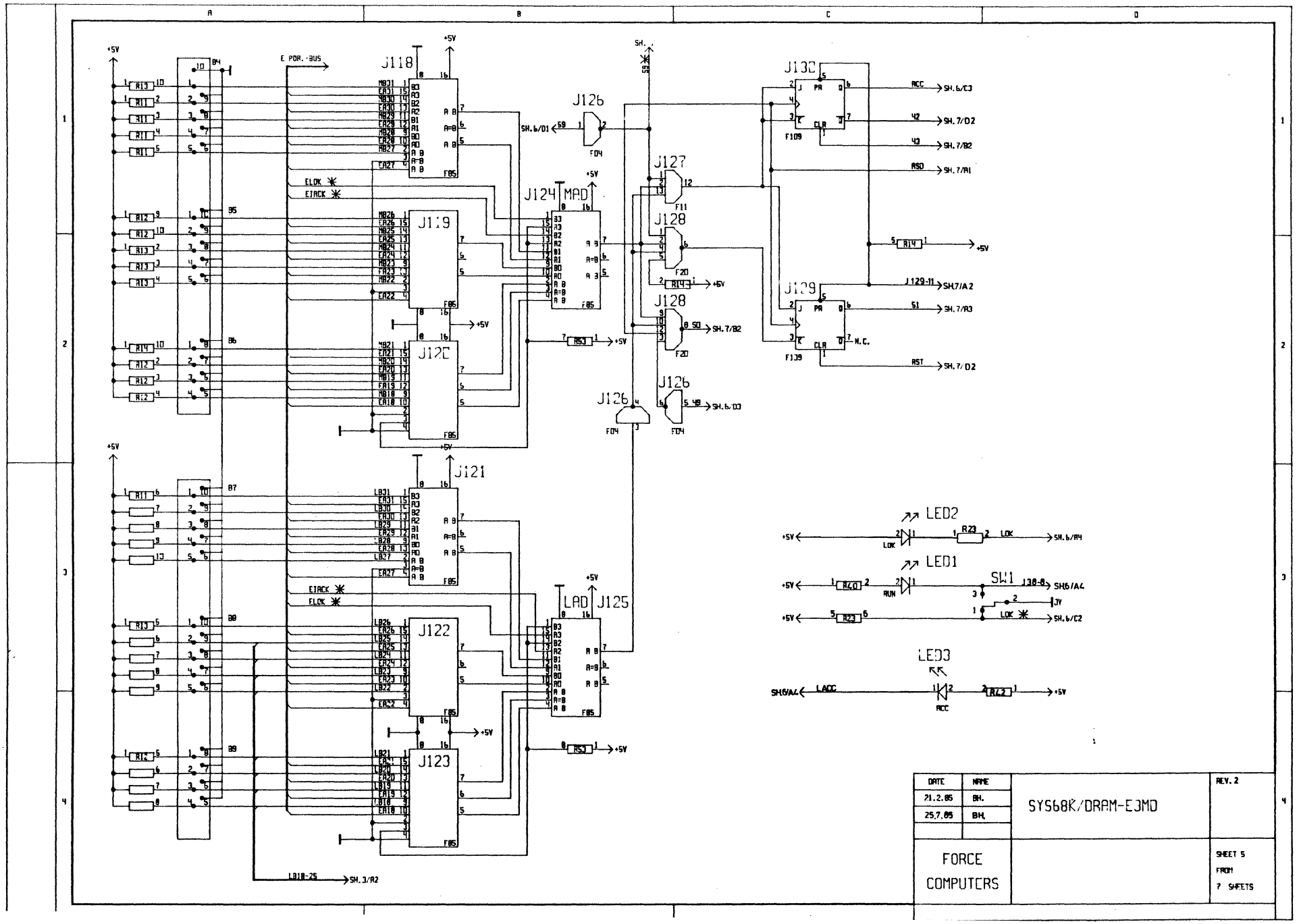


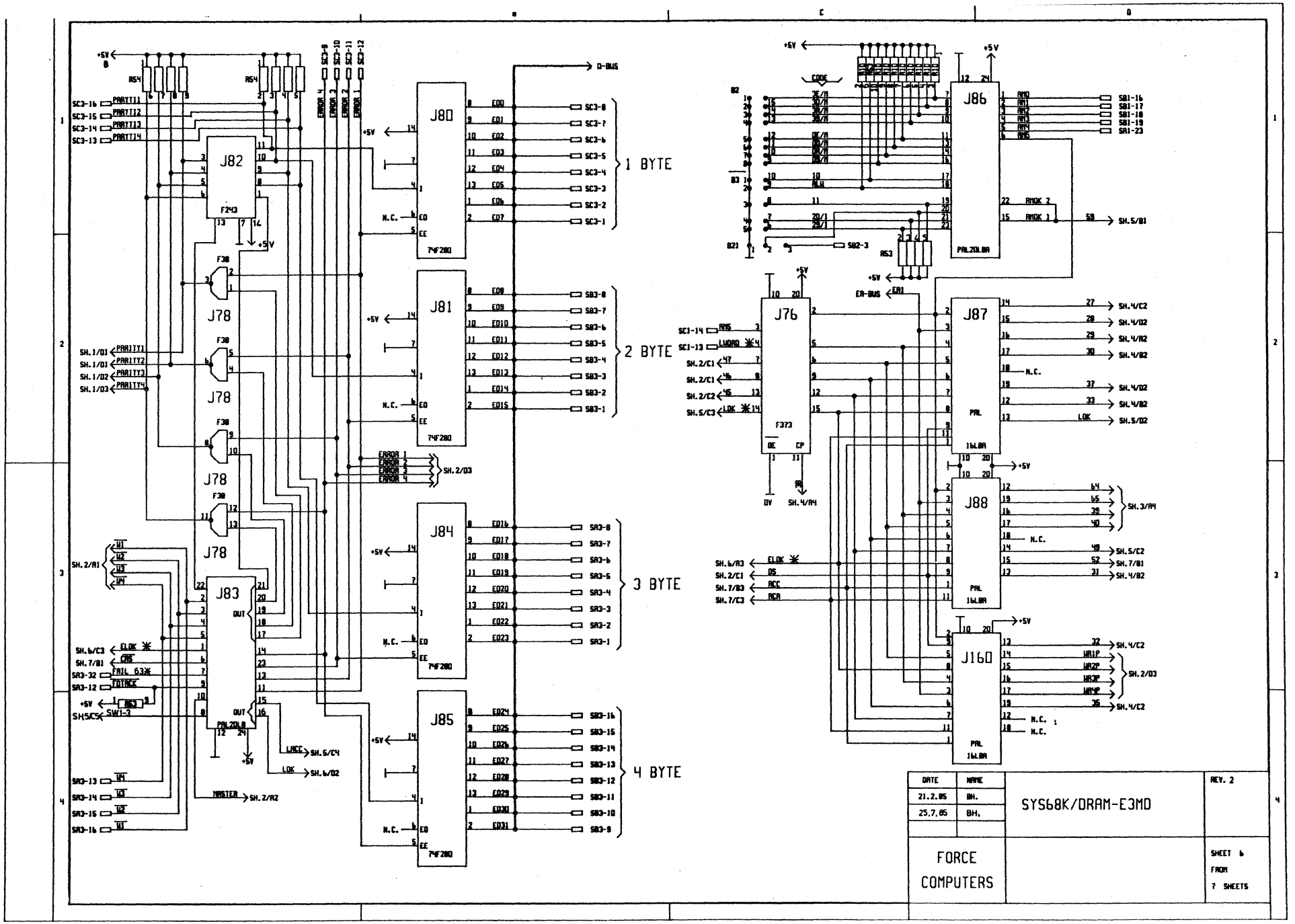
DATE	NAME		REV. 2
21.2.85	BH.	SYS68K/DRAM-E3MD	
25.7.85	BH.		
FORCE COMPUTERS			SHEET 2 FROM 7 SHEETS

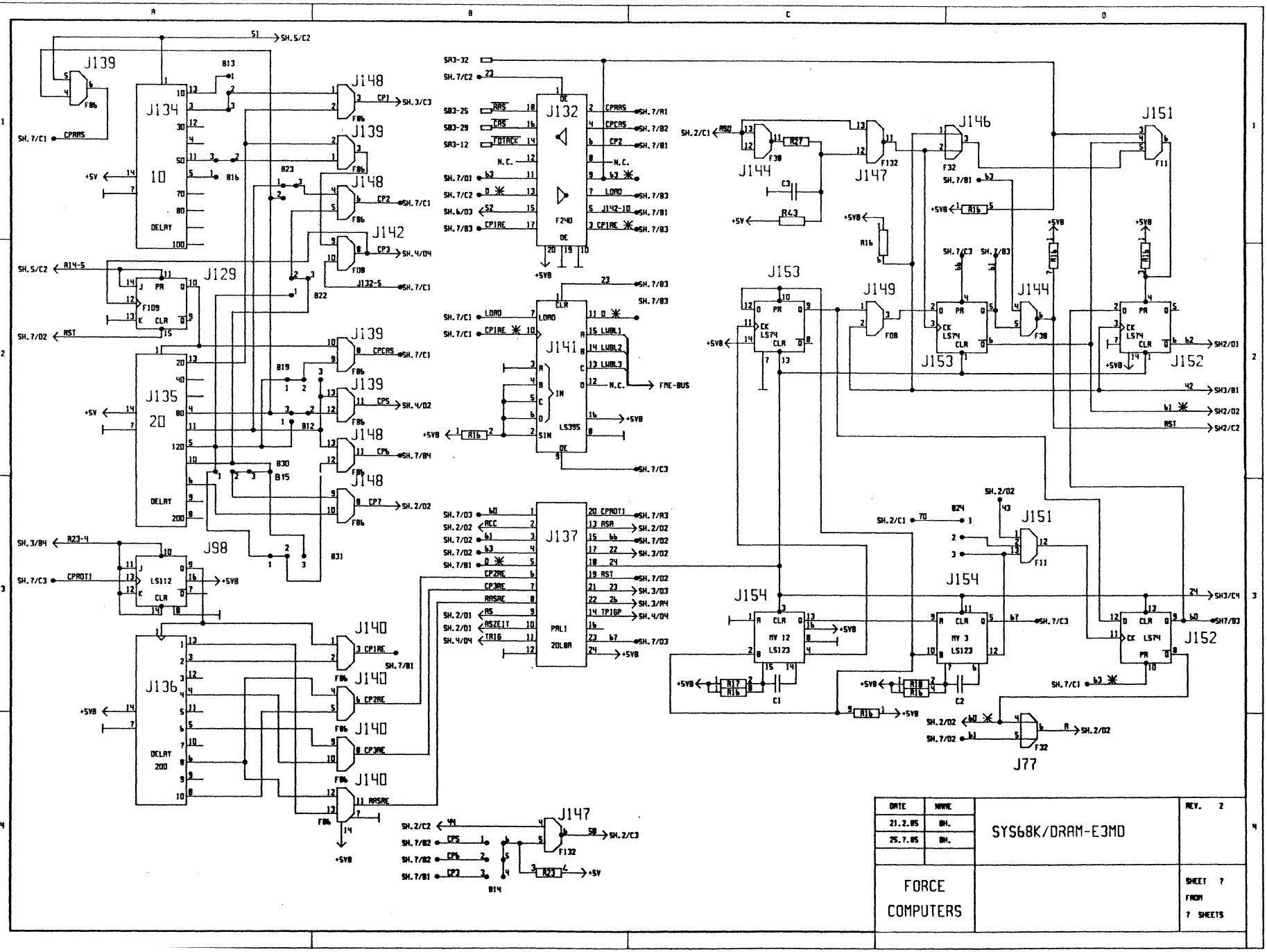

SYS68K/DRAM-E3MD
FORCE COMPUTERS
DATE
NAME
21.2.85
BH.
25.7.85
BH.
REV. 2
SHEET 3
FROM
7 SHEETS
VME-BUS
E ADR.-BUS
FME-BUS
AEA18-25
AEA18-21
J90
J91
J92
J93
J94
J95
J96
J97
J98
J99
J100
J142
J77
J155
J156
J157
74LS240
LS393
LS241
F241
F373
F283
R14
R51
R23
R7
R8
B10
B18



DATE	NAME		REV. 2
21.2.86	BH.	SYS68K/DRAM-E3MD	
25.7.86	BH.		
FORCE COMPUTERS			SHEET 4 FROM 7 SHEETS


E POR.-BUS
J118
J119
J120
J121
J122
J123
J124 MAD
J125 LAD
J126
J127
J128
J129
J130
ELOK
ETACK
FLOK
LED2
LED1
LED3
SW1
R23
RUN
LOK
LACC
ACC
RST
SYS68K/DRAM-E3MD
DATE
NAME
21.2.89 BH.
25.7.89 BH.
REV. 2
FORCE COMPUTERS
SHEET 5 FROM 7 SHEETS


D-BUS
J80
J81
J84
J85
J82
J83
J86
J87
J88
J160
J76
J78
1 BYTE
2 BYTE
3 BYTE
4 BYTE
F243
F373
74F280
PAL20L8A
PAL
16L8A
SH.2/03
SH.3/04
SH.4/C2
SH.4/02
SH.4/82
SH.5/81
SH.5/02
SH.5/C2
SH.7/81
SH.4/82
SH.2/03
SH.5/C4
SH.6/02
SH.2/82
SH.4/84
SH.6/C3
SH.7/81
SH.2/81
SH5/CS
SWI-3
SB2-3
SB1-16
SB1-17
SB1-18
SB1-19
SB1-23
DATE
NAME
21.2.85
BH.
25.7.85
BH.
SYS68K/DRAM-E3MD
REV. 2
FORCE
COMPUTERS
SHEET 6
FROM
7 SHEETS


J139
J134
10
DELAY
J148
J139
J148
J142
J129
J139
J135
20
DELAY
J139
J148
J148
J98
LS112
J136
DELAY
200
J140
J140
J140
J140
J132
F240
J141
LS395
J137
PAL1
20L8A
J147
F132
J144
F30
J147
F32
J146
J151
F11
J153
J149
F08
J144
F30
J153
J152
J154
MY 12
LS123
J154
MY 3
LS123
J151
F11
J152
J77
F32
SH.5/C2
SH.7/C1
CPRAS
SH.7/D2
RST
SH.3/B4
CPROT1
SH.7/C3
SH.2/D2
SH.2/C1
SH.2/D1
SH.7/B1
SH.7/A1
SH.7/B2
SH.7/B3
SH.7/A3
SH.2/B2
SH.3/D2
SH.7/D2
SH.3/A4
SH.3/D3
SH.4/D4
SH.2/C3
SH.3/C3
SH.7/B4
SH.4/D2
SH.3/B1
SH.2/B2
SH.2/C2
SH.3/C4
SH.7/B3
FME-BUS
+5V
+5VB
DATE
NAME
21.2.85
BH.
25.7.85
BH.
SYS68K/DRAM-E3MD
REV. 2
FORCE COMPUTERS
SHEET 7 FROM 7 SHEETS

APPENDIX E

P3 Pin Assignment to FME Interface

Component Side

PIN NUMBER	ROW C SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW A SIGNAL MNEMONIC
1	Byte 1/7	Byte 2/7	Byte 3/7
2	Byte 1/6	Byte 2/6	Byte 3/6
3	Byte 1/5	Byte 2/5	Byte 3/5
4	Byte 1/4	Byte 2/4	Byte 3/4
5	Byte 1/3	Byte 2/3	Byte 3/3
6	Byte 1/2	Byte 2/2	Byte 3/2
7	Byte 1/1	Byte 2/1	Byte 3/1
8	Byte 1/Ø	Byte 2/Ø	Byte 3/Ø
9	Error 4	Byte 4/7	Address 2
1Ø	Error 3	Byte 4/6	Address 1
11	Error 2	Byte 4/5	EFDTACK*
12	Error 1	Byte 4/4	FDTACK*
13	Parity 4	Byte 4/3	WR 4
14	Parity 3	Byte 4/2	WR 3
15	Parity 2	Byte 4/1	WR 2
16	Parity 1	Byte 4/Ø	WR 1
17	+5V BATT.	+5V-	Address 3
18	+5V BATT.	+5V |-BATT.	Address 4
19	Reserved	+5V |	Address 5
2Ø	ØV	+5V-	Address 6
21	ØV	Reserved	Address 7
22	ØV	ØV	Address 8
23	Address 11	ØV	Address 9
24	Address 12	ØV	Address 1Ø
25	Address 13	RAS 1	LWBL 3
26	Address 14	RAS 2	LWBL 2
27	Address 15	RAS 3	LWBL 1
28	Address 16	RAS 4	Card 1(Block 1)
29	Address 17	CAS 1	Card 2(Block 2)
3Ø	Address 18	CAS 2	Card 3(Slave 2)
31	Address 19	CAS 3	Card 4(Slave 1)
32	Address 2Ø	CAS 4	FAIL

P3 Pin Assignments to FME Interface

Backside

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	Byte 3/7	Byte 2/7	Byte 1/7
2	Byte 3/6	Byte 2/6	Byte 1/6
3	Byte 3/5	Byte 2/5	Byte 1/5
4	Byte 3/4	Byte 2/4	Byte 1/4
5	Byte 3/3	Byte 2/3	Byte 1/3
6	Byte 3/2	Byte 2/2	Byte 1/2
7	Byte 3/1	Byte 2/1	Byte 1/1
8	Byte 3/Ø	Byte 2/Ø	Byte 1/Ø
9	Address 2	Byte 4/7	Error 4
1Ø	Address 1	Byte 4/6	Error 3
11	EFDTACK*	Byte 4/5	Error 2
12	FDTACK*	Byte 4/4	Error 1
13	WR 4	Byte 4/3	Parity 4
14	WR 3	Byte 4/2	Parity 3
15	WR 2	Byte 4/1	Parity 2
16	WR 1	Byte 4/Ø	Parity 1
17	Address 3	+5V-	+5V BATT.
18	Address 4	+5V |-BATT.	+5V BATT.
19	Address 5	+5V |	Reserved
2Ø	Address 6	+5V-	ØV
21	Address 7	Reserved	ØV
22	Address 8	ØV	ØV
23	Address 9	ØV	Address 11
24	Address 1Ø	ØV	Address 12
25	LWBL 3	RAS 1	Address 13
26	LWBL 2	RAS 2	Address 14
27	LWBL 1	RAS 3	Address 15
28	Card 1(Block 1)	RAS 4	Address 16
29	Card 2(Block 2)	CAS 1	Address 17
3Ø	Card 3(Slave 2)	CAS 2	Address 18
31	Card 4(Slave 1)	CAS 3	Address 19
32	FAIL	CAS 4	Address 2Ø

P1 Pin Assignments to VMEbus

PIN Number	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	DØØ	-	DØ8
2	DØ1	-	DØ9
3	DØ2	-	D1Ø
4	DØ3	BGØIN* (1)	D11
5	DØ4	BGØOUT* (1)	D12
6	DØ5	BG1IN* (1)	D13
7	DØ6	BG1OUT* (1)	D14
8	DØ7	BG2IN* (1)	D15
9	GND	BG2OUT* (1)	GND
1Ø	SYSCLK	BG3IN* (1)	-
11	GND	BG3OUT* (1)	BERR*
12	DS1*	-	SYSRESET*
13	DSØ*	-	LWORD*
14	WRITE*	-	AM5
15	GND	-	A23
16	DTACK*	AMØ	A22
17	GND	AM1	A21
18	AS*	AM2	A2Ø
19	GND	AM3	A19
2Ø	-	GND	A18
21	IACKIN* (1)	-	A17
22	IACKOUT* (1)	-	A16
23	AM4	GND	A15
24	AØ7	-	A14
25	AØ6	-	A13
26	AØ5	-	A12
27	AØ4	-	A11
28	AØ3	-	A1Ø
29	AØ2	-	AØ9
3Ø	AØ1	-	AØ8
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

Note (1): IN to OUT Connected

P2 Pin Assignments to VMEbus

PIN Number	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	-	+5V Volts	-
2	-	GND	-
3	-	RESERVED	-
4	-	A24	-
5	-	A25	-
6	-	A26	-
7	-	A27	-
8	-	A28	-
9	-	A29	-
10	-	A30	-
11	-	A31	-
12	-	GND	-
13	-	+5 Volts	-
14	-	D16	-
15	-	D17	-
16	-	D18	-
17	-	D19	-
18	-	D20	-
19	-	D21	-
20	-	D22	-
21	-	D23	-
22	-	GND	-
23	-	D24	-
24	-	D25	-
25	-	D26	-
26	-	D27	-
27	-	D28	-
28	-	D29	-
29	-	D30	-
30	User I/O	D31	-
31	User I/O	GND	-
32	User I/O	+5 Volts	-

User I/O for standby power connection.

APPENDIX F

PRODUCT ERROR REPORT

DEAR CUSTOMER,

WHILE FORCE COMPUTERS HAS ACHIEVED A VERY HIGH STANDARD OF QUALITY IN OUR PRODUCTS AND DOCUMENTATION, WE CONTINUALLY SEEK SUGGESTIONS FOR IMPROVEMENTS.

WE WOULD APPRECIATE ANY FEEDBACK YOU CARE TO OFFER.

PLEASE USE ATTACHED "PRODUCT ERROR REPORT" FORM FOR YOUR COMMENTS AND RETURN IT TO ONE OF OUR FORCE COMPUTERS OFFICES.

SINCERELY

FORCE COMPUTERS

P R O D U C T E R R O R R E P O R T

HARDWARE/SOFTWARE/SYSTEMS

PRODUCT : _____

SERIAL NO. : _____

DATE OF PURCHASE : _____

ORIGINATOR : _____

COMPANY : _____

ADDRESS : _____

_____

_____

DATE : _____

TELEPHONE : ( ) _____ EXT _____

CONTACT : _____

This box to be completed by FORCE
DATE : _____
PR# : _____
ACTION BY :
Engineering ( )
Marketing ( )
Production ( )

AFFECTED PRODUCT: ( ) SOFTWARE ( ) HARDWARE ( ) SYSTEM

AFFECTED DOCUMENTATION: ( ) SOFTWARE ( ) HARDWARE ( ) SYSTEM

ERROR DESCRIPTION : _____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

SEND TO :

FORCE Computers Inc.
Marketing
727 University Avenue
Los Gatos, CA 95030
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FORCE Computers GmbH
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FORCE Computers FRANCE
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92100 Boulogne
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