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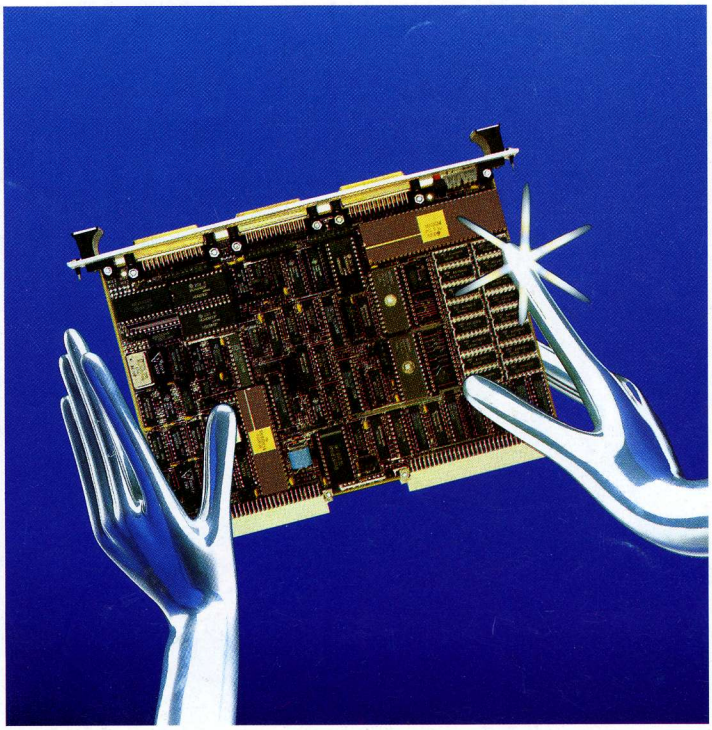
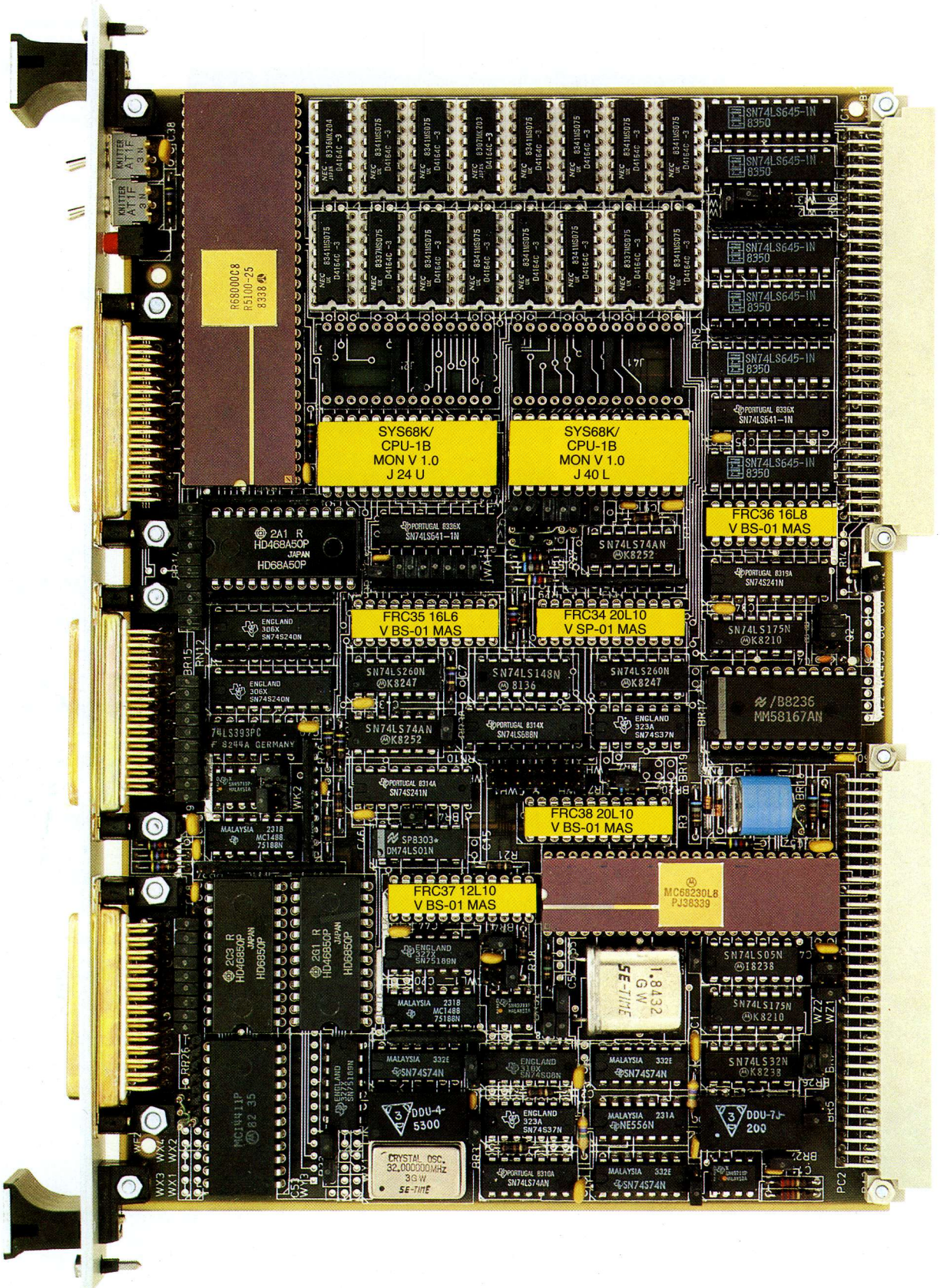


System 68000 VME
SYS68K/CPU-1B
CPU-Board


SYS68K/
CPU-1B
MON V 1.0
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SYS68K/
CPU-1B
MON V 1.0
J 40 L
FRC36 16L8
V BS-01 MAS
FRC35 16L6
V BS-01 MAS
FRC34 20L10
V SP-01 MAS
FRC38 20L10
V BS-01 MAS
FRC37 12L10
V BS-01 MAS

General Description SYS68K/CPU-1B/C

The SYS68K/CPU-1B/C Board is a high performance, low-cost system computer board based on the 68000 CPU and the VME-bus for high speed real time applications.

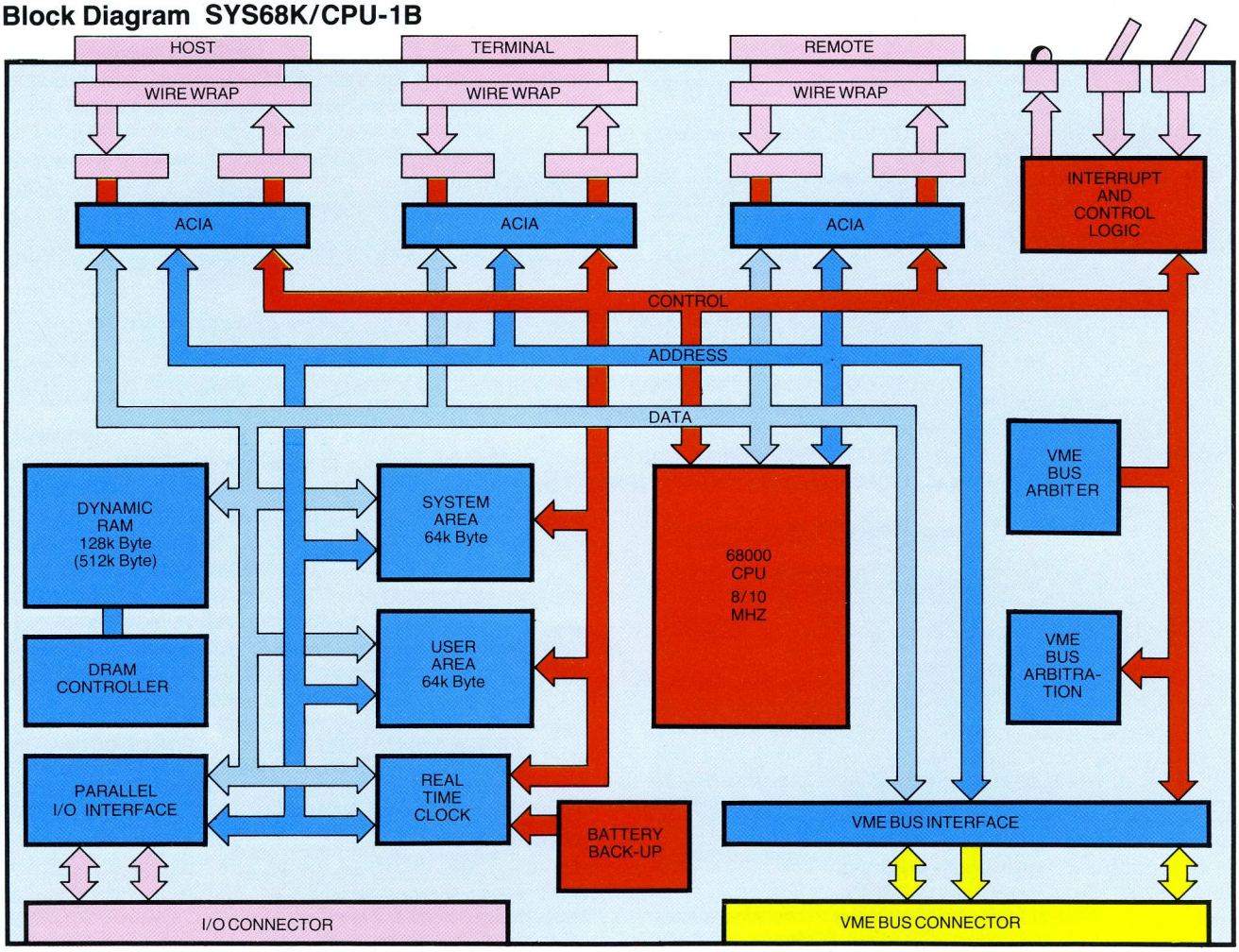
It contains 128k bytes of DRAM, up to 128k bytes of EPROM/ ROM, parallel I/O, a real-time clock, 3 serial communications interfaces and the system monitor.

The implemented VMEbus interface is fully VMEbus compatible and includes the slave bus arbitration as well as a single level bus arbiter.

SYS68K/CPU-1B/C Features

- 68000 CPU (8 MHz) on CPU-1B
- 68000 CPU (10 MHz) on CPU-1C
- 128k bytes of dynamic RAM with distributed refresh every 15μsec.
- 16k bytes of firmware in ROM/EPROM expandable to 64k bytes
- 64k bytes of USER EPROM area or 16k bytes of USER SRAM area
- Memory access times
  PROM 200 – 500 ns (jumper selectable)
  DRAM 280 ns (typ.)
- Three serial communication ports with RS232 compatible interface
- Strap selectable I/O signal assignment
- Parallel I/O with 3 ports 8 bit each
- Timer 24 bit with 5 bit prescaler
- Real Time Clock with battery back-up
- Auto Interrupt Vectoring on all on-board devices (5 different interrupt levels and vectors)
- Fully VMEbus compatible
- 7 interrupt levels from the VMEbus
- Slave bus arbitration
- Single level bus arbiter
- RESET and ABORT function switches
- HALT mode indication LED
- Indirect connection on all connectors
- Double Eurocard form factor with front panel
- Self contained operating firmware that provides monitor, debug, one-line assembly/disassembly, and I/O control functions.
- Operating Software for different applications available.

Block Diagram SYS68K/CPU-1B



Features of the SYS68K/CPU-1D

- The CPU-1D contains the same features as the CPU-1C
- The dynamic memory capacity is increased to 512k bytes

Functional Description

Memory, real time clock, serial and parallel I/O communicates with the MPU via their common internal system bus.

Table 1. shows the global memory layout and the various functional areas of the board are described briefly in the following paragraphs.

Address	
000 000 000 007	Initialisation vectors from system EPROM
000 008 01F FFF	Dynamic RAM on CPU-1B on CPU-1C
000 008 07F FFF	Dynamic RAM on CPU-1D
080 000 09F FFF	SYSTEM Area
0A0 000 0BF FFF	USER Area
0E0 000 0FF FFF	I/O Interfaces
100 000 FEF FFF	VMEbus addresses
FF0 000 FFF FFF	Short I/O access (VMEbus)

1. 68000 CPU (8 or 10 MHz)

The 68000 CPU has a 16-bit data bus and a 23-bit address bus. The address bus provides a direct memory addressing range of 16 megabytes. The processor has eight 32-bit data registers, seven 32-bit address registers, two 32-bit stack-pointers, a 32-bit program counter, and a 16-bit status register. Seven interrupt levels allow an auto- and a non-auto-interrupt vector mode (192 vectors). The 68000 Data Sheet and the User's Manual describe the device in detail.

2. The Dynamic RAM

The local addresses space consists of 128k bytes with a typical access time of 280 ns. By usage of 256k*1 oriented DRAM's the memory capacity is increased to 512k bytes (on CPU-1D).

For critical real time applications the distributed »RAS only« refresh can delay every 15 micro sec a pending access for a maximum of 290 ns. The refresh works totally asynchronous to the CPU. Therefore, no time delay is required if the CPU accesses other memory areas.

3. The SYSTEM Area

The SYSTEM area contains a pair socket (28 pins) with a JEDEC compatible pin-out. This allows the usage of different ROM's and EPROM's with a maximum capacity of 64k bytes. The access time of the SYSTEM area and of the USER area is jumper selectable from 150 to 500 ns.

Table 2. shows the list of usable devices.

The SYS68K MONITOR firmware package resides in two 2764 EPROM's (included in the shipment).

Table 2.		EPROM
2k x 16	4k bytes	2716
4k x 16	8k bytes	2732
8k x 16	16k bytes	2764
16k x 16	32k bytes	27128
32k x 16	64k bytes	27256

4. The USER Area

The USER area contains two 28 pin sockets with JEDEC compatible pin out. To allow the usage of static RAM's, the access to the USER area is byte oriented.

Table 3. lists the usable device types.

Table 3.		EPROM	SRAM
2k*16	4k bytes	2716	6116
4k*16	8k bytes	2732	–
8k*16	16k bytes	2764	6264
16k*16	32k bytes	27128	–
32k*16	64k bytes	27256	–

5. Serial Communication Ports

Three asynchronous serial communication ports, designated Port 1 for the terminal, Port 2 for the host, and Port 4 for user applications, are provided on the board. All of these ports are RS232C compatible. (E.I.A. standard). The terminal acts as a user interface and works in conjunction with the monitor. Port 2 interfaces to a modem or directly to a host computer. The host computer may be used to provide more powerfull software capabilities, such as program assembly and downloading of programs. Also an operational transparent mode condition is callable via the system monitor. This transparent mode effectively bypasses the board and allows the terminal to communicate directly with the host. The third serial communication port interfaces either to a printer, acts as a remote link to another computer or to a back-up unit such as a Floppy/Cartridge system. All serial ports are jumper selectable for various data transmission rates (110-9600 or 600-19200 baud).

For each serial port the I/O signals can be assigned to one of the 25 pins of the D-sub female connector on the front panel.

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6. Parallel I/O

The board contains a Parallel Interface and Timer chip PI/T 68230 with a clock frequency of 8 MHz.

The PI/T operates in uni- or bi-directional mode either 8 or 16 bits wide.

Each of the 24 I/O lines may be configured as an input or as an output.

For asynchronous software control the third 8 bit port can be configured to drive two interrupts on level 5, one for the handshake interface and one as a timer output.

7. Programmable Timer

The PI/T 68230 (Parallel Interface and Timer) includes a 24-bit programmable timer. The timer is a synchronous counter to be used for generating or measuring time delays and various frequencies. The timer is either clocked by a 5-bit prescaler or directly, and the clock source can either be the 8 MHz system clock or an external clock.

8. Programmable Real Time Clock

The on-board Real Time Clock (RTC) allows various applications, such as time scheduling, time comparison, time-out counter, etc. Additionally, the real time clock may act as an actual time base providing month, day of month, and day of week. An on-board battery ensures time base operation during power down times.

9. On-Board Interrupt Handling

All on-board devices are able to force interrupts on different levels to the CPU. In this case the auto-interrupt vector of the 68000 will be forced and each device has its own interrupt vector.

Table 4. shows the interrupt structure of the CPU-1B/C/D.

Description	Device	Level	Vector No.
ABORT	Switch	7	31
Real Time Clock	58167A	6	30
Paralle Interface and Timer	68230	5	29
Terminal ACIA	6850	4	28
Remote ACIA	6850	3	27
Host ACIA	6850	2	26

10. The VMEbus

The implemented VMEbus Interface includes 24 address, 16 data, 6 address modifier and the asynchronous control signals.

A single level bus arbiter is provided to build multi master systems. In Addition to the bus arbiter, a separate slave bus arbitration allows selection of the arbitration level (0-3).

The address modifier range »short I/O Access« can be selected via jumper for variable system generation.

The 7 interrupt request levels of the VMEbus are fully supported from the SYS68K/CPU-1B/C/D. For multi-processing, each IRQ signal can be enabled/disabled via a jumper field.

Additionally, the SYS68K/CPU-1B/C/D supports the ACFAIL, SYSRESET, SYSFAIL and SYSCLK signal (16 MHz).

11. The MONITOR Firmware

The SYS68K/CPU board operates under control of the SYS68k MONITOR firmware. This 16k byte software package provides an easy interface to the SYS68K family hardware and offers excellent functionality. SYS68K MONITOR is a system monitor which controls communication with the terminal and exercises other elements of the system. It provides debug capability, one-line assembly/disassembly, and I/O control.

For program development and debug, a dynamic line-by-line editor/assembler function is used. Each instruction is translated into the proper opcode and stored in the memory.

In order to display an instruction, the firmware disassembles the opcode and displays the instruction mnemonic and operands.

Data and programs can be uploaded and downloaded via a serial port (HOST INTERFACE).

SYS68K MONITOR has the following features:

SYS68K MONITOR COMMAND SUMMARY

COMMAND	DESCRIPTION
BF <address1> <address2> <data> <CR>	Block Fill memory – from add1 through add2 with data
BM <address1> <address2> <address 3> <CR>	Block Move – move from add1 through add2 to add3
BR [<address> [; <count>]...] <CR>	Set/display Breakpoint
BS <address1> <address2> <data> <CR>	Block Search – search add1 through add2 for data
BT <address1> <address2> <CR>	Block Test of memory
DC <expression> <CR>	Data Conversion
DF <CR>	Display Formatted registers
DU [n] <address1> <address2> [<string>] <CR>	Dump memory to object file
GO [<address>] <CR>	Execute program
GD [<address>] <CR>	Go direct
GT <address> <CR>	Exec prog: temp. breakpoint
HE <CR>	Help; display monitor commands
LO [n] [;<options>] <CR>	Load Object file
MD <address> [<count>] <CR>	Memory Display
MM <address> [<data>] [;<options>] <CR>	Memory Modify
MS <address> <data1> <data2> <... <CR>	Memory Set – starting at addr with data 1, data 2,..
NOBR [<address> ...] <CR>	Remove Breakpoint
NOPA <CR>	Printer Detach
OF <CR>	Offset
PA <CR>	Printer Attach
PF [n] <CR>	Set/display Port Format
RM <CR>	Register Modify
TM [<exit character>] <CR>	Transparent Mode
TR [<count>] <CR>	Trace
TT <address> <CR>	Trace: temperature breakpoint
VE [n] [<string>] <CR>	Verify memory/object file
.AO – .A7 [<expression>] <CR>	Display/set address register
.DO – .D7 [<expression>] <CR>	Display/set data register
.RO – .R6 [<expression>] <CR>	Display/set offset register
.PC [<expression>] <CR>	Display/set program counter
.SR [<expression>] <CR>	Display/set status register
.SS [<expression>] <CR>	Display/set supervisor stack
.US [<expression>] <CR>	Display/set user stack
MD <address> [<count>];DI <CR>	Disassemble memory location
MM <address>;DI <CR>	Disassemble/Assemble memory location

Available Software

Rommable Software	Operating System	Real Time Packages
Full Screen EDITOR/ASSEMBLER called SYS68K/FORCE IDEAL	A UNIX™ Version 7 compatible Operating System for single User and multi tasking called SYS68K/COHERENT™	Real Time Multi Tasking Kernal with logical I/O interfaces called pSOS-68K
BASIC Interpreter/ Compiler called SYS68K/BASIC-68K		
FORTH Interpreter/ Compiler called SYS68K/FORTH-68K		

Data sheets are available for all software packages.

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Specification of the SYS68K/CPU-1B/C/D

Table 5	Specifications
Microprocessor	68000 (8MHz on CPU-1B/10MHz on CPU-1C and CPU-1D)
Parallel I/O	68230 PI/T, 16 data lines and 8 control lines configurable as a Centronics parallel interface
Serial I/O	3 R232C interfaces strap selectable baud rate from 110-9600 or 600-19200 baud
Timer	One 24-bit timer with a 5-bit prescaler,
Real Time Clock	Programmable real time clock with battery back-up
Memory	128k bytes of RAM,on CPU-1B and CPU-1C, 512k bytes of RAM on CPU-1D, 64k bytes of SYSTEM area, 64k bytes of USER area.
Firmware	16k bytes of monitor called SYS68K MONITOR including a one-line assembler/disassembler
Power Requirements	+5V/2.8A, +12V/200mA −12V/200mA
Operating Temp.	0 to +60 degrees C
Storage Temp.	−50 to +85 degrees C
Relative Humidity	0−95% (non-condensing)
Board Dimensions	Double Eurocard 234 x 160 mm (9.2 x 6.3")

Ordering Information:

SYS68K/CPU-1B	68000 CPU Board including HUM and SUM (8MHz clock frequency/128kB RAM)
SYS68K/CPU-1C	68000 CPU Board includung HUM and SUM (10MHz clock frequency/128kB RAM)
SYS68K/CPU-1D	68000 CPU Board including HUM and SUM (10MHz clock frequency/512kB RAM)
SYS68K/CPU-1B/HUM	Hardware User's Manual
SYS68K/CPU-1B/SUM	Software User's Manual

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