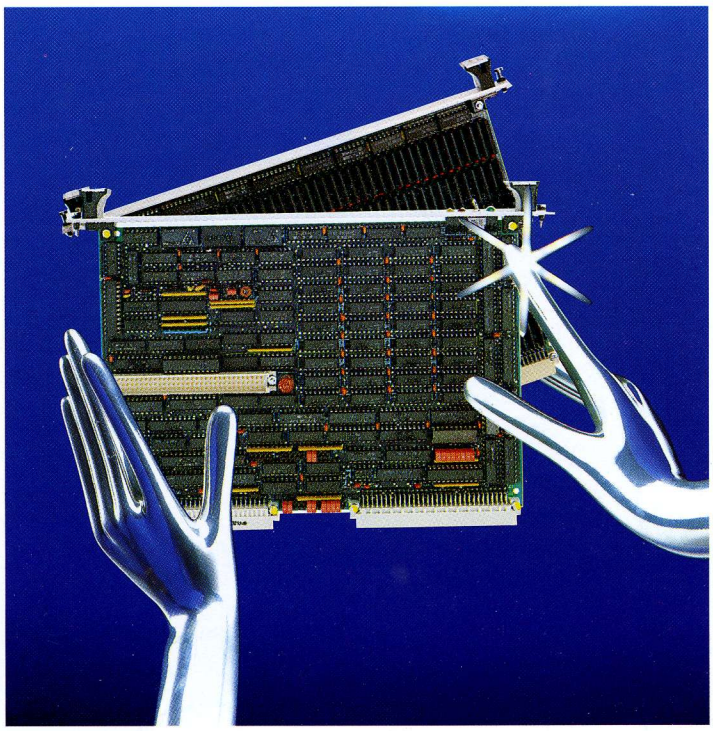
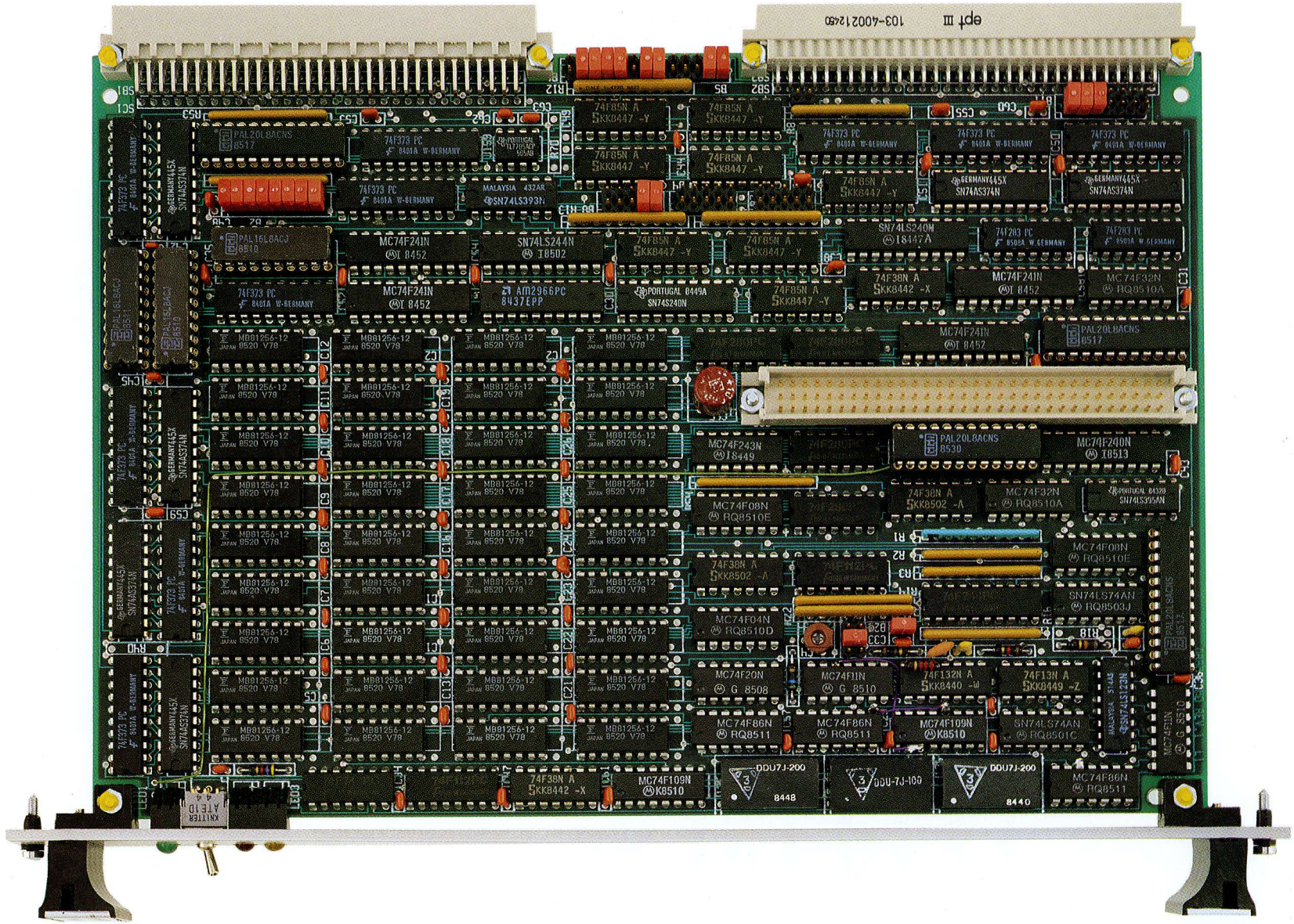


SYSTEM 68000 VME

SYS68K/DRAM-E3M/S

32 Bit Dynamic Memory Board with Byte Parity and FME Interface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General Description SYS68K/DRAM-E3M1

The SYS68K/DRAM-E3M1 board is a high speed dynamic memory board supporting 32 address and data lines, including byte parity check. The address modifier codes are free jumper selectable. The memory capacity of 1Mbyte can be expanded via FME* slave boards to a maximum capacity of 13Mbyte.

The block diagram of the DRAM-E3M1 board shows the building blocks in detail.

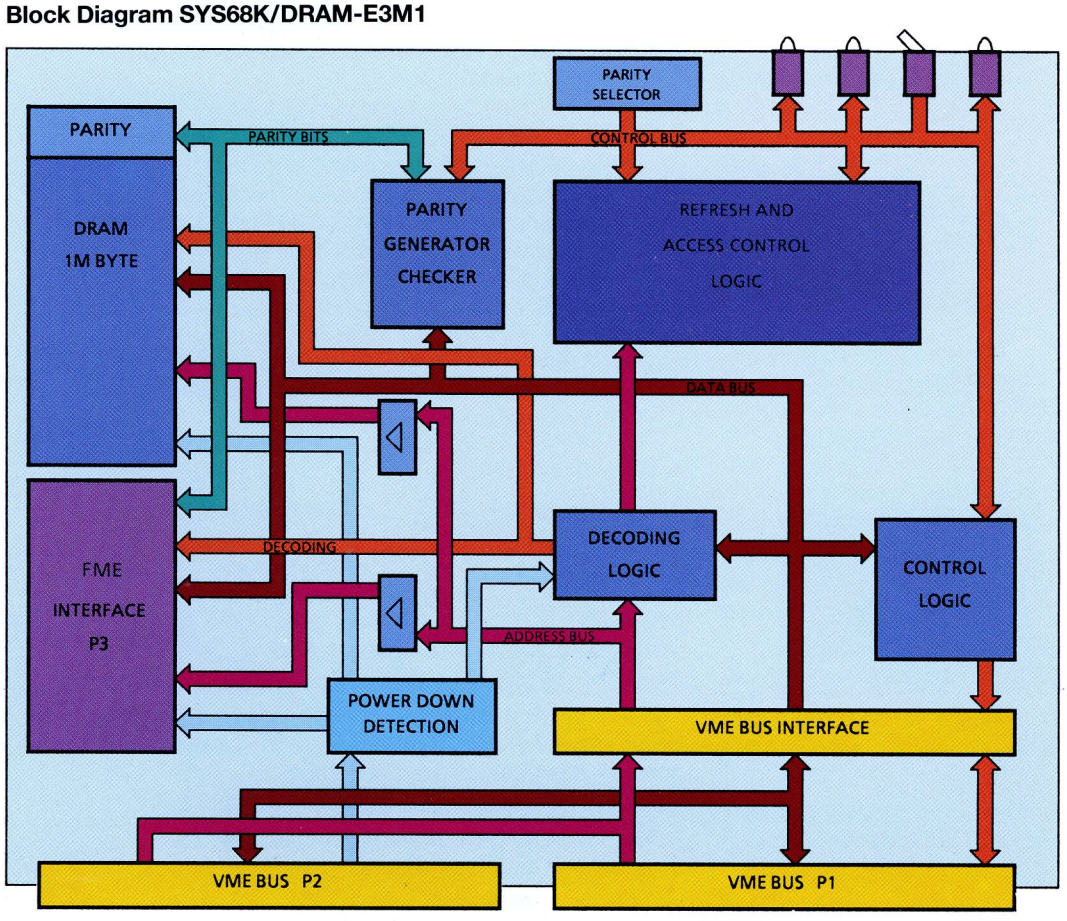
SYS68K/DRAM-E3M1 Features

- 1Mbyte dynamic RAM
- 75ns Write Access Time
- 225ns Read Access Time
- Parity check for each byte
- 32 Address Lines are supported
- 32 Data Lines are supported
- Support of the Unaligned Transfer UAT (IEEE P1014**)
- Read Modify Write is supported (8, 16, 24 and 32 bit)
- Address Modifier Code and Access Address free jumper selectable
- Refresh Interleave
- FME Interface
- Battery Backup through P2
- RUN/LOCAL function switch
- RUN/LOCAL/ACCESS and ERROR indication LEDs

FME* Force Memory Expansion

IEEE P1014 ** Bus Specification (VMEbus) of the IEEE Computer Society TC.

Block Diagram SYS68K/DRAM-E3M1



Functional Description

All of the technical features of the DRAM-E3M1 board are briefly described in the following paragraphs:

1. Memory Capacity and Organization

The DRAM-E3M1 board consists of 36 dynamic RAM chips with an internal organization of 256K by 1 bit. 32 chips are used for data storage and 4 chips contain the parity information.

The total capacity of the DRAM-E3M1 board is 1Mbyte.

The selected address modifier code (A32 or A24) defines the decoding range of the memory. Automatic adjustment to the VMEbus transfer type (8, 16, 24 or 32 bit) is provided.

The IEEE P1014 unaligned transfers (Read, Write and Read Modify Write) for the 68020 are supported.

Data Transfer Types Read/Write and Read Modify Write	D24-31	D16-23	D8-D15	D0-D7
Single Byte Even			x	
Single Byte Odd				x
Double Byte			x	x
Quad Byte	x	x	x	x
Unaligned Transfer	x	x x x	x x x	x

2. The Parity Check

A byte parity check is installed on the board to provide error checking. The parity check can be enabled or disabled via jumper settings. The timing to the RAM chips is identical in both modes, but the access time for a Read cycle is 30ns faster if the parity check is disabled.

If a parity error occurs, the red FAIL LED on the front panel turns on, and a BERR is forced to the VMEbus. The latched ERROR status can be reset via a switch on the front panel.

3. Access Times

The DRAM-E3M1 contains address and data latches to provide maximum throughput to the VMEbus.

If an access is performed on the DRAM-E3M1 board, the yellow SELECT LED on the front panel turns on.

Access Times	Typ	max
WRITE	65ns	75ns
READ with Parity Check	240ns	255ns
READ without Parity Check	210ns	225ns
Overhead time for Refresh	120ns	450ns

4. The Refresh

The refresh for the dynamic RAMs is distributed over 4ms and provision is made to minimize the overhead and delay to the VMEbus accesses.

After the internal read cycle of the DRAMs is finished and the data on a read cycle has been stored in the output data latches, a pending refresh request (every 15us) is executed independent from all VMEbus activities. Therefore the overhead time for the VMEbus protocol is used to refresh the RAMs. In addition to the refresh interleave, a refresh to the DRAMs is forced if a not on-board access is detected between 11 and 15us after the execution of the last refresh.

The refresh control logic for the FME slave modules (memory expansion) is included on the DRAM-E3M1 board.

5. Battery Backup

All of the DRAMs and the control logic can be powered through the P2 connector. The typical power consumption of the DRAM-E3M1 board in the battery backup mode is 1.0A if refresh is not active, and 2.4A of a refresh cycle is executed (peak current). Due to the limitation of the power consumption of 1.2A per DIN connector pin, 3 pins on the P2 connector are used to provide the battery backup. For special purposes the P1 STDBY line can be used to power the board.

6. The Address Selection

Easy address and address modifier code selection is provided through jumper fields. The access address is jumper selectable in 256Kbyte increments over the whole range of 16Mbytes or 4G bytes. The start and end address selection is not memory capacity dependent including FME memory expansion.

Twelve different address modifier codes are jumper selectable. Each of the AM-codes can be enabled seperately via jumper setting.

24 and/or 32 address lines are supported on the DRAM-E3M1 to provide maximum flexibility for 16 and 32 bit microprocessors.

Usable Address Modifier Codes:

No	HEX Code	Address Modifier	Function
1	3E	HHHHHL	Standard Supervisory Program Access
2	3D	HHHHLH	Standard Supervisory Data Access
3	3A	HHHLHL	Standard Non-priviledged Program Access
4	39	HHHLLH	Standard Non-priviledged Data Access
5	0E	LLHHHL	Extended Supervisory Program Access
6	0D	LLHHLH	Extended Supervisory Data Access
7	0A	LLHLHL	Extended Non-priviledged Program Access
8	09	LLHLLH	Extended Non-priviledged Data Access
9	XX	XXXXXX	Respond Always
10	1E	LHHHHL	User defined
11	10	LHHHLH	User defined
12	19	LHHLLH	User defined

7. RUN/LOCAL Switch

A RUN/LOCAL switch can be used to isolate the DRAM-E3M1 from the VMEbus during maintenance or for test purposes. The state is shown on two LEDs available on the front panel.

8. The FME

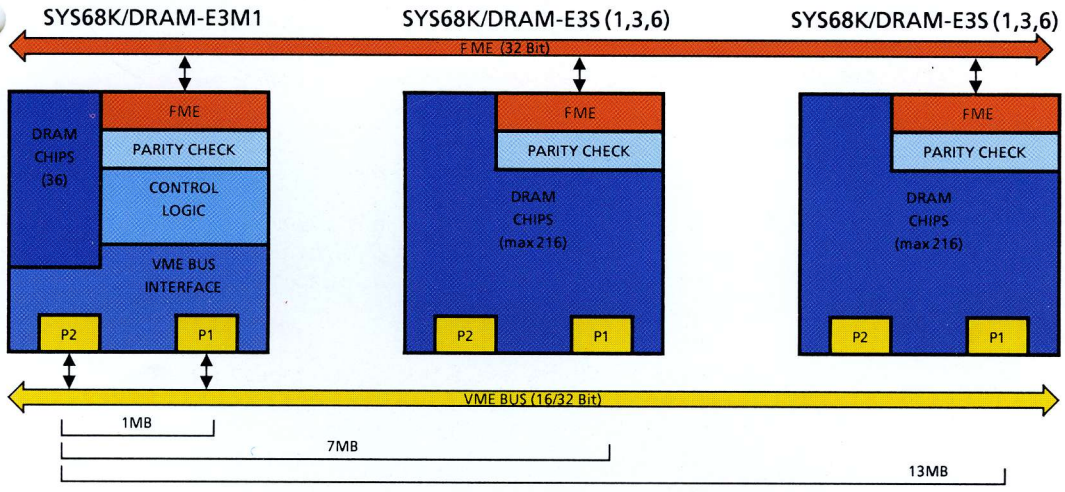
The SYS68K/DRAM-E3M1 supports the FME (FORCE Memory Expansion) to provide cost effective memory expansion through FME slave boards. The FME master interface on the DRAM-E3M1 supports a maximum of 2 FME slave boards which can be connected directly to the DRAM-E3M1 via a 96 pin DIN connector (P3). No time overhead is required through and for the expansion with FME slave modules because the access times listed in point 3 are valid for the onboard RAM as well as for the FME slave modules.

The FME concept allows the local memory extention of RAM and CPU boards by using their on-board DRAM control logic as well as their bus interfaces.

TheFME allows easy system integration using the VMEbus and/or VMXbus for memory expansion in high performance system configurations.

Slave boards are available with a capacity of 1, 3 and 6Mbytes. Therefore a maximum capacity of 13Mbytes is provided using the DRAM-E3M1 and 2 slave boards, both with 6Mbytes capacity.

The FME Concept



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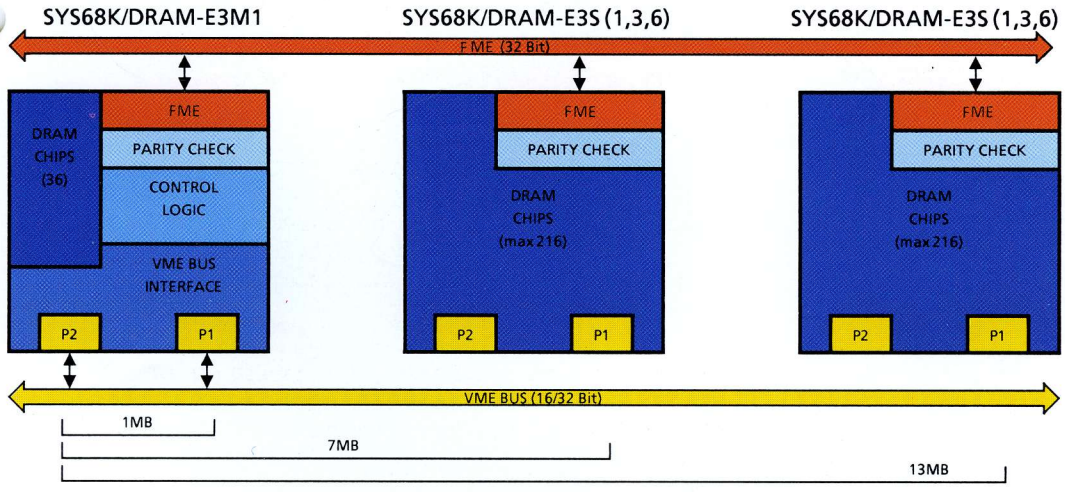
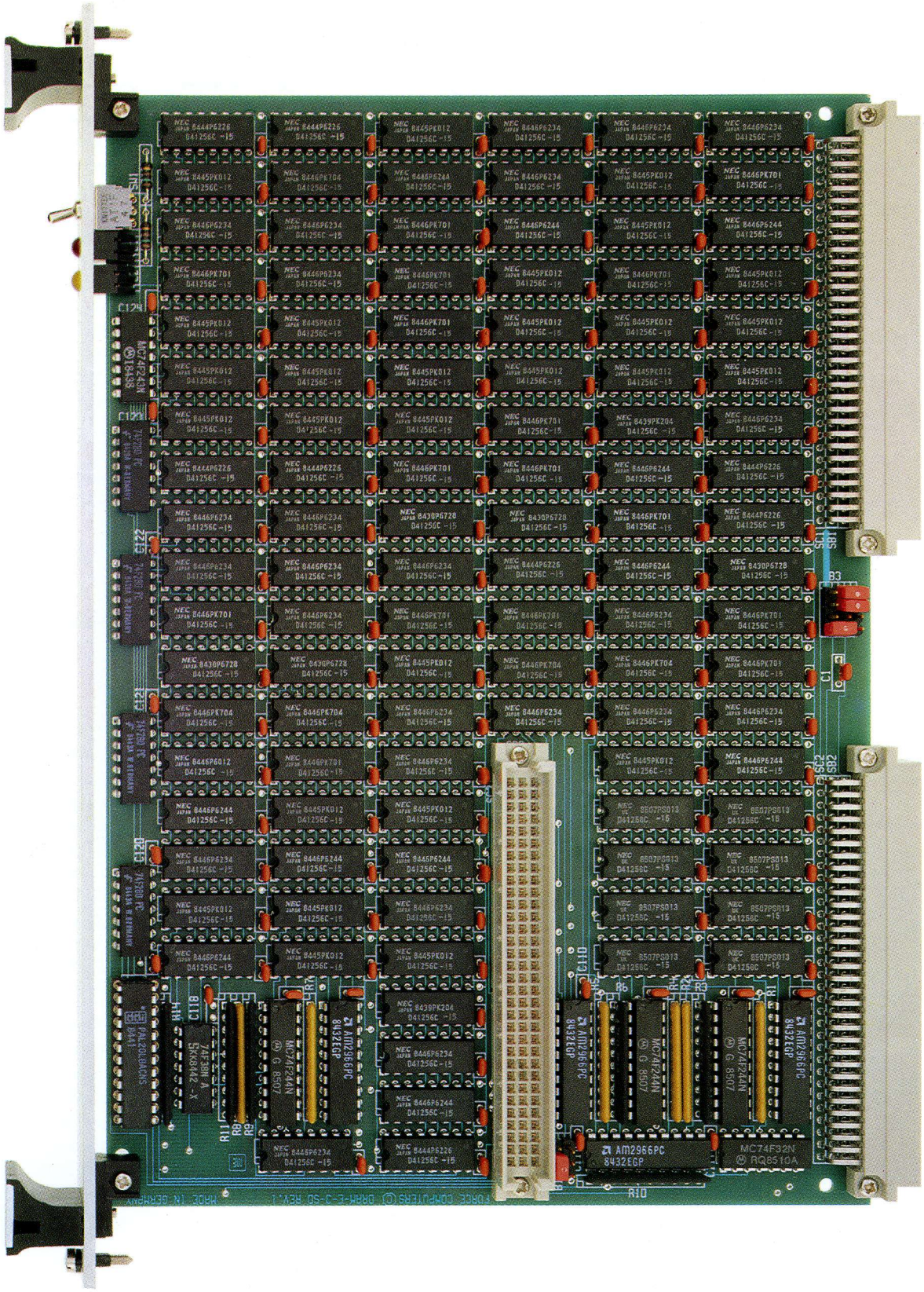
The FME Concept





General Description SYS68K/DRAM-E3SX

The SYS68K/DRAM-E3SX boards are high speed dynamic memory boards based on the FME. Each of the slave boards contains 32-bit data and 4 parity bits as well as the complete decoding logic for the FME. Three different memory boards with a capacity of 1, 3 or 6Mbytes are available.

SYS68K/DRAM-E3SX Features

- FME Slave board
- 32 data lines are supported
- 4 parity bits
- 4 strobes control every byte seperately
- Read Modify Write is supported
- Parity Error LED
- Access LED
- Refresh Interleave Support
- DRAM-E3S1 : 1Mbyte RAM
  DRAM-E3S3 : 3Mbyte RAM
  DRAM-E3S6 : 6Mbyte RAM

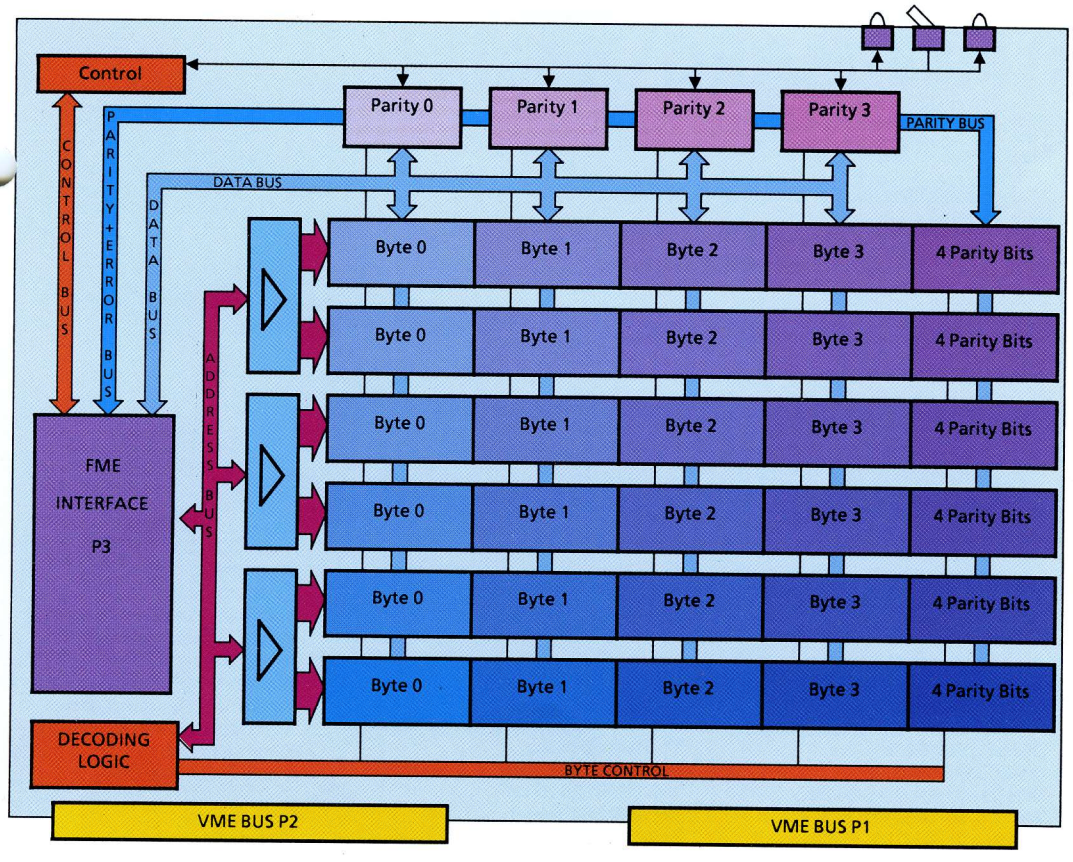
Functional Description

The FME boards DRAM-E3S1/3/6 are designed to interface any FME master board as a memory expansion. FME master boards (i.e. DRAM-E3M1) control the access as well as the refresh function of the DRAMs on the slave boards. The FME master board has to achieve timing and control to the slave modules for optimized througput.

All the memory range decoding and bank selection is made on the master board to allow the usage of every slave board in 8, 16 or 32 bit environments. Each of the DRAM-E3SX boards uses 256K x 1 oriented DRAMs with an access time of 120ns. The DRAM-E3S1 and E3S3 boards use Dual Inline packages and the E3S6 board uses a Zick Zack package.

To avoid power consumption peaks, the DRAM-E3SX boards can refresh the memory cells for each memory bank seperately. The FME master board controls this function.

Block Diagram SYS68K/DRAM-E3S6



Specification SYS68K/DRAM-E3SX

	E3M1	E3S1	E3S3	E3S6
Memory Capacity	1Mbyte	1Mbyte	3Mbyte	6Mbyte
Organization	32+4 Bit	32+4 Bit	32+4 Bit	32+4 Bit
Data Transfer Mode any of 4 bytes	Yes	Yes	Yes	Yes
Used DRAM Organization	256Kx1	256Kx1	256Kx1	256Kx1
DRAM Chips	36pcs	36pcs	108pcs	216pcs
RAS DRAM Access Time	120ns	120ns	120ns	120ns
Interface	FME (master) VMEbus	FME (slave)	FME (slave)	FME (slave)
Access Times Write	65	65	65	65
With Parity Check Read	240	240	240	240
Without Parity Check Read	210	210	210	210
Power Requirements				
+5V (Refresh Peak)	65.9A	2.8A	3.5A	5.0A
+5V (Average Max)	4.3A	2.7A	3.0A	4.8A
+5V (Average Typ)	3.2A	2.5A	2.8A	4.6A
+5V BATTERY	2.4A			
Operating Temperature (degrees C)	0 to +60	0 to +60	0 to +60	0 to +60
Storage Temperature (degrees C)	–55 to +85	–55 to +85	–55 to +85	–55 to +85
Relative Humidity (non-condensing)	0–95%	0–95%	0–95%	0–95%
Double Eurocard 233x160mm (9.2x6.3")	Yes	Yes	Yes	Yes

Ordering Information

SYS68K/DRAM-E3M1 Part No1. 200004	1Mbyte DRAM card for 32 bit including the FME master interface and E3M1/HUM.
SYS68K/DRAM-E3S1 Part No. 200101	1Mbyte DRAM card for memory expansion. E3SX/HUM included.
SYS68K/DRAM-E3S3 Part No. 200103	3Mbyte DRAM card for memory expansion. E3SX/HUM included.
SYS68K/DRAM-E3S6 Part No. 200105	6Mbyte DRAM card for memory expansion. E3SX/HUM included.
SYS68K/DRAM-E3M1/HUM Part No. 800043	Hardware User's Manual for the SYS68K/DRAM-E3M1 card.
SYS68K/DRAM-E3SX/HUM Part No. 800061	Hardware User's Manual for the FME Slave cards.

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