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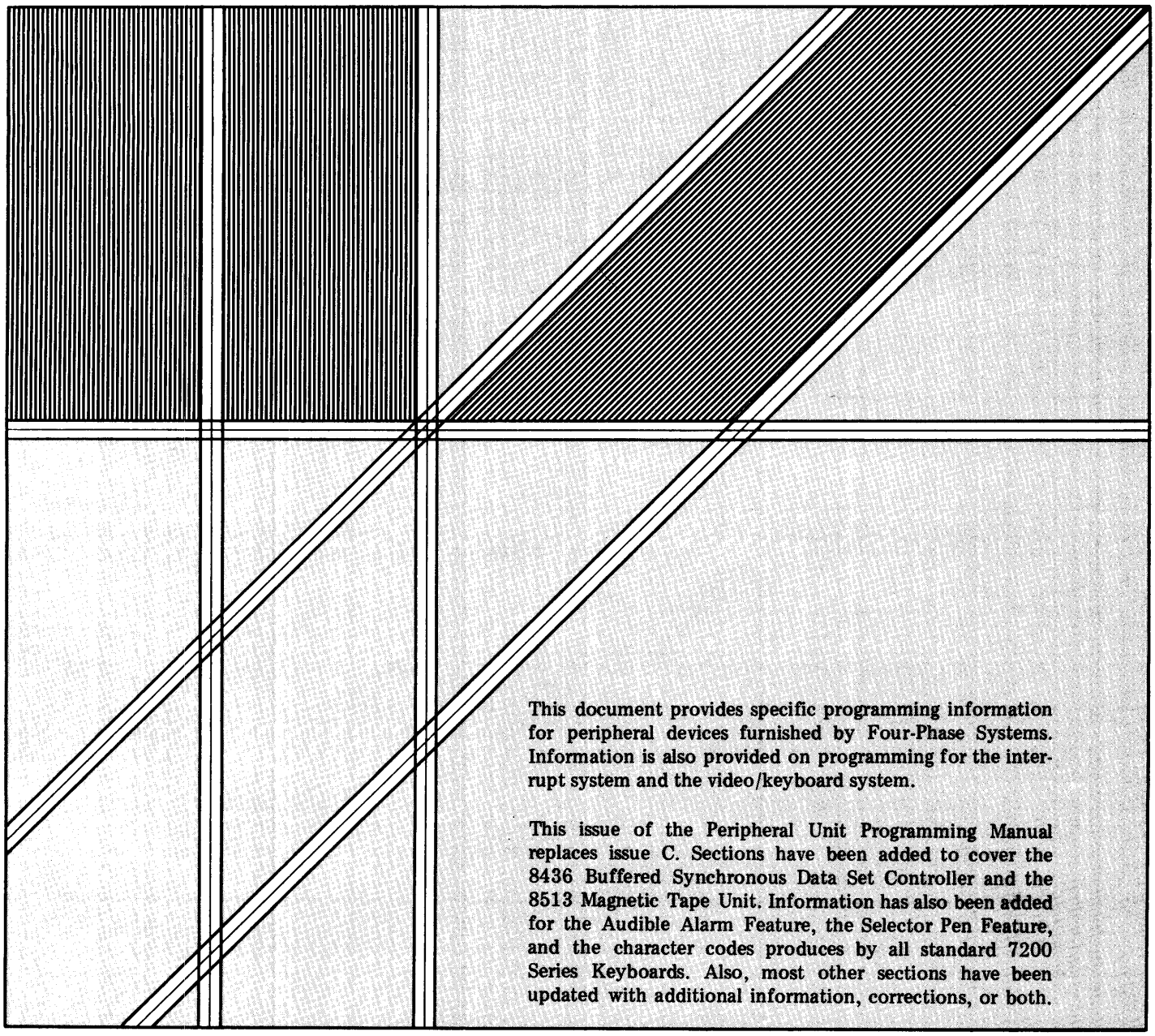
System IV/70

Peripheral Unit Programming Manual



This document provides specific programming information for peripheral devices furnished by Four-Phase Systems. Information is also provided on programming for the interrupt system and the video/keyboard system.

This issue of the Peripheral Unit Programming Manual replaces issue C. Sections have been added to cover the 8436 Buffered Synchronous Data Set Controller and the 8513 Magnetic Tape Unit. Information has also been added for the Audible Alarm Feature, the Selector Pen Feature, and the character codes produces by all standard 7200 Series Keyboards. Also, most other sections have been updated with additional information, corrections, or both.

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Section 1
Introduction

This document is written for the programmer who is programming for the peripheral devices furnished by Four-Phase Systems. It is intended to be used with the "System IV/70 Computer Reference Manual," document SIV/70—11—1, especially Sections 3 through 7.

Topics covered in this manual include programming for the interrupt system, the video/keyboard system, and other peripheral units. Although information is given in the Computer Reference Manual on programming the interrupt system and the video/keyboard displays, further details are added here for those actually programming the system. Full attention is given to status word, control word, and data formats for each peripheral unit where applicable. Illustrative examples of working programs are given for typical units.

The System IV/70 Computer employs an input/output structure with the following features:

- Eight separate I/O channels, each of which may contain up to 64 peripheral units.
- Eight levels of priority interrupts, one for each I/O channel, with true hardware nesting of all eight levels. Each level may have up to 64 separately addressable devices (unit addresses) with chained subpriority.
- Each I/O device interfaces with the computer using a peripheral controller circuit, which performs buffering, handshaking, and other required interfacing functions.

THE IO INSTRUCTION

The IO instruction transfers data into or out of the computer using a single instruction. The instruction uses a word-pair in memory to select the device for the transfer, the type of transfer, and a buffer address for the transfer. Depending on the options selected by the programmer, the instruction will issue proper signals to the peripheral unit controller to perform the transfer, accept input data or present output data, and update the memory buffer by adding one to the buffer address for each transfer performed. The types of I/O transfers that may be selected are data in, data out, status in, and control out; the type of transfer along with the address of the selected unit are determined using program constants. Status and control data are arranged as bit patterns in a single data word so that they may be easily tested or generated using program constants.

The IO instruction is used for transfers in the "handshaking" mode of operation. The significance of the handshaking mode is that the computer and the peripheral device exchange a series of non-data signals before, during, and after any I/O transfer. From the software point of view, the handshaking is all automatically performed by the IO instruction.

Format

The IO instruction points to a word pair in memory which controls the execution of the instruction. The first word, which must have an even address, is the select or CUT word. It identifies the unit being selected and the type of I/O transfer. The second word (located at Select Word Address+1) contains the buffer address into which or from which the transfer will occur. See illustration, "Select Word and Buffer Address Word Formats." Note that the buffer address is incremented by one with every data, control, or status transfer. It is normal practice to decrement (using the DEC instruction) the buffer address after a status or control IO instruction, or to restore it using a LOAD/STORE sequence after a multiple transfer.

Block Transfers

Note that the IO instruction does not distinguish between block and one-word transfers. Whether a given transfer is to be one word or a block is controlled by the interface hardware and determined by either one or both of two factors:

- The nature of the device. Thus, a disc transfers data in blocks, a card reader in words or bytes, and teletypes in bytes (one byte to a word). The programmer will normally determine which kind of transfer is needed from the nature of the device, and specify his buffer sizes correspondingly.
- A control word. With some devices the control word is used to indicate whether a block or single word transfer is required. On output, whenever a block transfer is required, the program must furnish a control word telling the device exactly how many words of data to expect, or the program will hang. On input, the program may also be required to tell the device how big a block to send.

OTHER I/O INSTRUCTIONS

The IO instruction handles the majority of I/O programming cases. Other instructions are: BOOT (bootstrap load), IOB (IO with three bytes packed into a word on input or unpacked on output), EXCT (output signals), EXSN (sense external lines), and ECS (enter the contents of the console keys into a specified register).

BOOT Instruction

This instruction provides a simplified means for inputting a loader program any time the computer is turned on or the contents of memory are destroyed. The BOOT instruction is normally keyed in at the console control panel, and the input device is prepared to load the program. When the instruction is executed, it will communicate with the device in the handshaking mode and load in the program; it can operate in either character (pack) or word mode. Details of the BOOT instruction are covered in Section 6 of the "Computer Reference Manual."

IOB Instruction

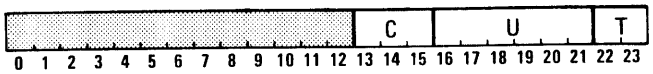
The IOB instruction is used to interface with byte oriented I/O devices whose controllers do not have provision for packing and unpacking bytes. Bytes are packed into a word on input and unpacked from a word on output by the computer itself. Since this instruction is relatively slow and locks up the computer for the full three-byte transfer, it is not widely used except in loader programs associated with byte-oriented devices such as teletypes.

Note that this instruction is not suitable for use with a device where the controller is also required to display the character as it is typed, because the first character will not be displayed until three characters are received. The controller must be designed to lock up for 3 characters. No Four-Phase Systems controllers are now designed for use with the IOB instruction.

EXCT Instruction

This instruction operates by gating the four least-significant bits of the contents of the effective address onto the four external command lines of the I/O system for two machine cycles; see illustration "External Command Line Gating." These four lines may be encoded as required. Codes 14_8,

Select Word (even address)



Bits	Symbol	Meaning
0—12	— — —	Not used.
13—15	C	Device channel number
16—21	U	Device unit number
22, 23	T	Type of operation as follows:

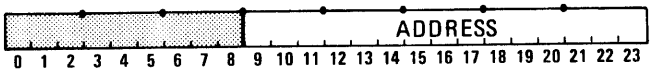
00 Data Out. Data will be sent to the selected device starting from the address designated by the buffer address word.

01 Data In. Data will be supplied from the selected device to main storage starting at the address designated by the buffer address word.

10 Control. The control word from the address designated by the buffer address word is sent to the selected device. This information typically contains device orders such as read, write, rewind, etc.

11 Status. A status word is supplied from the selected device to the address designated by the buffer address word. This information contains status bits peculiar to the device indicating such conditions as device ready, beginning of tape, end of tape, device error, etc.

Buffer Address Word (odd address)



Note that the buffer address (i.e., the contents of the buffer address word) will be incremented by one automatically at the time of each byte or word transfer. Thus, for block transfers, the buffer address will be incremented by the number of words or bytes transferred, and will point to the location following the last location that participated in the transfer.

A067B

Select Word and Buffer Address Word Formats

15_8, 16_8, and 17_8 are used to control the memory parity circuits (see "Main Storage" in the "Computer Reference Manual"); codes 11_8, 12_8, and 13_8 control the video attribute characters; in many Four-Phase supported programs, code 1_8 is used to trigger interrupt level 7 from inside the software; the eight remaining combinations may be used by the programmer.

$$[EA]_{20} \rightarrow EXC_0$$
$$[EA]_{21} \rightarrow EXC_1$$
$$[EA]_{22} \rightarrow EXC_2$$
$$[EA]_{23} \rightarrow EXC_3$$

External Command Line Gating

EXSN Instruction†

This instruction compares the computer's four external sense lines with the four least-significant bits of the contents of the effective address, skipping conditionally on the results of the comparison. See illustration "External Sense Comparisons". These inputs are not used in the current configuration (except for diagnostic purposes) and are available to be encoded as required by the programmer.

$EXS_0 : EA_{20}$
$EXS_1 : EA_{21}$
$EXS_2 : EA_{22}$
$EXS_3 : EA_{23}$

If $([EA]_{20} \cap EXS_0) \cup ([EA]_{21} \cap EXS_1) \cup ([EA]_{22} \cap EXS_2) \cup ([EA]_{23} \cap EXS_3) = 1, [RP] + 1 \rightarrow [RP]$

External Sense Comparisons

ECS Instruction

This instruction transfers the contents of the console keys into the destination register of the instruction under byte control. This information may be used for control or data purposes by the programmer. A conventional program for using these switches might loop waiting for the state of one or more bits to change before taking some course of action.

INTERRUPT STRUCTURE

The interrupt system for the System IV/70 Computer is entirely implemented using LSI hardware. The priority structure, waiting and pending logic for interrupts, and channel and unit addresses are all strictly hardware generated. The software may arm, disarm, or reset interrupt levels, and may recognize an interrupt and readily sort out channel and unit addresses. The use of the instructions that arm, disarm, and reset the priority interrupt structure is explained in Section 7 of the "Computer Reference Manual."

† This instruction is available only on the 7002 Processing Unit.

The IOID instruction enables the programmer to identify unit addresses easily when more than one device is connected to a channel. When an IOID instruction is placed in any of the eight dedicated hardware interrupt locations (0, 2, 4, 6, 10, 12, 14, and 16 octal), it forces execution of an instruction whose location is determined by the unit address, whenever an interrupt occurs on that level. The least-significant six bits of the IOID effective address are replaced by the six bit unit address, then control is transferred to the location thus generated. Thus, control may be transferred to any location of the form 64N + UA, where N is any integer ($127 \geqslant N \geqslant 0$ with 24K bytes of memory; $255 \geqslant N \geqslant 0$ with 48K bytes, etc.) and UA is the unit address. A simplified program using the IOID instruction follows. This program will begin loading at location 5600_8 and continue from that point; the channel selected is 6 and the unit address is 32_8.

```
        ORG     0
        PIA     SIX     ARM INTERRUPT
        BRA     $       WAIT FOR AN INTERRUPT
        FORCE   0
        DCN     03151   C=6, U=32, T=DATA IN
        DCN     05600   BUFFER ADDRESS. WILL BE
                        AUTOMATICALLY UPDATED.
SIX     DCN     0100
        .
        .
        .
        ORG     014
        IOID    02000
        .
        .
        .
        ORG     02032
        IO      2       ASK FOR DATA
```

Note that some controllers may furnish more than one IOID address (unit address) to force different starting locations for different I/O routines. Thus, the 8001 card reader controller will give one IOID address for character ready and another for pick needed (end of card). This facilitiates the acceptance of character data using a single instruction IO. However, this function requires the addition of extra circuitry on the controller card.

Note that all software furnished by Four-Phase Systems is based on the assumption that specific channel and unit addresses are being used. These assignments are shown in the table, "Four-Phase Standard I/O Priority Assignments" in Section 3.

With various controllers that operate under the interrupt system and generate interrupts for several different status-bit changes, it is possible for an interrupt to occur out of synchronization with the software. This can occur, for example, if status is taken with the interrupt level of the device disarmed, or if status on a device is taken from a higher level than that of the device. Particular devices where this problem can occur are printers and data sets.

The symptom of this problem is that apparently spurious interrupts occur, with no expected status changes; such interrupts can cause a program to blow. The method for coping with such interrupts is to test explicitly for all legal status conditions that could generate an interrupt from the device and to return to the background program if no such condition is found. Example (Interrupt routine for hypothetical device):

```
INTLOC  BSS     1       BRM from IOID address
        IO      STAT    Read status
        DEC     STAT+1
        LDA*    STAT+1  Get status word into RA
        CPA     N0      0, 1, 5 are legal
        BZO     READY   Other interrupts illegal
        CPA     N1
        BZO     NREADY
        CPA     N5
        BZO     INTRVN  Operator intervention
RETURN  BRD     INTLOC
READY   BSS     0
        .
        .
        .
        BRA     RETURN
NREADY  BSS     0
        .
        .
        .
        BRA     RETURN
INTRVN  BSS     0
        .
        .
        .
        BRA     RETURN
N0      DCN     0
N1      DCN     1
N5      DCN     5
        FORCE   0
STAT    BSS     1       Channel, unit, type
        BSS     1       Buffer address
```

Section 2
Video/Keyboard Interface

The Video/Keyboard Terminal consists of a keyboard input device and a video screen that displays character data from the keyboard. A unique property of this system is that the video display is generated and refreshed directly from the computer's main memory; to display a character it is merely necessary to store the character in a memory location dedicated to the particular display.

The video output and keyboard input are separate I/O devices in this system, but are designed to be used together. The programming for the two devices, although quite separate conceptually, will normally occur in the same program. This is because the usual storage area for characters read in from the keyboard will be the video display refresh area. Thus the programming sequence for the video/keyboard system is to take a character from the keyboard, process it as required, and store it in the appropriate refresh area; the character is now automatically displayed.

KEYBOARD UNIT INPUT

There are five standard keyboard configurations for the 7200 Series Keyboards. These configurations all generate the same codes with a few exceptions; other differences between them are limited to the legends that appear on the keytops. The keytop legends and ASCII codes for each of these keyboards are shown in the table "Keyboard Character Codes"; the index number assigned to each key is shown in the figure "Key Numbers".

The 7200 Series Keyboards operate with a controller circuit that provides a character buffer for each keyboard (up to a maximum of 32). This isolates the keyboards from one another by allowing all the keyboards to be used at once without mutual interference. The method used is polling: the controller checks the status of each character buffer in turn and generates an interrupt when a character is found.

The keyboard controller performs no packing and presents its data to bits 16-23 of the bus; it does not interface with the rest of the bus. The only IO control instruction used is for the Audible Alarm Feature available as an option with the 7002 Processing Unit. The IO status instruction is only used for Software Polling and not for the normal method of keyboard programming — IOID Programming.

IOID Programming

The 7200 Series Keyboards may be treated as a conventional input unit designed to operate under the interrupt system using the IOID instruction. The keyboard can generate characters at a rate of approximately one every 54 milliseconds. Up to 32 keyboards can be serviced on a single I/O channel. As presently configured, the 32 (or fewer) keyboards on a channel will be wired to Unit Address locations 0 through 37_8. However, if an error has occurred, on IOID the keyboard controller will supply an address of 40_8 through 77_8, automatically indicating error status without software overhead.

The significance of an error in the keyboard system is that a character has been lost through too great a delay in servicing an interrupt. Thus, if keyboard 14_8 generates an interrupt, address 14 will be given on IOID if there has been no error, but address $14 + 40 = 54_8$ will be given if a character has been lost. This feature allows the software to detect data lost through too heavy of an I/O loading on the system. If too many characters are lost, I/O loading will have to be adjusted.

Since the error condition is the only status condition normally associated with the keyboard, the program will normally not need to check status on this device. Thus, it may be handled with an economical interrupt routine to save software overhead.

Software Polling

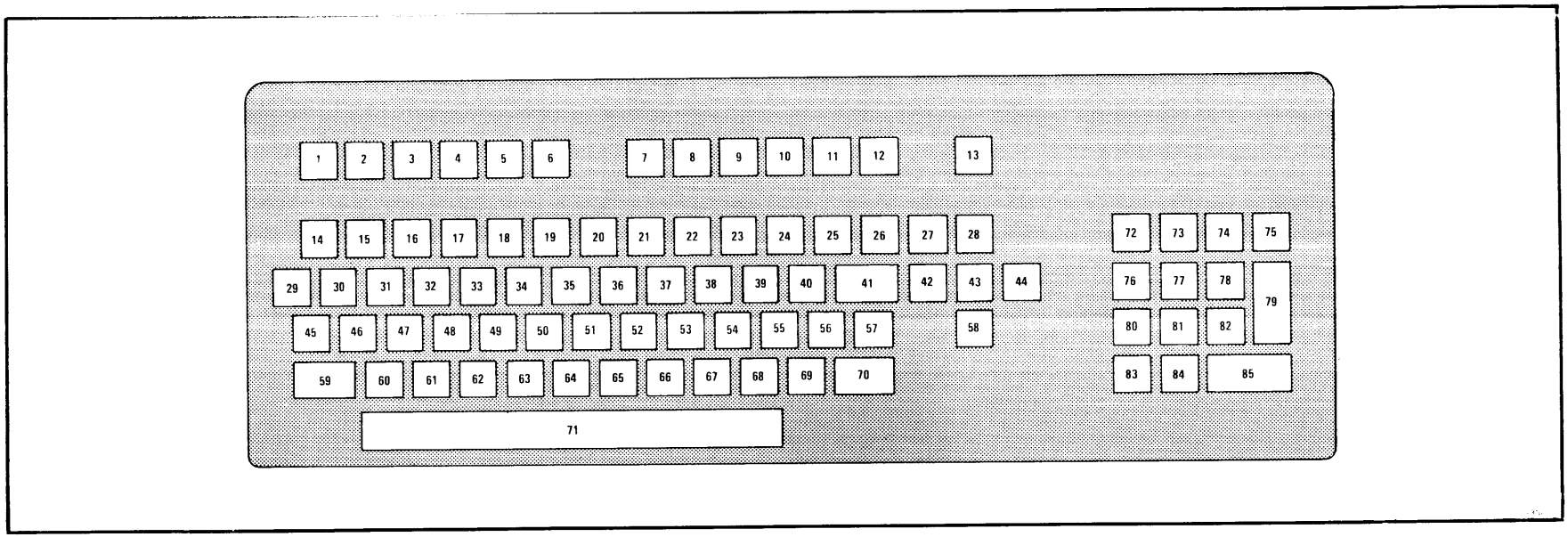
If the keyboard is being used in a software polling environment without hardware interrupts, the keyboard controller will respond to an IO status instruction by putting its unit address ($0\text{-}37_8$) on bits 19-23 of the bus and a status bit (data ready) on bit 16. If bit 16 is set, the program must execute an IO data in instruction to receive the data. If bit 18 is set, a character has been lost. Note the implication that the software does not ask for the status of a given keyboard, but rather polls all the keyboards at once (select word = 00001403). This is because the controller itself operates in a hardware polling scheme and is in contact with only one keyboard at a time. If the character buffer for a keyboard contains a character, the hardware polling stops at that keyboard until an IO data in instruction is executed.

Optional Features

The 7002 Processing Unit allows the attachment of two keyboard features: the Audible Alarm Feature and the Selector Pen Feature.

AUDIBLE ALARM FEATURE

The Audible Alarm Feature on the 7002 Processing Unit is controlled by the software using an IO control instruction. The alarm is sounded once for each control IO sent to the keyboard. When the IO control instruction is given, the first word of the word-pair in memory (the CUT word) must contain the channel and unit address of the selected



Key Numbers

Key No.	7200/7220 Legend	7201 Legend	7202 Legend	7203 Legend	7204 Legend	ASCII Codes Unshift	ASCII Codes Shift	ASCII Codes Control	Remarks
1	CTRL	CTRL	– – –	CTRL	CTRL	– – –	– – –	– – –	Forces control code for any other key pressed at the same time except on 7202. No effect on 7202.
2	F1	PASSW	ASD	ASD	PASSW	0221	0221	0221	Keys 2-13 do not respond to shift or control.
3	F2	SEE	PROG CTRL	PROG CTRL	SEE	0222	0222	0222	
4	F3	SHOW	?	?	SHOW	0223	0223	0223	
5	F4	MONIT	VALID	VALID	MONIT	0224	0224	0224	
6	F5	– – –	INDEX	INDEX	– – –	0225	0225	0225	
7	F6	PRINT	PROG 1	PROG 1	PRINT	0226	0226	0226	
8	F7	ERASE EOL	PROG 2	PROG 2	ERASE EOL	0227	0227	0227	
9	F8	ERASE EOS	PROG 3	PROG 3	ERASE EOS	0230	0230	0230	
10	F9	LOWER CASE	PROG 4	PROG 4	LOWER CASE	0231	0231	0231	
11	F10	REST	PROG 5	PROG 5	REST	0232	0232	0232	
12	F11	START	PROG 6	PROG 6	START	0233	0233	0233	

Key No.	7200/7220 Legend	7201 Legend	7202 Legend	7203 Legend	7204 Legend	ASCII Codes Unshift	ASCII Codes Shift	ASCII Codes Control	Remarks
13	ATTN	ATTN	MODE	MODE	ATTN	0205	0205	0205	
14	! 1	! 1	MULT	! 1	– – –	061	041	0261	
15	" 2	" 2	= @	" 2	# @	062	042	0262	
16	# 3	# 3	, %	# 3	, %	063	043	0263	
17	$ 4	$ 4	$ *	$ 4	$ *	064	044	0264	
18	% 5	% 5	. <	% 5	. =	065	045	0265	
19	& 6	& 6	TOTAL	& 6	+ +	066	046	0266	
20	' 7	' 7	DUP	' 7	DUP MARK	067	047	0267	
21	(8	(8	- -	(8	- -	070	050	0270	
22	) 9	) 9	0 /	) 9	0 /	071	051	0271	
23	` 0	` 0	– – –	` 0	– – –	060	0140	0260	
24	| _	| _	REL	| _	– – –	055	0135	035	

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Keyboard Character Codes

Key No.	7200/7220 Legend	7201 Legend	7202 Legend	7203 Legend	7204 Legend	ASCII Codes Unshift	Shift	Control	Remarks
25	$\overline{X}$	$\overline{X}$	– – –	AUX DUP	– – –	0134	0137	0174	
26	EXP ↑ ÷	EXP ↑ ÷	– – –	MULT SKIP	– – –	0133	0136	0173	
27	REPT	REPT	REPT	REPT	REPT	– – –	– – –	– – –	"Repeat" Switch. Any key held down with REPT is entered nine times per second.
28	ROLL ↑	ROLL ↑	REC ↑	REC ↑	ROLL ↑	0200	0212	0176	
29	TAB	TAB	CORR RESET	CORR RESET	TAB	0211	0213	0377	
30	Q	Q	+ Q	Q	< Q	0161	0121	021	
31	W	W	$\overline{W}$	W	> W	0167	0127	027	
32	E	E	) E	E	| E	0145	0105	05	
33	R	R	¢ R	R	R	0162	0122	022	
34	T	T	0-8-2 T	T	T	0164	0124	024	
35	Y	Y	| Y	Y	Y	0171	0131	031	
36	U	U	1 U	U	1 U	0165	0125	025	
37	I	I	2 I	I	2 I	0151	0111	011	
38	O	O	3 O	O	3 O	0157	0117	017	
39	P	P	& P	P	& P	0160	0120	020	
40	@ =	@ =	– – –	@ =	– – –	075	0100	000	
41	CURSOR RETURN	NEW LINE	– – –	LEFT ZERO	ENTER	0215	0216	0376	
42	DEL ←	DEL ←	FIELD ←	FIELD ←	DEL ←	0201	0220	0177	
43	ERASE HOME	ERASE HOME	ERASE HOME	ERASE HOME	ERASE HOME	0210	0207	0375	
44	INSRT →	INSRT →	FIELD →	FIELD →	INSRT →	0202	0217	0234	
45	SHIFT LOCK	SHIFT LOCK	SHIFT LOCK	SHIFT LOCK	SHIFT LOCK	– – –	– – –	– – –	Forces shift code for any other key pressed at the same except on 7202. Forces control code on 7202.
46	A	A	A	A	(A	0141	0101	01	
47	S	S	> S	S	) S	0163	0123	023	
48	D	D	: D	D	? D	0144	0104	04	
49	F	F	; F	0-8-2 F	F	0146	0106	06	
50	G	G	¬ G	G	G	0147	0107	07	
51	H	H	' H	H	H	0150	0110	010	
52	J	J	4 J	J	4 J	0152	0112	012	

Key No.	7200/7220 Legend	7201 Legend	7202 Legend	7203 Legend	7204 Legend	ASCII Codes Unshift	Shift	Control	Remarks
53	K	K	5 K	K	5 K	0153	0113	013	
54	L	L	6 L	L	6 L	0154	0114	014	
55	; +	; +	SKIP	; +	FIELD MARK	053	073	033	
56	: *	: *	LEFT ZERO	: *	– – –	052	072	0175	Keys 56 and 57 are combined on 7202. Code generated is the same as key 57.
57	EOM	ENTER		REL	NEW LINE	0204	0214	0237	
58	ROLL ↓	ROLL ↓	REC ↓	REC ↓	ROLL ↓	0203	0206	0236	
59	SHIFT	SHIFT	NUMERIC	SHIFT	SHIFT	– – –	– – –	– – –	Forces shift code for any other key pressed at the same time.
60	Z	Z	Z	Z	, Z	0172	0132	032	
61	X	X	? X	X	X	0170	0130	030	
62	C	C	" C	¢ C	C	0143	0103	03	
63	V	V	= V	V	V	0166	0126	026	
64	B	B	! B	B	B	0142	0102	02	
65	N	N	(N	¬ N	N	0156	0116	016	
66	M	M	7 M	M	7 M	0155	0115	015	
67	< ,	< ,	8 ,	< ,	8 ,	054	074	034	
68	> .	> .	9 .	> .	9 .	056	076	036	
69	? /	? /	AUX DUP	? /	; :	057	077	037	
70	SHIFT	SHIFT	ALPHA	SHIFT	SHIFT	– – –	– – –	– – –	Forces shift on all but 7202. Forces control shift on 7202.
71	– – –	– – –	– – –	– – –	– – –	040	040	040	Space Bar.
72	7	7	– – –	7	– – –	067	067	067	Numeric data island keys do not respond to shift or control keys. 7202 and 7204 have these keys disabled.
73	8	8	– – –	8	– – –	070	070	070	
74	9	9	– – –	9	– – –	071	071	071	
75	TOTAL	TOTAL	– – –	TOTAL	– – –	0235	0235	0235	
76	4	4	– – –	4	– – –	064	064	064	
77	5	5	– – –	5	– – –	065	065	065	
78	6	6	– – –	6	– – –	066	066	066	
79	+ SUB TOTAL	+ SUB TOTAL	– – –	+ SUB TOTAL	– – –	053	053	053	
80	1	1	– – –	1	– – –	061	061	061	
81	2	2	– – –	2	– – –	062	062	062	
82	3	3	– – –	3	– – –	063	063	063	
83	0	0	– – –	0	– – –	060	060	060	
84	.	.	– – –	.	– – –	056	056	056	
85	-	-	– – –	-	– – –	055	055	055	

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Keyboard Character Codes (Continued)

keyboard, plus control type (10 in bits 22-23). The contents of the second word of the pair are irrelevant. The buffer pointer (second word) is not incremented by one, and the word it points to (if any) is not sent to the controller.

SELECTOR PEN FEATURE

Selector Pen Feature on the 7002 Processing Unit employs an interaction between the video display and the keyboard, operating together under software control. The Selector Pen is connected to the keyboard in such a manner that, whenever the switch on the Selector Pen goes closed, and whenever the photocell on the Selector Pen senses a transition between dark and light with the switch closed, the keyboard logic generates an interrupt to the computer. When this interrupt is serviced, the keyboard logic sends the special character code 0241, which is reserved for the use of the Selector Pen Feature.

In general, the Selector Pen is intended to be used for menu-selection implementation, where the user touches the Selector Pen against a point (rectangular cursor: Four-Phase ASCII 032) to select the item indicated by the text associated with the selected point. The method for implementing this is to have the software display the rectangular cursors when the first 0241 interrupt is received and wait a required period to see if the Selector Pen interrupt is received again. If it is, the software should blank the cursors again for a required period, then display only half of them and wait for an interrupt with the 0241 character. If the interrupt is not received, the software should split the nondisplayed half of the screen and fill half of it with cursors, looking for the Selector Pen. In this manner, if the MVE instruction is used (which moves words rapidly in blocks), a binary search can be performed to locate the word that is selected. Then, if it is required to locate the exact byte within the word, the cursor can be blinked in each byte location of the word until the required character location is found.

Often, of course, the software will not be required to locate the exact byte location, but only a given line or some other specified part of the screen. If so, a simpler search method can be derived.

The following timing considerations are derived from the hardware nature of the Selector Pen and from timings connected with the video signal used by Four-Phase Systems. The basic unit of time in the system is nominally 17 milliseconds — for example, the software is required to hold the cursor characters on the screen for at least 17 milliseconds. If a hit is made, the software can expect to receive a 0241 interrupt within 31 milliseconds. At the end of the 17 milliseconds the software should blank the screen out. If no 0241 interrupt is received, the partial pattern may be displayed after a delay of two 17-millisecond periods (34 milliseconds). If the 0241 interrupt is received, the screen must be kept blanked for a minimum of three 17-millisecond periods (51 milliseconds). This allows time for the hardware in the Selector Pen to reset itself. Thus, each try in the search requires at least 51 milliseconds if no hit is found under the Selector Pen, and at least 68 milliseconds if a hit is found. Therefore, the average decision time is approximately 60 milliseconds.

The following considerations will help in designing a routine to count time under the interrupt system: Each disc sector read or written under $IDISC (the currently-supported interrupt disc utility) requires 5 milliseconds; each character processed from the keyboard under the 2260 Simulator requires 1 millisecond; a MVE 63 instruction requires 1/2 millisecond.

VIDEO DISPLAY OUTPUT

The video display output is unique in that the usual I/O structure is not invoked in controlling its display. Rather, character information is taken directly from the computer's main memory, used to generate video information, and displayed in the form of letters, numbers, and symbols. The character information thus generated can come from the keyboard associated with the particular display in question or may be generated by the software. The character codes and corresponding display outputs are shown in Appendix A of the "System IV/70 Computer Reference Manual," along with a photograph showing the display characters. Note that octal codes of 200 or greater from the keyboard are used strictly for control purposes and are never displayed; the keyboard program must route these characters to a control routine rather than displaying them. If a code of 0200 or greater is stored in a display area, it will be treated modulo 0200 by the video circuits.

Similarly, programs that use codes as control characters rather than display characters (e.g., 0176 "control ↑" and 0177 "control ←") must route these characters to the control program.

Although certain memory areas are dedicated for display purposes, there is no restriction against the programmer using these areas for other purposes, such as storage of data or instructions. It must be understood, however, that garbage may be displayed on the screens associated with these areas. The hardware allows for selecting (at time of manufacture) screen formats of either 48 or 81 characters per line. At time of installation, the user may select 6, 12, or 24 lines for the 48-character format and 6, 12, or 24 lines for the 81-character format. The number of lines per screen may be altered in the field, but not the line length. The exact addresses of the memory areas dedicated to the 48 and 81 character screen formats are shown in the table "Dedicated Memory Locations". Display format sheets for use with the two video systems are shown in accompanying illustrations.

FOUR-PHASE SYSTEMS, INC.

DISPLAY FORMAT SHEET
(48 CHARACTERS/ROW)

SIV/70–05–2A

PROGRAM	COMMENTS	PAGE OF
PROGRAMMER		DATE

ROW	OCTAL ADDRESS	COLUMN 1 2 3	4 5 6	7 8 9	10 11 12	13 14 15	16 17 18	19 20 21	22 23 24	25 26 27	28 29 30	31 32 33	34 35 36	37 38 39	40 41 42	43 44 45	46 47 48
		OCTAL ADDRESS 00	01	02	03	04	05	06	07	10	11	12	13	14	15	16	17
1	60																
2	100																
3	120																
4	140																
5	160																
6	200																
7	220																
8	240																
9	260																
10	300																
11	320																
12	340																
13	360																
14	400																
15	420																
16	440																
17	460																
18	500																
19	520																
20	540																
21	560																
22	600																
23	620																
24	640																

B047B

48 Character Line Display Format

FOUR-PHASE SYSTEMS, INC.

DISPLAY FORMAT SHEET
(81 CHARACTERS/ROW)

SIV/70-05-3A

PROGRAM	COMMENTS	PAGE OF
PROGRAMMER		DATE

ROW	OCTAL ADDRESS	COLUMN 1 2 3	4 5 6	7 8 9	10 11 12	13 14 15	16 17 18	19 20 21	22 23 24	25 26 27	28 29 30	31 32 33	34 35 36	37 38 39	40 41 42	43 44 45	46 47 48	49 50 51	52 53 54	55 56 57	58 59 60	61 62 63	64 65 66	67 68 69	70 71 72	73 74 75	76 77 78	79 80 81
		OCTAL ADDRESS 00	01	02	03	04	05	06	07	10	11	12	13	14	15	16	17	20	21	22	23	24	25	26	27	30	31	32
VIDEO AREA A																												
1	140																											
2	200																											
3	240																											
4	300																											
5	340																											
6	400																											
7	440																											
8	500																											
9	540																											
10	600																											
11	640																											
12	700																											
VIDEO AREA B																												
1	740																											
2	1000																											
3	1040																											
4	1100																											
5	1140																											
6	1200																											
7	1240																											
8	1300																											
9	1340																											
10	1400																											
11	1440																											
12	1500																											

B048C

81 Character Line Display Format

Octal Location	Function	Octal Location	Function
00000	Interrupt level 0	00012	Interrupt level 5
00002	Interrupt level 1	00014	Interrupt level 6
00004	Interrupt level 2	00016	Interrupt level 7
00006	Interrupt level 3	00041	Arithmetic Trap, Supervisory Trap
00010	Interrupt level 4		
7001, 48 Character/Line Video Systems†		7001, 81 Character/Line Video Systems†	
00060-00657	Video display area A	00140-00732‡	Video display area A
01060-01657	Video display area B	00740-01532‡	Video display area B
02060-02657	Video display area C	02140-02732‡	Video display area C
03060-03657	Video display area D	02740-03532‡	Video display area D
04060-04657	Video display area E	04140-04732‡	Video display area E
05060-05657	Video display area F	04740-05532‡	Video display area F
06060-06657	Video display area G	06140-06732‡	Video display area G
07060-07657	Video display area H	06740-07532‡	Video display area H
7002, 48 Character/Line Video Systems†		7002, 81 Character/Line Video Systems†	
00060-00657	Video display area 000	00140-00732‡	Video display area 00
01060-01657	Video display area 001	00740-01532‡	Video display area 01
02060-02657	Video display area 002	02140-02732‡	Video display area 02
03060-03657	Video display area 003	02740-03532‡	Video display area 03
04060-04657	Video display area 004	04140-04732‡	Video display area 04
05060-05657	Video display area 005	04740-05532‡	Video display area 05
06060-06657	Video display area 006	06140-06732‡	Video display area 06
07060-07657	Video display area 007	06740-07532‡	Video display area 07
10060-10657	Video display area 010	10140-10732‡	Video display area 010
11060-11657	Video display area 011	10740-11532‡	Video display area 011
12060-12657	Video display area 012	12140-12732‡	Video display area 012
13060-13657	Video display area 013	12740-13532‡	Video display area 013
14060-14657	Video display area 014	14140-14732‡	Video display area 014
15060-15657	Video display area 015	14740-15532‡	Video display area 015
16060-16657	Video display area 016	16140-16732‡	Video display area 016
17060-17657	Video display area 017	16740-17532‡	Video display area 017
20060-20657	Video display area 020	20140-20732‡	Video display area 020
21060-21657	Video display area 021	20740-21532‡	Video display area 021
22060-22657	Video display area 022	22140-22732‡	Video display area 022
23060-23657	Video display area 023	22740-23532‡	Video display area 023
24060-24657	Video display area 024	24140-24732‡	Video display area 024
25060-25657	Video display area 025	24740-25532‡	Video display area 025
26060-26657	Video display area 026	26140-26732‡	Video display area 026
27060-27657	Video display area 027	26740-27532‡	Video display area 027
30060-30657	Video display area 030	30140-30732‡	Video display area 030
31060-31657	Video display area 031	30740-31532‡	Video display area 031
32060-32657	Video display area 032	32140-32732‡	Video display area 032
33060-33657	Video display area 033	32740-33532‡	Video display area 033
34060-34657	Video display area 034	34140-34732‡	Video display area 034
35060-35657	Video display area 035	34740-35532‡	Video display area 035
36060-36657	Video display area 036	36140-36732‡	Video display area 036
37060-37657	Video display area 037	36740-37532‡	Video display area 037

† Video systems with 40 or 80 characters/line are achieved by programming blanks in the appropriate character positions.

‡ There are 5 unused memory locations at the end of each video line for 81 character/line systems. For example, the characters for the first line of area A occupy locations 00140-00172 while the second line of characters occupies locations 00200-00232.

A312A

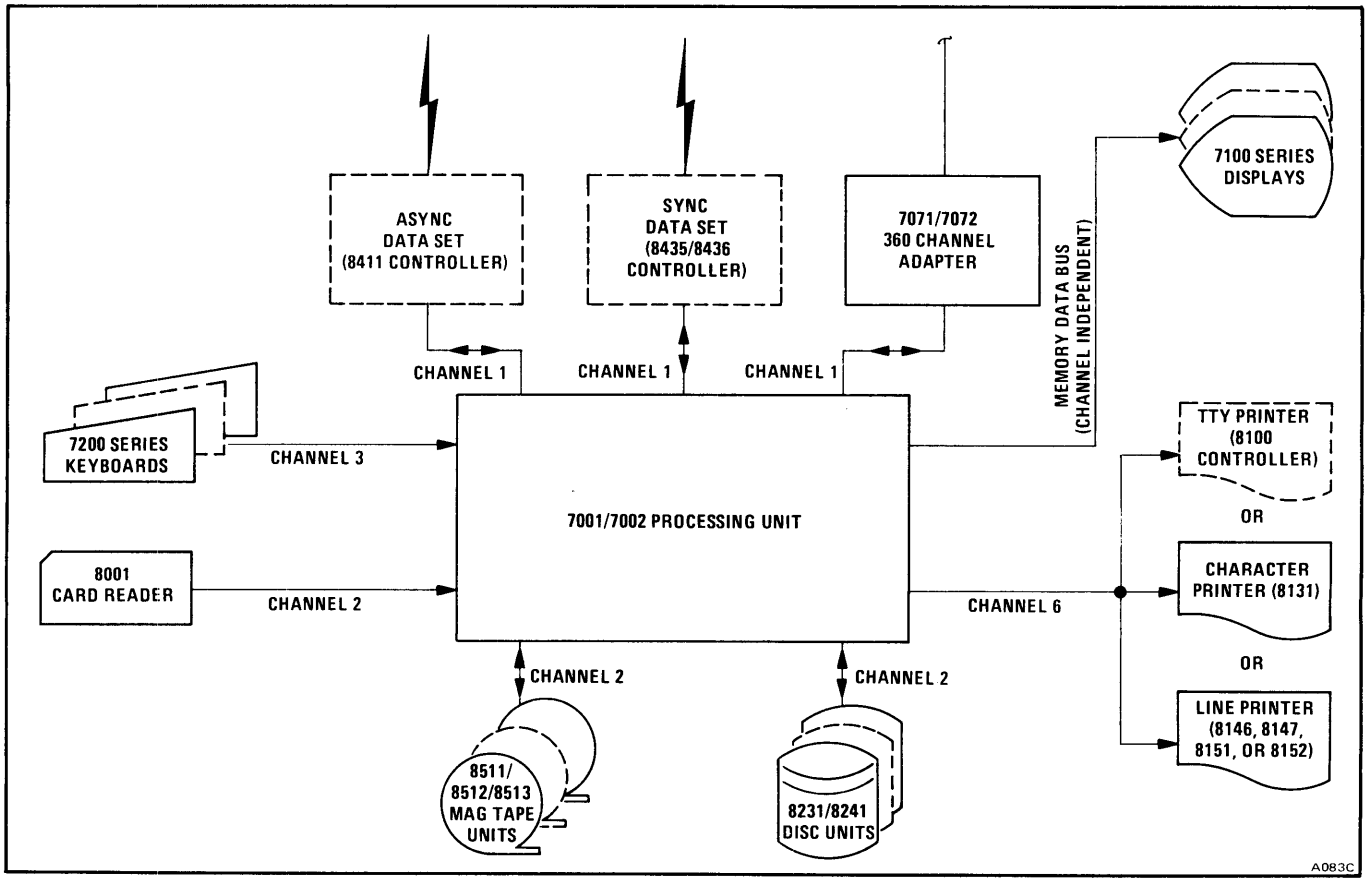
Dedicated Memory Locations

Section 3
Peripheral Devices

The peripheral devices described in this manual all interface with the System IV/70 Computer using Four-Phase Systems peripheral controller cards. These cards perform the actual tasks of controlling the peripherals, receiving and buffering data (input or output), testing and communicating status, etc. Except for special instances noted in the individual sections, the programmer may assume that he is programming for the peripheral controller card appropriate to his peripheral device.

Software supported by Four-Phase Systems assumes that the peripheral units are assigned to specific channel and unit addresses. These addresses are listed in the table, "Four-Phase Standard I/O Priority Assignments." The standard I/O devices are configured as shown in the illustration, "Typical System IV/70 Configuration."

The following sections describe each peripheral device from the programmer's viewpoint, noting special features and programming specifications. Status messages and command messages will be listed as appropriate. Examples of working programs will be given for selected devices. Note that "output" indicates a transfer from the computer to the peripheral unit unless otherwise indicated; "input" indicates data flow into the computer.



Typical System IV/70 Configuration

Channel Number	Unit Number (Octal)	Select Word‡ (Octal)	Device Description
0	—	—	Reserved for real time clock: an INR instruction is placed in memory location 0 and a 60 Hz clock is tied to the int 0 line on Interface Card 1.
1†	33	0554	Synchronous Data Set (8435/8436)
1	35	0564	Asynchronous Data Set (8411) or other interactive device
1	50‡	0640	360 Channel Adapter (7070 Series); initial interrupt
1	51‡	0644	360 Channel Adapter (7070 Series); continue interrupt
1	52‡	0650	360 Channel Adapter (7070 Series); end interrupt
1	53‡	0654	360 Channel Adapter (7070 Series); data in/out
2†	20‡	1100	Card Reader (8001); character ready
2	22‡	1110	Card Reader (8001); end of card
2	24	1120	Disc 0 (8231)
2	25	1124	Disc 1
2	26	1130	Disc 2
2	27	1134	Disc 3
2	40	1200	Disc 0 (8241)
2	41	1204	Disc 1
2	42	1210	Disc 2
2	43	1214	Disc 3
2	44	1220	Mag Tape 0 (8511/8512/8513); data interrupt
2	45	1224	Mag Tape 1; status interrupt
2	46	1230	Mag Tape 2
2	47	1234	Mag Tape 3
3†	0-37	1400-1574	Keyboard Units (7200 Series) 0 through 37_8, data ready, no error.
3	40-77	1600-1774	Keyboard Units 0 through 37_8, data ready, character lost.
4	—	—	Reserved for interrupt caused by INR instruction in address 0: a BRM instruction to a clock counter routine is placed in address 10_8 and the "int on Z" line from the CPU Card is tied to the int 4 line on Interface Card 1.
5			Not assigned
6†	30	3140	Line Printer
6	31	3144	Character Printer
6	36	3170	Keyboard/Printer (8100/8101)
7	—	—	Reserved for low priority processing: a BRM instruction is placed in address 16_8 and external command line 3 (EXC_3) is tied to the int 7 line on Interface Card 1. This allows an interrupt on channel 7 to be generated by using the corresponding EXCT instruction (EXCT EA, where [EA] = 1) in a higher priority interrupt routine.

† Memory Locations 02, 04, 06, and 014_8 contain an IOID instruction.

‡ When this device is identifying itself, it uses the unit numbers corresponding to its present status. However, when the device is being selected by an IO or IOB instruction, the instruction always uses the lowest unit number (for example 50 for the channel adapter).

‡ Not including the "type" field.

A096D

Four-Phase Standard I/O Priority Assignments

7071/7072
Channel Adapter

The 7071/7072 Channel Adapter allows the System IV/70 to interface with a System/360 or System/370 in the 2848 local mode; in addition, further capability may be achieved by additional programming for the IV/70 and the 360/370. The 7071 interfaces with the 7001 Processing Unit; the 7072 with the 7002. They are identical in operation.

Provision is made for operating the IV/70 with 32 video/keyboard terminals and a system printer. With certain restrictions it is possible to operate the System IV/70 with the 8001 Card Reader, 8231 Disc Unit, and/or 8511/8512/8513 Magnetic Tape Unit when the channel adapter is connected.

The channel adapter may be attached to either the selector or the multiplexor channel of the 360/370, and will transfer data a byte at a time, as required by the type of channel. In either case, the IV/70 software will be the same, and the operation will appear the same in all ways from the viewpoint of the IV/70, except that the multiplexor channel will often operate slower than the selector channel.

On either channel, the channel adapter operates with the IV/70 by transferring three bytes per transfer, issuing an interrupt for each word required (on output to the channel) or presented (on input from the channel). In this manner, the rate of transfer is controlled by the 360/370 channel, up to the maximum data rate of the System IV/70 in the word-per-interrupt mode, which is 39,000 bytes per second. When operating in this mode at maximum speed, the IV/70 Processing Unit will be completely loaded and time for other processing will not be available, although interrupts on higher levels will be processed as usual; this will slow down the data transfer. This may preclude the use of other I/O devices in the same time frame with the channel adapter.

All data communication over the channel adapter is assumed to use purely character data. The IV/70 interface is in the augmented 8-bit ASCII defined by Four-Phase Systems†. The 360 interface uses an augmented 8-bit EBCDIC. See the tables "ASCII to EBCDIC Conversion" and "EBCDIC to ASCII Conversion" for the conversions between these two codes. Although the standard IBM software is limited to the 64-character code defined for the 2260/2848‡, any character transactions across the interface can be accommodated if both software systems are prepared.

† See "System IV/70 Computer Reference Manual," Four-Phase document SIV/70—11—1, Appendix A.

‡ See "IBM System/360 Component Description: IBM 2260 Display Station, IBM 2848 Display Control," IBM Form A27-2700-4, Page 26.

The channel adapter performs all high-speed functions required by the 2848 local mode interface: sense byte, status byte, and control sequences are performed (as defined in IBM Form A27-2700-4, Pages 34-36 and related documentation) and all tag line operations are performed by the channel adapter. The channel adapter also decodes 360/370 commands to the 2848 local and performs address decoding to enable the IV/70 to respond quickly as required by the 360/370 channel. The channel adapter performs data transfer functions required for interfacing the two machines by passing data both ways as required by the 360/370 and the IV/70. The adapter also sets the attention bit for the 360/370 and sets status signals for the IV/70 as required by the 360/370's control sequences.

The channel adapter issues interrupt requests to the IV/70 to initiate various data transactions. The interrupts are made on different unit (IOID) addresses, as required by system considerations. Depending on the type of interrupt, the unit address will be one of four addresses as follows:

Unit Address	Type of Interrupt	Meaning
50	New Command‡	A new command has been issued by the channel.
51	Continue‡	Continue the old command; a NL has been received from the 360/370 or the IV/70, or channel adapter byte count is zero.
52	End of Operation‡	The operation (read or write) is terminated by order of the channel or channel adapter.
53	Data	Signals the Processing Unit that either the read buffer is empty or the write buffer is full.

The channel adapter also performs specific character recognition functions for the interface when the code converter is turned on. If a 2260 EOM character (ASCII 023 or 0223) is received from the IV/70 during a "read MI" or "short read MI", the channel adapter will start a Control Unit initiated disconnect sequence. If the channel adapter receives a NL (ASCII 04 or 0204) from the IV/70 during a "read MI" or "short read MI", it will terminate reading the IV/70

‡ The IV/70 software should request status from the channel adapter whenever one of these changes occur.

Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)
000	00	040	40	100	7C	140	79	200	20	240	70	300	90	340	CC
001	01	041	4F	101	C1	141	81	201	21	241	41	301	9A	341	CD
002	02	042	7F	102	C2	142	82	202	22	242	42	302	9D	342	CE
003	03	043	7B	103	C3	143	83	203	23	243	43	303	9E	343	CF
004	37	044	5B	104	C4	144	84	204	15	244	44	304	9F	344	DC
005	2D	045	6C	105	C5	145	85	205	15	245	45	305	AA	345	DD
006	2E	046	50	106	C6	146	86	206	06	246	46	306	AC	346	DE
007	2F	047	7D	107	C7	147	87	207	17	247	47	307	AD	347	DF
010	16	050	4D	110	C8	150	88	210	28	250	48	310	AE	350	EC
011	05	051	5D	111	C9	151	89	211	29	251	49	311	AF	351	ED
012	25	052	5C	112	D1	152	91	212	2A	252	51	312	BA	352	EE
013	0B	053	4E	113	D2	153	92	213	2B	253	52	313	BB	353	EF
014	0C	054	6B	114	D3	154	93	214	2C	254	53	314	BC	354	FC
015	7F	055	60	115	D4	155	94	215	09	255	54	315	BD	355	FD
016	5F	056	4B	116	D5	156	95	216	0A	256	55	316	BE	356	FE
017	0F	057	61	117	D6	157	96	217	1B	257	56	317	BF	357	B9
020	10	060	F0	120	D7	160	97	220	30	260	57	320	71	360	CA
021	11	061	F1	121	D8	161	98	221	31	261	58	321	72	361	CB
022	12	062	F2	122	D9	162	99	222	1A	262	59	322	73	362	DA
023	6A	063	F3	123	E2	163	A2	223	33	263	62	323	74	363	DB
024	3C	064	F4	124	E3	164	A3	224	34	264	63	324	75	364	EA
025	3D	065	F5	125	E4	165	A4	225	35	265	64	325	76	365	EB
026	32	066	F6	126	E5	166	A5	226	36	266	65	326	77	366	FA
027	26	067	F7	127	E6	167	A6	227	08	267	66	327	78	367	FB
030	18	070	F8	130	E7	170	A7	230	38	270	67	330	B1	370	80
031	19	071	F9	131	E8	171	A8	231	39	271	68	331	B2	371	A0
032	3F	072	7A	132	E9	172	A9	232	3A	272	69	332	B3	372	B0
033	27	073	5E	133	4A	173	C0	233	3D	273	8A	333	B4	373	8B
034	1C	074	4C	134	E0	174	6A	234	04	274	8C	334	B5	374	9B
035	1D	075	7E	135	4F	175	D0	235	14	275	8D	335	B6	375	AB
036	4A	076	6E	136	5F	176	A1	236	3E	276	8E	336	B7	376	9C
037	1F	077	6F	137	6D	177	07	237	E1	277	8F	337	B8	377	FF

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ASCII to EBCDIC Conversion

IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)	IBM EBCDIC (Hex)	Four-Phase ASCII (Octal)
00	000	20	200	40	040	60	055	80	370	A0	371	C0	173	E0	134
01	001	21	201	41	241	61	057	81	141	A1	176	C1	101	E1	237
02	002	22	202	42	242	62	263	82	142	A2	163	C2	102	E2	123
03	003	23	203	43	243	63	264	83	143	A3	164	C3	103	E3	124
04	234	24	204	44	244	64	265	84	144	A4	165	C4	104	E4	125
05	011	25	012	45	245	65	266	85	145	A5	166	C5	105	E5	126
06	206	26	027	46	246	66	267	86	146	A6	167	C6	106	E6	127
07	177	27	033	47	247	67	270	87	147	A7	170	C7	107	E7	130
08	227	28	210	48	250	68	271	88	150	A8	171	C8	110	E8	131
09	215	29	211	49	251	69	272	89	151	A9	172	C9	111	E9	132
0A	216	2A	212	4A	036	6A	023	8A	273	AA	305	CA	360	EA	364
0B	013	2B	213	4B	056	6B	054	8B	373	AB	375	CB	361	EB	365
0C	014	2C	214	4C	074	6C	045	8C	274	AC	306	CC	340	EC	350
0D	015	2D	005	4D	050	6D	137	8D	275	AD	307	CD	341	ED	351
0E	016	2E	006	4E	053	6E	076	8E	276	AE	310	CE	342	EE	352
0F	017	2F	007	4F	135	6F	077	8F	277	AF	311	CF	343	EF	353
10	020	30	220	50	046	70	240	90	300	B0	372	D0	175	F0	060
11	021	31	221	51	252	71	320	91	152	B1	330	D1	112	F1	061
12	022	32	026	52	253	72	321	92	153	B2	331	D2	113	F2	062
13	023	33	223	53	254	73	322	93	154	B3	332	D3	114	F3	063
14	235	34	224	54	255	74	323	94	155	B4	333	D4	115	F4	064
15	204	35	225	55	256	75	324	95	156	B5	334	D5	116	F5	065
16	010	36	226	56	257	76	325	96	157	B6	335	D6	117	F6	066
17	207	37	004	57	260	77	326	97	160	B7	336	D7	120	F7	067
18	030	38	230	58	261	78	327	98	161	B8	337	D8	121	F8	070
19	031	39	231	59	262	79	140	99	162	B9	357	D9	122	F9	071
1A	222	3A	232	5A	135	7A	072	9A	301	BA	312	DA	362	FA	366
1B	217	3B	233	5B	044	7B	043	9B	374	BB	313	DB	363	FB	367
1C	034	3C	024	5C	052	7C	100	9C	376	BC	314	DC	344	FC	354
1D	035	3D	025	5D	051	7D	047	9D	302	BD	315	DD	345	FD	355
1E	036	3E	236	5E	073	7E	075	9E	303	BE	316	DE	346	FE	356
1F	037	3F	032	5F	016	7F	015	9F	304	BF	317	DF	347	FF	377

B219A

EBCDIC to ASCII Conversion

and send a continue interrupt to the IV/70. If the NL is received from the 360/370 channel (EBCDIC hex 15) during a write, the channel adapter will send a continue interrupt instead of a data interrupt to the IV/70.

Note that, to the character recognition feature, 023 or 0223 will be recognized as EOM and 04 or 0204 will be recognized as NL; to the code converter, 023 is required for EOM and 0204 for NL.

STATUS CHECKING

The channel adapter generates a status word to the Processing Unit in response to a status I/O instruction. This status word may be of two types: normal or diagnostic, depending on bit 0 of the control word (see "Control Signals").

When reading status or control words, note that all fields and addresses read from left to right (i.e., low bit numbers to high bit numbers).

Normal Status

The normal status word is formatted as follows:

Bit	Name	Meaning
23-16	Device Address	Valid only when bits 7-6 = 0. 23-20 = device within 2848 19-16 = 2848 address
15-14	Ending Byte Position	Only valid for the last word of a write; bits 7-6 must be 1, 2, or 3. 0 = last word full (3 bytes of data) 1 = last word has 1 byte (left just) 2 = last word has 2 bytes (left just)
15-12	Line Address	Four-bit line address ($0\text{-}13_8$) if bits 7-6 = 0 and bits 11-9 = 2 (new command only).
11-9	Command Code	The following commands are specified by the command byte from the channel. 0 = No command 1 = Write buffer (screen or printer) 2 = Write line address 3 = Erase buffer 4 = Not used 5 = Read manual input 6 = Short read manual input 7 = Read full buffer
8	Keyboard Lock	Do not restore the keyboard at the end of the current operation.
7-6	Type	0 = New command (channel initiated sequence; command from 360/370 indicated by status bits 9-11). 1 = Continue the old command. 2 = End operation. The operation (read or write) is terminated by order of the channel. 3 = End operation.
5	Printer Status Request	Device end required when printer operation complete.
4		Not used.
3	System Reset	System reset for the channel. All video screens are cleared, the cursors are returned to home position, the keyboards are restored, and all transfers are terminated.
2	Enable/ Disable	0 = Enable (the IV/70 is on-line) 1 = Disable (the IV/70 is off-line)
1	Attention or Device End Accepted	Attention (control bit 12) or device end (control bits 7, 13) is accepted by the controller and sent to the channel. If the controller is busy with the IV/70 or the channel, it will not accept attention or device end.
0	Data	Signals the Processing Unit that the read buffer is empty and needs a new data word, or that the write buffer is full and data is ready to be transferred.

Diagnostic Status

When the Processing Unit control word specifies diagnostic status (bit 0 = 1), the channel adapter enables a four-word buffer. This buffer, in response to a status I/O instruction, is gated onto the data bus in a four-word lockup burst. These words reflect the levels of various signals within the channel adapter as shown in the illustration "Diagnostic Status Words." These status words are intended for diagnostic programs developed by Four-Phase Systems.

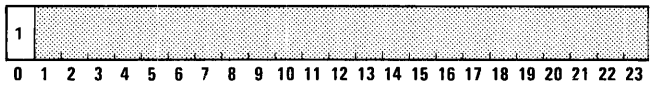
CONTROL SIGNALS

Five types of control words are accepted by the channel adapter. They are all one word in length and are distinguished by the presence of "ones" in certain bit configurations. Thus, it is illegal and uncertain results will occur if a control word is sent that contains "ones" for more than one type of control. The 5 types are: diagnostic control, initialization control, load byte control, load bit register control, and load address register control.

Diagnostic Control

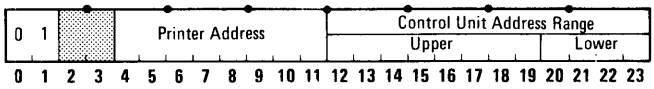
The diagnostic control word is used only by diagnostic programs. It places the channel adapter in the diagnostic

mode. The next I/O *should* be a status, which will read 4 words of diagnostic information into four consecutive memory locations starting at the buffer address location. This status condition is reset when read. The diagnostic control word is formatted as follows:



Initialization Control

The initialization control word sets the address recognition logic in the channel adapter to the range of device addresses expected from the 360/370. These addresses are usually considered as hex digits (i.e., 4 bits to each digit). The initialization control word is formatted as follows:



Bit	Name	Meaning
23-20	Lower Control Unit Address Range	The most significant hex digit of the lowest 2848 address.
19-12	Upper Control Unit Address Range	The actual hex device address (2 digits) of the highest address recognized not including the printer address.

Bit	Signal			
	Word 0	Word 1	Word 2	Word 3
0	BOOT Address Equal	Interrupt	Interrupt Request 1 & 2	Data Interrupt
1	Upper ≠ and Lower ≠	Upper Less or Equal	Printer Address Equal	Upper Less
2	– – –	– – –	Control Unit Request	Clocked Read Buffer Full
3	– – –	BOOT Address Ok	Channel Request	Write Buffer Full
4	IV/70 Buffer Full	Read Buffer Full	Device Busy	Allow Write
5	Convert	Status Request	Control Unit Busy	Request Next Word
6	Bus Out Parity Ok	Service Request	Adapter Busy	Continue
7	Not Enable Bus In	Printer Intervention Required	Interface Busy	End Op
8	DB1-0	Address Ok	Proceed	Hold/Select Out Gated
9	DB1-1	Test I/O	Map	Allow Bus
10	DB1-2	No Op	360 System Reset	Stop
11	DB1-3	Sense	Load Line Address Register	Allow Request In
12	DB1-4	Gate Address to Address Register	Attention	Attention Accepted
13	DB1-5	Printer Busy	Done	Under Flow
14	DB1-6	Intervention Required	Byte Counter Lo-A	First Byte
15	DB1-7	Gate Bus In-A	Byte Counter Lo-B	Read
16	Internal Bus Out-0	Gate Bus In-B	Byte Counter Lo-C	Write
17	Internal Bus Out-1	Bus Out Check	Byte Counter Lo-D	Stack
18	Internal Bus Out-2	Command Reject	Byte Position 0	Bus and Status
19	Internal Bus Out-3	Control Unit End	Byte Position 1	Read Special
20	Internal Bus Out-4	Command Chain	Byte Position 2	Printer Request Device End
21	Internal Bus Out-5	Channel End	Load Byte 0	EOM Character IV/70
22	Internal Bus Out-6	Device End	Load Byte 1	NL Character From IV/70
23	Internal Bus Out-7	Unit Check	Load Byte 2	NL Character From Channel

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Diagnostic Status Words

Bit	Name	Meaning
11-4	Printer Address	A unique address for printer applications. If no printer is specified, it must be set to hex FF. For 2260 local applications, it is set to the first address higher than the upper control unit address range. For special applications (printer or nonprinter), it can be set to any address outside the range of upper-lower.

ADDRESSING SCHEME

The printer address requires a unique match from the bus-out lines. All other device addresses require that the high-order hex digit of bus out (bits 0 to 3) be equal to the high-order hex digit of upper (bits 12 to 15) or to the hex digit of lower. If a match occurs with the high-order hex digit of upper, the low-order hex digit on bus out (bits 4 to 7) must be equal to or less than the low-order hex digit of upper (bits 16 to 19). Note that examples 4 and 5 are incompatible with Four-Phase 2260 local implementation, which does not support split 2848 addressing.

EXAMPLES:

Case 1: 10 video terminals (2260's), no printer, 2848 address = 40_{16}.

Printer = FF
Upper = 49
Lower = 4

Case 2: Same as case 1 except with printer.

Printer = 4A
Upper = 49
Lower = 4

Case 3: Same as case 1 except 20 video terminals.

Printer = FF
Upper = 53
Lower = 4

Case 4: Same as case 3 except second 2848 not consecutive but = 70_{16}.

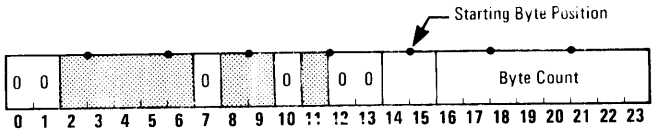
Printer = FF
Upper = 73
Lower = 4

Case 5: 33 devices, first group 20 - 2F, second is A0 - AF, last is D0.

Printer = D0
Upper = AF
Lower = 2

Load Byte Control

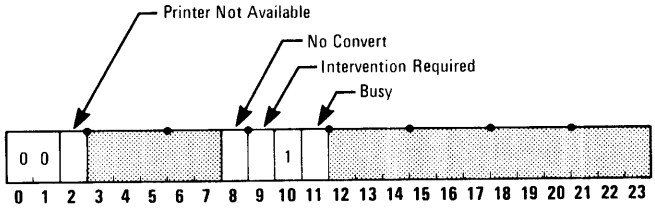
The load byte control word establishes the starting byte position of the first word of data to be transferred to or from the channel and the number of bytes to be transferred. It is used only in response to an initial or continue interrupt. Once issued, it allows the channel adapter to request a data transfer to or from the 360/370. Data interrupts (53_8) are not permitted until load byte control is received. The load byte control word is formatted as follows:



Bit	Name	Meaning
23-16	Byte Count	The maximum number of bytes to be transferred to or from the 360/370. When the count goes to zero, continue interrupt is issued. Overridden by "Channel Initiated Stop Sequence", a NL character, or an EOM character during read MI or short read. In normal usage the byte count is set equal to the number of bytes from the current position (cursor) to the end of the line. Hence, for the 2260 simulator, the maximum is 40 or 80.
15-14	Starting Byte Position	00 = left, 01 = middle, 10 = right, and 11 = illegal.
13-0		Must be zero.

Load Bit Register Control

The load bit register control word sets the state of four flip-flops: printer not available, no convert, printer intervention required, and printer busy. System reset forces all four flip-flops to the one state. This control word can be issued at any time, however, bits 2 and 8 are required during initialization. Bits 9 and 11 are used during printer I/O operations and are effective only if bit 2 is zero. The load bit register control word is formatted as follows:

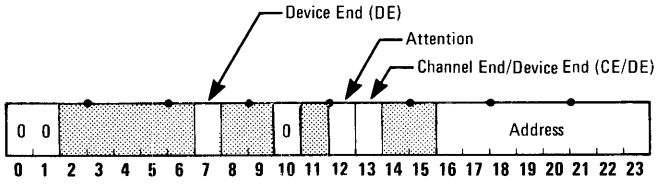


Bit	Name	Meaning
23-12		Not used.
11	Printer Busy	Should be turned on during the initial interrupt for a write printer operation and turned off when the

Bit	Name	Meaning
		printer is physically done printing. Valid only if bit 2 is zero. Printer-status-request status (bit 5) should be checked when changing bit 11 from a one to a zero.
10		Must be a one.
9	Printer Intervention Required	The printer is out of paper or off line for some reason. If the 360/370 tries any printer I/O, it will be rejected by the channel adapter and intervention required will be indicated in the 360/370 sense byte. This bit of the sense byte is also presented in bootstrap mode if the 360 gives other than a write command. Bit 9 is valid only if bit 2 is zero. When the printer becomes available, turn bit 9 off and do a status to check printer-status-request status (bit 5).
8	No Convert	Disables the conversion of EBCDIC to ASCII on input (to the System IV/70) and ASCII to EBCDIC on output.
7-3		Not used.
2	Printer Not Available	The printer logic is disabled. However, the printer address will be recognized.
1-0		Must be zero.

Load Address Register Control

The load address register control word forces the channel adapter to issue a status interrupt to the 360/370. It also indicates one of three status conditions: device end, device and channel end, or attention. The System IV/70 may use this control word to terminate any operation. The load address register control word is formatted as follows:



Bit	Name	Meaning
23-16	Address	Specifies the Control Unit address and the address of the device causing the interrupt. For device end, it is typically the address of the printer. For attention, it may be any legal address within the upper-lower range of the initialization control word. For device and channel end, it must be the same address as indicated in the initial interrupt.
15-14		Not used.
13	Channel End/Device End (CE/DE)	When bit 7 is zero, this bit forces a status interrupt to the 360/370 with the channel end and device end status bits on. This signals the completion of an I/O operation between the IV/70 and the 360/370. It is normally issued in response to the end-of-operation interrupt from the channel adapter. It also indicates that the channel adapter is ready to accept the next I/O command. It can be issued in response to the initial or continue interrupts instead of a load byte control word to force a control unit disconnect sequence. Bit 12 should be zero.
12	Attention	Forces a status interrupt to the 360/370 with the attention bit (bit 0) on. Normally issued when the ENTER key is pressed to indicate that a message is waiting to be transferred. Since the channel adapter will ignore the control if it is busy, the attention accepted status bit (bit 1) should be checked immediately to confirm acceptance. If not, the control must be retried until accepted. Bits 7 and 13 should be zero.
11-8		Must be zero.
7	Device End (DE)	Forces a status interrupt to the 360/370 with the device-end status bit on if bit 13 is on. Device-end accepted status (bit 1) must be checked and if the channel adapter was busy (bit 1 = 0), this control message must be retried. Bit 12 should be zero.
6-0		Must be zero.

SENSE AND STATUS BYTES

The 360/370 sense byte for the channel adapter is:

Bit	Name	Meaning
0	Command Reject	An invalid command or command modifier.
1	Intervention Required	See "Load Bit Register Control", bit 9.
2	BusOut Check	A parity error in a command byte or incoming data byte.
3	Equipment Check	A parity error in data transfer to channel.
4-7		Not used.

The 360/370 status byte for the channel adapter is:

Bit	Name	Meaning
0	Attention	See "Load Address Register Control", bit 12.
1	Status Modifier	Set, along with Busy, during a short control unit busy sequence.
2	Control Unit End	†
3	Busy	†
4	Channel End	†
5	Device End	†
6	Unit Check	†
7		Not used.

PROGRAMMING NOTES

Except for attention, all sequences of signals on the channel interface are initated by the 360 channel. For all these sequences, the channel adapter will accept and decode commands from the 360 and set the appropriate status bits for the System IV/70. The interpretation of read, write, and erase status bits is the function of the IV/70 software, allowing implementation of a flexible interface.

If the System/360 and IV/70 software are properly tailored, short read MI, read MI, read full, erase, write line address, and write data station commands can be given interpretations other than those outlined for the standard 2848/2260‡, with the reservation that write commands must be used to initiate transfers to the IV/70 and read commands must be used for transfers to the 360. In addition, the keyboard restore modifier bit can be used for other meanings as determined in the software design.

In addition, with the code converter turned off, the full range of 256 possible bit combinations per byte may be sent in either direction over the interface, so that word-oriented data or other bit configurations may be transmitted. The bootstrap mode makes use of this feature. If the NL and EOM decode feature is to be disabled at all times, a jumper is provided on the channel adapter controller to disable conversion.

The usual sequence of events for transferring data is as follows: first the channel and IV/70 exchange command and status bits to initiate a read or write sequence. The first interrupt for a data transfer will be a new command interrupt which the IV/70 should respond to with a load byte control. When the data transfer begins, each word of data (single byte mode) or each block (other modes) will be transferred to the channel adapter using the data interrupt. This interrupt can be serviced using a single IO instruction stored in the IOID table, at relative location 053.

When a full block of data (either a display line or other block of data) has been transferred, the channel adapter will give the IV/70 a continue interrupt; the IV/70 should respond to continue by taking and checking status. If status is ok, the IV/70 will give a load byte control unless it wishes to terminate the transfer, in which case a load address control should be given. If the response from the IV/70 is a load byte control, the next block of data will be transferred and the cycle will continue until an EOM is encountered or the 360 channel terminates, at which time the end of operation interrupt will be given. This basic method operation may be used to control the transfer of any block of data; screenfuls of data and printer buffers are typical data blocks to be transferred using this method.

During write operations, when the continue or end operation status is given, the status word will contain the byte boundary of the final word of data transferred. If the byte boundary is 0, the last word transferred to the IV/70 will be a full word of data. If the byte boundary is 1 or 2, the last word of the line will not be transferred until after the continue is given and the status is read. The software must then given another IO instruction to receive the partial word. Thus, the software may read the last partial word of a line and mask in the data that lies to the left of a NL symbol in the line.

On a read operation, when the NL symbol is the first or second byte of a word, the word following the word with the NL will be read before the NL is detected; this extra word will not be sent to the 360 channel, but the buffer pointer in the I/O software will point one location beyond the usual expected location, which is the word one beyond the location that contains the NL character. If the NL symbol is the third byte of the word (i.e., a full word is transferred), the buffer pointer will point to a word two locations past the end of the buffer.

BOOTSTRAP MODE

The 7071/7072 Channel Adapter may be used as a bootstrap device if selected at time of manufacture. In bootstrap mode (initiated using SYSTEM RESET) several required functions are performed by the channel adapter: a hard-wired 2848/2260 address is furnished to the channel. This address is selected at time of manufacture and is usually the principal (lowest-numbered) 2260 address on the system. The channel adapter will only accept a write command in this mode, and will reject other commands by giving unit check and intervention required sense to the channel.

Boot mode also forces the load byte command with a starting byte boundary of 0 (so that the word-data of the instructions will be loaded properly) and byte count will be overridden so that any length of program can be loaded. The write will continue until a channel initiated stop sequence

† See "IBM System/360 Component Description: IBM 2260 Display Station, IBM 2848 Display Control," IBM Form A27-2700-4, Pages 35, 36.

‡ See "IBM System/360 Component Description: IBM 2260 Display Station, IBM 2848 Display Control," IBM Form A27-2700-4, Pages 28-33.

is detected, which resets the boot condition, and transfers control to the program at location 1. The program must first issue channel end and device end to complete the operation.

Conventionally the program that is transferred during bootstrap will contain a message that is intended to appear in the first video screen area. A typical message is "BOOTSTRAP UNSUCCESSFUL — PLEASE LOAD AGAIN"; then if successful, the bootstrap program will erase this message from the screen as its first act after giving channel end and device end, so that the message will not appear to the user. The bootstrap program may then proceed to load the operational program in convenient-sized blocks. Note that erase and read commands can be accepted by the channel adapter as soon as the bootstrap mode is terminated.

8001
Card Reader Unit

INTRODUCTION

The Four-Phase 8001 Card Reader reads 300 punched cards per minute with automatic code conversion (when selected by control word bit 22) from Hollerith code to ASCII. The hopper and stack will hold at least 450 cards. The data rate of the card reader is 1050 columns per second. This controller can operate under IOID or not as selected on the card; however, as normally configured, IOID is selected. There are 64 ASCII codes that can be produced; these codes are listed in the table, "Card Reader Code Conversion". See "Special Hollerith Codes" to determine the ASCII codes produced by other hole patterns.

The controller operates in four states as selected by the control word; see the table "Card Reader States".

ASCII Code	ASCII Graphic	Hollerith Code	029 Graphic	026 Graphic Business Science	ASCII Code	ASCII Graphic	Hollerith Code	029 Graphic	026 Graphic Business Science
240	SP		SP	SP	055	-	11	-	-
261	1	1	1	1	312	J	11-1	J	J
262	2	2	2	2	113	K	11-2	K	K
063	3	3	3	3	314	L	11-3	L	L
264	4	4	4	4	115	M	11-4	M	M
065	5	5	5	5	116	N	11-5	N	N
066	6	6	6	6	317	O	11-6	O	O
267	7	7	7	7	120	P	11-7	P	P
270	8	8	8	8	321	Q	11-8	Q	Q
071	9	9	9	9	322	R	11-9	R	R
072	:	8-2	:		041	!	11-2-8	!	
243	#	8-3	#	# or =	044	$	11-3-8	$	$
300	@	8-4	@	@ or '	252	*	11-4-8	*	*
047	'	8-5	'		251	)	11-5-8	)	
275	=	8-6	=		273	;	11-6-8	;	
042	"	8-7	"		335	] †	11-7-8	¬	
060	0	0	0		246	&	12	&	& or +
257	/	0-1	/	/	101	A	12-1	A	A
123	S	0-2	S	S	102	B	12-2	B	B
324	T	0-3	T	T	303	C	12-3	C	C
125	U	0-4	U	U	104	D	12-4	D	D
126	V	0-5	V	V	305	E	12-5	E	E
327	W	0-6	W	W	306	F	12-6	F	F
330	X	0-7	X	X	107	G	12-7	G	G
131	Y	0-8	Y	Y	110	H	12-8	H	H
132	Z	0-9	Z	Z	311	I	12-9	I	I
134	\ †	0-2-8	(0-2-8)		333	[†	12-2-8	¢	
254	,	0-3-8	,		056	.	12-3-8	.	
245	%	0-4-8	%	% or (	074	<	12-4-8	<	¤ or)
137	_	0-5-8	_		050	(	12-5-8	(	
276	>	0-6-8	>		053	+	12-6-8	+	
077	?	0-7-8	?		336	^ †	12-7-8	|	

† ASCII Codes 333, 134, 335, and 336 display as ÷, ×, |, and ↑ on the System IV/70 video display.

A097C

Card Reader Code Conversion

State	Words/Card	Data Rate	Columns/Word	Control Bits 22	23
Packed Binary	40	1.9 mS/word	2	0	0
Unpacked Binary	80	952 μS/word	1	0	1
Packed ASCII	27	2.83 mS/word	3	1	0
Unpacked ASCII	80	952 μS/word	1	1	1

Card Reader States

TIMING

If a word is not taken in time (approximately 1 to 3 mS), the second word will be lost. No data lost indication is given. The card reader should not be operated in the same time frame (simultaneously) with the 7071/7072 Channel Adapter; the 8231 Disc; the 8511, 8512, or 8513 Magnetic Tape Unit; or the 8411, 8435, or 8436 Data Set because of probable timing problems associated with the servicing of these devices. For example, if card-to-disc or card-to-tape transfers are being performed, cards should be read until a buffer is filled, then no further pick given until the output is completed.

STATUS CHECKING

The status bits for the card reader controller are:

Bit	Name	Meaning
23	Not Ready	A command will be ignored; maybe because some alarm condition exists.
22	Busy	Valid data is not available from the controller now.
21	Card in Reader	A card is in the read station.

An interrupt will be generated whenever a word becomes available in the controller output buffer (bit 22 goes false) and whenever a card leaves the read station (bit 21 goes false). These interrupts force different IOID addresses. Before a "pick" (any Control forces a pick; see "Control Signals") is issued, status should be checked and 02_8 found. Status 03 indicates that manual intervention is required at the reader; 06 indicates that a card is in the reader and that valid data is not available. Once the pick command is given, the status word will change to 06 as the leading edge of the card enters the read station, and status will change to 04 when a character or word becomes available. (Note that the controller gives one IOID address for status 04 (character ready) and another for 02 (end of card; pick needed). This facilitates the taking of character data using a single instruction IO.) On the last card in a stack, "not ready" will appear when the card-in reader bit drops. Thus, the status should go from 06 to 03 since the last character or word will normally have been transferred to the computer by the time the card leaves the read station. However, in the packed ASCII mode, status will always go from 04 to 01 since the card will always leave the read station before the data is ready to be transferred.

CONTROL SIGNALS

Any control word causes one card to be picked and read. The control word associated with the card reader is:

Bit	Name	Meaning
23	Unpacked Mode	Either 8 or 12 bits from each column are stored per word as shown below; in the packed mode two or three columns are packed into each word as shown below.
22	Convert	Convert Hollerith code to ASCII. Convert = 0 is also referred to as binary mode.

UNPACKED MODE

Word Bit	Card Row (Convert)		ASCII Bit (Convert)	
23	9		2^0	
22	8		2^1	
21	7		2^2	
20	6		2^3	
19	5		2^4	
18	4	Every	2^5	Every
17	3	Column	2^6	Column
16	2		2^7 (even parity)	
15	1		undefined	
14	0		undefined	
13	11		undefined	
12	12		undefined	
11-0	undefined		undefined	

PACKED MODE

Word Bit	Card Row (Convert)		ASCII Bit (Convert)	
23	9		2^0	
22	8		2^1	
21	7		2^2	
20	6		2^3	Third Column
19	5		2^4	
18	4	Second	2^5	
17	3	Column	2^6	
16	2		2^7 (even parity)	
15	1		2^0	
14	0		2^1	
13	11		2^2	
12	12		2^3	Second Column
11	9		2^4	
10	8		2^5	
9	7		2^6	
8	6		2^7 (even parity)	
7	5		2^0	
6	4	First	2^1	
5	3	Column	2^2	
4	2		2^3	First Column
3	1		2^4	
2	0		2^5	
1	11		2^6	
0	12		2^7 (even parity)	

EXAMPLE

This generalized program will control the card reader and read cards into memory in packed or unpacked, binary or ASCII forms. The state and the starting buffer address are selected in the calling sequence for the program. For state use 0 for packed binary, 1 for unpacked binary, 2 for packed ASCII, and 3 for unpacked ASCII. The program, as presented here, assumes that the card reader in question is located on channel 2, unit address 20_8 and that interrupts are not being used.

```
         ENTRY    CARDIN          SAVES RB-X3
*        BAL      CARDIN          CALLING SEQUENCE
*0       DCN      STATE           CONTROL FOR PICK
*1       DCN      BUFFER ADDRESS
*2                RETURN
STATE    DCN      -40             0-PACKED BINARY
         DCN      -80             1-UNPACKED BINARY
         DCN      -27             2-PACKED ASCII
         DCN      -80             3-UNPACKED ASCII
CARD     EQU      01100           CHANNEL 2, UNIT 20
         FORCE    0
READ     DCN      CARD+1          TYPE = DATA IN
         BSS      1
PICK     DCN      CARD+2          TYPE = CONTROL
SENSE    BSS      1
STATUS   DCN      CARD+3          TYPE = STATUS
         BSS      1
CARD2    BSS      2
CARDM    DCN      7               STATUS MASKS
CARDP    DCN      2
CARDC    DCN      3
TIME     DCN      077770000       TIME OUT AFTER .64 SEC
*                                 PROGRAM FOLLOWS
CARDIN   ST23     CARD2           KEEP REGISTERS
```

```
NREADY   LDA      @SENSE          STATUS LOOP
         STA      STATUS+1
         IO       STATUS
@SENSE   LDA      SENSE           CHECK STATUS
         ANA      CARDM
         CPA      CARDP           NEED STATUS 2 TO PICK
         BZO      READY           GO PICK IF 2
         RCC      RA
         BNZ      NREADY          LOOP ON BAD STATUS
         LDA      1,X2            GET BUFFER ADDRESS
         STA      READ+1
         IO       READ            REMOVE ANY HANGING DATA
         BRA      NREADY          STATUS AGAIN
READY    ST2      PICK+1          PICK LOOP
         IO       PICK            START THE CARD
         LDA      1,X2            GET BUFFER ADDRESS
         STA      READ+1
         LD2*     CARD2
         LD2      STATE,X2        120MS IS AVAILABLE BEFORE FIRST
         LD3      TIME            COLUMN MUST BE READ
COLUMN   BC3      COLMN
         LD2      CARD2
         BRA      NREADY          LOOP ON NOT READY
COLMN    LDA      @SENSE
         STA      STATUS+1
         IO       STATUS          TAKE STATUS AGAIN
         LDA      SENSE
         ANA      CARDC           OK TO READ
         BNZ      COLUMN          WAIT
         IO       READ            READ A WORD
         BC2      COLUMN          IS CARD DONE
         LD23     CARD2           RESTORE REGISTERS
         BRA      2,X2
         END                                        A091A
```

BOOTSTRAP MODE

The card reader can function as a bootstrap unit if the appropriate jumper is installed on the controller at time of manufacture; this is the normal configuration for all Four-Phase Systems supported card reader controllers. The bootstrap mode is forced any time System Reset is pressed, and cleared when a card is read or status is taken. However, the unit will not begin to function as a bootstrap input device until it is selected in the channel and unit address fields of an IO select word. If System Reset is issued for some reason other than bootstrapping from this device, the software must issue a status IO operation before the unit can be used. For this and other reasons it is considered good programming practice to issue a status IO before controlling or giving any other IO operation.

During bootstrap operation, the bootstrap mode is cleared after the first card is read, but a second pick is issued automatically. The second card may be read in or not, at the programmer's option; in the conventional bootstrap program furnished by Four-Phase Systems, the second card contains program information and makes possible the implementation of an 80-word bootstrap loader program. In bootstrap mode, cards are read in unpacked binary.

SPECIAL HOLLERITH CODES

The ASCII character and code produced by nonstandard hole patterns may be determined as follows. First determine the *zone* from the table "Zone Determination". Then determine the *digit* by summing each of the numbers (8, 4, 2, and 1) indicated in the table "Digit Determination" for all

holes punched in the numeric fields. Using the zone and the digit, look up the ASCII character and code in the table "ASCII Characters and Codes Produced by Special Hollerith Codes". For example, with holes in fields 0, 9, and 3, the zone is 2 and the digit is 11 giving a "," and code 254.

Holes Punched In Zone Fields...	None	0	11	12	More Than One Hole
Zone...	3	2	1	0	0

Zone Determination

Holes Punched In Numeric Fields	Digit = Sum Of 8	4	2	1
1				X
2			X	
3			X	X
4		X		
5		X		X
6		X	X	
7		X	X	X
8	X			
9	X			X

Digit Determination

Zone	Digit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	& 246	A 101	B 102	C 303	D 104	E 305	F 306	G 107	H 110	I 311	[333	. 056	< 074	(050	+ 053	^ 336
1	- 055	J 312	K 113	L 314	M 115	N 116	O 317	P 120	Q 321	R 322	! 041	$ 044	* 252	) 251	; 273	] 335
2	0 060	/ 257	S 123	T 324	U 125	V 126	W 327	X 330	Y 131	Z 132	\ 134	, 254	% 245	_ 137	> 276	? 077
3	Space 240	1 261	2 262	3 063	4 264	5 065	6 066	7 267	8 270	9 071	: 072	# 243	@ 300	' 047	= 275	" 042

ASCII Characters and Codes Produced by Special Hollerith Codes

8100
Keyboard/Printer Controller

The 8100 Keyboard/Printer Controller enables the computer to interface with keyboard/printers, such as Teletype KSR 33/35. These controllers are designed to operate with devices that send and receive data serially (bit-by-bit) and operate at relatively low speeds (110 baud to 2400 baud). The data rate is a function of a clock located on the controller card and can be adjusted to match the speed of the device. The data character length (9, 10, or 11 bits including start and stop bits) can also be adjusted at the card, but these adjustments cannot be changed while the card is in operation. The controller can operate with devices that use either a mark or space as the more positive voltage level. The controller operates with a 20 mA current loop or with a standard TTL output. The Teletype keyboard/printers use the 64 character ASCII subset only. See the table "Character Codes Recognized by the Character Printers" in the section "CP Character Printers". The controller can operate under IOID or not as selected on the card; however, as normally configured, IOID is selected.

If the controller is being used with devices that expect nine-bit communication, on output the software must ensure that bit 16 of the character = 0 so that a valid stop bit will be generated. On input, bit 23 will always be 1, and the character should be shifted right logical one for proper alignment.

Data transfers are bidirectional allowing full duplex operation. Transfers may be restricted to half duplex operation by software.

On input, characters are assembled into a serial register, one bit at a time, until a full character is received. Then the character is transferred in parallel to a receive holding register and an interrupt request is sent to the computer. The software then must check the controller status (character received) and then may input the character over the least-significant eight bits of the data bus (bits 16-23 of the data word).

On output, characters are transferred from the computer to the controller over the least-significant eight bits of the data bus, and placed in a transmit holding register. The character is then transferred to a parallel-to-serial shift register where it is sent bit-by-bit along with the appropriate start and stop bits. Each time the holding register is unloaded an interrupt request is sent to the computer. The software then checks status (transmitter ready) to determine whether another character may be sent.

TIMING

On output, if the controller is ready to transmit but not transmitting, a character can be loaded and transferred from the transmit holding register to the serial register. Then a second character may be loaded immediately, although the characters will only be transferred at the data rate of the printer.

Data rates for both input and output vary between the following limits:

Character Length	Data Rate at 2400 Baud	Data Rate at 110 Baud
9	3.75 mS/char	81.9 mS/char
10	4.16 mS/char	91 mS/char
11	4.59 mS/char	100 mS/char

STATUS CHECKING

The status word associated with the controllers is:

Bit	Name	Meaning
23	Character Received	On input, a character is ready to be sent to the processor. An interrupt is generated when this bit goes true. This bit is reset by an IO input.
22	Transmitter Ready	The controller is capable of receiving a new character for output to the peripheral unit. An interrupt is generated when this bit goes true. The bit is cleared by an IO output.
21	Rate Error	At least two characters have been received by the controller from the teletype without an intervening IO input operation; only the last character received is kept. An interrupt is generated by the "character received" condition for each input. This bit is cleared by an IO input.

CONTROL SIGNALS

No control signals are used with this controller. If an IO control is sent, the computer will hang until System Reset is activated.

81CP
Character Printers

The Character Printer Controller enables the computer to interface with printers that operate asynchronously and receive a character at a time. It outputs data serially (bit-by-bit) and operates at relatively low speeds. Supported printers include the 8131 Printer (UNIVAC DCT500). The 8131 Printer prints 132 characters per line in the 64-character ASCII subset: see the table "Character Codes Recognized by the Character Printers". The controller operates in accordance with EIA Specification RS-232-C as required by UNIVAC printers.

Characters are transferred from the computer to the controller over the least-significant eight bits of the data bus, and placed in a transmit holding register. The character is then transferred to a parallel-to-serial shift register where it is sent bit-by-bit along with the appropriate start and stop bits. Each time the holding register is unloaded an interrupt request is sent to the computer. The software then checks status (transmitter ready) to determine whether another character may be sent. The controller can operate under IOID or not as selected on the card; however, as normally configured, IOID is selected.

TIMING

If the controller is ready to transmit but not transmitting, a character can be loaded and transferred from the transmit holding register to the serial register. Then a second character

Third Octal Digit	First & Second Octal Digits															
	00	01	02	03	04	05	06	07	10	11	12	13	14	15	16	17
0	NUL				SP	(	0	8	@	H	P	X	`	h	p	x
1					!	)	1	9	A	I	Q	Y	a	i	q	y
2		LF			"	*	2	:	B	J	R	Z	b	j	r	z
3				ESC	#	+	3	;	C	K	S	[	c	k	s	{
4		FF			$	,	4	<	D	L	T	\	d	l	t	¦
5		CR			%	-	5	=	E	M	U	]	e	m	u	}
6					&	.	6	>	F	N	V	^	f	n	v	~
7	BEL				'	/	7	?	G	O	W	_	g	o	w	

NUL, BEL, LF, and CR are recognized by Teletype Printers (8100 Controller). LF, FF, CR and DEL are recognized by the 8131 Printer. DEL (0377) is used as the null character with this printer.

64-Character ASCII subset, recognized by all character printers. Note that codes 133 ([), 134 (\), 135 (]), and 136 (^) are displayed as ÷, ×, ¦, and ↑ respectively on the 7100/7101 video displays.

31 additional characters that may be recognized by some printers.

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Character Codes Recognized by the Character Printers

may be loaded immediately, although the characters will only be transferred at the data rate of the printer. The 8131 Printer operates at 30 characters per second (300 baud) giving a data rate of 33 milliseconds per character; ten bits are transferred per data character.

STATUS CHECKING

The status word associated with the character printer controller is:

Bit	Name	Meaning
22	Transmitter Ready	The controller is capable of receiving a new character for output to the peripheral unit. An interrupt is generated when this bit goes true. The bit is cleared by an IO output operation.
21	Not Ready	The printer is physically not ready. Operator intervention is required. When this happens, the last character (or the last message if desired) should be sent again. An interrupt is generated when this bit goes false.

CONTROL SIGNALS

No control signals are used with this controller. If an IO control is sent, the computer will hang until System Reset is pressed.

PROGRAMMING NOTES

The illustration "SYSOUT Printer Driver Program" under "81LP Line Printers" contains a driver to print characters on the character printers.

8131 Printer

The 8131 Printer is configured for the 64-character ASCII subset (see the table "Character Codes Recognized by the Character Printers").

An automatic perforation skip is provided with the 8131 Printer. After 60 lines, the paper is fed to the top of the next page leaving three blank lines at the top and bottom of each page.

The sequence of events in a standard line feed operation is CR, LF, followed by some number of DEL characters (ASCII 0377). The DEL characters are required to time the carriage return; the formula for the number of DEL characters required is 11 + N/32 where N is the number of print characters in the line (i.e., the number of characters between the last DEL and the CR). To eject a page from the top of a page requires a FF (014) and 37 DEL characters. Also, to perform a line feed that goes to the top of the next page requires seven extra DEL characters.

81LP
Line Printers

The Line Printer Controller allows the System IV/70 computer to interface with a variety of printers that operate at 200 lines per minute or greater and that contain internal buffering for a full line of characters or a significant fraction of a line. These printers with their operating characteristics, are listed in the table "Characteristics of Line Printers".

The line printer controller operates with the computer in lock-up mode, taking enough characters to fill the printer's internal buffer before disconnecting. A burst may be terminated short of the full buffer length by an ASCII control character or other control character (see "Control Characters"). The printers are normally programmed with a full line buffer, to simplify formatting of print lines. The ASCII control characters are those with values less than 040, but only certain of the characters are considered legal controls for each printer (see "Control Characters"). In general, any short block terminated by an illegal control character will not be printed.

The first control character terminates the transfer immediately: thus LF followed by LF in one transfer is legal but the second line feed will be lost. It is recommended that a form feed be given before a new printing operation (i.e., group of transfers) is started. The printer controller operates under the interrupt system and will generate an interrupt whenever it can accept another block of data. The controller can operate under IOID or not as selected on the card; however, as normally configured, IOID is selected. If the printer is used under the interrupt system, it must be used with the IOID instruction. The conventional address assignment is channel 6, unit 30.

For printers that print 132 characters per line (an even multiple of three), it is necessary to place the line feed character in the leftmost byte of the first word after the end of the line buffer. On printers that accept less than a full line of data per transfer, the software can always detect whether the full line has been accepted yet by examining the IO instruction buffer pointer (location of select word + 1); if this word points to the word following the last word of the output buffer, the line of data has been printed.

CONTROL CHARACTERS

Three form control characters are valid:

Code	Meaning
012	Line Feed (LF) — single line space
014	Form Feed (FF) — top of form
015	Carriage Return (CR) — no line feed

FORM CONTROLS

In addition to the usual Form Controls (012, 014, 015), these printers allow the user to program slewing on a

Model	Lines Per Minute	Characters Per Line	Print Characters Per Burst	Characters Per Font	Time Between Bursts (nominal)	Maximum Transfer Time Per Burst (nominal)	Total Transfer Time/Line
8146	245-1110†	132+1‡	24	64	35 mS	163 μS	929 μS
8147	173-843†	132+1‡	24	96	50 mS	163 μS	929 μS
8151	700-1800‡	132+1‡	132	64	90 mS	613 μS	625 μS
8152	560-1200‡	132+1‡	132	96	107 mS	613 μS	625 μS

†Smaller figure is for full line alphanumeric print; larger figure is first 24 characters only.

‡Smaller figure is for full line alphanumeric print; larger figure is numeric and first 72 characters only.

‡If a full 132 character line is printed, the form feed must be placed in the leftmost character position of the 45th word.

Characteristics of Line Printers

channel or line-count basis. The channels select paper feeds to any line position on a sheet as selected using a special paper tape. The form controls are the codes between 0200 and 0237. Codes between 0200 and 0213 are used to control channel slewing; codes from 0220 to 0237 are used to skip a specified number of lines.

Code	Channel Selected	Usage
0200	0	8 or 12 channel (form feed)
0201	1	8 or 12 channel (line feed)
0202	2	8 or 12 channel
0203	3	8 or 12 channel
0204	4	8 or 12 channel
0205	5	8 or 12 channel
0206	6	8 or 12 channel
0207	7	8 or 12 channel
0210	8	12 channel only
0211	9	12 channel only
0212	10	12 channel only
0213	11	12 channel only

Code	Number of Lines Slewed
0220	0
0221	1
0222	2
0223	3
0224	4
0225	5
0226	6
0227	7
0230	8
0231	9
0232	10
0233	11
0234	12
0235	13
0236	14
0237	15

STATUS CHECKING

The status word associated with the printer controller is:

Bit	Name	Meaning
23	Not Ready	Printer is unable to operate; operator intervention (e.g., turn printer on, load paper, etc.) is required.
22	Busy	Printer buffer is unable to accept data (e.g., a transmission is under way).

CONTROL SIGNAL

The control word associated with the printer controller is:

Bit	Name
23	Character Mode

In the *character mode* the data is assembled as one character per word; a complete line of print-out will thus be represented by as many data words as there are characters in the line, plus one control word. This mode is not widely used. In the *noncharacter (word) mode*, three characters will be assembled into a word and a complete line will contain a number of words equal to one-third the number of characters in the line plus 1, rounded up as required. Thus, 132 character-per-line printers require 45 words for a line buffer. Note that activating SYSTEM RESET forces the word mode. The bit arrangement for word and character mode is:

Word Bit	Character Mode	Word Mode	
23	2^0	2^0	Third Character
22	2^1	2^1	
21	2^2	2^2	
20	2^3	2^3	
19	2^4	2^4	
18	2^5	2^5	
17	2^6	2^6	
16	2^7	2^7	
15	Don't care	2^0	Second Character
14		2^1	
13		2^2	
12		2^3	
11		2^4	
10		2^5	
9		2^6	
8		2^7	
7		2^0	First Character
6		2^1	
5		2^2	
4		2^3	
3		2^4	
2		2^5	
1		2^6	
0		2^7	

If a control signal is given while the printer is operating, the message being printed will be destroyed. Therefore, it is mandatory to check status and receive bit 22=0 before controlling.

CODE SET

The table, "ASCII Code Set for Line Printers" includes all the character codes for the supported line printers. The 8147 and 8152 printers recognize the complete 96 characters; the other printers only recognize the 64-character subset.

PROGRAMMING EXAMPLE

The illustration "SYSOUT Printer Driver Program" lists the SYSOUT, SYSJCT program supplied with the Disc Operating System. This program will list a line of characters on any Four-Phase supported character printer (8131) or line printer (8146, 8147, 8151, and 8152). The printer is selected by the contents of LPOUT: 3 for the 8131, 4 for no printout, and 5 for 8146, 8147, 8151, and 8152. A line feed or a form feed must be implemented in each line by supplying the ASCII controls LF (012) or FF (014) at the end of the line. A calling sequence of "BAL SYSJCT" also results in a form feed. Note that characters will be lost if the character string is longer than the maximum line length of the selected printer.

Third Octal Digit	First & Second Octal Digits															
	00	01	02	03	04	05	06	07	10	11	12	13	14	15	16	17
0					SP	(	0	8	@	H	P	X	`	h	p	x
1					!	)	1	9	A	I	Q	Y	a	i	q	y
2					"	*	2	:	B	J	R	Z	b	j	r	z
3					#	+	3	;	C	K	S	[	c	k	s	{
4					$	,	4	<	D	L	T	\	d	l	t	|
5					%	-	5	=	E	M	U	]	e	m	u	}
6					&	.	6	>	F	N	V	↑	f	n	v	¬
7					'	/	7	?	G	O	W	←	g	o	w	□

Control and form feed characters. See text for details

64-Character ASCII subset, recognized by all line printers

32 additional codes recognized by 8147 and 8152 printers

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ASCII Code Set for Line Printers

```
        ENTRY   SYSOUT                                          000010
        ENTRY   SYSJCT                                          000020
*       PRINTER INDEPENDENT SYSTEM OUTPUT DRIVER,  CALLING SEQUENCE:  000030
*       BAL     SYSOUT                                          000040
*        DCN    BUFFER                                          000050
*               RETURN ON COMPLETION                            000060
*       THE FORMAT OF THE BUFFER IS A STRING OF ASCII GRAPHICS  000070
*       FOLLOWED BY LF OR FF.                                   000080
*                                                               000090
SYSJCT ST2     SJ2                                             000100
        BAL     SYSOUT          GO TO TOP OF FORM USING SYSOUT  000110
         DCN    3022                                            000120
        BRA*    SJ2                                             000130
SJ2     BSS     1                                               000140
SYSOUT ST23     SV              SAVE ALL USED INDEX REGISTERS   000150
        LD3     0,X2            BUFFER ADDRESS                  000160
        RCPY    R0,X3,4                                         000170
        LD2     LR2T            LCR POINTER TO BUFFER           000180
        ST23    3012                                            000190
        ST23    3011                                            000200
3001    LCR     3011            SCAN LINE FOR ENDING CONTROL    000210
        AND     3020                                            000220
        CPA     3021                                            000230
        BMI     3002                                            000240
        BZO     3001                                            000250
        LD23    3011            SAVE LCR POINTER TO LAST NON-BLANK  000260
        BRA     3001                                            000270
3002    STA     3030            SAVE CONTROL CHARACTER          000280
3003    ST23    3011                                            000290
        LCR     3011                                            000300
        STA     3031            SAVE END CHARACTER              000310
        A02     06              CONVERT TO SCR POINTER          000320
        RCPY    R0,X3,4                                         000330
        LDA     LPOUT           GO TO INDIVIDUAL PRINTER'S DRIVER  000340
        AND     07                                              000350
        RADD    RA,RP                                           000360
         BRA    ST10            0=LINE PRINTER                  000370
         BRA    ST20            1=80 COLUMN LINE PRINTER        000380
         BRA    ST30            2=MEMOREX                       000390
         BRA    ST40            3=DCT 500                       000400
         BRA    3099            4=NO PRINT                      000410
         BRA    ST50            5=DP 2410 OR 2440 WITH VFU OPTION  000420
         BRA    3099            6=NOT ASSIGNED                  000430
         BRA    3099            7=NOT ASSIGNED                  000440
3007    LD23    3012                                            000450
3008    ST23    3011            RESTORE LINE TO ORIGINAL        000460
        LDA     3031                                            000470
        SCR     3011                                            000480
3009    LD23    SV              RESTORE REGISTERS               000490
        BRA     1,X2            RETURN                          000500
*       GENERAL LINE PRINTER DRIVER                             000510
ST10    LDA     3030                                            000520
ST11    ST23    3011            INSERT LINE ENDING CONTROL      000530
        SCR     3011            CHARACTER                       000540
        LDA     3010&1                                          000550
        STA     ST14&1                                          000560
ST12    IO      ST13            WAIT FOR STATUS ZERO            000570
        DEC     ST13&1                                          000580
        MCC     ST00                                            000590
        BNZ     ST12                                            000600
        IO      ST14            OUTPUT A BLOCK                  000610
        LDA     ST14&1                                          000620
        RCPY    R0,RA,4                                         000630
        RSUB    RA,X3,0         CHECK FOR CONTROL TAKEN         000640
        BPL     ST12                                            000650
        BRA     3008            DONE                            000660
*       TRUNCATE TO 80 COL, THEN USE GENERAL LINE PRINTER DRIVER  000670
ST20    LDA     3010&1                                          000680
        RSUB    X3,RA                                           000690
        ADD     ST21                                            000700
        BPL     ST10            #BF+(80/3) >= #LF               000710
        RADD    RA,X3                                           000720
        LD2     LR1T                                            000730
        BRA     3003                                            000740
ST21    DCN     80/3                                            000750
*       SWAP CONTROLS, THEN USE GENERAL LINE PRINTER DRIVER     000760
ST50    LDA     3030                                            000770
        CPA     3022                                            000780
        LDA     ST52            LF REPLACEMENT                  000790
        BNZ     ST11                                            000800
        LDA     ST53            FF REPLACEMENT                  000810
        BRA     ST11                                            000820
ST52    OCN     0201*256*256                                    000830
ST53    DCN     FF*256*256                                      000840
*       MEMOREX PRINTER DRIVER                                  000850
ST30    LDA     3033                                            000860
        BRM     ST300           OUTPUT THE GRAPHICS WITHOUT TABS  000870
        BRM     ST31                                            000880
         DCN    CR                                              000890
        RSUB    R1,X3,0                                         000900
        BZO     ST34                                            000910
        SB3     ST33                                            000920
        BPL     ST342                                           000930
ST341   BAL     ST320           DELAY FOR LF                    000940
ST342   BRM     ST31                                            000950
         DCN    LF                                              000960
        LDA     3030                                            000970
        CPA     3022            CHECK FOR FF                    000980
        CPA     3020            CHECK FOR FORM FEED             000990
        BNZ     3007            DONE                            001000
ST36    LD8     ST37            FORM FEED ENDS LINE             001010
ST38    BRM     ST31                                            001020
         DCN    LF              SPACE PAPER 5 INCHES            001030
        LD3     ST35                                            001040
        BAL     ST320                                           001050
        RADD    R1,RB                                           001060
        BMI     ST35                                            001070
        BRA     3007            DONE                            001080
ST34    LD3     ST35            NO GRAPHICS IN LINE             001090
        BRA     ST341                                           001100
ST33    DCN     42                                              001110
ST35    DCN     -3                                              001120
ST37    DCN     -6*5                                            001130
*       DCT 500 PRINTER DRIVER                                  001140
ST40    LDA     3033                                            001150
        BRM     ST300           OUTPUT GRAPHICS                 001160
        BRM     ST31                                            001170
         DCN    CR                                              001180
        LDA     3030                                            001190
        CPA     3022            CHECK FOR FF                    001200
        BZO     ST43                                            001210
        BRM     ST31                                            001220
         DCN    LF                                              001230
        RCPY    X3,RA           COMPUTE TIMING                  001240
        SRL*    ST41                                            001250
        ADD     ST42                                            001260
        MCM2    RA,X3                                           001270
        BAL     ST320                                           001280
        BRA     3007            DONE                            001290
ST43    BRM     ST31            FORM FEED ENDED LINE            001300
         DCN    FF                                              001310
        LD3     ST44                                            001320
        BAL     ST320                                           001330
        BRA     3007            DONE                            001340
ST42    DCN     11              11                              001350
ST41    DCN     5                  + N/2**5 NULLS TO TIME OUT CR, LF  001360
ST44    DCN     -37                                             001370
*       GENERAL CHARACTER PRINTER DRIVER WITHOUT CONTROLS       001380
ST300   BSS     1                                               001390
        ST23    3012                                            001400
        ST23    3011            INSERT LINE ENDING CONTROL CHARACTER  001410
        SCR     3011                                            001420
ST301   LD23    3010            LCR POINTER TO START OF LINE    001430
        ST23    3011                                            001440
        RCPY    R0,X3           INITIALIZE CHARACTER COUNT      001450
ST305   LCR     3011            GET A BYTE                      001460
        AND     3020                                            001470
        CPA     3021                                            001480
        BMI*    ST300           END IF CONTROL                  001490
        SLR     8                                               001500
        STA     ST306                                           001510
        BRM     ST31            OUTPUT THE GRAPHIC              001520
ST306    BSS    1                                               001530
        BRA     ST305                                           001540
ST32    BRM     ST31            ERROR REPORTED--RETRY LINE      001550
         DCN    CR                                              001560
        LD3     ST44                                            001570
        BAL     ST320           DELAY                           001580
        BRA     ST301           RETRY                           001590
ST320   BRM     ST31            OUTPUT (X3) EO'S TO             001600
         DCN    0377              TIME OUT THE PRINTER          001610
        BMI     ST320                                           001620
        RCPY    X2,RP           DONE                            001630
*       OUTPUT A BYTE TO A CHARACTER PRINTER                    001640
        FORCE   0                                               001650
ST312   DCN     03147                                           001660
        DCN     ST20                                            001670
ST311   DCN     03144                                           001680
ST31    BSS     1                                               001690
ST313   IO      ST312           STATUS THE PRINTER              001700
        DEC     ST312&1                                         001710
        RCL     R1,RA,7,2       BIT 21                          001720
        AND     ST00                                            001730
ST314   BNZ     ST32            ERROR--RESTART LINE             001740
        RCL     R1,RA,7,1       BIT 22                          001750
        AND     ST00                                            001760
        BZO     ST313           TRANSMITTER NOT READY           001770
        IO      ST311                                           001780
        RADD    R1,X3           COUNT CHARACTERS                001790
        BRA*    ST31            SAVE CC OF X3 INCREMENT         001800
*                                                               001810
06      DCN     06                                              001820
07      DCN     07                                              001830
3020    DCN     0177*256*256                                    001840
3021    DCN     040*256*256     ASCII BLANK                     001850
3022    DCN     FF*256*256      ASCII FORM FEED                 001860
3030    BSS     1                                               001870
3031    BSS     1                                               001880
ST00    BSS     1                                               001890
        FORCE   0                                               001900
ST13    DCN     03143                                           001910
        DCN     ST00                                            001920
ST14    DCN     03140                                           001930
        BSS     1                                               001940
3010    BSS     2                                               001950
3011    BSS     2                                               001960
3012    BSS     2                                               001970
SV      BSS     2                                               001980
LF      EQU     012                                             001990
FF      EQU     014                                             002000
CR      EQU     015                                             002010
        END                                                     002020
```

C211A

Note that this program includes printers that are not currently supported.

SYSOUT Printer Driver Program

8231
Cartridge Disc Unit

INTRODUCTION

The 8231 Cartridge Disc Unit has a 2.5M byte capacity, a 184K bytes per second transfer rate, a 70 millisecond maximum average track seek time, a 135 millisecond maximum track seek time, and a 20 millisecond average latency time. There are 203 cylinders, each divided into two tracks (one top, one bottom). Each track is divided into eight sectors, each containing 768 data bytes or 256 24-bit data words (see the table, "Disc Memory Structure"). A cyclic redundancy check word is added to each sector during an output operation and checked on input; this check is completely performed by the hardware; however, a cyclic redundancy error status bit is set accordingly.

It is possible to write or read up to 16 contiguous sectors in one operation by starting with sector address 0; thus 4K words may be transferred using a single instruction. Every sector on the disc is separately addressable. Since up to four disc drives may be attached to one controller, more than one seek can take place at a time, but only one transfer.

Disc	Cylinders	Tracks	Sectors	Data Words	Bytes
1	203	406	3248	831,488	2,494,464
	1	2	16	4,096	12,288
		1	8	2,048	6,144
			1	256	768
				1	3

Disc Memory Structure

The disc memory operates with the computer in the lock-up mode, inputting or outputting data in sector-sized blocks. The controller will always transfer a multiple of full sectors at a time. A transfer locks up the system for about five milliseconds per sector; this may preclude using the disc in the same time frame with card reader, magnetic tape, or data set transfers.

The controller is wired for IOID. The first disc on a multidisc system is conventionally assigned to unit address 24, channel 2, as shown in the table, "Four-Phase Standard I/O Priority Assignments" in Section 3. However, even in nonstandard configurations, the lowest numbered disc on a controller circuit must be assigned to a unit address number divisible by 4. The only IOID address generated will be the first device address (nominally 024); the software must keep track of which disc is currently communicating, in a multidisc environment.

To transfer data to or from the disc, the program issues a control word (see "Control Signals") to the disc controller specifying a seek and the number of the cylinder required. When the specified cylinder is found, the controller issues an interrupt indicating that the seek is completed (exception: a seek to the current cylinder will not generate an interrupt). After checking status, the program issues a second control word specifying the direction of transfer (write or read), the address of the starting sector for the transfer, and the number of sectors to be transferred. Approximately 1 millisecond before the start of the first sector, the controller will generate an interrupt and the transfer may begin; the program has 1 millisecond to begin transferring data. The program must issue the appropriate IO instruction to cause the machine to lock-up in the IO loop until the transfer is complete.

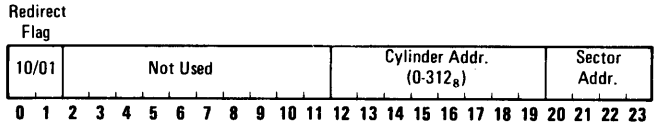
Note that it is necessary for the program to ask for status on the disc before each control and after transferring data. For example if the program waits too long after the 1 millisecond interrupt before starting the data transfer, the too late bit will be set; the second control operation must be repeated; and the system must wait for the disc to rotate to the desired sector again before transferring data. See the illustration "Recommended Sequence of Events for Disc Transfers" for details.

SECTOR FORMAT

Every sector has a header formatted as described in the following paragraph. This is followed by a preamble used for synchronizing the disc; the preamble is not transferred to the program except for a brute-force control signal. Next follows 256 words of data. Next follows a cyclic redundancy check word.

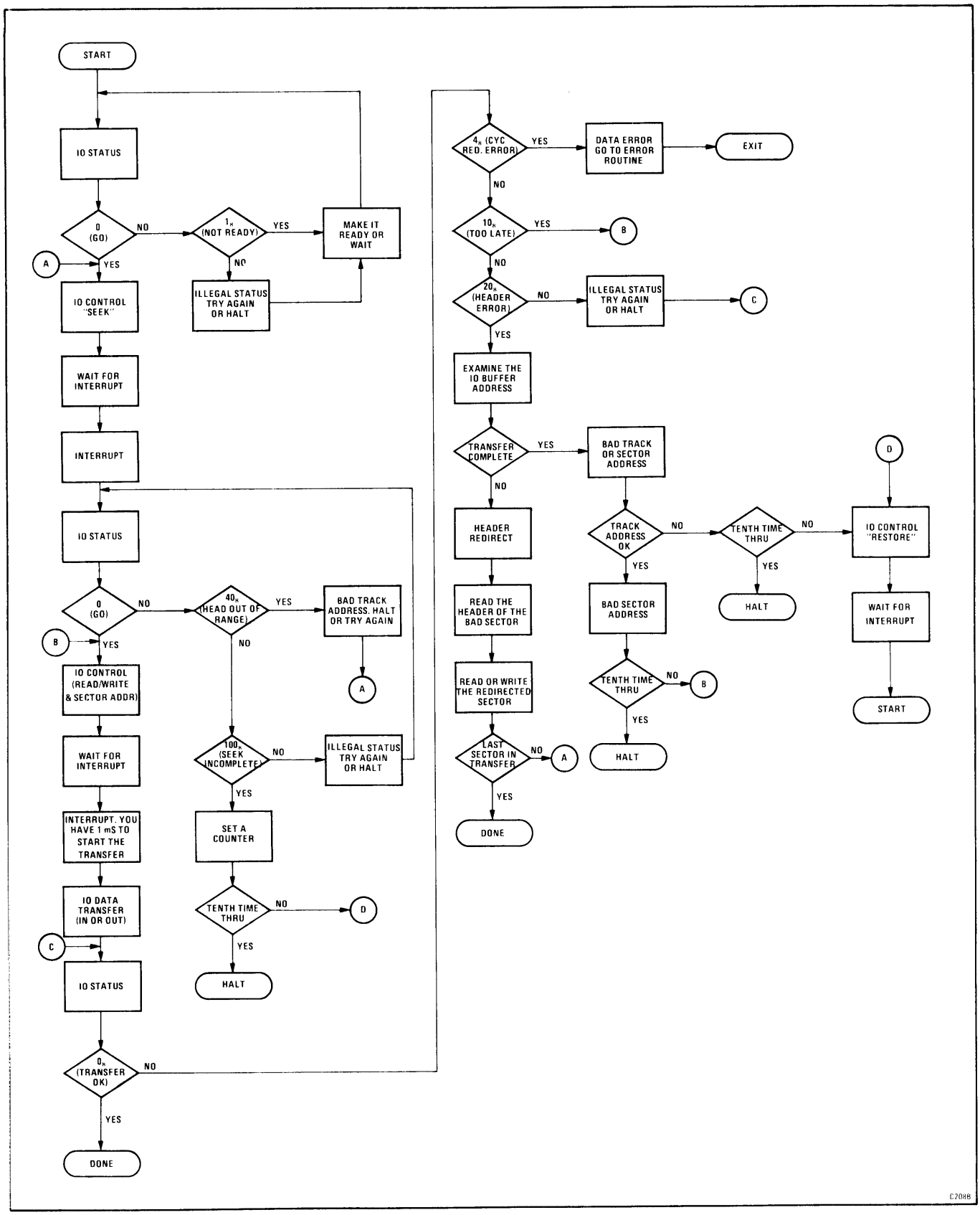
HEADER FORMAT

The header word contains a redirect flag and sector identification as shown below. See "Redirect Logic" for details on the use of the header word.



STATUS CHECKING

Bit	Name	Meaning
23	Not Ready	The disc won't seek, read, or write.



Recommended Sequence of Events for Disc Transfers

Bit	Name	Meaning
		Caused by power off, no cartridge, not up to speed, bad disc, or seek in progress. An interrupt is generated when this bit goes false; e.g., seek complete.
22	Busy	A read or write operation has started but is not complete.
21	Cyclic Redundancy Error	Computed on the 256 data words of a sector only. Reset by a status IO.
20	Too Late	It is too late to read or write starting at the last addressed sector. Issue the control again and wait for the interrupt. Reset by a status IO. When operating under interrupts, it is recommended that a restore be given after this error is encountered.
19	Header Error	Redirect flag encountered or sector addressing error. Reset by a status IO. When operating under interrupts, it is recommended that a restore be given after this error is encountered.
18	Head Out of Range	Program error. The program tried to address a track above 202_{10} = 312_8. Sets bit 23 to zero and generates an interrupt. Reset by a restore control signal.
17	Seek Incomplete	Hardware error. The positioning mechanism is out of alignment. Sets bit 23 to zero and generates an interrupt. Reset by a restore control signal.
16-0		Not used.

CONTROL SIGNALS

Bit	Name	Meaning
23-20	- - -	Sector address.
19-12	- - -	Cylinder address (0-312_8). Cylinders 310-312 are reserved for redirect addresses.
11-8	- - -	Number of sectors - 1. The sector count cannot force a seek to another cylinder.
7-5	- - -	Not used.
4	Header Only	One word only. Read: read the header only. Write: write a header.
3	Restore	Moves disc heads to home position and clears status bits 17 and 18. Takes precedence over all other controls.
2	Brute Force	For control bit 0 = 1, write a header and preamble for the addressed sector and write garbage to the rest of the sector. For bit 0 = 0, read all the data to the end of the sector. Intended for diagnostic uses only.
1	Seek	Go to the addressed track. This takes priority over all controls but restore. A seek to the current track gives an immediate interrupt.
0	Read/Write	0 = read, 1 = write.

PROGRAMMING DISC TRANSFERS

It is intended that all disc I/O operations take place under control of the $DISC or $IDISC system programs provided to perform all seeks, reads, and writes for up to eight disc units. $IDISC uses the interrupt system of the System IV/70; $DISC does not.

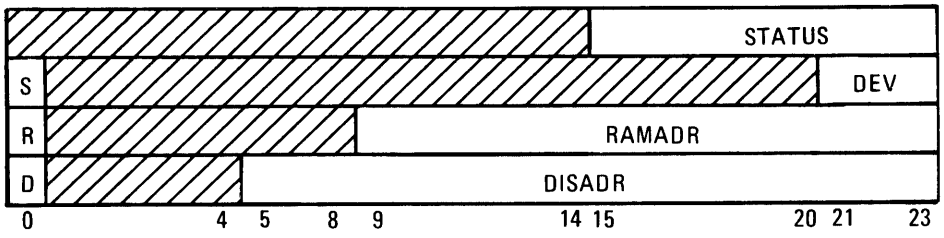
All I/O activity is coordinated with a four-word ($DISC) or five-word ($IDISC) Device Status Table (DST) for each disc. The program takes status, controls, and reads or writes for each disc as needed. Error recovery attempts are provided automatically. All requests for I/O operations are made using the DST, which may not be altered by the user until the I/O operation is complete or rejected. All 8231 I/O operations should be done using one of these programs so that the DSTs contain valid information.

The noninterrupt program is not reentrant and if any attempt is made to enter it while it is in use, the request will be rejected. However, $DISC may be called from an interrupt level if a software lock is provided or if the appropriate interrupt level is disarmed when $DISC is used at a lower level or in the background. The interrupt version ($IDISC) may be used reentrantly if separate DSTs are used for each request; if $IDISC is busy and cannot handle a new call immediately, the call will be queued. Using $IDISC means that $IOPEN and $ICLOS must be used also; see "Disc Operating System (DOS) Reference Manual" document SIV/70—50—1C or later.

Permanent error conditions must be processed by the user using the information contained in the status word. No provision is made for generating error messages suitable for the video display or printer. This program makes no provision for handling symbolic disc addresses; this is assumed to be a higher level function of the Disc Operating System (DOS). The program saves all registers.

To request disc I/O operations using $DISC, first set up the DST beginning at a conveniently labeled location, such as REQTAB (see illustration — "Disc Device Status Table (DST) Format for $DISC"), and then call $DISC as follows:

```
      BAL    $DISC
+0    PZE    REQTAB
+1    BRx    reject      reject or permanent error return
                         normal return
```



Word	Bits	Symbol	Meaning
REQTAB	23-0	STATUS†	Bit 23 = Not Ready Bit 22 = Busy Bit 21 = Cyclic Redundancy Error Bit 20 = Too Late Bit 19 = Header Error Bit 18 = Head Out of Range Bit 17 = Seek Incomplete Bit 16 = Illegal Request Bit 15 = Incorrect Length Bits 0-14 = Not Used
REQTAB+1	23-21	DEV‡	Index to drive 0 ⩽ device ⩽ 7
	20-1	—	Not used
	0	S‡	1 Do seek only 0 Do data transfer (with seek if necessary)
REQTAB+2	23-9	RAMADR‡	Location in memory of data buffer
	8-1	—	Not used
	0	R‡	1 Normal return only when status = 0 0 Normal return after operation initiated or stacked
REQTAB+3	23-5	DISADR‡	Disc address request word SECTOR COUNT - 1 (5–11) | CYLINDER (12–19) | SECTOR (20–23)
	4-1	—	Not used
	0	D‡	1 write data on disc 0 read data from disc

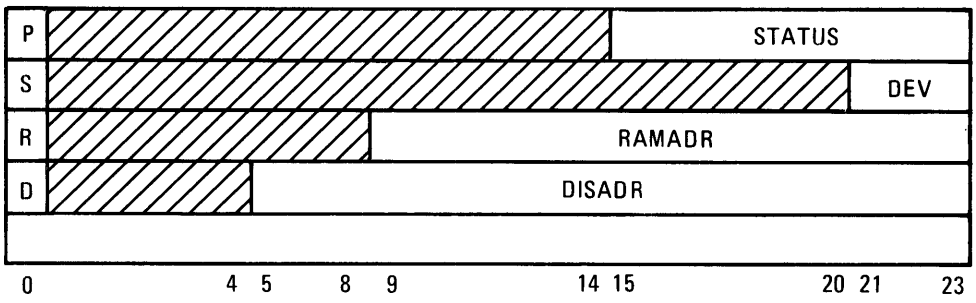
†Furnished by $DISC

‡Furnished by user program

The reject return is taken if any of the input values are out of range. Note that cylinders 200 through 202 are illegal.

A098E

Disc Device Status Table (DST) Format for $DISC



Word	Bits	Symbol	Meaning
REQTAB	23-0	STATUS†	Bit 23 = Not Ready Bit 22 = Busy Bit 21 = Cyclic Redundancy Error Bit 20 = Too Late Bit 19 = Header Error Bit 18 = Head Out of Range Bit 17 = Seek Incomplete Bit 16 = Illegal Request Bit 15 = Incorrect Length Bits 1-14 = Not Used
		P†	Bit 0 = Status posted, operation complete
REQTAB+1	23-21	DEV‡	Index to drive 0 ⩽ device ⩽ 7
	20-1	—	Not used
	0	S‡	1 Do seek only 0 Do data transfer (with seek if necessary)
REQTAB+2	23-9	RAMADR‡	Location in memory of data buffer
	8-1	—	Not used
	0	R‡	1 Normal return only when status = 0 0 Normal return after operation initiated or stacked
REQTAB+3	23-5	DISADR‡	Disc address request word SECTOR COUNT – 1 | CYLINDER | SECTOR 5 11 12 19 20 23
	4-1	—	Not used
	0	D‡	1 write data on disc 0 read data from disc
REQTAB+4	23-0	—	BSS 1 — used by queuing software

†Furnished by $IDISC

‡Furnished by user program

The reject return is taken (status bits 0, 16 = 1) if any of the input values are out of range, Note that cylinders 200 through 202 are illegal.

A363A

Disc Device Status Table (DST) Format for $IDISC

Normally the user should check the status word in the request table to determine the outcome of the I/O request. If the return flag (R) is set to 1 when the call to $DISC is made, then the normal return is made only when the operation has completed successfully without error. The reject return is taken if the request is invalid (e.g., device is not ready, DEV is too large, illegal disc address, reentrant call) of if a permanent error develops (e.g., solid cyclic data error, other status error which is illegal).

To use $IDISC, use the following:

```
      BAL    $IDISC
+0      PZE    REQTAB
```

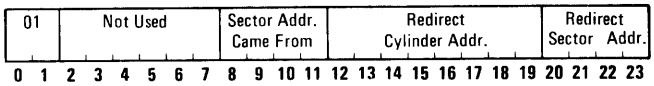
When the $IDISC program returns control to the user, the status word should be checked. If bit 0 = 1, the operation is complete and correct; otherwise a rejection has occurred. This is similar to the reject return from $DISC.

REDIRECT LOGIC

Each new disc is formatted using a program that runs diagnostic checks on the 3248 sectors of the disc. If a sector fails the diagnostic tests, the format program writes a redirect message into the header word for that sector.

A redirect flag is contained in the first two bits of the header word: if the sector is considered good, the first two bits will be 10; if the diagnostic program discovers a bad bit in the sector, it will change the redirect flag to 01. (Bit patterns 11 and 00 are currently not used.) If the sector is good (flag = 10), the sector identification information (in bits 12 through 23 of the word) will be the address of the cylinder and sector being identified; but if the sector is found bad (flag = 01), the diagnostic program will change the identification to the address of a sector on a cylinder between 200 and 202 (310_8 and 312_8), which is the redirect area.

When the disc file is performing a transfer and the controller encounters a redirect flag different from 10, the controller will terminate the transfer immediately and set the header-error status bit. After taking status and discovering this error, the $DISC program examines its data buffer to determine how many sectors were transferred and reads the header of the bad sector. The next data transfer will then involve the cylinder and sector addressed in the identification field of the header word. The format of the header word in a redirect location is as follows:



BOOTSTRAP MODE

The disc can function as a bootstrap unit if the appropriate jumper is installed on the controller at time of manufacture; this is the normal configuration for all Four-Phase Systems supported disc controllers. The bootstrap mode is forced any time System Reset is pressed, and cleared when a sector is read or status is taken. However, the unit will not begin to function as a bootstrap input device until it is selected in the channel and unit address fields of an IO select word. If System Reset is issued for some reason other than bootstrapping from the disc, the software must issue a status IO operation before the unit can be used. For this other reasons it is considered good programming practice to issue a status IO before controlling or giving any other IO operation.

If more than one disc is installed on a controller, only disc 0, cylinder 0, sector 0 can be used for bootstrapping.

8411
Asynchronous Data Set Controller

The 8411 Asynchronous Data Set Controller enables the computer to interface asynchronously with data sets designed in accordance with EIA Specification RS-232-C. This controller operates with devices that send and receive data serially (bit-by-bit) at relatively low speeds (110 baud to 2400 baud). The data rate is a function of a clock located on the controller card and can be adjusted to match the speed of the device†. The data character length (9, 10, or 11 including start and stop bits) can also be adjusted at the card but these adjustments cannot be changed while the card is in operation. The controller can operate under IOID or not as selected on the card; however, as normally configured, IOID is selected.

Data transfers are bidirectional allowing full duplex operation. Transfers may be restricted to half duplex operation with a change in wiring.

On input, characters are assembled into a serial register, one bit at a time, until a full character is received. Then the character is transferred in parallel to a receive holding register and an interrupt request is sent to the computer. The software then must check the controller status (character received) and then may input the character over the least-significant eight bits of the data bus (bits 16-23 of the data word). If the program operates with parity checking enabled, bit 16 will contain even parity on the byte; if parity is disabled, the parity bit is just another data bit. In either case, the bit is passed through to the user program.

On output, characters are transferred from the computer to the controller over the least-significant eight bits of the data bus, and placed in a transmit holding register. The character is then transferred to a parallel-to-serial shift register where it is sent bit-by-bit along with the appropriate start and stop bits. If parity is enabled, even parity is calculated on the least significant 7 bits of the character and placed in bit 16; if parity is disabled, bit 16 is passed through like any other bit. Each time the holding register is unloaded, an interrupt request is sent to the computer. The program then must check status (transmitter ready) to determine whether another character may be sent.

The controller will generate and check even parity on each byte transferred; this function can be enabled or disabled by the software.

If 9-bit communications are being used, on output the software must ensure that bit 16 = 0, so that a valid stop bit will be generated. On input, bit 23 will always be 1 (the start bit), and the character should be shifted right logical 1 to get rid of this bit and align the character properly.

†In special applications, the speed of the controller may be locked to the Data Set clock. In this case the controller can operate at any Data Set speed. This option requires a wiring change, however.

Programming for this controller involves a thorough knowledge of the data set or other interactive device and of the communications discipline for the system in question. This section merely covers programming from the IV/70 point of view.

TIMING

If the controller is ready to transmit but not transmitting and "clear to send" is on, a character can be loaded and transferred from the transmit holding register to the serial register. Then a second character may be loaded immediately, although the characters will only be transferred at the data rate of the Data Set. Data rates for both input and output vary between the following limits:

Character Length	Data Rate at 2400 Baud	Data Rate at 110 Baud
9	3.75 mS/char	81.9 mS/char
10	4.16 mS/char	91 mS/char
11	4.59 mS/char	100 mS/char

STATUS CHECKING

The status word associated with the Asynchronous Data Set Controller is:

Bit	Name	Meaning
23	Character Received	A serial character has been received from the data set and transferred to the receive holding register. An interrupt is generated whenever this bit goes true. This bit is cleared by an IO input. This bit must be true before a data in IO is issued, or the computer will hang.
22	Transmitter Ready	The controller is capable of receiving a new character for output to the data set. An interrupt is generated when this bit goes true. Note that bits 22 and 23 can turn on with the same interrupt. This bit is cleared by an IO output. This bit must be true before a data out IO is issued or the computer will hang until the transmit buffer is empty.
21	Rate Error	At least two successive receive transfers have occurred with no intervening IO input instruction; only the last character received is kept. An interrupt is generated by the

Bit	Name	Meaning
		"character received" condition for each character. This bit is cleared by an IO input instruction.
20	Parity Error	In receive mode, even parity has been checked and an error found. An interrupt is generated, but only for the "character received" condition. This bit is cleared by an IO status operation.
19	Carrier Detect	The data set is conditioned to receive and data may now be accepted by the controller. An interrupt is generated when this bit changes. This bit goes false when the carrier is lost.
18	Clear to Send	Send carrier is on ready and the controller may send data. An interrupt is generated when this bit goes true. This bit should be checked before the first character is sent.
17	Data Set Ready	The data set is connected, powered up, and not in the test mode. An interrupt is generated whenever this bit changes.
16	Ring Indicator	The unit at the other end of the line is trying to make contact. An interrupt is generated whenever this bit goes true. This unit should respond by sending the "turn on data set" control bit (see "Control Signals" below). The unit at the other end of the line may then send its message.
15-13		Not used.
12	Long Blank	The data set has received a "long blank" (continuous space) signal from the unit on the other end. An interrupt is generated when this bit goes true. The bit is reset when status is taken.

CONTROL SIGNALS

The control word associated with the Asynchronous Data Set Controller is:

Bit	Name	Meaning
23	Request to Send	Turns the send carrier on if one, off if zero. In some single poll environments, this control may be eliminated and the send carrier left on all the time. If this bit is used, it enables the data set to send data. Once "request to send" has been issued, the user must wait for a "clear to send" status before sending any data. Clear to send goes true between 0 and 200 milliseconds after request to send is issued. After receiving clear to send, the user must check "transmitter ready" before sending. When transmitting, the software must receive "transmitter ready" status before turning the send carrier off, or the last character will be lost.
22	Turn on Data Set	Enables data set operation and turns on "data set ready". If private lines are being employed, this bit will normally be left on. If the auto dial/answer function is used, this bit causes the off-hook condition. Thus, if a "ring indicator" is received, this bit will cause off-hook and answer the incoming call. If this station is initiating, this bit must be on to enable dialing. If this bit is turned off, the on-hook condition will occur and the line will be disconnected. This bit is reset by system reset.
21	Suppress Parity	Causes the data set to suppress the generation and checking of parity. The 8 data bits will be transmitted (either direction) exactly as received.
20-13		Not used.
12	Force Long Blank	Sends a long blank (continuous space) to the device at the other end of the line.

8435
Synchronous Data Set Controller

The 8435 Synchronous Data Set Controller enables the computer to interface with any synchronous data set designed in accordance with EIA Specification RS-232-C, such as a Western Electric 201A or B. Synchronous communications regularly use a sync word (e.g., ASCII 026_8) for synchronizing purposes. The controller can use any sync word, as selected at time of manufacture.

These devices transfer data serially (bit-by-bit) and operate at speeds defined by the data set; the controller operates at this speed and can function at higher speeds than any RS-compatible data set. Data transfers are bidirectional, allowing full duplex operation.

A data character length of 7 or 8 bits can be selected. This option is selected by a wiring change on the controller card, when it is not in operation.

On input, characters are assembled into a serial-to-parallel register, one bit at a time, until a full character is received. Then the character is transferred in parallel to a receive holding register and an interrupt request is sent to the computer. The computer must then issue a data in IO instruction to receive the character plus a 7-bit status word from the controller. The character is in the eight least-significant bits (16-23) of the bus, and the status message is in bits 9-15. If the characters are to be packed three to a word, it must be performed by the software.

If the device at the other end of the line is trying to initiate a contact or a response, it will do so by sending sync words. The controller must receive two consecutive sync words from the line before it will respond by notifying the computer.

On output, characters are transferred to the controller one at a time, over the least-significant eight bits of the data bus. The character is placed in a transmit holding register, then copied into a parallel-to-serial shift register from which it is sent, bit-by-bit, to the data set. The output rate of the shift register is controlled by a clock from the data set. Each time the holding register is unloaded an interrupt request is sent to the computer. The computer then issues a data in IO instruction to get the status information and determine if another character may be sent. If the transmitter is idle, a character can be loaded into the transmit holding register. A second character may be loaded as soon as a "clear to send" status is received, although the characters will only be transferred at the clock rate of the data set.

Whenever the transmitter is turned on, the contents of the holding register will be copied into the shift register and sent to the data set one bit at a time with every clock pulse of the data set. An interrupt is issued when the character is transferred from the holding register, asking for another character; but if the computer does not respond with another character, a word of all ones will be sent.

An interrupt is also generated any time the data set becomes ready or not ready and any time that the receiving carrier status goes true or false (changes state). See "Status Checking" for details. The controller can operate under IOID or not as selected on the card; however, as normally configured, IOID is selected.

Programming for this controller involves a thorough knowledge of the data set or other interactive device and of the communications discipline for the system in question. This section merely covers programming from the IV/70 point of view.

STATUS CHECKING

The status bits associated with the Synchronous Data Set Controller are attached to the data byte (if any) on input; the data byte is in bits 16-23. Sending a status in IO instruction to this controller is illegal.

Bit	Name	Meaning
15	Byte Ready	If true, this is a good data byte that has not been received before. If false, either no data input transfer is taking place, or the byte being presented has been received by the computer already. An interrupt is generated when this bit goes true. This bit is reset by a data in IO instruction or a reset-receiver control.
14	Receiving Carrier	The data set is receiving a carrier from the remote data set. An interrupt is generated when this bit changes.
13	Data Lost	At least one character of data has been lost. The holding register will not accept a new character until the old one has been taken by the computer; therefore bit 13 true means this is the last valid data byte. This bit is reset by a data in IO instruction or a reset-receiver control.
12	Sync Word Received	The local controller is synchronized with the remote controller. This condition goes true after two successive sync words have been received and stays true until a reset-receiver control is given or until system reset.

Bit	Name	Meaning
11	Clear to Send	The data set has received a request-to-send control from the computer, is transmitting a carrier, and is ready to send data.
10	Data Set Ready	An interrupt will be generated whenever the data set becomes ready or not ready. Bit 10 true means that the data set is on and functional.
9	Output Needed	Valid only for the transmit mode. An interrupt will be generated and this bit set true whenever a character has been transferred from the holding register to the shift register. The controller can now accept another character of data. If bit 9 is on for the time required to transmit one character without a new character being given (or a control to reset the transmitter), the character in the holding register will be sent again.

Changes in bits 10 or 14, or bits 9 or 15 going true will generate an interrupt. The programmer is advised to give a data in IO instruction and check status every time an interrupt occurs. Note that in two-way full duplex communications, when the transmitter is idling by sending only sync characters, an interrupt on bit 9 will be generated for each sync character sent. If an interrupt occurs on bit 9 and transmission is complete, the program should give a reset transmitter control (see "Control Signals") within the time required to transmit one character. If an interrupt occurs on bit 15, the data word accompanying status is good data.

CONTROL SIGNALS

The control word associated with the Synchronous Data Set Controller is:

Bit	Name	Meaning
23	Reset Receiver	Must be given by the computer to clear the receiver sometime before receiving each message. Resets status bits 12, 13, and 15.
22	Request to Send	Turns on the request-to-send line to the data set thereby requesting the data set to transmit a carrier. When the carrier is turned on, the data set responds with a clear-to-send status. The request-to-send line is turned off by a reset-transmitter control; a zero request-to-send bit does nothing.
21	Reset Transmitter	Must be given by the computer at the termination of an output operation and at the beginning of operations to initialize the system. Sets status bit 9, disables interrupts on bit 9, and turns off the request-to-send line as described above.

Before initiating communication with the device on the other end of the line the program should issue a control 5_8 to reset both the transmitter and the receiver.

After a request-to-send control is given, the data set will delay a period of time defined by the data set before setting clear to send. This is to allow transients on the phone lines to clear. Typical turn around delay between a request-to-send control and clear-to-send status is 200 milliseconds for half duplex data sets and 8 milliseconds for full duplex data sets. There is no turn around delay associated with these signals going off.

8436
Buffered Synchronous Data Set Controller

The 8436 Buffered Synchronous Data Set Controller enables the computer to interface with any synchronous data set designed in accordance with EIA Specification RS-232-C, such as a Western Electric 201A or B. Synchronous communications regularly use a sync word (e.g., ASCII 026_8) for synchronizing purposes. The controller can use any sync word, as selected at time of manufacture.

These devices transfer data serially (bit-by-bit) and operate at speeds defined by the data set; the controller operates at this speed and can function at higher speeds than any RS-compatible data set. Data transfers are bidirectional, allowing full duplex operation.

A data character length of 7 or 8 bits can be selected. This option is selected by a wiring change on the controller card when it is not in operation. The standard channel and unit assignment is channel 1 unit 033.

On input, characters are assembled into a serial-to-parallel register, one bit at a time, until a full character is received. Then the character is transferred to one of two sixteen-byte input buffers. This proceeds until a buffer is full, at which time an interrupt is generated with a "data ready" status. The computer must then issue a data in IO instruction that will cause the sixteen bytes to be read into the sixteen word block of memory specified in the buffer address word associated with the IO instruction. The bytes are read into bits 16-23, all other bits being zero. When a buffer is full, data from the communications line is entered into the other buffer. All switching of buffers is done by the controller.

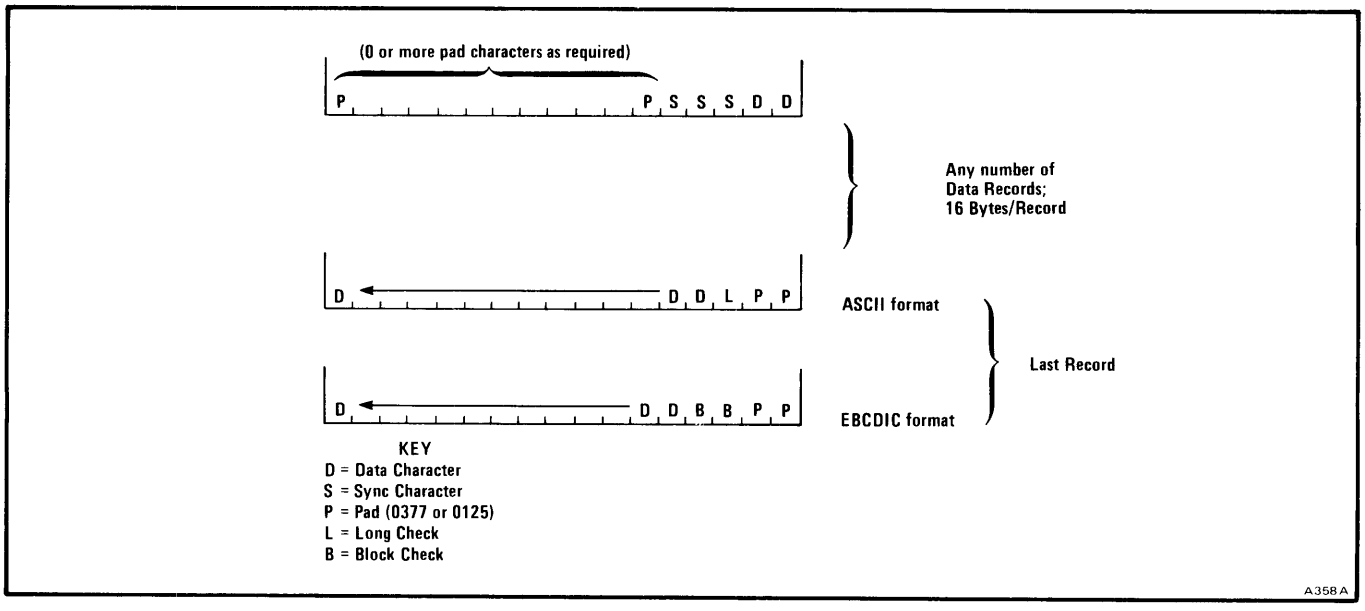
On output, characters are transferred to the controller, sixteen at a time, from the sixteen word block specified by the buffer address word associated with the IO instruction. The characters are loaded into one of a pair of 16 byte output buffers. Characters are then transferred one at a time into a shift register from which they are sent, bit-by-bit to the data set under control of the transmit clock. Whenever a buffer becomes available to be filled an interrupt will be generated and the output needed status bit will be set. All switching of buffers is done by the controller.

An interrupt is also generated any time the data set becomes ready or not ready and any time that the receiving carrier status goes true or false (changes state). See "Status Checking" for details. The controller can operate under IOID or not as selected on the card; however, as normally configured, IOID is selected.

Programming for this controller involves a thorough knowledge of the data set or other interactive device and of the communications discipline for the system in question. This section merely covers programming from the IV/70 point of view.

STATUS CHECKING

The status bits associated with the 8436 Buffered Synchronous Data Set Controller are fetched using an IO



Data Record Format

status instruction; this contrasts with the 8435 Unbuffered Synchronous Controller, where status is presented in each word of input data.

Bit	Name	Meaning
15	Input Ready	If true, a block of data is available for input. An interrupt is generated when this bit goes true. This bit is reset by a data in IO instruction or a reset-receiver control.
14	Receiving Carrier	The data set is receiving a carrier from the remote data set. An interrupt is generated when this bit changes.
13	Received Data Lost	At least one block of data has been lost on input. This bit is reset by a data in IO instruction or a reset-receiver control.
12	Sync Word Received	The local controller is synchronized with the remote controller. This condition goes true after two successive sync words have been received and stays true until a reset-receiver control is given or until system reset.
11	Clear to Send	The data set has received a request-to-send control from the computer, is transmitting a carrier, and is ready to send data. An interrupt is generated when this bit changes.
10	Data Set Ready	An interrupt will be generated whenever the data set becomes ready or not ready. Bit 10 true means that the data set is on and functional.
9	Output Needed	Valid only for the transmit mode. An interrupt will be generated and this bit set true whenever an output buffer is able to be filled.
8	Transmitted Data Lost	At least one byte of data has been lost on output. Reset by a reset transmit or data out operation.

Changes in bits 10, 11, or 14, or bits 9 or 15 going true will generate an interrupt. Also, when a ring indicator signal is received an interrupt is generated. The programmer is advised to give a status IO instruction and check status every time an interrupt occurs. Note that in two-way full duplex communications, when the transmitter is idling by sending only sync characters, an interrupt on bit 9 will be generated for each block of sync characters sent. Bit 10 going true will, in an auto answer installation, be taken to mean that a ring has been answered.

CONTROL SIGNALS

The control word associated with the Buffered Synchronous Data Set Controller is:

Bit	Name	Meaning
23	Reset Receiver	Must be given by the computer to clear the receiver sometime before receiving each message. Resets status bits 12, 13, and 15.
22	Request to Send	Turns on the request-to-send line to the data set thereby requesting the data set to transmit a carrier. When the carrier is turned on, the data set responds with a clear-to-send status. The request-to-send line is turned off by a reset-transmitter control; a zero request-to send bit does nothing.
21	Reset Transmitter	Must be given by the computer at the termination of an output operation and at the beginning of operations to initialize the system. Sets status bit 9, disables interrupts on bit 9, and turns off the request-to-send line as described above.
20	Reset Data Set Ready	This is used in an auto answer installation to terminate a call (equivalent to placing the receiver "on hook").
19	Set Data Set Ready	This is normally only used when the system is initialized. In an auto answer installation the detection of the ring signal from the modem will set Data Set Ready.

Before initiating communication with the device on the other end of the line, the program should issue a control 5_8 to reset both the transmitter and the receiver.

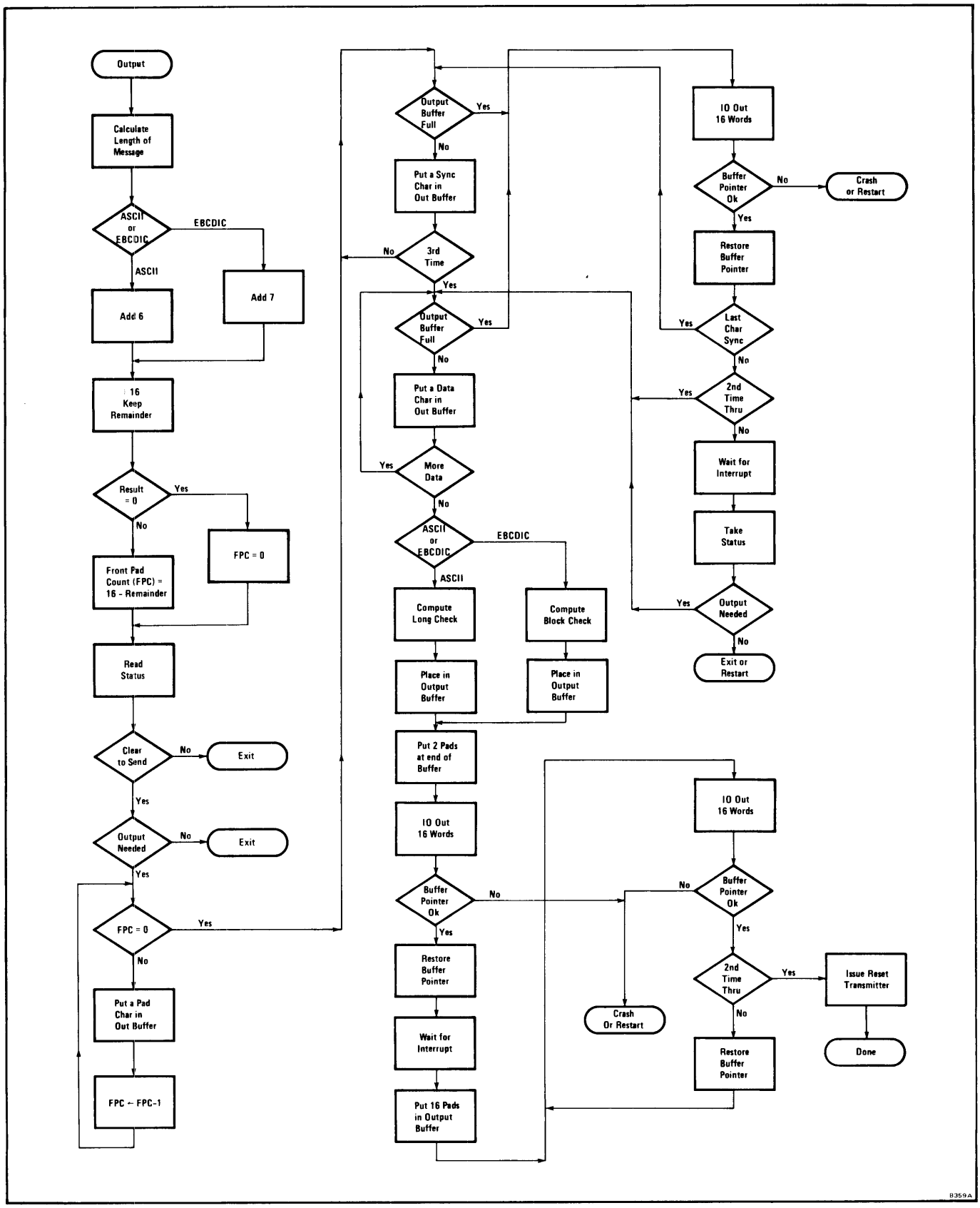
After a request-to-send control is given, the data set will delay a period of time defined by the data set before sending clear to send. This is to allow transients on the phone lines to clear. Typical turn around delay between a request-to-send control and clear-to-send status is 200 milliseconds for half duplex data sets and 8 milliseconds for full duplex data sets. There is no turn around delay associated with these signals going off.

PROGRAMMING NOTES

The data format for use with the 8436 Buffered Synchronous Controller is shown in the illustration "Data Record Format". All transactions are made in 16-byte records that must be constructed as shown; data received on input will appear in this form with one byte in each of 16 words, right justified. Similarly, the data for output must appear in 16 words, one byte to a word, right justified.

Output Method

Essentially, the message is constructed starting at the end: The last two characters of the last record must be pad



Recommended Sequence of Events for Buffered Synchronous Output Transfers

characters (0377), preceded by the longitudinal check character (ASCII) or the two block check characters (EBCDIC) of the message, preceded by the last data character of the message. The first character of the message (in the first or second record) must be preceded by three sync characters (conventionally 026 in ASCII, Hex 62 in EBCDIC). Also, the first record of the message must be left-filled with pads (0377 or 0125 as required by the device).

To calculate the number of pads for the first record, first determine the length of the message in characters (including any start and/or stop characters required by the communications protocol in use). Add 6 to the length (ASCII) or 7 (EBCDIC), divide by 16, then subtract the remainder from 16 for the number of pads. If the result is greater than 13, some of the sync characters will go into both the first and second records.

Before sending a message, make sure status bits 9 and 11 are both 1 (i.e., clear to send and output needed). Then send the first two 16-word records of the message, then idle or go into background processing to wait for an interrupt. When the interrupt is received, make sure status bit 9 is a 1 (output needed), then send one 16-word record and idle again waiting for another interrupt. When the last record of the message is sent, wait for one more interrupt, then send two records of 16 pad characters (0377). This is required to clear the buffers on the controller. Last, issue a reset transmitter control.

All the essential steps in constructing and sending a message are shown conceptually in the flowchart "Recommended Sequence of Events for Buffered Synchronous Output Transfers".

Input Method

On an input operation, the blocks will appear as 16-character records with the sync and pads stripped off. Only the last block of a transfer can be short, with garbage fill to the right. If the characters are to be packed three to a word, it must be done by the software.

The correct procedure for checking status on input is first to check bit 15 (input ready), then bit 12 (sync received). Then, to make sure that a spurious message is not in the buffer, keep a flag to make sure that a carrier was received on this message.

8511/8512
Magnetic Tape Unit

INTRODUCTION

The 8511/8512 Magnetic Tape Unit moves IBM-compatible 9-track, NRZI tape at 12-1/2† inches per second and reads or writes 800 bytes per inch. Data can be read in both the forward and reverse directions, but written only in the forward direction. The tape drive transfers data at a rate of 10,000 characters per second in blocks of from 10 to 4095 characters. Up to four tape drives may be attached to one controller.

The controller is wired to operate under the interrupt system, with an interrupt generated for each word needed on output and for each word received on input. (The controller cannot be used effectively with interrupts disabled.) Thus an interrupt is generated for each three characters transferred. This implies that an interrupt will be generated approximately every 300 microseconds during tape transfers; the software must be prepared to read or write 3 bytes on an average of every 300 microseconds. However, under worst case conditions the controller can wait approximately 450 microseconds for a single interrupt to be honored, but the interrupt immediately following must be serviced more quickly to compensate. If the software delays too long in servicing the interrupt, the data lost status bit will be set, an interrupt will be generated, and the transfer will terminate.

The controller stays selected to the tape drive for all operations except the rewind command. When the rewind command is issued to a tape drive, data transfers with another tape may resume, if the reset command is given. When the drive has been rewound and locates the beginning of tape (BOT) marker, an interrupt will be issued if the reset command has not been given.

Three types of data checking are performed in the controller:

- *Vertical Redundancy Check (VRC).* The vertical parity bit recorded in channel P is generated so that the total number of one bits in each data character is odd.
- *Cyclic Redundancy Check (CRC).* The CRC character recorded at the end of a block of data is based on a modified cyclic code and provides a rigorous method of error detection.
- *Longitudinal Redundancy Check (LRC).* The longitudinal parity bit, recorded at the end of a block of data, is generated so that the total number of one bits on every track (including the CRC character) is even.

† 25 ips or faster drives may also be accommodated by the same controller.

If an error is detected on any of these checks, the parity status bit will be set and the software may try again or set an alarm. Note that these checks are performed on read, write, and skip operations. The parity checking on skip operations can be used to check data without reading it. On tapes written on single capstan machines, data and parity checks obtained on backwards operations may not be completely reliable. This happens principally when tapes written on one machine are read on another. In addition, on write operations, a "read after write" check is performed and the parity bit is set if an error is detected.

A write protect feature is provided. A write enable ring must be installed or the tape cannot be written. If an attempt is made to write a read-only tape, the attempt will fail and the system will hang until SYSTEM RESET is pressed.

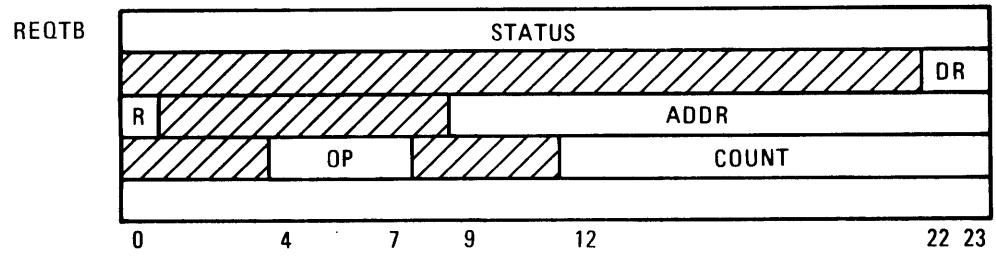
Each tape has a beginning-of-tape (BOT) and end-of-tape (EOT) marker. When the BOT is sensed by the hardware, the tape is halted, an interrupt is generated, and the BOT status bit is set. Note that an attempt to skip backwards past the BOT will fail. When the EOT is sensed, the EOT bit is set and stays up until a rewind is performed.

File marks are written on the tape at the user's discretion; the controller will stop the tape and send a stop interrupt whenever a file mark is read. The tape will be fully stopped before the interrupt is given.

The number of bytes to be read or written by the controller must be specified by the software. On a read operation, the transfer will terminate when a block gap is encountered or this count is reached, whichever comes first unless the transfer is terminated by a data lost (too late) status. On a write operation, exactly this number of bytes will be written unless the transfer is terminated by a data lost status.

A reset feature is provided to allow the software to reset all controls to the addressed tape drive and disconnect the drive. All tape motion is halted immediately, except for rewind. If status is taken on a drive and no control is sent to the drive subsequently, the reset command must be given twice to deselect the drive before another can be statused.

The first tape on a multitape system is conventionally assigned to unit address 44, channel 2, as shown in the table "Four-Phase Standard I/O Priority Assignments" in



Word	Bits	Symbol	Meaning
REQTB	23-0	STATUS†	Bit 23, Drive not ready Bit 22, Busy (error condition) Bit 21, Parity error Bit 20, Write Protect Bit 19, Beginning of Tape (BOT) Bit 18, End of Tape (EOT) Bit 17, Data Lost (too late) Bit 16, File mark Bits 15-13, Not used Bits 12 and 11, Byte boundary on a read = 00, Last data word full, operation complete = 01, Last word has 1 byte left justified = 10, Last word has 2 bytes left justified = 11, Last word full, operation complete Bit 10, Short count Bit 9, Device address out of range (see REQTB+2)‡ Bit 8, Incorrect operation type (see REQTB+3)‡ Bit 7, Number of words transmitted is wrong‡ Bit 6, Lost interrupt Bits 5-1, Not used Bit 0 = 1, Status posted, operation complete‡ = 0, Operation incomplete‡
REQTB+1	23-22 21-0	DR‡	Drive index: 00, 01, 10, or 11 Not used
REQTB+2	23-9 8-1 0	ADDR‡ R‡	Memory address of tape data buffer Not used Bit 0 = 1, Normal return only when operation complete = 0, Return when operation queued or initiated
REQTB+3	23-12 11-8 7-4 3-0	COUNT‡ OP‡	Read or Write count in bytes Not used Operation Type 000 = Read; interrupts 001 = Write; interrupts 002 = Write file mark 003 = Erase 004 = Skip record 005 = Backspace record 006 = Skip file 007 = Backspace file 010 = Rewind 011 = Reset 012 = Read backward; interrupts 013 = Read backward; lockup 014 = Read; lockup 015 = Write; lockup Not used
REQTB+4	23-0	—	BSS 1 — Used by time critical processing in $ITAPE

†Furnished by $ITAPE ‡Furnished by user program ‡Generated by $ITAPE; other bits come from controller and are posted by $ITAPE.

A207C

Tape Device Status Table (DST) Format for $ITAPE

Section 3. However, even in nonstandard configurations, the lowest-numbered drive on a controller circuit must be assigned to a unit address number divisible by 4.

The controller is wired to operate under the interrupt system, using two separate IOID addresses. These addresses do not correspond exactly to the unit addresses of the separate drives (see the table in Section 3). It is the responsibility of the software to keep track of which drive the controller is selected to.

The two IOID addresses that can be generated are 045, which signals the normal or abnormal (data lost) end of a data transfer and should be interpreted as a request from the controller for the CPU to read status, and 044, which indicates "data needed or ready" (see status bit 15). IOID address 044 allows the CPU to accept a word or block on input or present a word or block on output using a single instruction IO.

On a write operation, the sequence of operations is: status, control, IO data out. The first word sent will be kept by the controller and written when the tape deck is up to speed. After this happens, the interrupt 044 will be given as soon as the next word is needed.

On all other operations except reset, the sequence is status, control, then wait for interrupt.

The method for selecting a deck is to ask for status on the deck; but if the controller is busy with another deck, Busy (bit 22) = 1 and the software must wait for the other transfer to terminate (interrupt 045) or it must give a reset.

STATUS CHECKING

The status word associated with the 8511/8512 Magnetic Tape Unit is:

Bit	Name	Meaning
23	Not ready	The tape unit is not ready for a transfer. Usually this means that some physical intervention is required: e.g., tape not loaded, power off, etc.
22	Busy	The controller is performing a transfer with (selected to) another unit. The controller can deal with only one unit at a time. If the controller is selected to the addressed unit, then Busy = 0.
21	Parity	An error has been detected in one of the parity checking circuits. This bit is reset when status is taken.
20	Write Protect	No write enable ring is installed on this tape. It is not possible to write on a tape without the ring being installed.
19	Beginning of Tape	A BOT has been sensed and the heads are positioned just past this point. A stopped-tape interrupt is generated when this bit goes true on rewind or backwards.
18	End of Tape	An EOT has been sensed. This bit stays up when the tape is past the EOT stripe, and resets when a rewind is performed.
17	Data Lost	The computer has waited too long between read or write operations and a word or words of data have been lost or not written. An interrupt is generated when this bit goes true unless one is pending; the bit is reset when status is taken.
16	File mark	A file mark† has been encountered. This bit can terminate a read or skip operation. A stopping tape operation is initiated when this bit goes true; reset when status is taken.
15	Word needed or ready	Functions only during word mode (control bit 8). Whenever this mode is selected for a read or write operation, an interrupt is generated every time a word has been sent or received and another I/O transaction is required. This interrupt generates a special IOID address (044), so that status need not be taken when it comes up. The bit is reset by the IO data in or out instruction.
14	Stopping	A tape operation is complete and the controller is halting the motion of the tape at the end of a block. If the computer doesn't respond within the tape drive's stop time by initiating another operation, the currently selected unit will be allowed to disconnect. An interrupt is generated when this bit goes false (tape is stopped).
13	Rewind in progress	A rewind is taking place on the selected unit. No other operation can take place on this unit at this time. On termination of rewind, BOT (bit 19) goes true.

† A file mark is defined as a block of two special characters eight character spaces apart. This precludes data and file marks being confused.

Bit	Name	Meaning
12, 11	Byte boundary	Read operation only. The last word of a read operation may contain 1, 2, or 3 bytes of valid data, with garbage fill. The byte boundary is encoded as follows:

Bit 11	12	Last Data Byte
0	0	All bytes full
0	1	Right byte full
1	0	Right & middle bytes full
1	1	All bytes full

10	Short	The count given on a read operation was shorter than the block actually on the tape. This bit will also occur on a skip operation when a zero byte count is given. It may also appear on a rewind. Any command except reset and rewind resets short.

CONTROL SIGNALS

The control word associated with the 8511/8512 Magnetic Tape Unit is:

Bit	Name	Meaning
23-12	Byte Count	The number of bytes to be read or written, in binary, right justified (i.e., least significant bit in bit 23). On a read operation, the read will terminate when this count is reached or a block gap, data lost, or file mark occurs, whichever comes first. On a write operation, exactly this number of bytes will be written, unless a word needed interrupt (status bit 15) is not acted upon soon enough. In this case, the operation will be terminated prematurely with the data lost status (bit 17) set.
11-10		Not used.
9	Reset	Resets all controls to the selected tape drive and disconnects the drive. All tape motion (except for rewind) is halted immediately. Rewind is not affected by reset. If reset is given during a write operation, the operation will halt, the data will be lost, and an invalid block may be written. If status is taken on a drive and no control is given to the drive subsequently, reset must be used to deselect the drive before another can be statused. Reset only operates after another control has been given, so that if status has been taken and no control given, two reset controls are required to deselect the drive.
8	Word mode	On read or write, a single word will be transferred, then an interrupt generated on status bit 15. This is the special interrupt that gives a different IOID address (044) from other status conditions (IOID address 045). Thus, the interrupt may be serviced using IOID followed by IO data in or out, without need for taking status. If bit 8 = 0, the controller will operate in lockup mode, keeping the CPU locked until the data transfer is complete.
7	File mark	If given with bit 0, write a file mark. If given with bit 3, skip to file mark.
6	Rewind	Rewinds the tape. This is the only tape movement that does not require the controller to remain selected to the drive.
5	Erase	A 3-1/2 inch length of tape will be erased. Normally this control will not be required because the drive erases as it writes.
4		Not used.
3	Skip	If given without any other bits, skip a physical block to the next block gap. If given with bit 7, skip to the next file mark. Any skip may be backwards.
2	Backward	If given with bit 1, read backwards. If given with bit 3, skip backwards. Illegal with write or erase.
1	Read	For the legal read combinations, see "Legal Combinations of Control Bits".
0	Write	For the legal write combinations, see "Legal Combinations of Control Bits".

LEGAL COMBINATIONS OF CONTROL BITS

Bits 0-8 (Octal)	Meaning	Explanation
004	Rewind	Upon receiving this command, the controller issues a rewind signal to the selected tape deck. When the signal has been given, the controller terminates the IO transfer from the CPU, which then continues with other operations. While rewinding is proceeding, status bit 13 (rewind in progress) stays true for this deck (if reset is not used), until the BOT marker is sensed. When this happens, the tape deck stops, then moves forward to the BOT marker, and the stopping and BOT status bits (14 and 19) are set, then stopping is reset.
010	Erase	Causes the tape deck to erase about 3.5 inches of tape. When the erase is finished, the stopping status bit (14) is set, then reset when stopped.
040	Skip forward one block	The same as a read except that no data is read. The operation is terminated by the sensing of a block gap. Short and stopping (10 and 14) may be set in the status word.
042	Skip forward to file mark	The same as skip forward one block except that the operation is terminated when a file mark is sensed and the file mark status bit (16) is set. Stopping (bit 14) is set when stopping begins and reset when it is finished.
140	Skip backward one block	The same as skip forward one block except that the direction of tape motion is backwards. Skip backwards one block followed by write should not be repeated more than five times without skipping backwards a second block or performing some other operation to reestablish the size of the block gap.
142	Skip backward to file mark	The same as skip forward to file mark except that the direction of tape motion is backwards.
200	Read forward in lockup	A block of data and its check characters (in a separate word) are transferred to the CPU in lockup mode. The controller will not drop the CPU until either the byte count is exhausted or the end of the block is detected. At the end of the operation the stopping bit (14) and byte boundary status bits (11 and 12) are set appropriately, and parity (21), short count (10), and data lost (17) are set conditionally.
201	Read forward in word mode	The same as read forward in lockup, except that the controller drops the CPU after every word transferred and issues a word ready interrupt (bit 15) every time a word is ready. After the block is read, stopping status and the other status bits are set appropriately as under read forward in lockup. Data lost (bit 17) may be set.
300	Read backward in lockup	The same as read forward in lockup, except that the direction of tape motion is backwards, and the data appears in memory last word first. The check characters are in the 1st word.
301	Read backward in word mode	The same as read forward in word mode, except that the direction of tape motion is backwards, and the data appears in memory last word first.
400	Write in lockup	The data from the CPU is written onto tape in lockup mode. The controller locks up the CPU for the duration of the transfer, which is determined by the byte count in the command word. The controller generates and writes the CRC and LRC characters also. VRC and LRC parity are also checked during writing. When the write is terminated, the stopping bit (14) is set and parity (21) and data lost (17) are set conditionally.
401	Write in word mode	The data from the CPU is written onto tape in word mode. The controller takes a single word from the CPU, drops the CPU, and writes the word to tape. When another word is needed, a data needed interrupt (bit 15) is issued. The operation is terminated by completion of the byte count or by the data lost status (17) going true. As in write in lockup, the CRC and LRC characters are also written.
402	Write file mark	A file mark is written on the tape. The file mark is generated by the controller and no IO out instruction is issued by the program. When the operation is complete, stopping (bit 14) and either file mark (16) or parity (21) are set conditionally.

PROGRAMMING TAPE TRANSFERS

It is intended that all tape I/O operations take place under control of $ITAPE, a system program provided to perform all controls, reads, and writes for up to four tape units. The $ITAPE program provided for the 8511/8512 tape drives operates under the interrupt system of the System IV/70 processor, expecting an interrupt from the controller every time a word is read on input or needed on output. Another program is provided for faster tape drives; it will operate with the System IV/70 in lockup.

All I/O activity in $ITAPE is coordinated with a five-word Device Status Table (DST) for each drive. The program takes status, performs control functions, and reads or writes for each drive as needed. Error recovery attempts are provided automatically. All requests for I/O operations are made using the DST which may not be altered by the user until the I/O operation is complete or rejected. All I/O operations should be performed using $ITAPE so that the DSTs always contain valid information.

The program can be used reentrantly if separate device status tables are used for each request. If the program is busy and cannot serve a new request, the request will be queued and honored as soon as possible.

Permanent error conditions must be processed by the user using the information contained in the status word. No provision is made for generating error messages suitable for the video display or printer. No provision is made for checking tape labels or headers; this is assumed to be a higher level function of the user software. The program saves all registers: RA, RB, X1, X2, and X3.

To request tape I/O operations, first set up the DST beginning at a conveniently labeled location, such as REQTB (see illustration — "Tape Device Status Table (DST) Format"), and then call $ITAPE as follows:

```
      BAL    $ITAPE
+0     PZE   REQTB
+1   (return)
```

Normally the user should check the status word in the DST to determine the outcome of the I/O request. If the return flag (R) is set to 1 when the call to $ITAPE is made, then the return is made only when the operation has been completed successfully or a hard error has developed.

The number of bytes the user program wants transferred on a read or write must be included in the DST. On a write, the output buffer is prepared by the user program and CRC and LRC bytes are added by the controller. On a read, the controller will transfer the block of data (terminated by end-of-block or count-exhausted, whichever comes first) into the memory buffer, then will write the CRC and LRC characters, right justified, into the next word. Thus, the software must allow for a buffer one word longer than the number of words required to hold the block.

On a read, $ITAPE will count the number of bytes actually transferred and return this number in the DST in bits 12-23 of REQTB+3. If the read operation is terminated by a inter-block gap, the count returned by the program will be smaller that that given by the user; this offers the user a method for detecting a short block. If the read operation is terminated by count-exhausted before end-of-block is detected, the short-count status bit will be set and only the number of words requested will be sent.

When $ITAPE returns to the calling program after any operation, the status of the addressed drive is contained in location REQTB+0. The $ITAPE program generates certain status bits in addition to those generated by the hardware.

Note that the DST contains five words, rather than the four used with $DISC. The fifth word is used as a queuing trigger when time-critical processing is specified. Time-critical processing involves use of the tape with (for example) the card reader, as explained in this document. Time-critical processing is an option that is specified when $ITAPE is assembled.

BOOTSTRAP MODE

The magnetic tape unit can function as a bootstrap unit if the appropriate jumper is installed on the controller at time of manufacture; this is the normal configuration for all Four-Phase Systems supported tape controllers. The bootstrap mode is forced any time System Reset is pressed, and cleared when a record is read or status is taken. However, the unit will not begin to function as a bootstrap input device until it is selected in the channel and unit address fields of an IO select word. If System Reset is issued for some reason other than bootstrapping from this device, the software must issue a status IO operation before the unit can be used. For this and other reasons it is considered good programming practice to issue a status IO before controlling or giving any other IO operation.

If more than one magnetic tape unit is installed on a controller, only drive 0 can be used as a bootstrap device. Bootstrap functions from BOT only.

8513
Magnetic Tape Unit

INTRODUCTION

The 8513 Magnetic Tape Unit moves IBM-compatible, 9-track, Phase-Encoded tape at 37-1/2 inches per second and reads or writes 1600 bytes per inch. Data can be read in both the forward and reverse directions but written only in the forward direction. The tape unit transfers data at a rate of 60,000 characters per second in blocks of from 10 to 16,383 characters. Up to four tape drives may be attached to one controller.

The controller is wired to operate under the interrupt system† of the System IV/70 with two IOID addresses, as explained below. One interrupt address is generated for operation complete or rejected, the other for data needed or ready. An interrupt is generated for each block transferred, in or out, and the transfers are made using the computer's lockup mode. Data is transferred three bytes to a word, and a complete block is transferred for each successful input or output operation.

Before any I/O transfer can occur with a deck, the controller must be selected to the deck; i.e., communication between controller and deck must be initiated and confirmed. The method for performing the selection is for the software to ask for status on the specified deck; the method for confirming that the selection has occurred is to receive ready status (bit 23 = 0). (Other statuses may also be true at selection time: beginning of tape, end of tape, etc. These do not interfere with the selection process.) The selection may fail for one of several reasons. A physical problem requiring human intervention can cause selection to fail, as can the controller being selected to some other deck than the one addressed. If the controller cannot accept a selection at this time, the status word will return with reject set (other status bits will be valid at this time), and the software can either issue reset to deselect the other deck or wait for operation complete.

Once successful selection is achieved, the required control may be given. If any operation but a read or a write is needed, the control IO instruction can be given and the software may go about its business until the operation-complete or reject interrupt is given; the software must then take status to determine which. In any event, if the control is accepted, busy status will be set, indicating that the control is accepted and another control will not be accepted until the current operation is complete or reset is given; i.e., until busy drops.

On a read, the software can go about its business if the control is accepted: the data-ready interrupt will occur when the deck is up to speed and the deck logic has started searching for a block to be read. If the deck is stopped in front of a long erased section when the IO in instruction is given, the controller will keep the computer locked up until the data is found and the read is completed. This can take considerable time; if the gap is long, it can require many milliseconds. In the best case, when the deck is positioned just at the end of a block gap, the software has the preamble time or about 700 microseconds to respond to the interrupt. If the software is engaged in time critical operations, such as those involving taking characters from a keyboard, the read timeout feature is available. If this control (bit 8) is given on a read, the deck will search for 11 milliseconds and then drop the computer if no data is found. Too late status will indicate that this failure has occurred. The software can then retry by skipping backward and reading forward, since it is presumably closer to the start of the block now.

On a write, first the control is given, then the software must immediately give an IO out instruction. Only the first word of the block will be taken by the controller at this time. Then, when the controller is up to speed and the write is about to begin, a data needed interrupt will occur. The software must then respond with a second IO out instruction to send the rest of the block.

The controller stays selected to the tape deck for all operations except the rewind command. When the rewind command is issued to a tape deck, the reset command may be given to allow the controller to select to another deck. When the drive has been rewound and has located the beginning-of-tape (BOT) marker, an interrupt will be issued if the reset command has not been given. If reset has been given, the deck must be statused to find out when the rewind is complete.

The tape deck and formatter logic performs parity checking and automatically attempts error recovery procedures when an error is detected. If an error is detected on a write, the software must perform a retry. On a read, some error conditions can be corrected by the logic; if this happens,

† It is also possible to operate the tape drive without interrupts, although this procedure is not generally recommended. The software loops on status between operations with level 2 interrupts disabled or, alternatively, loops on status and discards interrupts that are irrelevant to its operations. The software must be alert for status changes that occur asynchronously; note that a new control can only be accepted after operation complete (status bit 6) is true.

The corrected-parity-error bit will be set in the status word given when the read is complete. The software has the option to accept the corrected data or retry. Four-Phase supported software will always retry. Other error conditions can be detected that the logic cannot correct; if this occurs, the hard-error status bit will be set and the software must retry. Most parity errors can also be detected on a skip operation, and a skip operation can be used to check data without reading it. However, on tapes written on single capstan machines, parity checks obtained on skip backward operations may not be completely reliable. This happens principally when tapes written on one machine are read on another.

A write protect feature is provided. A write enable ring must be installed or the tape cannot be written. If an attempt is made to write a read-only tape, the attempt will fail and reject will be set.

Each tape has a beginning-of-tape (BOT) and end-of-tape (EOT) marker. When the BOT is sensed by the hardware, the tape is halted, an interrupt is generated, and the BOT status bit is set. Note that an attempt to skip backward past the BOT will be rejected. When the EOT is sensed, the EOT bit is set and stays up during the operation in which it is detected only — unless the tape is stopped over the tab, in which case it stays up until the tape is moved.

File marks are written on the tape at the user's discretion; the controller will stop the tape and send an operation complete interrupt with file mark status set whenever a file mark is read. The tape will be fully stopped before the interrupt is given.

The number of bytes to be read or written by the controller must be specified by the software. On a read operation, the transfer will terminate when a block gap is encountered or this count is reached, whichever comes first, unless the transfer is terminated by a data lost (too late) status. On a write operation, exactly this number of bytes will be written unless the transfer is terminated by a data lost status.

A reset feature is provided to allow the software to reset all controls to the addressed tape drive and disconnect the drive. All tape motion is halted immediately, except for rewind. The reset control bit should be used with care.

The first tape on a multitape system is conventionally assigned to unit address 044, channel 2, as shown in the table "Four-Phase Standard I/O Priority Assignments" in Section 3. However, even in nonstandard configurations, the lowest-numbered drive on a controller circuit must be assigned to a unit address number divisible by 4.

The controller is wired to operate under the interrupt system, using two separate IOID addresses. These addresses do not correspond exactly to the unit addresses of the separate drives (see the table in Section 3). It is the responsibility of the software to keep track of which drive the controller is selected to.

The two IOID addresses that can be generated are 045, which signals the normal or abnormal (operation complete or reject) completion of a command, and should be interpreted as a request from the controller for the processor to read status, and 044, which indicates "data needed or ready" (see status bit 15). IOID address 044 allows the processor to accept a block on input or present a block on output using a single instruction IO.

STATUS CHECKING

The status word associated with 8513 Magnetic Tape Unit is:

Bit	Name	Meaning
23	Not ready	The tape unit is not ready for a transfer. This may mean that some physical intervention is required: e.g., tape not loaded, power off, etc., or it may mean that the drive addressed is not selected. Bit 23 = 0 means that this drive is selected and not rewinding.
22	Busy	The controller is performing an operation with this or another selected unit. The controller can deal with only one unit at a time. If the controller is selected to the addressed unit (can accept a control for the unit), Busy = 0.
21	Hard Error	A parity error or other error that the drive error correcting circuits cannot correct has been detected. This error can occur on read, write, or skip operations. The software *must* retry. Forces operation complete (bit 6) with its corresponding interrupt. This bit is reset by taking status after operation complete has come on.
20	Write Protect	No write enable ring is installed on this tape. It is not possible to write on a tape without the ring being installed.
19	Beginning of Tape	A BOT has been sensed and the heads are positioned just past this point. Rewinding (bit 13) goes false and operation complete (bit 6) goes true and generates an interrupt when BOT is sensed.
18	End of Tape	An EOT has been sensed. At the end of the current block, operation complete (bit 6) will be set and its interrupt generated, unless the tape is stopped over the EOT mark. The bit is reset after the operation complete status is taken.

Bit	Name	Meaning
17	Too Late	The computer has waited too long in responding to bit 15 (data needed). Since the nominal wait time is about 350 machine cycles (700 microseconds), this should happen rarely. Also set on a read timeout when read data is not encountered within 11 milliseconds. See control bit 8. Forces operation complete (bit 6) with its associated interrupt. Reset when status is taken.
16	File mark	A file mark† has been encountered. This bit can terminate a read, skip or write file mark operation. An operation complete (bit 6) will be forced for the end of read or skip, with its associated interrupt. Bit 16 is reset when status is taken.
15	Data Transfer Required	The tape drive is ready for a write or read transfer in response to the latest control word. This interrupt generates a special IOID address (044) so that status need not be taken when it comes up. The controller operates only in lockup mode and will transfer the entire message with a single IO instruction. On a read, if a block gap or file mark is encountered before the count in the control word is exhausted, short (bit 10) and operation complete (bit 6) will be set. Bit 15 is reset by the IO in or out instruction.
14		Not used.
13	Rewinding Tape	Rewinding is taking place as ordered by control bit 6. The drive will not respond to controls until the operation is finished. At the end of rewind, operation complete will be generated, BOT (bit 19) set, bit 13 reset, an interrupt generated, and the drive deselected. However, if the software sends a reset (control bit 9), the interrupt will not occur and the drive will be deselected immediately.
12, 11	Byte Boundary	Read operation only. The last word of a read operation may contain 1, 2, or 3 bytes of valid data, right adjusted with garbage fill. The byte boundary is encoded as follows:

Bit	Bit	Last data byte
0	0	All bytes full
0	1	Right byte full
1	0	Right & middle bytes full
1	1	All bytes full

Bit	Name	Meaning
10	Short	The count given on a read operation was shorter than the block actually on the tape. Forces operation complete and an interrupt. This bit is reset by taking status after operation complete has come on.
9	Reject	There are four reject conditions: (1) An illegal change of address. If the controller is selected to one drive and an attempt is made to address another (for read, write, or control), reject will be set. (2) An attempt to write or erase illegally or with any other tape movement command (e.g., skip). (3) An attempt to move backward from BOT. (4) If a data out IO is given when a write command is not active or a data in IO is given when a read command is not active. In conditions 1, 2, and 3, the operation specified is merely rejected, an interrupt is generated for bit 9 (IOID address 045), and the controller remains selected to the same drive. If condition 4 occurs, reject, too late, and operation complete will all be set and the drive will be deselected. The interrupt will come on address 045.
8	Corrected Parity Error	A parity error has occurred and the hardware correction circuits have adjusted for it. On a write, this bit means that the operation must be repeated; on a read, the data may be used, if absolutely necessary. However, on Four-Phase supported software, this condition is treated as a block error and the software will retry. This bit will be set when the operation complete interrupt is given at the end of the block; bit 8 is reset when status is taken.
7	1600 ID	An IBM 1600 bpi marker has been read on this tape. This bit is set when BOT is encountered and is reset on the first operation.

† A file mark is a special pattern of 40 characters preceded by 3.5 inches of blank tape. File marks are written and read automatically.

Bit	Name	Meaning
6	Operation Complete	Signals that an operation has come to a normal (or nonnormal) completion and the device is deselected. This bit forces an interrupt to IOID address 045. If the software is running fully under interrupts, it will issue a command for read or write, wait for the interrupt (address 044), and give the IO in or out instruction when the interrupt is received. The software will wait until operation complete is received; it may then start the next operation by statusing another (or the same) drive to select it. However, the software is not required to wait for operation complete if its next operation is with the same drive: i.e., after the software comes out of the IO lockup, it may status the same drive to make sure that the operation was performed correctly and then issue a new command to the same drive. The software has a unpredictable number of milliseconds in which it may take status again before operation complete comes up. Status bits are reset by the status in IO instruction following the 045 interrupt associated with this bit.

CONTROL SIGNALS

The control word associated with the 8513 Magnetic Tape Unit is:

Bit	Name	Meaning
23-10	Byte Count	The number of bytes to be read or written, in binary, right justified (i.e., least significant bit in bit 23). On a read operation, the read will terminate when this count is reached or a block gap, data lost, or file mark occurs, whichever comes first. On a data write operation, exactly this number of bytes will be written, unless a data lost occurs.
9	Reset Controller	Resets all controls to the selected tape drive and disconnects the drive. All tape motion (except for rewind) is halted immediately. Rewind is not affected by reset. If status is taken on a drive and "ready" is received, indicating that the drive is selected, and if no action is to be taken with the drive, reset must be used to deselect the drive before another drive can be statused for selection.
8	Read Timeout Enable	Enables the time-out circuit on the controller for read operations, forward or backward. This control is used in processing where the magnetic tape is being used at the same time as other time-critical devices such as the keyboards†. When a read command is given to the controller, the interrupt is given to the computer as soon as the drive is up to speed and is looking for the read data (preamble). The computer then gives an IO in instruction and hangs, waiting for the data. If bit 8 was set in the control word, however, the attempted read will end after about 11 milliseconds if no read data is encountered. If this occurs, status bit 17 (too late) will be set and the software must retry. The procedure for this retry is the same as the procedure for a normal too late retry.
7	File mark	If given with bit 0, write a file mark. If given with bit 3, skip to file mark.
6	Rewind	Rewinds the tape. This is the only tape movement that does not require the controller to remain selected to the drive.
5	Erase	A 3-1/2 inch length of tape will be erased. Normally this operation will not be required because the drive erases as it writes.
4		Not used.
3	Skip	If given without any other bits, skip a physical block to the next block gap. If given with bit 7, skip to the next file mark. Any skip may be backward. The software does not need to give any further intervention with this control — when skip is finished, operation complete (bit 6) will be set and its interrupt will be given.

† In reasonably heavy keyboard loading, there is a theoretical maximum of about 17 milliseconds for which keyboard interrupts may be locked out; beyond this length of time keystrokes will probably be lost. The nominal 11 millisecond read timeout period on the magnetic tape is selected to allow a certain amount of leeway.

Bit	Name	Meaning
2	Backward	If given with bit 1, read backward. If given with bit 3, skip backward. Illegal with write or erase.
1	Read	For the legal read combinations, see "Legal Combinations of Control Bits".
0	Write	For the legal write combinations, see "Legal Combinations of Control Bits".

LEGAL COMBINATIONS OF CONTROL BITS

Following are the legal controls that may be given, with the status bits that may occur when they are given. Note that EOT (bit 18) can be set by any operation; 1600 ID (bit 7) will appear on any read or skip from BOT; corrected or hard error (bits 8 or 21) can occur on any read, write, or skip operation; and too late (bit 17) on any read or write operation. File mark (bit 16) can occur on any read or skip operation and will terminate the operation; reject (bit 9) can occur after any illegal command (e.g., when a tape deck is not selected or is busy). Also, operation complete (bit 6) will come up when any operation is completed and another operation can be initiated.

Bits 0-8 Octal	Meaning	Explanation
004	Rewind	Upon receiving this command, the controller issues a rewind signal to the selected tape deck. When the signal has been given, the controller terminates the IO transfer from the processing unit, which then continues with other operations. The not-ready status bit (23) is set but the controller remains selected to the deck unless the reset command is given. While rewinding is proceeding, status bit 13 (rewinding tape) stays true for this deck (unless reset is given), until the BOT marker is sensed. When this happens, the tape deck stops, then moves forward to the BOT marker, and the operation-complete and BOT status bits (6 and 19) are set.
010	Erase	Causes the tape deck to erase about 3.5 inches of tape. When the erase is finished, the operation-complete status bit (6) is set and its interrupt is given.
040	Skip forward one block	The same as a read except that no data is read. The operation is terminated by the sensing of a block gap (or file mark).
042	Skip forward to file mark	The same as skip forward one block except that the operation is terminated only when a file mark is sensed; the file-mark status bit (16) is also set when the operation is complete.
140	Skip backward one block	The same as skip forward one block except that the direction of tape movement is backward. Skip backward one block followed by write should not be repeated more than five times without skipping backward a second block or performing some other operation to reestablish the size of the block gap.
142	Skip backward to file mark	The same as skip forward to file mark except that the direction of tape motion is backward. Terminates at BOT if no file mark is found.
200	Read forward	A block of data is transferred to the processor in lockup mode. The controller will not drop the processor until either the byte count is exhausted or the end of the block is detected.
201	Read forward with timeout	The same as read forward except that the timer is started when the tape drive starts searching for data and if 11 milliseconds elapses before a data block preamble is encountered, the operation is halted and too-late status bit (17) is set. The operation-complete status bit (6) and its interrupt are also generated.
300	Read backward	The same as read forward except that the direction of tape motion is backward, and the data appears in memory with the last character first. The operation will terminate if BOT is sensed.
301	Read backward with timeout	The same as read forward with timeout except that the direction of tape movement is backward and the data appears in memory last character first.
400	Write	The data from the processor is written onto tape in lockup mode. The controller locks to the processor for the duration of the transfer, which

Bit	Name	Meaning
		is determined by the byte count in the command word.
402	Write file mark	A file mark is written on the tape. The file mark is generated by the controller and no IO out instruction is issued by the program. When the operation is finished, operation complete and file mark (bits 6 and 16) are set.

PROGRAMMING TAPE TRANSFERS

It is intended that all tape I/O transfers take place under control of $JTAPE, a system program provided to perform all controls, reads, and writes for up to four tape units. The $JTAPE program is provided exclusively for the 8513 Magnetic Tape Unit; $ITAPE is used for the 8511/8512 (800 bpi) Magnetic Tape Unit. $JTAPE operates under the interrupt system of the System IV/70 processor, expecting an interrupt from the controller every time a block is read on input or needed on output. On read and write operations $JTAPE operates strictly in lockup mode. On a write, it takes exactly the number of bytes specified, and on a read, it gives the number of bytes specified or sets the short status bit if too few bytes are available in the block.

All I/O activity in $JTAPE is coordinated with a five-word Device Status Table (DST) for each drive (see the illustration — "Tape Device Status Table (DST) Format"). The program takes status, performs control functions, and reads or writes for each drive, using the DST to communicate with the background or calling program. All requests for I/O operations are made using the DST, which may not be altered by the user until the I/O operation is complete or rejected. All tape I/O operations should be made using $JTAPE so that the DSTs always contain valid information.

Note that the DST contains five words, rather than the four used with the $DISC program. The fifth word is used as a queuing trigger when time-critical processing is specified. Time-critical processing normally involves use of the tape with (for example) the card reader as explained in this document. Time-critical processing is an option that the user must specify at the time $JTAPE is assembled.

The program can be used without regard for the problem of reentrancy if separate DSTs are used for each request. If the program is busy and cannot serve a new request, the request will be queued and honored as soon as possible.

The $JTAPE program provides error recovery attempts automatically, but permanent error conditions must be processed by the user using the information contained in the status word. No provision is made for generating error messages suitable for the video display or printer. No provision is made for checking tape labels or headers; this is assumed to be a higher level function of the user software. The program saves all registers: RA, RB, X1, X2, X3.

To request a tape I/O operation, first set up the DST beginning at a conveniently labeled location, such as REQTB (see the illustration — "Tape Device Status Table (DST) Format"), then call $JTAPE as follows:

```
      BAL    $JTAPE
+0     PZE   REQTB
+1    (return)
```

Conventionally the user will check the status word in the DST to determine the outcome of the I/O request. If the return flag (R) is set to 1 when the call to $JTAPE is made, then the return is made only when the operation has been completed successfully or a hard error has developed.

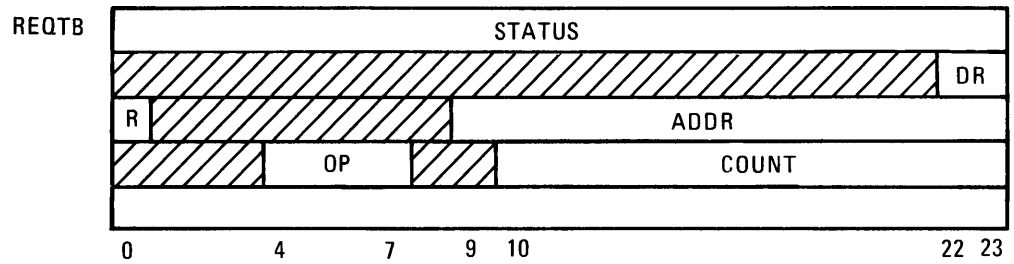
On a read, $JTAPE will count the number of bytes actually transferred and return this number in the DST in bits 10-23 of location REQTB + 3. If the read operation is terminated by an interblock gap, the count returned by the program will be smaller than that given by the user; this offers the user a method for detecting a short block. If the read operation is terminated by count-exhausted before end-of-block is detected, the short-count status bit will be set and only the number of words requested will be sent.

When $JTAPE returns to the calling program after any operation, the status of the addressed drive is contained in location REQTB + 0, if status posted is true (bit 0 = 1). The $JTAPE program generates certain status bits in addition to those generated by the hardware.

BOOTSTRAP MODE

The magnetic tape unit can function as a bootstrap unit if the appropriate jumper is installed on the controller at time of manufacture; this is the normal configuration for all Four-Phase Systems supported tape controllers. The bootstrap mode is forced any time System Reset is pressed, and cleared when a record is read or status is taken. However, the unit will not begin to function as a bootstrap input device until it is selected in the channel and unit address fields of an IO select word. If System Reset is issued for some reason other than bootstrapping from this device, the software must issue a status IO operation before the unit can be used. For this and other reasons it is considered good programming practice to issue a status IO before controlling or giving any other IO operation.

If more than one magnetic tape unit is installed on a controller, only drive 0 can be used as a bootstrap device. Bootstrap functions from BOT only.



Word	Bits	Symbol	Meaning
REQTB	23-0	STATUS†	Bit 23, Drive not ready Bit 22, Busy Bit 21, Hard Error Bit 20, Write Protect Bit 15, Transfer required Bit 14, Not used Bit 13, Rewinding Bits 12 and 11, Byte boundary on a read = 00, Last data word full, operation complete = 01, Last word has 1 byte left justified = 10, Last word has 2 bytes left justified = 11, Last word full, operation complete Bit 10, Short count Bit 9, Reject Bit 8, Corrected parity Bit 7, 1600 ID Bit 6, Operation complete Bit 5, Device address out of range (see REQTB+2)‡ Bit 4, Incorrect operation type (see REQTB+3)‡ Bit 3, Number of words transmitted is wrong‡ Bit 2, Lost interrupt Bit 0 = 1, Status posted, operation complete‡ = 0, Operation incomplete‡ Bit 19, Beginning of Tape (BOT) Bit 18, End of Tape (EOT) Bit 17, Too Late Bit 16, File mark Bit 1, Not used
REQTB+1	23-22 21-0	DR‡	Drive index: 00, 01, 10, or 11 Not used
REQTB+2	23-9 8-1 0	ADDR‡ R‡	Memory address of tape data buffer Not used Bit 0 = 1, Normal return only when operation complete = 0, Return when operation queued or initiated
REQTB+3	23-10 9-8 7-4 3-0	COUNT‡ OP‡ —	Read or Write count in bytes Not used Operation Type 000 = Read 001 = Write 002 = File mark 003 = Erase 004 = Skip record 005 = Backspace record 006 = Skip file 007 = Backspace file 010 = Rewind 011 = Reset Not used
REQTB+4	23-0	—	BSS 1 — Used by time critical processing in $JTAPE

†Furnished by $JTAPE ‡Furnished by user program ‡Generated by $JTAPE; other bits come from controller and are posted by $JTAPE.

A364A

Tape Device Status Table (DST) Format for $JTAPE

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SIV/70–40–1D

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