M243XL

Magnetic Tape Subsystem
MTU Theory of Operation

FUJITSU

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CHAPTER 1. GENERAL DESCRIPTION OF THE MAGNETIC TAPE UNIT

1.1 Introduction

The M243XL magnetic tape unit (MTU) is connected to the host controller via the magnetic tape formatter (FMT). Data is recorded and read back using magnetic tape as the storage medium.

The MTU consists of the magnetic tape feeding mechanism, autoload mechanism, record/read-back mechanism, and control circuits. Because the tape-drive mechanism uses a single capstan system driven by a DC motor, the oxide coating surface of the magnetic tape loaded in the tape feeding mechanism touches only the read/write head, the cleaning ribbon, and the tape cleaner blades, thereby achieving high reliability. The auto-hub mechanism makes it easy to mount and remove tape reels; the power window automates the window opening and closing, and the autocleaner reduces operator tasks.

The magnetic head uses a two-gap head to perform instantaneous read-in of written data and to check data. The system uses 9 tracks. Available recording densities are 6250 rpi (rows per inch), 1600 rpi, and 800 rpi, in recording modes of group coded recording (GCR), phase encoded recording (PE), and nonreturn to zero change at "1" (NRZI).

The normal tape speed of the equipment is 75ips for models M2434L1/L2, M2430L, M2431L, and is 125ips for model M2435L1/L2, M2432L, and M2433L. These speeds can be increased to 125ips and 200 ips, respectively, by a streaming function command. The tape speed of models M2436L1/L2/L8 is 200ips.

1.2 Operational Performance

Table 1-1 lists the operational performance of each model.

Table 1-1. MTU specifications.

Items \ Model			M2434L1/ L2 M2430L	M2431L	M2435L1/ L2 M2432L	M2433L	M2436L1/ L2 M2436L8
Density (BPI)			6250/1600	1600/800	6250/1600	1600/800	6250/1600
Recording method			GCR/PE	PE/NRZI	GCR/PE	PE/NRZI	GCR/PE
Data transfer rate (Kb/sec)	Normal (start/stop)		469/120	120/60	781/200	200/100	1250/320
	Streaming		781/200	200/ -	1250/320	320/ -	-
Access time (ms)	Read	Normal	2.6/4.0	4.0/4.0	1.6/2.6	2.6/2.6	1.7/2.3
		Streaming	6.9/6.9	6.9/ -	4.5/4.5	4.5/ -	-
	Write	Normal	2.3/3.0	3.0/3.0	1.5/2.0	2.0/2.0	1.6/1.9
		Streaming	5.7/5.7	5.7/ -	3.7/3.7	3.7/ -	-
Positioning time (ms)	Read		12.3		9.5		-
	Write		22.9		17.3		-
Inter-block gap (IBG) length (inches)			0.3/0.6	0.6/0.6	0.3/0.6	0.6/0.6	0.4(W) 0.3(R)/0.6
Tape speed (IPS)	Normal		75		125		200
	Streaming		125		200		-
Number of tracks			9				
Rewind time (2400 feet reel nominal) (sec)			55				66
Rewind/unload time (2400 feet reel, nominal) (sec)			65				76
Autoloading time (sec)			12				12

1.3 External Features

The M243XL magnetic tape subsystem (MTS) master unit consists of an MTU and either one or two FMTs housed in a single cabinet. Figure 1-1 is a front view of the master unit, showing the MTU on the left and the FMT on the right. Figure 1-2 is a rear view of the master unit, showing the location of the MTU and FMT power supply units and the MTU logic gate. Figure 1-3 shows the rear view of the MTU slave unit. A slave unit contains no FMT.

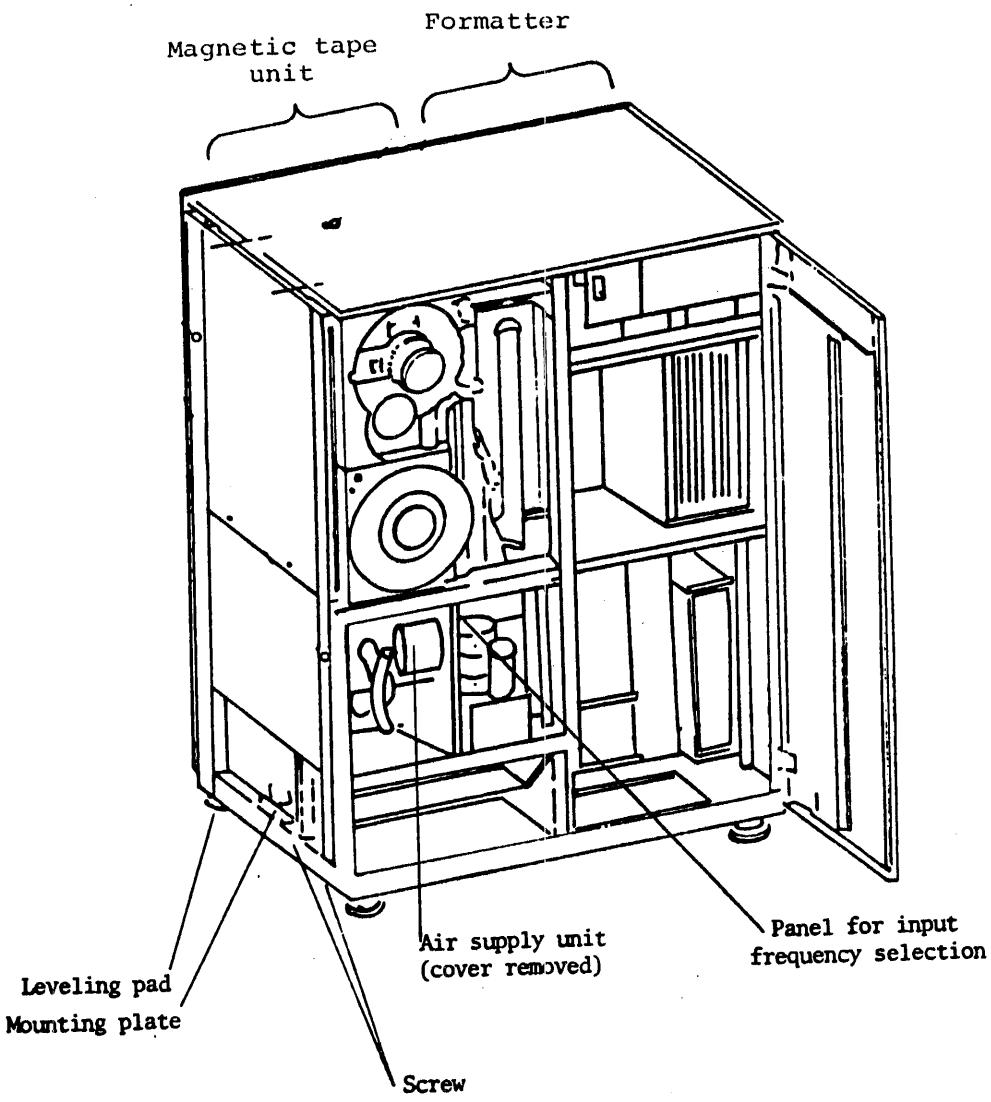


Figure 1-1. Master unit (front view).

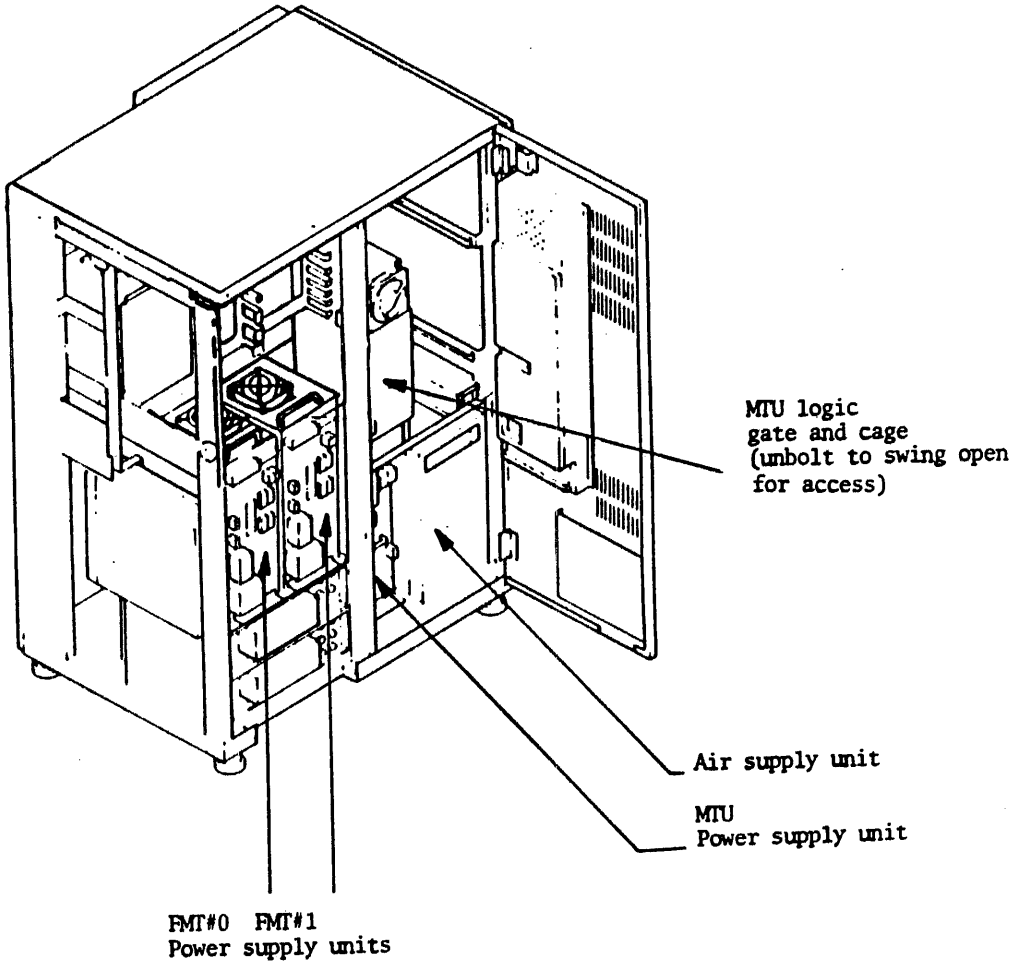


Figure 1-2. Master unit (rear view).

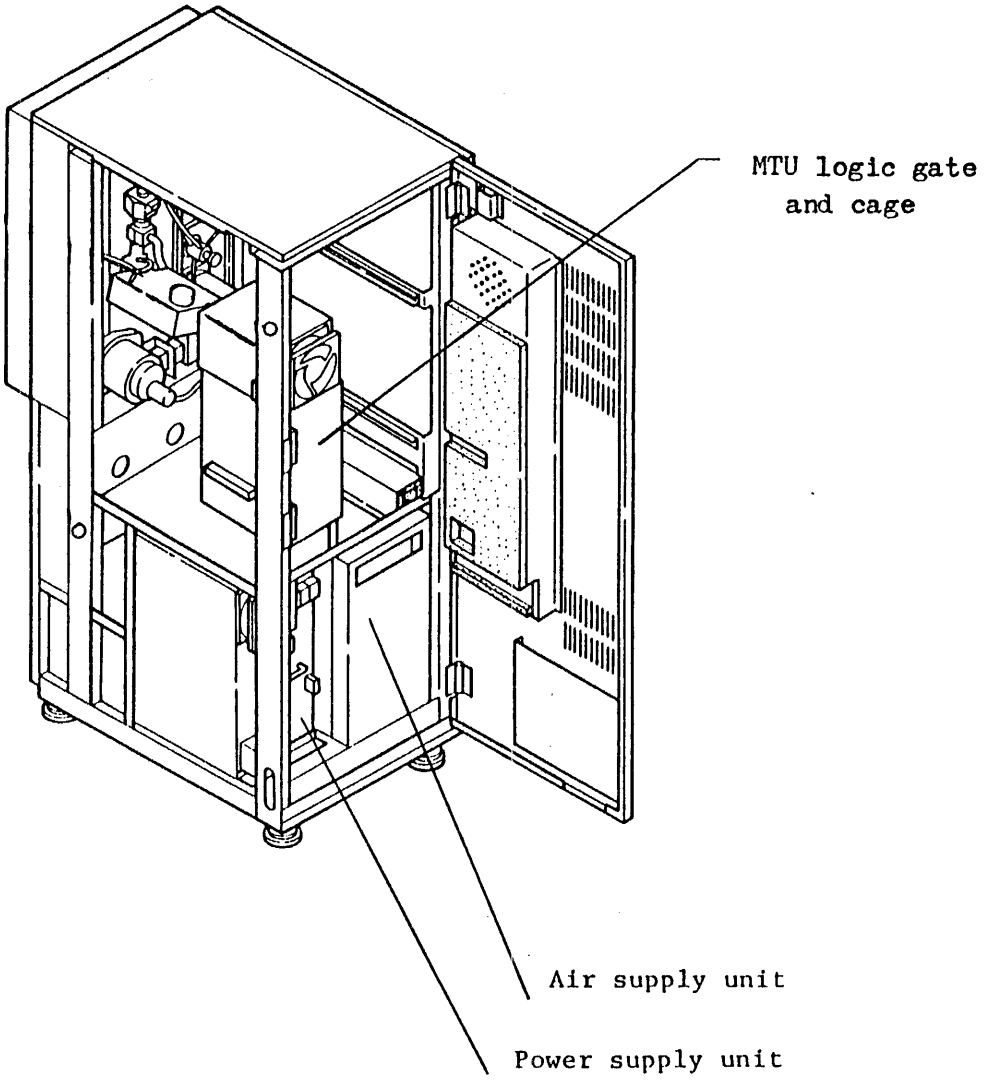
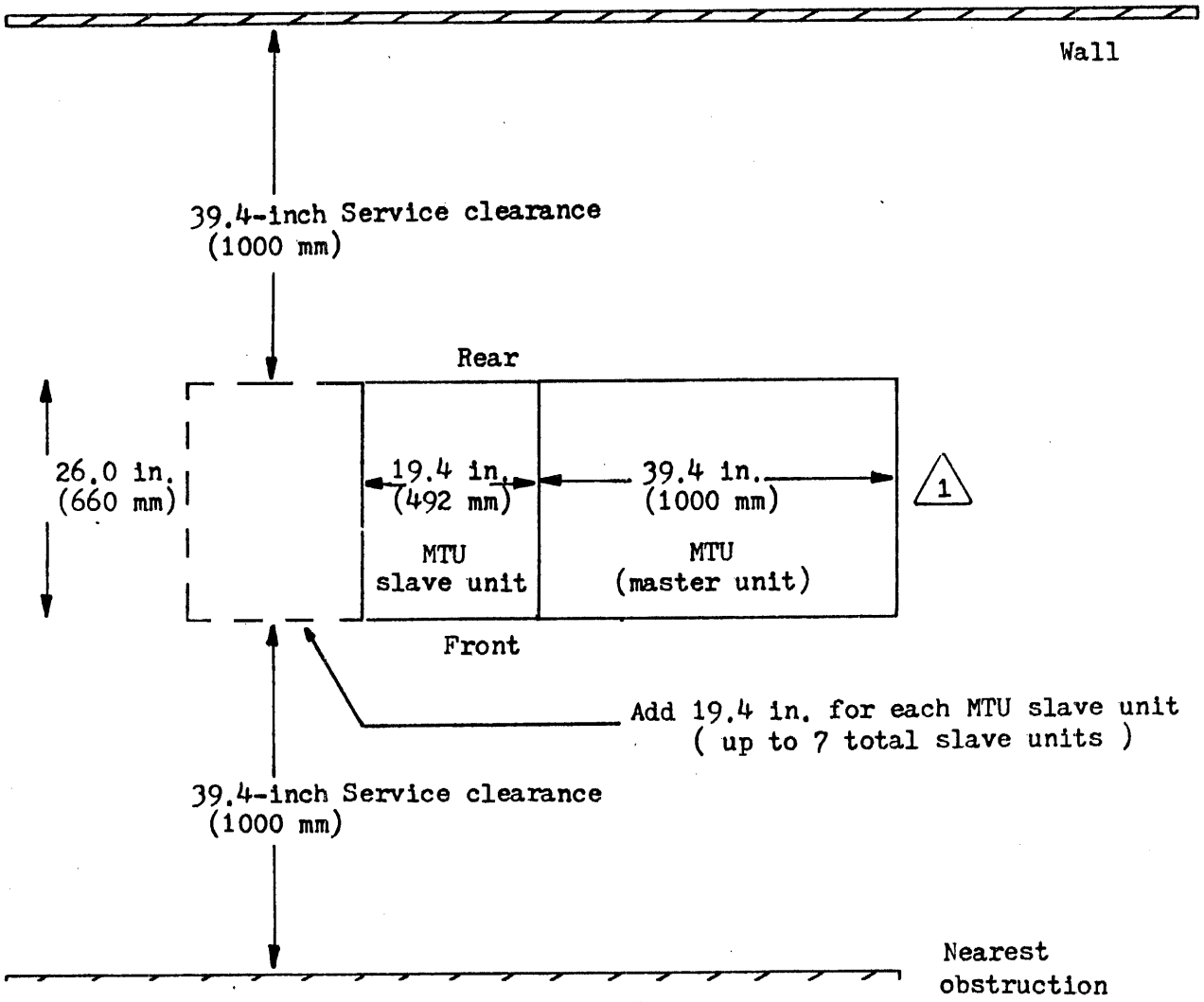


Figure 1-3. Slave unit (rear view).

1.4 Service Clearances

Clearances required for servicing the magnetic tape unit are shown in Figure 1-4.



1 No side clearances required except for installation and maintenance access to rear of unit(s).

Figure 1-4. Service clearances. Plan view.

1.5 Interconnectors

The MTUs are connected to the host/controller via the formatter (FMT), as shown in Figure 1-5. The interface between the FMT and the MTU is the distribution PCA. One FMT can control up to 8 MTUs.

The master unit is available in two models, L1 (one FMT) and L2 (two FMTs). Model L2 is applicable for device crosscall.

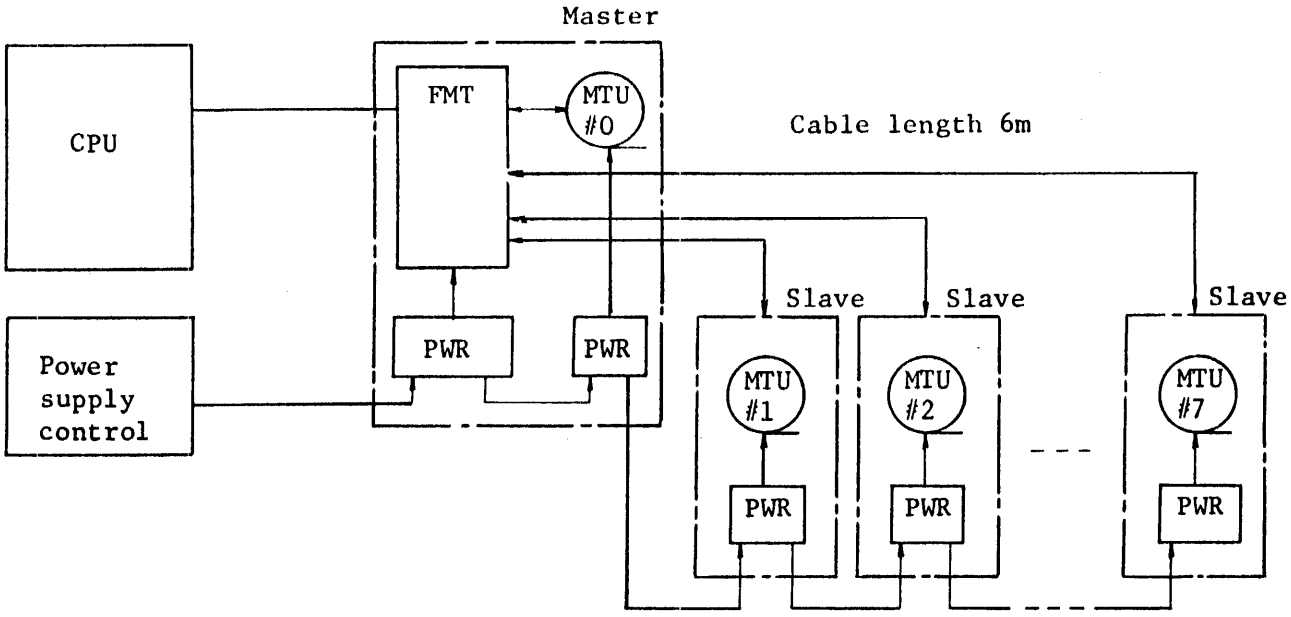


Figure 1-5. MTU interconnections.

1.6 MTU Shorting Plugs.

Shorting plug settings for the MTU are shown below. Refer to the Maintenance Manual when checking or setting the short circuits.

Table 1-2. MTU shorting plugs.

PCA	Mounting position	Level '0' (not enable)	Level '0' (enable)	Setting (see notes)	Contents
1A02				(b)	
1A05	BG7	02 - 03	03 - 04	'0' (b)	
		05 - 06	06 - 07	'0' (b)	
		09 - 10	10 - 11	'0' (a)	APR is supported
		12 - 13	13 - 14	'0' (b)	
1A06	AF4	02 - 03	03 - 04	'0' (a)	Reserved
		05 - 06	06 - 07	'0' (a)	Reserved
		09 - 10	10 - 11	'0' (a)	Reserved
		12 - 13	13 - 14	'0' (a)	APR installed
	AG4	02 - 03	03 - 04	'1' (b)	Extended interface
		05 - 06	06 - 07	'1' (b)	File search by tape drive
		09 - 10	10 - 11	'0' (b)	Tape drive serial number
		12 - 13	13 - 14	(a)	
	AG5	02 - 03 05 - 06	03 - 04 06 - 07	(a)	Tape drive serial number
	AG6	09 - 10	10 - 11	(a)	Tape drive serial number
	AG7	12 - 13	13 - 14	(a)	Tape drive serial number
	AJ6	02 - 03	03 - 04	(a)	Optional density-select panel
		05 - 06 (Step C)	06 - 07 (Step A)	'0' (a)	Threshold gain step for switching read slice level
		12 - 13	13 - 14	'1' (b)	Tri-or dual density tape unit
Read/ write PCA		S3 S4		(b) (b)	S3 = 200 ips S4 = 125 or 200 ips

(a) Setting is determined by factory but can be changed.
(b) Factory set. Do not change.

CHAPTER 2 MECHANICAL OPERATION

2.1 Mechanical Features

Front and rear views of the MTU mechanism are shown in Figures 2-1 and 2-2, respectively.

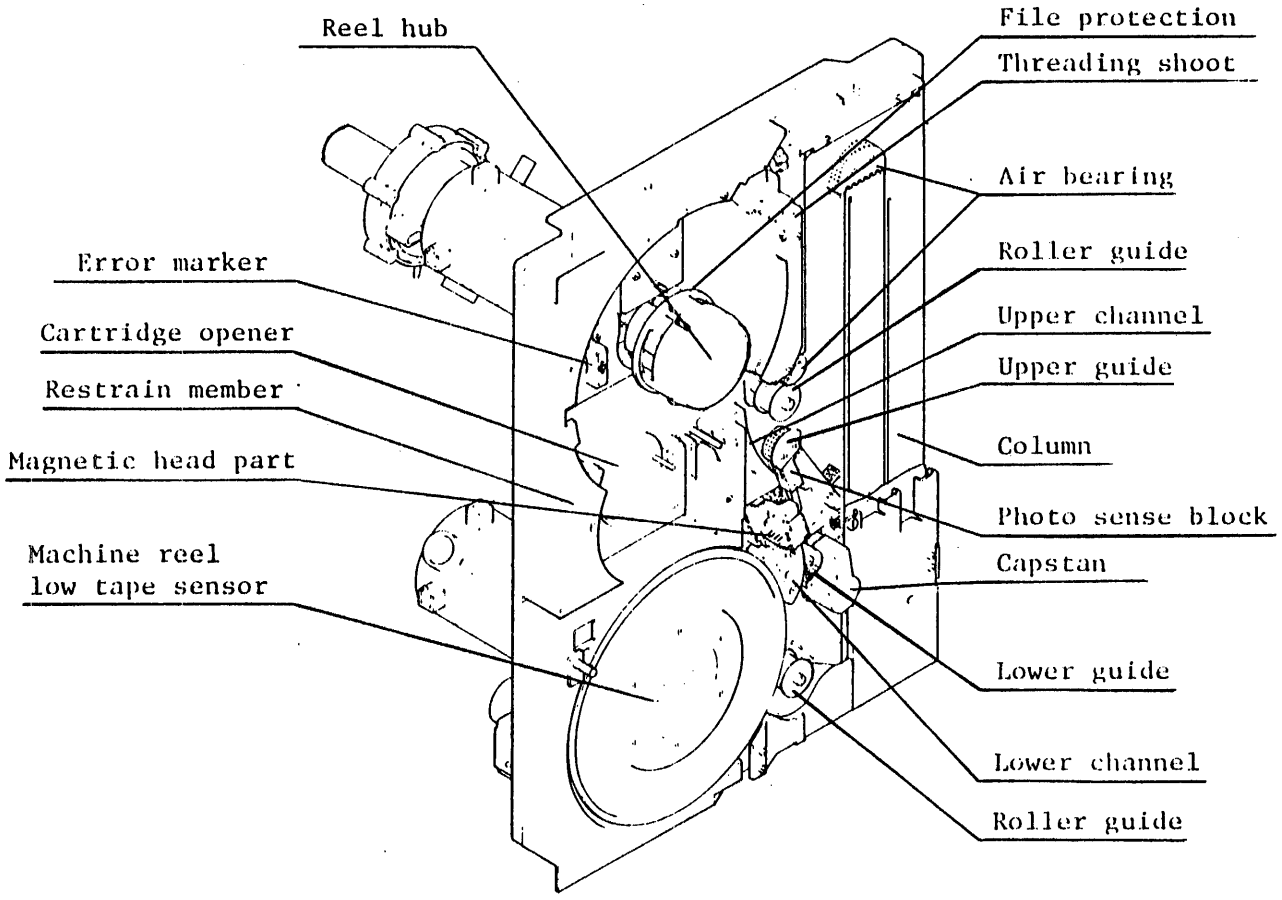


Figure 2-1. MTU front view.

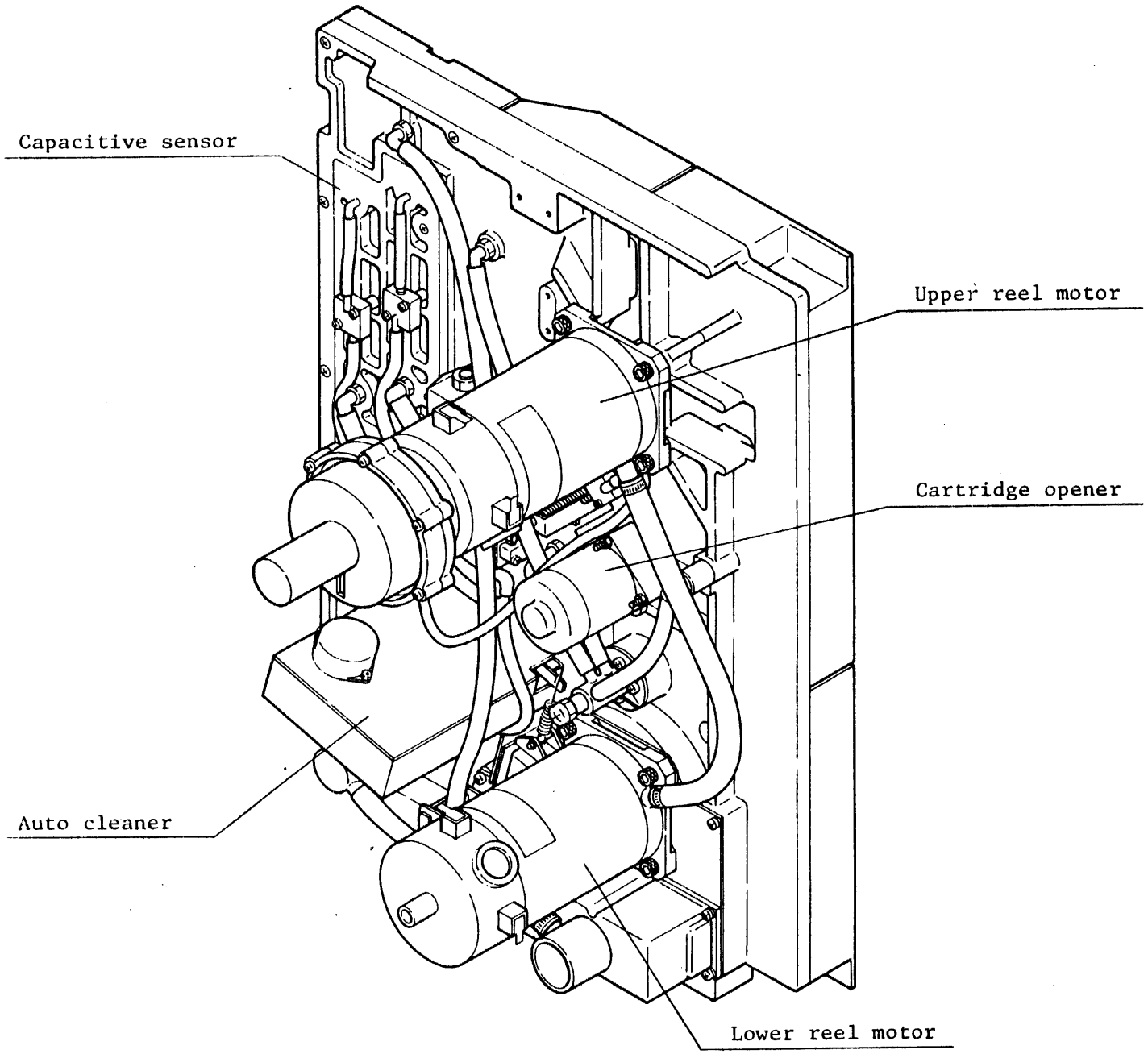


Figure 2-2. MTU rear view.

2.1.1 Tape Path

The MTU tape path, shown in Figure 2-3, is designed to minimize scratches on the coated surface of the tape and to increase system reliability. The tape coating surface touches only the magnetic head, tape cleaner, and cleaning ribbon. The base surface of the tape is guided by roller guides, shown in Figure 2-4, which reduce friction.

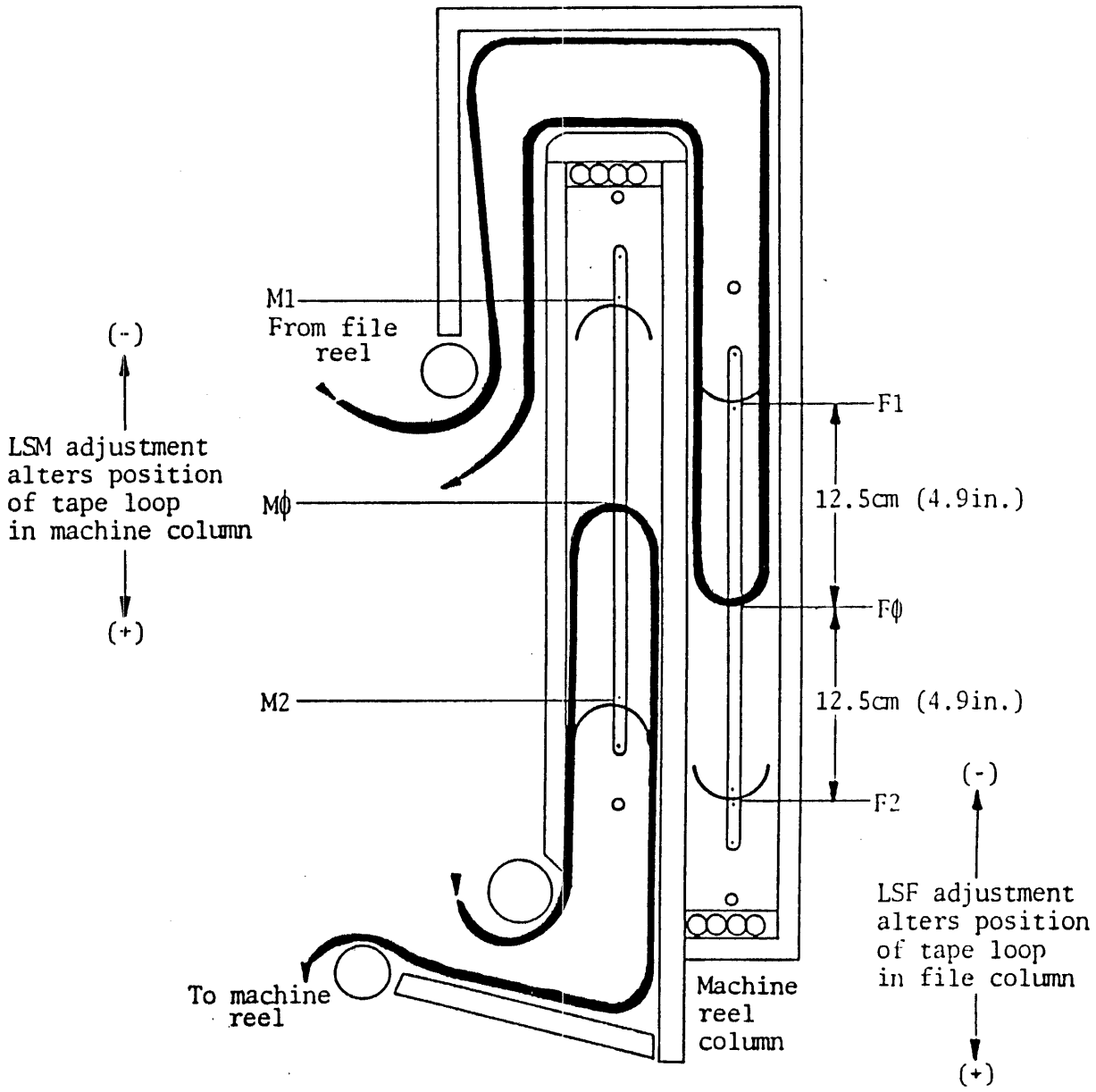


Figure 2-3. Tape path.

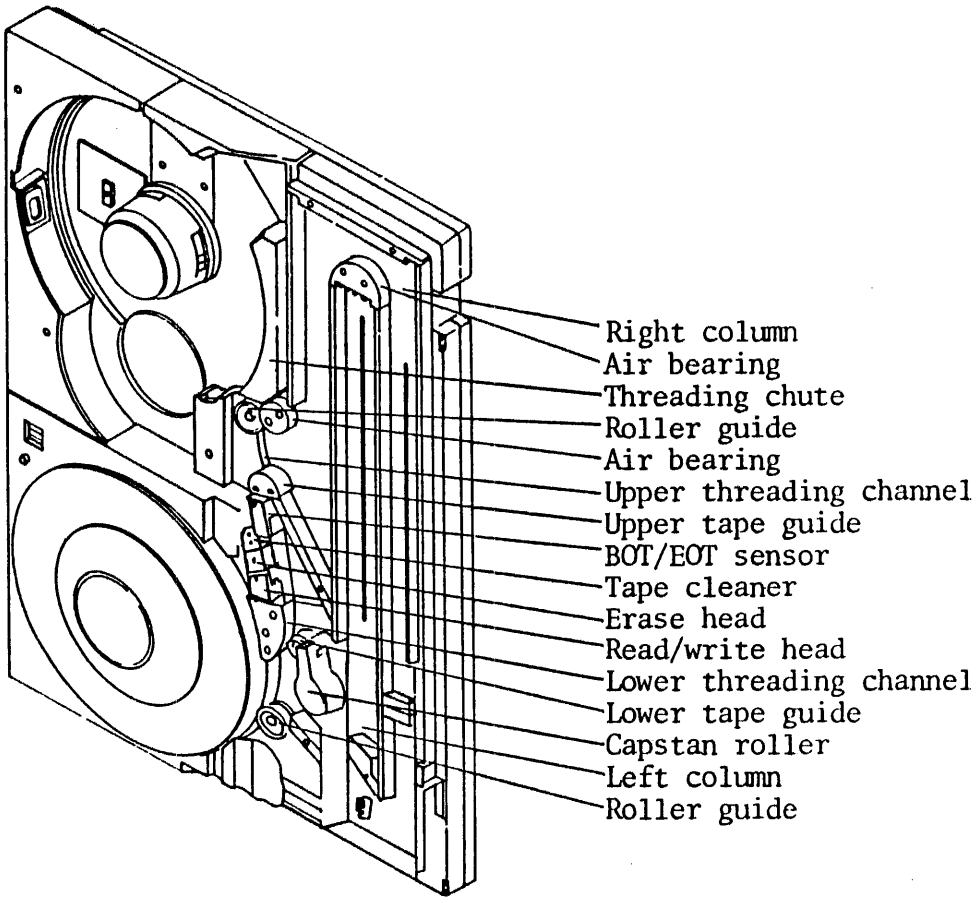
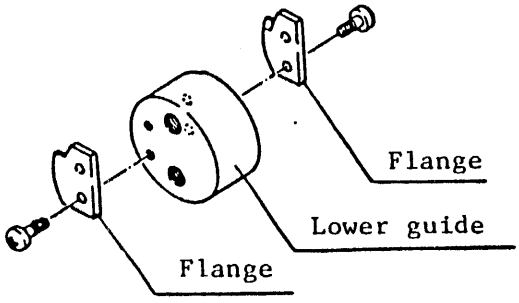


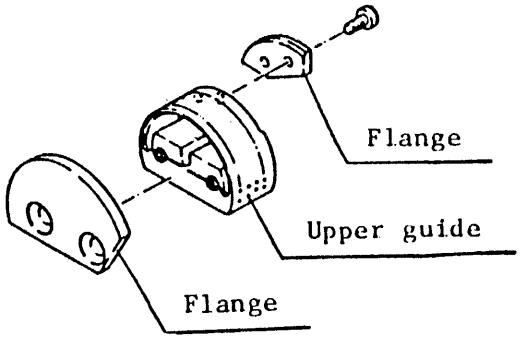
Figure 2-4. MTU components related to the tape path.

Tape guide

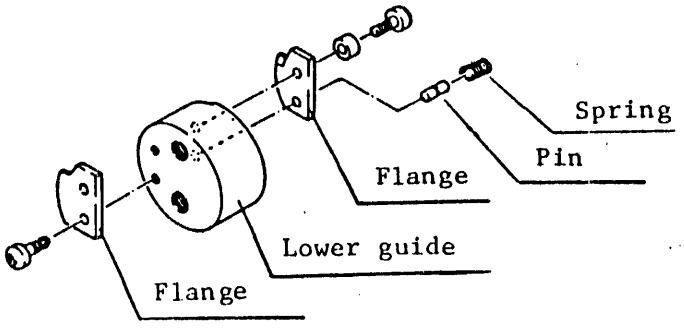
The upper and lower guides are located above and below the magnetic head. As shown in Figure 2-5, the fixed flanges are attached to both the front and rear sides of the upper guide, respectively. Both the fixed flanges are precisely positioned, and the tape runs between the flanges. The flange on the rear side of the lower guide is movable. The tape runs while being pressed by the movable flange in the front direction such that the standard edge of the tape always touches the fixed flange on the front side. Thus, the information track is protected from movement relative to the magnetic head.



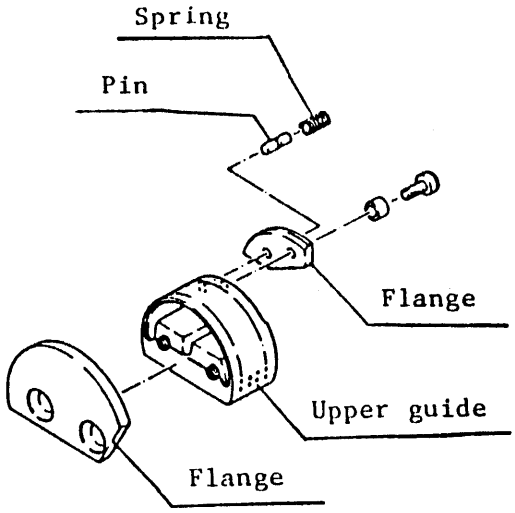
Lower guide (Fixed Flange)



Upper guide (Fixed flange)



Lower guide (Movable flange)



Upper guide (Movable flange)

Figure 2-5. Upper and lower guides.

Roller guide

Two kinds of large and small roller tape guides are used. The large roller tape guide, shown in Figure 2-6, is designed to reduce the friction of tape passing the file reel, the machine reel, and the entry to the column, and to reduce uneven winding.

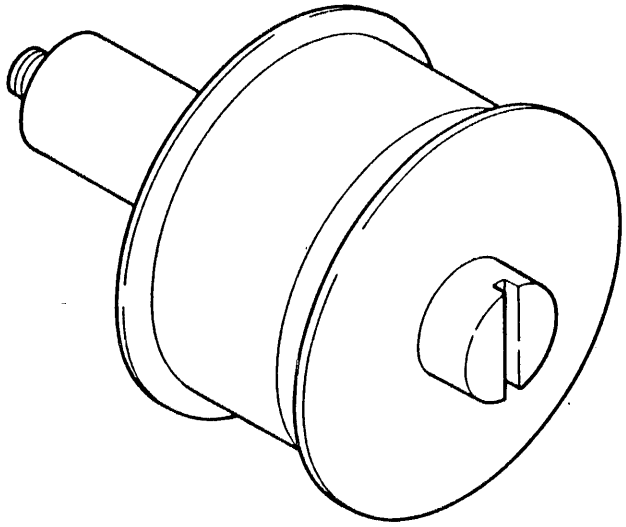


Figure 2-6. Roller guide.

Tape column

This is a buffer mechanism installed between the capstan and the machine and file reels. The capstan activates abrupt starts and stops repeatedly. The reel drive cannot follow the capstan's action due to their large inertia. An electrostatic capacitive sensor and air pressure are used to maintain and detect the position of the tape loop in the tape column.

2.1.2 Autoload mechanism

The autoload mechanism, shown in Figure 2-7, feeds the tape on the manually locked file reel to the machine reel via the upper and lower channels. The tape is wound five to six times on the machine reel and is then loaded into the tape columns.

The autoload mechanism consists of four main elements:

- o Restraint member
- o Cartridge opener
- o Cartridge sensor
- o Threading shoot.

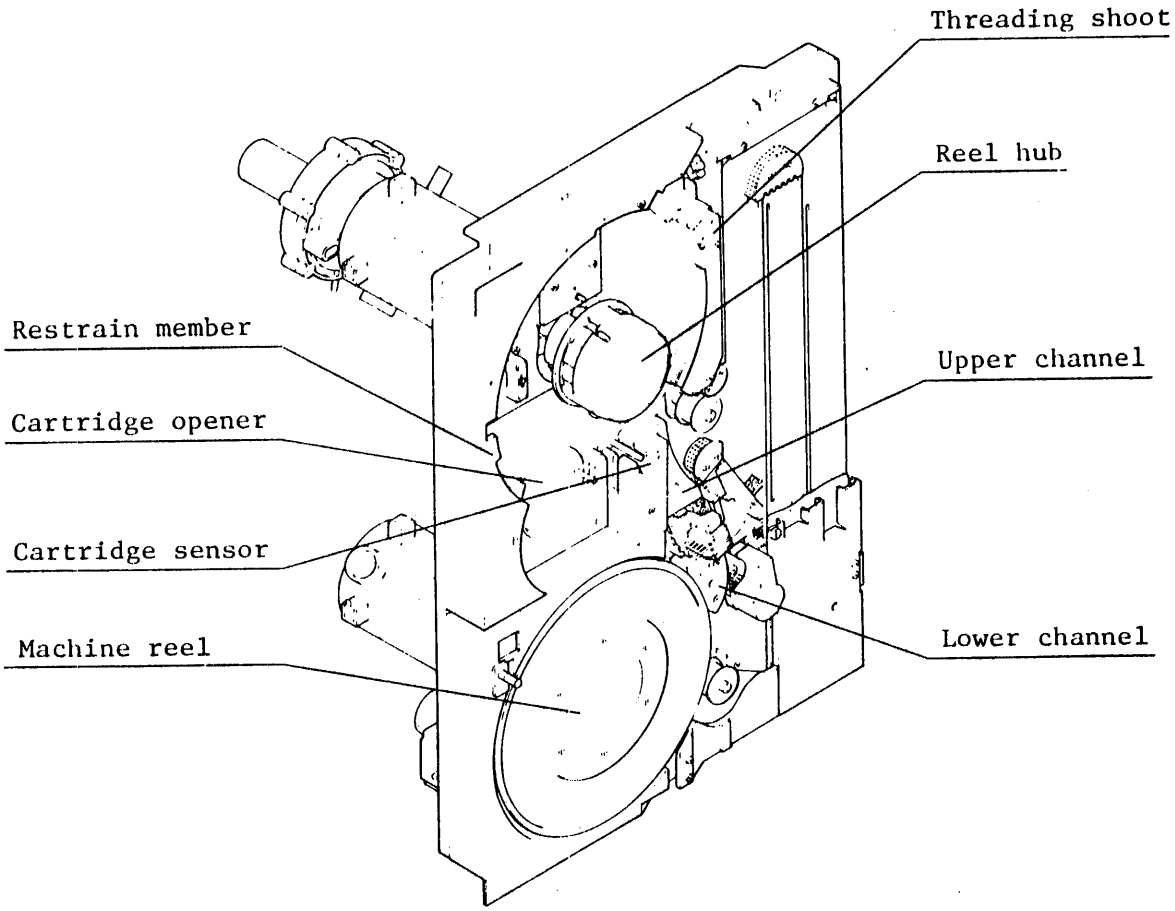


Figure 2-7. Autoload mechanism.

Restraint member

The restraint member, shown in Figure 2-8, is used during the autoload operation with a cartridge. It supports the cartridge and blows air inside the cartridge to cause the tape to more easily exit.

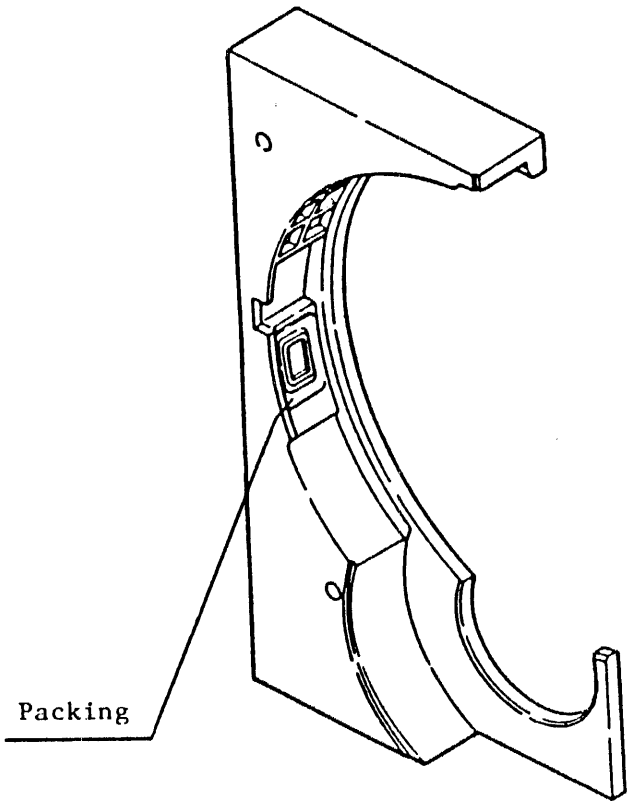


Figure 2-8. Restraint member.

Cartridge opener

The cartridge opener, shown in Figure 2-9, causes the tape cartridge to open and close. When a cartridge mounted tape is loaded, a pin is inserted into a hole in the cartridge open and close mechanism. The pin rotates causing the cartridge to open or close. the angle of opening and closing the cartridge is detected and determined by a cam and microswitch.

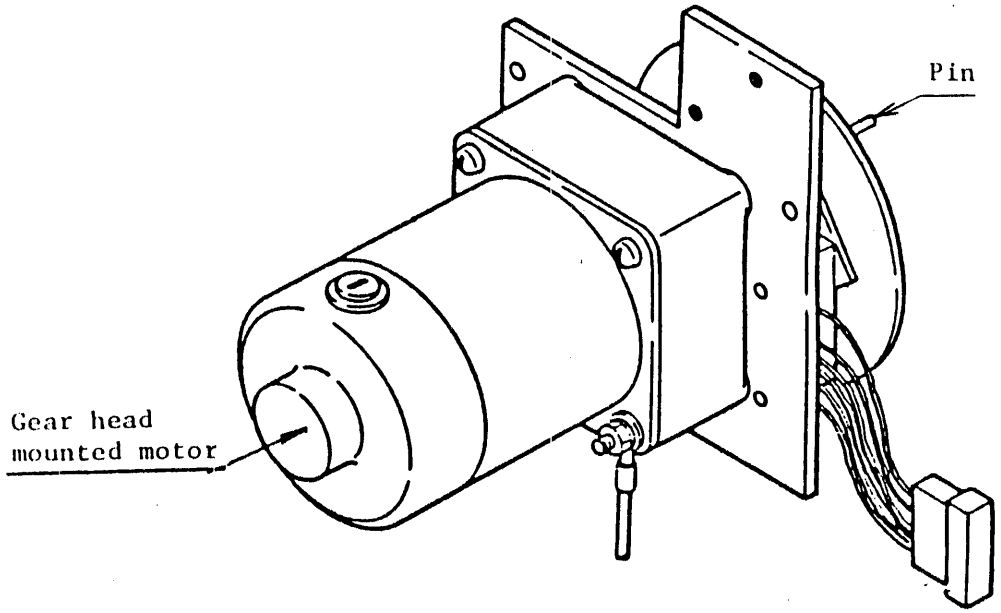


Figure 2-9. Cartridge opener.

Cartridge sensor

Because the autoload sequence depends on the presence or absence of a cartridge, a cartridge sensor, shown in Figure 2-10, is used. When a cartridge mounted reel is loaded, a push bar is depressed, and the microswitch is activated.

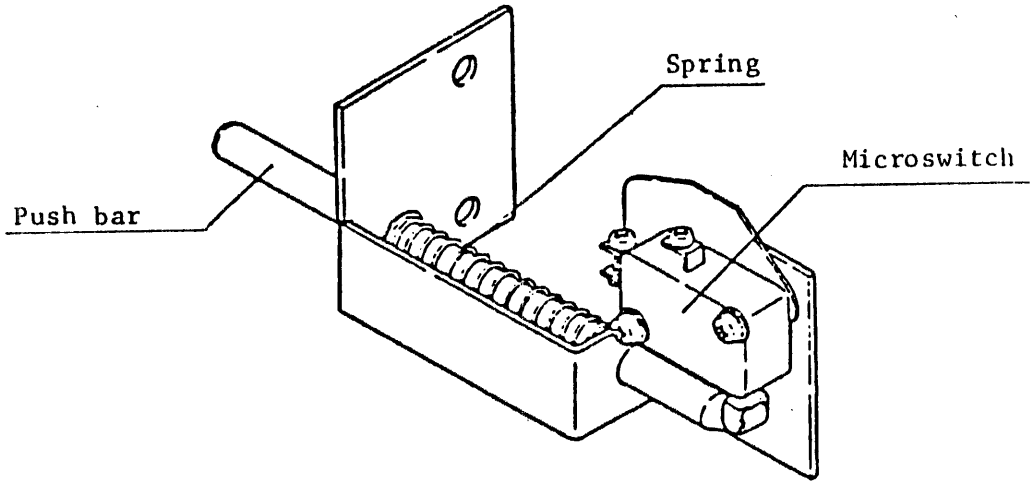


Figure 2-10. Cartridge sensor.

Threading chute

In the autoload mode using a reel installed in a cartridge, the threading chute in conjunction with the restraint member supports the cartridge. When no cartridge is used, the tape entry must be inserted in a grooved pad for threading to start autoloading. The air blown from the opening between the two plates of the threading chute and air blown from a channel (for peeling off the tape) make it possible to thread the tape smoothly.

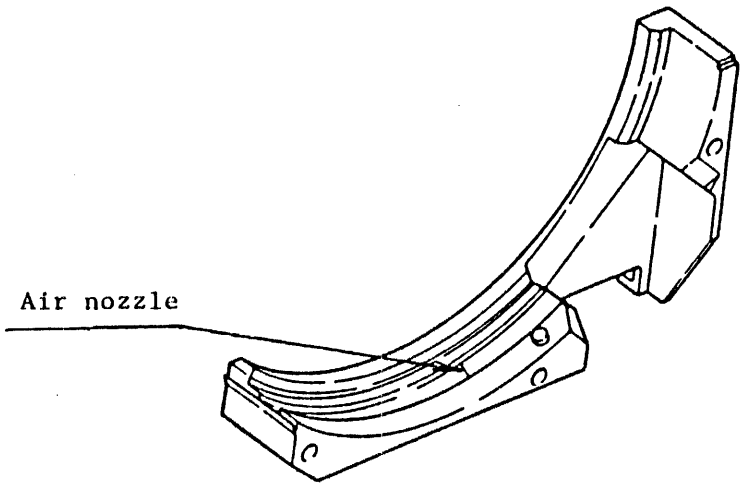


Figure 2-11. Threading chute.

Upper channel

The upper channel, shown in Figure 2-12, has three inclined slits to produce a stable air stream along the channel and to feed the tape. A mirror is attached to the bottom end of the upper channel through which the photosense block detects whether or not tape is present by the presence or absence of the light reflected from the mirror.

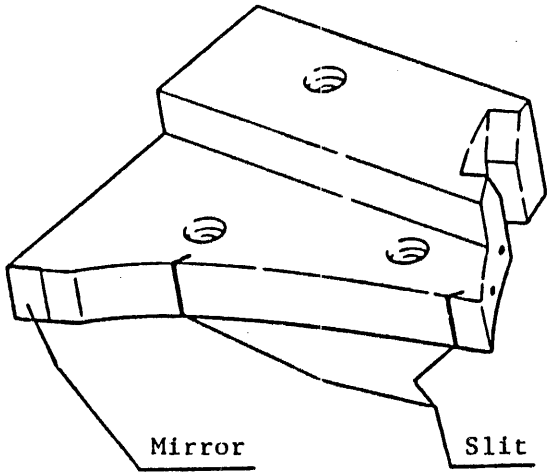


Figure 2-12. Upper channel.

Lower channel

Similar to the upper channel, the lower channel shown in Figure 2-13 blows air to feed the tape to the machine reel.

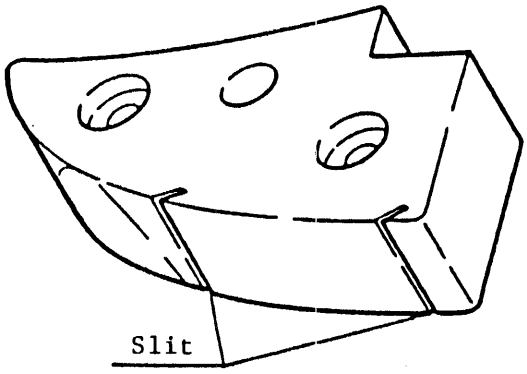


Figure 2-13. Lower channel.

Machine reel

The machine reel air inlets, shown in Figure 2-14, provides suction to assist in winding the tape onto the machine reel during autoloading. The air inlets are most effective from the bottom right position so that the inlet can effectively apply suction to the tape. A reflective marker is attached to the front plate of the machine reel. The low-tape sensor detects the rotation speed of the machine reel and the amount of tape remaining on the reel.

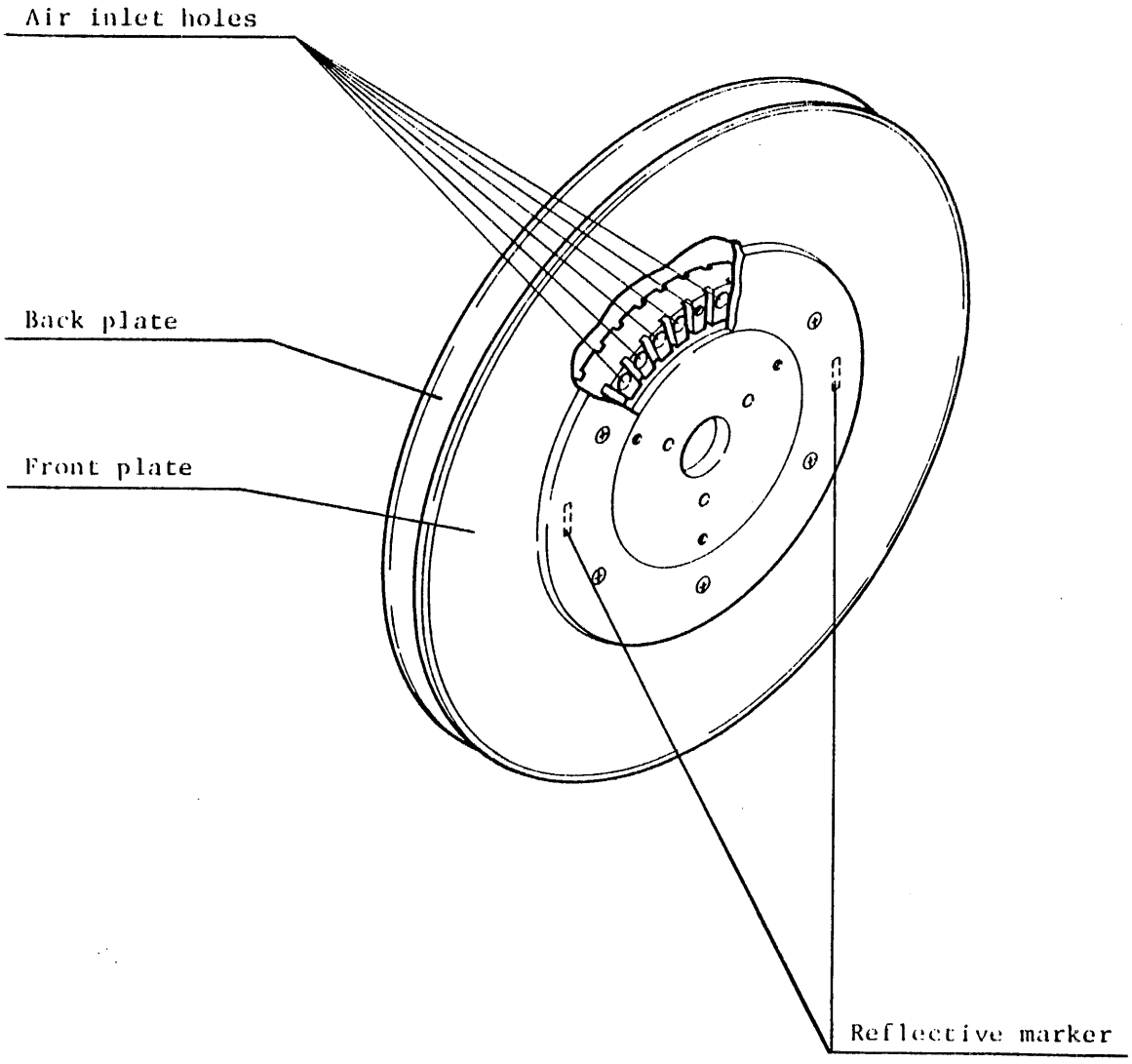


Figure 2-14. Machine reel.

2.1.3 Auto Hub

The Auto hub, shown in Figures 2-15 and 2-16, consists of three main sections:

(1) A section to convert pneumatic pressure into mechanical power. This section contains the diaphragm, piston, and front cover.

(2) A section to retain the reel that contains the reel boss, cam, roller, claw, and rubber tip.

(3) A wheel that holds the reel in its position and provides safety in case of a malfunction.

The diaphragm has a double-wall configuration. When air pressure is applied between the diaphragm and the front cover, the retainer ring moves, and the roller rises. As the roller rises, the claw enlarges; the reel is held in place by the friction of the rubber tip.

If the wheel is mounted, the reel is positioned properly when the reel is pressed inside. The wheel prevents the reel from being pushed out accidentally.

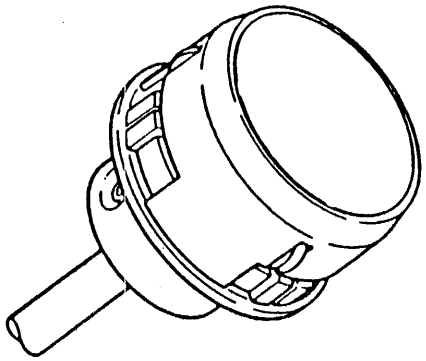


Figure 2-15. Auto hub.

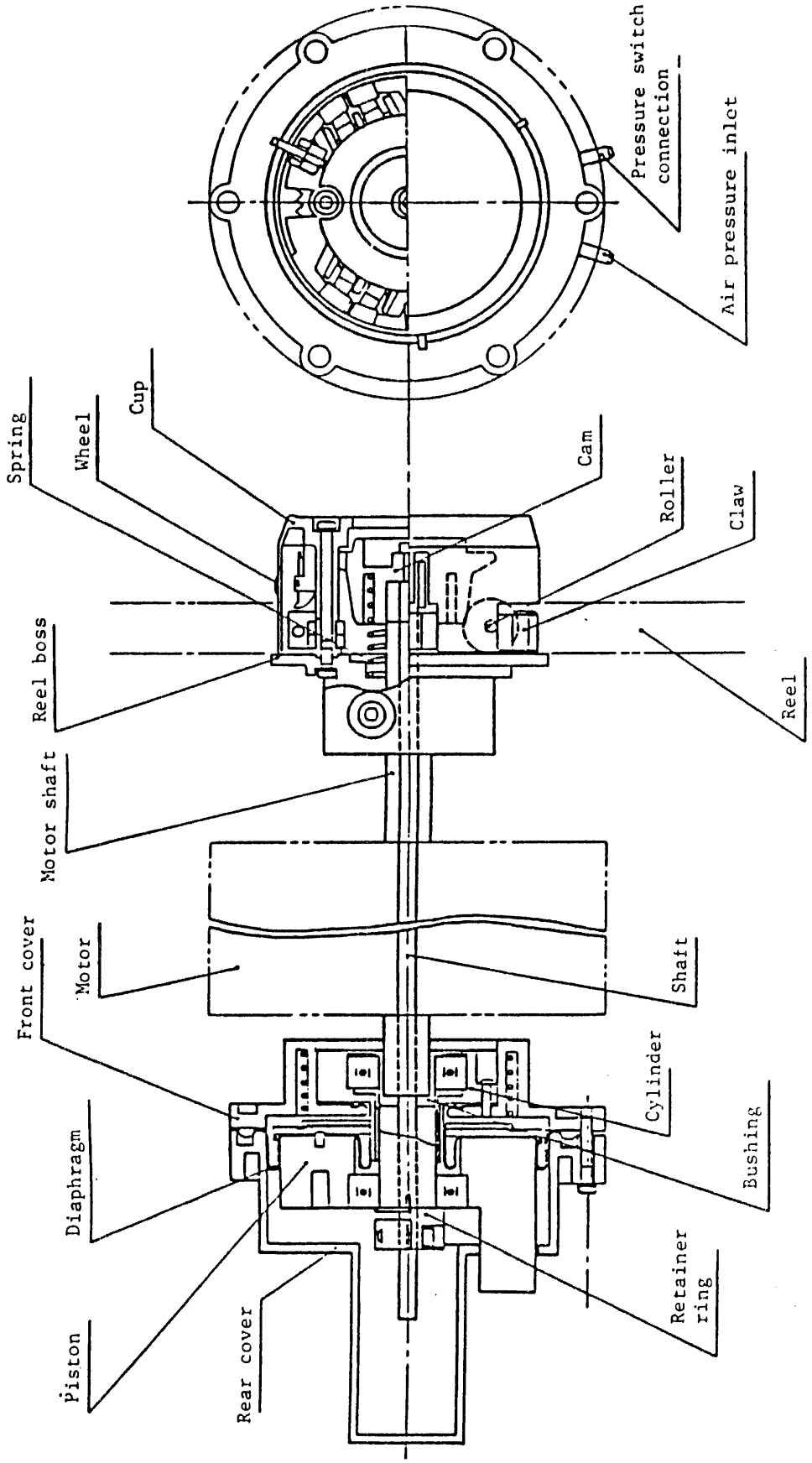


Figure 2-16. Auto hub.

2.1.4 Head Assembly

The head assembly, shown in Figure 2-17, consists of a magnetic read/write head, erase head, tape cleaner, and azimuth adjusting mechanism.

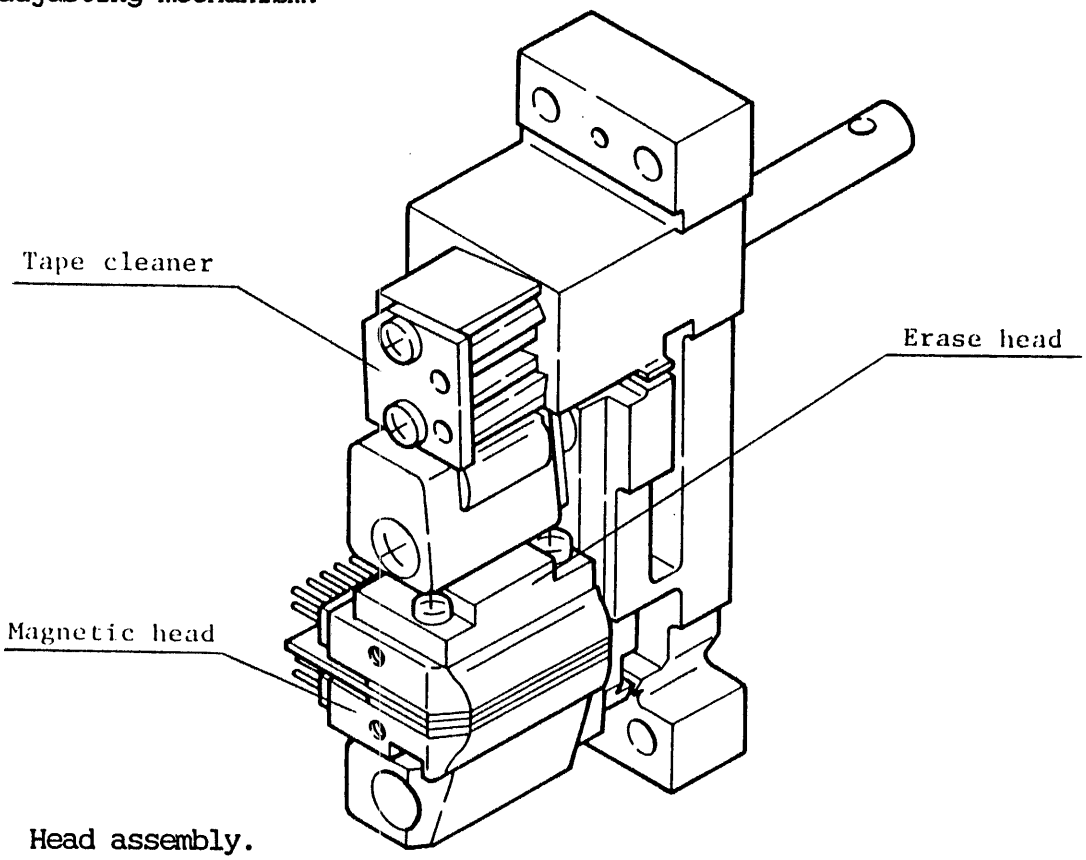


Figure 2-17. Head assembly.

Magnetic head

The magnetic head contacts the coating surface of the tape to perform data recording and regeneration.

Erase head

The erase head is located close to the coating surface of the tape (but does not touch the tape surface) to perform erase operations.

Tape cleaner

The tape cleaner is provided with a sharp edge to remove dust, foreign substances, and purple oxide adhering to the coating surface of the tape. All such materials are likely to cause the tape to drop data. The removed substances are blown off by the air stream from the cleaner edge.

Azimuth adjusting mechanism

The azimuth adjusting mechanism is shown in Figure 2-18. When rotating the azimuth adjusting screw, the deformation part shown in the figure deforms, and the magnetic head is inclined. This mechanism is used to adjust azimuth while observing tape skew.

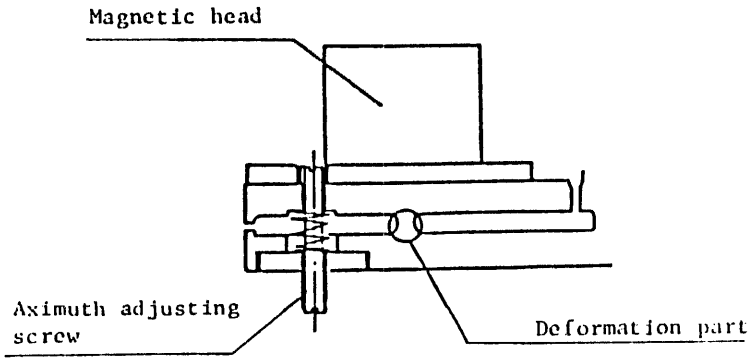


Figure 2-18. Azimuth adjusting mechanism.

2.1.5 Capstan

Capstan motor

Tape is fed by rotation of the capstan roller, shown in Figure 2-19. The roller is connected directly to the capstan motor and operates in forward or backward direction.

The capstan motor starts and stops abruptly since it uses a DC servo motor with low inertia. The surface of the capstan roller is lined with material having a high coefficient of friction to protect against tape slippage. The lining is extremely thin. Exercise care when servicing the capstan to avoid scratching or deforming the surface of the capstan roller.

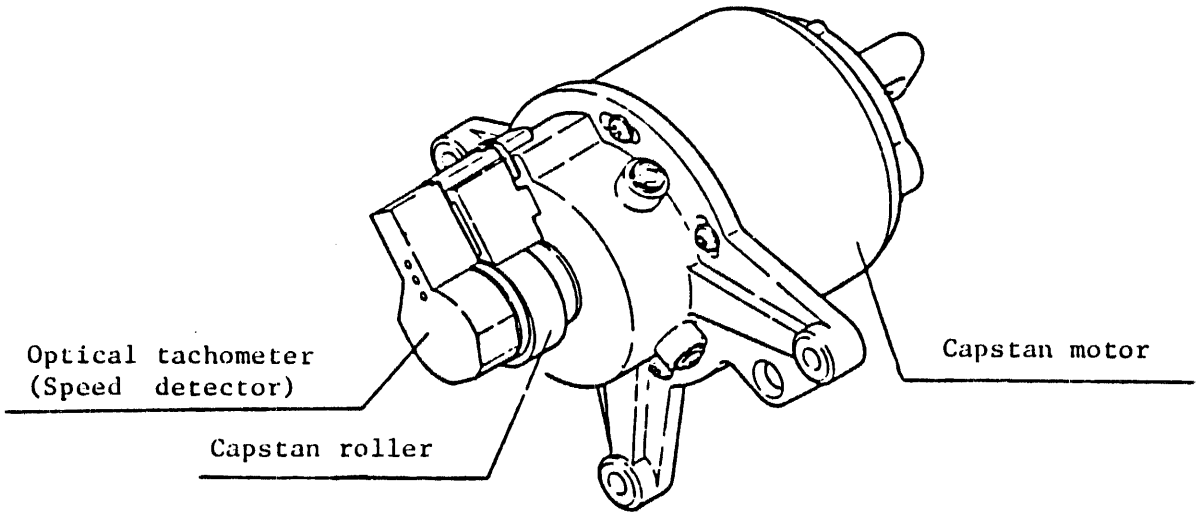


Figure 2-19. Capstan motor.

Detection of capstan rotation speed

An optical tachometer detects the capstan motor's speed of rotation. The 500 optical tachometer is provided with the code plate on which 500 slits are printed between an LED and a phototransistor, which has a mask for detection. The code plate is mounted on the capstan motor shaft.

The mask is concentric with the code plate and is mounted on the capstan motor. The rotating direction of the capstan motor is detected by the slits with a phase shift of 90^{o}.

2.1.6 File Protection Mechanism

A tape file is protected such that when the file reel has a write enable ring installed, the ring pin is inserted and pulled in by the air cylinder. The ring pin is separated from the enable ring. When the microswitch shown in Figure 2-20 detects the separation of the pin from the ring,a write-enable signal is issued.

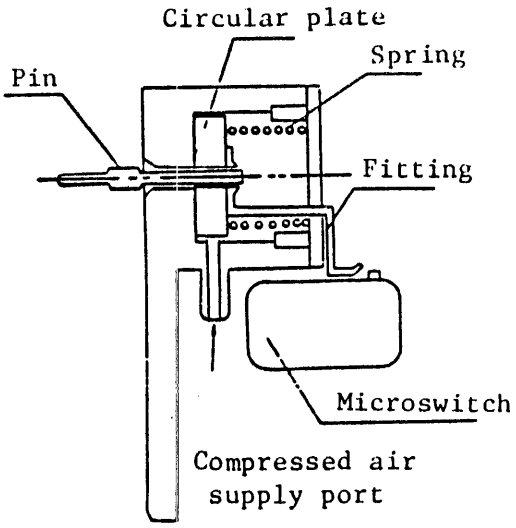


Figure 2-20. File-protection mechanism.

2.1.7 Photo Sense Block

The photo sense block shown in Figure 2-21 detects the beginning-of-tape (BOT) marker, the end-of-tape (EOT) marker, and the presence or absence of the reflection from the mirror mounted on the upper channel. The presence or absence of tape, the current tape position, the sequence of events, and the BOT and EOT are all detected by the photo sense block.

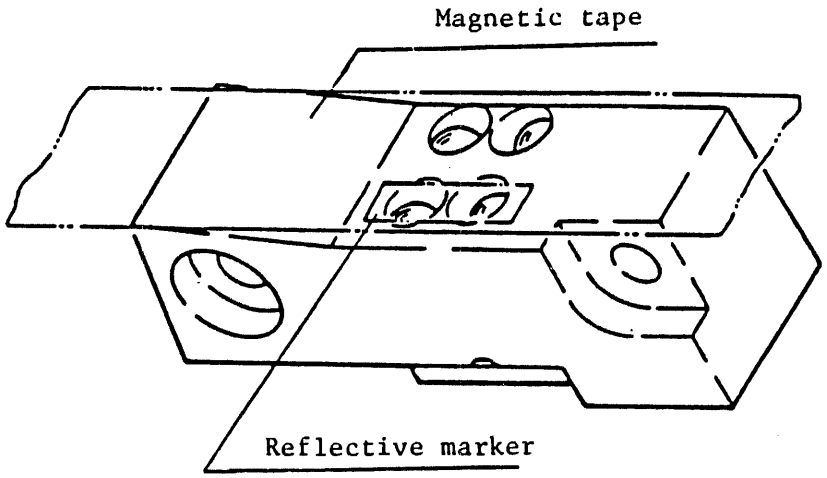


Figure 2-21. Photo sense block.

2.1.8 Low-Tape Sensor

Abrupt stoppage of tape being rewound at high speed is difficult even when the BOT is detected. Thus, the low-tape sensor shown in Figure 2-22 detects the amount of tape wound on the machine reel in advance. The tape speed is reduced when low tape is detected. The amount of tape wound on the machine reel is detected by reflected light from the reflective marker attached to the front plate of the machine reel. During autoloading, the detected frequency of reflected light from the reflective marker makes up the number of machine reel rotations. This allows timing for the column in action.

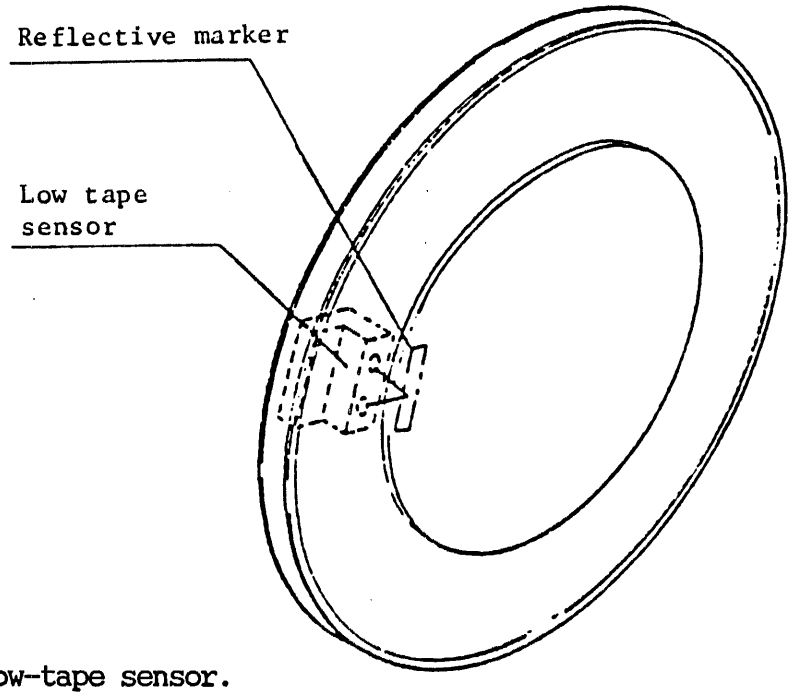


Figure 2-22. Low-tape sensor.

2.1.9 Autocleaner

The autocleaner shown in Figure 2-23 cleans dust adhering to the tape and protects the magnetic head from wear. The autocleaner cleans the tape coating surface by inserting a cleaning ribbon between the magnetic head and the magnetic tape during rewinding in normal speed. In addition, manual cleaning of the magnetic head, erase head, and tape cleaner a can be performed by manually inserting the autocleaner.

Slide assembly

The slide assembly that guides the cleaning ribbon is located below the right side of the magnetic head. It is activated by the solenoid and causes the cleaning ribbon to move under the write/read gap as shown in Figure 2-24. This cleaning ribbon cleans the magnetic head while preventing the magnetic tape from touching the magnetic head. When the solenoid is turned off, it is returned to its original position by releasing the spring.

Cleaning ribbon

The cleaning ribbon is activated when the slide assembly is in operation. Delivery rate is 2 to 5 mm/min. The cleaning ribbon is 50 m long.

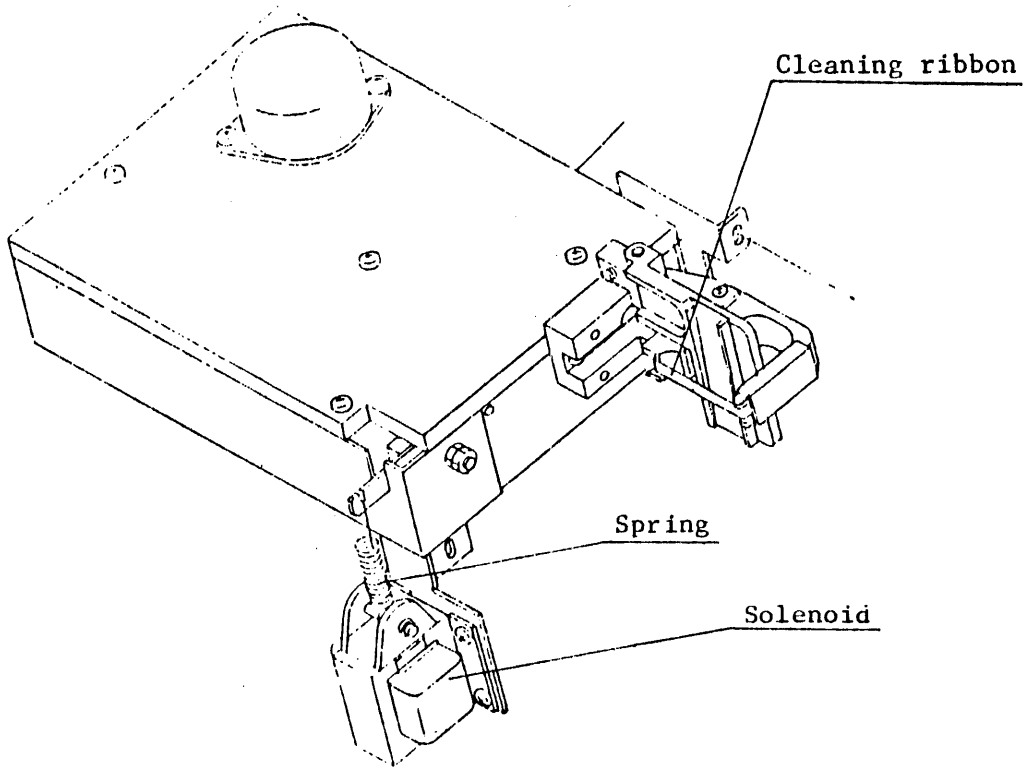
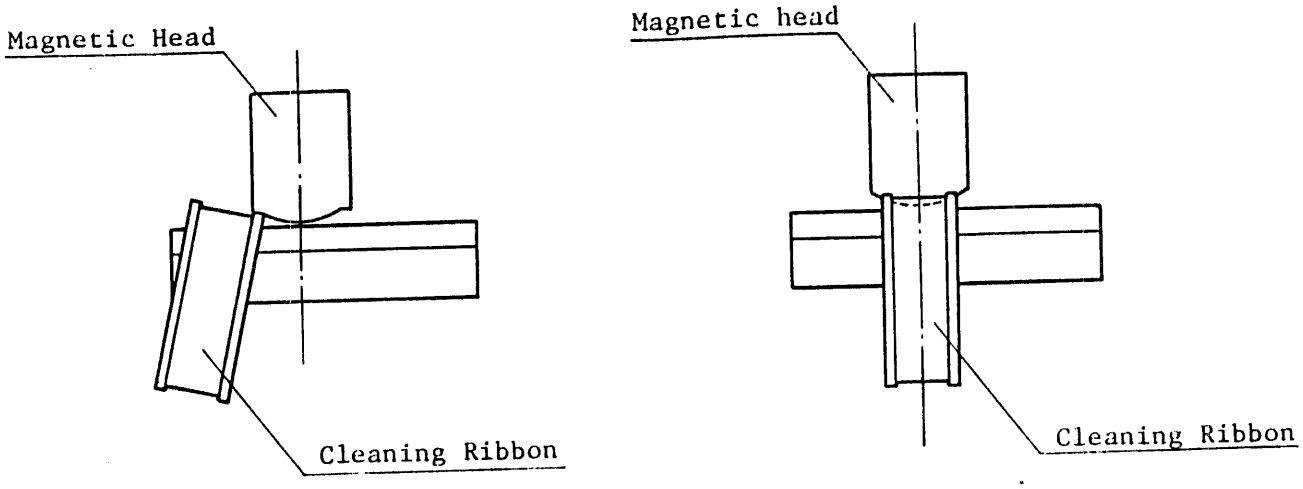


Figure 2-23. Autocleaner.



(a) Cleaning ribbon in the state when the solenoid is not in operation

(b) Cleaning ribbon in the state when the solenoid is in operation

Figure 2-24. Cleaning ribbon position.

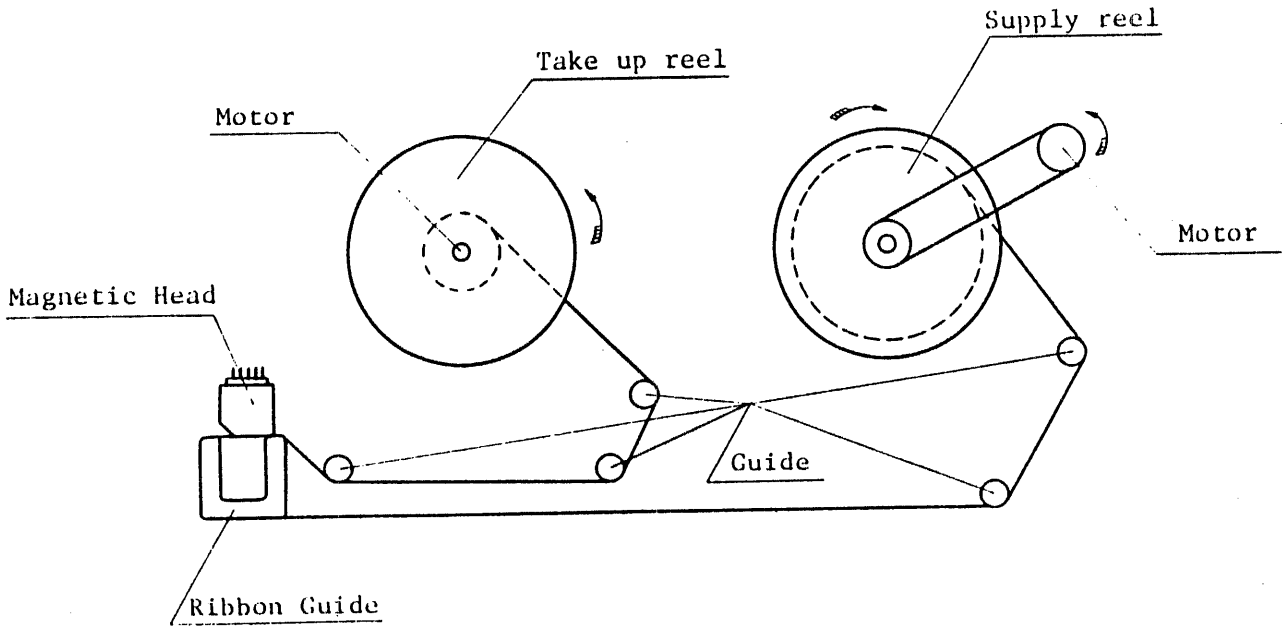


Figure 2-25. Autocleaner structure.

2.1.10 Error Marker

The error marker shown in Figure 2-26 places a mark on tape reels that produce frequent errors. The magnetic channel counts errors occurring during the write operation. If many errors occur, an appropriate signal is issued to the MTU. When receiving the signal, the MTU stamps a mark on the reel during unloading. The mark is made by a rubber stamp embedded in the solenoid axle when the solenoid operates.

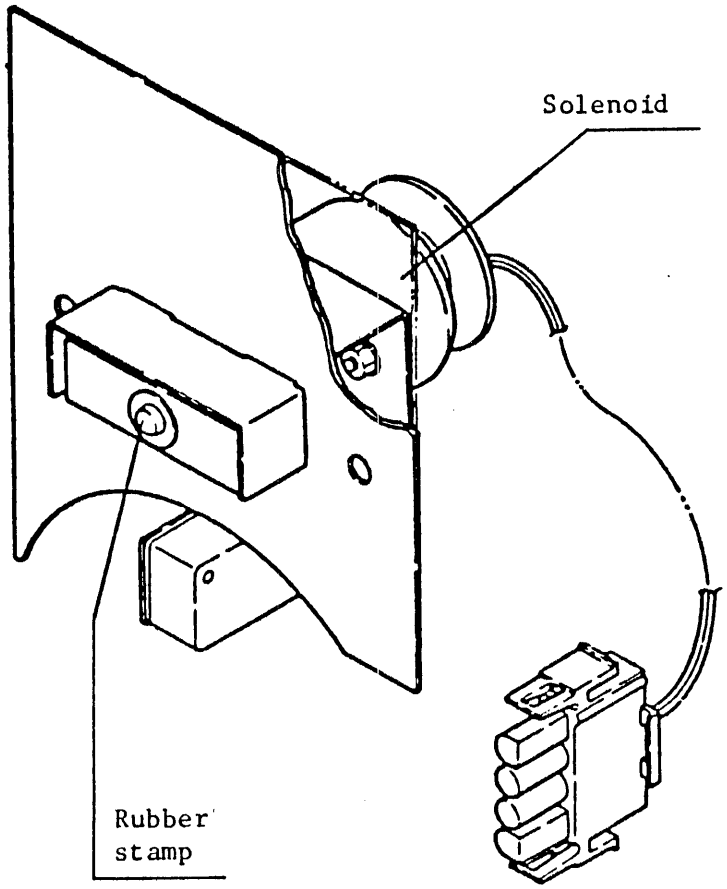


Figure 2-26. Error marker.

2.2 Air Supply System

The air supply system, shown in Figure 2-27 and 2-28, performs air pressure and vacuum operations for each section. Air pressure and vacuum are generated by suction and blowing of air by the motor driven blower. The locations to which air pressure and vacuum are supplied vary as a function of conditions of operation. Switching is executed by an electromagnetic valve.

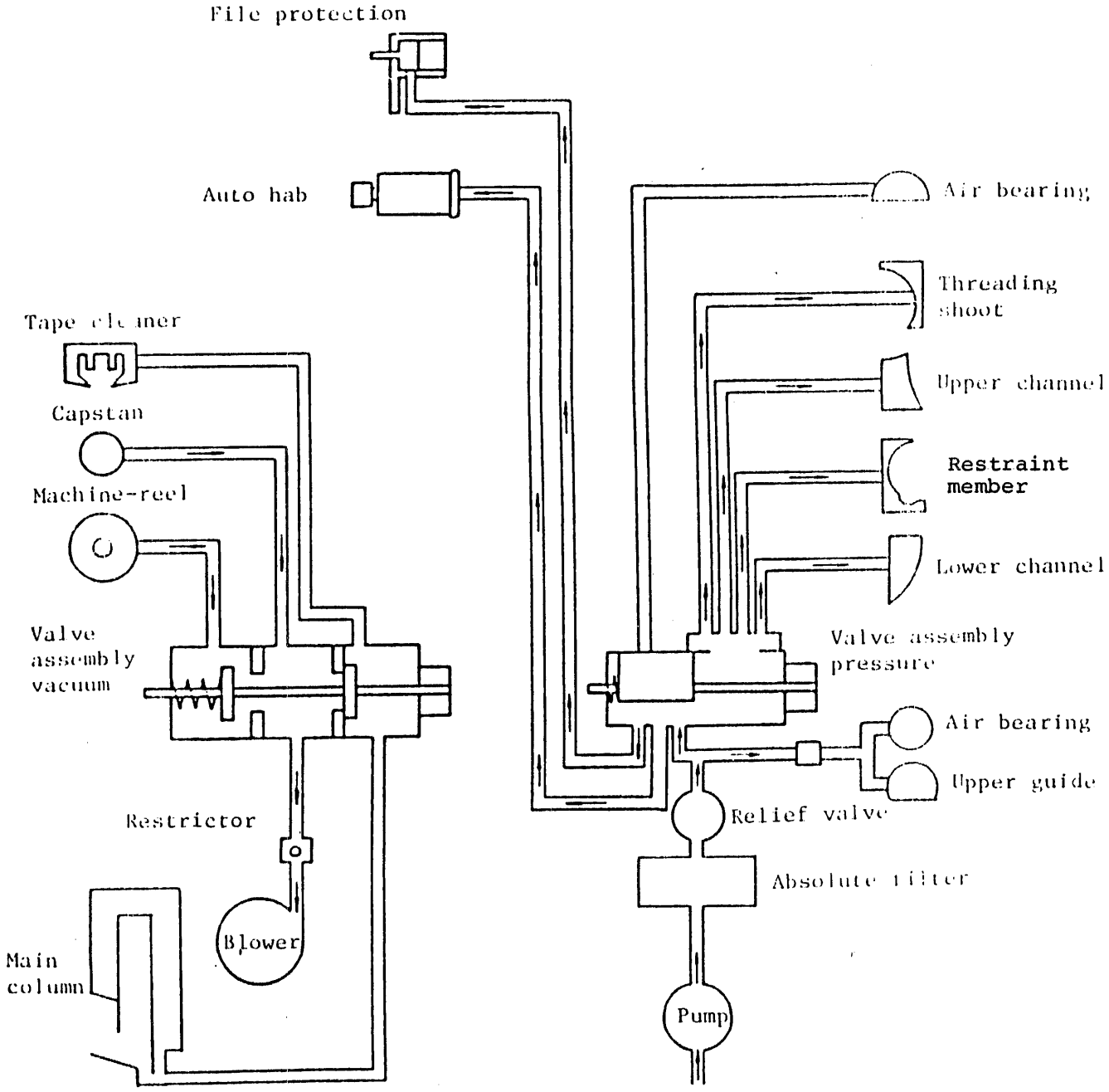


Figure 2-27. Air supply system during autoload operation.

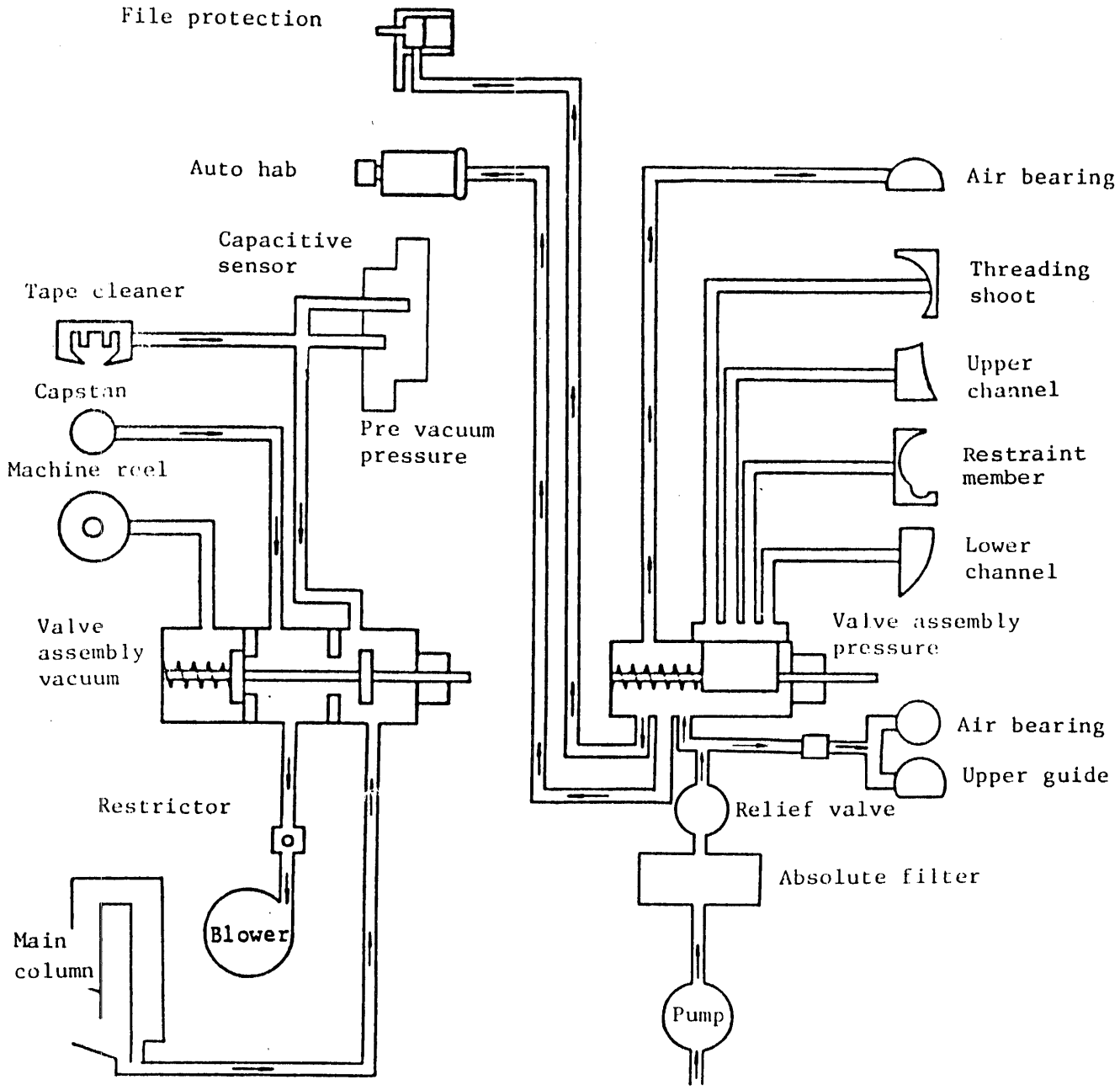


Figure 2-28. Air supply system during normal tape run.

CHAPTER 3 CIRCUIT OPERATION

3.1 Overall Circuit Configuration

Figure 3-1 shows the overall circuit configuration of the MTU. Power supply lines are omitted in this illustration because power is supplied to every section of the MTU.

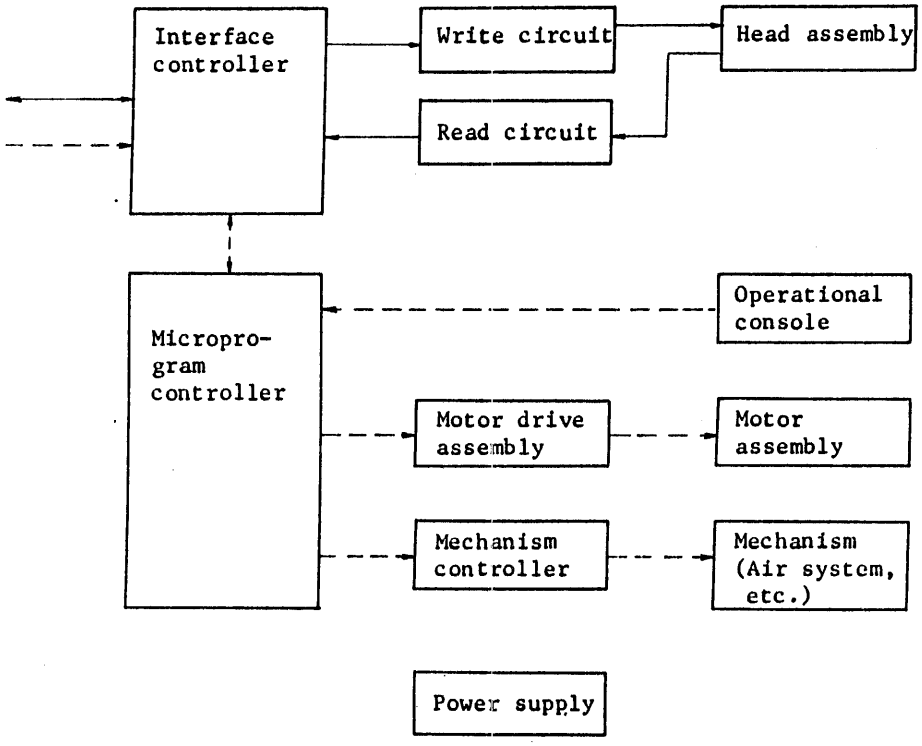


Figure 3-1. Circuit configuration of the MTU.

The overall system circuit consists of 11 main elements.

(1) The microprogram controller consists of the read-only memory (ROM), arithmetic logic unit (ALU), resistors, and bus control circuit.

(2) The interface controller is the interface circuit to the FMT that receives instructions from the FMT and sends and receives control signals to and from the microprogram controller.

(3) The write circuit is the circuit for writing data from the FMT on the tape with the write head. This circuit also supplies current to the erase head and to the automatic degauss of the write head.

(4) The read circuit amplifies the read signal from the read head, digitizes, and transmits the signal to the FMT. In the 6250 rpi (rows per inch) mode, the circuit that automatically adjusts the gain of the read amplifiers is included in the read circuit.

(5) The motor driving circuit consists of a current amplifying circuit to drive the capstan motor, the servo system circuit for the reel motor, a drive circuit for the window motor, and the cartridge motor.

(6) The mechanism controller consists of a driving circuit network for air supply, solenoid, and valve operations.

(7) The head assembly consists of the write head, read head, and erase head.

(8) The operator panel contains pushbutton switches and indication lamps (LED). This panel is described in more detail in Section 3.2.

(9) The motor section consists of the capstan motor, reel motor, window motor, and cartridge motor.

(10) The mechanism section consists of air supply units, a sensor mechanism, and the autoload mechanism.

(11) The power supply section includes the power supply for PCA operation, the power supply for mechanisms, and all remaining units requiring power.

3.2 Operator Panel

The operator panel consists of various switches necessary for MTU operation. Indication lamps (LED) show the condition of each operation. Figure 3-2 is an exterior view of the operator panel.

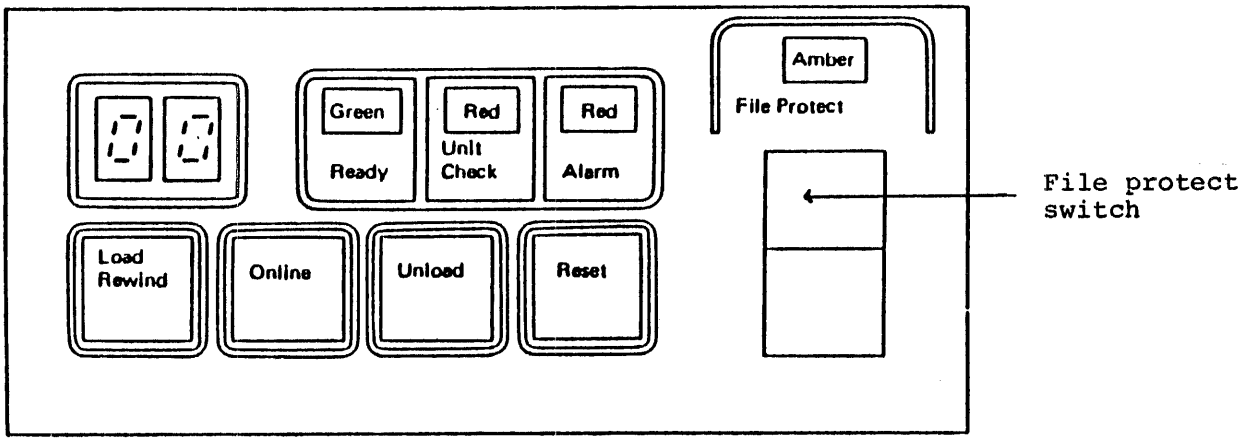


Figure 3-2. Exterior view of the operator panel.

(1) READY LED

When the MTU is in the ready state under control of the FMT, the green light of the Ready lamp goes on. During the rewind operation, data security erase (DSE) operation, space file and back space file operations, or tape load operation, this lamp will not be ON until the operation is completed.

(2) UNIT CHECK (LED)

When tape loading fails, the red Unit Check lamp flashes. If an abnormal state occurs at other times, this red lamp remains ON. When the RESET switch is depressed, this lamp turns off.

(3) ALARM (LED)

The Alarm lamp lights (red) when a fuse blows, when a circuit breaker shuts off, a power supply fails, or when an abnormal temperature rise is detected.

(4) LOAD/REWIND Switch

This switch is effective only in the offline state. To use the LOAD/REWIND switch, place the reel on the hub and install the tape on the file reel. Place the point of tape on the threading chute and depress this LOAD/REWIND switch. The tape reel is automatically locked, auto threading and tape loading are executed, and the tape runs until the BOT marker is detected (the window also automatically closes). When this switch is depressed while tape is in the loaded state, the tape is rewound at high speed until the BOT marker is detected.

To reload (also referred to as mid-load) tape that is only partly in the column due to some problem, such as electric stoppage, gently rotate the file reel to extract the stacked part of the tape until the tape becomes tense between the machine reel and the file reel. Press the LOAD/REWIND switch. The tape is automatically fed into the column and rewound until the BOT marker is detected.

(5) ONLINE Switch

Use the ONLINE switch to turn the MTU to the online state. Press the ONLINE switch to make the MTU available with the FMT.

(6) UNLOAD (switch)

This switch is effective only when the MTU is in the offline state. Use the UNLOAD switch to rewind loaded tape at high speed to BOT, to unlock the auto hub, and to open the window. when this switch is depressed and tape is completely rewound on the file reel, the window opens.

(7) RESET (Switch)

Depress the RESET switch to turn the MTU to the offline state and to reset the control line. The window is also closed by this switch. When the MTU fails in tape loading (the UNIT CHECK lamp flashes), depressing this switch releases the reel brake, thereby enabling the tape to be rewound manually. If the MTU fails during tape loading, the window opens automatically. If an abnormal state (with the UNIT CHECK lamp continuing to light), depressing this switch opens the window.

(8) FILE PROTECT LED and Switch

This lamp lights (amber) when the write-enable ring is removed from the file reel. When the switch is depressed, the file is protected from writing.

(9) Two-digit Indicator LED

This lamp indicates a two-digit code representing the condition of the power supply and an abnormal (error) condition of the MTU.

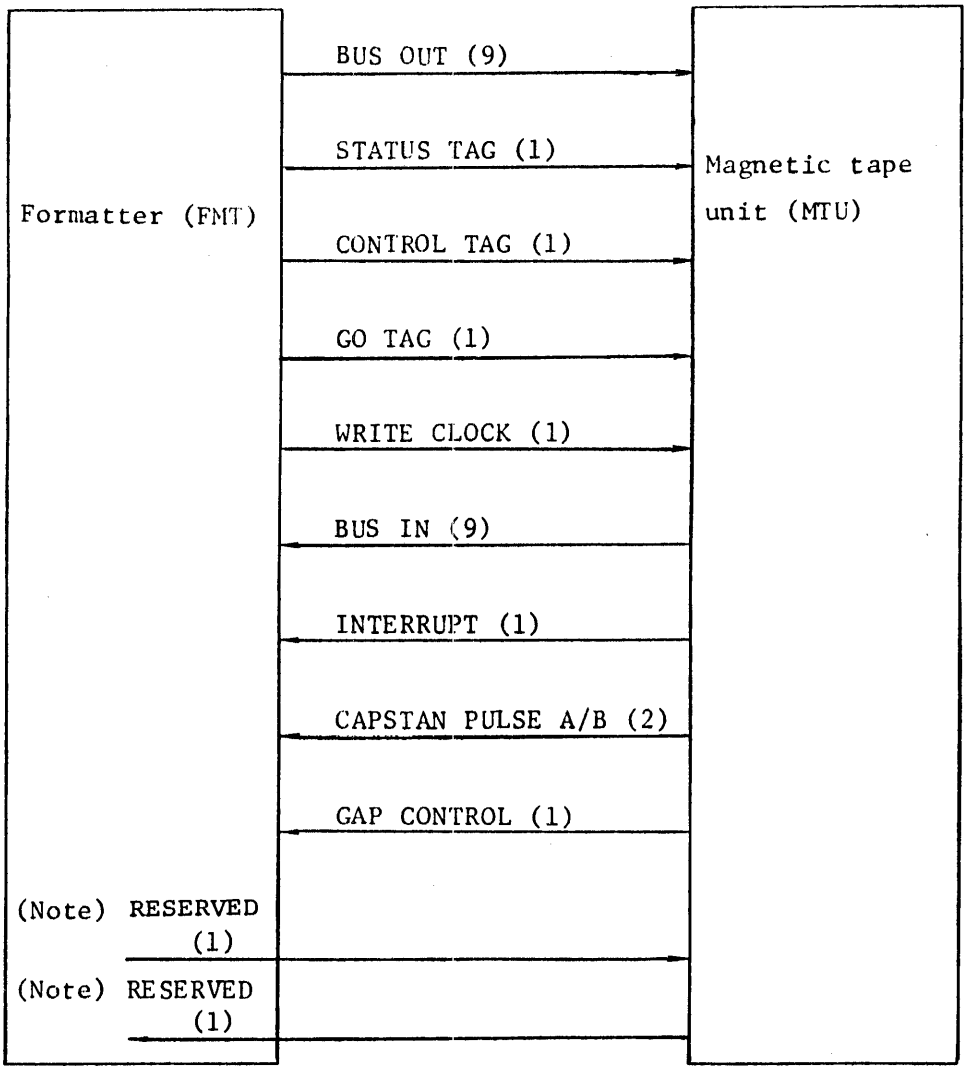
00 Represents no MTU errors (if the Unit Check lamp is off).

01 Indicates that an erroneous operation is occurring in the relevant unit, or displays the contents of an error. When either of these codes is indicated, the UNIT CHECK lamp flashes or remains ON.

3.3 FMT Interface

3.3.1 Connecting Cable

Each MTU is connected to the FMT through a single, flat cable. The address of each MTU is determined by the connection on the FMT distribution PCA. All 28 pairs of signals between the FMT an the MTU are digital. The signals between the FMT and the MTU are shown in Figure 3-3.



Note: The RESERVED signals are not used in the MTU. However, the MTU should be provided with a terminal resistance.

Figure 3-3. Signals between FMT and MTU.

3.3.2 Interface Signal Lines

(1) Data lines

These lines are used to transmit data from the FMT to the MTU. Data represents the status control command, encoded write data, and sense data. Data is discriminated by the tag signal.

Bus In through 8

These lines transmit data from the MTU to the FMT. The data represents status byte data, control byte data, command byte data, read data from the tape, loop write-to-read return data, and the sense data. Data is discriminated by the tag line.

(2) Tag line

Tag control is shown in Tables 3-1 and 3-2.

Table 3-1. Contents of tag control.

TAG / BUS OUT/IN BIT	BUS OUT				BUS IN			
	STATUS	CONTROL	COMMAND (Status Control "1")	GO	STATUS	CONTROL	COMMAND (Status Control "1")	GO
0	Set Erase	Level Test 0		WD0/RDL0	ERS	Level Test 0		RD0
1	Set Read Forward	" 1	See the following table	WD1/RDL1	FWD	" 1	See the following table	RD1
2	Set Read Backward	" 2		WD2/RDL2	BWD	" 2		RD2
3	Set Write Status	Set Test Mode		WD3/RDL3	Write Status	Test Mode		RD3
4	Reset	Set Error Marker		WD4/RDL4	TU Check	EMK		RD4
5	Set 6250 & SAGC or Set NRZI	Set Data Security Erase		WD5/RDL5	SAGC ON	DSE		RD5
6	Set 1600	Set Rewind		WD6/RDL6	1600	REW		RD6
7	Set LWR	Set Unload		WD7/RDL7	LWR TUIF	UNL		RD7
8	Parity	Parity	Parity	WD8/RDL8	TAG IN	TAG IN	TAG IN	RD8

Table 3-2. Contents of the command tag.

Bus Out		Command
0123	4567	
0	0	
0	1	
0	2	Set Streaming Mode
0	3	Reset Streaming Mode
0	4	Space File
0	5	Back Space File
0	6	
0	7	
0	8	Set LWR RW
0	9	Reset LWR RW
0	A	Set Low Slice
0	B	Reset Low Slice
0	C	
0	D	
0	E	
0	F	

	Content of BUS IN	
BUS OUT / BUS IN	0 / 0 1 2 3	Character "X" may be any digit / 4 5 6 7
0	STRMF (Streaming Feature)	
1	SKIPF (Skip File Feature)	
2		
3	LWSL (Low Slice)	
4	STRMD (Streaming Mode)	
5	LWR RW	
6	HACT (Action)	
7	RDY (Ready)	
8	TAG IN	

Bus Out		Communication Registers
Address 0 1 2 3	Contents of 4 5 6 7	
1 0 0 0	0 through F	Reg. 0 Upper 4 bits
1 0 0 1	0 through F	Reg. 0 Lower 4 bits
1 0 1 0	0 through F	Reg. 1 Upper 4 bits
1 0 1 1	0 through F	Reg. 1 Lower 4 bits
1 1 0 0	0 through F	Reg. 2 Upper 4 bits
1 1 0 1	0 through F	Reg. 2 Lower 4 bits
1 1 1 0	0 through F	Reg. 3 Upper 4 bits
1 1 1 1	0 through F	Reg. 3 Lower 4 bits

BUS OUT / BUS IN	0 to 3 8 or 9	4 to 7 "X"	0 to 3 A or B	4 to 7 "X"	0 to 3 C or D	4 to 7 "X"	0 to 3 E or F	4 to 7 "X"
0 1 2 3 4 5 6 7	Reg. 0		Reg. 1		Reg. 2		Reg. 3	
8	TAG IN							

Status Tag

a. This signal causes the FMT to call the status information from the MTU or sets the status operation.

b. To implement status call, set Status Tag to "1". The Write Clock must not be set to "1".

c. To implement status set to the MTU, the FMT sets a predetermined control item to "1" on the Bus Out line and sets both the Status Tag and the Write Clock to "1".

d. When GO Tag is "1", the Tape Unit (TU) Sense Byte 8 is issued to Bus In when Status Tag is set to "1".

e. When Status Tag, in conjunction with Control Tag, is set to "1", it acts as a Command Tag.

Control Tag

f. This signal causes the FMT to call the control information from the MTU or to set control operation.

g. To call the control information, set Control Tag to "1", but do not set Write Clock to "1".

h. To set Control to the MTU, the FMT sets a predetermined control item to "1" on the Bus Out line and sets both the Control Tag and the Write Clock to "1".

i. When the Control Tag, in conjunction with the Status Tag, is set to "1", it acts as a Command Tag.

Command Tag

a. When both the Status Tag and the Command Tag are "1", the MTU regards them as a Command Tag.

b. This signal causes the FMT to call the command information from the MTU or to set command operation.

c. To call the command information, set the Command Tag to "1". The Write Clock must not be set to "1".

d. To issue a command to the MTU, the FMT sets a predetermined control item to "1" on the Bus Out line and sets both the Command Tag and the Write Clock to "1".

Go Tag

a. This signal causes the FMT to direct the MTU to set the tape drive for the read or write operation.

b. If the MTU is already in the Write Status when this signal is "1", the Bus Out line provides the write information to the tape, and the "Write Clock" is used together.

c. If the MTU is already in the Read Status when this signal is "1", this signal becomes control information to switch the threshold level of the read circuit in the MTU to zero.

d. If the MTU is already in the Read Status when the Go Tag signal is "1", the Bus In line becomes data from the tape.

(3) Write Clock

a. When the Status Tag, the Control Tag, or the Command Tag, in conjunction with the Write Clock, is set to "1", the contents of the Bus Out are stored.

b. To call the Status information, the command information, the Sense information, and the Write Clock are not needed.

c. When the MTU is in the Write Status and the Go Tag is "1" the MTU implements sampling of the data on the Bus Out line at the rise of Write Clock.

(4) Interrupt

This signal is set to "1" when the MTU causes the following conditions in offline operation:

a. When file protect occurs during the forward action in the write or erase operation.

b. When the condition that causes the Unit Check to be "1" occurs within the MTU.

c. When the Ready or the Online is set to "0" during the write or read operation (Go Tag - "1").

d. When ONLINE is set to "0" during Rewind or DSE operation.

e. When the BOT is detected during the Read backward operation (when the Go Tag is issued from the MTU).

f. When the Test Mode FF in the MTU is "1" and the EOT is detected during Write or Read operation.

g. When the Self-Adjust Gain Control (SAGC) Check occurs during the SAGC operation.

h. When BOT is detected in the back-space file.

i. When the 20-m check is detected in the space file.

(5) Capstan pulse A/B

a. This signal provides information about tape-drive speed detected optically from the code disk connected directly to the capstan.

b. When the capstan rotates in the forward direction, pulse A is in a phase delay relative to pulse B. When rotating in the backward direction, the phase relation between pulse A and pulse B is reversed.

(6) Gap Control

a. This is the block-access start signal that the FMT receives from the MTU after the FMT sets the Go Tag to "1" during the read/write operation.

b. The MTU starts counting capstan pulses when the Go Tag is set to "0" in the immediately preceding read/write operation. The number of capstan pulses are counted since the beginning of the present operation when the Go Tag was set to "1". The MTU sets the Gap Control signal to "1" at the time that the amount of tape length fed by capstan rotation reaches a predetermined length of Inter-Block Gap (IBG).

3.3.3 Tag Line Control

(1) The meaning of the Bus Out bit in the Status Tag is as follows:

a. Bit 0 Set Erase

When this bit is "1", the MTU is set to the erase status.

b. Bit 1 Set Read Forward

When this bit is "1" and both bits 2 and 3 are "0", the MTU sets the write status to "0" (Read Status) and changes to the FWD status.

c. Bit 2 Set Read Backward

When this bit is "1" and both bits 2 and 3 are "0", the MTU sets the write status to "0" (Read Status) and changes to the BWD status.

d. Bit 3 Set Write Status

When this bit is "1" and both bits 2 and 3 are "0", the MTU is set to the write status.

e. Bit 4 Reset

When this bit is "1", the following signal in the MTU is set to "0".

- TU check (Status Tag bit 4)
- Interrupt
- Ready hold (TU Sense Byte 3 bit 2)
- Overrun (TU Sense Byte 8 bit 5)
- Tape Mark (TU Sense Byte 8 bit 7)
- Test Mode (Control Tag bit 3)
- LWR (Status Tag bit 7)
- LWR2 (Command Tag bit 5)
- TU Sense Byte 2

f. Bit 5 Set 6250 and SAGC or Set NRZI

- For the MTU in the GCR/PE mode. This means that the MTU is set in the 6250 rpi and SAGC mode.

- For the MTU in the PE/NRZI mode. This means that the MTU is set in the 800 rpi NRZI mode.

g. Bit 6 Set 1600

When this bit is "1" and bit 5 is "0", the MTU is operated in the 1500 rpi mode.

h. Bit 7 Set LWR TUIF (Loop-Write-to-Read TU interface)

This bit sets the MTU in the LWR TUIF mode. The MTU is set in the loop mode, and the output on the BO line is input to the BI line without changing the wave shape, where the MTU is set in the loop mode when the GO TAG signal is "1".

(2) The meaning of the Bus Out bits in the Control Tag is as follows:

a. Bits 0 through 2 Level Test 0 through 2

The combination of bits 0 through 2 determines the slice level as shown in Table 3-3.

Table 3-3. Slice level of each mode.

Application	Level Test 0 1 2	READ FWD	READ BWD	WRITE FWD	Mode
Diagnosis	1 1 1	125 ± 12%			GCR/PE
	1 1 0	100 ± 12%			
	1 0 1	80 ± 8%			
	1 0 0	64 ± 8%			
	0 1 1	51 ± 5%			
	0 1 0	41 ± 5%			
Marginal	0 0 1	15±2%	10±1% 15±2% (AGC step is greater than C)	37±4% (AGC step is greater than C)	
Normal	0 0 0	10±1%	7±1% 10±1% (AGC step is greater than C)	20±2% 25±2% (AGC step is greater than C)	
Marginal	x x 1	26±4%		50±5%	NRZI
Normal	x x 0	17±2%		40±5%	

b. Bit 3 Set Test Mode

When this bit is "1", the MTU is set in the Test Mode.

c. Bit 4 Set Error Marker (EMK)

This bit specifies the action to print character (E) on the back of a file reel.

d. Bit 5 Set Data Security Erase (DSE)

When the MTU is in the write status, this bit initiates the data security erase action of the MTU. The MTU carries out the erase action until the EOT marker is detected. During the erase action, READY (Sense byte 0 bit 7) is in the "0" state. When the EOT marker is detected and the erase action is completed, the DSE status is set to OFF and READY returns to "1".

e. Bit 6 Set Rewind (REW)

This bit specifies high-speed rewinding until the BOT marker is detected. After the rewind action starts, the FMT need not intervene until the rewind action is completed. During the rewind action, the READY state is "0", the Online status is kept as "1", and the MTU is in the busy condition. At the completion of the rewind action, the READY state is recovered.

f. Bit 7 Set Unload (UNL)

This bit specifies the unload action. When the unload action starts, both the Online status and the READY are set to "0". These are not automatically returned to "1" even when the unload action is completed. When the unload action is completed, the tape is wound entirely on the file reel, resulting in servo-off, reel lock release, and window open.

(3) The meaning of Bus Out in the Command Tag (both the Status Tag and the Control Tag are "1") is as follows:

a. Code 02 Set Streaming Mode

This command sets the MTU in the streaming mode.

b. Code 03 Reset Streaming Mode

This command resets the streaming mode.

c. Code 04 Space File

This command makes the MTU set the READY signal to "0" and moves the loaded tape in the forward direction until the Tape Mark (TM) block is detected.

d. Code 05 Backspace File

This command makes the MTU set the READY signal to "0" and moves the loaded tape in the backward direction until the TM block is detected.

e. Code 08 Set Loop-Write-to Read RW

This command causes the MTU to loop the write data onto the read data lines. The LWR RW is made to return. The write data is returned via the analog circuit following the pre-amplifier circuit. The LWR is the same shape as the write data, while the wave shape of the LWR RW is similar to that of the data read by the read head.

f. Code 09 Reset Loop-Write-to Read RW

This command resets the LWR RW mode.

g. Code 0A Set Low Slice

This command sets the slice level to the MTU to the low level (7%). This command is effective only for the erase instruction.

h. Code 0B Reset Low Slice

This command returns the slice level to the normal level.

i. Set Communication Registers

This command sets or resets the registers by using 4 lower bits of the Bus Out and specifying greater than 8 for its upper bits. A 4-byre register can be set or reset in units of 4 bits.

(4) The definition of the Bus in bit in the Status Tag is as follows:

a. Bit 0 ERS

When the MTU is in the erase status, this bit is "1".

b. Bit 1 FWD

When the forward status is determined, this bit is set to "1".

c. Bit 2 BWD

When the backward status is determined, this bit is set to "1".

d. Bit 3 Write Status

When the MTU is in the write status, this bit is set to "1".

e. Bit 4 Tape Unit (TU) Check

When this bit is "1", it indicates that an abnormal condition is occurring in the MTU.

f. Bit 5 Self-Adjust Gain Control (SAGC)

This bit is set to "1" when Set 6250 and SAGC or Set NRZI is specified while the MTU in the 6250/1600 rpi mode does not detect the BOT.

g. Bit 6 1600

When the MTU is operated in the 1600 rpi mode this bit is "1".

h. Bit 7 LWR TUIF

When this bit is "1" , the MTU is set in the Loop-to-Read Through the TU Interface mode.

i. Bit 8 TAG IN

When the contents of the Bus Out bits 0 through 8 represent an odd number, this bit is set to "1".

(5) The meaning of the Bus In bit in the Control Tag is as follows:

a. Bit 0 through 2 Level Test 0 through 2

These bits indicate that the MTU is set to the slice level.

b. Bit 3 Test mode

The MTU is in the Test mode when this bit is "1".

c. Bit 4 EMK

This signal is set to "1" by the Set EMK signal from the MTU.

d. Bit 5 Data Security Erase (DSE)

When the MTU operates in the forward direction and in the write status, it executes the data security erase using the Set DSE from the FMT. The MTU carries out the erase action until the EOT marker is detected. When the erase action is completed, the DSE status is set to "0", and the ready signal is returned to "1". During the erase operation, the MTU is busy.

e. Bit 6 REW

This bit is set to "1" by the Set REW from the FMT when the ready signal is set to "0". During the rewind operation, the ready signal is "0" and the MTU is busy.

f. Bit 7 UNL

This bit is set to "1" by Set UNL; Online and Ready are set to "0". This bit is reset when the unload operation is completed or suspended.

g. Bit 8 TAG IN

This bit is set to "1" when the contents of Bus Out 0 through 8 represent an odd number.

(6) The meaning of the Bus Out in the Command Tag (both the Status Tag and the Control Tag are "1") is as follows:

a. Bit 0 (when the upper digit of the Bus Out is "0".)
STRMF (Streaming Feature)

If the relevant MTU has the streaming function, this bit is "1".

b. Bit 1 (when the upper bit of Bus Out is "0".)
SKIPF (Skip File Feature)

If the relevant MTU has the space file and backspace file functions, this bit is "1".

c. Bit 2 (when the upper bit of Bus Out is "0".)

This bit is always "0".

d. Bit 3 (when the upper bit of Bus Out is "0".)
LWSL (Low Slice)

When the Low Slice is specified for the relevant MTU, this bit is "1".

e. Bit 4 (when the upper bit of Bus Out is "0".)
STRMD (Streaming mode)

When the MTU is set in the streaming mode, this bit is "1".

f. Bit 5 (when the upper bit of Bus Out is "0".)
LWR RW (Loop-Write-to-Read Through Read/Write Circuit)

When the LWR RW is specified for the relevant MTU, this bit is "1".

g. Bit 6 (when the upper bit of Bus Out is "0".)
HACT (Action)

This bit is "1" during actual functioning of the MTU.

h. Bit 7 (when the upper bit of Bus Out is "0".)
RDY (Ready)

This bit indicates that the MTU is ready to execute the instruction from the FMT for carrying out tape action.

i. Register 0 through 3 (when the upper digits of the Bus Out are 8 through F.)

This bit represents the contents of the communication register set by the FMT.

j. Bit 8 TAG IN

This bit is "1" when contents of the Bus Out 0 through 8 is an odd number.

(7) The Bus Out/ Bus In line in the Go Tag

When the Go Tag is set to "1", the Bus Out line has the following meanings:

a. If the MTU is in the READ status and is to carry out the read action in a recording mode other than the NRZI mode, the read threshold level is specified without the presence of the write clock. The MTU if effective for both the FWD and the BWD operations.

b. If the MTU is in the Write status and neither LWR TUIF nor LWR RW is set, the MTU outputs the write data on magnetic tape with the presence of the write clock.

c. When the MTU is set in the LWR (Loop Write-to-Read) TUIF or LWR RW, the MTU outputs the turnaround data to the Bus In line.

d. When the GO Tag is "1", the TU Sense Byte 8 is output to the Bus In line if the status is set to "1".

e. In case of items (a) and (b) above, the data output on to the Bus In line is the read data from the loaded magnetic tape. In case of item (c) above, the Bus Out loop data of LWR TUIF or LWR RW, and the content of the TU Sense Byte 8 is output.

(8) Sense Byte

When all Tag lines are "0" or both Go Tag and the Status Tag are "1", the Bus In line indicates the particular sense information. Table 3-4 shows the contents of the sense information.

Table 3-4. Contents of the MTU Sense Byte Bus In

TU Sense Byte	0	1	2	3	4	5	6	7	8
Bus Out Bit / Bus In Bit	7, 8, all "0"	6	5	4	3	2	1	0	* 3&5 or GO & STS TAG
0	BWD	EXT IF	MISC Error	MTU Model 0	Tape Unit Unique ID Low Order 2^7	SAGC Count 0	Read Data 0	Error Code 0	UERS (Unit Erase Current ON)
1	Not FP	Reset Key	Tape Loop Alarm Left	MTU Model 1	" 2^6	" 1	" 1	" 1	UACT (Unit Action)
2	TWA	DSE	Tape Loop Alarm Right	Ready Hold	" 2^5	" 2	" 2	" 2	UBWD (Unit Backward)
3	BOT	7 Track	ROM parity Error	Tape Unit Unique ID High Order 2^{12}	" 2^4	" 3	" 3	" 3	UWCON (Unit Write Current ON)
4	Write Status	Test Mode	Write Circuit Alarm	" 2^{11}	" 2^3	EC Level 2^3	" 4	" 4	U64S (Unit 64% Slice)
5	Online	Dual Density	Not Use	" 2^{10}	" 2^2	" 2^2	" 5	" 5	UOVRN (Unit Over Run 20 m Check)
6	TU Check	High Density	Air Alarm	" 2^9	" 2^1	" 2^1	" 6	" 6	UPE (Unit PE Mode)
7	Ready	6250	Load Failure	" 2^8	" 2^0	" 2^0	" 7	" 7	TM (Tape Mark)
8	TAG IN	TAG IN	TAG IN	TAG IN	TAG IN	TAG IN	" 8	TAG IN	TAG IN

a. Sense Byte 0

1) Bit 0 Backward (BWD)
This bit is "1" when the MTU is in the backward status.

2) Bit 1 No File Protect (FP)
This bit is "1" when the MTU is not file protected.

3) Bit 2 Tape Warning Area (TWA)
When the current tape position is in the Tape Warning Area (that is, when the EOT is detected in the forward direction), this bit is set to "1". When EOT is detected in the backward direction, this bit is set to "0".

4) Bit 3 Beginning of Tape (BOT)
This bit is "1" when the BOT marker has been detected.

5) Bit 4 Write Status
This bit is "1" when the MTU is in the Write Status.

6) Bit 5 Online
This bit is set to "1" when the MTU meets online requirements and the Online Switch is depressed.

7) Bit 6 Tape Unit Check
This bit is "1" when a malfunction of the MTU occurs.

8) Bit 7 Ready
This bit indicates that the MTU is ready to execute the instruction for tape operation.

9) Bit 8 TAG IN
Of the Bus Out bits 0 through 8, only bits 7 or 8 indicate "1".

b. Sense Byte 1

1) Bit 0 Extended Interface (EXTIF)
This bit indicates "1" if the MTU is provided with the streaming function or the skip-file function.

2) Bit 1 Reset Key
This bit is "0" when the reset key on the operator panel is depressed or the door is manually opened.

3) Bit 2 Data Security Erase (DSE)
This bit is "1" while the MTU is executing the data security erase.

4) Bit 3 Not Used.
This bit is always "0".

5) Bit 4 Test Mode
This bit is "1" when the MTC specifies the Online and Set Test mode for the MTU.

6) Bit 5 Dual Density Feature
This bit is "1" if the MTU is of two different recording density types: either 6250/1600 rpi or 1600/800 rpi.

7) Bit 6 High Density Mode
This bit is "1" when the MTU is set in the high recording density mode.

8) Bit 7 6250 Feature
This bit is "1" when the MTU is set in the 6250/1600 rpi mode.

9) Bit 8 TAG IN
Of the Bus Out bits 0 through 8, only bit 6 is "1".

c. Sense Byte 2

1) Bit 0 MISC Error (miscellaneous Error)
This bit is set to "1" when the MTU detects an error occurring somewhere other than the bits in Sense Byte 2.

2) Bit 1 Tape Loop Alarm Left
This bit is set to "1" when the running tape enters the warning area in the left column.

3) Bit 2 Tape Loops Alarm Right
This bit is set to "1" when the running tape enters the warning area in the right column.

4) Bit 3 ROM Parity Error
This bit is set to "1" when a parity error takes place in the PROM of the MTU.

5) Bit 4 Write Circuit Alarm
This bit is set to "1" when an abnormal condition occurs in the write circuit system.

6) Bit 5 Not Used
This bit is always "0".

7) Bit 6 Air Bearing Alarm
This bit is set to "1" when abnormal pressure is detected.

8) Bit 7 Load Failure
This bit is set to "1" when the MTU fails in autoloading.

8) Bit 8 TAG IN
Of the Bus Out bits 0 through 8, bit 5 indicates "1".

d. Sense Byte 3

1) Bits 0,1 MTU Models 0, 1
The bits 0 and 1 specify the following models:

Bit 0	Bit 1	Model
0	0	125 ips
0	1	50 ips
1	0	200 ips
1	1	75 ips

2) Bit 2 Ready Hold
This bit is set to "1" when the MTU changes its status from Not Ready to Ready.

3) Bit 3 (2^{12}) through bit 7(2^{8})
This bit indicates the Tape Unit Unique ID High Order.

4) Bit 8 TAG IN
Of the Bus Out bits 0 through 8, only bit 4 indicates "1".

e. Sense Byte 4

1) Bits 0 (2^{7}) through 7 (2^{0}) indicate the Tape Unit Unique ID Low Order.

2) Bit 8 TAG IN
Of the Bus Out bits 0 through 8, only bit 3 indicates "1".

f. Sense Byte 5

1) The bits 0 through 3 indicate the maximum value of the SAGC count.

2) The bits 4 (2^{3}) through 7 (2^{0}) indicate an EC level.

3) Bit 8 TAG IN
Of the Bus Out bit 0 through 8, only bit 2 indicates "1".

g. Sense Byte 6

When the Bus Out bit 1 is set to "1" after the Go TAG is reset, the MTU sends out the Read data to the Bus In. bits 0 through 8 of the Bus In represent the Read data.

h. Sense Byte 7

1) Bits 0 through 7 indicate an error code
Error code 00 indicates that the power supply condition and the MTU condition are normal. Error codes 01 through 99 indicate the contents of an erroneous operation and a unit failure. (See Section C of the Maintenance Manual for a description of error codes and corrective actions.)

2) Bit 8 TAG IN
Of the Bus Out bits 0 through 8, only bit 0 indicates "1".

i. Sense Byte 8
This byte is effective when all bits of the Go, Control, and the Status Tag, are zeros and both B03 and B05 are "1"s. This byte is also effective when both the Go Tag and the Status Tag are "1".

1) Bit 0 UERS (Unit Erase Current ON)
This bit indicates the state of the current flow in the erase head of the MTU.

2) Bit 1 UACT (Unit Action)
This bit is "1" while the MTU is in a range of operation from the actual start of the MTU operation to the end of its operation. (The turn-around time is not included. However, it is included during positioning of the MTU.)

3) Bit 2 UBWD (Unit Backward Status)
This bit indicates that the MTU is in the Backward status. The signal varies with the advancement of the MTU operation during the Forward operation or stop position.

4) Bit 3 UWCON (Unit Write Current ON)
This bit indicates that the current is flowing in the write head of the MTU.

5) Bit 4 U64S (Unit 64% Slice)
This bit indicates that in the 6250 rpi read/write operation, the slice level is cut down to 64% after counting up the Self-Adjust Gain Control

6) Bit 5 UOVRN (Unit Overrun)
This bit indicates that the length of data block (TMBOB) did not exceed 20m while the MTU executed the Space file operation.

7) Bit 6 UPE (Unit PE Mode)
This bit indicates that the operation mode in which the MTU is actually carrying out the processing is the Phase Encoded (PE) mode.

8) Bit 7 TM (Tape Mark)
This bit is set to "1" when the MTU normally detectes a TM block using the SPF or BSPF command.

9) Bit 8 TAG IN
If the Bus Out bits 0 through 8 are an odd number, this bit is "1".

3.4 Control Circuit of the MTU

3.4.1 Introduction

The control circuit is implemented by TTL circuit ICs, which are mounted on two logical circuit packages. The primary functions of the control circuit are to:

(1) Control the sending and receiving of interface signals between the FMT and the MTU.

(2) Determine the timing for driving the motors and solenoids in the mechanism section of the MTU and control automatic tape feeding.
(3) Carry out the servo control on the capstan motor.

(4) Carry out the servo control on the reel motor.

(5) Receive commands from the operator through the operator panel and the maintenance operating panel to execute various tape handling operations (autoloading, rewinding, unloading, and resetting).

Most of these functions are controlled by the memory circuit using the Programmable Read Only Memory (PROM) having 32K bits (Microprogram system).

One word consists of 24 bits, whose uppermost bit is the parity bit. Since the control circuit is provided with 3 PROM units, each consisting of 32K bits, the memory capacity is 4K words.

The microprogram for the present MTU is written using 26 kinds of microcommands. Execution of one microcommand takes 1 s.

3.4.2 Logical Operation of the Control Circuit

Block diagrams of the control circuit are shown in figures 3-4 and 3-5.

Interface Control Section

Figure 3-4 shows the circuit that carries out the interface control. First, a signal from the MTC is received by the receiver circuit and is converted into a signal with standard logic level. This converted signal is divided into two; the Tag signal and the Bus Out signal, as described for the interface in the preceding Section 3.3. The Tag signal and the Bus Out signal enter the check circuit, and they are checked as to whether they meet the given interface rules. After checking, the composite Tag signal and the composite Bus Out signal enter the test signal selecting circuit shown in Figure 3-5 and are used for the interface control with the aid of the PROM. The other signals, which are not subjected to the microprogram, are processed in the interface control logical section. The circuit in this section primarily controls the communication registers and generates reset signals for various errors.

The Bus Out signals are output as written data to the write amplifier as follows:

- The Read signal
- The Bus Out signal (at the time of the LWR)
- The register output
- The Sense signal
- The Communication Register signal
- Physical unit number setting.

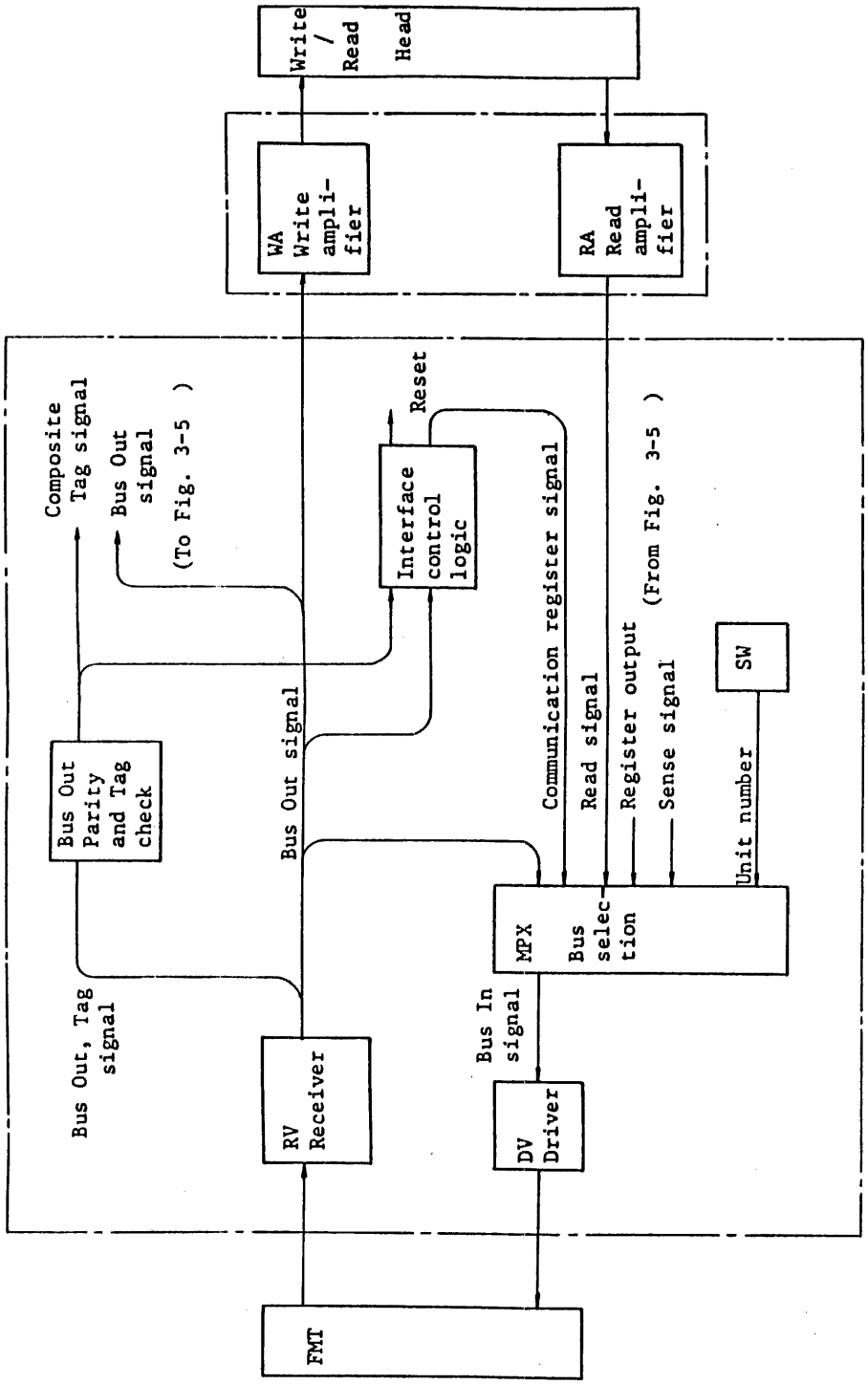


Figure 3-4. Block diagram of control circuit (page 1 of 2).

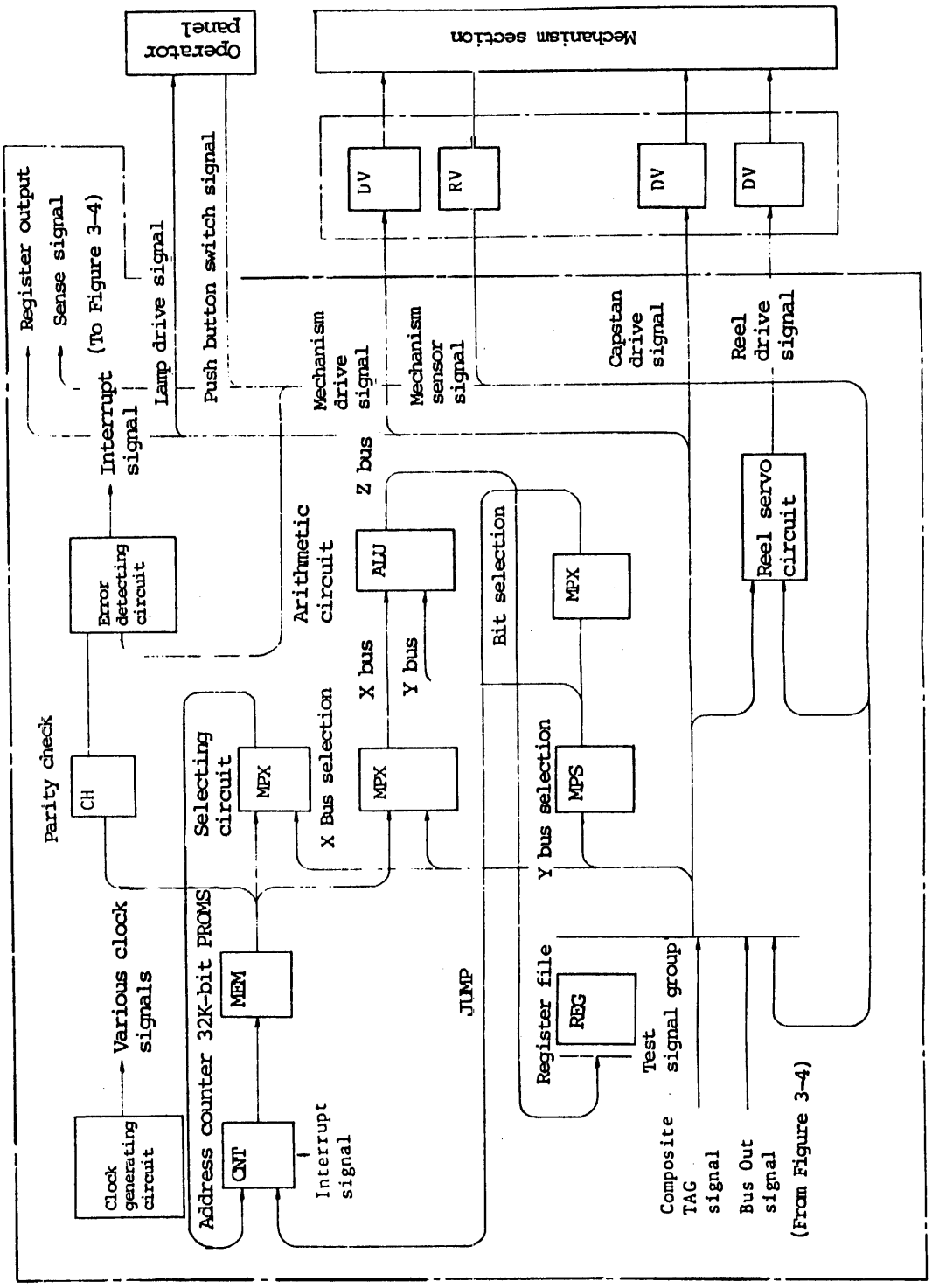


Figure 3-5. Block diagram of control circuit (page 2 of 2).

Microprogram Control Section

Figure 3-5 shows a block diagram of the microprogram control section. The clock generating circuit generates a clock by dividing a standard frequency of 8 MHz. The main clock signals, CL1MA and DSPCL, are two-phase clocks (with a phase difference of 500 ns) having a pulse width of 62 ns and a repetitive frequency of 1MHz.

The microprogram is stored in three 32 kilobit PROMs. One word consists of 24 bits, and each microcommand has a one-word or two-word structure. The address for the microprogram is indicated by the address counter. There are 4096 addresses from 0 to 4095 in decimal notation (or from 0000 to 0FFF in hexadecimal). The address counter counts the address by +1 for a normal microcommand. In a branch, the address of the destination is preset on the address counter if the JUNP signal indicates "1". When only a specified test signal in the test and jump instruction satisfies the requirements, the JUMP signal indicates "1".

One word (24 bits) of the microprogram used in the MTU has even parity, which is checked by the detected circuit. When a parity error is detected, the error detecting circuit for monitoring the failure of the MTU interrupts the microprogram and issues a TUCK (Tape Unit Check) signal. This error detecting circuit also monitors the mechanical section (including the air system, capstan system, and tape reel system). When the MTU fails, the error detecting circuit issues an interrupt signal to the microprogram.

The register file consists of 20 registers, three counters, and test signals. One register has an 8-bit structure; one counter has a 12-bit structure. Each bit can be set and reset by a microcommand. The test signals are the read-only signals, which are considered to be the same as other physical registers from the program standpoint. Each bit of the registers/counters and each test signal that constitutes the register file is described in section 3.4.4. The output of this register file is selected by the Y Bus selecting circuit and only the one byte (8 bit) signal specified by the microcommand is indicated on the Y Bus. The output of the PROM and the output of the work register (WK0) are selected by the X Bus selecting circuit. Only the one-byte signal from either output is indicated on the X bus. The arithmetic operation is executed between the X bus and the Y bus, and the result is sent out to the Z bus. The Z bus is connected to the write input for the register file. The data loaded on the Z bus is written in the register/counter specified by the microcommand.

A particular bit of the one-byte signal on the Y bus is extracted by the bit selecting circuit to be used as a test condition for a test and jump instruction. The bit to be selected is determined according to the specification of the microcommand.

The register section of the register file comprises the register to determine the operation of the air system, the register to indicate the current value for the capstan, the register related to the reel control, and so forth. The outputs of these individual registers are sent to special packages to control the operations of the mechanical section. On the other hand, the outputs of various detectors that check operations of the mechanical section are converted into the data at various levels and are then sent out. These sensor signals for the mechanical operations constitute part of the test signal group in the register file. Other than these signals, the pushbutton switch signals from the front panel, the composite signals, and Bus Out signals from the interface control section are input in the test signal group. The reel servo circuit receives the output from the register file and sensor signals for the mechanical operations to generate the reel drive signal.

3.4.3 Microcommands

The microprogram carries out the control of the autoload sequence, capstan servo, FMT interface, self diagnosis, and error recovery. the microprogram has 27 types of instructions. These instructions are translated individually through the assembler into machine language, each consisting of 24 bits. The following paragraphs explain the rules for the conversion between a microcommand and its corresponding machine language.

(1) ORI/OR instruction

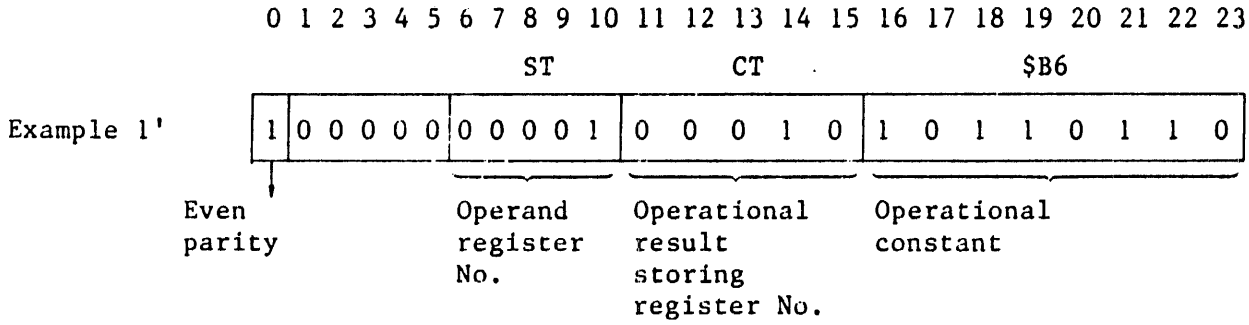
This instruction is intended to take summation of the contents of a register in the file and the constant (or the contents of general register 0) in bit-to-bit correspondence, and to store the results in another register.

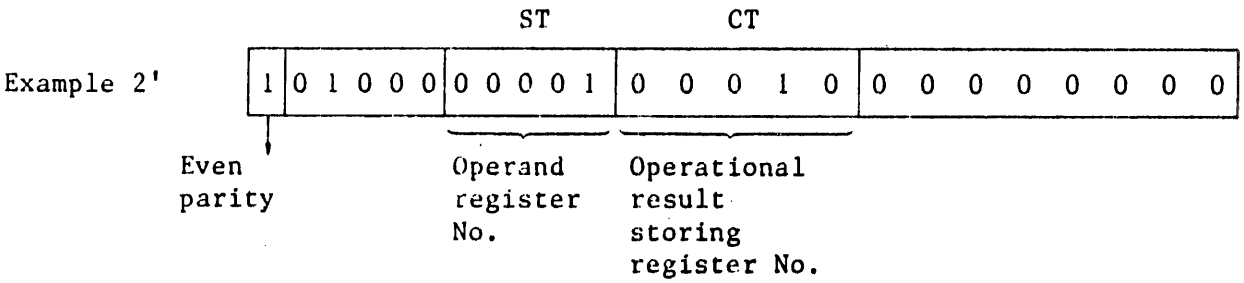
	1st operand	2nd operand	3rd operand	
Example 1	ORI ST , $B6 , CT			ST or $B6 —> CT

	1st operand	2nd operand	
Example 2	ORI ST , CT		ST or WKO —> CT

Instruction / Operand	ORI	OR
1	Signal name for operand register	The same as the left
2	Write an operational in hexadecimal	Name of the register for storing operational results
3	Name of the register for storing the operational results	

The corresponding machine languages are as follows.





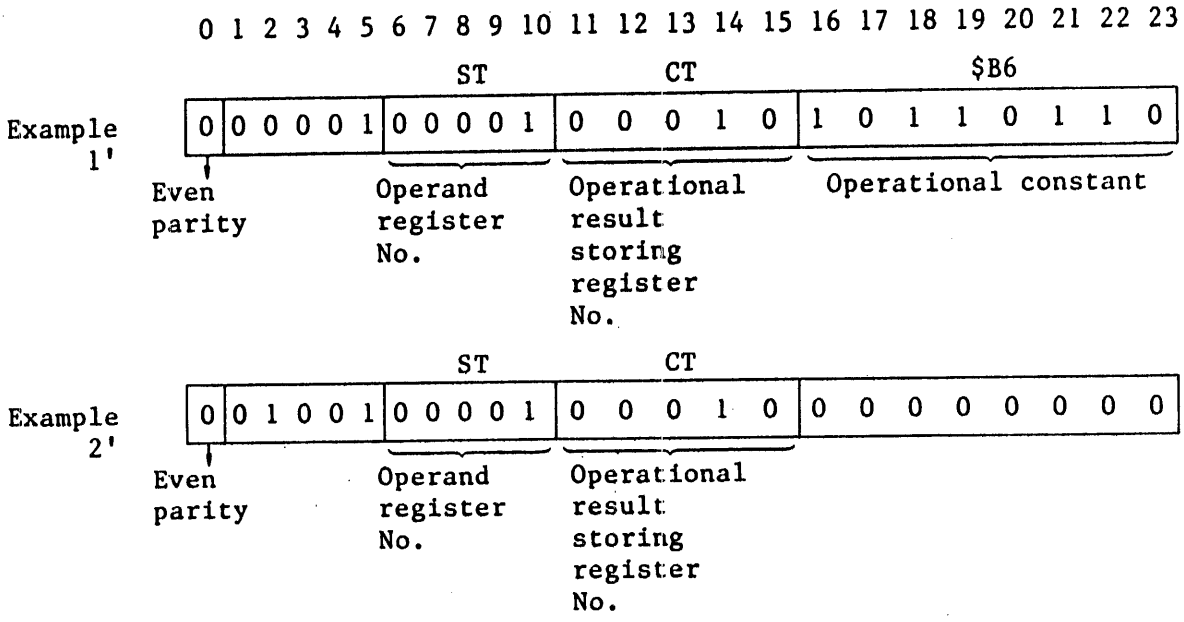
Here, ST stands for register No. $1 and CT for register No. $02

(2) ANDI/AND instruction

This instruction is intended to take the product of the contents of a register in the file and the constant (or the contents, of general register 0) in bit-to-bit correspondence, and to store the results in another register.

Example 1	ANDI ST , $B6 , CT	ST AND $B6 → CT
Example 2	AND ST , CT	ST AND WK0 → CT (General register)

The corresponding machine languages are as follows.

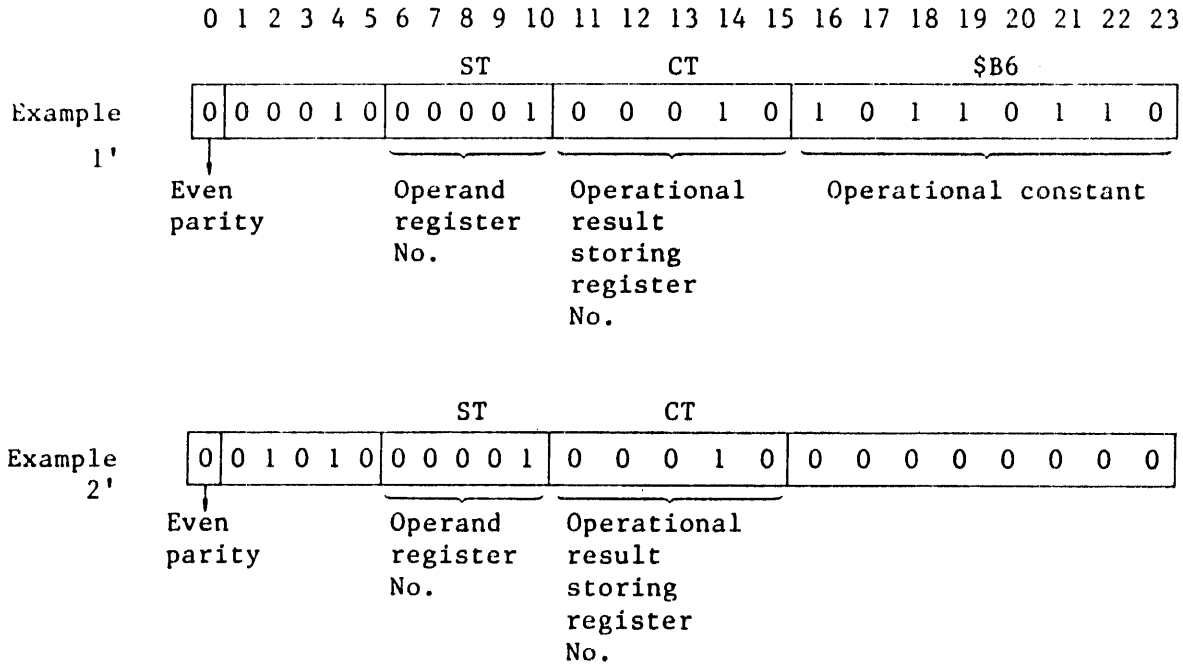


(3) EORI/EOR instruction

Replacing the term for the kind of operation "logical summation" with "exclusive OR", this instruction is intended to carry out the same as the instruction in (1).

Example 1	EORI ST , $B6 , CT	ST EOR $B6 → CT
Example 2	EOR ST , CT	ST EOR WK0 → CT (General register)

The corresponding machine languages are as follows.



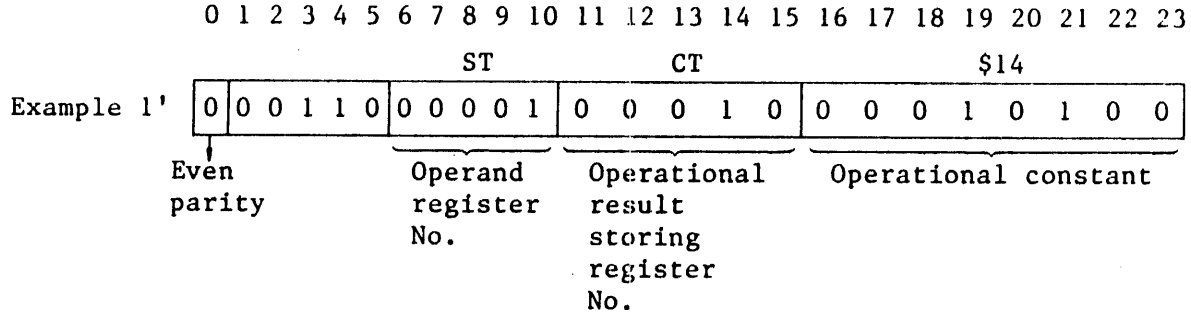
(4) SUB I/SUB instruction

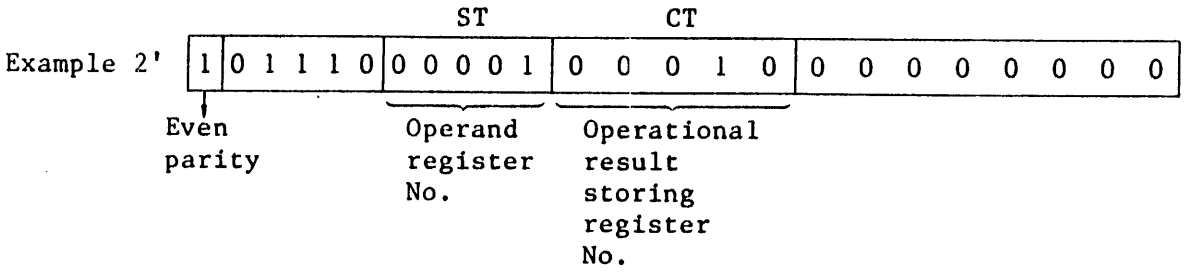
This instruction is intended to subtract a constant (or the contents of the general register) from the content of a register in the file, and to store the results in another register.

Example 1 | SUB I ST , $B6 , CT | ST - $14 —> CT

Example 2 | SUB ST , CT | ST - WKO —> CT (General register)

The corresponding machine languages are as follows.





(5) ADDI/ADD instruction

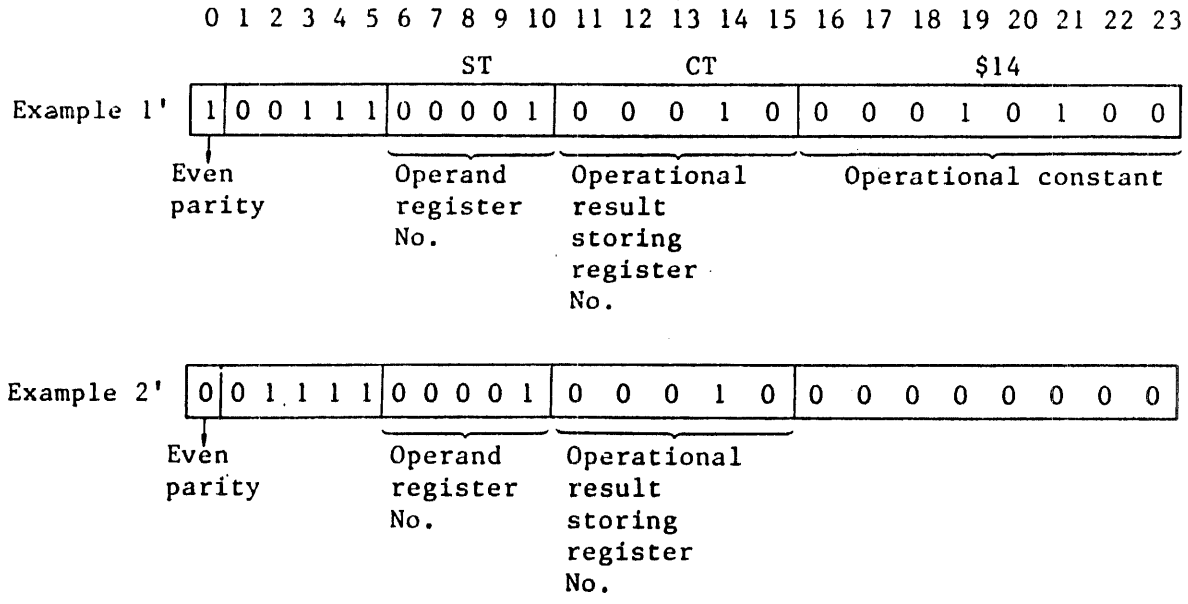
This instruction is intended to add a constant (or the constants of the general register) to the contents of a register in the file, and to store the results in another register.

When the add result overflows, the signal (CARRY) is turned to "0".

Example 1 | ADDI ST , $B6 , CT | ST + $14 —> CT

Example 2 | ADD ST , CT | ST + WKO —> CT (General register)

The corresponding machine languages are as follows.

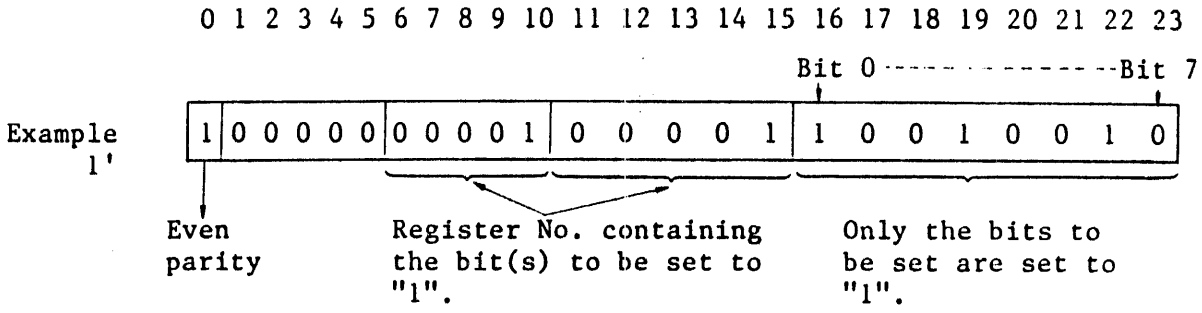


(6) SET instruction

This instruction is intended to set a specified bit in the file to "1". The operand represents the name of the signal for the specified bit. One or more bits may be set to "1" if they are contained in the same register in a file.

	Operand
Example 1	SET SERS,SWRS,1600

The corresponding machine



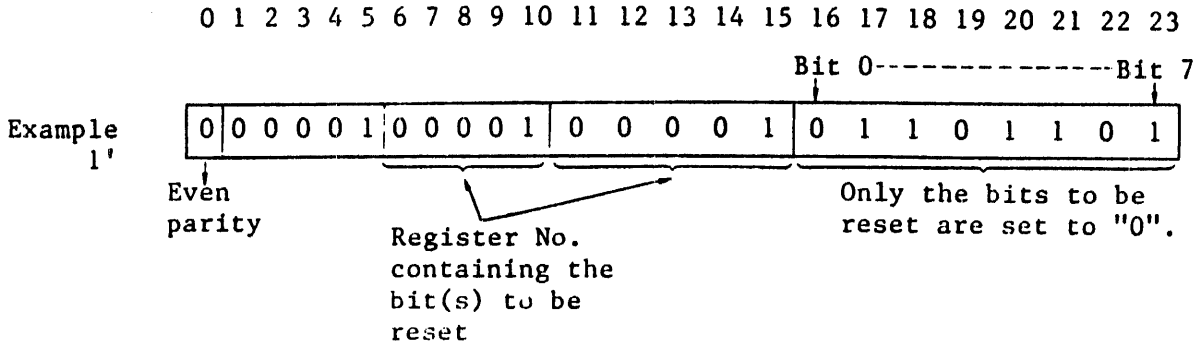
Here, SERS stands for register No. $01, bit 0
SWRS stands for register No. $01, bit 3
1600 stands for register No. $01, bit 6

(7) RESET instruction

This instruction is intended to set a specified bit in the file to "0". The other functions of this instruction are the same as those of the preceding instruction in (6).

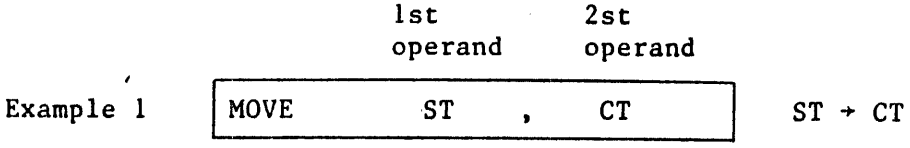
Example 1	RESET SERS,SWRS,1600

The corresponding machine language is shown as follows.

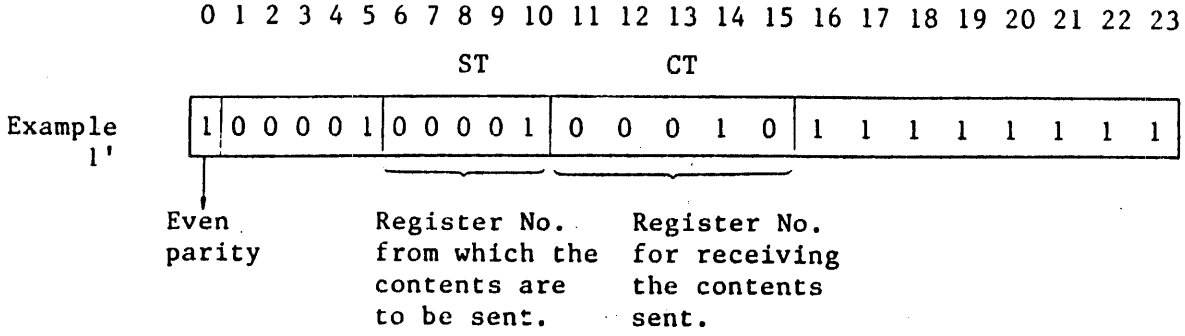


(8) MOVE instruction

This instruction is intended to move the contents of a specified register to another register. The first operand indicates the name of the register of which the contents are to be sent. The second operand indicates the name of the register for receiving the contents sent.



The corresponding machine language is shown as follows.

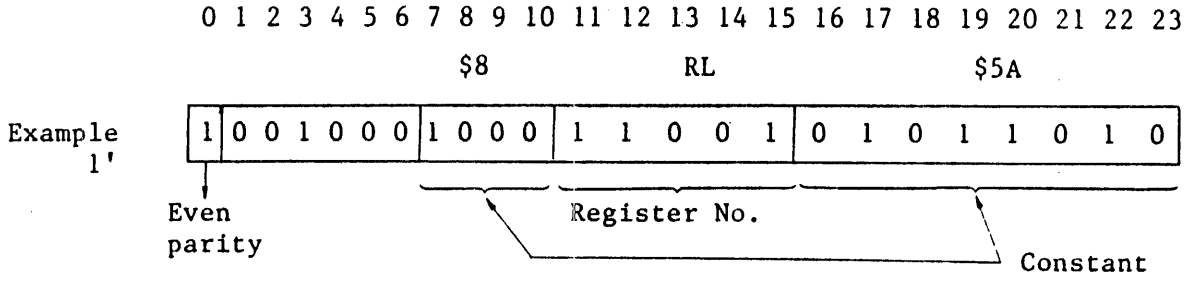


(9) LOAD instruction

This instruction is intended to load a contant on a specified register in the file. The first operand indicates a two-digit hexadecimal constant. The second operand indicates the name of the specified register.

	1st operand	2nd operand		
Example 1	LOAD	$85A ,	RL	$85A → RL

The corresponding machine language is shown as follows.



Here, the register No. in the RL is written as $19 in hexadecimal.

(10) TIME instruction

This instruction is intended to cause the timer to overflow when the timer steps up as many as the number of steps specified in the operand. The register No. in a file of the timer is specified as $11. The operand indicates the decimal or hexadecimal number of steps which causes the timer to overflow. When the number of steps reaches 256 the timer overflows.

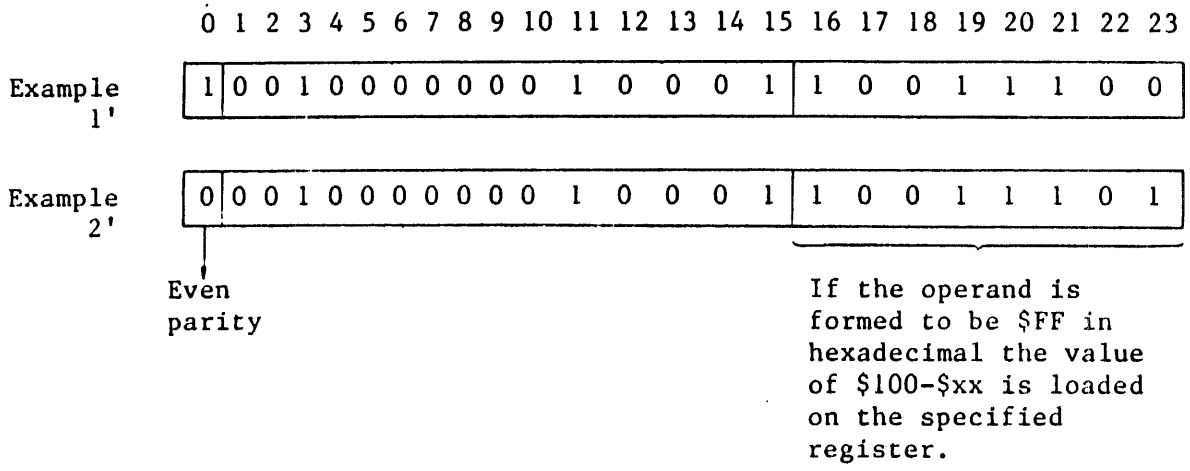
		Operand
Example 1	TIME	100
		Decimal

Example 2

TIM	$63

Decimal

The corresponding machine languages are shown as follows.



(11) COUNT instruction

This instruction is intended to cause the counter to overflow when counting steps up as many as the number of steps specified in the operand. The register No. in a file of the counter is $12. The remaining functions of this instruction are the same as those of the instruction in (10).

Example 1

COUNT	100

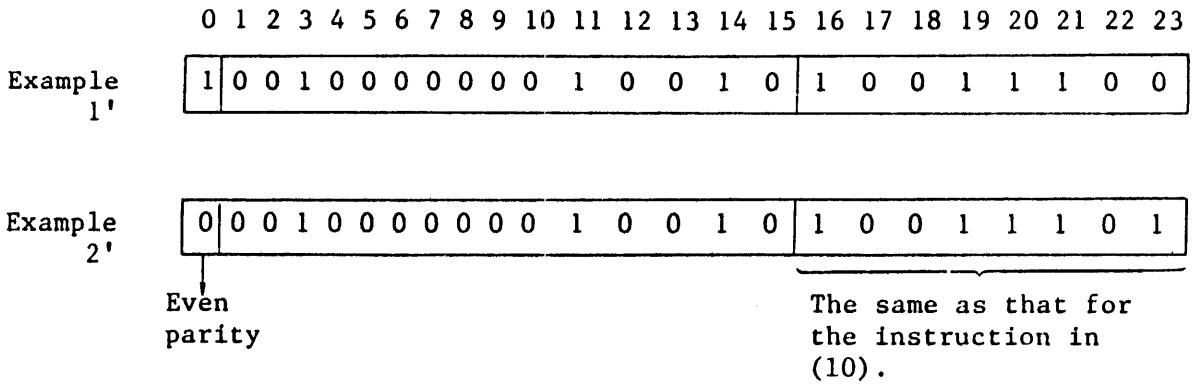
Decimal

Example 2

COUNT	$63

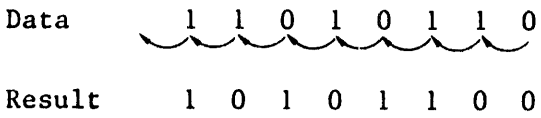
Decimal

The corresponding machine languages are as follows.



(12) SHIFT instruction

This instruction is intended to shift each bit of the content of a specified register in a file to the next higher weight position and to store it in another register.

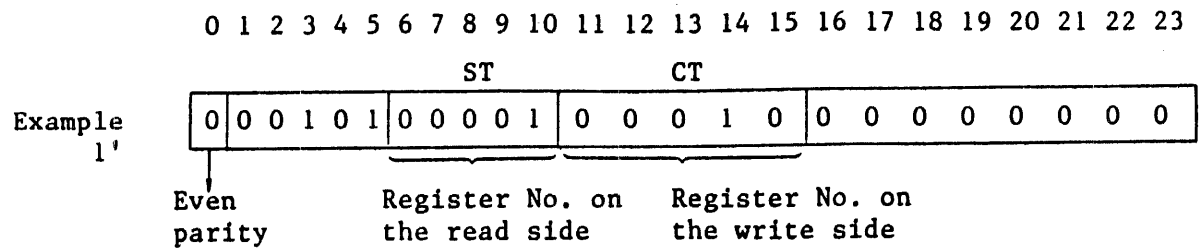


The first operand represents the name of the signal for the register on the read side.

The second operand represents the name of the signal for the register in which the result is loaded.

	1st operand		2nd operand
Example 1	SHIFT	ST ,	CT

The corresponding machine language is shown as follows.



(13) COMPARE (COMP) instruction

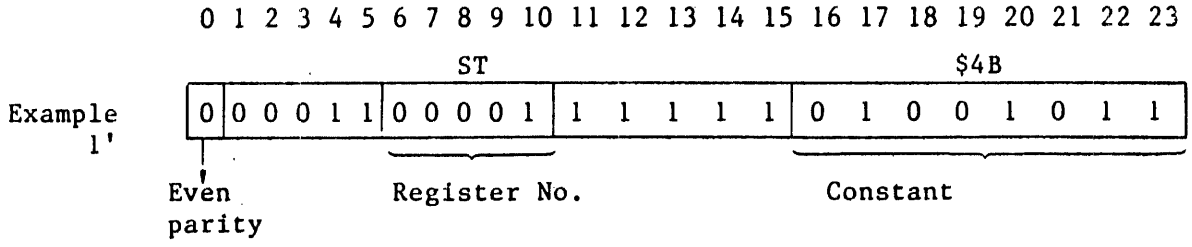
This instruction is intended to compare the contents of a specified register in a file with a given constant (or the contents of the general register). The first operand represents the name of the signal for the specified register. The second operand represents the hexadecimal constant or the name of the signal for the general register. The compared results can be seen from the signal (EQUAL) or (CARRY).

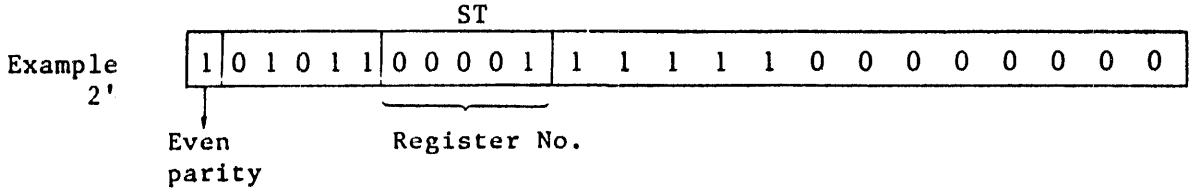
	1st operand		2nd operand
Example 1	COMPARE ST	,	$4B

	1st operand		2nd operand
Example 2	COMPARE ST	,	WK0

(General register)

The corresponding machine languages are shown as follows.





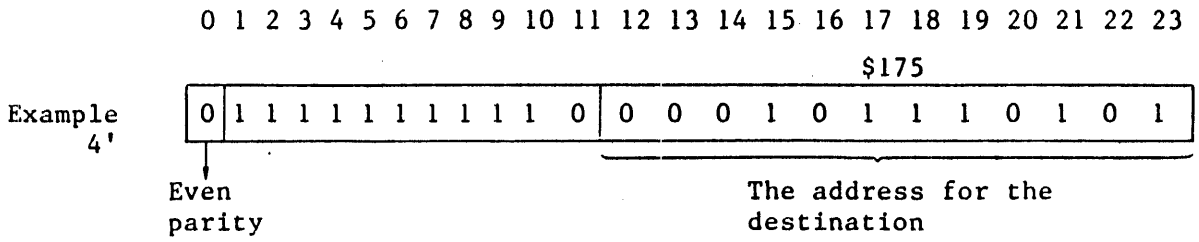
(14) JUMP instruction

This instruction is intended to make an unconditional jump to the address specified by the operand. There are three ways of specifying the address in the operand:

- o Using a label to indicate the destination
- o Using an asterisk * for the original address from which the forward or backward jump is made as shown in examples 2 and 3.
- o Using an absolute address to indicate the destination

		Operand
Example 1	JUMP	LABEL
Example 2	JUMP	*-3
Example 3	JUMP	*+5
Example 4	JUMP	$175

The following shows the machine language into which example 4 is converted.

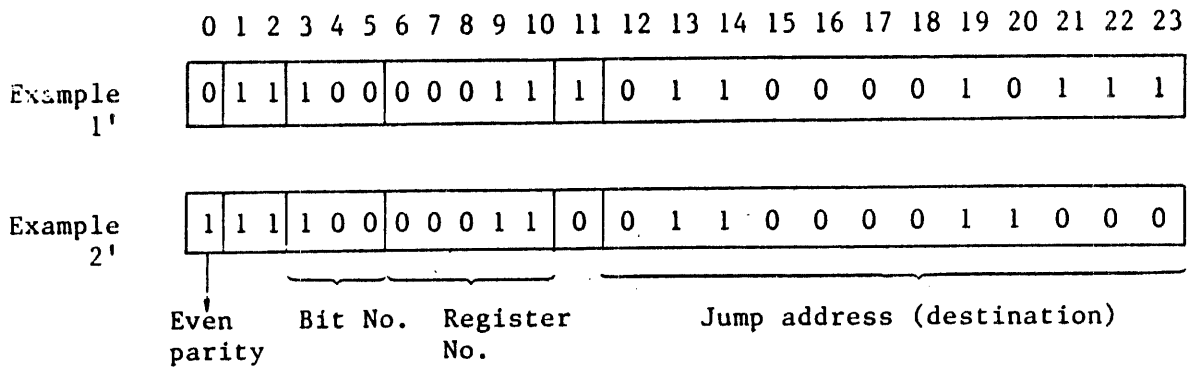


(15) JUMP=1/JUMP=0 instruction

The JUMP=1 instruction is intended to make a jump when it finds a bit in a specified file to indicate "1". The JUMP=0 instruction is intended to make a jump when it finds a bit in a specified file to indicate "0". When no jump is made the execution moves to the next address. The first operand indicates a jump address. There are three ways of specifying the jump address in the first operand, similar to the preceding instruction in (14). The second operand indicates the name of the test bit signal in the specified file.

		1st operand		2nd operand
Example 1	JUMP=1	$617	,	SVOK
Example 2	JUMP=0	$618	,	SVOK

The corresponding machine language is shown as follows.



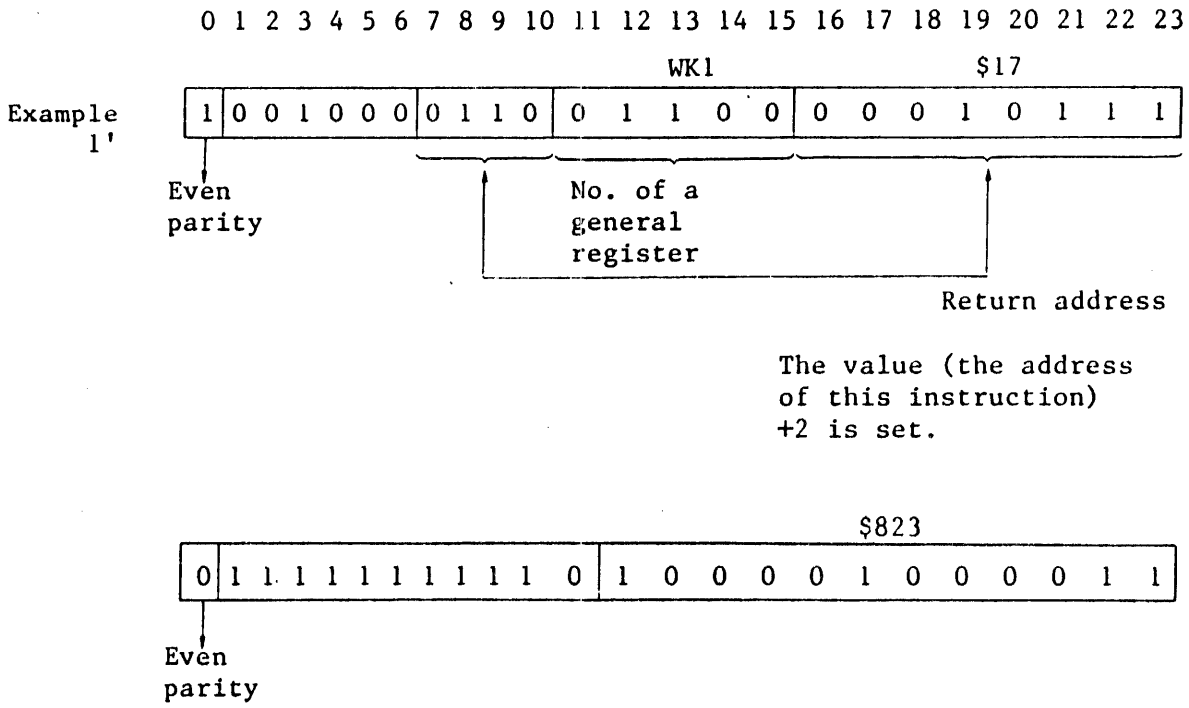
Here, SVOK represents register No. $03, bit No. $14.

(16) CALL instruction

This instruction is the CALL instruction for a subroutine. Its machine language consists of two words. The first operand specifies the name of a specified subroutine. The second operand specifies one from general registers 1 to 4 for storing the return addresses.
Here, the register No. for WKI is defined as $0C, the address of this instruction is defined as $615 and the address of SUBR is defined as $823.

	1st operand	2nd operand	
Example 1	CALL	SUBR ,	WK1

The corresponding machine language is shown as follows.



Here, the register No. for WK1 is defined as $0C, the address of this instruction is defined as $615 and the address of SUBR is defined as $823.

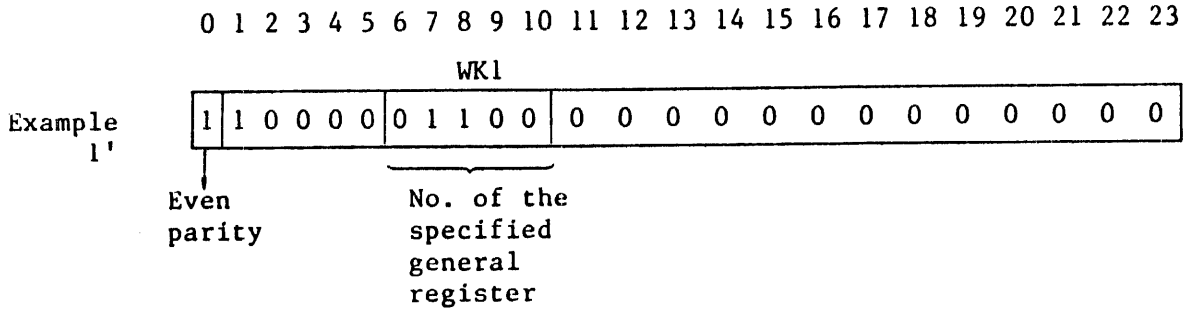
(17) RETURN instruction

This instruction is the RETURN instruction to be issued from a specified subroutine. The operand specifies one from among general registers 1 to 4 storing the return address.

This instruction carries out no operation and has no operand. All the bits of the machine language of the NOP instruction are converted into zeros. All the bits of the machine language of the HOP instruction are converted into "1"s.

	Operand
Example 1	RETURN WK1

The corresponding machine language is shown as follows.



(18) NOP/HOP instruction

This instruction carries out no operation and has no operand. All the bits of the machine language of the NOP instruction are converted into zeros. All the bits of the machine language of the HOP instruction are converted into "1"s.

Example 1	NOP
Example 2	HOP

(19) The $ instruction

This instruction is intended to represent the operand in machine language without conversion.

	Operand
Example 1	$ $789ABC

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Example 1'	0	1	1	1	1	0	0	0	1	0	0	1	1	0	1	0	1	0	1	1	1	1	0	0

3.4.4 Register Files and Test Signals

A register file is set or reset by an instruction in the microprogram (see the preceding Section 3.4.3) to drive the motors or solenoid installed in the mechanical section of the MTU. When a jump instruction is applied to a register file, a bit in the register file is detected, and the execution jumps to the specified destination. The jump condition comprising various detecting signals from the mechanical section or the signals from the control circuit is used to change the flow of the microprogram during execution.

The contents of register files and jump conditions are described in the following paragraphs (1) to (36). In the following tables, an address product is a hexadecimal address assigned to the relevant register. Numbers in the bit column represent ordinal bit numbers. Symbols in the name column are signal names used in a circuit or flowchart.

(1) Work 0 register (WK0, WORK 0)

Register		Signal name	Description of the signal name	Function
Address	Bit			
00	0	WK00	Work 0 Bit 0	A number of bits together play the role of temporary register supplementary to another register
	7	WK07	Work 0 Bit 7	

(2) Status register (ST, STATUS)

Register		Signal name	Description of the signal name	Function
Address	Bit			
01	0	SERS	Set Erase Status	This bit is set to "1" by the erase instruction from the FMT or the maintenance panel, and is set to "0" by the read instruction.
	1	BWD	Backward Status	This bit indicates "1" when the MTU is in the backward status.
	2	ALUOK	ALU-OK	When the ALU check routine is executed after the power is supplied and the operation of the MTU is normal, this bit is set to "1".
	3	SWRS	Set Write Status	This bit is set to "1" by the write instruction from the FMT or the maintenance panel and set to "0" by the read instruction.

Register		Signal name	Description of the signal name	Function
Address	Bit			
01	4	ERRST	Error Reset	The error reset signal
	5	STRMD	Streaming Mode	This bit is set to "1" when the MTU is operated in the streaming mode.
	6	1600	1600 rpi	This bit is set to "1" by the Set 1600 instruction from the FMT or the maintenance panel and is set to "0" by the Set 6250 or NRZI signal.
	7	PE	PE Mode	This bit is the same as the 1600 signal, and always indicates 1 when the tape comes to the BOT.

(3) Control register (CT, CONTROL)

Register		Signal name	Description of the signal name	Function
Address	Bit			
02	0 1 2	LVLT0 LVLT1 LVLT2	Level Test 0 to 2	This signal specifies the slice level according to the signal from the FMT or the maintenance panel.
	3	RLACT	Reel Action	The reel action signal to be sent to the reel control circuit.
	4	SEMK	Set Error Mark	This bit is set to "1" by the print error mark instruction from the FMT.

Register		Signal name	Description of the signal name	Function
Address	Bit			
02	5	DSE	Data Security Erase	This bit is set to "1" during the execution of the DSE operation.
	6	RWD	Rewind	This bit is set to "1" during the execution of rewinding.
	7	UNL	Unload Reset Online (RSONL)	This bit is set to "1" during the execution of unloading. Also, this signal is used for the signal for on-line resetting.

(4) Servo register (SV, SERVO)

Register		Signal name	Description of the signal name	Function
Address	Bit			
03	0	HSRUN	High Speed Run	This bit is set to "1" when the reel/capstan motor is operated at a high speed during a rewind or unload operation.
	1	CAPGO	Capstan Go	This bit is set to "1" when receiving the GO signal from the FMT.
	2	LTPAS	Low Tape Pass	This bit is set to "1" when detecting the low tape during the rewind operation.
	3	RVSL	Reversal	This is the signal set when a certain time passes after the capstan motor stops.

Register		Signal name	Description of the signal name	Function
Address	Bit			
03	3		Mid Load (MIDLD)	This bit is set to "1" when the LOAD REWIND switch is depressed and the MTU is in the mid load status.
	4	SVOK	Servo OK	If no failure occurs in the servo system after setting the Servo ON, this bit is set to "1".
	5	SVON	Servo ON	This signal activates the servo circuit for the capstan and reel motor.
	6	RLSTP	Reel Stop	This bit is set to "1" when one second elapses after the capstan stops. When the capstan starts this bit indicates "0".
	7	RSVSW	Reel Servo Switch	The same as the reel stop signal. However, this bit always indicates "1" when the M2432L, M2433L, M2435L1/L2 MTU is operated in the high speed mode.

(5) Mechanism register (ME, MECHA)

Register		Signal name	Description of the signal name	Function
Address	Bit			
04	0	UCKLP	Unit Check Lamp	The signal for lighting the UNIT CHECK lamp on the operating panel.
	1	EMKDV	Error Marker Drive	The signal for activating the error marker solenoid.
	2	CTGCL	Cartridge Close	The signal for closing the cartridge
	3	WNDCL	Window Close	The signal for closing the window
	4	CLNDV	Cleaner Drive	The signal for activating the autocleaner
	5	AIRDV	Air Drive	The motor drive signal for generating air pressure and vacuum.
	6	SOLVL	Solenoid Valve Drive	The signal for switching the solenoid valve. This bit indicates "0" during auto-loading and "1" while the tape is running and pressure is on.
	7	PRSVL	Pressure Valve Drive	The signal for switching the pressure valve. When this signal indicates "1" the pressure valve operates during autoloading, and it is in the "0" state while the tape is running.

(6) Spare register (SPR, SPARE)

Register		Signal name	Description of the signal name	Function
Address	Bit			
05	0			Not used at present
	1			
	2			
	3			
	4			
	5			
	6			
	7			

(7) Capstan register (CP, CAPSTAN)

Register		Signal name	Description of the signal name	Function
Address	Bit			
06	0	LOCK	Capstan Lock	The signal to activate the servo locking when the capstan motor stops.
	1	ACT	Capstan Action	The signal driving the capstan motor.
	2	*SIGN	Sign Bit	When this signal indicates "0" the capstan motor rotates in the forward direction and when this signal indicates "1"

(continued on next page)

Register		Signal name	Description of the signal name	Function
Address	Bit			
	2			the capstan motor rotates in the backward direction.
06	3	DAC16	D/A Converter 16 to 1	This signal indicates the value of the drive current to the capstan motor.
	4	DAC8		
	5	DAC4		
	6	DAC2		
	7	DAC1		

(8) Error/Key register (ER, KEY)

Register		Signal name	Description of the signal name	Function
Address	Bit			
07	0	ECD0	Error Code 0 to 7	This signal represents the contents of error with error code 0 to 7 occurring when the Unit Check status is generated.
	7	ECD7		
	0	K0	Key 0 to 7	This signal is usually used as the Key register. It is the index bit signal for the microprogram and can be used in various ways by various routines.
	7	K7		

(9) Sense register (SN, SENSE)

Register		Signal name	Description of the signal name	Function
Address	Bit			
08	0	INSTL	Installed	After the power supply is turned on, this signal checks a signal from each printed circuit board, and if the checking results prove to be correct this bit is set to ON.
	1	DIAG	Diagnosis Mode	The signal for checking the photosensor.
	2	GAPEN	Gap Control Enable	The control signal for the gap control.
	3	READY	Device Ready	This bit is set to "1" when the MTU gets in a status that can be controlled by the FMT.
	4	BOTS	BOT Sensed	The signal to hold the status that the BOT is detected during backward tape running.
			TWA Sensed (TWAS)	The signal to hold the TWA.
	5	SHBOT	Search BOT	The signal to execute tape feeding as far as the BOT during autoload, rewind, or unload operation.
			Load Retry (RETRY)	The retry signal for auto loading the tape with cartridge.
	6	LOAD	Auto Load	This signal is set to "1" when the LOAD REWIND button is depressed and auto loading starts; it is set to "0" when

Register		Signal name	Description of the signal name	Function
Address	Bit			
	6			the auto load operation is completed.
	7	.FILE	Space/Backspace File	The signal indicating that the tape mark search is being executed.

(10) Flag register (FL, FLAG)

Register		Signal name	Description of the signal name	Function
Address	Bit			
09	0 1	TSL10 TSL11	Timer 1 Select 0, 1	Signal for switching the input condition of the timer. TSL10=0, TSL11=0 : 1μs TSL10=0, TSL11=1 : 200μs TSL10=1, TSL11=0 : 3.2ms TSL10=1, TSL11=1 : 51.2ms
	2 3	CSL0 CSL1	Count Select 0, 1	Signal for switching the input condition of the counter. CSL0=0, CSL1=0 : 1μs CSL0=0, CSL1=1 : QTP CSL0=1, CSL1=0 : LTP CSL0=1, CSL1=1 : 16QTP
	4	TSL00	Timer 0 Select 0	Signal for switching the input condition of the timer. TSL00 = 0 : 200μs TSL00 = 1 : 1μs

Register		Signal name	Description of the signal name	Function
Address	Bit			
09	5 6	WKSL0 WKSL1	Work 5 to 8 Select 0, 1	Select signal for work 5 to 8 registers. WKSL0=0. WSL1=0 : Work 5 WKSL0=0, WSL1=1 : Work 6 WKSL0=1, WSL1=0 : Work 7 WKSL0=1, WSL1=1 : Work 8
	7	MASK	Mask	This is the interrupt control signal that accepts an interrupt signal when this signal indicates "0"; it does not accept an interrupt signal when this signal indicates "1".

(11) Register (SPR2)

Register		Signal name	Description of the signal name	Function
Address	Bit			
0A	0			
	1	ACADV	Accelate Air Drive	When air motor is started, this bit is set to "1" during the acceleration.
	2			
	3	BFBOT	Before BOT	This indicates the BOT is before the load point under unloading up to column out.
	4	RETENS	Tape Retension	This indicates doing Tape Retension from BOT to EOT.
	5			
	6	CMTDV	Cartridge Drive	This activates the cartridge motor drive circuit.
	7			

(12) Motion register (MC, MOTION)

Register		Signal name	Description of the signal name	Function
Address	Bit			
0B	0	LWSL	Low Slice	The signal to set the slice level to 7% when erasing.

Register		Signal name	Description of the signal name	Function
Address	Bit			
0B	1	WTRC	Write Control	Signal to flow the write current.
	2	ERSC	Erase Control	Signal to flow the erase current.
	3	HSC	High Speed Control	Signal for indicating that the tape rewind or unload operation is being executed at greater than 200 ips.
	4	SPOS	Set Positioning	Signal for indicating that the set positioning at the time of switching normal to streaming and while streaming is being executed.
	5	WPOS	Write positioning	The signal is kept at the set position until the write current is turned on during the write operation in the streaming mode.
	6	HSMD	High Speed Mode	Signal for indicating that the tape is running at streaming mode (125 ips or 200 ips).
	7	MTU	MTU	This signal indicates "0" when the M2430L, M2431L, M2434L1/L2 MTU is operating; it indicates "1" when the M2432L, M2433L, M2435L1/L2 is operating.

(13) Work 1 register (WK1, WORK 1)

Register		Signal name	Description of the signal name	Function
Address	Bit			
0C	U-0	WK10U	Work 1 Upper bit 0 to 3	A number of bits together play the role of temporary register supplementary to another register (bits 0 to 7 are used). A number of bits of this register are also intended to set return address for the subroutine in use (Upper bits 0 to 3 and bits 0 to 7 are used).
	U-3	WK13U		
	0	WK10	Work 1 bit 0 ∿ 7	
	7	WK17		

(14) Work 2 register (WK2, WORK 2)

Register		Signal name	Description of the signal name	Function
Address	Bit			
0D	U-0	WK20U	Work 2 Upper bit 0 to 3	A number of bits together play the role of temporary register supplementary to another register (bits 0 to 7 are used).
	U-3	WK23U		
	0	WK20	Work 2 bit 0 to 7	A number of bits of this register together are also intended to set the return address for the subroutine in use (Upper bits 0 to 3 and bits 0 to 7 are used).
	7	WK27		

(15) Work 3 register (WK3, WORK 3)

Register		Signal name	Description of the signal name	Function
Address	Bit			
0E	U-0 : U-3	WK30U : WK33U	Work 3 Upper bit 0 to 3	A number of bits together play the role of temporary register supplementary to another register (bits 0 to 7 are used).
	0 : 7	WK30 : WK37	Work 3 Bit 0 to 7	A number of bits of this register are also intended to set the return address for the subroutine in use (Upper bits 0 to 3 and bits 0 to 7 are used).

(16) Work 4 register (WK4, WORK 4)

Register		Signal name	Description of the signal name	Function
Address	Bit			
0F	U-0 : U-3	WK40U : WK43U	Work 4 Upper bit 0 to 3	A number of bits together play the role of temporary register supplementary to another register (bits 0 to 7 are used).
	0 : 7	WK40 : WK47	Work 4 bit 0 to 7	A number of bits of this register are also intended to set the return address for the subroutine in use (Upper bits 0 to 3 and bits 0 to 7 are used).

(17) Time 0 register (TM0, TIME 0)

Register		Signal name	Description of the signal name	Function
Address	Bit			
10	0 ⋮ 7	TM00 ⋮ TM07	Timer 0 bit 0 to 7	This register carries out time counting according to the indication of bit 4 (TSL00) of the flag register.

(18) Jump condition (SH)

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
11	0			Not used at present
	1			
	2			
	3			
	4			
	5			
	6			
	7	*MARGN	Margin Test	This bit directs the MTU to increase the capstan speed by approximately 20% and to carry out testing.

(19) Time 1 register (TM1, TIMER 1)

Register		Signal name	Description of signal name	Function
Address	Bit			
11	0	TM10	Timer 1 Bit 0 to 7	This register carries out time counting according to the indication of bits 0 and 1 (TSL10 and TSL11) of the flag register.
	7	TM17		

(20) Count register (CN, COUNTER)

Register		Signal name	Description of the signal name	Function
Address	Bit			
12	U-0	C2048	Count 2048	This register is a 12-bit up/down counter to carry out counting according to the indication of bits 2 and 3 (CSL0 and CSL1) of the flag register.
	U-1	C1024	" 1024	
	U-2	C512	" 512	
	U-3	C256	" 256	
	0	CN0	Counter bit 0 to 7	
	7	CN7		

(21) Work 58 register (WK5, WK6, WK7, WK8, WK58)

Register		Signal name	Description of the signal name	Function
Address	Bit			
13	0	WK580	Work 5 to 8 bit 0 to 7	This register is selected by bits 5 and 6 (WKSL0 and WKSL1) of the flag register to be used as a temporary register supplementary to another register.
	7	WK587		

Register		Signal name	Description of the signal name	Function
Address	Bit			
13	0 ⋮ 7	HS0 ⋮ HS7	High Speed 0 to 7	These bits are used as flag bit in a high speed rewinding routine.

(22) Jump condition (PH)

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
14	0	TP	Tape Present	This bit indicates "1" while the tape is passing the BOT/EOT sensor and it indicates "0" when the tape is completely wound on the file reel.
	1	LWTP	Low Tape	While the low tape sensor is continuously detecting the reflective marker this bit indicates "1".
	2 3	CTPA CTPB	Capstan Tacho Pulse A, B	Capstan tachometer pulses A and B
	4	SBOT	Sense BOT	This bit is set to "1" when the BOT marker is detected.
	5	SEOT	Sense EOT	This bit is set to "1" when the EOT marker is detected.
	6	FTPA	Full Tacho Pulse A	This signal has a cycle of capstan tachometer 4QTP.
	7			

(23) Set/Reset pulse signal (SETP)

Pulse signal 1		Signal name	Description of the signal name	Function
Address	Bit			
14	U-0			
	U-1			
	U-2			
	U-3			
	0	RNOIS	Reset Noise	The DNOIS reset signal.
	1	RUCHL	Reset Unit Check Hold	The Unit Check Hold reset signal.
	2			
	3			
	4	SIRPT	Set Interrupt	This signal carries out setting of an interrupt signal to the MTC.
	5			
	6	RTSFL	Reset Tester Flag	This signal is used to reset the mode for the tester when the ONLINE switch is depressed after the use of the field tester is completed.
	7	ESTDL	End Stop Delay	The signal to carry out synchronization of the capstan tachometer after terminating the stop delay.

(24) Jump conditions (OP)

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
15	0	ROMPE	ROM Parity Error	This bit is set to "1" when the PROM parity error is detected.
	1	RGPE	Register Parity Error	This bit is set to "1" when the Register LSI parity error is detected.
	2	RSTK	Reset Key	This bit is set to "1" when the RESET button is depressed.
	3	DOPN	Door Open	This bit is set to "1" when the front door is open.
	4	*HUBLK	Hub Lock	The signal to lock the auto hub.
	5			
	6	UNLK	Unload Key	This bit indicates "1" while depressing the UNLOAD button to execute the unload operation.
	7	LDRK	Load Rewind Key	When depressing the LOAD REWIND button this bit is set to "1" to execute auto loading, mid loading, or rewinding.

(25) Jump conditions (TSW)

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
16	0	*SW0	Tester Switch 0 to 7	Switch signal for the field tester.
	⋮	⋮		
	7	*SW7		

(26) Jump conditions (TJ)

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
17	0	TMOV0	Timer 0 Overflow	When the time register overflows this bit is set to "1" which is kept until the time register is loaded with a new value.
	1	TMOV1	Timer 1 Overflow	
	2	CNOV0	Counter Overflow 0	When the count register overflows at 256, this bit is set to "1" which is kept until the count register is loaded with a new value.
	3	CNOV1	Counter Overflow 1	When the count register overflows at 4096 this bit is set to "1" which is kept until the count register is loaded with a new value.

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
17	4	CARY	Carry	This signal is set to "1" if the arithmetic operation on X-Y and X+Y in the ALU results in X≦Y and no carrier in that turn, respectively.
	5	EQUAL	Equal	This signal is set to "1" when two inputs of the ALU are equal.
	6	TSFL	Test Flag	When operating the maintenance panel this bit is set to "1" and when the ONLINE switch is depressed this bit is set to "0".
	7	TST	Test Start	When the SSS switch is turned to ON this bit is set to "1" and when the SSS switch is turned on again this bit is set to "0". In mode setting this bit is also set to "0" after mode setting is completed.

(27) Interface register (IF)

Register		Signal name	Description of the signal name	Function
Address	Bit			
18	0	MISCE	Miscellaneous Error	The error signal to be set when the microprogram detects an error.
	1	TM	Tape Mark Detected	When a tape mark is detected by the skip file instruction this bit is set to "1".
	2	TOVRN	Tape Over Run	If a block or tape mark is not detected within 20 m when the space file instruction is executed this bit is set to "1".
	3	AGCON	Self Adjust Gain Control ON	The signal indicating that the SAGC operation is being executed.
	4	RDYHL	Ready Hold	The signal to be set by the rise of the READY status.
	5	TMOD	Test Mode	This signal is set to "1" by the set test mode signal from the FMT and the MTU is set in the inline mode.
	6	LWR	Loop Write to Read	This bit is set to "1" by the Loop Write to Read signal from the FMT, by which the Bus Out and Bus In are logically connected.
	7	LWR2	Loop Write to Read 2	This bit is set to "1" by the Loop Write to Read 2 signal from the FMT, by which the Bus Out and Bus In are connected through the write/read printed circuit board.

(28) Jump conditions (ITR)

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
19	0	*ONL	Online	This bit indicates "1" when the MTU is in the online status, and is reset by the RESET button or the UNLOAD instruction.
	1	INTRP	Interruption	The interrupt signal to the FMT
	2	UCHLD	Unit Check Hold	The signal for holding the state in which a hardware error occurs. This bit is reset by the RESET button.
	3	TUCHK	Tape Unit Check	This bit is set to "1" when a hardware error occurs while the servo is operating.
	4	GAPCT	Gap Control	The signal to direct the MTU to set an IBG. When the quarter tach pulse signal (QTP) is counted as many times as a prescribed number this bit is set to "1" and the signal is sent to the FMT.
	5	TWA	Tape Warning Area	When the EOT marker is detected during a forward run this bit is set to "1", and it is reset when the EOT is detected during a backward run.
	6	BOT	Beginning of Tape	When the BOT marker is detected this bit is set to "1".
	7	OD	Opposite Direction	This bit indicates "1" when the rotational direction of the capstan motor is opposite to the status of the MTU.

(29) Reel register (RL)

Register		Signal name	Description of the signal name	Function
Address	Bit			
19	U-0	KT	Start Time	The signal for measuring the start time of the capstan motor.
	U-1	STPCK	Stop Lock Check	The check signal for the stop control at the time the capstan motor is stopped.
	U-2	SP-KT	Stop Time	The signal for measuring the stop time of the capstan motor.
	U-3			
	0			
	1			
	2	FRF	File Reel Forward	The signal to rotate the file reel in the forward direction during the auto load or unload operation.
	3	FRB	File Reel Backward	The signal to rotate the file reel in the backward direction during the auto load or unload operation.
	4	MRF	Machine Reel Forward	The signal to rotate the machine reel in the forward direction during the auto load or unload operation.
	5	MRB	Machine Reel Backward	The signal to rotate the machine reel in the backward direction during the auto load or unload operation.

Register		Signal name	Description of the signal name	Function
Address	Bit			
19	6	RPWR	Reel Power	This signal is for supplying the reel motor with the drive current. When this signal indicates "0" the dynamic brake is applied to the reel motor.
	7	SLOW	Reel Slow	The signal to reduce the reel rotation speed during the auto load or unload operation.

(30) Jump condition (AL)

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
1A	0	RTLAL	Right Tape Loop Alarm	The LOOP ALARM signal for the right tape column.
	1	LTLAL	Left Tape Loop Alarm	The LOOP ALARM signal for the left tape column.
	2	HUBAL	Hub Lock Alarm	The hub lock error signal during the servo on operation.
	3	ECER	Erase Circuit Error	An error signal for the erase circuit
	4	WCER	Write Circuit Error	An error signal for the write circuit
	5	*WRIST	Write/Read PCA Installed	The signal for indicating that the connection of the write/read PCA is completed.

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
1A	6	HSCM	High Speed Control Machine	The speed up/down control signal from the machine reel circuit.
	7	HSCF	High Speed Control File	The speed up/down control signal from the file reel circuit.

(31) AGC register (AGC)

Register		Signal name	Description of the signal name	Function
Address	Bit			
1A	U-0			
	U-1			
	U-2			
	U-3			
	0			
	1	SAGC	Self Adjust Gain Control	The SAGC signal to the READ circuit.
	2	RDINH	Inhibit Read Data	The signal to suppress the read data during the GSD (Gain Step Down) operation.
	3	SSTEP	SAGC Step Pulse	The clock signal for the DGC amplifier control counter.
	4	LVL64	Slice Level 64%	The signal to set up the slice level of the read amplifier to 64%.

Register		Signal name	Description of the signal name	Function
Address	Bit			
1A	5	LVL90	Slice Level 90%	The signal to set up the slice level of the read amplifier to 90%.
	6	SET	Set	The suppression signal for the DGC amplifier control counter.
	7	PRESET	Counter Reset	The clear signal for the DGC amplifier control counter

(32) Jump conditions (MSW)

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
1B	0	*WDCLS	Window Closed Switch	The signal for indicating that the window is closed.
	1	CTGON	Cartridge ON	This signal is set to "1" when the cartridge is detected by the cartridge switch
	2	*CGOPN	Cartridge Opened	The signal for indicating that the cartridge is open.
	3	*CLINF	Column In File	The signal for indicating that the tape is in the right tape column.
	4	*CLINM	Column In Machine	The signal for indicating that the tape is in the left tape column.

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
1B	5	BVLM	Backward Voltage Limit Machine	The signal for indicating that the machine reel is being pulled by the file reel when the reels rotate in the backward direction under the auto load or unload operation.
	6	FVLF	Forward Voltage Limit File	The signal for indicating that the file reel is being pulled by the machine reel when the reels rotate in the forward direction under the auto load operation.
	7	*EMMVD	Error Marker Moved	The signal for checking an erroneous operation of an error marker.

(33) Jump conditions (F)

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
1C	0	STEP6	Step 6 All	The step signal for the DGC amplifier indicating that all the tracks have 6 or 7 steps.
	1			Not used at present
	2			
	3			
	4	STRMF	Streaming Feature	This signal indicates the MTU has the streaming function.
	5	ENITR	Enable Interrupt	The signal for controlling an interrupt signal.
	6	NEWF	New Function	This signal indicates the MTU has the streaming function or the skip file function.
	7	SKIPF	Skip File Feature	This signal indicates the MTU has the space file function or the back space file function.

(34) Jump conditions (WR)

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
1D	0	FP	File Protect	This signal indicates that the MTU is in the file protect status. In this status the MTU does not accept the write instruction or the erase instruction.
	1	WVON	Write Voltage ON	This signal indicates that the power for write has been set up.
	2	ECON	Erase Current ON	This signal indicates that the current flows through the erase head.
	3	6250F	6250 Feature	This signal indicates the MTU can be operated in the 6250 (GCR) mode.
	4	DDF	Dual Density Feature	This signal indicates the MTU has the two-record mode.
	5	AGCOK	SAGC OK	This signal indicates that all the track amplifications have been set up during the SAGC operations.
	6 7	VEL0 VEL1	Velocity Mode 0, 1	This signal defines the tape speed of the MTU.

(35) Jump conditions (BO, TMSR)

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
1E	0	BO0	Bus Out 0 to 7	The Bus Out signal from the FMT
	7	BO7		
	0	TMSR0	Time Sensor 0 to 7	The signal for detecting the amplitude of the read data (This signal is outputted when operating the field tester or when taking the initial diagnosis.)
	7	TMSR7		

(36) Jump conditions (TG)

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
1F	0	GOB	GO Tag B	This signal is set to "1" when TAG signal from the FMT is decoded and the GO TAG signal is sent out precisely. This signal carries out the speed control on the capstan motor.
	1	STS	Status Tag	The Status TAG signal and the Control TAG signal from the MTC;
	2	CTL	Control Tag	STS = 1, CTL = 0 ... Status Tag STS = 1, CTL = 0 ... Status Tag STS = 0, CTL = 1 ... Control Tag STS = 1, CTL = 1 ... Command Tag

Jump condition		Signal name	Description of the signal name	Function
Address	Bit			
1F	2	TMSR8	Time Sensor 8	The signal for detecting the amplitude of the read data (This signal is output when operating the field tester or taking the initial diagnosis.)
	3	DNOIS	Detected Noise	This bit is set to "1" when the noise data is detected.
	4	DBOB	Detected Beginning of Block	This bit is set to "1" when the block data is detected.
	5	DIBG	Detected Inter Block Gap	This bit is set to "1" when an IBG is detected.
	6	DTM	Detected Tape Mark	This bit is set to "1" when a tape mark is detected.
	7	0	Logical "0"	This bit always indicates "0".

3.4.5 The Executing Microprogram

The executing microprogram to control the MTU is functionally partitioned into 13 routines. Figure 3-6 shows the general relationship among routines. A description of each routine is shown in Figure 3-6 is as follows.

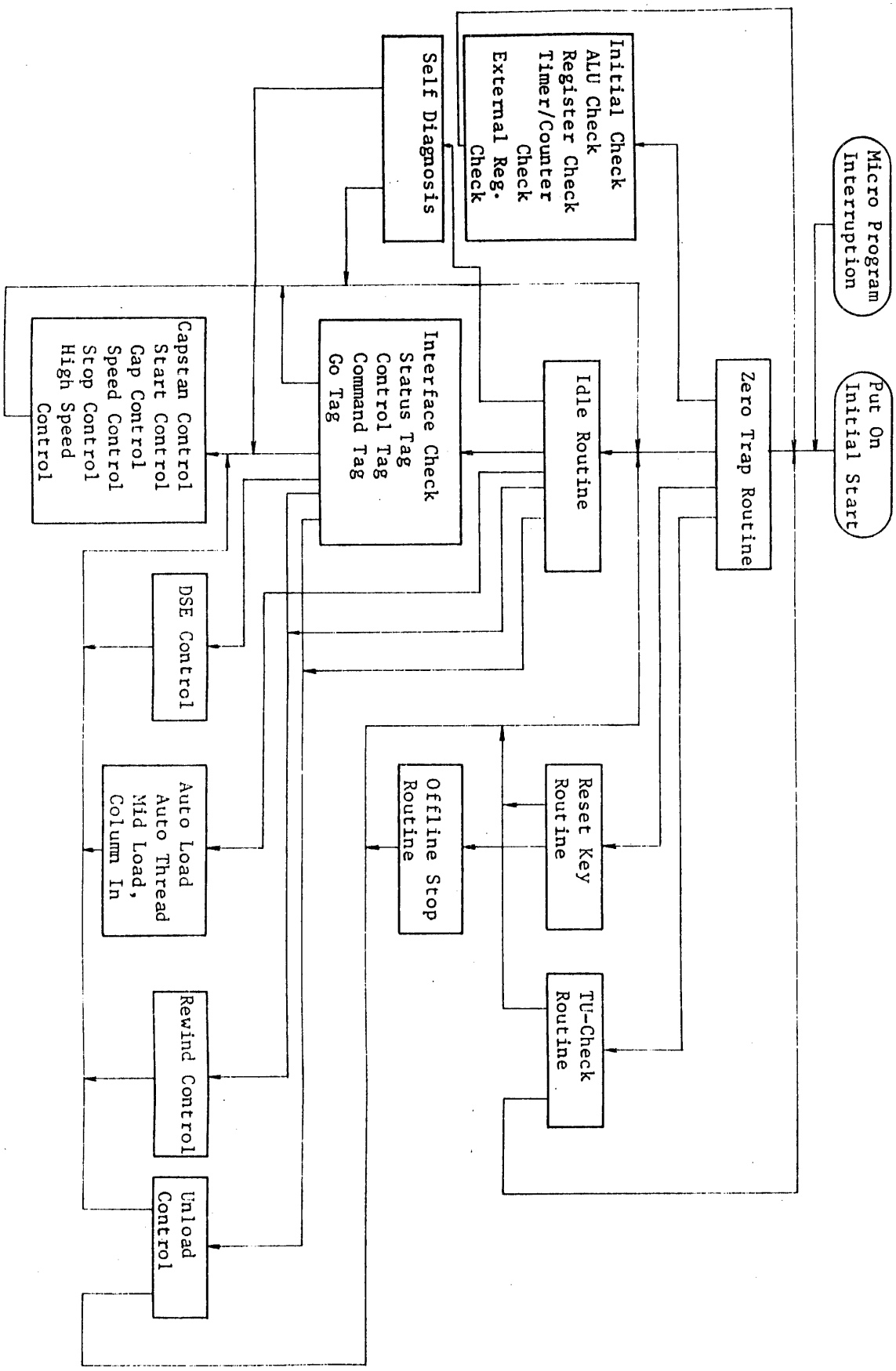


Figure 3-6. General flowchart of the microprogram.

(1) ZERO TRAP routine

The start address of this routine is 0. When the power supply of the MTU is turned on, the microprogram starts execution from this address 0. When the microprogram is interrupted, the execution address is forcibly set at address 0 to execute the main routine. An interrupt is caused by one of the following three conditions:

(a) MTU failure,
(b) RESET button on the operator panel is depressed, or
(c) Front door open.

The main routine checks the cause of the interrupt. To carry out error recovery processing, the execution jumps to the TU-CHECK routine if condition (a) is the cause of interrupt, to the RESET KEY routine if condition (b) is the cause of interrupt, and to the TU-CHECK if the interrupt is caused by condition (c).

In addition, when the microprogram is interrupted immediately after the power supply is turned on and the execution of microprogram has just started, the execution jumps to the INITIAL CHECK routine to carry out self checking of the hardware for the microprogram. When the cause of interrupt is released, the execution jumps to the IDLE routine, resulting in the waiting status of the MTU.

(2) INITIAL CHECK routine

First this routine carries out self-checking of the Arithmetic Logic Unit (ALU) . t When the ALU is found to be erroneous through the self-check, this routine reads out the command indicating the parity error. The ROM parity error is set, and the TUCHK (Tape Unit Check) status is set. If the ALU is normal, this routine executes the checkup of each register, timer, and counter, and further carries out the initial condition of each signal subject to jump conditions. If all the above items are normal, the routine issues the ALUOK signal.

This routine also initializes the cartridge opener (to be opened if the tape-present signal is detected and to be closed if no-tape-present signal is detected) and initializes the window.

(3) TAPE UNIT CHECK routine

This is the processing routine for the occurrence of MTU failure. This routine sets various error data and then causes the execution to jump to the IDLE routine.

(4) RESET KEY routine

This routine is started by depressing the RESET button. When started, the routine resets a predetermined signal and then causes the execution to jump to the OFFLINE STOP routine to stop the operation of the MTU. If the MTU is already in the halt status, the execution jumps to the IDLE routine.

(5) IDLE routine

When the MTU is in the wait status and carries out no action, this routine is executed repeatedly. When the MTU is in offline status, this routine monitors the buttons on the operator panel. When a button on the operator panel is pressed manually, this routine causes the execution to jump to the UNLOAD REWIND or the AUTO LOAD routine to start the specified operation. When operating the field tester, this routine causes the execution to jump to the SELF DIAGNOSIS routine. When the MTU is in the ONLINE READY status, the execution jumps to the INTERFACE CHECK routine.

(6) INTERFACE CHECK routine

This routine is executed when the MTU is in the READY status. The MTU sets or resets a required status by the Status Tag, Control Tag, or Go Tag signal.

(7) OFFLINE STOP routine

This routine stops the action of the capstan regardless of the presence of Inter-block gap (IBG). this routine is executed by depressing the RESET button during the tape run. It is also executed when the MTU in the ONLINE status receives a REWIND, UNLOAD, or Data Security Erase (DSE) command before the tape stops.

(8) AUTO LOAD routine

This routine causes the closing of the window and the action of the air motor and valve when depressing the LOAD REWIND button on the operator panel. If the cartridge is on, it is opened.

After the rise time of air passes, this routine rotates both reels clockwise, detects a tape-present signal, and again rotates the reels a few times when the tape is wound on the machine reel to switch the valve.

The reels are continuously rotated until BOT is detected, and the tape is fed into the tape column. When the tape is fed in the tape column, the capstan motor is driven in the forward direction. When the BOT passes the BOT sensor or when a certain time passes after drive in the forward direction, the capstan motor is driven in the backward direction until BOT is detected. When BOT is detected, the motor stops and tape loading is completed.

During mid-load operation, the COLUMN IN and remaining actions are the same as those in the auto load operation.

(9) UNLOAD routine

When the MTU is in the servo on status, this routine is executed by depressing the UNLOAD button in offline or when the MTU receives an UNLOAD command.

This routine resets the READY state, checks if BOT is detected, and if BOT is not detected, the execution is jumped to the REWIND routine. If BOT is detected, the routine causes the tape to feed in the backward direction as far as a certain predetermined distance, to set the servo off, and to wind up the tape from the tape column. After winding the tape, it is wound on the file reel until no tape present signal is detected. The UNLOAD operation is then completed.

When the MTU is in the servo off status and the tape is placed within the cartridge, the cartridge is closed and the window is opened by this routine.

(10) REWIND routine

To carry out the rewind operation this routine performs the necessary processing and causes the execution to jump to the CAPSTAN CONTROL routine. This routine primarily resets the write/erase status to operate the tape cleaner.

(11) DSE routine

When the MTU receives a Data Security Erase (DSE) instruction, this routine carries out the erase status check and causes the execution to jump to the CAPSTAN CONTROL routine.

(12) CAPSTAN CONTROL routine

This routine carries out control on the capstan motor. Control is differentiated into the following five items:

(a) A predetermined drive current is applied to the capstan motor to start tape feeding. Capstan tachometer check is carried out.

(b) Since the Gap Control signal must be issued to the FMT at an appropriate timing to carry out the IBG control in execution of the usual write/read command, the length of IBG is set up so that the Gap Control signal is set according to a predetermined value.

(c) The current value to the capstan motor is determined according to the quantity of deflection from the reference speed.

(d) The capstan rotation is controlled so that, after the Go signal is reset, the tape runs through a predetermined distance (called the Stop Delay) at a constant speed. The written data is checked and the tape stops at the specified position within an IBG. The decelerating current is controlled to stop the tape within a certain distance.

(e) Control for high-speed tape rewinding.

(13) SELF DIAGNOSIS routine

This routine executes various actions done through manual operation of the field tester.

3.5 Maintenance Functions Using the Field Tester

Connecting the field tester to PCA IC05 makes it easy to carry out maintenance inspection and alignment work. Refer to Part I of the Maintenance Manual for information on operation and use of the field tester.

3.6 Capstan Control Circuit

3.6.1 Introduction

Figure 3-7 shows the capstan control circuit. Each section of the circuit is described in the following paragraphs.

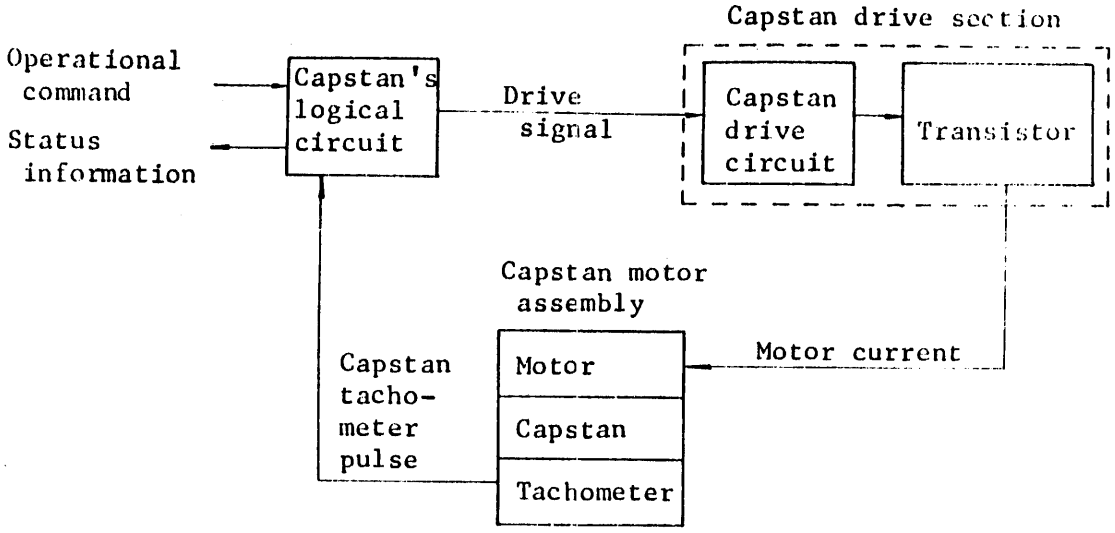


Figure 3-7. Capstan control circuit network.

3.6.2 Capstan Motor Assembly

The capstan motor assembly contains a DC motor with low inertia capable of generating a high-output torque into which a tachometer and a capstan are united. Figure 3-8 shows a scheme of the capstan motor assembly.

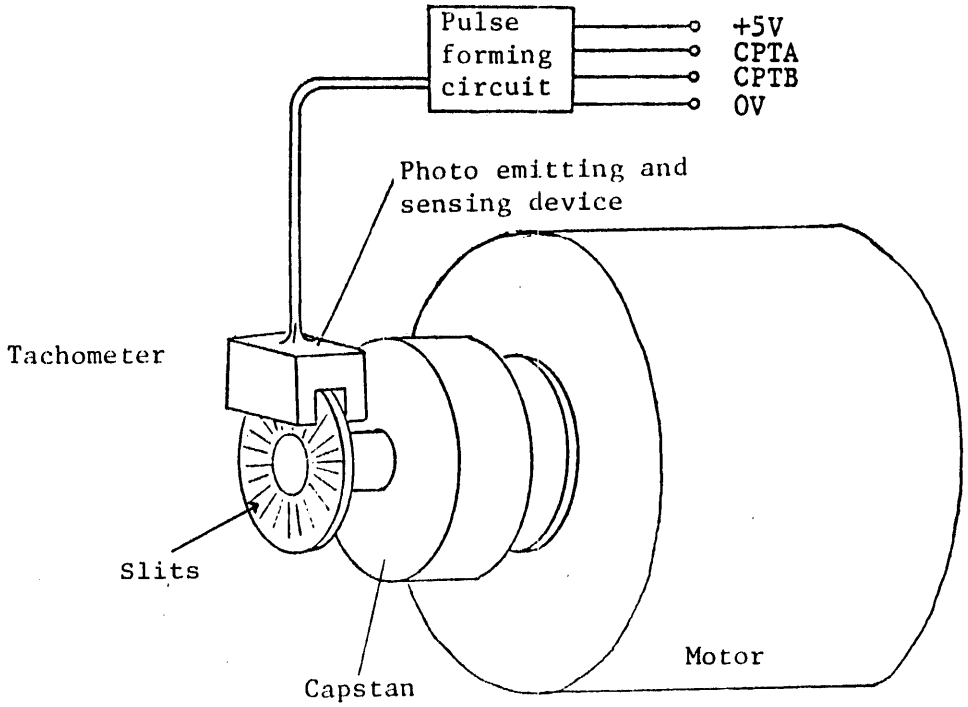


Figure 3-8. Capstan motor assembly.

The capstan surface is coated with the special material to increase the friction with tape. Avoid touching the surface of the capstan.

The tachometer section consists of a disk fixed to the motor axle and a photo emitting and sensing device fixed to an external structure. The disk is provided with 500 radial slits. this slit-engraved disk is rotated with the motor axle to allow the motor rotation to be converted into an electric signal. When the DC motor runs at a speed of V1 m/s, the pulse forming circuit generates repetitive pulses of V2 KHz.

	Running speed V1 (m/s)	Pulse Frequency V2 (KHz)	Pulse Period T1 (ms)
75 ips	1.905	7.958	125.66
125 ips	3.175	13.263	75.40
200 ips	5.08	21.222	47.12

To detect the rotational direction of the motor, a photo detecting device is placed at the position where the phase differs by 90° from the rotational direction. The pulses output from this photo detecting device are signals Capstan Tachometer Pulse A and B (CTPA) and (CTPB) (Refer to Figure 3-9). When the tape runs in the forward direction, the phase of signal CTPB leads that of signal CTPA by 90°, while the former lags the latter by 90° when the tape runs in the backward direction. Signal CTPA is used to measure the tape speed. Signal Quarter Tachometer Pulse (QTP), generated at every changing edge of signals CTPA and CTPB, is used to measure the length of the running tape. Since the diameter of the capstan is 1.5 inches long and the number of slits engraved on the disk is 500.

$$1QTP = \frac{\pi \times 1.5}{500 \times 4} = 0.002356 \text{ inch} = 0.060 \text{ mm}$$

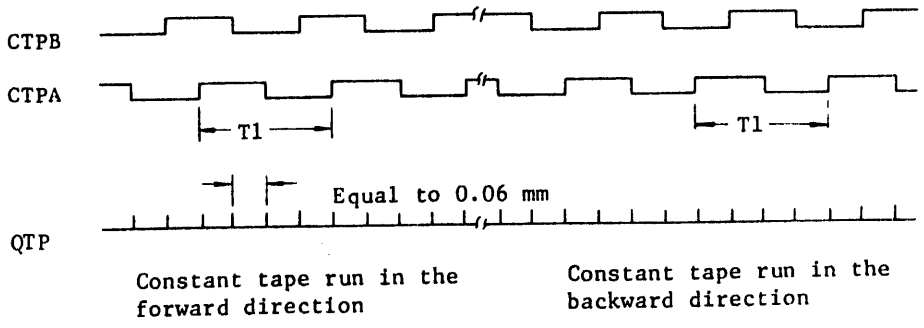


Figure 3-9. Tachometer pulse signals.

3.6.3 Logical Circuit

The capstan logical circuit receives an external command signal, and the tachometer pulse as input signals, issues the drive signal to the capstan drive section to send the operational status of the capstan as status information to another logical circuit.

The operation of the capstan logical circuit is described for each block in the following paragraphs. The relationship among the blocks is illustrated in Figure 3-10.

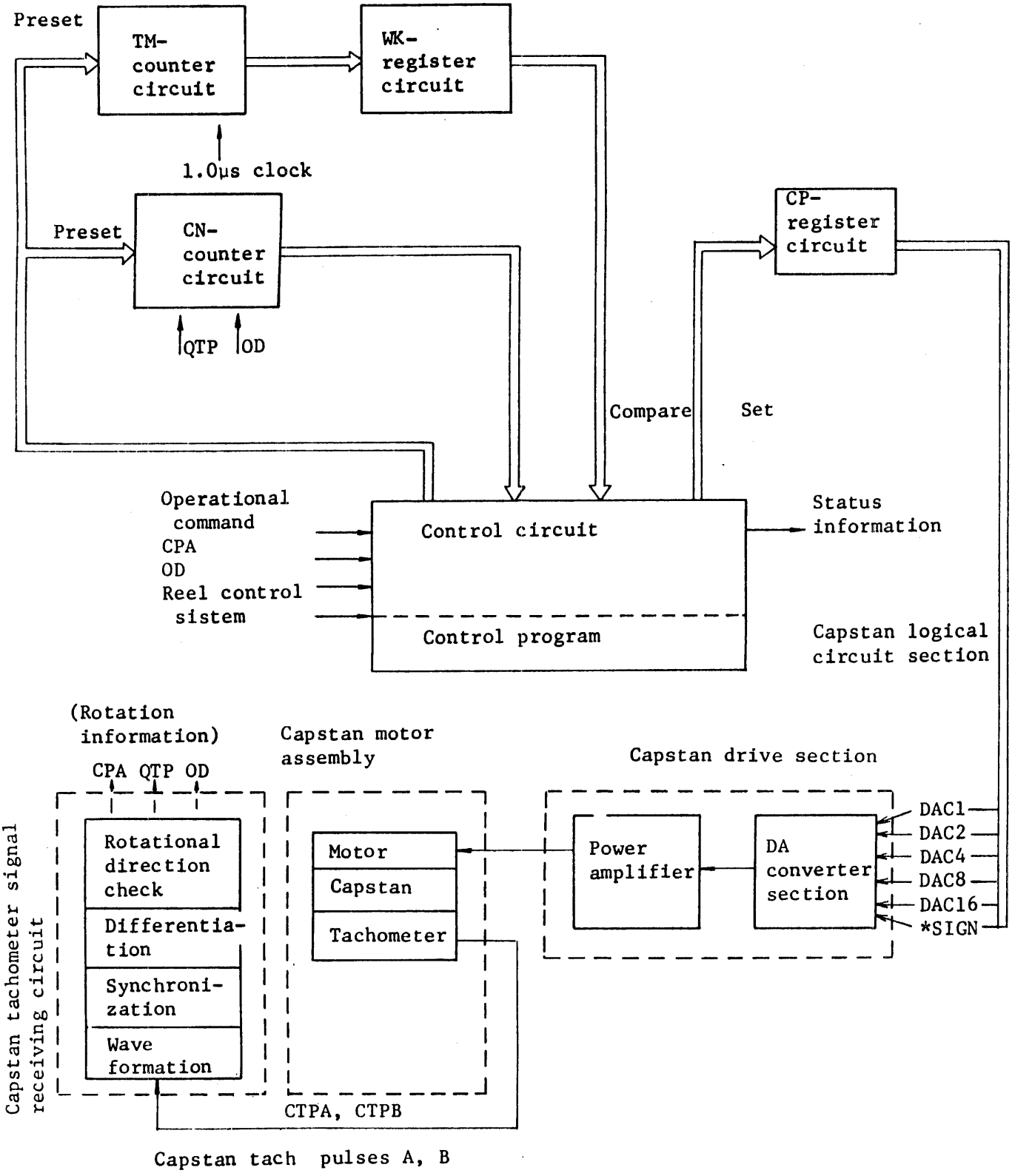


Figure 3-10. Block diagram of capstan control circuit network.

(1) Capstan tachometer signal receiving circuit

In the 6250 rpi mode, the length of IBG is 7.62 mm, which is one-half that used in the 800/1600 rpi mode. The allowance for the stop position is tight. To meet such tight requirements two circuits are provided for the capstan tachometer to upgrade the precision of tape-feed detection and to enable the MTU to detect the tape-feed direction.

The capstan motor issues tach pulses A and B with a 90° phase difference. When the capstan motor is rotated in the forward direction, pulse A lags pulse B; in the backward rotation the phase relationship is reversed. Tach pulses CTPA and CTPB (Capstan Tacho Meter Pulses A and B) output from the capstan motor enter the wave forming circuit where they are converted into signals CPA and CPB. These signals are input to a flip-flop circuit to be synchronized with the clock. Another flip flop is added to generate a signal having one clock lag over the preceding signal. This phase-delayed signal and the preceding no-delay signal are used together to produce pulses that are initiated at the rise and fall of each tach pulse.

Signal QTP (Quarter Tach Pulse) is initiated at the rise and fall of signal CTPA and at the rise and fall of signal CTPB, respectively, as shown in Figure 3-11. Signal FTP (Full Tach Pulse) has a cycle 4 times longer than that of signal QTP.

Signal OD (Opposite Direction) indicates the rotational direction of the capstan. This signal OD is produced by making a phase comparison of signals CTPA and CTPB to detect the rotational direction and by comparing it with the capstan drive direction signal. When signal OD indicates "0", it means that the drive direction of the capstan is in agreement with its rotational direction. When signal OD indicates "1", the directions are opposite to each other.

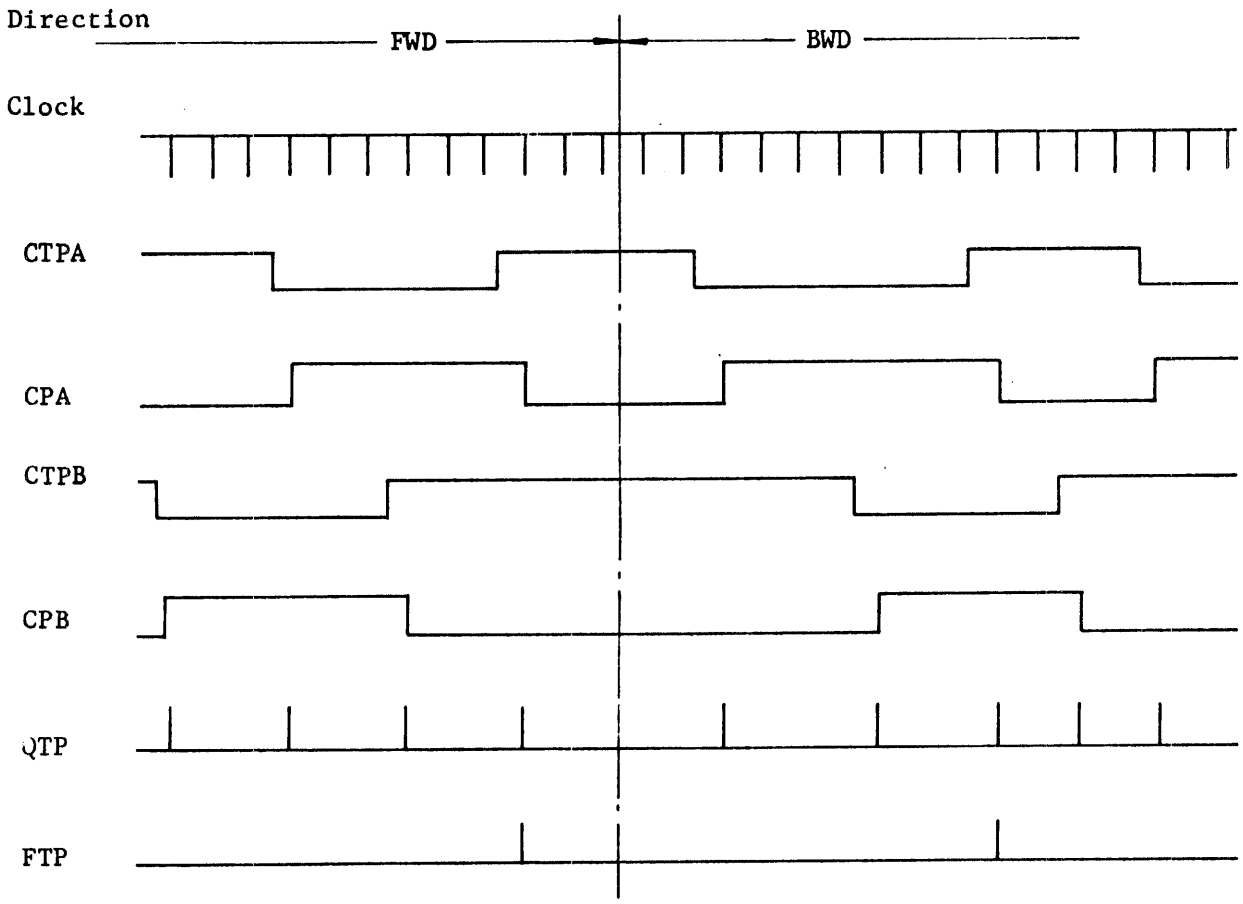


Figure 3-11. Time diagram of capstan tach pulses.

(2) TM-counter circuit

This counter consists of 8 bits to measure the time interval of a pulse cycle. For the speed control and high-speed control, the time interval (one tach pulse cycle) of signal FTP is measured using the clock of approximately 1.0 μs.

(3) CN-counter circuit

This counter is a 12-bit up/down counter used to control tape position. During such control, this counter counts the positional signal QTP while comparing it with the running direction signal. The counting is additive when the changing direction of tape position is in agreement with the tape running direction. The counting is subtracted when those directions are opposite to each other.

(4) WK-register circuit

This register consists of 8 bits. In the speed control, this register holds the final count number on the TM counter and sends it to the control circuit. The value sent to the control circuit is compared with the reference signal for the capstan motor speed. The current value for the capstan motor is set in the CP register.

(5) CP-register circuit

In speed control and high-speed control, the current value for the capstan motor is set up according to the speed control data sent to the control circuit from the WK register. The content of this CP register consists of a 6-bit signal DAC1, DAC2, DAC4, DAC8, DAC16, and *SIGN which is sent to the capstan drive circuit and becomes the input signal to the DA converter.

(6) The control circuit

This circuit sets the data on a counter or register according to the control microprogram or an appropriate processing according to the content loaded in a counter or register.

3.6.4 Operation of the Servo System

The role of the capstan motor control is to:

- Keep the capstan motor speed constant. Speed control is necessary during the write/read operation.
- Make out the IBG, which has a given length for the write operation, and to make the capstan motor speed constant for the read operation before data is output. In other words, both the start transient of the motor (the rise transient from the zero speed to constant speed) and the stop transient of the motor (the fall transient from constant speed to speed zero) are completed within the IBG. This is called the position control.

- Carry out high-speed rewinding. During this high-speed control, high-speed rewinding is executed while keeping in connection with the reel control circuit operation so that the tape will not run out of the tape column.

(1) Speed control

Speed control includes the control for the start transient operation, the stop transient operation, and that for constant-speed operation. Speed control is somewhat different for each of these operations.

Figure 3-11 explains the speed control. the cycle of a tachometer signal inversely proportional to the tape speed. The cycle of tachometer signal FTP is measured by the TM-counter, where the TM-counter is preset at the time of count start. when the tape runs at constant speed A, one cycle of signal CTPA is C, as shown in Figure 3-10, so that the final count value on the TM-counter is:

	Preset value	Counted value		
70 ips	(8	+ 126)	÷ 1	= 134
125 ips	(56	+ 75)	÷ 1	= 131
200 ips	(85	+ 47)	÷ 1	= 132

(1.0μs for one clock)

Speed	Running Speed A (m/s)	FTP Period B (μs)
75 ips	1.905	125.66
125 ips	3.175	75.40
200 ips	5.080	47.12

The WK register holds the final count value on the TM counter. The value held in the WK-register is sent to the control circuit where the speed comparison is carried out. The value of the current for the capstan motor is set in the CP register and sent to the capstan drive assembly. The output of the DA converter installed in the tape drive circuit provides the value of the current and that of the voltage necessary to make the capstan motor rotate at constant speed A. If the capstan motor speed is lowered, the final count value increases, thereby producing a greater output voltage to increase the motor speed.

(2) Position control

The normal length of IBG in the 6250 rpi mode is 7.62 mm (0.3 inches), and 10.16 mm (0.4 inches) in 200 ips MTU write mode. Accordingly, the start and stop operations of the capstan motor must be completed within this length. The length of IBG can be represented by the number of pulses of QTP, as follows:

$$\frac{7.62\ \text{mm}}{0.06\text{mm}} = 127, \quad \text{or} \quad \left(\frac{10.16\ \text{mm}}{0.06\ \text{mm}} = 170\right) \text{ in the case of 200 ips MTU}$$

The above value will be denoted as 127 QTP (170 QTP) hereinafter. I QTP corresponds to 0.06 mm. The usual start and stop lengths are set at 32 QTP and 36 QTP (59 QTP and 48 QTP) respectively.

The method of preparing IBG when the write operation is carried out in the 6250 rpi mode is as follows (refer to Figure 3-12):

Step (1) When writing terminates, the capstan drive signal GO is reset. Then, the CN-counter is preset at 207 (204). The motor speed remains constant for checking the written data, and the CN counter counts the number of pulses QTP. That period is called Stop Delay.

Step (2) When the CN-counter counts 256, the process enters the deceleration. The CN-counter is again preset at 92 (80) after the motor runs as far as 1 QTP to make synchronization. Since the motor is turned to stop while conducting the speed control, the speed reaches zero when the CN-counter counts 36 QTP (48 QTP). When the capstan makes the complete stop the CN-counter counts 92 + 36 = 128, (80 + 48 = 128).

Step (3) Since the position control on the capstan operation is carried out so that once the capstan stops, the CN counter can hold value 128 even if the external force is applied to the capstan, the tape will be locked.

Step (4) When signal GO is set, the capstan motor starts rotating at normal speed. Speed control starts, and the CN counter is added by 96 (69).

Step (5) When the CN counter counts 32 QTP (59 QTP) (= counter value of 256), a GAP Control signal (GAPC) is sent out to the FMT. At about the time this signal is set, the capstan reaches normal speed.

Step (6) When the FMT receives the gap control signal, the FMT monitors the capstan speed. When the FMT ascertains the speed is correct, the write operation starts after approximately 10 QTP.

Writing is carried out such that the length of IBG is given in terms of QTP units, as follows:

(256 - 208) + 1 + (128 - 92) + 32 + 10 = 127
[(256 - 204) + 1 + (128 - 80) + 59 + 10 = 170]
Stop Delay Stop Start Check

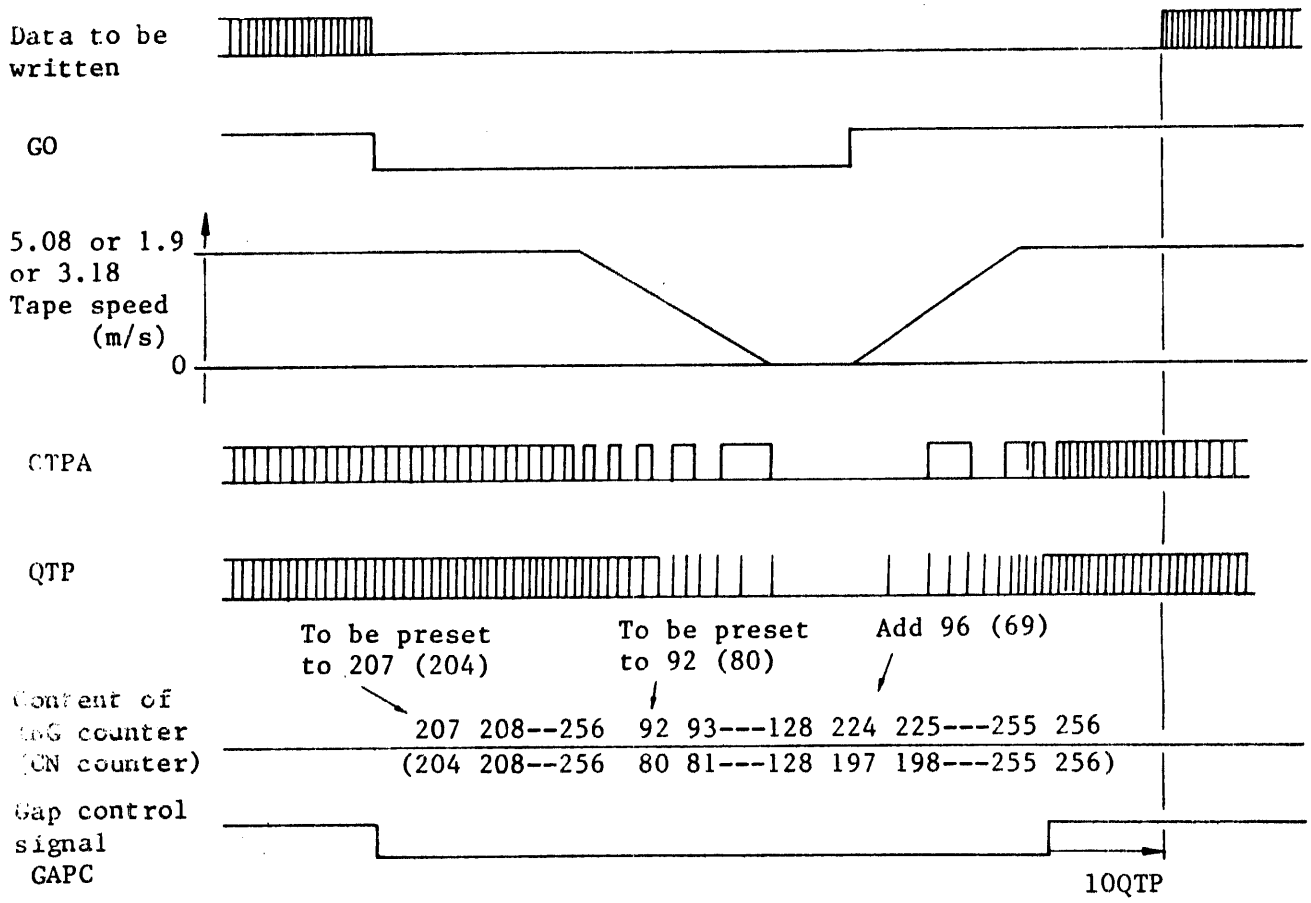
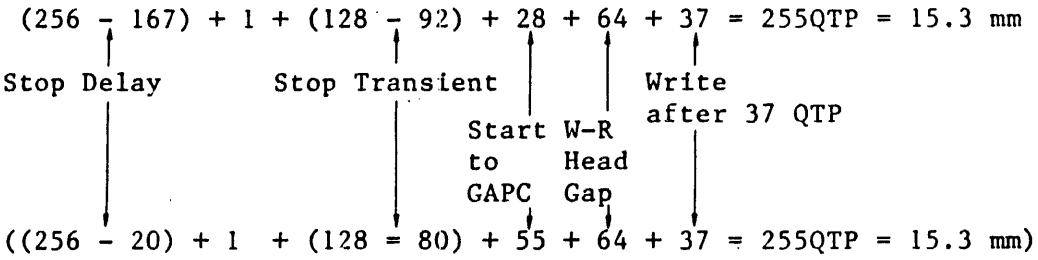


Figure 3-12. Preparing the IBG (6250 rpi mode).

In the 1600 rpi mode, writing is carried out in the same manner as in the 6250 rpi mode. A distance of 64 QTP between the write head and the read head is added to the length of IBG set up for the 6250 rpi mode because the signal GO is reset after checking the written data terminates.

In the 1600 rpi mode, the start/stop distances are different from those in the 6250 rpi mode. The length of IBG is 15.3 mm where the stop delay is 90 QTP.



When signal GO is set for chaining, the status at step (1) or step (2) is moved step (4). When the forward hitch is performed, the CN counter subtracts while feeding the tape in the forward direction. The term "forward hitch" refers to the operation to feed the tape by some small distance in the forward direction when starting the capstan motor in the backward direction. This forward hitch is performed when the stop time before starting the capstan motor in the backward direction is long.

The term "chain" means to carry out the next start transient operation before the motor completely stops. Here, the chain is used when the start operation is made in the same running direction. The chain is not used when the start operation is made in the opposite direction, that is, from the forward to the backward, or vice versa. In such cases, the chain is made after the capstan motor stops. The tape speed variation appearing when the chain is applied is shown in Figure 3-13.

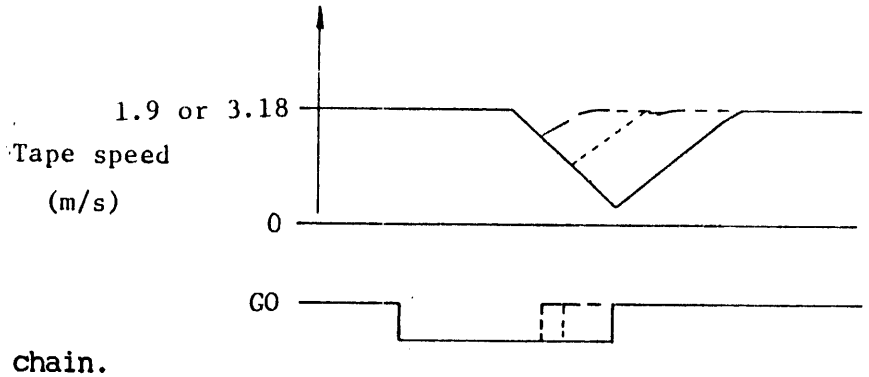


Figure 3-13. The chain.

(3) Operation in the High-Speed Mode

In conventional MTUs or in the normal-speed mode, the sum of the length of tape for the start transient operation and the length of tape for the stop transient operation is shorter than the length of the IBG. The start/stop operations must be done within IBG. To achieve high-speed performance, more advanced structure is required for the motor drive circuit, the drive system mechanism, and so forth.

In the MTU, high-speed operation is based on the 75/125 ips mechanism. this mechanism is capable of achieving the 125/200 ips high-speed performance.

In the high-speed mode, the tape continues running at a constant speed for a certain time, assuming that the same command will be issued immediately after the data block processing is completed. When a command is issued within this time, the MTU keeps executing the processing on the next block without changing the 125/200 ips mode.

If the MTU fails to issue the command within the time in which the tape continues running at constant speed, positioning control is applied, as shown in Figure 3-14. The capstan motor returns to the position where the motor can reach a normal speed so that the MTU can access data when the next command is issued.

Table 3-5. Timing of access.

(Unit: ms)

Item \ MTU and commands			M2430L M2431L M2434L1/L2		M2432L M2433L M2435L1/L2	
			READ	WRITE	READ	WRITE
Normal mode	Access Time	6250 rpi	2.6	2.3	1.6	1.5
		1600/800 rpi	4.0	3.0	2.6	2.0
Streaming mode	Reinstruction Time	6250 rpi	2.2	1.0	1.3	0.55
		1600 rpi	4.6	3.4	2.8	2.05
	Positioning Time		12.3	22.9	9.5	17.3
	Access Time		6.9	5.7	4.5	3.7
	Repositioning Time		19.2	28.6	14.0	21.0

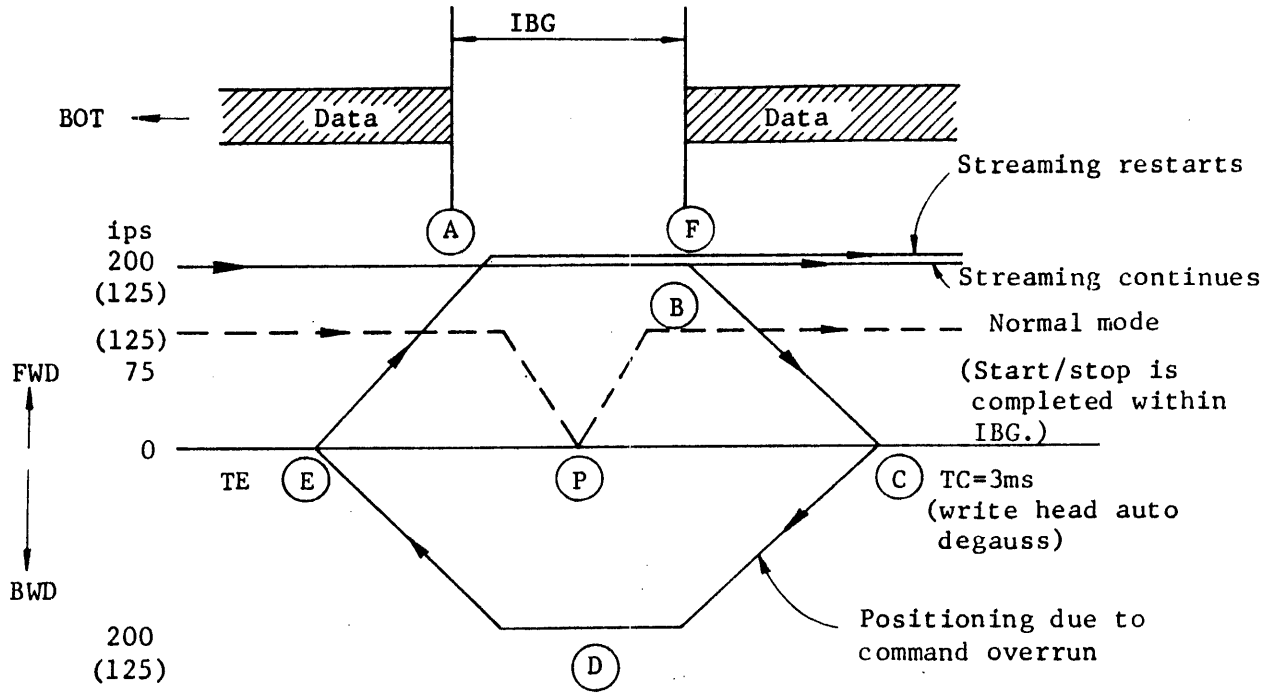


Figure 3-14. Streaming mode operation.

Refer to Figure 3-14 for the following terms.

Reinstruction Time, A —> B

Streaming continues after the command operation is completed if the next command is issued within this time range. If the next command is issued after the reinstruction time, 0-positioning is applied. The FMT requires 0-.2 ms for command end processing.

Positioning Time, B —> C —> Tc —> D —> E

When reinstruction time overrun occurs, the tape moves to the waiting point (E).

Auto Degauss Time, Tc

In the write positioning, the auto degauss is carried out on the write head for 3 ms at point (C).

Turnaround Time, Te

Refers to point E in Figure 3-14. For models M2432L, 3L, 5L, and 6L, if the command that directs the reverse operation to maintain the stable tape loop, servo operation, and backward commands is issued, and if the halting time is excessive, 400 ms is set and the tape starts.

Access Time, E —> F

The access time begins from the time at which the MTU receives a command in the waiting status at point (E), reaching point (F), to the time at which data transfer starts.

Repositioning Time, B —> C —> D —> E —> Te —> F
(TC)

Positioning Time + Access Time = Repositioning Time.

When a command overrun takes place in the high-speed mode, a certain amount of processing time (for repositioning) may be lost, as indicated in Table 3-5 even though a read/write command is issued immediately after the reinstruction times. The efficiency of the high-speed operation depends on the number of blocks to which the command chain can be applied, the length of one block, and the recording density of tape. The efficiency of the high-speed mode is sometimes lower than that of the normal-speed mode.

(4) High-Speed Control

High-speed control is carried out in connection with the reel control circuit operation. In general, the capstan motor is superior to the reel motor in terms of its ability to follow at high speed. Accordingly, the high-speed control is designed to control the speed of the capstan motor by using the signal from the reel control circuit. When the reel motor drive section has adequate capability of accelerating the reel motor, the capstan speed is increased. The capstan speed is decelerated if the reel motor drive section does not have adequate capability of accelerating the reel motor or when a low tape signal (LTP) is detected near the end of a rewind operation.

During high-speed control, the TM counter is reset and the capstan motor speed is controlled by measuring the time interval of the FTP signal two or more times, so that the total cycle time reaches 236 s. For example, if the control is carried out so that 5 cycles of FTP signal takes 236 s, the tape speed reaches 5.08 m/sec (200 ips). If the control is carried out so that 15 cycles of FTP signal takes 236 s, the tape speed reaches the maximum speed of 15.24 m/sec (600 ips). 12.7 m/sec (500 ips) are required for the 200 ips MTU. Figure 3-15 is a time diagram of FTP signal pulses.

Acceleration and deceleration of the capstan motor is controlled by a signal from the reel control circuit. If the reel motor drive section has adequate capability of accelerating the reel motor, the capstan motor is accelerated from 5.08 m/sec to 15.24 m/sec (12.7 m/sec) at a step of 1.016 m/sec. Otherwise, the capstan motor is decelerated.

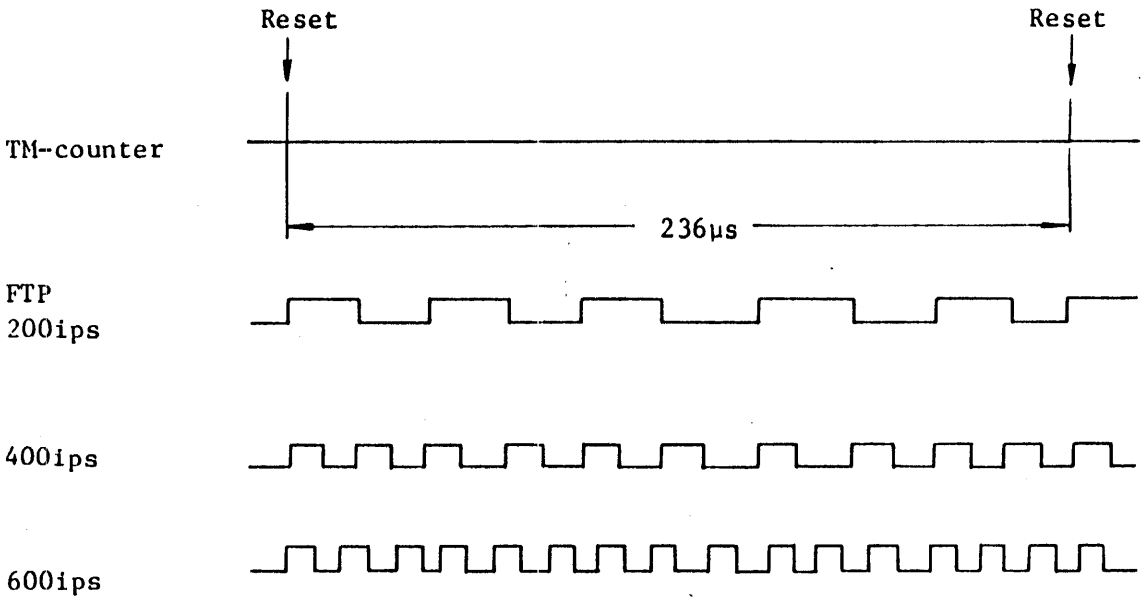


Figure 3-15. CPA signals under high-speed control.

3.6.5 Capstan Drive Circuit

The capstan drive assembly consists of two special printed-circuit assembly (PCA) packages. One of the two packages is called "tape drive circuit B or H," which is also referred to as PCA 1A04. This package includes the file and machine reel drive control sections.

The second package is called "transistor circuit A" or tape drive A PCA. This PCA encompasses the power amplifier and is fixed to the lower part of the side board of the MTU. Tape drive A PCA is the circuit for converting a digital signal into an analog voltage and appliers power amplification to the analog voltage to drive the capstan motor.

Figure 3-16 is a block diagram of the capstan drive circuit. (See the Maintenance Manual PCA Location Charts for nomenclature and location of all printed circuit assemblies.)

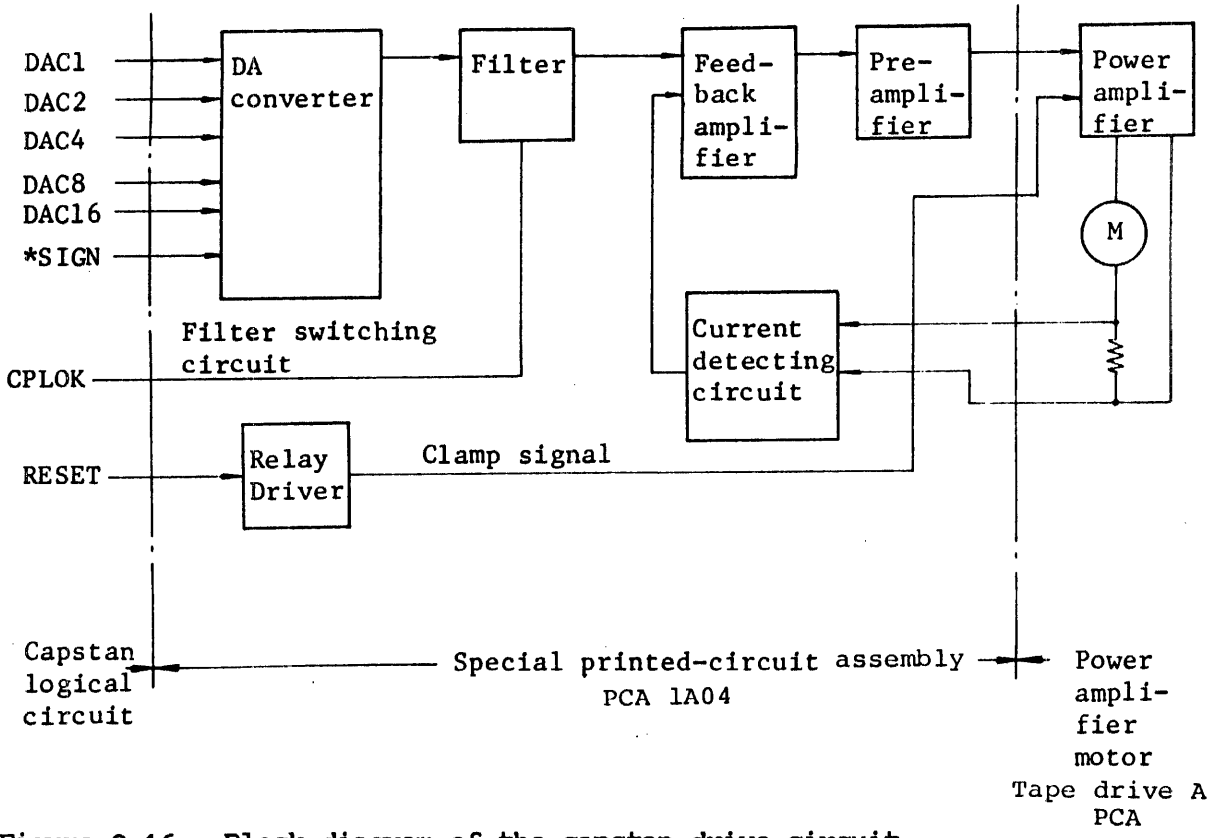


Figure 3-16. Block diagram of the capstan drive circuit.

The motor current digital signals DAC1 through 16, and SIGN are converted by a digital-to-analog (DA) converter into an analog voltage, which then passes through a filter. This filter receives signal CPLOK when the capstan motor stops and its frequency characteristic changes. When the analog voltage passes through this filter, it is amplified and applied to the capstan motor. The current that flows into the motor is converted into a voltage by the current detecting circuit and fed back to the feedback amplifier. As a result, the motor current is determined completely by the signal from the logical circuit.

The relay used in the capstan drive circuit protects the capstan motor from causing a faulty operation at the time of power on and off.

The transistor circuit comprises a power amplifier for driving the capstan motor. A schematic of the power amplifier is shown in Figure 3-17. A logical signal sent from the capstan logical section is converted by the tape drive circuit B into an analog voltage (DA converter) and applied to the power amplifier input IN1 and IN2. Signals IN1 and IN2 have opposite polarities.

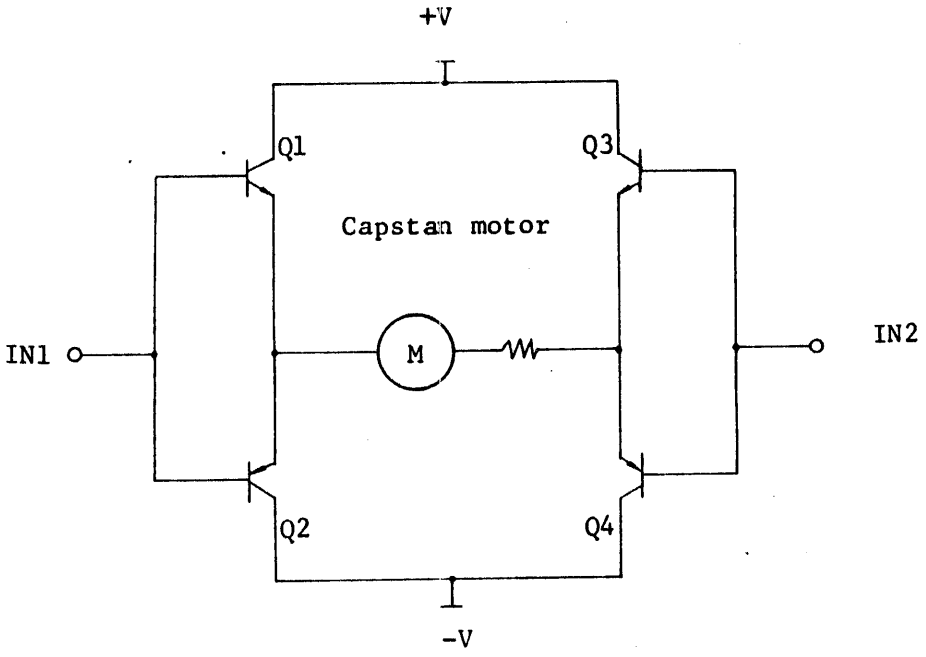


Figure 3-17. Schematic of the power amplifier.

3.7 Reel Control Circuit

3.7.1 Reel Motor and Tape-Loop Detection

The reel motor uses a permanent magnet exciting DC servo motor. Driving, coasting, or braking is applied clockwise or counterclockwise to keep the tape in an appropriate state inside the vacuum tape columns.

As the position detector for the tape loops inside the vacuum tape columns, a capacitive sensor is used to convert the variation of pressure distribution along the tape loop into the variation of electrostatic capacity. The structure of the capacitive sensor is shown in Figure 3-18.

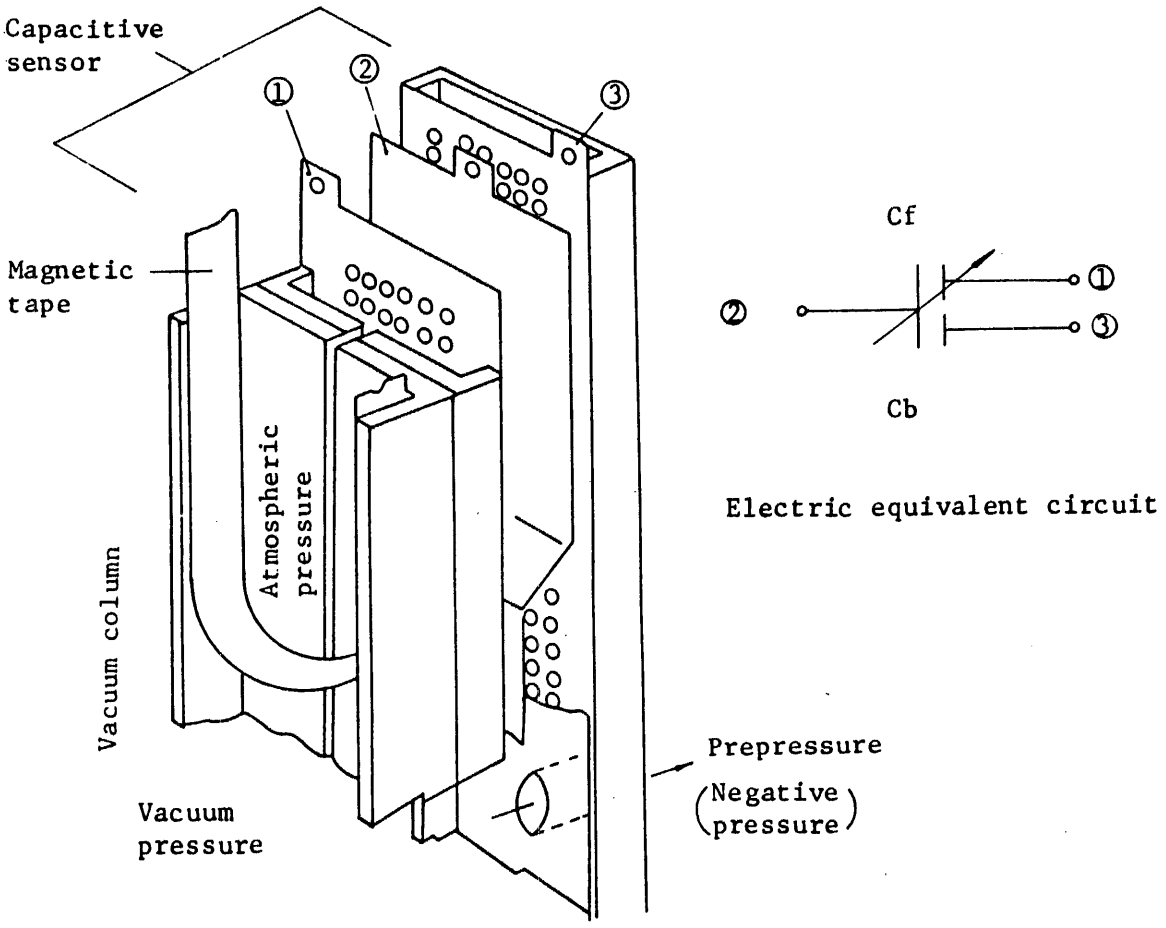


Figure 3-18. Capacitive sensor and its equivalent circuit.

The front plate of the capacitive sensor contains arrays of holes in the long direction. A fixed electrode (1) with many holes is located on the inner side of the sensor. The rear surface of the sensor is provided with an air inlet opening. Another electrode (3), similar to electrode (1), is located on the inside rear surface.

The middle part inside the sensor contains a movable foil electrode (2), which divides the inside of the sensor into the front part and the rear part. The movable electrode (2) and the fixed electrode (1) together form a variable capacitor C_f. The movable electrode (2) and the fixed electrode (3) together form another variable capacitor C_b.

On the back surface of the vacuum column a long, narrow groove is engraved in the long direction. The groove contains small holes prepared so that holes on the front plate of the capacitive sensor can open into the inside of the vacuum column through the holes in the groove. The pressure distribution in the front part of the inside of the sensor becomes the same as that inside the column.

The low negative pressure (which is called the pre-pressure) is lower than the vacuum pressure inside the vacuum column. The pre-pressure is supplied to the rear half of the inside of the sensor from the air inlet passing through the rear wall of the sensor. If the pressure inside the column is equal to atmospheric pressure, the pressure in the front part of the inside of the sensor is equal to atmospheric pressure. As a result, the movable foil electrode (2) is attracted by the pre-pressure in the rear part of the inside space of the sensor and moved backward. The movable electrode (2) is moved forward toward the column when the pressure inside the column is vacuum pressure because vacuum pressure is lower than the pre-pressure. As the electrode (2) moves toward the column, the space between the electrode (2) and the fixed electrode (1) becomes narrow and the electrostatic capacity between these electrodes increases. The distance between the fixed electrode (3) and the movable electrode (2) becomes wider and the electrostatic capacity between these electrodes (3) and (2) decreases. However, because this increment and decrement of electrostatic capacity are the same in absolute value, their sum is always constant.

Consider the case where the tape loop is located in the middle of the vacuum column. The pressure above the tape loop in the column (on the side of column entry) equals atmospheric pressure, so that the upper half of movable electrode (2) moves in the direction opposite to the column. On the other hand, the pressure below the tape loop (on the bottom side of column) equals the vacuum pressure, and the lower half of movable electrode (2) moves toward the column. Since the area of the upper half of the movable electrode (2) is equal to that of the lower half, the electrostatic capacity C_f between electrodes (2) and (1) equals the electrostatic capacity C_b between electrodes (2) and (3). If the tape loop is located above the middle of the column, the space of vacuum pressure below the tape loop in the column becomes wider, and the movable area of the lower half of movable electrode (2) toward the column becomes large. The electrostatic capacity of the capacitor increases as the distance between electrodes is reduced and the areas of the surfaces of electrodes are large. Accordingly, the electrostatis capacity C_f between two electrodes (2) and (1) increases. As a consequence, the area the movable electrode (2) moves in the direction opposite to the column decreases, so that electrostatic capacity C_b between two electrodes 2 and (3) becomes small. If the tape loop is located below the middle of the column, the situation is opposite to the above, resulting in the decrease of C_f and the increase of C_b.

Thus, change of location of the tape loop inside the vacuum column causes a change in pressure distribution inside the column. the area of movement of the movable electrode is changed, and the electrostatic capacity changes in proportion to the change of the moved area. In the reverse direction, the location of the tape loop can be detected by measuring the variation in this electrostatic capacity. However, to reduce an error caused by the variation in electrostatic capacity of the sensor, the difference between two electrostatic capacities C_f and C_b is measured.

Loop position detecting holes are provided at the entry and bottom of the vacuum column. One hole at the entry is connected to the high-pressure terminal of the vacuum switch; the other to the low-pressure terminal of the same vacuum switch. The difference in pressure between these two high and low pressure terminals is used to set the mechanical point switch to on and off to detect the tape loop position. when the tape loop is located above the detecting hole at the entry portion of the column the vacuum pressure is applied to both pressure terminals. Since there is no pressure difference between the terminals, the mechanical switch is off while when the tape loop is located below the detecting hole at the entry portion of the column. the atmospheric pressure is applied to the high pressure terminal connected to the detecting hole at the entry portion, which causes a pressure difference between both pressure terminals, and the mechanical switch is set to on. When the tape loop is located below the loop position detecting hole at the bottom part of the column, the atmospheric pressure is applied to both pressure terminals, causing no pressure difference and resetting the mechanical switch to off.

Capacitive Sensor Circuit

This circuit converts the difference in electrostatic capacity between the two capacitive sensors into the DC voltage proportional to the difference. A pair of capacitive sensor receiving circuits (unit F and M) is provided for each reel motor drive circuit. Figure 3-19 shows this circuit. Figure 3-20 shows the relationship in operational wave form between currents and voltages.

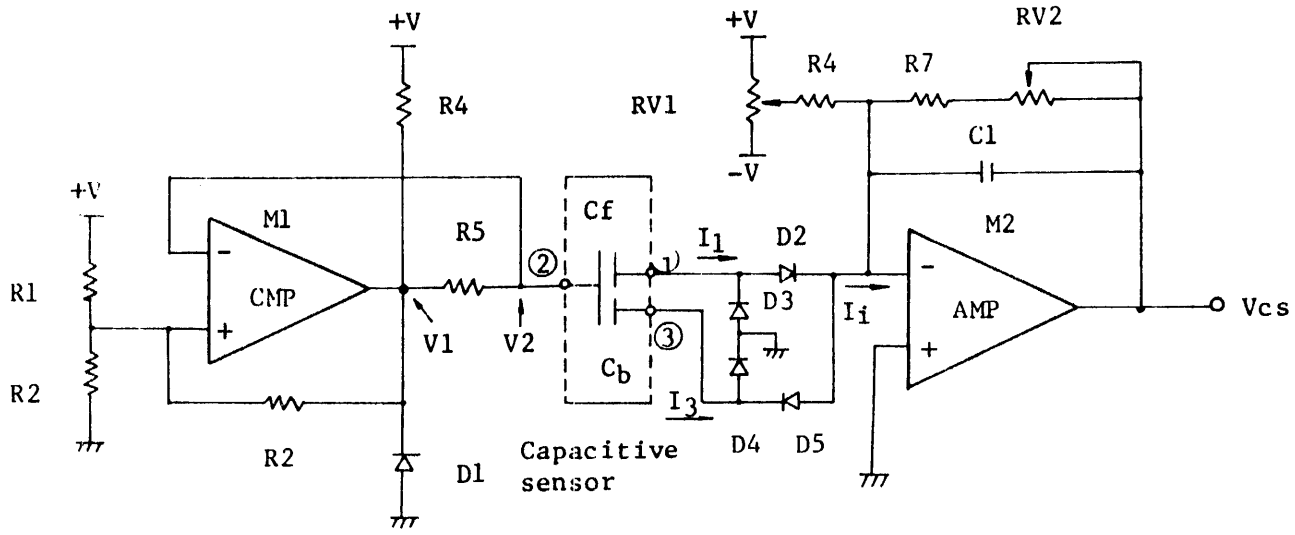


Figure 3-19. Capacitive sensor circuit.

The left part of Figure 3-19 represents a generator for driving the capacitive sensor. This generator is an oscillator (by means of a comparator) having the resistor R5 and the compound electrostatic capacity (C_f + C_b) of the capacitive sensor. D1 is a constant-voltage diode to make the output voltage of comparator M1. The circuit on the right is a current-voltage converting circuit. The output current of the capacitive sensor is rectified by diodes D2 through D5. the positive half cycle of the output current on the sensor C_f side flows into amplifier M2, and the negative half cycle of the output current on the sensor C_b side flows out from amplifier M2. This negative cycle of current that flows out from amplifier M2 is smoothed by capacitor C1, and the DC voltage proportional to the smoothed mean current becomes the output voltage of amplifier M2.

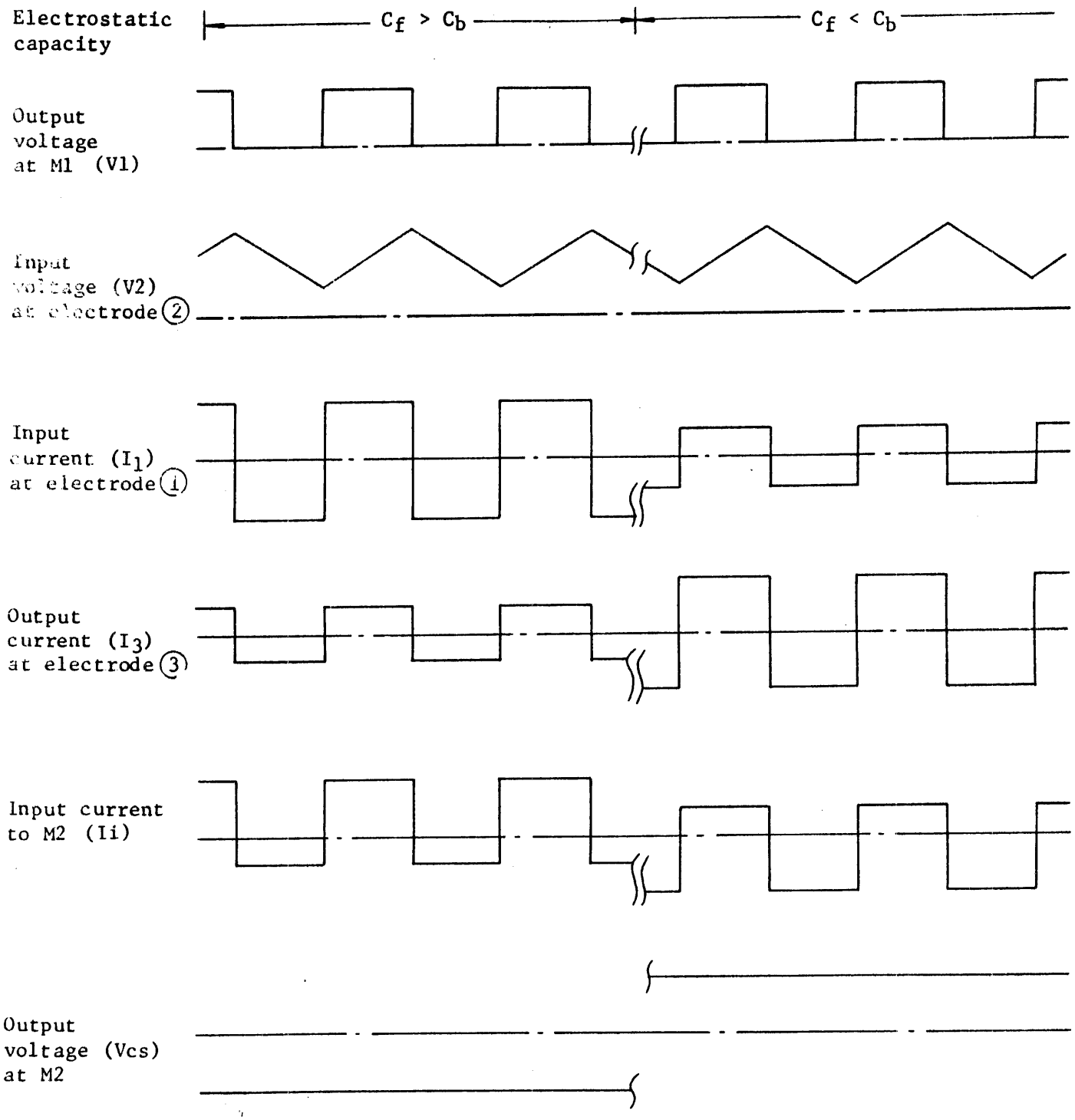


Figure 3-20. Relationship in operational wave form between currents and voltages in the capacitive sensor receiving circuit.

When the tape loop is located in the vacuum column corresponding to the middle position in the operational range of the capacitive sensor and electrostatic capacities, C_f and C_b are equal. The absolute value of the input current to amplifier M2 is equal to that of the output current from M2. Their mean value becomes zero, and the output voltage at M2 becomes zero volts.

When the tape loop moves and electrostatic capacity C_f becomes greater than electrostatic capacity C_b, the current that flows into amplifier M2 increases and the output voltage at M2 becomes negative. When C_f is smaller than C_b the output voltage becomes positive. Thus, a DC voltage is obtained that is proportional to the difference between two electrostatic capacities of the capacitive sensor. Semi-fixed resistor RV2 is used for balance adjustment. When the tape loop is located at the position in column corresponding to the middle position in the operational range of the capacitive sensor, the balance adjustment is carried out so that the output voltage of the capacitive sensor circuit becomes zero volts. In addition, semi-fixed resistor RV1 is used for adjusting the sensitivity of the capacitive sensor.

Reel Motor Drive Signal

The circuit shown in Figure 3-21 generates the reel motor drive signal. It uses the position of tape loop obtained from the capacitive sensor circuit and the tape run signal from the device control circuit.

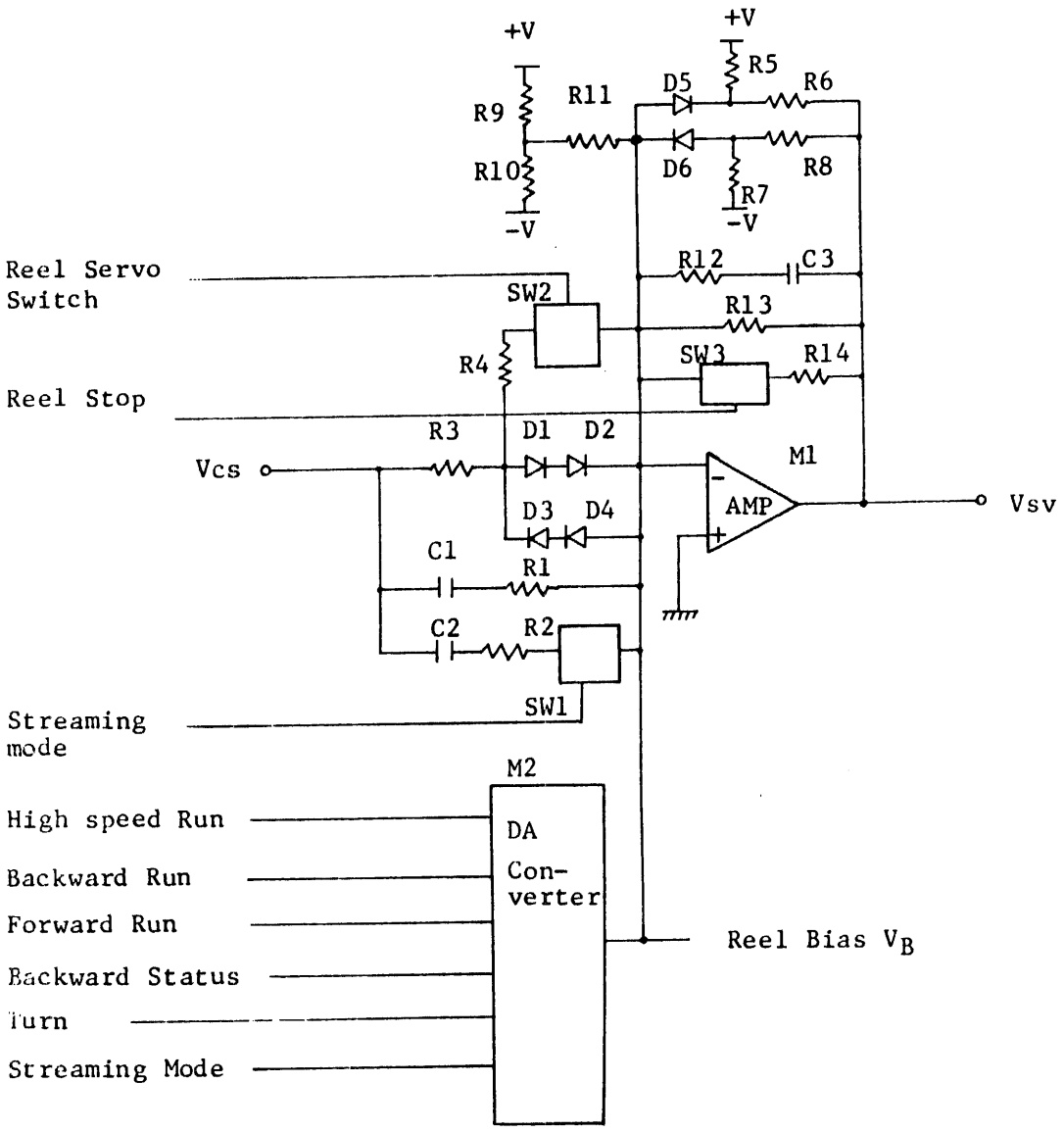


Figure 3-21. Reel control circuit.

M1 represents a summing amplifier used for amplifying output signal Vcs from the capacitive sensor. This amplifier is also used for summing the rate of movement of the tape loop by differentiating tape loop position signal Vcs with the differentiating circuit (C1, R1, C2, R2), thereby upgrading the transient response of the reel motor. Switch SW1 is used to switch the differential gain by the normal/streaming mode, thereby optimizing the transient response of the reel motor.

The balanced position adjustment of tape loop is carried out by apply the bias voltage appropriate to various operations such as FWD/BWD, STREAMING FWD/BWD Status, STREAMING FWDll/BWD RUN, and High Speed BWD. This adjustment uses DA converter M2 in accordance with the running condition of tape.

Diodes D1 through D4 lower the sensitivity of the sensor for the positional component of tape loop by reducing the gain of M1 when the input voltage approaches zero. (This occurs when the tape loop is located at the position in column corresponding to the middle position in the operational range of the capacitive sensor.) The gain of M1 becomes small near zero input voltage while the TURN operation with a short cycle is executed. Switch SW2 suppresses the dead zone of diodes D1 through D4 to protect the position of tape loop from being dislocated greatly from the bias position in the direction opposite to the current direction in which the bias position is used.

Diodes D5 and D6 and resistors R5 through R8 keep the output voltage of the motor drive circuit below a predetermined value. Thus, they prevent overcurrent from flowing into this circuit.

Resistors R9 through R11 apply a constant voltage to the amplification circuit. These resistors produce a constant torque in the tape-winding direction. This torque is required due to the prepressure inside the vacuum column, which attracts the tape loop.

While the capstan motor and the tape loop inside the vacuum column are halted, switch SW3 changes the feedback of M1. It also, reduces the sensitivity of the sensor for the dislocation of tape loop position to keep the capstan motor and the tape loop in a stable halt condition.

Reel Motor Drive Circuit

The circuit shown in Figure 3-22, drives the reel motor. It uses the motor drive signal obtained from the reel motor drive signal generating circuit. This circuit supplies a constant current proportional to the drive signal voltage and drives the reel motor at a constant rotational frequency during autoloading or unloading. The power amplifier is associated with tape drive B PCA.

The remainder is associated PCA 1A04. (See the PCA location charts in the Maintenance Manual for nomenclature and location of all printed circuit assemblies.)

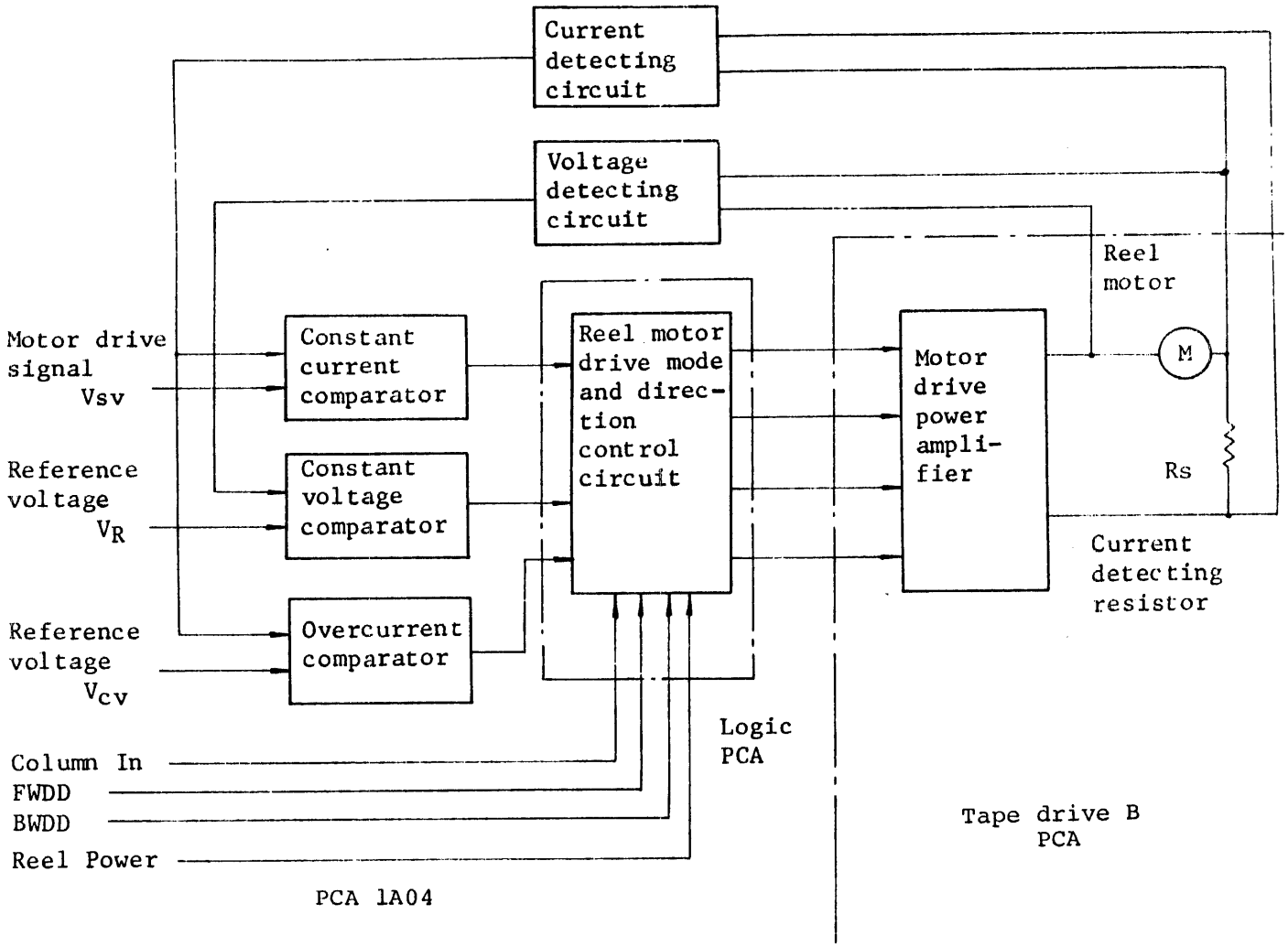


Figure 3-22. Reel motor drive circuit.

The components of the reel motor drive circuit are as follows:

(1) Current Detecting Circuit

This circuit converts the current flowing through the armature of the reel motor into the voltage proportional to the current by the amplifying the voltage generated between both ends of resistor Rs. This resistor is connected in series with the reel motor circuit.

(2) Voltage Detecting Circuit

This circuit integrates and amplifies the inductive voltage generated between the terminals of the reel motor when it is rotated. It converts the rotating speed of the reel motor into the voltage proportional to its rotating speed. The gain of this circuit is changed during auto threading, column out, or when detecting that tape has been removed from the vacuum column and rewound.

(3) Constant Current Comparator

This circuit compares the reel motor drive signal Vsv obtained from the reel motor drive signal generating circuit and the reel motor current signal obtained from the current detecting circuit with respect to magnitude and polarity. If the reel motor drive signal and the reel motor current signal are the same in polarity and the former is greater in absolute value than the latter, the power amplifier is driven. Otherwise, the power amplifier drive is halted. If those signals are opposite in polarity, the power amplifier is driven to have the same polarity.

(4) Constant Voltage Comparator

This circuit compares the magnitude of the reel motor voltage signal with the reference voltage corresponding to a pre-determined rotational frequency of the reel motor. The circuit drives the power amplifier if the reel motor voltage is smaller than the reference voltage. It halts the power amplifier if the reel motor voltage is greater than the reference voltage.

Thus, the reel motor can be regulated to rotate at a predetermined constant frequency. In addition, because the frequency of the reel motor varies at the file reel, machine reel, and during clockwise counterclockwise rotation, the reference voltage of the constant voltage comparator is supplied individually for each situation.

(5) Overcurrent Comparator

This circuit compares the amount of reel motor current signal with the reference voltage determined to correspond to a predetermined current value. If the reel motor current signal is smaller than the reference voltage, the current drive status of the power amplifier is maintained. Otherwise, the power amplifier is shut off so as not to increase the reel motor current to a value greater than the current amount. Thus, the maximum reel motor current is suppressed and does not exceed the rated current of the transistors in the power amplifier during motor driving or braking, thereby preventing the transistors of the power amplifier from being destroyed.

(6) Reel Motor Drive Mode and Direction Control Circuit

This circuit is loaded in the logic PCA. When the tape loop is placed inside the vacuum column (Column In), this circuit selects the input signal from the constant current comparator and carries out the constant current drive control. When the tape loop is not inside the column, this circuit carries out the constant voltage (constant rotation) drive control using logical signal (FWDD and SWDD) from the device control circuit and the input a signal from the constant voltage comparator. At the same time, this circuit determines the driving direction of the power amplifier and controls the rotational direction of the reel motor. When the driving direction of the power amplifier suddenly changes, the power amplifier is suppressed for a prescribed time to prevent the power amplifier's transistors from being destroyed by the large spike-shaped current. This control circuit is made effective by the logical signal (Reel Power) and ineffective when the overcurrent signal is input from the overcurrent comparator.

(7) Reel Motor Drive Power Amplifier

Figure 3-23 is a schematic of the power amplifier assembly. A drive signal form the reel motor drive mode and direction control circuit is applied to the power amplifier inputs CWD/*CWD or CCWD/*CCWD. When inputs CWD/*CWD are effective, Q1 and Q4 are set to on and the reel motor rotates clockwise. When inputs CCWD/*CCWD are effective, Q3 and Q2 are set on and the reel motor rotates counterclockwise.

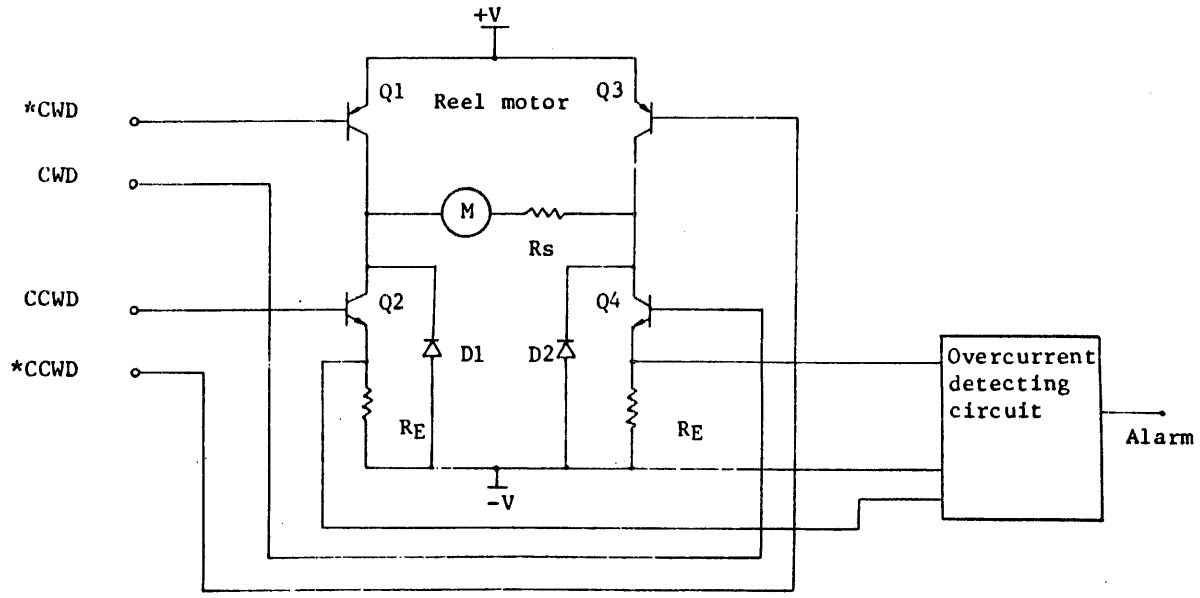


Figure 3-23. Schematic of the power amplifier.

During normal operation, short-circuit protection is obtained because Q1 and Q2 versus Q3 and Q4 are not set to on at the same time. If a short-circuit current flows into the power amplifier due to faulty operation of the control circuit or destruction of the power amplifier transistors, the current detecting resistor RE detects the faulty current. An alarm signal is output from the overcurrent detecting circuit to the logic circuit, and this alarm signal shuts off the current to the power amplifier.

Diodes D1 and D2 perform the switching operation. These diodes protect the system from applying voltage to Q2 and Q4 in opposite directions when either Q1 or Q3 is reset.

3.7.2 Operation of the Reel Motor Drive Circuit

Reel Motor Drive Method

This method detects the position and speed of the tape loop inside the vacuum column. The motor torque correspond to the difference in position and speed between the actual current position and speed of the tape loop, and the predetermined loop's balanced position and reel speed. Thus, the position of tape loop falls within a predetermined range. To control the motor torque, the reel motor drive circuit performs the switching operation to flow the constant current specified by the input signal into the reel motor. Figure 3-24 shows the signals, used in the power amplifier during constant current operation.

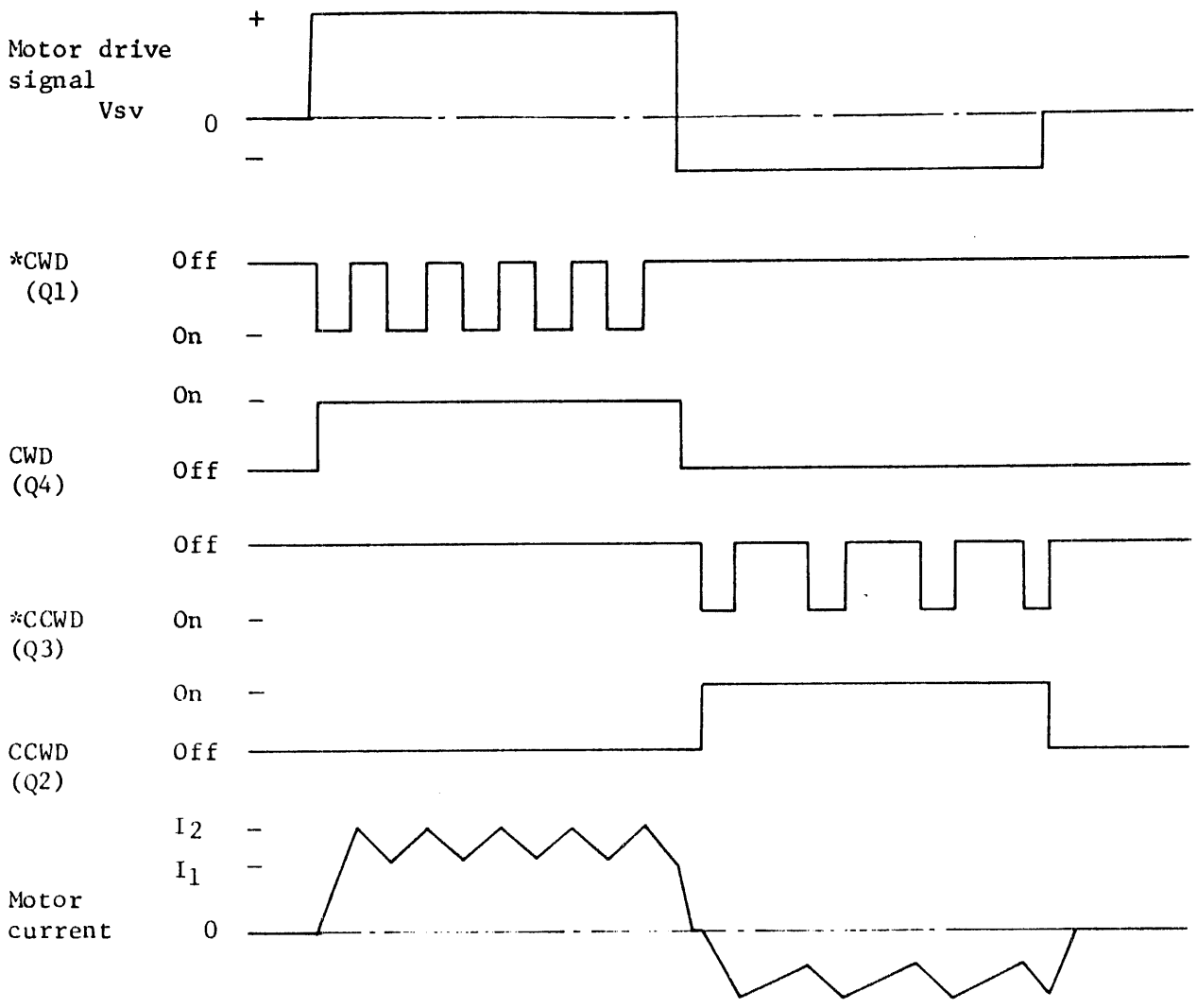


Figure 3-24. Time diagram of correlated signals during constant current.

When motor drive signal Vsv is positive, the constant current comparator and the drive mode and direction control circuit set the power amplifier transistors Q1 and Q4 to on. The power supply voltage is applied to the reel motor, and current flows from power supply terminal +V —> transistor Q1 —> reel motor --> transistor Q4 --> power supply terminal -V. Since the armature of the reel motor has considerable inductance, the reel motor current does not reach the saturation value determined by the amount of DC resistance in the circuit, but rather, increases gradually.

When the reel motor current reaches I_2, the output of the constant current comparator resets transistor Q1. Although no power supply voltage is applied to the reel motor, the current does not instantaneously become zero. Due to the large inductance of the armature, the current decreases gradually from reel motor —> transistor Q4 —> diode D1 —> reel motor. When the reel motor current decreases to I_1, the constant current comparator turns again. the power supply voltage is applied to the reel motor, and the reel motor current increases once again. Thus, when the on/off operation of the power amplifier transistors is repeated, the reel motor current varies between two current values, I_1 and I_2, determined by the motor drive signal. The mean current value becomes constant.

When the reel motor drive signal Vsv is negative, power amplifier transistors Q3 and Q2 performs the same operation as when signal Vsv is positive. The reel motor current flows into the motor in the direction opposite that when the signal Vsv is positive.

To allow the reel motor to perform low-speed rotation for autoloading or unloading, constant voltage is applied between both terminals of the reel motor. A predetermined rotation frequency is ten obtained. In this case, the power amplifier transistors are turned on and off. Similar to the case of constant current operation, the mean voltage applied to the motor is constant and the reel motor performs a low, constant-speed rotation.

High-Speed Rewind Operation

The operation of the capstan drive system during high-speed rewinding is described in Section 3.6. However, high-speed rewinding is not handled independently by the capstan drive system. Rather, it is restricted by the response from the reel motor. Figure 3-25 shows the timing during high-speed rewinding.

If the reel speed cannot reach the capstan speed while the capstan is accelerating or in high-speed, the tape loop inside the both columns moves downward. The rewind speed control circuit detects the mismatch between reel speed and capstan speed. The reel motor reaches full drive status and issues the high-speed control signal to forcibly reduce the capstan speed.

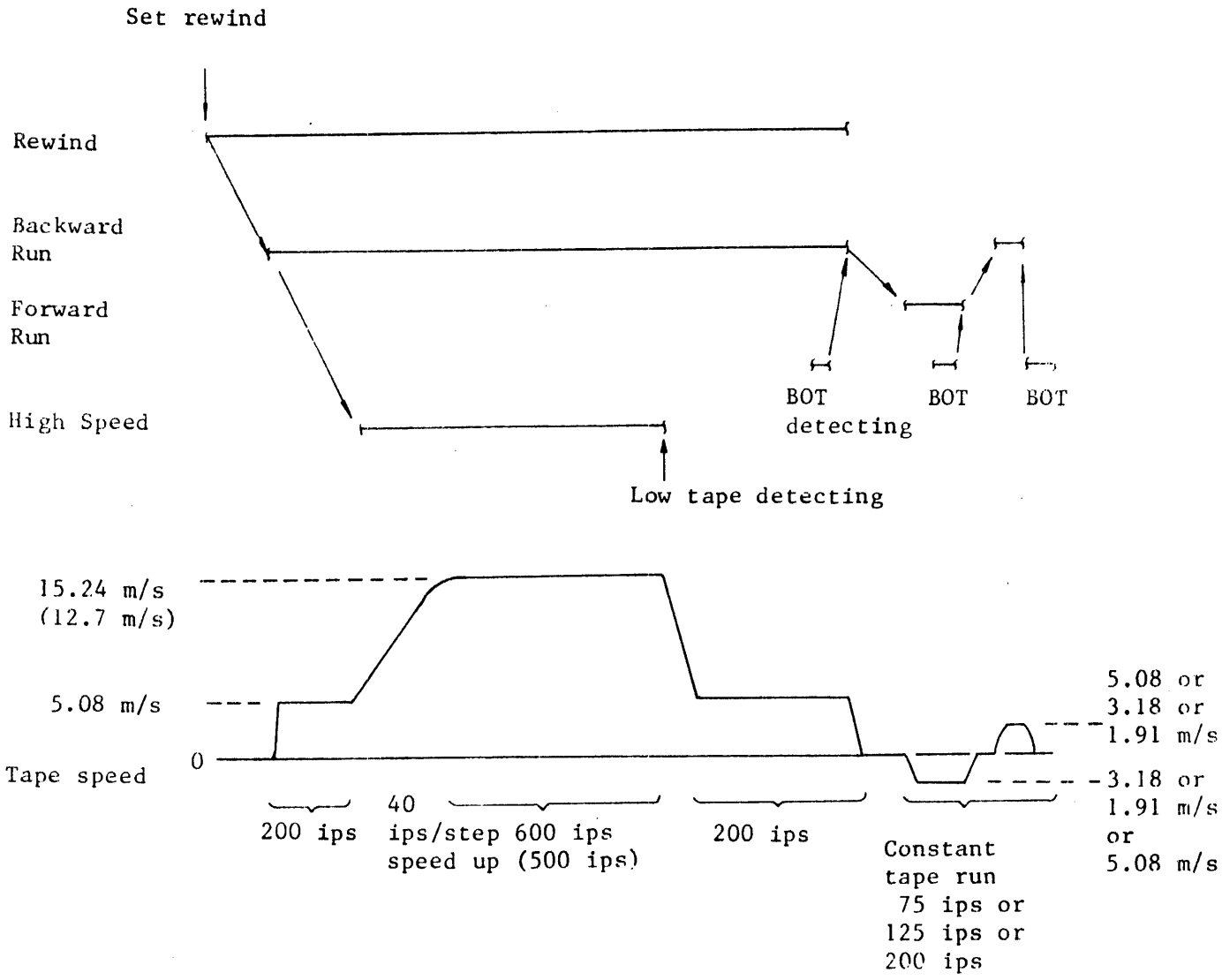


Figure 3-25. Time diagram during high-speed rewinding.

3.8 Write/Read Circuit

3.8.1 Write/Read Operation

Figure 3-26 is a schematic representation of the write/read circuit. This circuit is divided into three main sections: the interface circuit, the write circuit, and the read circuit. The interface circuit sends and receives information necessary for the write/read operation to and from the formatter (FMT) through the interface control section installed in the MTU. The write circuit records write information on the loaded magnetic tape through the magnetic head. The read circuit reads the information recorded on magnetic tape.

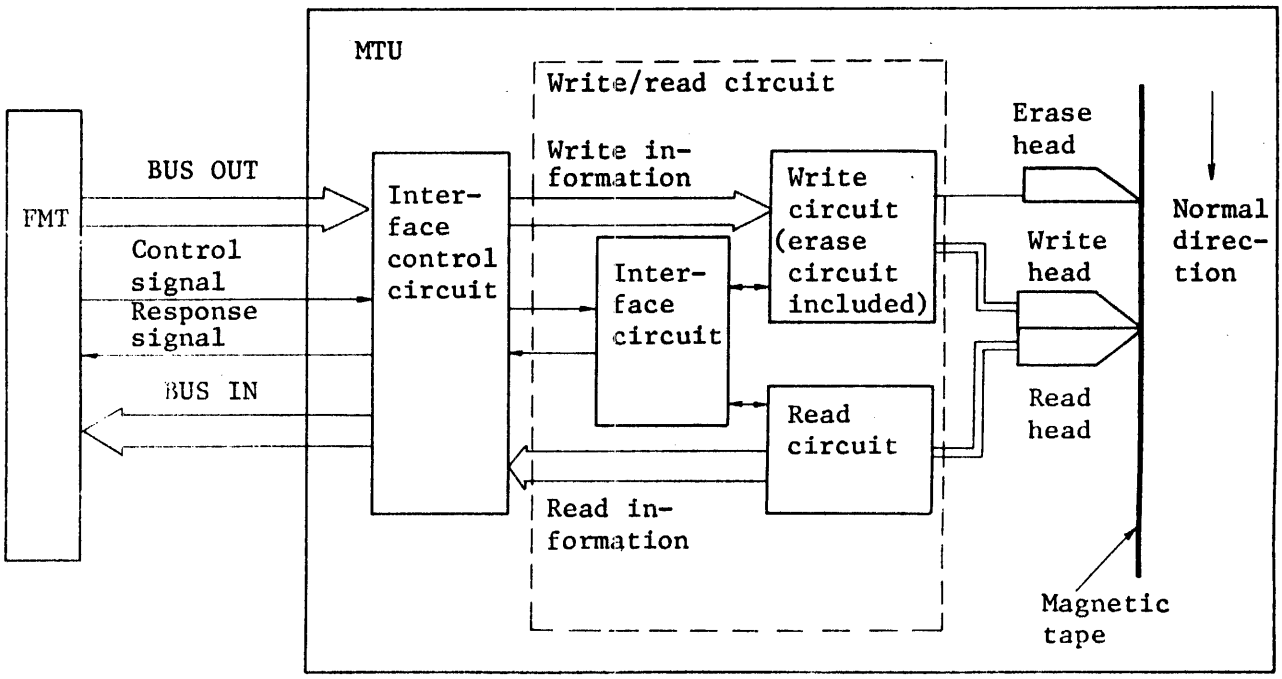


Figure 3-26. Write/Read circuit.

When the MTU is in the write status, the Bus Out information (write data) is sent to the write circuit through the interface control circuit. The write circuit records data on tape by magnetizing inversion of the write head. The erase head generates a strong DC magnetic field to erase old data recorded on the magnetic tape when the MTU is in the write and erase status. The magnetized inversion recorded on the tape generates a signal in the read head when the tape passes through the read head. The read signal voltage is converted by the read circuit into the pulse signal that can be demodulated and sent to FMT through the interface control circuit and Bus In.

Figure 3-27 shows the pulse forming process for a read signal in the (PE) Phase Encoded/(GCR) Group Coded Recording read circuit. (Figure 3-28 shows the process in the NRZI mode.

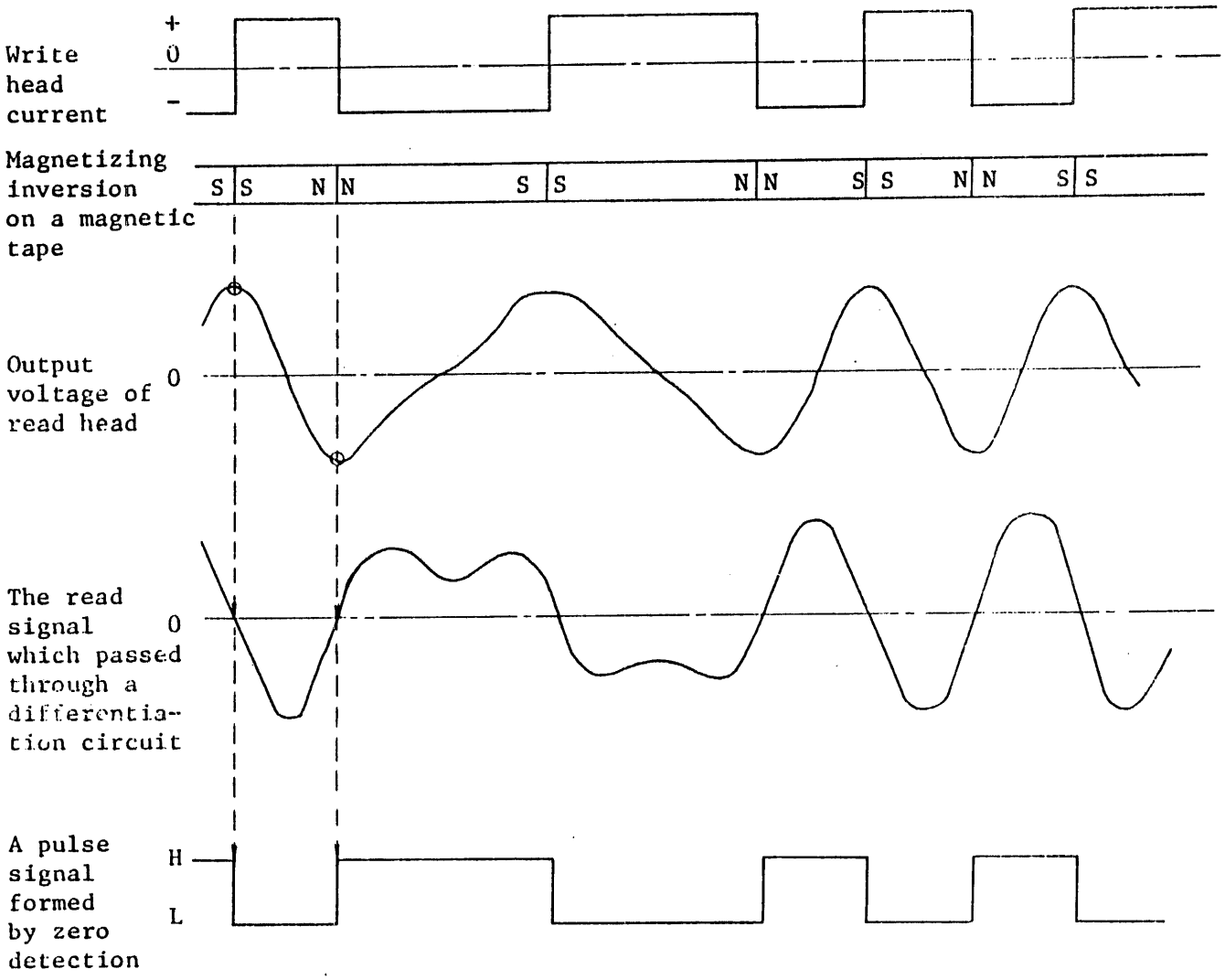


Figure 3-27. Pulse Regeneration in PE/GCR.

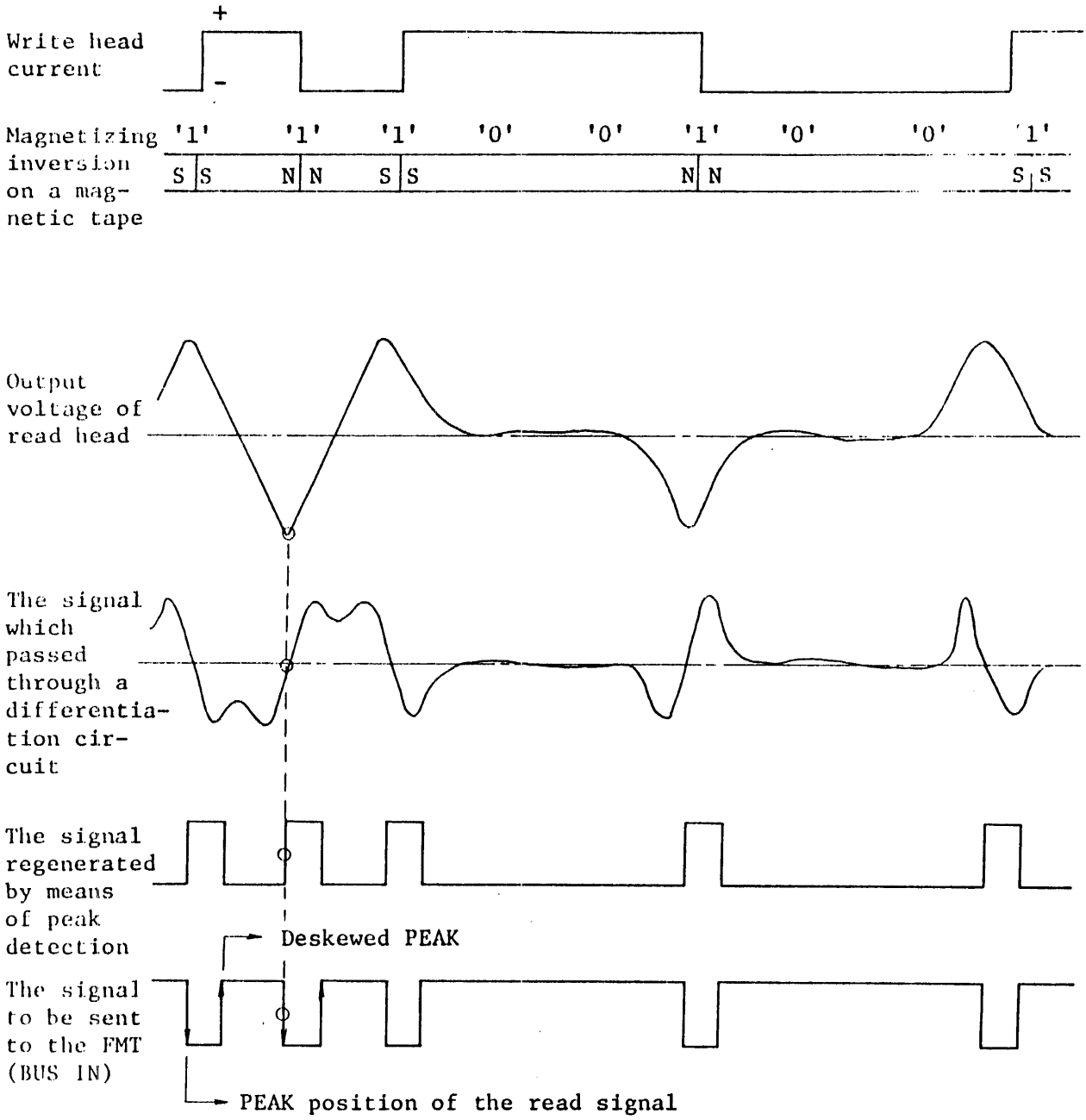


Figure 3-28. Pulse regeneration in NRZI mode.

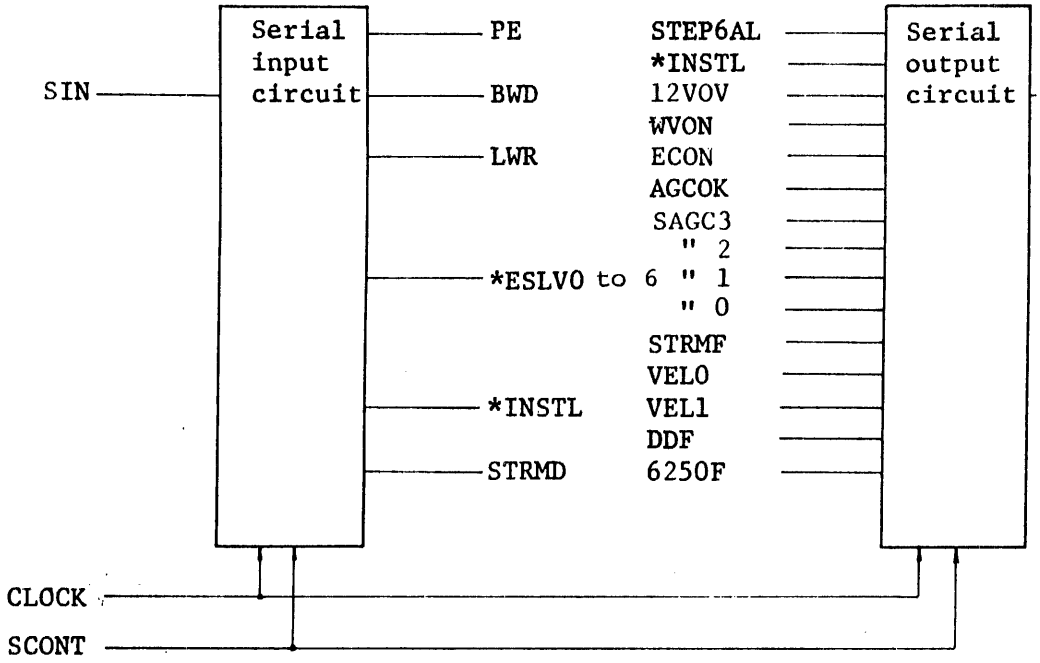
The write/read circuit shown in Figure 3-26 is implemented on one PCA. Table 3-6 lists model, function, and the PCA.

Table 3-6. Write/read circuit of each model

Unit name	Function		Write/read PCA Part Number
	SPEED (ips)	DENSITY (rpi)	
M2432L M2435L1/L2 M2436L1/L2/L8	125/200	6250/1600	B16B-7230-0030A#U
M2433L	"	1600/800	B16B-7250-0020A#U
M2430L M2434L1/L2	75/1600	6250/1600	B16B-7240-0030A#U
M2431L	"	1600/800	B16B-7260-0020A#U

3.8.2 Interface Circuit

The interface circuit sends and receives the information required by the write/read circuit to and from the FMT with the aid of the interface control circuit installed in the MTU. Figure 3-29 shows the structure of the interface circuit.



Note: Inputs STEP6AL, AGCOK, and SAGC0 through 3 are ineffective when the 1600/800 rpi modes are used (clamped to zero volts).

Figure 3-29. Interface circuit.

The serial input circuit converts 12 serial signals sent by the SIN signal into parallel signals. This circuit uses the CLOCK and SCONT signals and loads the converted signals into the register.

The parallel output circuit converts 15 input signals into serial signal SOUT with the aid of the CLOCK and SCONT signals.

Input/Output Signal Lines of the Interface Circuit

a. SIN

The SIN signal can serially receive up to 15 signals in synchrony with the CLOCK and SCONT signals. The present MTUs of these use 12 signals.

b. Output signals by the SIN signal

The signals obtained from the SIN signal are as follows:

- o PE — Indicates that the MTU in use operates in the PE (1600 rpi) mode.
- o BWD — Indicates that the MTU in use operates in the BWD (BACKWARD) mode.
- o ESLV0 through 6 — Controls the slice level in the read circuit.
- o INSTL — (Install signal) becomes the INSTL signal of the SOUT input signal to check the connection of the interface cable.
- o STRMD — Indicates that the MTU in use operates in the streaming mode.

c. CLOCK and SCONT signals

These two signals execute the serial to parallel conversion between interfaces. Operation of these is shown in Figure 3-30.

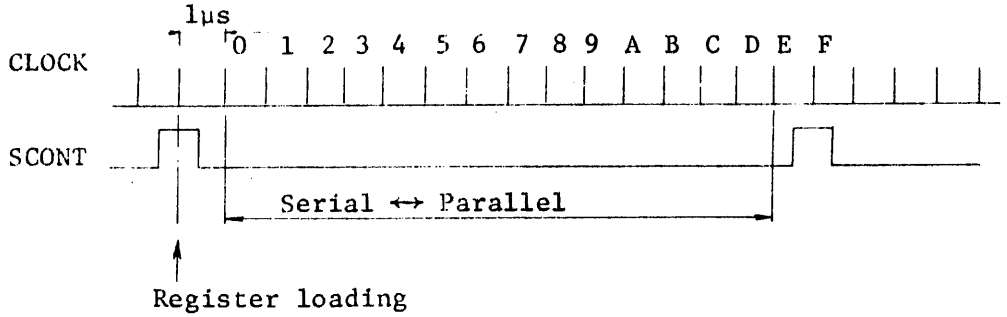


Figure 3-30. Operation of the CLOCK and SCONT signals.

d. SOUT signal

This signal can send up to 15 signals in synchrony with the CLOCK and SCONT signals.

e. Input signals to the SOUT signal

Input signals that the SOUT signal can send are listed below.

- o STEP6AL Is effective only when the MTU operates in the 6250/1600 rpi mode. This signal indicates that SAGC count of all tracks has 6 or 7 steps.

- o INSTL Is the signal received from the signal INSTL output from the SIN signal. It is used to check an interface cable.

- o 12VOV Is set to "1" when the voltage of the 12V power supply used in the write circuit rises higher than the required value. The detecting voltage is set up at about 16 volts.

- o WVON Is set to "1" when the write voltage is supplied to the write head.

- o AGCOK Is effective for the 6250/1600 rpi modes. This signal is set to "1" when the read circuit completes level setting to all the tracks during the (SAGC) Self-Adjust Gain Control operation.

- o SAGC0 through 5 Are effective only for the 6250/1600 rpi modes. These signals specify the setting level in the read circuit.

- o STRMF Is "1" when the MTU in use can be operated in the streaming mode.

- o VEL0, 1 Represent the operating speed of the MTU. The correspondence between these signals and operating speed of the MTU is shown in table below, where the operating speed means the normal speeds.

Speed	VEL signal	
	0	1
75 ips	1	1
125 ips	0	0
200 ips	1	0

- o DDF is "1" when the write/read circuit can operate in the 2-density mode (6250/1600 rpi or 1600/800 rpi)

o 6250F is "1" when the write/read circuit is ready to operate in the 6250 rpi mode.

3.8.3 Write Circuit for the 6250/1600 rpi MTU

The write circuit shown in Figure 3-31 consists primarily of the write current control circuit, the write voltage generating circuit, the erase circuit, the write control circuit, and the file protect circuit. The write current control circuit is provided individually for each track; other circuits are used in common.

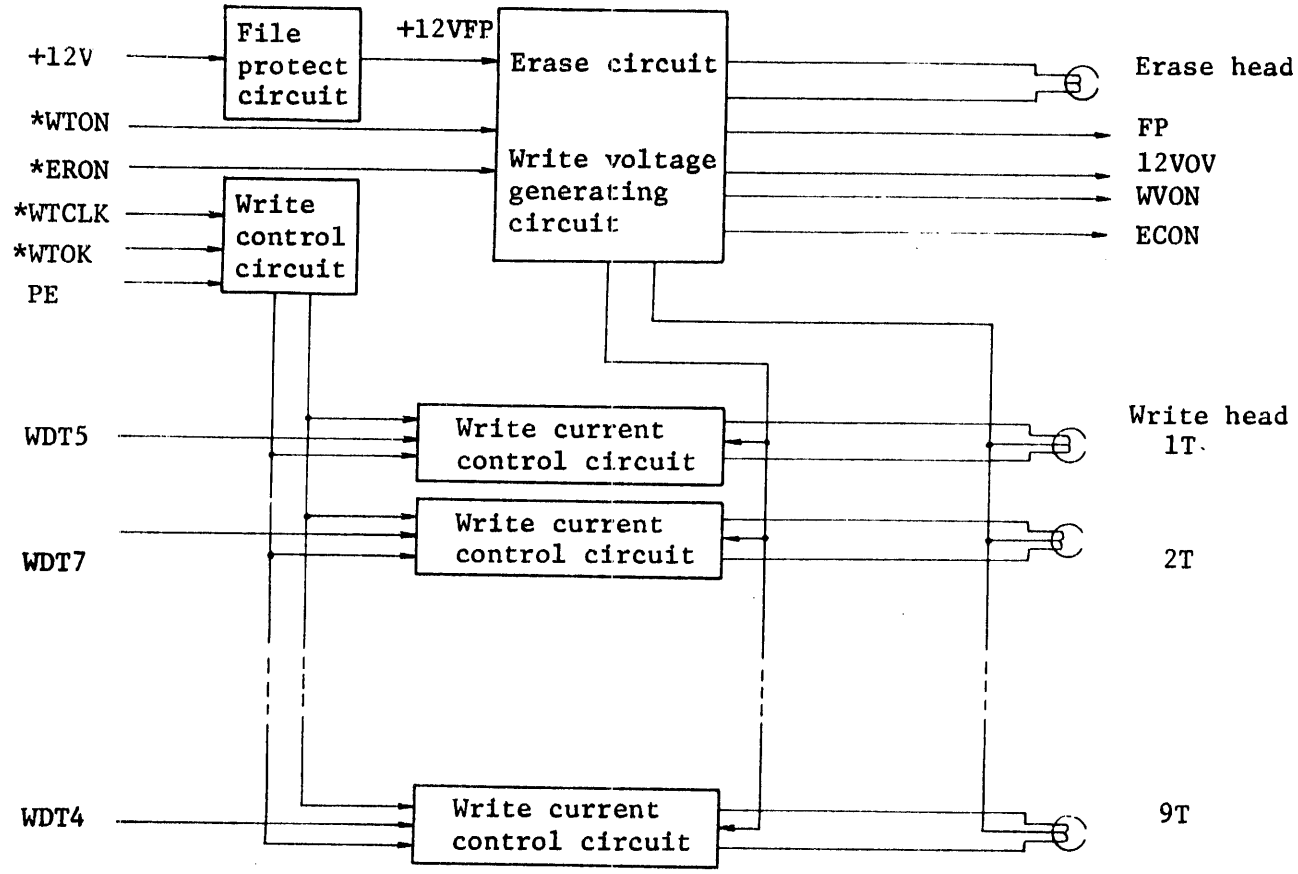
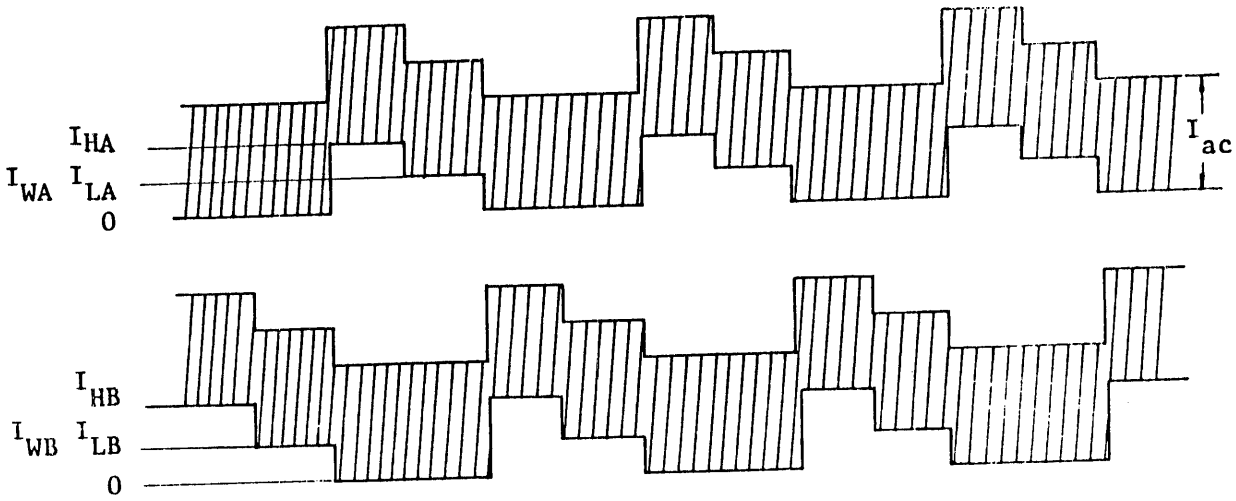


Figure 3-31. Write circuit.

a. Write current control circuit

This circuit controls the current flowing in the write head. The write current has a rectangular wave form for the PE mode. The compound waveform (AC bias is overlapped to a stepped wave for the GCR mode) is shown in Figure 3-32. The current used for PE is higher than that of GCR. The current supply is based on the constant current system. Current is supplied by the voltage from the voltage generating circuit.



I_{WA} and I_{WB} are the currents which flow to one side of the write head.

Figure 3-32. Write current wave shapes.

b. Write control circuit

This circuit carries out the write current control circuit (such as selecting the PE or GCR mode) upon receiving the status signal in the interface circuit. This circuit consists of a generating circuit for AC bias, the write clock setting circuit to carry out pulse-width conversion on the write clock signal (WTCLK) sent from the FMT for stepped wave-form control, and the current control circuit for GCR/PE degauss operation.

c. Write voltage generating circuit and erase circuit. These circuits generate the write voltage and initiates the erase circuit upon receiving two signals WTON and ERON from the interface control circuit. These circuits send four signals FP, 12V0V, WVON, and ECON as response signals to the instructions from the FMT.

d. File protect circuit.

The file protect circuit protects information on the tape from being erroneously erased or rewritten. Figure 3-33 shows the schematic diagram of the file protect circuit.

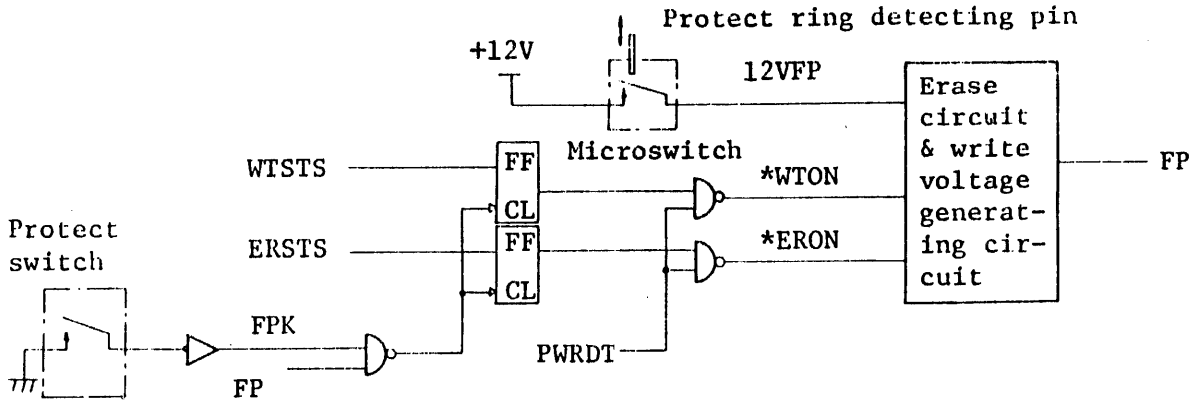


Figure 3-33. File protect circuit.

This circuit is applied by file protection when one of the following conditions occurs:

- When no write enable ring is mounted to the file reel.
- When the PROTECT switch on the operating board is depressed again, the MTU is set in the write enable status.

When the MTU is set in the file protect status by either one of the above actions, the PROTECT lamp on the operating board lights.

Input and Output Signals of the Write Circuit

Input and output signals shown in Figure 3-29 are as follows:

Input signals

WTON turns on the write voltage

ERON turns on the erase circuit

WTCLK is the clock signal to synchronize with write data

WTOK indicates that the write operation is ready

PE indicates the PE mode.

WDT0 through 8 — the write data 0 through 8

Output signals

FP indicates the presence or absence of the 12VFP voltage when the 12VFP voltage is absent, this signal is "1".

12VOV informs of an abnormal rise of 12VFP

WVON indicates that the write voltage has been supplied to the write head.

ERON indicates that current flows in the erase head.

Write Data Cycle

Figure 3-34 shows the write data cycle. The erase status (ERSTS) instruction from the FMT is issued prior to or during the write status (WTSTS) instruction. The ERSTS instruction is converted into the ERON signal, which activates the erase circuit to apply current to the erase head. When the rise of current is sufficient the ECON signal is set on.

When the WTST instruction is issued, it is converted into the WTON signal, which activates the write voltage generating circuit to supply write voltage to the write head. When voltage has sufficiently risen, the WVON signal is set on. When the WVON signal is set on, the WTOK signal is issued, and the write circuit is ready to operate. 9-bit write data WDT0 through 8 is written on the tape in synchrony with the write clock (WTCLK) sent from the FMT.

The write head current wave-form for writing data is rectangular in the PE mode. In the GCR mode, the write head current has a stepped wave compounded by AC bias. When WTST instruction is released, the write circuit enters the degauss operation. The write voltage then decreases gradually, and the write current control circuit uses the pulse for the degauss operation to change the direction of the write head current at a certain cycle. Upon completion of degaussing, the write voltage is lowered, the WVON signal is reset, and the write data cycle terminates.

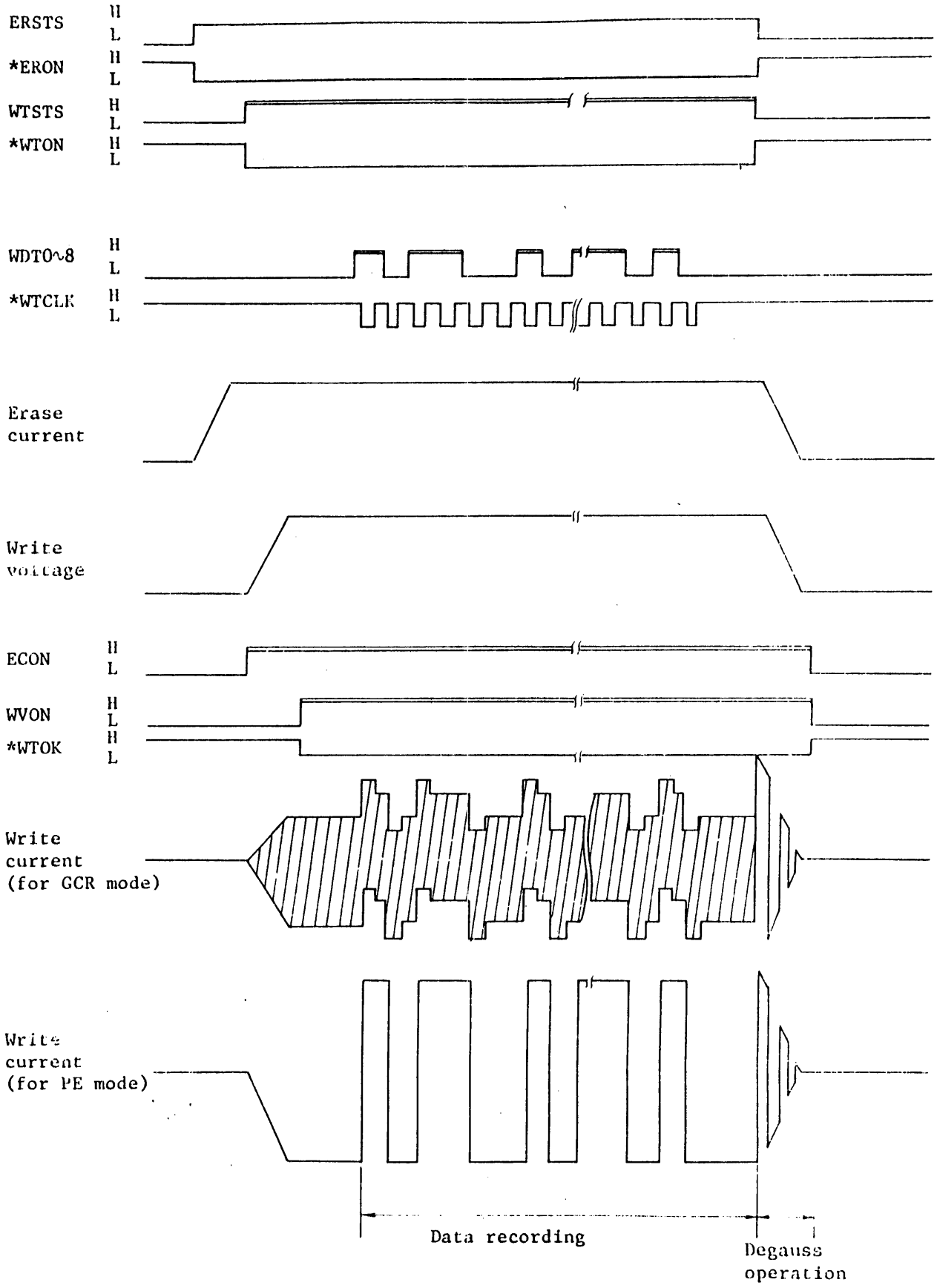


Figure 3-34. Write data cycle.

3.8.4 Write Circuit for the 1600/800 rpi MTU

The write circuit network consists of the write amplification circuit, the write deskew circuit, the write voltage generating circuit, the erase circuit, the write control circuit, and the file protect circuit. Figure 3-35 shows the write circuit. Write amplification and deskew are provided individually for each track; others are provided in common.

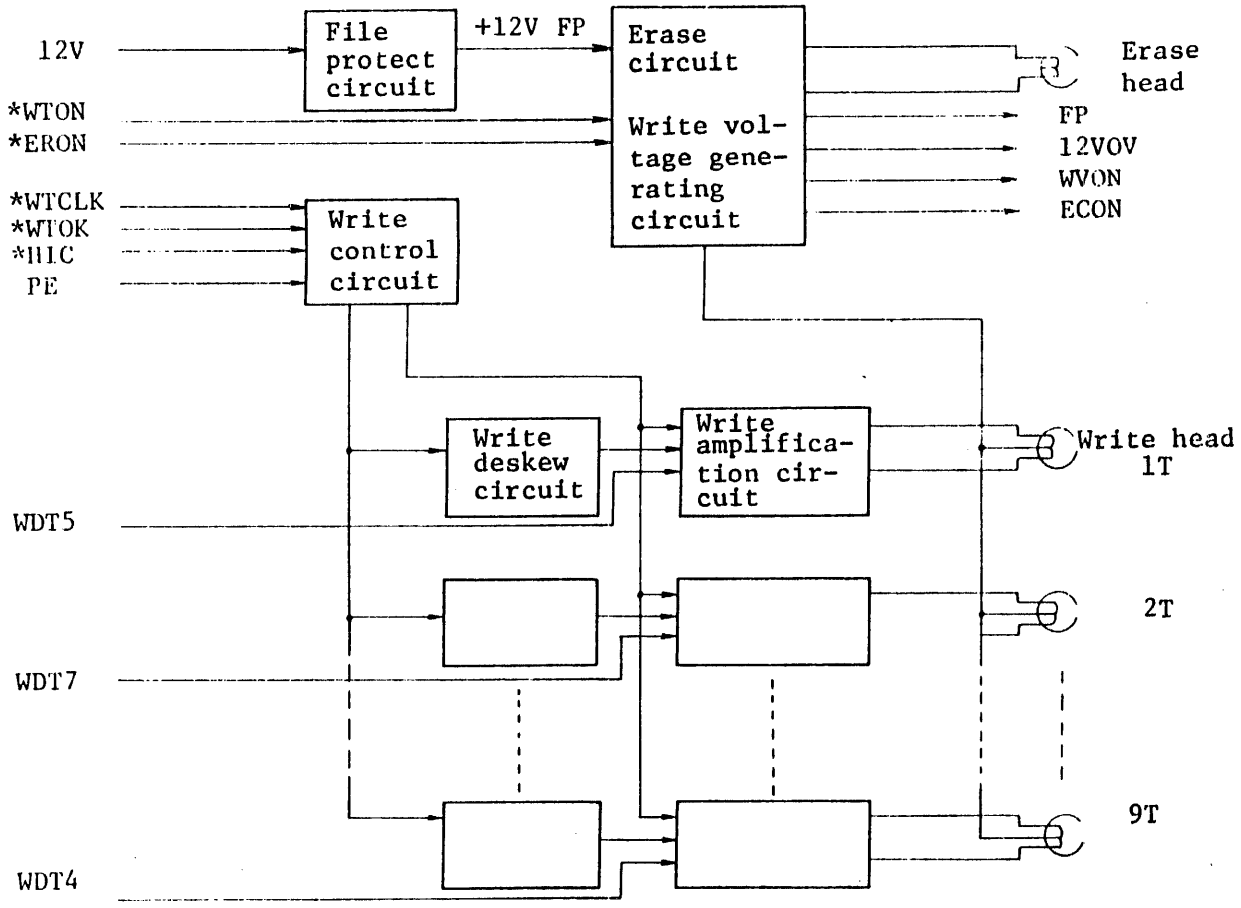


Figure 3-35. Write circuit.

The elements of the write circuit are as follows:

a. Write amplification circuit

This circuit converts write data (WDT) sent from the FMT into the write head current.

b. Write deskew circuit

This circuit corrects static skew of the write head. Write data is synchronized with the write clock (WTCLK) sent from the FMT. This deskew is carried out by independently providing the write clock to each track with delay time.

c. Write control circuit

This circuit controls the write amplification circuit and the write deskew circuit such as selection of PE and NRZI modes) upon receiving the status signal.

d. Write voltage generating circuit

Same as the write voltage generating circuit, explained in Section 3.8.3.

e. File protect circuit

Same as the file protect circuit explained in Section 3.8.3.

Input and Output Signals of the write circuit

Most of the input and output signal lines shown Figure 3-35 are the same as those explained in Section 3.8.3. Only the input signal *HIC differs. This signal indicates write head current in the NRZI mode. This signal is effective when the write mode is NRZI or the high current erase operation is carried out in the PE mode.

Write data cycle

Figure 3-36 shows the write data cycle. The erase status (ERSTS) instruction is issued from the FMT prior to or during the write status (WTSTS) instruction. The ERSTS instruction is converted into the *ERON signal, which activates the erase circuit current. When current has risen sufficiently, the ECON signal is turned on.

When the WTSTS instruction is issued, it is converted into the WTON signal, which activates the write voltage generating circuit to supply the write head with write voltage. When the voltage has risen sufficiently, the WVON signal is turned on. When the WVON signal has risen sufficiently, the *WTOK signal is issued and the write circuit is ready to operate. 9-bit write data WDT 0 through 8 signals are synchronized with the write clock (*WTCLK) and written on the tape.

To carry out the deskew operation in the NRZI mode, the write clock *WTCLK for each track from 1 to 9 is provided independently with delay time.

When the WTSTS instruction is released, the write circuit enters the degauss operation. The write voltage gradually decreases, and the write current control circuit uses the pulses for degaussing to change the direction of write head current. Upon completion of degaussing and when the write voltage has sufficiently decreased, the WVON signal is reset, and the write data cycle terminates.

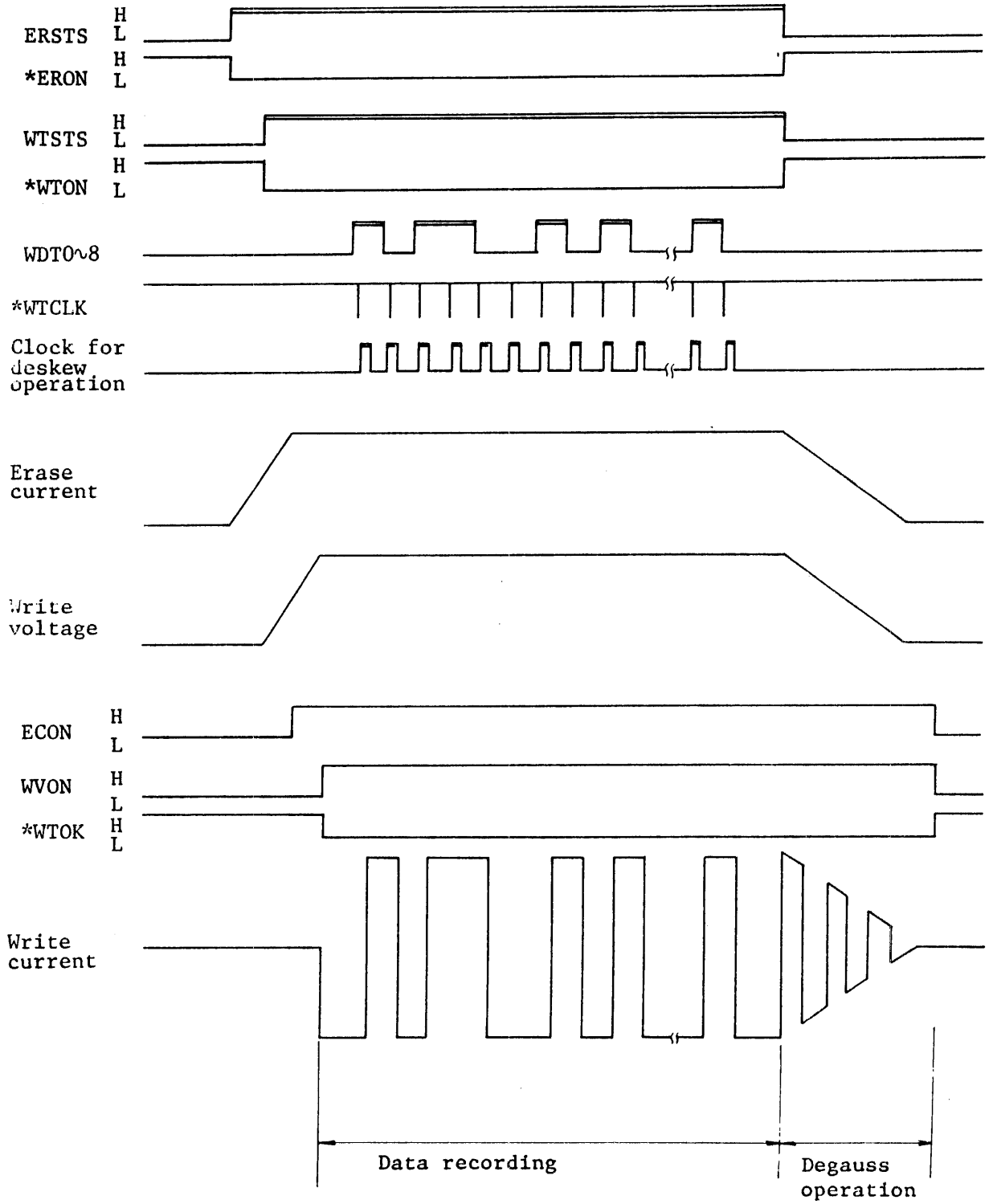


Figure 3-36. Write data cycle.

3.8.5 Read Circuit for the 6250/1600 rpi MTU

The read circuit amplifies the magnetic head output, detects the write data PEAK, converts it into a pulse signal, and sends the converted pulse signal to the FMT.

Figure 3-37 shows the read circuit. This circuit consists of a preamplifier, loop write/read wave generating circuit, gain switching circuit, differentiation amplification circuit, filter amplification circuit, PEAK detecting circuit, amplitude checkup circuit A, demodulation circuit, counter register circuit, amplitude checkup circuit B for automatic gain control, read amplification control circuit, level control voltage generating circuit and reference voltage generating circuit. The read amplification control circuit, level control voltage generating circuit, and reference voltage generating circuit are used in common; others are provided individually for each track.

a. Preamplifier

   This circuit amplifies the output signal from the read head. This preamplifier consists of three differential amplifiers having a gain of 40 and housed in one package.

b. Loop write/read wave generating circuit

   This circuit converts write data (WDT) into the pseudo head wave-form when the MTU operates in the loop write/read (LWR) mode. The converted wave-form is added to the preamplifier output to execute the loop write/read operation.

c. Gain switching circuit and differentiation amplification circuit.

   These two circuits are contained in the same IC. The gain switching circuit switches gain within a range of 4 bits. The gain changes digitally by 4 bits over 16 steps. The ratio between two adjacent steps is always 1.2.

   The differentiation amplification circuit differentiates an amplified signal from the read head for detecting the PEAK position and amplifies the differentiated signal again.

   The control output voltage is 2Vp-p (relative to the ground) for the PE mode and 1.8% 2.2Vp-p (relative tot he ground) for GCR mode after the SAGC operation.

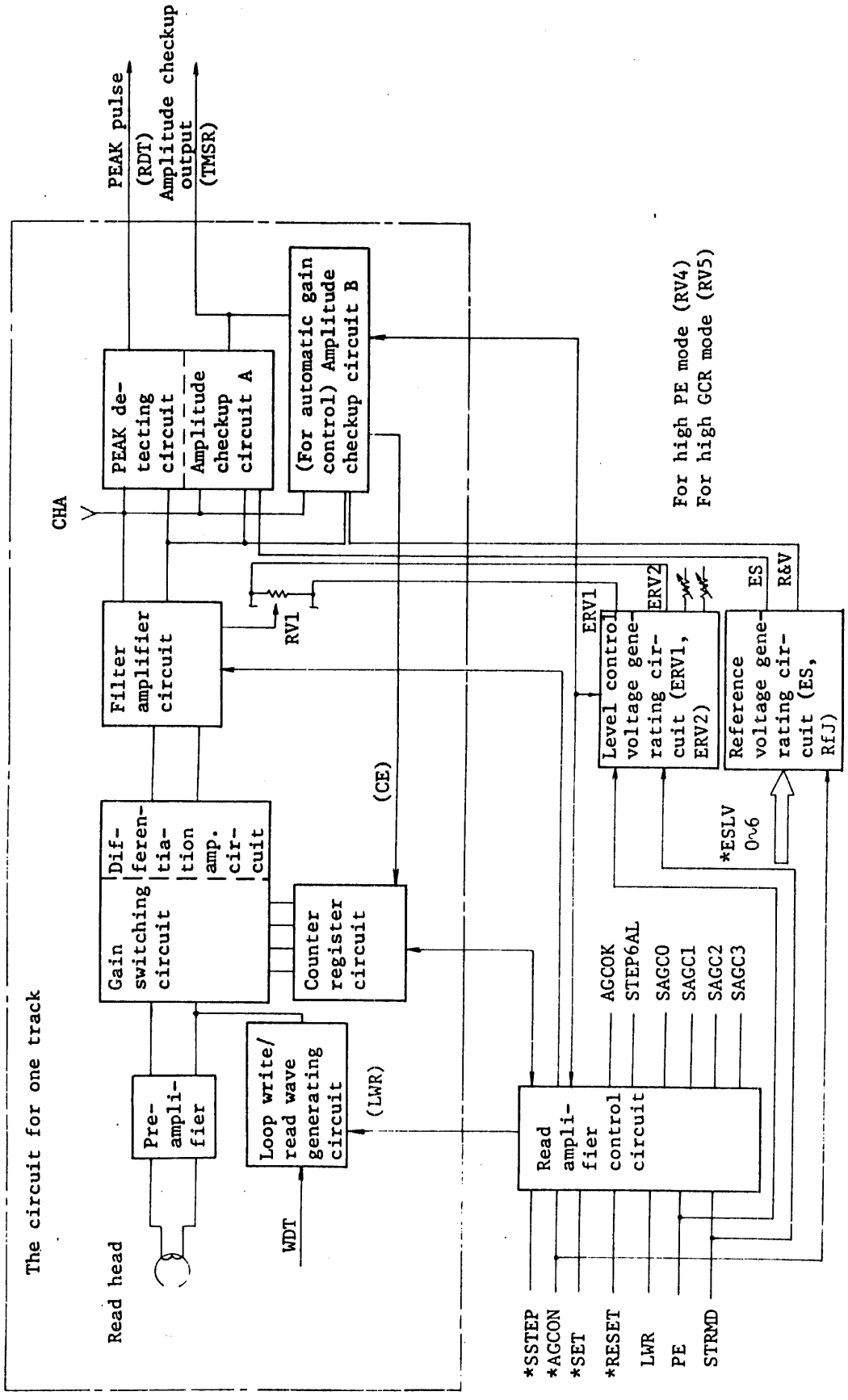


Figure 3-37. Read circuit (6250/1600 rpi)

d. Counter register circuit
This counter register circuit is a 4-bit binary counter and can be used as the register for holding a counted value. This counter register circuit also returns a 4-bit value as 5-bit information of 6.7/8.9/10.11/12.13/14.15 to the read amplifier control circuit.

e. Filter amplification circuit
This circuit is contained in a single IC comprising a low speed active filter, high speed active filter, select circuit, and gain control circuit. It accompanies an external R.C of which the characteristics of the two active filters can further be switched for the PE/GCR modes.

f. PEAK detecting circuit
As differentiated read signals indicate the PEAK positions at zero volts, this circuit carries out zero cross detecting on read signals with opposite phases to produce a PEAK pulse output.

g. Amplitude checkup circuit A
This circuit inspects whether the input signal has a greater than normal amplitude. The inspection is carried out to protect an erroneous operation of the read circuit network caused by signal dropout or noise of the input signal. If the input signal voltage exceeds the reference voltage by a few bits, this circuit generates an output. If the input voltage is lower by a few bits than the reference voltage, this circuit resets the output. Figure 3-38 shows the relationship between input and output signals. The signal is AND-gated with the preceding PEAK pulse in the interface control circuit of the MTU to produce the read pulse.

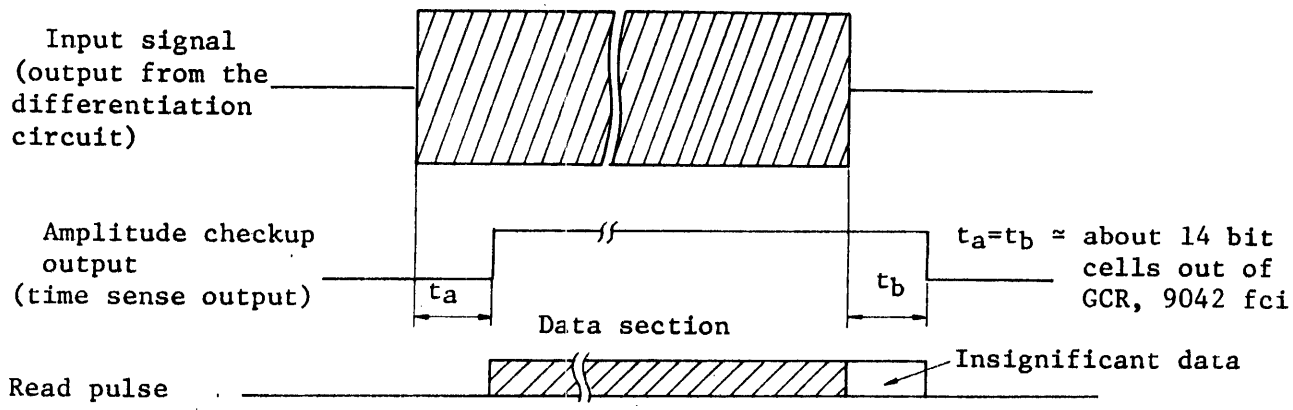


Figure 3-38. Relationship between input and output signals in amplitude checkup circuit A.

h. Amplitude checkup circuit B (for automatic gain control)
This circuit determines whether the output of the filter amplifier exceeds the regular level in the Gain Step Down (GSD) operation.
The reference voltage level (R_{fV}) is different for GSD mode operation.

i. Reference voltage generating circuit
This circuit supplies amplitude checkup circuits A and B with reference voltages E_S and R_{fV}. The supply rate of reference voltage E_S is specified such that bits 0 through 6 of signal *EsLV represent 1, 2, 4, 8, 16, 32, and 64% of voltage level respectively. Bits *EsLV 0 through 6 are assigned by the interface control circuit of the MTU, as shown in Table 3-7. In addition to the above voltage levels, 110% may be specified in the diagnostics mode. The voltage level assigned to reference voltage R_{fV} is about 160% and is 250% for SAGC operation.

Table 3-7. Es level of each mode.

Mode used	Level control (LVC)			Es level			Remarks
				READ		WRITE	
	0	1	2	FWD	BWD		
OLTE	1	1	1	125%			OLTE
	1	1	0	100%			
	1	0	1	80%			
	1	0	0	64%			
	0	1	1	51%			
	0	1	0	41%			
Marginal mode	0	0	1	15%	10%	37%	
Normal mode	0	0	0	10%	7% (10%)	20% (25%)	The value in parentheses is used when the SAGC step is greater than C.
SAGC operation 1				90%			GCR mode only
SAGC operation 2				64%			
Low slice				7% (10%)			The value in parentheses is used when the SAGC step is greater than C.

j. Level control voltage generating circuit
This circuit supplies the gain control section in the filter amplification circuit with voltages ERV1 and ERV2 for voltage level control. The voltage level control for the GCR/PE mode read amplifier is carried out as follows:

(1) By RV1 in the low speed PE mode, and independently for each of the 9 tracks.

(2) By RV4 in the high speed PE mode, for all 9 tracks.

(3) After the SAGC operation is carried out in the low speed GCR mode, the level control is carried out for 9 tracks in the high speed GCR mode by RV5.

(4) The control voltage is always 2Vp-p at terminal CHA.

k. Read amplifier control circuit
This circuit carries out counter-register circuit control, filter switching of the filter amplification circuit, and control for amplitude checkup circuit B. The SAGC and Gain Step Down (GSD) operation in the GCR mode and the control for the counter-register circuit and amplitude checkup circuit B are directed by *SSTEP, *AGCON, *SET, and *RESET signals, respectively. These signals are controlled by the microprogram in the interface control circuit of the MTU. This circuit issues signal AGCOK, STEP6AL and SAGC 0 through 3 to the interface control circuit.

Input and Output Signals of the Read Circuit

Input signals are as follows:

*SSTEP	is the clock signal for the counter-register circuit.
*AGCON	indicates SAGC operation.
*SET	sets the output CE of amplitude checkup circuit B to "1".
LWR	indicates the loop write/read mode.
PE	indicates the PE mode.
STRMD	indicates the streaming mode.
*EsLV 0 through 6	sets up the voltage for the reference voltage generating circuit.
WDT	indicates write data.

Output signals are as follows:

AGCOK — indicates that level setting for all the tracks in the SAGC operation has been completed normally.

STEP6AL — indicates that step values in the counter-register is 6 or 7 for all the tracks. In the PE mode, all the tracks have 6 steps.

SAGC0 — indicates that more than one track has 8 or 9 steps.

SAGC1 — indicates that more than one track has 10 or 11 steps.

SAGC2 — indicates that more than one track has 12 or 13 steps.

SAGC3 — indicates that more than one track has 14 or 15 steps.

RDT — represents a turning point of the information recorded on the magnetic tape. This signal is provided for each of 9 tracks.

TMSR — provides the output of the amplitude checkup circuit A. This signal is provided for each of 9 tracks.

SAGC and GSD operation

Both the Self-Adjust Gain Control (SAGC) and the Gain Step Down (GSD) operation are automatic gain controls. They are performed when the MTU is in the GCR mode.

SAGC operation

Immediately following the BOT mark, after which data is recorded in the GCR mode, the amplitude reference signal Automatic Read Amplification (ARA) is written. The read circuit network carries out gain control using the ARA signal at the beginning of processing.

The SAGC operation, shown in Figure 3-39, is started by the SAGC Start (Set SAGC) instruction from the FMT. When SAGC operation starts, the gain of all tracks is minimized (step 0). After a prescribed time, the read circuit network raises the gain to about 1.2 times the preceding value. When the output (CHA) of the filter amplification circuit reaches 90% of the reference amplitude (2Vp-p), the content of the counter-register circuit is fixed. When the output voltage of all the tracks reaches the reference amplitude, the signal AGCOK is set on. The microprogram ascertains that the signal AGCOK has been set on, resets the SAGCON signal, and terminates the SAGC operation.

The operation described above is called SAGC operation 1. When the amplitude of one track is not settled within the maximum number of steps, the slice level is lowered from 90% to 64%. The microprogram ascertains that the signal AGCOK has been set on.

If the AGCOK signal is on. the microprogram considers that this SAGC operation is completed normally, as for the SAGC operation 1, resets the SAGCON signal, and terminates the SAGC operation. This operation, following SAGC operation 1, is called SAGC operation 2.

If the AGCOK has not been set on in SAGC operation 2, the FMT is informed that the SAGCON signal has not been reset due to failure of the SAGC operation.

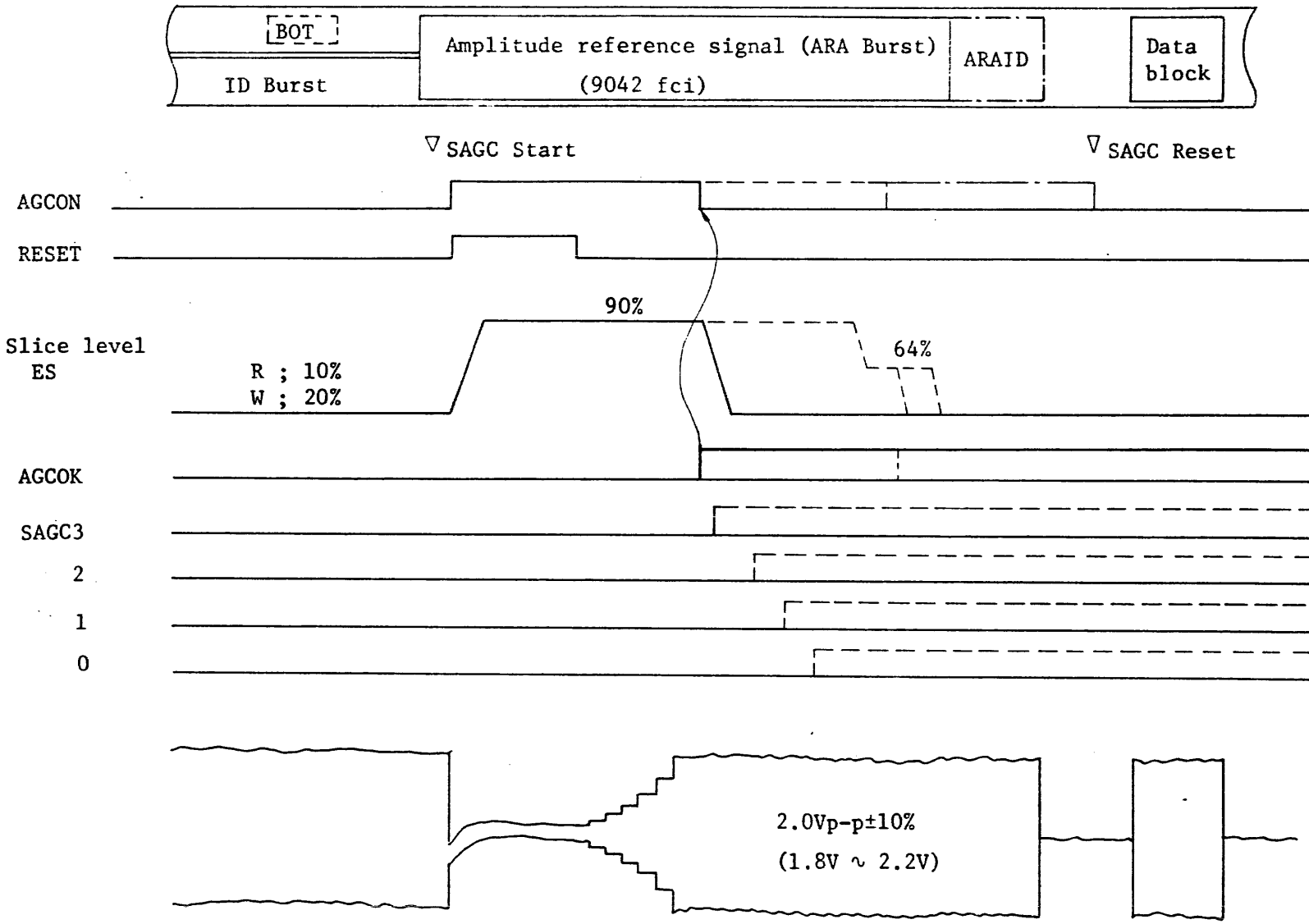


Figure 3-39. SAGC operation.

Solid line ; Normal SAGC operation (For SAGC operation 1)
Broken line; Normal SAGC operation (For SAGC operation 2)
One-dot chained line; The SAGC operation that does not terminate normally.

Gain Step Down (GSD) Operation
This operation lowers by one step, the step gain of the counter-register circuit (after reading a data block is terminated) if the amplitude of the data block is higher than required. The GSD functions independently for each track and upgrades the quality of the writing voltage level.

3.8.6 Read Circuit for the 1600/800 rpi MTU

The read circuit amplifies the output of the magnetic head, detects the PEAK write data, converts the PEAK into a pulse signal, and issues it to the FMT.

Figure 3-40 shows the read circuit. This circuit consists of a preamplifier, loop write/read wave generating circuit, filter amplification circuit, differentiation amplification circuit, NRZI demodulating circuit, skew control circuit, PEAK detecting circuit, amplitude checkup circuit, read amplifier control circuit, level control voltage generating circuit, and reference voltage generating circuit. The read amplifier control circuit, level control voltage generating circuit, and reference voltage generating circuit are used in common. The other circuits are provided independently for each track.

a. Preamplifier
This circuit amplifies the output signal from the read head. The preamplifier contains three differential amplifiers with a gain of 40 times and is housed in one integrated circuit.

b. Loop write/read wave generating circuit
This circuit converts write data (WDT) into the pseudo waveform when the MTU is operated in the loop write/read mode. The converted waveform is applied to the output of the preamplifier to execute the loop write/read operation (LWR).

c. Filter amplification circuit

This circuit consists of a filter to remove the noise contained in a signal and an amplifier to control the amplitude the output voltage read out in the NRZI mode. The filter band is switched according to tape speed. CHA is 2.0Vp-p (relative to ground) for the NRZI 800 rpi mode.

d. Differentiation amplification circuit
Since the PEAK position of a signal from the read head is at a magnetic inversion point on the tape, this circuit differentiates and amplifies the read head signal. This circuit and the filter amplification circuit accompanying an external R.C are contained on one IC. The filter is switched according to tape speed. CHB is controlled to 2Vp-p (relative to ground) in the PE mode 3200 fci (all "0" or all "1").

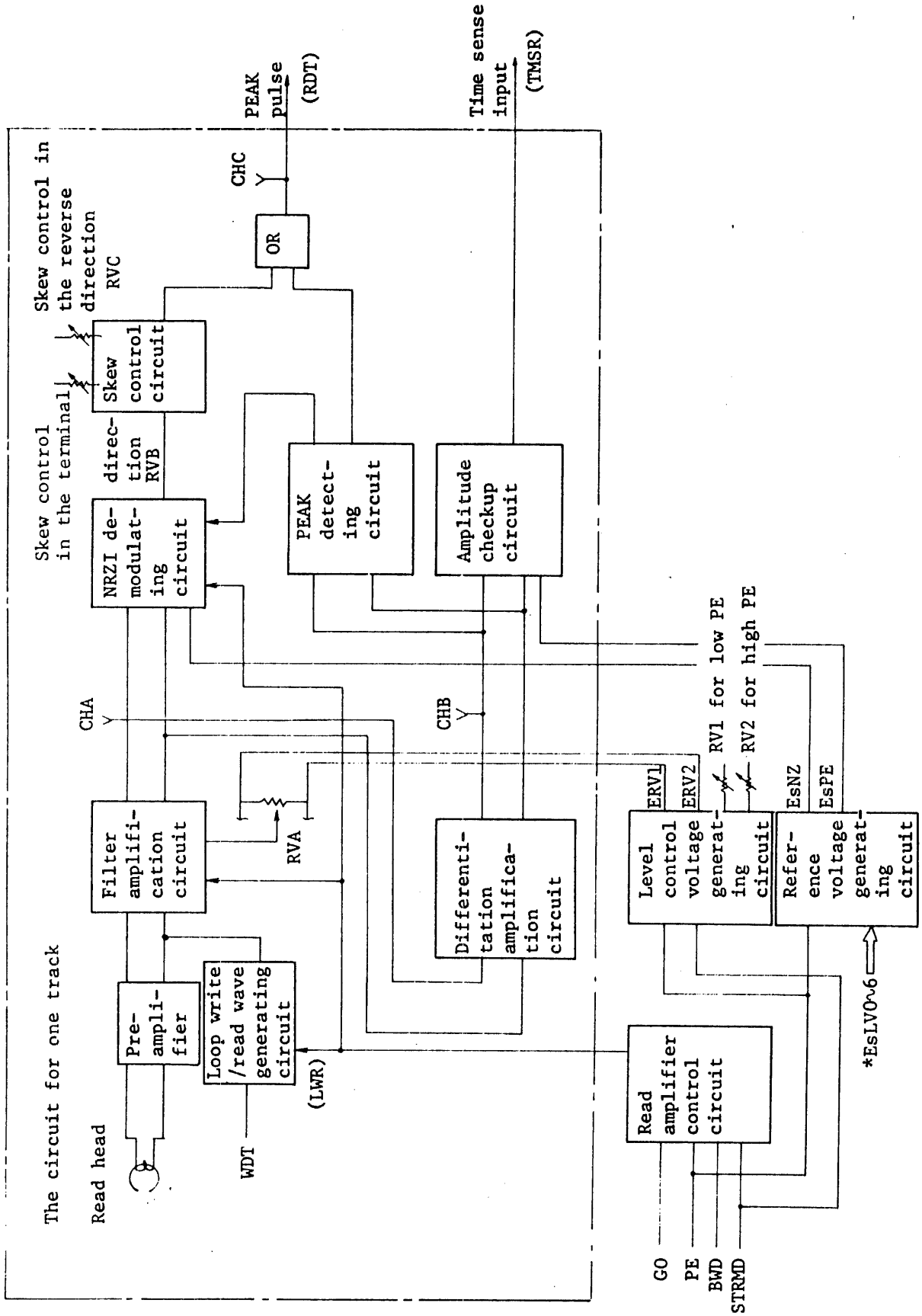


Figure 3-40. Read circuit (1600/800 rpi).

e. NRZI demodulating circuit
This circuit demodulates the NRZI mode signals into a pulse signal with the aid of amplitude information and PEAK position signal.

f. Skew control signal
This circuit is made effective when the MTU operates in the NRZI mode. It compensates for the time lag caused by skew of the read head. Skews in both forward and reverse directions are controlled individually. The CHC signal pulse is shown in Figure 3-41. The rise represents the position of the read head output PEAK; the fall represents the skew-controlled PEAK position for demodulating the FMT. The actual CHC signal is a logical negative output.

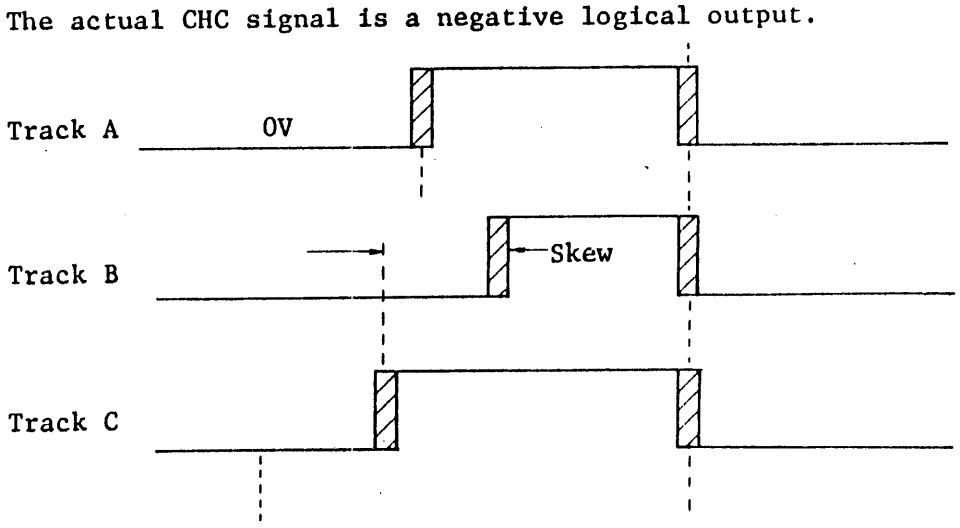


Figure 3-41. CHC pulses.

g. PEAK detecting circuit
The differentiated read signal has the PEAK position at zero volts. This circuit carries out the zero detection on read signals with opposite phases to produce a PEAK pulse output.

h. Amplitude checkup circuit
This circuit inspects whether the input signal has greater than normal amplitude. To protect against faulty operation of the read circuit network due to dropout or input signal noise, the inspection is carried out to generate an output signal when the input signal exceeds the reference voltage by a few bits. The time sense output is reset when the input signal is lower by a few bits than the reference voltage. Figure 3-42 shows the relationship between the input and output of this circuit. The time sense signal and the preceding PEAK pulse are applied to the AND gate in the interface control circuit and become a read pulse.

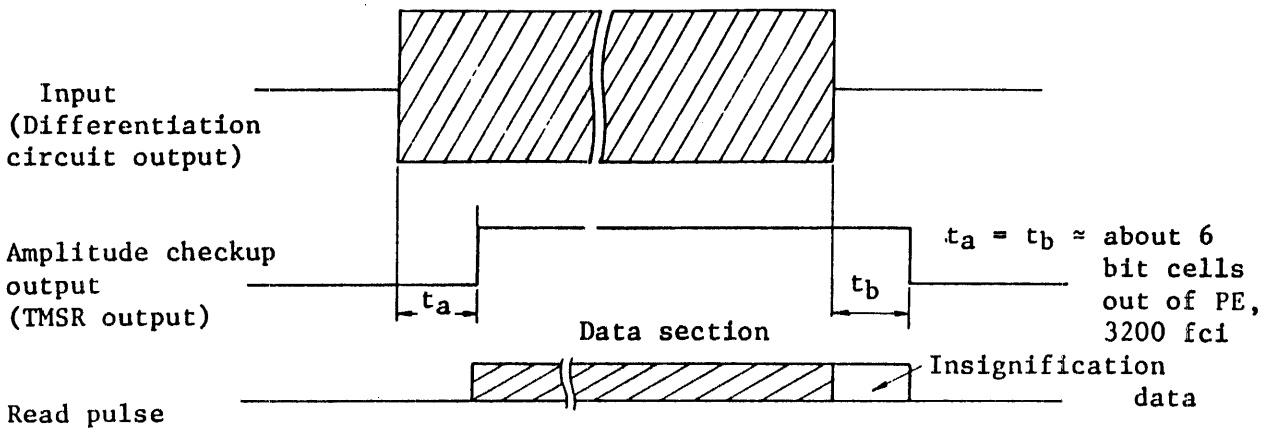


Figure 3-42. Relationship between input and output signals in the amplitude checkup circuit.

i. Reference voltage generating circuit
This circuit supplies the NRZI demodulating circuit and the amplitude checkup circuit with reference voltages EsNZ and EsPE. Reference voltages EsNZ and EsPE are specified such that bits 0 through 6 of signal EsLV represent voltage levels of 1, 2, 4, 8, 16, 64%, respectively. Signal EsLV 0 through 6 are specified in the interface control circuit of the MTU as shown in Table 3-8. Signals EsPE and EsNZ are switched by the PE signal. In addition to the above applications, a voltage level of 110% can be provided for diagnostics. Signals EsPE and EsNZ are given a voltage level higher than 150% when they are used in a different mode.

Table 3-8. Voltage levels of EsPE and EsNZ.

Application	Level Control (LVC)			PE mode (EsPE)			NRZI mode (EsNZ)		Remarks
				READ					
	0	1	2	FWD	BWD	WRITE	READ	WRITE	
OLTE	1	1	1	125%					OLTE
	1	1	0	100%					
	1	0	1	80%					
	1	0	0	64%					
	0	1	1	51%					
	0	1	0	41%					
Marginal mode	0	0	1	15%	10%	37%	26%	50%	When the NRZI mode is specified, the LVC0 and 1 are ineffective.
Normal	0	0	0	10%	7%	20%	17%	40%	

j. Level control voltage generating circuit
This circuit supplies the gain control section of the filter amplification circuit with voltages ERV1 and ERV2 for level control. Level control of the read amplifier used in the 1600/800 rpi mode is carried out as follows:

(1) In the NRZI mode, level control is carried out independently for each of the 9 tracks by RVA. The control voltage is 2Vp-p relative to ground at CHA.

(2) In the PE mode, level control is carried out for 9 tracks as a unit by RV1. The control voltage is from 1.8 to 2.2 Vp-p relative to ground at CHB.

(3) In the high-speed PE mode, level control is carried out for 9 tracks as a unit by RV2. The control voltage is from 1.8 to 2.2 Vp-p relative to ground at CHB.

k. Read amplifier control circuit
This circuit carries out filter switching of the filter amplification circuit and controls the NRZI demodulating circuit.

Input and Output Signal of the Read Circuit

Input signals are as follows:

LWR	indicates that the MTU operates in the loop write/read mode.
PE	indicates that the MTU operates in the PE mode.
BWD	indicates that the MTU operates in the backward read mode.
STRMD	indicates that the MTU operates in the streaming mode.
*EsLV 0 through 6	signals set the voltage to the reference voltage generating circuit.
GO	indicates that the tape is running.
WDT	represents write data.

Output signals are as follows:

RDT	is the turning point of information on tape for each of the 9 tracks.
TMSR	is the output signal of the amplitude checkup circuit provided for each of the 9 tracks.

3.9 Circuits for Mechanical Parts of the MTU and Stabilizing Power Supply Circuit

3.9.1 Introduction

This circuit receives signals from the microprogram control circuit and drives each mechanical MTU. The circuit network also sends signals from switches and sensors in the mechanical part to the microprogram control circuit.

3.9.2 Components

Figure 3-43 is a block diagram of this circuit.
The tape drive circuit, transistor circuit, and stabilizing power supply circuit packages are comprised of the following components:

(1) Cartridge motor drive circuit
(2) Window motor drive circuit
(3) Error marker drive circuit
(4) Moving meter drive circuit
(5) Low tape detecting circuit
(6) BOT/EOT marker detecting circuit
(7) Capstan tachometer signal transmitting circuit
(8) Switch receiving circuit
(9) Stabilizing power supply circuit
(10) Capstan drive circuit
(11) Reel motor drive circuit

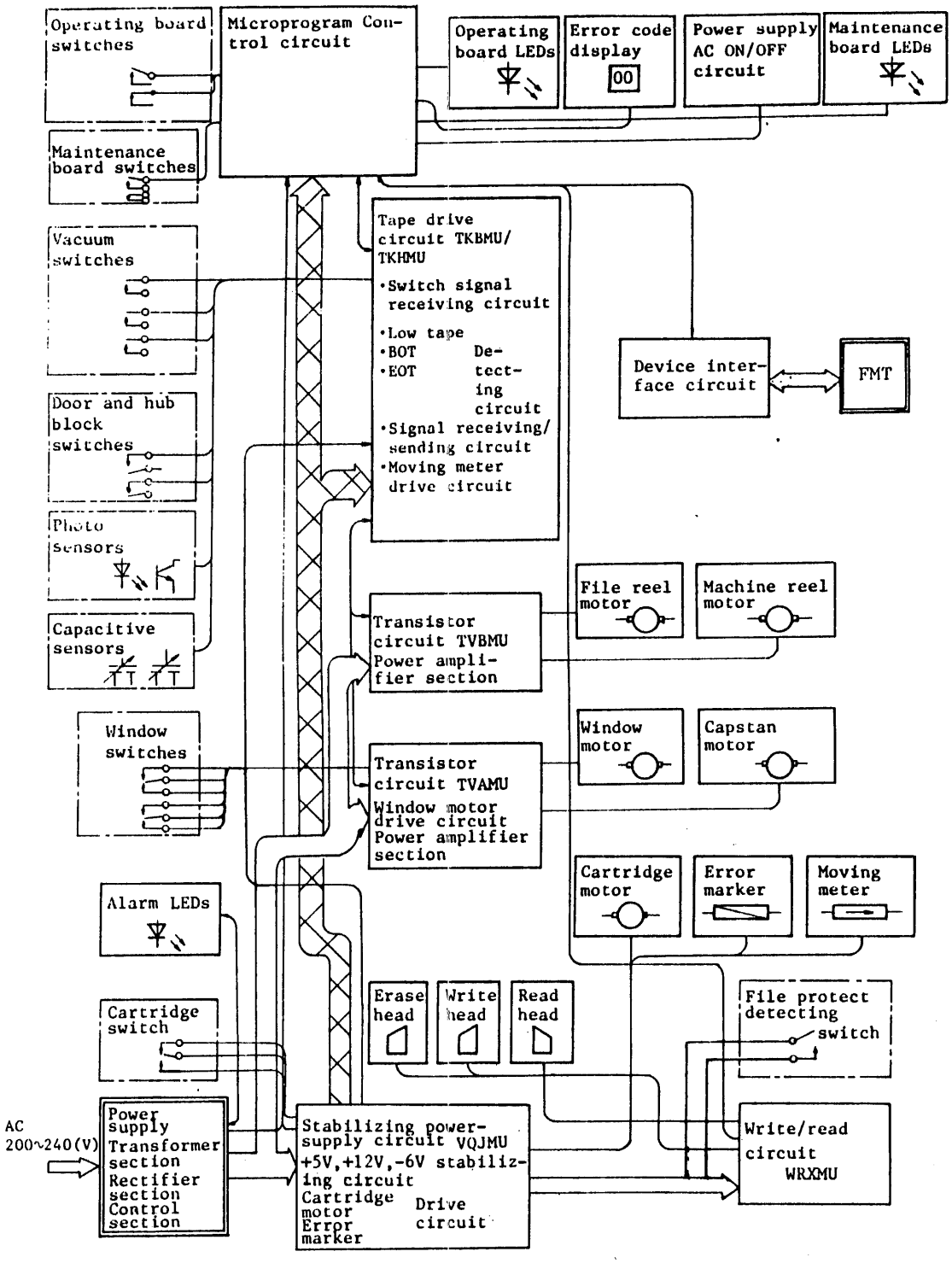


Figure 3-43. Block diagram.

3.9.3 Circuit operation

(1) Cartridge motor drive circuit
Figure 3-44 shows the cartridge motor drive circuit. when signal CTGCL is "1", the cartridge is closed. Switch SW1 detects that the cartridge has been loaded, outputs signal CTGON, and activates the cartridge open drive circuit. Switch SW2 is released when the cartridge is completely closed, and the cartridge close operation terminates. Switch SW3 is released when the cartridge is completely opened. Upon terminating the open operation, SW3 outputs signal CGOPN.

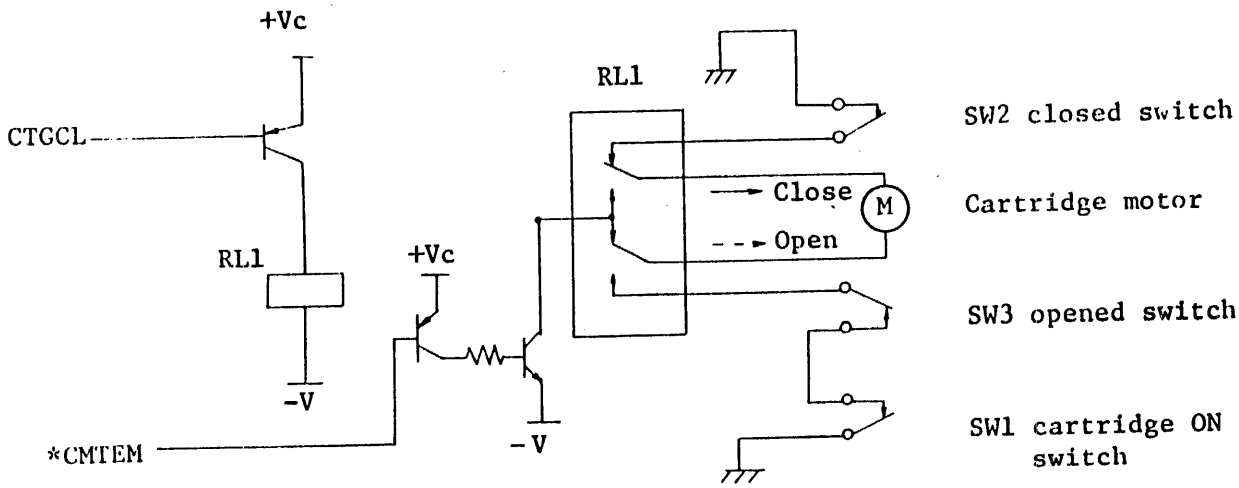


Figure 3-44. Cartridge motor drive circuit.

(2) Window motor drive circuit
Figure 3-45 shows the window motor drive circuit. When signal WNDPW is "1" and signal *WNDCL is "0", the window is closed. Switch SW1 is released when the window is completely closed. When the close operation terminates, this circuit outputs signal *WDCLS. Switch SW2 is released when the window is completely opened and the open operation terminates. Transistor Q3 is set to ON when the window motor or installed cables are short circuited, outputs signal *WNDAL, and turns on the alarm.

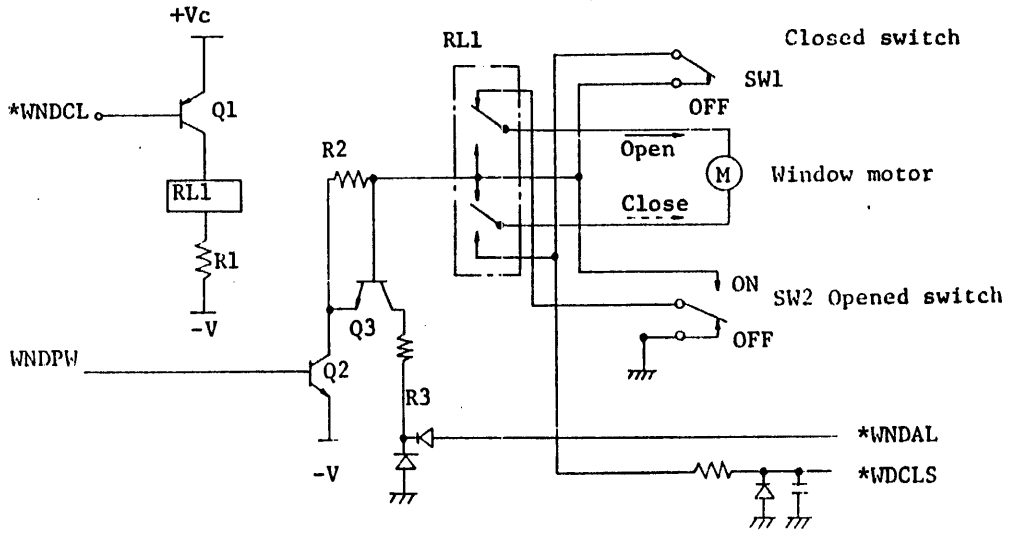


Figure 3-44. Window motor drive circuit.

(3) Error marker drive circuit

Figure 3-46 shows the error marker drive circuit. Because the operation of the solenoid used in this circuit is intermittent, its continuous operation results in overheating. Accordingly, when the solenoid is driven, the action response signal is issued to the device control circuit to ascertain that the solenoid action works normally.

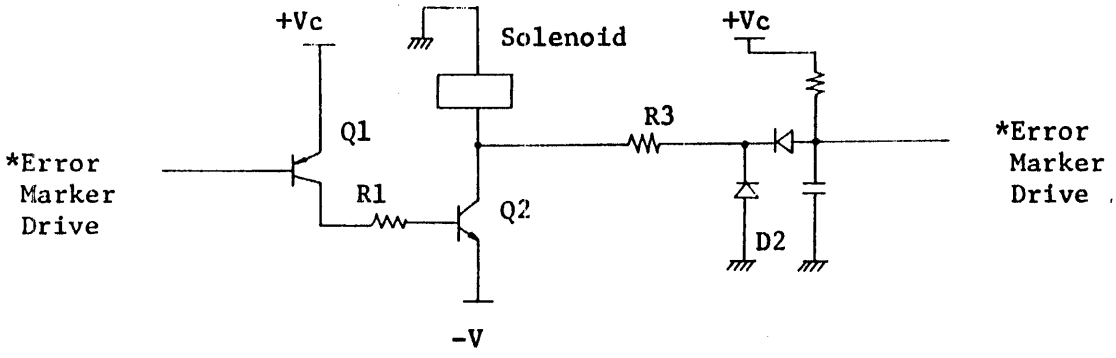


Figure 3-46. Error marker drive circuit.

(4) Moving meter drive circuit

This circuit drives an integrating time meter that indicates the total time of the tape run, excluding time for tape rewind.

(5) Low-tape detecting circuit

This circuit outputs the signal to detect that the amount of tape remaining on the machine reel during high-speed rewinding is insufficient. It also detects the amount of rotation of the machine reel during autoloading.

Figure 3-47 shows the low-tape detecting circuit. The beam emitted from the photo emitting diode is reflected by the low-tape marker when the machine reel rotates and enters the photo transistor. The output of this transistor is amplified by amplifier M1 and sent to capacitor C1. This output is compared with a predetermined slice voltage at comparator M2, which then outputs a low-tape pulse signal. Figure 3-48 shows the waveform of each section of the low-tape detecting circuit.

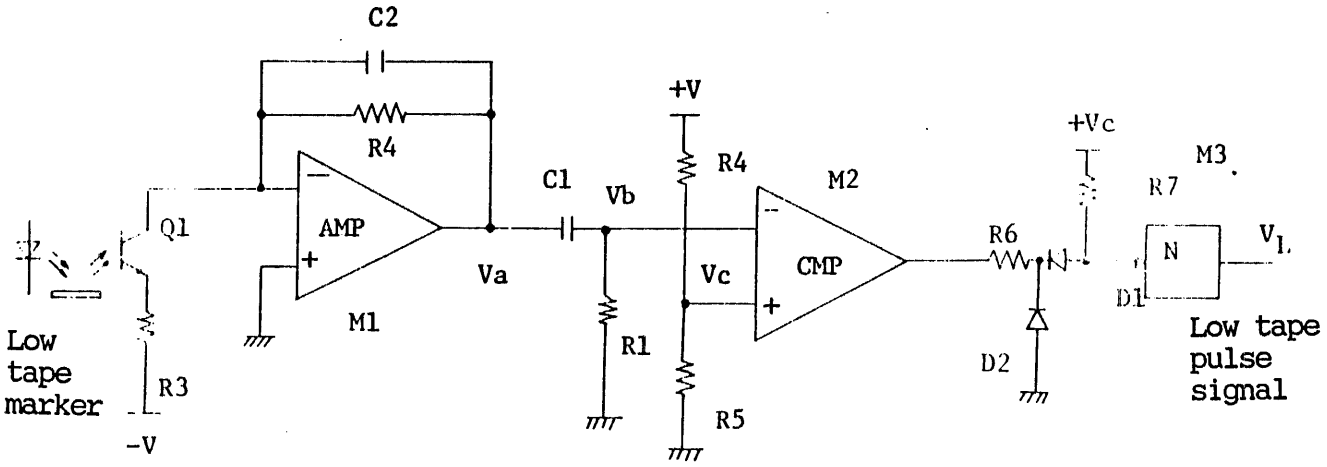


Figure 3-47. Low-tape detecting circuit.

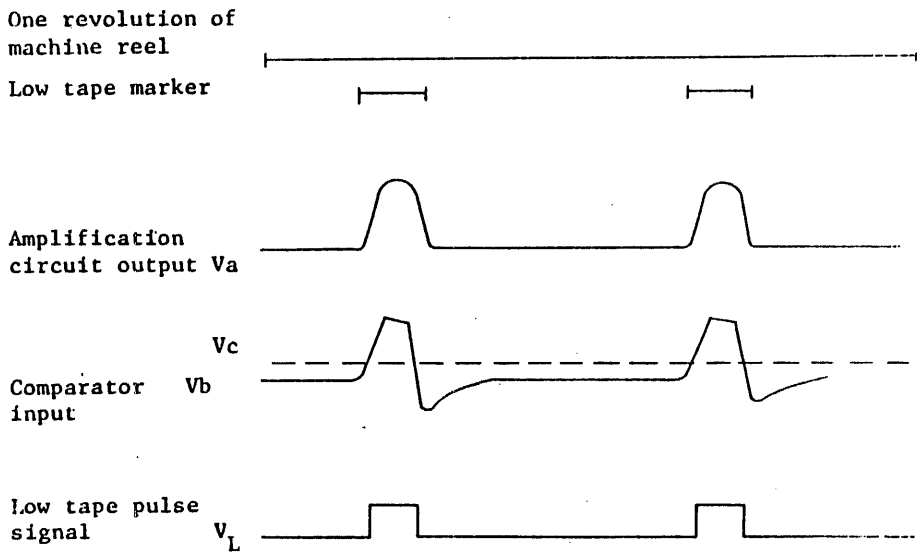


Figure 3-48. Low-tape waveforms.

(6) BOT/EOT marker detecting circuit
This circuit detects the two reflective markers BOT/EOT attached at the beginning and end of the tape. This data indicates the range of tape usable for recording. Figure 3-49 shows the BOT detecting circuit. The same circuit applies to the EOT detecting circuit.

Variable resistor RV1 detects sensitivity control. The output voltage of the photo transistor is compared with the slice voltage at comparator M1. when the former voltage is greater than the latter, a marker detecting signal is output. During execution of the marker detecting sensitivity control, when he BOT/EOT marker detecting circuit receives signal DIAG1 from the device control circuit and is set in the self-diagnosis mode, the slice voltage of comparator M1 is switched to the voltage level for marker detecting sensitivity control. Sensitivity control is achieved by adjusting variable resistor RV1 to the lighting boundary points of LED bits 4 (SBOT) and 5 (SEOT) using the field tester.

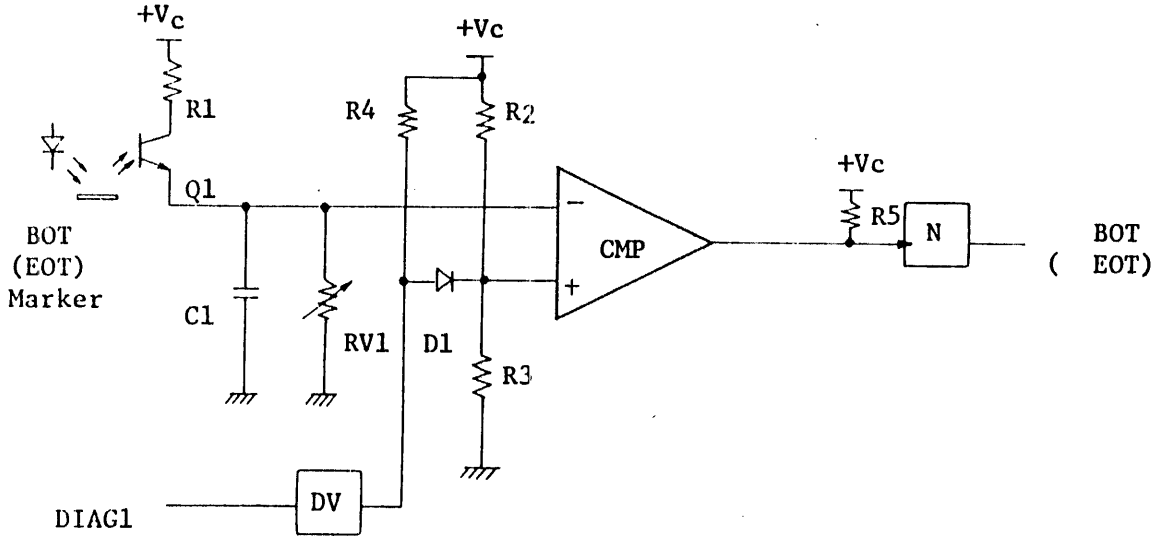


Figure 3-49. BOT/EOT marker detecting circuit.

(7) Capstan tachometer signal transmitting circuit
To detect rotation speed, rotational distance, and rotational direction of the capstan motor, a 2-phase digital tachometer circuit is incorporated into the capstan motor. This circuit supplies the tachometer circuit with power and then relays the output 2-phase tachometer signal signal to the microprogram control circuit.

(8) Switch signal receiving circuit
This circuit receives vacuum switch (right-column switch and left-column switch) signals, the door switch signal, and the reel hub lock signal and sends information to the microprogram control circuit. Inputs of the receiving circuit reflect chattering of switches. Figure 3-50 shows the structure of the switch signal receiving circuit.

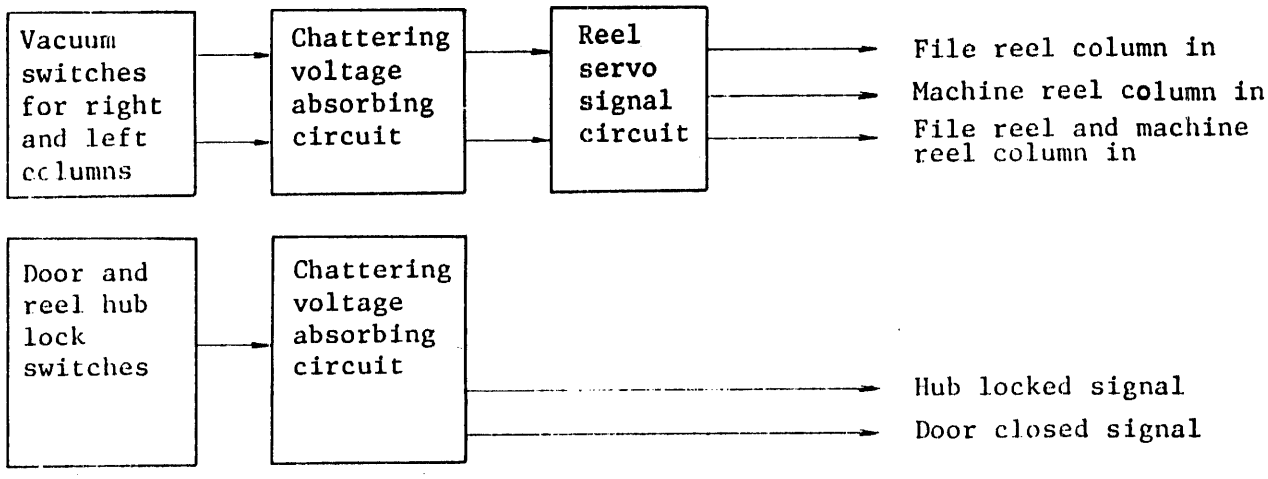


Figure 3-50. Block diagram of the switch signal receiving circuit.

(9) Stabilizing power supply circuit
This circuit stabilizes the output voltage of the device drive power supply, and supplies the tape drive circuit, microprogram control circuit, and write/read circuit networks with an output voltage of +5V. The write/read circuit networks are also supplied with output voltages of +12V and -6V. The structure of this circuit is shown in Figure 3-51.

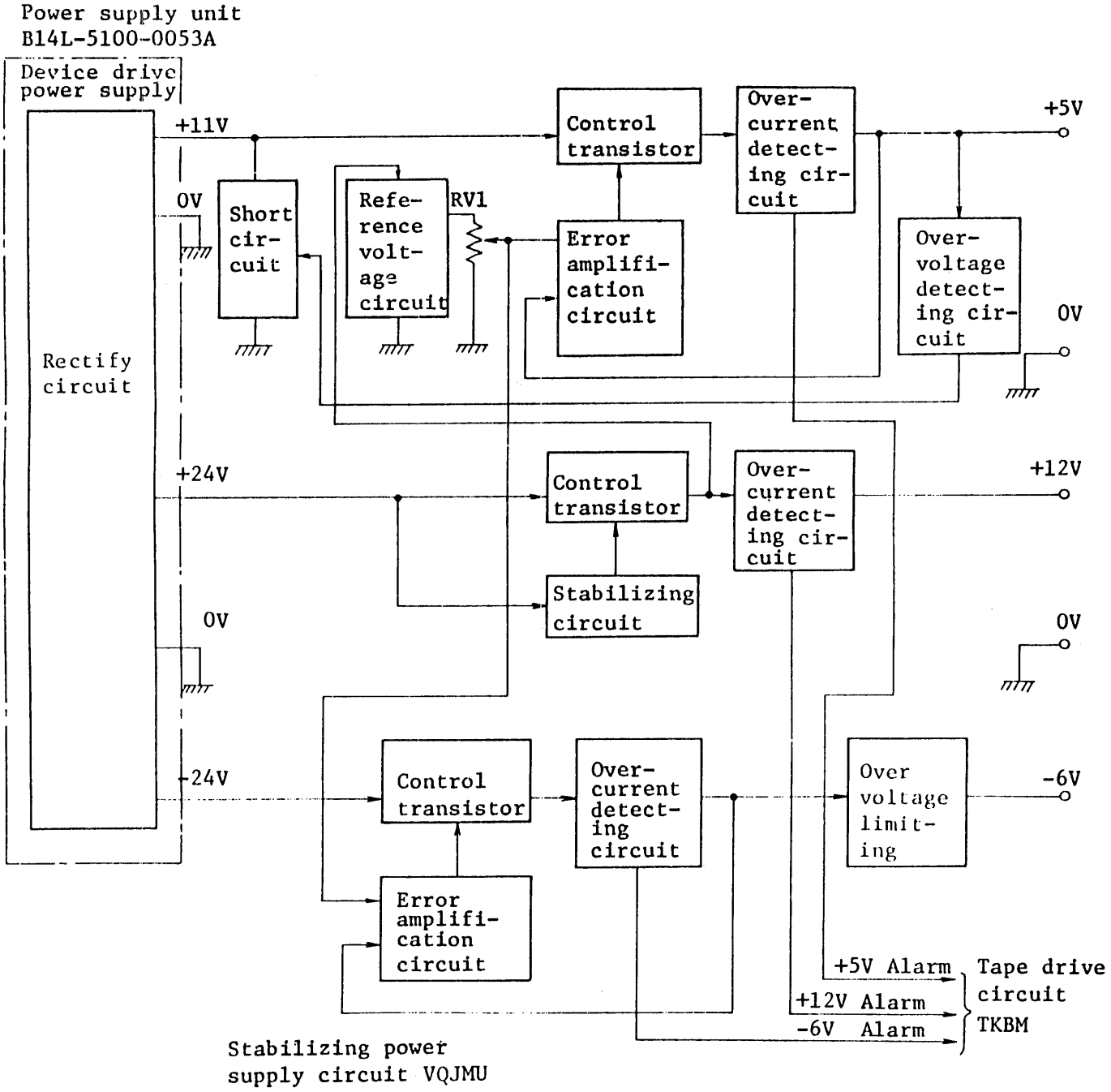


Figure 3-51. Block diagram of the stabilized power supply circuit.

a. Reference voltage circuit
This circuit supplies two stabilizing power supply circuits with a reference voltage. The reference voltage can be varied by variable resistor RV1. When the output voltage of the +5V stabilizing circuit is adjusted by variable resistor RV1 to +5V, the output voltage of the -6V stabilizing circuit (which uses the same +5V reference voltage) reaches a predetermined voltage.

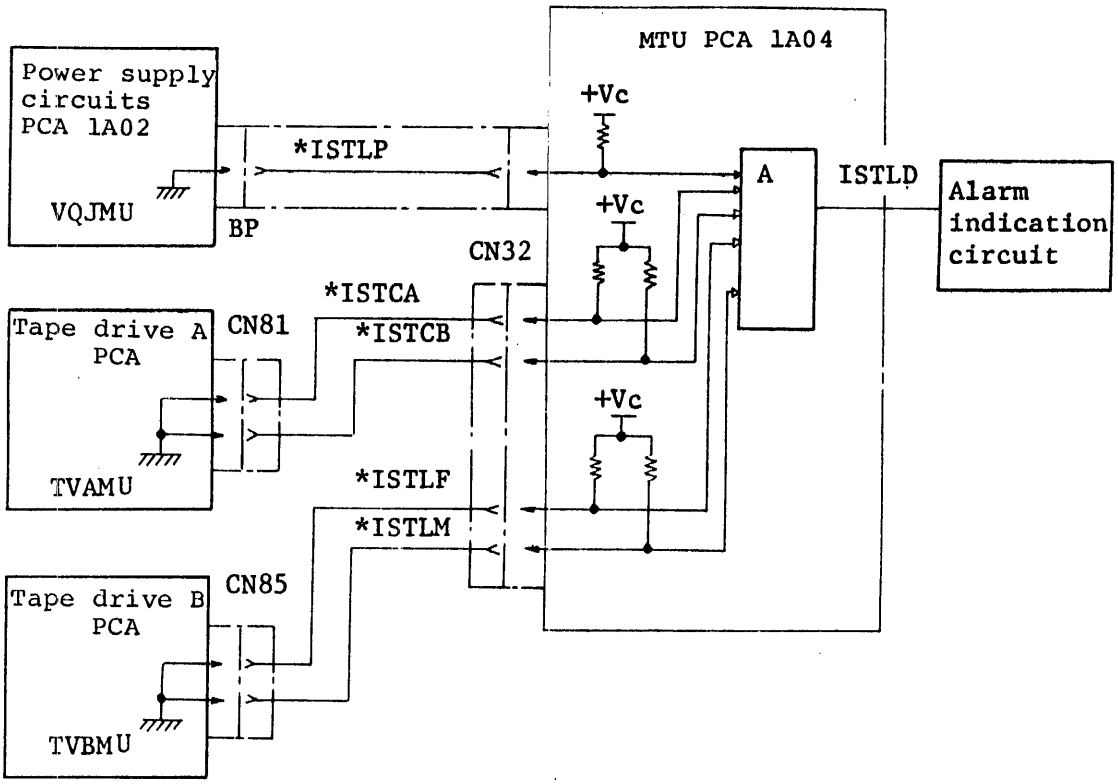
b. Error amplification circuit
This circuit compares the reference voltage and the output voltage, amplifies the difference, and drives the control transistor to compensate for voltage variation.

c. Control transistor
The control transistor stabilizes the voltages +5V, +12V, and -6V of the stabilizing circuit obtained from the error amplification circuit and the stabilizing circuit. The stabilized voltage is amplified and supplied to a load circuit.

d. Overcurrent detecting circuit
When an overcurrent flows into the stabilized power supply circuit due to a short circuit, this circuit detects the overcurrent, controls the output of the amplification circuit, and reduces the load current to protect the control transistor from being destroyed. When an overcurrent is detected, this circuit outputs the corresponding alarm signal to the power supply section and shuts off the power supply to the MTU.

e. Overvoltage detecting circuit
when the stabilizing power supply circuit fails to control the output voltage and the voltage exceeds a specified upper limit, this circuit detects the over voltage and activates the short circuit (thyrister) to fuse the device drive power supply. The power supply is shut off to protect the load circuit from being destroyed. After an overcurrent, the stabilizing power supply circuit does not recover normal operation.

f. PCA cable detecting circuits
These circuits generate the signal ISTL to ascertain whether cables between PCAs are normally connected. If connections are in error, the power supply unit is turned off and an alarm is activated.



In case connection between cables of the drive system and PCAs is not perfect, the power supply is shut off and alarm is indicated.

Figure 3-52. Install check circuit.

CHAPTER 4 POWER SUPPLY

4.1 Introduction

The power supply receives 200V AC to 240V AC single-phase power and supplies the magnetic tape units with necessary AC or DC voltage.

4.2 Functions

The power supply of the MTU is functionally divided into four circuits. Figure 4-1 shows a block diagram of the power supply. The power supply units are regulated by PCA 1A02.

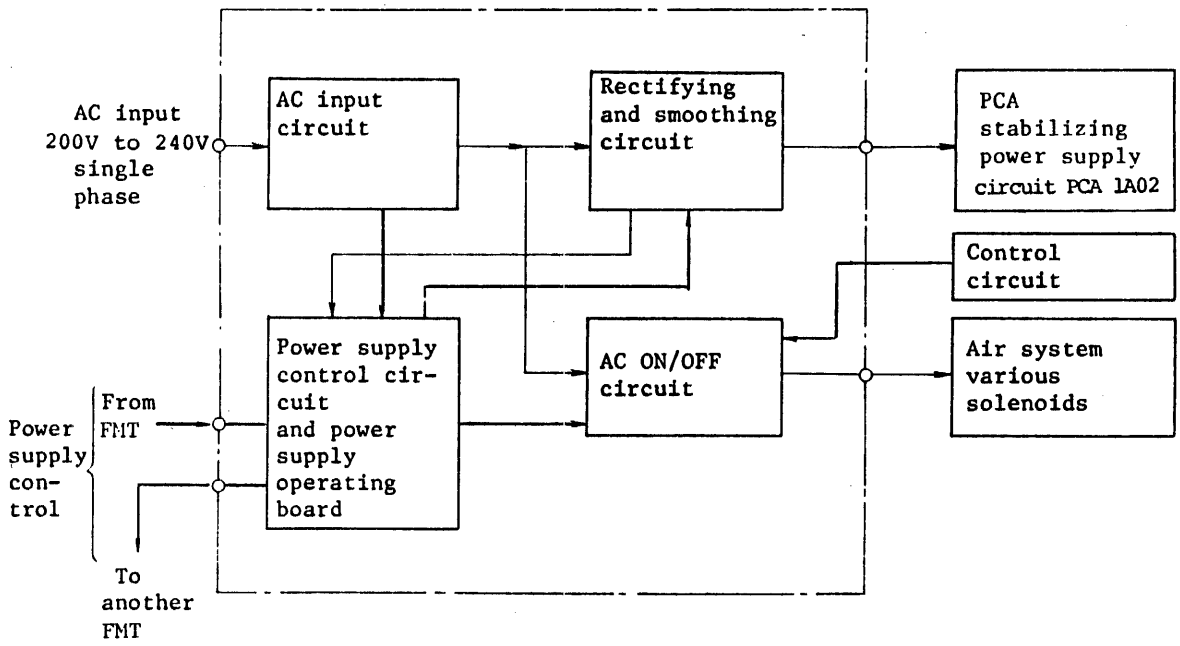


Figure 4-1. Block diagram of the power supply.

(1) AC input circuit
This circuit consists of a noise filter, circuit braker, power source, and an ON/OFF relay. AC input is turned on and off by the signal from the power control division of the FMT.

(2) Rectifying and smoothing circuit
This circuit consists of a transformer, rectifier, and a large capacitor. The DC output of the division has four levels shown in Table 4-1.

Output name	Voltage range	Fuse capacity	Application
+11V	+8.8V ∿ +13.75V	15A	Electronic circuit
+24V	+18.0V ∿ +28.8V	30A	Motor drive
-24V	-18.0V ∿ +28.8V	30A	Motor drive
-48V	-40.32V ∿ -58.6V	1.3A	Power supply control

(3) AC ON/OFF circuit
This circuit consists primarily of a relay and a magnetic contact device, and is used to drive the air system (air supply motor, etc.). It performs ON/OFF operation of the air system, control devices and turns on/off the AC drive devices, such as the solenoid of the autocleaner.

(4) Power supply control circuit
This circuit consists of a PCA with two primary functions. The first function is to receive the remote mode power on/off signal from the FMT power supply control circuit and the local mode power on/off signal from the power supply front panel to control power on/off timing for the MTU. In power on operation in the remote mode, the magnetic tape units power on sequentially with a time lag from one unit to the other to protect against rush current.

The second function is to monitor for the occurrence of an abnormal status of the MTU. A faulty status turns on the "ALARM" LED (red) indicator and informs the FMT of the abnormal status. When the power supply circuit fails, only the "ALARM" LED (red) indicator on the operating board of the MTU is lit. When a failure occurs in a circuit other than the power supply, the "ALARM" LED (red) indicator on the operating board at the MTU and the "ALARM" LED (red) indicator on the power supply operating board are both lit. The "ALARM" LED indicator on the power supply operating board is coded in four bits. Table 4-2 shows the content of failure for each code.

Table 4-2. Power alarm codes.

Alarm code (hexa-decimal)	"ALM" LED				Content of failure
	0	1	2	3	
1	off	off	off	on	+12V system short circuit or overvoltage
2	off	off	on	off	+5V system short circuit
3	off	off	on	on	Not used
4	off	on	off	off	Not used
5	off	on	off	on	Not used
6	off	on	on	off	Alarm for abnormal temperature rise at capstan power amplifier (higher than 90°C)
7	off	on	on	on	Alarm for abnormal temperature rise in +5V stabilizing power supply circuit (higher than 90°C)
8	on	off	off	off	Overcurrent and overvoltage are detected in -6V stabilizing power supply circuit network.
9	on	off	off	on	Overcurrent is detected in +12V stabilizing power supply circuit network.
A	on	off	on	off	Overcurrent is detected in +5V stabilizing power supply circuit network.
B	on	off	on	on	Overcurrent is detected in capstan power amplifier.
C	on	on	off	off	Not used
D	on	on	off	on	Overcurrent is detected in machine reel power amplifier.
E	on	on	on	off	Overcurrent is detected in file reel power amplifier.
F	on	on	on	on	Connection is not yet completed between the drive system PCA and the cable. Cable connection is not yet completed between the logic PCA and the PCA 1A04.

4.3 Power Supply Front Panel

The power supply front panel is provided with a two-position alternate switch for LOCAL/REMOTE operation and a three-position momentary switch for power on/off operation. The LOCAL/REMOTE switch determines the type of power on/off operation, either manual or remote. When the LOCAL/REMOTE switch is at the LOCAL position, the power on/off to the MTU can be performed manually by the power on/off switch. The power on/off switch is ineffective when the LOCAL/REMOTE switch is set at the REMOTE position.

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