gri-909

6
general purpose registers

GRI Computer Corporation
320 NEEDHAM STREET, NEWTON, MASSACHUSETTS 02164

Price $1.25

GRI-909

6 General Purpose Registers Manual

(S40-122)

GRI Computer Corporation, 320 Needham Street, Newton, Massachusetts 02164

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CHAPTER I

6 GENLRAL PURPOSE REGISTERS

1.1 Introduction:

The 6GPR is a firmware option that provides 6 general purpose storage registers for the GRI-909 computer. These registers can be used for argument passing or temporary storage of any data.

1.2 General Description:

1.2.1 Physical

The 6GPR option is contained on one 9 X 13 inch firmware card. It plugs in the front of the GRI-909 computer, into one of the three available firmware operator locations. As there are no Interrupt or Direct Memory Access capabilities on this card, its position in the bus is unimportant. It has built-in jumpers to pass the Interrupt and DMA Priority chain onto the next location in the bus. (This is described in the GRI-909 System Reference Manual, pages 2-16 and B-11.)

1.2.2 Electrical Specifications

Operating Temperature ----- 0 - 50°C

DC Power ---------- 1.7 Amps at +5v

CHAPTER II

OPERATION

2.1 Detailed Description:

The 6 General Purpose Registers consist of six separate 16 bit "D" type flip flop registers with their own pre-wired Source and Destination Address decoders.

They are loaded by the Destination Address Bits (DAB 0-5) decoded to the appropriate Destination Address, and Data Strobe (DSTR). They are read out by the Source Address Bits (SAB0-5) being decoded to the appropriate Source Address.

The Source and Destination Address for the six registers are as follows:

Register 1 ----- Address 30_8

Register 2 ----- Address 31_8

Register 3 ----- Address 32_8

Register 4 ----- Address 33_8

Register 5 ----- Address 34_8

Register 6 ----- Address 35_8

The data can be manipulated in and through these registers like any other register in the processor. That is, the registers may be complemented, incremented, and/or shifted left or right.

2.2 Programming:

The general registers may be loaded by any register reference instruction. This, of course, includes all register to register and memory to register instructions. The general registers may participate in any valid register transaction or data test instruction.

2.2.1 Mnemonic Register Addresses

The general registers have no permanent symbol names in either the BASE or FAST assemblers. This is done to prevent any potential user conflicts in symbols. It also permits the user to give these registers mnemonics that have specific meaning to his own usage for the registers. For example, a user may use two registers for passing arguments to subroutines, three registers for temporary storage, and one register for a counter in loop counting applications. He might then assign meaningful mnemonics with the following assembly statements:

BASE	FAST
ARG1 = 30	ARG1#1,30
ARG2 = 31	ARG2#1,31
TEMP1 = 32	TEMP1#1,32
TEMP2 = 33	TEMP2#1,33
TEMP3 = 34	TEMP3#1,34
COUNT = 35	COUNT#1,35

2.2.2 General Register Usage

A typical call for a subroutine with two arguments in memory might look like this:

BASE	FAST
MR WORD1,ARG1	WORD1 TO ARG1
MR WORD2,ARG2	WORD2 TO ARG2
JU SUBR	GO TO SUBR

On entering the subroutine, a loop count of 16_{10} (208) may have to be preset as follows:

BASE	FAST
MRI -20,COUNT	I -20 TO COUNT

At the end of the loop, the count is incremented and tested for count overflow:

BASE	FAST
RS COUNT,P1	COUNT P1
JC MSR,GEZ,LOOP	IF MSR GEZ GO TO LOOP

The temporary locations might be used to save the AX,AY, and TRP registers on entering the subroutine:

BASE	FAST
RR TRP,TEMP1	TRP TO TEMP1
RR AX,TEMP2	AX TO TEMP2
RR AY,TEMP3	AY TO TEMP3

On leaving the subroutine, the registers are restored and return is made via the TRP (stored in TEMP3):

BASE	FAST
RR TEMP2,AX	TEMP2 TO AX
RR TEMP3,AY	TEMP3 TO AY
RR TEMP1,SC	TEMP1 TO SC

NOTE: When writing in the BASE language, the user need not assign any mnemonics to the general registers. Thus, he may simply write

RRC 35,P1

to 2's complement the general register whose address is 35. The FAST language requires a symbolic entry in its symbol table (a type #1 definition) in order to distinguish between device (register) addresses and memory locations. If the user does not wish to assign particularly meaningful mnemonics to the general registers, he may use something like GR1,2,3,4,5, and 6 (see Sec. 2.2.1 for format of definition statement).

2.2.3 The GRI-909/40 includes the 6GPR option along with the EAO as standard hardware. The EAO utilizes register 30 of 6GPR along with registers AX and AY of the AO. Special software packages have been developed for the 909/40 which take advantage of the extra hardware. These package names end with a "4", i.e. $SXP4, $DXP4, $SFI4, etc. When using these software systems, the user should consult the respective program writeups to see what use they make of the 6GPR ($SFI4, Floating Point Interpretive System, uses all 6 of the registers as floating point accumulators and index storage).

CHAPTER III

TESTING

3.1 Preliminary Test:

To see that the registers transmit and receive data correctly, dial up the register Device Address in the Device Select switches on the console. Then transmit the console switches to the register by pressing the TRM key. To check that the data got there correctly, press the DISP key and the contents of the register will be displayed in the Data Display lights. Various combinations of switch register data patterns such as all 1's, 0's, alternate 1's and 0's should be tried manually to assure proper static operation.

To check the registers under program control, toggle in the following program:

Location	Machine Language	Function
40	30 0100 30	;Reg 30 Plus 1 to Self
41	30 0000 22	;Reg 30 to 22
42	31 0100 31	;Reg 31 Plus 1 to Self
43	31 0000 23	;Reg 31 to 23
44	32 0100 32	;Reg 32 Plus 1 to Self
45	32 0000 24	;Reg 32 to 24
46	10 0000 33	;SWR to Reg 33
47	33 0000 25	;Reg 33 to 25
50	34 0100 34	;Reg 34 Plus 1 to Self
51	34 0000 26	;Reg 34 to 26
52	35 0100 35	;Reg 35 Plus 1 to Self
53	35 0000 27	;Reg 35 to 27
54	00 0100 03	;Jump back
55	000040	;To beginning

The above program causes all the registers but one to increment themselves and be transferred to another location. The odd register gets the contents of the switch register. This is a simple check for interaction between the registers.

By dialing the address of the registers, you can see in the DATA DISPLAY lights the data being sent to the registers, and by dialing up the address the data is being sent to, you can see what the registers hold.

3.2 Diagnostic Program:

DGRT (79-43-018) is a comprehensive diagnostic and exercise program for testing the 6 General Purpose Registers.

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TEL: (617) 969-0800