User Manual

Model GT306
Programmable Real-Time
Clock and
Clock Calendar

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MEASUREMENT & CONTROL DIV.

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MODEL 306

PROGRAMMABLE REAL TIME CLOCK &

CLOCK CALENDAR

TABLE OF CONTENTS

FEATURES

* Direct Replacement for DEC KWV11 Series Programmable Real Time Clock
* Standard DEC Dual Height Board 8.9" x 5.2"
* All Standard DEC Features
* Totally Compatible with DEC Software
* Optional Clock Calendar with Battery Back-Up
* Programmable Square wave Output
* Alarm & Periodic Interrupt Generation

GENERAL DESCRIPTION

The Model 306 is a programmable real time clock and optional battery back-up clock calendar designed to plug into DEC's Q-bus. The 306 is a direct replacement for the DEC KWV11-A & C Programmable Real Time Clock. It is packaged on the standard 8.9" x 5.2" DEC style dual height board and is electrically and mechanically compatible with DEC's LSI-11, 11/2 and 11/23 Microcomputer Series.

The 306 consists of a 16 bit programmable counter which can count at one of five software selectable crystal controlled frequencies, an external clock, or jumper select the BEVENT line (50/60 Hz) or clock calendar square wave output. The counter can be programmed to operate in any one of four modes. Mode Ø consists of timing a single interval. Mode 1 is the same as Mode Ø except that the counter is reloaded and restarted. Mode 2 is used to time an external event by loading the count of the free running counter into a buffer via an external Schmitt triggered input. This result can then be read by the processor. Mode 3 is the same as Mode 2 except that the counter is reset to zero.

If desired, the processor may be interrupted when a counter overflow occurs or an external event takes place. For the purpose of triggering external events, the clock overflow signal is brought out to a 40 pin connector. The 306 is ideally suited for controlling and synchronizing external processes, such as triggering A/D converters, or it may be used as a watch dog timer.

The 306 may also be equipped with a battery backed-up clock calendar, which is a complete time of day clock with interrupt alarm, one hundred year calendar, a programmable periodic interrupt and a programmable square wave generator. The data can be read as BCD or binary.

SPECIFICATIONS

Clock	10 MHz crystal oscillator
Oscillator Accuracy	0.01%
Program Selectable Clock Ranges	1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz, External Clock, Line Frequency or Square wave output
Input Signals	
Schmitt Trigger Inputs	2
Maximum Input Voltage	±30 Volts
Trigger Range	TTL or Pot selectable ±12 Volts
Trigger Polarity	Jumper selectable Pos. or Neg.
Trigger Source	User Device
Hysteresis	Approximately 0.5 Volts
Output Signals	
Clock Overflow	500 nsec. neg. pulse
Output Characteristics	Open collector driver with 470 ohm pull-up to 5 Volts. Source current max. is 5 ma @ 2.4 Volts. Sink source max. is 8 ma @ 0.4 Volts
Schmitt Trigger Inputs	2. Same as Clock Overflow
Clock Calendar (Optional)	
Oscillator Accuracy	.003%
Programming Format	Binary or BCD Representation of Time, Calendar, and Alarm
Mode	12 or 24 hour clock with AM PM flag in 12 hour mode

Battery Back-up	7 days fully charged
Battery Back-up Supply Current	100 microamps
Leap Year	Automatic 100 year calendar
Daylight Saving Time	Yes
Bus Interface	Q-bus. Direct Replacement for KWV11 Series
Addressing	Jumper Selectable 776000_8 to 777740_8
Base Vector Range	0 to 760_8
Priority Level	Level 4
Mechanical & Environmental	
Dimensions	DEC LSI-11 standard 8.9" x 5.2" dual height board
Power Requirements	5 Volts @ 1 Amp
Bus Loading	3 AC Load, 1.5 DC Load
Operating Temperature Range	0 to 55°C
Storage Temperature Range	0 to 75°C
Relative Humidity	To 85% non-condensing
Mating Connector	3M P/N 3417 (40 Pin) or equivalent

Q-BUS INTERFACE

The Q-bus interface consists of address/data transceivers, an address comparator, and I/O select and control logic. Refer to Figures 1 and 2.

During the addressing portion of a bus cycle, the Address/Data transceivers are in the receive mode. Address lines 12 through 2, gated by bus line BBS7, are compared to the base address setting selected by the address selection jumpers. When the correct address is asserted by the

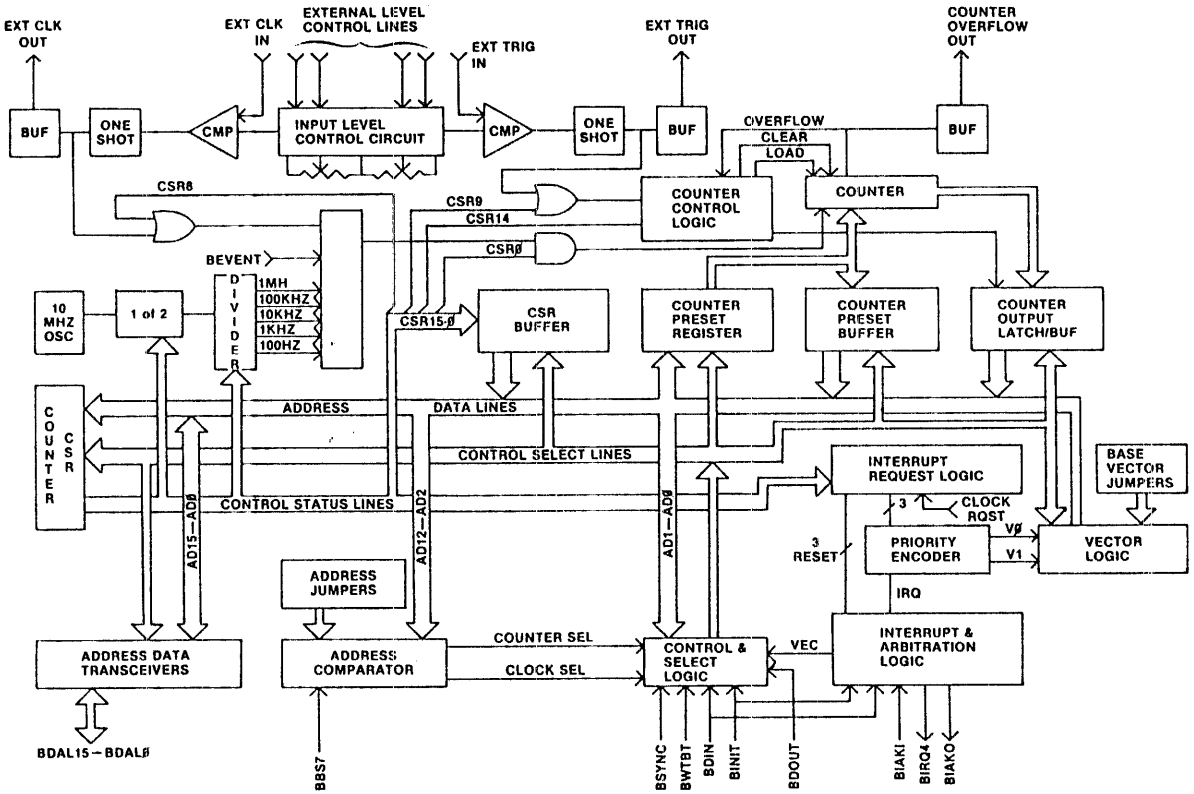


Figure 1

Functional Block Diagram

Model 306

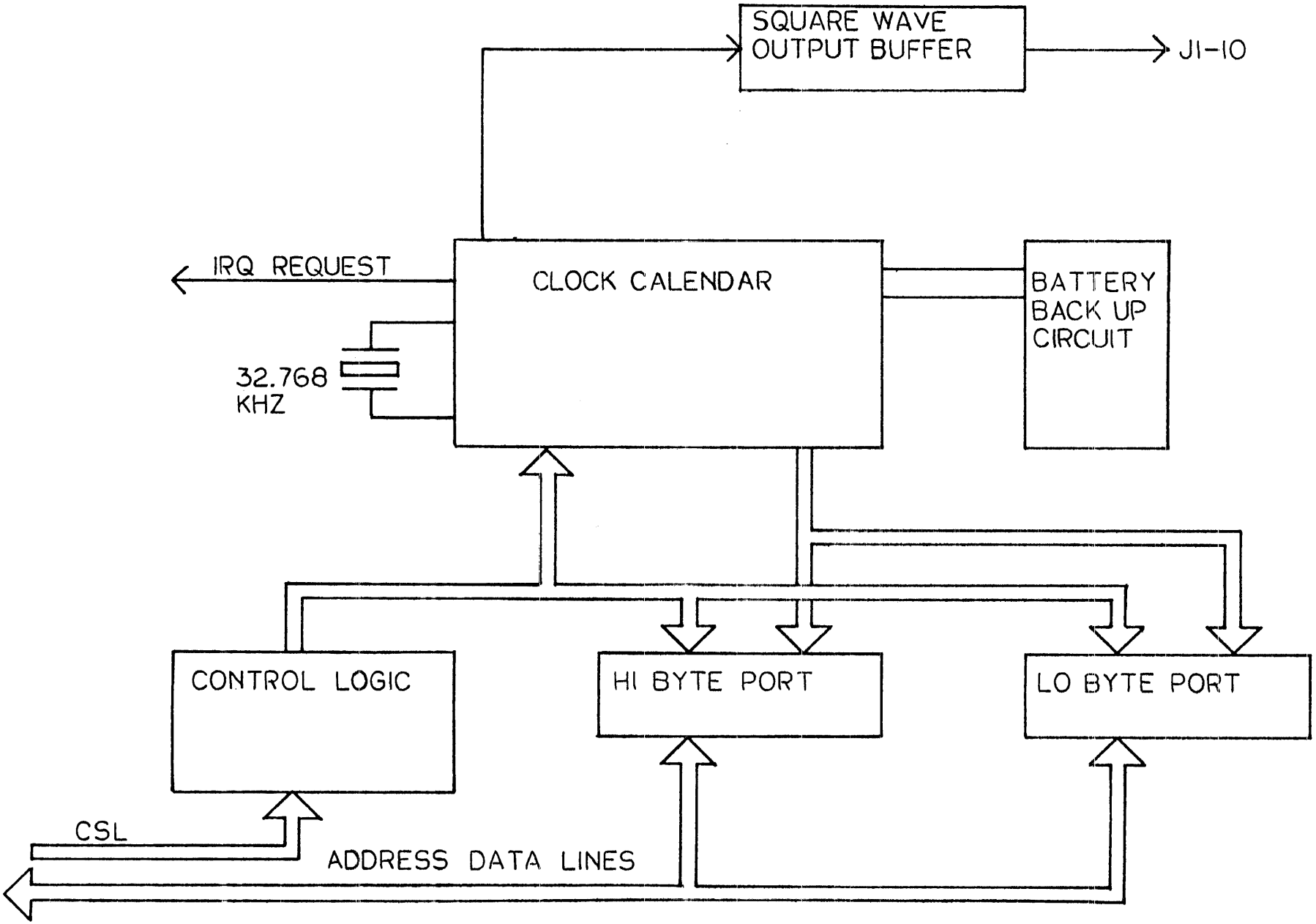


Figure 2

Clock Calendar Block Diagram

processor, the comparator output (COUNTER SEL or CLOCK SEL) is asserted. This, in conjunction with the assertion of BSYNC is used by the Control and Select Logic (CSL) to select the appropriate on-board logic register for the remainder of the bus cycle.

If the processor is performing a read, then the BDIN line is decoded in conjunction with the CSL to enable the tri-state buffers of the selected register, place the bus transceivers in the transmit mode, and then assert the BRPLY line.

If the processor is performing a write operation, then the register which is to be written to is selected during the Address/Data portion of the bus cycle and the BDOUT line is used to clock the latches of the receiving register, and to assert BRPLY.

INTERRUPT LOGIC

The interrupt circuit consists of interrupt request logic, a priority encoder, interrupt level logic, arbitration control, and vector logic.

The interrupt request logic contains three latches, one for the counter overflow, one for the ST2 Flag, and one for the clock calendar. When the appropriate interrupt request enable bit is set, that latch will become set upon setting the condition flag.

The output of each latch is fed into a priority encoder which controls the vector logic output of the appropriate vector during interrupt servicing.

When more than one on-board request is pending, the interrupt and arbitration logic clears the latch of the request being serviced, leaving the other requests pending. This logic also controls the interrupt grant signal BIAKI by either inhibiting the signal or allowing it to pass.

The on-board interrupt priority is:

Level	Description	Base Vector Offset
Highest	Counter Overflow	Base +Ø
	ST2 Flag	Base +4
Lowest	Clock Calendar	Base +10

COUNTER, CONTROL & STATUS LOGIC

The Counter, Control and Status Logic consists of the counter clock frequency select logic, the Control & Status Register (CSR), the CSR buffer, a Counter Buffer Register (CBR), Counter Preset Register (CPR) and Counter Preset Buffer (CPB).

The CSR contains the logic necessary for setting up and controlling the various operating modes of the counter.

The CSR buffer is used to read back the CSR status.

The CBR is used to store the instantaneous count of the counter whenever the ST2 input is triggered.

The CPR is where the processor writes the count for Modes Ø and 1. The CPB allows the CPR to be read back.

16 BIT COUNTER

The counter is a 16 bit counter with asynchronous clear and load and counts at one of eight software selectable rates. The counter overflow is used to fire a one shot which sets the overflow flag of the CSR. The output of the counter is connected to the Counter Buffer Register such that the firing of the ST2 input in Modes 2 and 3 causes the instantaneous count to be loaded into this register. The Counter Preset Register output is connected to the counter input. During Modes Ø and 1, the contents of this register is loaded into the counter whenever the GO Bit is set.

CLOCK OSCILLATOR & DIVIDER LOGIC

Five of the eight program selectable counter clock frequencies are generated by a 10 MHz oscillator. The output of the oscillator is fed into a five decade divider which generates the user selectable clock rates of 1 MHz, 100 kHz, 10 kHz, and 100 Hz. These outputs are fed into a one of eight multiplexer of which the other three inputs are tied to the BEVENT line, the ST1 external input line from the connector, and ground to generate the counter stop selection.

CLOCK CALENDAR CIRCUIT

The clock calendar circuit contains a 32.768 kHz time base oscillator. The oscillator output is fed into counter logic which generates the time of day and calendar functions. The

counter outputs are buffered so that their count is never read directly. Fifteen taps of the counter logic are fed into a one of fifteen selector which is controlled by the periodic interrupt and square wave rate selection logic. The output of the selector is brought out to the I/O connector through a buffer.

The clock calendar also includes bus interface circuitry, clock calendar buffer update logic, and four alarm bytes, eighteen bytes of user selectable RAM, and four control and status bytes.

During a power failure, the clock calendar continues to keep track of time through its battery back-up circuit. The user RAM is also protected. A fully charged battery will keep the clock running for a minimum of seven days and a fully drained battery will be charged within eight hours of power applied to the system.

COUNTER TIMER OPERATING MODES

Mode Ø - Single Interval Timer

Mode Ø is suited for timing a single event. In this mode setting the GO bit (Bit Ø of the CSR) causes the contents of the Counter Preset Register to be loaded into the counter and starts the counter. The GO bit may be set directly under program control or by an external event triggering the ST2 input. Before the ST2 input may be used to set the GO bit, the ST2 Trigger Enable bit (Bit 13 of the CSR) must be set.

The counter counts at the frequency selected by the CSR until the counter overflows. The counter overflow clears the GO bit and sets the overflow flag (Bit 7 of the CSR). If the interrupt enable bit (Bit 6 of the CSR) is set, an interrupt will be generated.

Since the counter always counts up, the Counter Preset Register should be loaded with the 2's complement of the desired count.

Mode 1 - Repeated Interval Timer

Mode 1 is identical to Mode Ø except that when the counter overflows, the GO bit is not cleared. Instead, the counter is reloaded with the contents of the CPR and the counter is restarted.

Mode 2 - External Event Timing

Mode 2 can be used to time external events. Setting the GO bit clears the Counter Buffer Register and starts the counter counting from Ø at the rate selected by the CSR. When the ST2 input encounters a signal which will trigger it, the instantaneous count of the free running counter is loaded into the Counter Buffer Register, and the ST2 flag (Bit 15 of the CSR) is set. The program can then read the Counter Buffer Register to obtain the count. The act of reading this register does not clear the register.

If the ST2 Interrupt Enable bit is set then the processor will be interrupted when the ST2 flag is set.

Mode 3 - External Event Timing for Zero

Mode 3 is identical in operation to Mode 2 except that the counter is cleared and restarted from Ø as a result of an ST2 input.

HARDWARE CONFIGURATIONS

The hardware selectable function of the 306 consists of the base address, vector address, clock calendar enable, clock calendar RAM size, clock calendar power and selecting either 60 Hz (BEVENT) or the square wave output of the clock calendar as one of the eight available time bases of the counter timer.

FACTORY CONFIGURATIONS

The Model 306 is shipped configured as follows:

Clock Calendar Base Address	170400_8
Counter Timer Base Address	170420_8
Vector Base Address	440_8
Counter Timer Clock Base 7	BEVENT (50/60 Hz)
Clock Calendar Power	+5V system power
Clock Calendar Enables	Yes

SETTING THE COUNTER TIME BASE ADDRESS

The base address of the 306 can be set to reside anywhere within the I/O Page. The location of the base address jumpers (JP3) is found on Figure 3.

To change the counter timer base address requires re-configuring the base address jumpers. To set an address bit to Ø requires the installation of a jumper between two adjacent pins. To set an address bit to 1 requires no jumper. As an example, the factory configured base address is 170420_8. To set this base address requires installing jumpers at posts B11, B10, B9, B7, B6, B5, B3 and B2 of JP3 and removing any jumpers at posts B12, B8 and B4.

CLOCK CALENDAR ADDRESS & RAM SIZE

When the 306 is equipped with the clock calendar option, the board's base address is determined by address selection jumpers B12 through B2; however, address selection jumpers B4 through B2 are used to also set the clock calendar address and the size of the clock calendar RAM. Jumper post B5 must always be set to Ø.

The base address of the counter timer is still a function of all the address selection jumpers; however, the starting address of the clock calendar is equal to the address set by jumpers B12 through B6 and B5 set to Ø. The

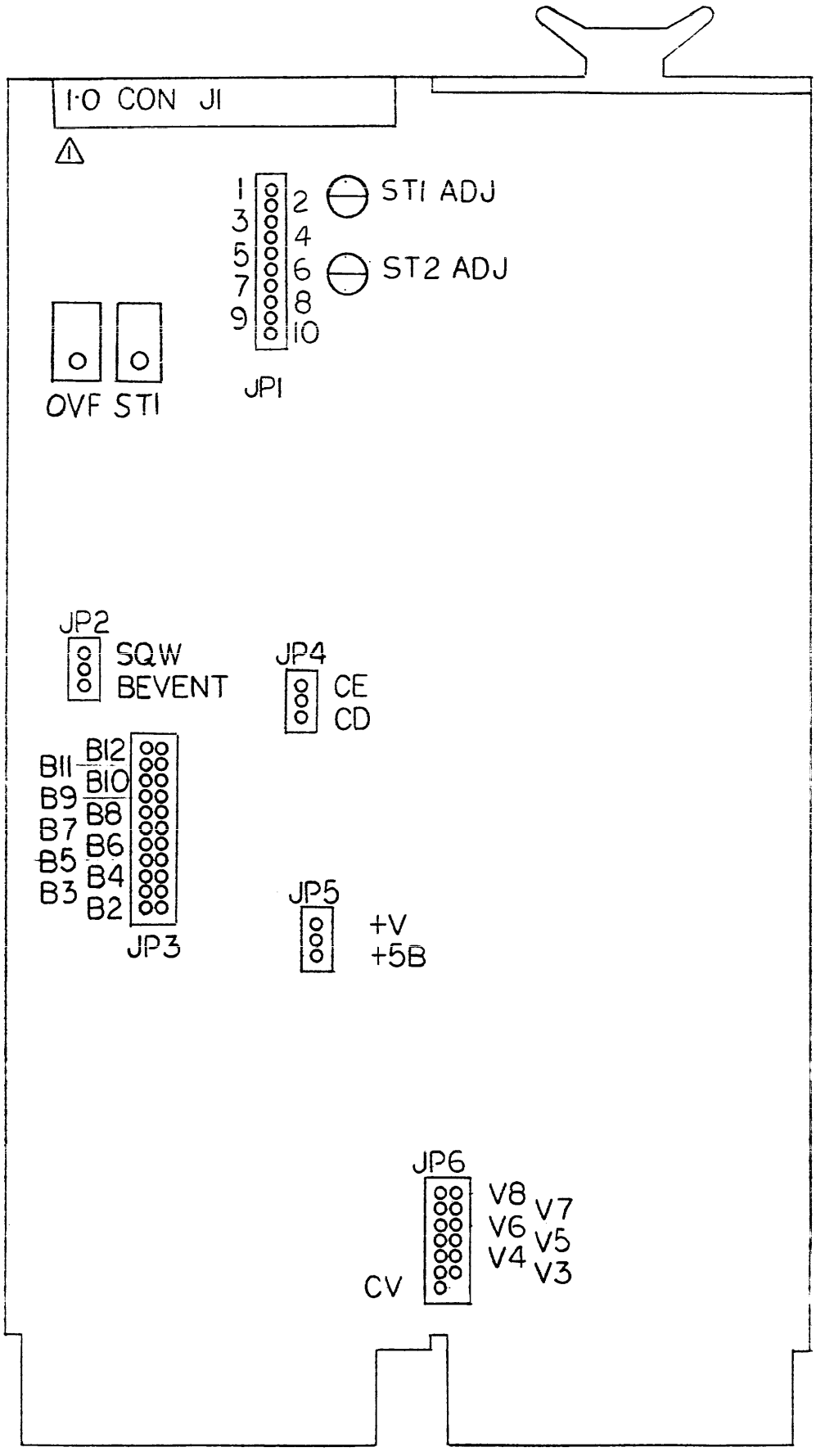


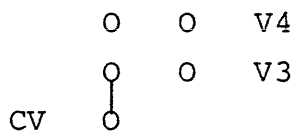
Figure 3

Model 306 Layout Diagram

numerical difference between the base set by jumpers B12 through B5 and the additional jumpers B4 through B2 determines the number of bytes the clock calendar will occupy between the primary base address (bits 12-5) and the counter timer base address (bits 12-2). This size can vary from Ø bytes, (no clock calendar selected) to 28 bytes (14 clock calendar bytes and 14 RAM bytes). As an example, the factory configured base address when the clock calendar option is installed is 770420_8. The clock calendar occupies addresses 770400_8 through 770417_8 and the counter timer resides at 770420 and 770422. In other words, the clock calendar occupies the address space between the counter timer base address which is set by all the address selection jumpers and address bits 12 through 5 only.

SETTING THE VECTOR

The vector address of the 306 can be set from 0 to 760_8 in increments of 10_8 or 20_8 with clock calendar interrupts. The location of the vector select jumpers JP6 are found by referring to Figure 3. A "1" is set by removing a jumper, a "Ø" is set by installing a jumper. When the clock calendar option is installed, an interrupt will be generated by this option. Jumper V3 must be connected to CV as shown:



Clock Calendar Vector Jumpers

TIME BASE 7 SELECT

The counter timer is set at the factory such that selection of time base 7 will input the BEVENT line (50/60 Hz) to the counter. If the 306 is equipped with the clock calendar option, the square wave output may be jumper selected in place of the BEVENT line. JP 2 is used for this purpose.

DISABLING THE CLOCK CALENDAR

JP 4 is used to completely disable the clock calendar. Connecting post CE to the center post enables the clock calendar, connecting CD to the center post disables the clock calendar.

SELECTING ALTERNATE SYSTEM POWER

JP 5 is used to select an optional power source for the clock calendar if it is available on the +5B line on the bus. For normal operation the +V pin is jumpered to the center pin of JP 5. The optional power is selected by removing the +V jumper and installing a jumper from the +5B pin to the center pin of JP 5.

COUNTER TIMER PROGRAMMING

CSR Register Description (Base Address +Ø)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø
ST2F	ST2 IE	ST2E	ERR FLG	OSCM SEL	OSCM	ST2M	ST1M	OVF	OIE	R2	R1	RØ	M1	MØ	GO

ST2F FLAG BIT 15 (Read/Write to Ø)

The ST2 Flag is set by setting the ST2M bit of the CSR or whenever an external event triggers the ST2 input provided that GO bit or the ST2E bit has been previously set.

The ST2F bit is cleared under program control or reset. Setting the GO bit will also clear this flag unless ST2E (bit 13) is set.

ST2IE: ST2 INTERRUPT ENABLE BIT 14 (Read/Write)

Setting the ST2 IE bit will cause an interrupt to be generated as a result of setting the ST2 Flag (Bit 15).

ST2E: ST2 ENABLE BIT 13 (Read/Write)

Setting the ST2E bit will cause the GO bit to be set whenever the ST2 Flag is set. This bit is cleared under program control by a reset or by setting the GO bit. Thus, when the GO bit becomes set as a result of the ST2 Flag, this bit is cleared.

ERR FLG - ERROR FLAG BIT 12 (Read/Write

This bit is set whenever an ST2 Flag or Overflow Flag overrun occurs. This bit is set and cleared under program control and cleared by reset or setting the GO bit.

OSCM SEL - MAINTENANCE OSC. SELECT BIT 11 (Read/Write)

This read/write bit is used to select the on-board 10 MHz oscillator (bit 11 = Ø) or the OSCM bit (bit 11 = 1) as the decade counter clock. Cleared by reset.

OSCM - OSCILLATOR MAINTENANCE BIT 10 (Write Only)

Writing a one to this bit will cause one clock pulse to be output to the counter timer divider when Bit 11 the OSCM SEL, is set to 1. Always reads Ø. Used for testing purposes.

ST2M - ST2 MAINTENANCE BIT 9 (Write Only)

Writing a one to this bit simulates an ST2 input. Always reads Ø. Used for testing purposes.

ST1M - ST1 MAINTENANCE BIT 8 (Write Only)

Writing a one to this bit simulates an ST1 input pulse. Always reads Ø. Used for testing purposes.

OVF - OVERFLOW FLAG BIT 7 (Read/Write to Ø)

Set whenever the counter timer overflows. Cleared under program control, reset, or setting the GO bit.

OIE - OVERFLOW INTERRUPT ENABLE BIT 6 (Read/Write)

Set and cleared under program control or cleared by reset. When set, an interrupt will be generated whenever the OVF bit is set.

R2, R1, & RØ RATE SELECT BITS, BIT 5, 4, & 3 (Read/Write)

These read/write bits are used to select the counter timer clock rate as depicted by the following table:

R2 Bit 5	R1 Bit 4	RØ Bit 3	Rate
0	0	0	STOP
0	0	1	1 MHz
0	1	0	100 kHz
0	1	1	10 kHz
1	0	0	1 kHz
1	0	1	100 Hz
1	1	0	ST1
1	1	1	BEVENT or SQW OUT

Counter Timer Rate Selection

M1 & MØ - MODE SELECTION BITS, BIT 2 & 1 (Read/Write)

These bits select the counter timer mode of operation as illustrated in the following table:

M1 Bit 2	MØ Bit 1	MODE
0	0	Mode Ø
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3

Mode Selection

GO BIT, BIT Ø (Read/Write)

All actions of the counter timer are initiated by setting this bit as determined by the Rate and Mode Select bits of the CSR. This bit is set and cleared under program control or when the ST2 Flag is set if the ST2E is also set. This bit is cleared by reset or when the counter overflows in MODE Ø operation.

COUNTER PRESET & BUFFER REGISTERS (Base Address +2)

During Modes Ø and 1, the Counter Preset Register is automatically selected by the hardware. The program deposits the 2's complement of the count into this address where it will remain unchanged until reset or changed by the program. When the GO bit is set in the CSR, the contents of this register is loaded into the counter.

During Modes 2 and 3 the counter buffer register is automatically selected by the hardware. Whenever the ST2 input is triggered as a result of an external signal, the instantaneous count is loaded into this read only register. The program interrogates this address for the count.

CLOCK CALENDAR PROGRAMMING

CLOCK CALENDAR

The clock calendar contains a complete time of day clock with alarm and one hundred year calendar, a programmable periodic interrupt and square wave generator and up to 14 bytes of user selectable RAM. The clock calendar with RAM has two distinct uses. First, as a battery backed up RAM, timer, and calendar. Secondly, it may be used to relieve the software of the timekeeping workload.

Programming the clock calendar should be done through byte instructions. Reading a clock calendar location with a word instruction will cause the high or low byte to be loaded with unknown data. The invalid data will be loaded in the byte opposite of which byte is addressed through Bit Ø.

Writing data to the clock calendar should also be done through byte instructions. The high or low byte data will be lost if an attempt to write a word is made. The lost byte will be the one opposite of Bit Ø of the address.

ADDRESS MAP

Table 1 shows the address map of the clock calendar. The memory consists of 14 general purpose RAM bytes, 10 bytes which contain the time, calendar, alarm data, and four control and status bytes. All 28 bytes are directly readable and writable by the processor program except Registers C and D which are read only. Bit 7 of Register A and the seconds byte are also read only. Bit 8 of the second byte always reads "Ø". The content of the four control and status registers are described in the Register Section.

TABLE 1

Clock Calendar Address Map

Description	Base Address Offset (Octal)
Seconds	Base +0
Seconds Alarm	Base +1
Minutes	Base +2
Minutes Alarm	Base +3
Hours	Base +4
Hours Alarm	Base +5
Day of the Week	Base +6
Date of the Month	Base +7
Month	Base +10
Year	Base +11
Register A	Base +12
Register B	Base +13
Register C	Base +14
Register D	Base +15
Next 14 Bytes are RAM	Base +16 through Base +33

TIME, CALENDAR & ALARM LOCATIONS

The program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these locations. The contents of the 10 time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the ten locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized, the time of day clock makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the 10 data bytes.

Table 2 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12 hour format is selected, the high-order bit of the hours byte represents PM when it is a "1".

TABLE 2

Time, Calendar & Alarm Data Modes

Function	Decimal Range	Range In Octal Binary Data Mode		Range in Hex BCD Data Mode
Seconds	0-59	0-73		0-59
Seconds Alarm	0-59	0-73		0-59
Minutes	0-59	0-73		0-59
Minutes Alarm	0-59	0-73		0-59
Hours (12 hour mode)	1-12	1-14	(AM)	0-12
		201-214	(PM)	80-92
Hours (24 hour mode)	0-23	0-27		0-23
Hours Alarm (12 hours)	1-12	1-14	(AM)	0-12
		201-214	(PM)	80-92
Hours Alarm (24 hours)	0-23	0-27		0-23
Day of the Week Sunday = 1	1-7	1-7		1-7
Day of the Month	1-31	1-37		1-31
Month	1-12	1-14		1-12
Year	0-99	0-143		0-99

The time, calendar, and alarm bytes are not always accessible by the processor program. Once per second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 1948 microseconds. The Update Cycle Section shows how to accommodate the update cycles in the software.

The three alarm bytes may be used in two ways. When the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is set. The alternate usage is to insert a "don't care" code in any octal byte from 300 to 377. That is, the two most significant bits of each byte, when set to "1", create a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

CLOCK CALENDAR RAM

The RAM bytes can be used by the processor program and are fully available during the update cycle.

When time and calendar information must use battery back-up, very frequently there is other non-volatile data that must be retained when power is removed. The 14 user RAM byte can serve this use for battery backed storage.

The number of RAM bytes is jumper selectable from two to eighteen. This corresponds to an I/O page requirement of 10 to 16 words including the clock calendar and the counter timer I/O page requirements.

INTERRUPTS

The clock calendar includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at a rate from once per second to once a day. The periodic interrupt may be selected for rates from half a second to 30.517 microseconds. The update-ended interrupt may be used to indicate to the program that an up-date cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a "1" to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "Ø" in the interrupt-enable bit prohibits the interrupt.

If an interrupt flag is already set when the interrupt becomes enabled, the request is generated though the event initiating the interrupt may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupt flags before enabling new interrupts.

When an interrupt event occurs, a flag bit is set to a "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The "interrupt" flag bit becomes a status bit which the software interrogates. When the software detects that a flag is set, it is an indication to software that the "interrupt" event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared when Register C is read. All bits which are high when read by the program are cleared and new interrupts (on any bit) are held until after the read cycle.

One, two, or three flag bits may be set. The program should inspect all utilized flag bits every time Register C is read to insure that no status is lost.

When an interrupt-flag bit is set and the corresponding interrupt-enable bit is also set, an interrupt is generated. The program can determine what initiated the interrupt by reading Register C. A "1" in Bit 7 of Register C (IRQF bit) indicates that one or more interrupts have been initiated. The act of reading Register C clears all the then-active flag bits plus the IRQF bit.

DIVIDER STAGES

The clock calendar has 22 binary-divider stages following the time base as shown in Table 3. The output of the dividers is a 1 Hz signal to the update-cycle logic. The dividers are controlled by three bits (DV2, DV1, and DVØ) in Register A.

DIVIDER CONTROL

The divider-control bits have three uses, as shown in Table 4. Three usable operating time bases may be selected (4.194304 MHz, 1.048576 MHz, or 32.768 kHz), however, only the 32.768 kHz is available. The divider chain may be held at reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one second later. Since the clock calendar uses a 32.768 kHz time base, bits DVØ and DV2 must be set to "Ø" and DV1 must be set to "1" for proper clock timing.

SQUARE WAVE OUTPUT SELECTION

Fifteen of the 22 divider taps are made available to a 1 of 15 selector as shown in Table 4. The first purpose of selecting a divider tap is to generate a square wave output signal available at connector J1 Pin 10. Four bits in Register A establish the square wave frequency as listed in Table 4. The square wave frequency selection shares the 1 of 15 selector with periodic interrupts.

Once the frequency is selected, the output of the square wave pin may be turned on and off under program control with the

square wave (SQWE) bit in Register B. Altering the divider, square wave output selection bits, or the square wave output-enable bit may generate an asymmetrical waveform at the time of execution. The square wave output pin has a number of potential uses. For example, it can serve as a frequency standard for external use, a frequency synthesizer, or could be used to generate one or more audio tones under program control.

PERIODIC INTERRUPT SELECTION

The periodic interrupt allows an interrupt to be generated from once every 500 ms to once every 122.07 microseconds. The periodic interrupt is separate from the alarm interrupt which may generate an interrupt from once per second to once per day.

Table 4 also shows that the periodic interrupt rate is selected with the same Register A bits which select the square wave frequency. Changing one also changes the other. But each function may be separately enabled so that a program could switch between the two features or use both. The square wave output is enabled by the SQWE bit. Similarly, the periodic interrupt is enabled by the PIE bit in Register B.

The Periodic interrupt is usable by practially all real-time systems. It can be used to scan for all forms of inputs from contact closures to serial receive bits or types. It can be used in multiplexing displays or with the counter timer to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

The clock calendar executes an update cycle once per second, assuming one of the proper time bases is in place, the divider is not clear, and the SET bit in Register B is clear. The SET bit in the "1" state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues and sets a flag if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

TABLE 3

Divider Configurations

Time-Base Frequency	Divider Bits Register A DV2	DV1	DVØ	Operation Mode	Divider Reset	Bypass First N-Divider Bits
4.194304 MHz	0	0	0	Yes	-	N = 0
1.048576 MHz	0	0	1	Yes	-	N = 2
32.768 kHz	0	1	0	Yes	-	N = 7
Any	1	1	0	No	Yes	-
Any	1	1	1	No	Yes	-

Note: Other combinations of divider bits are used for test purposes only.

TABLE 4

Periodic Interrupt Rate & Square Wave Output Frequency

Rate Select Control Register A RS3	RS2	RS1	RSØ	Periodic Interrupt Rate	SQW Output Frequency
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.281 µs	2.048 kHz
0	1	1	0	976.562 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

The update cycle takes 1984 microseconds. During the update cycle, the time, calendar, and alarm bytes are not accessible by the processor program. The clock calendar protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion off the bus during the entire update cycle. If the processor reads these locations before the update is complete, the output will be undefined. The update in progress (UIP) status bit is set during this interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Two methods of accommodating non-availability during updates are available by the program.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 998 ms are available to read valid time and date information. During this time a display could be updated or the information could be transferred to continuously available RAM. Before leaving the interrupt service routine, the IRQF bit should be cleared by reading Register C.

The second method uses the update-in-process bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once per second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes high, the update cycle begins 244 microseconds later. Therefore, if a low is read on the UIP bit, the user has at least 244 microseconds before the time/calendar data will be changed. If a "1" is read in the UIP bit, the time/calendar may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid clock calendar data to exceed 244 microseconds.

CLOCK CALENDAR CONTROL STATUS REGISTERS

REGISTER A

MSB LSB

b7	b6	b5	b4	b3	b2	b1	bØ
UIP	DV2	DV1	DVØ	RS3	RS2	RS1	RSØ

Read/Write Register except UIP

Figure 4

Register A

UIP

The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1", the update cycle is in progress or will soon begin. When UIP is a "Ø", the update cycle is not in progress and will not be for at least 244 microseconds. The time, calendar, and alarm information is fully available to the program when the UIP bit is zero -- it is not in transition. The UIP bit is a read only bit, and is not affected by reset. Writing the SET bit in Register B to a "1" inhibits the update cycle and clears the UIP status bit.

DV2, DV1, DVØ

These bits are used to permit the program to select various conditions of the 22 stage divider chain. The divider selection bits identify which of the three bases of 4.194304 MHz, 1.048576 MHz, and 32.768 kHz may be used. Because the clock calendar is only equipped with a 32.768 kHz time base, bits DV2 and DVØ must be set to "0" and DV1 must be set to "1" for proper clock operation. The divider selection bits are also used to reset the divider chain. When the clock calendar is first initialized, the program may start the divider at the precise time stored in the clock calendar registers. When the divider reset is removed, the first update cycle begins one second later. These three read/write bits are not affected by reset.

RS3, RS2, RS1, RSØ

The four rate selection bits select one of fifteen taps on the 22 stage divider, or disable the divider output. The tap selected may be used to select the square wave output frequency and/or a periodic interrupt rate. The program may do one of the following: 1) enable the interrupt with the PIE bit, 2) enable the SQW output with the SQWE bit, 3) enable both at the same time at the same rate, or 4) enable neither. Table 4 lists the periodic interrupt rates and the square wave output frequencies that may be chosen with the RS bits. These four bits are read/write bits which are not affected by reset.

REGISTER B

MSB							LSB	Read/Write Register
b7	b6	b5	b4	b3	b2	b1	bØ	
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	

Figure 5

Register B

SET

When the SET bit is a "0", the update cycle functions normally by advancing the clock once per second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not cleared by reset.

PIE

The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic interrupt flag (PF) bit to cause an interrupt. A program writes a "1" to the PIE bit in order to enable periodic interrupts at the rate specified by the RS3, RS2, RS1, and RSØ bits in control Register A. A zero in PIE disables the periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is cleared to "0" by a reset.

AIE

The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) to generate an interrupt. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate a request. The reset clears AIE to "0".

UIE

The UIE (update ended interrupt enable) bit is a read/write bit which enables the update end flag (UF) bit to generate an interrupt. A reset or the SET bit going high clears the UIE bit.

SQUARE WAVE ENABLE (SQWE)

When the square wave enable (SQWE) bit is set to a "1" by the program, a square wave signal at the frequency specified in the rate selection bits (RS3 to RSØ) appears on Pin 10 of J1. When the SQWE bit is set to a zero, the square wave output is held high. SQWE is cleared by a reset. SQWE is a read/write bit.

DATA MODE (DM)

The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is not modified by any internal functions or reset. A "1" in DM signifies binary data, while a "0" specified binary coded decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours bytes as either the 24 hour mode (a "1") or the 12 hour mode (a "Ø"). This is a read/write bit, which is affected only by the software.

DAYLIGHT SAVING ENABLE (DSE)

The daylight saving enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1"). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or reset.

REGISTER C

MSB LSB Read Only Register

b7	b6	b5	b4	b3	b2	b1	bØ
IRQF	PF	AF	UF	0	0	0	0

Figure 6

Register C

IRQF

The interrupt request flag (IRQF) is set to a "1" when one or more of the following are true:

PF = PIE = "1"

AF = AIE = "1"

UF = UIE = "1"

i.e., IRQF = PF · PIE + AF · AIE + UF · UIE

All flag bits are cleared after Register C is read or when a reset occurs. A program write to status Register B does not modify any of the flag bits.

PERIODIC INTERRUPT FLAG (PF)

The periodic interrupt flag (PF) is a read only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RSØ bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an interrupt request and sets the IRQF bit when PIE is also a "1". The PF bit is cleared by a software read of Register C.

ALARM INTERRUPT FLAG (AF)

A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF generates an interrupt and causes a "1" to appear in the IRQF bit when the AIE bit is a "1". A reset or a read of Register C clears AF.

UF

The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes an interrupt. UF is cleared by a Register C read or a reset.

B3 to BØ

The unused bits of Status Register 1 are read as "Ø's". They cannot be written.

REGISTER D

MSB LSB Read Only Register

b7	b6	b5	b4	b3	b2	b1	bØ
VRT	0	0	0	0	0	0	0

Figure 7

Register D

VRT

The vaid RAM and time (VRT) bit indicates the contents of the clock calendar and RAM has not undergone a power failure. A "Ø" appears in the VRT bit when a power failure has been detected. This power failure indicates that the batteries have fully discharged during a system power failure. The processor can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read only bit. The VRT bit can only be set by reading the D Register.

B6 to BØ

The remaining bits of Register D are unused. They always read zero.

INTERFACING

CONNECTOR DESCRIPTION

The 306 contains a 40 pin 3M connector as shown in Figure 8. Table 5 gives the names and functions of the I/O pins.

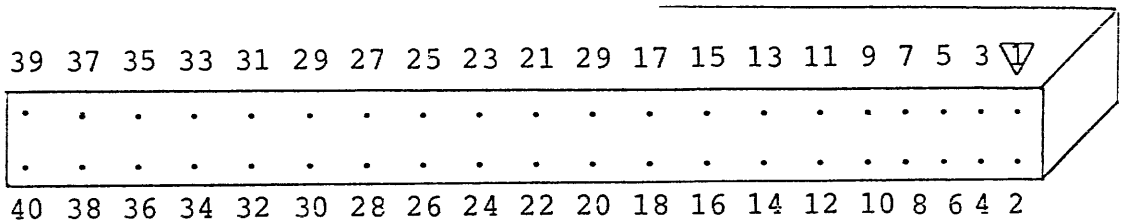


Figure 8

J1 Pin Numbering Diagram

TABLE 5

J1 Pin Out Description

Pin #	Name	Description
1	ST1 Input	
2	ST1 Output	500 nsec. neg. pulse which indicates an ST1 input signal
3	ST2 Input	
4	ST2 Output	500 nsec. neg. pulse which indicates an ST2 input signal
5	OVF OUT	500 nsec. pulse which indicates counter overflow
6,7,35	GROUND	
25	S1	Selects neg. slope for ST1 when grounded
27	S2	Selects neg. slope for ST2 when grounded
29	LV1	Level control input for ST1
31	LV2	Level control input for ST2
33	+3V	Pos. 3V reference used to externally set ST1 & ST2 levels
		All unused pins are not connected

SCHMITT TRIGGER INPUTS

The 306 contains two Schmitt Trigger inputs, ST1 and ST2. Each input can be configured to fire an internal one shot by either a negative or positive going signal at any voltage from -12 to +12 or at TTL levels. The level and polarity is controlled by jumper posts JP1 and pots ST1 ADJ and ST2 ADJ. Refer to Figure 3.

The ST1 input is used to provide a method of counting an external event or as a means of inputting a unique external clock. The output of the one shot which is triggered by the ST1 input is brought out to Pin 2 of J1 and the ST1 tab. The one shot output is also connected to an input of the one of eight multiplexer of the clock oscillator and divider logic.

The ST2 input is used to provide an external means of starting the counter timer operation according to the mode selected by the CSR. When bit 13 (ST2E) of the CSR is set, then any signal which will cause the ST2 input to trigger the internal ST2 one shot will cause the GO bit to become set and also set the ST2 Flag (bit 15 of the CSR). When triggered during Mode 2 and 3 operation, the instantaneous count of the counter will be latched by the Counter Buffer Register.

The output of the one shot which is triggered by the ST2 input is brought out to Pin 4 of J1.

The ST1 and ST2 one shot outputs are approximately 500 nsec. negative going TTL pulses.

ST1 & ST2 TRIGGER LEVEL ADJUSTMENT

Jumper posts JP1 and pots ST1 ADJ and ST2 ADJ are used to set the trigger voltage levels and polarity of the ST1 and ST2 inputs. These inputs may also be externally controlled through connector, J1.

To select an ST1 trigger voltage between -12 to +12 volts requires jumpering JP1 Pin 1 to JP1 Pin 2 and adjusting the ST1 ADJ pot. To trigger the ST1 input with TTL levels requires jumpering JP1 Pin 2 to JP1 Pin 3.

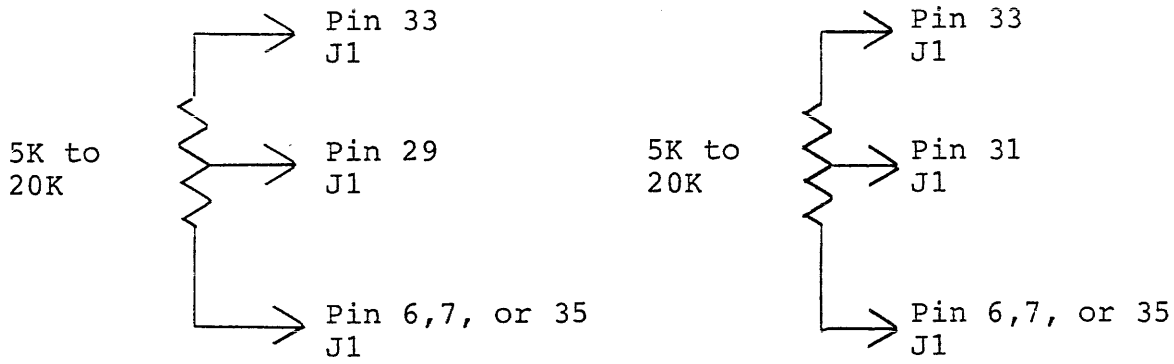
To set the ST2 trigger voltage between -12 and +12 volts requires jumpering Pin 4 of JP1 to Pin 5. To trigger the ST2 input with TTL levels requires jumpering JP1 Pin 5 to JP1, Pin 6.

To trigger the ST1 input on a positive going slope requires installing a jumper between JP1, Pin 7 and JP1, Pin 8. No jumper installed between these pins will cause a negative going slope to trigger this input.

JP1, Pin 9 and JP1, Pin 10 performs the same function for the ST2 input as Pins 7 and 8 does for the ST1 input.

When the level is to be set externally through J1, the SP1 level select jumper for that input must be set for -12 to +12 operation and the adjustment pot must be centered. Also, the slope control jumper must also be removed if the slope is to be externally selected.

To set the ST1 or ST2 levels externally requires attaching a pot(s) as shown below:



ST1 External Pot Connection

ST2 External Pot Connection

Figure 9

External Adjustment of ST1 or

ST2 Trigger Level

To externally select a positive going slope to trigger the ST1 input requires connecting Pin 25 of J1 to ground (Pins 6,7, or 35 of J1). No connection selects a negative going slope. For external slope selection of the ST2 input, Pin 27 of J1 is used.

SQUARE WAVE OUTPUT

When the clock calendar option is installed, Pin 10 of J1 contains the square wave output at the frequency selected by Register A of the clock calendar.

COUNTER OVERFLOW

When the counter of the counter timer overflows, a 500 nsec. negative going pulse is generated. This signal is brought out to Pin 5 of J1 and the OVF tab shown in Figure 3. This signal may be used to trigger an external event at equal time intervals or as a pulse train at a set frequency.