HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

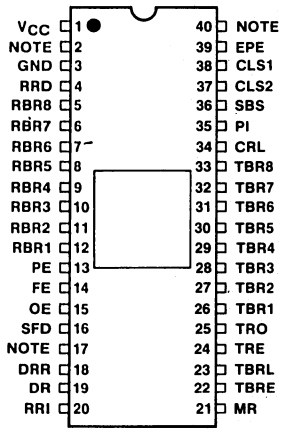
Preliminary

HD-6402/6403
HD-6402A/6403A
CMOS/LSI Universal Asynchronous Receiver (UART)

FEATURES

- OPERATION FROM D.C. TO 3.2MHz
- LOW POWER – TYP. 10mW @ 3.2MHz
- 4V–11V OPERATION
- PROGRAMMABLE WORD LENGTH, STOP BITS AND PARITY
- AUTOMATIC DATA FORMATTING AND STATUS GENERATION
- COMPATIBLE WITH INDUSTRY STANDARD UART's
- CRYSTAL OPERATION–HD-6403

CONNECTION DIAGRAM



NOTE:

PIN	HD-6402	HD-6403
2	N/C	CONTROL
17	RRC	OSC IN
40	TRC	OSC OUT

ORDERING INFORMATION

HD 1 - 6402 A - 2

- HD 1: HARRIS
- 6402: DEVICE NUMBER
- A: VERSION:
  - A: 10.0V Nominal
  - BLANK: 5.0V Nominal
- 2: TEMPERATURE:
  - 2: -55°C to +125°C
  - 9: -40°C to +85°C
- PACKAGE CODE

DESCRIPTION

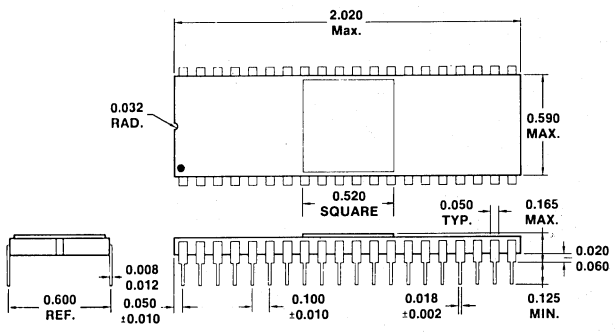
The HD-6402 and HD-6403 are CMOS/LSI subsystems for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

The HD-6402 and HD-6403 can be used in a wide range of applications including modems, printers, peripherals and remote data aquisition systems. CMOS/LSI technology permits operating clock frequencies up to 3.2 MHz (200K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

The HD-6402 differs from the HD-6403 on pins 2, 17, 19, 22, and 40 as shown in the connection diagram. The HD-6403 utilizes pin 2 as a control and pins 17 and 40 for an inexpensive crystal oscillator as shown on page 5. TBR Empty and DReady are always active. All other input and output functions of the HD-6402 and HD-6403 are as described.

PACKAGE

40 PIN D.I.P.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -.05V to V_{CC} +0.5V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HD-6402A-9/6403A-9	-40°C to +85°C
Military HD-6402A-2/6403A-2	-55°C to +125°C

D.C. ELECTRICAL CHARACTERISTICS V_{CC} = 4V to 11V, T_A = Industrial or Military

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Logical "1" Input Voltage	V_{IH}	70% V_{CC}			V	
Logical "0" Input Voltage	V_{IL}			20% V_{CC}	V	
Input Leakage	I_{IL}	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
Logical "1" Output Voltage	V_{OH}	V_{CC} -0.01			V	$I_{OUT} = 0$
Logical "0" Output Voltage	V_{OL}			GND +0.01	V	$I_{OUT} = 0$
Output Leakage	I_O	-1.0		1.0	μA	$0V \; V_O \; V_{CC}$
Supply Current HD-6402A/03A	I_{CC}		5.0	500	μA	$V_{IN} = V_{CC}$
Input Capacitance	C_{IN}		7.0	8.0	pF	
Output Clearance	C_O		6.0	10.0	pF	

A.C. ELECTRICAL CHARACTERISTICS V_{CC} = 10.0V, C_L = 50pF, T_A = 25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Frequency	f_{clock}	D.C.		6.4	MHz	
Pulse Widths CRL, DRR, TBRL	t_{pw}		100		ns	
Pulse Width MR	t_{pw}		250		ns	See Switching Time
Input Data Setup Time	t_{SET}		50		ns	Waveforms 1, 2, 3
Input Data Hold Time	t_{HOLD}		50		ns	
Output Propagation Delays	t_{pd}		100		ns	

SWITCHING WAVEFORMS

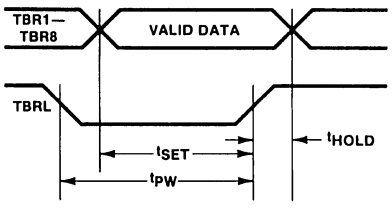


Figure 1.
DATA INPUT CYCLE

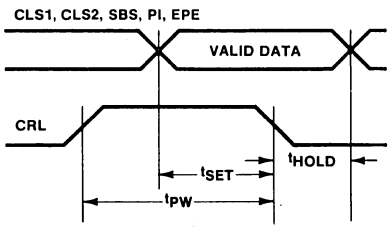


Figure 2.
CONTROL REGISTER LOAD CYCLE

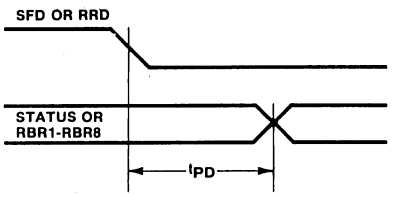


Figure 3.
STATUS FLAG OUTPUT DELAYS
OR DATA OUTPUT DELAYS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6402-9/6403-9	-40°C to +85°C
Military HD-6402-2/6403-2	-55°C to +125°C

D.C. ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%. T_A = Operating Temperature Range.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Logical "1" Input Voltage	V_{IH}	V_{CC} -2.0			V	
Logical "0" Input Voltage	V_{IL}			0.8	V	
Input Leakage	I_{IL}	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
Logical "1" Output Voltage	$V_{OH}2$	V_{CC} -0.01			V	I_{OUT} = 0
Logical "1" Output Voltage	$V_{OH}1$	2.4			V	I_{OH} = -0.2mA
Logical "0" Output Voltage	$V_{OL}2$			GND +0.01	V	I_{OUT} = 0
Logical "0" Output Voltage	$V_{OL}1$			0.45	V	I_{OL} = 2.0mA
Output Leakage	I_O	-1.0		1.0	μA	$0V \leq V_O \leq V_{CC}$
Supply Current	I_{CC}		1.0	100	μA	V_{IN} = GND or V_{CC}; Output Open
Input Capacitance	C_{IN}		7.0	8.0		
Output Capacitance	C_O		8.0	10.0	pF	

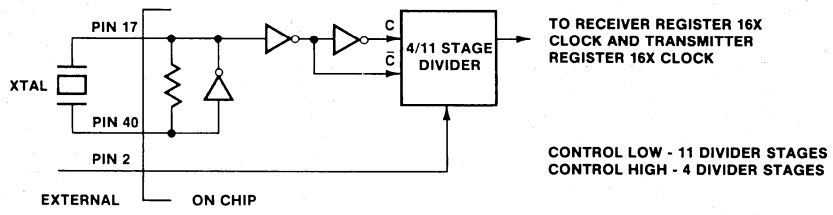
A.C. ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, T_A = 25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Frequency	f_{clock}	D.C.		3.2	MHz	
Pulse Widths CRL, DRR, TBRL	t_{pw}		200		ns	
Pulse Width MR	t_{pw}		500		ns	See Switching Time
Input Data Setup Time	t_{SET}		100		ns	Waveforms 1, 2, 3
Input Data Hold Time	t_{HOLD}		100		ns	
Output Propagation Delays	t_{pd}		200		ns	

HD-6403 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER WITH ON CHIP 4/11 STAGE DIVIDER

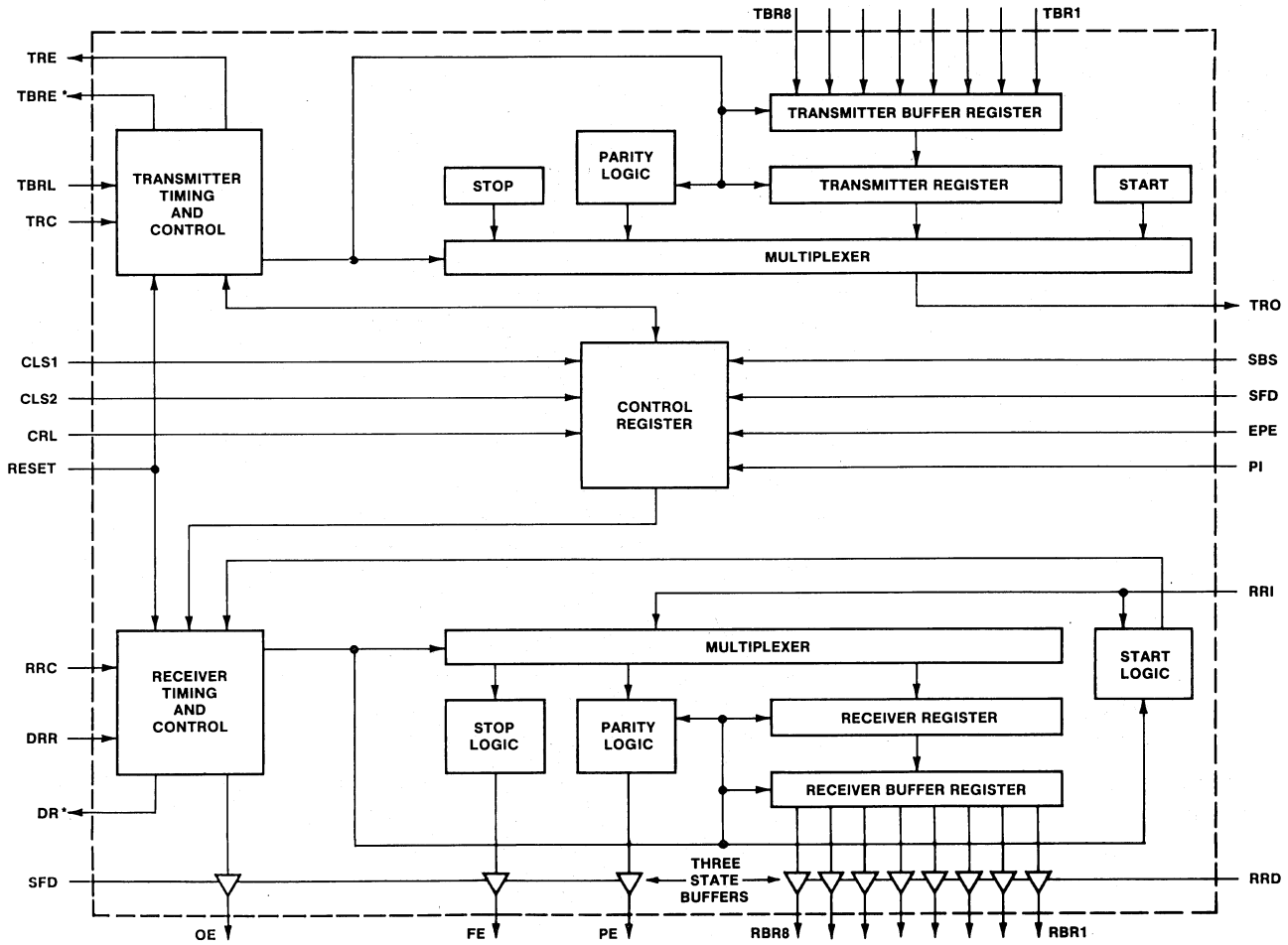
The HD-6403 differs from the HD-6402 on three inputs, TRC, RRC, and pin 2, and two outputs TBRE and DR. Outputs DR and TBRE are not three-state, but are always active.



The divider chain output acts as a 16X clock to both the receiver register and transimitter register. Consequently both receiver and transmitter operate at the same frequency. The TRClock and RRClock inputs are used for a crystal oscillator while pin 2 controls the number of divider stages.

The on chip divider and oscillator allow an inexpensive crystal to be used as a timing source rather than additional circuitry such as baud rate generators. For example, a color TV crystal at 3.579545MHz results in a baud rate of 109.2Hz for an easy teletype interface.

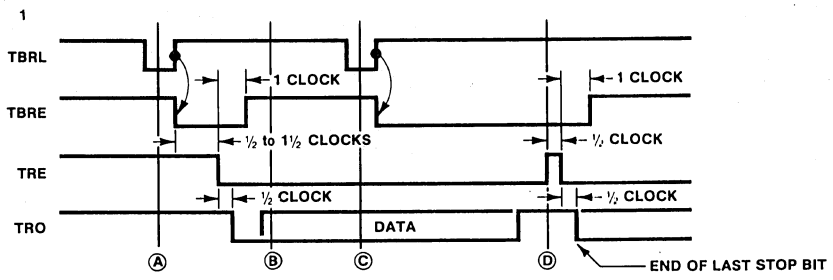
FUNCTIONAL BLOCK DIAGRAM



* Those outputs are three state (HD-6402) or always active (HD-6403).

TRANSMITTER OPERATION

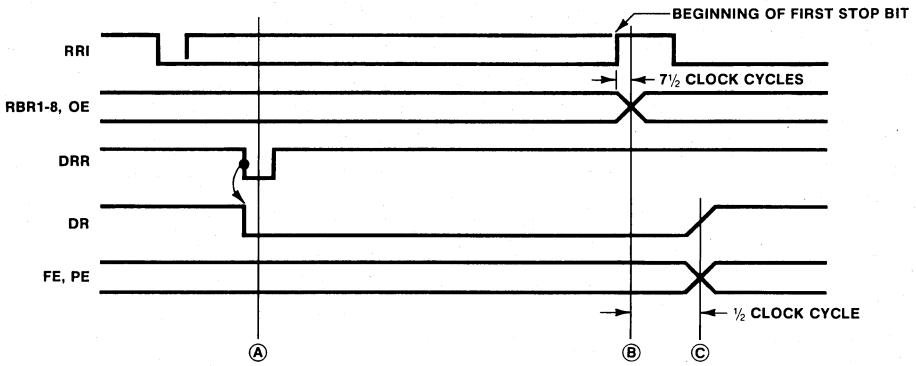
The transmitter section accepts parallel data, formats it and transmits it in serial form on the TROutput terminal. (A) Data is loaded into the transmitter buffer register from the inputs TR1 through TR8 by a logic low on the TBRLoad input. Valid data must be present at least t_{SET} prior to and t_{HOLD} following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TR1. (B) The rising edge of TBRL clears TBREmpty. ½ to 1½ clock cycles later data is transferred to the transmitter register and TREmpty in cleared. ½ cycle later transmission starts. Output data is clocked by TRClock. The clock rate is 16 times the data rate. ½ clock cycle later TBREmpty is reset to a logic high. (C) A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. (D) Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.



TRANSMITTER TIMING (NOT TO SCALE)

RECEIVER OPERATION

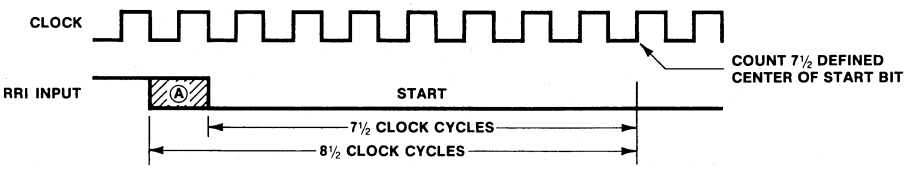
Data is received in serial form at the RInput. When no data is being received, RInput must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. (A) A low level on DRReset clears the DReady line. (B) During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transferred to the RBRegister. (C) ½ clock cycle later DReady is reset to a logic high, PError and FError are evaluated. A logic high on FError indicates an invalid stop bit was received, a framing error. A logic high on PError indicates a parity error.



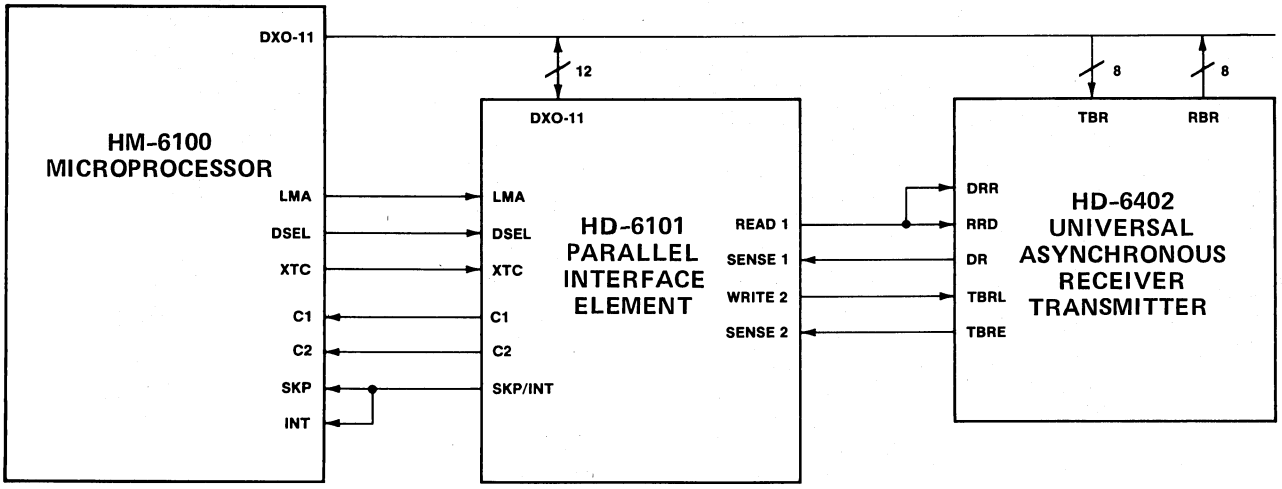
RECEIVER TIMING (NOT TO SCALE)

START BIT DETECTION

The receiver uses a 16X clock for timing. (A) The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symetrical square wave, the center of the start bit will be located within ±½ clock cycle, ±1/32 bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.



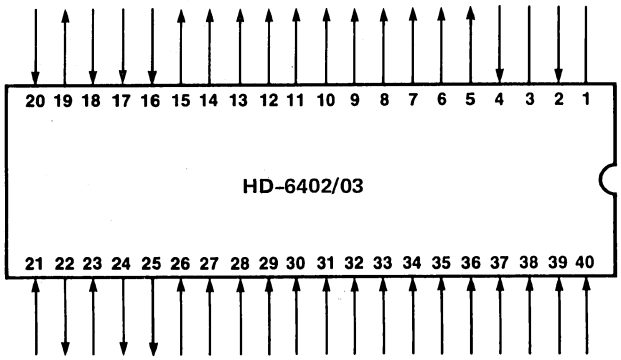
INTERFACING WITH THE HM-6100 MICROPROCESSOR



PIN ASSIGNMENT AND FUNCTIONS

PIN	SYMBOL	DESCRIPTION
1	VCC	+5 Volts Supply
2	HD-6402-N/C HD-6403-Control	No Connection 4/11 Stage Divider High: 4 Stage Low: 11 Stage
3	GND	Ground
4	RRD	A High level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 - RBR8
7	RBR6	See Pin 5 - RBR8
8	RBR5	See Pin 5 - RBR8
9	RBR4	See Pin 5 - RBR8
10	RBR3	See Pin 5 - RBR8
11	RBR2	See Pin 5 - RBR8
12	RBR1	See Pin 5 - RBR8

PIN	SYMBOL	DESCRIPTION
13	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register.
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	HD-6402-RRC HD-6403-OSCIN	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	DRR	A low level on DATA RECEIVED RESET clears the data received outputDR, to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.



PIN	SYMBOL	DESCRIPTION
21	MR	A high level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter output to a high level.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE 6	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1-TBR8	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.

PIN	SYMBOL	DESCRIPTION
27	TBR2	See Pin 26 - TBR1
28	TBR3	See Pin 26 - TBR1
29	TBR4	See Pin 26 - TBR1
30	TBR5	See Pin 26 - TBR1
31	TBR6	See Pin 26 - TBR1
32	TBR7	See Pin 26 - TBR1
33	TBR8	See Pin 26 - TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
37	CLS2	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits)
38	CLS1	See Pin 37 - CLS2
39	EPE	When PI is low a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	HD-6402-TRC HD-6403-OSCOUT	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.