DATAmatic 1000

Electronic Data Processing System

Preliminary
Manual of Information

DATAmatic Corporation
151 Needham Street
Newton Highlands 61, Massachusetts

March 31, 1956

DATAmatic 1000

Performance Specifications

INPUT: Punched cards

INPUT RATE: 900 punched cards per minute

INTERNAL CODE: Binary coded decimal and alphanumeric

STORAGE: 2700-ft. reels of 3-inch wide magnetic tape

MAGNETIC TAPE CAPACITY: 37,200,000 decimal digits per reel, up to 100 reels can be directly connected.

MAGNETIC READ-WRITE RATE: 60,000 decimal digits per second

INDEPENDENT OPERATIONS: Input conversion, output conversion, and processing may take place concurrently

TRANSFER STORAGE: Two input, two output buffers

BUFFER CAPACITY: 744 decimal digits per buffer

INTERNAL MEMORY: Magnetic cores

MEMORY CAPACITY: 24,000 decimal digits

MEMORY ACCESS TIME: Parallel access to 12 decimal digits in 10 microseconds

MULTI-TAPE SEARCH: Scans up to 10 magnetic tapes simultaneously

SEARCH RATE: Up to 600,000 decimal digits per second

COMPARISON RATE: 5000 alphabetic or numeric comparisons per second

ADDITION RATE: 4000 sets 11-digit (plus sign) numbers per second

MULTIPLICATION RATE: 1000 sets 11-digit (plus sign) numbers per second

OUTPUT FORMAT: Exceptional flexibility via plugboards

OUTPUT RATE — PUNCHED CARDS: 100 per minute

OUTPUT RATE — LOW SPEED PRINTER: 150 120-character lines per minute maximum

OUTPUT RATE — HIGH SPEED PRINTER: 900 120-character lines per minute maximum

ORDER STRUCTURE: Three address

DATAmatic
CORPORATION
151 NEEDHAM STREET • NEWTON HIGHLANDS 61, MASS.

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DATAmatic 1000

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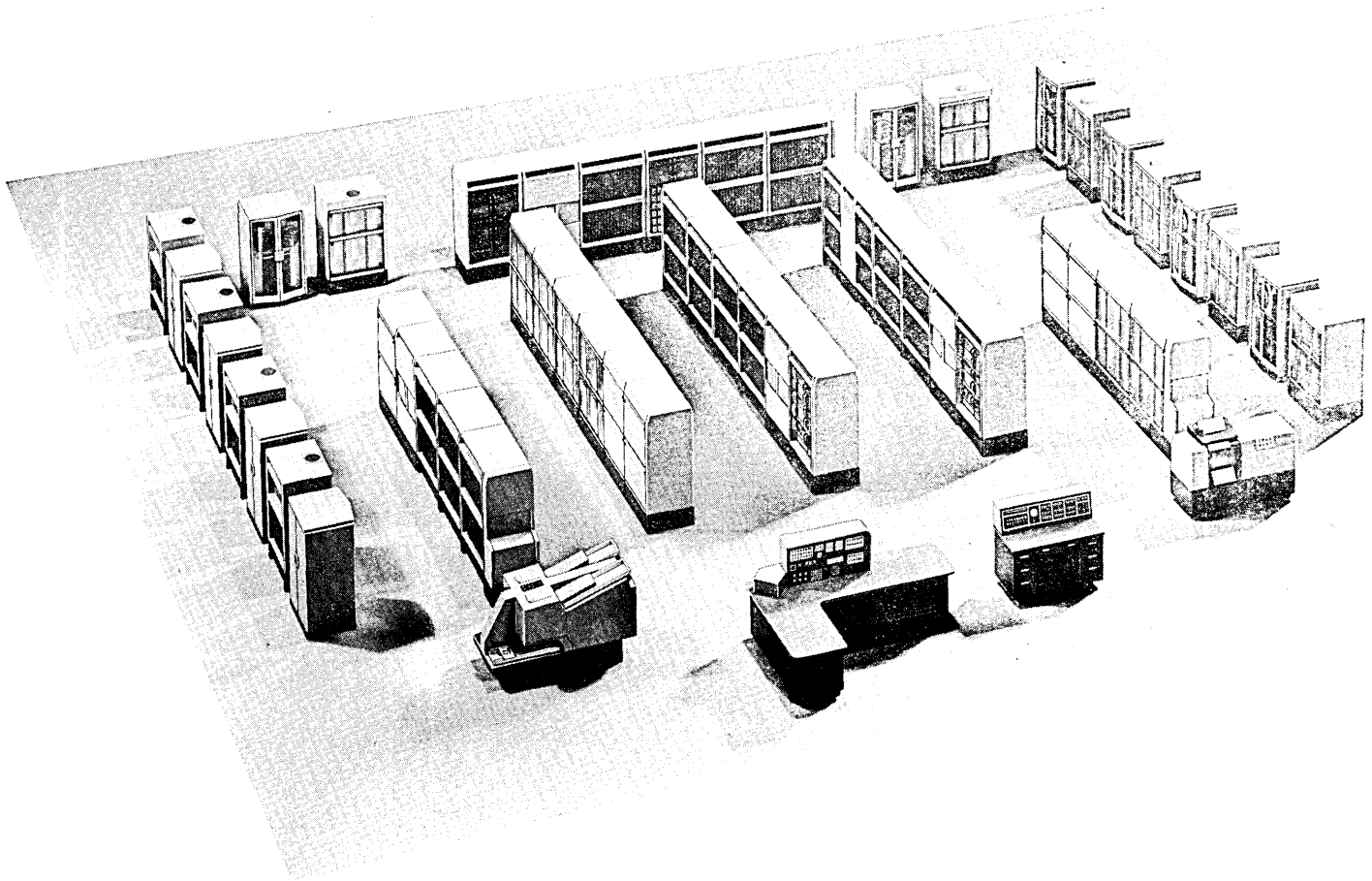


DATAmatic 1000 Electronic Data Processing System

The DATAmatic 1000

Electronic Data Processing System

INTRODUCTION

The DATAmatic 1000 is an electronic data processing system designed and engineered as an efficient management tool. It incorporates entirely new concepts and procedures for handling business data, conceived to exploit the accuracy, speed and versatility available in the latest DATAmatic equipment.

The DATAmatic 1000 system consists of a group of electronic units which are used as building blocks to produce a data processing system of any desired capacity. A typical installation contains the following elements:

Central Processor (Type 1000)
Central Console (Type 1090)
Magnetic File Unit (Type 1100)
Input Converter (Type 1200)
Output Converter (Type 1300)
File Reference Unit (Type 1150)
File Console (Type 1190)

Among the features of the DATAmatic 1000 are:

1. Separate input and output converters, each operating independently of the main machine.
2. 3 inch wide magnetic tape with magnetic material sandwiched between layers of tough plastic to make it practically unbreakable and impervious to handling.
3. Advanced frequency modulation principles used in recording information on the tape.
4. Magnetic core internal memory provides compact, low-power, high reliability storage.
5. Intermediate or buffer storage permits extremely fast File Maintenance by scanning up to 10 different Magnetic File Units simultaneously.
6. Comprehensive built-in checking systems guarantees unequaled performance in reliability and accuracy.

7. Extremely versatile system of orders permits ease of programming and greatly increases scope of applications.

8. Sorting can be accomplished with both input and output Magnetic File Units running at full speed reading and writing 60,000 decimal digits per second while the main machine is simultaneously sorting the items as they come and sending sorted items to the output, all of this completely self-checked.

9. Up to 100 Magnetic File Units can be connected into the system at any one time and can be split up in any way between the reading and recording operations.

INPUT-OUTPUT

In order to permit the main DATAmatic 1000 System to process data at its inherent electronic speeds, the conversion of original information onto magnetic tape for processing and also the printing or punching of output information from magnetic tape are carried on in input and output converters completely separate from the main machine.

The Input Converter incorporates as part of its own system a pluggable control panel that allows complete flexibility of format. Freedom of card format is obtained by column switching, duplication or deletion when reading the punched card. Numeric, alphabetic, multiple column punchings, symbolic punching can be handled with equal facility.

The Output Converter translates the information from the wide magnetic tape to either a 120 character line printer or an 80 column punched card. It also is a unit separate from the central processor and includes a pluggable control panel to edit information from the tape to a desired card or printed form format.

The Input Converter and the Output Converter both incorporate the comprehensive self-checking features available in the DATAmatic 1000. The most advanced and proven techniques using "magnetic core logic" have been applied in the design of these converters. These techniques employ magnetic cores to perform functions previously performed by electronic tubes, thereby increasing reliability by reducing the tube count and the cooling requirements.

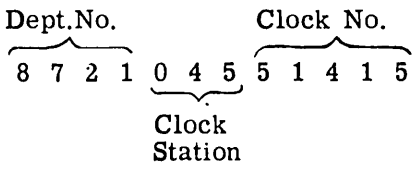
INFORMATION STORAGE

Machine Word

For more efficient machine operation, numeric characters and alphabetic characters and mixtures of these are handled in groups inside the machine. Since each of these various groups of characters occupies the same amount of space in the machine it is convenient to refer to them by a term which is applicable to all of them. Word is the commonly used term. Thus, by a 2000 word memory is meant a memory with 2000 storage locations or "pigeon holes", each of which can store one word consisting of a

group of numeric, alphabetic or mixed characters. The difference between these words is automatically interpreted by the machine.

Numeric words are groups of 12 decimal digits. An example of a numeric word is the identification of an individual by clock number, department number and clock station, using fields in a word in a manner similar to a punched card field.

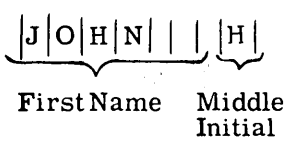


However, if numeric words are to be used in arithmetic operation they must have a plus or minus sign in the extreme left position. For example, if this week's gross pay is to be added to the gross pay to date, both numeric words would have a sign.

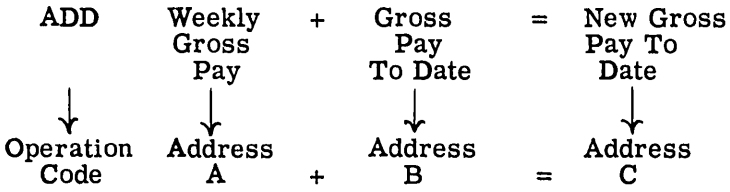
	12 Decimal Characters
Gross Pay	+|0|0|0|0|0|0|7|4.|8|3
Gross Pay to Date	+|0|0|0|0|0|3|4|7|1.|9|1
New Gross Pay to Date	+|0|0|0|0|0|3|5|4|6.|7|4

Alphabetic words are made up of 8 letters, in contrast to the 12 digits of a numeric word. This is necessary because it requires more space to identify any one of 26 letters than to identify one of 10 numbers. An example of the use of alphabetic words would be the name of an employee.

Example: John H Smith

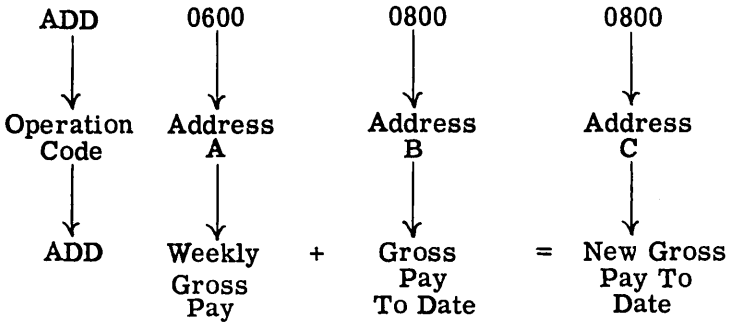


Order words are the instructions available to the programmer to guide the machine through a routine. The example shown under the numeric word description is the addition of weekly gross pay to gross pay to date to obtain a new gross pay to date. The 3 address order system used in the DATAmatic 1000 easily allows you to make this statement directly into a machine order.



Here the first 3 letters indicate the operation (ADD), the next 4 digits specify the address (Address A) or location in the 2000 word memory containing the Weekly Gross Pay, the next 4 digits (Address B) specify the address of the Gross Pay to Date and the last 4 digits (Address C) specify the location where the result of the addition (New Gross Pay to Date) shall be stored.

If the Weekly Gross Pay is located in memory address 600 and the Gross Pay to Date is located in memory address 800, the order appears in the following manner:



If the assignment of memory addresses had been 1643 and 1829 respectively the order would appear as:

ADD	1643	1829	1829

The coding of characters and operations within the machine need not concern the operator or programmer during normal operation.

Magnetic Tape External Storage

The 3 inch wide magnetic tape is one of the advancements available in the DATAmatic 1000 system. A single reel of tape can store up to 37,200,000 decimal digits (465,000 fully punched 80 column cards) and moves at the rate of 100 inches per second. This tremendous capacity and speed permits 60,000 decimal digits each second to be delivered to the central processing system for sorting, collating or other purposes. A single tape, when used as file storage, can store many years of historic files that require reference. Figure 1 shows how the magnetic oxide coating of the tape is sand-

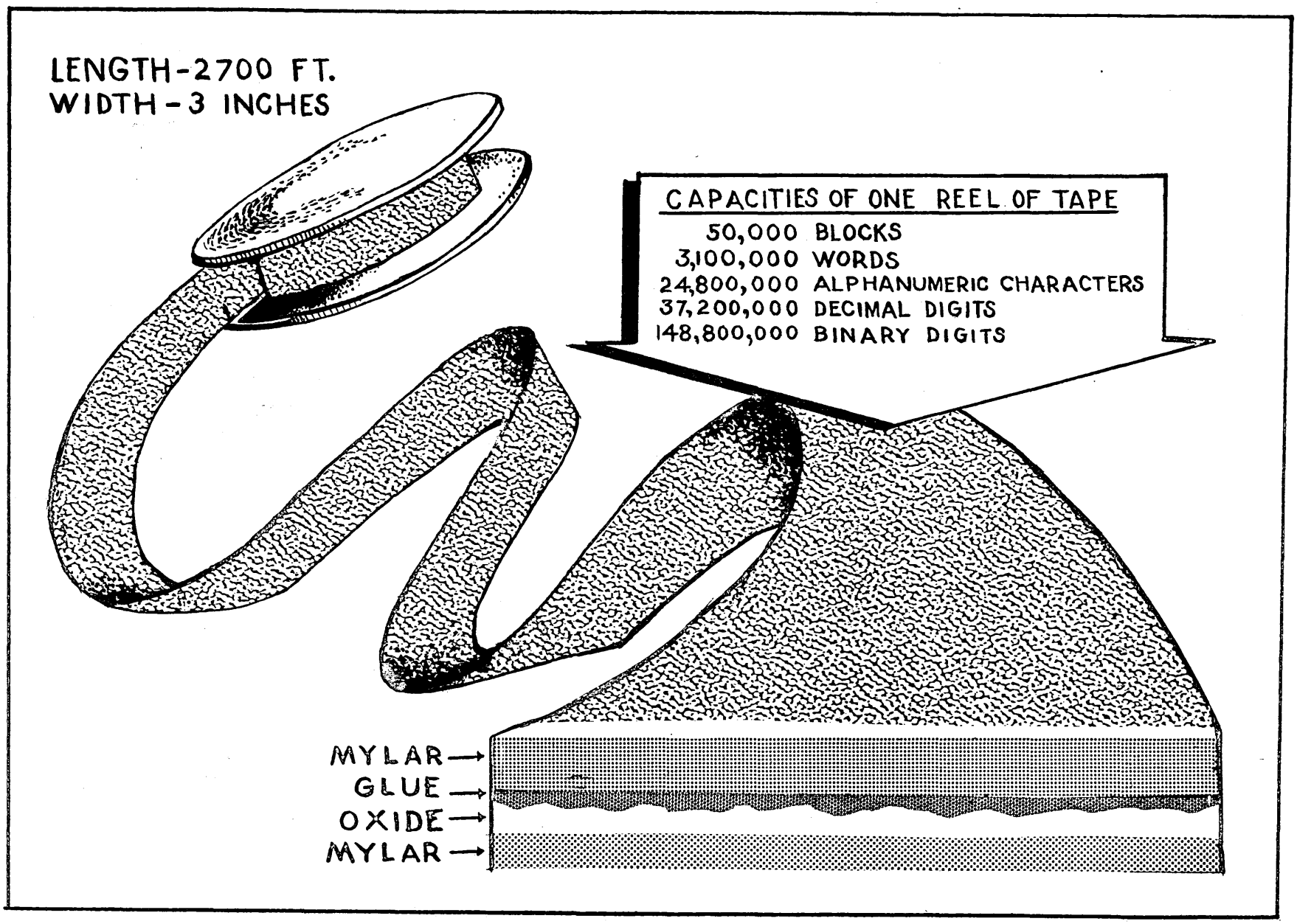


Figure 1. DATAmatic 1000 Magnetic Tape.

wiched between plastic layers that completely protect the recorded information and make the tape extremely durable.

The manner of recording information on the 3 inch wide magnetic tape has kept pace with the many other advancements available in the Magnetic File Unit and the tape itself. The DATAmatic 1000, to make more efficient use of the tape, records information along the tape in groups of 62 words each, called blocks. As shown in Figure 2, there are 31 levels across the tape and 2 words are recorded along the tape in each level when a block is recorded. In this fashion, 50,000 blocks of information are recorded on each tape.

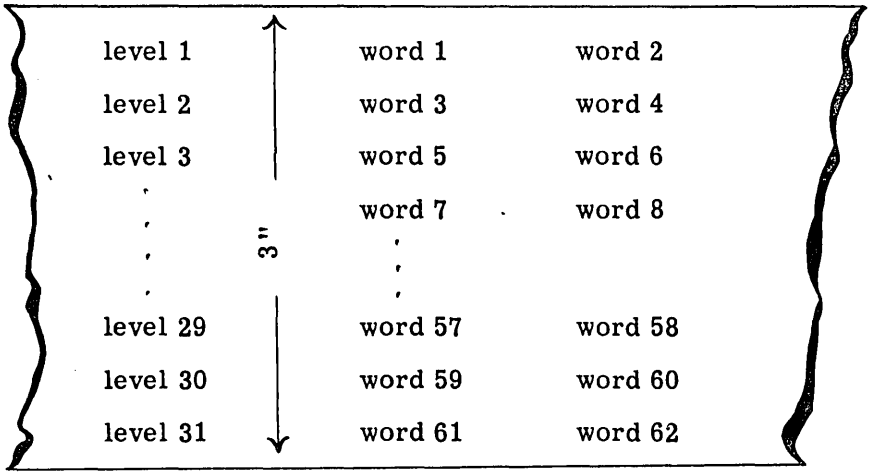


Figure 2. Arrangement of Words on Magnetic Tape.

The Magnetic File Unit will traverse a single active block, including starting and stopping, in less than 18 milliseconds. When running continuously, 80 active blocks per second can be read either in the direction of recording or in the opposite direction.

Another advancement in the DATAmatic 1000 is the technique of recording the blocks themselves on tape. An interlace system is used to minimize the blank or dead spaces between the blocks. The dead spaces are normally necessary to permit the tape to accelerate and decelerate. This interlace is accomplished by recording on every other block while the tape is moving in one direction and upon reaching the physical end of the tape, returning and filling in the unrecorded blocks. Figure 3 shows this technique with arrows indicating the direction of tape motion.

Obviously, a further advantage of the interlace system is that, when a tape has been completely read or recorded, no rewinding is necessary because the tape is already back at its physical beginning.

To further improve the reliability of the magnetic tape storage, the principles of frequency modulation have been applied to the recording technique. Variations in signal amplitude now have no effect on the recorded information, thus increasing the quality of

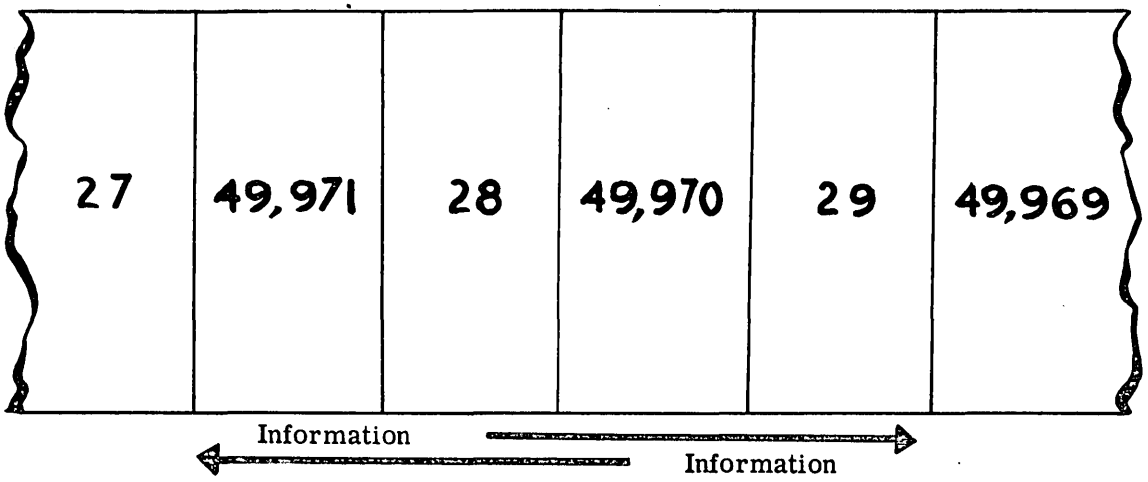


Figure 3. Interlacing of Blocks on DATAmatic 1000 Tape.

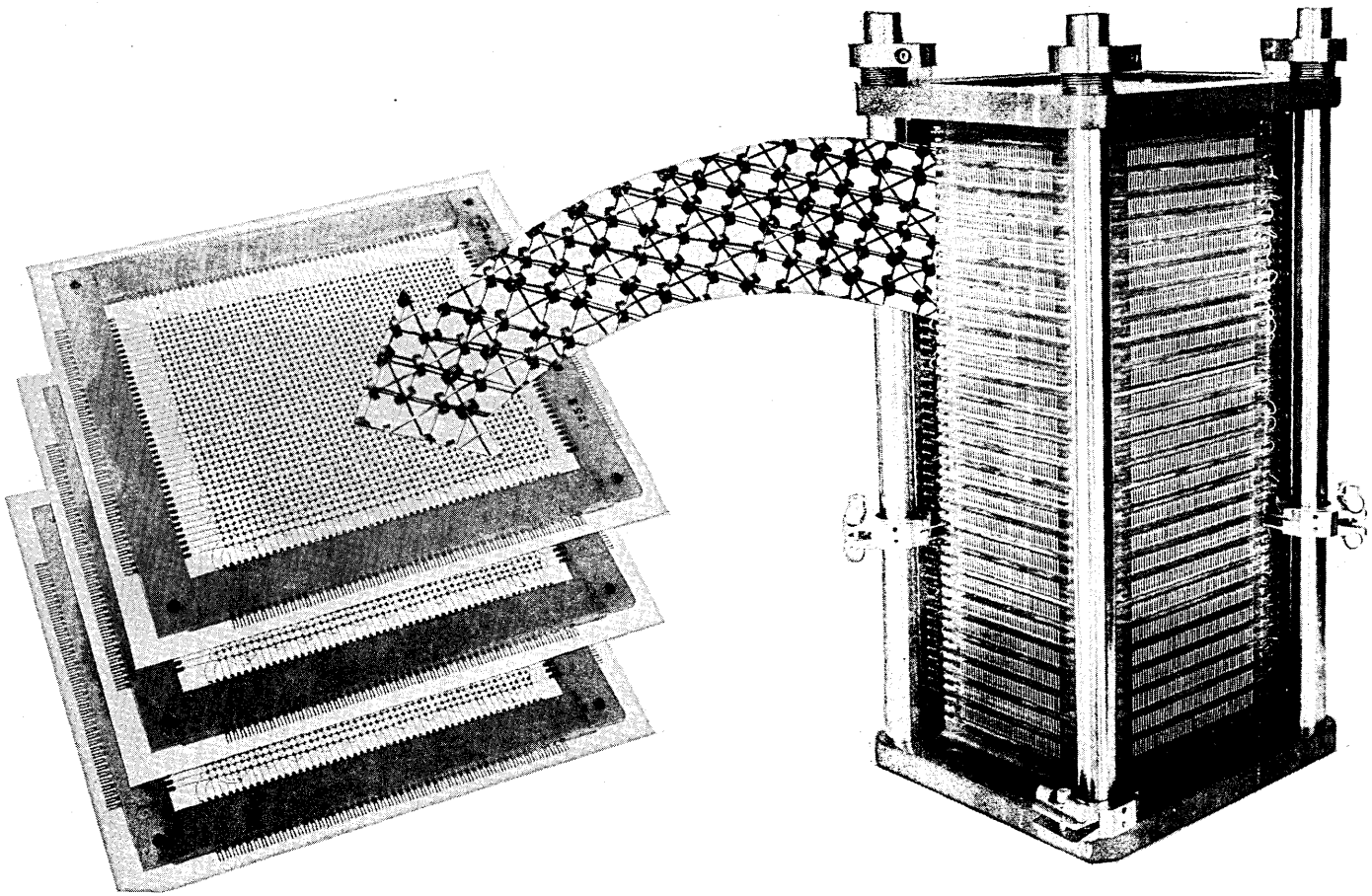
the system in a manner similar to the well known improvement of frequency modulation over Standard Broadcast radio.

The recording techniques described are all completely automatic and therefore do not concern the programmer.

Magnetic Core Internal Storage

The ferrite magnetic cores used in the DATAmatic 1000 provide a high speed memory which is reliable, simple and compact. These cores, tiny doughnut-shaped rings, are strung together on fine wires as shown in Figure 4a.

A core can be magnetized in either of two opposite orientations. To distinguish them, one may speak of the "1" state and the "0" state. Thus, current passing through a core in one direction magnetizes the core in the "1" state as shown in Figure 5a, while current passing through the core in the opposite direction magnetizes the core in the "0" state. Using two wires for this purpose, as in Figure 5b, allows a group of cores to be arranged on common wires in a plane as in Figure 4a, since any desired core in the plane can be magnetized in the "1" or the "0" state by passing current through an appropriate pair of horizontal and vertical wires.



(a) (b)

Figure 4. DATAmatic 1000 Magnetic Core Memory.

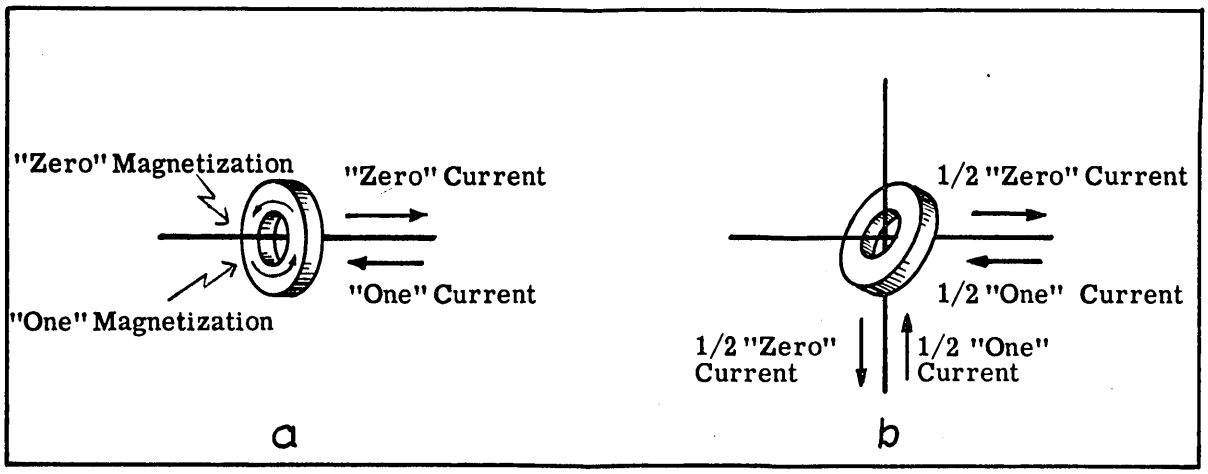


Figure 5. Typical Magnetic Core.

A single core plane contains 2,000 cores and thus can store, for example, the first pulse of each of the 2000 possible words to be stored in the memory. By stacking 52 of these planes together as in Figure 4b, 52 cores can be selected simultaneously (one in each plane) and thus a single machine word (numeric, alphabetic or order) is stored.

The total of 104,000 cores store the equivalent of 24,000 decimal digits or 16,000 alphabetic characters. Information is obtained from any one of the 2000 addresses, 12 decimal digits at a time, in approximately ten millionths of a second.

Certain addresses in the group 1983 to 1999 are of special interest. Those from 1983 to 1989 are usually reserved for control purposes and may be selected automatically as order sources under certain circumstances. Addresses from 1990 to 1999 are located in the Arithmetic and Control Units and contain special words used for control purposes. They can be read into and out of by orders.

Intermediate Storage Units

The need of management to handle large amounts of data is not filled by electronic processing speed alone. Many procedures are limited by the rate at which information stored on magnetic tape can be made available to the electronic high speed processing of the central machine.

The Input and Output Intermediate Storage Units of the DATAmatic 1000 are the devices that permit information to be transferred between the tape and the Central Processor at a constant rate. This rate of delivery of information may be maintained while the Magnetic File Unit is scanning the tape, at the rate of 80 blocks per second.

Complete flexibility is maintained when transferring between the Intermediate Storage Units and the magnetic core memory, both in the number of words being transferred and in the location in the memory where the information is stored.

The scope of application is greatly increased by the ability of the Input Intermediate Storage Unit to receive information simultaneously from 10 different Magnetic File Units. This feature makes it possible to search, simultaneously, on 10 Magnetic File Units.

The Input Intermediate Storage Unit consists of two high speed storage sections each being capable of handling 62 words. Each section may be controlled independently or both may be coordinated to act as a single unit. Figure 6 shows in two diagrams the ability of this unit to accept one block of information from tape while transferring other information to the core memory for processing.

The Output Intermediate Storage Unit also consists of two high speed storage sections each capable of handling 62 words. Figure 7 shows how one block of information can be written onto magnetic tape while another block is being accumulated for later writing.

PROGRAMMING AND OPERATION

Many steps are followed prior to running a procedure on a machine. The procedure is first analyzed and broken down to the operations that can be performed by the DATAmatic 1000. Usually these procedures are set down in a detail flow chart. The instructions or orders that fulfill the purpose of the flow chart are then recorded on paper. For example, the procedure flow chart might indicate "Compute Gross Pay". Three instructions are necessary to accomplish this, assuming the source data (the time card) has been converted to magnetic tape. First read the information (employee identification, hours worked, rate of pay) from tape to the intermediate storage unit -- a read tape order. Second transfer information from the intermediate storage to the memory - - a transfer order. Third multiply hours worked times rate of pay - - - a multiply order. The setting down of the read order, the transfer order and the multiply order in sequence and in the form that can be interpreted by the machine is called programming. The complete sequence of instructions necessary to carry out a desired procedure are written down in this fashion and then recorded on the magnetic tape. Once this has been read into the high speed core memory the operator needs merely to manually insert a tape read order and a Transfer In order and depress the start button. The DATAmatic 1000 system will perform these instructions, and then proceed automatically to carry out each of the other instructions in sequence.

Each order, in turn, is selected from the high speed memory location whose address is contained in the Sequence Register. Unity is automatically added to the contents of the Sequence Register immediately following the selection.

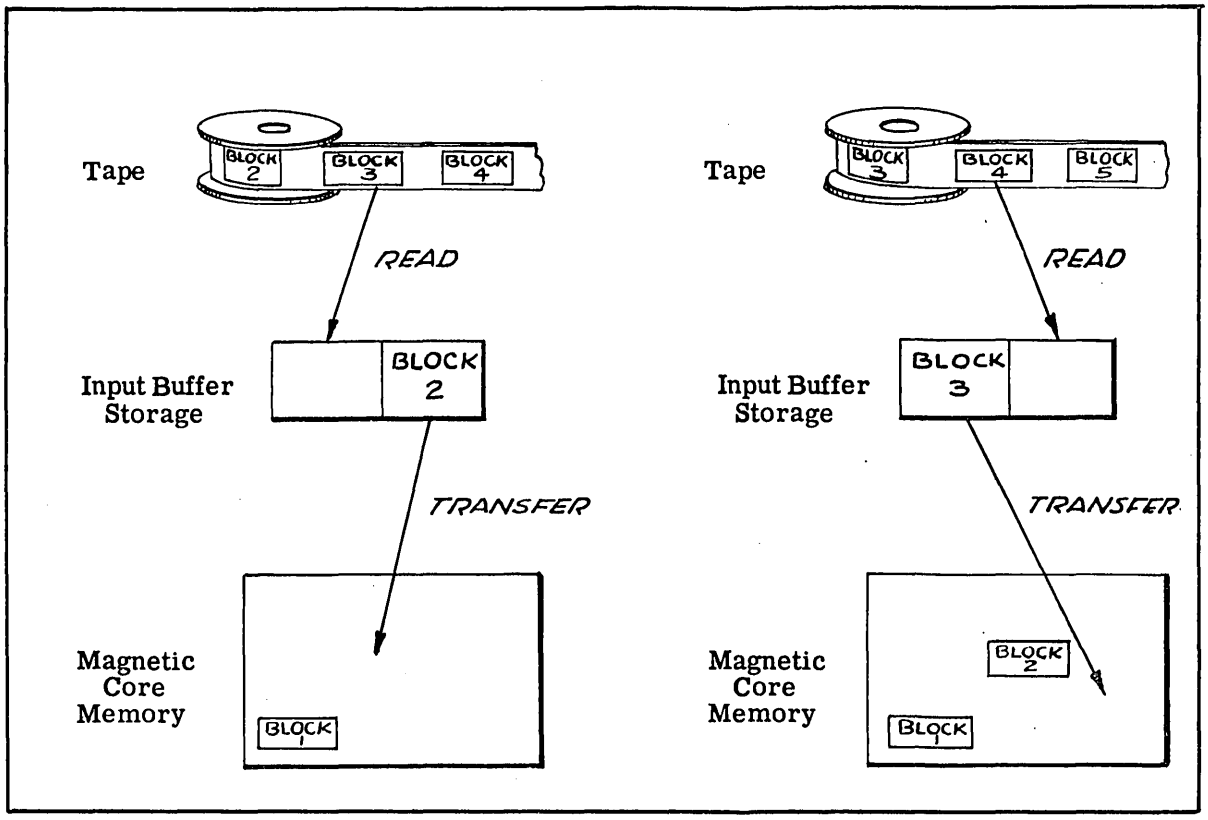


Figure 6. Input Buffer Storage.

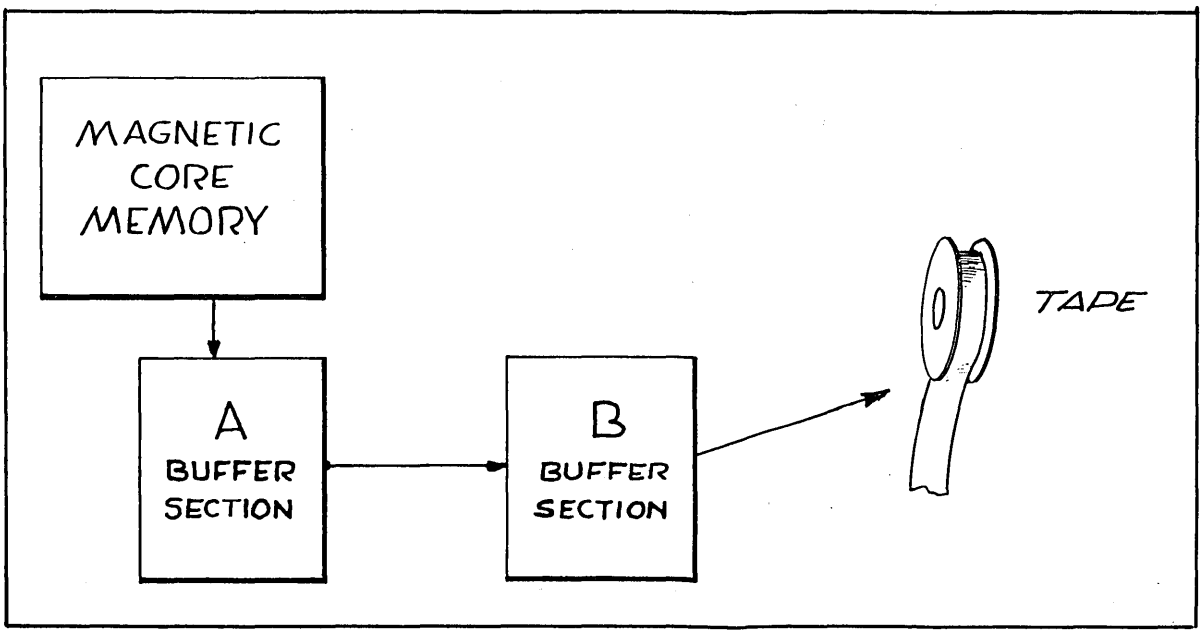


Figure 7. Output Buffer Storage.

To provide flexibility of control, some orders have the ability to change the contents of the Sequence Register and thus change the sequence of operations. When this occurs, the Sequence Register is changed to the address indicated by the order being processed. After completion of such an order the next order is obtained from the new setting of the Sequence Register. The tape orders and control orders have this ability to change the Sequence Register.

Also available to the programmer is the ability to "subsequence" or step out of the normal sequence of orders to perform some extra order and then return to the normal sequence.

A further ability available in the DATAmatic 1000 is its ability to modify its own orders or to compose new orders, based on decisions which it makes in processing a set of information. This is possible since, as pointed out earlier, an instruction "word" looks just like a numeric or alphabetic word. Therefore the machine can choose to look on an instruction as a numeric word and modify it by an arithmetic operation.

An additional feature of the DATAmatic 1000 is that the programmer can easily tag any order as a sentinel order which will tell the computer that it has now reached a particular place in the program where special action should be taken. This powerful feature permits the utmost flexibility for the programmer.

Automatic programming is still another feature of the DATAmatic 1000. Delivered with each installation will be a library of routines which can be assembled by the programmer in many different variations by merely inserting a group of key instructions into the system. This automatic programming facility cuts to a minimum the time required to set up any desired program.

CHECKING

The DATAmatic 1000 is a completely internally checked machine. Four different types of automatic checking are performed to insure the accuracy that is required in processing business data. These built-in checking features when combined with the powerfully designed circuits (circuits which operate even though a tube is 50 percent weak) make the DATAmatic 1000 the most accurate machine available to management.

The four general types of automatic checking available are:

Transfer Checking - to prove information is transferred between any two portions of the machine correctly.

Arithmetic Checking - to prove the accuracy of all arithmetic operations.

Selection Checking - to prove that proper interpretation is made of the orders and that the correct memory locations were selected.

Tape Safe Checking - to prove the proper tape unit has been selected and to guarantee against destruction of information on tape due to malfunction.

In addition, other specific automatic checks are provided to ensure the utmost in reliability. There is even an automatic double-check which checks the check circuits.

These types of checking are completely automatic and do not concern the programmer. In the event of an error the machine will stop and the type of failure will be indicated by lights on the console.

As part of a normal maintenance procedure a Marginal Checking system is used. This system detects weak components prior to their failure thus insuring operating time that permits a day's work to be done in a day's time.

DATAmatic CENTRAL PROCESSOR (TYPE 1000)

The DATAmatic Central Processor (Type 1000) consists of a High Speed Memory, an Input Buffer Storage Unit, an Output Buffer Storage Unit and a Manipulative Section consisting of an Arithmetic Unit and a Control Unit. As many as 100 Magnetic Tape Units may be controlled by the Central Processor.

The operation of the Central Processor is governed by orders which are stored in the High Speed Memory. As described earlier, each order constitutes one word and consists of an operation code and three addresses. Unless otherwise specified, orders are selected in sequence from the High Speed Memory. However, as previously mentioned under Programming, there are special provisions whereby this sequence may be departed from for one or more orders.

Transfer of information between the Central Processor and the Magnetic File Units takes place by way of the Input and Output Buffer Storage Units. The information channels on the tape are numbered from 1 to 31. The sequence in which the words are recorded on the tape via the Output Buffer Storage Unit is preserved, so that when information is recovered from tape, the 62 words of each block are delivered by the Input Storage Unit in the same sequence, regardless of the direction of tape motion. Channel 1 on the tape is called the key channel. It contains words 1 and 2 of each block which can be coded words identifying the contents of the block if the tape is a file tape. The other channels are called satellite channels.

Isolation between the reading and recording circuits is provided by relays, controlled by the orders. When a channel is in the Write state, it is connected to the recording circuits; when it is in the Read state it is isolated from them. The states of the key and satellite channels of each Magnetic File Unit are independent, and the Magnetic File Units are independent of each other. Any combination of states of the key and satellite channels of all the Magnetic File Units is legitimate, except that no Magnetic File Unit may have its key channel in the Write state and its satellite channels simultaneously in the Read state.

In searching, the key channel only of the selected Magnetic File Unit is read to a designated channel of the Input Storage Unit. Each Magnetic File Unit is addressed by a two-digit number, and the Magnetic File Units are grouped according to the units digit of this address; all Magnetic File Units of a group search to the same Input Storage Channel.

The Input Buffer Storage Unit consists of two halves, the A half section and the B half section as shown in Figure 6, each capable of storing 62 words. Information may be transferred from a selected Magnetic File Unit to a selected half of the Input Buffer Storage or from a selected half of the Input Storage to the High Speed Memory under the control of an appropriate order. Except in the case of searching, a full block of infor-

mation comprising 62 words is transferred from the tape to the selected section of Input Storage. Except in the case of the Key Comparison orders, words are transferred sequentially from the selected section of Input Storage to the High Speed Memory, word 1 being transferred first. This is a destructive readout. As the words of the selected buffer half section are exhausted, fillers are automatically supplied. The two sections of the input Storage Unit are selected and operated independently.

During transfer of information between the High Speed Memory and Input or Output Buffer Storage, words are examined to see if they are sentinels. Sentinel sensing is the feature of the DATAmatic 1000 that provides an automatic monitoring of information under programmed control. This feature may be used with all orders that transfer information between the High Speed Memory in either Input or Output Buffer Storage Units. The sentinel is used by the Programmer to denote such conditions on tape as: beginning of information, end of information, classification of groups of information, the marking of an item as special or different, control input or output tape orders, and other such conditions.

A sentinel is any word having zeroes as the two highest order binary digits. The disposition of sentinels is specified in the descriptions of the orders.

Information is transferred to the Output Buffer Storage Unit for recording on magnetic tape. The Output Storage Unit consists of two sections each having a capacity of 62 words as shown in Figure 7. The A section of Output Storage accepts words transferred sequentially from the High Speed Memory. Under control of a Write order, the contents of the A section are transferred to the B section and subsequently recorded on the selected Magnetic File Unit, leaving the A section free to accept further information. If 62 or fewer words are transferred to Output Storage, the first two words will be recorded sequentially in the key channel, and fillers will be supplied where necessary to make up a full block. If more than 62 words are transferred to Output Storage before a Write order, sufficient words will be discarded, beginning with the first, to leave 62. The first two words not discarded will be recorded in the key channel. A full block of data (including fillers where needed) is always recorded.

Recording on magnetic tape, recovery of information from magnetic tape, and high speed manipulation, including transfer of information to and from the Buffer Storage Units, may all take place simultaneously, subject to the following restrictions (note that searching is considered separately from reading):

1. If any Magnetic File Unit is busy reading, no other Magnetic File Unit may be reading or searching.
2. If any Magnetic File Unit is searching, no other Magnetic File Unit in the same group (having the same units digit) may be searching.

3. Only one Magnetic File Unit may be writing at any one time.

4. If any Magnetic File Unit is reading or searching with its satellite channels in the Write state, the other Magnetic File Units are prevented from writing.

5. When any Magnetic File Unit is busy reading, searching or writing, a new order for the same Magnetic File Unit is delayed until the previous read, search or write is completed.

No precautions are necessary on the part of the user to prevent any of the above situations since automatic interlocking circuits prevent them from occurring.

LEGEND:

- D_s THE SIGN OF THE ORDER
- D_a THE MEMORY DESIGNATOR (THOUSANDS DIGIT) OF ADDRESS A
- D_b THE MEMORY DESIGNATOR(THOUSANDS DIGIT) OF ADDRESS B
- D_c THE MEMORY DESIGNATOR(THOUSANDS DIGIT) OF ADDRESS C

SUBSCRIPT
- $_u$ UNITS DIGITS
- $_t$ TENS DIGITS
- $_h$ HUNDREDS DIGITS

BIT POSITION	52	51	50	49	48	47	46	45	44	43	42
TRANSFER WEIGHT	8	4	2	1	8	4	2	1	8	4	2

ORDER WORD NO 1		memory designator			OPERATION COD						
	D_s	D_a	D_b	D_c	O_p						
ORDER WORD NO 2	D_s	D_a	B_1	D_c	OPERATION COD						
					O_p						
ORDER WORD NO 3		memory designator			OPERATION COD						
	D_s	D_a	D_b	D_c	O_p						
ORDER WORD NO 4		memory designator			OPERATION COD						
	D_s	D_a	D_b	D_c	O_p						
NUMERIC WORD	SIGN	1	0	1	11^{th} DIGIT	10^{th} DIGIT					
ALPHABETIC WORD	8^{th} CHARACTER (most significant)				7^{th} CHARACTE						

	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
GHT	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1

ORD	D_S	memory designator D_a	D_b	D_c	OPERATION CODE O_P	ADDRESS A: hundreds digits	tens digits	units digits	ADDRESS B: hundreds digits	tens digits	units digits	ADDRESS C: hundreds digits	tens digits	units digits	WEIGHT COUNT W

ORD	D_S	D_a	B_1	D_c	OPERATION CODE O_P	ADDRESS A: hundreds digits	tens digits	units digits	B_1	B_P	B_d	B_a	B_2	ADDRESS C: hundreds digits	tens digits	units digits	WEIGHT COUNT W

ORD	D_S	memory designator D_a	D_b	D_c	OPERATION CODE O_P	ADDRESS A: hundreds digits	tens digits	units digits	ADDRESS B: hundreds digits	tens digits	units digits	meaningless	C_2	WEIGHT COUNT W

ORD	D_S	memory designator D_a	D_b	D_c	OPERATION CODE O_P	ADDRESS A: hundreds digits	tens digits	units digits	B_h	0	1	0	1 / B_t	meaningless	ADDRESS C: hundreds digits	tens digits	units digits	WEIGHT COUNT W

RD	SIGN	1	0	1	11^{th} DIGIT	10^{th} DIGIT	9^{th} DIGIT	8^{th} DIGIT	7^{th} DIGIT	6^{th} DIGIT	5^{th} DIGIT	4^{th} DIGIT	3^{rd} DIGIT	2^{nd} DIGIT	1^{st} DIGIT	WEIGHT COUNT W

WORD	8^{th} CHARACTER (most significant)	7^{th} CHARACTER	6^{th} CHARACTER	5^{th} CHARACTER	4^{th} CHARACTER	3^{rd} CHARACTER	2^{nd} CHARACTER	1^{st} CHARACTER (least significant)	WEIGHT COUNT W

DATAmatic 1000 ORDER DESCRIPTIONS

Introduction

The DATAmatic 1000 employs a three-address order system in which each order contains a three-letter operation code and three four-decimal-digit addresses (A, B and C) arranged as shown in Figure 8.

Operation Code			Address A				Address B				Address C			
First letter	Second letter	Third letter	A thous.	A hund.	A tens	A units	B thous.	B hund.	B tens	B units	C thous.	C hund.	C tens	C units

Figure 8. DATAmatic Order Word Structure.

Normally an "address" refers to a storage location in the High Speed Memory and lies in the range 0000 - 1999. The usage of three addresses in an order is made clear by simple arithmetic examples, like "ADD the contents of Address A to the contents of Address B and deliver the result to Address C", which would be encoded ADD A B C.

However, there are orders which by their nature require less than three addresses, and, at the same time, require special numeric information. In such cases one of the address portions of the instruction word may carry numeric information which is not an address. This usage of an address portion is discussed fully in the order descriptions.

All programming can be done in this mnemonic notation. The Input Routine converts this order word to the internal machine form, so care should be taken to examine this internal form before serious detailed programming is undertaken.

Any order can be made a sentinel order provided its A address is not greater than 0999. To specify that the order is a sentinel order, place the letter "s" at the end of the order.

In the descriptions of the orders which follow, they are grouped for convenience into categories according to the type of function they perform.

Calculating Orders

The Calculating Orders group contains the usual arithmetic orders plus the SUBSTITUTE order. In all orders of this group the address positions are used to denote actual High Speed Memory Storage locations.

ADD ADD

Add the number at address A to the number at address B and deliver the sum to address C. In the event of an overflow, there is an automatic subsequence call to memory location 1988 where the first order of an appropriate routine is stored.

When using this order to modify another order the address of the order to be modified should go into the A position.

SUB SUBTRACT

Subtract the number at address B from the number at address A and deliver the difference to address C. In the event of an overflow, there is an automatic subsequence call to memory location 1988 where the first order of an appropriate routine is stored. When using this order to modify another order the address of the order to be modified should go into the address A position.

MUL MULTIPLY

Multiply the number at address A by the number at address B. Store the (rounded) high-order half of the 22-digit product in address C and the low-order half in the "Remainder" register (1995), each half accompanied by the sign of the product. Rounding is accomplished by adding 5 (with the same sign as the product) into the high-order digit of the Remainder register and permitting carry into the low-order digit of address.

DIV DIVIDE

Divide the number at address B by the number at address A. Deliver the quotient to address C and the remainder to the Remainder register (1995), unless the numerator equals or exceeds the denominator. If the numerator equals or exceeds the denominator in absolute value, make an automatic subsequence call to memory location 1986 where the first order of an appropriate routine is stored.

SST SUBSTITUTE

From the numbers stored at address A and address C form a new number and store it at address C. The new number is formed under the control of an Extractor word which is stored at address B. The Extractor may control the extraction of alphabetic or numeric characters or portions of characters. Thus, wherever the extractor digit is a 1, the new word gets its corresponding character from address A. Wherever the extractor digit is a 0; the corresponding character in address C is preserved.

Notes

Calculating Orders

1. The Calculating orders are of word type 1 (see detailed word structure at end of orders.)
2. MULTIPLY - Both the Select Order Register (1994) and the Sentinel Register (1997) (see description of Addresses of Significance) are used by the Arithmetic Unit in performing multiplication. After the completion of a multiply order, unless the product is transmitted to one of them, these two registers contain respectively 7 times the word at address A and 4 times the word at address A - in each case without a sign.
3. MULTIPLY-DIVIDE - If either operand contains a non-decimal 4-bit group or an incorrect sign, a weight count error occurs.
4. SUBSTITUTE - The Extractor stored at address B may have any bit configuration. Each bit of address C is preserved if the corresponding bit of address B is a zero - otherwise the bit of address C is replaced by the corresponding bit of address A.

Shift Orders

A group of orders are provided for shifting information within the machine. Shifting is defined as moving the characters of a machine word either right or left within the word itself.

In the Shift Orders, the A and C addresses are used for denoting High Speed Memory storage locations; the B address contains information controlling the amount of the shift. No attempt should be made to modify the amount of the shift internally without consulting a description of the internal machine structure of the order.

SLP SHIFT LEFT PRESERVING SIGN

Shift the word at address A to the left by the number of digit spaces indicated in address B, keeping the sign unchanged and unshifted. "B" must be in the range 0-12. Deliver the result to address C. The word remains unchanged at address A.

SLA SHIFT LEFT, ALPHABETIC

Shift the word at address A to the left by the number of alphabetic spaces indicated in address B, and deliver the result to address C. "B" lies in the range 1-8. This shift includes the sign position. The word remains unchanged at address A.

SLN SHIFT LEFT NUMBERIC, SIGN INCLUDED

Shift the word at address A to the left by the number of digit spaces indicated in address B, including the sign position. "B" must be in the range 0-12. Deliver the result to address C. The word remains unchanged at address A.

SRP SHIFT RIGHT PRESERVING SIGN

Shift the word at address A to the right by the number of digit spaces indicated in address B, keeping the sign unchanged and unshifted. "B" must be in the range 0-12. Deliver the results to address C. The word remains unc hanged at address A.

SRA SHIFT RIGHT ALPHABETIC

Shift the word at address A to the right by the number of alphabetic spaces indicated in address B, and deliver the result to address C. "B" lies in the range 1-8. This shift includes the sign position. The word remains unchanged at address A.

SRN SHIFT RIGHT NUMERIC, SIGN INCLUDED

Shift the word at address A to the right, by the number of digit spaces indicated in address B, including the sign position. "B" must be in the range 0-12. Deliver the result to address C. The word remains unchanged at address A.

Notes

Shift Orders

1. The Shift Orders are of word type 4 (see detailed DATAmatic Order Word Structure following description of orders). The amount of shift, is controlled by B_h and B_t. In every case the number of 4-bit shifts to be made is indicated by B_h, which is a hexadecimal digit in the range 0-12. For SLP and SRP orders $B_t = 0$. For the other shifts B_t can be zero or 5. If it is 5, an extra 2-bit shift occurs after the indicated number of 4-bit shifts has been completed. In the alphabetic shifts, the Input Routine converts "B" to the appropriate number of 4-bit shifts, and uses the 2-bit shift if necessary.
2. The B address may be modified by additions, except through the transition between $B_h = 9$ and $B_h = (10)$ (hexadecimal). The rule for modifying orders given with the ADD order description should be followed.

Buffer Transfer Orders

The orders of this group are used for transferring words between the Buffer Storage Units and the High Speed Memory. Information transmission between the High Speed Memory and magnetic tape passes through the Input and Output Buffers. Orders of the Tape Control group are concerned with the phase of the transmission between the magnetic tape and the Buffers. In addition to the Buffer Transfer orders described here the Key Comparison orders (described under Comparison Orders) transfer words into the High Speed Memory from the Input Buffer Storage.

The word structure of these words is:

Operation Code			Address A				Address B				Address C			
First letter	Second letter	Third letter	A thous.	A hund.	A tens	A units	B thous.	B hund.	B tens	B units	C thous.	C hund.	C tens	C units
							B1			B2				
			Storage				Control				Subsequence			

Address B is divided into two parts B1 and B2. B1 consists of the hundreds and and thousands digits of address B. B2 consists of the units and tens digits of address B. Both B1 and B2 are restricted to the range 1-32. No attempt should be made to modify address B internally without reference to the bit-structure of the order.

In each of the orders of the Buffer Transfer group, address A is the first location of a segment of the High Speed Memory to or from which B2 words are to be transferred. The range of addresses specified by A and B2 should not include Special Registers nor, in the same order, both 0999 and 1000. Address C provides for a Subsequence Call if desired and should not be 1990.

If a Weighted Count error is detected in any word transferred in, or in the Buffer word following the last one transferred in, the result is an automatic Subsequence Call to register 1985 where the first order of an appropriate routine is stored, or else results in a computer Stop, depending upon whether the Central Console "Rerun" switch is on or off.

For each type of order in this group which provides for transfer from the Input Buffer, the transfer can be made from either the A section or the B section. The choice of section is governed by the third letter of the code symbol.

Thus, if the third letter of the code symbol is:

A - Transfer from the A section of the buffer
B - Transfer from the B section of the buffer
S - Transfer from the same section of the buffer to which the last previous connection was made (by Transfer In, Double Transfer and Select, Transfer and Select, or Read Orders)
D - Transfer from a different (the opposite) section of the buffer to which the last previous connection was made (by Transfer In, Double Transfer and Select, Transfer and Select, or Read Orders)

TRANSFER IN

The eight **TRANSFER IN** orders fall into two sets as follows:

TIA TIB TIS TID	Hold up if necessary, via the interlock, the transfer of words from Input Buffer to the High Speed Memory until the Input Buffer has received a block of words from a file unit as a result of the last Read order initiated prior to this order. This interlocking is necessary for the situation in which an order is given to transfer information out of one half of the Input Buffer after a Read order has been given to read information from tape into that same Buffer half.
TBA TBB TBS TBD	Transfer words from Input Buffer to High Speed Memory during the period between the time a Read order is given and the time that the transfer of words from the file unit to the Input Buffer is actually begun, by bypassing the interlock mentioned above.

Each of the orders causes the transfer of B2 words from the Input Buffer to consecutive High Speed Memory locations starting at address A. The B2 words transferred and also the next word in the Input Buffer are examined for sentinels. The first sentinel sensed is stored in the Sentinel Register (1997). If no sentinel is sensed a PASS order (see Control Orders) is stored in the Sentinel Register.

If B2 exceeds the number of words contained by the Input Buffer section then fillers will be added to make up B2 words. These fillers are sentinel Sequence Change orders (see Control Orders) whose A and B addresses are void and whose address C is 1985. If B2 equals the number of words contained in the Input Buffer section a filler of this type (being a sentinel) will go to the Sentinel Register (1997).

Make a Subsequence Call to address C. B1 is not used.

DOUBLE TRANSFER AND SELECT

There are eight Double Transfer and Select orders which fall into two sets of four each. The sets are identical except for the fact that interlocks are used or not used, as described below:

DTA
DTB
DTS
DTD — At step (2) below delay, by means of an interlock, the transfer of words from the Input Buffer to the High Speed Memory until the Input Buffer has received a full block of new words as a result of the last Read order initiated prior to this order.

DBA
DBB
DBS
DBD — At step (2) below begin transferring words immediately from the Input Buffer to the High Speed Memory, bypassing the interlock referred to above

There are four steps required for the performance of each order:

(1) Transfer B2 words to the Output Buffer Storage from the consecutive High Speed Memory locations starting at address A. Output Buffer overflow is not examined for sentinels.

(2) Transfer B2 words from the Input Buffer to the consecutive Memory locations starting at address A. Examine the B2 words transferred and the next Input Buffer word for sentinels. The first sentinel sensed is stored in the Sentinel Register. If no sentinel is sensed, a Pass order is stored in the Sentinel Register.
If B2 exceeds the number of words contained in the Input Buffer section then fillers will be added to make up B2 words. These fillers are sentinel Sequence Change orders (see Control Orders) whose address B is void and whose address C is 1985. If B2 equals the number of words contained in the Input Buffer section a filler of this type (being a sentinel) will go to the Sentinel Register (1997).

(3) Extract one digit from the B1th word transferred from the Input Buffer, add it to the units digit of address C permitting carry into the tens digit, and make a Subsequence Call to the resultant address C. The particular digit which is extracted will be determined by the word in the Extractor Register which can be made to choose any one of the digits of the B1th word.

(4) Store this order itself in the Select Order Register (1994) in its original form (i.e., not in the modified form it has after the completion of step (3)).

TRANSFER AND SELECT

The eight Transfer and Select orders are identical to the eight corresponding Double Transfer and Select orders except that step (1) is omitted. Consequently, all description of these orders apply to Transfer and Select, except for step (1). The symbols for these orders are:

TSA TSB TSS TSD	At step (2) hold up, via an interlock, the transfer of words from Input Buffer Storage to High Speed Memory until Input Storage has received a full block of new words as a result of the last Read order initiated prior to this order.
BSA BSB BSS BSD	At step (2) begin transferring words immediately from the Input Buffer Storage to the High Speed Memory, bypassing the interlock mentioned above.

TXO TRANSFER OUT

Transfer the number of words indicated by the units and tens digits of address B to the Output Buffer Storage from the consecutive memory locations starting with address A. If there is an overflow of words from the Output Buffer Storage, examine the overflow words for sentinels. The first sentinel word which overflows is transferred to the Sentinel Register (1997). If no sentinel overflows, a Pass order is stored in this Sentinel Register. Address C can be used for a subsequence call if desired.

The number of words transferred by this order can vary from 1 to 32.

Notes

Buffer Transfer Orders

1. The Buffer Transfer orders are of word type 2 (see detailed DATAmatic Order Word Structure following description of orders). The numbers B1 and B2 are 5-bit binary numbers (with the high order bit of B1 located in bit position 50) covering the range 1-32, with 32 being represented by all zeros.

   The three basic types of orders are specified by the following 2-digit (hexadecimal) Operation Codes:

Order Type	Operation Code
TRANSFER IN	(15) (3)
DOUBLE TRANSFER AND SELECT	(15) (10)
TRANSFER AND SELECT	(14) (11)

   The eight variations of each type are obtained by using the three control bits in bit positions 22, 23, and 24. If $B_p = 0$ the Input Buffer interlock remains in effect and this corresponds to the first set of 4 orders under each heading. If $B_p = 1$ the interlock is inactivated giving the second set of 4 orders.

   The Buffer to Memory connection is controlled by bits B_a and B_d as shown in the following table:

B_d	B_a	Letter Designation	Effect on the Buffer-Memory Connection
0	0	S	Leave unchanged
0	1	A	Connect to the A-section
1	0	B	Connect to the B-section
1	1	D	Change the connection

Notes

Buffer Transfer Orders (Cont.)

2. **DOUBLE TRANSFER AND SELECT** (8 orders), **TRANSFER AND SELECT** (8 orders). Step (3) of the description of these orders can be done with more generality if the bit structure of the order is taken into account. The following substeps describe this step in detail.

(3a) Form a word, K, which has binary ones in those bit positions wherein both the (B2-B1)th word transferred in and the word in the Extractor Register (1993) have binary ones, and zeros elsewhere. Either word may have any bit configuration whatever.

(3b) Superimpose all 12 of the 4-bit groups (hexadecimal digits) of the word K resulting from substep (3a) onto one digit position. This results in a hexadecimal digit which has a binary 1 in a given one of its four bit positions if and only if one or more of the 12 digits of K has a binary 1 in the corresponding position.

(3c) Add the hexadecimal digit constructed in substep (3b) to the units digit of address C of the order, permitting carry into the tens digit. This addition is accomplished as if the hexadecimal digit had been converted to a decimal in the range 0-16 except that a weight count error occurs if

- (c_1) the sum of the hexadecimal digit and the units digit of address C exceeds 19 or
- (c_2) the sum of the hexadecimal digit and address C causes a carry into the thousands column of address C.

Make a Subsequence Call to the resultant address C.

Memory Transfer Orders

There are three orders in the Memory Transfer group and they are used for making transfers of information from one part of High Speed Memory to another. One of them, the Transfer Internally (TXI) order, is the only order of the three which contains control information in the address C position.

TXI TRANSFER INTERNALLY

Transfer the number of words indicated by the units and tens digits of address C from consecutive memory locations starting with address A to consecutive memory locations starting with address B. The number of words transferred lies in the range 1-32. The range of addresses specified by "A" and "C" or by "B" and "C" should not include both 0999 and 1000 or any of the Special Registers .

If the programmer desires to modify the number of words expressed in address C, internal machine word structure should be understood.

TTX TWIN TRANSFER

Transfer the word in the Select Order Register (1994) to address A, and the word at address B to address C. This is a special order designed for use with the DOUBLE TRANSFER AND SELECT and the TRANSFER AND SELECT orders in sorting.

No Transfer is made to address A if this is the address of a Special Register (see Addresses of Significance). Neither address B nor address C should be 1990 (the Control Register).

TXS TRANSFER AND SUBSEQUENCE CALL

Transfer the word stored at address A to address B and make a subsequence call to address C. Neither address B nor address C should be 1990.

Notes

Memory Transfer Orders

1. **TRANSFER INTERNALLY** is an order of word type 3 (see detailed DATAmatic Order Word Structure following description of orders) and the number of words transferred is controlled by C_2 which consists of 5 bits. When all bits are zero, 32 words are transferred.

2. Address C cannot be modified by addition or subtraction through any part of its range which includes the pairs 9 and 10, 15 and 16, or 25 and 26.

Tape Control Orders

The Tape Control Orders are those which govern reading, writing, searching and rewinding of the Magnetic File Units. In each of the Tape Control Orders address B can be used for changing the Sequence Counter and address C for making a Subsequence Call. The units and tens digits of address A are used to designate the desired Magnetic File Unit.

If one of these orders (except the REWIND order) is given after the tape has reached its end (or its beginning in the case of the orders which move the tape backwards) the order is not executed. Instead, it is transferred to the Current Order Register (1999), and an automatic Subsequence Call is made to register 1989 where the first order of an appropriate routine is stored.

The operation of putting the key and satellite channels into the appropriate state for Reading, Searching, or Writing involves relay switching time; hence an order of this type can be performed more quickly if the channels have been left in the correct state by a previous order of the same type.

READING

Each READ order affects a Magnetic File Unit designated by the tens and units digits of address A. Each READ order (except for the READ FORWARD KEY and READ BACKWARD KEY) causes both the key and satellite channels of the specified Magnetic File Unit to be put into the Read state, if they are not already in that state. Then one block (62 words) from the designated tape is transferred to the indicated section of the Input Buffer. The reading may be accomplished in either the forward or reverse direction of tape movement. The resulting arrangement of information in the Input Buffer is independent of the direction of tape movement when a given block is read.

The third letter of the Operation Code governs the portion of Input Buffer into which the information from the tape is read.

READ FORWARD

RFA	Read Forward to the A section of the Input Buffer.
RFB	Read Forward to the B section of the Input Buffer.
RFD	Read Forward to that section of Input Buffer which was not read into by the last previous read order (i. e., change sections). Connect the section not being read into to the High Speed Memory.

READ BACKWARD

RBA	Read Backward to the A section of the Input Buffer.
RBB	Read Backward to the B section of the Input Buffer.
RBD	Read Backward to that section of Input Buffer which was not

read into by the last previous read order (i. e., change sections). Connect the section not being read into to the High Speed Memory.

There are two orders which permit the reading of the key channel into the B half of the Input Buffer, leaving the satellite channels in the Write state:

RFK READ FORWARD, KEY CHANNEL

Put the key channel of the Magnetic File Unit designated by the units and tens digits of address A into the Read state and the satellite channels in the Write state - if they are not already in these states, Read the key channel of one block to the B section of the Input Buffer, moving the tape forward.

RBK READ BACKWARD, KEY CHANNEL

Same as RFK except that tape is moved backward.

WRITING

Writing consists of transferring one block of words from the Output Buffer to the Magnetic File unit designated by the units and tens digits of address A. If the Output Buffer is not full when the Write order is given, "fillers" are supplied in sufficient quantity to complete a block of 62 words. Each of these fillers is a sentinel Sequence Change order whose A and B addresses are void and whose C address is 1984.

If, on account of reaching the end of tape, a Write order can not be executed (see the earlier general discussion of Tape Control orders), the contents of the Output Buffer remain unchanged except that some fillers will have been added if needed.

Writing can be done only in the forward direction of tape movement.

WFA WRITE FORWARD

Put both key and satellite channels of the designated Magnetic File Unit into the Write state, if they are not already in this state. Add fillers if necessary, and then Write one block.

WFP WRITE FORWARD, EXCEPT ON KEY CHANNEL

Put the satellite channels of the designated Magnetic File Unit into the Write state and the key channel into the Read state, if they are not already in the required states. Add fillers if necessary and then write one block.

SEARCHING

It is possible to search up to 10 tapes simultaneously, comparing the contents of the key channel of each tape with an interrogation key for branching control. One search

order is used for each tape being searched (10 orders for 10 tapes) but the speed of processing is such that all the tapes being searched can be moving at the same time.

This is accomplished by designating a certain portion of the A-half of the Input Buffer to serve as ten independent "2-word Search Buffers" for each of the ten (or fewer) tapes. These ten 2-word Search Buffers are numbered zero through nine. The searching of any given tape is accomplished by reading its key channel into the 2-word Search Buffer having the same number as the units digit of that tape. This essentially means that the tapes can be considered grouped according to their units digit and only one tape from a group may be searched at a time. Thus, for example, tapes 20, 11, 42, 63, 84, 55, 36, 07, 98 and 79 can be searched at the same time. The example shows the restriction on the units digit but flexibility of the tens digit.

Only the key channel of each block is read when searching. The keys are then transferred from the Input Buffer to the High Speed Memory by the First and Second Key Comparison Orders (see Comparison Orders discussed next).

SFR SEARCH FORWARD, READING

Put the key and satellite channels into the Read state, if they are not already in this state and Search one block forward.

SFW SEARCH FORWARD, WRITING

Put the key channel into the Read state and the satellite channels into the Write state, if they are not already in the required state, and search one block forward.

SBR SEARCH BACKWARD, READING

SBW SEARCH BACKWARD, WRITING

The two SEARCH BACKWARD orders are the same as the corresponding SEARCH FORWARD orders except that the tape moves backward.

REW REWIND TAPE

Rewind the tape on the Magnetic File Unit designated by the units and tens digits of address A. Upon completion of this order the tape is positioned for Reading or Writing on the first block.

Comparison Orders

The Comparison Orders provide for comparing two quantities and branching a routine on the basis of this comparison. The branching is accomplished by changing, or by leaving unchanged, the contents of the Sequence Register.

NUMERIC COMPARISONS

The Numeric Comparisons cause an algebraic comparison to be made between the quantities stored at addresses A and B. These comparisons treat +0 and -0 as algebraically equal.

LCN LESS THAN COMPARISON, NUMERIC

If the number at address A is algebraically less than or equal to the number at address B, change the Sequence Register to address C.

ICN INEQUALITY COMPARISON, NUMERIC

If the number at address A is not algebraically equal to the number at address B change the Sequence Register to address C.

ALPHABETIC COMPARISONS

The Alphabetic Comparisons make it possible to distinguish between +0 and -0; and, therefore, between alphabetic characters which may extend into the sign position. The order of alphabetic and numeric characters is: 0, 1, 2, ... , 9, A, B, C, ... Z. Thus, in particular, all numerics precede (are "algebraically less than") all alphabetics.

LCA LESS THAN COMPARISON, ALPHABETIC

Change the Sequence Register to address C if the word at address A is alphabetically less than or equal to the word at address B.

ICA INEQUALITY COMPARISON, ALPHABETIC

If the words at addresses A and B are not identical, change the Sequence Register to address C.

KEY COMPARISONS

The two Key Comparison orders are used for examing the Keys brought into the A half of the Input Buffer by the Search orders described in the last group. These Keys are words 1 and 2 of the block of 62 words and identify the items in that block. An order of this type transfers a Key from one of the ten Search Buffers, mentioned in "Searching"

above, to address A. The particular Search Buffer is picked out by the units digit of address A. The order then compares the word at address A with that at address B to determine whether or not the Sequence Register should be changed to address C. The comparison is of the "alphabetic" type just described.

If a Search order has been given but not completed, a Key Comparison order referring to the same Search Buffer; i. e., which has the same units digit in address A as does the Search order, will be delayed by an interlock until the Search order is completed. Key Comparison orders referring to other Search Buffers are not affected.

If a Key Comparison order is given before the corresponding Search Buffer has been refilled and also before a Search Order has been given to refill it, the comparison proceeds using whatever was in address A previously. No transfer is made from the buffer and no interlocking occurs.

If the word at address A when the comparison occurs is a sentinel, it is stored in the Sentinel Register (1997); otherwise a Pass order (see Control Orders) is stored in the Sentinel Register.

Address A should not be a Special Address.

The features distinguishing between the two Key Comparison orders are as follows:

FKC FIRST KEY COMPARISON

Transfer the first Key from the Search Buffer specified by the units digit of address A to address A. If the resulting word at address A is greater than or equal to the word at address B, change the Sequence Register to address C.

SKC SECOND KEY COMPARISON

Transfer the second Key from the Search Buffer specified by the units digit of address A to address A. If the resulting word at address A is less than or equal to the word at address B, change the Sequence Register to address C.

Notes

Comparison Orders

(1) In the numeric comparisons, bits 49, 50 and 51 are ignored. In the alphabetic comparisons, these bits are treated the same as any others.

Print Orders

PRA PRINT ALPHABETIC

Print on the Central Console typewriter, in alphabetic form, the word at address A. Address B can be used if it is desired to change the Sequence Register and address C can be used to subsequence out of the present routine if desirable.

PRN PRINT NUMERIC

This order is the same as PRINT ALPHABETIC, except that the printing is in numeric form.

Control Orders

PSS PASS

Go to the Sequence Register for the next order. The content of addresses "A", "B", and "C" is immaterial.

OST OPTIONAL STOP

Stop, or not, according to the relationship of address B and a set of eleven switches on the console. Subsequence call to address C.

The eleven switches on the console consist of, first, a three-position toggle switch called the "Optional Stop" switch, and, second, a set of ten two-position toggle switches called the "Breakpoint" switches, numbered 1 to 10.

The address B in this order is a twelve-digit number consisting entirely of 0's and 1's. The digit positions are numbered 1 to 12, from left to right.

If the digit in position 12 is 1, stop, regardless of the positions of the Optional Stop and Breakpoint switches. If the digits in positions 11 and 12 are both 0, the position of the Optional Stop switch is the next controlling factor. If it is set to "stop", stop; if it is set to "proceed", proceed. Both of these take place regardless of the positions of the Breakpoint switches.

The Breakpoint switches determine whether or not a stop occurs only when the digits in positions 11 and 12 are both 0 and the Optional Stop switch is set to "compare". In this case, stop if there is a 1 in any position for which the corresponding Breakpoint toggle switch is on; otherwise, proceed.

If the Central Processor stops because of an effective Optional Stop order, there are two Control Console buttons for starting again. Pushing the "Start" button will cause a start by making a Subsequence Call to address C. Pushing the "Set Up" button and then the "Start" button will cause a start with the

Sequence Register determining the next order. Address C must not be 1990. Address A does not have to be void but it must not contain non-numeric data.

SCS — SEQUENCE CHANGE

Change the Sequence Register to address B, Subsequence Call to address C.

Address A does not have to be void (0000) but it must contain numeric data.

BAR — BRANCH AND RETURN

Subsequence call to address C. Change the Sequence Register to address B. Store in address A an order which can later be used to change the Sequence Register back to its present reading. (The Sequence Register has already been incremented by one before being used here).

Neither address A nor address C should be 1990.

Notes

Control Orders

OPTIONAL STOP

The OPTIONAL STOP order operates as described above. However its bit structure after being transformed by the Input Routine is such that control is accomplished by the individual bits of address "B".

"Stop" if bit 17 is a 1.
"Proceed" if bit 17 is 0 and bit 18 is 1.

Each of the 10 "Breakpoint Switches" corresponds to one of the bits 19 through 29. Thus, for example, an Optional Stop occurs when there is a binary 1 in bit position 19, the Breakpoint Switch Zero is "ON", and the "Optional Stop" switch is set to COMPARE.

THE DATAmatic INPUT CONVERTER TYPE 1200

Introduction

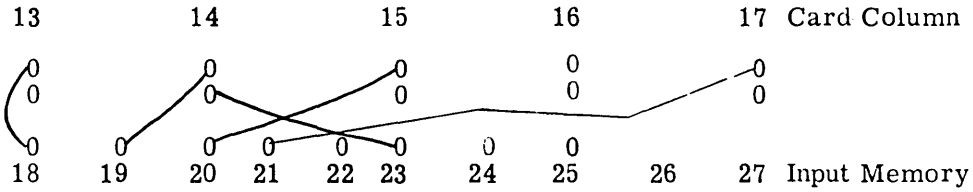
The DATAmatic Input Converter (Type 1200) is used to read source data from punched cards and write it on magnetic tape in a form substantially edited for use by the DATAmatic Central Processor (Type 1000). For convenience, this operation may be thought of as divided into three steps:

1) reading information from cards to an Input Memory unit;
2) transferring information from the Input Memory unit to the Output Memory;
3) writing information from the Output Memory onto tape.

Each of the first two steps is carried out under control of a plugboard. The third step occurs automatically upon completion of the first two, and will not be treated in this discussion. Automatic checking insures reliability of conversion while the converter is in operation. Reference to Figure 9, Input Converter, may prove helpful in the discussion that follows.

Reading Information from Card to Input Memory.

The card reader operates at the rate of 900 eighty-column cards per minute. Each card column read may be wired to one of 100 positions in the Input Memory unit or be discarded. Up to twenty columns of an 80 column card may be wired to two positions of the Input Memory. If less than 80 columns of punched data are to be converted, a proportionate increase in columns that can be duplicated will be realized up to the 100 position maximum. Triplication of card columns is not permitted. An example of the wiring is shown.



In this diagram, card column 13 is wired to position 18, card column 14 to positions 19 and 23, column 15 to positions 20 and 22, column 16 discarded and column 17 wired to position 21. It should be noted that all transposition, duplication, and discarding of information from the card must be done with this plugboard which is called the Card Reader Plugboard.

Each card is read twice, the second reading being used to check the first. After the second reading, the information from the card is sent to the Input Memory unit as described above. The card then moves to a printing station where a number is printed on the card. This number is called the Continuous Sequence Number and is emitted by the card

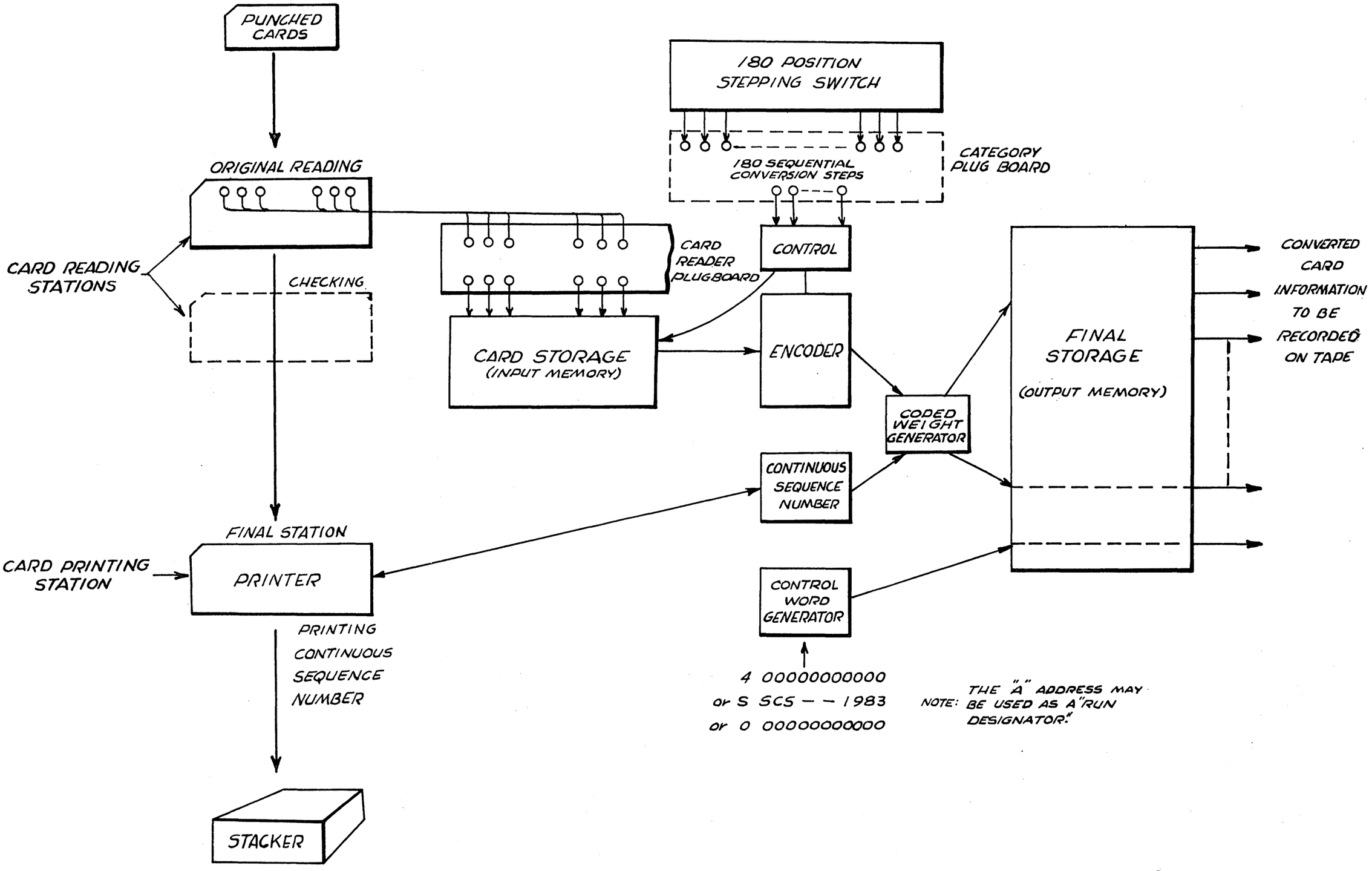


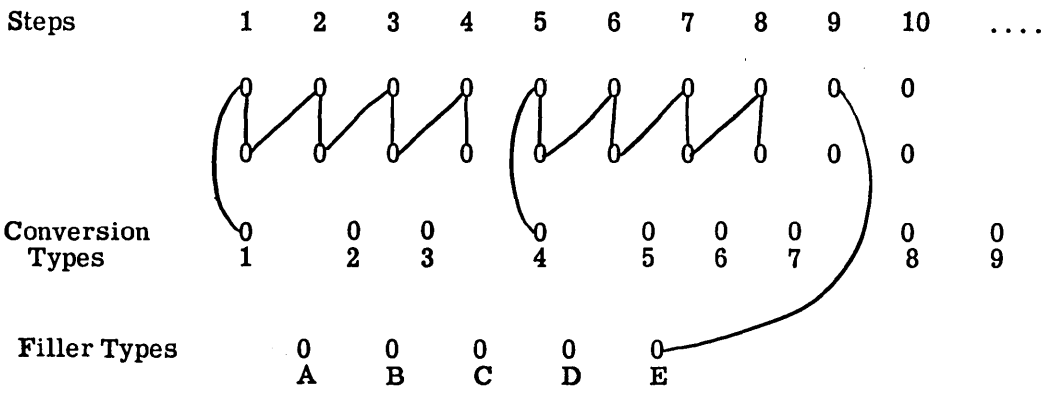
FIGURE 9
INPUT CONVERTER TYPE 1200

reader. There are twelve rotating number wheels associated with the Input Converter, and as the card reader is loaded with a batch of cards, the twelve digit number to identify the first card is set by manually rotating these wheels. This number is printed on the first card, and, as each additional card is read, the number is increased by one and printed on the card. Thus, the cards are numbered consecutively in the order in which they are processed. It should be noted that the five high order digits are fixed so that when the 7 low order digits reach 9,999,999, they start again at zero. This number is also transmitted to the Output Memory unit for identification purposes. Choice of the high order digits should be made mindful of the automatic sentinel sensing features of the DATAmatic 1000 Central Processor. After the Continuous Sequence Number has been printed, the card is sent to the stacker. The printing operation described here is independent of the plugboard wiring.

Transferring Information from Input Memory to Output Memory.

The 100 positions of the Input Memory storage are converted sequentially and under control of the Category Plugboard. This plugboard has hubs for a maximum of 180 conversion steps. Nine ways of converting a single card column of information are available; these are listed in Table 1. Table 2 lists the maximum number of steps to which a particular hub associated with any one conversion method may be applied. As will be illustrated later, each position of the Input Memory to be converted must be wired such that the desired mode of conversion is applied. Between successive converted card columns of information zero bit fillers may be introduced, as desired, by proper wiring. Fillers may also be used to space information as desired within the DATAmatic word. Table 3 lists the filler types available and the number of fillers that may be generated from any one hub associated with a specific filler type. The information in the Input Memory unit must be converted in sequence and no information in positions between the first and last positions of data to be converted may be skipped. This requirement indicates the importance of the previous statement to the effect that all transposition, duplication, and discarding of card information must be done with the Card Reader Plugboard. When the proper number of steps have been wired to produce exactly 14 words of 48 binary digits each, an end of program must be wired. If the number of binary digits produced is not correct, the Converter will halt.

The Category Plugboard will be wired in the following manner:



where each step wired represents either one converted column from the Input Memory unit or insertion of one filler.*

The 14 words which have been produced are sent to the Output Memory unit and are stored in word positions 1-14. The Continuous Sequence Number which was printed on the card from which this information originally came is placed automatically into word position 15 in the Output Memory unit. Position 16 of the Output Memory unit, the Control Word, is also filled automatically with one of three words. If no illegal punches (as defined in Table 1) have been detected in reading the card, the word will have the decimal digit 4 in the sign position and the rest of the word will be zero. If an illegal punch has been detected, i.e., any punch configuration that is contrary to those specified for this particular category, the word will be a sentinel Sequence Change order with the B address void and the C address equal to 1983. If a converter error has occurred, the word will contain all blanks. It should be noted that switches are available by means of which a controllable A address may be automatically inserted into this 16th word thus providing a "run identification" number. The bit construction of this number is restricted and must have a weight count of 9. Table 4, the Control Word, summarizes the above information. Words 1-16 in the Output Memory will be written as words 1-16 of the tape block.

The next card processed will be converted in the same fashion and stored in the Output Memory. Words 1-16 of the Output Memory will then be written on a block of tape as words 17-32 of the block. The last 30 words of the block will be unchanged. Each block of tape written by the Input Converter will thus contain information corresponding to that in two successive cards, except for the case in which an odd number of cards are to be processed. In this case, the final block of tape written will contain

*

A complete listing of available card punches per category and their representation in DATAmatic tape code is given on Table 5.

only 16 words from the Input Converter and the remaining 46 words on tape will be unchanged.

Automatic Checking

Automatic checking occurs during the conversion process. If the Input Converter makes an error it will stop, but, because it cannot stop instantly, reading of cards and writing on tape may occur after the error. However, cards read after the error signal will not be delivered to the regular stacker. They will be sent to a reject pocket, will not be processed or recorded on tape and will not have had Continuous Sequence Numbers printed on them. However, the converted information containing the error will be written on tape before the Input Converter is able to stop. (The card in this case will have a Continuous Sequence Number and will be lodged in the regular stacker.) The record can then be singled out during the Central Processor operation, thus permitting corrective steps to be taken as are necessary. As is evident, this 16th word may be either the 16th or the 32nd word on tape.

If a long section of the tape has been coded for rejection (approximately 8 inches or longer), the converter may not be able to bypass this section before the next block is ready to be written. In this case the converter will stop with cards in the reject pocket as described for an error. The tape, however, will be advanced until a good block is found, and the block in the Output Memory will be written before the tape and writing circuits are halted. Suitable indicator lights are available so that a machine stop can be identified as due to either a converter error or a long length of tape.

The converter will require a manual restart for any type of stop.

Application

In order to illustrate the above discussion, a punched card containing representative data will be converted to tape. Figure 10 shows this card with the first 45 columns punched as follows:

Information	Columns	Contents
Clock Number	1 - 6	152973
Dept.	1 - 2	15
Man No.	3 - 6	2973
Name	7 - 30	John Robert Wellington
Pay Rate	31 - 34	1625
Dependents	35	4
Hours Worked	36 - 39	4000
Date	40 - 45	021556
Mo.	40 - 41	02
Day	42 - 43	15
Yr.	44 - 45	56

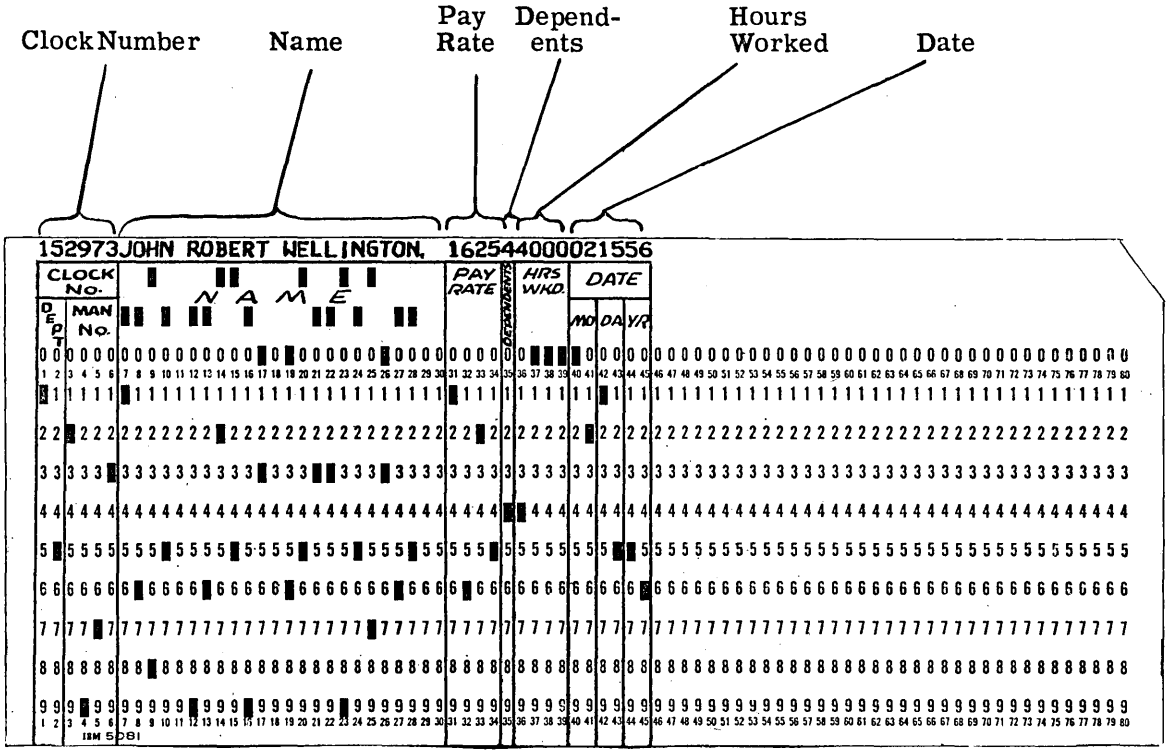


Figure 10. Punched Card With Representative Data.

The preceding information is to be written on tape as indicated in Figure 11. Two successive preparatory steps are required for this operation:

1. The Card Reader Plugboard must be wired to edit the incoming data, i. e., the data must be transposed, duplicated and/or discarded as is necessary to conform to specified tape requirements.
2. The Category Plugboard must be wired so that the Input Memory storage contents are sequentially interpreted and converted in accordance with the specified tape format. Consistent with this the Plugboard must be wired so that fillers are introduced, as necessary, to properly space the converted data.

Details of Programming

The two successive steps indicated in Application are summarized in Figure 12. They are now treated in detail.

1. Wiring the Card Reader Plugboard

The various items on punch card are in the sequence:

(1) Clock Number
(2) Name
(3) Pay Rate
(4) Dependents
(5) Hours Worked
(6) Date

It is desired that the Card Reader Plugboard place these items in the following sequence in order that they conform to the specified tape format:

(1) Clock Number
(2) Pay Rate
(3) Name
(4) Hours Worked
(5) Pay Rate
(6) Dependents
(7) Date
(8) Columns 38 - 45

It should be noted that this new format requires a duplication of Pay-Rate. In addition, it should be noted that columns 38-45 are duplicated. This is done in order to have columns available with unpunched RX positions for sign conversion purposes.

INPUT CONVERTER
TAPE FORMAT

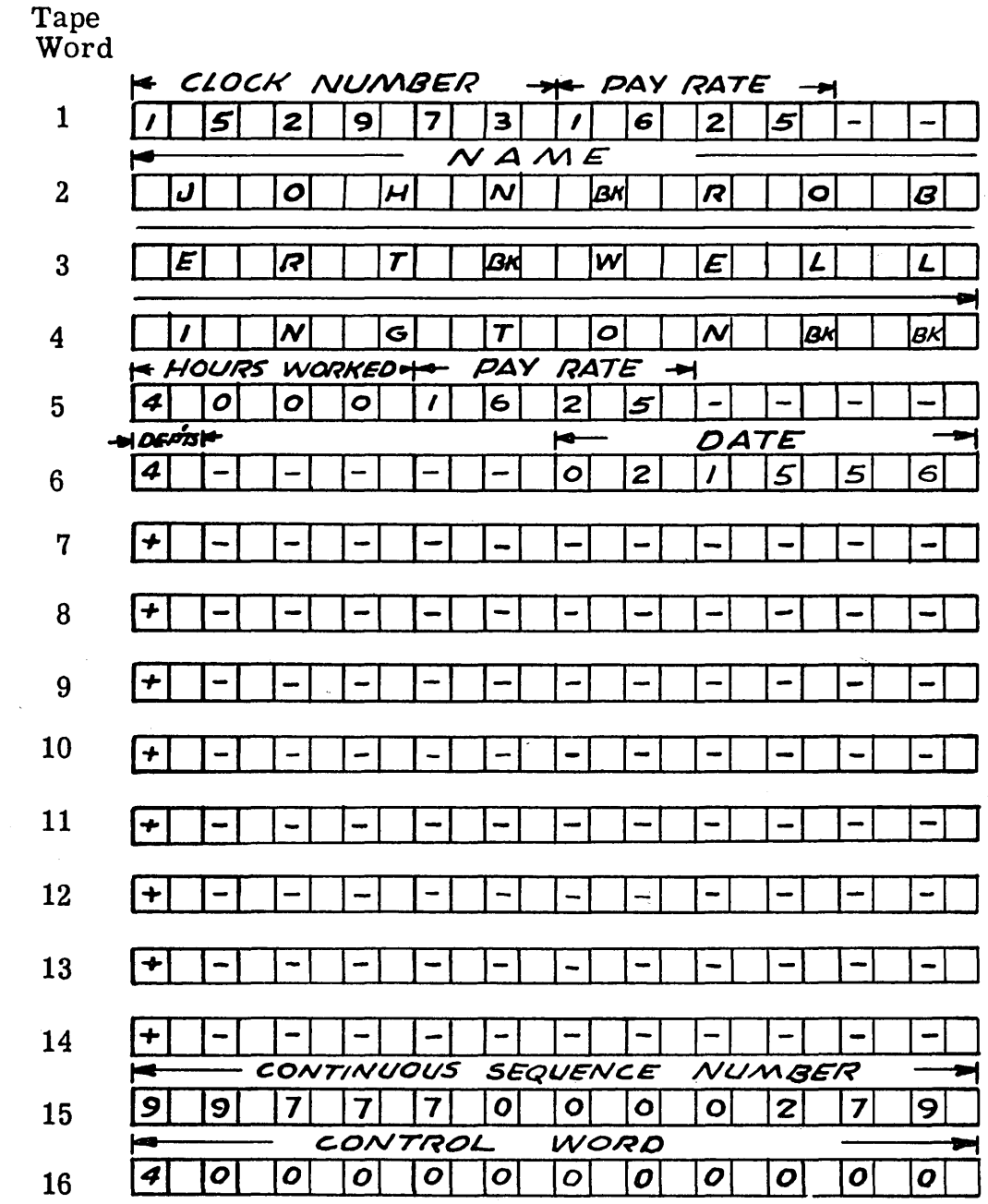
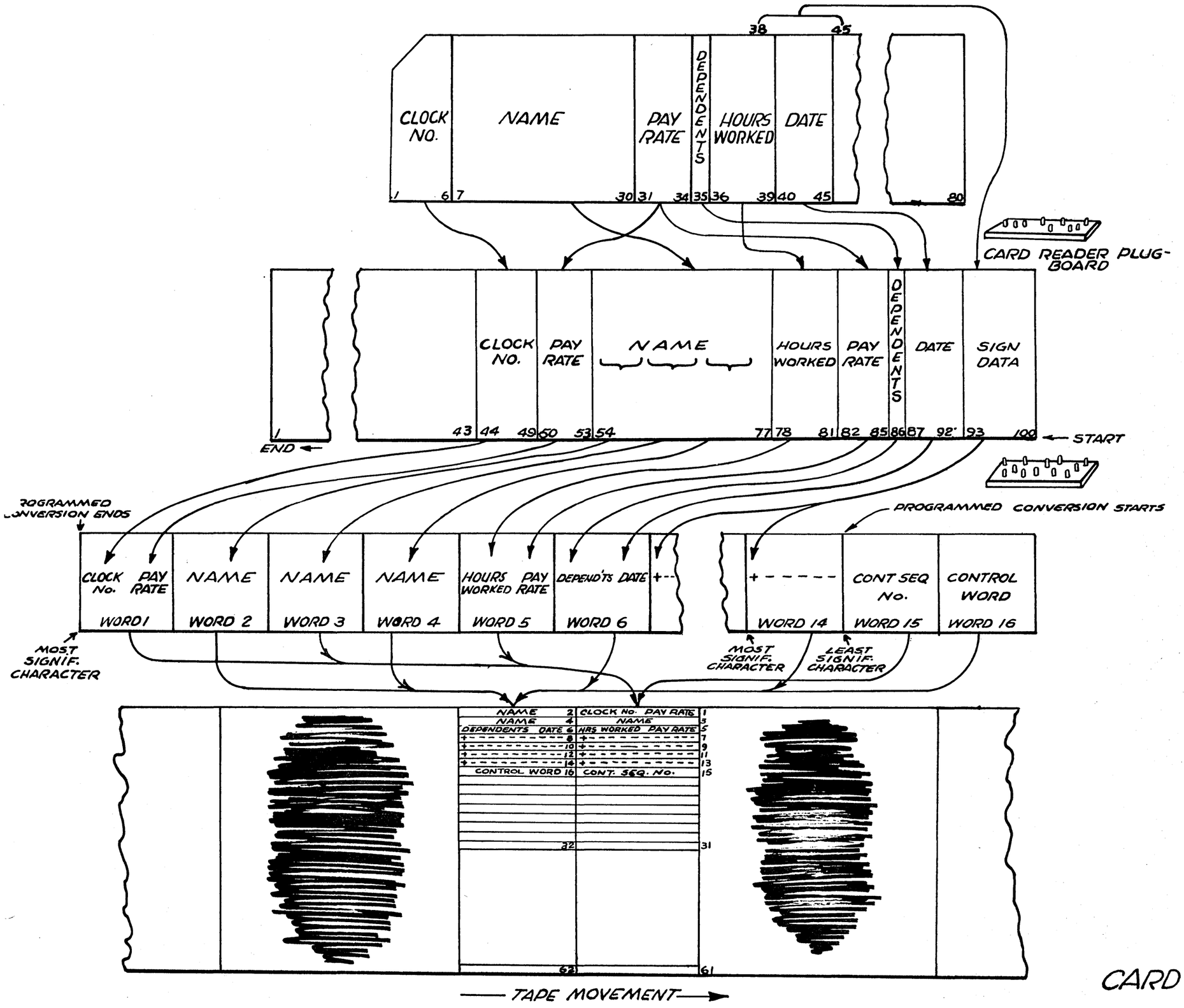


FIGURE 11 TAPE FORMAT



PUNCHED CARD

INPUT MEMORY

OUTPUT MEMORY

MAGNETIC TAPE

FIGURE 12
CARD TO TAPE CONVERSION

Reference to Figure 13. Card Reader Plugboard Work Sheet, indicates that this new sequence of data is achieved by wiring the various card columns to the Input Memory as follows:

Information	Card Columns	Input Memory
Clock Number	1 - 6	43 - 48
Name	7 - 30	53 - 76
Pay Rate	31 - 34	49 - 52 81 - 84
Dependents	35	85
Hours Worked	36 - 39	77 - 80
Date	40 - 45	86 - 92
Sign	38 - 45	83 - 100

2. Wiring the Category Plugboard

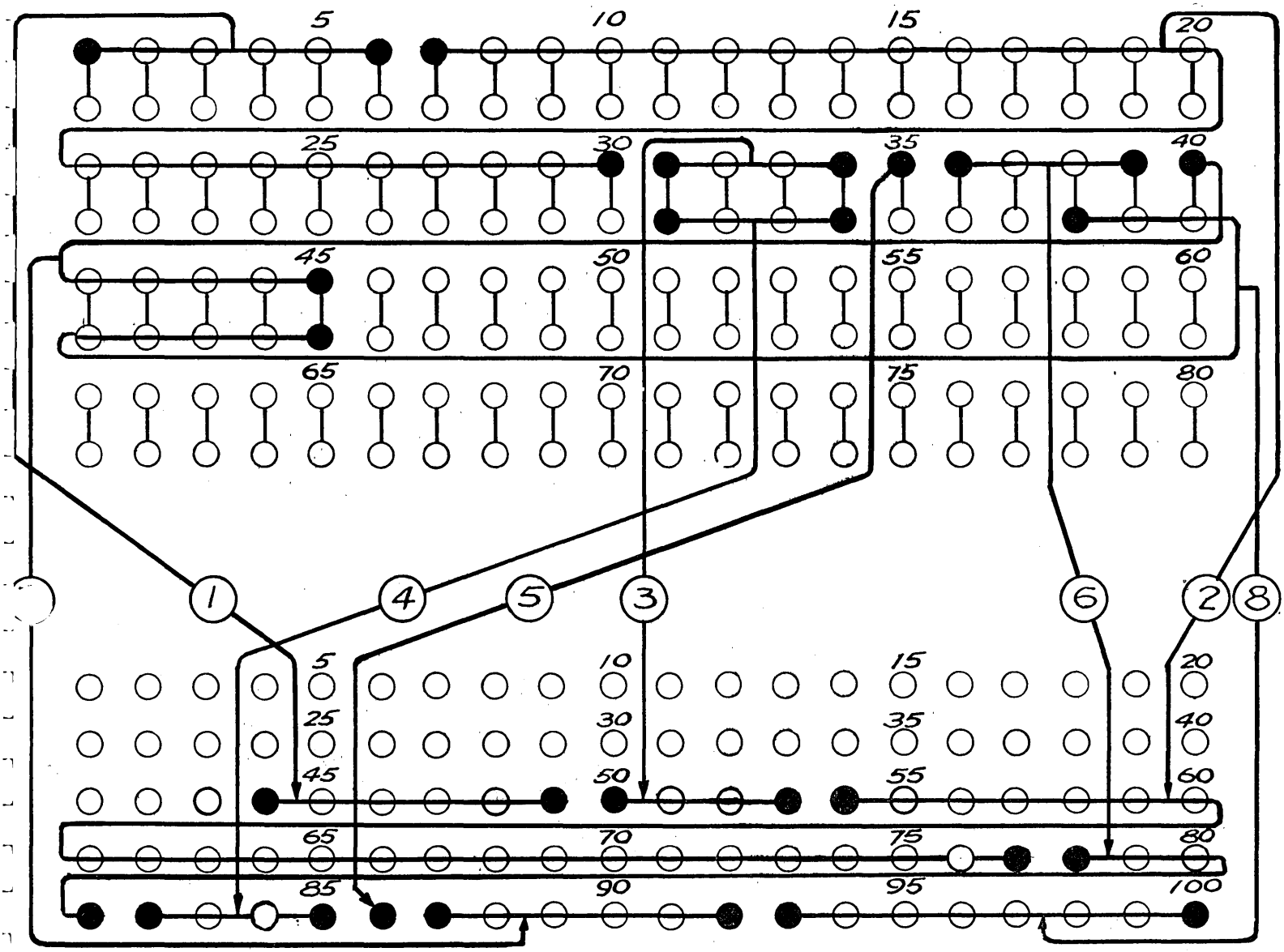
The various items to be written on tape are in the Input Memory in the sequence required to achieve the desired tape format. It is now necessary to convert this data according to the rules of conversion that are listed in Table 1. In addition, certain fillers must be introduced as required between various items in order to position the data on tape. The Input Converter Category Plugboard is used for these purposes. Sequentially the Input Memory positions are encoded in accordance with the rules specified on Figure 14, Input Converter Program Plugging Work Sheet. Each step, as pointed out previously, represents either one converted column from the Input Memory or the insertion of one filler. As noted above, several columns have been duplicated for sign conversion purposes. They are employed here to insure that each word not having data in it during the conversion process will have a positive sign in its high order position, thus eliminating the possibility that the word would be incorrectly sensed as a sentinel. This work sheet specifies the following sequential categories as necessary to arrive at a final storage of correctly positioned data:

Description	Conversion Steps	Rule of Conversion
Word 14	1 - 5	Start E, E, E, D, 8
Word 13	6 - 10	E, E, E, D, 8
Word 12	11 - 15	E, E, E, D, 8
Word 11	16 - 20	E, E, E, D, 8
Word 10	21 - 25	E, E, E, D, 8
Word 9	26 - 30	E, E, E, D, 8
Word 8	31 - 35	E, E, E, D, 8

Input Converter
Card Reader Plugboard

Program _____ Date _____

Programmer _____



(1) CLOCK NUMBER

(2) NAME

(3)(4) PAY RATE

(5) DEPENDENTS

(6) HOURS WORKED

(7) DATE

(8) SIGN DATA

FIGURE 13
WORK SHEET

Input Converter

Program _____ Date _____

Programmer _____

	10	9	8	7	6	5	4	3	2	1	
10	8	0	E	E	E	8	D	E	E	E	
20	8	D	E	E	E	8	D	E	E	E	11
30	8	D	E	E	E	8	D	E	E	E	21
40	8	D	E	E	E	8	D	E	E	E	31
50	E	4	D	E	4	4	4	4	4	4	41
60	3	4	4	4	4	4	4	4	4	B	51
70	3	3	3	3	3	3	3	3	3	3	61
80	3	3	3	3	3	3	3	3	3	3	71
90	4	4	4	4	4	4	D	3	3	3	81
100						Ep	4	4	4	4	91
110											101
120											111
130											121
140											131
150											141
160											151
170											161
180											171

NOTES:

E - 12 ZERO BIT FILLER

D - 8 ZERO BIT FILLER

B - 4 ZERO BIT FILLER

3 - ALPHANUMERIC WITH BLANK COLUMN PERMITTED

4 - NUMERIC WITH BLANK COLUMN DETECTION

8 - SIGN RX WITH BLANK COLUMN PERMITTED

Ep - END OF PROGRAM

1 - END OF WORD

FIGURE 14
PROGRAM PLUGGING WORK SHEET

Description	Conversion Steps	Rule of Conversion
Word 7	36 - 40	E, E, E, D, 8
Word 6		
Date	41 - 46	4, 4, 4, 4, 4, 4
Filler	47 - 48	E, D
Dependents	49	4
Word 5		
Filler	50 - 51	E, B
Pay Rate	52 - 55	4, 4, 4, 4
Hours Worked	56 - 59	4, 4, 4, 4
Word 4		
Name	60 - 67	3, 3, 3, ...3
Word 3		
Name	68 - 75	3, 3, 3, ...3
Word 2		
Name	76 - 83	3, 3, 3, ...3
Word 1		
Filler	84	D
Pay Rate	85 - 88	4, 4, 4, 4
Clock Number	89 - 94	4, 4, 4, 4, 4, 4
End of Program	95	End of Program

Adherence to the rules specified on this worksheet results in the Category Plugboard wired as shown in Figure 15.

The Category Plugboard is now wired to fill the first 14 word locations in the Output Memory. Words 15 and 16, the Continuous Sequence Number and the Control Word, respectively, are automatically inserted to complete the process of card conversion.

After the various steps specified by the Category Plugboard are performed, the first of a pair of records is automatically written on words 1 - 16 of the tape block. The tape then returns to its original position and, when the 2nd record has been processed through the Category Plugboard, it is written on words 17 - 32 of this same block. The tape then advances to the next block preparatory to processing the next pair of input records.

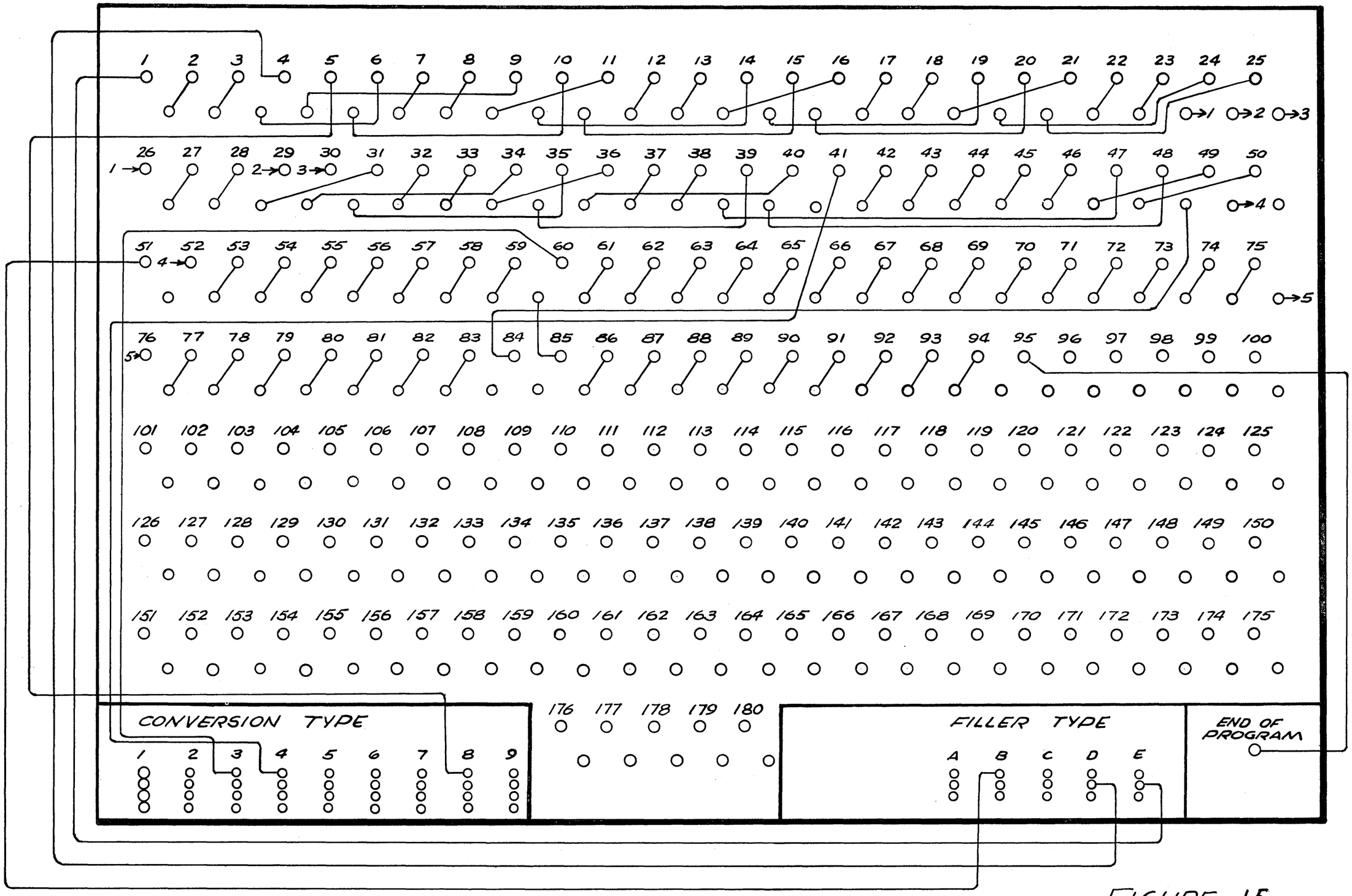


FIGURE 15
INPUT CONVERTER CATEGORY
PLUGBOARD

Central Processor Considerations

The first time the tape containing converted records is introduced into the Central Processor it is mandatory that an inspection be made on each record converted to insure that it is valid for use in processing, i. e., contains neither illegal punches nor converter errors. As pointed out previously, the 16th word is used for this purpose. The Sentinel Register of the Central Processor permits this word to be isolated so that it may be inspected and interpreted. The sentinel isolating features of the Sentinel Register become valuable when it is remembered that this Register stores the first sentinel word sensed if one or more exist during a transfer from Input Buffer to the High Speed Memory. In addition, the next word to be transferred in is similarly sensed. Thus, the presence of a sentinel in the Sentinel Register may be due to (1) the presence of one or more sentinels in the converted information; (2) the presence of one in the 16th word; or, (3) the presence of one in the next word to be transferred in.

The three conditions described present no problem if the possibility of their existence is kept in mind. Thus, the first condition could be handled, as indicated in the example problem given above, by wiring the two plugboards on the Input Converter to insure that none of the 1 - 14 words can be sentinels.

A more generalized solution to this problem would be to handle each block of information (2 records) such that:

(1) fifteen words are transferred in, then
(2) one word is transferred in.
(3) fourteen words are transferred, then
(4) one word is transferred in

Steps (1) and (2) permit the first record on the block to be treated and (3) and (4) permit the second one to be treated. Thus, a comparison of the 16th word with the contents of the Sentinel Register after step (2) serves to identify this 16th word as a sentinel.

Steps (3) and (4) permit the second record to be handled. Since the 15th word contains the Continuous Sequence Number, one can insure that it is not a sentinel. Hence, a sentinel can exist in the Sentinel Register after step (4) only if the next word that is to be transferred in (the 16th word) is a sentinel.

TABLE 1

Methods of Conversion

Method	Description
1. Transcription	The twelve positions of a card column are considered to be a 12 bit number with 9 the high order bit and R the low order bit. A punch in any position creates a binary one in that position of the 12 bit number which is recorded on tape.
2. Alphanumeric with Blank Column Detection	Each card column of data in the Input Memory creates 6 bits on tape. A blank is considered an illegal punch.
3. Alphanumeric with Blank Column Permitted	Same as 2 except that a blank column in the card is legal (considered valid).
4. Numeric with Blank Column Detection	Each card column of data in the Input Memory creates 4 bits on tape. The conversion applies only to positions 0 - 9 of the card column. The R and X rows are not sensed. A blank is considered an illegal punch.
5. Numeric with Blank Column Permitted	Same as 4 except that a blank column in the card is legal (considered valid).
6. Hexadecimal with Blank Column Detection	Each card column in Input Memory creates 4 bits on tape. The X row is not sensed. A blank column is considered an illegal punch.
7. Sign XR With Blank Column Permitted	Each card column in Input Memory creates 4 bits on tape. A blank column in the card is legal (considered valid).
8. Sign RX with Blank Column Permitted	Same as 7 above except that the meaning of the R and X punches has been interchanged.
9. Months with Blank Column Detection	Each card column in Input Memory creates 8 bits on tape. A blank column is considered an illegal punch.

TABLE 2

Maximum Number of Conversions per Hub

Method	Maximum Number of Conversions
1. Transcription	30
2. Alphanumeric with Blank Column Detection	30
3. Alphanumeric with Blank Column Permitted	30
4. Numeric with Blank Column Detection	30
5. Numeric with Blank Column Permitted	30
6. Hexadecimal with Blank Column Detection	30
7. Sign XR with Blank Column Permitted	30
8. Sign RX with Blank Column Permitted	30
9. Months with Blank Column Detection	30

TABLE 3

Fillers

Types	Maximum Number of Fillers Per Hub
A. Two Zero Bit Filler	30
B. Four Zero Bit Filler	30
C. Six Zero Bit Filler	30
D. Eight Zero Bit Filler	30
E. Twelve Zero Bit Filler	30

TABLE 4

Control Word

Conversion Status	Sign	O P	A	B	C	W. C.
Legal	0100	Zeros	(See "Run" Designator)	Zeros	Zeros	0100
Illegal Punch	0001	Zeros	"	Zeros	983	0011
Converter Error	0000	Zeros	"	Zeros	Zeros	Zeros

Run Designator

Run Number	"A" Address		(low order)
1	1000	0000	0001
2	0111	0000	0010
3	0110	0000	0011
4	0101	0000	0100
5	0100	0000	0101
6	0011	0000	0110
7	0010	0000	0111
8	0001	0000	1000
9	0000	0000	1001
10	1000	0001	0000
11	0111	0001	0001
12	0110	0001	0010
13	0101	0001	0011
14	0100	0001	0100
15	0011	0001	0101
16	0010	0001	0110
17	0001	0001	0111
18	0000	0001	1000
19	1000	0001	1001
20	0111	0010	0000

TABLE 5

CATEGORY	CARD PUNCHES				TAPE CODE	
	R X O	1 2 3	4 5 6	7 8 9		
Transcription	R X O	1 2 3	4 5 6	7 8 9	987654	321OXR
Alphanumeric (blank=error)	1					000000
		1				000001
		1				000010
		1				000011
			1			000100
			1			000101
			1			000110
				1		000111
				1		001000
				1		001001
		1		1		001011
			1	1		001100
1						110000
1		1				010001
1		1				010010
1		1				010011
1			1			010100
1			1			010101
1			1			010110
1				1		010111
1				1		011000
1				1		011001
1		1		1		011011
1			1	1		011100
1						100000
1	1					100001
1	1					100010
1	1					100011
1			1			100100
1			1			100101
1			1			100110
1				1		100111
1				1		101000
1				1		101001
1		1		1		101011
1			1	1		101100
1	1					110001
1	1					110010
1	1					110011
1			1			110100
1			1			110101
1			1			110110
1				1		110111
1				1		111000
1				1		111001
1		1		1		111011
1			1	1		111100

TABLE 5 (Cont.)

CATEGORY	CARD PUNCHES				TAPE CODE
	R X O	1 2 3	4 5 6	7 8 9	
Alphanumeric (blank=legal) same as alphanumeric above except for blank code					010000
Hexadecimal-blank column illegal	1 (NOT SENSED)	1			0000
		1			0001
		1			0010
			1		0011
					0100
	(SENSED)		1		0101
			1		0110
				1	0111
				1	1000
				1	1001
1 (SENSED)		1			1010
1		1			1011
1			1		1100
1			1		1101
1			1		1110
1				1	1111
Numeric-blank column illegal	(NOT SENSED) 1	1			0000
		1			0001
		1			0010
			1		0011
					0100
	(SENSED)		1		0101
			1		0110
				1	0111
				1	1000
				1	1001
Numeric-blank column legal same as numeric above except for blank code					0000
Sign XR	1	NOT SENSED			1101
	1				1101
					0101
Sign RX	1	NOT SENSED			1101
	1				0101
					1101

TABLE 5 (Cont.)

CATEGORY	CARD PUNCHES				TAPE CODE	
	R X O	1 2 3	4 5 6	7 8 9		
Months		1			00	000001
		1			00	000010
		1			00	000011
			1		00	000100
			1		00	000101
			1		00	000110
				1	00	000111
				1	00	001000
				1	00	001001
	1				00	010000
	1				00	010001
	1				00	010010

THE DATAmatic OUTPUT CONVERTER TYPE 1300

Introduction

The purpose of the DATAmatic Output Converter Type 1300 is to accept information recorded on DATAmatic Magnetic Tape and generate suitable electrical signals to permit the printing or punching of this information by specific equipment. The DATAmatic Output Converter produces the electrical equivalent of a punched card having 120 columns. It may be converted to an IBM Type 407 Tabulator, or to an IBM Type 519 Card Punch.

The operation of the Output Converter may be explained by means of the Block Diagram, Figure 16. Information is read from tape into the conversion input storage, whose capacity is 15 words. It is read into Converter Output Storage through a code translator, controlled by a program plugboard. The Output Storage is designed to simulate a punched card of 120 columns, with 12 binary positions per column, in which information is stored in punched card (Hollerith) Code. To effect this, the Output Storage is wired permanently to 120 reading hubs on the 407 plugboard, in such a way that readings from the simulated (120 column) punched cards have the same pulse sequence and timing as a card read at second reading.

When information is prepared for printing, it must be stored on a DATAmatic Tape in conversion groups of 16 words each, occupying words 1 - 16 or words 17 - 32 of a tape block. The 16th word of each conversion group is an acceptance word and must be a 12-digit number consisting of decimal zeros (0000) or fives (0101). Corresponding to each of the 12 decimal digit positions, there is an acceptance switch on the converter. If any digit position of the acceptance word has a decimal "five" whose corresponding acceptance switch is "on", the first 15 words of the conversion group will be accepted for output conversion. Unless the 407 is in the MLR mode of operation, a single line of printing will result. Otherwise, the entire conversion group is rejected without printing or spacing, and the next conversion group is read from tape.

The conversion from input storage to output storage occurs in steps, of which a maximum of 240 may be wired on the converter plugboard. Each step extracts a specified number of bits and rejects them or converts them to a colum of punched card (Hollerith) code in output storage. The number of bits is specified by the wiring of the step. Successive steps in the conversion program select bits sequentially from input storage and insert characters sequentially into output storage. The sequence of selection from input storage begins with the lowest order bit of word 15 of the conversion group and proceeds towards the high order of word 15, then to the low order of word 14, and so on through word 1. The sequence of insertion into output storage begins with column 120 of the simulated punch card and proceeds towards column 1.

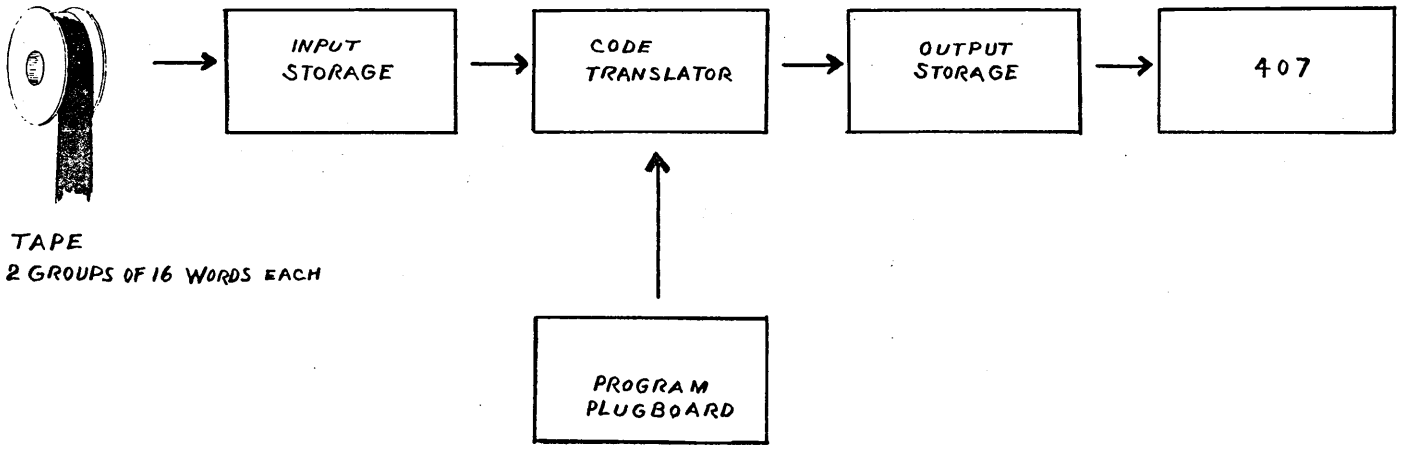


Figure 16. DATAmatic Output Converter Type 1300 Block Diagram.

Wiring for Conversion, Without Use of Special Controls

Each step in the conversion must result in the execution of one of the eleven conversion rules listed in Table 6. Rule selection is effected by means of plugboard wiring. There are two sets of "Rules" plughubs on the Output Converter Program Plugboard shown in Figure 21. Those on the left side of the plugboard are for use with steps 1 - 120, those on the right side are for use with steps 121-240.

Step 1 must be wired to the appropriate rule plughub. Whenever a step repeats the rule used by the preceding step, it must be wired to a T-hub. T-hubs, like rule hubs, appear on the left side of the plugboard for use with steps 1-120, and on the right side for use with steps 121-240. When successive steps use the same rule, only the first is wired to the rule hub: the others are wired to the repeat hub.

In planning the conversion plugging, it is necessary to keep track of the number of bits extracted from input storage. Whenever a word is exhausted, the next step must be wired to Rule 9 (end-of-word), except that Rule 10 is used at the end of word 9, and Rule 11 is used at the end of word 1. The next following step must not be wired to a T-hub.

The full 15 words must be wired. If fewer than 15 words are to be converted, enough steps must be wired to rejection rules and end-of-word rules to account for a total of 15.

As an example we may consider the problem of preparing the dividend checks shown in Figure 17. The information necessary for preparing a check may be stored in sixteen words, comprising one conversion group; and two conversion groups may be stored on a tape block, as in Figure 18. The tape format of the conversion group corresponding to the first check of Figure 17 is shown in Figure 19. The correpondence between the characters of the conversion group and the conversion rules is shown in Figure 20. The corresponding plugging, shown in Figures 21a and 21b, lends to the output storage array shown in Figure 22a. It may be seen that, in this example, columns 1 through 59 of the simulated punched card are not used. Such features as column switching and column duplication may be obtained readily by suitably wiring the output storage plughubs to the print entry plughubs on the 407 plugboard.

Table 6

Output Converter Type 1300 Conversion Rules

1. Six bit alphabetic

   Six bits are read from input memory and converted to an alphanumeric character.

2. Four bit hexadecimal

   Four bits are read from input memory and converted to a number 0-9 or a symbolic letter B-G.

3. Four bit sign

   Four bits are read from input memory and converted to sign information. Associated with this mode is a three position "sign switch" on the Converter. One of three types of sign conversion can be selected to apply when a sign mode of conversion is specified by the program plugboard.

4. One bit transcription

   One bit is read from memory and converted as a 1 or 0.

5. Six bit month

   Six bits are read from input memory and converted to one of the 12 monthly designations.

6. One bit reject

   One bit is read from input memory and discarded.

7. Four bit reject

   Four bits are read from input memory and discarded.

8. Six bit reject

   Six bits are read from input memory and discarded.

9. End of word

   The four bits of the weight count are read to the converter's check circuits, but are discarded as far as the output is concerned.

10. End of First half

    Same as 9, except that this rule must be used instead of rule 9 at the end of word 9.

11. End of Second half

    This is used instead of rule 9 at the end of word 1.

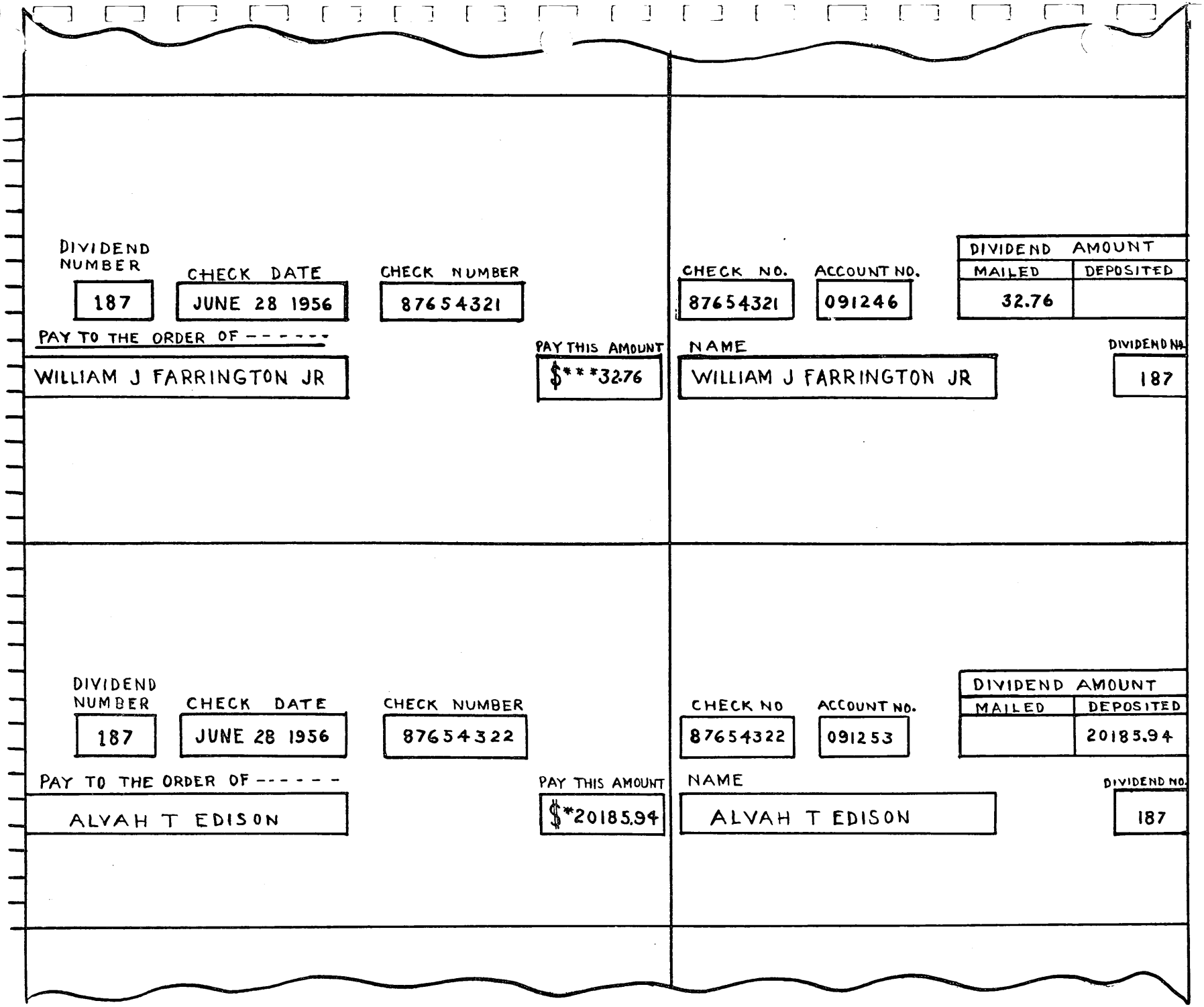


Figure 17. Typical Dividend Checks.

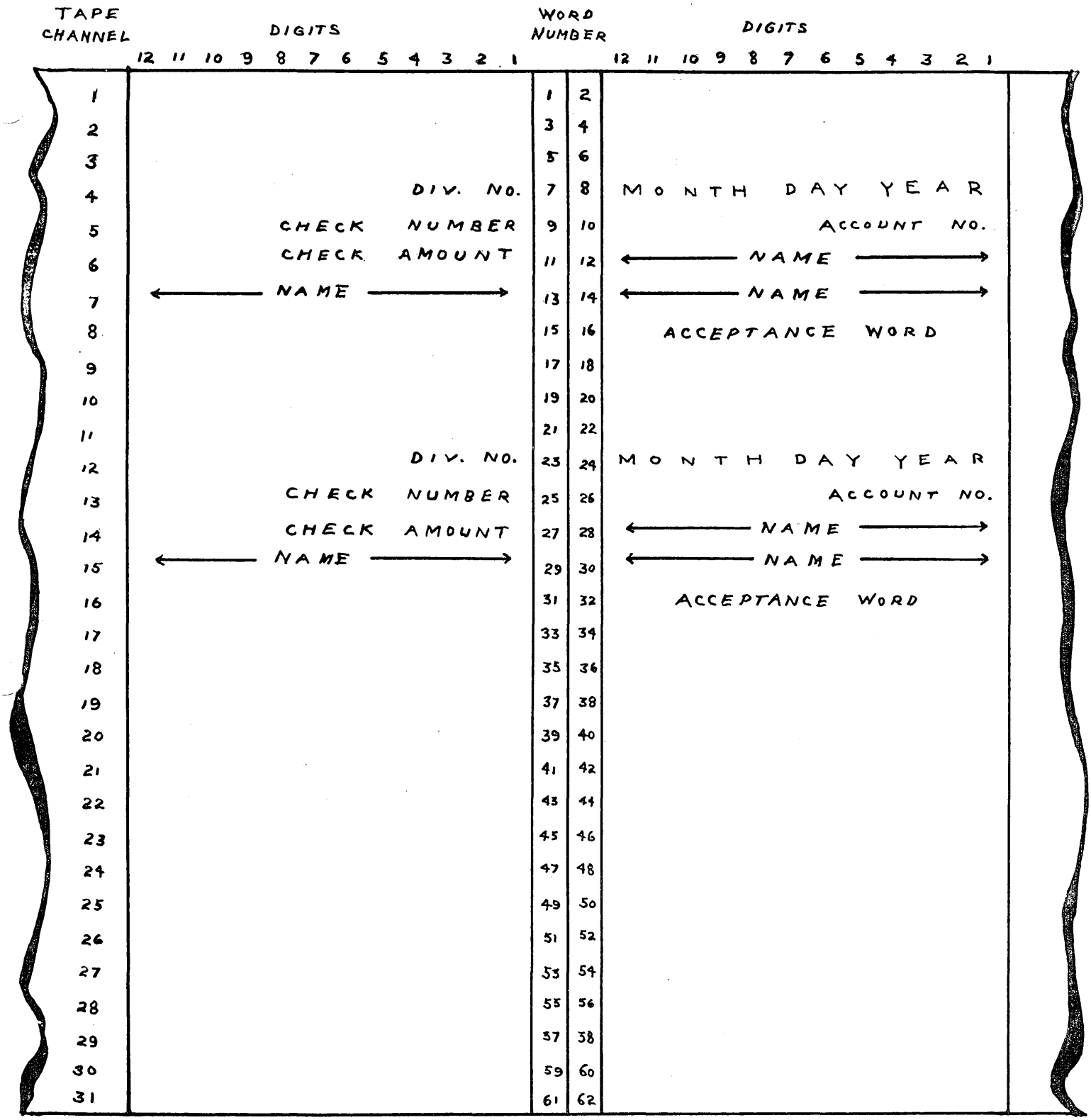


Figure 18. Tape Format for Typical Dividend Checks.

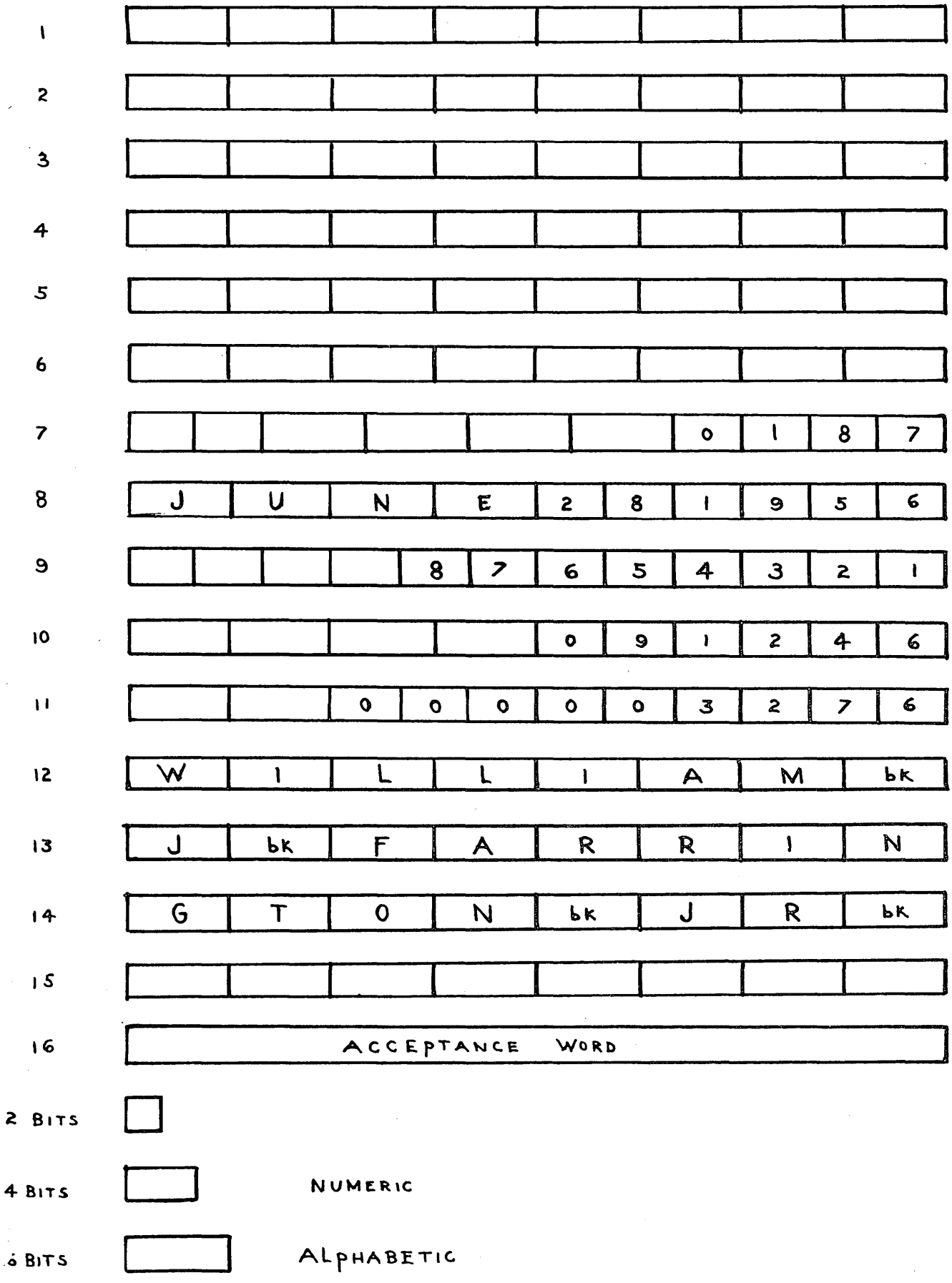


Figure 19. Format of One Dividend Check Conversion G roup of Figure 18.

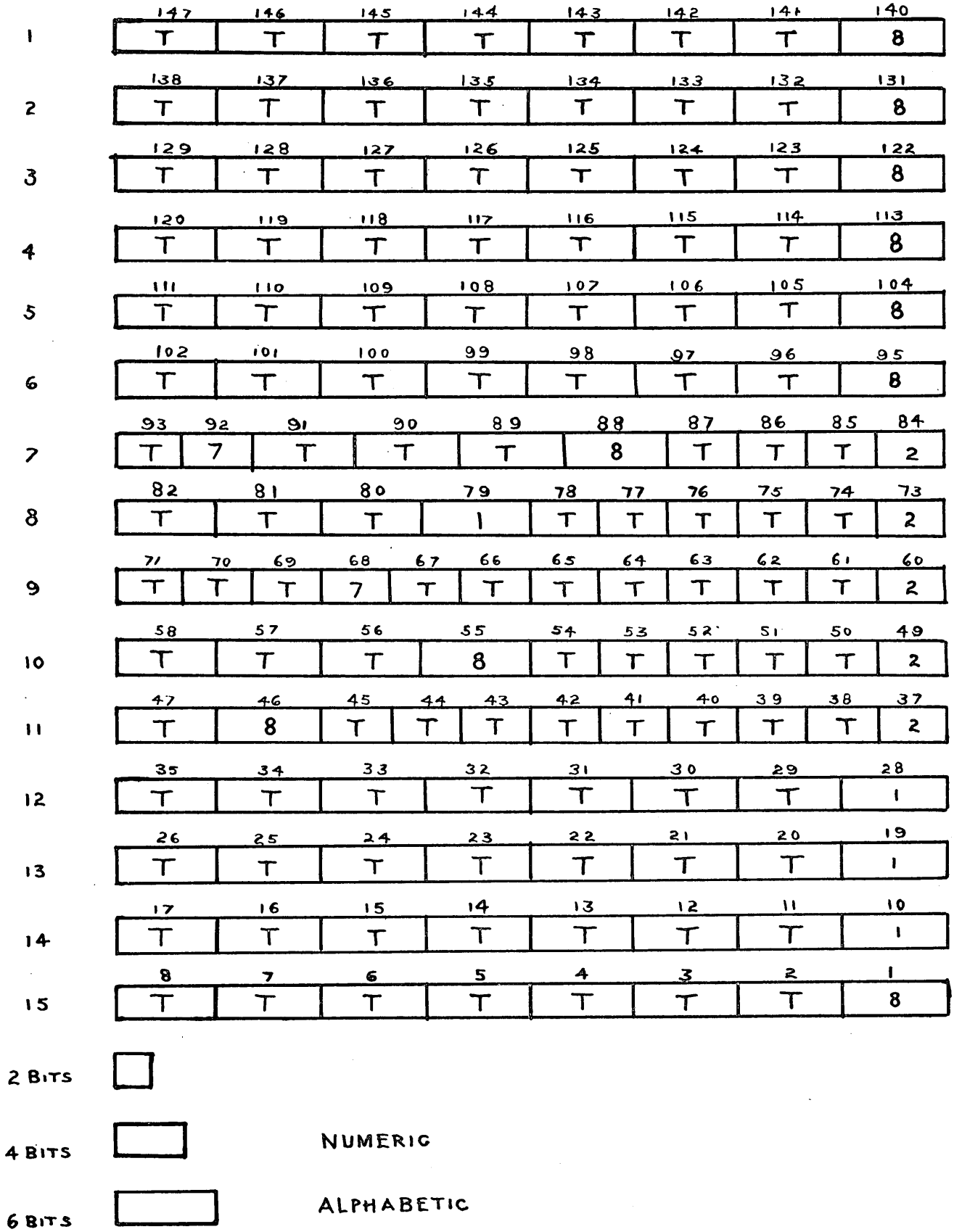


Figure 20. Allocation of Conversion Rules.

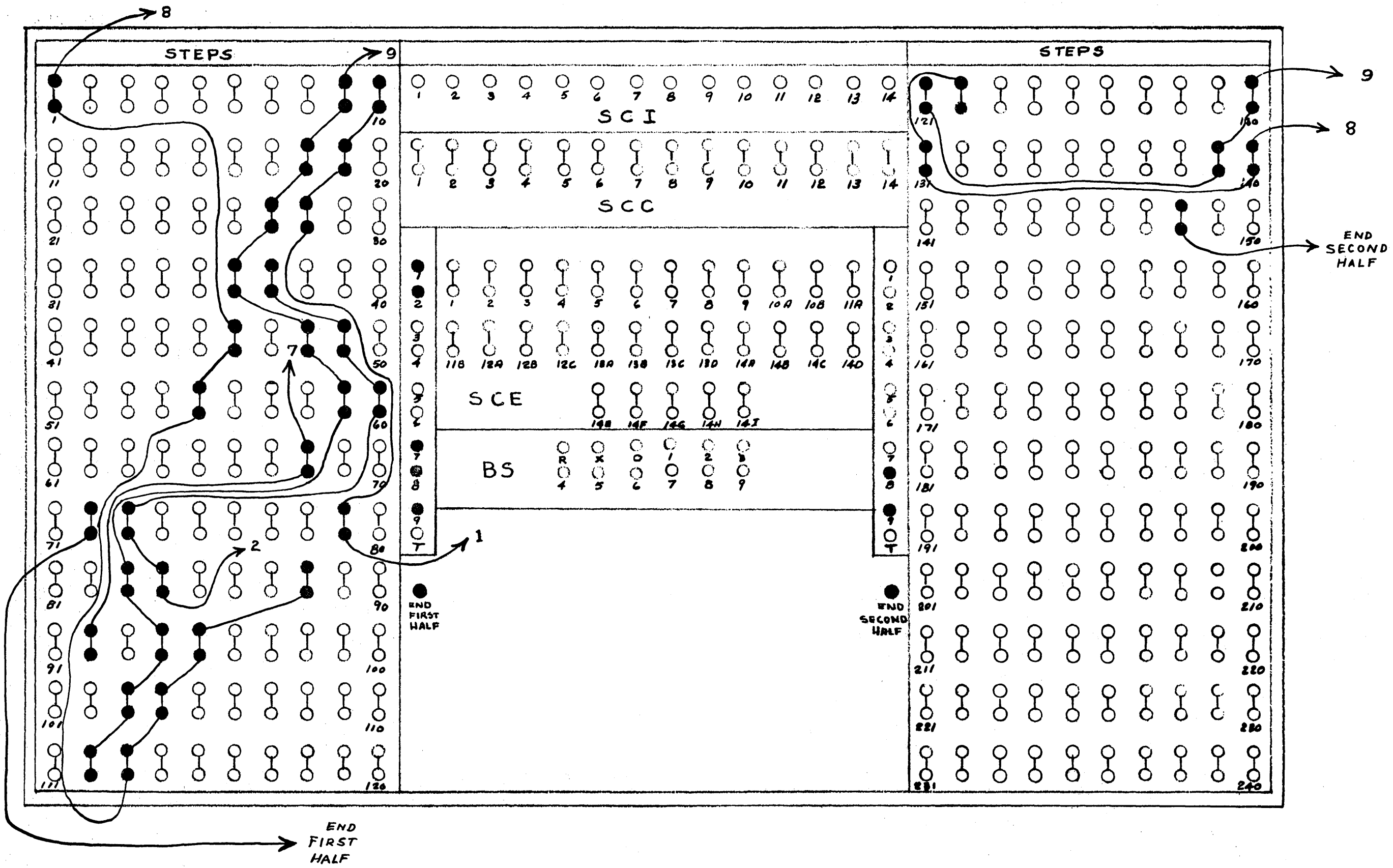


FIGURE 21 a

PROGRAM PLUGBOARD—OUTPUT CONVERTER

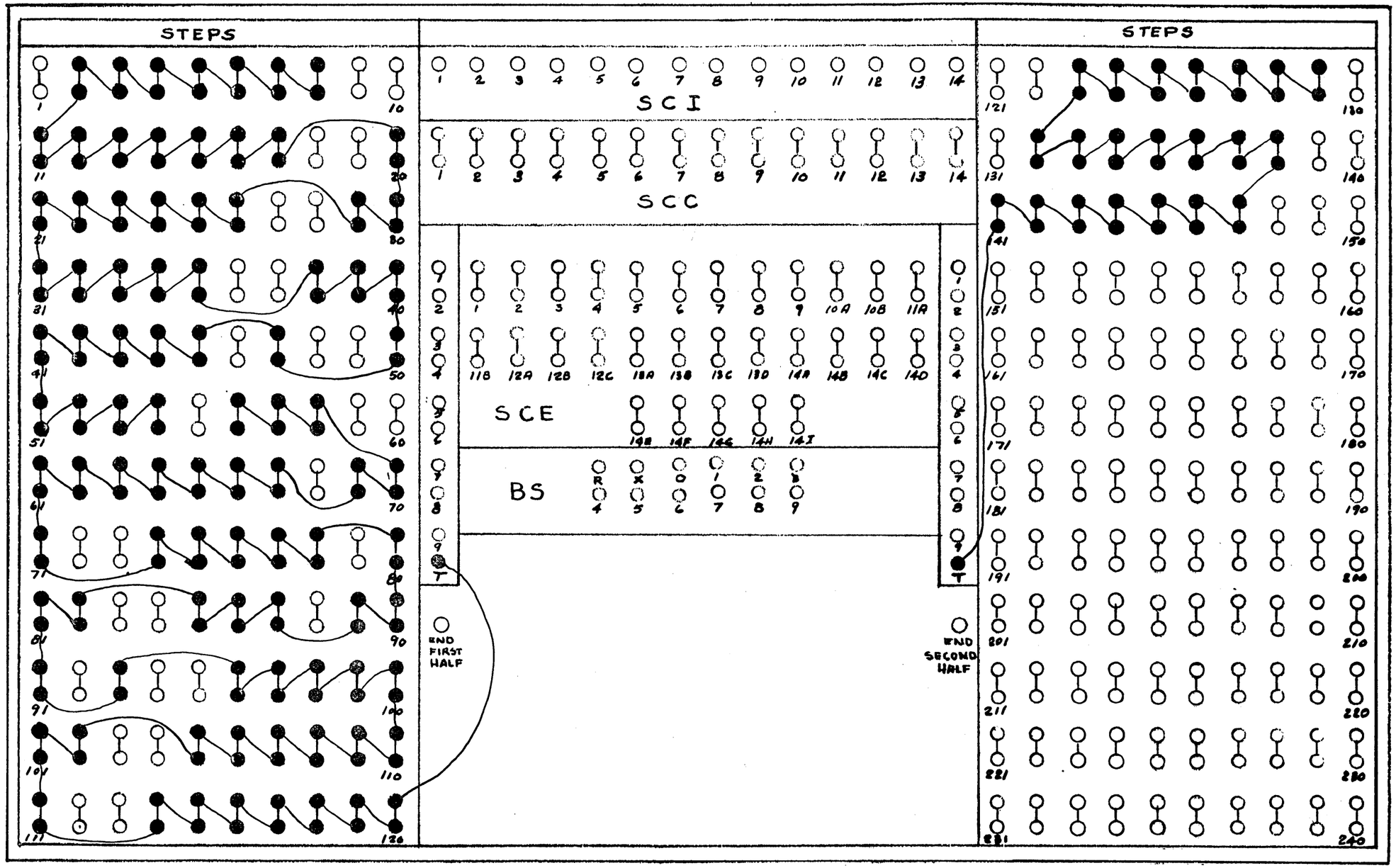
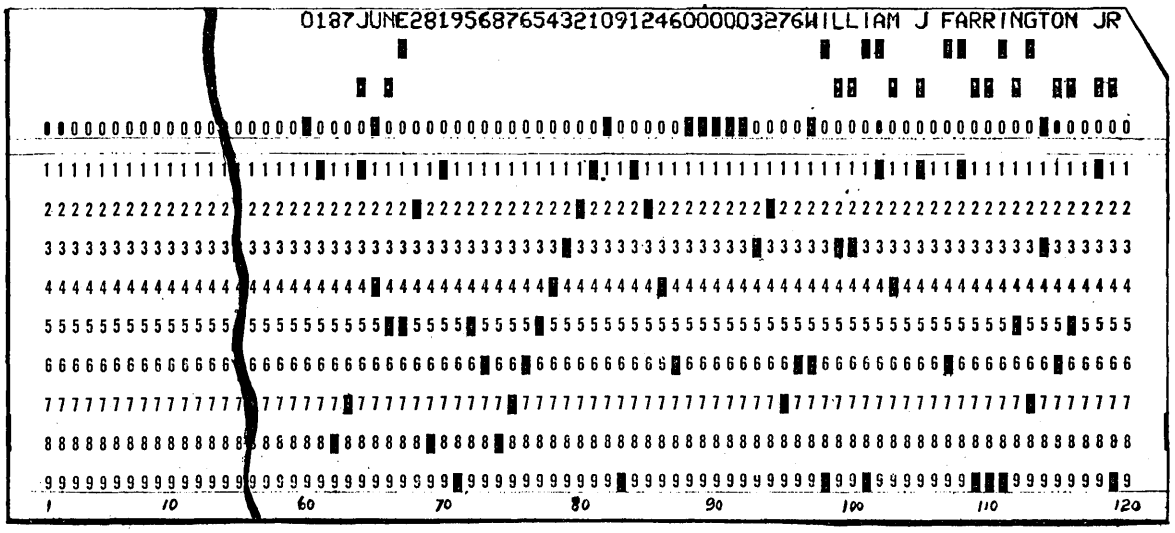
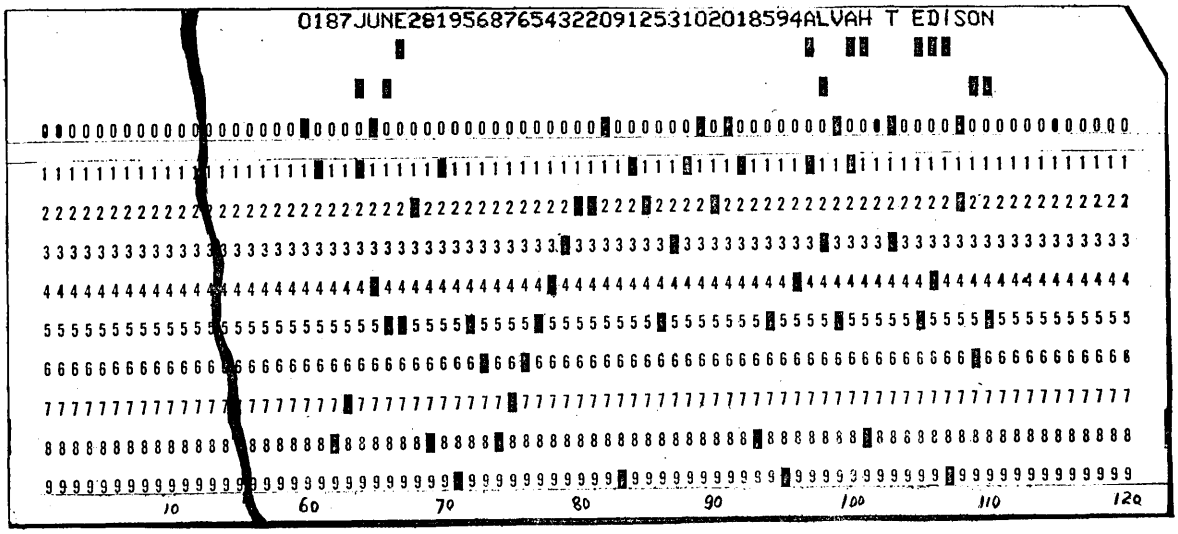


FIGURE 21b

PROGRAM PLUGBOARD—OUTPUT CONVERTER



(a)



(b)

Figure 22. Output Storage Array Showing Simulated 120 Column Card.

Wiring for Special Functions

The Bit Selection Function provides a means of controlling the 407 on the basis of specified bits in a column of the simulated punched card. For use with the DATA Output Converter Type 1300, the 407 plugboard has been modified to include Bit Selection exit hubs. There are 14 Early and 14 matching Late Exits for Bit Selection. On the converter plugboard, there are 12 Bit Selection (BS) entry plughubs, labelled for the 12 punching positions of a column of Hollerith Code. The entry hubs are wired via Special Control Distributors to steps in the conversion program; they serve to specify output storage columns to be examined for Bit Selection.

On the converter plugboard appear several plughubs associated with each Special Control Distributor. They are a single input hub SCI, a pair of coupler hubs SCC, and one or more exit hubs SCE. There are 14 such distributors, and each plughub is labelled with the associated distributor number. If a step of the conversion program is to be wired to a Bit Selection, the step hub is wired to the SCI hub of an available Special Control Distributor, and the SCE hub of the same distributor is wired to the desired function - one of the 12 BS hubs. Each step wired to a Bit Selection must also be wired to execute one of the conversion rules (Rules 1-6). This is accomplished by wiring from a SCC hub of the Special Control Distributor to the rule, or to a T-hub.

Only one step hub may be wired to an SCI hub. If additional steps are to be used with a rule wired from an SCC hub, they may be wired via the coupled SCC hub, either directly from the step hub, or via another SCC hub. Likewise, only one Bit Selection hub may be wired to an SCE hub, but several Bit Selections may be impulsed from one program step by using a Special Control Distributor with an adequate number of SCE hubs. Any number of steps may be wired to a single Bit Selection hub, using the coupled SCE hubs.

For an example of the use of Bit Selection consider again the preparation of the dividend checks shown in Figure 17. These checks differ slightly in format, the difference depending upon whether the dividend is to be mailed or deposited. In the conversion group this distinction can be made by means of a code digit, stored as the ninth character of word 11 (corresponding to step 45). Let this be a 0 for a dividend to be mailed, a 1 for a dividend to be deposited. The wiring can be changed to sense for a 1 in this character. In fact, that portion of the wiring shown in Figure 21a may be retained without change, and the wiring of Figure 21b is modified to the form of Figure 23. The modified wiring will convert the tape information to output storage arrays like the ones shown in Figures 22a and 22b, and in addition will signal the presence of a 1 in column 88. By appropriate wiring of the converter plugboard, this signal may be utilized to shift the printing of the dividend amount on the check stub to the column reserved for dividends to be deposited.

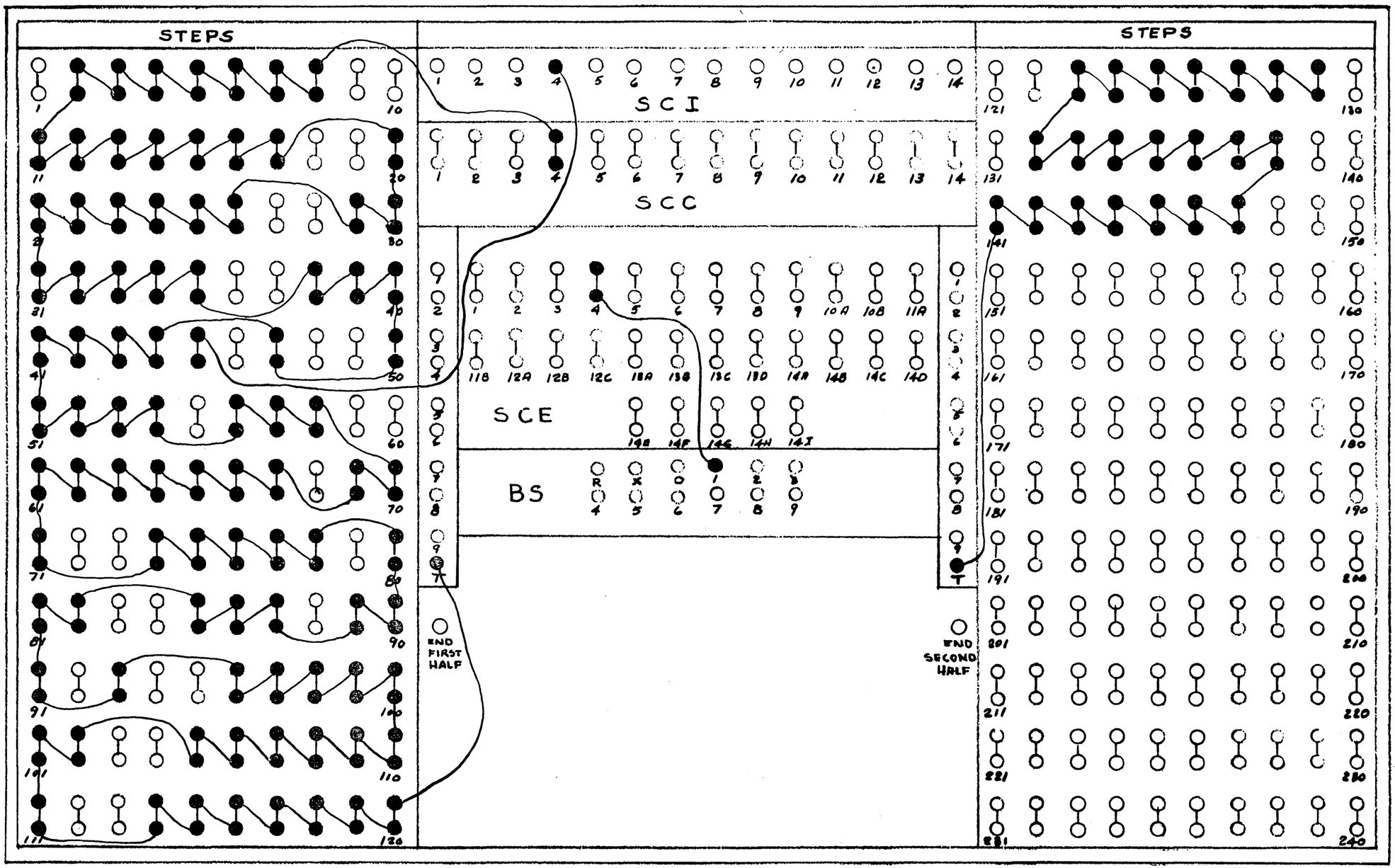


FIGURE 23

PROGRAM PLUGBOARD—OUTPUT CONVERTER

Bit Selection is performed on characters in output storage; that is, on columns of a simulated punched card. The step creating the character upon which Bit Selection is performed is wired to the appropriate BS hubs via Special Control Distributor. The presence of a binary one in a bit so specified will be signalled by impulses delivered at the Late and Early Bit Selection exit hubs on the modified plugboard used with the 407. There are ten pairs of exit hubs from which the impulses may appear, numbered from 0 through 9. The number n of the hubs at which the impulses appear is determined by the order in which the BS impulses are activated by the steps: the first appears at plughub 1, the second at plughub 2, et cetera. In counting, it must be noted that a BS impulse triggered by a lower numbered step precedes one due to a higher numbered step. In determining the order between BS impulses triggered by the same step, the succession goes from high to low; more precisely, the succession is 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, X, R. The numbers n may be written down readily once a table corresponding to Table 6 has been made up. In the example given, an output impulse due to Bit Selection will appear at the BS exit plughub number 1.

Timing of Special Function Exit Hubs

Impulses from corresponding Early and Late Bit Selection Exit hubs on the 407 plugboard result from identical conditions, but are timed to occur in different operating cycles of the 407. An impulse from a Late Exit hub always occurs if the required condition is satisfied, and is timed from 325° to 185° of the cycle in which the controlling conversion group is read from output storage to the 407. The timing of impulses from the Early hubs depends in part on the location in the conversion program of the steps creating the controlling conditions. On each step wired to a rejection rule one timing point is expended; on each other step two timing points are expended. If the condition resulting in an exit impulse occurs within 145 points of the beginning of the conversion program, the Early Exit impulse will occur from 200° to 270° of the cycle preceding the transfer to the 407 of the controlling conversion group. If the step occurs later than 145 points of the program, the end of the impulse still occurs at 270°, but the beginning is determined by the formula:

$$\text{Number of degrees} = 184 + 0.108 \text{ (number of points)}$$

The longest possible program contains 120 conversion rules, 15 end-of-word rules, and 105 rejection rules, to make a total of 240 steps. This program contains 375 points, and ends at 225° of the 407 cycle. Thus, the latest time at which an Early Exit impulse may begin is 225°.

Pilot selectors picked up by early impulses wired to the D-pickups of the selectors will be transferred during the cycle in which the controlling conversion group is read to the 407. The X-pickups may not be used with the converter, as they are not connected. A pilot selector picked up from a Late hub will be transferred for the subsequent reading cycle. Co-Selectors drop out at 285^{o} of the cycle in which they are picked up; consequently, co-selectors should be picked up through pilot selectors or from Late Exit hubs if they are to be transferred while the controlling conversion group is being read to the 407. By virtue of the modifications made to the 407, MLR Start may be impulsed from an Early or Late Exit hub, and the controlling conversion group will be treated as an MLR card. MLR Stop should be impulsed in the normal manner from the output storage exit hubs (corresponding to the normal wiring of MLR Stop from Second Reading). Programs, counters, carriage controls, et cetera, may be used normally within the limitations imposed by the timing of the Special Function exits. If a condition is controlled by a program step later than 148 points of the program, the Early Exit hub should not be heavily loaded, in order to avoid damage to the relay contacts.

ADDRESSES OF SIGNIFICANCE

Of the 2000 addresses in the DATAmatic 1000, ten are special addresses which contain special words for control purposes. Of the remaining 1990 addresses seven of them (1983-1989) are usually reserved for control purposes and may be selected automatically as order sources under certain circumstances. For example, when the end of tape is reached, the sequence of operation is interrupted, and an automatic subsequence call is made to location 1989. The programmer should have anticipated this situation and stored an order initiating an end of tape routine in location 1989.

Similarly, orders initiating the division over capacity routine or addition or subtraction overflow routines may be stored in 1986 and 1988, respectively. If the console rerun switch is on, errors in the transmittal of data from the Input Buffer to the Manipulative Section will cause a subsequence call to 1987 where the proper error detection routine may be initiated. As mentioned previously, the Input Buffer automatically inserts fillers when they are needed. These fillers are sentinel orders which instruct the central system to go to location 1985 for its next order. These fillers may be used for input and output data control. In like fashion a multiple punch present during a card to tape conversion will result in an order instructing the Central Processor to go to location 1983 for its next order.

In summary, the addresses (locations) 1983 through 1989 may be used for the following control purposes:

Address	Possible Control Uses
1983	Multiple punches present during the input conversion process will cause a sentinel order with 1983 as the location of the next address.
1984	Fillers transferred from the output buffer will be sentinel orders with 1984 as the location of the next address.
1985	Fillers transferred from the input buffer will be sentinel orders with 1985 as the location of the next address.
1986	Division over capacity results in a subsequence call to 1986.
1987	If the console "Rerun" switch is on and there is an error in transfer of data, a subsequence call to 1987 is produced.

1988	Addition or subtraction overflow results in a subsequence call to 1988.
1989	Reaching the end of tape results in a subsequence call to 1989.

The address 0000 is also of interest. Except in the case of Comparison orders, an instruction to change the Sequence Register or make a Subsequence Call to memory address 0000 (void address) will be ignored and the Sequence Register will be used in the normal fashion.

Storage addresses 1990 through 1999, located in the Arithmetic and Control units, are special addresses which contain special words used for control purposes. They can be read into and out of by orders.

1990 - Control Register

The Control Register is part of the DATAmatic 1000's control circuitry. It stores each order during the time the order is being performed by the system.

The primary use of this control register in programming is as a C address for order modification purposes. Modifications to an order are usually made by means of an Addition order which adds a constant to the order being modified. Because the Addition order does not provide for a subsequence call, the program would ordinarily continue the current order sequence after an order modification. However, since the control register is addressable, it is possible to modify an addition order and to make an immediate subsequence call. This is accomplished by sending the result of the order modification addition to the Control Register (i.e., the C address of the Add order is 1990). This will result in an automatic subsequence call to 1990, so that the modified order is the next order executed.

The address 1990 may be used as the A, B or C address of an order. Because the address portions of the order word are shifted, end-around, during the execution of an order, the programmer must know the relative positions of the A, B and C addresses of the word in the Control Register, if it is used as a word source.

If 1990 is used as an A address, the order word in the Control Register is in normal (unshifted) form. If 1990 is used as a B address, the address portions of the order word have been shifted so that they are in the sequence BCA, when the actual selection is made. In general, the programmer should not address 1990 without taking special precautions.

1992 - Output Buffer Register

The Output Buffer Register contains the same word as that found in the first word position of the Output Buffer. Thus, when sixty-two words have been sent to the Output Buffer this register (1992) will contain the first word which was transferred. Then, if another word is sent to the Output Buffer, the first word is pushed out and replaced by the second word which was transferred, and so forth. The word in this register is then the same as the first word which will be written on tape by the next tape write order. When the Output Buffer is not full, i.e., contains less than sixty-two words, the Output Buffer Register still contains the word that previously occupied the final word position of the Output Buffer which is the word which was written into the key channel in tape by the previous tape write order.

1993 - Extractor Register

This register contains the constant used for the extraction that is performed in the two Transfer and Select orders. Although this register is used during the execution of several of the arithmetic operations, its contents, prior to the operation, are temporarily stored elsewhere and are then restored after the completion of the operation. It may be used as the A, B or C address of most orders, however it can not be used as address B of the Add, Subtract, Multiply or Substitute orders.

1994 - Selection Register

This register contains one of the operands in the Double Transfer Order. Both Transfer and Select Order are stored in this register after their execution. Four times the multiplicand is stored in this register as a result of the Multiply order and the previous contents are thereby destroyed. This register may be the A, B or C address of all orders, except the Transfer and Select or Multiply orders.

1995 - Remainder Register

This register receives the low order product of a multiplication after it has been modified by rounding. The low order product is made up of the eleven low order decimal digits of the complete product. Rounding is accomplished by adding five to the high order digit of the low order product and allowing any end carry to be added to the low order digit of the high order product. This register also receives the remainder after the execution of a Divide order. It may be used as the A, B or C address of an order.

1997 - Sentinel Register

Any order which implements a transfer between the high speed memory and a buffer will also implement the transfer of a word to the Sentinel Register. If the trans-

fer order senses a sentinel, then the first sentinel sensed by the order is stored in the Sentinel Register; if no sentinel is sensed, then a Pass Order is stored there.

The Transfer orders in question are Transfer In, Transfer Out, Transfer and Select, Double Transfer and Select, First Key Comparison, and Second Key Comparison. In the case of Transfer In, Transfer and Select, and Double Transfer and Select, all words transferred in and also the next word in the input buffer are examined for sentinels. In the case of the Key Comparison Orders the sentinel sensing is performed on the word at address A, that is, on the word that has been transferred. In the case of Transfer Out the overflow words are sensed for sentinels. Notice that output words are not sensed for sentinels in the Double Transfer and Select Order.

This register also plays a special role in multiplication, and contains seven times the multiplicand upon completion of a multiplication.

1999 - Current Order Register

DATAmatic 1000 orders are processed in eight word cycles. The Current Order Register is used for storing a number of different items of information related to these eight cycles under the conditions mentioned below.

1. When an order is chosen in a normal order sequence:
   a. During cycle 0 through 7, it contains the address of the order being executed.
   b. During cycle 8, it contains the order just executed.
2. When an order is chosen by a subsequence selection:
   a. During cycle 0 through 7, it contains the previous order executed, i.e., the order that made the subsequence selection.
   b. During cycle 8, it contains the order just executed.
3. When an order is chosen as the result of changing to a new order sequence:
   a. During cycle 0 through 7, it contains the address or order being executed.
   b. During cycle 8, it contains the order just executed.

At the beginning of cycle 0, the next order is being selected for execution. At the end of cycle 7, the order has been executed, but some checking* remains to be done. This checking is done during cycle 8; at the end of cycle 8 the order is officially completed.

*All phases of the execution of an order are checked by built-in equipment.

When the Current Order Register contains the address of the order being executed, the 3 decimal digits of the address are located in its A address position. However, the binary designator (zero or one, depending on which half of the 2000-word memory is being used) for this address resides in the B binary designator position. All other word positions are blank. When the Current Order Register contains the order just executed, the address portions of the order word are in the order CAB rather than the normal ABC. Thus, the address of the order being executed always resides in the same word position (A address) whether a programmed third address or a normal order sequence address.

Since this register contains the address of the order being processed, the programmer may use it as a diagnostic aid when the central system stops.