Bull

DEVICE ADAPTER UNIT
MODULE MANUAL
WDAU66LA/LC
58010008

THIS APPLIES TO THE FOLLOWING CABINETS:

WIOU100A/B
WIMU600D
WDAU001A/B

58010008-501
DIST. CODE NCO, XAN

REV D
JULY 1989

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RECORD OF REVISION			
REV	DATE	AUTHORIZATION	PAGES AFFECTED
A	11/84	PHAFPW982	58010008-012 58010008-031 58010008-500 58010008-011,1F 58010008-014,1F 58010008-530,1 THRU 5F 58010008-015,1-1, 1-2F 58010008-051,2-1 THRU 2-2F 58010008-100,3-1 THRU 3-91F 58010008-800,1F 58010008-900,1,2,3F 58010008-101,1F 58010008-102,1F 58010008-802,1F 58010008-103,1F 58010008-803,1F 58010008-104,1F 58010008-804,1F 58010008-105,1F 58010008-805,1F 58010008-106,1F 58010008-107,1F 58010008-108,1F 58010008-109,1F 58010008-110,1F
B	1/85	PHAFPW986	58010008-500 58010008-014,1F 58010008-530,1 58010008-100,3-22 & 3-26 58010008-101,1F 58010008-401,1,2F 58010008-102,1F 58010008-402,1,2F 58010008-103,1F 58010008-403,1,2,3,4F 58010008-104,1F 58010008-404,1,2F

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C	5/86	PHAFPW806	VOLUME 1 58010008-012,1F 58010008-031,1F 58010008-501 58010008-014,1F 58010008-034,1F 58010008-035,1F 58010008-531,1 THRU 5F 58010008-015,1-1, 1-2F 58010008-051,2-1 THRU 2-5F 58010008-800,1F 58010008-900,1, 2F VOLUME 2 58010008-502 58010008-011,1F 58010008-532,1F 58010008-101,1F 58010008-401,1 THRU 5F 58010008-102,1F 58010008-402,1 THRU 4F 58010008-802,1F 58010008-103,1F 58010008-403,1 THRU 10F 58010008-803,1F 58010008-104,1F 58010008-404,1 THRU 6F 58010008-804,1F 58010008-105,1F 58010008-405,1 THRU 10F 58010008-111,1F

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REV	DATE	AUTHORIZATION	PAGES AFFECTED
D	7/89	PHAFPW815	VOLUME 1 58010008-012,1F 58010008-030,1F 58010008-501 58010008-011,1F 58010008-014,1, 2F 58010008-034,1F 58010008-035,1F 58010008-531,1 THRU 5F 58010008-015,1-1, 1-2F 58010008-051,2-1 THRU 2-5F 58010008-100,3-1 THRU 3-91F 58010008-800,1F 58010008-900,1, 2F VOLUME 2 58010008-502 58010008-011,1F 58010008-532,1F 58010008-101,1F 58010008-401,1 THRU 5F 58010008-102,1F 58010008-402,1 THRU 4F 58010008-802,1F 58010008-103,1F 58010008-403,1 THRU 10F 58010008-803,1F 58010008-104,1F 58010008-404,1 THRU 6F 58010008-804,1F 58010008-105,1F 58010008-405,1 THRU 10F 58010008-106,1F 58010008-107,1F 58010008-108,1F 58010008-109,1F 58010008-110,1F 58010008-111,1F 58010008-112,1F 58010008-113,1F 58010008-114,1F 58010008-115,1F 58010008-116,1F

RECORD OF REVISION			
REV	DATE	AUTHORIZATION	PAGES AFFECTED

SUMMARY OF REVISION D CHANGES:

Volume 1 Changes:

1. Removed all reference to Honeywell.
2. Changed binder to the new gray binder.
3. Changed spine to 2 inches.
4. Changed Honeywell Confidential and Proprietary to Bull Confidential and Proprietary.
5. Added CL2 Cable Requirements.
6. Changed Customer Service Division to Customer Service Operation. Also Changed CSD to CSO.
7. Added Options WCAB001B, WACT66LE, WACT003A, WACT003B, and WGND001A to Volume 2 Table of Contents located in Volume 1.

Volume 2 Changes:

1. Removed all reference to Honeywell.
2. Changed binder to the new gray binder.
3. Changed spine to 2 inches.
4. Changed Honeywell Confidential and Proprietary to Bull Confidential and Proprietary.
5. Added Option Tab 12: Added WCAB001B Option and Installation Kit Parts List and Installation Instructions.
6. Added Option Tab 13: Added WACT66LE Option and Installation Kit Parts List and Installation Instructions.
7. Added Option Tab 14: Added WACT003A Option and Installation Kit Parts List and Installation Instructions.
8. Added Option Tab 15: Added WACT003B Option and Installation Kit Parts List and Installation Instructions.
9. Added Option Tab 16: Added WGND001A Option and Installation Kit Parts List and Installation Instructions.

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TITLE	DEVICE ADAPTER UNIT MODULE MANUAL WDAU66LA/LC	MANUAL #	58010008
		REVISION	REV D
		DATED	JULY 1989

ERRORS IN PUBLICATION

SUGGESTIONS FOR IMPROVEMENT TO PUBLICATION

Your comments will be investigated by appropriate technical personnel and action will be taken as required. Receipt of all forms will be acknowledged; however, if you require a detailed reply, check here. ☐

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TABLE OF CONTENTS
VOLUME 1

LIST OF ILLUSTRATIONS

DAU MODULE MANUAL

LIST OF TABLES

DAU MODULE MANUAL

VOLUME 2

OPTIONS

1.0 GENERAL

1.1 INTRODUCTION

This section contains an introduction to the WDAU66LA/B/C/D Device Adapter Unit Module Manual which describes the scope, purpose, and structure of the manual.

1.1.1 SCOPE

This manual is designed as part of the Product Maintenance Documentation (PMD) for the Series WDAU66LA/B/C/D Device Adapter Unit. The manual is primarily for use by the Customer Services Operation (CSO) and LCPD Manufacturing. The manual is Bull Confidential & Proprietary and is divided into sections separated by tabs.

1.1.1.1 GENERAL TAB

This section contains the introductory material.

1.1.1.2 PHYSICAL OUTLINE TAB

This section contains an outline drawing of the functional unit showing the installed location of its options and optimum replaceable units.

1.1.1.3 THEORY OF OPERATION TAB

This section contains a multilevel description of unit operation keyed to Major Block, Intermediate Block and Flow diagrams. Coverage will give the specialist the information necessary to trace signals in the Logic Block Diagrams (LBDs).

1.1.1.4 PARTS TAB

This section contains the DAU assembly and subassembly drawings and Parts Lists (PLs).

1.1.1.5 WIRE LISTS/SCHEMATICS TAB

This section contains the MICROFICHE INDEX which lists the logic wire lists that are contained on microfiche cards located in the microfiche card box. It also contains the schematics pertinent to the DAU assemblies and subassemblies.

1.1.1.6 OPTIONS TAB

This section contains the installation kits and installation instructions for the DAU options.

1.1.1.7 CKT/LOGIC TAB

This section contains the Logic Block Diagram (LBD), the Revision Status Sheet (RSS), and the Component Installation List (CIL) and/or installation instructions for each circuit board.

1.1.2 PURPOSE

This manual is a reference document which contains information to aid CSO instructors and students in training on the DAU and CSO installation and maintenance of the DAU in the field.

1.1.2.1 CSO TRAINING

The student should become familiar with, and be able to, effectively use this manual even if the student is supported with additional material (handouts) by the instructor.

1.1.2.2 CSO FIELD INSTALLATION AND MAINTENANCE

This manual can be used by CSO for installation of the DAU options or for direct maintenance of the DAU at customer sites to isolate failures not found by T&D ORU callout and replacement.

1.1.2.3 CSO TECHNICAL ASSISTANCE CENTER (TAC)

This manual can be used for remote support of field sites. It should be part of a primary reference library for use by TAC in contact with CSO or a maintenance computer at a customer site.

1.2 REFERENCE DOCUMENTATION

The following manuals contain supplemental documentation for servicing the DAU:

- 58010075 Test and Repair Manual for ELS-1E/2
- 58010012 Test and Repair Manual for DPS 8 52/70
- 58009933 Test and Repair Manual for DPS 88

1.3 FEEDBACK

Send any comments on this manual to:

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Phoenix, Arizona 85066-8000

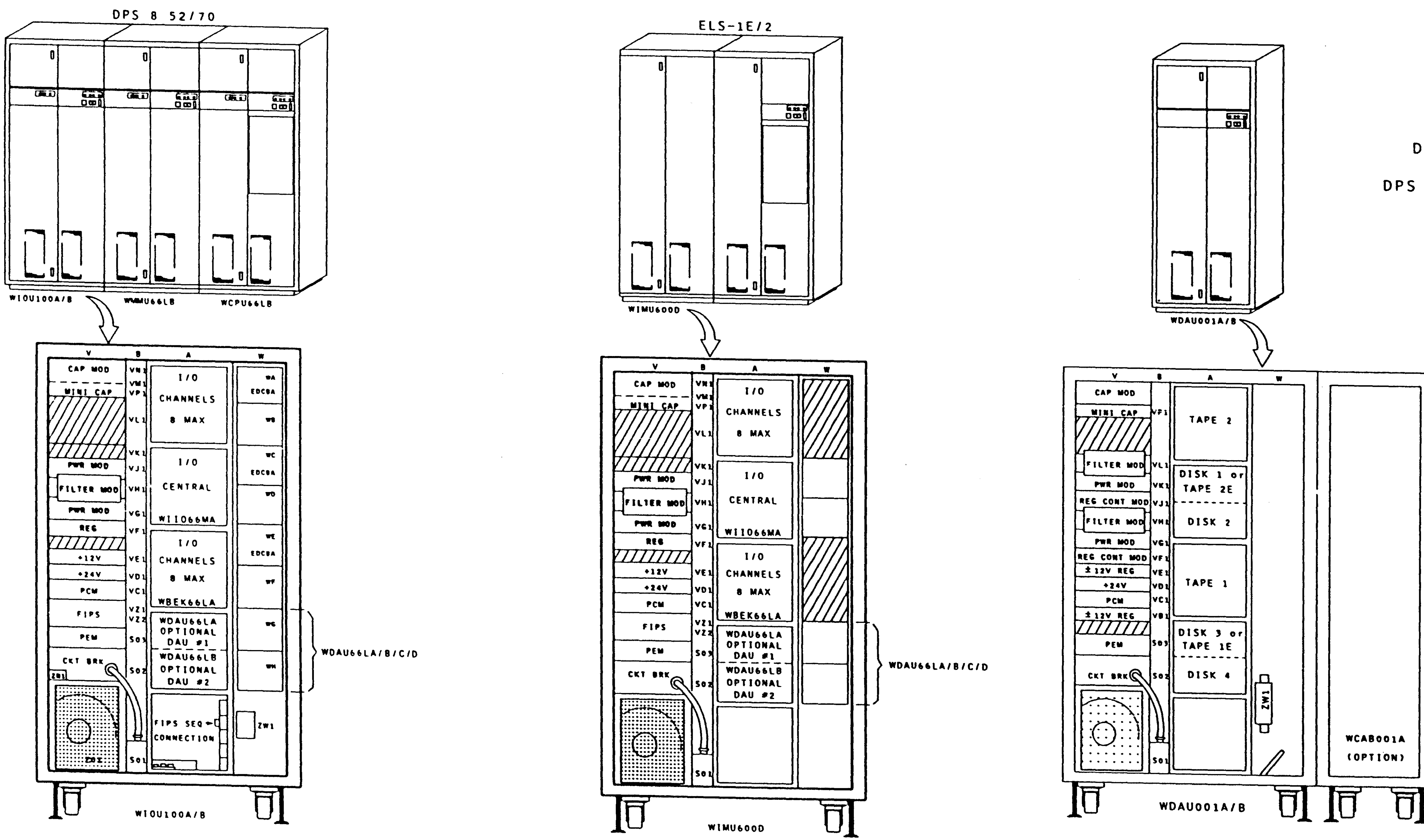

FIGURE 2.0-1. DEVICE ADAPTER UNIT PHYSICAL OUTLINE

WIOU100A/B OR WIMU600D CABINETS			
MODULE	SLOT	BOARD	FUNCTION
A3	A	MPCDI	THIRD WDDI66LA/LB OPTION
	B	MPCDI	SECOND WDDI66LA/LB OPTION
	C	MPCDI	FIRST WDDI66LA/LB OPTION
	D	WDAEI	FIRST DAU (WDAU66LA/LC)
	E	WDASE	FIRST DAU (WDAU66LA/LC)
	F	WDAMP	FIRST DAU (WDAU66LA/LC)
	G	WDASB	FIRST DAU (WDAU66LA/LC)
	H	WDACI	SECOND WDDA66LC/LD OPTION
	J	WDACI	FIRST WDDA66LC/LD OPTION
	K		
	L		
	M		
	N		
	P		
	Q		
	R		
	S		
	T		
	U		

ONE DAU INSTALLED

WIOU100A/B OR WIMU600D CABINETS			
MODULE	SLOT	BOARD	FUNCTION
A3	A	MPCDI	FIFTH WDDI66LA/LB OPTION
	B	MPCDI	THIRD WDDI66LA/LB OPTION
	C	MPCDI	FIRST WDDI66LA/LB OPTION
	D	WDAEI	FIRST DAU (WDAU66LA/LC)
	E	WDASE	FIRST DAU (WDAU66LA/LC)
	F	WDAMP	FIRST DAU (WDAU66LA/LC)
	G	WDASB	FIRST DAU (WDAU66LA/LC)
	H	WDACI	THIRD WDDA66LC/LD OPTION
	J	WDACI	FIRST WDDA66LC/LD OPTION
	K		
	L	WDACI	SECOND WDDA66LC/LD OPTION
	M	WDACI	FOURTH WDDA66LC/LD OPTION
	N	WDASB	SECOND DAU (WDAU66LB/LD)
	P	WDAMP	SECOND DAU (WDAU66LB/LD)
	Q	WDASE	SECOND DAU (WDAU66LB/LD)
	R	WDAEI	SECOND DAU (WDAU66LB/LD)
	S	MPCDI	SECOND WDDI66LA/LB OPTION
	T	MPCDI	FOURTH WDDI66LA/LB OPTION
	U	MPCDI	SIXTH WDDI66LA/LB OPTION

TWO DAUs INSTALLED

FIGURE 2.0-2. DAU BOARD LAYOUT AND OPTIONS (SHEET 1 OF 4)

WDAU001A/B CABINETS			
MODULE	SLOT	BOARD	FUNCTION
A1	A	MPCDI	THIRD WDDI66LA/LB OPTION
	B	MPCDI	SECOND WDDI66LA/LB OPTION
	C	MPCDI	FIRST WDDI66LA/LB OPTION
	D	WDAEI	FIRST DAU (WDAU66LA/LC)
	E	WDASE	FIRST DAU (WDAU66LA/LC)
	F	WDAMP	FIRST DAU (WDAU66LA/LC)
	G	WDASB	FIRST DAU (WDAU66LA/LC)
	H	WDACI	SECOND WDDA66LC/LD OPTION
	J	WDACI	FIRST WDDA66LC/LD OPTION
	K		
	L		
	M		
	N		
	P		
	Q		
	R		
	S		
	T		
	U		

ONE DAU INSTALLED

WDAU001A/B CABINETS			
MODULE	SLOT	BOARD	FUNCTION
A1	A	MPCDI	FIFTH WDDI66LA/LB OPTION
	B	MPCDI	THIRD WDDI66LA/LB OPTION
	C	MPCDI	FIRST WDDI66LA/LB OPTION
	D	WDAEI	FIRST DAU (WDAU66LA/LC)
	E	WDASE	FIRST DAU (WDAU66LA/LC)
	F	WDAMP	FIRST DAU (WDAU66LA/LC)
	G	WDASB	FIRST DAU (WDAU66LA/LC)
	H	WDACI	THIRD WDDA66LC/LD OPTION
	J	WDACI	FIRST WDDA66LC/LD OPTION
	K		
	L	WDACI	SECOND WDDA66LC/LD OPTION
	M	WDACI	FOURTH WDDA66LC/LD OPTION
	N	WDASB	SECOND DAU (WDAU66LB/LD)
	P	WDAMP	SECOND DAU (WDAU66LB/LD)
	Q	WDASE	SECOND DAU (WDAU66LB/LD)
	R	WDAEI	SECOND DAU (WDAU66LB/LD)
	S	MPCDI	SECOND WDDI66LA/LB OPTION
	T	MPCDI	FOURTH WDDI66LA/LB OPTION
	U	MPCDI	SIXTH WDDI66LA/LB OPTION

TWO DAUs INSTALLED

FIGURE 2.0-2. DAU BOARD LAYOUT AND OPTIONS (SHEET 2 OF 4)

WDAU001A/B CABINETS			
MODULE	SLOT	BOARD	FUNCTION
A1	A	MPCDI	SEVENTH WDDI66LA/LB OPTION
	B	MPCDI	FOURTH WDDI66LA/LB OPTION
	C	MPCDI	FIRST WDDI66LA/LB OPTION
	D	WDAEI	FIRST DAU (WDAU66LA/LC)
	E	WDASE	FIRST DAU (WDAU66LA/LC)
	F	WDAMP	FIRST DAU (WDAU66LA/LC)
	G	WDASB	FIRST DAU (WDAU66LA/LC)
	H	WDACI	FOURTH WDDA66LC/LD OPTION
	J	WDACI	FIRST WDDA66LC/LD OPTION
	K		
	L	WDACI	SECOND WDDA66LC/LD OPTION
	M	WDACI	FIFTH WDDA66LC/LD OPTION
	N	WDASB	SECOND DAU (WDAU66LB/LD)
	P	WDAMP	SECOND DAU (WDAU66LB/LD)
	Q	WDASE	SECOND DAU (WDAU66LB/LD)
	R	WDAEI	SECOND DAU (WDAU66LB/LD)
	S	MPCDI	SECOND WDDI66LA/LB OPTION
	T	MPCDI	FIFTH WDDI66LA/LB OPTION
	U	MPCDI	EIGHTH WDDI66LA/LB OPTION

THREE DAUs INSTALLED

WDAU001A/B CABINETS			
MODULE	SLOT	BOARD	FUNCTION
A3	A	MPCDI	NINETH WDDI66LA/LB OPTION
	B	MPCDI	SIXTH WDDI66LA/LB OPTION
	C	MPCDI	THIRD WDDI66LA/LB OPTION
	D	WDAEI	THIRD DAU (WDAU66LA/LC)
	E	WDASE	THIRD DAU (WDAU66LA/LC)
	F	WDAMP	THIRD DAU (WDAU66LA/LC)
	G	WDASB	THIRD DAU (WDAU66LA/LC)
	H	WDACI	SIXTH WDDA66LC/LD OPTION
	J	WDACI	THIRD WDDA66LC/LD OPTION
	K		
	L		
	M		
	N		
	P		
	Q		
	R		
	S		
	T		
	U		

FIGURE 2.0-2. DAU BOARD LAYOUT AND OPTIONS (SHEET 3 OF 4)

WDAU001A/B CABINETS			
MODULE	SLOT	BOARD	FUNCTION
A1	A	MPCDI	NINTH WDDI66LA/LB OPTION
	B	MPCDI	FIFTH WDDI66LA/LB OPTION
	C	MPCDI	FIRST WDDI66LA/LB OPTION
	D	WDAEI	FIRST DAU (WDAU66LA/LC)
	E	WDASE	FIRST DAU (WDAU66LA/LC)
	F	WDAMP	FIRST DAU (WDAU66LA/LC)
	G	WDASB	FIRST DAU (WDAU66LA/LC)
	H	WDACI	FIFTH WDDA66LC/LD OPTION
	J	WDACI	FIRST WDDA66LC/LD OPTION
	K		
	L	WDACI	SECOND WDDA66LC/LD OPTION
	M	WDACI	SIXTH WDDA66LC/LD OPTION
	N	WDASB	SECOND DAU (WDAU66LB/LD)
	P	WDAMP	SECOND DAU (WDAU66LB/LD)
	Q	WDASE	SECOND DAU (WDAU66LB/LD)
	R	WDAEI	SECOND DAU (WDAU66LB/LD)
	S	MPCDI	SECOND WDDI66LA/LB OPTION
	T	MPCDI	SIXTH WDDI66LA/LB OPTION
	U	MPCDI	TENTH WDDI66LA/LB OPTION

FOUR DAUs INSTALLED

WDAU001A/B CABINETS			
MODULE	SLOT	BOARD	FUNCTION
A3	A	MPCDI	ELEVENTH WDDI66LA/LB OPTION
	B	MPCDI	SEVENTH WDDI66LA/LB OPTION
	C	MPCDI	THIRD WDDI66LA/LB OPTION
	D	WDAEI	THIRD DAU (WDAU66LA/LC)
	E	WDASE	THIRD DAU (WDAU66LA/LC)
	F	WDAMP	THIRD DAU (WDAU66LA/LC)
	G	WDASB	THIRD DAU (WDAU66LA/LC)
	H	WDACI	SEVENTH WDDA66LC/LD OPTION
	J	WDACI	THIRD WDDA66LC/LD OPTION
	K		
	L	WDACI	FOURTH WDDA66LC/LD OPTION
	M	WDACI	EIGHTH WDDA66LC/LD OPTION
	N	WDASB	FOURTH DAU (WDAU66LB/LD)
	P	WDAMP	FOURTH DAU (WDAU66LB/LD)
	Q	WDASE	FOURTH DAU (WDAU66LB/LD)
	R	WDAEI	FOURTH DAU (WDAU66LB/LD)
	S	MPCDI	FOURTH WDDI66LA/LB OPTION
	T	MPCDI	EIGHTH WDDI66LA/LB OPTION
	U	MPCDI	TWELFTH WDDI66LA/LB OPTION

FIGURE 2.0-2. DAU BOARD LAYOUT AND OPTIONS (SHEET 4 OF 4)

3.0 THEORY OF OPERATION

3.1 BASIC PRINCIPLES OF DAU SUBSYSTEM

The DAU is a Microprogrammed Peripheral Device Adapter Unit for the control of 4XX (MSU0402 and MSU0451) and 50X (MSU0500, MSU0501/MSU0501N) type devices. It provides control for seeking, address verification and read or write operations. The upstream connection to an I/O Controller is via the PSI/PSIA 2- or 4-trip interface. The downstream connection is to the device via the device level interface.

Figure 3.1-1 is a functional block diagram of the DAU. It shows that the DAU is implemented in five board types for the minimum configuration. The DAU consists of a low performance microprocessor (MP), a high performance sequencer (SE) and support hardware (CI, SB, and EI). All major data buses and control signals between the different board types are shown on this diagram

Overall supervision is accomplished by the microprocessor with support chips. It operates as a memory-mapped I/O using a split bus.

The microprocessor controls the command dialog with the PSIA by loading and reading registers in the PSI interface logic. It controls data transfer by preconditioning the interface and store logic, requests data transfers from/to the PSIA by issuing hardware service codes, and monitors store space available or data ready. The sequencer monitors a store full flag and will halt the impending write if the data is not available or impending read if space is not available.

In cases where the data transfer is internal between the store board and the EDAC board or store board to store board, the microprocessor sets the store read and write sector addresses, loads the number of sectors affected counter, and loads the Store Mode Register. The microprocessor then monitors the completion flag.

Device control is accomplished by a unique sequencer which is loaded by the microprocessor firmware at startup. Once started this sequencer can independently select any type of data or control required by the device and can monitor for any type error or exception. The DAU has the ability to sustain multisector reads or writes to the end of track, switch heads and continue with the transfer.

The sequencer microtask assignment is accomplished by loading hardware registers, counters, and the sequencer starting address (dependent on the task). The microprocessor then returns to multitasking. When the sequencer completes its task or encounters an error or exception, it sets a flag or flags in a status register which is monitored by the microprocessor.

All users' data paths and most control paths carry parity. Integrity of the write EDAC bytes is checked by wrapping them back into the EDAC from the final DAU register, where parity is generated or checked. The Microprocessor executes the 4XX EDAC correction by fetching bytes from the store, correcting them, and then restoring the corrected bytes.

The corrected sector is then recirculated through the EDAC to assure that the microprocessor did not err or that the correction was not programmed wrong. Parity is carried on the I/O split bus up to the microprocessor chip. The hardware does the 50X EDAC correction and its integrity is also verified.

3.2 CHANNEL INTERFACE (CI)

3.2.1 CI OVERVIEW

The purpose of the CI board is to provide a vehicle for the microprocessor (firmware) to control the flow of data from the DAU to I/O interface.

The CI is a hardware communication circuit board which connects the DAU to the PSI (see Figure 3.1-1). The DAU firmware controls the CI. Up to two CIs can be connected to the DAU. Each CI has two PSI ports which allow the CI to be shared by two physical PSI channels. The two channels can be connected to the same I/O or two different I/Os. The CI can transfer data over both physical PSI channels, but not simultaneously, and only by switching from one channel to the other under control of the DAU firmware.

In addition, either channel may operate as a 2- or 4-trip interface. This allows connections to all I/O equipment. The 2- or 4-trip selection is made by a backpanel jumper plug.

A PSI Reset Out signal on any channel will initialize the DAU and start the preliminary self test. The self test will destroy any firmware that is in the DAU. So, firmware must be reloaded.

Firmware will be down line loaded from the system.

3.2.2 CI BLOCK DIAGRAM

Refer to Figure 3.2-1. This figure is a major block diagram of the CI board. It shows the data paths within the CI board and its connections to the PSI, SB, and MP boards. These data paths and their control are discussed in the following paragraphs.

3.2.3 MICROPROCESSOR INTERFACE LOGIC

3.2.3.1 WRITE CONTROL

Refer to the Microprocessor Write Control Diagram, Figure 3.2-2.

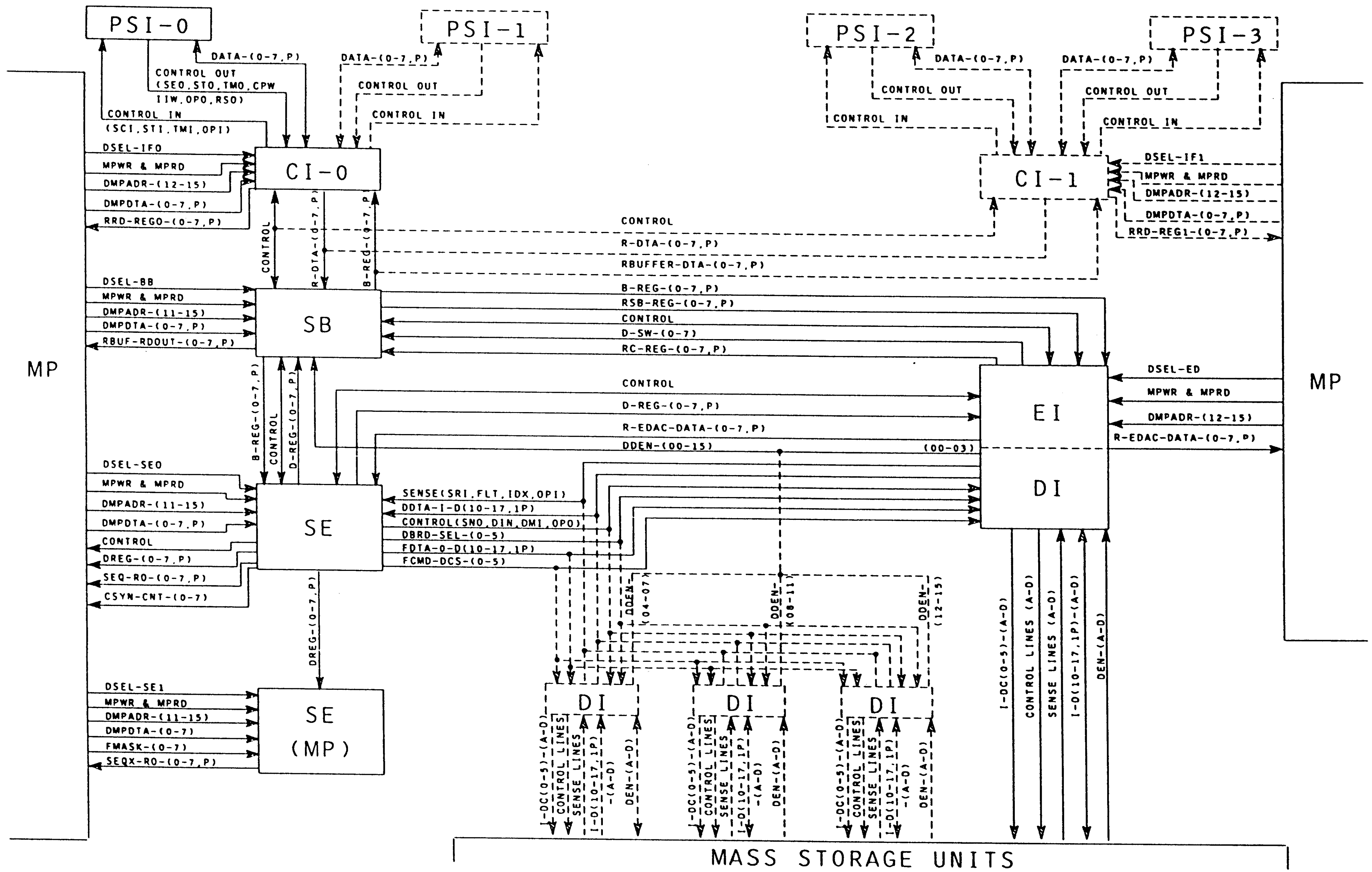

FIGURE 3.1-1. DAU FUNCTIONAL BLOCK DIAGRAM

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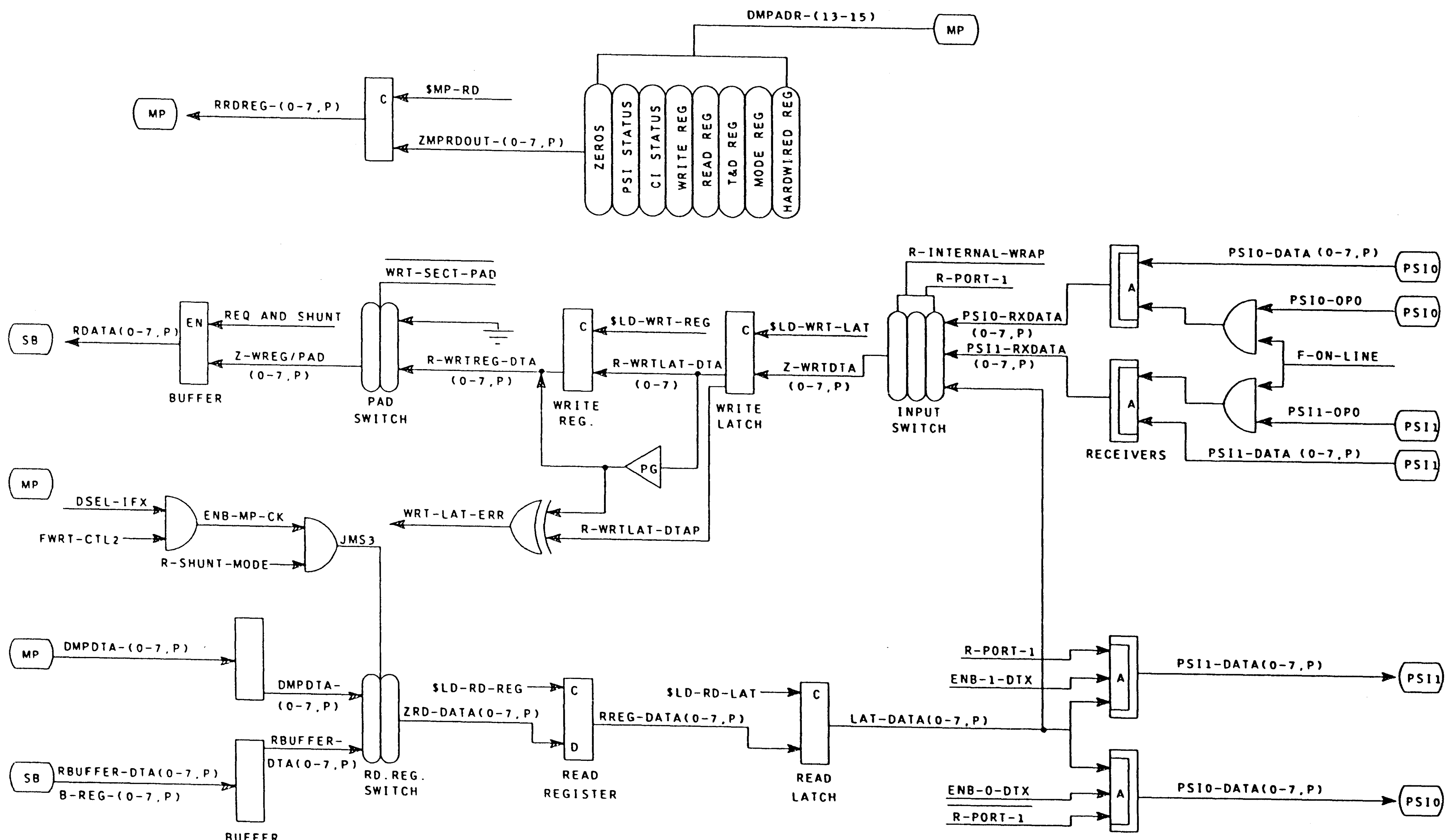


FIGURE 3.2-1. CI BOARD MAJOR BLOCK DIAGRAM

Signals $MP-WR and $MP-RD enter the CI board from the MP board and are used to clock their respective Write (FWR) and Read (FRD) flip-flops provided the microprocessor has selected this CI board (DSEL-IFX). FWR and FRD are synchronized by the free-running clock to produce control signals FWRT-CTL1, FWRT-CTL2, and FRD-CTL1. These signals are used to gate various control signals and data throughout the CI logic.

3.2.3.2 MICROPROCESSOR WRITE ADDRESSING

In order for the microprocessor to perform its required functions, the CI board has been designed with numerous registers and counters which the microprocessor has the ability to load and read back.

Figure 3.2-2 shows the microprocessor address lines DMPADR-12 through MPADR-15 as inputs to a 1 of 8 select chip. The CI selected signal (DSEL-IFX) is used to enable the chip. The 1 of 8 select chip decodes the address lines into commands which are used to control the setting of the various registers and control flip-flops.

CMD-SEL-RESET address B0X0 is ANDed with FWRT-CTL2 to generate DCMD-B0X0. DCMD-B0X0 is ANDed with the microprocessor's data lines DMPDTA(0-7) to load the CI Control Register.

DCMD-B0X0, ANDed with DMPDTA-0, toggles the F-ON-LINE flip-flop, which returns CI-ON-LINE to the microprocessor. F-ON-LINE enables the PSI interface signals on the CI board.

Line CIX-ONLINE comes from the ONLINE/OFFLINE switch mounted on the DAU Control Panel. This line passes through the CI board. It allows the microprocessor to determine if a CI board is present or not when the switch is in the online position.

DCMD-B0X0, ANDed with DMPDTA-1, sets the Partial Clear flip-flop F-PCLR. F-PCLR is used to reset selected control and error logic on the CI board.

DCMD-B0X0, ANDed with DMPDTA-2, sets the Total Clear flip-flop F-TCLR. F-TCLR is used to initialize the CI logic.

DCMD-B0X0, ANDed with DMPDTA-3, sets the Transfer Request flip-flop FXFRREQ. FXFRREQ allows the loading of zeros from the Pad Switch if a full sector of data is not transferred from the central system.

DCMD-B0X0, ANDed with DMPDTA-6, sets the F-OPI0 and F-OPI1 flip-flops. DMPDTA-7 resets either F-OPI0 or F-OPI1, depending on which PSI port is selected by the Mode Register (R-PORT-1).

CMD-LD-MODE address B0X1 is ANDed with FWRT-CTL2 and $FREE-RUNNING to generate $LD-MODE. $LD-MODE clocks the microprocessor data lines DMPDTA-(0-7) into the Mode Register.

CMD-LD-T&D address B0X2 is ANDed with FWRT-CTL2 and $FREE-RUNNING to generate $LD-TD. $LD-TD clocks the microdata lines DMPDTA-(0-5) into the T&D Mode Register.

The remaining commands decoded by the Address Decoder are used to load the microdata line into the Read Register. These commands may send a Terminate In, a Service Code In, or both, to the PSI interface.

3.2.3.3 READ CONTROL

Refer to Figure 3.2-3. This figure shows the Microprocessor Read Control logic for the CI board. The CI Registers, status and selected control flip-flops are read by the microprocessor. The select 1 of 8 Readout switch is addressed by the micro when in the read mode ($MP-RD). The selected byte is sent to the MP board, along with the generated parity bit. Parity is checked on the contents of the Mode Register, Read Register and Write Register when they are read. FRD-OUT-PTY-ERR is set if bad parity is detected.

3.2.3.4 HARDWARE REGISTER ADDRESSING

The addresses utilized by the microprocessor to access the various registers and control functions within the CI board are shown below. Some of the registers are write only, some are read only, and others have the capability to be loaded and read back.

ADDR	WRITE	READ
B0X0	CI Control	Hardwired Register
B0X1	Mode Register	Mode Register
B0X2	T&D Register	T&D Register
B0X3	Read Register	Read Register
B0X4	Read Reg. & Term.	Write Register
B0X5	Read Reg. & Serv. Code	CI Status
B0X6	Read Reg. & Serv. Code & Term	PSI Status
B0X7	Not Used	Not Used

NOTE: For addresses above, the "X" will be:

"0" or "1" for CI-0
"2" or "3" for CI-1

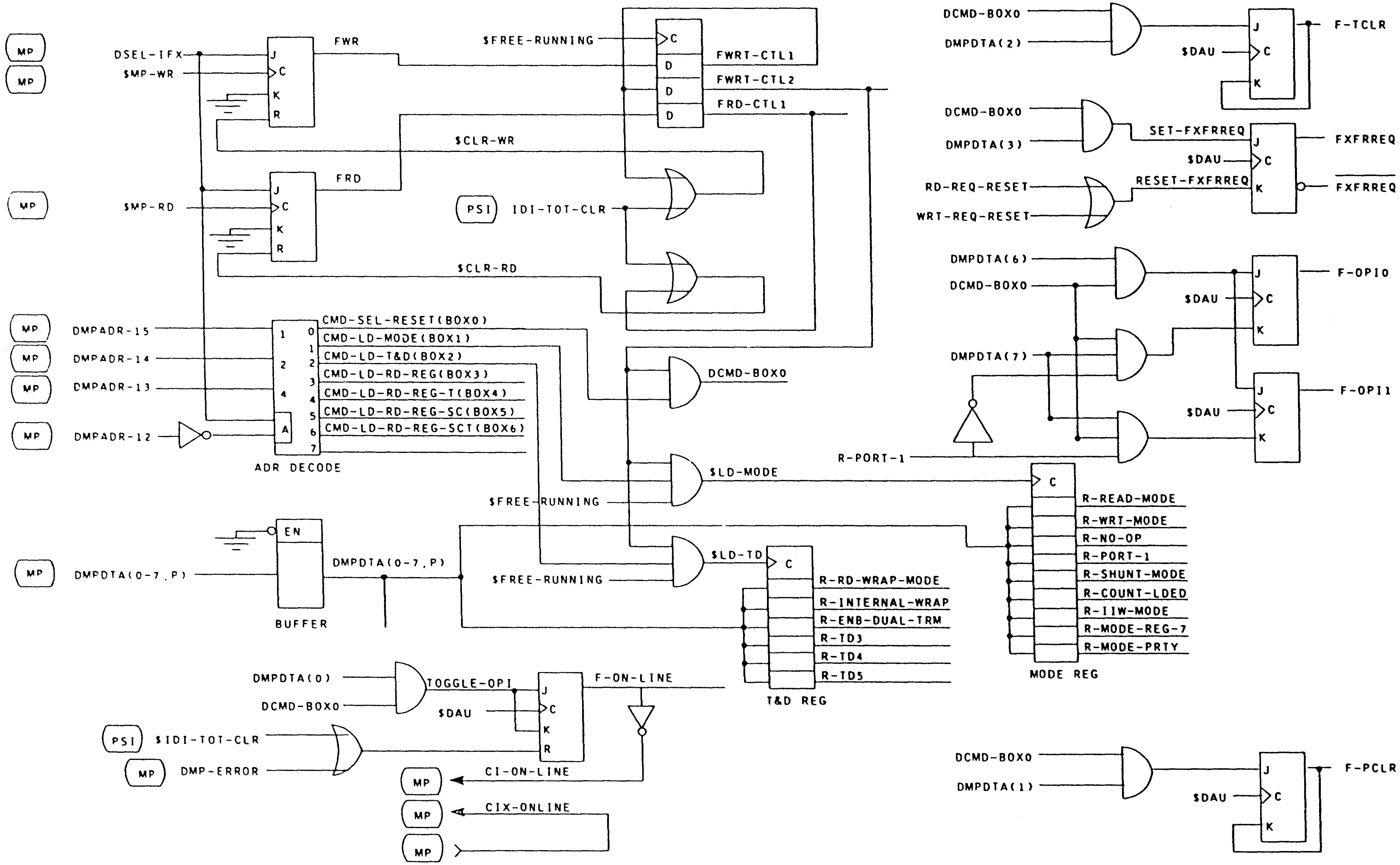


FIGURE 3.2-2. MICROPROCESSOR WRITE CONTROL

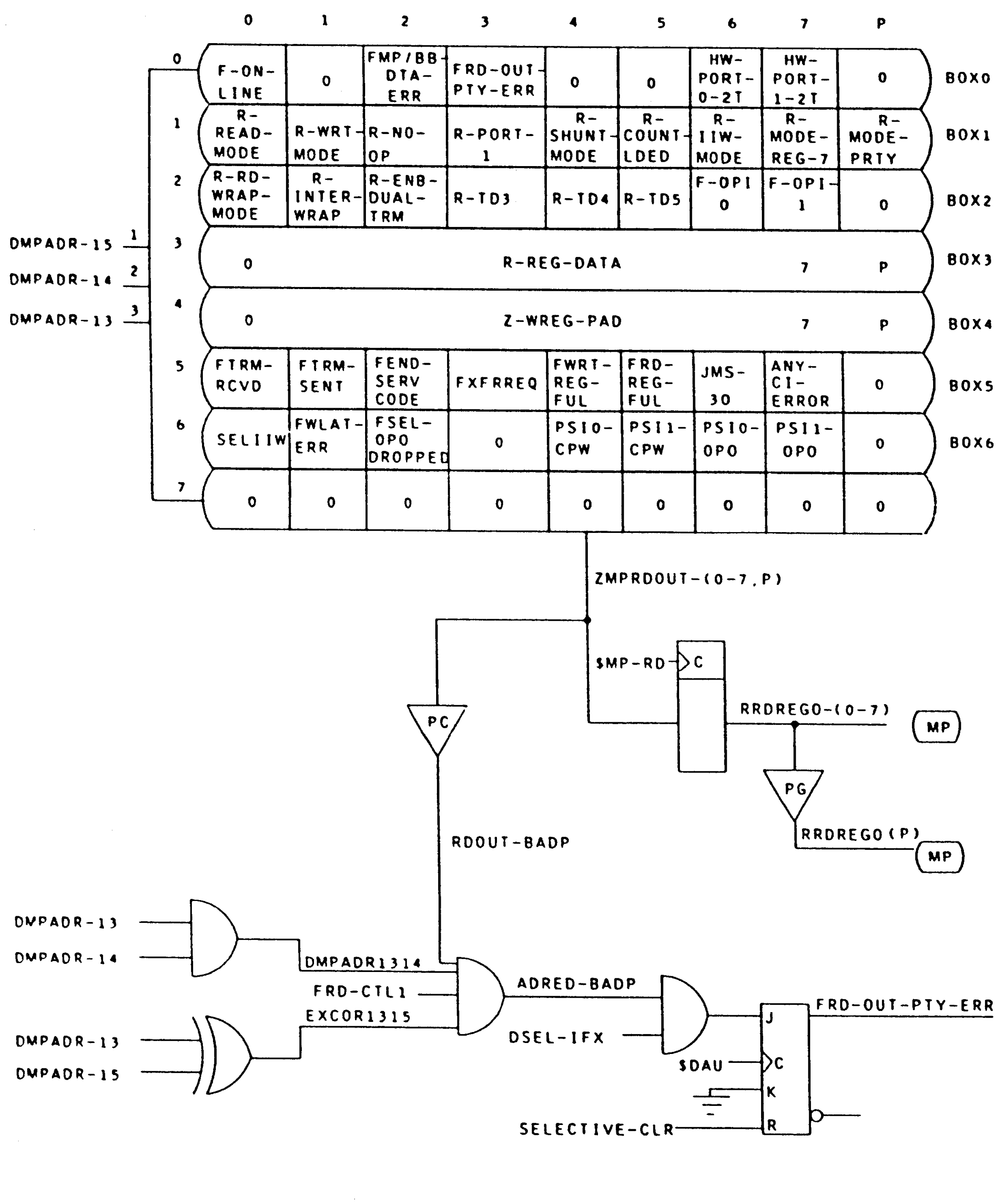


FIGURE 3.2-3. MICROPROCESSOR READOUT

3.2.4 HARDWARE REGISTER DESCRIPTION

3.2.4.1 WRITE CI CONTROL (BOX0)

This address is used by the microprocessor to selectively set and/or reset particular flip-flops.

0	1	2	3	4	5	6	7
CI STAT	PART CLR	TOT CLR	XFER REQ.			OPI-CONTROL	
						SET	RESET

Bit

0 CI State: This bit will allow the microprocessor control of the ON/OFF line state of the CI board. Writing to this register with this bit = 1 will change the state of the ON/OFF line flip-flop (F-ON-LINE).

1 Partial Clear: This bit at a one causes the Partial Clear flip-flop (F-PCLR) to set. Used by the microprocessor to reset selected flip-flops on the CI board (i.e., Term Rx, Term Tx, End Service Code).

2 Total Clear: This bit at a one causes the Total Clear flip-flop (F-TCLR) to set. Used by the microprocessor to reset the total CI board.

3 Transfer Request: This bit at a one causes the Transfer Request flip-flop (FXFRREQ) to set. Used by the microprocessor to enable the transfer of Data to/from the PSIA.

4 Not Used

5 Not Used

6 OPI Control Set: This bit at a one will allow the microprocessor to set the Operational In line to both ports (PSI-0 and PSI-1).

7 OPI Control Reset: This bit at a one will allow the microprocessor to reset the Operational In line to the PSI. PSI-0 or PSI-1 will be affected, depending on the state of the PSI Port Select bit in the Mode Register.

3.2.4.2 READ HARDWARE REGISTER (BOXO)

This address will be utilized by the microprocessor to obtain detailed hardware information from the Hardwired Register on the CI board.

0	1	2	3	4	5	6	7
CI STAT		MP WRITE ERROR	MP READ ERROR			2/4 TRIP PSI 0	2/4 TRIP PSI 1

Bit

0 CI State: This bit will indicate whether the CI board is in an online or offline condition by testing the state of flip-flop (F-ON-LINE).

1 Not Used

2 Microwrite Data Error: This bit will indicate that the CI board has detected a parity error in the data received from the MP or SB boards (FMP/BB-DTA-ERR).

3 Microread Error: This bit will indicate that there has been an error while the microprocessor is trying to read a register from the CI board (FRD-OUT-PTY-ERR).

4 Not Used

5 Not Used

6 PSI-0 2/4: This bit will indicate whether this PSI is in the 2-trip (=1), or the 4-trip (=0) mode of operation (HW-PORT0-2T).

7 PSI-1 2/4: This bit will indicate whether this PSI is in the 2-trip (=1), or the 4-trip (=0) mode of operation (HW-PORT1-2T).

3.2.4.3 WRITE OR READ MODE REGISTER (BOX1)

This register is provided to allow the microprocessor to specify the type of operation it desires and the proper port to select.

0	1	2	3	4	5	6	7
READ	WRITE	NO OPER	PSI PORT	SHUNT	CNTR LOAD	IIW	

Bit

0 Read: This bit will allow the microprocessor to specify that the CI board is to be doing a read operation (R-READ-MODE). A read is a transfer of data, status, or service code from the DAU to the system.

1 Write: This bit will allow the microprocessor to specify that the CI is to be doing a write operation (R-WRT-MODE). A write is a transfer of commands or data from the system to the DAU.

2 No Operation: This bit may be set and read back for testing purposes, but it will produce no action within the CI board (R-NO-OP).

3 PSI Port Select: This bit will allow the microprocessor to specify the port (R-PORT1) for the subsequent operation (PSI 0 = 0, PSI 1 = 1).

4 Shunt: This bit will allow the microprocessor to specify that the CI is to be operating in either of the previous conditions (read or write mode), but the information is to go to/from the store board (R-SHUNT-MODE).

5 Count Loaded: This bit will tell the CI board that the transfer counter (number of bytes to transfer) has been loaded (R-COUNT-LDED). When the counter expires, the CI board will send terminate to the system.

6 Illegal Instruction Word: This bit (R-IIW-MODE) will allow fetching of the fault byte.

7 Not Used: (R-MODE-REG-7)

3.2.4.4 WRITE OR READ T&D REGISTER (B0X2)

This register will be reserved for T&D functional use. It has yet to be determined just what information/operations can/will be performed.

0	1	2	3	4	5	6	7
READ WRAP MODE	INT WRAP MODE	DUAL TERM MODE	R-TD3	R-TD4	R-TD5	OPI	
						PSI 0	PSI 1

Bit

0 Read Wrap Mode: This mode bit (R-RD-WRAP-MODE) will allow the microprocessor to initiate a read sequence (data from the buffer), but the data byte will stop at the Write Register. It must then be read by the microprocessor.

1 Internal Wrap Mode: This mode bit (R-INTERNAL-WRAP) will allow the microprocessor to initiate a read sequence, the data will go from the buffer through the CI board and back to the buffer.

2 Dual Terminate: This mode bit (R-ENB-DUAL-TRM) will allow the microprocessor to test the terminate logic within the CI board.

3 Reserved for T&D.

4 Reserved for T&D.

5 Reserved for T&D.

6 OPI: This bit (read only) will reflect the state of the Operational In line (F-OPI0) to PSI 0.

7 OPI: This bit (read only) will reflect the state of the Operational In line (F-OPI1) to PSI 1.

3.2.4.5 WRITE READ REGISTER (B0X3)

This address will be utilized when the microprocessor desires to send information (data or status) to the PSIA.

3.2.4.6 READ READ REGISTER (B0X3)

When the microprocessor reads the Read Register, the Read Register Full flip-flop will be reset.

0	1	2	3	4	5	6	7
DATA, STATUS OR SERVICE CODE							

Bit

0-7 Data, Status, or Service Code (R-REG-DATA).

3.2.4.7 WRITE READ REGISTER AND TERMINATE (B0X4)

This address will be utilized by the microprocessor when it desires to send information (data or status) to the PSIA. The hardware will also send terminate with this byte if it is in a read mode. If the write mode is selected, the hardware will generate a terminate to the PSIA with the next byte received. (Refer to address B0X3 for register pictorial.)

3.2.4.8 WRITE READ REGISTER AND SERVICE CODE (B0X5)

This address will be utilized by the microprocessor when it desires to send a service code to the PSIA. (Refer to address B0X3 for register pictorial).

3.2.4.9 WRITE READ REGISTER AND SERVICE CODE AND TERMINATE (B0X6)

This address will be utilized by the microprocessor when it desires to send a service code to the PSIA. The hardware will also send terminate with this byte. (Refer to address B0X3 for register pictorial).

3.2.4.10 READ WRITE REGISTER (B0X4)

This address will be utilized by the microprocessor when it wishes to obtain information (IDCW, FAULT BYTE, etc.) from the PSIA. The hardware will reset the Write Register Full flip-flop.

0	1	2	3	4	5	6	7
INFORMATION OR DATA							

Bit 0-7 Information or Data (Z-WREG-PAD).

·.2.4.11 READ CI STATUS (BOX5)

his address will be used when the microprocessor wishes to obtain the tatus of the CI board.

0	1	2	3	4	5	6	7
TERM RX	TERM TX	END SERV. CODE	XFER REQ.	WRT FULL	READ FULL	WT/E IIW	CI ERROR

Bit

0 Terminate Received: This flag will indicate that the CI board has received a terminate signal (FTRM-RCVD) from the PSIA.

1 Terminate Transmitted: This flag will indicate that the CI board has transmitted a terminate signai (FTRM-SENT) to the PSIA.

2 End Of Service Code: This flag will indicate that the CI board has completed the dialog with the PSIA when sending a service code (FEND-SERV-CODE).

3 Transfer Request: This flag will indicate that the sector (either 64, 512 or absolute) transfer to/from the PSI is still in process (F-XFR-REQ).

4 Write Register Full: This bit will indicate to the microprocessor that the Write Register is full (FWRT-REG-FUL).

5 Read Register Full: This bit will indicate to the microprocessor that the Read Register is full (FRD-REG-FUL).

6 Write parity error or IIW: This bit will indicate that a Write Latch Parity Error (FWLAT-ERR), Illegal Instruction Word (SEL-IIW), or OPO dropped on the selected PSI (FSEL-OPO-DROPED) had occurred (JMS-30).

7 CI Error: This bit will indicate to the microprocessor that the CI board has detected a parity error (ANY-CI-ERROR) on either the microprocessor or store board data after it has passed the Read Register Switch (FMP/BB-DTA-ERR); or on the Microprocessor Read Out Register (FRD-OUT-PTY-ERR).

3.2.4.12 READ PSI STATUS (BOX6)

This address will be used by the microprocessor when it wishes to obtain the status of the PSI interface.

0	1	2	3	4	5	6	7
IIW	PRTY ERROR	OPO DROP		CPW		OPO	
				PSI 0	PSI 1	PSI 0	PSI 1

Bit

0 IIW: This flag (SELIIW) will indicate that there has been a fault detected by the selected PSIA (PSIA 0 or PSIA 1, based on the PSI Port Select bit in the Mode Register).

1 Parity Error: This bit indicates that the CI board has detected a parity error (FWLAT-ERR) on the selected PSIA interface (PSIA 0 or PSIA 1, based on the PSI Port Select bit in the mode Register).

2 OPO Dropped: This flag will indicate that there has been a drop of the Operational Out Line (FSEL-OPO-DROPPED) on the selected PSI interface.

3 Not Used

4 CPW PSI 0: This flag will indicate that there is a Channel Program Waiting on PSI 0 (PSI0-CPW).

5 CPW PSI 1: This flag will indicate that there is a Channel Program Waiting on PSI 1 (PSI1-CPW).

6 OPO PSI 0: This flag will indicate the presence/absence of the Operational Out Line from PSI 0 (PSI0-OPO).

7 OPO PSI 1: This flag will indicate the presence/absence of the Operational Out Line from PSI 1 (PSI1-OPO).

3.2.5 SERVICE CODES

Service codes are firmware's method of communicating with the PSIA. The service codes for the DAU are listed on the following page. Notice that bits 0 through 3 must always be zero.

BITS 0 3 4 7	SERVICE CODE DESCRIPTION
0000 0000	Invalid Code
0000 0001	Initiate New Channel Program
0000 0010	Move Pointer - Initiate Command Transfer
0000 0011	Back Pointer - Initiate Command Transfer
0000 0100	Read Binary
0000 0101	Read ASCII
0000 0110	Write Binary
0000 0111	Write ASCII
0000 1000	Special Interrupt Status
0000 1001	Termination Status
0000 1010	Invalid Code
0000 1011	Extended Status
0000 1100	Invalid Code
0000 1101	Termination Interrupt
0000 1110	Marker Interrupt
0000 1111	Special Interrupt

3.2.6 PSI INTERFACE

Figure 3.2-4 identifies the PSI to CI interface lines and their corresponding abbreviations. All lines with the designation IN originate at the DAU and terminate at the I/O Controller. All lines with the designation OUT originate at the I/O Controller and terminate at the DAU.

Mnemonics for the lines are obtained by using the first or most significant letters in the words that name the lines. The data lines (D) are followed by a digit indicating the position of the line in the data path.

3.2.6.1 SERVICE CODE IN (SCI)

This line extends from the DAU to the I/O Controller. When set, SCI indicates that the DAU has a service code to send to the I/O Controller. This line is fully interlocked with Service Enable Out (SEO). The DAU will not transfer the service code until SEO is high. SCI may not rise unless SEO is low. SCI remains high for the duration of the service code sequence and will fall when the DAU detects the drop of TMO for the last byte transferred in this service code sequence. SCI must fall after every service code sequence. If the DAU wants to send another service code sequence without any intervening data or command transfer, it must lower SCI until it detects the fall of SEO. Then it may again raise SCI and initiate the transfer of the next service code sequence. The first byte transferred in a service code sequence is always a service code.

3.2.6.2 SERVICE ENABLE OUT (SEO)

This line extends from the I/O Controller to the DAU and is used to indicate that the I/O is ready to receive a service code sequence. The line is fully interlocked with Service Code In (SCI). SEO will only rise after SCI rises, and can only be reset when the I/O detects the fall of SCI. The fall of SEO enables the DAU to initiate a new operation over the PSI. A hardware failure will be assumed if this line is reset while SCI is high or set while SCI is low.

No dialog other than a DAU initiated service code sequence may take place over the interface unless both SCI and SEO are in a logical zero state. SEO cannot be raised if a difference between STI and STO exists.

3.2.6.3 STROBE IN (STI)

The Strobe In line, in conjunction with Strobe Out (STO), controls the data transfers on the interface. This line extends from the DAU to the I/O Controller. It is activated by the DAU for a read or write operation.

For a read operation the STI line may be changed only if STI and STO are at the same logical level. A change of STI by the DAU when data is ready will cause the I/O to detect a difference between STI and STO. This will indicate to the I/O Controller that data is available on the data lines.

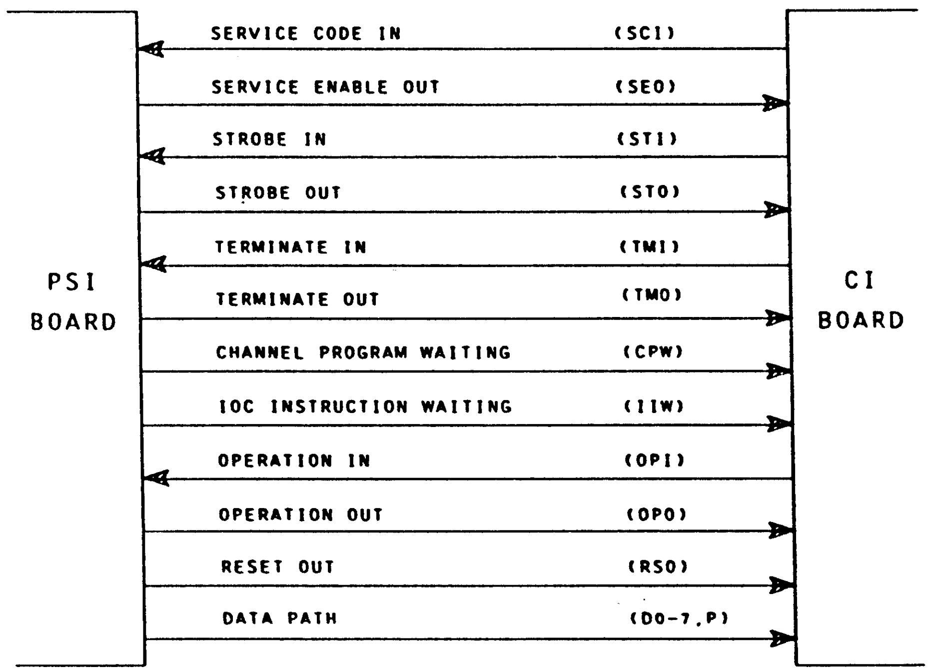


FIGURE 3.2-4. CI TO PSI INTERFACE

To obtain the data, the I/O will deskew STI a minimum of 40 nanoseconds, then store the data and check for a terminate condition. If a terminate condition exists, the I/O, when ready, will respond by setting the Terminate Out (TMO) line and performing the dialogue described for TMO. If a terminate condition does not exist, the I/O, when ready, will respond by forcing STO to the same logical level as STI. Detection of STI and STO being equal signals the DAU that the data lines may now be altered and that STI may be changed for another byte transfer when the new data is ready.

For a write operation, the roles of STI and STO are reversed. The I/O Controller will change STO when it places data on the data lines. When the DAU detects a difference between STI and STO it will deskew STO, store the data and check for a terminate condition. If a terminate condition exists, the DAU, when ready, will respond by setting the TMI line and performing the dialogue described for TMI. If a terminate condition does not exist the DAU, when ready, will respond by forcing the STI line to the same logical level as STO. In either case, the DAU may hold up the dialogue at this point by delaying the change of STI or TMI if necessary. Detection of STI and STO being equal signals the I/O that the data lines may now be altered and that STO may be changed for another byte transfer when the new data is ready.

STI will be forced to the reset state by the DAU while OPI or OPO are reset.

3.2.6.4 STROBE OUT (STO)

The Strobe Out line is used by the I/O Controller to indicate its participation in the dialog on the interface. This line extends from the I/O Controller to the DAU.

For a write operation, the STO line may be changed only if STI and STO are at the same logical level. A change of STO by the I/O when data is ready will cause the DAU to detect a difference between STI and STO, which will indicate to the DAU that data is available on the data lines. To obtain the data, the DAU will deskew STO a minimum of 40 nanoseconds, then store the data and check for a terminate condition. If a terminate condition exists, the DAU, when ready, will respond by setting the Terminate In (TMI) line and performing the dialogue described for TMI.

If a terminate condition does not exist, the DAU, when ready, will respond by forcing STI to the same logical level as STO. Detection of STI and STO being equal signals the I/O Controller that the data lines may now be altered and that STO may be changed for another byte transfer dialogue when the new data is ready.

For a read operation, the roles of STI and STO are reversed. The DAU will change STI when it places data on the data lines. When the I/O Controller detects a difference between STI and STO it will deskew STI, store the data and check for a terminate condition.

If a terminate condition exists, the I/O, when ready, will respond by setting the TMO line and performing the dialogue described for TMO. If a terminate condition does not exist the I/O Controller, when ready, will respond by forcing the STO line to the same logical level as STI. In either case, the I/O may hold up the dialogue at this point by delaying the change of STO or TMO if necessary. Detection of STI and STO being equal signals the DAU that the data lines may now be altered and that STI may be changed for another byte transfer when the new data is ready.

STO will be forced to the reset state by the I/O Controller while OPO or OPI are reset.

3.2.6.5 TERMINATE OUT (TMO)

Terminate Out is used by the I/O Controller to end the current dialogue whether a read or a write. The TMO line extends from the I/O Controller to the DAU and is used in conjunction with the TMI line to control the PSI terminate sequence.

For a write operation, TMO can indicate one of the following conditions:

- o For a data transfer, TMO implies that a byte being transferred is the last byte of a field and the data count is exhausted. Since data chaining is transparent to the DAU, TMO rises only when the count of the last data chained DCW in the data chain array is exhausted. Due to an error, the transfer may be terminated prematurely.

- o For a command or I/O instruction transfer, TMO indicates that the transfer is complete with the byte being sent on the current transfer and that no more bytes are forthcoming.

- o For any transfer, if the Terminate In line has been received with the most recent byte from the DAU. TMO will be sent to the DAU after data has been deskewed.

3.2.6.6 TERMINATE IN (TMI)

Terminate In is used by the DAU to end the current dialogue, whether a read or a write. The TMI line extends from the DAU to the I/O Controller.

For a write operation, TMI can indicate one of the following conditions:

- o For a data transfer, TMI indicates that the byte being received is the last byte the DAU will accept for this transfer sequence.

- o For a command transfer, TMI indicates that the byte being received is the last byte required by the DAU.

- For any transfer, if the Terminate Out line has been received with the most recent byte from the I/O Controller, TMI will be sent to the I/O after data is deskewed by the DAU.

For a read operation, TMI can indicate one of the following conditions:

- For a data transfer, TMI indicates that the byte being transferred is the last byte available from the media for this data transfer sequence, or that the DAU is temporarily suspending the data transfer sequence. The suspended sequence may be resumed by using the appropriate service code.

- For a service code sequence, TMI indicates that the byte being transferred is the last byte in the service code sequence.

- For any transfer, the Terminate Out line has been received in answer to a change of the STI line for the most recent byte to the I/O Controller. TMI will be sent to the I/O Controller.

3.2.6.7 CHANNEL PROGRAM WAITING (CPW)

Channel Program Waiting indicates to the DAU that a channel program (DCW list) is waiting. The CPW line extends from the I/O Controller to the DAU.

A command received by the I/O Controller results in the I/O setting the CPW line to a logical one state. As soon as the DAU is able, it issues an Initiate New Channel Program service code to start the new channel program, and the I/O then begins transferring a logical channel number and the first IDCW to the DAU. CPW remains up until no new channel programs remain to be initiated. CPW resets when the last entry in the initiation queue is satisfied.

3.2.6.8 IOC INSTRUCTION WAITING (IIW)

IIW indicates to the DAU that the I/O Controller has a fault byte or instruction to send. The IIW line extends from the I/O Controller to the DAU. The DAU must, upon recognizing that IIW is high, send a service code to the I/O Controller at its next service code sequence opportunity. The I/O then sends the IOC instruction to the DAU, accompanied by a logical channel number if applicable.

If a data transfer is in progress at the time IIW rises, it should continue to its normal termination point. If however, the I/O Controller requires immediate transmission of an IOC instruction, it will terminate data transfer by sending TMO.

If IIW and CPW are up at the same time, the DAU must service IIW first. When IIW is high, the DAU must service it before any other service code sequence it wishes to send.

If IIW is to be set during a service code or data transfer sequence, it must be set prior to or simultaneously with the resetting of TMO.

IIW will reset when SCI is set for the transmission of the Initiate IOC Instruction service code or whatever service code is used to accomplish this action. If the IIW line is active at the end of a service code sequence, the DAU is to assume that any transfers called for by the service code will not occur.

3.2.6.9 OPERATIONAL OUT (OPO)

Operational Out indicates the state of the I/O Controller. When activated, it indicates that the I/O is operational and capable of communication with the DAU. When deactivated, it means that the I/O is powered down or is in a state that makes it incapable of responding on the PSI interface. The OPO line extends from the I/O Controller to the DAU.

When the PSI is physically disconnected from the I/O Controller, this line is deactivated. This line may be activated or deactivated at any time. If this line is deactivated while dialogue is in progress, the DAU ceases the dialogue on the PSI. If OPO is down, the DAU should not attempt any dialogues on the PSI.

3.2.6.10 OPERATIONAL IN (OPI)

Operational In indicates the DAU operational state to the I/O Controller. The OPI line extends from the DAU to the I/O Controller.

When activated, OPI indicates that the DAU is operational and capable of communication with the I/O Controller. When deactivated, it means that the DAU is powered down or is in a state that makes it incapable of responding on the PSI interface.

The Operational In line will be deactivated if it is set when the I/O Controller activates the Reset Out (RSO) line. The OPI line will remain deactivated until resetting (initialization) and any self diagnosis activities intrinsic to initialization are completed.

When the PSI is physically disconnected from the DAU, this line is deactivated. This line may be activated or deactivated at any time except it may not be activated if RSO is high. If it is deactivated while some dialogue is in progress on the interface, the I/O Controller will cease the dialogue on the PSI interface.

3.2.6.11 RESET OUT (RSO)

The Reset Out line extends from the I/O Controller to the DAU. Reset Out resets and initialized the DAU to a known state. The RSO line is implemented as a pulse.

When RSO is raised, the affected unit will immediately cease dialogue on the PSI. While initialization is taking place in the DAU, the OPI line will be in the logical zero state. When initialization is complete and RSO has dropped, OPI can be raised to a logical one.

3.2.7 HARDWARE DESCRIPTION

3.2.7.1 DATA PATH (D0-7,P)

The data path lines are a one byte wide path, eight bits plus odd parity, that extends between the DAU and the I/O Controller.

The nature of the information on the data lines (data, service code, etc.) is determined by the dialog.

Data can be put on the data lines by either the I/O Controller or the DAU. Data is put on the data lines by the I/O Controller whenever the I/O changes the state of STO or sets TMO to a logical one on an output operation. Data is out on the data lines by the DAU whenever the DAU changes the state of STI or sets TMI to a logical one on an input operation. When the state of STO is changed during a write operation, the DAU detects a logical difference between STO and STI, accepts the data from the data lines and sets STI to the same level as STO. For the last data byte the I/O Controller sets TMO to a logical one. Upon reception of the TMO signal the DAU accepts the data from the data lines and sets TMI to a logical one. Upon reception of the TMI signal the I/O Controller will reset TMO. The DAU recognizes the reset of TMO and resets TMI.

A read operation takes place in the same manner with STI and TMI initiating a byte transfer instead of STO and TMO.

3.2.7.2 READ DATA PATH

Refer to Figure 3.2-5.

Read data enters the CI board from either the MP board (DMPDTA 0-7,P) or the SB board (RBUFFER-DTA 0-7,P). The MP board supplies controller data such as status, service codes, etc. The SB board supplies data from its buffer through the B-register. This data is primarily read data from the device. Buffer data is gated through the Read Register Switch if the CI board is in the shunt mode, otherwise, the MP data is transferred. Data is transferred from the Read Register to the Read Latch then to the selected PSI port transmitters and onto the PSI interface. Control signals are used to move the data along the read path.

3.2.7.3 LOAD READ REGISTER ($LD-RD-REG)

Refer to Figure 3.2-6.

$LD-RD-REG is produced by data transfers from the SB board B-register or by one of the following microprocessor commands:

- CMD-LD-RD-REG: Loads Data or Status information into the Read Register.

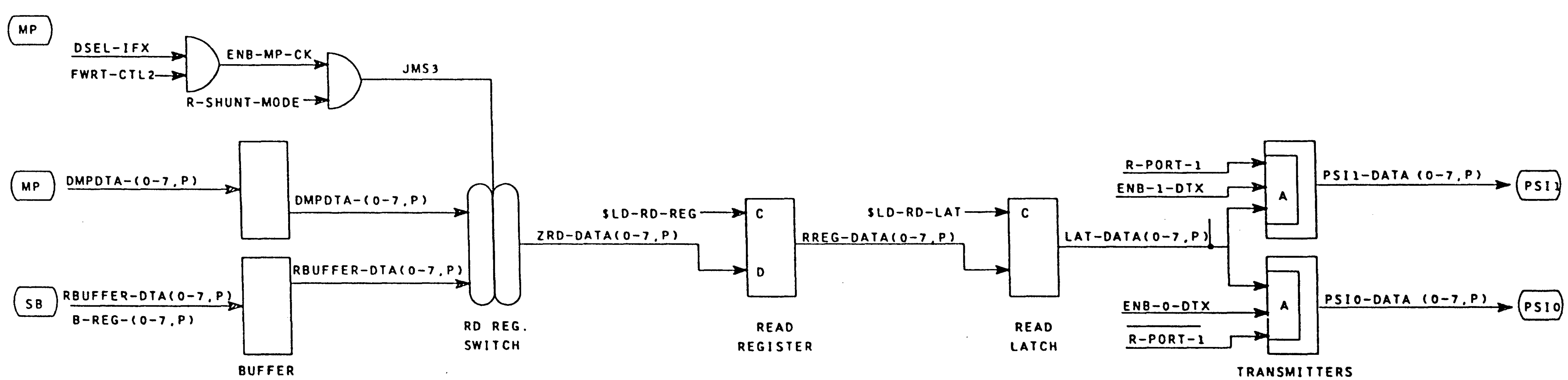


FIGURE 3.2-5. READ DATA PATH

- o CMD-LD-RD-REG-T: Loads data or status into the Read Register and sends terminate (TMI).

- o CMD-LD-RD-REG-SC: Loads service code into the Read Register. The logical channel number may also be loaded with this command.

- o CMD-LD-RD-REG-SCT: Loads service code or logical channel number into the Read Register. A terminate (TMI) will be sent with this command.

The Microprocessor Address Decode for each CI command is listed alongside these commands. Data transfers from the SB buffer are loaded into the Read Register by setting the B-register acknowledge flip-flop (FB-REG-ACK). The conditions to set this flip-flop are as follows:

- o The Read Register is empty ($\overline{\text{FRD-REG-FUL}}$) or is about to be emptied (FRD-SYNC).

- o The store board's B-register is full (FB-REG-FUL) and Read Shunt Stop is not set.

- o The CI board is in the read and shunt modes and the microprocessor has issued a Transfer Request (FXFRREQ).

3.2.7.4 READ REGISTER FULL RESET

Refer to Figure 3.2-6

The conditions that reset the Read Register Full flip-flop are:

- o Any Load Read Register command when the microprocessor is performing a read operation (FRD CTL1).

- o Upon sending/receiving a terminate to/from the I/O Controller (FSYNC-TRM-TXRX).

- o As data is transferred from the Read Register to the Read Latch (FRD-SYNC).

3.2.7.5 READ REGISTER TERMINATION

Read Register Terminate (FRD-REG-TRM) and Read Shunt Stop are set to terminate the read and to lock out further data transfers from the SB and MP boards. The microprocessor terminates transfers by issuing the Load Read Register Terminate or service code terminate commands.

The data transfer terminates when the last data byte has been sent (R-COUNT-LDED) and the SB board sends terminate (FB-REG-TRM).

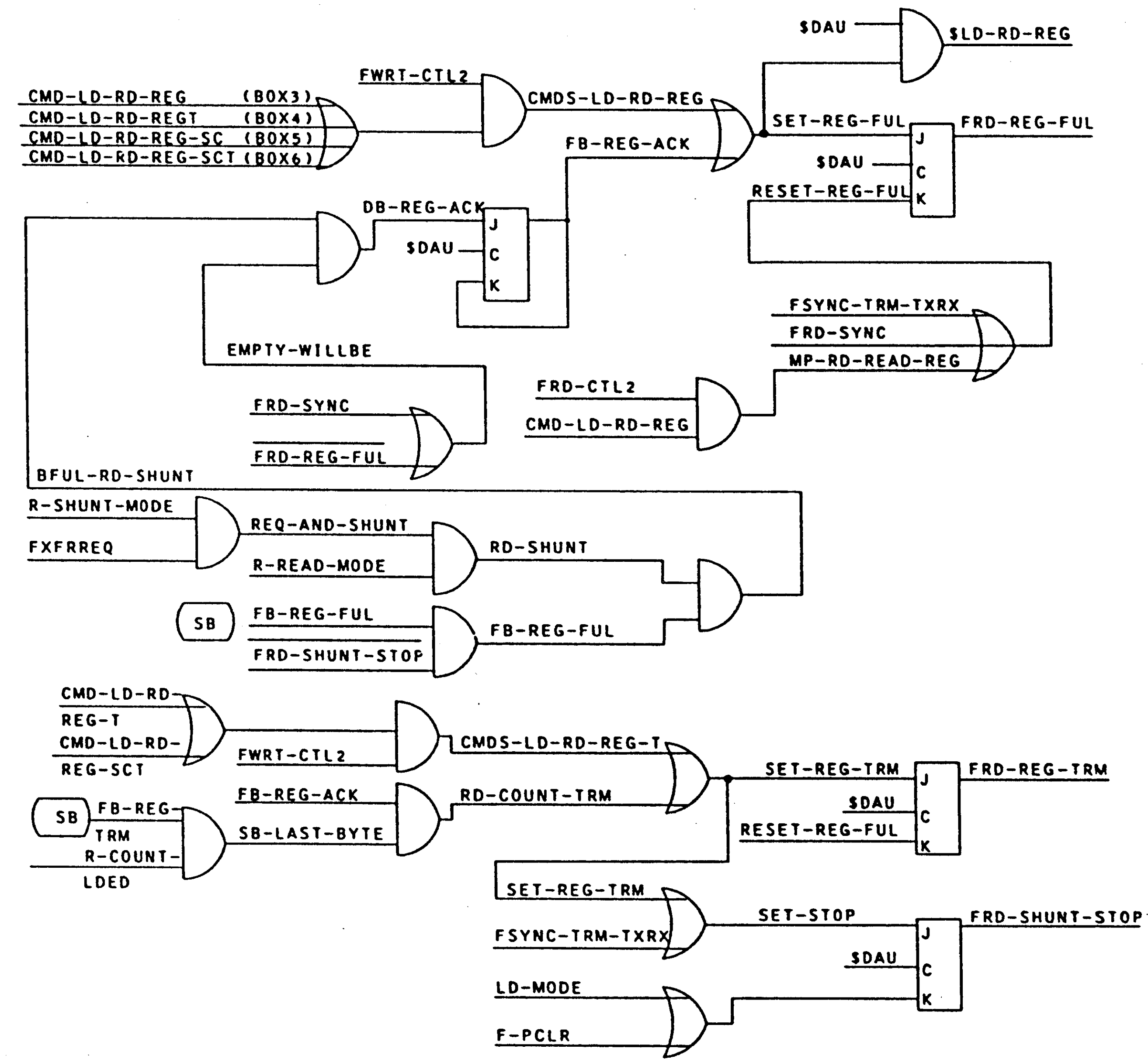


FIGURE 3.2-6. LOAD READ REGISTER CONTROL

3.2.7.6 READ LATCH CONTROL

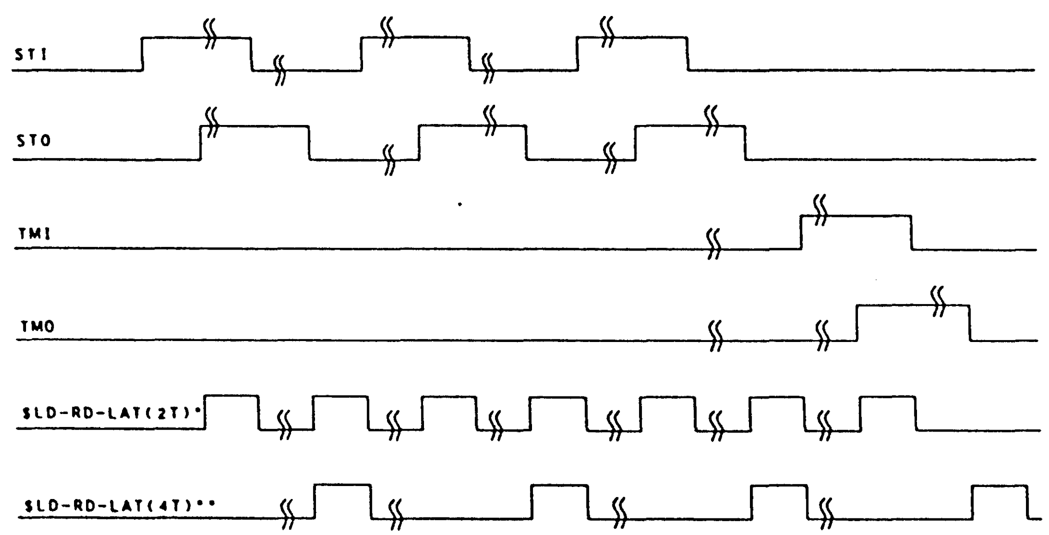
Refer to Figure 3.2-7.

Data is transferred from the Read Register to the Read Latch by $LD-RD-LAT. This signal is produced if the Read Register is full (FRD-REG-FUL) on the rise and fall of each Strobe Out (STO) signal when the DAU is connected to a 2-trip PSIA or as STO falls (SEL-STO) when connected to a 4-trip PSIA. Refer to Figure 3.2-8.

The top leg of the $LD-RD-LAT AND gate establishes whether a 2-trip or a 4-trip PSIA is employed in the disk subsystem. If the backpanel jumpers are not installed, the 2-trip logic is activated and the 4-trip logic is inhibited. The jumpers are installed when the DAU is connected to a 4-trip PSIA. The jumpers ground out the 2-trip PSIA logic. In 4-trip operation, Strobe Out (SEL-STO) must fall before data is transmitted. This is not required for 2-trip operation. The last byte is transferred to the Read Latch when Read Register Terminate (FRD-REG-TRM) sets and neither Terminate In (FTMI) or Terminate Out (SEL-TMO) are active.

$LD-RD-LAT is inhibited if one of the following conditions exists:

- o The Read Latch contains data already (FRD-LAT-FILED).
- o The Mode Register is being loaded (FLD-MODE).
- o Terminate has been sent or received (FTRM-RCD-SENT10).
- o The Read Register is empty (FRD-REG-FUL).
- o The DAU is waiting for a Service Enable Out (WAIT-SEO).



*$LD-RD-LAT(2T) = (SEL-STIEQSTO)+(SEL-TMIEQTMO·TMO)

**$LD-RD-LAT(4T) = (SEL-STIEQSTO·$\overline{\text{STO}}$)+(SEL-TMIEQTMO·$\overline{\text{SEL-TMO}}$)

FIGURE 3.2-7. LOAD READ LATCH TIMING (2T/4T)

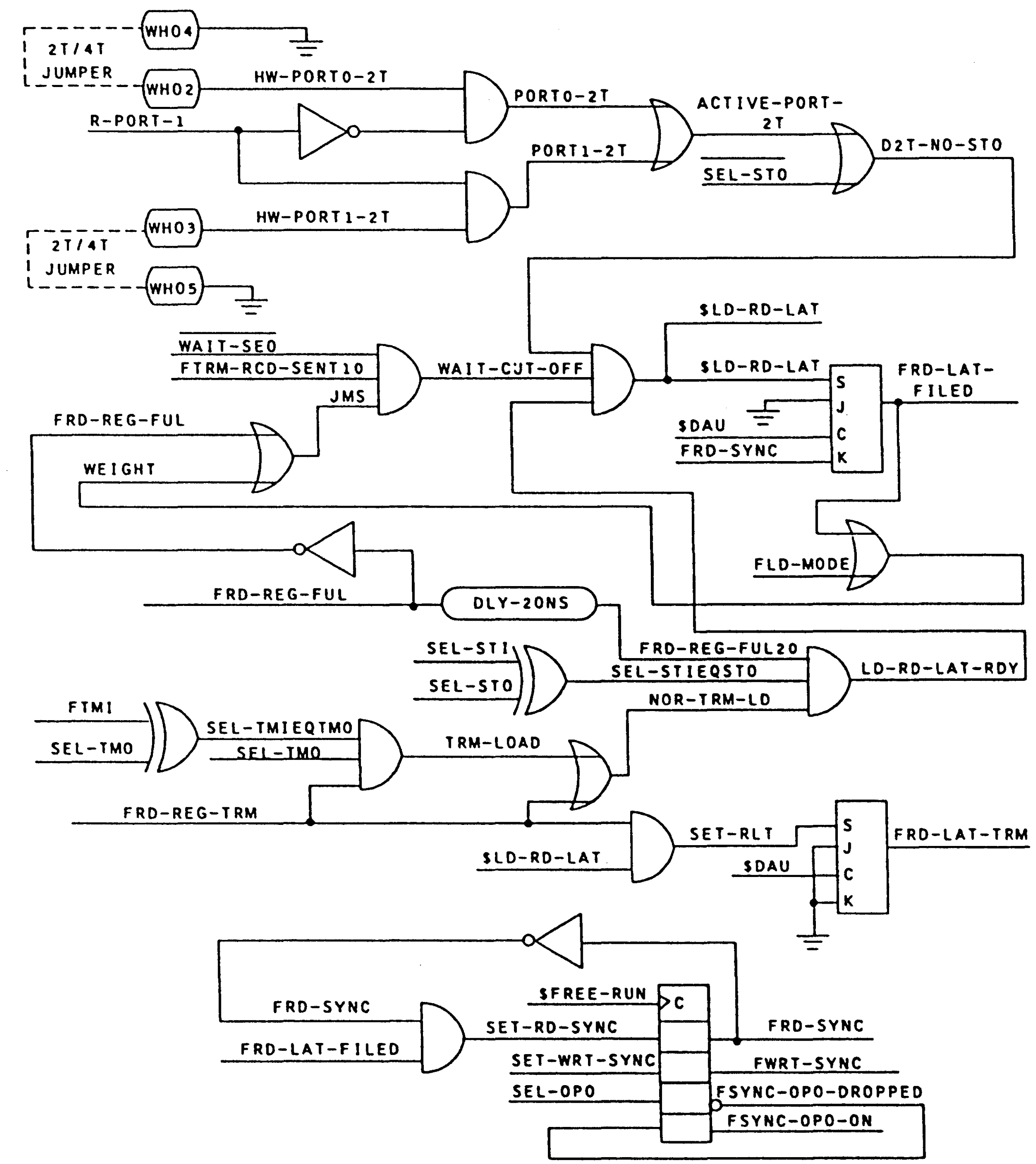


FIGURE 3.2-8. READ LATCH CONTROL

3.2.7.7 DATA TRANSMITTERS

Refer to Figure 3.2-9.

The appropriate Data Transmitters are enabled depending upon whether the microprocessor has selected PSI0 (R-PORT-1) or PSI1 (R-PORT-1) and which Transmitter Enable signal (ENB-0-DTX or ENB-1-DTX) is active.

A Transmitter Enable signal is generated if Operation Out is present at the respective port (either PSI0-OPO or PSI1-OPO), the CI board is online (F-ON-LINE) and in the read mode (R-READ-MODE).

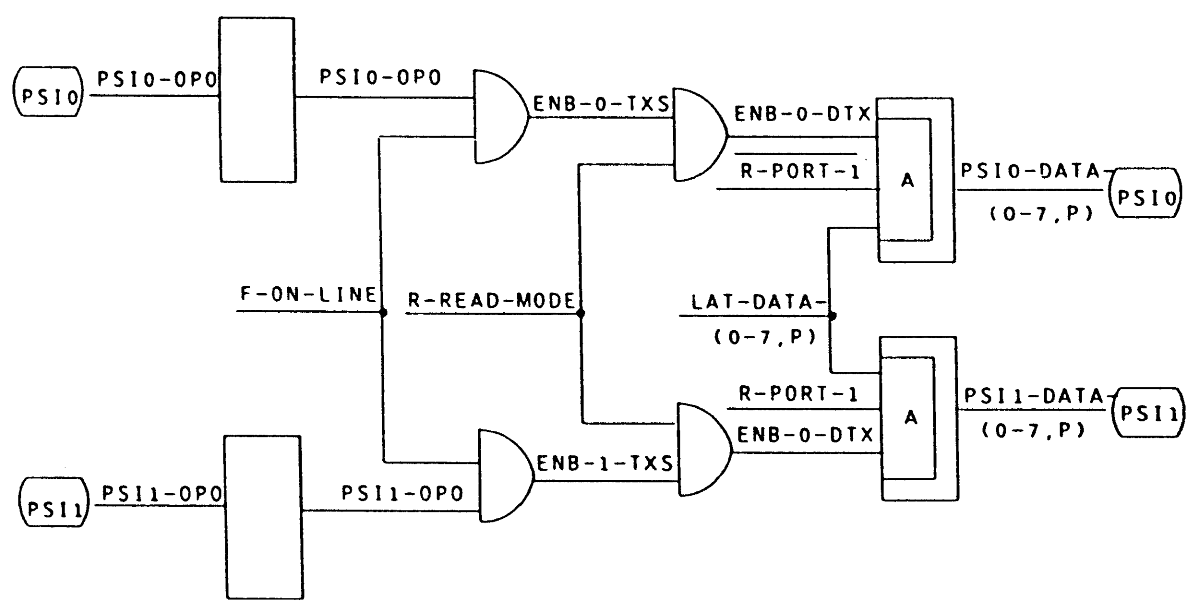


FIGURE 3.2-9. DATA TRANSMITTERS

3.2.7.8 CONTROL SIGNAL TRANSMITTERS

Refer to Figure 3.2-10.

This figure shows the Control Signal Transmitters. These signals allow the CI board to communicate with the desired PSI interface.

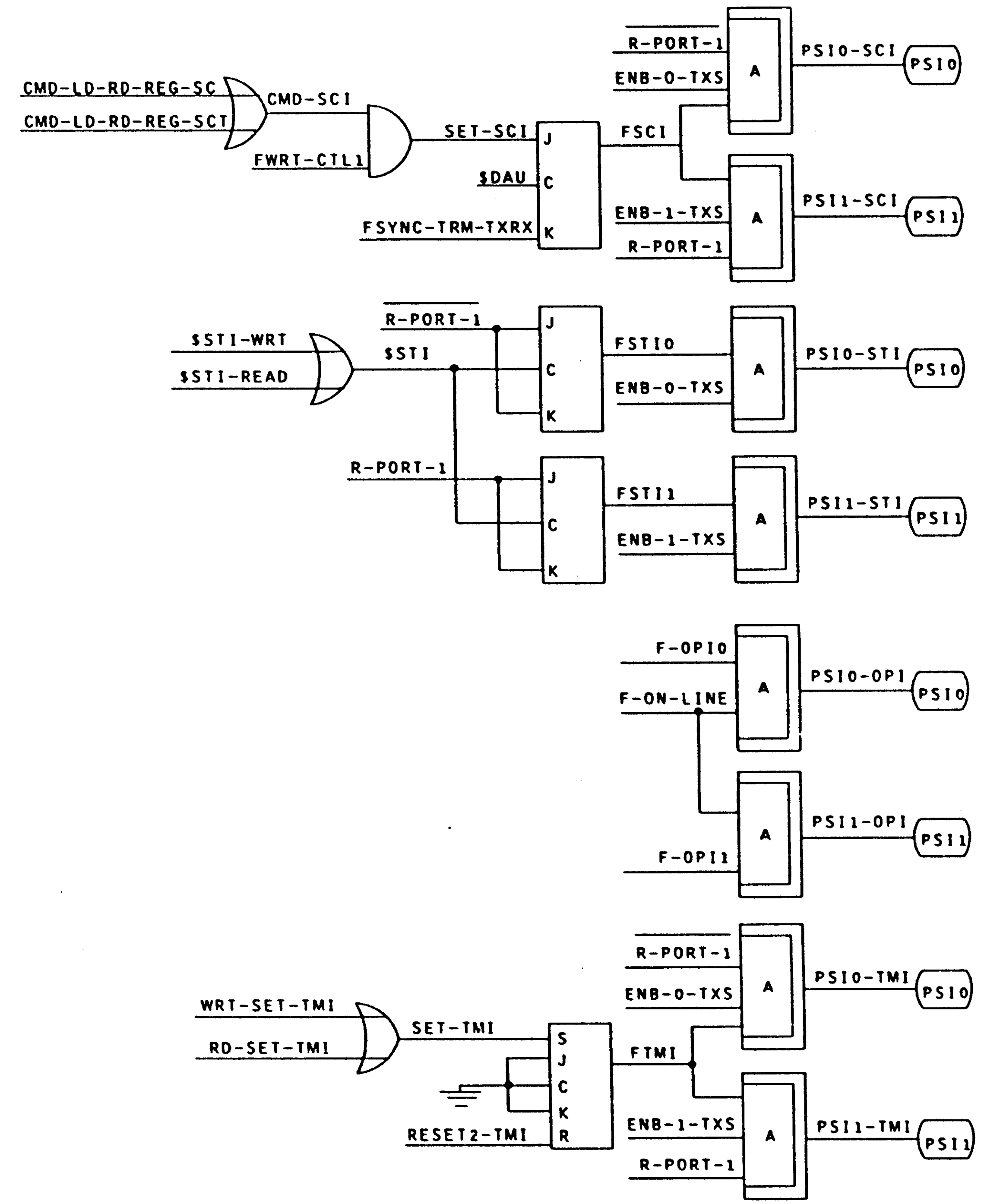


FIGURE 3.2-10. CONTROL SIGNAL TRANSMITTERS

3.2.7.9 CONTROL SIGNAL RECEIVERS

Refer to Figure 3.2-11.

The Control Signal Receivers are enabled when the microprocessor places the DAU online (F-ON-LINE) and the OPO signal is present from the respective Port

The outputs from the Control Signal Receivers are then sent to 1 of 2 or 1 of 4 selectors to generate the select signals. The exceptions are the PSI0-CPW and PSI1-CPW signals. These two signals go directly to the microprocessor readout 1 of 8 select switch and are read as PSI Status.

The PSI0-RSO and PSI1-RSO signals are ORed together on the CI board and sent to the MP board. This causes the DAU self-test to be run and the DAU to be initialized to a known state.

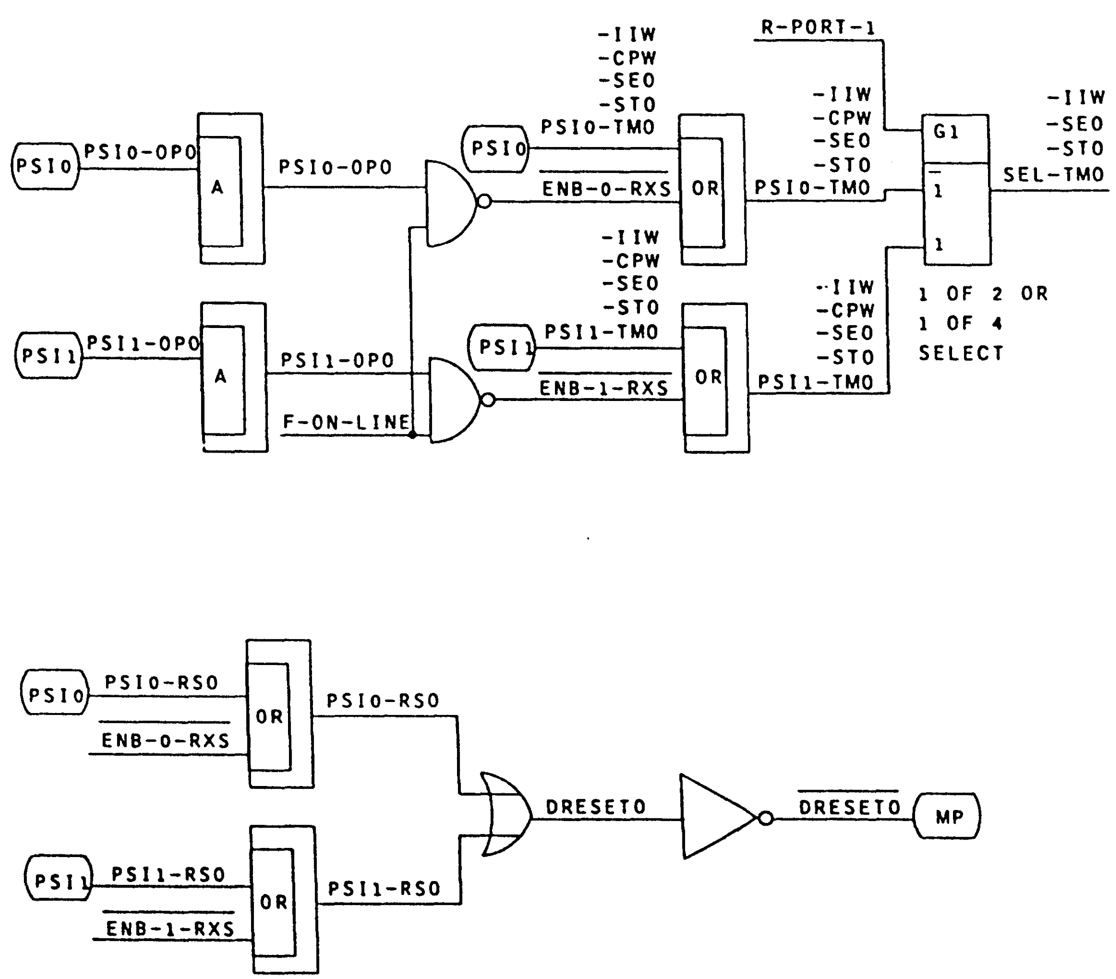


FIGURE 3.2-11. CONTROL SIGNAL RECEIVERS

3.2.7.10 WRITE DATA PATH

Refer to Figure 3.2-12.

System data is loaded into the Write Latch from either PSI0 or PSI1 depending on which port the microprocessor has selected (R-PORT-1 or R-PORT-1).

Under T&Ds, the data from the Read Latch [LAT-DATA-(0-7,P)] is wrapped around to the Write Latch. This is accomplished by setting the internal wrap bit in the T&D Register and placing the DAU in both the write and read modes.

Write data passes through the Write Register, Pad Switch, Buffer, and on to the store board (SB). As data is transferred from the Write Latch, parity is generated. This is compared with the parity bit received with the data. If the two parity bits are not equal, a Write Latch Error Signal is generated.

3.2.7.11 LOAD WRITE LATCH

Refer to Figure 3.2-14.

The Write Latch is loaded by the signal $LD-WRT-LAT which is generated by a 4-input NAND gate. The lower input to the NAND gate (ABORT-TRM-TXRX) is used to inhibit the loading of the Write Latch if it is already loaded (FWRT-LAT-FILED10), or the microprocessor has aborted the write due to an error (FWRT-ABORT).

The third input (R-WRT-MODE) indicates the CI board must be in the write mode.

The top two inputs to the NAND gate supply the timing for $LD-WRT-LAT. This timing depends on whether the CI board is in the 2-trip or 4-trip mode of operation and the state of interface signals STO, STI, TMO and TMI. Refer to Figure 3.2-13 for Load Write Latch timing diagram.

For 2-trip operations, normal data transfers (not last byte) are based on STI not equal to STO delayed (SEL-STIEQSTO20) and the port jumpers removed (ACTIVE-PORT-2T). When these conditions are met, signal D2T-STO-LOAD is generated. The last byte is loaded by TMI not equal to TMO delayed (SEL-TMIEQTMO20), and TMO active (SEL-TMO). These conditions produce signal D2T-TMO-LOAD.

For 4-trip operations, normal data transfers are based on STI not equal to STO delayed (SEL-STIEQSTO5) and STO not (SEL-STO). These conditions produce signals D4T-STO-LOAD and D2T-NOSTOTMO. The last byte is loaded by TMI not equal to TMO delayed (SEL-TMIEQTMO20) and TMO has fallen (SEL-TMO). These conditions produce signals D2T-TMO-LOAD and D2T-NOSTOTMO.

3.2.7.12 LOAD WRITE REGISTER

Refer to Figure 3.2-14.

Each $LD-WRT-LAT sets the Write Latch Filed flip-flop (FWRT-LAT-FILED) to denote that the Write Latch is full. FWRT-LAT-FILED is used to generate SET-WRT-SYNC. The other conditions needed to produce SET-WRITE-SYNC are:

- o Not attempting to unload the Read Latch (SET-RD-SYNC).
- o Write sync is reset (FWRT-SYNC).
- o The Write Register is empty now (FWRT-REG-FUL), or the SB board has the last data byte and its OK to load the Write Register (FWRT-REG-ACK).

SET WRITE SYNC sets FWRT-SYNC which in turn, resets FWRT-LAT-FILED and generates $LD-WRT-REG to strobe the data into the Write Register.

Refer to Figure 3.2-15.

FWRT-SYNC also sets the Write Register Full flip-flop (FWRT-REG-FUL) to provide the handshake signal ACT-WT-REG-FUL to the SB board. When the SB board receives the data byte, it will respond with the acknowledge signal (FWRT-REG-ACK) to reset FWRT-REG-FUL.

3.2.7.13 PAD SWITCH CONTROL

System data is gated through the pad switch as long as WRT-SECT-PAD is low. Padding is invoked when the system is sending device data and terminates the transfer prior to reaching a sector boundary. This condition is detected on the SB board and causes WRT-SECT-PAD to go high. WRT-SECT-PAD will finish filling the sector with zeros until a Write Sector Terminate (DWT-SEC-TRM) is received from the SB board.

WRT-SECT-PAD is generated if Transfer Request (FXFRREQ) and FPAD are set and the DAU is not writing in the absolute mode (RABS-WRT). FPAD sets on receipt of Write Register Acknowledge (FWRT-REG-ACK) from the SB board, System Terminate (FWRT-REG-TRM), and Write Request Reset Not high (WRT-REQ-RESET).

WRT-REQ-RESET is held high because Absolute write (RABS-WRT) is not enabled and the SB board has not detected the end of the sector boundary (DWT-SEC-TRM). When sector padding is completed, DWT-SEC-TRM goes high and WRT-REQ-RESET goes low to reset FPAD.

From the pad switch, zeros pass through the buffer and on to the SB board, providing the microprocessor is still requesting data transfers (FXFRREQ) in the shunt mode.

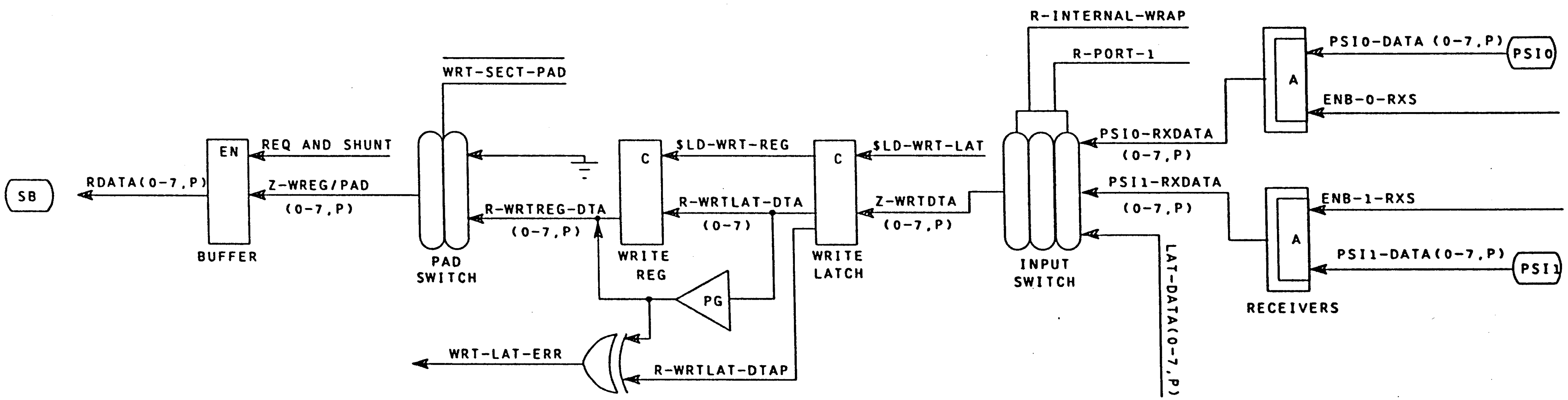


FIGURE 3.2-12. WRITE DATA PATH

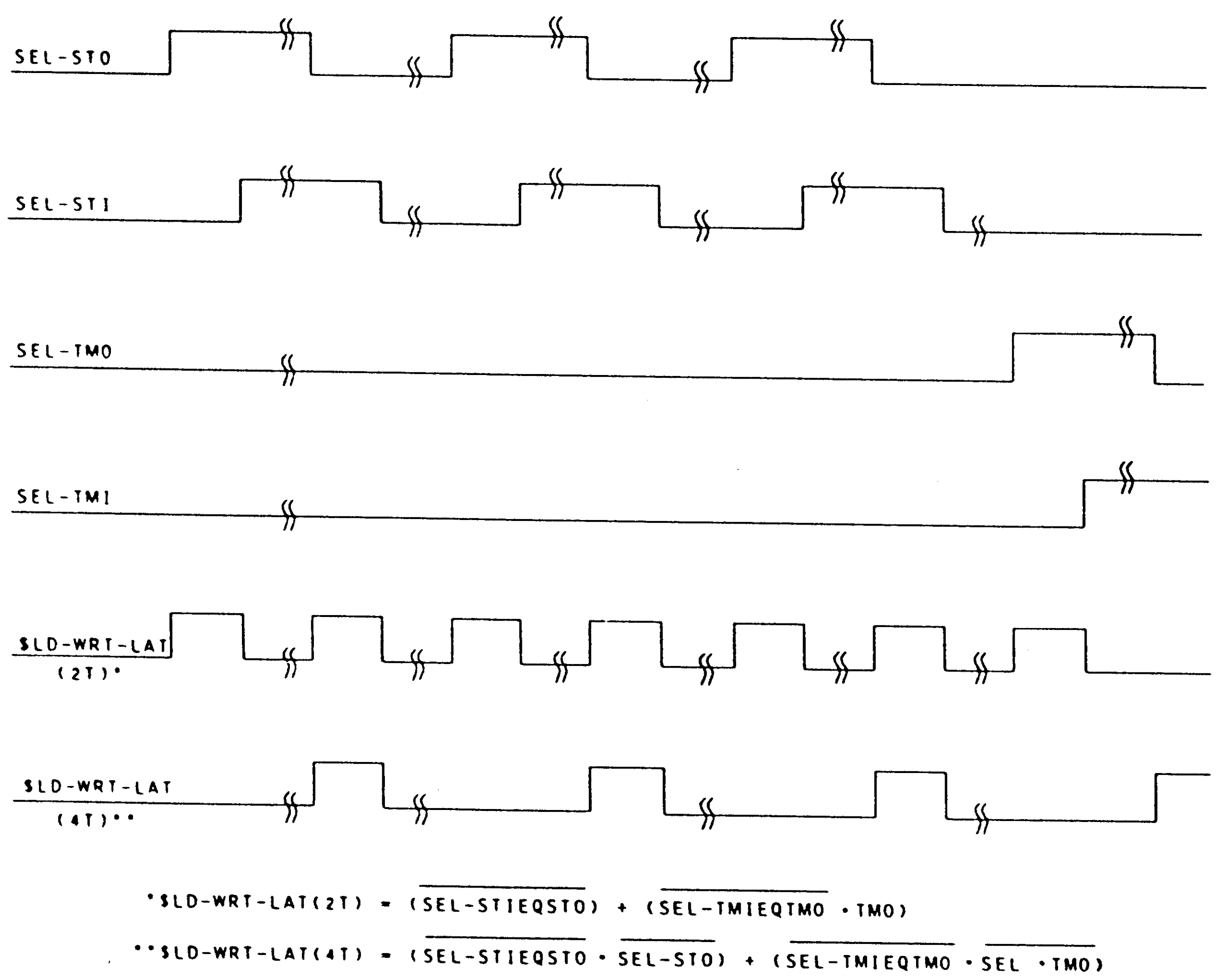


FIGURE 3.2-13. LOAD WRITE LATCH TIMING (2T/4T)

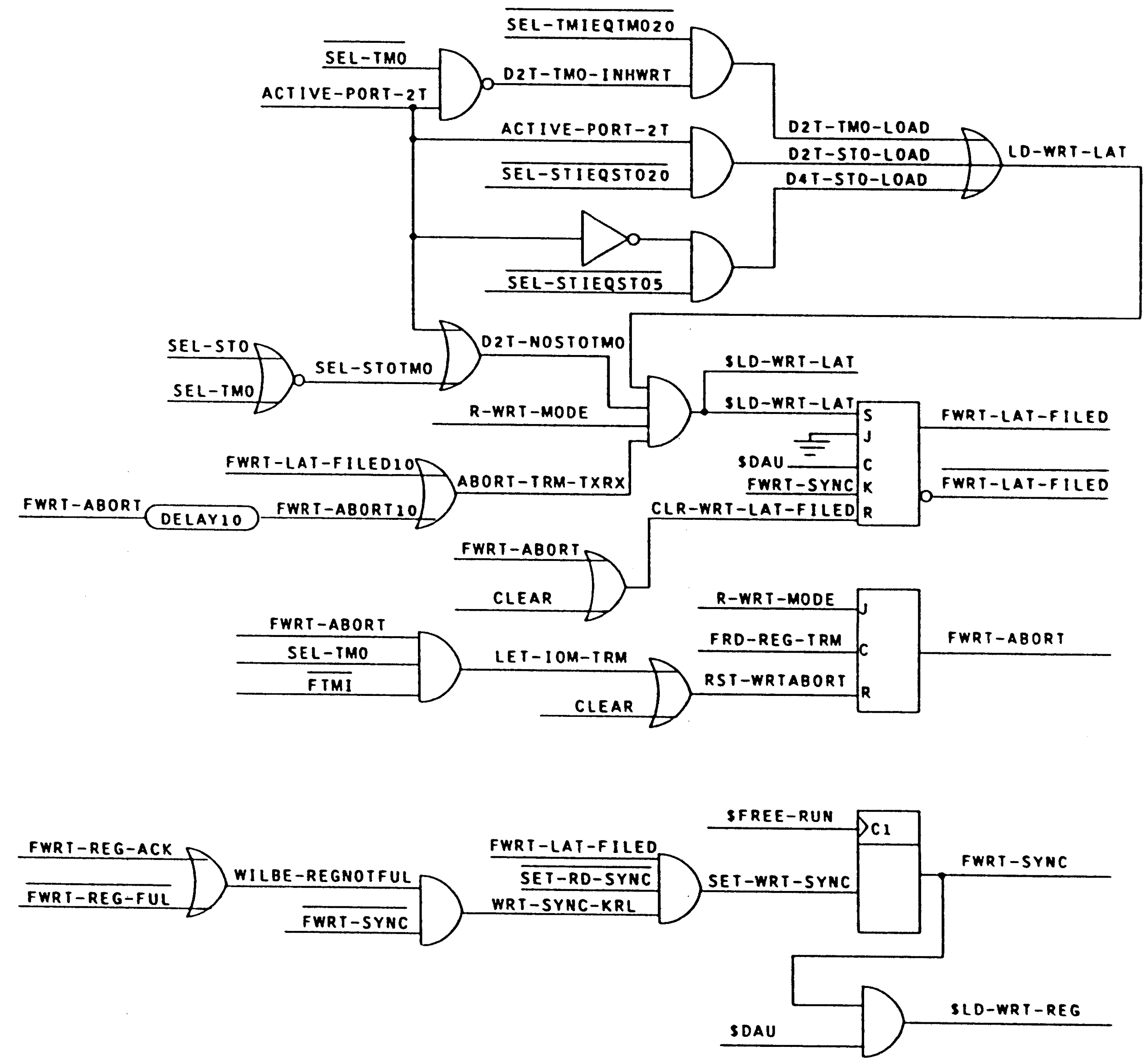


FIGURE 3.2-14. WRITE LATCH CONTROL

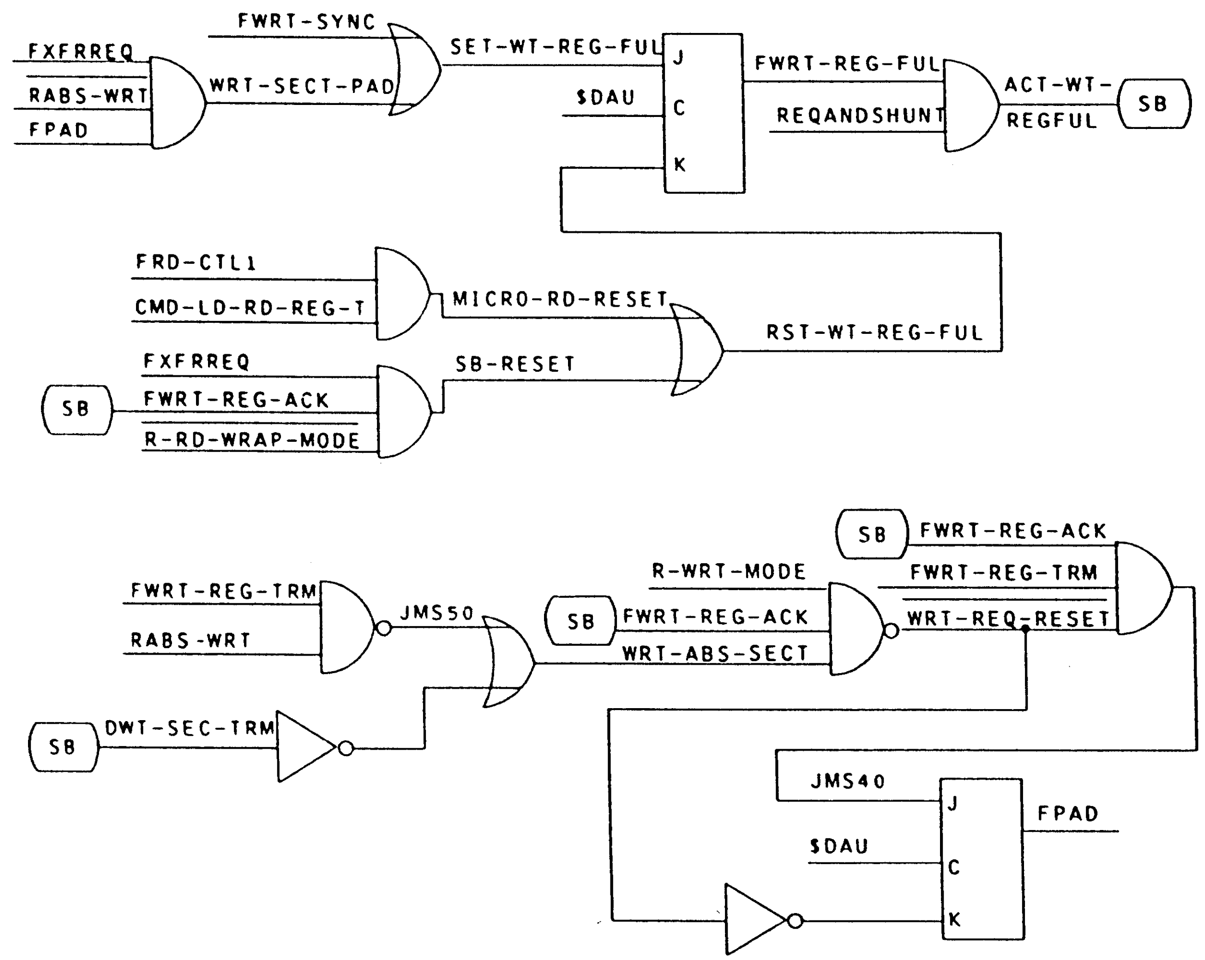


FIGURE 3.2.15. WRITE REGISTER CONTROL

3.2.7.14 TERMINATE

Refer to Figure 3.2-16.

The Write Latch Terminate flip-flop (FWRT-LAT-TRM) will set when the system terminates (SEL-TMIEQTM020) normal data transfers to the device as the last byte is loaded into the Write Latch ($LD-WRT-LAT). Then Write Sync (FWRT-SYNC) comes true to load the last byte into the Write Register and sets FWRT-REG-FUL and Write Register Terminate (FWRT-REG-TRM). If the last byte fills out the current sector, DWT-SEC-TRM will be ANDed with these two signals to generate ACT-WT-TRM. This signal is sent to the SB board and indicates that the system terminated on a sector boundary and padding is not needed.

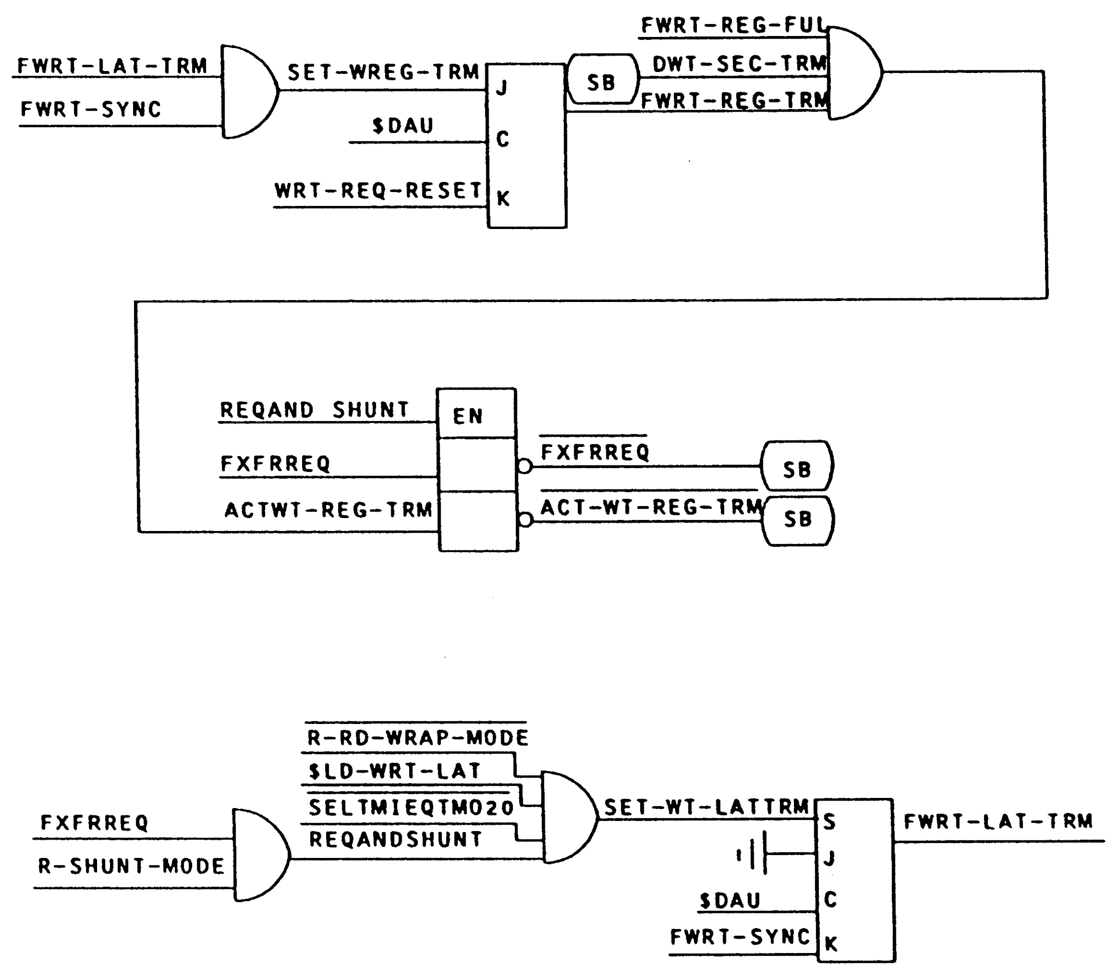


FIGURE 3.2-16. TERMINATE

3.3 MICROPROCESSOR (MP)

3.3.1 MP OVERVIEW

The MP board contains the microprocessor and its associated logic as well as some spillover of the sequencer logic. Only the microprocessor and its associated logic will be discussed here, the sequencer logic will be discussed under the SE board paragraphs.

The microprocessor board is the control element of the DAU subsystem. It controls the random logic contained on the other DAU boards (CI, SE, SB and EI) by establishing the proper conditions and states, initiating processes, and monitoring the progress and results of those processes.

In order to exert this control, the microprocessor has the ability to read and write various registers on each board. In addition, the microprocessor can read and write various registers and peripherals on its own board. This includes the following:

- o 32K of RAM for operational firmware and data
- o 16K of EPROM for T&D and maintenance firmware
- o Intel 8253 Programmable Interval Timer (PIT) to provide various timing signals
- o Intel 8259 Programmable Interrupt Controller (PIC)
- o Intel 8251A Programmable Communication Interface (USART) to communicate with a terminal for maintenance and testing purposes
- o A 16-bit register, the contents of which are compared with the address bus in order to provide a "stop on address" signal

3.3.2 MP BLOCK DIAGRAM

Refer to Figure 3.3-1.

This figure is a Major Block Diagram of the microprocessor board (MP). This figure consists of the microprocessor chip and its supporting chips. These chips are discussed in the following paragraphs.

3.3.3 MP ADDRESSING

Although the 8088 microprocessor is capable of addressing up to one megabyte, the addressing scheme is simplified by restricting it to 64K. This means that the upper four address bits (A16-A19) are not used.

TABLE 3.3-1. MICROPROCESSOR ADDRESS SPACE

MSB 0 7	LSB 8 15	HEX	CONTENTS
0000 0000 TO 0111 1111	0000 0000 TO 1111 1111	0000 TO 7FFF	32K RAM
1000 0000 TO 1010 1111	0000 0000 TO 1111 1111	8000 TO AFFF	-------
1011 0000 TO 1011 0000	0000 0000 TO 0001 1111	B000 TO B01F	CI-0 BOARD
1011 0000 TO 1011 0000	0010 0000 TO 0011 1111	B020 TO B03F	CI-1 BOARD
1011 0000 TO 1011 0000	0100 0000 TO 0101 1111	B040 TO B05F	SE BOARD
1011 0000 TO 1011 0000	0110 0000 TO 0111 1111	B060 TO B07F	SEQUENCER LOGIC ON MP BOARD
1011 0000 TO 1011 0000	1000 0000 TO 1001 1111	B080 TO B09F	SB BOARD
1011 0000 TO 1011 0000	1010 0000 TO 1011 1111	B0A0 TO B0BF	EI BOARD
1011 0000 TO 1011 0000	1100 0000 TO 1111 1111	B0C0 TO B0FF	-------
1011 0001 TO 1011 0001	0000 0000 TO 0001 1111	B100 TO B11F	MP BOARD
1011 0001 TO 1011 1111	0010 0000 TO 1111 1111	B120 TO BFFF	-------
1100 0000 TO 1111 1111	0000 0000 TO 1111 1111	C000 TO FFFF	16K EPROM

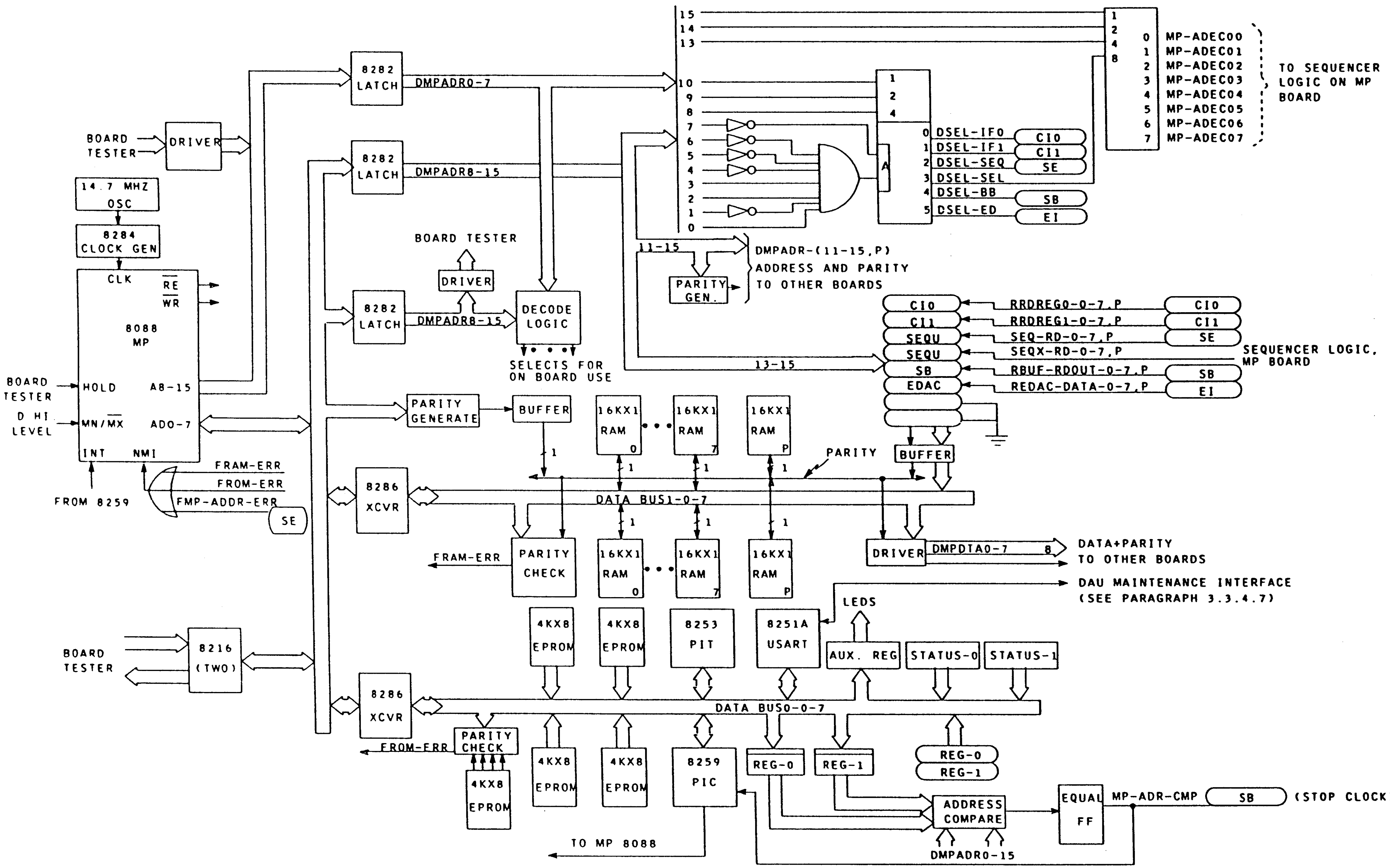


FIGURE 3.3-1. MP BOARD MAJOR BLOCK DIAGRAM

A breakdown of the microprocessor's 64K address space is shown in Table 3.3-1. Note that each board has 32 addressable locations, although not all 32 are used on every board.

A breakdown of the microprocessor board addresses is shown in Table 3.3-2.

TABLE 3.3-2. MICROPROCESSOR BOARD ADDRESSES

MSB 0 7	LSB 8 15	HEX	CONTENTS
1011 0001	0000 0000	B100	PROGRAMMABLE
1011 0001	0000 0001	B101	INTERVAL
1011 0001	0000 0010	B102	TIMER
1011 0001	0000 0011	B103	
1011 0001	0000 0100	B104	PROGRAMMABLE
1011 0001	0000 0101	B105	INTERRUPT CONTROLLER
1011 0001	0000 0110	B106	USART
1011 0001	0000 0111	B107	
1011 0001	0000 1000	B108	ADDRESS UPPER
1011 0001	0000 1001	B109	ADDRESS LOWER
1011 0001	0000 1010	B10A	STATUS 0 (READ ONLY)
1011 0001	0000 1011	B10B	UNUSED
1011 0001	0000 1100	B10C	AUXILIARY REG (WRITE)
1011 0001	0000 1101	B10D	UNUSED
1011 0001	0000 1110	B10E	STATUS 1
1011 0001	0000 1111	B10F	UNUSED

3.3.3.1 STATUS 0 (READ ONLY) (B10A)

0	1	2	3	4	5	6	7
MP TIMEOUT	BOARD PARITY ERROR	RAM PARITY ERROR	EPROM PARITY ERROR	MP ADDR PARITY ERROR	BIT 0 OF AUX REG	-----	BOARD TEST

Bit
0 Microprocessor time-out. This bit is set if firmware hangs up. Cleared by programming the interval timer.

1 Board parity error. Is set when bad data is received from any of the other DAU boards. It is cleared by a total or partial clear.

2 RAM parity error. Cleared by a total or partial clear.

3 ROM parity error. Cleared by a total or partial clear.

4 Microprocessor address parity error. The parity check is located on the SE board.

5 Bit 0 of the Auxiliary Register. Used for writing bad parity.

6 Not used.

7 Board Test. Equals 1 when in the board tester.

3.3.3.2 AUXILIARY REGISTER (WRITE ONLY) (B10C)

0	1	2	3	4	5	6	7
SET BAD PARITY	GREEN LED	RED LED	RED LED	RED LED	RED LED	RED LED	RED LED

Bit
0 If set, bad parity will be generated (for testing purposes).

1 Connected to a green LED on the free edge of the board. The LED lights after firmware is loaded into the microprocessor. It will be turned off with any hardware error.

2 Connected to a red LED on the free edge of the board. This LED will light if a hardware error is detected on the CI 0 board during self-test. It will also light when a seek command is being executed by the DAU.

3 Connected to a red LED on the free edge of the board. This LED will light if a hardware error is detected on the CI 1 board during self-test. It will also light when a write command is being executed by the DAU.

4 Connected to a red LED on the free edge of the board. This LED will light if a hardware error is detected on the store board during self-test. It will also light when a read command is being executed by the DAU.

5 Connected to a red LED on the free edge of the board. This LED will light if a hardware error is detected on the sequencer board during self-test. It will also light when a read-alter-rewrite command is being executed by the DAU.

6 Connected to a red LED on the free edge of the board. This LED will light if a hardware error is detected on the microprocessor board during self-test. It will also light when a terminate command is sent or received by the DAU.

7 Connected to a red LED on the free edge of the board. This LED will light if a hardware error is detected on the EDAC (EI) board during self-test. It will also light when an initiate command is received by the DAU.

NOTE: The above register is loaded by self-test firmware to indicate failures. All lights come on near the beginning of self-test and are used as a lamp check. The Auxiliary Register is reset by the same signal that resets the microprocessor. It is also set by the firmware to indicate the type of command being executed by the DAU. When firmware is in the idle loop the red lights will be counting (lights incremented in sequence) to indicate the idle loop.

3.3.3 STATUS 1 (0-3 READ, 4-7 WRITE) (B10E)

0	1	2	3	4	5	6	7
TIMER 0	USART TX RX READY	CI 0 ONLINE	CI 1 ONLINE	-----	PWR ON MCLR	ENB PIT	CLEAR ADD COMP

Bit

0 Runout of timer #0 of the interval timer.

1 USART transmit or receive ready. (the OR of these two signals from the Maintenance Terminal).

2 Interface board CI-0 online.

3 Interface board CI-1 online.

4 Not used.

5 Power on Master Clear.

6 Enable Programmable Interval Timer.

7 Clear address compare flip-flop.

3.3.3.4 ADDRESS BUSES

The address bus is latched via three 8282 octal latches. Two of the 8282's are connected to the microprocessor's address and data bus (AD0-7). The outputs of one are used on the MP board for addressing components on the board, RAM, EPROM, etc. The outputs of the other are split. Five of the bits are sent to the backpanel to be used to address various components on other boards. These are address bits 11 through 15. The other three bits (8-10) go to the board select logic, along with eight bits from the third 8282, connected to the micro's address bus. Using these 11 bits, the board select logic provides a unique board select signal for each of the other boards, plus a select signal for the sequencer logic located on the MP board.

3.3.3.5 DATA BUSES

There are two separate bidirectional data buses. Both are buffered and driven by an 8286 octal transceiver connected to the micro's address and data lines. The two buses are used primarily for loading purposes.

3.3.3.5.1 DATA BUS 0: This bus contains various micro peripherals and logic, which is basically everything except RAM and data to and from other boards.

3.3.3.5.2 DATA BUS 1: This bus handles RAM and data to and from the other boards. It also has parity associated with it, since a parity check is provided for both RAM and board data.

3.3.4 MP HARDWARE DESCRIPTION

This section separates the hardware of the MP board into different areas and describes the functionality and implementation of each.

3.3.4.1 8088 MICROPROCESSOR

The best way to describe the implementation of the microprocessor is to list the inputs and outputs of the chip. They are as follows:

3.3.4.1.1 INPUTS

PIN	NAME	CONNECTED TO:
17	NMI	A gate which OR's together RAM, EPROM, and microprocessor address parity errors. Signal will stay high until error flip-flops are cleared.

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PIN	NAME	CONNECTED TO:
18	INTR	The INT output of 8259 PIC.
19	CLK	The CLK output of the 8284 clock generator. Clock is provided to the 8284 via a 14.745600 megahertz oscillator. The CLK output of the 8284 is one-third (1/3) of its input frequency.
21	RESET	A signal which will go high during power up, when a command reset (RSO) is received from the PSI interface or when the Reset Switch on the Operator Panel is activated and the Online/Offline Switch is in the Offline position. Any of these actions causes the microprocessor to fetch and execute the self-tests.
22	READY	The output of the 8284 clock generator, but the inputs to the 8284 are not used.
23	^TEST	Ground.
31	HOLD	A free-edge pin so that the microprocessor can be put in HOLD for board test purposes. A pull-up resistor and inverter provide a low level to this input otherwise.
33	MN/^MX	+5V to establish minimum mode. Minimum mode refers to the fact that there is only one processor, hence there is no bus contention.

3.3.4.1.2 OUTPUTS

PIN	NAME	CONNECTED TO:
2-8,39	A8-15	One octal latch, and tristated with a driver of free-edge inputs. This allows the board tester to control these lines.
24	^INTA	The 8259 Interrupt Controller. It is also used in logic to enable Data Bus 0.
25	ALE	Logic used to latch the 8282 octal latches.
26	^DEN	Logic used to enable the 8286 data bus transceivers.
27	DT/^R	Logic to determine the direction of data flow through the 8286 bus transceivers.
28	IO/^M	Not connected.
29	^WR	All logic and peripherals that the microprocessor has the capability of writing to. Also tristated with a free-edge input so that the board tester can control this line.
30	HLDA	Not connected.
32	^RD	All logic and peripherals that the microprocessor has the capability of reading. Also tristated with a free-edge input so that the board tester can control this line.
34	^SSO	Not connected.
35-38	A16-19	Not connected.

3.3.4.1.3 BIDIRECTIONAL

PIN	NAME	CONNECTED TO:
9-16	A0-7	1. Two 8282 latches to demultiplex the address 2 Two 8286 transceivers to send and receive data 3. 8216 driver/receivers for board test purposes 4. A parity generate chip

3.3.4.2 RAMS

The MP board contains 32,768 bytes of RAM, organized as 32K X 9 bits. Eight bits are data and one parity bit. This is implemented using eighteen 16K X 1 RAM chips. Access times are fast enough so that no wait states are required. Bits 2 through 15 of the microprocessor's address go to all RAM chips. Bit 1 selects between the two sets of nine 16K X 1 chips. Parity is generated for each write to RAM, and is checked whenever information is read from RAM. A flip-flop (FRAM-ERR) is set and the signal NMI is generated in the event of a parity error. This flip-flop is reset by a total or partial clear.

3.3.4.3 EPROMS

The MP board contains 16,384 bytes of EPROM, organized as 16K X 9. Eight bits are data and one bit is parity. This is implemented using five 4K X 8 EPROM chips. Access times are fast enough so that no wait states are required. Four chips are used for data and the fifth is used for parity. Bits 4 through 15 of the microprocessor's address go to all EPROM chips. Bits 2 and 3 select between the four 4K X 8 chips. Parity is stored in the fifth EPROM.

Four parity bits are stored in each byte, one bit for each of the other four EPROMs. Bits 4 through 15 of the microprocessor's address go to this EPROM chip, and bits 2 and 3 control a separate switch to select the proper bit. Parity is checked whenever information is read from EPROM. A flip-flop (FROM-ERR) is set and a signal NMI is generated in the event of a parity error. This flip-flop is reset by a total or partial clear.

3.3.4.4 BOARD INPUT/OUTPUT DATA

Data to and from other boards is handled via Data Bus 1.

For data from the MP board to other boards, a driver is provided to send the bits to the backpanel. This driver is always enabled, as is a parity generator on this data. Other boards will only recognize this data if they have the proper board select, and if a write operation is in progress. A write operation is signaled by the presence of a write strobe (MPWR).

Data coming to the MP board from other boards is put through a 1 of 8 switch, and is buffered to Data Bus 1. Six of the switch positions are used, one for each of the other five boards and one for the sequencer logic on the MP board. Farity is checked whenever data is read. If an error occurred, a flip-flop (FBD-ERR) is set. This error signal is sent to the store board to generate a hardware error. The parity error flip-flop is reset by a total or partial clear.

3.3.4.5 8253 INTERVAL TIMER

The Interval Timer has three separate programmable counters, 0 through 2. The gate input of each is strapped to +5V. The CLK input of timers 0 and 1 come from a 4-bit counter which divides down the basic microprocessor clock. The runout of timer 0 sets bit 0 of status byte 1. In response, firmware updates the Time-In Q counters and RPS window. Also, runout of this counter increments the Auxiliary Register. This causes the red LEDs to increment, indicating that the DAU is in the Idle Loop.

The output of timer 1 is applied to the USART Transmitter/Receiver Clock inputs to control the rate which the USART character is transferred.

Timer 2 is used as an integrity check on the microprocessor. Its input is the output of timer 0, and its output is referred to as "microprocessor time out". Firmware loads this counter such that it will runout in approximately 0.45 seconds if firmware does not periodically reload it. Normally, it is reloaded periodically and should never runout unless firmware hangs up. Runout of this timer sets bit 0 in status byte 0 and drops OPI to the PSIA and OPO to the devices.

3.3.4.6 8259 INTERRUPT CONTROLLER

The INT output of the Interrupt Controller is tied directly to the INTR input of the microprocessor. The interrupt request inputs are as follows:

0 Address compare. This input will be latched high when the microprocessor reads or writes to the address contained in the address registers.
1 Hard errors from the SB, SE, CI, EI or MP boards.
2 Soft errors from the SE or SB boards.
3 Sequencer halt.
4 Hard errors from the SB, EI, CI, or MP boards of MP time-out (timer #2).
5 Hard or soft errors from the SE board.
6 Interface input FIFO output ready. This interrupt is the "OR" of these two signals from each interface board.
7 Timer interrupt, from timer 0 of the Interval Timer.

Interrupts 0 through 3 are dedicated to T&D functions.
Interrupts 4 through 7 are dedicated to firmware functions.
During normal operation firmware masks all interrupts except interrupt 4.

3.3.4.7 8251A USART (DAU MAINTENANCE INTERFACE)

The purpose of the USART is to provide visibility to the DAU via a terminal. The drivers and receivers associated with the USART were chosen for compatibility with the RS 423 interface standard. The USART outputs and inputs are connected to the left free edge. A -5V adapter is required for these drivers and receivers. The adapter is supplied as a special tool and plugs into the left free edge of the MP board. A description and instructions for use of this adapter is covered on drawing 58014349 (located behind the PARTS TAB).

3.3.4.8 ADDRESS COMPARE

Two 8-bit registers called "Address Registers" are provided for the microprocessor to write to. They are labeled REG-0 and REG-1. The contents of these registers are compared with the microprocessor's address bus. When the microprocessor reads or writes to the address contained in the address registers, the EQUAL flip-flop is set. The output of this flip-flop is sent to interrupt request 0 of the 8259 Interrupt Controller and to the SB board. It is used to stop the microprocessor and/or the DAU at a predetermined address.

The flip-flop is cleared by a total or partial clear, or by writing a Hex 01 to status byte 1 (address B10E).

3.3.4.9 BOARD TESTER LOGIC

Additional logic was included on the MP board to make it easier to test on the board tester. Drivers and receivers were placed so that the board tester can have access to the microprocessor's address and data buses via the free edge of the board. Various control lines are also brought in from the free edge in order to place the microprocessor in hold. The board tester is also given control of the RD, WR, DEN, DT/R and ALE outputs of the microprocessor.

3.3.4.10 OPERATOR PANEL INTERFACE

The following signals are exchanged between the MP board and the Operator Panel:

- o Power confidence (POWER-CONF*100) is received from the Operator Panel and is used to reset the microprocessor, the USART, and the Auxiliary Register during power-up or in case of a power failure.

- o Two signals are received (CI0-ON-LINE*000 and CI1-ON-LINE*000) one from each of two external switches, to signal on or off line.

They can be read out in status byte 1 (address B10E). These signals are routed through the CI boards, so that the microprocessor will read a zero if the corresponding CI board is not present, regardless of the state of the switch.

- o The above two signals are "ORed" together and firmware can then put the DAU on line by setting an online flip-flop on the specific CI board.

- o A signal is provided to the Operator Panel to indicate a nonoperational or trouble condition. This signal is bit 1 of the Auxiliary Register "ANDed" with the DAU-ON-LINE signal. This results in an output signal (DAU-TROUBLE*000) that indicates when there is trouble in an online DAU.

- o One signal is received from an external pushbutton switch (SWITCH-RESET*000) and is used to perform a reset and branch when the Online/Offline switch is online or execute the self-tests when Offline.

CAUTION

ACTUATION OF THE PUSHBUTTON WILL DESTROY FIRMWARE WHEN THE DAU IS OFFLINE.

3.4 STORE BOARD (SB)

3.4.1 SB OVERVIEW

Refer to the Block Diagram, Figure 3.4-1.

The basic function of the store board is speed matching between the PSIA and the disk device. This function is accomplished mainly by a buffer memory (called the store) made up of RAM chips. The store size is 16K bytes (nine 16K X 1 RAM chips).

There are two modes of addressing, absolute and sector. The absolute mode is used for formatting, loading firmware, transferring extended status, etc.

The sector mode is used for storing sectors of data to be written to or read from the device. Refer to the Store Maps, Figures 3-20 and 3-21. Note that the read or write is always referenced to the system. In write sector mode, except for T&D, the store contains no EDAC bytes.

The EDAC bytes are appended to the data via the EDAC board, EI, under control of the sequencer board, SE. In the 4XX or 500 modes, the sector size is 288 bytes, (4.5 bytes X 64 words). In the 501/509 modes, the sector size is 2304 bytes, (4.5 bytes X 512 words) of data. To facilitate sector address decode of the store, the 512 word mode consists of eight 64 word sectors.

In read sector mode, the EDAC bytes from the device are also read into the store. In the 500 read mode, the sector size is 288 bytes of data followed by six bytes of EDAC for a total of 294 bytes. In the 4XX read mode, the sector size is 288 bytes of data followed by seven bytes of EDAC for a total of 295 bytes. In this mode, the sync byte is contained in the EDAC generation and it is shunted to the Sync Byte Register on this board. The sync byte is used by the microprocessor in EDAC correction for the final EDAC check. In the 501 read mode, the sector size is implemented as eight 64 word sectors followed by six EDAC bytes to the last sector of data for a total of 2310 bytes, (8 X 4.5 X 64). The EDAC bytes are not sent to the system on normal read op-codes. Special op-codes are provided for test and diagnostics to receive the data and the EDAC bytes.

3.4.2 SB BLOCK DIAGRAM

Refer to Figure 3.4-1.

This figure is a Major Block Diagram of the SB board. It shows the data flow through the SB board as well as the major control logic. Basic data flow is from the Buffer Switch, through the A-register into memory or store. Data from memory go to the Read Register and on to the B-register.

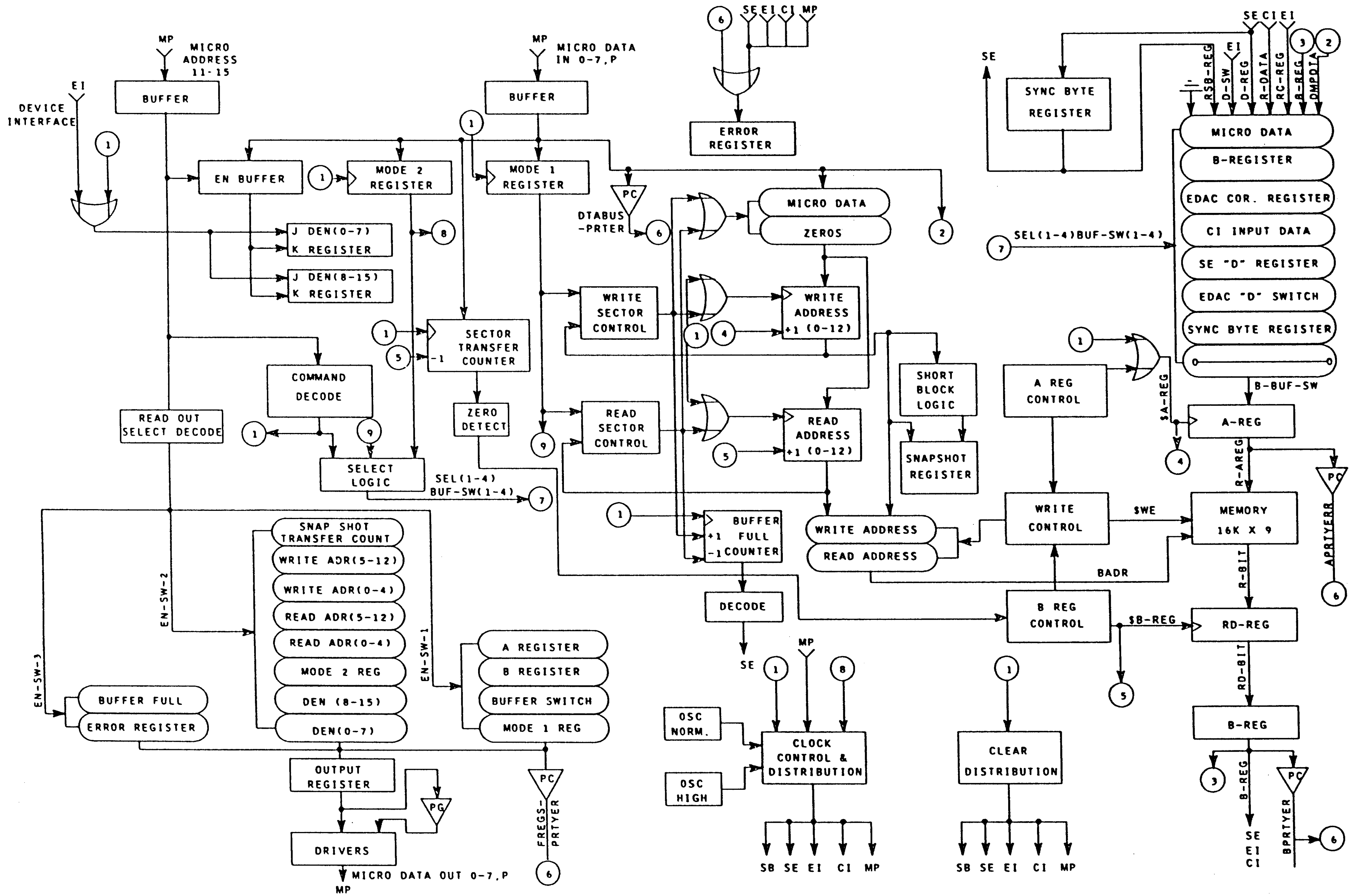


FIGURE 3.4-1. SB BOARD MAJOR BLOCK DIAGRAM

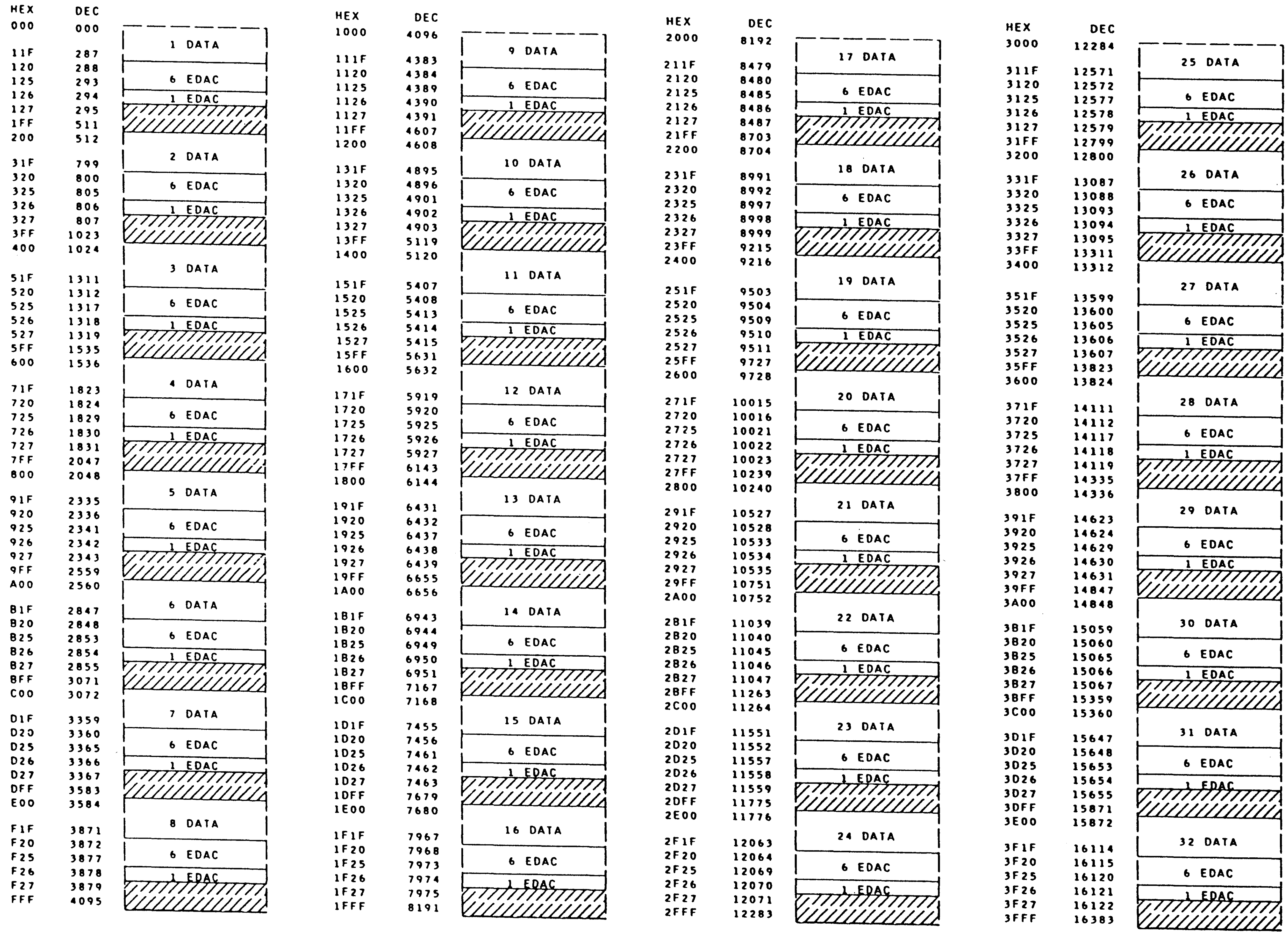


FIGURE 3.4-2. STORE BOARD MEMORY MAP (4XX & 50X MODES)

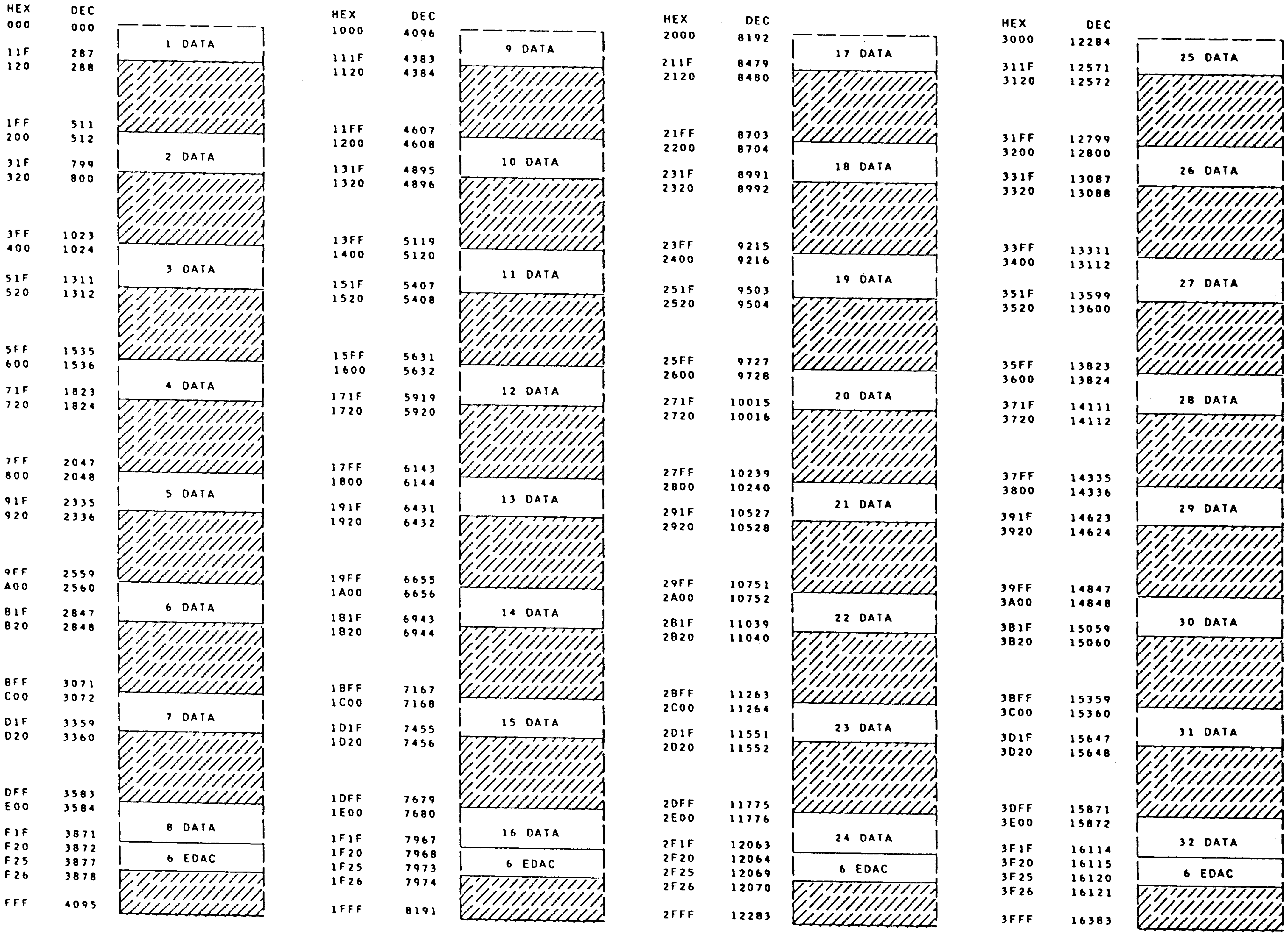


FIGURE 3.4-3. STORE BOARD MEMORY MAP (501 MODE)

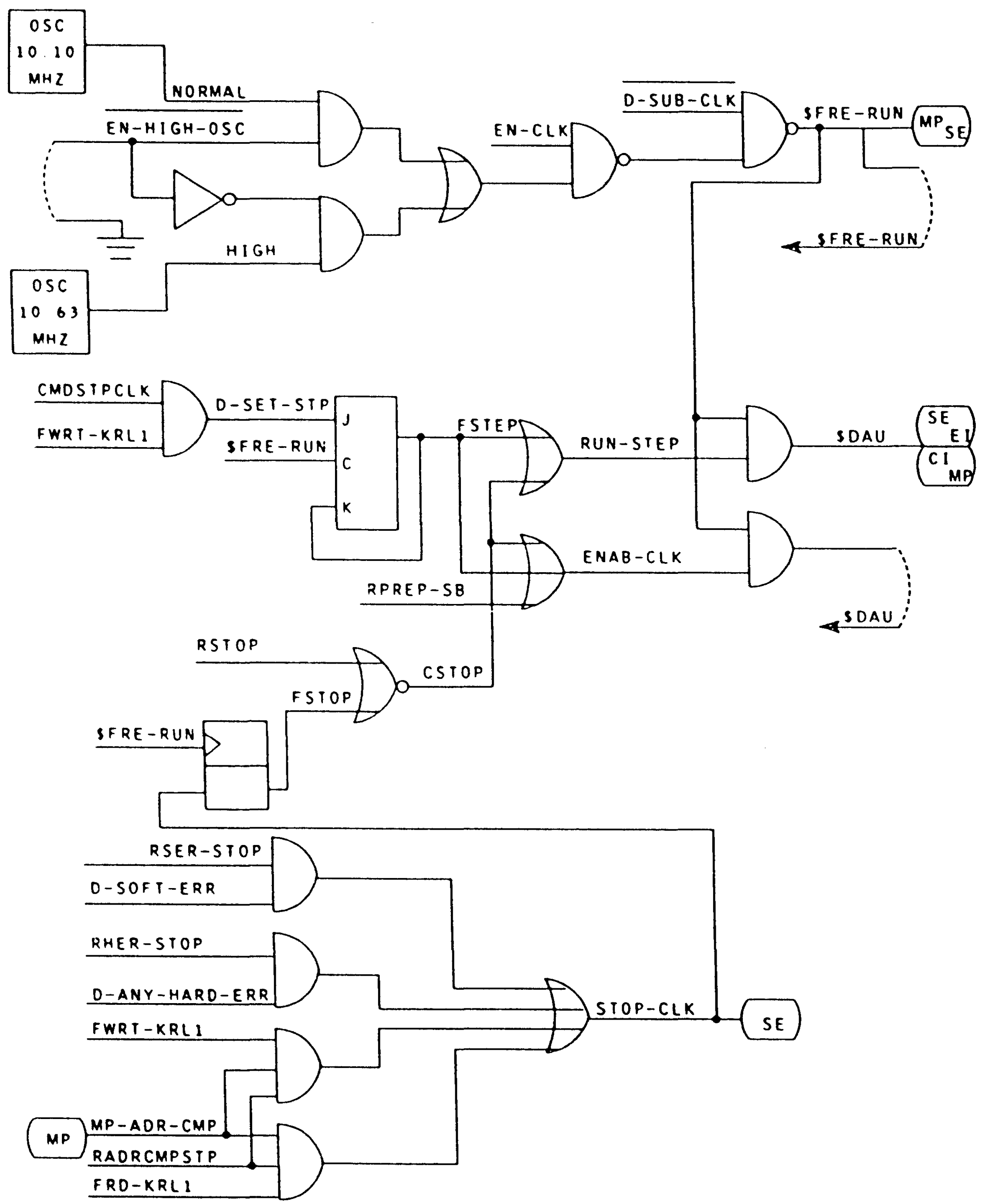


FIGURE 3.4-4. CLOCK CONTROL AND DISTRIBUTION

If the DAU is in a read operation data from the B-register is gated to the CI board. If the DAU is in a write operation data from the B-register is routed to the SE and EI boards. If the DAU is in either the correction mode or the recirculate mode the data from the B-register goes to the EI board.

Data from the Buffer Switch, A-register and B-register may also be read by the microprocessor.

3.4.3 CLOCK CONTROL AND DISTRIBUTION

Refer to Figure 3.4-4.

The clock control and distribution logic consists of two oscillators, one normal and one high speed, and various control logic. The normal oscillator is 10.10 megahertz and produces a clock approximately every 100 nanoseconds. This clock is used for normal operations. The high speed oscillator is 10.63 megahertz and is used for marginal testing. The high speed oscillator is enabled by installing a jumper on the backpanel to ground. This jumper disables the output of the normal oscillator.

The enabled oscillator output is ANDed with EN-CLK and D-SUB-CLK to produce the free-running clock $FRE-RUN. $FRE-RUN is routed to the MP and SE boards and to the DAU clock gates $DAU. $DAU is routed to the MP, SE, EI and CI boards. Notice that the clock for the store board, $FRE-RUN and $DAU, are also routed through the backpanel. This is done to eliminate clock skew.

$DAU is controlled by either RUN-STEP or ENAB-CLK. These signals are generated by FSTEP OR CSTOP. The FSTEP flip-flop is set by a step clock command (CMDSTPCLK) and write control signal FWRT-KRL1. CSTOP is the result of a Mode 2 Register command and some condition. RSTOP is a stop clock command in the Mode 2 Register. The STOP-CLK signal is the result of Mode 2 Register command to stop on a soft error (RSER-STOP) and a soft error (D-SOFT-ERR) or a command to stop on any hard error (RHER-STOP) and any hard error (D-ANY-HARD-ERR) or an address compare stop command (RADRCMPSTP) an address compare by the MP board (MP-ADR-CMP) and either a Read or Write Control signal (FRD-KRL1 or FWRT-KRL1). The STOP-CLK signal is routed to the SE board to reset the Data Control Strobe flip-flop (DCS). This stops data transfers from the device.

3.4.4 COMMAND DECODE

Refer to Figure 3.4-5.

The SB board has been designed with numerous registers and counters which the microprocessor has the ability to load and read back. In order to do this the microprocessor address lines DMPADR-11 through DMPADR-15 are used as inputs to three 1 of 8 select chips. The SB board selected signal (DSEL-BB) is used to enable the chips.

The one of eight select chips decode the address lines into commands, which are used to control the setting of the various registers and control flip-flops. This is shown in more detail in Table 3.4-1. Here address bits 08 through 10 are used to generate the board select signal DSEL-BB.

3.4.5 COMMAND SET

TABLE 3.4-1. SB BOARD REGISTER MAP

0 0 1 1 1 1 1 1 8 9 0 1 2 3 4 5	HEX	WRITE	READ
1 0 0 0 0 0 0 0	80	A-REG 0-7,P	A-REG 0-7,P
1 0 0 0 0 0 0 1	81		B-REG 0-7,P
1 0 0 0 0 0 1 0	82		BUFFER SWITCH 0-7,P
1 0 0 0 0 0 1 1	83	MODE 1 REG 0-7,P	MODE 1 REG 0-7,P
1 0 0 0 0 1 0 0	84	BFRFUL 0-4, DTA 3-7	BFRFUL 0-4, DTA 3-7
1 0 0 0 0 1 0 1	85	SET DEN 0-15	ERR REG 0-5, REV 6-7
1 0 0 0 0 1 1 0	86	SECTOR REQ	
1 0 0 0 0 1 1 1	87	STEP DAU CLOCK	
1 0 0 0 1 0 0 0	88	XFER CNT 4-7	SNAPSHOT 0-3, SEC CNT 4-7
1 0 0 0 1 0 0 1	89	CI CLEAR	
1 0 0 0 1 0 1 0	8A	DAU CLEAR	
1 0 0 0 1 0 1 1	8B	PARTIAL CLEAR	
1 0 0 0 1 1 0 0	8C		
1 0 0 0 1 1 0 1	8D	MODE 2 REG 0-7	MODE 2 REG 0-7
1 0 0 0 1 1 1 0	8E	RESET DEN 8-15	DEN 8-15
1 0 0 0 1 1 1 1	8F	RESET DEN 0-7	DEN 0-7
1 0 0 1 0 0 0 0	90		
1 0 0 1 0 0 0 1	91	WRITE ADR 5-12	WRITE ADR 5-12
1 0 0 1 0 0 1 0	92	WRITE ADR 0-4	WRITE ADR 0-4/SEC16-1
1 0 0 1 0 0 1 1	93	READ ADR 5-12	READ ADR 5-12
1 0 0 1 0 1 0 0	94	READ ADR 0-4	READ ADR 0-4/SEC 16-1
1 0 0 1 0 1 0 1	95	BYTE CNT 4-11	
1 0 0 1 0 1 1 0	96	BYTE CNT 0-3	
1 0 0 1 0 1 1 1	97		

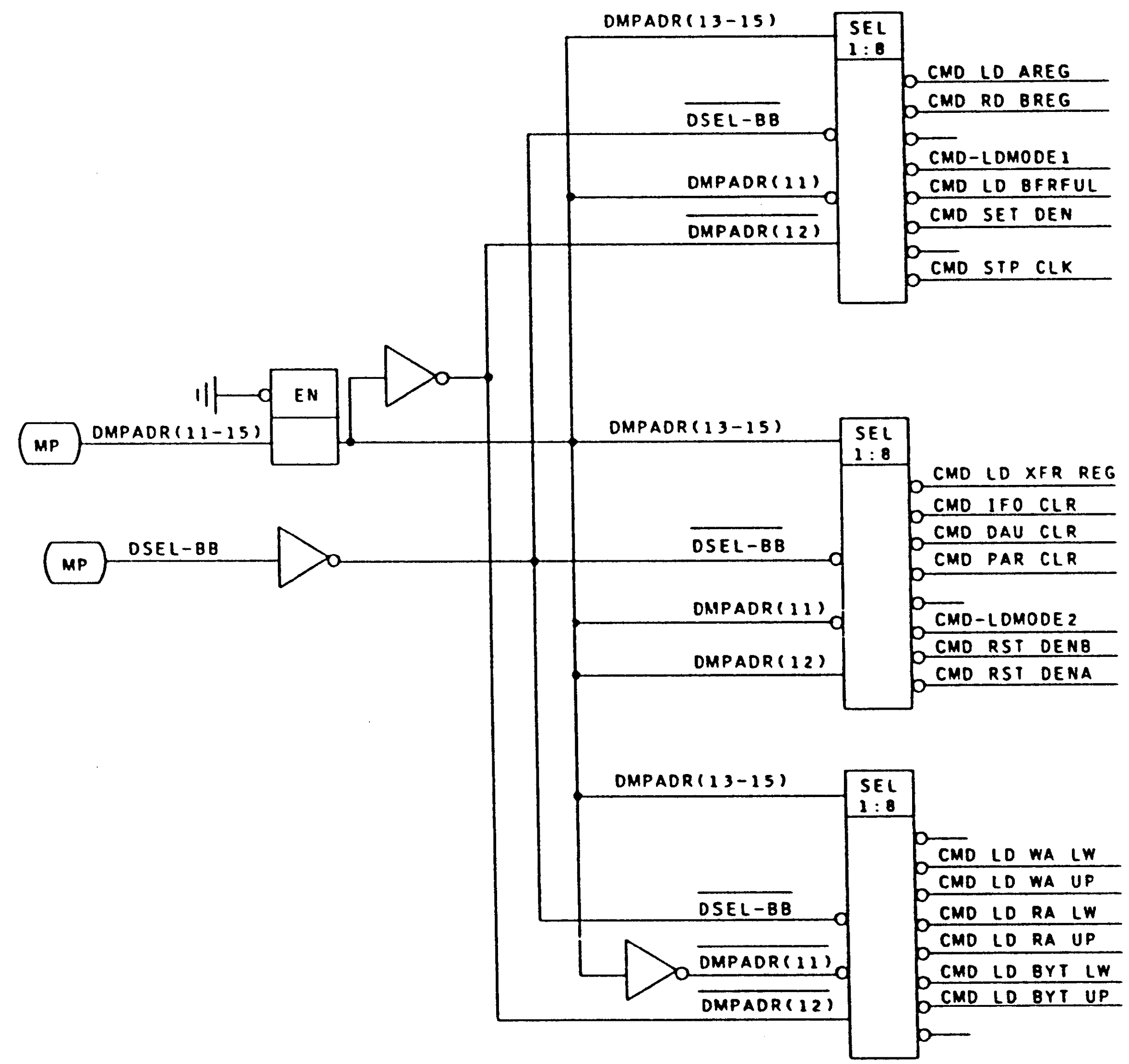


FIGURE 3.4-5. COMMAND DECODE

3.4.6 MODE REGISTERS AND CONTROL

Refer to Figure 3.4-6.

Signals MP-WR and MP-RD enter the SB board from the MP board and are used to clock their respective write (FWR) and read (FRD) flip-flops, provided the microprocessor has selected the SB board (DSEL-BB). FWR and FRD are synchronized by the free-running clock ($FRE-RUN) to produce control signals FWRT-KRL1, FWRT-KRL2 and FRD-KRL1. These signals are used to gate various control signals and data throughout the SB logic.

3.4.6.1 MODE 1 REGISTER (B083)

Refer to Figure 3.4-6.

Microprocessor data (DMPDTA0-DMPDTA7 and DMPDTAP) is loaded into the Mode 1 Register by a load mode 1 command (CMD-LDMODE1), write control 2 (FWRT-KRL2) and the free-running clock ($FRE-RUN). The outputs of the Mode 1 Register determines what mode the DAU is operating in. In other words, the Mode 1 Register determines data flow in the DAU.

0	1	2	3	4	5	6	7
DECODE4	DECODE2	DECODE1	RECIRC. MODE	CORR. MODE	EDAC PLUS	MICRO MODE	WRITE/ READ

DECODE4, DECODE2 and DECODE1 bits are decoded as follows:

DECODE4	DECODE2	DECODE1	
0	0	0	64 Word Sector Mode
0	0	1	Absolute Mode
0	1	0	320 Word Sector Mode (Not Used)
1	0	0	512 Word Sector Mode
1	0	1	320 Word T&D (Not Used)
1	1	0	CI Wrap Around

ABSOLUTE MODE: Addresses the store contiguously. The absolute write mode is obtained by the hardware detecting the presence of the write/read mode bit and the absolute mode decode.

SECTOR WORD MODE: Specifies the sector size.

RECIRCULATE MODE: In the 501 mode, the recirculation mode is set to execute the read-alter-rewrite shuffle. In the 4XX mode, the recirculation mode is set to make the final CRC check after EDAC correction.

CORRECTION MODE: In the 50X mode, the correction mode is set to direct a sector of data through the correction process.

PLUS EDAC: The plus EDAC is set to control the sector size and switching when EDAC bytes are to be sent to, or received from, the system.

MICRO MODE: The microprocessor mode is set to enable data transfers between store and the microprocessor board.

WRITE/READ MODE: The write/read mode is set to enable the write/read switching and control logic (1 = write, 0 = read).

MODE 1 PARITY: This bit checks the integrity of the Mode 1 Register.

3.4.6.2 MODE 2 REGISTER (B08D)

Refer to Figure 3.4-6.

Microprocessor data 0 through 5 (DMPDTA0 through DMPDATA5) is loaded into the Mode 2 Register with a load mode 2 register command, (LD-MODE2), write control 2 (FWRT-KRL2) and the free-running clock ($FRE-RUN). The output of the Mode 2 Register is used to stop the DAU clock ($DAU). RSPARE3 sets the T&D mode.

0	1	2	3	4	5	6	7
HARD ERROR STOP	ADDRESS COMPARE STOP	PREPARE SYNC BYTE	SOFT ERROR STOP	STOP CLOCK	T&D MODE	WRITE SECTOR	READ SECTOR

HARD ERROR STOP: The hard error stop is set to stop the DAU clock when a DAU hardware failure is detected.

ADDRESS COMPARE STOP: The address compare stop is set to stop the DAU when an address compare flag is received from the microprocessor board.

PREPARE SYNC BYTE: The prepare sync byte is set to enable the microprocessor to read out the sync byte for test and diagnostics.

SOFT ERROR STOP: The soft error stop is set to stop the DAU clock when an EDAC or status error from the sequencer is detected.

STOP CLOCK: The stop clock is set to stop the DAU clock.

T&D MODE: The test and diagnostic mode is set to enable the 501 logic without the flag from the sequencer board.

WRITE SECTOR: A test and diagnostic read only indicator. It indicates that an invalid number of bytes of information has been received from the system.

READ SECTOR: A test and diagnostic read only indicator. It indicates that an invalid number of bytes of information has been requested by the system.

3.4.6.3 ERROR REGISTER (B085)

0	1	2	3	4	5	6	7
MICRO DATA PAR ERR	A REG PAR ERR	B REG PAR ERR	READ OUT PAR ERR	ANY ERROR	SHORT BLOCK	BYTE COUNT ONES	SNAP SEC 16

MICRO DATA PAR ERR: Indicates a parity error has been detected on the data received from the MP board (FDBUS-PRTER).

A REG PAR ERR: Indicates a parity error has been detected on the data contained in the A-register (FAREG-PRTERR).

B REG PAR ERR: Indicates a parity error has been detected on the data contained in the B-register (FBREG-PER).

READ OUT PAR ERR: Indicates a parity error has been detected on the data read into the Read-out Buffer. Parity is checked on the data read into the Read-out Buffer when Switch 1 is selected as the output control. Switch 1 controls the multiplexer which selects data from the A-register, B-register, Buffer Switch or the Mode 1 Register as output to the Read-out Buffer (FREGS-PRTYER).

ANY ERR: Indicates any hardware or software error has been detected by the DAU (D-ANY-ERROR).

SHORT BLOCK: Indicates insufficient data has been received (i.e. data does not begin or end on a sector boundary).

BYTE COUNT ONES: Counter has exhausted indicating END of data transfer.

SNAP SEC 16: Sector 16 position of the Snapshot Register.

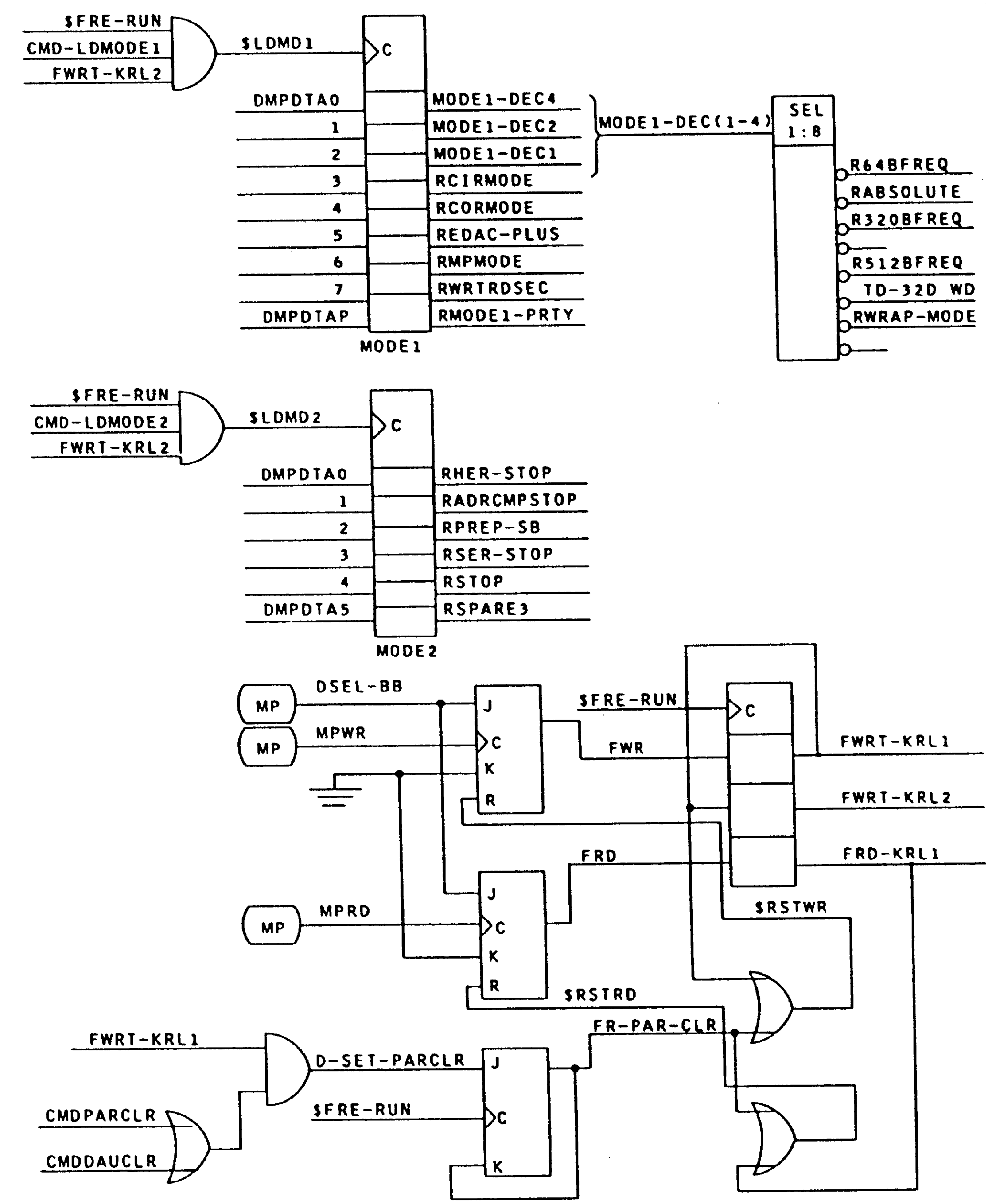


FIGURE 3.4-6. MODE REGISTERS AND CONTROL

3.4.7 A-REGISTER CONTROL

Refer to Figure 3.4-7.

Data is loaded into the A-register from the 1 of 8 select Buffer Switch, by signal $A-REG. The position of the Buffer Switch to be enabled is controlled by the encoder chip. The numbers at the input to the encoder correspond to the switch position to be enabled. Encoder position 0 will enable the MP data to the A-register, while encoder position 1 will enable the B-register data to the A-register, etc. The $A-REG signal will be produced in response to the Encoder inputs if conditions are met. For example, the top input to the $A-REG NOR gate will be enabled with a load A-register command (CMDLDAREG) and a Write Control 2 (FWRT-KRL2) or the DAU is in the correction mode (RCOR-MODE), the A-register is not full (FAREG-FUL) and the Correction Register on the EI board is full (FCREG-FUL). $A-REG sets the A-register Full flip-flop (FAREG-FUL) on the next $DAU.

FAREG-FUL and FRD-SECTOR reset, causes the generation of the write enable signal ($WE) on the next $DAU. $WE enables the writing of the contents of the A-register into the buffer at the address specified by the write address. At the same time FAREG-FUL will be reset.

3.4.8 WRITE BUFFER ADDRESS AND SECTOR CONTROL

Refer to Figure 3.4-8.

The logic on this figure is used to control the address to which data is written into the store buffer. Remember, all data for the device from the system is written into the store buffer as 64 word sectors (288 bytes) with no EDAC bytes attached. When data is read from a device it is written into the store buffer as 64 word sectors with EDAC bytes attached. In the 4XX mode, a sector will consist of 288 bytes of data and seven EDAC bytes, for a total of 295 bytes. In the 500 mode, a sector will consist of 288 bytes of data and 6 EDAC bytes, for a total of 294 bytes. In the 501 mode, the 512 word sector (2310 bytes) is stored as eight 64 word sectors. The six EDAC bytes are attached to the last 64 word sector. The results is seven 288 byte sectors and one 294 byte sector. This was shown on Figure 3.4-2 for the 4XX and 500 modes and Figure 3.4-3 for the 501 mode.

Transfer Request, (FXFRREQ) on the CI board, (FSECREQ) on the SB board, sets FWR-SECTOR flip-flop if the data is from the central system (RWRT/RDSEC). FWRT-SECTOR enables data from the CI board (R-DATA 0-7,P) to be transferred to the A-register (Figure 3.4-7). The data is then transferred to the store and written into the location specified by the Write Address Counter (C-WADR-00-12) by the Write Enable Strobe ($WE). $WE increments the Write Address Counter.

FWT-SECTOR generates PLUSRD-DEV if the DAU is not in the correction, recirculate, or plus-EDAC modes.

PLUSRD-DEV is then ANDed with D501WNLSTSEC to generate W286. The 286th data byte loaded into store generates the WDCD286 decode of the Write Address Counter and CWB-SECADR is generated.

CWB-SECADR is ANDed with the loading of the 287th byte into store ($WE) to set F-RD-SEC-DLY. The loading of the 288th byte into the A-register ($A-REG) sets Increment Write Sector Address (FINCWSECADR). FINCWSECADR loads the next modulo 512 byte address into the Write Address Counter. This is done when FLD-ZEROS loads zeros into the lower write address counter bits (C-WADR04-12). Strobe Increment Write Sector Address (INCWSA) is generated to increment the counter to the beginning of the next sector.

When data is written into store from a device, CMD-WR-DCS generates PLUSRD-DEV. PLUSRD-DEV is then ANDed with a signal that corresponds to the device type. If the device type is either a 4XX or 500, PLUSRD-DEV is ANDed with WD4294-5293. A 4XX device will produce this signal when the 294th byte is loaded into store. A 500 device will produce this signal when the 293rd byte is loaded. If the device is a 501, the first seven 64 word sectors will be written, utilizing the W286 NAND gate. The eighth 64 word sector will utilize the C501EDAC NAND gate. This allows the six EDAC bytes to be stored with the last 64 word sector (D501WLASTSEC).

During a read from a device, signal RD-WTSEC-INC will be used to set FINCWSECADR in order to increment the Write Address Counter to the beginning of the next sector.

The Increment Read Sector Address (FINCRSECADR) and FSNAP-SHOT signals are used in the 501 mode, when a short block is received from the central system. The short block causes a read-alter-rewrite operation. FINCRSECADR is used to load an unused sector address into Write Address Counter in preparation for reading the next sector from the device. FSNAP-SHOT is used to load the Write Address Counter with the sector address to start the alter operation.

The Write Address Counter can be loaded by the microprocessor. The low order bits (C-WADR05-12) are loaded with microprocessor data (DMPDTA0-7) by a Command Load Write Address Lower (CMDLDWALW). The remaining write address counter bits are loaded with microprocessor data (DMPDTA2-7) by Command Load Write Address Upper (CMDLDWAUP).

3.4.9 READ BUFFER ADDRESS AND SECTOR CONTROL

Refer to Figure 3.4-9.

The Read Address Counter can be loaded by the microprocessor. The low order bits (C-RADR05-12) are loaded with microprocessor data (DMPDTA0-7) by Command Load Read Address Lower (CMDLDRALW). The remaining read address counter bits are loaded with microprocessor data (DMPDTA2-7) by Command Load Read Address Upper (CMDLDRAUP).

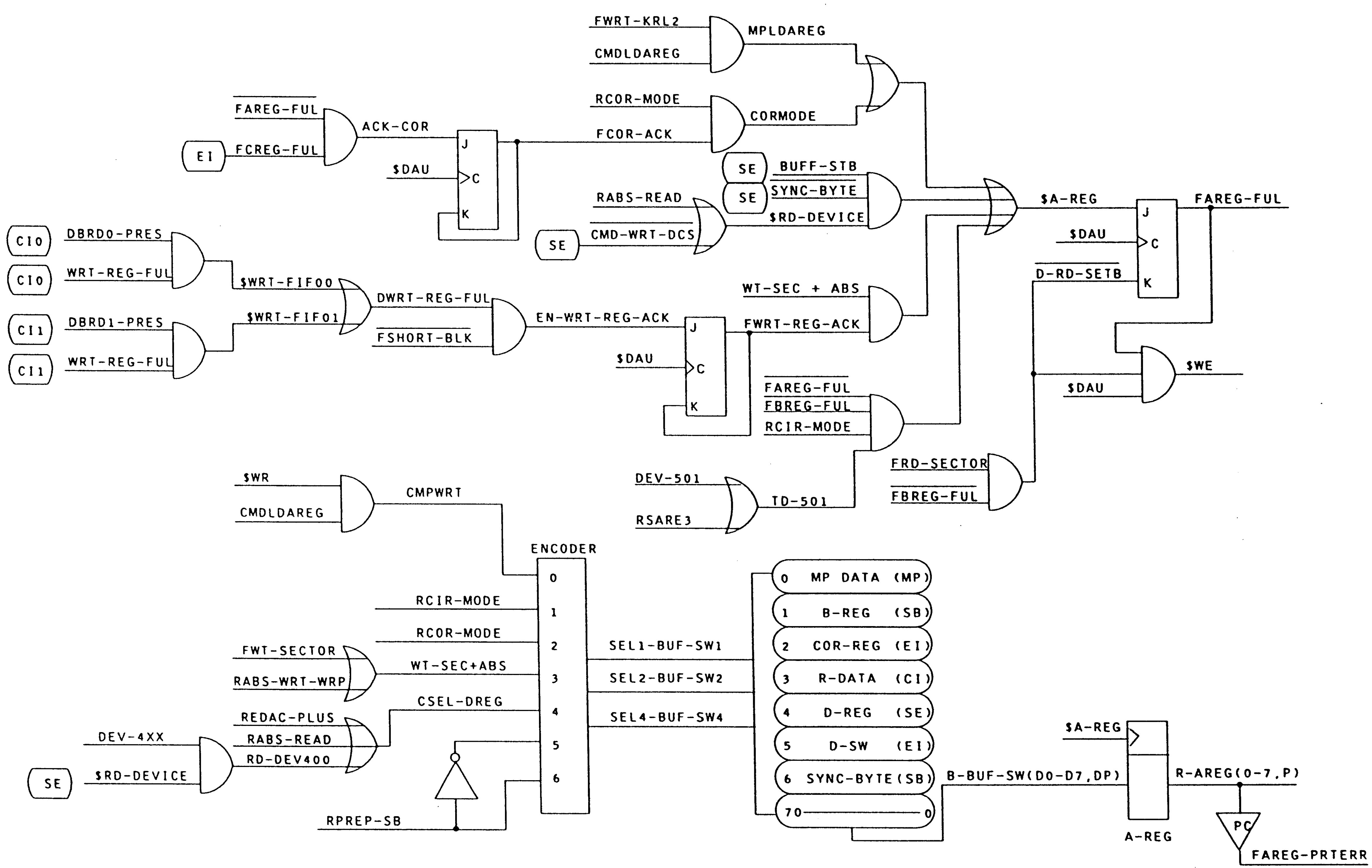


FIGURE 3.4-7. A-REGISTER CONTROL

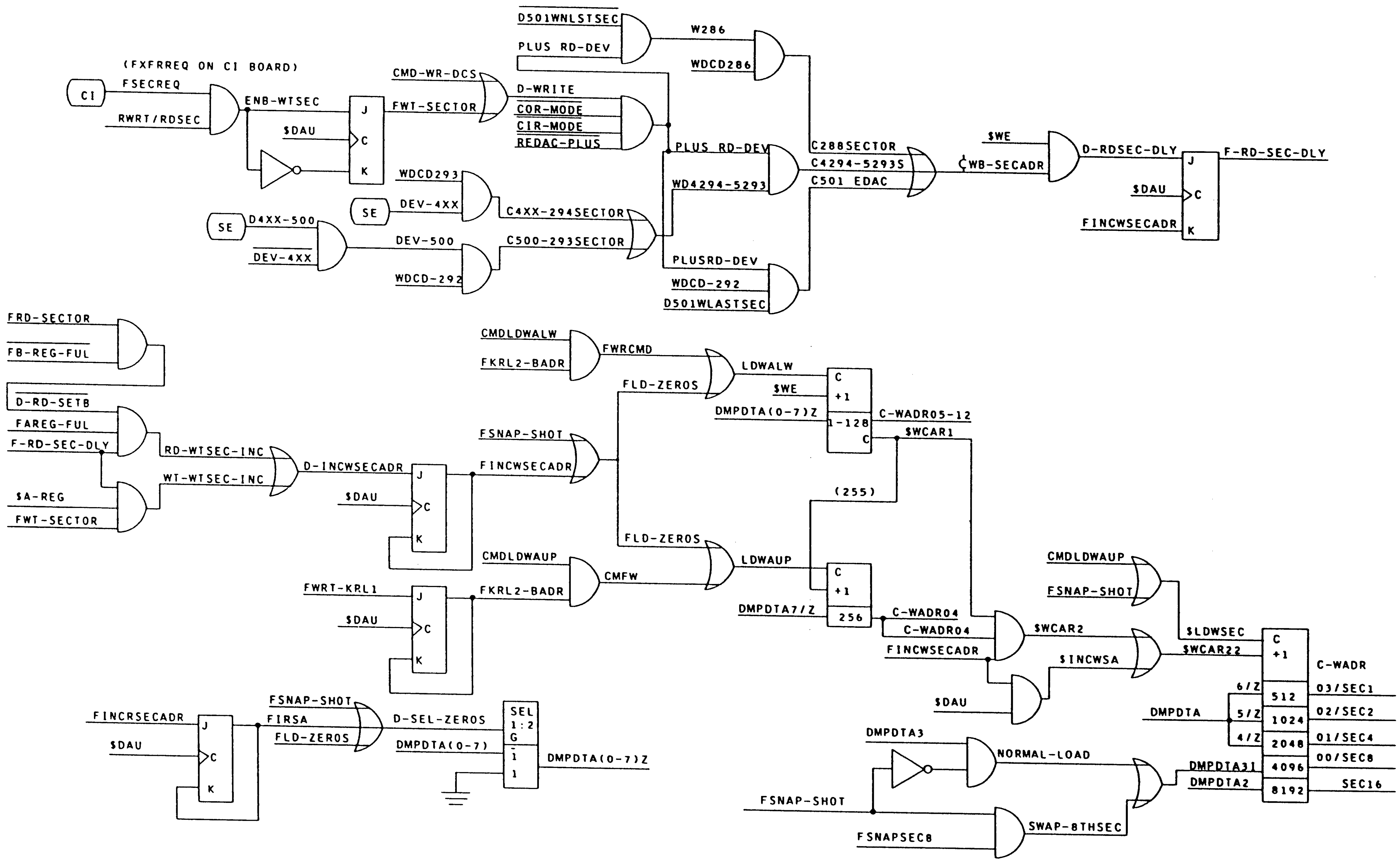


FIGURE 3.4-8. WRITE BUFFER ADDRESS AND SECTOR CONTROL

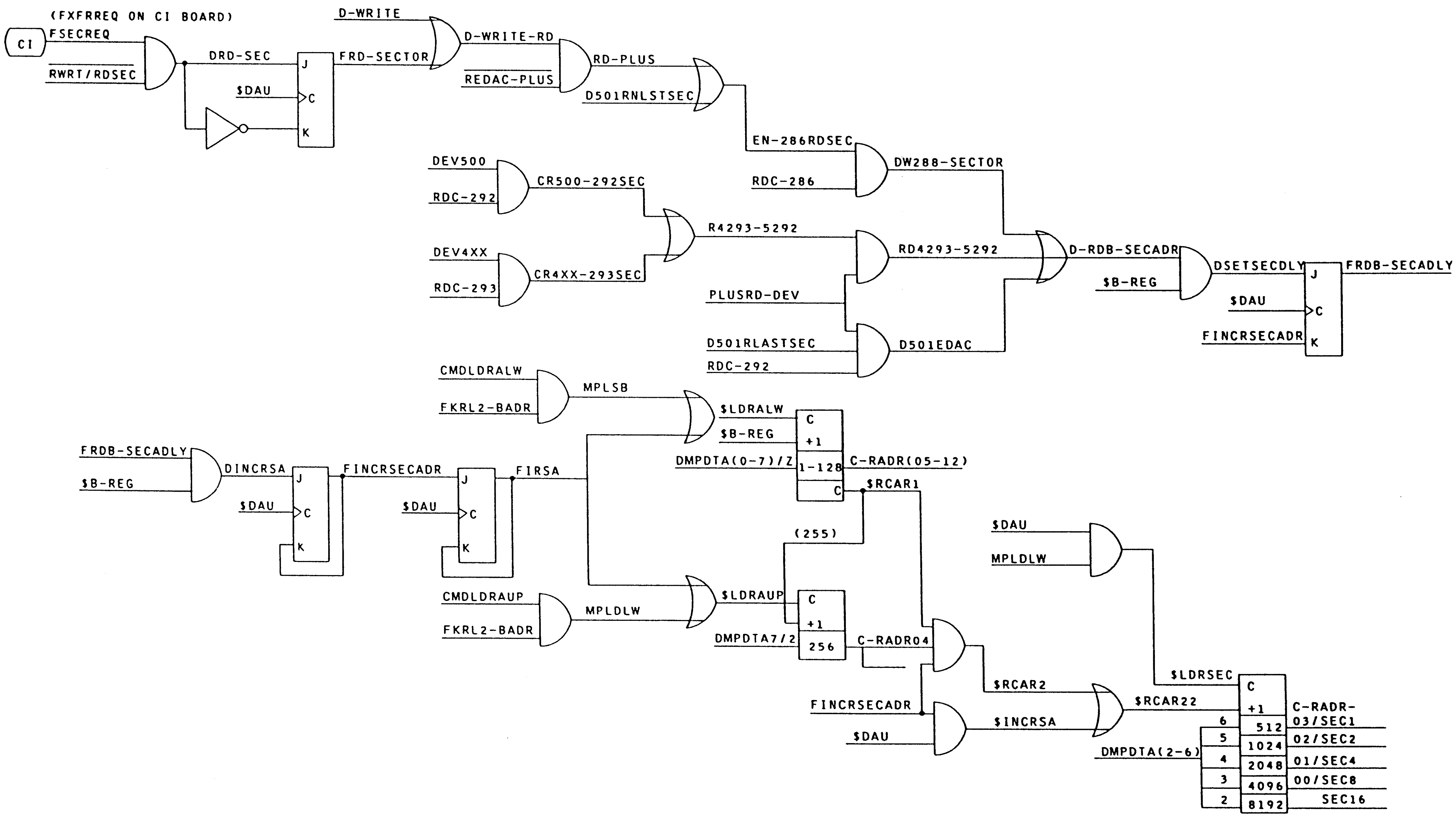


FIGURE 3.4-9. READ BUFFER ADDRESS AND SECTOR CONTROL

Each time data is read from the store and strobed into the B-register ($B-REG) the Read Address Counter is incremented. When data is read from store during a write to device operation, the signal D-WRITE is generated. This produces RW-PLUS, if the DAU is not in the T&D mode (REDAC-PLUS) to transfer EDAC and therefore EN-286RDSEC. When the 286th byte of the sector is read, WRDC-286 will be decoded from the Read Address Counter and DW288-SECTOR and D-RDB-SECADR are generated. When the 287th byte is strobed into the B-register flip-flop, FRDB-SECADLY will set. As the 288th byte is strobed into the B-register, the Increment Read Sector Address flip-flop (FINCRSECADR) sets. The next DAU clock ($DAU) sets FIRSA which loads zeros into the low order bits of the Read Address Counter (C-RADR04-12). At the same time, signal $INCRSA is generated to increment the sector portion of the Read Address Counter.

When data is read from store during a read to system operation, the CI board generates a Transfer Request (FXFRREQ on the CI board, FSECREQ on the SB board). This is ANDed with read sector (RWRT/RDSEC) to set the FRD-SECTOR flip-flop. The remainder of the read buffer address and sector control logic operates the same as the write to device operation.

Remember, during both of the above operations, only data is transferred. The EDAC bytes are not transferred.

During EDAC PLUS, correction, and recirculate operations all inputs to the D-RDB-SECADR NOR gate will be utilized. Their operation is similar to that explained for the write buffer address and sector control logic.

3.4.10 STORE BUFFER AND CONTROLS

Refer to Figure 3.4-10.

The store buffer is shown with three inputs; the A-register data (R-AREG0-7,P), the Write Enable Strobe ($WE), and the 14 Address Select Lines (BADR00-12/SEC1-16). The address select lines come from a 1 of 2 select chip. This chip selects between the Write Address Counter (C-WADR00-12/SEC1-16) and the Read Address Counter (C-RADR00-12/SEC1-16). The Write Address Counter inputs will be selected when the A-register is full (FAREG-FUL) and the DAU is not reading a sector (FRD-SECTOR is low). The Read Address Counter inputs will be selected when the DAU is reading a sector (FRD-SECTOR) and the B-register is not full (FBREG-FUL).

When the Read Address Counter is selected as the store address, the write Enable signal ($WE) will be low. The contents of the RAM address are read out and strobed into the Read Bit Register (RD-BIT0-7,P) by the B-register strobe ($B-REG). The data passes on to the B-register and is available to the other boards. $B-REG will be produced when:

- Writing to a device (FCMD-WRITE), neither the A- or B-registers are full (A + BREG-FUL), and the write is not inhibited by one of the modes (D-WRTDEV-INH).
- The DAU is in the correction mode (RCORMODE), the B-register is not full (FBREG-FUL), and the device is not a 4XX (DEV-4XX).
- The DAU is in the recirculate mode (RCIR-MODE), the device is a 4XX (DEV4XX/501), and the B-register is not full (FBREG-FUL).
- The B-register is not full and either the DAU is in the microprocessor mode (RMPMODE), in a read sector operation (FRD-SECTOR), or in the absolute read wrap mode (RABS-READ-WRP) with a transfer request from the CI board (F-SEC-REQ).

$B-REG sets the B-register full flip-flop on the next $DAU. FBREG-FUL can also be set by DPAD-SETBFUL. However this input is generated when the DAU is in the TD300 mode and is not presently used.

FBREG-FUL is reset when data is transferred from the B-register or when a new mode is loaded into the Mode 1 Register ($LDMD1).

3.4.11 BYTE COUNTER

Refer to Figure 3.4-11.

The microprocessor loads the 2's complement of the number of bytes or sectors to be transferred into the byte counter. CMDLDBYT-LW loads the low-order eight bits of the byte counter with microprocessor data (DMPDTA0-7). CMDLDBYT-UP loads the high-order four bits with DMPDTA 4-7. The byte counter is incremented each time a data byte is sent to, or a 64 word sector is received from, the central system. When the byte counter reaches a count of all ones, B-register Terminate (FB-REG-TRM) is sent to the CI board to stop data transfer.

The byte counter is used to terminate data transfers to/from the system when the DAU is performing any of the following operations:

- Read-alter-rewrite when the system is writing to a 501 device. The block count limit is loaded into the counter. The counter is incremented by each 64 word sector (FINCWSECADR).
- Read Absolute Mode (RABSREAD). Microprocessor loads the number of bytes to be sent to the system.
- 320 Word Sector Correction Pad (not used).

3.4.12 SECTOR TRANSFER CONTROL

Refer to Figure 3.4-11.

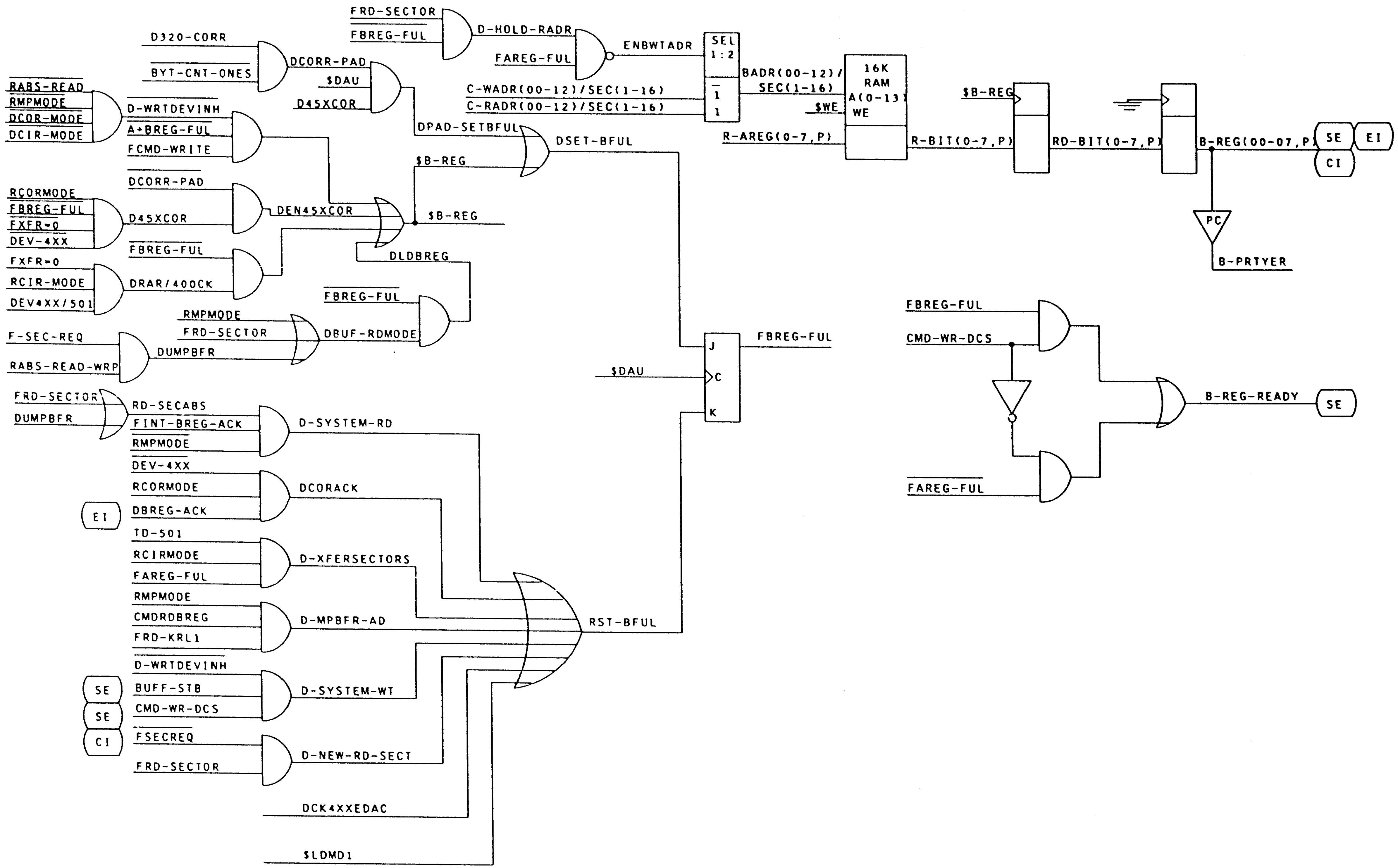


FIGURE 3.4-10. STORE BUFFER - B-REGISTER AND CONTROLS

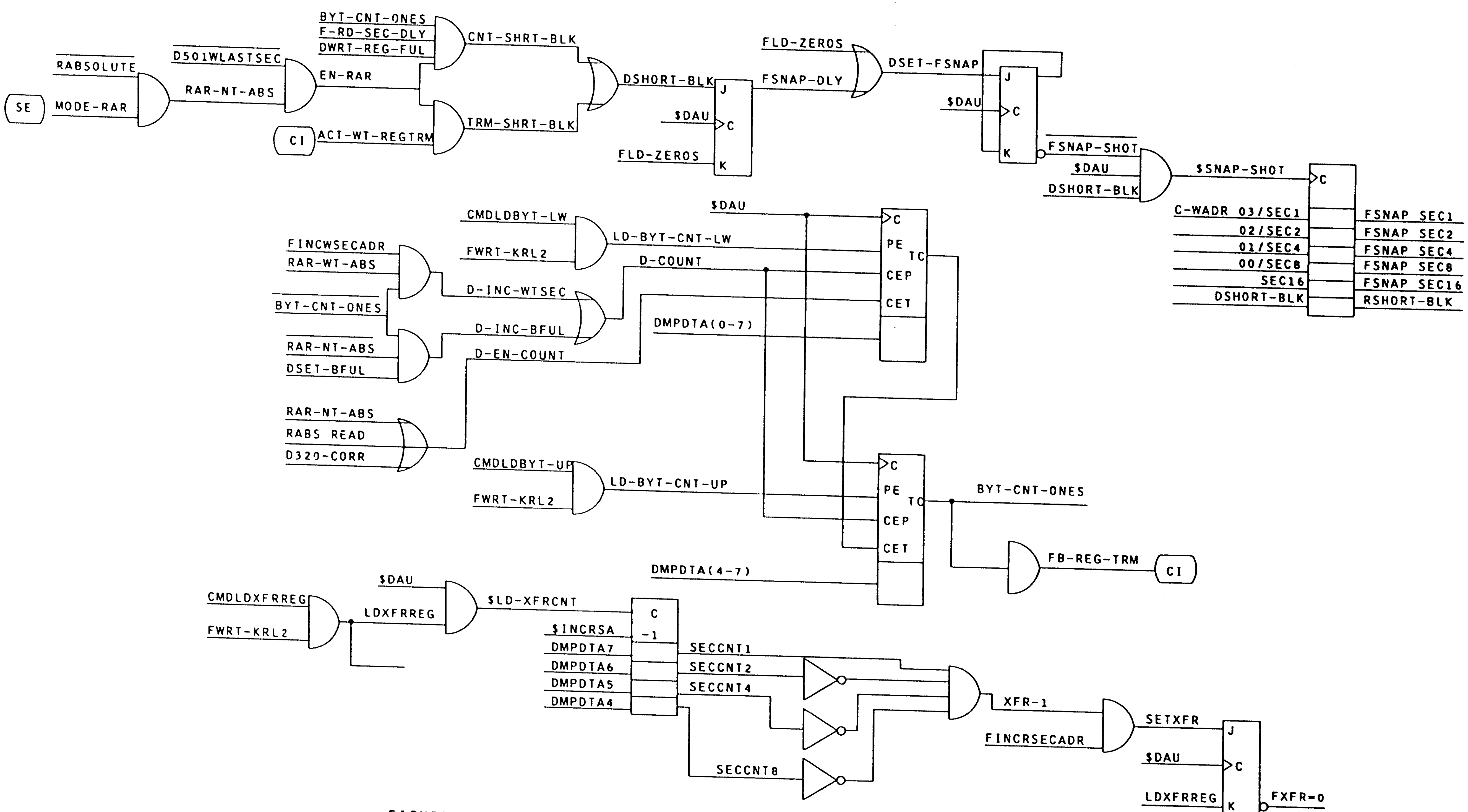


FIGURE 3.4-11. SHORT BLOCK-SNAPSHOT-BYTE COUNTER AND SECTOR TRANSFER CONTROL

The sector transfer control logic is used when the DAU is in the 50X correction mode. It allows one sector of data to be gated through the EI board in order to correct the data. The Sector Counter will be loaded with a one for the 50X mode (64 word sector) or eight for the 501 mode (512 word sector) by the Command Load Transfer Register (CMDLDXFRREG). This command also resets the Transfer Equal Zero flip-flop (FXFR=0). As long as FXFR=0 is reset, byte transfers for the sector to be corrected are enabled. Each time a 64 word sector is transferred, the Increment Read Sector Address signal (FINCRSECADR) is generated. FINCRSECADR produces $INCRSA which decrements the Sector Counter. The FINCRSECADR that occurs after the Sector Counter equals one sets the Transfer Equal Zero flip-flop (FXFR=0) and resets the Sector Counter to zero. FXFR=0 going set inhibits any further byte transfers.

3.4.13 SHORT BLOCK AND SNAPSHOT REGISTER

Refer to Figure 3.4-11.

MODE-RAR is set when firmware determines that system data will be transferred to a 501 Device in 64 word sectors (GCOS) rather than in 512 word sectors (CP6). The Read Alter Rewrite firmware routine is entered initially only if the starting address of the transfer is not on a modulo 512 word starting address. Otherwise, the normal write routine is started and if the system sends a Short Data Block, the RAR is performed at the end of the transfer.

DSHORT-BLK is generated when data transfers are terminated before 512 words have been transferred. Data transfers can be stopped by the DAU when the byte counter equals all ones and CNT-SHRT-BLK is generated or by the CI board when it sends ACT-WT-REGTRM. DSHORT-BLK sets the FSNAP-DLY flip-flop on the next $DAU. At this same time the Snapshot Register is loaded with the current contents of the Buffer Write Address. The Snapshot Register will continue to be loaded by each $DAU until the FSNAP-SHOT flip-flop is set. This occurs when the next 64 word sector boundary is reached and FLD-ZEROES is generated to increment the sector address. FLD-ZEROES also resets the FSNAP-DLY flip-flop.

3.4.14 BUFFER FULL REGISTER

Refer to Figure 3.4-12.

The signal BUF-FUL informs the sequencer that a sector or more of data is in the store and available for transfer. At least one sector of data must be in store before a write to a device or read to the system can be initiated.

When the sequencer receives the BUF-FUL signal, it replys with CMD-WR-DCS and FCMD-WRITE is generated to enable the transfer of data from the store.

The buffer counter may be loaded by the microprocessor with the load buffer full command (CMDLDBUFFUL). The buffer counter is incremented as a sector of data is loaded into store and decremented as a sector is read. The buffer counter is incremented/decremented by one for each 64 word sector written/read from store when a 4XX/500 device is selected. For a 501 device the counter is incremented/decremented by one as each 512 word sector is written/read.

3.4.15 SYNC BYTE REGISTER

In the 4XX mode, the sync byte is included in the EDAC sector generation. So it is stored in the Sync Byte Register so that it can be included in the final CRC check following data correction. Both the Sync Byte Register and FS-SYNC flip-flop outputs go to the EI board. FS-SYNC is used to hold off the transfer of data from store until after the sync byte has been transferred during the recirculate mode. The first DB-REG-ACK from the EI board resets FS-SYNC which allows data to be transferred from the store.

3.4.16 LAST DATA BYTE

Refer to Figure 3.4-13.

The last byte flip-flop is set when the last byte of a sector is clocked into the B-register by $B-REG. For the 4XX or 500 mode this occurs on the transfer of the 288th byte for each 64 word sector. For the 501 devices this occurs when the 288th byte of the eighth 64 word sector is transferred. Last byte is reset when the last byte is unloaded from the B-register by BUFF-STB.

3.4.17 LAST EDAC BYTE

Refer to Figure 3.4-13.

FLAST-EDAC is generated when the DAU is in the recirculate mode. Remember the recirculate mode enables the final CRC check in order to verify the accuracy of data correction utilizing EDAC. FLAST-EDAC is set when the last byte of a sector is received from the store. This is indicated by FINCRSECADR which occurs when the read address is incremented to the next sector address. In the 4XX mode, FINCRSECADR occurs when the 295th byte is read from store. In the 500 mode, it occurs when the 294th byte is read for 64 word sectors. In the 501 mode, it occurs when the 294th byte of the eighth 64 word sector (D501RLASTSEC) is read. FLAST-EDAC is sent to the EI board to enable the setting of F-EDAC-ERROR if the correction attempt was not successful.

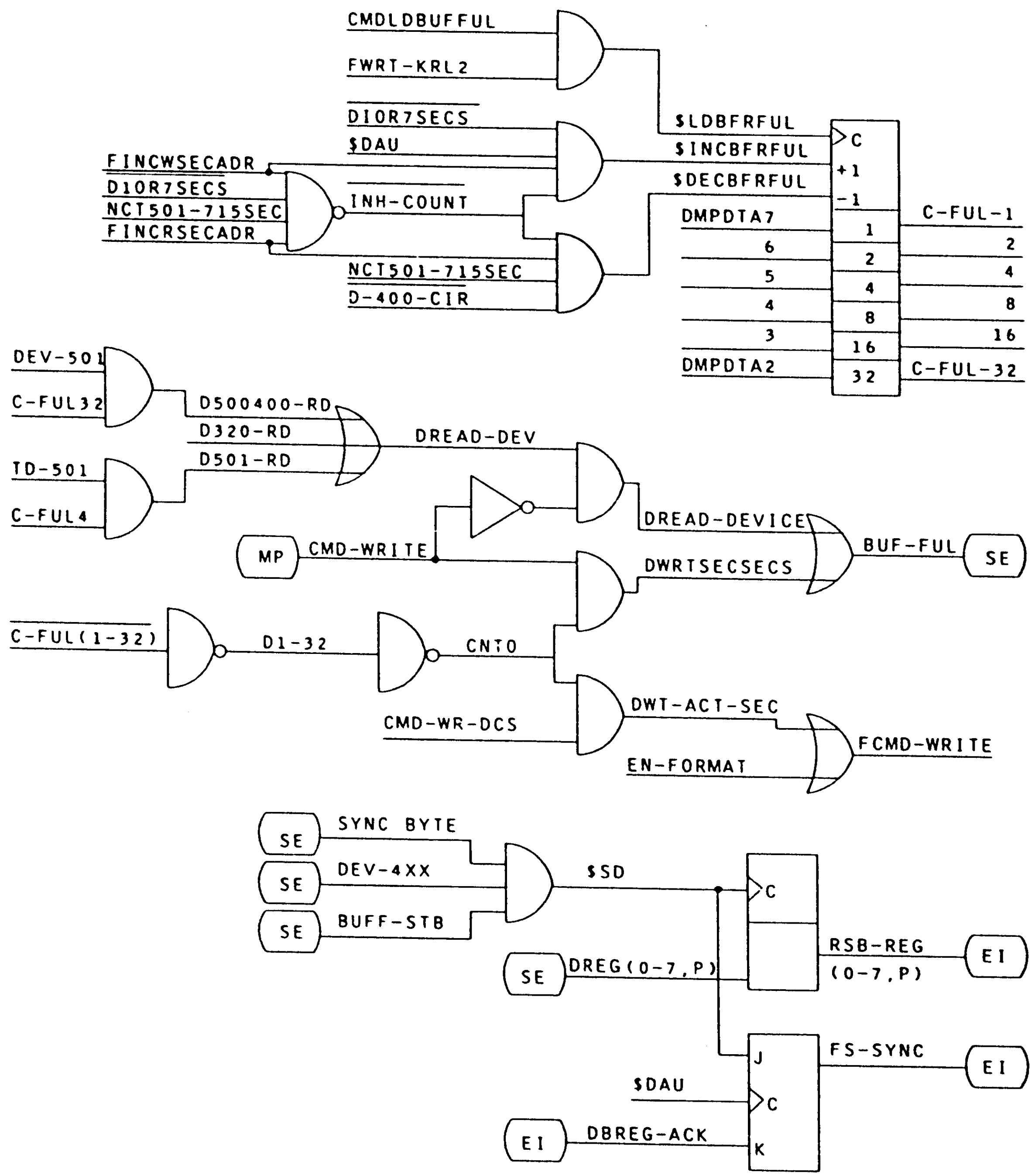


FIGURE 3.4-12. BUFFER FULL AND SYNC BYTE REGISTER

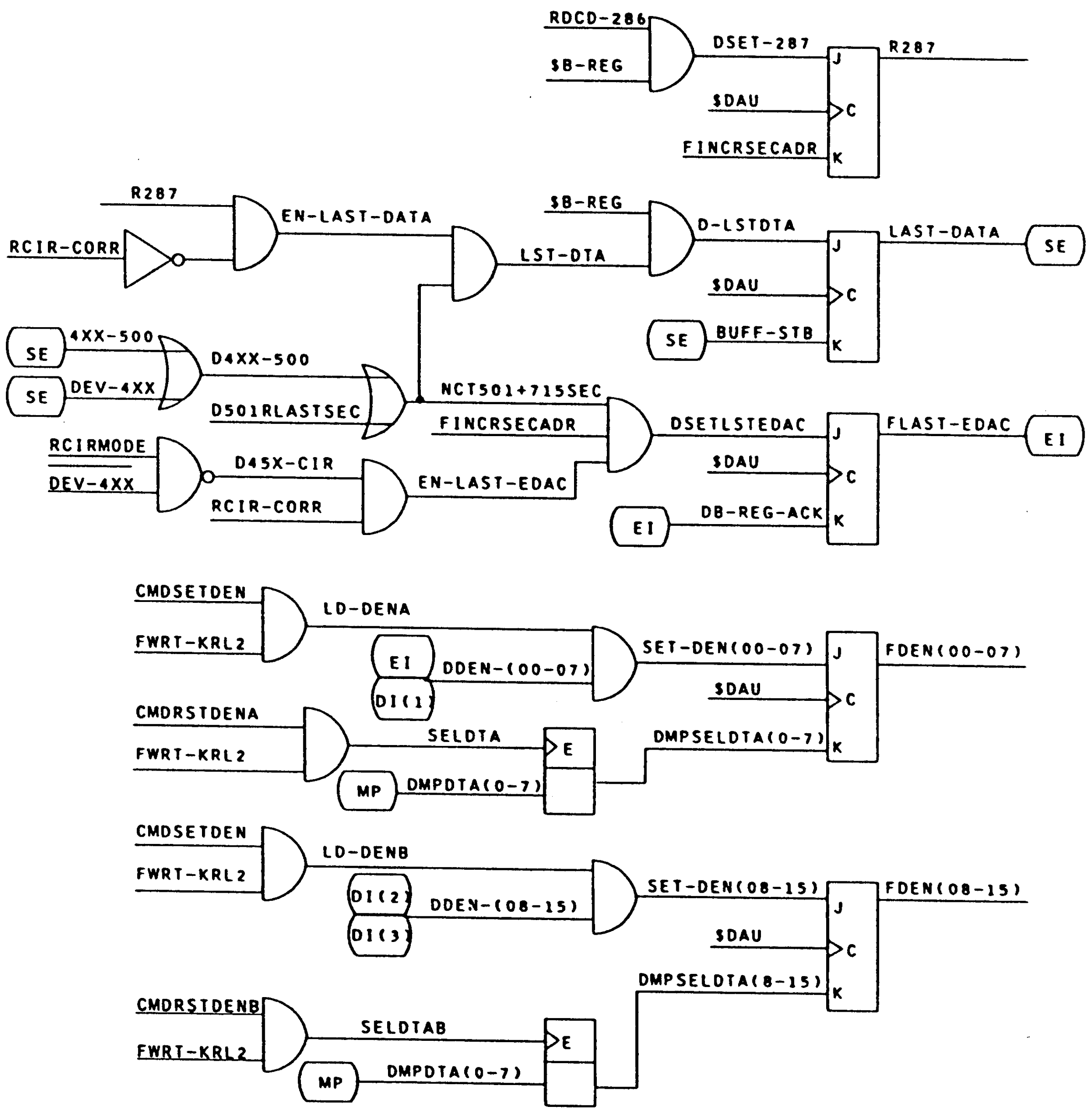


FIGURE 3.4-13. LAST DATA, LAST EDAC BYTE AND DEN REGISTER

3.4.18 DEVICE EVENT NOTIFICATION

Device event notification is stored in two 8-bit registers (FDEN00-07 and FDEN08-15). There is one bit for each of the 16 possible devices which can be connected to a DAU. The FDEN registers can be loaded with the device event notification lines from any device by a Set Device Event Notification Command (CMDSETDEN) from the microprocessor. The FDEN registers can be selectively reset by microprocessor data (DMPDTA0-7) and either CMDRSTDENA or CMDRSTDENB microprocessor command.

3.4.19 DATA PATHS PER MODE

3.4.19.1 MICROPROCESSOR TO STORE

The microprocessor must first load the desired write store address. Next the microprocessor must load 23 hex into Mode Register 1. This places the store board into the absolute write and microprocessor mode. When the microprocessor executes a load A-register command the following takes place: The A-register full flip-flop sets, the A-register is clocked into the store, the write address is incremented, and the A-register full flip-flop resets. Succeeding data bytes can be loaded as desired.

3.4.19.2 STORE TO MICROPROCESSOR

The microprocessor must first load the desired read store address. Mode bits in the Mode 1 Register, such as recirculate and correction, must be set off so that these functions do not interfere with the operation. Next a 22 hex must be set into the Mode 1 Register. This places the store board into absolute read and microprocessor mode (Figure 3.4-6). The microprocessor mode allows the B-register to be loaded from the store, the read address to be incremented, and the B-register full flip-flop to be set. When the microprocessor executes a read B-register command, the B register full flip-flop resets, the next byte is read into the B-register, the read address is incremented, and the B-register full flip-flop sets. Each succeeding byte is read in the same manner.

3.4.19.3 SYSTEM TO MICROPROCESSOR

The store board must be placed into the absolute write mode and the two's complement of the number of bytes to be transferred loaded into the SB byte counter. The PSIA and the CI boards must be set up for a write data transfer and the transfer request on the CI board set on. The transfer request and the terminate on the CI board must be monitored for completion of the transfer. The hardware operation is as follows: The Absolute Write enables the CI Write Register's output into the A-register. The CI sends the DWR-REG-FUL handshake signal to the store board as the CI Write Register is loaded. Then the store board will set the FWRT-REG-ACK flip-flop which will enable the clocking of the Write Register into the A-register and the setting of the FA-REG-FUL flip-flop and the reset of the FWRT-REG-FUL flip-flop. Next the FA-REG-FUL enables the clocking of the A-register into the store and the increment of the store write address by one. At the completion of the data transfer, the microprocessor can read the data as explained in the STORE TO MICROPROCESSOR section. In addition, the firmware can read the data bytes directly from the Write Register as they are available and completely ignore the store board.

3.4.19.4 MICROPROCESSOR TO SYSTEM

The firmware must load the store as described in the section, MICROPROCESSOR TO STORE. Next, the microprocessor must place the PSIA in the read mode and load the proper mode controls on the CI board. Firmware loads the store read address, sets the store board in absolute read mode and loads the byte counter. Next, the transfer request on the CI board is set to enable the data transfer. The B-register will go full with the first byte and the read address increments by one. The FB-REG-FUL signal is sent to the CI board to set the acknowledge flip-flop, and transfer the data byte to the Read Register on the CI board. FB-REG-ACK is sent back to the store board to reset the FB-REG-FUL flip-flop. The following bytes are transmitted in the same manner until the byte counter expires or until the I/O terminates the operation.

3.4.19.5 SYSTEM TO DEVICE (WRITE)

The SB and CI boards are preconditioned as in the SYSTEM TO MICROPROCESSOR via the store board. However this time the store is preconditioned for sector operation. For ease of implementation, all write sector operations are written into the store modulo 288 bytes. The exception is the test and diagnostic mode with EDAC. The 512 word sector, (2304 bytes) is written into store as eight 64 word sectors. The firmware must precondition the store for this operation by loading a 02 hex into the Mode 1 Register for 64 word sectors and a 42 hex for 512 word sectors.

Hardware operation is as follows: The transfer request on the CI board will set the store board FWRT-SECTOR flip-flop. FWRT-SECTOR will enable the CI Write Register as input to the A-register. The A-register will transfer to the store in the same manner as the Absolute Write Operation. When hardware detects that the 287th byte has been transferred to store, the F-RDSEC-DLY flip-flop is set. When the 288th byte is written into the A-register, FINCWSECADR flip-flop is set. FINCWSECADR loads the next modulo 512 byte address immediately after the 288th byte is written into store. If a write/read store conflict exists, the read is delayed one clock. The store board contains store full logic that informs the sequencer that a sector or more of data is available for transfer to the device. If a sector is not available when the sector to be written is ready, the sequencer allows the device to take a latency.

If the store has a sector available, the sequencer raises the signal CMD-WRT which enables the store to load the B-register and the read address to increment by one. The sequencer returns a signal back to the store to reset the B-REG-FUL flip-flop and load the next data byte. The remaining sectors of data are written in the same manner. A signal D-LAST-DTA is sent to the sequencer, which is also counting bytes per sector. If the two counts do not agree the miscompare error flag is set.

3.4.19.6 DEVICE TO SYSTEM (READ)

Both the absolute and the read sector operation are used. The absolute operation is used for reading the record headers. The read sector operation is used for reading the data records. Since the absolute operation is basically the same as the read sector operation, only the read sector operation will be explained. The chief difference is that in the absolute operation the record size is variable.

In the 4XX mode, plus EDAC or absolute modes, the D-register on the sequencer board is directly selected as input to the A-register. In the 50X modes, the D-register D-REG or D-REG NOT switch on the EDAC board is selected as input to the A-register. The sequencer board switches to D-register D-REG or D-REG NOT when the EDAC bytes come through the switch. Inversion of the EDAC bytes is required because they are written onto the disk in the inverted form. Therefore they must be returned to their original form for EDAC error check. They are inserted into the store in case they require correction.

When the sequencer board obtains a data byte in the D-register to be transferred to the store, either directly of indirectly, it will raise the BUFF-STB and CMD-WRITE signals to enable the clocking of data into the A-register and the A-REG-FUL flip-flop. The setting of A-REG-FUL enables the clocking of the A-register into the store. This causes the Write Address to increment by one, and the A-REG-FUL flip-flop to reset. This process is repeated until a sector bound is encountered. In the 4XX mode, 64 word record (288 bytes of data and seven EDAC bytes) are loaded into store. When the sector boundary is encountered the Sector Address is forced to the next modulo 288 byte boundary. In the 500 mode 64 word record, the sector length is 288 bytes plus six, (6), EDAC bytes are loaded into store. In the 501 mode, the 512 word sector is implemented as seven 64 word sectors (288 bytes) with no EDAC. The last or eight sector is implemented as 64 words (288 bytes) and six EDAC bytes. To transfer data back to the system, firmware must issue a Request command to the CI board. The request flip-flop will set, which in turn sets the FRD-SECTOR flip-flop. FRD-SECTOR and FB-REG-FUL enables the clocking of the first data byte into the B-register and the store read address to increment. The transfer of data to the system is the same as described in the MICROPROCESSOR TO SYSTEM section. To increase performance, if the hardware detects a write/read conflict, priority is given to the read.

3.4.19.7 50X EDAC CORRECTION

The 50X EDAC Correction Operation will occur as the result of an EDAC error detected after reading a sector into store. The 501 or 500 mode bits from the sequencer will determine the sector size, 2310 bytes or 294 bytes.

To enter this mode the firmware is required to do the following: Set the read and write store sector address to the sector that caused the error, load the sector number counter with one, and turn on the correction mode bit.

The hardware functions as follows: The correction mode will select the processed bytes from the EDAC board as input to the A-register and enables the first read byte to be placed in the B-register. The read address is incremented and FB-REG-FUL is set. FB-REG-FUL is sent to the EDAC board along with the data byte. The EDAC board sets FB-REG-ACK which in turn resets FB-REG-FUL on the same clock that the EDAC register accepted that byte. When the EDAC board loads the corrected or processed byte into its correction register it sets FC-REG-FUL, which goes to the store board. FC-REG-FUL enables the setting of FC-REG-ACK on the store board. FC-REG-ACK enables the clocking of the correction register into the A-register, the setting of FA-REG-FUL, and the resetting of FC-REG-ACK and FC-REG-FUL. FA-REG-FUL enables the clocking of the A-register into the store, the incrementing of the Store Write Address, and the resetting of FA-REG-FUL. When the 293rd byte is loaded into the B-register, a look ahead flip-flop, FRDB-SECDLY, is set. FRDB-SECDLY, FB-REG-REG-FUL and FC-REG-ACK then sets the increment sector flip-flop, FINCRSECADR, as FB-REG-FUL is reset from retrieval of the 293rd byte. On the next clock the B-register will go full with the 294th byte. The last EDAC byte flip-flop, FLAST-EDAC, sets. FLAST-EDAC enables the 500 EDAC and CRC error check.

3.4.19.8 4XX CORRECTION

In the 4XX mode, the sequencer board informs the microprocessor that an EDAC error has occurred. The microprocessor's firmware will allow all the error free sectors to be returned to the system and stop the store transfer requests at the sector in error. Firmware then turns on the correction mode bit which is sent to the EDAC board. The correction syndrome is then read. Firmware calculates the address of the bits in error. Firmware then loads the store read and write address of the first byte in error. A string of 11 bits are correctable. They can cover up to three bytes. After fetching, correcting and restoring the bytes in error, the firmware turns off the correction mode.

3.4.19.9 FINAL CRC CHECK

The final CRC check is made to verify the data that was corrected during the 4XX correction mode.

Before considering the final CRC check, an explanation of the sync byte is in order. In the 4XX mode this byte, actually the record count, is the first byte received from the device. It is included in the EDAC generation for the sectors. Since it is included in the EDAC generation, it is saved in a special register on the store board in case it is required for a final CRC check. Also the FS-SYNC flip-flop is set and sent to the EDAC board.

When firmware checks the validity of the correction it loads the store read sector address, sets the sector count to 1, and turns on the recirculate mode. The first read byte is loaded into the B-register, the FB-REG-FUL flip-flop is set, and the store read address is incremented. FS-SYNC and recirculate enables the sync byte in the special register to be inputted to the EDAC board. The resetting of FB-REG-FUL by B-REG-ACK is inhibited until the first data byte in the B-register is transferred to the EDAC board. FB-REG-FUL is reset by the second B-REG-ACK, and the next byte is loaded into the B-register. This process continues until the sector count is exhausted.

3.4.19.10 READ ALTER REWRITE

Read-alter-rewrite mode (RAR-MODE) is set when firmware determines that system data will be transferred to a 501 device in 64 word sectors (GCOS) rather than 512 word sectors (CP6). The RAR firmware routine is entered initially only if the starting address of the transfer is not on a modulo 512 word starting address. Otherwise, the normal write routine is started, and if the system sends a short data block the RAR is performed at the end of the transfer. An example of the latter case follows.

Refer to Figure 3.4-14

This operation is entered as a result of the stopping of data transfer on a nonmodulo 512 word sector boundary when accessing data from a device formatted in 512 word sectors. For the write sector case, if the system stops sending data on the 10th 64 word sector, the controller must finish writing the complete proceeding 512 word sector to the device. This would be 64 word sectors 0 through 7. The DAU then sets the store write sector address to the beginning of an unused 512 word sector. The DAU must then switch from the write mode to the read mode. The next eight 64 word sectors from the device are then read into the unused 512 word sector (sector 0 in this case). This is done so that firmware can combine it with the short data block. The altered sector will then be rewritten on the disk.

When the DAU receives a terminate from the system (ACT-WR-REG-TRM) or the byte counter exhausted (BYT-CNT-ONES) and the last sector was not detected (D501WLASTSEC) (the store write sector is not modulo eight), the short block signal is generated. This signal is sent to the sequencer and notifies it to read the next sector from the device. SHORT-BLOCK saves the present store write sector address in the Snapshot Register for firmware to use later.

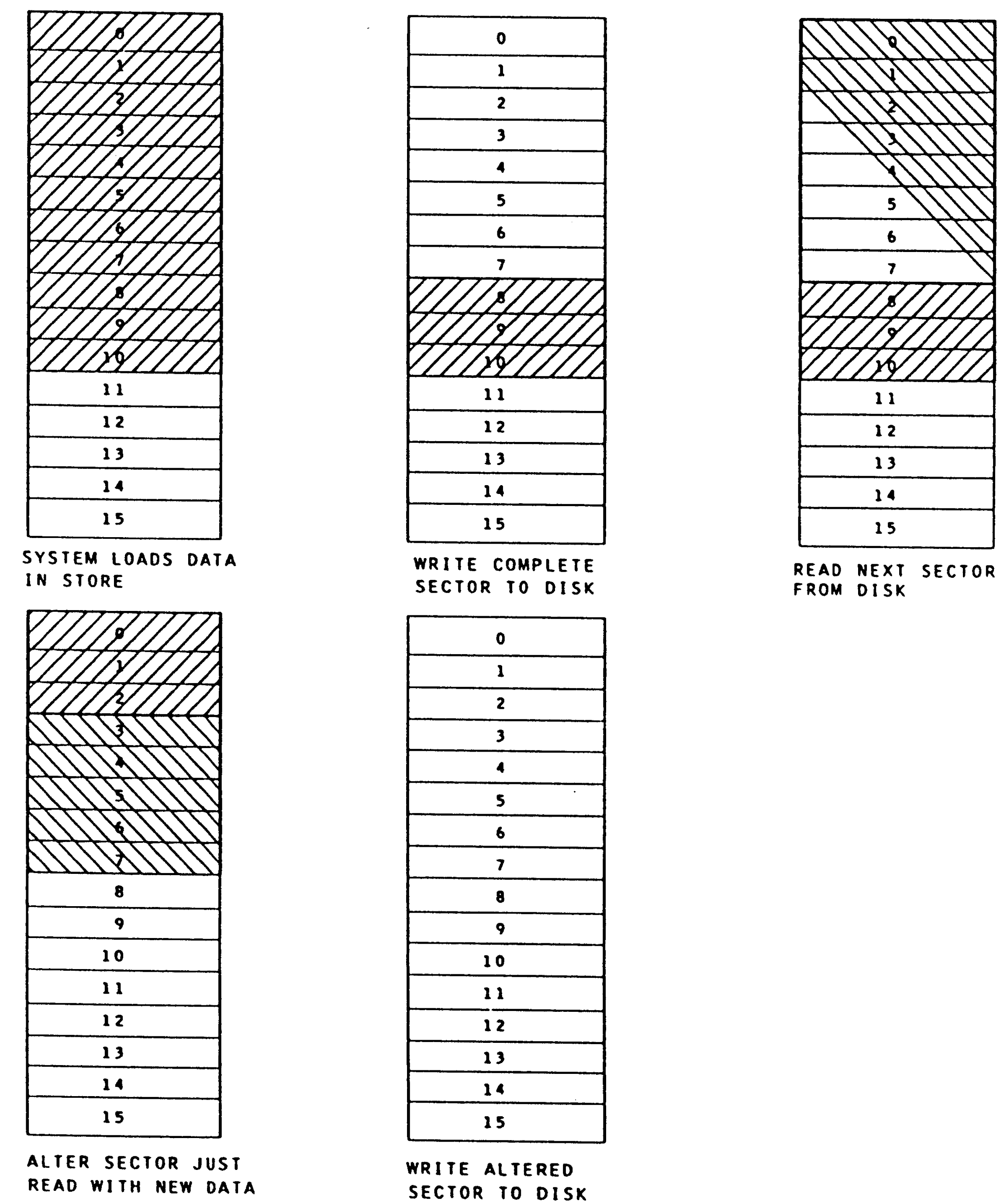


FIGURE 3.4-14. READ ALTER REWRITE

At this same time, FSNAP-SHOT flip-flop is set to lock up the Snapshot Register. The sequencer tests for BFR-FUL going away before testing for short block to assure the previous sector has completed the write before switching to read.

FSNAP-SHOT loads zeros into the lower bits of the Buffer Write Address Counter and switches the state of the sector 8 bit by gating FSNAPSEC8 into this bit position. This sets the Write Address Counter to the beginning of an unused 512 word sector.

After the 512 word sector has been read, firmware must set up to execute the alter. This is done by reading the snapshot address and loading the store read sector address to modulo eight. The store write address is set to the beginning of the 512 word sector just read from the device. In this case it will be set to sector zero. The Sector Counter is loaded with three and the circulate mode is turned on. The hardware will transfer the three sectors (8 through 10) from the store through the B-register to A-register to the store (0 through 2). Firmware can monitor this transfer by reading out the Sector Counter. The 512 word sector is now ready to be rewritten to the device. In order for the DAU to do this, firmware must reset the store read address to the beginning of the 512 word sector, load the BFR-FUL counter to one, reset the circulate mode, and restart the sequencer. The altered sector will be written on the next revolution of the disk.

NOTE: If firmware so desires, it could have transferred the old five 64 word sectors to the new three 64 word sectors and rewritten them to the device starting at 512 word sector one.

3.5 ERROR DETECTION AND CORRECTION (EI)

The EI board contains two distinct portions of logic which were placed on one board because of space limitations. One portion is interface logic that communicates directly with the devices. It was copied essentially intact from the existing MPCDI (device interface) boards. A description of this logic is given under the DISK INTERFACE paragraph, reference Section 3.7.

The remainder of the board contains the EDAC logic for both the 4XX and 50X type devices. The EDAC codes and algorithms are basically the same as used in previous MPCs, but some differences do exist. The logic was entirely reimplemented for microprocessor programmed control. This EDAC logic will be explained here.

3.5.1 EI OVERVIEW

The accurate recording of data on a media is ensured by appending to the data stream a series of bytes that are generated by an algorithm. Such bytes contain no new information.

The algorithm can be expressed as the product of two polynomials, one of which is entirely defined by the data stream, the other of which depends upon the total number of bits to be examined.

Polynomial multiplication is executed in hardware through the use of shift registers. An error is detected when it is determined that the relationship between the recovered appended bits and the recovered data bit stream can no longer be described by the product of the same two polynomials.

There are several major differences between the 4XX EDAC and the 50X EDAC. One major difference is that the 4XX EDAC can correct a maximum of 11 contiguous errors, whereas the 50X EDAC can correct only a maximum of four contiguous errors. The 4XX EDAC corrects only data errors and the 50X corrects both count field and data errors. The number of errors that each EDAC can detect but not correct, and the time required for the detection and correction of errors also differ.

The mechanism with which each EDAC corrects detected errors is also different. The 4XX EDAC corrects errors in firmware while the 50X EDAC corrects errors in hardware. Other differences include the number of EDAC bytes appended to the data stream. The 4XX appends seven bytes of EDAC while the 50X appends six bytes.

3.5.2 EI BLOCK DIAGRAM

The Major Block Diagram for the EI board has been divided into two parts. One part covers the 4XX EDAC logic and is contained on Figure 3.5-3. The other part covers the 50X EDAC logic and is contained on Figure 3.5-7. These diagrams will be covered separately for each type of device.

3.5.3 COMMON LOGIC

The EDAC algorithms and polynomials used for the 4XX and 50X are completely different. Separate hardware is implemented for each, although there is some common hardware. The sequencer board determines which of the two EDAC logics are to be enabled. If any of the 50X mode bits in the sequencer's SEDC Register (SEDC-C0, SEDC-CN, SEDC-64 or SEDC-512) are set, the 50X EDAC logic is enabled. If none of the SEDC Register bits are set, the 4XX EDAC logic is enabled. The logic common to both EDAC logic is explained first.

3.5.3.1 DATA INPUT SWITCH

Refer to Figure 3.5-1.

Data from other boards to be passed through the EDAC logic is selected by a 1 of 4 selector on the EI board. Inputs to the selector are:

- The D-register [DREG-(0-7,P)] from the SE board.
- The one's complement of the D-register generated on the EI board.
- The B-register [BREG-(00-07,P)] from the SB board.
- The Sync Byte Register [RSB-(0-7,P)] from the SB board.

Switch selection is accomplished using various control signals from the SE and SB boards. The output [D-SW-(0-7)] is sent to both the 4XX and 50X EDAC logic and also back to the SB board.

In the 4XX mode, data is always used from the D-register except in the recirculate mode. In the 4XX recirculate mode, the first byte in the data stream is from the Sync Byte Register, and the rest of the data is from the B-register.

In the 50X mode, data from the D-register or the B-register is used. When in the correction mode, the B-register is used, otherwise the D-register is used. The exception is if the D-register has EDAC bytes in it, in which case the one's complement of the D-register is used.

Parity is checked on the output of this switch every time a byte of data is received from the SE or SB boards. A parity error is latched in the F-PAR flip-flop. The parity error is reported in a status byte readable by the microprocessor. It is also sent to the SB board where it is "ORed" into the HARD error logic. The F-PAR flip-flop is reset by a total or partial clear.

3.5 3.2 DATA OUTPUT SWITCH

Refer to Figure 3.5-3.

There are two separate data out switches, one for the 4XX EDAC logic and the other for the 50X EDAC logic (only the 4XX output switch is shown here). These switches are tristated together, and only one is enabled at any given time. Either the microprocessor address lines [DMPADR-(12-15)] or sequencer state lines [SEQ-STATE-(5-7)] can control the output selector. When the microprocessor has selected the board, its address has exclusive control of the output switch. Parity is generated on the output data and this along with the data are routed through common drivers to be sent to the SE and MP boards as R-EDAC-DATA-(0-7,P).

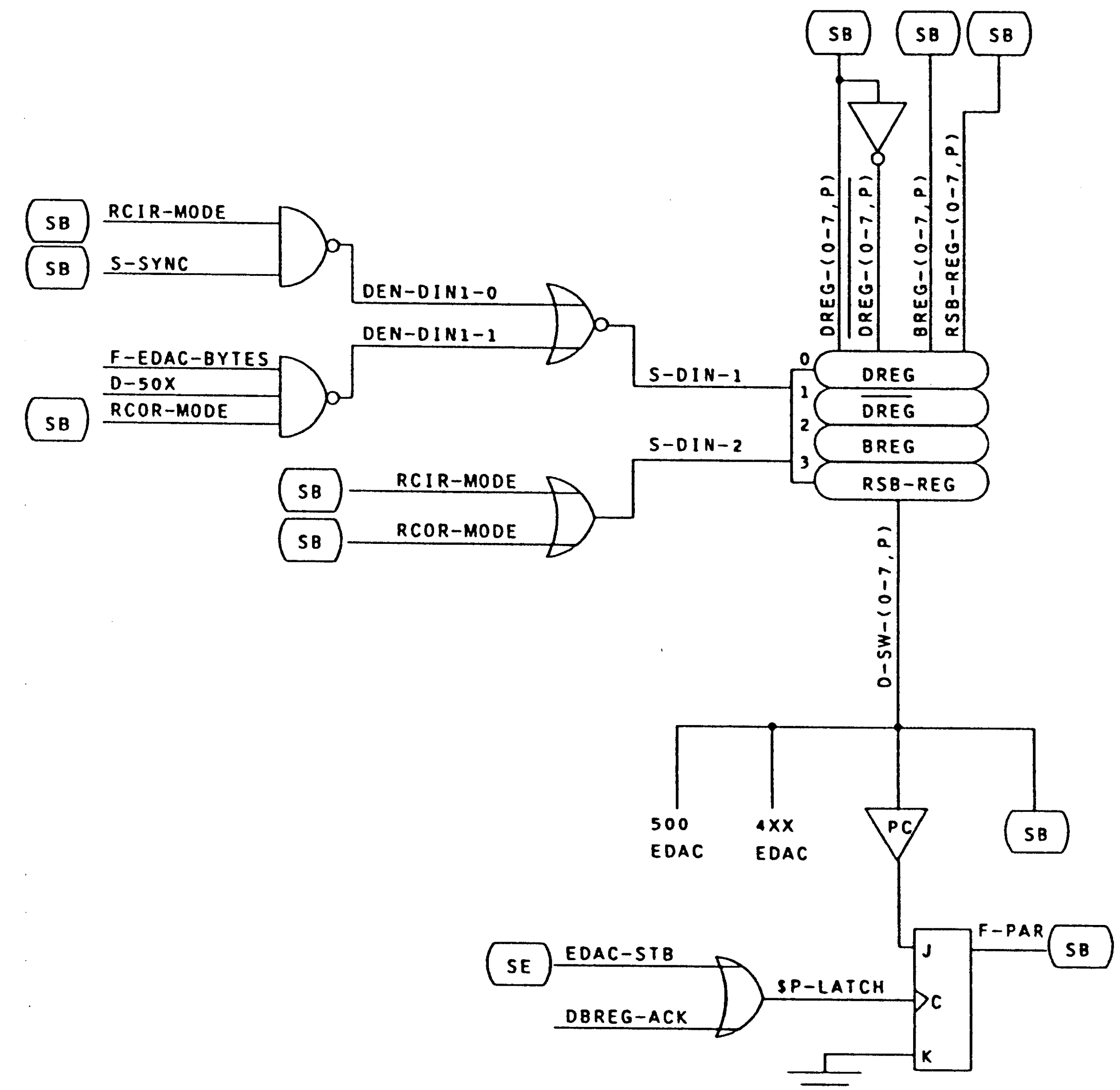


FIGURE 3.5-1. DATA INPUT SWITCH

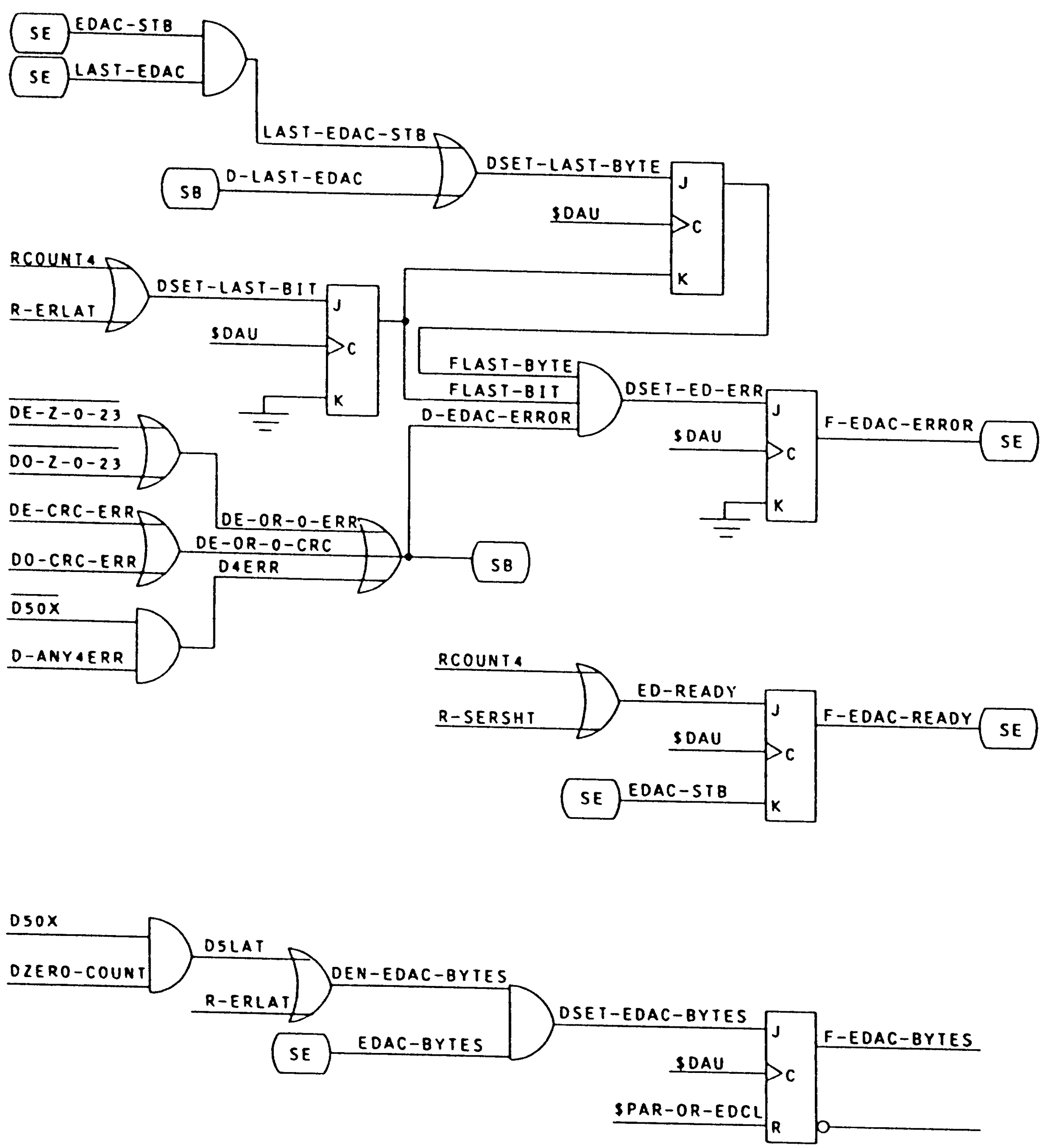


FIGURE 3.5-2. ERROR LATCHING, READY AND EDAC BYTE CONTROL

3.5.3.3 ERROR LATCHING

Refer to Figure 3.5-2.

The logic used to latch an EDAC error at the appropriate time is common to both 4XX and 50X. This is done by using three flip-flops in series. The first, FLAST-BYTE, latches when the last byte has been given to EDAC. The second, FLAST-BIT, latches when the last bit of the current byte has been passed through EDAC. The last flip-flop, F-EDAC-ERROR, is used to latch the error indication after the last bit of the last byte of a data stream is passed through EDAC. That is, when the first two flip-flops are set. This error signal is sent to the SE board and the MP board. It is referred to as EDAC soft error.

3.5.3.4 EDAC READY

Refer to Figure 3.5-2.

The flip-flop that signals to the SE board that EDAC is ready is common to both 4XX and 50X logic. This flip-flop, F-EDAC-READY, is reset whenever the EDAC logic is working with a byte of data, and is set at all other times. It is set by a total or EDAC clear to indicate the ready condition.

3.5.3.5 EDAC BYTES

Refer to Figure 3.5-2.

The flip-flop that is set when EDAC bytes as opposed to data bytes, are being transferred is common to both 4XX and 50X. The sequencer provides the signal EDAC-BYTES, that indicates when EDAC bytes are being transferred. This is used to set the F-EDAC-BYTES flip-flop after EDAC is finished with the current (last) byte of data. The F-EDAC-BYTES flip-flop is reset by a total or EDAC clear.

3.5.4 4XX EDAC

3.5.4.1 OVERVIEW OF THE 4XX EDAC LOGIC

Refer to Figure 3.5-3.

Error detection and correction for 4XX type devices is performed by a AMZ8065 Burst Error Processor (BEP) circuit. The AMZ8065 BEP is a LSI circuit that facilitates the most common error detection and correction schemes accommodating data streams of up to 585K bits at up to 20M bits/second effective data transfer rate.

The AMZ8065 BEP provides a choice of four standard polynomials, including the 56, 48, 35 and 32 bit versions, to satisfy a broad range of applications.

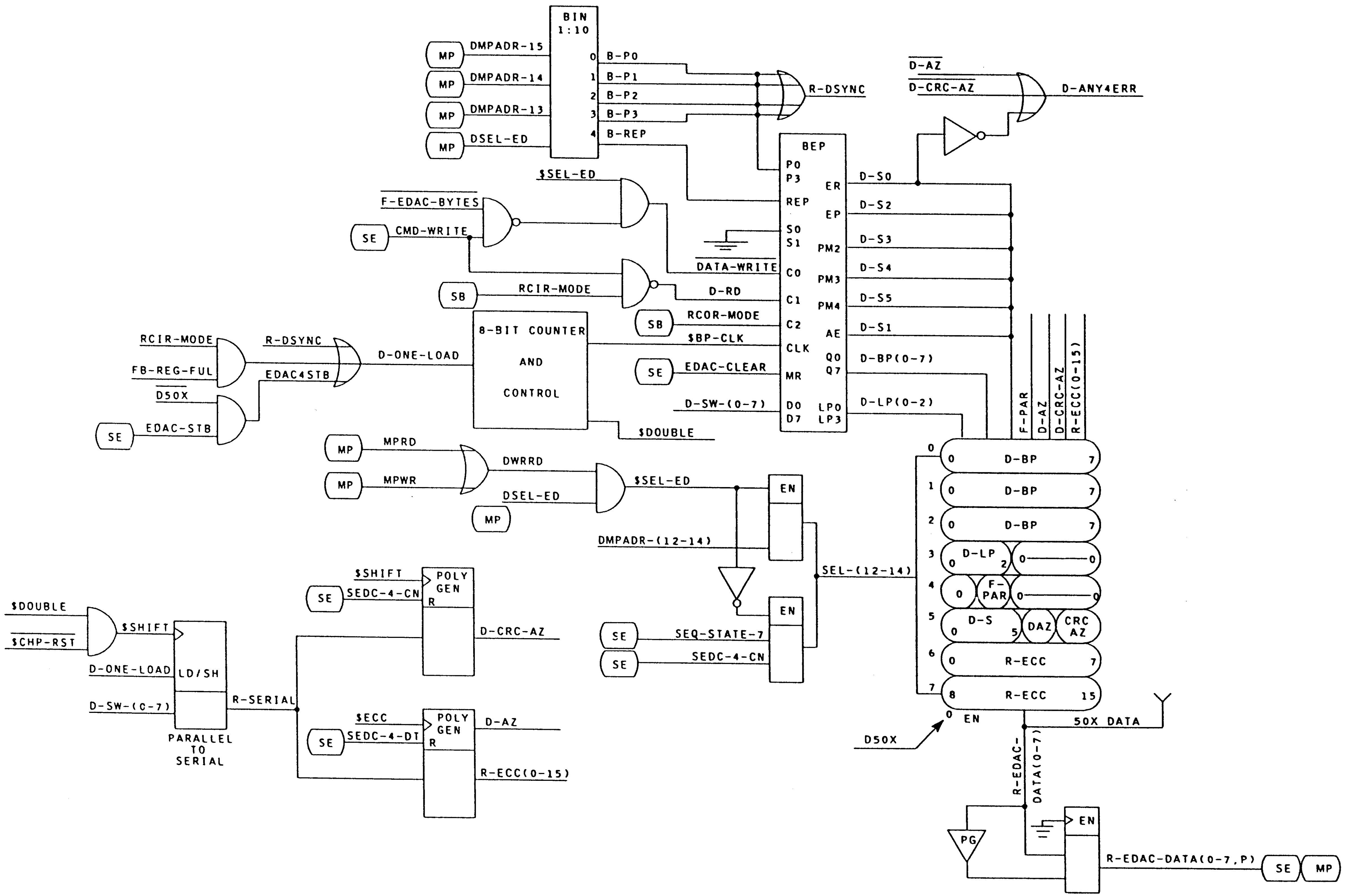


FIGURE 3.5-3. 4XX EDAC MAJOR BLOCK DIAGRAM

The circuit divides the data stream by the selected polynomial using the rules of algebra in polynomial fields. The resulting remainder is the check word which is then appended to the data for writing on the disk as a record. When the record is read back, the BEP computes the syndrome for data validation. If an error is detected, the location and pattern of this burst in the data stream is determined for correction.

3.5.4.2 WRITE TO DEVICE

The microprocessor sets the BEP controls (C_0-C_2) to compute check bytes. Write Data (D-SW-0-7) is clocked (BP-CLK) into the BEP one byte at a time. The EDAC-4STB strobe is generated for each byte. This strobe causes the 8-bit Shift Register to produce a clock to load each byte. The sequencer sends the EDAC-BYTES signal after the last data byte enters the BEP. This causes the control to switch to write check bytes.

The sequencer continues to use signal EDAC-4STB to output the seven check bytes at Q_0 through Q_7 one byte at a time. The check bytes are read out of the Output Selector Switch by Sequencer State Counter bit seven (SEQ-STATE-7).

3.5.4.3 READ FROM DEVICE

The microprocessor places the BEP into the read mode. This is done by making the signal CMD-WRITE low. BP-CLK is generated in the same way as in the write mode. After the last EDAC byte in entered, BEP output signal ER (D-S_0) indicated whether or not an error was detected. If ER is high an error exists, and the syndrome held in the BEP Registers contain the information required to locate the error.

3.5.4.4 CORRECTION MODE

For 4XX type devices, data correction is accomplished by firmware. The BEP is used in this mode to locate the error pattern that is embedded in the syndrome that was produced by the read operation. The error pattern is found by repeated shifting of an Internal Feedback Register until output EP goes high. After locating the error pattern, three other internal registers are shifted until each register's bit configuration matches the error pattern. Firmware maintains a record of all this shifting in order to determine where in the data stream the error exists and whether the error is correctable.

To correct the data the microprocessor switches the controls to the correction mode. In this mode the microprocessor drives inputs P_0 through P_3 to provide the required shifting of the four BEP feedback registers. Input P_0 shifts the first feedback register. Signal R-DSYNC becomes true to produce the clock (BP-CLK). After each shift EP (D-S_2) is tested until the error pattern is found or until the maximum allowable number of shifts is exceeded.

If the latter occurs the error is uncorrectable and the process is aborted.

After finding the error pattern, the microprocessor will drive inputs P_1 through P_3 consecutively to shift the corresponding feedback register until each register matches the error pattern. For each match the corresponding match output (PM_2 through PM_4) becomes active. Should any register fail to match the error pattern after the maximum allowable shifts are performed the error is uncorrectable. If outputs PM_2 through PM_4 all go high within the allowed number of shifts, the error is correctable. The microprocessor then reads out the 11-bit error pattern available on outputs Q_0 through Q_7 and LP_1 through LP_3.

Firmware calculates the location of the error and then aligns the eleven bits of data in error with the 11-bit error pattern. For every "1" in the error pattern the corresponding data bit is complemented to correct the data.

3.5.4.5 RECIRCULATE MODE

After the correction process is completed the DAU is placed in the recirculate mode (RCIR-MODE) and the corrected data, now in the store, is passed back to the EI board to validate the correction.

To accomplish the validation, the microprocessor places the BEP controls back into the read mode. Each data byte is then clocked into the BEP in response to FB-REG-FUL. After the last byte is entered, the microprocessor reads output selector byte 5 and tests for an ER or a CRC error.

3.5.4.6 CRC AND ECC ERROR DETECTION

The CRC and ECC circuits function independently of the BEP. These circuits are fed serial data (R-SERIAL) from the parallel to serial converter circuit. The CRC performs error checking during the processing of the 4XX data fields. The ECC generates and checks the two count field bytes (ECC0-15). Signal SEDC-4-CN disables the CRC circuit during count field processing and signal SEDC-4-DT disables the ECC circuit while processing the data field. These signals are derived from bits 2 and 3 of the EDAC Control Register on the SE board. SEDC-4-CN is also used in conjunction with SEQ-STATE-7 to read out the two count field check bytes. An all zeros signal is produced if no errors are detected in the count field (D-AZ) or in the data field (D-CRC-AZ). Signal ANY-4-ERR is generated if an error is detected by either the CRC, ECC or BEP.

3.5.5 BEP INTERFACE SIGNAL DESCRIPTION

See Figure 3.5-4 for pin location for the following signals.

V_{cc} +5V power supply.
V_{ss} Ground.

3.5.5.1 MASTER RESET ($\overline{MR}$) (INPUT)

Low on this input initializes the BEP. This input must remain low for a specific time to accomplish initialization before returning to the quiescent high state. In general, the BEP requires initialization prior to performing Compute Check Bits, Read Normal, Read High Speed and the Load functions.

3.5.5.2 CLOCK (CP) (INPUT)

BEP operations are controlled by this input. Outputs become valid some propagation delay after the low to high transition on the CP input. The quiescent state of the CP input is high. Any changes on the data and control inputs must take place only when the CP input is high.

3.5.5.3 POLYNOMIAL SELECT (S_0-S_1) (INPUTS)

Logic levels on these two inputs select one of the four standard polynomials provided in the AMZ8065. The following chart specifies the polynomial select codes (the DAU uses only the 56-bit code).

S1	S0	POLYNOMIAL	NUMBER OF CHECK BITS
L	L	$(X^{22} + 1)$ & $(X^{11} + X^7 + X^6 + X + 1)$ & $(X^{12} + X^{11} + X^{10} + \ldots + X + 1)$ & $(X^{11} + X^9 + \ldots + X + 1)$	56
L	H	$(X^{21} + 1)$ & $(X^{11} + X^2 + 1)$	32
H	L	$(X^{23} + 1)$ & $(X^{12} + X^{11} + X^8 + X^7 + X^3 + X + 1)$	35
H	H	$(X^{13} + 1)$ & $(X^{35} + X^{23} + X^8 + X^2 + 1)$	48

3.5.5.4 DATA IN (D_0-D_7) (INPUTS)

These eight inputs are used for entering information into the BEP. D_0 is the least significant bit and D_7 is the most significant bit position.

High on any input corresponds to a 1 and a low corresponds to a 0. Data entry occurs on the low to high transition of the CP input. Any change on the D_0-D_7 inputs must take place only when the CP input is high.

3.5.5.5 FUNCTION SELECT (C_0-C_2) (INPUTS)

These three inputs specify the desired function according to the following table. Detailed description of each function is found in later sections. Any change on the C_0-C_2 inputs must take place only when the CP input is high.

C_2	C_1	C_0	FUNCTION
L	L	L	Compute check bits
L	L	H	Write check bits
L	H	L	Read normal (Not Used by the DAU)
L	H	H	Read high speed (DAU Uses)
H	L	L	Load
H	L	H	Reserved
H	H	L	Correct normal (Full period clock around)
H	H	H	Correct high speed (DAU Uses) (Chinese remainder theorem method)

3.5.5.6 DATA OUT (Q_0-Q_7) (OUTPUTS, 3-STATE)

The check bits are made available on these eight outputs one byte at a time. Q_0 is the least significant bit position and Q_7 is the most significant. The Q_0-Q_7 outputs are active only during the following conditions:

- o The C_0-C_2 inputs specify write check bits function.
- o The REP input is high.

During all other conditions Q_0-Q_7 outputs are in a high impedance state.

3.5.5.7 LOCATED ERROR PATTERN (LP_0-LP_3) (OUTPUTS, 3-STATE)

The LP_0-LP_3 outputs together with the Q_0-Q_7 outputs provide the 12-bit error pattern in which Q_7 is the most significant bit and LP_0 is the least significant bit position. The REP input must be high to read the error pattern.

If the REP input is low, the LP_0-LP_3 outputs are in the high impedance state. The DAU does not use LPO, so error pattern is only 11 bits.

3.5.5.8 READ ERROR PATTERN (REP) (INPUT)

A high on this input activates the LP_0-LP_3 and Q_0-Q_7 outputs. This error pattern information is valid only after a high is indicated on the EP output during correction operations.

3.5.5.9 ERROR (ER) (OUTPUT)

High on this output indicates that the BEP has detected an error. This output must be considered valid only after the last check byte during read normal or read high speed functions has been entered. The resulting syndrome is then contained in the register array. A nonzero syndrome indicates error, while a zero syndrome indicates no error. The ER output always reflects the state of this register array. The ER output is low after initialization.

3.5.5.10 ERROR PATTERN (EP) (OUTPUT)

High on this output indicates that the error pattern has been found during the correction process. When the last check byte was entered during a read function the resulting syndrome is contained in the register array. The error pattern information is buried in this syndrome. To extract the error pattern, the BEP is clocked while the appropriate code is applied to the C_0-C_2 inputs until EP goes high. The number of clocks required to find the error pattern is used to calculate where in the data stream the error has occurred.

The EP output is valid only during the correction operations and must be ignored at all other times. The EP output will be low after initialization.

3.5.5.11 PATTERN MATCH (PM_2-PM_4) (OUTPUTS)

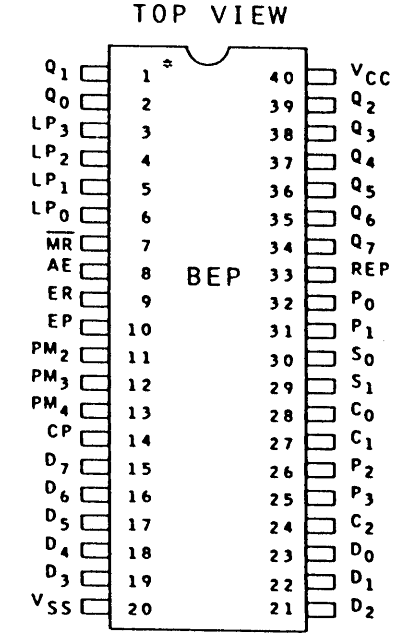
The DAU uses the Chinese remainder theorem for error correction, which causes the data to be loaded into several feedback shift registers simultaneously. The number of registers is equal to the number of factors of the polynomial. After a high speed operation, there are as many syndromes as there are factors. For correction, the register corresponding to the first factor must be shifted until the EP output indicates high. Then each register corresponding to the remaining factors must be shifted until a match occurs in each register with the error pattern contained in the first register. High on PM_2, PM_3 or PM_4 outputs indicates that corresponding registers match. The PM_2 corresponds to the second factor, PM_3 corresponds to the third and PM_4 corresponds to the fourth factor. If a polynomial has only two factors, the PM_3 and PM_4 outputs have no meaning. Indications on the PM_2-PM_4 outputs must be considered valid only during the correct high speed function and should be ignored at all other times.

3.5.5.12 POLYNOMIAL SHIFT CONTROL (P_0-P_3) (INPUTS)

Correction procedure using the Chinese remainder theorem method requires that each syndrome obtained from the high speed read function be shifted individually. The P_0-P_3 inputs provide this capability: P_0 corresponds to the first factor, P_1 corresponds to the second factor and so on. High on an input, allows the corresponding register to shift and a low causes it to hold. These inputs have an effect only during the correct high speed function. Any change on these inputs must occur only when the CP input is high.

3.5.5.13 ALIGNMENT EXCEPTION (AE) (OUTPUT)

The AMZ8065 BEP uses an 8-bit parallel mechanization of the feedback shift register configurations. Under certain conditions, the error pattern will not automatically line up in predetermined positions of the register array during the correction operations. High on the AE output indicates that such a condition has been detected. The BEP automatically switches into the one-bit shift mode. The number of clocks for which the AE output is high is used in the error location calculation.



NOTE: Pin 1 is marked for orientation.

FIGURE 3.5-4. BEP CHIP

3.5.6 BEP FUNCTIONAL DESCRIPTION

Figure 3.5-5 is a block diagram of the Burst Error Processor. It consists of four major sections; Register Array, Polynomial Divide Matrix, Status Logic and Control Logic.

3.5.6.1 REGISTER ARRAY

This section consists of 56 flip-flops used for check bit computation during write operation, syndrome computation during read operation and error pattern extraction during error correction operation. In general, the Polynomial Divide Matrix provides the bit patterns required for the Register Array. The combination of Register Array and Polynomial Divide Matrix mechanizes the familiar serial form of feedback shift register arrangement into an 8-bit parallel form. The Q_0-Q_7 outputs of the BEP are obtained from the Register Array. When correction operations are complete, the error pattern is available on 12 outputs: eight bits on the Q_0-Q_7 outputs and the remaining four bits on the LP_0-LP_3 outputs. The Read Error Pattern (REP) input must be high for the error pattern to be available. The control logic generates clock signals for the Register Array.

3.5.6.2 POLYNOMIAL DIVIDE MATRIX

The Polynomial Divide Matrix is the heart of the BEP. The control logic decodes the Polynomial Select (S_0-S_1) and Function Select (C_0-C_2) inputs to generate the necessary gating signals to the matrix. The matrix establishes connections such that a byte of data presented on the D_0-D_7 inputs will be suitably divided by the selected generator polynomial. The BEP supports four different polynomials, selected by logic levels on the S_0-S_1 inputs. The DAU uses the 56 check bit polynomial only. The BEP can be used in three fundamentally different types of operations; write, read and correct. The various functions are selected by the C_0-C_2 control inputs.

3.5.6.3 WRITE

While data is being written on the disk, the BEP is in the compute check bits mode looking at the data bytes without affecting the flow of data to the disk. After the last data byte, the BEP is switched into the Write check bits function outputting the 4, 5, 6 or 7 check bytes. This is the additional information appended to the data stream that allows the detection and correction of possible read errors. The DAU uses seven check bytes only.

3.5.6.4 READ

When the read mode is enabled, bytes that are read from the disk traverse two paths. The first path directs the bytes through the A-register and into the store. The second path directs the bytes through the EDAC error detection circuitry. When information, both data and check bytes, is being read the BEP must be in either the read normal mode or the read high speed mode. These modes differ only in the correction algorithm that will be used if an error has occurred. In both modes parallel bytes are read into the BEP. After the last information byte has been entered the ER output is checked. If ER is low, there is no error. If ER is high, a read error has occurred. If an error is detected then further processing of the data is interrupted. If the detected error is in the data field then the correction mode is enabled. The read mode must be preceded by an EDAC clear.

3.5.6.5 CORRECTION

After the read operation, the syndrome held in the Register Array contains all the information necessary to find the error location and the error pattern. In the correct normal mode, the error location is found by counting the number of clock pulses required to make the EP output go high. The error pattern is then available on the LP_0-LP_3 and Q_0-Q_7 outputs. These outputs can be used to Exclusive "OR" with data for correction.

In correct high speed mode, the error location is also found by counting clock pulses, but they are routed in succession to the different sections of the register array. This results in slightly more complicated but substantially faster operation.

3.5.6.6 GENERATE

The seven data field EDAC bytes (56 bits) that are to be written onto a 4XX series disk are generated from the data field through the use of the 56th order polynomial generator. The S_0-S_1 inputs select this polynomial. They are both grounded in the DAU. When the data field is eventually read from the disk, errors are detected and corrected through the use of the high speed correction technique. Using this technique, a single error pattern that spans less than 12 bits can be corrected.

The sequence of operations necessary to generate the EDAC bytes is as follows:

1. The CP input is in the high state.
2. The BEP is initialized by activating the $\overline{MR}$ input low and then returning it high.
3. The S_0-S_1 inputs both low specify the 56 bit polynomial.
4. The C_0-C_2 inputs all low selects the compute check bits mode.
5. Place a byte of data on the D_0-D_7 inputs.

6. Make the CP input low and then high. This clocks the data into the BEP.

7. Keep repeating from step 5 until all data bytes have been entered.

3.5.6.7 WRITE CHECK BITS

In compute check bits mode the polynomial matrix and the Register Array are connected in a feedback shift register configuration. However, when write check bits code is established on the C_0-C_2 inputs, the feedback paths are disabled such that the register array will behave as a simple shift register. When the last data byte is entered in the compute check bits mode, the register array holds the check bits. These check bits will be available on the Q_0-Q_7 outputs, one byte at a time.

The sequence of events to write the check bits is as follows:

1. The CP input is in the high state.

2. Establish appropriate code on the S_0-S_1 inputs. This code must be the same as that used for the compute check bits function. The S_0-S_1 inputs both low specify the 56 bit polynomial.

3. The C_0 input high and the C_1 and C_2 inputs low selects the write check bits function.

4. After a propagation delay the Q_0-Q_7 outputs will contain the first check byte.

5. Make CP input low then high. The next check byte will be available on the Q_0-Q_7 outputs.

6. Repeat form step 5 until all seven check bytes have been read out.

3.5.6.8 READ HIGH SPEED

This function must be used for reading data if the Chinese remainder theorem method is to be used for error correction. In general, the Chinese remainder method accomplishes error correction in fewer clock cycles than the normal method. The only difference between read normal and read high speed modes is as follows: In the read normal, the input stream is divided by the expanded version of the polynomial, whereas in the read high speed mode, the input stream is simultaneously divided by all factors of the polynomial. Thus the high speed mode results in as many syndromes as the number of factors of the polynomial. If all syndromes are zero after entering the last check byte, the ER output will be low indicating error free operation. If there was an error the ER will be high.

The sequence of events in this mode are as follows:

1. The CP input is in the high state.

2. The S_0-S_1 inputs both low specify the 56-bit polynomial. This must be the same polynomial that generated the check bits originally.

3. The C_0 and C_1 inputs high and the C_2 input low selects the read high speed mode.

4. The BEP is initialized by activating the $\overline{MR}$ input low and then returning it high.

5. Present a byte of data read from disk to the D_0-D_7 inputs.

6. Toggle the CP input.

7. Keep repeating from step 5 until all data and check bytes are entered.

8. Test the ER output after entering the last check byte. A high on this output indicates a read error.

3.5.6.9 CORRECT HIGH SPEED

To employ the Chinese remainder theorem method, the syndromes must be obtained first using the read high speed function. This function gives as many syndromes as the number of factors in the polynomial. In other words, the register array is divided into four sections; each section implementing one factor of the polynomial. The first factor of every BEP polynomial is of the form $(X^c + 1)$. This factor is sometimes called the error pattern polynomial. The Chinese remainder theorem method requires that the syndrome obtained by the error pattern polynomial be repeatedly divided by the error pattern polynomial until the error pattern is found. The register section corresponding to the error pattern polynomial is repeatedly clocked. The error pattern is always characterized by a known number of consecutive zeros at predetermined bit positions.

After locating the error pattern, the error pattern register is prevented from clocking. Next, the register corresponding to the second factor is repeatedly clocked until it matches the error pattern and then this register is prevented from further clocking. This procedure is repeated for all remaining factors. As mentioned earlier, the P_0-P_3 inputs are provided in the BEP to control clocking of the individual registers and the PM_2-PM_4 outputs are provided to indicate matching of each register with the error pattern.

Every error detected may not necessarily be correctable.

If the number of clock cycles to find the error pattern exceeds the period of the error pattern polynomial, or the number of clock cycles required to match a register exceeds the period of the polynomial corresponding to that register, the correction process must be aborted. Table 3.5-1 lists the maximum number of shifts allowed for each of the four factors of the 56-bit polynomial.

TABLE 3.5-1. 56-BIT POLYNOMIAL MAXIMUM SHIFTS/FACTOR

FACTOR	MAXIMUM NO. OF SHIFTS
1	22
2	13
3	89
4	23

When the correction mode is enabled, the microprocessor executes the steps that are outlined below. If the error is determined to be uncorrectable then no further processing of the data occurs. If the error is determined to be correctable then the store address of the error is calculated by the microprocessor. The microprocessor then uses the hardware generated correction bits to correct the erroneous data bits that are located at the previously calculated store address. The recirculate mode is then enabled.

The sequence of events for the high speed correction process is as follows:

1. The CP input is in the high state. The ER output is high indicating an error from the read high speed operations.
2. Select the 56-bit polynomial using the S_0-S_1 inputs and specify correct high speed code on the C_0-C_2 inputs.
3. Set inputs P_0-P_3 low.
4. Two external registers (R_1 and R_2) must be initialized to zero.
5. Test the EP output. If the EP output is high, the error pattern has already been found and $M_1 = 8R_1 + R_2$. Bring P_0 input low and go to step 10. If the EP output is low go to next step.
6. Set the P_0 input high.
7. If the EP output is low, test the AE output. If the AE output is low, clock the CP input. Increment register R_1. If the AE output is high, clock the CP input and increment register R_2.
8. If $R_1 + R_2$ is greater than the period of the first factor (22), abort the correction process; the error is not correctable.
9. If the error is correctable, repeat from step 5.
10. Set input P_1 high.
11. Initialize external counter register M_2 to zero.
12. Test the PM_2 output. If the PM_2 output is high, the second factor located the matching error pattern. Set P_1 input low and go to step 16.
13. If the PM_2 output is low, clock the CP input and increment M_2.
14. If M_2 is greater than the period of the second factor (13), abort the correction process; the error is not correctable.
15. If the error is correctable, repeat from step 12.
16. Set P_2 input high.
17. Initialize external counter register M_3 to zero.
18. Test the PM_3 output. If it is high, the third factor located the matching error pattern. Set P_2 input low and go to step 22.
19. If the PM_3 output is low, clock the CP input and increment M_3.
20. If M_3 is greater than the period of the third factor (89), abort the correction process; the error is not correctable.
21. If the error is correctable repeat from step 18.
22. Set the P_3 input high.
23. Initialize external counter register M_4 to zero.
24. Test the PM_4 output. If it is high, the matching error pattern is found by the fourth factor. Compute the error location.
25. If the PM_4 output is low, clock the CP input and increment M_4. If M_4 is greater than the period of the fourth factor (23), abort the correction process; the error is not correctable.
26. If the error is correctable, repeat from step 24.

3.5.6.10 ERROR PATTERN INFORMATION

The discussion of the correct high speed function described the procedure for finding the error pattern and calculating the location of the error burst. The AMZ8065 provides the error pattern on 12 outputs. Eight bits on the Q_0-Q_7 outputs and four bits on the LP_0-LP_3 outputs. The DAU only uses 11 of these outputs, Q_0-Q_7 and LP_1-LP_3. It was also stated that the REP input must be high to read the error pattern from the BEP.

The error location calculated is always in number of bits. In the case of the 56-bit polynomial, the calculated error location value corresponds to the beginning of the error burst counting from the last check bit. The calculated error location is such that when 11 consecutive bits of the record are Exclusive ORed into the error pattern, the error burst is corrected.

3.5.7 RECIRCULATE MODE

After the data within the store has been corrected, it is then recirculated through the EDAC circuitry as if it had just been read from the disk. If an error is detected, it is an indication of a significant hardware or firmware problem. The correction mode will not be enabled. The recirculate mode must be preceded by an EDAC clear.

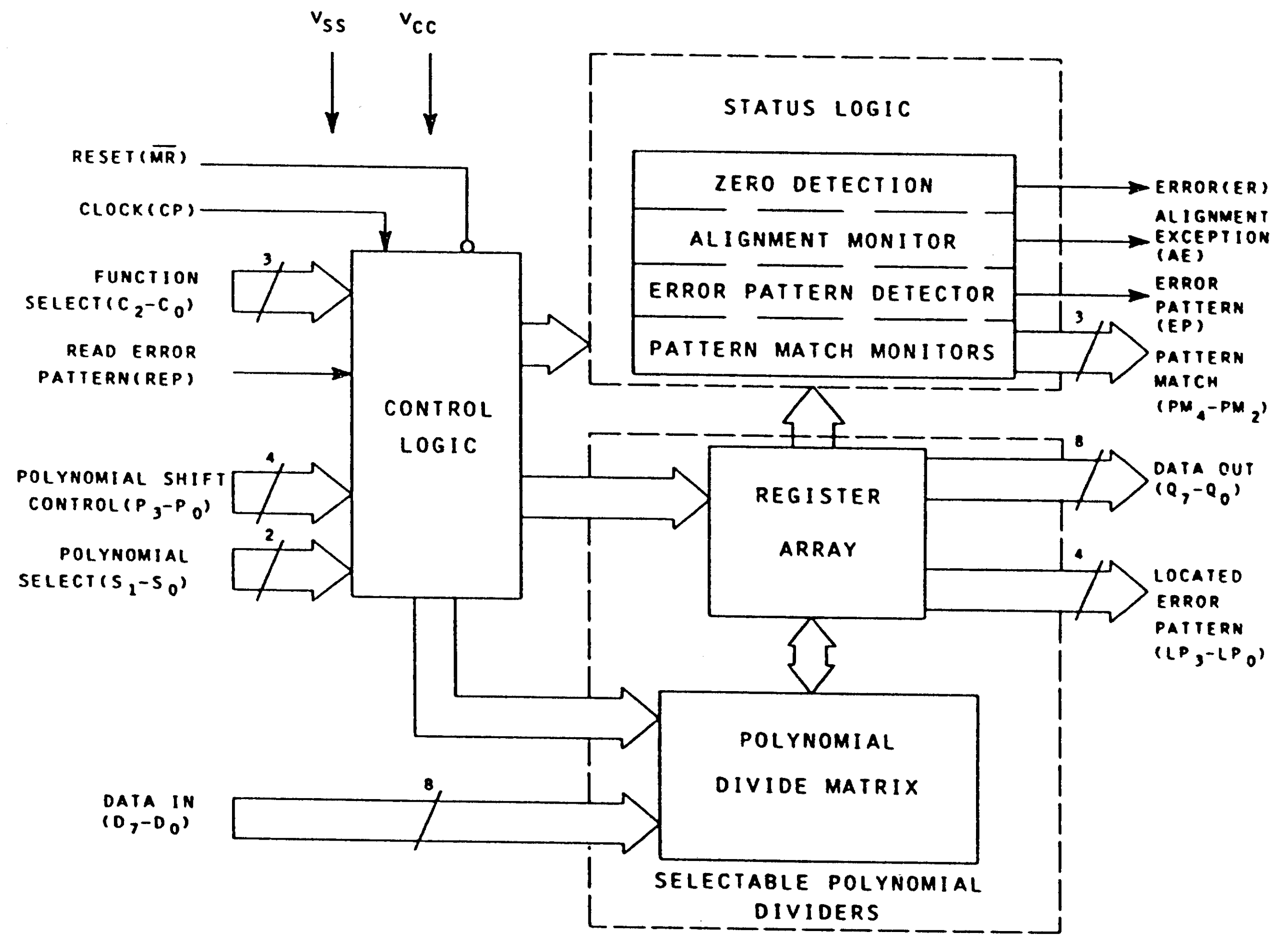


FIGURE 3.5-5. BURST ERROR PROCESSOR BLOCK DIAGRAM

3.5.8 ERROR CYCLIC CHECK (ECC)

The ECC logic is made up of four 4-bit Universal Polynomial Generator chips. The generator polynomial can be described by the expression (P_c = X^{16} + 1). The two count field EDAC bytes that are to be written onto a 4XX series disk are generated from the count field through the use of this 16th order generator polynomial. When the count field is eventually read from the disk, the same polynomial is used to detect errors. Errors detect on count field data for the 4XX series disk are not corrected. The count field error detection circuitry is enabled for both the read and the write modes.

3.5.9 CYCLIC REDUNDANCY CHECK (CRC)

The CRC logic is made up of three 4-bit Universal Polynomial Generator chips. The CRC polynomial is $X^{11} + X^9 + X^7 + X^6 + X^5 + X + 1$. This polynomial is a factor of the generator polynomial for both the count field and data field EDAC generators.

Effectively, the CRC logic compares the data with the appended EDAC characters. If the result is equal it indicated that the EDAC characters are a true representation of the data on which the EDAC was generated and the CRC will be zero. If the EDAC characters are not a true representation of the data then the CRC will not be zero. In the write mode, this CRC provides a check on the generated EDAC bits. In the read mode, the CRC provides an additional integrity check on the data. In the correction mode, the CRC ensures that the data has been corrected properly. The CRC chips are reset by a partial or EDAC clear.

3.5.10 EIGHT BIT COUNTER

Refer to Figure 3.5-6.

The 800 nanosecond clock, $BP-CLK, that is required by the clock input of the BEP is provided by an 8-bit counter. The 8-bit counter can be enabled by each of the following signals:

o	EDAC-4STB	EDAC STROBE (read or write mode).
o	DBSTB	B-REGISTER-FULL (recirculate mode).
o	R-DSYNC	MICROPROCESSOR WRITE STROBE (correction mode).
o	EDAC CLEAR	(all modes: 4XX or 50X).

3.5.11 EDAC CLEAR

Before the EDAC circuity is used to detect count field or data field errors, the sequencer issues an EDAC CLEAR. The clear serves two functions. The first function is to initialize the count field error detection shift registers to all ones. This initialization is required before count field EDAC bytes can be generated or read. The second function is to enable the 8-bit counter described above. The 8-bit counter is then used to provide the 800 nanosecond reset signal, ($CHP-RST), that is required by the BEP data field shift registers.

3.5.12 50X EDAC

3.5.12.1 OVERVIEW

EDAC as used for the 50X type device accommodates count fields of 8 or 16 bytes and data fields of 64 words (288 bytes) or 512 words (2304 bytes). Forty eight EDAC bits are appended to each field. The same polynomial is used to generate the EDAC bytes regardless of count or data field size, but four different polynomials are used during the checking process, one for each of the four different fields.

Input data, i.e. data or count fields, is partitioned into two segments, one consisting of even positioned bits, the other of odd positioned bits. Identical 24-bit shift registers operate on each segment simultaneously. This interleaved design provides for correction of single error bursts of length 4 or less and guaranteed detection of 16-bit error bursts or less with a very high probability of detecting bursts in excess of length 16. The partitioning of even and odd segments also greatly reduces the risk of miscorrection.

In addition, a Cyclic Redundancy Check (CRC) is used during writing, reading, and correcting to further increase data integrity.

3.5.12.2 50X WRITE

As write data is sent to the device, it is also sent to the EI board to generate the EDAC bytes for appendage to the data stream. After the EDAC bytes have been generated they will be returned to the EI board and used to check the data for integrity.

Once all the input data bits have been shifted through, the EDAC bytes can be read out by the sequencer or the microprocessor via a 1 of 8 selector on the output of the shift registers. The inverted outputs of the selectors are used, since the one's complement of the generated bits are actually stored on the device. This is because the EDAC bits for an all zeros field is all zeros, which is undesirable.

Input data from the D-register on the SE board is latched, even bits in one register (RE-RWC-DATA), odd bits in another (RO-RWC-DATA).

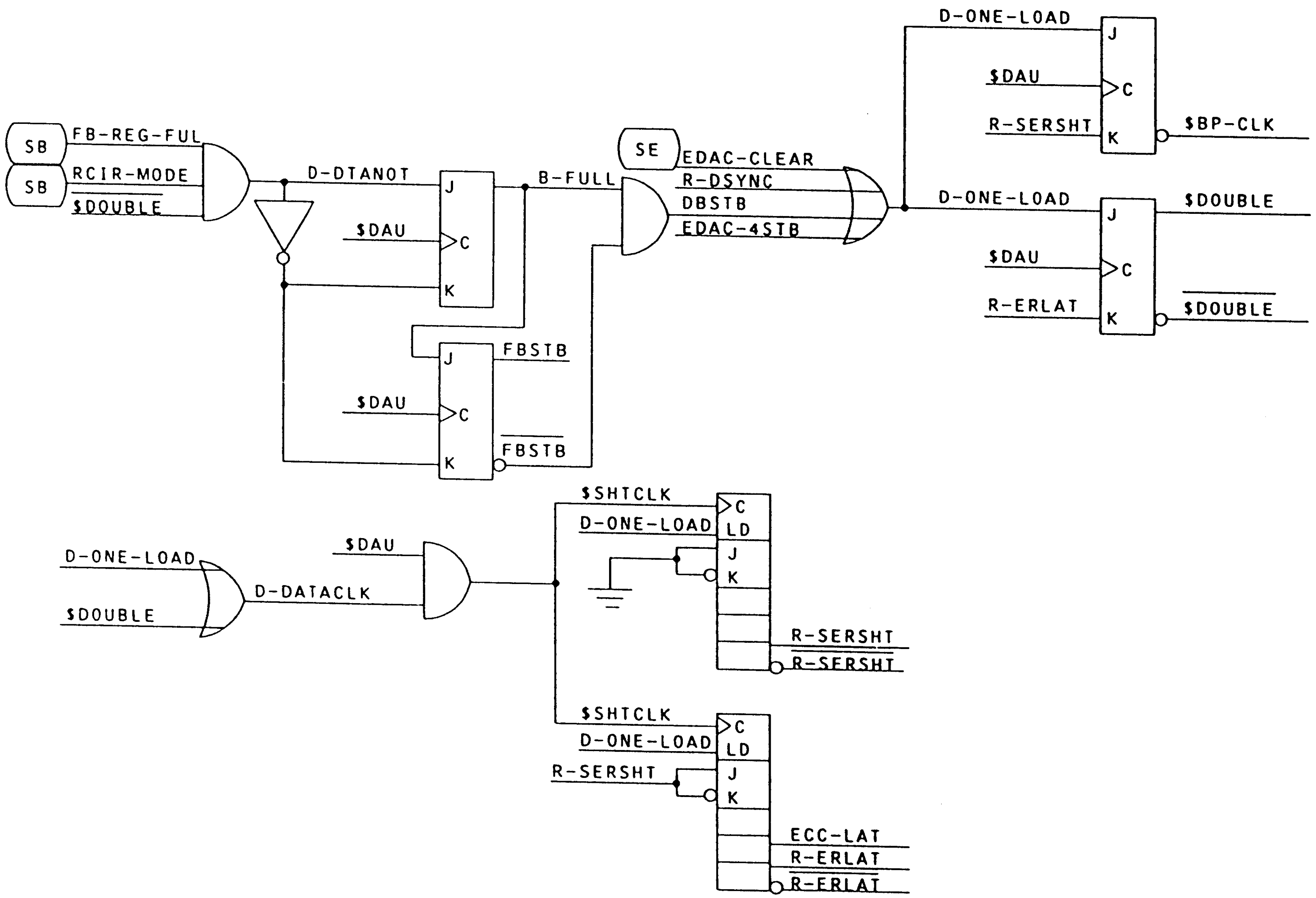


FIGURE 3.5-6. EIGHT-BIT COUNTER

These are shifted out serially through a shift register arrangement and into the even/odd EDAC generators, (RE-W00-W23 for even, RO-W00-W23 for odd) to generate the EDAC bytes. The polynomial represented by the shift registers is:

$$X^{24} + X^{23} + X^{22} + X^{21} + X^{20} + X^{15} + X^{14} + X^{13} + X^{10} + X^{9} + X^{3} + X^{2} + X + 1.$$

This is equivalent to the following polynomial which is most frequently seen in documentation and literature.

$$(X^{15} + X^{14} + X^{13} + X^{12} + X^{11} + X^{3} + X^{2} + X + 1)(X^{9} + 1).$$

After the EDAC bytes have been generated the sequencer will initiate their transfer to the device by entering the two's complement of the number of EDAC bytes (6) into the Sequencer State Counter (SEQ-STATE-5-7) and setting F-EDAC-BYTES. F-EDAC-BYTES inhibits the even/odd EDAC generators so that the EDAC bytes can be read out to the device. The transfer is complete when the State Counter reaches an all ones count. As the EDAC bytes are dispatched to the device, they are fed back via the D-register to the EI board for the CRC check. The EDAC bytes will cause the CRC to return to an all zeros value if no error was detected. If the CRC results is not all zeros, the F-EDAC-ERROR flip-flop will set (see Figure 3.5-2).

Notice, the write command disables the Even/Odd Shift Registers at the top of this drawing during the write operation.

3.5.12.3 CHECK

Read Data from the device is loaded into the store. It is also sent to the EI board to check its integrity. As in the generate process, input data is received from the D-register on the SE board, partitioned into even and odd segments and latched in parallel (RE-DATA for even bits and RO-DATA for odd bits). These are shifted serially out through a shift register with feedback. The EDAC bytes that were stored on the device then follow through the same path. They are inverted before being latched because the EDAC bits were inverted before being stored on the disk.

Depending on the type of field being read, the input data is gated into different locations in the feedback loop, effectively forming a different polynomial for each field. The polynomials represented are:

COUNT FIELD ZERO:	16 BYTES	$X^{19} + X^{18} + X^{15} + X^{14} + X^{13} + X^{8} + X^{6} + X^{5} + X^{4} + X + 1$
COUNT FIELD N:	8 BYTES	$X^{23} + X^{18} + X^{12} + X^{10} + X^{5} + X^{4} + X^{3} + X + 1$
DATA RECORD:	64 WORDS	$X^{23} + X^{16} + X^{13} + X^{10} + X^{7} + X^{5} + X^{4} + X + 1$
DATA RECORD	512 WORD	$X^{23} + X^{20} + X^{18} + X^{15} + X^{13} + X^{12} + X^{10} + X^{6} + X^{5} + X^{4} + X^{3} + X^{2} + X$

After the last EDAC byte has been shifted through, the two 24-bit shift registers contain what is called the "SYNDROME". If the syndrome (all 48 bits) equal zero, there has been no error. If any bit of the syndrome is one, and error has been detected, and the syndrome can be used to correct the error.

3.5.12.4 CORRECT

When an error has been detected, firmware will initiate the correction process. Correction is the same for any count or data field. It is accomplished by sending the data back, via the B-register on the SB board, through a parallel in/serial out register (RE-RWC DATA and RO-RWC-DATA) into a serial in/parallel out register (RC-REG) and back to the SB board. RCOR-MODE selects the B-register as input and disables the Even/Odd Shift Registers at the top of this drawing. As data is shifted through, the syndrome is also shifted, with zeros on the inputs. The data bits are exclusively ORed as they are shifted out of the Shift Registers with the bits being shifted out of the Syndrome Registers. Any data bit in error will be inverted by the Exclusive OR. When the first 22 bits in either syndrome are zero, the upper two bits indicate the location of the error, and are used to correct the data before it enters the Even/Odd CRC Register for validation. The corrected data is loaded into the Correction Register (RC-REG-00-07) and returned to the store for transmission to the system.

The Syndrome Register inputs are set to zero as its contents are shifted out. So, at the end of the shifting, these registers should contain all zeros if the data was corrected properly. If after all the bits (data plus EDAC) has been sent back through, the syndrome does not equal zero, the error was an uncorrectable one.

3.5.12.5 CYCLIC REDUNDANCY CHECK

An additional CRC check is performed on both the even and odd segments of the data for all three processes (generate, check and correct). The CRC polynomial is: $X^{16} + X^{11} + X^{4} + 1$.

This polynomial is a factor of the generator polynomial and exists on a single chip. The check is performed on even and odd segments separately. Effectively, the CRC logic compares the data with the appended EDAC characters. If the result is equal it indicated that the EDAC characters are a true representation of the data on which the EDAC was generated and the CRC will be zero. If the EDAC characters are not a true representation of the data then the CRC will not be zero. In the write mode, this CRC provides a check on the generated EDAC bits. In the read mode, the CRC provides an additional integrity check on the data.

In the correction mode, the CRC ensures that the data has been corrected properly. The CRC chips are reset by a partial or EDAC clear.

3.5.12.6 CONTROL AND READ OUT

During 50X generate and check, the sequencer has control of the EDAC logic. It sends an EDAC Strobe (EDAC-STB) to the EI board to signal that another byte of data or EDAC is to be transferred. This strobe is used to latch the even data bits in one four-bit register (RE-RWC-DATA) and odd data bits in another (RO-RWC-DATA). It is also used to load a one into a separate four-bit Shift Register (RCOUNT1-4) used for control. This control register acts as a counter by shifting the one out with the next four clocks. A nonzero state of this counter enables four clocks to be sent to the appropriate polynomial generators.

The sequencer also provides a signal to indicate when EDAC bytes are being transferred (F-EDAC-BYTES). This signal is latched and during the generate mode, is used to inhibit shifting of the shift registers containing the EDAC bytes. This is done so the the EDAC bytes can be read out and sent back through other logic on the EI board for the CRC check.

During the 50X correction process, the store board controls the EDAC logic. A handshaking arrangement exists between the SB board and the EI board such that the board receiving a byte of data sends back a signal to acknowledge its receipt. Data to be corrected comes from the B-register and the process proceeds as follows:

1. A partial clear is issued to clear the CRC checkers, without affecting the syndrome.

2. The correction mode bit (RCOR-MODE) is set on the SB board.

3. The SB loads a byte of data into the B-register and sends a B-register full signal (FB- REG-FUL).

4. The EI board latches the byte from the B-register, sends back a B-register acknowledge (DBREG-ACK), and starts its control register (RCOUNT1-4). This is the same control register used to generate and check the EDAC.

5. The control register is nonzero for four clocks, enabling the shifting of the data byte and the syndrome through the correction logic, and into the C-register.

6. The C-register full flip-flop (FCREG-FULL) is set and the signal is sent to the SB board.

7. The SB board receives the byte and sends back a C-register acknowledge signal (FCREG-ACK).

8. Steps 2 through 7 are repeated until all data and EDAC have been passed through the C-register.

9. If the syndrome equals zero and there was no CRC error (status byte = OF] the data has been corrected properly.

3.5.13 STATUS BYTE

0	1	2	3	4	5	6	7
0	INPUT DATA PE	EVEN CRC ERR	ODD CRC ERR	22 EVEN = 0	22 ODD = 0	24 EVEN = 0	24 ODD = 0

Bit

0 Not used

1 Input data parity error

2 Even CRC error

3 Odd CRC error

4 Zero detected on first 22 even syndrome bits

5 Zero detected on first 22 odd syndrome bits

6 Zero detected on all 24 even syndrome bits

7 Zero detected on all 24 odd syndrome bits

After a total or EDAC clear, the status byte should equal OF. A partial clear will clear bits 1, 2 and 3 only.

NOTE: In order to have access to the 50X status byte, one of the 50X bits in the sequencer's SEDC Register (CO, CN, 64 or 512) must be set to enable the 50X output selector and disable the 4XX selector, when the microprocessor or sequencer has control of the output selector.

3.6 SEQUENCER (SE)

3.6.1 SE OVERVIEW

The purpose of the sequencer board in the DAU is to provide a vehicle for the microprocessor and firmware to control the action of the disk devices.

This includes, seizing and/or releasing the device, obtaining summary and detail status, and performing seeks. The microprocessor sets up the sequencer to perform the actual read or write operation as requested by the external system.

In order for the microprocessor to perform it's required functions, the sequencer has been designed with numerous registers and counters which the microprocessor has the ability to load and read back. The sequencer has the capability, once started, of sustaining a read or write operation through numerous sectors on the disk. The limiting factor in this scheme is the ability of the microprocessor and system to keep the store empty on a read or the store full on a write operation.

3.6.2 SE BLOCK DIAGRAM

Refer to Figure 3.6-1.

Some of the sequencer logic resides on the microprocessor board due to space limitations. This logic consists of the flag, flag mask and cylinder/head address registers. This includes the compare logic and all of the defective track skip control logic.

3.6.3 HARDWARE DESCRIPTION

3.6.3.1 CONTROL REGISTERS

Let's go over the Major Block Diagram of the control registers. This block diagram depicts all of the control registers within the sequencer and the source of the information loaded into each one.

The microprocessor has the capability of loading the sequencer RAM, the Sequencer Address Counter, and most of the other registers. This includes the Port Number, Mode, Record Control (RCT), Count Sync Byte (CSYN) and Starting Record Count (SRC) Registers. Also the Flag Mask, Flag, Cylinder Lower (CL), Cylinder Upper/Head (CU/HD), and the two Defect Skip Registers (DEF 0 and 1). These last six (6) registers are located on the microprocessor board.

The sequencer can control the loading of some of the registers. These include the Sequencer State Counter (SEQ CTR), Field Count (FCT), Device Command (CMD), Status (STAT), and the EDAC Control (SEDC) Registers. The sequencer can also load the Sequencer Address Counter, Record Control (RCT), Count Sync Byte (CSYN) and controls the loading of the two Defect Skip (DEF 0 and 1) Registers with count field information from the device.

A couple of things about the registers should be pointed out at this time. You will note that the RCT and CSYN Registers can be loaded by either the microprocessor or the sequencer. Initially, before starting the sequencer into a read or write operation, the microprocessor must load both registers.

The RCT Register contains the two's complement of the number of records to be read, or the number of records from the starting record to the end-of-track. The CSYN Register will contain the starting count field number. The sequencer will also load these registers after an automatic head switch if it is allowed to do the switch.

The Cylinder Upper/Head Register is double buffered, i.e., the microprocessor must load this register twice prior to starting the sequencer into a read or write operation. The first load will place information into the secondary register and set a flip-flop indicating it is full. The second load will place the new information into the primary register and reset the full flip-flop.

The microprocessor may then decide to reload the secondary register with the next head number to be operated on, assuming the transfer will continue on multiple heads. This again will set the full flip-flop which will indicate to the sequencer that it is allowed to do the automatic head switch after finishing on the current track. When the current track has been read or written with no errors detected and the microprocessor has preloaded the next head information (cylinder upper must remain the same) the sequencer will be:

1. Send the next head number to the device
2. Transfer the Cylinder/Head information from the secondary to the primary register and reset the full flip-flop.
3. Preset the Count Sync Byte (CSYN) Register with a hex 80.
4. Preset the Record Count (RCT) Register with the two's complement of the number of records to the end-of-track.
5. Loop back to the top of the read or write sequence and prepare to continue the operation on the newly selected track.

This sequence of operations can continue throughout the current cylinder, as long as no error has been detected by the sequencer, the microprocessor continues to reload the next head number and the DAU/system is fast enough to keep the buffer either full (in a write command) or empty (in a read command).

3.6.3.2 DATA FLOW

Let us now go over the Major Block Diagram of the data flow. This block diagram depicts the data flow from the output FIFO, store or EDAC boards through the D-register to the device. Data also flows from the device through the D-register to the input FIFO, store or EDAC boards and to other control logic within the sequencer.

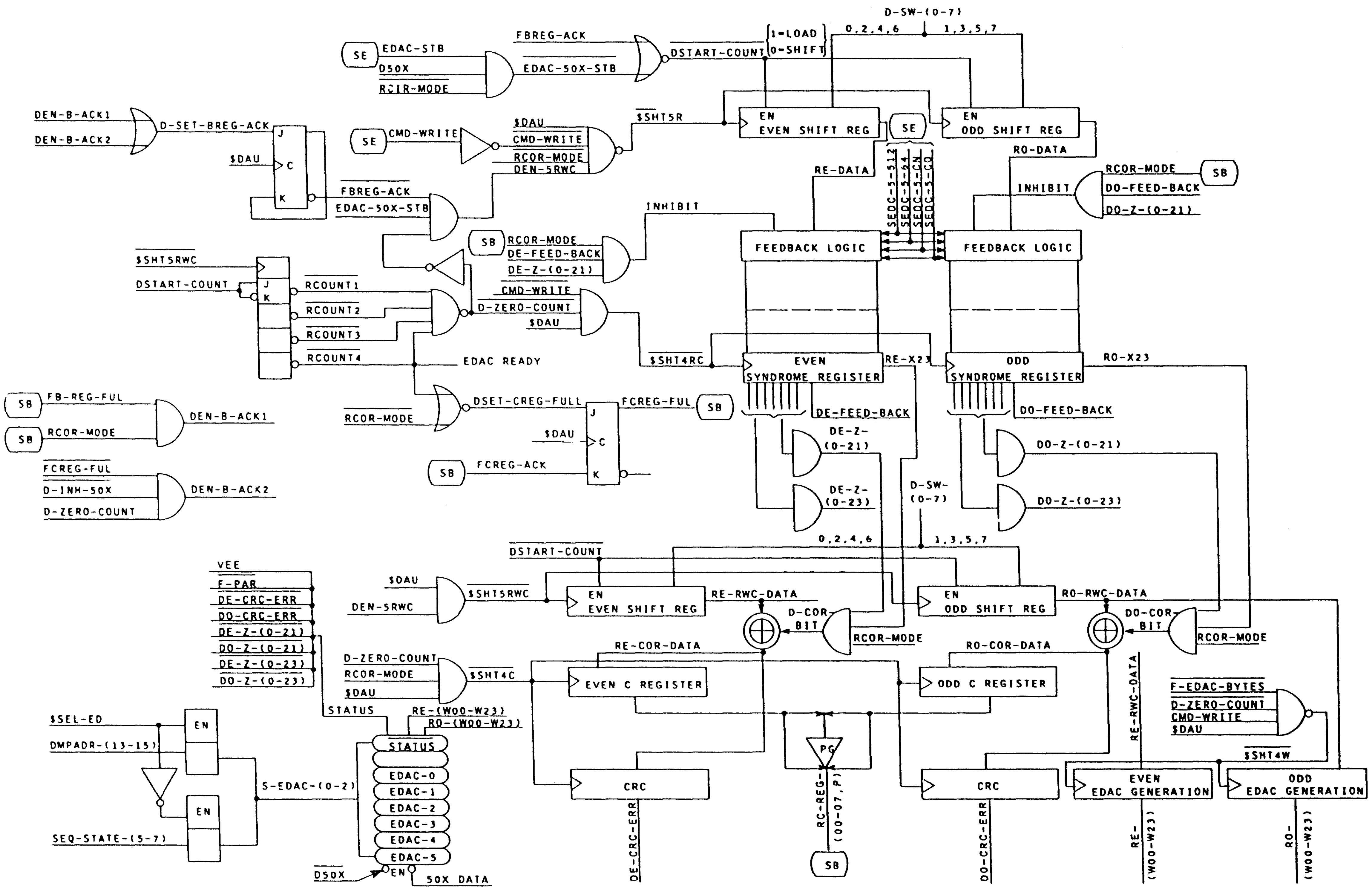


FIGURE 3.5-7. 50X EDAC MAJOR BLOCK DIAGRAM

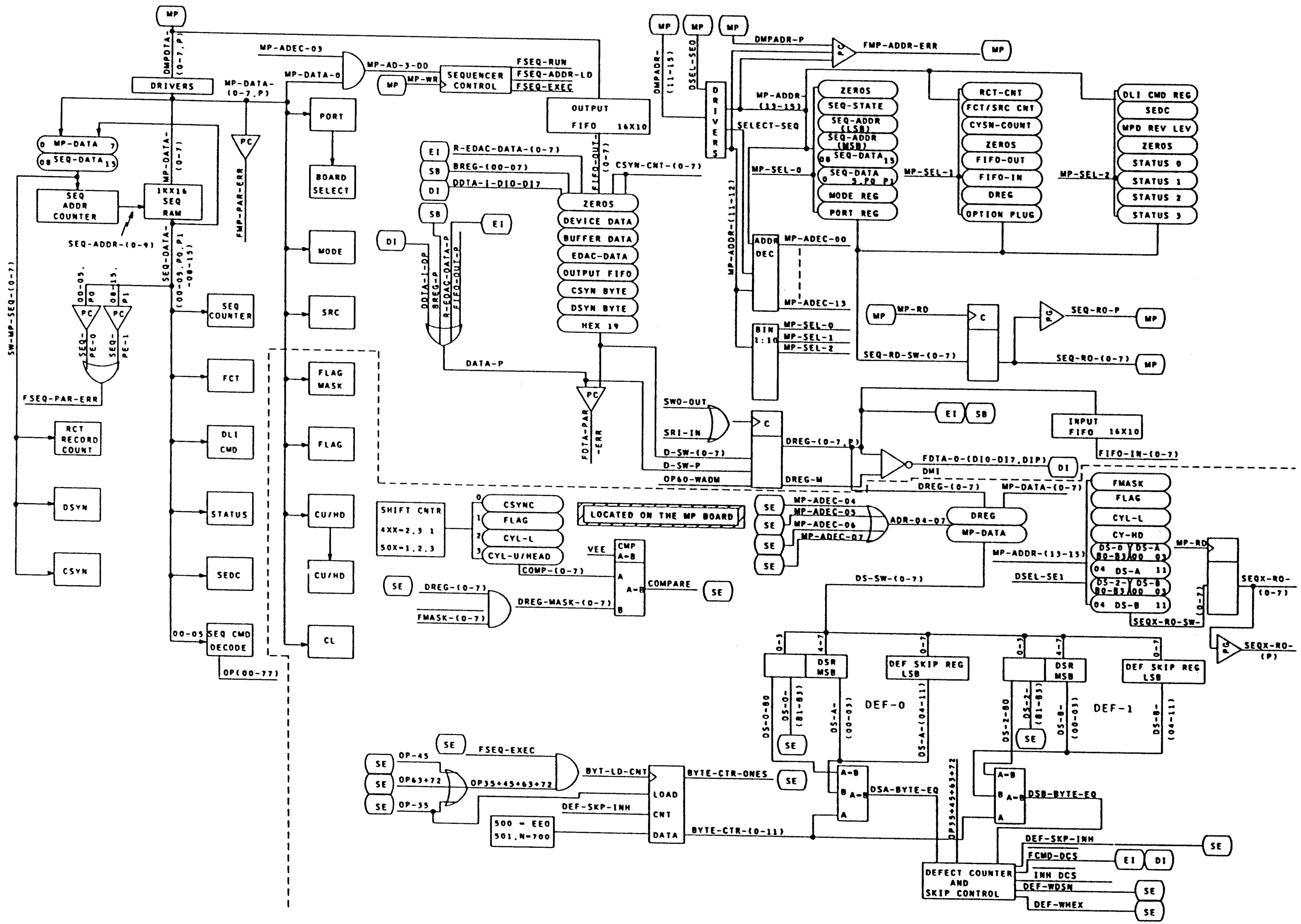


FIGURE 3.6-1. SEQUENCER LOGIC MAJOR BLOCK DIAGRAM

The D-register is the only register through which data or control information is communicated to/from the device.

The source of the data/control information to the device is from the output FIFO, the store or the EDAC boards through the D-register switch. The D-register switch is a one of eight selector. Other inputs to this switch consist of a hard wired zeros, and hex 19. Also the Count Sync Byte Register (CSYN) is inputted to two positions of the switch, one for writing the count field sync (CSYN) and the other for writing the data field sync (DSYN) byte. This is because the data field sync byte can be written improperly, on system command. The last position of the switch is utilized for inputs from the device for read type operations.

3.6.3.3 WRITE OPERATIONS

A very brief description of a write operation follows: After the count field has been read and verified the sequencer will:

1. Set the device into a write operation by loading the DLI CMD Register.
2. Enable the "Zeros" switch position and write a predetermined number of bytes of zeros for the gap area.
3. Enable the hex 19 and then the DSYN switch positions and write these bytes on the device.
4. Enable the store position of the switch and write the data from the store. This data is wrapped back to the EDAC board, for cyclic code generation, at the same time it is sent to the device.
5. Enable the EDAC position and write the applicable number of Error Detection and Correction bytes.
6. Lastly, the sequencer will enable the "Zeros" position again and write a few bytes of zeros, to make sure all the data bytes have been written.

3.6.3.4 READ OPERATIONS

During read operations, data/control information from the device enters through the D-register switch into the D-register. This information, depending upon the type of operation being performed at the time, is routed to the input FIFO (control or count field) or to the store/EDAC boards (data). The information is also utilized in the compare function and can also be placed into the Defect Skip Register.

A very brief description of the read operation follows. After the count field has been read and verified the sequencer will:

1. Set the device into a read operation by loading the DLI CMD Register.
2. Enable the device input position of the D-register switch and wait for the first byte of information from the device. This byte should be the data field sync byte, which is routed to the compare network. If this byte compares to the Count Field Sync Register then the read operation is continued with the data being routed to the store and EDAC boards.
3. With the device input position still enabled, the EDAC bytes are also received and routed to both the store and EDAC boards.
4. The Device Command Strobe (DCS) is then reset and the sequencer enters into a no-op delay loop of short duration. This is to allow the EDAC board to process the last EDAC bytes.
5. The sequencer will then test a signal from the EDAC board to see if there was an error on the just read data field. Based on the result, the sequencer will either halt or prepare to read the next count field.

3.6.4 CONTROL REGISTERS

3.6.4.1 ADDRESSING

The addresses utilized by the microprocessor to access the various registers and control functions within the sequencer board are shown below. Some of the registers are write only, some are read only and others have the capability to be loaded and read back. These are indicated by an asterisk under the column WR/RD.

The following is a list of the addresses used to access the various register. Refer to the following section for a full description of each register or control function.

ADDR	WR	RD	REGISTER/FUNCTION
B040	•		Control/Clear
B041		•	Sequencer State Counter
B042	•	•	Sequencer RAM Address (LSB)
B043	•	•	Sequencer RAM Address (MSB)
B044	•	•	Sequencer RAM Data/Instruction (LSB)
B045	•	•	Sequencer RAM Data/Instruction (MSB)
B046	•	•	Mode Register
B047	•	•	Port Select Register
B048	•	•	Record Count Register (Two's Complement)
B049	•	•	Starting Record (One's Complement 4XX only)
B04A	•	•	Count Field Sync Byte
B04B			Not Used
B04C	•	•	FIFO (Data out to Device)
B04D		•	FIFO (Data in from Device)
B04E		•	Data Register (D-Register)
B04F		•	Option Plug
B050		•	DLI Command Register (CMD to Device)
B051		•	EDAC Control Register
B052		•	Revision Level
B053			Not Used
B054		•	Status Register 0
B055		•	Status Register 1
B056		•	Status Register 2
B057		•	Status Register 3

The following addresses are utilized to access the registers located on the microprocessor board.

ADDR	WR	RD	REGISTER/FUNCTION
B060	•	•	Flag Byte Mask Register
B061	•	•	Flag Byte Register
B062	•	•	Cylinder Lower Register
B063	•	•	Cylinder Upper and Head Register
B064	•	•	Defect Skip 0 Register
B065	•	•	Defect Skip 0 Register
B066	•	•	Defect Skip 1 Register
B067	•	•	Defect Skip 1 Register

3.6.4.2 REGISTER DESCRIPTION

The following is a description of all of the registers mentioned in the addressing section.

3.6.4.2.1 CLEAR AND CONTROL REGISTER (B040) (WRITE ONLY): This address is used to halt the sequencer or to clear appropriate registers.

0	1	2	3	4	5	6	7
HALT SEQ.				DEV. INIT.		FIFO IN	FIFO OUT

BIT

0 Halt the Sequencer: Used by the microprocessor to halt the sequencer if it is running. This may be caused by a defective count field (i.e., one that cannot be found or read).

1 Not Used

2 Not Used

3 Not Used

4 Device Initialize: The device currently selected by the Port Register is cleared/initialized. A "one" in this bit position sets the initialize flip-flop, a "zero" in this bit position resets the initialize flip-flop.

5 Not Used

6 The input FIFO (data or status) from the device is cleared. This FIFO is utilized as a receptacle for data/status from the device during control commands, (i.e., cylinder, head, status information fetches). It is also used during a read/write command by the sequencer. The count field information is placed here in case of a miscompare so that the microprocessor can figure out what went wrong.

7 The output FIFO (data) to the device is cleared. This FIFO is utilized as a receptacle for data, (i.e., cylinder, head, seek difference information) to be sent to the device.

3.6.4.2.2 SEQUENCER STATE COUNTER (B041) (READ ONLY): This readout gives an indication as to the progress of the sequencer in a particular state, (i.e., the number of times a state is repeated). The number loaded into this register must be in two's complement form. The register is then incremented until an all one's condition (runout) is detected.

0	1	2	3	4	5	6	7
SEQUENCER STATE COUNTER							

3.6.4.2.3 SEQUENCER RAM ADDRESS (LSB) (B042): This byte is the least significant byte of the Sequencer Address Register/Counter. The RAM address is used to step through and execute instructions out of the sequencer RAM.

0	1	2	3	4	5	6	7
SEQUENCER RAM ADDRESS (LSB)							

3.6.4.2.4 SEQUENCER RAM ADDRESS (MSB) (B043): This byte is the most significant byte of the Sequencer Address Register/Counter.

0	1	2	3	4	5	6	7
START SEQ.						SEQUENCER ADDR. (MSB)	

Bit

0 Start Sequencer: If this bit is "one" when this address is loaded the sequencer will start executing instructions from the sequencer RAM at the just loaded address.

1 Not Used
2 Not Used
3 Not Used
4 Not Used
5 Not Used

6 Most significant bit of the Sequencer Address Register.

7 Next most significant bit of the Sequencer Address Register.

3.6.4.2.5 SEQUENCER RAM DATA (LSB) (B044): This is the data (i.e., sequencer instruction information) which will reside in the RAM. This portion of the RAM data is the branch address, immediate data, of the instruction repeat count (i.e., the number of times the current instruction is repeated).

0	1	2	3	4	5	6	7
INSTRUCTION INFORMATION							

3.6.4.2.6 SEQUENCER RAM DATA (MSB) (B045): This is the data (i.e., sequencer instructions) which will reside in the RAM. This portion of the RAM data is the operation code (instruction). It also contains two bits of parity.

NOTE: When this data is read or loaded, the sequencer will automatically increment to the next sequential RAM address.

0	1	2	3	4	5	6	7
INSTRUCTION INFORMATION						P0	P1

Bit

0-5 Sequencer Instruction: This is the particular operation code that the sequencer will operate on.

6 P0: This bit is the odd parity bit for bits 0 through 5 of this byte. Parity is checked by the sequencer when the instructions are fetched from RAM.

7 P1: This bit is the odd parity bit for the instruction information byte (B044). Parity is checked by the sequencer when the instructions are fetched from RAM.

3.6.4.2.7 MODE REGISTER (B046): This register contains control flags which will effect the operation of the sequencer.

0	1	2	3	4	5	6	7
DEV. INH.	DIAG. SEL.	VERIFY	EDAC OVER-RIDE	RAR			DEST. COUNT SYNC

Bit

0 Device Inhibit: When this bit is set all sequencer outputs to the device are inhibited. This is utilized in conjunction with diagnostic select (bit 1) when it is desired to perform testing of the sequencer board.

1 Diagnostic Select: When this bit is set, it places the sequencer in a state so that test and diagnostics can be run, i.e., different data paths are enabled and the device timing is generated within the sequencer board.

2 Verify: When this bit is set, and the sequencer is placed in a read operation, the data from the device is sent to the EDAC board for verification, i.e., EDAC is calculated and checked. No data is sent to the store board.

3 EDAC override: When this bit is set and the sequencer is placed in a write operation, the EDAC data that is written to the device originates from the operating system via the store board. Normally the EDAC would come from the EDAC board. Note, when in a read operation, the EDAC bytes are always sent to the store board.

4 Read-Alter-Rewrite: This bit is utilized on the store board only, and is used to enable the short block function.

5 Not Used

6 Not Used

7 Destroy Data Field Sync Byte: When this bit is set and the sequencer is in a write or format operation the data field sync byte is destroyed (not written properly). This is used when the system program (MTAR) is attempting to recover a defective track and rebuild the data base.

3.6.4.2.8 PORT REGISTER (B047): This byte indicates to the sequencer the actual port, hence the physical device selected and also the type of format on that device.

```
    0       1       2       3       4       5       6       7
+-------+-------+-------+-------+-------+-------+-------+-------+
|       |       |       |       |                               |
|  T0   |       |  T1   |       |          PORT SELECT          |
|       |       |       |       |                               |
+-------+-------+-------+-------+-------+-------+-------+-------+
```

Bit

0 T0: This bit in conjunction with bit 2 defines the device type. See definition of T1 (bit 2) for device type coding.

1 Not Used

2 T1: This bit in conjunction with bit 0 defines the device type. The following is the code utilized for bits 0 and 2, to define the device type for the sequencer.

T0	T1	DEVICE TYPE
0	0	501 Device (512 word record 8/trk)
0	1	500 Device (64 word record 40/trk)
1	0	4XX Device (64 word record 40/trk)
1	1	5YY Device (64 word record 46/trk)

3 Not Used

4-7 Port Select: These four bits select the physical port on the DAU and hence the device. Bits 4 and 5 are decoded to select one of four port boards, and bits 6 and 7 are sent to the port board where they are used to select one of four ports.

3.6.4.2.9 RECORD COUNT REGISTER (B048): This register must be loaded with the two's complement of the number of records to be read/written or the number of records to the end of the track. The sequencer will increment this register after each record is read/written and when it becomes all "ones" it is time to switch heads (if allowed) or to stop.

```
    0       1       2       3       4       5       6       7
+-------+-------+-------+-------+-------+-------+-------+-------+
|                                                               |
|                      RECORD COUNT (RCT)                       |
|                                                               |
+-------+-------+-------+-------+-------+-------+-------+-------+
```

3.6.4.2.10 FIELD COUNT AND STARTING RECORD (B049): This register is divided into two parts: The field count (bits 0 through 3) are read only. The starting record (bits 4 through 7) are write and/or read.

```
    0       1       2       3       4       5       6       7
+-------+-------+-------+-------+-------+-------+-------+-------+
|                               |                               |
|          FIELD COUNT          |        STARTING RECORD        |
|                               |                               |
+-------+-------+-------+-------+-------+-------+-------+-------+
```

BIT

0-3 Field Count (read only): These four bits give an indication of the data field the sequencer was working on. This is used for the 4XX type of device only, where there are four (4) records for each count field.

4-7 Starting Record: These four bits, loaded in one's complement form, gives the sequencer the starting record number of a group of four used for the 4XX type of device only, where there are four records for each count field.

3.6.4.2.11 COUNT SYNC BYTE (B04A): This register, when loaded by the microprocessor contains the starting count field number, i.e., where the data transfer is to start.

0	1	2	3	4	5	6	7
1	0	COUNT FIELD SYNC					

BIT

0 This bit must be loaded with a "one". This is the most significant bit of the sync byte on all types of devices connected to the DAU.

1 This bit should be loaded as a "zero". It is not used as part of the count field sync byte. If loaded as a "one" the sequencer would not be able to compare the count field from the device.

2-7 These bits indicate to the sequencer which count field, hence which data field to search for before starting a data transfer.

3.6.4.2.12 FIFO OUT (B04C): This register will be loaded with information to be transferred to the device, i.e., head, cylinder and seek difference information.

0	1	2	3	4	5	6	7
FIFO OUTPUT TO DEVICE							

3.6.4.2.13 FIFO IN (B04D) (READ ONLY): This register will contain the information received from the device, i.e., cylinder, summary and detail status. This register is also used by the sequencer during a read of write operation. The count field information read from the device is saved in this register just in case the sequencer detects a miscompare on the count field. The microprocessor can then read this information and determine what went wrong.

0	1	2	3	4	5	6	7
FIFO INPUT FROM DEVICE							

3.6.4.2.14 DATA REGISTER "DREG" (B04E) (READ ONLY): This register is the main register to or from the device. All data and control information passes through this register.

0	1	2	3	4	5	6	7
DATA IN-OUT REGISTER							

3.6.4.2.15 OPTION PLUG REGISTER (B04F) (READ ONLY): This byte will convey the state of the backpanel option plug. It will be used to determine if, for example, the 501 type of device is allowed to be configured.

0	1	2	3	4	5	6	7
OPT 0	OPT 1	OPT 2					

Bit

0 Option 0: Spare option position

1 Option 1: Spare option position

2 Option 2: This option will indicate whether the 501 type (512 word sector size) device is allowed to be configured on the DAU.

3-7 Not Used

3.6.4.2.16 DLI COMMAND REGISTER (B050) (READ ONLY): This register, loaded by the sequencer, will contain the command to the device, i.e., head out, cylinder in or out, status request, seek lower, read, write, etc.

```
    0       1       2       3       4       5       6       7
+-------+-------+-------+-------+-------+-------+-------+-------+
|       |       |                                               |
|  R/W  |  O/W  |             DLI COMMAND TO DEVICE             |
|       |       |                                               |
+-------+-------+-------+-------+-------+-------+-------+-------+
```

Bit

0-1 Read/Write (R/W) and Output/Write (O/W): These bits are decoded and used by the sequencer to indicate the type of operation being performed on the device as follows:

R/W	O/W	Type of Operation
0	0	Control input i.e., detail status
0	1	Control output i.e., seek information
1	0	Read data transfer
1	1	Write data transfer

2-7 Command to the Device: Some representative commands are as follows (hex numbers includes bits 0 and 1). Refer to "PERFORMANCE SPECIFICATION FOR MASS STORAGE DEVICE LEVEL INTERFACE (DLI)", Number BL0026 for a full set and description of all DLI commands. Also, reference can be made to the specific device specification.

20	head in upper	44	seek reverse upper
21	head in lower	45	seek reverse lower
22	cylinder in upper	46	cylinder out upper
23	cylinder in lower	47	cylinder out lower
24	RPS input	48	head out upper
26	device number	49	head out lower
27	device type	50	seize device
28	summary status	51	release device
29	detail status 1	52	recalibrate
2A	detail status 2	53	set standby
2B	detail status 3	55	reset diagnostic
2C	detail status 4	58	shift positioner out
2D	detail status 5	59	shift positioner in
2E	detail status 6	7D	return track center
2F	detail status 7	A5	read data
3F	detail status 8	BE	read header
42	seek forward upper	CF	write data
43	seek forward lower		

3.6.4.2.17 EDAC CONTROL REGISTER (B051) (READ ONLY): This register, loaded by the sequencer, indicates to the EDAC board the type of device and the type of field the sequencer is writing or reading.

```
    0       1       2       3       4       5       6       7
+-------+-------+-------+-------+-------+-------+-------+-------+
|       |       |      4XX      |              50X              |
|       | DATA  |-------+-------+-------+-------+-------+-------|
|       |       |  CNT  | DATA  |  CO   |  CN   |  64   |  512  |
+-------+-------+-------+-------+-------+-------+-------+-------+
```

Bit

0 Not Used

1 Data: This bit when a "one" indicates that the sequencer is currently processing a data field in a read or write operation (used by sequencer only).

2 4XX Count Field: This bit indicates to the EDAC board that the sequencer is currently processing a count field from the 4XX type device.

3 4XX Data Field: This bit indicates to the EDAC board that the sequencer is currently processing a data field from the 4XX type device.

4 50X Count Field Zero: This bit indicates to the EDAC board that the sequencer is currently processing count field zero from the 50X type device.

5 50X Count Field "N": This bit indicates to the EDAC board that the sequencer is currently processing some other count field (other than zero) from the 50X type device.

6 50X 64 Word Data Field: This bit indicates to the EDAC board that the sequencer is currently processing a 64 word data field from the 50X type device.

7 50X 512 Word Data Field: This bit indicates to the EDAC board that the sequencer is currently processing a 512 word data field from the 50X type device.

3.6.4.2.18 REVISION LEVEL (B052) (READ ONLY): This byte will indicate the revision status of the DAU hardware. This is taken from a dip switch mounted on the sequencer board.

0	1	2	3	4	5	6	7
REVISION LEVEL							

3.6.4.2.19 STATUS 0 (B054) (READ ONLY): This is the first of four status bytes that the microprocessor can read to analyze what is happening or did happen in the sequencer.

0	1	2	3	4	5	6	7
SEQ. RUN	OPI DOWN	DEV. FAULT	R/W TTE	LAST DATA ERROR	SHORT BLOCK	NO DATA	ANY ERROR

Bit

0 Sequencer Running: This bit indicates that the sequencer is running, it is doing something.

1 OPI Down: This bit indicates that on the selected port the Operational In line from the device is down, i.e., the device doesn't exist or it is off line.

2 Device Fault: This bit indicates that the device on the selected port has developed a fault condition.

3 Read/Write Transfer Timing Error: This bit indicates that either the EDAC or the store board was not ready to transfer data or EDAC when the device either needed or wanted to get rid of another data byte.

4 Last Data Error: This bit indicates that the data counters on the store board and the sequencer board did not run out at the same time, i.e., either the store or sequencer indicates that there is more than or fewer than 288 or 2304 bytes written on the device.

5 Short Block: This indicates that while the sequencer was writing a 2304 byte record, the store detected a terminate from the PSIA before the next 2304 byte store was filled. The sequencer will automatically switch to a read operation and read the next 2304 byte record from the device, to prepare for a read-alter-rewrite.

6 No Data: This indicates that while the sequencer was in a data transfer operation the store either went empty (write) or filled up (read). The system was too slow.

7 Any Error: This is an indication that one of the error bits has been set in one of the first two status bytes.

3.6.4.2.20 STATUS 1 (B055) (READ ONLY): This is the second byte of status, error conditions detected by the sequencer.

0	1	2	3	4	5	6	7
DATA CC ERROR	DATA SYNC	DATA SYNC DS	COUNT MIS- COMP	COUNT CC ERROR	D-REG PARITY ERROR	SEQ. DATA PE	MICRO DATA PE

Bit

0 Data Cyclic Code Error: This indicates that the EDAC board has detected an EDAC error on the current data field.

1 Data Sync Error: This indicates that the sequencer has detected a miscompare on the data field sync byte.

2 Data Sync, Defect Skip, Error: This bit indicates that the sequencer hardware, while controlling a defect skip situation, has detected a miscompare on the data field sync byte following a defect.

3 Count Miscompare: This bit indicates that the sequencer has detected a miscompare on the count field from the device. The error could be in the flag byte or the cylinder or head bytes. The microprocessor will have to read the count field information out of the FIFO to determine the actual miscompare.

4 Count Cyclic Code Error: This indicates that the EDAC board has detected an EDAC or ECC error on the count field.

5 D-Register Parity: This indicates that we detected a parity error on data from the device or from the buffer or EDAC board.

6 Sequencer Data Parity Error: This indicates that during an instruction fetch from sequencer RAM a parity error was detected.

7 Micro Data Parity Error: This indicates that the sequencer has detected a parity error on data coming from the microprocessor.

3.6.4.2.21 STATUS 2 (B056) (READ ONLY): This status byte is mainly for information purposes only. It gives the state of some control flip-flops.

0	1	2	3	4	5	6	7
FIFO IN RDY	FIFO OUT RDY	CY/HD FULL	DEF. SKIP INH.	DEF. SKIP COMP	TWO DEF. COMP	FEQU	CSYN =0

Bit

1 FIFO Out Output Ready: This bit indicates that there is something in the output FIFO, to the device.

2 Cylinder/Head Register Full: This bit indicates that the microprocessor has loaded the next head address in the Cylinder/Head Register. This allows the sequencer to automatically switch heads at the end of the current track.

3 Defect Skip Inhibit: This bit indicates that the sequencer is currently processing a defect on the device and data is inhibited.

4 Defect Skip Compare: This bit indicates that the sequencer has detected a defect in the upcoming record or that it is currently processing a defect.

5 Two Defects Compare: This bit indicates that the sequencer has detected two defects in the current record being read or written.

6 FEQU: This bit indicates the current state of the equal (compare), flip-flop. This is used by the sequencer to hold the state of the compare on the count field or data field sync byte, when incrementing the record count, field count or starting record (all ones), and also when the count field (flag/cyl/head) is being compared.

7 CSYN = 0: This bit indicates that the Count Field Sync Register, (six least significant bits), contains "zero", i.e., the sequencer is searching for count field zero.

3.6.4.2.22 STATUS 3 (B057) (READ ONLY): This status byte is for information only. It contains the state of some of the flip-flops.

0	1	2	3	4	5	6	7
SWO	SRI	SY1	SY2	SY3	SY4		

Bit

0 Serial Write Out (SWO): This bit indicates the state of the handshake flip-flop. This is used to indicate to the device that the sequencer has received a byte or that the sequencer has a byte to give to the device.

1 Serial Read In (SRI): This bit indicates the state of the line from the device which indicates that the device has a data byte to send or that it has received a byte from the sequencer.

2-5 Sync States (SY1, SY2, SY3 and SY4): These bits indicate the state of the Sync Shift Register. This is used to sync the bytes received from the device to the DAU clocking scheme.

6-7 Not Used

3.6.4.2.23 FLAG MASK REGISTER (B060): This register, loaded by the microprocessor, is utilized during a read or write operation. It is a mask which is applied to the flag byte coming from the device such that specified bits are "don't cares". A "one" in any bit position will inhibit (not compare) that particular bit from the device.

0	1	2	3	4	5	6	7

3.6.4.2.24 FLAG BYTE (B061): This register, loaded by the microprocessor, will contain the flag byte that is expected from the device, (except for masked bits).

0	1	2	3	4	5	6	7
SIZE	HISI FMT			FIX HEAD	LOG TRK	TRACK INDICATOR	

Bit

0 Size: This bit indicates the size of the record on the device. A "zero" indicates 288 bytes, 64 word record sizes. While a "one" indicates 2304 byte, 512 word record sizes, (50X devices only). This bit is "zero" for 4XX type devices.

1 HISI Format: This bit indicates that the disk pack has been formatted utilizing HISI Program MTAR, i.e., not formatted at the factory, (50X type devices only). This bit is "zero" for 4XX type devices.

2-3 Not Used

4 Fixed Head: This bit indicates that this record resides on one of the fixed heads (50X devices only). This bit is "zero" for 4XX type devices.

5 Log Track: This bit indicates that the record associated with this count field consists of logging information, (50X type devices only). The log contains a record of all defects on the disk pack. This bit will be "zero" on 4XX type devices.

6-7 Track Indicators: These bits contain a code indicating the condition of the track.

Bit 6 7	
0 0	Good track (primary)
0 1	Good track (alternate)
1 0	Defective track alternate assigned
1 1	Defective track no alternate assigned

3.6.4.2.25 CYLINDER LOWER (B062): This register will contain the cylinder lower address of the current track being read or written. The sequencer utilizes this byte and compares it to the applicable byte from the device.

0	1	2	3	4	5	6	7
CYLINDER LOWER							

3.6.4.2.26 CYLINDER UPPER/HEAD (B063): This register, loaded by the microprocessor, will contain the address of the current track being read or written. The sequencer will compare this byte with the appropriate byte coming from the device.

NOTE: This register is double buffered, i.e., it must be loaded twice before the sequencer is started in a read or write operation or the contents can be read back. The reason for this is to facilitate the automatic head switching built into the sequencer. Refer to the Hardware Description Section for further information.

0	1	2	3	4	5	6	7
CYLINDER UPPER		HEAD NUMBER					

Bit

0-1 Cylinder Upper: These two bits are the most significant bits of the cylinder number, i.e., binary weight 512 and 256.

2-7 Head Number: These bits contain the physical head number being accessed by this operation.

3.6.4.2.27 DEFECT SKIP 0 REGISTER (B064): This register will be loaded by the sequencer when it is reading a count field from the device (50X only). It contains information concerning the "first" defect within this record.

0	1	2	3	4	5	6	7
DEF 0	DEF 1	DEF 2	DEF 3	DEFECT POSITION			

Bit

0 Def 0: This bit will indicate that there is a defect in the data field. If it is a "one" then bits 4-7 of this byte plus the next byte will contain the defect position.

1 Def 1: This bit will indicate that there is a defect in the gap between the count field and the cata field.

2 Def 2: This bit will indicate that there is a defect in the gap following the data field.

3 Def 3: This bit, used in count field zero only, indicates that there is a defect between the index mark and the first count field. This bit will be "zero" in all other count fields.

4-7 Defect Position: These four bits are the most significant bits of the defect position located in the data field, if bit 0 is a "one".

3.6.4.2.28 DEFECT SKIP 0 REGISTER (B065): This byte will contain the least significant bits of the defect position located in the data field, if bit 0 of the previous byte is a "one".

0	1	2	3	4	5	6	7
DEFECT POSITION							

3.6.4.2.29 DEFECT SKIP 1 REGISTER (B066): This register will be loaded by the sequencer when it is reading a count field from the device (50X only). It contains information concerning the "second" defect within this record.

0	1	2	3	4	5	6	7
DEF 0	DEF 1	DEF 2	DEF 3	DEFECT POSITION			

Bit

0 Def 0: This bit will indicate that there is a second defect in the data field. If it is a "one" then bits 4-7 of this byte plus the next byte will contain the defect position.

1 Def 1: This bit will indicate that there is a second defect in the gap between the count field and the data field.

2 Def 2: This bit will indicate that there is a second defect in the gap following the data field.

3 Def 3: This bit, used in count field zero only, indicates that there is a second defect between the index mark and the first count field. This bit will be "zero" in all other count fields.

4-7 Defect Position: These four bits are the most significant bits of the defect position located in the data field, if bit 0 is a "one".

3.6.4.2.30 DEFECT SKIP 1 REGISTER (B067): This byte will contain the least significant bits of the second defect position located in the data field, if bit 0 of the previous byte is a "one".

0	1	2	3	4	5	6	7
DEFECT POSITION							

3.6.5 SEQUENCER OPERATION CODES

The heart of the sequencer board is the SEQUENCER LOGIC itself. It consists of an address counter, 1K X 16 bits of RAM storage, and the operation code decoder. The operation codes are divided into four groups:

1. Branch Type Operations
2. Immediate Type Operations
3. Read Type Operations
4. Write Type Operations

The output of the sequencer RAM is shown below. The RAM contains the operation codes and instruction information.

```
  0   1   2   3   4   5   6   7   8   9   10   11   12   13   14   15
+---+---+---+---+---+---+---+---+---+---+----+----+----+----+----+----+
|                       |   |   |                                     |
|    OPERATION CODE     | P | P |      INSTRUCTION INFORMATION        |
|                       |   |   |                                     |
+---+---+---+---+---+---+---+---+---+---+----+----+----+----+----+----+
```

The operation code is the specific instruction being executed. This is decoded and used through out the logic. These codes will be defined in the following paragraphs.

The parity bits is the odd parity of each byte which is checked when the instruction is pulled from RAM.

The instruction information will contain different types of information based on the type of operation code. This will be explained in more detail during the description of the different types of operation codes.

BRANCH TYPE — This field will be the real branch address.

IMMEDIATE TYPE — This field will contain different information depending on the instruction. Some uses of this data is listed below:

1. This field will not be used
2. Will contain a value to be loaded into a register
3. Will be a control bit to reset a condition
4. Will be a status to be set in the Status Register

READ TYPE — This field will be the number of iterations of the operation code, i.e., the number of events or bytes to read.

WRITE TYPE — This field will be the number of iterations of the operation code, i.e., the number of events or bytes to write.

3.6.5.1 BRANCH TYPE

The following is a list of the branch type instructions, including the mnemonic (used in the firmware), its octal code (used in the logic diagrams), and a brief explanation of its function. The instruction information for the branch type operations will contain the address to be branched to, therefore the sequencer is able to branch plus or minus 255 locations, but only within the same segment, i.e., within a 256 location area.

MNEM	OP	DESCRIPTION
bun	00	Branch Unconditional: Just go to the address specified and continue execution from that instruction.
beq	01	Branch If Equal: If the equal flip-flop is set, based on the action of some previous operation (compare sync byte or count field), then the branch is taken.
bcce	02	Branch If Cyclic Code Error: If an ECC or EDAC or AUX error has been detected by the EDAC board, then the branch is taken.
bsnz	03	Branch If Sync Byte Zero: If the six least significant bits of the count field sync byte are "zero". This is because count field zero is longer than the rest of the count fields.
bbfl	04	Branch If Buffer Full: If the store board indicates its buffer is full.
bsht	05	Branch If Short Block: If the store board had detected a terminate condition before the next 2304 byte buffer is full.
b501	06	Branch If Device Is 501: If the bits in the Port Register indicate this is a 501 type device. This is because the gap sizes are different on the 500 vs the 501 type device.
bcs6	07	Branch If Count Sync Byte Bit 6: If count sync byte bit 6 = 0, a branch is taken because of the difference in gap length between records (sectors) within a group on the 4XX type device.
bcs7	10	Branch If Count Sync Byte Bit 7: If count sync byte bit 7 = 0, a branch is taken because of the difference in gap length between records (sectors) within a group on the 4XX type device.

MNEM	OP	DESCRIPTION
bs01	11	Branch If Defect Skip 0 Bit 1 = 0: If this bit is "zero" it indicates there is no defect between the count field and data field.
bs02	12	Branch If Defect Skip 0 bit 2 = 0: If this bit is "zero" it indicates there is no defect between the data field and the next count field.
bs03	13	Branch If Defect Skip 0 bit 3 = 0: If this bit is "zero" it indicates there is no defect between the index mark and the first count field.
bs21	14	Branch If Defect Skip 1 bit 1 = 0: If this bit is "zero" it indicates there is no defect between the count field and data field.
bs22	15	Branch If Defect Skip 1 bit 2 = 0: If this bit is "zero" it indicates there is no defect between the data field and the next count field.
bs23	16	Branch If Defect Skip 1 bit 3 = 0: If this bit is "zero" it indicates there is no defect between the index mark and the first count field.
bnft	17	Branch If New Format: If the code contained in the Port Register indicates 5YY, a branch is taken because of the different gap sizes.

3.6.5.2 IMMEDIATE TYPE

The following is a list of the immediate type instructions, including the mnemonic (used in the firmware), Its octal code (used in the logic diagrams), and a brief explanation of its function. The use of the instruction information will be explained for each operation code.

MNEM	OP	DESCRIPTION
dcss	20	Device Command Strobe (set): When this operation code is encountered the DCS flip-flop is set. The device command strobe is an indication to the device that the command lines contain valid information. The Instruction Information portion of thes command is not used.
dcsr	21	Device Command Strobe (Reset): When this operation code is encountered the DCS flip-flop is reset. This indicates to the device that the command is completed, and ignore the command on the command lines. The instruction information portion of this command is not used.
lcsn	22	Load Count Sync Byte: This operation code will load the count sync byte with the information contained in the instruction information (normally hex 80). This is utilized after a head switch, to prepare the sequencer to search for count field zero.
icsn	23	Increment Count Sync Byte: This operation code will increment the count sync byte after a read or write sector operation, to prepare the sequencer for the next sector. The instruction information portion of this command is not used.
lrct	24	Load Record Count Byte: This operation code will load the Record Count Register with the information contained in the instruction information byte. This is to prepare the sequencer for the next track after an automatic head switch.
ifct	25	Increment Field Count: This operation code will increment the Field Count Register. This register is utilized on the 4XX type of device only i.e., it keeps track of the specific sector of a group of four. The Instruction Information byte is not used for this operation code.
irct	26	Increment Record Count Register: This operation code will increment the Record Count Register. This register is utilized to keep track of the number of records remaining to be read, written or the number of records to the end of track. The Instruction Information byte is not used.
isrc	27	Increment Starting Record Count: This operation code will increment the Starting Record Count Register. This register is utilized to inform the sequencer what sector of a group of four to start the read or write (4XX only). The instruction information byte is not used.
xxxx	30	SPARE

MNEM	OP	DESCRIPTION
lcmd	31	Load DLI Command Register: This operation code will load the DLI Command Register with the command contained in the instruction information byte. This is the specific command to the device. Refer to the addressing section for a partial list of commands.
lfct	32	Load Field Count Register: This operation code will load the Field Count Register with the count contained in the instruction information byte (normally 4, in two's complement form). This register keeps track of the specific sector of a group of four (4XX only).
xxxx	33	SPARE
rctl	34	Reset Control: This operation code will perform different functions depending on the specific bit set in the instruction information byte. These functions are defined below:

Bit	
08	Not Used
09	Not Used
10	Not Used
11	Halt the sequencer if the Cyl/Head Register is not loaded. This will prevent an automatic head switch.
12	Halt the sequencer if we have detected a D-register parity error.
13	Not Used
14	Clear the input FIFO
15	Reset the FEQUAL flip-flop, to get ready for another compare.

MNEM	OP	DESCRIPTION
sedc	35	Set EDAC Control: This operation code will reset the EDAC control logic and also set the SEDC Register to indicate to the EDAC board the type of field the sequencer will be operating on next. i.e., count field, or data field and the length of each. Refer to the register definition section address B051 for specific bit definitions.
stat	36	Set Status Register: This operation code will set the Status Register with the contents of the instruction information byte. This will convey information to the microprocessor on the type of error detected or if there even was an error.
halt	37	Halt sequencer: This operation code is utilized to halt the sequencer. The instruction information byte is not used.

3.6.5.3 READ TYPE

The following is a list of the read type instructions, including the mnemonic (used in the firmware), its octal code (used in the logic diagrams), and a brief explanation of its function. The instruction information for the read type operations will contain the number of iterations of the operation code (i.e., the number of bytes to read, or in the case of the no-op, it is the number of no-ops to perform).

MNEM	OP	DESCRIPTION
ccsn	40	Compare Count/Data Field Sync Byte: This operation code will prepare the sequencer to perform a compare on the next byte of information coming from the device, which should be the count or data field sync byte. The sync byte is put into the input FIFO.
ccnf	41	Compare Count Field Bytes: This operation code will prepare the sequencer to perform a compare on the flag, cylinder lower, cylinder upper and head bytes read from the count field. This information is also put into the input FIFO.
ccnb	42	Compare Count Field Bytes: This operation code is similar to "ccnf" except that the information is sent to the buffer board.
xxxx	43	Not Used
xxxx	44	Not Used
rdds	45	Read Data, Defect Skip Control: This operation code will prepare the logic to read a data field from a 50X type device under defect skip control, (i.e., There may be defects on the media in the data field). This data is also sent to the EDAC board for error detection purposes.
rdtb	46	Read Data to Buffer: This operation code will prepare the logic to read a data field from the device into the buffer. This data is also sent to the EDAC board for error detection purposes.
rdtf	47	Read Data To FIFO: This operation code will prepare the sequencer to read the information from the device into the input FIFO.

MNEM	OP	DESCRIPTION
rdtx	50	Read Data To Register: This operation code will prepare the logic to read the information (normally the count field, defect skip) into the input FIFO and also into the appropriate Defect Skip Register.
recc	51	Read Cyclic Code: This operation will prepare the logic to read the cyclic code field from a 4XX type device. The ECC code is utilized on the count field only.
redc	52	Read EDAC: This operation code will prepare the sequencer to read the Error Detection and Correction Code from the device.
xxx	53	Not Used
idta	54	Ignore Data: This operation code will prepare the logic to read the data field and ignore its contents, (i.e., it is not used). This is so the sequencer can step over data fields, on the 4XX type of device, but still remain in sync. As an illustration, the sequencer must start reading or writing the second, third or fourth data field of a group on the 4XX. In order to do this the sequencer must remain in sync with the device through the previous records to be able to miss the write splice on a read or where to put the splice on a write operation. The splice is the area in the gap where the write is started.
xxxx	55	Not Used
xxxx	56	Not Used
NO-OP	57	No Operation: This operation code is just a no operation code, (i.e., it is used for delay purposes only).

3.6.5.4 WRITE TYPE

The following is a list of the write type instructions, including the mnemonic, its octal code and a brief explanation of its function. The instruction information for the write type operations will contain the number of iterations of the operation code (i.e., the number of bytes to write).

MNEM	OP	DESCRIPTION
wadm	60	Write Address Mark: This operation code is utilized by the sequencer to control writing the address mark on the device. This operation code is used during a format operation only.
wcsn	61	Write Count Field Sync Byte: This operation code conditions the sequencer to write the count field sync byte, used during a format operation only
wdsn	62	Write Data Field Sync Byte: This operation code will condition the logic of the sequencer to write the data field sync byte. This is used during all write operations, including format.
wdds	63	Write Data, Defect Skip Control: This operation code will prepare the logic to write a data field to a 50X type device under defect skip control, (i.e., there may be defects on the media in the data field).
wdtb	64	Write Data From Buffer: This operation code will prepare the logic to write a data field from the buffer.
wdtf	65	Write Data From FIFO: This operation code will prepare the sequencer to send the information (normally control) from the output FIFO. This information, for example, could be cylinder, head, seek difference, etc.
wdtx	66	Write Data To Register: This operation code will prepare the logic to write the information (normally the count field, defect skip) from the buffer and places it into the appropriate Defect Skip Register. This is utilized during a format operation only.
wecc	67	Write Cyclic Code: This operation will prepare the logic to write the cyclic code field from the EDAC board to a 4XX type device.
wedc	70	Write EDAC: This operation code will prepare the sequencer to write the Error Detection and Correction Code from the EDAC board to the device.
whex	71	Write Hex 19 Sync Byte: This operation code will enable the sequencer to write the hex 19 sync byte to the device.
wzds	72	Write Zeros, Defect Skip: This operation code will prepare the sequencer to write a data field of "zeros" under the control of the defect skip logic. Used during a format operation and on 50X type devices only.

MNEM	OP	DESCRIPTION
wzrd	73	Write Zeros, Data Field: This operation code will condition the logic to write a data field filled with "zeros". This is used during a format operation on the 4XX type of device only.
wzro	74	Write Zeros, Gap Area: This operation code will set up the sequencer to write a specific number of bytes of "zeros" to establish a gap area.
wzix	75	Write Zeros To Index: This operation code will condition the sequencer logic to write data bytes of "zeros" till the index mark is detected. This is used during a format operation only, to generate the gap from the last data field to the index mark.
xxxx	76	Not Used
widx	77	Wait For Index Mark: This operation code is utilized during a format operation only. It conditions the sequencer to wait for index mark before continuing the next operation code.

3.6.6 LOGIC GROUPS

In the following paragraphs the hardware will be separated into specific groups with a brief description of their operation given.

3.6.6.1 D-REGISTER DATA FLOW

Refer to Figure 3.6-2.

The D-register is the center of activity for transfer of information between the DAU and the devices. The transfers are accomplished by interface signals SWO-OUT and SRI-IN. Except for the address mark line (DREG-M), all data and control information applied to the D-register are routed through the D switch (D-SW-0-7). The address mark line is activated by sequencer op code (OP60) to write the device address marks.

Parity is checked for device data, buffer data, EDAC data and output FIFO data. A zero parity bit is generated for zeros, CSYNC, DSYNC and HEX 19 bytes.

The D-register contents is sent to the MP, SB, and EI boards and to the input FIFO. It is also sent to any DI boards that are installed. The Input FIFO is loaded with cylinder, summary and detail status from the device during a read (OP40+41+47). This information is retrieved by the microprocessor (MP-RD) with address B04D (MP-ADEC-13).

Information selected from the D switch is determined by the decode logic as follows:

DECODE	INFORMATION SELECTED
000	Zeros for writing gaps, defective skip areas and formatting.
001	Data from the device (SEQ 00 & $\overline{01}$).
010	Buffer Data: Write data (OP63), format zeros 50X devices only (OP72), EDAC bytes originating from the system (MODE-EDAC-RD). Write data from buffer (OP64), write format data into Defect Skip Register (OP66), Write Data, Defect Skip not inhibited (BUFF-WSTB).
011	EDAC Data: Write cyclic code (OP67) from EI board to 4XX device. Write EDAC bytes (OP70) from EI board to device.
100	Output FIFO: Load output FIFO data (OP65).
101	CSYNC bytes: Write count field sync bytes (OP61).
110	DSYNC bytes: Write data field sync byte (OP62) or Write Sync byte after defect skip area (DEF-WDSN).
111	HEX-19: Write this character after the defect skip area (WHEX).

3.6.6.2 COMPARE NETWORK

Refer to Figure 3.6-3.

The compare network is located on the microprocessor board, This network consists of the following: The Flag Mask, Flag, Cylinder Lower, Cylinder Upper/Head Registers, the compare switching logic and the comparator chips themselves.

The compare network is utilized to compare the count field or data field sync bytes which occurred before each field on the disk. Also, the count field bytes consisting of the flag, cylinder lower and cylinder upper/head bytes will be compared to verify we are on the correct head and cylinder. This would normally be a straight forward piece of logic but because of the difference in format, between the 4XX and 50X type of device, a unique gating network was required.

Table 3.6-1 shows the difference between the 4XX and 50X count fields. Both devices will have a hex 19, which the device utilizes to find the beginning of a field. This byte is not returned to the DAU. The count/data field sync byte in front of each field is the first byte sent to the DAU. These are not shown in the table.

TABLE 3.6-1. COUNT FIELDS FOR 4XX AND 50X DEVICES.

BYTE	50X	4XX
0	Flag	Cylinder Lower
1	Cylinder Lower	Cylinder Upper/Head
2	Cylinder Upper/Head	Flag
3	Record	Record
4	Def Skip 0	Cylinder Lower *
5	Def Skip 0	Cylinder Upper/Head *
6	Def Skip 1	Flag *
7	Def Skip 1	Record *
8	Cylinder Lower *	
9	Cylinder Upper/Head *	
A-B	Track Skip 3	
C-D	Track Skip 2	
E-F	Track Skip 1	

NOTE: The Count Field bytes followed by an asterisk are utilized for alternate track processing, i.e., if this track is formatted as defective, alternate assigned, these bytes will be the address of the alternate track.

The comparator switching logic will be the only area described in detail in this section. The one or four selector switch has as its inputs:

Select 0 Count Field Sync Register
Select 1 Flag Byte Register
Select 2 Cylinder Lower Register
Select 3 Cylinder Upper/Head Register

Now the challenge is to get the proper select code to the switch, and hence the proper information gated to the comparator at the proper time based on the device type.

The select inputs are controlled by a 4-bit Shift Register which is preset to a value of "0110" for the 4XX type of device and to "1101" for the 50X type of device. The two most significant bits of the Shift Register are utilized for the comparator switch selection process.

The output of these two bits will provide a selection code sequence of "10", "11" and "01" for the 4XX type of device and a sequence of "01", "10" and "11" for the 50X type of device.

It can be seen that each selection code will gate the proper register through the switch at the proper time and in the correct sequence so that the information from the specific device type can be compared.

It should be noted that the selection code of "00", which is used to gate the Count Sync Register through the switch for comparison is just the inhibit function, i.e., if the sequencer is not in the OP41-42 control state.

These bytes are compared with their corresponding bytes from the device (DREG 0-7). All compares are gated by the appropriate sequencer op code to set the EQUAL flip-flop. Then the sequencer will enter the BRANCH IF EQUAL state (OP01), and branch to the appropriate routine.

OP40 gates sync byte compares for those sync bytes located in their regular positions on the track. OP45 is used to gate a data sync byte that follows a defect skip area (WDSN). Should a miscompare occur in this case, DEF-SYNC-ERR sets. The sequencer is stopped, and the appropriate bits are set in status bytes 0 and 1. The EQUAL flip-flop is also set if the Field Count Register (FCT-ALL-1), Record Count Register (RCT-ALL-1), or the Starting Record Count Register (SRC-ALL-1) runs out (becomes all ones).

3.6.6.3 DEFECT SKIP LOGIC

Refer to Figure 3.6-4 for the following paragraphs.

The defect skip control logic also resides on the microprocessor board and consists of the following elements: The byte counter, the Defect Skip Registers (DEF 0 and 1), the defect skip comparator and the defect skip control logic itself. This defect skip function is applicable only for the 50X type of device. There is no skip function associated with the 4XX type of device. The defect skip logic is only utilized when a defect occurs in a data field. The defects in the gap areas are handled via the branch capability of the sequencer.

Before we get into the heart of the logic itself a brief description of the possibilities of occurrences of defects is in order. First of all it should be noted that there are a maximum of three defects on any one track and a maximum of two defects in any one record. A record, for this discussion, consists of the following: count field, gap 2, data field and then gap 3. To complicate matters, there are differences in the processing of the defects based on device type.

On the 500 type of device, any defect in the gap area will have a 512 byte skip (dead area) centered around the defect and there are no defects allowed in the data field. If a defect occurs where a data field would fall, a 512 byte skip area is placed before the count field thus pushing the count and data fields further down the track.

On the 500E, 501, or 501N type of device, the defect skip size will be 64 bytes wide in any area. Defects are allowed to fall in the data field.

Defects can occur in any gap area on the media, i.e., between the index mark and the first count field, between any count field and the associated data field, and between the data field and the next count field or index mark if it happens to be the last data field on the track.

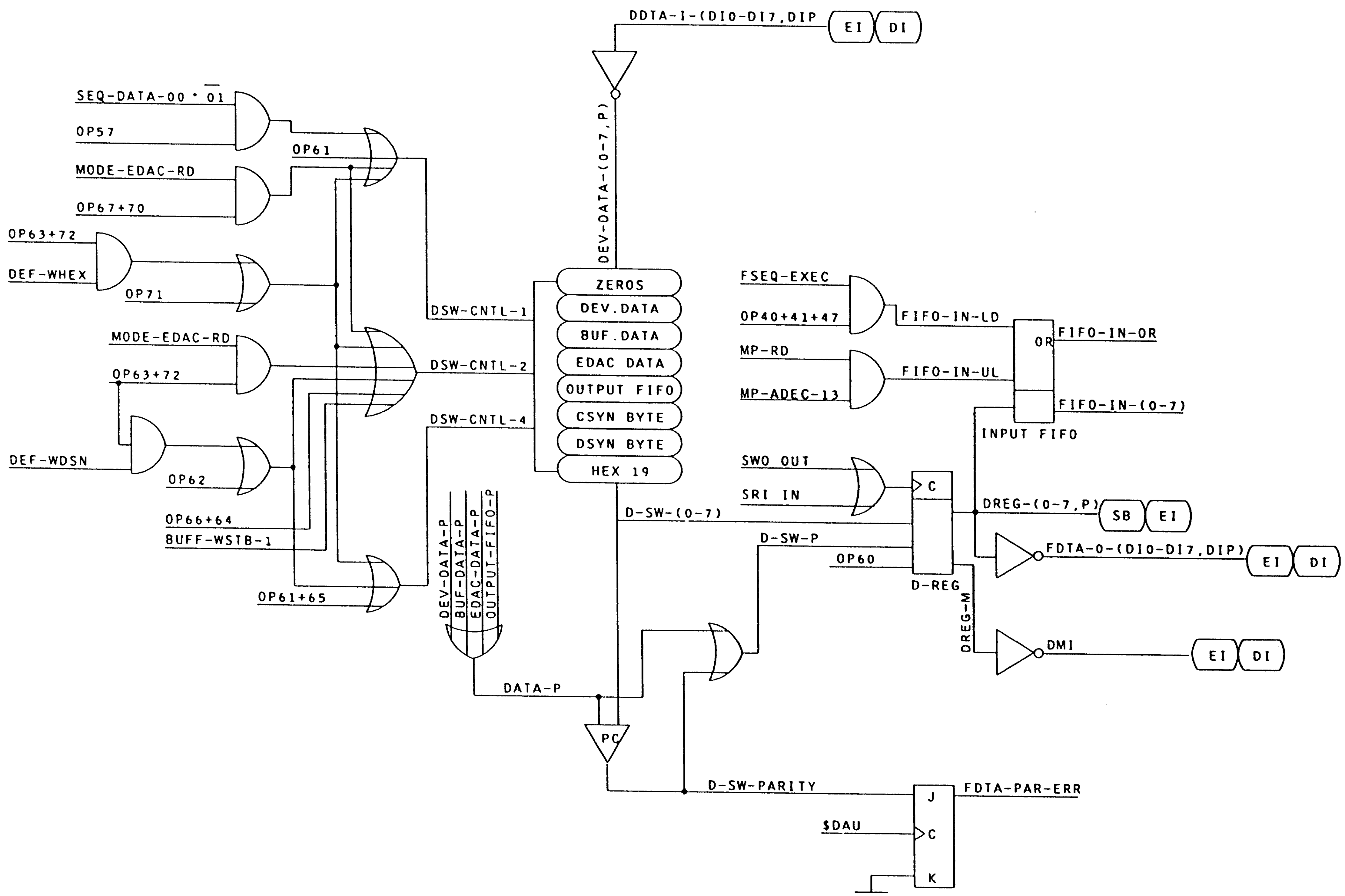


FIGURE 3.6-2. D-REGISTER AND INPUT FIFO

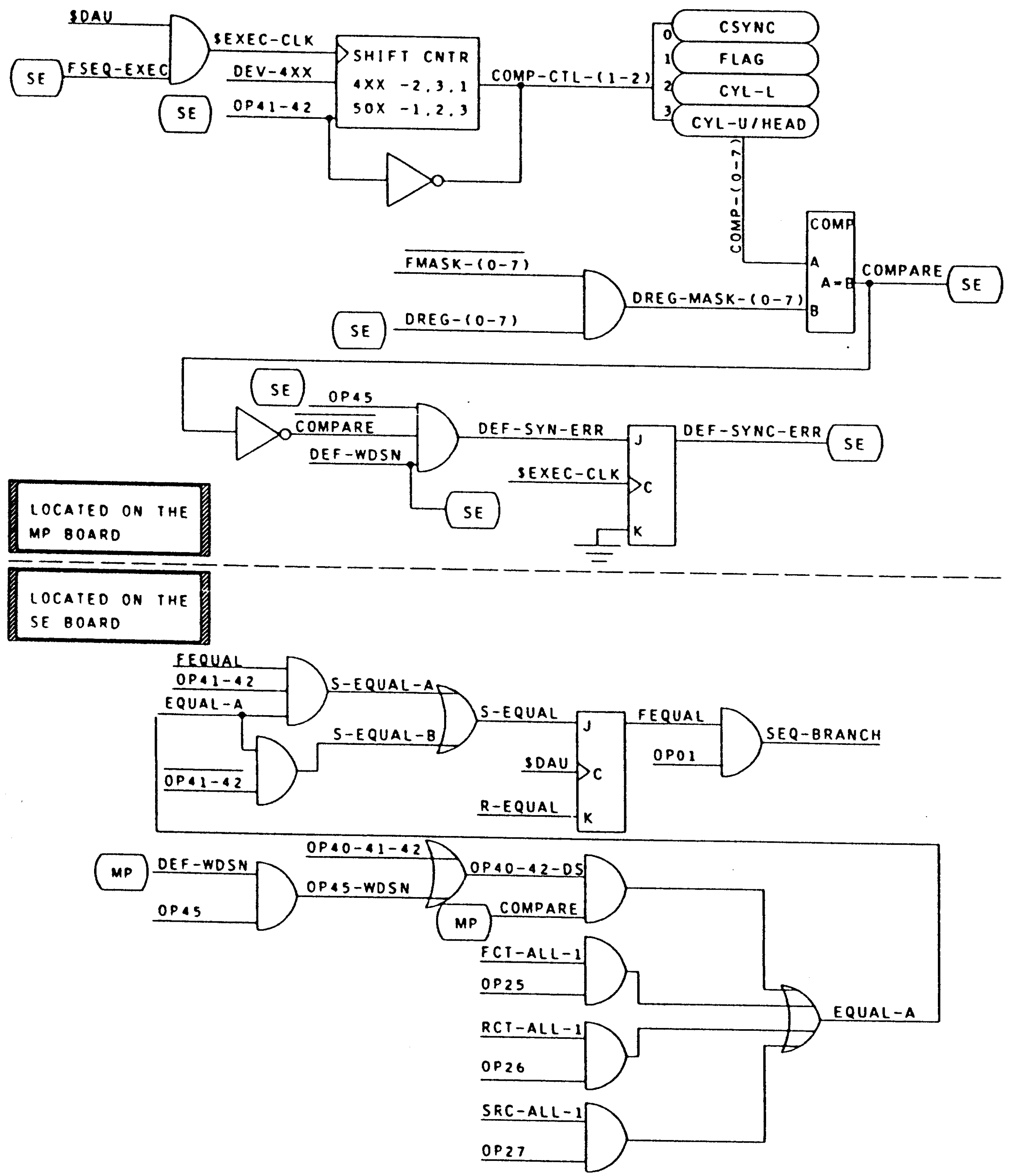


FIGURE 3.6-3. COMPARE GATING NETWORK

As was noted previously, there are a maximum of three defects per track and they can occur in any combination but only two defects in any one record, i.e., any count field, data field and associated gap area.

The two defects in any one record present some interesting possibilities. They could both occur between the count field and data field, both be in the data field itself, or be in the gap following the data field. They could also be split and we could have one Defect in any of two fields. Refer to the REGISTER DEFINITIONS section, addresses B064 through B067 for a description of the flags the sequencer utilizes to determine if and where the defects exist.

3.6.6.4 BYTE COUNTER

Refer to Figure 3.6-4.

The byte counter is a 12-bit counter which is preset to two different values based upon the device type which we are about to read or write. The counter is preset to the two's complement of 288 bytes for the 500 or 500E type of device, (actual preset value is EE0 Hex). The counter is preset to the two's complement of 2304 bytes for the 501 or 501N type of device, (actual preset value is 700 hex). The byte counter is loaded with one of these values when the sequencer is in the set EDAC control state (OP35).

The counter is incremented once for each byte read or written from/to the device (FSEQ-EXEC) when the sequencer is in the read (OP45) or write (OP63-72) mode. The end of the data field is indicated when this counter reaches an all ones condition.

The compare logic is enabled for "Compare If Equal" (A=B) only if bit 0 of the associated Defect Skip Register is set (DS-0-B0 or DS-2-B0). This bit indicates that a defect exists in the data field. The outputs of the compare logic is applied to the defect control logic.

3.6.6.5 DEFECT SKIP REGISTERS

Refer to Figure 3.6-4.

These registers consist of four 8-bit register chips which are utilized to hold the skip information until it is required during the actual read or write operation. They can be loaded by the microprocessor (MP-DATA-0-7) or by the sequencer (DREG-0-7) during the formatting or reading of a count field. These registers must be loaded by the microprocessor with count field zero defect skip information prior to a format operation.

Defect skip information is clocked ($EXEC-CLK) into the Defect Skip Registers by the microprocessor addresses as follows:

MICRO ADDRESS	ADDRESS DECODE	DEF-0 REG	DEF-1 REG
B064	MP-ADEC-04	MSB	---
B065	MP-ADEC-05	LSB	---
B066	MP-ADEC-06	---	MSB
B067	MP-ADEC-07	---	LSB

The registers are loaded from the sequencer by loading the sequence state counter with the two's complement of four (FC hex) and executing the appropriate read (OP50) or write (OP66) command. The Defect Skip Registers will then be loaded as the counter increments as follows:

SEQ STATE CTR 6	7	DEF-0 REG	DEF-1 REG
0	0	MSB	---
0	1	LSB	---
1	0	---	MSB
1	1	---	LSB

3.6.6.6 DEFECT SKIP COMPARE

Refer to Figure 3.6-4.

The defect skip compare logic is always comparing the byte counter with the two Defect Skip Registers. Remember, there is the possibility of two defects within one data field. These defects could be close together, double defect, (DOUBLE-DEF) or separated, in effect two single defects, (DEF-SKP).

3.6.6.7 DEFECT SKIP CONTROL

Whenever there is a defect on the media, its exact location is calculated, either at the factory during media certification or by a system program "MTAR" during media testing. A skip (gap) area of 64 or 512 bytes is centered around it. The calculated location, which is entered into one of the defect skip bytes in the count field is the two's complement of the number of bytes from the start of the data field to the edge of the skip area surrounding the defect.

During a format or write operation these skip areas will be written over with zeros. Now during a read operation, the device must be controlled such that it does not read through the defective area. This is because it may cause the read data recovery circuit to become unlocked.

The defect skip detection logic compares the output of the 12-bit byte counter (BYTE-CTR-00-11) with the output of the first Defect Register (DS-A-00-11) and the second Defect Register (DS-B-00-11).

The byte counter is loaded with the two's complement of the number of data bytes for a sector read or write. The Defect Skip Registers are loaded with the two's complement of the number of bytes from the beginning of the data field to the edge of the defect skip area. Therefore, a compare between the byte counter and a Defect Skip Register locates the beginning of the defect skip area within the data field.

When a compare between the byte counter and a Defect Skip Register occurs, signal DEF-RW comes true to enable this section of the defect skip control logic. The first thing that happens is the step counter starts counting with each $DAU-CLK.

At a count of one (PRESET-DS), the defect counter (DEF-CNT) is preset and a flip-flop (DEF-SKP-INH) is set which will inhibit the byte counter from counting. The preset value for the defect counter will depend on whether the operation is a read or a write. Data transfer to or from the store and EDAC boards is inhibited. If a read operation is in progress the control line DCS to the device is dropped thus stopping the read.

At a count of two (ENABLE-DS), the step counter is inhibited from counting further, the defect counter (DEF-CNT) is conditioned for counting, and if a read operation is in progress (OP45) the defect read counter (DEF-RD-CNT) is also enabled to count $DAU-CLK's.

Now, lets separate the discussion into what happens during a read operation, then we will go over the write operation.

3.6.6.8 DEFECT SKIP DURING READ OPERATION

The preset value for the defect counter (DEF-CNT) will be 28 decimal in two's complement (E4 Hex) if a single defect has been detected and 60 decimal in two's complement (C4 hex) if a double defect has been sensed.

During a read operation, when the flip-flop (DEF-SKP-INH) is set the device command strobe (DCS) line to the device is dropped which inhibits the read and stops all inputs from the device. Now with the byte clocks (SRIs) from the device stopped, the sequencer must have some way of timing out, (counting through the defect area) so the counter (DEF-RD-CNT) is utilized. This counter along with the preset values in the defect counter (DEF-CNT) were selected to generate a delay of sufficient length such that the device command strobe (DCS) control could be enabled between the defect and the sync bytes which follow the defect. The defect read counter (DEF-RD-CNT) will divide down the DAU-CLK, i.e., for each 16 DAU-CLK's the defect counter (DEF-CNT) is incremented by one. When DEF-CNT reaches an all one's value, the signal DEF-WDSN becomes true which allows DCS to be sent to the device. Thus restarting the read operation.

The device then looks for the Hex 19 sync byte and when found sends the next byte (data field sync) to the sequencer. This byte generates an execute signal (FSEQ-EXEC), which will reset the DEF-SKP-INH flip-flop.

This byte is also compared to the count field sync byte to make sure no records have been skipped. When DEF-SKP-INH resets it allows the following bytes of information from the device to be sent to the store and EDAC boards. Thus restarting the read operation and EDAC generation.

3.6.6.9 DEFECT SKIP DURING WRITE OPERATION

The preset value for the defect counter in a write operation will be 66 decimal (BE Hex in two's complement form) for a single defect and 130 decimal (7E Hex in two's complement) for a double defect.

In the write mode of operation, when the DEF-SKP-INH flip-flop gets set, DCS control remains high. This allows the device to continue in a write operation. Data from the store board is inhibited, EDAC generation is stopped and 64 or 128 bytes of "zeros" are written on the device. The defect counter DEF-CNT is incremented by one for each byte written on the device.

The defect counter was preset to a value of either 66 or 130 decimal. After the 64 or 128 bytes of "zeros" are written, the signal DEF-WHEX becomes true which causes the hex 19 sync byte to be written on the device. On the count the counter reaches the maximum count (FF), signal DEF-WDSN comes true and the data field sync byte is written. After these bytes have been written, DEF-SKP-INH is reset thus restarting the normal write operation. The data from the store is again sent to the device and the EDAC board. EDAC generation is restarted, and the byte counter is enabled to count bytes as in a normal write operation.

3.6.6.10 SEQUENCER LOGIC

The following descriptions of the sequencer hardware will concern the logic implemented on the sequencer board. The heart of the sequencer is the sequencer logic itself. This logic consists of three flop flops (FSEQ-RUN, FSEQ-ADDR-LD and FSEQ-EXEC), the Address Register/Counter, the RAM, the State Register/Counter, the Command Decoder, the increment/branch decision logic and lots of control logic.

The speed of the sequencer is mainly driven by the device which is currently being used. For example, the 4XX data transfer rate is 806 KB, or one byte every 1.24 microseconds, whereas the 50X type of device has a transfer rate of 1.2 MB, or one byte every 834 nanoseconds. For the branch or immediate type of operation, the execution rate is 200 nanoseconds per instruction, or iteration count.

3.6.6.10.1 SEQUENCER CONTROL FLIP-FLOPS: Refer to Figure 3.6-5.

In order to get the sequencer running, the microprocessor must load the starting address of a routine into the Sequencer Address Register. When the most significant byte of the RAM address (MP-ADEC-03) is loaded, and bit 0 = 1 on the data bus, MP-START-SEQ sets. On the next clock FSEQ-SYNC sets which, in turn, sets the control flip-flop FSEQ-RUN. FSEQ-RUN enables the rest of the sequencer. It also indicates to the microprocessor that the sequencer is doing something. In many instances the microprocessor will simply loop on the set state of FSEQ-RUN waiting for the sequencer to complete its task. The FSEQ-RUN flip-flop will be reset with $TOT-CLR, if a halt sequencer instruction is received from the microprocessor, if an error is detected or when a HALT command is reached in the sequencer RAM.

The FSEQ-ADDR-LD flip-flop is set initially when FSEQ-RUN sets. It is then set at the completion of each operation code (i.e., whenever the address counter is incremented or loaded). This flip-flop is used to control the loading of the sequence state counter. FSEQ-ADDR-LD is reset on the next $MPD-CLK, with $TOT-CLR, or if an error is detected.

FSEQ-EXEC is a flip-flop which is utilized to define one MPD-CLK as special, (i.e., it is the one that will be used to clock or increment registers/counters. The set function for the FSEQ-EXEC flip-flop consists of the following:

1. A no-op instruction is decoded (OP57).
2. For any branch or immediate instruction (SEQ-DATA-00).
3. Each time a byte of information has been sent or received from the device (FSY2).
4. When the instruction "wzix" or "widx" is in operation and the index mark from the device is sensed (FINDEX).

FSEQ-EXEC is reset on the next $MPD-CLK, with $TOT-CLR, or if an error is detected.

3.6.6.10.2 SEQUENCER ADDRESS REGISTER/COUNTER: Refer to Figure 3.6-6.

The Address Register/Counter is a 10-bit counter utilized to access any one of 1024 locations of RAM storage. The microprocessor can load the full ten bits and thus start the sequencer at any location. The sequencer has been limited to being able to load only the least significant eight bits for the branch type instructions, thus giving a branch range of up to a maximum of 255 locations but only within the same segment or 256 location block.

The LSB is loaded by either address B042 (MP-ADEC-02) or by decode of any branch instruction. The MSB is loaded with the high order two bits upon decode of address B043 (MP-ADEC-03). The counter is loaded from the microprocessor data bus if the micro is performing a write (MP-WR) to the counter; otherwise, the counter will be loaded from the sequencer's RAM.

The counter increments when the MSB of the RAM is read or loaded (MP-ADEC-05). It is also incremented upon setting the execute flip-flop (FSEQ-EXEC) for any of the following conditions:

1. A no-op or and immediate type instruction was executed.

2. Control type information (SEQ-DATA-00 not read or write) has transferred (SEQ-ST-ONES State Counter Exhausted).

3. Read/write data transfers have completed (BYTE-CTR-ONES).

4. Device index (DEV-IDX) was detected while the sequencer was in OP75 or OP77 control state.

3.6.6.10.3 SEQUENCER RANDOM ACCESS MEMORY (RAM): The RAM memory consists of four 1K by 4-bit chips. This RAM contains the entire operating firmware for the sequencer. This includes all format, read or write commands or programs for normal operation. The RAM is loaded with the sequencer codes during DAU initialization. The LSB is loaded by address B044 (MP-ADEC-04) and then the MSB is loaded (MP-ADEC-05). SEQ-DATA-00-15 contains the op codes (00-05) in octal format, parity bits (06-07) for both bytes, and the instruction information (08-15). The sequencer starts executing the op codes in RAM when the FSEQ-RUN flip-flop sets, and stops when it resets. The RAM is loaded once during DAU initialization and need not be loaded again unless a parity error is detected or some overlay (maintenance) has been used which wipes out the code. Parity is checked on each instruction pulled from RAM and if bad, it will stop the sequencer.

3.6.6.10.4 SEQUENCER STATE COUNTER: The sequencer state counter (SEQ-STATE) is loaded when each instruction is pulled from RAM. It is loaded with the two's complement of the number of iterations of the instruction required. There may be cases where this information is not used but it is loaded anyway. This counter is incremented once for each FSEQ-EXEC strobe. When it reaches a count of all one's (runout) it indicates that the number off iterations of this instruction have been completed. The SEQ-ADDR Register is incremented by one and the next instruction is placed in execution.

3.6.7 SEQUENCER COMMAND DECODE

The sequencer command decoder is a straight forward decode of six bits of the op-code read out of the RAM. It will provide 64 unique codes (00-77 octal).

3.6.8 TYPICAL SEQUENCER OPERATION

The following is a listing of a small portion of the WRITE 50X firmware routine which resides in the sequencer RAM. This is taken directly from the DAU firmware listing. Refer to this listing for the the following discussion.

```
wr5_50X   dw   (lcmd + rdh)               set DLI cmd = read header
          dw (dcss)
          dw (rctl + 03h)                 reset fifo/flag
          dw (sedc + 0Ch)                 set edac control CO +CN
          dw (ccsn + low(-1))             compare count sync byte
          dw (beq + wr5_lpa - base)       test - count miscompare

          dw (dcsr)                       count miscompared
          dw (no-op + low(-50))           delay
          dw (bun + wr5_50X - base        go try again

wr5_lpa   dw   (ccnf + low(-3))           compare next 3 bytes
          dw (rdtf + low(-1))             read count to fifo
          dw (rdtx + low(-4))             read count def to def reg
          dw (bsnz + wr5_lpb - base)      test if CO

          dw (rdtf + low(-8))             read rest of CO

wr5_lpb   dw   (redc + low(-6))           read count edac
          dw (dcsr)
          dw (no-op + low(-5))            delay
          dw (bcce + d5_cedac-base)       test - count edac error

          dw (beq + wr5_lpc - base        test - count compared

          dw (bun + d5_cmiss-base)        count miscompared - exit

wr5_lpc   dw   (no-op + low(-40))         delay
          dw (lcmd + wrt)                 set DLI cmd - write
          dw (bbfl + wr5_lpd - base)      test - buffer has data

          dw (bsht + wr5_sht - base)      test - short block

          dw (bun + d5_ndata - base)      no more data to write
```

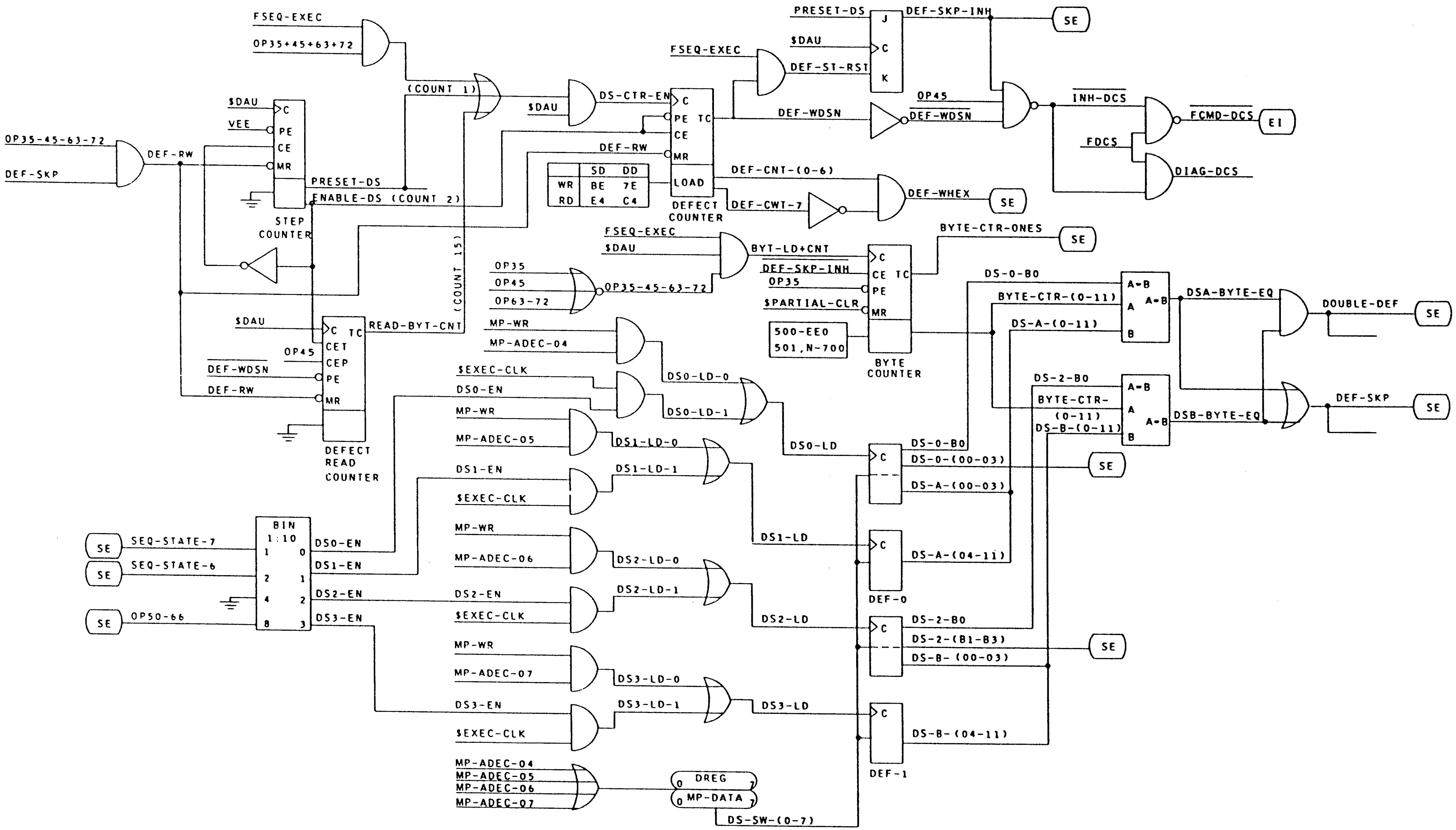


FIGURE 3.6-4. DEFECT SKIP LOGIC

NOTE: dw = declare word (2 bytes) - assembler pseduo-op.
low(-xx) = define negative number for instruction information

If the microprocessor decides that the command it is executing is a write command to a 50X type of device it will use the starting address of "wr5 50X". It loads this address into the Sequencer Address Register.

The sequencer will then start executing this piece of code. The first instruction "lcmd" will load the DLI Command Register with a read header "BE" command to the device. Then "dcss" will set the device command strobe indicating that the command lines contain valid information. Then while the device is looking for the address mark and hex 19 sync byte, the sequencer will execute a couple of miscellaneous instructions. The first, "rctl" will reset the input FIFO and clear the equal flag. Then the next instruction will preset the EDAC board and set the SEDC Register. This register tells the EDAC board what type of field the sequencer will be operating on next. When the sequencer gets to the next op code "ccsn", it will have to wait for the device to send the count field sync byte, and then perform the compare. The next instruction "beq" will test the equal flag to see if the sync byte compared to the CSYN Register.

If there was a miscompare the sequencer does not take the branch. It falls through and executes "dcsr", which will reset the device command strobe flip-flop. This shuts off the read operation. The sequencer then goes through a "NO-OP" delay before taking the "bun" back to the top and retrying the operation.

Now, if the compare was equal, the sequencer would take the branch to wr5 lpa, the "ccnf" op code. Here again the sequencer must wait for the device to send in bytes of information. The next three bytes of information, the flag, cylinder lower, and cylinder upper/head are place into the input FIFO and also compared to the appropriate register. While this compare is taking place the equal flip-flop is remembering this condition. The next instruction "rdtf" will read the record number byte into the input FIFO when it is received from the device. Then "rdtx" will read the defect skip information from the count field into the input FIFO and also into the Defect Skip Registers.

We now come to another decision point, "bsnz" instruction tests the condition of the Count Field Sync Register (six least significant bits are equal zero). This is required because count field zero on the device is a different length than the rest. If it is count field zero, the branch is not taken and the sequencer will execute the "rdtf" instruction immediately following the "bsnz". This will read the remainder of count field zero into the FIFO.

Now that the count field had been read the next instruction will read the EDAC bytes and indicate to the EDAC board that these are the EDAC bytes. The next op code will reset DCS strobe to the device, thus stopping the read. The sequencer will then delay for awhile utilizing the NO-OP instruction.

This is to allow the EDAC board to process the last byte of EDAC and determine if there is an error or not.

The sequencer operation now will test to see if there were any errors in the count field. The first check "bcce" will branch if there is an error indicated from the EDAC board. The next check "beq" will test the equal flag to see if the cylinder/head tested correct. Then there is the "bun" if all else failed, this branch indicates that there was a miscompare error (i.e., the device is not on the correct cylinder or head or the flag byte was in error).

This completes the discussion on the sequencer firmware.

3.7 DISK INTERFACE (DI)

Refer to Figure 3.7-1.

The disk interface is located on the WDAEI board and up to three optional MPCDI boards. This logic connects the DAU to the Mass Storage Units with dc coupled line transmitters and receivers. Data is transferred across the DLI on bidirectional transmission lines, I-DIO-DI7,P, with a single byte wide data path (eight bits plus parity) in a byte serial data transfer mode. The DLI dialog control signals are transmitted and received on separate lines. Each board can connect up to four MSUs but only one MSU at a time can be selected for operation.

3.7.1 DEVICE SELECTION CONTROL

The device selection control allows one MSU only to be selected for operation at one time. It consists of two 1-of-4 data select chips on each board. The four board-select lines, DBRD-SEL-0-3, from the DAU are hardwired to the corresponding board slot for board selection. The two device select lines, FDEV-SEL-2,3 control the output of the data select chips to select the MSU port data and control lines as follows:

FDEV-SEL 2	FDEV-SEL 3	MSU/PORT SELECTED
0	0	A
0	1	B
1	0	C
1	1	D

The control line, DEV-(A-D)-SEL/INH, activated by the selection process enables the transmitters and receivers for the port on the selected board and inhibits nonselected transmitters and receivers.

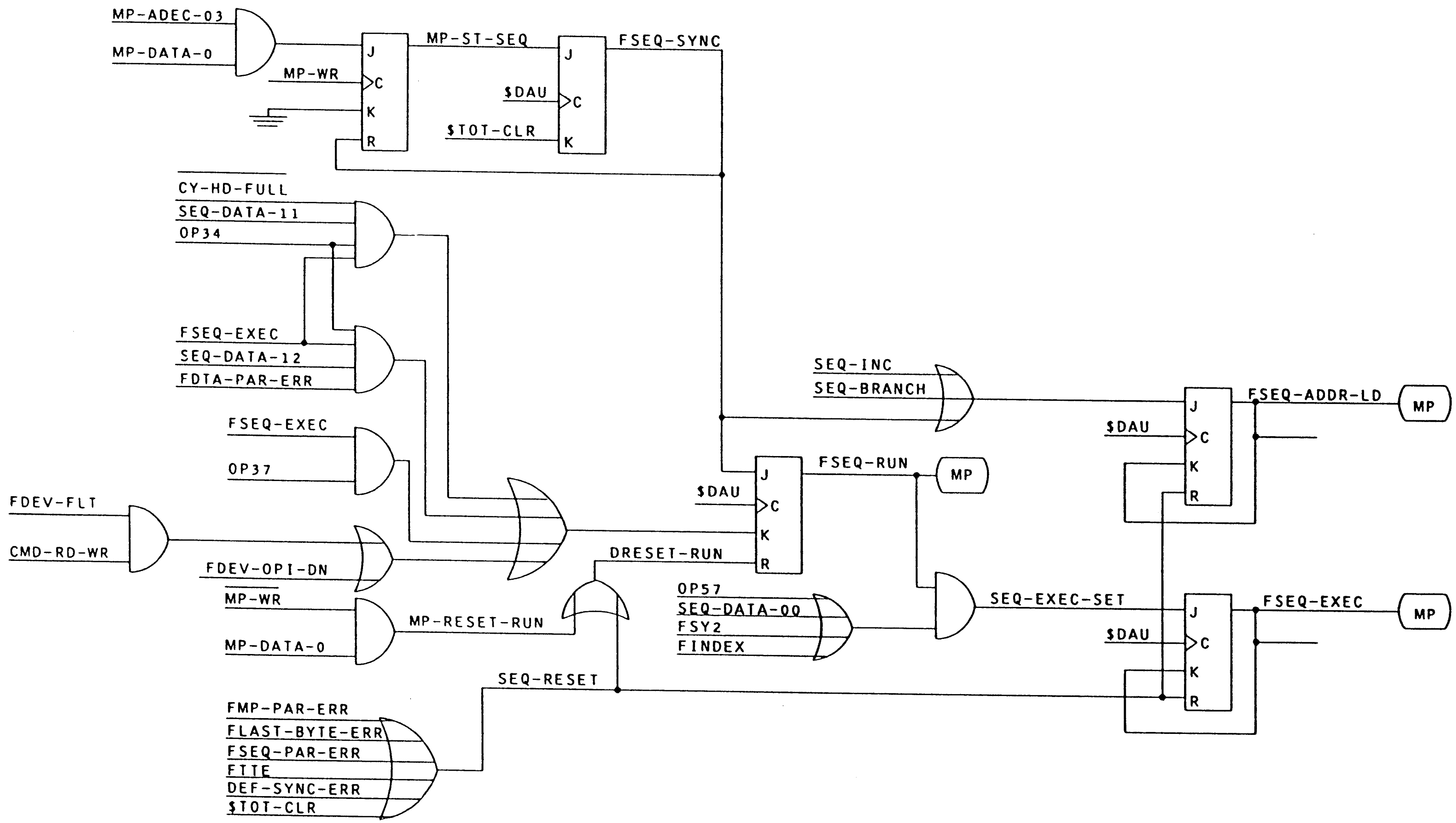


FIGURE 3.6-5. SEQUENCER CONTROL

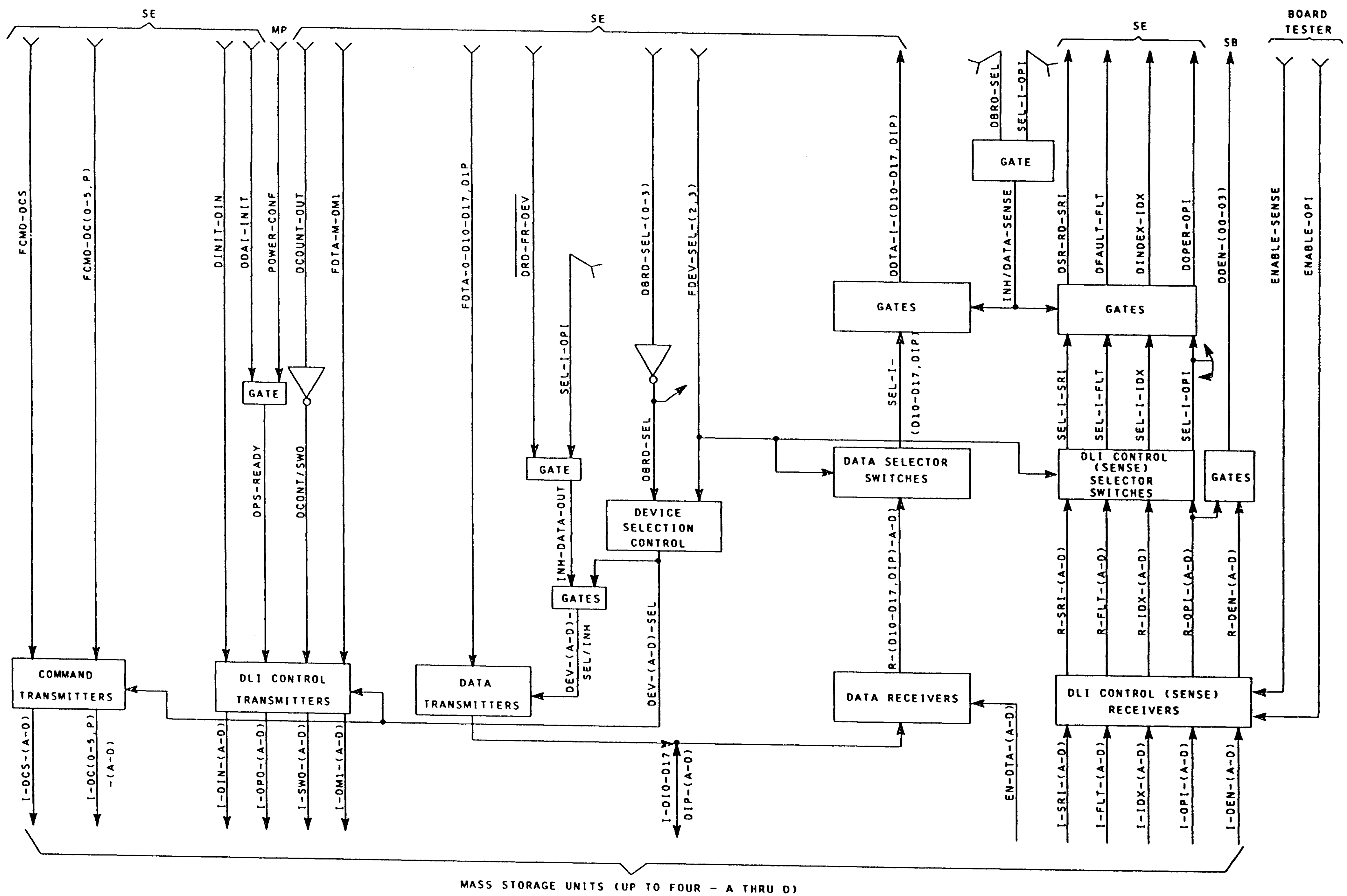


FIGURE 3.7-1. DISK INTERFACE (DI) (WDAEI AND/OR MPCDI BOARDS)

Honeywell HONEYWELL INFORMATION SYSTEMS INC.		SPEC. NO. 58014349	SHEET 1/20	REV. A
LOC. PHOENIX, ARIZONA	Dist. Code None	PROJECTION	CODE	
PREPARED BY Y. Gutz DATE 85/1/21	TITLE DAU MAINTENANCE INTERFACE PROCEDURES			
APPROVED BY See sheet 20F DATE				

REVISION RECORD

REV.	AUTHORITY	DATE	SIGNATURE	SHEETS AFFECTED
A	Level 3 Issued	JAN 31 1985	Conine	Sheets 1 thru 20F

CE 350P (12-78)

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

CE 350P-1 (12-78)

1.0 GENERAL DESCRIPTION

This document describes the maintenance interface of Device Adapter Unit WDAU66LA/B. The maintenance interface is incorporated into the EPROMS of the WDAMP board and can function in a stand-alone environment, i.e., even if firmware is not loaded. Figure 1.0-1 shows where and how the DAU maintenance port is connected to a terminal via a test interface board.

NOTE: The maintenance interface, including the terminal, cable, and the free-edge test interface board, are not required for normal operation of the DAU.

CAUTION

SOME OPTIONS OF THE MAINTENANCE INTERFACE CAN HAVE ADVERSE EFFECTS ON NORMAL OPERATION OF THE DAU. THE PERSON USING THESE OPTIONS MUST BE FAMILIAR WITH THE HARDWARE AND THE FIRMWARE.

The IC chip used for the maintenance interface is an INTEL 8251A programmable communications interface (USART). The USART chip provides visibility into the DAU via a terminal for testing and troubleshooting. The transmitters and receivers of the USART are compatible with the RS-423 interface standard (RS-232C serial) and their inputs and outputs are connected to the left free-edge of the WDAMP board. A test interface board is required for the physical interface to the terminal (see Section 4.0).

1.1 REFERENCE DOCUMENTATION

- TDM-NIO-037 DAU Maintenance Interface
- 58081562 DAU Test Interface PWA
- 58059036 System Tools List
- 58010008-100 DAU Theory of Operation

1.2 DOCUMENTATION REQUIREMENTS

- 58086200 Firmware Listing (Current)

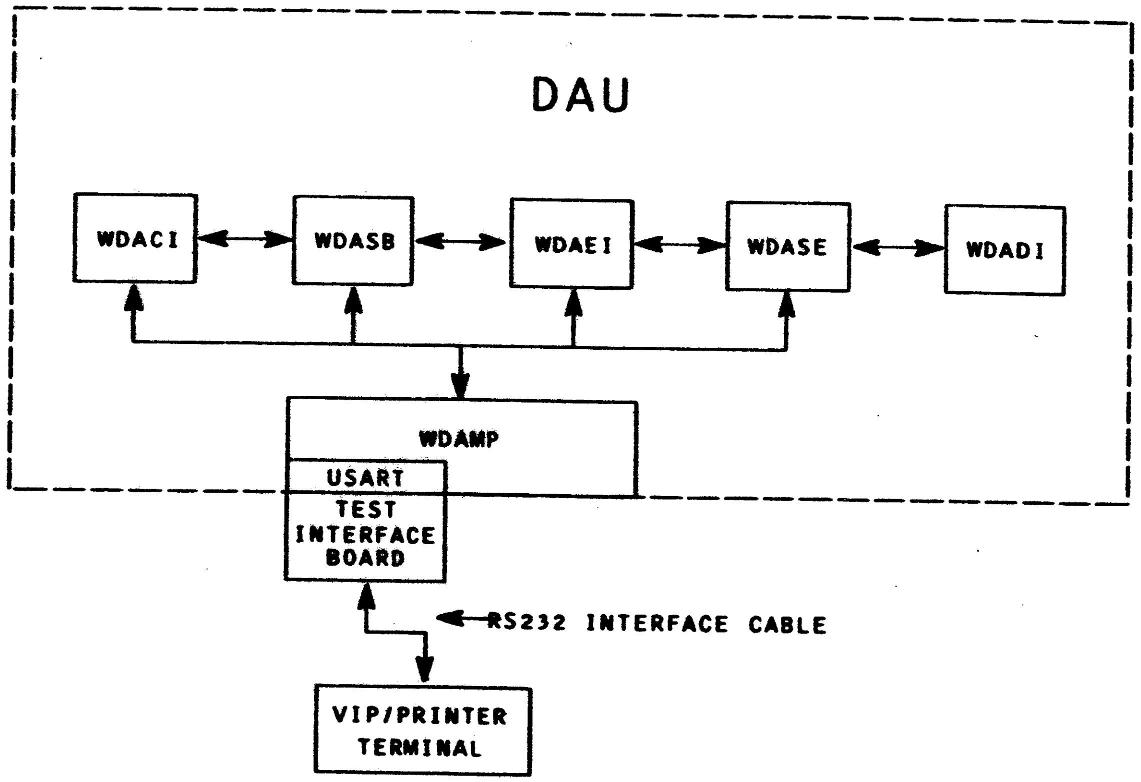


FIGURE 1.0-1. DAU MAINTENANCE INTERFACE

2.0 TERMINAL REQUIREMENTS

The terminal to be connected to the maintenance interface requires the following:

- o Interface - RS-232C Serial TTY (async)
- o Display - Echo or Local Copy
- o Baud Rate - 300/1200
- o Stop Bits - One
- o Parity - Even or Mark (none)
- o Duplex Mode - Half

The following terminal types meet the requirements and can be used as the user interface to the DAU:

- o Honeywell - VIP7205
- o Honeywell - ROSY 24 (TWU1003)
- o Honeywell - ROSY 26 (TWU1005)
- o Execuport - 4080 (with option C)

3.0 CABLE REQUIREMENTS

The following cables can be used for connecting the terminal to the test interface board:

- o 59B400394-xxx
- o 04910129-001
- o 04910129-002
- o 04910129-003

4.0 TEST INTERFACE BOARD DESCRIPTION AND CONNECTION

The test interface board (PWA 58081562-001) is a special tool required to access the maintenance capabilities of the DAU (ref: System Tools List 58059036). The board contains the following (see Figure 4.0-1):

- o A toggle switch SW1 controls power on/off
- o A toggle switch SW2 controls the interface
- o A rocker switch SW3 controls the baud rate and parity
- o A free-edge connector to the WDAMP board
- o An RS232 jack J1 cable connector to the terminal

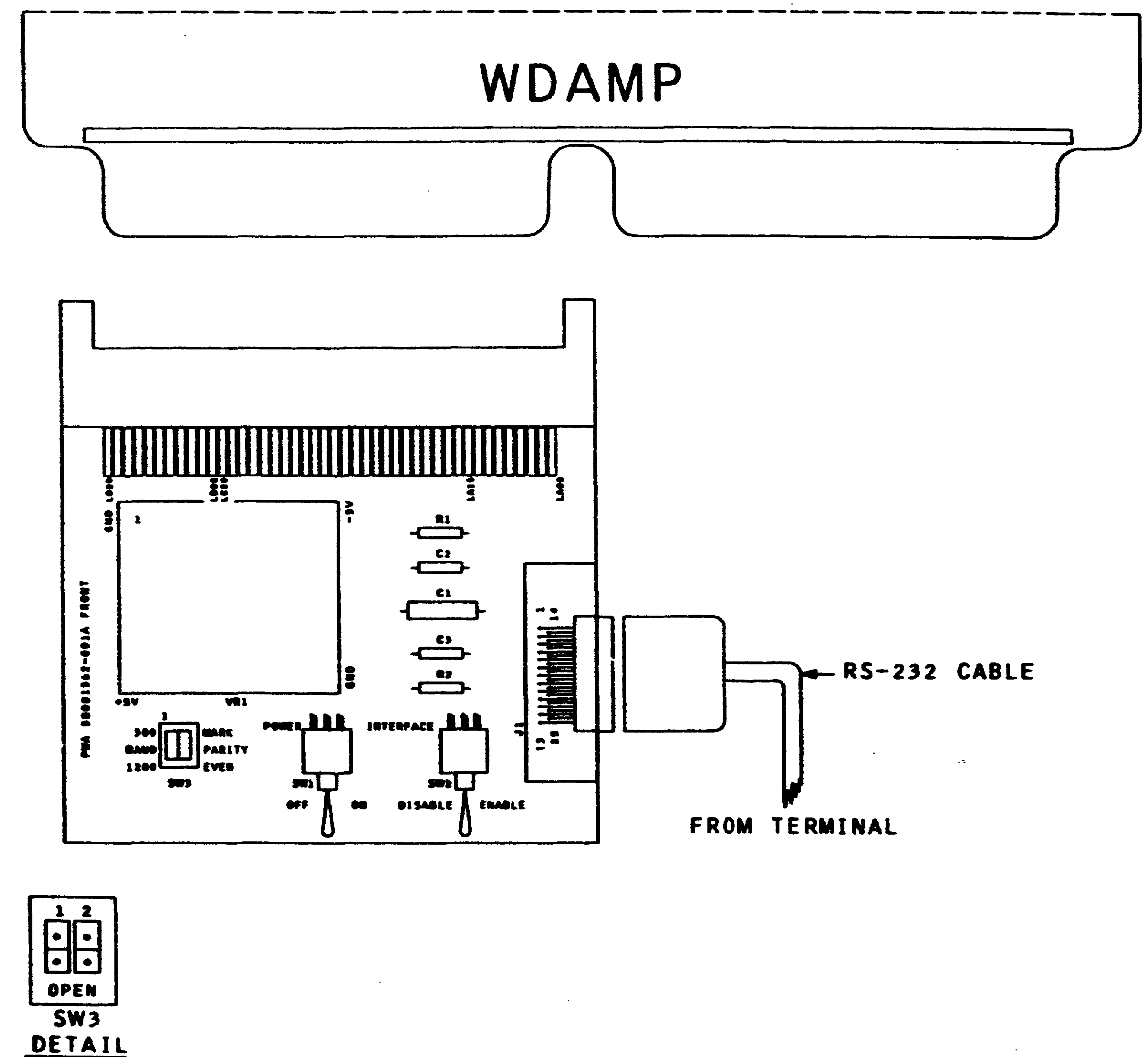


FIGURE 4.0-1. TEST INTERFACE BOARD

The procedure for connecting and configuring the maintenance interface is as follows:

CAUTION

WHEN THE TEST INTERFACE BOARD IS CONNECTED OR DISCONNECTED FROM THE WDAMP BOARD THE TEST INTERFACE BOARD POWER SWITCH MUST BE OFF AND ITS INTERFACE SWITCH MUST BE IN DISABLE.

1. At terminal:

   a. Set baud, parity, and echo (as required).
   b. Connect cable from test interface board to terminal.
   c. Turn terminal power on.

2. At test interface board (disconnected from DAU):

   a. Set baud and parity same as terminal.
   b. Ensure POWER switch is OFF.
   c. Ensure INTERFACE switch is set to DISABLE.
   d. Connect test interface board to left free-edge of WDAMP board.
   e. Set POWER switch to ON.
   f. Set INTERFACE switch to ENABLE.

3. At terminal perform options from menu as required (see Section 5.0).

5.0 DAU MAINTENANCE INTERFACE MENU SUMMARY

The following menu can be obtained at any time by entering an "M" at the terminal.

BREAK aaaa	- Prints register contents at aaaa
CALC nnnn (+)(-) nnnn	- Adds or subtracts hex numbers

(Menu Summary continued on next page)

5.0 DAU MAINTENANCE INTERFACE MENU SUMMARY (CONT.)

DEV	- Prints devices configured
DEV nn	- Prints device table
DEV nn D	- Prints device status
DEV nn S	- Prints device statistics
DLI p c d	- Issues DLI commands to device
G	- Reset STEP/STOP - cont. execution
G aaaa	- Reset STEP/STOP - execute to aaaa
PEEKB aaaa [nn]	- Prints 8 or [nn] bytes from aaaa
PEEKW aaaa [nn]	- Prints 8 or [nn] words from aaaa
POKEB aaaa xx [xx]	- Writes byte(s) xx into aaaa
POKEW aaaa xxxx [xxxx]	- Writes word(s) xxxx into aaaa
S	- Step - Execute next instruction
S aaaa	- Step - From address aaaa
STOP aaaa	- Stop - execution at aaaa
STOPE	- Stop - on hard error
TRACE	- Print firmware trace information
TRACE ON	- Turns TRACE option on
TRACE OFF	- Turns TRACE option off
TRACE aaaa	- Turns TRACE off at aaaa

The following list of functions can be obtained at any time by entering an "F" at the terminal.

@	- Delete last character entered
#	- Delete all input
Ctl X	- Delete all input
Ctl C	- Stops output,reset STEP/STOP & BREAK
CTL E	- Changes USART echo (turn echo on or off)
Ctl I	- Initialize DAU, rebuild device tables
Ctl T	- Execute SELFTEST - destroys firmware
Ctl Z	- Reset device statistics

6.0 MENU DESCRIPTION

6.1 OPTIONS

BREAK aaaa

This option prints out the microprocessor register content when the instruction immediately prior to address (aaaa) is executed. This output repeats indefinitely, until reset by "Ctl C", or the USART interface is disabled.

EXAMPLE:

```
BREAK 6685

??
AX=0080 BX=E060 CX=0000 DX=6685 SI=8009 DI=0000 BP=3000 SP=05F2
IP=6685 CS=0000 FG=F207

??
AX=0080 BX=0F00 CX=0000 DX=4004 SI=8009 DI=0000 BP=3000 SP=05F2
IP=6685 CS=0000 FG=F213
```

CALC nnnn (+)(-) nnnn

This option adds or subtracts two numbers and gives the result in hex form. When patching firmware, this option can be used to calculate the displacement value for branch/jump/call instructions.

EXAMPLE:

```
?? CALC 3500+500
3A00

?? CALC 3500-500
3000
```


6.1 OPTIONS (CONT.)

DEV

This option prints out a list of all devices that are presently configured. The output gives the decimal and hex numbers, device type, current summary status, DAU port number (where device is connected), and the starting memory address of the device table.

EXAMPLE:

```
?? DEV

-------> DEVICES_CONFIGURED <-------
DEC-HEX--TYPE--STAT--PORT--TABLE_ADR
 01  01   451   30     2      2200
 02  02   451   30     0      2000
 13  0D   500   00     6      2600
 14  0E   500   00     6      2680
 15  0F   501   00     4      2400
 16  10   501   00     4      2480
```

DEV nn

This option prints out the contents of the device table in byte form.

EXAMPLE:

```
?? DEV 13

2600 66 39 00 30 00 30 00 00 00 02 F8 02 2D 03 2E 03
2610 26 0D 0D CA 26 28 00 02 00 00 00 00 60 00 F8 0A
2620 38 02 00 00 3E 11 01 00 00 00 4A C0 68 01 00 00
2630 00 00 00 00 00 00 21 00 00 00 00 00 00 00 00 00
2640 00 00 00 00 00 00 21 00 00 00 00 00 00 00 00 00
2650 00 00 00 00 00 00 21 00 00 00 00 00 00 00 00 00
2660 50 00 47 40 31 75 BC 0C 00 00 00 00 00 00 4F 01
2670 00 00 00 00 00 00 3B 01 14 00 00 00 0F 00 00 00
```

6.1 OPTIONS (CONT.)

DEV nn D

This option prints out the current information from the device, which includes the number, type, current servo position, and the summary and detail status bytes.

EXAMPLE:

?? DEV 13 D

```
DNR-0D   DTR-CA   CYU-00   CYL-00   HDL-00
SS--40   DS1-00   DS2-00   DS3-00   DS4-00
DS5-00   DS6-00   DS7-00   DS8-00   SS--40
```

DEV nn S

This option prints out the current device statistics in hex form.

EXAMPLE:

?? DEV 13 S

```
MOVEMENT SEEKS- - - - - - - - - - 0050
SECTORS WRITTEN - - - - - - - - - 4047
SECTORS READ- - - - - - - - - - - 7531
DATA XFER COMMANDS- - - - - - - - 0CBC
SEEK INCOMPLETES- - - - - - - - - 0000
HEADER VERIFICATION ERRORS- - - - 0000
XFER TIMING ERRORS- - - - - - - - 0000
EDAC ERRORS - - - - - - - - - - - 014F
COUNT FIELD ERRORS- - - - - - - - 0000
INTERFACE PARITY ERRORS - - - - - 0000
ALTERNATE TKS PROCESSED - - - - - 0000
EDAC CORRECTABLE ERRORS - - - - - 013B
EDAC UNCORRECTABLE ERRORS - - - - 0014
LATENCIES LOST- - - - - - - - - - 0000
RE-READ ATTEMPTS- - - - - - - - - 000F
SEARCH ALERTS - - - - - - - - - - 0000
```


6.1 OPTIONS (CONT.)

DLI p c d

This option issues DLI commands (c) to the device connected to DAU port (p) and also sends any output data (d). If DLI(cr) is input, a list of applicable commands (c) are output. The (p) is the DAU port number in hex form. If DLI p(cr) is input, the device is initialized. The (d) is optional and if not supplied, all zeros are sent on output type commands.

EXAMPLE:

?? DLI

```
20-HIU   21-HIL   22-CIU   23-CIL   24-API   26-DNR   27-DTR   28-SSR
29-DS1   2A-DS2   2B-DS3   2C-DS4   2D-DS5   2E-DS6   2F-DS7   3F-DS8

42-SFU   43-SFL   44-SRU   45-SRL   46-COU   47-COL   48-HOU   49-HOL

50-SZE   51-RLS   52-RCB   53-SSS   54-SLS   55-RDM   56-ENM   57-DSM
58-SPO   59-SPI   5A-ARC   5B-RRC   5C-HDS   5D-HDD   5E-SDM   5F-SDE
```

?? DLI 6

?? DLI 6 28

DEV INPUT = 00

?? DLI 6 50

?? DLI 6 28

DEV INPUT = 40

?? DLI 6 51

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6.1 OPTIONS (CONT.)

G
G aaaa

These options reset the STEP or STOP condition (if set) and normal instruction execution is resumed. If (aaaa) is supplied, a new STOP is established at that address.

EXAMPLE: See STOP aaaa Option.

PEEKB aaaa [nn]

This option prints out the contents of memory or the hardware registers in byte form starting at address aaaa. Eight contiguous locations are output, unless over-ridden by "nn" which has a maximum value of 99 decimal.

EXAMPLE:

```
?? PEEK 3500

3500  A0 4D 02 A2 0C B1 8D 2E

?? PEEK 3500 16

3500  A0 4D 02 A2 0C B1 8D 2E 00 30 2B FF A1 AA 00 A2

?? PEEK 3500 99

3500  A0 4D 02 A2 0C B1 8D 2E 00 30 2B FF A1 AA 00 A2
3510  02 B1 90 88 26 02 B1 A0 0E B1 32 06 5E 02 24 F0
3520  75 64 A1 50 02 22 26 06 B0 75 0B 22 06 26 B0 74
3530  08 BF 20 00 86 E0 E9 B9 01 02 06 F0 02 74 03 E9
3540  E6 02 03 06 08 30 74 31 8D 2E 00 1F 81 C5 00 01
3550  D1 E0 73 F8 A3 08 30 8B 46 08 85 06 8E B0 74 11
3560  A3 8E B0
```


6.1 OPTIONS (CONT.)

PEEKW aaaa [nn]

This option is the same as "PEEKB aaaa [nn]" except that the output is in word form.

EXAMPLE:

```
??  PEEKW 3500

3500  4DA0 A202 B10C 2E8D 3000 FF2B AAA1 A200

?? PEEKW 3500 16

3500  4DA0 A202 B10C 2E8D 3000 FF2B AAA1 A200
3510  B102 8890 0226 A0B1 B10E 0632 025E F024
```

POKEB aaaa xx [xx]

This option writes the supplied byte(s) "xx" into consecutive locations starting at address aaaa in memory or the hardware registers.

EXAMPLE:

```
?? POKE 3FF0 12 13 14

?? PEEK 3FF0

3FF0   12 13 14 00 00 00 00 00
```

POKEW aaaa xxxx [xxxx]

This option is the same as "POKEB aaaa xx [xx]" except that the write is in word form.

EXAMPLE:

```
?? POKEW 3FF0 1234

?? PEEKW 3FF0

3FF0   1234 0014 0000 0000 0000 0000 0000 0000
```

6.1 OPTIONS (CONT.)

S

This option allows the next instruction in sequence to be executed if the STEP or STOP option is set.

EXAMPLE: See STOP aaaa Option.

S aaaa

This option conditions the DAU to begin executing instructions at address "aaaa". See Note below for options available during the STEP option.

EXAMPLE:

```
?? S 6685

AX=0000 BX=0000 CX=0000 DX=0000 SI=8009 DI=0000 BP=3000 SP=05F8
IP=6685 CS=0000 FG=F246

Above Reg Content Okay? - (Y or N) = N
Enter Reg Info - (cr)only = no chg - E = end
AX=1234
BX=2345
CX=FFFF
DX=4511
SI=0
DI=0020
BP=
SP=
IP=
CS=
FG=

AX=1234 BX=2345 CX=FFFF DX=4511 SI=0000 DI=0020 BP=3000 SP=05F8
IP=6685 CS=0000 FG=F246

Above Reg Content Okay? - (Y or N) = Y
AX=FFFE BX=2345 CX=FFFF DX=4511 SI=0000 DI=0020 BP=3000 SP=05F8
IP=6688 CS=0000 FG=F346

?? S
AX=FFFE BX=2345 CX=FFFF DX=4511 SI=0000 DI=0020 BP=3000 SP=05F6
IP=6D69 CS=0000 FG=F346

?? G
```


6.1 OPTIONS (CONT.)

STOP aaaa

This option conditions the DAU to halt normal instruction execution immediately prior to "aaaa". When the STOP condition is reached, the microprocessor register content is printed. See Note below for options available during the STOP option.

EXAMPLE: Follows Note below.

STOPE

This option conditions the DAU to halt normal instruction execution upon the detection of any hard error. When the STOPE condition is reached, the microprocessor register content is printed. See Note below for options available during the STOPE option.

EXAMPLE: See STOP aaaa Option.

NOTES:
1. The DAU is initialized if the USART interface is disabled.
2. Most options and control functions are available during the "S aaaa", "STOP aaaa", and "STOPE" conditions. If any is not available, a message "INVALID PARAMETERS" is output. Some of the options are listed below:

```
S      - Execute next instruction in sequence
G      - Reset option - resume normal operation
S aaaa - Execute instructions from address aaaa
G aaaa - Execute instructions normally until aaaa

Ctl C  -\
Ctl I  - > Reset options - initialize DAU
Ctl Z  -/
```

6.1 OPTIONS (CONT.)

NOTE 2 (CONT.)

EXAMPLE:

```
?? STOP 6685

AX=0080 BX=E060 CX=0000 DX=6685 SI=8009 DI=0000 BP=3000 SP=05F2
IP=6685 CS=0000 FG=F217

?? S

AX=FFFE BX=E060 CX=0000 DX=6685 SI=8009 DI=0000 BP=3000 SP=05F2
IP=6688 CS=0000 FG=F317

?? S

AX=FFFE BX=E060 CX=0000 DX=6685 SI=8009 DI=0000 BP=3000 SP=05F0
IP=6D69 CS=0000 FG=F317

?? S

AX=FFFE BX=E060 CX=0000 DX=6685 SI=F010 DI=0000 BP=3000 SP=05F0
IP=6D6D CS=0000 FG=F317

?? G 6685

AX=0080 BX=0F00 CX=0000 DX=4004 SI=8009 DI=0000 BP=3000 SP=05F2
IP=6685 CS=0000 FG=F217

?? S

AX=FFFE BX=0F00 CX=0000 DX=4004 SI=8009 DI=0000 BP=3000 SP=05F2
IP=6688 CS=0000 FG=F317

?? G
```


6.1 OPTIONS (CONT.)

<u>TRACE</u>

This option causes the firmware TRACE information to be printed. The listing is from the last trace entered backward, i.e., a back-track of DAU activity. The firmware listing can be referred to for a description of the TRACE information.

EXAMPLE:

```
?? TRACE

7010 F700 0000 F600 F100 0711 760D F000 F700
7000 0000
7FFC F600 0040 F400 2511 F300 4AC0 F200 F100
7FEC 0791 360D F000 F700 0000 F600 003F F400
7FDC 2511 F300 4ACD F200 F100 0791 360D F000
7FCC F700 0000 F600 003E F400 2511 F300 4ACD
7FBC F200 F100 0791 360D F000 F700 0000 F600
7FAC 003D F400 2511 F300 4ACD F200 F100 0791
7F9C 360D F000 F700 0000 F600 003C F400 2511
7F8C F300 4AC0 F200 F100 0791 360D F000 F700
7F7C 0000 F600 0038 F400 2511 F300 4AC0 F200
7F6C F100 0791 360D F000 F700 0000 F600 003A
7F5C F400 2511 F300 4AC0 F200 F100 0791 360D
7F4C F000 F700 0000 F600 0039 F400 2511 F300
7F3C 4AC0 F200 F100 0791 360D F000 F700 0000
7F2C F600 0038 F400 2511 F300 4AC0 F200 F100
7F1C 0791 360D F000 F700 0000 F600 0037 F400
7F0C 2511 F300 4AC0 F200 F100 0791 360D F000
7EFC F700 0000 F600 0036 F400 2511 F300 4AC0
7EEC F200 F100 0791 360D F000 F700 0000 F600
7EDC 0035 F400 2511 F300 4AC0 F200 F100 0791
```

<u>TRACE ON</u>
<u>TRACE OFF</u>

These options enable or disable the TRACE option. Firmware normally traces the execution of all commands.

EXAMPLE: N/A

6.1 OPTIONS (CONT.)

TRACE aaaa

This option disables the TRACE option within firmware when address "aaaa" is reached.

EXAMPLE:

?? TRACE 6685

??
TRACE OFF

6.2 FUNCTIONS

●

This function deletes the last character entered. As many "●"s can be used as required to correct typing errors.

#
Ctl X

These functions delete all characters just entered.

Ctl C

This function stops any output in process. It can also be used to reset the BREAK, STEP, and STOP options.

Ctl E

This function enables/disables the character ECHO back to the terminal. The default is character ECHO.

Ctl I

This function initializes the DAU. If any commands are in the queue, they are not executed.

Ctl T

This function, if repeated, performs a forced jump to fixed location FFF0 hex which is the start of Self Test.

Ctl Z

This function sequences through the port tables and resets (zeros) the device statistics area.

DATE: January 1985

TITLE: DAU MAINTENANCE INTERFACE PROCEDURES

APPROVED BY: J. A. Caslake — 85/01/21
J. A. CASLAKE
IOSP Des. & Dev.
Date

APPROVED BY: J D Abel — 1-21-85
J. M. WOODS, Mgr.
IOSP Des. & Dev.
Date

CONCURRED BY : J.E. Rinehart — 1-28-85
J. E. RINEHART
CSD
Date

58081562

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO. 001	TAB NO. 002	PL ALL	DWG. SH. 1
A	LEVEL 1 ISSUE	84	JUL	24	[illegible] 7/19/84	A		A	A
A1	PHA0 X S625	84	DEC	20	G. Miller	A1			
B	PHA0 X S626	85	JAN	09	[illegible]	B	B	B	B
						OBSOLETE			
	58059114				SCHEM. DIA.	A	A		
	58081744-001				PWB ETCH	A1	A1		

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LOC PHOENIX ARIZONA

[illegible] 7/11/84

MADE BY Efren Anaya 6/6/84

APPROVED [illegible] 7-11-84

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TITLE PW ASM DAU TEST INTERFACE BD

SIZE	REVISION STATUS FOR	SHEET	REV
C	58081562	1/1	B

DIST. 30

BRUNING 44-141 40366

CE 300 A-3 (1-79)

PD 85/01/10 *SECTION- 1* C 58081562 1/1 B

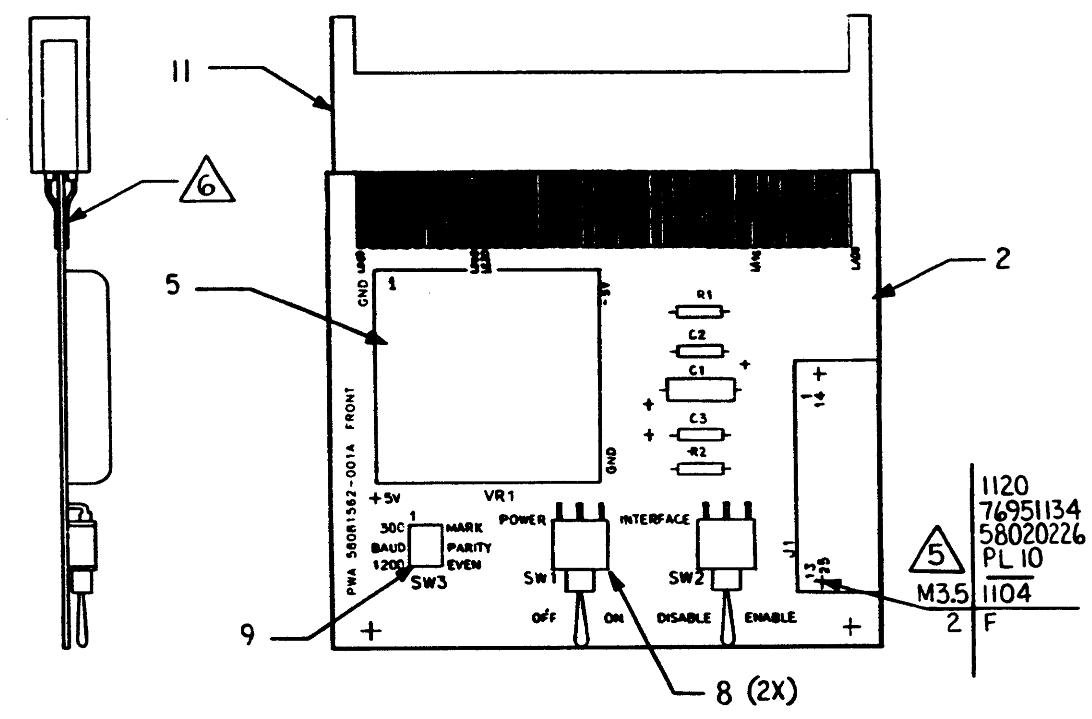
					002	
*	1	C	58059114	D SCHEM DIA DAU T	X	
*	2	C	58081744-001	A PWB ETCH DAU TEST	1	EA
*	3	A	43A114748P16	V CAPACITOR TANT	1	EA
*	4	A	43A114748P9	V CAPACITOR TANT	2	EA
*	5	A	58020393-004	W LP REG PS/CONVERTER	1	EA
*	6	A	70928104-021	V RESISTOR,1/4W	1	EA
*	7	A	70928104-301	V RESISTOR 1/4 W	1	EA
*	8	A	60067007-011	V SWITCH TOGGLE MIN	2	EA
*	9	A	58020295-001	V SW.ROCKER,DIP,SPST	1	EA
*	10	A	58053426-001	W CONNECTOR,PWB	1	EA
*	11	A	43A143895P1	P CONNECTOR 88PIN	1	EA
*	12	A	58014354	D DAU MAINT TOOL	X	

PW ASM

C 58081562 1/1 B

REV	AUTHORITY	DATE YR MO DAY	SIGNATURE

REVISIONS



-001 OBSOLETE

-002

CAP.	PL IT. TAB 001/002	COMP. SPAC.
C1	3	20.3 / .8
C2	4	15.2 / .6
C3	4	15.2 / .6

CONV.	PL IT. TAB 001/002	COMP. SPAC.
VR1	5	STD.

RES.	PL IT. TAB 001/002	COMP. SPAC.
R1	6	15.2 / .6
R2	7	15.2 / .6

SWITCH	PL IT. TAB 001/002	COMP. SPAC.
SW1	8	STD.
SW2	8	STD.
SW3	9	STD.

△6. CONNECTOR CONTACTS TO BE SOLDER TERMINATED WITHIN RELATED PLATED CIRCUIT CONTACT ON BOARD.
△5. HARDWARE BUILD-UP PER M50EB00506-CR.
4. MAXIMUM HEIGHT SOLDER SIDE $\frac{3.17}{.125}$.
3. MAXIMUM HEIGHT COMPONENT SIDE $\frac{12.06}{.475}$.
2. ASSEMBLE PER 43A226454.
1. FOR TABS 001& 002 SEE SCHEMATIC 58059114.

NOTES: UNLESS OTHERWISE SPECIFIED.

FOR DOCUMENT STATUS SEE REVISION STATUS SHEET

REF SPEC NO
M50EB00506-CR
58059114
43A226454

UNLESS OTHERWISE SPECIFIED
DIMENSIONS= MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN M
PROJECTION

MATL

TREAT.

FIN 7/11/84

DR Efren Anaya 5/21/84

APPD 7-11-84

DISTR 30

SCALE 1:1

CODE

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC PHOENIX, ARIZONA U. S. A.

TITLE PW ASM
DAU TEST INTERFACE BD

SIZE	DWG NO	SH	REV
C	58081562	1/1	.B

58081562

CE 300 C (12 71)

58059556

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	ASSEMBLY TAB 001	002	003	004	005	PL ALL
A	LEVEL I ISSUE	81	11	02	[illegible] 10-30-81	A	A	A			A
B	PHA0XS058	82	02	15	C.A. Beattey			B			B
C	PHAØXS072	82	04	05	G. Drenth	C					C
D	PHAØXS095	82	JUN	03	B. Vanasek	D					D
E	PHAØXS120	82	08	18	S. Miller			E			E
F	PHAØNJ004	82	09	01	B. Vanasek	F	F	F			F
G	PHAØXS136	82	11	11	B. Vanasek	G					G
H	PHAØNJ007	82	12	15	S. Miller	H	H	H			H
J	PHAØXS151	83	01	25	G. Drenth		J				J
K	PHAØXS163	83	03	14	T. Inouye		K				K
L	PHAØXS162		ND		G. Drenth	L					L
L1	ADD TABS -004 & -005	83	04	04	S. Miller				L1	L1	L1
M	PHAØXS177	83	JUN	21	G. Drenth		M				M
N	PHAØXS219	83	06	24	G. Drenth		N				N
P	PHAØXS256	83	08	12	G. Drenth	P	P				P
R	PHAØBE090		ND		G. Drenth				R		R

FCF 58059584

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BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

CE 300 A-3 (1-79)

MADE BY S. Jameson 21 OCT 81

APPROVED F. J. Flores 27 SEPT 81

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TITLE MODULE & BKPNL ASM.

SIZE	REVISION STATUS FOR	SHEET	REV
X	58059556	1/2	S

DIST. C125-5

58059556

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	ASSEMBLY TAB 001	002	003	004	005	PL ALL
S	PHAØBE089	83	09	14	G Drenth	P	P	H	R	S	S
T	PHAØXS275	83	09	15	G Drenth		T				T
U	PHAØNJ016	83	10	05	G Drenth			U			U
V	PHAØXS322	83	10	19	T. [illegible]	V	V				V
V1	ENXS144		ND		G Drenth				V1		
W	PHAØXS341	83	11	11	G Drenth		W				W
W1	ENXS162		ND		G Drenth					W1	
W2	LEVEL 2 ENXS149		ND		G Drenth			W2			
X	PHAØXS296	84	03	06	G Drenth			X			X
Y	PHAØTG233		ND		G Drenth					Y	Y
Z	PHAØTG232	84	08	13	G Drenth				Z		Z
AA	PHAØNJ032	84	10	10	G Drenth			AA			AA
AB	PHAØXS611	84	11	19	G Drenth				AB		AB

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY S. JAMESON 21OCT81

APPROVED F. J. FLOWERS 27SEP81

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE MODULE + BKPNL ASM.

SIZE	REVISION STATUS FOR	SHEET	REV
X	58059556	2F	AB

DIST. -5

BRUNING 44-141 40366

CE 300 A-3 (1-79)

				001	002	003	004	005	
1	X	58071940-103	A BKPNL WRD WDAAO			1			EA
2	X	58066470-106	A BKPNL WIRED IPCAO	1					EA
2	X	58066470-406	A BKPNL WIRED IPCAO	NOINT					EA
3	X	58078410-307	A BKPNL WRD WXCA1		1				EA
3	X	58078410-206	A BKPNL WRD WXCA1		NOINT				EA
9	D	58060822	D MOD COMM ASM INSTR	X	X	X	X	X	
10	B	43B137240P3	W NUT CLIP	2	2	2	2	2	EA
11	C	43C243202G4	A CARD CAGE	1	1	1	1	1	EA
12	C	58059375-001	A THERMOSTAT CABLE ASM		1				EA
13	A	58056756-001	P ROD, SLIDE		3				EA
14	A	58053358-001	W NUT, PUSH-ON		6				EA
15	X	58078220-103	A BKPNL WRD TC3A0				1		EA
15	X	58078220-203	A BKPNL WRD TC3A0				INTCH		EA
15	X	58078220-002	A BKPL WRD TC3A0				NOINT		EA
16	X	58078230-103	A BKPNL WRD TC3A1					1	EA
16	X	58078230-203	A BKPNL WRD TC3A1					INTCH	EA

MODULE & BKPNL ASM

PD 84/11/19 X 58059556 2/F AB

			001	002	003	004	005	
16 X	58078230-002	A BKPL WRD TC3A1					NOINT	EA

MODULE & BKPNL ASM

X 58059556 2/F AB

58034134

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB 001	TAB 002	TAB 003	TAB 004	PL ALL	DWG SH 1
A	LEVEL 1 ISSUE	79	10	09	T Challis 10/2/79	A	A			A	A
B	PHAØPV083	79	12	13	Noel L. Diaz	B	B			B	B
C	PHAØPS308	80	DEC	09	Jim Richardson	C	C	C	C	C	C
D	PHAOPV313	82	JAN	15	Eileen Anaya	D	D	D	D	D	D
D1	Level 2 ENBE014		ND		G Drenth	D1		D1			
D2	Level 3 ENPV128		ND		G Drenth		D2		D2		
E	PHAØPV563	82	DEC	10	B Vanasek	E	E	E	E	E	E
F	PHAØGD694	84	OCT	01	G Drenth	F	F	F	F		F

FCF:

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY [signature] 79 JUN 5

APPROVED R. T. Abraham 79/09/20

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CONNECTOR GUIDE

SIZE	REVISION STATUS FOR	SHEET	REV
C	58034134	1/1	F

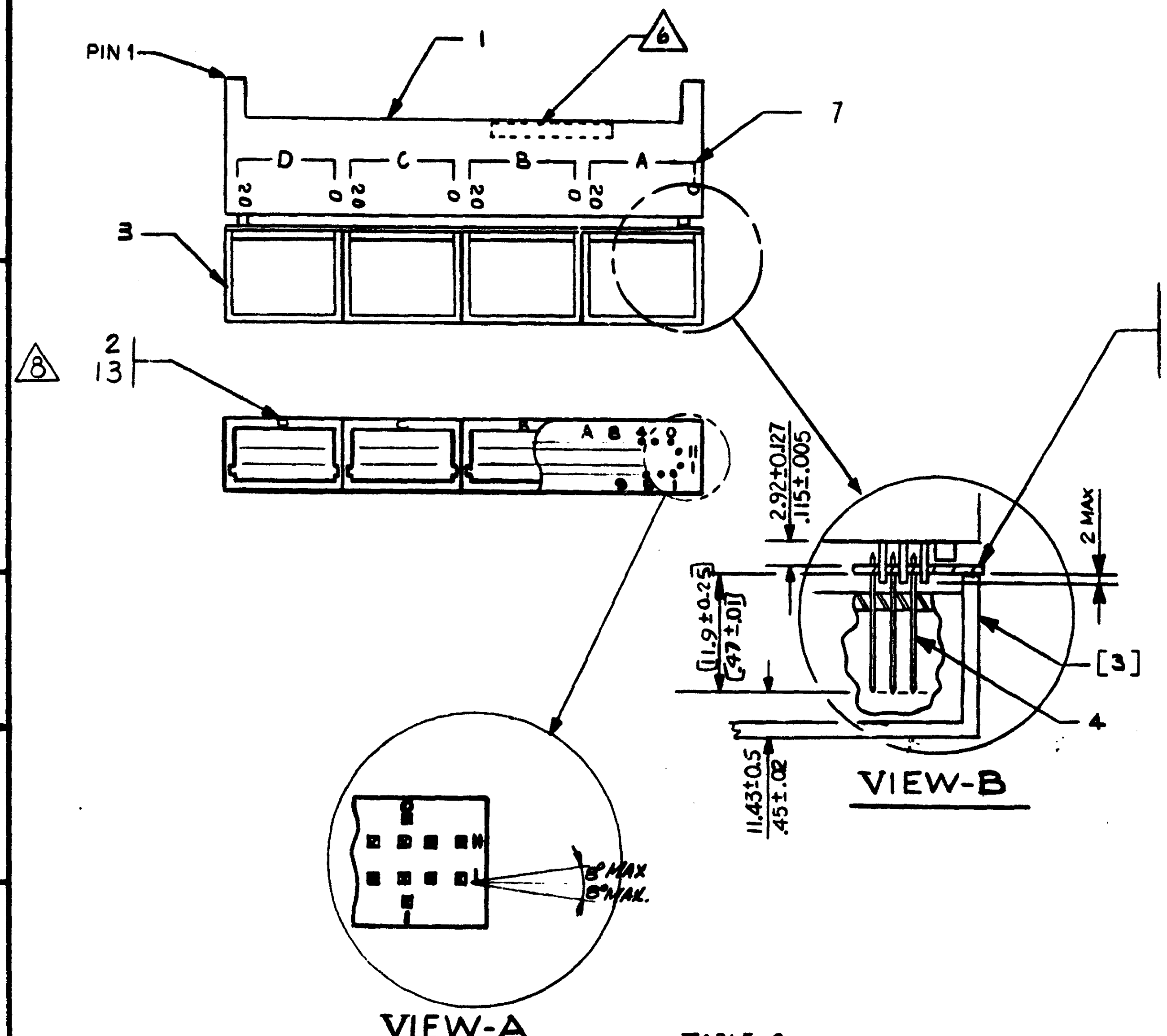
DIST. - 3

BRUNING 44-141 40366

CE 300 A-3 (1-79)

					001	002	003	004	
	1	A	58052731-001	P CONNECTOR 88 PIN	1	1	1	1	EA
*	2	B	58059668-003	V LABEL	1	1			EA
*	2	B	58059668-001	V LABEL	INTCH	INTCH			EA
	3	C	58034050-001	V CONNECTOR GUIDE	4	4	2	2	EA
	4	A	43A216107P13	V PIN,WIRE WRAP	80	80	40	40	EA
	5	X	58054156-002	A PWB BOND & ETCH	1				EA
	6	C	58051465	D SCH-FE/CABLE ADD BD		X			
	7	X	58051464-001	A PWB BOND & DRILL		1			EA
	8	C	58054157	D SCH FE/CABLE ADP BD	X				
	9	X	58052517-001	A PWB BOND & DRILL			1		EA
	10	D	58052546	D SCHEMATIC			X		
	11	X	58052518-001	A PWB BOND & DRILL				1	EA
	12	D	58052545	D SCHEMATIC				X	
*	13	B	58059668-004	V LABEL			1	1	EA
*	13	B	58059668-002	V LABEL			INTCH	INTCH	EA

CONNECTOR GUIDE



REVISIONS			
REV	AUTHORITY	DATE YR MO DAY	SIGNATURE

△ 8. ATTACH MARKER STRIP ORIENTED AS SHOWN.

△ 7. CONNECTOR PIN NUMBERING FOR REFERENCE ONLY, DO NOT MARK ON ASM.

△ 6. MFG TO MARK ASM NO., TAB NO. AND REVISION. PER: M50EB00655.

△ 5. CONNECTOR GUIDE ITEM 3 SHALL BE INSTALLED IN THE LOCATIONS INDICATED IN TABLE C.

4. ASSEMBLE PER 43A226454.

3. BEFORE THE INSTALLATION OF GUIDE ITEM 3:

A. THE TIP OF PIN ITEM 4 SHALL BE WITHIN A RADIUS OF .13MM OF ITS TRUE HOLE POSITION.

B. THE MAXIMUM ITEM 4 PIN ANGULAR ORIENTATION WITH RESPECT TO ITS PIN ROW SHALL BE PER VIEW-A.

2. INSTALL PWB ITEM 5 ORIENTED AS SHOWN.

1. ITEMS SHOULD BE ASSEMBLED IN THE FOLLOWING ORDER:

A. STAKE PINS ITEM 4 INTO P.W.B. ITEM 5 AND SOLDER.

B. PLACE THE PINNED PWB OVER THE PINS OF ITEM 1 & SOLDER PARTS TOGETHER.

C. PRESS ITEM 3 OVER THE SOLDERED PINS SO ITEM 3 BUTTS AGAINST THE SURFACE OF PWB ITEM 5.

NOTES:

58034134

TABLE C

DWG. TAB	P.L. ITEM	LOGIC INTERFACE NAME	ITEM 3 LOCATION △5
-001	5	MAGNETIC TAPE HANDLER	A,B,C AND D
-002	7	DISC FILE, URE & GENERAL USE	A,B,C AND D
-003	9	MPC TAPE/DISC (PSIA)	B AND C
-004	11	IOM (PSIA)	B AND C

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

43A226454
M50EB00655
58008590
REF SPEC NO

UNLESS OTHERWISE SPECIFIED DIMENSIONS= MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN M
PROJECTION

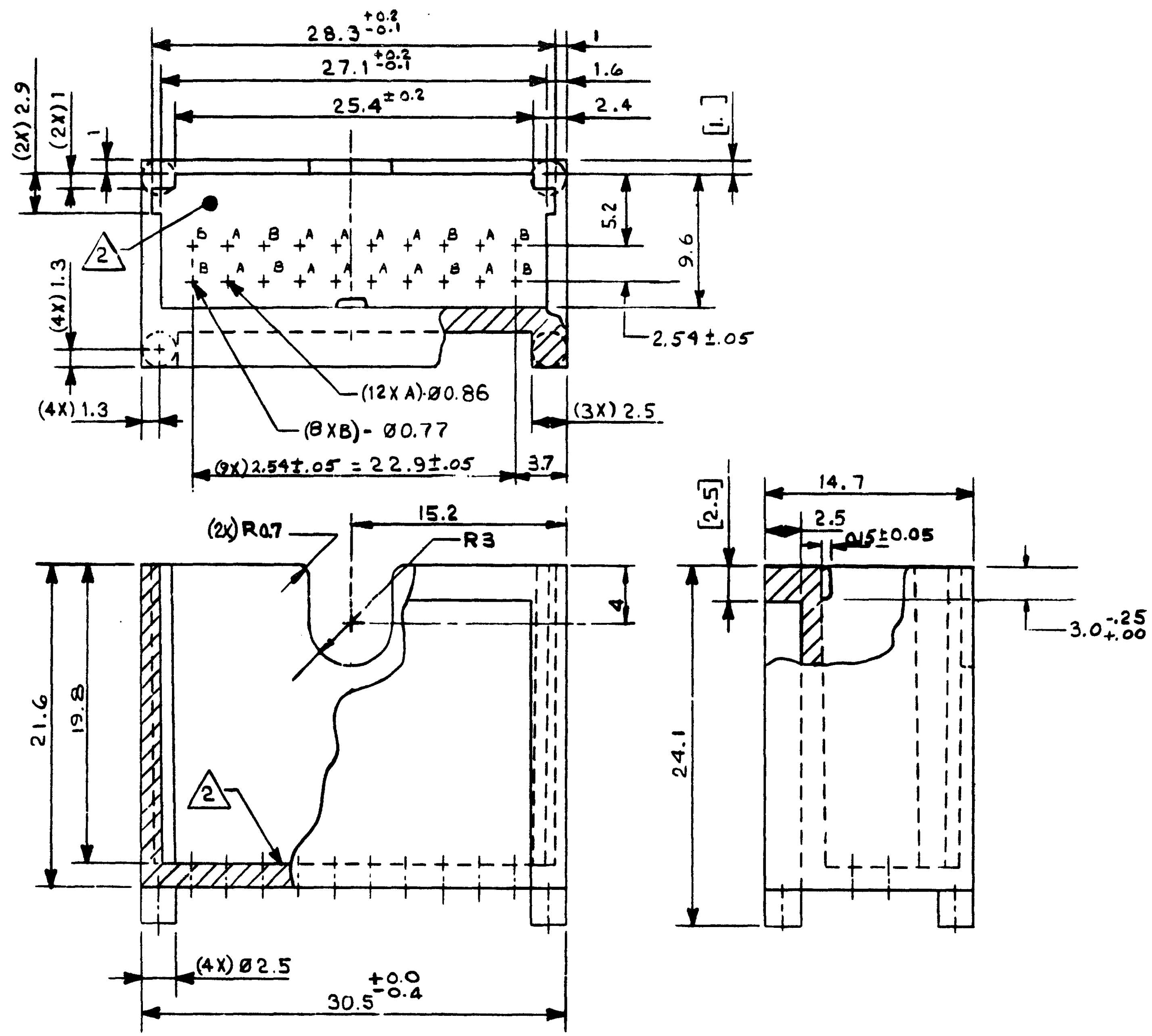
SCALE 1/1 | CODE

MATL
DES. Tod Guilford
CHKR JK Hall 79
FIN.
DR O. Mullinger 79 JUN 5
APPD R. G. Abraham 79/06/20
DISTR -3

T Chandler 10/4/79

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC PHOENIX, ARIZONA U.S.A.
TITLE CONNECTOR GUIDE

SIZE C | DWG NO 58034134 | SH 1/1 | REV F



REV	AUTHORITY	YR	MO	DAY	SIGNATURE
A	LEVEL 1 ISSUE	79	SEP	27	[illegible]
B	PHAØAC 353	80	FEB	18	V. Davis
B1	LEVEL 3 ISSUE	80	03	17	V. Davis
C	PHAØPV!99	80	05	09	[illegible]

NOTES:

1. TOLERANCE ± 0.25 UNLESS OTHERWISE SPECIFIED.
2. 5° MOLD TAPER PERMITTED ON INSIDE DIMENSIONS FROM BASE SURFACE AS SHOWN.
3. 0.3R. PERMITTED ON INSIDE CORNERS.
4. FINISHED PART MUST MEET FLAMMABILITY REQUIREMENTS OF 94V-2 OR BETTER PER UL478.

PURCHASE FROM AN APPROVED VENDOR PER 43A997260.

(001)

58022709
REF SPEC NO

UNLESS OTHERWISE SPECIFIED DIMENSIONS= MILLIMETERS
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN M
PROJECTION

MATL 30% G.F. POLYCARBONATE 58022709
DES [illegible] 79 MAY 22
CHKD. [illegible] 79 SEP 10
FIN.
SCALE 4/1
CODE MP 9390
DR [illegible] 79 MAY 4
APPD [illegible] 80/3/11
DISTR GU-50

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC PHOENIX, ARIZONA U.S.A.
TITLE CONNECTOR GUIDE
FLF: 58052696

SIZE	DWG NO	SH	REV
C	58034050	1/1	C

58034050

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58034110

REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE	TAB 001	014	018	022	009	012			PL AL					ASM. SH. 1	2	3	4	5	6	
A	LEVEL 1 ISSUE	79	10	09	S.E. Strode 79-09-28	A								A					A						
B	PHAØFC008	79	Nov	15	C. Ripley	B													B						
C	PHAØPV083	79	12	13	P.M. D'Agostino	C								C											
D	PHAØPV140	80	Mar	24	A. Topley	D								D					D						
E	PHAØPS293	80	08	06	A. Eylund	E								E					E						
F	PHAØPV165	80	Dec	10	Connie Dale	F								F											
G	PHAØXW114	82	Apr	02	S.J. Steele	G	G	G	G					G					G						
H	PHAØGD451	82	11	08	S. Miller	H	H	H	H					H					H						
J	PHAØGD489	83	07	27	S. Miller	J	J	J	J					J											
K	PHAØGD535	83	12	23	S. Miller	K	K	K	K	K	K			K					K	K	K	K	K	K	

F.C.F.

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS

LOC PHOENIX, ARIZONA

MADE BY Ted Griffard 79 MAY 29

APPROVED R.G. Abraham 79/09/20

TITLE I/O CABLE ASSEMBLY

REVISION STATUS FOR EACH PAGE, SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

SIZE	REVISION STATUS FOR	SHEET	REV
A	58034110	1/1	K

CE 300 A-3 (12-71) BRUNING 44-141

DIST. C106- 73

					001	009	012	014	018	022	
*	1 C	58034066-001	V PADDLE BD COVER		1	1	1	1	1	1	EA
*	2 A	58000038-008	V CONNECTOR, PWB		1	1	1	1	1	1	EA
*	3 C	58047470-003	A PWB ETCH & DRILL		1	1	1	1	1	1	EA
*	6 B	43B133945P21	V CONNECTOR,PLUG		1	1	1	1	1	1	EA
*	7 A	58014257-010	M TAPE POLY .007X0035		2	2	2	2	2	2	
*	7 A	43A981308P1	V TAPE		INTCH	INTCH	INTCH	INTCH	INTCH	INTCH	IN
*	8 A	58020397-001	V CABL MULTICOND COAX		600	354	472	551	709	866	IN
*	9 B	58003743-001	P CLOSED ENT. GUIDE		1	1	1	1	1	1	EA
*	10 B	43B240058P2	P CONNECTOR HOUSING		1	1	1	1	1	1	EA
*	11 C	43C142270P4	V CLAMP CABLE		2	2	2	2	2	2	EA
*	12 B	8788222P120	V SLEEVING		10	10	10	10	10	10	IN
*	13 A	58058844-003	A CONTACT ACCUM KIT		14	14	14	14	14	14	EA
*	13 A	58020371-001	V CONTACT,SUBMIN.COAX		INTCH	INTCH	INTCH	INTCH	INTCH	INTCH	EA
*	17 A	43A115944P42	P TAPE POLYESTER		2	2	2	2	2	2	IN
*	18 A	76951715-045	V LOCKWASHER		1	1	1	1	1	1	EA
*	19 A	76951715-059	V LOCKWASHER		2	2	2	2	2	2	EA

I/O CABLE ASSEMBLY

					001	009	012	014	018	022	
*	20	A	58033849	V #608 HYSOL	AR	AR	AR	AR	AR	AR	OZ
*	21	B	43B111126P15	V WIRE BARE SOLID	3	3	3	3	3	3	IN
*	22	A	58053707	V IPL EXTRNL CBL ASM		X	X	X	X	X	EA

58034110

REF SPEC NO
58053700
58053707

REVISION					
REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE

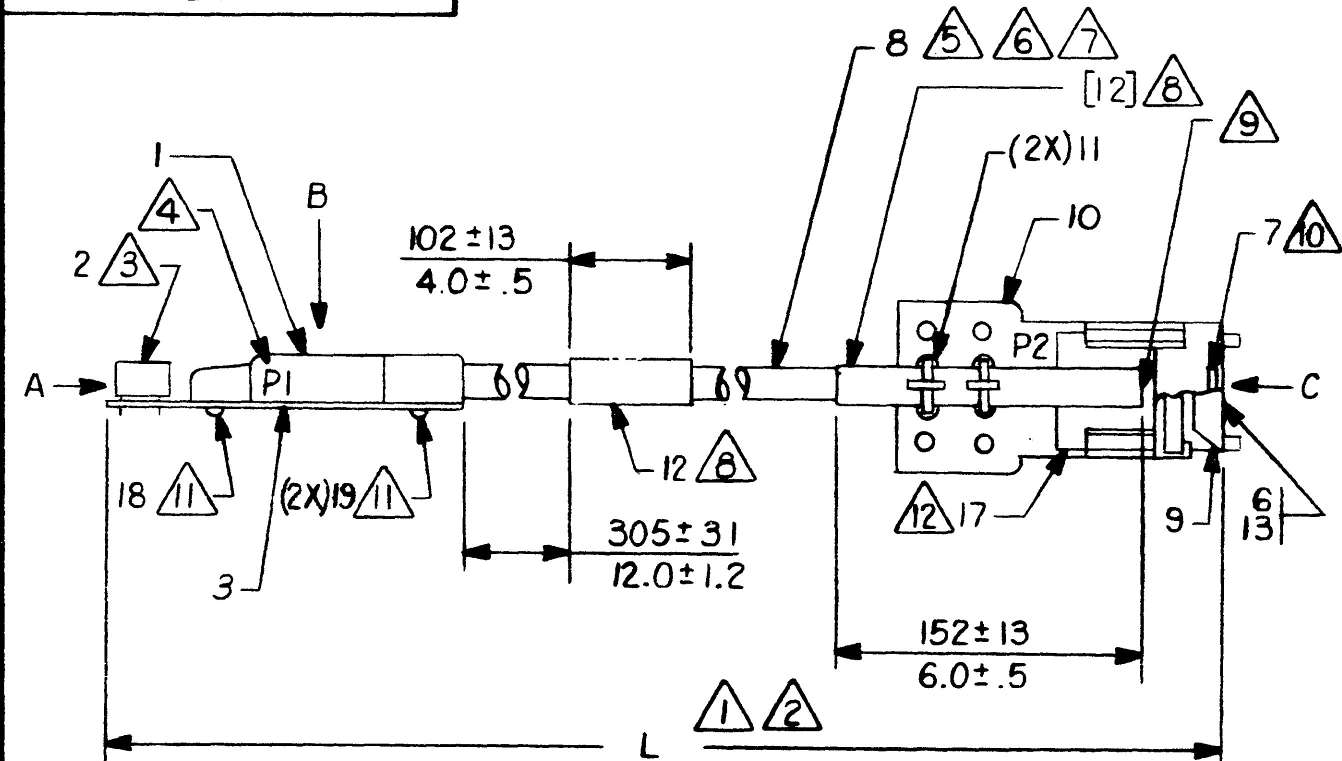


FIGURE 1. EXTERNAL CABLE ASSEMBLY

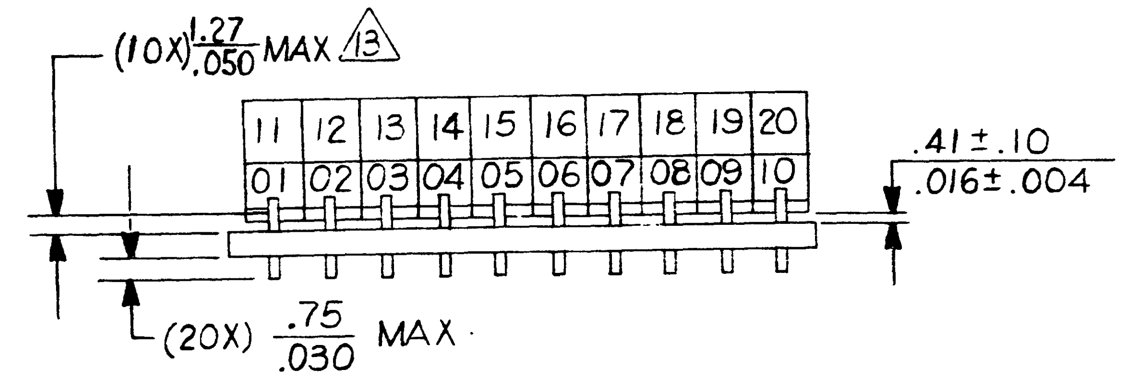
FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS = MILLIMETERS / INCHES; TOLERANCE OF SIZE AND FORM PER; INITIAL DESIGN; PROJECTION	MATL	**Honeywell** HONEYWELL INFORMATION SYSTEMS LOC PHOENIX, ARIZONA U. S. A.
	TREAT.	
	FIN.	TITLE I/O CABLE ASSEMBLY
SCALE NONE	CODE	DR C. RIPLEY 79-9-27
		APPD R.P. ABRAHAM 79-9-27

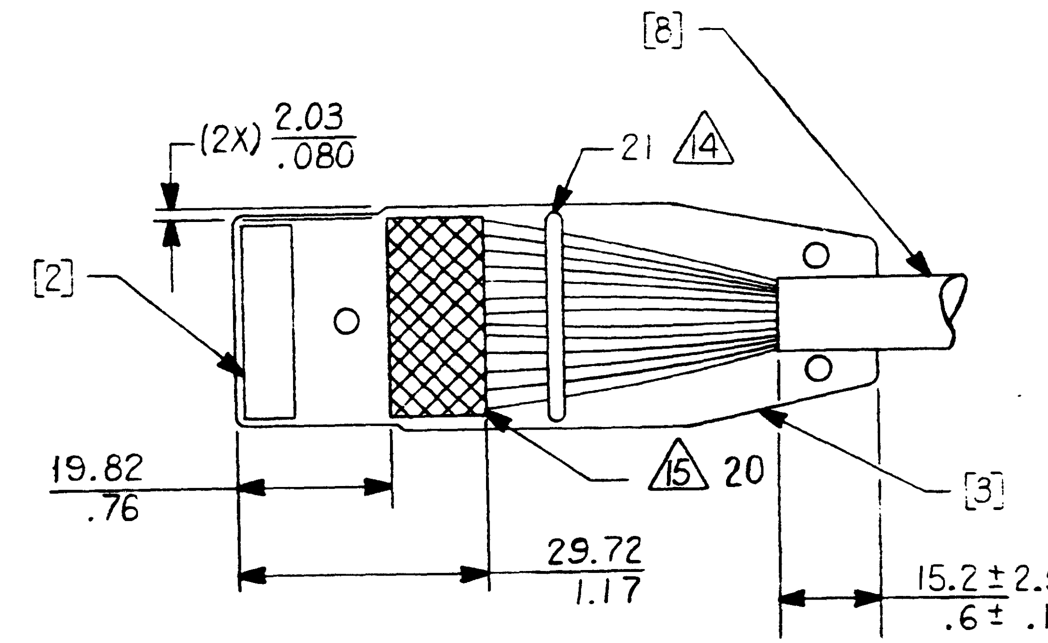
SIZE	DWG NO	SH	REV
A	58034110	1/6	K

CE 300 A-1 (12-71)

58034110



VIEW-A
PIN NUMBERING LOOKING AT CONNECTOR P1



VIEW-B 16

FIGURE 1. EXTERNAL CABLE ASSEMBLY-CONTINUED

Honeywell	SIZE	DWG NO	SH	REV
	A	58034110	2	K

CE 300 A-2 (5-73)

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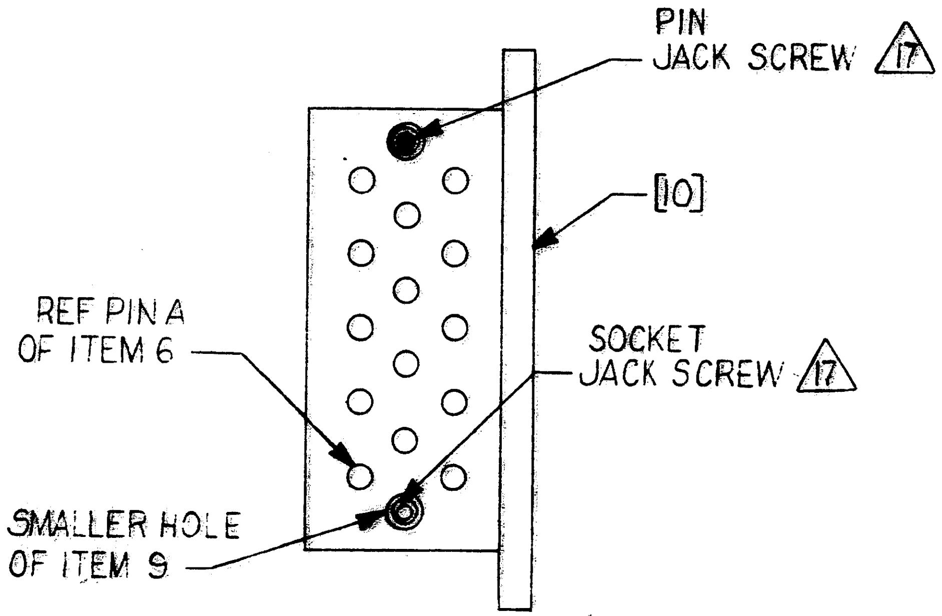


VIEW - C

FIGURE I. EXTERNAL CABLE ASSEMBLY- CONTINUED

TABLE I. TOLERANCE FOR CABLE ASM LENGTH △2

LENGTH RANGE (M)	TOLERANCE (M)
1 TO 10	+.15 , -0
11 TO 20	+.20 , -0
21 TO 30	+.30 , -0
31 TO 40	+.40 , -0
41 TO 50	+.50 , -0

TABLE II. WIRE LIST △5 △7 △18

FROM P1	TO P2
20	A
09	B
10	C
07	D
06	E
18	F
04	H
17	J
15	K
03	L
01	M
14	N
12	P
11	R

NOTES:

1. TAB-001 OF THIS DRAWING SHALL BE USED ONLY FOR ADVANCE ORDERING OF MATERIAL. THE CONDUCTOR LENGTH SPECIFIED IN TAB-001 IS AN AVERAGE LENGTH TO FACILITATE ADVANCE ORDERING.

2. THE TAB NUMBER (EXCEPT TAB 001) SPECIFIES THE CABLE ASM LENGTH IN METERS.

   EXAMPLE:

   580XXXXX-003 IS THE L DIMENSION OF A 3 METER CABLE ASM. TOLERANCE OF THE CABLE ASM LENGTH SHALL BE PER TABLE I.

3. SOLDER CONNECTOR (ITEM 2) TO PWB (ITEM 3) PER 58053700.

4. MARK PER 58053700.

5. TERMINATE CABLE (ITEM 8) TO PWB (ITEM 3) PER TABLE II WIRE LIST AND 58053700. EXTENSION OF CABLE'S CENTER CONDUCTORS BEYOND THE BOTTOM SIDE OF PWB (ITEM 3) SHALL BE .75 MM (.030 INCH) MAX. SOLDER CONNECTIONS AND EPOXY COAT PER 58053700.

6. THERE SHALL BE NO EVIDENCE OF THE CABLE'S JACKET MATERIAL HARDENING AS A RESULT OF THE SOLVENT CLEANING PROCESS.

7. TERMINATE CABLE (ITEM 8) TO CONTACTS (ITEM 13) PER 58053700 AND INSTALL INTO CONNECTOR (ITEM 6) PER TABLE II WIRE LIST.

8. MARK PER 58053700 AS A UL LISTED LOGIC CABLE ASM USING DRAWING NUMBER 58034110, TAB NUMBER, AND REVISION LETTER AS THE ASM IDENTIFICATION.

9. GAP BETWEEN THE CONNECTOR'S (ITEM 6) PLASTIC BODY AND SLEEVING (ITEM 12) SHALL BE 5 MM (.197 INCH) MAX.

10. APPLY TAPE (ITEM 7) TO BOTH SIDES OF CONNECTOR (ITEM 6) IN THE APPROXIMATE LOCATION SHOWN.

NOTES (CONTINUED):

11. SCREWS (ITEM 18 AND ITEM 19) ATTACH COVER (ITEM 1) TO PWB (ITEM 3).

12. APPLY TAPE (ITEM 17) TO CONNECTOR HOUSING (ITEM 10) AS SHOWN.

13. LEADS OF CONNECTOR (ITEM 2) SHALL NOT HAVE ANY SOLDER BEYOND DIMENSION SPECIFIED.

14. HOLD DOWN WIRE (ITEM 21) TO BE INSTALLED PER 58053700 AND SHALL HAVE A MAX EXTENSION BEYOND BOTTOM SIDE OF PWB (ITEM 3) OF .75 MM (.030 INCH).

15. CABLE TERMINATION NOT SHOWN IN ORDER TO MORE CLEARLY SHOW THE AREA TO WHICH THE EPOXY (ITEM 20) IS RESTRICTED. THE HEIGHT OF THE CURED EPOXY SHALL BE 2.21 MM (.087 IN.) MAX.

16. VIEW B IS SHOWN WITHOUT COVER (ITEM 1) INSTALLED.

17. JACKSCREWS OF CONNECTOR (ITEM 6) TO BE ASSEMBLED AS SHOWN.

18. PINS 02, 05, 08, 13, 16, AND 19 ARE GROUNDED TO CABLE SHIELD IN P1.

19. CABLE ASM SHALL MEET THE COMPLETED CABLE ASM REQUIREMENTS OF 58053700.

20. THIS CABLE ASM IS GOVERNED BY PURCHASE SPECIFICATION 58053707.

58081041

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	ASM TAB NO. 001	014	018	022	009	012	PL ALL	DWG.NO. 1	2	3	4	5	6
A	LEVEL I ISSUE	83	JUN	10	J.M.Botz 5-?-83	A	A	A	A			A	A					
B	PHA0GD519	83	OCT	31	G Drenth	B	B	B	B			B	B					
C	PHA0GD526	83	DEC	09	B Vanush	C	C	C	C			C	C					
C1	LEVEL 2 ENK149		ND		G DRENTH	C1	C1	C1	C1									
D	PHA0GD539	84	01	26	[illegible]	D	D	D	D			D	D	D	D	D	D	D
D1	ADD TABS 009, 012 Level 2	84	JUN	18	G Drenth					D1	D1	D1						

FOR CONTINUATION OF REVISION STATUS SEE SHEET

BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

CE 300 A-3 (1-79)

MADE BY R. Hoekstra 83, April 04

APPROVED R Abraham 5/20/83

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CABLE I/O ASM

SIZE	REVISION STATUS FOR	SHEET	REV
A	58081041	1/1	D1

DIST. 71

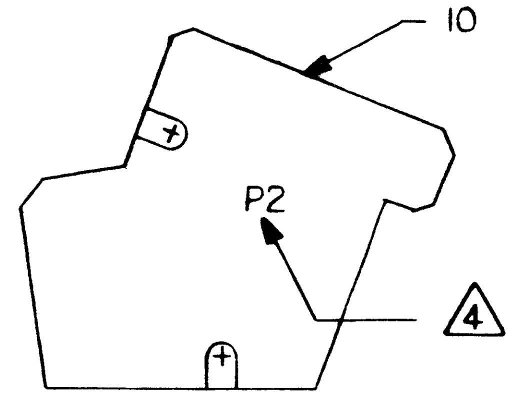
					001	009	012	014	018	022	
*	1 C	58034066-001	V	PADDLE BD COVER	1	1	1	1	1	1	EA
*	2 A	58000038-008	V	CONNECTOR, PWB	1	1	1	1	1	1	EA
*	3 C	58047470-003	A	PWB ETCH & DRILL	1	1	1	1	1	1	EA
*	6 A	76951105-563	V	SCREW THD FORMING	2	2	2	2	2	2	EA
*	7 A	58020397-001	V	CABL MULTICOND COAX	600	354	472	551	709	866	IN
*	8 A	76951105-502	V	SCREW THD FORMING	5	5	5	5	5	5	EA
*	9 D	60121950-001	P	HOOD CONN CASTING	1	1	1	1	1	1	EA
*	10 C	60121964-001	P	COVER	1	1	1	1	1	1	EA
*	11 A	60120593-001	P	RING PULL	1	1	1	1	1	1	EA
*	12 C	60121967-001	P	CAPTIVE SCREW	1	1	1	1	1	1	EA
*	13 B	60117607-001	P	STRAIN RELIEF	1	1	1	1	1	1	EA
*	14 A	03910182-001	V	LABEL PERMANENT	1	1	1	1	1	1	EA
*	15 B	58054218-003	A	PWB ETCH & DRL	1	1	1	1	1	1	EA
	15 B	58054218-002	A	PWB ETCH & DRILL	NOINT			NOINT	NOINT	NOINT	EA
*	16 B	8788222P120	V	SLEEVING	15	15	15	15	15	15	IN
*	21 A	58073431-011	V	LK/WASH.EXT.TOOTH,ST	2	2	2	2	2	2	EA

CABLE I/O ASSEMBLY

					001	009	012	014	018	022	
*	22	A	76951715-045	V LOCKWASHER	1	1	1	1	1	1	EA
*	23	A	76951715-059	V LOCKWASHER	2	2	2	2	2	2	EA
*	24	A	58033849	V #608 HYSOL	AR	AR	AR	AR	AR	AR	OZ
*	25	B	438111126P15	V WIRE BARE SOLID	3	3	3	3	3	3	IN
*	26	A	58053382-006	V TUBING,FLEX,CLEAR	1	1	1	1	1	1	IN
*	27	A	58053732	V IPL EXT CABLE ASM	X	X	X	X	X	X	EA

REF SPEC NO
58053700
58053732

REVISION					
REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE



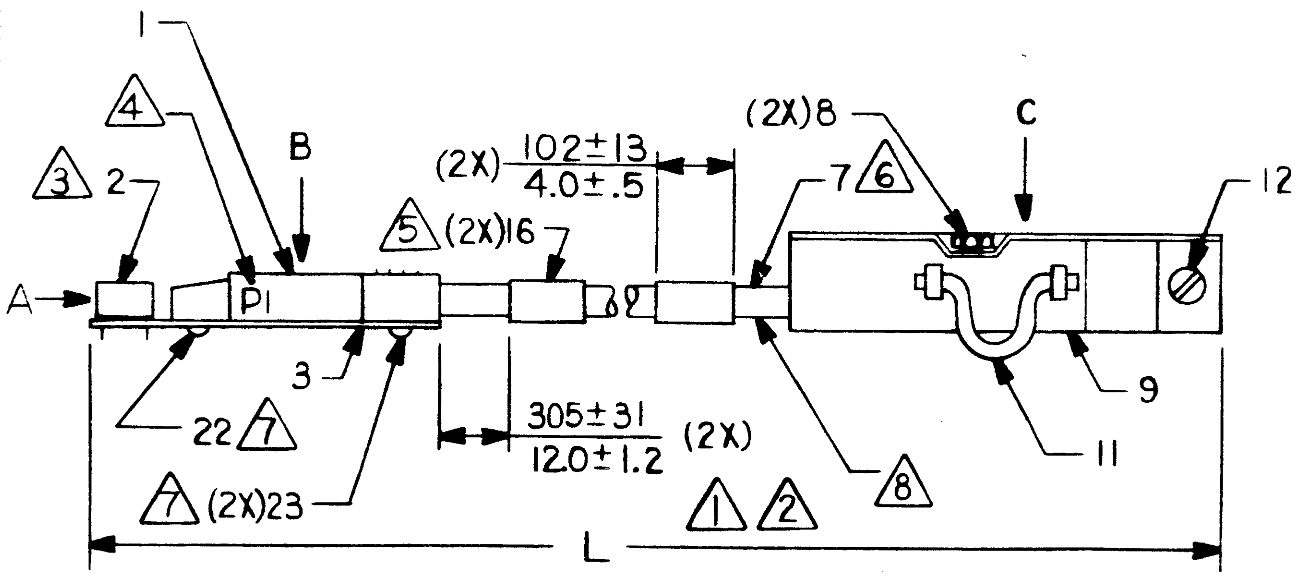
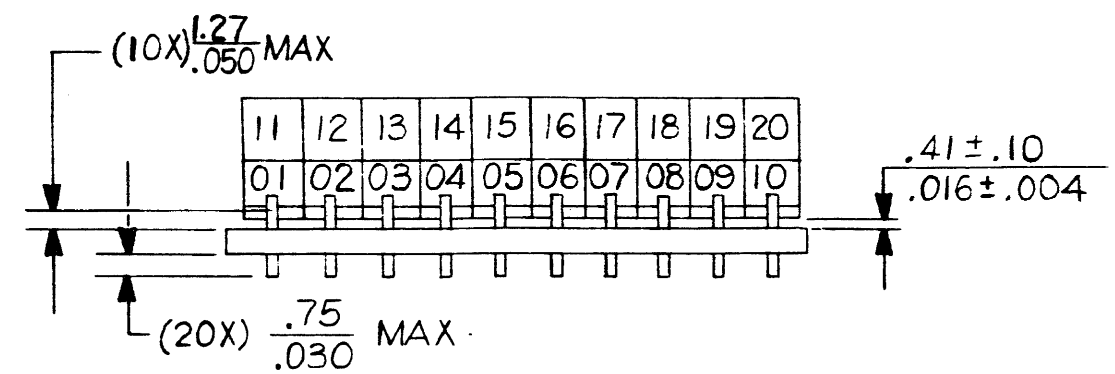


FIGURE I. EXTERNAL CABLE ASSEMBLY

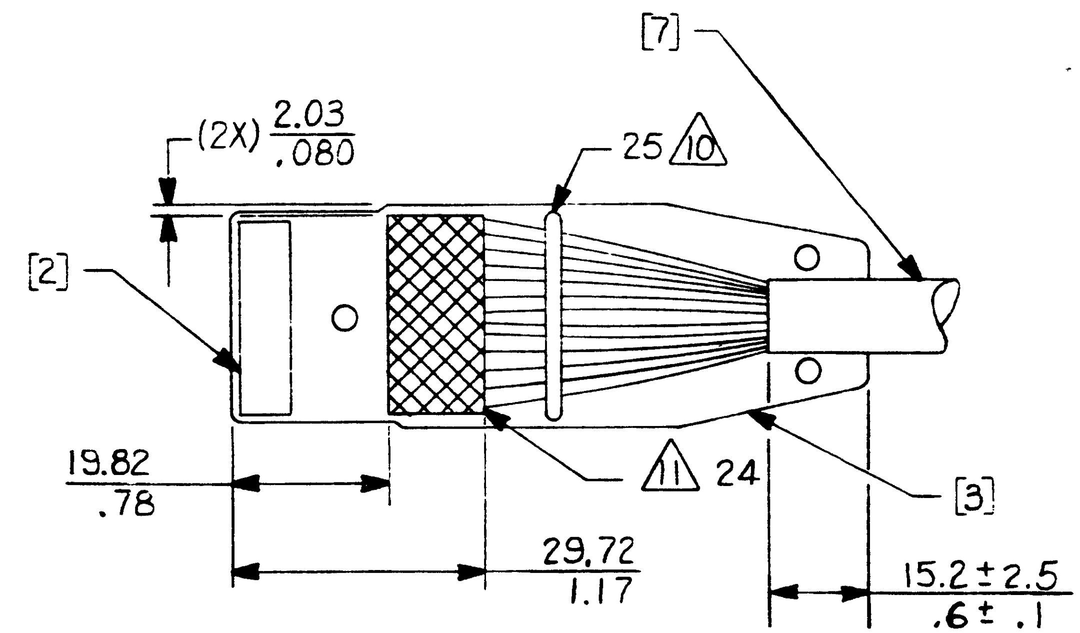
FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS = MILLIMETERS / INCHES TOLERANCE OF SIZE AND FORM PER INITIAL DESIGN PROJECTION	MATL TREAT. FIN.	**Honeywell** HONEYWELL INFORMATION SYSTEMS LOC PHOENIX, ARIZONA U. S. A. TITLE CABLE I/O ASSEMBLY
SCALE NONE | CODE	DR R.HOEKSTRA 83-04-05 APPD K.P. ABRAHAM 83-05-20	SIZE A | DWG NO 58081041 | SH 1/6 | REV D

CE 300 A (12 71)



VIEW–A
PIN NUMBERING LOOKING AT CONNECTOR P1



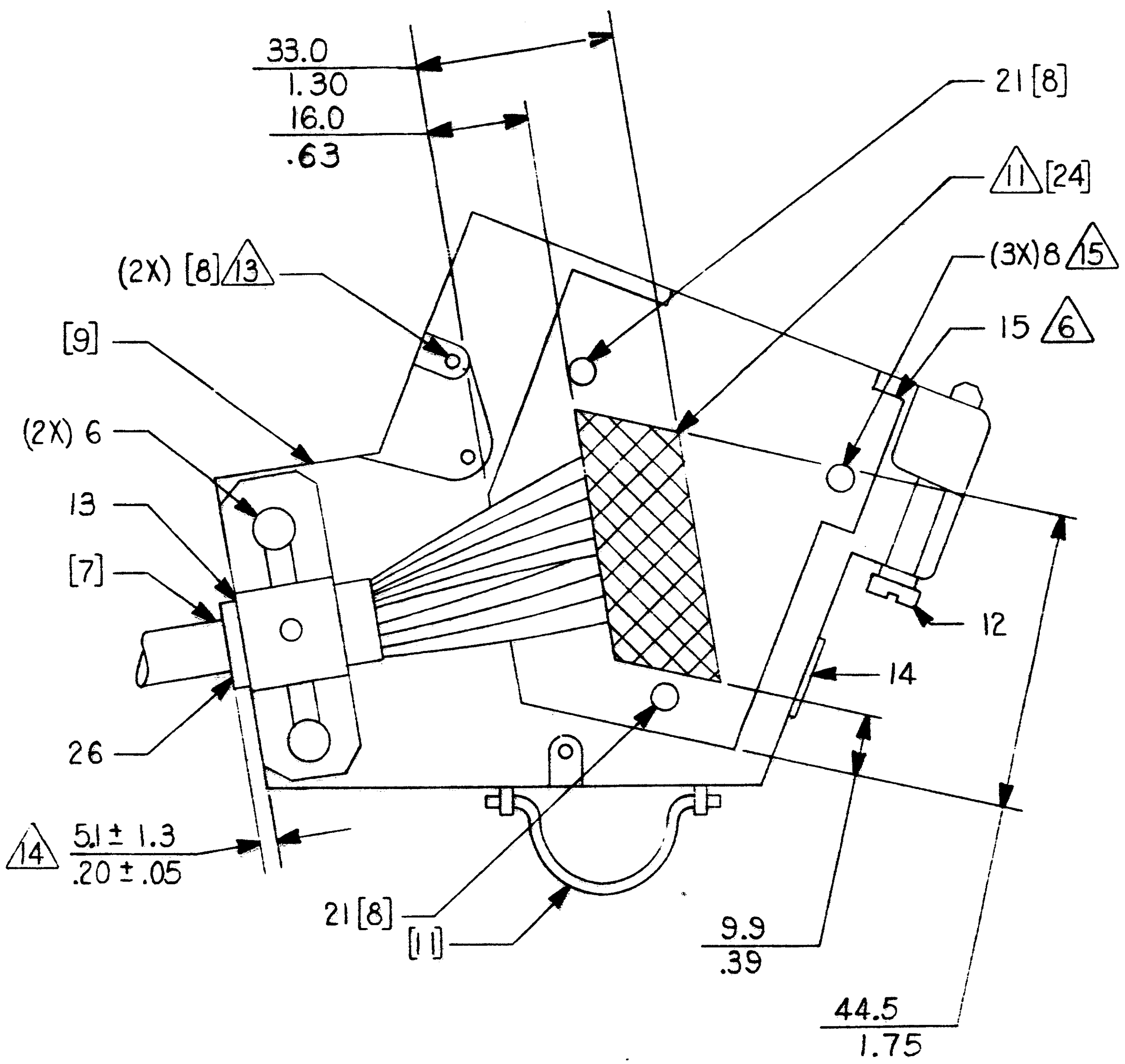
VIEW-B 12

FIGURE I. EXTERNAL CABLE ASSEMBLY-CONTINUED

Honeywell	SIZE A | DWG NO 58081041	SH 2	REV D

CE 300 A-2 (5-71)

THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROPRIETARY TO HONEYWELL INFORMATION SYSTEMS AND IS INTENDED FOR INTERNAL HONEYWELL USE ONLY. SUCH INFORMATION MAY BE DISTRIBUTED TO OTHERS ONLY BY WRITTEN PERMISSION OF AN AUTHORIZED HONEYWELL OFFICIAL. THIS RESTRICTION DOES NOT APPLY TO VENDOR PROPRIETARY PARTS THAT MAY BE DISCLOSED IN THIS DOCUMENT.



VIEW- C 16

FIGURE I. EXTERNAL CABLE ASSEMBLY

TABLE I. TOLERANCE FOR CABLE ASM LENGTH 2

LENGTH RANGE (M)	TOLERANCE (M)
1 TO 10	+.15 , -0
11 TO 20	+.20 , -0
21 TO 30	+.30 , -0
31 TO 40	+.40 , -0
41 TO 50	+.50 , -0

TABLE II. WIRE LIST 6 17

FROM P1	TO P2
01	13
03	14
04	16
06	59
07	19
09	21
10	20
11	11
12	12
14	53
15	15
17	56
18	17
20	22

NOTES:

1. TAB-001 OF THIS DRAWING SHALL BE USED ONLY FOR ADVANCE ORDERING OF MATERIAL. THE CONDUCTOR LENGTH SPECIFIED IN TAB-001 IS AN AVERAGE LENGTH TO FACILITATE ADVANCE ORDERING.

2. THE TAB NUMBER (EXCEPT TAB 001) SPECIFIES THE CABLE ASM LENGTH IN METERS.

   EXAMPLE:

   580XXXXX-003 IS THE L DIMENSION OF A 3 METER CABLE ASM. TOLERANCE OF THE CABLE ASM LENGTH SHALL BE PER TABLE I.

3. SOLDER CONNECTOR (ITEM 2) TO PWB (ITEM 3) PER 58053700.

4. MARK PER 58053700.

5. MARK PER 58053700 AS A UL LISTED LOGIC CABLE ASM USING DRAWING NUMBER 58081041, TAB NUMBER, AND REVISION LETTER AS THE ASM IDENTIFICATION.

6. TERMINATE CABLE (ITEM 7) TO PWB'S (ITEM 3 AND ITEM 15) PER TABLE II WIRE LIST AND 58053700. SOLDER CONNECTIONS AND EPOXY COAT PER 58053700.

7. SCREWS (ITEM 18 AND ITEM 19) ATTACH COVER (ITEM 1) TO PWB (ITEM 3).

8. THERE SHALL BE NO EVIDENCE OF THE CABLE'S JACKET MATERIAL HARDENING AS A RESULT OF THE SOLVENT CLEANING PROCESS.

9. LEADS OF CONNECTOR (ITEM 2) SHALL NOT HAVE ANY SOLDER BEYOND DIMENSION SPECIFIED.

10. HOLD DOWN WIRE (ITEM 25) TO BE INSTALLED PER 58053700 AND SHALL HAVE A MAX EXTENSION BEYOND BOTTOM SIDE OF PWB (ITEM 3) OF .75 MM (.030 INCH).

NOTES (CONTINUED):

11. CABLE TERMINATION NOT SHOWN IN ORDER TO MORE CLEARLY SHOW THE AREA TO WHICH THE EPOXY (ITEM 24) IS RESTRICTED. THE HEIGHT OF THE CURED EPOXY SHALL BE 2.21 MM (.087 IN.) MAX.

12. VIEW B IS SHOWN WITHOUT COVER (ITEM 1) INSTALLED.

13. SCREWS (ITEM 8) ATTACH COVER (ITEM 10) TO CONNECTOR CASTING (ITEM 9).

14. CABLE (ITEM 7) SHALL BE SECURELY CLAMPED TO CONNECTOR CASTING (ITEM 9) USING STRAIN RELIEF (ITEM 13), SCREWS (ITEM 6), AND TUBING (ITEM 26). WHEN INSTALLED, TUBING (ITEM 26) SHALL EXTEND WITHIN DIMENSION SPECIFIED.

15. SCREWS (ITEM 8) ATTACH PWB (ITEM 15) TO CONNECTOR CASTING (ITEM 9).

16. VIEW C IS SHOWN WITHOUT COVER (ITEM 10) INSTALLED.

17. PINS 02, 05, 08, 13, 16, AND 19 ARE GROUNDED TO CABLE SHIELDS IN BOTH P1 AND P2.

18. CABLE ASM SHALL MEET THE COMPLETED CABLE ASM REQUIREMENTS OF 58053700.

19. THIS CABLE ASM IS GOVERNED BY PURCHASE SPECIFICATION 58053732.

58034102

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB 001	TAB 014	TAB 018	TAB 022	PL ALL	ASM 1
A	LEVEL 1-ISSUE	79	10	09	S.E. Steoda 79-09-28	A				A	A
B	PHAØFC008	79	Nov	15	C. Ripley	B					B
C	PHAØPV083	79	12	13	P.M. D'Agostino	C				C	
D	PHAØPV140	80	03	24	A. Lopez	D				D	D
E	PHAØPV165	80	DEC	10	Carrie Dale	E				E	
F	PHAØXW114	82	APR	02	A.J. Steele	F	F	F	F	F	F
G	PHAØGD483	83	06	21	S. Miller	G	G	G	G		G
						INACTIVE-RESV	INACTIVE-RESV	INACTIVE-RESV	INACTIVE-RESV		

F.C.F.

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS

LOC PHOENIX, ARIZONA

MADE BY Ted Gulford 79,MAY,23

APPROVED R. M. Abraham 79/09/20

REVISION STATUS FOR EACH PAGE, SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CABLE I/O

SIZE C | REVISION STATUS FOR 58034102 | SHEET 1/1 | REV G

CE 800 A-3 (12-71) BRUNING 44-141

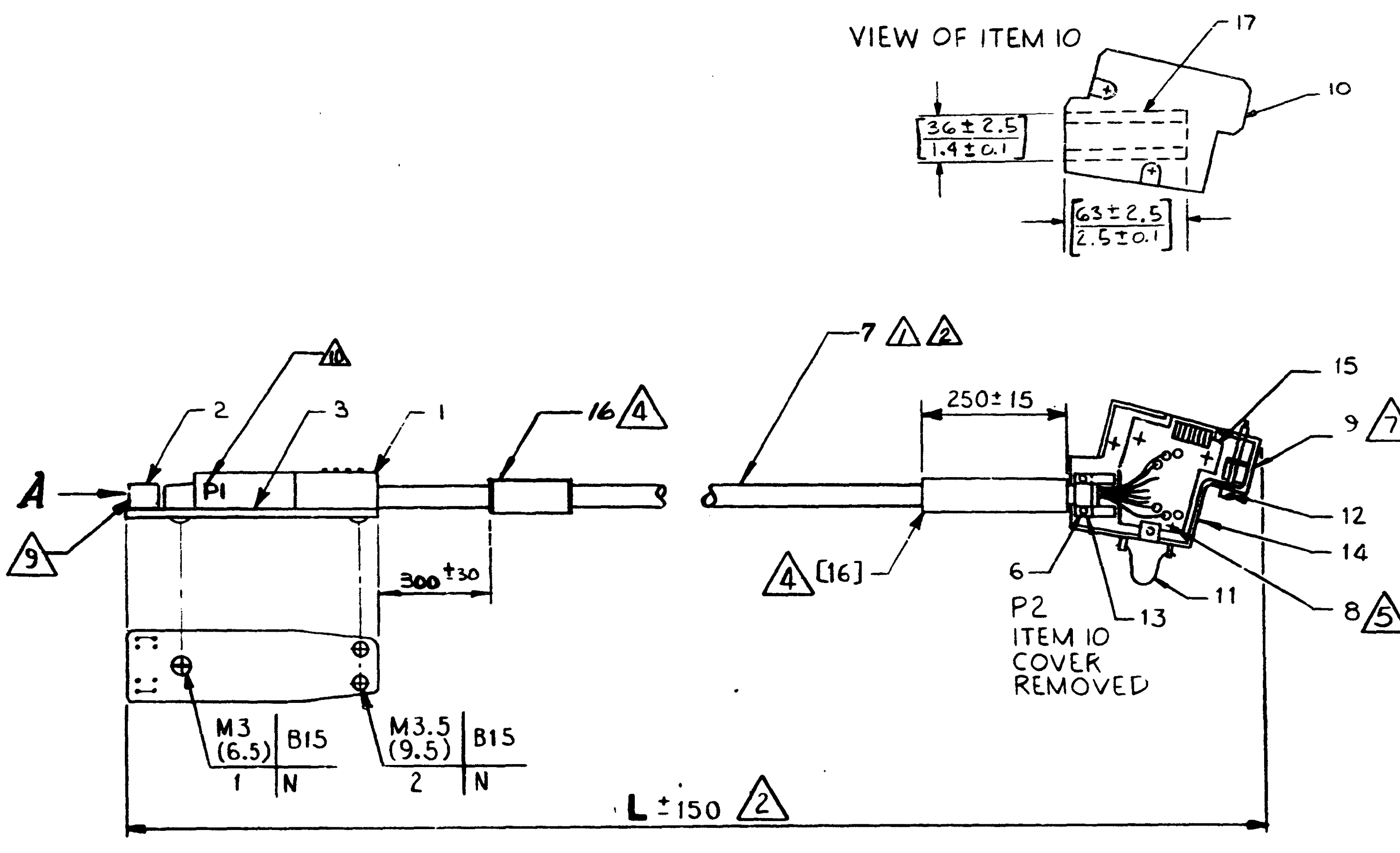
DIST. C106- 73

				001	014	018	022	
•	1 C	58034066-001	V PADDLE BD COVER	1	1	1	1	EA
•	2 A	58000038-008	V CONNECTOR, PWB	1	1	1	1	EA
•	3 C	58047470-003	A PWB ETCH & DRILL	1	1	1	1	EA
•	6 A	76951105-563	V SCREW THD FORMING	2	2	2	2	EA
•	7 A	58020397-001	V CABL MULTICOND COAX	600	551	709	866	IN
•	8 A	76951105-502	V SCREW THD FORMING	5	5	5	5	EA
•	9 D	60121950-001	P HOOD CONN CASTING	1	1	1	1	EA
•	10 C	60121964-001	P COVER	1	1	1	1	EA
•	11 A	60120593-001	P RING PULL	1	1	1	1	EA
•	12 C	60121967-001	P CAPTIVE SCREW	1	1	1	1	EA
•	13 B	60117607-001	P STRAIN RELIEF	1	1	1	1	EA
•	14 A	03910182-001	V LABEL PERMANENT	1	1	1	1	EA
•	15 B	58054218-002	A PWB ETCH & DRILL	1	1	1	1	EA
•	16 B	878B222P120	V SLEEVING	15	15	15	15	IN
•	17 A	43A115944P42	P TAPE POLYESTER	5	5	5	5	IN

CABLE, I/O

REV	AUTHORITY	DATE YR MO DAY	SIGNATURE

REVISIONS



001 1

INACTIVE-
FOR NEW DESIGN
SEE DWG- 58081041

11	12	13	14	15	16	17	18	19	20
01	02	03	04	05	06	07	08	09	10

VIEW-A
PIN NUMBERING LOOKING AT CONNETOR P1.

WIRE LIST 7

FROM P1	TO P2
01	13
03	14
04	16
06	59
07	19
09	21
10	20
11	11
12	12
14	53
15	15
17	56
18	17
20	22

NOTES:

△1. TAB-001 OF THIS DRAWING SHALL BE USED ONLY FOR ADVANCE ORDERING OF MATERIAL. ~~THE CONDUCTOR LENGTH SPECIFIED IN TAB 001 IS AN AVERAGE LENGTH TO FACILITATE ADVANCE ORDERING.~~

△2. THE TAB NUMBERS (EXCEPT TAB 001) SPECIFIES THE CABLE LENGTH IN METERS. TYPICAL EXAMPLE ARE: 58034102-003 IDENTIFIES A 3 METER CABLE. PREFERRED STANDARD CABLE LENGTHS. USE CABLE LENGTHS 14, 18 AND 22 METERS.

3. ASSEMBLE HARDWARE PER M50EB00505-CR.

△4. MARK PER 43A144110 AS A UL LISTED LOGIC CABLE.

△5. ITEM 8 (SCREWS) ATTACHES ITEMS 15 AND 10 TO 9.

△6. PINS 02, 05, 08, 13, 16 & 19 ARE GROUNDED TO CABLE SHIELDS IN BOTH CONNECTORS.

△7. ITEM 9 IS SHOWN WITH COVER REMOVED.

8. ASSEMBLE ITEMS 2 & 7 TO ITEM 3 AND ITEM 7 TO ITEM 15 PER 43A226454.

△9. CONNECTOR ITEM 2 SHALL BE SOLDERED 0.4±0.1mm ABOVE SURFACE OF ITEM 3.

△10 MARK PER. 43A226458 CLASS-C.

11. THE MAXIMUM SOLDERED LEAD LENGTH OF CONNECTOR ITEM 2 SHALL BE .75MM BEYOND THE SURFACE OF PWB ITEM 3.

12. ASSEMBLE COAX ITEM 7 TO PWBS ITEM 3 AND ITEM 15 PER 58020440.

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS= MILLIMETERS / INCHES	MATL
TOLERANCE OF SIZE AND FORM PER	DES. 79 JUN 14
INITIAL DESIGN M	CHKR 79 SEP 27
PROJECTION	FIN.
SCALE / CODE	DR 79 JUN 5
79-09-28	APPD 79/09/20
	DISTR L106-73

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC PHOENIX, ARIZONA U. S. A.

TITLE CABLE I/O

FCF:

SIZE	DWG NO	SH	REV
C	58034102	1/1	G

REF SPEC NO

58034102

58059634

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	ASSEMBLY TAB 001	101	002	102	702	802	PL ALL	DRAWING SHEET 1
A	LEVEL I ISSUE	82	01	18	[illegible] 12-21-81	A	A					A	A
B	PHA0XS094	82	06	16	S. Miller	B	B					B	B
C	PHA0SR154	83	03	10	G Drenth	C	C					C	
D	PHA0NJ016	83	10	05	G Drenth		D					D	D
D1	ENXS149		ND		G Drenth	D1	D1						
E	PHA0XS365	84	JAN	04	G Drenth	E	E	E	E			E	E
F	PHA0NJ027	84	JAN	13	G Drenth	OBSOLETE	OBSOLETE	F	F	F		F	
G	PHA0NJ030	84	JUN	11	G Drenth			G		G	G	G	

ECF

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY S. Jackson 11 DEC 81

APPROVED C.E. Wilcox 12/17/81

TITLE DAU PANEL ASSEMBLY

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

SIZE	REVISION STATUS FOR	SHEET	REV
C	58059634	1/1	G

DIST. 3

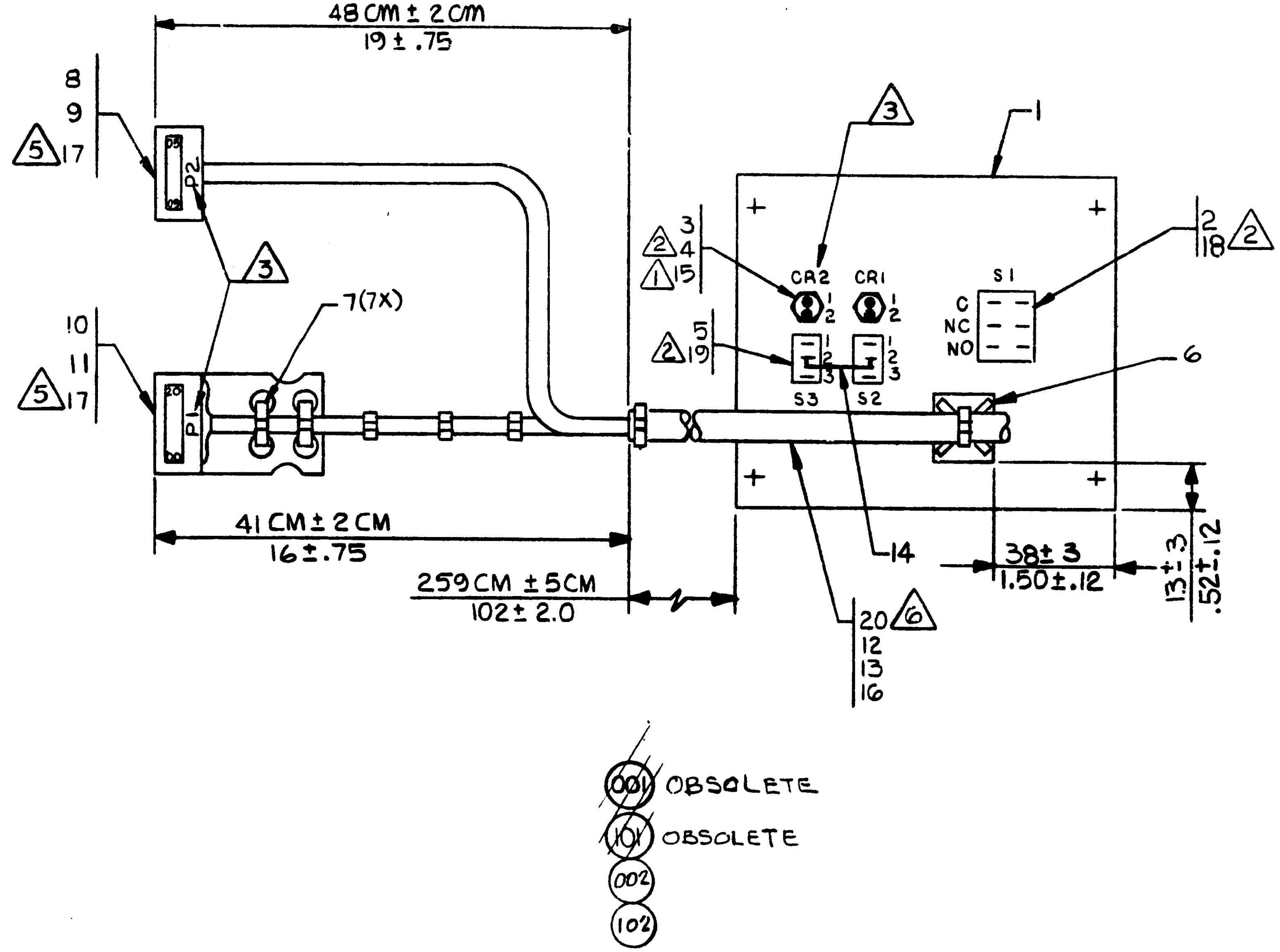
BRUNING 44-141 40368

CE 300 A-3 (1-79)

				002	102	702	802	
1	C	58059633-001	P DAU CONFIG PANEL	1				EA
2	B	8768219P8	V SWITCH PB	1				EA
3	A	58020206-001	V DIODE,LIGHT EMIT,RED	2				EA
4	A	58000076-002	P HOLDER LED	2				EA
5	A	58008225-004	V SWITCH MIN TOGGLE	2				EA
6	C	43C142270P52	V CLAMP CABLE	1				EA
7	C	43C142270P8	V CLAMP CABLE		7			EA
8	B	43B166701P67	V DECAL			1		EA
9	B	43B216136P1	V HOUSING MINI			1		EA
10	B	58028255-002	A ID CONNECTOR			1		EA
11	B	43B166701P4	V DECAL			1		EA
12	A	43A180043P209	V WIRE PAIR TWIST			245		IN
13	A	43A167218P029	V WIRE			480	3	IN
14	B	43B111126P15	V WIRE BARE SOLID	3				IN
15	B	8738126P40	V SLEEVING ELEC	2				IN
16	A	58008294-001	V SLEEVING ZIPPER			100		IN

DAU PNL ASM

					002	102	702	802	
17	B	438216106P1	V	MINI TERMINAL			14		EA
18	B	876B219P1101	V	GUARD, BUTTON	1				EA
19	B	438175995P4	V	CAP PLASTIC	2				EA
20	C	58059634-102	A	DAU PNL WIRING	1				EA
21	A	58057946-002	D	W.L.MAIN PNL	X	X	X		
22	C	58059634-702	A	DAU PNL ASM		1			EA
* 23	C	58059634-802	A	DAU PNL ASM	1				EA



NOTES:

1. SHRINK SLEEVING ON ALL DIODES.
2. ASSEMBLE PER 43A232701 FIG 15, 19A AND 30.
3. MARK PER 43A226458 CLASS C.
4. CORRECT HARNESS LENGTHS, CABLE CLAMPS OR TIES AND ROUTING TO BE ESTABLISHED BY MANUFACTURING.
5. INSTALL MINI TERMINAL IN CORNER AND END CAVITIES TO INCREASE CONNECTOR RETENTION.
6. MARK PER 43A144110 AS AN UNLISTED HARNESS.

58059634

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

REVISIONS					
REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE

REF SPEC NO
43A144110
43A226458
43A232701

CF 300 C (12-71)

UNLESS OTHERWISE SPECIFIED
DIMENSIONS = MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN M
PROJECTION

CODE

MATL

DES. S. [illegible] 21 Dec 81
CHK.
FIN.
DR W. [illegible] 81 Nov 12
APPD C. E. Wilcox 12/17/81
DISTR C120-3 C125-3

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC PHOENIX, ARIZONA U. S. A.

TITLE DAU PANEL ASSEMBLY
FCF

SIZE	DWG NO	SH	REV
C	58059634	1/1	E

0 10 20 30 40 50 60 70 80 MM
0 1 2 3 IN

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58047483

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO. 001	TAB NO. 002	PL SH ALL	DWG SH 1
A	LEVEL I ISSUE	79	09	19	T Chiarello 9/13/79	A		A	A
B	PHAØGD289	80	06	20	Shackelford	B	B	B	B
B1 C	ENXW008 PHAØGD468	83	ND 04	22	G Drenth G Drenth	INACTIVE	B1 C	C	
D	PHAØGD592	84	05	14	G Drenth		D		D

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS

LOC PHOENIX, ARIZONA

MADE BY W. E. Hakkinen 79/04/05

APPROVED [signature] 79/08/06

TITLE JUMPER BD ASM

REVISION STATUS FOR EACH PAGE, SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

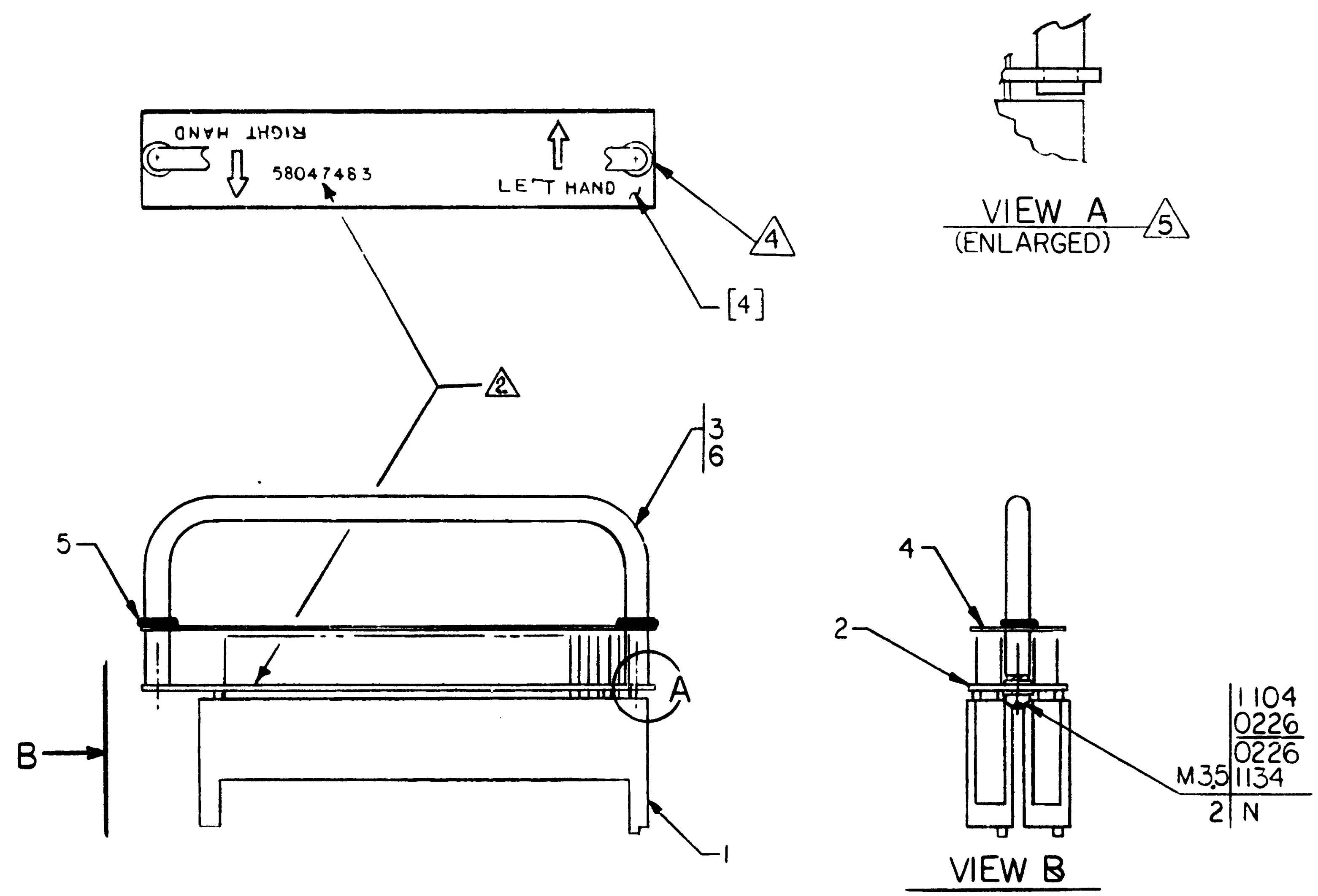
SIZE	REVISION STATUS FOR	SHEET	REV
C	58047483	1/1	D

CE 300 A-3 (12-71) BRUNING 44-141

					001	002	
	1 C	43C175991P1	P CONNECTOR 88PIN		2	2	EA
	2 C	58047482-001	A PWB ETCH & DRL		1	1	EA
	3 B	58047415-002	P HANDLE		1		EA
	4 C	58047478-001	P COVER		1	1	EA
	5 A	N5601P9	P BUNA N O-RING		2		EA
*	5 A	12A1566P80	V SEAL O RING			2	EA
*	5 A	N5601P9	P BUNA N O-RING			INTCH	EA
	6 B	58056711-004	P HANDLE			1	EA

JUMPER BD ASM

REVISIONS					
REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE



NOTES:

1. ASSEMBLE PER 43A226454.
2. △ MARK ASSEMBLY NUMBER PER 43A226458 CLASS C.
3. ASSEMBLE HARDWARE PER M50EB00506-CR.
4. △ PWB NOTCH THIS END.
5. △ FIT GROOVE IN HANDLE INTO NOTCH ON END OF BOARD AND ATTACH FASTENING HARDWARE TO OPPOSITE END.

(001) INACTIVE-DO NOT USE ON NEW DRAWINGS-SEE TAB-002.

(002) △5

58047483

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

REF SPEC NO
M50EB00506-CR
43A226458
43A226454

UNLESS OTHERWISE SPECIFIED DIMENSIONS= MILLIMETERS / INCHES	MATL	Honeywell HONEYWELL INFORMATION SYSTEMS
TOLERANCE OF SIZE AND FORM PER	TREAS. CHECKED H. Kayen Sept 10 1979	LOC PHOENIX, ARIZONA U. S. A.
INITIAL DESIGN M	FIN.	TITLE JUMPER BOARD ASM
PROJECTION		
SCALE 1/1	CODE	DR W. E. Hakkinen 79/04/05
Thall 9/13/79	APPD [signature] SEPT. 6, 1979	SIZE C — DWG NO 58047483 — SH 1/1 — REV D
	DISTR C107-30	

BRUNING 44-141 CE 300 C (12-71)

0 10 20 30 40 50 60 70 80 MM
0 1 2 3 IN

ORIGINAL LOST

58006130

REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE	ASM TAB. NO 001	002	003	PL ALL	DWG. SH. 1
A	ISSUED	73	03	26	R. HOEKSTRA	A				
B	PHAØCX011	74	05	06	R. HOEKSTRA	B				
B1	C.O# AT REV B SHOULD BE PHAØXC011	74	07	15	R. HOEKSTRA	B1				
B2	ADD TAB002 PER EWA Z3921	77	02	03	W. SEIDERS		B2			
C	PHAØXJ043 AND ADDED TAB-003	78	06	05	R. HOEKSTRA		C	C		
D	PHAØGB066	79	05	11	B. VANASIK	D	D	D		
E	PHAØGB097	81	07	31	[signature]	E	E	E	E	E

FCF: 58006131

FOR CONTINUATION OF REVISION STATUS SEE SHEET

BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

CE 300 A-3 (1-79)

MADE BY R. HOKESTRA 73-FEB-19
S. J. Stal 81-JULY-13

APPROVED J.M WOODS 3-7-73

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CABLE, PSI ADAPTER

SIZE C | REVISION STATUS FOR 58006130 | SHEET V1 | REV E

DIST. L 22-2-3

PD 81/07/28

SIZE		SHEET	REV
C	58006130	1/1	E

*	ITEM NO.	P C	IDENTIFICATION NO.	S C	DRAWING TITLE	ASSEMBLY / QUANTITY 001	002	003						U M
	1	C	43C175991P1	P	CONNECTOR 88PIN	2	2	2						EA
*	2	A	43A216152P2	V	CABLE MULTICOND	131	191	191						IN
	3	A	58003661-001	D	WIRE LIST	X		X						
	4	C	43C142270P8	V	CLAMP CABLE	4	4	4						EA
	5	D	58035970-001	V	COVER,CONN BRACKET	2	2	2						EA
	5	D	43D232042P1	P	CONN.SHIELD ID	INTCH	INTCH	INTCH						EA
	6	D	58016519-001	V	SHIELD CONN	2	2	2						EA
	6	D	43D232043P1	P	CONN.SHIELD	INTCH	INTCH	INTCH						EA
	7	D	43D232044	D	ASM INSTRUCTION	X	X	X						
	8	A	N402P5C13	V	WASHER FLAT	DISC								EA
	9	A	58028075-001	D	WL PSI FREE EDGE		X							

Honeywell

HONEYWELL INFORMATION SYSTEMS
LOC: PHOENIX, ARIZONA, U.S.A.

UM = UNIT OF MEASURE
EA = EACH IN = INCHES
CM = CENTIMETER OZ = OUNCE
G = GRAMS

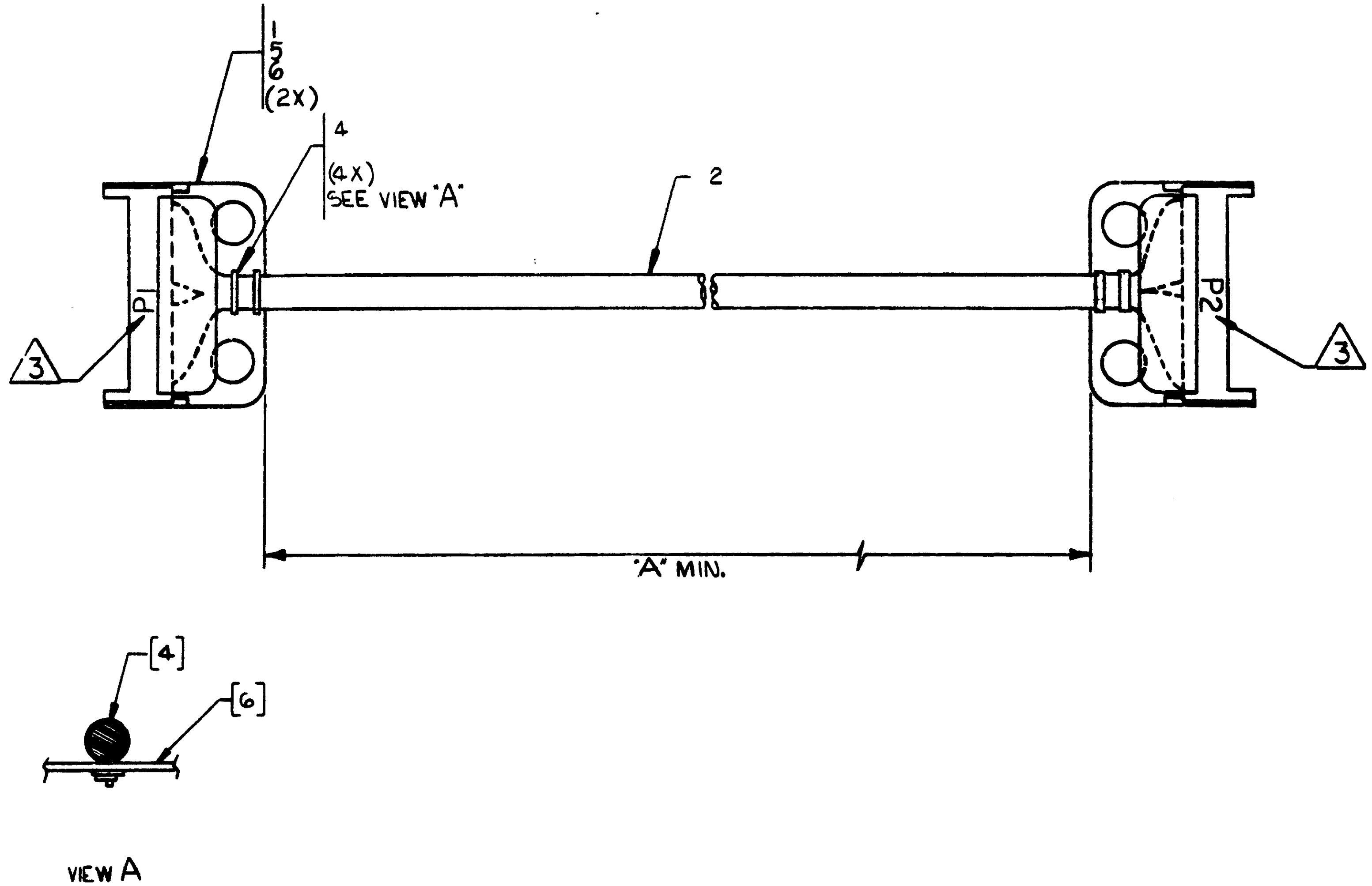
* ITEMS REVISED SINCE PREVIOUS ISSUE

TITLE
CABLE PSI ADAPT

SIZE	P.L. NO.	SHEET	REV.
C	58006130	1/1	E

DOES DOCUMENT REVISION STATUS SHEET EXIST? YES

CE 300A 4 (0-74)



TAB NO.	"A" DIM.
001	120.00
002	180.00
003	180.00

△3. MARK IN AREA SHOWN PER 43A226458, CLASS "C"

△2. MARK PER 43A144110.

1. DRAWING INTERPRETATION PER 43A226599.

NOTES:

FOR DOCUMENT STATUS SEE REVISION STATUS SHEET.

REVISIONS			
REV	AUTHORITY	DATE YR MO DAY	SIGNATURE

REF SPEC NO
43A226458
43A144110
43A226599

CE 300 C (12-71)

UNLESS OTHERWISE SPECIFIED
DIMENSIONS = MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN IN.
PROJECTION

CODE G.L.K. 73-3-12

Ben J. Bryan 3-14-73

MATL

TREAT.

FIN.

DR [signature] 73 Feb. 19

APPD [signature] 3-7-73 [signature] 3-7-73

DISTR L22-3

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC PHOENIX, ARIZONA U. S. A.

TITLE CABLE, PSI ADAPTER
FCF: 58006131

SIZE	DWG NO	SH	REV
C	58006130	1/1	E

58006130

0 10 20 30 40 50 60 70 80 MM
0 1 2 3 IN

58059990

REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE	ASM. TAB NO. 500	PL ALL	DWG. SH. NO. 1
A	LEVEL 1 ISSUE	82	08	13	8-9-82 D Webster	A	A	A
B	PHAO GD483	83	JUN	21	S. Miller	B	B	B
B1	Level 2 ENXS149		ND		G Drenth	B1		
C	PHAOGD734	85	JAN	30	G Drenth	C	C	C

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY CH Bentley BLADS 2

APPROVED [illegible] 8/4/82

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE IPL CABLE SELECT FCF: 58059593

SIZE	REVISION STATUS FOR	SHEET	REV
A	58059990	1/1	C

DIST. 73

BRUNING 44-141 40366

CE 300 A-3 (1-79)

				500	
	1 A	58034110-001	A I/O CABLE ASSEMBLY	X	EA
	2 A	58034110-014	A I/O CABLE ASSEMBLY	X	EA
	3 A	58034110-018	A I/O CABLE ASSEMBLY	X	EA
*	4 A	58034110-023	A I/O CABLE ASSEMBLY	X	EA
	5 A	58081041-001	A CABLE I/O ASSEMBLY	X	EA
	5 C	58034102-001	A CABLE,I/O	INTCH	EA
	6 A	58081041-014	A CABLE I/O ASSEMBLY	X	EA
	6 C	58034102-014	A CABLE I/O	INTCH	EA
	7 A	58081041-018	A CABLE I/O ASSEMBLY	X	EA
	7 C	58034102-018	A CABLE I/O	INTCH	EA
*	8 A	58081041-023	A CABLE I/O ASSEMBLY	X	EA

IPL CABLE SELECT

58059990

REF SPEC NO

REVISION			
REV	AUTHORITY	DATE YR MO DAY	SIGNATURE

500

AT LEAST ONE PAIR AND UP TO FOUR PAIRS (DEPENDING ON NUMBER OF DISK DRIVES) OF THE FOLLOWING IPL CABLES LISTED BELOW ARE REQUIRED WITH EACH DISK DEVICE INTERFACE OPTION WDDI66LA.

SELECT THE PROPER PAIR (PAIRS) PER MARKETING INSTRUCTIONS.

IDENT No.	LENGTH	QTY REQD	
(FOR 4XX DISK DRIVES)			
58034110-001	AD REQD	1 TO 4 PAIRS	
58034110-014	14 METERS	"	
58034110-018	18 METERS	"	
58034110-023	23 METERS	"	
(FOR 5XX DISK DRIVES)			
58034102-001	AS REQD	1 TO 4 PAIRS	INACTIVE
58034102-014	14 METERS	"	INACTIVE
58034102-018	18 METERS	"	INACTIVE
58034102-022	22 METERS	"	INACTIVE
58081041-001	AS REQ'D	1 TO 4 PAIRS	
58081041-014	14 METERS	"	
58081041-018	18 METERS	"	
58081041-023	23 METERS	"	

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS = MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN M
PROJECTION

MATL

TREAT

FIN.

SCALE CODE

DR [signature] 8-4-82

APPD [signature] 8/4/82

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC PHOENIX, ARIZONA U. S. A.

TITLE IPL CABLE SELECT

SIZE	DWG NO	SH	REV
A	58059990	1/1	C

58059992

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	ASM. TAB. NO. 500	PL ALL	DWG. SH. NO. 1
A	LEVEL 1 ISSUE	82	08	13	8-9-82 D Webster	A	A	A
B	PHAO GD483	83	JUN	21	S. Miller	B	B	B
B1	LEVEL 2 ENXS149		ND		G Drenth	B1		
C	PHAO GD734	85	JAN	30	G Drenth	C	C	C

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY C [illegible] 82/6/29

APPROVED J. A. Roehlke 7/30/82

TITLE IPL CABLE SELECT

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

SIZE	REVISION STATUS FOR	SHEET	REV
A	58059992	1/1	C

DIST. 73

BRUNING 44-141 40366

CE 300 A-3 (1-79)

.PD 85/01/31 *SECTION- 1* A 58059992 1/1 C

					500	
	1	A	58034110-001	A I/O CABLE ASSEMBLY	X	EA
	2	A	58034110-014	A I/O CABLE ASSEMBLY	X	EA
	3	A	58034110-018	A I/O CABLE ASSEMBLY	X	EA
*	4	A	58034110-023	A I/O CABLE ASSEMBLY	X	EA
	5	A	58081041-001	A CABLE I/O ASSEMBLY	X	EA
	5	C	58034102-001	A CABLE, I/O	INTCH	EA
	6	A	58081041-014	A CABLE I/O ASSEMBLY	X	EA
	6	C	58034102-014	A CABLE I/O	INTCH	EA
	7	A	58081041-018	A CABLE I/O ASSEMBLY	X	EA
	7	C	58034102-018	A CABLE I/O	INTCH	EA
*	8	A	58081041-023	A CABLE I/O ASSEMBLY	X	EA

IPL CABLE SELECT

A 58059992 1/1 C

58059992

REF SPEC NO

REVISION					
REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE

500

AT LEAST ONE PAIR AND UP TO FOUR PAIRS (DEPENDING ON NUMBER OF DISK DRIVES) OF THE FOLLOWING IPL CABLES LISTED BELOW ARE REQUIRED WITH EACH DEVICE ADAPTER OPTION WDAU66LA OR WDAU66LB.

SELECT THE PROPER PAIR (PAIRS) PER MARKETING INSTRUCTIONS.

IDENT No.	LENGTH	QTY REQD	
(FOR 4XX DISK DRIVES)			
58034110-001	AS REQD	1 TO 4 PAIRS	
58034110-014	14 METERS	"	
58034110-018	18 METERS	"	
58034110-023	23 METERS	"	
(FOR 5XX DISK DRIVES)			
58034102-001	AS REQD	1 TO 4 PAIRS	INACTIVE
58034102-014	14 METERS	"	INACTIVE
58034102-018	18 METERS	"	INACTIVE
58034102-022	22 METERS	"	INACTIVE
58081041-001	AS REQ'D	1 TO 4 PAIRS	
58081041-014	14 METERS	"	
58081041-018	18 METERS	"	
58081041-023	23 METERS	"	

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS = MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN
PROJECTION

MATL
TREAT
FIN.

SCALE | CODE

DR [signature]
APPD G. A. Rochlke 7/30/82

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC PHOENIX, ARIZONA U. S. A.

TITLE IPL CABLE SELECT

SIZE	DWG NO	SH	REV
A	58059992	1/1	C

CE 300 A (12-71) BRUNING 44-141

58082911

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB 500	PL ALL	DWG. SHT. 1
A	LEVEL-1-ISSUE	86	01	16	1/16/85	A	A	A

FCF: 58082908

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX, ARIZONA

MADE BY Ted [illegible] Jan '86

APPROVED J.A. Rehlke 1/7/86

REVISION STATUS FOR EACH PAGE, SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE IPL CABLE SELECT

SIZE	REVISION STATUS FOR	SHEET	REV
A	58082911	1/1	A

DIST. -73

BRUNING 44-141 40366

CE 300 A-3 (1-79)

				500		
*	1	A	58082960-001	A SHIELDED I/O CABLE	X	EA
*	2	A	58082960-009	A SHIELDED I/O CABLE	X	EA
*	3	A	58082960-014	A SHIELDED I/O CABLE	X	EA
*	4	A	58082960-018	A SHIELDED I/O CABLE	X	EA
*	5	A	58082960-023	A SHIELDED I/O CABLE	X	EA
*	6	A	58082959-001	A SHIELDED I/O CABLE	X	EA
*	7	A	58082959-009	A SHIELDED I/O CABLE	X	EA
*	8	A	58082959-014	A SHIELDED I/O CABLE	X	EA
*	9	A	58082959-018	A SHIELDED I/O CABLE	X	EA
*	10	A	58082959-023	A SHIELDED I/O CABLE	X	EA

IPL CABLE SELECT

Honeywell

Dwg No.	Rev.	Sheet
58082911	A	1/1

PRINT TO | TITLE IPL CABLE SELECT

500

AT LEAST ONE PAIR AND UP TO FOUR PAIRS (DEPENDING ON NUMBER OF DISK DRIVES) OF THE FOLLOWING IPL CABLES LISTED BELOW ARE REQUIRED WITH EACH OPTION.

SELECT THE PROPER PAIR (PAIRS)PER MARKETING INSTR-TIONS.

IDENT NO.	LENGTH	QTY REQD.
(FOR 4XX DISK DRIVES)		
58082960-001	AS REQUIRED	1 TO 4 PAIRS
58082960-009	9 METERS	" "
58082960-014	14 METERS	
58082960-018	18 METERS	" "
58082960-023	23 METERS	" "
(FOR 5XX DISK DRIVES)		
58082959-001	AS REQUIRED	1 TO 4 PAIRS
58082959-009	9 METERS	
58082959-014	14 METERS	" "
58082959-018	18 METERS	" "
58082959-023	23 METERS	" "

MADE BY	REV.	DATE		DWG.NO.	SH.NO.
[illegible] 86 Jan 7				58082911	1/1

58082782

REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE	TAB NO. 001	002	PL ALL	DWG. SH. NO. 1	2	3	4	5	6	7
A	LEVEL 1 ISSUE	85	12	13	W Toledo	A	A	A	A	A	A	A	A	A	A
B	PHAØGE056	86	05	13	D. Williams	B		B							

FOR CONTINUATION OF REVISION STATUS SEE SHEET

BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX, ARIZONA

CE 380 A-3 (1-79)

MADE BY Sandy Hamngel 85JUN18

APPROVED T Chiarelli 11-26-85

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE BULKHEAD HARNESS

SIZE	REVISION STATUS FOR	SHEET	REV
A	58082782	1/1	B

DIST. 71A

				001	002	
1	C	43C175991P1	P CONNECTOR 88PIN	1	1	EA
2	D	58035970-001	W COVER,CONN BRACKET	1	1	EA
3	D	58016519-001	W SHIELD CONN	1	1	EA
4	B	878B222P180	V SLEEVING	2	2	IN
5	C	43C142270P8	V CLAMP CABLE	12	8	EA
6	A	43A216152P15	V CABLE TWPR	80	80	IN
7	B	878B222P060	V SLEEVING THERMO	4	4	IN
8	B	43B138943P2	P SCREW LOCK ASM.	8	8	EA
9	B	43B223079P18	W CONN SUB-MIN CR	4	4	EA
10	B	43B223079P104	W SOCKET	112	112	EA
12	B	878B222P090	V SLVG SHRINKING	40	40	IN
13	B	58082841-004	A PLATE, BULKHEAD	1		EA
14	B	58093421-002	P CONSOLE CONN PLATE		2	EA
15	B	58095390-002	P NUT BAR		2	EA
16	A	58041104-503	V SCREW,CR RECES, P HD		4	EA
17	A	58041134-490	V LOCKWASH SPR ST M		4	EA

					001	002	
	18	A	58041126-490	V WASHER,FLAT,STL.		4	EA
	19	C	43C142270P52	V CLAMP CABLE		2	EA
*	20	B	58082879-002	P CONNECTOR PLATE	4		EA
*	20	B	58082879-001	P CONNECTOR PLATE	INTCH		EA
	21	A	58060950-030	D LABEL	1	1	EA
	22	A	58041104-593	V SCREW,CR RECES, P HD	2		EA
	23	A	58041134-580	V LOCKWASH SPR ST M	2		EA
	24	A	58020396-005	W WASHER INSULATING	2		EA

58082782

REF. SPEC.
58053700

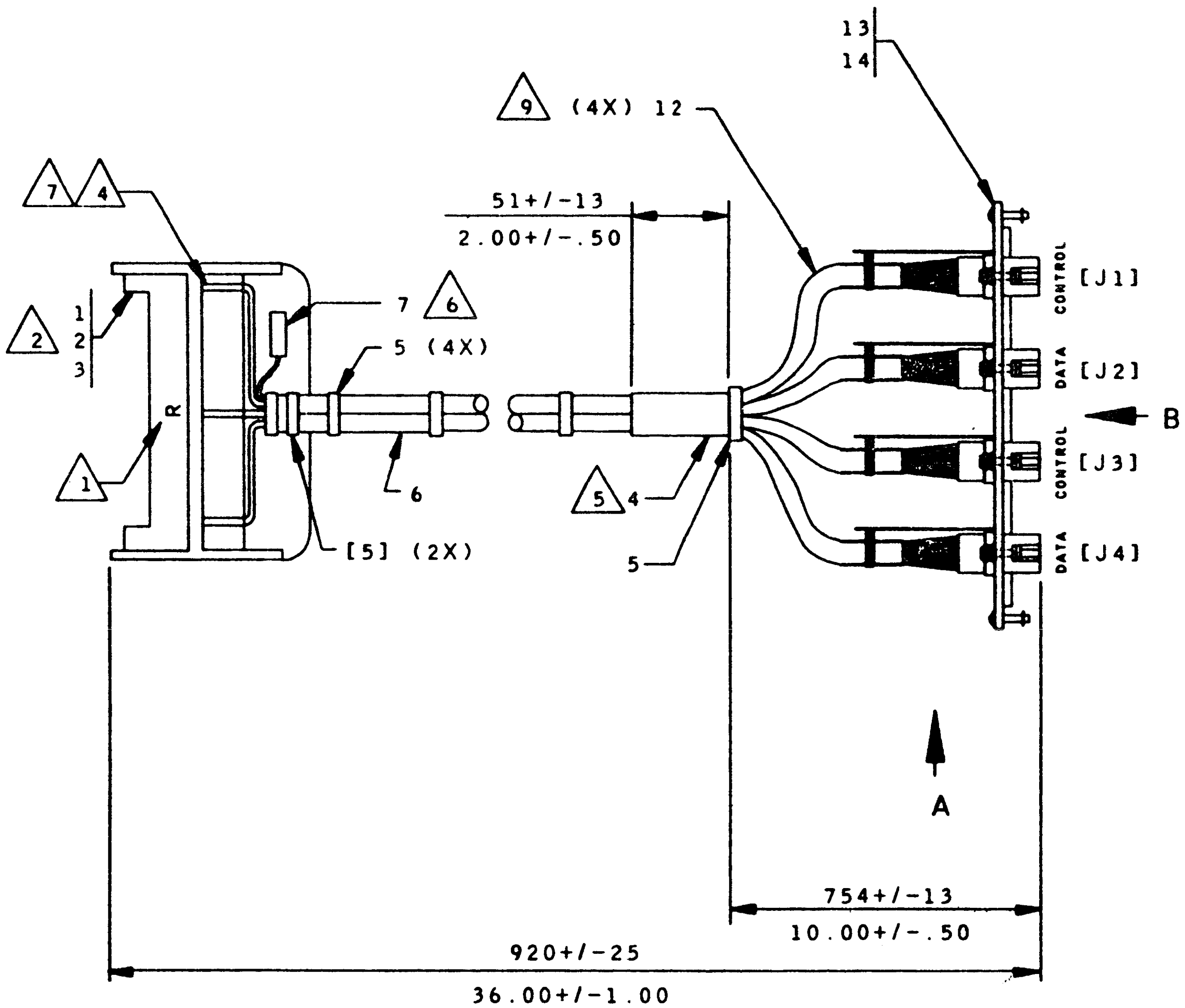
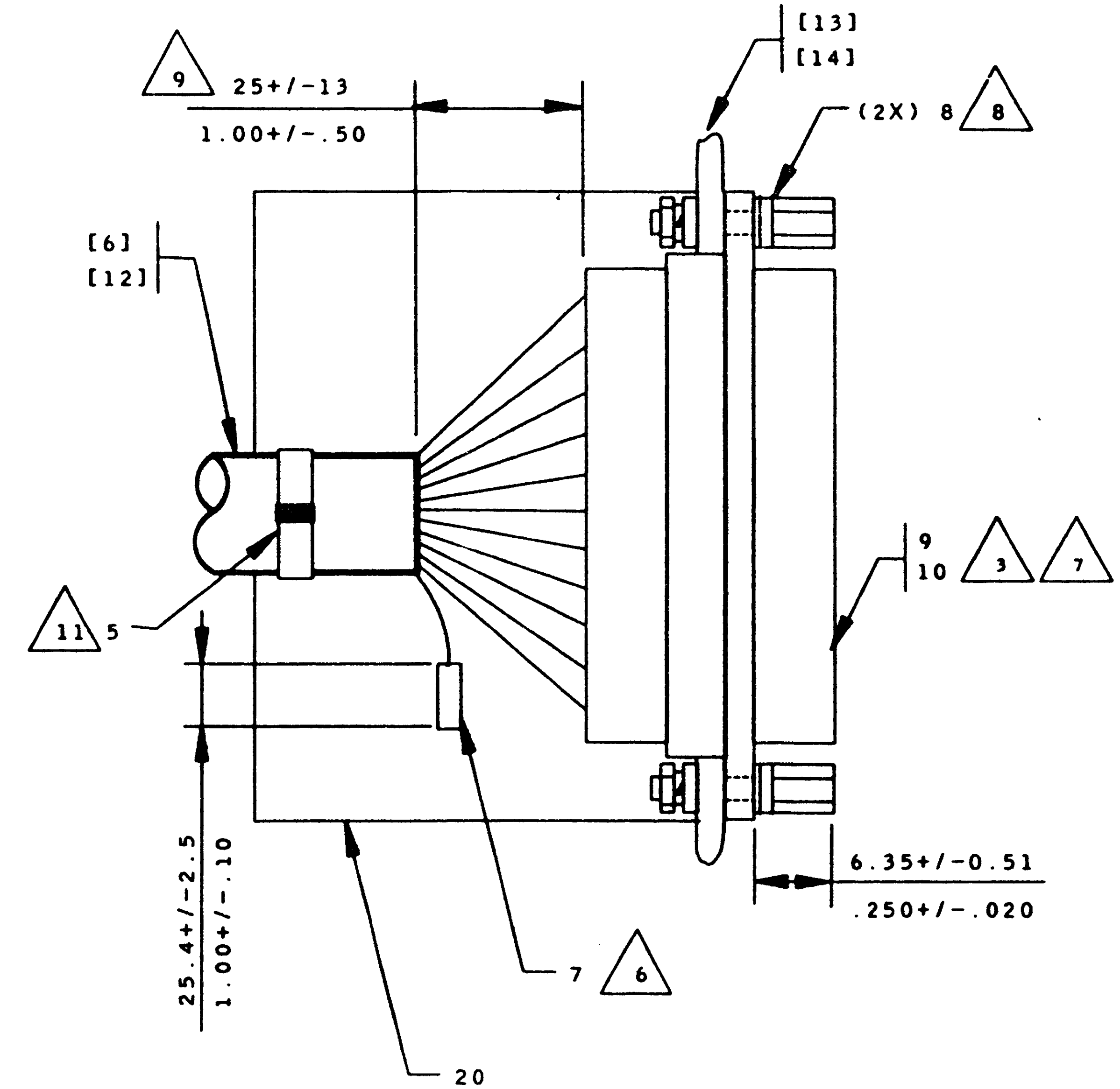


FIGURE 1, INTERNAL CABLE ASSEMBLY

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET.

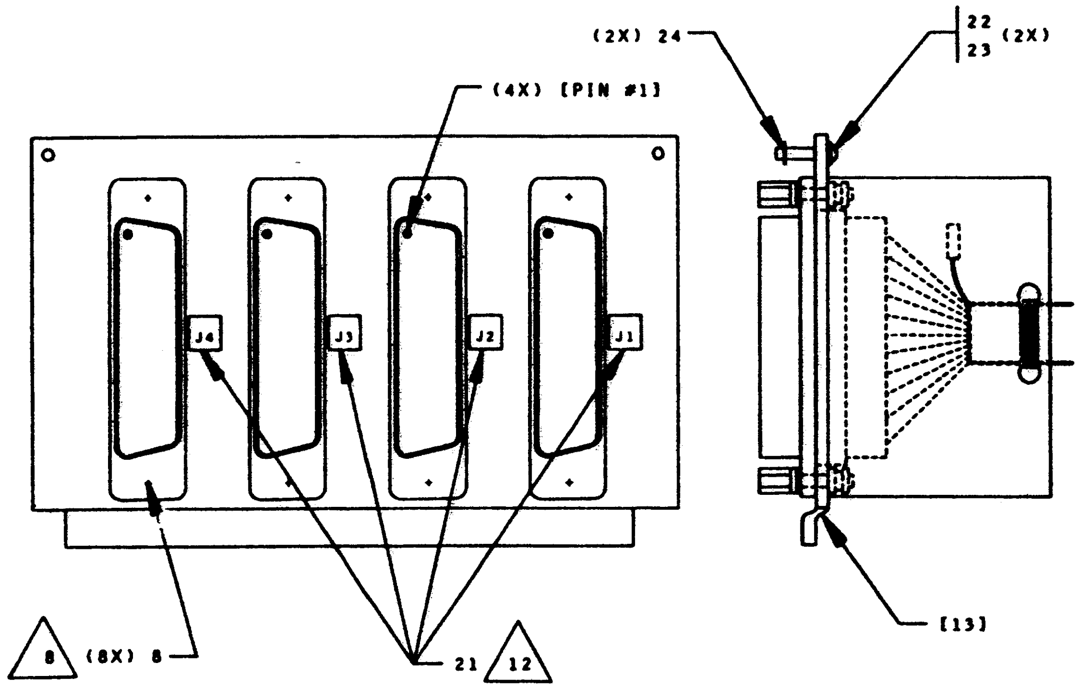
UNLESS OTHERWISE SPECIFIED DIMENSIONS: MILLIMETERS / INCHES. TOLERANCE OF SIZE AND FORM PER	MATL	HONEYWELL HONEYWELL INFORMATION SYSTEMS LOC PHOENIX, ARIZONA U.S.A.
INITIAL DESIGN	DSN	TITLE
PROJECTION	CHK FIN	BULKHEAD HARNESS
SCALE NONE / CODE	DR Crete Ripley 850CT02	SIZE A / DWG NO 58082782 / SH 1/7 / REV A
FCF	APPR DISTR CODE: - - -	

58082782



VIEW-A (4X)

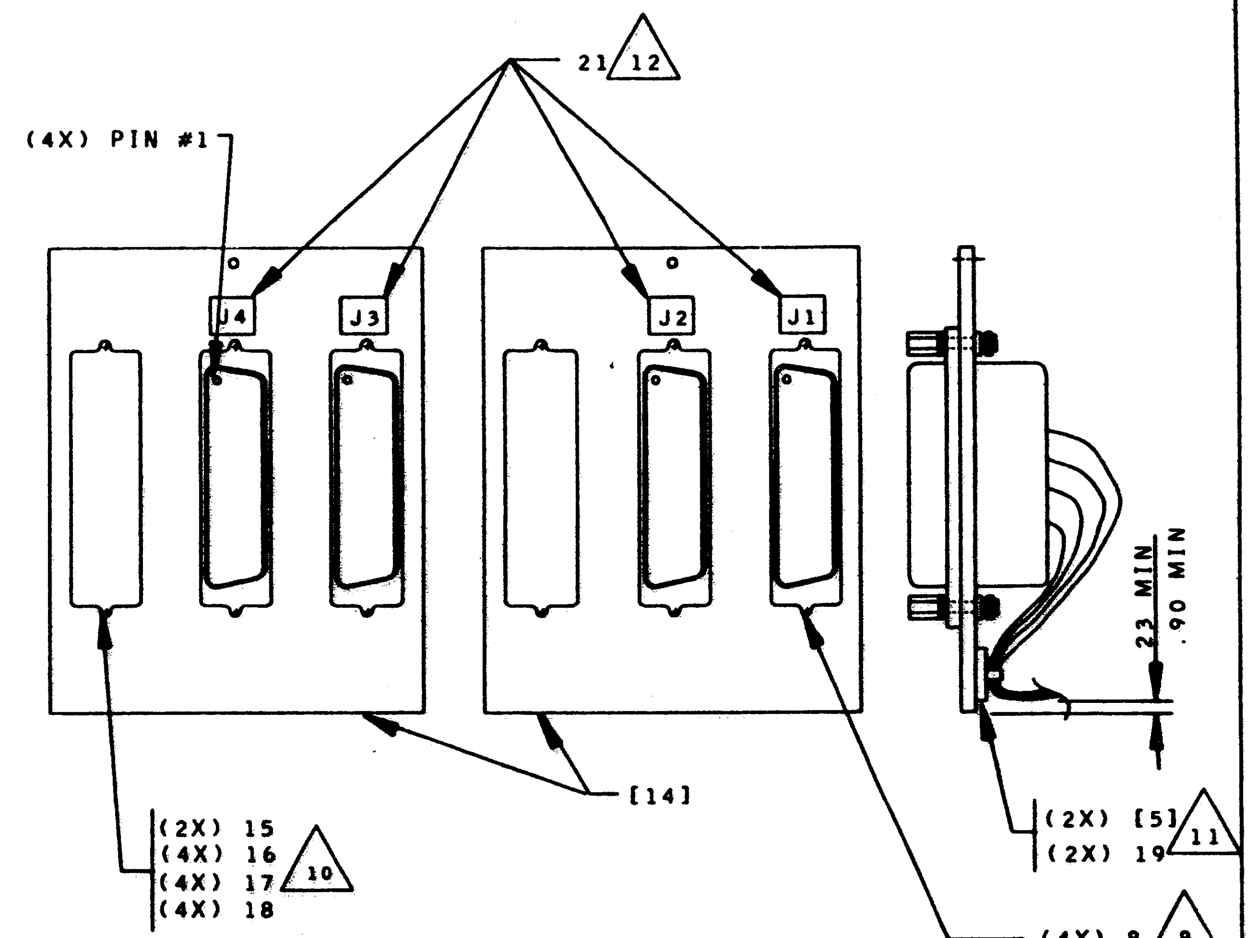
Honeywell HONEYWELL INFORMATION SYSTEMS	SIZE A	DWG NO 58082782	SH 2	REV A



001

VIEW B

ROTATED 90° CLOCKWISE



002

VIEW-B

ROATED 90° CLOCKWISE

TABLE I. WIRE LIST 3 4

CONTROL		DATA		CONTROL		DATA	
FROM	TO	FROM	TO	FROM	TO	FROM	TO
A00	J01 02	B00	J02 02	C00	J03 02	D00	J04 02
02	20	02	20	02	20	02	20
01	03	01	03	01	03	01	03
05	21	05	21	05	21	05	21
03	04	03	04	03	04	03	04
05	22	05	22	05	22	05	22
04	05	04	05	04	05	04	05
02	23	02	23	02	23	02	23
06	06	06	06	06	06	06	06
08	24	08	24	08	24	08	24
07	07	07	07	07	07	07	07
11	25	11	25	11	25	11	25
09	08	09	08	09	08	09	08
11	26	11	26	11	26	11	26
10	09	10	09	10	09	10	09
08	27	08	27	08	27	08	27
12	10	12	10	12	10	12	10
14	28	14	28	14	28	14	28
13	11	13	11	13	11	13	11
17	29	17	29	17	29	17	29
15	12	15	12	15	12	15	12
17	30	17	30	17	30	17	30
16	13	16	13	16	13	16	13
14	31	14	31	14	31	14	31
18	14	18	14	18	14	18	14
20	32	20	32	20	32	20	32
19	15	19	15	19	15	19	15
A20	J01 33	B20	J02 33	C20	J03 33	D20	J04 33

NOTES:

1. MARK PER 58053700.

2. INSTALL SHIELDS (ITEM 2 AND ITEM 3) ONTO CONNECTOR (ITEM 1).

3. TERMINATE TWISTED PAIR WIRES OF CABLE (ITEM 6) TO CONTACTS (ITEM 10) AND CRIMP PER 58053700. INSTALL TERMINATED WIRES INTO CONNECTOR (ITEM 9) PER TABLE I WIRE LIST.

4. TWISTED PAIR WIRES OF CABLE (ITEM 6) SHALL BE FIRST LEVEL WIRE WRAPPED TO PINS OF CONNECTOR (ITEM 1) PER 58053700 USING TABLE I WIRE LIST.

5. MARK PER 58053700 AS AN UNLISTED LOGIC CABLE ASM USING DRAWING NUMBER, TAB NUMBER, AND REVISION LETTER AS THE ASM IDENTIFICATION.

6. UNUSED TWISTED PAIR WIRES FROM CABLE (ITEM 6) SHALL BE SECURED TOGETHER SEPARATELY USING SLEEVING (ITEM 7) AS SHOWN FOR USE AS SPARES.

7. MAXIMUM UNTWIST FOR CABLE (ITEM 6) TWISTED PAIRS SHALL BE 25mm/1.0 INCH.

8. ASSEMBLE CONNECTORS (ITEM 9) TO PLATE (ITEM 12) OR ITEM 13, AS APPLICABLE), AS SHOWN. USING HARDWARE (ITEM 8).

9. APPROXIMATELY 254mm (10 INCHES) OF SLEEVING (ITEM 12) SHALL COVER CABLE (ITEM 6) TWISTED PAIRS AND EXTEND WITHIN DIMENSION SPECIFIED.

10. INSTALL BAR (ITEM 15) TO PLATE (ITEM 14) USING SCREWS (ITEM 16) AND WASHERS (ITEM 17 AND ITEM 18).

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11. FOR STRAIN RELIEF, SECURE WIRES USING CLAMP (ITEM 5) AS SHOWN.

12. INSTALL INDIVIDUAL LABELS WHERE SHOWN.

13. CABLE ASM SHALL MEET THE COMPLETED CABLE ASM REQUIREMENTS OF 58053700. INSTALL INDIVIDERAL LABELS AS SHOWN.

14. CABLE ASM QUALITY ASSURANCE PROVISIONS SHALL BE PER SECTION 4 OF 58053700.

15. INTERNAL CABLE ASM PREPARATION FOR DELIVERY SHALL BE PER SECTION 5 OF 58053700.

58082783

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 001	PL AL	DWG. SH. NO. 1	2	3	4	5	6
A	LEVEL 1 ISSUE	85	12	13	W. Bilcas	A	A	A	A	A	A	A	A
B	PHAØGE056	86	05	13	D. Williams	B	B						

F.C.F

FOR CONTINUATION OF REVISION STATUS SEE SHEET

BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

CE 300 A-3 (1-79)

MADE BY [illegible] 85FEB19

APPROVED [illegible]

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE INTERNAL BULKHEAD CABLE ASSEMBLY

SIZE	REVISION STATUS FOR	SHEET	REV
A	58082783	1/1	B

DIST. 71A

				001	
	1 C	43C175991P1	P CONNECTOR 88PIN	1	EA
	2 D	58035970-001	W COVER,CONN BRACKET	1	EA
	3 D	58016519-001	W SHIELD CONN	1	EA
	4 B	878B222P150	V SLEEVING	2	IN
	5 B	878B222P090	V SLVG SHRINKING	12	IN
	6 A	43A216152P15	V CABLE TWPR	40	IN
	7 B	878B222P060	V SLEEVING THERMO	3	IN
	8 B	43B138943P2	P SCREW LOCK ASM.	2	EA
	9 B	43B223079P18	W CONN SUB-MIN CR	2	EA
	10 B	43B223079P104	W SOCKET	42	EA
	11 C	43C142270P8	V CLAMP CABLE	4	EA
	12 A	43A167256P2	V WIRE MACH WRAP	36	IN
	13 B	58082841-002	A PLATE, BULKHEAD	1	EA
*	14 B	58082879-002	P CONNECTOR PLATE	2	EA
*	14 B	58082879-001	P CONNECTOR PLATE	INTCH	EA
	15 A	58060950-030	D LABEL	1	EA

INT BLKHD CABLE ASM

				001	
16	A	58041104-593	V SCREW,CR RECES, P HD	2	EA
17	A	58041134-580	V LOCKWASH SPR ST M	2	EA
18	A	58020396-005	W WASHER INSULATING	2	EA

REF. SPEC.

58053700

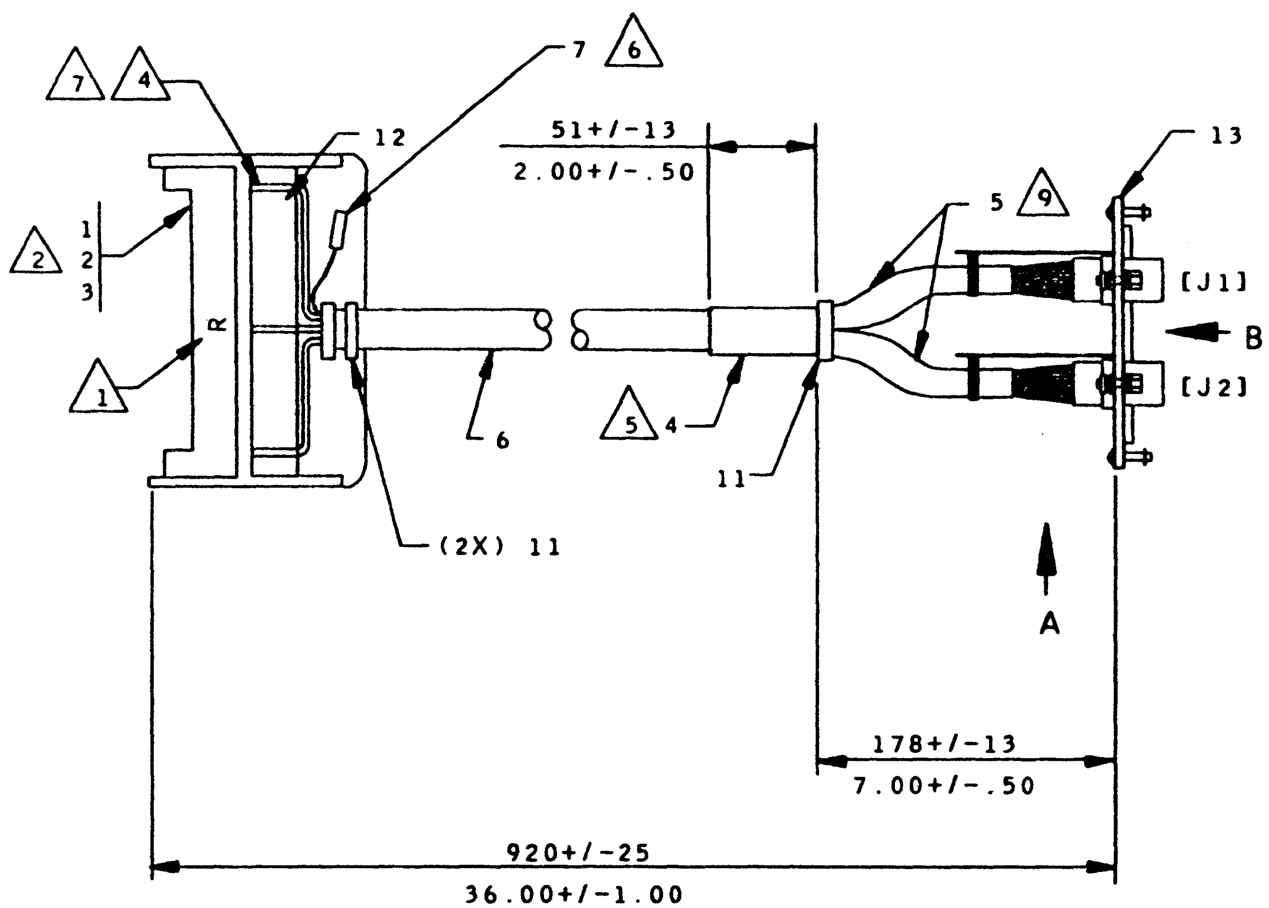
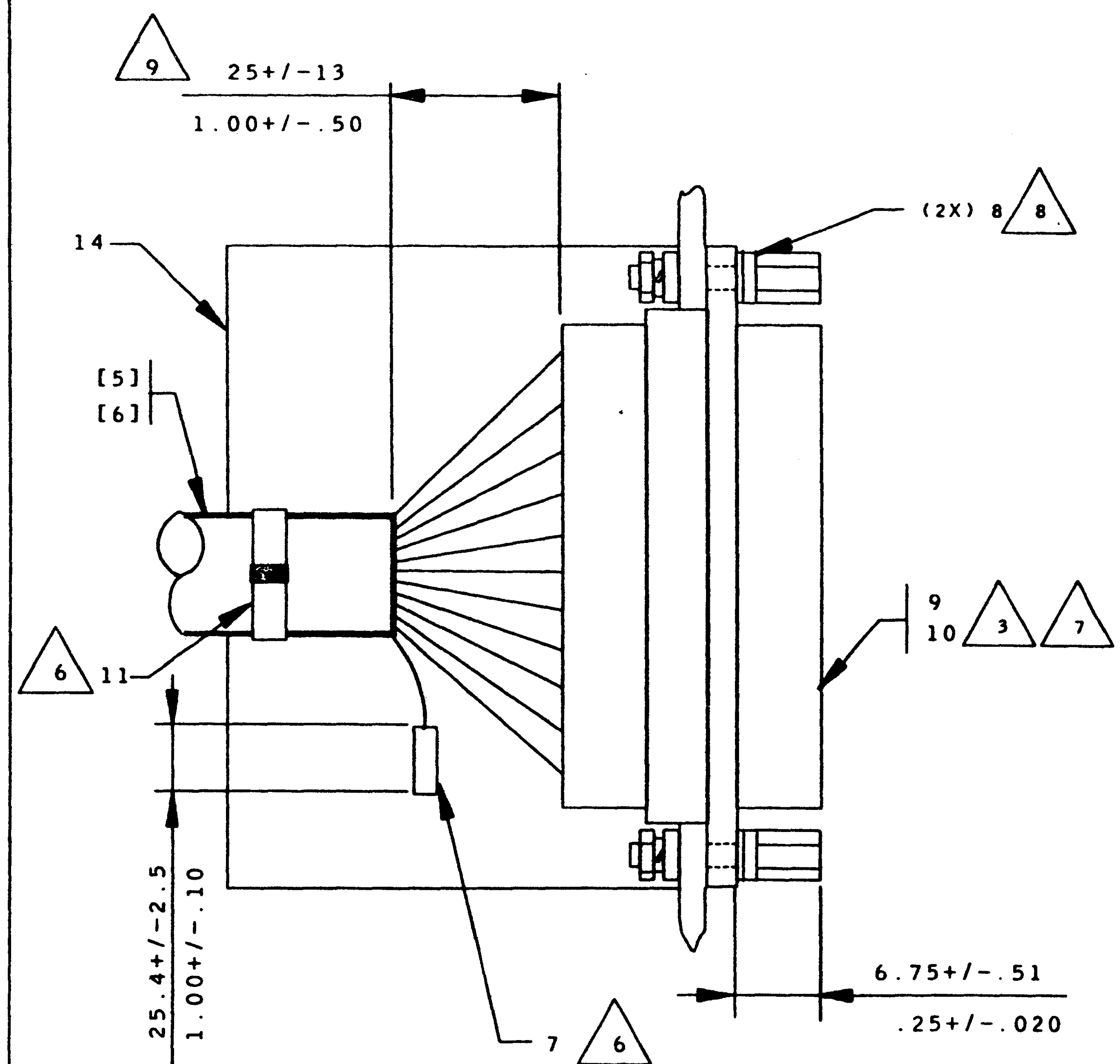


FIGURE 1, INTERNAL CABLE ASSEMBLY

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET.

UNLESS OTHERWISE SPECIFIED DIMENSIONS = MILLIMETERS / INCHES TOLERANCE OF SIZE AND FORM PER INITIAL DESIGN PROJECTION	MATL DSN Ted Gufford CHK FIN	HONEYWELL HONEYWELL INFORMATION SYSTEMS LOC PHOENIX, ARIZONA U.S.A. TITLE BULKHEAD HARNESS
SCALE NONE CODE FCF:	DR S. HARNAGEL 85AUG23 APPR	SIZE A | DWG NO. 58082783 | SH 1/6 | REV A

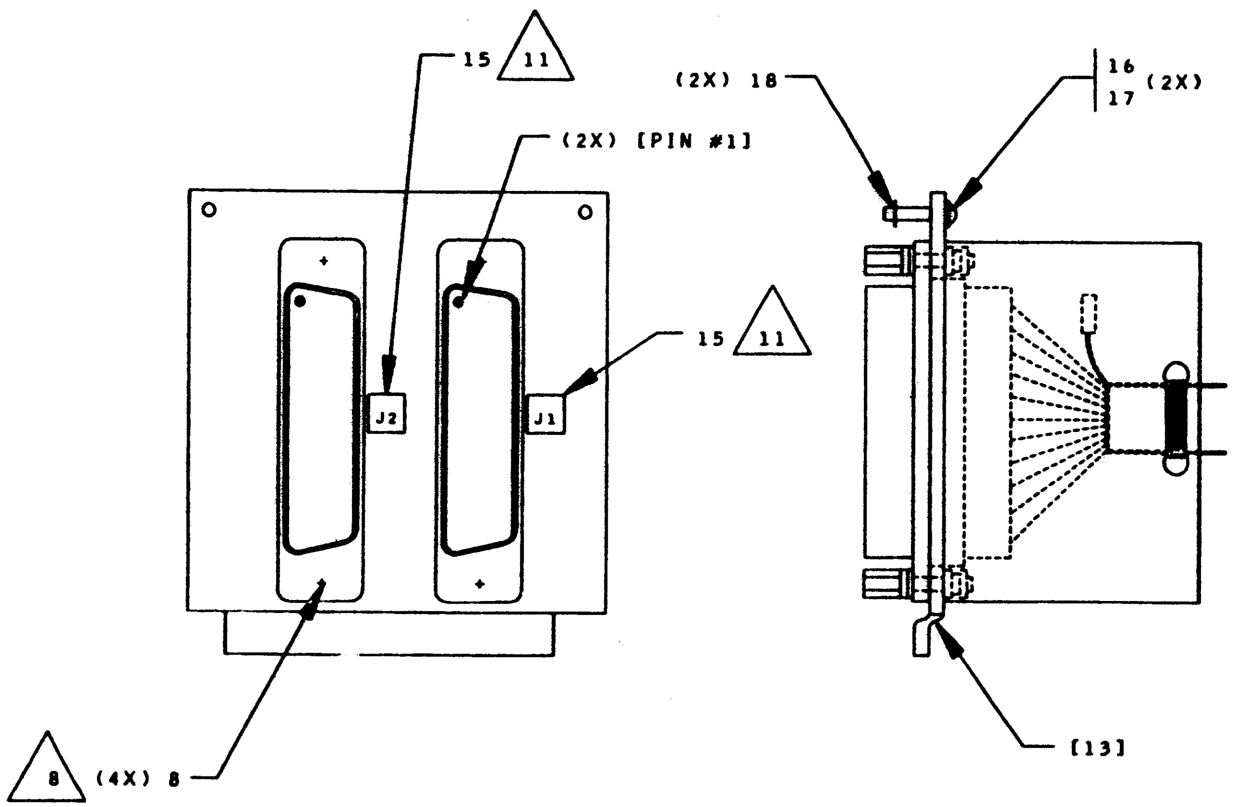
DISTR CODE: 71A



VIEW-A (2X)

Honeywell HONEYWELL INFORMATION SYSTEMS	SIZE A	DWG NO 58082783	SH 2	REV A

58082783



001

VIEW B

ROTATED 90° CLOCKWISE

58082783

TABLE I WIRE LIST 3 4

CONTROL		DATA	
TO	FROM	TO	FROM
RC00	J01 02	RA02	J02 02
RC06	20	RA00	20
RD07	03	RA05	03
RD06	21	RA08	21
RB21	04	RA13	04
RB17	22	RA17	22
RB12	05	RA14	05
RB11	23	RB01	23
RD14	06	RA03	06
RD10	24	RA01	24
RD00	07	RA11	07
RD02	25	RA09	25
RD09	08	RB10	08
RD11	26	RB13	26
RD16	09	RB18	09
RD20	27	RB16	27
RD21	10	RC19	10
RD17	28	RC17	J02 28
RC08	11	RA02	RA04
RC14	29	RA05	RA10
RC11	12	RA13	RA19
RC01	30	RA14	RA21
RC15	13	RA06	RA03
RC13	J01 31	RA11	RA15
		RB10	RB14
		RB18	RB20
		RC19	RC21

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NOTES:

1. MARK PER 58053700.

2. INSTALL SHIELDS (ITEM 2 AND ITEM 3) ONTO CONNECTOR (ITEM 1).

3. TERMINATE TWISTED PAIR WIRES OF CABLE (ITEM 6) TO CONTACTS (ITEM 10) AND CRIMP PER 58053700. INSTALL TERMINATED WIRES INTO CONNECTOR (ITEM 9) PER TABLE I WIRE LIST.

4. TWISTED PAIR WIRES OF CABLE (ITEM 6) SHALL BE FIRST LEVEL WIRE WRAPPED TO PINS OF CONNECTOR (ITEM 1) PER 58053700 USING TABLE I WIRE LIST. JUMPER WIRES (ITEM 12) ARE TO BE SECOND LEVEL WRAPPED.

5. MARK PER 58053700 AS AN UNLISTED UL LOGIC CABLE ASM USING DRAWING NUMBER, TAB NUMBER, AND REVISION LETTER AS THE ASM IDENTIFICATION.

6. UNUSED TWISTED PAIR WIRES FROM CABLE (ITEM 6) SHALL BE SECURED TOGETHER SEPARATELY USING SLEEVING (ITEM 7) AS SHOWN FOR USE AS SPARES.

7. MAXIMUM UNTWIST FOR CABLE (ITEM 6) TWISTED PAIRS SHALL BE 25mm/1.0 INCH.

8. ASSEMBLE CONNECTOR (ITEM 9) AND STRAIN RELIEF (ITEM 14) TO PLATE (ITEM 13) AS SHOWN, USING HARDWARE (ITEM 8).

9. APPROXIMATELY 203mm (8 INCHES) OF SLEEVING (ITEM 5) SHALL COVER CABLE (ITEM 6) TWISTED PAIRS AND EXTEND WITHIN DIMENISION SPECIFIED.

10. FOR STRAIN RELIEF, SECURE WIRES USING CLAMP (ITEM 11) AS SHOWN.

11. INSTALL INDIVIDERAL LABELS WHERE SHOWN.

12. CABLE ASM SHALL MEET THE COMPLETED CABLE ASM REQUIREMENTS OF 58053700.

13. CABLE ASM QUALITY ASSURANCE PROVISIONS SHALL BE PER SECTION 4 OF 58053700.

14. INTERNAL CABLE ASM PREPARATION FOR DELIVERY SHALL BE PER SCCTION 5 OF 58053700.

58081329

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB.NO. 001	TAB.NO. 002	PL ALL	DWG.SH.NO 1
A	LEVEL 1 ISSUE	83	07	25	RBeul 7/19/83	A	A	A	A
B	PHAO NJ016	83	10	05	S. Miller	B	B		B

FCF: 58081328

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX, ARIZONA

MADE BY R. Hoekstra 83 Mar 18

APPROVED L.G. Roehlke 6/30/83

REVISION STATUS FOR EACH PAGE, SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE JUMPER, BACKPANEL

SIZE	REVISION STATUS FOR	SHEET	REV
B	58081329	1/1	B

DIST. C120-3 C125-3

BRUNING 44-141 40366

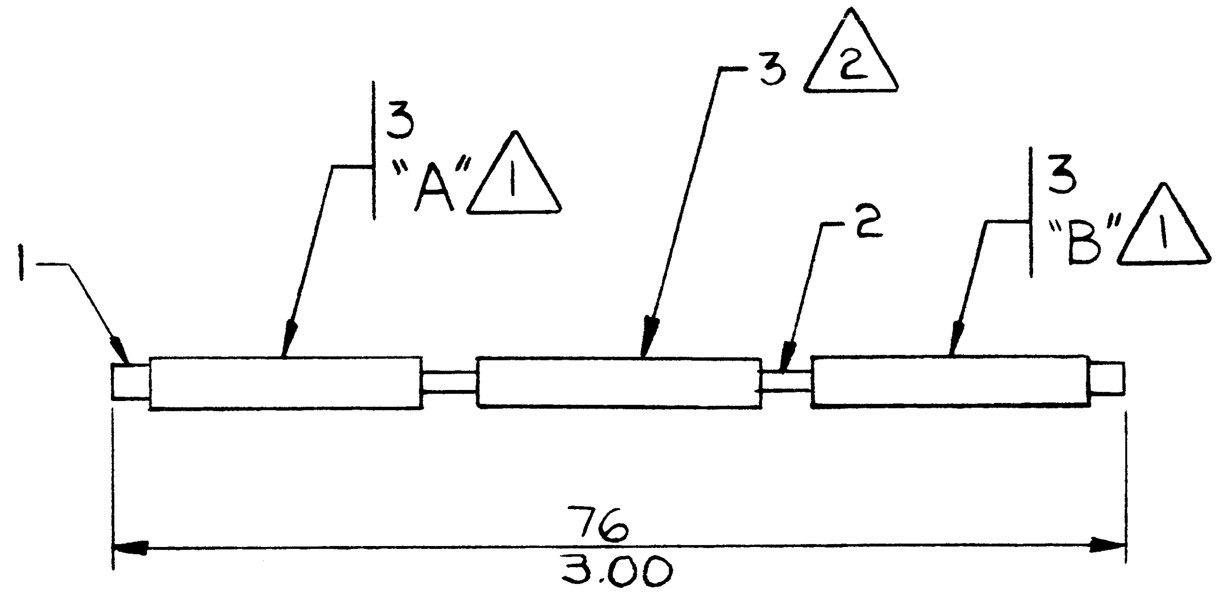
CE 300 A-3 (1-79)

					001	002	
*	1	B	43B216106P1	V MINI TERMINAL	2	2	EA
*	2	A	43A167218P069	V WIRE	3	3	IN
*	3	B	878B222P060	V SLEEVING THERMO	3	3	IN

JUMPER, BACKPANEL

5808 329

REVISION			
REV	AUTHORITY	DATE (YR MO DAY)	SIGNATURE



MARKING TABLE		
TAB NO	"A"	"B"
001	WH02	WH11
002	WH03	WG21

△2. MARK PER 43A144110 AS AN UNLISTED CABLE.

1. MARK AS SHOWN PER MARKING TABLE PER 43A226458, CLASS C.

NOTES:

43A226458

REF SPEC NO

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

UNLESS OTHERWISE SPECIFIED	MATL	Honeywell
DIMENSIONS= MILLIMETERS / INCHES		HONEYWELL INFORMATION SYSTEMS
TOLERANCE OF SIZE AND FORM PER	TREAT.	LOC PHOENIX, ARIZONA U. S. A.
INITIAL DESIGN PROJECTION	FIN.	TITLE JUMPER, BACKPANEL
SCALE / CODE	DR [illegible] 83 Jun	SIZE B / DWG NO 58081329 / SH 1/1 / REV B
	APPD [illegible] 83	
	DISTR C125-3, C120-3	

58059979

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	DWG SHEET NUMBER 1	2
A	LEVEL 3 ISSUE	82	09	01	J.M. Boyle 8-30-82	A	A
B	PHAØNJ015	83	07	27	T. Inouye	B	B
C	PHAØRH431	84	09	07	G. Drenth	C	C
D	PHAØNJ037	85	01	18	G. Drenth		D

FCF: NDAU001A

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY C.H. Bentley 82 Aug 13

APPROVED L.G. Roehlke 8/20/82

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CABLE CONFIGURATOR PPW

SIZE	REVISION STATUS FOR	SHEET	REV
B	58059979	1/1	D

DIST. 73

BRUNING 44-141 40366

CE 300 A-3 (1-79)

58059979

REV	AUTHORITY	DATE (YR MO DAY)	SIGNATURE

△3. CABLE LENGTH DESIGNATED BY XXX REFERS TO LENGTH IN METERS (M) OR FEET (F) AS SPECIFIED ON CABLE DRAWING.

△2. QUANTITY OF CABLES DESIGNATED ADJACENT TO THE OPTION MODEL NUMBER MUST BE ORDERED BASED ON THE NUMBER OF DEVICES WHICH INTERFACE WITH THE OPTION.

1. THE PURPOSE OF THIS DOCUMENT IS TO PROVIDE EXTERNAL CABLE DATA TO BE USED IN CONJUNCTION WITH CUSTOMER SITE LAYOUTS FOR ESTABLISHING CABLE LENGTH REQUIREMENTS BETWEEN EQUIPMENT AND TO CREATE A SYSTEM INSTALLATION PARTS LIST IPL FOR ORDERING EXTERNAL SYSTEM CABLES.

~~△5 DAU INTERFACE JUMPER INTERFACE ONE MODULE. USED FOR SHORT CABLING BETWEEN ADJACENT DAU BULK HEADS.~~

~~△4 QUANTITY OF CABLES DEPENDS ON THE TYPE OF SYSTEM CONFIGRATION (NUMBER OF IPC MAD'S AND DAU'S INTERFACED) TOTAL COMBINED LENGTH OF CABLES BETWEEN IPC MAD'S AND DAU'S SHALL NOT EXCEED 91.4 METERS (300 FEET).~~

NOTES:

FOR DOCUMENT STATUS SEE REVISION STATUS SHEET.

UNLESS OTHERWISE SPECIFIED DIMENSIONS = MILLIMETERS / INCHES; TOLERANCE OF SIZE AND FORM PER; INITIAL DESIGN; PROJECTION	MATL	**Honeywell** HONEYWELL INFORMATION SYSTEMS	
	DES. [signature]	LOC PHOENIX, ARIZONA U.S.A.	
	CHK. [signature]	TITLE CABLE CONFIGURATOR PPU	
	FIN		
SCALE / CODE	DR [signature] 82AUG13	SIZE B	DWG NO 58059979 / SH 1/2 / REV C
	APPD J.C. Roehlke 8/20/82		
	DISTR 73		

REF SPEC NO

CE 300 B (12 71) BRUNING 44 141 31362-4

58059979

REVISION				
REV	AUTHORITY	DATE YR MO DAY	SIGNATURE	

PRIME UNIT	CABLE			PRIME UNIT STUB-OUT LENGTH FROM FLOOR UP		TOTAL CABLE LENGTH				SECONDARY UNIT STUB-OUT LENGTH FROM FLOOR UP		SECONDARY UNIT	
OPTION MODEL NUMBER	QTY (2)	DRAWING NUMBER	M/F (3)	METERS	FEET	MIN LENGTH METERS	MIN LENGTH FEET	MAX LENGTH METERS	MAX LENGTH FEET	METERS	FEET	OPTION MODEL NUMBER	DEVICE
WDAU66LA	2	58034110-XXX 58081041-XXX	M	1.52	5	9	29.5	22	72.2	.61	2		4XX DISK DRIVE 50X DISK DRIVE
WDAU66LB	2	58034110-XXX 58081041-XXX	M	1.52	5	9	29.5	22	72.2	.61	2		4XX DISK DRIVE 50X DISK DRIVE
WDDI66LA	2	58034110-XXX 58081041-XXX	M	1.52	5	9	29.5	22	72.2	.61	2		4XX DISK DRIVE 50X DISK DRIVE
WADE66LA	2	58081041-XXX	M	1.52	5	9	29.5	22	72.2	1.52	5		MTU070X MTU0410 MTU050X MTU060X MTU061X MTU063X

REF SPEC NO

UNLESS OTHERWISE SPECIFIED DIMENSIONS= MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN
PROJECTION
SCALE CODE

MATL
DES C.W. Bentley
CHK WALTER L. [illegible]
FIN.
DR C.W. Bentley 82 Aug 12
APPD L.G. Roehlke 8/20/82
DISTR

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC PHOENIX, ARIZONA U. S. A.
TITLE CABLE CONFIGURATOR PPU
SIZE B | DWG NO 58059979 | SH 2F | REV D

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE
A	LEVEL 1 ISSUE	85	11	11	[illegible]
B	PHAØPNQ84	86	02	05	C. Ripley 86/1/20

PRIME UNIT OPTION MODEL NUMBER	CABLE QTY △2	CABLE DRAWING NUMBER	M/F △3	PRIME UNIT STUB-OUT LENGTH FROM FLOOR UP METERS	FEET	TOTAL CABLE LENGTH MIN LENGTH METERS	FEET	MAX LENGTH METERS	FEET	SECONDARY UNIT STUB-OUT LENGTH FROM FLOOR UP METERS	FEET	SECONDARY UNIT OPTION MODEL NUMBER	DEVICE
WDAU66LC	2	58082960-XXX 58082959-XXX	M	1.52	5	9	29.5	23	75	.61	2		4XX DISK DRIVE 50X DISK DRIVE
WDAU66LD	2	58082960-XXX 58082959-XXX	M	1.52	5	9	29.5	23	75	.61	2		4XX DISK DRIVE 50X DISK DRIVE
WDDI66LB	2	58082960-XXX 58082959-XXX	M	1.52	5	9	29.5	23	75	.61	2		4XX DISK DRIVE 50X DISK DRIVE
WADE66LB	2	58082959-XXX	M	1.52	5	9	29.5	23	75	1.52	5		MTU070X MTU0410 MTU050X MTU060X MTU061X MTU063X
WURP66LA	2	58082959-XXX	M	1.52	5	9	29.5	23	75				PRU1200 PRU1600 PCU0120 PCU0121 CCU0401 CRU0501 CRU1050
WUDI66LA	2	58082959-XXX	M	1.52	5	9	29.5	23	75				

△ 3. CABLE LENGTH DISIGNATED BY XXX REFERS TO LENGTH IN METERS (M) OR FEET (F) AS SPECIFIED ON CABLE DRAWING.

△ 2. QUANTITY OF CABLES DESIGNATED ADJACENT TO THE OPTION MODEL NUMBER MUST BE ORDERED BASED ON THE NUMBER OF DEVICES WHICH INTERFACE WITH OPTION.

1. THE PURPOSE OF THIS DOCUMENT IS TO PROVIDE EXTERNAL CABLE DATA TO BE USED IN CONJUNCTION WITH CUSTOMER SITE LAYOUTS FOR ESTABLISHING CABLE LENGTH REQUIREMENTS BETWEEN EQUIPMENT AND TO CREATE A SYSTEM INSTALLATION PARTS LIST IPL FOR ORDERING EXTERNAL SYSTEM CABLES.

NOTES:

58082829

REF SPEC NO

UNLESS OTHERWISE SPECIFIED
DIMENSIONS= MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN
PROJECTION

MATL

DES:
CHK: [illegible] 85 OCT 28
FIN.

SCALE NONE
CODE

DR C. Ripley
APPD L.G. Rochlle 10/28/85
DISTR 73

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC PHOENIX, ARIZONA U. S. A.
TITLE CABLE CONFIGURATOR PPU (SHIELDED)

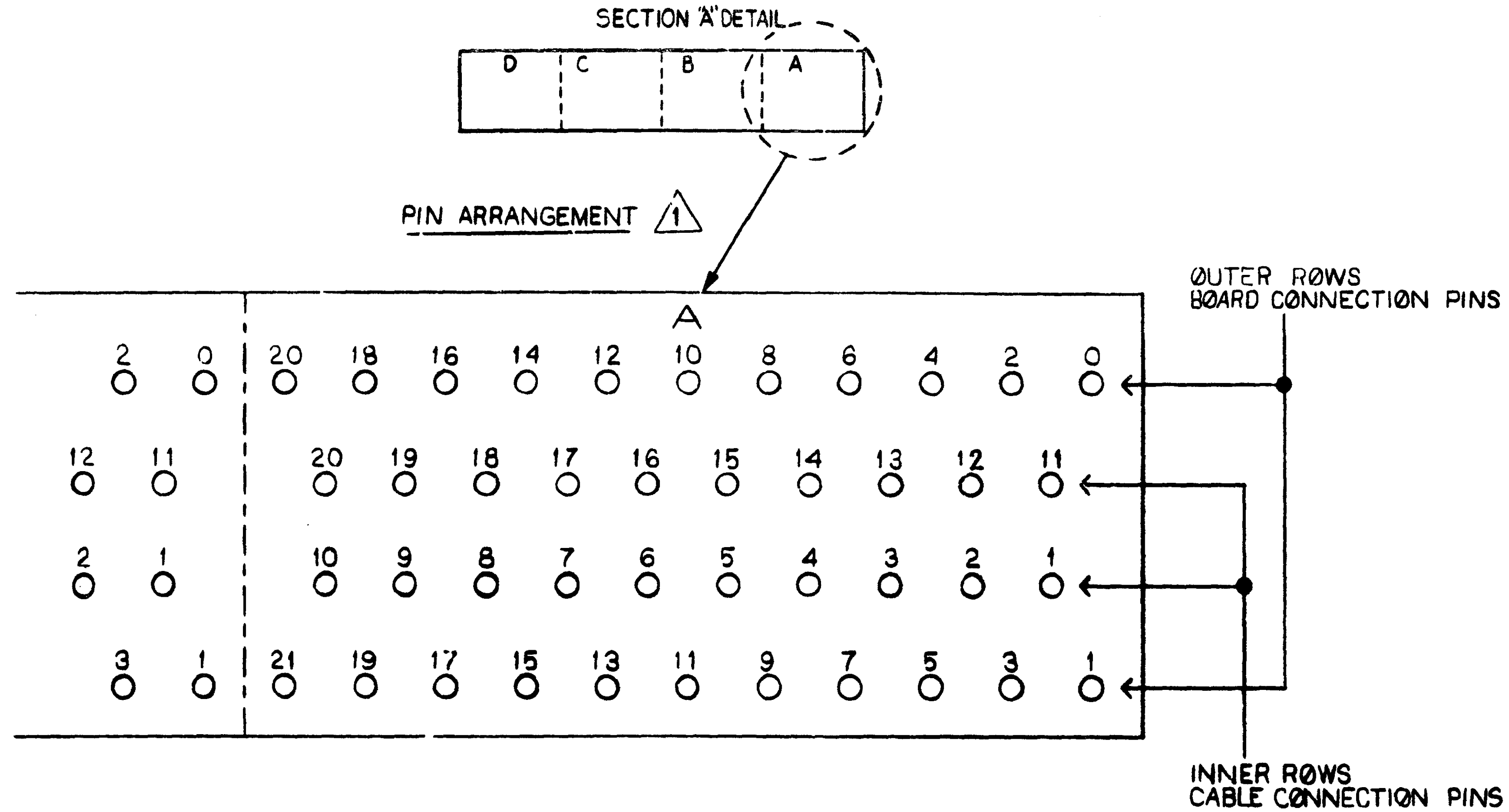
SIZE	DWG NO	SH	REV
C	58082829	1/1	B

MICROFICHE INDEX
MODULE MANUAL
DEVICE ADAPTER UNIT WDAU66LA/LC

REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE
A	LEVEL 3 ISSUE	79	8	05	S.E. Str...
B	PHAØPV313	82	JAN	15	Efren Araujo

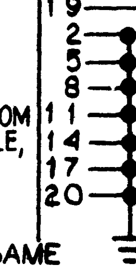
SECTION 'A' DETAIL

PIN ARRANGEMENT ⚠1



PIN CØNNECTIØN LIST ⚠1

PIN NØ. ØUTER RØWS	PIN NØ. INNER RØWS
0	20
1	9
3	10
4	7
6	6
7	18
9	4
10	17
12	15
13	3
15	1
16	14
18	12
19	11
2	2
5	5
8	8
11	13
14	16
17	19
20	



NØTES:

⚠1. SECTIØNS A, B, C & D HAVE THE SAME PIN INTERCØNNECTIØN & ARRANGEMENTS.

2. REFERENCE ONLY: SCHEMATIC MADE FROM WIRE LISTS, 43A229856 MTC 500 DLI CABLE, 43A243630 MPCMX CABLE, 43A229761 DLI CABLE, & 58018104 LSMX CABLE.

REF SPEC NO
43A229856
43A243630
43A229761
58018104

UNLESS OTHERWISE SPECIFIED DIMENSIONS= MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN
PROJECTION
SCALE | CODE

MATL | TREAT. | FIN.

DR Melodie Abel 26 July '79
S.E. Strode 79-09-28
APPD R.J. Abraham 79/09/20
DISTR C106-10

Honeywell
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

TITLE SCHEMATIC DIAGRAM FE/CABLE ADP BD

SIZE	DWG NO	SH	REV
C	58051465	1/1	B

58051465

CE 300 C (12-71)

58059634

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	ASSEMBLY TAB 001	101	202	102	702	802	PL ALL	DRAWING SHEET 1
A	LEVEL I ISSUE	82	01	18	12-21-81 [illegible]	A	A					A	A
B	PHAOXS094	82	06	16	S. Miller	B	B					B	B
C	PHAOSR154	83	03	10	G Drenth	C	C					C	
D	PHAONJ016	83	10	05	G Drenth		D					D	D
D1	ENXS149		ND		G Drenth	D1	D1						
E	PHAOXS365	84	JAN	04	G Drenth	E	E	E	E			E	E
F	PHAONJ027	84	JAN	13	G Drenth	OBSOLETE	OBSOLETE	F	F	F		F	
G	PHAONJ030	84	JUN	11	G Drenth			G		G	G	G	

ECF

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY S. Jensen 11 DEC 81

APPROVED C.E. Wilcox 12/17/81

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE DAU PANEL ASSEMBLY

SIZE	REVISION STATUS FOR	SHEET	REV
C	58059634	1/1	G

DIST. 3

BRUNING 44-141 40366

CE 300 A-3 (1-79)

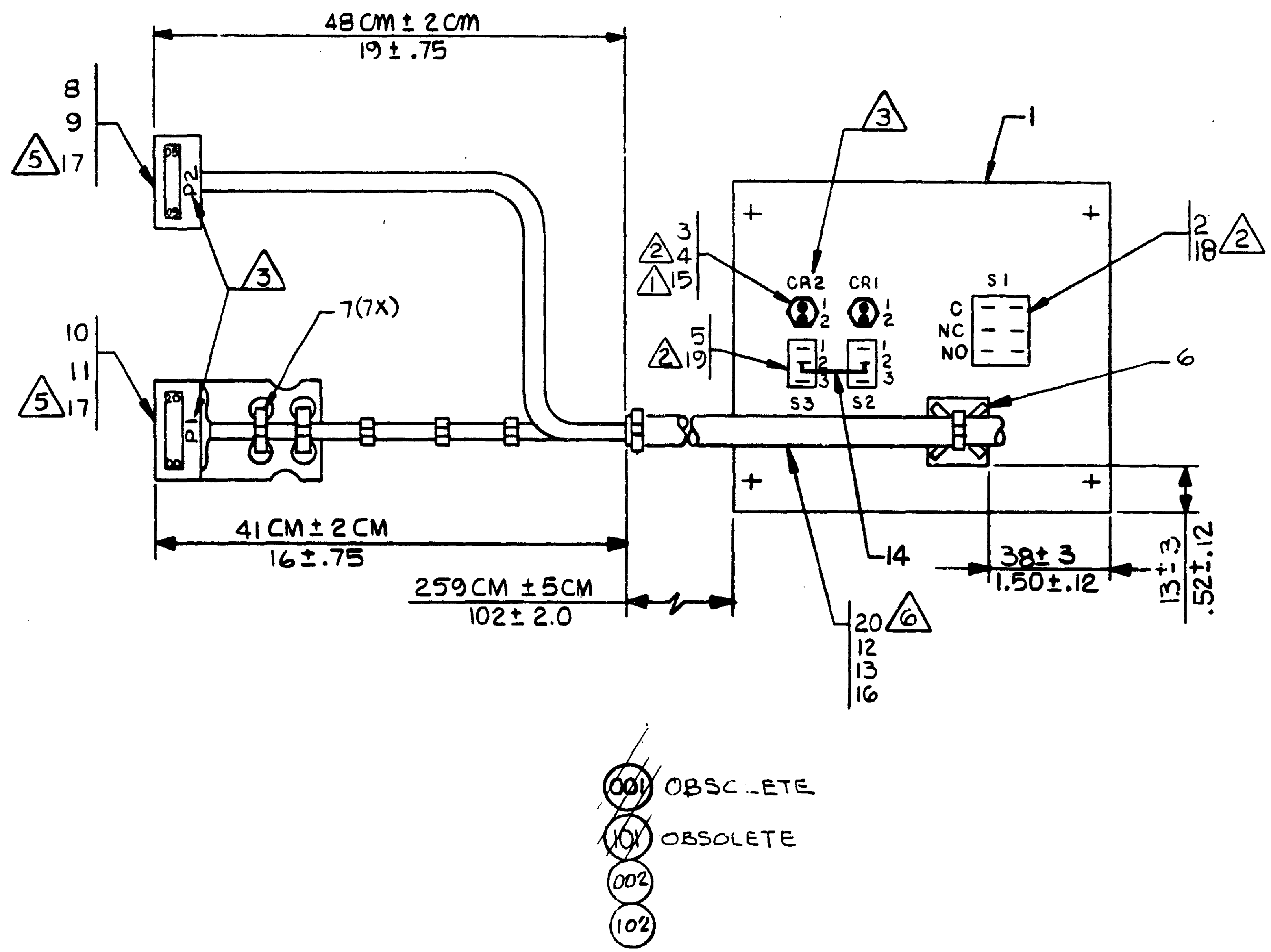
PD 84/06/12 C 58059634 1/2 G

				002	102	702	802	
1	C	58059633-001	P DAU CONFIG PANEL	1				EA
2	B	8768219P8	V SWITCH PB	1				EA
3	A	58020206-001	V DIODE,LIGHT EMIT,RED	2				EA
4	A	58000076-002	P HOLDER LED	2				EA
5	A	58008225-004	V SWITCH MIN TOGGLE	2				EA
6	C	43C142270P52	V CLAMP CABLE	1				EA
7	C	43C142270P8	V CLAMP CABLE		7			EA
8	B	43B166701P67	V DECAL			1		EA
9	B	43B216136P1	V HOUSING MINI			1		EA
10	B	58028255-002	A ID CONNECTOR			1		EA
11	B	43B166701P4	V DECAL			1		EA
12	A	43A180043P209	V WIRE PAIR TWIST			245		IN
13	A	43A167218P029	V WIRE			480	3	IN
14	B	43B111126P15	V WIRE BARE SOLID	3				IN
15	B	873B126P40	V SLEEVING ELEC	2				IN
16	A	58008294-001	V SLEEVING ZIPPER			100		IN

DAU PNL ASM

C 58059634 1/2 G

				002	102	702	802	
17	B	43B216106P1	V MINI TERMINAL			14		EA
18	B	876B219P1101	V GUARD, BUTTON	1				EA
19	B	43B175995P4	V CAP PLASTIC	2				EA
20	C	58059634-102	A DAU PNL WIRING	1				EA
21	A	58057946-002	D W.L.MAIN PNL	X	X	X		
22	C	58059634-702	A DAU PNL ASM		1			EA
* 23	C	58059634-802	A DAU PNL ASM	1				EA



6. MARK PER 43A144110 AS AN UNLISTED HARNESS.

5. INSTALL MINI TERMINAL IN CORNER AND END CAVITIES TO INCREASE CONNECTOR RETENTION.

4. CORRECT HARNESS LENGTHS, CABLE CLAMPS OR TIES AND ROUTING TO BE ESTABLISHED BY MANUFACTURING.

3. MARK PER 43A226458 CLASS C.

2. ASSEMBLE PER 43A232701 FIG 15, 19A AND 30.

1. SHRINK SLEEVING ON ALL DIODES.

NOTES:

REVISIONS					
REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

REF SPEC NO
43A144110
43A226458
43A232701

UNLESS OTHERWISE SPECIFIED
DIMENSIONS = MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN M
PROJECTION
CODE

MATL
DES. [signature] 21 Dec 81
CHK.
FIN.
DR W [signature] 81 NOV 12
APPD C. E. Wilcox 12/17/81
DISTR C120-3 C125-3

Honeywell
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U. S. A.
LOC
TITLE DAU PANEL ASSEMBLY
FCF

SIZE	DWG NO	SH	REV
C	58059634	1/1	E

58059634

CE 300 C (12-73)

58057946

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB'S 001	002	SHEETS 1
A	LEVEL 3 ISSUE	81	NOV	19	11/17/81	A		A
B	PHAØXS044	81	DEC	15		B		B
C	PHAØXS289	83	SEP	21	G Drenth	C		C
D	PHAØXS365	84	JAN	03	G Drenth	D	D	D

OBSOLETE

STD: 58037000

FCF: FMF: DIPPER

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY DAPS 81 OCT 6

APPROVED 11-6-81

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE WIRE LIST MAIN-PANEL

SIZE	REVISION STATUS FOR	SHEET	REV
A	58057946	1/1	D

DIST. CAB, C125-C130-13A

DRAWING 44-141 40365

CE 300 A-3 (1-79)

WIRE LIST
MAIN-PANEL

TAB	SEQ	FROM	TO	TY	CL	TM	LOGIC	RV	BK
002	0001	S2-2	S3-2	KK	--	NN	GND		
002	0002	CR1-1	CR2-1	AM	99	NN	+5V	C	
002	0003	CR1-1	P203	FM	00	NL	+5V	B	TP
002	0004	S2-2	P211	FM	99	NL	GND	D	TP
002	0005	CR1-2	P112	AM	99	NL	IF0-ON-LED*000	C	
002	0006	CR2-2	P113	AM	99	NL	IF1-ON-LED*000	C	
002	0007	S2-3	P106	AM	99	NL	IF0-ON-LINE*000	C	
002	0008	S3-3	P107	AM	99	NL	IF1-ON-LINE*000	C	
002	0009	S1-NO	P119	FM	00	NL	SWITCH-RESET*000	B	TP
002	0020	S1-C	P121	FM	99	NL	SWITCH-RESET*000GND	B	TP

THE INFORMATION CONTAINED IN THIS DOCUMENT PROPRIETARY TO HONEYWELL INFORMATION SYSTEMS, INC. AND IS INTENDED FOR INTERNAL HONEYWELL USE ONLY. SUCH INFORMATION MAY BE DISTRIBUTED TO OTHERS BY WRITTEN PERMISSION OF AN AUTHORIZED HONEYWELL OFFICIAL. THIS RESTRICTION DOES NOT APPLY TO VENDOR PROPRIETARY THAT MAY BE DISCLOSED IN THIS DOCUMENT.

58028075

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB 001	SHEETS 1	2	3	-	5F
A	LEVEL / ISSUE	77	FEB	03	J. Michelson	A	A	A	A	A	A

FMF WCH0038F FCF LATER

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS

LOC PHOENIX, ARIZONA

MADE BY EDP 77 JAN 31

APPROVED R E Sauer 77 Feb 2

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE WIRE LIST PSI FREE EDGE TO FREE EDGE CABLE

SIZE	REVISION STATUS FOR	SHEET	REV
A	58028075	1/1	A

CE 380 A-3 (12-71) BRUNING 44-141 DIST CODE L22-12 TØS NCØ

1) TYPE (WIRE TYPE : WIRE SIZE)
WIRE TYPE (SEE P.D.B. 7.2.1 FOR PREFERRED SIZES)

CODE	DESCRIPTION	DWG. OR IDENT.
A ------	1/C STRANDED	43A167218
B ------	1/C SOLID	43A167218
C ------	1/C 600V STRANDED	43A167219
D ------	1/C 600V SOLID	43A167219
E ------	TW. PR. STRANDED	43A162530
F ------	SHLD. TW. PR. STRND	878B247
G ------	TENDRIL WIRE	
H ------	TW. TRIPLE STRND	12A8267
J ------	JUMPER	43A114946
K ------	1/C SHLD STRND	43B135641
L ------	(RESERVED)	
M ------	BARE SOLID	43B111126
N ------	TW. PR.	43A180043
P ------	WIRE WRAP G/D #24	43A127043
Q ------	KYNAR TW. PR. SOLID	43A175958
R ------	WIRE WRAP G/D #30	43A167256
S ------	1/C SHLD STRND	878B285
T ------	CABLE STRAP	43B228384
U ------	JUMPER	43A108800
V ------	A. C. 3 COND. WIRE	12A8230
W ------	BUSS-BAR JUMPER	43B111125
X ------	30 AWG RIBBON CABLE	58005026
Y ------	27 AWG RIBBON CABLE	58005027
Z ------	75 OHM COAXIAL CABLE	58000062

WIRE SIZE

CODE	GAGE (AWG)
A -----	4
B -----	6
C -----	8 (LO)
D -----	10 (LO)
E -----	12 (LO)
F -----	14
G -----	16
H -----	18
J -----	20
K -----	22
L -----	24
M -----	26
N -----	28
P -----	(NONE)
Q -----	30
R -----	8 (HIGH)
S -----	10 (HIGH)
T -----	12 (HIGH)

I PIN CODING AS FOLLOWS - 0A - UPPER CASE A
I AA - UPPER CASE AA
I 1A - LOWER CASE A
I 2A - LOWER CASE AA

NOTE:
ON TWISTED PAIR WIRING, THE LIGHTER COLOR WIRE IS THE GROUND WIRE, DARKER WIRE THE SIGNAL.

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

2) COLOR CODE (WIRE COLOR : TRACER COLOR)

CODE	COLOR
0	BLACK
1	BROWN
2	RED
3	ORANGE
4	YELLOW
5	GREEN
6	BLUE
7	PURPLE
8	GRAY
9	WHITE
-	NONE SPECIFIED

3) TERMINATIONS (FROM END : TO END)

TYPE

A -------	SOLDERLESS
B -------	43C140824P1,P3,P5
C -------	43C140824P2,P4,P5
D -------	43C140847P1 OR 43C140824P1,P3,P5,P7
E -------	TEMP SENSER 43A216171
F -------	FASTON
G -------	(RESERVED)
H -------	WIRE-WRAPPED
J -------	CONTACT
K -------	SPLICE
L -------	CRIMPED CONTACT (BERG) 43B216106
M -------	43C140824P2,P4,P5,P7
N -------	SOLDER
P -------	(RESERVED)
Q -------	STRIP-CRIMP LATER
R -------	STRIP-TIN
S -------	FERRULE
T -------	WIRE-WRAPPED & SOLDER
U -------	43B112143
V -------	(RESERVED)
W -------	43D140854P2
X -------	43D140854P1
Y -------	43D140854P3
Z -------	43D140854P4

WIRE LIST
PSI FREE EDGE TO FREE EDGE CABLE

TAB	SEQ	FROM	TO	TY	CL	TM	LOGIC	RV	BK
001	0001	P1-A02	P1-A04	RQ	66	HH	*PS-DATA-0;100		JJ
001	0002	P1-A05	P1-A10	RQ	66	HH	*PS-DATA-1;100		JJ
001	0003	P1-A13	P1-A19	RQ	66	HH	*PS-DATA-2;100		JJ
001	0004	P1-A14	P1-A21	RQ	66	HH	*PS-DATA-3;100		JJ
001	0005	P1-A03	P1-A06	RQ	66	HH	*PS-DATA-4;100		JJ
001	0006	P1-A11	P1-A15	RQ	66	HH	*PS-DATA-5;100		JJ
001	0007	P1-B10	P1-B14	RQ	66	HH	*PS-DATA-6;100		JJ
001	0008	P1-B18	P1-B20	RQ	66	HH	*PS-DATA-7;100		JJ
001	0009	P1-C19	P1-C21	RQ	66	HH	*PS-DATA-PRTY;100		JJ
001	0010	P2-A02	P2-A04	RQ	66	HH			JJ
001	0011	P2-A10	P2-A05	RQ	66	HH			JJ
001	0012	P2-A19	P2-A13	RQ	66	HH			JJ
001	0013	P2-A21	P2-A14	RQ	66	HH			JJ
001	0014	P2-A03	P2-A06	RQ	66	HH			JJ
001	0015	P2-A11	P2-A15	RQ	66	HH			JJ
001	0016	P2-B10	P2-B14	RQ	66	HH			JJ
001	0017	P2-B18	P2-B20	RQ	66	HH			JJ
001	0018	P2-C19	P2-C21	RQ	66	HH			JJ
001		CABLE #1							
001	0019	P1-A02	P2-A02	XQ	66	HH	*PS-DATA-0;100		TP
001	0020	P1-A00	P2-A00	XQ	44	HH	*PS-DATA-0;100GN		TP
001	0021	P1-A10	P2-A10	XQ	66	HH	*PS-DATA-1;100		TP
001	0022	P1-A08	P2-A08	XQ	44	HH	*PS-DATA-1;100GN		TP
001	0023	P1-A19	P2-A19	XQ	66	HH	*PS-DATA-2;100		TP
001	0024	P1-A17	P2-A17	XQ	44	HH	*PS-DATA-2;100GN		TP
001	0025	P1-A21	P2-A21	XQ	66	HH	*PS-DATA-3;100		TP
001	0026	P1-B01	P2-B01	XQ	44	HH	*PS-DATA-3;100GN		TP
001	0027	P1-A03	P2-A03	XQ	66	HH	*PS-DATA-4;100		TP
001	0028	P1-A01	P2-A01	XQ	44	HH	*PS-DATA-4;100GN		TP
001	0029	P1-A11	P2-A11	XQ	66	HH	*PS-DATA-5;100		TP
001	0030	P1-A09	P2-A09	XQ	44	HH	*PS-DATA-5;100GN		TP
001	0031	P1-B10	P2-B10	XQ	66	HH	*PS-DATA-6;100		TP
001	0032	P1-B12	P2-B11	XQ	44	HH	*PS-DATA-6;100GN		TP
001	0033	P1-B18	P2-B18	XQ	66	HH	*PS-DATA-7;100		TP
001	0034	P1-B16	P2-B16	XQ	44	HH	*PS-DATA-7;100GN		TP

WIRE LIST
PSI FREE EDGE TO FREE EDGE CABLE

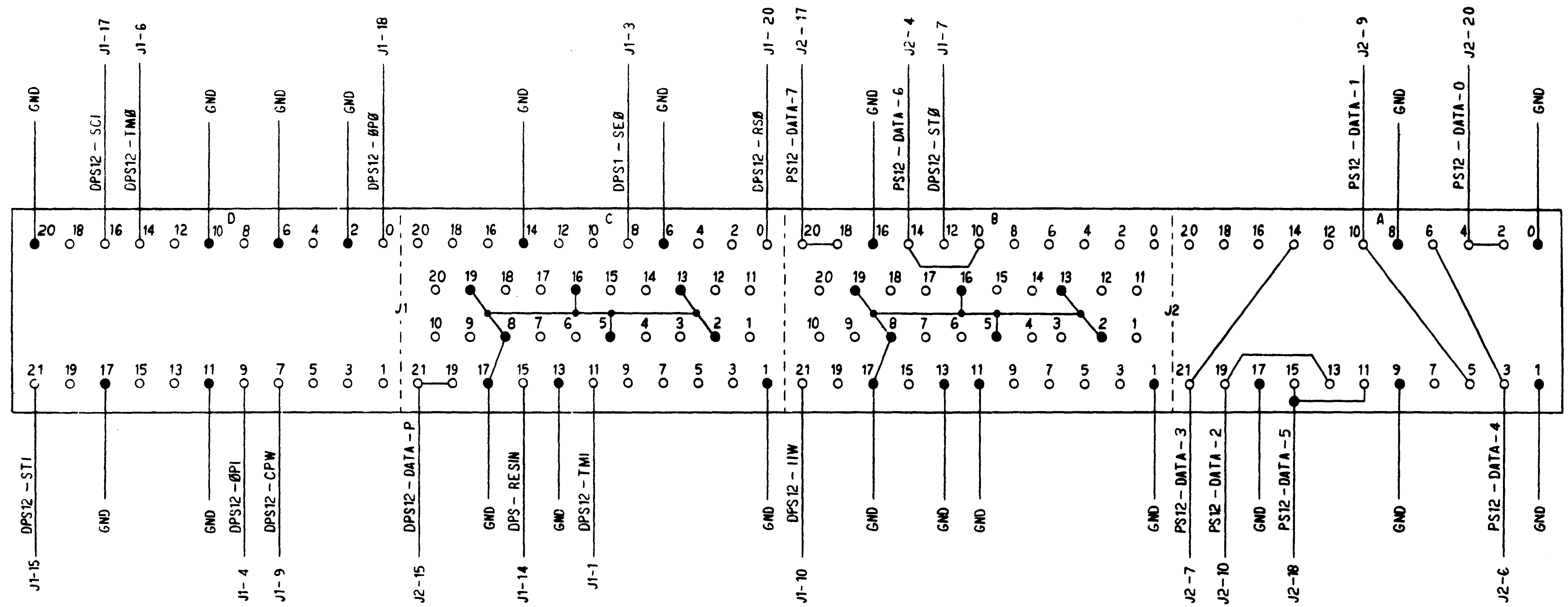
TAB	SEQ	FROM	TO	TY	CL	TM	LOGIC	RV	BK
001	0035	P1-C19	P2-C19	XQ	66	HH	*PS-DATA-8;100		TP
001	0036	P1-C17	P2-C17	XQ	44	HH	*PS-DATA-8;100GN		TP
001	0037	P1-B11	P2-C00	XQ	66	HH	*PS-RSO;100		TP
001	0038	P1-B13	P2-C01	XQ	44	HH	*PS-RSO;100GN		TP
001	0039	P1-B19	P2-D07	XQ	66	HH	*PS-CPW;100		TP
001	0040	P1-B17	P2-D06	XQ	44	HH	*PS-CPW;100GN		TP
001	0041	P1-C15	P2-B21	XQ	66	HH	*PS-IIW;100		TP
001	0042	P1-C14	P2-B17	XQ	44	HH	*PS-IIW;100GN		TP
001	0043	P1-D09	P2-D00	XQ	66	HH	*PS-OPO;100		TP
001	0044	P1-D10	P2-D02	XQ	44	HH	*PS-OPO;100GN		TP
001	0045	P1-D00	P2-D09	XQ	66	HH	*PS-OPI;100		TP
001	0046	P1-D02	P2-D10	XQ	44	HH	*PS-OPI;100GN		TP
001	0047	P1-C00	P2-D16	XQ	66	HH	*PS-SCI;100		TP
001	0048	P1-C01	P2-D17	XQ	44	HH	*PS-SCI;100GN		TP
001		CABLE #2							
001	0049	P1-C08	P2-C09	XQ	66	HH	*PS-TMI;100		TP
001	0050	P1-C06	P2-C13	XQ	44	HH	*PS-TMI;100GN		TP
001	0051	P1-C05	P2-C09	XQ	66	HH	*PS-TMI;100		TP
001	0052	P1-C06	P2-C13	XQ	44	HH	*PS-TMI;100GN		TP
001	0053	P1-C05	P2-C11	XQ	66	HH	*PS-TMI;100		TP
001	0054	P1-C06	P2-C13	XQ	44	HH	*PS-TMI;100GN		TP
001	0055	P1-C11	P2-B15	XQ	66	HH	*PS-STO;100		TP
001	0056	P1-C13	P2-B13	XQ	44	HH	*PS-STO;100GN		TP
001	0057	P1-C10	P2-B15	XQ	66	HH	*PS-STO;100		TP
001	0058	P1-C13	P2-B13	XQ	44	HH	*PS-STO;100GN		TP
001	0059	P1-C10	P2-B12	XQ	66	HH	*PS-STO;100		TP
001	0060	P1-C13	P2-B13	XQ	44	HH	*PS-STO;100GN		TP
001	0061	P1-D07	P2-D15	XQ	66	HH	*PS-STI;100		TP
001	0062	P1-D06	P2-D20	XQ	44	HH	*PS-STI;100GN		TP

WIRE LIST
PSI FREE EDGE TO FREE EDGE CABLE 5F

TAB	SEQ	FROM	TO	TY	CL	TM	LOGIC	RV	BK
001	0063	P1-D05	P2-D15	XQ	66	HH	*PS-STI;100		TP
001	0064	P1-D06	P2-D20	XQ	44	HH	*PS-STI;100GN		TP
001	0065	P1-D05	P2-D21	XQ	66	HH	*PS-STI;100		TP
001	0066	P1-D06	P2-D20	XQ	44	.HH	*PS-STI;100GN		TP
001	0067	P1-D16	P2-C05	XQ	66	HH	*PS-SEQ;100		TP
001	0068	P1-D17	P2-C06	XQ	44	HH	*PS-SEO;100GN		TP
001	0069	P1-D15	P2-C05	XQ	66	HH	*PS-SEO;100		TP
001	0070	P1-D17	P2-C06	XQ	44	HH	*PS-SEO;100GN		TP
001	0071	P1-D15	P2-C08	XQ	66	HH	*PS-SEO;100		TP
001	0072	P1-D17	P2-C06	XQ	44	HH	*PS-SEO;100GN		TP
001	0073	P1-D21	P2-D08	XQ	66	HH	*PS-TMO;100		TP
001	0074	P1-D20	P2-D11	XQ	44	HH	*PS-TMO;100GN		TP
001	0075	P1-D19	P2-D08	XQ	66	HH	*PS-TMO;100		TP
001	0076	P1-D20	P2-D11	XQ	44	HH	*PS-TMO;100GN		TP
001	0077	P1-D19	P2-D14	XQ	66	HH	*PS-TMO;100		TP
001	0078	P1-D20	P2-D11	XQ	44	HH	*PS-TMO;100GN		TP

Honeywell

REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE
A	LEVEL 3 ISSUE	80	09	09	[illegible]



REFERANCE W.L. 58018720

58018720	REF SPEC NO

UNLESS OTHERWISE SPECIFIED
DIMENSIONS = MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN
PROJECTION
SCALE | CODE
MATL
TREAT.
FIN.
DR G. Pepple 80 AUG. 6
APPD [illegible]
DISTR C106 — 10

Honeywell
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U. S. A.
LOC

TITLE SCHEMATIC
HSLA (MPC)

SIZE	DWG NO	SH	REV
D	58052546	1/1	A

58052546

REV	AUTHORITY	DATE
B	PHAOXS582	84OCT20

SIGNAL NAME	PAGE
$BP-CLK•000	42.0
$BP-CLK•001	4.0
$CHP-RST•000	44.0
$CHP-RST•010	44.0
$CHP-RST•100	44.0
$CHP-RST•110	44.0
$CHP-TST-RST•000	47.0
$DAU•011	37.0
$DAU•021	37.0
$DAU-TOT-CLR•012	37.0
$DBL-AN-NRST•100	44.0
$DOUBLE•000	42.0
$DOUBLE•100	42.0
$ECC•100	44.0
$ECC•101	4.0
$ED-DAU•000	37.0
$ED-DAU•100	37.0
$ED-DAU•101	37.0
$LD-P0-3•100	48.0
$P-LATCH•100	45.0
$P4CLR•000	42.0
$PAR-OR-EDCL•000	43.0
$PART-OR-ED-CL•010	37.0
$PART-OR-ED-CL•011	37.0
$PART-OR-ED-CL•100	37.0
$PART-OR-ED-CL•101	37.0
$PARTIAL-CLR•012	34.0
$PARTIAL-CLR•022	34.0
$SEL-ED•010	47.0
$SEL-ED•100	47.0
$SHIFT•100	44.0
$SHT4C•000	39.0
$SHT4RC•000	39.0
$SHT4RWC•100	39.0
$SHT4W•000	39.0
$SHT5R•000	39.0
$SHT5RWC•000	38.0
$SHTCLK•100	42.0
$TOT-OR-ED-CLR•100	37.0
$TOT-OR-ED-CLR•101	37.0
$TOT-OR-ED-CLR•102	37.0
+5V-09ME-00	6.0
B-FULL•100	42.0
B-P0•000	47.0
B-P1•000	47.0
B-P2•000	47.0
B-P3•000	47.0
B-REP•000	47.0
B-REP•110	48.0
BREG-00•110	40.0
BREG-01•110	40.0
BREG-02•110	40.0
BREG-03•110	40.0
BREG-04•110	41.0
BREG-05•110	41.0
BREG-06•110	41.0
BREG-07•110	41.0
BREG-P•110	41.0
CMD-WRITE•030	39.0
CMD-WRITE•120	39.0
CMD-WRITE•140	39.0
D-ANY4ERR•000	48.0
D-AZ•000	45.0
D-AZ•000	46.0
D-AZ•000	45.0

SIGNAL NAME	PAGE
D-AZ•110	46.0
D-BP0•100	47.0
D-BP1•100	47.0
D-BP2•100	47.0
D-BP3•100	47.0
D-BP4•100	47.0
D-BP5•100	47.0
D-BP6•100	47.0
D-BP7•100	47.0
D-CRC-CL•100	44.0
D-CRCAZ•010	46.0
D-CRCAZ•100	45.0
D-CRCAZ1•000	46.0
D-CRCAZ2•000	46.0
D-CRCAZ3•000	46.0
D-DATACLK•100	42.0
D-DTANOT•010	42.0
D-DTANOT•100	42.0
D-ECC-CL•100	44.0
D-ED-P-ERR•100	45.0
D-EDAC-ERROR•100	40.0
D-EDAC-ERROR•101	4.0
D-EN-ECC•100	44.0
D-INH-50X•000	38.0
D-INH-ECC•000	44.0
D-LAST-EDAC•020	39.0
D-LAST-EDAC•110	39.0
D-LP0•100	47.0
D-LP1•100	47.0
D-LP2•100	47.0
D-ONE•100	33.0
D-ONE-LOAD•010	42.0
D-ONE-LOAD•100	42.0
D-ONE-LOAD•101	4.0
D-RD•100	47.0
D-RESET-SYNC•000	43.0
D-S0•010	48.0
D-S0•100	47.0
D-S1•100	47.0
D-S2•100	47.0
D-S3•100	47.0
D-S4•100	47.0
D-S5•100	47.0
D-SW-0•100	40.0
D-SW-1•100	40.0
D-SW-2•100	40.0
D-SW-3•100	40.0
D-SW-4•100	41.0
D-SW-5•100	41.0
D-SW-6•100	41.0
D-SW-7•100	41.0
D-SW-P•100	41.0
D-WR-RD•100	47.0
D4ERR•000	40.0
D50X•010	24.0
D50X•100	24.0
D5LAT•100	38.0
DATA-WRITE•000	43.0
DATA-WRITE•001	4.0
DBRD-SEL•100	22.0
DBRD-SEL-0-0S0•100	22.0
DBREG-ACK•100	43.0
DBSTB•000	42.0
DCONT/SWO•100	21.0
DCOUNT-OUT-0S0•100	21.0

SIGNAL NAME	PAGE
DDAI-INIT-0S1•100	13.0
DDEN-00-0S0•100	21.0
DDEN-01-0S0•100	21.0
DDEN-02-0S0•100	21.0
DDEN-03-0S0•100	21.0
DDTA-I-D10-0S0•100	21.0
DDTA-I-D11-0S0•100	21.0
DDTA-I-D12-0S0•100	21.0
DDTA-I-D13-0S0•100	22.0
DDTA-I-D14-0S0•100	22.0
DDTA-I-D15-0S0•100	22.0
DDTA-I-D16-0S0•100	22.0
DDTA-I-D17-0S0•100	22.0
DDTA-I-D1P-0S0•100	21.0
DE-16•000	24.0
DE-16•110	25.0
DE-16-512•100	25.0
DE-16-64•100	25.0
DE-512•000	24.0
DE-512•110	25.0
DE-64•000	24.0
DE-64•110	25.0
DE-8•000	24.0
DE-8•110	25.0
DE-8-16-512•100	25.0
DE-8-16-64•100	25.0
DE-8-16-64-512•100	25.0
DE-8-64•100	25.0
DE-8-64-512•100	25.0
DE-COR-BIT•100	35.0
DE-CRC-ERR•010	36.0
DE-CRC-ERR•100	36.0
DE-FBK-OUT•100	28.0
DE-FEEDBACK•000	28.0
DE-FEEDBACK•110	28.0
DE-FEEDBACK•111	28.0
DE-IN-X00•100	26.0
DE-IN-X02•100	26.0
DE-IN-X03•100	26.0
DE-IN-X09•100	26.0
DE-IN-X10•100	26.0
DE-IN-X12•100	26.0
DE-IN-X13•100	27.0
DE-IN-X14•100	27.0
DE-IN-X15•100	27.0
DE-IN-X20•100	27.0
DE-IN-X21•100	27.0
DE-IN-X22•100	27.0
DE-IN-X23•100	27.0
DE-INH-FBK•000	28.0
DE-OR-O-CRC•000	39.0
DE-OR-O-ERR•000	40.0
DE-SET-W04•100	31.0
DE-SET-W08•100	31.0
DE-SET-W12•100	31.0
DE-SET-W16•100	31.0
DE-SET-W20•100	31.0
DE-SET-X04•100	27.0
DE-SET-X08•100	27.0
DE-SET-X12•100	27.0
DE-SET-X16•100	27.0
DE-SET-X20•100	28.0
DE-Z-0-19•100	27.0
DE-Z-0-19•100	28.0
DE-Z-0-19•100	27.0

SIGNAL NAME	PAGE
DE-Z-0-19•100	28.0
DE-Z-0-21•010	28.0
DE-Z-0-21•100	28.0
DE-Z-0-23•000	28.0
DE-Z-20-23•100	28.0
DEN-5RWC•100	38.0
DEN-B-ACK1•000	37.0
DEN-B-ACK2•000	37.0
DEN-DIN1-0•000	40.0
DEN-DIN1-1•000	40.0
DEN-EDAC-BYTES•100	43.0
DEV-A-SEL•000	21.0
DEV-A-SEL•100	21.0
DEV-A-SEL•110	22.0
DEV-A-SEL/INH•100	21.0
DEV-B-SEL•000	21.0
DEV-B-SEL•100	21.0
DEV-B-SEL•110	22.0
DEV-B-SEL/INH•100	21.0
DEV-C-SEL•000	20.0
DEV-C-SEL•100	20.0
DEV-C-SEL•110	20.0
DEV-C-SEL/INH•100	21.0
DEV-D-SEL•000	20.0
DEV-D-SEL•100	20.0
DEV-D-SEL•110	20.0
DEV-D-SEL/INH•100	21.0
DEW-FEEDBACK•100	31.0
DEW-FEEDBACK•101	31.0
DFAULT-FLT-0S0•100	22.0
DHI1•100	36.0
DINDEX-IDX-0S0•100	22.0
DINIT-DIN•100	22.0
DINIT-DIN-0S0•100	22.0
DMPADR-12•100	34.0
DMPADR-12•110	34.0
DMPADR-13•100	34.0
DMPADR-13•110	34.0
DMPADR-14•100	34.0
DMPADR-14•110	34.0
DMPADR-15•100	34.0
DMPADR-15•110	34.0
DO-16•000	25.0
DO-16•110	26.0
DO-16-512•100	26.0
DO-16-64•100	26.0
DO-512•000	25.0
DO-512•110	26.0
DO-64•000	25.0
DO-64•110	26.0
DO-8•000	25.0
DO-8•110	26.0
DO-8-16-512•100	26.0
DO-8-16-64•100	26.0
DO-8-16-64-512•100	26.0
DO-8-64•100	26.0
DO-8-64-512•100	26.0

DISTRIBUTION CODE C120-26

HONEYWELL
LOC CEO HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAEI
LOGIC -
PAGE CROSS REFERENCE

ASM REF 58075910-X04

DATA BASE NIODAU/DAU$45/HE
OR DFTG 84OCT20

SIZE	DWG NO	SH	REV
B	58075914	1.0	B

58075914

REV	AUTHORITY	DATE
B	PHAOXS582	84OCT20

SIGNAL NAME	PAGE
DO-COR-BIT•100	35.0
DO-CRC-ERR•010	36.0
DO-CRC-ERR•100	36.0
DO-FBK-OUT•100	30.0
DO-FEEDBACK•000	30.0
DO-FEEDBACK•110	30.0
DO-FEEDBACK•111	30.0
DO-IN-X00•100	28.0
DO-IN-X02•100	28.0
DO-IN-X03•100	28.0
DO-IN-X09•100	29.0
DO-IN-X10•100	29.0
DO-IN-X12•100	29.0
DO-IN-X13•100	29.0
DO-IN-X14•100	29.0
DO-IN-X15•100	29.0
DO-IN-X20•100	29.0
DO-IN-X21•100	29.0
DO-IN-X22•100	29.0
DO-IN-X23•100	29.0
DO-INH-FBK•000	30.0
DO-SET-W04•100	32.0
DO-SET-W08•100	32.0
DO-SET-W12•100	32.0
DO-SET-W16•100	32.0
DO-SET-W20•100	32.0
DO-SET-X04•100	29.0
DO-SET-X08•100	29.0
DO-SET-X12•100	29.0
DO-SET-X16•100	30.0
DO-SET-X20•100	30.0
DO-Z-0-19•100	29.0
DO-Z-0-19•100	30.0
DO-Z-0-19•100	29.0
DO-Z-0-19•100	30.0
DO-Z-0-21•010	30.0
DO-Z-0-21•100	30.0
DO-Z-0-23•000	30.0
DO-Z-20-23•100	30.0
DOPER-OPI-0S0•100	22.0
DOW-FEEDBACK•100	32.0
DOW-FEEDBACK•101	32.0
DPSREADY•000	13.0
DPSREADY•110	13.0
DRD-PR-DEV-0S0•100	21.0
DREG-0•020	24.0
DREG-0•110	24.0
DREG-1•020	24.0
DREG-1•110	24.0
DREG-2•020	24.0
DREG-2•110	24.0
DREG-3•020	24.0
DREG-3•110	24.0
DREG-4•020	24.0
DREG-4•110	24.0
DREG-5•020	24.0
DREG-5•110	24.0
DREG-6•020	24.0
DREG-6•110	24.0
DREG-7•020	24.0
DREG-7•110	24.0
DREG-P•110	41.0
DSE-WR•000	43.0
DSEL-ED•020	47.0
DSEL-ED•110	41.0

SIGNAL NAME	PAGE
DSEL-ED•120	41.0
DSET-BREG-ACK•100	37.0
DSET-CREG-FULL•100	39.0
DSET-ED-ERR•100	40.0
DSET-EDAC-BYTES•100	43.0
DSET-LAST-BIT•100	39.0
DSET-LAST-BYTE•100	39.0
DSET-P0-3•010	48.0
DSET-P0-3•100	48.0
DSR-RD-SRI-0S0•100	22.0
DSTART-COUNT•010	38.0
DSTART-COUNT•100	38.0
DZERO-COUNT•000	38.0
DZERO-COUNT•001	4.0
DZERO-COUNT•110	38.0
ECC-LAT•100	41.0
ED-CLR-OR-DTA•100	44.0
ED-READY•100	48.0
EDAC-4STB•000	38.0
EDAC-50X-STB•000	38.0
EDAC-BYTES•120	41.0
EDAC-BYTES•130	41.0
EDAC-CLEAR•040	37.0
EDAC-CLEAR•130	37.0
EDAC-CLEAR•150	44.0
EDAC-DATA-P•100	35.0
EDAC-STB•130	38.0
EDAC-STB•140	41.0
EN-DTA-A-1S0•100	14.0
EN-DTA-A-1S0•100	6.0
EN-DTA-A-1S0•100	14.0
EN-DTA-B-1S0•100	15.0
EN-DTA-B-1S0•100	6.0
EN-DTA-B-1S0•100	15.0
EN-DTA-C-1S0•100	15.0
EN-DTA-C-1S0•100	6.0
EN-DTA-C-1S0•100	15.0
EN-DTA-D-1S0•100	6.0
EN-DTA-D-1S0•100	15.0
EN-OUTLAT•100	48.0
ENABLE-OPI•100	6.0
ENABLE-OPI•100	21.0
ENABLE-OPI•110	21.0
ENABLE-SENSE•100	21.0
ENABLE-SENSE•100	6.0
ENABLE-SENSE•110	21.0
EVEN-PAR•100	45.0
F-ACK•000	43.0
F-ACK•100	43.0
F-EDAC-BYTES•000	43.0
F-EDAC-BYTES•100	43.0
F-EDAC-ERROR•100	40.0
F-EDAC-ERROR•110	35.0
F-EDAC-READY•100	48.0
F-EDAC-READY•110	35.0
F-PAR•000	45.0
F-PAR•100	45.0
FB-ACK-RES•000	43.0
FB-ACK-RES•110	43.0
FB-REG-FUL•110	37.0
FB-REG-FUL•120	41.0
FBREG-ACK•000	37.0
FBREG-ACK•100	37.0
FBSTB•000	42.0
FBSTB•100	42.0

SIGNAL NAME	PAGE
FCMD-DC0•100	23.0
FCMD-DC0-0S0•100	23.0
FCMD-DC1•100	23.0
FCMD-DC1-0S0•100	23.0
FCMD-DC2•100	23.0
FCMD-DC2-0S0•100	23.0
FCMD-DC3•100	23.0
FCMD-DC3-0S0•100	23.0
FCMD-DC4•100	23.0
FCMD-DC4-0S0•100	23.0
FCMD-DC5•100	23.0
FCMD-DC5-0S0•100	23.0
FCMD-DCP•100	22.0
FCMD-DCP-0S0•100	22.0
FCMD-DCS•100	23.0
FCMD-DCS-0SD•100	23.0
FCREG-ACK•110	41.0
FCREG-ACK•120	41.0
FCREG-FULL•000	39.0
FCREG-FULL•100	39.0
FCREG-FULL•110	35.0
FDEV-SEL-2•100	22.0
FDEV-SEL-2-0S0•100	22.0
FDEV-SEL-3•100	22.0
FDEV-SEL-3-0S0•100	22.0
FDTA-M-DM1•100	22.0
FDTA-M-DM1-0S0•100	22.0
FDTA-O-D10•100	23.0
FDTA-O-D10-0S0•100	23.0
FDTA-O-D11•100	23.0
FDTA-O-D11-0S0•100	23.0
FDTA-O-D12•100	23.0
FDTA-O-D12-0S0•100	23.0
FDTA-O-D13•100	23.0
FDTA-O-D13-0S0•100	23.0
FDTA-O-D14•100	23.0
FDTA-O-D14-0S0•100	23.0
FDTA-O-D15•100	23.0
FDTA-O-D15-0S0•100	23.0
FDTA-O-D16•100	23.0
FDTA-O-D16-0S0•100	23.0
FDTA-O-D17•100	23.0
FDTA-O-D17-0S0•100	23.0
FDTA-O-D1P•100	23.0
FDTA-O-D1P-0S0•100	23.0
FLAST-BIT•100	39.0
FLAST-BYTE•100	39.0
FMPEDRD•100	43.0
GND-00A-08	6.0
GND-00B-08	6.0
GND-00BE	4.0
GND-00C-08	8.0
GND-00D-08	7.0
GND-00D-08	8.0
GND-00DE	4.0
GND-00E-08	13.0
GND-00F-08	13.0
GND-00G-08	6.0
GND-00H-08	6.0
GND-00H-08	7.0
GND-00HE	4.0
GND-00J-08	8.0
GND-00K-08	8.0
GND-00KE	4.0
GND-00L-08	13.0

SIGNAL NAME	PAGE
GND-00M-08	7.0
GND-00ME	5.0
GND-00N-08	7.0
GND-00P-08	8.0
GND-00P-08	9.0
GND-00PE	5.0
GND-00Q-08	8.0
GND-00R-08	14.0
GND-00S-08	14.0
GND-00T-08	7.0
GND-00TE	5.0
GND-00U-08	7.0
GND-00V-08	9.0
GND-00VE	5.0
GND-00W-08	9.0
GND-00X-08	14.0
GND-09A-08	9.0
GND-09B-08	9.0
GND-09BE	4.0
GND-09C-08	11.0
GND-09D-08	11.0
GND-09DE	4.0
GND-09E-08	11.0
GND-09E-08	13.0
GND-09FE	4.0
GND-09G-08	9.0
GND-09G-08	10.0
GND-09H-08	10.0
GND-09HE	5.0
GND-09J-08	11.0
GND-09K-08	11.0
GND-09KE	5.0
GND-09L-08	12.0
GND-09L-08	13.0
GND-09M-08	10.0
GND-09N-08	10.0
GND-09P-08	12.0
GND-09PE	5.0
GND-09Q-08	12.0
GND-09R-08	12.0
GND-09R-08	14.0
GND-09RE	5.0
GND-09T-08	10.0
GND-09TE	5.0
GND-09U-08	11.0
GND-09U-08	10.0
GND-09V-08	12.0
GND-09VE	5.0
GND-09W-08	12.0
GND-09X-08	13.0
GND-09X-08	14.0
GND-18A-08	14.0
GND-18A-08	15.0
GND-18B-08	15.0
GND-18B-08	16.0
GND-18C-08	16.0
GND-18D-08	18.0

DISTRIBUTION CODE C120-26

HONEYWELL
LOC CEO HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAEI LOGIC - PAGE CROSS REFERENCE

ASM REF 58075910-X04

DATA BASE NIODAU/DAU$45/HEI

DR DFTG 84OCT20

SIZE	DWG NO	SH	REV
B	58075914	1.1	B

58075914

REV	AUTHORITY	DATE
B	PHAOXS582	84OCT2Ø

SIGNAL NAME	PAGE
GND-18D-Ø8	17.Ø
GND-18DE	5.Ø
GND-18E-Ø8	17.Ø
GND-18E-Ø8	18.Ø
GND-18E-Ø8	17.Ø
GND-18F-Ø8	21.Ø
GND-18G-Ø8	15.Ø
GND-18H-Ø8	15.Ø
GND-18H-Ø8	16.Ø
GND-18H-Ø8	15.Ø
GND-18J-Ø8	16.Ø
GND-18K-Ø8	18.Ø
GND-18KE	5.Ø
GND-18L-Ø8	18.Ø
GND-18M-Ø8	15.Ø
GND-18N-Ø8	16.Ø
GND-18N-Ø8	15.Ø
GND-18N-Ø8	17.Ø
GND-18P-Ø8	17.Ø
GND-18Q-Ø8	2Ø.Ø
GND-18R-Ø8	18.Ø
GND-18RE	6.Ø
GND-18S-Ø8	18.Ø
GND-18T-Ø8	15.Ø
GND-18T-Ø8	16.Ø
GND-18T-Ø8	15.Ø
GND-18U-Ø8	17.Ø
GND-18U-Ø8	16.Ø
GND-18U-Ø8	17.Ø
GND-18U-Ø8	16.Ø
GND-18V-Ø8	17.Ø
GND-18VE	6.Ø
GND-18W-Ø8	19.Ø
GND-18X-Ø8	19.Ø
GND-27A-Ø8	27.Ø
GND-27B-Ø8	27.Ø
GND-27C-Ø8	27.Ø
GND-27K-Ø8	2Ø.Ø
GND-27R-Ø8	5Ø.Ø
GND-27S-Ø8	49.Ø
GND-27V-Ø8	46.Ø
GND-27W-Ø8	46.Ø
GND-27X-Ø8	46.Ø
GND-36A-Ø8	28.Ø
GND-36B-Ø8	28.Ø
GND-36C-Ø8	27.Ø
GND-36K-Ø8	31.Ø
GND-36L-Ø8	31.Ø
GND-36M-Ø8	31.Ø
GND-36Q-Ø7	35.Ø
GND-36R-Ø8	49.Ø
GND-36S-Ø8	49.Ø
GND-36U-Ø8	45.Ø
GND-36V-Ø8	45.Ø
GND-36W-Ø8	45.Ø
GND-36X-Ø8	45.Ø
GND-45K-Ø8	31.Ø
GND-45L-Ø8	31.Ø
GND-45M-Ø8	31.Ø
GND-45R-Ø8	49.Ø
GND-45S-Ø8	49.Ø
GND-54A-Ø8	29.Ø
GND-54B-Ø8	29.Ø
GND-54C-Ø8	29.Ø
GND-54K-Ø8	32.Ø

SIGNAL NAME	PAGE
GND-54L-Ø8	32.Ø
GND-54M-Ø8	32.Ø
GND-54Q-Ø8	41.Ø
GND-54S-Ø8	48.Ø
GND-54T-Ø8	42.Ø
GND-6ØG-Ø8	4Ø.Ø
GND-6ØH-Ø8	38.Ø
GND-62U-Ø8	43.Ø
GND-62V-Ø8	41.Ø
GND-63A-Ø8	3Ø.Ø
GND-63B-Ø8	3Ø.Ø
GND-63C-Ø8	3Ø.Ø
GND-63K-Ø8	32.Ø
GND-63L-Ø8	32.Ø
GND-63M-Ø8	32.Ø
GND-63Q-Ø8	4Ø.Ø
GND-71V-Ø8	41.Ø
GND-72K-Ø8	35.Ø
GND-72L-Ø8	35.Ø
GND-72M-Ø8	34.Ø
GND-72P-Ø8	4Ø.Ø
GND-72Q-Ø8	41.Ø
GND-72S-2Ø	47.Ø
GND-8ØV-Ø8	43.Ø
GND-8ØV-Ø8	45.Ø
GND-81A-Ø8	36.Ø
GND-81B-Ø8	36.Ø
GND-81K-Ø8	25.Ø
GND-81L-Ø8	24.Ø
GND-81M-Ø8	35.Ø
GND-81Q-Ø8	41.Ø
GND-89V-Ø8	44.Ø
GND-9ØA-Ø8	36.Ø
GND-9ØB-Ø8	37.Ø
GND-9ØB-Ø8	21.Ø
GND-9ØB-Ø8	37.Ø
GND-9ØC-Ø7	36.Ø
GND-92P-Ø8	34.Ø
GND-92R-Ø8	41.Ø
I-D1Ø-A-1SØ•1ØØ	9.Ø
I-D1Ø-A-1SØ•1ØØ	4.Ø
I-D1Ø-B-1SØ•1ØØ	[illegible]
I-D1Ø-B-1SØ•1ØØ	5.Ø
I-D1Ø-C-1SØ•1ØØ	5.Ø
I-D1Ø-C-1SØ•1ØØ	1Ø.Ø
I-D1Ø-D-1SØ•1ØØ	5.Ø
I-D1Ø-D-1SØ•1ØØ	1Ø.Ø
I-D11-A-1SØ•1ØØ	9.Ø
I-D11-A-1SØ•1ØØ	4.Ø
I-D11-B-1SØ•1ØØ	5.Ø
I-D11-B-1SØ•1ØØ	1Ø.Ø
I-D11-C-1SØ•1ØØ	5.Ø
I-D11-C-1SØ•1ØØ	1Ø.Ø
I-D11-D-1SØ•1ØØ	5.Ø
I-D11-D-1SØ•1ØØ	1Ø.Ø
I-D12-A-1SØ•1ØØ	9.Ø
I-D12-A-1SØ•1ØØ	4.Ø
I-D12-B-1SØ•1ØØ	1Ø.Ø
I-D12-B-1SØ•1ØØ	5.Ø
I-D12-C-1SØ•1ØØ	1Ø.Ø
I-D12-C-1SØ•1ØØ	5.Ø
I-D12-D-1SØ•1ØØ	5.Ø
I-D12-D-1SØ•1ØØ	11.Ø
I-D13-A-1SØ•1ØØ	4.Ø
I-D13-A-1SØ•1ØØ	11.Ø

SIGNAL NAME	PAGE
I-D13-B-1SØ•1ØØ	5.Ø
I-D13-B-1SØ•1ØØ	11.Ø
I-D13-C-1SØ•1ØØ	12.Ø
I-D13-C-1SØ•1ØØ	5.Ø
I-D13-D-1SØ•1ØØ	5.Ø
I-D13-D-1SØ•1ØØ	12.Ø
I-D14-A-1SØ•1ØØ	11.Ø
I-D14-A-1SØ•1ØØ	4.Ø
I-D14-B-1SØ•1ØØ	11.Ø
I-D14-B-1SØ•1ØØ	5.Ø
I-D14-C-1SØ•1ØØ	5.Ø
I-D14-C-1SØ•1ØØ	12.Ø
I-D14-D-1SØ•1ØØ	12.Ø
I-D14-D-1SØ•1ØØ	5.Ø
I-D15-A-1SØ•1ØØ	11.Ø
I-D15-A-1SØ•1ØØ	4.Ø
I-D15-B-1SØ•1ØØ	11.Ø
I-D15-B-1SØ•1ØØ	4.Ø
I-D15-C-1SØ•1ØØ	5.Ø
I-D15-C-1SØ•1ØØ	12.Ø
I-D15-D-1SØ•1ØØ	5.Ø
I-D15-D-1SØ•1ØØ	12.Ø
I-D16-A-1SØ•1ØØ	4.Ø
I-D16-A-1SØ•1ØØ	11.Ø
I-D16-B-1SØ•1ØØ	5.Ø
I-D16-B-1SØ•1ØØ	11.Ø
I-D16-C-1SØ•1ØØ	5.Ø
I-D16-C-1SØ•1ØØ	12.Ø
I-D16-D-1SØ•1ØØ	5.Ø
I-D16-D-1SØ•1ØØ	12.Ø
I-D17-A-1SØ•1ØØ	11.Ø
I-D17-A-1SØ•1ØØ	4.Ø
I-D17-B-1SØ•1ØØ	5.Ø
I-D17-B-1SØ•1ØØ	12.Ø
I-D17-C-1SØ•1ØØ	5.Ø
I-D17-C-1SØ•1ØØ	12.Ø
I-D17-D-1SØ•1ØØ	13.Ø
I-D17-D-1SØ•1ØØ	5.Ø
I-D1P-A-1SØ•1ØØ	4.Ø
I-D1P-A-1SØ•1ØØ	9.Ø
I-D1P-B-1SØ•1ØØ	4.Ø
I-D1P-B-1SØ•1ØØ	9.Ø
I-D1P-C-1SØ•1ØØ	5.Ø
I-D1P-C-1SØ•1ØØ	1Ø.Ø
I-D1P-D-1SØ•1ØØ	1Ø.Ø
I-D1P-D-1SØ•1ØØ	5.Ø
I-DCØ-A-1SØ•1ØØ	6.Ø
I-DCØ-A-1SØ•1ØØ	4.Ø
I-DCØ-B-1SØ•1ØØ	4.Ø
I-DCØ-B-1SØ•1ØØ	6.Ø
I-DCØ-C-1SØ•1ØØ	5.Ø
I-DCØ-C-1SØ•1ØØ	7.Ø
I-DCØ-D-1SØ•1ØØ	7.Ø
I-DCØ-D-1SØ•1ØØ	5.Ø
I-DC1-A-1SØ•1ØØ	6.Ø
I-DC1-A-1SØ•1ØØ	4.Ø
I-DC1-B-1SØ•1ØØ	4.Ø
I-DC1-B-1SØ•1ØØ	6.Ø
I-DC1-C-1SØ•1ØØ	5.Ø
I-DC1-C-1SØ•1ØØ	7.Ø
I-DC1-D-1SØ•1ØØ	5.Ø
I-DC1-D-1SØ•1ØØ	7.Ø
I-DC2-A-1SØ•1ØØ	4.Ø
I-DC2-A-1SØ•1ØØ	6.Ø
I-DC2-B-1SØ•1ØØ	7.Ø

SIGNAL NAME	PAGE
I-DC2-B-1SØ•1ØØ	4.Ø
I-DC2-C-1SØ•1ØØ	7.Ø
I-DC2-C-1SØ•1ØØ	5.Ø
I-DC2-D-1SØ•1ØØ	5.Ø
I-DC2-D-1SØ•1ØØ	7.Ø
I-DC3-A-1SØ•1ØØ	4.Ø
I-DC3-A-1SØ•1ØØ	7.Ø
I-DC3-B-1SØ•1ØØ	8.Ø
I-DC3-B-1SØ•1ØØ	4.Ø
I-DC3-C-1SØ•1ØØ	5.Ø
I-DC3-C-1SØ•1ØØ	8.Ø
I-DC3-D-1SØ•1ØØ	9.Ø
I-DC3-D-1SØ•1ØØ	5.Ø
I-DC4-A-1SØ•1ØØ	8.Ø
I-DC4-A-1SØ•1ØØ	4.Ø
I-DC4-B-1SØ•1ØØ	4.Ø
I-DC4-B-1SØ•1ØØ	8.Ø
I-DC4-C-1SØ•1ØØ	5.Ø
I-DC4-C-1SØ•1ØØ	8.Ø
I-DC4-D-1SØ•1ØØ	9.Ø
I-DC4-D-1SØ•1ØØ	5.Ø
I-DC5-A-1SØ•1ØØ	4.Ø
I-DC5-A-1SØ•1ØØ	8.Ø
I-DC5-B-1SØ•1ØØ	4.Ø
I-DC5-B-1SØ•1ØØ	8.Ø
I-DC5-C-1SØ•1ØØ	8.Ø
I-DC5-C-1SØ•1ØØ	5.Ø
I-DC5-D-1SØ•1ØØ	5.Ø
I-DC5-D-1SØ•1ØØ	9.Ø
I-DCP-A-1SØ•1ØØ	6.Ø
I-DCP-A-1SØ•1ØØ	4.Ø
I-DCP-B-1SØ•1ØØ	4.Ø
I-DCP-B-1SØ•1ØØ	6.Ø
I-DCP-C-1SØ•1ØØ	5.Ø
I-DCP-C-1SØ•1ØØ	7.Ø
I-DCP-D-1SØ•1ØØ	7.Ø
I-DCP-D-1SØ•1ØØ	5.Ø
I-DCS-A-1SØ•1ØØ	8.Ø
I-DCS-A-1SØ•1ØØ	4.Ø
I-DCS-B-1SØ•1ØØ	8.Ø
I-DCS-B-1SØ•1ØØ	4.Ø
I-DCS-C-1SØ•1ØØ	9.Ø
I-DCS-C-1SØ•1ØØ	5.Ø
I-DCS-D-1SØ•1ØØ	9.Ø
I-DCS-D-1SØ•1ØØ	5.Ø
I-DEN-A-1SØ•1ØØ	18.Ø
I-DEN-A-1SØ•1ØØ	5.Ø
I-DEN-B-1SØ•1ØØ	5.Ø
I-DEN-B-1SØ•1ØØ	18.Ø
I-DEN-C-1SØ•1ØØ	6.Ø
I-DEN-C-1SØ•1ØØ	18.Ø
I-DEN-D-1SØ•1ØØ	19.Ø
I-DEN-D-1SØ•1ØØ	6.Ø
I-DIN-A-1SØ•1ØØ	4.Ø
I-DIN-A-1SØ•1ØØ	13.Ø
I-DIN-B-1SØ•1ØØ	[illegible]
I-DIN-B-1SØ•1ØØ	4.Ø

DISTRIBUTION CODE C12Ø-26

HONEYWELL

LOC CEO HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAEI LOGIC - PAGE CROSS REFERENCE

ASM REF 58Ø7591Ø-XØ4

DATA BASE NIODAU/DAU$45/HEI

DFIG 84OCT2Ø

SIZE B | DWG NO 58Ø75914 | SH 1.2 | REV B

58Ø75914

REV	AUTHORITY	DATE
B	PHAOXS582	84OCT2Ø

SIGNAL NAME	PAGE
I-DIN-C-1SØ•1ØØ	14.Ø
I-DIN-C-1SØ•1ØØ	5.Ø
I-DIN-D-1SØ•1ØØ	5.Ø
I-DIN-D-1SØ•1ØØ	14.Ø
I-DM1-A-1SØ•1ØØ	13.Ø
I-DM1-A-1SØ•1ØØ	4.Ø
I-DM1-B-1SØ•1ØØ	5.Ø
I-DM1-B-1SØ•1ØØ	13.Ø
I-DM1-C-1SØ•1ØØ	14.Ø
I-DM1-C-1SØ•1ØØ	5.Ø
I-DM1-D-1SØ•1ØØ	14.Ø
I-DM1-D-1SØ•1ØØ	5.Ø
I-FLT-A-1SØ•1ØØ	5.Ø
I-FLT-A-1SØ•1ØØ	17.Ø
I-FLT-B-1SØ•1ØØ	5.Ø
I-FLT-B-1SØ•1ØØ	18.Ø
I-FLT-C-1SØ•1ØØ	6.Ø
I-FLT-C-1SØ•1ØØ	18.Ø
I-FLT-D-1SØ•1ØØ	19.Ø
I-FLT-D-1SØ•1ØØ	6.Ø
I-IDX-A-1SØ•1ØØ	5.Ø
I-IDX-A-1SØ•1ØØ	17.Ø
I-IDX-B-1SØ•1ØØ	18.Ø
I-IDX-B-1SØ•1ØØ	5.Ø
I-IDX-C-1SØ•1ØØ	18.Ø
I-IDX-C-1SØ•1ØØ	6.Ø
I-IDX-D-1SØ•1ØØ	6.Ø
I-IDX-D-1SØ•1ØØ	19.Ø
I-OPI-A-1SØ•1ØØ	18.Ø
I-OPI-A-1SØ•1ØØ	5.Ø
I-OPI-B-1SØ•1ØØ	18.Ø
I-OPI-B-1SØ•1ØØ	5.Ø
I-OPI-C-1SØ•1ØØ	18.Ø
I-OPI-C-1SØ•1ØØ	6.Ø
I-OPI-D-1SØ•1ØØ	6.Ø
I-OPI-D-1SØ•1ØØ	19.Ø
I-OPO-A-1SØ•1ØØ	4.0
I-OPO-A-1SØ•1ØØ	13.Ø
I-OPO-B-1SØ•1ØØ	4.Ø
I-OPO-B-1SØ•1ØØ	13.Ø
I-OPO-C-1SØ•1ØØ	14.Ø
I-OPO-C-1SØ•1ØØ	5.Ø
I-OPO-D-1SØ•1ØØ	5.Ø
I-OPO-D-1SØ•1ØØ	14.Ø
I-SRI-A-1SØ•1ØØ	17.Ø
I-SRI-A-1SØ•1ØØ	5.Ø
I-SRI-B-1SØ•1ØØ	18.Ø
I-SRI-B-1SØ•1ØØ	5.Ø
I-SRI-C-1SØ•1ØØ	18.Ø
I-SRI-C-1SØ•1ØØ	6.Ø
I-SRI-D-1SØ•1ØØ	19.Ø
I-SRI-D-1SØ•1ØØ	6.Ø
I-SWØ-A-1SØ•1ØØ	4.Ø
I-SWØ-A-1SØ•1ØØ	13.Ø
I-SWØ-B-1SØ•1ØØ	4.Ø
I-SWØ-B-1SØ•1ØØ	13.Ø
I-SWØ-C-1SØ•1ØØ	14.Ø
I-SWØ-C-1SØ•1ØØ	5.Ø
I-SWØ-D-1SØ•1ØØ	14.Ø
I-SWØ-D-1SØ•1ØØ	5.Ø
INH-DATA-OUT•1ØØ	21.Ø
INH-DTA-OUT•Ø1Ø	22.Ø
INH/DATA-SENSE•Ø1Ø	21.Ø
INH/DATA-SENSE•12Ø	22.Ø
INH/DATA-SENSE•121	22.Ø

SIGNAL NAME	PAGE
LAST-EDAC•13Ø	39.Ø
LAST-EDAC-STB•ØØØ	39.Ø
MPRD•Ø3Ø	47.Ø
MPRD•12Ø	47.Ø
MPWR•Ø3Ø	47.Ø
MPWR•12Ø	41.Ø
MPWR•13Ø	41.Ø
P-EDAC-DATA-P•1ØØ	35.Ø
POWER-CONF•1ØØ	13.Ø
R-CON1•1ØØ	45.Ø
R-CON2•1ØØ	45.Ø
R-CON3•1ØØ	45.Ø
R-CON4•1ØØ	45.Ø
R-CRCCON1•1ØØ	46.Ø
R-CRCCON2•1ØØ	46.Ø
R-D1Ø-A•1ØØ	14.Ø
R-D1Ø-B•1ØØ	15.Ø
R-D1Ø-C•1ØØ	15.Ø
R-D1Ø-D•1ØØ	15.Ø
R-D11-A•1ØØ	15.Ø
R-D11-B•1ØØ	15.Ø
R-D11-C•1ØØ	15.Ø
R-D11-D•1ØØ	16.Ø
R-D12-A•1ØØ	15.Ø
R-D12-B•1ØØ	15.Ø
R-D12-C•1ØØ	15.Ø
R-D12-D•1ØØ	16.Ø
R-D13-A•1ØØ	16.Ø
R-D13-B•1ØØ	16.Ø
R-D13-C•1ØØ	16.Ø
R-D13-D•1ØØ	17.Ø
R-D14-A•1ØØ	16.Ø
R-D14-B•1ØØ	16.Ø
R-D14-C•1ØØ	17.Ø
R-D14-D•1ØØ	17.Ø
R-D15-A•1ØØ	16.Ø
R-D15-B•1ØØ	16.Ø
R-D15-C•1ØØ	17.Ø
R-D15-D•1ØØ	17.Ø
R-D16-A•1ØØ	15.Ø
R-D16-B•1ØØ	15.Ø
R-D16-C•1ØØ	17.Ø
R-D16-D•1ØØ	17.Ø
R-D17-A•1ØØ	16.Ø
R-D17-B•1ØØ	16.Ø
R-D17-C•1ØØ	17.Ø
R-D17-D•1ØØ	17.Ø
R-D1P-A•1ØØ	14.Ø
R-D1P-B•1ØØ	15.Ø
R-D1P-C•1ØØ	15.Ø
R-D1P-D•1ØØ	15.Ø
R-DEN-A•1ØØ	18.Ø
R-DEN-B•1ØØ	18.Ø
R-DEN-C•1ØØ	18.Ø
R-DEN-D•1ØØ	19.Ø
R-DSYNC•ØØØ	43.Ø
R-DTA-CRC•1ØØ	46.Ø
R-ECCØ•1ØØ	45.Ø
R-ECC1•1ØØ	45.Ø
R-ECC1Ø•1ØØ	45.Ø
R-ECC11•1ØØ	45.Ø
R-ECC12•1ØØ	45.Ø
R-ECC13•1ØØ	45.Ø
R-ECC14•1ØØ	45.Ø
R-ECC15•1ØØ	45.Ø

SIGNAL NAME	PAGE
R-ECC2•1ØØ	45.Ø
R-ECC3•1ØØ	45.Ø
R-ECC4•1ØØ	45.Ø
R-ECC5•1ØØ	45.Ø
R-ECC6•1ØØ	45.Ø
R-ECC7•1ØØ	45.Ø
R-ECC8•1ØØ	45.Ø
R-ECC9•1ØØ	45.Ø
R-EDAC-DATA-Ø•1ØØ	33.Ø
R-EDAC-DATA-Ø•1ØØ	48.Ø
R-EDAC-DATA-Ø•11Ø	35.Ø
R-EDAC-DATA-1•1ØØ	49.Ø
R-EDAC-DATA-1•1ØØ	33.Ø
R-EDAC-DATA-1•11Ø	35.Ø
R-EDAC-DATA-2•1ØØ	33.Ø
R-EDAC-DATA-2•1ØØ	49.Ø
R-EDAC-DATA-2•11Ø	34.Ø
R-EDAC-DATA-3•1ØØ	49.Ø
R-EDAC-DATA-3•1ØØ	33.Ø
R-EDAC-DATA-3•11Ø	34.Ø
R-EDAC-DATA-4•1ØØ	33.Ø
R-EDAC-DATA-4•1ØØ	49.Ø
R-EDAC-DATA-4•11Ø	34.Ø
R-EDAC-DATA-5•1ØØ	49.Ø
R-EDAC-DATA-5•1ØØ	33.Ø
R-EDAC-DATA-5•11Ø	34.Ø
R-EDAC-DATA-6•1ØØ	49.Ø
R-EDAC-DATA-6•1ØØ	34.Ø
R-EDAC-DATA-6•11Ø	34.Ø
R-EDAC-DATA-7•1ØØ	34.Ø
R-EDAC-DATA-7•1ØØ	5Ø.Ø
R-EDAC-DATA-7•11Ø	34.Ø
R-ERLAT•ØØØ	41.Ø
R-ERLAT•1ØØ	41.Ø
R-FB-CRC•1ØØ	46.Ø
R-FLT-A•1ØØ	17.Ø
R-FLT-B•1ØØ	18.Ø
R-FLT-C•1ØØ	18.Ø
R-FLT-D•1ØØ	19.Ø
R-IDX-A•1ØØ	17.Ø
R-IDX-B•1ØØ	18.Ø
R-IDX-C•1ØØ	18.Ø
R-IDX-D•1ØØ	19.Ø
R-OPI-A•1ØØ	18.Ø
R-OPI-B•1ØØ	18.Ø
R-OPI-C•1ØØ	18.Ø
R-OPI-D•1ØØ	19.Ø
R-OUTLAT•1ØØ	42.Ø
R-PØ•1ØØ	48.Ø
R-PØ•1Ø1	4.Ø
R-P1•1ØØ	48.Ø
R-P1•1Ø1	4.Ø
R-P2•1ØØ	48.Ø
R-P2•1Ø1	4.Ø
R-P3•1ØØ	48.Ø
R-P3•1Ø1	4.Ø
R-SERIAL•1ØØ	44.Ø
R-SERSHT•ØØØ	41.Ø
R-SERSHT•1ØØ	41.Ø
R-SRI-A•1ØØ	17.Ø
R-SRI-B•1ØØ	18.Ø
R-SRI-C•1ØØ	18.Ø
R-SRI-D•1ØØ	19.Ø
R-SYNC•ØØØ	43.Ø
R-SYNC•11Ø	43.Ø

SIGNAL NAME	PAGE
R-SYNC1•11Ø	43.Ø
R-SYNC2•11Ø	43.Ø
RC-REG-ØØ•1ØØ	36.Ø
RC-REG-ØØ•11Ø	36.Ø
RC-REG-Ø1•1ØØ	36.Ø
RC-REG-Ø1•11Ø	36.Ø
RC-REG-Ø2•1ØØ	36.Ø
RC-REG-Ø2•11Ø	36.Ø
RC-REG-Ø3•1ØØ	36.Ø
RC-REG-Ø3•11Ø	36.Ø
RC-REG-Ø4•1ØØ	36.Ø
RC-REG-Ø4•11Ø	36.Ø
RC-REG-Ø5•1ØØ	36.Ø
RC-REG-Ø5•11Ø	36.Ø
RC-REG-Ø6•1ØØ	36.Ø
RC-REG-Ø6•11Ø	37.Ø
RC-REG-Ø7•1ØØ	36.Ø
RC-REG-Ø7•11Ø	37.Ø
RC-REG-P•1ØØ	36.Ø
RC-REG-P•11Ø	37.Ø
RCIR-MODE•Ø1Ø	47.Ø
RCIR-MODE•1ØØ	47.Ø
RCIR-MODE•12Ø	47.Ø
RCOR-MODE•Ø1Ø	24.Ø
RCOR-MODE•1ØØ	24.Ø
RCOR-MODE•12Ø	24.Ø
RCOUNT1•Ø1Ø	38.Ø
RCOUNT1•1ØØ	38.Ø
RCOUNT2•Ø1Ø	38.Ø
RCOUNT2•1ØØ	38.Ø
RCOUNT3•Ø1Ø	38.Ø
RCOUNT3•1ØØ	38.Ø
RCOUNT4•ØØØ	38.Ø
RE-COR-DATA•1ØØ	35.Ø
RE-DATA•1ØØ	24.Ø
RE-RWC-DATA•1ØØ	35.Ø
RE-WØØ•1ØØ	31.Ø
RE-WØ1•1ØØ	31.Ø
RE-WØ2•1ØØ	31.Ø
RE-WØ3•1ØØ	31.Ø
RE-WØ4•1ØØ	31.Ø
RE-WØ5•1ØØ	31.Ø
RE-WØ6•1ØØ	31.Ø
RE-WØ7•1ØØ	31.Ø
RE-WØ8•1ØØ	31.Ø
RE-WØ9•1ØØ	31.Ø
RE-W1Ø•1ØØ	31.Ø
RE-W11•1ØØ	31.Ø
RE-W12•1ØØ	31.Ø
RE-W13•1ØØ	31.Ø
RE-W14•1ØØ	31.Ø
RE-W15•1ØØ	31.Ø
RE-W16•1ØØ	31.Ø
RE-W17•1ØØ	31.Ø
RE-W18•1ØØ	31.Ø
RE-W19•1ØØ	31.Ø
RE-W2Ø•1ØØ	31.Ø

DISTRIBUTION CODE C12Ø-26

HONEYWELL
LOC CEO HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAEI
LOGIC -
PAGE CROSS REFERENCE

ASM REF 58Ø7591Ø-XØ4 | DATA BASE NIODAU/DAU$45/HEI | DR DFTG 84OCT2Ø

SIZE	DWG NO	SH	REV
B	58Ø75914	1.3	B

58Ø75914

REV	AUTHORITY	DATE
B	PHAOXS582	84OCT20

SIGNAL NAME	PAGE
RE-W21•100	31.0
RE-W22•100	31.0
RE-W23•100	31.0
RE-X20•010	28.0
RE-X20•100	28.0
RE-X21•010	28.0
RE-X21•100	28.0
RE-X23•100	28.0
RO-COR-DATA•100	35.0
RO-DATA•100	25.0
RO-RWC-DATA•100	35.0
RO-W00•100	32.0
RO-W01•100	32.0
RO-W02•100	32.0
RO-W03•100	32.0
RO-W04•100	32.0
RO-W05•100	32.0
RO-W06•100	32.0
RO-W07•100	32.0
RO-W08•100	32.0
RO-W09•100	32.0
RO-W10•100	32.0
RO-W11•100	32.0
RO-W12•100	32.0
RO-W13•100	32.0
RO-W14•100	32.0
RO-W15•100	32.0
RO-W16•100	32.0
RO-W17•100	32.0
RO-W18•100	32.0
RO-W19•100	32.0
RO-W20•100	32.0
RO-W21•100	32.0
RO-W22•100	32.0
RO-W23•100	32.0
RO-X20•010	30.0
RO-X20•100	30.0
RO-X21•010	30.0
RO-X21•100	30.0
RO-X23•100	30.0
RSB-REG-0•100	40.0
RSB-REG-1•100	40.0
RSB-REG-2•100	40.0
RSB-REG-3•100	40.0
RSB-REG-4•100	41.0
RSB-REG-5•100	41.0
RSB-REG-6•100	41.0
RSB-REG-7•100	41.0
RSB-REG-P•100	41.0
S-DIN-1•100	40.0
S-DIN-2•100	40.0
S-EDAC-0•100	34.0
S-EDAC-1•100	34.0
S-EDAC-2•100	34.0
S-SYNC•100	40.0
SEDC-4-CN•110	34.0
SEDC-4-DT•020	44.0
SEDC-4-DT•110	44.0
SEDC-4-DT•130	44.0
SEDC-5-512•020	23.0
SEDC-5-512•110	23.0
SEDC-5-64•020	23.0
SEDC-5-64•110	23.0
SEDC-5-C0•020	23.0
SEDC-5-C0•110	23.0

SIGNAL NAME	PAGE
SEDC-5-CN•020	23.0
SEDC-5-CN•110	23.0
SEL-12•100	34.0
SEL-13•100	34.0
SEL-14•100	34.0
SEL-I-D10•100	19.0
SEL-I-D11•100	19.0
SEL-I-D12•100	19.0
SEL-I-D13•100	19.0
SEL-I-D14•100	19.0
SEL-I-D15•100	20.0
SEL-I-D16•100	20.0
SEL-I-D17•100	20.0
SEL-I-D1P•100	19.0
SEL-I-FLT•100	20.0
SEL-I-IDX•100	20.0
SEL-I-OPI•100	20.0
SEL-I-SRI•100	20.0
SEQ-STATE-5•110	34.0
SEQ-STATE-6•110	34.0
SEQ-STATE-7•110	34.0
TEST-RESET•000	47.0

58075914

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HONEYWELL
LOC CEO HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAEI LOGIC - PAGE CROSS REFERENCE

ASM REF	DATA BASE / DR	SIZE	DWG NO	SH	REV
58075910-X04	NIODAU/DAU$45/HEI / DFTG 84OCT20	B	58075914	1.4	B

I/O PIN		PAGE	SIGNAL NAME
LAØØ	O	5.Ø	I-OPO-C-1SØ•1ØØ
LAØ1	O	5.Ø	I-DCP-C-1SØ•1ØØ
LAØ3	O	5.Ø	I-DCS-C-1SØ•1ØØ
LAØ4	O	5.Ø	I-DCØ-C-1SØ•1ØØ
LAØ6	O	5.Ø	I-DC1-C-1SØ•1ØØ
LAØ7	O	5.Ø	I-DC2-C-1SØ•1ØØ
LAØ9	O	5.Ø	I-DC3-C-1SØ•1ØØ
LA1Ø	O	5.Ø	I-DC4-C-1SØ•1ØØ
LA12	O	5.Ø	I-DC5-C-1SØ•1ØØ
LA13	O	5.Ø	I-DIN-C-1SØ•1ØØ
LA18	I	18.Ø	I-IDX-C-1SØ•1ØØ
LA19	I	18.Ø	I-OPI-C-1SØ•1ØØ
LA21	I	15.Ø	EN-DTA-C-1SØ•1ØØ
LBØØ	O	5.Ø	I-D1P-C-1SØ•1ØØ
LBØ1	O	5.Ø	I-D1Ø-C-1SØ•1ØØ
LBØ3	O	5.Ø	I-D11-C-1SØ•1ØØ
LBØ4	O	5.Ø	I-D12-C-1SØ•1ØØ
LBØ6	O	5.Ø	I-D13-C-1SØ•1ØØ
LBØ7	O	5.Ø	I-D14-C-1SØ•1ØØ
LBØ9	O	5.Ø	I-D15-C-1SØ•1ØØ
LB1Ø	O	5.Ø	I-D16-C-1SØ•1ØØ
LB12	O	5.Ø	I-D17-C-1SØ•1ØØ
LB13	O	5.Ø	I-SWØ-C-1SØ•1ØØ
LB15	I	18.Ø	I-FLT-C-1SØ•1ØØ
LB16	O	5.Ø	I-DM1-C-1SØ•1ØØ
LB18	I	18.Ø	I-DEN-C-1SØ•1ØØ
LB19	I	18.Ø	I-SRI-C-1SØ•1ØØ
LCØØ	O	5.Ø	I-OPO-D-1SØ•1ØØ
LCØ1	O	5.Ø	I-DCP-D-1SØ•1ØØ
LCØ3	O	5.Ø	I-DCS-D-1SØ•1ØØ
LCØ4	O	5.Ø	I-DCØ-D-1SØ•1ØØ
LCØ6	O	5.Ø	I-DC1-D-1SØ•1ØØ
LCØ7	O	5.Ø	I-DC2-D-1SØ•1ØØ
LCØ9	O	5.Ø	I-DC3-D-1SØ•1ØØ
LC1Ø	O	5.Ø	I-DC4-D-1SØ•1ØØ
LC12	O	5.Ø	I-DC5-D-1SØ•1ØØ
LC13	O	5.Ø	I-DIN-D-1SØ•1ØØ
LC18	I	19.Ø	I-IDX-D-1SØ•1ØØ
LC19	I	19.Ø	I-OPI-D-1SØ•1ØØ
LC21	I	15.Ø	EN-DTA-D-1SØ•1ØØ
LDØØ	O	5.Ø	I-D1P-D-1SØ•1ØØ
LDØ1	O	5.Ø	I-D1Ø-D-1SØ•1ØØ
LDØ3	O	5.Ø	I-D11-D-1SØ•1ØØ
LDØ4	O	5.Ø	I-D12-D-1SØ•1ØØ
LDØ6	O	5.Ø	I-D13-D-1SØ•1ØØ
LDØ7	O	5.Ø	I-D14-D-1SØ•1ØØ
LDØ9	O	5.Ø	I-D15-D-1SØ•1ØØ
LD1Ø	O	5.Ø	I-D16-D-1SØ•1ØØ
LD12	O	5.Ø	I-D17-D-1SØ•1ØØ
LD13	O	5.Ø	I-SWØ-D-1SØ•1ØØ
LD15	I	19.Ø	I-FLT-D-1SØ•1ØØ
LD16	O	5.Ø	I-DM1-D-1SØ•1ØØ
LD18	I	19.Ø	I-DEN-D-1SØ•1ØØ
LD19	I	19.Ø	I-SRI-D-1SØ•1ØØ
RAØØ	O	4.Ø	I-OPO-A-1SØ•1ØØ
RAØ1	O	4.Ø	I-DCP-A-1SØ•1ØØ
RAØ3	O	4.Ø	I-DCS-A-1SØ•1ØØ
RAØ4	O	4.Ø	I-DCØ-A-1SØ•1ØØ
RAØ6	O	4.Ø	I-DC1-A-1SØ•1ØØ
RAØ7	O	4.Ø	I-DC2-A-1SØ•1ØØ
RAØ9	O	4.Ø	I-DC3-A-1SØ•1ØØ
RA1Ø	O	4.Ø	I-DC4-A-1SØ•1ØØ
RA12	O	4.Ø	I-DC5-A-1SØ•1ØØ
RA13	O	4.Ø	I-DIN-A-1SØ•1ØØ
RA18	I	17.Ø	I-IDX-A-1SØ•1ØØ

I/O PIN		PAGE	SIGNAL NAME
RA19	I	18.Ø	I-OPI-A-1SØ•1ØØ
RA21	I	14.Ø	EN-DTA-A-1SØ•1ØØ
RBØØ	O	4.Ø	I-D1P-A-1SØ•1ØØ
RBØ1	O	4.Ø	I-D1Ø-A-1SØ•1ØØ
RBØ3	O	4.Ø	I-D11-A-1SØ•1ØØ
RBØ4	O	4.Ø	I-D12-A-1SØ•1ØØ
RBØ6	O	4.Ø	I-D13-A-1SØ•1ØØ
RBØ7	O	4.Ø	I-D14-A-1SØ•1ØØ
RBØ9	O	4.Ø	I-D15-A-1SØ•1ØØ
RB1Ø	O	4.Ø	I-D16-A-1SØ•1ØØ
RB12	O	4.Ø	I-D17-A-1SØ•1ØØ
RB13	O	4.Ø	I-SWØ-A-1SØ•1ØØ
RB15	I	17.Ø	I-FLT-A-1SØ•1ØØ
RB16	O	4.Ø	I-DM1-A-1SØ•1ØØ
RB18	I	18.Ø	I-DEN-A-1SØ•1ØØ
RB19	I	17.Ø	I-SRI-A-1SØ•1ØØ
RCØØ	O	4.Ø	I-OPO-B-1SØ•1ØØ
RCØ1	O	4.Ø	I-DCP-B-1SØ•1ØØ
RCØ3	O	4.Ø	I-DCS-B-1SØ•1ØØ
RCØ4	O	4.Ø	I-DCØ-B-1SØ•1ØØ
RCØ6	O	4.Ø	I-DC1-B-1SØ•1ØØ
RCØ7	O	4.Ø	I-DC2-B-1SØ•1ØØ
RCØ9	O	4.Ø	I-DC3-B-1SØ•1ØØ
RC1Ø	O	4.Ø	I-DC4-B-1SØ•1ØØ
RC12	O	4.Ø	I-DC5-B-1SØ•1ØØ
RC13	O	4.Ø	I-DIN-B-1SØ•1ØØ
RC18	I	18.Ø	I-IDX-B-1SØ•1ØØ
RC19	I	18.Ø	I-OPI-B-1SØ•1ØØ
RC21	I	15.Ø	EN-DTA-B-1SØ•1ØØ
RDØØ	O	4.Ø	I-D1P-B-1SØ•1ØØ
RDØ1	O	5.Ø	I-D1Ø-B-1SØ•1ØØ
RDØ3	O	5.Ø	I-D11-B-1SØ•1ØØ
RDØ4	O	5.Ø	I-D12-B-1SØ•1ØØ
RDØ6	O	5.Ø	I-D13-B-1SØ•1ØØ
RDØ7	O	5.Ø	I-D14-B-1SØ•1ØØ
RDØ9	O	4.Ø	I-D15-B-1SØ•1ØØ
RD1Ø	O	5.Ø	I-D16-B-1SØ•1ØØ
RD12	O	5.Ø	I-D17-B-1SØ•1ØØ
RD13	O	4.Ø	I-SWØ-B-1SØ•1ØØ
RD15	I	18.Ø	I-FLT-B-1SØ•1ØØ
RD16	O	5.Ø	I-DM1-B-1SØ•1ØØ
RD18	I	18.Ø	I-DEN-B-1SØ•1ØØ
RD19	I	18.Ø	I-SRI-B-1SØ•1ØØ
WAØØ	O	36.Ø	RC-REG-ØØ•11Ø
WAØ2	O	36.Ø	RC-REG-Ø1•11Ø
WAØ3	O	36.Ø	RC-REG-Ø2•11Ø
WAØ4	O	36.Ø	RC-REG-Ø3•11Ø
WAØ5	O	36.Ø	RC-REG-Ø4•11Ø
WAØ6	O	36.Ø	RC-REG-Ø5•11Ø
WAØ7	O	37.Ø	RC-REG-Ø6•11Ø
WAØ8	O	37.Ø	RC-REG-Ø7•11Ø
WAØ9	O	37.Ø	RC-REG-P•11Ø
WA1Ø	O	4.Ø	DZERO-COUNT•ØØ1
WA12	O	4.Ø	D-EDAC-ERROR•1Ø1
WA19	I	21.Ø	ENABLE-SENSE•1ØØ
WA2Ø	I	21.Ø	ENABLE-OPI•1ØØ
WBØØ	I	22.Ø	FCMD-DCP-ØSØ•1ØØ
WBØ1	I	23.Ø	FCMD-DCØ-ØSØ•1ØØ
WBØ2	I	23.Ø	FCMD-DC1-ØSØ•1ØØ
WBØ3	I	23.Ø	FCMD-DC2-ØSØ•1ØØ
WBØ4	I	23.Ø	FCMD-DC3-ØSØ•1ØØ
WBØ5	I	23.Ø	FCMD-DC4-ØSØ•1ØØ
WBØ6	I	23.Ø	FCMD-DC5-ØSØ•1ØØ
WBØ7	I	23.Ø	FCMD-DCS-ØSD•1ØØ
WB1Ø	I	13.Ø	DDAI-INIT-ØS1•1ØØ

I/O PIN		PAGE	SIGNAL NAME
WB12	I	22.Ø	DINIT-DIN-ØSØ•1ØØ
WB13	I	13.Ø	POWER-CONF•1ØØ
WB15	I	21.Ø	DRD-FR-DEV-ØSØ•1ØØ
WB19	I	21.Ø	DCOUNT-OUT-ØSØ•1ØØ
WCØØ	I	23.Ø	FDTA-O-D1P-ØSØ•1ØØ
WCØ1	I	23.Ø	FDTA-O-D1Ø-ØSØ•1ØØ
WCØ2	I	23.Ø	FDTA-O-D11-ØSØ•1ØØ
WCØ3	I	23.Ø	FDTA-O-D12-ØSØ•1ØØ
WCØ4	I	23.Ø	FDTA-O-D13-ØSØ•1ØØ
WCØ5	I	23.Ø	FDTA-O-D14-ØSØ•1ØØ
WCØ6	I	23.Ø	FDTA-O-D15-ØSØ•1ØØ
WCØ7	I	23.Ø	FDTA-O-D16-ØSØ•1ØØ
WCØ8	I	23.Ø	FDTA-O-D17-ØSØ•1ØØ
WCØ9	I	22.Ø	FDTA-M-DM1-ØSØ•1ØØ
WC12	I	22.Ø	FDEV-SEL-2-ØSØ•1ØØ
WC13	I	22.Ø	FDEV-SEL-3-ØSØ•1ØØ
WC14	I	22.Ø	DBRD-SEL-Ø-ØSØ•1ØØ
WC2Ø	O	22.Ø	DSR-RD-SRI-ØSØ•1ØØ
WDØØ	O	21.Ø	DDTA-I-D1P-ØSØ•1ØØ
WDØ1	O	21.Ø	DDTA-I-D1Ø-ØSØ•1ØØ
WDØ2	O	21.Ø	DDTA-I-D11-ØSØ•1ØØ
WDØ3	O	21.Ø	DDTA-I-D12-ØSØ•1ØØ
WDØ4	O	22.Ø	DDTA-I-D13-ØSØ•1ØØ
WDØ5	O	22.Ø	DDTA-I-D14-ØSØ•1ØØ
WDØ6	O	22.Ø	DDTA-I-D15-ØSØ•1ØØ
WDØ7	O	22.Ø	DDTA-I-D16-ØSØ•1ØØ
WDØ8	O	22.Ø	DDTA-I-D17-ØSØ•1ØØ
WD12	O	22.Ø	DINDEX-IDX-ØSØ•1ØØ
WD13	O	22.Ø	DFAULT-FLT-ØSØ•1ØØ
WD14	O	22.Ø	DOPER-OPI-ØSØ•1ØØ
WD15	I	36.Ø	DHI1•1ØØ
WD16	I	33.Ø	D-ONE•1ØØ
WD17	O	21.Ø	DDEN-ØØ-ØSØ•1ØØ
WD18	O	21.Ø	DDEN-Ø1-ØSØ•1ØØ
WD19	O	21.Ø	DDEN-Ø2-ØSØ•1ØØ
WD2Ø	O	21.Ø	DDEN-Ø3-ØSØ•1ØØ
WEØ5	O	45.Ø	D-ED-P-ERR•1ØØ
WEØ9	I	37.Ø	$DAU•Ø11
WE1Ø	I	41.Ø	DSEL-ED•11Ø
WE12	O	35.Ø	R-EDAC-DATA-Ø•11Ø
WE13	O	35.Ø	R-EDAC-DATA-1•11Ø
WE14	O	34.Ø	R-EDAC-DATA-2•11Ø
WE15	O	34.Ø	R-EDAC-DATA-3•11Ø
WE16	O	34.Ø	R-EDAC-DATA-4•11Ø
WE17	O	34.Ø	R-EDAC-DATA-5•11Ø
WE18	O	34.Ø	R-EDAC-DATA-6•11Ø
WE19	O	34.Ø	R-EDAC-DATA-7•11Ø
WE2Ø	O	35.Ø	P-EDAC-DATA-P•1ØØ
WFØØ	I	34.Ø	$PARTIAL-CLR•Ø12
WFØ9	I	37.Ø	$DAU-TOT-CLR•Ø12
WF1Ø	I	34.Ø	SEDC-4-CN•11Ø
WF12	I	44.Ø	SEDC-4-DT•11Ø
WF13	I	23.Ø	SEDC-5-CØ•11Ø
WF14	I	23.Ø	SEDC-5-CN•11Ø
WF15	I	23.Ø	SEDC-5-64•11Ø
WF16	I	23.Ø	SEDC-5-512•11Ø
WF18	I	37.Ø	EDAC-CLEAR•13Ø

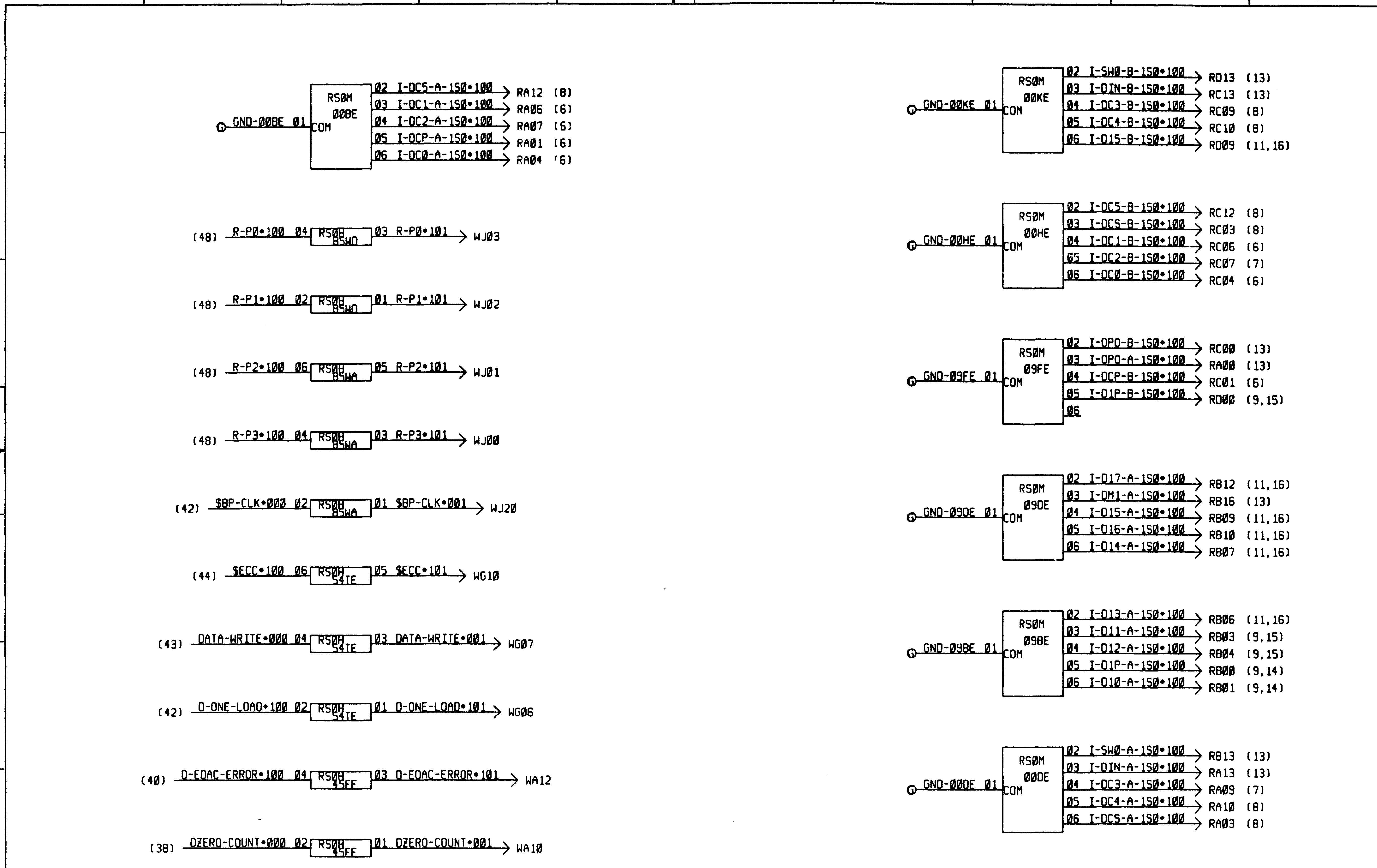
HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI I/O PIN - PAGE CROSS REFERENCE	SIZE B	DWG NO 58Ø75914	SH 3.Ø	REV B

I/O PIN		PAGE	SIGNAL NAME
WF19	I	39.0	LAST-EDAC•130
WF20	I	41.0	EDAC-BYTES•120
WF21	I	39.0	CMO-WRITE•120
WG00	I	34.0	DMPADR-15•100
WG02	I	34.0	DMPADR-14•100
WG03	I	34.0	DMPADR-13•100
WG04	I	34.0	DMPADR-12•100
WG06	O	4.0	D-ONE-LOAD•101
WG07	O	4.0	DATA-WRITE•001
WG10	O	4.0	$ECC•101
WG16	I	41.0	MPWR•120
WG19	I	47.0	MPRD•120
WH00	I	24.0	DREG-0•110
WH01	I	24.0	DREG-1•110
WH02	I	24.0	DREG-2•110
WH03	I	24.0	DREG-3•110
WH04	I	24.0	DREG-4•110
WH05	I	24.0	DREG-5•110
WH06	I	24.0	DREG-6•110
WH07	I	24.0	DREG-7•110
WH08	I	41.0	DREG-P•110
WH12	I	40.0	BREG-00•110
WH13	I	40.0	BREG-01•110
WH14	I	40.0	BREG-02•110
WH15	I	40.0	BREG-03•110
WH16	I	41.0	BREG-04•110
WH17	I	41.0	BREG-05•110
WH18	I	41.0	BREG-06•110
WH19	I	41.0	BREG-07•110
WH20	I	41.0	BREG-P•110
WJ00	O	4.0	R-P3•101
WJ01	O	4.0	R-P2•101
WJ02	O	4.0	R-P1•101
WJ03	O	4.0	R-P0•101
WJ04	O	35.0	F-EDAC-READY•110
WJ05	O	35.0	F-EDAC-ERROR•110
WJ06	I	34.0	SEQ-STATE-5•110
WJ07	I	34.0	SEQ-STATE-6•110
WJ08	I	34.0	SEQ-STATE-7•110
WJ09	I	38.0	EDAC-STB•130
WJ10	I	40.0	S-SYNC•100
WJ12	I	37.0	FB-REG-FUL•110
WJ13	I	41.0	FCREG-ACK•110
WJ14	I	39.0	D-LAST-EDAC•110
WJ15	O	43.0	DBREG-ACK•100
WJ16	O	35.0	FCREG-FULL•110
WJ19	I	47.0	TEST-RESET•000
WJ20	O	4.0	$BP-CLK•001
WK01	O	40.0	D-SW-0•100
WK02	O	40.0	D-SW-1•100
WK03	O	40.0	D-SW-2•100
WK04	O	40.0	D-SW-3•100
WK05	O	41.0	D-SW-4•100
WK06	O	41.0	D-SW-5•100
WK07	O	41.0	D-SW-6•100
WK08	O	41.0	D-SW-7•100
WK09	I	47.0	RCIR-MODE•100
WK10	I	24.0	RCOR-MODE•100
WK12	I	40.0	RSB-REG-0•100
WK13	I	40.0	RSB-REG-1•100
WK14	I	40.0	RSB-REG-2•100
WK15	I	40.0	RSB-REG-3•100
WK16	I	41.0	RSB-REG-4•100
WK17	I	41.0	RSB-REG-5•100
WK18	I	41.0	RSB-REG-6•100
WK19	I	41.0	RSB-REG-7•100
WK20	I	41.0	RSB-REG-P•100

LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAEI I/O PIN - PAGE CROSS REFERENCE

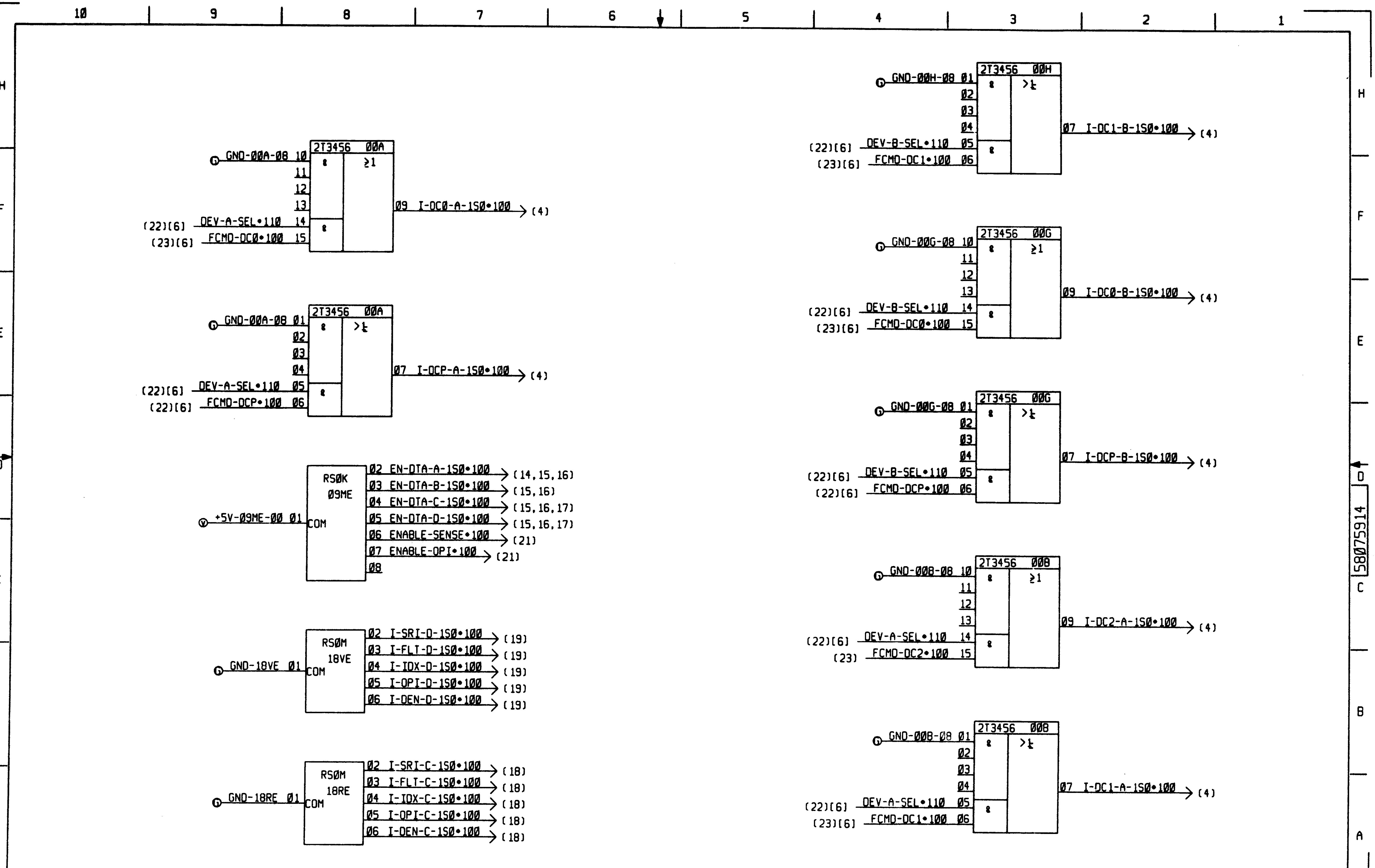
SIZE B | DWG NO 58075914 | SH 3.1 | REV B



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58Ø75914	SH 4.Ø	REV B

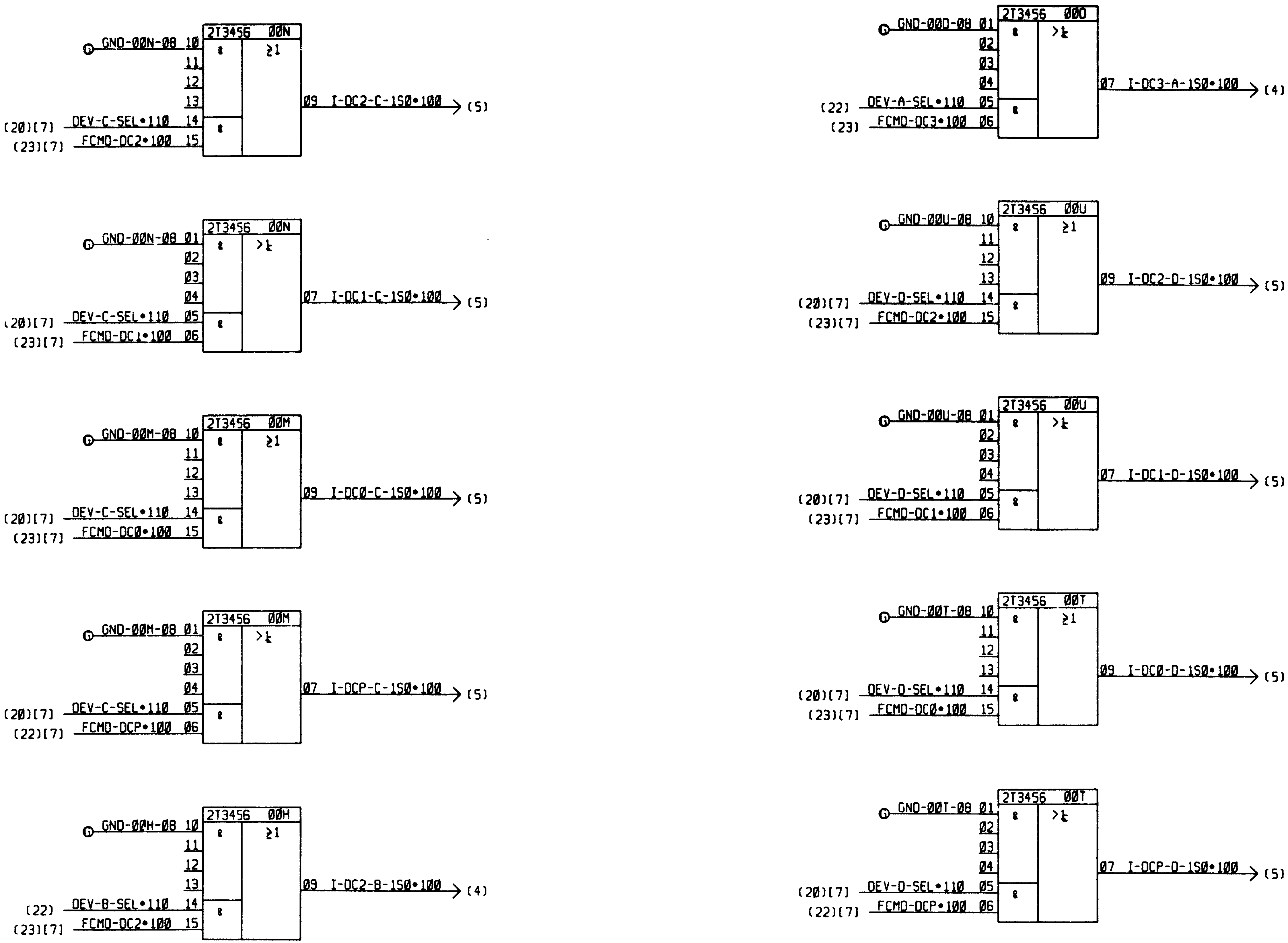
58Ø75914

LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58Ø75914	SH 5.Ø	REV B



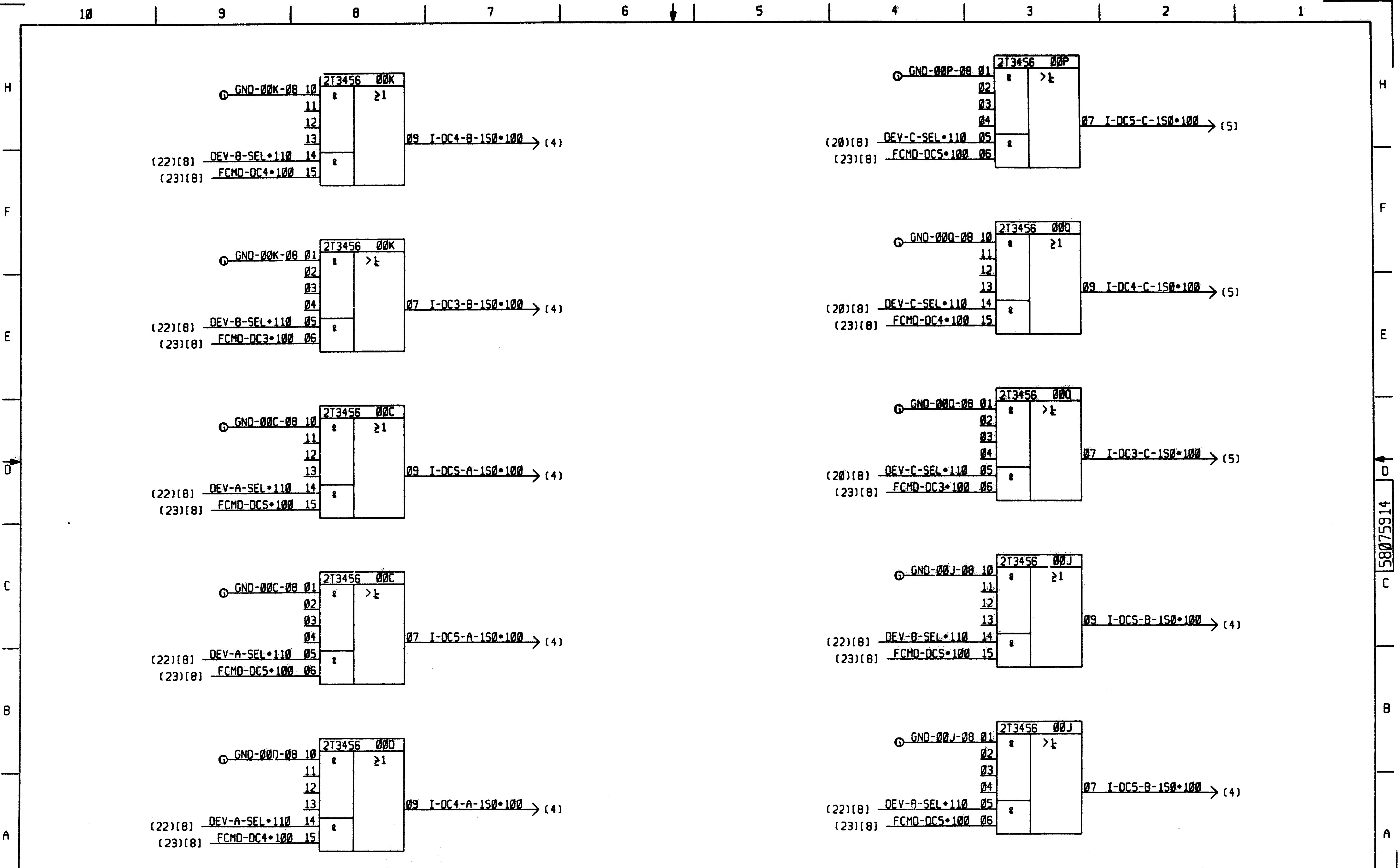
HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 6.0	REV B

58075914

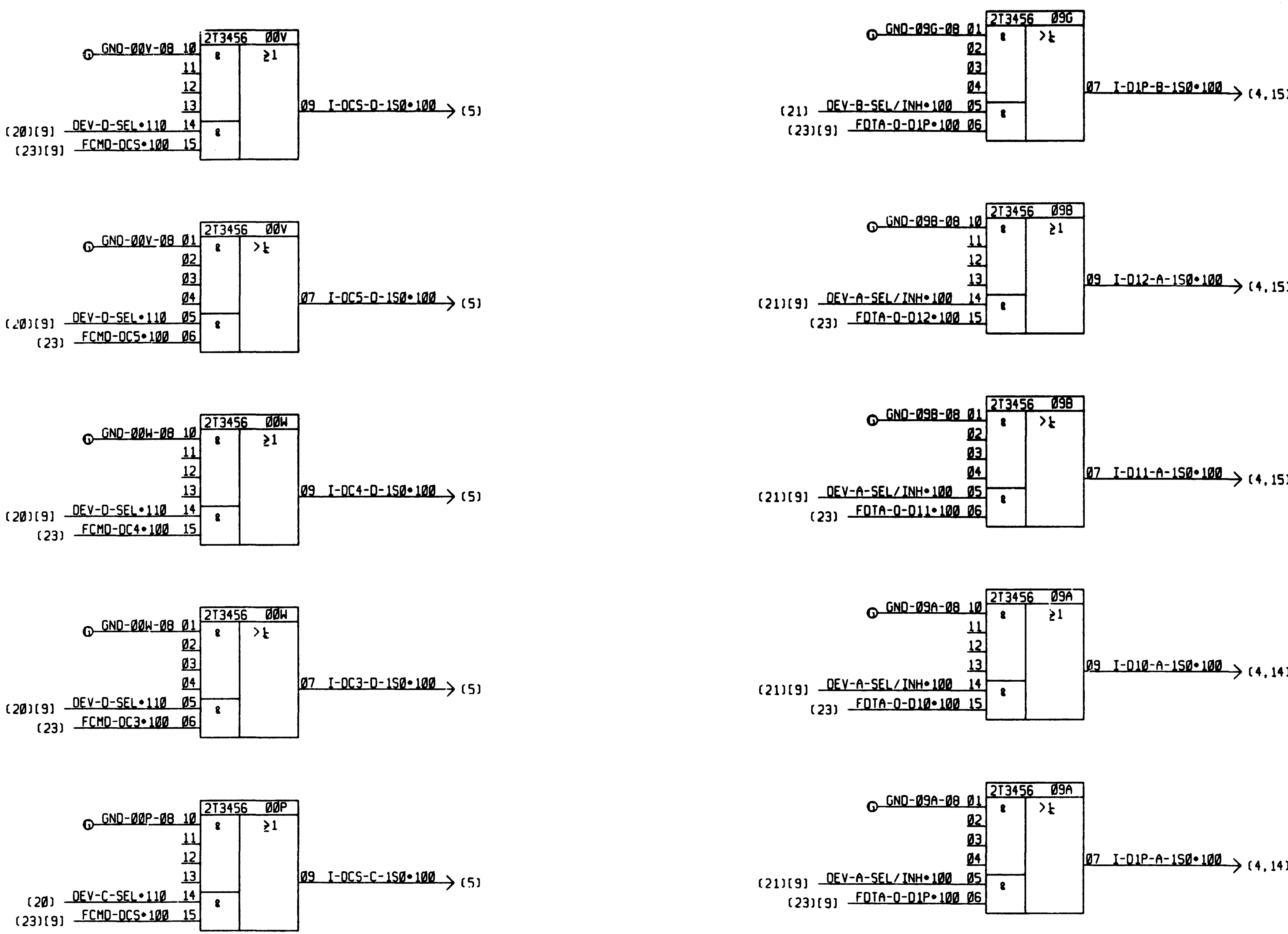


58Ø75914

LOC HONEYWELL — HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58Ø75914	SH 7.Ø	REV B

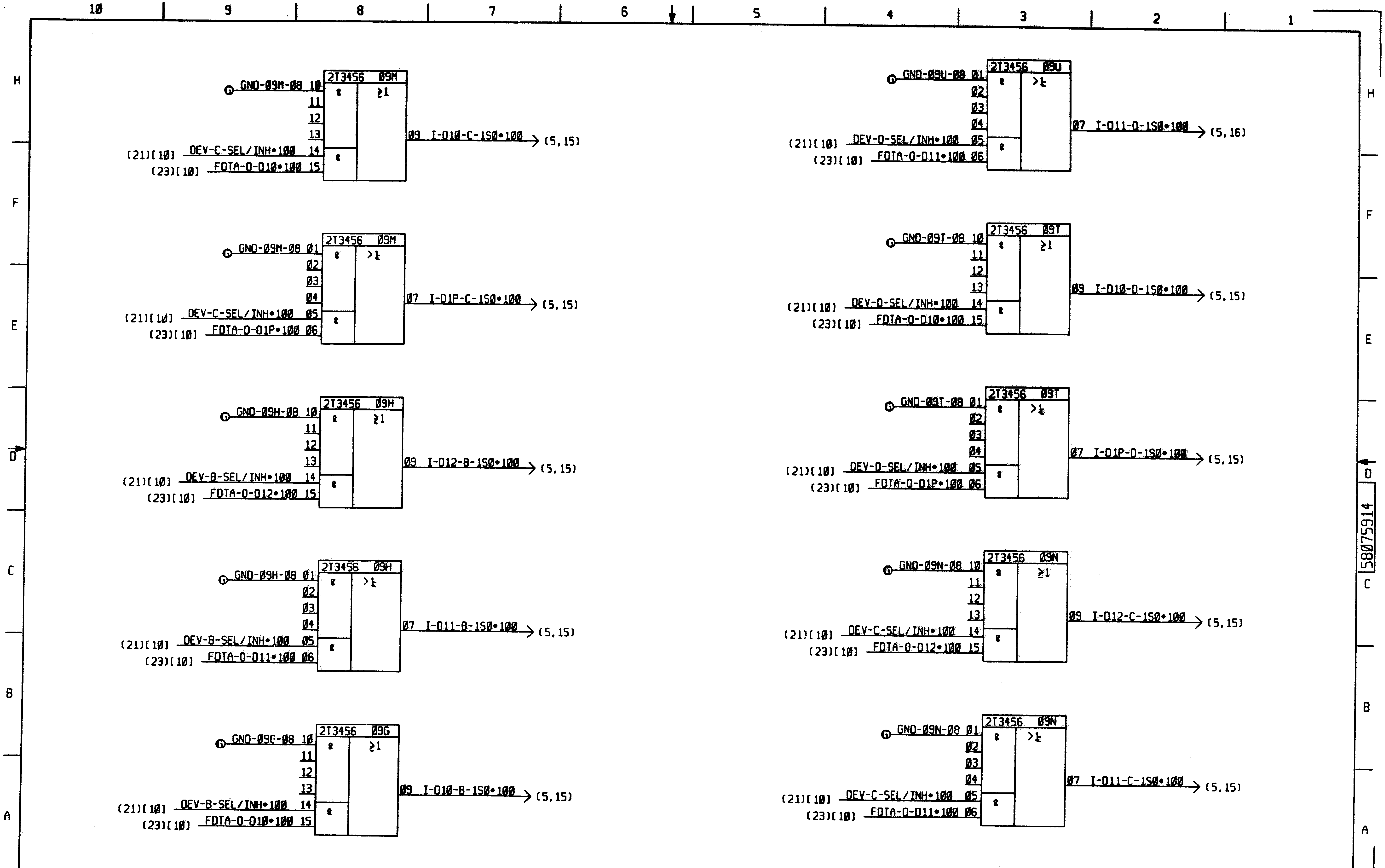


LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58Ø75914	SH 8.Ø	REV B

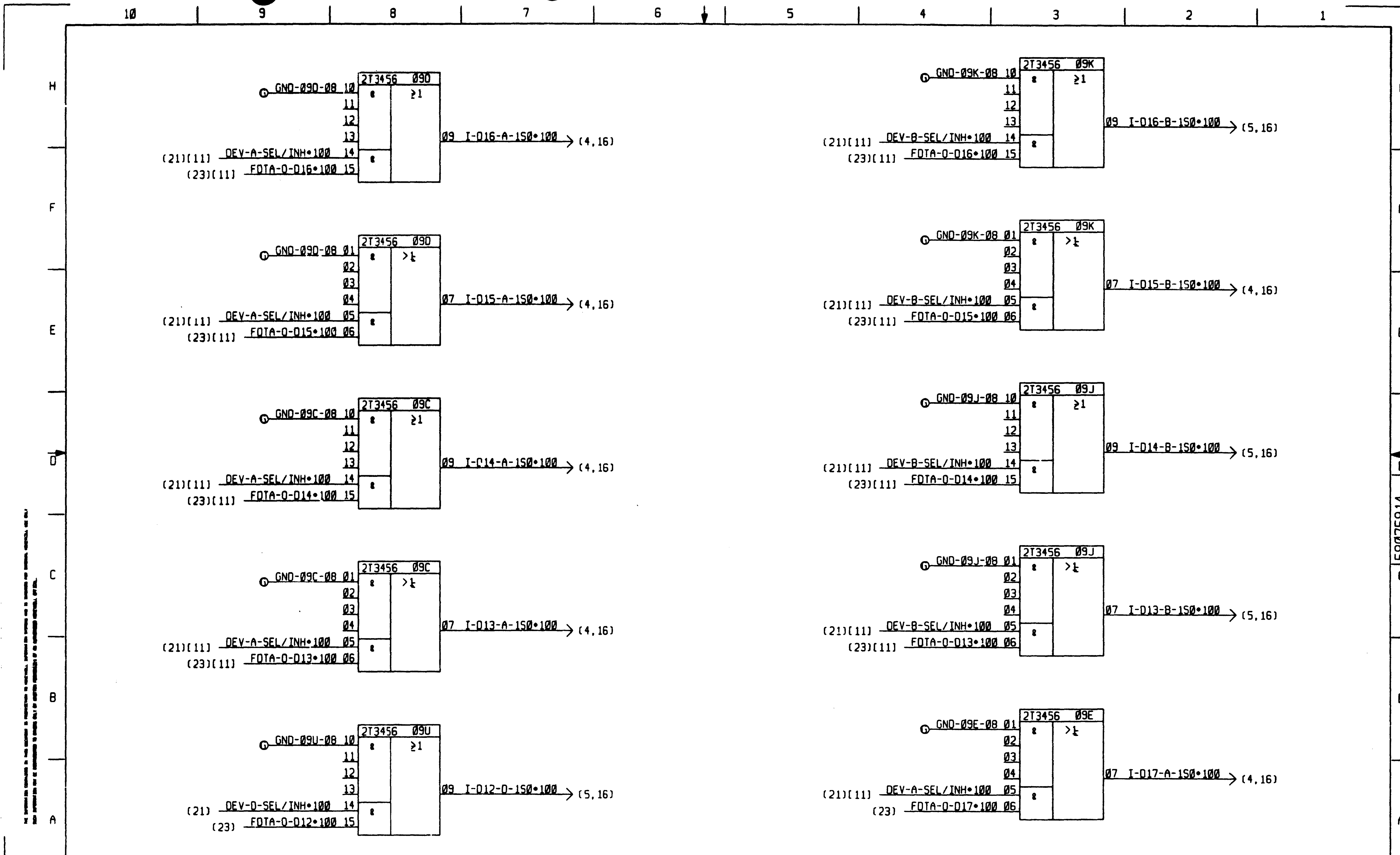


58Ø75914

LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58Ø75914	SH 9.Ø	REV B

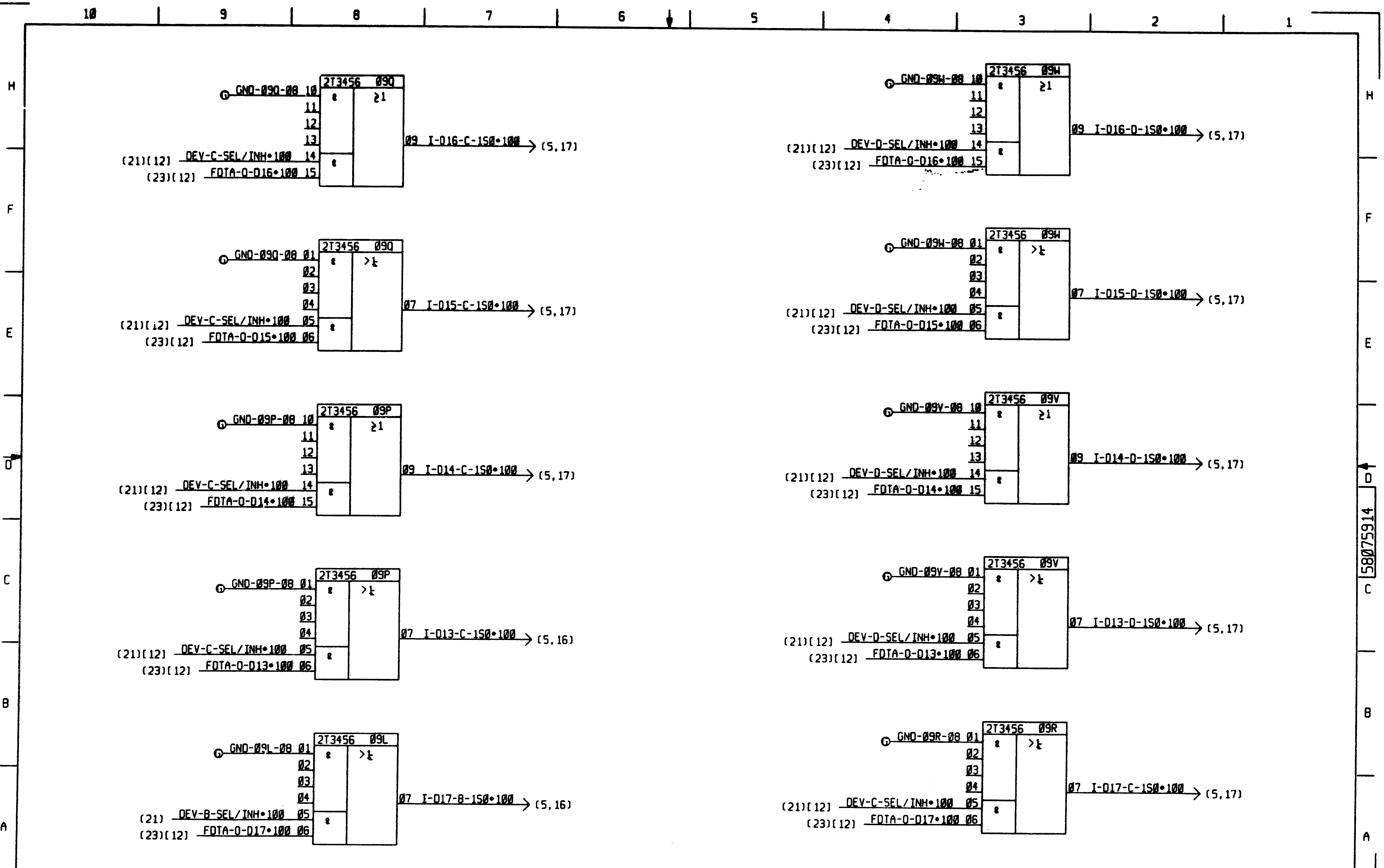


LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58Ø75914	SH 1Ø.Ø REV B

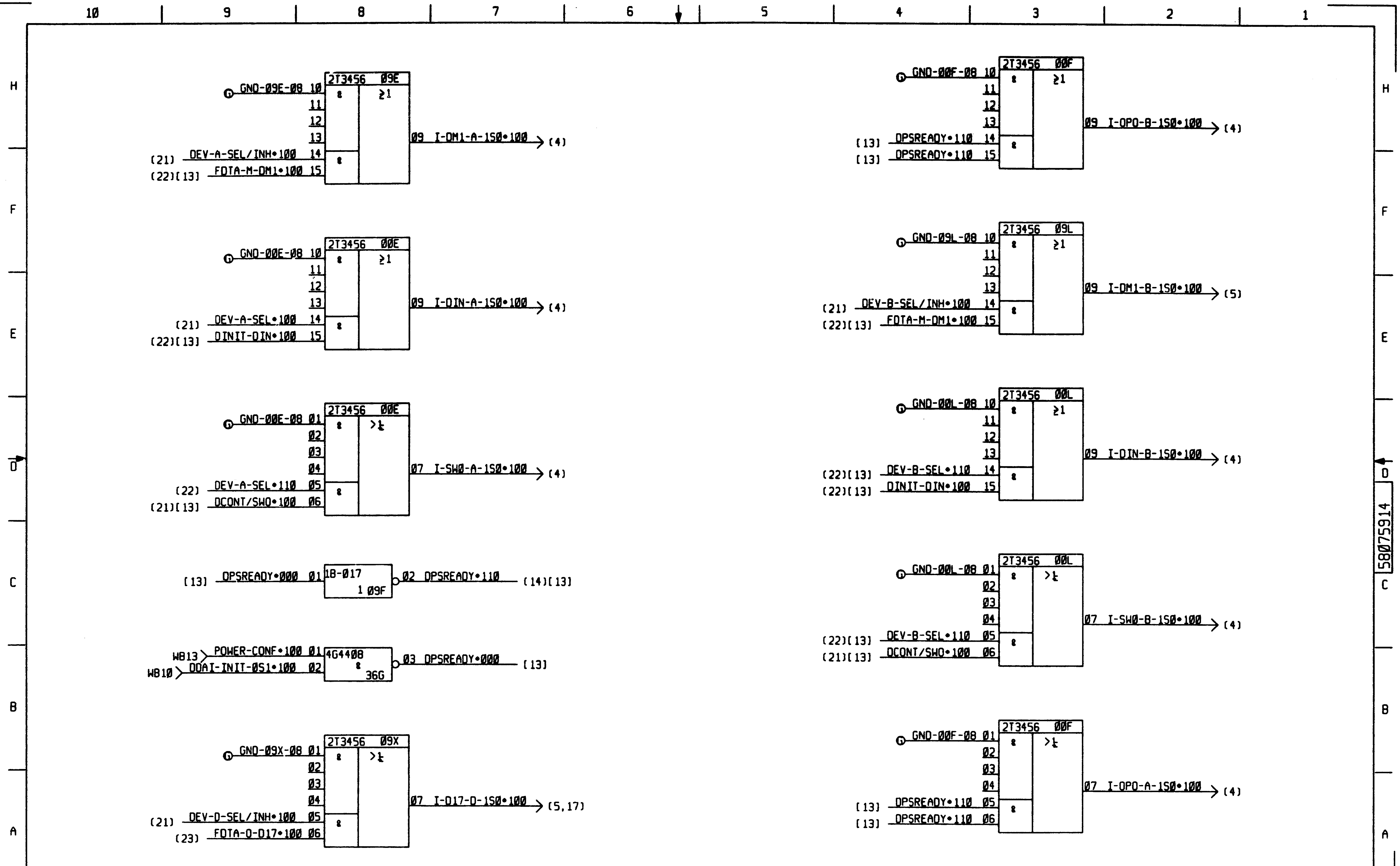


HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE	SIZE	DWG NO	SH	REV
LOGIC DIAGRAM- WDAEI	B	58075914	11.0	B



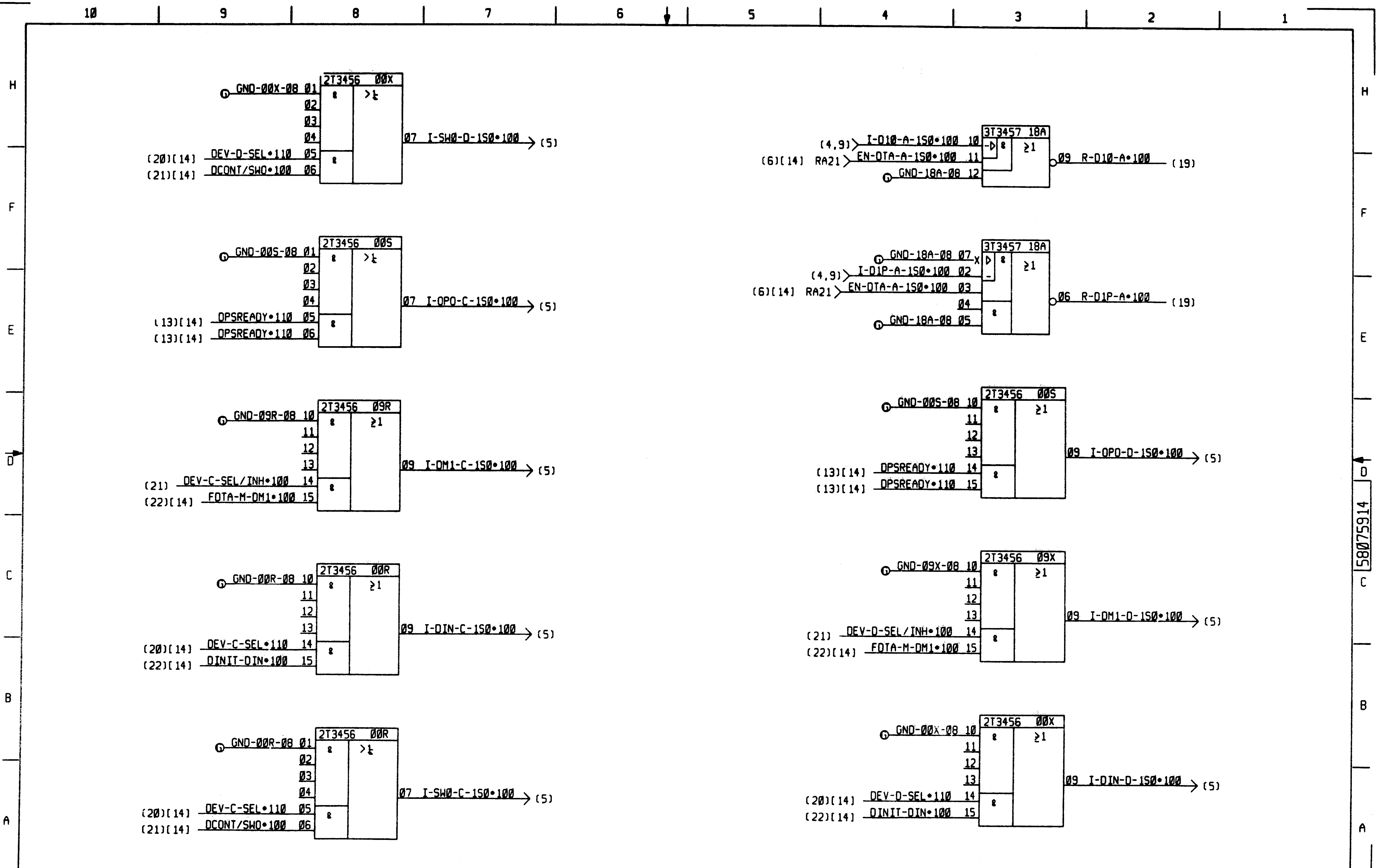
LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58Ø75914	SH 12.Ø	REV B



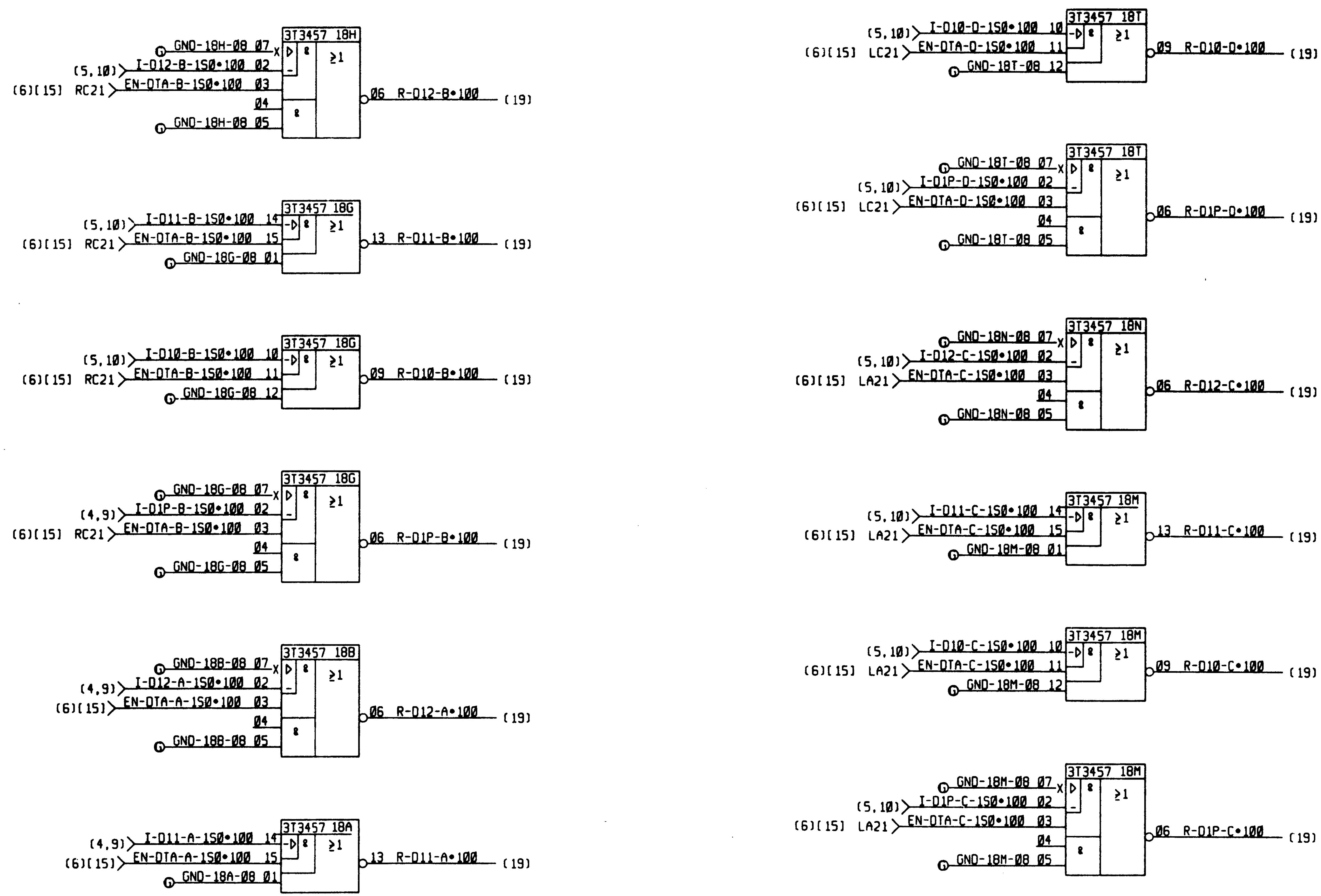
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

TITLE	SIZE	DWG NO	SH	REV
LOGIC DIAGRAM- WDAEI	B	58Ø75914	13.Ø	B



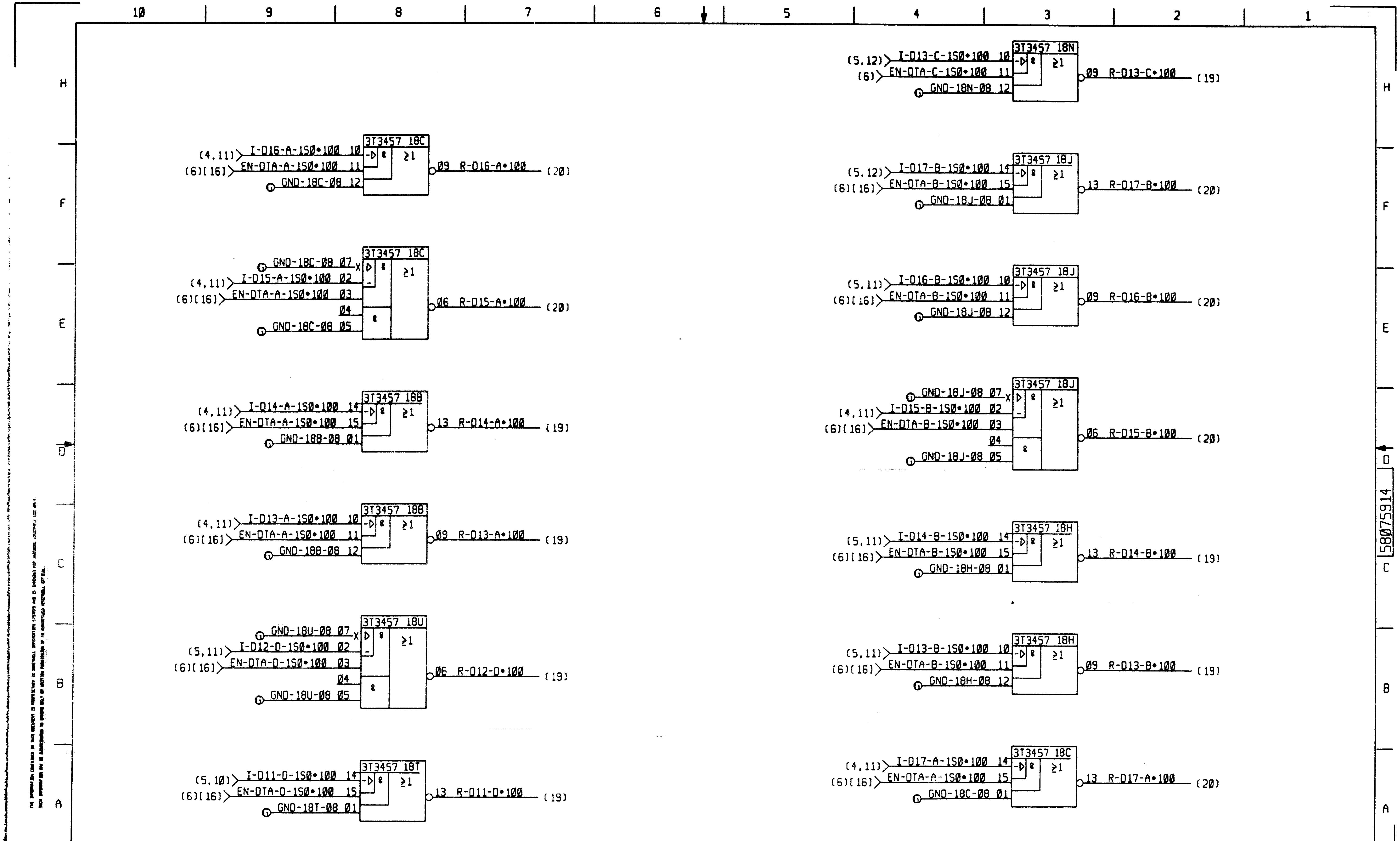
HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A. LOC	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 14.0	REV B



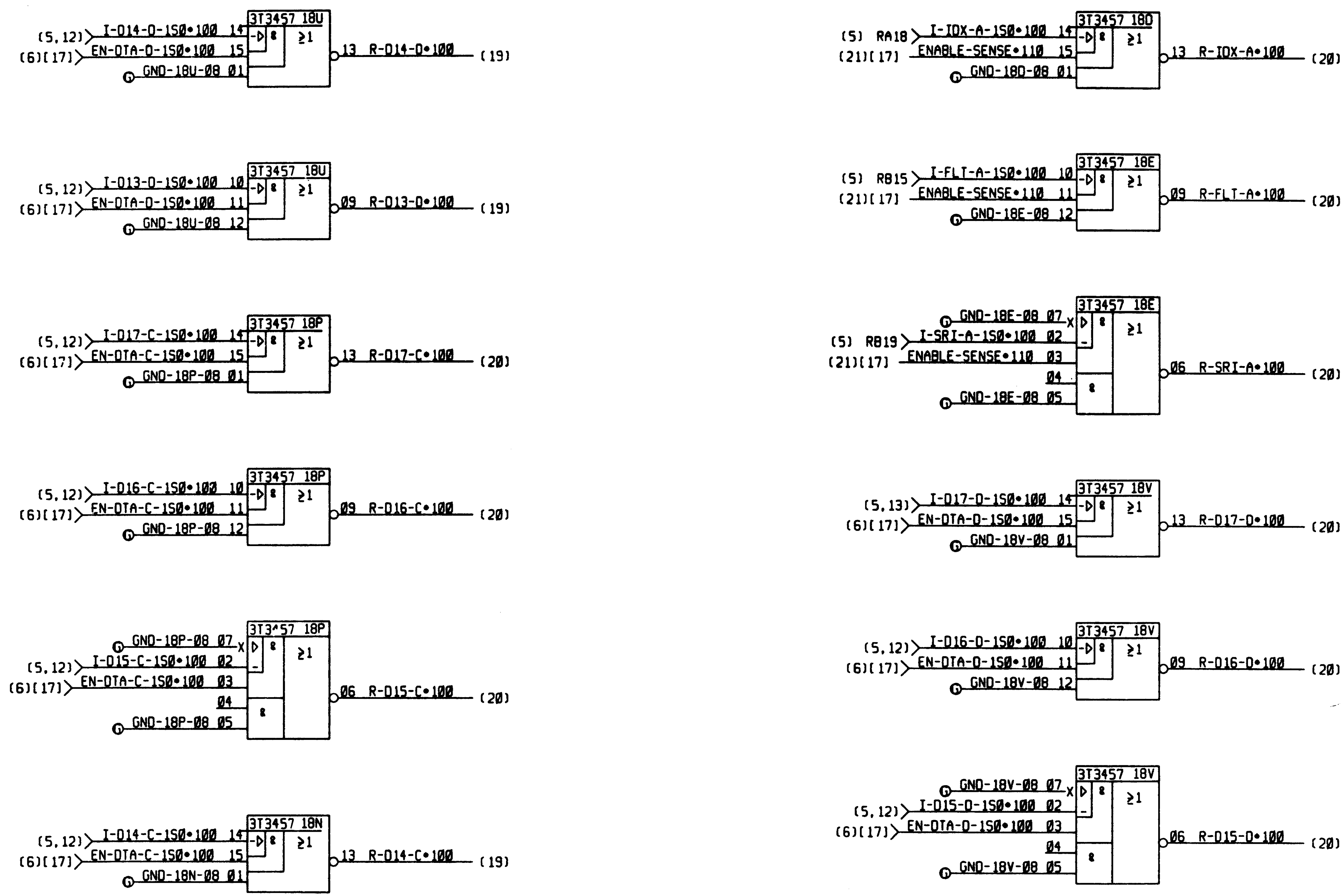
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAEI

SIZE B | DWG NO 58075914 | SH 15.0 | REV B

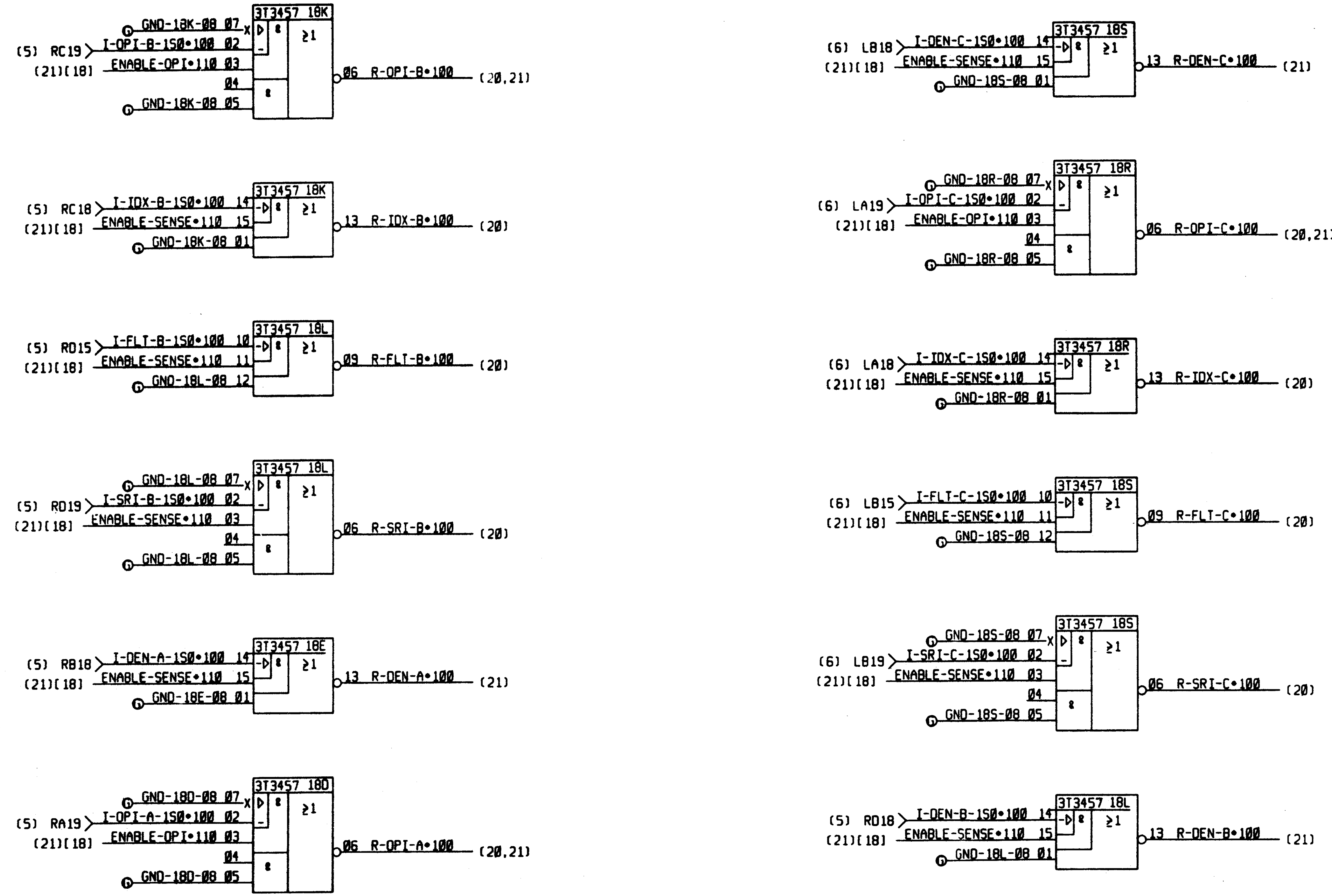


LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58Ø75914	SH 16.Ø	REV B



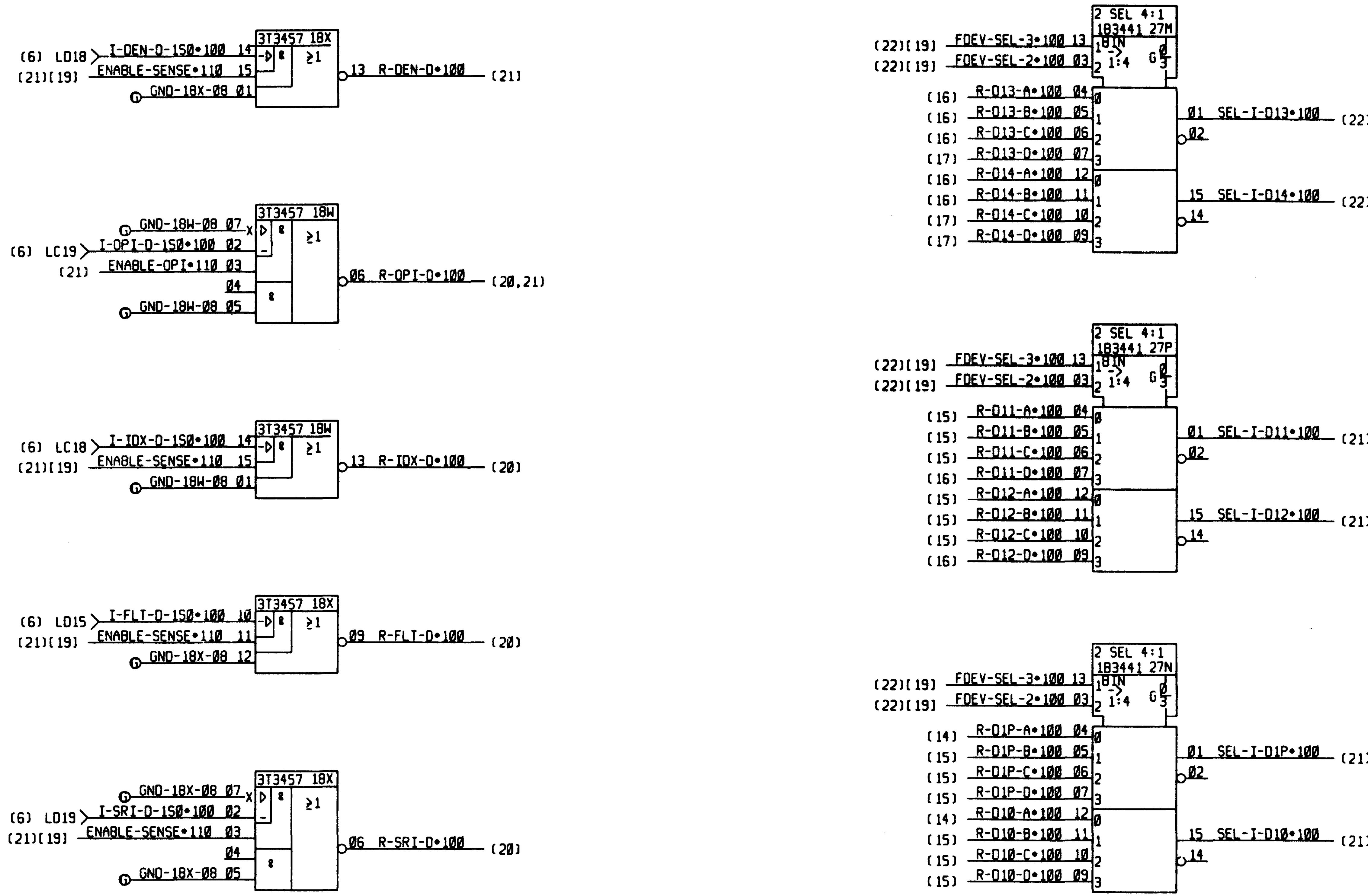
HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 17.0	REV B

58075914



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 18.0	REV B

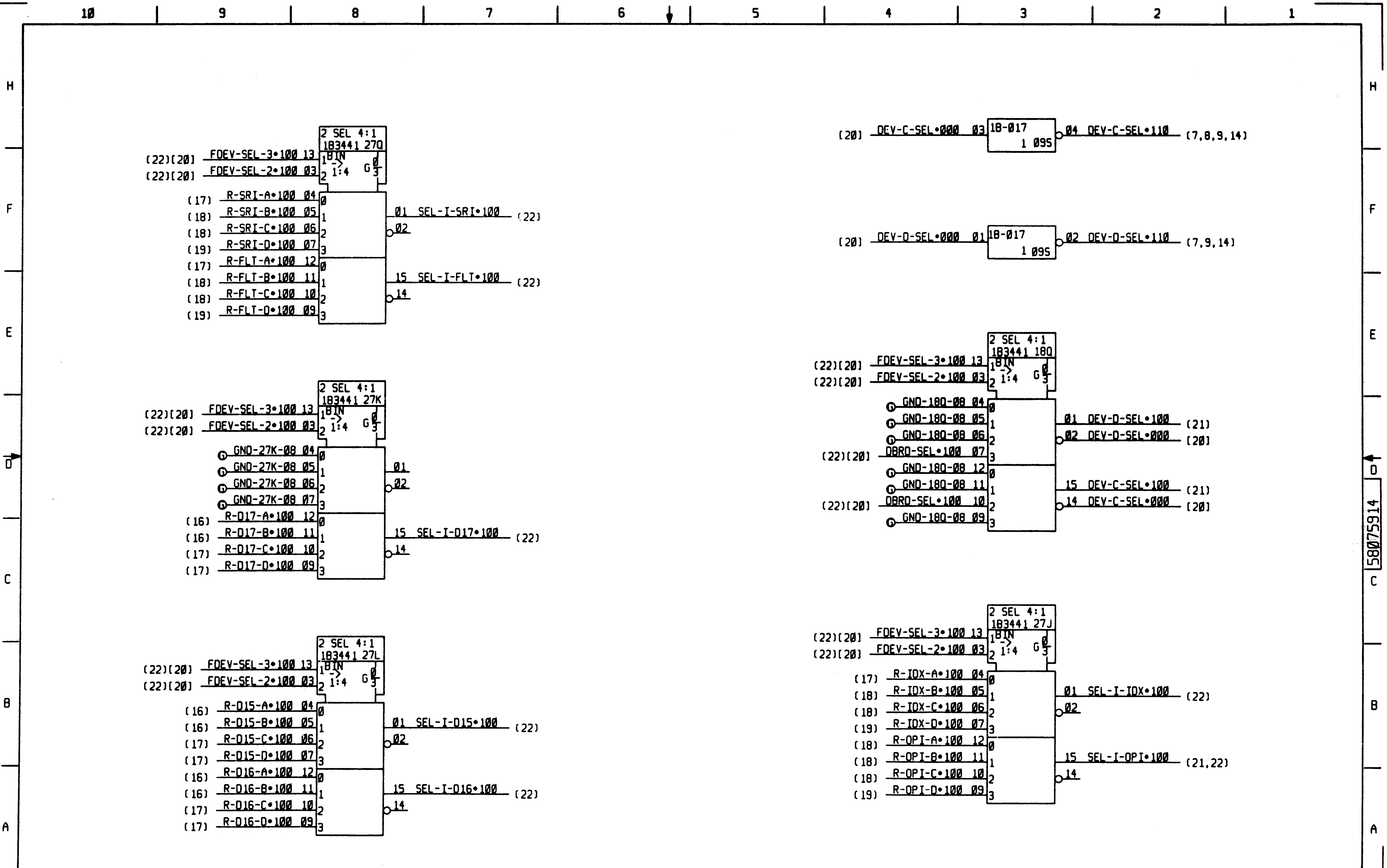
58075914



58075914

HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

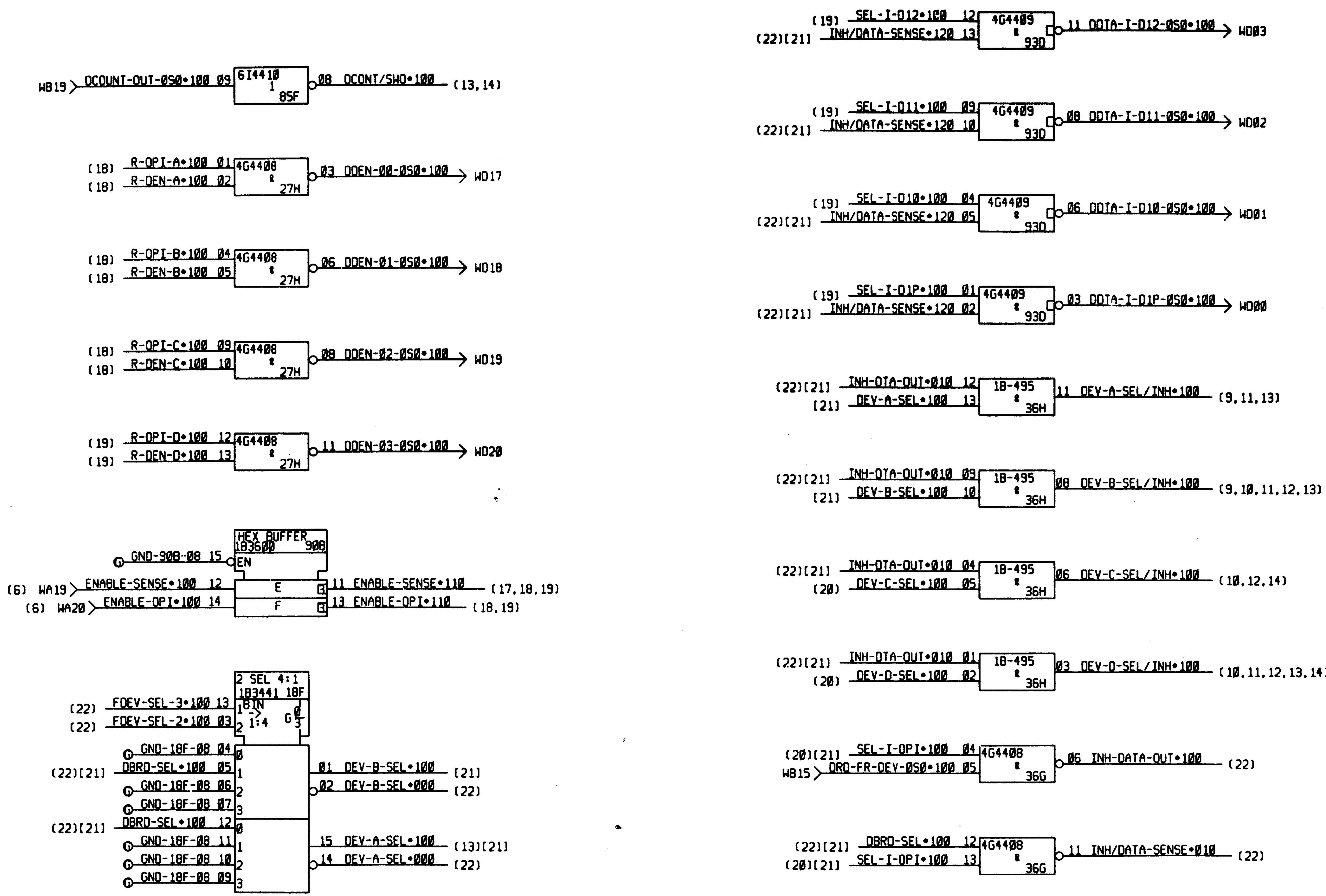
LOC | TITLE LOGIC DIAGRAM- WDAEI | SIZE B | DWG NO 58075914 | SH 19.0 | REV B



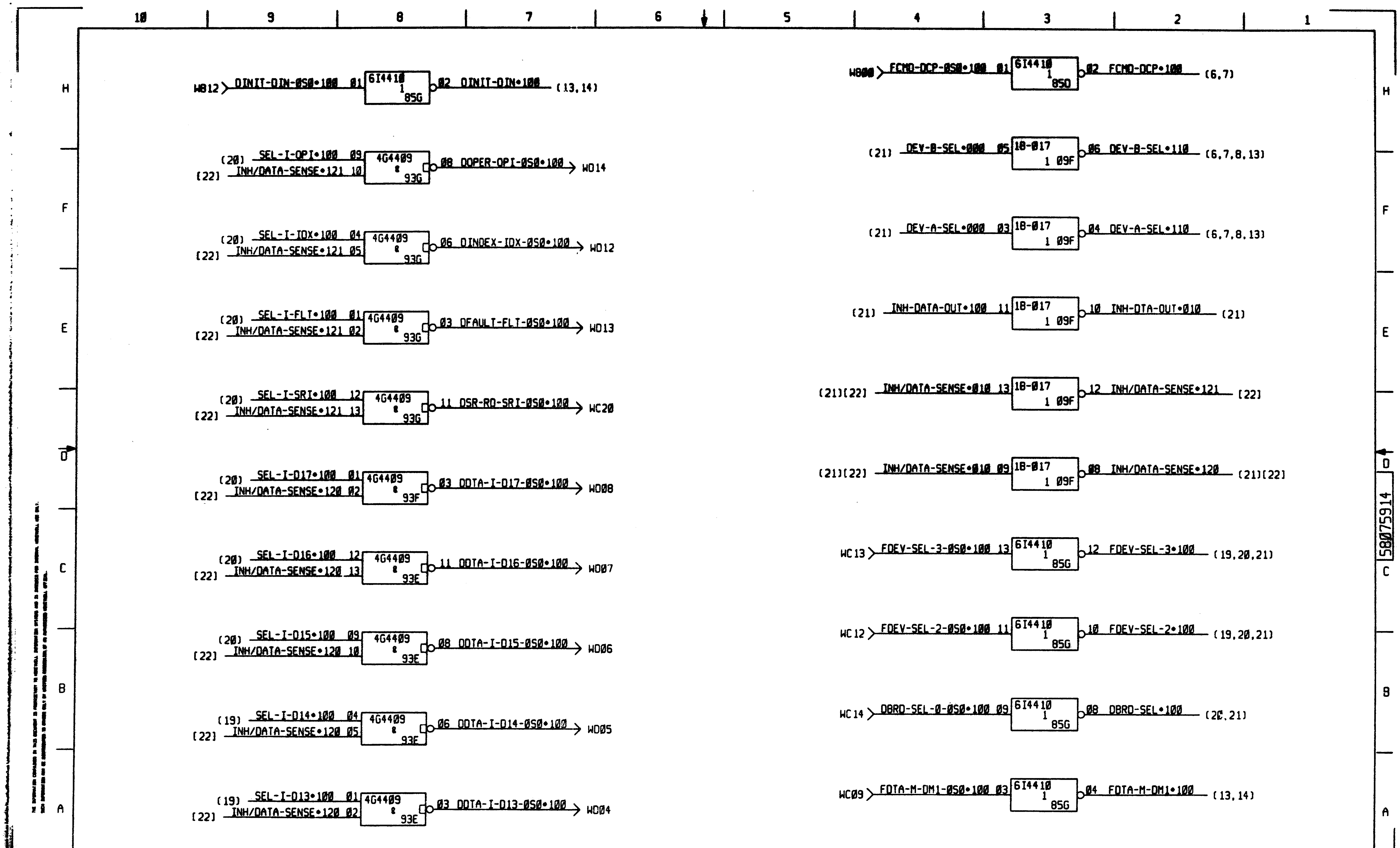
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

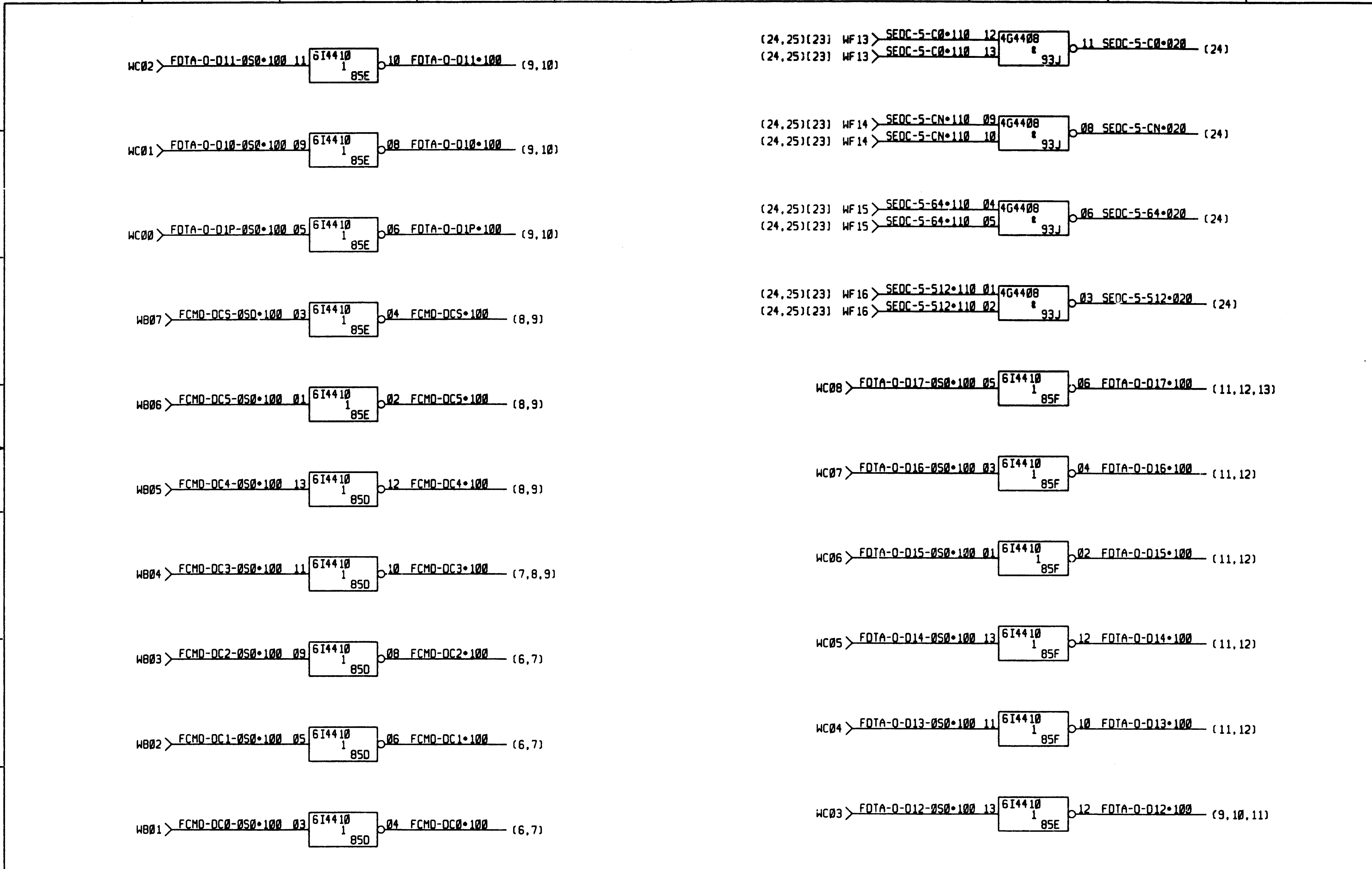
TITLE	SIZE	DWG NO	SH	REV
LOGIC DIAGRAM- WDAEI	B	58Ø75914	2Ø.Ø	B



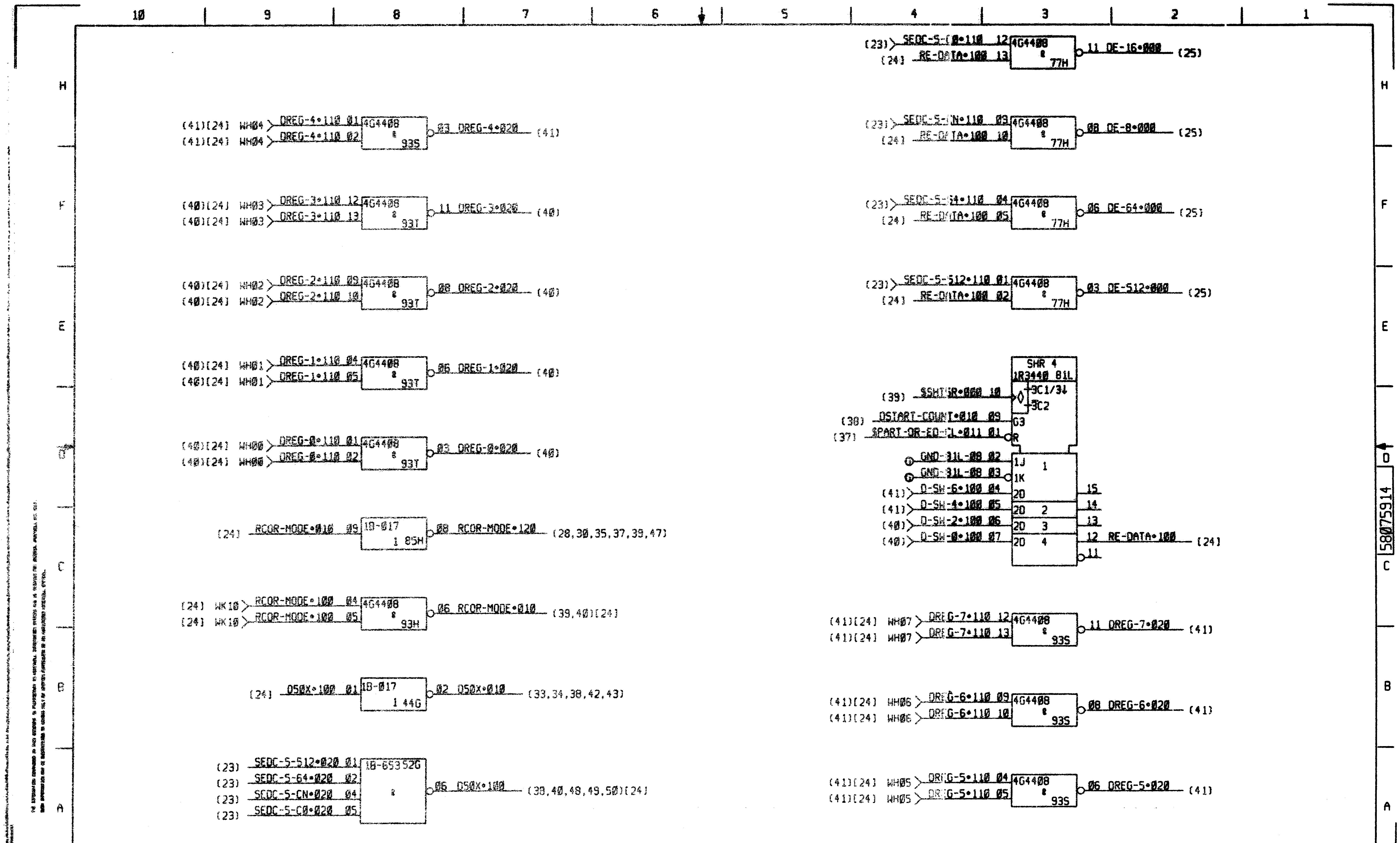
HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 21.0	REV B



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 22.0	REV B



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 23.0	REV B



HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC

TITLE LOGIC DIAGRAM- WDAEI

SIZE	DWG NO	SH	REV
B	58075914	24.0	B

HONEYWELL
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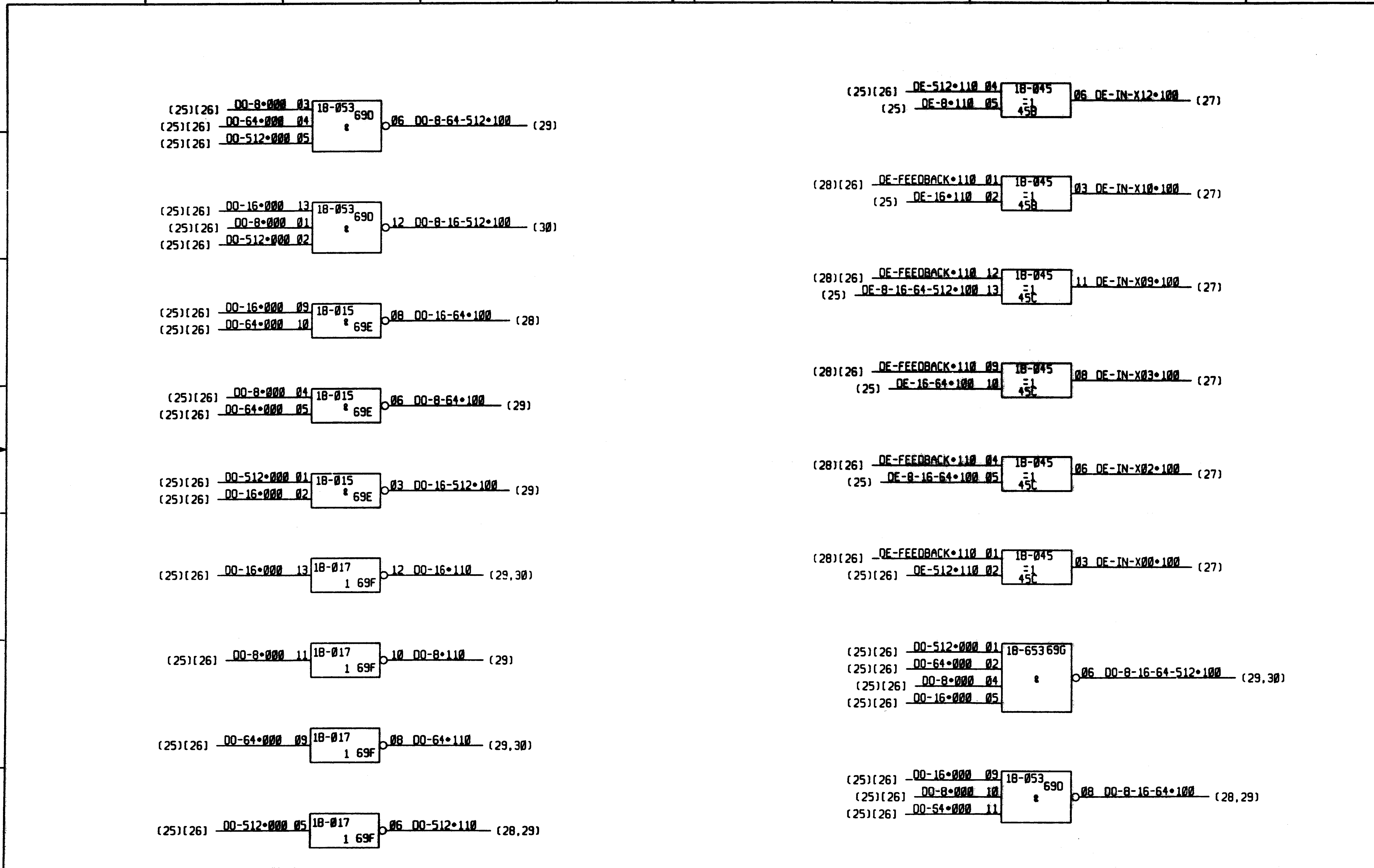
PHOENIX, ARIZONA U.S.A.
LOC

TITLE LOGIC DIAGRAM- WDAEI

SIZE	DWG NO	SH	REV
B	58075914	25.0	B

58075914



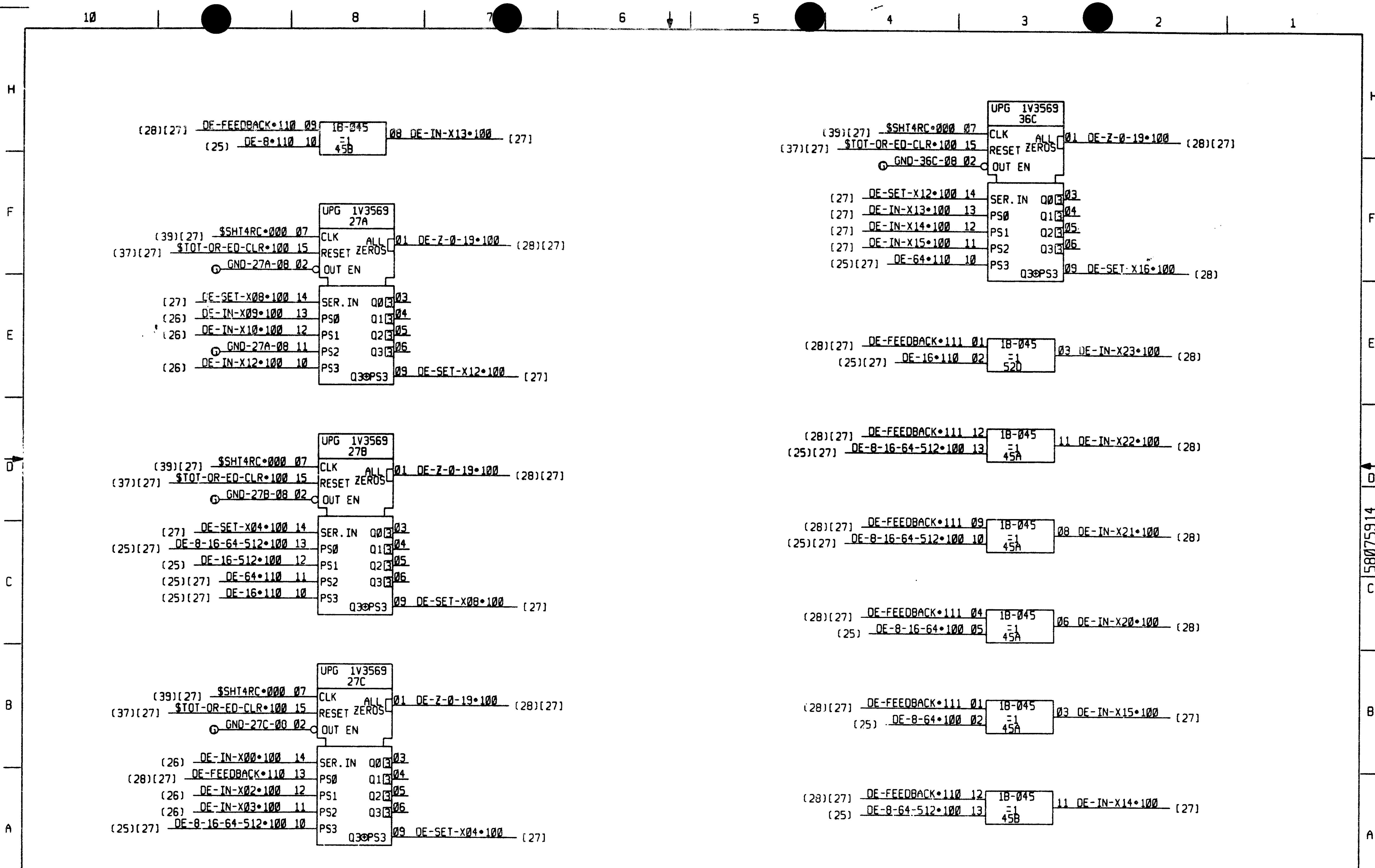
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

TITLE LOGIC DIAGRAM- WDAEI

SIZE	DWG NO	SH	REV
B	58075914	26.0	B

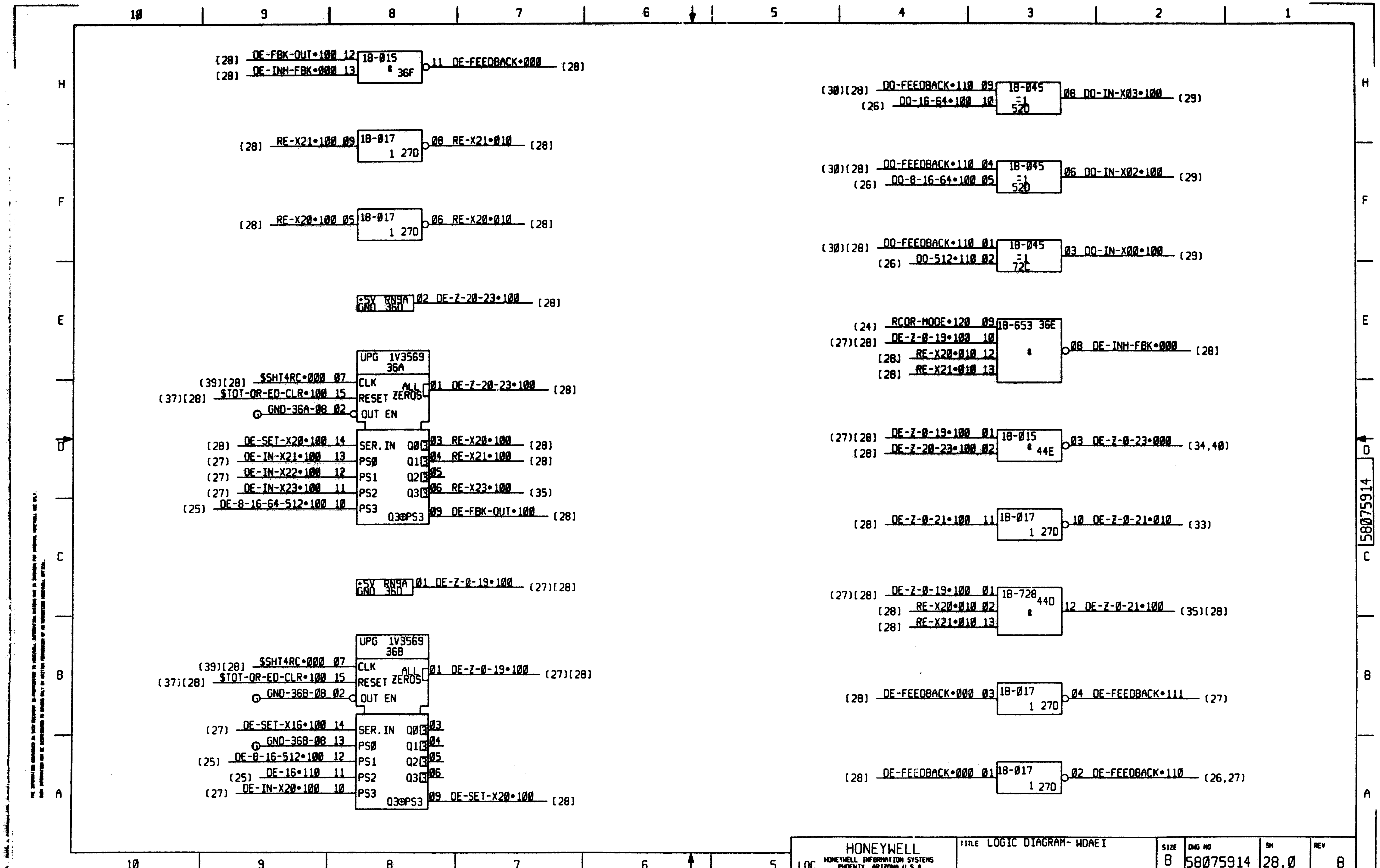
58075914



HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC	TITLE	SIZE	DWG NO	SH	REV
	LOGIC DIAGRAM- WDAEI	B	58075914	27.0	B

58075914



[28] DE-FBK-OUT•100 12
[28] DE-INH-FBK•000 13
1B-015 & 36F
11 DE-FEEDBACK•000 [28]
[28] RE-X21•100 09
1B-017 1 270
08 RE-X21•010 [28]
[28] RE-X20•100 05
1B-017 1 270
06 RE-X20•010 [28]
+5V RN9A GND 36D
02 DE-Z-20-23•100 [28]
UPG 1V3569 36A
[39][28] $SHT4RC•000 07 CLK
[37][28] $TOT-OR-ED-CLR•100 15 RESET
GND-36A-08 02 OUT EN
ALL ZEROS 01 DE-Z-20-23•100 [28]
[28] DE-SET-X20•100 14 SER.IN
[27] DE-IN-X21•100 13 PS0
[27] DE-IN-X22•100 12 PS1
[27] DE-IN-X23•100 11 PS2
[25] DE-8-16-64-512•100 10 PS3
Q0 03 RE-X20•100 [28]
Q1 04 RE-X21•100 [28]
Q2 05
Q3 06 RE-X23•100 [35]
Q3⊕PS3 09 DE-FBK-OUT•100 [28]
+5V RN9A GND 36D
01 DE-Z-0-19•100 [27][28]
UPG 1V3569 36B
[39][28] $SHT4RC•000 07 CLK
[37][28] $TOT-OR-ED-CLR•100 15 RESET
GND-36B-08 02 OUT EN
ALL ZEROS 01 DE-Z-0-19•100 [27][28]
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GND-36B-08 13 PS0
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Q0 03
Q1 04
Q2 05
Q3 06
Q3⊕PS3 09 DE-SET-X20•100 [28]
[30][28] DO-FEEDBACK•110 09
[26] DO-16-64•100 10
1B-045 =1 52D
08 DO-IN-X03•100 [29]
[30][28] DO-FEEDBACK•110 04
[26] DO-8-16-64•100 05
1B-045 =1 52D
06 DO-IN-X02•100 [29]
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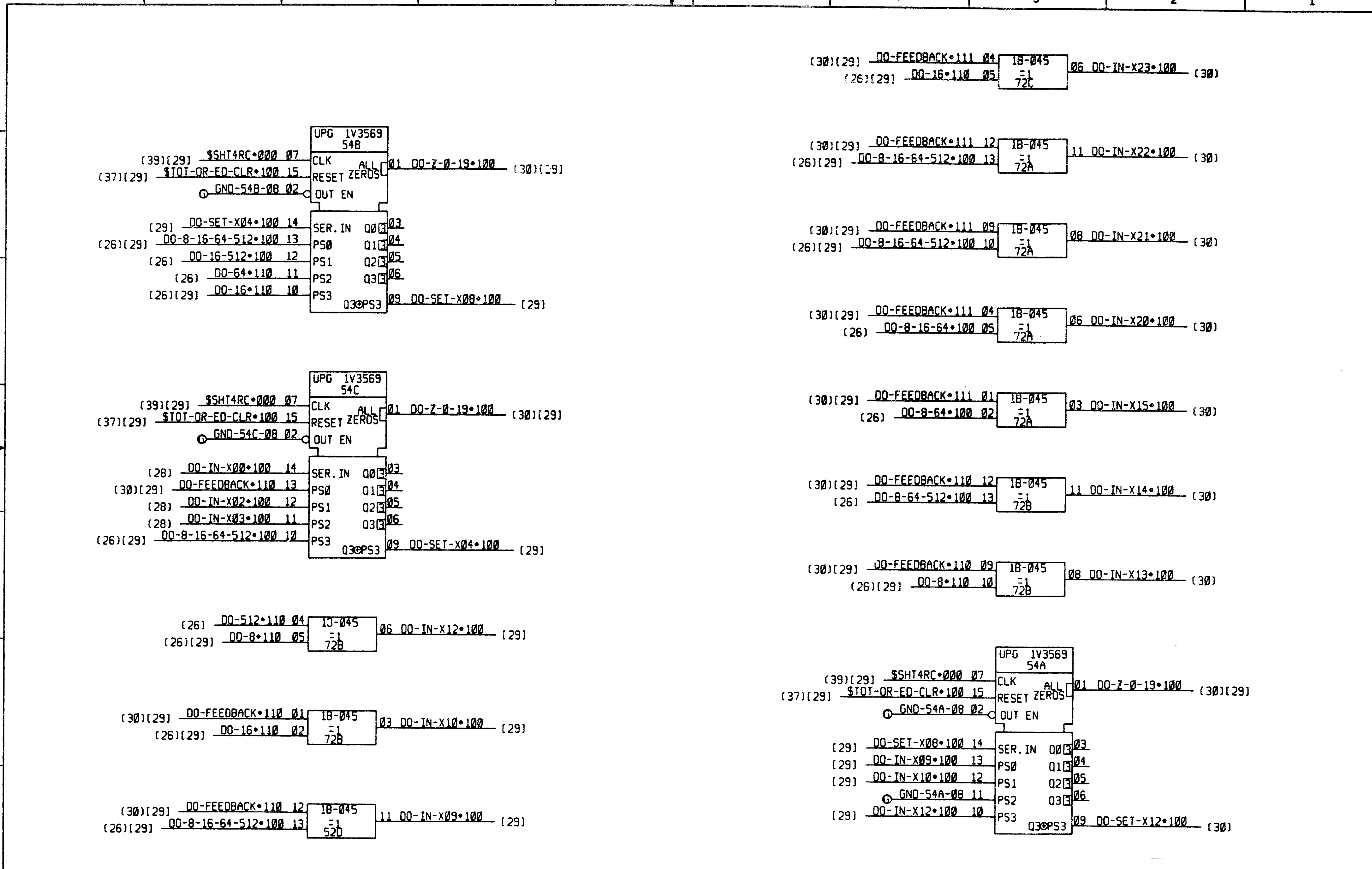
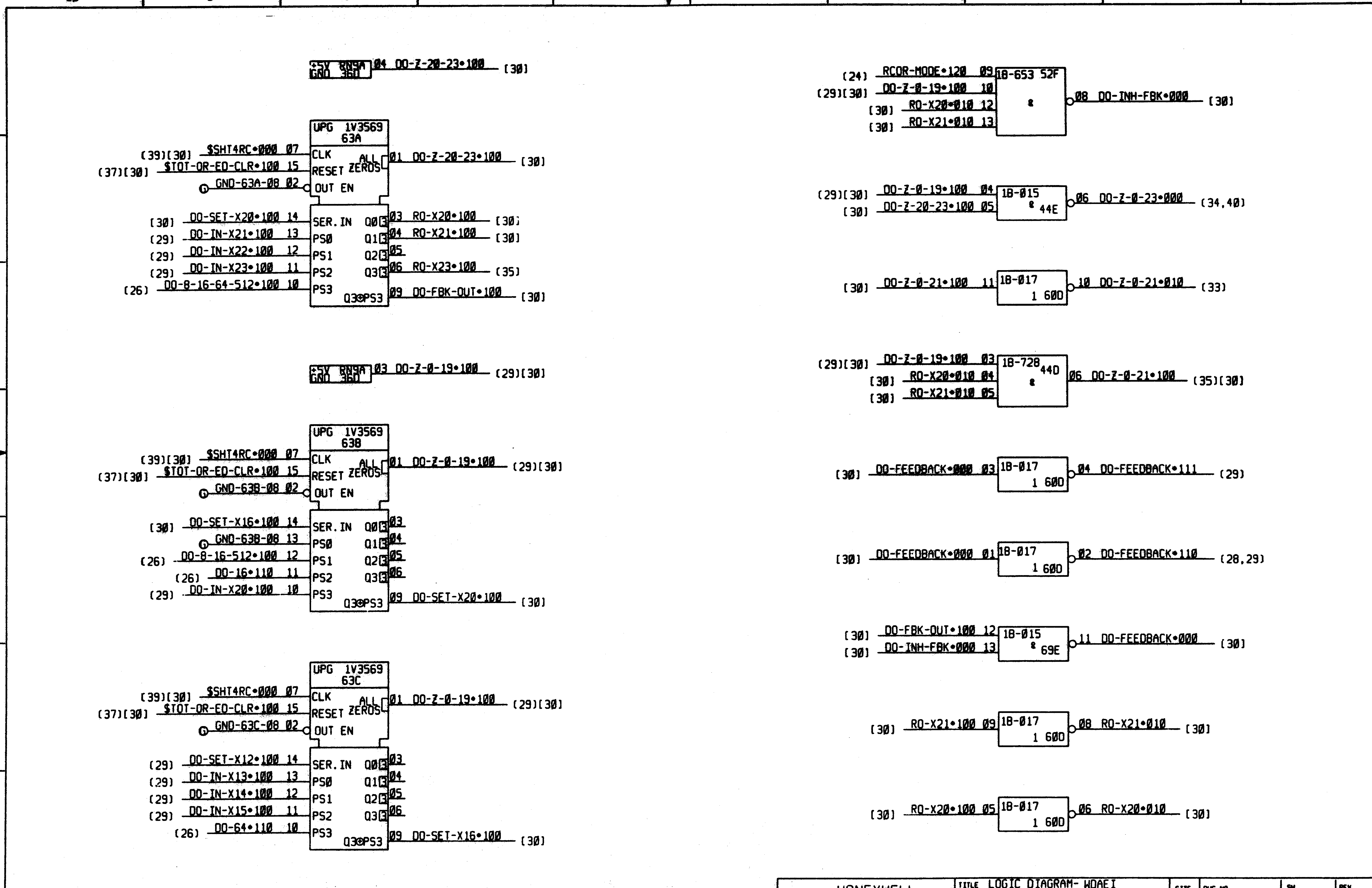
[26] DO-512•110 02
1B-045 =1 72C
03 DO-IN-X00•100 [29]
[24] RCOR-MODE•120 09
[27][28] DE-Z-0-19•100 10
[28] RE-X20•010 12
[28] RE-X21•010 13
1B-653 36E &
08 DE-INH-FBK•000 [28]
[27][28] DE-Z-0-19•100 01
[28] DE-Z-20-23•100 02
1B-015 & 44E
03 DE-Z-0-23•000 [34,40]
[28] DE-Z-0-21•100 11
1B-017 1 270
10 DE-Z-0-21•010 [33]
[27][28] DE-Z-0-19•100 01
[28] RE-X20•010 02
[28] RE-X21•010 13
1B-728 44D &
12 DE-Z-0-21•100 [35][28]
[28] DE-FEEDBACK•000 03
1B-017 1 270
04 DE-FEEDBACK•111 [27]
[28] DE-FEEDBACK•000 01
1B-017 1 270
02 DE-FEEDBACK•110 [26,27]
58075914
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- WDAEI
SIZE B
DWG NO 58075914
SH 28.0
REV B

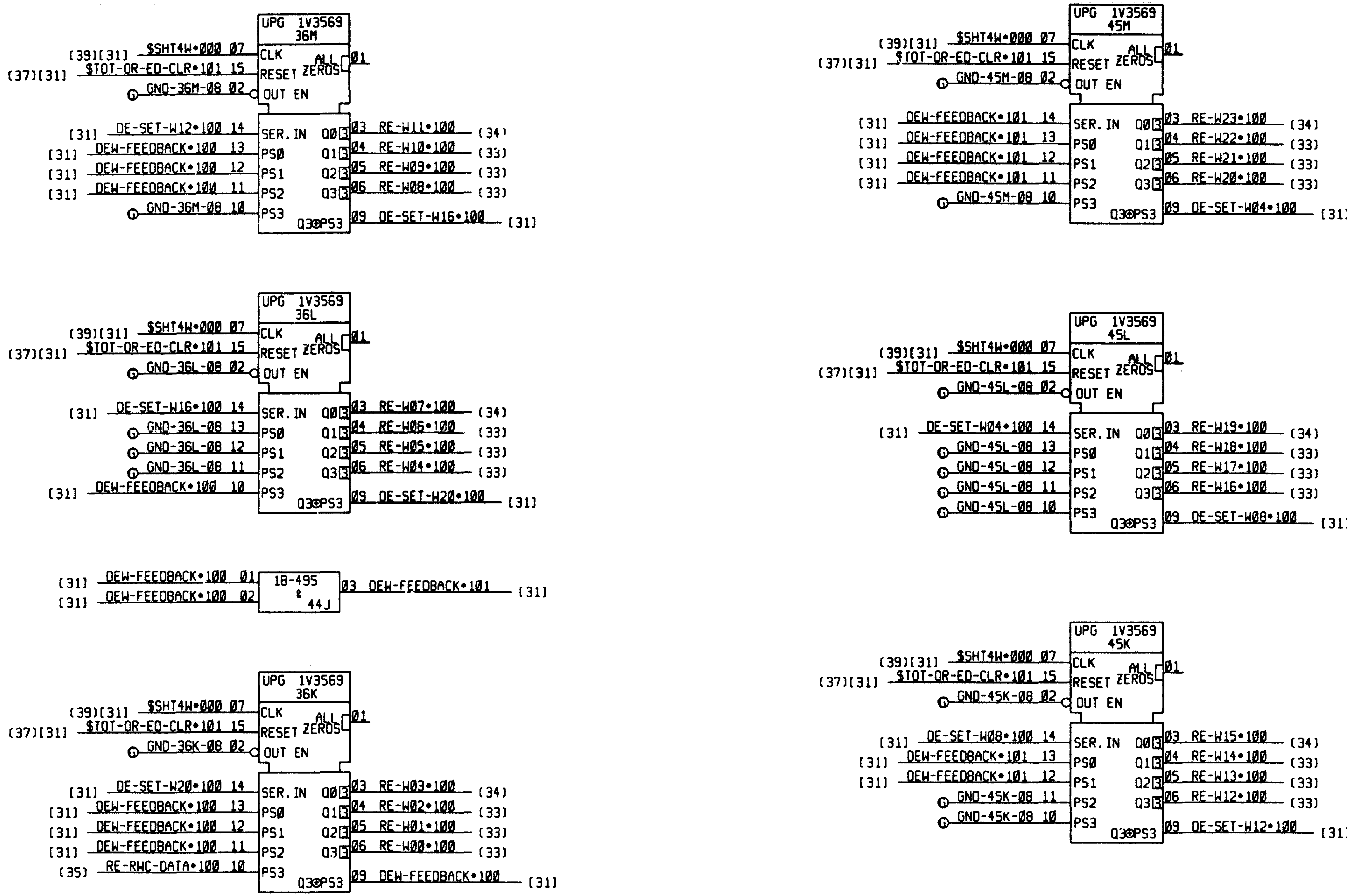


HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 29.0	REV B



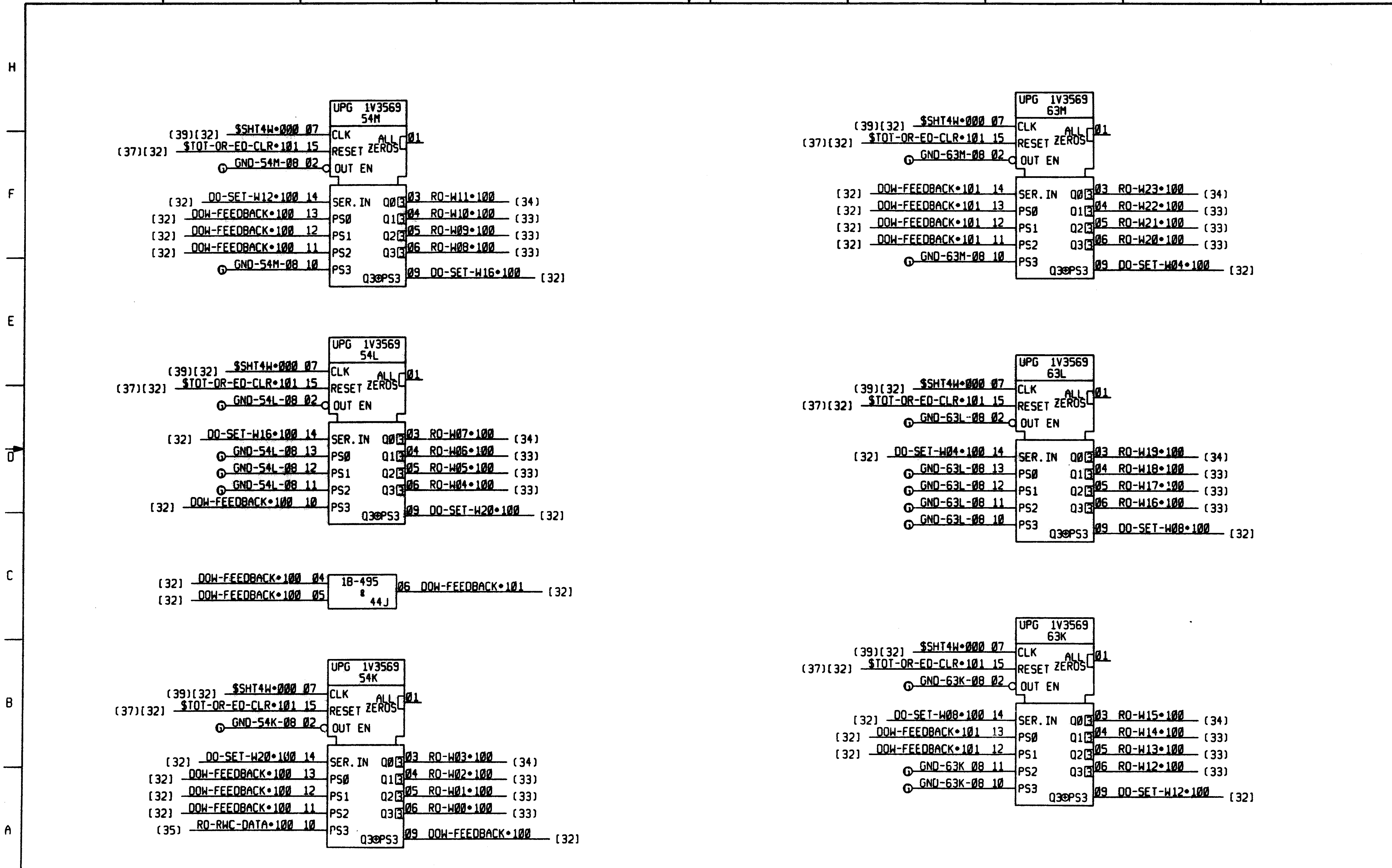
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

LOC | TITLE LOGIC DIAGRAM- WDAEI | SIZE B | DWG NO 58075914 | SH 30.0 | REV B



58075914

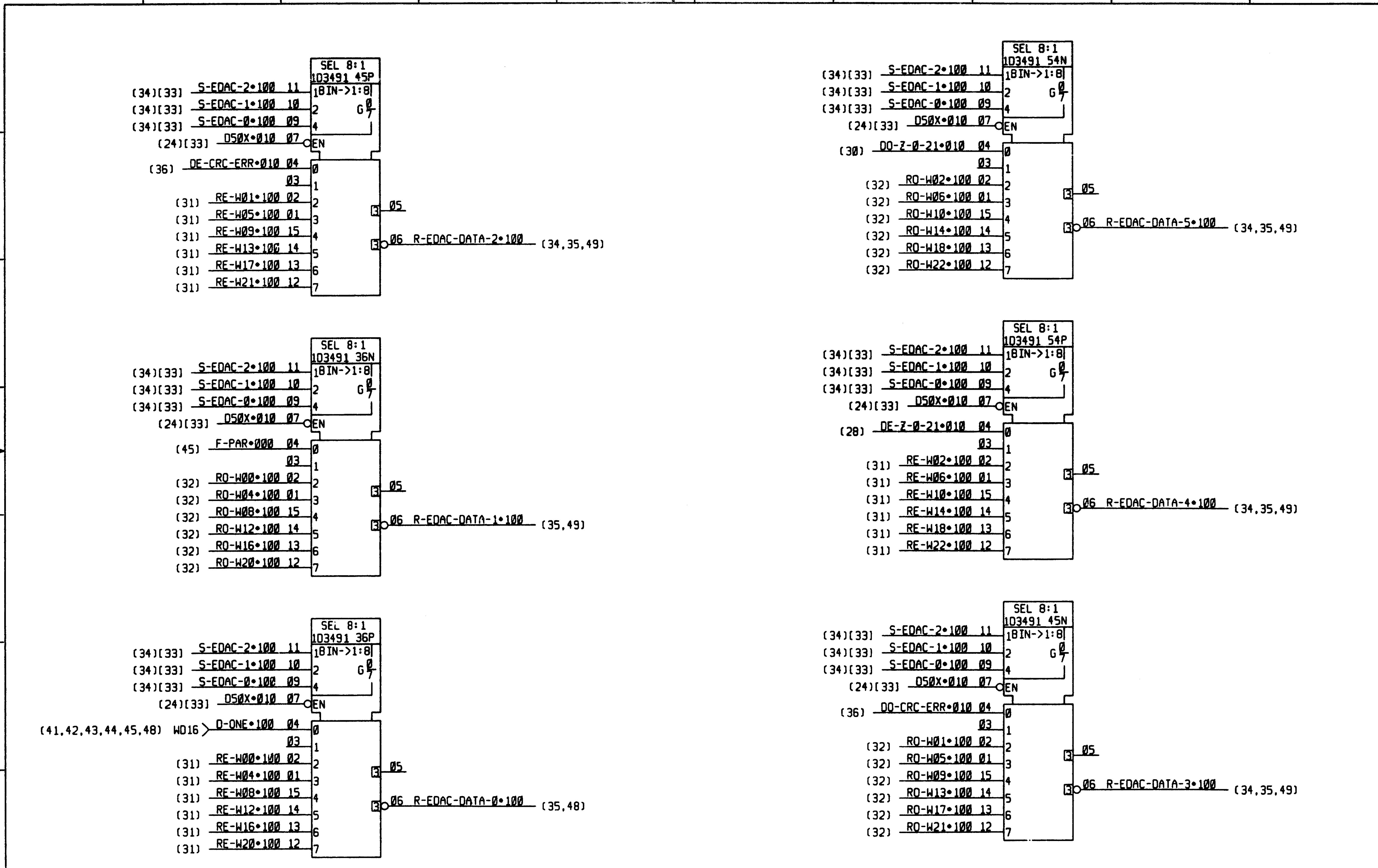
HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A. LOC	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 31.0	REV B



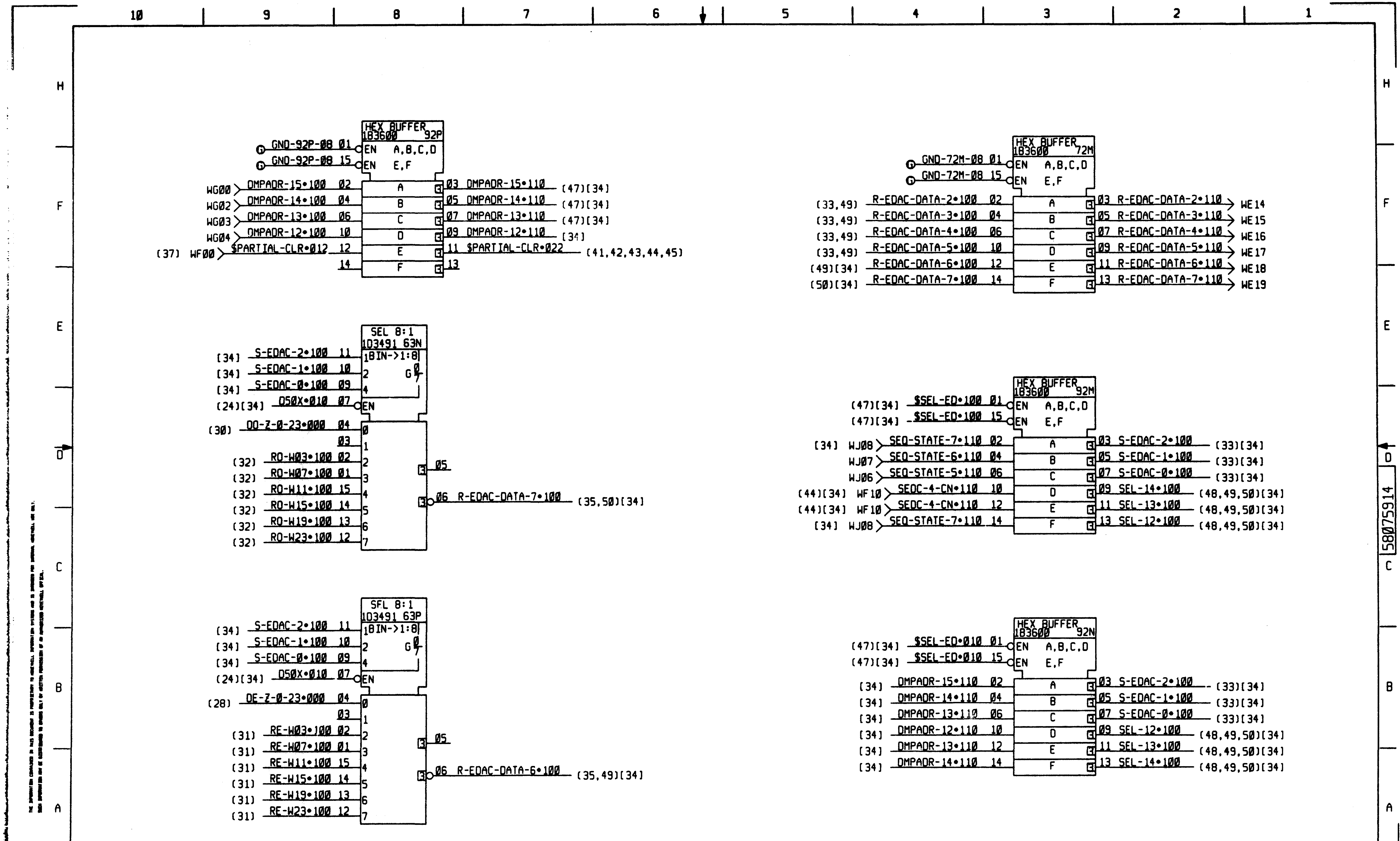
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC

TITLE LOGIC DIAGRAM- WDAEI

SIZE	DWG NO	SH	REV
B	58075914	32.0	B

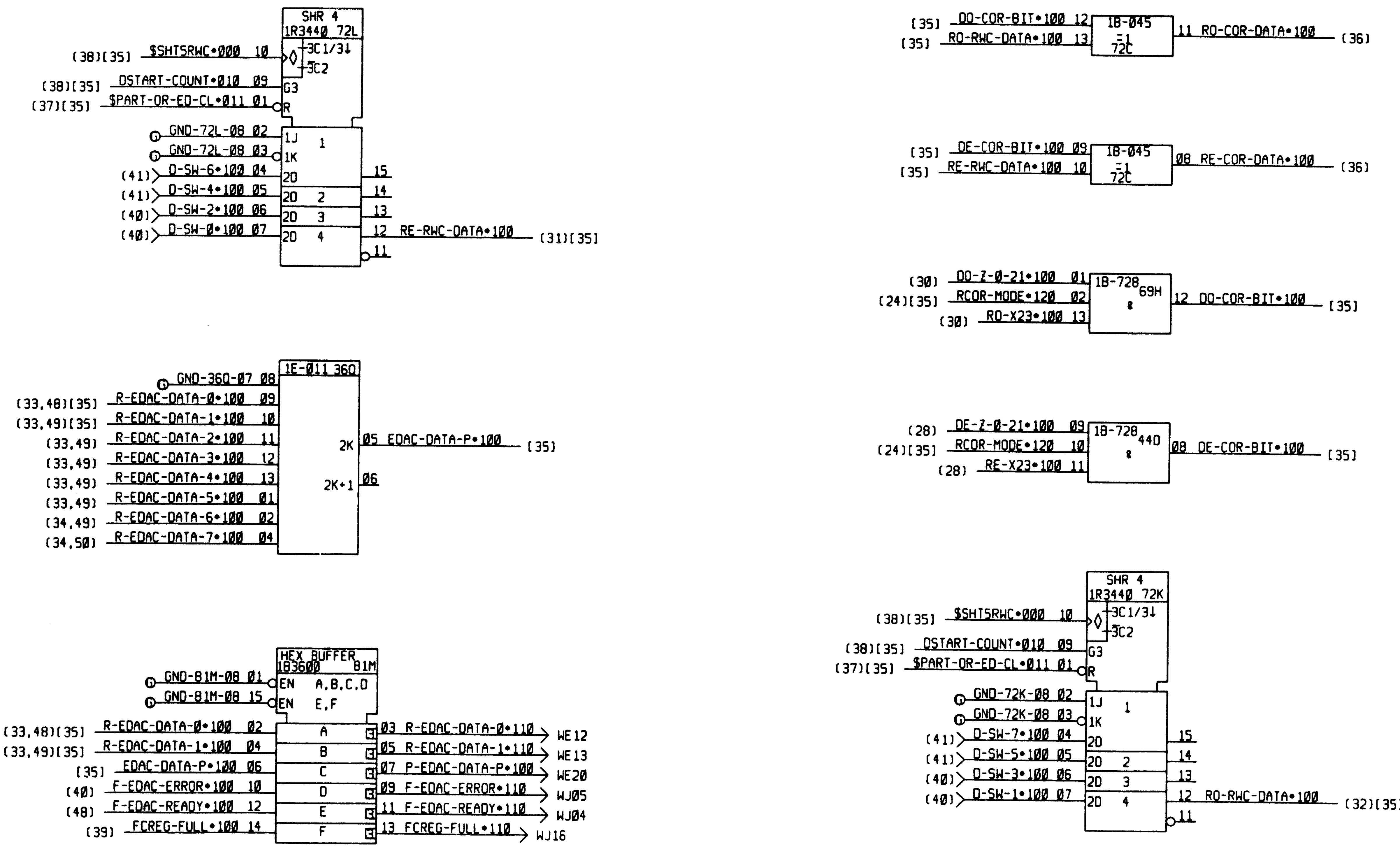


HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A. LOC	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 33.0	REV B



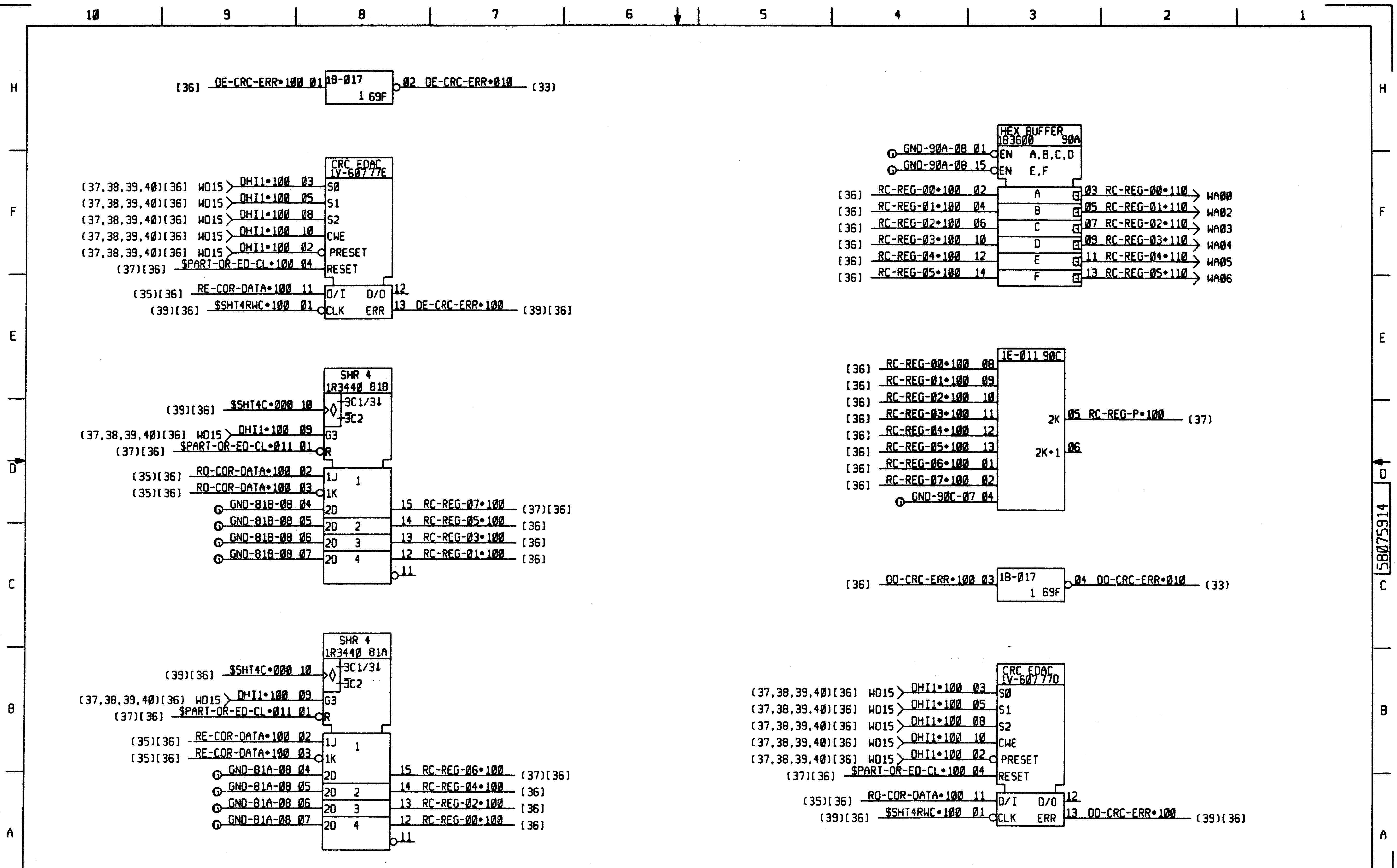
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC	TITLE	SIZE	DWG NO	SH	REV
	LOGIC DIAGRAM- WDAEI	B	58075914	34.0	B



HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

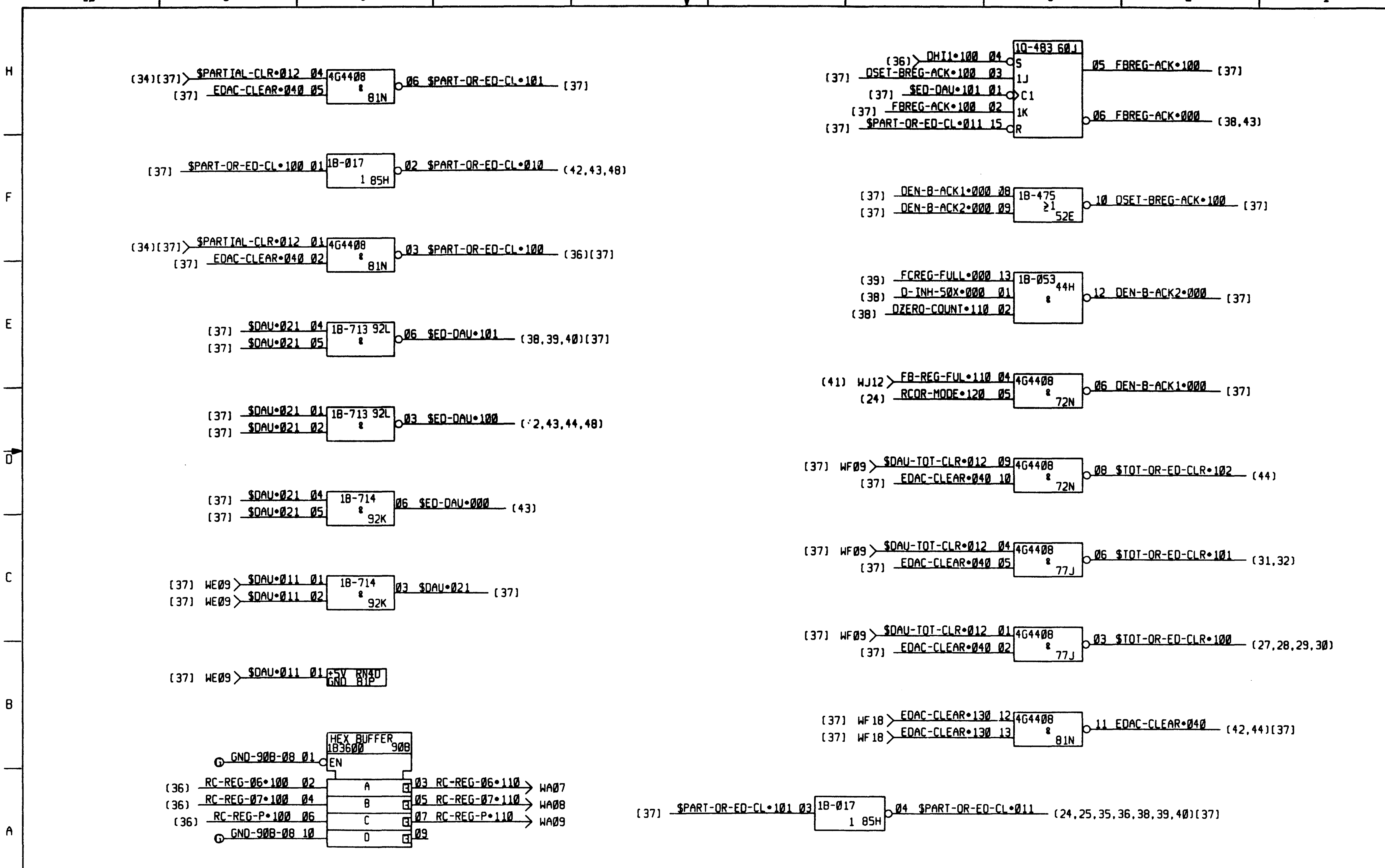
TITLE	SIZE	DWG NO	SH	REV
LOGIC DIAGRAM- WDAEI	B	58075914	35.0	B



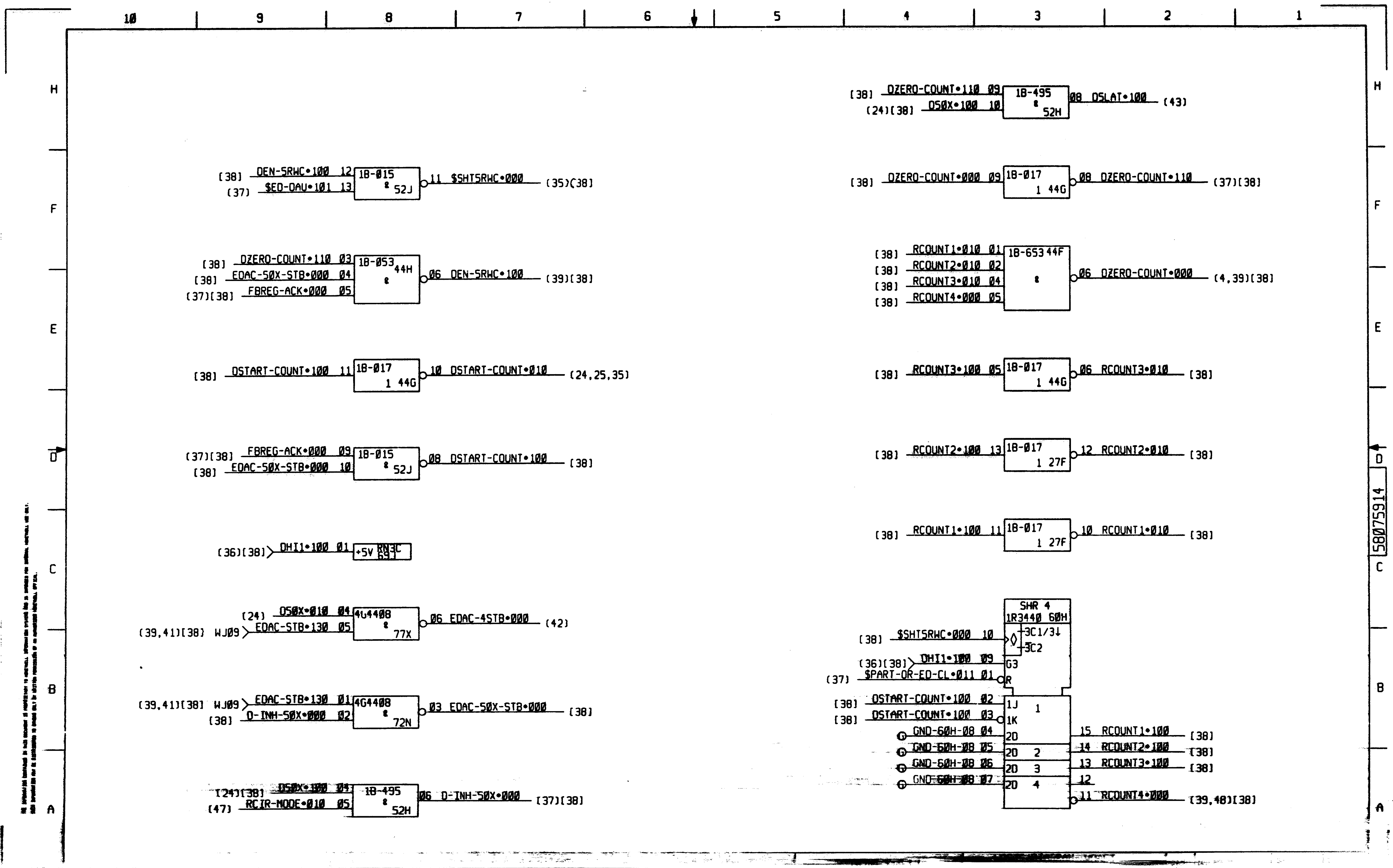
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC

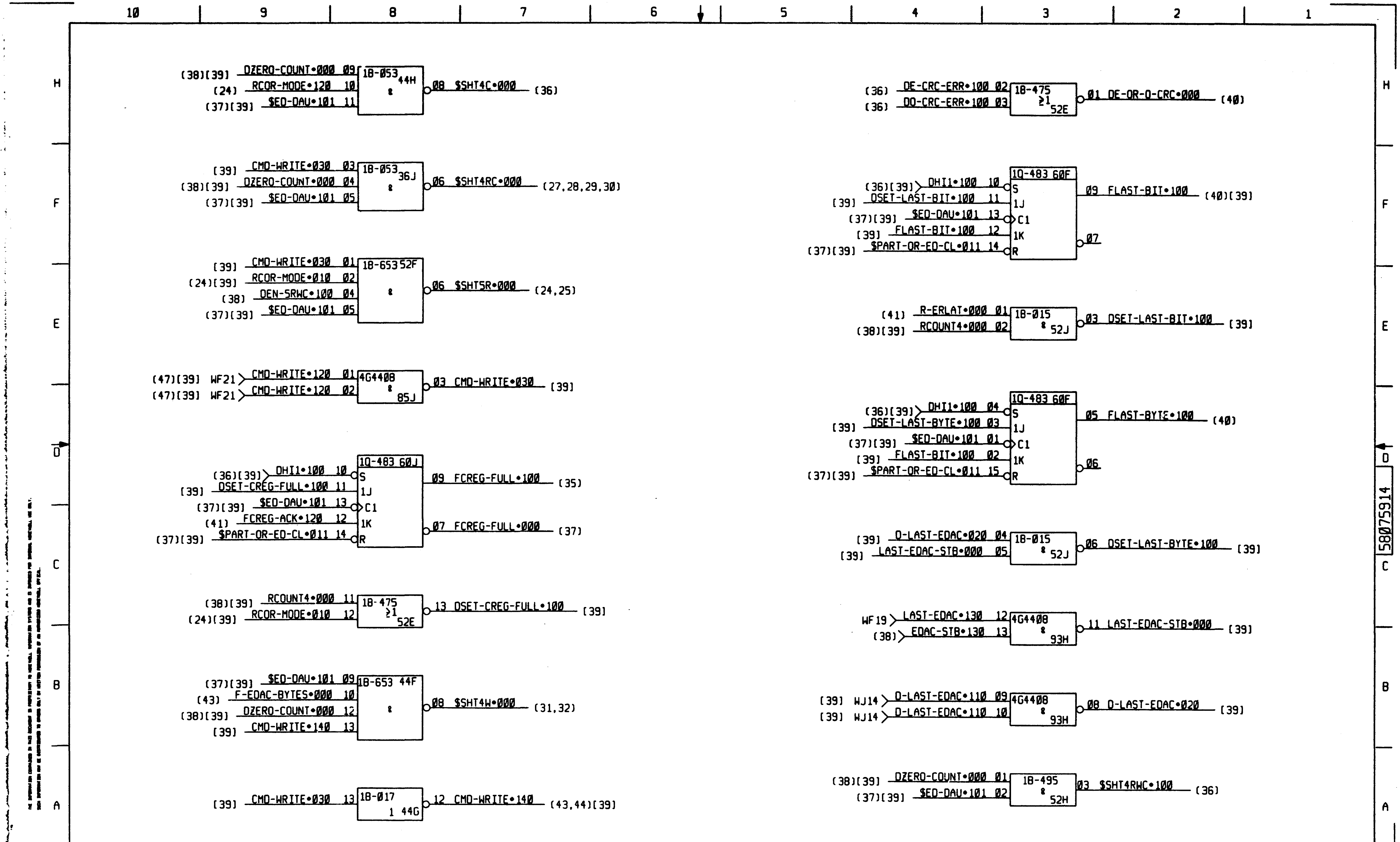
TITLE LOGIC DIAGRAM- WDAEI

SIZE	DWG NO	SH	REV
B	58075914	36.0	B

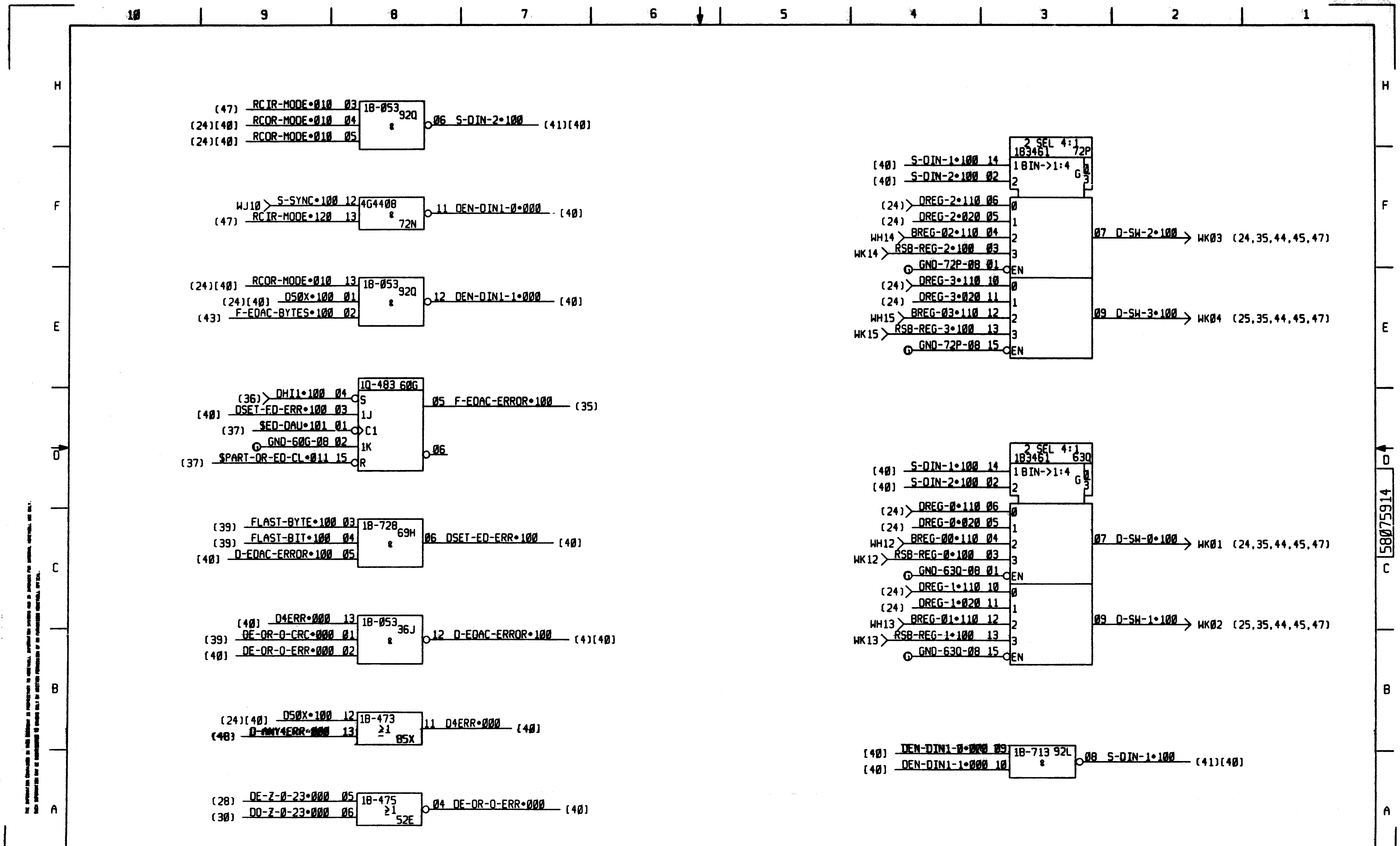


LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 37.0	REV B


DEN-SRWC•100 12
$ED-DAV•101 13
1B-015 52J
11 $SHTSRWC•000
DZERO-COUNT•110 03
EDAC-50X-STB•000 04
FBREG-ACK•000 05
1B-053 44H
06 DEN-SRWC•100
DSTART-COUNT•100 11
1B-017 1 44G
10 DSTART-COUNT•010
FBREG-ACK•000 09
EDAC-50X-STB•000 10
1B-015 52J
08 DSTART-COUNT•100
DHI1•100 01
+5V
D50X•010 04
EDAC-STB•130 05
4G4408 77X
06 EDAC-4STB•000
EDAC-STB•130 01
D-INH-50X•000 02
4G4408 72N
03 EDAC-50X-STB•000
D50X•100 04
RCIR-MODE•010 05
1B-495 52H
06 D-INH-50X•000
DZERO-COUNT•110 09
D50X•100 10
1B-495 52H
08 DSLAT•100
DZERO-COUNT•000 09
1B-017 1 44G
08 DZERO-COUNT•110
RCOUNT1•010 01
RCOUNT2•010 02
RCOUNT3•010 04
RCOUNT4•000 05
1B-653 44F
06 DZERO-COUNT•000
RCOUNT3•100 05
1B-017 1 44G
06 RCOUNT3•010
RCOUNT2•100 13
1B-017 1 27F
12 RCOUNT2•010
RCOUNT1•100 11
1B-017 1 27F
10 RCOUNT1•010
SHR 4
1R3440 60H
$SHTSRWC•000 10
DHI1•100 09
$PART-OR-ED-CL•011 01
DSTART-COUNT•100 02
DSTART-COUNT•100 03
GND-60H-08 04
GND-60H-08 05
GND-60H-08 06
GND-60H-08 07
15 RCOUNT1•100
14 RCOUNT2•100
13 RCOUNT3•100
12
11 RCOUNT4•000
58075914



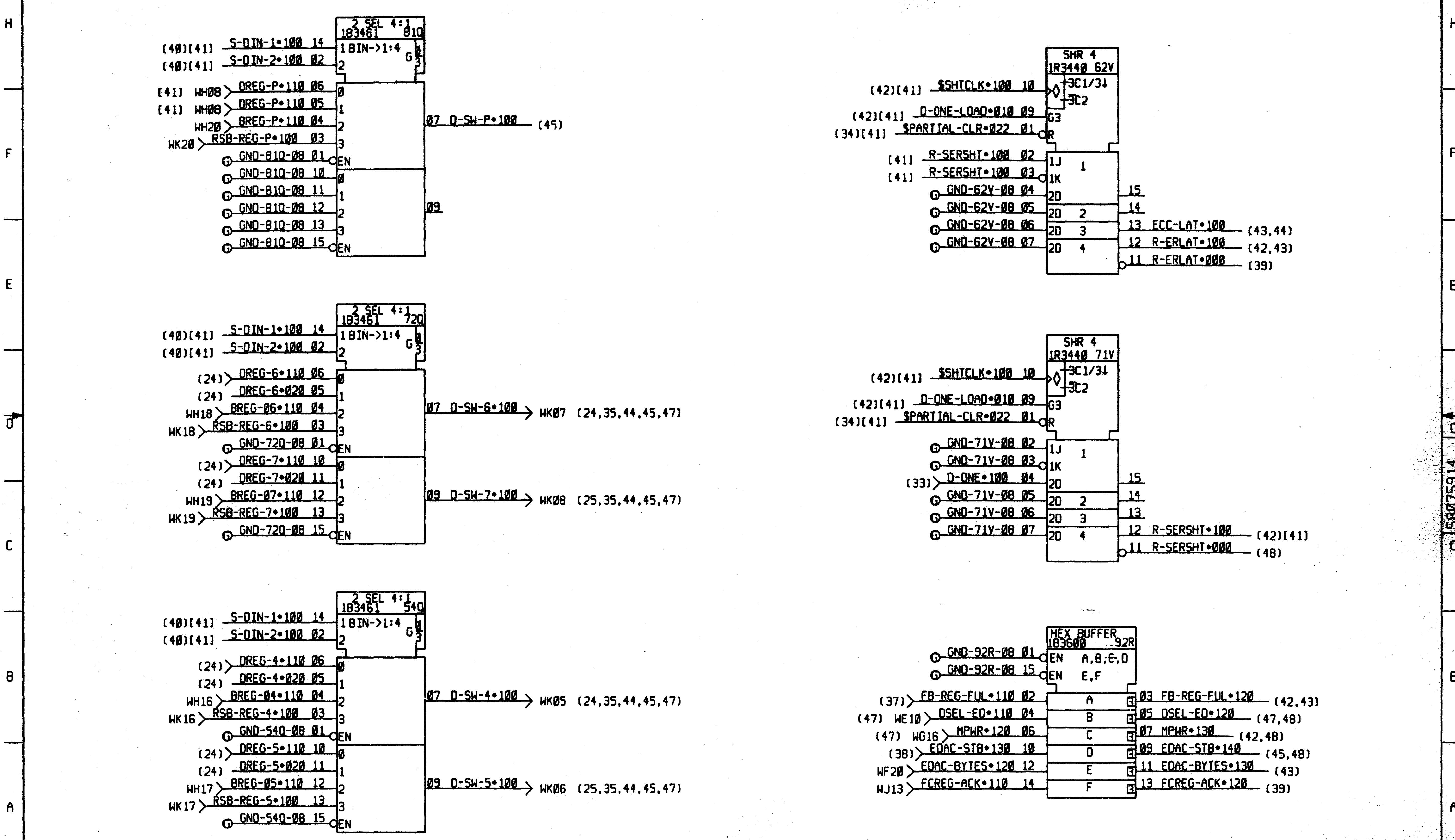
LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 39.0	REV B



HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAEI

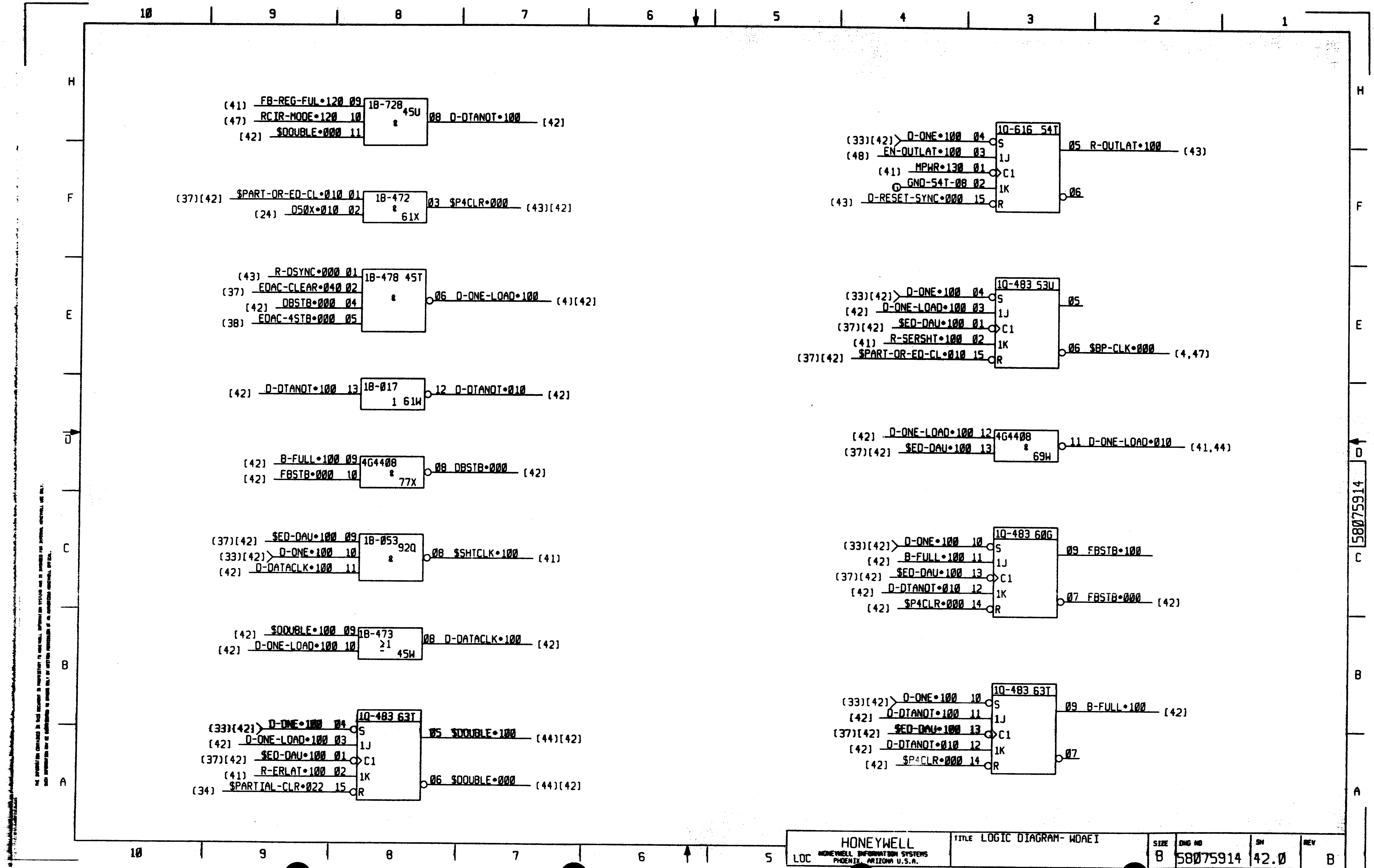
SIZE B | DWG NO 58075914 | SH 40.0 | REV B



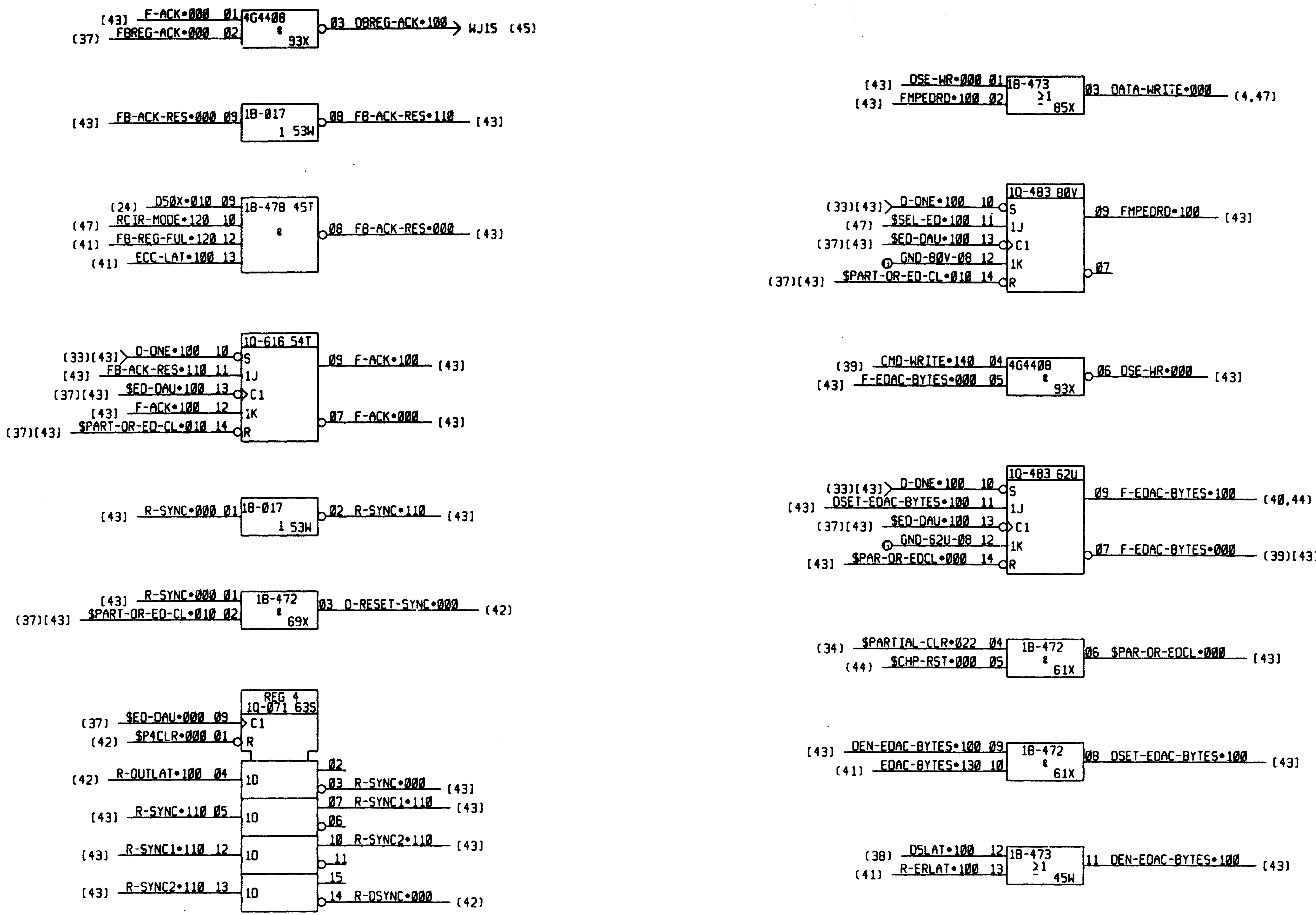
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC

TITLE LOGIC DIAGRAM- WDAEI

SIZE	DWG NO	SH	REV
B	58075914	41.0	B



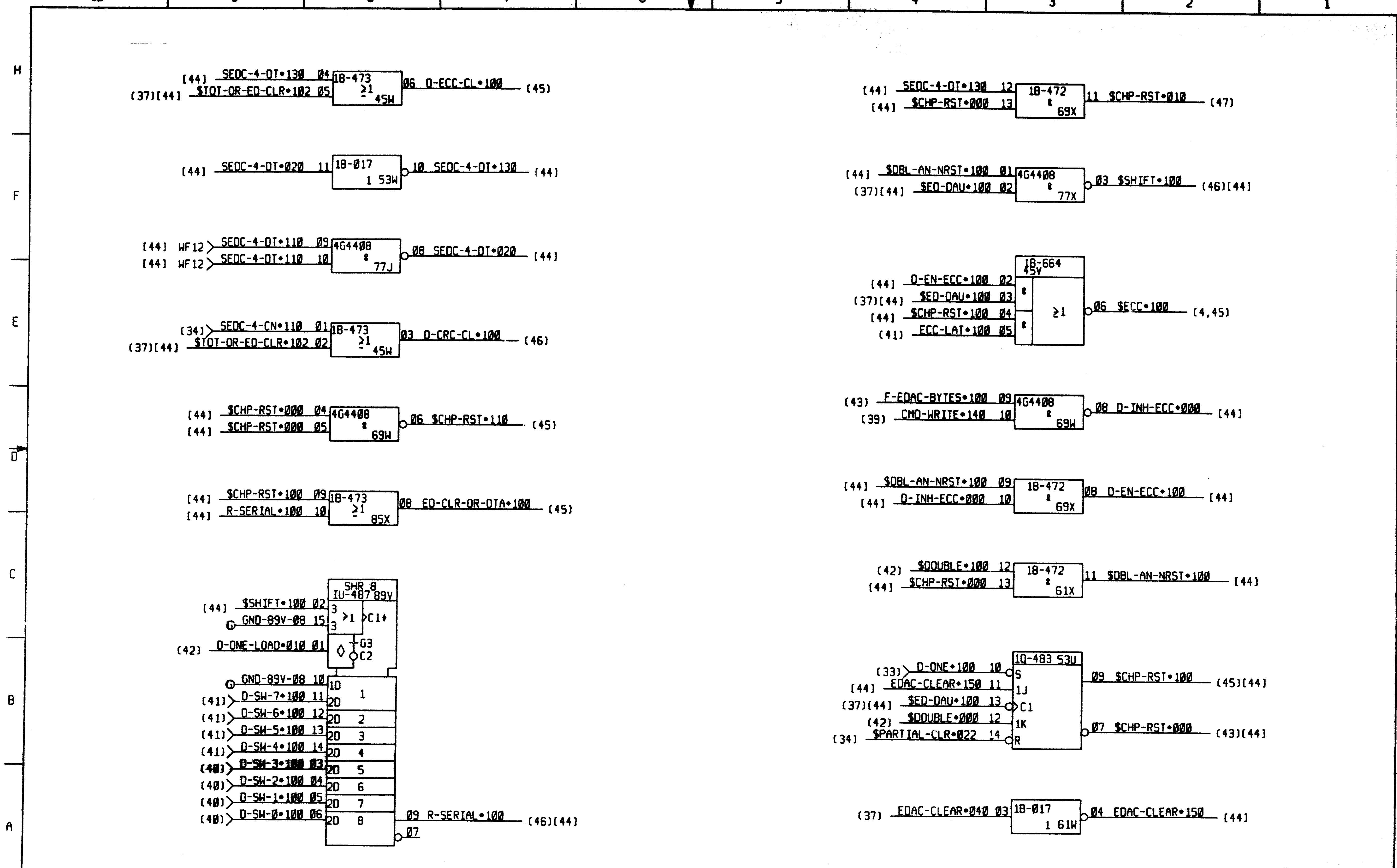
(41) FB-REG-FUL•120 09
(47) RCIR-MODE•120 10
(42) $DOUBLE•000 11
1B-728 45U &
08 D-DTANOT•100 (42)
(37)(42) $PART-OR-ED-CL•010 01
(24) D50X•010 02
1B-472 & 61X
03 $P4CLR•000 (43)(42)
(43) R-DSYNC•000 01
(37) EDAC-CLEAR•040 02
(42) DBSTB•000 04
(38) EDAC-4STB•000 05
1B-478 45T &
06 D-ONE-LOAD•100 (4)(42)
(42) D-DTANOT•100 13
1B-017 1 61W
12 D-DTANOT•010 (42)
(42) B-FULL•100 09
(42) FBSTB•000 10
4G4408 & 77X
08 DBSTB•000 (42)
(37)(42) $ED-DAU•100 09
(33)(42) D-ONE•100 10
(42) D-DATACLK•100 11
1B-053 92Q &
08 $SHTCLK•100 (41)
(42) $DOUBLE•100 09
(42) D-ONE-LOAD•100 10
1B-473 ≥1 45W
08 D-DATACLK•100 (42)
(33)(42) D-ONE•100 04
(42) D-ONE-LOAD•100 03
(37)(42) $ED-DAU•100 01
(41) R-ERLAT•100 02
(34) $PARTIAL-CLR•022 15
1Q-483 63T
S 1J C1 1K R
05 $DOUBLE•100 (44)(42)
06 $DOUBLE•000 (44)(42)
(33)(42) D-ONE•100 04
(48) EN-OUTLAT•100 03
(41) MPWR•130 01
GND-54T-08 02
(43) D-RESET-SYNC•000 15
1Q-616 54T
05 R-OUTLAT•100 (43)
06
(33)(42) D-ONE•100 04
(42) D-ONE-LOAD•100 03
(37)(42) $ED-DAU•100 01
(41) R-SERSHT•100 02
(37)(42) $PART-OR-ED-CL•010 15
1Q-483 53U
05
06 $BP-CLK•000 (4,47)
(42) D-ONE-LOAD•100 12
(37)(42) $ED-DAU•100 13
4G4408 & 69W
11 D-ONE-LOAD•010 (41,44)
(33)(42) D-ONE•100 10
(42) B-FULL•100 11
(37)(42) $ED-DAU•100 13
(42) D-DTANOT•010 12
(42) $P4CLR•000 14
1Q-483 60G
09 FBSTB•100
07 FBSTB•000 (42)
(33)(42) D-ONE•100 10
(42) D-DTANOT•100 11
(37)(42) $ED-DAU•100 13
(42) D-DTANOT•010 12
(42) $P4CLR•000 14
1Q-483 63T
09 B-FULL•100 (42)
07
58075914
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- WDAEI
SIZE B
DWG NO 58075914
SH 42.0
REV B



HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAEI

SIZE	DWG NO	SH	REV
B	58075914	43.0	B



HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC

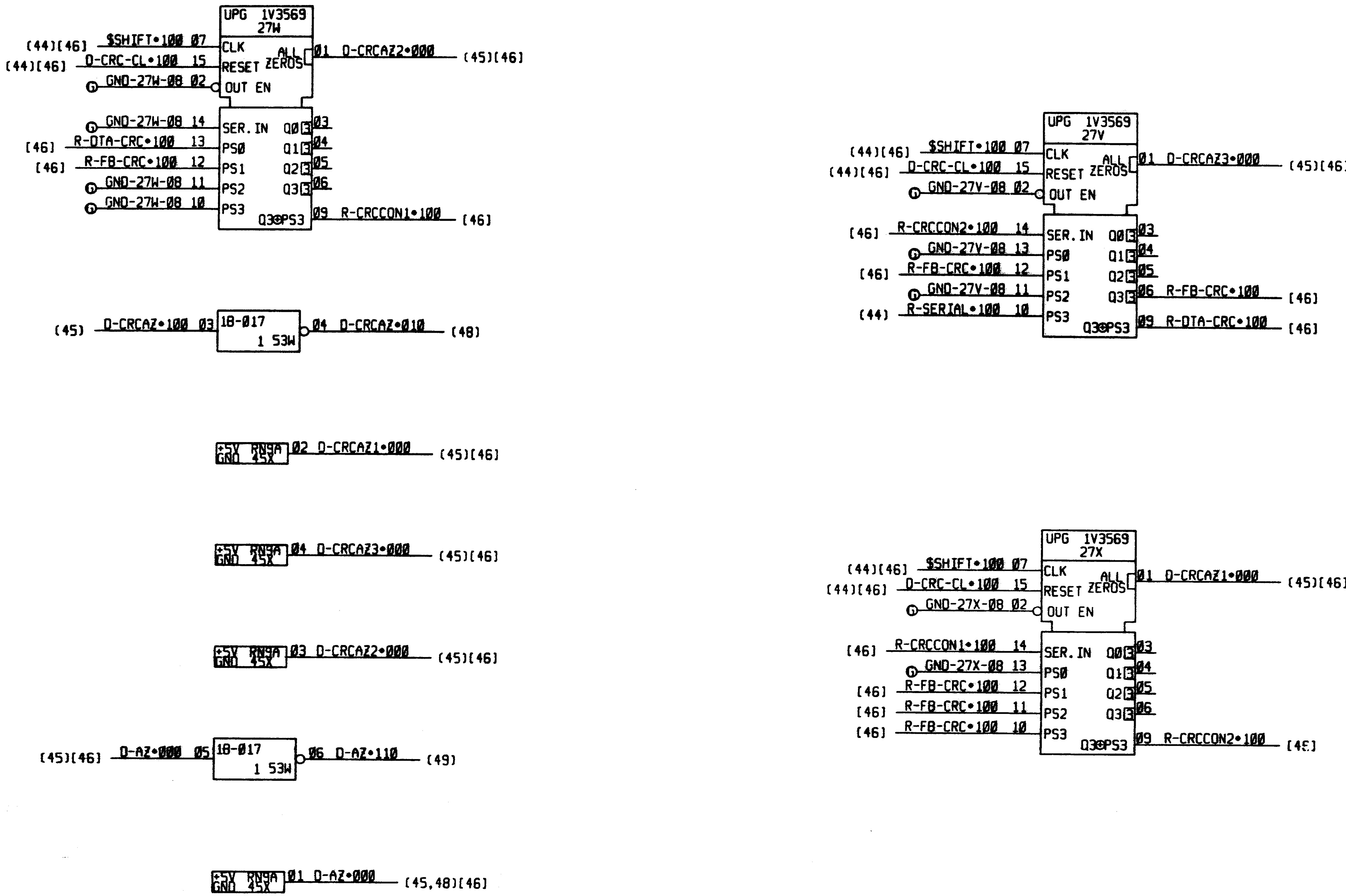
TITLE	SIZE	DWG NO	SH	REV
LOGIC DIAGRAM- WDAEI	B	58075914	44.0	B

HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

LOC

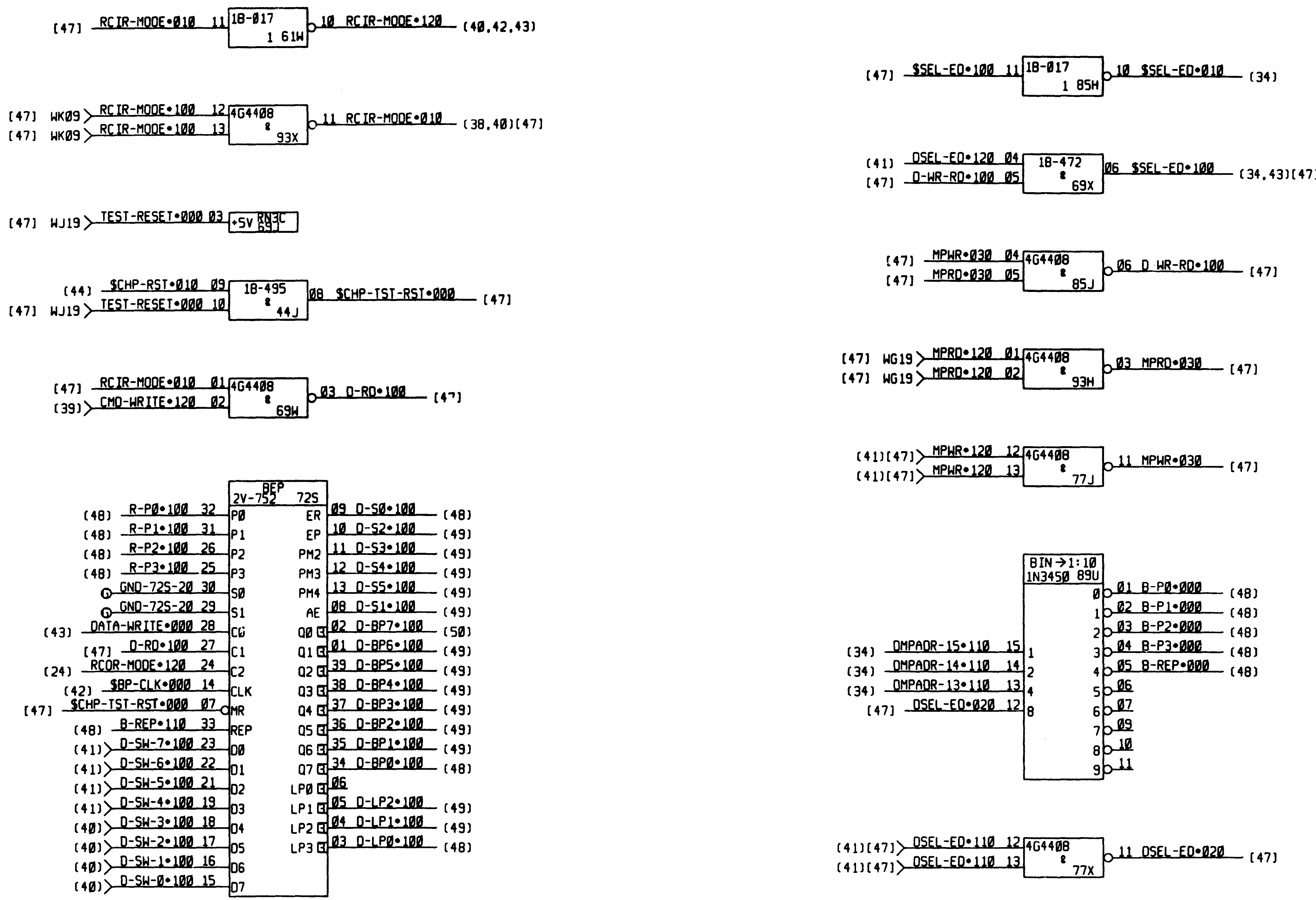
TITLE LOGIC DIAGRAM- WDAEI

SIZE	DWG NO	SH	REV
B	58075914	45.0	B

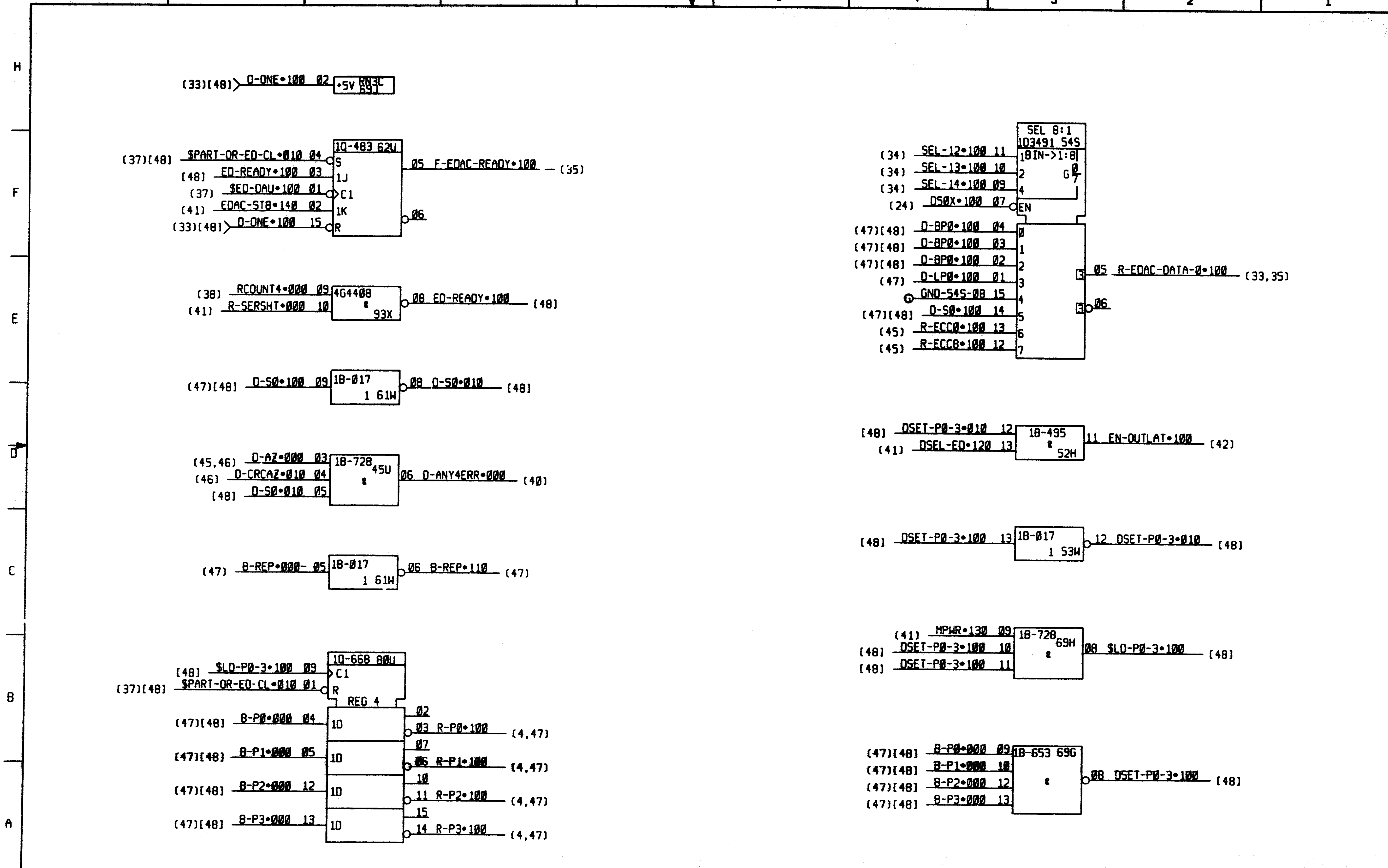


58075914

LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 46.0	REV B



HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAEI	SIZE B	DWG NO 58075914	SH 47.0	REV B

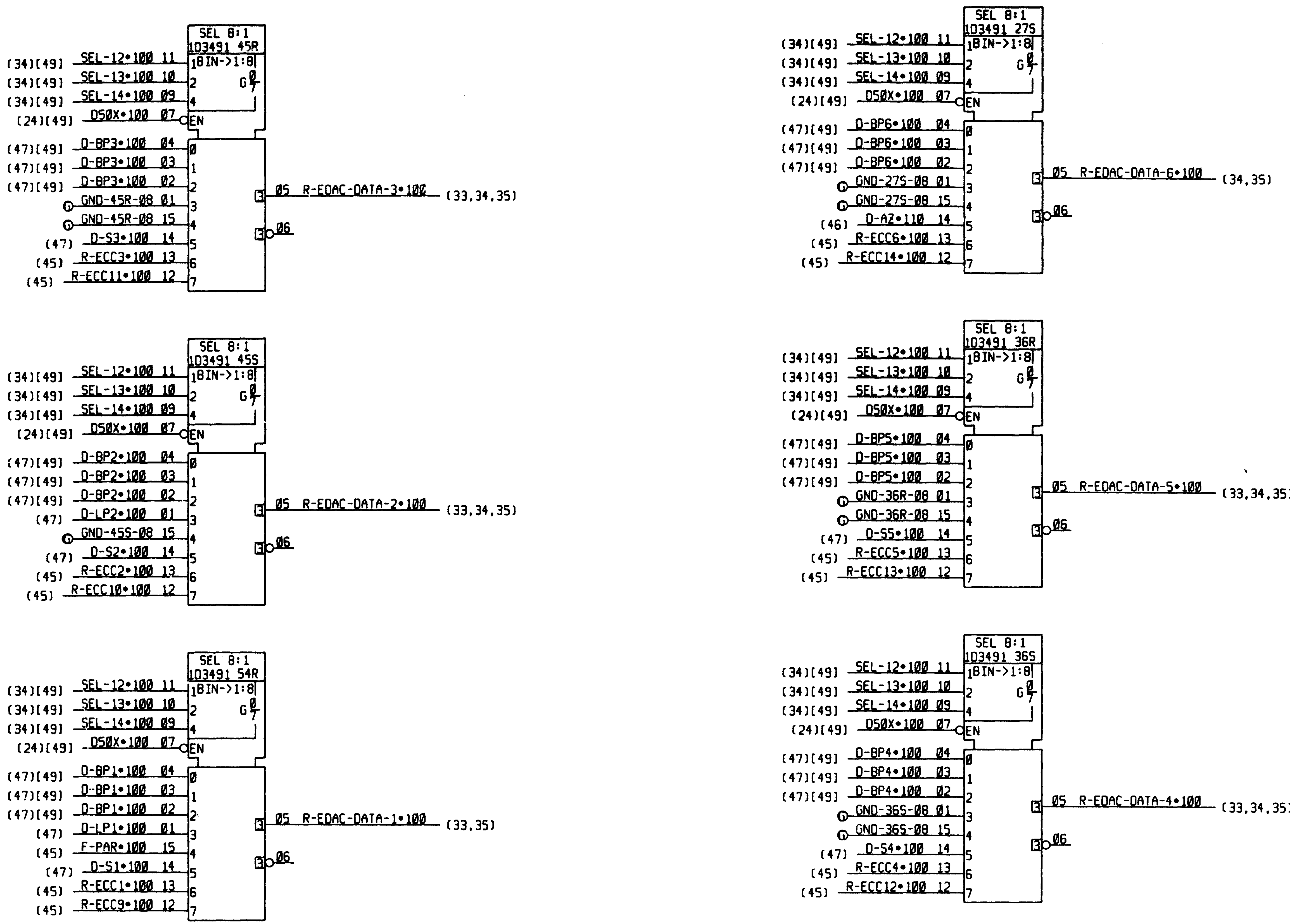


HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

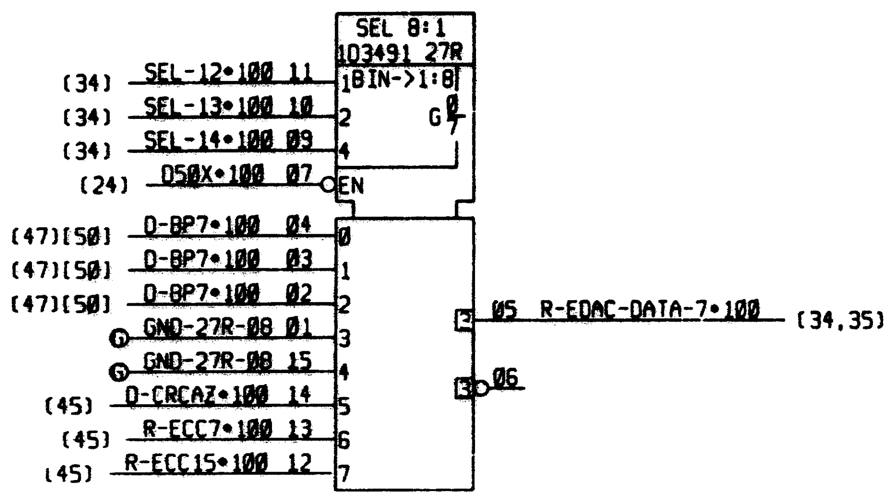
TITLE LOGIC DIAGRAM- WDAEI

SIZE	DWG NO	SH	REV
B	58075914	48.0	B



58075914

HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A. LOC	TITLE LOGIC DIAGRAM- WDAFI	SIZE B	DWG NO 58075914	SH 49.0	REV B



TOTAL NUMBER OF SHEETS = 54

HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

TITLE LOGIC DIAGRAM- WDAEI

SIZE	DWG NO	SH	REV
B	58Ø75914	5Ø.ØF	B

58Ø75914

58075910

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB 001	002	102	203	103	304	204	004	PL ALL
A	LEVEL 1 ISSUE	82	AUG	19	J. H. Boyle 8-13-82	A								A
B	PHAØXS240	83	JUL	22	G Drenth	B	B	B						B
C	PHAØXS355	83	NOV	29	T Insung	OBSOLETE	C	C	C	C				C
C1	Level 2 ENXS149		ND		G Drenth		OBSOLETE	OBSOLETE	C1	C1				
D	PHAØXS582	84	OCT	30	G Drenth				D	D	D	D	D	D
									RESV	RESV				
	58075914				LOGIC DIAG						B	B	B	
					BD TEST DECK									

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY G Weston 81 AUG 12

APPROVED E Gosfued 8-12-82

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE HDUHC PWA WDAEI

SIZE	REVISION STATUS FOR	SHEET	REV
X	58075910	1/1	D

DIST. -30

BRUNING 44-141 40366

CE 300 A-3 (1-79)

58075912

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 001	002		SH 1/1
A	LVL 3 ISSUE	82	08	17	J.M. Boyle 8-13-82	A		1-11 F	A
B	PHA8XS240	83	07	22	G Drenttle	B	B	1-11 F	B
						OBSOLETE			

FOR CONTINUATION OF REVISION STATUS SEE SHEET

BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX, ARIZONA

CE 300 A-3 (1-79)

MADE BY D Kajiurski 82 Aug 02

APPROVED E. Gottfried 8-12-82

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CIL WDAEI

SIZE	REVISION STATUS FOR	SHEET	REV
A	58075912	1/1	B

DIST. C125-37

TAB-002

STANDARD LOCATION CODE PATTERN
X-POS & Y-POS PER 5C046507-002
UNLESS OTHERWISE SHOWN, ROTATION IS NORTH

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
00A	2T3456	43C216456P1			
00AE	P9	43A114748P9			
00B	2T3456	43C216456P1			
00BE	RSOM	58020479-012			
00C	2T3456	43C216456P1			
00CE	P1043	43C212092P1043			
00D	2T3456	43C216456P1			
00DE	RSOM	58020479-012			
00E	2T3456	43C216456P1			
00EE	P1043	43C212092P1043			
00F	2T3456	43C216456P1			
00G	2T3456	43C216456P1			
00GE	P9	43A114748P9			
00H	2T3456	43C216456P1			
00HE	RSOM	58020479-012			
00J	2T3456	43C216456P1			
00JE	P1043	43C212092P1043			
00K	2T3456	43C216456P1			
00KE	RSOM	58020479-012			
00L	2T3456	43C216456P1			
00LE	P1043	43C212092P1043			
00M	2T3456	43C216456P1			
00ME	RSOM	58020479-012			
00N	2T3456	43C216456P1			
00NE	P9	43A114748P9			
00P	2T3456	43C216456P1			
00PE	RSOM	58020479-012			
00Q	2T3456	43C216456P1			
00QE	P1043	43C212092P1043			
00R	2T3456	43C216456P1			
00S	2T3456	43C216456P1			
00SE	P1043	43C212092P1043			

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
00T	2T3456	43C216456P1			
00TE	RSOM	58020479-012			
00U	2T3456	43C216456P1			
00UE	P9	43A114748P9			
00V	2T3456	43C216456P1			
00VE	RSOM	58020479-012			
00W	2T3456	43C216456P1			
00WE	P1043	43C212092P1043			
00X	2T3456	43C216456P1			
08AE	P9	43A114748P9			
08CE	P1043	43C212092P1043			
08EE	P1043	43C212092P1043			
08GE	P9	43A114748P9			
08JE	P1043	43C212092P1043			
08LE	P1043	43C212092P1043			
08NE	P9	43A114748P9			
08QE	P1043	43C212092P1043			
08SE	P1043	43C212092P1043			
08UE	P9	43A114748P9			
08WE	P1043	43C212092P1043			
09A	2T3456	43C216456P1			
09B	2T3456	43C216456P1			
09BE	RSOM	58020479-012			
09C	2T3456	43C216456P1			
09D	2T3456	43C216456P1			
09DE	RSOM	58020479-012			
09E	2T3456	43C216456P1			
09F	1B-017	58002017-001			
09FE	RSOM	58020479-012			
09G	2T3456	43C216456P1			
09H	2T3456	43C216456P1			
09HE	RSOM	58020479-012			
09J	2T3456	43C216456P1			
09K	2T3456	43C216456P1			
09KE	RSOM	58020479-012			
09L	2T3456	43C216456P1			
09M	2T3456	43C216456P1			
09ME	RSOK	58020479-010			

COMP INSTL LIST - WDAEI

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
09N	2T3456	43C216456P1			
09P	2T3456	43C216456P1			
09PE	RSOM	58020479-012			
09Q	2T3456	43C216456P1			
09R	2T3456	43C216456P1			
09RE	RSOM	58020479-012			
09S	1B-017	58002017-001			
09T	2T3456	43C216456P1			
09TE	RSOM	58020479-012			
09U	2T3456	43C216456P1			
09V	2T3456	43C216456P1			
09VE	RSOM	58020479-012			
09W	2T3456	43C216456P1			
09X	2T3456	43C216456P1			
16AE	P9	43A114748P9			
16CE	P1043	43C212092P1043			
16EE	P1043	43C212092P1043			
16GE	P9	43A114748P9			
16JE	P1043	43C212092P1043			
16LE	P1043	43C212092P1043			
16NE	P9	43A114748P9			
16QE	P1043	43C212092P1043			
16SE	P1043	43C212092P1043			
16UE	P9	43A114748P9			
16WE	P1043	43C212092P1043			
18A	3T3457	43C216457P1			
18B	3T3457	43C216457P1			
18C	3T3457	43C216457P1			
18D	3T3457	43C216457P1			
18DE	RSOM	58020479-012			
18E	3T3457	43C216457P1			
18F	1B3441	43C216441P1			
18G	3T3457	43C216457P1			
18H	3T3457	43C216457P1			
18J	3T3457	43C216457P1			
18K	3T3457	43C216457P1			
18KE	RSOM	58020479-012			
18L	3T3457	43C216457P1			

COMP INSTL LIST - WDAEI

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
18M	3T3457	43C216457P1			
18N	3T3457	43C216457P1			
18P	3T3457	43C216457P1			
18Q	1B3441	43C216441P1			
18R	3T3457	43C216457P1			
18RE	RSOM	58020479-012			
18S	3T3457	43C216457P1			
18T	3T3457	43C216457P1			
18U	3T3457	43C216457P1			
18V	3T3457	43C216457P1			
18VE	RSOM	58020479-012			
18W	3T3457	43C216457P1			
18X	3T3457	43C216457P1			
24AE	P9	43A114748P9			
24CE	P1043	43C212092P1043			
24EE	P1043	43C212092P1043			
24GE	P9	43A114748P9			
24JE	P1043	43C212092P1043			
24LE	P1043	43C212092P1043			
24NE	P9	43A114748P9			
24QE	P1043	43C212092P1043			
24SE	P1043	43C212092P1043			
24UE	P9	43A114748P9			
24WE	P1043	43C212092P1043			
27A	1V3569	58002569-001			
27B	1V3569	58002569-001			
27C	1V3569	58002569-001			
27D	1B-017	58002017-001			
27E	1B-053	58002053-001			
27F	1B-017	58002017-001			
27H	4G4408	43C216408P1			
27J	1B3441	43C216441P1			
27K	1B3441	43C216441P1			
27L	1B3441	43C216441P1			
27M	1B3441	43C216441P1			
27N	1B3441	43C216441P1			
27P	1B3441	43C216441P1			
27Q	1B3441	43C216441P1			

COMP INSTL LIST - WDAEI

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
27R	1D3491	58002491-001			
27S	1D3491	58002491-001			
27V	1V3569	58002569-001			
27W	1V3569	58002569-001			
27X	1V3569	58002569-001			
32AE	P9	43A114748P9			
32CE	P1043	43C212092P1043			
32EE	P1043	43C212092P1043			
32GE	P9	43A114748P9			
32JE	P1043	43C212092P1043			
32LE	P1043	43C212092P1043			
32NE	P9	43A114748P9			
32QE	P1043	43C212092P1043			
32SE	P1043	43C212092P1043			
32UE	P9	43A114748P9			
32WE	P1043	43C212092P1043			
36A	1V3569	58002569-001			
36B	1V3569	58002569-001			
36C	1V3569	58002569-001			
36D	RN9A	43B216592P22			
36E	1B-653	58002653-001			
36F	1B-015	58002015-001			
36G	4G4408	43C216408P1			
36H	1B-495	58002495-001			
36J	1B-053	58002053-001			
36K	1V3569	58002569-001			
36L	1V3569	58002569-001			
36M	1V3569	58002569-001			
36N	1D3491	58002491-001			
36P	1D3491	58002491-001			
36Q	1E-011	58002011-001			
36R	1D3491	58002491-001			
36S	1D3491	58002491-001			
36U	1V3569	58002569-001			
36V	1V3569	58002569-001			
36W	1V3569	58002569-001			
36X	1V3569	58002569-001			
40AE	P9	43A114748P9			

COMP INSTL LIST - WDAEI

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
40CE	P1043	43C212092P1043			
40EE	P1043	43C212092P1043			
40GE	P9	43A114748P9			
40JE	P1043	43C212092P1043			
40LE	P1043	43C212092P1043			
40NE	P9	43A114748P9			
40QE	P1043	43C212092P1043			
40SE	P1043	43C212092P1043			
40UE	P9	43A114748P9			
40WE	P1043	43C212092P1043			
44D	1B-728	58002728-001			
44E	1B-015	58002015-001			
44F	1B-653	58002653-001			
44G	1B-017	58002017-001			
44H	1B-053	58002053-001			
44J	1B-495	58002495-001			
45A	1B-045	58002045-001			
45B	1B-045	58002045-001			
45C	1B-045	58002045-001			
45FE	RSOH	58020479-008			
45K	1V3569	58002569-001			
45L	1V3569	58002569-001			
45M	1V3569	58002569-001			
45N	1D3491	58002491-001			
45P	1D3491	58002491-001			
45R	1D3491	58002491-001			
45S	1D3491	58002491-001			
45T	1B-478	58002478-001			
45U	1B-728	58002728-001			
45V	1B-664	58002664-001			
45W	1B-473	58002473-001			
45X	RN9A	43B216592P22			
48AE	P9	43A114748P9			
48CE	P1043	43C212092P1043			
48EE	P1043	43C212092P1043			
48GE	P9	43A114748P9			
48JE	P1043	43C212092P1043			
48LE	P1043	43C212092P1043			

COMP INSTL LIST - WDAEI

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
48NE	P9	43A114748P9			
48QE	P1043	43C212092P1043			
48SE	P1043	43C212092P1043			
48UE	P9	43A114748P9			
48WE	P1043	43C212092P1043			
52D	1B-045	58002045-001			
52E	1B-475	58002475-001			
52F	1B-653	58002653-001			
52G	1B-653	58002653-001			
52H	1B-495	58002495-001			
52J	1B-015	58002015-001			
53U	1Q-483	58002483-001			
53W	1B-017	58002017-001			
53X	1B-053	58002053-001			
54A	1V3569	58002569-001			
54B	1V3569	58002569-001			
54C	1V3569	58002569-001			
54K	1V3569	58002569-001			
54L	1V3569	58002569-001			
54M	1V3569	58002569-001			
54N	1D3491	58002491-001			
54P	1D3491	58002491-001			
54Q	1B3461	43C216461P1			
54R	1D3491	58002491-001			
54S	1D3491	58002491-001			
54T	1Q-616	58002616-001			
54TE	RSOH	58020479-008			
56AE	P9	43A114748P9			
56CE	P1043	43C212092P1043			
56EE	P1043	43C212092P1043			
56GE	P9	43A114748P9			
56JE	P1043	43C212092P1043			
56LE	P1043	43C212092P1043			
56NE	P9	43A114748P9			
56QE	P1043	43C212092P1043			
56SE	P1043	43C212092P1043			
56UE	P9	43A114748P9			
56WE	P1043	43C212092P1043			

COMP INSTL LIST - WDAEI

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
60D	1B-017	58002017-001			
60F	1Q-483	58002483-001			
60G	1Q-483	58002483-001			
60H	1R3440	43C216440P1			
60J	1Q-483	58002483-001			
61W	1B-017	58002017-001			
61X	1B-472	58002472-001			
62U	1Q-483	58002483-001			
62V	1R3440	43C216440P1			
63A	1V3569	58002569-001			
63B	1V3569	58002569-001			
63C	1V3569	58002569-001			
63K	1V3569	58002569-001			
63L	1V3569	58002569-001			
63M	1V3569	58002569-001			
63N	1D3491	58002491-001			
63P	1D3491	58002491-001			
63Q	1B3461	43C216461P1			
63S	1Q-071	58002071-001			
63T	1Q-483	58002483-001			
64AE	P9	43A114748P9			
64CE	P1043	43C212092P1043			
64EE	P1043	43C212092P1043			
64GE	P9	43A114748P9			
64JE	P1043	43C212092P1043			
64LE	P1043	43C212092P1043			
64NE	P9	43A114748P9			
64QE	P1043	43C212092P1043			
64SE	P1043	43C212092P1043			
64UE	P9	43A114748P9			
64WE	P1043	43C212092P1043			
69D	1B-053	58002053-001			
69E	1B-015	58002015-001			
69F	1B-017	58002017-001			
69G	1B-653	58002653-001			
69H	1B-728	58002728-001			
69J	RN3C	43B216592P12			
69W	4G4408	43C216408P1			

COMP INSTL LIST - WDAEI

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
69X	1B-472	58002472-001			
71V	1R3440	43C216440P1			
72A	1B-045	58002045-001			
72AE	P9	43A114748P9			
72B	1B-045	58002045-001			
72C	1B-045	58002045-001			
72CE	P1043	43C212092P1043			
72EE	P1043	43C212092P1043			
72GE	P9	43A114748P9			
72JE	P1043	43C212092P1043			
72K	1R3440	43C216440P1			
72L	1R3440	43C216440P1			
72LE	P1043	43C212092P1043			
72M	1B3600	58002600-001			
72N	4G4408	43C216408P1			
72NE	P9	43A114748P9			
72P	1B3461	43C216461P1			
72Q	1B3461	43C216461P1			
72QE	P1043	43C212092P1043			
72S	2V-752	58002752-001			
72TE	P1043	43C212092P1043			
72UE	P9	43A114748P9			
72WE	P1043	43C212092P1043			
77D	1V-607	58002607-001			
77E	1V-607	58002607-001			
77G	4G4408	43C216408P1			
77H	4G4408	43C216408P1			
77J	4G4408	43C216408P1			
77X	4G4408	43C216408P1			
80AE	P9	43A114748P9			
80CE	P1043	43C212092P1043			
80EE	P1043	43C212092P1043			
80GE	P9	43A114748P9			
80JE	P1043	43C212092P1043			
80LE	P1043	43C212092P1043			
80NE	P9	43A114748P9			
80QE	P1043	43C212092P1043			
80TE	P1043	43C212092P1043			

COMP INSTL LIST - WDAEI

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
80U	1Q-668	58002668-001			
80UE	P9	43A114748P9			
80V	1Q-483	58002483-001			
80WE	P1043	43C212092P1043			
81A	1R3440	43C216440P1			
81B	1R3440	43C216440P1			
81K	1R3440	43C216440P1			
81L	1R3440	43C216440P1			
81M	1B3600	58002600-001			
81N	4G4408	43C216408P1			
81P	RN4D	43B216592P17			
81Q	1B3461	43C216461P1			
85D	614410	43C216410P1			
85E	614410	43C216410P1			
85F	614410	43C216410P1			
85G	614410	43C216410P1			
85H	1B-017	58002017-001			
85J	4G4408	43C216408P1			
85WA	RSOH	58020479-008			
85WD	RSOH	58020479-008			
85X	1B-473	58002473-001			
88AE	P9	43A114748P9			
88CE	P1043	43C212092P1043			
88EE	P1043	43C212092P1043			
88GE	P9	43A114748P9			
88JE	P1043	43C212092P1043			
88LE	P1043	43C212092P1043			
88NE	P9	43A114748P9			
88QE	P1043	43C212092P1043			
88TE	P1043	43C212092P1043			
88UE	P9	43A114748P9			
88WE	P1043	43C212092P1043			
89U	1N3450	43C216450P1			
89V	1U-487	58002487-001			
90A	1B3600	58002600-001			
90B	1B3600	58002600-001			
90C	1E-011	58002011-001			
92K	1B-714	58002714-001			

COMP INSTL LIST - WDAEI

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
92L	1B-713	58002713-001			
92M	1B3600	58002600-001			
92N	1B3600	58002600-001			
92P	1B3600	58002600-001			
92Q	1B-053	58002053-001			
92R	1B3600	58002600-001			
93D	4G4409	43C216409P1			
93E	4G4409	43C216409P1			
93F	4G4409	43C216409P1			
93G	4G4409	43C216409P1			
93H	4G4408	43C216408P1			
93J	4G4408	43C216408P1			
93S	4G4408	43C216408P1			
93T	4G4408	43C216408P1			
93W	1E-011	58002011-001			
93X	4G4408	43C216408P1			

58060527

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 001	002	003	004	005	006	007	008	PL ALL
A	LEVEL 1 ISSUE	83	01	27	J.M. Boyle 1-27-83	A								A
B	PHA0XS239	83	09	01	S. Miller	B								B
B1	Level 2 ENXS149		ND		G Drenth	B1								
C	PHA0XS409	84	02	02	G Drenth	C	C							C
D	PHA0XS459	84	03	23	G Drenth	OBSOLETE	D	D						D
E	PHA0XS469	84	05	11	G Drenth		OBSOLETE	E	E					E
F	PHA0XS584	84	10	22	E. Hecke			OBSOLETE	F	F				F
G	PHA0XS650	85	APR	25	G Drenth				OBSOLETE	G	G			G
H	PHA0NJ059	86	03	04	G Drenth					OBSOLETE	H	H		H
J	PHA0NJ063	86	05	21	D. Williams						OBSOLETE	J	J	J
K	PHA0NJ065	87	06	29	D. Williams							OBSOLETE	K	K

FOR CONTINUATION OF REVISION STATUS SEE SHEET

BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX, ARIZONA

CE 300 A-3 (1-79)

MADE BY P.M. DeCosta 82 Sep 8

APPROVED E. Southfield 1-19-83

REVISION STATUS FOR EACH PAGE, SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE FUNCTIONAL PWA WDAMP

SIZE	REVISION STATUS FOR	SHEET	REV
X	58060527	1 1	K

DIST. 30

					008	
*	1	X	58075890-006	A HDUHC PWA WDAMP	1	EA
*	1	X	58075890-106	A HDUHC PWA WDAMP	INTCH	EA
*	1	X	58075890-306	A HDUHC PWA WDAMP	INTCH	EA
*	1	X	58075890-506	A HDUHC PWA WDAMP	INTCH	EA
	2	A	58060528	D INSTL INSTR WDAMP	X	
	3	X	58060529-005	A FWACKT WDAMP-1	1	EA
	4	A	58060578-011	P ID LABEL FUNCT PWA	1	EA

FNC PWA WDAMP-1

SIGNAL NAME	PAGE
$BITCLK•010	24.0
$BITCLK•100	16.0
$DAU•012	25.0
$DAU•022	25.0
$DAU•132	25.0
$DAU-CLK•030	31.0
$DAU-CLK•130	31.0
$DAU-TOT-CLR•013	22.0
$DAU-TOT-CLR•020	30.0
$EXEC-CLK•040	31.0
$EXEC-CLK•140	31.0
$MP-CLK•020	6.0
$MP-CLK•100	5.0
$MP-CLK•110	6.0
$MP-TEST•000	6.0
$OSC•100	5.0
$PARTIAL-CLR•011	22.0
$PIT-16•100	15.0
$PIT-256•100	15.0
$PIT-4•010	24.0
$PIT-4•100	15.0
$PIT-8•100	15.0
$TEST-BITCLK•100	24.0
$TOT-PAR-CLR•010	22.0
$TOT-PAR-CLR•100	22.0
$XFER-CH-REG•140	35.0
$XFER-CH-REG•141	4.0
$XFER-CYHD•050	35.0
A-08•100	5.0
A-08•100	28.0
A-09•100	5.0
A-09•100	28.0
A-10•100	5.0
A-10•100	28.0
A-11•100	5.0
A-11•100	28.0
A-12•100	28.0
A-12•100	5.0
A-13•100	5.0
A-13•100	28.0
A-14•100	28.0
A-14•100	5.0
A-15•100	5.0
A-15•100	28.0
AD-0•100	27.0
AD-0•100	10.0
AD-0•100	9.0
AD-0•100	5.0
AD-1•100	5.0
AD-1•100	9.0
AD-1•100	27.0
AD-1•100	10.0
AD-2•100	9.0
AD-2•100	5.0
AD-2•100	27.0
AD-2•100	10.0
AD-3•100	10.0
AD-3•100	5.0
AD-3•100	9.0
AD-3•100	27.0
AD-4•100	5.0
AD-4•100	10.0
AD-4•100	27.0
AD-4•100	9.0
AD-5•100	9.0

SIGNAL NAME	PAGE
AD-5•100	5.0
AD-5•100	27.0
AD-5•100	10.0
AD-6•100	5.0
AD-6•100	10.0
AD-6•100	27.0
AD-6•100	9.0
AD-7•100	9.0
AD-7•100	10.0
AD-7•100	27.0
ANY-SEQ-ERR•100	17.0
BAUD-1200-300•100	28.0
BYT-CTR-LSB•101	4.0
BYT-LD-CNT•040	37.0
BYT-LD-CNT•041	4.0
BYTE-CTR-00•100	38.0
BYTE-CTR-01•100	38.0
BYTE-CTR-02•100	38.0
BYTE-CTR-03•100	38.0
BYTE-CTR-04•100	38.0
BYTE-CTR-05•100	38.0
BYTE-CTR-06•100	38.0
BYTE-CTR-07•100	38.0
BYTE-CTR-08•100	38.0
BYTE-CTR-09•100	38.0
BYTE-CTR-10•100	38.0
BYTE-CTR-11•100	38.0
BYTE-CTR-LSB•100	38.0
BYTE-CTR-NSB•100	38.0
BYTE-CTR-ONES•100	38.0
BYTE-CTR-ONES•110	31.0
CLR-ADR-EQ•100	20.0
CLR-CYHD-FULL•000	35.0
CLR-OR-SEDC•010	42.0
CLR-OR-SEDC•100	42.0
CMP-LSB•100	37.0
CMP-LSB•101	4.0
CMP-MSB•100	37.0
CMP-MSB•101	4.0
CNT-CMP-A-LD•100	34.0
CNT-CMP-A-LD•101	4.0
CNT-CMP-B-LD•100	33.0
CNT-CMP-B-LD•101	4.0
CNT-CMP-C-LD•100	34.0
CNT-CMP-C-LD•101	4.0
COMP-0•100	35.0
COMP-1•100	35.0
COMP-2•100	35.0
COMP-3•100	35.0
COMP-4•100	35.0
COMP-5•100	35.0
COMP-6•100	35.0
COMP-7•100	35.0
COMP-CTL-1•100	36.0
COMP-CTL-1•101	4.0
COMP-CTL-2•100	36.0
COMP-CTL-2•101	4.0
COMP-G1•100	36.0
COMP-G2•010	36.0
COMP-G2•100	36.0
COMPARE•010	37.0
COMPARE•110	37.0
COMPARE•120	31.0
CSYN-CNT-0•110	30.0
CSYN-CNT-0•120	30.0

SIGNAL NAME	PAGE
CSYN-CNT-1•110	30.0
CSYN-CNT-1•120	30.0
CSYN-CNT-2•110	30.0
CSYN-CNT-2•120	30.0
CSYN-CNT-3•110	30.0
CSYN-CNT-3•120	30.0
CSYN-CNT-4•110	30.0
CSYN-CNT-4•120	30.0
CSYN-CNT-5•110	30.0
CSYN-CNT-5•120	30.0
CSYN-CNT-6•110	30.0
CSYN-CNT-6•120	30.0
CSYN-CNT-7•110	30.0
CSYN-CNT-7•120	30.0
CY-HD-0•100	34.0
CY-HD-1•100	34.0
CY-HD-2•100	34.0
CY-HD-3•100	34.0
CY-HD-4•100	34.0
CY-HD-5•100	34.0
CY-HD-6•100	34.0
CY-HD-7•100	34.0
CYHD-0•100	34.0
CYHD-1•100	34.0
CYHD-2•100	34.0
CYHD-3•100	34.0
CYHD-4•100	34.0
CYHD-5•100	34.0
CYHD-6•100	34.0
CYHD-7•100	34.0
CYHD-FULL•000	35.0
CYHD-FULL•010	31.0
CYHD-FULL•100	35.0
CYL-L-0•100	34.0
CYL-L-1•100	34.0
CYL-L-2•100	34.0
CYL-L-3•100	34.0
CYL-L-4•100	34.0
CYL-L-5•100	34.0
CYL-L-6•100	34.0
CYL-L-7•100	34.0
D-ADR-EQ•100	18.0
D-ALE•100	5.0
D-ANY-HARD-ERR•010	17.0
D-ANY-HARD-ERR•120	17.0
D-CARRIER-HI•100	25.0
D-CTS-423•010	23.0
D-CTS-423•100	23.0
D-DEN•000	5.0
D-DEN•000	28.0
D-DSR-423•010	23.0
D-DSR-423•100	23.0
D-DTR•000	24.0
D-DTR•110	24.0
D-DTR-423•120	25.0
D-HARD-ERR•100	16.0
D-INT•100	17.0
D-INTA•000	5.0
D-NMI•100	23.0
D-PIT-WR•100	16.0
D-READY•100	5.0
D-RES-BAUD•100	16.0
D-RES-POMC•000	19.0
D-RES-TMR•100	16.0
D-RESET•010	26.0

SIGNAL NAME	PAGE
D-RESET•100	25.0
D-ROM-P•100	29.0
D-RTS•000	24.0
D-RTS•110	24.0
D-RTS-423•120	25.0
D-RXD-423•000	24.0
D-RXD-423•110	24.0
D-STB•100	28.0
D-TIMER-0•010	16.0
D-TIMER-0•100	16.0
D-TRAN•010	27.0
D-TRAN•100	28.0
D-TRAN•100	5.0
D-TXD•010	24.0
D-TXD•100	24.0
D-TXD-423•020	25.0
D-USART-TEST•000	24.0
D-USART-TEST•110	24.0
DAD-P•000	10.0
DATA-BUS0-0•100	16.0
DATA-BUS0-0•100	22.0
DATA-BUS0-0•100	20.0
DATA-BUS0-0•100	9.0
DATA-BUS0-0•100	19.0
DATA-BUS0-0•100	24.0
DATA-BUS0-0•100	22.0
DATA-BUS0-0•100	21.0
DATA-BUS0-0•100	17.0
DATA-BUS0-0•100	20.0
DATA-BUS0-1•100	16.0
DATA-BUS0-1•100	21.0
DATA-BUS0-1•100	22.0
DATA-BUS0-1•100	24.0
DATA-BUS0-1•100	20.0
DATA-BUS0-1•100	22.0
DATA-BUS0-1•100	17.0
DATA-BUS0-1•100	9.0
DATA-BUS0-1•100	19.0
DATA-BUS0-1•100	20.0
DATA-BUS0-2•100	21.0
DATA-BUS0-2•100	20.0
DATA-BUS0-2•100	17.0
DATA-BUS0-2•100	9.0
DATA-BUS0-2•100	24.0
DATA-BUS0-2•100	19.0
DATA-BUS0-2•100	16.0
DATA-BUS0-2•100	22.0
DATA-BUS0-2•100	20.0
DATA-BUS0-2•100	22.0
DATA-BUS0-3•100	21.0
DATA-BUS0-3•100	20.0
DATA-BUS0-3•100	24.0
DATA-BUS0-3•100	9.0
DATA-BUS0-3•100	17.0
DATA-BUS0-3•100	16.0
DATA-BUS0-3•100	21.0
DATA-BUS0-3•100	22.0

REV	AUTHORITY	DATE
C	PHAOX5584	84OCT15

DISTRIBUTION CODE C120-26

HONEYWELL
LOC CEO HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAMP LOGIC - PAGE CROSS REFERENCE

ASM REF 58075890-X05 | DATA BASE NIODAU/DAU$45/HMP | DFTG 84OCT15 | SIZE B | DWG NO 58075894 | SH 1.0 | REV C

58075894

REV	AUTHORITY	DATE
C	PHAOXS584	84OCT15

SIGNAL NAME	PAGE
DATA-BUSØ-3•1ØØ	19.Ø
DATA-BUSØ-4•1ØØ	21.Ø
DATA-BUSØ-4•1ØØ	9.Ø
DATA-BUSØ-4•1ØØ	24.Ø
DATA-BUSØ-4•1ØØ	21.Ø
DATA-BUSØ-4•1ØØ	19.Ø
DATA-BUSØ-4•1ØØ	22.Ø
DATA-BUSØ-4•1ØØ	16.Ø
DATA-BUSØ-4•1ØØ	22.Ø
DATA-BUSØ-4•1ØØ	2Ø.Ø
DATA-BUSØ-4•1ØØ	17.Ø
DATA-BUSØ-5•1ØØ	2Ø.Ø
DATA-BUSØ-5•1ØØ	24.Ø
DATA-BUSØ-5•1ØØ	16.Ø
DATA-BUSØ-5•1ØØ	17.Ø
DATA-BUSØ-5•1ØØ	21.Ø
DATA-BUSØ-5•1ØØ	22.Ø
DATA-BUSØ-5•1ØØ	9.Ø
DATA-BUSØ-5•1ØØ	21.Ø
DATA-BUSØ-5•1ØØ	22.Ø
DATA-BUSØ-5•1ØØ	19.Ø
DATA-BUSØ-6•1ØØ	19.Ø
DATA-BUSØ-6•1ØØ	16.Ø
DATA-BUSØ-6•1ØØ	22.Ø
DATA-BUSØ-6•1ØØ	21.Ø
DATA-BUSØ-6•1ØØ	17.Ø
DATA-BUSØ-6•1ØØ	28.Ø
DATA-BUSØ-6•1ØØ	9.Ø
DATA-BUSØ-6•1ØØ	22.Ø
DATA-BUSØ-6•1ØØ	2Ø.Ø
DATA-BUSØ-6•1ØØ	24.Ø
DATA-BUSØ-6•1ØØ	21.Ø
DATA-BUSØ-7•Ø1Ø	18.Ø
DATA-BUSØ-7•1ØØ	9.Ø
DATA-BUSØ-7•1ØØ	21.Ø
DATA-BUSØ-7•1ØØ	19.Ø
DATA-BUSØ-7•1ØØ	21.Ø
DATA-BUSØ-7•1ØØ	16.Ø
DATA-BUSØ-7•1ØØ	22.Ø
DATA-BUSØ-7•1ØØ	2Ø.Ø
DATA-BUSØ-7•1ØØ	22.Ø
DATA-BUSØ-7•1ØØ	24.Ø
DATA-BUSØ-7•1ØØ	17.Ø
DATA-BUSØ-7•1ØØ	28.Ø
DATA-BUS1-Ø•1ØØ	8.Ø
DATA-BUS1-Ø•1ØØ	11.Ø
DATA-BUS1-Ø•1ØØ	13.Ø
DATA-BUS1-Ø•1ØØ	1Ø.Ø
DATA-BUS1-1•1ØØ	8.Ø
DATA-BUS1-1•1ØØ	13.Ø
DATA-BUS1-1•1ØØ	11.Ø
DATA-BUS1-1•1ØØ	1Ø.Ø
DATA-BUS1-2•1ØØ	11.Ø
DATA-BUS1-2•1ØØ	13.Ø
DATA-BUS1-2•1ØØ	8.Ø
DATA-BUS1-2•1ØØ	1Ø.Ø
DATA-BUS1-3•1ØØ	8.Ø
DATA-BUS1-3•1ØØ	1Ø.Ø
DATA-BUS1-3•1ØØ	14.Ø
DATA-BUS1-3•1ØØ	11.Ø
DATA-BUS1-4•1ØØ	9.Ø
DATA-BUS1-4•1ØØ	14.Ø
DATA-BUS1-4•1ØØ	1Ø.Ø
DATA-BUS1-4•1ØØ	12.Ø
DATA-BUS1-5•1ØØ	14.Ø

SIGNAL NAME	PAGE
DATA-BUS1-5•1ØØ	12.Ø
DATA-BUS1-5•1ØØ	9.Ø
DATA-BUS1-5•1ØØ	1Ø.Ø
DATA-BUS1-6•1ØØ	14.Ø
DATA-BUS1-6•1ØØ	9.Ø
DATA-BUS1-6•1ØØ	12.Ø
DATA-BUS1-6•1ØØ	1Ø.Ø
DATA-BUS1-7•1ØØ	15.Ø
DATA-BUS1-7•1ØØ	12.Ø
DATA-BUS1-7•1ØØ	9.Ø
DATA-BUS1-7•1ØØ	1Ø.Ø
DATA-BUS1-P•1ØØ	8.Ø
DATA-BUS1-P•1ØØ	13.Ø
DATA-BUS1-P•1ØØ	15.Ø
DATA-BUS1-P•1ØØ	9.Ø
DAU-INIT•1ØØ	25.Ø
DAU-ON-LINE•1ØØ	29.Ø
DAU-RES•ØØØ	25.Ø
DAU-TROUBLE•ØØØ	3Ø.Ø
DBD-IN-Ø•ØØØ	8.Ø
DBD-IN-1•ØØØ	8.Ø
DBD-IN-2•ØØØ	8.Ø
DBD-IN-3•ØØØ	8.Ø
DBD-IN-4•ØØØ	8.Ø
DBD-IN-5•ØØØ	9.Ø
DBD-IN-6•ØØØ	9.Ø
DBD-IN-7•ØØØ	9.Ø
DBD-IN-P•ØØØ	9.Ø
DBD-SEL•1ØØ	7.Ø
DEF-CNT-Ø-3•1ØØ	42.Ø
DEF-CNT-4•1ØØ	42.Ø
DEF-CNT-4-6•11Ø	42.Ø
DEF-CNT-4-7•1ØØ	42.Ø
DEF-CNT-5•1ØØ	42.Ø
DEF-CNT-6•1ØØ	42.Ø
DEF-CNT-7•Ø1Ø	42.Ø
DEF-CNT-7•1ØØ	42.Ø
DEF-RW•15Ø	41.Ø
DEF-SI-RST•13Ø	42.Ø
DEF-SKP-INH•ØØØ	42.Ø
DEF-SKP-INH•1ØØ	42.Ø
DEF-SKP-INH•11Ø	31.Ø
DEF-SYN-ER•14Ø	42.Ø
DEF-SYNC-ERR•ØØØ	42.Ø
DEF-SYNC-ERR•Ø1Ø	31.Ø
DEF-WDSN•Ø2Ø	42.Ø
DEF-WDSN•Ø3Ø	31.Ø
DEF-WDSN•13Ø	42.Ø
DEF-WHEX•Ø2Ø	42.Ø
DEF-WHEX•Ø3Ø	31.Ø
DEFECT-SKP•11Ø	41.Ø
DEFECT-SKP•12Ø	3Ø.Ø
DEN-16KRAM-Ø•ØØØ	1Ø.Ø
DEN-16KRAM-1•ØØØ	1Ø.Ø
DEN-4KROM-Ø•ØØØ	1Ø.Ø
DEN-4KROM-1•ØØØ	1Ø.Ø
DEN-4KROM-2•ØØØ	1Ø.Ø
DEN-4KROM-3•ØØØ	1Ø.Ø
DEN-BD-READ•ØØØ	9.Ø
DEN-BD-SEL•ØØØ	7.Ø
DEN-BD-SEL•11Ø	7.Ø
DEN-BUSØ•ØØØ	27.Ø
DEN-BUS1•ØØØ	27.Ø
DEN-P•ØØØ	1Ø.Ø
DEN-PIT•ØØØ	19.Ø

SIGNAL NAME	PAGE
DEN-PIT•1ØØ	19.Ø
DEN-PITØ•ØØØ	19.Ø
DEN-PIT1•ØØØ	19.Ø
DEN-STATUS-Ø•ØØØ	2Ø.Ø
DEN-STATUS-1•ØØØ	2Ø.Ø
DEV-4XX•Ø3Ø	36.Ø
DEV-4XX•11Ø	3Ø.Ø
DEV-4XX•12Ø	3Ø.Ø
DEV-5Ø1•Ø4Ø	37.Ø
DEV-5Ø1•12Ø	3Ø.Ø
DEV-5Ø1•13Ø	3Ø.Ø
DHI-LEVEL-1•1ØØ	6.Ø
DHI-LEVEL-2•1ØØ	7.Ø
DIS-$MP•ØØØ	6.Ø
DLWR-ADR-EQ•ØØØ	18.Ø
DLWR-ADR-EQ•ØØ1	4.Ø
DMP-ERROR•1ØØ	16.Ø
DMP-ERROR•11Ø	27.Ø
DMP-ERROR•12Ø	27.Ø
DMP-POMC•1ØØ	23.Ø
DMPADR-Ø•Ø1Ø	1Ø.Ø
DMPADR-ØØ•1ØØ	6.Ø
DMPADR-Ø1•1ØØ	6.Ø
DMPADR-Ø2•1ØØ	6.Ø
DMPADR-Ø3•1ØØ	6.Ø
DMPADR-Ø4•1ØØ	6.Ø
DMPADR-Ø5•1ØØ	6.Ø
DMPADR-Ø6•1ØØ	6.Ø
DMPADR-Ø7•1ØØ	6.Ø
DMPADR-Ø8•1ØØ	6.Ø
DMPADR-Ø9•1ØØ	6.Ø
DMPADR-1•Ø1Ø	6.Ø
DMPADR-1Ø•1ØØ	6.Ø
DMPADR-1Ø•1Ø1	6.Ø
DMPADR-11•1ØØ	6.Ø
DMPADR-11•1Ø1	6.Ø
DMPADR-12•1ØØ	6.Ø
DMPADR-12•1Ø1	6.Ø
DMPADR-13•1ØØ	6.Ø
DMPADR-13•1Ø1	6.Ø
DMPADR-14•Ø11	16.Ø
DMPADR-14•1ØØ	6.Ø
DMPADR-14•1Ø1	6.Ø
DMPADR-15•Ø11	2Ø.Ø
DMPADR-15•1ØØ	6.Ø
DMPADR-15•1Ø1	6.Ø
DMPADR-4•Ø1Ø	7.Ø
DMPADR-5•Ø1Ø	7.Ø
DMPADR-6•Ø1Ø	7.Ø
DMPADR-8•1Ø1	6.Ø
DMPADR-9•1Ø1	6.Ø
DMPADR-P•ØØØ	1Ø.Ø
DMPADR-P•1ØØ	1Ø.Ø
DMPDTA-Ø•1ØØ	27.Ø
DMPDTA-1•1ØØ	27.Ø
DMPDTA-2•1ØØ	27.Ø
DMPDTA-3•1ØØ	27.Ø
DMPDTA-4•1ØØ	27.Ø
DMPDTA-5•1ØØ	27.Ø
DMPDTA-6•1ØØ	27.Ø
DMPDTA-7•1ØØ	27.Ø
DMPDTA-P•1ØØ	27.Ø
DOUBLE-DEF•Ø2Ø	41.Ø
DOUBLE-DEF•11Ø	41.Ø
DOUBLE-DEF•12Ø	3Ø.Ø

SIGNAL NAME	PAGE
DPAR-ERR•1ØØ	23.Ø
DPWR-UP-RES•1ØØ	5.Ø
DRAM-OR-BD•ØØØ	27.Ø
DRAM-OR-BD•1ØØ	27.Ø
DRD-ADR•ØØØ	2Ø.Ø
DREG-Ø•11Ø	3Ø.Ø
DREG-Ø•12Ø	3Ø.Ø
DREG-1•11Ø	3Ø.Ø
DREG-1•12Ø	3Ø.Ø
DREG-2•11Ø	3Ø.Ø
DREG-2•12Ø	3Ø.Ø
DREG-3•11Ø	3Ø.Ø
DREG-3•12Ø	3Ø.Ø
DREG-4•11Ø	3Ø.Ø
DREG-4•12Ø	3Ø.Ø
DREG-5•11Ø	3Ø.Ø
DREG-5•12Ø	3Ø.Ø
DREG-6•11Ø	3Ø.Ø
DREG-6•12Ø	3Ø.Ø
DREG-7•11Ø	3Ø.Ø
DREG-7•12Ø	3Ø.Ø
DREG-MASK-Ø•12Ø	36.Ø
DREG-MASK-1•12Ø	36.Ø
DREG-MASK-2•12Ø	36.Ø
DREG-MASK-3•12Ø	36.Ø
DREG-MASK-4•12Ø	37.Ø
DREG-MASK-5•12Ø	37.Ø
DREG-MASK-6•12Ø	37.Ø
DREG-MASK-7•12Ø	37.Ø
DRES-SEQ-HLT•ØØØ	17.Ø
DROM-P-Ø•1ØØ	29.Ø
DROM-P-1•1ØØ	29.Ø
DROM-P-2•1ØØ	29.Ø
DROM-P-3•1ØØ	29.Ø
DROM-P-ERR•1ØØ	29.Ø
DS-Ø-BØ•1ØØ	39.Ø
DS-Ø-B1•1ØØ	39.Ø
DS-Ø-B1•11Ø	31.Ø
DS-Ø-B2•1ØØ	39.Ø
DS-Ø-B2•11Ø	31.Ø
DS-Ø-B3•1ØØ	39.Ø
DS-Ø-B3•11Ø	31.Ø
DS-2-BØ•1ØØ	39.Ø
DS-2-B1•1ØØ	39.Ø
DS-2-B1•11Ø	31.Ø
DS-2-B2•1ØØ	39.Ø
DS-2-B2•11Ø	31.Ø
DS-2-B3•1ØØ	39.Ø
DS-2-B3•11Ø	31.Ø
DS-A-ØØ•1ØØ	39.Ø
DS-A-Ø1•1ØØ	39.Ø
DS-A-Ø2•1ØØ	39.Ø
DS-A-Ø3•1ØØ	39.Ø
DS-A-Ø4•1ØØ	39.Ø
DS-A-Ø5•1ØØ	39.Ø
DS-A-Ø6•1ØØ	39.Ø
DS-A-Ø7•1ØØ	39.Ø

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LOC CEO HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAMP LOGIC - PAGE CROSS REFERENCE

ASM REF 58Ø7589Ø-XØ5
DATA BASE NIODAU/DAU$45/HM
DR DFIG 84OCT15
SIZE B | DWG NO 58Ø75894 | SH 1.1 | REV C

58Ø75894

REV	AUTHORITY	DATE
C	PHAOXS584	84OCT15

SIGNAL NAME	PAGE
DS-A-08•100	39.0
DS-A-09•100	39.0
DS-A-10•100	39.0
DS-A-11•100	39.0
DS-B-00•100	39.0
DS-B-01•100	39.0
DS-B-02•100	39.0
DS-B-03•100	39.0
DS-B-04•100	40.0
DS-B-05•100	40.0
DS-B-06•100	40.0
DS-B-07•100	40.0
DS-B-08•100	40.0
DS-B-09•100	40.0
DS-B-10•100	40.0
DS-B-11•100	40.0
DS-CTR-EN•050	42.0
DS-CTR-EN•051	4.0
DS-CTR-EN0•040	41.0
DS-CTR-EN1•040	41.0
DS-SW-0•100	38.0
DS-SW-1•100	38.0
DS-SW-2•100	38.0
DS-SW-3•100	38.0
DS-SW-4•100	38.0
DS-SW-5•100	38.0
DS-SW-6•100	38.0
DS-SW-7•100	38.0
DS0-EN•000	38.0
DS0-LD•130	39.0
DS0-LD•131	4.0
DS0-LD-0•020	38.0
DS0-LD-1•020	39.0
DS1-EN•000	38.0
DS1-LD•130	39.0
DS1-LD•131	4.0
DS1-LD-0•020	39.0
DS1-LD-1•020	39.0
DS2-EN•000	38.0
DS2-LD•130	39.0
DS2-LD•131	4.0
DS2-LD-0•020	39.0
DS2-LD-1•020	39.0
DS3-EN•000	38.0
DS3-LD•130	39.0
DS3-LD•131	4.0
DS3-LD-0•020	39.0
DS3-LD-1•020	39.0
DSA-BYT-EQ•001	4.0
DSA-BYT-EQ•010	40.0
DSA-BYT-EQ•100	40.0
DSA-BYT-EQ•101	4.0
DSA-BYTE-EQ•010	40.0
DSB-BYT-EQ•001	4.0
DSB-BYT-EQ•010	40.0
DSB-BYT-EQ•100	40.0
DSB-BYT-EQ•101	4.0
DSB-BYTE-EQ•000	40.0
DSEL-ADR•000	19.0
DSEL-AUX•000	19.0
DSEL-BB•000	7.0
DSEL-BB•110	7.0
DSEL-BUS0•000	27.0
DSEL-ED•000	7.0
DSEL-ED•110	7.0

SIGNAL NAME	PAGE
DSEL-IF0•000	7.0
DSEL-IF0•110	7.0
DSEL-IF1•000	7.0
DSEL-IF1•110	7.0
DSEL-MP0•000	7.0
DSEL-MP1•100	19.0
DSEL-PIC•000	19.0
DSEL-PIT•000	19.0
DSEL-PIT•110	16.0
DSEL-ROMS•100	22.0
DSEL-SE0•000	7.0
DSEL-SE0•110	7.0
DSEL-SE1•000	7.0
DSEL-SE1•030	31.0
DSEL-SE1•110	7.0
DSEL-SE1•120	31.0
DSEL-STATUS-0•000	19.0
DSEL-STATUS-1•000	19.0
DSEL-STATUS-1•110	19.0
DSEL-USART•000	19.0
DSET-BD-ERR•100	23.0
DSET-RAM-ERR•100	23.0
DSET-ROM-ERR•100	22.0
DSR•000	24.0
DUPR-ADR-EQ•000	18.0
DUPR-ADR-EQ•001	4.0
DW-AUX•000	26.0
DWR-ADR-0•100	20.0
DWR-ADR-1•100	20.0
EN-DSR•000	24.0
EN-FMASK•100	36.0
EN-MP-CLK•100	6.0
ENAB-BC-MSB•110	37.0
ENABLE-DS•010	41.0
ENABLE-DS•100	41.0
F-ADR-EQ•100	18.0
F-EDAC-ERROR•110	16.0
F-EDAC-ERROR•120	16.0
F-RESET•100	25.0
FBD-ERR•000	23.0
FBD-ERR•100	23.0
FBD-ERR•110	23.9
FIPC-RESET•010	25.0
FIPC-RESET•120	25.0
FLAG-0•100	34.0
FLAG-1•100	34.0
FLAG-2•100	34.0
FLAG-3•100	34.0
FLAG-4•100	34.0
FLAG-5•100	34.0
FLAG-6•100	34.0
FLAG-7•100	34.0
FMASK-0•100	34.0
FMASK-1•100	34.0
FMASK-2•100	34.0
FMASK-3•100	34.0
FMASK-4•100	34.0
FMASK-5•100	34.0
FMASK-6•100	34.0
FMASK-7•100	34.0
FMASK-LD•100	33.0
FMASK-LD•101	4.0
FMP-ADDR-ERR•010	29.0
FMP-ADDR-ERR•020	29.0
FMP-ADDR-ERR•130	29.0

SIGNAL NAME	PAGE
FRAM-ERR•000	23.0
FRAM-ERR•100	23.0
FROM-ERR•000	23.0
FROM-ERR•100	23.0
FSEQ-EXEC•110	30.0
FSEQ-EXEC•120	30.0
FSEQ-HALT•100	17.0
FSEQ-RUN•110	16.0
FSEQ-RUN•120	16.0
GND-00D-08	26.0
GND-00F-08	28.0
GND-00G-08	28.0
GND-00P-08	23.0
GND-00P-08	24.0
GND-00S-08	42.0
GND-00T-08	41.0
GND-00U-08	41.0
GND-00W-08	38.0
GND-00X-08	38.0
GND-09E-12	29.0
GND-09R-08	37.0
GND-09S-08	37.0
GND-09W-07	37.0
GND-18W-08	40.0
GND-18X-08	40.0
GND-22E-08	29.0
GND-22G-10	18.0
GND-22H-10	17.0
GND-24K-20	5.0
GND-27M-07	6.0
GND-27Q-08	15.0
GND-34E-10	18.0
GND-34F-10	18.0
GND-35P-09	5.0
GND-36A-08	10.0
GND-36M-08	15.0
GND-36Q-07	33.0
GND-36R-08	33.0
GND-43G-10	6.0
GND-43H-10	6.0
GND-43J-10	6.0
GND-45M-08	23.0
GND-45N-08	15.0
GND-45P-08	25.0
GND-45Q-08	42.0
GND-45R-08	33.0
GND-54L-08	29.0
GND-54M-08	23.0
GND-54M-08	25.0
GND-54P-10	34.0
GND-54Q-08	31.0
GND-54U-08	35.0
GND-54V-08	35.0
GND-54W-08	35.0
GND-54X-08	35.0
GND-63G-08	9.0
GND-63H-08	8.0
GND-63Q-08	31.0
GND-63S-08	38.0
GND-63T-08	38.0
GND-63X-08	38.0
GND-72G-08	8.0
GND-72H-08	8.0
GND-72J-08	8.0
GND-72N-08	16.0

SIGNAL NAME	PAGE
GND-72P-08	17.0
GND-72Q-08	31.0
GND-72R-08	36.0
GND-72W-08	31.0
GND-72X-08	31.0
GND-81G-08	9.0
GND-81H-08	8.0
GND-81J-08	8.0
GND-81N-07	10.0
GND-81T-08	30.0
GND-81U-08	30.0
GND-81V-08	30.0
GND-81W-08	30.0
GND-81X-08	30.0
GND-90G-08	9.0
GND-90H-08	9.0
GND-90J-08	9.0
GND-90N-08	27.0
GND-90P-08	27.0
GND-90Q-10	40.0
GND-90R-10	39.0
GND-90S-10	39.0
GND-90T-10	39.0
GND-90U-10	34.0
GND-90V-10	34.0
GND-90W-10	34.0
GND-90X-10	34.0
HI-LVL-0•100	37.0
HI-LVL-1•100	19.0
IF0-ON-LINE•000	29.0
IF0-ON-LINE•010	29.0
IF1-ON-LINE•000	29.0
IF1-ON-LINE•010	29.0
MASK-0•010	36.0
MASK-1•010	36.0
MASK-2•010	36.0
MASK-3•010	36.0
MASK-4•010	36.0
MASK-5•010	36.0
MASK-6•010	36.0
MASK-7•010	36.0
MP-ADDR-13•110	31.0
MP-ADDR-14•110	31.0
MP-ADDR-15•110	31.0
MP-ADEC-00•000	32.0
MP-ADEC-01•000	32.0
MP-ADEC-02•000	32.0
MP-ADEC-03•000	32.0
MP-ADEC-04•000	32.0
MP-ADEC-05•000	32.0
MP-ADEC-06•000	32.0
MP-ADEC-07•000	32.0
MP-ADR-CMP•010	18.0
MP-DATA-0•110	31.0
MP-DATA-1•110	31.0
MP-DATA-2•110	31.0
MP-DATA-3•110	31.0

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LOC CEO HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- HDAMP LOGIC - PAGE CROSS REFERENCE

ASM REF 58075890-X05

DATA BASE NIODAU/DAU$45/HM

DFTG 84OCT15

SIZE	DWG NO	SH	REV
B	58075894	1.2	C

58075894

REV	AUTHORITY	DATE
C	PHAOXS584	84OCT15

SIGNAL NAME	PAGE
MP-DATA-4•11Ø	31.Ø
MP-DATA-5•11Ø	31.Ø
MP-DATA-6•11Ø	31.Ø
MP-DATA-7•11Ø	31.Ø
MP-RD•13Ø	31.Ø
MP-WR•Ø4Ø	31.Ø
MP-WR•13Ø	31.Ø
MPRD•ØØØ	5.Ø
MPRD•ØØØ	28.Ø
MPRD•11Ø	6.Ø
MPRD•12Ø	27.Ø
MPWR•ØØØ	5.Ø
MPWR•ØØØ	28.Ø
MPWR•Ø1Ø	6.Ø
MPWR•12Ø	6.Ø
MPWR•13Ø	27.Ø
OP22-LCSN•Ø1Ø	3Ø.Ø
OP22-LCSN•Ø2Ø	3Ø.Ø
OP22-LCSN•13Ø	35.Ø
OP33-45-63-72•14Ø	37.Ø
OP35-SEDC•Ø1Ø	3Ø.Ø
OP35-SEDC•Ø2Ø	3Ø.Ø
OP41-42•12Ø	3Ø.Ø
OP41-42•13Ø	3Ø.Ø
OP45-RDDS•Ø1Ø	3Ø.Ø
OP45-RDDS•Ø2Ø	3Ø.Ø
OP45-RDDS•13Ø	41.Ø
OP5Ø-66•Ø1Ø	3Ø.Ø
OP5Ø-66•Ø2Ø	3Ø.Ø
OP63-72•Ø2Ø	3Ø.Ø
OP63-72•Ø3Ø	3Ø.Ø
OP63-72•14Ø	41.Ø
P-EDAC-DATA-P•1ØØ	9.Ø
POMC•Ø1Ø	23.Ø
POMC•1ØØ	23.Ø
POWER-CONF•Ø1Ø	23.Ø
POWER-CONF•1ØØ	23.Ø
POWER-CONF•12Ø	23.Ø
PRDREGØ-P•1ØØ	9.Ø
PRDREG1-P•1ØØ	9.Ø
PRES-RD•11Ø	41.Ø
PRESET-BC3•14Ø	38.Ø
PRESET-DS•1ØØ	41.Ø
PRTY-EVEN-MARK•1ØØ	28.Ø
R-EDAC-DATA-Ø•11Ø	8.Ø
R-EDAC-DATA-1•11Ø	8.Ø
R-EDAC-DATA-2•11Ø	8.Ø
R-EDAC-DATA-3•11Ø	8.Ø
R-EDAC-DATA-4•11Ø	8.Ø
R-EDAC-DATA-5•11Ø	9.Ø
R-EDAC-DATA-6•11Ø	9.Ø
R-EDAC-DATA-7•11Ø	9.Ø
RAUX-Ø•1ØØ	26.Ø
RAUX-1•Ø1Ø	26.Ø
RAUX-1•Ø2Ø	26.Ø
RAUX-1•Ø21	3Ø.Ø
RAUX-1•1ØØ	26.Ø
RAUX-1•11Ø	29.Ø
RAUX-2•Ø1Ø	26.Ø
RAUX-2•Ø2Ø	26.Ø
RAUX-2•1ØØ	26.Ø
RAUX-3•Ø1Ø	26.Ø
RAUX-3•Ø2Ø	26.Ø
RAUX-3•1ØØ	26.Ø
RAUX-4•Ø1Ø	26.Ø

SIGNAL NAME	PAGE
RAUX-4•Ø2Ø	26.Ø
RAUX-4•1ØØ	26.Ø
RAUX-5•Ø1Ø	26.Ø
RAUX-5•Ø2Ø	26.Ø
RAUX-5•1ØØ	26.Ø
RAUX-6•Ø1Ø	26.Ø
RAUX-6•Ø2Ø	26.Ø
RAUX-6•1ØØ	26.Ø
RAUX-7•Ø1Ø	26.Ø
RAUX-7•Ø2Ø	26.Ø
RAUX-7•1ØØ	26.Ø
RBUF-RDOUT-Ø•1ØØ	8.Ø
RBUF-RDOUT-1•1ØØ	8.Ø
RBUF-RDOUT-2•1ØØ	8.Ø
RBUF-RDOUT-3•1ØØ	8.Ø
RBUF-RDOUT-4•1ØØ	8.Ø
RBUF-RDOUT-5•1ØØ	9.Ø
RBUF-RDOUT-6•1ØØ	9.Ø
RBUF-RDOUT-7•1ØØ	9.Ø
RBUF-RDOUT-P•1ØØ	9.Ø
RCMP-ADR-ØØ•1ØØ	17.Ø
RCMP-ADR-Ø1•1ØØ	17.Ø
RCMP-ADR-Ø2•1ØØ	17.Ø
RCMP-ADR-Ø3•1ØØ	17.Ø
RCMP-ADR-Ø4•1ØØ	17.Ø
RCMP-ADR-Ø5•1ØØ	17.Ø
RCMP-ADR-Ø6•1ØØ	17.Ø
RCMP-ADR-Ø7•1ØØ	17.Ø
RCMP-ADR-Ø8•1ØØ	18.Ø
RCMP-ADR-Ø9•1ØØ	18.Ø
RCMP-ADR-1Ø•1ØØ	18.Ø
RCMP-ADR-11•1ØØ	18.Ø
RCMP-ADR-12•1ØØ	18.Ø
RCMP-ADR-13•1ØØ	18.Ø
RCMP-ADR-14•1ØØ	18.Ø
RCMP-ADR-15•1ØØ	18.Ø
RD-DDS•Ø4Ø	41.Ø
RD-OR-WR•1ØØ	1Ø.Ø
READ-BYT-CNT•1ØØ	41.Ø
RES-RESET•Ø2Ø	25.Ø
RES-RESET•11Ø	25.Ø
RRDREGØ-Ø•1ØØ	8.Ø
RRDREGØ-1•1ØØ	8.Ø
RRDREGØ-2•1ØØ	8.Ø
RRDREGØ-3•1ØØ	8.Ø
RRDREGØ-4•1ØØ	8.Ø
RRDREGØ-5•1ØØ	9.Ø
RRDREGØ-6•1ØØ	9.Ø
RRDREGØ-7•1ØØ	9.Ø
RRDREG1-Ø•1ØØ	8.Ø
RRDREG1-1•1ØØ	8.Ø
RRDREG1-2•1ØØ	8.Ø
RRDREG1-3•1ØØ	8.Ø
RRDREG1-4•1ØØ	8.Ø
RRDREG1-5•1ØØ	9.Ø
RRDREG1-6•1ØØ	9.Ø
RRDREG1-7•1ØØ	9.Ø
RRES-RES•ØØØ	25.Ø
SEQ-ERR•12Ø	16.Ø
SEQ-ERR•13Ø	16.Ø
SEQ-RO-Ø•1ØØ	8.Ø
SEQ-RO-1•1ØØ	8.Ø
SEQ-RO-2•1ØØ	8.Ø
SEQ-RO-3•1ØØ	8.Ø
SEQ-RO-4•1ØØ	8.Ø

SIGNAL NAME	PAGE
SEQ-RO-5•1ØØ	9.Ø
SEQ-RO-6•1ØØ	9.Ø
SEQ-RO-7•1ØØ	9.Ø
SEQ-RO-P•1ØØ	9.Ø
SEQ-STATE-6•11Ø	3Ø.Ø
SEQ-STATE-6•12Ø	3Ø.Ø
SEQ-STATE-7•11Ø	3Ø.Ø
SEQ-STATE-7•12Ø	3Ø.Ø
SEQX-RO-Ø•1ØØ	33.Ø
SEQX-RO-1•1ØØ	33.Ø
SEQX-RO-2•1ØØ	33.Ø
SEQX-RO-3•1ØØ	33.Ø
SEQX-RO-4•1ØØ	33.Ø
SEQX-RO-5•1ØØ	33.Ø
SEQX-RO-6•1ØØ	33.Ø
SEQX-RO-7•1ØØ	33.Ø
SEQX-RO-P•1ØØ	33.Ø
SEQX-RO-SW-Ø•1ØØ	32.Ø
SEQX-RO-SW-1•1ØØ	32.Ø
SEQX-RO-SW-2•1ØØ	32.Ø
SEQX-RO-SW-3•1ØØ	32.Ø
SEQX-RO-SW-4•1ØØ	32.Ø
SEQX-RO-SW-5•1ØØ	33.Ø
SEQX-RO-SW-6•1ØØ	33.Ø
SEQX-RO-SW-7•1ØØ	33.Ø
SET-RES-PIT-GT•1ØØ	19.Ø
STAT-ERR•11Ø	16.Ø
STAT-ERR•12Ø	16.Ø
SWITCH-RESET•ØØØ	16.Ø
SWITCH-RESET•Ø1Ø	16.Ø
SWITCH-RESET•12Ø	25.Ø
T-A-IN-Ø•1ØØ	28.Ø
T-A-IN-1•1ØØ	28.Ø
T-A-IN-2•1ØØ	28.Ø
T-A-IN-3•1ØØ	28.Ø
T-A-IN-4•1ØØ	28.Ø
T-A-IN-5•1ØØ	28.Ø
T-A-IN-6•1ØØ	28.Ø
T-A-IN-7•1ØØ	28.Ø
T-A-OUT-Ø8•1ØØ	28.Ø
T-A-OUT-Ø9•1ØØ	28.Ø
T-A-OUT-1Ø•1ØØ	28.Ø
T-A-OUT-11•1ØØ	28.Ø
T-A-OUT-12•1ØØ	28.Ø
T-A-OUT-13•1ØØ	28.Ø
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T-A-OUT-15•1ØØ	28.Ø
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T-AD-IN-5•1ØØ	27.Ø
T-AD-IN-6•1ØØ	27.Ø
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T-AD-OUT-1•1ØØ	27.Ø
T-AD-OUT-2•1ØØ	27.Ø
T-AD-OUT-3•1ØØ	27.Ø
T-AD-OUT-4•1ØØ	27.Ø
T-AD-OUT-5•1ØØ	27.Ø
T-AD-OUT-6•1ØØ	27.Ø
T-AD-OUT-7•1ØØ	27.Ø
T-ALE•ØØØ	28.Ø
T-ALE•11Ø	28.Ø

SIGNAL NAME	PAGE
T-DEN•ØØØ	28.Ø
T-HOLD•ØØØ	28.Ø
T-HOLD•Ø2Ø	28.Ø
T-HOLD•11Ø	28.Ø
T-LOAD•ØØØ	15.Ø
T-LOAD•Ø1Ø	29.Ø
T-LOAD•12Ø	29.Ø
T-MPRD•ØØØ	28.Ø
T-MPWR•ØØØ	28.Ø
T-TRAN•1ØØ	28.Ø
TEST•ØØØ	28.Ø
TEST•Ø2Ø	2Ø.Ø
TEST•11Ø	28.Ø
TND-HARD-ERR•1ØØ	17.Ø
TND-SOFT-ERR•1ØØ	17.Ø
WR-DDS•Ø4Ø	41.Ø
WR-SDS•Ø4Ø	41.Ø
XFER-REG•Ø1Ø	35.Ø

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TITLE LOGIC DIAGRAM- WDAMP LOGIC - PAGE CROSS REFERENCE

ASM REF 58Ø7589Ø-XØ5 | DATA BASE NIODAU/DAU$45/HMP | OR DFIG 84OCT15 | SIZE B | DWG NO 58Ø75894 | SH 1.3 | REV C

58Ø75894

I/O PIN		PAGE	SIGNAL NAME
LAØØ	O	25.Ø	D-DTR-423•12Ø
LAØ1	O	25.Ø	D-RTS-423•12Ø
LAØ2	O	25.Ø	D-TXD-423•Ø2Ø
LAØ6	O	25.Ø	D-CARRIER-HI•1ØØ
LAØ9	I	23.Ø	D-CTS-423•1ØØ
LA1Ø	I	23.Ø	D-DSR-423•1ØØ
LA12	I	24.Ø	D-RXD-423•ØØØ
LA2Ø	I	24.Ø	EN-DSR•ØØØ
LA21	I	24.Ø	EN-DSR•ØØØ
LB12	I	28.Ø	PRTY-EVEN-MARK•1ØØ
LB14	I	28.Ø	BAUD-12ØØ-3ØØ•1ØØ
LCØØ	O	4.Ø	$XFER-CH-REG•141
LCØ1	O	4.Ø	DUPR-ADR-EQ•ØØ1
LCØ2	O	4.Ø	DLWR-ADR-EQ•ØØ1
LCØ3	O	4.Ø	FMASK-LD•1Ø1
LCØ4	O	4.Ø	CNT-CMP-B-LD•1Ø1
LCØ5	O	4.Ø	CNT-CMP-A-LD•1Ø1
LCØ6	O	4.Ø	CNT-CMP-C-LD•1Ø1
LCØ7	O	4.Ø	COMP-CTL-2•1Ø1
LCØ8	O	4.Ø	DSØ-LD•131
LCØ9	O	4.Ø	COMP-CTL-1•1Ø1
LC1Ø	O	4.Ø	CMP-MSB•1Ø1
LC12	O	4.Ø	DS1-LD•131
LC13	O	4.Ø	BYT-LD-CNT•Ø41
LC14	O	4.Ø	BYT-CTR-LSB•1Ø1
LC16	O	4.Ø	DSA-BYT-EQ•1Ø1
LC17	O	4.Ø	DSB-BYT-EQ•1Ø1
LC18	O	4.Ø	DSA-BYT-EQ•ØØ1
LC19	O	4.Ø	DSB-BYT-EQ•ØØ1
LC2Ø	O	4.Ø	DS-CTR-EN•Ø51
LDØØ	O	4.Ø	DS2-LD•131
LDØ1	O	4.Ø	CMP-LSB•1Ø1
LDØ2	I	6.Ø	$MP-TEST•ØØØ
LDØ3	I	6.Ø	EN-MP-CLK•1ØØ
LDØ4	I	24.Ø	D-USART-TEST•ØØØ
LDØ5	I	19.Ø	HI-LVL-1•1ØØ
LDØ7	O	4.Ø	DS3-LD•131
LD1Ø	O	6.Ø	$MP-CLK•Ø2Ø
RAØØ	O	26.Ø	RAUX-1•Ø1Ø
RAØ1	O	26.Ø	RAUX-2•Ø1Ø
RAØ2	O	26.Ø	RAUX-3•Ø1Ø
RAØ3	O	26.Ø	RAUX-4•Ø1Ø
RAØ4	O	26.Ø	RAUX-5•Ø1Ø
RAØ5	O	26.Ø	RAUX-6•Ø1Ø
RAØ6	O	26.Ø	RAUX-7•Ø1Ø
RB12	I	15.Ø	T-LOAD•ØØØ
RB13	I	28.Ø	TEST•ØØØ
RB15	I	28.Ø	T-HOLD•ØØØ
RB16	I	28.Ø	T-MPWR•ØØØ
RB17	I	28.Ø	T-MPRD•ØØØ
RB18	I	28.Ø	T-DEN•ØØØ
RB19	I	28.Ø	T-TRAN•1ØØ
RCØØ	O	28.Ø	T-A-OUT-Ø8•1ØØ
RCØ1	O	28.Ø	T-A-OUT-Ø9•1ØØ
RCØ2	O	28.Ø	T-A-OUT-1Ø•1ØØ
RCØ3	O	28.Ø	T-A-OUT-11•1ØØ
RCØ4	O	28.Ø	T-A-OUT-12•1ØØ
RCØ5	O	28.Ø	T-A-OUT-13•1ØØ
RCØ6	O	28.Ø	T-A-OUT-14•1ØØ
RCØ7	O	28.Ø	T-A-OUT-15•1ØØ
RC12	I	28.Ø	T-A-IN-Ø•1ØØ
RC13	I	28.Ø	T-A-IN-1•1ØØ
RC14	I	28.Ø	T-A-IN-2•1ØØ
RC15	I	28.Ø	T-A-IN-3•1ØØ
RC16	I	28.Ø	T-A-IN-4•1ØØ
RC17	I	28.Ø	T-A-IN-5•1ØØ
RC18	I	28.Ø	T-A-IN-6•1ØØ
RC19	I	28.Ø	T-A-IN-7•1ØØ
RDØØ	O	27.Ø	T-AD-OUT-Ø•1ØØ
RDØ1	O	27.Ø	T-AD-OUT-1•1ØØ
RDØ2	O	27.Ø	T-AD-OUT-2•1ØØ
RDØ3	O	27.Ø	T-AD-OUT-3•1ØØ
RDØ4	O	27.Ø	T-AD-OUT-4•1ØØ
RDØ5	O	27.Ø	T-AD-OUT-5•1ØØ
RDØ6	O	27.Ø	T-AD-OUT-6•1ØØ
RDØ7	O	27.Ø	T-AD-OUT-7•1ØØ
RD12	I	27.Ø	T-AD-IN-Ø•1ØØ
RD13	I	27.Ø	T-AD-IN-1•1ØØ
RD14	I	27.Ø	T-AD-IN-2•1ØØ
RD15	I	27.Ø	T-AD-IN-3•1ØØ
RD16	I	27.Ø	T-AD-IN-4•1ØØ
RD17	I	27.Ø	T-AD-IN-5•1ØØ
RD18	I	27.Ø	T-AD-IN-6•1ØØ
RD19	I	27.Ø	T-AD-IN-7•1ØØ
WA12	I	8.Ø	SEQ-RO-Ø•1ØØ
WA13	I	8.Ø	SEQ-RO-1•1ØØ
WA14	I	8.Ø	SEQ-RO-2•1ØØ
WA15	I	8.Ø	SEQ-RO-3•1ØØ
WA16	I	8.Ø	SEQ-RO-4•1ØØ
WA17	I	9.Ø	SEQ-RO-5•1ØØ
WA18	I	9.Ø	SEQ-RO-6•1ØØ
WA19	I	9.Ø	SEQ-RO-7•1ØØ
WA2Ø	I	9.Ø	SEQ-RO-P•1ØØ
WBØØ	I	8.Ø	RRDREGØ-Ø•1ØØ
WBØ1	I	8.Ø	RRDREGØ-1•1ØØ
WBØ2	I	8.Ø	RRDREGØ-2•1ØØ
WBØ3	I	8.Ø	RRDREGØ-3•1ØØ
WBØ4	I	8.Ø	RRDREGØ-4•1ØØ
WBØ5	I	9.Ø	RRDREGØ-5•1ØØ
WBØ6	I	9.Ø	RRDREGØ-6•1ØØ
WBØ7	I	9.Ø	RRDREGØ-7•1ØØ
WBØ8	I	9.Ø	PRDREGØ-P•1ØØ
WB12	I	8.Ø	RRDREG1-Ø•1ØØ
WB13	I	8.Ø	RRDREG1-1•1ØØ
WB14	I	8.Ø	RRDREG1-2•1ØØ
WB15	I	8.Ø	RRDREG1-3•1ØØ
WB16	I	8.Ø	RRDREG1-4•1ØØ
WB17	I	9.Ø	RRDREG1-5•1ØØ
WB18	I	9.Ø	RRDREG1-6•1ØØ
WB19	I	9.Ø	RRDREG1-7•1ØØ
WB2Ø	I	9.Ø	PRDREG1-P•1ØØ
WCØØ	I	8.Ø	RBUF-RDOUT-Ø•1ØØ
WCØ1	I	8.Ø	RBUF-RDOUT-1•1ØØ
WCØ2	I	8.Ø	RBUF-RDOUT-2•1ØØ
WCØ3	I	8.Ø	RBUF-RDOUT-3•1ØØ
WCØ4	I	8.Ø	RBUF-RDOUT-4•1ØØ
WCØ5	I	9.Ø	RBUF-RDOUT-5•1ØØ
WCØ6	I	9.Ø	RBUF-RDOUT-6•1ØØ
WCØ7	I	9.Ø	RBUF-RDOUT-7•1ØØ
WCØ8	I	9.Ø	RBUF-RDOUT-P•1ØØ
WCØ9	I	22.Ø	$DAU-TOT-CLR•Ø13
WD13	I	28.Ø	T-ALE•ØØØ
WD15	I	16.Ø	FSEQ-RUN•11Ø
WD16	O	23.Ø	FBD-ERR•11Ø
WD17	O	18.Ø	MP-ADR-CMP•Ø1Ø
WD18	I	17.Ø	D-ANY-HARD-ERR•Ø1Ø
WD2Ø	O	27.Ø	DMP-ERROR•12Ø
WEØ4	I	25.Ø	$DAU•Ø12
WEØ6	O	7.Ø	DSEL-IFØ•11Ø
WEØ7	O	7.Ø	DSEL-IF1•11Ø
WEØ8	O	7.Ø	DSEL-BB•11Ø
WEØ9	O	7.Ø	DSEL-ED•11Ø
WE1Ø	O	7.Ø	DSEL-SEØ•11Ø
WE12	I	8.Ø	R-EDAC-DATA-Ø•11Ø
WE13	I	8.Ø	R-EDAC-DATA-1•11Ø
WE14	I	8.Ø	R-EDAC-DATA-2•11Ø
WE15	I	8.Ø	R-EDAC-DATA-3•11Ø
WE16	I	8.Ø	R-EDAC-DATA-4•11Ø
WE17	I	9.Ø	R-EDAC-DATA-5•11Ø
WE18	I	9.Ø	R-EDAC-DATA-6•11Ø
WE19	I	9.Ø	R-EDAC-DATA-7•11Ø
WE2Ø	I	9.Ø	P-EDAC-DATA-P•1ØØ
WE21	I	22.Ø	$PARTIAL-CLR•Ø11
WFØ3	I	3Ø.Ø	DEV-5Ø1•12Ø
WFØ6	I	16.Ø	SEQ-ERR•12Ø
WFØ7	I	16.Ø	STAT-ERR•11Ø
WF12	I	25.Ø	FIPC-RESET•Ø1Ø
WGØØ	O	6.Ø	DMPADR-15•1ØØ
WGØ2	O	6.Ø	DMPADR-14•1ØØ
WGØ3	O	6.Ø	DMPADR-13•1ØØ
WGØ4	O	6.Ø	DMPADR-12•1ØØ
WGØ5	O	6.Ø	DMPADR-11•1ØØ
WGØ6	O	27.Ø	DMPDTA-Ø•1ØØ
WGØ7	O	27.Ø	DMPDTA-1•1ØØ
WGØ8	O	27.Ø	DMPDTA-2•1ØØ
WGØ9	O	27.Ø	DMPDTA-3•1ØØ
WG1Ø	O	27.Ø	DMPDTA-4•1ØØ
WG12	O	27.Ø	DMPDTA-5•1ØØ
WG13	O	27.Ø	DMPDTA-6•1ØØ
WG14	O	27.Ø	DMPDTA-7•1ØØ
WG15	O	27.Ø	DMPDTA-P•1ØØ
WG16	O	27.Ø	MPWR•13Ø
WG17	O	1Ø.Ø	DMPADR-P•1ØØ
WG18	O	31.Ø	CYHD-FULL•Ø1Ø
WG19	O	27.Ø	MPRD•12Ø
WG2Ø	I	29.Ø	FMP-ADDR-ERR•Ø1Ø
WHØØ	I	3Ø.Ø	DREG-Ø•11Ø
WHØ1	I	3Ø.Ø	DREG-1•11Ø
WHØ2	I	3Ø.Ø	DREG-2•11Ø
WHØ3	I	3Ø.Ø	DREG-3•11Ø
WHØ4	I	3Ø.Ø	DREG-4•11Ø
WHØ5	I	3Ø.Ø	DREG-5•11Ø
WHØ6	I	3Ø.Ø	DREG-6•11Ø
WHØ7	I	3Ø.Ø	DREG-7•11Ø
WHØ8	I	16.Ø	F-EDAC-ERROR•11Ø
WH1Ø	O	3Ø.Ø	DEFECT-SKP•12Ø
WH18	O	31.Ø	DEF-WHEX•Ø3Ø
WH19	O	31.Ø	DEF-WDSN•Ø3Ø
WJØØ	I	29.Ø	IFØ-ON-LINE•ØØØ
WJØ1	I	29.Ø	IF1-ON-LINE•ØØØ
WJØ2	I	16.Ø	SWITCH-RESET•ØØØ
WJØ4	I	23.Ø	POWER-CONF•1ØØ
WJØ6	O	3Ø.Ø	DAU-TROUBLE•ØØØ
WJØ7	I	3Ø.Ø	SEQ-STATE-6•11Ø
WJØ8	I	3Ø.Ø	SEQ-STATE-7•11Ø
WJØ9	O	29.Ø	DAU-ON-LINE•1ØØ
WJ1Ø	O	3Ø.Ø	DOUBLE-DEF•12Ø

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TITLE LOGIC DIAGRAM- WDAMP
I/O PIN -
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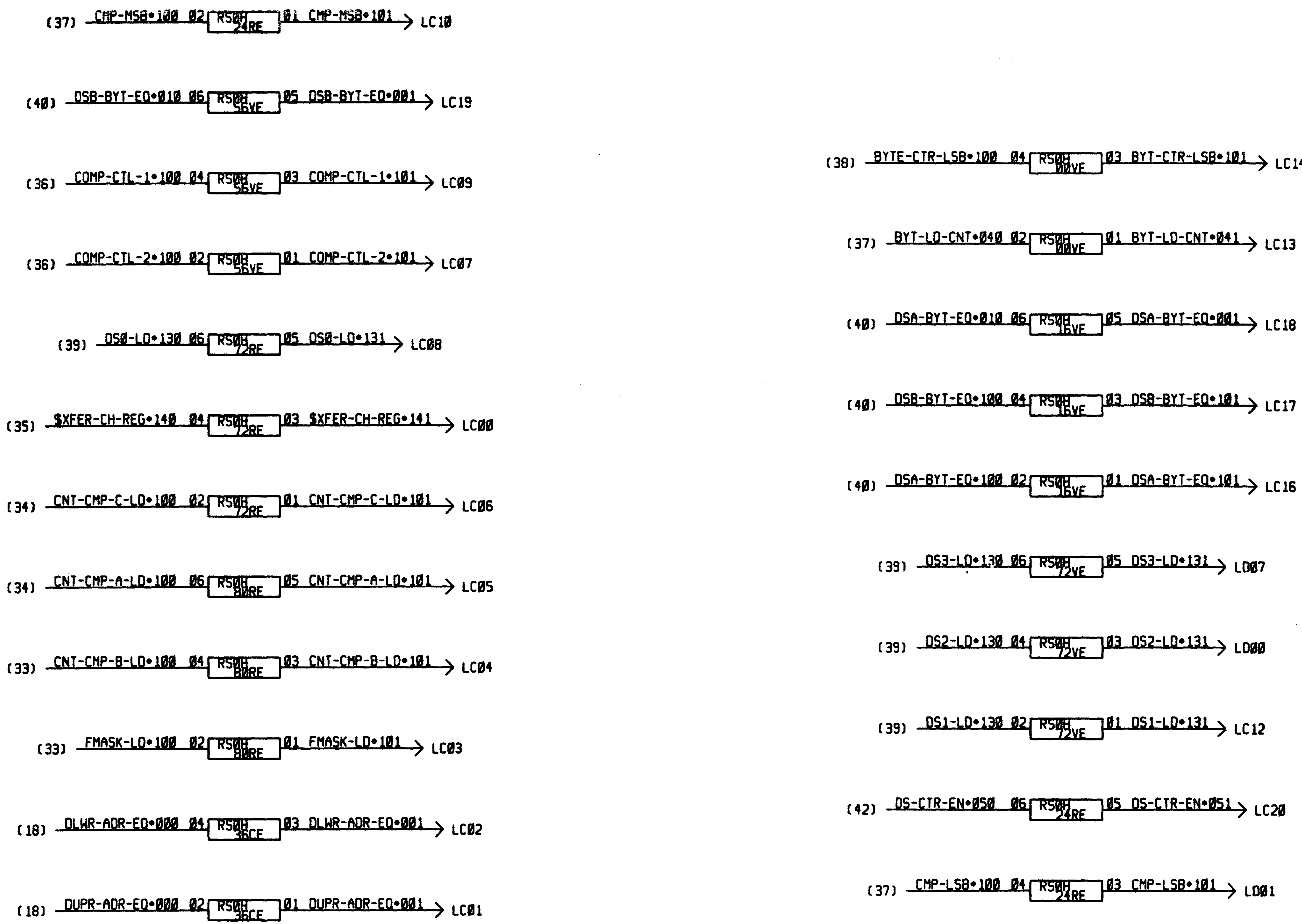
SIZE	DWG NO	SH	REV
B	58Ø75894	3.Ø	C

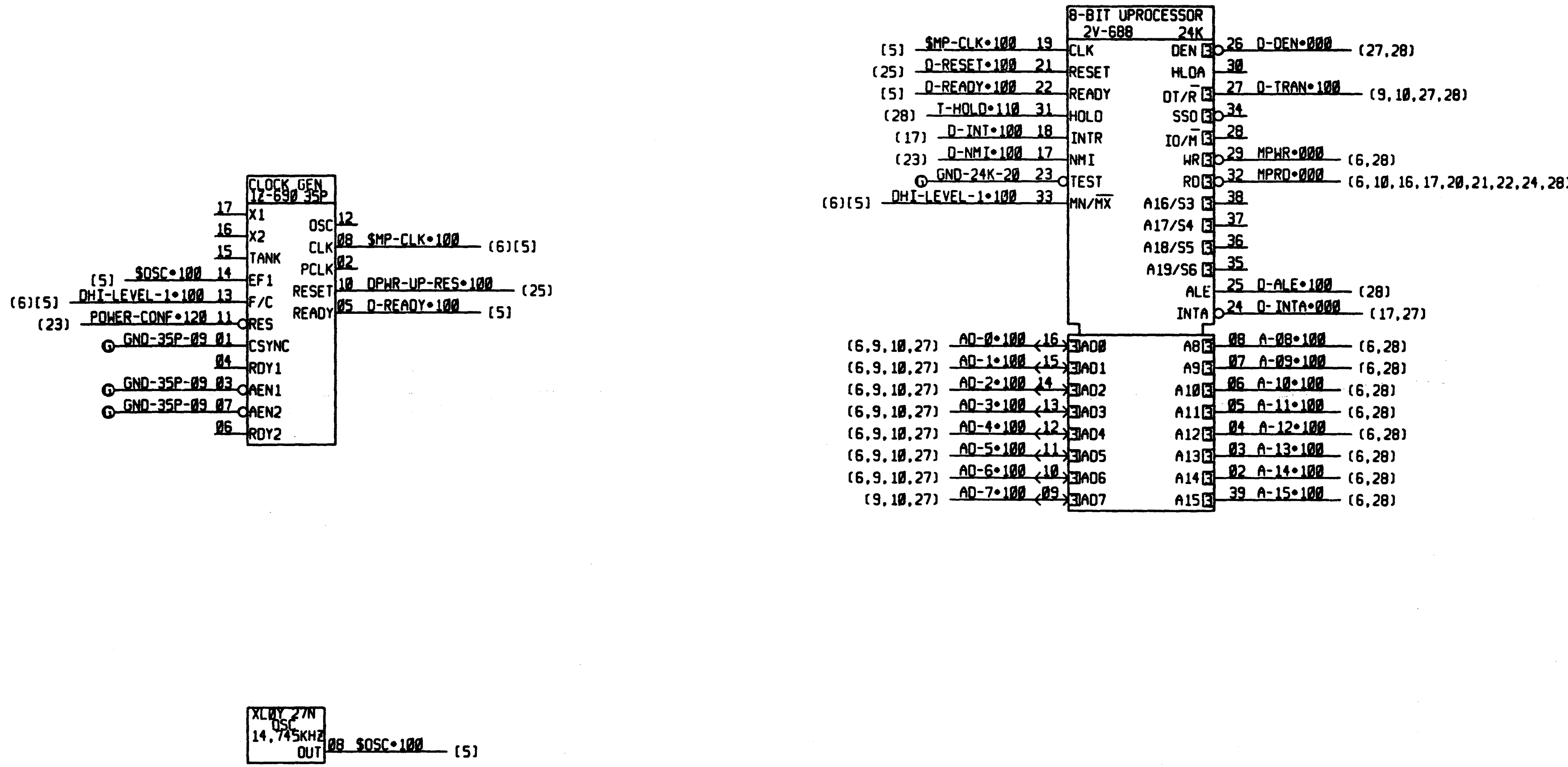
58Ø75894

I/O PIN		PAGE	SIGNAL NAME
WJ12	I	30.Ø	CSYN-CNT-Ø•11Ø
WJ13	I	30.Ø	CSYN-CNT-1•11Ø
WJ14	I	30.Ø	CSYN-CNT-2•11Ø
WJ15	I	30.Ø	CSYN-CNT-3•11Ø
WJ16	I	30.Ø	CSYN-CNT-4•11Ø
WJ17	I	30.Ø	CSYN-CNT-5•11Ø
WJ18	I	30.Ø	CSYN-CNT-6•11Ø
WJ19	I	30.Ø	CSYN-CNT-7•11Ø
WJ2Ø	O	23.Ø	POMC•Ø1Ø
WKØØ	I	30.Ø	DEV-4XX•11Ø
WKØ1	I	30.Ø	FSEQ-EXEC•11Ø
WKØ2	I	30.Ø	OP35-SEOC•Ø1Ø
WKØ3	I	30.Ø	OP45-RDDS•Ø1Ø
WKØ4	I	30.Ø	OP22-LCSN•Ø1Ø
WKØ5	I	30.Ø	OP5Ø-66•Ø1Ø
WKØ6	I	30.Ø	OP41-42•12Ø
WKØ7	I	30.Ø	OP63-72•Ø2Ø
WKØ8	O	31.Ø	DS-Ø-B1•11Ø
WKØ9	O	31.Ø	DS-Ø-B2•11Ø
WK1Ø	O	31.Ø	DS-Ø-B3•11Ø
WK12	O	31.Ø	DS-2-B1•11Ø
WK13	O	31.Ø	DS-2-B2•11Ø
WK14	O	31.Ø	DS-2-B3•11Ø
WK15	O	31.Ø	BYTE-CTR-ONES•11Ø
WK16	O	31.Ø	DEF-SKP-INH•11Ø
WK17	O	31.Ø	DEF-SYNC-ERR•Ø1Ø
WK2Ø	O	31.Ø	COMPARE•12Ø



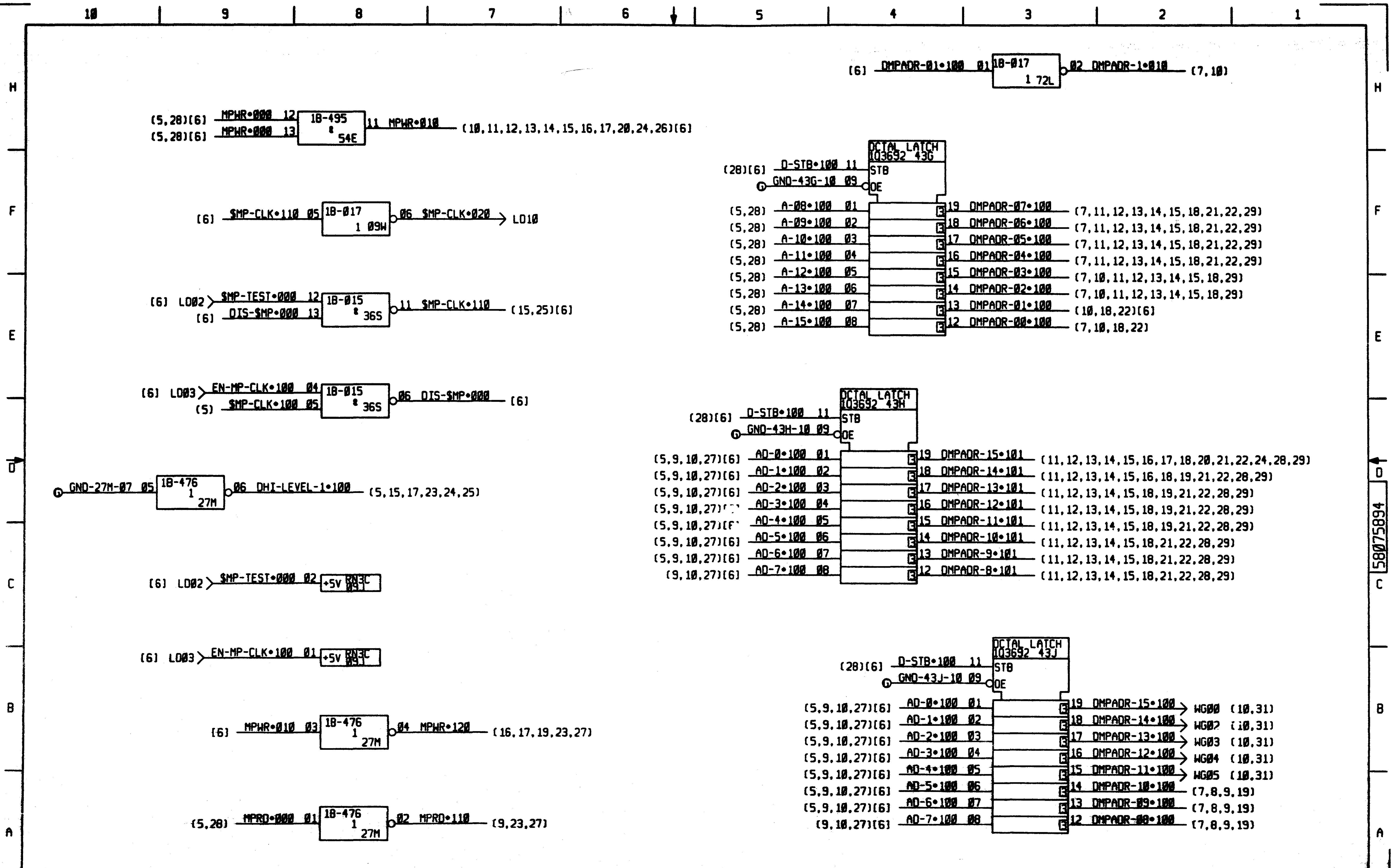
58075894

LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 4.0	REV C



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 5.0	REV C

58075894



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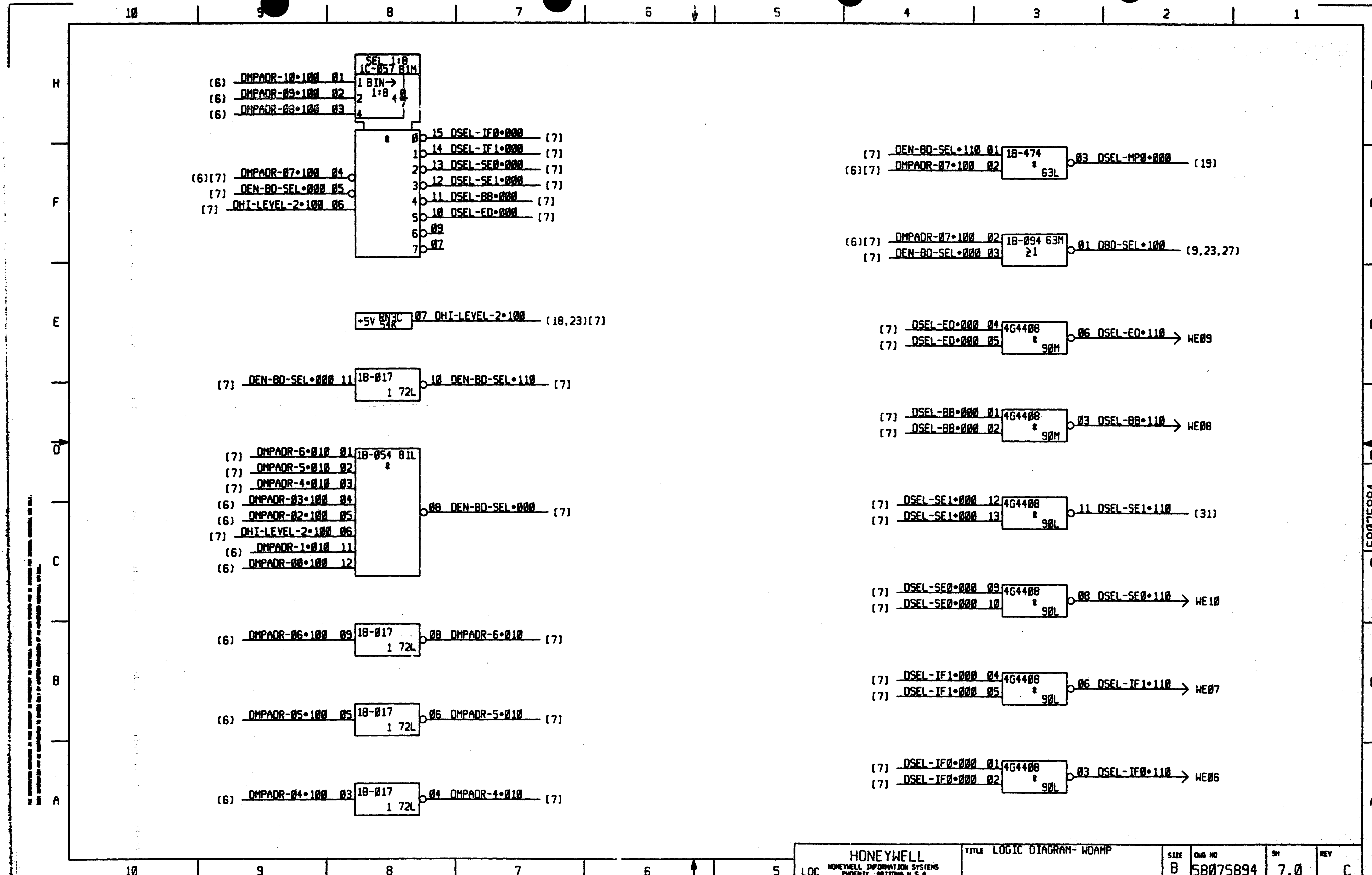
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC

TITLE LOGIC DIAGRAM- WDAMP

SIZE	DWG NO	SH	REV
B	58075894	6.0	C



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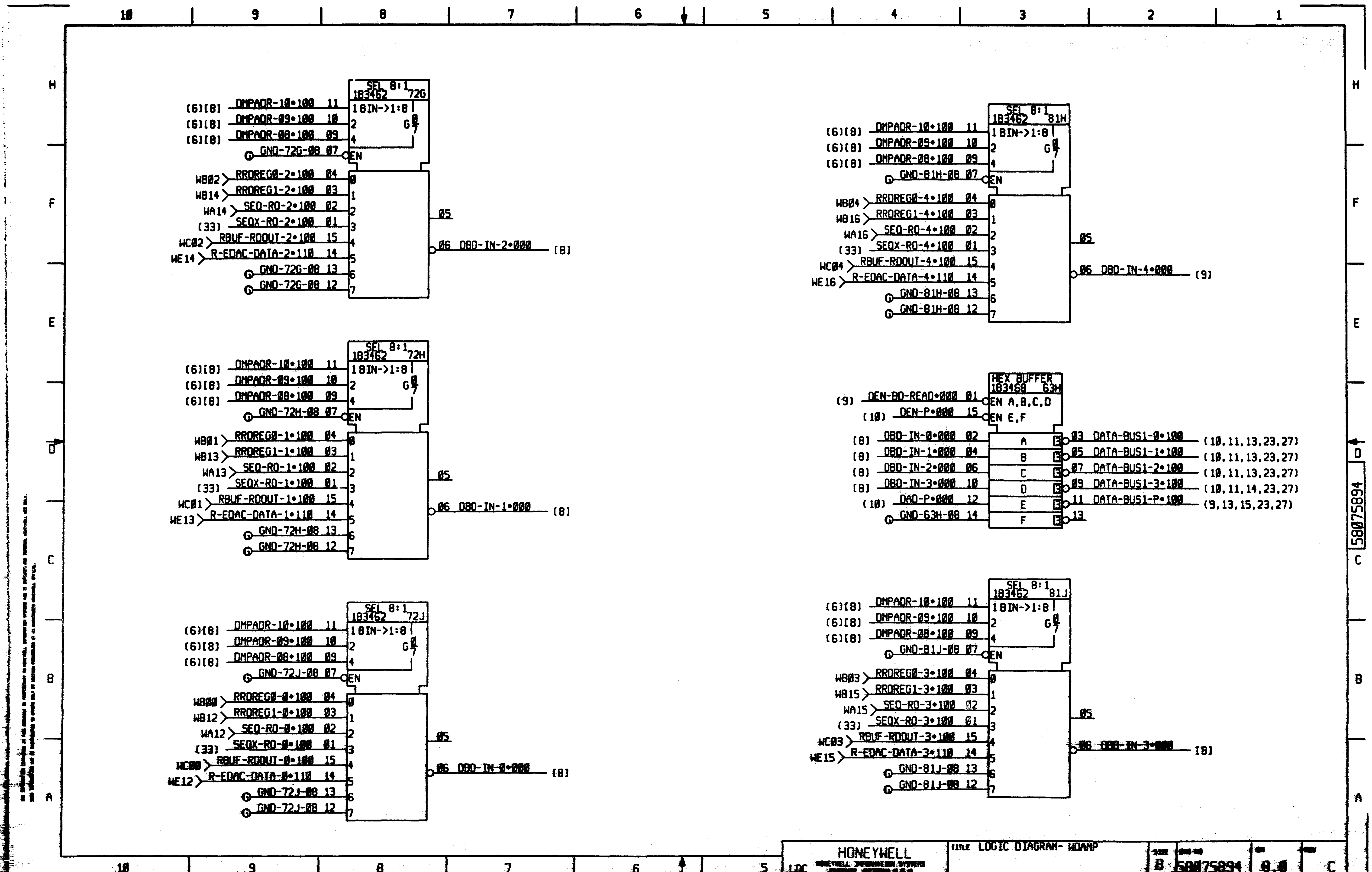
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE	SIZE	DWG NO	SH	REV
LOGIC DIAGRAM- WDAMP	B	58Ø75894	7.Ø	C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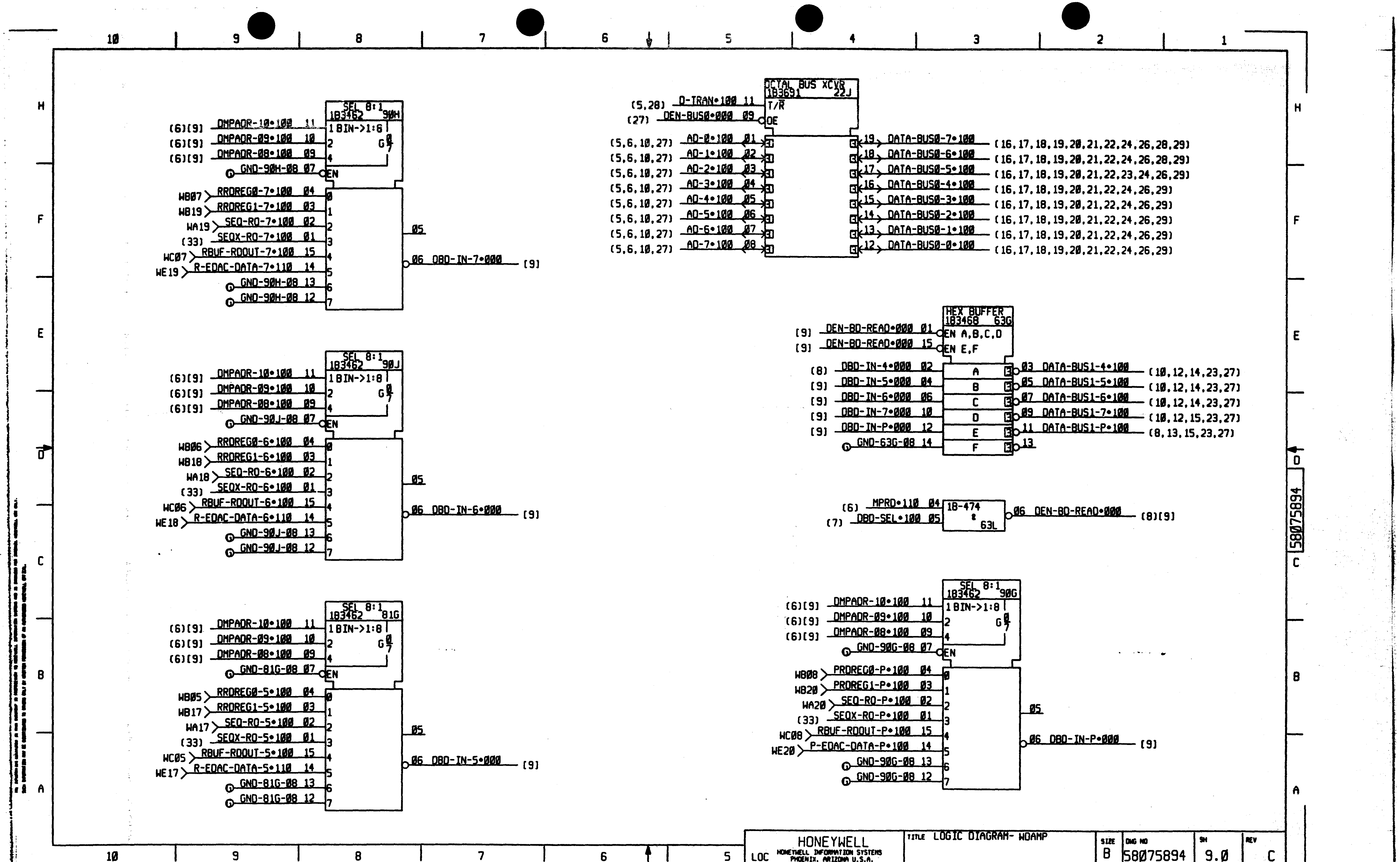
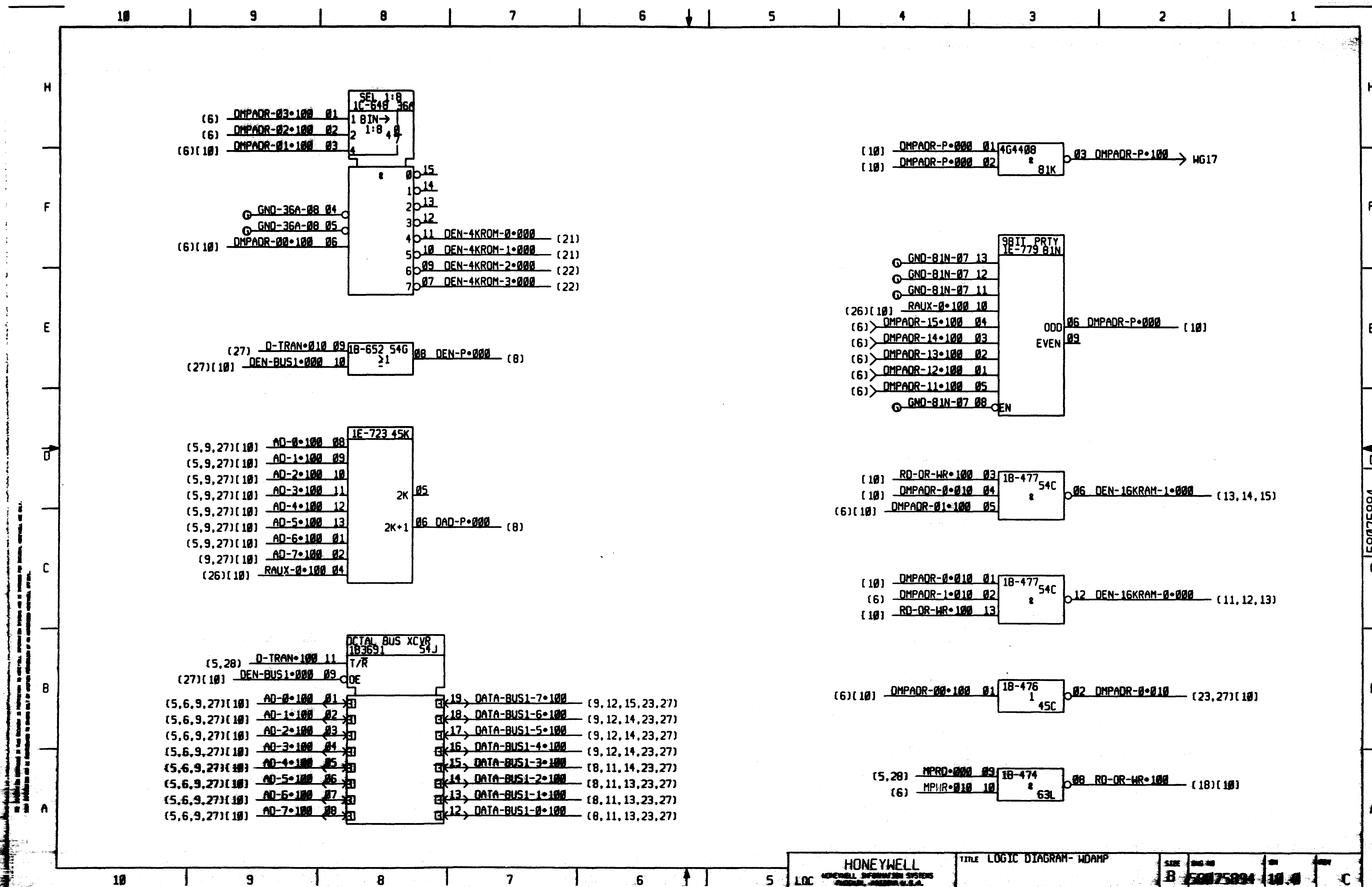
DMPADR-10•100 11
DMPADR-09•100 10
DMPADR-08•100 09
GND-72G-08 07
RRDREG0-2•100 04
RRDREG1-2•100 03
SEQ-RO-2•100 02
SEQX-RO-2•100 01
RBUF-RDOUT-2•100 15
R-EDAC-DATA-2•110 14
GND-72G-08 13
GND-72G-08 12
05
06 DBD-IN-2•000 (8)
SEL 8:1
1B3462 72H
DMPADR-10•100 11
DMPADR-09•100 10
DMPADR-08•100 09
GND-72H-08 07
RRDREG0-1•100 04
RRDREG1-1•100 03
SEQ-RO-1•100 02
SEQX-RO-1•100 01
RBUF-RDOUT-1•100 15
R-EDAC-DATA-1•110 14
GND-72H-08 13
GND-72H-08 12
05
06 DBD-IN-1•000 (8)
SEL 8:1
1B3462 72J
DMPADR-10•100 11
DMPADR-09•100 10
DMPADR-08•100 09
GND-72J-08 07
RRDREG0-0•100 04
RRDREG1-0•100 03
SEQ-RO-0•100 02
SEQX-RO-0•100 01
RBUF-RDOUT-0•100 15
R-EDAC-DATA-0•110 14
GND-72J-08 13
GND-72J-08 12
05
06 DBD-IN-0•000 (8)
SEL 8:1
1B3462 81H
DMPADR-10•100 11
DMPADR-09•100 10
DMPADR-08•100 09
GND-81H-08 07
RRDREG0-4•100 04
RRDREG1-4•100 03
SEQ-RO-4•100 02
SEQX-RO-4•100 01
RBUF-RDOUT-4•100 15
R-EDAC-DATA-4•110 14
GND-81H-08 13
GND-81H-08 12
05
06 DBD-IN-4•000 (9)
HEX BUFFER
1B3468 63H
(9) DEN-BD-READ•000 01 EN A,B,C,D
(10) DEN-P•000 15 EN E,F
(8) DBD-IN-0•000 02 A 03 DATA-BUS1-0•100 (10,11,13,23,27)
(8) DBD-IN-1•000 04 B 05 DATA-BUS1-1•100 (10,11,13,23,27)
(8) DBD-IN-2•000 06 C 07 DATA-BUS1-2•100 (10,11,13,23,27)
(8) DBD-IN-3•000 10 D 09 DATA-BUS1-3•100 (10,11,14,23,27)
(10) DAD-P•000 12 E 11 DATA-BUS1-P•100 (9,13,15,23,27)
GND-63H-08 14 F 13
SEL 8:1
1B3462 81J
DMPADR-10•100 11
DMPADR-09•100 10
DMPADR-08•100 09
GND-81J-08 07
RRDREG0-3•100 04
RRDREG1-3•100 03
SEQ-RO-3•100 02
SEQX-RO-3•100 01
RBUF-RDOUT-3•100 15
R-EDAC-DATA-3•110 14
GND-81J-08 13
GND-81J-08 12
05
06 DBD-IN-3•000 (8)
58075894
HONEYWELL
LDC
TITLE LOGIC DIAGRAM- WDAMP
B 58075894 0.0 C



HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC

TITLE LOGIC DIAGRAM- WDAMP

SIZE	DWG NO	SH	REV
B	58075894	9.0	C



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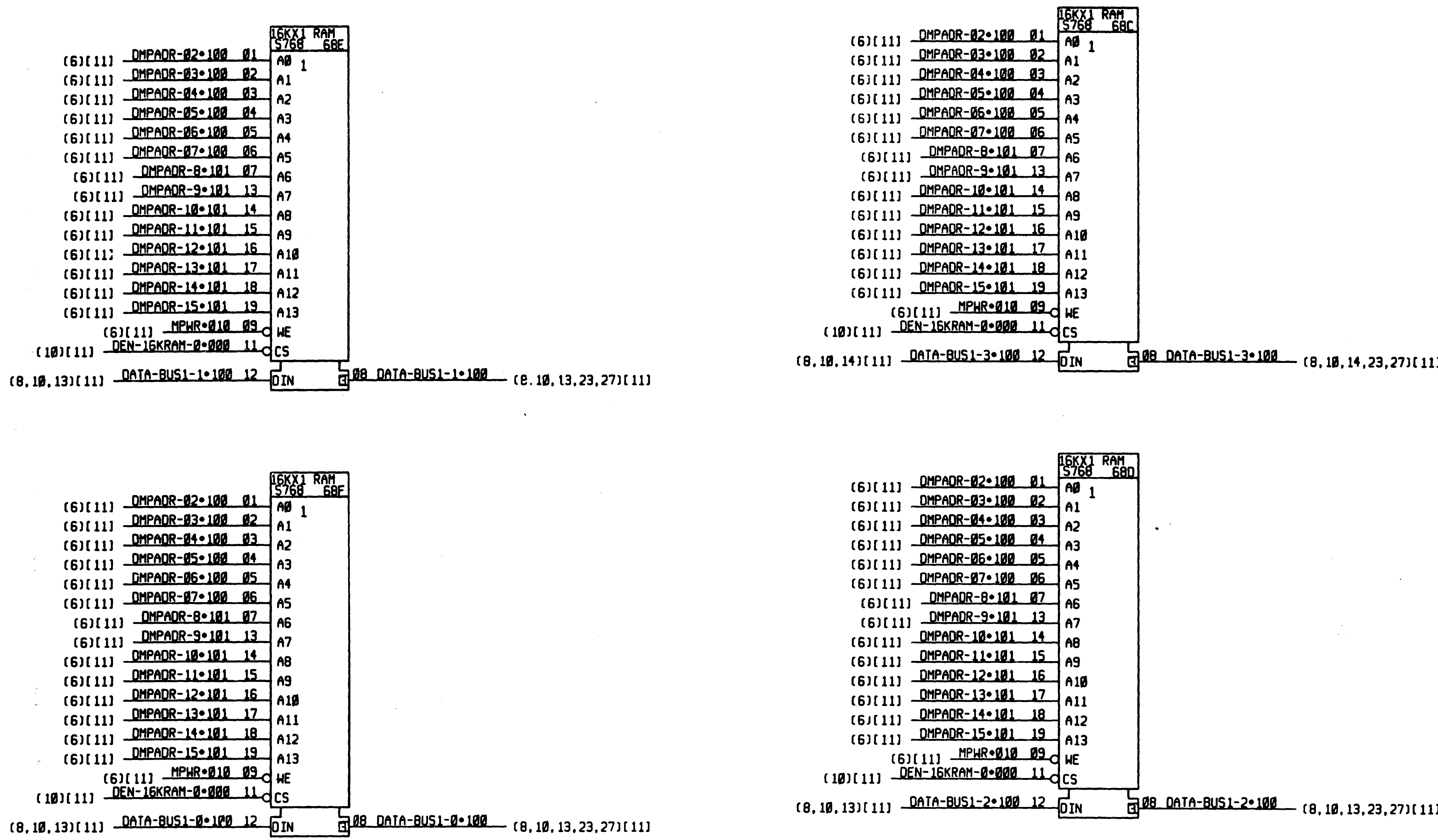
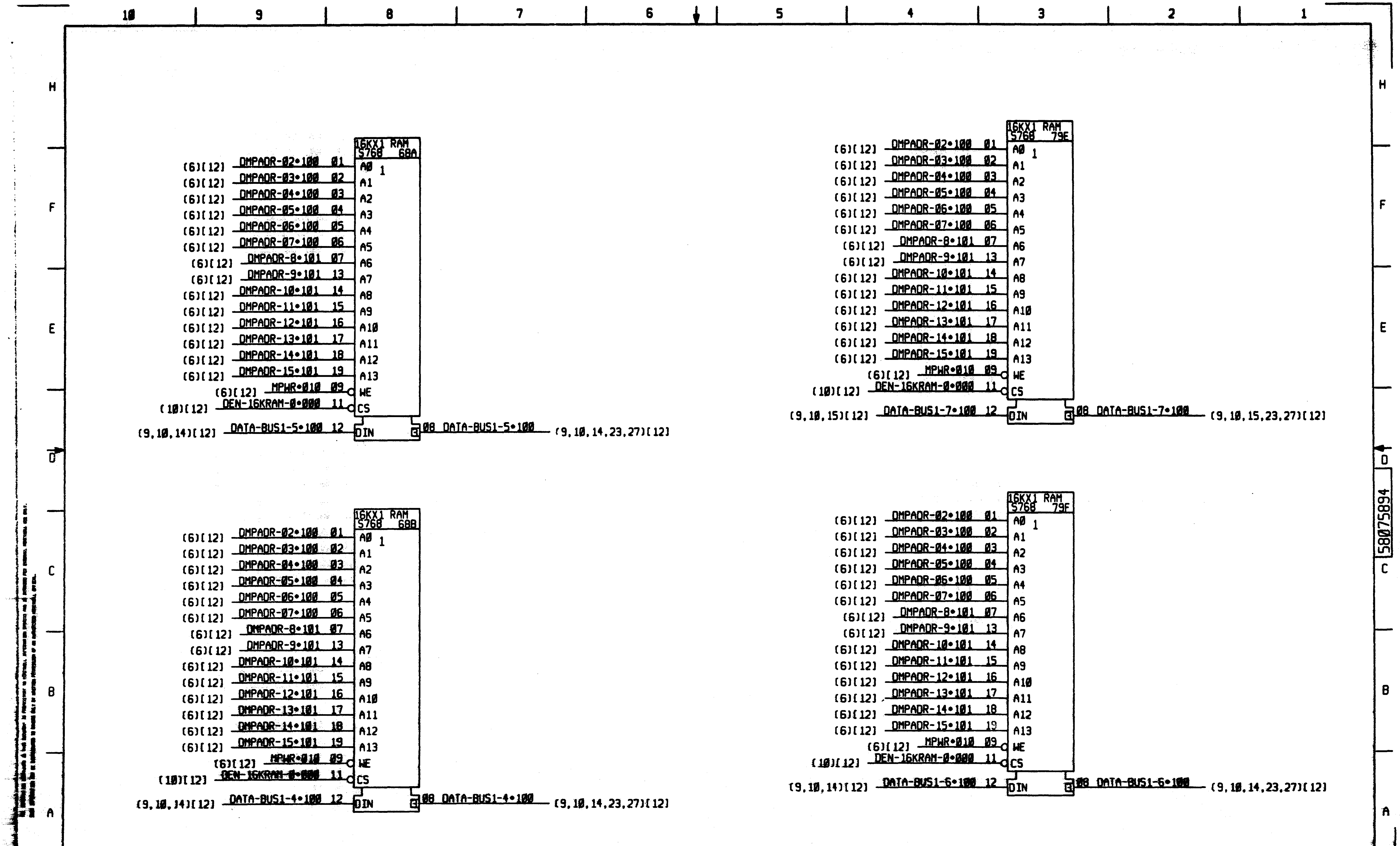
DMPADR-02•100
DMPADR-01•100
GND-36A-08
DMPADR-00•100
DEN-4KROM-0•000
DEN-4KROM-1•000
DEN-4KROM-2•000
DEN-4KROM-3•000
1B-652 54G
D-TRAN•010
DEN-BUS1•000
DEN-P•000
1E-723 45K
AD-0•100
AD-1•100
AD-2•100
AD-3•100
AD-4•100
AD-5•100
AD-6•100
AD-7•100
RAUX-0•100
DAD-P•000
OCTAL BUS XCVR
1B3691 54J
D-TRAN•100
DATA-BUS1-7•100
DATA-BUS1-6•100
DATA-BUS1-5•100
DATA-BUS1-4•100
DATA-BUS1-3•100
DATA-BUS1-2•100
DATA-BUS1-1•100
DATA-BUS1-0•100
4G4408 81K
DMPADR-P•000
DMPADR-P•100
WG17
9BIT PRTY
1E-779 81N
GND-81N-07
DMPADR-15•100
DMPADR-14•100
DMPADR-13•100
DMPADR-12•100
DMPADR-11•100
ODD
EVEN
1B-477 54C
RD-OR-WR•100
DMPADR-0•010
DMPADR-01•100
DEN-16KRAM-1•000
DMPADR-1•010
DEN-16KRAM-0•000
1B-476 45C
DMPADR-00•100
1B-474 63L
MPRD•000
MPWR•010
HONEYWELL
LOGIC DIAGRAM- WDAMP
58075894

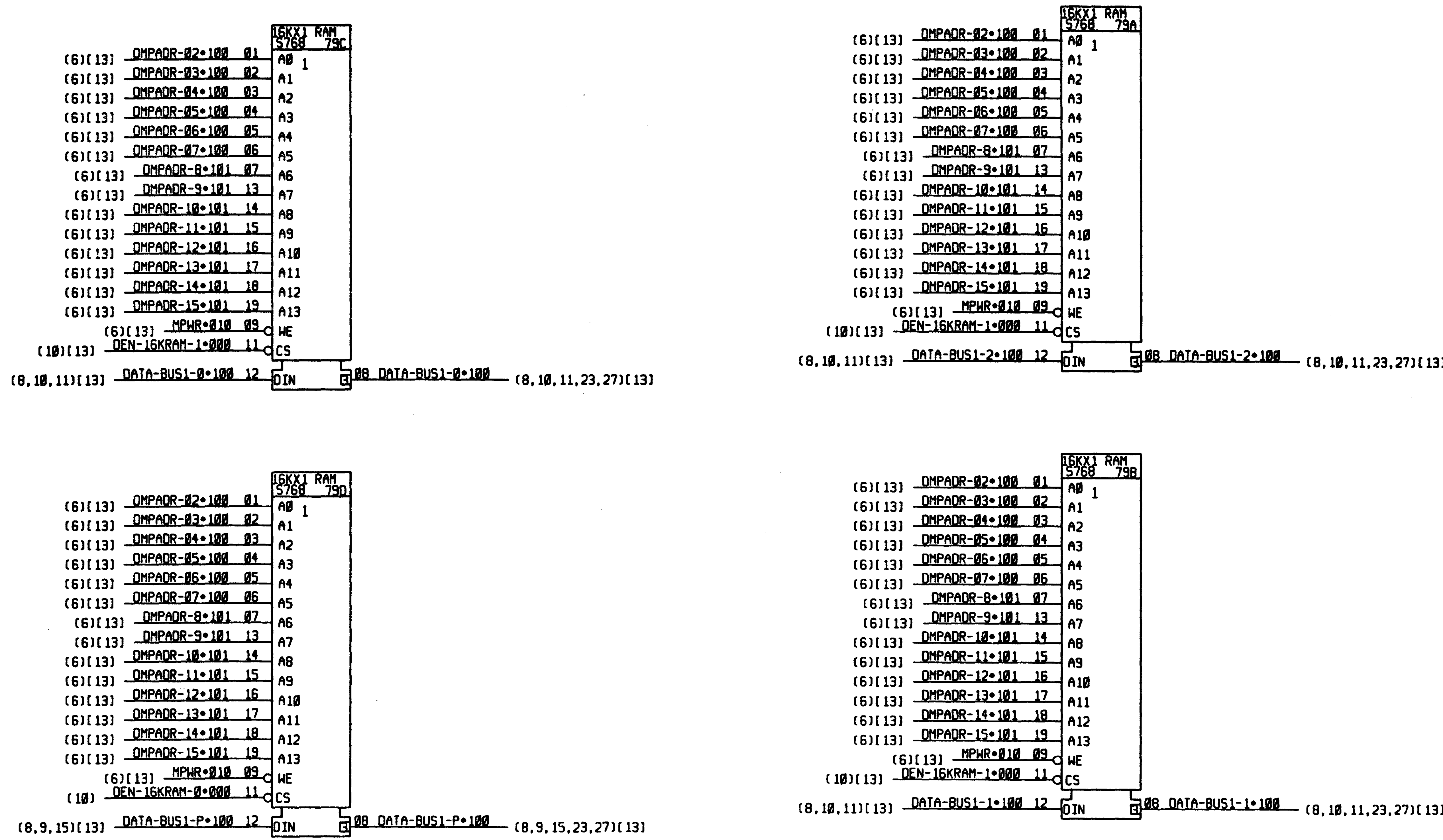


HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- WDAMP
SIZE B | DWG NO 58075894 | SH 11.0 | REV C

58075894



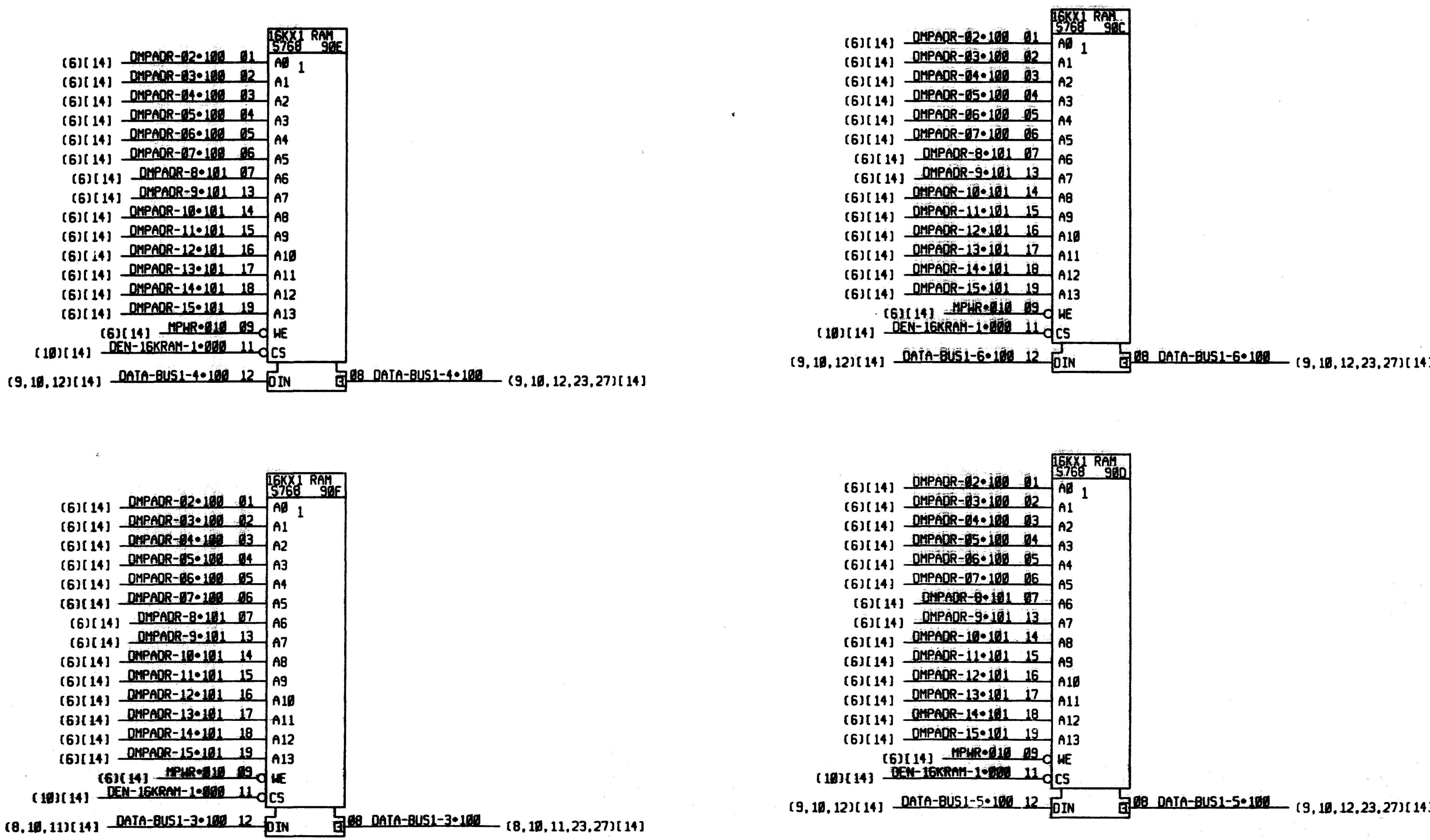
LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 12.0	REV C



HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC

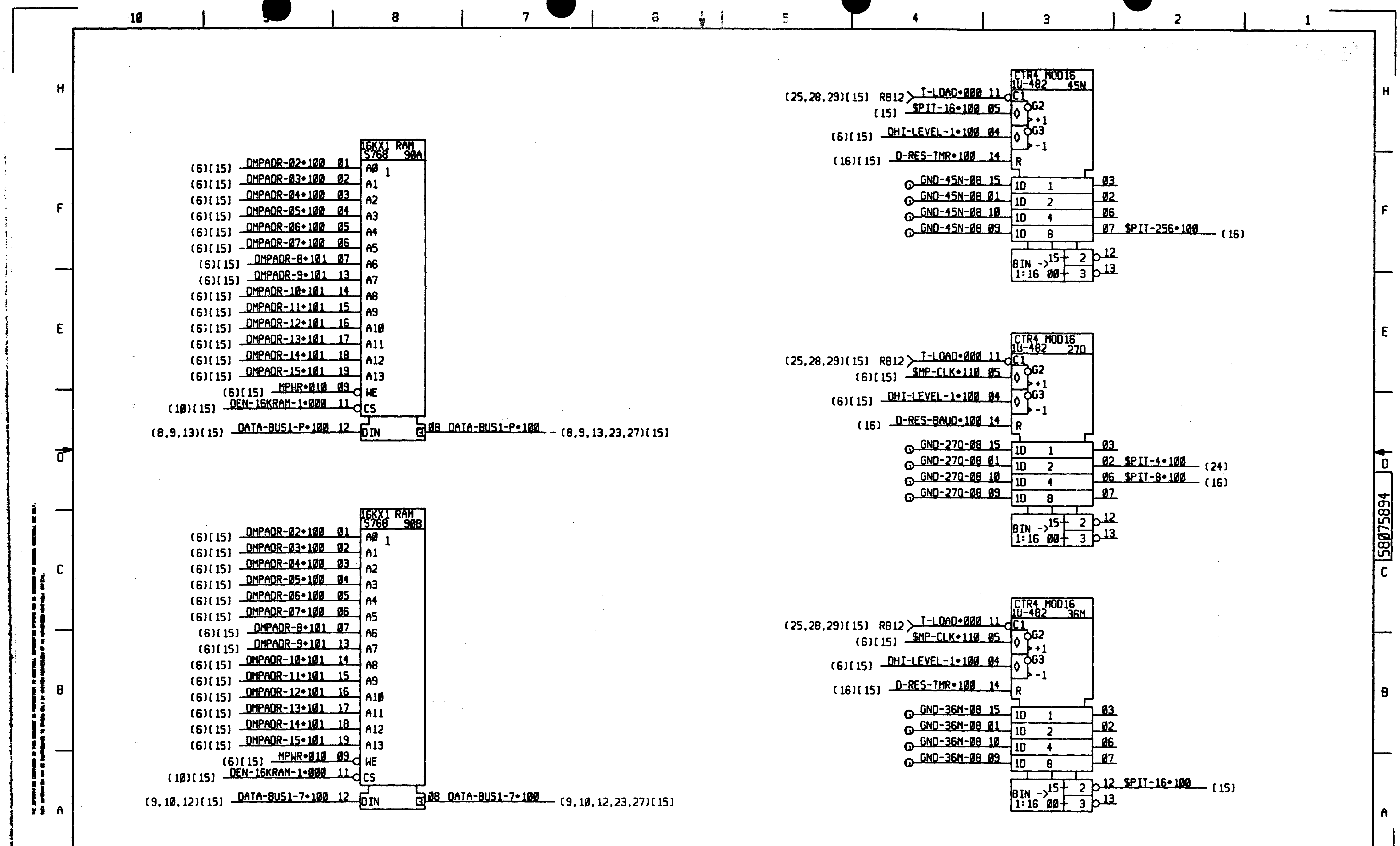
TITLE LOGIC DIAGRAM- WDAMP

SIZE	DWG NO	SH	REV
B	58075894	13.0	C



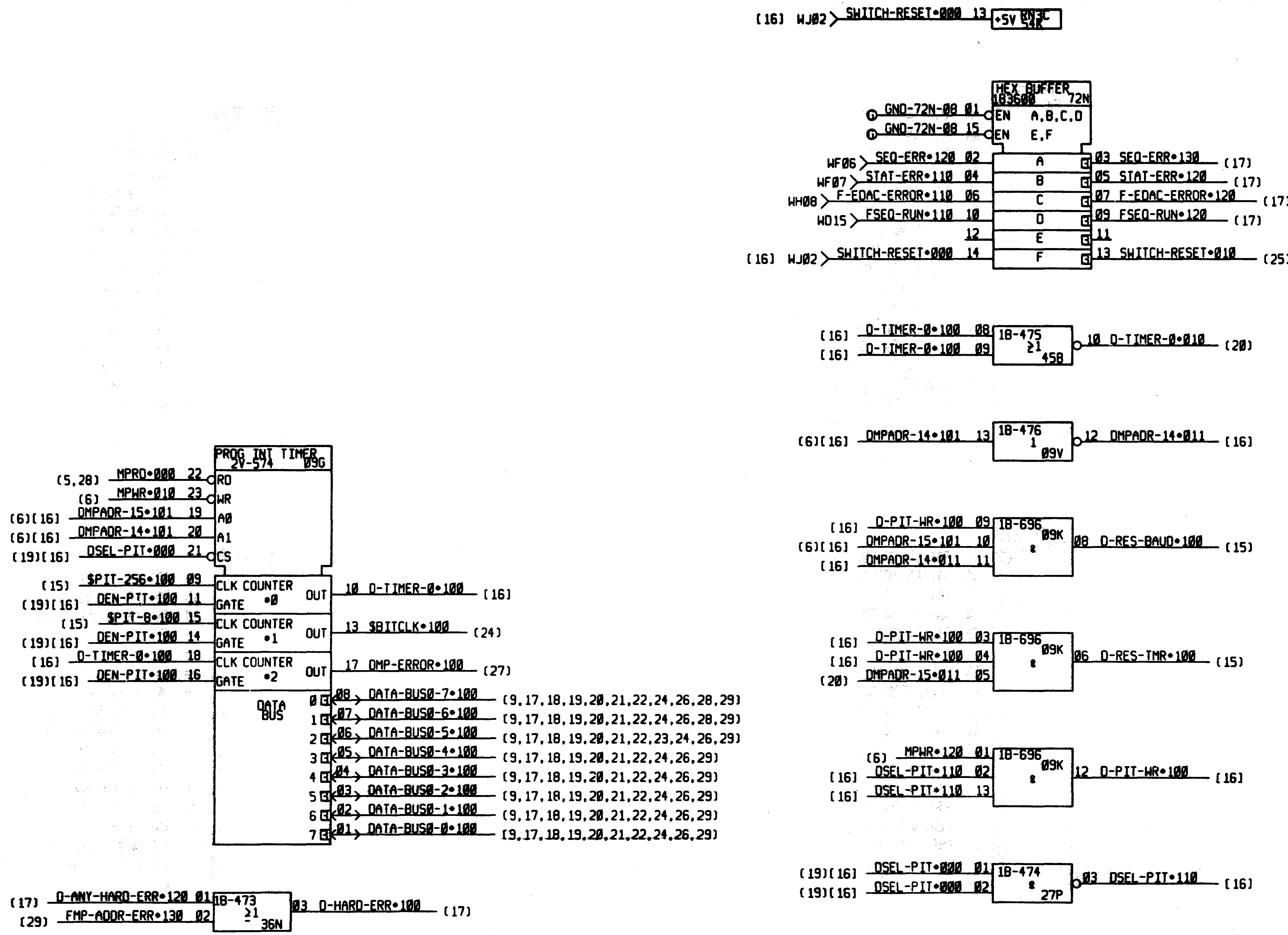
58Ø75894

LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58Ø75894	SH 14.Ø	REV C



HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC

TITLE	SIZE	DWG NO	SH	REV
LOGIC DIAGRAM- WDAMP	B	58075894	15.0	C

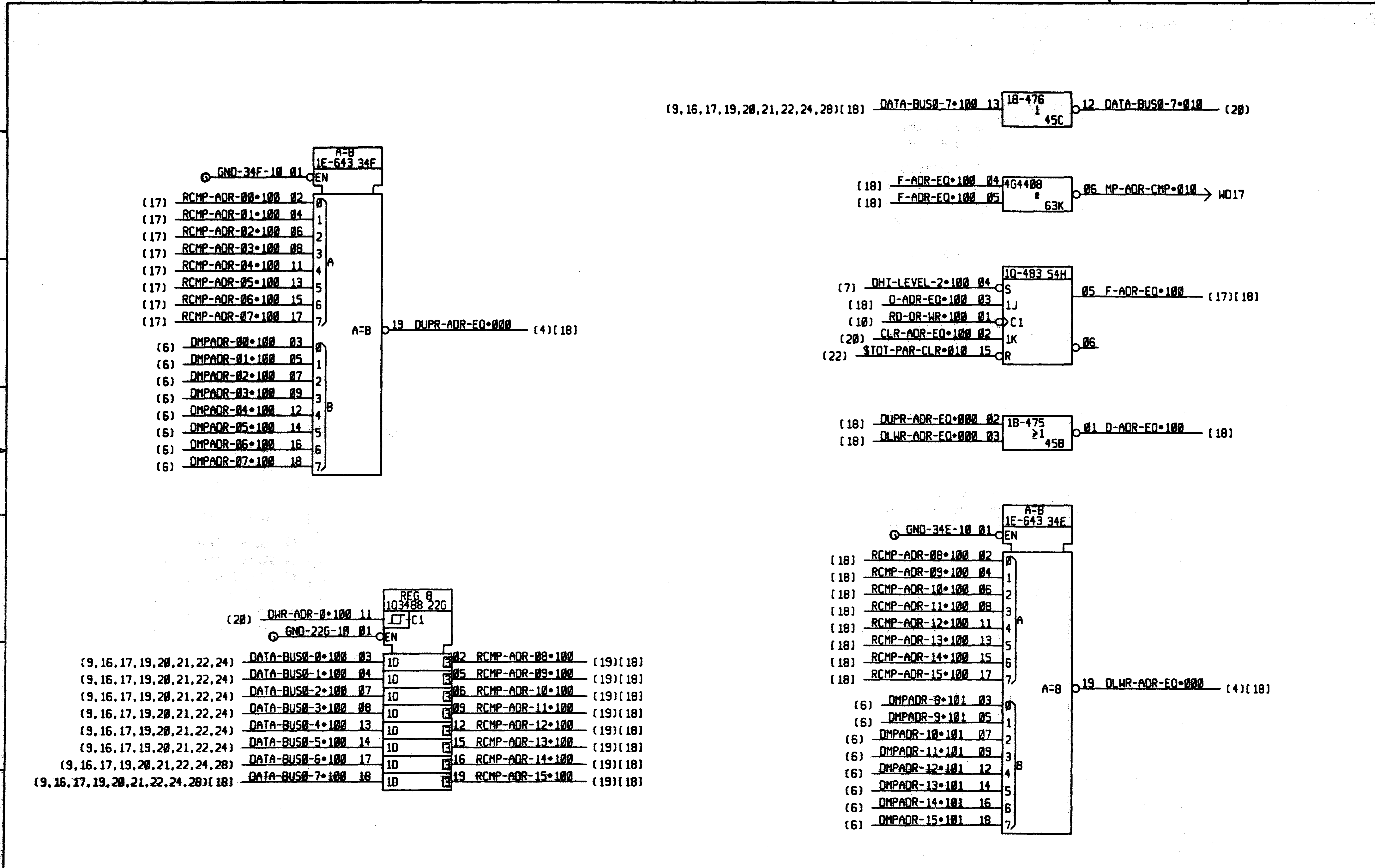


LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 16.0	REV C

58075894

58075894

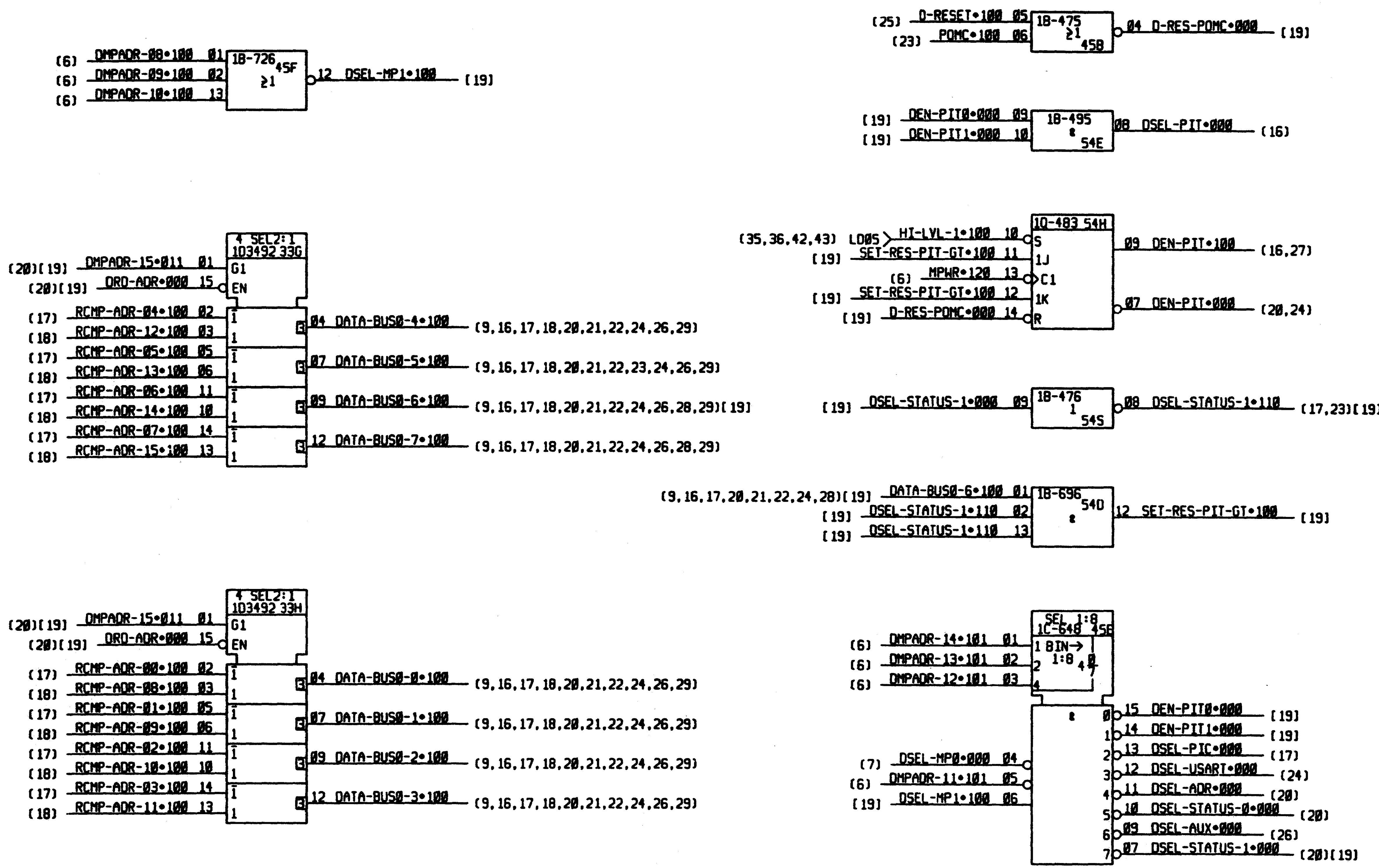
LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 17.0	REV C



HONEYWELL
LGC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAMP

SIZE	DWG NO	SH	REV
B	58075894	18.0	C

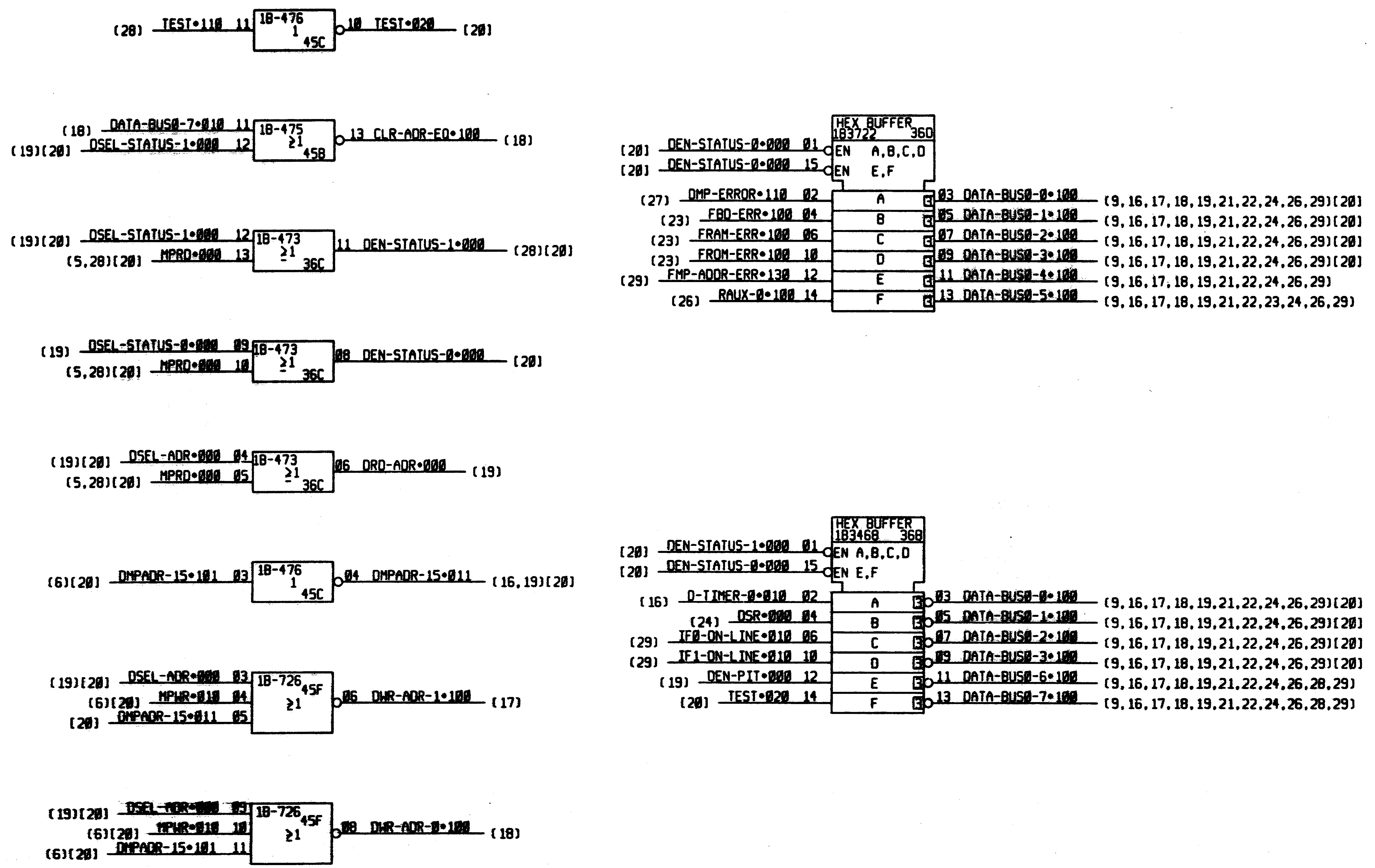


58075894

HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC

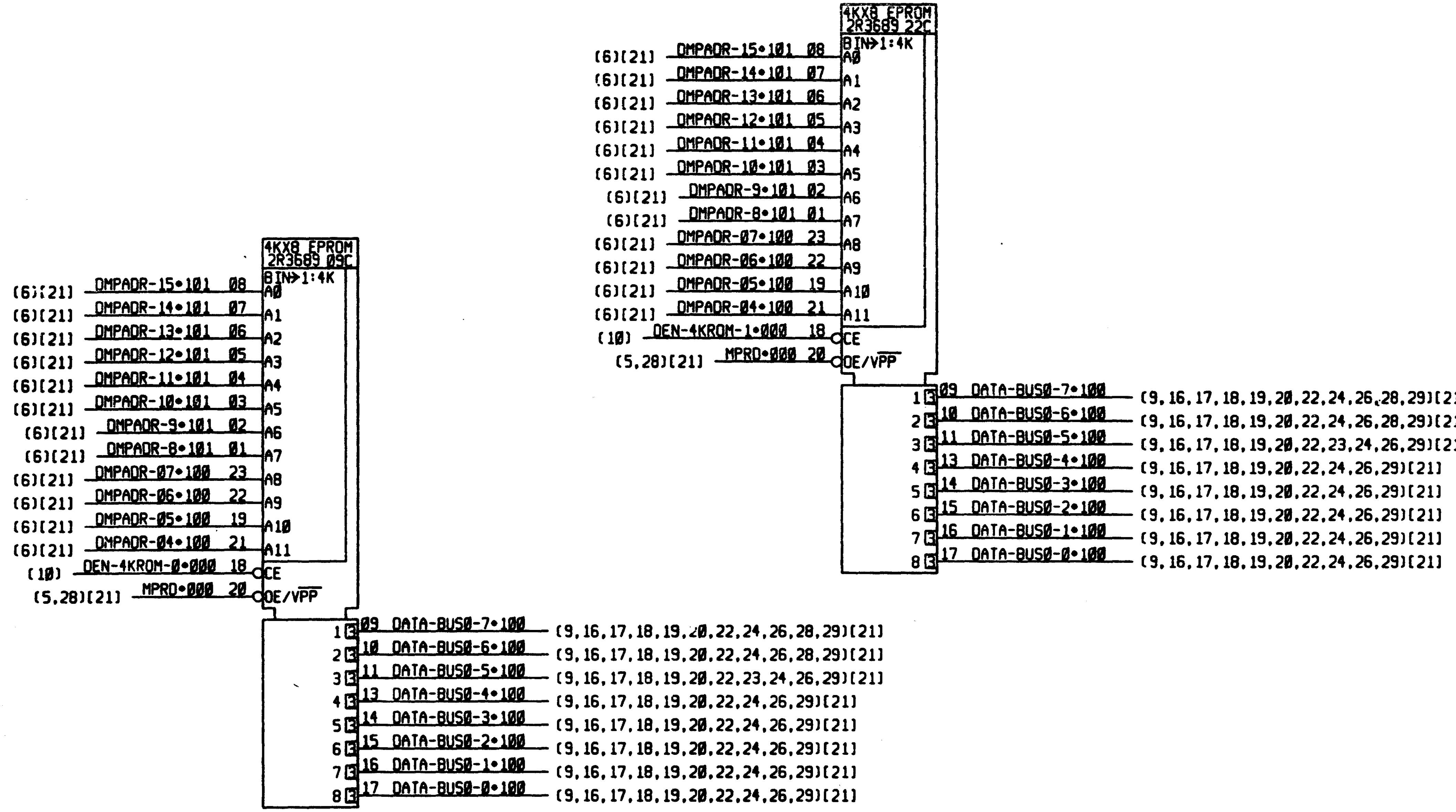
TITLE LOGIC DIAGRAM- WDAMP

SIZE	DWG NO	SH	REV
B	58075894	19.0	C



58075894

LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 20.0	REV C



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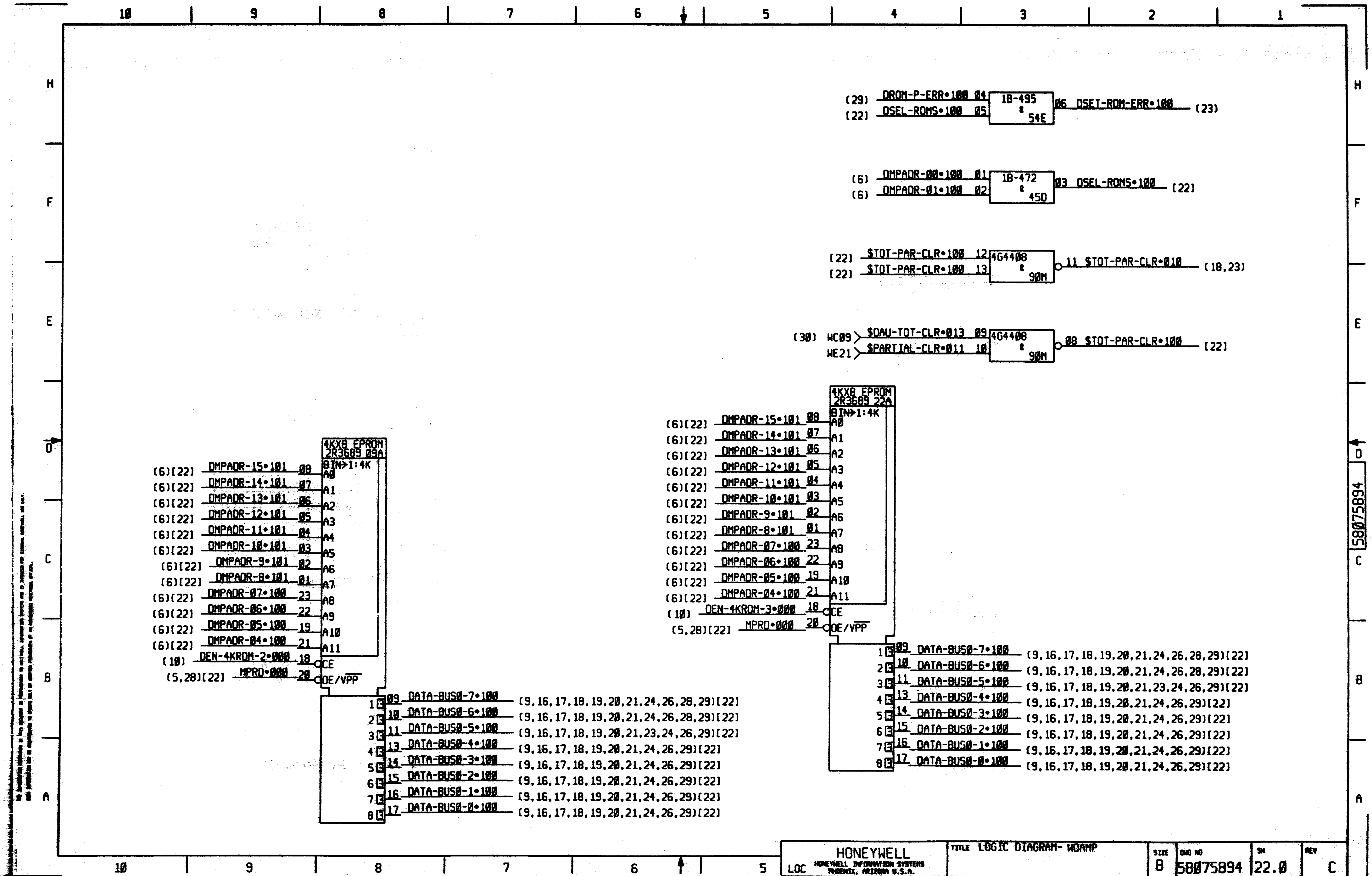
LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 21.0	REV C



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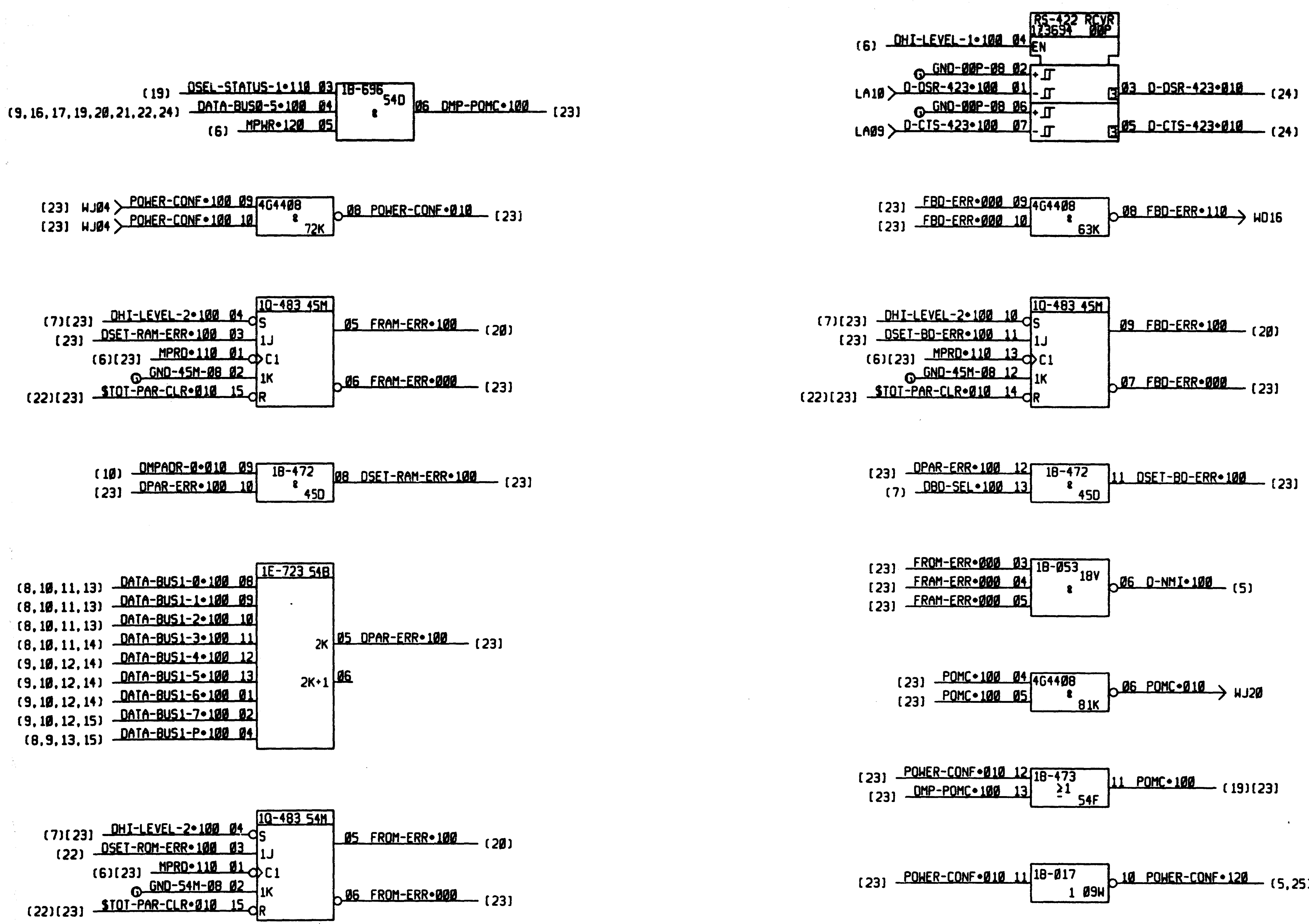
H F E D C B A
(29) DROM-P-ERR•100 04
(22) DSEL-ROMS•100 05
18-495
54E
06 DSET-ROM-ERR•100 (23)
(6) DMPADR-00•100 01
(6) DMPADR-01•100 02
18-472
450
03 DSEL-ROMS•100 (22)
(22) $TOT-PAR-CLR•100 12
(22) $TOT-PAR-CLR•100 13
4G4408
90M
11 $TOT-PAR-CLR•010 (18,23)
(30) WC09 $DAU-TOT-CLR•013 09
WE21 $PARTIAL-CLR•011 10
4G4408
90M
08 $TOT-PAR-CLR•100 (22)
4KX8 EPROM
2R3689 09A
BIN→1:4K
(6)(22) DMPADR-15•101 08 A0
(6)(22) DMPADR-14•101 07 A1
(6)(22) DMPADR-13•101 06 A2
(6)(22) DMPADR-12•101 05 A3
(6)(22) DMPADR-11•101 04 A4
(6)(22) DMPADR-10•101 03 A5
(6)(22) DMPADR-9•101 02 A6
(6)(22) DMPADR-8•101 01 A7
(6)(22) DMPADR-07•100 23 A8
(6)(22) DMPADR-06•100 22 A9
(6)(22) DMPADR-05•100 19 A10
(6)(22) DMPADR-04•100 21 A11
(10) DEN-4KROM-2•000 18 CE
(5,28)(22) MPRD•000 20 OE/VPP
1 09 DATA-BUS0-7•100 (9,16,17,18,19,20,21,24,26,28,29)(22)
2 10 DATA-BUS0-6•100 (9,16,17,18,19,20,21,24,26,28,29)(22)
3 11 DATA-BUS0-5•100 (9,16,17,18,19,20,21,23,24,26,29)(22)
4 13 DATA-BUS0-4•100 (9,16,17,18,19,20,21,24,26,29)(22)
5 14 DATA-BUS0-3•100 (9,16,17,18,19,20,21,24,26,29)(22)
6 15 DATA-BUS0-2•100 (9,16,17,18,19,20,21,24,26,29)(22)
7 16 DATA-BUS0-1•100 (9,16,17,18,19,20,21,24,26,29)(22)
8 17 DATA-BUS0-0•100 (9,16,17,18,19,20,21,24,26,29)(22)
4KX8 EPROM
2R3689 22A
BIN→1:4K
(6)(22) DMPADR-15•101 08 A0
(6)(22) DMPADR-14•101 07 A1
(6)(22) DMPADR-13•101 06 A2
(6)(22) DMPADR-12•101 05 A3
(6)(22) DMPADR-11•101 04 A4
(6)(22) DMPADR-10•101 03 A5
(6)(22) DMPADR-9•101 02 A6
(6)(22) DMPADR-8•101 01 A7
(6)(22) DMPADR-07•100 23 A8
(6)(22) DMPADR-06•100 22 A9
(6)(22) DMPADR-05•100 19 A10
(6)(22) DMPADR-04•100 21 A11
(10) DEN-4KROM-3•000 18 CE
(5,28)(22) MPRD•000 20 OE/VPP
1 09 DATA-BUS0-7•100 (9,16,17,18,19,20,21,24,26,28,29)(22)
2 10 DATA-BUS0-6•100 (9,16,17,18,19,20,21,24,26,28,29)(22)
3 11 DATA-BUS0-5•100 (9,16,17,18,19,20,21,23,24,26,29)(22)
4 13 DATA-BUS0-4•100 (9,16,17,18,19,20,21,24,26,29)(22)
5 14 DATA-BUS0-3•100 (9,16,17,18,19,20,21,24,26,29)(22)
6 15 DATA-BUS0-2•100 (9,16,17,18,19,20,21,24,26,29)(22)
7 16 DATA-BUS0-1•100 (9,16,17,18,19,20,21,24,26,29)(22)
8 17 DATA-BUS0-0•100 (9,16,17,18,19,20,21,24,26,29)(22)
58075894
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- WDAMP
SIZE B
DWG NO 58075894
SH 22.0
REV C



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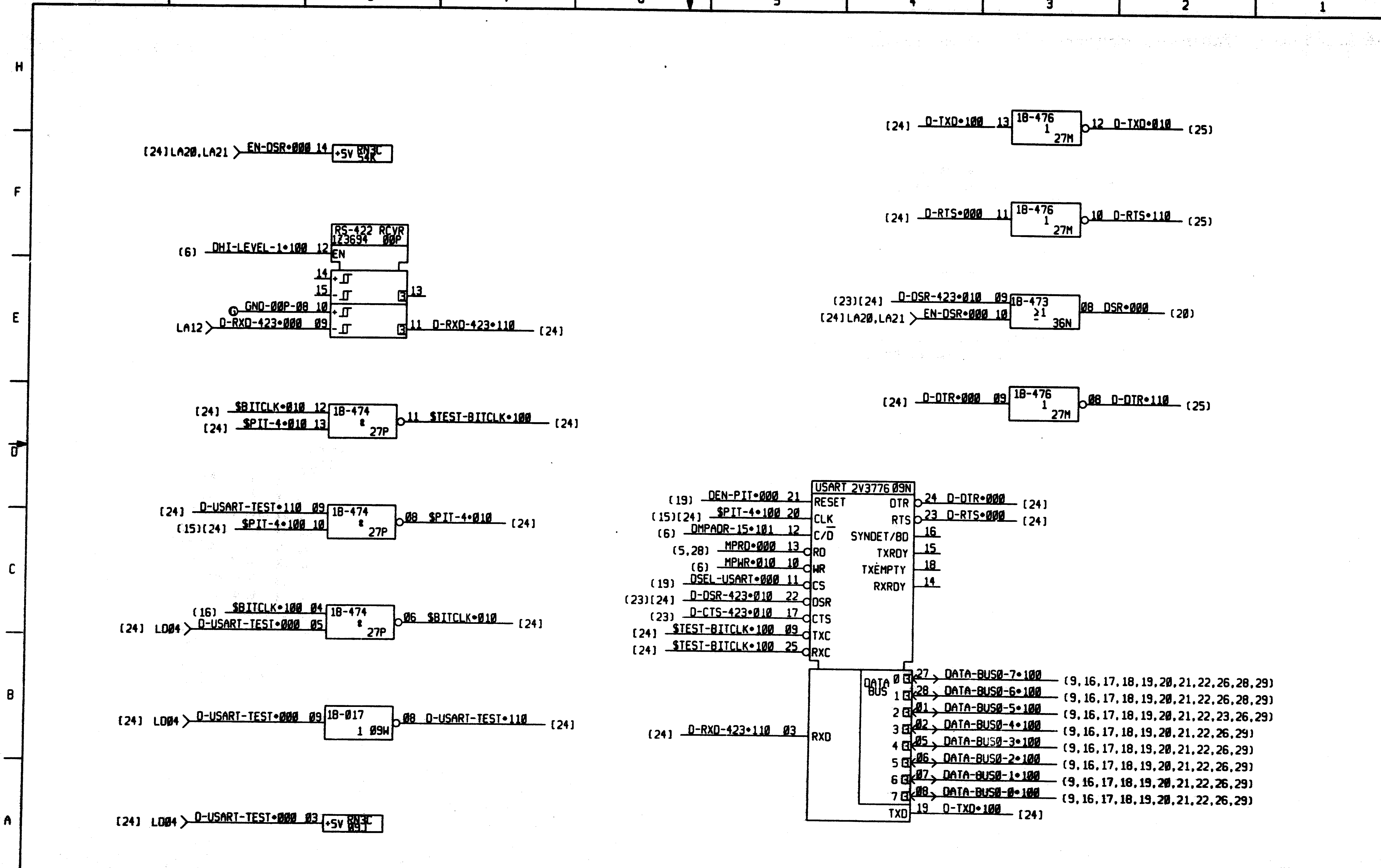
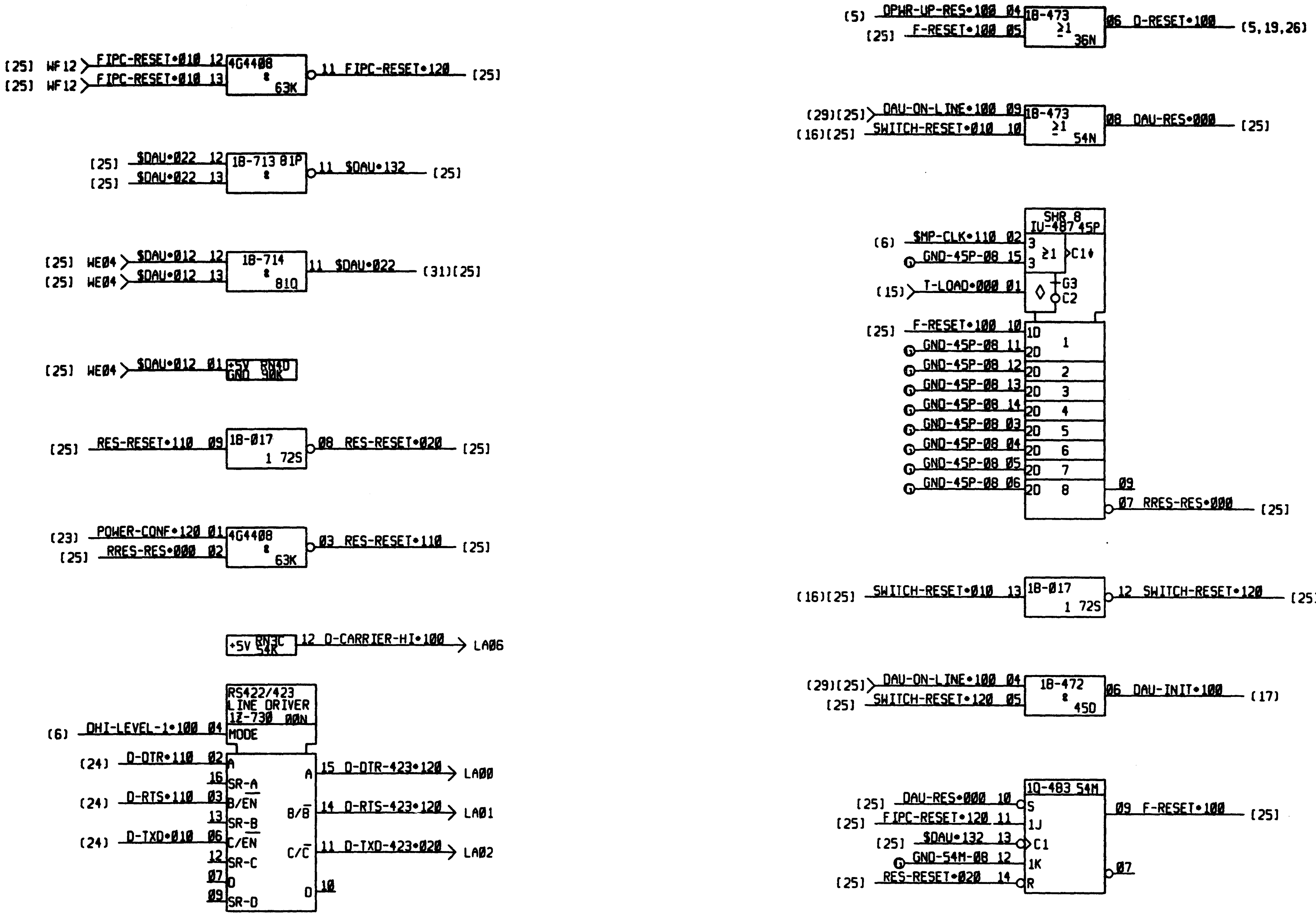
HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 23.0	REV C



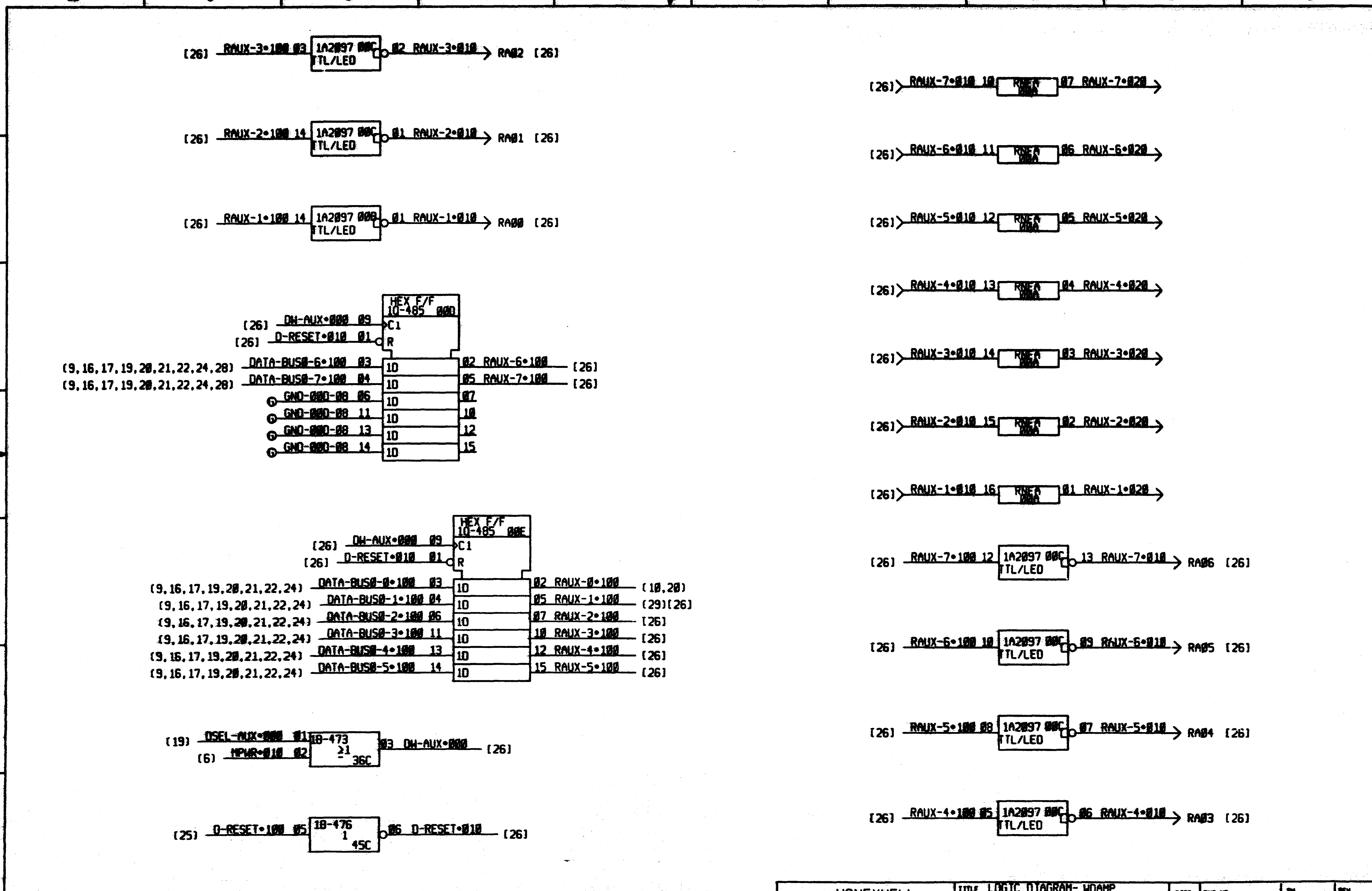
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- WDAMP
SIZE B
DWG NO 58075894
SH 24.0
REV C



HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 25.0	REV C

LOC

58075894



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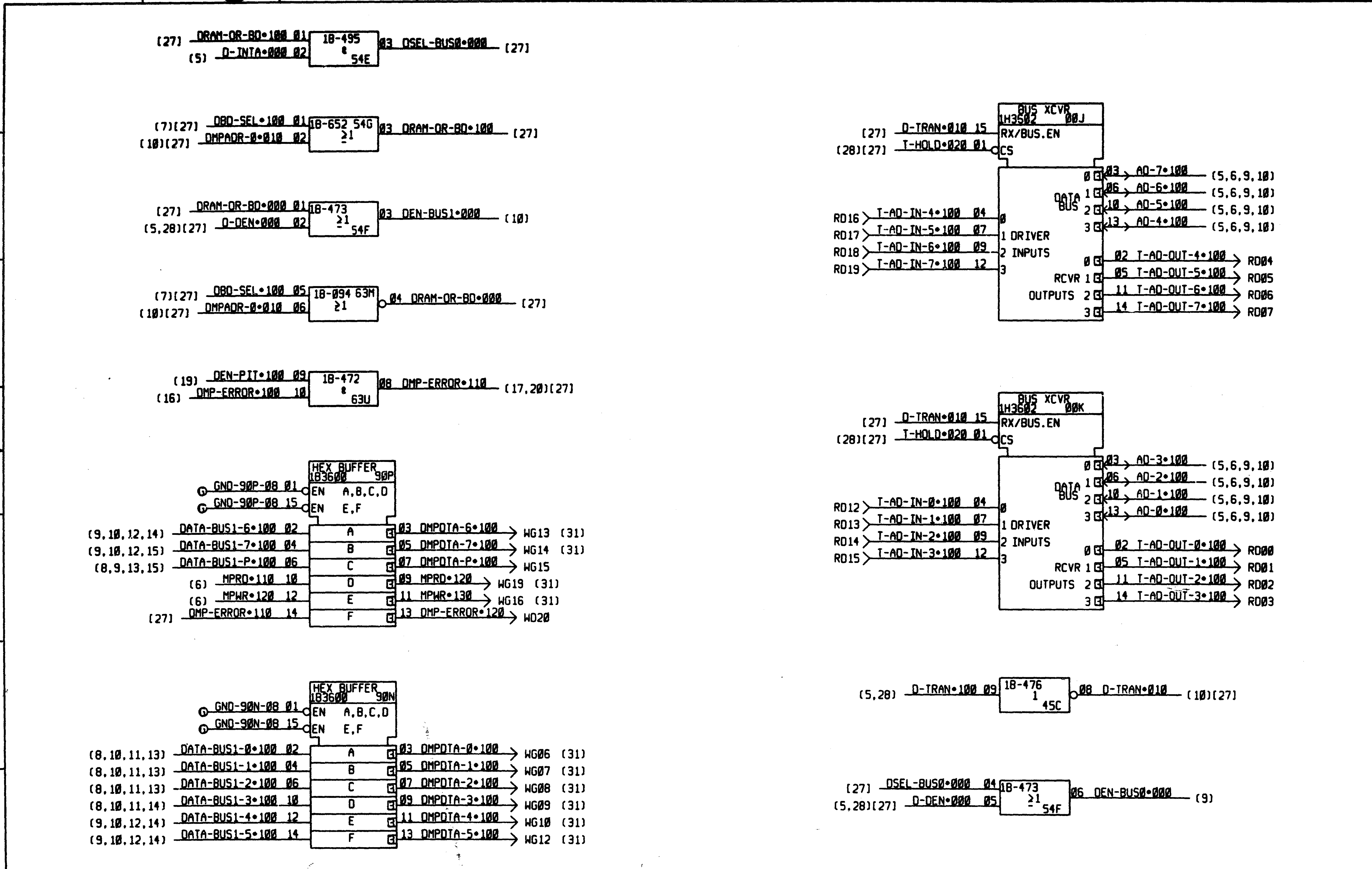
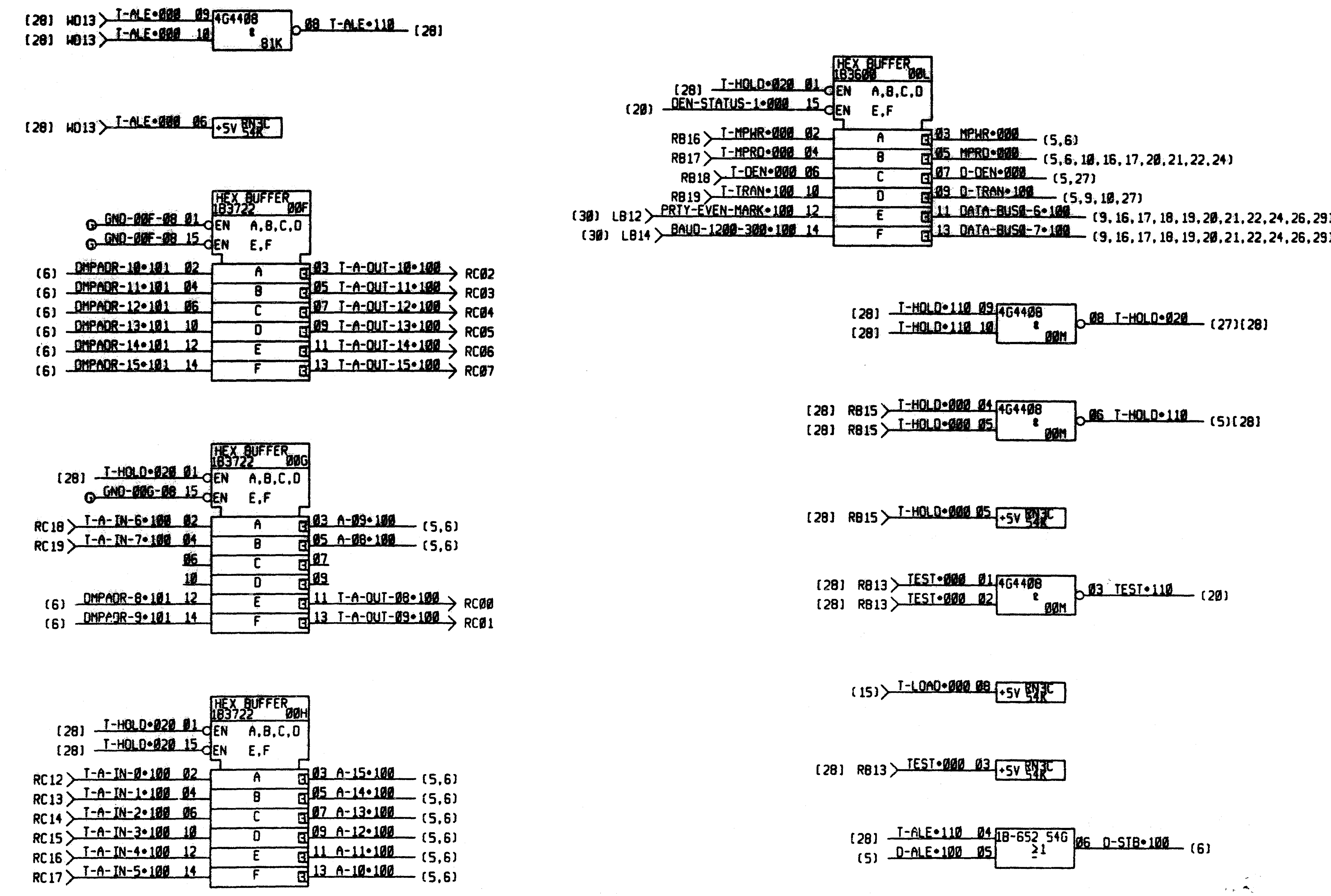
LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 26.0	REV C



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 27.0	REV C

58075894

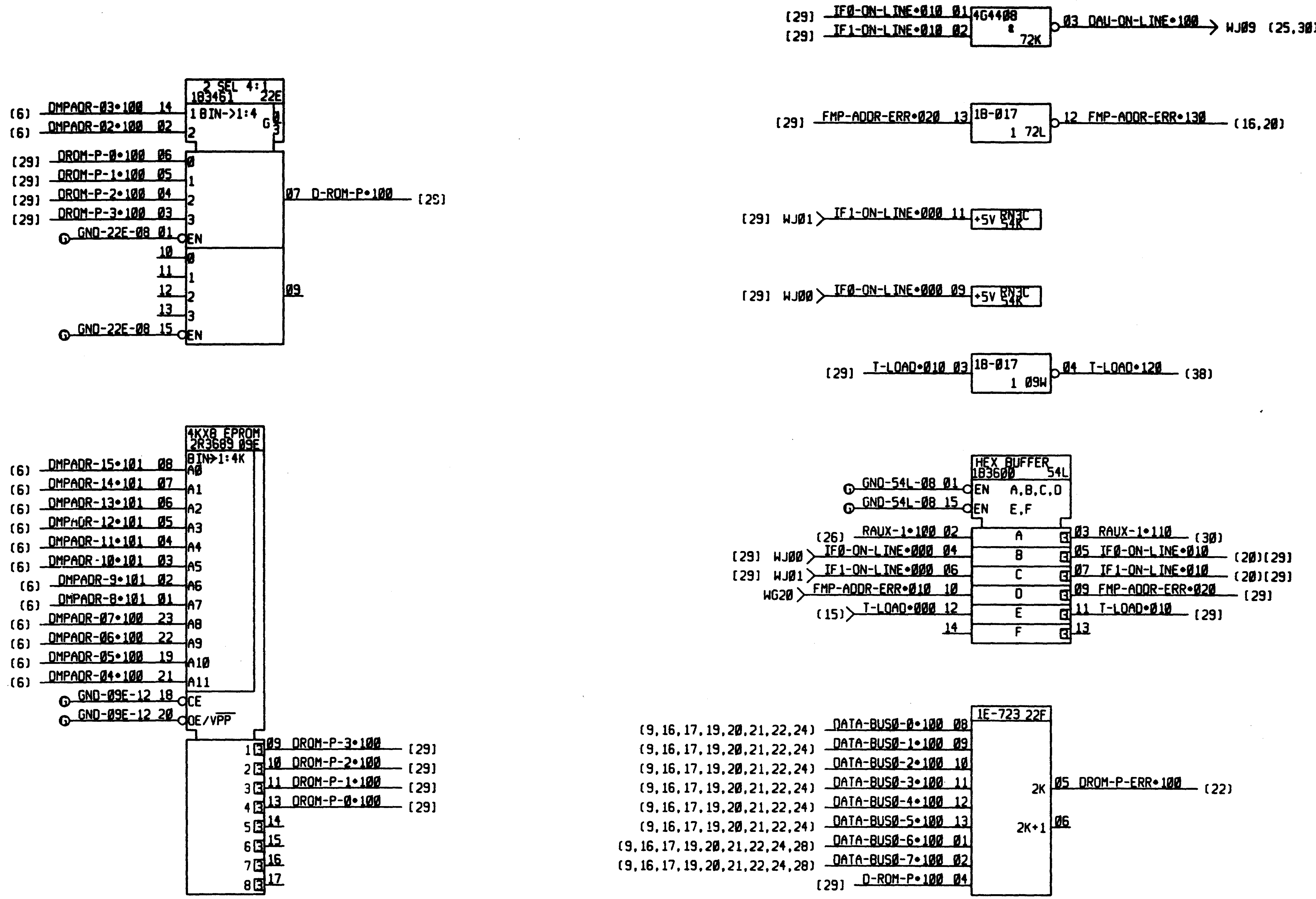


HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDAMP

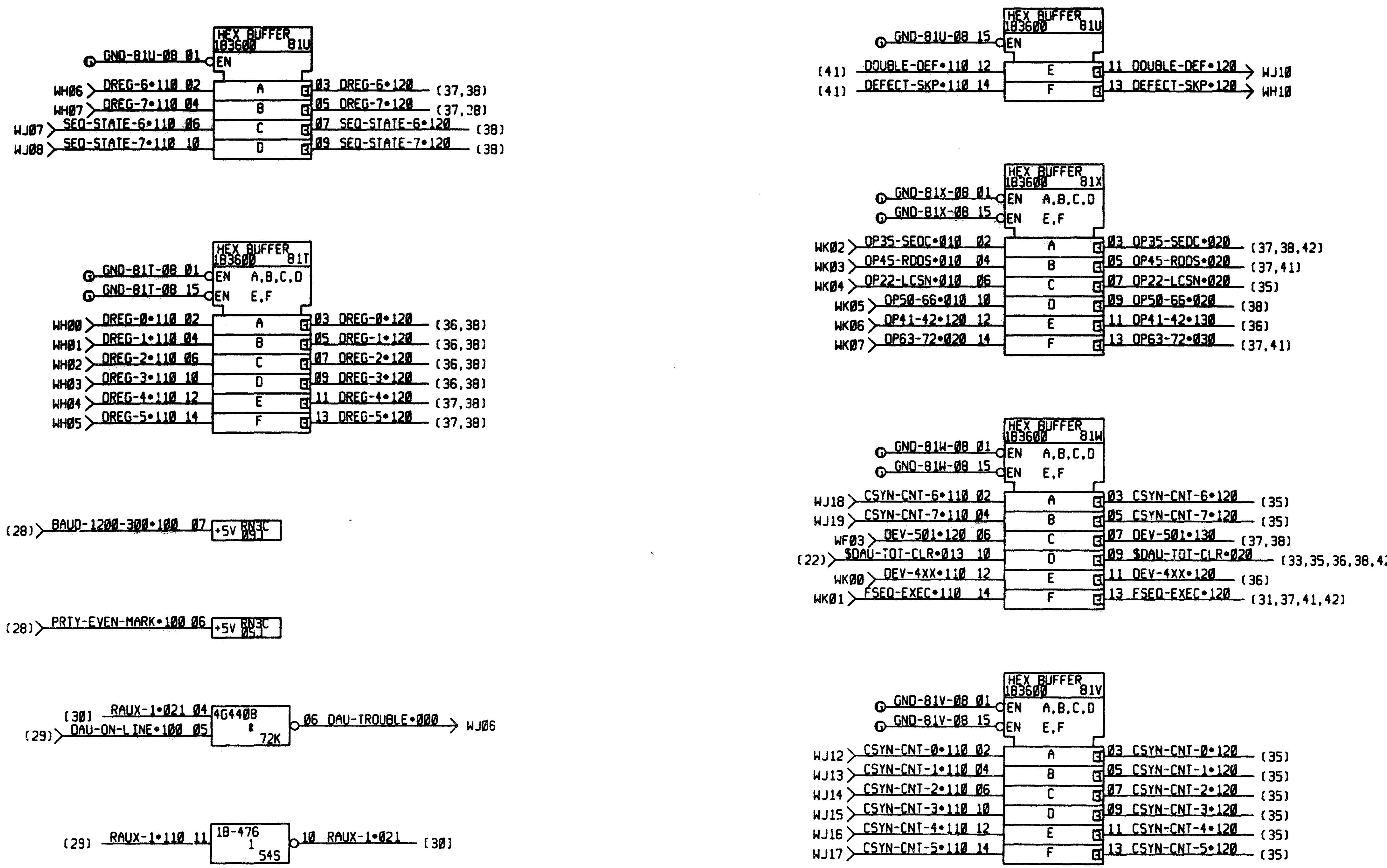
SIZE	DWG NO	SH	REV
B	58075894	28.0	C

58075894



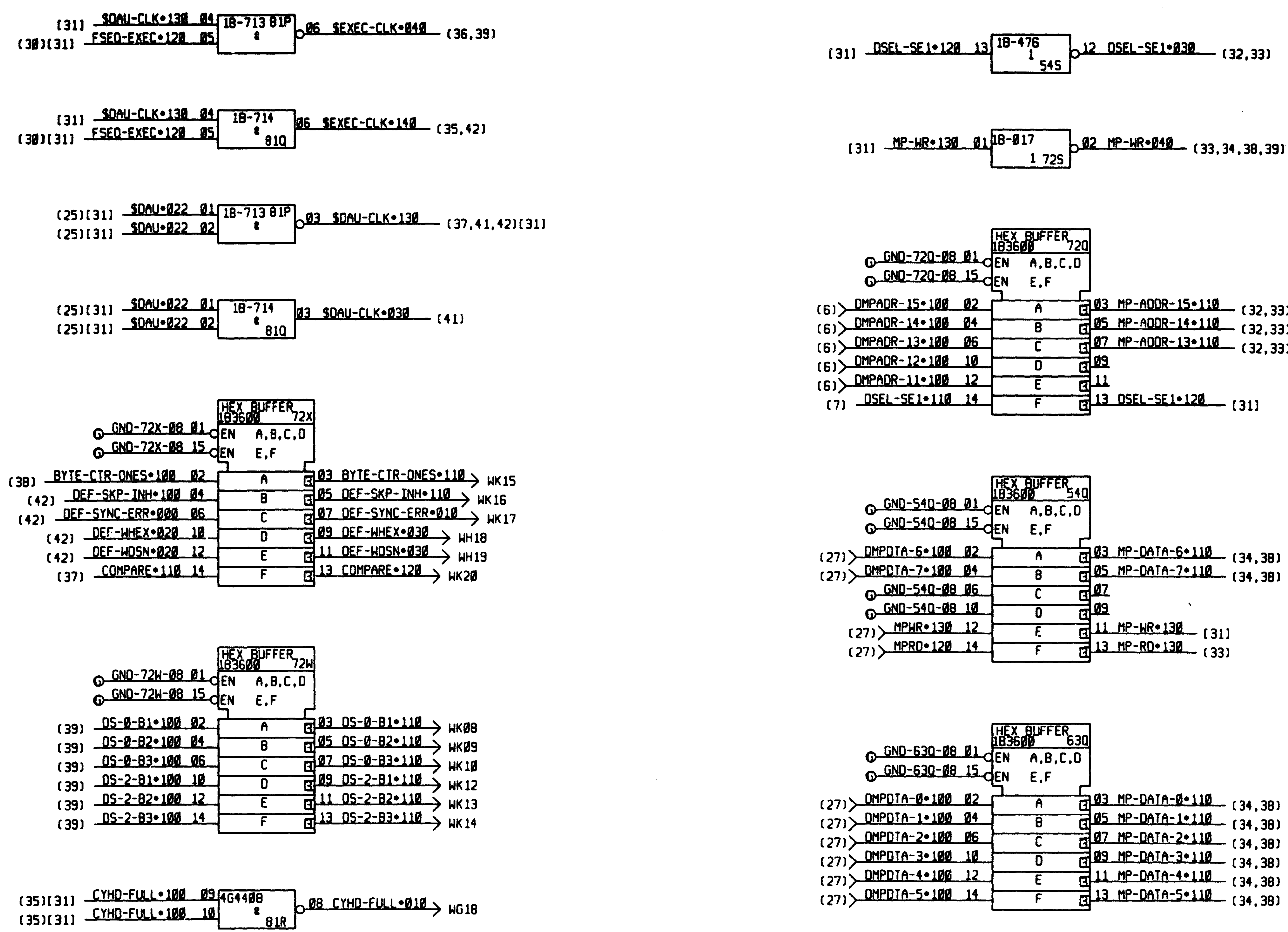
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

LOC	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 29.0	REV C

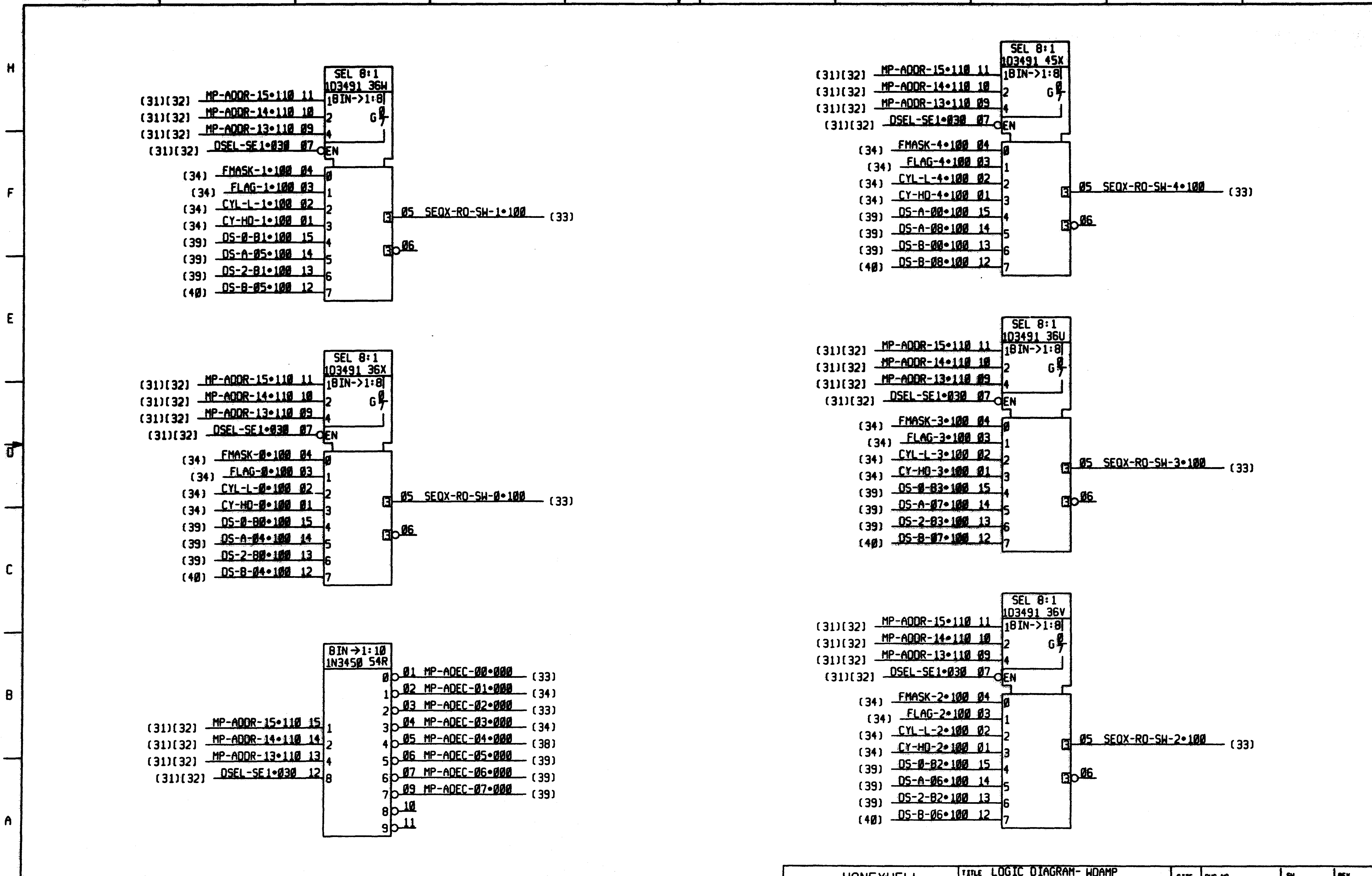


LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 30.0	REV C

58075894



HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A. LOC	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 31.0	REV C



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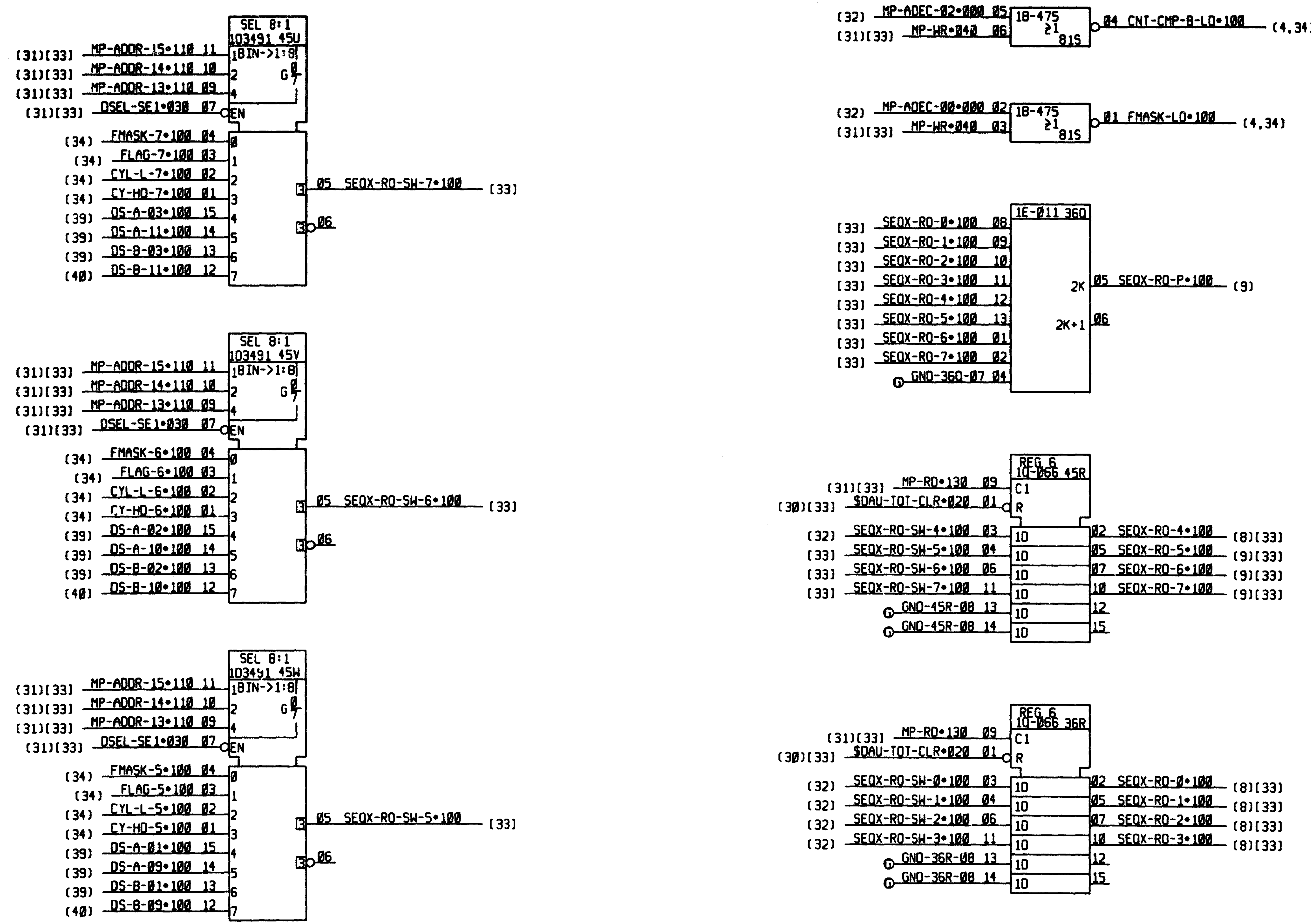
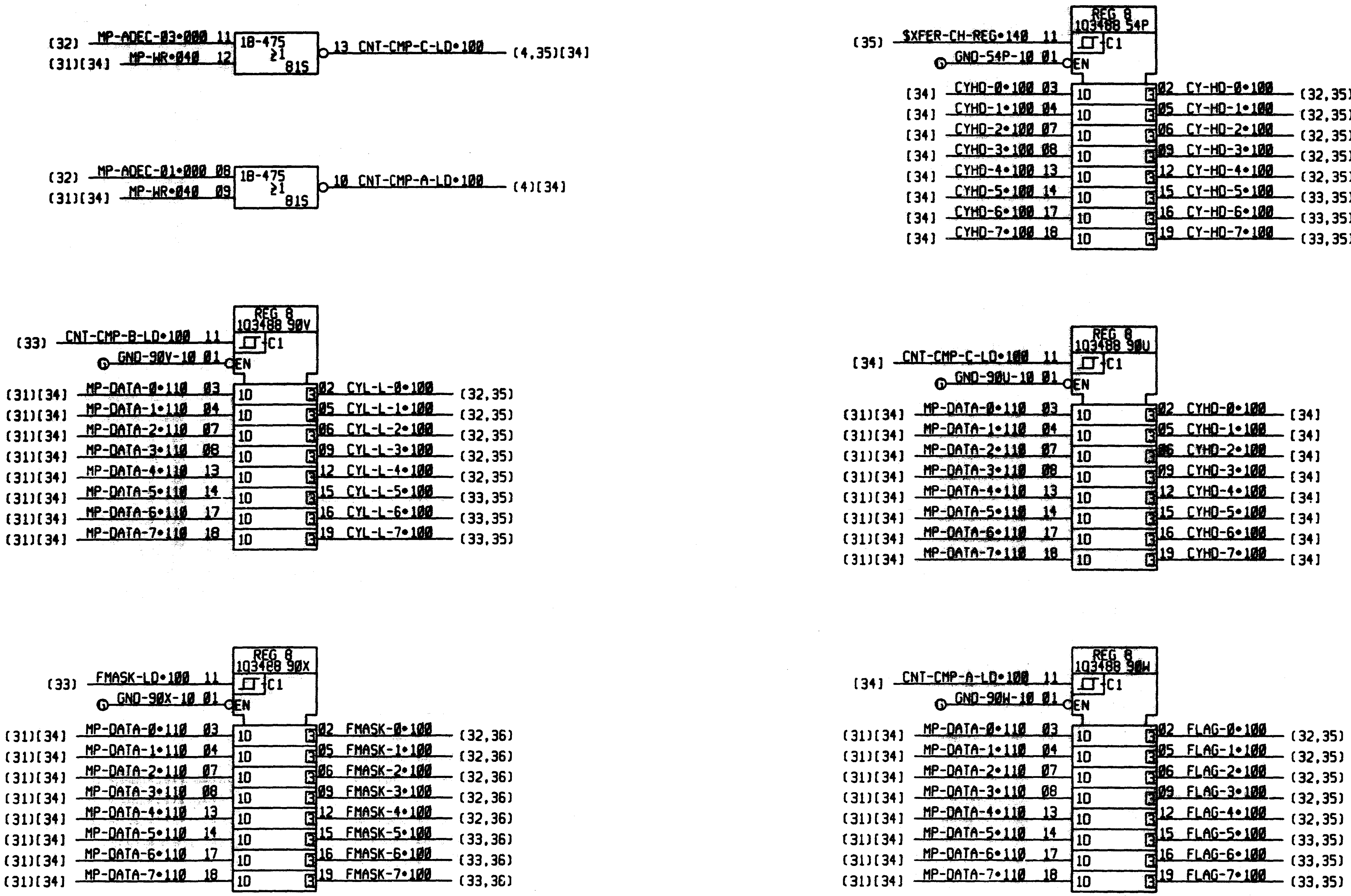
HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A. LOC	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58Ø75894	SH 32.Ø	REV C



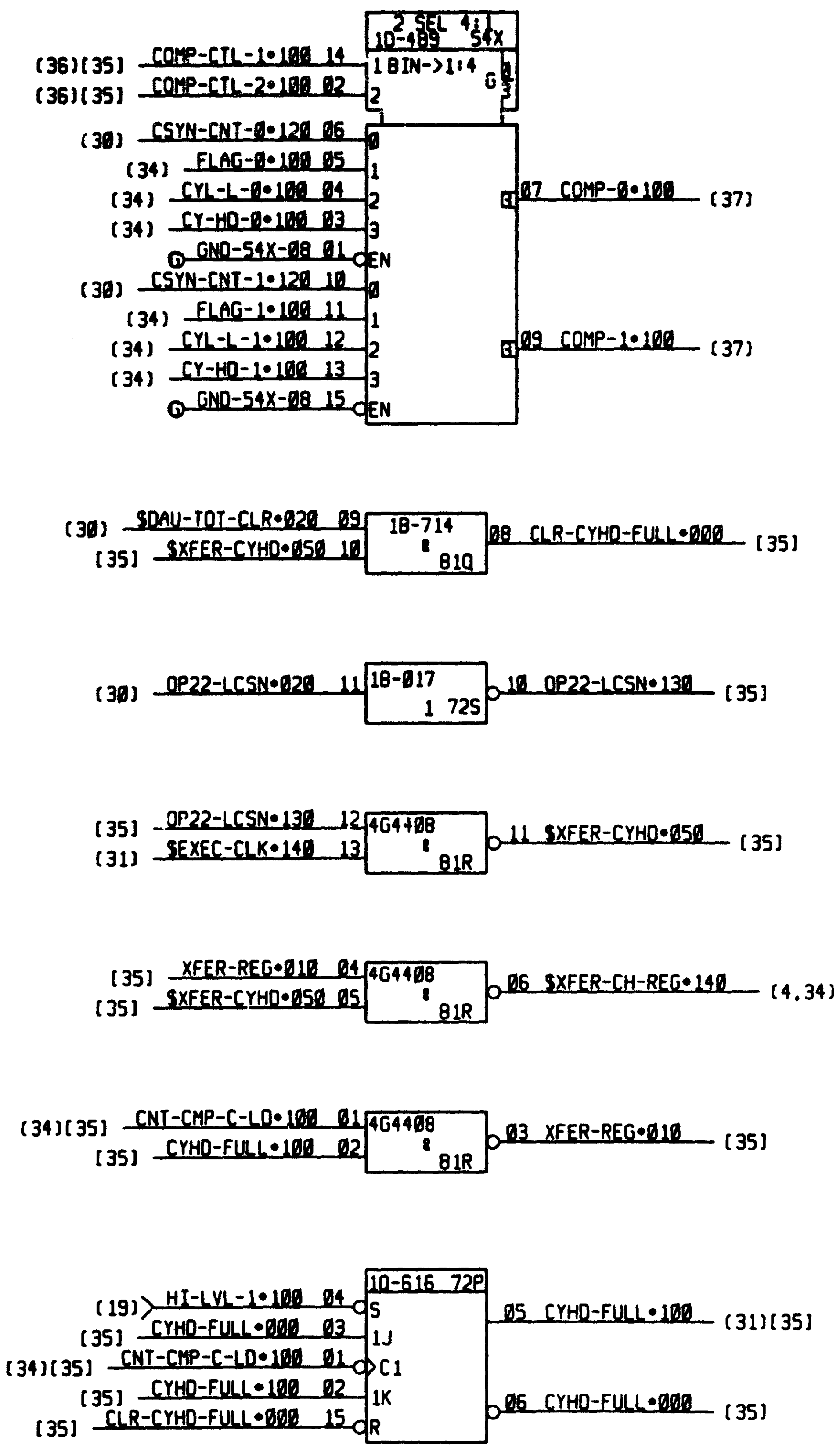
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC

TITLE	SIZE	DWG NO	SH	REV
LOGIC DIAGRAM- WDAMP	B	58075894	33.0	C

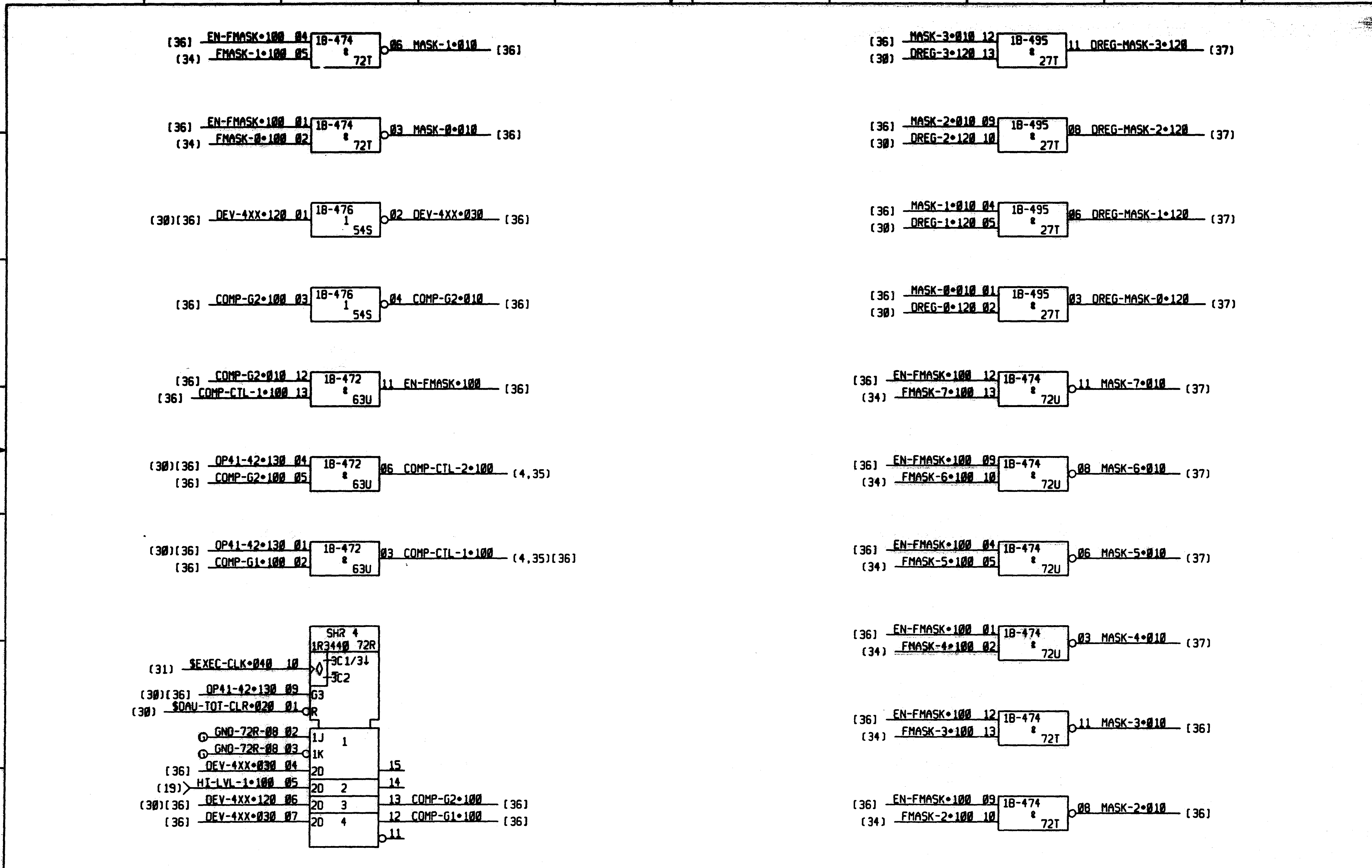


58075894

LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 34.0	REV C



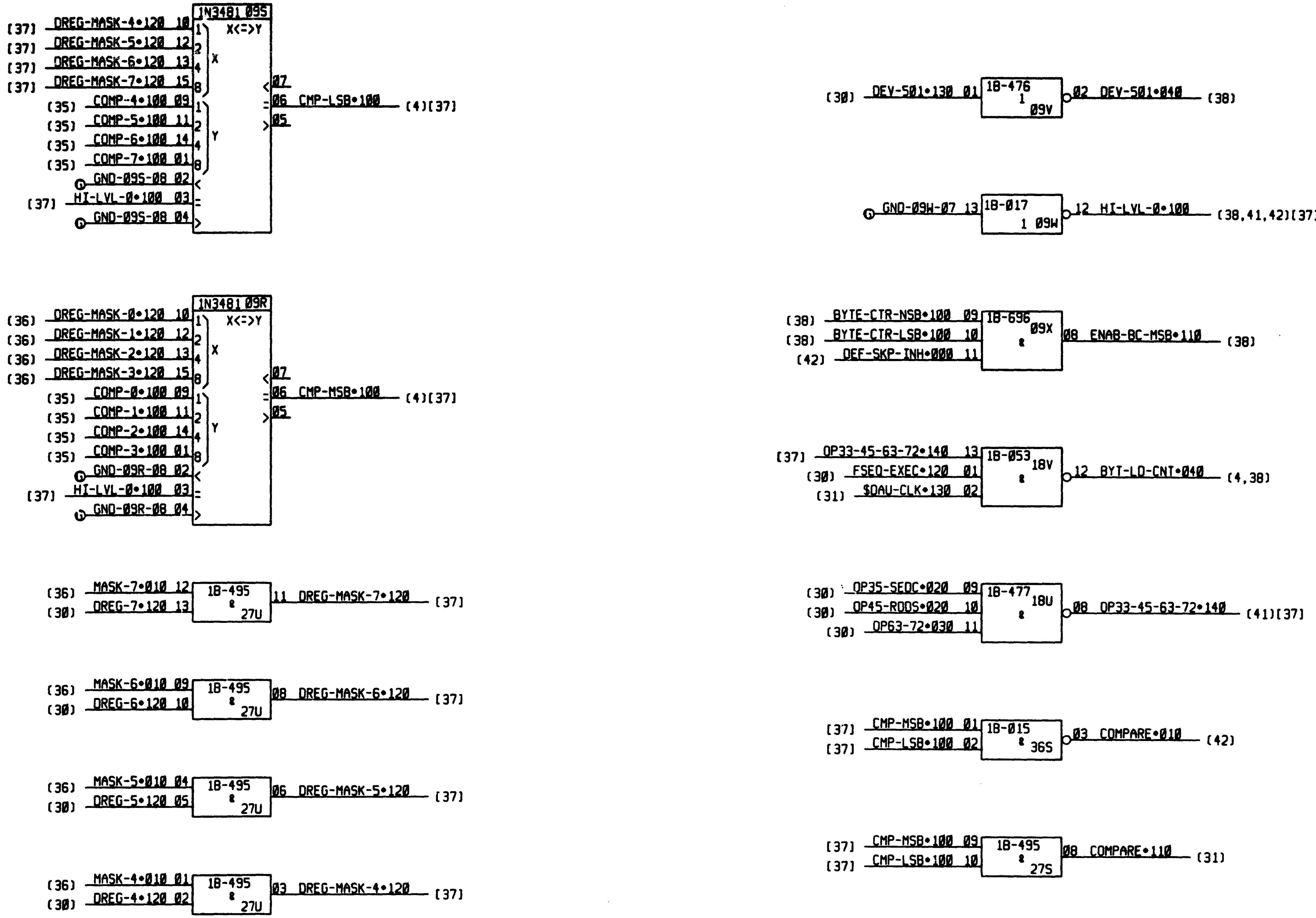
LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 35.0	REV C



HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC

TITLE LOGIC DIAGRAM- WDAMP

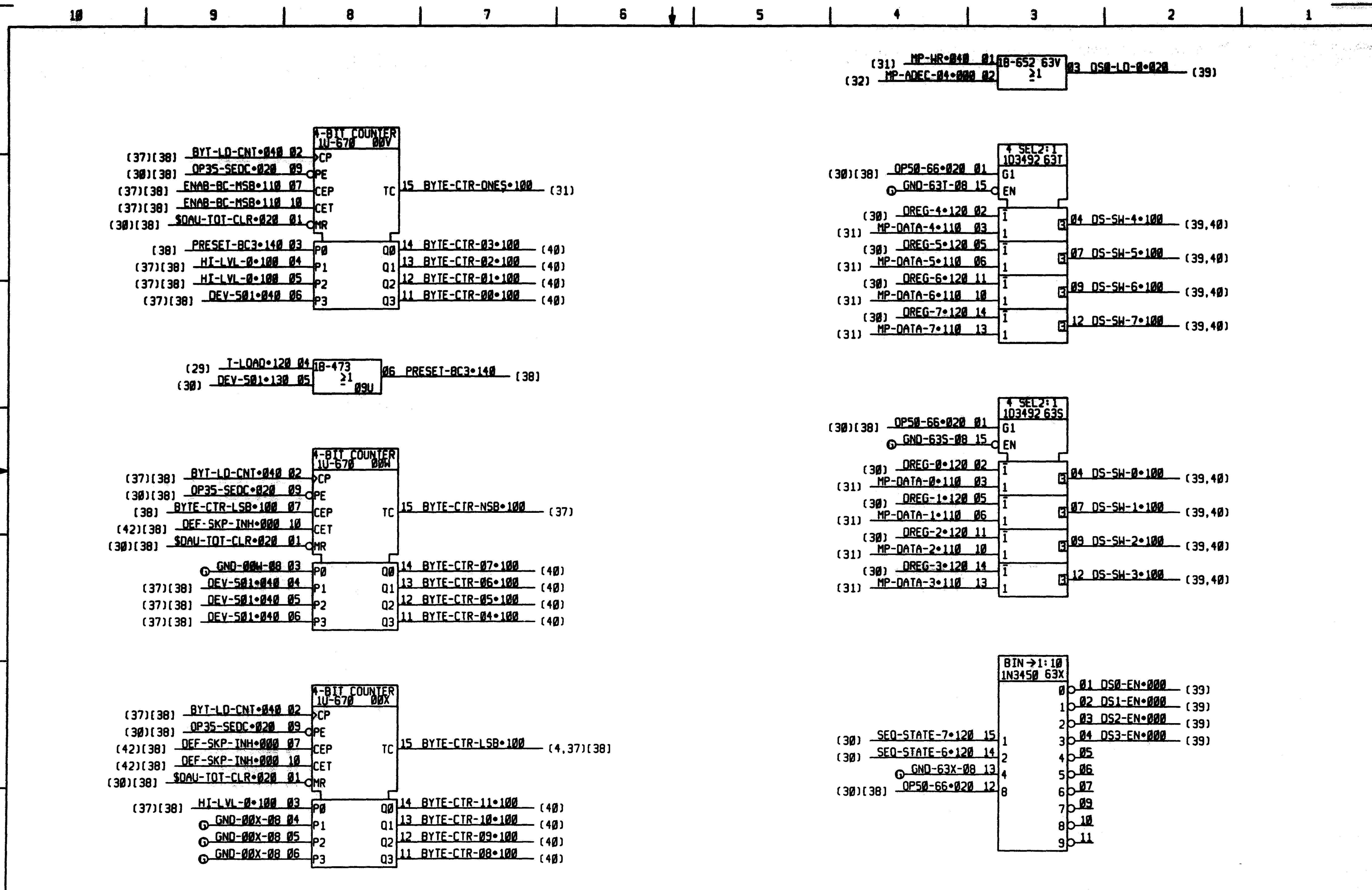
SIZE	DWG NO	SH	REV
B	58Ø75894	36.Ø	C



58075894

HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- WDAMP

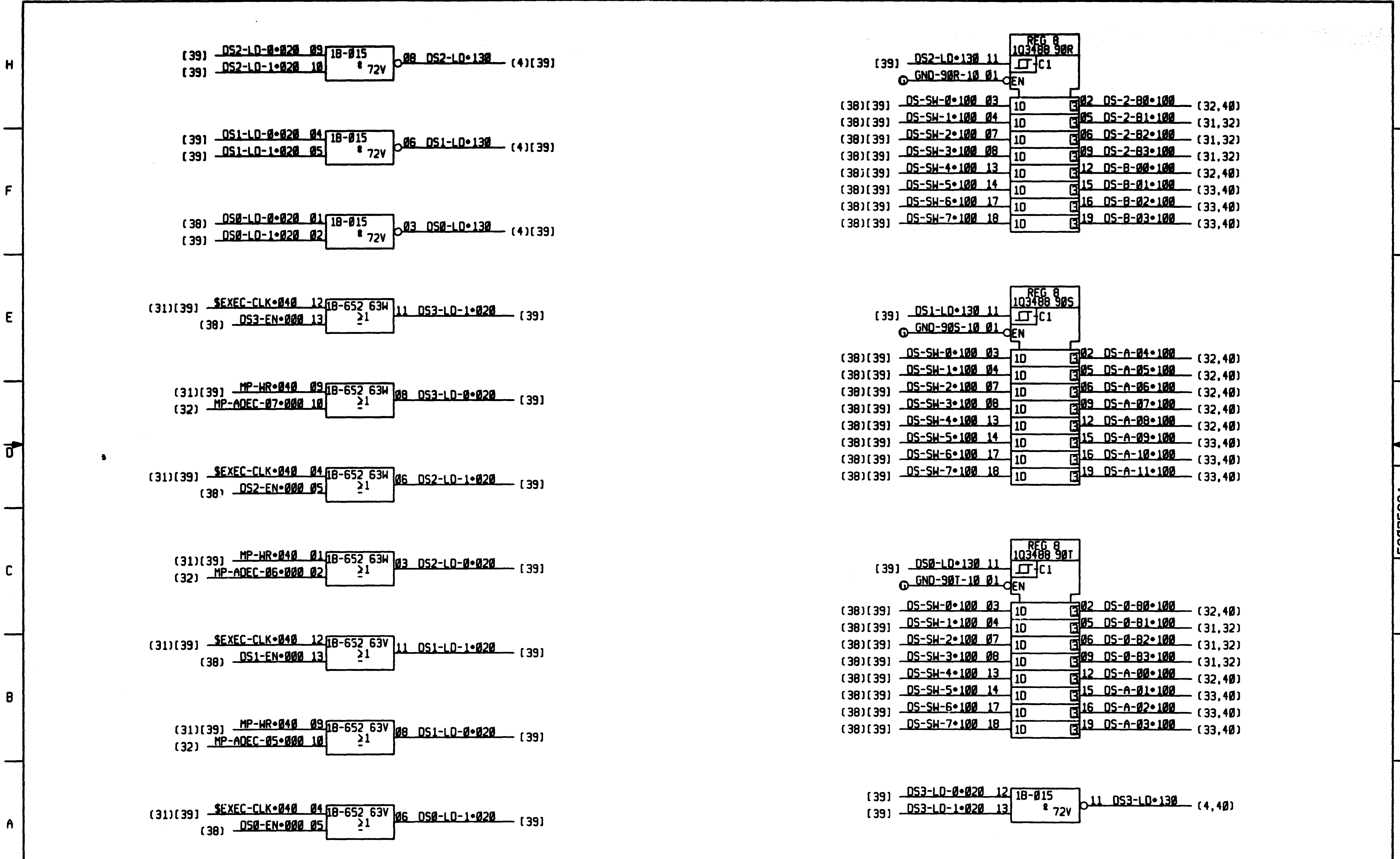
SIZE	DWG NO	SH	REV
B	58075894	37.0	C



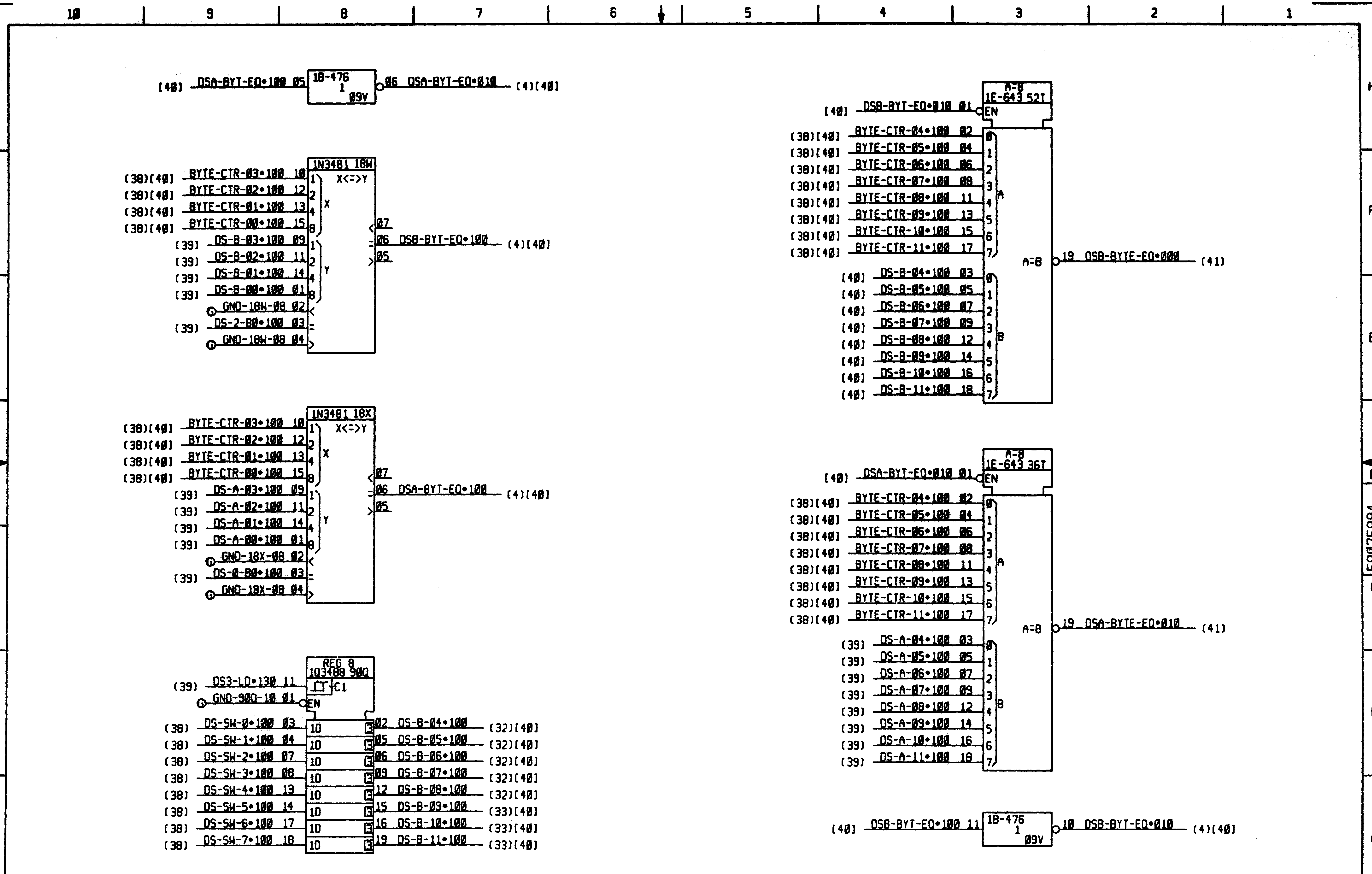
HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58Ø75894	SH 38.Ø	REV C

LOC

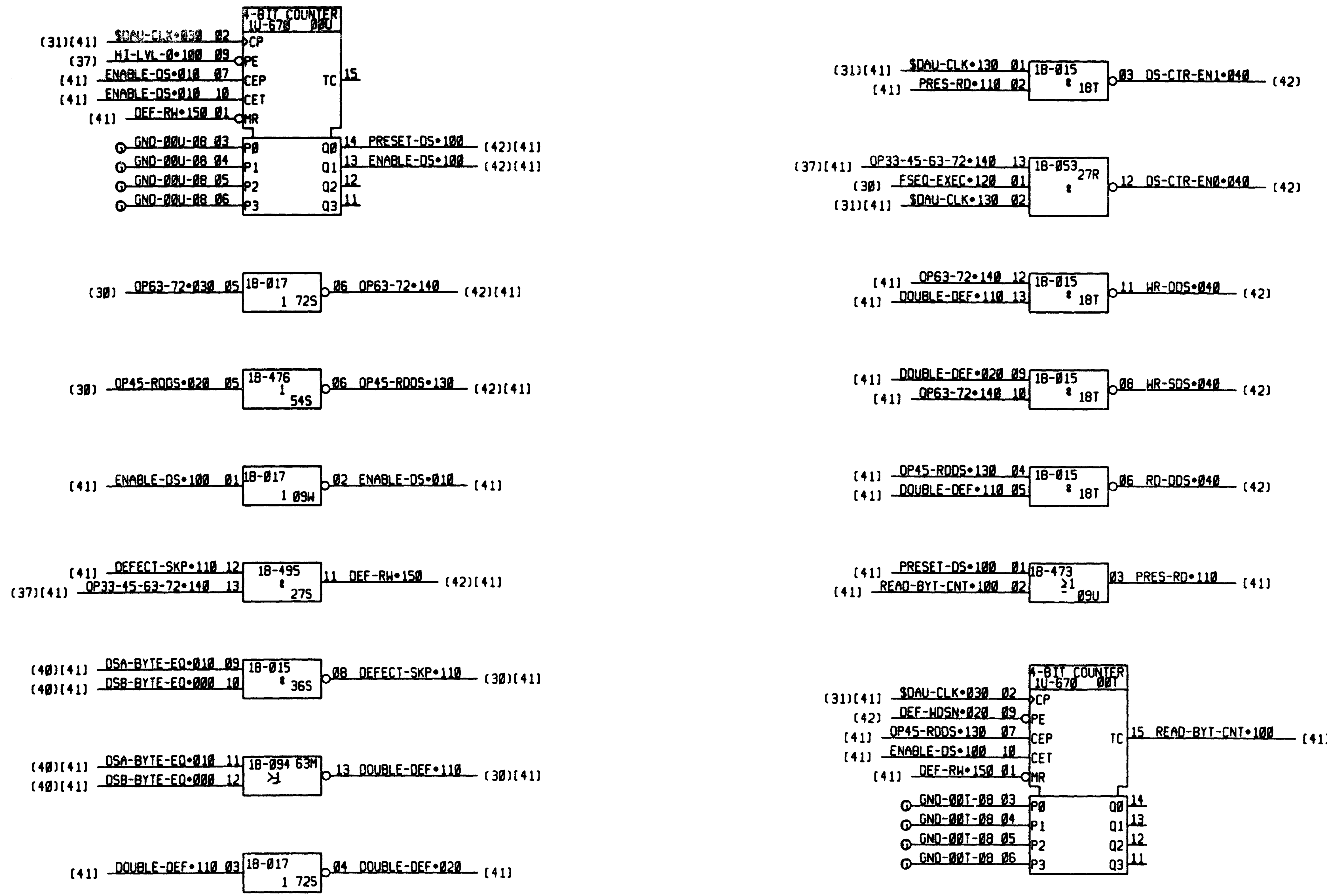
58Ø75894



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 39.0	REV C

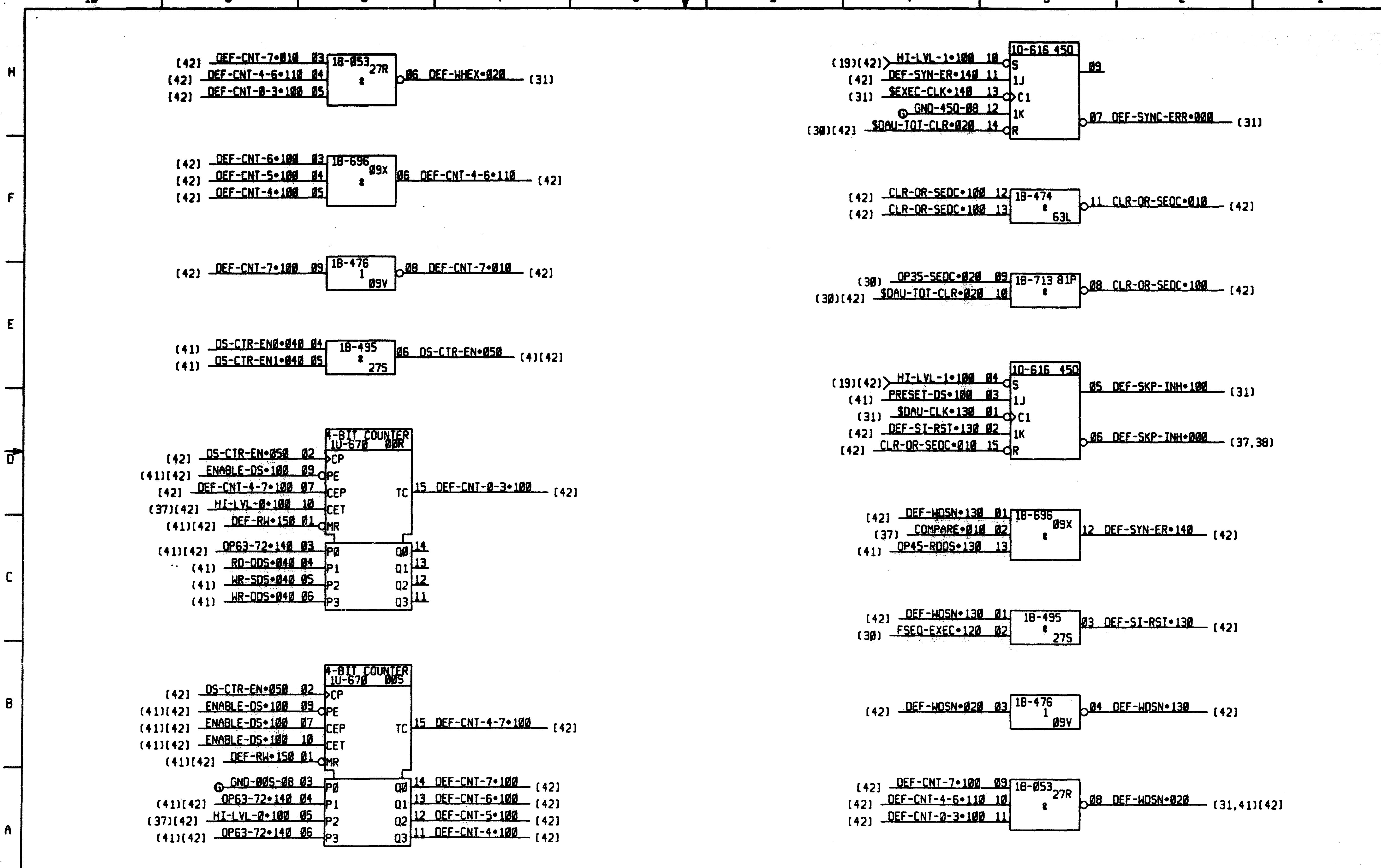


HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58Ø75894	SH 4Ø.Ø	REV C

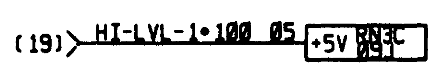


HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A. LOC	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 41.0	REV C

58075894



LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDAMP	SIZE B	DWG NO 58075894	SH 42.0	REV C


(19)
HI-LVL-1•1ØØ Ø5
+5V
RN3C
Ø9J

																			58075890	
REV	AUTHORITY	DATE			SIGNATURE	TAB													PL	
		YR	MO	DAY		001	102	003	203	104	304	405	205	005	506	306	106	006	All	
A	LEVEL 1 ISSUE	82	OCT	26	J.W. Boyle 10-6-82	A													A	
B	PHA0XS150	83	JAN	07	S. Miller	B													B	
C	PHA0XS156	83	01	25	G Drenth	C													C	
D	PHA0XS239	83	09	01	S. Miller	D	D												D	
D1	Level 2 ENXS149		ND		G Drenth		D1	E	E											
E	PHA0XS396	84	02	02	G Drenth		E	E	E										E	
F	PHA0XS469	84	05	11	G Drenth	OBSOLETE		F	F	F	F								F	
G	PHA0XS584	84	10	22	E Hicks		OBSOLETE			G	G	G	G	G					G	
H	PHA0AD518	84	NOV	26	G Drenth				OBSOLETE		RESERVED			H					H	
H1	PHA0GD739	85	FEB	21	G Drenth			H1		H1				H1					H1	
J	PHA0NJ059	86	03	04	G Drenth			OBSOLETED AT F REV		RESERVED AT G REV		J	J	J	J	J	J		J	
K	PHA0NJ065	87	06	29	D. Williams							RESV	RESV	RESV				K	K	
	58075894				LOGIC DIA					B	B	C	C	C	C	C	C			
					BD TEST DECK															

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX, ARIZONA

MADE BY C. Akers 9-23-82

APPROVED E. [illegible] 10-3-82

TITLE HDUHC PWA WDAMP

REVISION STATUS FOR EACH PAGE, SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

SIZE	REVISION STATUS FOR	SHEET	REV
X	58075890	1/1	K

DIST. 30

BRUNING 44-141 40366

CE 380 A-3 (1-79)

58060529

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 001	002	003	004	005	PL ALL
A	LEVEL 1 ISSUE	83	01	27	J.M. Boyle 1-21-83	A					A
A1	LEVEL 2 ENXS149		ND		G Drentle	A1					
B	PHA0XS459	83	03	23	G Drentle	B	B				B
C	PHA0XS584	84	10	22	E [illegible]	OBSOLETE	C	C			C
D	PHA0XS650	85	APR	25	G Drentle		OBSOLETE	D	D		D
E	PHA1NJ063	86	MAY	21	D. Williams			OBSOLETE	E	E	E
									OBSOLETE		

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY R.M.D Agostino 82 Sep 8

APPROVED E. [illegible] 1-19-83

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE FW ACCUM KIT WDAMP-1

SIZE	REVISION STATUS FOR	SHEET	REV
X	58060529	1/1	E

DIST. -6

BRUNING 44-141 40366

CE 300 A-3 (1-79)

				005		
*	1	A	58060530-005	D FW CIL WDAMP-1	X	
*	2	A	58060578-001	P ID LABEL FUNCT PWA	1	EA
*	3	A	58060578-002	P ID LABEL FUNCT PWA	1	EA
*	4	A	58002689-220	V UV 32K 4KX8 EPROM	1	EA
*	5	A	58002689-266	V UV 32K(4KX8) EPROM	1	EA
*	6	A	58002689-267	V UV 32K(4KX8) EPROM	1	EA
*	7	A	58002689-223	V UV 32K 4KX8 EPROM	1	EA
*	8	A	58002689-268	V UV 32K(4KX8) EPROM	1	EA

Honeywell HONEYWELL INFORMATION SYSTEMS		DWG. NO. 58060528	SHEET 1/3	REV B
LOC. PHOENIX, ARIZONA	DISTR C111-7B DATA BASE T060528 D060528	PROJECTION	CODE	
PREPARED BY DATE PMDAJB 83JAN20 APPROVED BY E. GOTTFRIED 83JAN20	TITLE INSTALLATION INSTRUCTION WDAMP EPROM FW KIT(S)		F.C.F.: 58060527 OP.LST: N/A	

REVISION RECORD

REV.	AUTHORITY	DATE	SIGNATURE	SHEETS AFFECTED
A	LEVEL 1 ISSUE	83JAN20	SEE APERTURE CARD	RSS, 1 THRU 3F
B	PHA0XS459	84FEB28	E. SERSANSIE	1 THRU 3F

I. SCOPE:

THIS INSTRUCTION PROVIDES THE INFORMATION NECESSARY IN THE INSTALLATION OF EPROMS ON THE WDAMP BOARD.

II. INSTALLATION PROCEDURE

1. FUNCTIONAL PWA WDAMP-1

1.1. REFER TO THE FUNCTIONAL PWA ASSEMBLY 58060527 PL FOR THE ITEM NUMBERS REFERENCED IN THE FOLLOWING INSTRUCTIONS UNLESS OTHERWISE SPECIFIED.

1.2. REFER TO FIGURE 1 FOR APPROXIMATE LOCATION AND IDENTITY OF ITEMS REFERRED TO IN INSTRUCTION STEPS THAT FOLLOW.

1.3. PLUG-IN THE PROGRAMMED EPROMS ON THE WDAMP-1 BOARD IN SOCKET LOCATIONS LISTED IN COMPONENT INSTALLATION LIST, 58060530, CALLED FOR ON ACCUMULATION KIT 58060529. USE CARE IN HANDLING AND INSTALLING THE EPROMS BY AVOIDING ANY STATIC CHARGE BUILD-UP ON THE BODY OF THE HANDLER OR PERSON.

1.4. INSTALL THE FUNCTIONAL BOARD ASM LABEL ITEM 4 ON BOARD. INSTALL THE LABEL ON THE BOARD STIFFENER SUCH THAT THE LABEL IS VERTICAL . REFER TO FIGURE 1 FOR GENERAL LOCATION OF THE FUNCTIONAL LABEL.

1.5. INSTALL THE APPROPRIATE TAB NUMBER AND REVISION LABELS TO THE FUNCTIONAL BOARD IDENTIFICATION NUMBER USING ITEMS 2 AND 3 PROVIDED IN THE FIRMWARE ACCUMULATION KIT, 58060529. (EXAMPLE: "001 A" AS INITIALLY ISSUED). SEE FUNCTIONAL BOARD ASSEMBLY RSS FOR TAB NUMBER AND REVISION LETTER.

III. REMOVAL PROCEDURE FOR BASIC OR OPTION PLUGGABLE EPROM KIT(S):

1. FOLLOW THE REVERSE PROCEDURE AND PRECAUTIONS OF THE INSTALLATION.

IV. PARTS DISPOSITION:

1. RETURN THE PARTS REMOVED IN THE STEP III ABOVE TO "LCPD" MANUFACTURING.

ADDRESS::

HONEYWELL INFORMATION SYSTEMS
P.O. BOX 8000
PHOENIX, ARIZONA 85066

C/O MGR LCPD WAREHOUSE
MAIL DROP J-2

Honeywell HONEYWELL INFORMATION SYSTEMS	INSTALLATION INSTRUCTION	DWG. NO. 58060528	SHEET 3F	REV B

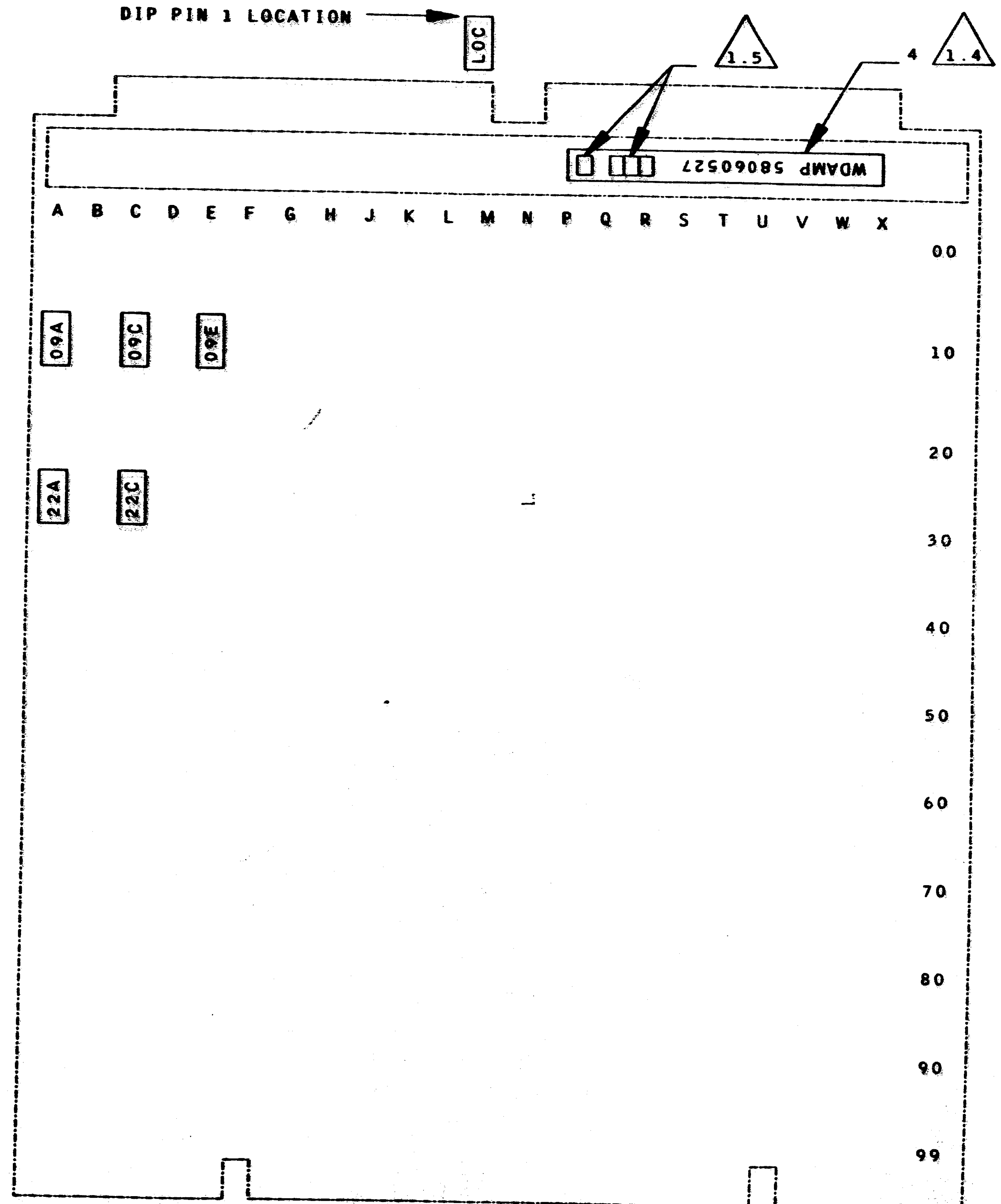


FIGURE 1

58075892

REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE	TAB NO 001	002	003	004		SH ALL
A	LVL 3 ISSUE	82	OCT	26	J. W. Boyle 10-6-82	A				1-10F	A
B	PHA0XS239	83	SEP	01	S. Miller	B	B			1-10F	B
C	PHA0XS396	84	02	02	G. Drenth	OBSOLETE	C	C		1-9F	C
D	PHA0XS469	84	05	11	G. Drenth		OBSOLETE	D OBSOLETE	D	1-9F	D

FOR CONTINUATION OF REVISION STATUS SEE SHEET

BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX, ARIZONA

CE 300 A-3 (1-79)

MADE BY J. Kajurski 82 Sept. 07

APPROVED E. Gottfried 10-3-82

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CIL WDAMP

SIZE A | REVISION STATUS FOR 58075892 | SHEET 1/1 | REV D

DIST. 37

COMP INSTL LIST - WDAMP

TAB-004

STANDARD LOCATION CODE PATTERN
X-POS & Y-POS PER 58046507-002
UNLESS OTHERWISE SHOWN, ROTATION IS NORTH

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
00A	RNFA	43B216592P47			
00AE	P9	43A114748P9			
00B	1A2097	58002097-001			
00C	1A2097	58002097-001			
00CE	P1043	43C212092P1043			
00D	1Q-485	58002485-001			
00E	1Q-485	58002485-001			
00EE	P1043	43C212092P1043			
00F	1B3722	58002722-001			
00G	1B3722	58002722-001			
00GE	P9	43A114748P9			
00H	1B3722	58002722-001			
00J	1H3602	58002602-001			
00JE	P1043	43C212092P1043			
00K	1H3602	58002602-001			
00KE	P1043	43C212092P1043			
00L	1B3600	58002600-001			
00LE	P1043	43C212092P1043			
00M	4G4408	43C216408P1			
00ME	P1243	43C212092P1243			
00N	1Z-730	58002730-001			
00NE	P9	43A114748P9			
00P	1Z3694	58002694-001			
00QE	P1043	43C212092P1043			
00R	1U-670	58002670-001			
00S	1U-670	58002670-001			
00SE	P1043	43C212092P1043			
00T	1U-670	58002670-001			
00U	1U-670	58002670-001			
00UE	P9	43A114748P9			
00V	1U-670	58002670-001			
00VE	RSOH	58020479-008			

COMP INSTL LIST - WDAMP

TAB-004

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
00W	1U-670	58002670-001			
00WE	P1043	43C212092P1043			
00X	1U-670	58002670-001			
09A	2R3689	*----------*			
09A	SK24	58020384-006			
09BD	P9	43A114748P9			
09C	2R3689	*----------*			
09C	SK24	58020384-006			
09DD	P1043	43C212092P1043			
09E	2R3689	*----------*			
09E	SK24	58020384-006			
09FD	P1043	43C212092P1043			
09G	2V-574	58002574-001			
09HD	P9	43A114748P9			
09J	RN3C	43B216592P12			
09JE	P1043	43C212092P1043			
09K	1B-696	58002696-001			
09KE	P1043	43C212092P1043			
09L	2V-576	58002576-001			
09MD	P1043	43C212092P1043			
09N	2V3776	58002776-001			
09PD	P1043	43C212092P1043			
09QE	P1043	43C212092P1043			
09R	1N3481	58002481-001			
09S	1N3481	58002481-001			
09SE	P1043	43C212092P1043			
09U	1B-473	58002473-001			
09UE	P9	43A114748P9			
09V	1B-476	58002476-001			
09W	1B-017	58002017-001			
09WE	P1043	43C212092P1043			
09X	1B-696	58002696-001			
16VE	RSOH	58020479-008			
18SE	P9	43A114748P9			
18T	1B-015	58002015-001			
18U	1B-477	58002477-001			
18UE	P1043	43C212092P1043			
18V	1B-053	58002053-001			

TAB-004

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
18W	1N3481	58002481-001			
18WE	P1043	43C212092P1043			
18X	1N3481	58002481-001			
22A	2R3689	*-----------*			
22A	SK24	58020384-006			
22C	2R3689	*-----------*			
22C	SK24	58020384-006			
22E	1B3461	43C216461P1			
22F	1E-723	58002723-001			
22G	1Q3488	58002488-001			
22H	1Q3488	58002488-001			
22J	1B3691	58002691-001			
24BD	P9	43A114748P9			
24DD	P1043	43C212092P1043			
24EE	P1043	43C212092P1043			
24GE	P9	43A114748P9			
24HE	P1043	43C212092P1043			
24K	SK40	58020384-008			
24K	2V-688	58002688-001			
24LD	P1043	43C212092P1043			
24RE	RSOH	58020479-008			
27M	1B-476	58002476-001			
27N	XLOY	43C216118P59			
27P	1B-474	58002474-001			
27PE	P9	43A114748P9			
27Q	1U-482	58002482-001			
27QE	P9	43A114748P9			
27R	1B-053	58002053-001			
27S	1B-495	58002495-001			
27SE	P1043	43C212092P1043			
27T	1B-495	58002495-001			
27U	1B-495	58002495-001			
27UE	P9	43A114748P9			
27WE	P9	43A114748P9			
32GE	P9	43A114748P9			
32HE	P1043	43C212092P1043			
33G	1D3492	58002492-001			
33H	1D3492	58002492-001			

TAB-004

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
34E	1E-643	58002643-001			
34F	1E-643	58002643-001			
35P	1Z-690	58002690-001			
36A	1C-648	58002648-001			
36B	1B3468	58002468-001			
36BE	P9	43A114748P9			
36C	1B-473	58002473-001			
36CE	RSOH	58020479-008			
36D	1B3722	58002722-001			
36DE	P1043	43C212092P1043			
36EE	P1043	43C212092P1043			
36LE	P1043	43C212092P1043			
36M	1U-482	58002482-001			
36N	1B-473	58002473-001			
36NE	P9	43A114748P9			
36Q	1E-011	58002011-001			
36QE	P1043	43C212092P1043			
36R	1Q-066	58002066-001			
36S	1B-015	58002015-001			
36SE	P1043	43C212092P1043			
36T	1E-643	58002643-001			
36U	1D3491	58002491-001			
36UE	P9	43A114748P9			
36V	1D3491	58002491-001			
36W	1D3491	58002491-001			
36WE	P1043	43C212092P1043			
36X	1D3491	58002491-001			
43G	1Q3692	58002692-001			
43H	1Q3692	58002692-001			
43J	1Q3692	58002692-001			
45AE	P9	43A114748P9			
45B	1B-475	58002475-001			
45C	1B-476	58002476-001			
45CE	P1043	43C212092P1043			
45D	1B-472	58002472-001			
45E	1C-648	58002648-001			
45EE	P1043	43C212092P1043			
45F	1B-726	58002726-001			

COMP INSTL LIST - WDAMP

TAB-004

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
45GE	P9	43A114748P9			
45HE	P9	43A114748P9			
45JE	P1043	43C212092P1043			
45K	1E-723	58002723-001			
45LE	P1043	43C212092P1043			
45M	1Q-483	58002483-001			
45N	1U-482	58002482-001			
45NE	P9	43A114748P9			
45P	1U-487	58002487-001			
45Q	1Q-616	58002616-001			
45QE	P1043	43C212092P1043			
45R	1Q-066	58002066-001			
45SE	P1043	43C212092P1043			
45U	1D3491	58002491-001			
45UE	P9	43A114748P9			
45V	1D3491	58002491-001			
45W	1D3491	58002491-001			
45WE	P1043	43C212092P1043			
45X	1D3491	58002491-001			
52T	1E-643	58002643-001			
54AE	P9	43A114748P9			
54B	1E-723	58002723-001			
54C	1B-477	58002477-001			
54CE	P1043	43C212092P1043			
54D	1B-696	58002696-001			
54E	1B-495	58002495-001			
54EE	P1043	43C212092P1043			
54F	1B-473	58002473-001			
54G	1B-652	58002652-001			
54GE	P9	43A114748P9			
54H	1Q-483	58002483-001			
54J	1B3691	58002691-001			
54JE	P1043	43C212092P1043			
54K	RN3C	43B216592P12			
54L	1B3600	58002600-001			
54LE	P1043	43C212092P1043			
54M	1Q-483	58002483-001			
54N	1B-473	58002473-001			

COMP INSTL LIST - WDAMP

TAB-004

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
54NE	P9	43A114748P9			
54P	1Q3488	58002488-C01			
54Q	1B3600	58002600-001			
54QE	P1043	43C212092P1043			
54R	1N3450	43C216450P1			
54S	1B-476	58002476-001			
54SE	P1043	43C212092P1043			
54U	1D-489	58002489-001			
54UE	P9	43A114748P9			
54V	1D-489	58002489-001			
54W	1D-489	58002489-001			
54WE	P1043	43C212092P1043			
54X	1D-489	58002489-001			
56VE	RSOH	58020479-008			
63G	1B3468	58002468-001			
63H	1B3468	58002468-001			
63K	4G4408	43C216408P1			
63L	1B-474	58002474-001			
63M	1B-094	58002094-001			
63Q	1B3600	58002600-001			
63S	1D3492	58002492-001			
63T	1D3492	58002492-001			
63U	1B-472	58002472-001			
63V	1B-652	58002652-001			
63W	1B-652	58002652-001			
63X	1N3450	43C216450P1			
64GE	P9	43A114748P9			
64JE	P1043	43C212092P1043			
64LE	P1043	43C212092P1043			
64NE	P9	43A114748P9			
64QE	P1043	43C212092P1043			
64SE	P1043	43C212092P1043			
64UE	P9	43A114748P9			
64WE	P1043	43C212092P1043			
68A	1S2768	98002768-001			
68B	1S2768	98002768-001			
68C	1S2768	98002768-001			
68D	1S2768	98002768-001			

TAB-004

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
68E	1S2768	98002768-001			
68F	1S2768	98002768-001			
72AE	P1043	43C212092P1043			
72BE	P1043	43C212092P1043			
72CE	P1043	43C212092P1043			
72DE	P1043	43C212092P1043			
72EE	P1043	43C212092P1043			
72FE	P1043	43C212092P1043			
72G	1B3462	43C216462P1			
72GE	P9	43A114748P9			
72H	1B3462	43C216462P1			
72J	1B3462	43C216462P1			
72JE	P1043	43C212092P1043			
72K	4G4408	43C216408P1			
72L	1B-017	58002017-001			
72LE	P1043	43C212092P1043			
72N	1B3600	58002600-001			
72NE	P9	43A114748P9			
72P	1Q-616	58002616-001			
72Q	1B3600	58002600-001			
72QE	P1043	43C212092P1043			
72R	1R3440	43C216440P1			
72RE	RSOH	58020479-008			
72S	1B-017	58002017-001			
72SE	P1043	43C212092P1043			
72T	1B-474	58002474-001			
72U	1B-474	58002474-001			
72UE	P9	43A114748P9			
72V	1B-015	58002015-001			
72VE	RSOH	58020479-008			
72W	1B3600	58002600-001			
72WE	P1043	43C212092P1043			
72X	1B3600	58002600-001			
72YD	P16	43A114748P16			
79A	1S2768	98002768-001			
79B	1S2768	98002768-001			
79C	1S2768	98002768-001			
79D	1S2768	98002768-001			

TAB-004

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
79E	1S2768	98002768-001			
79F	1S2768	98002768-001			
80AE	P1043	43C212092P1043			
80BE	P1043	43C212092P1043			
80CE	P1043	43C212092P1043			
80DE	P1043	43C212092P1043			
80EE	P1043	43C212092P1043			
80FE	P1043	43C212092P1043			
80GE	P9	43A114748P9			
80JE	P1043	43C212092P1043			
80LE	P1043	43C212092P1043			
80NE	P9	43A114748P9			
80QE	P1043	43C212092P1043			
80RE	RSOH	58020479-008			
80SE	P1043	43C212092P1043			
80UE	P9	43A114748P9			
80WE	P1043	43C212092P1043			
81G	1B3462	43C216462P1			
81H	1B3462	43C216462P1			
81J	1B3462	43C216462P1			
81K	4G4408	43C216408P1			
81L	1B-054	58002054-001			
81M	1C-057	58002057-001			
81N	1E-779	58002779-001			
81P	1B-713	58002713-001			
81Q	1B-714	58002714-001			
81R	4G4408	43C216408P1			
81S	1B-475	58002475-001			
81T	1B3600	58002600-001			
81U	1B3600	58002600-001			
81V	1B3600	58002600-001			
81W	1B3600	58002600-001			
81X	1B3600	58002600-001			
88AE	P1043	43C212092P1043			
88BE	P1043	43C212092P1043			
88CE	P1043	43C212092P1043			
88DE	P1043	43C212092P1043			
88EE	P1043	43C212092P1043			

TAB-004

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
88FE	P1043	43C212092P1043			
88GE	P9	43A114748P9			
88HE	P1243	43C212092P1243			
88JE	P1043	43C212092P1043			
88LE	P1043	43C212092P1043			
88NE	P9	43A114748P9			
88QE	P1043	43C212092P1043			
88SE	P1043	43C212092P1043			
88UE	P9	43A114748P9			
88WE	P1043	43C212092P1043			
90A	1S2768	98002768-001			
90B	1S2768	98002768-001			
90C	1S2768	98002768-001			
90D	1S2768	98002768-001			
90E	1S2768	98002768-001			
90F	1S2768	98002768-001			
90G	1B3462	43C216462P1			
90H	1B3462	43C216462P1			
90J	1B3462	43C216462P1			
90K	RN4D	43B216592P17			
90L	4G4408	43C216408P1			
90M	4G4408	43C216408P1			
90N	1B3600	58002600-001			
90P	1B3600	58002600-001			
90Q	1Q3488	58002488-001			
90R	1Q3488	58002488-001			
90S	1Q3488	58002488-001			
90T	1Q3488	58002488-001			
90U	1Q3488	58002488-001			
90V	1Q3488	58002488-001			
90W	1Q3488	58002488-001			
90X	1Q3488	58002488-001			
92YD	P16	43A114748P16			

58060530

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 001	002	003	004	005	DWG SH. NO. 1	2
A	LEVEL 1 ISSUE	83	01	26	J.M. Berg 1-21-83	A					A	
A1	Level 2 ENXS149		ND		G Dreuth	A1						
B	PHA0XS459	84	03	23	G Dreuth	B	B				B	
C	PHA0XS489	84	06	15	G Dreuth	OBSOLETE	C				C	
D	PHA0XS584	84	10	22	E Hicks		D	D			D	
E	PHA0XS650	85	APR	25	G Dreuth		OBSOLETE	E	E		E	E
F	PHA0NJ063	86	MAY	21	J. Williams			OBSOLETE	F	F	F	F
									OBSOLETE			

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY G.M.T. Agostino 82 Sep 8

APPROVED E. Schofield 1-19-83

TITLE: FW CIL WDAMP-1

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

SIZE	REVISION STATUS FOR	SHEET	REV
A	58060530	1/1	F

DIST. 37

BRUNING 44-141 40366

CE 300 A-3 (1-79)

Honeywell HONEYWELL INFORMATION SYSTEMS INC.		SPEC. NO. 58060530	SHEET 1/2	REV. F

COMPONENT INSTALLATION FOR WDAMP-1

TAB-001

LOCATION	TYPE	IDENT
09C	2R3689	58002689-001*
09E	2R3689	58002689-001*
09A	2R3689	58002689-001*
22A	2R3689	58002689-001*
22C	2R3689	58002689-001*

* All Tab-001 devices will be reidentified with programmed tab numbers prior to first customer shipment.

TAB-002

LOCATION	TYPE	IDENT
09A	2R3689	58002689-066
09C	2R3689	58002689-067
09E	2R3689	58002689-068
22A	2R3689	58002689-069
22C	2R3689	58002689-070

TAB-003

LOCATION	TYPE	IDENT
09A	2R3689	58002689-169
09C		-170
09E		-171
22A		-172
22C	2R3689	58002689-173

Honeywell HONEYWELL INFORMATION SYSTEMS	COMPONE INSTL LIST	SPEC.NO 58060530	SHEET 2F	REV F

PROM TAB NUMBER TO BOARD LOCATION REFERENCE.

PROM IDENTIFICATION NUMBER IS 58002689 :

		TAB NUMBER &STATUS							
		OBSO							
LOCATION	TYPE	-004	-005						
09A	2R3689	-220	-220						
09C		-221	-266						
09E		-222	-267						
22A		-223	-223						
22C	2R3689	-224	-268						

REV	AUTHORITY	DATE
C	PHAOXS624	84DEC13

SIGNAL NAME	PAGE
$A-REG•ØØØ	16.Ø
$A-REG•ØØ1	4.Ø
$A-REG•11Ø	24.Ø
$ANY-CLR•1ØØ	5.Ø
$B-REG•ØØØ	31.Ø
$B-REG•11Ø	27.Ø
$B-REG•111	4.Ø
$BR•ØØØ	35.Ø
$CLR-RDSEC•1ØØ	22.Ø
$CLR-WTSEC•1ØØ	2Ø.Ø
$CLRRBA•141	22.Ø
$CR•ØØØ	35.Ø
$DAU•Ø1Ø	11.Ø
$DAU•Ø11	11.Ø
$DAU•Ø12	11.Ø
$DAU•Ø14	11.Ø
$DAU•Ø16	1Ø.Ø
$DAU•Ø17	11.Ø
$DAU•Ø19	12.Ø
$DAU•Ø24	12.Ø
$DAU•Ø34	12.Ø
$DAU•Ø35	1Ø.Ø
$DAU•1ØØ	11.Ø
$DAU•1Ø1	11.Ø
$DAU•134	12.Ø
$DAU•135	12.Ø
$DAU•136	12.Ø
$DAU-TOT-BCL•Ø3Ø	6.Ø
$DAU-TOT-BCL•Ø31	6.Ø
$DAU-TOT-BCL•Ø32	7.Ø
$DAU-TOT-BCL•12Ø	7.Ø
$DAU-TOT-CLR•Ø1Ø	6.Ø
$DAU-TOT-CLR•Ø11	6.Ø
$DAU-TOT-CLR•Ø12	6.Ø
$DAU-TOT-CLR•Ø13	6.Ø
$DAU-TOT-CLR•1ØØ	5.Ø
$DECBFRFUL•ØØØ	36.Ø
$FRE-RUN•Ø1Ø	1Ø.Ø
$FRE-RUN•Ø3Ø	11.Ø
$FRE-RUN•Ø31	11.Ø
$FRE-RUN•Ø36	11.Ø
$FRE-RUN•Ø37	11.Ø
$FRE-RUN•Ø41	11.Ø
$FRE-RUN•Ø51	12.Ø
$FRE-RUN•1ØØ	1Ø.Ø
$FRE-RUN•12Ø	11.Ø
$FRE-RUN•13Ø	11.Ø
$FRE-RUN•151	11.Ø
$ID-TOTCLRØ•1ØØ	5.Ø
$IDI-TOT-CLR•Ø1Ø	6.Ø
$IDI-TOT-CLR•Ø11	6.Ø
$INCBFRFUL•ØØØ	35.Ø
$INCRSA•ØØØ	27.Ø
$INCWSA•ØØØ	24.Ø
$LD-WSEC16•ØØØ	3Ø.Ø
$LD-XFERCNT•ØØØ	35.Ø
$LDBFRFUL•ØØØ	35.Ø
$LDMD1•ØØØ	8.Ø
$LDMD2•ØØØ	8.Ø
$LDRALW•ØØØ	22.Ø
$LDRAUP•ØØØ	22.Ø
$LDRSEC•ØØØ	22.Ø
$LDWALW•ØØØ	2Ø.Ø
$LDWAUP•ØØØ	2Ø.Ø
$LDWSEC•ØØØ	2Ø.Ø

SIGNAL NAME	PAGE
$PART-BCLR•Ø3Ø	6.Ø
$PART-BCLR•Ø31	6.Ø
$PART-BCLR•Ø32	6.Ø
$PART-BCLR•Ø33	6.Ø
$PART-BCLR•12Ø	7.Ø
$PARTIAL-CLR•Ø1Ø	5.Ø
$PARTIAL-CLR•Ø11	5.Ø
$PARTIAL-CLR•Ø12	5.Ø
$RCARØ•ØØØ	21.Ø
$RCAR1•ØØØ	21.Ø
$RCAR1•ØØ1	4.Ø
$RCAR1•11Ø	22.Ø
$RCAR2•ØØØ	22.Ø
$RCAR22•ØØØ	22.Ø
$RCAR3•ØØØ	22.Ø
$RD•Ø2Ø	4.Ø
$RD•13Ø	47.Ø
$RDØ-UL-CK•ØØØ	37.Ø
$RD1-UL-CK•ØØØ	37.Ø
$READ-FIFOØ•1ØØ	37.Ø
$READ-FIFO1•1ØØ	37.Ø
$RSTBFRFUL•ØØØ	35.Ø
$RSTRQ•ØØØ	5.Ø
$RSTWR•ØØØ	5.Ø
$SB•ØØØ	39.Ø
$SB•11Ø	39.Ø
$SNAP-SHOT•ØØØ	37.Ø
$WCARØ•ØØØ	19.Ø
$WCAR1•ØØØ	19.Ø
$WCAR1•ØØ1	4.Ø
$WCAR1•11Ø	2Ø.Ø
$WCAR2•ØØØ	2Ø.Ø
$WCAR2•ØØ1	4.Ø
$WCAR22•ØØØ	21.Ø
$WCAR3•ØØØ	2Ø.Ø
$WE•ØØØ	18.Ø
$WR•Ø2Ø	4.Ø
$WR•13Ø	4.Ø
$WRT-FIFOØ•Ø2Ø	14.Ø
$WRT-FIFOØ•11Ø	14.Ø
$WRT-FIFO1•Ø2Ø	14.Ø
$WRT-FIFO1•11Ø	14.Ø
A-BREG-FUL•ØØØ	33.Ø
ACK-COR•ØØØ	18.Ø
ACK-COR•11Ø	17.Ø
ACT-WT-REGTRM•ØØØ	17.Ø
ACT-WT-REGTRM•11Ø	17.Ø
ALLOW-DB-ERR•1ØØ	1Ø.Ø
ANYCLR•1ØØ	4.Ø
APRTYERR•1ØØ	19.Ø
B-BUF-SW-DØ•1ØØ	15.Ø
B-BUF-SW-D1•1ØØ	15.Ø
B-BUF-SW-D2•1ØØ	16.Ø
B-BUF-SW-D3•1ØØ	16.Ø
B-BUF-SW-D4•1ØØ	16.Ø
B-BUF-SW-D5•1ØØ	16.Ø
B-BUF-SW-D6•1ØØ	15.Ø
B-BUF-SW-D7•1ØØ	15.Ø
B-BUF-SW-DP•1ØØ	15.Ø
B-PRTYER•1ØØ	34.Ø
B-REG-READY•ØØØ	46.Ø
B-REG-READY•11Ø	46.Ø
BADR-SEC16•1ØØ	28.Ø
BADRØØSEC8•1ØØ	28.Ø
BADRØ1SEC4•1ØØ	28.Ø

SIGNAL NAME	PAGE
BADRØ2SEC2•1ØØ	28.Ø
BADRØ3SEC1•1ØØ	28.Ø
BADRØ4•1ØØ	28.Ø
BADRØ5•1ØØ	28.Ø
BADRØ6•1ØØ	28.Ø
BADRØ7•1ØØ	28.Ø
BADRØ8•1ØØ	28.Ø
BADRØ9•1ØØ	28.Ø
BADR1Ø•1ØØ	28.Ø
BADR11•1ØØ	28.Ø
BADR12•1ØØ	28.Ø
BREG-ØØ•11Ø	33.Ø
BREG-Ø1•11Ø	33.Ø
BREG-Ø2•11Ø	33.Ø
BREG-Ø3•11Ø	33.Ø
BREG-Ø4•11Ø	33.Ø
BREG-Ø5•11Ø	33.Ø
BREG-Ø6•11Ø	34.Ø
BREG-Ø7•11Ø	34.Ø
BREG-P•11Ø	34.Ø
BUF-FULL•11Ø	36.Ø
BUFF-STB•13Ø	16.Ø
BYT-CNT-ONES•Ø1Ø	13.Ø
BYT-CNT-ONES•1ØØ	13.Ø
C-RADR-SEC16•1ØØ	31.Ø
C-RADRØØSEC8•1ØØ	22.Ø
C-RADRØ1SEC4•1ØØ	22.Ø
C-RADRØ2SEC2•1ØØ	22.Ø
C-RADRØ3SEC1•1ØØ	22.Ø
C-RADRØ4•1ØØ	21.Ø
C-RADRØ5•1ØØ	21.Ø
C-RADRØ6•1ØØ	21.Ø
C-RADRØ7•1ØØ	21.Ø
C-RADRØ8•1ØØ	21.Ø
C-RADRØ9•1ØØ	21.Ø
C-RADR1Ø•1ØØ	21.Ø
C-RADR11•1ØØ	21.Ø
C-RADR12•1ØØ	21.Ø
C-WADR-SEC16•1ØØ	31.Ø
C-WADRØØSEC8•1ØØ	2Ø.Ø
C-WADRØ1SEC4•1ØØ	2Ø.Ø
C-WADRØ2SEC2•1ØØ	2Ø.Ø
C-WADRØ3SEC1•1ØØ	2Ø.Ø
C-WADRØ4•1ØØ	2Ø.Ø
C-WADRØ5•1ØØ	19.Ø
C-WADRØ6•1ØØ	19.Ø
C-WADRØ7•1ØØ	19.Ø
C-WADRØ8•1ØØ	19.Ø
C-WADRØ9•1ØØ	19.Ø
C-WADR1Ø•1ØØ	19.Ø
C-WADR11•1ØØ	19.Ø
C-WADR12•1ØØ	19.Ø
C288SECTOR•ØØØ	23.Ø
C4294-5293S•ØØØ	23.Ø
C4XX-294SECTOR•ØØØ	23.Ø
C5ØØ-293SECTOR•ØØØ	23.Ø
C5Ø1EDAC•ØØØ	24.Ø
CARRY1•1ØØ	13.Ø
CARRY2•1ØØ	13.Ø
CCORR-MPWT•1ØØ	18.Ø
CFUL1•1ØØ	35.Ø
CFUL16•1ØØ	34.Ø
CFUL2•1ØØ	35.Ø
CFUL32•1ØØ	34.Ø
CFUL4•1ØØ	35.Ø

SIGNAL NAME	PAGE
CFUL8•1ØØ	35.Ø
CMD-LDMODE1•ØØØ	9.Ø
CMD-LDMODE2•ØØØ	9.Ø
CMD-WR-DCS•Ø4Ø	17.Ø
CMD-WR-DCS•12Ø	7.Ø
CMD-WR-DCS•13Ø	7.Ø
CMD-WRITE•Ø3Ø	35.Ø
CMD-WRITE•12Ø	35.Ø
CMD-WRITE•14Ø	35.Ø
CMDDAUCLR•ØØØ	9.Ø
CMDIFØCLR•ØØØ	9.Ø
CMDLDAREG•ØØØ	9.Ø
CMDLDAREG•11Ø	17.Ø
CMDLDBFRFUL•ØØØ	9.Ø
CMDLDBYT-LW•ØØØ	9.Ø
CMDLDBYT-LW•11Ø	13.Ø
CMDLDBYT-UP•ØØØ	9.Ø
CMDLDBYT-UP•11Ø	14.Ø
CMDLDRALW•ØØØ	9.Ø
CMDLDRAUP•ØØØ	9.Ø
CMDLDWALW•ØØØ	9.Ø
CMDLDWAUP•ØØØ	9.Ø
CMDLDXFRREG•ØØØ	9.Ø
CMDPARCLR•ØØØ	9.Ø
CMDRDBREG•ØØØ	9.Ø
CMDRDBREG•11Ø	32.Ø
CMDRSTDENA•ØØØ	9.Ø
CMDRSTDENA•11Ø	41.Ø
CMDRSTDENB•ØØØ	9.Ø
CMDRSTDENB•11Ø	41.Ø
CMDSETDEN•ØØØ	9.Ø
CMDSETDEN•11Ø	41.Ø
CMDSTPCLK•ØØØ	9.Ø
CMFW•1ØØ	2Ø.Ø
CMPWRT•ØØØ	14.Ø
CNT-SHRT-BLK•ØØØ	38.Ø
CNTØ•ØØØ	36.Ø
CORMODE•ØØØ	18.Ø
CR4XX-293SEC•ØØØ	27.Ø
CR5ØØ-292SEC•ØØØ	27.Ø
CRD-DEVICE•1ØØ	17.Ø
CSEL-DREG•Ø1Ø	14.Ø
CSEL-DREG•1ØØ	14.Ø
CSTOP•1ØØ	1Ø.Ø
CWB-SECADR•Ø1Ø	23.Ø
CWB-SECADR•Ø11	4.Ø
CWB-SECADR•1ØØ	23.Ø
D-4ØØCIR•ØØØ	18.Ø
D-4ØØCIR•11Ø	17.Ø
D-ANY-ERR•1ØØ	48.Ø
D-ANY-HARD-ERR•Ø1Ø	48.Ø
D-ANY-HARD-ERR•1ØØ	49.Ø
D-AORB-PER•ØØØ	49.Ø
D-AREG•1ØØ	18.Ø
D-COUNT•1ØØ	14.Ø
D-ED-P-ERR•Ø1Ø	49.Ø
D-ED-P-ERR•1ØØ	49.Ø

DISTRIBUTION CODE C12Ø-26

HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS CEO PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDASB
LOGIC -
PAGE CROSS REFERENCE

ASM REF 58Ø8887Ø-XØ4

DATA BASE NIODAU/HSB/WDASB
DFTG 84DEC13

SIZE	DWG NO	SH	REV
B	58Ø88874	1.Ø	C

58Ø88874

REV	AUTHORITY	DATE
C	PHAOXS624	84DEC13

SIGNAL NAME	PAGE
D-EN-COUNT•1ØØ	13.Ø
D-ER-IFØ•ØØØ	1Ø.Ø
D-ER-IF1•ØØØ	1Ø.Ø
D-HARD-ERR•1ØØ	48.Ø
D-HOLD-RADR•ØØØ	28.Ø
D-IF-ERR•Ø1Ø	48.Ø
D-IF-ERR•1ØØ	1Ø.Ø
D-INC-BFUL•ØØØ	13.Ø
D-INC-WTSEC•ØØØ	13.Ø
D-INCWTSEC•1ØØ	24.Ø
D-LAST-EDAC•11Ø	38.Ø
D-LSTDTA•1ØØ	37.Ø
D-MPBFR-AD•ØØØ	32.Ø
D-NEW-RD-SECT•ØØØ	31.Ø
D-RAD-P•1ØØ	47.Ø
D-RD-SETB•ØØØ	18.Ø
D-RDB-SECADR•Ø1Ø	27.Ø
D-RDB-SECADR•Ø11	4.Ø
D-RDB-SECADR•1ØØ	27.Ø
D-RDSEC-DLY•1ØØ	25.Ø
D-SELZEROES•1ØØ	39.Ø
D-SET-DAU-CLR•1ØØ	4.Ø
D-SET-PARCLR•1ØØ	4.Ø
D-SETIFØCLR•1ØØ	4.Ø
D-SOFT-ERR•1ØØ	48.Ø
D-SUB-CLK•ØØØ	11.Ø
D-SW-Ø•1ØØ	15.Ø
D-SW-1•1ØØ	15.Ø
D-SW-2•1ØØ	16.Ø
D-SW-3•1ØØ	16.Ø
D-SW-4•1ØØ	16.Ø
D-SW-5•1ØØ	16.Ø
D-SW-6•1ØØ	15.Ø
D-SW-7•1ØØ	15.Ø
D-SYSTEM-RD•ØØØ	32.Ø
D-SYSTEM-WT•ØØØ	32.Ø
D-WRITE•1ØØ	23.Ø
D-WRITE-RD•1ØØ	27.Ø
D-WRTDEVINH•Ø1Ø	32.Ø
D-WRTDEVINH•1ØØ	32.Ø
D-XFERSECTORS•ØØØ	32.Ø
D12Ø•1ØØ	36.Ø
D16-32-Ø•1ØØ	36.Ø
D1OR7SECS•ØØØ	36.Ø
D28ØOR288•ØØØ	24.Ø
D32Ø-CORR•ØØØ	13.Ø
D32Ø-CORR•11Ø	34.Ø
D32Ø-RD•ØØØ	35.Ø
D32ØRSECRST•1ØØ	26.Ø
D32ØWSECRST•1ØØ	25.Ø
D45X-CIR•ØØØ	37.Ø
D45XCOR•ØØØ	32.Ø
D45XCOR•11Ø	33.Ø
D48Ø•1ØØ	36.Ø
D4XX-5ØØ•ØØØ	38.Ø
D5ØØ4ØØ-RD•ØØØ	35.Ø
D5Ø1-RD•ØØØ	35.Ø
D5Ø1EDAC•ØØØ	25.Ø
D5Ø1RLASTSEC•ØØØ	26.Ø
D5Ø1RLASTSEC•1ØØ	26.Ø
D5Ø1RNLSTSEC•ØØØ	26.Ø
D5Ø1WLASTSEC•ØØØ	25.Ø
D5Ø1WLASTSEC•1ØØ	25.Ø
D5Ø1WNLSTSEC•ØØØ	25.Ø
D5THRDSEC•1ØØ	26.Ø

SIGNAL NAME	PAGE
D5THWTSEC•1ØØ	25.Ø
DBRDØ-PRES•1ØØ	14.Ø
DBRDØ-PRES1•1ØØ	37.Ø
DBRD1-PRES•1ØØ	14.Ø
DBRD1-PRES1•1ØØ	37.Ø
DBREG-ACK•1ØØ	18.Ø
DBREG-ACK•11Ø	31.Ø
DBUF-RDMODE•1ØØ	32.Ø
DCIR-MODE•Ø1Ø	14.Ø
DCK4XXEDAC•ØØØ	18.Ø
DCOR-MODE•Ø1Ø	14.Ø
DCORACK•ØØØ	32.Ø
DCORR-PAD•1ØØ	34.Ø
DDEN-ØØ-Ø5Ø•1ØØ	4Ø.Ø
DDEN-Ø1-Ø5Ø•1ØØ	4Ø.Ø
DDEN-Ø2-Ø5Ø•1ØØ	39.Ø
DDEN-Ø3-Ø5Ø•1ØØ	39.Ø
DDEN-Ø4-Ø5Ø•1ØØ	4Ø.Ø
DDEN-Ø5-Ø5Ø•1ØØ	4Ø.Ø
DDEN-Ø6-Ø5Ø•1ØØ	4Ø.Ø
DDEN-Ø7-Ø5Ø•1ØØ	4Ø.Ø
DDEN-Ø8-Ø5Ø•1ØØ	4Ø.Ø
DDEN-Ø9-Ø5Ø•1ØØ	4Ø.Ø
DDEN-1Ø-Ø5Ø•1ØØ	4Ø.Ø
DDEN-11-Ø5Ø•1ØØ	4Ø.Ø
DDEN-12-Ø5Ø•1ØØ	4Ø.Ø
DDEN-13-Ø5Ø•1ØØ	4Ø.Ø
DDEN-14-Ø5Ø•1ØØ	41.Ø
DDEN-15-Ø5Ø•1ØØ	41.Ø
DEN45XCOR•1ØØ	33.Ø
DEV-4XX•Ø3Ø	23.Ø
DEV-4XX•11Ø	7.Ø
DEV-4XX•12Ø	7.Ø
DEV-4XX-5ØØ•12Ø	7.Ø
DEV-4XX-5ØØ•13Ø	7.Ø
DEV-5ØØ•1ØØ	24.Ø
DEV-5Ø1•Ø4Ø	17.Ø
DEV-5Ø1•12Ø	7.Ø
DEV-5Ø1•13Ø	7.Ø
DEV-5Ø1-32Ø•Ø4Ø	33.Ø
DEV-5Ø1-32Ø•13Ø	34.Ø
DEV4XX5Ø1•1ØØ	32.Ø
DINCRSA•1ØØ	27.Ø
DLAST-DTA•ØØØ	37.Ø
DLDBREG•1ØØ	33.Ø
DMPADR-11•1ØØ	7.Ø
DMPADR-12•1ØØ	7.Ø
DMPADR-13•1ØØ	7.Ø
DMPADR-14•1ØØ	7.Ø
DMPADR-15•1ØØ	7.Ø
DMPADR11•Ø2Ø	1Ø.Ø
DMPADR11•11Ø	7.Ø
DMPADR12•Ø2Ø	8.Ø
DMPADR12•11Ø	7.Ø
DMPADR13•Ø2Ø	1Ø.Ø
DMPADR13•11Ø	7.Ø
DMPADR14•Ø2Ø	46.Ø
DMPADR14•11Ø	7.Ø
DMPADR15•Ø2Ø	46.Ø
DMPADR15•11Ø	7.Ø
DMPDTA-Ø•1ØØ	7.Ø
DMPDTA-1•1ØØ	7.Ø
DMPDTA-2•1ØØ	7.Ø
DMPDTA-3•1ØØ	7.Ø
DMPDTA-4•1ØØ	7.Ø

SIGNAL NAME	PAGE
DMPDTA-5•1ØØ	7.Ø
DMPDTA-6•1ØØ	7.Ø
DMPDTA-7•1ØØ	7.Ø
DMPDTA-P•1ØØ	7.Ø
DMPDTAØ•11Ø	7.Ø
DMPDTAØZ•1ØØ	39.Ø
DMPDTA1•11Ø	7.Ø
DMPDTA1Z•1ØØ	39.Ø
DMPDTA2•11Ø	7.Ø
DMPDTA2Z•1ØØ	39.Ø
DMPDTA3•11Ø	7.Ø
DMPDTA3I•1ØØ	21.Ø
DMPDTA3Z•1ØØ	39.Ø
DMPDTA4•11Ø	7.Ø
DMPDTA4Z•1ØØ	39.Ø
DMPDTA5•11Ø	7.Ø
DMPDTA5Z•1ØØ	39.Ø
DMPDTA6•11Ø	7.Ø
DMPDTA6Z•1ØØ	39.Ø
DMPDTA7•11Ø	7.Ø
DMPDTA7Z•1ØØ	39.Ø
DMPDTAP•11Ø	7.Ø
DMPSELDTAØ•1ØØ	41.Ø
DMPSELDTAØ•1ØØ	4Ø.Ø
DMPSELDTA1•1ØØ	4Ø.Ø
DMPSELDTA1Ø•1ØØ	42.Ø
DMPSELDTA11•1ØØ	42.Ø
DMPSELDTA12•1ØØ	42.Ø
DMPSELDTA13•1ØØ	42.Ø
DMPSELDTA14•1ØØ	42.Ø
DMPSELDTA15•1ØØ	42.Ø
DMPSELDTA2•1ØØ	4Ø.Ø
DMPSELDTA3•1ØØ	41.Ø
DMPSELDTA3•1ØØ	4Ø.Ø
DMPSELDTA4•1ØØ	4Ø.Ø
DMPSELDTA5•1ØØ	4Ø.Ø
DMPSELDTA6•1ØØ	4Ø.Ø
DMPSELDTA7•1ØØ	4Ø.Ø
DMPSELDTA8•1ØØ	42.Ø
DMPSELDTA9•1ØØ	42.Ø
DPAD-SETBFUL•ØØØ	33.Ø
DRAR•ØØØ	18.Ø
DRAR4ØØCK•ØØØ	32.Ø
DRAR4ØØCK•11Ø	33.Ø
DRD-SEC•Ø1Ø	26.Ø
DRD-SEC•1ØØ	27.Ø
DREAD-DEV•1ØØ	35.Ø
DREAD-DEVICE•ØØØ	35.Ø
DREG-Ø•11Ø	15.Ø
DREG-1•11Ø	15.Ø
DREG-2•11Ø	16.Ø
DREG-3•11Ø	16.Ø
DREG-4•11Ø	16.Ø
DREG-5•11Ø	16.Ø
DREG-6•11Ø	15.Ø
DREG-7•11Ø	15.Ø
DREG-P•11Ø	15.Ø
DREGCIR•1ØØ	17.Ø
DRESETØ•ØØØ	6.Ø
DRESET1•ØØØ	6.Ø
DSEL-B8•Ø2Ø	7.Ø
DSEL-B8•11Ø	4.Ø
DSEL-B8•13Ø	1Ø.Ø
DSET-287•1ØØ	38.Ø
DSET-BFUL•1ØØ	32.Ø

SIGNAL NAME	PAGE
DSET-FSNAP•1ØØ	36.Ø
DSET-PERR•ØØØ	47.Ø
DSET-R32ØRST•1ØØ	26.Ø
DSET-W32ØRST•1ØØ	24.Ø
DSETLSTEDAC•1ØØ	38.Ø
DSETSECDLY•1ØØ	27.Ø
DSETSTP•1ØØ	12.Ø
DSHORT-BLK•1ØØ	38.Ø
DSYSRDLSTSEC•1ØØ	26.Ø
DSYSWLASTSEC•1ØØ	25.Ø
DTABUS-PRTER•ØØØ	8.Ø
DUMPBFR•ØØØ	32.Ø
DUMPBFR•11Ø	32.Ø
DW288-SECTOR•ØØØ	27.Ø
DWRT-REG-FUL•13Ø	14.Ø
DWRTSECSECS•ØØØ	35.Ø
DWT-ACT-SEC•ØØØ	34.Ø
DWT-SEC-TERM•ØØØ	25.Ø
DWT-SEC-TERM•11Ø	25.Ø
EN-286RDSEC•1ØØ	26.Ø
EN-BFUL-DECR•1ØØ	36.Ø
EN-CLK•1ØØ	1Ø.Ø
EN-FORMAT•ØØØ	12.Ø
EN-HI-OSC•ØØØ	1Ø.Ø
EN-HI-OSC•11Ø	11.Ø
EN-LAST-DATA•1ØØ	37.Ø
EN-LAST-EDAC•1ØØ	37.Ø
EN-RAR•1ØØ	38.Ø
EN-SW1•ØØØ	47.Ø
EN-SW1•11Ø	47.Ø
EN-SW2•ØØØ	46.Ø
EN-SW3•ØØØ	48.Ø
EN-WRT-REG-ACK•1ØØ	17.Ø
ENAB-CLK•1ØØ	11.Ø
ENB-WTSEC•Ø1Ø	24.Ø
ENB-WTSEC•1ØØ	24.Ø
ENBDCD•ØØØ	27.Ø
ENBWTADR•ØØØ	28.Ø
F-EDAC-ERROR•Ø2Ø	48.Ø
F-EDAC-ERROR•11Ø	48.Ø
F-RD-SEC-DLY•1ØØ	24.Ø
F-RD-SEC-DLY•1Ø1	4.Ø
F32ØRSECRST•ØØØ	27.Ø
F32ØRSECRST•1ØØ	27.Ø
F32ØWSECRST•ØØØ	24.Ø
F32ØWSECRST•1ØØ	24.Ø
FAREG-FUL•ØØØ	16.Ø
FAREG-FUL•1ØØ	16.Ø
FAREG-PRTERR•ØØØ	19.Ø
FAREG-PRTERR•1ØØ	19.Ø
FB-REG-FUL•ØØØ	31.Ø
FB-REG-FUL•Ø1Ø	33.Ø
FB-REG-FUL•1ØØ	31.Ø
FB-REG-FUL•11Ø	32.Ø
FB-REG-TRM•111	13.Ø
FBD-ERR•Ø2Ø	49.Ø
FBD-ERR•11Ø	49.Ø

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LOC CEO HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDASB LOGIC - PAGE CROSS REFERENCE

ASM REF 58Ø8887Ø-XØ4 | DATA BASE NIODAU/HSB/WDASB | DR DFTG 84DEC13 | SIZE B | DWG NO 58Ø88874 | SH 1.1 | REV C

58Ø88874

REV	AUTHORITY	DATE
C	PHAOXS624	84DEC13

SIGNAL NAME	PAGE
FBREG-PER•000	34.0
FBREG-PER•100	34.0
FCMD-WRITE•100	12.0
FCMD-WRITE•110	12.0
FCOR-ACK•000	17.0
FCOR-ACK•100	17.0
FCOR-PAD-INH•000	18.0
FCREG-ACK•110	18.0
FCREG-FULL•110	18.0
FDBUS-PRTER•000	9.0
FDBUS-PRTER•100	9.0
FDEN-00•100	42.0
FDEN-01•100	42.0
FDEN-02•100	42.0
FDEN-03•100	42.0
FDEN-04•100	43.0
FDEN-05•100	43.0
FDEN-06•100	43.0
FDEN-07•100	43.0
FDEN-08•100	43.0
FDEN-09•100	43.0
FDEN-10•100	43.0
FDEN-11•100	43.0
FDEN-12•100	44.0
FDEN-13•100	44.0
FDEN-14•100	44.0
FDEN-15•100	44.0
FINCRSECADR•000	26.0
FINCRSECADR•100	26.0
FINCWSECADR•000	24.0
FINCWSECADR•100	24.0
FINT-BREG-ACK•100	38.0
FIPC-RESET•000	5.0
FIPC-RESET•010	31.0
FIRSA•000	6.0
FIRSA•100	6.0
FKRL2-BADR•000	6.0
FKRL2-BADR•100	6.0
FLAST-EDAC•000	37.0
FLD-ZEROES•000	6.0
FLD-ZEROES•100	6.0
FR-DAU-CLR•000	5.0
FR-DAU-CLR•100	5.0
FR-IDIOCLR•000	5.0
FR-IDIOCLR•100	5.0
FR-PAR-CLR•000	5.0
FR-PAR-CLR•100	5.0
FRD•100	5.0
FRD-KRL1•000	5.0
FRD-KRL1•110	5.0
FRD-SECTOR•000	26.0
FRD-SECTOR•100	26.0
FROB-SECADLY•100	26.0
FREGS-PRTYER•000	47.0
FREGS-PRTYER•100	47.0
FS-SYNC•000	39.0
FSECREQ•010	17.0
FSECREQ•030	31.0
FSECREQ•120	17.0
FSECREQ•130	12.0
FSHORT-BLK•000	36.0
FSNAP-DLY•100	37.0
FSNAP-SHOT•000	36.0
FSNAP-SHOT•100	36.0
FSNAPSEC1•100	37.0

SIGNAL NAME	PAGE
FSNAPSEC16•100	37.0
FSNAPSEC2•100	37.0
FSNAPSEC4•100	37.0
FSNAPSEC8•010	36.0
FSNAPSEC8•100	37.0
FSTEP•000	12.0
FSTEP•100	12.0
FSTOP•000	12.0
FSTOP•110	12.0
FWR•100	4.0
FWRCMD•100	20.0
FWRT-KRL1•000	5.0
FWRT-KRL1•100	5.0
FWRT-KRL1•110	5.0
FWRT-KRL2•000	5.0
FWRT-KRL2•100	5.0
FWRT-REG-ACK•010	17.0
FWRT-REG-ACK•100	17.0
FWT-SECTOR•100	24.0
FXFR0•000	34.0
FXFR0•001	4.0
GEN-RESET•000	4.0
GND-00M-08	45.0
GND-00N-08	45.0
GND-09F-08	40.0
GND-09S-08	34.0
GND-18K-08	45.0
GND-18N-08	19.0
GND-18N-08	9.0
GND-18W-08	39.0
GND-27E-08	48.0
GND-27H-08	15.0
GND-27J-08	16.0
GND-27K-08	16.0
GND-27L-08	16.0
GND-27U-08	36.0
GND-27W-08	39.0
GND-27X-08	39.0
GND-36J-08	15.0
GND-36K-08	15.0
GND-36M-08	15.0
GND-36R-00	41.0
GND-36T-08	31.0
GND-45C-07	47.0
GND-45D-08	47.0
GND-45F-00	41.0
GND-45K-08	15.0
GND-45M-08	16.0
GND-54K-08	15.0
GND-54N-08	31.0
GND-54P-08	8.0
GND-54S-08	9.0
GND-63F-08	12.0
GND-63K-08	47.0
GND-63K-08	34.0
GND-63M-08	5.0
GND-63M-08	4.0
GND-63N-08	19.0
GND-63Q-07	21.0
GND-72A-00	7.0
GND-72L-08	31.0
GND-72N-08	33.0
GND-72R-08	21.0
GND-72V-08	20.0
GND-81M-08	34.0

SIGNAL NAME	PAGE
GND-81N-08	33.0
GND-81P-08	7.0
GND-81Q-08	7.0
GND-81R-08	7.0
GND-81U-08	28.0
GND-81V-08	28.0
GND-81W-08	28.0
GND-81X-08	28.0
GND-90P-10	30.0
GND-90Q-10	30.0
GND-90R-10	30.0
GND-90S-10	30.0
GND-90T-10	29.0
GND-90U-10	29.0
GND-90V-10	29.0
GND-90W-10	29.0
GND-90X-10	28.0
INH-ACK•100	18.0
INH-COUNT•000	36.0
IPC-RESET•100	6.0
IPC-RESET•110	7.0
LAST-DATA•110	38.0
LD-BYT-CNT-LW•000	13.0
LD-BYT-CNT-UP•000	14.0
LD-DENA•000	41.0
LD-DENB•000	41.0
LD-MODE1•100	7.0
LD-MODE2•100	8.0
LD-ZEROES•100	20.0
LDBFRFUL•100	36.0
LDLW•100	22.0
LDRALW•100	22.0
LDWALW•100	20.0
LDWAUP•100	20.0
LDWSEC•100	20.0
LDXFRREQ•100	36.0
LOGIC1•100	4.0
LOGIC1•101	21.0
LST-DTA•000	37.0
MODE-RAR•110	31.0
MODE-RAR•120	31.0
MODE1-DEC1•100	8.0
MODE1-DEC2•100	8.0
MODE1-DEC4•100	8.0
MP-ADR-CMP•010	49.0
MP-ADR-CMP•120	49.0
MP-LD-WSEC•100	20.0
MPLDAREG•000	17.0
MPLDLW•100	22.0
MPLSB•100	22.0
MPRD•120	4.0
MPWR•120	4.0
NCT501-715SEC•100	37.0
NORMAL-LOAD•100	21.0
OSC-HIGH•100	10.0
OSC-NORMAL•100	11.0
PLUSRD-DEV•100	23.0
POMC•100	31.0
POWER-CONF•110	31.0
R-AREG-0•100	19.0
R-AREG-1•100	19.0
R-AREG-2•100	19.0
R-AREG-3•100	19.0
R-AREG-4•100	19.0
R-AREG-5•100	19.0

SIGNAL NAME	PAGE
R-AREG-6•100	19.0
R-AREG-7•100	19.0
R-AREG-P•100	19.0
R-BIT0•100	28.0
R-BIT1•100	29.0
R-BIT2•100	29.0
R-BIT3•100	29.0
R-BIT4•100	29.0
R-BIT5•100	30.0
R-BIT6•100	30.0
R-BIT7•100	30.0
R-BITP•100	30.0
R287•100	38.0
R320BFREQ•000	9.0
R320BFREQ•000	25.0
R320BFREQ•000	26.0
R4293-5292•100	27.0
R512BFREQ•000	9.0
R512BFREQ•000	26.0
R512BFREQ•000	25.0
R64BFREQ•000	9.0
RABS-READ•010	14.0
RABS-READ•011	10.0
RABS-READ•100	9.0
RABS-READ-WRP•100	10.0
RABS-WRT•100	10.0
RABS-WRT-WRP•010	8.0
RABS-WRT-WRP•100	10.0
RABS-WRT-WRP-ED•011	8.0
RABS-WRT-WRP-ED•100	8.0
RABSOLUTE•000	9.0
RADRCMPSTP•100	8.0
RAR-NT-ABS•010	13.0
RAR-NT-ABS•100	38.0
RBUF-RDOUT-0•100	47.0
RBUF-RDOUT-1•100	47.0
RBUF-RDOUT-2•100	47.0
RBUF-RDOUT-3•100	47.0
RBUF-RDOUT-4•100	47.0
RBUF-RDOUT-5•100	47.0
RBUF-RDOUT-6•100	47.0
RBUF-RDOUT-7•100	47.0
RBUF-RDOUT-P•000	47.0
RBUF-RDOUT-P•100	47.0
RC-REG-00•110	15.0
RC-REG-01•110	15.0
RC-REG-02•110	16.0
RC-REG-03•110	16.0
RC-REG-04•110	16.0
RC-REG-05•110	16.0
RC-REG-06•110	15.0
RC-REG-07•110	15.0
RC-REG-P•110	15.0
RCIR-MODE•100	31.0
RCIRCORR•010	23.0
RCIRCORR•100	23.0
RCIRMODE•100	8.0

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TITLE LOGIC DIAGRAM- WDASB LOGIC - PAGE CROSS REFERENCE

ASM REF 58088870-X04 | DATA BASE NIODAU/HSB/WDASB | DFTG 84DEC13 | SIZE B | DWG NO 58088874 | SH 1.2 | REV C

58088874

REV	AUTHORITY	DATE
C	PHAOXS624	84DEC13

SIGNAL NAME	PAGE
RCOR-MODE•1ØØ	31.Ø
RCORMODE•1ØØ	8.Ø
RD-BITØ•1ØØ	33.Ø
RD-BIT1•1ØØ	33.Ø
RD-BIT2•1ØØ	33.Ø
RD-BIT3•1ØØ	33.Ø
RD-BIT4•1ØØ	33.Ø
RD-BIT5•1ØØ	33.Ø
RD-BIT6•1ØØ	33.Ø
RD-BIT7•1ØØ	33.Ø
RD-BITP•1ØØ	33.Ø
RD-BITP•1Ø1	33.Ø
RD-DEV4ØØ•ØØØ	14.Ø
RD-PLUS•ØØØ	26.Ø
RD-SECABS•1ØØ	32.Ø
RD-WTSEC-INC•ØØØ	24.Ø
RD4293-5292•ØØØ	27.Ø
RDATA-Ø•11Ø	15.Ø
RDATA-1•11Ø	15.Ø
RDATA-2•11Ø	16.Ø
RDATA-3•11Ø	16.Ø
RDATA-4•11Ø	16.Ø
RDATA-5•11Ø	16.Ø
RDATA-6•11Ø	15.Ø
RDATA-7•11Ø	15.Ø
RDATA-P•11Ø	15.Ø
RDC-286•11Ø	27.Ø
RDC-292•11Ø	26.Ø
RDC-293•11Ø	27.Ø
RDCD-28Ø•ØØØ	25.Ø
RDCD-286•ØØØ	26.Ø
RDCD-288•ØØØ	25.Ø
RDCD-292•ØØØ	26.Ø
RDCD-293•ØØØ	26.Ø
READ-OUT-Ø•1ØØ	45.Ø
READ-OUT-Ø•1ØØ	48.Ø
READ-OUT-Ø•1ØØ	44.Ø
READ-OUT-1•1ØØ	44.Ø
READ-OUT-1•1ØØ	45.Ø
READ-OUT-1•1ØØ	48.Ø
READ-OUT-2•1ØØ	45.Ø
READ-OUT-2•1ØØ	48.Ø
READ-OUT-2•1ØØ	44.Ø
READ-OUT-3•1ØØ	48.Ø
READ-OUT-3•1ØØ	44.Ø
READ-OUT-3•1ØØ	45.Ø
READ-OUT-4•1ØØ	48.Ø
READ-OUT-4•1ØØ	46.Ø
READ-OUT-4•1ØØ	44.Ø
READ-OUT-5•1ØØ	48.Ø
READ-OUT-5•1ØØ	46.Ø
READ-OUT-5•1ØØ	44.Ø
READ-OUT-6•1ØØ	46.Ø
READ-OUT-6•1ØØ	45.Ø
READ-OUT-6•1ØØ	48.Ø
READ-OUT-7•1ØØ	48.Ø
READ-OUT-7•1ØØ	46.Ø
READ-OUT-7•1ØØ	45.Ø
READ-OUT-P•1ØØ	45.Ø
REDAC-PLUS•Ø1Ø	14.Ø
REDAC-PLUS•1ØØ	8.Ø
RES-INH1•1ØØ	18.Ø
RES-INH2•1ØØ	18.Ø
RHER-STOP•1ØØ	8.Ø
RMODE1-PRTY•1ØØ	8.Ø

SIGNAL NAME	PAGE
RMPMODE•Ø1Ø	33.Ø
RMPMODE•1ØØ	8.Ø
RPREP-SB•Ø1Ø	14.Ø
RPREP-SB•1ØØ	8.Ø
RSB-REG-Ø•1ØØ	38.Ø
RSB-REG-1•1ØØ	38.Ø
RSB-REG-2•1ØØ	38.Ø
RSB-REG-3•1ØØ	38.Ø
RSB-REG-4•1ØØ	38.Ø
RSB-REG-5•1ØØ	38.Ø
RSB-REG-6•1ØØ	39.Ø
RSB-REG-7•1ØØ	39.Ø
RSB-REG-P•1ØØ	39.Ø
RSER-STOP•1ØØ	8.Ø
RSHORT-BLK•1ØØ	37.Ø
RSPARE3•1ØØ	8.Ø
RST-BFUL•1ØØ	31.Ø
RST-BFUL•1Ø1	4.Ø
RST-RDSEC•Ø1Ø	25.Ø
RSTOP•1ØØ	8.Ø
RUNSTEP•1ØØ	11.Ø
RWRAP-MODE•ØØØ	9.Ø
RWRAP-MODE•11Ø	1Ø.Ø
RWRTRDSEC•Ø1Ø	1Ø.Ø
RWRTRDSEC•1ØØ	8.Ø
S-SYNC•1ØØ	39.Ø
SEC-CNT1•1ØØ	34.Ø
SEC-CNT2•Ø1Ø	35.Ø
SEC-CNT2•1ØØ	34.Ø
SEC-CNT4•Ø1Ø	35.Ø
SEC-CNT4•1ØØ	34.Ø
SEC-CNT8•Ø1Ø	35.Ø
SEC-CNT8•1ØØ	34.Ø
SEL1-BUF-SW1•1ØØ	15.Ø
SEL1-BUF-SWI•1Ø1	4.Ø
SEL2-BUF-SW2•1ØØ	15.Ø
SEL4-BUF-SW4•1ØØ	15.Ø
SELDTA•ØØØ	41.Ø
SELDTAB•ØØØ	41.Ø
SEQ-ERR•12Ø	34.Ø
SEQ-ERR•13Ø	34.Ø
SET-DEN-ØØ•1ØØ	4Ø.Ø
SET-DEN-Ø1•1ØØ	4Ø.Ø
SET-DEN-Ø2•1ØØ	39.Ø
SET-DEN-Ø3•1ØØ	39.Ø
SET-DEN-Ø4•1ØØ	4Ø.Ø
SET-DEN-Ø5•1ØØ	4Ø.Ø
SET-DEN-Ø6•1ØØ	4Ø.Ø
SET-DEN-Ø7•1ØØ	4Ø.Ø
SET-DEN-Ø8•1ØØ	41.Ø
SET-DEN-Ø9•1ØØ	41.Ø
SET-DEN-1Ø•1ØØ	41.Ø
SET-DEN-11•1ØØ	41.Ø
SET-DEN-12•1ØØ	41.Ø
SET-DEN-13•1ØØ	41.Ø
SET-DEN-14•1ØØ	42.Ø
SET-DEN-15•1ØØ	42.Ø
SET-PERR•1ØØ	47.Ø
SETDBPRTY•1ØØ	9.Ø
SETXFR•1ØØ	36.Ø
SHORT-BLK•11Ø	38.Ø
STAT-ERR•Ø2Ø	48.Ø
STAT-ERR•11Ø	48.Ø
STOP-CLK•Ø1Ø	48.Ø
STOP-CLK•12Ø	49.Ø

SIGNAL NAME	PAGE
STOP-CLK•121	48.Ø
SWAP-8THSEC•1ØØ	21.Ø
SYNC-BYTE•Ø3Ø	18.Ø
SYNC-BYTE•12Ø	18.Ø
SYNC-BYTE•14Ø	17.Ø
SYNCIPCRST•1ØØ	6.Ø
TD-32Ø•1ØØ	9.Ø
TD-32ØWD•ØØØ	9.Ø
TD-5Ø1•1ØØ	18.Ø
TD-5Ø1•1Ø1	17.Ø
TRM-SHRT-BLK•ØØØ	38.Ø
UP•1ØØ	9.Ø
UPDENS•1ØØ	12.Ø
W286•1ØØ	23.Ø
WD4294-5293•1ØØ	23.Ø
WDCD-28Ø•ØØØ	22.Ø
WDCD-286•ØØØ	23.Ø
WDCD-286•11Ø	23.Ø
WDCD-288•ØØØ	22.Ø
WDCD-292•ØØØ	23.Ø
WDCD-292•11Ø	23.Ø
WDCD-293•ØØØ	23.Ø
WDCD-293•11Ø	23.Ø
WT-SECABS•ØØØ	14.Ø
WT-SECABS•11Ø	16.Ø
WT-WTSEC-INC•ØØØ	24.Ø
XFR1•ØØØ	36.Ø

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TITLE LOGIC DIAGRAM- WDASB LOGIC - PAGE CROSS REFERENCE

ASM REF 58Ø8887Ø-XØ4 | DATA BASE NIODAU/HSB/WDASBD | DR DFTG 84DEC13 | SIZE B | DWG NO 58Ø88874 | SH 1.3 | REV C

I/O PIN		PAGE	SIGNAL NAME
LDØØ	O	4.Ø	$WCAR1•ØØ1
LDØ2	O	4.Ø	D-RDB-SECADR•Ø11
LDØ3	O	4.Ø	FXFRØ•ØØ1
LDØ4	O	4.Ø	CWB-SECADR•Ø11
LDØ7	O	4.Ø	$WCAR2•ØØ1
LD14	O	4.Ø	$RCAR1•ØØ1
RAØØ	O	4.Ø	$B-REG•111
RAØ5	O	4.Ø	$A-REG•ØØ1
RAØ7	O	4.Ø	RST-BFUL•1Ø1
RAØ9	O	4.Ø	SEL1-BUF-SWI•1Ø1
RA1Ø	O	4.Ø	F-RD-SEC-DLY•1Ø1
WAØØ	I	15.Ø	RDATA-Ø•11Ø
WAØ2	I	15.Ø	RDATA-1•11Ø
WAØ3	I	16.Ø	RDATA-2•11Ø
WAØ6	I	16.Ø	RDATA-5•11Ø
WAØ7	I	15.Ø	RDATA-6•11Ø
WAØ8	I	15.Ø	RDATA-7•11Ø
WAØ9	I	15.Ø	RDATA-P•11Ø
WA1Ø	I	14.Ø	$WRT-FIFOØ•11Ø
WA12	I	14.Ø	$WRT-FIFO1•11Ø
WA13	I	6.Ø	DRESETØ•ØØØ
WA14	I	6.Ø	DRESET1•ØØØ
WA15	I	14.Ø	DBRDØ-PRES•1ØØ
WA16	I	14.Ø	DBRD1-PRES•1ØØ
WA17	O	1Ø.Ø	$DAU•Ø16
WA18	I	17.Ø	ACT-WT-REGTRM•ØØØ
WA19	I	1Ø.Ø	EN-HI-OSC•ØØØ
WA2Ø	I	16.Ø	RDATA-3•11Ø
WBØØ	I	15.Ø	RC-REG-ØØ•11Ø
WBØ1	I	15.Ø	RC-REG-Ø1•11Ø
WBØ2	I	16.Ø	RC-REG-Ø2•11Ø
WBØ3	I	16.Ø	RC-REG-Ø3•11Ø
WBØ4	I	16.Ø	RC-REG-Ø4•11Ø
WBØ5	I	16.Ø	RC-REG-Ø5•11Ø
WBØ6	I	15.Ø	RC-REG-Ø6•11Ø
WBØ7	I	15.Ø	RC-REG-Ø7•11Ø
WBØ8	I	15.Ø	RC-REG-P•11Ø
WBØ9	O	11.Ø	$DAU•Ø14
WB1Ø	O	11.Ø	$FRE-RUN•Ø3Ø
WB12	O	13.Ø	FB-REG-TRM•111
WB13	I	11.Ø	$FRE-RUN•Ø31
WB14	O	25.Ø	RST-RDSEC•Ø1Ø
WB15	O	25.Ø	DWT-SEC-TERM•11Ø
WB16	I	12.Ø	$DAU•Ø19
WB17	I	16.Ø	RDATA-4•11Ø
WB18	O	8.Ø	RABS-WRT-WRP-ED•Ø11
WB19	O	48.Ø	STOP-CLK•121
WCØØ	O	47.Ø	RBUF-RDOUT-Ø•1ØØ
WCØ1	O	47.Ø	RBUF-RDOUT-1•1ØØ
WCØ2	O	47.Ø	RBUF-RDOUT-2•1ØØ
WCØ3	O	47.Ø	RBUF-RDOUT-3•1ØØ
WCØ4	O	47.Ø	RBUF-RDOUT-4•1ØØ
WCØ5	O	47.Ø	RBUF-RDOUT-5•1ØØ
WCØ6	O	47.Ø	RBUF-RDOUT-6•1ØØ
WCØ7	O	47.Ø	RBUF-RDOUT-7•1ØØ
WCØ8	O	47.Ø	RBUF-RDOUT-P•1ØØ
WCØ9	O	6.Ø	$DAU-TOT-CLR•Ø13
WC13	I	4Ø.Ø	DDEN-ØØ-ØSØ•1ØØ
WC14	I	4Ø.Ø	DDEN-Ø1-ØSØ•1ØØ
WC15	I	39.Ø	DDEN-Ø2-ØSØ•1ØØ
WC16	I	39.Ø	DDEN-Ø3-ØSØ•1ØØ
WC17	I	4Ø.Ø	DDEN-Ø4-ØSØ•1ØØ
WC18	I	4Ø.Ø	DDEN-Ø5-ØSØ•1ØØ
WC19	I	4Ø.Ø	DDEN-Ø6-ØSØ•1ØØ
WC2Ø	I	4Ø.Ø	DDEN-Ø7-ØSØ•1ØØ

I/O PIN		PAGE	SIGNAL NAME
WDØ1	O	11.Ø	$DAU•Ø17
WDØ2	O	33.Ø	BREG-ØØ•11Ø
WDØ3	O	33.Ø	BREG-Ø1•11Ø
WDØ4	O	33.Ø	BREG-Ø2•11Ø
WDØ5	O	33.Ø	BREG-Ø3•11Ø
WDØ6	O	33.Ø	BREG-Ø4•11Ø
WDØ7	O	33.Ø	BREG-Ø5•11Ø
WDØ8	O	34.Ø	BREG-Ø6•11Ø
WDØ9	O	34.Ø	BREG-Ø7•11Ø
WD1Ø	O	34.Ø	BREG-P•11Ø
WD12	I	37.Ø	DBRDØ-PRES1•1ØØ
WD13	I	37.Ø	$READ-FIFOØ•1ØØ
WD14	I	37.Ø	DBRD1-PRES1•1ØØ
WD15	I	37.Ø	$READ-FIFO1•1ØØ
WD16	I	49.Ø	FBD-ERR•11Ø
WD17	I	49.Ø	MP-ADR-CMP•Ø1Ø
WD18	O	48.Ø	D-ANY-HARD-ERR•Ø1Ø
WD19	O	11.Ø	$FRE-RUN•Ø36
WD2Ø	O	11.Ø	$FRE-RUN•Ø37
WEØ2	O	11.Ø	$DAU•Ø1Ø
WEØ4	O	11.Ø	$DAU•Ø12
WEØ5	I	49.Ø	D-ED-P-ERR•1ØØ
WEØ6	I	4.Ø	LOGIC1•1ØØ
WEØ7	I	12.Ø	UPDENS•1ØØ
WEØ8	I	1Ø.Ø	EN-CLK•1ØØ
WEØ9	O	11.Ø	$DAU•Ø11
WE1Ø	I	4.Ø	DSEL-BB•11Ø
WE12	I	4Ø.Ø	DDEN-Ø8-ØSØ•1ØØ
WE13	I	4Ø.Ø	DDEN-Ø9-ØSØ•1ØØ
WE14	I	4Ø.Ø	DDEN-1Ø-ØSØ•1ØØ
WE15	I	4Ø.Ø	DDEN-11-ØSØ•1ØØ
WE16	I	4Ø.Ø	DDEN-12-ØSØ•1ØØ
WE17	I	4Ø.Ø	DDEN-13-ØSØ•1ØØ
WE18	I	41.Ø	DDEN-14-ØSØ•1ØØ
WE19	I	41.Ø	DDEN-15-ØSØ•1ØØ
WE2Ø	I	11.Ø	D-SUB-CLK•ØØØ
WE21	O	5.Ø	$PARTIAL-CLR•Ø11
WFØØ	O	5.Ø	$PARTIAL-CLR•Ø12
WFØ1	I	31.Ø	MODE-RAR•11Ø
WFØ2	I	7.Ø	DEV-4XX-5ØØ•12Ø
WFØ3	I	7.Ø	DEV-5Ø1•12Ø
WFØ4	I	18.Ø	SYNC-BYTE•12Ø
WFØ5	O	6.Ø	$DAU-TOT-CLR•Ø11
WFØ6	I	34.Ø	SEQ-ERR•12Ø
WFØ7	I	48.Ø	STAT-ERR•11Ø
WFØ9	O	6.Ø	$DAU-TOT-CLR•Ø12
WF12	O	31.Ø	FIPC-RESET•Ø1Ø
WF13	O	6.Ø	$IDI-TOT-CLR•Ø1Ø
WF15	O	6.Ø	$IDI-TOT-CLR•Ø11
WF18	I	9.Ø	UP•1ØØ
WF19	I	35.Ø	CMD-WRITE•12Ø
WF21	I	7.Ø	CMD-WR-DCS•12Ø
WGØØ	I	7.Ø	DMPADR-15•1ØØ
WGØ2	I	7.Ø	DMPADR-14•1ØØ
WGØ3	I	7.Ø	DMPADR-13•1ØØ
WGØ4	I	7.Ø	DMPADR-12•1ØØ
WGØ5	I	7.Ø	DMPADR-11•1ØØ
WGØ6	I	7.Ø	DMPDTA-Ø•1ØØ
WGØ7	I	7.Ø	DMPDTA-1•1ØØ
WGØ8	I	7.Ø	DMPDTA-2•1ØØ
WGØ9	I	7.Ø	DMPDTA-3•1ØØ
WG1Ø	I	7.Ø	DMPDTA-4•1ØØ
WG12	I	7.Ø	DMPDTA-5•1ØØ
WG13	I	7.Ø	DMPDTA-6•1ØØ
WG14	I	7.Ø	DMPDTA-7•1ØØ

I/O PIN		PAGE	SIGNAL NAME
WG15	I	7.Ø	DMPDTA-P•1ØØ
WG16	I	4.Ø	MPWR•12Ø
WG17	I	1Ø.Ø	D-ER-IFØ•ØØØ
WG18	I	1Ø.Ø	D-ER-IF1•ØØØ
WG19	I	4.Ø	MPRD•12Ø
WHØØ	I	15.Ø	DREG-Ø•11Ø
WHØ1	I	15.Ø	DREG-1•11Ø
WHØ2	I	16.Ø	DREG-2•11Ø
WHØ3	I	16.Ø	DREG-3•11Ø
WHØ4	I	16.Ø	DREG-4•11Ø
WHØ5	I	16.Ø	DREG-5•11Ø
WHØ6	I	15.Ø	DREG-6•11Ø
WHØ7	I	15.Ø	DREG-7•11Ø
WHØ8	I	15.Ø	DREG-P•11Ø
WHØ9	O	32.Ø	FB-REG-FUL•11Ø
WH12	O	33.Ø	BREG-ØØ•11Ø
WH13	O	33.Ø	BREG-Ø1•11Ø
WH14	O	33.Ø	BREG-Ø2•11Ø
WH15	O	33.Ø	BREG-Ø3•11Ø
WH16	O	33.Ø	BREG-Ø4•11Ø
WH17	O	33.Ø	BREG-Ø5•11Ø
WH18	O	34.Ø	BREG-Ø6•11Ø
WH19	O	34.Ø	BREG-Ø7•11Ø
WH2Ø	O	34.Ø	BREG-P•11Ø
WJØØ	O	36.Ø	BUF-FULL•11Ø
WJØ1	O	38.Ø	SHORT-BLK•11Ø
WJØ2	O	38.Ø	LAST-DATA•11Ø
WJØ3	O	32.Ø	FB-REG-FUL•11Ø
WJØ4	O	46.Ø	B-REG-READY•11Ø
WJØ5	I	48.Ø	F-EDAC-ERROR•11Ø
WJØ8	I	17.Ø	FSECREQ•Ø1Ø
WJØ9	I	16.Ø	BUFF-STB•13Ø
WJ1Ø	O	39.Ø	S-SYNC•1ØØ
WJ12	O	17.Ø	FWRT-REG-ACK•Ø1Ø
WJ13	O	18.Ø	FCREG-ACK•11Ø
WJ14	O	38.Ø	D-LAST-EDAC•11Ø
WJ15	I	18.Ø	DBREG-ACK•1ØØ
WJ16	I	18.Ø	FCREG-FULL•11Ø
WJ17	O	1Ø.Ø	RABS-READ•Ø11
WJ2Ø	I	31.Ø	POMC•1ØØ
WKØØ	I	7.Ø	DEV-4XX•11Ø
WKØ1	I	15.Ø	D-SW-Ø•1ØØ
WKØ2	I	15.Ø	D-SW-1•1ØØ
WKØ3	I	16.Ø	D-SW-2•1ØØ
WKØ4	I	16.Ø	D-SW-3•1ØØ
WKØ5	I	16.Ø	D-SW-4•1ØØ
WKØ6	I	16.Ø	D-SW-5•1ØØ
WKØ7	I	15.Ø	D-SW-6•1ØØ
WKØ8	I	15.Ø	D-SW-7•1ØØ
WKØ9	O	31.Ø	RCIR-MODE•1ØØ
WK1Ø	O	31.Ø	RCOR-MODE•1ØØ
WK12	O	38.Ø	RSB-REG-Ø•1ØØ
WK13	O	38.Ø	RSB-REG-1•1ØØ
WK14	O	38.Ø	RSB-REG-2•1ØØ
WK15	O	38.Ø	RSB-REG-3•1ØØ
WK16	O	38.Ø	RSB-REG-4•1ØØ
WK17	O	38.Ø	RSB-REG-5•1ØØ

I/O PIN		PAGE	SIGNAL NAME
WK18	O	39.Ø	RSB-REG-6•1ØØ
WK19	O	39.Ø	RSB-REG-7•1ØØ
WK2Ø	O	39.Ø	RSB-REG-P•1ØØ

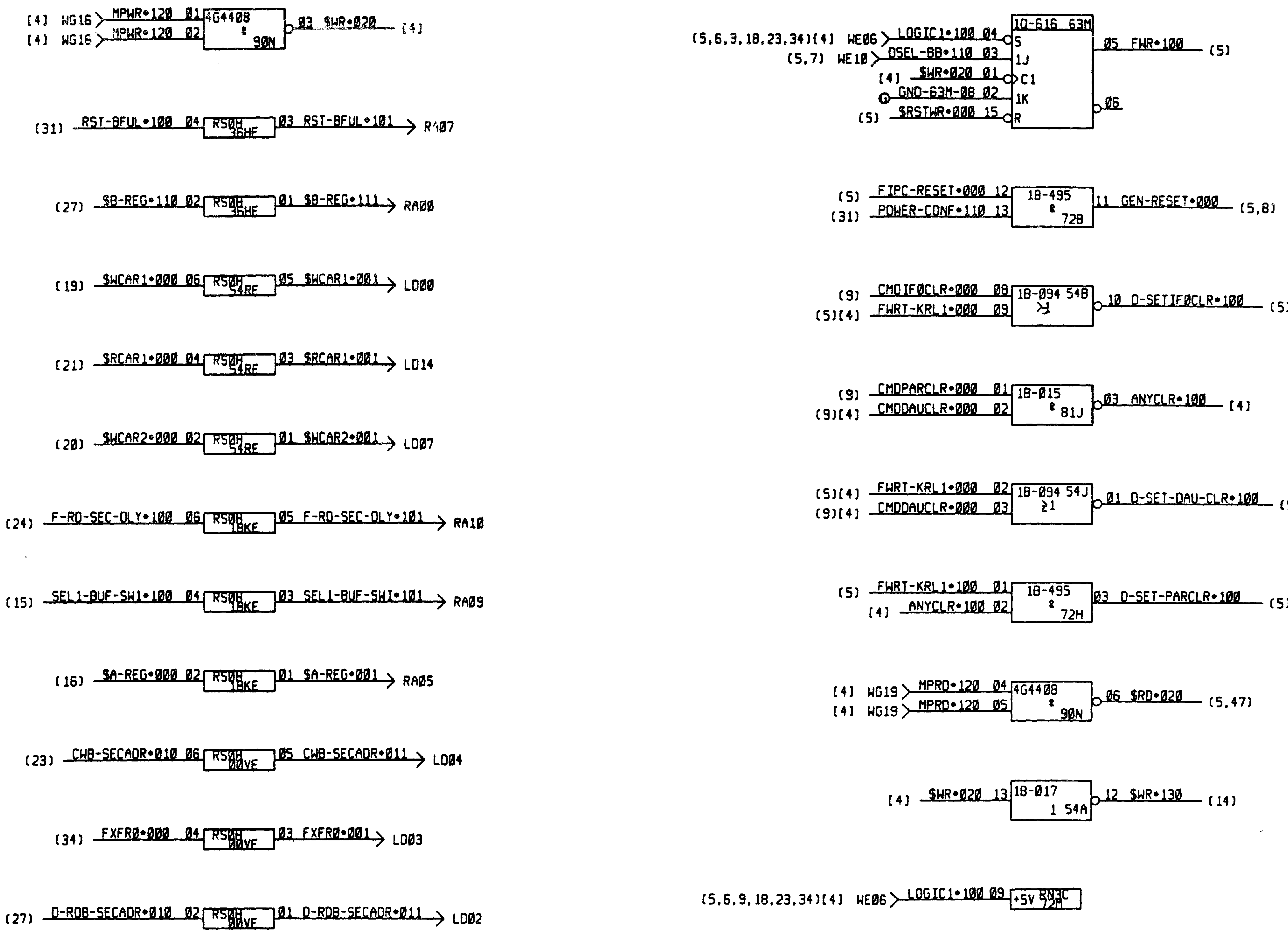
58Ø88874

HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

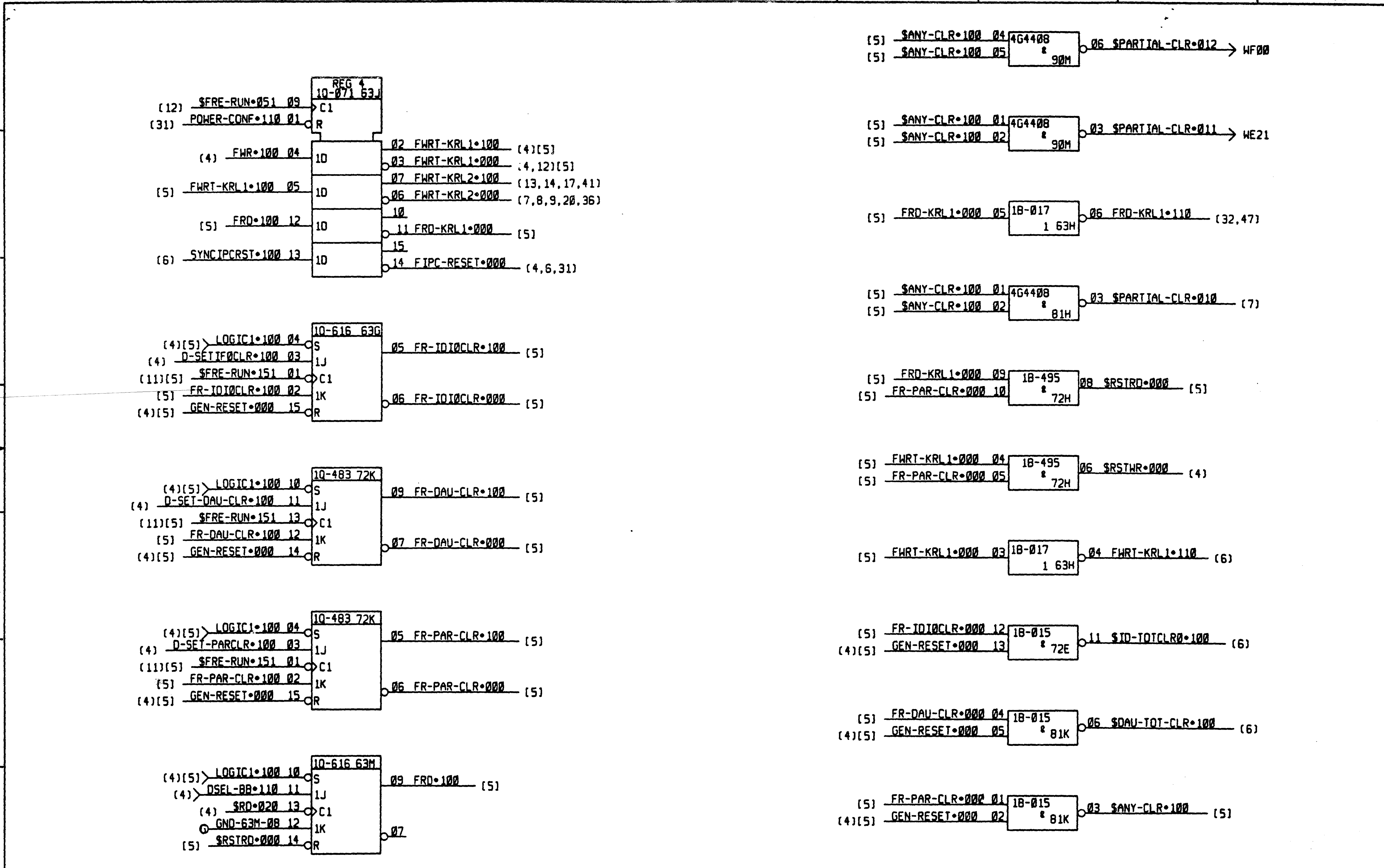
TITLE LOGIC DIAGRAM- WDASB
I/O PIN -
PAGE CROSS REFERENCE

SIZE	DWG NO	SH	REV
B	58Ø88874	3.1	C

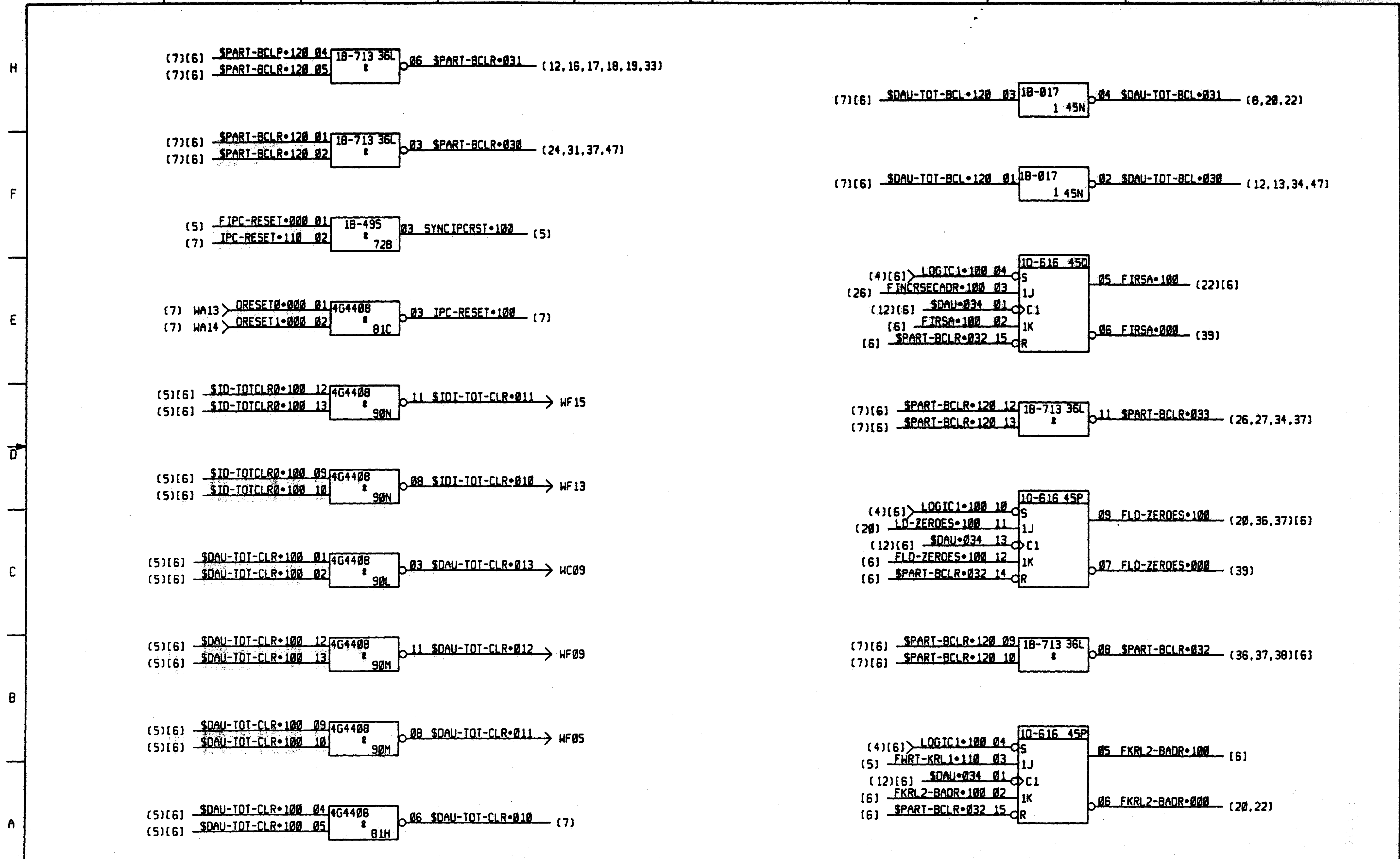


HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 4.0	REV C

58088874



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 5.0	REV C

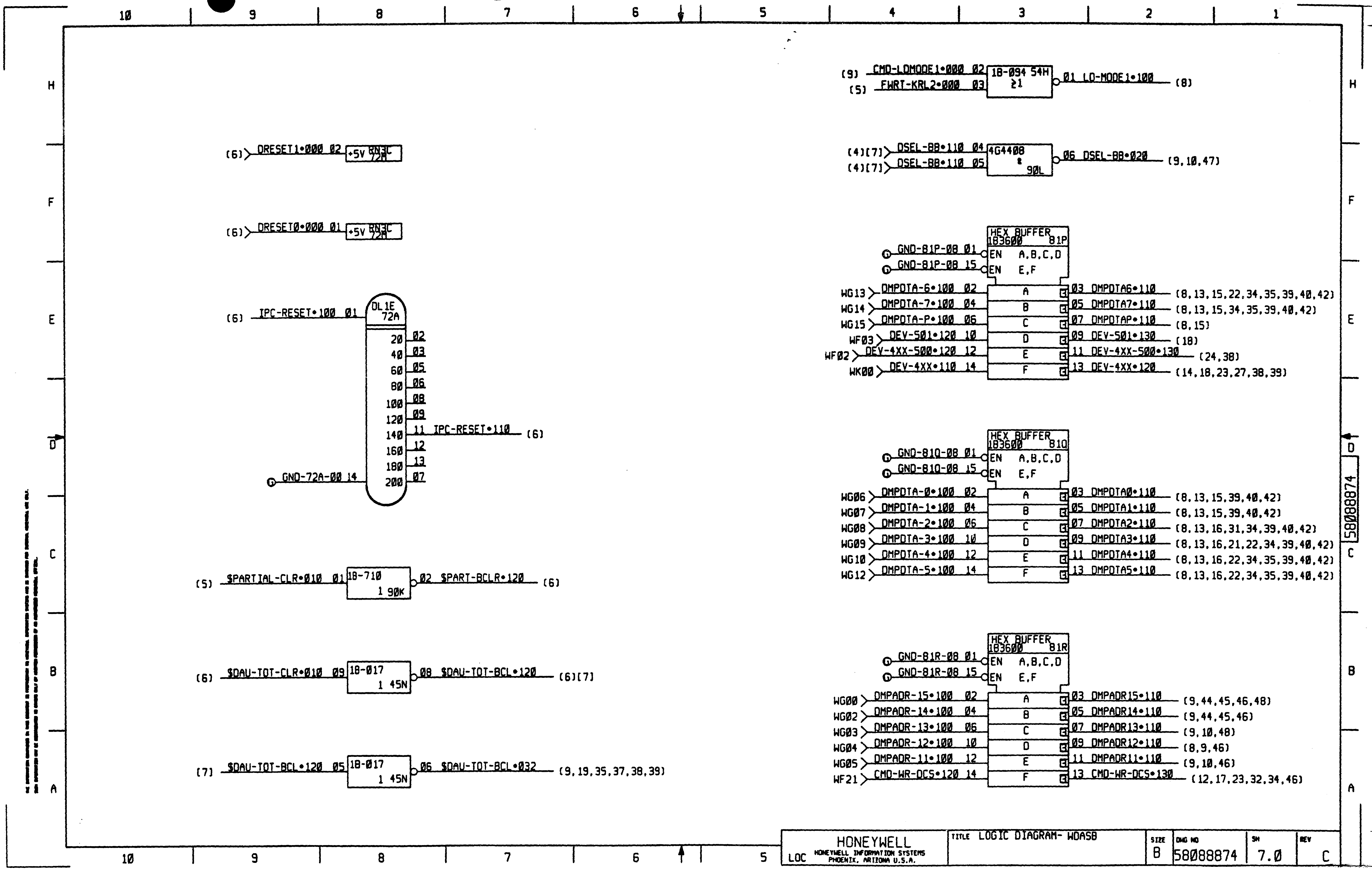


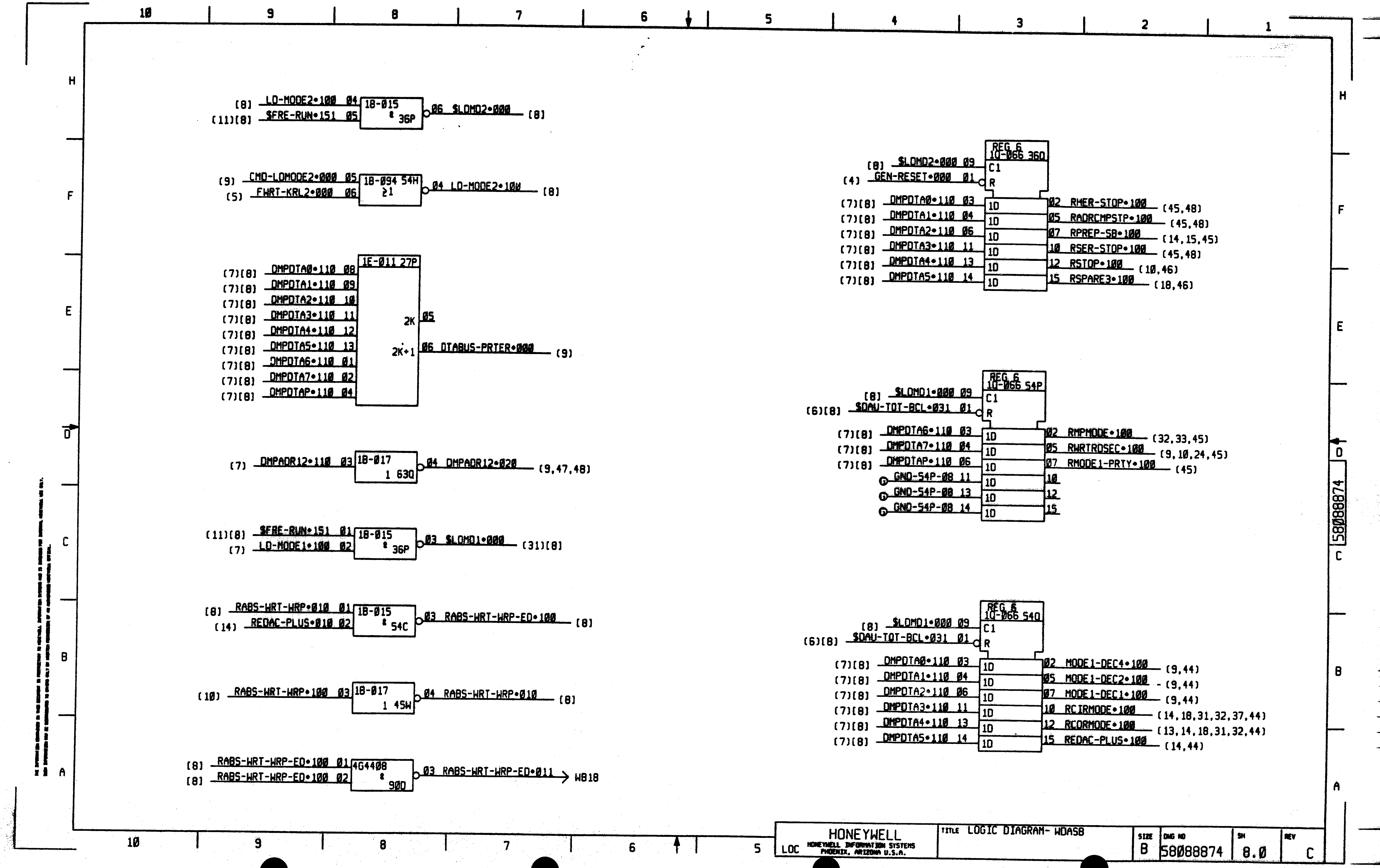
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

LOC

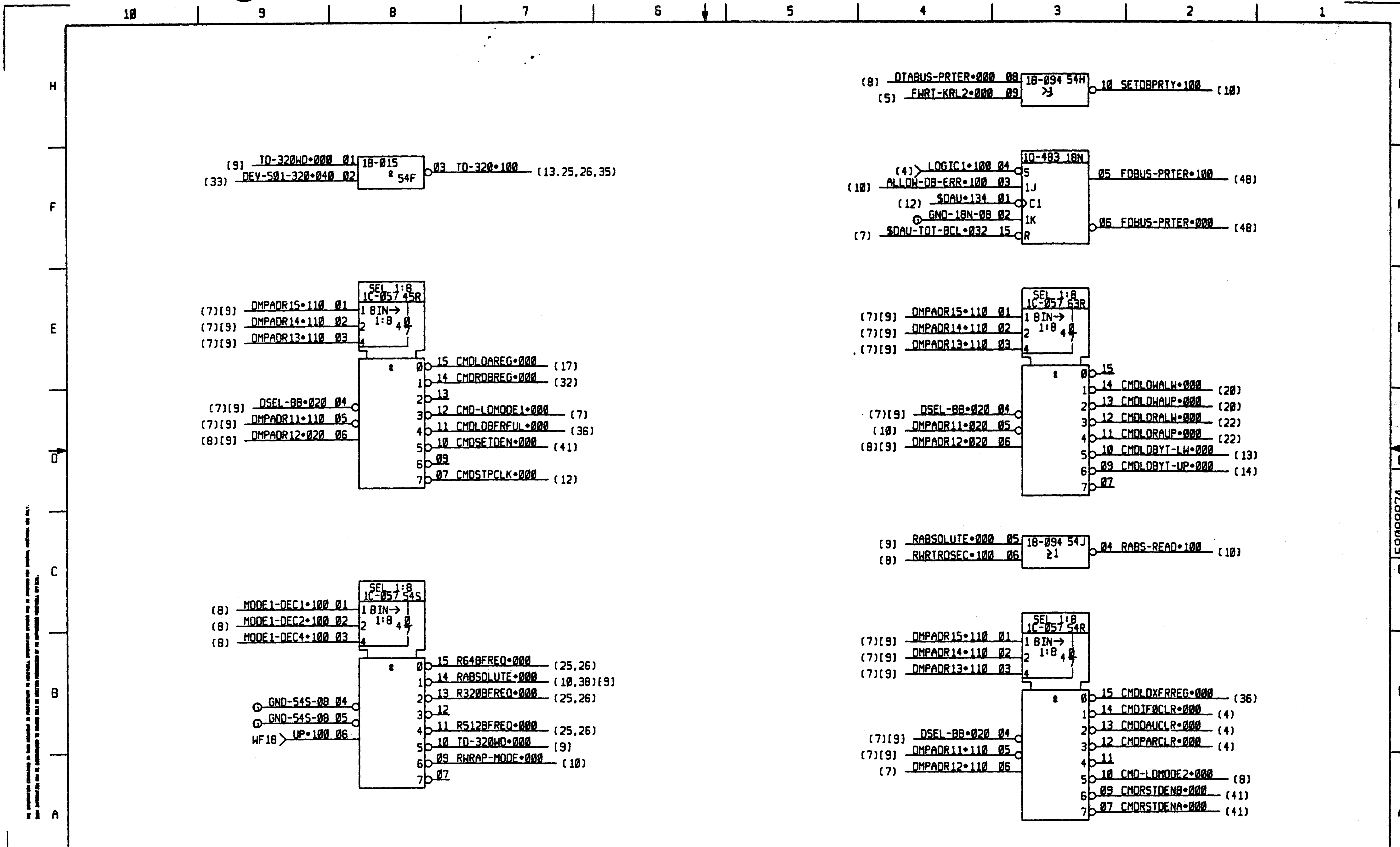
TITLE LOGIC DIAGRAM- WDASB

SIZE	DWG NO	SH	REV
B	58088874	6.0	C


(9) CMD-LDMODE1•000 02
(5) FWRT-KRL2•000 03
1B-094 54H ≥1
01 LD-MODE1•100 (8)
(4)(7) DSEL-BB•110 04
(4)(7) DSEL-BB•110 05
4G4408 & 90L
06 DSEL-BB•020 (9,10,47)
(6) DRESET1•000 02 +5V RN3C 72M
(6) DRESET0•000 01 +5V RN3C 72M
(6) IPC-RESET•100 01
DL1E 72A
20 02
40 03
60 05
80 06
100 08
120 09
140 11 IPC-RESET•110 (6)
160 12
180 13
200 07
GND-72A-00 14
(5) $PARTIAL-CLR•010 01
1B-710 1 90K
02 $PART-BCLR•120 (6)
(6) $DAU-TOT-CLR•010 09
1B-017 1 45N
08 $DAU-TOT-BCL•120 (6)(7)
(7) $DAU-TOT-BCL•120 05
1B-017 1 45N
06 $DAU-TOT-BCL•032 (9,19,35,37,38,39)
HEX BUFFER 1B3600 81P
GND-81P-08 01 EN A,B,C,D
GND-81P-08 15 EN E,F
WG13 DMPDTA-6•100 02 A 03 DMPDTA6•110 (8,13,15,22,34,35,39,40,42)
WG14 DMPDTA-7•100 04 B 05 DMPDTA7•110 (8,13,15,34,35,39,40,42)
WG15 DMPDTA-P•100 06 C 07 DMPDTAP•110 (8,15)
WF03 DEV-501•120 10 D 09 DEV-501•130 (18)
WF02 DEV-4XX-500•120 12 E 11 DEV-4XX-500•130 (24,38)
WK00 DEV-4XX•110 14 F 13 DEV-4XX•120 (14,18,23,27,38,39)
HEX BUFFER 1B3600 81Q
GND-81Q-08 01 EN A,B,C,D
GND-81Q-08 15 EN E,F
WG06 DMPDTA-0•100 02 A 03 DMPDTA0•110 (8,13,15,39,40,42)
WG07 DMPDTA-1•100 04 B 05 DMPDTA1•110 (8,13,15,39,40,42)
WG08 DMPDTA-2•100 06 C 07 DMPDTA2•110 (8,13,16,31,34,39,40,42)
WG09 DMPDTA-3•100 10 D 09 DMPDTA3•110 (8,13,16,21,22,34,39,40,42)
WG10 DMPDTA-4•100 12 E 11 DMPDTA4•110 (8,13,16,22,34,35,39,40,42)
WG12 DMPDTA-5•100 14 F 13 DMPDTA5•110 (8,13,16,22,34,35,39,40,42)
HEX BUFFER 1B3600 81R
GND-81R-08 01 EN A,B,C,D
GND-81R-08 15 EN E,F
WG00 DMPADR-15•100 02 A 03 DMPADR15•110 (9,44,45,46,48)
WG02 DMPADR-14•100 04 B 05 DMPADR14•110 (9,44,45,46)
WG03 DMPADR-13•100 06 C 07 DMPADR13•110 (9,10,48)
WG04 DMPADR-12•100 10 D 09 DMPADR12•110 (8,9,46)
WG05 DMPADR-11•100 12 E 11 DMPADR11•110 (9,10,46)
WF21 CMD-WR-DCS•120 14 F 13 CMD-WR-DCS•130 (12,17,23,32,34,46)
58088874
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- WDASB
SIZE B
DWG NO 58088874
SH 7.0
REV C



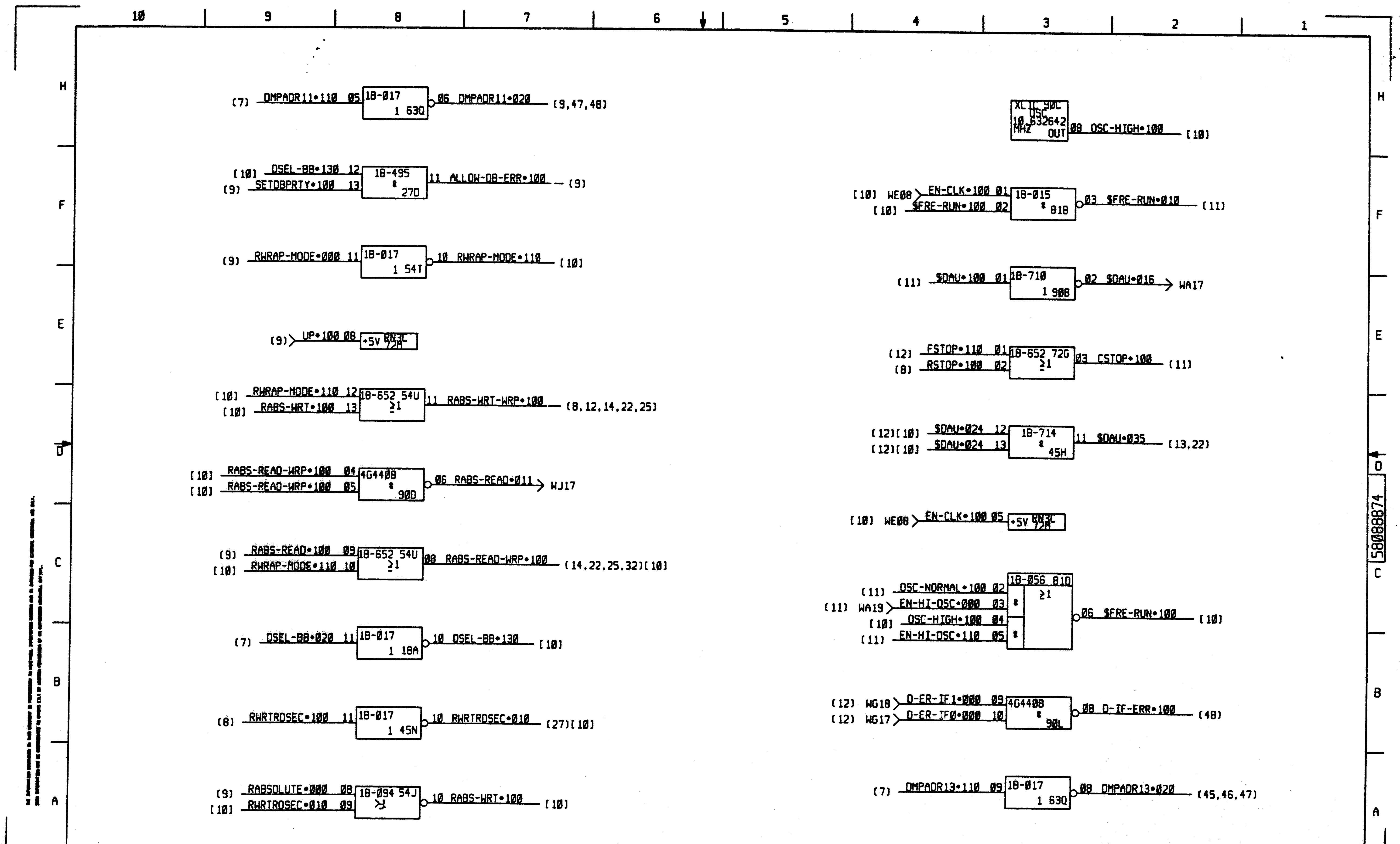
LD-MODE2•100 04
$FRE-RUN•151 05
1B-015 & 36P
06 $LOMD2•000
CMD-LDMODE2•000 05
FWRT-KRL2•000 06
1B-094 54H ≥1
04 LD-MODE2•100
1E-011 27P
DMPDTA0•110 08
DMPDTA1•110 09
DMPDTA2•110 10
DMPDTA3•110 11
DMPDTA4•110 12
DMPDTA5•110 13
DMPDTA6•110 01
DMPDTA7•110 02
DMPDTAP•110 04
2K 05
2K+1 06 DTABUS-PRTER•000
DMPADR12•110 03
1B-017 1 63Q
04 DMPADR12•020
$FRE-RUN•151 01
LD-MODE1•100 02
1B-015 & 36P
03 $LOMD1•000
RABS-WRT-WRP•010 01
REDAC-PLUS•010 02
1B-015 & 54C
03 RABS-WRT-WRP-ED•100
RABS-WRT-WRP•100 03
1B-017 1 45W
04 RABS-WRT-WRP•010
RABS-WRT-WRP-ED•100 01
RABS-WRT-WRP-ED•100 02
4G4408 & 90D
03 RABS-WRT-WRP-ED•011
WB18
REG 6 1D-066 36Q
$LOMD2•000 09
GEN-RESET•000 01
RMER-STOP•100
RADRCMPSTP•100
RPREP-SB•100
RSER-STOP•100
RSTOP•100
RSPARE3•100
REG 6 1D-066 54P
$LOMD1•000 09
$DAU-TOT-BCL•031 01
RMPMODE•100
RWRTRDSEC•100
RMODE1-PRTY•100
GND-54P-08 11
GND-54P-08 13
GND-54P-08 14
REG 6 1D-066 54Q
MODE1-DEC4•100
MODE1-DEC2•100
MODE1-DEC1•100
RCIRMODE•100
RCORMODE•100
REDAC-PLUS•100
(14,18,31,32,37,44)
(13,14,18,31,32,44)
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- WDASB
SIZE B
DWG NO 58088874
SH 8.0
REV C



HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDASB

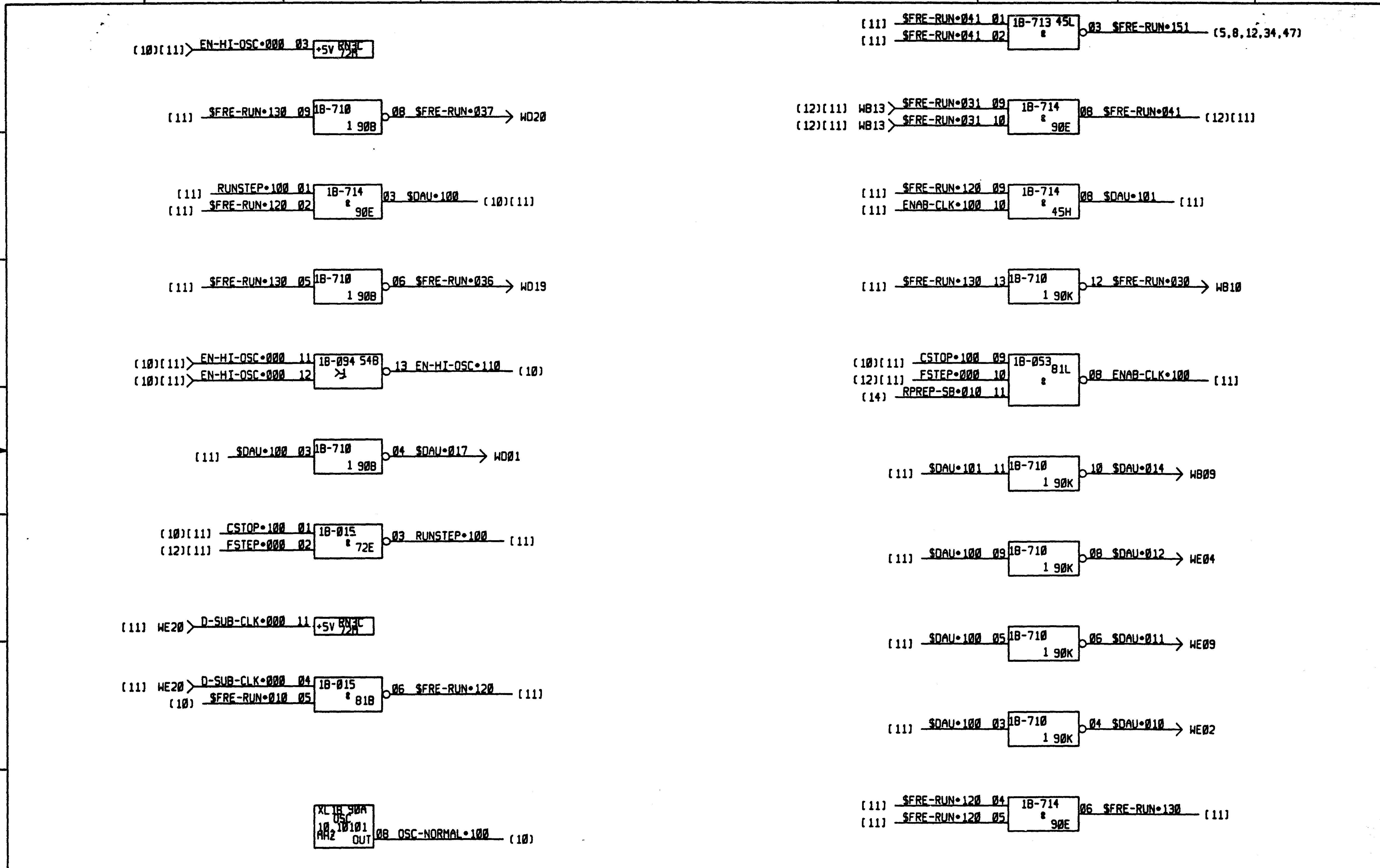
SIZE	DWG NO	SH	REV
B	58088874	9.0	C



HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

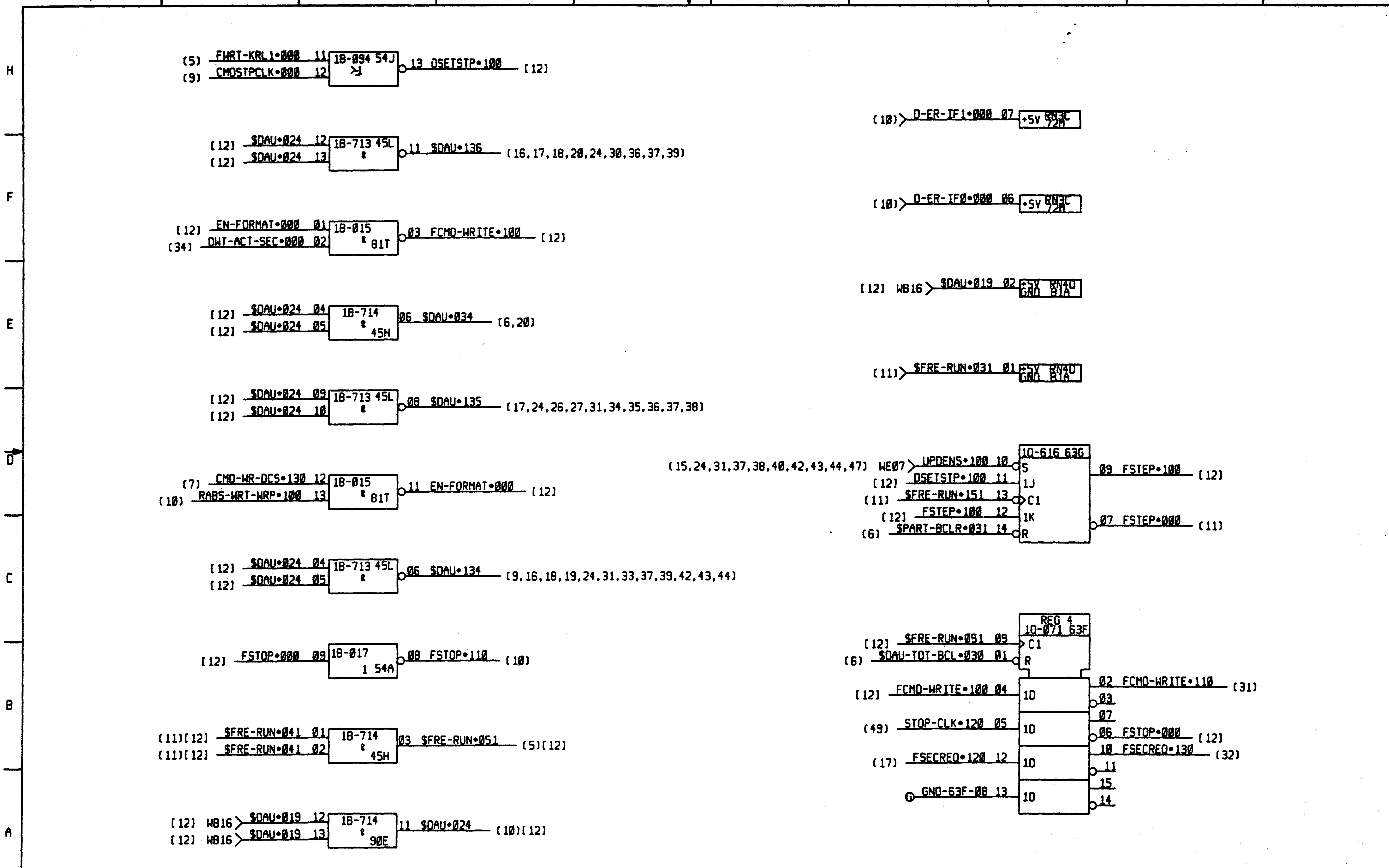
TITLE LOGIC DIAGRAM- WDASB

SIZE	DWG NO	SH	REV
B	58088874	10.0	C



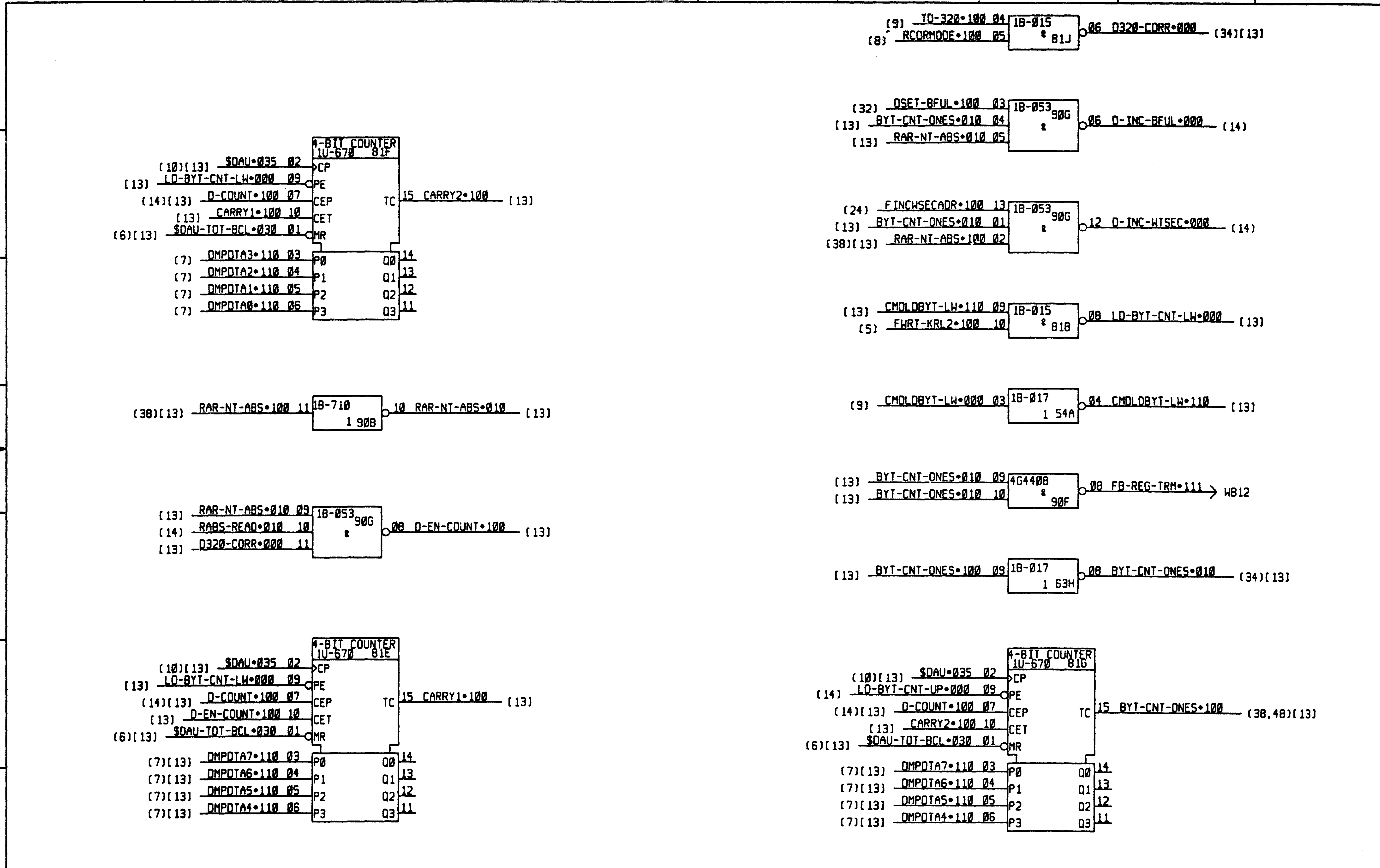
HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE	SIZE	DWG NO	SH	REV
LOGIC DIAGRAM- WDASB	B	58088874	11.0	C



58088874

HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 12.0	REV C

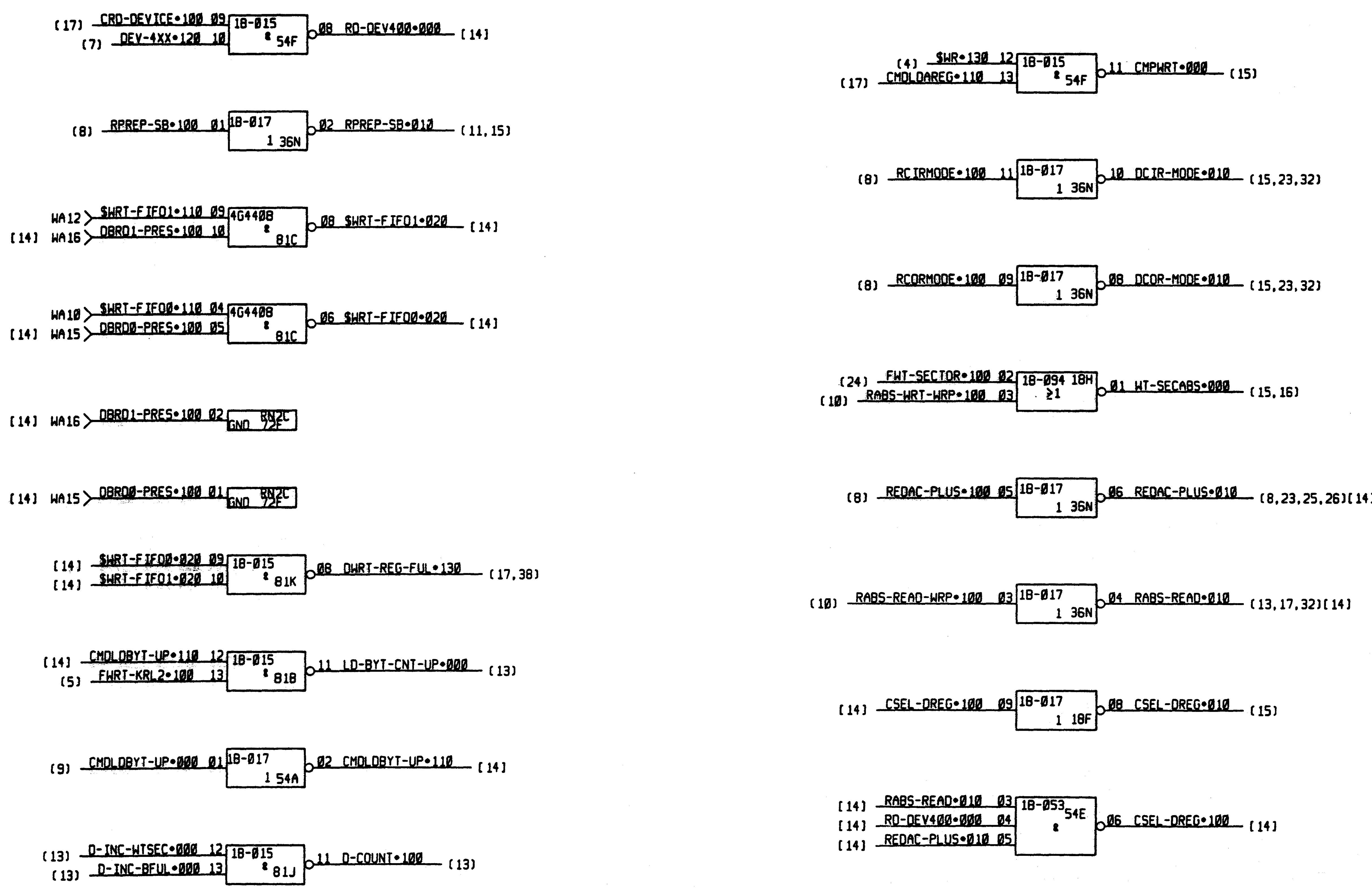


HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

LOC

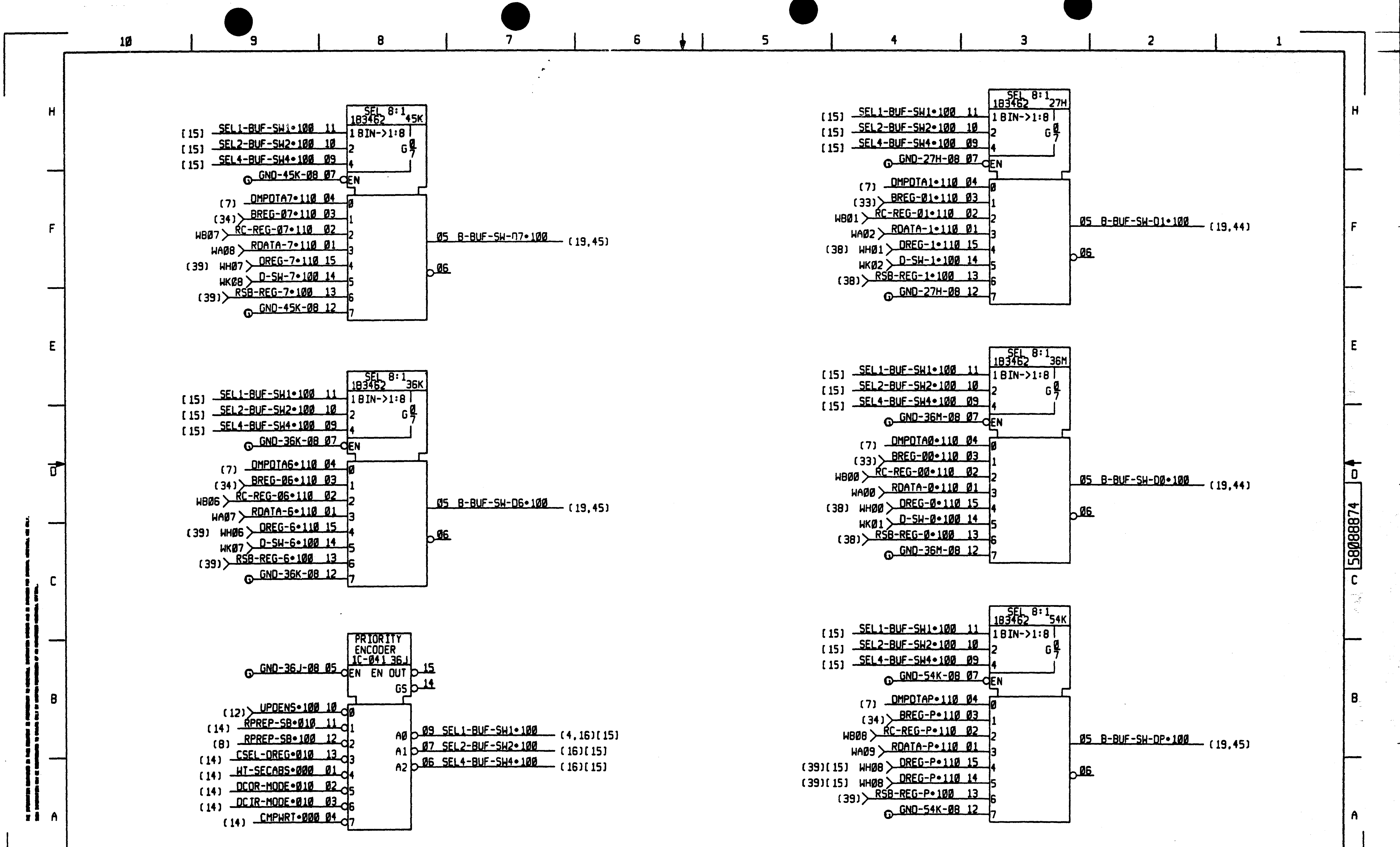
TITLE LOGIC DIAGRAM- WDASB

SIZE	DWG NO	SH	REV
B	58088874	13.0	C

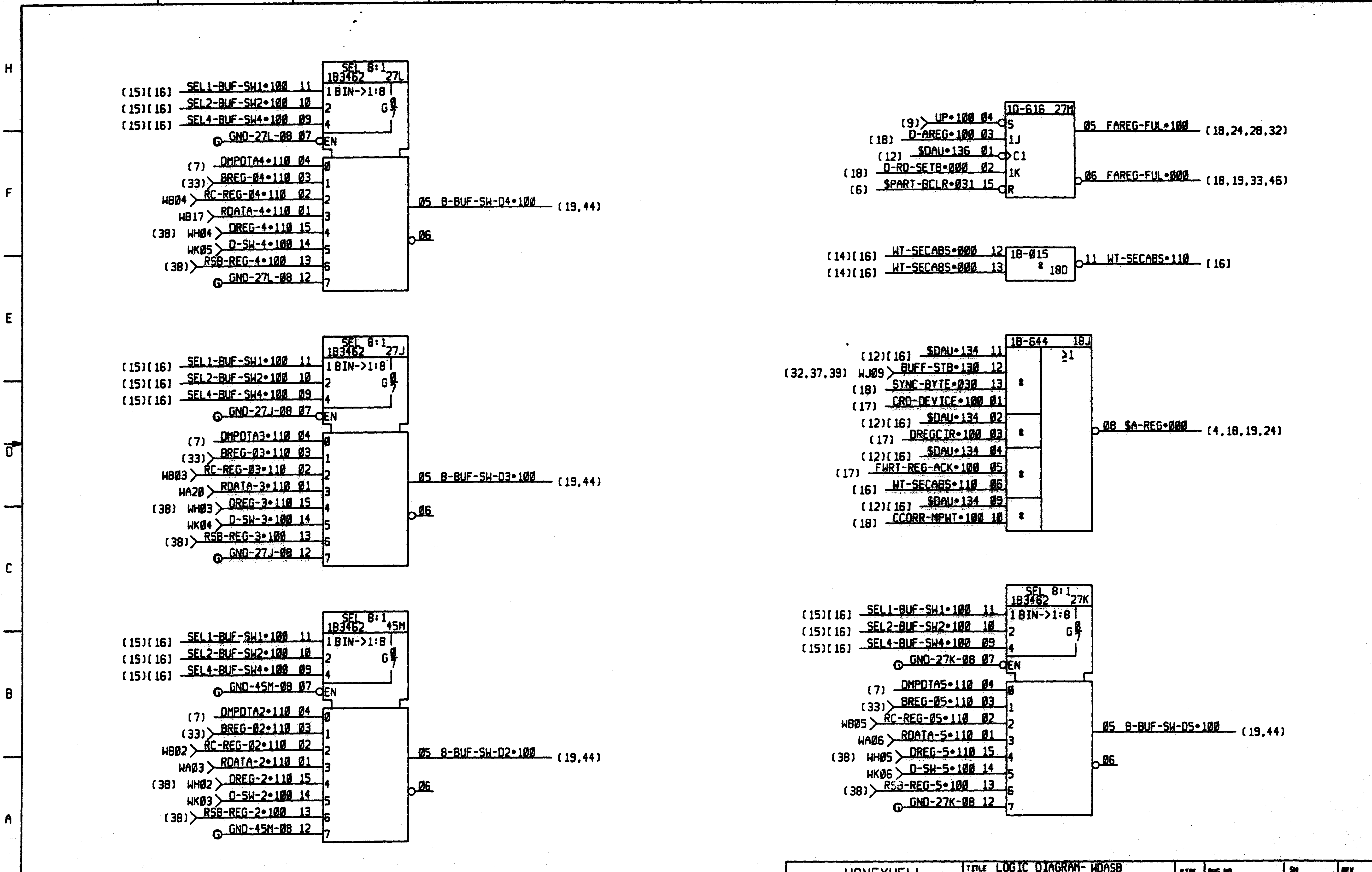


HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC	TITLE	SIZE	DWG NO	SH	REV
	LOGIC DIAGRAM- WDASB	B	58088874	14.0	C



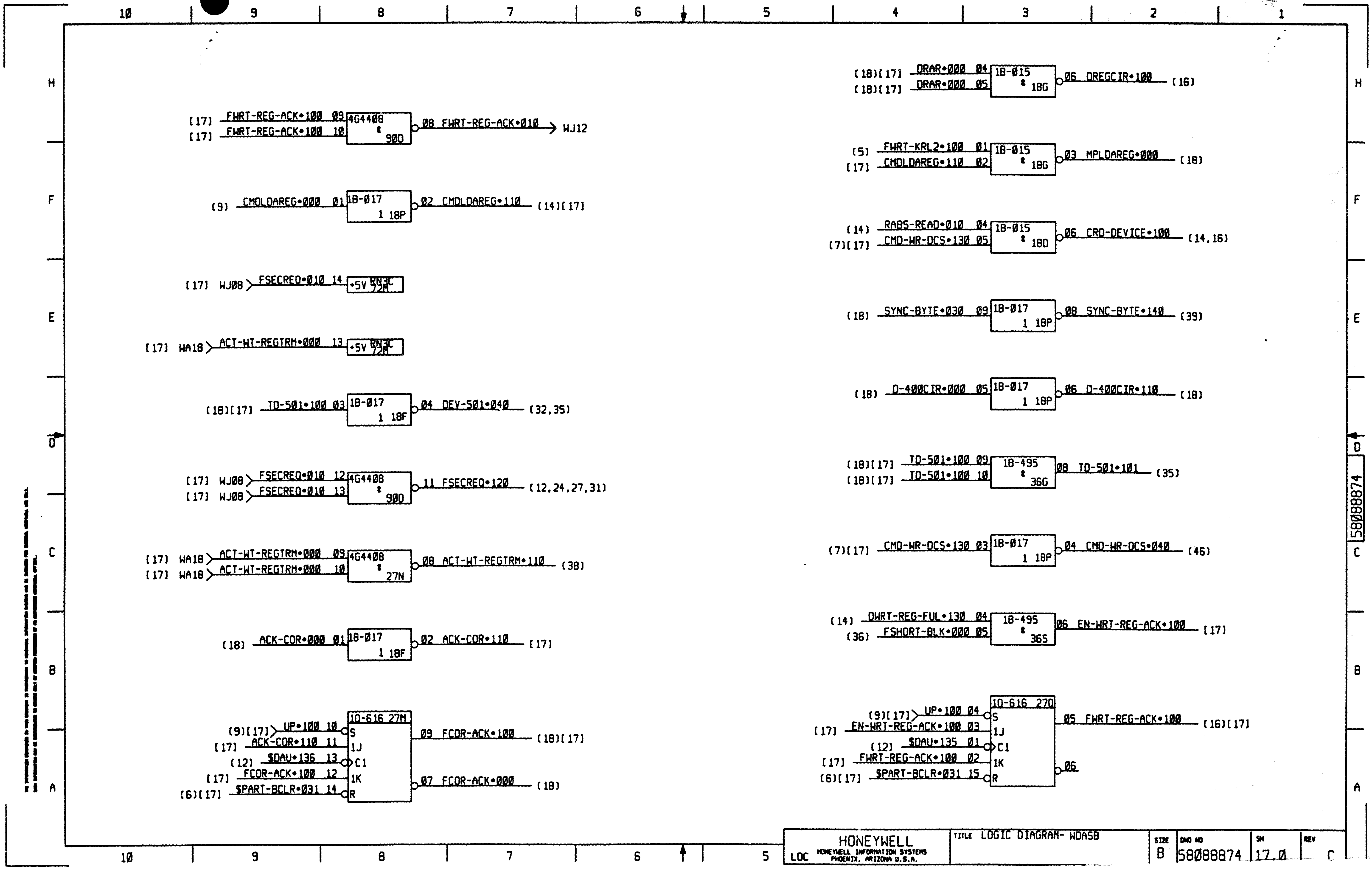
LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 15.0	REV C



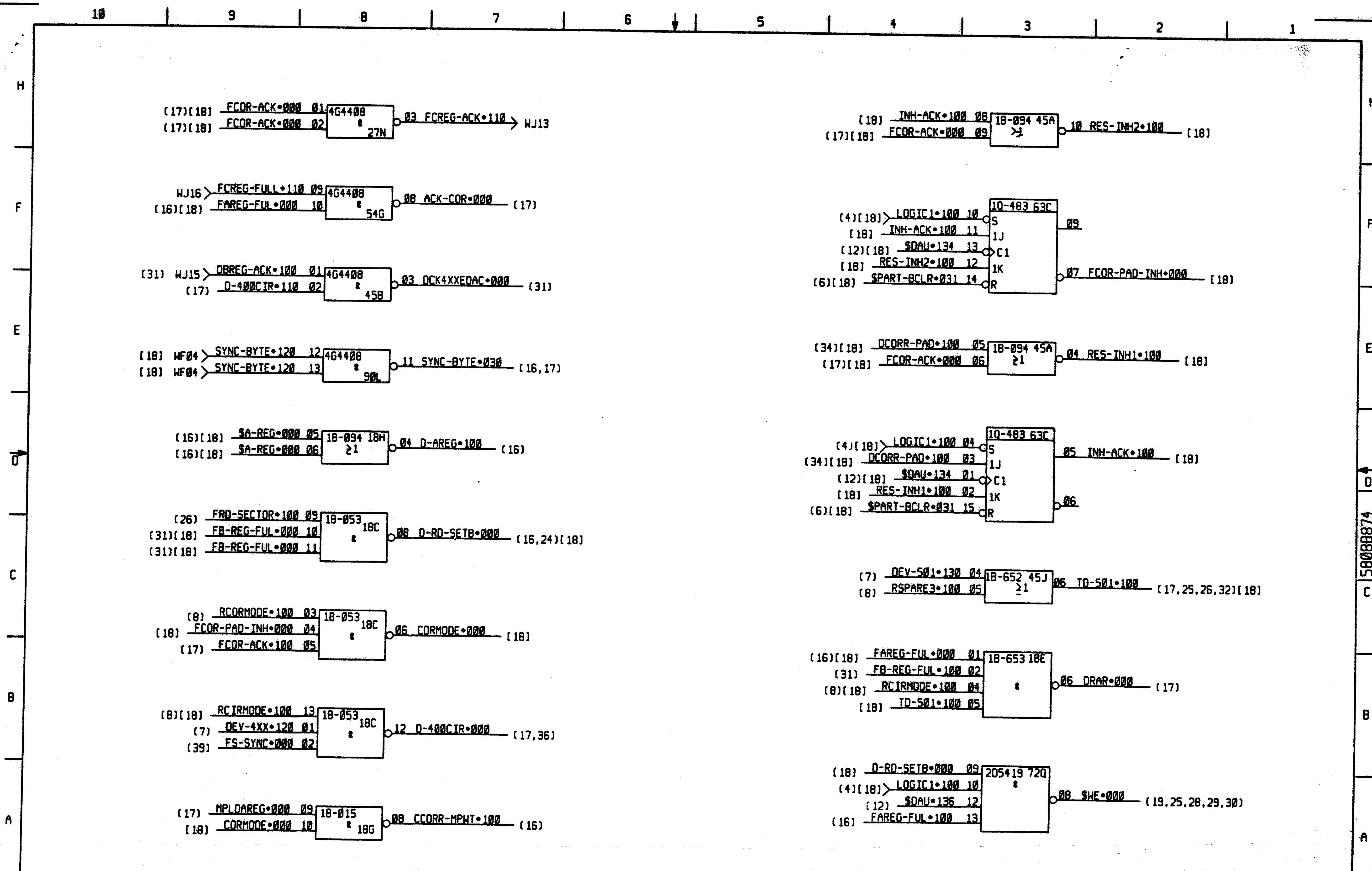
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDASB

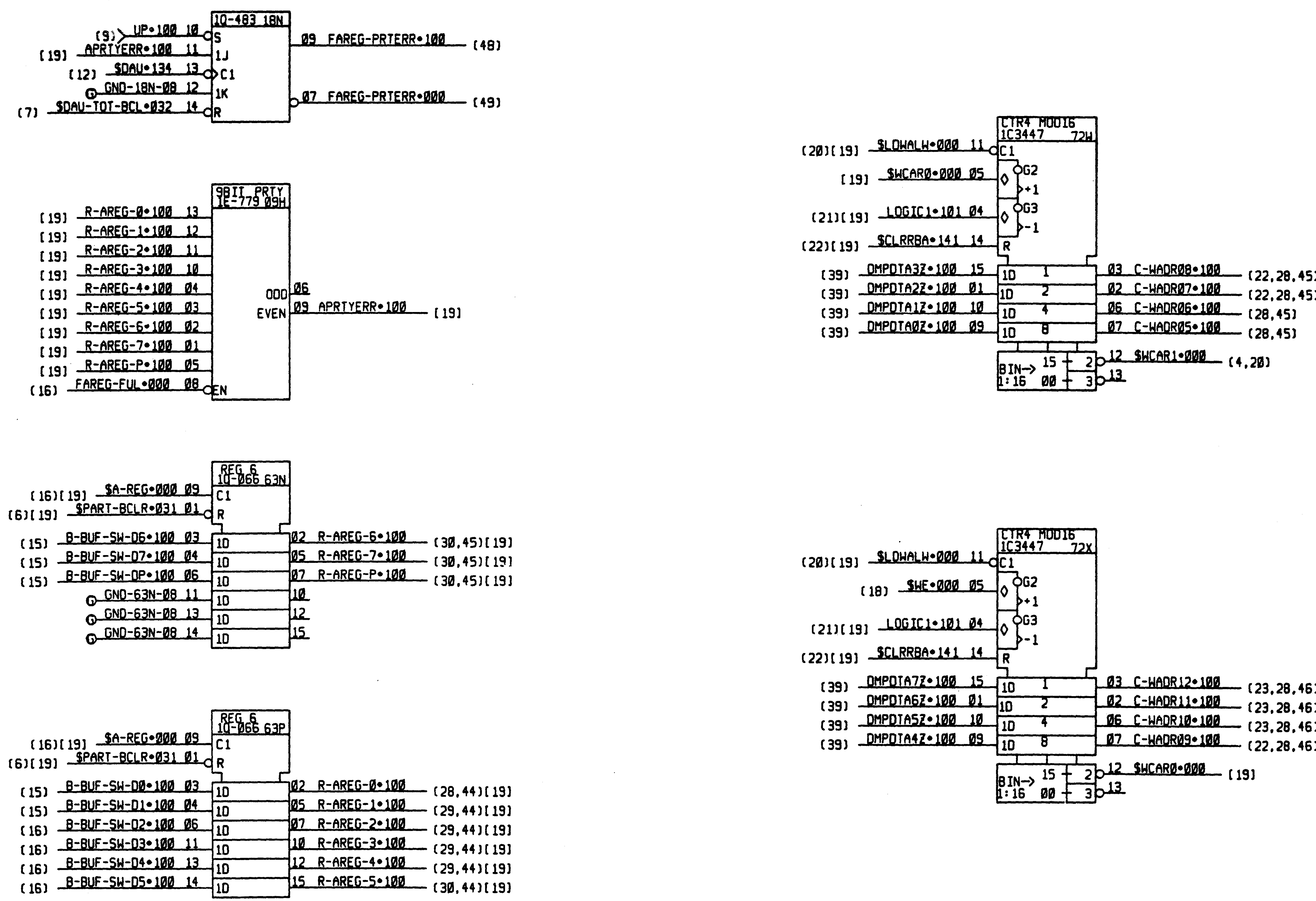
SIZE	DWG NO	SH	REV
B	58088874	16.0	C



[17] FWRT-REG-ACK•100 09
[17] FWRT-REG-ACK•100 10
4G4408 & 90D
08 FWRT-REG-ACK•010 WJ12
(9) CMDLDAREG•000 01
1B-017 1 18P
02 CMDLDAREG•110 [14][17]
[17] WJ08 FSECREQ•010 14 +5V RN3C 72H
[17] WA18 ACT-WT-REGTRM•000 13 +5V RN3C 72H
[18][17] TD-501•100 03
1B-017 1 18F
04 DEV-501•040 [32,35]
[17] WJ08 FSECREQ•010 12
[17] WJ08 FSECREQ•010 13
4G4408 & 90D
11 FSECREQ•120 [12,24,27,31]
[17] WA18 ACT-WT-REGTRM•000 09
[17] WA18 ACT-WT-REGTRM•000 10
4G4408 & 27N
08 ACT-WT-REGTRM•110 [38]
[18] ACK-COR•000 01
1B-017 1 18F
02 ACK-COR•110 [17]
[9][17] UP•100 10 S
[17] ACK-COR•110 11 1J
[12] $DAU•136 13 C1
[17] FCOR-ACK•100 12 1K
[6][17] $PART-BCLR•031 14 R
10-616 27M
09 FCOR-ACK•100 [18][17]
07 FCOR-ACK•000 [18]
[18][17] DRAR•000 04
[18][17] DRAR•000 05
1B-015 & 18G
06 DREGCIR•100 [16]
[5] FWRT-KRL2•100 01
[17] CMDLDAREG•110 02
1B-015 & 18G
03 MPLDAREG•000 [18]
[14] RABS-READ•010 04
[7][17] CMD-WR-DCS•130 05
1B-015 & 180
06 CRD-DEVICE•100 [14,16]
[18] SYNC-BYTE•030 09
1B-017 1 18P
08 SYNC-BYTE•140 [39]
[18] D-400CIR•000 05
1B-017 1 18P
06 D-400CIR•110 [18]
[18][17] TD-501•100 09
[18][17] TD-501•100 10
1B-495 & 36G
08 TD-501•101 [35]
[7][17] CMD-WR-DCS•130 03
1B-017 1 18P
04 CMD-WR-DCS•040 [46]
[14] DWRT-REG-FUL•130 04
[36] FSHORT-BLK•000 05
1B-495 & 365
06 EN-WRT-REG-ACK•100 [17]
[9][17] UP•100 04 S
[17] EN-WRT-REG-ACK•100 03 1J
[12] $DAU•135 01 C1
[17] FWRT-REG-ACK•100 02 1K
[6][17] $PART-BCLR•031 15 R
10-616 270
05 FWRT-REG-ACK•100 [16][17]
06
58088874
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- WDASB
SIZE B
DWG NO 58088874
SH 17.0
REV C

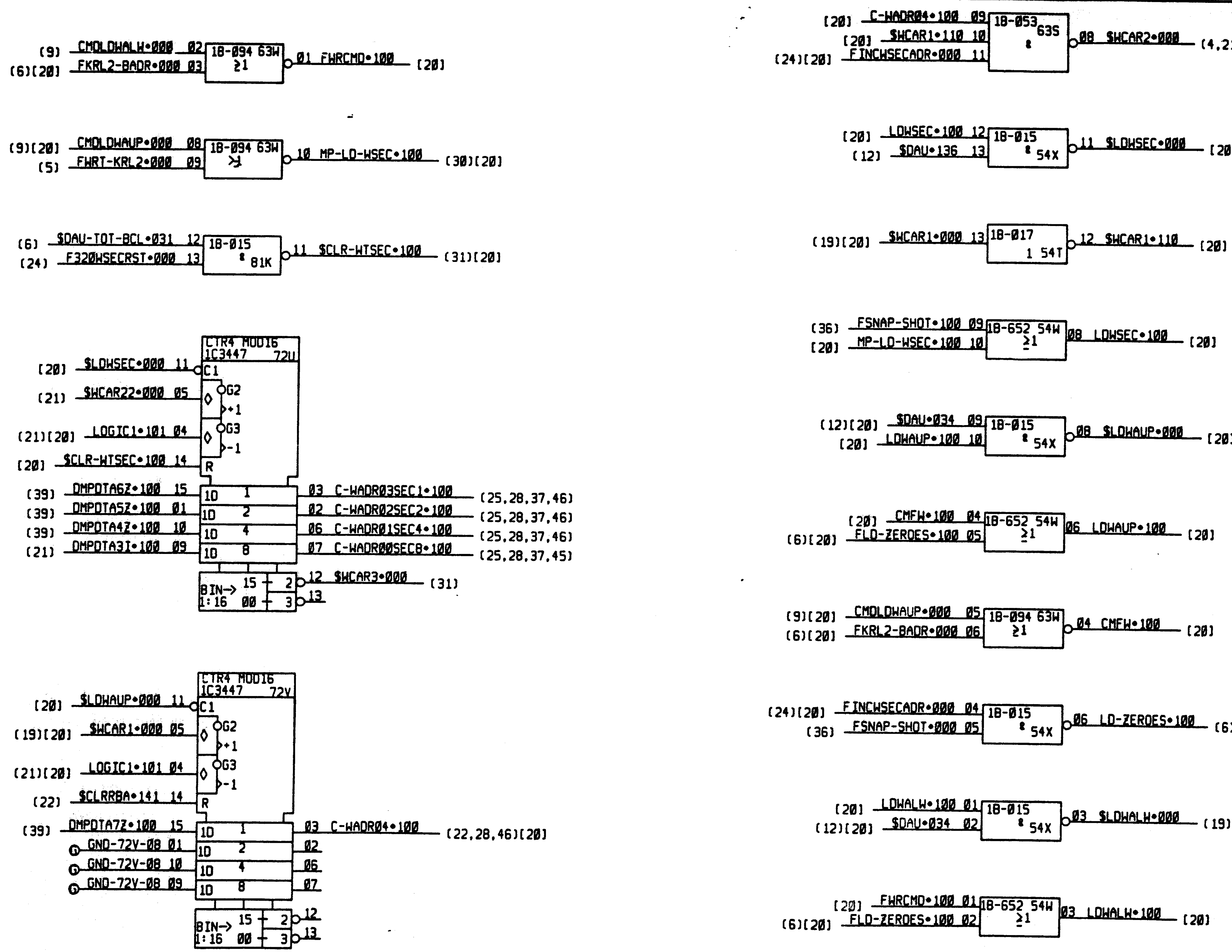


HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- WDASB
SIZE B | DWG NO 58088874 | SH 18.0 | REV C

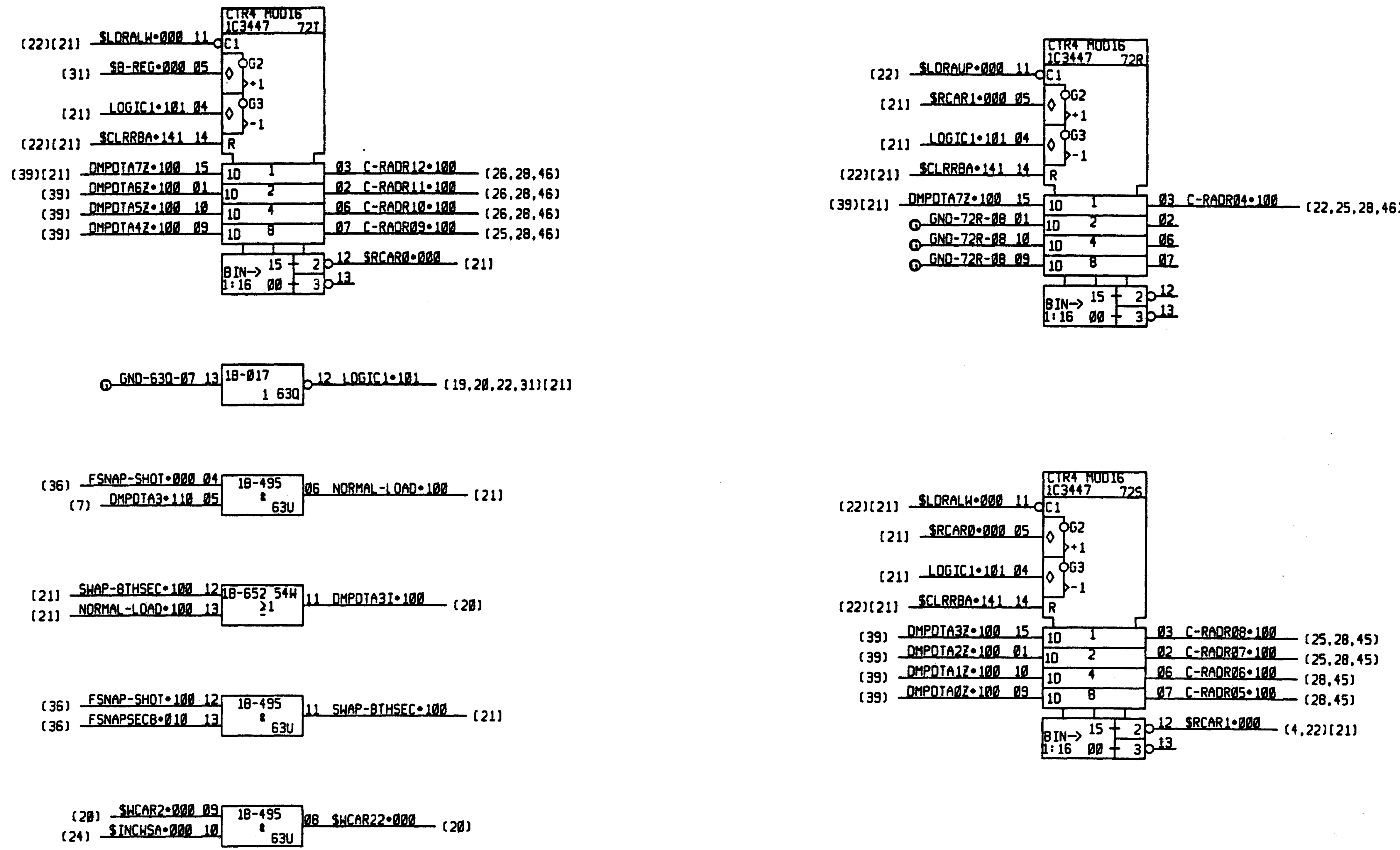


LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 19.0	REV C

58088874



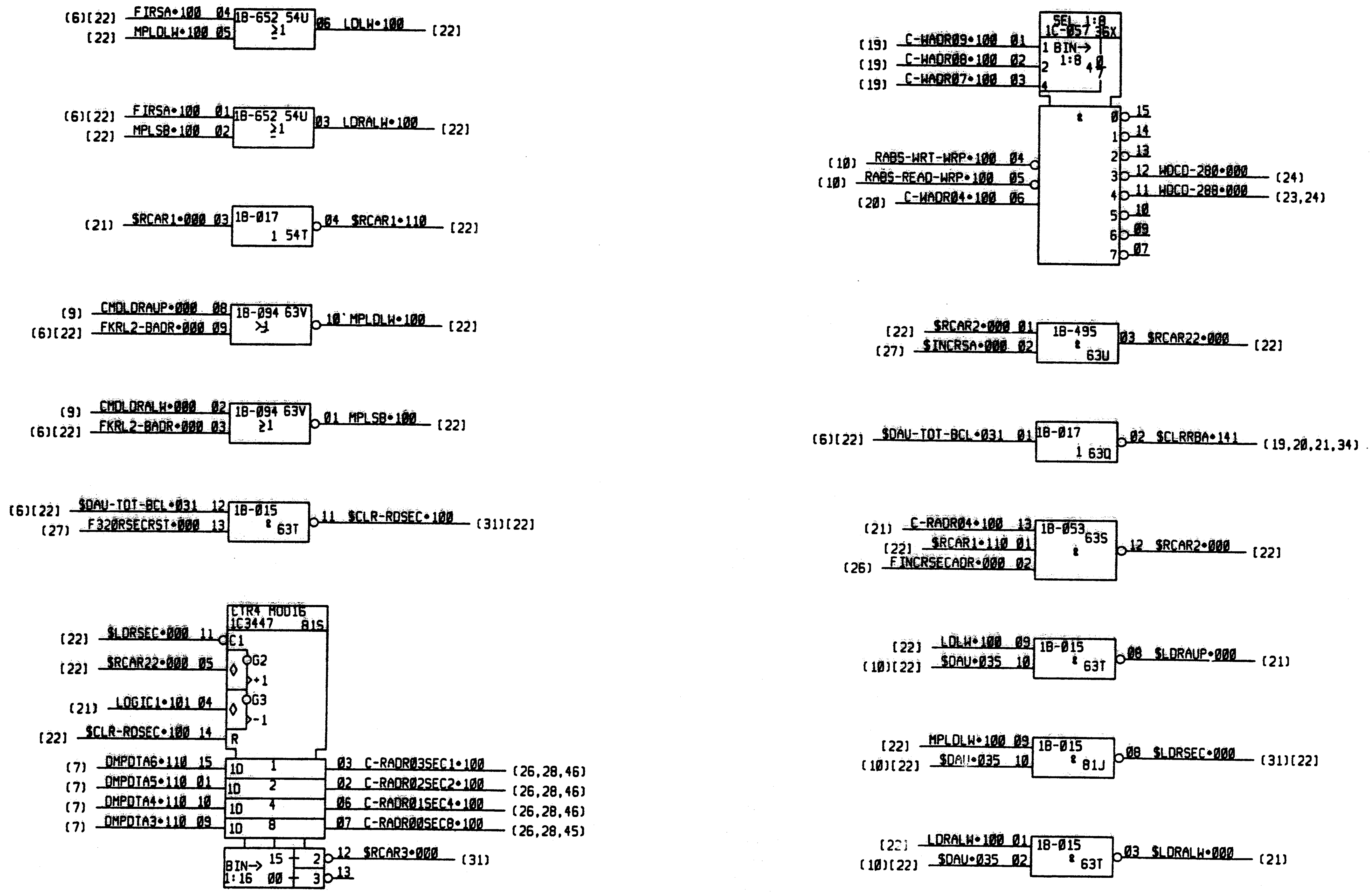
LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 20.0	REV C



HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC	TITLE	SIZE	DWG NO	SH	REV
	LOGIC DIAGRAM- WDASB	B	58088874	21.0	C

58088874

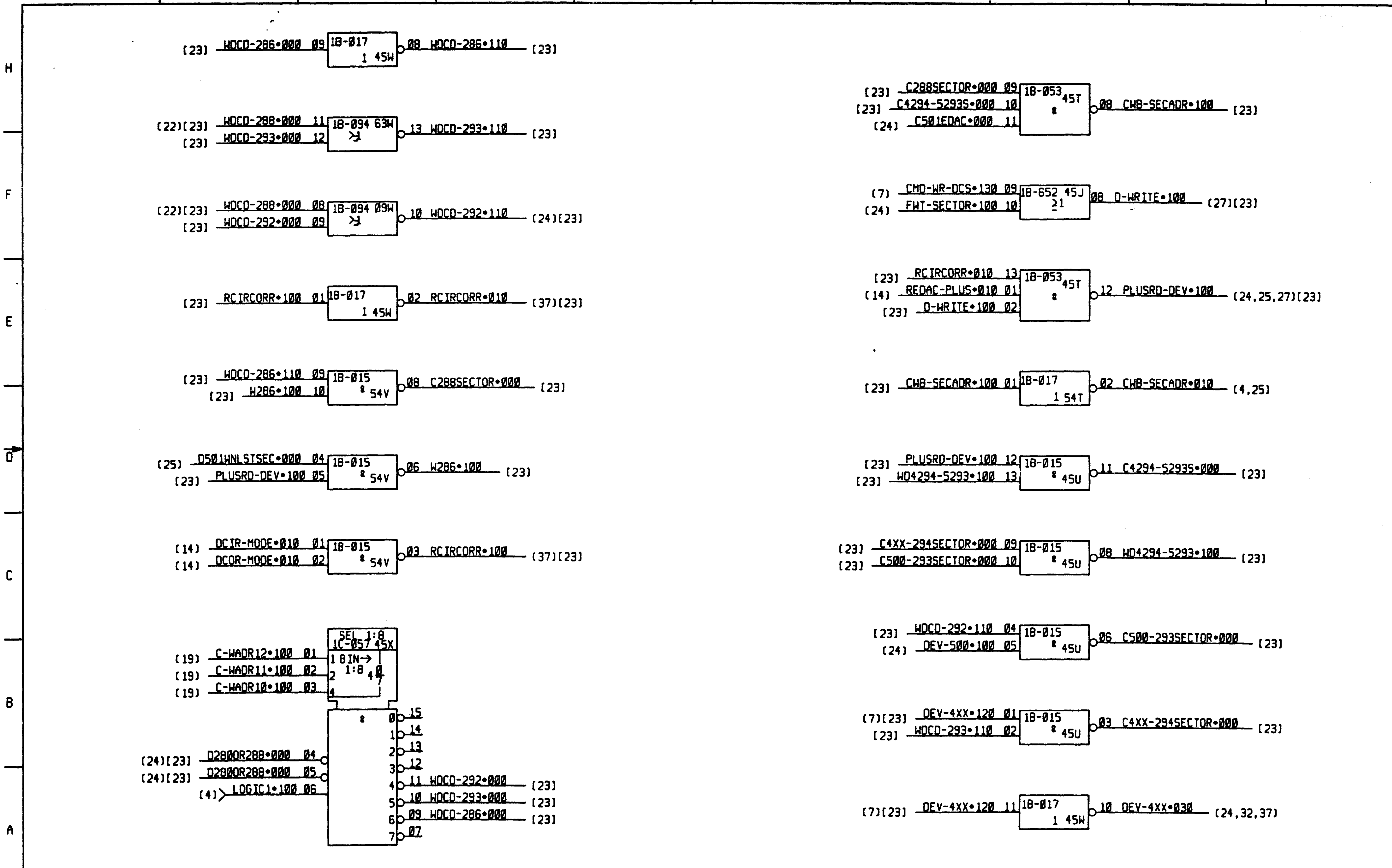


HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDASB

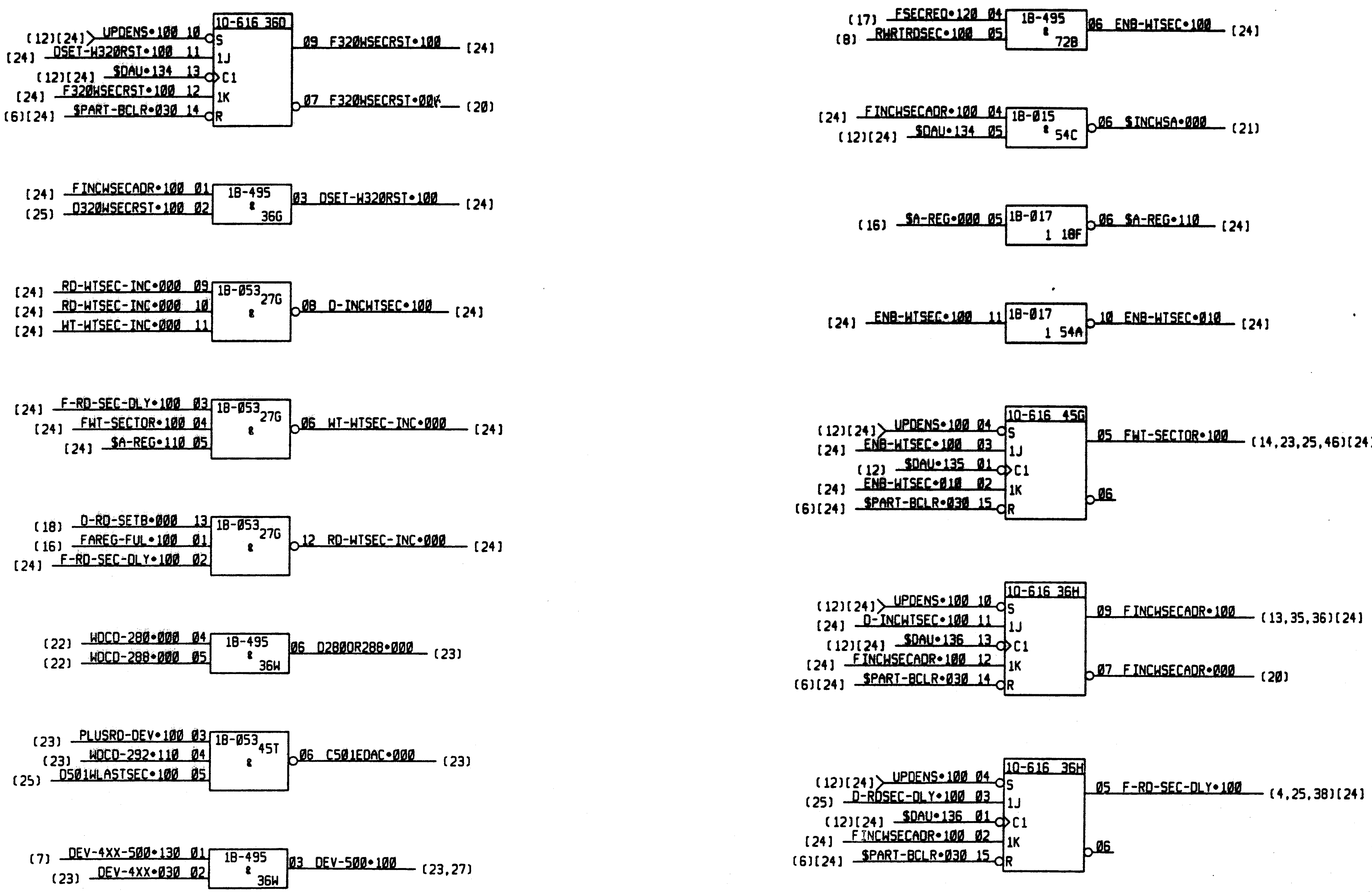
SIZE	DWG NO	SH	REV
B	58088874	22.0	C

58088874



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 23.0	REV C

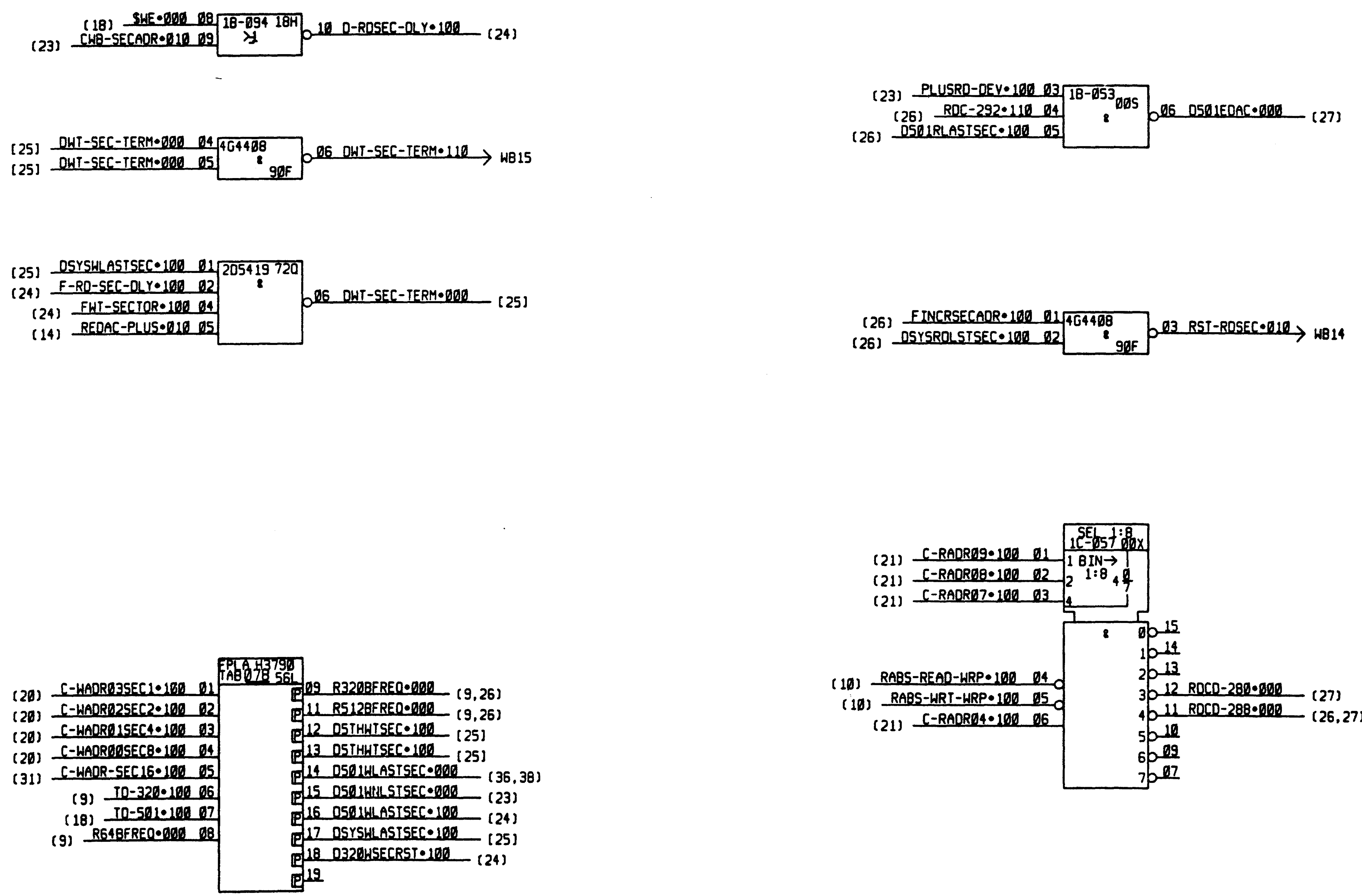
58088874



58088874

HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 24.0	REV C



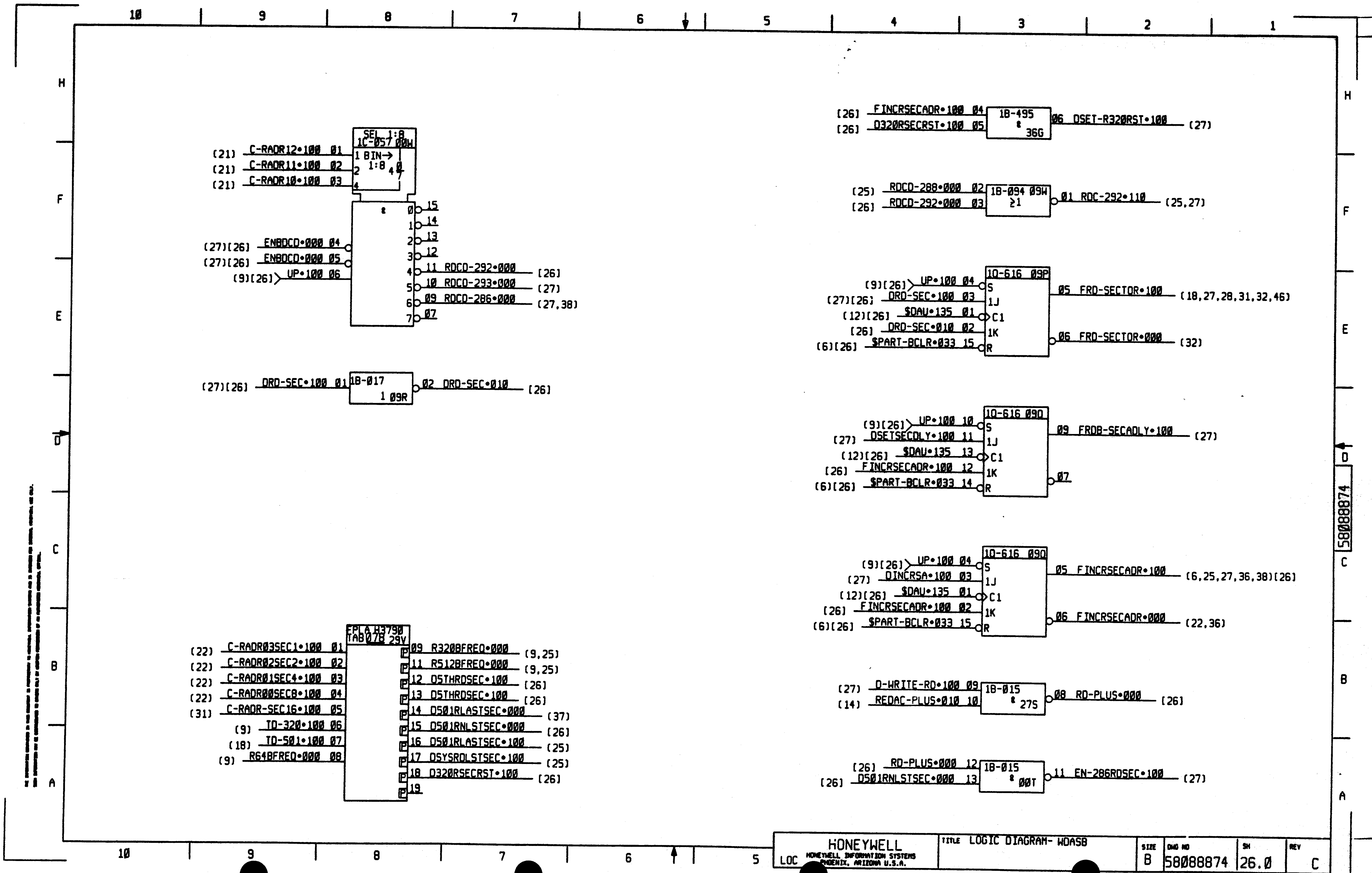
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

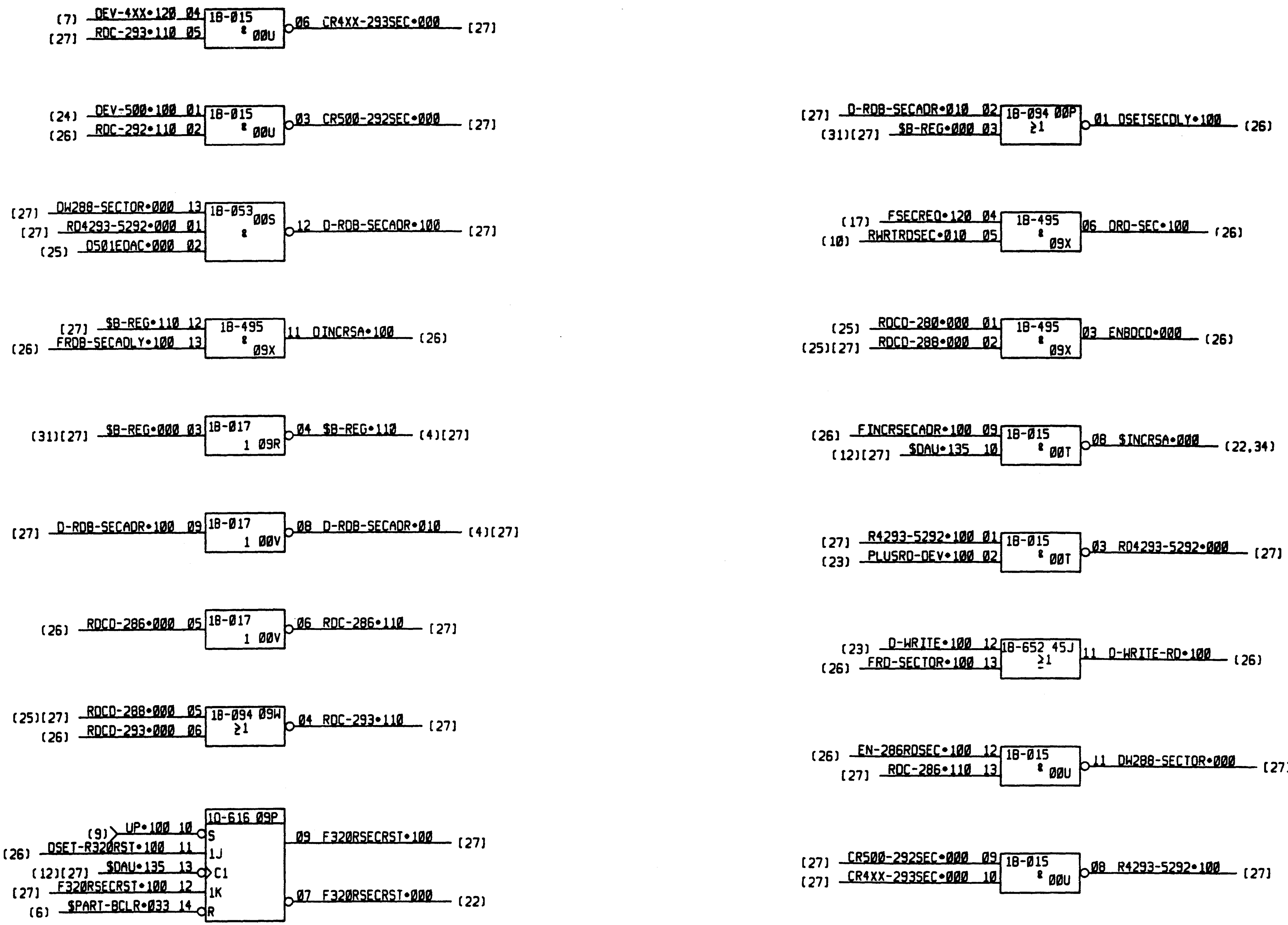
TITLE LOGIC DIAGRAM- WDASB

SIZE	DWG NO	SH	REV
B	58088874	25.0	C

58088874



SEL 1:8
1C-057 00W
1 BIN→
1:8
C-RADR12•100 01
C-RADR11•100 02
C-RADR10•100 03
ENBDCD•000 04
ENBDCD•000 05
UP•100 06
11 RDCD-292•000 [26]
10 RDCD-293•000 [27]
09 RDCD-286•000 [27,38]
DRD-SEC•100 01
1B-017
1 09R
02 DRD-SEC•010 [26]
EPLA H3790
TAB 078 29V
C-RADR03SEC1•100 01
C-RADR02SEC2•100 02
C-RADR01SEC4•100 03
C-RADR00SEC8•100 04
C-RADR-SEC16•100 05
TD-320•100 06
TD-501•100 07
R64BFREQ•000 08
09 R320BFREQ•000 [9,25]
11 R512BFREQ•000 [9,25]
12 D5THRDSEC•100 [26]
13 D5THRDSEC•100 [26]
14 D501RLASTSEC•000 [37]
15 D501RNLSTSEC•000 [26]
16 D501RLASTSEC•100 [25]
17 DSYSRDLSTSEC•100 [25]
18 D320RSECRST•100 [26]
19
[26] FINCRSECADR•100 04
[26] D320RSECRST•100 05
1B-495
36G
06 DSET-R320RST•100 [27]
[25] RDCD-288•000 02
[26] RDCD-292•000 03
1B-094 09W
≥1
01 RDC-292•110 [25,27]
1D-616 09P
[9][26] UP•100 04
[27][26] DRD-SEC•100 03
[12][26] $DAU•135 01
[26] DRD-SEC•010 02
[6][26] $PART-BCLR•033 15
05 FRD-SECTOR•100 [18,27,28,31,32,46]
06 FRD-SECTOR•000 [32]
1D-616 09Q
[9][26] UP•100 10
[27] DSETSECDLY•100 11
[12][26] $DAU•135 13
[26] FINCRSECADR•100 12
[6][26] $PART-BCLR•033 14
09 FRDB-SECADLY•100 [27]
07
1D-616 09Q
[9][26] UP•100 04
[27] DINCRSA•100 03
[12][26] $DAU•135 01
[26] FINCRSECADR•100 02
[6][26] $PART-BCLR•033 15
05 FINCRSECADR•100 [6,25,27,36,38][26]
06 FINCRSECADR•000 [22,36]
[27] D-WRITE-RD•100 09
[14] REDAC-PLUS•010 10
1B-015
27S
08 RD-PLUS•000 [26]
[26] RD-PLUS•000 12
[26] D501RNLSTSEC•000 13
1B-015
00T
11 EN-286RDSEC•100 [27]
58088874
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- WDASB
SIZE B
DWG NO 58088874
SH 26.0
REV C

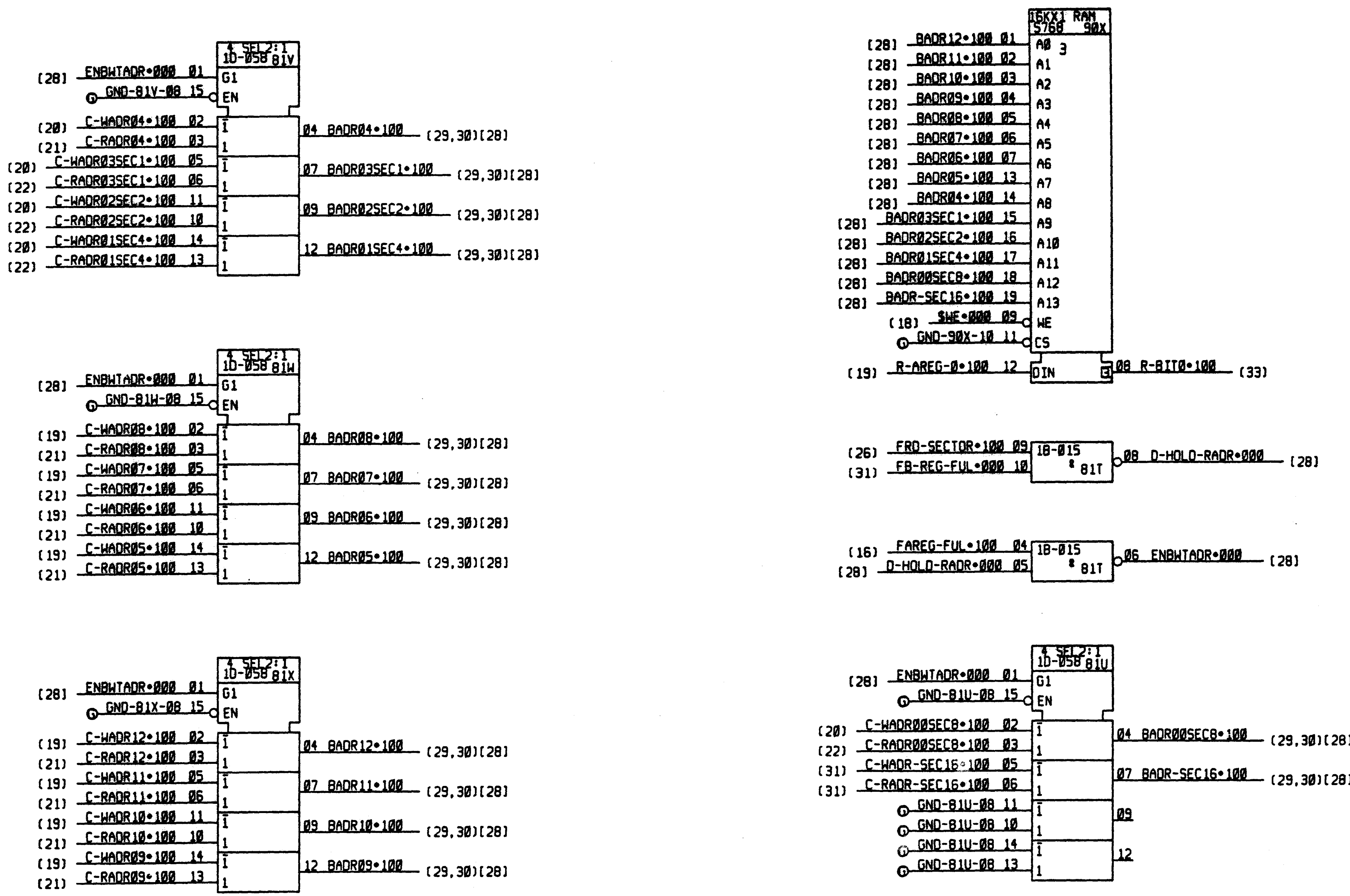


HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

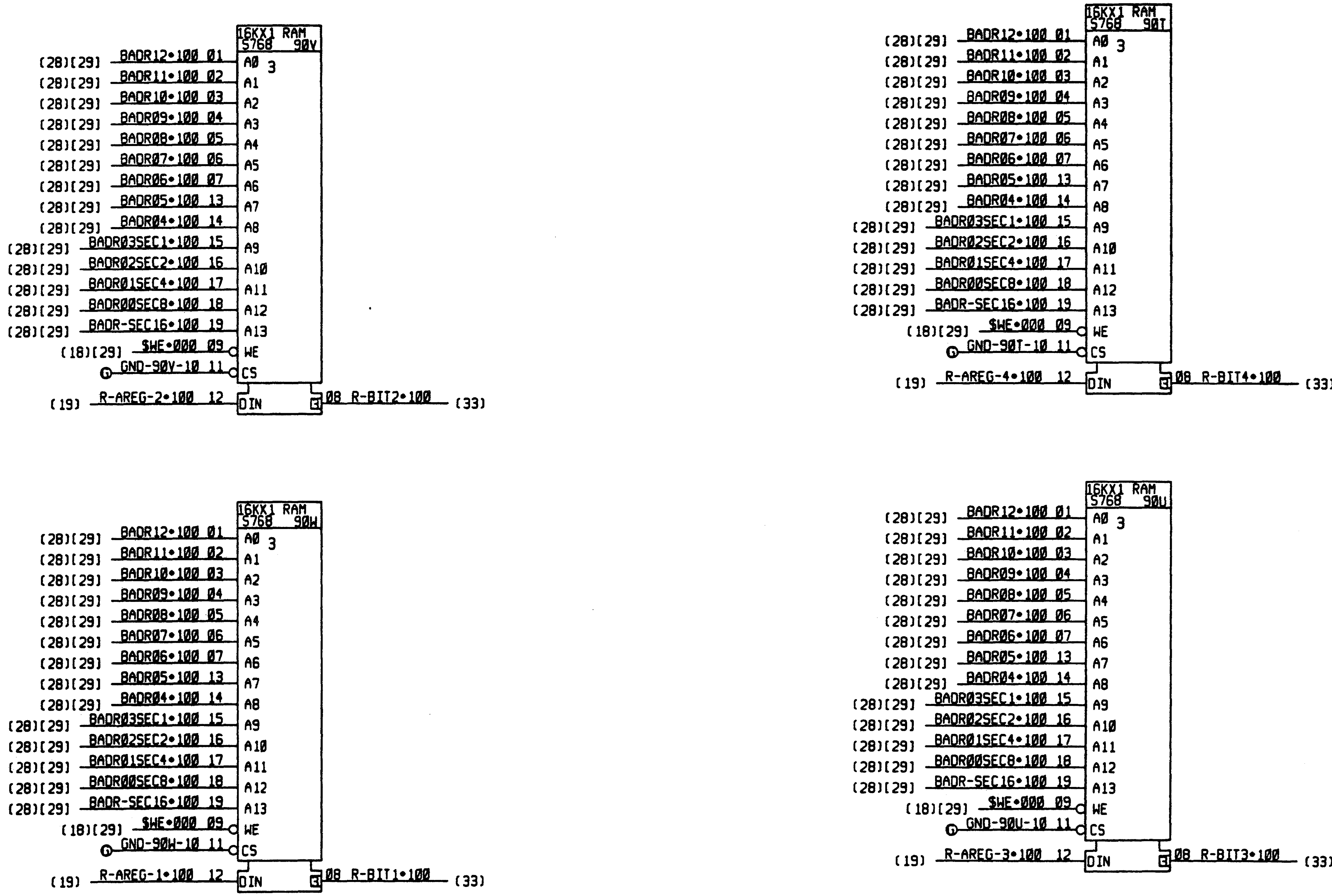
LOC

TITLE LOGIC DIAGRAM- WDASB

SIZE	DWG NO	SH	REV
B	58088874	27.0	C

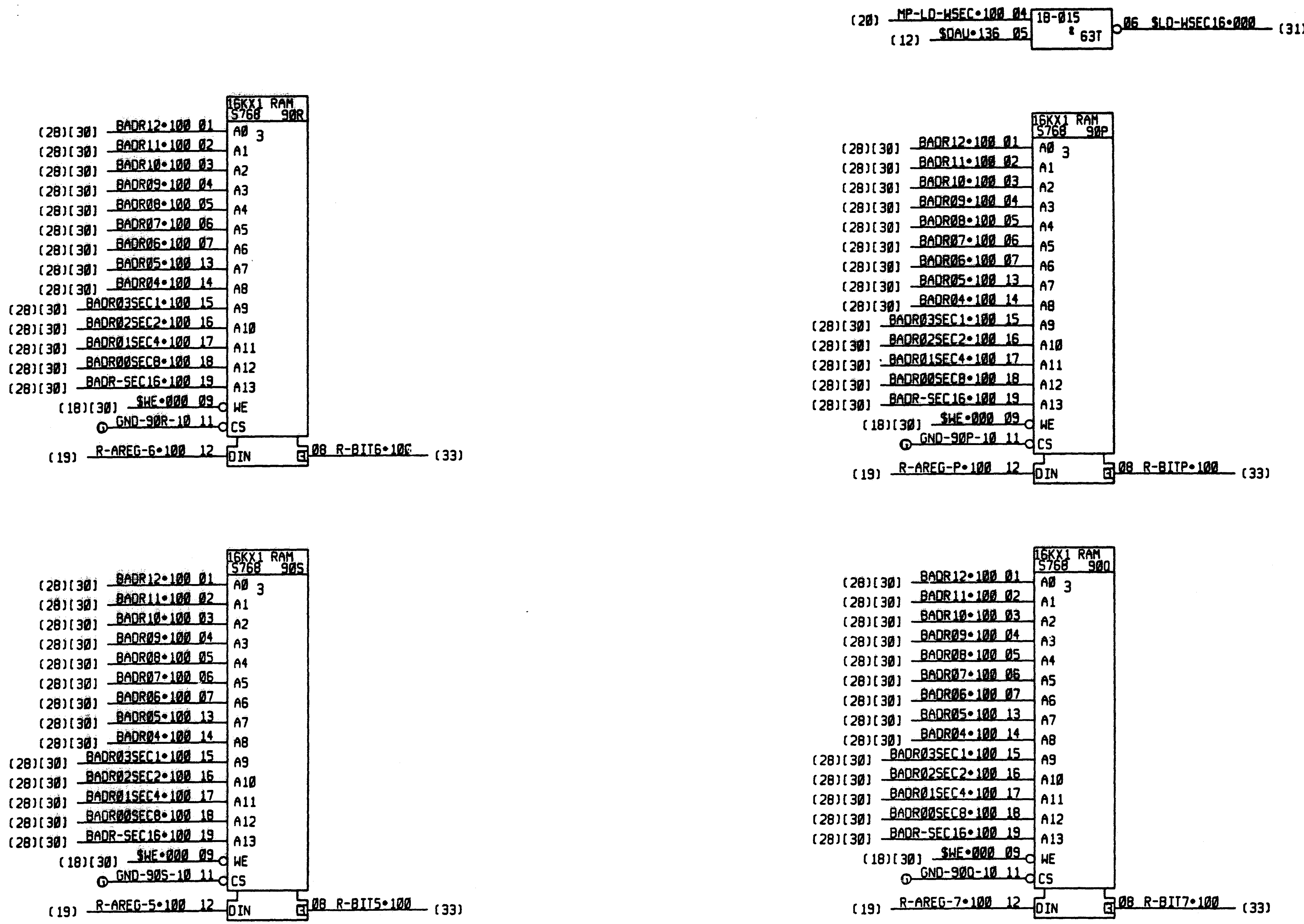


LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58Ø88874	SH 28.Ø	REV C



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 29.0	REV C

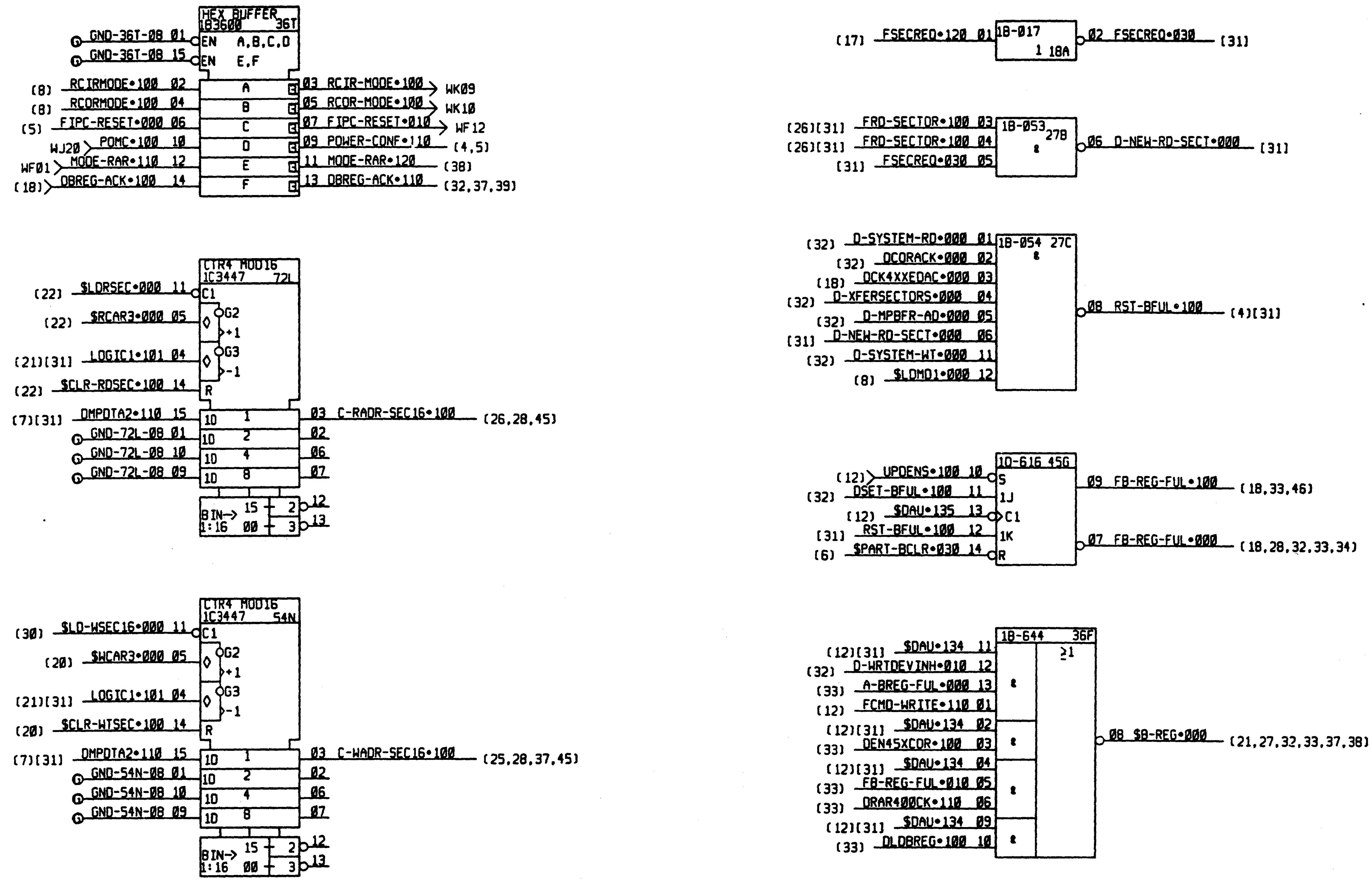
58088874



58088874

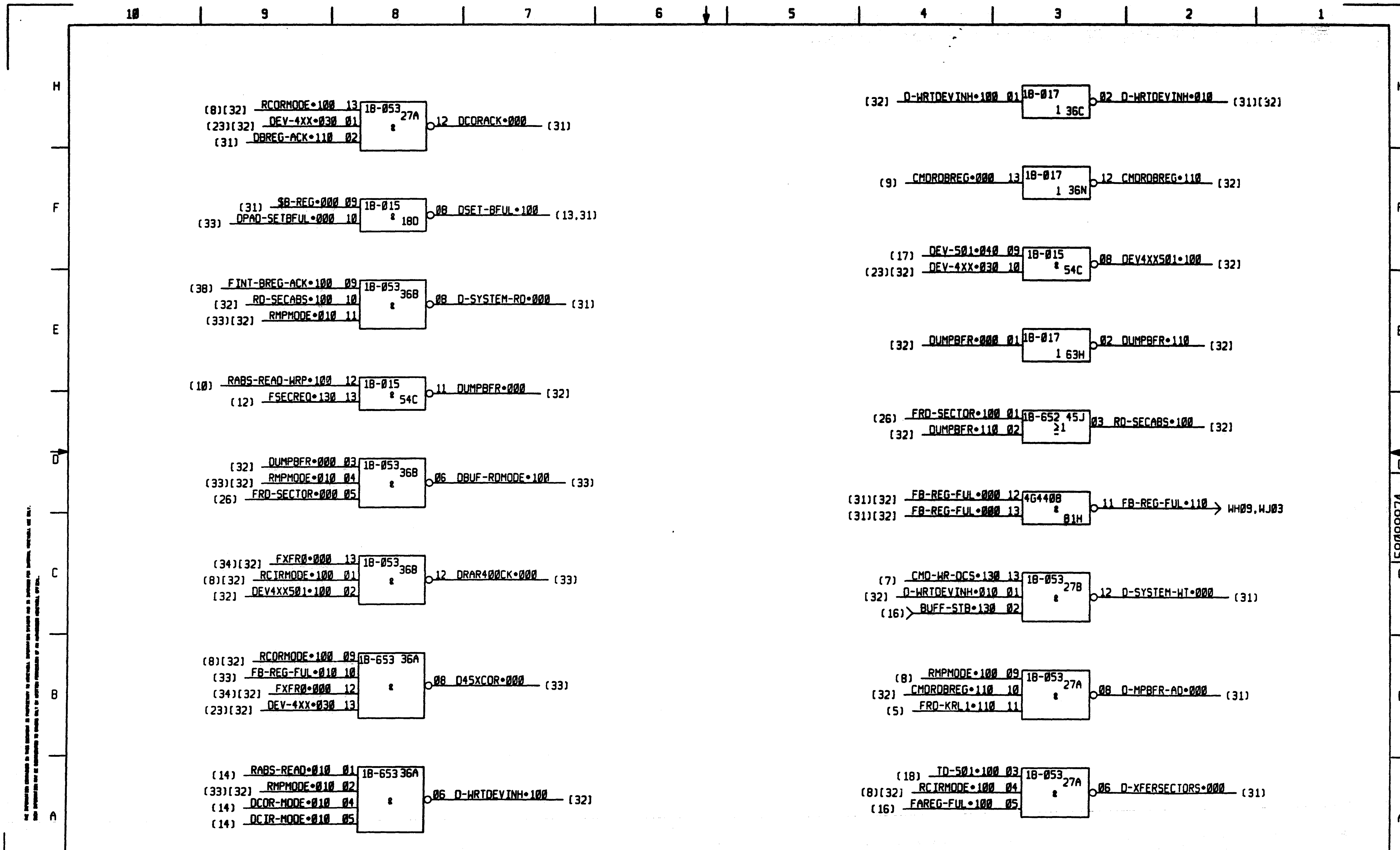
HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 30.0	REV C

LOC



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 31.0	REV C

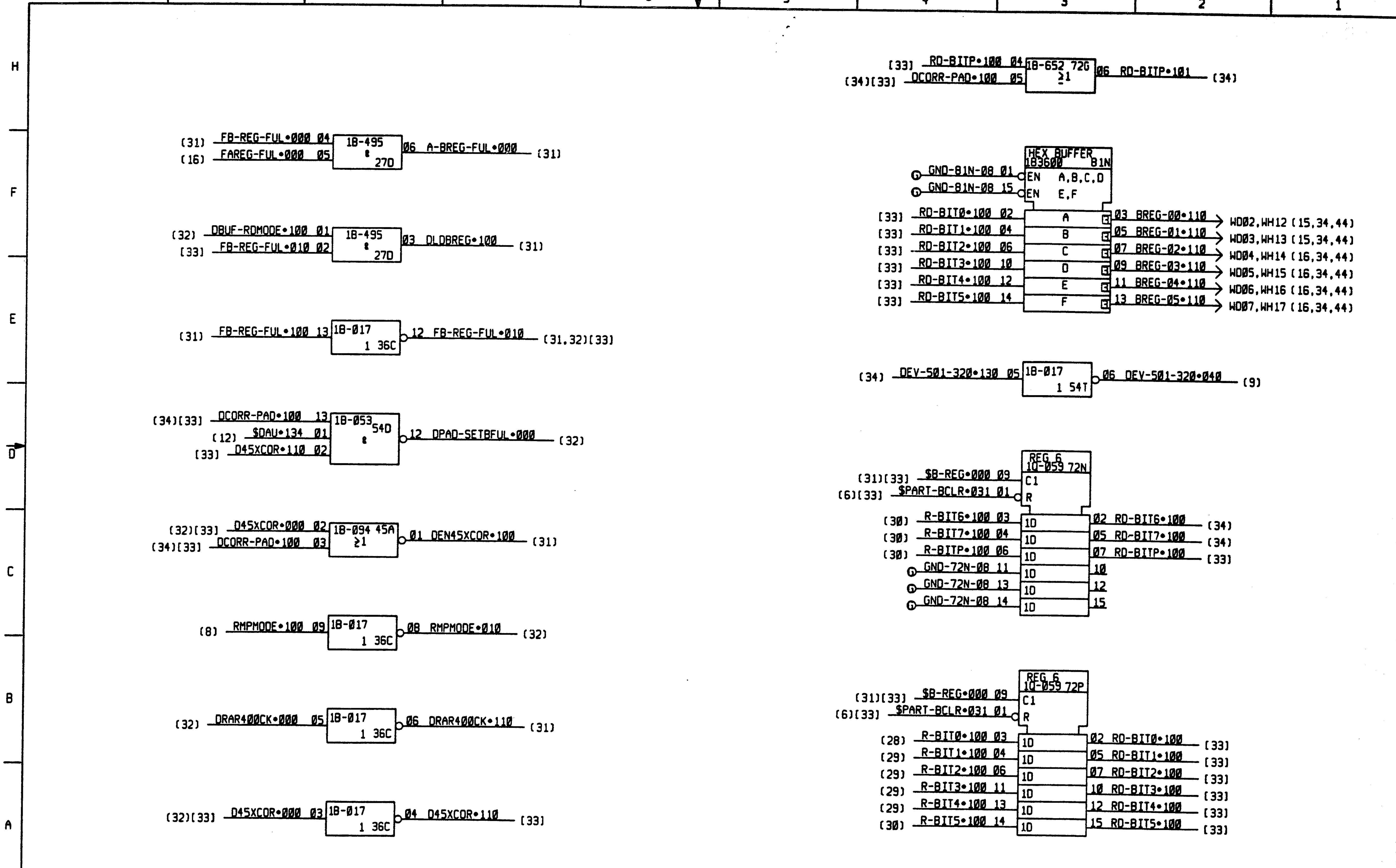
58088874



HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC

TITLE LOGIC DIAGRAM- WDASB

SIZE	DWG NO	SH	REV
B	58088874	32.0	C



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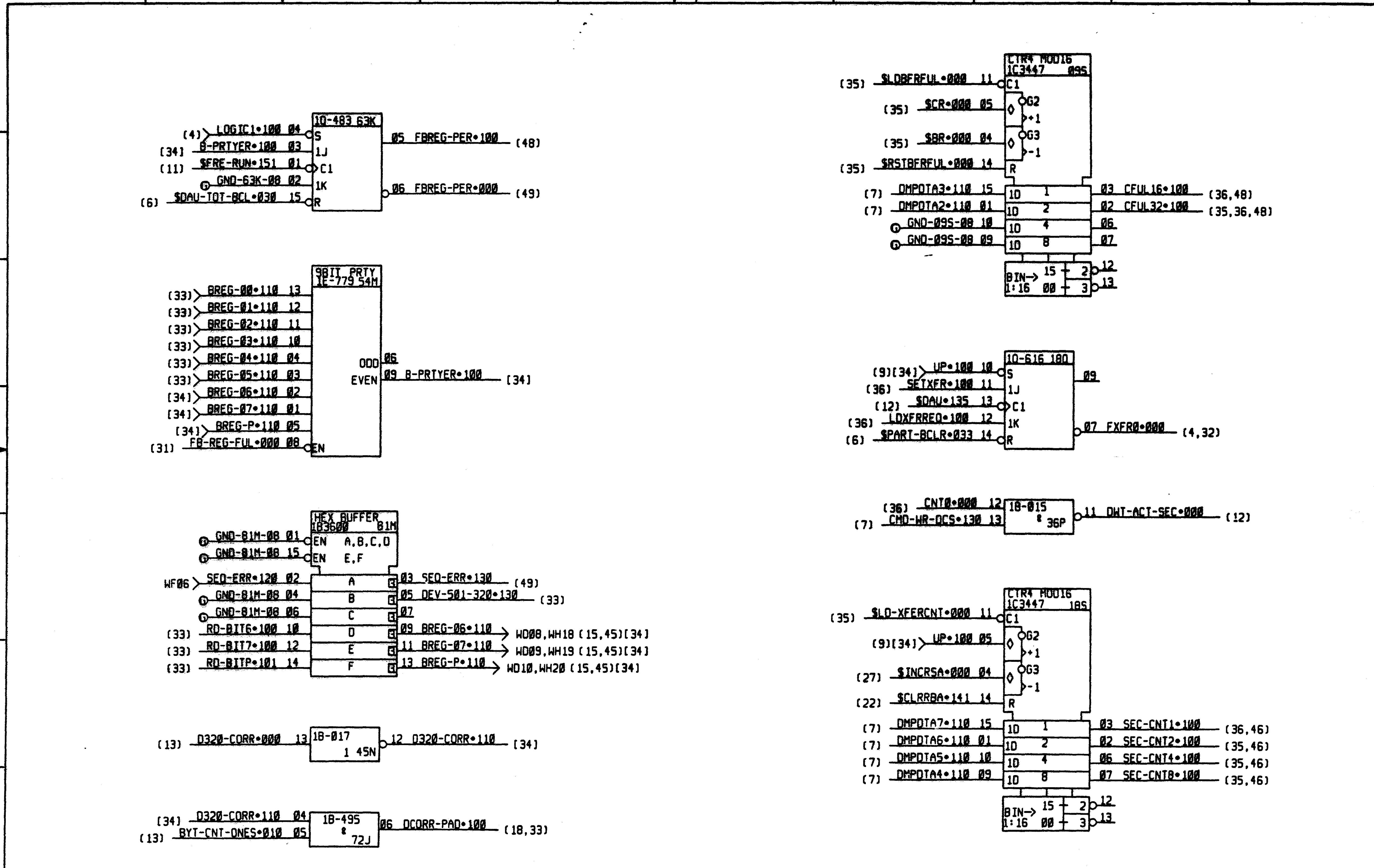
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

LOC

TITLE LOGIC DIAGRAM- WDASB

SIZE	DWG NO	SH	REV
B	58008874	33.0	C

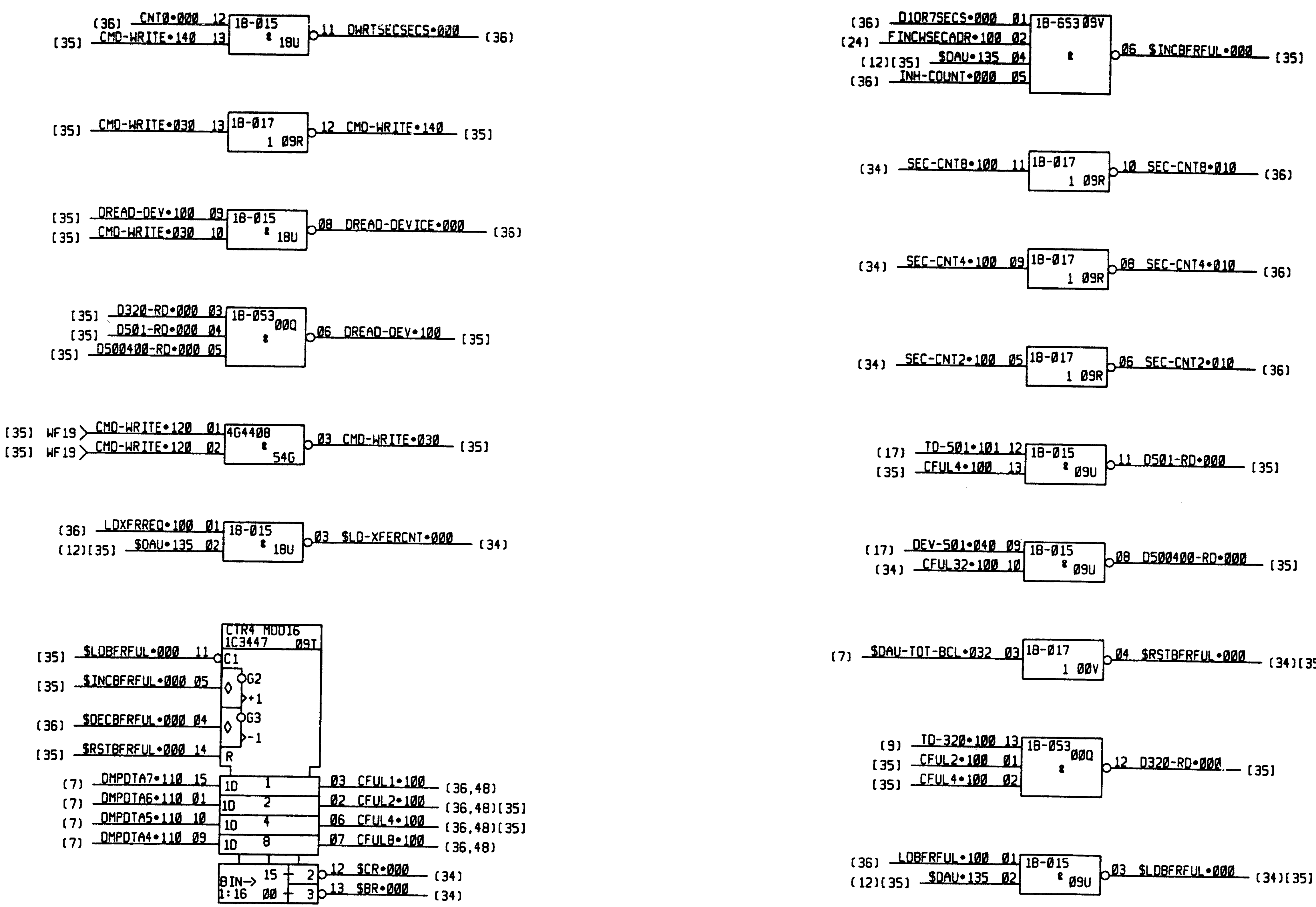
58008874



HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC

TITLE LOGIC DIAGRAM- WDASB

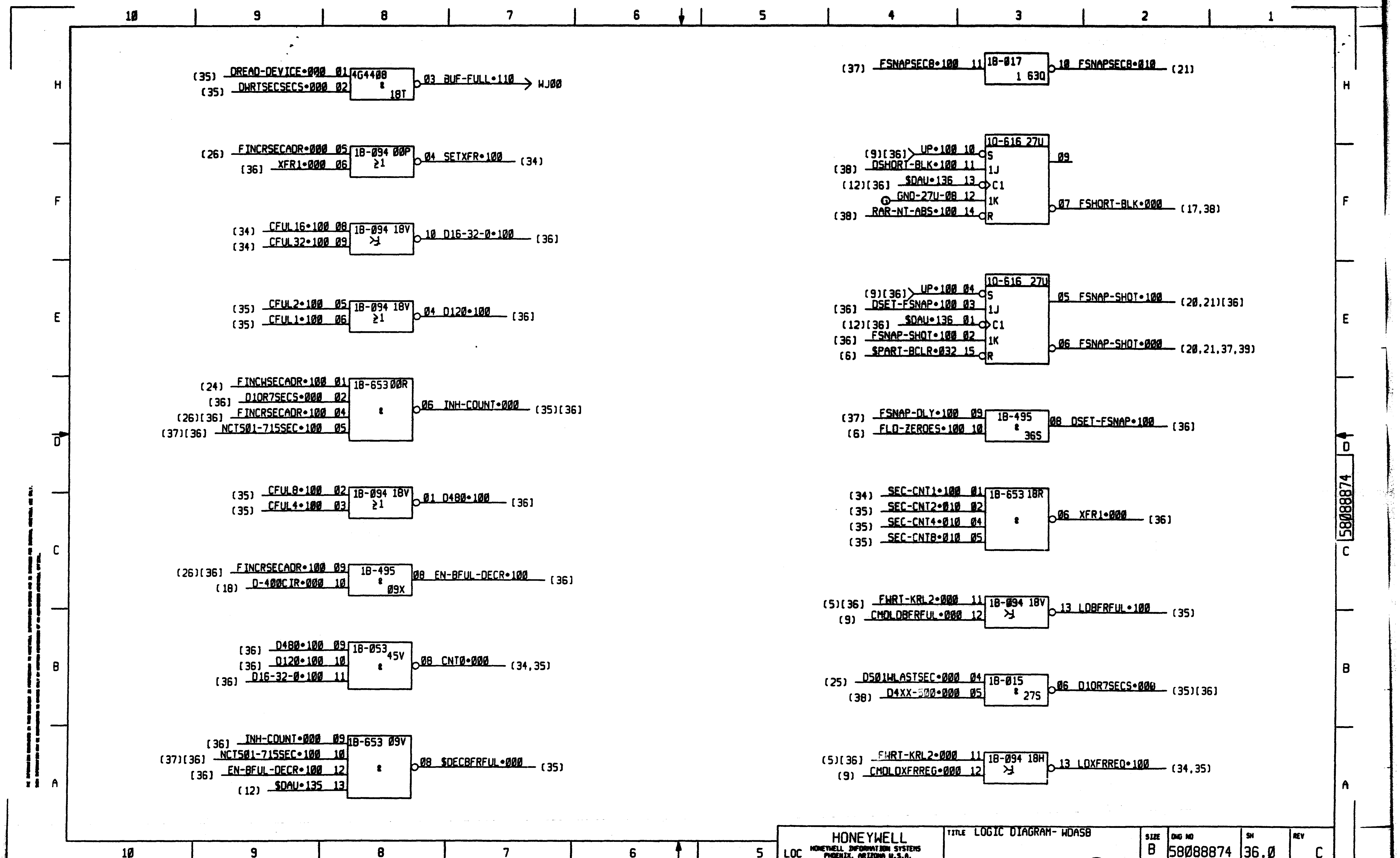
SIZE	DWG NO	SH	REV
B	58088874	34.0	C

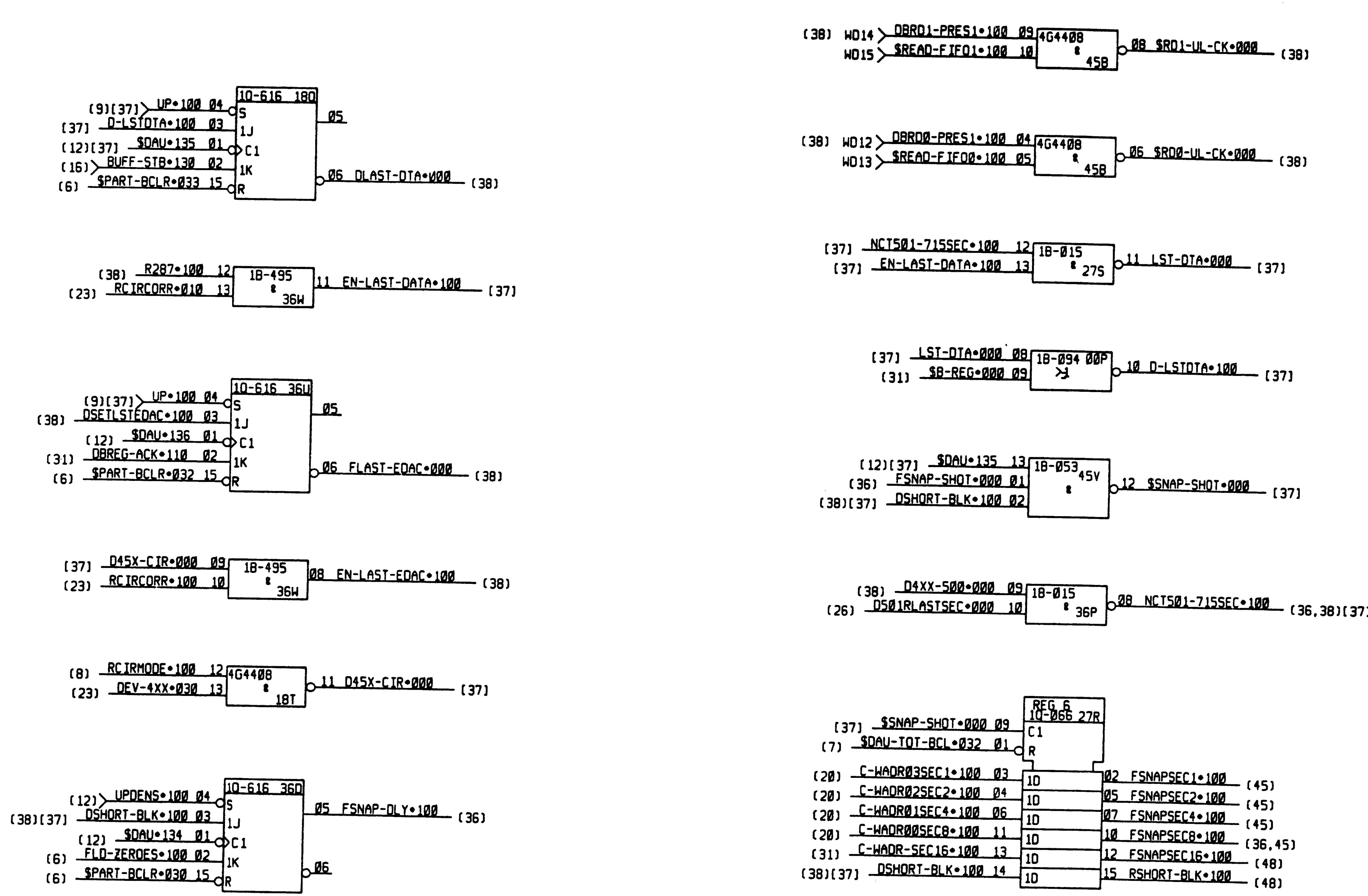


HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDASB

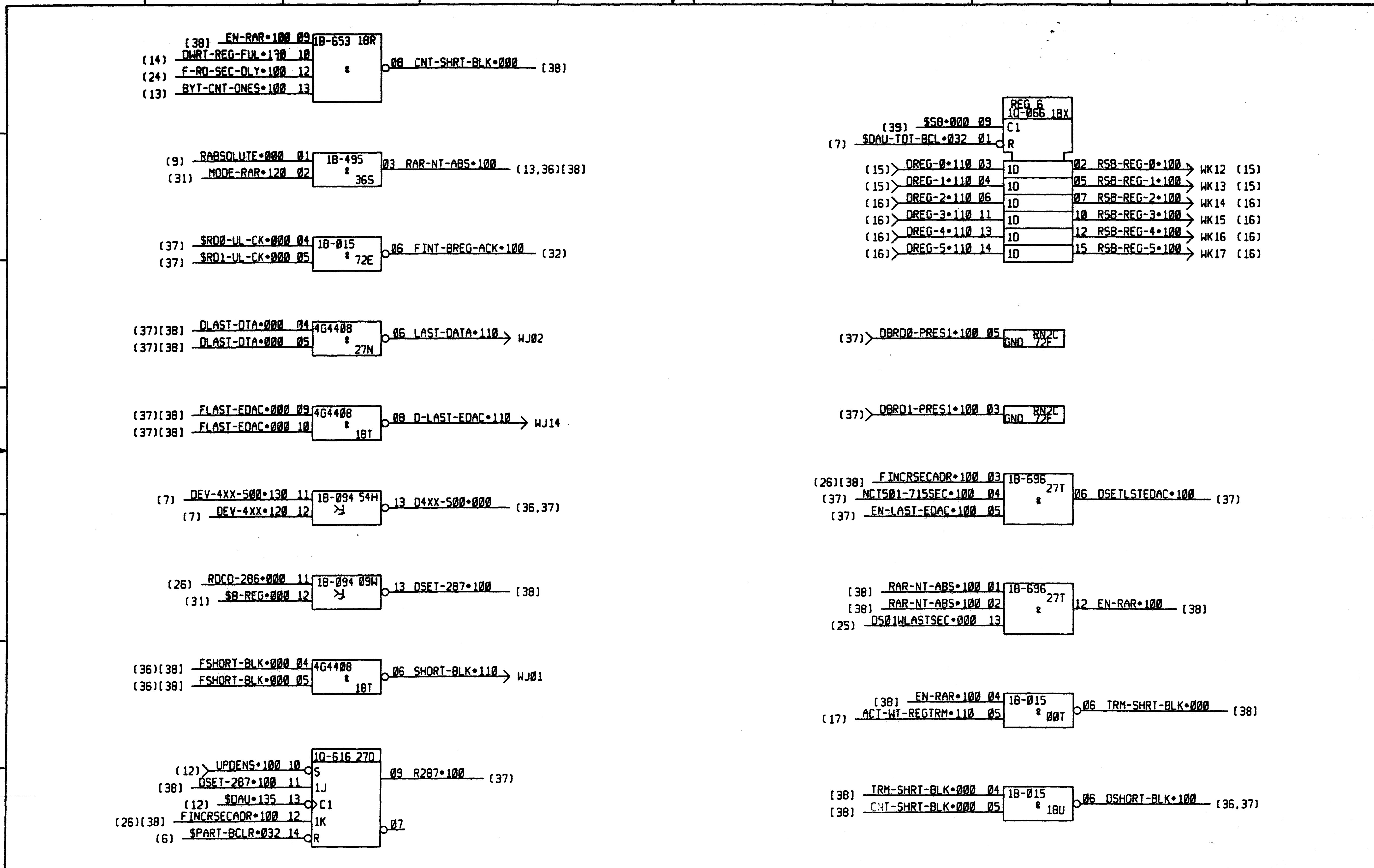
SIZE	DWG NO	SH	REV
B	58088874	35.0	C


(35) DREAD-DEVICE•000 01
(35) DWRTSECSECS•000 02
4G4408 & 18T
03 BUF-FULL•110
WJ00
(26) FINCRSECADR•000 05
(36) XFR1•000 06
1B-094 00P ≥1
04 SETXFR•100 (34)
(34) CFUL16•100 08
(34) CFUL32•100 09
1B-094 18V
10 D16-32-0•100 (36)
(35) CFUL2•100 05
(35) CFUL1•100 06
1B-094 18V ≥1
04 D120•100 (36)
(24) FINCWSECADR•100 01
(36) D1OR7SECS•000 02
(26)(36) FINCRSECADR•100 04
(37)(36) NCT501-715SEC•100 05
1B-653 00R &
06 INH-COUNT•000 (35)(36)
(35) CFUL8•100 02
(35) CFUL4•100 03
1B-094 18V ≥1
01 D480•100 (36)
(26)(36) FINCRSECADR•100 09
(18) D-400CIR•000 10
1B-495 & 09X
08 EN-BFUL-DECR•100 (36)
(36) D480•100 09
(36) D120•100 10
(36) D16-32-0•100 11
1B-053 45V &
08 CNT0•000 (34,35)
(36) INH-COUNT•000 09
(37)(36) NCT501-715SEC•100 10
(36) EN-BFUL-DECR•100 12
(12) $DAU•135 13
1B-653 09V &
08 $DECBFRFUL•000 (35)
(37) FSNAPSEC8•100 11
1B-017 1 63Q
10 FSNAPSEC8•010 (21)
10-616 27U
(9)(36) UP•100 10 S
(38) DSHORT-BLK•100 11 1J
(12)(36) $DAU•136 13 C1
GND-27U-08 12 1K
(38) RAR-NT-ABS•100 14 R
09
07 FSHORT-BLK•000 (17,38)
10-616 27U
(9)(36) UP•100 04 S
(36) DSET-FSNAP•100 03 1J
(12)(36) $DAU•136 01 C1
(36) FSNAP-SHOT•100 02 1K
(6) $PART-BCLR•032 15 R
05 FSNAP-SHOT•100 (20,21)(36)
06 FSNAP-SHOT•000 (20,21,37,39)
(37) FSNAP-DLY•100 09
(6) FLD-ZEROES•100 10
1B-495 & 36S
08 DSET-FSNAP•100 (36)
(34) SEC-CNT1•100 01
(35) SEC-CNT2•010 02
(35) SEC-CNT4•010 04
(35) SEC-CNT8•010 05
1B-653 18R &
06 XFR1•000 (36)
(5)(36) FWRT-KRL2•000 11
(9) CMDLDBFRFUL•000 12
1B-094 18V
13 LDBFRFUL•100 (35)
(25) D501WLASTSEC•000 04
(38) D4XX-500•000 05
1B-015 & 27S
06 D1OR7SECS•000 (35)(36)
(5)(36) FWRT-KRL2•000 11
(9) CMDLDXFRREQ•000 12
1B-094 18H
13 LDXFRREQ•100 (34,35)
58088874
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- WDASB
SIZE B
DWG NO 58088874
SH 36.0
REV C



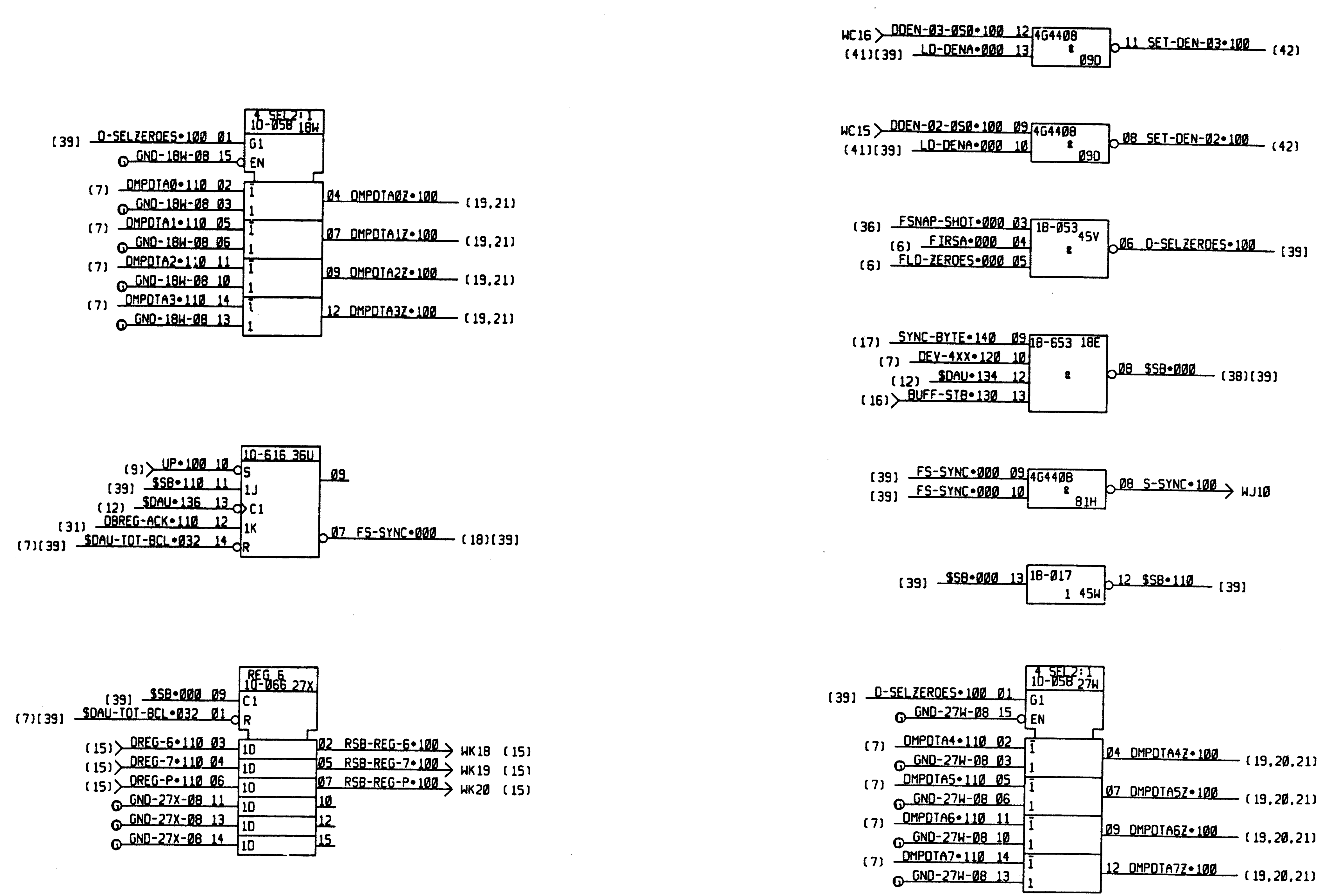
LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 37.0	REV C

58088874



HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 38.0	REV C

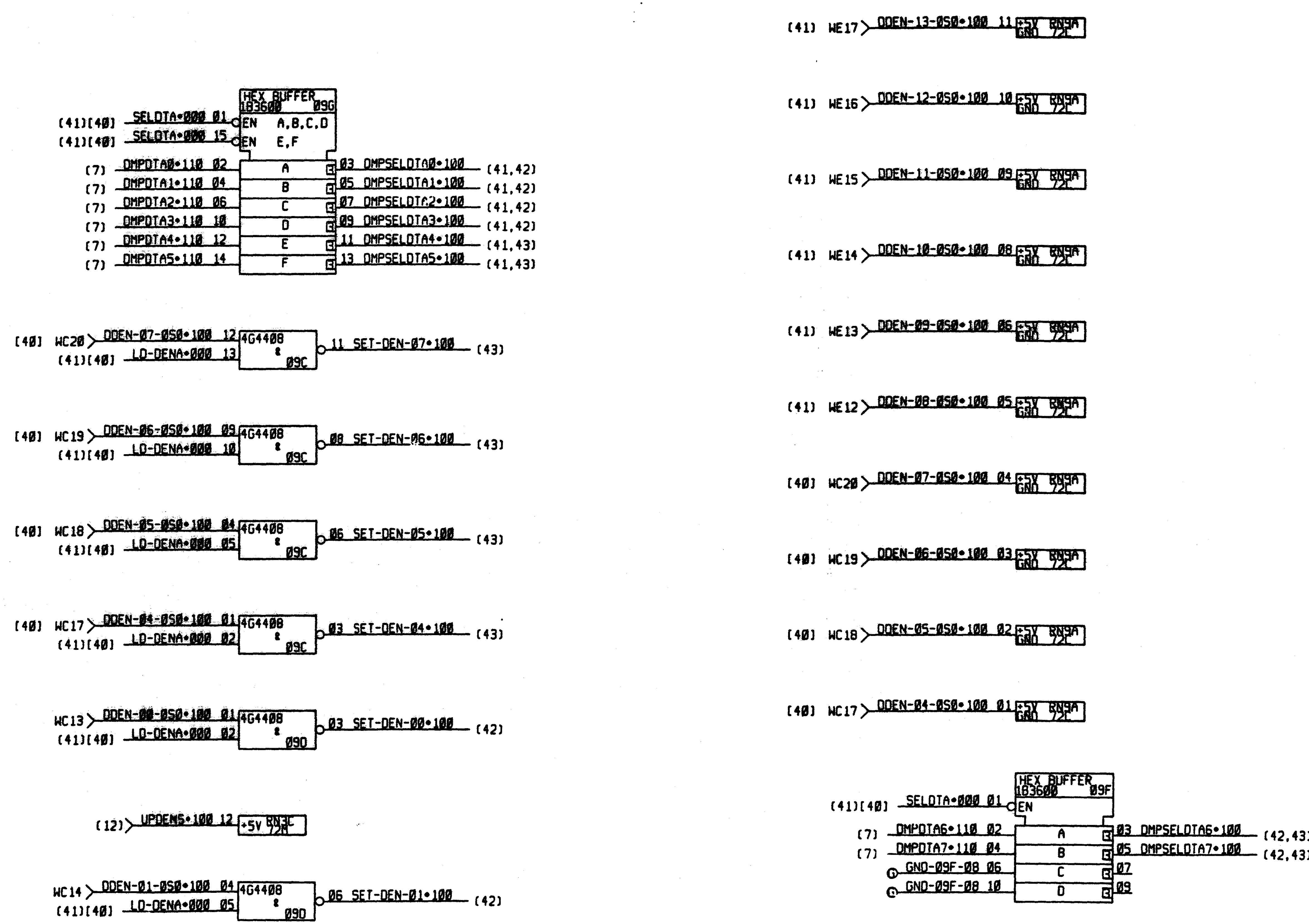
58088874



HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDASB

LOC	SIZE	DWG NO	SH	REV
	B	58088874	39.0	C

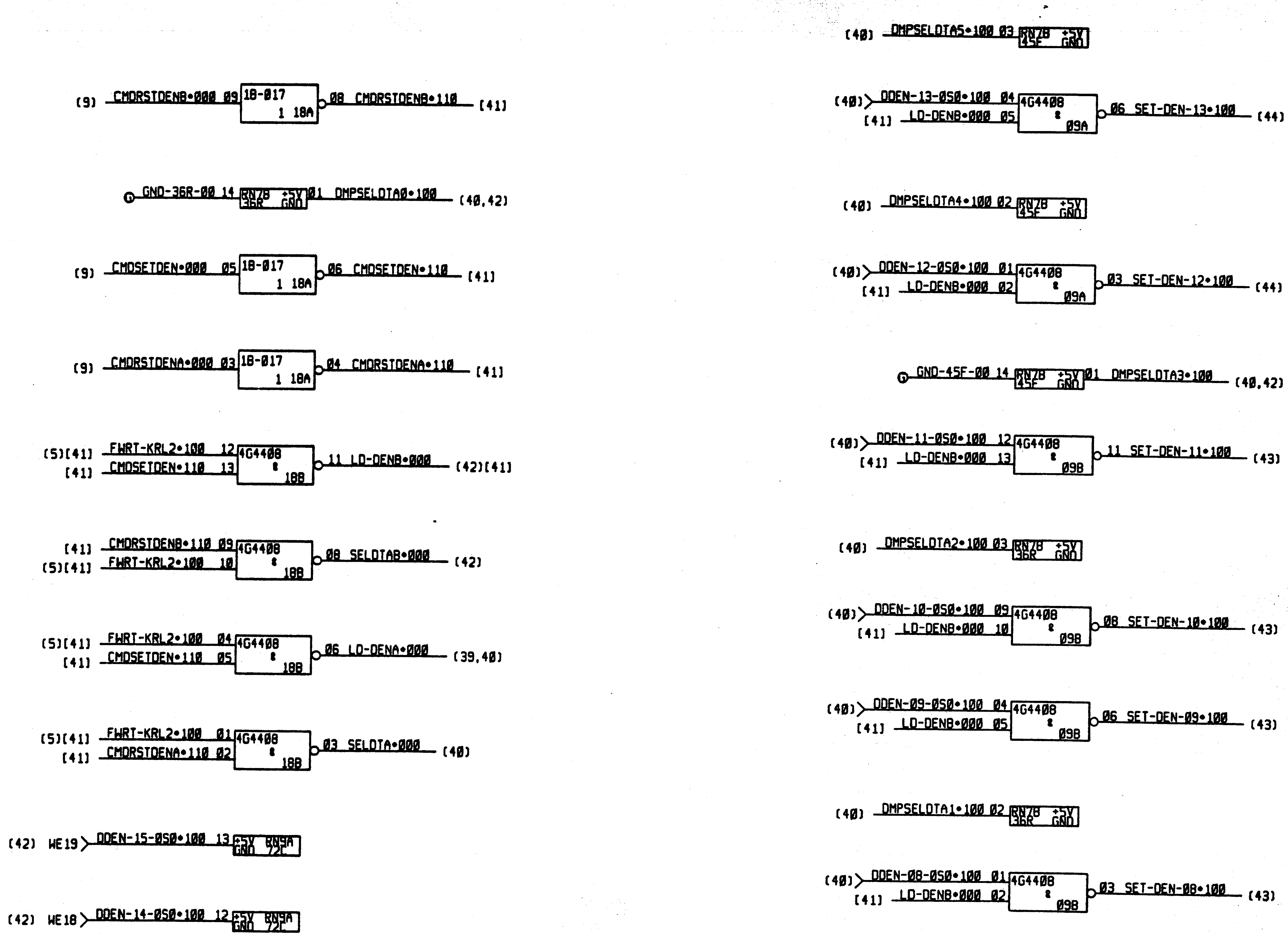


58088874

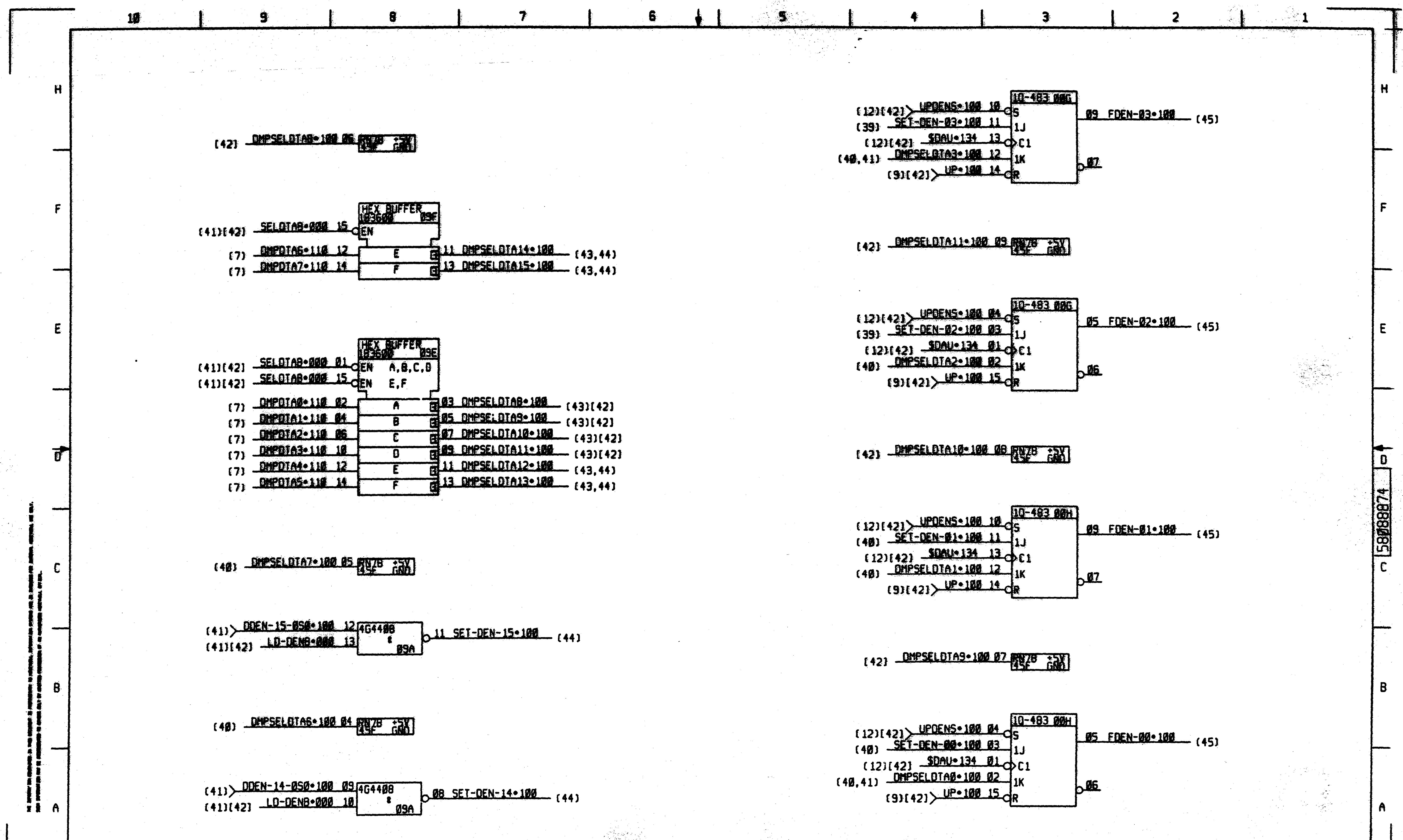
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC

TITLE LOGIC DIAGRAM- WDASB

SIZE	DWG NO	SH	REV
B	58088874	40.0	C



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 41.0	REV C

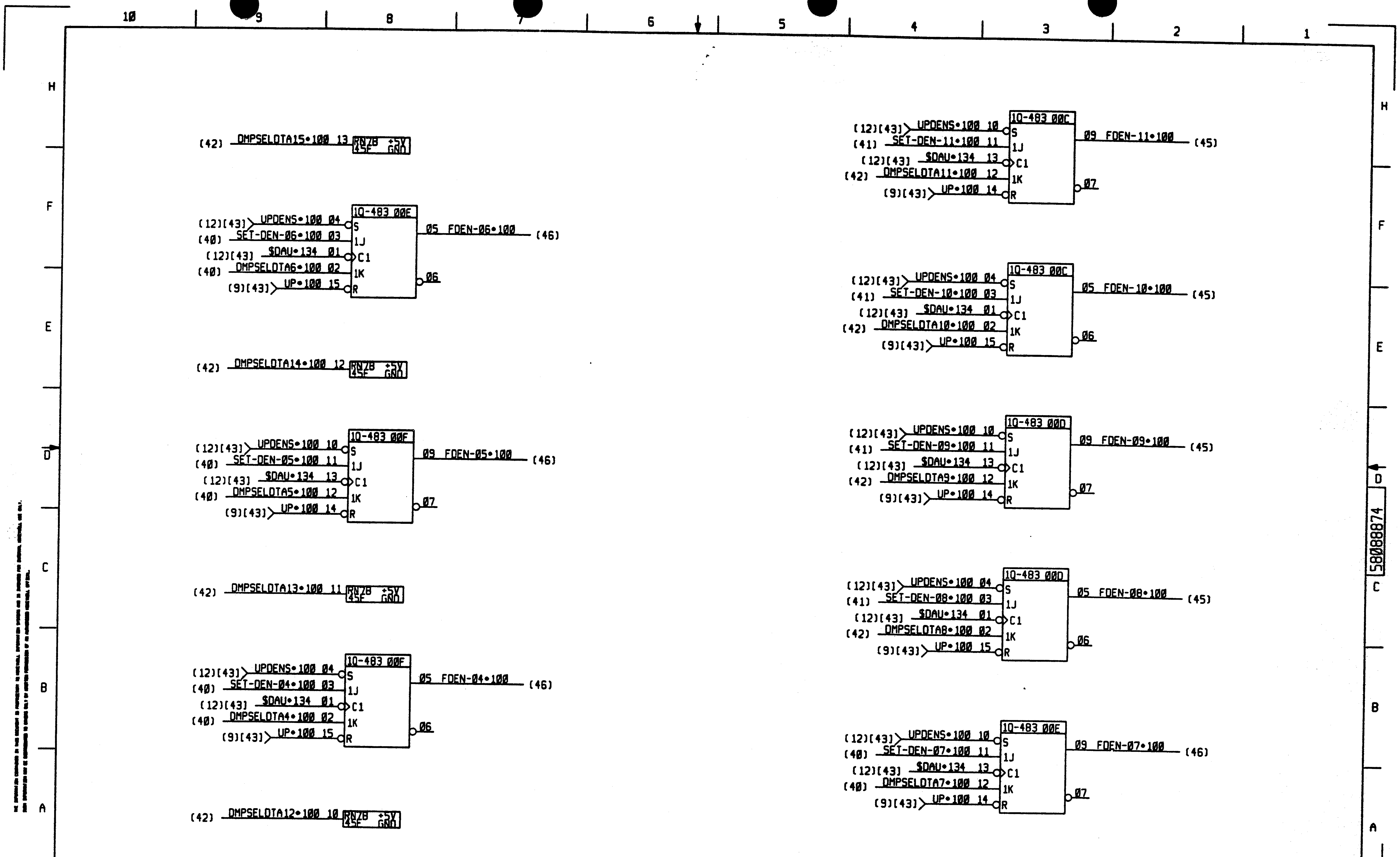


HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

TITLE LOGIC DIAGRAM- WDASB

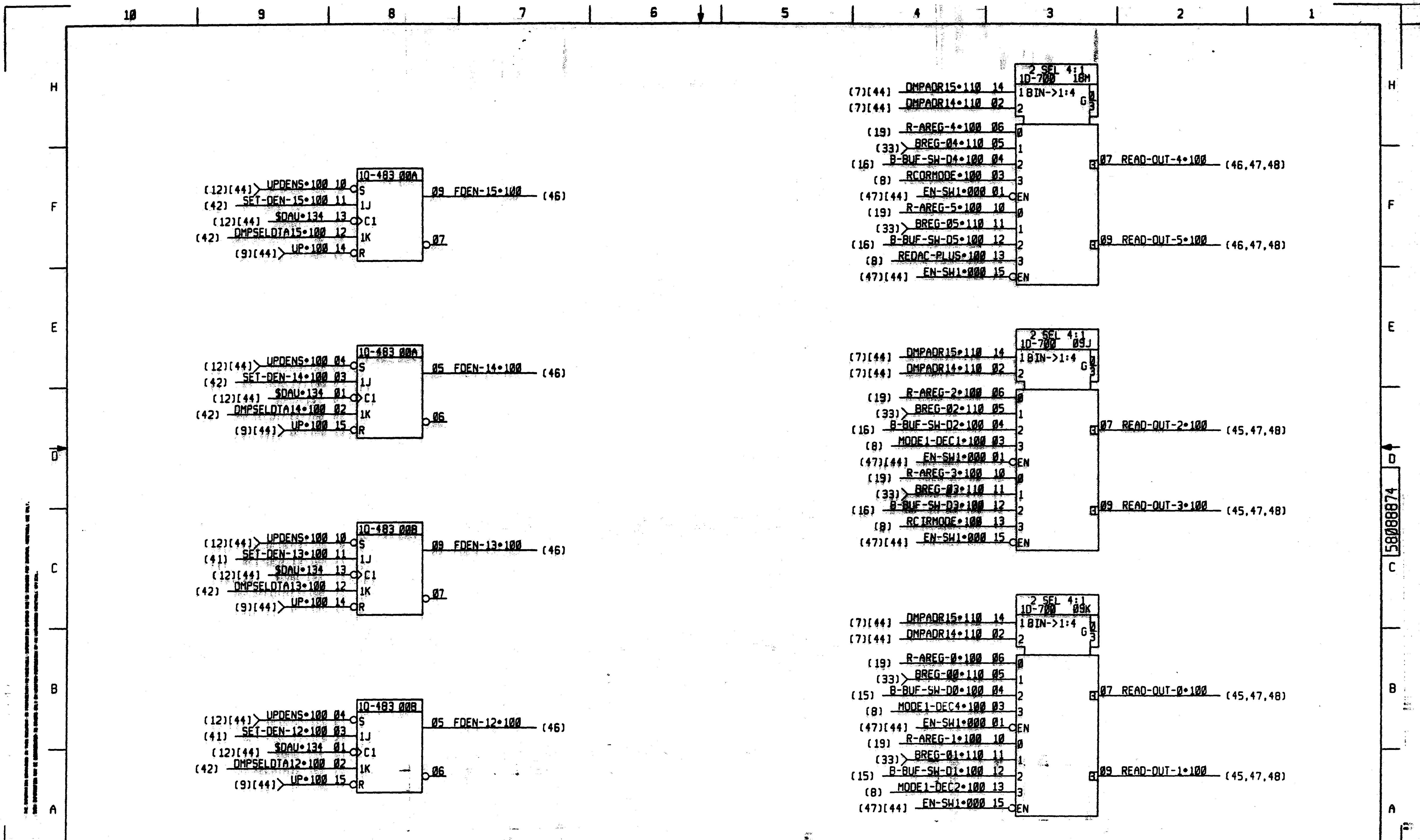
SIZE	DWG NO	SH	REV
B	58088874	42 0	C



LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDASB

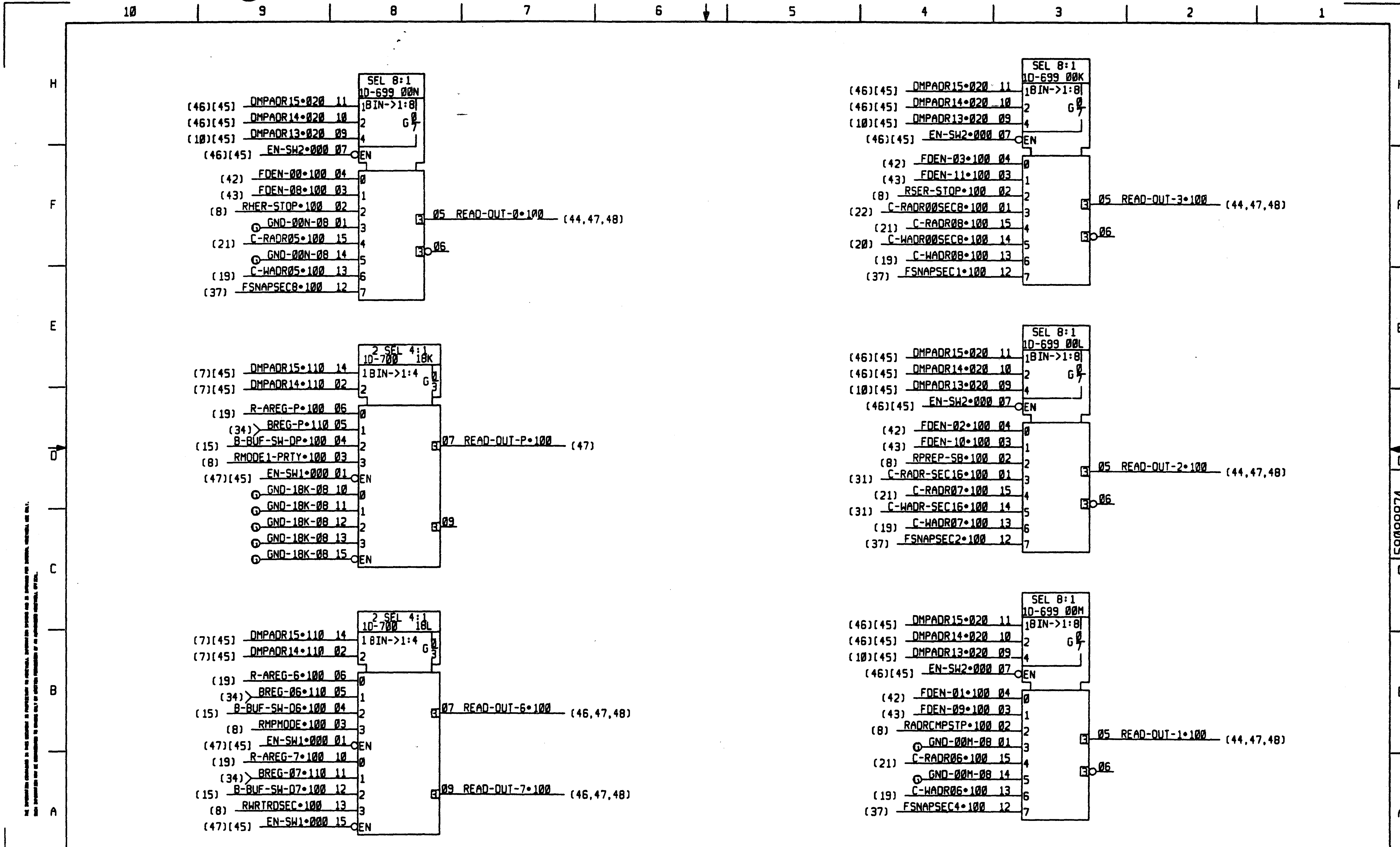
SIZE B | DWG NO 58088874 | SH 43.0 | REV C



HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC

TITLE LOGIC DIAGRAM- WDASB

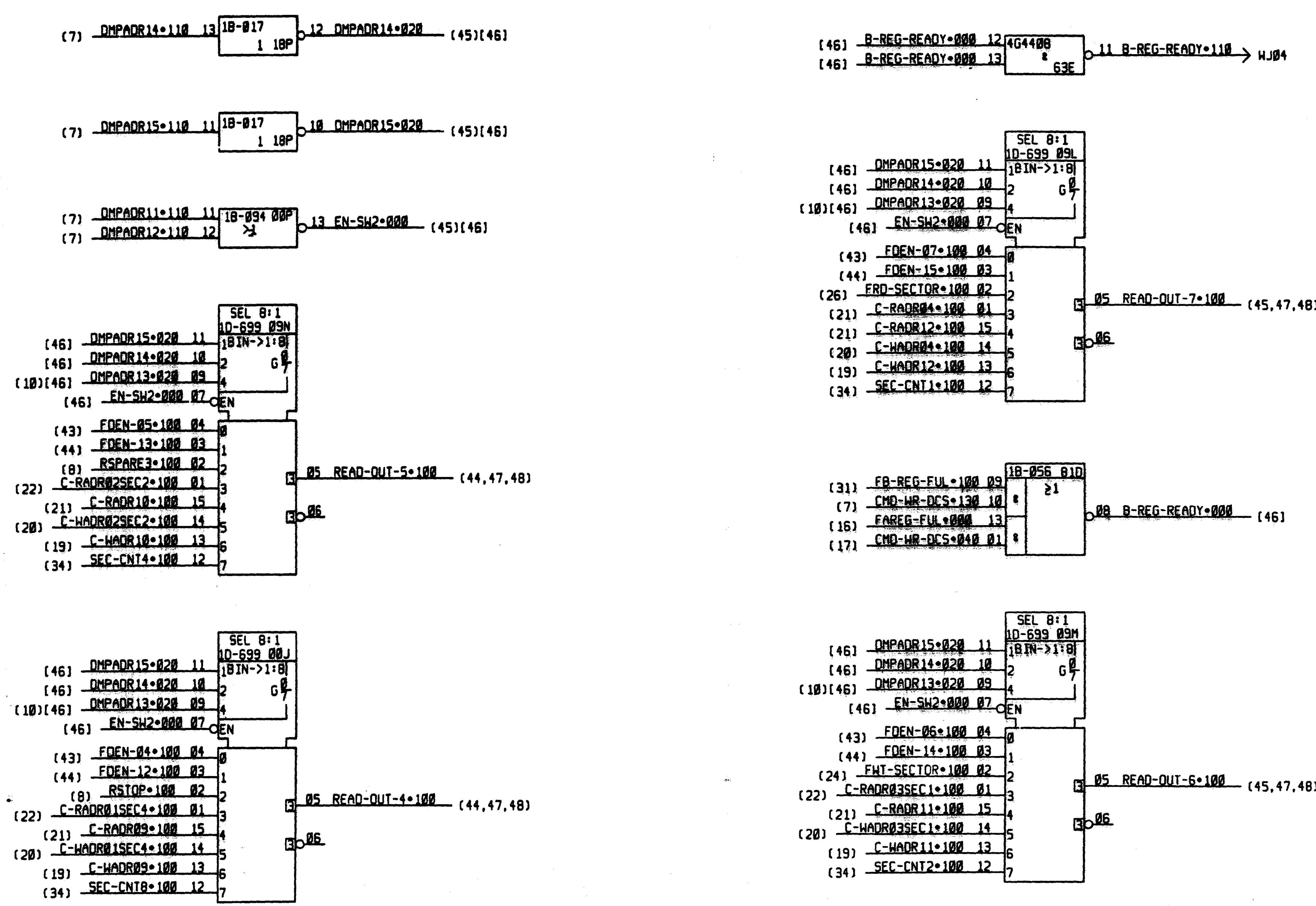
SIZE	DWG NO	SH	REV
B	58088874	44.0	C



HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

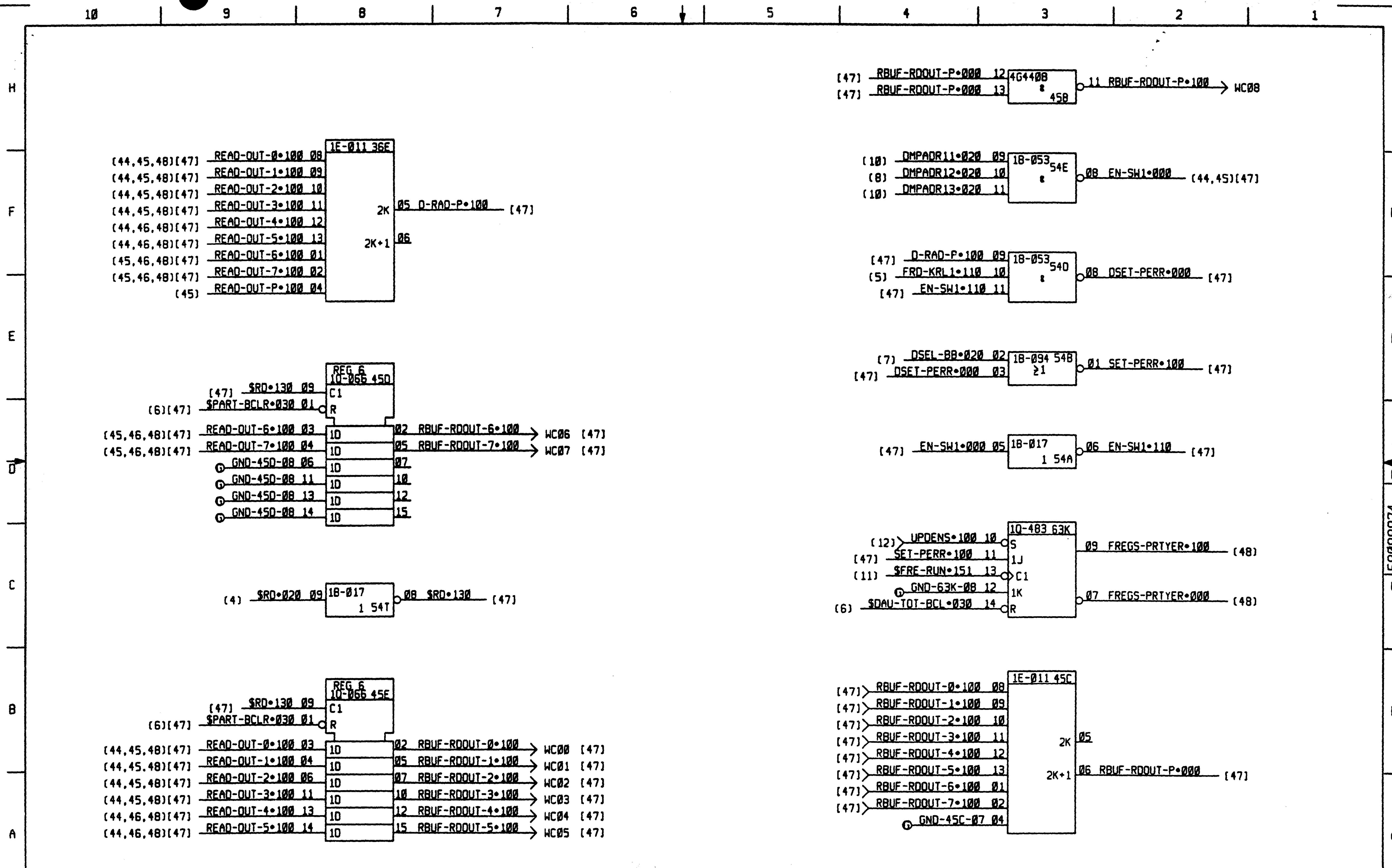
TITLE LOGIC DIAGRAM- WDASB

SIZE	DWG NO	SH	REV
B	58088874	45.0	C



HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 46.0	REV C

LOC

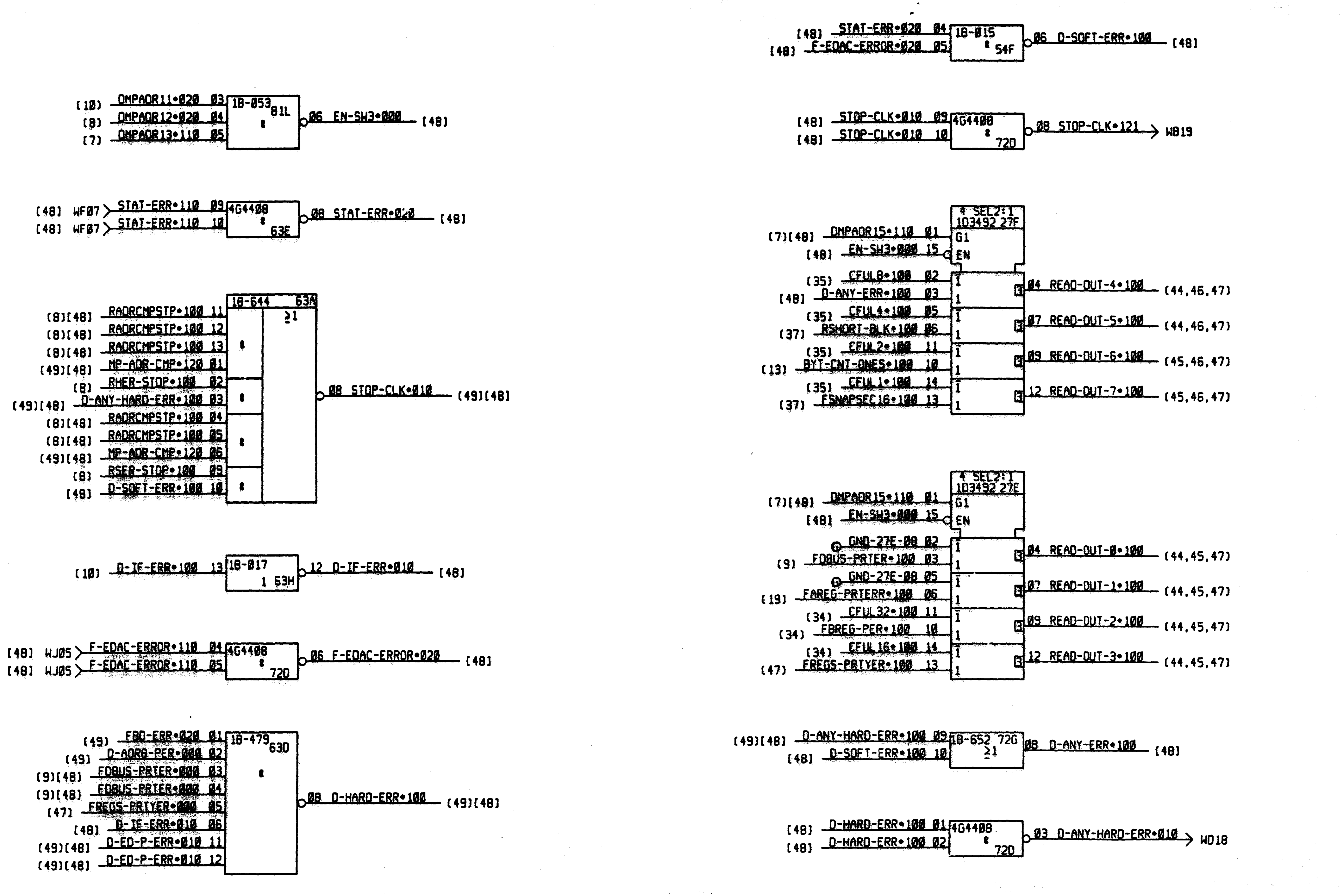


HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

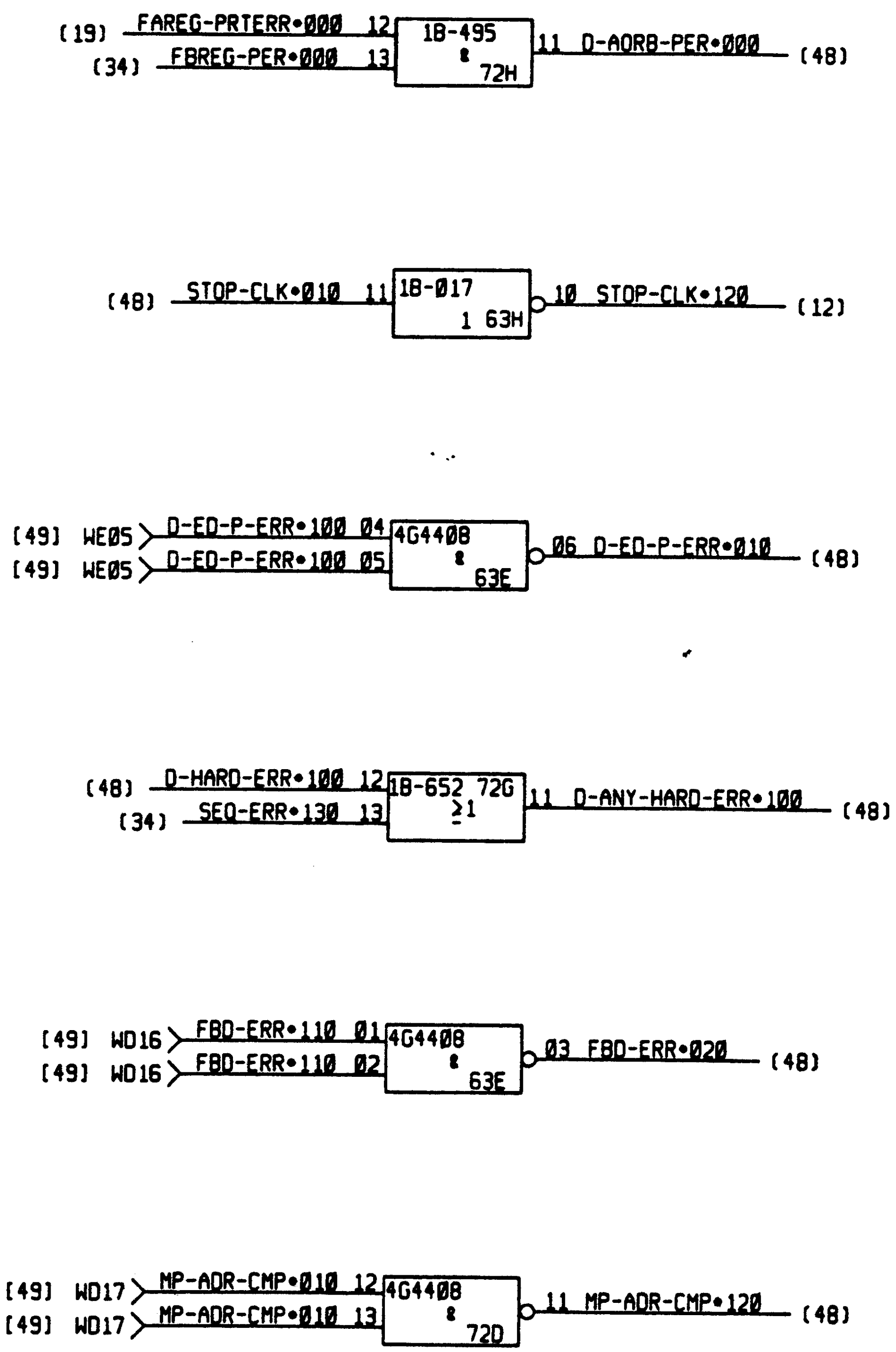
LOC

TITLE LOGIC DIAGRAM- WDASB

SIZE	DWG NO	SH	REV
B	58Ø88874	47.Ø	C



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58088874	SH 48.0	REV C



58Ø88874

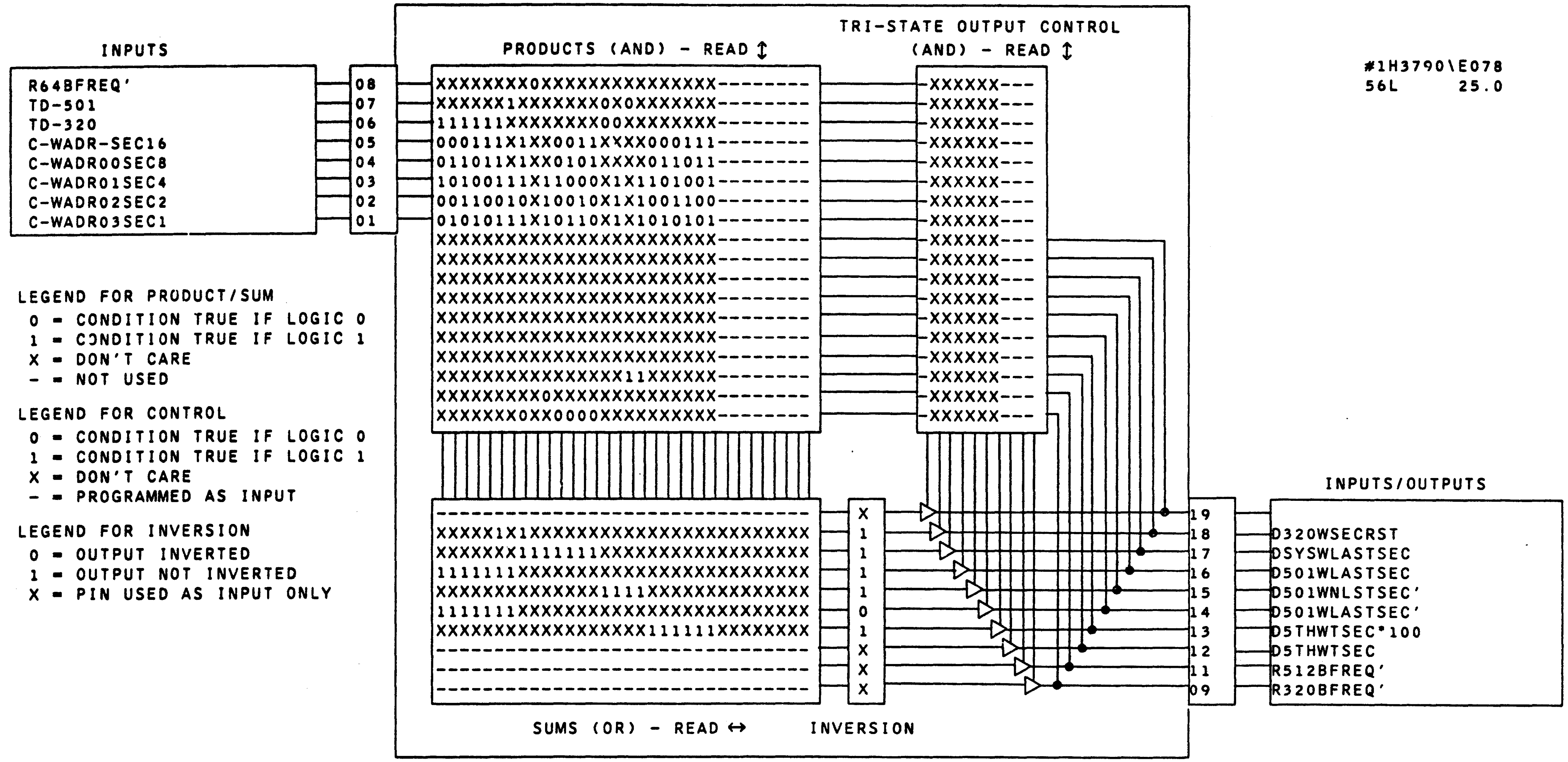
TOTAL NUMBER OF SHEETS = 52

LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASB	SIZE B	DWG NO 58Ø88874	SH 49.ØF	REV C

58088874

REVISION					
REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE

#1H3790\E078
56L 25.0



LEGEND FOR PRODUCT/SUM
0 = CONDITION TRUE IF LOGIC 0
1 = CONDITION TRUE IF LOGIC 1
X = DON'T CARE
- = NOT USED

LEGEND FOR CONTROL
0 = CONDITION TRUE IF LOGIC 0
1 = CONDITION TRUE IF LOGIC 1
X = DON'T CARE
- = PROGRAMMED AS INPUT

LEGEND FOR INVERSION
0 = OUTPUT INVERTED
1 = OUTPUT NOT INVERTED
X = PIN USED AS INPUT ONLY

UNLESS OTHERWISE SPECIFIED
DIMENSIONS = MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN
PROJECTION
SCALE | CODE

MATL
DES
CHK
FIN
DR
APPD
DISTR C120-26

HONEYWELL
HONEYWELL INFORMATION SYSTEMS
LOC PHOENIX, ARIZONA U.S.A.

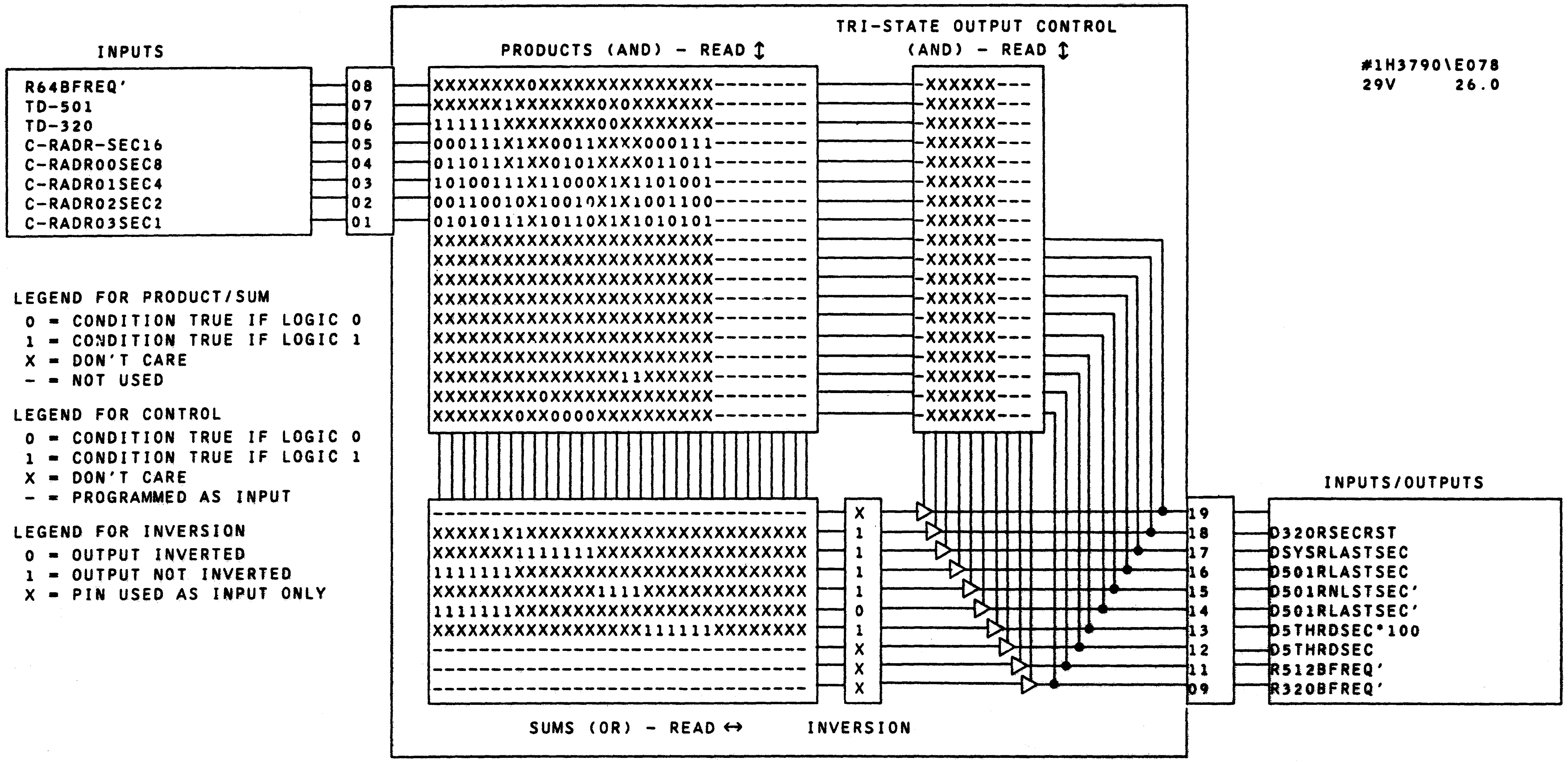
TITLE FPLA BLOCK DIAGRAM
WDASB

SIZE	DWG NO	SH	REV
B	58088874	A1	C

58088874

REVISION					
REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE

#1H3790\E078
29V 26.0



UNLESS OTHERWISE SPECIFIED DIMENSIONS = MILLIMETERS / INCHES	MATL	HONEYWELL HONEYWELL INFORMATION SYSTEMS LOC PHOENIX, ARIZONA U.S.A.	
TOLERANCE OF SIZE AND FORM PER	DES	TITLE FPLA BLOCK DIAGRAM WDASB	
INITIAL DESIGN	CHK		
PROJECTION	FIN		
SCALE / CODE	DR	SIZE B / DWG NO 58088874 / SH A2F	REV C
	APPD		
	DISTR C120-26		

58088870

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 001	102	203	304	004	PL ALL
A	LEVEL 1 ISSUE	83	07	01	[illegible] 9/28/83	A					A
B	PHAØAD304	83	09	12	G. Miller	B					B
C	PHAØXS297	83	OCT	14	[illegible]	C	C				C
D	PHAØXS328	83	NOV	11	[illegible]		D	D			D
D1	ENXS149 LVL 2		ND		[illegible]			D1			
E	PHAØXS398	84	01	30	E [illegible]	OBSOLETE	OBSOLETE		E		E
F	PHAØXS589	84	11	05	[illegible]					F	F

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY Efren Anaya 83 June 22

APPROVED [illegible] 6-23-83

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE HDUHC PWA WDASB

SIZE	REVISION STATUS FOR	SHEET	REV
X	58088870	1/1	F

DIST. - 30

BRUNING 44-141 40366

CE 300 A-3 (1-75)

58088872

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	SH 001	002		ALL
A	LVL 3 ISSUE	83	06	30	E Parker 4/28/83	A		1-10 F	A
B	PHA0XS297	83	10	14	L Drenth	B	B	1-10 F	B

OBSOLETE

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX, ARIZONA

BRUNING 44-141 40366

CE 300 A-3 (1-79)

MADE BY S Gregory 83 Jun 20

APPROVED 6-23-83

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CIL WDASB

SIZE	REVISION STATUS FOR	SHEET	REV
A	58088872	1/1	B

DIST. C125 -37

TAB-002

STANDARD LOCATION CODE PATTERN
X-POS & Y-POS PER 58046507-002
UNLESS OTHERWISE SHOWN, ROTATION IS NORTH

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
00A	1Q-483	58002483-001			
00AE	P9	43A114748P9			
00B	1Q-483	58002483-001			
00C	1Q-483	58002483-001			
00CE	P1043	43C212092P1043			
00D	1Q-483	58002483-001			
00E	1Q-483	58002483-001			
00EE	P1043	43C212092P1043			
00F	1Q-483	58002483-001			
00G	1Q-483	58002483-001			
00GE	P9	43A114748P9			
00H	1Q-483	58002483-001			
00J	1D-699	58002699-001			
00JE	P1043	43C212092P1043			
00K	1D-699	58002699-001			
00L	1D-699	58002699-001			
00LE	P1043	43C212092P1043			
00M	1D-699	58002699-001			
00N	1D-699	58002699-001			
00NE	P9	43A114748P9			
00P	1B-094	58002094-001			
00Q	1B-053	58002053-001			
00QE	P1043	43C212092P1043			
00R	1B-653	58002653-001			
00S	1B-053	58002053-001			
00SE	P1043	43C212092P1043			
00T	1B-015	58002015-001			
00U	1B-015	58002015-001			
00UE	P9	43A114748P9			
00V	1B-017	58002017-001			
00VE	RSOH	58020479-008			
00W	1C-057	58002057-001			

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
00WE	P1043	43C212092P1043			
00X	1C-057	58002057-001			
09A	4G4408	43C216408P1			
09AE	P9	43A114748P9			
09B	4G4408	43C216408P1			
09C	4G4408	43C216408P1			
09CE	P1043	43C212092P1043			
09D	4G4408	43C216408P1			
09E	1B3600	58002600-001			
09EE	P1043	43C212092P1043			
09F	1B3600	58002600-001			
09G	1B3600	58002600-001			
09GE	P9	43A114748P9			
09H	1E-779	58002779-001			
09J	1D-700	58002700-001			
09JE	P1043	43C212092P1043			
09K	1D-700	58002700-001			
09L	1D-699	58002699-001			
09LE	P1043	43C212092P1043			
09M	1D-699	58002699-001			
09N	1D-699	58002699-001			
09NE	P9	43A114748P9			
09P	1Q-616	58002616-001			
09Q	1Q-616	58002616-001			
09QE	P1043	43C212092P1043			
09R	1B-017	58002017-001			
09S	1C3447	43C216447P1			
09SE	P1043	43C212092P1043			
09T	1C3447	43C216447P1			
09U	1B-015	58002015-001			
09UE	P9	43A114748P9			
09V	1B-653	58002653-001			
09W	1B-094	58002094-001			
09WE	P1043	43C212092P1043			
09X	1B-495	58002495-001			
18A	1B-017	58002017-001			
18AE	P9	43A114748P9			
18B	4G4408	43C216408P1			

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
18C	1B-053	58002053-001			
18CE	P1043	43C212092P1043			
18D	1B-015	58002015-001			
18E	1B-653	58002653-001			
18EE	P1043	43C212092P1043			
18F	1B-017	58002017-001			
18G	1B-015	58002015-001			
18GE	P9	43A114748P9			
18H	1B-094	58002094-001			
18J	1B-644	58002644-001			
18JE	P1043	43C212092P1043			
18K	1D-700	58002700-001			
18KE	RSOH	58020479-008			
18L	1D-700	58002700-001			
18LE	P.1043	43C212092P1043			
18M	1D-700	58002700-001			
18N	1Q-483	58002483-001			
18NE	P9	43A114748P9			
18P	1B-017	58002017-001			
18Q	1Q-616	58002616-001			
18QE	P1043	43C212092P1043			
18R	1B-653	58002653-001			
18S	1C3447	43C216447P1			
18SE	P1043	43C212092P1043			
18T	4G4408	43C216408P1			
18U	1B-015	58002015-001			
18UE	P9	43A114748P9			
18V	1B-094	58002094-001			
18W	1D-058	58002058-001			
18WE	P1043	43C212092P1043			
18X	1Q-066	58002066-001			
27A	1B-053	58002053-001			
27AE	P9	43A114748P9			
27B	1B-053	58002053-001			
27C	1B-054	58002054-001			
27CE	P1043	43C212092P1043			
27D	1B-495	58002495-001			
27E	1D3492	58002492-001			

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
27EE	P1043	43C212092P1043			
27F	1D3492	58002492-001			
27G	1B-053	58002053-001			
27GE	P9	43A114748P9			
27H	1B3462	43C216462P1			
27J	1B3462	43C216462P1			
27JE	P1043	43C212092P1043			
27K	1B3462	43C216462P1			
27L	1B3462	43C216462P1			
27LE	P1043	43C212092P1043			
27M	1Q-616	58002616-001			
27N	4G4408	43C216408P1			
27NE	P9	43A114748P9			
27P	1E-011	58002011-001			
27Q	1Q-616	58002616-001			
27QE	P1043	43C212092P1043			
27R	1Q-066	58002066-001			
27S	1B-015	58002015-001			
27SE	P1043	43C212092P1043			
27T	1B-696	58002696-001			
27U	1Q-616	58002616-001			
27UE	P9	43A114748P9			
27W	1D-058	58002058-001			
27WE	P1043	43C212092P1043			
27X	1Q-066	58002066-001			
29V	1H3790-078	58002790-078			
36A	1B-653	58002653-001			
36AE	P9	43A114748P9			
36B	1B-053	58002053-001			
36C	1B-017	58002017-001			
36CE	P1043	43C212092P1043			
36D	1Q-616	58002616-001			
36E	1E-011	58002011-001			
36EE	P1043	43C212092P1043			
36F	1B-644	58002644-001			
36G	1B-495	58002495-001			
36GE	P9	43A114748P9			
36H	1Q-616	58002616-001			

COMP INSTL LIST - WDASB

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
36HE	RSOH	58020479-008			
36J	1C-041	58002041-001			
36JE	P1043	43C212092P1043			
36K	1B3462	43C216462P1			
36L	1B-713	58002713-001			
36LE	P1043	43C212092P1043			
36M	1B3462	43C216462P1			
36N	1B-017	58002017-001			
36NE	P9	43A114748P9			
36P	1B-015	58002015-001			
36Q	1Q-066	58002066-001			
36QE	P1043	43C212092P1043			
36R	RN7B	43B216592P42			
36S	1B-495	58002495-001			
36SE	P1043	43C212092P1043			
36T	1B3600	58002600-001			
36U	1Q-616	58002616-001			
36UE	P9	43A114748P9			
36W	1B-495	58002495-001			
36WE	P1043	43C212092P1043			
36X	1C-057	58002057-001			
45A	1B-094	58002094-001			
45AE	P9	43A114748P9			
45B	4G4408	43C216408P1			
45C	1E-011	58002011-001			
45CE	P1043	43C212092P1043			
45D	1Q-066	58002066-001			
45E	1Q-066	58002066-001			
45EE	P1043	43C212092P1043			
45F	RN7B	43B216592P42			
45G	1Q-616	58002616-001			
45GE	P9	43A114748P9			
45H	1B-714	58002714-001			
45J	1B-652	58002652-001			
45JE	P1043	43C212092P1043			
45K	1B3462	43C216462P1			
45L	1B-713	58002713-001			
45LE	P1043	43C212092P1043			

COMP INSTL LIST - WDASB

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
45M	1B3462	43C216462P1			
45N	1B-017	58002017-001			
45NE	P9	43A114748P9			
45P	1Q-616	58002616-001			
45Q	1Q-616	58002616-001			
45QE	P1043	43C212092P1043			
45R	1C-057	58002057-001			
45SE	P1043	43C212092P1043			
45T	1B-053	58002053-001			
45U	1B-015	58002015-001			
45UE	P9	43A114748P9			
45V	1B-053	58002053-001			
45W	1B-017	58002017-001			
45WE	P1043	43C212092P1043			
45X	1C-057	58002057-001			
54A	1B-017	58002017-001			
54AE	P9	43A114748P9			
54B	1B-094	58002094-001			
54C	1B-015	58002015-001			
54CE	P1043	43C212092P1043			
54D	1B-053	58002053-001			
54E	1B-053	58002053-001			
54EE	P1043	43C212092P1043			
54F	1B-015	58002015-001			
54G	4G4408	43C216408P1			
54GE	P9	43A114748P9			
54H	1B-094	58002094-001			
54J	1B-094	58002094-001			
54JE	P1043	43C212092P1043			
54K	1B3462	43C216462P1			
54LE	P1043	43C212092P1043			
54M	1E-779	58002779-001			
54N	1C3447	43C216447P1			
54NE	P9	43A114748P9			
54P	1Q-066	58002066-001			
54Q	1Q-066	58002066-001			
54QE	P1043	43C212092P1043			
54R	1C-057	58002057-001			

COMP INSTL LIST - WDASB

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
54RE	RSOH	58020479-008			
54S	1C-057	58002057-001			
54SE	P1043	43C212092P1043			
54T	1B-017	58002017-001			
54U	1B-652	58002652-001			
54UE	P9	43A114748P9			
54V	1B-015	58002015-001			
54W	1B-652	58002652-001			
54WE	P1043	43C212092P1043			
54X	1B-015	58002015-001			
56L	1H3790-078	58002790-078			
63A	1B-644	58002644-001			
63AE	P9	43A114748P9			
63C	1Q-483	58002483-001			
63CE	P1043	43C212092P1043			
63D	1B-479	58002479-001			
63E	4G4408	43C216408P1			
63EE	P1043	43C212092P1043			
63F	1Q-071	58002071-001			
63G	1Q-616	58002616-001			
63GE	P9	43A114748P9			
63H	1B-017	58002017-001			
63J	1Q-071	58002071-001			
63JE	P1043	43C212092P1043			
63K	1Q-483	58002483-001			
63LE	P1043	43C212092P1043			
63M	1Q-616	58002616-001			
63N	1Q-066	58002066-001			
63NE	P9	43A114748P9			
63P	1Q-066	58002066-001			
63Q	1B-017	58002017-001			
63QE	P1043	43C212092P1043			
63R	1C-057	58002057-001			
63S	1B-053	58002053-001			
63SE	P1043	43C212092P1043			
63T	1B-015	58002015-001			
63U	1B-495	58002495-001			
63UE	P9	43A114748P9			

COMP INSTL LIST - WDASB

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
63V	1B-094	58002094-001			
63W	1B-094	58002094-001			
63WE	P1043	43C212092P1043			
72A	DL1E	43B216593P15			
72AE	P9	43A114748P9			
72B	1B-495	58002495-001			
72C	RN9A	43B216592P22			
72CE	P1043	43C212092P1043			
72D	4G4408	43C216408P1			
72E	1B-015	58002015-001			
72EE	P1043	43C212092P1043			
72F	RN2C	43B216592P11			
72G	1B-652	58002652-001			
72GE	P9	43A114748P9			
72H	1B-495	58002495-001			
72J	1B-495	58002495-001			
72JE	P1043	43C212092P1043			
72K	1Q-483	58002483-001			
72L	1C3447	43C216447P1			
72LE	P1043	43C212092P1043			
72M	RN3C	43B216592P12			
72N	1Q-059	58002059-001			
72NE	P9	43A114748P9			
72P	1Q-059	58002059-001			
72Q	2D5419	43C216419P1			
72QE	P1043	43C212092P1043			
72R	1C3447	43C216447P1			
72S	1C3447	43C216447P1			
72SE	P1043	43C212092P1043			
72T	1C3447	43C216447P1			
72U	1C3447	43C216447P1			
72UE	P9	43A114748P9			
72V	1C3447	43C216447P1			
72W	1C3447	43C216447P1			
72WE	P1043	43C212092P1043			
72X	1C3447	43C216447P1			
81A	RN4D	43B216592P17			
81AE	P9	43A114748P9			

COMP INSTL LIST - WDASB

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
81B	1B-015	58002015-001			
81BE	P9	43A114748P9			
81C	4G4408	43C216408P1			
81CE	P1043	43C212092P1043			
81D	1B-056	58002056-001			
81DE	P9	43A114748P9			
81E	1U-670	58002670-001			
81EE	P1043	43C212092P1043			
81F	1U-670	58002670-001			
81G	1U-670	58002670-001			
81GE	P9	43A114748P9			
81H	4G4408	43C216408P1			
81J	1B-015	58002015-001			
81JE	P1043	43C212092P1043			
81K	1B-015	58002015-001			
81L	1B-053	58002053-001			
81LE	P1043	43C212092P1043			
81M	1B3600	58002600-001			
81N	1B3600	58002600-001			
81NE	P9	43A114748P9			
81P	1B3600	58002600-001			
81Q	1B3600	58002600-001			
81QE	P1043	43C212092P1043			
81R	1B3600	58002600-001			
81S	1C3447	43C216447P1			
81SE	P1043	43C212092P1043			
81T	1B-015	58002015-001			
81U	1D-058	58002058-001			
81UE	P9	43A114748P9			
81V	1D-058	58002058-001			
81W	1D-058	58002058-001			
81WE	P1043	43C212092P1043			
81X	1D-058	58002058-001			
90A	XL1B	43C216118P62			
90B	1B-710	58002710-001			
90C	XL1C	43C216118P63			
90D	4G4408	43C216408P1			
90DE	P1043	43C212092P1043			

COMP INSTL LIST - WDASB

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
90E	1B-714	58002714-001			
90EE	P1043	43C212092P1043			
90F	4G4408	43C216408P1			
90G	1B-053	58002053-001			
90GE	P9	43A114748P9			
90JE	P1043	43C212092P1043			
90K	1B-710	58002710-001			
90L	4G4408	43C216408P1			
90LE	P1043	43C212092P1043			
90M	4G4408	43C216408P1			
90N	4G4408	43C216408P1			
90NE	P9	43A114748P9			
90P	3S2768	98002768-003			
90Q	3S2768	98002768-003			
90QE	P1043	43C212092P1043			
90R	3S2768	98002768-003			
90S	3S2768	98002768-003			
90SE	P1043	43C212092P1043			
90T	3S2768	98002768-003			
90U	3S2768	98002768-003			
90UE	P9	43A114748P9			
90V	3S2768	98002768-003			
90W	3S2768	98002768-003			
90WE	P1043	43C212092P1043			
90X	3S2768	98002768-003			

REV	AUTHORITY	DATE
A	LEVEL3ISSUE	84APR20

SIGNAL NAME	PAGE
$DAU•010	5.0
$DAU-CLK•020	5.0
$DAU-CLK•030	5.0
$DAU-CLK•130	5.0
$DAU-CLK•131	5.0
$DAU-TOT-CLR•011	5.0
$EXEC-22-23•020	34.0
$EXEC-24-26•020	33.0
$EXEC-CLK•010	30.0
$EXEC-CLK•110	42.0
$EXEC-CLK•111	42.0
$LD-SEQ-ADDR-LSB•020	23.0
$LD-SEQ-ADDR-LSB•021	4.0
$LD-SEQ-ADDR-MSB•020	23.0
$PAR-TOT-CLR•030	5.0
$PAR-TOT-CLR•031	5.0
$PAR-TOT-CLR•032	5.0
$PAR-TOT-CLR•120	5.0
$PARTIAL-CLR•011	5.0
$SEQ-CTR-LD•010	27.0
$SEQ-CTR-LD•011	4.0
$TOT-CLR•030	5.0
$TOT-CLR•031	5.0
$TOT-CLR•032	5.0
$TOT-CLR•120	5.0
B-REG-READY•110	19.0
BREG-00•110	17.0
BREG-01•110	17.0
BREG-02•110	17.0
BREG-03•110	17.0
BREG-04•110	17.0
BREG-05•110	17.0
BREG-06•110	17.0
BREG-07•110	17.0
BREG-P•110	17.0
BUF-DATA-0•120	17.0
BUF-DATA-1•120	17.0
BUF-DATA-2•120	17.0
BUF-DATA-3•120	17.0
BUF-DATA-4•120	17.0
BUF-DATA-5•120	17.0
BUF-DATA-6•120	17.0
BUF-DATA-7•120	17.0
BUF-DATA-P•120	17.0
BUF-FULL•110	17.0
BUF-FULL•120	17.0
BUF-LST-BYT•120	17.0
BUF-SHB•120	17.0
BUFF-RD-STB•020	17.0
BUFF-RDY•030	42.0
BUFF-RDY•120	19.0
BUFF-RDY-STB•060	43.0
BUFF-RSTB•040	43.0
BUFF-RSTB•130	17.0
BUFF-RSTB•131	4.0
BUFF-RSTB-0•020	17.0
BUFF-RSTB-0•130	18.0
BUFF-RSTB-1•020	17.0
BUFF-RSTB-2•020	17.0
BUFF-RW-STB•050	43.0
BUFF-STB•130	17.0
BUFF-WR-STB•020	17.0
BUFF-WSTB•040	43.0
BUFF-WSTB•130	17.0
BUFF-WSTB•131	4.0

SIGNAL NAME	PAGE
BUFF-WSTB-0•020	17.0
BUFF-WSTB-1•020	17.0
BYTE-CTR-ONES•110	20.0
BYTE-CTR-ONES•120	20.0
CLK-TTE•100	42.0
CLR-SYNC•010	21.0
CLR-SYNC•011	45.0
CLR-SYNC•012	44.0
CMD-DC0•100	32.0
CMD-DC1•100	32.0
CMD-DC2•100	32.0
CMD-DC3•100	32.0
CMD-DC4•100	32.0
CMD-DC5•100	32.0
CMD-DCP•100	32.0
CMD-LD•120	31.0
CMD-OT-WR•010	32.0
CMD-OT-WR•100	32.0
CMD-RD-WR•100	32.0
CMD-READ•110	32.0
CMD-WR-DCS•120	19.0
CMD-WRITE•110	32.0
CMD-WRITE•120	19.0
CMD-WRITE-DCS•100	19.0
COMPARE•120	20.0
COMPARE•130	20.0
CONT-SEQ-ADDR•010	23.0
CSYN-2-3•110	35.0
CSYN-4-5•110	35.0
CSYN-6-7•110	35.0
CSYN-CNT-0•100	34.0
CSYN-CNT-0•110	20.0
CSYN-CNT-1•100	34.0
CSYN-CNT-1•110	20.0
CSYN-CNT-2•100	34.0
CSYN-CNT-2•110	20.0
CSYN-CNT-3•100	34.0
CSYN-CNT-3•110	20.0
CSYN-CNT-4•100	34.0
CSYN-CNT-4•110	20.0
CSYN-CNT-5•100	34.0
CSYN-CNT-5•110	20.0
CSYN-CNT-6•010	35.0
CSYN-CNT-6•100	34.0
CSYN-CNT-6•110	20.0
CSYN-CNT-7•010	35.0
CSYN-CNT-7•100	34.0
CSYN-CNT-7•110	20.0
CSYN-CNT-ZRO•030	35.0
CSYN-CNT-ZRO•120	35.0
CSYN-LD•040	34.0
CSYN-LD•041	4.0
CSYN-LSB-1•100	34.0
CSYN-PE•000	34.0
CTL-EQ-RST•020	42.0
CYHD-FULL•010	20.0
CYHD-FULL•030	21.0
CYHD-FULL•120	20.0
D$ERROR•100	8.0
D-DIS-BRAN•000	29.0
D-SUB-BRAN•000	29.0
D-SW-0•100	38.0
D-SW-1•100	38.0
D-SW-2•100	39.0
D-SW-3•100	39.0

SIGNAL NAME	PAGE
D-SW-4•100	39.0
D-SW-5•100	39.0
D-SW-6•100	39.0
D-SW-7•100	39.0
D-SW-P•100	40.0
D-SW-PARITY•100	40.0
DATA-63-64•100	38.0
DATA-P•020	40.0
DATA-P•130	40.0
DATA-PAR-ER•140	40.0
DBRD-SEL-0-0S0•100	16.0
DBRD-SEL-1-0S0•100	16.0
DBRD-SEL-2-0S0•100	16.0
DBRD-SEL-3-0S0•100	16.0
DBRD-SEL-4-0S0•100	16.0
DBRD-SEL-5-0S0•100	16.0
DBRD-SEL-6-0S0•100	16.0
DBRD-SEL-7-0S0•100	16.0
DCONT-OUT-0S0•100	15.0
DDAI-INIT-0S1•100	15.0
DDTA-I-D10-0S0•100	14.0
DDTA-I-D11-0S0•100	14.0
DDTA-I-D12-0S0•100	14.0
DDTA-I-D13-0S0•100	14.0
DDTA-I-D14-0S0•100	14.0
DDTA-I-D15-0S0•100	14.0
DDTA-I-D16-0S0•100	14.0
DDTA-I-D17-0S0•100	14.0
DDTA-I-D1P-0S0•100	14.0
DEC-BRAN•040	29.0
DEC-BRAN•060	30.0
DEC-BRAN•130	30.0
DEC-BRAN•150	29.0
DEC-BRAN-0•020	29.0
DEC-BRAN-0•021	4.0
DEC-BRAN-1•020	30.0
DEC-BRAN-1•021	4.0
DEC-BRAN-2•020	30.0
DEC-BRAN-2•021	4.0
DEC-BRAN-3•020	30.0
DEC-BRAN-3•021	4.0
DEF-SKP-INH•030	16.0
DEF-SKP-INH•110	20.0
DEF-SKP-INH•120	20.0
DEF-SYNC-ERR•010	20.0
DEF-SYNC-ERR•020	20.0
DEF-SYNC-ERR•130	21.0
DEF-WDSN•030	20.0
DEF-WDSN•040	20.0
DEF-WDSN-DS•030	37.0
DEF-WHEX•030	20.0
DEF-WHEX•040	20.0
DEF-WHEX-DS•030	37.0
DEFECT-SKP•120	20.0
DEFECT-SKP•130	20.0
DEV-4XX•100	34.0
DEV-4XX•110	20.0
DEV-4XX-500•110	34.0
DEV-4XX-500•120	18.0
DEV-501•110	34.0
DEV-501•120	18.0
DEV-501-NFMT•120	34.0
DEV-DATA-0•100	14.0
DEV-DATA-1•100	14.0
DEV-DATA-2•100	14.0

SIGNAL NAME	PAGE
DEV-DATA-3•100	14.0
DEV-DATA-4•100	14.0
DEV-DATA-5•100	14.0
DEV-DATA-6•100	14.0
DEV-DATA-7•100	14.0
DEV-DATA-P•100	14.0
DEV-FLT•100	15.0
DEV-FLT-SET•110	45.0
DEV-IDX•100	15.0
DEV-IDX-SET•110	45.0
DEV-NFMT•110	34.0
DEV-OPI•010	45.0
DEV-OPI•100	15.0
DEV-OPI-DN•120	45.0
DEV-SRI•010	43.0
DEV-SRI•100	14.0
DFAULT-FLT-0S0•100	15.0
DFLT-RW•010	21.0
DIAG-ALL-ONES•100	6.0
DIAG-CNT-SRI•020	6.0
DIAG-D0•010	5.0
DIAG-D1•010	6.0
DIAG-D2•010	6.0
DIAG-D3•010	6.0
DIAG-D4•010	6.0
DIAG-D5•010	6.0
DIAG-D6•010	6.0
DIAG-D7•010	6.0
DIAG-DCS•110	6.0
DIAG-DP•010	6.0
DIAG-RD-CTL•020	6.0
DIAG-RW-CTL•020	6.0
DIAG-RW-DCS•100	6.0
DIAG-SEL•020	6.0
DIAG-SEL•110	6.0
DIAG-SRI•010	6.0
DINDEX-IDX-0S0•100	15.0
DINIT-DIN-0S0•100	15.0
DMP-ERROR•110	15.0
DMPADR-11•100	7.0
DMPADR-12•100	7.0
DMPADR-13•100	7.0
DMPADR-14•100	7.0
DMPADR-15•100	7.0
DMPADR-P•100	8.0
DMPDTA-0•100	7.0
DMPDTA-1•100	7.0
DMPDTA-2•100	7.0
DMPDTA-3•100	7.0
DMPDTA-4•100	7.0
DMPDTA-5•100	7.0
DMPDTA-6•100	7.0
DMPDTA-7•100	7.0
DMPDTA-P•100	7.0
DOPER-OPI-0S0•100	15.0
DOUBLE-DEF•120	20.0
DOUBLE-DEF•130	20.0

DISTRIBUTION CODE C120-26

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LOC CEO HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- WDASE LOGIC - PAGE CROSS REFERENCE
ASM REF 58075900-X02
DATA BASE NIODAU/DAU$45/HSE
DR DFTG 84APR20
SIZE B DWG NO 58075904 SH 1.0 REV A

58075904

REV	AUTHORITY	DATE
A	LEVEL3ISSUE	84APR2Ø

SIGNAL NAME	PAGE
DRO-FR-DEV-ØSØ•1ØØ	15.Ø
DREG-Ø•1ØØ	41.Ø
DREG-Ø•11Ø	19.Ø
DREG-1•1ØØ	41.Ø
DREG-1•11Ø	19.Ø
DREG-2•1ØØ	41.Ø
DREG-2•11Ø	19.Ø
DREG-3•1ØØ	41.Ø
DREG-3•11Ø	19.Ø
DREG-4•1ØØ	41.Ø
DREG-4•11Ø	19.Ø
DREG-5•1ØØ	41.Ø
DREG-5•11Ø	19.Ø
DREG-6•1ØØ	41.Ø
DREG-6•11Ø	19.Ø
DREG-7•1ØØ	41.Ø
DREG-7•11Ø	19.Ø
DREG-LD•1ØØ	4Ø.Ø
DREG-M•1ØØ	41.Ø
DREG-P•1ØØ	41.Ø
DREG-P•11Ø	19.Ø
DRESET-RUN•ØØØ	22.Ø
DS-Ø-B1•Ø2Ø	2Ø.Ø
DS-Ø-B1•11Ø	2Ø.Ø
DS-Ø-B2•Ø2Ø	2Ø.Ø
DS-Ø-B2•11Ø	2Ø.Ø
DS-Ø-B3•Ø2Ø	2Ø.Ø
DS-Ø-B3•11Ø	2Ø.Ø
DS-2-B1•Ø2Ø	2Ø.Ø
DS-2-B1•11Ø	2Ø.Ø
DS-2-B2•Ø2Ø	2Ø.Ø
DS-2-B2•11Ø	2Ø.Ø
DS-2-B3•Ø2Ø	2Ø.Ø
DS-2-B3•11Ø	2Ø.Ø
DSEL-SEØ•11Ø	7.Ø
DSR-RD-SRI-ØSØ•1ØØ	14.Ø
DSW-CNTL-1•13Ø	38.Ø
DSW-CNTL-1•131	4.Ø
DSW-CNTL-2•13Ø	38.Ø
DSW-CNTL-2•131	4.Ø
DSW-CNTL-4•13Ø	38.Ø
DSW-CNTL-4•131	4.Ø
DSYN-BIT-Ø•11Ø	35.Ø
ECC-EDAC-ER•12Ø	19.Ø
ED-LAST•Ø2Ø	38.Ø
EDAL-BYTES•11Ø	19.Ø
EDAC-BYTES•12Ø	19.Ø
EDAC-CLEAR•12Ø	2Ø.Ø
EDAC-CLEAR•13Ø	19.Ø
EDAC-DATA-Ø•12Ø	19.Ø
EDAC-DATA-1•12Ø	19.Ø
EDAC-DATA-2•12Ø	19.Ø
EDAC-DATA-3•12Ø	19.Ø
EDAC-DATA-4•12Ø	19.Ø
EDAC-DATA-5•12Ø	19.Ø
EDAC-DATA-6•12Ø	19.Ø
EDAC-DATA-7•12Ø	19.Ø
EDAC-DATA-P•12Ø	19.Ø
EDAC-F-BUFF•Ø2Ø	37.Ø
EDAC-F-EDAC•Ø2Ø	37.Ø
EDAC-RD-STB•Ø2Ø	18.Ø
EDAC-RDY•Ø3Ø	42.Ø
EDAC-RDY•12Ø	19.Ø
EDAC-RSTB•13Ø	18.Ø
EDAC-RSTB•131	4.Ø

SIGNAL NAME	PAGE
EDAC-RSTB-Ø•Ø2Ø	18.Ø
EDAC-RSTB-1•Ø2Ø	18.Ø
EDAC-RSTB-2•Ø3Ø	18.Ø
EDAC-STB•13Ø	19.Ø
EDAC-WR-STB•Ø2Ø	18.Ø
EDAC-WSTB•13Ø	18.Ø
EDAC-WSTB•131	4.Ø
EDAC-WSTB-Ø•Ø2Ø	18.Ø
EDAC-WSTB-1-Ø2Ø	18.Ø
EDAC-WSTB-2•Ø2Ø	18.Ø
EN-PAR-CK•13Ø	4Ø.Ø
EN-PAR-F-BUFF•1ØØ	37.Ø
ENAB-WDSN•Ø4Ø	37.Ø
ENAB-WHEX•Ø4Ø	37.Ø
EQUAL-A•ØØØ	41.Ø
EQUAL-A•11Ø	41.Ø
F-EDAC-ERROR•11Ø	19.Ø
F-EDAC-READY•11Ø	19.Ø
FCMD-DCØ-ØSØ•1ØØ	16.Ø
FCMD-DC1-ØSØ•1ØØ	16.Ø
FCMD-DC2-ØSØ•1ØØ	16.Ø
FCMD-DC3-ØSØ•1ØØ	16.Ø
FCMD-DC4-ØSØ•1ØØ	16.Ø
FCMD-DC5-ØSØ•1ØØ	16.Ø
FCMD-DCP-ØSØ•1ØØ	16.Ø
FCMD-DCS-ØSD•1ØØ	16.Ø
FCT-ALL-1•1ØØ	31.Ø
FCT-CNT•11Ø	31.Ø
FCT-CNT-Ø•1ØØ	31.Ø
FCT-CNT-1•1ØØ	31.Ø
FCT-CNT-2•1ØØ	31.Ø
FCT-CNT-3•1ØØ	31.Ø
FDCS•ØØØ	44.Ø
FDCS•1ØØ	44.Ø
FDEV-FLT•ØØØ	45.Ø
FDEV-FLT•1ØØ	45.Ø
FDEV-INIT•1ØØ	44.Ø
FDEV-OPI-DN•ØØØ	45.Ø
FDEV-OPI-DN•1ØØ	45.Ø
FDEV-SEL-2-ØSØ•1ØØ	16.Ø
FDEV-SEL-3-ØSØ•1ØØ	16.Ø
FDTA-M-DM1-ØSØ•1ØØ	15.Ø
FDTA-O-D1Ø-ØSØ•1ØØ	15.Ø
FDTA-O-D11-ØSØ•1ØØ	15.Ø
FDTA-O-D12-ØSØ•1ØØ	15.Ø
FDTA-O-D13-ØSØ•1ØØ	15.Ø
FDTA-O-D14-ØSØ•1ØØ	15.Ø
FDTA-O-D15-ØSØ•1ØØ	15.Ø
FDTA-O-D16-ØSØ•1ØØ	15.Ø
FDTA-O-D17-ØSØ•1ØØ	15.Ø
FDTA-O-D1P-ØSØ•1ØØ	15.Ø
FDTA-PAR-ERR•ØØØ	41.Ø
FDTA-PAR-ERR•1ØØ	41.Ø
FEQUAL•1ØØ	42.Ø
FEQUAL-RST•Ø3Ø	42.Ø
FIFO-IN-Ø•1ØØ	36.Ø
FIFO-IN-1•1ØØ	36.Ø
FIFO-IN-2•1ØØ	36.Ø
FIFO-IN-3•1ØØ	36.Ø
FIFO-IN-4•1ØØ	36.Ø
FIFO-IN-5•1ØØ	36.Ø
FIFO-IN-6•1ØØ	36.Ø
FIFO-IN-7•1ØØ	36.Ø
FIFO-IN-CØ•Ø1Ø	35.Ø
FIFO-IN-C1•Ø4Ø	35.Ø

SIGNAL NAME	PAGE
FIFO-IN-CLR•Ø2Ø	36.Ø
FIFO-IN-LD•Ø2Ø	36.Ø
FIFO-IN-OR•1ØØ	36.Ø
FIFO-IN-UL•Ø2Ø	36.Ø
FIFO-OUT-Ø•1ØØ	36.Ø
FIFO-OUT-1•1ØØ	36.Ø
FIFO-OUT-2•1ØØ	36.Ø
FIFO-OUT-3•1ØØ	36.Ø
FIFO-OUT-4•1ØØ	36.Ø
FIFO-OUT-5•1ØØ	36.Ø
FIFO-OUT-6•1ØØ	36.Ø
FIFO-OUT-7•1ØØ	36.Ø
FIFO-OUT-CLR•Ø5Ø	36.Ø
FIFO-OUT-CO•Ø4Ø	36.Ø
FIFO-OUT-LD•Ø3Ø	35.Ø
FIFO-OUT-OR•1ØØ	36.Ø
FIFO-OUT-P•1ØØ	36.Ø
FIFO-OUT-UL•Ø2Ø	35.Ø
FIFO-UL-CTL•12Ø	35.Ø
FINDEX•1ØØ	45.Ø
FINDEX•1Ø1	4.Ø
FLAST-BYT-ERR•ØØØ	38.Ø
FLAST-BYT-ERR•1ØØ	38.Ø
FLAST-BYTE•ØØØ	37.Ø
FLAST-BYTE•1ØØ	37.Ø
FLAST-BYTE•1Ø1	5.Ø
FMP-ADDR-ERR•ØØØ	8.Ø
FMP-ADDR-ERR•Ø1Ø	19.Ø
FMP-PAR-ERR•ØØØ	8.Ø
FMP-PAR-ERR•1ØØ	8.Ø
FMP-SEQ-PE•Ø1Ø	21.Ø
FSEQ-ADDR-LD•ØØØ	22.Ø
FSEQ-ADDR-LD•1ØØ	22.Ø
FSEQ-ADDR-LD•1Ø1	4.Ø
FSEQ-EXEC•ØØØ	23.Ø
FSEQ-EXEC•1ØØ	23.Ø
FSEQ-EXEC•1Ø1	22.Ø
FSEQ-EXEC•1Ø2	4.Ø
FSEQ-EXEC•11Ø	2Ø.Ø
FSEQ-EXEC•111	23.Ø
FSEQ-PAR-ERR•ØØØ	26.Ø
FSEQ-PAR-ERR•1ØØ	26.Ø
FSEQ-RUN•ØØØ	22.Ø
FSEQ-RUN•1ØØ	22.Ø
FSEQ-RUN•1Ø1	4.Ø
FSEQ-RUN•11Ø	14.Ø
FSEQ-SYNC•ØØØ	22.Ø
FSEQ-SYNC•ØØ1	4.Ø
FSEQ-SYNC•11Ø	22.Ø
FSTRT-SET•11Ø	43.Ø
FSTRT-SWO•1ØØ	43.Ø
FSTRT-SWO•1Ø1	4.Ø
FSWO•ØØØ	44.Ø
FSWO•1ØØ	44.Ø
FSWO-RST•Ø2Ø	44.Ø
FSWO-SET•Ø2Ø	44.Ø
FSWO-SET-Ø•12Ø	44.Ø
FSWO-SET-1•Ø1Ø	44.Ø
FSWO-SET-2•Ø1Ø	44.Ø
FSY1•1ØØ	43.Ø
FSY1-RST•Ø2Ø	42.Ø
FSY2•ØØØ	43.Ø
FSY2•11Ø	43.Ø
FSY2•111	43.Ø
FSY3•1ØØ	43.Ø

SIGNAL NAME	PAGE
FSY4•1ØØ	43.Ø
FTTE•ØØØ	43.Ø
FTTE•1ØØ	43.Ø
FWDDS-DTB•1ØØ	37.Ø
FWDDS-DTB•1Ø1	5.Ø
GND-ØØA-ØØ	13.Ø
GND-ØØL Ø8	6.Ø
GND-Ø9L-Ø8	41.Ø
GND-Ø9L-Ø8	38.Ø
GND-Ø9M-Ø8	37.Ø
GND-18G-Ø8	11.Ø
GND-18H-Ø8	12.Ø
GND-18J-Ø8	12.Ø
GND-18K-Ø8	12.Ø
GND-18N-Ø8	12.Ø
GND-18P-Ø8	12.Ø
GND-18Q-Ø8	12.Ø
GND-18R-Ø8	13.Ø
GND-27G-Ø8	1Ø.Ø
GND-27H-Ø8	1Ø.Ø
GND-27J-Ø8	1Ø.Ø
GND-27K-Ø8	11.Ø
GND-27N-Ø8	11.Ø
GND-27P-Ø8	11.Ø
GND-27Q-Ø8	11.Ø
GND-27R-Ø8	11.Ø
GND-36A-Ø8	45.Ø
GND-36B-Ø8	45.Ø
GND-36G-Ø8	8.Ø
GND-36H-Ø8	9.Ø
GND-36J-Ø8	9.Ø
GND-36K-Ø8	9.Ø
GND-36N-Ø8	9.Ø
GND-36P-Ø8	9.Ø
GND-36Q-Ø8	9.Ø
GND-36R-Ø8	1Ø.Ø
GND-36S-Ø7	26.Ø
GND-45A-Ø8	44.Ø
GND-45A-Ø8	43.Ø
GND-45B-Ø8	26.Ø
GND-45M-Ø8	4Ø.Ø
GND-45S-Ø8	7.Ø
GND-45W-Ø7	8.Ø
GND-54D-Ø7	32.Ø
GND-54G-Ø8	38.Ø
GND-54H-Ø8	38.Ø
GND-54J-Ø8	39.Ø
GND-54K-Ø8	39.Ø
GND-54L-Ø8	41.Ø
GND-54M-Ø8	41.Ø
GND-54N-Ø8	39.Ø
GND-54P-Ø8	39.Ø
GND-54Q-Ø8	39.Ø
GND-54R-Ø8	39.Ø
GND-54S-Ø8	22.Ø
GND-54T-Ø8	8.Ø
GND-63A-Ø8	43.Ø

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TITLE LOGIC DIAGRAM- WDASE LOGIC - PAGE CROSS REFERENCE

ASM REF 58Ø759ØØ-XØ2

DATA BASE NIODAU/DAU$45/HSE

DFTG 84APR2Ø

SIZE B | DWG NO 58Ø759Ø4 | SH 1.1 | REV A

58Ø759Ø4

REV	AUTHORITY	DATE
A	LEVEL3ISSUE	84APR20

SIGNAL NAME	PAGE
GND-63D-08	22.0
GND-63K-08	24.0
GND-63N-08	23.0
GND-63P-08	23.0
GND-63R-07	23.0
GND-72L-08	19.0
GND-72M-08	19.0
GND-72N-08	19.0
GND-72P-08	19.0
GND-72Q-08	19.0
GND-72R-08	19.0
GND-72S-08	17.0
GND-72T-08	17.0
GND-81A-08	13.0
GND-81B-08	13.0
GND-81N-08	18.0
GND-81P-08	7.0
GND-81Q-08	7.0
GND-81R-08	7.0
GND-81V-08	21.0
GND-81W-08	20.0
GND-81X-08	20.0
GND-90A-07	13.0
GND-90F-10	36.0
GND-90G-10	36.0
GND-90H-10	32.0
GND-90J-10	31.0
GND-90K-09	25.0
GND-90L-09	25.0
GND-90M-09	24.0
GND-90N-09	25.0
GND-90R-10	33.0
GND-90S-10	33.0
GND-90T-10	36.0
GND-90U-10	36.0
GND-90X-08	20.0
HI-LVL-0•100	5.0
HI-LVL-1•100	5.0
HI-LVL-2•100	5.0
HI-LVL-3•100	5.0
INH-DCS•020	42.0
LAST-DATA•110	17.0
LAST-EDAC•120	20.0
LAST-EDAC•130	19.0
MODE-DEST•010	35.0
MODE-DEST•100	33.0
MODE-DEV-INH•100	33.0
MODE-DIAG-SEL•100	33.0
MODE-EDAC-RD•010	36.0
MODE-EDAC-RD•100	33.0
MODE-LD•130	32.0
MODE-RAR•100	33.0
MODE-RAR•110	18.0
MODE-SP0•100	33.0
MODE-SP1•100	33.0
MODE-VERIFY•010	17.0
MODE-VERIFY•100	33.0
MP-A00-D4•030	44.0
MP-A00-D4•120	44.0
MP-A3-D0•120	21.0
MP-ADDR-11•110	7.0
MP-ADDR-12•020	7.0
MP-ADDR-12•110	7.0
MP-ADDR-13•110	7.0
MP-ADDR-14•110	7.0

SIGNAL NAME	PAGE
MP-ADDR-15•110	7.0
MP-ADDR-ERR•100	8.0
MP-ADEC-00•000	7.0
MP-ADEC-00•110	44.0
MP-ADEC-02•000	7.0
MP-ADEC-03•000	7.0
MP-ADEC-03•110	21.0
MP-ADEC-04•000	7.0
MP-ADEC-05•000	7.0
MP-ADEC-06•000	7.0
MP-ADEC-07•000	7.0
MP-ADEC-08•000	8.0
MP-ADEC-09•000	8.0
MP-ADEC-10•000	8.0
MP-ADEC-12•000	8.0
MP-ADEC-13•000	8.0
MP-ADEC-13•110	35.0
MP-ADEC-2-5•110	23.0
MP-ADEC-3-5•110	23.0
MP-DATA-0•110	7.0
MP-DATA-1•110	7.0
MP-DATA-2•110	7.0
MP-DATA-3•110	7.0
MP-DATA-4•110	7.0
MP-DATA-5•110	7.0
MP-DATA-6•110	7.0
MP-DATA-7•110	7.0
MP-DATA-EN•040	23.0
MP-DATA-P•110	7.0
MP-PAR-ERR•120	8.0
MP-PAR-ERR•121	4.0
MP-RD•110	7.0
MP-RD-WR•100	8.0
MP-RESET-RUN•000	22.0
MP-SEL-0•020	7.0
MP-SEL-1•020	7.0
MP-SEL-2•020	7.0
MP-ST-SEQ•100	22.0
MP-WR•020	7.0
MP-WR•110	7.0
MP-WR•120	7.0
MP-WR-00•130	35.0
MP-WR-08•030	33.0
MP-WR-08-10•040	23.0
MP-WR-08-10•130	23.0
MP-WR-09•030	32.0
MP-WR-10•030	34.0
MP-WR-4•020	24.0
MP-WR-4•130	25.0
MP-WR-5•020	24.0
MP-WR-5•130	24.0
MPRD•120	7.0
MPWR•120	7.0
OP00-BUN•000	27.0
OP00-BUN•110	28.0
OP01-BEQ•000	27.0
OP01-BEQ•110	28.0
OP02-BCCE•000	27.0
OP02-BCCE•110	28.0
OP03-BSNZ•000	27.0
OP03-BSNZ•110	29.0
OP04-BBFL•000	27.0
OP04-BBFL•110	29.0
OP05-BSHT•000	27.0
OP05-BSHT•110	29.0

SIGNAL NAME	PAGE
OP06-BS01•000	27.0
OP06-BS01•110	29.0
OP07-BDS6•000	27.0
OP07-BDS6•110	29.0
OP10-BDS7•000	27.0
OP10-BDS7•110	29.0
OP11-BS01•000	27.0
OP11-BS01•110	29.0
OP12-BS02•000	27.0
OP12-BS02•110	29.0
OP13-BS03•000	27.0
OP13-BS03•110	29.0
OP14-BS21•000	27.0
OP14-BS21•110	29.0
OP15-BS22•000	27.0
OP15-BS22•110	29.0
OP16-BS23•000	27.0
OP16-BS23•110	29.0
OP17-BNFT•000	27.0
OP17-BNFT•110	29.0
OP20-DCSS•000	27.0
OP20-DCSS•110	43.0
OP21-DCSR•000	27.0
OP21-DCSR•110	44.0
OP22-23•010	34.0
OP22-LCSN•000	27.0
OP22-LCSN•010	21.0
OP23-ICSN•000	27.0
OP24-26•010	33.0
OP24-LRCT•000	27.0
OP25-7-40-2•130	41.0
OP25-IFCT•000	27.0
OP25-IFCT•110	41.0
OP26-IRCT•000	27.0
OP26-IRCT•110	41.0
OP27-ISRC•000	27.0
OP27-ISRC•110	41.0
OP31-LCMD•000	28.0
OP31-LCMD•110	31.0
OP32-LFCT•000	28.0
OP34-RCTL•000	28.0
OP34-RCTL•110	35.0
OP35-EXEC•020	37.0
OP35-SEDC•000	28.0
OP35-SEDC•010	21.0
OP35-SEDC•110	31.0
OP36-STAT•000	28.0
OP36-STAT•110	31.0
OP37-HALT•000	28.0
OP40-41-47•110	35.0
OP40-42-DS•020	42.0
OP40-42-DS•110	41.0
OP40-56•020	37.0
OP40-56•130	37.0
OP40-CCSN•000	28.0
OP40-CCSN•110	16.0
OP41-42•020	41.0
OP41-42•110	42.0
OP41-42•120	21.0
OP41-CCNF•000	28.0
OP42-CCNB•000	28.0
OP45-63-72-75•020	27.0
OP45-RDDS•000	28.0
OP45-RDDS•010	21.0
OP45-RDDS•110	42.0

SIGNAL NAME	PAGE
OP45-WDSN•030	41.0
OP46-RDTB•000	28.0
OP47-RDTF•000	28.0
OP50-66•010	20.0
OP50-66•020	21.0
OP50-RDTX•000	28.0
OP51-52•110	16.0
OP51-RECC•000	28.0
OP52-REDC•000	28.0
OP54-IDTA•000	28.0
OP57-NOP•000	28.0
OP57-NOP•110	21.0
OP60-WADM•000	28.0
OP60-WADM•110	40.0
OP61-WCSN•000	28.0
OP62-WDSN•000	28.0
OP63-64•110	37.0
OP63-64-66•020	37.0
OP63-64-66•110	37.0
OP63-72•010	27.0
OP63-72•020	21.0
OP63-72•120	27.0
OP63-WDDS•000	28.0
OP63-WDDS•110	16.0
OP64-WDTB•000	28.0
OP65-WDTF•000	28.0
OP65-WDTF•110	38.0
OP66-WDTX•000	28.0
OP67-70•020	40.0
OP67-70•110	36.0
OP67-WECC•000	28.0
OP70-WEDC•000	28.0
OP70-WEDC•110	38.0
OP71-WHEX•000	28.0
OP72-WZDS•000	28.0
OP73-WZRD•000	28.0
OP75-77•110	45.0
OP75-WZIX•000	28.0
OP77-WIDX•000	28.0
OPT-0•000	10.0
OPT-1•000	10.0
OPT-2•000	10.0
P-EDAC-DATA-P•100	19.0
PAR-F-BUFF•100	37.0
PORT-4XX•100	33.0
PORT-500•010	34.0
PORT-500•100	33.0
PORT-LD•130	33.0
PORT-SEL-0•100	33.0
PORT-SEL-1•100	33.0
PORT-SEL-2•100	33.0
PORT-SEL-3•100	33.0
PORT-SEL-E•100	33.0
PORT-SP0•100	33.0
R-EDAC-DATA-0•110	19.0
R-EDAC-DATA-1•110	19.0
R-EDAC-DATA-2•110	19.0

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TITLE LOGIC DIAGRAM- WDASE LOGIC - PAGE CROSS REFERENCE

DATA BASE NIODAU/DAU$45/HS
DR DFTG 84APR20

ASM REF 58075900-X02

SIZE B DWG NO 58075904 SH 1.2 REV A

58075904

REV	AUTHORITY	DATE
A	LEVEL3ISSUE	84APR20

SIGNAL NAME	PAGE
R-EDAC-DATA-3•110	19.0
R-EDAC-DATA-4•110	19.0
R-EDAC-DATA-5•110	19.0
R-EDAC-DATA-6•110	19.0
R-EDAC-DATA-7•110	19.0
R-EQUAL•140	42.0
R-EQUAL•141	5.0
RCT-ALL-1•100	34.0
RCT-CNT-0•100	34.0
RCT-CNT-1•100	34.0
RCT-CNT-2•100	34.0
RCT-CNT-3•100	34.0
RCT-CNT-4•100	33.0
RCT-CNT-5•100	33.0
RCT-CNT-6•100	33.0
RCT-CNT-7•100	33.0
RCT-LD•040	33.0
RCT-LSB-1•100	33.0
RCT-PE•040	33.0
RCT-PE•041	4.0
RD-NINH•020	16.0
RESET-DCS•040	44.0
REV-0•100	13.0
REV-1•100	13.0
REV-2•100	13.0
REV-3•100	13.0
REV-4•100	13.0
REV-5•100	13.0
REV-6•100	13.0
REV-7•100	13.0
S-EQUAL•140	42.0
S-EQUAL•141	4.0
S-EQUAL-A•020	42.0
S-EQUAL-B•030	42.0
SEDC-4-CN•100	31.0
SEDC-4-CN•110	19.0
SEDC-4-DT•100	31.0
SEDC-4-DT•110	19.0
SEDC-5-512•100	31.0
SEDC-5-512•110	19.0
SEDC-5-64•100	31.0
SEDC-5-64•110	19.0
SEDC-5-C0•100	31.0
SEDC-5-C0•110	19.0
SEDC-5-CN•100	31.0
SEDC-5-CN•110	19.0
SEDC-DATA•100	31.0
SEDC-LD•100	31.0
SEDC-S-512•100	31.0
SEDC-S-64•100	31.0
SEDC-S-C0•100	31.0
SEDC-S-CN•100	31.0
SEDC-SP0•100	31.0
SEL-SEQ-RW•130	7.0
SELECT-SEQ•120	7.0
SEQ-ADDR-0•100	24.0
SEQ-ADDR-1•100	24.0
SEQ-ADDR-2•100	24.0
SEQ-ADDR-3•100	24.0
SEQ-ADDR-4•100	24.0
SEQ-ADDR-5•100	24.0
SEQ-ADDR-6•100	24.0
SEQ-ADDR-7•100	24.0
SEQ-ADDR-8•100	24.0
SEQ-ADDR-9•100	24.0
SEQ-ADDR-LSB•100	24.0
SEQ-ADDR-NSB•100	24.0
SEQ-ADR-SET•130	22.0
SEQ-ANY-ERR•120	18.0
SEQ-BRANCH•000	30.0
SEQ-BRANCH•100	30.0
SEQ-CTR-INC•130	27.0
SEQ-DATA-00•010	27.0
SEQ-DATA-00•100	24.0
SEQ-DATA-00•100	25.0
SEQ-DATA-01•010	27.0
SEQ-DATA-01•100	25.0
SEQ-DATA-01•100	24.0
SEQ-DATA-02•010	27.0
SEQ-DATA-02•100	24.0
SEQ-DATA-02•100	25.0
SEQ-DATA-03•100	25.0
SEQ-DATA-03•100	24.0
SEQ-DATA-04•100	25.0
SEQ-DATA-05•100	25.0
SEQ-DATA-08•100	26.0
SEQ-DATA-08•100	25.0
SEQ-DATA-09•100	26.0
SEQ-DATA-09•100	25.0
SEQ-DATA-10•100	25.0
SEQ-DATA-10•100	26.0
SEQ-DATA-11•100	26.0
SEQ-DATA-11•100	25.0
SEQ-DATA-12•100	26.0
SEQ-DATA-12•100	25.0
SEQ-DATA-13•100	26.0
SEQ-DATA-13•100	25.0
SEQ-DATA-14•100	25.0
SEQ-DATA-14•100	26.0
SEQ-DATA-15•100	25.0
SEQ-DATA-15•100	26.0
SEQ-DATA-P0•100	25.0
SEQ-DATA-P1•100	25.0
SEQ-ERR•110	18.0
SEQ-ERR•120	18.0
SEQ-EXEC-SET•020	21.0
SEQ-EXEC-SET•130	22.0
SEQ-INCR•000	30.0
SEQ-INCR•110	30.0
SEQ-INCR•111	5.0
SEQ-PE•120	26.0
SEQ-PE-0•000	26.0
SEQ-PE-0-1•110	26.0
SEQ-PE-1•000	26.0
SEQ-RESET•030	22.0
SEQ-RESET•031	22.0
SEQ-RESET•120	22.0
SEQ-RO-0•100	13.0
SEQ-RO-1•100	13.0
SEQ-RO-2•100	13.0
SEQ-RO-3•100	13.0
SEQ-RO-4•100	13.0
SEQ-RO-5•100	13.0
SEQ-RO-6•100	13.0
SEQ-RO-7•100	13.0
SEQ-RO-P•000	13.0
SEQ-RO-P•100	14.0
SEQ-RO-SW-0•100	11.0
SEQ-RO-SW-0•100	10.0
SEQ-RO-SW-0•100	8.0
SEQ-RO-SW-1•100	9.0
SEQ-RO-SW-1•100	10.0
SEQ-RO-SW-1•100	12.0
SEQ-RO-SW-2•100	12.0
SEQ-RO-SW-2•100	10.0
SEQ-RO-SW-2•100	9.0
SEQ-RO-SW-3•100	12.0
SEQ-RO-SW-3•100	9.0
SEQ-RO-SW-3•100	11.0
SEQ-RO-SW-4•100	9.0
SEQ-RO-SW-4•100	11.0
SEQ-RO-SW-4•100	12.0
SEQ-RO-SW-5•100	11.0
SEQ-RO-SW-5•100	12.0
SEQ-RO-SW-5•100	9.0
SEQ-RO-SW-6•100	11.0
SEQ-RO-SW-6•100	9.0
SEQ-RO-SW-6•100	12.0
SEQ-RO-SW-7•100	11.0
SEQ-RO-SW-7•100	10.0
SEQ-RO-SW-7•100	13.0
SEQ-RUN-R1•020	21.0
SEQ-RUN-R2•020	21.0
SEQ-RUN-R3•020	22.0
SEQ-RUN-R3-0•010	21.0
SEQ-RUN-R3-1•010	21.0
SEQ-RUN-RST•130	22.0
SEQ-ST-LSB•100	26.0
SEQ-ST-ONES•100	26.0
SEQ-STATE-0•100	26.0
SEQ-STATE-1•100	26.0
SEQ-STATE-2•100	26.0
SEQ-STATE-3•100	26.0
SEQ-STATE-4•100	26.0
SEQ-STATE-5•100	26.0
SEQ-STATE-5•110	19.0
SEQ-STATE-6•100	26.0
SEQ-STATE-6•110	19.0
SEQ-STATE-7•100	26.0
SEQ-STATE-7•110	19.0
SET-LST-BYT•130	38.0
SET-TTE•100	42.0
SHORT-BLK•110	17.0
SRC-ALL-1•100	33.0
SRC-CNT-0•100	33.0
SRC-CNT-1•100	33.0
SRC-CNT-2•100	33.0
SRC-CNT-3•100	33.0
SRC-INC•110	32.0
SRC-LD•040	32.0
SRI-IN•020	40.0
STAT-C-CCE•100	32.0
STAT-C-CNE•100	32.0
STAT-D-CCE•100	32.0
STAT-D-SYE•100	32.0
STAT-ERR•100	32.0
STAT-ERR•110	18.0
STAT-LD•120	31.0
STAT-LD•121	4.0
STAT-NO-DATA•100	32.0
STAT-SH-BLK•100	32.0
STOP-CLK•030	17.0
STOP-CLK•121	17.0
SW-MP-SEQ-0•100	23.0
SW-MP-SEQ-1•100	23.0
SW-MP-SEQ-2•100	23.0
SW-MP-SEQ-3•100	23.0
SW-MP-SEQ-4•100	23.0
SW-MP-SEQ-5•100	23.0
SW-MP-SEQ-6•100	23.0
SW-MP-SEQ-7•100	23.0
SWO-OUT•010	40.0
SYNC-BYTE•120	18.0
TEST-DCS•000	44.0
TEST-EXEC•000	23.0
TEST-STRT-SWO•000	43.0
TTE-SYNC-ER•010	21.0
WR-LAST•020	38.0
WR-LST-BYT•130	37.0

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TITLE LOGIC DIAGRAM- WDASE LOGIC - PAGE CROSS REFERENCE

ASM REF 58075900-X02

DATA BASE NIODAU/DAU$45/HSE

DR DFTG 84APR20

SIZE	DWG NO	SH	REV
B	58075904	1.3	A

58075904

I/O PIN		PAGE	SIGNAL NAME
LDØ3	O	4.Ø	RCT-PE•Ø41
LDØ4	O	4.Ø	S-EQUAL•141
LDØ6	O	4.Ø	STAT-LD•121
LDØ7	O	4.Ø	$LD-SEQ-ADDR-LSB•Ø21
LDØ8	O	4.Ø	DSW-CNTL-1•131
LD1Ø	O	4.Ø	DSW-CNTL-4•131
LD12	O	4.Ø	EDAC-RSTB•131
LD13	O	4.Ø	DSW-CNTL-2•131
LD14	O	4.Ø	$SEQ-CTR-LD•Ø11
LD15	O	4.Ø	CSYN-LD•Ø41
LD16	O	4.Ø	MP-PAR-ERR•121
LD18	O	4.Ø	EDAC-WSTB•131
LD19	O	4.Ø	BUFF-WSTB•131
LD2Ø	O	4.Ø	BUFF-RSTB•131
RAØ1	O	4.Ø	FSEQ-EXEC•1Ø2
RAØ2	O	4.Ø	FSEQ-ADDR-LD•1Ø1
RAØ3	O	4.Ø	FSEQ-RUN•1Ø1
RAØ4	I	5.Ø	HI-LVL-Ø•1ØØ
RAØ5	O	4.Ø	FSEQ-SYNC•ØØ1
RAØ6	O	4.Ø	FSTRT-SWO•1Ø1
RAØ7	O	4.Ø	FINDEX•1Ø1
RAØ8	I	5.Ø	HI-LVL-1•1ØØ
RAØ9	O	4.Ø	DEC-BRAN-1•Ø21
RA1Ø	O	4.Ø	DEC-BRAN-2•Ø21
RA12	O	4.Ø	DEC-BRAN-3•Ø21
RA13	O	5.Ø	SEQ-INCR•111
RA14	O	5.Ø	R-EQUAL•141
RA15	O	4.Ø	DEC-BRAN-Ø•Ø21
RA16	I	5.Ø	HI-LVL-2•1ØØ
RA17	O	5.Ø	FLAST-BYTE•1Ø1
RA18	O	5.Ø	FWDDS-DTB•1Ø1
RA19	I	5.Ø	HI-LVL-3•1ØØ
RBØ1	I	29.Ø	D-SUB-BRAN•ØØØ
RBØ2	I	29.Ø	D-DIS-BRAN•ØØØ
RDØØ	I	44.Ø	TEST-DCS•ØØØ
RDØ1	I	43.Ø	TEST-STRT-SWO•ØØØ
RDØ2	I	23.Ø	TEST-EXEC•ØØØ
WAØ2	I	17.Ø	STOP-CLK•121
WAØ3	I	1Ø.Ø	OPT-Ø•ØØØ
WAØ7	I	1Ø.Ø	OPT-1•ØØØ
WAØ9	I	1Ø.Ø	OPT-2•ØØØ
WA12	O	13.Ø	SEQ-RO-Ø•1ØØ
WA13	O	13.Ø	SEQ-RO-1•1ØØ
WA14	O	13.Ø	SEQ-RO-2•1ØØ
WA15	O	13.Ø	SEQ-RO-3•1ØØ
WA16	O	13.Ø	SEQ-RO-4•1ØØ
WA17	O	13.Ø	SEQ-RO-5•1ØØ
WA18	O	13.Ø	SEQ-RO-6•1ØØ
WA19	O	13.Ø	SEQ-RO-7•1ØØ
WA2Ø	O	14.Ø	SEQ-RO-P•1ØØ
WBØØ	O	16.Ø	FCMD-DCP-ØSØ•1ØØ
WBØ1	O	16.Ø	FCMD-DCØ-ØSØ•1ØØ
WBØ2	O	16.Ø	FCMD-DC1-ØSØ•1ØØ
WBØ3	O	16.Ø	FCMD-DC2-ØSØ•1ØØ
WBØ4	O	16.Ø	FCMD-DC3-ØSØ•1ØØ
WBØ5	O	16.Ø	FCMD-DC4-ØSØ•1ØØ
WBØ6	O	16.Ø	FCMD-DC5-ØSØ•1ØØ
WBØ7	O	16.Ø	FCMD-DCS-ØSD•1ØØ
WB1Ø	O	15.Ø	DDAI-INIT-ØS1•1ØØ
WB12	O	15.Ø	DINIT-DIN-ØSØ•1ØØ
WB15	O	15.Ø	DRD-FR-DEV-ØSØ•1ØØ
WB19	O	15.Ø	DCONT-OUT-ØSØ•1ØØ
WCØØ	O	15.Ø	FDTA-O-D1P-ØSØ•1ØØ
WCØ1	O	15.Ø	FDTA-O-D1Ø-ØSØ•1ØØ
WCØ2	O	15.Ø	FDTA-O-D11-ØSØ•1ØØ

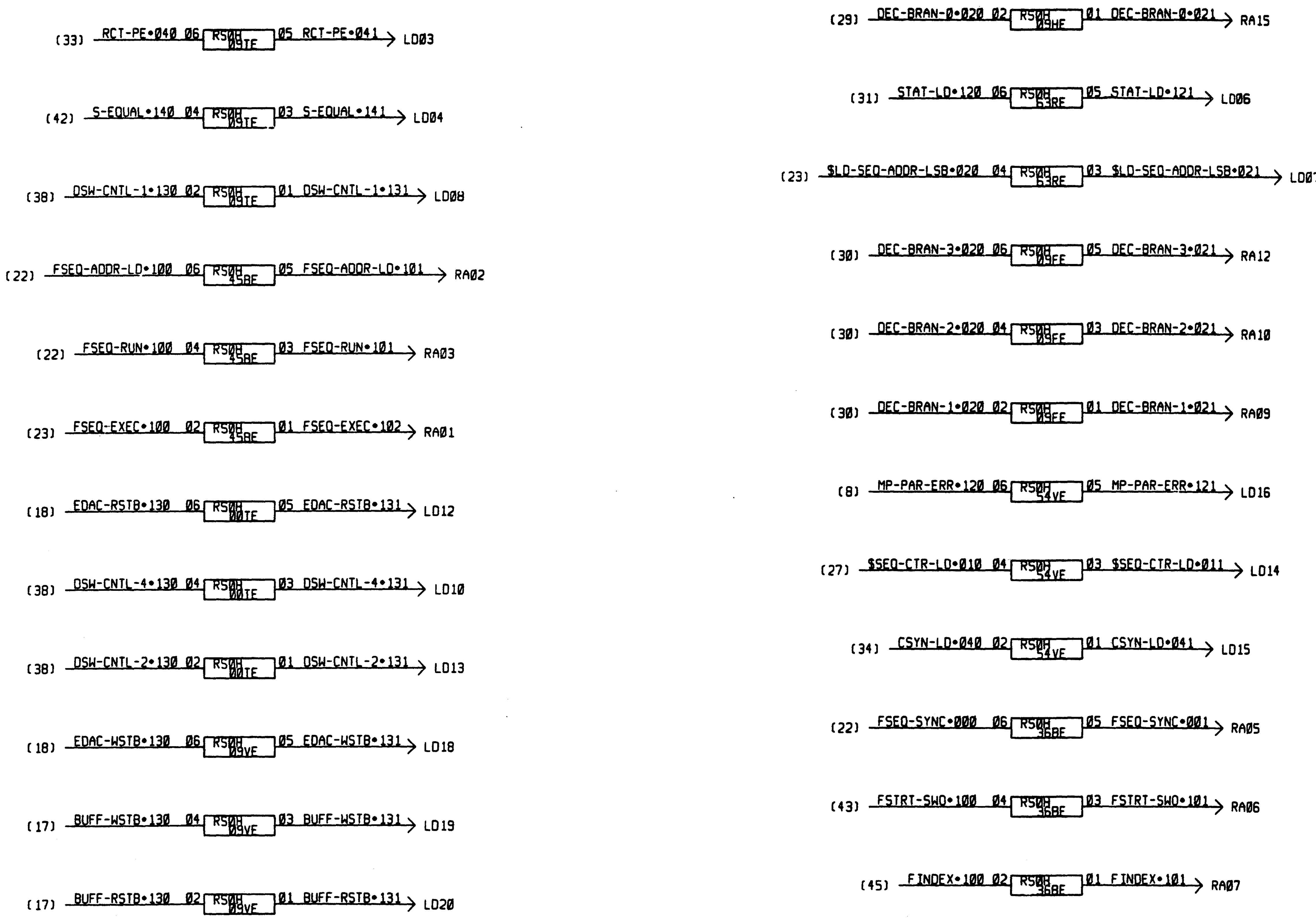
I/O PIN		PAGE	SIGNAL NAME
WCØ3	O	15.Ø	FDTA-O-D12-ØSØ•1ØØ
WCØ4	O	15.Ø	FDTA-O-D13-ØSØ•1ØØ
WCØ5	O	15.Ø	FDTA-O-D14-ØSØ•1ØØ
WCØ6	O	15.Ø	FDTA-O-D15-ØSØ•1ØØ
WCØ7	O	15.Ø	FDTA-O-D16-ØSØ•1ØØ
WCØ8	O	15.Ø	FDTA-O-D17-ØSØ•1ØØ
WCØ9	O	15.Ø	FDTA-M-DM1-ØSØ•1ØØ
WC12	O	16.Ø	FDEV-SEL-2-ØSØ•1ØØ
WC13	O	16.Ø	FDEV-SEL-3-ØSØ•1ØØ
WC14	O	16.Ø	DBRD-SEL-Ø-ØSØ•1ØØ
WC15	O	16.Ø	DBRD-SEL-1-ØSØ•1ØØ
WC16	O	16.Ø	DBRD-SEL-2-ØSØ•1ØØ
WC17	O	16.Ø	DBRD-SEL-3-ØSØ•1ØØ
WC18	O	16.Ø	DBRD-SEL-4-ØSØ•1ØØ
WC19	O	16.Ø	DBRD-SEL-5-ØSØ•1ØØ
WC2Ø	I	14.Ø	DSR-RD-SRI-ØSØ•1ØØ
WDØØ	I	14.Ø	DDTA-I-D1P-ØSØ•1ØØ
WDØ1	I	14.Ø	DDTA-I-D1Ø-ØSØ•1ØØ
WDØ2	I	14.Ø	DDTA-I-D11-ØSØ•1ØØ
WDØ3	I	14.Ø	DDTA-I-D12-ØSØ•1ØØ
WDØ4	I	14.Ø	DDTA-I-D13-ØSØ•1ØØ
WDØ5	I	14.Ø	DDTA-I-D14-ØSØ•1ØØ
WDØ6	I	14.Ø	DDTA-I-D15-ØSØ•1ØØ
WDØ7	I	14.Ø	DDTA-I-D16-ØSØ•1ØØ
WDØ8	I	14.Ø	DDTA-I-D17-ØSØ•1ØØ
WDØ9	O	16.Ø	DBRD-SEL-6-ØSØ•1ØØ
WD1Ø	O	16.Ø	DBRD-SEL-7-ØSØ•1ØØ
WD12	I	15.Ø	DINDEX-IDX-ØSØ•1ØØ
WD13	I	15.Ø	DFAULT-FLT-ØSØ•1ØØ
WD14	I	15.Ø	DOPER-OPI-ØSØ•1ØØ
WD15	O	14.Ø	FSEQ-RUN•11Ø
WD2Ø	I	15.Ø	DMP-ERROR•11Ø
WEØ2	I	5.Ø	$DAU•Ø1Ø
WE1Ø	I	7.Ø	DSEL-SEØ•11Ø
WE12	I	19.Ø	R-EDAC-DATA-Ø•11Ø
WE13	I	19.Ø	R-EDAC-DATA-1•11Ø
WE14	I	19.Ø	R-EDAC-DATA-2•11Ø
WE15	I	19.Ø	R-EDAC-DATA-3•11Ø
WE16	I	19.Ø	R-EDAC-DATA-4•11Ø
WE17	I	19.Ø	R-EDAC-DATA-5•11Ø
WE18	I	19.Ø	R-EDAC-DATA-6•11Ø
WE19	I	19.Ø	R-EDAC-DATA-7•11Ø
WE2Ø	I	19.Ø	P-EDAC-DATA-P•1ØØ
WE21	I	5.Ø	$PARTIAL-CLR•Ø11
WFØ1	O	18.Ø	MODE-RAR•11Ø
WFØ2	O	18.Ø	DEV-4XX-5ØØ•12Ø
WFØ3	O	18.Ø	DEV-5Ø1•12Ø
WFØ4	O	18.Ø	SYNC-BYTE•12Ø
WFØ5	I	5.Ø	$DAU-TOT-CLR•Ø11
WFØ6	O	18.Ø	SEQ-ERR•12Ø
WFØ7	O	18.Ø	STAT-ERR•11Ø
WF1Ø	O	19.Ø	SEDC-4-CN•11Ø
WF12	O	19.Ø	SEDC-4-DT•11Ø
WF13	O	19.Ø	SEDC-5-CØ•11Ø
WF14	O	19.Ø	SEDC-5-CN•11Ø
WF15	O	19.Ø	SEDC-5-64•11Ø
WF16	O	19.Ø	SEDC-5-512•11Ø
WF17	O	19.Ø	CMD-WRITE•12Ø
WF18	O	19.Ø	EDAC-CLEAR•13Ø
WF19	O	19.Ø	LAST-EDAC•13Ø
WF2Ø	O	19.Ø	EDAC-BYTES•12Ø
WF21	O	19.Ø	CMD-WR-DCS•12Ø
WGØØ	I	7.Ø	DMPADR-15•1ØØ
WGØ2	I	7.Ø	DMPADR-14•1ØØ
WGØ3	I	7.Ø	DMPADR-13•1ØØ

I/O PIN		PAGE	SIGNAL NAME
WGØ4	I	7.Ø	DMPADR-12•1ØØ
WGØ5	I	7.Ø	DMPADR-11•1ØØ
WGØ6	I	7.Ø	DMPDTA-Ø•1ØØ
WGØ7	I	7.Ø	DMPDTA-1•1ØØ
WGØ8	I	7.Ø	DMPDTA-2•1ØØ
WGØ9	I	7.Ø	DMPDTA-3•1ØØ
WG1Ø	I	7.Ø	DMPDTA-4•1ØØ
WG12	I	7.Ø	DMPDTA-5•1ØØ
WG13	I	7.Ø	DMPDTA-6•1ØØ
WG14	I	7.Ø	DMPDTA-7•1ØØ
WG15	I	7.Ø	DMPDTA-P•1ØØ
WG16	I	7.Ø	MPWR•12Ø
WG17	I	8.Ø	DMPADR-P•1ØØ
WG18	I	2Ø.Ø	CYHD-FULL•Ø1Ø
WG19	I	7.Ø	MPRD•12Ø
WG2Ø	O	19.Ø	FMP-ADDR-ERR•Ø1Ø
WHØØ	O	19.Ø	DREG-Ø•11Ø
WHØ1	O	19.Ø	DREG-1•11Ø
WHØ2	O	19.Ø	DREG-2•11Ø
WHØ3	O	19.Ø	DREG-3•11Ø
WHØ4	O	19.Ø	DREG-4•11Ø
WHØ5	O	19.Ø	DREG-5•11Ø
WHØ6	O	19.Ø	DREG-6•11Ø
WHØ7	O	19.Ø	DREG-7•11Ø
WHØ8	O	19.Ø	DREG-P•11Ø
WHØ9	O	17.Ø	BUFF-STB•13Ø
WH1Ø	I	2Ø.Ø	DEFECT-SKP•12Ø
WH12	I	17.Ø	BREG-ØØ•11Ø
WH13	I	17.Ø	BREG-Ø1•11Ø
WH14	I	17.Ø	BREG-Ø2•11Ø
WH15	I	17.Ø	BREG-Ø3•11Ø
WH16	I	17.Ø	BREG-Ø4•11Ø
WH17	I	17.Ø	BREG-Ø5•11Ø
WH18	I	17.Ø	BREG-Ø6•11Ø
WH19	I	17.Ø	BREG-Ø7•11Ø
WH2Ø	I	17.Ø	BREG-P•11Ø
WJØØ	I	17.Ø	BUF-FULL•11Ø
WJØ1	I	17.Ø	SHORT-BLK•11Ø
WJØ2	I	17.Ø	LAST-DATA•11Ø
WJØ3	I	19.Ø	B-REG-READY•11Ø
WJØ4	I	19.Ø	F-EDAC-READY•11Ø
WJØ5	I	19.Ø	F-EDAC-ERROR•11Ø
WJØ6	O	19.Ø	SEQ-STATE-5•11Ø
WJØ7	O	19.Ø	SEQ-STATE-6•11Ø
WJØ8	O	19.Ø	SEQ-STATE-7•11Ø
WJØ9	O	19.Ø	EDAC-STB•13Ø
WJ1Ø	I	2Ø.Ø	DOUBLE-DEF•12Ø
WJ12	O	2Ø.Ø	CSYN-CNT-Ø•11Ø
WJ13	O	2Ø.Ø	CSYN-CNT-1•11Ø
WJ14	O	2Ø.Ø	CSYN-CNT-2•11Ø
WJ15	O	2Ø.Ø	CSYN-CNT-3•11Ø
WJ16	O	2Ø.Ø	CSYN-CNT-4•11Ø
WJ17	O	2Ø.Ø	CSYN-CNT-5•11Ø
WJ18	O	2Ø.Ø	CSYN-CNT-6•11Ø
WJ19	O	2Ø.Ø	CSYN-CNT-7•11Ø
WKØØ	O	2Ø.Ø	DEV-4XX•11Ø
WKØ1	O	2Ø.Ø	FSEQ-EXEC•11Ø

58Ø759Ø4

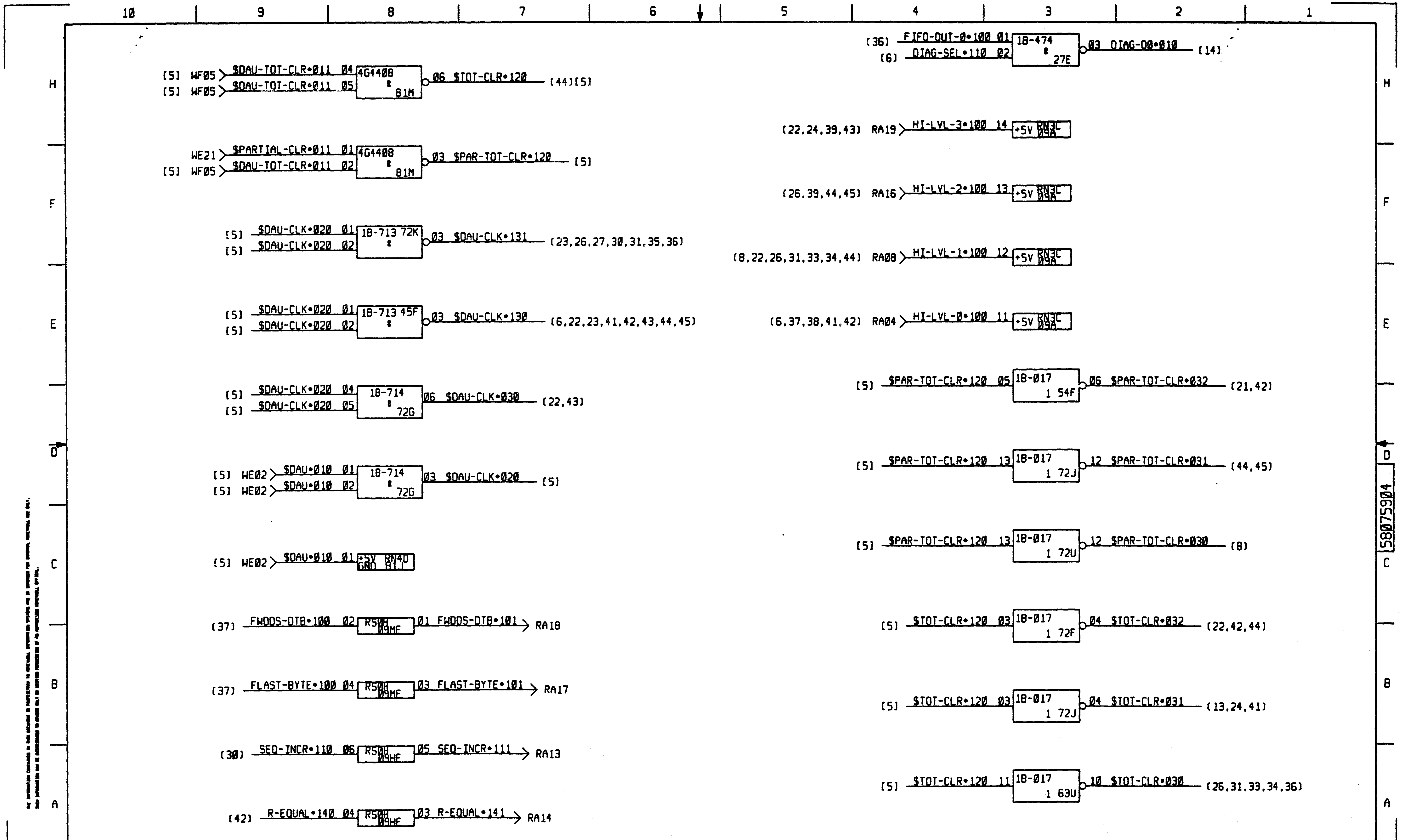
LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE I/O PIN - PAGE CROSS REFERENCE	SIZE B	DWG NO 58Ø759Ø4	SH 3.Ø	REV A

I/O PIN		PAGE	SIGNAL NAME
WK02	O	21.0	OP35-SEDC•010
WK03	O	21.0	OP45-RDDS•010
WK04	O	21.0	OP22-LCSN•010
WK05	O	21.0	OP50-66•020
WK06	O	21.0	OP41-42•120
WK07	O	21.0	OP63-72•020
WK08	I	20.0	DS-0-B1•110
WK09	I	20.0	DS-0-B2•110
WK10	I	20.0	DS-0-B3•110
WK12	I	20.0	DS-2-B1•110
WK13	I	20.0	DS-2-B2•110
WK14	I	20.0	DS-2-B3•110
WK15	I	20.0	BYTE-CTR-ONES•110
WK16	I	20.0	DEF-SKP-INH•110
WK17	I	20.0	DEF-SYNC-ERR•010
WK18	I	20.0	DEF-WHEX•030
WK19	I	20.0	DEF-WDSN•030
WK20	I	20.0	COMPARE•120



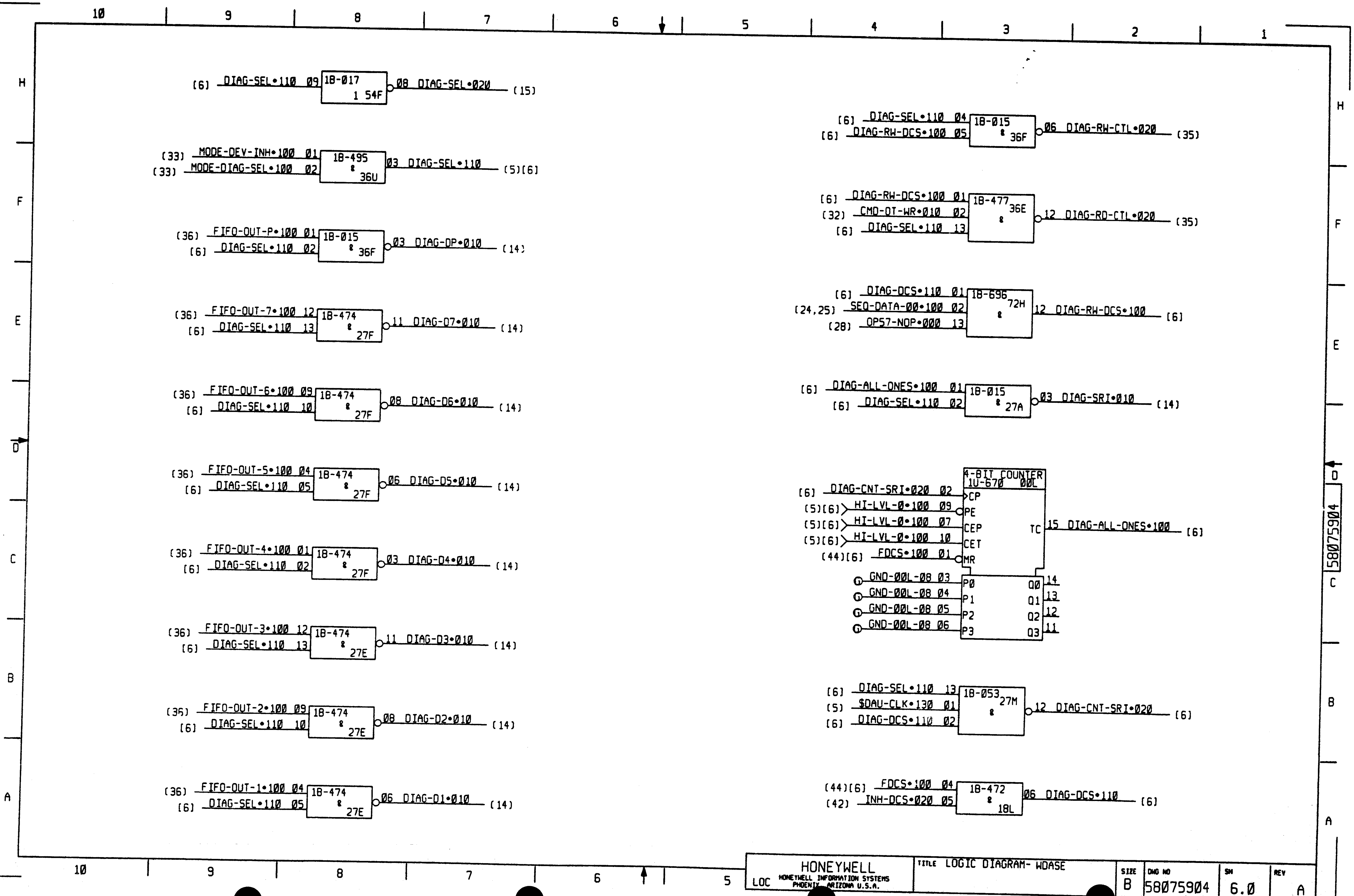
58075904

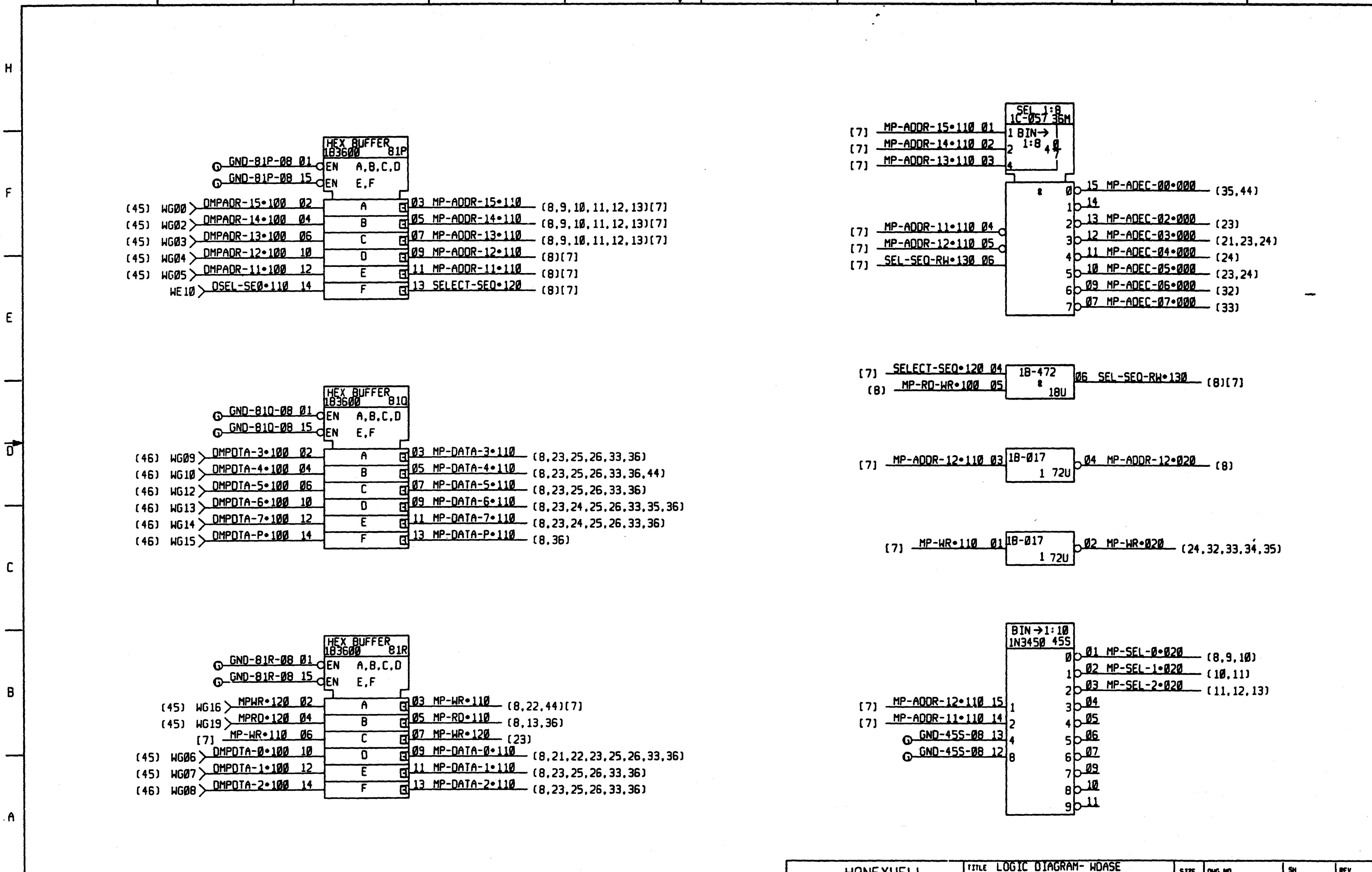
LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 4.0	REV A



HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

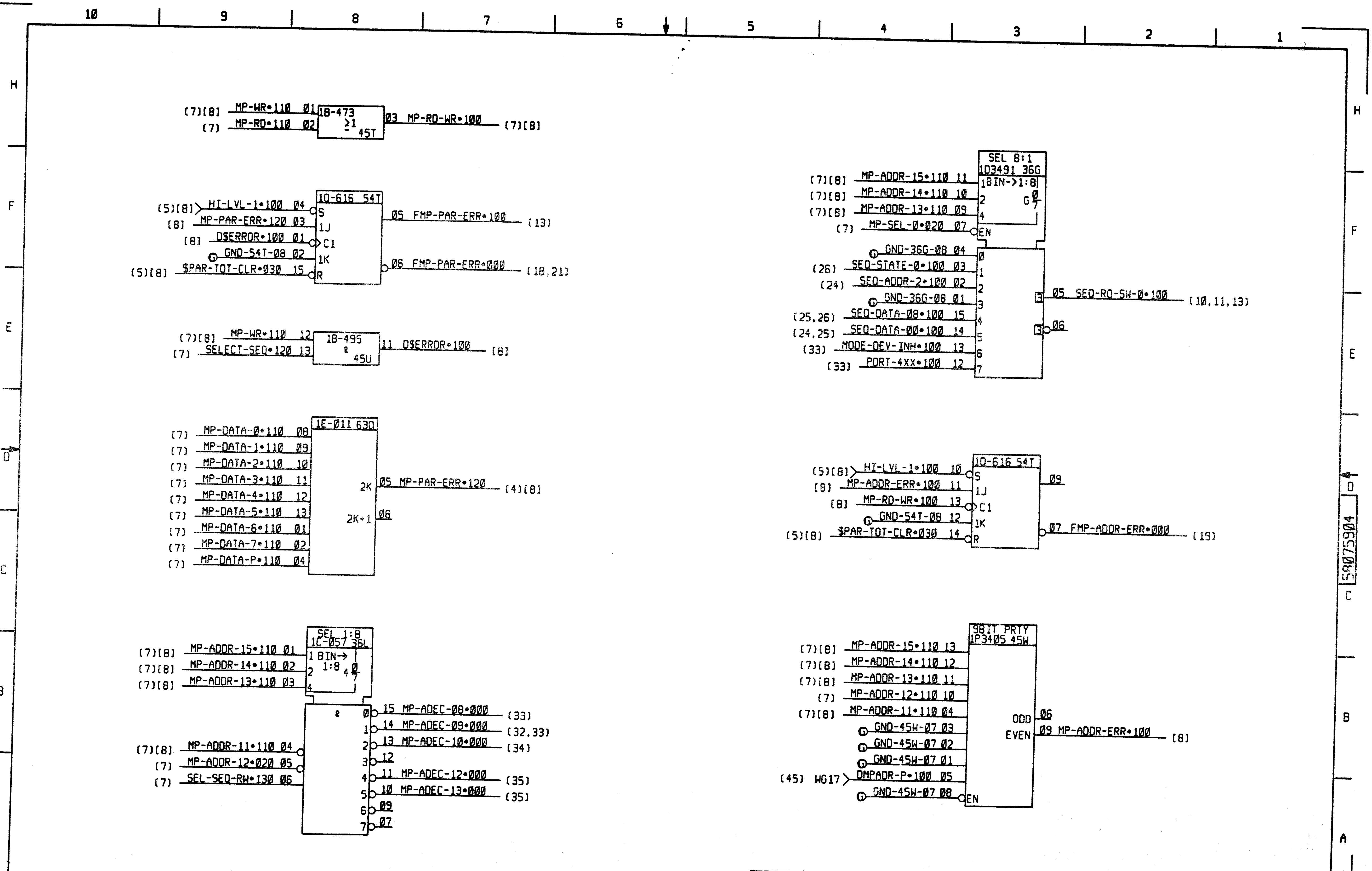
TITLE	SIZE	DWG NO	SH	REV
LOGIC DIAGRAM- WDASE	B	58Ø759Ø4	5.Ø	A


[6] DIAG-SEL•110 09 1B-017 1 54F 08 DIAG-SEL•020 [15]
[33] MODE-DEV-INH•100 01
[33] MODE-DIAG-SEL•100 02 1B-495 & 36U 03 DIAG-SEL•110 [5][6]
[36] FIFO-OUT-P•100 01
[6] DIAG-SEL•110 02 1B-015 & 36F 03 DIAG-DP•010 [14]
[36] FIFO-OUT-7•100 12
[6] DIAG-SEL•110 13 1B-474 & 27F 11 DIAG-D7•010 [14]
[36] FIFO-OUT-6•100 09
[6] DIAG-SEL•110 10 1B-474 & 27F 08 DIAG-D6•010 [14]
[36] FIFO-OUT-5•100 04
[6] DIAG-SEL•110 05 1B-474 & 27F 06 DIAG-D5•010 [14]
[36] FIFO-OUT-4•100 01
[6] DIAG-SEL•110 02 1B-474 & 27F 03 DIAG-D4•010 [14]
[36] FIFO-OUT-3•100 12
[6] DIAG-SEL•110 13 1B-474 & 27E 11 DIAG-D3•010 [14]
[36] FIFO-OUT-2•100 09
[6] DIAG-SEL•110 10 1B-474 & 27E 08 DIAG-D2•010 [14]
[36] FIFO-OUT-1•100 04
[6] DIAG-SEL•110 05 1B-474 & 27E 06 DIAG-D1•010 [14]
[6] DIAG-SEL•110 04
[6] DIAG-RW-DCS•100 05 1B-015 & 36F 06 DIAG-RW-CTL•020 [35]
[6] DIAG-RW-DCS•100 01
[32] CMD-OT-WR•010 02
[6] DIAG-SEL•110 13 1B-477 36E & 12 DIAG-RD-CTL•020 [35]
[6] DIAG-DCS•110 01
[24,25] SEQ-DATA-00•100 02
[28] OP57-NOP•000 13 1B-696 72H & 12 DIAG-RW-DCS•100 [6]
[6] DIAG-ALL-ONES•100 01
[6] DIAG-SEL•110 02 1B-015 & 27A 03 DIAG-SRI•010 [14]
4-BIT COUNTER 1U-670 00L
[6] DIAG-CNT-SRI•020 02 CP
[5][6] HI-LVL-0•100 09 PE
[5][6] HI-LVL-0•100 07 CEP
[5][6] HI-LVL-0•100 10 CET
[44][6] FDCS•100 01 MR
TC 15 DIAG-ALL-ONES•100 [6]
GND-00L-08 03 P0 Q0 14
GND-00L-08 04 P1 Q1 13
GND-00L-08 05 P2 Q2 12
GND-00L-08 06 P3 Q3 11
[6] DIAG-SEL•110 13
[5] $DAU-CLK•130 01
[6] DIAG-DCS•110 02 1B-053 27M & 12 DIAG-CNT-SRI•020 [6]
[44][6] FDCS•100 04
[42] INH-DCS•020 05 1B-472 & 18L 06 DIAG-DCS•110 [6]
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- WDASE
SIZE B
DWG NO 58075904
SH 6.0
REV A
58075904



HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE	SIZE	DWG NO	SH	REV
LOGIC DIAGRAM- WDASE	B	58075904	7.0	A

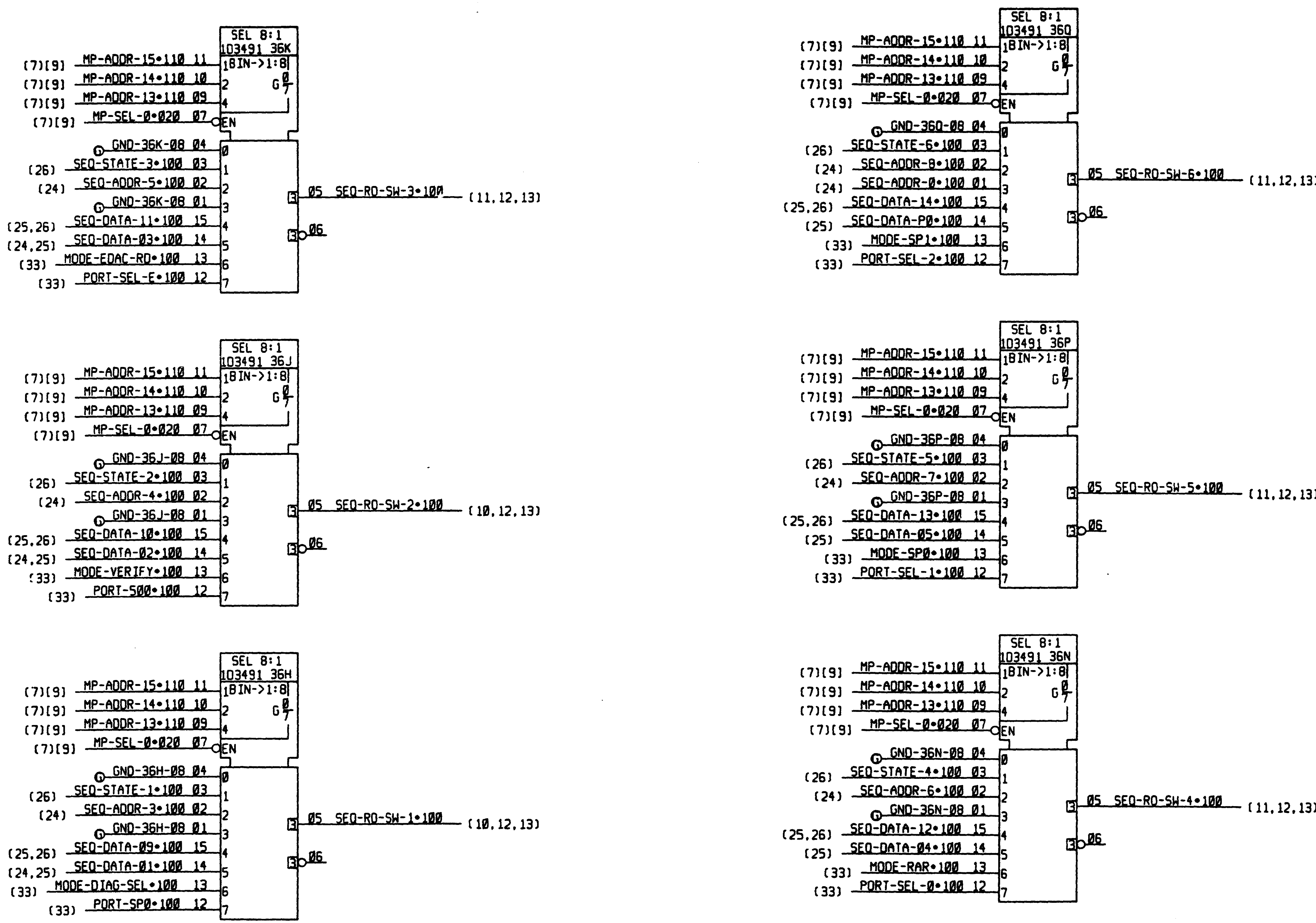


HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

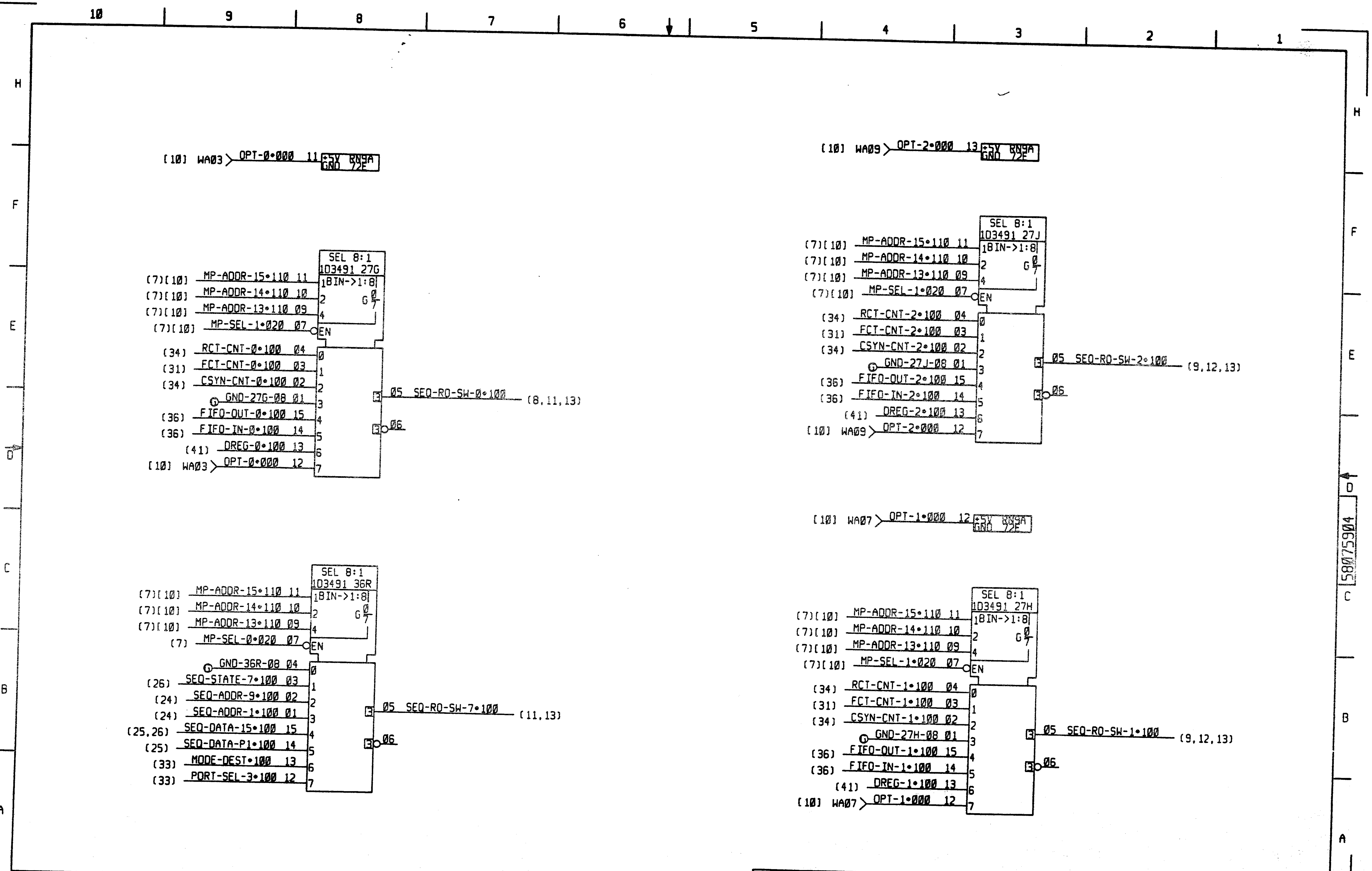
TITLE LOGIC DIAGRAM- WDASE

SIZE	DWG NO	SH	REV
B	58075904	8.0	A



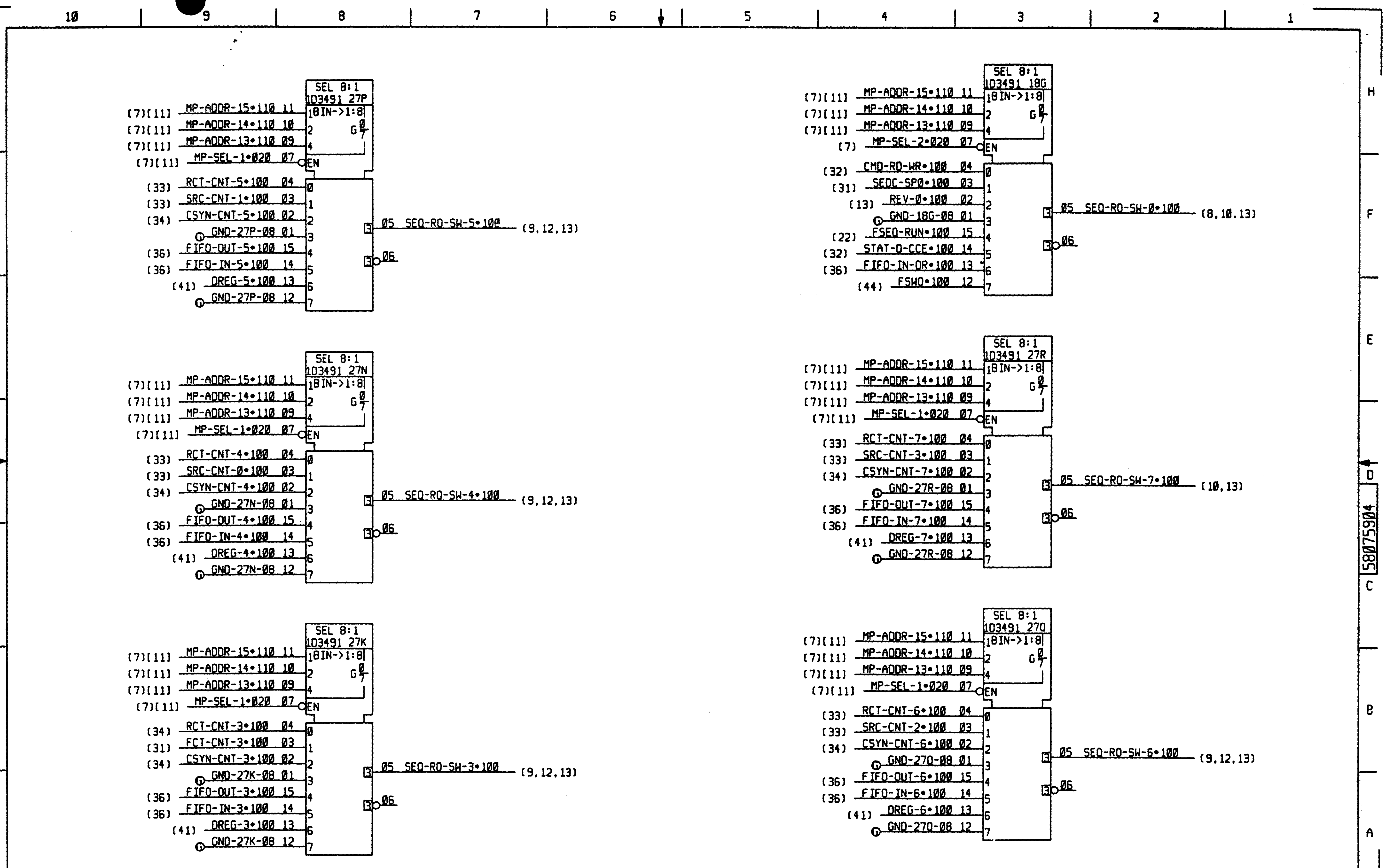
58075904

HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 9.0	REV A



LOC HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

TITLE	SIZE	DWG NO	SH	REV
LOGIC DIAGRAM- WDASE	B	58075904	10.0	A

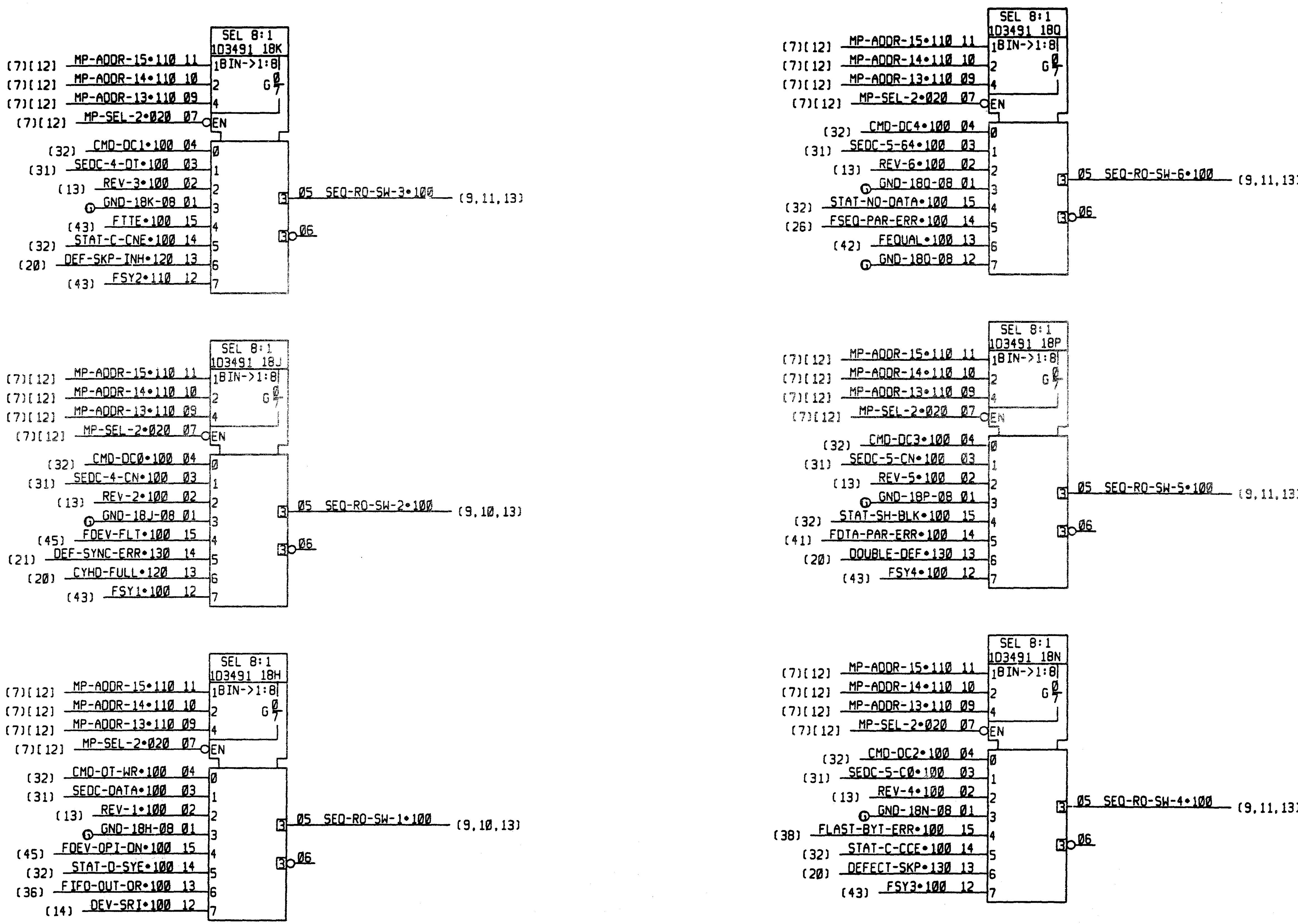


HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

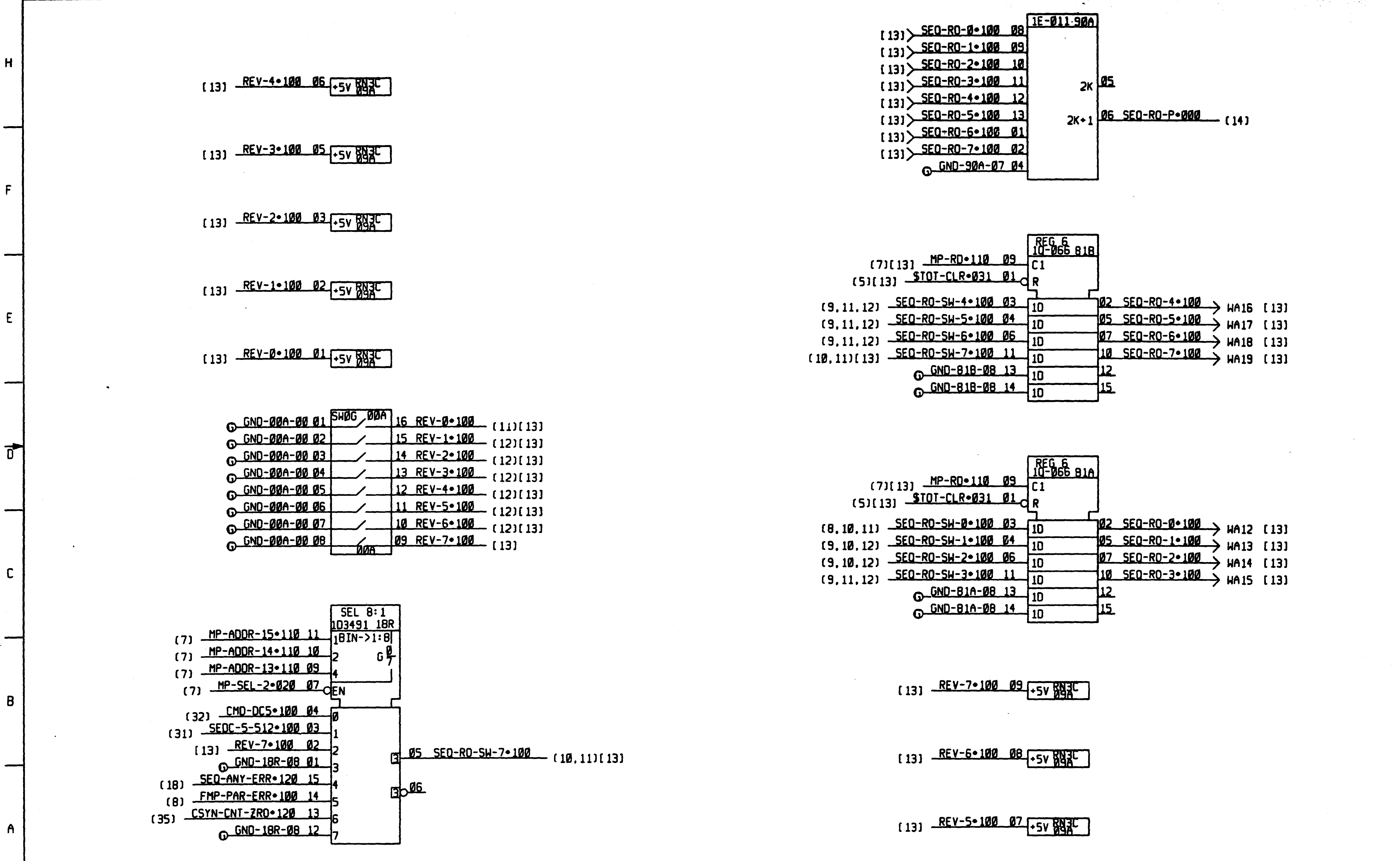
TITLE LOGIC DIAGRAM- WDASE

SIZE	DWG NO	SH	REV
B	58075904	11 Ø	A



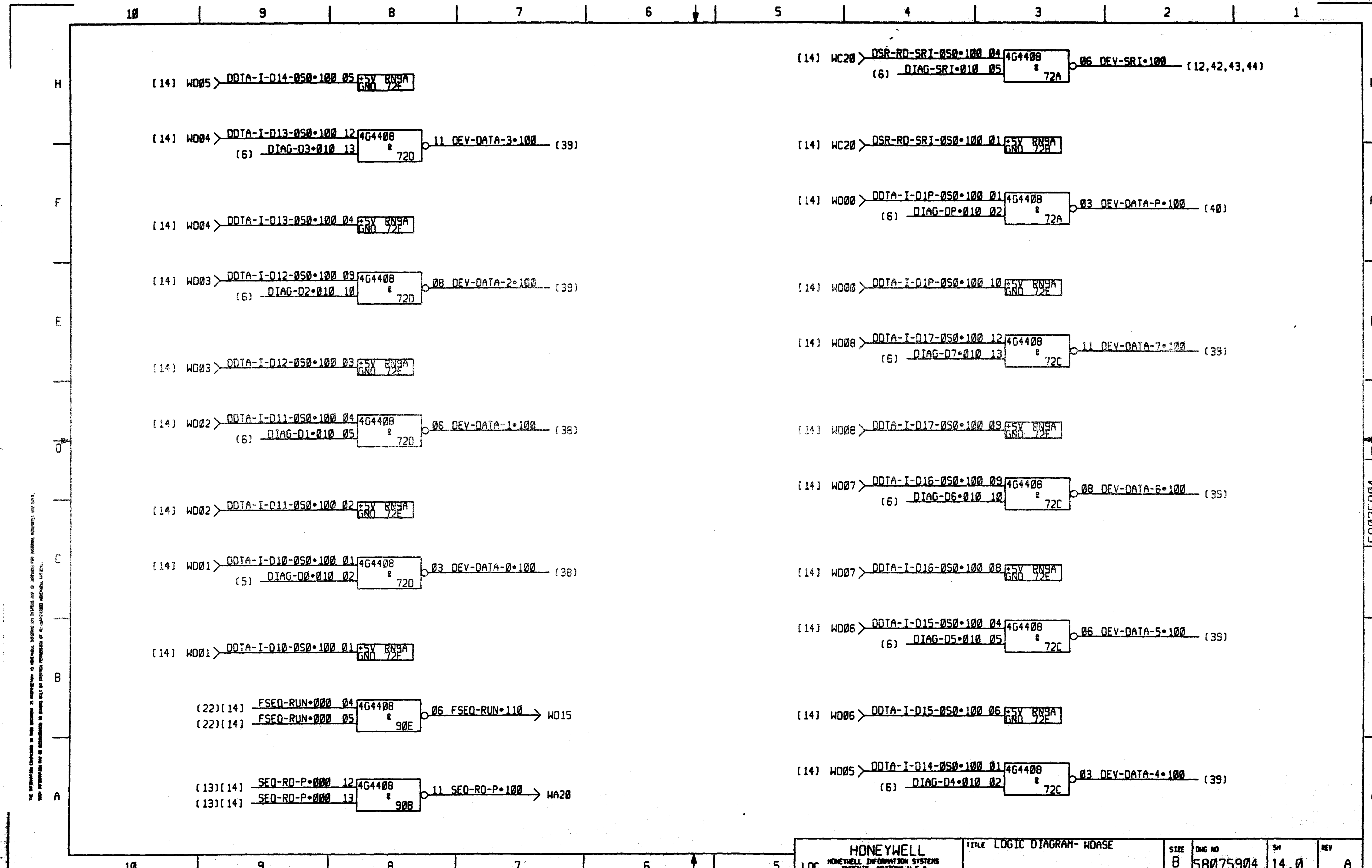
HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- WOASE
SIZE B | DWG NO 58075904 | SH 12.0 | REV A

58075904

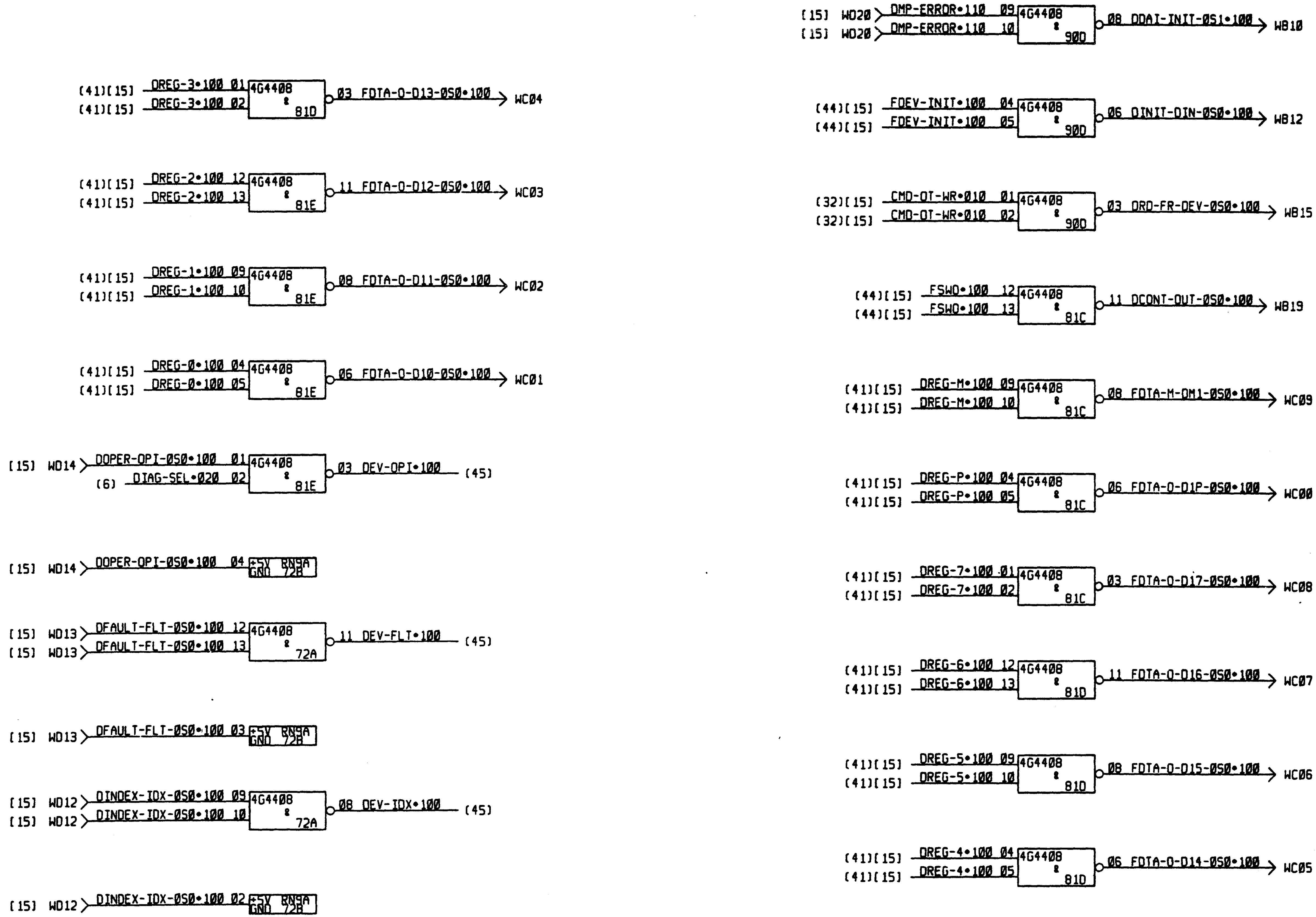


HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 13.0	REV A

LOC

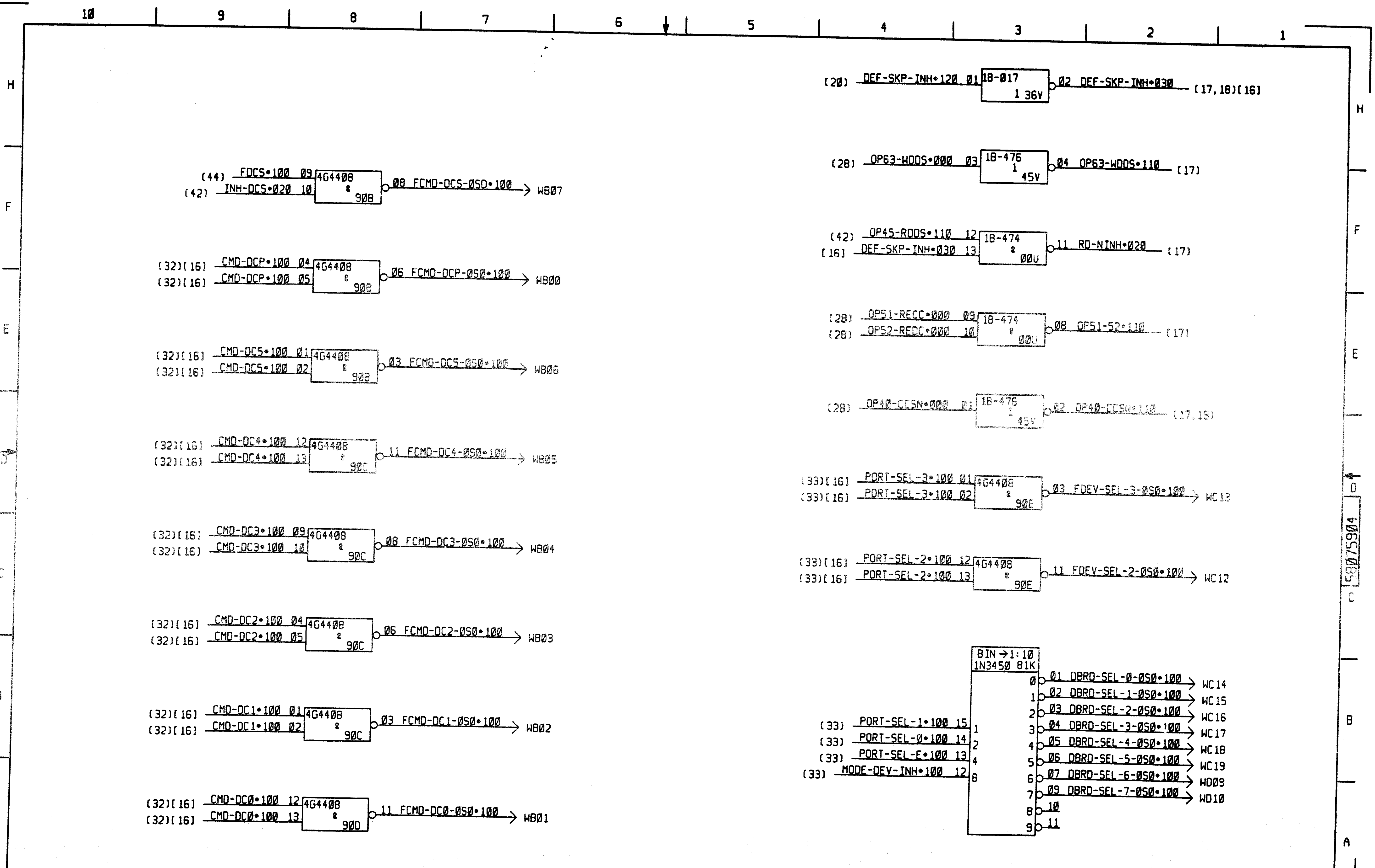


LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 14.0	REV A



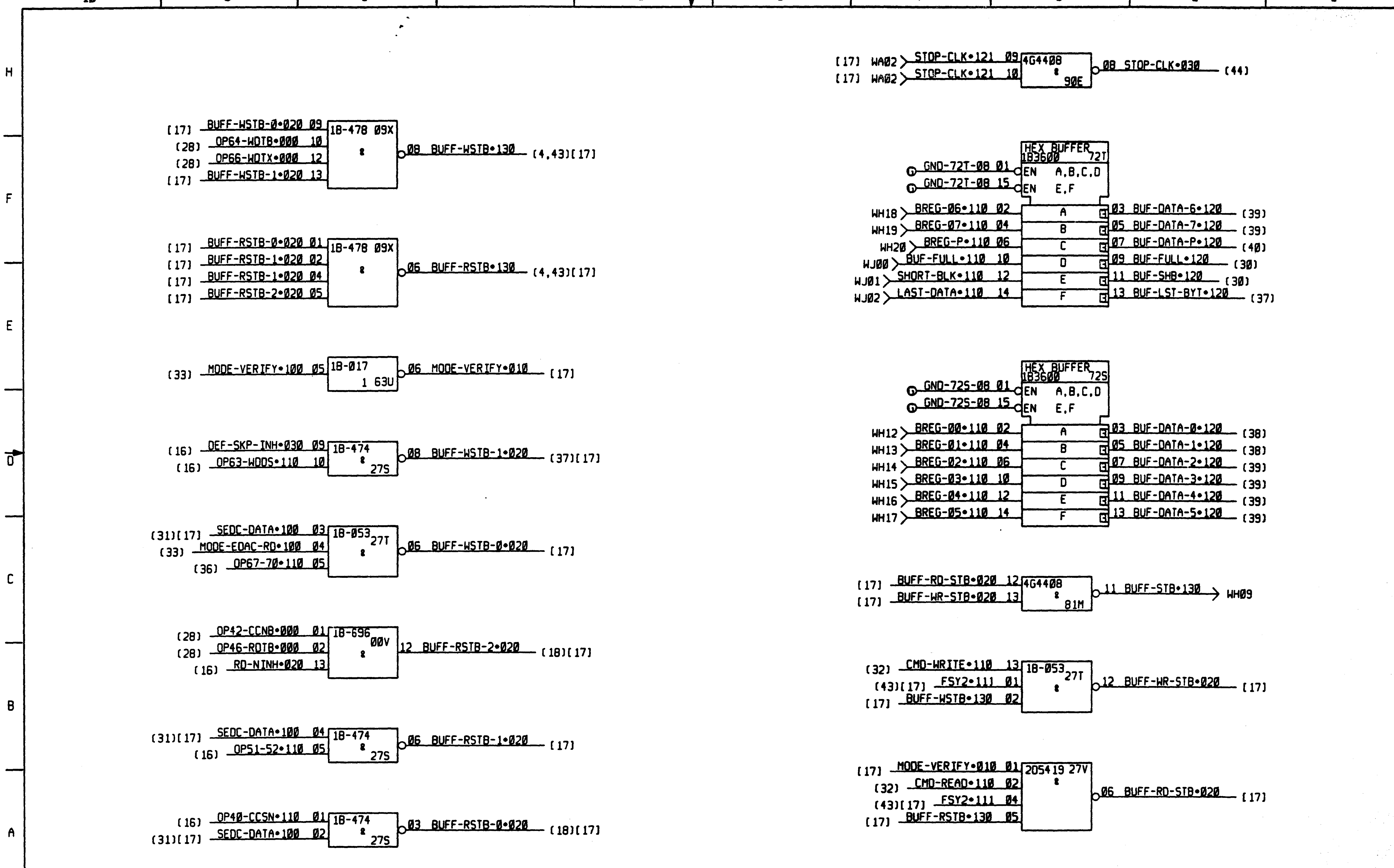
58075904

LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 15.0	REV A



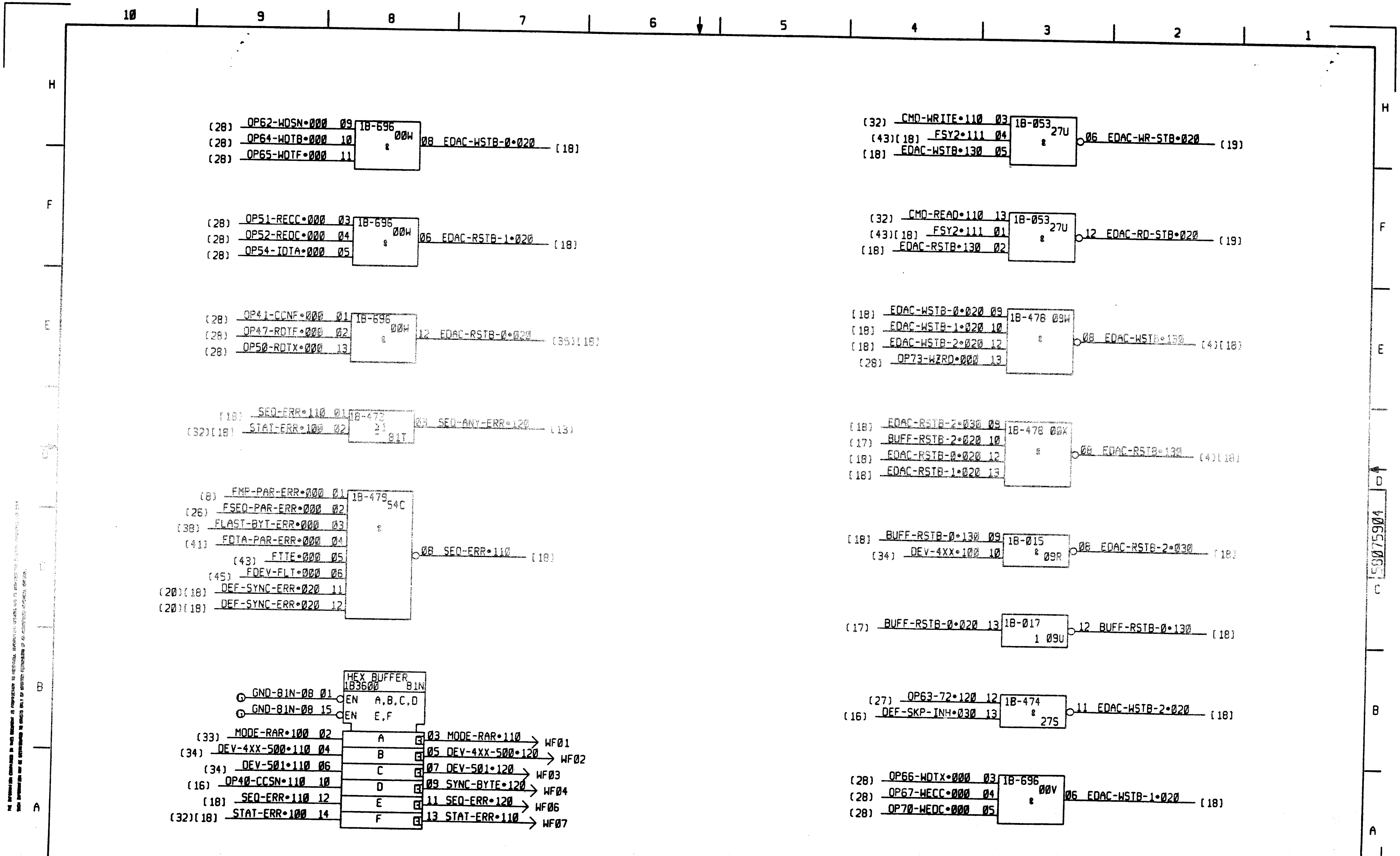
LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 16.0	REV A

58075904



HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

LOC | TITLE LOGIC DIAGRAM- WDASE | SIZE B | DWG NO 58Ø759Ø4 | SH 17.Ø | REV A



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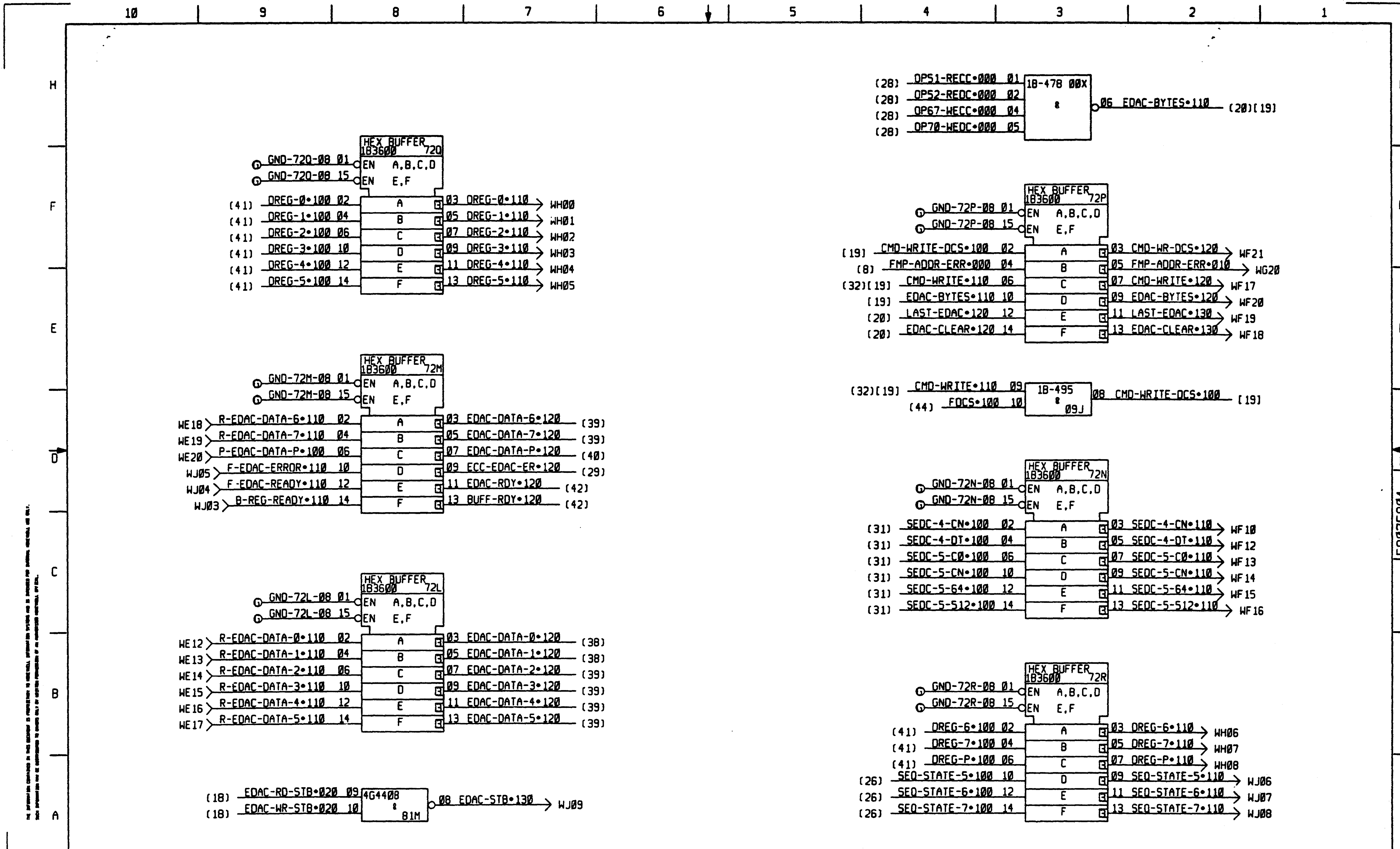
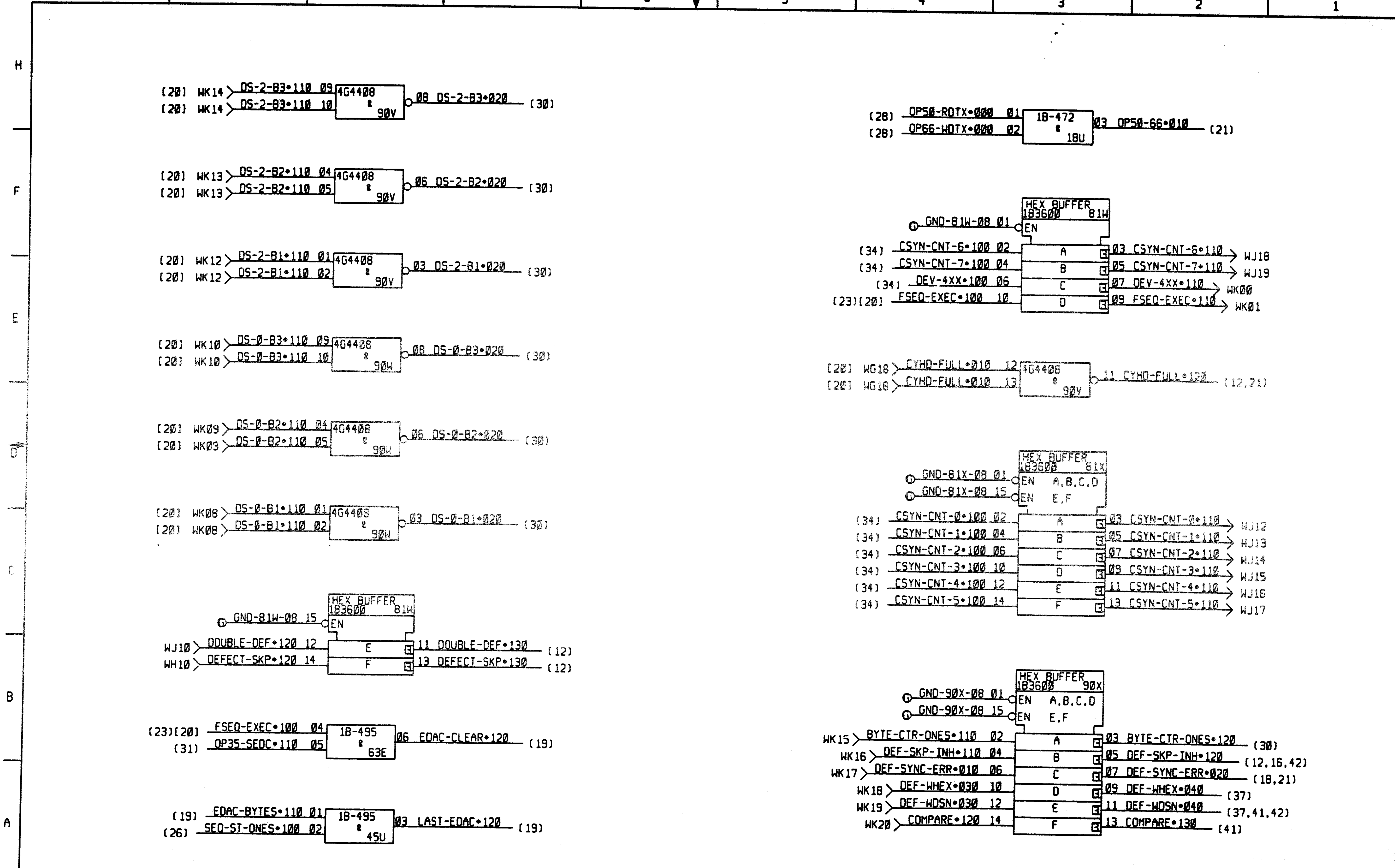


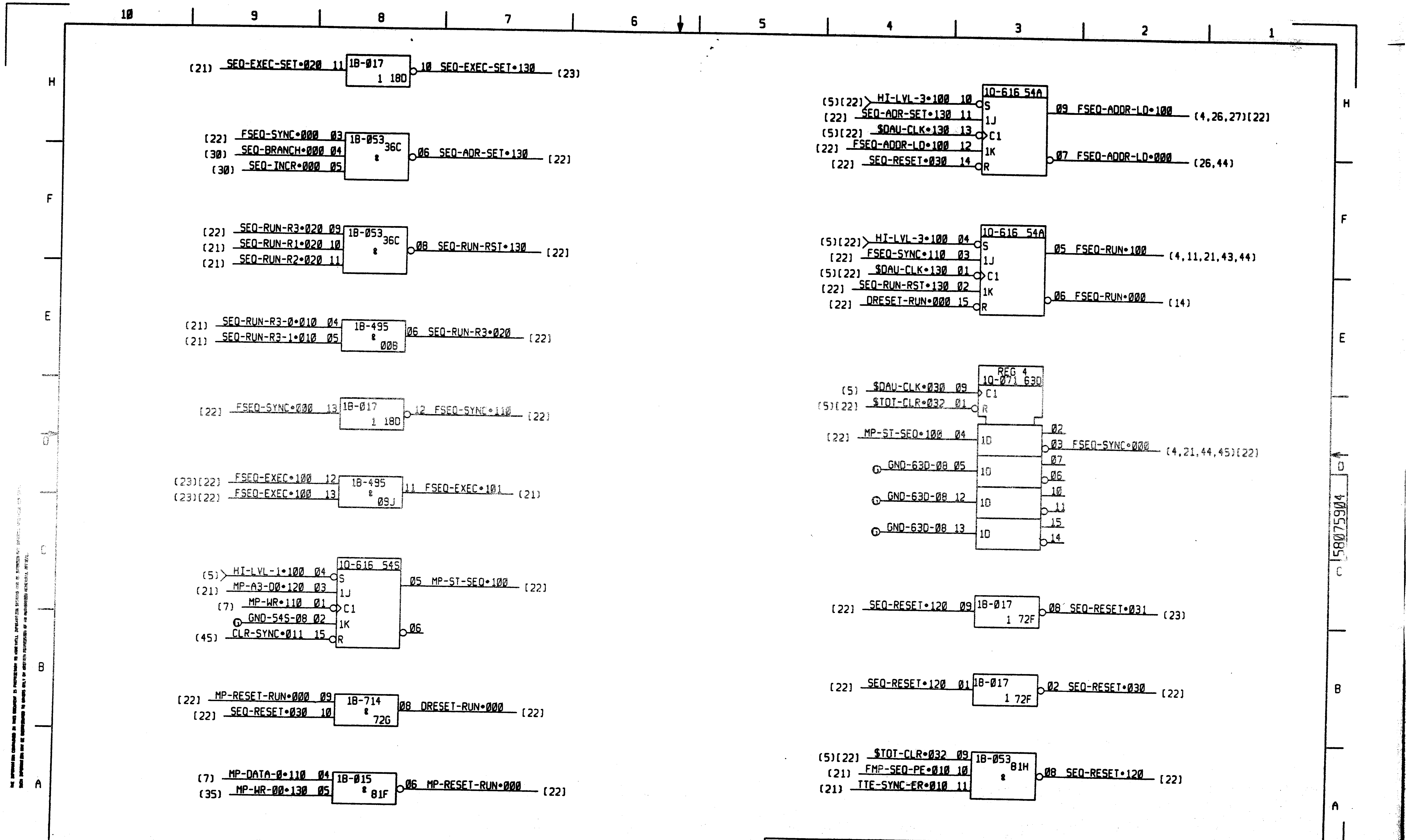
LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 19.0	REV A



HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- WDASE
SIZE B | DWG NO 58075904 | SH 20.0 | REV A

HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58Ø759Ø4	SH 21.Ø	REV A

58Ø759Ø4

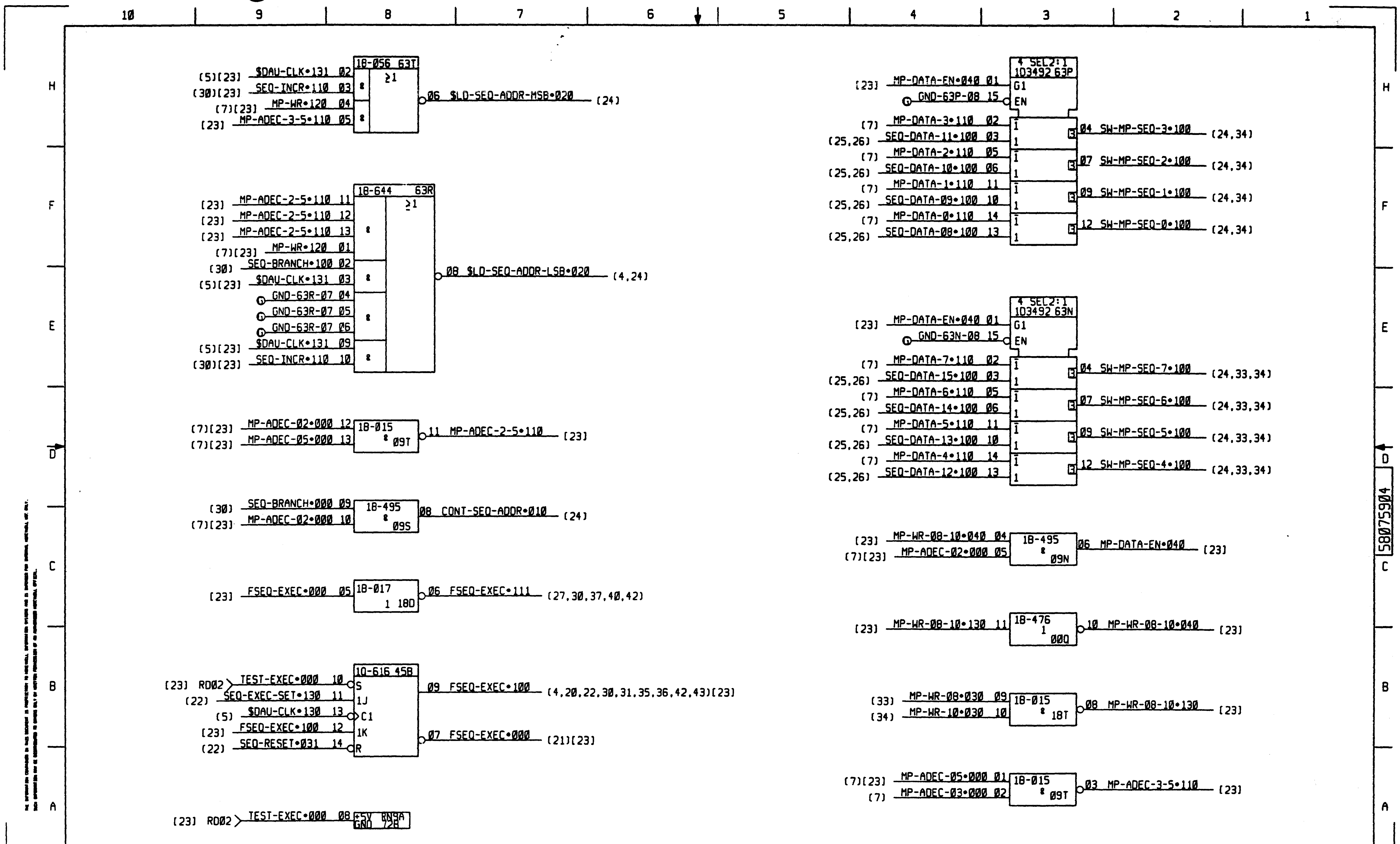


HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

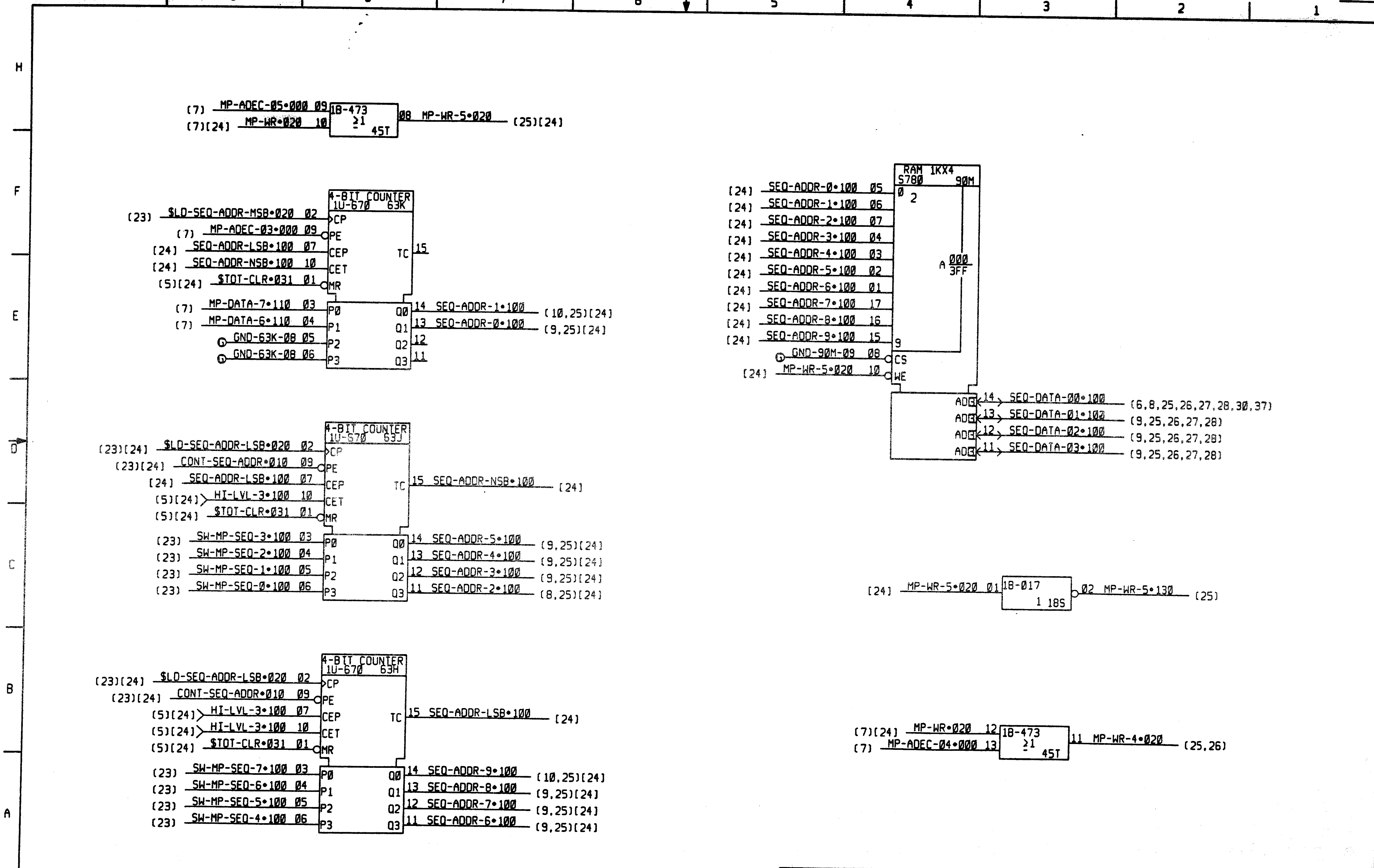
TITLE LOGIC DIAGRAM- WDASE

SIZE	DWG NO	SH	REV
B	58075904	22.0	A



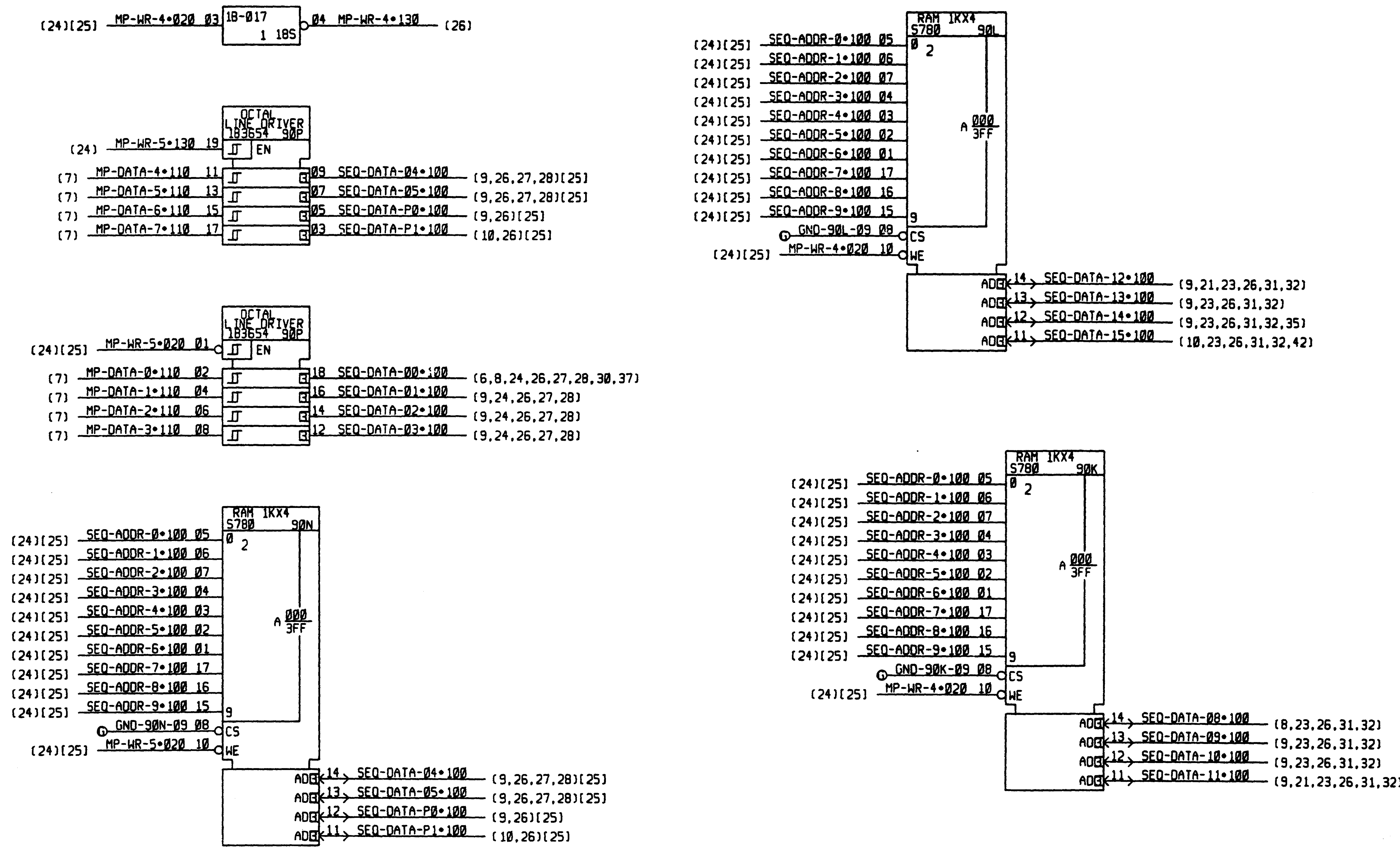
LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 23.0	REV A

58075904



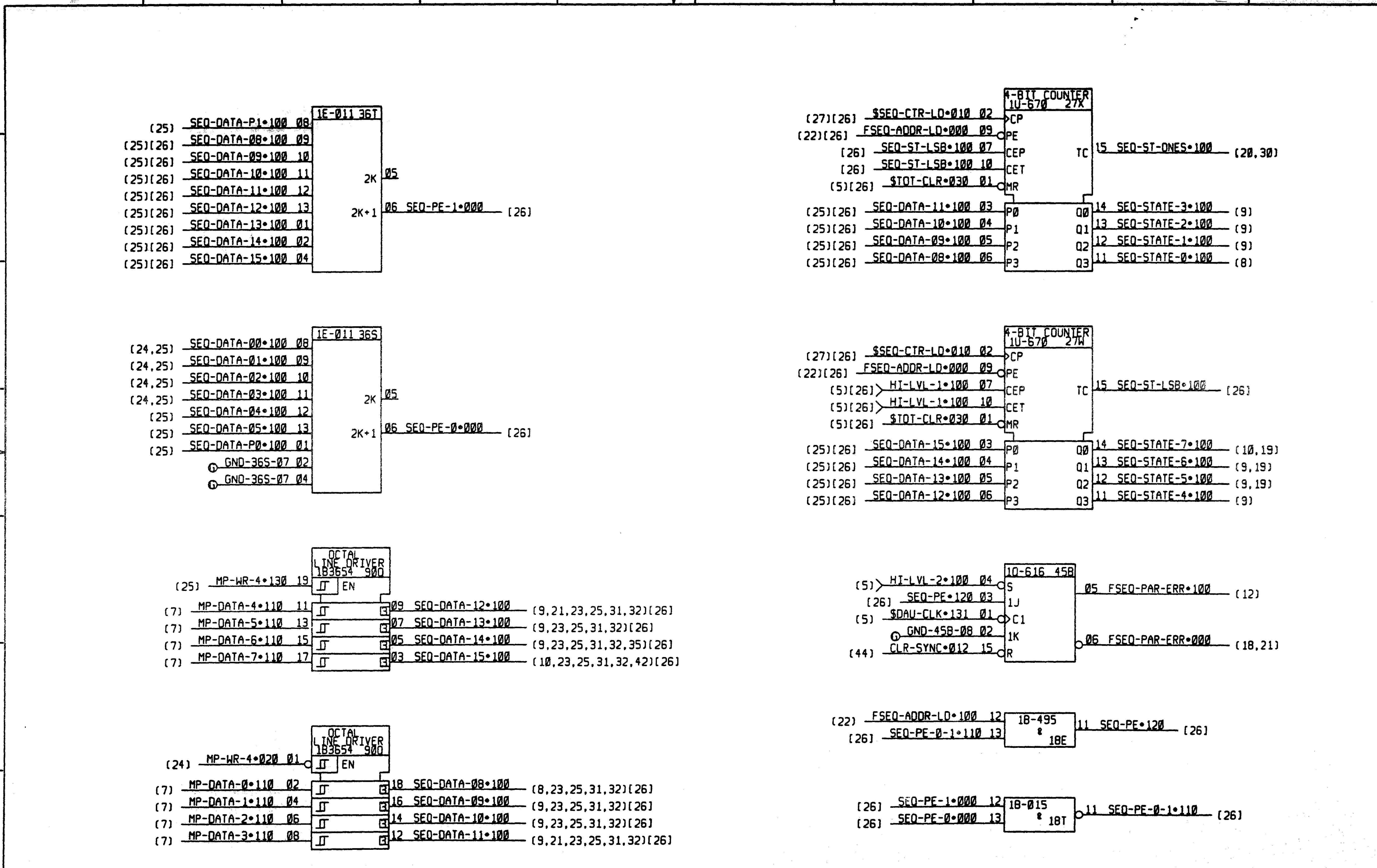
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC	TITLE	SIZE	DWG NO	SH	REV
	LOGIC DIAGRAM- WDASE	B	58075904	24.0	A



58075904

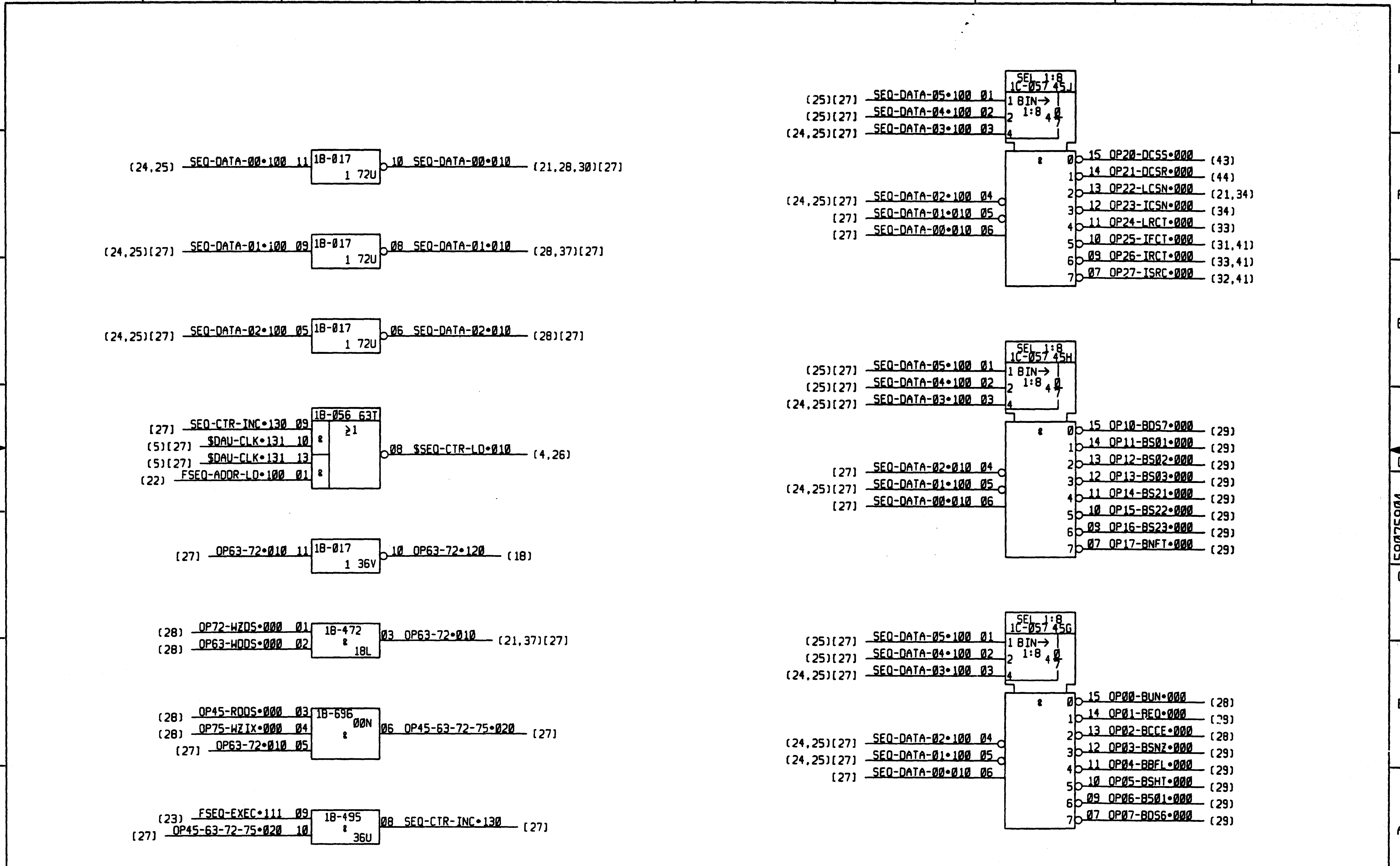
HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 25.0	REV A



HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC

TITLE LOGIC DIAGRAM- WDASE

SIZE	DWG NO	SH	REV
B	58Ø759Ø4	26.Ø	A

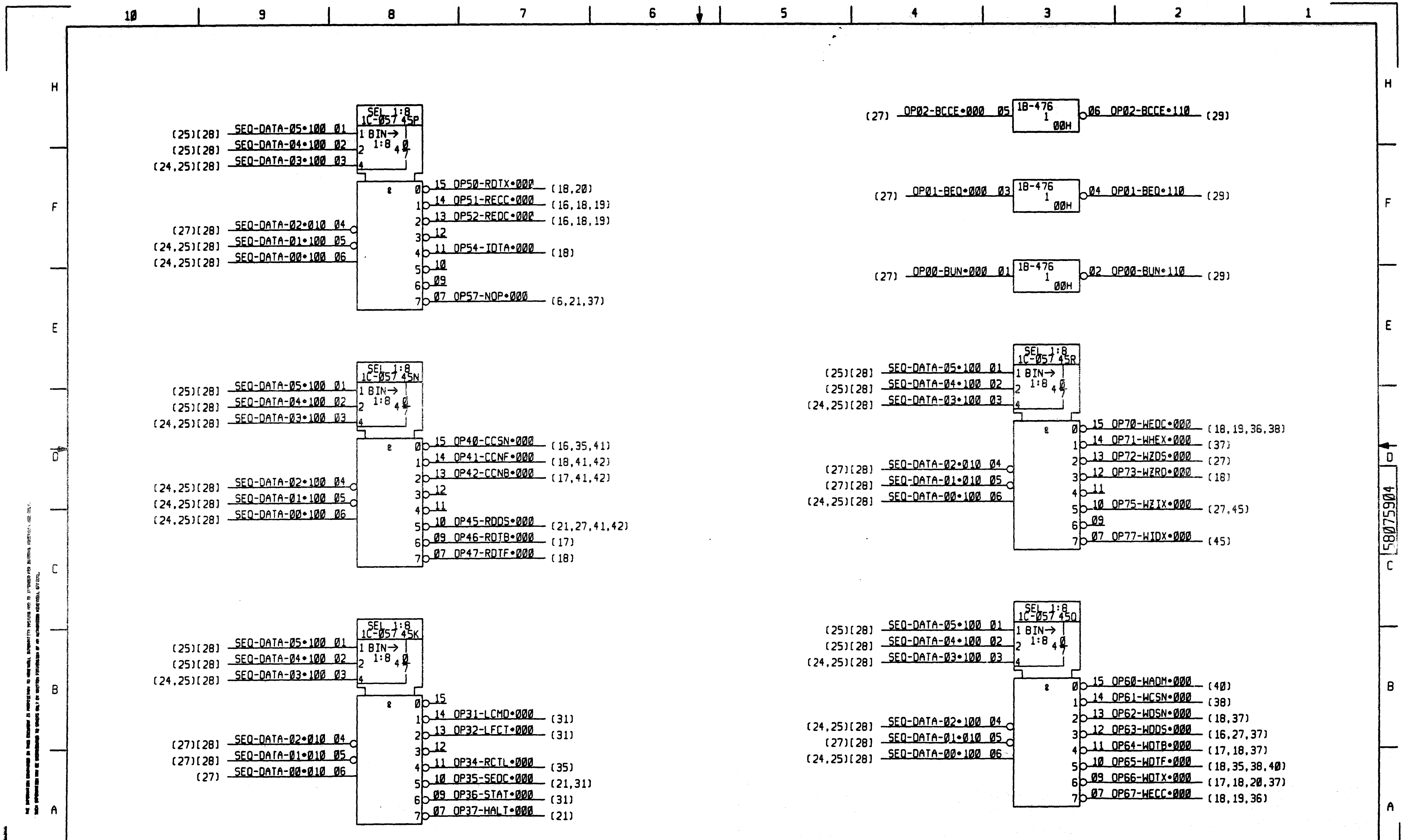


HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

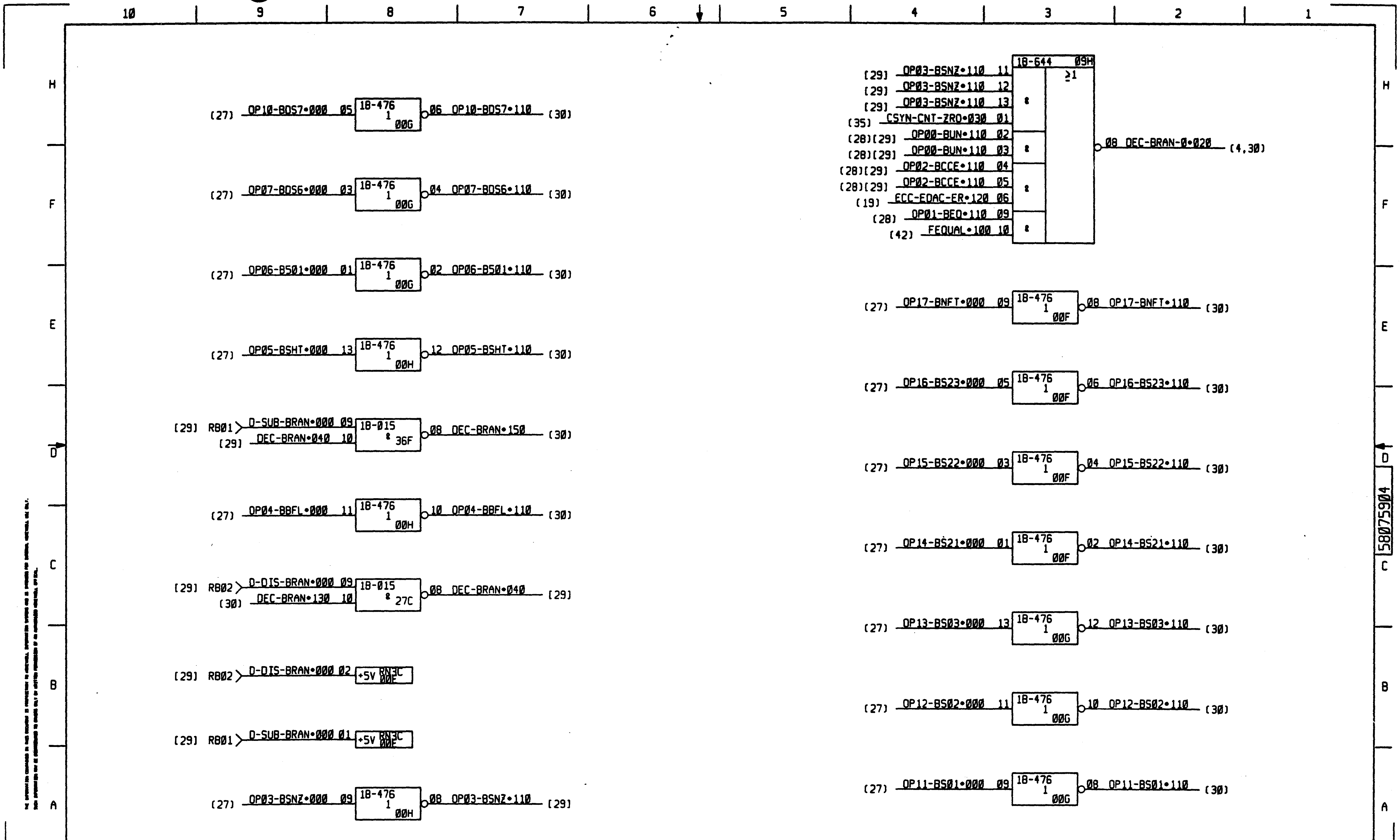
LOC

TITLE LOGIC DIAGRAM- WDASE

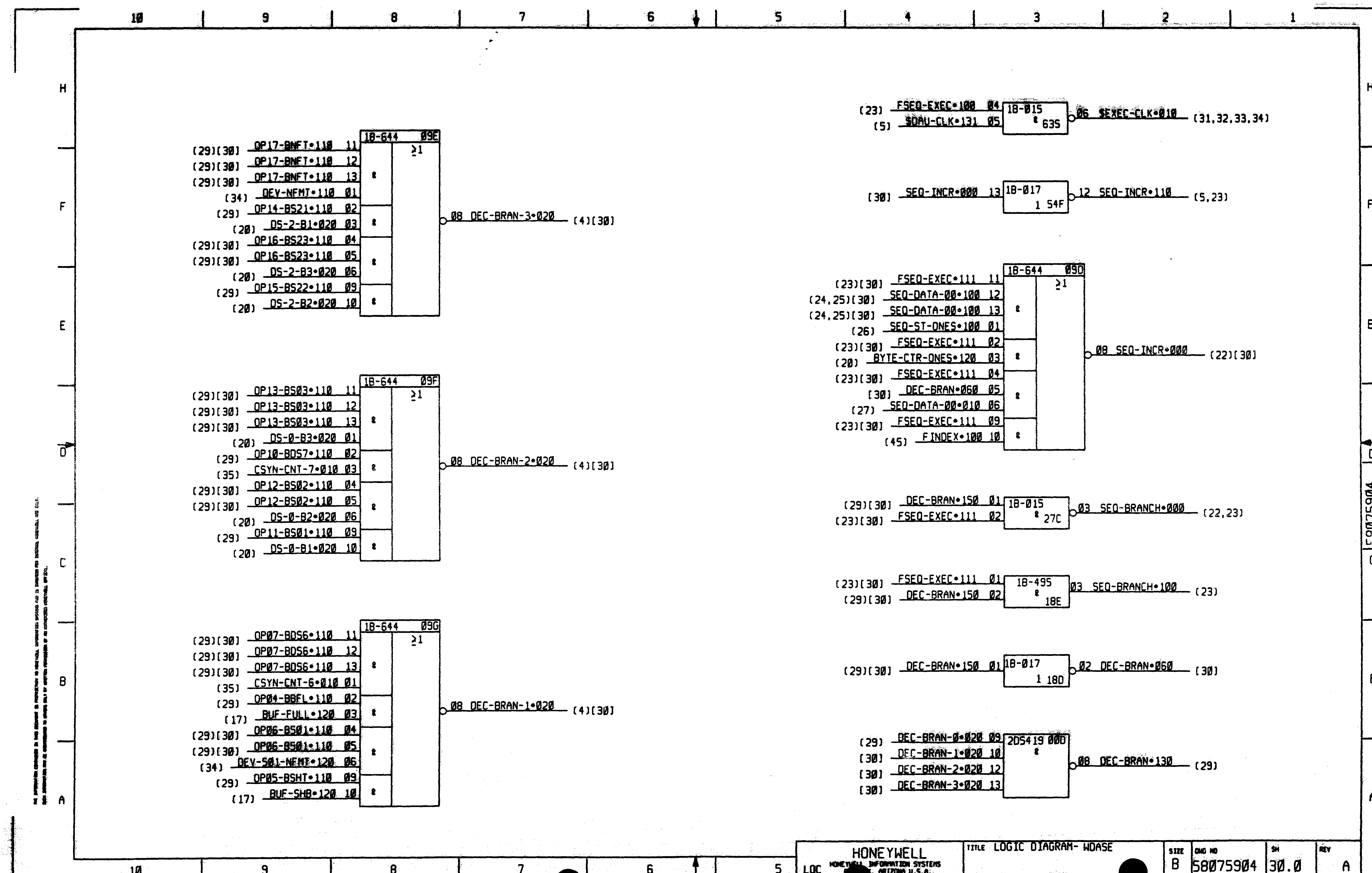
SIZE	DWG NO	SH	REV
B	58075904	27.0	A



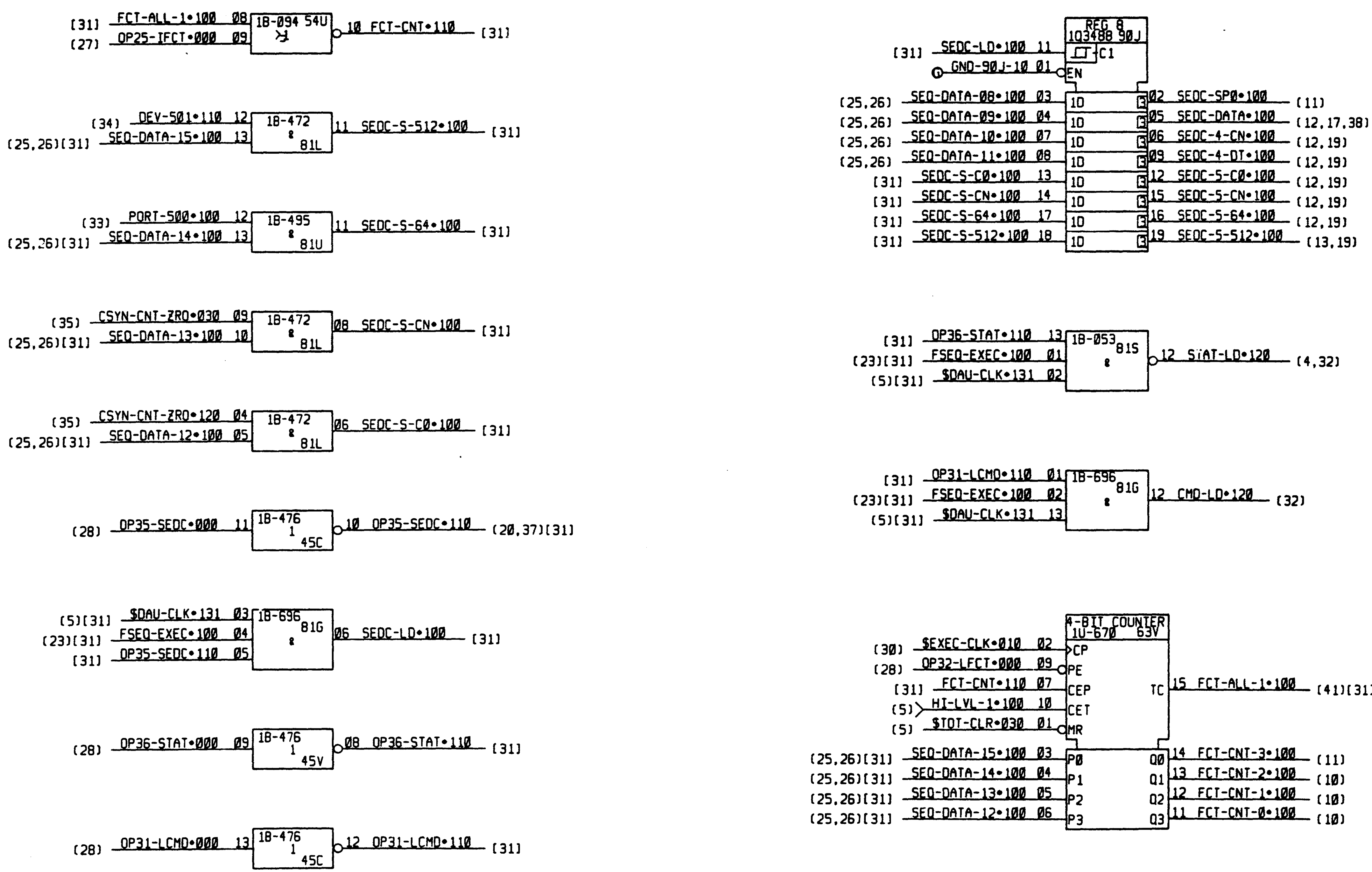
HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 28.0	REV A



LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 29.0	REV A

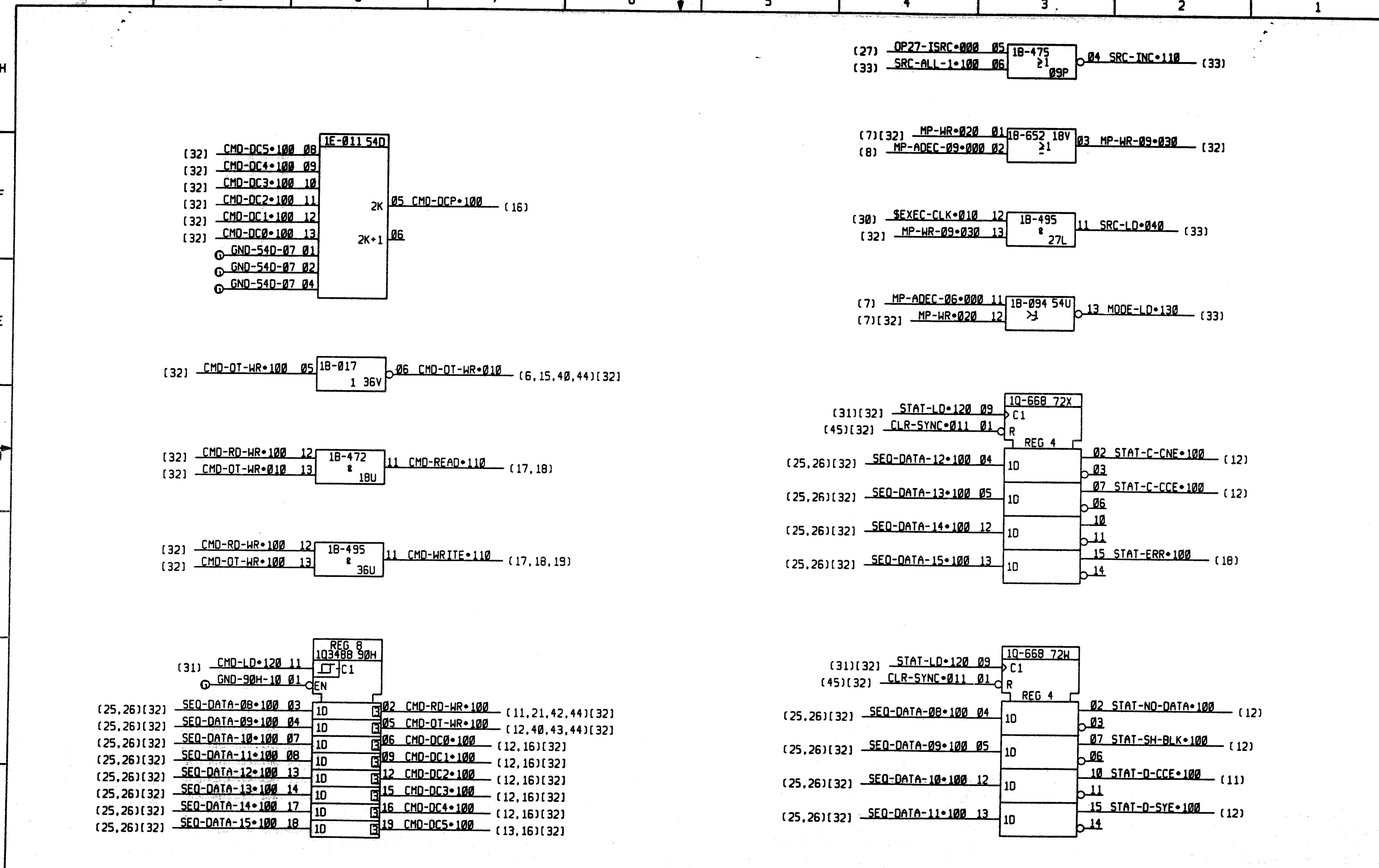


1B-644 09E
OP17-BNFT•110
DEV-NFMT•110
OP14-BS21•110
DS-2-B1•020
OP16-BS23•110
DS-2-B3•020
OP15-BS22•110
DS-2-B2•020
08 DEC-BRAN-3•020
1B-644 09F
OP13-BS03•110
DS-0-B3•020
OP10-BDS7•110
CSYN-CNT-7•010
OP12-BS02•110
DS-0-B2•020
OP11-BS01•110
DS-0-B1•020
08 DEC-BRAN-2•020
1B-644 09G
OP07-BDS6•110
CSYN-CNT-6•010
OP04-BBFL•110
BUF-FULL•120
OP06-BS01•110
DEV-S01-NFMT•120
OP05-BSHT•110
BUF-SHB•120
08 DEC-BRAN-1•020
FSEQ-EXEC•100
$DAU-CLK•131
1B-015 63S
06 $EXEC-CLK•010
SEQ-INCR•000
1B-017 54F
12 SEQ-INCR•110
1B-644 09D
FSEQ-EXEC•111
SEQ-DATA-00•100
SEQ-ST-ONES•100
BYTE-CTR-ONES•120
DEC-BRAN•060
SEQ-DATA-00•010
F INDEX•100
08 SEQ-INCR•000
DEC-BRAN•150
1B-015 27C
03 SEQ-BRANCH•000
1B-495 18E
03 SEQ-BRANCH•100
1B-017 18D
02 DEC-BRAN•060
DEC-BRAN-0•020
DEC-BRAN-1•020
DEC-BRAN-2•020
DEC-BRAN-3•020
2D5419 00D
08 DEC-BRAN•130
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- WDASE
SIZE B
DWG NO 58075904
SH 30.0
REV A



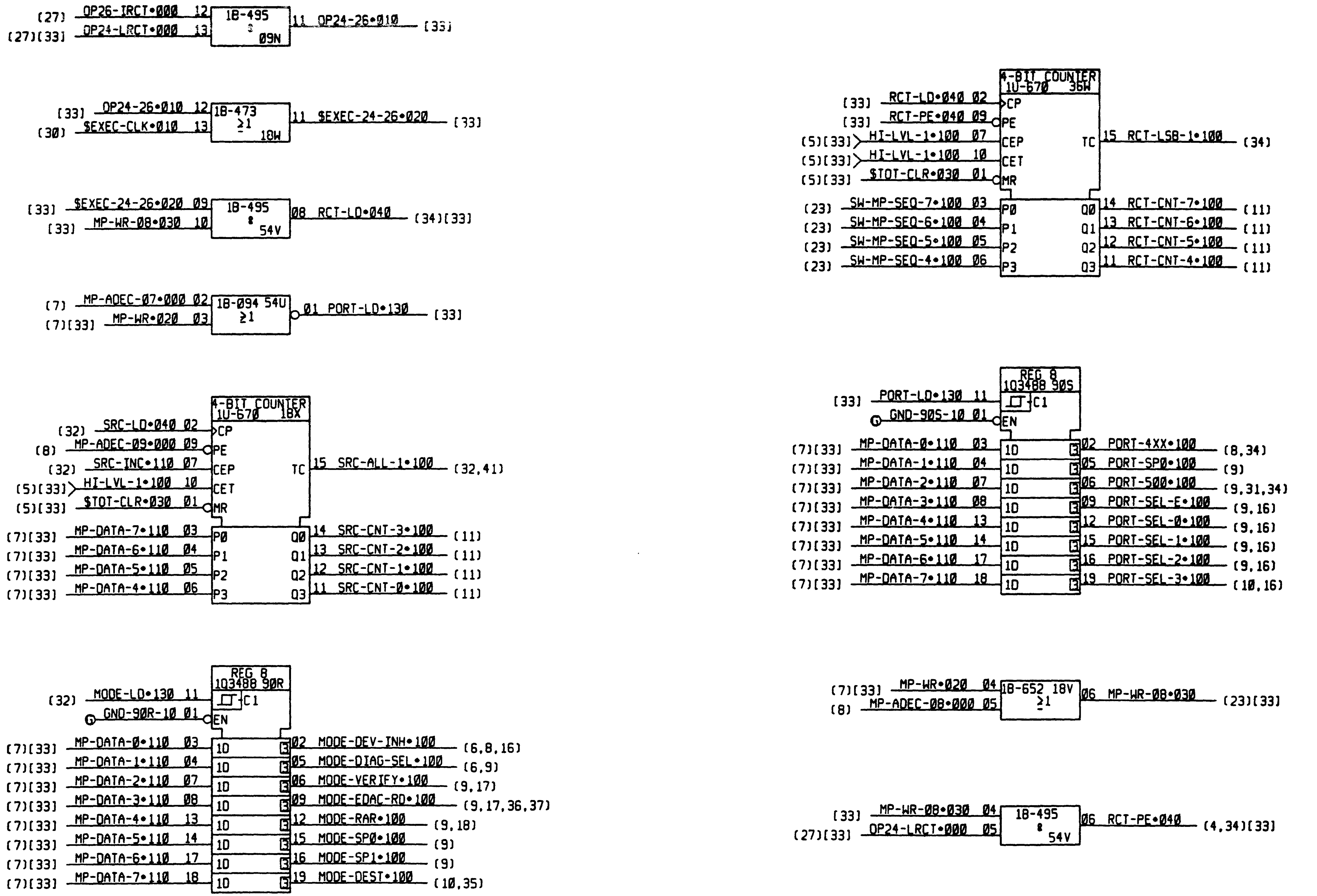
58075904

HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A. LOC	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 31.0	REV A



58075904

LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 32.0	REV A

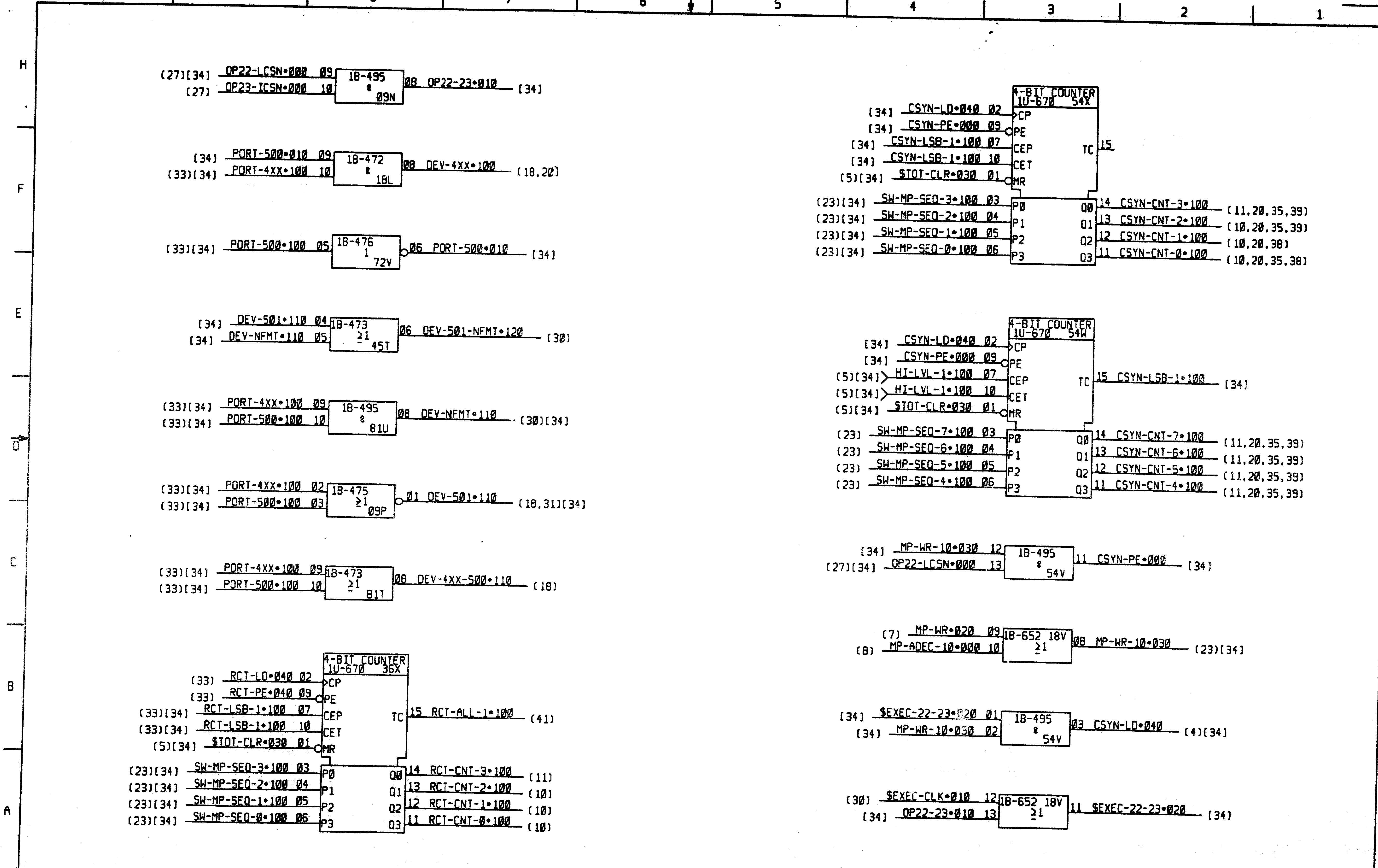


HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDASE

SIZE	DWG NO	SH	REV
B	58075904	33.0	A

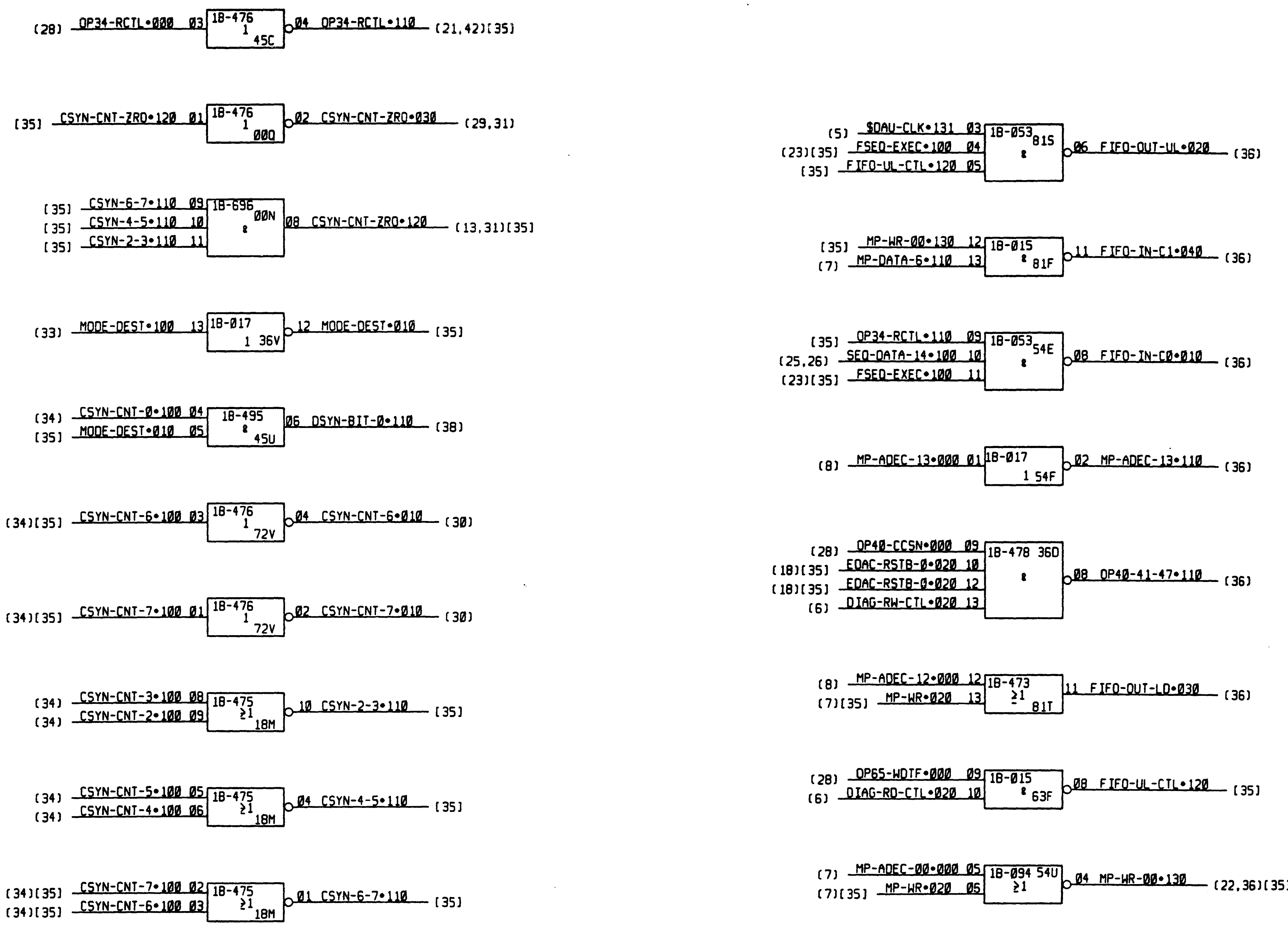
58075904



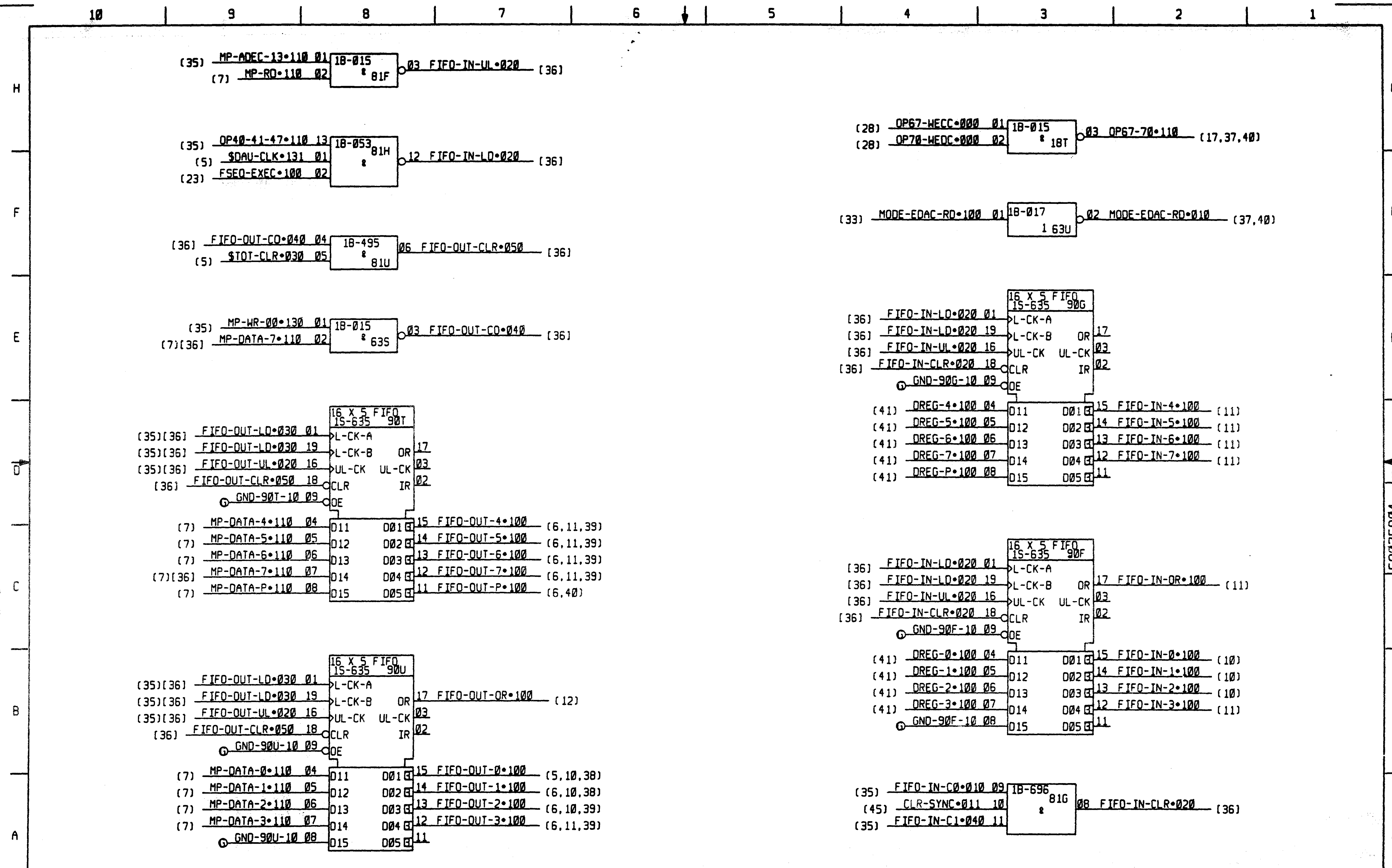
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

LOC	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 34.0	REV A

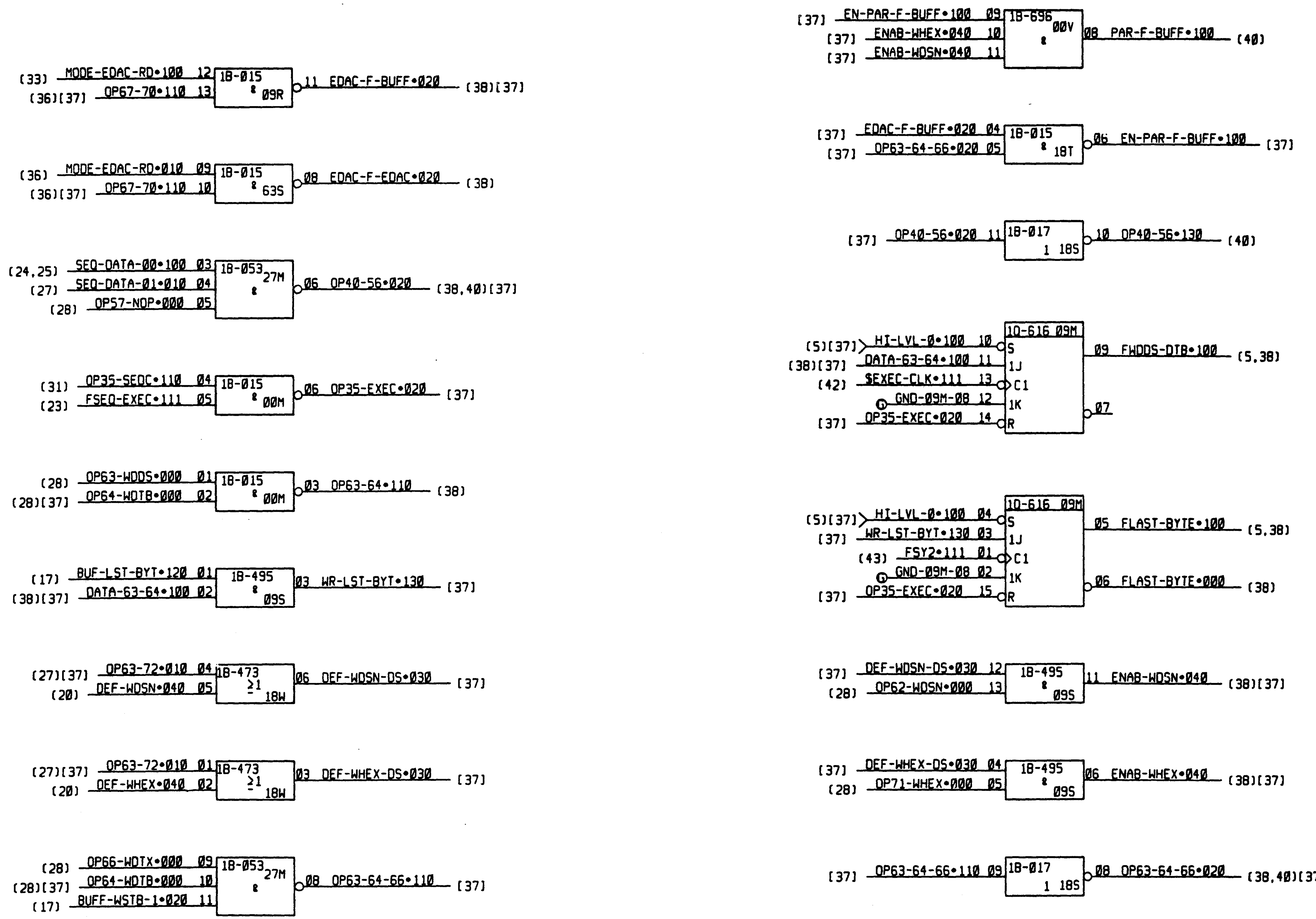
58075904



LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 35.0	REV A



LOC HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 36.0	REV A

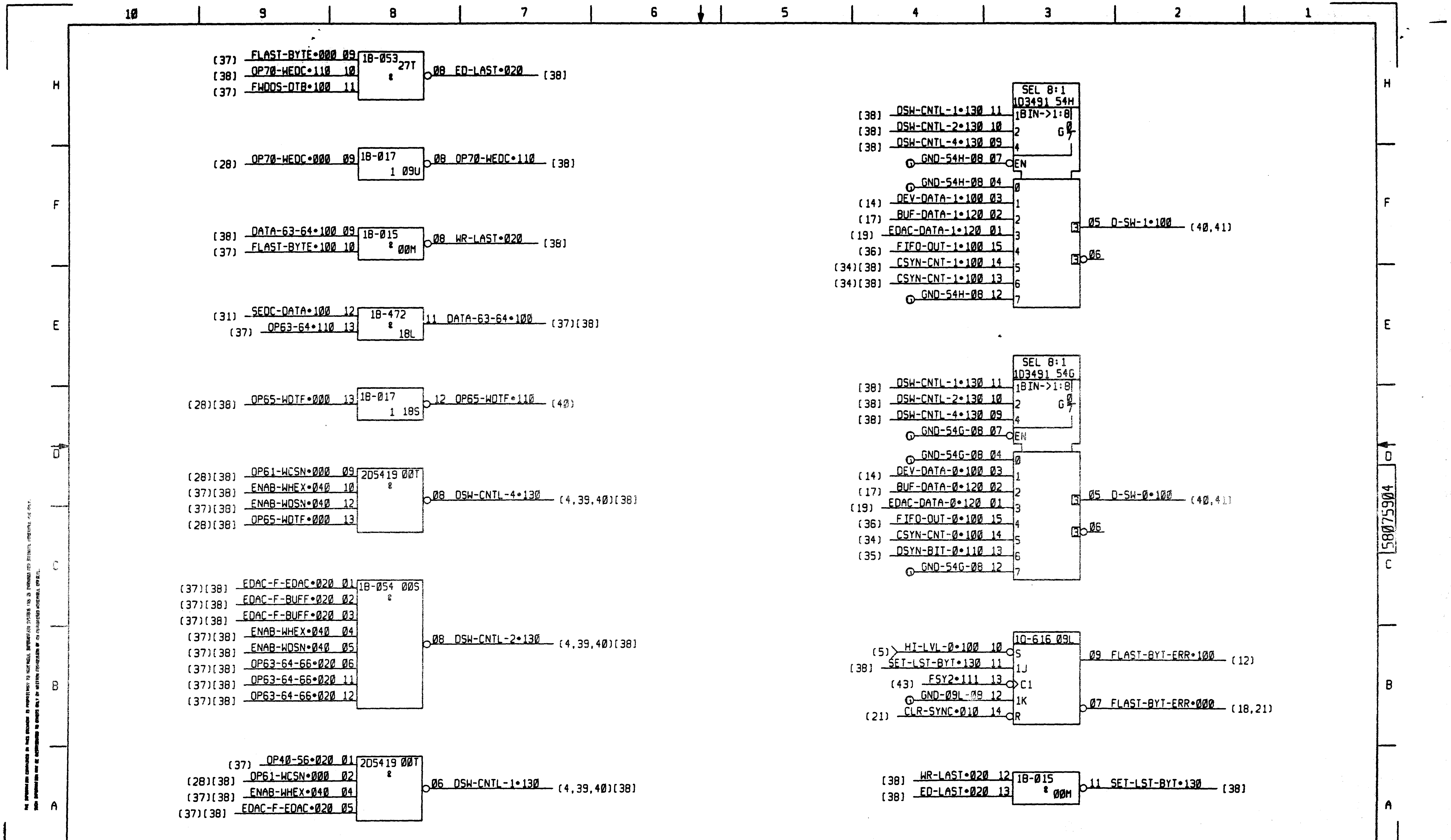


HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

TITLE LOGIC DIAGRAM- WDASE

SIZE	DWG NO	SH	REV
B	58Ø759Ø4	37.Ø	A

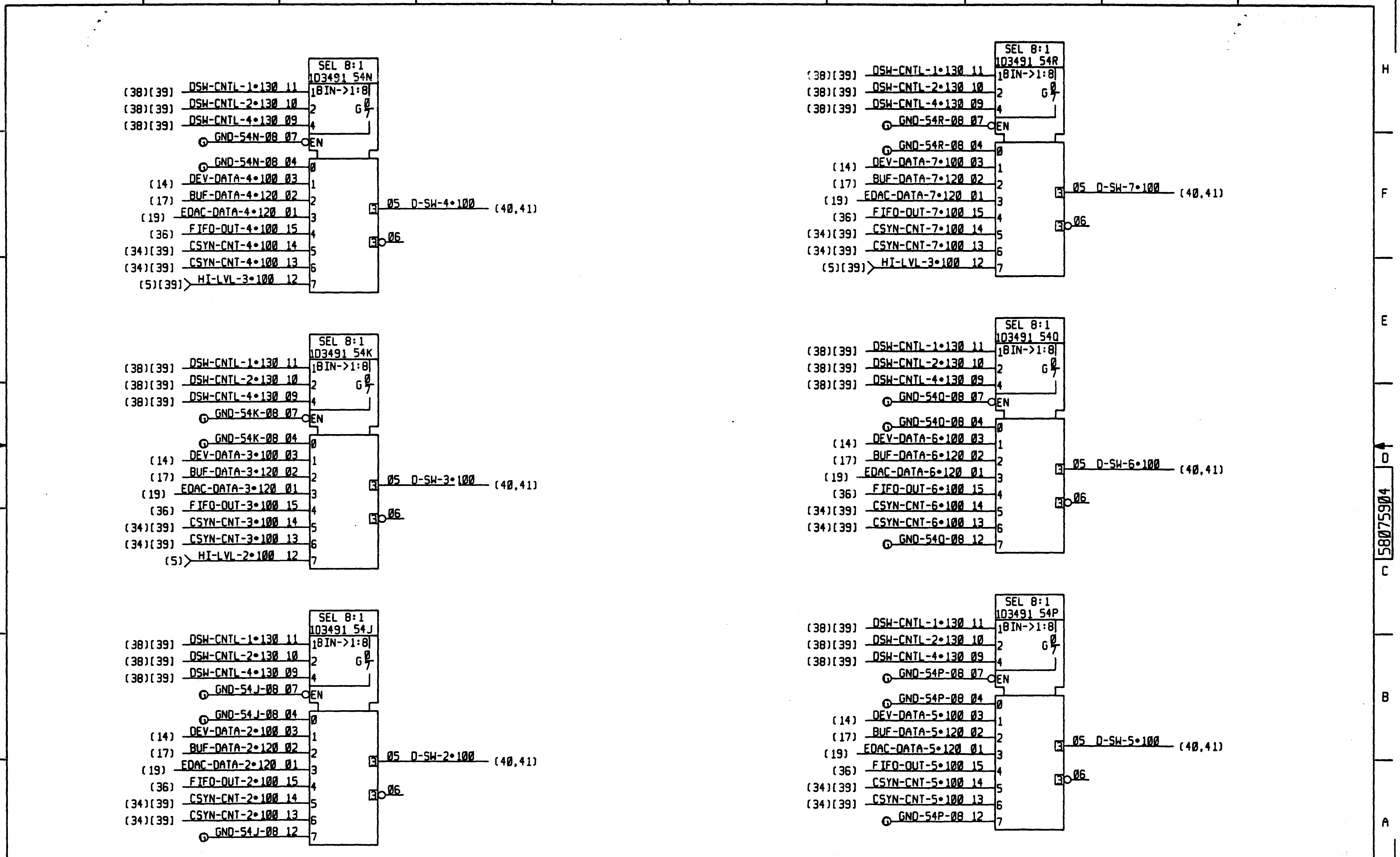


HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

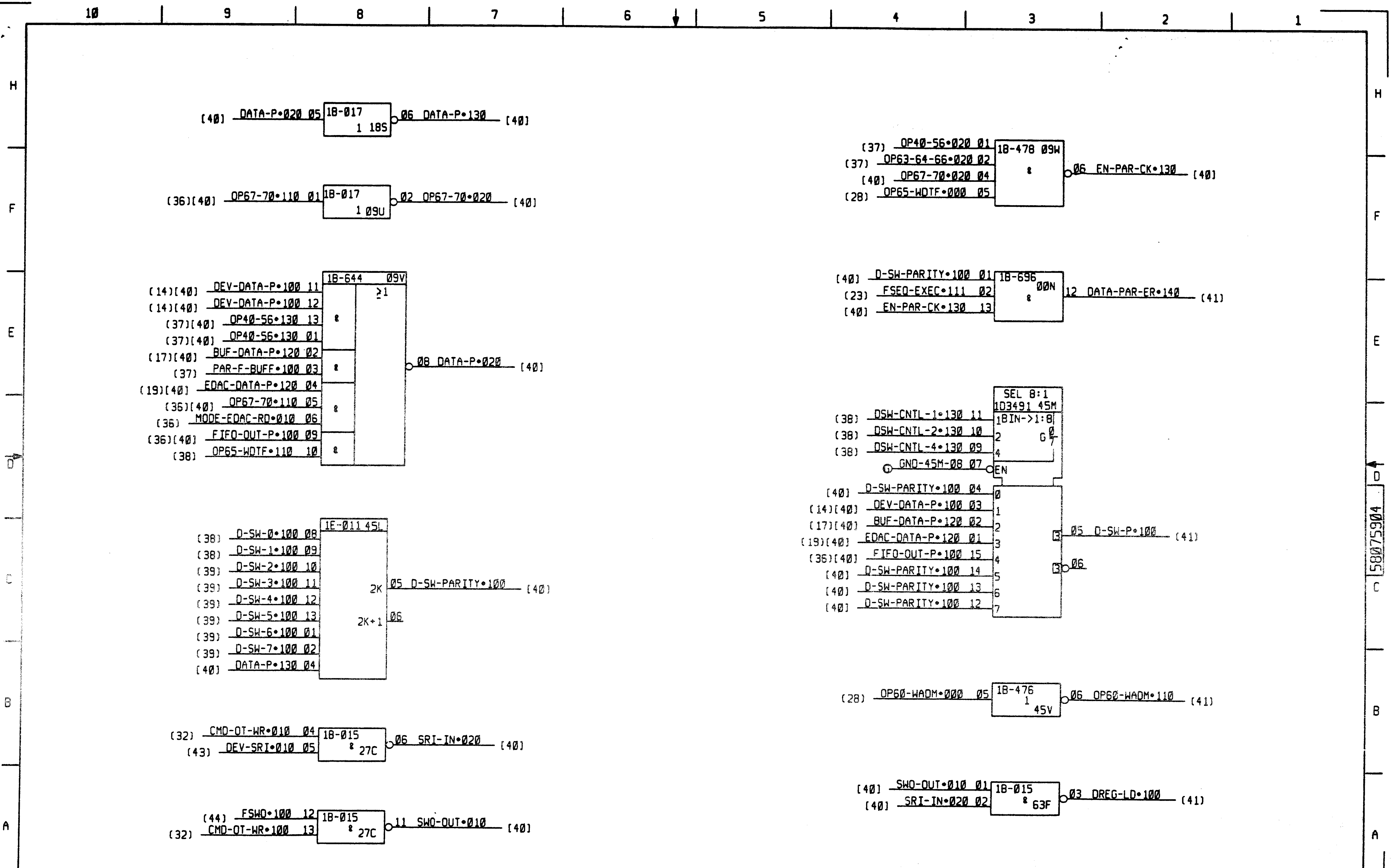
LOC

TITLE LOGIC DIAGRAM- WDASE

SIZE	DWG NO	SH	REV
B	58075904	38.0	A

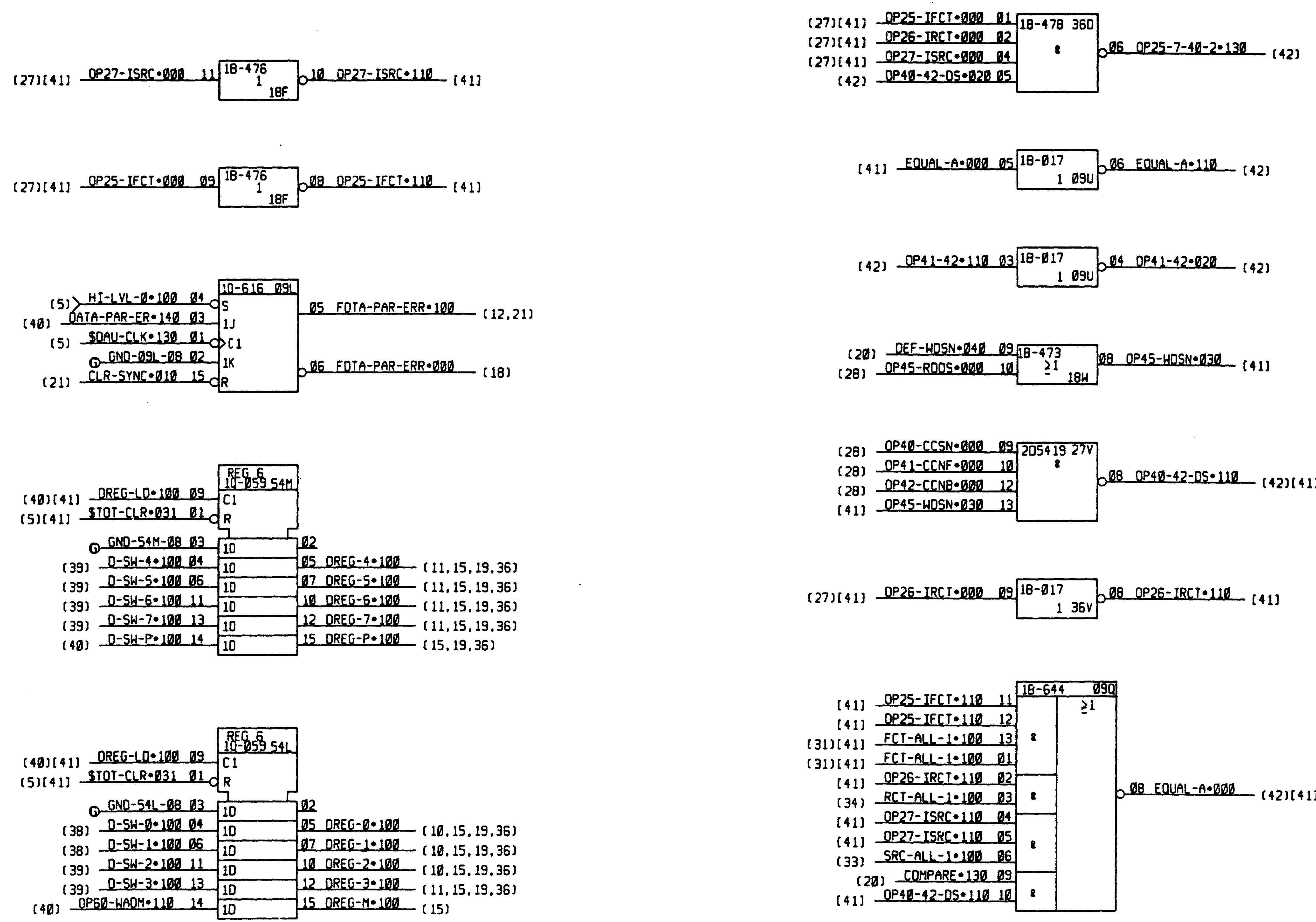


LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 39.0	REV A



HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

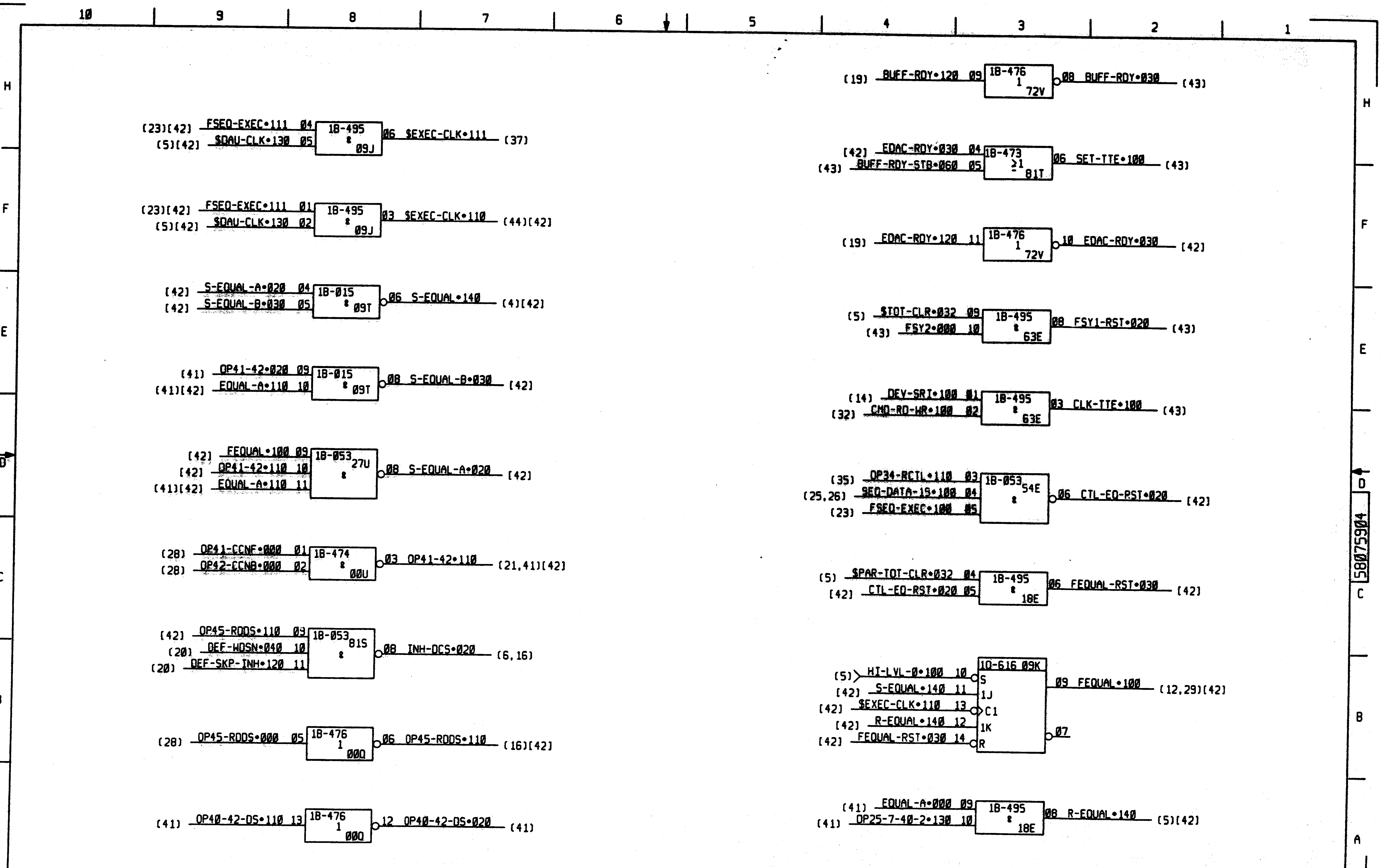
LOC	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 40.0	REV A



HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDASE

LOC	SIZE	DWG NO	SH	REV
	B	58075904	41.0	A



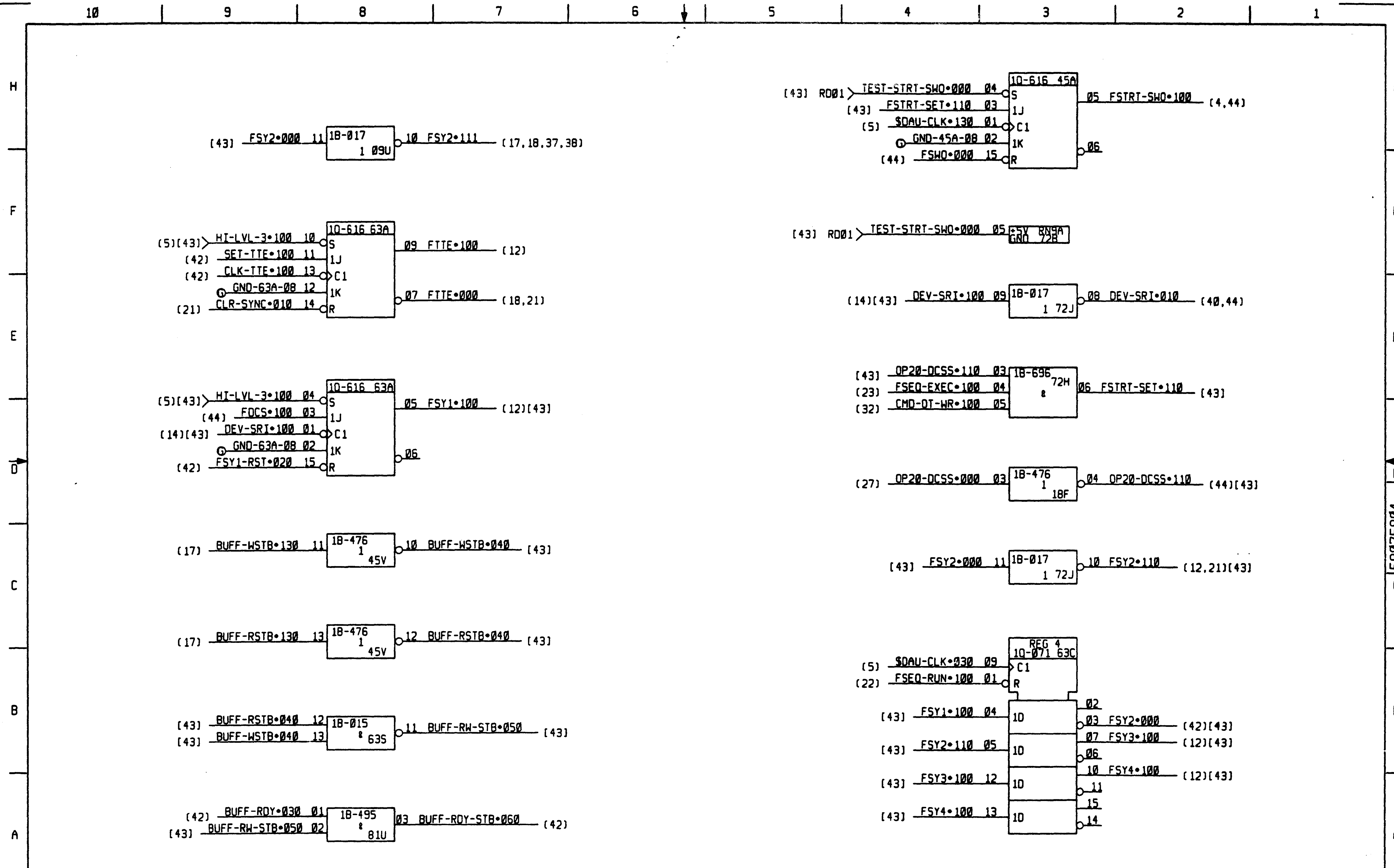
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

LOC

TITLE LOGIC DIAGRAM- WDASE

SIZE	DWG NO	SH	REV
B	58075904	42.0	A

58075904

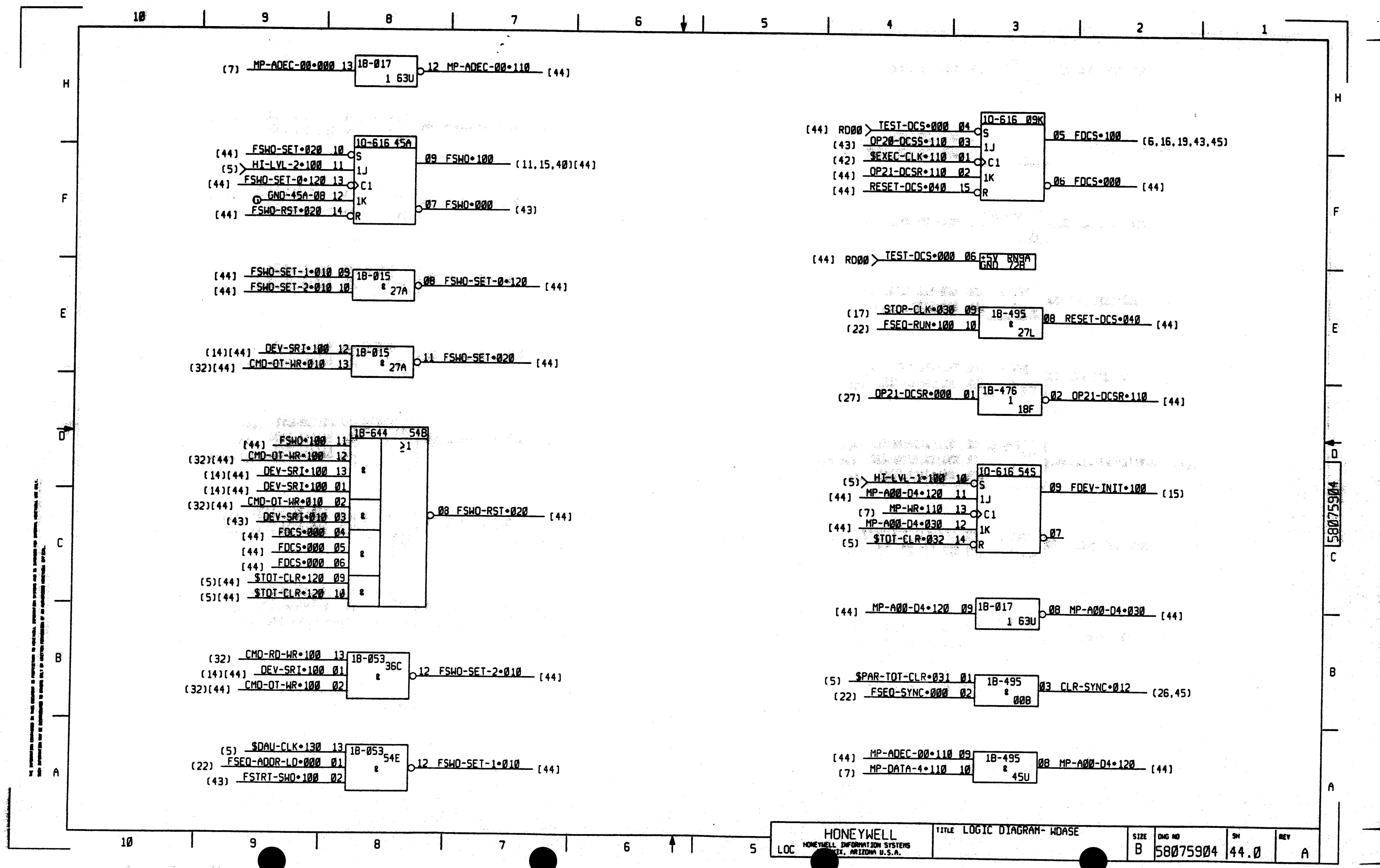


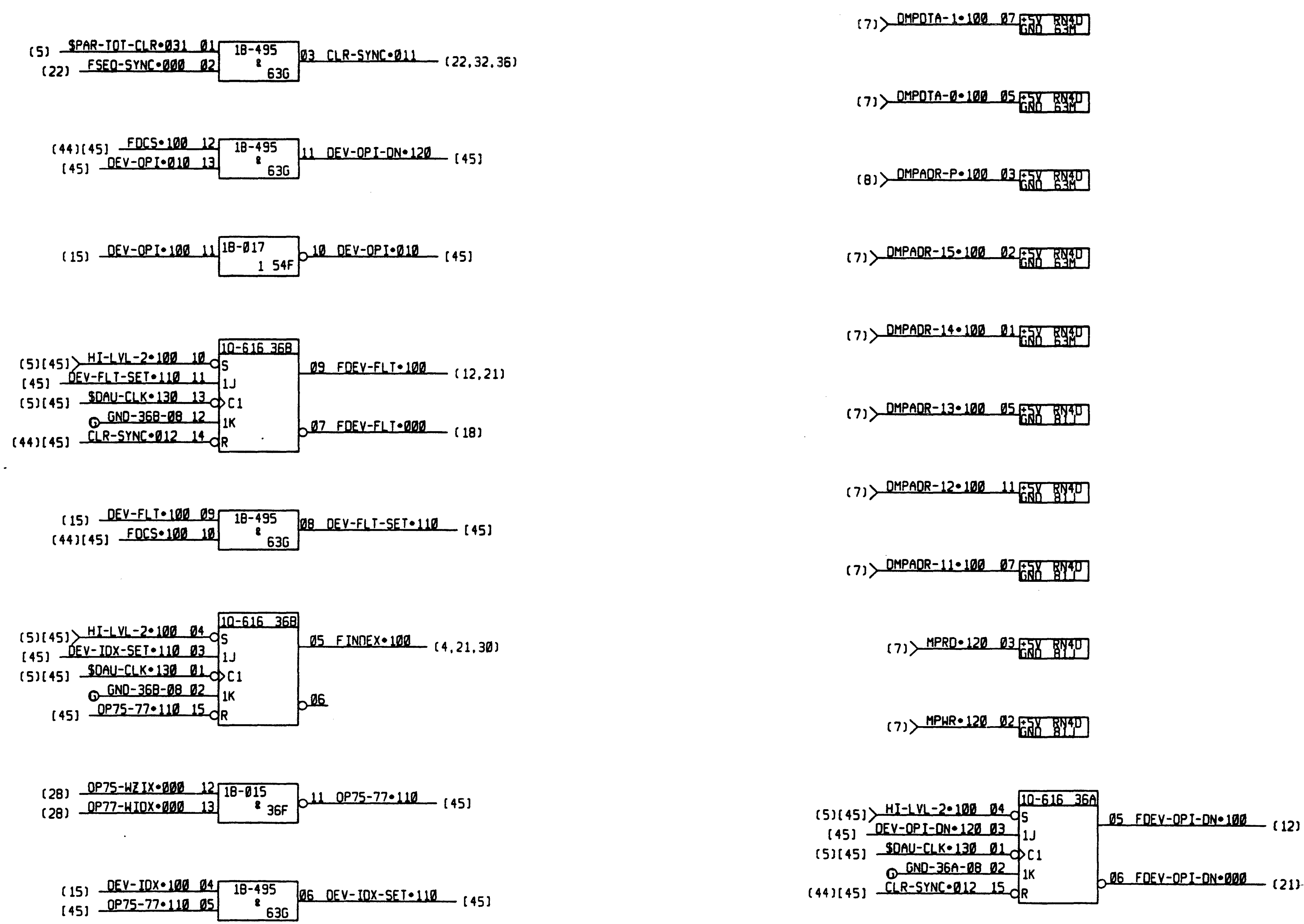
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.

LOC

TITLE LOGIC DIAGRAM- WDASE

SIZE	DWG NO	SH	REV
B	58075904	43.0	A

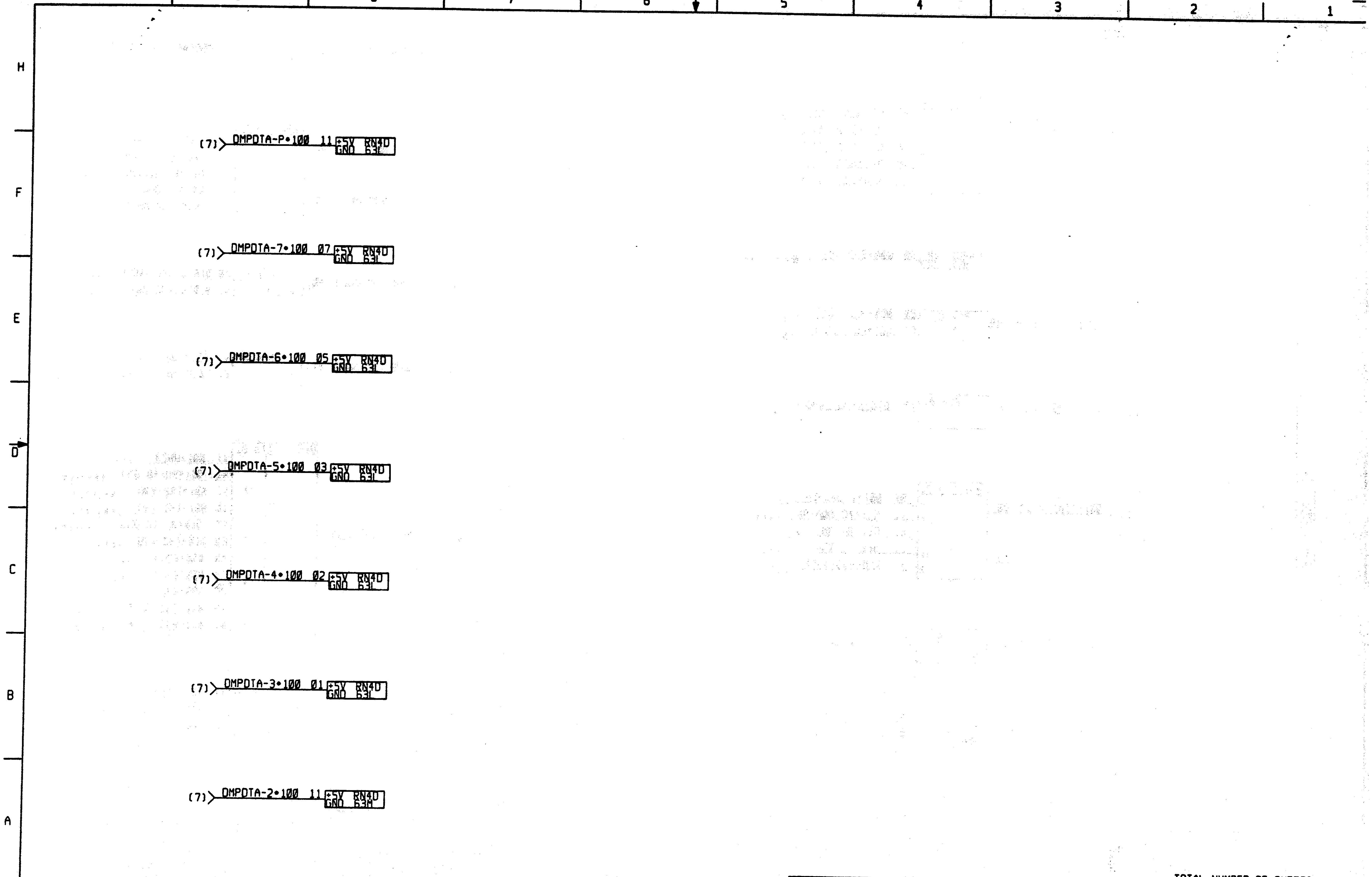

HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- WDASE
SIZE B
DWG NO 58075904
SH 44.0
REV A
58075904



LOC HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- WDASE

SIZE	DWG NO	SH	REV
B	58075904	45.0	A



TOTAL NUMBER OF SHEETS = 49

LOC	HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- WDASE	SIZE B	DWG NO 58075904	SH 46.0F

58075900

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB 001	TAB 102	TAB 002	PL ALL
A	LEVEL 1 ISSUE	82	08	27	J. M Boyle 8-13-82	A			A
A1	Level 2 ENXS149		ND		G Dreuth	A1			
B	PHA0XS475	84	06	08	G Dreuth	B	B		B
C	PHA0XS590	84	Nov	14	G Dreuth			C	C
D	PHA0XS696	85	OcT	02	G Dreuth			D	D
	58075904				LOGIC DIAG		A	A	
					TEST DATA				

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY G Weston 81 AUG 12

APPROVED E. Gifford 8-12-82

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE HDUHC PWA WDASE

SIZE	REVISION STATUS FOR	SHEET	REV
X	58075900	1/1	D

DIST. 30

BRUNING 44-141 40366

CE 300 A-3 (1-79)

58075902

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 001	002		SH All
A	LVL 3 ISSUE	82	08	17	J. H. Eagle 8-13-82	A		1-10F	A
B	PHA8XS475	84	06	08	G Drenttle		B	1-10F	B

FOR CONTINUATION OF REVISION STATUS SEE SHEET

BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY D Kajewski 82 Aug 09

APPROVED E Gottfried 8-12-82

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CIL WDASE

SIZE A | REVISION STATUS FOR 58075902 | SHEET 1/1 | REV B

CE 300 A-3 (1-79)

DIST. 37

TAB-002

STANDARD LOCATION CODE PATTERN
X-POS & Y-POS PER 58046507-002
UNLESS OTHERWISE SHOWN, ROTATION IS NORTH

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
00A	SWOG	58020295-007			
00AE	P9	43A114748P9			
00B	1B-495	58002495-001			
00C	1B-473	58002473-001			
00CE	P1043	43C212092P1043			
00D	2D5419	43C216419P1			
00E	RN3C	43B216592P12			
00EE	P1043	43C212092P1043			
00F	1B-476	58002476-001			
00G	1B-476	58002476-001			
00GE	P9	43A114748P9			
00H	1B-476	58002476-001			
00JE	P1043	43C212092P1043			
00L	1U-670	58002670-001			
00LE	P1043	43C212092P1043			
00M	1B-015	58002015-001			
00N	1B-696	58002696-001			
00NE	P9	43A114748P9			
00Q	1B-476	58002476-001			
00QE	P1043	43C212092P1043			
00S	1B-054	58002054-001			
00SE	P1043	43C212092P1043			
00T	2D5419	43C216419P1			
00TE	RSOH	58020479-008			
00U	1B-474	58002474-001			
00UE	P9	43A114748P9			
00V	1B-696	58002696-001			
00W	1B-696	58002696-001			
00WE	P1043	43C212092P1043			
00X	1B-478	58002478-001			
09A	RN3C	43B216592P12			
09AE	P9	43A114748P9			

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
09CE	P1043	43C212092P1043			
09D	1B-644	58002644-001			
09E	1B-644	58002644-001			
09EE	P1043	43C212092P1043			
09F	1B-644	58002644-001			
09FE	RSOH	58020479-008			
09G	1B-644	58002644-001			
09GE	P9	43A114748P9			
09H	1B-644	58002644-001			
09HE	RSOH	58020479-008			
09J	1B-495	58002495-001			
09JE	P1043	43C212092P1043			
09K	1Q-616	58002616-001			
09L	1Q-616	58002616-001			
09LE	P1043	43C212092P1043			
09M	1Q-616	58002616-001			
09ME	RSOH	58020479-008			
09N	1B-495	58002495-001			
09NE	P9	43A114748P9			
09P	1B-475	58002475-001			
09Q	1B-644	58002644-001			
09QE	P1043	43C212092P1043			
09R	1B-015	58002015-001			
09S	1B-495	58002495-001			
09SE	P1043	43C212092P1043			
09T	1B-015	58002015-001			
09TE	RSOH	58020479-008			
09U	1B-017	58002017-001			
09UE	P9	43A114748P9			
09V	1B-644	58002644-001			
09VE	RSOH	58020479-008			
09W	1B-478	58002478-001			
09WE	P1043	43C212092P1043			
09X	1B-478	58002478-001			
18AE	P9	43A114748P9			
18B	1B-644	58002644-001			
18C	1B-653	58002653-001			
18CE	P1043	43C212092P1043			

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
18D	1B-017	58002017-001			
18E	1B-495	58002495-001			
18EE	P1043	43C212092P1043			
18F	1B-476	58002476-001			
18G	1D3491	58002491-001			
18GE	P9	43A114748P9			
18H	1D3491	58002491-001			
18J	1D3491	58002491-001			
18JE	P1043	43C212092P1043			
18K	1D3491	58002491-001			
18L	1B-472	58002472-001			
18LE	P1043	43C212092P1043			
18M	1B-475	58002475-001			
18N	1D3491	58002491-001			
18NE	P9	43A114748P9			
18P	1D3491	58002491-001			
18Q	1D3491	58002491-001			
18QE	P1043	43C212092P1043			
18R	1D3491	58002491-001			
18S	1B-017	58002017-001			
18SE	P1043	43C212092P1043			
18T	1B-015	58002015-001			
18U	1B-472	58002472-001			
18UE	P9	43A114748P9			
18V	1B-652	58002652-001			
18W	1B-473	58002473-001			
18WE	P1043	43C212092P1043			
18X	1U-670	58002670-001			
27A	1B-015	58002015-001			
27AE	P9	43A114748P9			
27C	1B-015	58002015-001			
27CE	P1043	43C212092P1043			
27E	1B-474	58002474-001			
27EE	P1043	43C212092P1043			
27F	1B-474	58002474-001			
27G	1D3491	58002491-001			
27GE	P9	43A114748P9			
27H	1D3491	58002491-001			

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
27J	1D3491	58002491-001			
27JE	P1043	43C212092P1043			
27K	1D3491	58002491-001			
27L	1B-495	58002495-001			
27LE	P1043	43C212092P1043			
27M	1B-053	58002053-001			
27N	1D3491	58002491-001			
27NE	P9	43A114748P9			
27P	1D3491	58002491-001			
27Q	1D3491	58002491-001			
27QE	P1043	43C212092P1043			
27R	1D3491	58002491-001			
27S	1B-474	58002474-001			
27SE	P1043	43C212092P1043			
27T	1B-053	58002053-001			
27U	1B-053	58002053-001			
27UE	P9	43A114748P9			
27V	2D5419	43C216419P1			
27W	1U-670	58002670-001			
27WE	P1043	43C212092P1043			
27X	1U-670	58002670-001			
36A	1Q-616	58002616-001			
36AE	P9	43A114748P9			
36B	1Q-616	58002616-001			
36BE	RSOH	58020479-008			
36C	1B-053	58002053-001			
36CE	P1043	43C212092P1043			
36D	1B-478	58002478-001			
36E	1B-477	58002477-001			
36EE	P1043	43C212092P1043			
36F	1B-015	58002015-001			
36G	1D3491	58002491-001			
36GE	P9	43A114748P9			
36H	1D3491	58002491-001			
36J	1D3491	58002491-001			
36JE	P1043	43C212092P1043			
36K	1D3491	58002491-001			
36L	1C-057	58002057-001			

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
36LE	P1043	43C212092P1043			
36M	1C-057	58002057-001			
36N	1D3491	58002491-001			
36NE	P9	43A114748P9			
36P	1D3491	58002491-001			
36Q	1D3491	58002491-001			
36QE	P1043	43C212092P1043			
36R	1D3491	58002491-001			
36S	1E-011	58002011-001			
36SE	P1043	43C212092P1043			
36T	1E-011	58002011-001			
36U	1B-495	58002495-001			
36UE	P9	43A114748P9			
36V	1B-017	58002017-001			
36W	1U-670	58002670-001			
36WE	P1043	43C212092P1043			
36X	1U-670	58002670-001			
45A	1Q-616	58002616-001			
45AE	P9	43A114748P9			
45B	1Q-616	58002616-001			
45BE	RSOH	58020479-008			
45C	1B-476	58002476-001			
45CE	P1043	43C212092P1043			
45EE	P1043	43C212092P1043			
45F	1B-713	58002713-001			
45G	1C-057	58002057-001			
45GE	P9	43A114748P9			
45H	1C-057	58002057-001			
45J	1C-057	58002057-001			
45JE	P1043	43C212092P1043			
45K	1C-057	58002057-001			
45L	1E-011	58002011-001			
45LE	P1043	43C212092P1043			
45M	1D3491	58002491-001			
45N	1C-057	58002057-001			
45NE	P9	43A114748P9			
45P	1C-057	58002057-001			
45Q	1C-057	58002057-001			

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
45QE	P1043	43C212092P1043			
45R	1C-057	58002057-001			
45S	1N3450	43C216450P1			
45SE	P1043	43C212092P1043			
45T	1B-473	58002473-001			
45U	1B-495	58002495-001			
45UE	P9	43A114748P9			
45V	1B-476	58002476-001			
45W	1P3405	43C216405P1			
45WE	P1043	43C212092P1043			
54A	1Q-616	58002616-001			
54AE	P9	43A114748P9			
54B	1B-644	58002644-001			
54C	1B-479	58002479-001			
54CE	P1043	43C212092P1043			
54D	1E-011	58002011-001			
54E	1B-053	58002053-001			
54EE	P1043	43C212092P1043			
54F	1B-017	58002017-001			
54G	1D3491	58002491-001			
54GE	P9	43A114748P9			
54H	1D3491	58002491-001			
54J	1D3491	58002491-001			
54JE	P1043	43C212092P1043			
54K	1D3491	58002491-001			
54L	1Q-059	58002059-001			
54LE	P1043	43C212092P1043			
54M	1Q-059	58002059-001			
54N	1D3491	58002491-001			
54NE	P9	43A114748P9			
54P	1D3491	58002491-001			
54Q	1D3491	58002491-001			
54QE	P1043	43C212092P1043			
54R	1D3491	58002491-001			
54S	1Q-616	58002616-001			
54SE	P1043	43C212092P1043			
54T	1Q-616	58002616-001			
54U	1B-094	58002094-001			

COMP INSTL LIST - WDASE

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
54UE	P9	43A114748P9			
54V	1B-495	58002495-001			
54VE	RSOH	58020479-008			
54W	1U-670	58002670-001			
54WE	P1043	43C212092P1043			
54X	1U-670	58002670-001			
63A	1Q-616	58002616-001			
63AE	P9	43A114748P9			
63C	1Q-071	58002071-001			
63CE	P1043	43C212092P1043			
63D	1Q-071	58002071-001			
63E	1B-495	58002495-001			
63EE	P1043	43C212092P1043			
63F	1B-015	58002015-001			
63G	1B-495	58002495-001			
63GE	P9	43A114748P9			
63H	1U-670	58002670-001			
63J	1U-670	58002670-001			
63JE	P1043	43C212092P1043			
63K	1U-670	58002670-001			
63L	RN4D	43B216592P17			
63LE	P1043	43C212092P1043			
63M	RN4D	43B216592P17			
63N	1D3492	58002492-001			
63NE	P9	43A114748P9			
63P	1D3492	58002492-001			
63Q	1E-011	58002011-001			
63QE	P1043	43C212092P1043			
63R	1B-644	58002644-001			
63RE	RSOH	58020479-008			
63S	1B-015	58002015-001			
63SE	P1043	43C212092P1043			
63T	1B-056	58002056-001			
63U	1B-017	58002017-001			
63UE	P9	43A114748P9			
63V	1U-670	58002670-001			
63WE	P1043	43C212092P1043			
72A	4G4408	43C216408P1			

COMP INSTL LIST - WDASE

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
72AE	P9	43A114748P9			
72B	RN9A	43B216592P22			
72C	4G4408	43C216408P1			
72CE	P1043	43C212092P1043			
72D	4G4408	43C216408P1			
72E	RN9A	43B216592P22			
72EE	P1043	43C212092P1043			
72F	1B-017	58002017-001			
72G	1B-714	58002714-001			
72GE	P9	43A114748P9			
72H	1B-696	58002696-001			
72J	1B-017	58002017-001			
72JE	P1043	43C212092P1043			
72K	1B-713	58002713-001			
72L	1B3600	58002600-001			
72LE	P1043	43C212092P1043			
72M	1B3600	58002600-001			
72N	1B3600	58002600-001			
72NE	P9	43A114748P9			
72P	1B3600	58002600-001			
72Q	1B3600	58002600-001			
72QE	P1043	43C212092P1043			
72R	1B3600	58002600-001			
72S	1B3600	58002600-001			
72SE	P1043	43C212092P1043			
72T	1B3600	58002600-001			
72U	1B-017	58002017-001			
72UE	P9	43A114748P9			
72V	1B-476	58002476-001			
72W	1Q-668	58002668-001			
72WE	P1043	43C212092P1043			
72X	1Q-668	58002668-001			
81A	1Q-066	58002066-001			
81AE	P9	43A114748P9			
81B	1Q-066	58002066-001			
81C	4G4408	43C216408P1			
81CE	P1043	43C212092P1043			
81D	4G4408	43C216408P1			

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
81E	4G4408	43C216408P1			
81EE	P1043	43C212092P1043			
81F	1B-015	58002015-001			
81G	1B-696	58002696-001			
81GE	P9	43A114748P9			
81H	1B-053	58002053-001			
81J	RN4D	43B216592P17			
81JE	P1043	43C212092P1043			
81K	1N3450	43C216450P1			
81L	1B-472	58002472-001			
81LE	P1043	43C212092P1043			
81M	4G4408	43C216408P1			
81N	1B3600	58002600-001			
81NE	P9	43A114748P9			
81P	1B3600	58002600-001			
81Q	1B3600	58002600-001			
81QE	P1043	43C212092P1043			
81R	1B3600	58002600-001			
81S	1B-053	58002053-001			
81SE	P1043	43C212092P1043			
81T	1B-473	58002473-001			
81U	1B-495	58002495-001			
81UE	P9	43A114748P9			
81V	1B3600	58002600-001			
81W	1B3600	58002600-001			
81WE	P1043	43C212092P1043			
81X	1B3600	58002600-001			
90A	1E-011	58002011-001			
90AE	P9	43A114748P9			
90B	4G4408	43C216408P1			
90C	4G4408	43C216408P1			
90CE	P1043	43C212092P1043			
90D	4G4408	43C216408P1			
90E	4G4408	43C216408P1			
90EE	P1043	43C212092P1043			
90F	1S-635	58002635-001			
90G	1S-635	58002635-001			
90GE	P9	43A114748P9			

TAB-002

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
90H	1Q3488	58002488-001			
90J	1Q3488	58002488-001			
90JE	P1043	43C212092P1043			
90K	2S2780	98002780-002			
90L	2S2780	98002780-002			
90LE	P1043	43C212092P1043			
90M	2S2780	98002780-002			
90N	2S2780	98002780-002			
90NE	P9	43A114748P9			
90P	1B3654	58002654-001			
90Q	1B3654	58002654-001			
90QE	P1043	43C212092P1043			
90R	1Q3488	58002488-001			
90S	1Q3488	58002488-001			
90SE	P1043	43C212092P1043			
90T	1S-635	58002635-001			
90U	1S-635	58002635-001			
90UE	P9	43A114748P9			
90V	4G4408	43C216408P1			
90W	4G4408	43C216408P1			
90WE	P1043	43C212092P1043			
90X	1B3600	58002600-001			