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HP 12539B/C TIME BASE GENERATOR DIAGNOSTIC

reference manual

For HP 1000 Computers

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11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, 95014

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Section I

INTRODUCTION

1-1. GENERAL

This diagnostic checks the operation of the HP 12539B or C Time Base Generator (hereafter refered to as the TBG). The basic I/O portion of the TBG, which includes the Flag and Control circuits, will be tested. The diagnostic also aids the operator in detecting any component that has failed.

The diagnostic will run with the decade divider (jumper W1 if a 12539B, or W2 if a 12539C) in position A or B. The B position is used to reduce the time required to check the upper four decade dividers. Note that the HP 12539B TBG decade divider jumper is labeled W1A or B while the HP 12539C jumper is W2A or B. For the purposes of this diagnostic, the position for the decade divider short time will be called the B position. This will eliminate confusion between designations in TBG models.

The specified accuracy of the Time Base Generator can not be checked with this diagnostic. The Time Tolerance Test 12 can only check for an accuracy of better than ± 2%.

1-2. REQUIRED HARDWARE

The following hardware is required:

a. An HP 2100 series computer with at least 4K of memory.

b. An HP 12539B TBG with jumper W1 in position A or B, or an HP 12539C with jumpers W1 and W2 in position A or B.

c. A diagnostic input device (for loading only).

d. Optional: a console teleprinter device for message reporting.

1-3. REQUIRED SOFTWARE

The following software is required:

a. Diagnostic Configurator Product No. 24296 used for equipment configuration and as a console device driver.

Binary object tape	Part No. 24296-60001
Manual	Part No. 02100-90157

b. HP 12539B/C Time Base Generator Diagnostic binary object tape, Part No. 12539-16001.

Note: The Diagnostic Serial Number (DSN) for the TBG diagnostic, which resides in memory location 126 (octal), is 103301 (octal).

Section II

PROGRAM ORGANIZATION

2-1. ORGANIZATION

This diagnostic program consists of eleven tests plus a control and initialization section. The initialization and control section accepts the select code and options required by the tests. The tests are called into execution by the control section as sequential or selectable subroutines. The following circuits (or functions) are placed under test by this diagnostic:

a. Basic I/O (Flag and Interrupt logic) - Test ØØ (octal).

b. Relative time - Tests Ø1 through 1Ø (octal).

c. Error Status logic - Test 11 (octal).

d. Time tolerance check - Test 12 (octal).

2-2. TEST CONTROL AND EXECUTION

The diagnostic outputs a title message to the console device for operator information and then executes the tests according to the options selected on the Switch Register. The control section primarily checks Switch Register bits 15, 13, and 12.

The diagnostic outputs a title message with the DSN to the console device for operator information and then executes the tests according to the options selected on the Switch Register. The control section primarily checks Switch Register bits 15, 13, and 12.

Test sections are executed one after the other in each diagnostic pass. User selection or default will determine which test sections will be executed. (Refer to paragraph 2-3.)

2-3. TEST SELECTION

The operator has the capability of selecting his own tests or sequences of tests with the help of bit 9 in the Switch Register. Test selections are made after the diagnostic has been configured. Paragraph 3-5 outlines test selections.

2-4. MESSAGE REPORTING

There are two types of messages output for diagnostics: error and information. Error messages are used to inform the operator when the TBG fails to respond to a given control or sequence. Information messages are used to inform the operator of the progress of the diagnostic or to instruct the operator to perform some operations related to the function of the unit. In the latter case, an associated halt will occur to allow the operator time to perform the function. The operator must then press RUN. If a console device is used, the printed message will be preceded by an E (error) or H (information) and a number (in octal). The number is also related to the halt code when a console device is not available. Examples of error and information messages are as follows:

Example - Error with halt

Message: E031 CARD FAILED TO TIME OUT
Halt Code: 102031 (octal) (T-register or Memory Data Register)

Example - Information with halt

Message: H024 PRESS PRESET (EXT & INT), RUN
Halt Code: 102024 (octal)

Example - Information only

Message: H025 BI-O COMP
Halt Code: None

Error messages can be suppressed by setting Switch Register bit 11 and error halts can be suppressed by setting Switch Register bit 14. This is useful when looping on a single section that has several errors.

Information messages are suppressed by setting Switch Register bit 10.

Operator intervention is suppressed by setting Switch Register bit 8 (i.e., Preset Test in BI-O). When Switch Register bit 12 is set the tests that are selected will be repeated, and all operator intervention will be suppressed.

2-5. DIAGNOSTIC LIMITATIONS

TBG capability for receiving, passing, and denying priority (priority string logic) is not completely checked by this diagnostic. If the TBG does not receive priority (i.e., PRH from the next lower select code) an error E014 NO INT will occur. To check this, remove an interface of a lower select code and run the Basic I/O test. The above mentioned error should occur. Checking the TBG's ability to pass or deny priority is beyond the scope of this diagnostic.

Section III

OPERATING PROCEDURE

3-1. LOADING AND CONFIGURING

A flowchart of the operating procedure is provided in figure 3-1. (Note the jumper setting of W1 on the 12539B TBG board, or of W1 and W2 on the 12539C TBG board.

3-2. RUNNING THE DIAGNOSTIC

The program will execute the diagnostic according to options selected in the Switch Register. At the completion of each pass of the diagnostic, the pass count is printed on the console device for operator information. If Switch Register bit 12 was not set, the computer will halt with 102077 (octal) in the Memory Data Register. At this point, the A-register contains the pass count. To run another pass, the operator need only press RUN.

3-3. RESTARTING

The program may be restarted by setting the P-register to 2000 (octal). Select Switch Register options shown in table 3-2 and press RUN.

If a trap cell halt occurs (106077 octal), the user must determine the cause of the interrupt or transfer of control to the location shown in the M-register. The program may need to be reloaded to continue.

3-4. RECONFIGURATION

The diagnostic may be reconfigured by setting the P-register to 100 (octal). Set the Switch Register as per table 3-1 and press RUN.

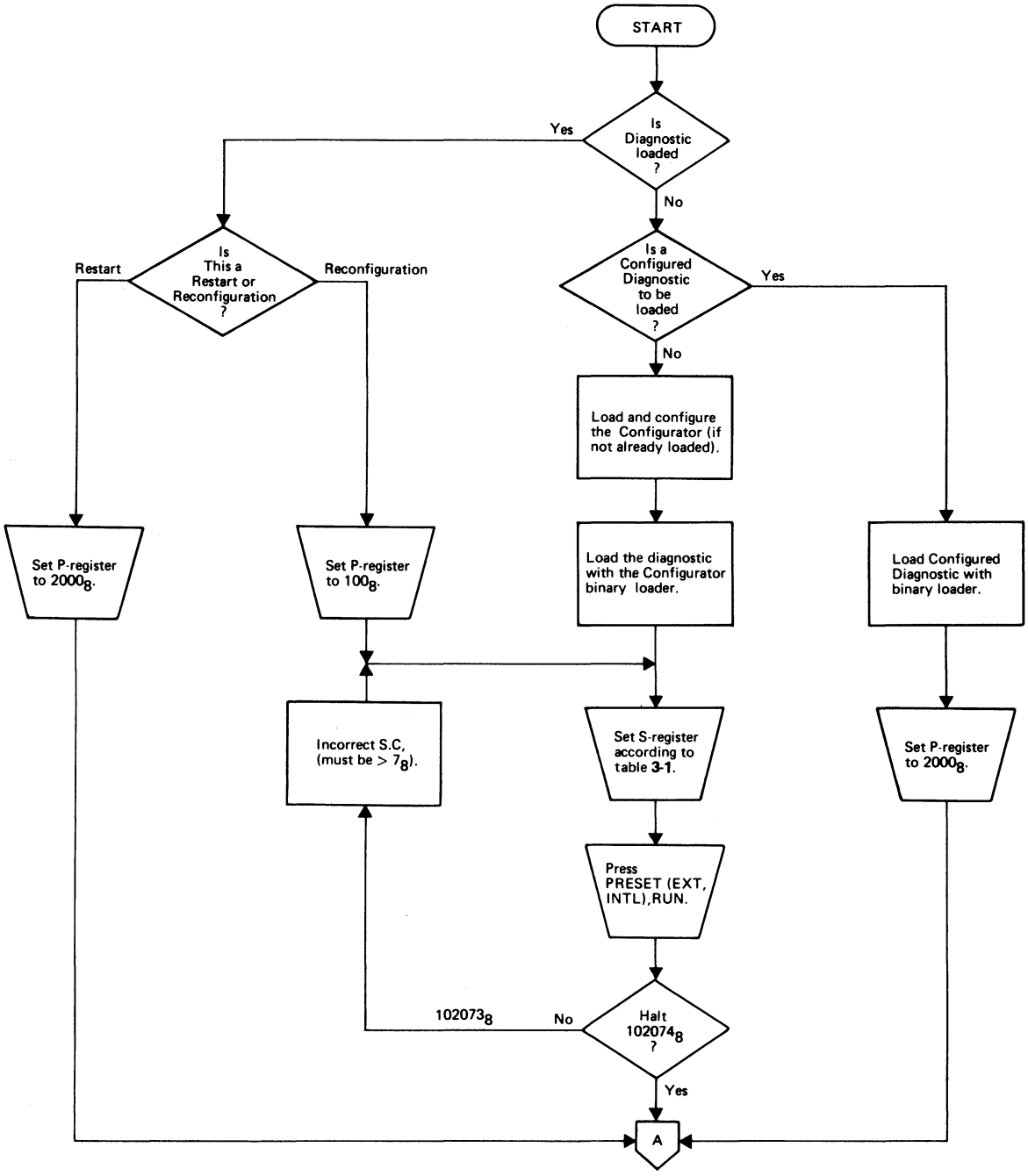

Figure 3-1. Operating Procedure Flowchart (Sheet 1 of 2)

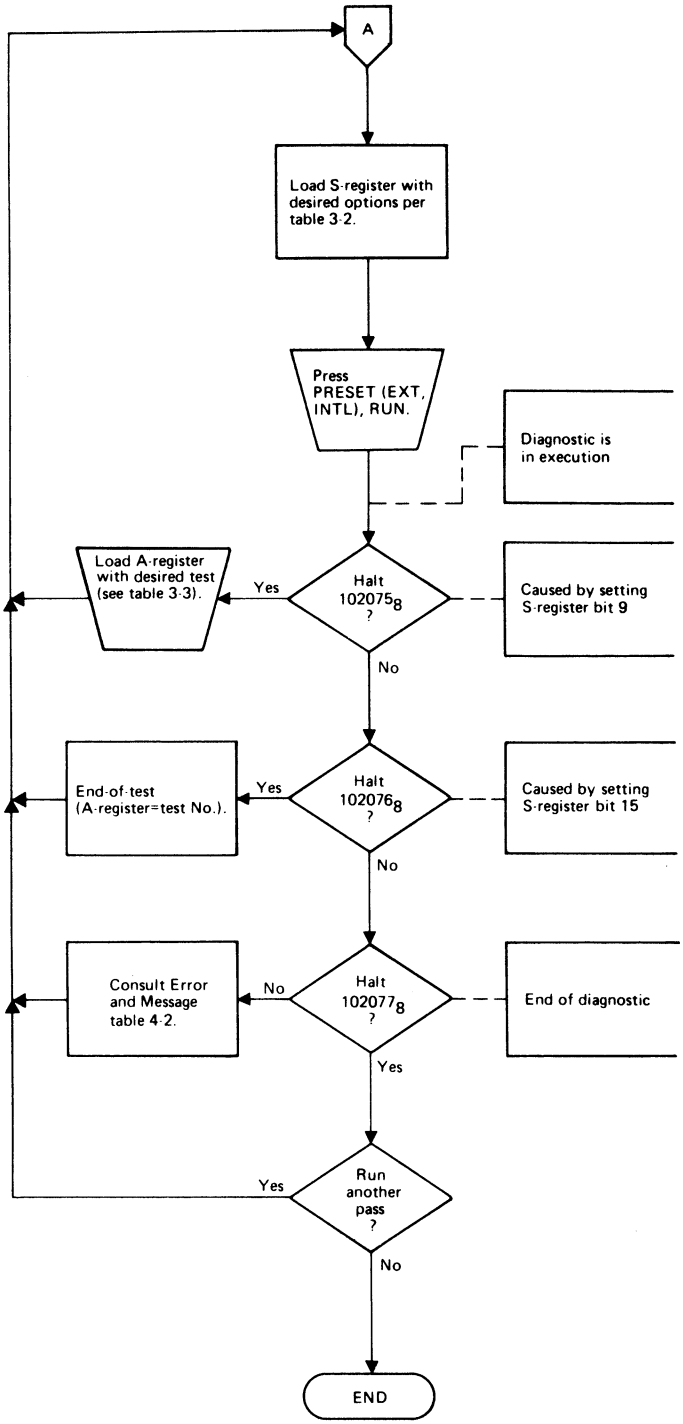

Figure 3-1. Operating Procedure Flowchart (Sheet 2 of 2)

Table 3-1. Initial Switch Register Options

BITS	12539B BOARD	12539C BOARD
0-5	Select code of 12539B/C board.	
6-13	Reserved	
14	Clear	Clear if W1 in position A; set if in position B.
15	Clear if W1 in position A; set if in position B.	Clear if W2 in position A; set if in position B.

Table 3-2. Switch Register Test Options

BIT	MEANING IF SET
0-7	Reserved
8	Suppress tests requiring operator intervention.
9	Abort current diagnostic execution and halt (102075); the user may specify a new group of tests in the A-register. Then clear bit 9 and press RUN.
10	Suppress non-error messages.
11	Suppress error messages.
12	Repeat all selected tests after diagnostic run has completed without halting. Message "PASS XXXXXX" will be output before looping unless bit 10 is set or a teletype is not present. Also, those tests requiring operator intervention will be suppressed.
13	Repeat last test executed (loop on test).
14	Suppress error halts.
15	Halt (102076) at the end of each test; the A-register will contain the test number in octal.

Table 3-3. Test Selection Summary

A-REGISTER BIT	IF SET WILL EXECUTE
Ø	Test Ø BASIC I/O
1	Test 1 Ø.1 Millisecond Relative Time
2	Test 2 1.Ø Millisecond Relative Time
3	Test 3 1Ø Milliseconds Relative Time
4	Test 4 1ØØ Milliseconds Relative Time
5	Test 5 1 Second Relative Time
6	Test 6 1Ø Seconds Relative Time
7	Test 7 1ØØ Seconds Relative Time
8	Test 1Ø 1ØØØ Seconds Relative Time
9	Test 11 Logic Test
1Ø	Test 12 Time Tolerance Test
11 to 15	Reserved

If user selection is not requested (Switch Register bit 9 is not set) the program will execute all tests (Tests Ø through 12).

If user selection is requested (Switch Register bit 9 is set) and bit Ø through 1Ø of the A-register are cleared, all tests will be executed. If one or several bits of the A-register (not including bits 11 through 15) are selected only the appropriate tests will be executed. Bits 11 through 15 are disregarded.

Section IV

DIAGNOSTIC PERFORMANCE

4-1. TEST DESCRIPTION

Tests Ø through 12 are described below. Refer to table 4-2 (comments on halt codes) for additional details on the content of each test.

4-2. BASIC I/O TEST Ø

Note that there are seven subtests in Test Ø, as follows.

Subtest 1 - Checks the ability to clear, set, and test the interrupt system. The following instruction combinations are tested:

CLF Ø - SFC Ø
CLF Ø - SFS Ø
STF Ø - SFC Ø
STF Ø - SFS Ø

Errors in the above sequences produce error messages EØØØ through EØØ3 as shown in table 4-2.

Subtest 2 - Checks the ability to clear, set and test the TBG flag. The following instruction combinations are tested:

CLF CH - SFC CH
CLF CH - SFS CH
STF CH - SFC CH
STF CH - SFS CH

Errors in the above sequences produce error messages EØØ5 through EØ1Ø as shown in table 4-2.

Subtest 3 - Checks that the test select code does not cause an interrupt with the flag and control set on the TBG and the interrupt system off. The sequence of instructions is shown below:

```
STF Ø
STF CH
STC CH
CLF Ø
```

The CLF Ø instruction should inhibit an interrupt from occuring. Error message EØØ4 occurs if CLF Ø fails.

Subtest 4 - Checks that the flag of the TBG under test is not set when all other select code flags are set. Error message EØ11 occurs if a flag is set incorrectly.

Subtest 5 - Checks the ability of the TBG to interrupt. With the flag and control set and the interrupt system on, the TBG should interrupt. If the interrupt is missing error message EØ14 occurs.

Checks that the interrupt occured where expected. The interrupt should not occur before a string of priority-affecting instructions are executed. The following instructions are used to check the hold off operation:

```
STC 1
STF 1
CLC 1
CLF 1
JMP *+1,I
DEF *+1
JSB *+1,I
DEF *+1
NOP
```

Error messages EØ12 and/or EØ15 will occur if the hold off failed. If a second interrupt is encountered after the interrupt system has been turned back on error message EØ13 will occur.

Checks that no instruction was missed during the interrupt (EØ26 INT EXECUTION ERROR).

Subtest 6 - Checks that with the interrupt system on and the CH control and flag set, there is no interrupt following a CLC CH instruction. The following sequence of instructions are used:

```
STC CH
STF CH
STF Ø
CLC CH
```

If the CLC CH fails to inhibit an interrupt, error message EØ16 will occur.

Checks that the CLC Ø instruction inhibits interrupts when the CH control and flag are set. The following sequence of instructions is used.

```
CLF CH
STC CH
STF CH
STF Ø
CLC Ø
```

If the CLC Ø fails to inhibit an interrupt, error message EØ17 will occur.

Subtest 7 - Checks that the PRESET (EXTERNAL and INTERNAL if applicable) switch(es) on the operator panel performs the following actions:

Sets the TBG flag (EXTERNAL).
Clears TBG control (EXTERNAL).
Turns off the interrupt system (INTERNAL).
Clears the I/O data lines (EXTERNAL).

4-3. RELATIVE TIME TESTS 1 THROUGH 1Ø

These tests ensure the TBG will interrupt within twice the time allowance for the gate time selected. They are go/no go tests only. If the TBG under test does not pass these tests, the Logic and Tolerance tests will fail.

Test 1: Ø.1 millisecond.

Test 2: 1.Ø millisecond.

Test 3: 1Ø milliseconds.

Test 4: 1ØØ milliseconds.

Test 5: 1 second (B, 1 millisecond).

Test 6: 1Ø seconds (B, 1Ø milliseconds).

Test 7: 1ØØ seconds (B, 1ØØ milliseconds).

Test 1Ø: 1ØØØ seconds (B, 1.Ø second).

An error or failure to time out will result in an error message EØXX CARD FAILED TO TIME OUT where the XX will equal 31 (octal) for Test 1 and up to 4Ø (octal) for Test 1Ø. A check is made also to ensure that the TBG does not interrupt immediately. This error would result in an error message EØXX CARD INTP'D IMMEDIATELY where the XX will equal 41 (octal) for Test 1 through 5Ø (octal) for Test 1Ø.

4-4. LOGIC TEST 11

This section checks the error status report in the following sequence:

Checks that the Error FF is clear. An STC CH instruction should clear the Error FF.

Allows TBG to time out. This sets up the 1 millisecond time out and checks that it does time out.

Checks that the Error FF did not set. The Error FF should not be set after the first interval.

Checks that flag was set after time out.

Checks that TBG does not interrupt again. Here the interrupt is turned back on and the computer waits one additional millisecond to insure that the TBG will not interrupt again if it has not been serviced.

Checks that status shows error. The Error FF should now be set because the TBG was not serviced before another complete time interval elapsed.

Checks that STC CH clears error.

Checks that OTB CH stops interrupts. The OTB instruction should reset the counters and the Count Enable FF.

4-5. TIME TOLERANCE TEST 12

This is primarily an oscillator test using the 100 millisecond gate time. The interrupt must occur after 98 milliseconds but before 102 milliseconds.

Error reports:

E061 INT BEFORE 98 MILLISECONDS
E062 INT AFTER 102 MILLISECONDS
E063 NO INTERRUPT

4-6. ERROR INFORMATION MESSAGE/HALT CODES

Tables 4-1 and 4-2 summarize halt codes and messages.

Table 4-1. Halt Code Summary

HALT	MEANING
TESTS Ø (OCTAL) THRU 12 (OCTAL)	
102000 thru 102063	Error (E) or information (H) messages ØØ thru 63 (octal).
CONTROL	
102073	Select code input error.
102074	Select code input complete.
102075	User selection request.
102076	End of Test (A-register contains test number).
102077	End of diagnostic run.
106077	Trap cell halt in locations 2 thru 77 (octal).

Table 4-2. Error and Information Messages and Halt Codes

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102073	Configuration	None	I/O select code entered at configuration is invalid. Must be greater than 7 (octal). Reenter a valid select code and press RUN.
102074	Configuration	None	Select code entered during configuration is valid. Enter program option bits in Switch Register and press RUN.
102075	Test Control	None	Test selection request resulting from Switch Register bit 9 being set. Enter the desired group of tests to be executed in the A-register then press RUN.
102076	Test Control	None	End of test halt resulting from Switch Register bit 15 being set (A-register equals test number). To continue press RUN.
102077	Test Control	PASS XXXXXX	Diagnostic run complete. (A-register value equals pass count.) Register options may be changed. To continue, press RUN.
106077	Test Control	None	Halt stored in locations 2 through 77 (octal) to trap interrupts which may occur unexpectedly because of hardware malfunctions. M-register contains the I/O slot number of interrupt. Diagnostic may be partially destroyed if halt occurs. The program may have to be reloaded; the problem should be corrected before proceeding.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
None	Test Control	TBG DIAGNOSTIC, DSN = XXXXX	Introductory message with DSN
None	Test Control	TEST XX	Information message before error message (XX equals test number). Message occurs only once within a test and is suppressed for any subsequent messages within the same test.
102000	Test 0	E000 CLF 0-SFC 0 ERROR	CLF/SFC 0 combination failed. CLF did not clear flag or SFC caused no skip with flag clear.
102001	Test 0	E001 CLF 0-SFS 0 ERROR	CLF/SFS 0 combination failed. CLF did not clear flag or SFS caused skip with flag clear.
102002	Test 0	E002 STF 0-SFC 0 ERROR	STF/SFC 0 combination failed. STF did not set flag or SFC caused skip with flag set.
102003	Test 0	E003 STF 0-SFS 0 ERROR	STF/SFS 0 combination failed. STF did not set flag or SFS caused no skip with flag set.
102004	Test 0	E004 CLF 0 DID NOT INHIBIT INT	With card flag and control set, CLF 0 did not turn off interrupt system.
102005	Test 0	E005 CLF CH-SFC CH ERROR	CLF/SFC CH combination failed. CLF did not clear flag or SFC caused no skip with flag clear.
102006	Test 0	E006 CLF CH-SFS CH ERROR	CLF/SFS CH combination failed. CLF did not clear flag or SFS caused skip with flag clear.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102007	Test 0	E007 STF CH-SFC CH ERROR	STF/SFC CH combination failed. STF did not set flag or SFC caused skip with flag set.
102010	Test 0	E010 STF CH-SFS CH ERROR	STF/SFS CH combination failed. STF did not set flag or SFS caused no skip with flag set.
102011	Test 0	E011 STF XX SET CARD FLAG	Select code screen test failed. A-register equals XX (octal). XX equals select code that caused card flag to set.
102012	Test 0	E012 INT DURING HOLD OFF INSTR	Interrupt occured during an I/O instruction or a JMP/JSB indirect instruction.
102013	Test 0	E013 SECOND INT OCCURED	Card interrupted a second time after initial interrupt was processed.
102014	Test 0	E014 NO INT	No interrupt occured with card flag and control set and the interrupt system on.
102015	Test 0	E015 INT RTN ADDR ERROR	Interrupt did not occur at the correct location in memory.
102016	Test 0	E016 CLC CH ERROR	CLC CH did not clear card control with the interrupt system on.
102017	Test 0	E017 CLC 0 ERROR	CLC 0 did not clear the TBG control with the interrupt system on.
102020	Test 0	E020 PRESET (EXT) DID NOT SET FLAG	PRESET (EXT) did not set the card flag.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102021	Test 0	E021 PRESET (INT) DID NOT DISABLE INTS	PRESET (INT) did not disable the interrupt system.
102022	Test 0	E022 PRESET (EXT) DID NOT CLEAR CONTROL	PRESET (EXT) did not clear control.
102023	Test 0	E023 PRESET (EXT) DID NOT CLEAR I/O LINES	PRESET (EXT) did not clear I/O data lines.
102024	Test 0	H024 PRESS PRESET (EXT & INT), RUN	Press PRESET (EXTERNAL/ INTERNAL) then RUN.
None	Test 0	H025 BI-O COMP	Basic I/O tests completed.
102026	Test 0	E026 INT EXECUTION ERROR	Interrupt was not processed correctly.
None	Tests 1 thru 12	H030 TEST XX IN PROGRESS	Used to indicate where the diagnostic is. XX equals the test number.
102031 to 102040	Tests 1 thru 10	E0XX CARD FAILED TO TIME OUT	The gate time requested did not interrupt within the expected time. XX equals 31 (octal) for Test 1 and up to 40 (octal) for Test 10 (octal).
102041 to 102050	Tests 1 thru 10	E0XX CARD INTP'D IMMEDIATELY	The TBG did not try to time out. The interrupt came as soon as the interrupt system was turned on.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102051	Test 11	E051 ERROR FF NOT RESET BY STC INSTRUCTION	Check that Error FF is clear to start with. An STC CH instruction should reset the Error FF.
102052	Test 11	E052 CARD FAILED TO TIME OUT	Allow TBG to time out; this sets up the 1 millisecond time out and checks that it does time out.
102053	Test 11	E053 ERROR FF SET AFTER ONLY ONE GATE TIME	Check that Error FF did not set. The Error FF should not be set after the first interval.
102054	Test 11	E054 FLAG DID NOT SET AFTER TIME OUT	Check that flag was set after time out.
102055	Test 11	E055 INTP'D AFTER FIRST TIME OUT	Check that TBG does not interrupt again. Here the interrupt is turned back on and the computer waits another millisecond to insure TBG will not interrupt again if it has not been serviced.
102056	Test 11	E056 ERROR FF DID NOT SET AFTER TWICE THE TIME INTERVAL	Status check shows error. The Error FF should now be set because the TBG was not serviced before another complete time interval elapsed.
102057	Test 11	E057 ERROR FF NOT RESET BY STC INSTRUCTION	Check that STC CH clears error.
102060	Test 11	E060 OTB INSTRUCTION DID NOT STOP INTERRUPT	Check that OTB CH stops interrupts. The OTB instruction should reset the counters and the Count Enable FF.
102061	Test 12	E061 INT BEFORE 98 MILLISECONDS	Interrupt occurred before 98 milliseconds.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102062	Test 12	E062 INT AFTER 102 MILLISECONDS	Interrupt occurred after 102 milliseconds.
102063	Test 12	E063 NO INTERRUPT	No interrupt occurred.

NOTE: Test numbers and error halt codes are in octal.

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