INSTALLATION AND MAINTENANCE MANUAL

2116C COMPUTER

VOLUME THREE

HEWLETT hp PACKARD

HP 2116C

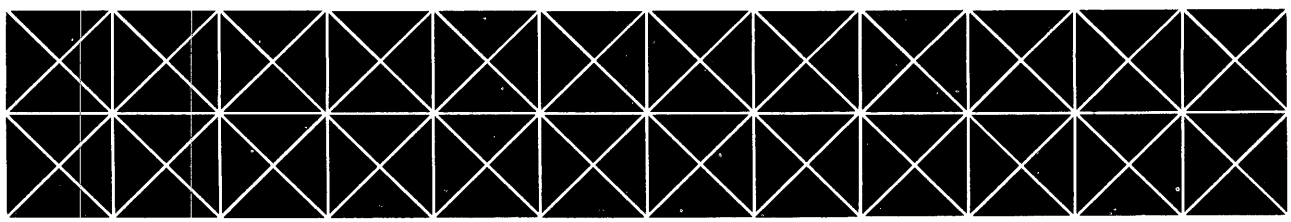
VOLUME THREE

INPUT/OUTPUT SYSTEM OPERATION MANUAL

MODEL 2116B

COMPUTER

SERIALS PREFIXED: 823- & 824-



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MANUAL ADDENDUM

GENERAL. The purpose of this addendum is to adapt the attached HP 2116B Input/Output System Operation Manual for use with the HP 2116C Computer with serial numbers prefixed 980- and above. Information in the manual applies, with the exceptions listed below as addendum, to the HP 2116C Computer. When available, the final version of the HP 2116C manual will be provided as a replacement for this manual.

ADDENDUM. To adapt this manual for use with the HP 2116C Computer, make the following changes:

1. Change all 2116B references to 2116C.

2. Page 2-13, paragraph 2-53. Delete subparagraphs "b. Option 02," and "c. Option 03." These options to the HP 2150B Input/Output and Memory Extender are not available for use with the HP 2116C Computer.

3. Page 2-13. Replace table 2-3 with the table included in this addendum.

4. Page 2-14, paragraph 2-56. Change all references to a "computer with an 8k or 16k memory" to "computer with an 8k, 16k, 24k, or 32k memory." The replacement table 2-3, above, provides the additional information for a computer with 24k or 32k of memory.

5. Page 1-0, figure 1-1. Some 2116C Computers have a toggle-type power switch instead of the illustrated pushbutton switch.

For additional copies of the 2116C Volume 3 manual, specify part no. 02116-91757.

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Table 2-3. Internal/External Power Supply Requirements

REQUIREMENTS	SUPPLY CURRENTS (AMP)			
	+12V	-12V	-2V	+4.5V
CURRENT AVAILABLE FROM POWER SUPPLIES				
Computer Power Supply	6	6	22.5	*22.5
Computer and HP 2160A Power Supplies	6	6	32.5	**32.5
CURRENT REQUIRED BY COMPUTER WITH NO PROCESSOR OR INPUT/OUTPUT OPTIONS				
Computer with 8k Memory	0.15	0.25	14.3	23.0
Computer with 16k Memory	0.15	0.25	15.6	24.2
Computer with 24k Memory	0.15	0.25	16.9	25.4
Computer with 32k Memory	0.15	0.25	18.2	26.6
CURRENT AVAILABLE FOR OPTIONS				
Computer with 8k Memory	5.85	5.75	8.2	†13.8
Computer with 16k Memory	5.85	5.75	6.9	†13.9
Computer with 24k Memory	5.85	5.75	5.6	†14.0
Computer with 32k Memory	5.85	5.75	4.3	†14.1
Computer with 8k Memory and HP 2160A Power Supply Extender	5.85	5.75	18.2	†23.8
Computer with 16k Memory and HP 2160A Power Supply Extender	5.85	5.75	16.9	†23.9
Computer with 24k Memory and HP 2160A Power Supply Extender	5.85	5.75	15.6	†24.0
Computer with 32k Memory and HP 2160A Power Supply Extender	5.85	5.75	14.3	†24.1

NOTES:
* Plus the current drawn from the -2V supply by the Computer with memory and options. Maximum available from +1.5V supply is 45 amperes.

** Plus the current drawn from the -2V supply by the Computer with memory and options. Maximum available from +4.5V supply is 65 amperes.

† Plus Plus the current drawn from the -2V supply by the selected options.

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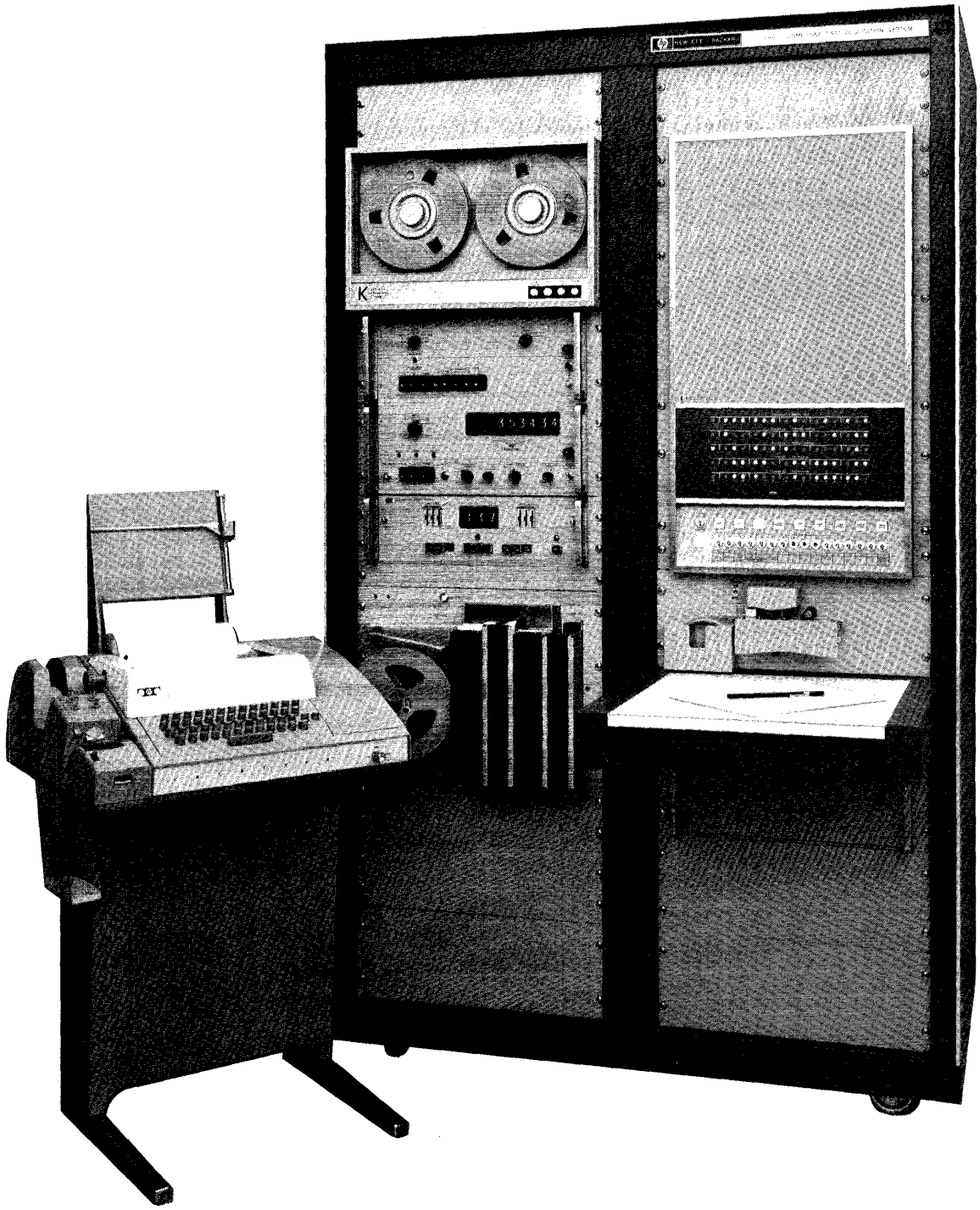


Figure 1-1. Typical HP 2116B Computer System

SECTION I
INTRODUCTION

1-1. COMPUTER SYSTEM.

1-2. The Computer System (Figure 1-1) consists of the HP 2116B Computer, associated input/output devices, and the necessary interface accessory kits and software.

1-3. The basic Computer is able to control and service up to 16 peripheral devices. Plug-in I/O options are available for expansion of Computer capabilities to 48 devices, and a wide range of input/output options are available. Refer to Volume One for detailed information on the Computer and available processor options, Volume Two for processor maintenance, and to Volume Four for programming information.

1-4. MANUAL CONTENTS.

1-5. Section II of this manual contains a description of the input/output structure of the HP 2116B Computer. Theory of Operation information and Logic Diagrams for the I/O Control card, the I/O Address card, and the Resistance Load card are contained in Sections III, IV, and V, respectively. Complete Operating and Service manuals are provided with each input/output device and Interface Kit in a system.

SECTION II
INPUT/OUTPUT STRUCTURE

2-1. INTRODUCTION.

2-2. The input/output (I/O) structure of the HP 2116B Computer system consists of input/output devices, their interface cards and interconnecting cables, an I/O Control card, and an I/O Address card (see Figure 2-1). The Input/Output section of the basic Computer, located directly behind the front panel and toward the bottom of the Computer, provides slots for 16 plug-in interface cards and two slots for the I/O Control and I/O Address cards. (A Resistance Load card is also used when less than 16 interface cards are used in the system; it then plugs into the highest-numbered interface-card slot.) The Computer selects and communicates with the interface cards through the I/O Control card, the I/O Address card, and through direct wiring to the interface card slot connectors. In most cases, each interface card is capable of interfacing a separate input/output device. Detailed information on computer logic required for control of the input/output devices is contained in the Installation and Maintenance Manual, Volume Two. Paragraphs 2-5 through 2-13 in this section contain a general description of computer logic operation in conjunction with the elements within the input/output structure.

2-3. The input/output structure also provides a means for the input/output devices to interrupt the computer program when they require servicing. When devices request an interrupt, the Computer processes the requests on a priority basis. Each input/output device has its own level of priority and when interrupting, causes program execution of the contents of a memory location uniquely associated with the interrupting device.

2-4. The number of input/output devices in the system is expandable to 32 or 48 devices simply by adding a HP 2151A or HP 2150B Extender Module, respectively, and the appropriate interface cards, cables, and devices. The interface cards and cables required for each input/output device are contained in an Interface Kit. Each addition, then, requires that the Interface Kit and device be ordered separately. Refer to the HP 2116B Computer Data Sheet for a description and ordering information.

2-5. COMPUTER SYSTEM INPUT/OUTPUT OPERATIONS.

2-6. GENERAL.

2-7. Figure 2-2 illustrates the main elements of the computer system concerned with the control of input/output operations. All elements shown are contained in the computer mainframe, except for the external devices. Although the R-, S-, and T-Buses are represented as single lines in Figure 2-2, each bus is actually 16 individual lines. Also, interface arrangements are shown for only two external devices, one input and one output, where as many as 48 devices may exist. The elements illustrated process all input/output operations in two ways, as follows:

a. Processes Input/Output instructions.

b. Processes interrupt requests from the external devices.

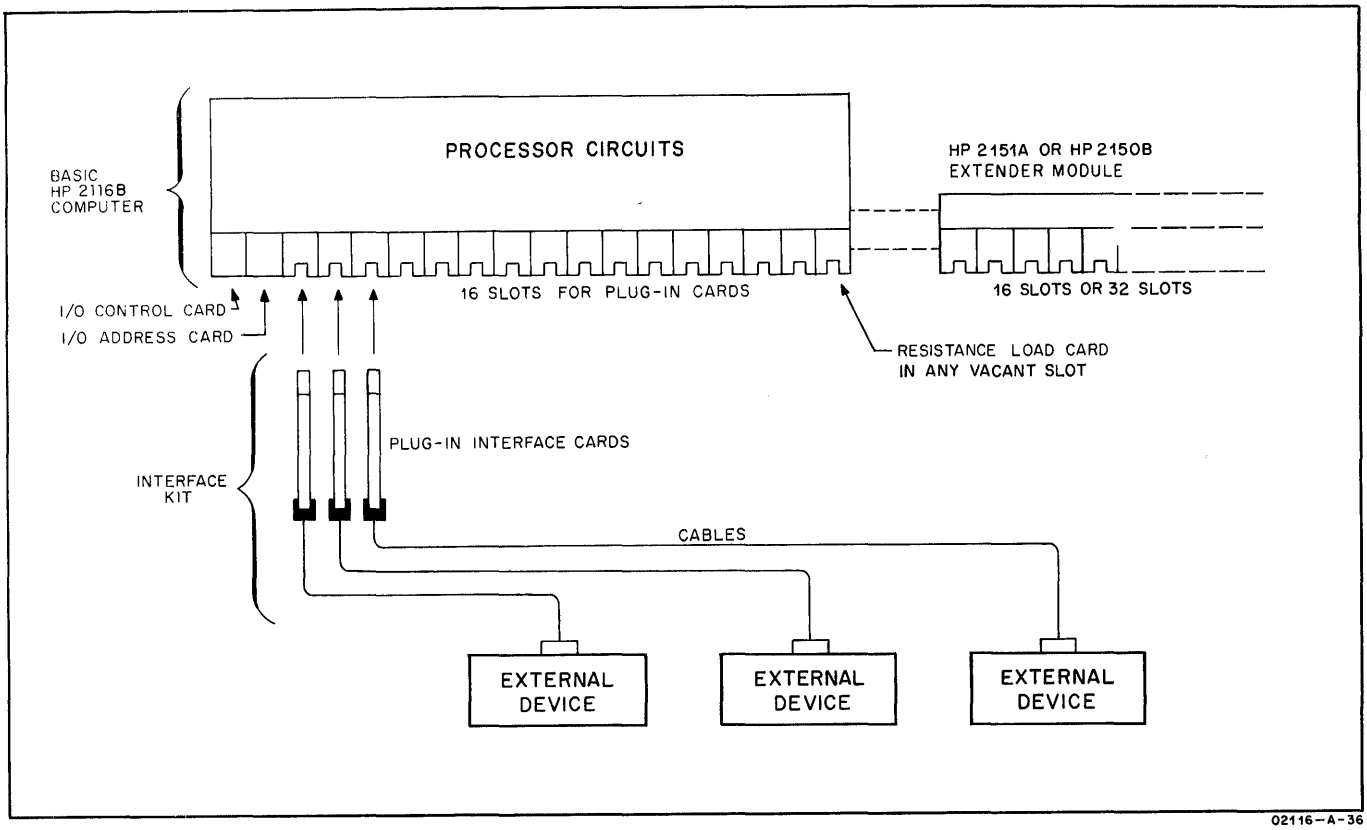


Figure 2-1. Input/Output Structure

2-8. INPUT/OUTPUT INSTRUCTIONS.

2-9. Refer to Figure 2-2. Input/Output instructions from memory via the T-Register are decoded by the I-Register and routed to the various register gate inputs and to the Control Logic which translates the instructions into appropriate driving signals. Instruction Commands are routed to a particular interface card and external device as determined by the Select Code from the T-Register via the I/O Address card. These signals can set or reset the Control and Flag flip-flops (FFs) on the interface cards and can test the set or reset condition of the Flag flip-flops. The Control and Flag flip-flops are used to control data transfer between the interface card and the external device.

2-10. The IOI (I/O Input) signal strobes all interface cards for input data as a result of a Load Into A (LIA), Load Into B (LIB), Merge Into A (MIA), or a Merge Into B (MIB) instruction. Only the data from the interface card selected by the Select Code can be enabled. The data is strobed by the IOI signal onto the S-Bus. From there it is transferred via the Arithmetic Logic (to alter or combine the data) and the T-Bus to the A- or B-Register. The particular register which will receive the data is determined by the LIA/B or MIA/B signal present at the register input gate.

2-11. Another driving signal from the Control Logic, the IOO (I/O Output) signal, strobes all interface cards to output data as a result of an OTA (Output from A) or an OTB (Output from B) instruction. The Select Code from the T-Register via the I/O Address card permits the IOO signal to strobe the data on the R-Bus into the appropriate interface card and external device. (The data was placed on the R-Bus from the A- or B-Register as a result of the OTA/B instruction.

2-12. INTERRUPT REQUESTS.

2-13. If a specific instruction to the I/O Control card has at some previous time enabled the interrupt system, an external device may request an interrupt to the computer program to obtain new data from the Computer or to feed new data to the Computer. This interrupt request is received by the I/O Control card. The I/O Control card signal to the I/O Address card causes it to interrupt the computer program by forcing the M-Register to be set (via the T-Bus) to a memory location corresponding to the Select Code of the interrupting device. This occurs during the Interrupt phase (Phase 4) machine cycle. The Fetch phase is then entered to make the Computer execute the instruction contained in the specified memory location. Generally, this instruction will be a jump to a service subroutine which will prepare or accept the new data. On completion of service, the subroutine must cause a return to the proper location in the main program. Refer to Paragraphs 2-28 through 2-53 for more detailed information on the interrupt system.

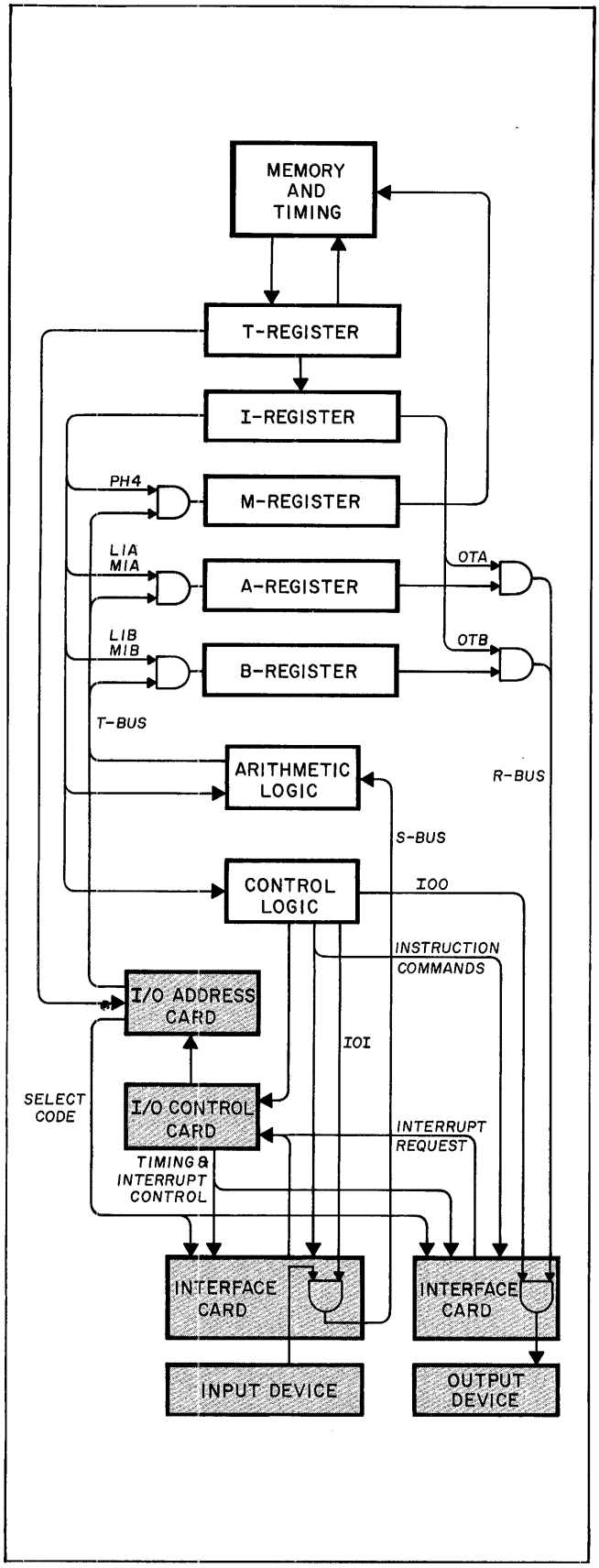


Figure 2-2. Block Diagram of System Input/Output Operations

2-14. INPUT/OUTPUT SYSTEM CARDS.

2-15. I/O CONTROL AND I/O ADDRESS CARDS.

2-16. The Computer contains one plug-in I/O Control card and one plug-in I/O Address card. The cards plug into the Computer, adjacent to the interface cards as shown in Figure 2-3. Each card contains extractor handles to aid in their removal from the Computer. The I/O Control card contains the master Interrupt System Enable flip-flop, receives command and timing signals from the Computer for transfer to the interface card slots, and provides the necessary gates and flip-flops for proper control of interface-card operation. For detailed information on the I/O Control card, refer to Section III of this manual. The I/O Address card provides a decoding function for program selection of the desired interface card and an encoding function for interface card interrupt identification. For detailed information on the I/O Address card, refer to Section IV of this manual.

NOTE

Possible damage to the I/O Control card or the I/O Address card may result if either one of these cards is inserted in an incorrect slot.

2-17. RESISTANCE LOAD CARD.

2-18. The Computer contains one plug-in Resistance Load card. The card provides 18 150-ohm resistors, connected to the -2 volt supply, to terminate the IOBO (I/O Bus Output) lines from the Computer to the interface cards. The card plugs into any of the input/output slots (Figure 2-3) of the Computer. The card remains in an I/O slot unless the total interface and Priority Jumper cards used in the system equal 16. At that time, the card is no longer required and must be removed. Extractor handles on the card aid in its removal. Refer to Section V for further information on the Resistance Load card.

2-19. INTERFACE CARDS.

2-20. PURPOSE. The interface cards provide channels through which data is transferred between the Computer and the input/output devices, and provide control (via computer commands) of the input/output device operation. An interface card may contain up to 16 or more buffer flip-flops for temporary storage of data to be transferred to the Computer or the input/output device. The number of buffer flip-flops on a particular interface card depends on the type of device connected to it. Other logic circuitry on the interface card also depends on the device to which it is connected. Certain devices are capable of interrupting the computer program while for others, this capability is not necessary; certain devices require control signals for movement of tape, etc., while others do not, and timing requirements for some devices must be provided on the interface card. For detailed information on a particular interface card, refer to the applicable Interface Kit Operating manual. In some cases, more than one interface card is required for an external device.

POSITION	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222
	I/O CONTROL CARD	I/O ADDRESS CARD	← INTERFACE CARDS → HIGH-SPEED PHOTO READER	HIGH-SPEED TAPE PUNCH	TELEPRINTER INPUT AND OUTPUT	PRIORITY JUMPER CARD												(RESISTANCE LOAD CARD)	I/O EXTENDER DRIVER	I/O EXTENDER DRIVER		
SELECT CODES																						
LOWER SELECT CODE (HIGH PRIORITY)			10	11	12	13	14	15	16	17	20	21	22	23	24	25	26	27	-	-	-	
HIGHER SELECT CODE (LOW PRIORITY)			11	12	13	14	15	16	17	20	21	22	23	24	25	26	27	30	-	-	-	

Figure 2-3. Computer Plug-In Card Positions, Front View

2-21. LOGIC ELEMENTS. Logic elements on the interface cards are provided by microcircuit packages which may contain more than one logic element and which are in numbered locations on the interface cards. The microcircuit package reference designations on the logic diagrams are preceded by MC. The number following MC corresponds to the numbered location of the package on the particular interface card. The individual elements of a package are further identified by a suffix letter. The Appendix in Volume Two provides logic diagrams for each of the microcircuit packages according to HP Part Number which is stamped on the microcircuit package.

2-22. PIN ASSIGNMENTS. Refer to Figure 2-4. One end of each interface card has 86 printed-circuit paths, 43 on each side of the card. This end of the card plugs into a computer slot connector to transfer signals to and from the Computer. It is also keyed to prevent incorrect insertion. The circuit path positions correspond to the pin positions of the slot connector. Odd-numbered pins 1 through 85 are on one side of the card as shown in Figure 2-4, and even-numbered pins 2 through 86 are on the other side of the card. Pins 1 and 2 are directly opposite each other on the card. Pin assignments for this end of the card are identical for all interface cards to permit the placement of any card in any of the input/output slots of the Computer.

2-23. The other end of most interface cards have 48 printed-circuit paths, 24 on each side of the card. The plug connector of the interconnecting cable to the input/output device plugs into this end of the card to transfer signals to and from the device. The circuit-path positions correspond to the pin positions of the plug connector. Pins 1 through 24 are on one side of the card as shown in Figure 2-4, and consecutively-lettered pins A through BB (with letters G, I, O and Q deleted) are on the other side of the card. Pins 1 and A are directly opposite each other on the card. Also on this end of the card are two extractor handles to aid in the removal of the card from the Computer.

2-24. Refer to Table 2-1 for a list of the pin connections and signals between the interface cards and the slot connectors. Although this table lists all of the pin assignments and signals between the cards and the slot connectors, an individual interface card may not necessarily use all signals. Pin assignments and signals between an interface card and its input/output device is provided in each Interface Kit section of this manual.

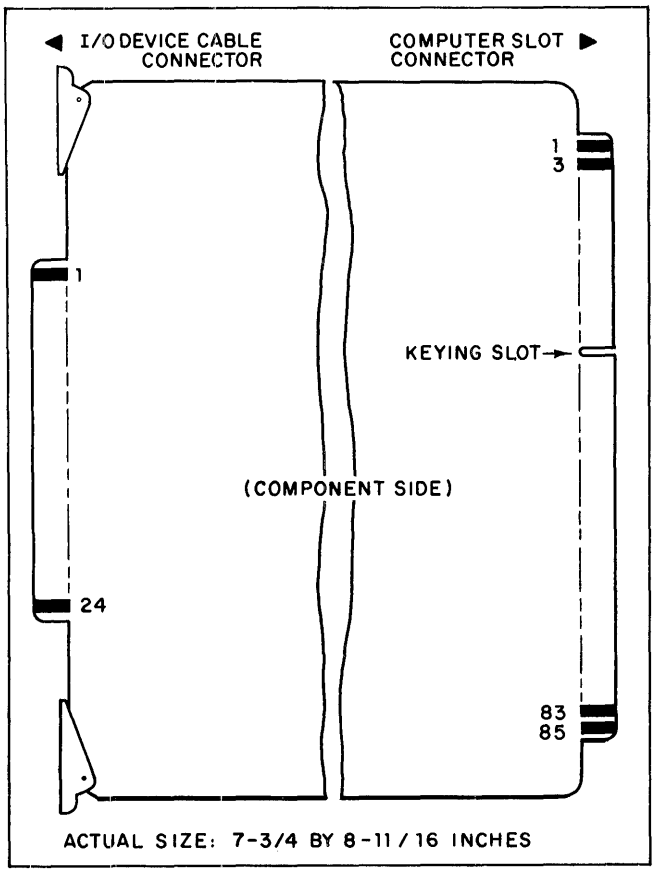


Figure 2-4. Interface Card Connectors

2-25. INPUT/OUTPUT DEVICE SELECTION.

2-26. Bits 0 through 5 of the Input/Output instruction form a Select Code to specify one of 64 possible input/output devices or functions. The Select Code is applied to the I/O Address card. This card decodes the 6-bit code and provides a two-digit octal code output. This output is transferred to the interface-card slot of the selected input/output device to permit program control of the device. Table 2-2 lists the Select Codes and their assignments, and indicates the corresponding interrupt location (i.e., the memory location containing the instruction to be executed when an interrupt occurs). Select Code 00 is the access to the master Interrupt System Enable Flip-Flop on the I/O Control card. Codes 01 through 07 are reserved for processor input/output functions or options, as listed. Codes 10 through 67 (octal) are used for selection of the 48 possible input/output devices and functions, each capable of causing an interrupt when used with the appropriate Extender Module.

2-27. Figure 2-3 illustrates the slots in the Computer card cage which are for the plug-in interface cards associated with input/output operation. These slots are capable of accepting interface cards of two basic types. The first is the parallel data-transfer type interface card. This interface card transfers data information to and from the Computer in parallel groups of bits (8 or 16 bits at a time) and requires the use of only one of the two Select Codes assigned to each I/O slot. This is the type of interface card used with most HP Accessory Kits. The second of the two interface card-types is the serial data-transfer interface card. This card transfers data information to and from the Computer in serial (one bit at a time) and normally requires that both of the Select Codes assigned to each I/O slot be used in order to control input and output functions. When a serial-type interface card is used, the I/O slot directly adjacent to it must contain a Priority Jumper card in order to maintain the priority continuity of the interrupt system. Since the I/O slot connector-wiring (on the Computer backplane) determines the Select Codes of each I/O slot, and interface cards can be inserted into any slot, each interface card assumes the two Select Codes of the slot into which it has been placed.

2-28. INTERRUPT SYSTEM.

2-29. The Interrupt System provides the means for an external device to interrupt the program in progress when data is available or when additional output data can be accepted. Figure 2-5 illustrates the relationship between the Computer, the I/O Control and I/O Address plug-in cards, and typical interrupt logic on a particular interface card; Figure 2-5 is for interrupt-logic explanatory purposes only. Refer to Figure 2-6 for a chart of typical interrupt system timing.

2-30. An interrupt request from an external device occurs when the following conditions are met:

a. The Interrupt System is enabled.

b. The Flag flip-flop of the specific device interface card is set.

c. The Control flip-flop of the specific device interface card is set.

d. No priority-affecting instruction (STF, CLF, STC and CLC), JSB,I instruction or JMP,I instruction is in progress.

e. No higher-priority devices satisfy the conditions of steps "b" and "c".

2-31. INTERRUPT SYSTEM ENABLE-DISABLE.

2-32. The computer program determines if interrupt requests from the external devices will be recognized. This is accomplished by enabling or disabling the Interrupt System Enable flip-flop on the I/O Control card. A set Flag (STF) instruction with a Select Code of 00 (octal) sets the FF and enables the interrupt system. A Clear Flag (CLF) instruction with a Select Code of 00 (octal) resets the flip-flop and disables the interrupt system.

2-33. When Computer power is initially turned on, pressing the POWER pushbutton automatically resets the Interrupt System Enable flip-flop, disabling the interrupt system. Initial turn-on also resets all Control flip-flops on the interface cards to prevent input/output devices from running when power is applied, and sets all Flag Buffer and Flag flip-flops on the interface cards. Therefore, to operate any device, it is first necessary to set the Interrupt System Enable flip-flop, reset the individual Flag Buffer and Flag flip-flops, and set the individual Control flip-flop.

Table 2-1. Interface Card-to-Computer Pin Connections

PIN	SIGNAL	PIN	SIGNAL
1	Ground	2	Ground
3	PRL: Priority Low	4	FLGL: Flag signal, Lower Select Code
5	SFC: Skip Flag Clear (Skip next instruction if Flag FF is reset)	6	IRQL: Interrupt Request, Lower Select Code
7	CLF: Clear (reset) Flag FF	8	IEN: Interrupt Enable
9	STF: Set Flag FF	10	IAK: Interrupt Acknowledge
11	T3(B): Machine phase time T3 (Buffered)	12	SKF: Skip Flag (Skip next instruction if SFS or SFC test is true)
13	CRS: Control Reset	14	LSCM: Lower Select Code Most Significant Digit
15	IOG(B): I/O Group instruction (Buffered)	16	LSCL: Lower Select Code Least Significant Digit
17	POPIO(B): Power On Preset I/O (Buffered)	18	IOBI 16: I/O Bus Input, Bit 16
19	SRQ: Service Request	20	IOO: I/O Output
21	CLC: Clear (reset) Control FF	22	STC: Set Control FF
23	PRH: Priority High	24	IOI: I/O Input
25	SFS: Skip Flag Set (Skip next instruction if Flag FF is set)	26	IOBI 0: I/O Bus Input, Bit 0
27	IOBI 8: I/O Bus Input, Bit 8	28	IOBI 9: I/O Bus Input, Bit 9
29	IOBI 1: I/O Bus Input, Bit 1	30	IOBI 2: I/O Bus Input, Bit 2
31	IOBI 10: I/O Bus Input, Bit 10	32	SIR: Set Interrupt Request
33	IRQH: Interrupt Request, Higher Select Code	34	HSCL: Higher Select Code Least Significant Digit
35	IOBO 0: I/O Bus Output, Bit 0	36	+30 volts, unregulated
37	HSCM: Higher Select Code Most Significant Digit	38	IOBO 1: I/O Bus Output, Bit 1
39	+4.5 volts	40	+4.5 volts
41	IOBO 2: I/O Bus Output, Bit 2	42	IOBO 4: I/O Bus Output, Bit 4
43	+12 volts	44	+12 volts
45	IOBO 3: I/O Bus Output, Bit 3	46	ENF: Enable Flag
47	-2 volts	48	-2 volts
49	FLGH: Flag signal, Higher Select Code	50	RUN
51	IOBO 5: I/O Bus Output, Bit 5	52	IOBO 7: I/O Bus Output, Bit 7
53	IOBO 6: I/O Bus Output, Bit 6	54	IOBO 8: I/O Bus Output, Bit 8
55	IOBO 11: I/O Bus Output, Bit 11	56	IOBO 9: I/O Bus Output, Bit 9
57	IOBO 12: I/O Bus Output, Bit 12	58	IOBO 10: I/O Bus Output, Bit 10
59	LDS: Load Switch	60	IOBI 11: I/O Bus Input, Bit 11
61	IOBO 13: I/O Bus Output, Bit 13	62	(Not Used)
63	(Not Used)	64	IOBI 3: I/O Bus Input, Bit 3
65	IOBO 14: I/O Bus Output, Bit 14	66	(Not Used)
67	(Not Used)	68	(Not Used)
69	-12 volts	70	-12 volts
71	(Not Used)	72	(Not Used)
73	IOBO 16: I/O Bus Output, Bit 16	74	IOBO 15: I/O Bus Output, Bit 15
75	(Not Used)	76	(Not Used)
77	IOBI 4: I/O Bus Input, Bit 4	78	IOBI 12: I/O Bus Input, Bit 12
79	IOBI 13: I/O Bus Input, Bit 13	80	IOBI 5: I/O Bus Input, Bit 5
81	IOBI 6: I/O Bus Input, Bit 6	82	IOBI 14: I/O Bus Input, Bit 14
83	IOBI 15: I/O Bus Input, Bit 15	84	IOBI 7: I/O Bus Input, Bit 7
85	Ground	86	Ground

NOTE: Pins 1 & 2, 39 & 40, 43 & 44, 47 & 48, 69 & 70, and 85 & 86 connected together on Slot Connector and on Interface Card.

2-34. INTERRUPT SYSTEM OPERATION.

2-35. When the external device has completed its operation, it generates a Device Flag signal to the Interface-card Flag Generator which sets the Flag Buffer flip-flop (see Figure 2-5). The output of the Flag Buffer flip-flop, in conjunction with the ENF (Enable Flag) signal from the I/O Control card during time T2 (Figure 2-6) causes "and" gate A to set the Flag flip-flop. The Flag flip-flop output is "anded" at gate B with the output of "nand" gate C. The gate C output is true when the Control flip-flop is set and when the IEN (Interrupt Enable) signal is received from the I/O Control card during time T3. Unless the Control flip-flop is set by a Set Control (STC) instruction, an interrupt request cannot occur.

Table 2-2. Select Code Assignments

SELECT CODE (OCTAL)	INTERRUPT LOCATION	ASSIGNMENT
00	None	Interrupt System Disable/Enable
01	None	Switch Register or Overflow
02	None	DMA Channel 1 Initialize
03	None	DMA Channel 2 Initialize
04	00004	Power Fail Interrupt/Central Interrupt Load
05	00005	Memory Protect/Parity Error Interrupt
06	00006	DMA Channel 1 Completion Interrupt
07	00007	DMA Channel 2 Completion Interrupt
10	00010	I/O Device, Highest Priority
thru	thru	thru
67	00067	I/O Device, Lowest Priority
70	00070	
thru	thru	Not wired in the HP 2150B Extender
77	00077	

2-36. The Control flip-flop is set under program control and therefore, is set at T4 time of a machine cycle. The STC instruction is enabled to the Control flip-flop by the SCM (Select Code Most Significant digit) and SCL (Select Code Least Significant digit) signals from the I/O Address card, and the IOG(B) (I/O Group instruction, Buffered) signal from the I/O Control card. The SCM and SCL signals are enabled on the individual interface card by the IOG(B) signal which occurs when the instruction to be performed is an I/O Group instruction. When the Control flip-flop sets, a true input is applied to "and" gate C. The inputs to "and" gates B and C are then true and gate B applies a true output to inverting "or" gate D. The false output of gate D disables "and" gate E, making the priority network bus to the lower-priority devices false. This prevents any device of lower priority from requesting an interrupt.

2-37. At the same time that gate B applied a true signal to gate D, it also applied the same true signal to "and" gate F. The priority network signal to gate F will be true if an interface card (device) of higher priority than the one represented in Figure 2-5 is not requesting an interrupt. In this case, the true output of gate F is combined with the SIR (Set Interrupt Request) signal from the I/O Control card at time T5 and the output of the set Flag Buffer flip-flop to provide a true output from "and" gate G. The gate G output sets the IRQ (Interrupt Request) flip-flop.

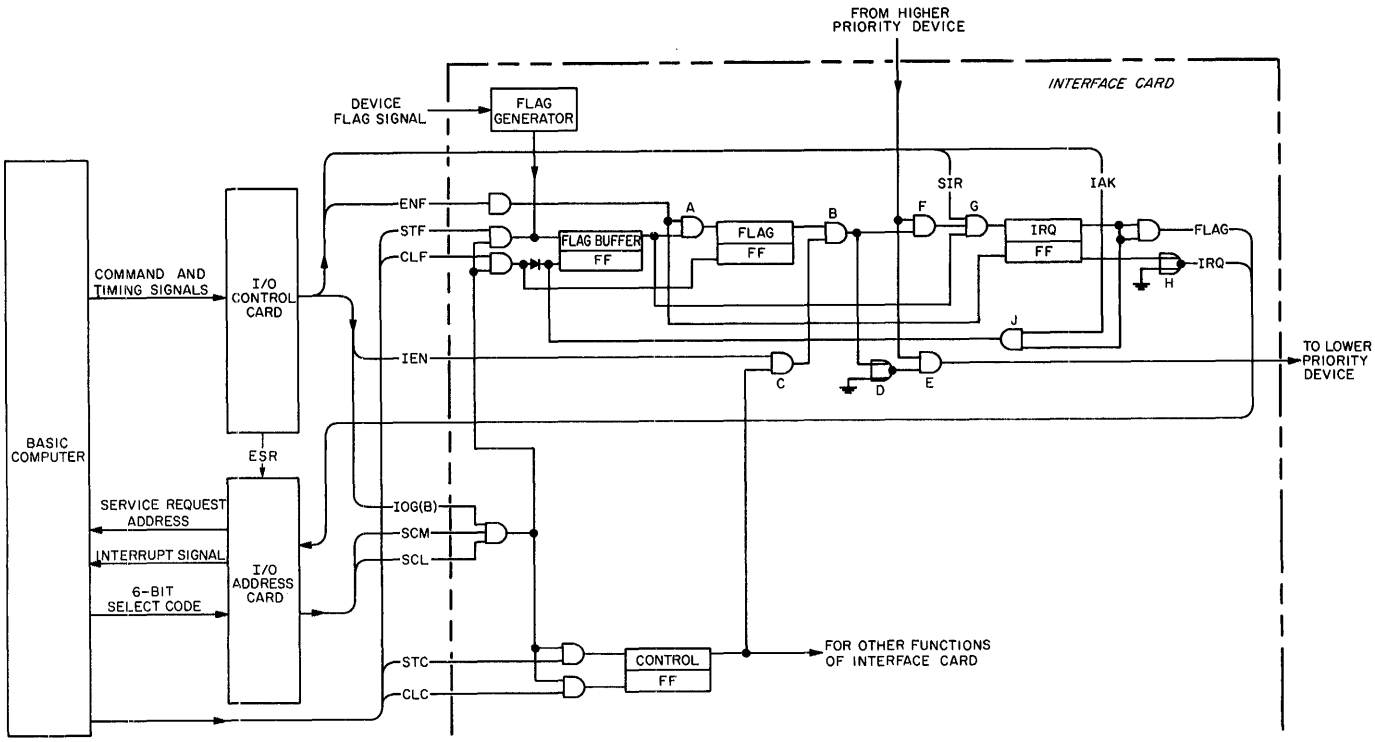


Figure 2-5. Typical Interrupt Logic

2-38. The IRQ flip-flop outputs provide the Flag signal and the IRQ signal to the I/O Address card. (The IRQ signal is obtained by the inversion of the false reset-side output of the IRQ flip-flop by inverting "or" gate H.) The Flag signal is "anded" in the I/O Address card with the Enable Service Request (ESR) signal from the I/O Control card to form an interrupt signal. However, the ESR signal is false for the remainder of the machine cycle during which an instruction occurs that affects device priorities (STC in Figure 2-6) as determined by the I/O Control card. At time T2, the IRQ flip-flop is reset by the ENF signal to allow a higher-priority device to request an interrupt. If the Control flip-flop is still set and no higher-priority devices have requested an interrupt, the IRQ flip-flop will again be set at time T5 (SIR). The Flag and IRQ signals are again sent to the I/O Address card. The signals are used to form a 6-bit Service Request Address which is enabled to the Computer at time T7 of the Interrupt Phase. The Flag signal and the now-true ESR signal cause the Interrupt signal (INT) to be sent to the Computer. This signal causes an interrupt at the end of the current machine phase, switching the Computer into the Interrupt Phase, except when any of the following conditions occur:

a. The Computer is in the HALT mode.

b. A Jump Indirect (JMP,I) or a Jump to Subroutine Indirect (JSB,I) instruction is not fully executed. (These instructions inhibit all interrupts until fully executed for any number of indirect levels of addressing. At the earliest, an interrupt request will be granted at the end of the machine phase immediately following one or more JMP,I or JSB,I instructions.)

c. Direct Memory Access (DMA) option is in process of transferring data. Exception: The Power Fail Interrupt can interrupt a DMA transfer.

d. A STC, CLC, STF or CLF machine cycle is being executed.

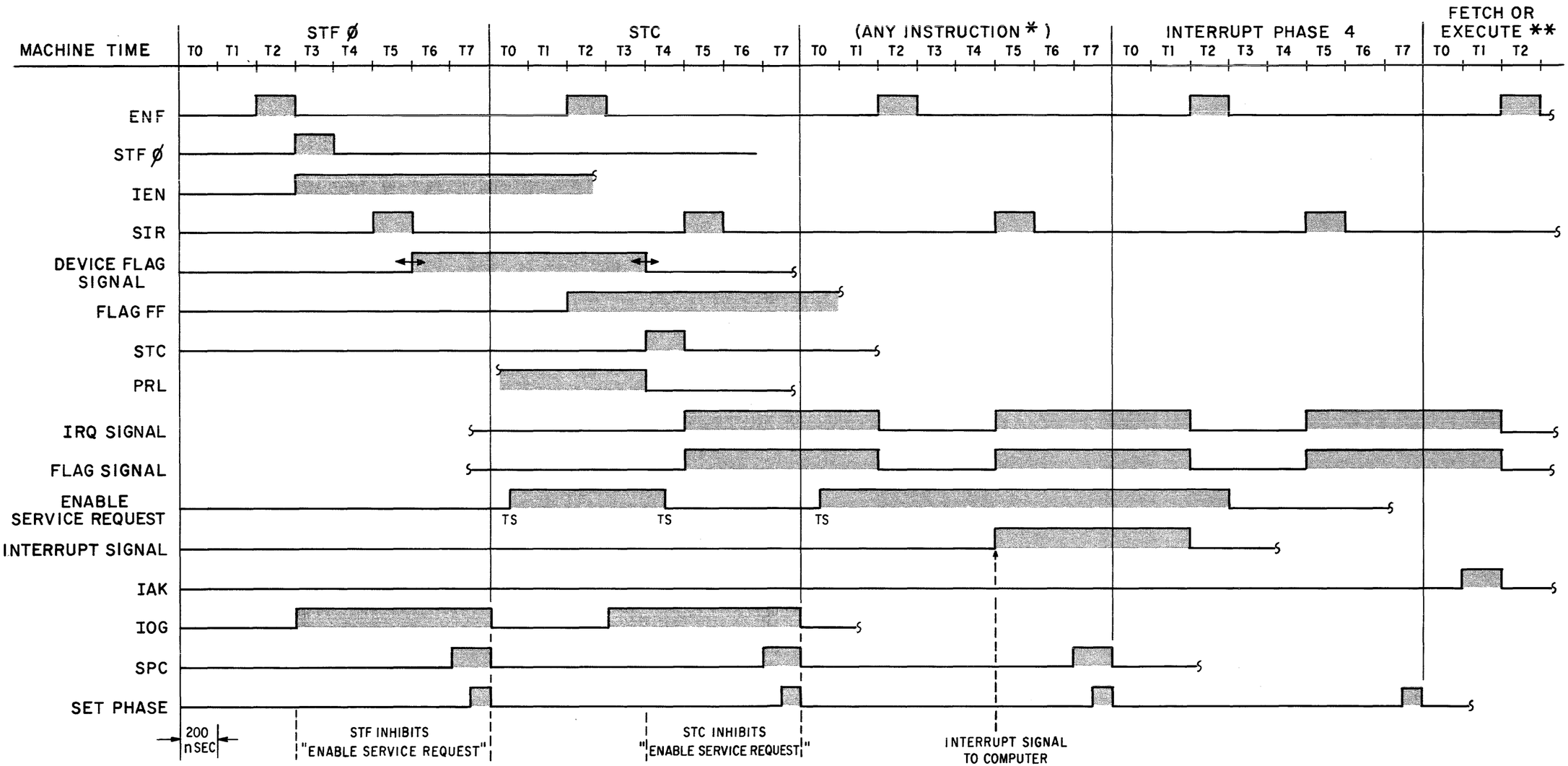
2-39. INTERRUPT PROCESSING.

2-40. During the Interrupt Phase, the Computer decrements the P-Register by one to ensure that the proper location in the main program will be returned to after the interrupt is processed. Also, the Computer places the Service Request Address (which is always equal to the Select Code of the interrupting device) from the I/O Address card into the M-Register at time T7. This causes the next instruction to be read from the memory location having the same number as the Service Request Address (Select Code) during the Fetch phase (Phase 1). This location in memory is referred to as the "interrupt location" and is reserved for that particular device. Example: A device specified by a Select Code of 10 will interrupt to (i.e., cause execution of the contents of) memory location 00010. At time T3 of Phase 4, the interrupt system is inhibited by the false Enable Service Request signal until the Fetch phase following the execution of the instruction at the interrupt location. This prevents interrupts from occurring until at least one instruction has been executed (except in the case of JMP,I and JSB,I instructions), which may be more than one instruction.

2-41. At time T1 of Phase 1 the IAK (Interrupt Acknowledge) signal from the I/O Control card and the set-side output of the IRQ flip-flop resets the Flag Buffer flip-flop through "and" gate J (Figure 2-5). Since the set-side output of the Flag Buffer flip-flop is applied to "and" gate G, resetting the flip-flop prevents the setting of the IRQ flip-flop and causing another interrupt from the same Flag signal at time T5 of Phase 1 when the SIR signal is again applied to gate G. (The Flag Buffer flip-flop can also be reset by a programmed CLF (Clear Flag) instruction.) During time T2, the ENF signal resets the IRQ flip-flop. The Computer fetches the instruction in the interrupt location which will usually be a jump to a subroutine (JSB) instruction. The contents of the P-Register plus one is stored in the first location (X) of the subroutine. (Since the previous contents of the first memory location are destroyed when P+1 is stored, the first instruction of the subroutine should always be a no-operation (NOP) instruction or equivalent.) The location of the subroutine (X+1) is placed in the P- and M-Registers, and the Computer resumes normal subroutine operation. Thus, the instruction at location X+1 is the first instruction of the subroutine to be executed. The contents of the working registers that were in use in the main program should be stored when entering the subroutine and restored before exit from the subroutine. The exit from the subroutine is made with a JMP,I to location X. This places the address of the interrupted program instruction in the P- and M-Registers and normal program operation resumes.

2-42. INTERRUPT PRIORITY.

2-43. PRIORITY ASSIGNMENTS. A priority network on the I/O slots allows only one external device at a time to interrupt the computer program regardless of the number of devices requesting an interrupt. The priority network gives highest priority to Select Code 04, reserved for Power Fail Interrupt, and decreasing priority to the remaining Select Codes in order from 05 to 67 (see Table 2-2). (See Figure 2-8, INTERRUPT PRIORITY CONTINUITY.) Select Code 05 is reserved for both the Memory Protect and Parity Error options. Either one, or both, of these options may be used but they always share the same Select Code of 05. When neither one of these two options (Memory Protect or Parity Error) is installed, jumper W3 on the I/O Control card (slot 201 of the computer card cage) must be installed in order to maintain priority continuity (see Figure 2-8). Select Codes 06 and 07 are reserved for the DMA (Direct Memory Access) option Channel 1 and Channel 2, respectively. When the DMA option is installed, jumper W2 on the I/O Control card must be removed. The DMI (Direct Memory Increment) option may be used in place of the DMA option Channel 1 and utilizes Select Code 06 only (see Figure 2-8). When the DMI option is installed, jumper W1 on the I/O Control card must be removed. All I/O slots from Select Code 10 ascending thru 67 may be used for I/O devices as desired by the computer user. The interrupt priority assignments of the I/O slots remain fixed but since any interface card can be inserted into any I/O slot, the interrupt priority of a given device can be easily changed by inserting the device interface card into another I/O slot.



NOTES:

* EXCEPT STF, CLF, STC, CLC, JMP I, AND JSB I.
** EXECUTE IF A SINGLE CYCLE INSTRUCTION.

Figure 2-6. Typical Interrupt System Timing

2-44. PRIORITY NETWORK OPERATION. As shown in Figure 2-7, priority is established by a hardware-implemented priority chain. The "and-or" gates illustrated in Figure 2-7 are identified by letters and correspond to those used in Figure 2-5. The true-false logic levels for an interface card which is not requesting an interrupt are illustrated on the first interface card (Select Code 11) with the Interrupt System enabled (IEN input is true). Also, the PRH (Priority High) signal is true, indicating that a device of higher priority is not requesting an interrupt. In this case, the "chain" is not broken and a true PRL (Priority Low) signal is available to the next interface card (Select Code 12) as a true PRH signal to that card.

2-45. If the output logic portion of the interface card with Select Code 12 in Figure 2-7 requests an interrupt, all inputs to "and" gate B will be true. Inverting "or" gate D will then apply a false input to "and" gate E. The output of gate E is then false, breaking the "chain", and preventing any interface card of lower priority from interrupting the computer program. A service subroutine can then be entered to process the interrupt of the output logic.

2-46. A service subroutine of any device can be interrupted by a higher-priority device; then after the higher-priority interrupt subroutine is completed, the lower-priority subroutine may continue. In this way, several service subroutines may be in a state of interruption at one time. Each will be permitted to continue when the next higher priority subroutine is completed.

2-47. Interrupt priority can also be program controlled. Since an interrupt cannot occur unless the Control flip-flop of the interface card is set, all Control flip-flops on interface cards of higher priority than the one desired can be reset by a Clear Control (CLC) instruction. This prevents those interface cards from requesting an interrupt and establishes the desired device as the highest-priority device.

2-48. INTERRUPT PRIORITY CONTINUITY.

2-49. Figure 2-8 illustrates the continuity of the interrupt priority network for all possible input/output interface cards and processor option cards capable of interrupting the Computer.

2-50. Since the Power Fail Interrupt (Select Code 04) is assigned the highest priority, it can interrupt the Computer (as also can the Memory Protect/Parity Error and the Direct Memory Increment options) regardless of the state of the Interrupt System Enable flip-flop. For all other interface cards and options, the flip-flop must be set before an interrupt can occur. When an interface card requests an interrupt, its false PRL signal is applied to the next interface card as a false PRH signal to prevent it from requesting an interrupt. This sequence continues from card to card until the last interface card receives a false PRH signal. When an interrupt request occurs, the PRL-PRH switching sequence proceeds to the next card and also to the "and" gate following the group of eight cards in which the interrupt request occurs. The false input to the "and" gate causes a false IEN output and all following interface cards are quickly disabled.

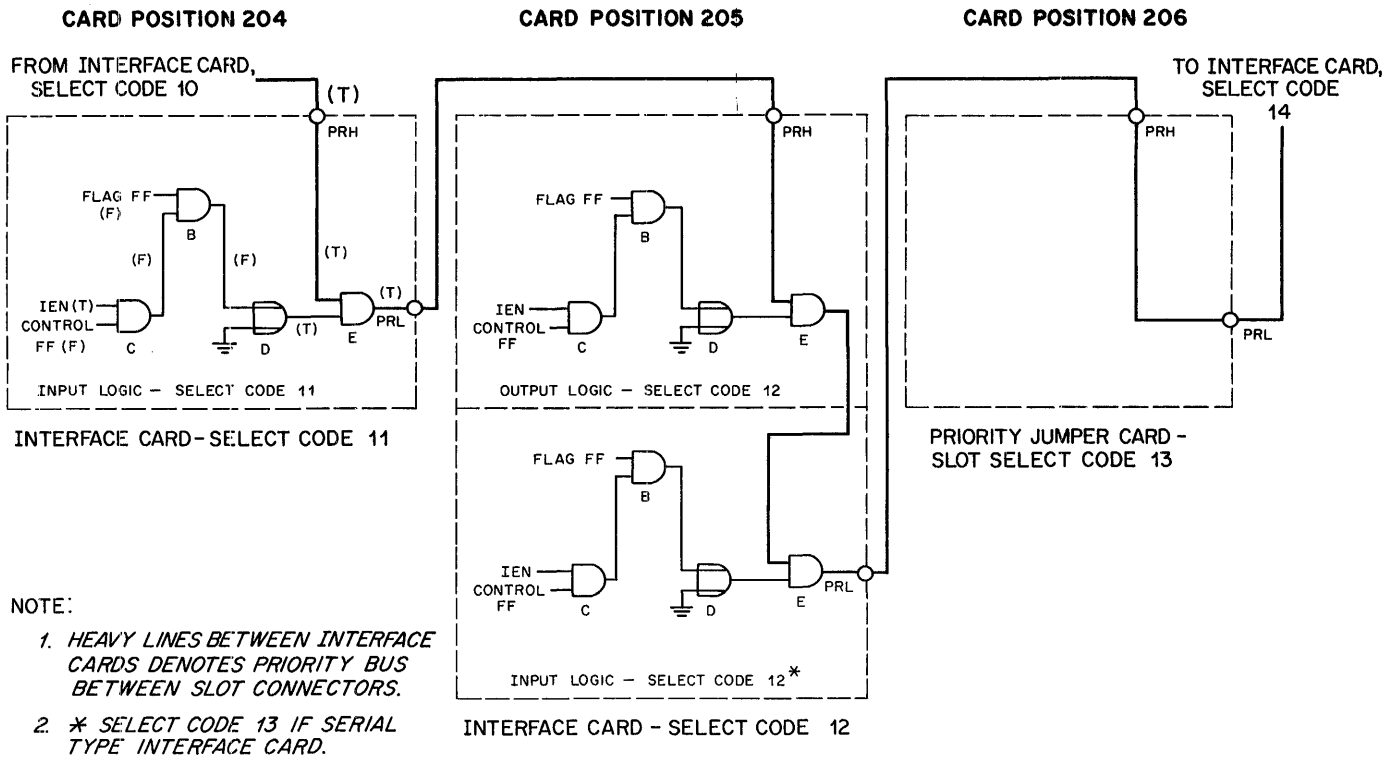


Figure 2-7. Interrupt Priority

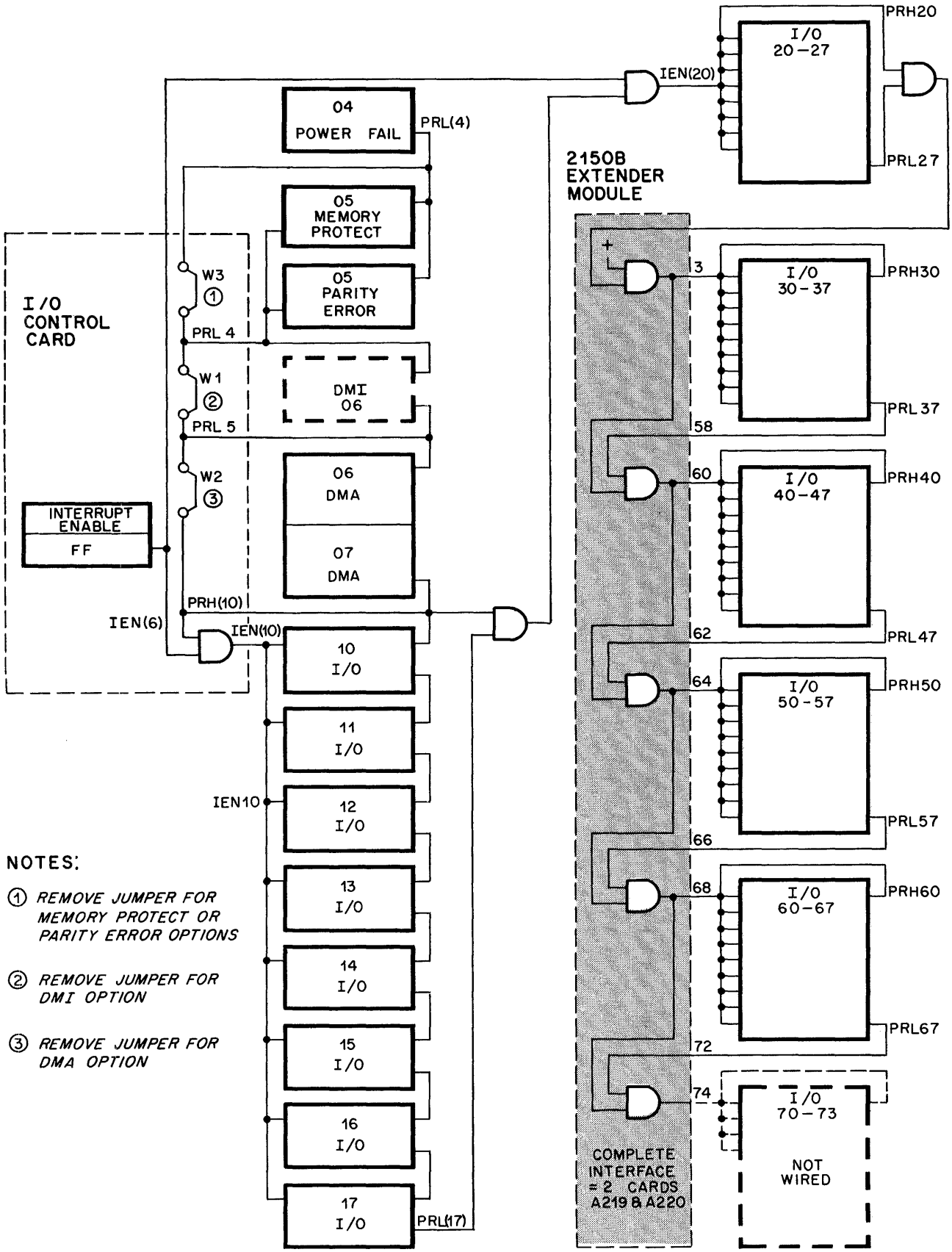


Figure 2-8. Priority Continuity

2-51. The Memory Protect and Parity Error options share Select Code 05 as they are connected in parallel in the interrupt priority chain (see Figure 2-8). If either one of these options is installed in the Computer, Select Code 05 is operative. If either of the options is installed, it is necessary to remove jumper W3 on the I/O Control card (Figure 2-8) in order to maintain interrupt priority continuity.

2-52. EXTENDER MODULES.

2-53. To increase the number of I/O Channels from 16 or to extend the computer memory from 16K (16,384 words), it is necessary to use one of two available extender modules. The HP 2151A Extender Module provides an additional 16 slots of I/O only and requires the HP 12596A Interface Kit, in order to be used with the HP 2116B Computer. It is easily installed by the use of interconnecting cabling and contains its own internal power supply. The HP 2150B Extender Module provides the Computer with the capability for an additional 32 slots of I/O and an additional 8K or 16K of memory and also contains its own internal power supply. The additional capabilities provided by the HP 2150B Extender Module are dependent upon which of several extender options are incorporated within the basic extender module unit. The options are as follows:

a. Option 01: This option comprises four plug-in cards and two interconnecting cables which are required for the operation of the interface cards (up to 32) added to the extender module.

b. Option 02: This option comprises an 8K memory module, a set of plug-in memory addressing cards, and two interconnecting cables. When combined with the 16K memory in the basic computer, this option gives a combined memory size of 24K (24,576 words).

c. Option 03: This option comprises a second 8K memory module, and set of memory addressing cards in addition to the 8K of Option 02. With Options 02 and 03 installed, the HP 2116B Computer and HP 2150B Extender Module combined provide the computer user with 32K (32,768 words) of memory.

2-54. POWER SUPPLY REQUIREMENTS.

2-55. When using certain combinations of I/O devices which have high current requirements, the Computer internal power supply may be inadequate. In order to furnish the necessary additional power, a HP 2160A Power Supply Extender must be used. The HP 2160A Power Supply Extender is a physically self-contained unit that is connected to the HP 2116B Computer by the use of two interconnecting cables. When connected, the power supply extender is a slaved extension of the computer power supply and provides an additional 20 amperes at +4.5V and 10 amperes at -2V. If desired, the power supply extender may be mounted in a standard 19-inch vertical mounting rack.

2-56. Table 2-3 lists the current available from the Computer power supply and from the combination of Computer power supply and HP 2160A Power Supply. The current available for options in Table 2-3 is

Table 2-3. Internal/External Power Supply Requirements

REQUIREMENTS	SUPPLY CURRENTS (AMP)			
	+12V	-12V	-2V	+4.5V
CURRENT AVAILABLE FROM POWER SUPPLIES				
Computer Power Supply	3	3	22.5	*22.5
Computer and HP 2160A Power Supplies	3	3	32.5	**32.5
CURRENT REQUIRED BY COMPUTER WITH NO PROCESSOR OR INPUT/OUTPUT OPTIONS				
Computer with 8K Memory	540 ma	600 ma	15.2	26.4
Computer with 16K Memory	1.0	1.1	15.7	28.4
CURRENT AVAILABLE FOR OPTIONS				
Computer with 8K Memory	2.5	2.4	7.3	***11.3
Computer with 16K Memory	2.0	1.9	6.8	*** 9.8
Computer with 8K Memory and HP 2160A Power Supply Extender	2.5	2.4	17.3	***21.3
Computer with 16K Memory and HP 2160A Power Supply Extender	2.0	1.9	16.8	***19.8

NOTES:
* Plus the current drawn from the -2V supply by the Computer with memory and options. Maximum available from +4.5V supply is 45 amperes.

** Plus the current drawn from the -2V supply by the Computer with memory and options. Maximum available from +4.5V supply is 65 amperes.

*** Plus the current drawn from the -2V supply by the selected options.

obtained by subtracting the current required by the Computer from the current available from the power supplies. Table 2-4 lists the current required by the processor and input/output options. To determine if the Computer power supply is adequate for the options to be used with the Computer or if a HP 2160A Power Supply must be added, proceed as follows:

a. Refer to Table 2-4 and add the currents required in each of the +12V, -12V, -2V, and +4.5V columns for the selected options.

b. Add the sum of the -2V supply currents obtained in step "a" to the value in the +4.5V column of Table 2-3 for a Computer with an 8K or 16K memory (as applicable) under the CURRENT AVAILABLE FOR OPTIONS title. Record this new sum.

c. Again refer to the currents listed for a Computer with 8K or 16K of memory (as applicable) under the CURRENT AVAILABLE FOR OPTIONS title in Table 2-3. If any of the individual +12V, -12V, or -2V supply current sums of step "a" are higher than those listed, or if the +4.5V supply current sum is higher than that recorded in step "b", an HP 2160A Power Supply is required. The current sums cannot then exceed those listed for a Computer with an 8K or 16K memory (as applicable) and an HP 2160A Power Supply. The HP 2160A Power Supply provides only -2V and +4.5V and does not supply +12V or -12V.

2-57. INTERFACE KITS.

2-58. Interface Kits for the HP 2116B Computer system provide the necessary interface cards, priority jumper cards, and cable for connection of external equipment to the Computer. The necessary software for driving the specific peripheral device, and the device diagnostic-program tape are also provided. The kits are identified by a 5-digit accessory number, a suffix revision letter, and a functional name (e.g., 12531B Teleprinter Input/Output). Available interface kits, identified in this manner, are listed on the Accessory Kit Ordering Information sheet that accompanies each HP 2116B Computer Technical Data Sheet.

Table 2-4. Current Required by Options

OPTIONS		SUPPLY CURRENT REQUIRED (AMP)			
	PROCESSOR OPTIONS	+12V	-12V	-2V	+4.5V
12578A	Direct Memory Access	0.00	0.00	0.72	6.20
12579A	Extended Arithmetic Unit	0.00	0.00	3.30	4.68
12581A	Memory Protect	0.00	0.00	0.90	1.92
12582A	Direct Memory Increment	0.00	0.00	0.12	2.04
12588A	Power Fail with Auto Restart	0.06	0.04	0.00	0.00
12591A	Memory Parity Check	0.00	0.00	0.5	0.91
	INPUT/OUTPUT OPTIONS				
12531B	Teleprinter Input/Output, Buffered	0.05	0.10	0.05	0.76
12532A	High-Speed Punched Tape Input	0.03	0.01	0.48	1.10
12533A	Digital Voltmeter Program Output (2401C)	0.00	0.30	0.24	0.42
12535A	Crossbar Scanner Program Output	0.01	0.04	0.84	1.10
12536A	High-Speed Punched Tape Output	0.01	0.01	0.30	0.72
12537A	Incremental Magnetic Tape Output	0.00	0.06	0.48	0.90
12538A	Magnetic Tape Input/Output (7 Channel)	0.09	0.18	4.20	6.00
12539A	Time Base Generator	0.01	0.00	0.42	1.10
12540A	Data-Phone Interface (103A)	0.11	0.05	0.90	1.40
12541A 12543A	Digital Voltmeter Data Input (2401C and 3440A)	0.05	0.01	0.30	0.96
12544A	Counter/Thermometer Data Input (8 Digits)	0.05	0.01	0.30	0.96
12548A	Counter Data Input (4, 5, 6, & 7 Digits)	0.05	0.01	0.30	0.96
12550A	Digital Voltmeter Program Output (2411A)	0.00	0.06	0.30	0.42
12551A	Relay Output Register (no Interrupt)	0.24	0.00	0.39	0.60
12551B	Relay Output Register (with Interrupt)	0.18	0.02	0.90	0.08
12554A	Duplex General Purpose Register	0.24	0.01	0.48	2.40
12555A	Digital-to-Analog Converter	0.25	0.30	0.90	2.00
12556A	40-Bit Output Register	0.07	0.00	0.06	0.80
12559A	9 Channel Magnetic Tape Input/Output	0.18	0.18	0.24	2.58
12561A	Disc Memory Interface	0.00	0.00	0.24	2.40
12564A	10-Bit A-to-D Converter	0.15	0.22	0.09	0.90
12566A	Microcircuit Interface	0.00	0.00	0.05	1.10
12596A	HP 2151A I/O Extender Interface	0.00	0.00	3.00	0.80
12597A	8-Bit Duplex Register (Positive-True)	0.18	0.02	0.80	0.05
	8-Bit Duplex Register Option 2 (Negative-True)	0.04	0.18	0.80	0.06

SECTION III
I/O CONTROL CARD

3-1. INTRODUCTION.

3-2. This section provides theory of operation information for the I/O Control card (HP Part No. 02116-6041). The card is of standard interface-card size and plugs into Position 201 on the left side of the input/output slots of the Computer. The slot connector transfers signals to and from the card; no additional cabling is required. The card output signals are transferred to all interface cards in the Computer, in parallel, through the interface-card slot connectors. The main function of the I/O Control card is to control the interrupt system. Certain clock signals, reset signals, and selection of the Switch Register and the Overflow bit of the Computer are also provided by the I/O Control card.

3-3. THEORY OF OPERATION.

3-4. COMPUTER POWER-ON.

3-5. When power is initially applied, the Computer is set to the HALT mode of Phase 1. At this time, the POPIO signal (Figure 3-3) is received at pin 63 of the I/O Control card. This signal is present for 100 milliseconds. (With power on, pressing the Computer PRESET switch applies the POPIO signal to the I/O Control card for as long as the switch is pressed.) The POPIO signal occurs at time T5 of Phase 1. When the POPIO signal drops, the Computer is still in Phase 1 and the initial conditions have been established for proper interface card operation. The POPIO signal performs the following functions which are described in Paragraphs 3-6 through 3-9.

a. Disables the Interrupt System.

b. Provides a false Enable Service Request signal to the I/O Address card.

c. Sets the Flag Buffer and Flag flip-flops and resets the IRQ flip-flops on all interface cards.

d. Resets the Control flip-flop on all interface cards.

3-6. Disables the Interrupt System: The POPIO signal resets the Interrupt System Enable flip-flop (MC66) through diode CR1, disabling the interrupt system. (The flip-flop consists of two inverting "or" gates which are connected such that the flip-flop can be reset by a true signal to either the reset-side input of the reset-side output of the flip-flop.

NOTE

Table 3-1 lists the part numbers of the microcircuit packages identified in Figure 3-3 by reference designations preceded by MC. The Appendix in Volume Two contains logic diagrams of the microcircuit packages according to part number.

3-7. Provides a False Enable Service Request Signal: When the Interrupt System Enable flip-flop was reset, the true reset-side output of the flip-flop is applied to the input of inverting "or" gate MC27A through diode CR3. The output of gate MC27A is a false Enable Service Request signal to the I/O Address card. This prevents the I/O Address card from sending an Interrupt Signal to the Computer which would switch the Computer into the Interrupt Phase, Phase 4.

3-8. Sets the Flag Buffer and Flag Flip-Flops and Resets the IRQ (Interrupt Request) Flip-Flop: The POPIO signal forms the buffered POPIO signal (POPIO(B)), through "and" gate MC86A, to set the Flag Buffer flip-flop on all interface cards. At time T2, the T2 clock signal to the I/O Control card (through "and" gate MC87B) forms the ENF signal. This signal resets the IRQ flip-flop on the interface cards and, with the set Flag Buffer flip-flop output, sets the Flag flip-flop on all interface cards.

3-9. Resets the Control Flip-Flop: The POPIO signal forms the CRS signal through "and" gate MC87A, to reset the Control flip-flop on all interface cards and to reset the Interrupt Control flip-flop (MC26) through diode CR2 on the I/O Control card. (The CRS signal can also be programmed by a CLC instruction with a Select Code of 00 (octal); see Paragraph 3-20.) Resetting the Control flip-flops prevents an interrupt from occurring when the interrupt system is initially enabled (Interrupt System Enable flip-flop on the I/O Control card gets set). Resetting Interrupt Control flip-flop MC26 ensures a false Enable Service Request signal to the I/O Address card when the POPIO signal drops. This prevents an interrupt from occurring until after time T7 of the first machine phase after the POPIO signal drops to permit the execution of at least one program instruction. (The reset-side output of the Interrupt Control flip-flop enables "and" gate MC35B to form the IAK signal at time T1 of Phase 1; the IAK signal has no affect on the interface cards during the presence of the POPIO signal.)

3-10. SIR SIGNAL.

3-11. At each T5 clock time, the T5 signal is sent to the I/O Control card by the Computer (Figure 3-3). After being applied to gate MC57B, this signal is applied to all interface-card slot connectors as the SIR (Set Interrupt Request) signal. The SIR signal enables setting of the IRQ (Interrupt Request) flip-flop on all interface cards in order to provide Flag and IRQ signals to the I/O Address card during an interrupt request. This signal is also applied to the set input of the PH4/5 SYNC 2 flip-flop (MC56) on the I/O Control card causing the flip-flop to apply a true output signal to pin 6 of "and" gate MC47B. (For a detailed description of the PH4/5 SYNC 2 flip-flop circuit, refer to Paragraph 3-25, DMA Phase 5.)

3-12. PRIORITY-AFFECTING INSTRUCTIONS.

3-13. Four instructions, STC CLC, STF, and CLF, affect the priority structure of the input/output devices; whether a device can request an interrupt or not depends upon whether its interface-card Control flip-flop is set or reset (STC, CLC) or its Flag flip-flop is set or reset (STF, CLF). If an I/O device cannot request an interrupt, it is not recognized as being part of the interrupt priority structure. In this case, all succeeding I/O devices are effectively moved up the interrupt priority structure by one.

3-14. The four instructions also inhibit all interrupt during the machine phase in which they occur, plus one machine cycle, by removing the ESR (Enable Service Request) signal to the I/O Address card. This prevents interrupts during JMP, I and JSB, I instructions (during entry and exit from subroutines. Also, a combination of two of the four instructions are normally the next-to-last instruction in a service subroutine processing an interrupt (the last being a JMP, I instruction to cause return to the main program or to an address in another service subroutine). If another input/output device could interrupt immediately after execution of these instructions (and before the JMP, I instruction), the possibility would exist that the first device may interrupt a second time before the JMP, I instruction is performed. In this event, the first main-program address (or the other service-subroutine address) stored in the beginning of the service subroutine would be destroyed, preventing a return to the main program or to the other service subroutine.

3-15. (Refer to Figure 3-3). Whenever any of the four instructions are programmed, the STC, CLC, STF, and CLF signals are received by the I/O Control card and applied to one of the MC77A through MC77D isolator gates. The applicable gate output is then a true input to "and" gate MC37C. The MC37C gate output becomes true on receipt of clock signal TS (pin 27) and the IOG signal at time T3 plus 80 nanoseconds from "and" gate MC57A.

3-16. The IOG signal from the Computer is sent to the I/O Control card at time T3 of each machine phase that an I/O Group instruction is performed and is applied to one input of "and" gate MC57A. The other input to gate MC57A is the IOG signal which has been delayed by about 80 nanoseconds to eliminate any noise which may have been generated during its formation. (The delay is caused by inverting "or" gates MC55A and MC55B, resistor R3, and capacitor C3.) At the end of the delay, gate MC57A provides a true output to "and" gate MC37C and a buffered IOG signal to all interface card slots. The IOG(B) signal is an enabling signal for the I/O Group instruction and the Select Code transferred to the selected interface card.

3-17. The true output of gate MC37C is applied to "and" gate MC36B. The other input to gate MC36B is true due to the inversion of the false PH5 signal by inverting "or" gate MC27B. The true output of "and" gate MC36B resets the Interrupt Control flip-flop. The true reset-side output of the Interrupt Control flip-flop is applied to inverting "or" gate MC27A, removing the Enable Service Request signal to the I/O Address card. Interrupt signals will not now be enabled to the Computer for the remainder of the current machine phase.

3-18. At time T7 of the current machine phase, the STM signal sets Interrupt Timing flip-flop MC16. At time T0, TS of the next machine phase, true T0 and TS signals are applied to "and" gate MC36A. The true output of gate MC36A resets the Interrupt Timing flip-flop. The set-side output of this flip-flop is applied to the Interrupt Control flip-flop which is set at time T0, TS by the trailing (negative-going) edge of the pulse output of the Interrupt Timing flip-flop. The false reset-side output of the Interrupt Control flip-flop is inverted by inverting "or" gate MC27A, providing a true Enable Service Request input to the I/O Address card, and enabling Interrupt signals to the Computer.

3-19. RESETTING CONTROL FLIP-FLOPS.

3-20. The Control flip-flop on all interface cards can be reset by the CLC instruction with a Select Code of 00. The CLC signal enters the I/O Control card at pin 75 and is applied to "and" gate MC76B, as shown in Figure 3-2. The other input to gate MC76B is from the output of "and" gate MC67C. This gate output is true when Select Code 00 (octal) is received at pins 36 and 38, and the output of the IOG "and" gate MC57A is true. The true output of "and" gate MC76B then applies a CRS signal to all interface card slots via pin 65. The CRS signal resets the Control flip-flop on the interface cards to prevent an interrupt request from any input/output device.

3-21. PHASE OPERATION.

3-22. INTERRUPT PHASE 4. During Phase 4 (Interrupt Phase), the PH4 signal and the T3 clock signal are received by the I/O Control card as shown in Figure 3-3. The T3 signal, after passing through "and" gate MC35A, is applied to "and" gates MC37A and MC36C as the T3(B) (buffered time-T3) signal. It is also sent out of the I/O Control card at pin 81 to all I/O interface-card slot connectors. The PH4 input signal is also applied to "and" gates MC37A and MC36C. When the PH4 signal and the T3(B) signal are simultaneously applied to "and" gate MC37A as input signals, (during time T3 of a Phase 4), a true output signal from gate MC37A is applied to the Interrupt Control flip-flop (MC26) as a reset pulse. The resulting true reset-side output signal of the flip-flop is inverted by inverting "or" gate MC27A and sent to the I/O Address card as a false ESR (Enable Service Request) signal. This action inhibits the INT (Interrupt) signal to the Computer until after the program counter steps (time T7 of Fetch Phase 1). The PH4 and T3(B) signals are also simultaneously applied to "and" gate MC36C at time T3 of Phase 4. This causes "and" gate MC36C to apply a true output signal to the direct-set input of the PH4/5 SYNC 1 flip-flop (MC46) which then applies its set-side true output signal to "and" gate MC47B. This signal, when true, remains in a true state as an input to "and" gate MC47B until the PH4/5 SYNC 1 flip-flop is directly reset by the POPIO pulse or is clocked by the IAK (Interrupt Acknowledge) signal at time T1 of Fetch Phase 1.

3-23. PHASE 1 (FETCH). At time T2 of Phase 1 (Fetch Phase), directly following the Interrupt Phase, the PH1 signal and clock signal T1 are applied as inputs to "and" gate MC37B. The true output of gate MC37B supplies one input of "and" gate MC35B. The other input to gate MC35B is the true reset-side output of the Interrupt Control flip-flop. When both of these inputs are true, gate MC35B sends its true output signal out of the I/O Control card to all interface-card slots as the IAK (Interrupt Acknowledge) signal. This signal causes the Flag Buffer flip-flop on the Interface card which initiated the interrupt to be reset. The IAK signal is also applied to the PH4/5 SYNC 1 flip-flop (MC46), on the I/O Control card, as a clock pulse.

3-24. The Enable Service Request signal is inhibited during the time between an Interrupt Phase 4 and time T7 of the Fetch Phase of the instruction in the computer-memory interrupt location unless further disabled by a JMP,I or JSB,I instruction in that interrupt location. This ensures full execution of at least one instruction before interrupts are again enabled. At time T7 of the Fetch phase, the STM signal sets the Interrupt Timing flip-flop. The flip-flop is reset at time T0, TS of the next machine phase by the true output of "and" gate MC36A. The trailing-edge output of the Interrupt Timing flip-flop sets the Interrupt Control flip-flop at time T0, TS. The false reset-side output of the Interrupt Control flip-flop is inverted by gate MC27A, providing a true Enable Service Request signal to the I/O Address card, and again allowing Interrupt signals to be sent to the Computer.

3-25. PHASE 5. Phase 5 is a one-cycle suspension of normal computer operation which is caused by the DMA (Direct Memory Access) and the DMI (Direct Memory Increment) Computer options. Since it is not one of the normal machine cycles, Phase 5 must be requested by an option when the option is ready to operate. When Phase 5 is requested (always at time T6 of the machine cycle immediately preceding a Phase 5), the HIS (Hold Interrupt System) signal is received by the I/O Control card. This signal is then applied to inverting "or" gate MC27A where it is inverted and sent to the I/O Address card as a false ESR signal (Paragraph 3-22). When Phase 5 begins actual operation (T0 of the Phase 5 machine cycle), the PH5 signal is received by the I/O Control card and is applied to inverting "or" gate MC27B and to "and" gate MC45B. The resulting false output of inverting "or" gate MC27B is sent to the I/O Address card as the false Enable I/O Address ($\overline{PH5}$) signal. The output of "and" gate MC45B during Phase 5 is dependent upon the state of the output signal from the set-side of the PH4/5 SYNC 1 flip-flop (MC46) (Paragraph 3-22). If Phase 5 has been immediately preceded by a Phase 4, pin 3 of "and" gate MC47B will receive a true input signal during all of Phase 5 from the PH4/5 SYNC 1 flip-flop. At time T5 of Phase 5, the SIR (Set Interrupt Request) signal from "and" gate MC57B is applied as a true signal to the set input of the PH4/5 SYNC 2 flip-flop (MC56). The resulting true output signal from the set-side of the flip-flop is then applied to pin 6 of "and" gate MC47B. This enables "and" gate MC47B which then applies a true output signal to pin 8 of "and" gate MC45B. With the PH5 signal at pin 6 and the true output signal from "and" gate MC47B at pin 8, "and" gate MC45B is now enabled (time T5 of Phase 5). When this occurs, "and" gate MC45B applies a true output signal to the PH4 line which distributes the signal, via Computer backplane wiring, to all Computer circuits normally receiving the PH4 signal.

3-26. If a Phase 5 was not immediately preceded by a Phase 4, the input signal to pin 8 of "and" gate MC45B will be false throughout the entire Phase 5 machine cycle. In this case, "and" gate MC45B will not apply a true signal to the Phase 4 backplane wiring during a Phase 5.

3-27. SWITCH AND OVERFLOW REGISTER SELECTION.

3-28. Select Code 01 must be used to enter the Computer Switch Register setting into the A- or B-Register when using Input/Output instructions LIA/B and MIA/B. Select Code 01 must also be used with Input/Output instructions STO, CLO, SOC, and SOS to perform operations using the 1-bit Overflow Register. Select Code 01 causes the SCM(0) and SCL(1) signals (Figure 3-3) to be applied to the I/O Control card "and" gate MC47C from the I/O Address card. The third input to gate MC47C is the IOG(B) signal, which became true at time T3. The true output of gate MC47C causes "and" gate MC76A to output the IOS signal. The IOS signal is sent to the Computer to enable the applicable Switch Register or Overflow Register operations.

3-29. INTERRUPT SYSTEM CONTROL.

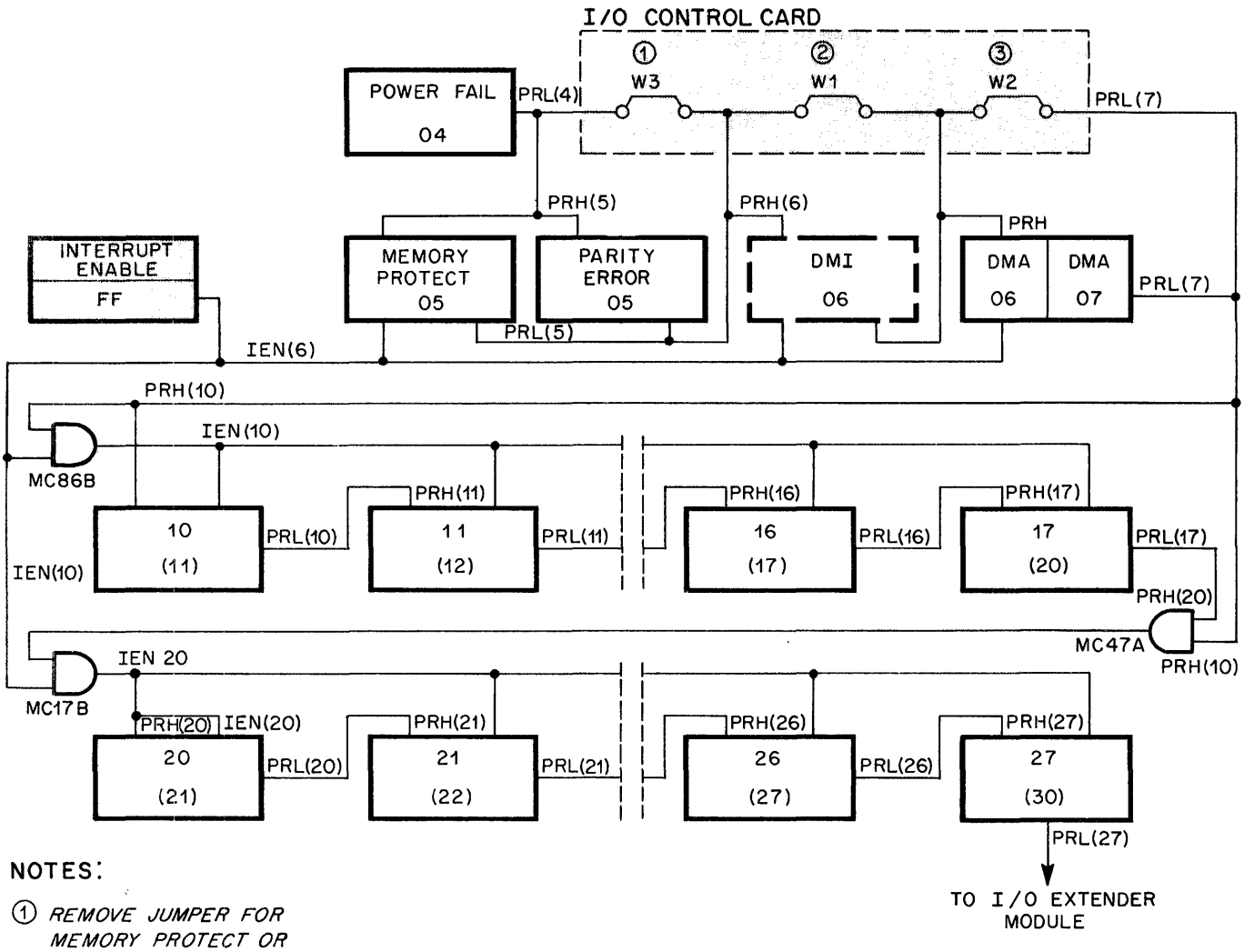
3-30. The set or reset condition of the Interrupt System Enable flip-flop (MC66) determines whether the interrupt system is "on" or "off", under program control. If the flip-flop is set, the IEN signals to the interface cards will enable interrupt requests; if the flip-flop is reset, the IEN signals are removed and interrupt requests will not be enabled. Initially, the interrupt system is disabled by the POPIO signal as described in Paragraph 3-6.

3-31. INTERRUPT SYSTEM ENABLE. If the interrupt system is to function, the Interrupt System Enable flip-flop (Figure 3-3) must be set by a STF instruction with a Select Code of 00. When this is programmed, the SCM(0) and SLC(0) signals are received by the I/O Control card (from the I/O Address card) and applied to "and" gate MC67C. The remaining input to gate MC67C is the true IOG(B) signal. The true output of gate MC67C is "anded" with the STF signal at "and" gate MC67A at time T3. The true output of gate MC67A sets the Interrupt System Enable flip-flop.

3-32. The ESR (Enable Service Request) signal is produced when there is a false input to pin 1 or pin 2 of inverting "or" gate MC27A on the I/O Control card. The input to pin 1 is supplied by the HIS (Hold Interrupt System) signal (pin 4 of I/O Control card), the reset output signal from pin 13 of the Interrupt System Enable flip-flop (MC66), or the POPIO (Power On Pulse to I/O) signal. The input to pin 2 of gate MC27A is the

reset output signal from the Interrupt Control flip-flop (MC26). When present, the ESR signal is applied to pin 21 of the I/O Address card from pin 21 of the I/O Control card.

3-33. Refer to Figures 3-1 and 3-3. The true set-side output signal of the Interrupt System Enable flip-flop (MC66) is applied to "and" gate MC86B and also out pin 10 of the I/O Control card as the IEN(6) (Interrupt Enable, Select Code 06) signal. Pin 10 sends this signal, via Computer backplane wiring, to the interface-card slot connectors which have Select Codes 05 and 06 and also back into the I/O Control card at pin 5 where it is applied to "and" gate MC17B. The Power Fail Interrupt card uses Select Code 04 and has the highest priority in the interrupt system. The Power Fail card generates the PRL(4) signal (Priority Low, Select Code 04) signal which is applied to the two interface-card slots using Select Code 05 as the PRH(5) (Priority High, Select Code 05) signal. These two interface-card slots are reserved for the Memory Protect and Parity Error options. When neither of these two options are in the process of interrupting normal Computer operation, a true PRL(5) signal is sent to the DMI interface-card slot (Select Code 06) as the PRH(6) signal. If neither the Parity



NOTES:

① *REMOVE JUMPER FOR MEMORY PROTECT OR PARITY ERROR OPTIONS*

② *REMOVE JUMPER FOR DMI OPTION*

③ *REMOVE JUMPER FOR DMA OPTION*

Figure 3-1. I/O Control Card IEN, PRN, and PRL Signals

Error or the Memory Protect option is installed in the Computer, the PRH(6) signal is received from the Power Fail card (as the PRL(4) signal) through jumper W3 on the I/O Control card, bypassing the two interface card slots which use Select Code 05, and is applied to the DMI interface-card slot (Select Code 06). If the DMI option is not installed in the Computer, the PRH(6) signal is sent through jumper W1 on the I/O Control card, bypassing the DMI interface-card slot, and is applied to the two interface-card slots reserved for the DMA option (Select Codes 06 and 07). Since the DMA option occupies two interface-card slots, there is no PRL(6)/PRH(7) signal sent from one of the DMA interface-card slots to the other. When DMA is installed in the Computer and not operating, the PRL(7) signal is generated by the DMA interface-card slot having Select Code 07. This signal is applied to "and" gates MC86B and MC47A and to the interface-card slot having Select Code 10 as the PRH(10) signal. If the DMA option is not installed in the Computer, the PRH(6) signal (from Power Fail, Memory Protect or Parity Error) is sent through jumper W2 on the I/O Control card, bypassing the DMA option interface-card slots, and effectively becomes the PRH(10) signal. This signal is then sent out of the I/O Control card and is applied to the same places as is the actual PRH(10) signal from the DMA option. If none of the Computer options described above (Memory Protect, Parity Error, DMI or DMA) are installed in the Computer, the PRL(4)/PRH(5) signal from the Power Fail card is sent through jumpers W3, W1, and W2 on the I/O Control card and then applied to the PRH(10) circuit as the PRH(10) signal.

3-34. When "and" gate MC86B receives two true input signals, IEN(6) from the Interrupt System Enable flip-flop and PRH(10) from DMA, a true output signal, IEN(10), is sent to the interface card slots having Select Codes 10 through 17. The PRH(10) signal is also applied to the interface-card slot that has Select Code 10. With both the IEN(10) and the PRH(10) signals true, the I/O device using the interface-card slot having Select Code 10 may interrupt normal Computer operation whenever requested by the Computer program or when the I/O device itself requests an interrupt. If one of the interface cards that has a higher priority (Power Fail, Memory Protect, Parity Error, DMI, or DMA) requests an interrupt, all succeeding interface-card slots of a lower priority will be disabled and the PRH(10) signal which is sent to "and" gate MC86B and to the interface-card slot having Select Code 10 will be false. When this happens, "and" gate MC86B in turn applies a false IEN(10) output signal to the interface-card slots having Select Codes 10 through 17. This action disables all eight I/O interface card slots (Select Codes 10 through 17). In this condition it is impossible for I/O devices using Select Codes 10 through 17 to interrupt the Computer program until both the IEN(6) and the PRH(10) signals to "and" gate MC86B are ture once again. When this block of eight interface-card slots (Select Codes 10 through 17) are enabled and the interface-card slots having Select Codes 04 through 17 are not requesting an interrupt, a true PRL(17) signal is sent from the interface-card slot having Select Code 17 to pin 16 of the I/O Control card. After entering pin 16 of the I/O Control card, this signal is applied to pin 2 of "and" gate MC47A as a true input signal. Now that "and" gate MC47A is receiving the true PRH(10) signal at pin 1 and the true PRL(17) signal at pin 2, it is enabled and it applies a true output signal to pin 6 of "and" gate MC17B. At this time, "and" gate MC17B is also receiving the true IEN(6) signal at pin 8, which causes "and" gate MC17B to apply a true output signal out pin 7 of the I/O Control card as the IEN(20) signal. From pin 7 of the I/O Control card the IEN(20) signal is applied to the interface-card slot having Select Code 20 as both the IEN(20) signal and the PRH(20) signal. The IEN(20) signal is also applied to the interface-card slots having Select Codes 21 through 27. Each of these seven interface-card slots receive their respective PRH signals, PRH(21) through PRH(27), from the preceding interface-card slot having the Select Code of the next highest priority. Interrupt operation of these eight interface-card slots (Select Codes 20 through 21) is now the same as the preceding block of eight interface-card slots (Select Code 10 through 17). The determining factor for any interface-card slot requesting an interrupt is the PRH signal. If an I/O device of a higher priority (lower Select Code) is already interrupting or has requested an interrupt, this signal is false causing interface-card slots having lower priority Select Codes to be disabled. This same interrupt enabling process is extended to include the additional Select Codes whenever an I/O Extender module is used.

3-35. INTERRUPT SYSTEM DISABLE. To disable the interrupt system, the Interrupt System Enable flip-flop must be reset by a CLF instruction with a Select Code of 00. When this is programmed, the SCM(0) and SCL(0) signals are applied to "and" gate MC67C. Since the CLF instruction is an IOG instruction, the output of "and" gate MC57A (which is applied to gate MC67C) will be true about 80 nanoseconds after receipt of the IOG signal. All inputs to gate MC67C are then true. The true output of gate MC67C is applied to "and" gate MC67B. The true CLF signal is also applied to gate MC67B. The true output of this "and" gate resets the Interrupt System Enable flip-flop. The set-side output of the flip-flop becomes false, removing the IEN signal to all interface-card slot connectors (see Figure 3-1). This immediately prevents any interface card (device) from requesting an interrupt.

3-36. SKIP FLAG INSTRUCTIONS.

3-37. Through the use of the SFS and SFC program instructions, the next instruction in the Computer program can be skipped depending on the set or reset condition of the Interrupt System Enable flip-flop. When the Interrupt System Enable flip-flop is set and an SFS instruction is programmed with a Select Code of 00, all inputs to "and" gate MC97A are true. (The output of "and" gate MC67C is true since the SFS instruction is an IOG instruction and provides the IOG signal, and the SCM(0) and SCL(0) signals represent the Select Code used.) Gate MC97A causes "and" gate MC17A to issue a true SKF signal to the Computer. The SKF signal causes the program to skip the next instruction since the Interrupt System Enable flip-flop was set.

3-38. Similarly, when the Interrupt System Enable flip-flop is reset and an SFC instruction is programmed with a Select Code of 00, all inputs to "and" gate MC97B are true (for the same reasons as in Paragraph 3-35). Gate MC97B causes "and" gate MC17A to issue a true SKF signal to the Computer. The SKF signal again causes the program to skip the next instruction since in this case, the Interrupt System Enable flip-flop was reset.

3-39. REPLACEABLE PARTS.

3-40. Refer to Table 3-1 for a list of replaceable parts in alpha-numerical order of their reference designations, with a description and HP part number for each part.

3-41. To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office. See the list at the rear of this manual for field-office addresses.

3-42. Specify the following information for each part when ordering:

a. Hewlett-Packard part number

b. Circuit reference designation

c. Description

3-43. To order a part not listed in Table 3-1, give a complete description of the part and include its function and location.

Table 3-1. Replaceable Parts for I/O Control Card

REFERENCE DESIGNATION	DESCRIPTION	HP PART NO.
C1,2	Capacitor, fixed, Tant., 2.2 μf	0180-0155
C3	Capacitor, fixed, ceramic, 300 pf	0140-0225
CR1,2,3	Diode	1910-0022
MC26,56	Microcircuit Package	1820-0957
MC17,35,45,57,76, 86,87	Microcircuit Package	1820-0956
MC16,27,55,66	Microcircuit Package	1820-0953
MC36,37,47,67	Microcircuit Package	1820-0953
MC77	Microcircuit Package	1820-0965
MC97	Microcircuit Package	1820-0954
R1,2,4-6	Resistor, fixed, 1K ±5%, 1/4W	0683-1025
R3	Resistor, fixed, 430 ohms ±2%	0757-0915

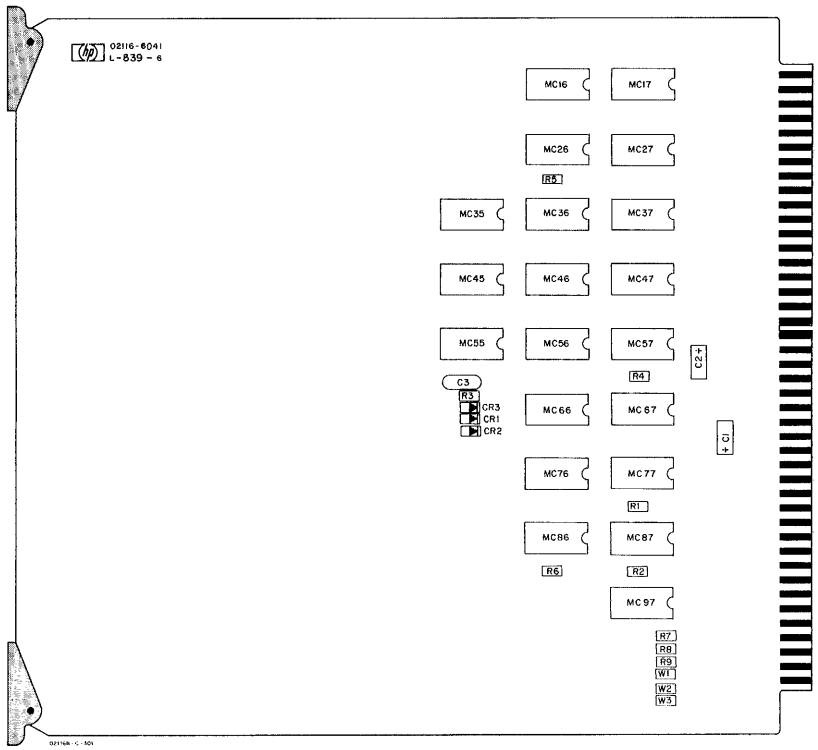
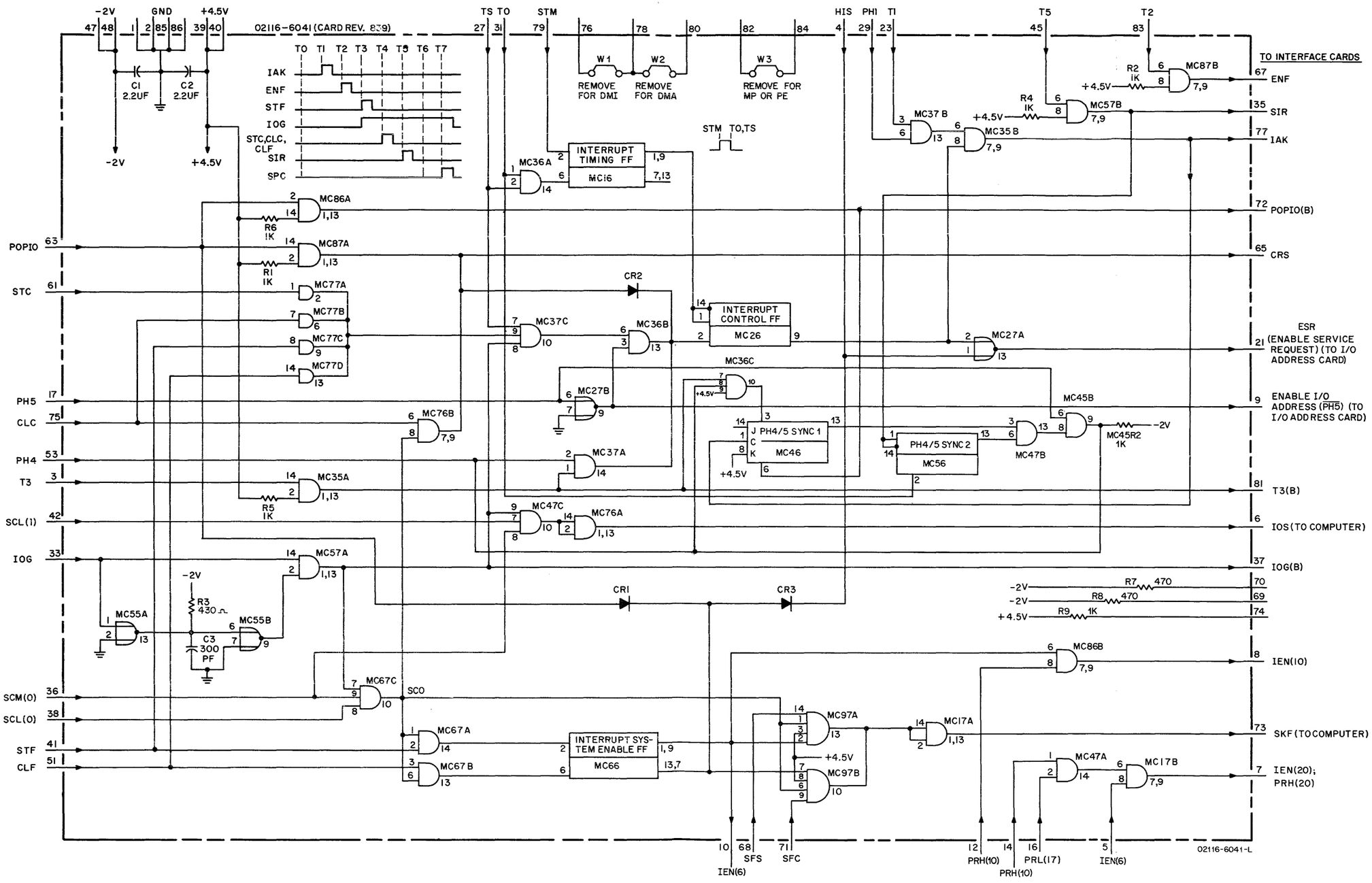


Figure 3-2. I/O Control Card, Component Location



NOTES:

1. ALL LOGIC IS POSITIVE-TRUE.
2. THE TIMING CHART DOES NOT RELATE SIGNALS TO THE MACHINE PHASE IN WHICH THEY OCCUR.

Figure 3-3. I/O Control Card

SECTION IV
I/O ADDRESS CARD

4-1. INTRODUCTION.

4-2. This section provides theory of operation information for the I/O Address card (HP Part No. 02116-6194). The card is of standard interface-card size and plugs into Position 202 on the left side of the input/output slots of the Computer. The slot connector transfers all signals to and from the card; no additional cabling is required. The I/O Address card has three main functions. First, it decodes the 6-bit Select Code from the Computer to provide a 2-digit octal code for selection of the interface card through which the Computer is to communicate with the input/output device. Second, it encodes the Flag and IRQ signals from the interface cards to provide a 6-bit address and an Interrupt signal to the Computer. The 6-bit address identifies the interface card (device) requesting an interrupt. Third, the Control Interrupt Register provides the address of the last I/O device that interrupted the computer program. This information is available for special program use by the computer user. The Central Interrupt Register will furnish this address to the computer central processor only when called for by program instructions.

4-3. THEORY OF OPERATION.

4-4. DECODING FUNCTION.

4-5. When an I/O instruction is programmed, the 6-bit Select Code portion (bits 0 through 5) of the instruction is received by the I/O Address card (Figure 4-2). The three least significant bits (0-2) and their NOT conditions are applied to eight "and" gates, MC55A/B, MC65A/B, MC75A/B, and MC85A/B. The three most significant bits (3-5) and their NOT conditions are also applied to eight "and" gates, MC95A/B, MC105A/B, MC115A/B, and MC125A/B. All "and" gates have a common enabling input from "and" gate MC16A. The Enable I/O Address signal to gate MC16A is received from the I/O Control card and is always true except during Direct Memory Access (DMA) and Direct Memory Increment (DMI) operations (Phase 5).

NOTE

Table 4-2 lists the part numbers of the microcircuit packages identified in Figure 4-2 by reference designations preceded by MC. The Appendix in Volume Two contains logic diagrams of the microcircuit packages according to part number.

4-6. The true output of each "and" gate represents an octal digit and only one "and" gate in each group of eight will be true for any given Select Code. The true outputs of the two "and" gates form the SCM (Select Code Most Significant Digit) and the SCL (Select Code Least Significant Digit) signals. Each of the outputs of this first group of 16 "and" gates are buffered out of the I/O Address card to the interface cards by a second group of 16 gates. These gates provide the drive necessary to apply signals of proper amplitude to the interface cards. The 1K resistor between each of the gates and the -2 volt supply minimizes the effect of any transient noise which may exist on the lines to the interface cards and reduces the fall time of the gate output voltage.

4-7. Example: With a Select Code of 11 (001 001 binary) applied to the I/O Address card, only bit 0 and bit 3 are true input signals. In Figure 4-2, each Select Code bit input is applied to four "and" gates as follows:

a. The bit 0 input is applied to "and" gates MC75B, MC55B, MC65B, and MC85B. The output of "and" gate MC75B is true since the bit 0, bit 1, and bit 2 inputs and the output of gate MC16A are true inputs. The outputs of the other three "and" gates are false since the bit 1 and bit $\overline{2}$ inputs are false. The output of gate MC75B is applied to "and" gate MC76B and then to pin 67 as a true SCL(1) signal to the interface cards.

b. The bit 3 input is applied to "and" gates MC105B, MC95B, MC115B, and MC125B. The output of "and" gate MC125B is true since the bit 3, bit $\overline{4}$, and bit $\overline{5}$ inputs and the output of gate MC16A are true inputs. The outputs of the other three "and" gates are false since the bit 4 and bit 5 inputs are false. The output of gate MC125B is applied to "and" gate MC126B and then to pin 77 as a true SCM(1) signal to the interface cards.

4-8. The SCM and SCL signal combination determines the slot connector containing the interface card to which the instruction portion of the I/O instruction word is directed. Each slot connector, and therefore each interface card, contains two octal Select Codes as was described in Section II. Figure 4-1 illustrates the SCM and SCL signal paths to basic Computer interface-card slot connectors. Note that the SCM(1) signal is applied to the most-significant-digit input pins on interface-card slot connectors with Select Codes of 10 through 17. The SCM(2) signal is applied to basic computer interface-card slot connectors with Select Codes of 20 through 27. Similarly, the SCM(3) through SCM(7) signals are applied to Module Extender options containing interface-card slot connectors with Select Codes of 30 through 47, 50 through 67, and 70 through 77. The SCM(0) signal is applied to the I/O Control card (Select Codes 00 and 01) slot connector in the input/output section of the Computer. It is also applied to the DMA 1 and DMA 2 option (Select Codes 02, 03, 06, and 07) and the Power Fail Interrupt (Select Code 04) slot connectors in the Logic section of the Computer. The SCL(0) through SCL(7) signals are applied to the least-significant-digit input pins on the

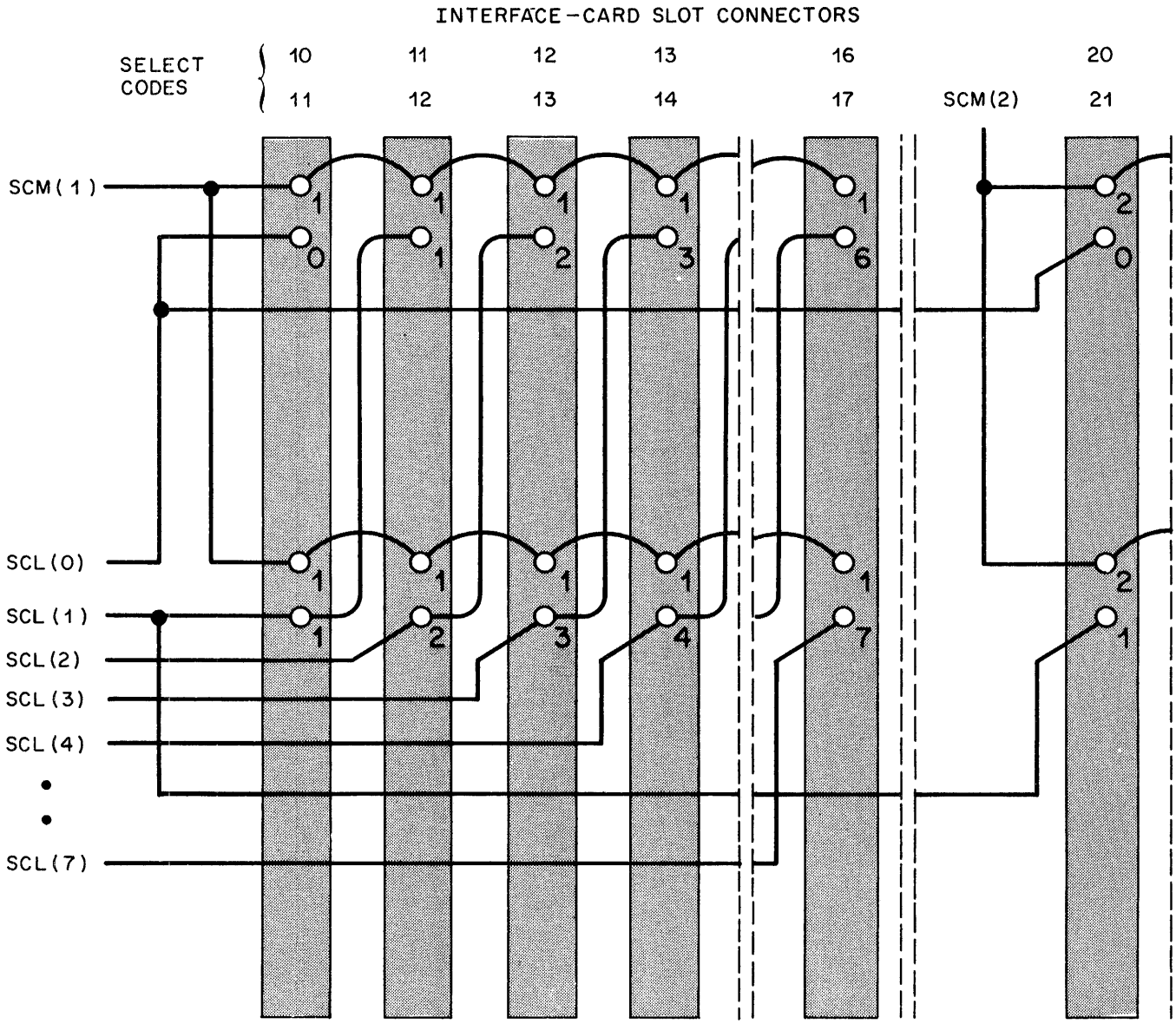


Figure 4-1. SCM and SCL Signal Paths

slot connectors in the Computer and in the Module Extenders. The slot connectors in the Module Extenders are wired in the same manner as those in the basic Computer.

4-9. The SCM and SCL signals are applied to the same-numbered pins on all interface-card slot connectors as follows:

a. Pin 14: Lower Select Code, Most Significant digit. (LSCM).

b. Pin 16: Lower Select Code, Least Significant digit. (LSCL).

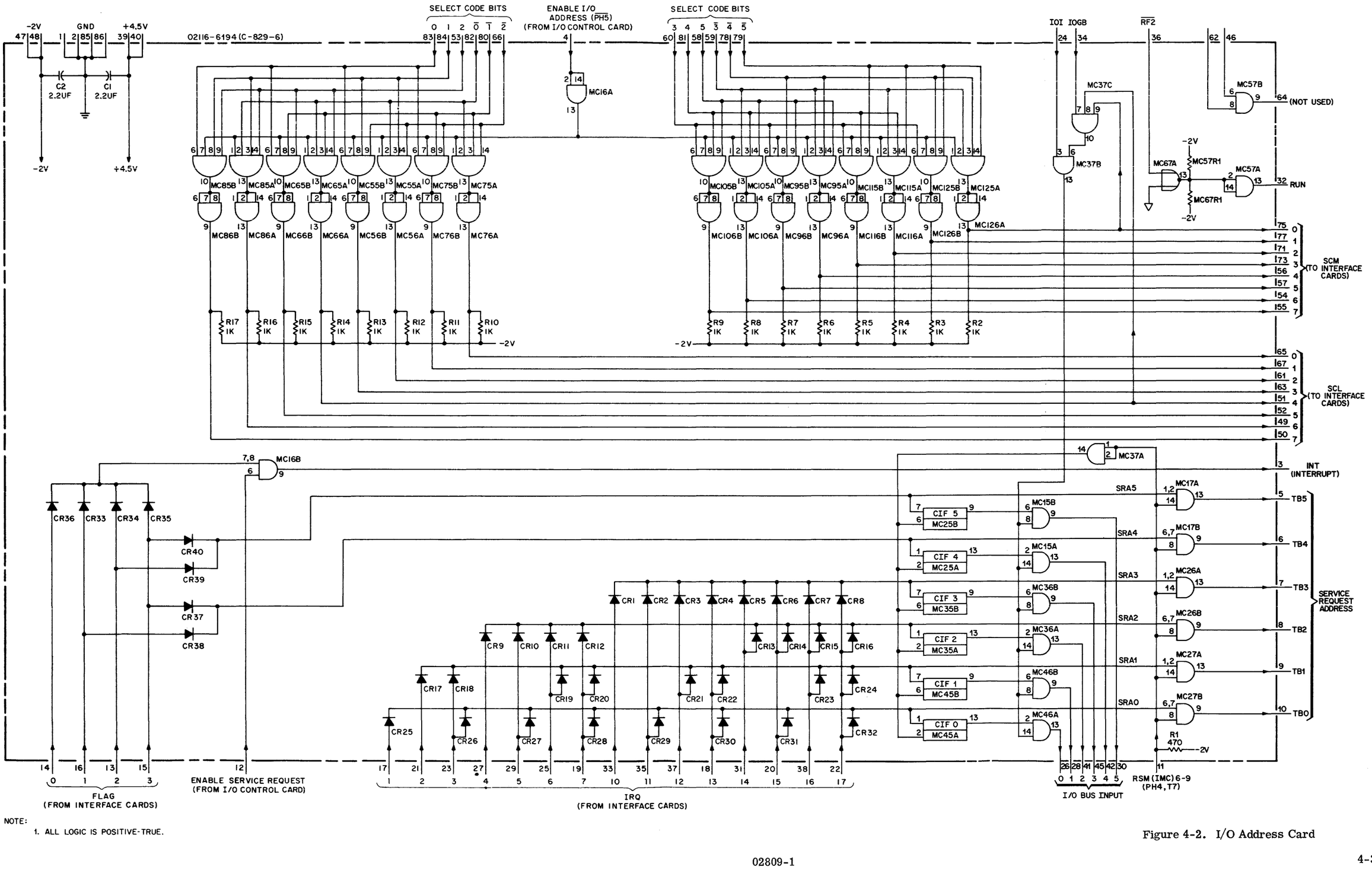
c. Pin 37: Higher Select Code, Most Significant digit. (HSCM).

d. Pin 34: Higher Select Code, Least Significant digit. (HSCL).

4-10. ENCODING FUNCTION.

4-11. When an input/output device requests an interrupt of the Computer program, the IRQ flip-flop on the interface card for the device is set. The set-side output of the IRQ flip-flop applies a true FLG (Flag) signal to the I/O Address card; the reset-side output of the flip-flop is inverted by an inverting "or" gate to apply a true IRQ signal to the I/O Address card. Refer to Figure 4-2. These two signals are used to form the Interrupt signal and the Service Request Address to be transferred to the Computer.

4-12. INTERRUPT SIGNAL. An Interrupt signal is sent to the Computer at time T5 of the current machine phase when a Flag signal is received from an interface card and if the Enable Service Request signal is received from the I/O Control card. (To establish



NOTE:

1. ALL LOGIC IS POSITIVE-TRUE.

Figure 4-2. I/O Address Card

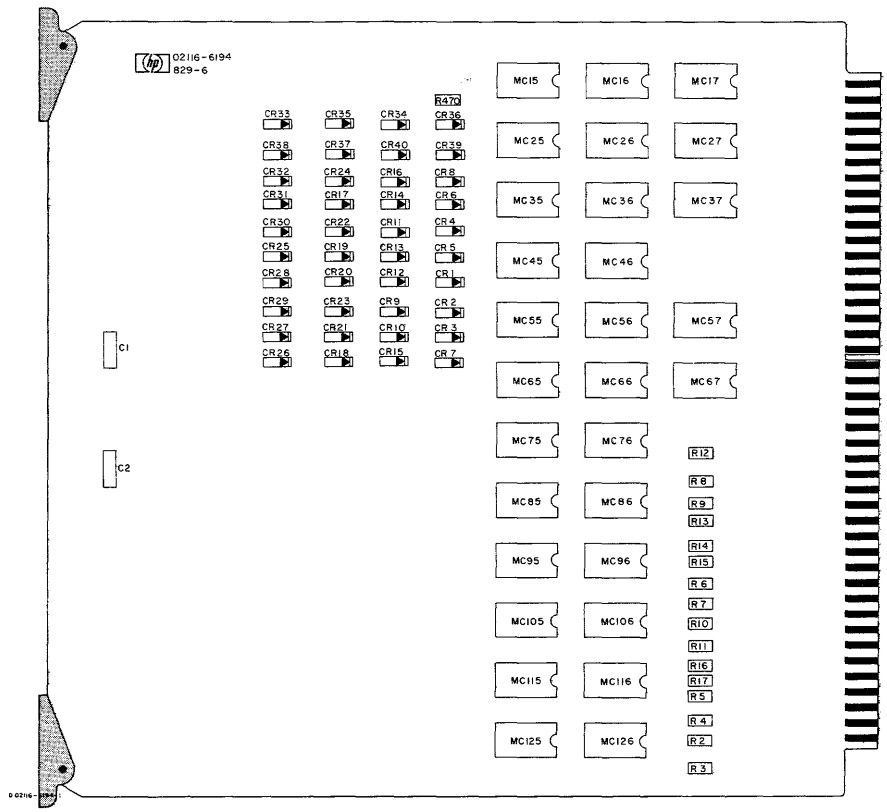


Figure 4-3. I/O Address Card, Component Location

when the Enable Service Request signal is true, refer to Figure 2-6, Typical Interrupt System Timing.) The Interrupt signal causes the Computer to enter Interrupt Phase 4 at the end of the current machine phase.

4-13. As shown in Figure 4-2, four Flag signals (0 through 3) can be received from the interface cards. These signals are described in steps "a" through "d". Receipt of a Flag signal applies a true input to "and" gate MC16B through one of the CR33 through CR36 diodes. If the Enable Service Request signal is true, the gate MC16B output is applied to the Computer as a true Interrupt signal.

a. Flag (0): This input is true when an interface card with a Select Code of 05 to 17 is requesting an interrupt.

b. Flag (1): This input is true when an interface card with a Select Code of 20 to 37 is requesting an interrupt.

c. Flag (2): This input is true when an interface card with a Select Code of 40 to 57 is requesting an interrupt.

d. Flag (3): This input is true when an interface card with a Select Code of 60 to 70 is requesting an interrupt.

4-14. SERVICE REQUEST ADDRESS. Refer to Figure 4-2. The 6-bit Service Request Address is the Select Code of the interface-card requesting an interrupt, in binary form. It is sent to the M-Register of the Computer via the T bus and specifies the interrupt location for that device in memory. (The interrupt location contains the instruction to be executed when the particular interrupt occurs.) While the Interrupt signal is sent to the Computer at time T5 of the current machine phase, the Service Request Address is not enabled to the Computer until time T7 of Interrupt Phase 4.

4-15. The Service Request Address is formed by encoding the combination of Flag and IRQ signals from the interface card requesting an interrupt. The flag signals are true for the conditions listed in Paragraph 4-13 steps "a" through "d". The Flag (0) through Flag (3) signals determine the two most significant bits (bits 4 and 5) of the address and are applied to diodes CR37 through CR40 and then to "and" gates MC17A and MC17B. The IRQ signals determine the four least significant bits (bits 0 through 3) of the address and are applied to diodes CR1 through CR32 and then to "and" gates MC26A, MC26B, MC27A, and MC27B. The remaining input to the Service Request Address "and" gates is applied at time T7 of Interrupt Phase 4 by the RSM (IMC)6-9 (PH4, T7) signal from the Computer. The Flag and IRQ signals received from various interface cards and their Select Codes are indicated by Table 4-1. This table also indicates the I/O Address Card components that these signals are applied to in obtaining the 6-bit Service Request Address. This table should be used in conjunction with Figure 4-2 to obtain an understanding of the encoding function of the I/O Address card.

4-16. RUN SIGNAL. The $\overline{RF2}$ (Run flip-flop 2, "not") signal from the Computer timing generator is input at pin 36 of the I/O Address card where it is applied to inverting "or" gate MC67A. When the Computer is running and is not in a HALT condition the $\overline{RF2}$ signal is always false. When the Computer is in a HALT condition the $\overline{RF2}$ signal is true. Inverting "or" gate MC67A inverts the $\overline{RF2}$ signal and applies it to "and" gate MC57A as an input. Since the two input pins

Table 4-1. I/O Address Card Encoding Examples

Interface Card Select Code (Octal)	Flag Signal	Flag Signal is Applied		IRQ Signal	IRQ Signal is Applied		For a Service Req. Address of (Binary)
		To Diode(s)	Then to "and" Gate(s)		To Diode(s)	"and" Gate(s)	
07	0	-	-	7	CR28,CR20, CR12	MC27B, MC27A, MC26B	000 111
10	0	-	-	10	CR1	MC26A	001 000
21	1	CR38	MC17B	1	CR25	MC27B	010 001
32	1	CR38	MC17B	12	CR21, CR3	MC27A, MC26A	011 010
43	2	CR39	MC17A	3	CR26,CR18	MC27B, MC27A	100 011
54	2	CR39	MC17A	14	CR13, CR5	MC26B, MC26A	101 100
65	3	CR37, CR40	MC17B, MC17A	5	CR27,CR10	MC27B, MC26B	110 101
76	3	CR37, CR40	MC17B, MC17A	16	CR23,CR15, CR7	MC27A, MC26B MC26A	111 110

(pin 2 and 14) of "and" gate MC57A are tied together, it produces a true output signal whenever it receives a true input from inverting "or" gate MC67A (whenever the Computer is in the RUN mode). This signal is then sent out of the I/O Address card at pin 32 as the RUN signal and is applied to pin 50 of all I/O interface-card slots (Select Codes 10 through 27). If an extender module is used with the Computer, the RUN signal is also applied to pin 50 of all interface-card slots in the extender.

4-17. CENTRAL INTERRUPT REGISTER.

4-18. The Central Interrupt Register (Flip-Flops CIF0 through CIF5 and "and" gates MC15A, MC15B, MC36A, MC36B, MC46A, and MC46B) stores the Service Request Address. This information, or address, is always available during a Phase 4 I/O operation and is strobed into the Central Interrupt Flip-Flops, CIF0 through CIF5, at T7 of Phase 4. To utilize this address, the computer operator must execute an I/O load or merge instruction containing a Select Code of 04. These instructions would be LIA/B and MIA/B used with Select Code 04. Select Code 04, the Power Fail Interrupt Select Code, is not required for any Power Fail Interrupt function during a load instruction so has been used here. On the I/O Address card, the Phase 4, T7 signal enables gate MC37A which then applies its true output to all flip-flops of the Register (CIF0 through CIF5). This action causes the address to be written into the register flip-flops. In order to then apply this address to the computer central processor, the IOGB signal and both Select Code signals (representing Select Code 04) must be applied to "and" gate MC37C. The output of gate MC37C is then applied to "and" gate MC37B simultaneously with the IOI signal. When all of these signals are presented, (having been generated by a computer program instruction of the type mentioned above) the output of gate MC37B is applied to all of the Central Interrupt Register output "and" gates (MC15A, MC15B, MC36A, MC36B, MC46A, and MC46B). This action enables all output gates of the register and the address that it contains is applied to the IOBI of the computer central processor.

4-19. REPLACEABLE PARTS.

4-20. Refer to Table 4-2 for a list of replaceable parts in alpha-numerical order of their reference designations, with a description and HP part number for each part.

4-21. To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office. See the list at the rear of this manual for field office addresses.

4-22. Specify the following information for each part when ordering:

a. Hewlett-Packard part number.
b. Circuit reference designation.
c. Description.

4-23. To order a part not listed in Table 4-2, give a complete description of the part and include its function and location.

Table 4-2. Replaceable Parts for I/O Address Card

REFERENCE DESIGNATION	DESCRIPTION	HP PART NO.
C1,2	Capacitor, fixed, Tant., 2.2 μf	0180-0155
CR1 thru 40	Diode	1901-0040
MC15,16,17,26,27, 36,46,56,57,66, 76,86,96,106, 116,126	Microcircuit Package	1820-0956
MC55,65,75,85,95, 105,115,125	Microcircuit Package	1820-0954
MC37	Microcircuit Package	1820-0953
MC25,35,45	Microcircuit Package	1820-0968
MC67	Microcircuit Package	1820-0952
R1	Resistor, fixed, 470 ohms ±5%, 1/4W	0683-4715
R2 thru 17	Resistor, fixed, 1K ±5%, 1/4W	0683-1025

SECTION V
RESISTANCE LOAD CARD

5-1. INTRODUCTION.

5-2. This section contains description, installation and replaceable parts information, and a schematic diagram for the Resistance Load Card.

5-3. DESCRIPTION.

5-4. The Resistance Load Card (HP Part No. 02116-6047) is of standard interface-card size and plugs into Position 218 on the right side of the input/output slots of the Computer. The card contains 18 resistors which are used to load the termination of the IOBO (I/O Bus Output) lines and the CRS line from the Computer to the interface card slot connectors. These lines terminate at slot position 218. The other end of the resistors are connected to the -2 volt supply through slot connector pins 47 and 48. The lines are loaded to eliminate any transient noise generated by these lines in the backplane wiring of the Computer. No external cabling to the Resistance Load card is required.

5-5. INSTALLATION.

5-6. Pull open the front panel of the Computer. Plug the Resistance Load card into slot position 218 of the Computer Input/Output section. Close the front panel of the Computer. The card remains in the Computer unless the total interface and Priority Jumper cards equal 16. At that time, remove the card as it is no longer required.

NOTE

The Resistance Load card does not contain a priority bus circuit. Therefore it cannot be plugged into a slot with a lower slot-position number than one containing an interface or Priority Jumper card. If it is, the interrupt system of the Computer will not function properly.

5-7. SCHEMATIC DIAGRAM.

5-8. Refer to Figure 5-1 for a schematic diagram of Resistance Load card.

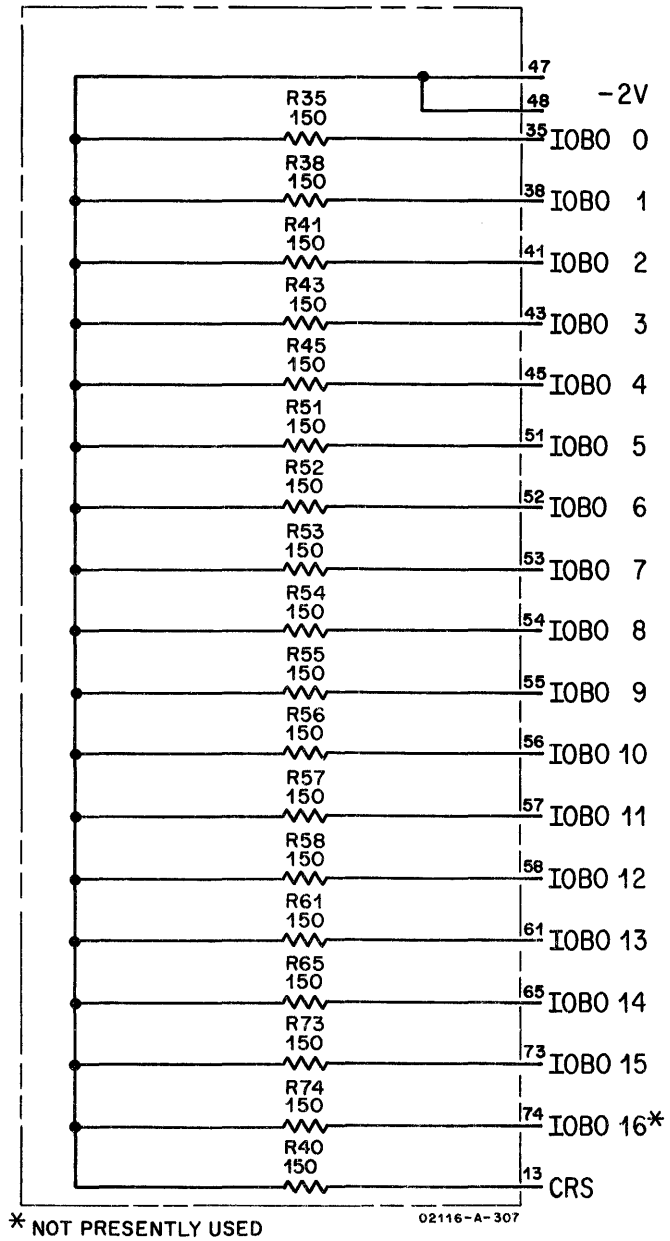


Figure 5-1. Resistance Load Card Schematic Diagram

5-9. REPLACEABLE PARTS.

5-10. Refer to Table 5-1 for a list of replaceable parts in alpha-numerical order of their reference designations, with a description and HP part number for each part.

5-11. To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office. See the list at the rear of this manual for field office addresses.

5-12. Specify the following information for each part when ordering:

a. Hewlett-Packard part number.
b. Circuit reference designation.
c. Description.

5-13. To order parts not listed in Table 5-1, give a complete description of the part and include its function and location.

Table 5-1. Replaceable Parts for Resistance Load Card

REFERENCE DESIGNATION	DESCRIPTION	HP PART NO.
R35,38,40,41,42,45, 51 thru 58,61,65,73, 74	Resistor, fixed, 150 ohms	0683-1515

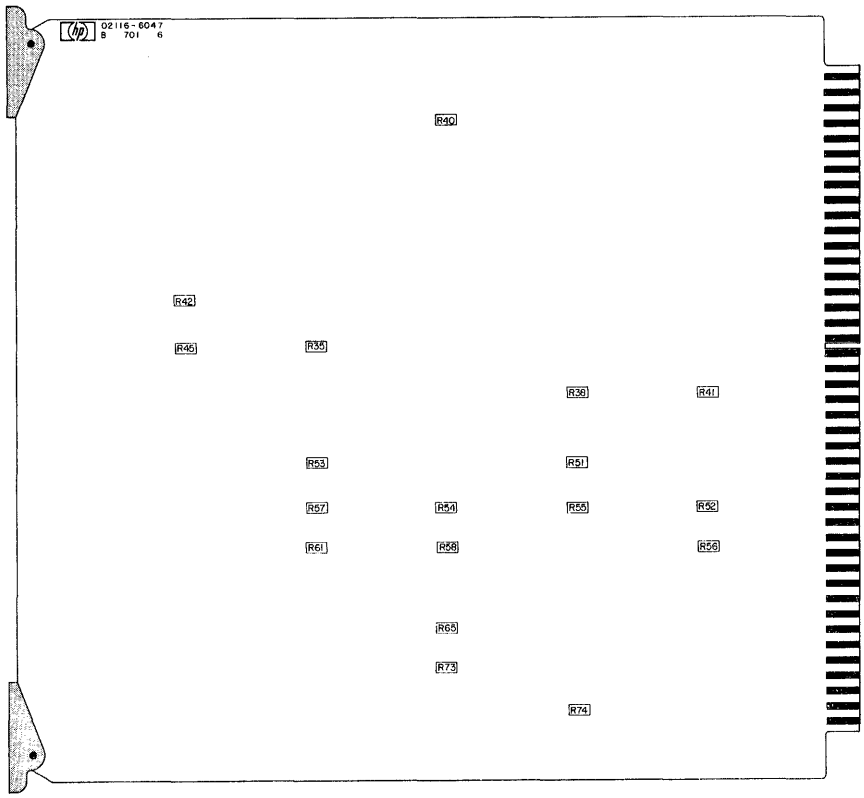


Figure 5-2. Resistance Load Card, Component Location

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