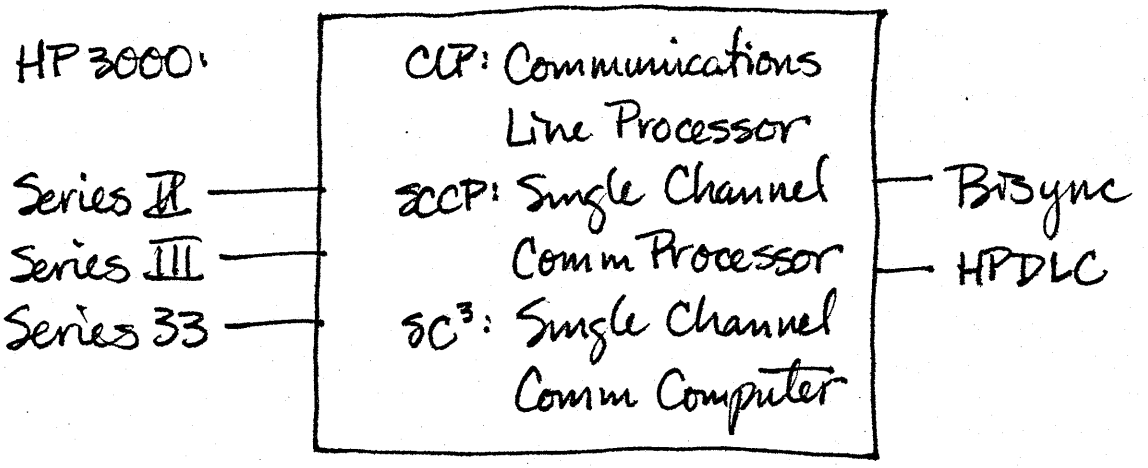
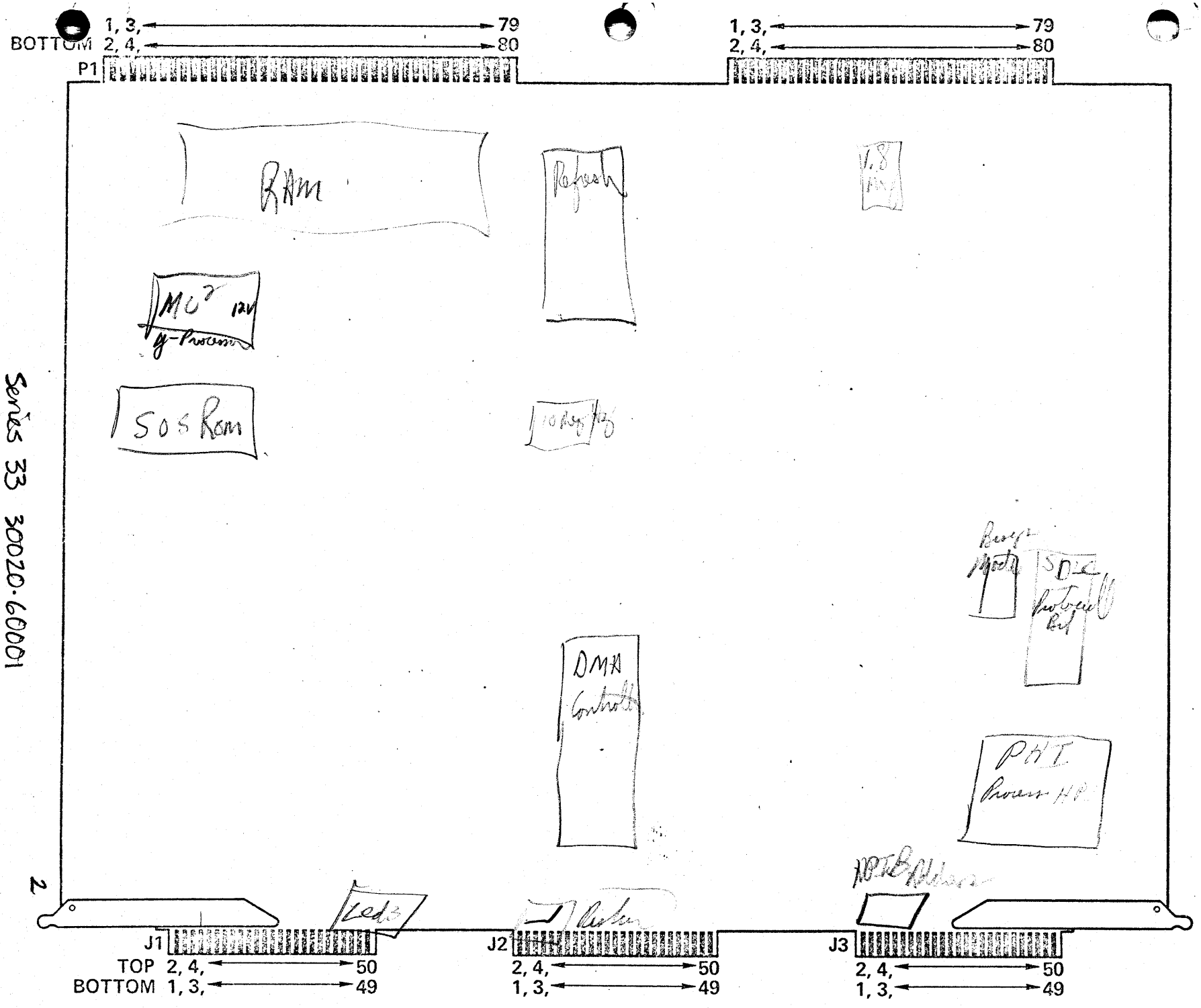
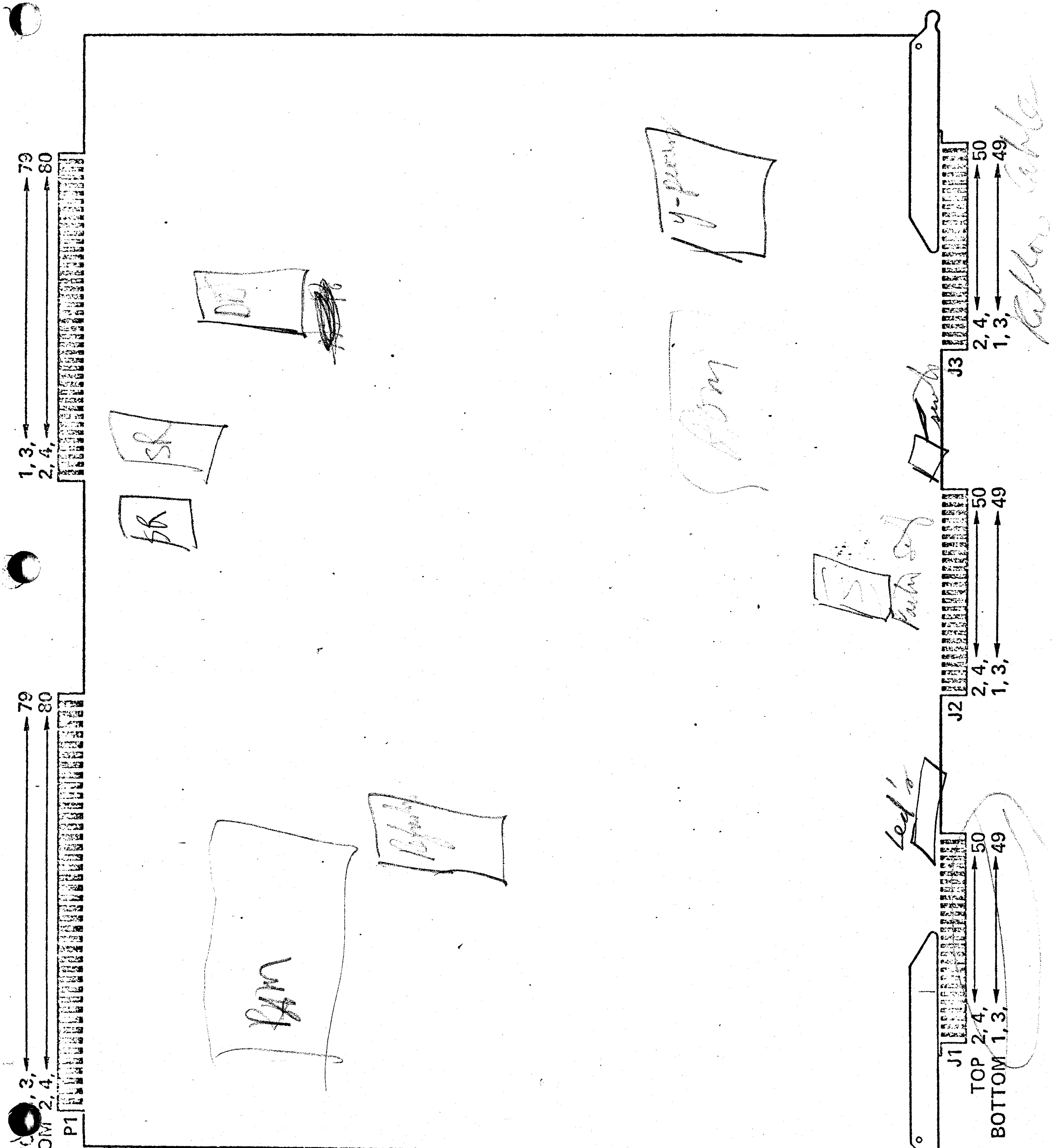

HP 3000:
Series II
Series III
Series 33
CLP: Communications Line Processor
SCCP: Single Channel Comm Processor
SC³: Single Channel Comm Computer
BiSync
HPDLC

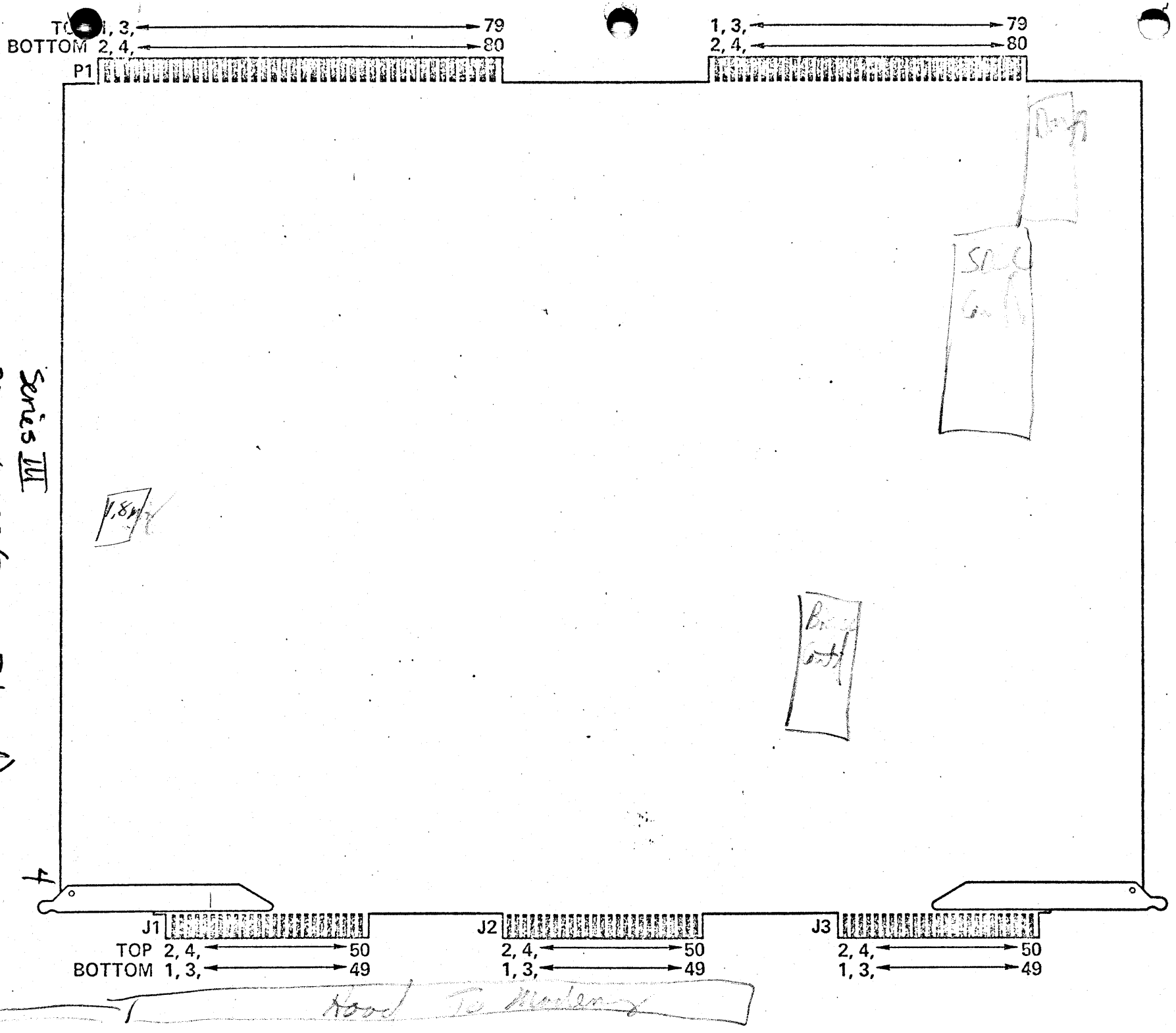


Series 33 30020-60001



Series III

30010-60001 (MPU or A board) Polled

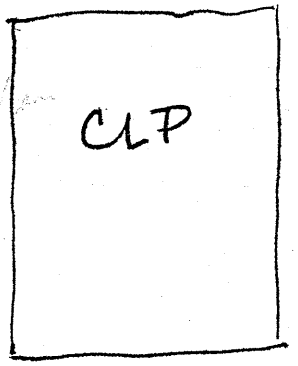


Series III
30010-60002 (DI or B board)

4

Hood To Hinder

1. Standard Bisync
2. IML
3. MRJE
4. HPDLC
5. HP2645 MTS



RS·232C
RS·449
Direct Connect
Bell DDS
Bell 303

APPENDIX D
CLP SELF-TEST DESCRIPTION

+ LED INDICATORS +

SELF TEST EXECUTING

7	6	5	4	3	2	1	0	
X						X	X	SELF TEST
	X					X	X	BASIC INSTRUCTION SET
		X				X	X	ROM TEST
		X				X	X	SDLC TEST
X		X				X	X	SDLC TEST W/DMA
			X			X	X	USART TEST
X			X			X	X	USART W/DMA
0	0	0	0	X		X	X	RAMTEST *
X	X					X	X	RAMTEST PARITY ERROR
	X	X				X	X	TIMER TEST

* DATA/ADDRESS/REFRESH ERROR

X=LED ON
0= WHEN ON EQUALS THE CHIP (BIT) FAILURE — IN BINARY

NOTE: LEDS 4, 5, & 7 CAN BE ON IF USART, SDLC, & DMA FAIL.

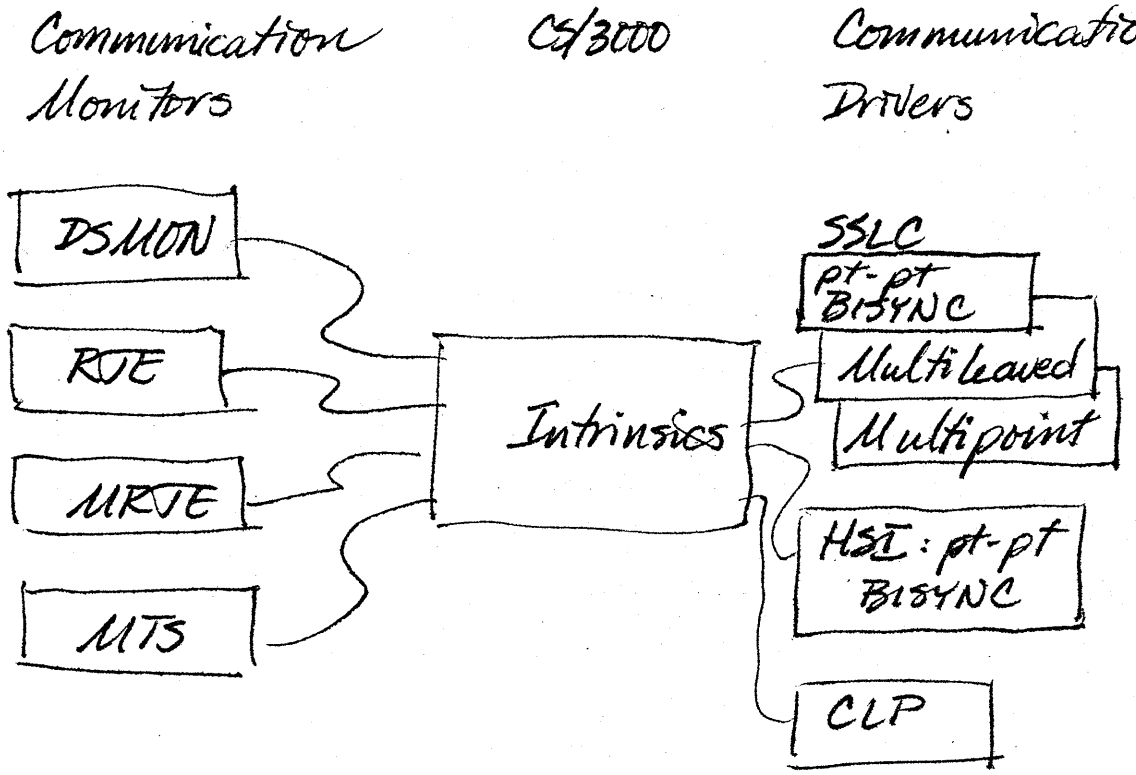
EXECUTING STATE

7	6	5	4	3	2	1	0	
X							X	ROM CONTROL PROGRAM
	X						X	SELF-TEST COMPLETED
		X					X	MASTER RESET/GROUP TRIGGER
			X				X	RAM SOFTWARE FAILURE
				X			X	POWER FAIL RECOVERY
					X		X	PARITY ERROR DETECTED
						X	X	POWER FAIL
						X		ENTERED RAM BY COMMAND
X						X		ENTERED RAM BY RECOVERY
			X	X			X	SHUTDOWN

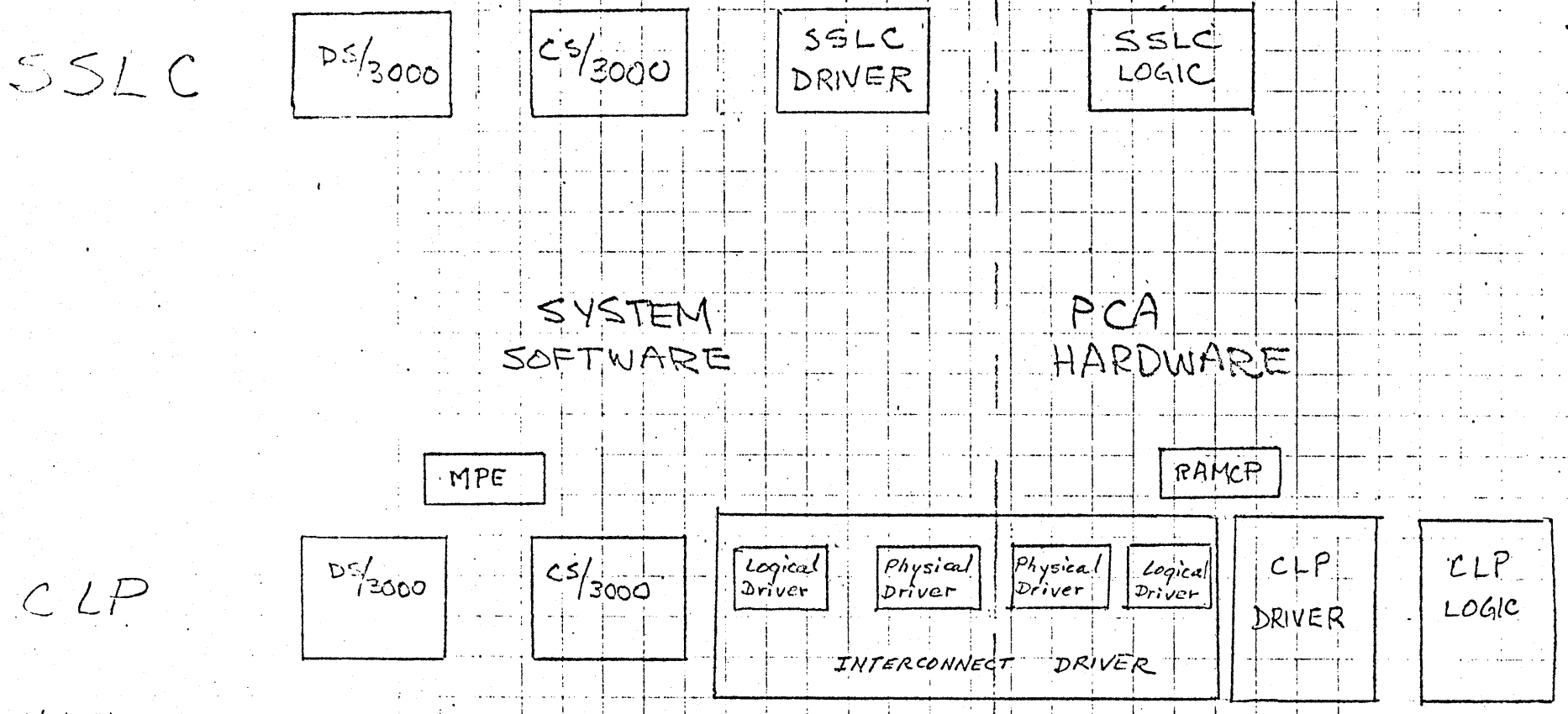
+ RESIDENT DIAGNOSTICS +

CLP6

These programs stored in ROM are executed after a self-test command is received from the mainframe. They provide confidence level testing of the system. The resident diagnostic programs detect the fundamental types of faults in the various units of

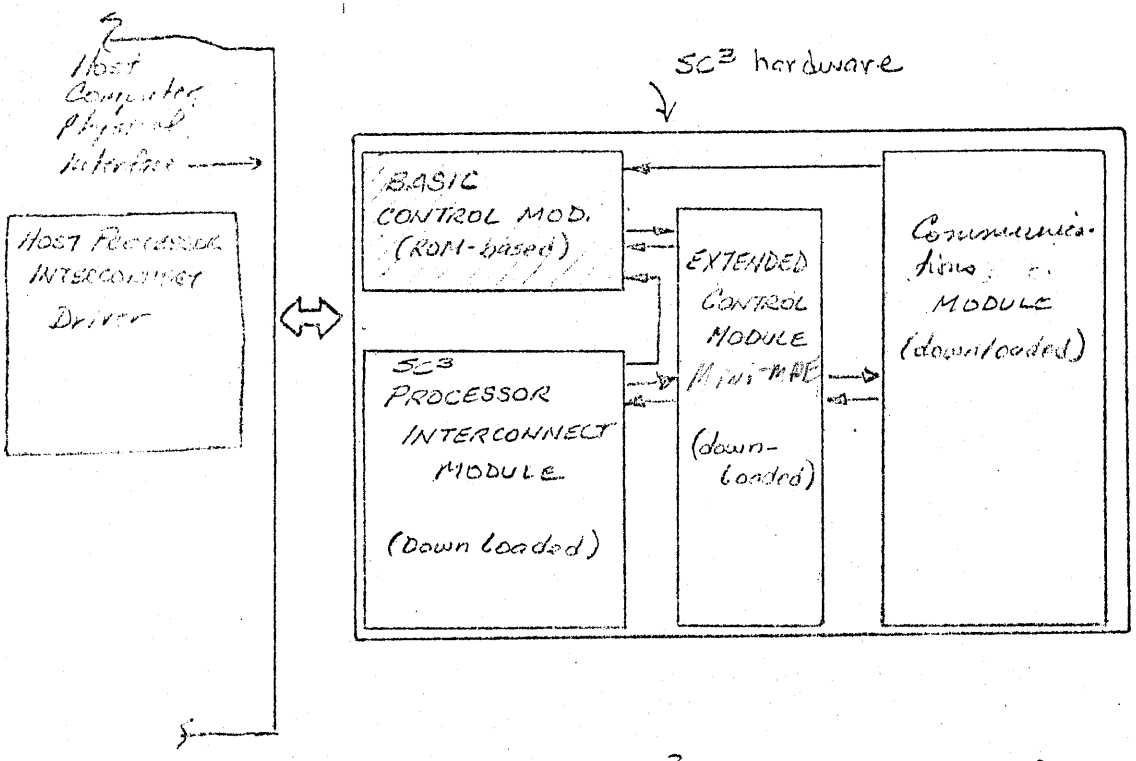

Communication Monitors
CS/3000
Communications Drivers
DSMON
RJE
MRJE
MTS
Intrinsics
SSLC
pt-pt BISYNC
Multileaved
Multipoint
HSI: pt-pt BISYNC
CLP

COMPARISON OF SOFTWARE STRUCTURE



S/W Changes
- downloading actual protocol into CLP memory. Errors on CLP dump on SYSDISC for analysis
- transmit/receive data simultaneously & Present PSC (COP) in half duplex, New BOP

SC³ -- TOP LEVEL SOFTWARE DESIGN



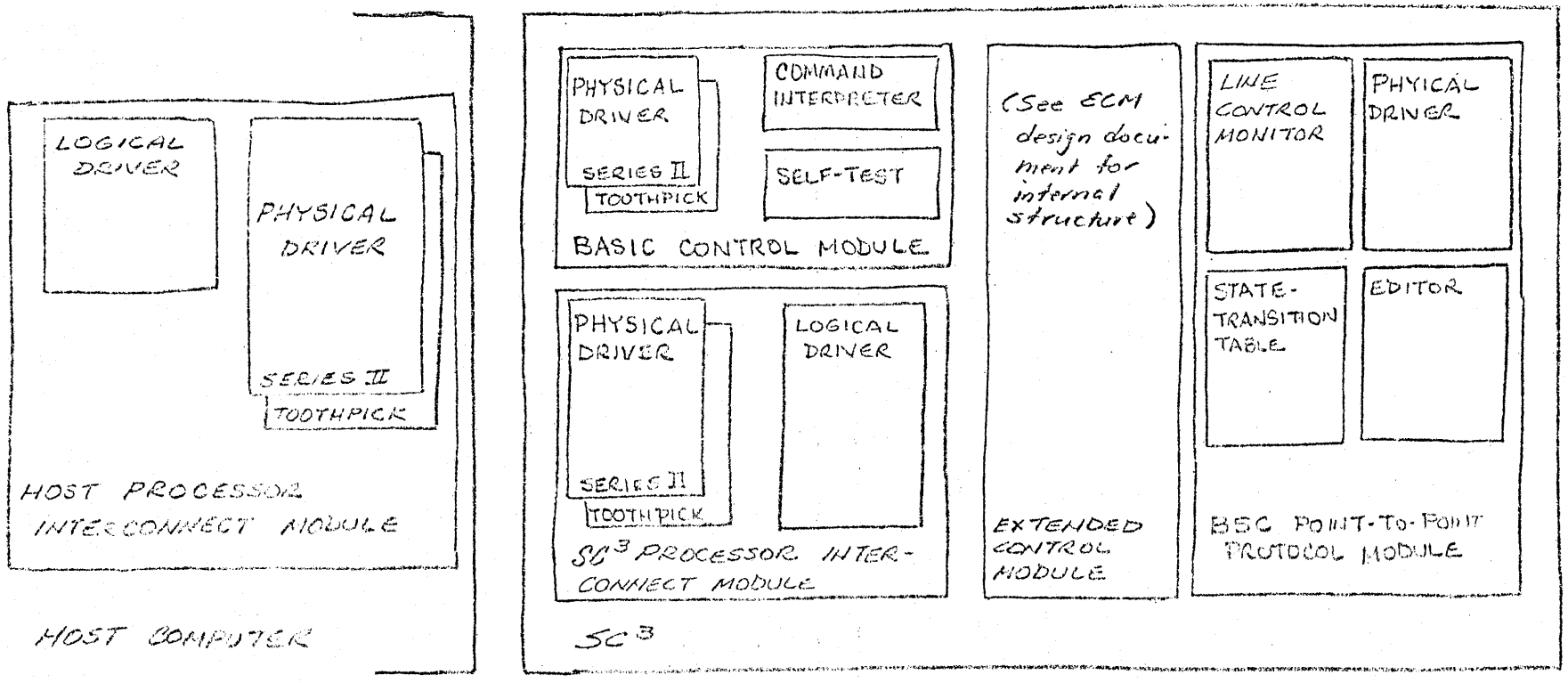
SC³ software has four primary modules. The Basic Control Module is stored in permanent Read-Only-Memory (ROM). The remaining modules are stored in Read-Write Random Access Memory (RAM) and are down-loaded when the communications sub-system is started.

Figure 3

CLP

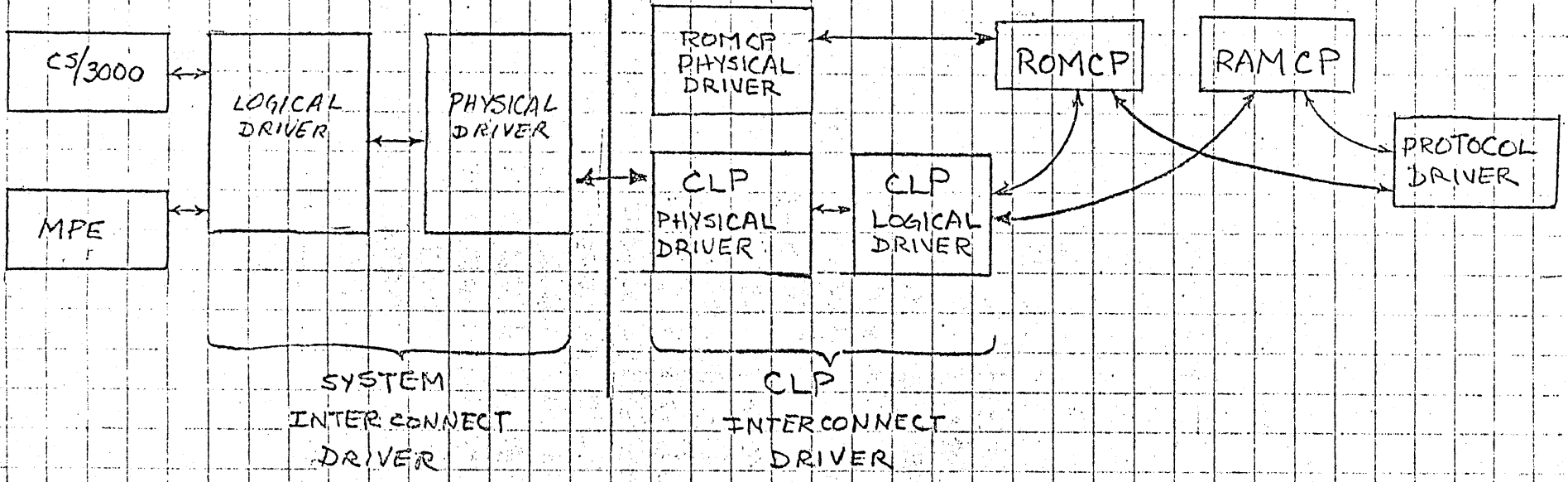
Figure Four

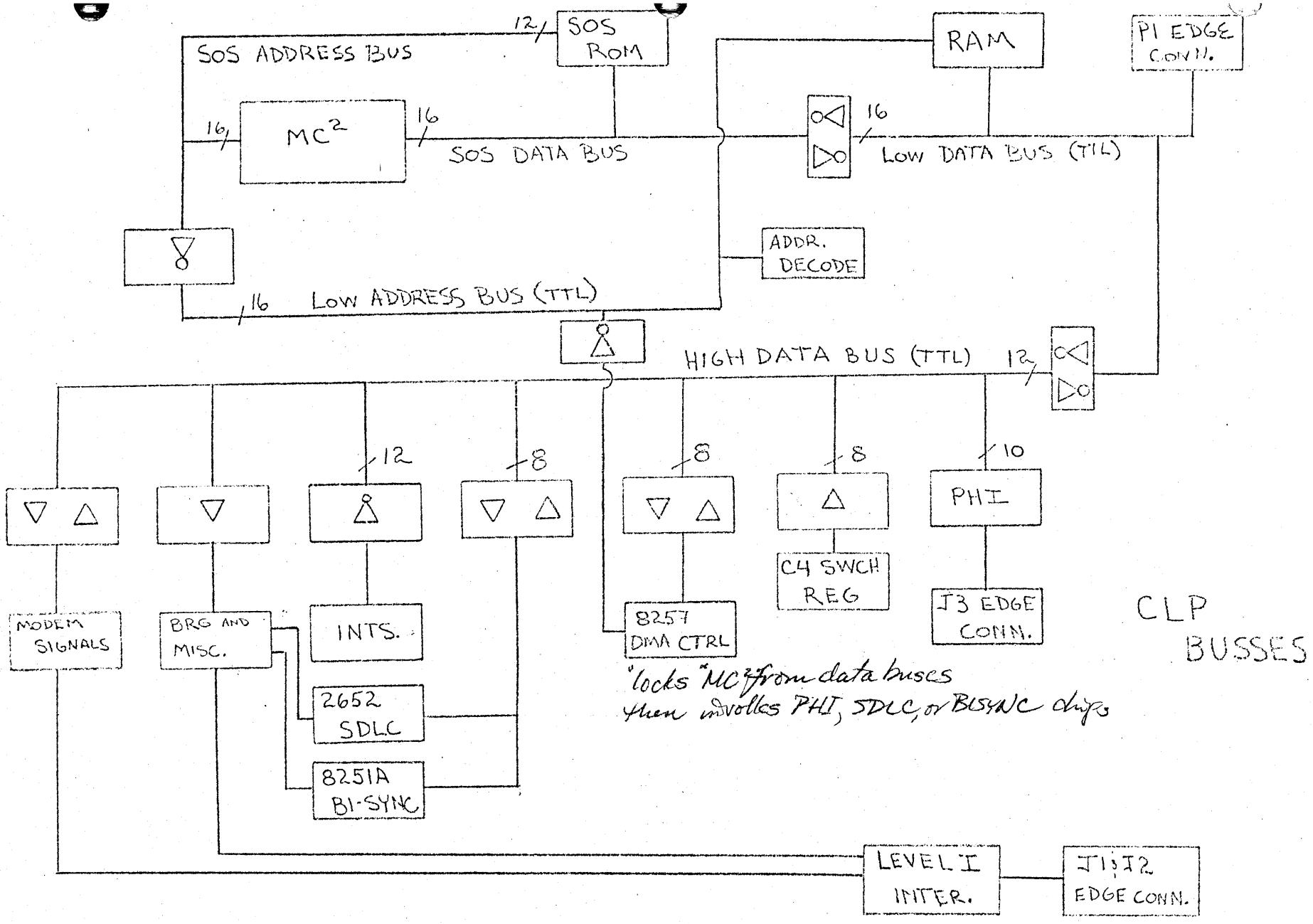
SC³ MODULE STRUCTURE



CLP80

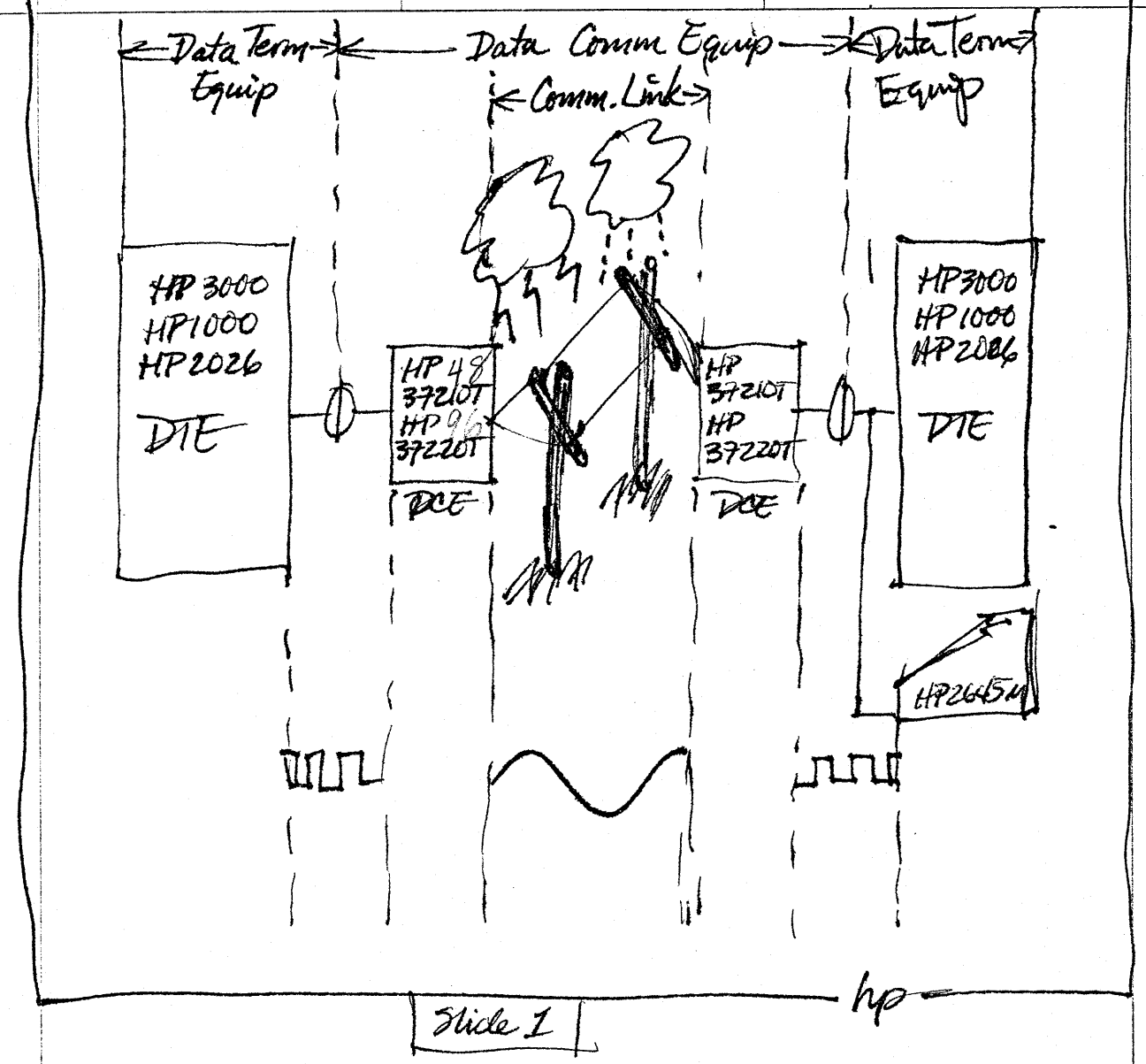
COMMUNICATIONS BETWEEN MODULES





CLP 12

12/4/78
DD

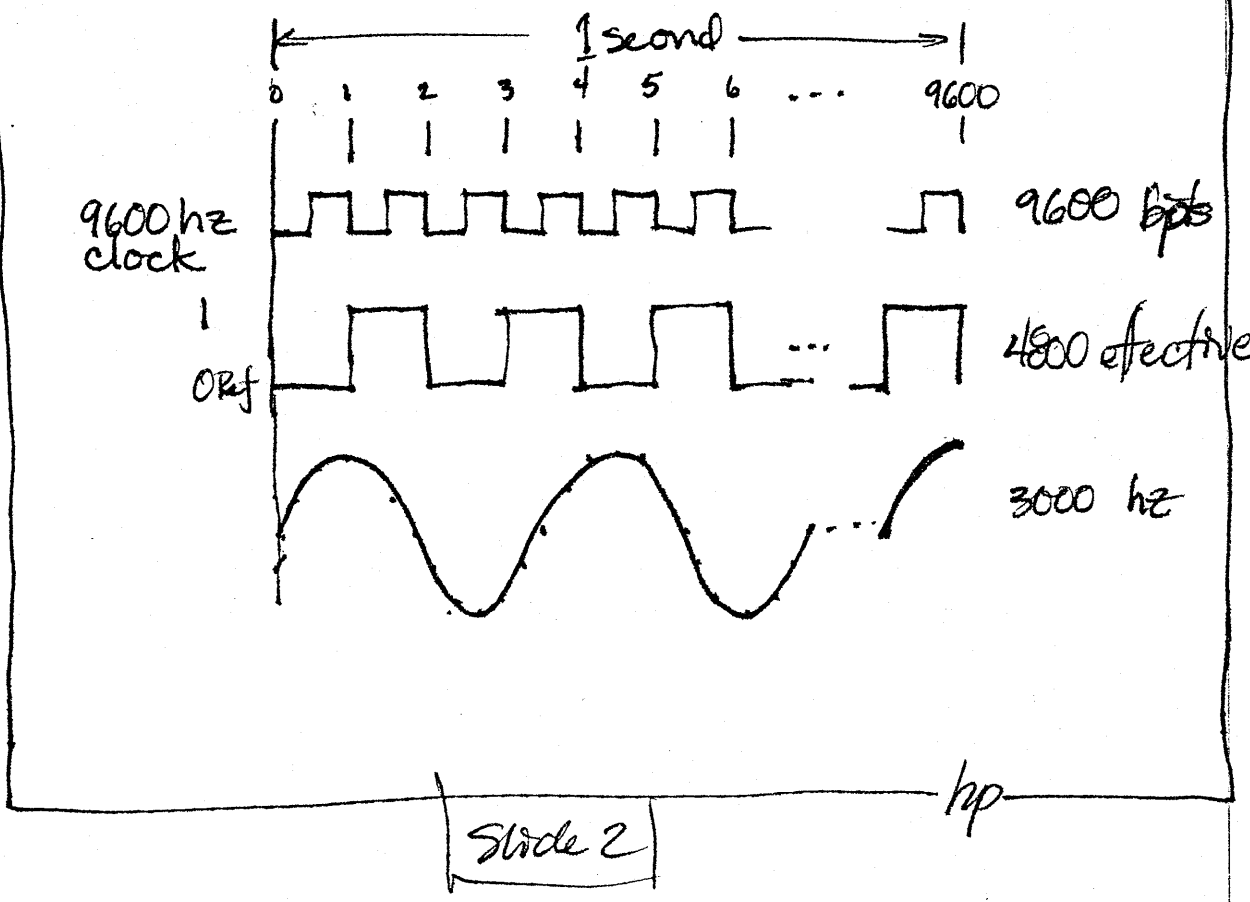


Slide 1

USA — 24

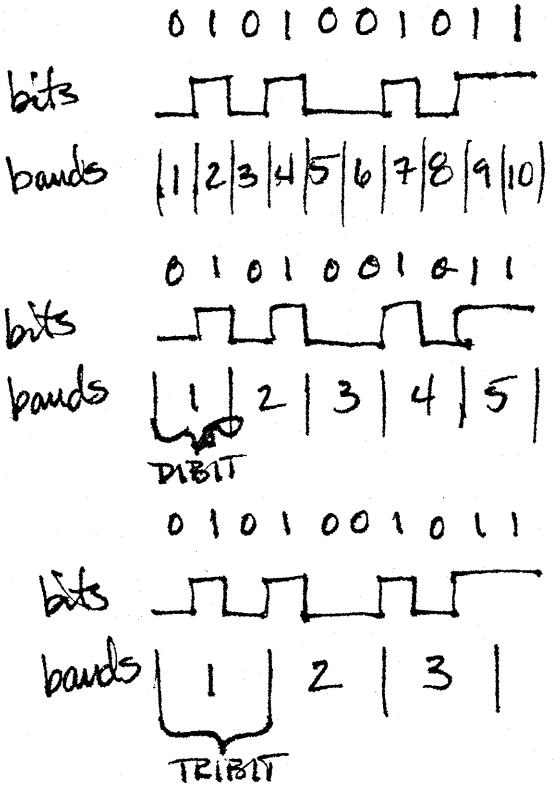
96 — 48

1500 Hz


1 second
0 1 2 3 4 5 6 ... 9600
9600 hz clock
9600 bps
1
0 Rf
4800 effective
3000 hz

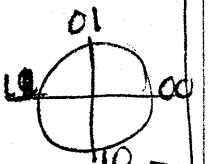
hp

Slide 2



2 state: Code Units {0, 1}

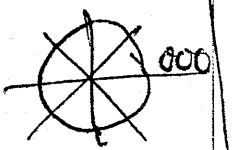
Baud = ~~BPS~~



4 state: ~~DIBIT~~

Code Units: {00, 01, 10, 11}

Baud = ~~BPS~~/2



8 state

Code Units: {000, 001, 010, 011, 100, 101, 110, 111}

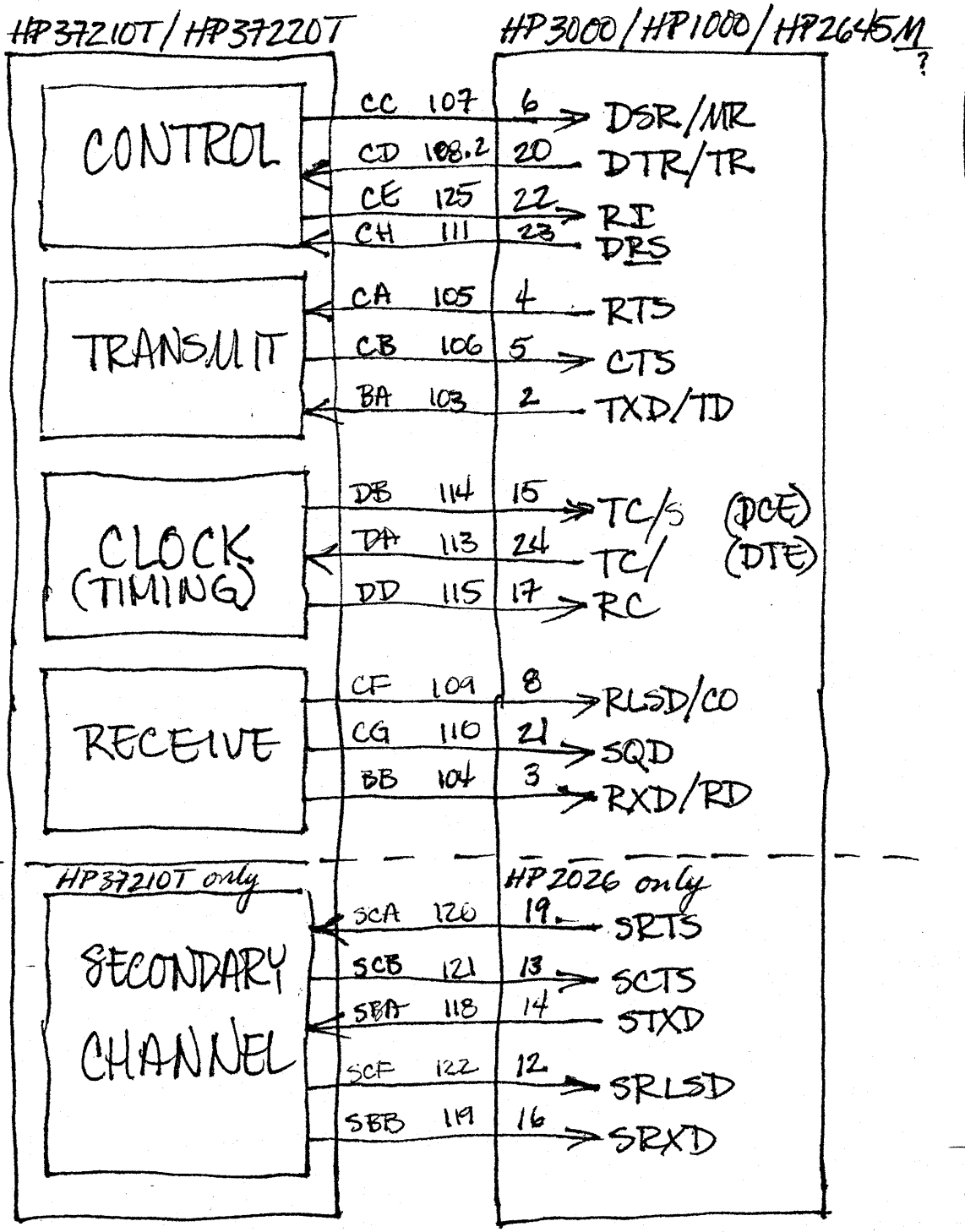
Baud = BPS/3

hp

Slide 3

Baud - line signal rate

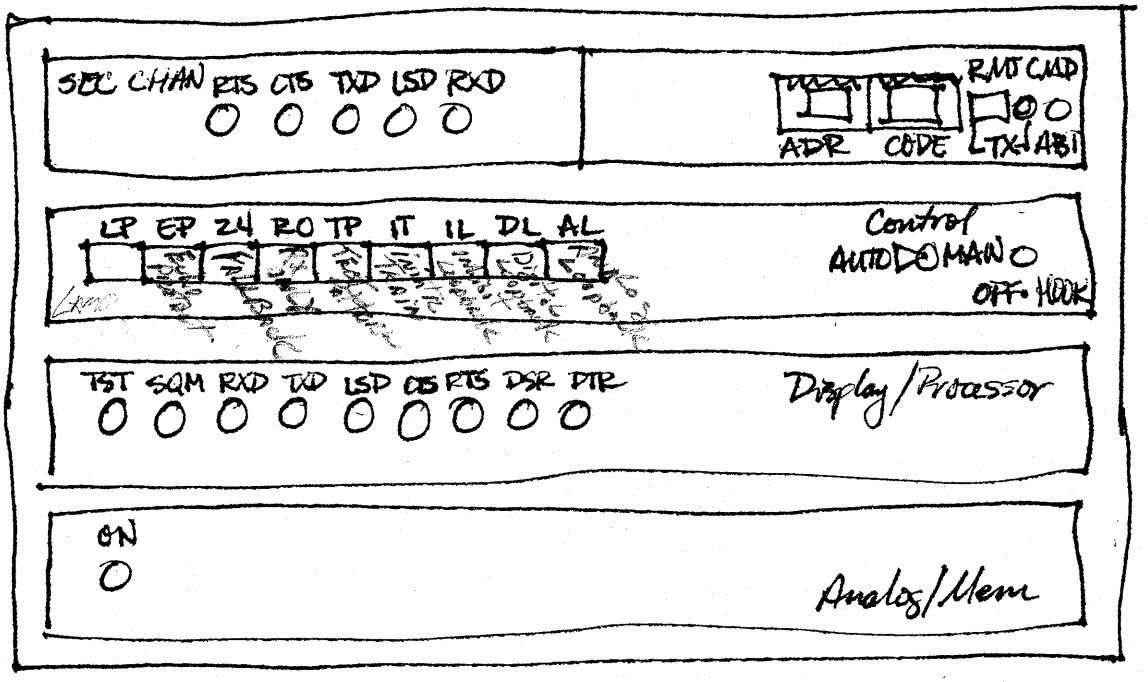
EIA RS-232C / CCITT V.24



hp

Slide 4

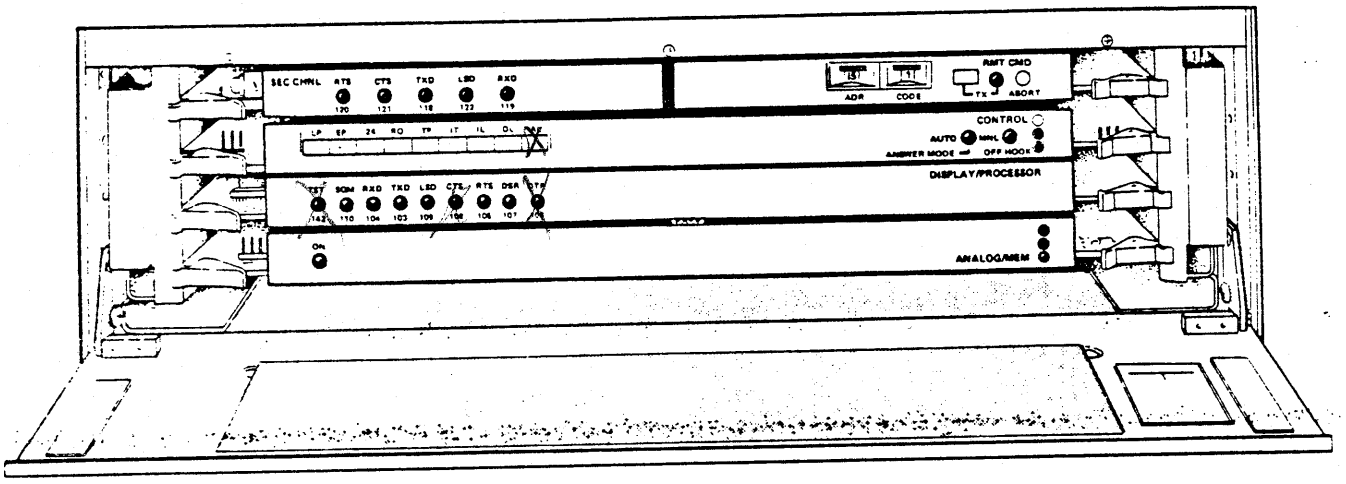
HP372TOT



hp

Slide 5

ON



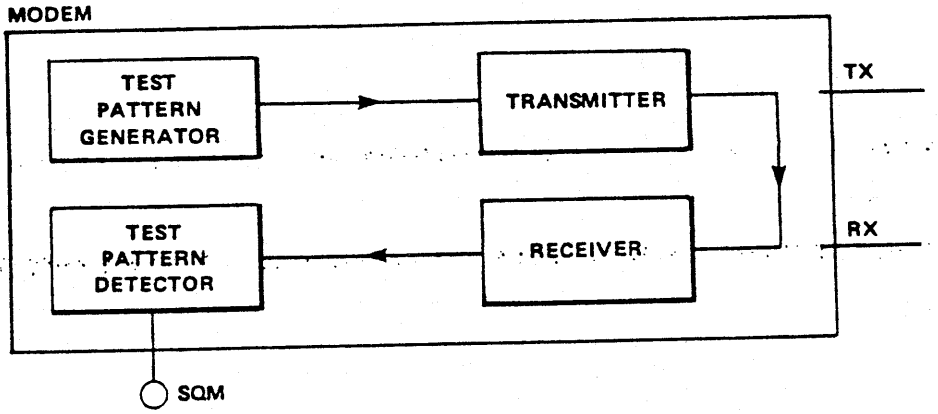
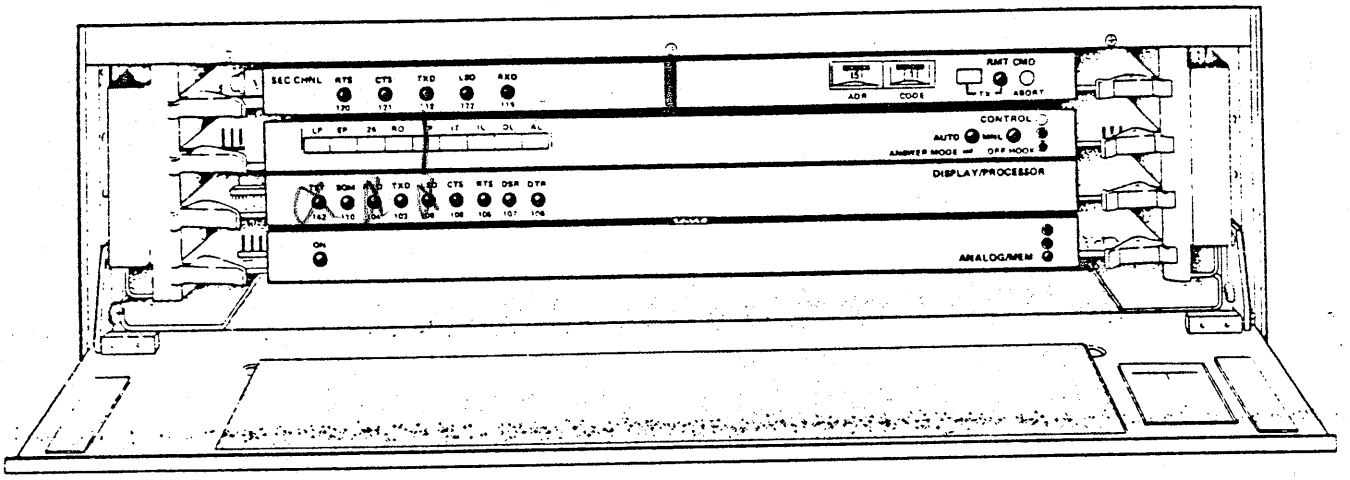


Figure 3-3 Analog Loopback Test



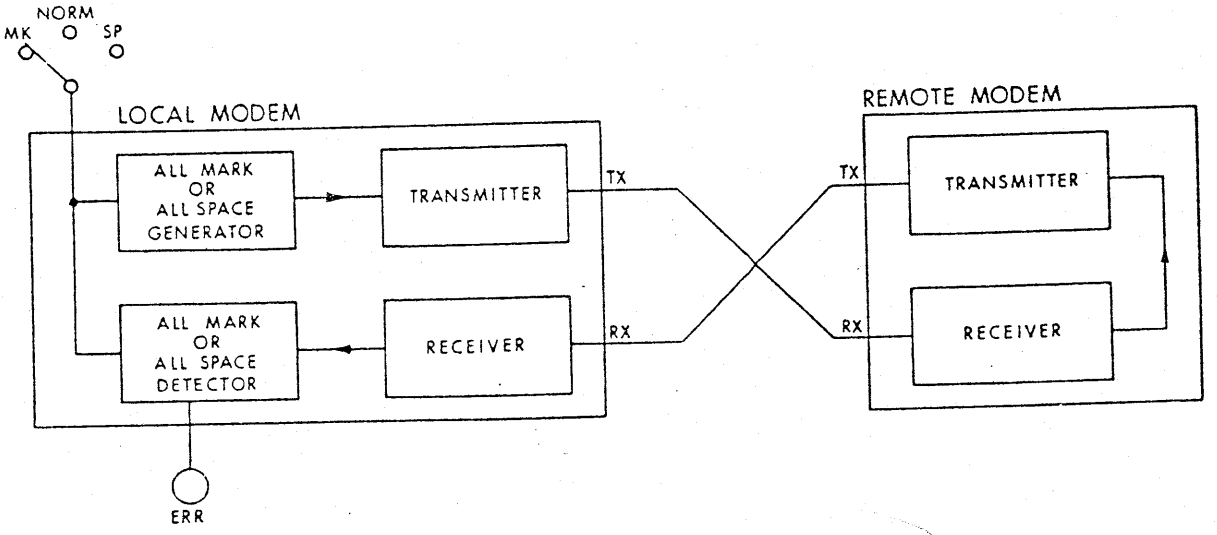
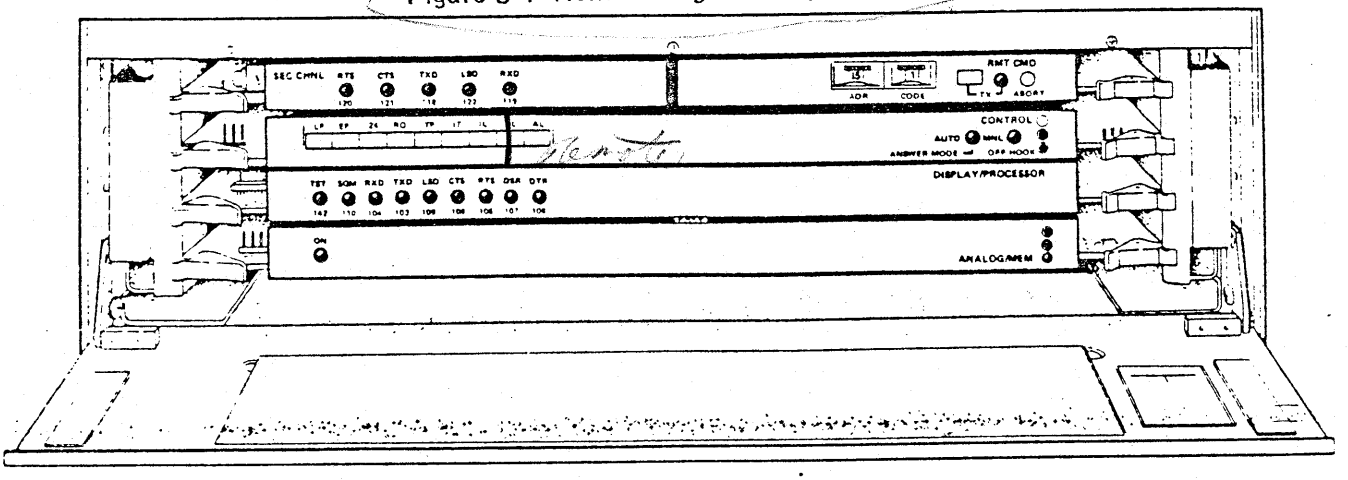
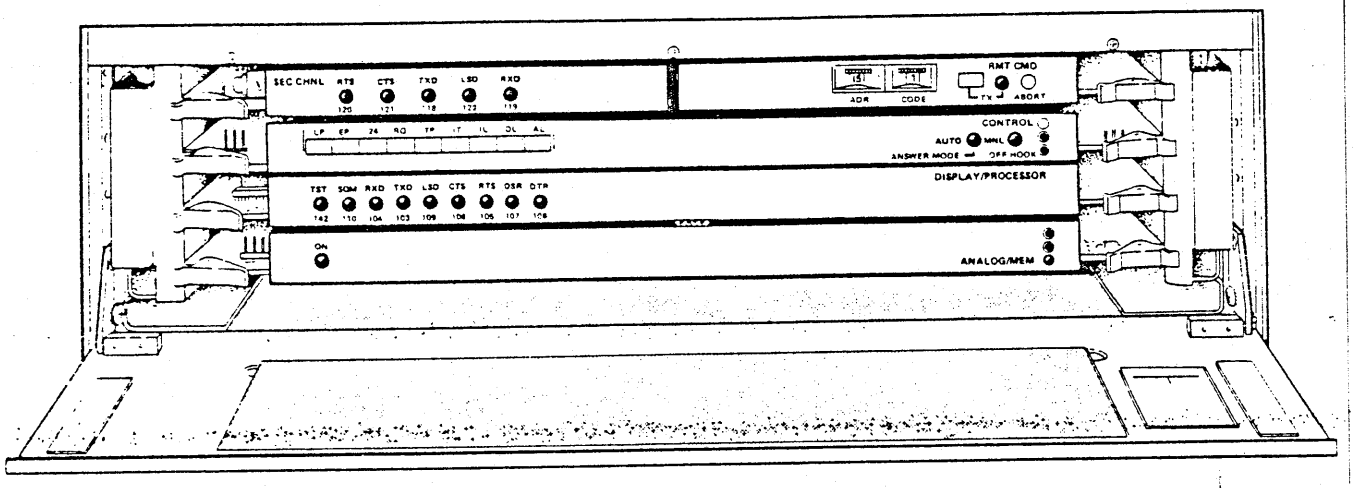


Figure 5-4 Remote Digital Loopback Test





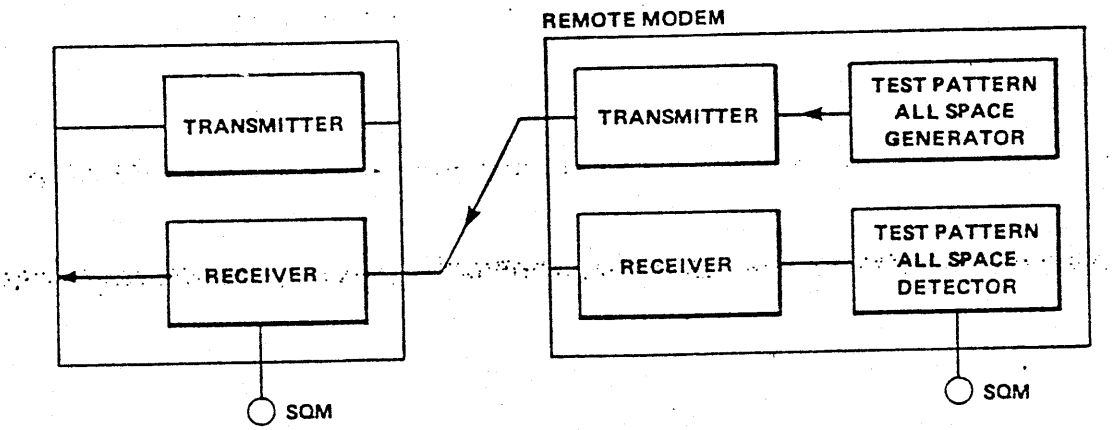
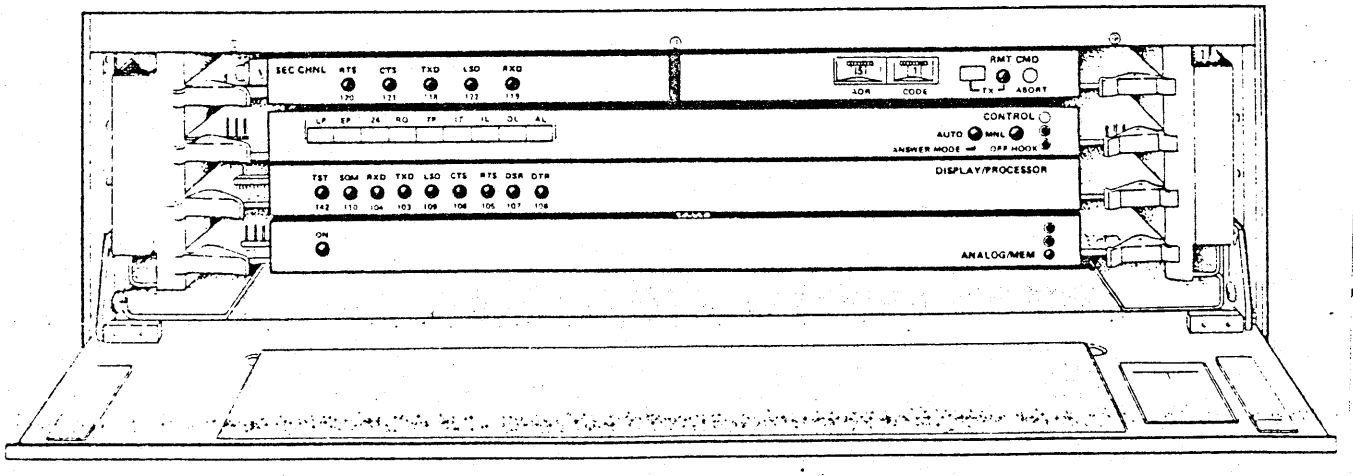


Figure 3-5 Receive Only Test Procedure



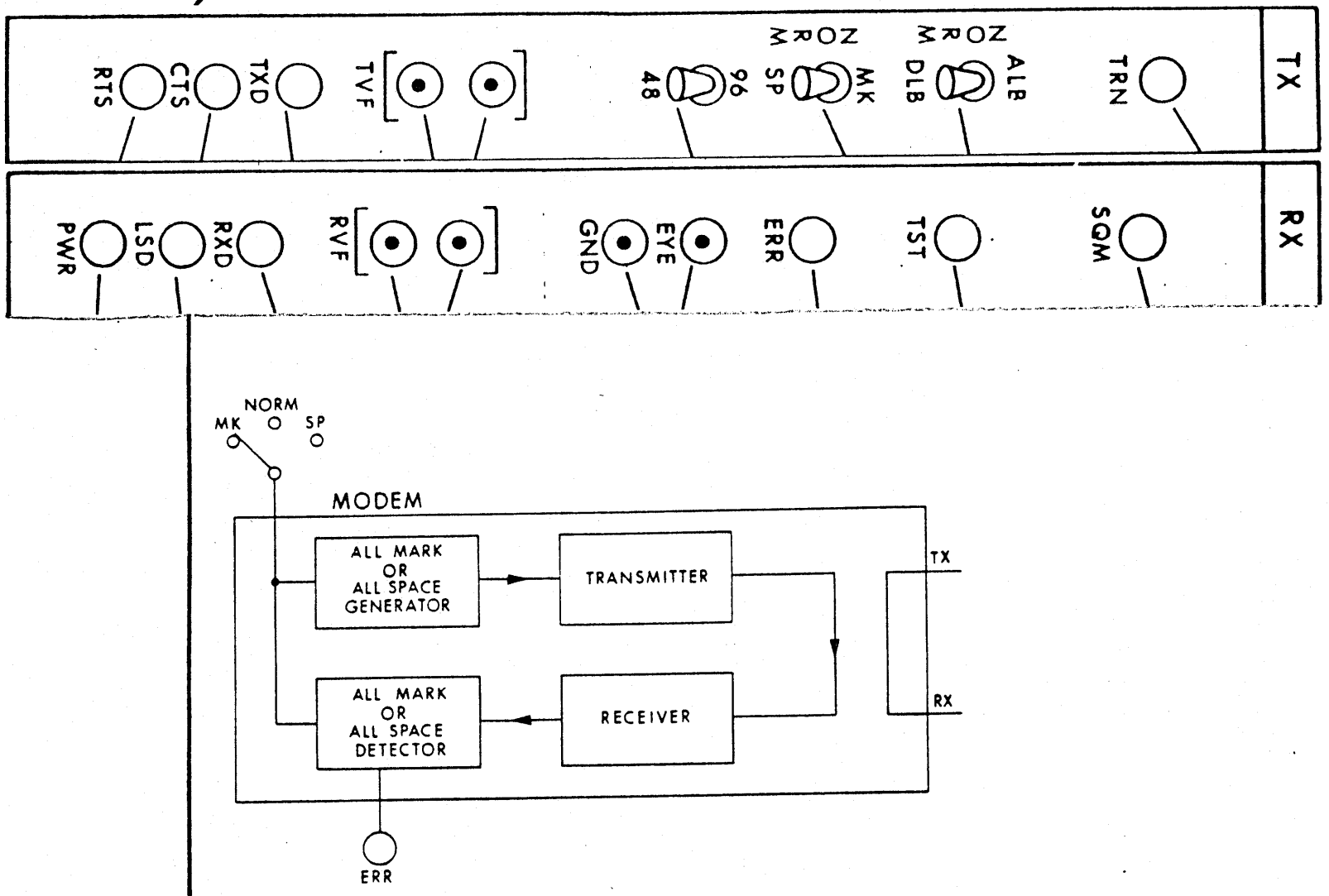


Figure 5-3 Local Analog Loopback Test

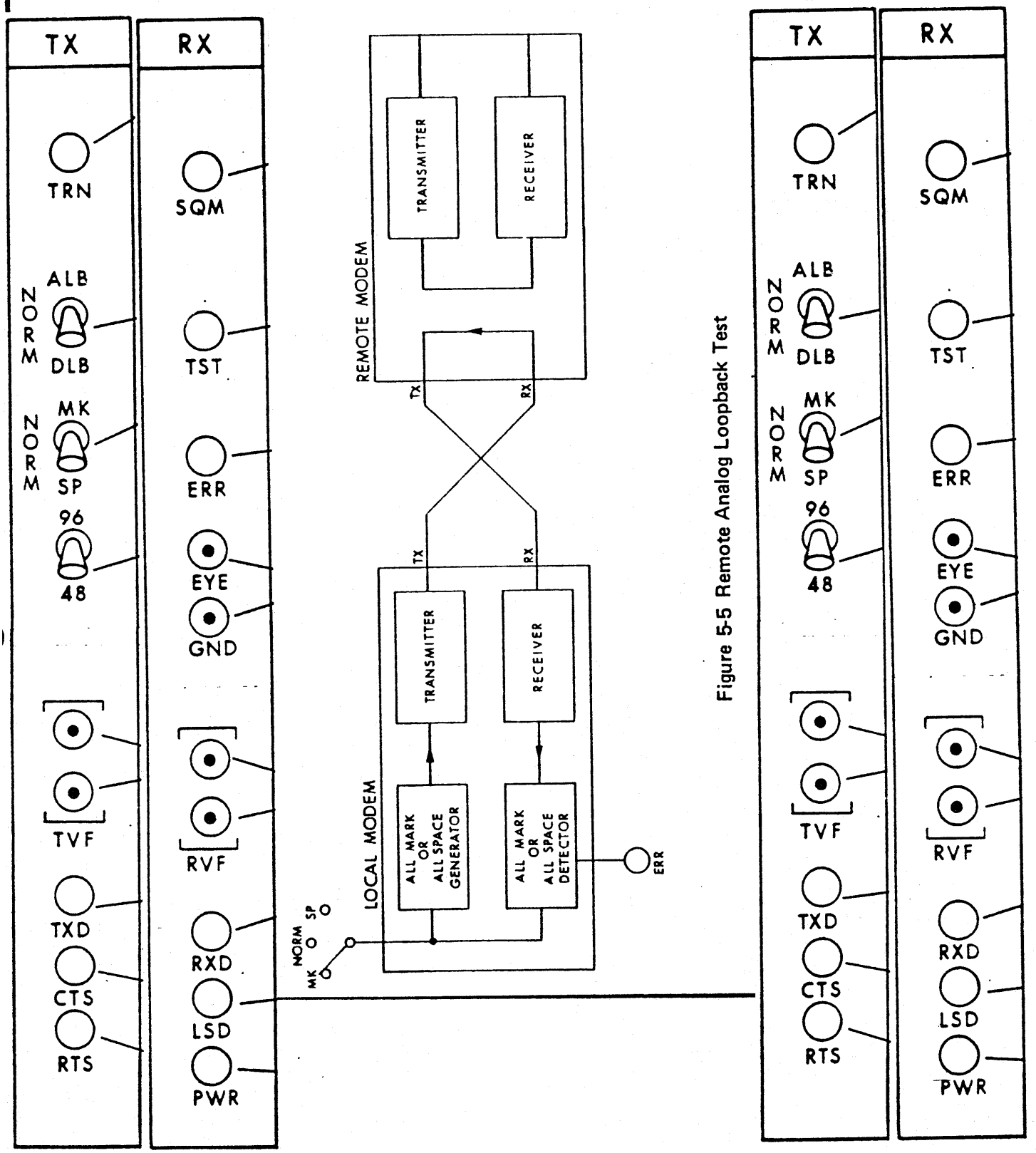


Figure 5-5 Remote Analog Loopback Test

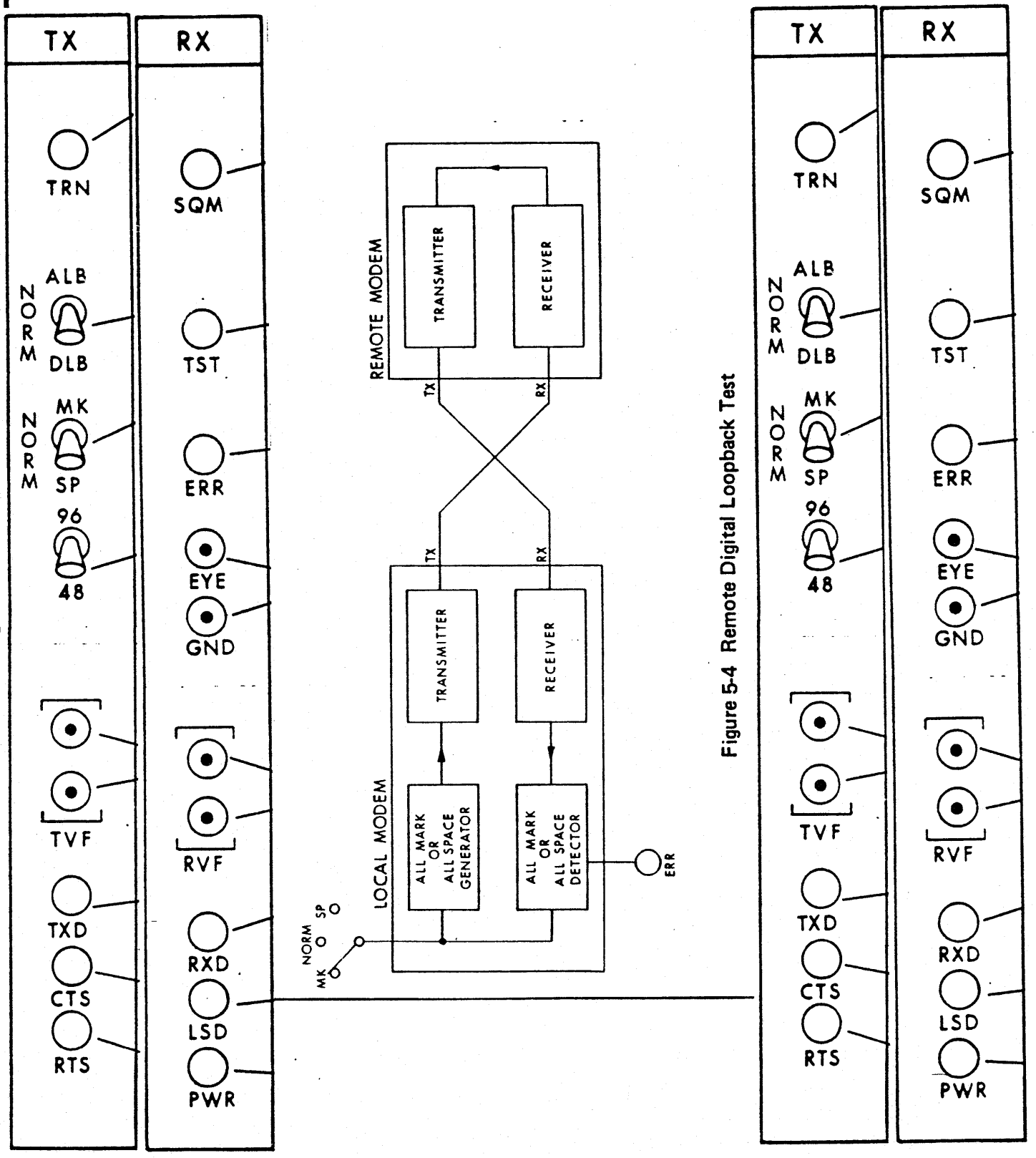


Figure 5-4 Remote Digital Loopback Test