



**HEWLETT
PACKARD**

Real-Time Emulator Intel® 8051

MODEL 64264S

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Description

Model 64264S Emulator provides real-time, transparent emulation for Intel 8051/8751/8031 microcomputer-based systems. As an integrated subsystem of the HP 64000 Logic Development System, the HP 64264S adds the power of emulation to all phases of 8051-product design, development, and maintenance.

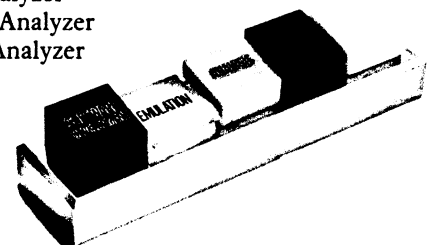
Model 64264S consists of an emulation control card, emulation pod, and operating system software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin, low-profile probe. A typical 8051 emulation system includes HP 64264S Emulation subsystem, HP 64156S Emulation Memory system, and HP 64302A Emulation Bus Analyzer. With this configuration the HP 64000 system's extensive set of development aids can be readily applied to 8051-based designs.

Directed syntax softkeys and an easy-to-use editor streamline software development and documentation. Logic software analysis and logic hardware analysis can be combined with emulation for an extra dimension of interactive measurements. Software performance measurements track total system activity, supporting optimum 8051 software designs for more efficient products. With Model 64264S emulator and the many compatible HP 64000 development tools, you can produce a better 8051-based product in less time, to gain a competitive edge.



Features

- Real-time execution up to 12 MHz independent of emulator/target system memory assignment
- Nonintrusive, real-time traces of 8051 activity for basic analysis and evaluation, including accesses to
 - Program memory
 - Internal and External data memory
 - Accumulator and Special Function Registers
 - I/O ports 0, 1, 2, and 3
- Disassembly of 8051 instruction set
- Program and External data memory mapped in 256-byte blocks to emulation or target system memory
- Comprehensive display and modify functions for all 8051 memory, I/O ports, and registers
- Expanded measurement systems through interactive operation with other HP 64000 subsystems
 - Another 8051 emulator or any other HP 64000 emulator
 - HP 64620S Logic State/Software Analyzer
 - HP 64600S Logic Timing/Hardware Analyzer
 - HP 64310A Software Performance Analyzer



Getting Started

Analysis and debugging can be applied immediately, with or without functional target system hardware. A 12 MHz internal clock and emulation memory provide real-time execution and evaluation as soon as the first code is written. Real-time operation is fully maintained to assure an accurate duplication of the final 8051-product performance.

Flexible mapping allows you to assign memory to the emulator or target system in 256-byte blocks. Program and External Data memory are mapped separately across the full 8051 address range (figure 1). The 256-byte blocks are a convenient size for transferring the newly developed resources from the emulation system to the target system efficiently.

Nonintrusive Analysis: A Must for Real-time Systems

Many 8051-based products are applied to controlling or monitoring real-time critical processes. With HP 64264S emulator, a designer is confident that the development tools do not perturb the 8051 system processes in any way. Data collection by the emulator supports a wide variety of real-time measurements, without intruding on target system operation. HP 64264S emulator monitors all 8051 data paths (including the internal data bus) nonintrusively and in real time.

Information monitored by the emulator is passed to the HP 64302A Emulation Bus Analyzer where trigger and storage directives are applied. Triggers are defined for any event and set for the start, center, or end of the trace measurement. Storage qualifiers let you specify which kinds of events are captured and stored in analyzer memory. Commands are entered with the softkeys, and the trigger and store specifications may include address, data, status, ranges, don't-care bits, and occurrence counts.

Access to the 8051 internal data bus is a key advantage for the designer. The unique capability of monitoring the internal bus nonintrusively lets you view all memory, as well as the contents of Accumulator and Special Function Registers each time one is accessed (figure 2).

entry	range	type	blocks
1	0- FF	prog	ROM USER
2	100- 3FF	prog	ROM EMUL 000-002
3	400- 4FF	prog	RAM EMUL 003-003
4	500- FFF	prog	ROM USER
5	F000-FFFF	prog	RAM EMUL 004-013
6	0- 1FF	data	RAM EMUL 014-015
7	200- 7FF	data	RAM USER
8	900- AFF	data	RAM EMUL 016-017

Emulation memory blocks: available* 40 mapped* 24 size* 256 bytes

STATUS: Default unspecified blocks: prog guarded; data user/rw _____ 3:55

0900H thru 0AFFH data emulation ram

__ADDRESS__ default delete _____ _start_ end_

Figure 1. Flexible mapping permits memory resources to be allocated in 256-byte blocks. Separate mapping of Program and External data memory into the prototype or emulation subsystem provides additional resolution.

time	address	opc	data	mnemonic	opcode or status	time, relative
-010	0111	05		INC 27H	= 04H	1. us
-009	0112	27		DEC B	= 50H	1. us
-008	0113	15		DEC B	= 50H	1. us
-007	0114	F0		MOV A,B	= 50H	1. us
-006	0115	E5		MOV A,B	= 50H	1. us
-005	0116	F0		MOV A,B		1. us
-004	0117	B4		CJNE A,#50H,0111H		1. us
-003	0118	50		MOV A,B		1. us
-002	0119	F7		MOV A,B		1. us
-001	011A	F0		MOVX @DPTR,A		1. us
0000	011A	F0		MOVX @DPTR,A		1. us
+001	011B	45		MOV A,B		1. us
+002	0315	50		MOV A,B	ext data write	1. us
+003	011B	45		ORL A,27H	= 54H	1. us
+004	011C	27		ORL A,27H		1. us
+005	011D	05		MOV 36H,DPL	= 15H	1. us

Trace: mnemonic break: none col: 1

STATUS: 18051--Running Trace Complete _____ 4:04

modify external_data_memory BUFF_START thru BUFF_END to 0

__run__ trace __step__ display modify break __+4__ __-Etc__

Figure 2. Access to the 8051 internal data bus allows Model 64264S to trace internal operations. A special advantage is real-time monitoring to view Accumulator and Special Functions Registers contents each time one is accessed.

Another distinct advantage of the HP 64264S emulator is tracing all four 8051 I/O ports. Since the data is extracted directly from the internal data bus, you know it is exactly the same data that the 8051 is operating on (figure 3).

Controlling Your 8051 System

Through the HP 64264S emulator, you have direct control over your evolving 8051 system. You can display and modify any register, memory location, or I/O port. Control the program flow with single-step, run-from, and run-until directives; run controls initiate or terminate program execution at a specified address or symbol.

Register displays are comprehensive, yet easily understood. For example, if a register contains individual control bits, the labels are shown on the display and included as softkey labels, further simplifying register-bit modifications (figure 4). Another display shows any memory location or range of locations as 8051 mnemonics, bytes and ASCII equivalents, or words and ASCII equivalents. Modifications are made by bytes or words; the 8051 bit-addressable memory may be modified by bit.

Advanced Analysis Power — from Micro to Macro Measurements

As your 8051 system grows, it becomes more complex and sophisticated. You can add correspondingly more sophisticated HP 64000 measurement systems as they are needed to serve new levels of analysis. Analyzers are available for the whole spectrum of logic measurements -- from a micro level for a bit-by-bit analysis to a total system performance analysis for the macro view.

As the target system hardware evolves, HP 64600S Logic Timing/Hardware Analyzer may be added to check timing relationships at speeds up to 400 MHz. Postprocessing captures and stores timing traces for detailed comparisons, statistical calculations, and documentation.

At the next level, HP 64620S Logic State/Software Analyzer supports intricate state analysis: up to 120 input channels, 15 levels of sequential triggering, broad definitions for storage qualifiers, and measurement window specifications. The HP 64620S analyzer can be added to the emulation system through the HP 64304A Emulation Bus Preprocessor, to enhance or replace the HP 64302A Emulation Bus Analyzer.

For optimizing and characterizing software performance, HP 64310A Software Performance Analyzer provides macro views of total system performance, by activity, interaction, or duration. The performance analyzer becomes an integral part of the emulation system, so you can begin optimizing your 8051 programs as soon as code exists.

Trace:	mnemonic	break: none	count:overflow				
addr	address	opc	data	mnemonic	opcode	or status	time, relative
+000	016D	F5	MOV P0,A	=	66H		
+001	016E	90				read	1. uS
+002	016F	E5	MOV A,P1	=	73H		<1. uS
+003	0170	90				read	1. uS
+004	0171	23	RL A	=	E6H		1. uS
+005	0172	F5				read	1. uS
+006	0172	F5	MOV P1,A	=	E6H		<1. uS
+007	0173	90				read	1. uS
+008	0174	E5	MOV A,P2	=	EFH		1. uS
+009	0175	A0				read	1. uS
+010	0176	65	XRL A,27H	=	30H		1. uS
+011	0177	27				read	<1. uS
+012	0178	E5	MOV A,26H	=	CDH		1. uS
+013	0179	28				read	1. uS
+014	017A	E5	MOV A,P3	=	55H		1. uS
+015	017B	B0				read	<1. uS

STATUS: 18051--Running Trace in process 4:12

trace before address program_memory BOOT or address external_NEW_data_memory
NEW_DATA data 6XH status read break-on trigger

run trace step display modify break end ---ETC---

Figure 3. The actual data operated on by the 8051 is displayed each time one of the ports is accessed. All four ports are supported.

8051 Registers(Hex)																					
A	R	DPTR	P1	P0	P3	P2	P1	P0	IP	IF	TMOD	TCON	T1	T0	SCON	SRUF	PSW	SP	next	PC	
75	F3	0315	EA	FE	36	86	38	75	E2	E2	02	08	0000	FF1D	02	FF	21	16		016F	
PC	016F	Opcode	E5	MOV	A,P1																
3B	F3	0315	EA	FE	36	86	38	75	E2	E2	02	08	0000	FF1D	02	FF	21	16		0171	
PC	0171	Opcode	23	RL	A																
76	F3	0315	EA	FE	36	86	38	75	E2	E2	02	08	0000	FF1D	02	FF	21	16		0172	
PC	0172	Opcode	F5	MOV	P1,A																
76	F3	0315	EA	FE	36	86	76	75	E2	E2	02	08	0000	FF1D	02	FF	21	16		0174	
PC	0174	Opcode	E5	MOV	A,P2																
86	F3	0315	EA	FE	36	86	76	75	E2	E2	02	08	0000	FF1D	02	FF	21	16		0176	

STATUS: 18051--Step Complete Trace Complete 4:20

modify register bit TF1 to 1

run trace step display modify break end ---ETC---

Figure 4. The comprehensive register display of allows examination and modification of all internal 8051 registers. Registers with specific control bits are supported by name on the HP 64000 softkeys for convenient modification.

For multiprocessor applications, the HP 64264S 8051 Emulator may be used interactively with any other HP 64000 system emulator with the Intermodule Bus (HP 64964A). The Intermodule Bus (IMB) also supports cross-triggering modes between analysis subsystems and emulators. The larger measurement system possible with the IMB is not restricted to analysis and emulation subsystems in a single development station; HP 64303A IMB Extender board gives you access to measurement systems resident in other development stations.

Making a Difference

Model 64264S emulator offers development support for all phases of 8051 microcomputer-based designs. HP 64000 tools have the flexibility, power, and convenience required for designing and implementing effective 8051-based products, quickly and efficiently. Friendliness and the powerful measurement systems of the logic development system foster good design practices and complete debugging, from the first design goal statements to the finished product.

Specifications

Processor compatibility: compatible with Intel 8051/8031/8751 microcomputers and any other processor that complies with the specifications of these devices.

ELECTRICAL

Maximum clock speed: 12 MHz.

Inputs: all inputs meet Intel specifications plus approx 40 pF capacitance; Port 0, low-level input, 0.45 mA; Port 1, Port 2, and Reset, low-level input, 0.1 mA; and EA, low-level input, 0.5 mA.

Power: 20 mA drawn from the target system; all other power supplied by the development station.

Ordering Information

Model 64264S 8051 Emulation Subsystem

Model 64156S Emulation Memory System with
memory control board and 32k-byte memory board

Model 64156S Option 011: expand to 64k-byte

Model 64156S Option 012: expand to 128k-byte

Model 64302A 48-channel Emulation Bus Analyzer

Model 64855A 8051 Assembler/Linker

COMPONENTS

Model 64263A 8051 Emulation Control Board

Model 64264A 8051 Emulation Pod (includes software)

PHYSICAL

Cable length: development station to emulation pod, approx 1.5 m (5 ft); emulation pod to target system interface, approx 305 mm (1 ft).

ENVIRONMENTAL

Temperature: operating, 0° to +40° C (+32° to +104° F); nonoperating, -40° to +75° C (-40° to +167° F).

Altitude: operating, 4600 m (15 000 ft); nonoperating, 15 300 m (50 000 ft).

Relative humidity: 5% to 80%.

ACCESSORIES SUPPLIED

Model 64264S 8051 Emulator includes an emulation control board (Model 64263A) and an emulation pod (Model 64264A); appropriate cables for connections from control board to the pod and from the pod to the target system; operating software supplied on flexible disc; and operators manual.