64000

HP64000 Logic Development System

Model 64151A Emulation Memory Controller

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

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THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW&A 2/81

SERVICE MANUAL

MODEL 64151A
EMULATION MEMORY CONTROLLER

REPAIR NUMBERS

This manual applies directly to Model 64151A Emulation Memory Controllers with repair number prefixes of **2153A.** With changes described in Section VII, this manual also applies to Model 64151A's with repair number prefixes of **2108A** and **1924A.**

Manual Part Number 64151-90901
Microfiche Part Number 64151-90801

PRINTED: MAY 1982

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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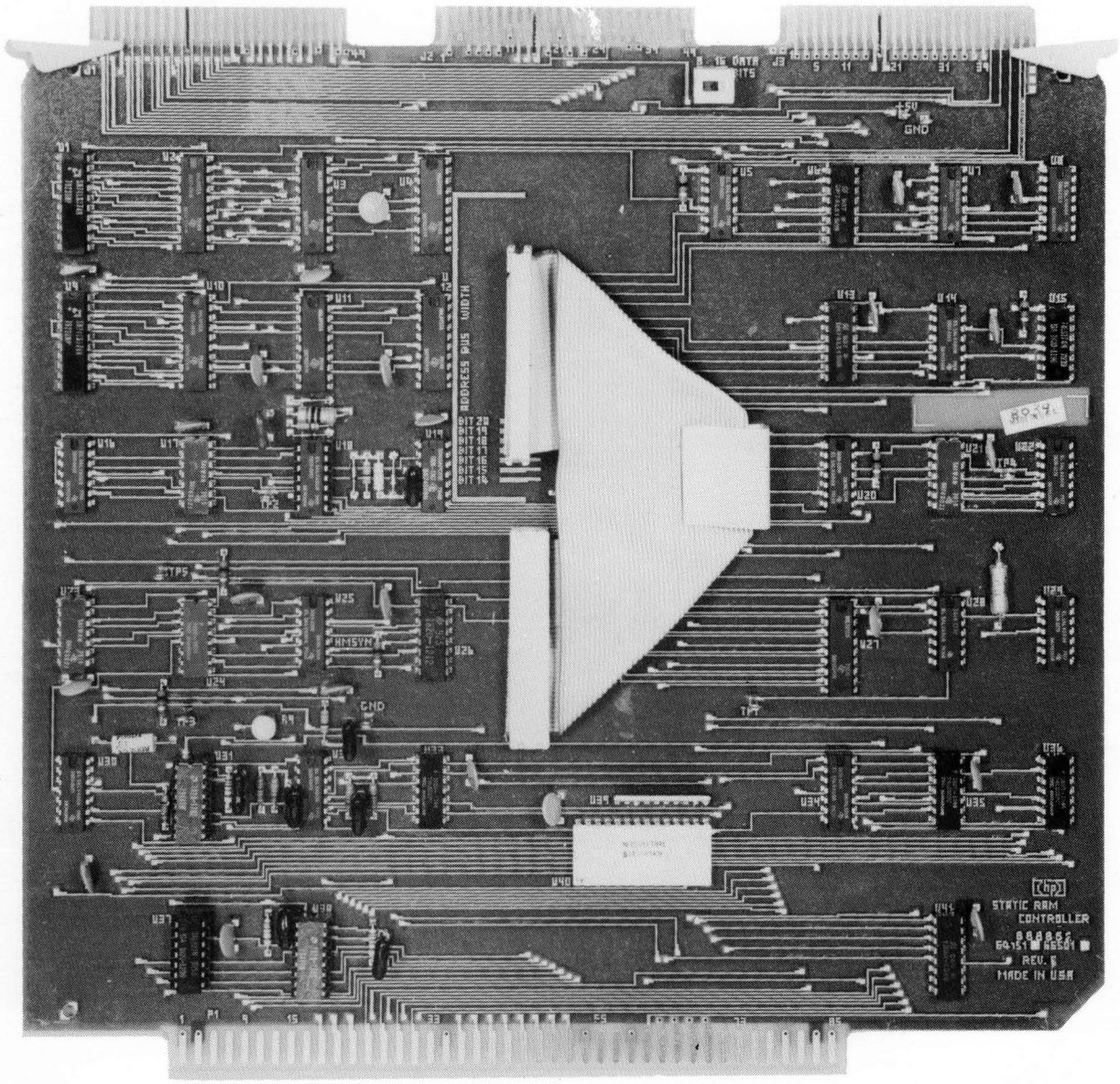


Figure 1-1. Model 64151A Memory Controller

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This service manual contains technical information concerning the application, troubleshooting, and theory of operation for the Model 64151A Emulation Memory Controller as used in the HP 64000 Logic Development System. Figure 1-1 is an illustration of the Model 64151A Memory Controller.

1-3. SAFETY CONSIDERATIONS.

1-4. There are no electrical shock hazards associated with this PC board since there are no high voltages present. There are, however, high voltages associated with the 64000 Mainframe and appropriate warnings are given where a hazard may exist.

1-5. INSTRUMENTS COVERED BY THIS MANUAL.

1-6. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the repair prefix, and the last five are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed on the title page.

1-7. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual for the newer instrument.

1-8. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard Sales/Service Office.

1-9. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Sales/Service Office.

1-10. DESCRIPTION.

1-11. The Model 64151A Emulation Memory Control Board drives the Emulation Memory Boards for the purpose of storing and retrieving emulation data from both the host processor and the target system. Up to 64k words can be mapped in any location in memory as ROM, RAM or illegal memory as defined by the user. Mapping control is provided by the Memory Control Board.

1-12. ACCESSORIES SUPPLIED.

1-13. The 64151A Emulation Memory Controller is supplied with one (1) 8120-3351 bus cable; and two (2) 8120-3352 bus cables, which are used to connect the Memory Controller to the Emulation Control Board, Analysis Module, and Static RAM Boards. Installation of these cables is covered in Section II.

1-14. ADDITIONAL EQUIPMENT REQUIRED.

1-15. The Model 64151A Emulation Memory Controller must be installed in a Model 64000 Mainframe with a minimum of one Static RAM Board (Models 64152B, 64153B, or 64154B) to have a functional emulation memory subsystem.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section provides installation instructions for the Model 64151A Emulation Memory Controller. Also included is information concerning initial inspection, damage claims, environmental considerations, and storage and shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents have been checked for completeness and the Model 64151A has been checked mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the Model 64151A does not pass performance verification, notify the nearest Hewlett-Packard Sales/Service Office. If the shipping container or cushioning material is damaged notify the carrier as well as the Hewlett-Packard Sales/Service Office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. INSTALLATION.

2-6. The Model 64151A Emulation Memory Controller is installed using the following procedure. Figure 2-2 shows the recommended location of the emulation option boards for two typical configurations: Emulation Memory only and Emulation Memory with Analysis.

NOTE

There must be one Memory Controller for every four Emulation Memory Boards, regardless of the amount of memory per board.

a. Turn off power to the 64000 station.

b. Loosen the two hold-down screws and remove the card cage access cover.

c. Set the "Data Bits" switch (S1) on the Emulation Memory Controller to the proper data bus width of the emulation processor: 8 bits wide or 16 bits wide.

d. Set the "Address Bus Width" jumper cable on the Emulation Memory Controller to "16" by moving the jumper cable connector vertically on the male connector block (J4) until the dash next to "16" just appears underneath the cable connector. Refer to figure 2-1.

e. Determine whether it is desired to have the Model 64151A cause an emulation break on a Write to ROM. If so, move R23 so that U27 pin 3 and U23 pin 3 will be connected via R23 (R23 horizontal on board, refer to figure 2-3). If the break on Write to ROM feature is to be disabled, then move R23 so that U23 pin 3 will be connected to +5 volts via R23 (R23 vertical on board, refer to figure 2-3). Refer to Section IV for information on the implications concerning this modification as related to Emulation Memory Controller Performance Verification. Note that this modification is only applicable to certain repair prefix numbers; refer to Section VII.

f. Making sure that the component side of the Emulation Memory Controller Board faces the front of the 64000 station, align the board with the card guide rails of the selected installation slot (figure 2-2) and press down the board until the P1 connector (large edge connector on board) seats in the motherboard connector of the mainframe.

g. Install the selected Emulation Memory Boards (8k,16k, or 32k) by repeating step "f" the appropriate number of times. Note that the maximum number of 32k memory boards for an 8-bit user system is two, which gives an emulation memory capacity of 64 kilobytes. The maximum number of 32k memory boards for a 16-bit user system is four, which gives an emulation memory capacity of 128 kilobytes.

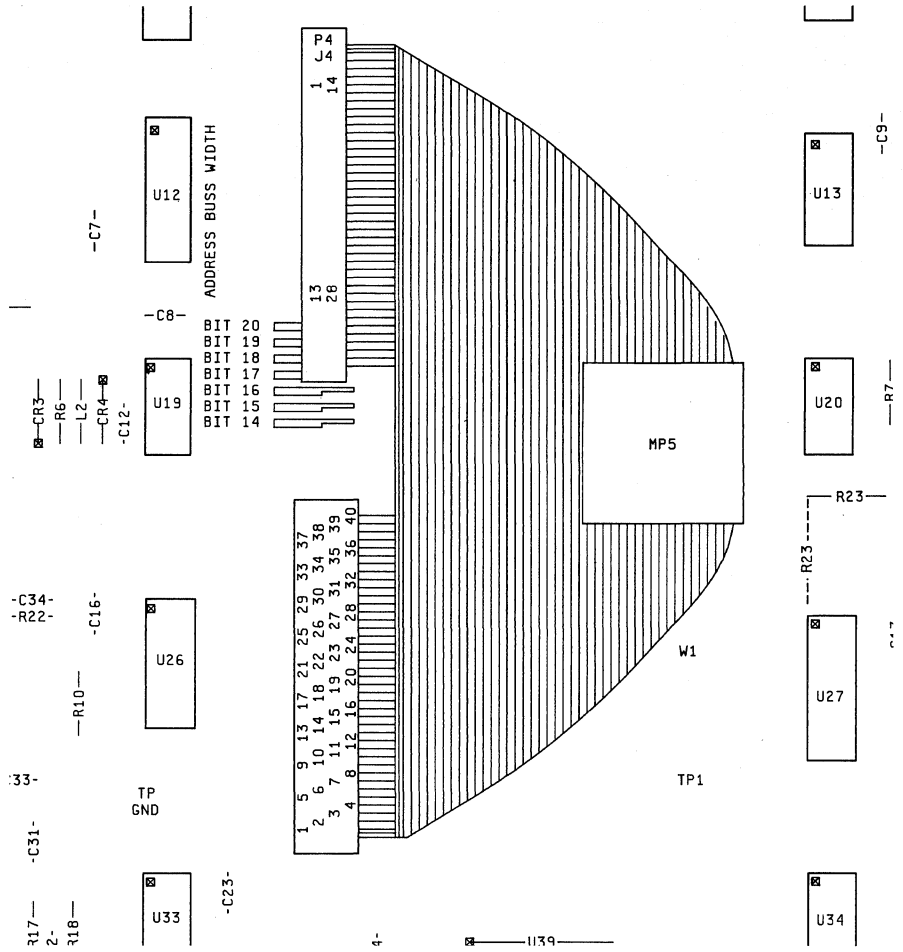


Figure 2-1. Address Bus Width Selection

h. Connect the Emulation Memory Bus ribbon cable across the left-hand set of edge connectors (as you face the front of the development station). The bus cable is keyed so that it will fit on the edge connectors in only one position.

i. Connect the Emulation Bus cables across the two right-hand sets of edge connectors (as you face the front of the development station). The bus cables are keyed so that they will fit on the edge connectors in only one position.

j. Reinstall the card cage access cover and tighten the 2 screws.

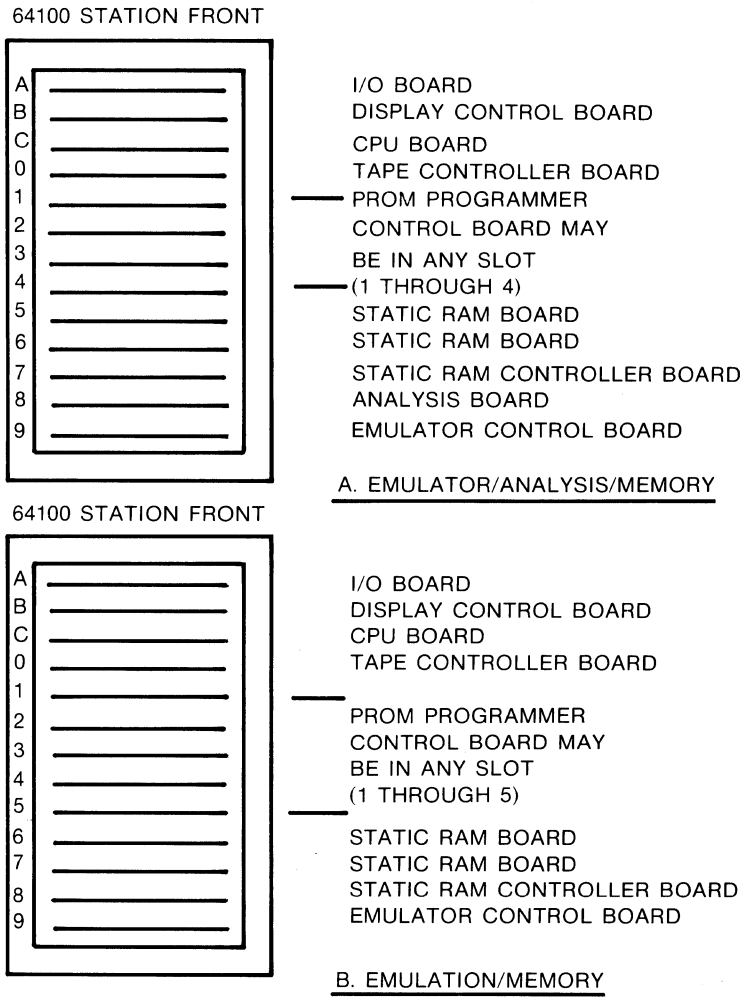


Figure 2-2. Recommended Card Cage Configuration

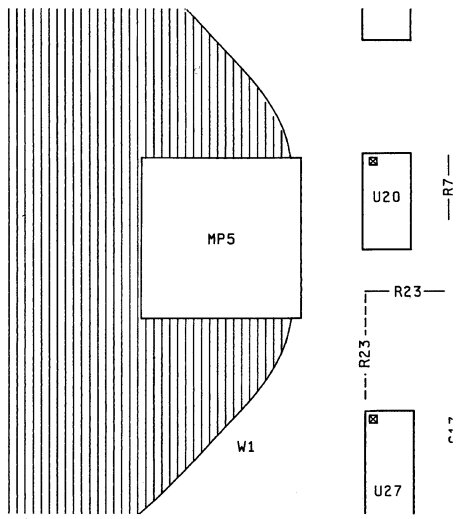


Figure 2-3. Write to ROM Jumper Position

2-7. REMOVAL.

2-8. Removal of the Model 64151A Emulation Memory Controller is covered in the following procedure.

a. Turn off power to the 64000 station.

b. Loosen the two hold-down screws and remove the card cage access cover.

c. Remove the two Emulation Bus ribbon cables.

d. Remove the Memory Bus ribbon cable.

e. Pull up on the two extractor levers until the Memory Controller clears the card cage.

2-9. OPERATING ENVIRONMENT.

2-10. The Model 64151A may be operated in environments within the following limits:

Temperature	0°C to +40°C
Humidity	5% to 80% relative humidity at +40°C
Altitude	4 600 m (15 000 ft)

It should be protected from temperature extremes which cause condensation within the instrument.

2-11. STORAGE AND SHIPMENT.

2-12. ENVIRONMENT.

2-13. The Model 64151A may be stored or shipped in environments within the following limits:

Temperature	-40°C to +75°C
Humidity	5% to 80% relative humidity
Altitude	15 000 m (50 000 ft)

2-14. ORIGINAL PACKAGING.

2-15. Containers and packing materials identical to those used in factory packaging are available through Hewlett-Packard Sales/Service Offices.

2-16. OTHER PACKAGING.

2-17. The following general instructions should be used for re-packing with commercially available materials:

a. Wrap the Model 64151A in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the Model 64151A to provide firm cushioning and prevent movement inside the container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to insure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

SECTION III

OPERATION

The operation of the Emulation Memory Controller Board is transparent and thus requires no interaction with the operator. Refer to the Emulator/Analyzer Operator's Manual for a complete explanation of emulation operation and partitioning memory space.

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. This section describes the Performance Verification (PV) for the Model 64151A Emulation Memory Controller. The PV procedures are in support of the Hewlett-Packard Blue Stripe exchange program; therefore, troubleshooting procedures are given to the board level only.

4-3. For convenience, the figures for the PV are grouped together at the end of this section.

4-4. TROUBLESHOOTING FLOWCHART.

4-5. Figure 4-1 is a flowchart which should be used when troubleshooting an Emulation Memory System which seems to be defective.

4-6. PERFORMANCE VERIFICATION.

4-7. The PV for the Model 64151A Emulation Memory Controller is a subset of the 64000 system option_test PV. The option_test PV tests all possible option modules that can be configured within the expansion slots of the 64000 Mainframe.

4-8. To test the Model 64151A Emulation Memory Controller, proceed as follows:

a. With the operating system initialized and awaiting a command, manually type or use the softkey:

option_test RETURN

Refer to figure 4-2.

b. The PV software will now display a directory of the installed option boards and their card slot number (refer to figure 4-3). Locate the "Static Memory" and enter the card slot number. For example, in figure 4-3 the Static Memory is in card slot number 7. Therefore, enter:

7 RETURN

c. A menu will now be displayed listing the three major tests available to exercise the Model 64151A (refer to figure 4-4). The test that is highlighted is the one that will be run if the **start** softkey is pressed. If a test other than the one that is highlighted is desired, press the **next test** softkey. The **next test** softkey is used to step through the tests displayed on the menu. To cause the option_test software to automatically execute each test in sequence, press the **cycle** softkey. The **next test** softkey can be used to exit the cycle mode.

d. Cycle through the Model 64151A PV tests. If no failures are observed, the Model 64151A operates correctly, and the testing may be terminated as described in the next paragraph. If a failure is observed, use the test descriptions given in the following sections along with the troubleshooting flowchart to isolate the failure.

e. To terminate execution of the Static RAM PV, press the **end** softkey. This returns the display to the Option Test PV card slot directory. If end is pressed at this level, the Option Test PV is completely exited and the system is returned to the awaiting command status.

4-9. PROCESSOR CONTROL TEST. (Figure 4-5.)

4-10. Purpose — verifies that the mainframe CPU interface circuitry on the Model 64151A and also verifies that the static RAM boards work correctly.

4-11. What — The mainframe CPU programs the memory mapper on the Model 64151A, then writes data to blocks of emulation memory. The CPU then reads the data back and compares it with the data written.

4-12. Results — A hexadecimal status word is formed for each block of memory, indicating which bits of data failed by placing a "one" in the appropriate bit position of the status word. The status is decoded as follows:

	HEX	BINARY			
Error	0000 =	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
		P O N M	L K J I	H G F E	D C B A

Where
A = D0
B = D1
C = D2
D = D3
E = D4
F = D5
G = D6
H = D7
I = D8
J = D9
K = D10
L = D11
M = D12
N = D13
O = D14
P = D15

For example, if the status message reads "Error = 1248", then D3, D6, D9 and D12 are bad.

4-13. Troubleshooting — A failure in this test is most likely to occur on the Model 64151A or a Static RAM Board. Use the Troubleshooting Flowchart (figure 4-1).

4-14. EMULATION BUS TEST. (Figure 4-6.)

4-15. The Emulation Bus Test consists of two subtests: Data and Address. Each is described in the following paragraphs.

4-16. DATA.

4-17. Purpose — to verify that data bus communication is possible between the emulation control board and the Model 64151A Emulation Memory Controller.

4-18. What — The mainframe CPU starts this test by mapping two 1k blocks of emulation memory at opposite ends of a 64k address range. The CPU then writes data in a walking one/zero pattern to these two blocks of memory through the Memory Controller. The emulation control board is then directed to read this data and the mainframe CPU verifies that correct data was transferred. Next, the CPU commands the emulation control board to write an inverse data pattern to the two memory blocks. Finally, the CPU reads emulation memory through the Memory Control Board to verify that the data was written correctly.

4-19. Results — There are two hexadecimal status messages, Read and Write. The Read message indicates problems with the emulation controller's ability to read emulation memory. The Write message indicates problems with the emulation controller's ability to write data into emulation memory. Errors are represented by placing a "one" in the status word at the position of each failing data bit. The messages are therefore decoded as follows (Read and Write status are decoded in the same way):

	HEX	BINARY			
Read	0000 =	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
(Write)		P O N M	L K J I	H G F E	D C B A

Where
A = D0
B = D1
C = D2
D = D3
E = D4
F = D5
G = D6
H = D7
I = D8
J = D9
K = D10
L = D11
M = D12
N = D13
O = D14
P = D15

For example, if the status message reads "Write = 1248", then D3, D6, D9 and D12 are failing.

4-20. Troubleshooting — A failure in this test could be caused by the emulator pod, emulation control board, or the Model 64151A Memory Controller. Refer to the Troubleshooting Flowchart (figure 4-1).

4-21. ADDRESS.

4-22. Purpose — to verify that the emulation controller can generate proper addresses on the emulation bus and that they are transmitted to emulation memory.

4-23. What — This test is similar to the Data Test except that a walking one/zero pattern is used to test the address bus. Any data bus failures in this test are assumed to represent address failures and are indicated as such on the status line; therefore, Data Test must pass before Address Test results can be considered valid.

4-24. Results — A hexadecimal status message is used to indicate address bus failures. A "one" is placed in the status word at the position of each failing bit. The message is therefore decoded as follows:

	HEX	BINARY			
Error	0000 =	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
		P O M N	L K J I	H G F E	D C B A

Where
A = A0
B = A1
C = A2
D = A3
E = A4
F = A5
G = A6
H = A7
I = A8
J = A9
K = A10
L = A11
M = A12
N = A13
O = A14
P = A15

For example, if the status message reads "Error = 1248", then A3, A6, A9, and A12 are failing.

4-25. Troubleshooting — A failure in this test could be caused by the Emulator Pod, Emulation Control Board, or the Model 64151A Memory Controller. Refer to the Troubleshooting Flowchart (figure 4-1).

4-26. FOREGROUND TEST. (Figure 4-7.)

4-27. The Foreground Test consists of six subtests. They are: Release, Run, Processor Break, Illegal Memory Reference, Write to ROM, and Illegal Opcode. Each is described in the following sections.

4-28. RELEASE.

4-29. Purpose — verifies that the emulator can execute a program from background memory (on the emulation controller) and modify a background memory location.

4-30. What — The mainframe CPU loads a program into background memory and commands the emulator to run the program. The CPU waits a defined amount of time, then checks to make sure that a background memory location was changed. The emulator's status is also checked.

4-31. Results — No status information is displayed.

4-32. Troubleshooting — Failures in this test normally indicate problems with the Emulation Control Board or the Emulator Pod. Refer to the Troubleshooting Flowchart (figure 4-1).

4-33. RUN.

4-34. Purpose — verifies that the emulator can execute a program residing in emulation memory.

4-35. What — The mainframe CPU maps emulation memory into two blocks: 0-1k as emulation RAM; and 2-3k as emulation ROM. A program is then loaded into emulation ROM and the emulator is directed to execute the program. The program causes the emulator to read a location then write to a location in RAM. The mainframe CPU checks to verify that the data was written correctly.

4-36. Results — a hexadecimal status word is formed to indicate the status of the emulator. A "one" is placed in the bit position of each status line that fails. This message is decoded as follows:

	HEX		BINARY			
Status	0000	=	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
			XXXA	BCDE	XXXX	XXXX

Where
A = Memory cycle clock not present
B = Background mode operation
C = Illegal opcode
D = Memory caused break (may be any one of the following)
- undefined memory
- write to ROM
- illegal memory access

E = Break has occurred on this board
X = Don't care status bits

For example, if the status line reads "Status = 1200", then the memory cycle clock and memory break are failing.

4-37. Troubleshooting — Failures may occur on either the Emulator Pod, Emulation Control Board, or the Memory Controller. Refer to the Troubleshooting Flowchart (figure 4-1).

4-38. PROCESSOR BREAK.

4-39. Purpose — verifies that the emulator responds properly to a mainframe CPU break command.

4-40. What — The mainframe CPU loads a program into emulation memory and commands the emulator to run. The CPU then asserts the emulator break and verifies emulator status and last opcode address.

4-41. Results — A hexadecimal status word is formed to indicate the status of the emulator. A "one" is placed in the bit position of each status line that fails. This message is decoded as follows:

	HEX		BINARY			
Status	0000	=	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
			X X X A	B C D E	X X X X	X X X X

Where
A = Memory cycle clock not present
B = Background mode operation
C = Illegal opcode
D = Memory caused break (may be any one of the following)
- undefined memory
- write to ROM
- illegal memory access

E = Break has occurred on this board
X = Don't care status bits

For example, if the status line reads "Status= 1200", then the memory cycle clock and memory break are failing.

4-42. Troubleshooting — Failures may occur on either the Emulator Pod, Emulation Control Board, or Memory Controller. Refer to the Troubleshooting Flowchart (figure 4-1).

4-43. ILLEGAL MEMORY REFERENCE.

4-44. Purpose — to verify that the Model 64151A Memory Controller can properly cause an emulator break when an illegal memory access is attempted by the emulator.

4-45. What — The mainframe CPU loads a program into emulation memory and commands the emulator to run. The program contains instructions which cause the emulator to attempt an access of emulation memory that has been mapped as guarded. The CPU then verifies that the Memory Controller causes an emulator break. The emulator status and last opcode address is then verified.

4-46. Results — No status information is displayed.

4-47. Troubleshooting — A failure in this test could occur on the Emulator Pod, Emulation Control Board, or the Memory Controller. Refer to the Troubleshooting Flowchart (figure 4-1).

4-48. WRITE TO ROM.

4-49. Purpose — to verify that the Model 64151A Memory Controller can properly cause an emulator break when the emulator attempts to access memory mapped as ROM.

NOTE

On Model 64151A Emulation Memory Controllers with a repair number prefix of 2153A and above, the break on Write to ROM feature can be defeated by moving a jumper. When this feature is defeated, the Memory Controller will fail the Write to ROM portion of Foreground Test.

4-50. What — The mainframe CPU loads a program into emulation memory and commands the emulator to execute the program. The program contains instructions which cause the emulator to attempt a write to emulation memory that has been mapped as ROM. The CPU verifies that the Memory Controller asserts an emulator break, and also verifies proper emulator status and last opcode address.

4-51. Results — No status information is displayed.

4-52. Troubleshooting — A failure in this test could occur on the Emulator Pod, Emulation Control Board, or Memory Controller. Refer to the Troubleshooting Flowchart (figure 4-1).

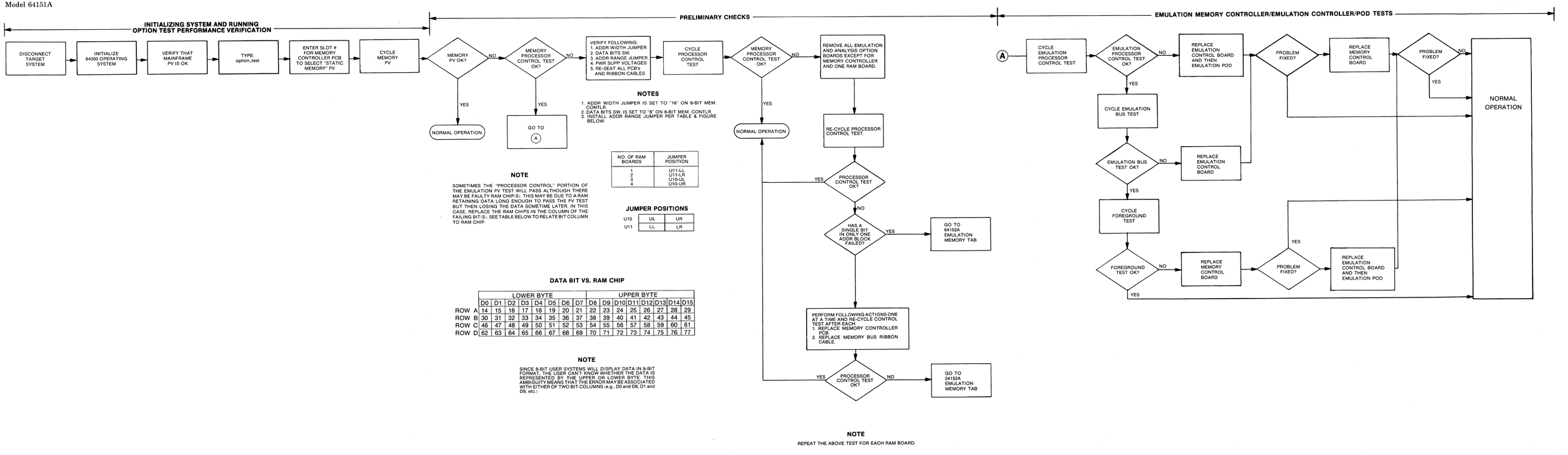
4-53. ILLEGAL OPCODE.

4-54. Purpose — to verify that an emulator break is generated upon detection of an illegal opcode.

4-55. What — The mainframe CPU loads a program into emulation memory and commands the emulator to execute the program. The program contains several illegal opcodes. The CPU verifies that the illegal opcode circuit on the Emulation Control Board properly detects these opcodes and generates an emulator break.

4-56. Results — No status information is displayed.

4-57. Troubleshooting — A failure in this test could occur on the Emulator Pod, Emulation Control Board, or Memory Controller. Refer to the Troubleshooting Flowchart (figure 4-1).



NOTES

1. ADDR WIDTH JUMPER IS SET TO "16" ON 8-BIT MEM. CONTLR.
2. DATA BITS SW. IS SET TO "8" ON 8-BIT MEM. CONTLR.
3. INSTALL ADDR RANGE JUMPER PER TABLE & FIGURE BELOW.

NO. OF RAM BOARDS	JUMPER POSITION
1	U11-LL U11-LR U10-UL U10-UR
2	
3	
4	

JUMPER POSITIONS

U10	UL	UR
U11	LL	LR

NOTE

SOMETIMES THE "PROCESSOR CONTROL" PORTION OF THE EMULATION PV TEST WILL PASS ALTHOUGH THERE MAY BE FAULTY RAM CHIP(S). THIS MAY BE DUE TO A RAM RETAINING DATA LONG ENOUGH TO PASS THE PV TEST BUT THEN LOSING THE DATA SOMETIME LATER. IN THIS CASE, REPLACE THE RAM CHIPS IN THE COLUMN OF THE FAILING BIT(S). SEE TABLE BELOW TO RELATE BIT COLUMN TO RAM CHIP.

DATA BIT VS. RAM CHIP

	LOWER BYTE								UPPER BYTE							
	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
ROW A	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
ROW B	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45
ROW C	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61
ROW D	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77

NOTE

SINCE 8-BIT USER SYSTEMS WILL DISPLAY DATA IN 8-BIT FORMAT, THE USER CAN'T KNOW WHETHER THE DATA IS REPRESENTED BY THE UPPER OR LOWER BYTE. THIS AMBIGUITY MEANS THAT THE ERROR MAY BE ASSOCIATED WITH EITHER OF TWO BIT COLUMNS (e.g., D0 and D8, D1 and D9, etc.)

NOTE

REPEAT THE ABOVE TEST FOR EACH RAM BOARD.

Figure 4-1.
Model 64151A Troubleshooting Flowchart

```
I/O BUS CONFIGURATION

ADRS    DEVICE
  0     7910 DISC MEMORY          LU=0
  1     2631 PRINTER
  4     THIS 64100
  6     64100




STATUS: Awaiting command      userid _____ 12:50

option_test_

_____ _____ _____ _____ _____ _____ _____ _____
```

Figure 4-2. Awaiting Command Status

```
HP 64000 Option Performance Verification

Card #    ID #    Module
  7       0200H   Static Memory
  8       0100H   Analysis
  9       0003H   8085 Emulator




STATUS: Awaiting test selection _____ 0:03

7_

 end    <SLOT #>  _____ _____ _____ _____ _____ print
```

Figure 4-3. Option Test Card Slot Listing

```
Memory Performance Verification

Static Memory in card slot # 7
8085 Emulator in card slot # 9
 Test                                  # Fail  # Test

Processor Control                        0       0

Emulation Bus                            0       0

Foreground                               0       0



STATUS: Awaiting test selection _____ 0:04

_

 end    cycle  next_test  start  _____ _____ _____ print
```

Figure 4-4. Memory Performance Verification

```
Memory Performance Verification
Processor Control Test

Static Memory in card slot # 7                  # Tests =      0
8085 Emulator in card slot # 9

 Block #      Error    # Fail        Block #      Error    # Fail

   0 -  4K    0000        0          32 -  36K   0000        0
   4 -  8K    0000        0          36 -  40K   0000        0
   8 - 12K    0000        0          40 -  44K   0000        0
  12 - 16K    0000        0          44 -  48K   0000        0
  16 - 20K    0000        0          48 -  52K   0000        0
  20 - 24K    0000        0          52 -  56K   0000        0
  24 - 28K    0000        0          56 -  60K   0000        0
  28 - 32K    0000        0          60 -  64K   0000        0

STATUS: Test in progress _____ 0:08

_

 end    cycle  next_test  start  _____ _____ _____ print
```

Figure 4-5. Processor Control Test

```
Memory Performance verification
Emulation Bus Test

Static Memory in card slot # 7
8085 Emulator in card slot # 9
 Test                                  # Fail  # Test

Data                    Read=0000        0       7
                        Write=0000       0
Address                 Error=0000       0



STATUS: Test in progress _____ 0:05

_

 end  _____ _____ _____ _____ _____ _____ print
```

Figure 4-6. Emulation Bus Test

```
Memory Performance Verification
Foreground Test

Static Memory in card slot # 7
8085 Emulator in card slot # 9
 Test                                  # Fail  # Test

Release                                  0       1

Run                     Status=0000      0

Processor Break         Status=0000      0

Illegal Memory Reference                 0

Write to Rom                             0

Illegal Opcode                           0

STATUS: Test in progress _____ 0:06

_

 end  _____ _____ _____ _____ _____ _____ print
```

Figure 4-7. Foreground Test

FIGURES 4-2 thru 4-7
LOCATED UNDER FOLD

SECTION V

ADJUSTMENTS

The Model 64151A Emulation Memory Controller has one adjustment. This adjustment (R9) is set by factory personnel using software which is not available to customers or field personnel. It is recommended that the calibration not be disturbed. If repair to the timing section of the Model 64151A is made, contact your local HP Sales/Service Office concerning procedures for returning the board to the factory for readjustment.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturer's five digit code numbers.

6-3. EXCHANGE ASSEMBLIES.

6-4. The Model 64151A is available through the Hewlett-Packard Corporate Parts Center by Blue Stripe Exchange. Exchange, factory repaired and tested assemblies are available only on a trade-in basis; therefore, assemblies required for spare parts stock must be ordered by the new assembly part number (found in table 6-2, Replaceable Parts). To order Blue Stripe Exchange assemblies, use the following part number:

A1: 64151-69503

6-5. ABBREVIATIONS.

6-6. Table 6-1 lists abbreviations used in the parts list, schematics and throughout the manual. In some cases, two forms of the abbreviations are used: one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-7. REPLACEABLE PARTS LIST.

6-8. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Chassis-mounted parts in alphanumeric order by reference designation.

b. Electrical assemblies and their components in alphanumerical order by reference designation.

c. Miscellaneous.

The information given for each part consists of the following:

a. The Hewlett-Packard part number and the check digit.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five-digit code that indicates the manufacturer.

e. The manufacturer's part number.

The total quantity for each part is given only once - at the first appearance of the part number in the list.

6-9. ORDERING INFORMATION.

6-10. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/Service Office.

6-11. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

6-12. DIRECT MAIL ORDER SYSTEM.

6-13. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum and minimum on any mail order (there is a minimum order amount for parts ordered through a local HP Sales/Service Office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-14. Mail-order forms and specific ordering information are available through your local HP Sales/Service Office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1	64151-66503	8	1	EMULATION MEMORY CONTROLLER	28480	64151-66503
A1C1	0160-2055	9	23	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C11	0160-2207	3	1	CAPACITOR-FXD 300PF +-5% 300VDC MICA	28480	0160-2207
A1C12	0140-0198	5	2	CAPACITOR-FXD 200PF +-5% 300VDC MICA	72136	DM15F201J0300WV1CR
A1C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C18	0180-0229	7	1	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A1C19	0160-0161	4	1	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
A1C20	0160-2200	6	1	CAPACITOR-FXD 43PF +-5% 300VDC MICA	28480	0160-2200
A1C21	0160-2198	1	3	CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
A1C22	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
A1C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C28	0140-0198	5		CAPACITOR-FXD 200PF +-5% 300VDC MICA	72136	DM15F201J0300WV1CR
A1C29	0140-0203	3	1	CAPACITOR-FXD 30PF +-5% 500VDC MICA	72136	DM15E300J0500WV1CR
A1C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C31	0160-2198	1		CAPACITOR-FXD 20PF +-5% 300VDC MICA	28480	0160-2198
A1C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C34	0140-0190	7	1	CAPACITOR-FXD 39PF +-5% 300VDC MICA	72136	DM15E390J0300WV1CR
A1CR1	1901-0040	1	4	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1J4	1251-5823	9	1	CONNECTOR 28-PIN M POST TYPE	28480	1251-5823
A1L1	9140-0114	4	1	INDUCTOR RF-CH-MLD 10UH 10% .166DX.385LG	28480	9140-0114
A1L2	9100-2264	5	1	INDUCTOR RF-CH-MLD 6.8UH 10% .105DX.26LG	28480	9100-2264
A1MP1	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
A1MP2	64151-85001	1	1	EXTRACTOR-P.C. BOARD	28480	64151-85001
A1MP3	64151-85002	2	1	EXTRACTOR-P.C. BOARD	28480	64151-85002
A1MP4	7124-0271	8		LABEL-ORANGE DOT	85480	QD25 TAPE B-810-OR
A1MP5	1400-0611	0	1	CLAMP-CABLE	06915	CFCC-8
A1R1	0684-1021	7	6	RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A1R2	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A1R3				NOT ASSIGNED		
A1R4	0757-0416	7	4	RESISTOR 511 1% .125W F TC=0+-100	24526	C4-1/8-TO-511R-F
A1R5				NOT ASSIGNED		
A1R6	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24526	C4-1/8-TO-511R-F
A1R7	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A1R8	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A1R9	2100-2497	9	1	RESISTOR-TRMR 2K 10% C TOP-ADJ 1-TRN	73138	82PR2K
A1R10	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A1R11	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A1R12				NOT ASSIGNED		
A1R13	0757-0453	2	1	RESISTOR 30.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3012-F
A1R14	0757-0438	3	3	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R15	0698-0084	9	2	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A1R16	0698-3151	7	2	RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A1R17	0698-3151	7		RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A1R18	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A1R19	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R20	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R21	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24526	C4-1/8-TO-511R-F
A1R22	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24526	C4-1/8-TO-511R-F
A1R23	0698-8271	2	1	RESISTOR 1.1 5% .25W F TC=0+-100	11502	TF07-1/4-T0-1R1-J
A1S1	3101-0458	1	1	SWITCH-SL DPDT SUBMIN .02A 20VDC PC	28480	3101-0458

See introduction to this section for ordering information.

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1TP1	0360-0535	0	8	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1U1	1820-1997	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U2	1820-1918	2	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
A1U3	1820-1624	7	4	IC BFR TTL S OCTL 1-INP	01295	SN74S241N
A1U4	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
A1U5	1820-0693	8	3	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U6	1820-1428	9	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A1U7	1820-1015	0	3	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
A1U8	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
A1U9	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U10	1820-1918	2		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
A1U11	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
A1U12	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
A1U13	1820-1428	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A1U14	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
A1U15	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A1U16	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U17	1820-1322	2	3	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A1U18	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
A1U19	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
A1U20	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A1U21	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A1U22	1820-1275	4	2	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
A1U23	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A1U24	1820-1372	2	1	IC FF TTL S J-K BAR CLEAR DUAL	07263	74S109DC
A1U25	1820-1200	5	1	IC INV TTL LS HEX	01295	SN74LS05N
A1U26	1820-1212	9	1	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A1U27	1820-1633	8	1	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
A1U28	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U29	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
A1U30	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
A1U31	1820-1782	8	2	IC MV TTL S MONOSTBL RETRIG/RESET DUAL	34335	AM26S02PC
A1U32	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U33	1820-1144	6	3	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U34	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U35	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U36	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U37	1820-1206	1	1	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
A1U38	1820-1782	8		IC MV TTL S MONOSTBL RETRIG/RESET DUAL	34335	AM26S02PC
A1U39	1810-0270	6	1	NETWORK-RES 10-SIP680.0 OHM X 9	01121	210A681
A1U40	1816-0909	0	1	IC TTL S RAM STAT 0-C	28480	1816-0909
A1U41	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1W1	8120-3366	1	1	CABLE-MEMORY-CONFIG	28480	8120-3366
A1XU18	1200-0638	7	2	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1XU31	1200-0607	0	2	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU37	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1XU38	1200-0607	0		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0607
				MISCELLANEOUS PARTS		
W1	8120-3351	4	1	CABLE-MEMORY BUS	28480	8120-3351
W2	8120-3352	5	2	CABLE- EMULATION BUS	28480	8120-3352
W3	8120-3352	5		CABLE- EMULATION BUS	28480	8120-3352

See introduction to this section for ordering information.

Table 6-3. Manufacturers' Codes

Mfr. Code	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
06915	RICHCO PLASTIC CO	CHICAGO	IL	60646
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
11502	TRW INC BOONE DIV	BOONE	NC	28607
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226
73138	BECKMAN INSTRUMENTS INC HELIPOT DIV	FULLERTON	CA	92634
85480	BRADY W H CO	MILWAUKEE	WI	53209

See introduction to this section for ordering information.

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. This section contains information for adapting this manual for which the content does not apply directly.

7-3. MANUAL CHANGES.

7-4. This manual applies directly to Model 64151A Emulation Memory Controllers with a repair number prefix of 2153A. With changes listed in table 7-1, it also applies to Model 64151A's with repair number prefixes of 2108A and 1924A. When making changes listed in table 7-1, make the change with the highest number first. Example: if backdating changes 1, 2, and 3 are required for your repair number prefix, do change 3 first, then change 2, and finally change 1.

7-5. If the repair number prefix of your instrument is not listed on the title page or in table 7-1, refer to an enclosed MANUAL CHANGES sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA changes.

Table 7-1. Manual Changes

Serial Prefix	Manual Changes
1924A	2, 1
2108A	2

CHANGE 1

Table 6-2, Replaceable Parts,
Change: HP and Mfr Part No. for A1 to 64151-66501, CD 6.
Change: C20 to HP Part No. 0160-2150, CD 5, CAPACITOR-FXD 33 PF +–5% 300VDC MICA, Mfr Code 28480, Mfr Part No. 0160-2150.
Change: C31 to HP Part No. 0140-0199, CD 6, CAPACITOR-FXD 240 PF +–5% 300VDC MICA, Mfr Code 28480, Mfr Part No. 0140-0199.
Delete: C34, R22.
Figure 8-6, Memory Access Circuitry,
Change: CPU access circuitry to the configuration shown in figure 7-2.

NOTE

If the repair number of the Model 64151A is 1924A00145 or below, refer to the Service Note reprinted at the end of this section for information concerning a field rework of the Model 64151A to correct a timing problem in the memory access circuitry. Most 64151A's in this repair number category have already been reworked; however, if yours has not been reworked, contact your local HP Sales/Service Office. See the paragraph entitled "OTHER CHANGES" within this section for further information relating to this change.

CHANGE 2

Section II, Installation,
Delete: figure 2-3.
Delete: Step e of the Model 64151A installation procedure on page 2-5.
Section IV, Performance Verification,
Delete: The note following paragraph 4-48, "Write to ROM".
Table 6-2, Replaceable Parts,
Change: HP and Mfr Part No. for A1 to 64151-66502, CD 7.
Delete: R23.
Figure 8-3, Model 64151A Component Locator,
Delete: R23.
Figure 8-6, Memory Access Circuitry,
Change: Illegal memory access circuitry to the configuration shown in figure 7-1.

7-6. OTHER CHANGES.

7-7. A few preferred parts changes have been made to improve performance of the Model 64151A. They are as follows:

a. On 64151-66501 and 64151-66502 boards, U39 may be HP Part No. 1810-0276, CD 2, NETWORK-RES 10-SIP 1.5K OHM X 9, Mfr Code 01121, Mfr Part No. 210A152. Preferred replacement for this part is HP Part No. 1810-0270, CD 6, NETWORK-RES 10-SIP 680.0 OHM X 9, Mfr Code 01121, Mfr Part No. 210A681.

b. The original Service Note 64151-1 outlining field rework to correct CPU access timing on the Model 64151A called for a 75 pF capacitor, HP Part No. 0160-2202, CD 8, CAPACITOR-FXD 75PF +-5% 300VDC MICA, Mfr Code 28480, Mfr Part No. 0160-2202. It has been determined that a 240 pF capacitor provides better performance in this modification than the 75 pF capacitor. Use HP Part No. 0140-0199, CD 6, CAPACITOR-FXD 240PF +-5% 300VDC MICA, Mfr Code 28480, Mfr Part No. 0140-0199. The Service Note reprinted in this manual has been corrected to reflect this change.

c. C11 in the LMAV delay circuit was originally a 180 pF capacitor, HP Part No. 0140-0197, CD 4, CAPACITOR-FXD 180PF +-5% 300VDC MICA, Mfr Code 28480, Mfr Part No. 0140-0197. It has been determined that a 300 pF capacitor provides better performance in this circuit. Use HP Part No. 0160-2207, CD 3, CAPACITOR-FXD 300PF +-5% 300VDC MICA, Mfr Code 28480, Mfr Part No. 0160-2207.

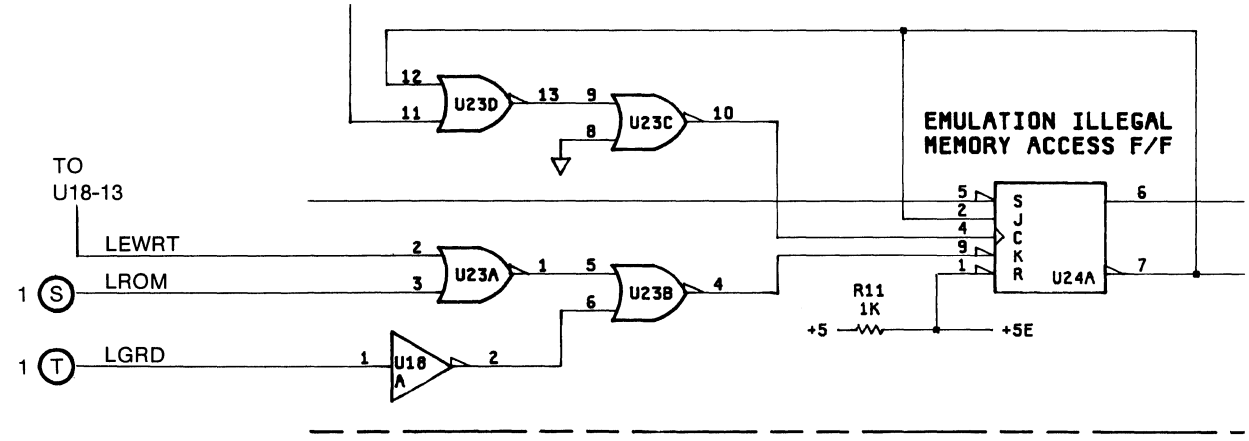


Figure 7-1. Illegal Memory Access Circuitry

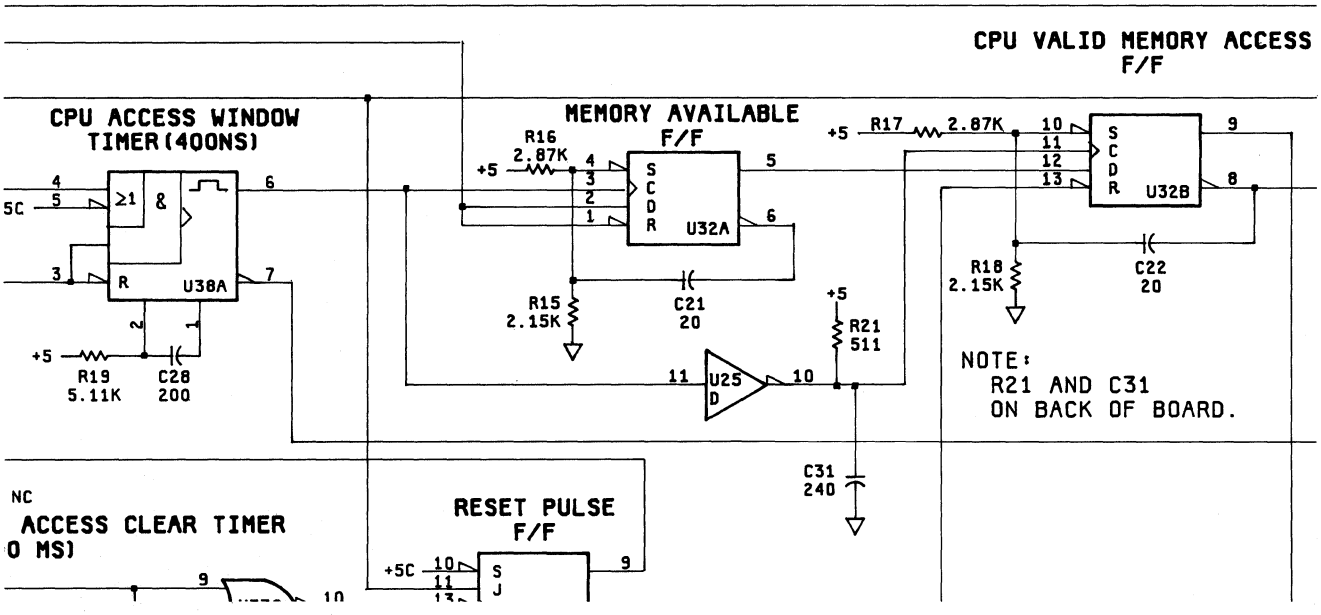


Figure 7-2. CPU Access Circuitry

64151-1

SERVICE NOTE

None

HP MODEL 64151 STATIC RAM CONTROLLER

Serial Numbers 1924A00145 and below
Rev C Boards

EMULATION "DISPLAY MEMORY MODE DYNAMIC" SHOWS MEMORY LOCATIONS INCORRECTLY CHANGING

A timing problem has been identified on the Static Ram Controller which causes an unstable display of memory. When doing a "DISPLAY MEMORY MODE DYNAMIC", one may occasionally observe the memory locations appearing to change. In actuallity, we are occasionally getting an incorrect sampling of the observed memory locations.

This problem can be corrected by installing the following modification on the Model 64151 boards, P/N 64151-66501 Rev. C.

PARTS REQUIRED

Quanity	Description	HP Part No.
1	Capacitor .01uf	0160-2055
1	Capacitor 240 pf	0140-0199
1	Resistor 511 ohm	0757-0416
1	IC Socket 14 pin, DIP	1200-0638
1	IC U25	1820-1200

INSTRUCTIONS

1. Cut the trace between U38 pin 7 and U32 pin 11.
2. Remove the existing jumper from the feedthrough near U12 to U32 pin 11. Place a mark by the feedthrough near U12.
3. Install a replacement jumper from the feedthrough near U12 to U38 pin 7.

CV/em/WA - 1 - 1/80-08

HEWLETT hp PACKARD

For more information, call your local HP Sales Office or East (201) 265-5000 • Midwest (312) 255-9800 • South (404) 955-1500 • West (213) 877-1281. Or, write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94304. In Europe, Post Office Box 85, CH-1217 Meyrin 2, Geneva, Switzerland. In Japan, Yokogawa-Hewlett-Packard, 1-59-1, Yoyogi, Shibuya-Ku, Tokyo, 151.

Printed in U.S.A.

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4. Remove IC U25.

5. Install a 14-pin socket (HP #1200-0638).

6. Install IC U25 (HP #1820-1200) into the socket.

7. Remove the .01uf bypass capacitor located between U25 and U32.

8. Clip about .5 inches of a lead from a 240 pf capacitor (HP #0140-0199).

9. Looking at the board from the component side, install the .5 inch lead into the feedthrough, vacated by the .01uf bypass capacitor. This is the feedthrough located farthest from the "GND" test point or as you hold the board (component side), with the 86 pin Motherboard connector down, the feedthrough is the left-most of the two. Solder the lead leaving about .25 inches of the lead protruding from the circuit side of the board.

10. Clip off the excess lead from the component side of the board.

11. Place about .25 inches of heat shrink tubing or spaghetti tubing over one leg of the 240 pf capacitor. Push this tubing tightly against the capacitor preventing any possible shorts with the capacitor lead.

12. On the circuit side, lay the 240 pf capacitor to allow the uninsulated end to connect with U25 pin 10 (do not solder) and connect the insulated end to wrap around the lead post extending from the feedthrough (do not solder). Connect the capacitor leads as short as possible and trim the extra lead lengths.

13. Lay the .01uf capacitor to allow one lead to wrap around the lead post, with the 240 pf capacitor, and the other end to be inserted into the other feedthrough. Trim the extra capacitor leads and solder the lead post and the feedthrough, to permanently affix the .01uf capacitor.

14. Place a 2 inch jumper between U25 pin 10 and U32 pin 11. With the 240 pf capacitor lead, solder the jumper and lead to U25 pin 10.

64151-1

15. Install a 511 ohm resistor (HP #0757-0416) between U32 pin 14 and U32 pin 11. Use heat shrink tubing or spagetti tubing over both leads to prevent any shorting with the leads. Solder the resistor lead to U32 pin 14. With the 2 inch jumper, solder the other resistor lead and jumper to U32 pin 11.

16. Install a 1.5 inch jumper wire between U25 pin 11 and U32 pin 3.

17. Use a drop of epoxy to secure the wires to the board surface. This is to avoid snagging the wires on other boards when removing or installing the boards.

64151-1

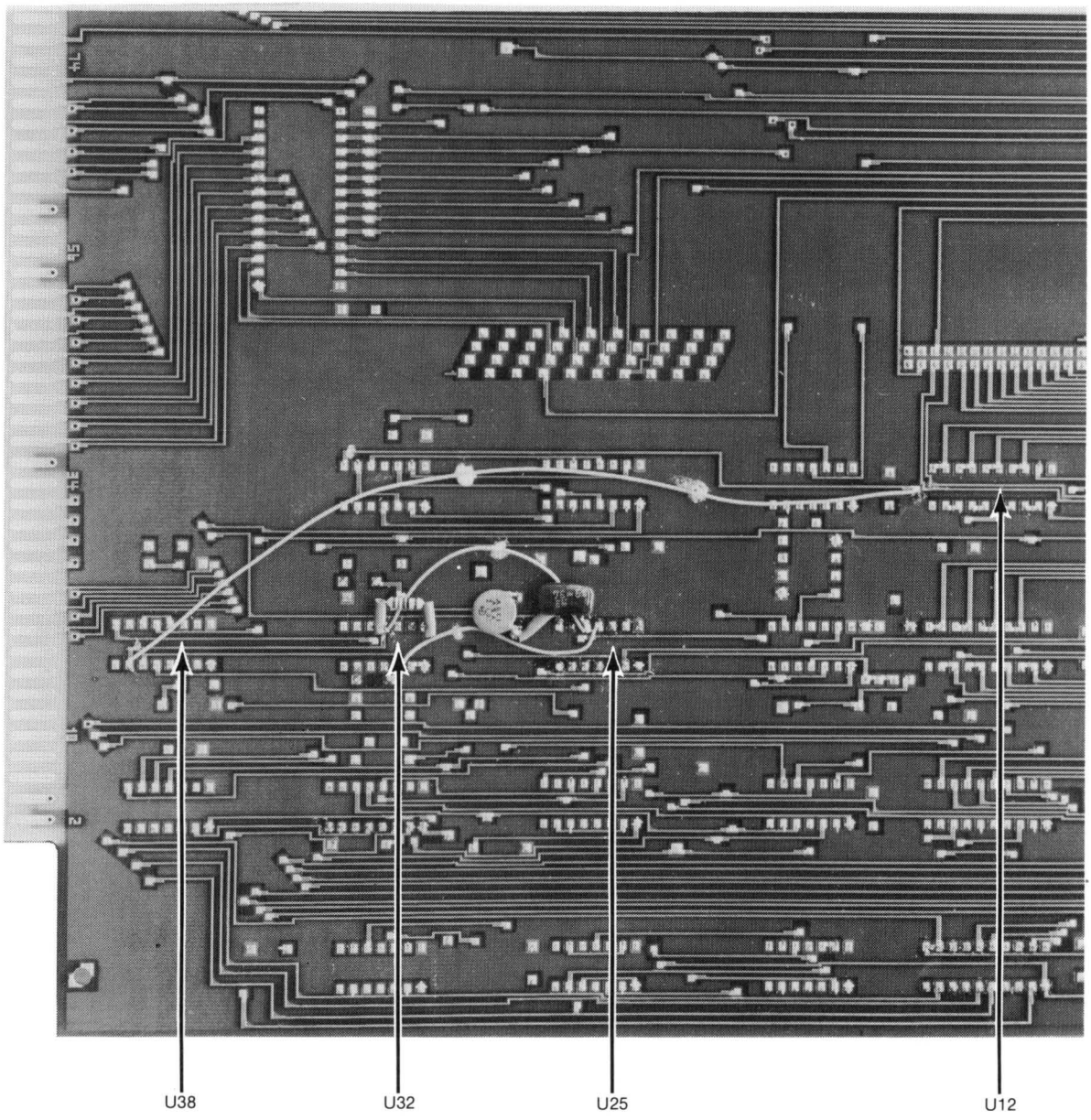


Figure 1

-4-

64151-1

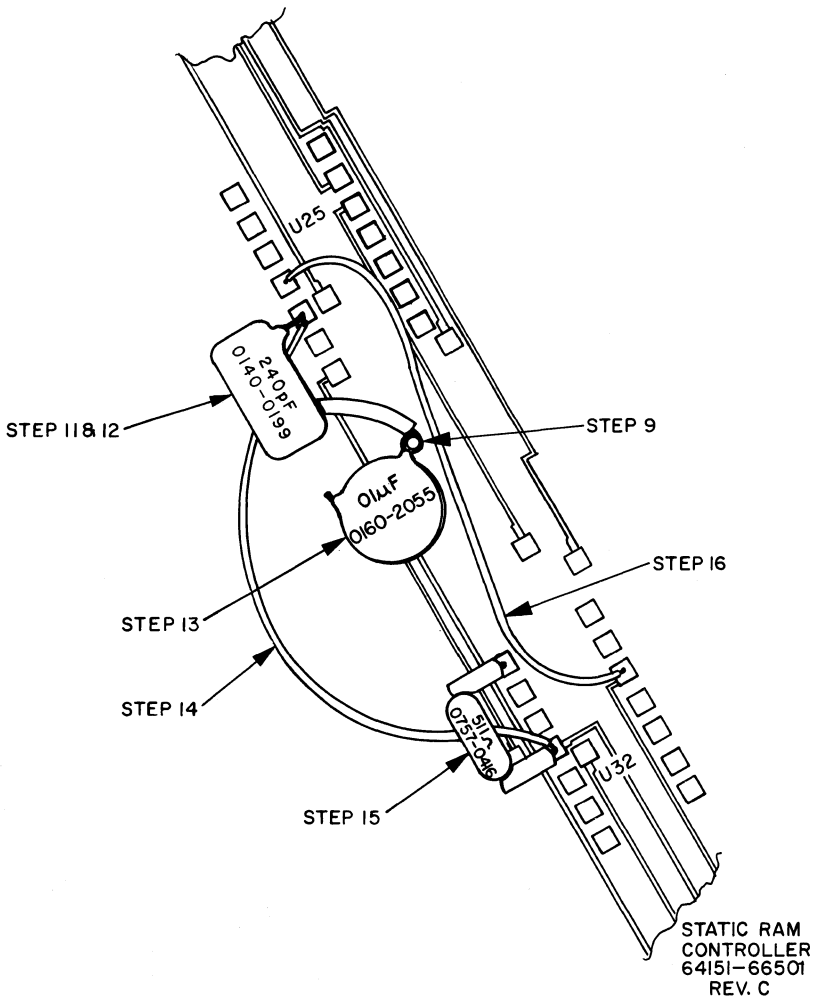


Figure 2

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains reference information for servicing the Model 64151A Emulation Memory Controller. Included are block diagrams on both the subsystem and board level, schematics, and component locators. Also included are functional descriptions of the block diagrams and schematics; and a list of mnemonics with their definitions, which are used throughout this section. Refer to Section IV for information on verifying proper operation of the Emulation Subsystem.

8-3. SAFETY.

8-4. Read the safety summary at the front of this manual before attempting to service the Model 64151A Emulation Memory Controller.

8-5. EMULATION SUBSYSTEM BLOCK DIAGRAM.

8-6. Figure 8-1 is a block diagram of the emulation subsystem, which is used to emulate various microprocessors in the user's target system. Capabilities include software development and debugging, hardware simulation, and real-time program execution.

8-7. DESCRIPTION.

8-8. The Emulator Pod contains the specific microprocessor to be emulated. It may be used as a stand-alone device for software development; or its user plug may replace the microprocessor in the target system, allowing execution of software developed on the 64000 system. The pod communicates with the rest of the emulation subsystem via the pod bus.

8-9. The Emulation Control Board performs the interface functions between the Emulator Pod, the emulation bus, and the BPC (mainframe) bus. It buffers and controls data transactions between these three buses; performs a memory mapping function which is used to control buffers within the Emulator Pod and Emulation Control Board, and records various pieces of status information from the Emulator Pod. It also contains the background memory, which is used by the BPC to control the emulation system.

8-10. The Internal Analysis Module is used to store the results of a program run. The information it stores may be qualified by a trigger state or a set of trigger states. Also provided in software is a disassembly function which converts binary information stored by the analysis board to instruction mnemonics, which may then be displayed on the 64000 CRT.

8-11. The Emulation Memory Controller is used to control access to emulation memory and perform a mapping function, which allows various blocks of memory to appear to reside at user selected address ranges and respond as different types of memory (ROM, RAM, undefined).

8-12. The Emulation Memory Board(s) consist of banks of RAM in multiples of 8 kilobytes. Access to this memory is controlled by the Emulation Memory Controller.

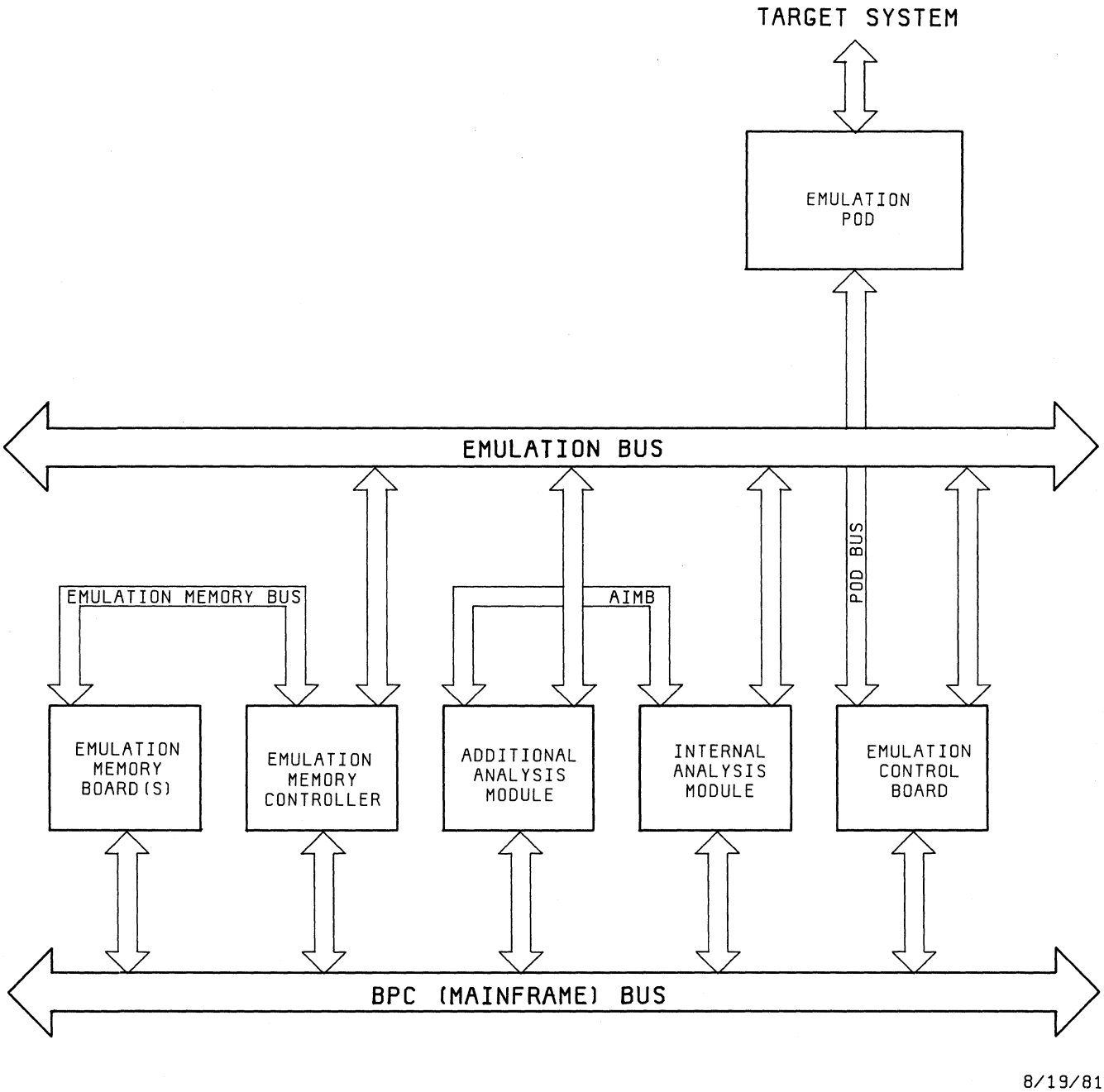


Figure 8-1. Emulation Subsystem Block Diagram

8-13. EMULATION MEMORY CONTROLLER BLOCK DIAGRAM.

8-14. Figure 8-2 is a block diagram of the Model 64151A Emulation Memory Controller. Following is a description of how each block functions.

8-15. DESCRIPTION.

8-16. The data transceivers buffer and control data transactions between the emulation data bus and the memory data bus; and also between the memory data bus and the mainframe (BPC) bus.

8-17. The 16k pager latch is programmed by the BPC to allow addressing of emulation memory to be split into 64-16k pages of memory. The pager is loaded by mainframe data bus LD 0-5 when the SET PAGER signal is asserted.

8-18. The address multiplexers determine whether the emulation address bus or the mainframe address bus will be allowed to drive the emulation memory address bus and the memory mapper RAM. The emulation address bus will be the driver when HMAV is false; and the mainframe address bus will be the driver when HMAV is true.

8-19. The memory mapper RAM is used to allow memory to appear to the emulator as blocks of RAM, ROM or illegal memory which may be contiguous or separated. This RAM is programmed by the mainframe from the user's commands, and the emulation address bus will be allowed to drive its address inputs during an emulation run, thus allowing the data information to be used as an address to emulation memory. The mapper also outputs data bits which indicate whether the currently addressed block of memory is ROM, RAM, or illegal memory. This information is used by the illegal memory access circuitry.

8-20. The illegal memory access circuitry uses the status outputs from the mapper RAM and the SET/CLEAR ILLEGAL output from the mainframe command decoder to determine whether or not to send a break (interrupt) signal to the emulator.

8-21. The mainframe command decoder uses the LMAP 1-3 signals from the mainframe bus to select various functions of the memory control board: SET PAGER, SET MAPPER, SET/CLEAR ILLEGAL, and MEMORY OPERATION.

8-22. The read/write control circuitry generates the upper and lower byte select signals to emulation memory and also generates the read/write signal to emulation memory. These strobes are driven by the respective signals from either the emulation bus or the mainframe bus, depending on the state of HMAV.

8-23. The access control circuitry decides whether the emulation system or the mainframe should be allowed to access emulation memory.

8-24. THEORY OF OPERATION.

8-25. The following paragraphs describe the theory of operation for the Model 64151A Emulation Memory Controller. The description is broken down by schematics and functional blocks.

8-26. SCHEMATIC 1.

8-27. Schematic 1 contains the function selector, the memory mapper RAM, the read/write strobe generation logic, a switch for selecting data bus width, and a jumper for selecting address bus width.

8-28. The function selector (U41) is a 1 of 8 decoder. Four outputs of the decoder are used to select various functions on the Model 64151A. These functions are: LSETMAP, LSETPG, LCPUAC, and LIDEN. The other four outputs of the selector are unconnected. To select a given function, the mainframe asserts LSEL and LSTB, then turns on LMAP 1 through LMAP 3 to select the desired function.

8-29. The memory mapper RAM (U40) is used to decode emulation addresses into emulation memory addresses. The address input of the RAM comes from the higher-order bits of the emulation address bus; and the data output of the RAM is used as the higher-order bits of the emulation memory address. The RAM is programmed by the BPC as follows: The BPC asserts LWRT and commands the function selector (U41) to assert LSETMAP. This causes a high on the output of U35C, which is inverted by U34C to assert the write input of the mapper RAM. Mainframe data bus LD0-LD8 will then be stored at the location pointed to by the address input of the RAM, which, in the programming mode, is driven by the mainframe through the address multiplexers on schematic 2. During normal emulation operation, LSETMAP is negated, and the mapper is in the read mode. The address input is then driven by the emulation address

bus via the multiplexers on schematic 2. The data output of the RAM is inverted by buffer U27 and sent to the emulation memory address bus. Also output from the RAM is data information indicating if the memory address has been mapped as user memory, ROM, or guarded (illegal) memory.

8-30. The read/write strobe generation logic consists of gates U18, 20, 21, 22, 28, 29, 34, 36. This logic is used to generate the upper and lower read/write strobes (LWRU, LWRL) in addition to a line which controls data buffer direction on the Emulation Memory Boards (LWRITE). These output lines can be driven by either the emulator or the mainframe, depending on who wishes to do a data transaction with emulation memory. Each line can be asserted as follows:

a. LWRU — this line will be asserted when the output of either U22A or U29A is high. U29A's output will go high when HMAV, LCPUWRT, and LUPB are asserted. U22A's output will go high when LEBUP and LEWR are asserted; HMAV is negated, and there are no illegal access or user access attempts.

b. LRWL — this line will be asserted when the output of either U22B or U29B is high. U29B's output will be high when HMAV and LCPUWRT are asserted, and LBYTE or LUPB are negated. U22B will output a high when LEWR and LEBUP or LEBYTE are asserted; HMAV is negated, and there are no illegal access or user access attempts.

c. LWRITE — this line will be asserted by either LEWRT or LWRT, depending on the state of HMAV.

8-31. SCHEMATIC 2.

8-32. Schematic 2 contains the address multiplexers, the 16k pager latch, data buffers to interface the emulation data bus and memory data bus, and data buffers to interface the mainframe data bus and memory data bus. Also on this schematic is circuitry for controlling buffer direction; and a circuit to identify the memory controller to the mainframe.

8-33. The address multiplexers (U6, 7, 8, 13, 14) are used to allow either the emulation address bus or the mainframe address bus to drive the memory address bus and the mapper RAM address. This is dependent on the state of LMAV. When LMAV is asserted, then the mainframe address is selected. When LMAV is negated, the emulation address is selected. The lower seven bits of output from the multiplexers drives the memory address bus directly; the upper thirteen bits are sent to drive the mapper RAM on schematic 1. The mapper output is used as the upper thirteen bits of memory address.

8-34. The CPU 16k pager latch (U15) is used to drive the address multiplexers when the mainframe address is selected. The pager is programmed by mainframe data bus LD 0-5 on a low-to-high transition of LSETPG (from the function selector) and LWRT (from the mainframe). This pager divides memory into 64 different 16k pages.

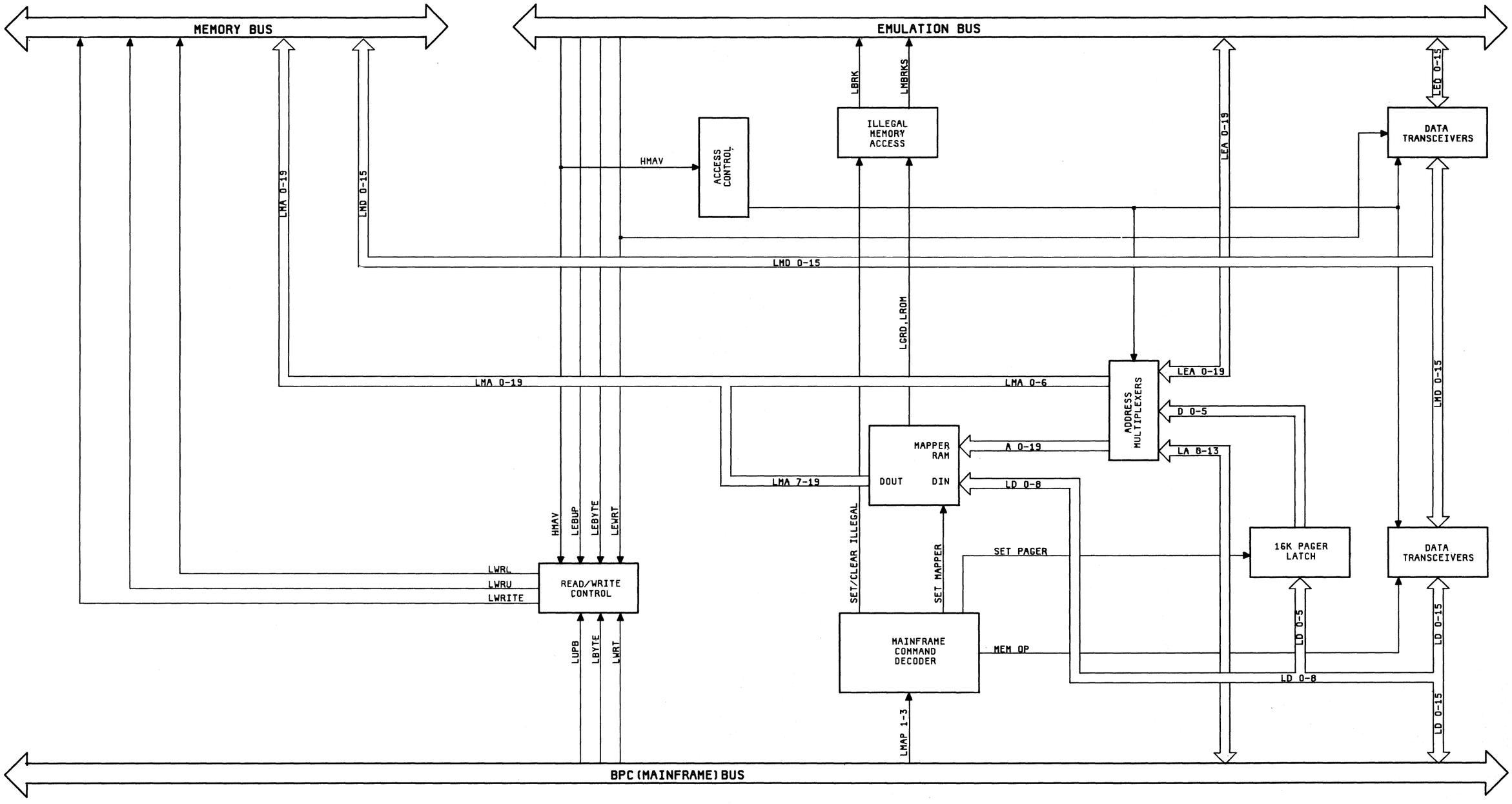
8-35. The emulation data bus buffers (U3, 4, 11, 12) are bi-directional buffers between the emulation data bus and the memory data bus. Data is transferred from the emulation data bus to the memory data bus when the output of U17D is high; indicating that LEWRT is asserted and HMAV is negated. Data will be transferred from the memory data bus to the emulation data bus when the Q output of U5A is low. This indicates that LUSER and LEWRT are negated, and a rising edge has occurred on LMAVD.

8-36. The CPU data read latches (U1, 9) and CPU data write buffers (U2, 10) are the mainframe interface for transferring data to and from emulation memory. During a mainframe read, data is latched on the rising edge of HDCLK (from schematic 3) and read when the output of U28B is low, indicating that LCPUAC (from the function selector) is asserted and LWRT is negated. Data is written to emulation memory when LCPUW and HCPUW are asserted.

8-37. The ID logic (U25, 30, 35) is controlled by LIDEN (from the function selector) and LID (from the mainframe). When both of these lines are asserted, the output of U35A will go high. This is complemented by open-collector inverter U25B to force a low on mainframe data bus LD 9, indicating to the mainframe that a Model 64151A Emulation Memory Controller is in the card slot that was polled. The output of U35A is also inverted by U30B to form LMBR; this line resets the illegal memory access flip-flop on schematic 3.

8-38. SCHEMATIC 3.

8-39. Schematic 3 contains circuitry to control emulation memory accesses by the mainframe and the emulator; it also contains a memory ready generator, an emulation write pulse generator, and a circuit to cause an emulator break (interrupt) when an illegal memory access is attempted.



NOTE:
THE ADDRESS BUS WIDTH SELECTION
JUMPER HAS BEEN OMITTED FOR CLARITY.

Figure 8-2.
Model 64151A Block Diagram

8-40. The CPU access circuitry is used to perform reads of emulation memory in between emulation processor memory cycles. The CPU is held off until the emulator has completed its memory transaction, at which time the CPU read is performed. If the transaction can be completed, a flag will be set indicating that fact to the mainframe. This circuitry is explained in the following paragraphs.

8-41. The CPU initiates an access request (access to emulation memory) by asserting LSEL and LMAP 1. This causes a high on the output of U33B, which is latched into the Q output of U26A when LSTM is asserted. The Q output is complemented by open-collector inverter U25D and sent back to the mainframe as LMSYN.

8-42. Pin 6 of U26A will go low when an access request occurs. When low, and LMAV is asserted, U37A pin 12 will be high, firing one-shot U38A. Pin 7 of U38A is sent to the CPU data latches on schematic 2 as HDCLK. HDCLK is true as the one-shot completes its time-out.

8-43. HDCLK is inverted by U25C to clock HMAV into the memory available flip-flop. It is inverted again by U25D to clock the Q output of the memory available flip-flop (U32A) into the CPU valid access flip-flop (U32B). If HMAV is true, a 1 will be latched into U32A and U32B. The Q/ output of U32B will then be low. LRD and LSETPG are true, causing HVAF to be asserted (U37-8) and inverted by U25F. This forces mainframe data bus LD 0 low, which indicates to the CPU that the read operation is valid.

8-44. The Q output of the CPU valid access flip-flop (U32B) is fed to the input of U33C, which clocks the access reset flip-flop. When the Q output of U32B goes high, a one will be clocked into U26B, which causes a low on the output of NOR-gate U35D, clearing the reset access request flip-flop. The access reset flip-flop may also be clocked by the time-out of U31A (approximately 2 μs) which is fired by the Q/ output of the access request flip-flop.

8-45. The access enable flip-flop (U24B) is clocked by the negation of LSETPG. When this occurs, a 0 is clocked into the Q/ output, resetting U26B, which prevents a reset of the access request flip-flop until the request occurs. It also resets the valid memory access flip-flop. When the access request occurs, U24B will be reset, releasing the valid memory access flip-flop and the access reset flip-flop.

8-46. The emulation illegal memory access flip-flop (U24A) is used to cause an emulator break (interrupt) whenever the emulator attempts an illegal memory operation. Two types of illegal accesses can be detected. They are:

a. Write to ROM — the LROM signal from the memory mapper and the LEWRT signal from the emulator are asserted, causing U23-1 to go high. LGRD is negated, causing U23-4 to go low. This puts a low on the K input of U24A. When LMAVD goes low, it passes through U23D, U23C to clock U24A. A high will then appear at the Q/ output of U24A. This is inverted by U25A to assert LBRK, which causes the emulator break. It is also fed back to U23D, which prevents subsequent transitions of LMAVD from clocking the flip-flop. The Q output of U24A is low, asserting LMBRKS, which indicates to the emulator that the memory board caused the break. The break condition will be reset when LMBR is asserted. This will occur when the mainframe does an ID poll.

b. Guarded memory — LROM is negated, forcing the output of U23A low. LGRD is asserted, which is inverted by U18A and causes a low on the K input of U24A. From here on the break operation is identical to the Write to ROM break above.

8-47. The ready pulse generator and the emulation access timer function together to provide a signal to the emulator that memory is ready to complete the data transfer. The circuit functions as follows: LUSER from the memory mapper is negated for an emulation memory access. This puts a high on the D input of U16A. At approximately the same time, HMAV and LEWRT are negated, which causes U17A to fire the emulation access timer (approximately 195 ns time-out). Some time later, LMAVD will go high, clocking the high on LUSER into U16A. The Q output of U16A is fed back to the D input of U16B. When the emulation access timer times-out, this one will be clocked into U16B, and U17 pin 10 will be low, which will reset U16A. The Q/ output of U16A will then be high, asserting HREADY which is sent to the emulator.

8-48. The emulation write pulse generator sends a pulse (LEWR) to the read/write strobe generation logic on schematic 1. To form the pulse, LWDV and U16-6 will go low. This puts a high on the output of U17B which causes the output of U19C to go high (U19C pin 9 high), forcing LEWR low. U17B's output is inverted by U18D, and delayed 50 ns. When the active low pulse from U18D clears the delay, U19 pin 9 will be low, causing the output of U19C to go low, and negating LEWR. The length of the write pulse is therefore approximately 50 ns.

8-49. LOGIC CONVENTION.

8-50. The circuits contained in the Model 64151A Emulation Memory Controller use a combination of both positive and negative logic. The following definitions are necessary to properly understand positive and negative logic:

0-state	—	the logic state which represents a false or negated logic condition.
1-state	—	the logic state which represents a true or asserted logic condition.
L level	—	the more negative of two voltage levels chosen to represent logic states.
H level	—	the more positive of two voltage levels chosen to represent logic states.

8-51. Given the above definitions, positive and negative logic are defined as follows:

Positive logic:	0-state = Low level voltage = negated 1-state = High level voltage = asserted
Negative logic:	0-state = High level voltage = negated 1-state = Low level voltage = asserted

8-52. The voltages representing the low and high levels within the Model 64151A are given as follows:

TTL Voltage Levels

Level	Voltage
Input Low	<0.8 V
Input High	>2.0 V
Output Low	<0.4 V
Output High	>2.4 V

8-53. MNEMONICS.

8-54. Table 8-1 is a list of signal names (mnemonics) in alphanumeric order. These signal names are used in the schematics and text to describe the function of the signals. The table indicates the active state and function of the signal.

Table 8-1. Mnemonics

Mnemonic	Description
A 7-19	Address 7 through 19 — Output from the address multiplexers. Used to address the memory mapper RAM. These lines can be driven by either the BPC or by an emulation address.
D 0-5	Data 0 through 5 — Output from the 16k pager latch, this data information is used to drive the address multiplexers. The information is used by the BPC to separate memory into 64 different 16k segments (pages).
HCPUW	High CPU Write — Output from U35D. When high, indicates that the BPC is initiating a write to emulation memory.
HDCLK	High Data Clock — Output from the CPU access window timer. A low to high transition on this line latches data from the memory data bus into the CPU read latches.
HMAV	High Memory Available — When high, indicates that the emulator is not attempting to access memory. Used in various circuits on the Memory Controller to control accesses to memory by the BPC or the emulator.
HPOP	High Power-on Preset — Inverted version of LPOP. Used by the mainframe to reset the CPU access circuitry to a known state.
HREADY	High Ready — Output to the emulation bus from the ready flip-flop. Indicates to the emulator that emulation memory is ready. This signal is active high.
HUSER	High User — Output to the emulation bus from the memory mapper. When high, indicates that the current address has been mapped to user target system memory.
HVAF	High Valid Access Flag — Output from the CPU access request logic. Indicates that the CPU read of emulation memory was valid.
LA 0-13	Low Address 0 through 13 — Input to the address multiplexers from the mainframe (BPC) address bus. This bus is used to drive the lower order memory address bits and the mapper address bits when LMAV is true.
LBRK	Low Break — Output to the emulation bus from the emulation illegal memory access flip-flop. When low, the memory controller is requesting the emulator to break.
LBYTE	Low Byte — Input to the read/write strobe generation circuitry from the mainframe (BPC) bus. When low, indicates that the BPC will transfer data on only the lower 8 bits of the data bus.
LCPUAC	Low CPU Access — Output from the mainframe command decoder. Used to control write strobes to emulation memory and control data transceivers. When low, indicates that the BPC wishes to perform operations on emulation memory.
LCPUW	Low CPU Write — Inverse of HCPUW, this signal will be low when the BPC is performing a write to emulation memory. LCPUW is used to enable the data buffers from the mainframe data bus to the memory data bus.
LCPUWRT	Low CPU Write — This signal differs from LCPUW above in that it is generated by the CPU write pulse generator. This line will pulse low when HCPUW is asserted.
LD 0-15	Low Data 0 through 15 — Mainframe (BPC) data bus, used to send data to emulation memory and program the memory mapper RAM and 16k pager.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LEA 0-19	Low Emulation Address 0 through 19 — Address bus from the emulator, input to the address multiplexers. This bus will drive the lower order memory addresses and the address bus to the memory mapper when LMAV is false.
LEBYTE	Low Emulation Byte — Input to the read/write strobe generation circuitry from the emulation bus. When low, indicates that data transfer will take place on the least significant 8 bits of the emulation data bus.
LEBUP	Low Emulation Byte Upper — Input to the read/write strobe generation circuitry from the emulation bus. When low, indicates that the data transfer will take place on the most significant 8 bits of the emulation data bus.
LED 0-15	Low Emulation Data 0 through 15 — Data bus to and from the emulator, low true. The emulator uses this bus to transfer data to and from emulation memory.
LEWR	Low Emulator Write — Output from the emulation write pulse generator, and input to the read/write strobe generation circuitry. This signal is produced by LWDV from the emulator gated with HREADY from the ready flip-flop, and is used to generate emulation memory write strobes LWRL and LWRU. When low, indicates a write operation by the emulator.
LEWRT	Low Emulation Write — Input to various control circuitry from the emulation bus. When low, indicates that the emulator is in a write cycle.
LID	Low Identification — Input to the ID logic from the mainframe (BPC) bus. When low, the mainframe is requesting the memory controller to place its identification code on the data bus.
LIDEN	Low Identification Enable — Output from the function decoder and input to the ID logic. When low, the LID signal from the mainframe will be passed through to force LD9 true, which indicates to the mainframe that a Model 64151A Emulation Memory Controller is in the card slot that was polled.
LGRD	Low Guarded — Output from the memory mapper and input to the illegal memory access circuitry. When low, the emulator has placed an address on the bus that was mapped as guarded memory space. When this line goes low, the illegal memory access circuitry will generate an emulator break.
LMA 0-19	Low Memory Address 0 through 19 — Output from the address multiplexers and the memory mapper RAM to the emulation memory bus. This address information is the translated address to emulation RAM from the emulator address.
LMAP 1-3	Low Map 1 through 3 — Input from the mainframe bus to the function selector. These lines are used to send mainframe commands to the memory controller.
LMAV	Low Memory Available — Inverse of HMAV from the emulation bus. When low, indicates that the emulator is not using memory. Used to control accesses to emulation memory by the mainframe and the emulator.
LMAVD	Low Memory Available Delayed — LMAV delayed by approximately 90 nanoseconds. Has the same uses as LMAV.
LMBR	Low Memory Break Reset — Output from the ID logic and input to the illegal memory access circuitry. This line will cause the emulator break lines to be reset to the high level state when the mainframe requests the ID of the memory control card.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LMBRKS	Low Memory Break Status — Output of the illegal memory access circuitry to the emulation bus. When low, this line indicates to the emulator that the memory controller requested the emulator break.
LMD 0-15	Low Memory Data 0 through 15 — Data bus to and from emulation memory. This bus is used for data transfers by both the emulator and the mainframe (BPC).
LMSYN	Low Memory Sync — Output to the mainframe bus from the CPU access circuitry. When low, requests the BPC to wait until the addressed device can complete the current operation.
LPOP	Low Power-on Preset — Input from the mainframe bus to the CPU access circuitry. Used to reset circuitry to a known state when low. LPOP is also used to create HPOP.
LRD	Low Read — Inverse of HWRT. When low, the BPC is performing a read operation. Used to force LD0 low when LSETPG is true.
LROM	Low ROM — Output of the memory mapper RAM. When low, indicates that the emulator has placed an address on the bus which has been mapped to ROM space. This line is gated with LEWRT in the illegal memory access circuitry to determine if the emulator is attempting to write to ROM. If so, an emulator break will be generated.
LSEL	Low Select — Input from the mainframe bus. When low, the memory controller has been selected for a data transfer operation.
LSETMAP	Low Set Mapper — Output of the function selector, and input to the mapper RAM after being gated with LWRT. When LSETMAP and LWRT are asserted, the memory mapper will store information from mainframe data bus LD 0-8.
LSETPG	Low Set Pager — Output from the function selector. When low, and LWRT is true, mainframe data bus LD 0-5 will be latched into the 16k pager.
LSTB	Low Strobe — Input from the mainframe (BPC) bus to the function selector. Used by the mainframe as an active low write strobe.
LSTM	Low Start Memory — Input to the CPU access request latch from the mainframe (BPC) bus. When low, indicates the beginning of a memory cycle; and that the address on the bus is valid.
LUPB	Low Upper Byte — Input to the read/write strobe generation logic from the mainframe (BPC) bus. When low, indicates that data is being transferred on the upper byte of the mainframe data bus.
LUSER	Low User — Output from the mapper RAM to the data bus control logic and the ready flip-flop. When low, indicates that the current emulation address lies within space mapped to user memory.
LWRITE	Low Write — Output of the read/write strobe generation logic to the memory bus. When low, a memory write is being performed.
LWRL	Low Write Lower — Output of the read/write strobe generation logic to the memory bus. When low, indicates that the data transfer will take place on the lower 8 bits of the memory data bus.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LWRT	Low Write — Input from the mainframe (BPC) bus to various circuitry on the memory controller. When low, indicates that the BPC is performing a write to the addressed device.
LWRU	Low Write Upper — Output from the read/write strobe generation logic to the memory bus. When low, indicates that the data transfer will take place on the upper 8 bits of the memory data bus.

Table 8-2. Schematic Diagram Notes

ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

TP1 ELECTRICAL TEST POINT TP (WITH NUMBER)

NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.

LETTERED TEST POINT NO MEASUREMENT AID PROVIDED

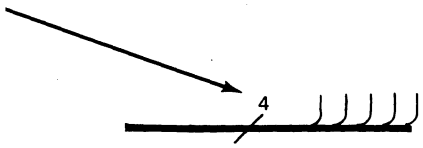
COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

1 3 NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION.
LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

A CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS



(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

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Table 8-3. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

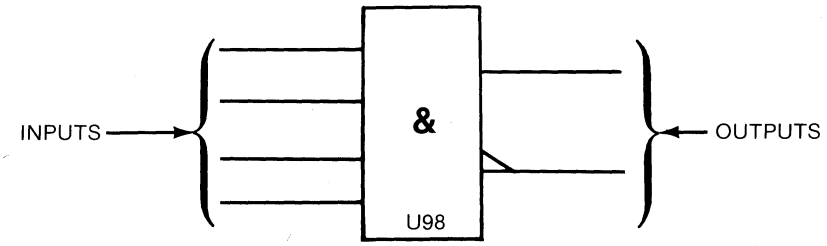
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

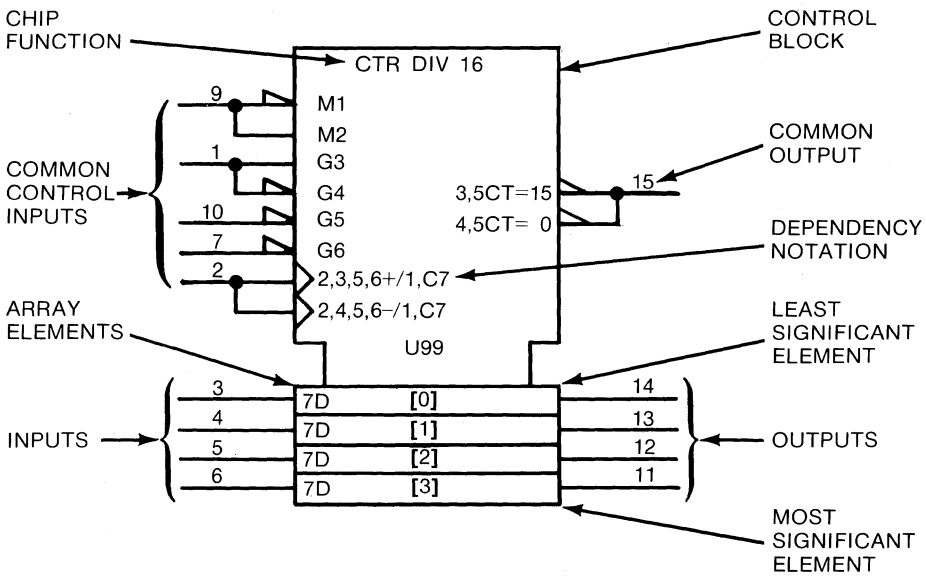
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

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Table 8-3. Logic Symbols (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state,

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-3. Logic Symbols (Cont'd)

OTHER SYMBOLS

Analog Signal	Inversion	Shift Right (or up)
& AND	O Negation	/ Solidus (allows an input or output to have more than one function)
Bit Grouping	Nonlogic Input/Output	Tri-State
Buffer	Open Circuit (NPN) (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
! Compare	Open Circuit (PNP) (external resistor)	( ) Used for factoring terms using algebraic techniques.
Dynamic	≥1 OR	[ ] Information not defined.
=1 Exclusive OR	Passive Pull Down (internal resistor)	Φ Logic symbol not defined due to complexity.
Hysteresis	Passive Pull Up (internal resistor)	
? Interrogation	Postponed	
— Internal Connection	← Shift Left (or down)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	–	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

Astable

100 ns Delay

Nonretriggerable Monostable

NV Nonvolatile

Retriggerable Monostable

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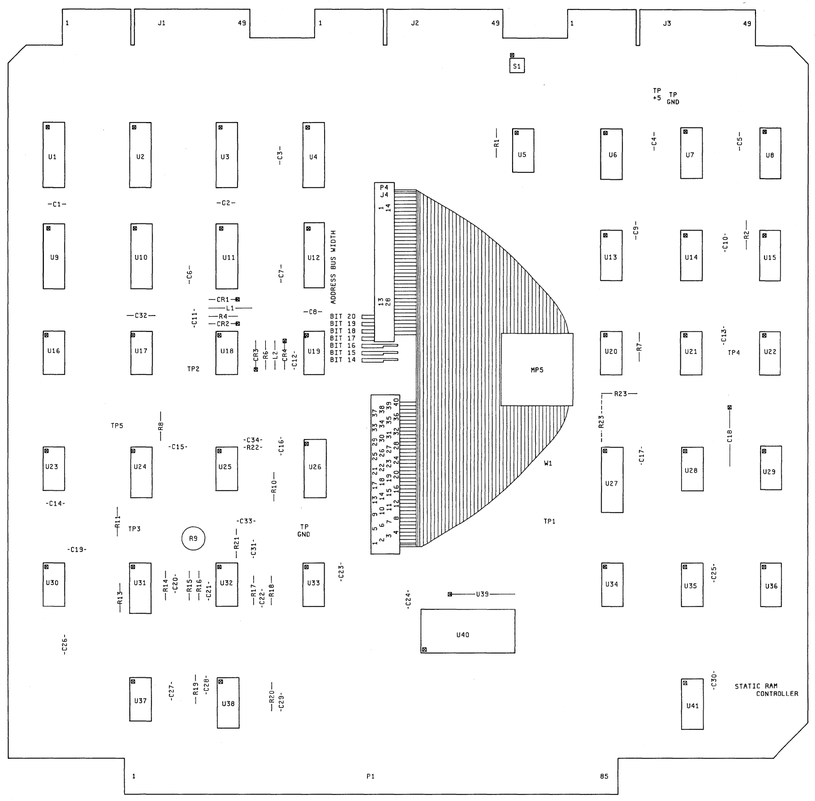
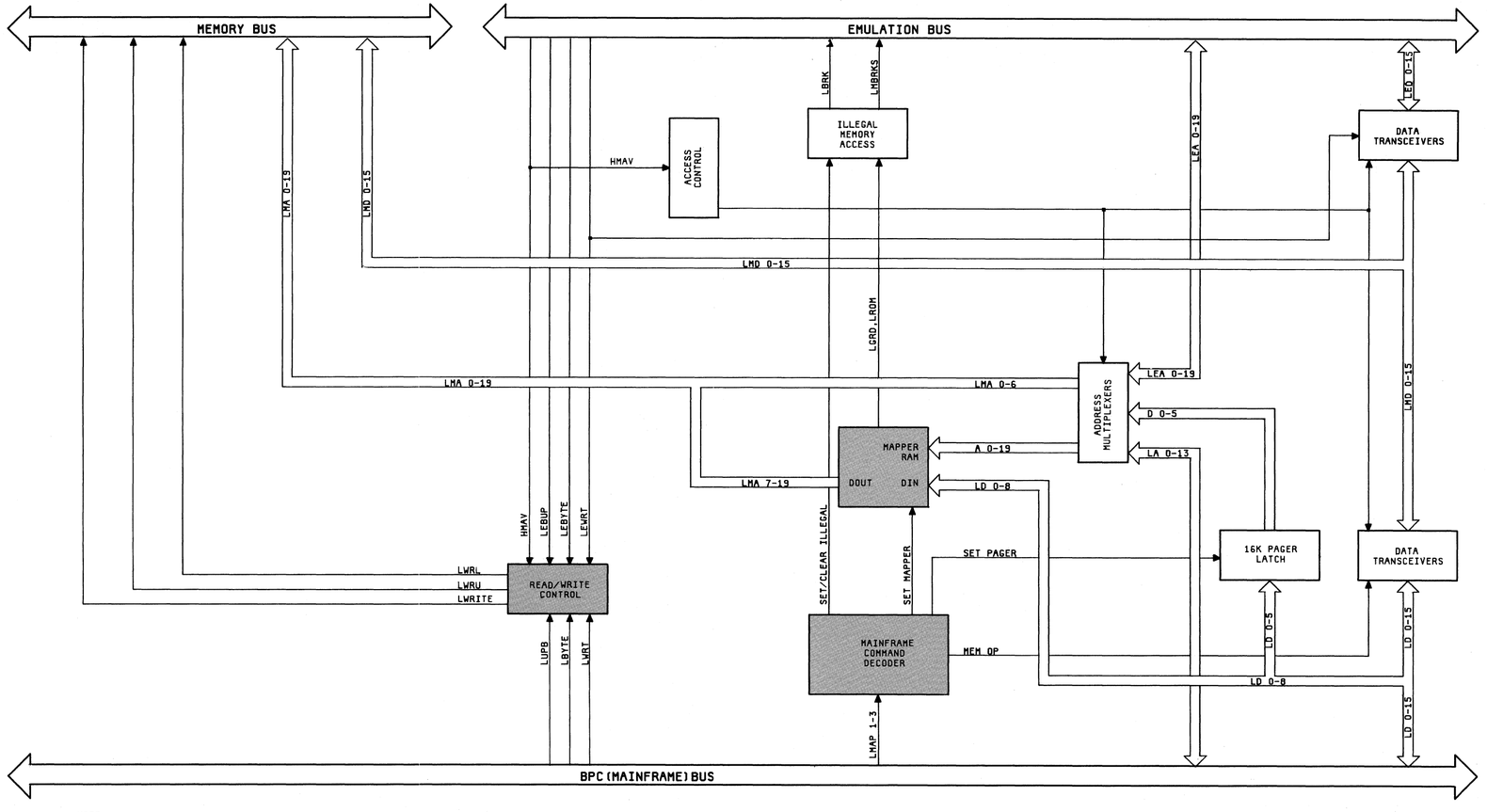
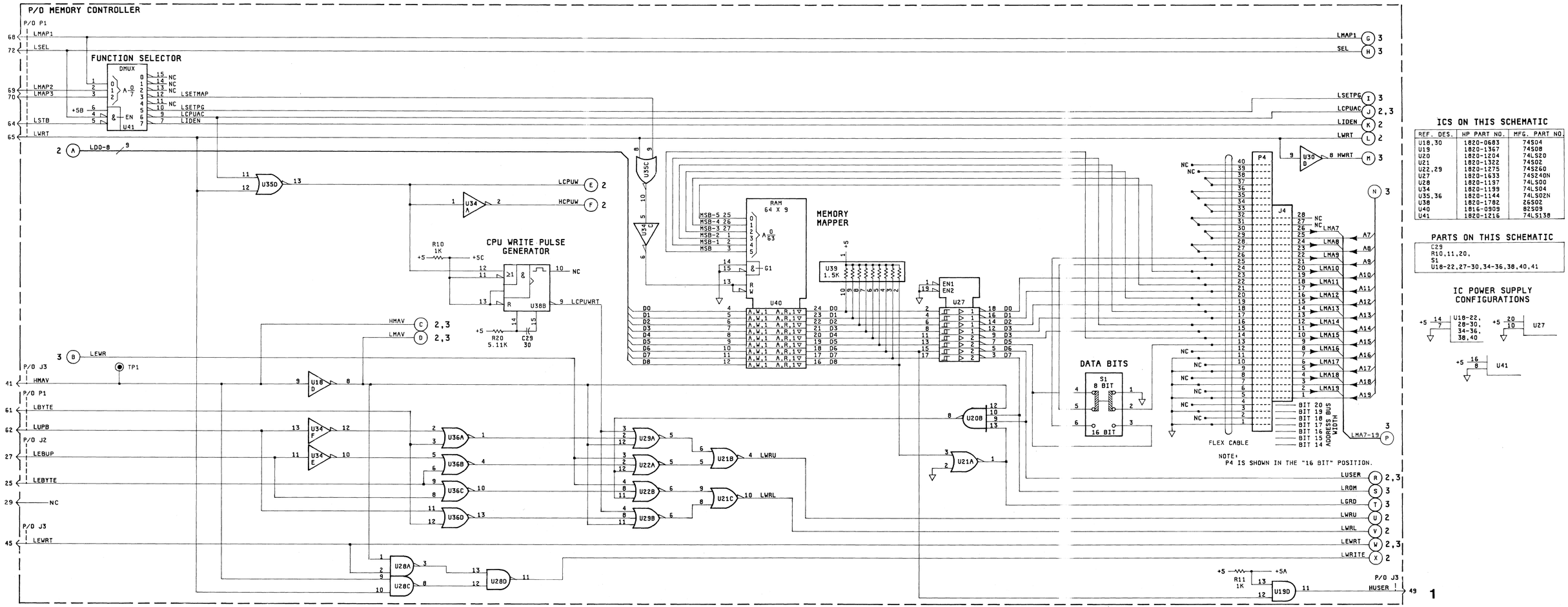


Figure 8-3. Model 64151A Component Locator (64151-66503)



NOTE:
THE ADDRESS BUS WIDTH SELECTION JUMPER HAS BEEN OMITTED FOR CLARITY.

Figure 8-4. Service Sheet 1, Memory Mapper and Write Strobe Control (Sheet 1 of 2)



ICS ON THIS SCHEMATIC

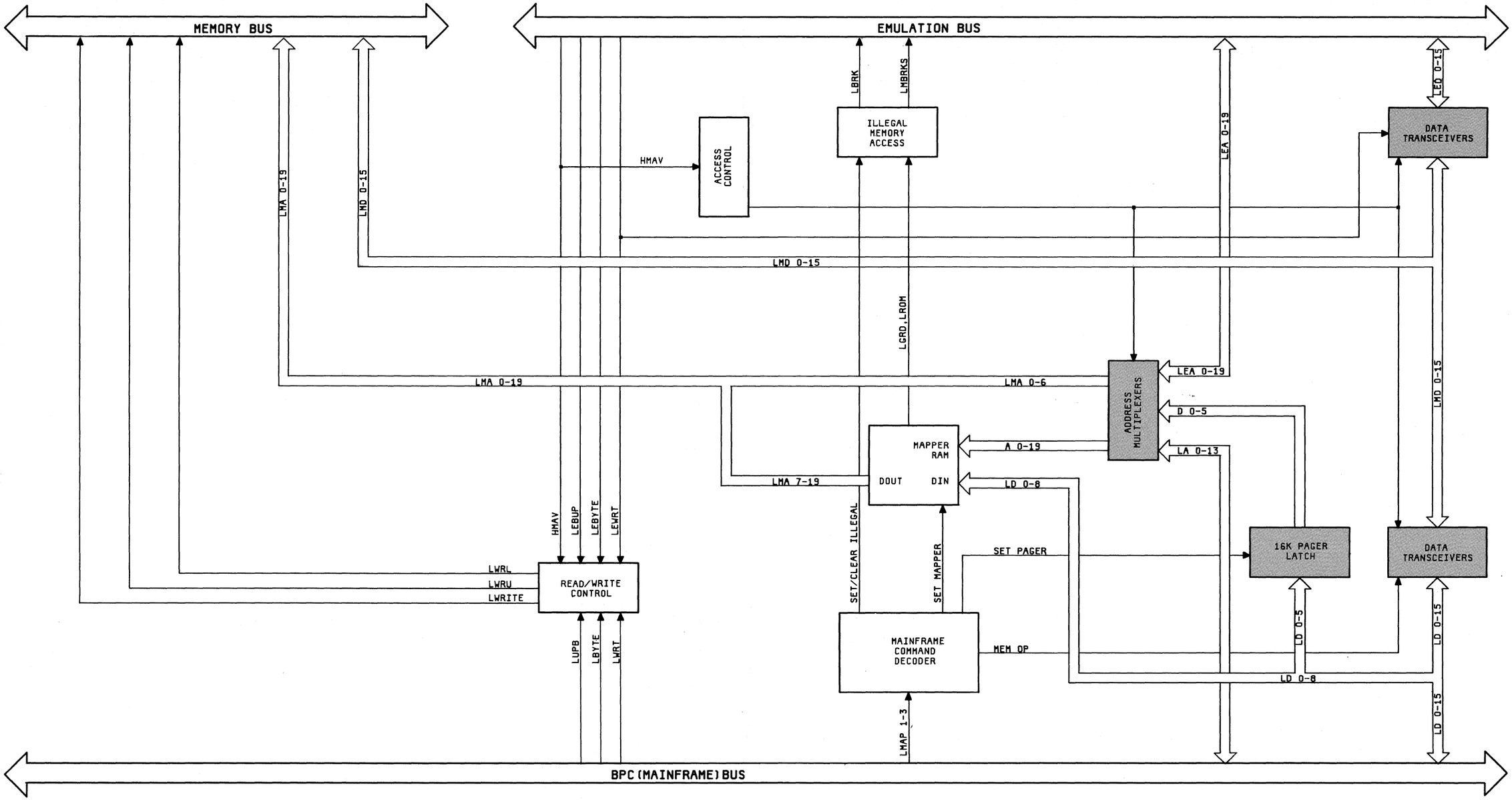
REF. DES.	HP PART NO.	MFG. PART NO.
U18,30	1820-0683	74S04
U19	1820-1367	74S08
U20	1820-1204	74LS20
U21	1820-1322	74S02
U22,29	1820-1275	74S260
U27	1820-1633	74S240N
U28	1820-1197	74LS00
U34	1820-1199	74LS04
U35,36	1820-1144	74LS02N
U38	1820-1782	26S02
U40	1816-0909	82S09
U41	1820-1216	74LS138

PARTS ON THIS SCHEMATIC

C29
R10,11,20,
S1
U18-22,27-30,34-36,38,40,41

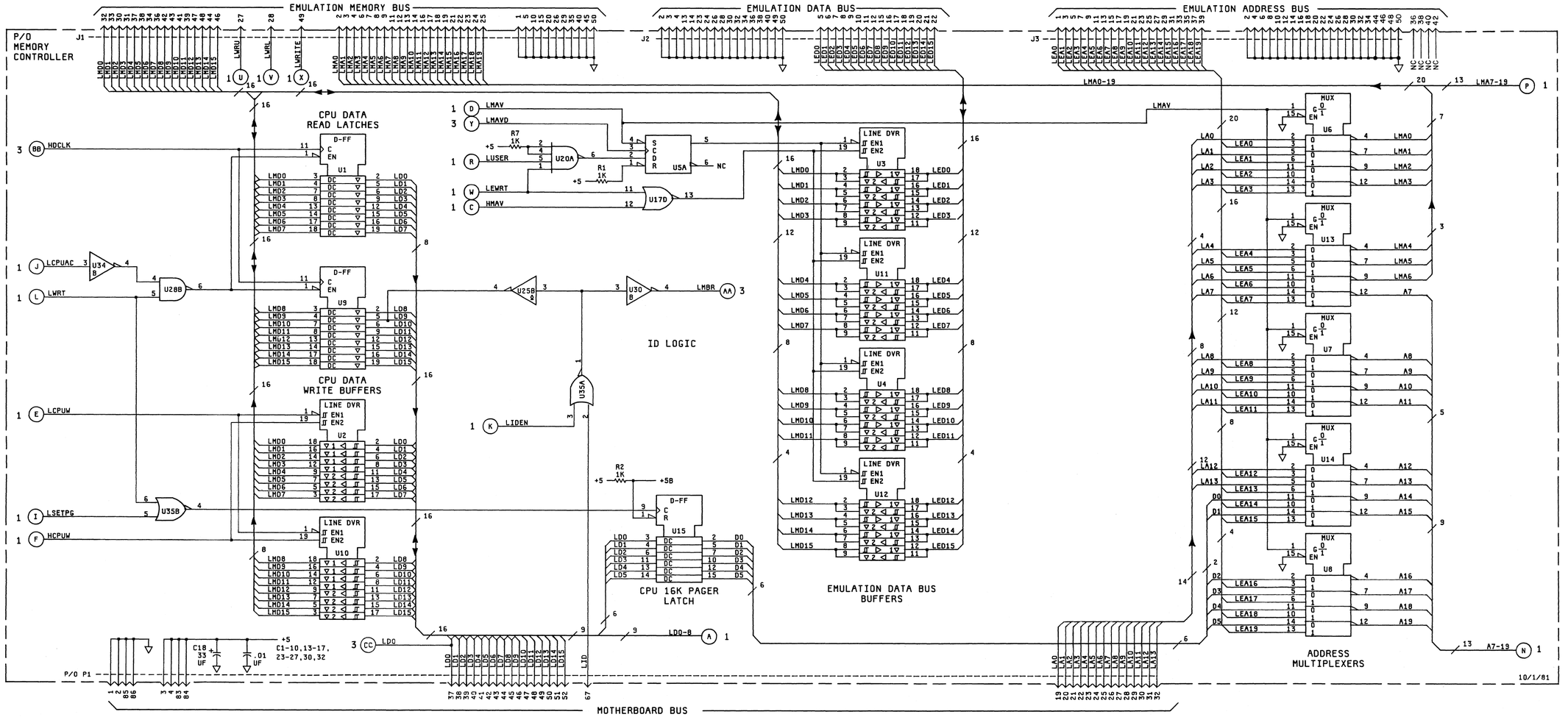
IC POWER SUPPLY CONFIGURATIONS

Figure 8-4.
Service Sheet 1, Memory Mapper and Write Strobe Control
(Sheet 2 of 2)



NOTE:
THE ADDRESS BUS WIDTH SELECTION
JUMPER HAS BEEN OMITTED FOR CLARITY.

Figure 8-5. Service Sheet 2, Data Transceivers and Address Multiplexers (Sheet 1 of 2)



ICS ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG PART NO.
U1,9	1820-1997	SN74LS374N
U2,10	1820-1918	SN74LS241N
U3,4,11,12	1820-1624	SN74S241N
U5	1820-0693	SN74S74N
U6,13	1820-1428	SN74LS158N
U7,8,14	1820-1015	SN74S158N
U15	1820-1196	SN74LS174N
U17	1820-1322	SN74S02N
U20	1820-1204	SN74LS20N
U25	1820-1200	SN74LS05N
U28	1820-1197	SN74LS00N
U30	1820-0683	SN74S04N
U34	1820-1199	SN74LS04N
U35	1820-1144	SN74LS02N

PARTS ON THIS SCHEMATIC

C1-10,13-18,23-27,30,32
J1,2
P1
R1,2,7
U1-15,17,20,25,28,30,34,35

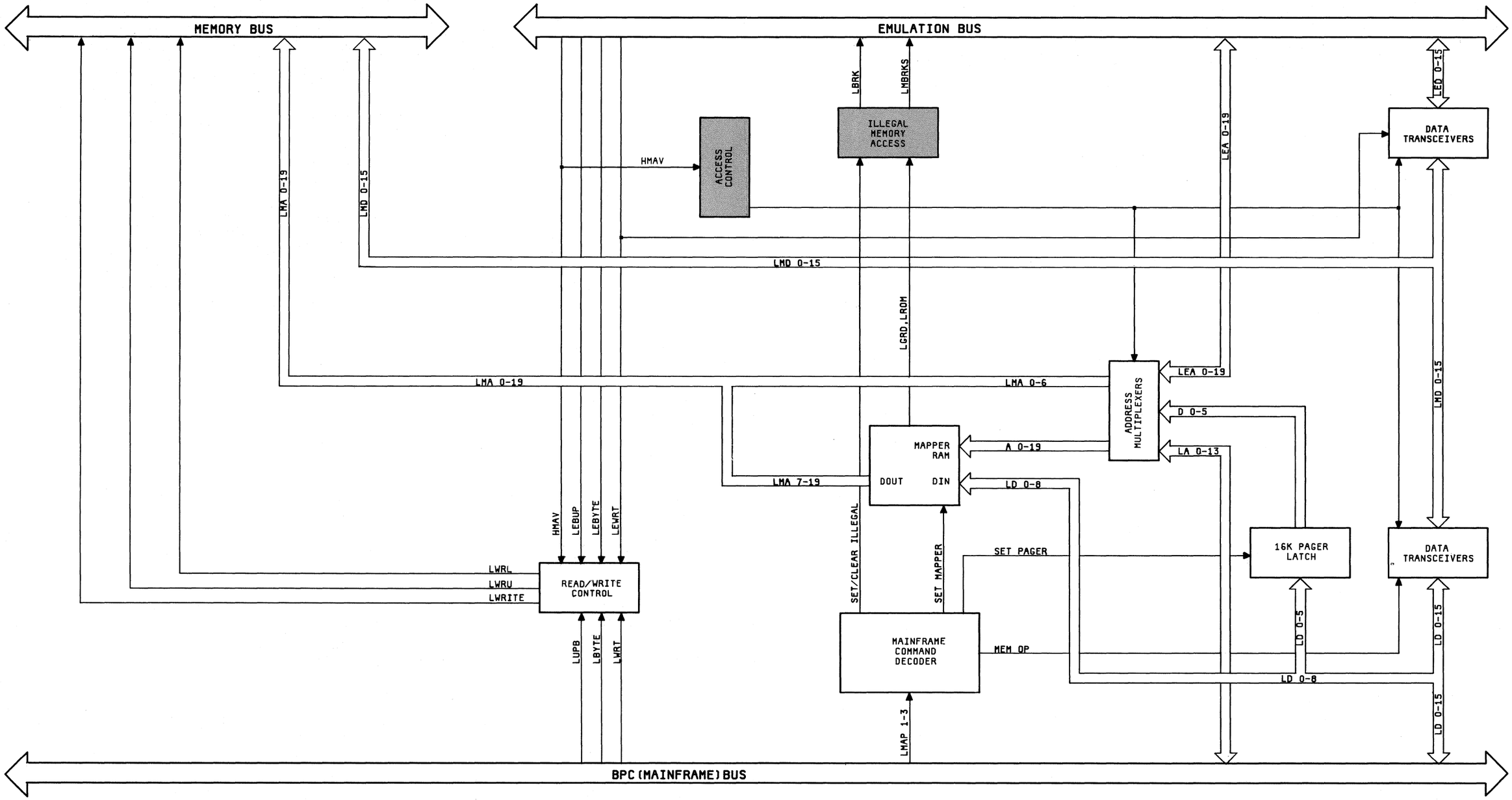
IC POWER SUPPLY CONFIGURATION

+5 20 10 U1-4 9-12

+5 14 7 U5,17,20,25, 28,30,34,35

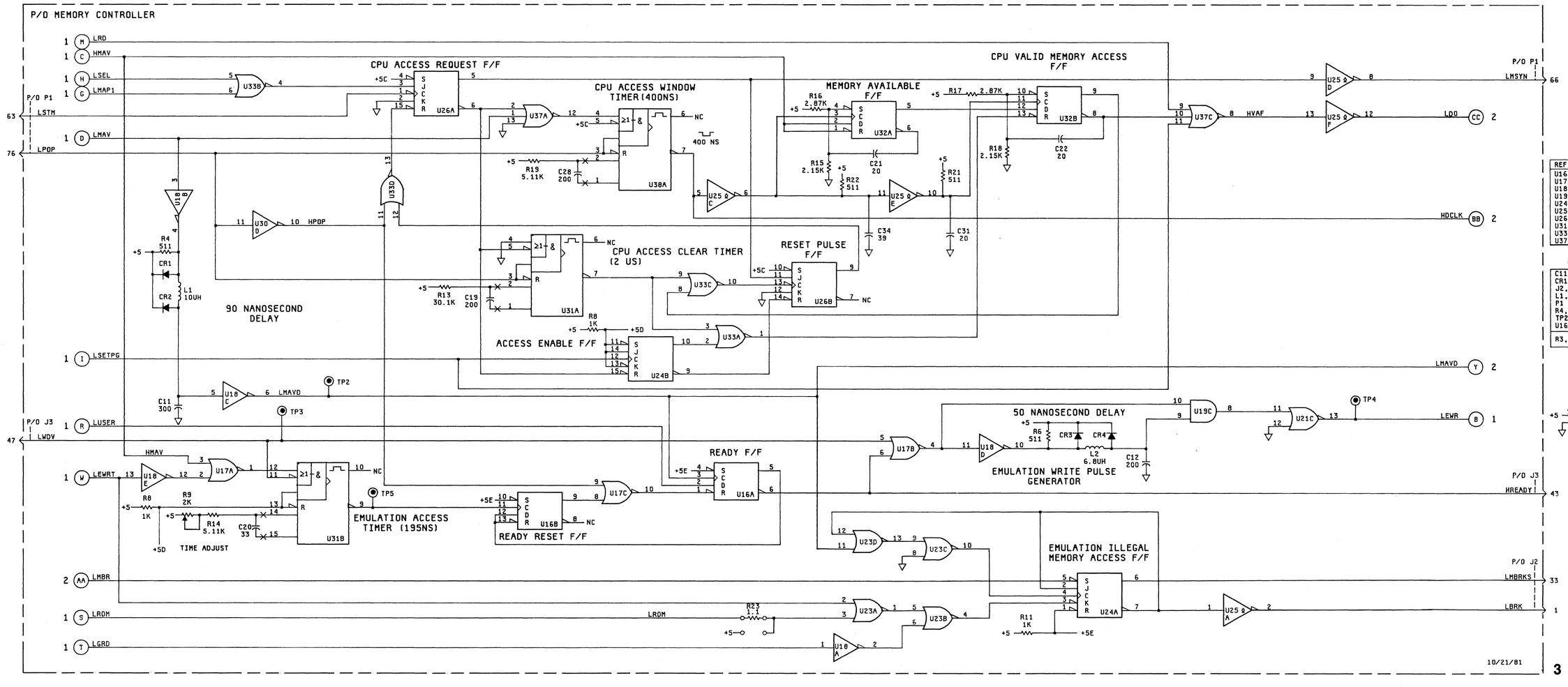
+5 16 8 U6-8,13, 14,15

Figure 8-5.
Service Sheet 2, Data Transceivers and Address Multiplexers (Sheet 2 of 2)



NOTE:
THE ADDRESS BUS WIDTH SELECTION JUMPER HAS BEEN OMITTED FOR CLARITY.

Figure 8-6. Service Sheet 3, Memory Access Circuitry (Sheet 1 of 2)



ICS ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG PART NO.
U16,32	1820-0693	SN74S74N
U17,21,23	1820-1322	SN74S02N
U18,30	1820-0683	SN74S04N
U19	1820-1367	SN74S08N
U24	1820-1372	74S109DC
U25	1820-1200	SN74LS05N
U26	1820-1212	SN74LS112AN
U31,38	1820-1782	AM26S02PC
U33	1820-1144	SN74LS02N
U37	1820-1206	SN74LS27N

PARTS ON THIS SCHEMATIC

C11,12,19-22,28,31
CR1-4
J2,3
L1,2
P1
R4,6,8,9,11,13-19,21
TP2-5
U16-19,21,23-26,30-33,37,38
R3,5,12 NOT ASSIGNED

IC POWER SUPPLY CONFIGURATIONS

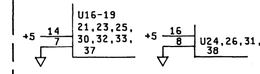


Figure 8-6.
Service Sheet 3, Memory Access Circuitry
(Sheet 2 of 2)

64151-90901, MAY 1982

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