64000

HP64000 Logic Development System

Model 64304A Emulation Bus Preprocessor

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

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HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

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HEWLETT PACKARD

SERVICE MANUAL

MODEL 64304A
EMULATION BUS PREPROCESSOR

REPAIR NUMBERS

This manual applies to 64304A Preprocessors with a repair number prefix of 2316A. For further information on repair numbers refer to "Instruments Covered by This Manual" in Section I.

Manual Part No. 64304-90901
Microfiche Part No. 64304-90801

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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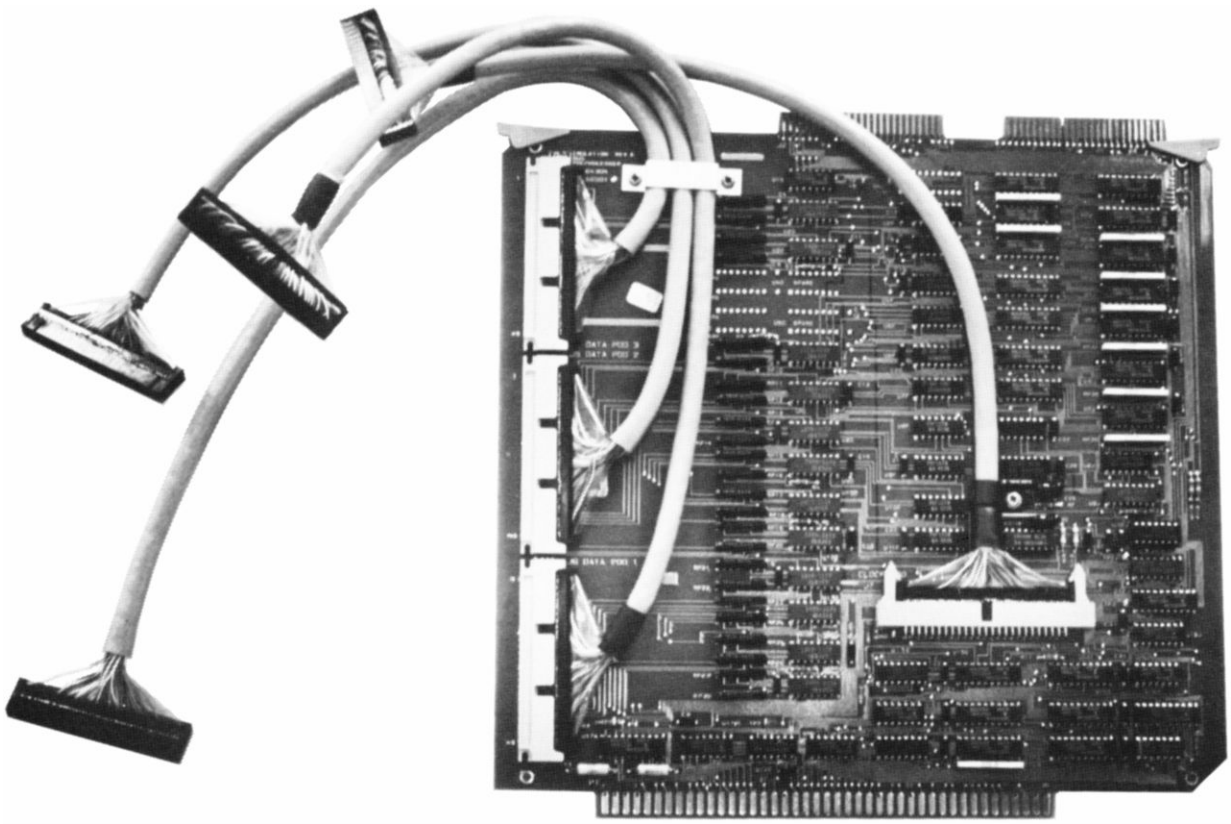


Figure 1-1. 64304A Emulation Bus Preprocessor Board

SECTION I

GENERAL INFORMATION

WARNING

The information in this manual is for the use of trained service personnel. To avoid electrical shock, do not perform any procedures in the manual or do any servicing to the 64304A unless you are qualified.

1-1. INTRODUCTION.

This manual contains technical information concerning the installation, operation, maintenance, and servicing of the 64304A Emulation Bus Preprocessor.

Note, the terms 64304A, Preprocessor, and EBPP will be used throughout this manual in reference to the 64304A Emulation Bus Preprocessor. The term CPU will be used when referring to the 64000 Host Microprocessor. The abbreviation PV will be used when referring to Performance Verification.

1-2. MANUAL ORGANIZATION.

SECTION I, General Information. This section contains a description of this manual and the 64304A. This section also includes a listing of the recommended test equipment for the 64304A.

SECTION II, Installation. Section II explains how to unpack and install the 64304A into the 64000 Development System; it also gives enviromental limits of operation and packing information should the 64304A ever need to be shipped.

SECTION III, Operation. Operation of the 64304A is beyond the scope of this service manual. For complete operating instructions refer to the Operators Manual.

SECTION IV, Performance Tests. This section concerns the execution of software based Performance Verification (PV) tests; which includes the interpretation of status codes to verify correct operation, and how to troubleshoot a failure.

SECTION V, Adjustments. This section normally contains calibration information; however, there are no adjustments applicable to the 64304A, so this section is blank.

SECTION VI, Replaceable Parts. This section contains ordering information and a list of all the parts that make the 64304A.

SECTION VII, Manual Changes. This section has information which adapts this manual to 64304A's with repair numbers below the one shown on the title page.

SECTION VIII, Service. The Service section contains information for servicing the 64304A; which includes block and component level theory of operation, and detailed schematics.

1-3. INSTRUMENTS COVERED BY THIS MANUAL.

Attached to the instrument or printed circuit board is a repair number plate. The repair number is in the form 0000A00000. It is in two parts; the first four digits and the letter are the repair prefix and the last five are the suffix. The prefix is the same for all identical instruments; it only changes when a prefix change is made to the instrument. The suffix is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with repair number prefix(es) listed under REPAIR NUMBERS on the title page.

An instrument manufactured after the printing of this manual may have a repair number prefix not listed on the title page. This unlisted repair number prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a yellow manual change supplement. The supplement contains "change information" that explains how to adapt the manual to the newer instrument.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest manual changes supplement. The supplement is identified by the manual print date and part number, both of which appear on the manual title page.

Shown on the title page is a microfiche part number. This number can be used to order 4 x 6 inch microfilm transparencies of this manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. DESCRIPTION.

The 64304A is an active interface between 64000 State Analysis and a Emulation Subsystem. The State Analyzer Control board clock pod and the data pod(s) of a State Acquisition board are connected directly to the 64304A allowing the State Analysis System to sample information on the Emulation Bus. The Emulation Bus, which is also connected to the 64304A, consists of address, data, and status information from either a General Purpose or Emulation Control board.

The 64304A Emulation Bus Preprocessor performs several functions under the control of Emulation Software or the host processor. The functions include converting the TTL logic levels of the Emulation Bus to ECL logic levels for the input channels to the State Acquisition boards, pattern recognition, Emulation Bus data and status multiplexing (used to configure expected State Analyzer input channels for analysis of 8 or 16 bit microprocessors).

1-5. RECOMMENDED TEST EQUIPMENT.

Table 1-1 lists the equipment required to troubleshoot and verify proper operation of the 64304A. Other equipment may be substituted if it meets or exceeds the critical specifications given in table 1-1.

Table 1-1. Recommended Test Equipment

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MODEL	USE *
Signture Analyzer		5005A or 5005B	T
Oscilloscope	Bandwidth: DC to 100MHz. Time Interval Measurements.	1740A	T

The following equipment is required to troubleshoot and to completely verify Option Test Performance Verification.

a.	One 64304A Emulation Bus Preprocessor	P,T
b.	One 40 or 60 Channel State Analysis System allowed **	P,T
c.	One minimum Emulation Subsystem.	P,T

* P=Performance Testing, T=Troubleshooting

** Accurate Performance Verification results may not occur with any other State Analysis System configurations. However, other operating configurations are available for the user. For further allowable State Analysis configurations refer to the 64000 Selection and Configuration Guide.

SECTION II

INSTALLATION

1-1. INTRODUCTION.

This section contains information necessary to install the Model 64304A Emulation Bus Preprocessor board. Also, included is information concerning initial inspection, damage claims, environmental considerations, storage and shipment.

2-2. INITIAL INSPECTION.

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents have been checked for completeness and the 64304A has been checked mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the 64304A does not pass Performance Verification, notify the nearest Hewlett-Packard office. If the shipping container or cushioning material is damaged notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for the carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for a claim settlement.

2-3. INSTALLATION.

WARNING

Read the safety summary at the front of this manual before installation or removal of the 64304A.

Procedure for installing a 64304A with the State Analyzer in the same mainframe:

a. Turn OFF the 64000 Development System.

b. Loosen the two hold-down screws of the 64100A and remove the card cage access cover. Refer to the 64110A Mainframe Service Manual for information on removing the card cage access cover.

This procedure is continued on the following page.

c. Insert the 64304A card directly behind either the General Purpose or Emulation Control card and before the State Analyzer Control card. See below.

d. Connect the clock cable from the 64304A to the clock input socket of the State Analyzer Control board. Connect the pod cable(s) from the 64304A to the corresponding pod cable input of the State Aquisition card(s). Make sure that pin 1 of the pod cable is connected to pin 1 on each of the State Analyzer boards. See below.

e. Install the Emulation Bus cables to the Emulation Memory Control board, either the General Purpose or Emulation Control board, and Emulation Bus Preprocessor board. The bus cables are keyed so they will connect to the edge connector in only one position. See below.

f. Reinstall the 64100A card cage access cover and tighten the 2 screws. Refer to the 64110A Mainframe Service Manual for information on replacing the card cage access cover.

NOTE: the boards listed are from the lowest available card cage slot number to the highest.

60 Channel State Configuration

```
1  |--> EMULATION MEMORY BOARD        (lowest available slot number)
   |--> EMULATION MEMORY CONTROLLER BOARD
c  |--> GENERAL PURPOSE OR EMULATION CONTROL BOARD                      4
a  |--> EMULATION BUS PREPROCESSOR BOARD ==========================>|
b       STATE ANALYZER CONTROL BOARD <-------------clock-------------| c
l       STATE ACQUISITION BOARD (40 channel) <-----pods 3,2----------| a
e       STATE ACQUISITION BOARD (20 channel) <-----pod 1-------------| b
                                                                     l
                                                                     e
                                                                     s
```

40 Channel State Configuration

```
1  |--> EMULATION MEMORY BOARD        (lowest available slot number)
   |--> EMULATION MEMORY CONTROLLER BOARD
c  |--> GENERAL PURPOSE OR EMULATION CONTROL BOARD                      3
a  |--> EMULATION BUS PREPROCESSOR BOARD ==========================>|
b       STATE ANALYZER CONTROL BOARD <-----------------clock---------| c
l       STATE ACQUISITION BOARD(s) (40 channels) <-----pods 1,2------| a
e                                                                    | b
                                                                     | l
                                                                     | e
            NOT CONNECTED <----------------------------pod 3---------| s
```

Procedure for installing a 64304A with the State Analyzer in a different mainframe:

a. Turn OFF both 64000 Development Systems.

b. Loosen the two hold-down screws of the 64100A and remove the card cage access covers. Refer to the 64110A Mainframe Service Manual for information on removing the card cage access cover.

c. Insert the 64304A card directly behind either the General Purpose or Emulation Control card of mainframe #1. See below.

d. Insert the State Analysis System into mainframe #2. See below.

e. Connect the clock cable from the 64304A to the clock input socket of the State Analyzer Control board. Connect the pod cable(s) from the 64304A to the corresponding pod cable input of the State Aquisition card(s). Make sure that pin 1 of the pod cable is connected to pin 1 on each of the State Analyzer boards. See below.

f. Install the Emulation Bus cables to the Emulation Memory Control board, either the General Purpose or Emulation Control board, and Emulation Bus Preprocessor board of mainframe #1. The bus cables are keyed so they will connect to the edge connector in only one position. See below.

g. Reinstall the 64100A card cage access covers and tighten the 2 screws. Refer to the 64110A Mainframe Service Manual for information on replacing the card cage access cover.

NOTE: For ease of cabling between 64100A systems the following configurations should be moved towards the BACK of the card cage.

Mainframe #1

```
1  |--> EMULATION MEMORY BOARD        (lowest available slot number)
   |--> EMULATION MEMORY CONTROLLER BOARD
c  |--> GENERAL PURPOSE OR EMULATION CONTROL BOARD
a  |--> EMULATION BUS PREPROCESSOR BOARD ----------------------->| 3 or 4
b                                                               |
l                                                               | c
e                        Connect the Emulation Bus Preprocessor | a
                         to the State Analyzer in mainframe #2  | b
                                                                | l
                                                                | e
                                                                | s
```

Mainframe #2 (see NOTE 1)

```
---------------------------    (lowest available slot number)  |
STATE ANALYZER CONTROL BOARD <-----------------------------------|
STATE AQUISITION BOARD (20 or 40 channel) <----------------------|
STATE AQUISITION BOARD (optional 20 or 40 channel) <-------------|
```

NOTE 1: See the 60 and 40 channel State Analysis configurations on the previous page for more information.

2-4. OPERATING ENVIRONMENT.

The 64304A may be operated in environments within the following limits:

Temperature.....0 to +40 degrees C (+32 to +104 degrees F)
Humidity..... 5% to 80% relative humidity at 40 degrees C
Altitude..... 4 600 m (15 000 ft)

The 64304A should be protected from temperature extremes which cause condensation within the 64000.

2-5. STORAGE AND SHIPMENT.

ENVIRONMENT.

The 64304A may be stored or shipped in environments within the following limits:

Temperature..... -40 to +75 degrees C (-40 to +167 degrees F)
Humidity..... 5% to 80% relative humidity
Altitude.....15 000 m (50 000 ft)

ORIGINAL PACKAGING.

Containers and packaging materials identical to those in factory packaging are available through Hewlett-Packard offices.

OTHER PACKAGING.

The following general instructions should be used for re-packing with commercially available materials:

a. Wrap the 64304A in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the 64304A to provide firm cushioning and prevent movement inside the container.

d. Seal shipping container securely.

e. Mark the shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to the instrument by model number and full serial number.

SECTION III

OPERATION

3-1. INTRODUCTION.

Complete operation of the 64304A is beyond the scope of this service manual. For complete operating instructions refer to the 64304A Operating Manual.

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

Performance Verification for the 64304A supports two forms of State Acquisition board configurations. First, is the 40 channel (total channels) configuration commonly used with State Analysis of 8 bit Microprocessor Emulators. Second, is the 60 channel (total channels) configuration commonly used with State Analysis of 16 bit Microprocessor Emulators. Other total channel configurations are not supported with PV for the 64304A. Other configurations may cause failures during PV tests or cause bad Signature Analysis to occur.

Note, the terms 64304A, Preprocessor, and EBPP will be used throughout this manual in reference to the 64304A Emulation Bus Preprocessor. The term CPU will be used when referring to the 64000 Host Microprocessor. The abbreviation PV will be used when referring to Performance Verification.

4-2. EQUIPMENT REQUIRED.

Equipment required for troubleshooting is listed in table 1-1 Recommended Test Equipment of Section I.

4-3. DESCRIPTION OF PV CONTROL SOFTKEYS.

Press one of the following softkeys to control or run a PV module test:

<end>	This softkey will end a test to the previous PV module or display.
<cycle>	Pressing this softkey will cycle through the tests displayed in a PV module until either the <end> or <cycle> softkeys are pressed.
<run>	Begins execution of the test that is selected.
<next_test>	This softkey moves the inverse video bar to the next test.
<disp_test>	Pressing this softkey will display the PV module that is associated with the test that is covered by the inverse video bar.
<start>	This inverse video softkey begins execution of a PV module test. Press this softkey again to stop a test while displaying that test.
<exit_test>	Pressing this softkey will stop a test and exit to the previous PV module or display.
<print>	This softkey prints the information that is above the status line.

4-4. EMULATION BUS PREPROCESSOR PV OUTLINE.

Table 4-2 is how the 64304A PV tests are structured and documented in this manual. Note that there are three main PV modules. Under each PV module there are sub-tests of that module. Furthermore, there are tests that support each sub-test. These supporting tests will get the user to an IC or a group of ICs that can cause a failure within a PV module.

For example:

```
PART I.  EMULATION BUS PREPROCESSOR BOARD PV MODULE.    <---- PV module

    A) BREAK CONTROL TEST    <----------------------- sub-test of the PV module
         1) Break Set Control    <-----\
         2) Break Reset Control    <----\---- supporting tests for the sub-test
```

4-5. GENERAL EMULATION BUS PREPROCESSOR PV FLOWCHART.

Follow the PV flowchart given in figure 4-1 to determine if the 64304A is operating properly. If a failure occurred while running any of the PV modules refer to paragraph 4-8 Required 64304A Card Cage Configuration before troubleshooting.

4-6. PROCEDURE FOR ACCESSING OPTION TEST.

Use the following procedure to access option test:

a. While in the monitor level display press the <---ETC---> softkey until the <opt_test> softkey is displayed.

b. Press the <opt_test> softkey followed by the RETURN key.

c. "HP 64000 Option Performance Verification" should be displayed followed by a list of all the option boards that are present in the card cage.

d. To access the Performance Verification tests for a certain option board enter the slot number of the board. Press RETURN.

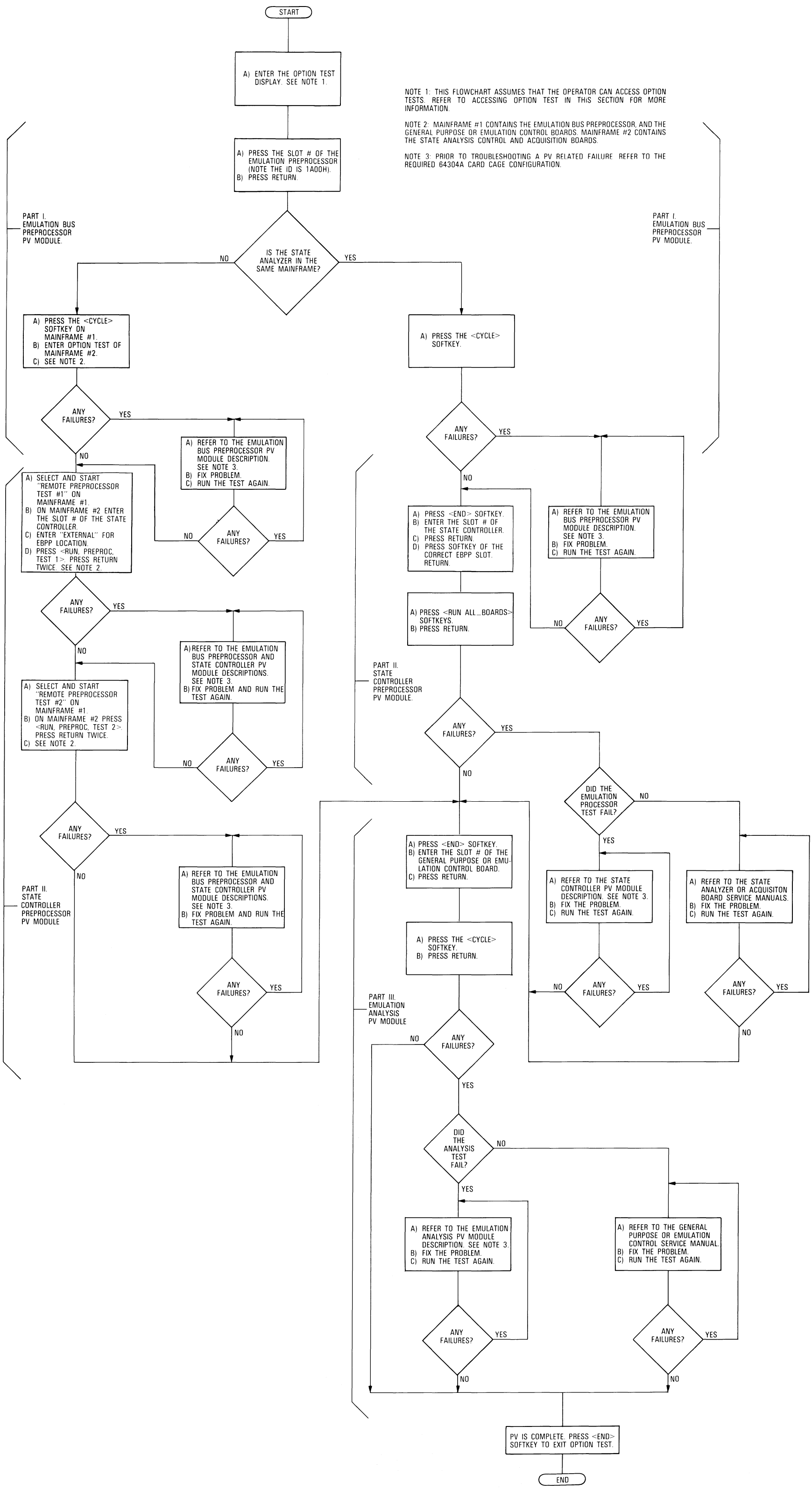


Figure 4-1. General Emulation Bus Preprocessor PV Flowchart

NOTES

4-7. TROUBLESHOOTING AND PV ON THE 64304A.

4-8. REQUIRED 64304A CARD CAGE CONFIGURATION.

Use the following hardware configuration procedure if a PV failure occurred while following the General Emulation Bus Preprocessor PV Flowchart (see figure 4-1):

a. Turn OFF the 64000 and remove any boards other than the EBPP, 40 or 60 channel State Analysis System, and a minimum Emulation Subsystem.

b. The following is the recommended card cage configuration for performing PV. For more detailed information about installing or removing the 64304A refer to Section II (Installation) in this manual.

Card cage configuration for an Emulation Bus Preprocessor and a State Analyzer in the same mainframe (this setup must be used for troubleshooting).

```
NOTE:  The boards listed are from the lowest available card cage slot number to the
highest.

EMULATION MEMORY BOARD        (lowest available slot number)
EMULATION MEMORY CONTROLLER BOARD
GENERAL PURPOSE OR EMULATION CONTROL BOARD
EMULATION BUS PREPROCESSOR BOARD
STATE ANALYZER CONTROL BOARD
STATE ACQUISITION BOARD (40 channel)
STATE ACQUISITION BOARD ( optional 20 channel)
```

Card cage configurations for a Emulation Bus Preprocessor and a State Analyzer in a separate mainframe (this setup for verification only).

```
NOTE:  For ease of cabling between 64100A systems the following configurations should be
moved towards the BACK of the card cage.

Mainframe #1
---------------------------
EMULATION MEMORY BOARD        (lowest available slot number)
EMULATION MEMORY CONTROLLER BOARD
GENERAL PURPOSE OR EMULATION CONTROL BOARD
EMULATION BUS PREPROCESSOR BOARD ------------------------------>|
                                                                |
                  Connect the Emulation Bus Preprocessor        |
                  to the State Analyzer in mainframe #2         |
                                                                |
Mainframe #2                                                    |
---------------------------    (lowest available slot number) |
STATE ANALYZER CONTROL BOARD <---------------------------------|
STATE AQUISITION BOARD (40 channel) <--------------------------|
STATE AQUISITION BOARD (optional 20) <--------------------------|
```

c. Turn ON the 64000.

d. Press the <opt_test> softkey.

e. Prior to troubleshooting refer to table 4-1 for some quick checks of the 64304A board.

f. Refer to the description of the PV module that failed while following the General Emulation Bus Preprocesor PV Flowchart. Table 4-2 is an outline of the tests in each PV module.

Table 4-1. Preliminary Troubleshooting Information

Check the following before troubleshooting the 64304A with PV.

a. Check that the Emulation Bus cables are connected and seated properly (pin 1 is connected to pin 1).

b. Check that the cables going to the State Control (clock) and State Acquisition boards (pods 1-3) are connected and seated properly (pin 1 is connected to pin 1).

c. Check that the PC board is properly seated in the card cage. Note that the contacts connecting the 64304A to the 64000 motherboard are clean.

d. Verify that the board is receiving +5, and -5.2 volts and that circuit ground is not fluctuating.

e. Check that the board identfication number given after the option test display is accessed is 1A00H. If the board ID is not 1A00H the wrong PV Software will be loaded.

Table 4-2. Emulation Bus Preprocessor PV Module Outline

PART I. EMULATION BUS PREPROCESSOR BOARD PV MODULE.

A) BREAK CONTROL TEST
- 1) Break Set Control
- 2) Break Reset Control

B) PATTERN RECOGNITION TEST
- 1) Run/Load Control
- 2) Data Lines
- 3) Step Control
- 4) Pattern Memory

C) REMOTE PREPROCESSOR TEST #1
- 1) Status: "Awaiting Initialization from external analyzer"
- 2) Status: "Stimulating Interface Channels and ID Register"
- 3) Status: "Awaiting Stimulus Break Check"
- 4) Status: "Awaiting Halt Break Check"

D) REMOTE PREPROCESSOR TEST #2
- 1) Status: "Awaiting Initialization from external analyzer"
- 2) Status: "Clocking Data into Analyzer"
- 3) Status: "Awaiting Analysis of Data"

PART II. STATE CONTROLLER PREPROCESSOR PV MODULE.

A) SMART INTERFACE VERIFICATION TEST # 1
- 1) Preprocessor ID Code
- 2) Secondary ID Register and Interface Channels
- 3) Status Word
- 4) Master Reset
- 5) Stimulus Break
- 6) Stimulus Disable
- 7) Halt Break
- 8) Halt Disable

B) CLOCK / DATA CHANNEL VERIFICATION TEST # 2
- 1) Clock Channel 0
- 2) Preprocessor Data Channels
- 3) External Data Channels

PART III. EMULATION ANALYSIS PV MODULE.

ANALYSIS TEST
- 1) Analysis Control
- 2) Address, Data, Status Field

4-9. PART I. EMULATION BUS PREPROCESSOR BOARD PV MODULE.

Entering the Emulation Bus Preprocessor PV Module:

After loading the software for the 64304A use the following procedure to access the 64304A Emulation Bus Preprocessor PV Module:

a. Refer to the procedure for accessing option test at the beginning of this section.

b. Enter the Slot # of the Emulation Preprocessor (note that the ID # is 1A00H).

c. Press RETURN.

The previous procedure should result in the following PV module being displayed:

```
=================================================================
                    Performance Verification
            64304A  Emulation Bus Preprocessor  Slot #4


    Test Description                            #Failures  #Tests
    ----------------                            ---------  ------
 Break Control Test                                  0        0

 Pattern Recognition Test                            0        0

    For Use With External Analyzer Only                     #Tests
    -----------------------------------                     ------
 Remote Preprocessor Test #1                                  0

 Remote Preprocessor Test #2                                  0

=================================================================
```

NOTE

The Remote Preprocessor Tests are NOT used when the EBPP and the State Controller are in the same mainframe. Refer to the Remote Preprocessor Test descriptions in Part I and Part II of this section for more information.

A) BREAK CONTROL TEST

Break Control Test display:

```
=================================================================
                    Performance Verification
          64304A  Emulation Bus Preprocessor  Slot #4
                       Break Control Test

    Test Description            Diagnostics       #Failures  #Tests
    ----------------            -----------       ---------  ------

 Break Set Control                [0000]               0       0

 Break Reset Control              [0000]               0

=================================================================
```

1) BREAK SET CONTROL TEST.

PURPOSE: To test the ability to set the pattern, halt, and stimulus break latches and to check that the associated status bits were correct from U16E, U16J, and U17G.

PROCEDURE: The slot select routine is called to select the EBPP board. 0FH is written to the Control Word Register (U16I) to put the board in a known state. Breaks are reset, set then reset, reading the status each time.

RESULTS: A "1" in the diagnostic indicates that stimulus, halt, pattern, or "any break" could not be set.

```
Diagnostic
  Equals          Indicates
-----------------------------------
  [0000]........No failures
  [1000]........Stimulus fails
  [0100]........Halt fails
  [0010]........Pattern fails
  [0001]........"Any Break" fails

  Note a bad status bit may cause a failure (U16J and U17G).
```

FAILURE: If a failure occurred refer to table 4-3 for information about troubleshooting a Break Set Control Test failure.

A) BREAK CONTROL TEST (Cont'd)

2) BREAK RESET CONTROL TEST.

PURPOSE: To test the ability to reset the pattern, halt, and stimulus break latches and to check that the associated status bits were correct from U16E, U16J, and U17G.

PROCEDURE: Included as part of the Break Set Control procedure.

RESULTS: A "1" in the diagnostic indicates that stimulus, halt, pattern, or "any break" could not be reset.

```
Diagnostic
  Equals          Indicates
-----------------------------------
  [0000]........No failures
  [1000]........Stimulus fails
  [0100]........Halt fails
  [0010]........Pattern fails
  [0001]........"Any Break" fails

  Note a bad status bit may cause a failure (U16J and U17G).
```

FAILURE: If a failure occurred refer to table 4-3 for information about troubleshooting a Break Reset Control Test failure.

Table 4-3. Troubleshooting Break Control Test Diagnostic Failures

IMPORTANT INFORMATION.

This table is meant as an aid to the service person to quickly troubleshoot a Break Control test failure. This involves taking KEY signatures to verify improper operation of the circuit group that would cause each diagnostic failure. If the KEY signature node for a certain diagnostic is bad then that signal path is bad. The IC signal path is given next to each KEY signature(s) along with the signature loop table(s) that pertain to the signal path ICs. If the KEY signature is good then it can be assumed that signal path to that point is good.

If more than one bit in the failure field is set take the key signatures from the top to the bottom of the chart and troubleshoot down the IC signal path of the first bad signature.

For general information about the circuit operation of the Break Control test see the Additional Information section of this table. For theory of operation and schematics see Section VIII (Service) of this manual.

TROUBLESHOOTING.

SA Setup A:

```
NORM MODE

CLOCK - negative edge, TTL, located on TP1 of EBPP.

START - positive edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

STOP  - negative edge, TTL, located on TP2 of 64100A I/O board.
                            located on TP5 of 64110A CPU I/O board.
VH = 007U
```

Break Set Control Troubleshooting Guide:

Diagnostic Failure	KEY Signature (use SA Setup A)	IC Signal Path	SA Table
[1000]	U16J-5 007C	U16J, U17E, U15J, U17J, U17B	4-8
[0100]	U17G-14 002P	U17G, U16E, U17E, U15J, U17J, U17B	4-8
[0010]	U17G-16 002P	U15E, U15J, U17J, U17B	4-8
[0001]	U17G-18 002P	U17G, U16E, U17E, U15E, U15J, U17J, U17B	4-8

Table 4-3. Troubleshooting Break Control Test Diagnostic Failures (Cont'd)

Break Reset Control Troubleshooting Guide:

Diagnostic Failure	KEY Signature (use SA Setup A)		IC Signal Path	SA Table
[1000]	U16J-5	007C	U16J, U17E, U15J, U17J, U17B	4-8
[0100]	U17G-14	002P	U17G, U16E, U17E, U15J, U17J, U17B	4-8
[0010]	U17G-16	002P	U15E, U15J, U17J, U17B	4-8
[0001]	U17G-18	002P	U17G, U16E, U17E, U15E, U15J, U17J, U17B	4-8

ADDITIONAL INFORMATION.

NOTE

Any data referred to in text is NEGATIVE TRUE, i.e. those bits are inverted in hardware. All signal levels referred to in CONTROL paths are the actual hardware levels.

A WRITE TO THE CONTROL WORD REGISTER: The Control Word Register is set by writing to address 4200H. CONTROL path for the write is a low-true pulse on LWCW: U17C, U15J, U17B, and U16I. The DATA path for the write is via the System Bus (located on the mainframe motherboard), through U17I and U16I of the EBPP.

TO SET BREAKS: Breaks are set by writing to address 4600H. CONTROL path for the write is a low-true pulse on LBRKSET: U17B, U17J, U15J, U17E, and U15E. The DATA path is not applicable.

TO RESET BREAKS: Breaks are reset by writing to address 4000H. The CONTROL path for the write is a low-true pulse on LBRKRST: U17B, U17J, U15J, U17E, and U15E. The DATA path is not applicable.

TO READ BOARD STATUS: Board status is read from host address 50xxH (via U17G and U16J), where xx signifies the use of the lower 8 bits to address and read the 256 locations of pattern RAM (00H to FFH). The CONTROL path for reading the status is with LREAD low: U15J, U17C, U17J, U17G, and U16J. The STATUS output path is: U17G, U16J, and System Bus.

B) PATTERN RECOGNITION TEST

Pattern Recognition Test display:

```
=================================================================

                    Performance Verification
          64304A  Emulation Bus Preprocessor  Slot #4
                    Pattern Recognition Test

    Test Description        Diagnostics          #Failures  #Tests
    ----------------        -----------          ---------  ------

 Run/Load Control                                     0        0

 Data Lines                   [000000]                0

 Step Control                    [000]                0

 Pattern Memory               [000000]                0

=================================================================
```

1) RUN/LOAD CONTROL TEST.

PURPOSE: To test that the Run/Load Contol bit (CW7 of U16I) will toggle and select the Emulation Bus Latches (U1J, U1H, U3J thru U7J) or the host RAM Load Buffers (U2J, U3H thru U7H) as the address source for the Pattern RAM (U2F thru U7F). The test assumes RAM address 0AH is good.)

PROCEDURE: Write 0DH to the Control Word Register (load mode). Read the data from RAM address 0AH. Write 80H to the Control Word Register (run mode) and write the complement of the RAM data back to address 0AH. Write 0DH to the Control Word Register (load mode) and read the contents of RAM address 0AH. Again, write the complement of the original RAM data to RAM address 0AH. Read the contents of address 0AH.

RESULTS: Test fails if the RAM data write in run mode (CW7 low) changed the contents of address 0AH, or if the RAM data write in load mode (CW7 high) did not change the data.

FAILURE: If a failure occurred refer to table 4-4 for information about troubleshooting a Run/Load Control test problem.

B) PATTERN RECOGNITION TEST (Cont'd)

2) DATA LINES TEST.

PURPOSE: To check that the RAM write data lines (U17I, U2F thru U7F) will independently toggle. Assume RAM address 00H is good.

PROCEDURE: While in the RAM load mode, write a "1" to RAM address 00H independently on each of the six RAM write data lines reading address 00H after each write. Then write all ones and then all zeros to all six RAMs at address 00H, reading the RAM data after each write.

RESULTS: A failure of any RAM data bit (U17I, U2F thru U7F) to toggle will set that bit (B5 down to B0) in the diagnostic and increment the number of Data Line failures.

```
Diagnostic
  Equals              Indicates
-------------------------------
B5[000000]..........No Failures
  [100000]..........Status Bit SW13 Failed
  [010000]..........Status Bit SW12 Failed
  [001000]..........Status Bit SW11 Failed
  [000100]..........Status Bit SW10 Failed
  [000010]..........Status Bit SW9  Failed
  [000001]..........Status Bit SW8  Failed
  [111111]..........Most likely a RAM control problem
                    (addressing and/or control).
```

FAILURE: If a failure occurred refer to table 4-4 for information about troubleshooting a Data Line failure.

B) PATTERN RECOGNITION TEST (Cont'd)

3) STEP CONTROL TEST.

PURPOSE: To test the Pattern Found Gate (U2H), the second stage of the Timing and Break Strobe Generator (U17B, U9J, U9H, U11H, U11J, R8, C30, RP32, RP33), Pattern Break Latch (U15E), and the Pattern Break Control bit (CW1, U16I).

PROCEDURE: While in the RAM load mode, write all zeros to RAM address 00H, reset breaks, and send one break strobe. Read the status word. Write all ones to RAM address 00H, reset breaks, and send one break strobe. Read the status word. Write 0FH to the control word register, disabling pattern breaks. Reset breaks, send one break strobe, and read the status word.

RESULTS: If a pattern break occurred with pattern false (RAM data all zeros) (U2H, U15E), the upper diagnostic bit is set. If a pattern break did not occur with the pattern true (RAM data all ones) (U2H, U15E), set the middle bit. If the pattern break disable (U16I, U15E) did not work, set the lower diagnostic bit. Increment Step Control fail if any diagnostic bit set.

```
Diagnostic
  Equals                        Indicates
-------------------------------------------------------------
 [000]...........No Failures
 [100]...........Pattern break occurred with pattern false
                 (RAM data all zeros).
 [010]...........Pattern break did not occur with pattern true
                 (RAM data all ones).
 [001]...........Pattern break disable did not work.
```

FAILURE: If a failure occurred refer to table 4-4 for information about troubleshooting a Step Control failure.

B) PATTERN RECOGNITION TEST (Cont'd)

4) PATTERN MEMORY TEST.

PURPOSE: To test the Pattern RAM address lines (U17A, U2J, and U3H thru U7H) and the Pattern RAM data cells of (U2F thru U7F).

PROCEDURE: Write "1s" and then "0s" to every address location in each of the six Pattern RAMs. Then read RAM data from every address location after each write cycle (00H thru 0FFH).

RESULTS: The upper bit of the diagnostic is set for a failure of the addressing circuitry of the Status RAM (U2J, U2F), the next two bits are for the addressing circuitry of the upper and lower Data RAMs (U3H, U3F, and U4H, U4F), and the lower three bits are for the addressing circuitry of the upper, middle and lower Address RAMs (U5H and U5F, U6H and U6F, U7H and U7F). Pattern Memory failures are incremented when any of the diagnostic bits are set. All bits should be set if the write address latch (U17A) fails.

```
Diagnostic
  Equals                          Indicates
-------------------------------------------------------------------
 [000000]........No Failures
 [100000]........Address path of the Status RAM fails (U2J & U2F).
 [010000]........Upper Data byte RAM address path fails (U3H & U3F).
 [001000]........Lower Data byte RAM address path fails (U4H & U4F).
 [000100]........Upper Address byte RAM address path fails (U5H & U5F).
 [000010]........Middle Address byte RAM address path fails (U6H & U6F).
 [000001]........Lower Address byte RAM address path fails (U7H & U7F).
 [111111]........Write Address Latch U17A fails.
```

FAILURE: If a failure occurred refer to table 4-4 for information about troubleshooting a Pattern Memory failure.

Table 4-4. Troubleshooting Pattern Recognition Test Diagnostic Failures

IMPORTANT INFORMATION.

This table is meant as an aid to the service person to quickly troubleshoot a Pattern Recognition test failure. This involves taking KEY signatures to verify improper operation of the circuit group that would cause each diagnostic failure. If the KEY signature node for a certain diagnostic is bad then that signal path is bad. The IC signal path is given next to each KEY signature(s) along with the signature loop table(s) that pertain to the signal path ICs. If the KEY signature is good then it can be assumed that signal path to that point is good.

For general information about the circuit operation of the Pattern Recognition test see the Additional Information section of this table. For theory of operation and schematics see Section VIII (Service) of this manual.

TROUBLESHOOTING.

SA Setup B:

NORM MODE

```
CLOCK - negative edge, TTL, located on TP1 of EBPP.

START - positive edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

STOP -  negative edge, TTL, located on TP2 of 64100A I/O board.
     -                      located on TP5 of 64110A CPU I/O board.

VH = HHU6
```

Run/Load Control Test Troubleshooting Guide:

Diagnostic Failure	KEY Signature (use SA Setup B)	IC Signal Path	SA Table
N/A	U17B-9 96C8 U8J -1 3551	U17B, U8J, U16I, U17I	4-9

NOTE: If the key signatures for this test are good use the Data Lines Test Troubleshooting Guide for fixing a Run/Load Control Test problem.

Table 4-4. Troubleshooting Pattern Recognition Test Diagnostic Failures (Cont'd)

Data Lines Test Troubleshooting Guide:

Diagnostic Failure	KEY Signature (use SA Setup B)	IC Signal Path	SA Table
[111111]	U17B-9 96C8 U8J -1 3551	U17B, U8J, U16I, U17I	4-9
[100000]	U16J-7 692F	U16J, U2F, U17I, U2J, U17A, U8J, U16I, U17B	4-9
[010000]	U16J-9 7143	U16J, U3F, U17I, U3H, U17A, U8J, U16I, U17B	4-9
[001000]	U16J-12 6259	U16J, U4F, U17I, U4H, U17A, U8J, U16I, U17B	4-9
[000100]	U16J-14 6392	U16J, U5F, U17I, U5H, U17A, U8J, U16I, U17B	4-9
[000010]	U16J-16 CH98	U16J, U6F, U17I, U6H, U17A, U8J, U16I, U17B	4-9
[000001]	U16J-18 P9PH	U16J, U7F, U17I, U7H, U17A, U8J, U16I, U17B	4-9

Table 4-4. Troubleshooting Pattern Recognition Test Diagnostic Failures (Cont'd)

Step Control Test Troubleshooting Guide:

Diagnostic Failure	KEY Signature (use SA Setup B)	IC Signal Path	SA Table
[100]	U17G-16 78P4	U15E, U2H, U11J, U9H, U11H, U9J, U16I, U17B	4-9
[010]	U17G-16 78P4	U15E, U2H, U16I, U17B, U11J, U9H, U11H, U9J	4-9
[001]	U17G-16 78P4	U15E, U2H, U16I, U17I, U17B	4-9

Pattern Memory Troubleshooting Guide:

Diagnostic Failure	KEY Signature (use SA Setup B)	IC Signal Path	SA Table
[100000]	U16J-7 692F	U16J, U2F, U17I, U17A, U2J, U8J, U16I	4-9
[010000]	U16J-9 7143	U16J, U3F, U17I, U17A, U3H, U8J, U16I	4-9
[001000]	U16J-12 6259	U16J, U4F, U17I, U17A, U4H, U8J, U16I	4-9
[000100]	U16J-14 6392	U16J, U5F, U17I, U17A, U5H, U8J, U16I	4-9
[000010]	U16J-16 CH98	U16J, U6F, U17I, U17A, U6H, U8J, U16I	4-9
[000001]	U16J-18 P9PH	U16J, U7F, U17I, U17A, U7H, U8J, U16I	4-9
[111111]	N/A	U17A, U17C, U11J	4-9

Table 4-4. Troubleshooting Pattern Recognition Test Diagnostic Failures (Cont'd)

ADDITIONAL INFORMATION.

NOTE

Any data referred to in text is NEGATIVE TRUE, i.e. those bits are inverted in hardware. All signal levels referred to in CONTROL paths are the actual hardware levels.

A WRITE TO THE CONTROL WORD REGISTER: The Control Word Register is set by writing to address 4200H. CONTROL path for the write is a low-true pulse on LWCW: U17C, U15J, U17B, and U16I. The DATA path for the write is via the System Bus (located on the mainframe motherboard), through U17I and U16I of the EBPP.

TO READ BOARD STATUS: Board status is read from host address 50xxH (via U17G and U16J), where xx signifies the use of the lower 8 bits to address and read the 256 locations of pattern RAM (00H to FFH). The CONTROL path for reading the status is with LREAD low: U15J, U17C, U17J, U17G, and U16J. The STATUS output path is: U17G, U16J, and System Bus.

TO SEND A BREAK STROBE: Pattern break is strobed by writing to address 47xxH, where xx signifies the use of the lower 8 bits to address a pattern in one of the 256 locations (00 to FFH) of the pattern RAM. When the Control Word Register is configured to set CW7 high (LOAD mode) RAM is addressed by the host (xx is ignored in the RUN mode). The CONTROL path for writing to RAM is a low-true pulse on LPVSTB to PBRKSTB: U17C, U17B, U9J, U9H, U11H, U11J, and 15E. ADDRESS path for writing to RAM in the LOAD mode is: System Bus, U17A, U2J, U3H thru U7H, and U2F thru U7F. DATA path is not applicable.

TO WRITE DATA TO RAM: Pattern RAM (U2F thru U7F) is loaded by writing to address 41xxH, where xx signifies the use of the lower 8 bits to address the 256 locations (00 to FFH) of the pattern RAM. When the control word register is configured to set CW7 high (LOAD mode) RAM is addressed by the host (xx is ignored in the RUN mode). The CONTROL path for writing to RAM is a low-true pulse on LWBREAK: U17C, U17B, to U2F thru U7F. The ADDRESS path for the write in the LOAD mode is: System Bus, U17A, U2J, U3H thru U7H, to U2F thru U7F. The DATA path for writing to RAM is: System Bus, U17I, U2F thru U7F.

TO READ RAM DATA: When control word register bit seven (CW7) is high the RAM address LOAD mode is asserted, allowing the write address latch to present data to RAM via the RAM load buffers. The ADDRESS path for reading RAM in the LOAD mode is: System Bus, U17A, U2J, U3H thru U7H, and U2F thru U7F. The DATA out path is: U16J, and System Bus. The CONTROL path for reading RAM is a high level on the LWBREAK: U15J, System Bus, U17B, and U2F thru U7F.

C) REMOTE PREPROCESSOR TEST #1

Remote Preprocessor Test #1 display:

```
=================================================================

                    Performance Verification
            64304A  Emulation Bus Preprocessor   Slot #4
                    Remote Preprocessor Test #1

This test enables the user to execute State Analyzer Performance
Verification - Preprocessor Test #1 when the Emulation Bus Prepro-
cessor in this mainframe is connected to a State Analyzer in a dif-
ferent mainframe.  The test must always be started before the assoc-
iated State test and status should be "Awaiting initialization... ".
The test may also be halted at this point.  All results are still
displayed in the State test.


   Test Status...                                          #Tests
  Awaiting initialization from external analyzer             0
  Stimulating Interface Channels and ID register
  Awaiting Stimulus Break Check
  Awaiting Halt Break Check

=================================================================
```

NOTE

This test is provided for ease of testing the State Analyzer/Preprocessor interface when the analyzer is in a different mainframe. It is NOT intended as a complete diagnostic tool for servicing purposes. For servicing, the 64304A should be tested in the SAME mainframe with a State Analyzer.

1) Status: "Awaiting Initialization from external analyzer"

PURPOSE: To synchronize the start of this test and the associated Preprocessor Test #1 in the external mainframe.

PROCEDURE: Slot select the EBPP. Write 0FH to the Control Word Register (load mode). Reading board status, wait for breaks to be reset by the external test, or wait for user input to halt or exit test.

RESULTS: If user input a halt or exit then service the input. If all breaks are set, then, the break drive latches are reset and testing is resumed.

See the associated test in Part II (State Analyzer Preprocessor PV Module) for any procedure explanation.

C) REMOTE PREPROCESSOR TEST #1 (Cont'd)

2) Status: "Stimulating Interface Channels and ID Register".

PURPOSE: To provide the EBPP stimulus of the Smart Interface channels for Preprocessor Test #1 (PT #1), and testing of the data lines and Processor ID register.

PROCEDURE: Write 0FH to the Control Word Register. Delay for 10 msec to allow PT #1 to read EBPP status. Write 00H to the Processor ID Register, and set breaks. Reading status, delay until breaks are reset by PT #1 or for 20 msec. If break reset is received then delay for another 10 msec. Write 0FH to the Control Word Register (reset from PT #1 clears the Control Word Register). Repeat this entire procedure, writing a "walking 1" (a "1" in data bit 7, then bit 6, then bit 5, down to bit 0) to the Processor ID Register and then once more, writing 0FFH. Wait for break reset or 100 msec on the last cycle.

RESULTS: No results; move on to the next part of the test.

3) Status: "Awaiting Stimulus Break Check".

PURPOSE: To determine if stimulus break logic and halt break disable are operating correctly.

PROCEDURE: Write 07H to the Control Word Register. Wait for a stimulus break from Preprocessor Test # 1 (PT #1) or 100 msec. Delay for 10 msec more if stimulus break received. Set breaks and delay for 10 msec. Reset breaks. Wait for halt break (should NOT occur) or 100 msec. Write 0BH to the Control Word Register and set breaks. delay 10 msec and reset breaks.

RESULTS: No results; move on to the next part of the test.

4) Status: "Awaiting Halt Break Check".

PURPOSE: To determine if the halt break logic and stimulus break disable is operating correctly.

PROCEDURE: Wait for halt break from Preprocessor Test #1 (PT#1) or 100 msec. IF break occurs delay 10 msec more. Set breaks. Delay 10 msec and reset breaks. Wait for stimulus break (should NOT occur) or 100 msec. Set breaks. Delay 10 msec and reset breaks. Wait for halt break from PT #1 or 100 msec. If break occurs, delay 10 msec more. Set breaks. Wait breaks to be reset or for 200 msec.

RESULTS: All results are still displayed in Preprocessor Test #1 (PT #1).

D) REMOTE PREPROCESSOR TEST #2

Remote Preprocessor Test #2 display:

```
==================================================================

                    Performance Verification
            64304A  Emulation Bus Preprocessor   Slot #4
                    Remote Preprocessor Test #2

This test enables the user to execute State Analyzer Performance
Verification - Preprocessor Test #2 when the Emulation Bus Prepro-
cessor in this mainframe is connected to a State Analyzer in a dif-
ferent mainframe.  The test must always be started before the assoc-
iated State test and status should be "Awaiting initialization... ".
The test may also be halted at this point.  All results are still
displayed in the State test.


     Test Status...                                          #Tests
   Awaiting initialization from external analyzer              0
   Clocking data into analyzer
   Awaiting analysis of data

==================================================================
```

NOTE

This test is provided for the ease of testing the State Analyzer/Preprocessor interface when the analyzer is in a different mainframe. It is NOT intended as a complete diagnostic tool for servicing purposes. For servicing, the 64304A should be tested in the SAME mainframe with a State Analyzer.

1) Status: "Awaiting Initialization from external analyzer"

PURPOSE: To synchronize the start of this test and the associated Preprocessor Test #2 (PT #2) in the external mainframe.

PROCEDURE: Slot select the EBPP. Write 0FH to the Control Word Register (load mode). Reading board status, wait for breaks to be reset by the external test, or wait for user input to halt or exit test.

RESULTS: If user input a halt, or exit, then service the input. If any breaks occur reset then proceed with testing.

See the associated test in Part II (State Analyzer Preprocessor PV Module) for any procedure explanation.

D) REMOTE PREPROCESSOR TEST #2 (Cont'd)

2) Status: "Clocking Data into Analyzer".

PURPOSE: To test multiplexors, TTL-to-ECL translators, and data lines to the analyzer.

PROCEDURE: Call routines to initialize and run the State analyzer. Slot select the EBPP. Read the Write Status Buffer and reset breaks. Write 00H to the Control Word Register. Clock a "0" to the State Analyzer. Write 01FH to the Control Word Register. Clock a "0" to the State Analyzer. Write a 02FH to the Control Word Register. Clock a "0" to the State Analyzer. Clock a "walking 1's" (a "1" in bit 0, then bit 1,...) pattern into the State Analyzer, clocking in each data pattern twice, once after writing 0FH to the Control Word Register and again after writing 03FH to the Control Word Register. Write 0FH to the Control Word Register and clock 0FFH into the State Analyzer. Write 03FH to the Control Word Register and clock 0FFH into the State Analyzer. Stop the State Analyzer and compare trace data with the data that was sent.

RESULTS: All results are displayed in Preprocessor Test #2.

3) Status: "Awaiting Analysis of Data".

PURPOSE: To synchronize end of this test with end of Preprocessor Test #2 (PT#2).

PROCEDURE: Set breaks. Wait for break reset from PT #2 or 800 msec. Write 0FH to the Control Word Register.

RESULTS: N/A

4-10. PART II. STATE CONTROLLER PREPROCESSOR PV MODULE

Entering the State Controller PV Module:

Use the following procedure to access the State Controller PV Module:

a. Refer to the procedure for accessing Option Test at the beginning of this section.

b. Enter the Slot # of the State Controller board. Press return.

c. A "Select preprocessor board for test: slot_X" will be displayed. X = the slot number of the EBPP. NOTE: The system should default to the slot number of the EBPP if it is the only preprocessor in the card cage. However, pressing the <slot_X> softkey indicating the slot location of the EBPP may also be done.

d. Press RETURN.

The previous procedure should result in the following PV module being displayed:

```
=================================================================

10 MHz State Test: Configuration

     Slot    ID        Description                Part Number
     ----    --        -----------                -----------
  10 MHz boards included
       6    1100   State Control and Clock        64621A  STATE-CT
       7    1200   40 Channel Acquisition         64622A  STATE-40
       8    1200   40 Channel Acquisition         64622A  STATE-40
    preproc   81   Emulation Bus Preprocessor     64304A  EBPP

  10 MHz boards excluded

  Boards for IMB testing


=================================================================
```

The procedures for executing the Emulation Bus Preprocessor interface tests are on the following page.

PART II. STATE CONTROLLER PREPROCESSOR PV MODULE (Cont'd)

The following procedures explain how to access the Emulation Bus Preprocessor PV Module of the State Controller PV module to verify proper operation of the State Controller to Emulation Bus Preprocessor interface.

State Controller and Emulation Bus Preprocessor in separate mainframes: (NOTE: This setup for verification only)

NOTE

This test is provided for ease of testing the State Analyzer/Preprocessor interface when the analyzer is in a different mainframe. It is NOT intended as a complete diagnostic tool for servicing purposes. For servicing, the 64304A should be tested in the SAME mainframe with a State Analyzer.

a. With the State Controller in mainframe #1 enter the State Controller PV module. Answer "external" to the "Select preprocessor board for test:" message that is displayed. Press RETURN.

b. Press these softkeys in sequence <run>, and <preproc>.

NOTE

To run each interface test separately press in sequence <run>, <preproc>, <test>, then enter either a "1" or "2" for the desired interface test. The descriptions of each of the interface test modules are given in the remainder of the documentation for the State Controller Preprocessor PV Module.

c. Press RETURN. The Emulation Bus Preprocessor automatic interface PV module will be displayed. A WARNING message will be displayed above the status line before each interface test prompting the user to start the corresponding Remote Preprocessor test before continuing the test.

d. Enter the Emulation Bus Preprocessor PV module in mainframe #2. Refer to the description of the Emulation Bus Preprocessor PV module for a procedure on entering this test.

e. Press the <next_test> softkey until the inverse video bar covers Remote Preprocessor Test #1 or #2.

f. Press the <disp_test> softkey to display the selected test.

g. Press <start> softkey on mainframe #2 to start the Remote Preprocessor Test.

h. Press RETURN on mainframe #1 to start the test.

PART II. STATE CONTROLLER PREPROCESSOR PV MODULE (Cont'd)

State Controller and Emulation Bus Preprocessor in the same mainframe: (NOTE: This setup is required for troubleshooting)

a. To perform the Emulation Bus Preprocessor automatic interface tests press in sequence, while in the State Controller PV module display, <run> and <preproc>. NOTE: To repeat this test continuously press <run, preproc, repeat> softkeys in sequence.

NOTE

To run each interface test separately press in sequence <run>, <preproc>, <test>, then enter either a "1" or "2" for the desired interface test. The descriptions of each of the interface test modules are given in the remainder of the documentation for the State Controller Preprocessor PV Module.

b. Press RETURN to begin the automatic interface tests.

The previous procedure should result in the following PV module being displayed:

```
=================================================================

10 MHz State Test: Preprocessor              Tested:   0  Failed:   0

    Test   Preproc: Emulation Bus Preprocessor       Tested   Failed
    ----   ----------------------------------        ------   ------
  Automatic Tests
      1    Smart Interface Verification                   0        0
      2    Clock / Data Channel Verification              0        0

=================================================================
```

A) SMART INTERFACE VERIFICATION TEST # 1

Emulation Bus Preprocessor Interface Test #1 display:

```
=================================================================

10 MHz State Test: Preprocessor       Pass  Tested:   1  Failed:   0

  Preproc: Emulation Bus Preprocessor         Location:  Slot #6
  Test  1: Smart Interface Verification

 Diagnostics
  76543210      Test Description
  --------      ----------------
  00000000      Preprocessor ID code (1=Error)
  00000000      Secondary ID register and Interface channels(1=Error)

    Pass        Status Word
    Pass        Master Reset
    Pass        Stimulus Break
    Pass        Stimulus Disable
    Pass        Halt Break
    Pass        Halt Disable

=================================================================
```

1) PREPROCESSOR ID CODE TEST.

PURPOSE: To re-test the Preprocessor ID Buffer (tests would not be loaded if problem exists) (U11J, U13J, and U12J) for data 81H.

PROCEDURE: Select State control board. Read preprocessor ID over smart interface.

RESULTS: Set diagnostic bits not corresponding to 10000001B. (failure of U11J, U13J, and U12J).

```
For Example:

 Diagnostic equals:  00100100  Indicates  bits 5  and 2 of  the internal
                               data bus LID0-7, from the EBPP, were read
                               as a "1" instead  of a "0" as   expected.
                               However, bits 7 and 0 are opposite  this.
```

FAILURE: If a failure occurred refer to table 4-5 for information about troubleshooting a Preprocessor ID Code failure.

A) SMART INTERFACE VERIFICATION TEST # 1 (Cont'd)

2) SECONDARY ID REGISTER AND INTERFACE CHANNELS TEST.

PURPOSE: To test the Processor ID Register and excercise the the interface data channels (U11J, U13J, U15I, and U15G).

PROCEDURE: Slot select the EBPP. Write 0FH to the Control Word Register. Set breaks. Write 00H to the Processor ID Register. Slot select the State Control Board and read the processor ID over the Smart Interface. Slot select the EBPP, write a "walking 1" (a "1" in bit 7, then bit 6, bit 5, ...down to bit 0) while selecting the State Control board and reading the ID over the Smart Interface after each write. Repeat the procedure once more writing 0FFH to the Control Word Register.

RESULTS: Bits are set in the diagnostic corresponding to the bad register bit or data line (bit 7 thru bit 0) (U11J, U13J, U15I, and U15G).

FAILURE: If a failure occurred refer to table 4-5 for information about troubleshooting a Secondary ID Register and Interface Channels test failure.

3) STATUS WORD TEST.

PURPOSE: To test the Write Preprocessor Status Buffer of the Analysis Smart Interface (U11J, U13J, and U16G).

PROCEDURE: Slot select the State Control board. Read EBPP status over the Smart Interface. Slot select the EBPP and read status. Set breaks. Slot select the State Control board and read the EBPP status. Slot select the EBPP and reset breaks. Slot select the State Control board and read the EBPP status.

RESULTS: Test will fail if lower 8 bits of Smart Interface status are not the same as the board status, or if the smart interface status doesn't correctly show that the breaks were set or reset (U11J, U13J, and U16G).

FAILURE: If a failure occurred refer to table 4-5 for information about troubleshooting a Status Word test problem.

A) SMART INTERFACE VERIFICATION TEST # 1 (Cont'd)

4) MASTER RESET TEST.

PURPOSE: To test the smart interface master reset of the EBPP (U11J, U13J, U17J, U15J, U15I, U16I, U15E, and U17E).

PROCEDURE: Slot select the EBPP. Set breaks and write 00H to the Processor ID Register. Slot select the State Sontrol board and assert master reset over the Smart Interface. Read the Processor ID Register and EBPP status over the Smart Interface.

RESULTS: Test fails if processor ID is not reset to 0FFH, or breaks are not reset.

FAILURE: If a failure occurred refer to table 4-5 for information about troubleshooting a Master Reset test problem.

5) STIMULUS BREAK TEST.

PURPOSE: To test the stimulus break logic of U11J, and U17E.

PROCEDURE: Call routines to set up the State Analyzer and load the hardware to assert stimulus on a trigger. Slot select the EBPP. Write 07H to the Control Word Register. Reset breaks. Call routines to execute a trace of the State Analyzer. Read status.

RESULTS: Test fails if stimulus break does not occur via U11J, and U17E.

FAILURE: If a failure occurred refer to table 4-5 for information about troubleshooting a Stimulus Break test problem.

6) STIMULUS DISABLE TEST.

PURPOSE: To test stimulus break control bit CW3 of U16I. NOTE: this test is done during a Halt Break test.

PROCEDURE: Load the State Analyzer to assert the stimulus line on a trigger. Slot select the EBPP. Write 0BH to the Control Word Register. Reset breaks. Execute a trace of the State Analyzer. Read the status of the EBPP.

RESULTS: Test fails if Stimulus Break test fails or if stimulus break could not be disabled (U16I).

FAILURE: If a failure occurred refer to table 4-5 for information about troubleshooting a Stimulus Disable test problem.

A) SMART INTERFACE VERIFICATION TEST # 1 (Cont'd)

7) HALT BREAK TEST.

PURPOSE: To test the Halt Break logic.

PROCEDURE: Load State Analyzer to assert the halt line on trace point. Slot select the EBPP. Write 0BH to the Control Word Register. Reset breaks. Slot select the State Control board. Assert preprocessor clear over the Smart Interface. Execute a trace of the State Analyzer again. Read the status of the EBPP. Perform Stimulus Disable test, then repeat procedure again.

RESULTS: Test fails if halt break did not occur both times (U11J, U13J, U15E, U17E, and U10J).

FAILURE: If a failure occurred refer to table 4-5 for information about troubleshooting a Halt Break test problem.

8) HALT DISABLE.

PURPOSE: To test halt break control bit CW2 of U16I. NOTE: this test is done after the Stimulus Break test.

PROCEDURE: Load the State Analyzer to assert the halt line on trace point. Slot select the EBPP. Write 07H to the Control Word Register. Reset breaks. Execute a trace of the State Analyzer. Read the status of the EBPP.

RESULTS: Test fails if Halt Break test fails or if the halt break could not be disabled (U16I, U10J, and U15E).

FAILURE: If a failure occurred refer to table 4-5 for information about troubleshooting a Halt Disable test problem.

Table 4-5. Troubleshooting Smart Interface Test #1 Diagnostic Failures

IMPORTANT INFORMATION.

This table is meant as an aid to the service person to quickly troubleshoot a Smart Interface verification test # 1 failure. This involves taking KEY signatures to verify improper operation of the circuit group that would cause each diagnostic failure. If the KEY signature node for a certain diagnostic is bad then that signal path is bad. The IC signal path(s) is given next to each KEY signature(s) along with the signature loop table(s) that pertain to the signal path ICs. If the KEY signature is good then it can be assumed that signal path to that point is good.

For general information about the circuit operation of the Smart Interface test see the Additional Information section of this table. For theory of operation and schematics see Section VIII (Service) of this manual.

TROUBLESHOOTING.

SA Setup C:

```
CLOCK - negative edge, TTL, located on U11J-12 of EBPP.

START - positive edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

STOP  - negative edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

VH = 399F
```

SA Setup D:

```
CLOCK - negative edge, TTL, located on TP1 of EBPP.

START - positive edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

STOP  - negative edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

VH = 99FA
```

Table 4-5. Troubleshooting Smart Interface Test #1 Diagnostic Failures (Cont'd)

Preprocessor ID Code Test Troubleshooting Guide:

Diagnostic Failure	KEY Signatures * (use SA Setup C)	IC Signal Path	SA Table
00000001	U16G-18 2FP9	U2J, U13J, U11J	4-10
00000010	U16G-16 HCH3	" " "	"
00000100	U16G-14 HA50	" " "	"
00001000	U16G-12 FHUH	" " "	"
00010000	U16G- 9 FCU2	" " "	"
00100000	U16G- 7 Pulsing probe	" " "	"
01000000	U16G- 5 Pulsing probe	" " "	"
10000000	U16G- 3 Pulsing probe	" " "	"

* NOTE: Key signatures are given on U16G due to easy accessability of its pins. U16G and U15G should be tri-stated during the Preprocessor ID Code test.

Secondary ID Register and Interface Channels Troubleshooting Guide:

Diagnostic Failure	KEY Signatures (use SA Setup C)	IC Signal Path *	SA Table
00000001	U15G-18 2FP9	} There are two IC	
00000010	U15G-16 HCH3	} Signal Paths available	
00000100	U15G-14 HA50	} for this test. Follow the	
00001000	U15G-12 FHUH	} paths in the order given:	
00010000	U15G- 9 FCU2	}	
00100000	U15G- 7 Pulsing probe	} U15G, U13J, U11J	4-10
01000000	U15G- 5 Pulsing probe	} then	
10000000	U15G- 3 Pulsing probe	} U15I, U17B, U17I	4-11

Table 4-5. Troubleshooting Smart Interface Test #1 Diagnostic Failures (Cont'd)

Status Word Test Troubleshooting Guide:

Diagnostic Failure	KEY Signature	IC Signal Path	SA Table
Fail	N/A	U16G, U13J, U11J	4-10
		then	
		U17G	4-11

Master Reset Test Troubleshooting Guide:

Diagnostic Failure	KEY Signature	IC Signal Path	SA Table
Fail	N/A	U15G, U15I, U15J, U17J, U13J, U11J, U16G, U16E, U15E, U17E, U16I	4-10

Stimulus Break Test Troubleshooting Guide:

Diagnostic Failure	KEY Signature (use SA Setup D)	IC Signal Path	SA Table
Fail	U17E- 7 46A3	U17E, U11J	4-11

Stimulus Disable Test Troubleshooting Guide:

Diagnostic Failure	KEY Signature (use SA Setup D)	IC Signal Path	SA Table
Fail	U17E- 7 46A3	U17E, U16I, U17I, U17B	4-11

Halt Break Test Troubleshooting Guide:

Diagnostic Failure	KEY Signature (use SA Setup D)	IC Signal Path	SA Table
Fail	U17E- 9 44C7	U17E, U15E, U10J, U11J	4-11
		then	
		U13J	4-10

Table 4-5. Troubleshooting Smart Interface Test #1 Diagnostic Failures (Cont'd)

Halt Disable Test Troubleshooting Guide:

Diagnostic Failure	KEY Signature (use SA Setup D)	IC Signal Path	SA Table
Fail	U17E- 9 44C7	U17E, U15E, U10J, U16I, U17I, U17B, U13J, U11J	4-11

ADDITIONAL INFORMATION.

NOTE

Any data referred to in text is NEGATIVE TRUE, i.e. those bits are inverted in hardware. All signal levels referred to in CONTROL paths are the actual hardware levels.

READING PREPROCESSOR ID OVER SMART INTERFACE: With the State Control board selected, a read from address 6000H reads the EBPP ID code over the Preprocessor Interface Bus (PPIB, clock cable to State Analyzer). The CONTROL path is a low-true pulse on LWID: State Analyzer, PPIB, U11J, U13J, and U12J. ADDRESS path not applicable. The DATA path is: U12J, PPIB, State Analyzer, and System Bus.

WRITE TO THE PROCESSOR ID REGISTER: The Processor ID Register is set by writing to address 4300H. The CONTROL path for the write is a low-true pulse on LWEMID: U17C, U15J, U17B, and U15I. The DATA path for the write is: System Bus, U17I, U15I, U15G, PPIB, and State Analyzer.

READ THE PROCESSOR ID OVER THE SMART INTERFACE: With the State Control board selected, a read from address 6002H reads the processor ID register over the PPIB. CONTROL path is a low-true pulse on LWED: State Analyzer, PPIB, U11J, U13J, and U15G. The ADDRESS path is not applicable. The DATA path is: U15I, U15G, PPIB, State Analyzer, and System Bus.

READING STATUS OVER SMART INTERFACE: With the State Control board selected, a read from address 6001H reads the EBPP status register over the PPIB. CONTROL path is a low-true pulse on LWPS: State analyzer, PPIB, U11J, U13J, and U16G. The ADDRESS path is not applicable. The DATA path is: U16G, PPIB, State Analyzer, and System Bus.

ASSERT MASTER RESET OVER SMART INTERFACE: With the State Control board selected, a write to address 6003H resets EBPP breaks, Control Word Register, Processor ID Register, and host address latch over the PPIB. The CONTROL path is a low-true pulse on LIMRST: State Analyzer, PPIB, U11J, U13J, U17J, and U15J. The ADDRESS path is not applicable. The DATA path is not applicable.

ASSERT PREPROCESSOR CLEAR OVER SMART INTERFACE: With the State Control board selected, a write to address 6000H sends a preprocessor clear pulse to the EBPP, over the PPIB, to qualify the State Analyzer loading of the Halt line hardware on the EBPP. The CONTROL path is a low-true pulse on LWHQCLK: State Analyzer, PPIB, U11J, U13J, and U15E. The ADDRESS path is not applicable. The DATA path is not applicable.

B) CLOCK / DATA CHANNEL VERIFICATION TEST # 2

Emulation Bus Preprocessor Interface Test #2 display: The following is displayed for 16 bit State Analysis configurations using 60 channels of State Acquisition.

```
=================================================================

10 MHz State Test: Preprocessor       Pass  Tested:   1  Failed:   0

  Preproc: Emulation Bus Preprocessor         Location:  Slot #6
  Test  2: Clock / Data Channel Verification

  Diagnostics   Test Description
  -----------   ----------------
     Pass       Clock Channel 0
     Pass       Preprocessor Data Channels [ Pods 1,2,3 ]
      N/A       External Data Channels

Slot            19     Channels     0          19     Channels     0
----            ---------------------          ---------------------
  9      Pod 1:  00000000000000000000
  8      Pod 2:  00000000000000000000   Pod 3:  00000000000000000000

=================================================================
```

Emulation Bus Preprocessor Interface Test #2 display: The following is displayed for 8 bit State Analysis configurations using 40 channels of State Acquisition.

```
=================================================================

10 MHz State Test: Preprocessor       Pass  Tested:   1  Failed:   0

  Preproc: Emulation Bus Preprocessor         Location:  Slot #6
  Test  2: Clock / Data Channel Verification

  Diagnostics   Test Description
  -----------   ----------------
     Pass       Clock Channel 0
     Pass       Preprocessor Data Channels [ Pods 1,2 ]
      N/A       External Data Channels

Slot            19     Channels     0          19     Channels     0
----            ---------------------          ---------------------
  8      Pod 1:  00000000000000000000   Pod 2:  00000000000000000000

=================================================================
```

B) CLOCK / DATA CHANNEL VERIFICATION TEST # 2 (Cont'd)

1) CLOCK CHANNEL 0 TEST.

PURPOSE: To determine that the second stage of the Timing and Break Strobe Generator can create clocks for the State Analyzer.

PROCEDURE: After the data has been clocked into the State Analyzer for the Preprocessor Data Channels test, the State Control board is selected and the current value of the State Counter is read.

RESULTS: Test fails if the number of clocks received by the State Analyzer (current value of the State Counter) was not equal to the 21 clock pulses from U11H.

FAILURE: If a failure occurred refer to table 4-6 for information about troubleshooting a Clock Channel 0 test problem.

2) PREPROCESSOR DATA CHANNELS TEST.

PURPOSE: To test the Data Multiplexors and TTL-to-ECL translators (U10J, U8H, U8F thru U11F, U2D, U3D, and U6D thru U15D).

PROCEDURE: Call routines to initialize and run the State analyzer. Slot select the EBPP. Read the Write Status Buffer and reset breaks. Write 00H to the Control Word Register. Clock a "0" to the State Analyzer. Write 01FH to the Control Word Register. Clock a "0" to the State Analyzer. Write a 02FH to the Control Word Register. Clock a "0" to the State Analyzer. Clock a "walking 1's" (a "1" in bit 0, then bit 1,...) pattern into the State Analyzer, clocking in each data pattern twice, once after writing 0FH to the Control Word Register and again after writing 03FH to the Control Word Register. Write 0FH to the Control Word Register and clock 0FFH into the State Analyzer. Write 03FH to the Control Word Register and clock 0FFH into the State Analyzer. Stop the State Analyzer and compare trace data with the data that was sent.

RESULTS: Bits are set in the pod diagnostics in each bit where incorrect data was received by the State Analyzer. Any bit set in the diagnostic will cause the test to fail.

FAILURE: If a failure occurred refer to table 4-6 for information about troubleshooting a Preprocessor Data Channels test problem.

B) CLOCK / DATA CHANNEL VERIFICATION TEST # 2 (Cont'd)

3) EXTERNAL DATA CHANNELS.

PURPOSE: To test the threshold functionality of any General Purpose Probe(s) connected to extra channels of the State Analyzer. This test has NOTHING to do with the Emulation Bus Preprocessor test. The test will fail if any State Analyzer data channels not used by the 64304A are not connected to a General Purpose Probe.

PROCEDURE: The General Purpose Probe thresholds are set in the maximum positive position. The State Analyzer then executes a trace and one analyzer PV strobe is sent to clock in the data. Probe thresholds are then set in the maximum negative position and another PV strobe is sent. The State Analyzer is stopped and the trace data is read.

RESULTS: Diagnostic bits are set for any EXTERNAL channel bit that did not toggle and the test will fail when a bit is set.

FAILURE: If a bit is set in the diagnostic refer to the service manual for that General Purpose Probe. The mainframe slot number of the State Acquisition board that the failing G. P. Probe is connected to is displayed under "Slot".

Table 4-6. Troubleshooting Clock/Data Channel Test #2 Diagnostic Failures

IMPORTANT INFORMATION.

This table is meant as an aid to the service person to quickly troubleshoot a Clock/Data Channel verification test # 2 failure. This involves taking KEY signatures to verify improper operation of the circuit group that would cause each diagnostic failure. If the KEY signature node for a certain diagnostic is bad then that signal path is bad. The IC signal path(s) is given next to each KEY signature(s) along with the signature loop table(s) that pertain to the signal path ICs. If the KEY signature is good then it can be assumed that signal path to that point is good.

For general information about the circuit operation of the Clock/Data Channel test see the Additional Information section of this table. For theory of operation and schematics see Section VIII (Service) of this manual.

TROUBLESHOOTING.

SA Setup E:

```
CLOCK - negative edge, TTL, located on TP1 of EBPP.

START - positive edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

STOP  - negative edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

VH = 2C34
```

Clock Channel 0 Test Troubleshooting Guide:

Diagnostic Failure	KEY Signature (use SA Setup E)	IC Signal Path	SA Table
Fail	U11H-7 TOTLZ=0021 ECL	U11H, U9H, U9J, U17B	4-12

Table 4-6. Troubleshooting Clock/Data Channel Test #2 Diagnostic Failures

Preprocessor Data Channels Test Troubleshooting Guide PART 1 of 2:

Diagnostic Failure	KEY Signature (use SA Setup E)	IC Signal Path	SA Table
If a pod is not not recognized all data channels fail "[Pods x, x]".	Pod 1: U17G-11 low	J6, U17G	4-12
	Pod 2: U17G-15 low	J5, U17G	4-12
	Pod 3: U17G-13 low	J4, U17G	4-12

Preprocessor Data Channels Test Troubleshooting Guide PART 2 of 2:

Diagnostic Failure	KEY Signature (use SA Setup E)	IC Signal Path	SA Table
A "1" set in diagnostic for a bad channel(s).	N/A	U2D-U15D, U8F-U11F U8H, U10J, U2J, U3H-U7H, U17A, U8J, U17B, U16I, U17I	4-12

ADDITIONAL INFORMATION.

CLOCKING DATA TO THE ANALYZER: Data is strobed to the State analyzer by writing to address 47xxH, where xx signifies the byte pattern of data sent to the State Analyzer. The byte pattern is generated across each byte of the 48 channels sent to the State Analyzer, except for the high data byte which is inverted. Again, xx is only meaningful in the LOAD mode, CW7 high. The CONTROL path for the write is a low-true pulse on LPVSTB to HCK0 and LCK0: U17C, U17B, U9J, U9H, U11H, PPIB, State Analyzer. The ADDRESS path for the write in LLOAD mode is: System Bus, U17A, U2J and U3H thru U7H, U8F thru U11F, U2D thru U15D, PPIB, State Analyzer. The DATA path is not applicable.

4-11. PART III. EMULATION ANALYSIS PV MODULE.

Entering the Emulation Analysis PV Module:

Use the following procedure to access the Emulation Analysis PV Module:

a. Refer to the procedure for accessing Option Test at the beginning of this section.

b. Enter the Slot # of either the Emulator or the General Purpose Control board.

c. Press RETURN. A "Select analysis board for test:" message should be displayed.

d. Input the <slot #> of the Emulation Preprocessor, note that the ID # is (1A00H). Press RETURN>

The previous procedure should result in the following PV module being displayed:

```
=====================================================================

              XXXXXX Emulator Performance Verification

 XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
 XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

      Test                                          # Fail  # Test

 Control board                                          0       0

 Pod register                                           0       0

 Pod functionality                                      0       0

 Analysis                                               0       0

=====================================================================
```

f. Press the <cycle> softkey to verify that the Emulator will pass PV.

NOTE

ONLY the "Analysis" test in the Emulator PV Module is of concern for verifying the operation of the Emulation Bus Preprocessor. However, it is most likely that the "Analysis" test will fail if any of the other Emulator PV tests fail.

The remainder of this procedure is on the following page.

PART III. EMULATION ANALYSIS PV MODULE (Cont'd).

f. If only the "Analysis" test fails press the <cycle> softkey to stop testing. Press the <next_test> softkey until the inverse video bar covers the "Analysis" test. Press the <disp_test> softkey and the following PV module should be displayed.

The Analysis Test display with preprocessor selected.

```
=================================================================

           XXXXXX Emulation System Performance Verification

 XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
 XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
    Analysis Test - Emulation Bus Preprocessor
                        Diagnostics  (Cumulative)     # Fail  # Test
 Analysis Control          Control : 000(000)              0       0

 Address Field             Address : 000(000)              0

 Data Field                   Data : 00(00)                0

 Status Field                                              0


=================================================================
```

The reminder of the documentation for the Emulation Analysis PV Module examines each of the tests displayed above.

1) ANALYSIS CONTROL TEST.

PURPOSE: To test the EBPP emulation break and break control logic (U1D, and CW0 of U16I), and the first stage of the Timing and Break Strobe Generator (U8J, U9J, U9H, U11H, R12, R7, C29, RP32, and RP33).

PROCEDURE: Slot select the EBPP. Write a 0CFH to the Control Word Register. Reset breaks. Call routines to configure, load and run the Emulator. Slot select the EBPP. Write a 0CEH to the Control Word Register. Set breaks. Call routine to read emulator status. Slot select the EBPP. Write 0CFH to the Control Word Register. Reset breaks. Call routine to configure, load and run the Emulator. Slot Select the EBPP. Set breaks. Call a routine to read emulator status. Slot select the EBPP. Write a 0FH to the Control Word Register. Load Pattern RAM with a don't care pattern (this will make the pattern out always true). Write a 0CFH to the Control Word Register and reset breaks. Call routines to configure, load and run the Emulator. Slot select the EBPP. Write 0CCH to the Control Word Register. Call a routine to read emulator status. Slot select the EBPP. Write 08FH to the Control Word Register and reset breaks. Call routines to configure, load and run the Emulator. Slot select the EBPP. Write 08CH to the Control Word Register. Call routine to read emulator status.

RESULTS: Upper diagnostic bit is set if no break is received by the emulator (U16I, and U1D). Middle bit is set if break can't be disabled (U16I, and U1D). Lower bit is set if pattern break could not be clocked by the emulator (timing strobe LANAL U8J, U9J, U9H, U11H, R12, R7, C29, RP32, and RP33), or if pattern break could not be disabled (U16I, and U9J). Test fails if any bit is set in the diagnostics.

Diagnostic Equals		Indicates
Control :	000(000)	No failures
	100(100)	No break from the EBPP was received by the emulator.
	010(010)	Break could not be disabled.
	001(001)	Pattern break could not be clocked by the emulator or disabled by the host processor. If the Address, Data, Status Field tests fail then a pattern break could not be clocked by the emulator or vice versa.

The failures in parenthesis are the cumlative failures for that test.

FAILURE: If a failure occurred refer to table 4-7 for information about troubleshooting an Analysis Control test problem.

2) ADDRESS, DATA, STATUS FIELD TEST.

PURPOSE: To test the Address, Data, and Status field input latches on the emulation bus.

PROCEDURE: Slot select the EBPP. Write 0FH to the Control Word Register and reset breaks. Call routines to configure, load and run the Emulator. Slot select the EBPP. Read emulator cycle data. If new bits are tested by this cycle, write 0FH to the Control Word Register and then load pattern RAM with cycle data using don't cares for a byte if entire byte not defined. Reset breaks and write 0CDH to the Control Word Register. Read status, delay for 1 msec or until a pattern break occurs. If pattern break doesn't occur, then load RAM with don't care patterns (looking for the faulty latch) until the pattern break occurs. Repeat until all cycles have been checked.

RESULTS: Set bits in the diagnostics corresponding to the latches that did not pass correct data; upper, middle and lower byte Emulation Address latches (U5J, U6J, and U7J), upper and lower byte Emulation Data latches (U3J, and U4J), and Emulation Status byte latch (U1H). Test fails if associated diagnostic bit is set.

```
Diagnostic
  Equals                                  Indicates
-------------------------------------------------------------------
Address: 000(000).........No failures
         100(100).........Emulation Address Latch U5J wrote bad data.
         010(010).........Emulation Address Latch U6J wrote bad data.
         001(001).........Emulation Address Latch U7J wrote bad data.

   Data: 00(00)...........No failures
         10(10)...........Emulation Data Latch U3J wrote bad data.
         01(01)...........Emulation Data Latch U4J wrote bad data.

 Status: 0................No failure
         1................Emulation Status Latch U1H wrote bad data.
```

FAILURE: If a failure occurred refer to table 4-7 for information about troubleshooting a Address, Data, Status Field test problem.

Table 4-7. Troubleshooting Analysis Test Diagnostic Failures

IMPORTANT INFORMATION.

This table is meant as an aid to the service person to quickly troubleshoot a Analysis test failure. The IC signal path is given next to each KEY node. If the KEY node is good then it can be assumed that signal path to that point is good.

For theory of operation of the circuitry that is tested by the Analysis test see Section VIII (Service) of this manual.

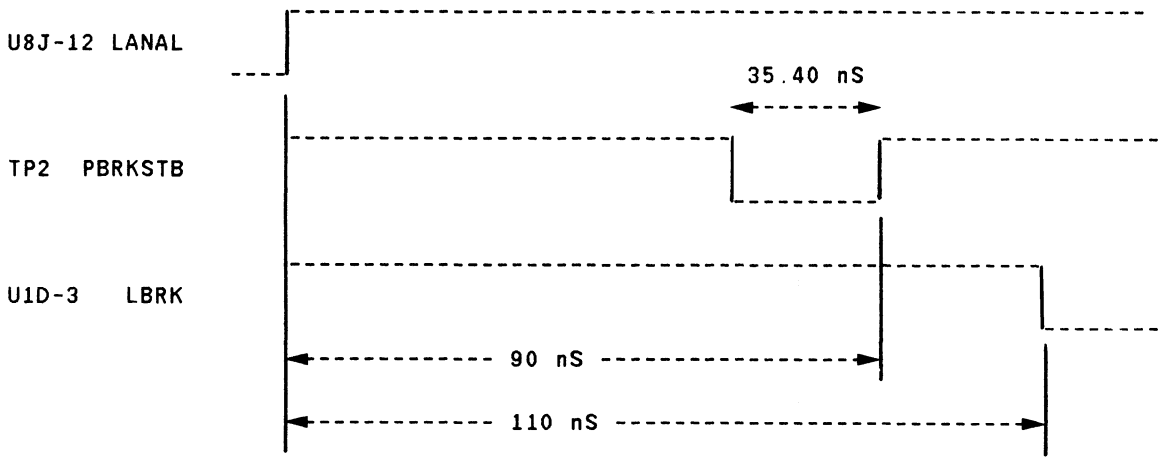
TROUBLESHOOTING.

Analysis Control Test Troubleshooting Guide:

Diagnostic Failure	KEY Node	IC Signal Path	SA Table
100	U1D-3	Pulsing probe	U1D, U16I
010	U1D-1	Pulsing probe	U1D, U16I
001	TP2	See PBRKSTB Timing procedure below.	

a. Trigger the oscilloscope on the rising edge of U8J-12 (LANAL).

b. Measure the following typical timing relationships between LANAL, TP2 (PBRKSTB) and U1D-3 (LBRK)



c. If the above timing relationships are not occurring note that the following nodes are pulsing (follow the node order given):

U8J-12, 13, U9J-4 ECL, U9H-2 ECL, U11H-15 ECL, U9H-14 ECL,

U11J-13 (TP2), U15E-6, U1D-3

Table 4-7. Troubleshooting Analysis Test Diagnostic Failures (Cont'd)

NOTE: The data on the Emulation Bus changes with the Emulator Controller being used. Therefore, accurate SA signatures on the outputs of the Emulation Bus Latches, of the EBPP, are not available. Use the following troubleshooting guides instead.

Address Field Test Troubleshooting Guide:

Diagnostic Failure	Troubleshooting Guide
100	Swap U5J with U6J. If the diagnostic failure followed U5J replace U5J. If the same diagnostic failure occurs troubleshoot the data and control paths to and from U5J.
010	Swap U6J with U5J. If the diagnostic failure followed U6J replace U6J. If the same diagnostic failure occurs troubleshoot the data and control paths to and from U6J.
001	Swap U7J with U6J. If the diagnostic failure followed U7J replace U7J. If the same diagnostic failure occurs troubleshoot the data and control paths to and from U7J.

Data Field Test Troubleshooting Guide:

Diagnostic Failure	Troubleshooting Guide
10	Swap U3J with U4J. If the diagnostic failure followed U3J replace U3J. If the same diagnostic failure occurs troubleshoot the data and control paths to and from U3J.
01	Swap U4J with U3J. If the diagnostic failure followed U4J replace U4J. If the same diagnostic failure occurs troubleshoot the data and control paths to and from U4J.

Status Field Test Troubleshooting Guide:

Diagnostic Failure	Troubleshooting Guide
1	Swap U1H with U4J. If the diagnostic failure followed U1H replace U1H. If the same diagnostic failure occurs troubleshoot the data and control paths to and from U1H.

4-12. TROUBLESHOOTING USING SIGNATURE ANALYSIS (SA).

The 64304A has been designed to use signature anlysis for troubleshooting to component level. Signature analysis is a technique that enables the signature analyzer to display a compressed, four digit "fingerprint" or signature of the data stream at a given node. Any fault associated with a device on that node will force a change in the data stream and, therefore, result in an erroneous signature.

The troubleshooting consists of connecting the signature analyzer and tracing signatures back through gates and memory elements until a part with correct inputs and faulty outputs is isolated. Signatures are determined good or bad by comparison to the good signatures given in this section.

KEY SIGNATURES (+).

While using SA on the 64304A some of the loops may contain key signatures. The use of the key signatures will reduce troubleshooting time considerably. A key signature is indicated with a "+" next to the node on the SA table. The key signatures should be checked before doing all of a given loop. If all of the key signatures are good then the rest of the signatures in that loop are good.

SIGNATURE KEY.

VH = Setup verification signature taken on +5 volts.

high = A VH signature without a blinking probe.

low = A constant low signal without a blinking probe.

ECL = When this label is next to a signature "DATA THRESHOLD" of the signature analyzer must be set to "ECL". All others are TTL.

TOTLZ= When a totalize signature is given in an SA loop it indicates that the "TOTLZ" key on the signature analyzer should be pressed and the node sampled again.

Pulsing=While the signature for this node may not be valid, logic activity can be detected by observing if the logic probe light is pulsing.

NOTE

The VH signature WILL NOT be valid until the PV test is executing.

Table 4-8. Signature Analysis Loop A

TEST: Break Control Test of the EBPP PV Module.

SA SETUP:

NORM MODE

CLOCK - negative edge, TTL, located on TP1 of EBPP.

START - positive edge, TTL, located on TP2 of 64100A I/O board.
- located on TP5 of 64110A CPU I/O board.

STOP - negative edge, TTL, located on TP2 of 64100A I/O board.
- located on TP5 of 64110A CPU I/O board.

+ = key signature
VH = 007U

U 15E- 6	0073	U 17C-10	007U
U 15E- 7	000F	U 17C-13	0015
U 15J- 1	0015	U 17E- 7	0073
U 15J- 2	006A	U 17E- 9	0073
U 15J- 6	0000		
U 15J-10	005H	U 17G- 1	0000
		U 17G- 2	000F
U 16E- 6	000F	U 17G- 4	000F
U 16E-12	000F	U 17G- 6	000F
		U 17G-14	002P +
U 16J- 1	006A	U 17G-16	002P +
U 16J- 5	007C +	U 17G-18	002P +
U 16J-15	0073	U 17G-19	006A
U 16J-19	006A		
		U 17I- 1	low
U 17B- 1	007U	U 17I- 3	002P
U 17B- 2	0037	U 17I- 5	002P
U 17B- 3	0077	U 17I- 7	002P
U 17B- 4	0000	U 17I- 9	002A
U 17B- 5	0000	U 17I-12	006A
U 17B- 6	006A	U 17I-14	006A
U 17B- 7	005H	U 17I-16	006A
U 17B- 9	high	U 17I-18	006A
U 17B-10	high	U 17I-19	low
U 17B-11	high		
U 17B-12	high	U 17J- 3	006A
U 17B-13	high	U 17J- 4	high
U 17B-14	0077	U 17J- 5	high
U 17B-15	high	U 17J- 6	low
		U 17J- 8	0022

Table 4-9. Signature Analysis Loop B

TEST: Pattern Recognition Test of the EBPP PV Module.

SA SETUP:

NORM MODE

CLOCK - negative edge, TTL, located on TP1 of EBPP.

START - positive edge, TTL, located on TP2 of 64100A I/O board.
- located on TP5 of 64110A CPU I/O board.

STOP - negative edge, TTL, located on TP2 of 64100A I/O board.
- located on TP5 of 64110A CPU I/O board.

+ = key signature
VH = HHU6

U 2F- 6	4U2F	U 5F- 6	3A5F
U 2H- 9	1UP8	U 5H- 3	4C12
		U 5H- 5	6A7C
U 2J- 3	4C12	U 5H- 7	5CH1
U 2J- 5	6A7C	U 5H- 9	P320
U 2J- 7	5CH1	U 5H-12	P380
U 2J- 9	P320	U 5H-14	C91F
U 2J-12	P380	U 5H-16	UF02
U 2J-14	C91F	U 5H-18	F437
U 2J-16	UF02		
U 2J-18	F437	U 6F- 6	P456
U 3F- 6	288H	U 6H- 3	4C12
		U 6H- 5	6A7C
U 3H- 3	A3C5	U 6H- 7	5CH1
U 3H- 5	82HF	U 6H- 9	P320
U 3H- 7	C376	U 6H-12	P380
U 3H- 9	0C87	U 6H-14	C91F
U 3H-12	0C27	U 6H-16	UF02
U 3H-14	51CC	U 6H-18	F437
U 3H-16	14A5		
U 3H-18	2F90	U 7F- 6	C023
U 4F- 6	28A7	U 7H- 3	4C12
		U 7H- 5	6A7C
U 4H- 3	4C12	U 7H- 7	5CH1
U 4H- 5	6A7C	U 7H- 9	P320
U 4H- 7	5CH1	U 7H-12	P380
U 4H- 9	P320	U 7H-14	C91F
U 4H-12	P380	U 7H-16	UF02
U 4H-14	C91F	U 7H-18	F437
U 4H-16	UF02		
U 4H-18	F437	U 8J- 1	3551

Table 4-9. Signature Analysis Loop B (Cont'd)

TEST: Pattern Recognition Test of the EBPP PV Module.

U 9J- 1	low
U 9H-14	0000 ECL
U 9H-14	TOTLZ=0003
U 9J-12	389P ECL
U 9J-12	TOTLZ=0003
U 11H- 3	0000 ECL
U 11H- 3	TOTLZ=0003
U 11H- 7	0000 ECL
U 11H- 7	TOTLZ=0003
U 11J-13	HHU6
U 11J-13	TOTLZ=0003
U 15E- 6	1U55
U 15E- 7	F2A3
U 16I- 1	high
U 16I- 2	high
U 16I- 5	CFPH
U 16I- 6	high
U 16I- 9	high
U 16I-12	high
U 16I-15	high
U 16I-16	high
U 16I-19	P8A7
U 16J- 5	HHU6
U 16J- 7	692F
U 16J- 9	7143
U 16J-12	6259
U 16J-14	6392
U 16J-16	CH98
U 16J-18	P9PH
U 17A- 1	high
U 17A- 2	F437
U 17A- 5	HA63
U 17A- 6	C91F
U 17A- 9	F5P1
U 17A-12	P320
U 17A-15	5CH1
U 17A-16	6A7C
U 17A-19	4C12
U 17B- 1	AP26
U 17B- 2	7UAH
U 17B- 3	P568
U 17B- 4	HHU6
U 17B- 5	0000
U 17B- 6	9828
U 17B- 7	AFFC
U 17B- 9	96C8
U 17B-10	4733
U 17B-11	HHU6
U 17B-14	HHU6
U 17B-15	P568
U 17B-15	TOTLZ=0003
U 17G- 1	9828
U 17G-14	4979
U 17G-16	78P4
U 17G-18	F0HH
U 17G-19	9828
U 17I- 3	F0HH
U 17I- 5	78P4
U 17I- 7	4979
U 17I- 9	H0P4
U 17I-12	F2CU
U 17I-14	76PU
U 17I-16	9828
U 17I-18	H4PC

Table 4-10. Signature Analysis Loop C

TEST: Smart Interface Test #1 of the State Controller PV Module.

SA Setup C:

```
CLOCK - negative edge, TTL, located on U11J-12 of EBPP.

START - positive edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

STOP  - negative edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

+  = key signature
VH = 399F

U 11J- 2  Pulsing ECL         U 15J- 2  028A
U 11J- 3  Pulsing ECL         U 15J- 6  3C09
U 11J- 4  Pulsing             U 15J-10  3C09
U 11J- 4  TOTLZ=0002
U 11J- 5  Pulsing             U 16E- 6  1180
U 11J- 5  TOTLZ=0005          U 16E-12  1180
U 11J- 6  Pulsing ECL
U 11J- 7  Pulsing ECL         U 16G- 3  Pulsing  +
U 11J-10  Pulsing ECL         U 16G- 5  Pulsing  +
U 11J-11  Pulsing ECL         U 16G- 7  Pulsing  +
U 11J-12  Pulsing             U 16G- 9  FCU2  +
                              U 16G-12  FHUH  +
U 12J-16  1851                U 16G-14  HA50  +
U 12J-18  2FP9                U 16G-16  HCH3  +
                              U 16G-18  2FP9  +
U 13J- 1  4F07
U 13J- 2  80PA                U 16I- 1  3C09
U 13J- 3  3C16                U 16I- 2  low
U 13J- 7  FP67                U 16I- 5  low
U 13J- 9  4P92                U 16I- 6  F057
U 13J-10  827U                U 16I- 9  0018
U 13J-12  3983                U 16I-12  F565
U 13J-15  3C09                U 16I-15  F565
                              U 16I-16  F565
U 15E- 5  3C09                U 16I-19  F565
U 15E- 6  281F
U 15E- 7  1180                U 17E- 1  3C09
                              U 17E- 7  281F
U 15G- 3  Pulsing  +          U 17E- 9  281F
U 15G- 5  Pulsing  +          U 17E-15  3C09
U 15G- 7  F7PF  +
U 15G- 9  FCU2  +             U 17J- 3  399F
U 15G-12  FHUH  +             U 17J- 5  high
U 15G-14  HA50  +             U 17J- 6  0000
U 15G-16  HCH3  +             U 17J- 8  0295
U 15G-18  2FP9  +
```

Table 4-11. Signature Analysis Loop D

TEST: Smart Interface Test #1 of the State Controller PV Module.

SA Setup D:

```
CLOCK - negative edge, TTL, located on TP1 of EBPP.

START - positive edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

STOP  - negative edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

+  = key signature
VH = 99FA

U 10J- 4  A069                U 17E- 1  09A3
U 10J- 5  44C7                U 17E- 2  07FF
U 10J- 6  8APU                U 17E- 3  07FF
                              U 17E- 4  0000
U 11J- 2  Pulsing ECL         U 17E- 5  0000
U 11J- 3  Pulsing ECL         U 17E- 7  46A3  +
U 11J- 4  Pulsing             U 17E- 9  44C7  +
U 11J- 5  Pulsing             U 17E-11  160U
U 11J- 6  Pulsing ECL         U 17E-12  00U8
U 11J- 7  Pulsing ECL         U 17E-13  high
                              U 17E-14  0000
U 15E-10  0000                U 17E-15  09A3
U 15E-11  high
U 15E-12  99FA                U 17G- 1  FP74
U 15E-13  00U8                U 17G- 2  HU78
U 15E-14  00U8                U 17G- 4  HH6F
U 15E-15  8APU                U 17G- 6  HU78
                              U 17G- 8  low
U 16E- 6  HU78                U 17G-11  low
U 16E-12  HU78                U 17G-13  low
                              U 17G-15  low
U 16I- 1  99FA                U 17G-19  FP74
U 16I- 6  A069
U 16I- 9  07FF                U 17I- 1  low
U 16I-11  HC3C                U 17I- 7  1UC2
                              U 17I- 9  962H
U 17B- 1  0AP3                U 17I-19  low
U 17B- 2  F7H7
U 17B- 3  160U
U 17B- 4  0000
U 17B- 5  0000
U 17B- 6  FP74
U 17B- 7  09A3
U 17B- 9  high
U 17B-10  HC3C
U 17B-11  0AP3
U 17B-14  160U
U 17B-15  high
```

Table 4-12. Signature Analysis Loop E

TEST: Clock/Data Channel Test #2 of the State Controller PV Module.

SA Setup E:

```
CLOCK - negative edge, TTL, located on TP1 of EBPP.

START - positive edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

STOP  - negative edge, TTL, located on TP2 of 64100A I/O board.
      -                     located on TP5 of 64110A CPU I/O board.

+  = key signature
VH = 2C34

U  2D- 1  2H72  ECL          U  4H- 3  2C61
U  2D- 2  4U0H  ECL          U  4H- 5  2P39
U  2D- 3  0646  ECL          U  4H- 7  7CCH
U  2D- 4  6439  ECL          U  4H- 9  23U1
U  2D-12  F061  ECL          U  4H-12  A737
U  2D-13  8F03  ECL          U  4H-14  PC55
U  2D-14  A737  ECL          U  4H-16  2H72
U  2D-15  PC55  ECL          U  4H-18  4U0H

U  2J- 3  2C61               U  5H- 3  2C61
U  2J- 5  2P39               U  5H- 5  2P39
U  2J- 7  7CCH               U  5H- 7  7CCH
U  2J- 9  23U1               U  5H- 9  23U1
U  2J-12  A737               U  5H-12  A737
U  2J-14  PC55               U  5H-14  PC55
U  2J-16  2H72               U  5H-16  2H72
U  2J-18  4U0H               U  5H-18  4U0H

U  3D- 1  7CCH  ECL          U  6D- 1  7CCH  ECL
U  3D- 2  23U1  ECL          U  6D- 2  23U1  ECL
U  3D- 3  5089  ECL          U  6D- 3  5089  ECL
U  3D- 4  08F5  ECL          U  6D- 4  08F5  ECL
U  3D-12  050H  ECL          U  6D-12  050H  ECL
U  3D-13  0055  ECL          U  6D-13  0055  ECL
U  3D-14  2C61  ECL          U  6D-14  2C61  ECL
U  3D-15  2P39  ECL          U  6D-15  2P39  ECL

U  3H- 3  0055               U  6H- 3  2C61
U  3H- 5  050H               U  6H- 5  2P39
U  3H- 7  5089               U  6H- 7  7CCH
U  3H- 9  08F5               U  6H- 9  23U1
U  3H-12  8F03               U  6H-12  A737
U  3H-14  F061               U  6H-14  PC55
U  3H-16  0646               U  6H-16  2H72
U  3H-18  6439               U  6H-18  4U0H
```

Table 4-12. Signature Analysis Loop E (Cont'd)

TEST: Clock/Data Channel Test #2 of the State Controller PV Module.

U	7D- 1	49U0	ECL
U	7D- 2	2F8U	ECL
U	7D- 3	65F4	ECL
U	7D- 4	07CC	ECL
U	7D-12	A3P3	ECL
U	7D-13	PU81	ECL
U	7D-14	F4C5	ECL
U	7D-15	88H7	ECL
U	7H- 3	2C61	
U	7H- 5	2P39	
U	7H- 7	7CCH	
U	7H- 9	23U1	
U	7H-12	A737	
U	7H-14	PC55	
U	7H-16	2H72	
U	7H-18	4U0H	
U	8D- 1	183U	ECL
U	8D- 2	4073	ECL
U	8D- 3	330C	ECL
U	8D- 4	6C47	ECL
U	8D-12	668U	ECL
U	8D-13	63H7	ECL
U	8D-14	48P3	ECL
U	8D-15	4HCC	ECL
U	8F- 4	2F8U	
U	8F- 7	4PU0	
U	8F- 9	88H7	
U	8F-12	F4C5	
U	8H- 3	48C6	
U	8H- 6	high	
U	8J- 1	low	
U	9D- 1	512H	ECL
U	9D- 2	0961	ECL
U	9D- 3	7A19	ECL
U	9D- 4	2255	ECL
U	9D-12	2U9H	ECL
U	9D-13	2AF5	ECL
U	9D-14	01U1	ECL
U	9D-15	04A9	ECL
U	9F- 4	4073	
U	9F- 7	183U	
U	9F- 9	4HCC	
U	9F-12	48P3	

U	9H-12	0000	ECL
U	9H-12	TOTLZ=0021	ECL
U	9H-14	0000	ECL
U	9H-14	TOTLZ=0021	ECL
U	9H-15	2C34	ECL
U	9J-10	P816	
U	9J-10	TOTLZ=0021	
U	9J-12	F322	ECL
U	9J-12	TOTLZ=0021	ECL
U	10D- 1	07P2	ECL
U	10D- 2	659H	ECL
U	10D- 3	2FH6	ECL
U	10D- 4	4PA9	ECL
U	10D-12	PAU1	ECL
U	10D-13	A693	ECL
U	10D-14	8HA7	ECL
U	10D-15	F1F5	ECL
U	10F- 4	0961	
U	10F- 7	512H	
U	10F- 9	04A9	
U	10F-12	01U1	
U	10J- 3	low	
U	11D- 1	2H72	ECL
U	11D- 2	4U0H	ECL
U	11D- 3	0646	ECL
U	11D- 4	6439	ECL
U	11D-12	F061	ECL
U	11D-13	8F03	ECL
U	11D-14	A737	ECL
U	11D-15	PC55	ECL
U	11F- 4	659H	
U	11F- 7	07P2	
U	11F- 9	F1F5	
U	11F-12	8HA7	
U	11H- 3	0000	ECL
U	11H- 3	TOTLZ=0021	ECL
U	11H- 7	0000	ECL
U	11H- 7	TOTLZ=0021	ECL

Table 4-12. Signature Analysis Loop E (Cont'd)

TEST: Clock/Data Channel Test #2 of the State Controller PV Module.

U 12D- 1	7CCH	ECL
U 12D- 2	23U1	ECL
U 12D- 3	5089	ECL
U 12D- 4	08F5	ECL
U 12D-12	050H	ECL
U 12D-13	0055	ECL
U 12D-14	2C61	ECL
U 12D-15	2P39	ECL
U 13D- 1	2H72	ECL
U 13D- 2	4U0H	ECL
U 13D- 3	0646	ECL
U 13D- 4	6439	ECL
U 13D-12	F061	ECL
U 13D-13	8F03	ECL
U 13D-14	A737	ECL
U 13D-15	PC55	ECL
U 14D- 1	7CCH	ECL
U 14D- 2	23U1	ECL
U 14D- 3	5089	ECL
U 14D- 4	08F5	ECL
U 14D-12	050H	ECL
U 14D-13	0055	ECL
U 14D-14	2C61	ECL
U 14D-15	2P39	ECL
U 15D- 1	2H72	ECL
U 15D- 2	4U0H	ECL
U 15D- 3	0646	ECL
U 15D- 4	6439	ECL
U 15D-12	F061	ECL
U 15D-13	8F03	ECL
U 15D-14	A737	ECL
U 15D-15	PC55	ECL
U 15J- 2	159A	
U 15J- 6	high	
U 16I- 2	low	
U 16I- 5	low	
U 16I- 6	low	
U 16I- 9	low	
U 16I-12	48C6	
U 16I-15	2A90	
U 16I-16	high	
U 16I-19	high	

U 17A- 1	high	
U 17A- 2	4U0H	
U 17A- 5	2H72	
U 17A- 6	PC55	
U 17A- 9	A737	
U 17A-12	23U1	
U 17A-15	7CCH	
U 17A-16	2P39	
U 17A-19	2C61	
U 17B- 1	27CH	
U 17B- 2	6P52	
U 17B- 3	P816	
U 17B- 4	2C34	
U 17B- 5	0000	
U 17B- 6	159A	
U 17B- 7	C463	
U 17B- 9	P49U	
U 17B-10	AH70	
U 17B-11	high	
U 17B-14	high	
U 17B-15	P816	
U 17G- 3	159A	
U 17G- 5	159A	+
U 17G- 7	0A1U	+
U 17G- 9	8H97	+
U 17G-12	93HP	
U 17G-14	93HP	
U 17G-16	93HP	
U 17G-18	93HP	
U 17G-19	159A	
U 17I- 3	93HP	
U 17I- 5	93HP	
U 17I- 7	93HP	
U 17I- 9	93HP	
U 17I-12	8H97	
U 17I-14	34C1	
U 17I-16	159A	
U 17I-18	159A	

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

The 64304A Emulation Bus Preprocessor board has no adjustments.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

This section contains information needed to order replacement parts. Table 6-1 lists reference designators and abbreviations used throughout the manual. Table 6-2 lists all 64304A replaceable parts in reference designator order. Table 6-3 contains a list of manufacturers' five digit code numbers and their corresponding names and addresses.

6-2. REFERENCE DESIGNATORS AND ABBREVIATIONS.

Table 6-1 lists reference designators and abbreviations used in the parts list, schematics and throughout the manual. Both designators and abbreviations are presented in upper case letters and their descriptions are lower cased.

6-3. REPLACEABLE PARTS LIST.

Table 6-2 is a list of replaceable parts organized in alphanumeric order by their reference designations. Information given for each part consists of the following:

a. The Hewlett-Packard Part Number and a check digit (for HP Internal Use).

b. The total quantity in the instrument. The total quantity for each part is given only once - at the first appearance of the part number in the list.

c. A description of the part.

d. A five-digit code indicating the manufacturer.

e. The manufacturer's part number.

6-4. MANUFACTURERS' CODES.

Table 6-3 lists the manufacturers' codes arranged in the order they appear in the replaceable parts list. Included with each code is the name and address of the manufacturer.

6-5. ORDERING INFORMATION.

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/Service Office.

To order a part that is not listed in the replaceable parts table, include the instrument model number, repair number, a description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

6-6. DIRECT MAIL ORDER SYSTEM.

Within the USA, Hewlett-Packard can supply parts through the direct mail order system. Advantages of using the system are outlined below.

a. Direct ordering and shipment from the Hewlett-Packard Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoices).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	64304-66501	1	1	EMULATION BUS PREPROCESSOR	28480	64304-66501
C1	0180-1746	5	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C2	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C3	0160-5321	8	37	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C4	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C6	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C7	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C8	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C9	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C10	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C11	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C13	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C14	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C15	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C16	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C17	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C18	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C19	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C20	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C21	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C22	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C23	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C24	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C25	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C26	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C27	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C28	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C29	0140-0200	0	2	CAPACITOR-FXD 390PF +-5% 300VDC MICA	72136	DM15F391J0300WV1CR
C30	0140-0200	0		CAPACITOR-FXD 390PF +-5% 300VDC MICA	72136	DM15F391J0300WV1CR
C31	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C32	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C33	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C34	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C35	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C36	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C37	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C38	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C39	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C40	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C41	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C42	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
C43	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
H1	2200-0103	2	2	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	28480	2200-0103
H2	2200-0105	4	1	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H3	3050-0235	3	1	WASHER-FL MTLC NO. 4 .117-IN-ID	28480	3050-0235
H4	64304-85001	6	1	EXTRACTOR 64304A	28480	64304-85001
H5	64304-85002	7	1	EXTRACTOR-EBPP	28480	64304-85002
H6	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
J4	1251-4428	8	3	CONNECTOR 50-PIN M POST TYPE	28480	1251-4428
J5	1251-4428	8		CONNECTOR 50-PIN M POST TYPE	28480	1251-4428
J6	1251-4428	8		CONNECTOR 50-PIN M POST TYPE	28480	1251-4428
J7	1251-7005	3	1	CONNECTOR 50-PIN M POST TYPE	28480	1251-7005
MP1	64304-01201	2	1	CABLE CLAMP 3 WIDE	28480	64304-01201
MP2	1400-0017	0	1	CLAMP-CABLE .312-DIA .375-WD NYL	28480	1400-0017
R1	0757-0427	0	4	RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
R2	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
R3	0757-0283	6	6	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
R4	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
R5	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
R5	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
R6	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
R7	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R8	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R9	0757-0385	9	2	RESISTOR 22.1 1% .125W F TC=0+-100	19701	MF4C1/8-T0-22R1-F
R10	0757-0385	9		RESISTOR 22.1 1% .125W F TC=0+-100	19701	MF4C1/8-T0-22R1-F
R11	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
R13	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
R14	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
RP1	1810-0475	3	24	NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP2	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP3	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP4	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP9	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
RP10	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP11	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP12	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP13	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP14	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP15	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP16	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP17	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP18	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP19	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP20	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP21	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP22	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP23	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP24	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP25	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP26	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP27	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP28	1810-0475	3		NETWORK-RES 8-SIP22.0 OHM X 4	28480	1810-0475
RP29	1810-0277	3	2	NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222
RP30	1810-0280	8	7	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP31	1810-0277	3		NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222
RP32	1810-0273	9	1	NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
RP33	1810-0219	3	1	NETWORK-RES 8-SIP220.0 OHM X 4	01121	208B221
RP34	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP35	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP36	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP37	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP38	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP39	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
TP1	0360-0535	0	6	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP +5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP GND	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1D	1820-0682	5	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S03N
U1H	1820-1997	7	7	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U1J	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U2D	1820-1173	1	13	IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U2F	1816-1092	4	6	IC TTL LS 256-BIT STAT RAM 35-NS 3-S	28480	1816-1092
U2H	1820-1130	0	1	IC GATE TTL S NAND 13-INP	01295	SN74S133N
U2J	1820-2024	3	11	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U3D	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U3F	1816-1092	4		IC TTL LS 256-BIT STAT RAM 35-NS 3-S	28480	1816-1092
U3H	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U3J	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U4F	1816-1092	4		IC TTL LS 256-BIT STAT RAM 35-NS 3-S	28480	1816-1092
U4H	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U4J	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U5F	1816-1092	4		IC TTL LS 256-BIT STAT RAM 35-NS 3-S	28480	1816-1092
U5H	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U5J	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U6D	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U6F	1816-1092	4		IC TTL LS 256-BIT STAT RAM 35-NS 3-S	28480	1816-1092
U6H	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U6J	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U7D	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U7F	1816-1092	4		IC TTL LS 256-BIT STAT RAM 35-NS 3-S	28480	1816-1092
U7H	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U7J	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U8D	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U8F	1820-2654	5	4	IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F157PC
U8H	1820-2690	9	1	IC GATE TTL F OR QUAD 2-INP	07263	74F32PC
U8J	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U9D	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U9F	1820-2654	5		IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F157PC
U9H	1820-0817	8	1	IC FF ECL D-M/S DUAL	04713	MC10131P
U9J	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U10D	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U10F	1820-2654	5		IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F157PC
U10J	1820-2686	3	1	IC GATE TTL F AND QUAD 2-INP	07263	74F08PC
U11D	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U11F	1820-2654	5		IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F157PC
U11H	1820-0810	1	1	IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10116P
U11J	1820-1052	5	1	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
U12D	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U12J	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U13D	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U13J	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U14D	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U15D	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U15E	1820-2693	2	2	IC FF TTL F J-K BAR POS-EDGE-TRIG	07263	74F109PC
U15G	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U15I	1820-1730	6	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U15J	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U16E	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U16G	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U16I	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U16J	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U17A	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U17B	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U17C	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U17D	1820-0269	4	1	IC GATE TTL NAND QUAD 2-INP	01295	SN7403N
U17E	1820-2693	2		IC FF TTL F J-K BAR POS-EDGE-TRIG	07263	74F109PC
U17G	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U17I	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U17J	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
W3	64304-61602	3	1	CABLE EBPP (DATA)	28480	64304-61602
W4	64304-61603	4	2	CABLE DATA LONG	28480	64304-61603
W5	64304-61603	4		CABLE DATA LONG	28480	64304-61603
W6	64304-61601	2	1	CABLE EBPP (CLOCK)	28480	64304-61601
XU10J	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
XU11H	1200-0607	0	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607

See introduction to this section for ordering information

Table 6-3. Manufacturer's Codes

Mfr No.	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE	SC	06226

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

This section contains information for adapting this manual to ET19776 units with earlier serial prefix numbers.

7-2. MANUAL CHANGES.

This manual applies directly to the instrument having the same serial prefix shown on the manual title page. If the serial prefix of the instrument is not the same as the one on the title page, find your serial prefix in table 7-1 and make the changes to the manual that are listed for that serial prefix. When making changes listed in table 7-1, make the change with the highest number first. Example: if backdating changes 1, 2, and 3 are required for your serial prefix, do change 3 first, then change 2, and finally change 1. If the serial prefix of the instrument is not listed either on the title page or in table 7-1, refer to an enclosed MANUAL CHANGES sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA corrections.

Table 7-1. Serial No. vs Manual Change No.

Serial Prefix	Make Changes	Affects

This manual has no backdating information for the mainframe as of the publication date of this manual.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

This section contains reference information for servicing the 64304A Emulation Bus Preprocessor. Included is block and component level theory of operation, definitions of the mnemonics used throughout this manual, and schematics. Refer to Section IV for information on verifying proper operation of the 64304A.

Note, the terms 64304A, Preprocessor, and EBPP will be used throughout this manual in reference to the 64304A Emulation Bus Preprocessor. The term CPU will be used when refering to the 64000 Host Microprocessor.

8-2. SAFETY CONSIDERATIONS.

Read the Safety Summary at the front of this manual before servicing the 64304A. Before performing each procedure, review it for cautions and warnings. For example, when working around the power supply circuitry, caution should be taken to avoid potentially lethal voltages.

8-3. BLOCK DIAGRAM THEORY (see Figure 8-1).

Write Status Buffer. The CPU enables this buffer when it requires the lower byte of (low true) status information from the EBPP.

Write Data Buffer. The CPU uses this buffer to load control information into the Control Word Register, Emulator identification information to the Analyzer, and to load data into the Pattern RAM.

Write Address Latch. This latch captures the lower address byte on the host bus. This information is then used to address Pattern RAM or simulate Emulation Bus cycles to the Analyzer data channels during PV.

Preprocessor Write Decoder. Used by the CPU to control Preprocessor programming functions. These functions include break reset, Pattern RAM and Control Word Register loading, Emulator ID loading, break set, and a PV strobe.

Control Word Register. The CPU uses this latch to select the operating modes of the 64304A through the use of CW0-7: run/load, Status and Data field multiplexing, and break drive enable/disable.

Preprocessor Control Decoder. The Analyzer controls interfacing between the Preprocessor and the Analyzer. The Analyzer controls the operations of the Smart Interface, the Break Drive Latches, and reseting and clearing of the Preprocessor. The Analyzer can provide itself with the the ID of the Preprocessor, the lower byte of Preprocessor status, and identification of the Emulator the EBPP is attached to.

Timing and Break Strobe Generator. This circuitry generates a delayed clock signal for the Analyzer and for pattern breaks. This circuit can be driven by the Emulation Analysis Clock (LANAL) or the PV Strobe from the CPU. CW6 determines which signal drives this circuit.

Analysis Smart Interface. The Analyzer uses this circuitry to provide itself the identification and status of the Preprocessor, and identification information about the Emulator Controller that the EBPP is connected to. This allows the Analyzer to configure it's input channels for analysis of 8 or 16 bit processors.

RAM Load Buffers. The CPU uses these buffers to load Pattern RAM and for simulation of emulation bus cycles during PV. When LLOAD is asserted the RAM Load Buffers are enabled.

Emulation Status, Data, and Address Latches. Information on the Emulation Bus is captured by these latches on the leading edge of the Emulation Analysis Clock (LANAL). The Emulation Latches are enabled by a low on LRUN.

Status, Data, and Address Pattern RAM. The Pattern RAM is used for recognizing data, status, and address patterns during an Emulation Bus cycle. The pattern data is used for the single-step feature in 16 bit Emulators.

Pattern Found Gate and Write Upper Status Byte Buffer. Each of the six Pattern RAM will output a "1" to the Pattern Found Gate when the specified (by the user) data pattern was found. The output level of the Pattern Found Gate is then clocked into the Pattern Break Drive Latch. The CPU can read Pattern RAM data, determine if a Stimulus Break occurred, or if the upper or lower byte of emulation data is being output to the Analyzer by reading the Write Upper Status Byte Buffer.

Break Drive Latches. This circuitry is used to drive the emulation break line (LBRK) on signals from the Analyzer or pattern detection circuitry.

Data/Status Multiplexors. When the EBPP is connected to a 16 bit Processor Emulator the upper byte of Emulation Bus Data will be sampled by the Analyzer. With an 8 bit Emulator the Emulation Bus Status lines will be sampled by the Analyzer.

Upper/Lower Byte Data Multiplexors. This circuitry is used to arrange the Emulation Bus Data into State Analyzer format for 8 and 16 bit Processor Emulators.

Status, Data, and Address Translators. Used to translate TTL Emulation Bus information into ECL logic levels required for the inputs to the State Analyzer.

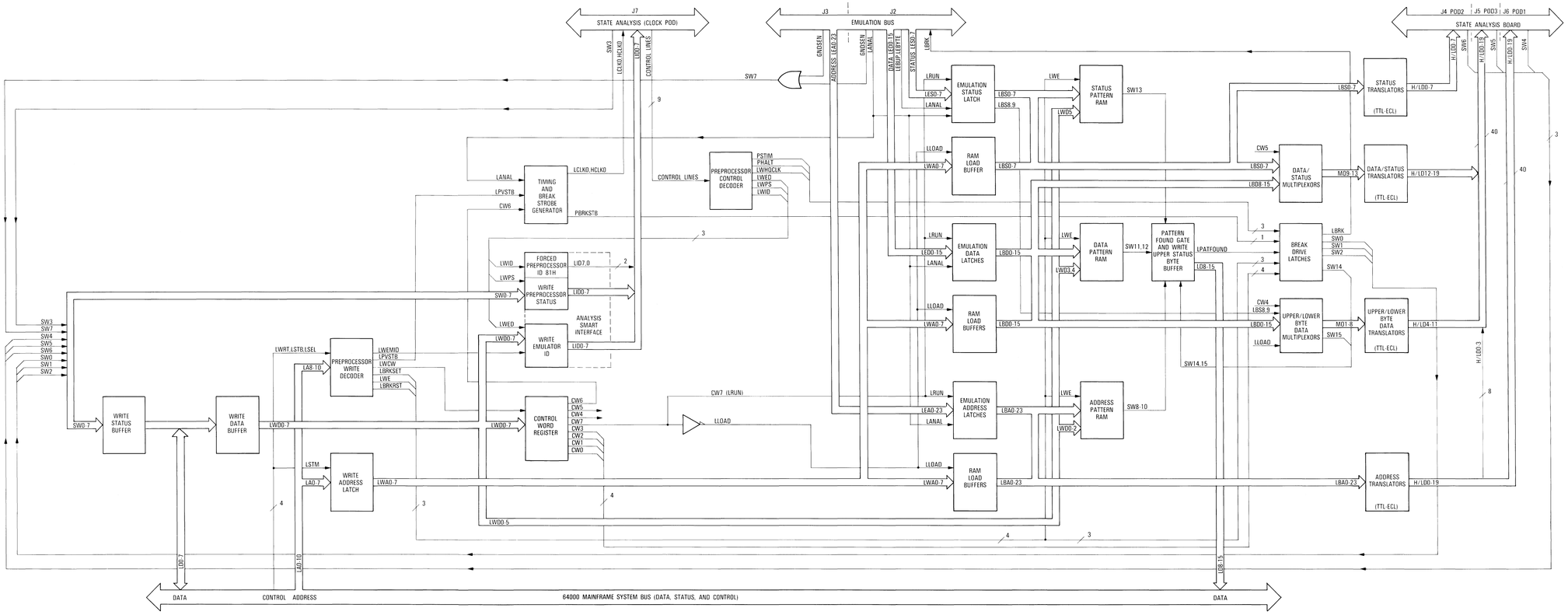


Figure 8-1.
Emulation Bus Preprocessor Block Diagram

NOTES

8-4. THEORY OF OPERATION (see Figure 8-3).

Emulation software controls the Preprocessor by writing to the Control Word Register (U16I), and also loads the ID of the Processor Emulator into the Write Emulator ID Register (U51G). In the RUN mode, Emulation Bus cycles of Address, Data, and Status are latched onto the Preprocessor Bus by the Emulation Bus Latches (U1J, and U3J-U7J) on the rising edge of LANAL. Also latched are the signals LEBYTE and LEBUP by U1H.

The Analyzer reads the Preprocessor ID (via U2J) and then the Processor Emulator ID (U15G) in order to properly format itself for a particular Emulator. The host CPU reads the Preprocessor Board ID to determine which card option is in which card cage slot. This infomation is used by other options and to load the correct Performance Verification software for Option Test.

The Data/Status Multiplexors (U11F and U10F) format the Emulation Bus Data and Status fields to either the 8 or 16 bit Analyzer format according to the configuration of the Control Word Register. LEBYTE and LEBUP are then used to select the proper byte of Emulation Bus Data being multiplexed by the Upper/Lower Byte Data Multiplexors (U8F and U9F) in either the 8 or 16 bit format. Buffered Emulation Bus Address, Data, and Status bits are then shifted from TTL to ECL logic levels and are sent out on the Preprocessor Interface Bus (PPIB) to the State Analyzer.

The Preprocessor Bus (LBA0-23, LBD0-15, and LBS0-7) also goes to six 256x1 Pattern RAM (U2F-U7F) which are used for Emulation Bus cycle pattern recognition for 16 bit emulator single-stepping. The Emulation software writes either a logical "0" or "1" to each address in each of the Pattern RAM (using the RAM Load Buffers (U2J, U3H-U7H), Write Address Latch (U17A), and Write Data Buffer (U17I)). Each Pattern RAM corresponds to a byte of data on the Emulation Bus which will be routed to that RAM. When each RAM is addressed by that particular byte of Emulation Bus information, the information stored in the addressed cell is inverted at the output of the RAM indicating the addressing pattern is true or false. All of the RAM outputs are then gated together (U2H) to form one "Pattern True" signal which is clocked into the Pattern Break Drive Latch (U15E) by PBRKSTB. The break signal (LBRK) is then gated onto the Emulation Bus, and will be cleared immediately after the emulator detects it. Pattern break is enabled by the emulation software only during single-step mode.

LANAL is also used to trigger the Timing and Break Strobe Generator, which consists of two discrete ECL monostable circuits (U9H and U11H), to generate a clock for the Analyzer with enough delay to allow for any on-board processing of the Emulation Bus data (Analyzer data formatting or Pattern Recognition). The PBRKSTB signal is a TTL output of the Timing and Break Strobe Generator with the ECL output being used to clock the Analyzer.

8-4. THEORY OF OPERATION (Cont'd).

The Preprocessor may also drive the Emulation Break line (LBRK) using signals on the Stimulus and Halt Lines (PSTIM and PHALT) from the State Analyzer. The Stimulus Line signal is a pulse generated when the Analyzer recognizes a trigger or a data sequence. This pulse is used as the clock to latch a Stimulus Break (U17E). The Halt Line signal is a low to high transition generated by an analysis trigger or measurement completion and must be first qualified in order to recognize the correct transition. If the Halt Line is to be driven by the Analyzer during a measurement it will be at a logical "1" after the State Analyzer hardware has been configured. The LWHQCLK signal, which is generated by the Analyzer just before a measurment starts but just after the State Analyzer hardware is configured, is used to latch (U15E) the Halt qualifying level. The Halt break is then clocked into U17E by the next positive transition on the Halt Line where it is gated onto the Emulation Bus. When the Halt break is driven, the qualifier latch (U15E) is immediately reset to await proper re-qualification. Emulation software enables or disables either of these breaks according to user input during configuration, and again will reset a break immediately after it is detected.

The Pod Sense logic (U8J, R13, R14, RP29, R1, R2, R5 and R11) is used during PV to determine what Analyzer Pods and Emulation Bus cables are connected to the Preprocessor.

8-5. LOGIC CONVENTION.

Logic states are defined as follows:

```
0--------------False, negated, inactive, or unasserted state.

1--------------True, active, or asserted state.
```

Voltage levels representing logic states:

```
LOW (L)--------The more negative of two voltage levels.

HIGH (H)-------The more positive of two voltage levels.
```

Signals may be either HIGH true, or LOW true, as indicated by the mnemonics on the schematics.

The 64304A includes both TTL and ECL ICs. Worst case voltage levels for troubleshooting and signature analysis purpose are as follows: (IC data sheet specifications may be more accurate)

TTL Voltage Levels

Level	Voltage
LOW	less than 0.8 V
HIGH	greater than 2.0 V

ECL Voltage Levels

Level	Voltage
LOW	less than -1.50
HIGH	greater than -1.10

8-6. ECL ATTRIBUTES.

Because ECL inputs are pulled down inside the IC, an unconnected ECL input is LOW.

ECL outputs may be tied together in the same way as open-collector TTL outputs. Thus, they may be wire-ANDed or wire-ORed.

Table 8-1. Logic Symbols, sheet 1 of 3

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

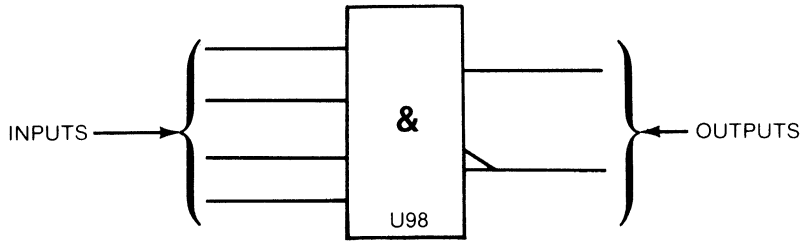
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

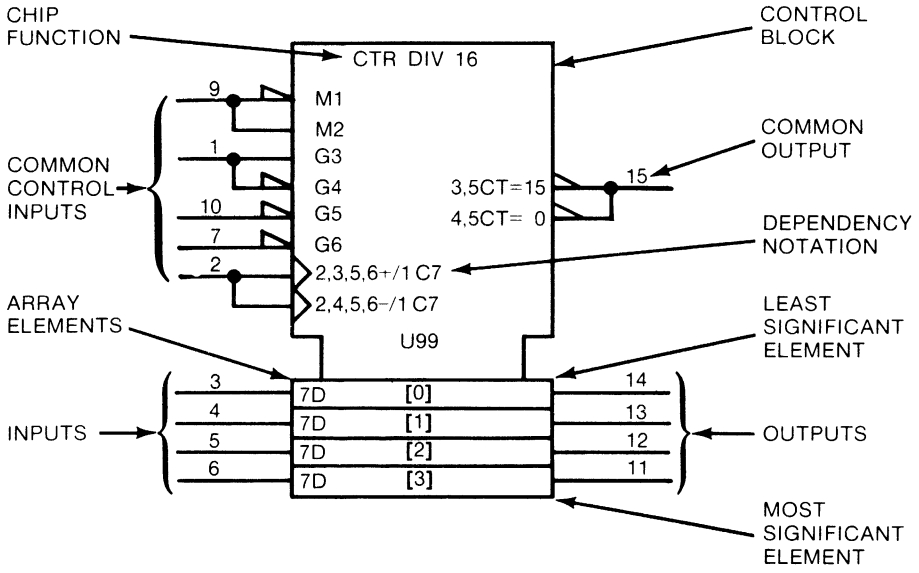
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

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Table 8-1. Logic Symbols, sheet 2 of 3

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (complements state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-1. Logic Symbols, sheet 3 of 3

OTHER SYMBOLS

⌒	Analog Signal	◺◿	Inversion	→	Shift Right (or down)
&	AND	O	Negation	/	Solidus (allows an input or output to have more than one function)
} {	Bit Grouping	—✕—	Nonlogic Input/Output	▽	Three State
▷	Buffer	◇	Open Circuit (external resistor)	,	Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
!	Compare	◇	Open Circuit (external resistor)	( )	Used for factoring terms using algebraic techniques.
▷	Dynamic	≥1	OR	[ ]	Information not defined.
=1	Exclusive OR	⊽	Passive Pull Down (internal resistor)	Φ	Logic symbol not defined due to complexity.
⊓	Hysteresis	⊼	Passive Pull Up (internal resistor)		
?	Interrogation	⊓	Postponed		
—	Internal Connection	←	Shift Left (or up)		

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	–	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

⎍⎍	Astable	NV	Nonvolatile
100 ns	Delay	I	State of initial power up
1⎍	Nonretriggerable Monostable	⎍	Retriggerable Monostable

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Table 8-2. Schematic Diagram Notes

ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

TP1 ELECTRICAL TEST POINT TP (WITH NUMBER)

NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.

LETTERED TEST POINT NO MEASUREMENT AID PROVIDED

COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

1 3 NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION.
LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

A CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

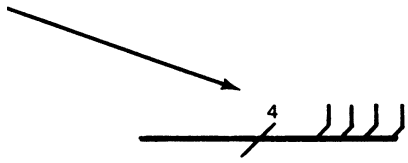
* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS



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8-7. MNEMONICS (see Table 8-3).

Signals on the 64304A board have been assigned mnemonics in alphabetical order that describes the active state and function of the signal (see table 8-1 Logic Symbols). A prefix letter (H, or L) is used to indicate the active state of the signal and the remaining letters indicate its function. An "H" prefix indicates that the function is active in the "high" state; an "L" prefix indicates that the function is active in the "low" state. Table 8-3 is a listing of the mnemonics used on the schematics and throughout this manual.

Table 8-3. Mnemonics

Mnemonic	Description
CW0-7	CONTROL WORD 0-7. The host processor uses these bits to control various operations of the EBPP. These 8 bits control the following functions: NOTE: these lines are represented with low true logic!!

```
CW0   GLOBAL BREAK ENABLE--must be enabled to allow any breaks
           0 = enable break
           1 = disabled
CW1   PATTERN BREAK (for 'step')
           0 = enable pattern break
           1 = disabled
CW2   BREAK ON ANALYSIS HALT (for 'break on analysis_halt')
           0 = enable analysis halt break
           1 = disabled
CW3   BREAK ON ANALYSIS STIMULUS (for 'break on analysis_stimulus')
           0 = enable analysis stimulus break
           1 = disable
CW4   FORMAT FOR DEMUXULTIPLEXING DATA
           0 = pod 2 bits H/LD4-11 always emulation data bits 0-7
               (16 bit format)
           1 = pod 2 bits H/LD4-11 multiplexed by byte status
               (8 bit format)
CW5   FORMAT FOR 8 BIT/16 BIT STATUS
           0 = pod 2 bits H/LD12-19 are emulation data bits 8-15
               (16 bit format)
           1 = pod 2 bits H/LD12-19 are emulation status
               (8 bit format)
CW6   CLOCK SOURCE
           0 = clock driven by PV strobe (load mode)
           1 = clock driven by emulation analysis clock (run mode)
CW7   DATA SOURCE
           0 = load address (load mode)
           1 = emulation data (run mode)
```

Table 8-3. Mnemonics (Cont'd)

Mnemonic	Description
GNDSEN	GROUND SENSE. These lines are tied to circuit ground on the General Purpose or Emulation Control cards; used to determine if the Emulation bus cables are connected to the EBPP.
HCLK0	HIGH CLOCK 0. Differential (LCLK0) clock signals or qualifier bits to the State Analyzer Control board.
HD0-19	HIGH DATA 0-19. Differential data signals (LD0-19) sent to the State Analyzer Aquisition cards for analysis.
HSTB	LOW STROBE. A signal originating in the mainframe. When low and the CPU is in the write mode (LWRT low), LSTB indicates the Data Bus has valid information on it. When low and the CPU is in the read mode, LSTB indicates that the CPU is not driving the Data Bus, and the device addressed may now drive it.
HSTM	HIGH START MEMORY. When high, clocks the valid information on the mainframe address bus into the Write Address Latch.
HTCLK	HIGH TRANSFER CLOCK. A differential clock (LTCLK) from the State Analyzer Control board. When HTCLK goes from a low to a high state, data is transferred to/from the State Analyzer and the Preprocessor.
LA0-10	LOW ADDRESS 0-10. Used by the CPU to address various devices on the EBPP. The Address Bus is transmit only from the CPU.
LANAL	LOW ANALYSIS. A rising edge on this line clocks data present on the emulation address, data, and status buses into the Emulation Bus Latches.
LBA0-23	LOW BUFFERED ADDRESS 0-23. Same as LEA0-23 with additional buffering.
LBD0-15	LOW BUFFERED DATA 0-15. Same as LED0-15 with additional buffering.
LBRK	LOW BREAK. When low indicates to the General Purpose or Emulator Control board to do a hardware break. This causes the emulator to stop processing and allow the user to analyze the cause of the break condition. This line may be asserted when the analyzer completes a requested trace.

Table 8-3. Mnemonics (Cont'd)

Mnemonic	Description
LBRKRST	LOW BREAK RESET. When this line or LRESET are low the Break Drive Latches are reset.
LBRKSET	LOW BREAK SET. When this line is low the Break Drive Latches are set.
LBS0-9	LOW BUFFERED STATUS 0-9. Same as LES0-7, LEBUP, and LEBYTE with additional buffering.
LCLK0	LOW CLOCK 0. Differential (HCLK0) clock signals or qualifier bits to the State Analyzer Control board.
LD0-12	LOW DATA 0-12. The bidirectional bus used to transfer data to and from the CPU. When LSTB is low, the data on the bus is valid. Data bits 9-12 are used to generate the Preprocessor board ID number (1A00H).
LD0-19	LOW DATA 0-19. Differential data signals (HD0-19) sent to the State Analyzer Aquisition cards for analysis.
LEA0-23	LOW EMULATION ADDRESS 0-23. These lines are the address outputs of the General Purpose or Emulator Control boards. These lines specify an active low address for memory or input/output location.
LEBUP	LOW EMULATION BYTE UPPER. This line is output to the Emulation Bus. When low, indicates that a byte of data data will be transferred on the upper 8 bits of the Emulation Data Bus. This signal becomes LBS9.
LEBYTE	LOW EMULATION BYTE. This line is output to the Emulation Bus. When low, indicates that all data transactions on the bus are byte instead of word transactions. This signal becomes LBS8.
LED0-15	LOW EMULATION DATA 0-15. This is a bidirectional, 16 bit bus. The analyzer uses this active low bus to trace both emulation memory transactions, and user memory and I/O transactions.
LES0-7	LOW EMULATION STATUS 0-7. These lines are output from various circuits on the General Purpose or Emulation Control boards to the Emulation Bus.
LIA0 & 1	LOW INTERFACE ADDRESS 0 and 1. Signals used for writing an address to the Preprocessor Control Decoder to control various operations.

Table 8-3. Mnemonics (Cont'd)

Mnemonic	Description
LID0-7	LOW INTERFACE DATA 0-7. A data bus that the State Analyzer Control board uses read data from the CPU, and status and preprocessor ID information from the 64304A.
LIMRST	LOW INTERFACE MASTER RESET. A low on this line will reset the Preprocessor.
LIWRT	LOW INTERFACE WRITE. The State analyzer Control board uses this line to address the Preprocessor Control Decoder.
LLOAD	LOW LOAD. When low, this signal enables the RAM Load buffers and allows the CPU to drive the address, data, and status buses. When high, the information stored in the Emulation Latches is allowed to drive the address, data, and status buses.
LPATFOUND	LOW PATTERN FOUND. A low on this line indicates that the Emulation Bus pattern was found.
LPVSTB	LOW PERFORMANCE VERIFICATION STROBE. The CPU uses this line to stimulate the second stage of the Timing and Break Strobe Generator during performance verification tests.
LPOP	LOW POWER ON PULSE. Normally high signal that will go low when the power supply shuts off. LPOP will pulse low shortly after the power supply turns on.
LREAD	LOW READ. When asserted by the CPU this signal enables the CPU to read the Upper Status Byte Buffer.
LRESET	LOW RESET. When this line is low the Preprocessor is disabled. When this line is high the CPU and the State Analyzer can control operations on the EBPP. A reset is asserted by a master reset (LIMRST) from the analyzer or a LPOP from the power supply.
LSEL	LOW SELECT. A signal originating in the mainframe. When low, LSEL allows the Preprocessor board Identification Code (ID # 1A00H) to be returned over the CPU's Data Bus. This allows the CPU to determine the Preprocessor installed in the mainframe, and which card cage slot it is installed in. This line is also used to enable the EBPP.

Table 8-3. Mnemonics (Cont'd)

Mnemonic	Description
LSTB	LOW STROBE. A signal originating in the mainframe. When low and the CPU is in the write mode (LWRT low), LSTB indictes the Data Bus has valid information on it. When low and in the read mode, LSTB indicates that the CPU is not driving the Data Bus, and the device addressed may now drive it.
LSTM	LOW START MEMORY. A signal originating in the mainframe. When low, LSTM indicates that the information on the CPU's Address Bus is valid.
LTCLK	LOW TRANSFER CLOCK. A differential clock (HTCLK) from the State Analyzer Control board. When LTCLK goes from a high to a low state, data is transferred to/from the State Analyzer and the Preprocessor.
LWA0-7	LOW WRITE ADDRESS 0-7. Low true address lines the CPU uses to address and control devices on the EBPP.
LWE	LOW WRITE ENABLE. When low, the CPU is writing to the Pattern RAM. When high, the CPU is reading from the Pattern RAM.
LWCW	LOW WRITE CONTROL WORD. The CPU uses this line to clock control information into the Control Word Register of the Preprocessor. See CW0-7 for more information.
LWD0-7	LOW WRITE DATA 0-7. These lines are the CPU Data Bus after buffering. Data bits LWD0-5 are also used as the data for the Pattern RAM.
LWHQCLK	LOW WRITE HALT QUALIFY CLOCK. The analyzer uses this line to clock in the level on the PHALT line. This line will be clocked prior to an analyzer trace.
LWID	LOW WRITE IDENTIFICATION. The State Analyzer Control board selects this line when the Emulation Bus Preprocessor ID (81H) is required. Also, used during PV.
LWED	LOW WRITE EMULATOR DATA. The State Analyzer Control board selects this line when it requires data. The data is emulator information sent from the CPU.
LWEMID	LOW WRITE EMULATOR IDENTIFICATION. This line clocks the identification information of the Microprocessor Emulator that is attached to the General Purpose or Emulation Control board. The analyzer can then configure it's data channels accordingly.

Table 8-3. Mnemonics (Cont'd)

Mnemonic	Description
LWPS	LOW WRITE PREPROCESSOR STATUS. The State Analyzer Control board selects this line when the status of the Preprocessor is required.
MO1-8	MULTIPLEXOR OUTPUTS 1-8. These lines are the outputs of the Upper/Lower Data Byte Multiplexors that become bits H/LD4-11 of Pod 2. Used for routing data information for analysis of 16 or 8 bit Emulators.
MO9-16	MULTIPLEXOR OUTPUTS 9-16. These lines are the outputs of the Data/Status Multiplexors that become bits H/LD12-19 of Pod 2. Used for routing data or status information for analysis of 16 or 8 bit Emulators.
NIHALT	NEGATIVE INTERFACE HALT. A differential signal (PIHALT) sent to the Preprocessor, from the analyzer, to qualify or disable a halt break (see PHALT).
NISTIM	NEGATIVE INTERFACE STIMULUS. A differential signal (PISTIM) sent to the Preprocessor, from the analyzer. NISTIM goes from a high to a low state when a Trigger Event or Sequence Event occurs if enabled by the user (see PSTIM).
PBRKSTB	POSITIVE BREAK STROBE. Clock signal from the Timing and Break Strobe Generator used to clock in the information on the output of the Pattern Found Gate.
PHALT	POSITIVE HALT. When high, indicates that a Halt Break has been qualified. When low, Halt Breaks are disabled.
PIHALT	POSITIVE INTERFACE HALT. A differential signal (NIHALT) sent to the Preprocessor, from the analyzer, to qualify or disable a halt break (see PHALT).
PISTIM	POSITIVE INTERFACE STIMULUS. A differential signal (NISTIM) sent to the Preprocessor, from the analyzer. PISTIM goes from a low to a high state when a Trigger Event or Sequence Event occurs if enabled by the user (see PSTIM).

Table 8-3. Mnemonics (Cont'd)

Mnemonic	Description
PSTIM	POSITIVE STIMULUS. The positive edge of PSTIM will clock the value of CW3 when a Trigger Event or Sequence Event occurs (see CW3).
SW0-15	STATUS WORD 0-15. The Preprocessor generates sixteen status bits that the Analyzer and the CPU can read. These lines show the status of the following functions: NOTE these lines are represented with low true logic !!

```
STATUS WORD BIT

        SW0      ANY BREAK
                      0 = A BREAK OCCURRED
                      1 = NO BREAK

        SW1      PATTERN BREAK
                      0 = PATTERN BREAK OCCURRED
                      1 = NO BREAK

        SW2      ANALYSIS BREAK (either HALT or STIMULUS)
                      0 = ANALYSIS BREAK OCCURRED
                      1 = NO BREAK

        SW3      CLOCK POD SENSE (used for PV)
                      0 = NO CLOCK POD
                      1 = CLOCK POD CABLE IS PRESENT

        SW4      DATA POD 1 SENSE (used for PV)
                      0 = NO POD 1
                      1 = POD 1 CABLE IS PRESENT

        SW5      DATA POD 3 SENSE (used for PV)
                      0 = NO POD 3
                      1 = POD 3 CABLE IS PRESENT

        SW6      DATA POD 2 SENSE (used for PV)
                      0 = NO POD 2
                      1 = POD 2 CABLE IS PRESENT

        SW7      EMULATION BUS SENSE (used for PV)
                      0 = EMULATION BUS IS CONNECTED
                      1 = NO EMULATION BUS CONNECTED
```

Table 8-3. Mnemonics (Cont'd)

Mnemonic	Description
SW0-15	STATUS WORD 0-15 (Con't)

```
SW8      LOW ADDRESS PATTERN
              0 = TRUE
              1 = FALSE

SW9      MID ADDRESS PATTERN
              0 = TRUE
              1 = FALSE

SW10     HIGH ADDRESS PATTERN
              0 = TRUE
              1 = FALSE

SW11     LOW DATA PATTERN
              0 = TRUE
              1 = FALSE

SW12     HIGH DATA PATTERN
              0 = TRUE
              1 = FALSE

SW13     STATUS PATTERN
              0 = TRUE
              1 = FALSE

SW14     STIMULUS BREAK
              0 = NO BREAK
              1 = STIMULUS BREAK OCCURRED

SW15     HIGH TO LOW MULTIPLEX
              0 = NORMAL
              1 = MULTIPLEXED
```

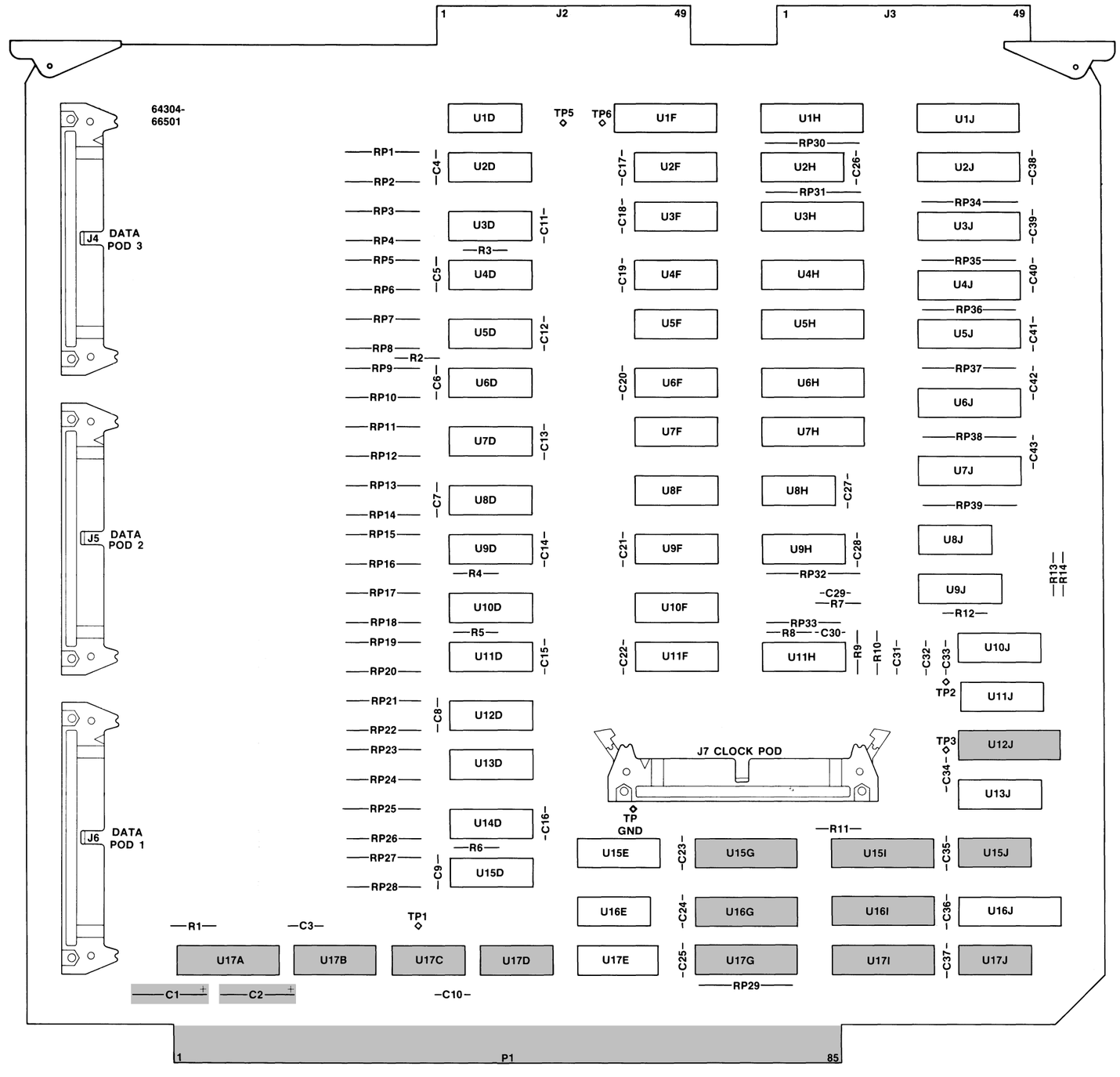
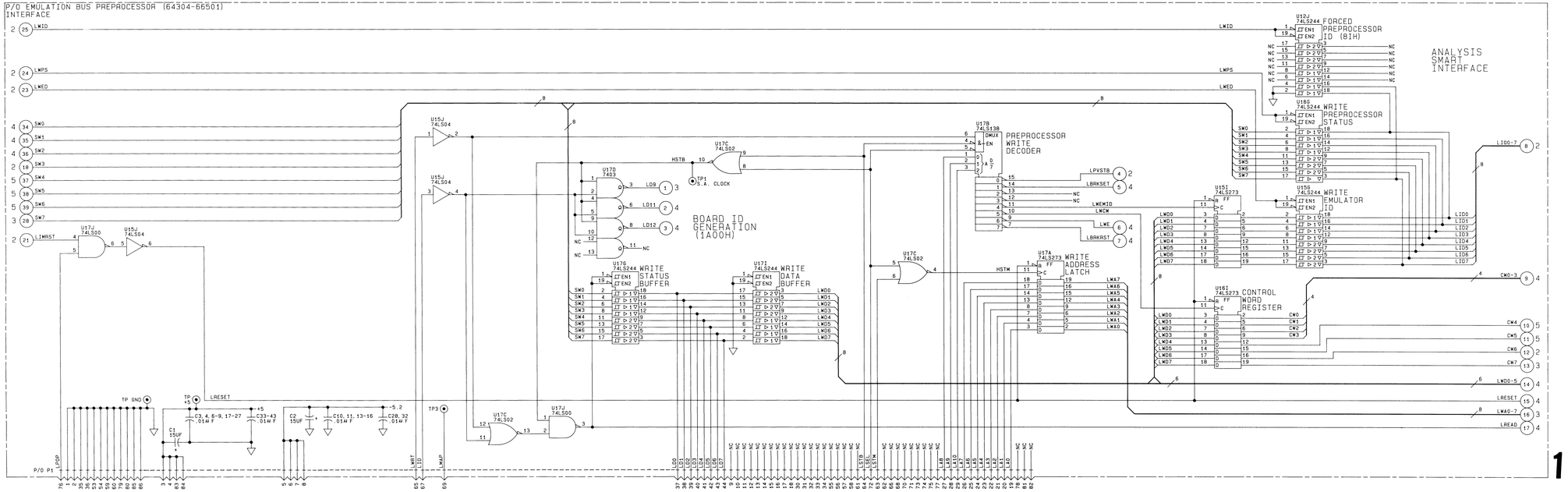


Figure 8-2. 64304A Component Locator (sheet 1 of 5)



1

IC's ON THIS SCHEMATIC

REF DES	HP PART NO.	MFG PART NO.	+5	GND	-5.2
U12J, U15G, U16G, U17G, U17I	1820-2024	SN74LS244N	20	10	
U15I, U16I, U17A	1820-1730	SN74LS273N	20	10	
U15J	1820-1199	SN74LS04N	14	7	
U17B	1820-1216	SN74LS138N	16	8	
U17C	1820-1144	SN74LS02N	14	7	
U17D	1820-0269	SN7403N	14	7	
U17J	1820-1197	SN74LS00N	14	7	

PARTS ON THIS SCHEMATIC

C1-4, 6-11, 13-28, 32
TP GND, TP +5, TP1, TP3

Figure 8-3.
64304A Schematic (sheet 1 of 5)

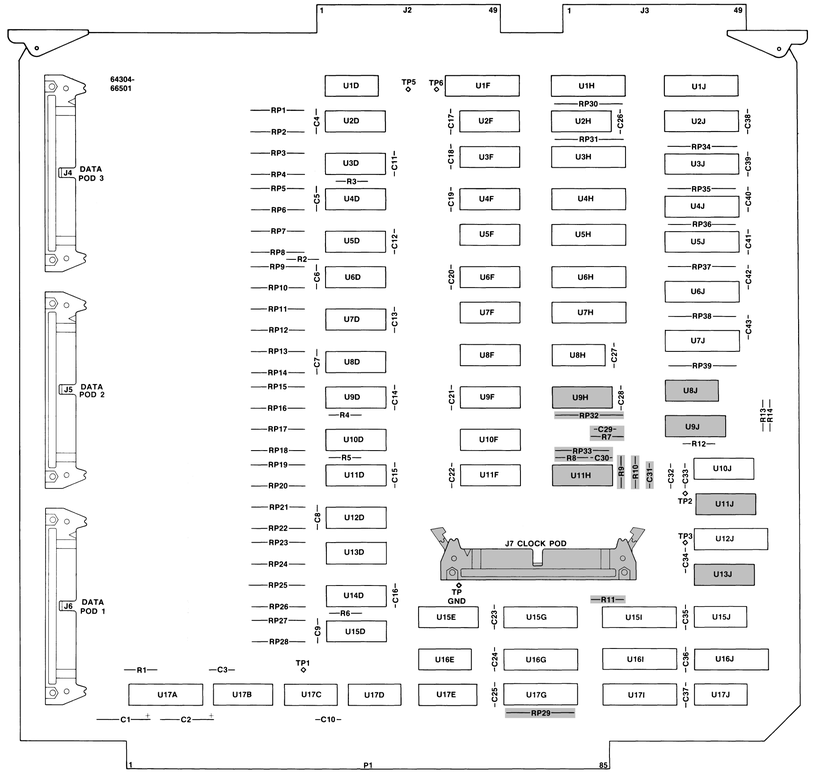
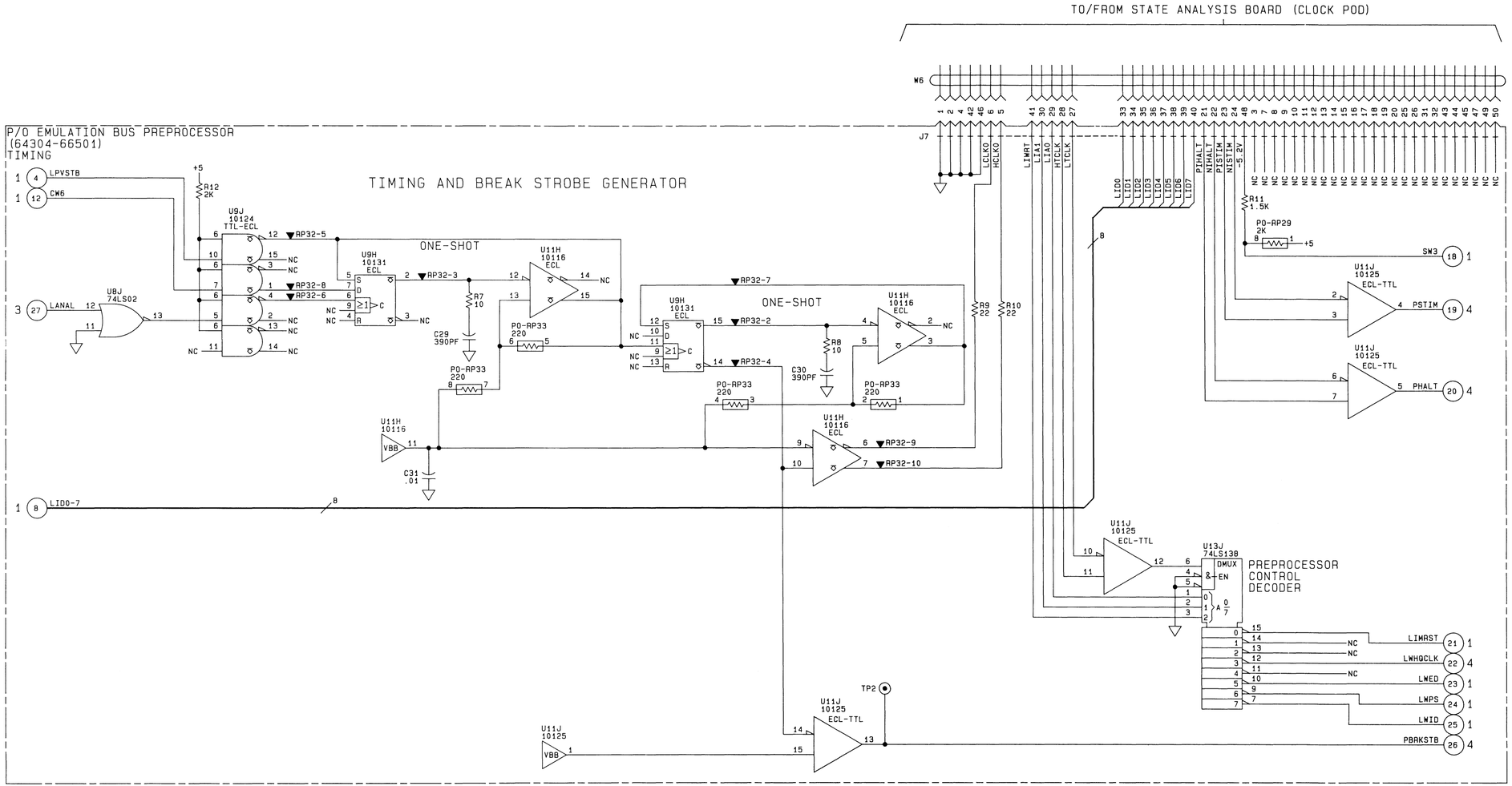


Figure 8-2. 64304A Component Locator (sheet 2 of 5)



IC's ON THIS SCHEMATIC

REF DES	HP PART NO.	MFG PART NO.	+5	GND	-5.2
U8J	1820-1144	SN74LS02N	14	7	
U9J	1820-1173	MC10124L	9	16	8
U9H	1820-0817	MC10131P		1,16	8
U11H	1820-0810	MC10116P		1,16	8
U11J	1820-1052	MC10125L	9	16	8
U13J	1820-1216	SN74LS138N	16	8	

PARTS ON THIS SCHEMATIC

C29-31
R7-12
RP29, 32, 33
TP2

RP VALUE TABLE

RP #	HP P/N	RESISTOR VALUE	POWER PIN AND VOLTAGE LEVEL	
32	1810-0273	470 X 9	1	-5.2

▼ CONNECTION SYMBOL

NOTE

▼ XX - XX

SEE RP VALUE TABLE FOR MORE INFORMATION

PIN NUMBER OF RESISTOR PACK

RESISTOR PACK NUMBER (RP#)

ECL LINE BEING PULLED DOWN

2

Figure 8-3.
64304A Schematic (sheet 2 of 5)

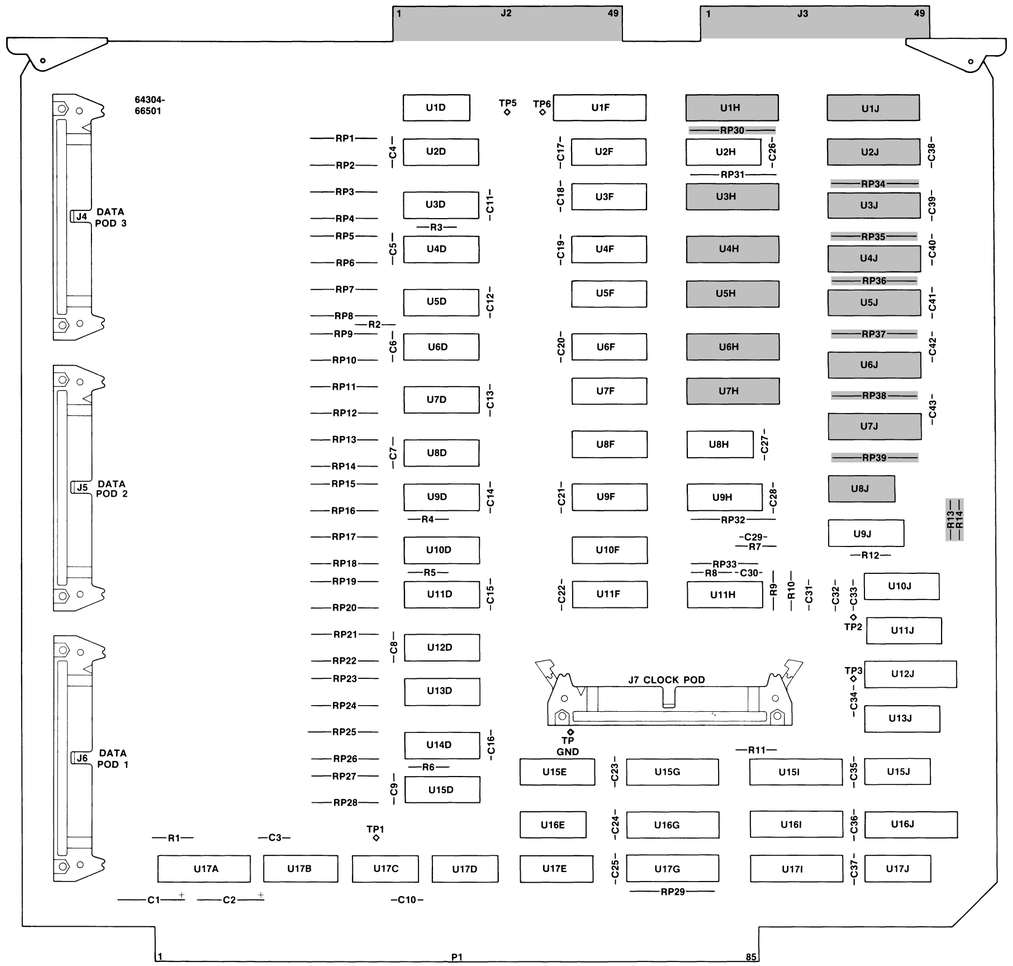
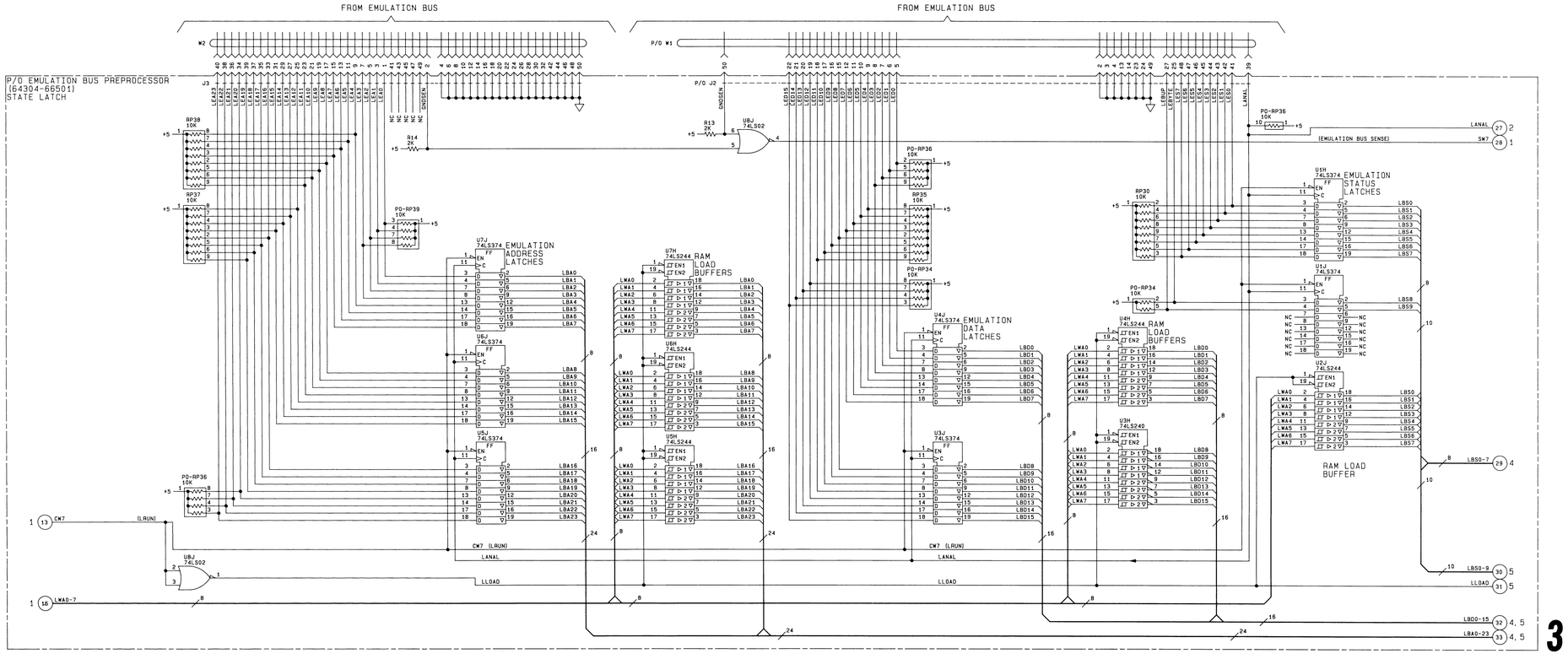


Figure 8-2. 64304A Component Locator (sheet 3 of 5)



3

IC's ON THIS SCHEMATIC

REF DES	HP PART NO.	MFG PART NO.	+5	GND	-5.2
U1H, U1J, U3J-U7J	1820-1997	SN74LS374N	20	10	
U2J, U4H-U7H	1820-2024	SN74LS244N	20	10	
U3H	1820-1917	SN74LS240N	20	10	
U8J	1820-1144	SN74LS02N	14	7	

PARTS ON THIS SCHEMATIC

R13, 14
RP30, 34-39

Figure 8-3.
64304A Schematic (sheet 3 of 5)

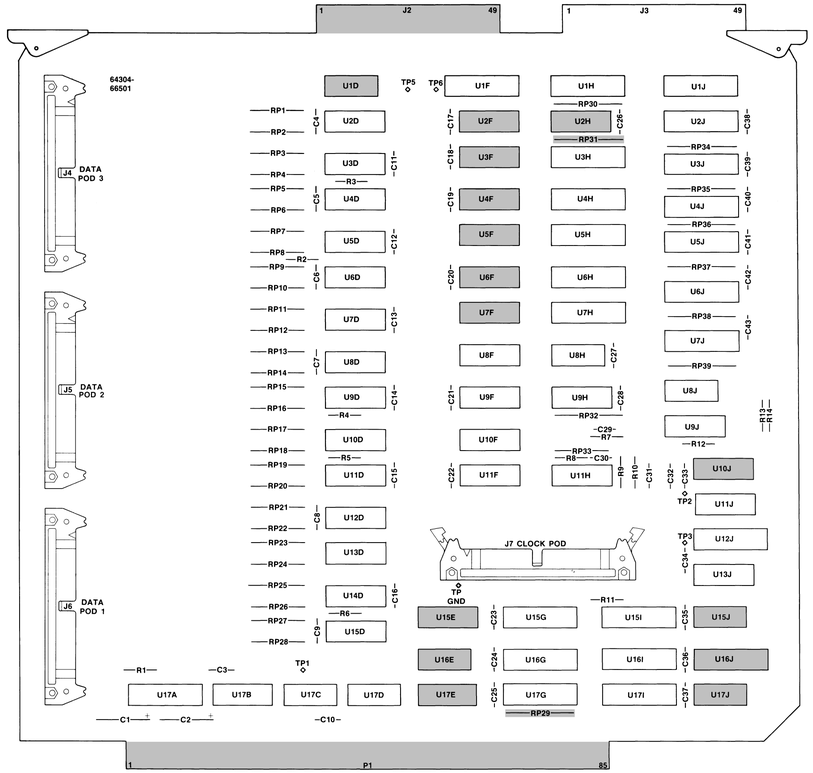
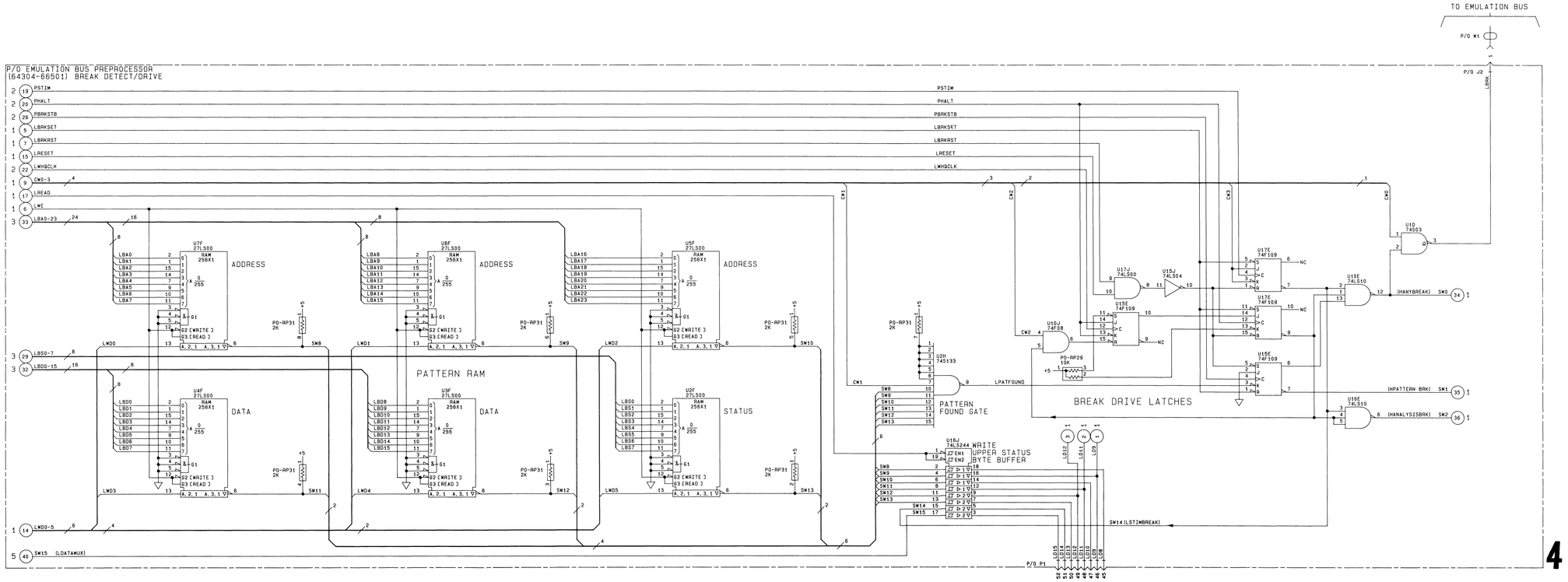


Figure 8-2. 64304A Component Locator (sheet 4 of 5)



IC's ON THIS SCHEMATIC

REF DES	HP PART NO.	MFG PART NO.	+5	GND	-5.2
U1D	1820-0682	SN74S03N	14	7	
U2F-U7F	1816-1092		16	8	
U2H	1820-1130	SN74S133N	16	8	
U10J	1820-2686	74F08PC	14	7	
U15E, U17E	1820-2693	74F109PC	16	8	
U15J	1820-1199	SN74LS04N	14	7	
U16E	1820-1202	SN74LS10N	14	7	
U16J	1820-2024	SN74LS244N	20	10	

PARTS ON THIS SCHEMATIC

RP29, 31

Figure 8-3.
64304A Schematic (sheet 4 of 5)

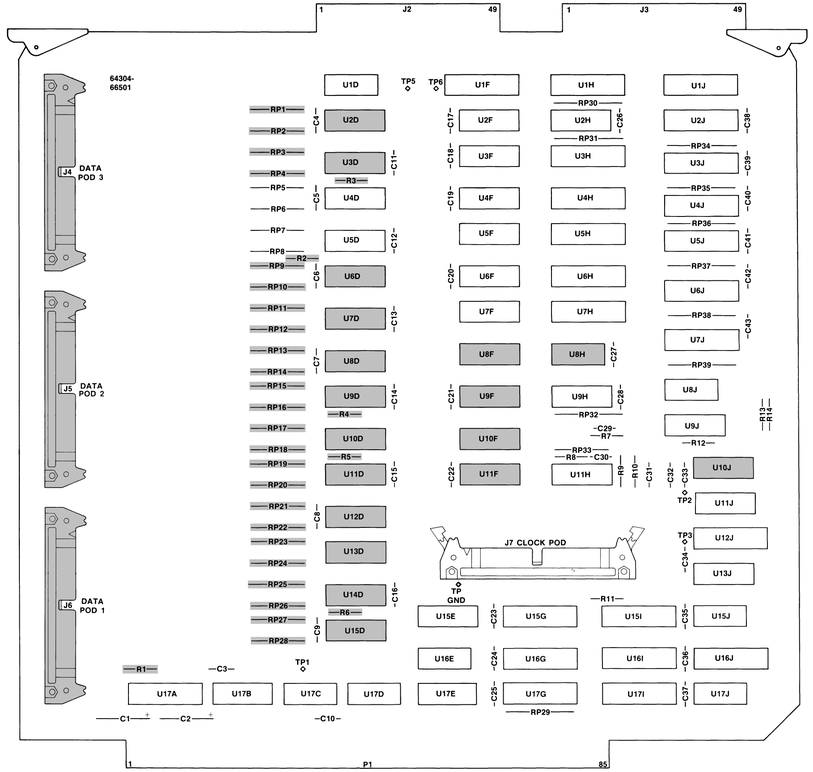
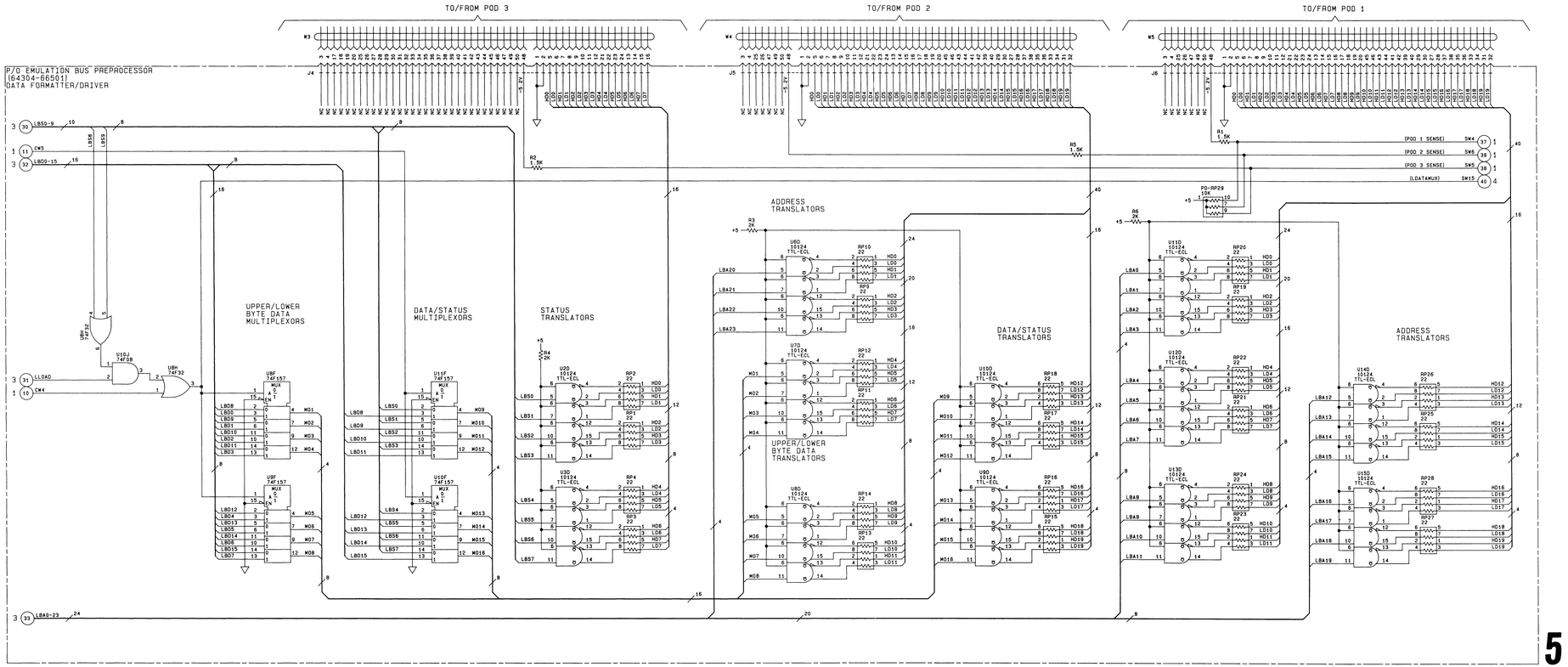


Figure 8-2. 64304A Component Locator (sheet 5 of 5)



5

IC's ON THIS SCHEMATIC

REF DES	HP PART NO.	MFG PART NO.	+5	GND	-5.2
U2D, U6D-U15D	1820-1173	MC10124L	9	16	8
U8F-U11F	1820-2654	74F157PC	16	8	
U8H	1820-2690	74F32PC	14	7	
U10J	1820-2686	74F08PC	14	7	

PARTS ON THIS SCHEMATIC

R1-6
RP1-4, 9-29

Figure 8-3.
64304A Schematic (sheet 5 of 5)

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Arranged alphabetically by country

Product Line Sales/Support Key

Key	Product Line
A	Analytical
CM	Components
C	Computer Systems Sales only
CH	Computer Systems Hardware Sales and Services
CS	Computer Systems Software Sales and Services
E	Electronic Instruments & Measurement Systems
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P	Personal Computation Products
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