64000

HP 64000 Logic Development System

Model 64650A General Purpose Preprocessor

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OPERATING MANUAL

Model 64650A
General Purpose
Preprocessor

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Chapter 1
GENERAL INFORMATION

The HP 64650A General Purpose Preprocessor is a versatile probe for the HP 64620S Logic State/Software Analyzer. The preprocessor is designed to operate with a variety of processor specific interface modules, providing a flexible and convenient probing capability.

By utilizing the appropriate interface module and control and data acquisition circuit boards, state/software analysis can be performed on both 8-bit and 16-bit microprocessor target systems and target system buses.

As many as 60 data channels are available for use in target system analysis. Channels not used for target system analysis are available for general purpose probing of the target system.

The components needed within the station mainframe for state/software analysis are:

a. 64621A Logic State Analyzer Control circuit board.
b. 64622A 40 Channel data acquisition circuit board.
c. 64623A 20 Channel data acquisition circuit board.

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Chapter 2
INSTALLATION

Connection of the preprocessor to the state/software analyzer is made through 50-conductor cables. The cables are plugged into the top cover of the preprocessor.

One of the cables is dedicated to transferring clock signals, and the remaining cables transfer address, data, and status signals. One clock cable and two data cables (40 data channels) are used for 8-bit target system analysis; one clock cable and three data cables (60 data channels) are used for 16-bit target system analysis.

Initializing the system is accomplished by loading software, normally provided on a mini-floppy disc, into the system.

In order to accommodate the specific target system to the state/software analyzer, an interface module must be installed in the preprocessor pod. The interface module must match the target system microprocessor.

If the analysis system is to be user defined, a special interface module must be installed in the preprocessor. The interface module must be designed and configured by the user. Software, including format specification, status mapping, and machine code inverse assembly, must also be user generated.

For additional information refer to the "Software Updating Procedure" found in the 64000 System Software Reference Manual.

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Chapter 3
INTERFACE MODULE

The interface module consists of microprocessor specific software and hardware.

The software includes a configuration file, composed of the trace specification (usually of a default type), the format specification and symbol maps, and an inverse assembler that will display trace information in the target system mnemonics.

The interface module has circuitry in it that provides the connection to the target system, and typically consists of buffers to reduce the loading of the target system. Some interface modules have circuitry to generate additional status, to dequeue instruction flow, or have other functions unique to that microprocessor. In addition, microprocessors that have multiplexed buses are demultiplexed so that all information about a bus cycle is contained in one analysis state.

Connection of the interface module to the target system is accomplished by removing the target system microprocessor, plugging the cable socket into the target system socket, and then installing the microprocessor into the cable socket.

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Chapter 4
PREPROCESSOR OPERATION

The preprocessor can accommodate 68 channels of information. These 68 channels are divided into five groups. There are 24 channels in the address group, 16 channels in the data group, 12 channels in the user definable group, 8 channels in the status group, and 8 channels in the clock group. The address and status groups are latched and can be sampled at any clock time; the user-definable and data groups are not latched and must be sampled at master clock time. Clocks 2 & 3 capture the address group, clocks 4 & 5 capture the status group, and the remaining clocks, 0, 1, 6, and 7, are connected directly to the analyzer. See Figure 4-1 for the preprocessor block diagram.

The interface module determines how the four clocks (two clocks for the status group, two clocks for the address group) latch target system information. The active polarity of each clock is selectable, or the clock may be disabled. The two clocks for each group are OR'ed. All of these options are defined when a using a microprocessor specific interface module.

The preprocessor and interface module identify themselves to the state/software analyzer so that proper configuration and inverse assembly software will be used.

Data collected from the target system is processed and displayed on the station CRT at the operators request. Control of data collection and mode of display is exercised through state/software analyzer softkey commands.

The preprocessor performs in a manner that is transparent to the target system unless a stimulus or halt signal is utilized. These signals are controlled in the state/software analyzer trace specification.

The STIMULUS line can be defined to become active at trigger, window, or sequencer events. The HALT line can be activated at trace point or at measurement complete. The trigger, window, or sequencer events can be assigned to drive BNC Port 1 with the STIMULUS line; the trace point or measurement complete can be assigned to drive BNC Port 2 with the HALT line. The signals at the BNC ports are not, however, controlled by the preprocessor.

The method by which the preprocessor utilizes the STIMULUS line is defined by the preprocessor-specification. The way in which it is connected to the target system is dependent upon the interface module being used.

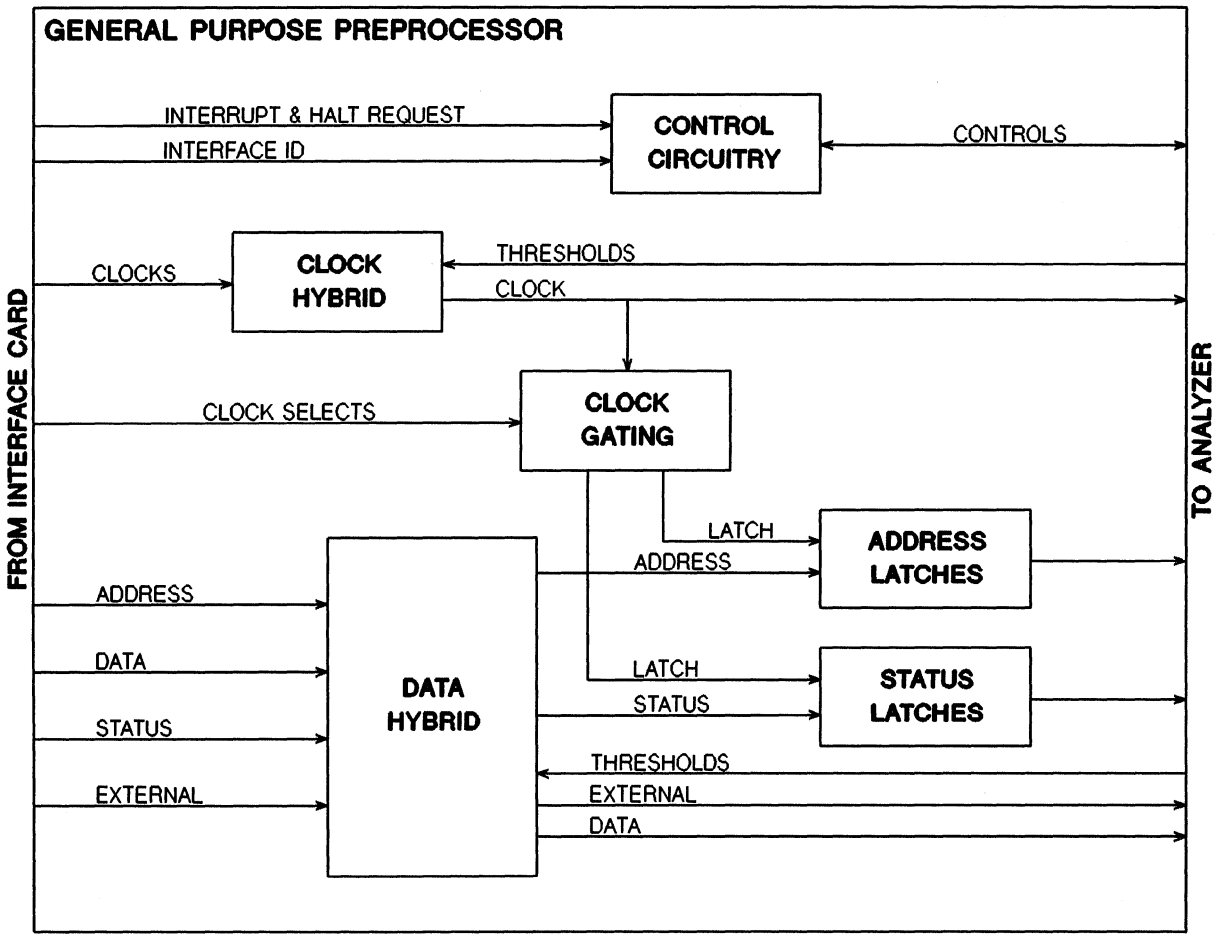

Figure 4-1. Preprocessor Block Diagram

The following sequence will cause the HALT line to exercise control of the target system after trace completion:

a. The desired trace must be correctly defined in the trace_specification.

b. The HALT line must be defined active, in the trace_specification, at measurement_complete. The syntax is:

    assert halt_line on measurement_complete

The HALT line is then connected to the target system through the interface module, and the target system will be halted at measurement_complete. The HALT line will remain active until the start of a new trace. The HALT line is an active low open collector output.

The STIMULUS line can be controlled with several variations in the preprocessor_specification. The choices are as follows:

a. Disabled.

b. Enabled.

   1. single mode.

      a) pulse mode (5 microsecond pulse).
      b) handshake mode (remains active once asserted).

   2. repetitive mode.

      a) pulse mode (5 microsecond pulse).
      b) handshake mode (remains active until acknowledged).

The preprocessor will block the signal if STIMULUS is disabled in the preprocessor_specification even though the STIMULUS line is defined in the trace_specification and becomes active during a trace.

The STIMULUS line, when enabled in the single mode, will be asserted only once during a trace, even if the conditions on which it is asserted become true more than once during the trace. The STIMULUS line, when enabled in the repetitive mode, will be asserted at each occurrence during the trace. The STIMULUS signal at the BNC port will in either case, single or repetitive, be asserted at each occurrence during the trace.

A choice of signal type, either pulsed or handshake, can be made for single or repetitive mode. The pulsed type is a signal approximately five microseconds in duration. The signal, in handshake mode, will remain asserted until acknowledged by the target system through the ACK line in the interface module. The ACK line is an active low input; the STIMULUS line is an active low open collector output.

There are nine INPUT/OUTPUT wires that can be plugged into the preprocessor endcap. (These wires and grabbers are supplied with the 64650A Preprocessor.) These lines are routed to the interface circuit board through connector J5 and are available at the wire wrap pins labeled INPUT/OUTPUT. The label on the preprocessor endcap can be written on with a standard lead pencil to identify the wires.

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