27140A

SIX CHANNEL MODEM MUX

FEATURES

- o Six full duplex modem/terminal channels
- o EIA RS-232-C AND CCITT V.28 compatability
- o Selectable number of bits/char: 5,6,7, or 8 plus parity
- o Selectable number of stop bits: 1,1.5,2
- o Two transmission modes: Full duplex hardwire or modem
- o Selectable parity: None, odd, or even
- o Internal clock
- o Programmable baud rate: 50,75,110,134.5,150,300,600,900, 1200,1800,2400,3600,4800,7200, 9600, or 19200. Default is 9600
- o Break detection and generation
- o Programmable device controlled X-ON/X-OFF handshaking
- o On board self-test which will automatically test frontplane circuitry if test hood is present
- o Timer for various modem functions
- o Optional interrupt for asynchronus event sensed

TERMINAL HANDSHAKING

X-ON/X-OFF

- Peripheral paces data transfer
- To stop card: X-OFF
- To start xmit: X-ON

ENQ/ACK

- Sender paces data
- Sender sends ENQ to request start
- Receiver responds with ACK

MODEM CONTROL

	Card Abbr	Common Abbr.	Description
INPUTS	RD	RD	Received Data
	CS	CTS	Clear To Send
	RR	CD (CARRIER DETECT)	Receiver Ready (Received Line Signal Detect)
	DM	DSR	Data Mode (Data Set Ready)
	IC	RI	Incoming Call (Ring Indicator)
OUTPUTS	SD	SD	Transmitted Data
	RS	RTS	Request To Send
	TR	DTR	Data Terminal Ready
	SR	SR	Frequency Select
	SG		Signal Ground

Modem Line Definitions

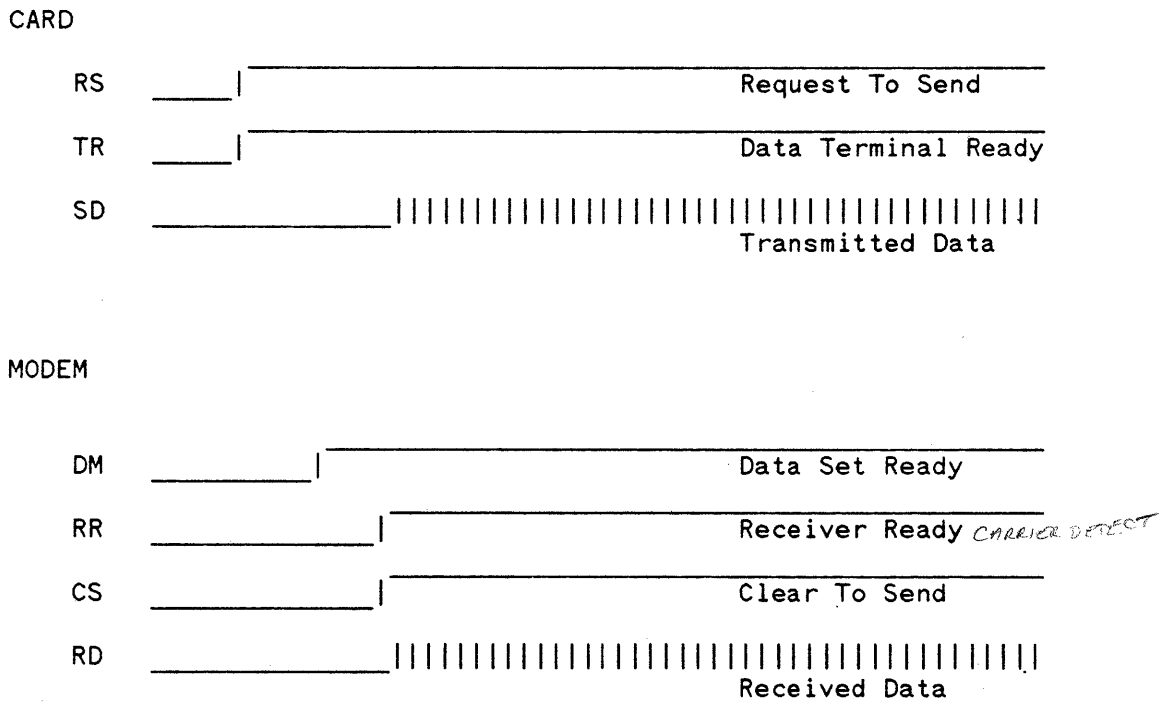
DM: Local modem is ready

RR: Remote modem is ready

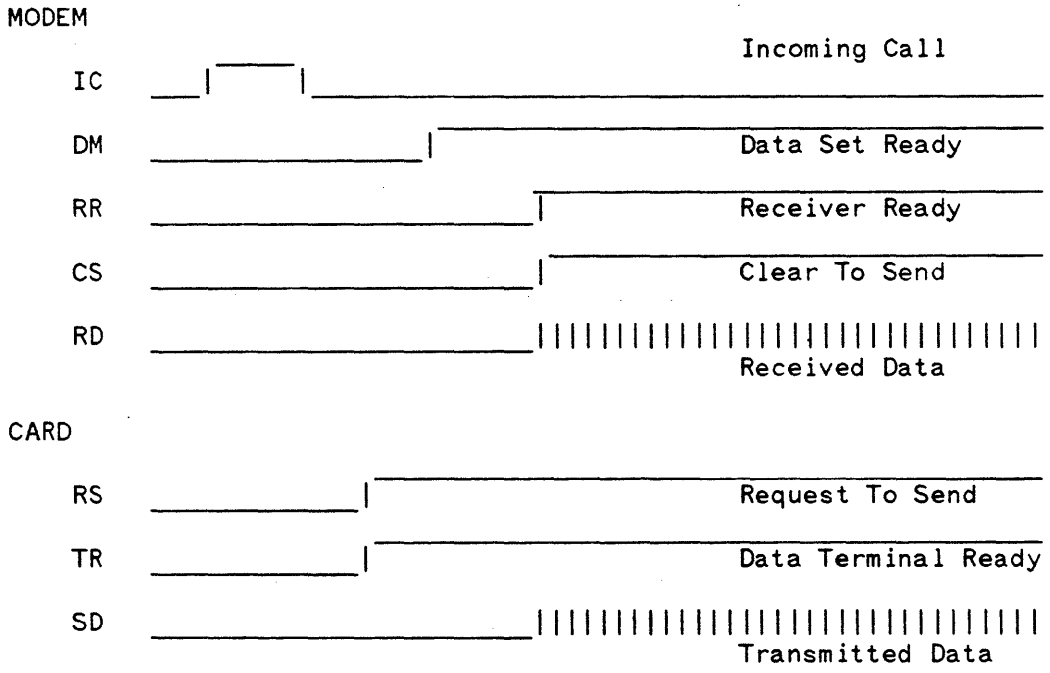
RD: Data, valid only while RR is active

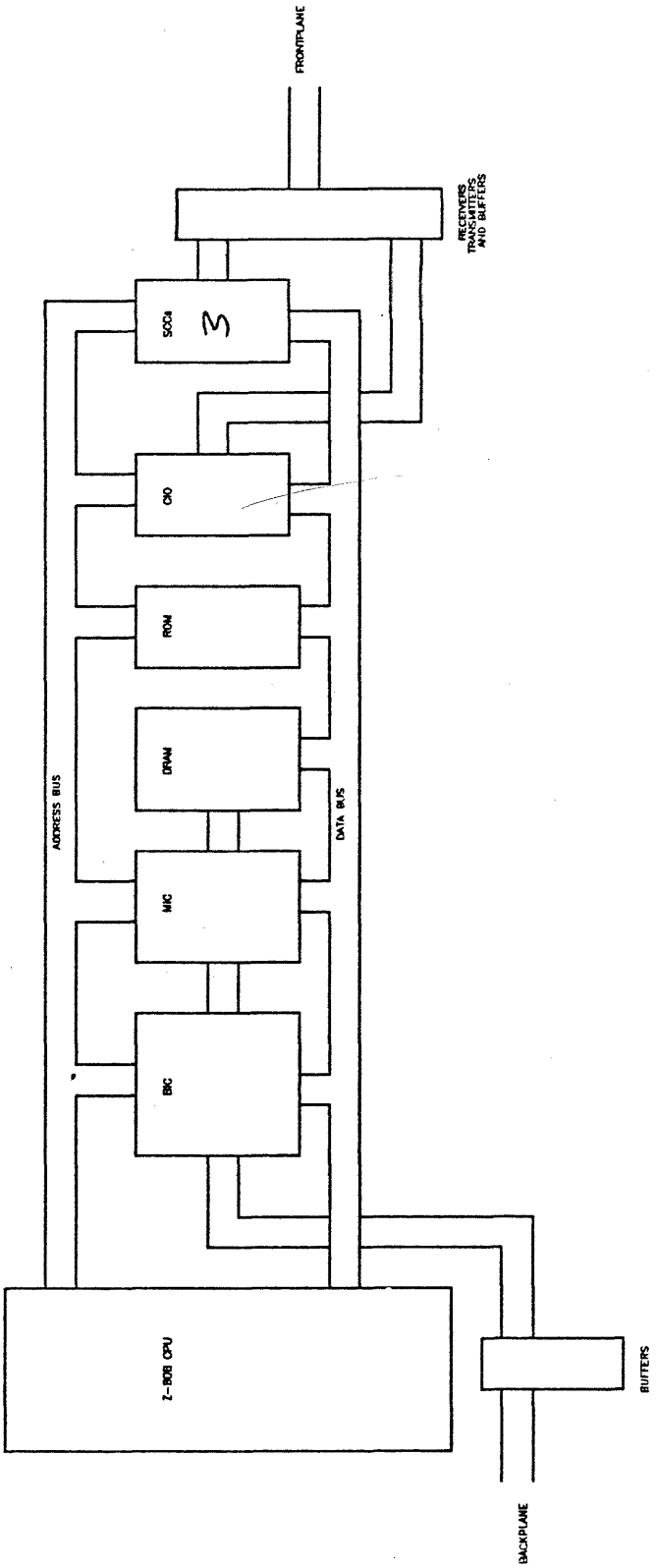
CS: Remote receiver ready to receive

CARD CALLS OUT



REMOTE MODEM CALLS





SIX PACK 6-Channel MODEM MUX Block Diagram.

FUNCTIONAL BLOCK OVERVIEW

CPU & CONTROL

I/O control PAL

Clock divider & I/O enable PAL

Frontplane Interface

75189A Receivers

75188A Drivers

J2-B2 +5V line not used

Data Com Circuit

3 SCCs

1 CIO (Parallel I/O & counter/timer)

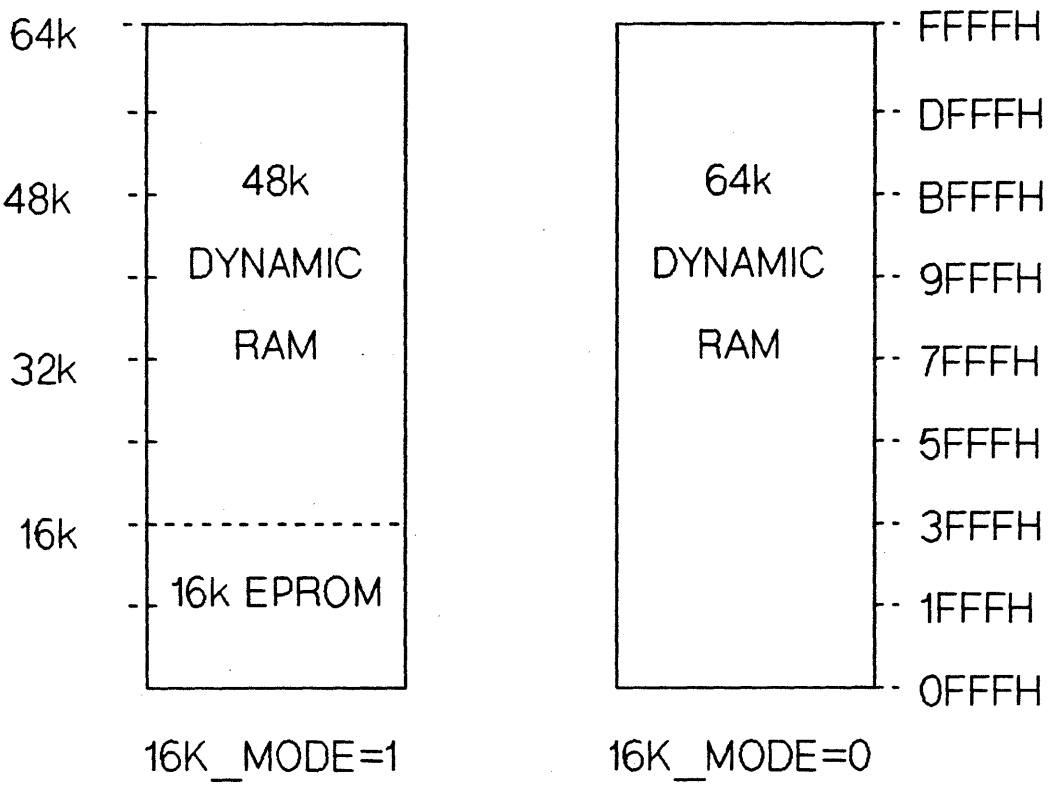
XMTR_DIS forces marking state

Memory Interface

MIC Chip

Hidden 16k unused

MEMORY ADDRESS SPACE



16K_MODE=1 CURRENT CONFIGURATION

16K_MODE=0 NOT USED

ABEHPD1

MEMORY INTERFACE CONTROLLER

- Controls up to 48K of DRAM
- Controls up to 16K of ROM
- Two programmable DMA channels
- Z80 compatible interrupts
- 12 programmable registers

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REGISTER  0 = MIC Configuration Register (read/write)
      Bit 7 = DM2, which selects which of IRQ1 or IRQ2 is
              the DMA request sensed by DMA channel B.
              If DM2 = 1, IRQ2 is sensed
              If DM1 = 0, IRQ1 is sensed
      Bit 6 = XNT, external interrupt enable.
              The IINT line to be sensed as an interrupt by
              the MIC interrupt control when XNT = 1.
      Bit 5 = DEND, when this bit = 1, the  function of OEND
              pin is disabled.
      Bit 4 through 0 are not used.

      NOTE: All of the above bits are zeroed upon reset.

REGISTER  1 = DMA B Upper Byte of Memory Address (write only)
              NOTE: This register is not effected by reset.

REGISTER  2 = DMA B Lower Byte of Memory Address (write only)
              NOTE: This register is not effected by reset.

REGISTER  3 = DMA B Configuration Register (read/write)
      Bit 7 = DMA channel B enable bit.
              1 = enable, 0 = disable.
      Bit 6 = Transfer from/to memory.
              0 = from memory, 1 = to memory.
      Bit 5 = Direction of memory address counter.
              0 = increment, 1 = decrement.
      Bit 4 = DMA channel B interrupt enable.
              0 = disable interrupt,
              1 = enable interrupt.
      Bit 3 = \
      Bit 2 =  \ Upper four bits of transfer
      Bit 1 =  / byte count for DMA B
      Bit 0 = /

            NOTE: Bits 4 through 7 are zeroed upon reset.
                  Bits 0 through 3 are not effected by reset.

REGISTER  4 = Lower Byte of Transfer Byte Count (read/write)
              Channel B.
              NOTE: This register is not affected by reset.

REGISTER  5 = DMA B I/O Port Address Register (read/write)
              NOTE: This register is not effected by reset.

REGISTER  6 = DMA A Upper Byte of Memory Address (write only)
                    (same as Register 1)

REGISTER  7 = DMA A Lower Byte of Memory Address (write only)
                    (same as Register 2)

REGISTER  8 = DMA A Configuration Register (read/write)
                    (same as Register 3)
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REGISTER 9 = Lower Byte of Transfer Byte Count
channel A (read/write)
(same as Register 4)

REGISTER A = DMA A I/O Port Address Register.
(same as Register 5)

REGISTER B = Interrupt Vector (read/write)
Bits 3 through 7 contain bits 3 through 7 of the interrupt vector address.

Bits 1 and 2 are modified automatically by the highest priority device requesting interrupt service. The following function shows how bits 2 and 1 are determined based on the interrupts sensed at interrupt acknowledge time.

DMA A	DMA B	IINT	VECTOR BITS		
			2	1	0
1	X	X	0	0	0
0	1	X	0	1	0
0	0	1	1	0	0

where X = don't care.

Bit 0 is always a logical zero.

NOTE: This register is not effected by reset.

I/O ADDRESSES

I/O PORT FUNCTION	I/O ADDRESS LINES								I/O PORT ADDR	REF DSG
	7	6	5	4	3	2	1	0		
MIC REGISTER 0	1	1	1	0	0	0	0	0	E0H	U57
MIC REGISTER 1	1	1	1	0	0	0	0	1	E1H	
MIC REGISTER 2	1	1	1	0	0	0	1	0	E2H	
MIC REGISTER 3	1	1	1	0	0	0	1	1	E3H	
MIC REGISTER 4	1	1	1	0	0	1	0	0	E4H	
MIC REGISTER 5	1	1	1	0	0	1	0	1	E5H	
MIC REGISTER 6	1	1	1	0	0	1	1	0	E6H	
MIC REGISTER 7	1	1	1	0	0	1	1	1	E7H	
MIC REGISTER 8	1	1	1	0	1	0	0	0	E8H	
MIC REGISTER 9	1	1	1	0	1	0	0	1	E9H	
MIC REGISTER 10	1	1	1	0	1	0	1	0	EAH	
MIC REGISTER 11	1	1	1	0	1	0	1	1	EBH	
BIC REGISTER 0	1	0	1	1	X	0	0	0	B0H	U42
BIC REGISTER 1	1	0	1	1	X	0	0	1	B1H	
BIC REGISTER 2	1	0	1	1	X	0	1	0	B2H	
BIC REGISTER 3	1	0	1	1	X	0	1	1	B3H	
BIC REGISTER 4	1	0	1	1	X	1	0	0	B4H	
BIC REGISTER 5	1	0	1	1	X	1	0	1	B5H	
BIC REGISTER 6	1	0	1	1	X	1	1	0	B6H	
SCC 0: CH B CONTROL	0	0	1	1	X	X	0	0	30H	U85
SCC 0: CH B DATA	0	0	1	1	X	X	0	1	31H	
SCC 0: CH A CONTROL	0	0	1	1	X	X	1	0	32H	
SCC 0: CH A DATA	0	0	1	1	X	X	1	1	33H	
SCC 1: CH B CONTROL	1	0	0	1	X	X	0	0	94H	U73
SCC 1: CH B DATA	1	0	0	1	X	X	0	1	95H	
SCC 1: CH A CONTROL	1	0	0	1	X	X	1	0	96H	
SCC 1: CH A DATA	1	0	0	1	X	X	1	1	97H	
SCC 2: CH B CONTROL	1	1	1	1	X	X	0	0	F8H	U83
SCC 2: CH B DATA	1	1	1	1	X	X	0	1	F9H	
SCC 2: CH A CONTROL	1	1	1	1	X	X	1	0	FAH	
SCC 2: CH A DATA	1	1	1	1	X	X	1	1	FBH	
CIO PORT C	1	0	1	0	X	X	0	0	A0H	U75
CIO PORT B	1	0	1	0	X	X	0	1	A1H	
CIO PORT A	1	0	1	0	X	X	1	0	A2H	
CIO CONTROL	1	0	1	0	X	X	1	1	A3H	

INTERRUPTS

MASKABLE

→ Controlled by Z80 commands DI & EI

DISABLE INTERRUPTS

ENABLE INTERRUPTS

IM0: Set interrupt mode 0, 8080A mode. CPU will execute as an instruction whatever vector the interrupting device outputs.

IM1: Set interrupt mode 1, CPU will execute a restart from location 38H.

IM2: Set interrupt mode 2, indirect call using register I and 8 bits from interrupting device as pointer.

I Register Contents	7 bits from peripheral	0
Upper address byte	Lower address byte	

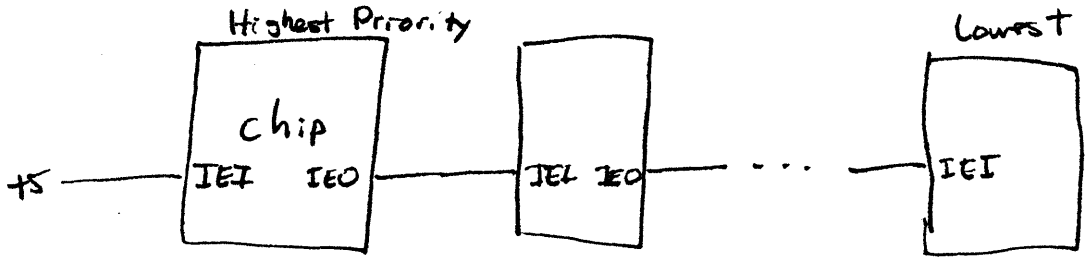
→ Prioritized by daisy chain

NON-MASKABLE

→ Restart from address 66H

DAISY CHAIN INTERRUPTS

PRIORITY	DEVICE	SUBFUNCTION
Highest	SCC 0	Channel A Receiver
	SCC 0	Channel A Transmitter
	SCC 0	Channel A External/Status
	SCC 0	Channel B Receiver
	SCC 0	Channel B Transmitter
	SCC 0	Channel B External/Status
	SCC 1	Channel A Receiver
	SCC 1	Channel A Transmitter
	SCC 1	Channel A External/Status
	SCC 1	Channel B Receiver
	SCC 1	Channel B Transmitter
	SCC 1	Channel B External/Status
	SCC 2	Channel A Receiver
	SCC 2	Channel A Transmitter
	SCC 2	Channel A External/Status
	SCC 2	Channel B Receiver
	SCC 2	Channel B Transmitter
	SCC 2	Channel B External/Status
	CIO	Counter/Timer 3
	CIO	Port A
	CIO	Counter/Timer 2
	CIO	Port B
	CIO	Counter/Timer 1
	MIC	DMA Channel A
	MIC	DMA Channel B
Lowest	BIC	



DMA PATH

RAM —— MIC —— BIC

→ 5120 Buffers used to maintain performance

→ HP-UX use character at a time I/O

→ Each character stored in a DMA quad in silo buffer

Data
Attribute (errors or spec. cmd.)
Port number
Number of data char = 1

SELF-TEST DETAILS

ROM TEST: The contents of the EPROM are verified using a Cyclic Redundancy Check (CRC) algorithm. The contents of the ROM are read one at a time in 4K blocks. Each byte is included in the algorithm and the resulting 16 bit number is checked against a 16 bit reference number stored in the EPROM. The two numbers must match.

RAM TEST: RAM is checked for stuck-at-0 and stuck-at-1 conditions. The address decoder is also checked. If reset was due to a RST, then the short RAM test is executed. If reset was due to a DCL, then the long RAM test is executed.

SCC TEST: The SCC is checked by performing basic asynchronus internal transmit and receive functions. If a loopback hood is sensed, a loopback is performed through the line drivers and receivers on the external data (RD and SD), and control lines connected to the SCC (RS, RR, CS, TR, and IC).

CIO TEST: Detects stuck-at faults in the data lines, system control, interrupt control, and the ?timers are checked? If the loopback hood is sensed, the modem signal lines (DM and SR) are checked through the line drivers and receivers.

BIC TEST: The BIC is tested for functional faults. Registers which can be tested like RAM by writing to them and then reading them have that done. The chip is also tested using the internal loopback functionality built into it. The testing of the BIC and the backplane receivers and drivers must be done in the system test.

MIC TEST: The MIC is tested for functional faults. The registers which can be written to and read from are tested for stuck-at-1 and stuck-at-0 faults. Some MIC registers cannot be tested (they are read only).

DMA TEST: This test transfers data between memory and the BIC through the MIC. The BIC operates in self-test mode in this operation.

1. A 6 byte pattern is written to the BIC FIFO (6 is the FIFO size)

2. The BIC is turned around by changing its configuration from host to device, which will cause the BIC to interrupt through the MIC (BIC interrupts are passed to the Z80 through the MIC).

3. The interrupt will initiate the BIC interrupt service routine which then sets up the DMA between the BIC and RAM.

4. When the transfer is complete, the MIC interrupts the Z80 and the Z80 compares the data in the RAM with the data it wrote into the BIC FIFOs.

When the card has completed self-test successfully, the LEDs are turned off on the card and on the hood and the card jumps to its standard firmware.