HEWLETT PACKARD

SERVICE MANUAL

7933 and 7935 DISC DRIVES

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OPTIONS COVERED

This manual covers options 120, 210, 220, 221, 222, 223, 241 and 242 as well as the standard HP 7933 and HP 7935 Disc Drives.

DESIGNED FOR HP-IB SYSTEMS

HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a computation system.

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The Federal Communications Commission (in 47 CFR 15.818) has specified that the following notice be brought to the attention of the users of this product.

FEDERAL COMMUNICATIONS COMMISSION
RADIO FREQUENCY INTERFERENCE
STATEMENT

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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PRINTING HISTORY

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NOTICE

PREFACE

This manual provides field service information for the Hewlett-Packard 7933 and 7935 Disc Drives and is intended for use by service-trained personnel. The disc drive is a state-of-the-art, mass memory product and, because of its product design, a modular replacement philosophy has been implemented to minimize on-site repair time. On-site troubleshooting and repair are assured through the use of the information provided in this manual and the maintenance aids contained in the service kit. For disc drive operator instructions, refer to the *HP 7933 Disc Drive Operator Instructions*, part no. 07930-90901, or the *HP 7935 Disc Drive Operator Instructions*, part no. 07935-90901. For installation and operating instructions, refer to the *HP 7933 Disc Drive Operating and Installation Manual*, part no. 07930-90902, or the *HP 7935 Disc Drive Operating and Installation Manual*, part no. 07935-90902, and the *Site Environmental Requirements Manual*, part no. 5955-3456. For functional differences of the controller cache drives from the standard drives (HP 7933H/7935H) see Appendix B.

WARNING

The disc drive contains magnetic material (motor-spindle assembly and actuator assembly), a potential hazard to personnel during shipping. Special packaging and markings are required by the United States Government for shipping. If reshipment of the disc drive becomes necessary, refer to the *HP 7933 Disc Drive Operating and Installation Manual,* part no. 07930-90902, or the *HP 7935 Disc Drive Operating and Installation Manual,* part no. 07935-90902, for repackaging instructions. If reshipment of the motor-spindle assembly becomes necessary, refer to section V of this manual for repackaging information.

The contents of this manual are organized in seven sections as follows:

- Section I, Theory of Operation, provides a general description of the disc drive followed by a functional circuit description of its operating systems.
- Section II, Channel Interface, provides a summary of the command and message formats required to implement channel communications of the Hewlett-Packard Interface Bus (HP-IB).
- Section III, Maintenance, provides maintenance information, maintenance precautions, lists standard and special tools and test equipment required to service the disc drive, and inspection and cleaning procedures.
- Section IV, Alignment and Adjustment, provides step-by-step alignment and adjustment procedures for the disc drive.
- Section V, Service Information, provides service information including details of the disc drive self-test and internal diagnostic routines.
- Section VI, Removal and Replacement, provides step-by-step removal and replacement procedures for each field-replaceable electrical and electro-mechanical assembly used in the disc drive.
- Section VII, Replaceable Parts, provides listings of all field-replaceable parts and an illustrated parts breakdown for the disc drive, as well as replacement part ordering information.
- Appendix A, Service Notes
- Appendix B, Controller Cache Service Information

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ILLUSTRATIONS

TABLES

SAFETY CONSIDERATIONS

KEEP WITH MANUAL

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an autotransformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by service-trained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

To install or remove a fuse, first disconnect the power cord from the device. Then, using a small screwdriver, turn the fuseholder cap counterclockwise until the cap releases. Install the proper fuse in the cap — either end of the fuse can be installed in the cap. Next, install the fuse and fuseholder cap in the fuseholder by pressing the cap inwards and then turning it clockwise until it locks in place.

THEORY OF OPERATION

SECTION I

1-1. INTRODUCTION

This section contains a general description of the HP 7933 and HP 7935 Disc Drives and their major components, followed by a discussion of the disc drive addressing structure, recording format, and principles of operation. Throughout this manual, any reference to "disc drive" is intended to mean the standard HP 7933 and HP 7935. The HP 7933XP and HP 7935XP controller cache drive differences are described in Appendix B.

1-2. GENERAL DESCRIPTION

The disc drive is a high-performance, random-access, microprocessor-controlled data storage device designed for use as a peripheral unit in medium and large computer systems. Data is stored on seven magnetic discs located in a self-contained media module housed in the disc drive. The media module is operator removable only in the HP 7935 Disc Drive. Only qualified service-trained personnel may remove the media module during required servicing of the HP 7933 Disc Drive.

The media module contains 13 surfaces for data storage and one servo surface with head positioning and sector timing information. Using the 13 data surfaces, the disc drive provides access to 404 million bytes of formatted information in a single package. Each data surface contains three precision head-position-determining bands that supply automatic head alignment information. A separate head is used for each data surface to retrieve existing data or to record new data. Head positioning on any of the 1,321 cylinder positions is controlled by a closed loop, track following, servo system that derives cylinder positioning information from the prerecorded data on the servo surface of the media module.

The disc drive contains sophisticated internal self-test diagnostics and fault detection circuitry that exercise the complete disc drive and indicate faults through an eight-character alphanumeric readout display on the front panel. The internal diagnostics permit complete off-line testing of the disc drive and the media module. The self-test diagnostics and the fault detection circuits furnish a quick and easy means of fault isolation to the printed-circuit assembly level. This quick isolation provides for increased serviceability and minimum downtime.

The disc drive is interfaced through the Hewlett-Packard Interface Bus (HP-IB) and has a built-in microprocessor controller providing for translation of high-level command words to command sequences intelligible to the disc drive. The controller supports system protocol designed to minimize the effects of data transfer errors. The controller is capable of managing bidirectional data transfers in multi-disc environments.

This furnishes the user with maximium capabilities in terms of system configuration and data transfer efficiency. Sophisticated error correction code (ECC) algorithms and hardware make it possible to detect and provide correction information for virtually all single-burst data errors.

The disc drive is housed in a free-standing cabinet. The principle components of the disc drive, as described in the following paragraphs, include disc rotation components, an electromechanical head-positioning actuator assembly, printed-circuit electronic assemblies, a power module, and air circulation and cooling components.

1-3. DISC ROTATION COMPONENTS

The disc rotation components include a media module chamber and a spindle assembly. The spindle assembly consists of a brushless dc spindle motor and hub on which the media module is attached. The media module is a magnetic disc data storage module containing seven 356-millimetre (14-inch) diameter discs. One disc surface is dedicated to servo head position and sector information and the remainder are data surfaces. The speed of the spindle motor is maintained at 2,700 rpm by control circuits on spindle driver printed-circuit assembly (PCA) A12.

1-4. ACTUATOR ASSEMBLY

The actuator assembly is an electromechanical unit consisting of a coil and carriage assembly, a magnet and rail assembly, a velocity transducer (tachometer), and two temperature sensors.

The read/write heads and the servo head are attached to the coil of the carriage assembly. This coil, together with the permanent magnet on the rail assembly form a linear motor. Head positioning is achieved by applying a current to the coil of the motor. The rail assembly is aligned such that when the motor is energized, the carriage moves the heads inwards or outwards from the center of the media module. The velocity

transducer measures the linear velocity of the coil and carriage assembly. The transducer consists of a small cylindrical coil and a permanent magnet. The coil is fixed in the center of the linear motor coil and the magnet is attached to the carriage. Movement of the magnet through the coil generates a voltage with a magnitude proportional to the linear velocity of the motor and the polarity indicating the direction of motion. This voltage is used by the servo loop controlling the linear motor to achieve acceleration/deceleration during carriage movement between disc tracks.

A carriage latch and carriage back detector mounted on the side of the linear motor magnet control the loading action of the actuator. When the heads load, the latch solenoid is energized momentarily to retract the latch and allow the carriage to move away from its retracted (home) position. When the carriage returns to its home position, the latch automatically locks the carriage in place. The carriage latch back detector reports to the microprocessor when the carriage is in the home position.

The temperature transducers monitor the temperature of the actuator assembly and the airstream exiting from the media module chamber, and alert the microprocessor of an over-temperature condition.

1-5. DATA AND SERVO HEADS

The media module contains 13 data surfaces and one servo surface. Using one head per surface, the disc drive has 13 data heads and one servo head. The data heads are read/write heads that read data from or write data onto the data surfaces. The servo head is a read-only head that reads head position information from the prerecorded servo surface.

The heads are designed to fly above the discs supported by a thin cushion of air that acts as an air bearing to the heads. This air bearing functions as a very stiff spring which is opposed by the leaf spring on each head arm. These two opposing spring forces tend to cancel one another at a flying height of approximately 25 microinches. In order for the heads to fly properly, several conditions must be satisfied. These conditions include the cleanliness of the air surrounding the disc surfaces, the axial runout and flatness of the disc surfaces, and the flatness of the head surface near the read/write gap.

Each head consists of a gapped ferrite core mounted in a ceramic shoe. There are two windings wound around the ferrite core and the windings are connected at a common point and phased such that the common point acts as a center tap. These windings are used for both reading and writing by detecting or producing a magnetic field at the gap in the ferrite core.

Data is written by passing a current through the windings in a selected data head. This current generates a flux field across the gap that magnetizes the iron oxide particles bound to the surface of the disc. The writing process orients the poles of each magnetized particle to permanently store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of the write current polarity. Erasing is accomplished by writing over any data which may have been previously recorded on the disc.

In a read operation, as the data surface passes beneath a data head, the magnetically stored flux fields intersect the gap in the ferrite core. Gap motion through the flux field causes a voltage to be induced into the windings wound around the core. This induced voltage is analyzed by the read circuitry to define the data recorded on the data surface. Each flux reversal, caused by a write current polarity change, generates a readback voltage pulse.

1-6. PRINTED-CIRCUIT ASSEMBLIES

There are 18 printed-circuit assemblies (PCA's) in the disc drive, as listed below.

- Regular PCA-A1
- Actuator Driver PCA-A2
- Servo PCA-A3
- Microprocessor PCA-A4
- Disc Memory Access (DMA) PCA-A6
- Formatter/Separator PCA-A8
- Track Follower PCA-A9
- Read/Write PCA-A10
- Motherboard PCA-A11
- Spindle Driver PCA-A12
- DC Power PCA-A13
- Control Panel PCA-A14
- Data Input PCA-A15 (part of A14)
- Load/Unload PCA-A16 (part of A14)
- HP-IB PCA-A17
- Actuator Status PCA-A18
- Emergency Retract PCA-A20 (part of A2)
- Line Filter PCA-A21

Controller Cache PCA's (see Appendix B):

- Cache PCA-A5
- CDMA PCA-A6

Ten of the PCA's (A1 through A4, A6, A8 through A11, and A20) are located in a card cage assembly and the remainder are mounted at other locations in the disc drive enclosure. A brief description of the function of each PCA is provided in the following paragraphs.

1-7. REGULATOR PCA-A1. Regulator PCA-A1 contains +5 Vdc, +12 Vdc, and -12 Vdc regulated supplies that provide operating power for the PCA's housed in the card cage. Unregulated dc voltages are input to PCA-A1 from dc power PCA-A13 in the power module via a cable assembly. Regulator PCA-A1 also contains circuitry that monitors certain conditions of the disc drive ac input power and dc voltages and makes this information available to microprocessor PCA-A4 for self-test purposes.

1-8. ACTUATOR DRIVER PCA-A2. The basic function of actuator driver PCA-A2 is to cause a current to flow in the coil of the actuator linear motor in response to a command voltage from servo PCA-A3. The actuator driver PCA also contains a number of the components comprising the emergency retract circuit. The actuator driver can be self tested by microprocessor PCA-A4.

1-9. SERVO PCA-A3. Servo PCA-A3 controls the positioning of the carriage and head assembly. The servo PCA also acts with microprocessor PCA-A4 to perform track-to-track seeks, head loading and unloading, and self test. The offset for automatic head alignment is input to servo PCA-A3. Servo PCA-A3 also contains circuits to compensate the servo system for track following.

1-10. MICROPROCESSOR PCA-A4. Microprocessor PCA-A4 supervises overall operation of the disc drive by addressing and enabling appropriate circuit blocks in response to input commands from the host computer. The input commands place the microprocessor in one of four operational modes: control operations, which do not involve transfer of data; sense operations which determine the state of the disc drive; read operations, which transfer data from the disc drive to the system host memory storage; and write operations, which transfer data from the system host memory to the disc drive. The microcodes for the specific instructions are stored in read-only memory (ROM) located on the microprocessor PCA. In addition, the microprocessor PCA circuitry includes ROM-based self check diagnostics and test programs that facilitate troubleshooting the disc drive operating systems.

1-11. DISC MEMORY ACCESS PCA-A6. Disc memory access (DMA) PCA-A6 provides an HP-IB interface, a microprocessor interface, serial/parallel data conversion, an implementation of the cyclic redundancy check (CRC) for data integrity on data transfers, and an error correction code (ECC) circuit for improving the integrity and recoverability of data written on the disc surfaces. The HP-IB interface is used to interface the disc drive to the system host computer through the Hewlett-Packard Interface Bus (HP-IB). The microprocessor interface gives microprocessor PCA-A4 the ability to control data transfers through the DMA, and allows the microprocessor access to the HP-IB for command interpretation and execution. During a write operation, the ECC circuitry adds redundant information to the data written on the disc. On a read operation, the ECC circuitry examines the data and the redundant information. From this information the ECC module can determine if an error has occurred and correct it if the length of the error is 12 bits or less. Most errors exceeding 12 bits are detected but not corrected. The serial/parallel data conversion function is part of the read/write system. The DMA PCA can be self tested by microprocessor PCA-A4.

1-12. FORMATTER/SEPARATOR PCA-A8. Formatter/Separator PCA-A8 encodes input data to the read/write channel and decodes output data from the read/write channel. During a write operation, data is clocked from the serial/parallel data conversion circuitry on DMA PCA-A6 to PCA-A8 where it is encoded and precompensated before being transmitted to read/write PCA-A10. During a read operation, data from read/write PCA-A10 is analyzed by decoder circuitry on PCA-A8 to define the data recorded and then it is clocked into the serial/parallel data conversion circuitry on PCA-A6. The formatter/separator PCA can be tested by microprocessor PCA-A4.

1-13. TRACK FOLLOWER PCA-A9. Track follower PCA-A9 provides an output that is proportional to the distance that the servo head is from the center of a servo track. This information is used by the head positioning system. The track follower PCA also informs the read/write system where data sectors begin and supplies automatic head alignment data. The track follower PCA can be self tested by microprocessor PCA-A4.

1-14. READ/WRITE PCA-A10. Read/Write PCA-A10 is an integral part of the read/write system. In the read mode, the readback signals caused by the flux transitions on the disc are changed by PCA-A10 into a series of narrow pulses coincident with zero crossings. These signals are sent to formatter/separator PCA-A8 for decoding and further processing. In the write mode, PCA-A10 changes the encoded write data from formatter/separator PCA-A8 into alternating flux transitions coincident with the incoming data to be written on the disc. The read/write circuitry can be self tested by microprocessor PCA-A4.

1-15. MOTHERBOARD PCA-A11. Motherboard PCA-A11, located at the base of the card cage assembly provides for the interconnection of signals and distribution of power between the PCA's housed in the card cage. The card cage PCA'S are connected

to motherboard PCA-A11 through receptacles mounted on the motherboard. An additional connector on the edge of the motherboard allows spindle driver PCA-A12 in the power module to be connected by cable to the card cage PCA's.

1-16. SPINDLE DRIVER PCA-A12. Spindle driver PCA-A12, located in the power module, provides power to the spindle motor to maintain its speed at 2,700 revolutions per minute. Spindle driver PCA-A12 also contains self-test logic circuitry and unregulated dc power supply circuits that furnish operating power for the spindle driver and actuator driver control amplifiers.

1-17. DC POWER PCA-A13. DC Power PCA-A13, located in the power module, rectifies and filters ac voltages from the secondary windings of the power transformer to provide unregulated dc power for regulator PCA-A1 in the card cage. The output voltages from PCA-A13 are connected by cable to PCA-A1 in the card cage.

1-18. CONTROL PANEL PCA-A14. Control panel PCA-A14, located behind the front panel of the disc drive, performs the following functions:

- Accepts inputs from the keyboard on data input PCA-A15.
- Accepts inputs from the switches on load/unload PCA-A16.
- Accepts input from the air pressure sensor.
- Displays status messages from the microprocessor.
- Displays internal diagnostic program data input by service-trained personnel.

Control panel PCA-A14 is connected to microprocessor PCA-A4 via a 34-conductor ribbon cable.

1-19. DATA INPUT PCA-A15. Data input PCA-A15 consists of a keyboard that permits front panel selection of the disc drive internal diagnostic commands. The data input PCA is a subassembly of control panel PCA-A14.

1-20. LOAD/UNLOAD PCA-A16. Load/Unload PCA-A16 contains two switches: one permits front panel control of the disc drive load/unload function, the other controls the top door unlock feature on the HP 7935. The second switch is disabled in HP 7933 Disc Drives. The load/unload PCA is a subassembly of control panel PCA-A14.

1-21. HP-IB PCA-A17. HP-IB PCA-A17, mounted at the rear of the enclosure, permits the disc drive to be interfaced to the system host via a standard HP-IB cable. The HP-IB channel select switch is also mounted on the HP-IB PCA.

1-22. ACTUATOR STATUS PCA-A18. Actuator status PCA-A18, mounted on the side of the actuator assembly and connected by cable to servo PCA-A3, provides an interface for the temperature sensors, tachometer, carriage lock solenoid, and carriage back detector on the actuator assembly.

1-23. DELETED

1-24. EMERGENCY RETRACT PCA-A20. Emergency retract PCA-A20 supplies emergency retract power to the actuator assembly in the event of an emergency condition requiring retraction of the heads. PCA-A20 is a subassembly of actuator driver PCA-A2.

1-25. LINE FILTER PCA-A21. Line filter PCA-A21, mounted in the power module input power assembly, contains a line filter that suppresses radio frequency energy generated by the disc drive.

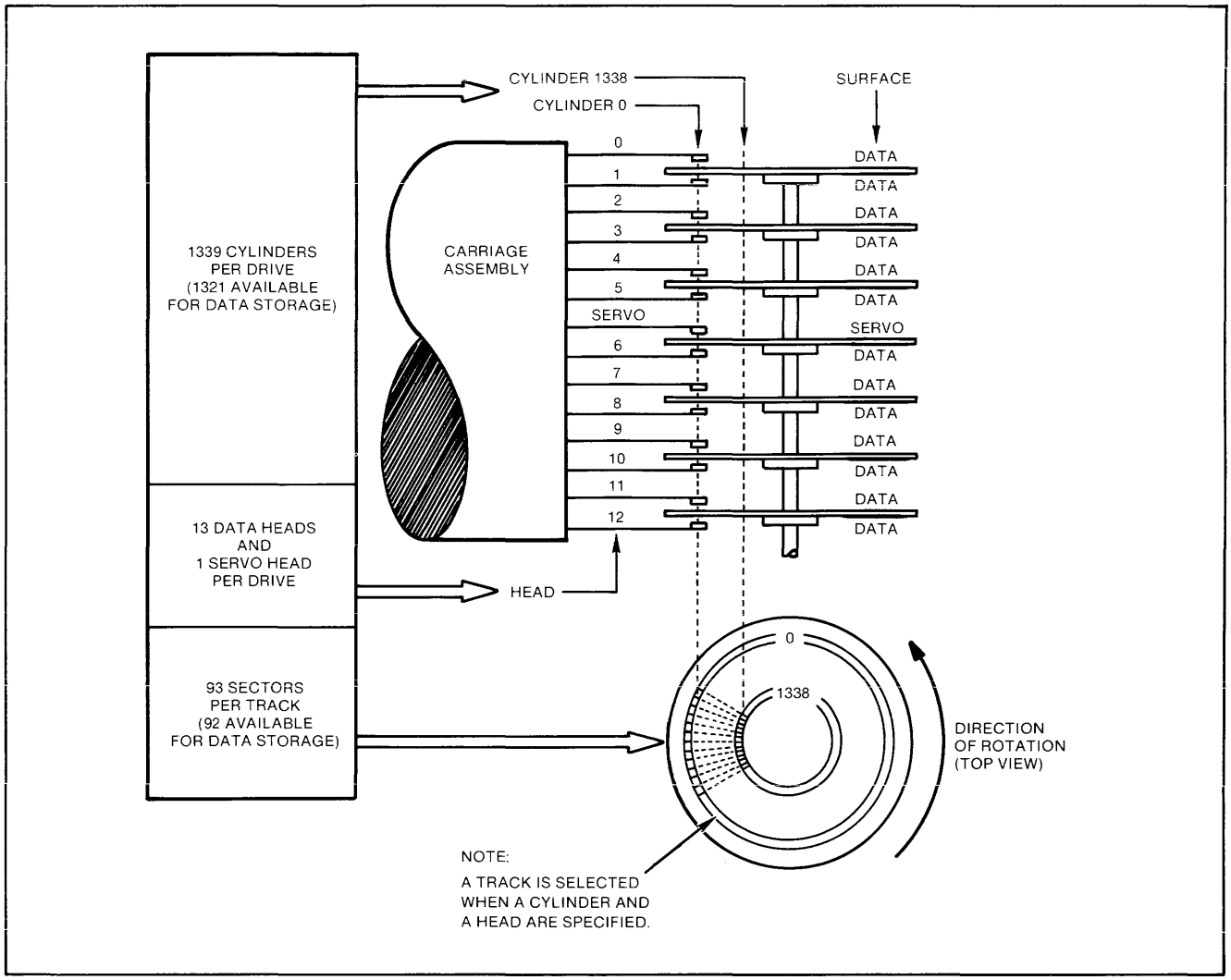
1-26. POWER MODULE

The power module consists of a metal casting on which are mounted a number of the components comprising the disc drive dc power system. The components include a captive power cord, a primary power circuit breaker, a power transformer, dc power PCA-A13, and line filter PCA-A21. Spindle driver PCA-A12 is also located in the power module. The power module is mounted on rack slides at the rear of the disc drive cabinet to facilitate servicing.

1-27. ADDRESSING STRUCTURE

The media module used with the disc drive contains seven discs. (See figure 1-1.) These discs provide 13 data surfaces and one servo surface. The disc drive accesses data on the 13 data surfaces with 13 read/write (data) heads.

Head positioning information and sector clocking are derived from the servo surface through a read-only servo head. There are 1321 ensured cylinder positions available for data storage. Cylinder addresses range from zero to 1320. Each data cylinder consists of 13 data tracks, one for each data surface. Tracks are addressed when both cylinder and head addresses are specified. Each data track is divided into 93 physical



7933-300

Figure 1-1. Disc Drive Addressing Structure

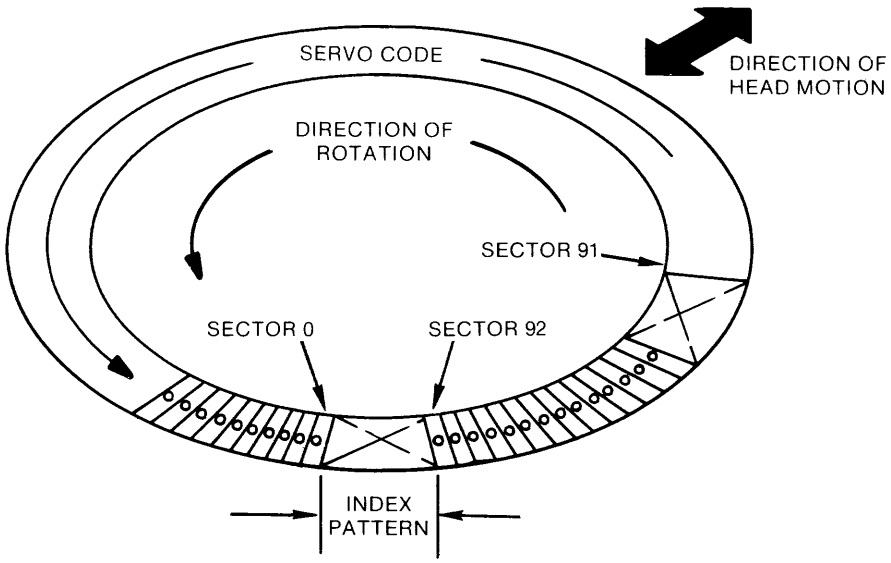
data sectors. Sectors are addressed when both head and sector addresses are specified for a given cylinder. Head addresses range from zero to 12.

All addressing in the disc drive is logical. The controller assigns physical addresses to the logical addresses. When a defective physical track is encountered, a new physical track (spare track) will be assigned to the same logical address. This eliminates dual seeks to obtain the correct data and reduces system overhead in managing the discs and spare tracks. A total of 1321 tracks are guaranteed as logical tracks through the use of the spares, which the controller assigns as required. There are 92 logical sectors (addressed from 0 to 91) for data storage, while the 93rd is reserved as a spare for use in the event that one of the original 92 logical sectors becomes defective. Sectors are spared by the controller. Should more than one sector per track develop unrecoverable errors, the entire logical track will then be assigned a new physical address (one of the spare tracks). This sparing action is transparent to the host CPU.

Each servo surface has 93 sector clock patterns encoded on it. (See figure 1-2.) A sector clock pattern consists of 8 dibits on the plus odd tracks and a pattern of 8 dibits on the plus even tracks. The physical location of each data sector is determined by counting index pulses after reading a sector. The sector counting electronics count these index pulses to keep track of the physical sectors as they pass beneath the heads.

1-28. ADDRESSING MODE

The microprocessor operates in a cylinder mode to access the data storage areas of the disc drive. (See figure 1-3.) In the cylinder mode, the heads are positioned over a particular cylinder and then data is written or read starting with the lowest numbered head and continuing to the highest numbered head. A cylinder of information therefore consists of all sectors on all tracks at a given cylinder address. Head switching occurs after the data in sector 91 of the cur-



NOTES:

1. SERVO CODE = 17,819 DIBITS PER REVOLUTION.
2. SECTOR CLOCK = 285,099 CYCLES PER REVOLUTION (12.8 MHz AT 2694 RPM).
3. ONE INDEX PULSE IS GENERATED PER SECTOR (93 PER REVOLUTION).

7933-301

Figure 1-2. Sector Clock and Index Generation

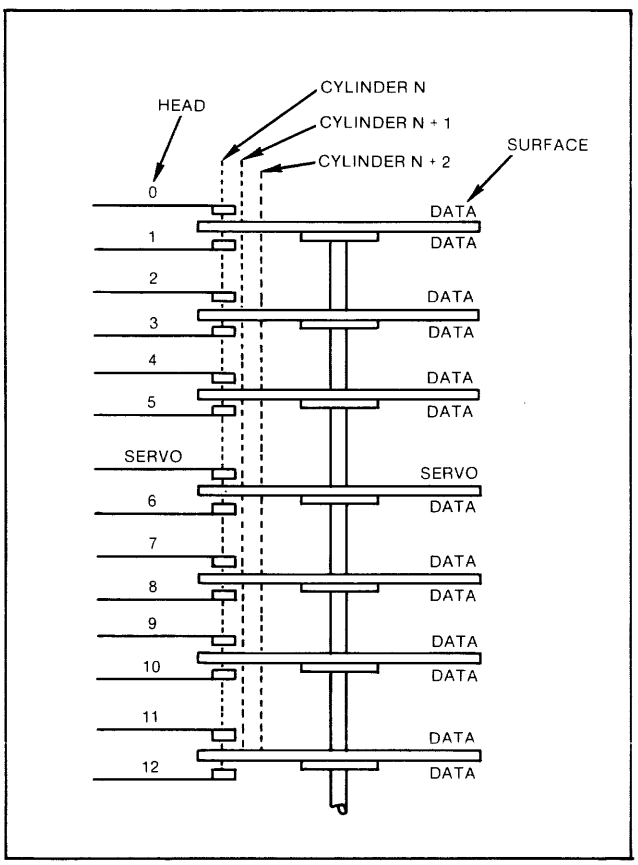
rent track has been transferred. Head switching is sequential, that is, head 1 will be selected after head 0, and so on. Data transfers will continue with sector 0 of the next track after the address fields and track status indicators of a sector of that track have been verified by the microprocessor.

1-29. SECTOR FORMAT

The smallest directly addressable storage area on a data surface is a data sector. (See figure 1-1.) Accessing a data sector is accomplished when the internal microprocessor-based controller specifies the address of the cylinder, head, and sector. Each data sector contains a 28.5-byte preamble, a 256-byte data field, and 6.375-byte postamble. (See figure 1-4.)

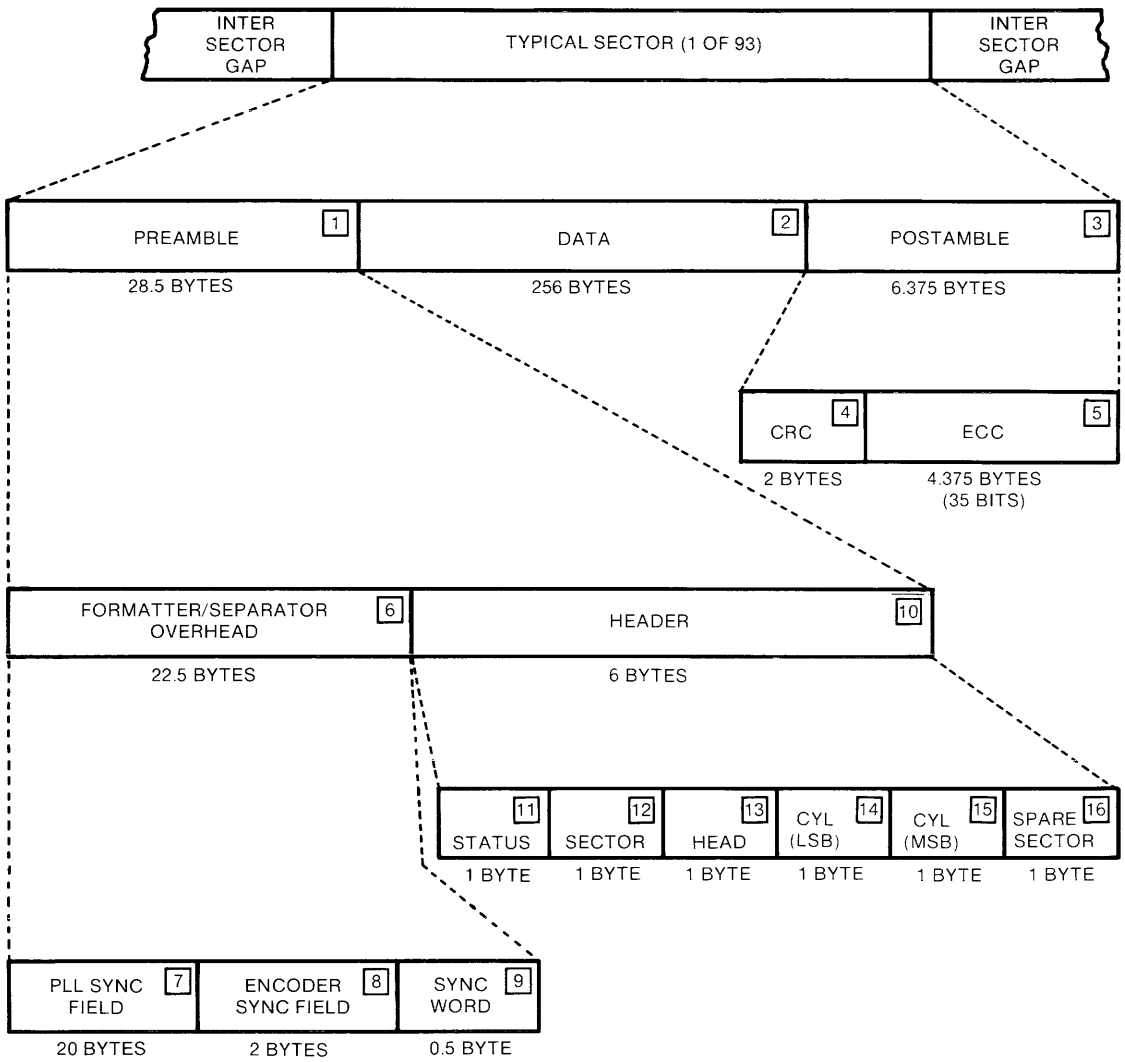
The 28.5-byte preamble is used for synchronization and addressing purposes. It is comprised of a 22.5-byte formatter/separator sync field; and a 6-byte header field which specifies status, head and sector addresses and provides the spare and track status indicators.

The data field is used to store 256 bytes of data. Each byte is defined as being eight bits. Only the data field is transferred to and from the system during most data operations. The preamble and postamble are normally generated and checked by the controller.



7933-302

Figure 1-3. Cylinder Mode



1 PREAMBLE — 28.5 BYTES FOR SYNCHRONIZING AND ADDRESSING.

2 DATA — 256 BYTES OF DATA.

3 POSTAMBLE — 6.375 BYTES FOR DATA CHECK AND ERROR CORRECTION.

4 CRC — CYCLIC REDUNDANCY CHECK. 16 BITS FOR CHECK AND CORRECTION INFORMATION.

5 ECC — ERROR CORRECTION CODE. 35 BITS FOR CHECK AND CORRECTION INFORMATION.

6 FORMATTER/SEPARATOR OVERHEAD — 22.5 BYTES TO ACHIEVE SYNCHRONIZATION.

7 PLL SYNC FIELD — 20 BYTES TO ACHIEVE PHASE.

8 ENCODER SYNC FIELD — 2 BYTES FOR ENCODE SYNCHRONIZATION.

9 SYNC WORD — 0.5 BYTE SIGNALLING START OF DATA FIELD.

10 HEADER — 6 BYTES FOR STATUS AND ADDRESSING INFORMATION.

11 STATUS — 1 BYTE FOR TRACK STATUS.

12 SECTOR — 1 BYTE FOR PHYSICAL SECTOR ADDRESS.

13 HEAD — 1 BYTE FOR PHYSICAL HEAD ADDRESS.

14 CYL (LSB) — 1 BYTE FOR PHYSICAL CYLINDER ADDRESS (LSB).

15 CYL (MSB) — 1 BYTE FOR PHYSICAL CYLINDER ADDRESS (MSB).

16 SPARE SECTOR — 1 BYTE FOR LOGICAL SPARE ADDRESS.

7933-304A

Figure 1-4. Disc Drive Sector Format

The 6.375-byte postamble consists of a 2-byte cyclic redundancy check (CRC) word and 4.375 bytes (35 bits) of error correction code. The controller generates the CRC information during a write operation and appends it to the other information written in the sector. The check information itself depends on the value of every bit from the first bit in the header field to the last bit in the data field. During a read operation, this check information is regenerated and compared in such a way that the presence of errors is detected. The ECC circuitry can automatically, and with no delay, correct up to 12 contiguous bits per sector.

1-30. FUNCTIONAL DESCRIPTION

The disc drive is organized into seven functional systems. (See figure 1-5.) These are the microprocessor control system, control panel system, spindle rotation system, head positioning system, read/write system, power distribution system, and air circulation and filtration system. Each of the functional systems is described in the following paragraphs.

The microprocessor control system (1) supervises overall operation of the disc drive, including self-test routines and internal diagnostics. The control panel system (2) accepts inputs from an operator through a keyboard and switches, displays the operating state of the disc drive on an eight-character alphanumeric display and provides an interface for sensor signals from the media module chamber. The spindle rotation system (3) provides power to the spindle motor and maintains its speed at 2,700 revolutions per minute. The head positioning system (4) controls the loading and unloading of the heads under normal and abnormal circumstances. The head positioning system also causes the heads to be accurately positioned over a specified cylinder during an initial head load, forward or reverse seek, or recalibration. The head positioning system also makes available sector data to the read/write system. The read/write system (5) provides an interface with the Hewlett-Packard Interface Bus (HP-IB) and the means to read information from a data surface or write information onto a data surface. The power distribution system (6) provides the operating voltages required for the remaining seven systems. The air circulation and filtration system (7) provides cooling air to the heat generating components of the disc drive and cool filtered air to the media module chamber.

Each of the functional systems is described in the following paragraphs. Accompanying the functional system descriptions are functional block diagrams and tables containing descriptions of the signal mnemonics used in the diagrams and text. Each of the functional block diagrams is identified by a large number in the lower right-hand corner of the page. These numbers are provided to assist in locating the system source and destination of signals flowing between the systems, and the source of the signals listed in the mnemonic tables. Most of the signal mnemonics have "-L" or "-H" suffixes. These suffixes identify active low and active high logic signals, respectively. Signals without such suffixes are analog signals. In addition, Section V, Service Information, contains an overall wiring diagram of the disc drive and a source and destination signal list for motherboard PCA-A11. The numbers identifying the system functional block diagrams are also included in this documentation.

1-31. MICROPROCESSOR CONTROL SYSTEM

The microprocessor control system consists of circuits on microprocessor PCA-A4. (See figure 1-15.) The primary purpose of the microprocessor control system is to supervise overall operation of the disc drive in response to input commands from the system host received via the Hewlett-Packard Interface Bus (HP-IB). Interface with the host takes place via disc memory access (DMA) PCA-A6 in the read/write system. (See figure 1-19.) Interface circuitry on PCA-A6 gives the microprocessor the ability to control data transfers through the DMA and also allows the microprocessor access to the HP-IB for command interpretation and execution.

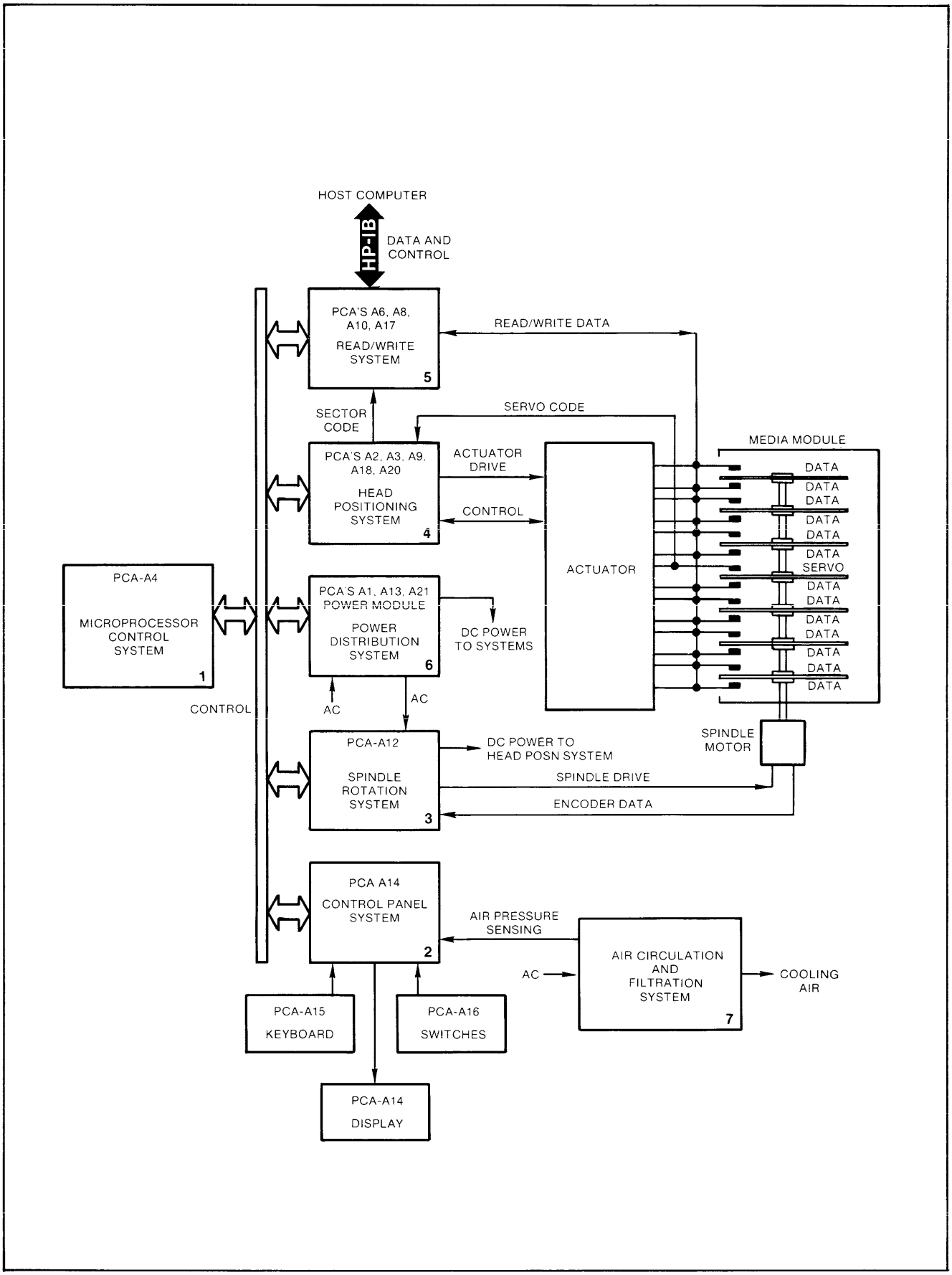
The commands can place the microprocessor in five operational categories: control operations which do not include the transfer of data between the microprocessor and the HP-IB, sense operations which determine the state of the microprocessor and the disc drive and identify the nature of any errors that may have occurred; read operations which transfer data from the disc drive to the host; write operations which transfer data from the host main storage to the disc drive; and internal self-test diagnostics. The microcode instructions for specific operations are stored in Read-Only Memory (ROM) located on PCA-A4. Refer to table 1-1 for a description of the signal mnemonics used in figure 1-15. In the "source" column of table 1-1, the numbers in parentheses following the PCA reference designations identify the functional block diagram locations of the PCA's. Communication with the read/write system and the other systems in the disc drive, with the exception of the control panel system, is via the connectors on motherboard PCA-A11. Microprocessor PCA-A4 communicates with the control panel system via a 34-conductor cable assembly (W5).

1-32. MICROPROCESSOR CPU

A Z-80A microprocessor integrated circuit is employed on PCA-A4. The Z-80A is a CPU with 158 instructions and executes programs in ROM to provide all of the control signals needed to operate the system.

1-33. COUNTER/TIMER

The counter/timer (CTC) is an integrated circuit with four separate counter channels (channels 0 through 3).



7933-303C

Figure 1-5. Disc Drive, Simplified Block Diagram

Table 1-1. Microprocessor Control System Mnemonics

MNEMONIC	DEFINITION	SOURCE	FUNCTION
A0-H thru A11-H	Address Bus, bits 0 thru 11	PCA-A4 (1)	Microprocessor address bus, bits 0 through 11.
ACTSL-L	Actuator Select	PCA-A4 (1)	Actuator driver PCA-A2 select line.
ACTTST	Actuator Test	PCA-A2 (4)	Analog test signal from actuator driver PCA-A2.
BF1SL-L	Buffer 1 Select	PCA-A4 (1)	DMA no. 1 buffer select line.
D0-H thru D7-H	Data Bus, bits 0 thru 7	PCA-A4 (1)	Microprocessor bidirectional data bus, bits 0 through 7.
DM1SL-L	DMA No. 1 Select	PCA-A4 (1)	DMA no. 1 register select.
DOPEN-H	Door Open	PCA-A14 (2)	Top door open flag.
EC1SL-L	ECC No. 1 Select	PCA-A4 (1)	DMA no. 1 ECC select line.
ER-H	Emergency Retract	PCA-A20 (4)	Emergency retract flag. Signal is active (high) when an emergency retract occurs.
FSSEL-L	Formatter/ Separator Select	PCA-A4 (1)	Formatter/separator PCA-A8 select line.
HIOA0-H thru HIOA2-H	Control Panel Address Bus, bits 0 thru 2	PCA-A4 (1)	Microprocessor control panel address bus, bits 0 through 2.
HIOD0-H thru HIOD7-H	Control Panel Data Bus bits 0 thru 7	PCA-A4/ PCA-A14 (1,2)	Control panel bidirectional data bus, bits 0 through 7.
HIODR-L	Control Panel Direction	PCA-A4 (1)	Microprocessor control panel bus direction command.

Table 1-1. Microprocessor Control System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
HIORD-L	Control Panel Read	PCA-A4 (1)	Microprocessor control panel read command.
HIOSL-L	Control Panel Select	PCA-A4 (1)	Control panel PCA-A14 select line.
HIOWR-L	Control Panel Write	PCA-A4 (1)	Control panel PCA-A14 write command.
HRST-L	Control Panel Reset	PCA-A4 (1)	Control panel PCA-A14 reset line.
IL5-L	Interlock	PCA-A4 (1)	Interlock line. (Not shown in figure 1-15.)
IL6-L	Interlock	PCA-A4 (1)	Interlock line. (Not shown in figure 1-15.)
IO1SL-L	I/O No. 1 Select	PCA-A4 (4)	DMA no. 1 PHI select line.
IP-L	Index Pulse	PCA-A9 (4)	Index timing pulse.
MBSEL-L	Motherboard Select	PCA-A4 (1)	Motherboard PCA-A11 select line.
MRST-L	Master Reset	PCA-A1 (6)	Master power-on reset line.
NMI-L	Nonmaskable Interrupt	PCA-A4 (1)	Microprocessor non-maskable interrupt.
OFTRK-H	Off-Track	PCA-A9 (4)	Off track fault flag.
PWRDN-H	Power Down	PCA-A1 (6)	Power down fault flag. Signal is active (high) for loss of regulated +12 or -12 Vdc supplies unregulated + 20 or -20 Vdc supplies, or +13 Vd supply.
RD-L	Read	PCA-A4 (1)	Microprocessor read command.
REGSL-L	Regulator Select	PCA-A4 (1)	Regulator PCA-A1 select line.

Table 1-1. Microprocessor Control System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
RWFLT-H	Read/Write Fault	PCA-A10 (5)	Read/write fault flag. Signal is active (high) for write with no dc, write with no ac, dc with no write, and multi-head fault.
RWTST	Read/Write Test	PCA-A10 (5)	Analog test signal from read/write PCA-A10.
SOS-L	Start of Sector	PCA-A9 (4)	Start of sector pulse.
SPDDN-H	Speed Down	PCA-A12 (3)	Spindle driver PCA-A12 speed down flag. Signal is active (high) when spindle speed drops.
SPDSL-L	Spindle Select	PCA-A4 (1)	Spindle driver PCA-A12 select line.
SPSPD-H	Spindle Is Is Rotating	PCA-A12 (3)	Spindle driver PCA-A12 signal indicating that spindle is rotating.
SRVSL-L	Servo Select	PCA-A4 (1)	Servo PCA-A3 select line.
SRVTST	Servo Test	PCA-A3 (4)	Analog test signal input from servo PCA-A3.
TFFLT-H	Track Follower Fault	PCA-A9 (4)	Track follower PCA-A9 fault flag. Signal is active (high) when phase-locked loop error occurs.
TFSEL-L	Track Follower Select	PCA-A4 (1)	Track follower PCA-A9 select line.
TFTST	Track Follower Test	PCA-A9 (4)	Analog test signal input from track follower PCA-A9.
WR-L	Write	PCA-A4 (1)	Microprocessor write command.
540 Hz-H	540-Hz Clock	PCA-A4 (1)	540-Hz clock signal to spindle driver PCA-A12. (Actual frequency is 538.7931 Hz.)

Table 1-1. Microprocessor Control System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
4 MHz-H	4-MHz Clock	PCA-A4 (1)	4-MHz self test signal to track follower PCA-A9.
+12 TST	+12V Test	PCA-A1 (6)	+12 Vdc test input to analog-to-digital converter. The input is a division of +12 Vdc.
-12 TST	-12V Test	PCA-A1 (6)	-12 Vdc test input to analog-to-digital converter. The input is a division of -12 Vdc.

Each channel has an eight-bit counter and, if used in a timer mode, a prescale of 16 or 256. The counters are used to count sectors on data transfers and time intervals. Channel 0 counts the 540-Hz clock and is used as a long interval counter. The input to channel 1 is the zero count output of channel 0. This allows cascading of counter channels so that channels 0 and 1 can be used as a 16-bit counter. The input to channel 2 is the zero count output of channel 1. This allows a possible 24-bit counter by cascading channels 0, 1, and 2. The input to channel 3 is the buffered Start of Sector (SOS-L) signal from track follower PCA-A9.

1-34. DATA BUS STRUCTURE

There are five separate data buses on microprocessor PCA-A4. (See figure 1-15.) The microprocessor data bus connects directly to the microprocessor CPU integrated circuit. The microprocessor data bus also connects to the counter/timer integrated circuit and three data bus buffers. The motherboard data bus is connected to the microprocessor data bus through an octal bidirectional bus driver (data bus buffer). The memory data bus is connected to all RAM and ROM on PCA-A4. The only other connections to the memory data bus is a data buffer to the microprocessor data bus and a data buffer to the control panel data bus. There is no other connection to the control panel data bus on PCA-A4 except to the memory bus. The microprocessor register data bus connects all microprocessor control registers and I/0 devices, except for the counter/timer integrated circuit, to the microprocessor data bus through a buffer.

The microprocessor register data bus connects all microprocessor registers and I/O devices, with the exception of the counter/timer, to the microprocessor data bus through a buffer. Data input to the microprocessor register data bus includes system sense lines such as Index Pulse (IP-L); and system fault lines such as Door Open (DOPEN-H), and Spindle Speed Down (SPDDN-H). A complete description of the sense and fault lines shown in figure 1-10 is provided in table 1-1. The output of the on-board analog-to-digital converter and the PCA-A4 revision data are also input to the microprocessor register data bus. Also, control data logic connected to the microprocessor register data bus transmits Control Panel Reset signal HRST-L to the control panel system.

1-35. ADDRESS BUS STRUCTURE

There are four separate address buses on microprocessor PCA-A4. The microprocessor address bus is the address bus connected to the microprocessor CPU. This bus also connects to the ROM's and to a set of buffers. The microprocessor address bus becomes the memory address bus after it is buffered. The memory address bus connects to the RAM, the memory decode and bus control logic, and to a set of transparent latches. The transparent latches provide a stable address to motherboard PCA-A11 and to the register and PCA select decode logic on PCA-A4.

The address bus beyond the transparent latches is called the motherboard Address Bus, and consists of bits 0 through 11 (A0-H through A11-H) and the latched address bus consisting of bits 4 through 7. The motherboard Address Bus connects directly to motherboard PCA-A11, and only bits 1, 2, 3, 8, and 9 connect to circuitry on PCA-A4. Bits 1, 2, and 3 are used for a self-test function. Bits 1, 2, and 3 are connected to an input register so that part of the motherboard address bus can be tested. Bits 8 and 9 of the motherboard address bus connect to a portion of the PCA select logic. The latched address bus connects to the register and PCA select decode logic only.

1-36. READ ONLY MEMORY

The Read Only Memory (ROM) block contains seven 8-kbyte by 8 ROM's for a total of 52 kbytes of code (4 kbytes are presently unused). The ROM's are 250-nanosecond devices with separate device enable and output enable lines. These separate device enable and output enable lines allow the ROM to operate with no bus contention. All of the ROM's are turned on with the device enable before it is decided which device is needed. When the decision is made, that device is selected by its output enable line.

The ROM's device enable is active only when either the microprocessor CPU device control signal (indicating a read operation) or a signal indicating an opcode fetch or an interrupt acknowledge is active. The ROM's output enable is active only when microprocessor CPU control signals indicate that a memory access operation is occurring. With this constraint, the ROM's are write protected.

1-37. RANDOM ACCESS MEMORY

The Random Access Memory (RAM) block contains a 2-kbyte by 8 static RAM. This RAM is used for temporary data storage, stack area, table area, and scratch pad area.

1-38. CONTROL SIGNAL GENERATOR

The function of the control signal generator is to buffer and synchronize the control signals from the microprocessor CPU. The control logic generator supplies the signals which control the action of all of the other circuitry on PCA-A4.

1-39. MEMORY DECODE AND BUS CONTROL LOGIC

The memory decode and bus control logic consists of two 256-byte by 4 PROM's. The memory decode PROM decodes address bits 8 through 15 to select

various hardware units (ROM element, RAM element, register and PCA select decode logic, etc.). The outputs of this PROM are used as inputs to the bus control PROM, along with address bits 5 to 7 and a control signal.

1-40. CLOCK GENERATOR

All clocks on microprocessor PCA-A4 are derived from an 8.0-MHz crystal oscillator on PCA-A4. The 8.0-MHz output is divided by two to provide a square 4.0-MHz master clock which is used to generate all of the clock signals supplied by PCA-A4. These signals include a 4-MHz clock, an inverted 4-MHz clock, a gated 4-MHz self-test clock for use by the PCA's on the motherboard, a 500-kHz clock for use by the analog-to-digital converter on PCA-A4, and a 538.7931-Hz clock (signal 540 Hz-H) for use by spindle driver PCA-A12.

The 4-MHz clock is used by the microprocessor CPU and most of the control logic on PCA-A4. The inverted 4-MHz clock is used for control logic requiring a different clock edge than the non-inverted clock. It is also used as the clock for the logic used to generate the 500-kHz clock and the 538.7931-Hz clock.

The 500 kHz is derived from the 538.7931-Hz clock logic. The 538.7931-Hz clock is obtained by dividing the 4-MHz clock signal by 256 and then by dividing that clock by 29. Since the divide by 256 is done first and by binary counters, the 500-kHz clock can be tapped off from one of the counters.

1-41. REGISTER AND PCA SELECT DECODE LOGIC

The register and PCA select decode logic is driven by bits from the memory decode and bus control logic select PROM's and by latched address bus bits. The PROM bits choose which of the on-board RAM, the DMA buffer RAM, the microprocessor registers, or the PCA selects will be active. Further decoding information is provided by the latched address bits.

The select logic is divided into two categories: I/O selects and memory-mapped selects. The memory-mapped selects are active only during a memory operation and the I/O selects are only active during an I/O operation. The only I/O selects are the two PHI selects, the control panel select, the analog-to-digital converter select, and the counter/timer select.

Selects for the two DMA PCA's are arranged so that both PCA's are accessed by the same address. Which DMA is selected is determined by a bit in the microprocessor control register. DMA PCA-A6 (primary port) is accessed when the control bit is high, otherwise DMA PCA-A5 (secondary port) is accessed.

1-42. ANALOG-TO-DIGITAL CONVERTER

An analog-to-digital converter on PCA-A4 is used to test a number of analog signals from various PCA's in the disc drive. These inputs are used for self test, limit checking, and auto head alignment. The signals input to the A/D converter are ACTTST, RWTST, SRVTST, TFTST, +12 TST, and -12 TST. Refer to table 1-1 for a description of these signals. The analog-to-digital converter takes an input from an analog multiplexer and performs a conversion on the signal. The sequence of operation for the A/D converter consists of setting up the multiplexer in the control register and waiting for the multiplexer to settle, writing to the A/D converter to start the conversion, waiting for the conversion to finish, and then reading the data via the microprocessor register data bus.

1-43. MICROPROCESSOR INTERFACE

Communication between the microprocessor and the PCA's in the disc drive is achieved via the bidirectional three-state motherboard Data bus (D0-H through D7-H). Together with this Data bus, a Read command (RD-L) and a Write command (WR-L) are also bused to the PCA's. In addition, an individual select line is sent to each PCA. The PCA select lines include BF1SL-L, DM1SL-L, ECC1SL-L, FSSEL-L, HIOSL-L, IOSL-L, MBSEL-L, REGSL-L, SPDSL-L, SRVSL-L, and TFSEL-L. The function of each one of these signals is described in table 1-1. Only one PCA select line is active (low) at any one time. If the Write command (WR-L) is active (low) at the same time that a PCA select line is active (low), data will be transferred from the microprocessor to the selected PCA. Conversely, if the Read command (RD-L) is low at the same time that a PCA select line is low, data is transferred from the selected PCA to the microprocessor. It should be noted that the Read (RD-L) and Write (WR-L) signals do not refer to the read and write operations of the disc drive.

1-44. CONTROL PANEL SYSTEM

The control panel system (see figure 1-16) consists of control panel PCA-A14, data input PCA-A15, and load/unload PCA-A16. Included on the PCA's are front panel switches, an eight-character alphanumeric display panel, an activity indicator, and a keyboard. Also included in the control panel system is an air pressure sensor, a top door latch sensor, and a top door latch solenoid (on the HP 7935 only). Control panel PCA-A14 is mounted on the operator control panel of the disc drive cabinet and is connected to microprocessor PCA-A4 in the card cage via a 34-conductor ribbon cable. Data input PCA-A15 and load/unload PCA-A16 are subassemblies of PCA-A14.

The purpose of the control panel system is to accept inputs from an operator through the keyboard and

switches, display the active state of the disc drive on the activity indicator, display disc drive status messages, unlock the top door of the disc drive (on the HP 7935 only), and provide an interface to the microprocessor for the signals generated by the sensors. Included in the following paragraphs are circuit descriptions of the top door latch solenoid drive, the LOAD/UNLOAD and UNLOCK DOOR switches, the activity indicator, and the display panel. Refer to table 1-2 for a description of the signal mnemonics used in figure 1-16. In the "source column" of table 1-2, the numbers in parentheses following the PCA reference designations identify the functional block diagram locations of the PCA's.

1-44A. TOP DOOR LATCH SOLENOID DRIVER (HP 7935 ONLY)

Part of the control panel PCA-A14 circuitry is the top door latch solenoid driver which, under microprocessor control, operates the solenoid controlling the top door latch. The driver uses a switching technique that is triggered by microprocessor PCA-A4 to discharge energy stored in capacitors into the top door latch solenoid. Bit 0 (HIOD0-H) of the control panel data bus, Unlock Door (UD-L), and Spindle Is Spinning (SPSPD-H) are inputs to the top door latch solenoid driver. Signals SOL+ and SOL- are the driver outputs to the solenoid. The driver is disabled after it detects that the top door is open. The top door sensor returns a Door Open (DOPEN-L) flag directly to microprocessor PCA-A4. The solenoid driver outputs a Door Open Flip-Flop (DOFF-H) signal to the microprocessor interface for self-test purposes. Signal Top Door Sensor Interlock (TDSI-L) is returned to the microprocessor interface to allow the microprocessor to check that the sensor is correctly attached to connector J4 on PCA-A14.

1-45. LOAD/UNLOAD PCA-A16

The operator control panel LOAD/UNLOAD switch and the UNLOCK DOOR switch (on the HP 7935 only) is mounted on load/unload PCA-A16. The output lines from the LOAD/UNLOAD switch are connected to the load/unload flip-flop on PCA-A14. The flip-flop output is Load signal (LD-L) to the microprocessor interface. When LD-L is active (low), the LOAD/UNLOAD switch is in the LOAD position; when the LD-L is inactive (high), the switch is in the UNLOAD position. The front panel UNLOCK DOOR switch is also mounted on PCA-A16. This switch is connected to the keyboard scan circuitry on data input PCA-A15.

1-46. DATA INPUT PCA-A15

Data input PCA-A15 contains a row-column encoded keyboard that is used to input commands to the disc drive. The keyboard/display interface integrated circuit described in paragraph 1-49 has all the circuitry needed for scanning the keyboard. Digit selection is accomplished by decoding the keyboard scan lines of the keyboard/display integrated circuit. The active-low output lines from the scan line decoder are used for keyboard scan. These lines are also used as digit select lines. The UNLOCK DOOR switch (on the HP 7935 only), mounted on PCA-A16, is also connected to this scan circuitry.

1-47. ACTIVITY INDICATOR AND DRIVER

The activity indicator informs the operator when the disc drive is performing a programmed function. The activity indicator is a light-emitting diode (LED) located adjacent to the eight-character display and is controlled by the activity indicator driver. The driver inputs are bit 0 of the microprocessor Control Panel Data Bus (HIOD0-H), the Activity LED (ACTIVE LED) select signal, and the HIO Reset signal (HRST-L).

1-48. SENSORS

The sensor circuitry is used to detect when the disc drive top door is open and the presence of cooling air flow. The state of the top door (open or closed) is detected by a Hall-effect sensor. The output of the top door open sensor is connected directly to control panel PCA-A14 and is reported to the microprocessor. A pressure-sensitive switch senses the air pressure in the absolute filter. Output from the absolute filter pressure-sensitive switch (S1) is connected to control panel PCA-A14 and is reported to the microprocessor.

The two sensor output lines to the control panel PCA-A14 microprocessor interface are: Top Door Open (DO-H) and Filter (FLTR-L). Refer to table 1-2 for further details.

1-49. KEYBOARD/DISPLAY INTERFACE

The keyboard/display interface circuit provides the operator with an eight-character alphanumeric display on which messages appear regarding the active state of the disc drive and its current operating condition, and a keyboard for command entries. The keyboard/display interface circuit consists of large- and medium-scale integrated circuits including a keyboard/display interface, an ASCII-to-18-segment display driver, a scan line decoder, a display segment driver, a digit driver, and an eight-character 18-segment LED display module. The keyboard/display interface integrated circuit has an internal 16 by 8 display buffer that allows storage of the eight characters needed for the control panel display. Since the display employs 18-segment characters, the ASCII-to-18-segment display driver is used for this function. The keyboard/display interface has eight data lines from the internal buffer to the display driver. Only the low order six bits are used because the display driver can only dis-

Table 1-2. Control Panel System Mnemonics

MNEMONIC	DEFINITION	SOURCE	FUNCTION
ACTIVE LED	Activity LED	PCA-A14 (2)	Address decoder output to activity indicator driver.
DO-H	Top Door Open	PCA-A14 (2)	Microprocessor interface input from top door closed sensor. Signal is inactive (low) when top door is closed.
DOFF-H	Door Open Flip-Flop	PCA-A14 (2)	Microprocessor interface input from the top door latch solenoid driver circuit.
DOPEN-H	Top Door Open	PCA-A14 (2)	Top door open flag returned directly to microprocessor PCA-A4. Signal prevents spin up of spindle motor when top door is open.
FLTR-L	Filter	PCA-A19 (2)	Microprocessor interface input from absolute filter air pressure sensor. Signal is active (low) when absolute filter is in good condition.
HIOA0-H thru HIOA2-H	Control Panel Address Bus, bits 0 thru 2	PCA-A4 (1)	Microprocessor control panel address bus, bits 0 through 2.
HIOD0-H thru HIOD7-H	Control Panel Data Bus, bits 0 thru 7	PCA-A4 (1)	Microprocessor control panel bidirectional data bus, bits 0 through 7.
HIODR-L	Control Panel Direction	PCA-A4 (1)	Microprocessor control panel bus direction command.
HIORD-L	Control Panel Read	PCA-A4 (1)	Microprocessor control panel read command.
HIOSL-L	Control Panel Select	PCA-A4 (1)	Microprocessor control panel select line.
HIOWR-L	Control Panel Write	PCA-A4 (1)	Microprocessor control panel write command.
HRST-L	Control Panel Reset	PCA-A4 (1)	Microprocessor control panel reset line.
LD-L	Load/Unload	PCA-A14 (2)	Microprocesor interface input from LOAD/UNLOAD switch circuit. When active (low), it indicates that switch is in LOAD position.

Table 1-2. Control Panel System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
MRST-L	Master Reset	PCA-A1 (6)	Master power on reset line.
SENS-L	Sensor	Media Module Chamber (2)	Output of sensor sensing condition of top door on disc drive. Signal is active (low) when door is closed.
SIL-L	Sensor Interlock	PCA-A19 (2)	Microprocessor interface input. When active (low), it indicates that module detect PCA-A19 is connected to Control Panel PCA-A14.
SOL+, SOL-	Solenoid +, -	PCA-A14 (2)	Top door latch solenoid driver output to top door latch solenoid.
SPSPD-H	Spindle Is Spinning	PCA-A12 (3)	Microprocessor interface input. When active (high) it indicates that spindle motor is spinning.
TDSI-L	Top Door Sensor Interlock	PCA-A14 (2)	Microprocesor interface input. When active (low), it indicates that top door sensor cable is in place.
UD-L	Unlock Door	PCA-A14	Address decoder output to the top door latch solenoid driver circuit.

play 64 characters. The resulting 18-segment data is used to drive the display through current limiting resistors. The display characters are selected by decoding the three low order bits of the scan lines from the display interface circuit. The decoded digit number is used to pull the cathodes of one character low thus enabling the segments for the digit.

The keyboard is connected to the keyboard/display interface as described in paragraph 1-46.

1-50. ADDRESS DECODER

The address decoder permits the microprocessor to address all the functions of the control panel. The decoder consists of two 2-to-4 line decoders. The "A" and "B" inputs are control panel address bus, bits 1 and 2 (HIOA1-H and HIOA2-H). The enable for the read address decoder is a logical "AND" of Control Panel Select (HIOSL-L) and Control Panel Read (HIORD-L). Similarly, the enable for the write address decoder is a logical "AND" of Control Panel Write (HIOWR-L) and Control Panel Select (HIOSL-L). This decoding scheme provides four read and four write addresses. Control Panel Address bit 0 (HIOA0-H) is not used for address decoding. This means that two consecutive microprocessor addresses enable the same decoder output lines.

The keyboard/display integrated circuit requires two addresses: one for commands and one for data. It also needs to read and write from both of these addresses. This is the reason that the address decoder generates one output for two addresses.

1-51. MICROPROCESSOR INTERFACE

The microprocessor interface consists of a number of registers that allow the microprocessor to sample the sensor detector outputs, the PCA artwork and revision register, and various self-test signals. For each register the output control signal is the appropriate select signal from the address decoder. These registers are used in pairs since each has only four output bits. The select signal for the registers is HIOA0-H. In this way, the register chooses which nibble to output depending on bit 0 of the address.

Signals that the microprocessor writes to PCA-A14 for the purpose of controlling the control panel circuitry include: Master Reset (MRST-L), Control Panel Data Bus, bit 0 (HIOD0-H), and Control Panel Reset (HRST-L).

Signals read by the microprocessor from PCA-A14 include: Load/Unload (LD-L), Top Door Open (DO-H), Filter (FLTR-L), Sensor Interlock (SIL-L), and Top Door Sensor Interlock (TDSI-L). Refer to table 1-2 for a description of the microprocessor interface output and input signals listed above.

1-52. SPINDLE ROTATION SYSTEM

The spindle rotation system (see figure 1-17) consists of circuits on spindle driver PCA-A12, located in the power module, and connected by cables to motherboard PCA-A11 and spindle motor B2. The primary purpose of the spindle rotation system is to provide power to the spindle motor and maintain its speed at 2,694 (2,700 nominal) revolutions per minute. The spindle rotation system also supplies dc power to actuator driver PCA-A2 and emergency retract PCA-A20 in the head positioning system. In addition, the spindle rotation system provides an interface to microprocessor PCA-A4, allowing the microprocessor to control and monitor operation of the spindle motor rotation system for both normal and self-test conditions. The following paragraphs provide a description of the components shown in figure 1-17, followed by system operating details. Refer to table 1-3 for a description of the signal mnemonics used in figure 1-17. In the source column of table 1-3, the numbers in parentheses following the PCA reference designations identify the functional block diagram locations of the PCA's.

1-53. SPINDLE MOTOR

Spindle motor B2 is a six-pole, two-phase brushless dc motor which develops a one-quarter horsepower output. Current is switched to the windings in a prescribed manner by a spindle phase encoder circuit that derives shaft position information from two Hall-effect sensors mounted on the stator of the spindle motor. To turn the motor, it is necessary to switch the current in the windings 12 times per revolution of the shaft in a pattern that repeats every 120 degrees of a revolution. This pattern is illustrated in figure 1-6. Note that the current in each winding alternates between a positive polarity and a negative polarity.

The polarity and relative timing between the two motor currents determine the direction in which the motor rotates; that is, reversing the polarity of the currents shown in figure 1-6 will reverse the direction in which the motor rotates. The magnitude of the torque that the motor develops is directly proportional to the magnitude of the current in the windings. By sensing the rotational speed of the motor and using this information to control the magnitude of the current in the windings, the motor can be made to turn at a constant speed for large variations of the load on the shaft.

1-54. SPINDLE PHASE DECODER

The spindle phase decoder takes the position information from the spindle motor encoders (Hall-effect sensors) and directs current of the correct polarity into the proper motor windings in order to turn the motor. Microprocessor control of motor spin up and spin down is also achieved by the spindle phase decoder.

Position sensing of the motor shaft is performed by the two Hall-effect sensors mounted in the stator of the spindle motor. Hall-effect sensors are latching devices, that is, they sense a threshold magnetic field in one direction, switch output state, and then retain that state until a threshold magnetic field in the opposite direction causes the state to change again. The sensors detect the magnetic fields from magnets attached to the motor shaft. The sensors are arranged to detect a radial magnetic field between the magnets and the pole pieces of the stator. The 30-degree spacing of the magnets on the shaft causes the two sensors to switch in a 2-bit Gray code. This 2-bit code has four states which are decoded to control switching the motor currents as shown in figure 1-6. The encoder signals from the motor are labelled ENCA and ENCB. After buffering and gating with self-test encoder signals from the microprocessor, the signals are labelled ENCODER A and ENCODER B.

The position information from the spindle phase decoder is combined with the torque information from the motor speed control loop in an analog switch for transmission to the power amplifiers.

Microprocessor control of spindle motor spin up and spin down is performed by signals Run (RUN-H) and Spindle Stopped (SPSTOP-H). The operation of these signals is discussed in paragraph 1-66.

1-55. MOTOR SPEED CONTROL LOOP

The motor speed control loop controls the speed of the spindle motor by comparing the phase of the edges of

Table 1-3. Spindle Rotation System Mnemonics

MNEMONIC	DEFINITION	SOURCE	FUNCTION
A0-H,A1-H	Address Bus, bits 0 and 1	PCA-A4 (1)	Microprocessor address bus, bits 0 and 1.
+ASUPTST-H	Actuator Positive Supply Test	PCA-A12 (3)	Microprocessor interface input from power supply detector sensing level of unregulated +36Vdc (+LMSUPP) output to actuator driver PCA-A2 in head positioning system. An inactive (low) signal indicates that voltage is less than +25 Vdc.
-ASUPTST-H	Actuator Negative Supply	PCA-A12 (3)	Microprocessor interface input from power supply detector sensing level of unregulated -36 Vdc (-LMSUPP) output to actuator driver PCA-A2 in head positioning system. An inactive (low) signal indicates that voltage is less that -25 Vdc.
CLEAR-L	Clear	PCA-A12 (3)	Microprocessor interface output that clears signal SPDDN-H.
1+CURR-H	Current Sense, Phase 1 Positive	PCA-A12 (3)	Microprocessor interface input from current detector in positive output of spindle motor phase 1 power amplifier.
1-CURR-H	Current Sense, Phase 1 Negative	PCA-A12 (3)	Microprocessor interface input from current detector in negative output of spindle motor phase 1 power amplifier.
2+CURR-H	Current Sense, Phase 2 Positive	PCA-A12 (3)	Microprocessor interface input from current detector in positive output of spindle motor phase 2 power amplifier.
2-CURR-H	Current Sense, Phase 2 Negative	PCA-A12 (3)	Microprocessor interface input from current detector in Negative output of spindle motor phase 2 power amplifier.
D0-H thru D7-H	Data Bus, bits 0 thru 7	PCA-A4 (1)	Microprocessor bidirectional data bus, bits 0 through 7.

Table 1-3. Spindle Rotation System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
DOPEN-H	Door Open	PCA-A4 (1)	Microprocessor signal indicating that top door of the disc drive is open. When DOPEN-H is active (high), spindle motor power amplifiers are disabled.
+EMRSUPP	Emergency Retract Positive Supply Voltage	PCA-A12 (3)	Unregulated +36 Vdc supplied by PCA-A12 to the emergency retract circuits on actuator driver PCA-A2 and emergency retract PCA-A20 in the head positioning system.
-EMRSUPP	Emergency Retract Positive Supply Voltage	PCA-A12 (3)	Unregulated -36 Vdc supplied to the emergency retract circuits on actuator driver PCA-A2 and emergency retract PCA-A20 in the head positioning system.
ENABLE-L	Enable	PCA-A12 (3)	Microprocessor interface output to phase 1 and phase 2 power amplifiers. Signal is returned to microprocessor for self-test purposes.
ENCA	Encoder A	Spindle Motor (3)	Output of Hall-effect sensor A on spindle motor. Signal is used to control spindle motor speed and is also input to microprocessor interface.
ENCB	Encoder B	Spindle Motor (3)	Output of Hall-effect sensor B on spindle motor. Signal is used to control spindle motor speed and is also input to microprocessor interface.
ENCODER A	Encoder A	PCA-A12 (3)	Buffered ENCA signal or microprocessor simulated encoder A signal.
ENCODER B	Encoder B	PCA-A12 (3)	Buffered ENCB signal or microprocessor simulated encoder B signal.
INTLK1	Interlock	PCA-A12 (3)	Interlock chain. Spindle motor power amplifiers are disabled when INTLK1 is active (high).

Table 1-3. Spindle Rotation System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
INTLK-H	Interlock	PCA-A12 (3)	Microprocessor interface input informing microprocessor that cable between PCA-A12 and the spindle motor is correctly connected.
+LMSUPP	Actuator Positive Supply Voltage	PCA-A12 (3)	Unregulated +36 Vdc supplied by PCA-A12 to actuator driver PCA-A2 in the head positioning system.
-LMSUPP	Actuator Positive Supply Voltage	PCA-A12 (3)	Unregulated -36 Vdc supplied by PCA-A12 to actuator driver PCA-A2 in the head positioning system.
MRST-L	Master Reset	PCA-A1 (6)	Master Reset signal originating in power regulator PCA-A1. Signal resets the disc drive circuitry at power turn on.
PHASE ERROR	Phase Error	PCA-A12 (3)	Output of phase/frequency detector in motor speed control loop. Signal is also input to microprocessor interface for self test purposes.
PH1OUT-H	Phase 1 Output	PCA-A12 (3)	Phase 1 power amplifier positive output to spindle motor.
PH1RET-H	Phase 1 Return	PCA-A12 (3)	Phase 1 power amplifier negative output to spindle motor.
PH2OUT-H	Phase 2 Output	PCA-A12 (3)	Phase 2 power amplifier positive output to spindle motor.
PH2RET-H	Phase 2 Return	PCA-A12 (3)	Phase 2 power amplifier negative output to spindle motor.
RD-L	Read	PCA-A4 (1)	Microprocessor read command to microprocessor interface logic on PCA-A12.
RUN-H	Run	PCA-A12 (3)	Microprocessor interface output to spindle phase encoder. State of RUN-H is also sensed by microprocessor for control purposes.

Table 1-3. Spindle Rotation System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
SCC+, SCC-	Spindle Current Command, + and -	PCA-A12 (3)	Zero to +5 Vdc and zero to -5 Vdc, respectively, output by spindle current command generator to drive current into the spindle motor to control its speed. Zero volts equals no current and 5 volts equals approximately 12 amperes into the motor. Torque information from the phase detector and position information from the spindle phase decoder are combined in an analog switch so that they can be amplified by the two spindle motor power amplifiers.
SPDDN-H	Speed Down	PCA-A12 (3)	A flag signal sent directly to microprocessor PCA-A4 and emergency retract PCA-A20 in the head positioning system warning that some fault has developed in PCA-A12 to cause the spindle motor to lose phase locked speed. SPDDN-H remains active (high) until it is cleared by the microprocessor or Master Reset (MRST-L).
SPDSL-L	Spindle Driver Select	PCA-A4 (1)	Spindle driver PCA-A12 select line from microprocessor. SPDSL-L is active (low) when microprocessor is addressing PCA-A12.
SPDUP-L	Speed Up	PCA-A12 (3)	Microprocessor interface input from spindle speed up detector indicating that the spindle motor has reached its operational speed of 2700 rpm (nominal).
SPSPD-H	Spindle Is Rotating	PCA-A12 (3)	A flag signal sent directly to microprocessor PCA-A4 indicating that the spindle motor is rotating.
SPSTOP-H	Spindle Stopped	PCA-A12 (3)	Microprocessor interface input from spindle phase decoder informing microprocessor that spindle motor is stopped.

Table 1-3. Spindle Rotation System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
+SSUPTST-H	Spindle Driver Positive Supply Voltage Test	PCA-A12 (3)	Microprocessor interface input from power supply detector sensing output level of unregulated +36 Vdc supply on PCA-A12. An inactive (low) signal indicates that voltage is less than +25 Vdc.
-SSUPTST-H	Spindle Driver Positive Supply Voltage Test	PCA-A12 (3)	Microprocessor interface input from power supply detector sensing output level of unregulated -36 Vdc supply on PCA-A12. An inactive (low) signal indicates that voltage is less than -25 Vdc.
TEMP-H	Temperature	PCA-A12 (3)	Microprocessor interface input from thermal switch on PCA-A12 heat sink. If the disc drive blower fails or the airflow path to the heat sink becomes blocked, the temperature will rise and cause the thermal switch to open. This disables the spindle motor power amplifiers. If the spindle had been spinning, SPDDN-H will become active (high).
WR-L	Write	PCA-A4 (1)	Microprocessor write command to microprocessor interface logic on PCA-A12.
540 Hz-L	540-Hz Clock	PCA-A4 (1)	A reference clock used to control the spindle motor speed. The clock is generated on microprocessor PCA-A4 from the 4-MHz master clock. The clock has a frequency of 538.79 Hz, assuming that the master clock oscillator is exactly 4.00000 MHz. This gives a spindle speed of 2,693.95 rpm, a negligible difference from the specified 2,700 rpm.
180 Hz-H	180-Hz Clock	PCA-A12 (3)	Internal 180-Hz clock signal used to limit the duty cycle of the spindle motor amplifiers to one-third when the spindle motor is turning slowly. Signal is also input to microprocessor interface.

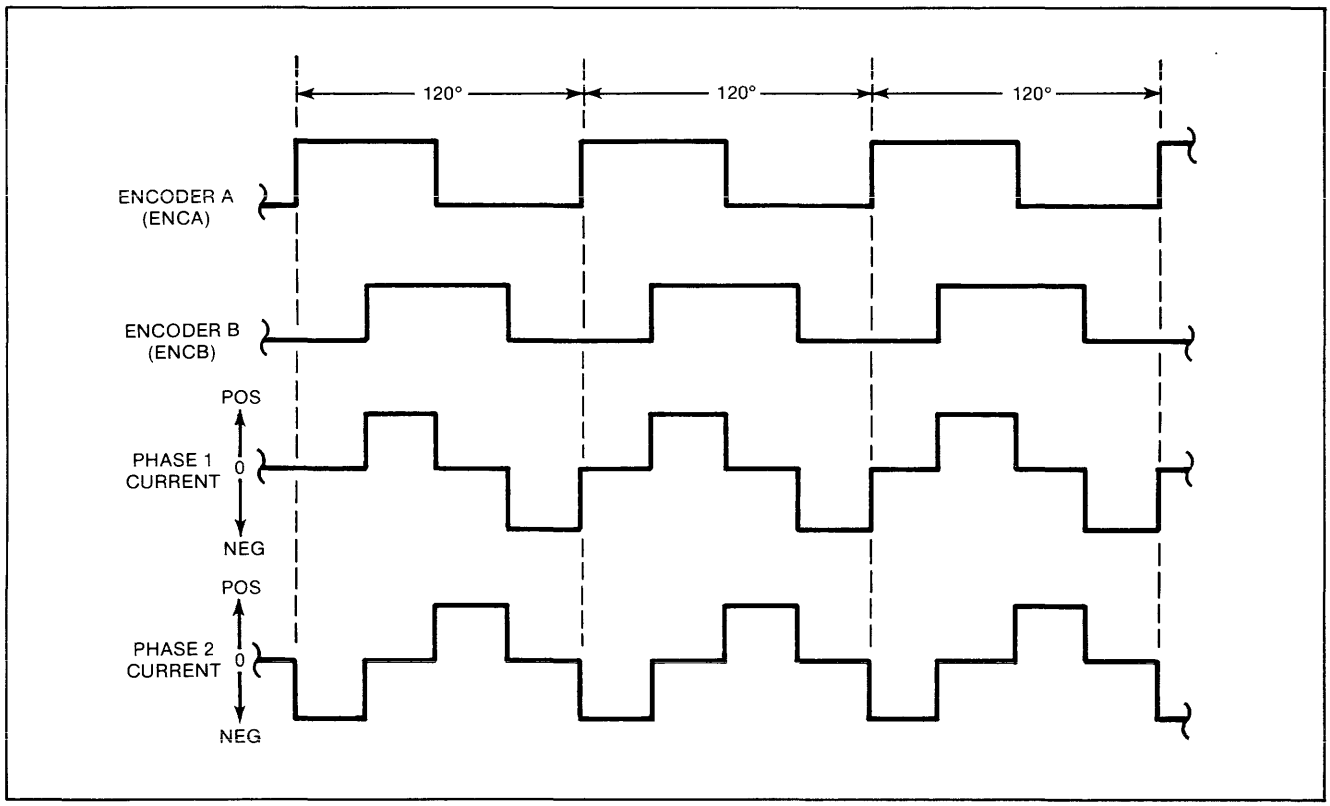


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Figure 1-6. Phase Selection Timing

motor encoder signals ENCODER A and ENCODER B to a crystal-controlled reference clock and driving a current into the motor windings proportional to the phase difference between the signals. Included in the control loop are a reference clock pulse generator, an encoder clock pulse generator, a phase detector, and a spindle current command generator. To prevent damage to the power amplifiers during acceleration and deceleration of the motor, the control loop also includes a current limiting feature. The current limiting circuitry includes a 180-Hz generator and a spindle current limiter. Also, in order to inform the microprocessor and other operating systems in the disc drive of the status of spindle motor rotation, a speedup detector is included in the control loop.

1-56. REFERENCE CLOCK PULSE GENERATOR. The clock pulses which the motor speed control loop phase detector (phase lock loop) uses to control the speed of the spindle motor are generated on microprocessor PCA-A4. The input to the reference clock pulse generator is signal 540 Hz-H, a square wave with a frequency of 538.79 Hz, assuming that the microprocessor master clock generator has a frequency of 4.0000 MHz. The reference clock pulse generator is a dual one-shot that provides two pulses for every rising edge of the reference clock input signal.

1-57. ENCODER CLOCK PULSE GENERATOR. The encoder clock pulse generator produces a clock pulse each time spindle motor encoder signal ENCODER A or ENCODER B changes state. The generator also outputs a flag signal, labelled Spindle Is Rotating (SPSPD-H). This signal is transmitted to control panel PCA-14 via microprocessor PCA-A4 where it is used to prevent the top door from being opened when the spindle motor is rotating.

1-58. PHASE DETECTOR. The phase detector is a phase/frequency detector. The output of the detector is an indication of the phase difference of the reference clock pulses and the encoder clock pulses and is also an indication of their relative frequency. When the reference clock is higher in frequency than the encoder clock (as during spin up), the output of the phase detector is at a high level. Conversely, when the encoder clock is higher in frequency, the phase detector output is low. When the two clocks are at the same frequency (spindle speed is phase locked), the output is a pulse with a duration directly proportional to the phase difference. The variable pulse width PHASE ERROR signal output from the detector is coupled to the input of the spindle current command generator. Signal PHASE ERROR is also input to the microprocessor interface for self-test purposes.

1-59. SPINDLE CURRENT COMMAND GENERATOR. The spindle current command generator supplies the signals that the motor speed control loop generates to drive current into the power amplifiers to control motor torque. Spindle Current Command signals SCC+ and SCC- can vary from zero to +5 Vdc

and zero to -5 Vdc, respectively. Zero volts equals no current in the motor and 5 Vdc equals approximately 12 amperes into the motor. An analog switch combines the torque information from the motor speed control loop with the position information from the spindle phase decoder so that it can be amplified by the power amplifiers.

1-60. SPINDLE CURRENT LIMITER. The spindle current limiter protects the power amplifiers from overload when the spindle motor is accelerating or decelerating.

When the spindle motor is turning slowly, it is possible for the output transistors in the power amplifiers to overheat due to the extended time that each transistor is turned on. To prevent this possibility, the spindle phase decoder is disabled by a 180-Hz generator that limits the duty cycle of the power amplifiers to one-third. Slow speed is sensed by monitoring the output of the encoder clock pulse generator. Whenever the time interval between encoder clock pulses is more than 10.6 milliseconds, corresponding to a motor speed of 470 rpm, the output of the 180-Hz generator is gated through to the spindle phase decoder. This signal, labelled duty cycle limit, disables the outputs of the spindle phase decoder and shuts off the power amplifiers.

When the spindle motor is spinning down, the spindle driver exerts a braking force by trying to spin the motor backwards. During the time that the motor is being decelerated, the voltage applied to the motor by the power amplifiers is out of phase with the back emf of the motor. The combination of this voltage and the 12 amperes of current that the amplifiers can deliver could cause equipment failure. To prevent this, the spindle current limiter limits signals SCC+ and SCC- to approximately 1.5 Vdc at spin down.

1-61. 180-HZ GENERATOR. The 180-Hz generator divides reference clock signal 540 Hz-H by three and supplies a 180-Hz signal to the spindle current limiting circuitry described in the previous paragraph. The 180-Hz output is also input to the microprocessor interface for self-test purposes.

1-62. POWER AMPLIFIERS

The spindle driver power amplifiers are transconductance amplifiers that convert the spindle current command generator output voltages (SCC+ and SCC-) into motor drive currents. The circuits for the phase 1 and phase 2 power amplifiers are identical. Each amplifier has phase plus and phase minus current detectors that allow the microprocessor to test the operation of the amplifiers. Enable signal ENABLE-L, input to the amplifiers from the microprocessor interface, is also used for self-test purposes.

1-63. POWER SUPPLIES

Spindle driver PCA-A12 contains a ±36 Vdc unregulated supply that provides operating power for the spindle rotation system and the head positioning system. The ±36 Vdc unregulated outputs are derived from a bridge rectifier circuit connected via fuses F510 and F520 to a secondary winding on power transformer T1. The ±36 Vdc output voltages are connected to the spindle rotation system circuits via fuses F590 and F580 and to the head positioning system via fuses F540 and F550. The ±36 Vdc outputs are also connected to the emergency retract circuit in the head positioning system via fuses F560 and F570. These eight fuses are located on PCA-A12 and are only accessible when the power module is fully extended on its rack slides.

The ±12 Vdc regulated outputs are obtained from voltage regulators powered by the ±36 Vdc supply. These ±12 Vdc regulated outputs are separate from the ±12 Vdc supply lines in the card cage. This isolation prevents the noise generated on PCA-A12 from being coupled into the noise-sensitive read/write and head positioning systems. In addition to not being connected directly to the ±12 Vdc supplies in the card cage, the ±12 Vdc regulated supplies on PCA-A12 employ the PCA-A12 ±36 Vdc supply ground. This prevents ground noise from being introduced into the card cage.

1-64. ACTUATOR ASSEMBLY EMERGENCY RETRACT POWER

The power required for an emergency retract of the actuator assembly in the head positioning system is available from three sources on spindle driver PCA-A12. Under normal circumstances, with the disc drive connected to an ac power source and the ~ LINE circuit breaker on, the energy for emergency retract will come from the ±36 Vdc supplies on PCA-A12. In addition to the dc supplies, the spindle motor itself will act as a generator which can supply energy to the ±36 volt supplies and provide enough power to retract the heads. Each of the motor windings acts as an ac voltage source with a voltage equal to the back emf of the motor for whatever speed that it is spinning. Diodes rectify the ac motor voltage so that if the peak value of the back emf is larger than the dc voltage on the power supplies, then the motor will force current into the supplies.

1-65. MICROPROCESSOR INTERFACE

The microprocessor interface consists of four registers that microprocessor PCA-A4 uses to communicate with PCA-A12. All four registers are used to read information from PCA-A12 regarding status and self test. Two of the registers can be written to for the purpose of controlling the action of the spindle motor and for clearing certain faults that can occur on PCA-A12.

Refer to table 1-3 for a description of the microprocessor interface input and output signals shown in figure 1-17.

1-66. SPIN UP AND SPIN DOWN

To spin up the spindle motor requires that the power amplifiers be enabled and the motor speed control loop is set to the run mode. To achieve this, the microprocessor activates Run/Stop (RUN-H), Enable Spindle (ENABLE-L) and ENCODER A and ENCODER B. This sets the motor speed control loop in a run mode, with the power amplifiers and spindle phase encoder enabled. Following this, the microprocessor checks the state of the run mode and amplifier lines and Speed Up signal (SPDUP-L). When SPDUP-L becomes active (low), it indicates that the spindle is rotating at the proper speed. Following power-on, the microprocessor senses, via the Speed Up (SPDUP-L) signal line to the microprocessor interface, the spin-up time of the spindle motor to determine whether or not the disc drive has a media module installed. If the spin-up time of the drive is too short, a NOMODULE message will be displayed at the front panel.

To spin down the spindle motor and brake it to a halt, the microprocessor sets Run/Stop (RUN-H) low. To spin down the motor and let it coast to a halt, the microprocessor sets both RUN-H and Enable (ENABLE-H) low. Signal Spindle Stopped (SPSTOP-H) from the spindle phase decoder informs the microprocessor when the spindle has stopped.

1-67. FAULT DETECTION

Spindle driver PCA-A12 contains fault detection circuitry that alerts microprocessor PCA-A4 and other PCA's in the disc drive to the occurrence of a failure in the spindle rotation system and the need to initiate emergency action.

If the spindle motor has been running and a fault develops that causes the motor to lose phase-locked speed, Speed Down flag (SPDDN-H) from the speedup detector will latch high. This flag alerts the microprocessor and the emergency retract circuit in the head positioning system to take appropriate action. Signal SPDDN-H will remain latched until it is cleared by a Clear (CLEAR-L) from the microprocessor interface.

In the event that the spindle motor cable connector is detached or incorrectly attached to PCA-A12, the power amplifiers will not be enabled and the motor will not turn.

If the disc drive air circulation system fails or the airflow path to the heat sink on spindle driver PCA-A12 becomes obstructed, a thermal switch on the heat sink will open and cause signal TEMP-H to disable the power amplifiers. If the spindle is spinning, Speed Down flag (SPDDN-H) will also be activated.

1-68. SELF TEST

Spindle driver PCA-A12 contains a number of circuits that permit the microprocessor to determine if the spindle rotation system is operating correctly. For this purpose, the microprocessor can effectively disconnect spindle motor Encoder signals ENCA and ENCB and substitute its own encoder signals. Several circuits can be tested with these substituted encoder signals. This includes testing the output status of the power amplifiers, testing for motor rotation, testing for proper operation of the spindle phase detector, speed-up detector, and spindle current command generator. The ±36 Vdc supplies to the spindle rotation and head positioning systems can also be tested by the microprocessor.

The power amplifiers are tested one at a time by substituting encoder signals and sensing the outputs of the power amplifiers via the phase current detector outputs. The microprocessor can determine with a series of encoder signals if the correct amplifier stages turn on.

While the amplifier output stages are being tested, the spindle will rotate 1/12 of a revolution each time current is driven into a different stage. The microprocessor can read the spindle motor encoder signals to determine if the spindle shaft has moved the correct amount when current is driven into the motor.

Operation of the phase detector is tested by the microprocessor reading the reference clock and substituting a changing encoder signal through the microprocessor interface. The phase detector can be read when the frequency of the substituted encoder is equal to the reference frequency. If the phase locked condition is maintained for more than 1.3 seconds, Speed Up signal SPDUP-L will go low.

The microprocessor checks the condition of the fuses in the ±36 Vdc outputs to the spindle driver and the head positioning system by checking the outputs of the power supply detectors connected to these lines.

1-69. HEAD POSITIONING SYSTEM

The head positioning system (see figure 1-18) consists of circuits on actuator driver PCA-A2, servo PCA-A3, track follower PCA-A9, actuator status PCA-A18, and emergency retract PCA-A20 (a part of PCA-A2). Also included are such electromechanical components as the actuator assembly, carriage latch solenoid, temperature sensors, and velocity transducer (tachometer).

The purpose of the head positioning system is to control, following microprocessor instructions, the application of power to the coil of the linear motor in the actuator assembly. This causes the heads to be accurately positioned over a specified cylinder during an initial head load, forward or reverse seek, or recalibration. In addition, the head positioning system provides the means to retract the heads under emergency and normal conditions and to control track following, including automatic head alignment.

Provided in the following paragraphs is a description of the system circuitry contained on the five printed-circuit assemblies, followed by a discussion of system operation. The operations described include head loading, head unloading, seek, recalibrate, track following, and emergency retract. Refer to table 1-4 for a description of the mnemonics used in figure 1-18. In the "source" column of table 1-4, the numbers in parentheses following the PCA reference designations identify the functional block diagram locations of the PCA's.

1-70. TRACK FOLLOWER PCA-A9

Track follower PCA-A9 amplifies and conditions the output signal from the servo head to a usable level and from this amplified signal extracts radial (cylinder) position information for the servo loop in the head positioning system. The amplified signal is also used to extract circumferential timing information required by the read/write system for sector placement. The track follower also provides the microprocessor with a signal that indicates when the servo head is over the servo surface.

The radial position and sector information is derived from servo code magnetically recorded on the servo surface. (See figure 1-7.) The servo code consists of a combination of plus odd and plus even dibits. There are 1,338 concentric servo bands alternating between plus odd and plus even bands on the servo surface. In addition, each servo band has 93 index patterns encoded on it from which start of sector information is derived. There are also servo guard bands on the servo surface that contain information that informs the disc drive electronics of the servo code direction. The guard bands also supply automatic gain control (AGC) and phase locked loop (PLL) information so that initialization and stabilization of the head positioning system can occur prior to track zero. The following paragraphs describe the functions of the track follower PCA-A9 circuit blocks shown in figure 1-18.

1-71. MICROPROCESSOR INTERFACE. The microprocessor interface consists of a number of registers that microprocessor PCA-A4 uses to communicate with PCA-A9. The registers are used to read information from PCA-A9 regarding status and self-test. The registers can also be written to, for the purpose of controlling the action of the track follower and for clearing certain faults that can occur on PCA-A9.

The signals that the microprocessor writes to PCA-A9 for the purpose of controlling the actions of track follower PCA-A9 include: Self Test Position Offset (STOPF-L), Index Sync (ISNC-H), Enable Start Of Sector (ESOS-L), Clear Error (CLER-H), Least Significant Bit (LSB-H), Skew Word Measure (SKWM-H), Sync Command (SNCM-L), Start Of Sector Presence (SOSP-L), and Self Test Enable (STEN-H).

Signals read by the microprocessor from PCA-A9 regarding status and self test include: Head Present (HP-H), AGC Fault (AGFLT-H), Sector Clock Presence (SCPR-H), Start of Sector Test (SOST-L), and Sync Error (SNCER-H). Refer to table 1-4 for a description of the microprocessor interface output and input signals listed above.

1-72. AMPLIFIER CHAIN. Data from the servo head is fed into an amplifier chain via connector J1. The amplifier chain consists of a preamplifier, an AGC amplifier, and a postamplifier. All three amplifiers have differential inputs and differential outputs. The gain of the AGC amplifier is controlled by signal Automatic Gain Control Voltage (AGCV) from the AGC reference summing circuit in the track position discriminator. A low pass filter is placed between the AGC amplifier and the postamplifier. The differential outputs from the postamplifier have an amplitude of 1.5 volts peak-to-peak and are labelled PRE+ and PRE-. Figure 1-7 illustrates the servo and data track assignments and the PRE waveforms that occur as the servo head moves across plus odd and plus even servo tracks.

1-73. AGC FAULT DETECTOR. During operation of the track follower, the absence of a servo head signal causes the amplifier chain to saturate. When this condition occurs, the AGC fault detector circuit transmits an AGC Fault Signal (AGFLT-H) to the microprocessor interface. Simultaneously, a Track Follower Fault Signal (TFFLT-H) is sent directly to the microprocessor. Following restoration of the servo head signal, the AGC voltage will move to its normal level. However, signals AGFLT-H and TFFLT-H are still active until the microprocessor asserts CLER-H.

1-74. PHASE LOCKED LOOP. The phase locked loop (PLL) circuit provides timing signals for the track follower signal processing circuits on PCA-A9. The PLL supplies timing pulses which are locked in phase with the servo code. These timing signals occur within three timing periods: dibit timing period, sector timing period, and disc revolution timing period. The PLL locks the outputs of a counter chain to the basic 800-kHz servo waveform signal. The PLL circuit consists of a phase discriminator, a 12.8-MHz voltage-controlled oscillator (VCO), and a gate generator.

1-75. Phase Discriminator. There are two inputs to the phase comparator: the recovered servo code (PRE+ and PRE-) and the locked reference (REF). The recovered servo code consists of balanced dibit patterns occurring at an 800-kHz rate when the track follower is on track. During seeks, the servo code becomes odd and even sets of amplitude modulated dibits with a 400-kHz fundamental frequency. The PLL retains lock during both conditions. The phase discriminator

Table 1-4. Head Positioning System Mnemonics

MNEMONIC	DEFINITION	SOURCE	FUNCTION
A0-H thru A11-H	Address bus, bits 0 thru 11	PCA-A4 (1)	Microprocessor address bus, bits 0 through 11.
ACT +, ACT -	Actuator Drive	PCA-A2 (4)	Power amplifier outputs or emergency retract outputs to linear motor M1.
ACTMP	Actuator Temperature	PCA-A8 (4)	Linear motor coil temperature sensor signal input to analog multiplexer on PCA-A18.
ACTSEL-L	Actuator Driver Select	PCA-A4 (1)	Actuator driver PCA-A2 select line from microprocessor. ACTSEL-L is active (low) when microprocessor is addressing PCA-A2.
ACTTST	Actuator Driver Test	PCA-A2 (4)	Analog test signal sent to microprocessor PCA-A4.
ACUR	Actuator Current	PCA-A2 (4)	Output of current sense detector. Detector monitors actuator driver current.
ADIS-L	Amplifier Disable	PCA-A20 (4)	Microprocessor interface input from emergency retract control logic signalling that the actuator driver power amplifier is disabled.
AGCV	Automatic gain Control Voltage	PCA-A9 (4)	Output of automatic gain control circuit on track follower PCA-A9.
AGFLT-H	AGC Fault	PCA-A9 (4)	Microprocessor interface input from AGC fault detector on PCA-A9. The microprocessor uses signal to sense absence or presence of servo signal from servo head.
CC	Current Command	PCA-A3 (4)	Input signal to actuator driver electronics.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
CCOM	Current Command For Actuator Driver	PCA-A3 (4)	Output from Servo PCA-A3 to actuator driver PCA-A2. Signal CCOM is amplified by PCA-A2 to drive the actuator assembly.
CLER-H	Clear Error	PCA-A9 (4)	Microprocessor interface output performing several functions on PCA-A9. It resets the SOSP-H (start of sector presence) signal and prepares the start of sector presence flip-flop to detect the next start of sector pulse which is too short for the microprocessor to detect directly. CLER-H is also used to clear the start of sector flip-flop for test purposes, making SOST-L (start of sector test) inactive while CLER-H is active. CLER-H resets the SCPR-H (sector clock pulse received) and PLER-H (phase lock error) lines and resets the sector sync sequencer circuit when a missing sector clock pulse occurs and the microprocessor does not want to resynchronize the track follower timing.
CLER-H/L	Clear Emergency Retract Latch	PCA-A20 (4)	Microprocessor interface output clearing emergency retract control logic on PCA-A20.
CLIP-L	Clear Input Latch	PCA-A20 (4)	Microprocessor interface output to emergency retract control logic.
CNVF-L	Connector Verify	PCA-A18 (4)	Microprocessor interface input indicating that the connector on the ribbon cable W1 between servo PCA-A3 and actuator status PCA-A18 is properly attached and that the velocity transducer (tachometer) cable is connected to J1 on PCA-A18.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
CRB-L	Carriage Is Back	PCA-A18 (4)	Microprocessor interface input from PCA-A18 indicating that the carriage is fully retracted into the actuator assembly.
CUL-H	Carriage Unlock	PCA-A3 (4)	Microprocessor interface output to carriage latch solenoid driver. When heads are loaded, microprocessor actuates solenoid long enough to allow carriage to move from its retracted position. Following this, the solenoid is deactivated.
D0-H thru D7-H	Data Bus, bits 0 thru 7	PCA-A4 (1)	Microprocessor bidirectional data bus, bits 0 through 7.
DCK-H	DTG Clock	PCA-A3 (4)	DTG clock control logic output register.
DCP-H	Data Clock Pulse	PCA-A10 (5)	Data clock pulses fed to track follower PCA-A9 for skew.
DEC-L	Deceler-ation Has Started	PCA-A3 (4)	Microprocessor interface input from deceleration indicator signaling that the carriage has started to decelerate during a normal seek operation. Signal is used by the microprocessor as an intermediate timeout check point.
DLE9-L	DTG Register less than or equal to 9	PCA-A3 (4)	Microprocessor interface input used during self test.
DT0-L thru DT2-L	Drive Type, bits 0 thru 2	PCA-A3 (4)	Microprocessor interface output to drive type gain select circuit programming gain of servo loop to match the moving mass of HP 7933 actuator.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
DTG0-H thru DTG10-H	Distance-To-Go Register, bits 0 thru 10	PCA-A3 (4)	Output of an 11-bit register used to address the velocity curve generator. During a write operation the microprocessor preloads the DTG register to the value desired to cause the servo system to perform a seek or other velocity control funtion. The microprocessor can also read the value of the DTG register for normal operations during a seek, and for self test.
DTGEN-H	Distance To-Go Register Clock Enable	PCA-A3 (4)	Microprocessor interface output controlling when the DTG register is clocked.
+EMRSUPP	Emergency Retract Positive Supply Voltage	PCA-A12 (3)	Unregulated +36 Vdc supplied by PCA-A12 to the emergency circuits on PCA's A2 and A20.
-EMRSUPP	Emergency Retract Negative Supply Voltage	PCA-A12 (3)	Unregulated -36 Vdc supplied by PCA-A12 to the emergency retract circuits on PCA's A2 and A20.
ERDR	Emergency Retract Drive	PCA-A2 (4)	A signal from the switching regulator to the emergency retract driver on PCA-A2 causing approximately 5 amperes to flow through the linear motor coil for approximately 0.5 second when an emergency retract command has been received.
ER-H	Emergency Retract	PCA-A20 (4)	Emergency retract flag signal from the emergency retract control logic. Signal is active (high) when an emergency retract occurs.
ERVCC	Emergency Retract Vcc	PCA-A2 (4)	A low voltage supply that powers the switching regulator on PCA-A20.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
ESOS-L	Enable Start of Sector	PCA-A9 (4)	Microprocessor interface output enabling SOS-L and SOST-L. (Start of Sector signals.)
FCEN-H	First Clock Enable	PCA-A3 (4)	Used in the DTG clock control logic. Causes the QTC-H signal to be used as the first track crossing.
FPOS	Fast Position	PCA-A9 (4)	Track follower position error signal used during seeks.
FPOSEN-L	Fast Position Switch Enable	PCA-A3 (4)	Enables the FPOS signal--both FPOSEN-L and SPOSEN-L are disabled when PST-L is active (low).
HP-H	Head Present	PCA-A9 (4)	Microprocessor interface input from head bias circuit indicating state of servo head. Signal is active (high) for a good head and inactive for a bad head.
INPUT-L	Input Latch	PCA-A20 (4)	Microprocessor interface input from emergency retract control logic reporting that an input signal capable of causing an emergency retract has been received. INPUT-L is reset by CLIP-L.
IP-L	Index Pulse	PCA-A9 (4)	Pulse generated once per spindle rotation by once-around counter on PCA-A9.
ISNC-H	Index Sync	PCA-A9 (4)	Microprocessor interface output synchronizing the once-around counter on track follower PCA-A9 that generates a pulse once per spindle rotation. The counter is preset when ISNC-H is active (high), and disabled when ISNC-H is inactive (low).

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
LER-H	Latched Emergency Retract	PCA-A20 (4)	Microprocessor interface input indicating the state of emergency retract latch. An active (high) signal indicates that the emergency retract latch is set. That is, an emergency retract has occurred and the microprocessor has not cleared the latch.
LIERR	Linear Error	PCA-A3 (4)	Output of linear mode error amplifier. The amplifier is a differencial amplifier that forms an error signal between the current command (CC) signal and the actuator current (ACUR) signal. The amplifier output is connected via an analog switch, operated by the linear/switching mode control circuit, and a buffer amplifier to the differential power amplifier on actuator driver PCA-A2. The buffer amplifier output is labeled CCOM.
LIN-H	Amplifier is Linear	PCA-A3 (4)	Output signal from linear/ switching mode control circuit. Signal LIN-H determines whether the amplifier operates in a linear mode (LIN-H high) or a switching mode (LIN-H low). The switching mode is used for controlling the high currents during a seek and the linear mode is used when track following.
+LMSUPP	Actuator Positive Supply Voltage	PCA-A12 (6)	Unregulated +36 Vdc supplied by PCA-A12 to PCA-A2.
-LMSUPP	Actuator Negative Supply Voltage	PCA-A12 (6)	Unregulated -30 Vdc supplied by PCA-A12 to PCA-A2.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
LNGSK-H	Long Seek	PCA-A3 (4)	Microprocessor interface output used in velocity curve control logic. Signal is active (high) when the disc drive is doing a seek of 33 or more tracks.
LSB-H	Least Significant Bit	PCA-A9 (4)	Microprocessor interface output. When tracking on even tracks, the slope of the position signal is different from the slope of the position signal when odd tracks are being tracked. This is due to the alternating band pattern of the servo disc. The microprocessor compensates for this by outputting the least significant bit of the physical track address. This ensures that the polarity of the track follower position signal output to servo PCA-A3 is correct. Signal LSB-H is also returned to microprocessor interface for self test purposes.
MNVEL-L	Maximum Negative Velocity Command Enable	PCA-A3 (4)	Velocity curve generator output voltage that causes carriage to accelerate toward the outside of the disc during the first part of a long seek.
MPVEL-L	Maximum Positive Velocity Command Enable	PCA-A3 (4)	Velocity curve control logic output that causes carriage to accelerate toward the inside of the disc during the first part of a long seek.
MRST-L	Master Reset	PCA-A1 (6)	Master reset signal. MRST-L resets the disc drive circuitry at power turn on.
MXSEL0-H thru MXSEL2-H	Multiplexer Select, bits 0 thru 2	PCA-A3 (4)	Microprocessor interface output selecting analog multiplexer signal for transmission to analog-to-digital converter on microprocessor PCA-A4. Signals input to the multiplexer include TAC, TEMP, CCOM, VREF, CC, VC, OFST, and POS.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
NTRI	Negative Triangle Wave	PCA-A3 (4)	A negative triangle waveform used when the actuator driver is in a switching mode. The waveform is used to pulse width modulate the switching mode error amplifier.
OFST	Offset	PCA-A3 (4)	Voltage offset from automatic head alignment offset DAC.
OFST0-H thru OFST7-H	Head Alignment Offset bits 0 thru 7	PCA-A3 (4)	Microprocessor interface output setting automatic head alignment offset value in digital-to-analog converter on PCA-A3.
OFTRK-H	Off Track Fault	PCA-A3 (4)	Latched output of track center detector. OFTRK-H becomes active (high) if the servo head goes off track after it should have settled. OFTRK-H is monitored by the microprocessor during normal operation and the detector is cleared by the microprocessor after the servo has settled on track.
OPOS	Offset Position	PCA-A3 (4)	Signal POS with automatic head alignment offset added.
OTSET-H	On Track Latch Set	PCA-A3 (4)	Microprocessor interface output clearing off track fault sensed by track center detector.
PADIS-H	Processor Amplifier Enable	PCA-A20 (4)	Microprocessor interface output controlling power amplifier on PCA-A2. An active (high) signal will disable the power amplifier. An inactive (low) signal will enable the power amplifier, provided that the emergency latch is cleared and no conditions are present that will cause an emergency retract.
PER-L	Micro-processor Emergency Retract	PCA-A20 (4)	Microprocessor interface output causing an emergency retract to occur.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
PEXS-H	Pack Exhaust Temperature Sensor Select	PCA-A3 (4)	Microprocessor interface output selecting output of actuator coil temperature sensor (PEXS-H low) or module exhaust temperature sensor (PEXS-H high) from actuator status PCA-A18. Selected output is TEMP signal input to analog signal multiplexer on Servo PCA-A3.
PEXTMP	Pack Exhaust Temperature	PCA-A18 (4)	Pack exhaust temperature sensor signal input to analog multiplexer on PCA-A18.
POS	Position	PCA-A3 (4)	Output of position signal select and self test logic. Selected signal is derived from track follower signal FPOS, SPOS, or OFST. FPOS is used during seeks, SPOS is used after settling on track, and OFST is used during self test.
POSEN-L	Position Control Loop Enable	PCA-A3 (4)	Microprocessor interface output controlling current command select logic. During normal operation, POSEN-L is inactive (high) when the disc drive is performing head loading, unloading, or seeks and is active (low) when the disc drive is following the servo track.
PRE+, PRE-	Pre-amplifier +,-	PCA-A9 (4)	Differential output of amplifier chain on PCA-A9.
PSF-H	Power Supply Fail	PCA-A20 (4)	Emergency retract control logic input from power supply failure monitor reporting that a power supply failure has occurred. Failure is also reported to microprocessor interface. An active (high) signal indicates that one or more of the +5V, +12V, +36V, or -36V power supplies is below acceptable limits.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
PST-L	Position Self Test	PCA-A3 (4)	Microprocessor interface input. Signal PST-L routes the auto head alignment offset signal into the POS signal path to test the POS related circuits on servo PCA-A3.
PTRI	Positive Triangle Waveform	PCA-A3 (4)	A positive triangle waveform used when the servo amplifier is in a switching mode. The waveform is used to pulse width modulate the switching mode.
PWM-L	Pulse Width Modu-ulator Self Test	PCA-A3 (4)	Microprocessor interface output that goes low whenever CCOM is above +1.4V or below -1.4V. Signal is used to check the PWM circuitry.
QTC-H	Plus or Minus Quarter Track Crossing	PCA-A3 (4)	A narrow pulse from the plus and minus quarter track crossing detector indicating when the servo head is either plus one quarter track from the center of a servo band or minus one quarter track from the center of a servo band. QTC-H is used to clock the DTG register when selected by the DTG clock control logic.
R0RD-L R1RD-L, R3RD-L, R6RD-L, R7RD-L	Register 0, 1, 3, 6, 7,	PCA-A3 (4)	Enables specified read register so that microprocessor can read the contents of the register.
R0WR-L thru R6WR-L	Register 0 thru Register 6 Write	PCA-A3 (4)	Indicates when the specified register is being written to by the microprocessor.
RD-L	Read	PCA-A4 (4)	Microprocessor read command to microprocessor interface circuitry.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
RK1	Relay 1 Coil	PCA-A20 (4)	Output of amplifier enable relay driver. This relay disables the power amplifier on PCA-A2 during emergency retracts. The default state of the relay (no power to actuator coil) disables the power amplifier.
RK2	Relay 2 Coil	PCA-A20 (4)	Output of emergency retract relay driver. This relay switches the coil of the actuator between the power amplifier output and the emergency retract driver output. The default state of the relay (no power to coil) connects the actuator coil to the emergency retract driver.
ROM-10H, ROM-11H	ROM Address bits 10,11	PCA-A3 (4)	Two high order address lines for ROM in VC generator. Selected profile is indicated as follows: BIT 11 — BIT 10 — SELECTED PROFILE 0 — 0 — Fast 0 — 1 — Half-fast 1 — 0 — Quarter-fast 1 — 1 — Slow
SCPR-H	Sector Clock Presence	PCA-A9 (4)	Microprocessor interface input. Signal SCPR-H becomes active (high) when the sync information at the beginning of a sector is received and remains active until reset by microprocessor interface signal CLER-H.
SKMFLG-L	Skew Measure-ment Strobe	PCA-A9 (4)	Microprocessor interface output to the skew measurement circuit. SKMFLG-L is set high at start of the skew word measure sequence which is initiated and terminated by SKWM-H. SKWM-L remains active until a DCP or self-test condition is detected.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
SKOF-H	Seek Off Disc	PCA-A3 (4)	Microprocessor interface output used to indicate which direction the carriage should move. SKOF-H is input to the velocity curve generator and the velocity curve control logic.
SKWM-H	Skew Word Measure	PCA-A9 (4)	Microprocessor interface output controlling skew correction. Track follower PCA-A9 contains a measuring and correction circuit for any displacement (skew) between the read and servo heads. Skew is measured as timing differences because the discs are in motion. When SKWM-H is activated (bit high), the skew measurement circuit waits for a DCP (data clock pulse) from the read/write system. The DCP signal occurs when read/write PCA-A10 detects a sector clock pulse. When track follower PCA-A9 receives a DCP pulse, it latches the current value of an internal counter into the skew measurement register. For zero skew between the read and servo heads this register will read 80 (hexadecimal).
SKW0-H thru SKW7-H	Skew Control Word, bits 0 thru 7	PCA-A9 (4)	Microprocessor interface signal used to control amount of skew required.
SKWM0-H thru SKWM7-H	Skew Measure, bits 0 thru 7	PCA-A9 (4)	The contents of a register on PCA-A9 containing a skew word that is compared with the track follower's internal counter to generate Start of Sector (SOS-L).
SLND	Solenoid	PCA-A3 (4)	Carriage latch solenoid driver output to carriage latch. Signal is connected to solenoid via actuator status PCA-A18.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
SMS-L	Skew Measurement Strobe	PCA-A9 (4)	Microprocessor interface signal used to latch the intra sector count into the skew measure latch during the skew measurement sequence.
SNCER-H	Sync Error	PCA-A9 (4)	Microprocessor interface input indicating that the sector clock pulse detect of the sector sync information on the servo bands does not occur when PCA-A9 expects it. The microprocessor can reset SNCER-H, ignore it, or activate SNCM-H.
SNCM-L	Sync Command	PCA-A9 (4)	Microprocessor interface output causing PCA-A9 to resynchronize its internal counters to the sector clock pulses. (See SNCER-H.)
SOS-L	Start of Sector	PCA-A9 (4)	Start of sector pulses output by skew delay comparator on PCA-A9.
SOSP-H	Start of Sector Presence	PCA-A9 (4)	Microprocessor interface input. PCA-A9 can generate start of sector pulses by comparing the skew set register contents with its internal counter. Start of sector pulses are captured by a flip-flop which generates SOSP-H. This signal can be reset with CLER-H.
SOST-L	Start of Sector Test	PCA-A9 (4)	Microprocessor interface input derived from SOS (start of sector) output. In normal operation, SOST-L is a train of short pulses. The function can be tested with WCLE-H and CLER-H. With CLER-H and WCLE-H inactive (low), SOST-L should be active (low).

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
SPDDN-H	Spindle Speed	PCA-A4 (3)	Signal from microprocessor PCA-A4 control logic on PCA-A20 indicating that spindle motor is out of speed lock control. SPDDN-H will initiate an emergency retract.
SPEN-H	Slow Position Signal Enable	PCA-A3 (4)	Microprocessor interface output selecting either the "slow" position signal (SPOS) or the "fast" position signal (FPOS) from track follower PCA-A9. SPOS is used when track following and FPOS is used during seeks.
SPOS	Slow Position	PCA-A9 (4)	Track follower position error signal used during track following.
SPOSEN-L	Slow Position Switch Enable	PCA-A3 (4)	Enables the SPOS signal- both FPOSEN-L and SPOSEN-L are disabled when PST-L is active (low).
SRVSL-L	Servo Select	PCA-A4 (1)	Servo PCA-A3 select line from microprocessor. SRVSL-L is active (low) when microprocessor is addressing PCA-A3.
SRVTST	Servo Test	PCA-A3 (4)	Output of analog signal multiplexer sending servo test signals to the analog-to-digital converter on microprocessor PCA-A4. Signals tested are TAC, TEMP, CCOM, VREF, CC, VC, OFST, and POS.
STCLK	Self Test Clock	PCA-A3 (4)	Microprocessor interface output used by the DTG generator clock logic to clock the DTG generator during self test.
STEN-H	Self Test Enable	PCA-A9 (4)	Microprocessor interface output activating the self test generator on PCA-A9. See STPOF-L. STEN-H also enables a test of the skew measuring circuitry.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
STPOF-L	Self Test Position Offset	PCA-A9 (4)	Microprocessor interface output activating the self-test signal generator to simulate the dibits that are received when the servo head is reading the servo bands. When the read/write heads are properly positioned, the servo head picks up alternating dibits from each of the two servo bands. These signals are of equal amplitude, causing the two track follower position signals, FPOS and SPOS to be at zero volts, indicating correct position. If the servo head moves off track, it picks up more signal from one servo band and less from the other, causing the position signals to change and indicate a non-zero value. Worst case for off position is when the servo head is centered over one servo band. This occurs when the heads are between tracks. The dibits from one servo band disappear causing the frequency at which dibits are received to be halved. This condition can be simulated by halving the frequency of the self-test generator. This is what happens when STPOF-L goes active (low).
SWERR	Pulse Width Modulation	PCA-A3 (4)	Output of switching mode error amplifier. The amplifier takes the error signal created by the difference between the current command (CC) signal and the actuator current (ACUR) signal and pulse width modulates it. The modulated output (PWM) is connected via an analog switch, operated by the linear/switching mode control circuit, and a buffer amplifier to the differential power amplifier on actuator driver PCA-A2.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
TAC	Tachometer	PCA-A3 (4)	Actuator tachometer signal output from tachometer buffer on servo PCA-A3.
TCC-H	Track Center Crossing Detector	PCA-A3 (4)	A narrow pulse from the center track crossing detector indicating when the servo head has gone over the center of a servo track. Signal TCC-H is used to clock the DTG register when selected by the DTG register clock control logic. (See DCK-H.)
TCD-H	Track Center Detector	PCA-A3 (4)	Microprocessor interface input from track center detector. Microprocessor Uses TCD-H to change the servo control from a velocity loop to a position loop during normal operations. When track following TCD-H is active (high) when the servo head is within 175 microinches of track center.
TEMP	Temperature	PCA-A18 (4)	Actuator status PCA-A18 temperature sensor multiplexier output connected to analog signal multiplexer on servo PCA-A3. The multiplexier output is selected by PEXS-H.
TFFLT	Track Follower Fault	PCA-A9 (4)	Track follower fault flag returned directly to microprocessor PCA-A4.
TFSEL-L	Track Follower Select	PCA-A4 (1)	Track follower PCA-A9 select line from microprocessor. TFSEL-L is active (low) when microprocessor is addressing PCA-A9.
TFTST	Track Follower Test	PCA-A9 (4)	Analog test signal sent from PCA-A9 to microprocessor PCA-A4. Signal is same as SPOS.
TO-H	Time Out	PCA-A20 (4)	Microprocessor interface input indicating that an emergency retract is currently in progress, that is, the emergency retract time is timing out.

Table 1-4. Head Positioning System Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
VC	Velocity Curve	PCA-A3 (4)	The output of the velocity curve generator.
VCEN-L	Velocity Curve Switch Enable	PCA-A3 (4)	Connects VC into velocity loop as desired velocity signal.
VREF	Reference Voltage	PCA-A3 (4)	A stable 6.2 Vdc voltage source on servo PCA-A3. The voltage is used to provide bias current for the digital-to analog converters on PCA-A3 and to define window sizes in the track center detect circuit.
WCLE-H	Write Clock	PCA-A9 (4)	Microprocessor interface output that gates the 30 MHz output of the PLL voltage-controlled oscillator to external signal TFCLK-L. In normal operation, WCLE-H is active (high). For test purposes, WCLE-H has a second funcion. When low, it sets SOSP-H, and causes SOST-L and SOS-L to be active.
WR-L	Write	PCA-A4 (1)	Microprocessor write command to microprocessor interface circuitry.
4 MHz-H	4-MHz clock	PCA-A4 (1)	Self-test clock used in self test circuitry.

is implemented using a sample and hold technique. The incoming dibit waveform is sampled by a solid-state switch and a capacitor. The switch is closed during the reference pulse and the trailing edge of the reference signal initiates the hold function. If the trailing edge of the reference signal occurs at the dibit zero, crossing zero error is held. If the trailing edge of the reference pulse is early, a positive error voltage is held and if it is late, a negative error voltage will result. If a dibit pattern does not appear, the sampling circuit samples zero volts and no significant transients will be encountered. On the average, the loop will drive the reference pulse trailing edge to coincide with the zero crossing when the loop is locked.

1-76. Voltage-Controlled Oscillator. The phase discriminator output is fed to the input of a voltage-controlled oscillator (VCO). The LC tank circuit of the oscillator is tuned to approximately 12.8 MHz and is made voltage-tuneable with varator tuning diodes. The oscillator output is level-shifted for TTL compatibility.

1-77. Gate Generator. The VCO output feeds 12.8 MHz to the gate generator which outputs dibit and sector timing signals. The 12.8-MHz clock signal is fed into five stages of binary counter. The last four bits of the 5-stage counter are used to form 16 different 115-nanosecond timing periods. An 8 by 32 ROM is used to decode the 4 bits into eight different timing waveforms. The fifth input to the ROM is signal Least Significant Bit (LSB-H), the least significant bit of physical track address. This signal indicates whether the track is even or odd. The generator outputs A Sample (ASMP) and B Sample (BSMP) signals to control the timing of the sample-and-hold circuits contained in the track position discriminator.

1-78. TRACK POSITION DISCRIMINATOR. The track position discriminator processes the incoming servo code to obtain position and amplitude information. Included in the discriminator are a dibit integrator, sample and hold circuits, an AGC reference summing circuit, a differential amplifier, and a limited-slew-rate amplifier.

1-79. Dibit Integrator. The dibit integrator processes the servo code by measuring the energy contained in the first half of each dibit, holding it for sampling, and then discharging it to a constant value before processing the next dibit.

1-80. A and B Sample and Hold Circuits. A pair of sample and hold circuits are used to demultiplex the even and odd dibits into A and B channels. The channels are scaled and summed by the AGC reference summing circuit to provide an AGC voltage reference level. The channels are also subtracted by a differential amplifier to provide position information.

1-81. AGC Reference Summing Circuit. The AGC reference summing circuit provides a voltage which is proportional to the sum of the A and B channels. This summation, labelled Automatic Gain Control Voltage (AGCV), is used to control the gain of the AGC amplifier in the amplifier chain.

1-82. Differential Amplifier. The differential amplifier subtracts the A and B channels to provide a bipolar signal referenced to zero and proportional to the linear position of the head relative to an odd-even track pair. The amplifier output, labeled Fast Position (FPOS), is the signal used by servo PCA-A3 for counting track crossings.

1-83. Limited-Slew-Rate Amplifier. Signal FPOS is also passed through a limited-slew-rate amplifier. The amplifier output, labelled Slow Position (SPOS), is the signal used by servo PCA-A3 for track following. The amplifier output is also returned to microprocessor PCA-A4 for self-test purposes. This line is labelled Track Follower Test (TFTST).

1-84. SECTOR DECODING. The servo code has sector timing information encoded on it for the following two purposes: a) to provide a physical reference from which the start of sector signal can be derived, and b) to differentiate between even and odd tracks. The information is encoded by including patterns of extra dibits at the beginning of each sector. The extra dibits occur in a pattern unique to an even track or an odd track. The circuits performing the sector decoding function include a sector clock pulse decoder, an inter-sector counter, and a sector counter synchronizer.

1-85. Sector Clock Pulse Decoder. The sector clock pulse decoder circuit decodes the extra dibit patterns on the servo surface to provide the required sector timing signals.

1-86. Intra-Sector Counter. The purpose of the intra-sector counter is to provide a reliable start of sector signal. This is required because the error rate of sector clock pulse detection due to noise, signal loss, and other phenomena is unacceptable for reliable operation of the disc drive. The intra-sector counter is synchronized with sector clock pulse detections, but thereafter depends only on the phase locked loop.

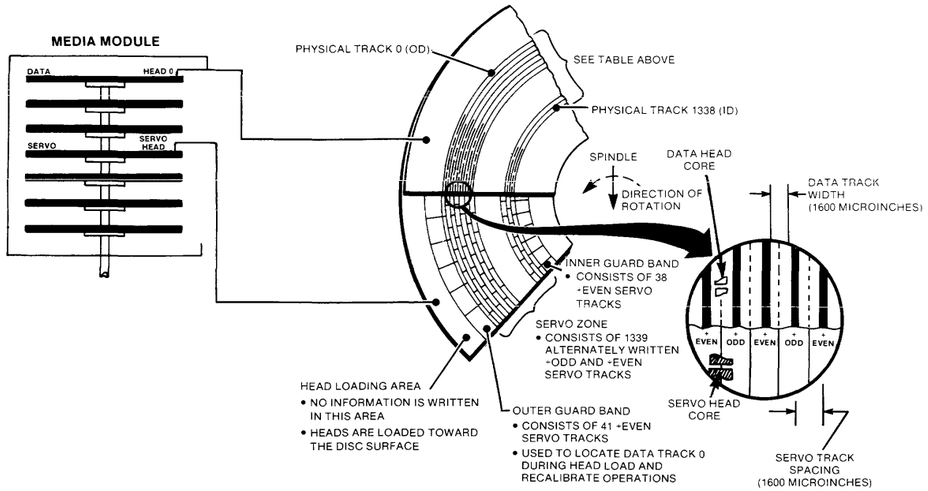
1-87. Sector Counter Synchronizer. Proper synchronization between the output of the sector clock

MEDIA MODULE PHYSICAL-LOGICAL CYLINDER MAPPING

PHYSICAL TRACK NO.	LOGICAL TRACK NO./TYPE
0 (OD)	LANDING TRACK
1	AHA } OD AUTOMATIC
2	AHA } HEAD ALIGNMENT
3	AHA } BAND
4	SYS. MAINT. NO. 1
5	0
6	1
.	.
.	.
.	.
113	108
114	109
115	SPARE (SEE NOTE 4)
116	110
117	111
.	.
.	.
.	.
334	328
335	329
336	SPARE (SEE NOTE 4)
337	330
338	331
.	.
.	.
.	.
555	548

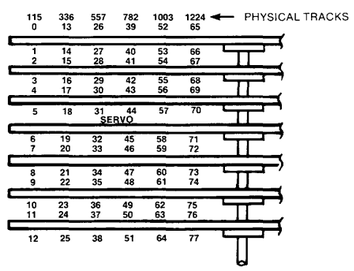
PHYSICAL TRACK NO.	LOGICAL TRACK NO./TYPE
556	549
557	SPARE (SEE NOTE 4)
558	550
559	551
.	.
.	.
.	.
638	630
639	631
640	AHA } MIDDLE AUTOMATIC
641	AHA } HEAD ALIGNMENT
642	AHA } BAND
643	SYS. MAINT. NO. 2
644	632
645	633
.	.
.	.
.	.
780	768
781	769
782	SPARE (SEE NOTE 4)
783	770
784	771
.	.
.	.
.	.
1001	988

PHYSICAL TRACK NO.	LOGICAL TRACK NO./TYPE
1002	989
1003	SPARE (SEE NOTE 4)
1004	990
1005	991
.	.
.	.
.	.
1222	1208
1223	1209
1224	SPARE (SEE NOTE 4)
1225	1210
1226	1211
.	.
.	.
.	.
1278	1263
1279	1264
1280	AHA } ID AUTOMATIC
1281	AHA } HEAD ALIGNMENT
1282	AHA } BAND
1283	1265
.	.
.	.
.	.
1336	1318
1337	1319
1338 (ID)	1320



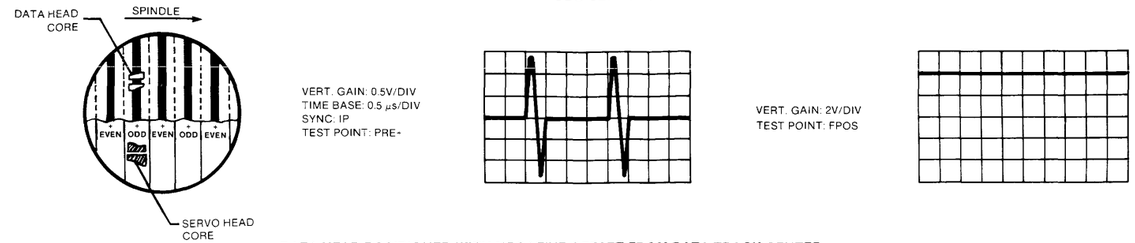
NOTES:

1. A DIBIT IS A READBACK SIGNAL PRODUCED FROM A MAGNETIC HEAD WHEN A MAGNETIC SURFACE WITH TWO CLOSELY SPACED SATURATED FLUX REVERSALS PASSES UNDER IT.
2. A +ODD TRACK IS A MAGNETIC SURFACE THAT PRODUCES DIBITS WITH THE LEADING EDGE POSITIVE AND THE TRAILING EDGE NEGATIVE WHEN READ BACK BY A CORRECTLY POLARIZED HEAD. THE DIBIT MUST OCCUR AT AN ODD INTERVAL. AN ODD INTERVAL IS DEFINED AS THE TIME PERIOD THAT IS AN ODD NUMBER OF INTERVALS FROM SOME REFERENCE LINE DRAWN RADIALLY FROM THE GEOMETRIC CENTER OF THE DISC.
3. A +EVEN TRACK IS A MAGNETIC SURFACE THAT PRODUCES DIBITS WITH THE LEADING EDGE POSITIVE AND THE TRAILING EDGE NEGATIVE WHEN READ BACK BY A CORRECTLY POLARIZED HEAD. THE DIBIT MUST OCCUR AT AN EVEN INTERVAL. AN EVEN INTERVAL IS DEFINED AS THE TIME PERIOD THAT IS AN EVEN NUMBER OF INTERVALS FROM SOME REFERENCE LINE DRAWN RADIALLY FROM THE GEOMETRIC CENTER OF THE DISC.
4. SPARE TRACKS ARE ENUMERATED ON THE 13 DATA SURFACES BY SCALAR NUMBERS, AS SHOWN BELOW:

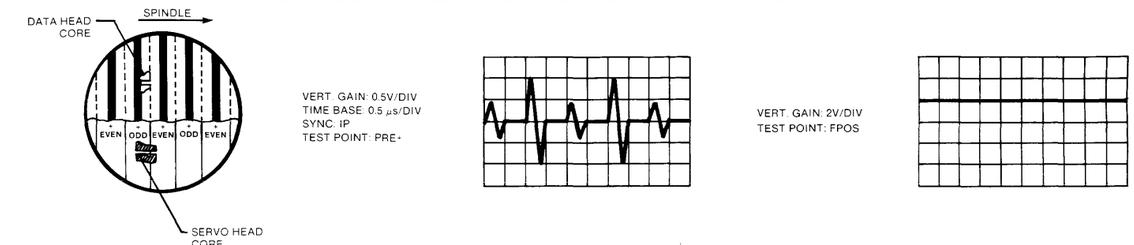


7933-348

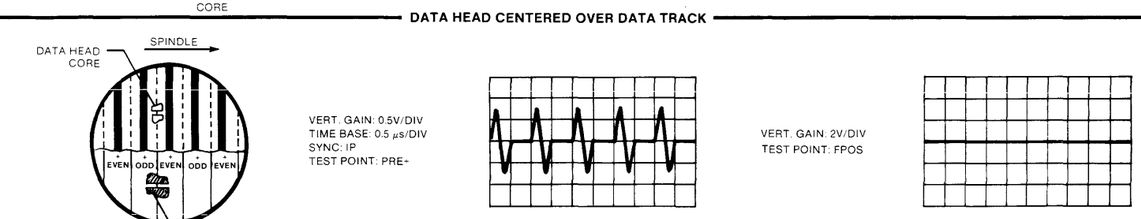
SERVO HEAD OVER +ODD SERVO TRACK



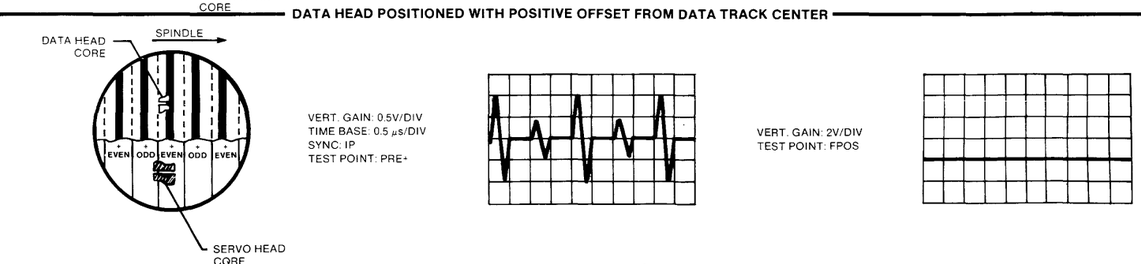
DATA HEAD POSITIONED WITH NEGATIVE OFFSET FROM DATA TRACK CENTER



DATA HEAD CENTERED OVER DATA TRACK



DATA HEAD POSITIONED WITH POSITIVE OFFSET FROM DATA TRACK CENTER



SERVO HEAD OVER +EVEN SERVO TRACK

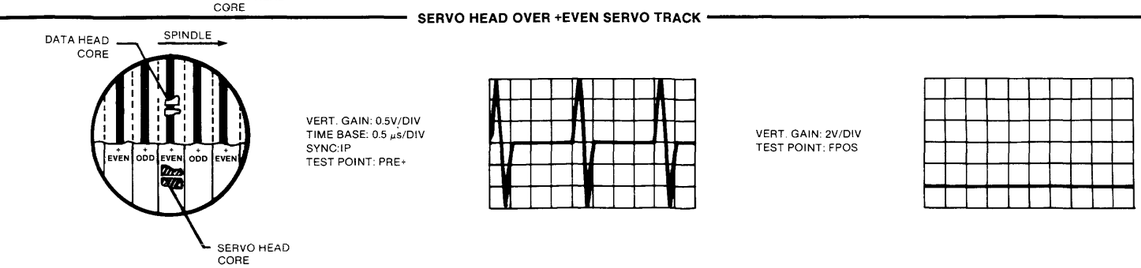


Figure 1-7. Data and Servo Track Assignments

pulse decoder (SCPGT) and the intra-sector counter (SCPDT) is maintained by the sector counter synchronizer.

1-88. ONCE-AROUND COUNTER. The function of the once-around counter is to provide an Index Pulse (IP-L) signal. Signal IP-L is generated once per revolution of the spindle motor. The counter can be preset to any sector by the microprocessor.

1-89. AUTOMATIC HEAD ALIGNMENT. The automatic head alignment circuits located on track follower PCA-A9 and read/write PCA-A10 provide the capability to measure and correct for dynamic head misalignment in radial position (offset) and circumferential position (skew).

The media module contains 13 data surfaces and one servo surface. There are 1,337 bands on the servo surface for track following and in addition, each band is marked with 93 sector marks for circumferential timing. Each data surface has three bands of special servo code. These bands are located precisely above servo bands 1, 641, and 1,281. The head positioning system, under microprocessor control, places the data heads over these special alignment bands for automatic head alignment measurements.

Each surface can be selected by the data head select circuit on read/write PCA-A10. The alignment band signals are fed into the read/write amplifier chain and the automatic head alignment module on PCA-A10. When the data heads are placed over an alignment band, an automatic head alignment position signal is produced that indicates how far from track center the data head is located. The signal, which is a bipolar voltage proportional to the error, is fed to the microprocessor for measurement. Sector timing is also indicated by Data Clock Pulse (DCP-H) signals, which occur where sectors should begin.

These DCP-H signals are fed to the skew measure sequencer on PCA-A9. The skew is measured by latching the value of the intra-sector counter at the arrival of signal DCP-H from the data surface. This value is fed to the microprocessor.

The microprocessor calls the automatic head alignment routines when the disc drive loads heads, after temperature changes, when a specified number of read errors is exceeded, and at regular time intervals. The sequence begins by recalling the automatic head alignment offset calibration factor. This factor is determined during self test by measuring the head alignment position signal for a simulated on-track condition. This value is subtracted from all head alignment readings. The microprocessor then selects a head, enables the automatic head alignment circuit, and measures the head alignment position voltage. This is accomplished by repeatedly measuring for one revolution (100 times) and averaging the result to null the runout component. An offset is added to the servo system equal to the measured offset. The measurement is repeated four times or until the measurement result is less than 2 counts. The final resulting offset is stored in the head alignment table.

Next, the skew measure circuit on track follower PCA-A9 is activated. Skew is defined as the circumferential timing difference of any data head with respect to the servo head. This value is measured by storing the value in the intra-sector counter on PCA-A9 at the instant that the Sector Clock Pulse (SCP) is received from the data surface via the automatic head alignment module on read/write PCA-A10. This value is stored in a skew table. The radial offset and circumferential skew measurements are repeated on all surfaces and at each alignment cylinder.

After the auto skew and offset tables are generated, the offset and skew can be adjusted for a seek to any track. The values for offset taken at the alignment bands on either side of the target track are recalled. An interpolation is then done to provide an offset value for the target track. A similar interpolation is made for skew.

1-90. Skew Measure Sequencer. The skew measure sequencer latches the output of the intra-sector counter at the instant DCP is asserted. The controller then reads the skew measure register. The microprocessor can set the start of sector pulse on the DCP signal by placing the measured value in the skew magnitude register. This register feeds the skew delay.

1-91. Skew Delay Comparator. The skew delay comparator outputs signal Start Of Sector (SOS-L) when the intra-sector timing counter equals the skew value register.

1-92. SELF TEST. Self test of PCA-A9 is accomplished by injecting a synthetic dibit signal derived from the microprocessor clock signal (4 MHz-H) into the AGC amplifier. This signal tests the phase locked loop and the track position discriminator circuitry. The AGC Fault (AGFLT-H) circuit and the Track Follower Test Signal (TFTST) signal are used to verify that the track follower analog circuits are operating properly. Signal Start Of Sector Presence (SOSP-L) is used to verify that Start Of Sector (SOS-L) is being issued. The sector clock pulse decoder is checked by sequencing a correct sector code through the sector clock pulse decoder circuit.

1-93. SERVO PCA-A3

The function of servo PCA-A3 is to provide control for the positioning of the carriage and head assembly.

The servo PCA acts with microprocessor PCA-A4 to perform track-to-track seeks, head loading and unloading, and self test. The offset for automatic head alignment is input to servo PCA-A3 from microprocessor PCA-A4. The servo PCA also contains the circuits required to compensate the servo system for track following.

1-94. MICROPROCESSOR INTERFACE. The microprocessor interface consists of eight registers that microprocessor PCA-A4 can address to either write to or read from servo PCA-A3. The signals that the microprocessor writes to PCA-A3 for the purpose of controlling and testing the servo circuitry include: Carriage Unlock (CUL-H), Drive Type (DT0-L through DT2-L), Distance-To-Go Clock Enable (DTGEN-H), Multiplexer Input Select (MXSEL0-H through MXSEL2-H), Head Alignment Offset (OFST0-H through OFST7-H), On Track Latch Set (OTSET-H), Pack Exhaust Temperature Sensor Select (PEXS-H), Position Self Test (PST-L), Seek Off Disc (SKOF-H), Slow Position Enable (SPEN-H), Self Test Clock (STCLK), Self Test Enable (STEN-H), Velocity Command Gate Enable (VCGEN-L), Position Control Loop Enable (POSEN-L), Long Seek (LNGSK-H), and ROM Address bits 10 and 11 (ROM10-H and ROM11-H). Refer to table 1-4 for a description of the functions of these signals.

Signals read by the microprocessor from PCA-A3 regarding status and self test include: Connector Verify (CNVF-L), Carriage Back (CRB-L), DTG Register Less Than Or Equal To Nine (DLE9-L), Deceleration Has Started (DEC-L), Pulse Width Modulator Self Test (PWM-L), Track Center Detector (TCD-H), and Distance-To-Go Register, bits 0 through 10 (DTG0-H through DTG10-H). Refer to table 1-4 for a description of these signals.

1-95. VELOCITY CURVE GENERATOR. The velocity curve generator consists of three components: a 4-byte by 8 ROM, a companding digital-to-analog converter, and an operational amplifier. When an address from the Distance-To-Go register (DTG0-H through DTG10-H) is input to the ROM, a voltage appears at the operational amplifier output. This voltage, labelled Velocity Command (VC), is used as the reference when servo PCA-A3 is controlling the velocity of the carriage.

The ROM has four sets of four curves stored in it which act as the reference for seeks of different lengths. Four curves per set are used to allow the disc drive to perform long seeks in an optimum manner, and still perform shorter seeks well. The four sets of curves are used to provide a combination of high performance (fast seeks) and high reliability (low power, slow seeks).

The slow profile is designed to guarantee that the actuator coil cannot be overheated. The power dissipation of this curve is approximately one half that of the fast curves. Only the "long" seek profile is different between the fast and slow sets of curves. Shorter seeks do not dissipate enough heat to require a slower seek time.

All of the discussion that follows applies to both the fast and slow velocity profiles. (Details of how the microprocessor decides to select the fast or slow curves are provided in later paragraphs.)

The specific curve which is selected for a given seek depends on the length of the seek. Seeks that are longer than 32 tracks are defined as "long" seeks. Seeks that are between nine and 32 tracks are defined as intermediate seeks, and seeks between three and eight tracks long are defined as "medium" seeks. Seeks that are one or two tracks long are called "short" seeks.

The shape of the four curves within each set is essentially the same. The desired velocity output is basically proportional to the square root of the distance to go to the desired track. This type of curve gives constant deceleration during the last part of the seek, which optimizes seek time.

The companding digital-to-analog converter in the velocity curve generator changes the digital input from the ROM to an output current. Seven bits from the ROM are used to determine the magnitude of the output current and one bit determines the sign. The sign bit is controlled by signal Seek Off The Disc (SKOF-H). The output current is converted to a voltage by the operational amplifier in the generator.

1-96. VELOCITY CURVE CONTROL LOGIC. The velocity curve control logic provides the logic that connects the output from the velocity curve generator into the current command select logic block. Inputs to the velocity curve control logic include Distance-To-Go Register bits 0 through 10 (DTG0-H through DTG10-H), Velocity Command Gated Enable (VCGEN-L), Long Seek (LNGSK-H), Position Control Enable (POSEN-L), and Seek Off Disc (SKOF-H). The output of the velocity curve generator select (VC) is selected by signal VCEN-L. Output signal Maximum Positive Velocity Command Enable (MPVEL-L) or Maximum Negative Velocity Command Enable (MNVEL-L) is selected as the input to the current command select logic when the disc drive is doing a long seek, and the carriage is more than 768 counts from the target.

1-97. CURRENT COMMAND SELECT LOGIC. This circuit provides switching that controls which analog signals are used in the servo loop. The signals which are switched into the servo loop are Velocity Command (VC), Maximum Positive Velocity

Command (MPVEL-L), Maximum Negative Velocity Command (MNVEL-L), Tachometer Velocity (TAC) signal, and Offset Position (OPOS) signal. The OPOS signal is the POS signal with the automatic head alignment offset added in. The OPOS signal is controlled by the Position Loop Enable (POSEN-L) signal. When POSEN-L is active, the OPOS signal is connected into the loop. When POSEN-L is inactive, the TAC signal is connected into the loop. Signal POSEN-L is a microprocessor interface output signal. Signal POSEN-L is inactive (high) when doing head loading, unloading, or seeks and is active (low) when the drive is following the servo track.

1-98. DISTANCE-TO-GO REGISTER. The distance-to-go (DTG) register is used to address the ROM in the velocity curve generator. The register consists of three four-bit up/down counters connected so that they always count down. The counters are preloaded by microprocessor Data Bus bits 0 through 7 (D0-H through D7-H) when the disc drive needs to move the carriage assembly. The counters are clocked by either the center track crossing detector, the quarter track crossing detector, or the self-test clock. The selection of the proper clock is performed by the distance-to-go clock control logic. The register output is labelled Distance-To-Go Register bits 0 through 10 (DTG0-H through DTG10-H).

The value of the DTG register can be used to calculate how far the carriage is from the target track. For this reason signals DTG0-H through DTG10-H are returned to the microprocessor interface. For long seeks, the DTG value essentially tells how many tracks the carriage is away from the target. For other seeks, the DTG value is twice the distance to target, plus a constant value.

1-99. DISTANCE-TO-GO CLOCK CONTROL LOGIC. This logic block selects which clock is used for the DTG register. Control inputs include DTGEN-H, STEN-H, LNGSK-H, and POSEN-L. The DTG register is clocked by the output of the plus and minus quarter track crossing detector (QTC-H) when signal Distance-To-Go Register Clock Enable (DTGEN-H) is active and the drive is not doing a long seek. Signal QTC-H is also used when doing a long seek and the distance-to-go value is less than or equal to 9 (five tracks from the target). The output of the center track crossing detector (TCC-H) is used whenever DTGEN-H is active and the plus and minus quarter track crossings are not being used. The Self-Test Clock (STCL-K) is selected when signal DTG Register Clock Self Test Enable (STEN-H) is active.

1-100. CENTER TRACK CROSSING DETECTOR. The center track crossing detector indicates when the servo head has gone over the center of the servo track. The detector input is signal Position (POS), derived from track follower PCA-A9 or the self-test circuitry. The output of the detector is a narrow pulse which goes high when the track center is crossed. The output signal is labelled Track Center Crossing (TCC-H). Signal TCC-H is used to clock the DTG register when it has been selected by the DTG clock control logic.

1-101. PLUS AND MINUS QUARTER TRACK CROSSING DETECTOR. This block detects when the servo head is either plus one-quarter track from the center of the servo track, or minus one-quarter track from center. The detector input is signal Position (POS), derived from track follower PCA-A9 or the self-test circuitry. The output of the detector is a narrow pulse which goes high when either a plus or minus quarter track location is crossed. The output from the detector is labelled Quarter Track Crossing (QTC-H). A quarter track is defined as 2.3 volts on the POS signal. The output of the detector is used to clock the DTG register when it has been selected by the distance-to-go clock control logic.

1-102. VOLTAGE REFERENCE. The voltage reference generator provides a stable 6.2 volts (VREF) for certain circuits on servo PCA-A3. The voltage is used to provide the bias currents for the digital-to-analog converters in the velocity curve generator and the auto head alignment offset circuit. The voltage is also used in the track center detector circuit for defining window sizes.

1-103. TRACK CENTER DETECTOR. The track center detector is used to tell the microprocessor when the servo head is within a certain distance of track center (including the offset added by the auto head alignment DAC). Two operational amplifiers full wave rectify the OPOS signal. The second of the two amplifiers also acts as a summing junction for signals which control the size of the detector window. The output from this second amplifier is compared to analog ground by a comparator. When the voltage from the second amplifier is positive, the servo head is outside the detector window. The inverted output, labelled Track Center Detector (TCD-H) is connected to the microprocessor interface.

The track center detector has two window sizes. When the POSEN-L signal from the microprocessor is inactive (high) the window size is ± 1.5 volts with 0.7 volt of hysteresis. When POSEN-L is active (low), the window size is reduced to 0.65 volt with the same hysteresis.

The larger of the two windows is used at the end of a seek to tell the microprocessor to change from veolcity control to position control. The smaller window indicates that the servo head is within 175 microinches of center, and is used to tell the microprocessor that the servo head is very close to track center.

An off track fault indicator is included in the track center detector. The indicator employs a latch which goes high if the servo head goes off track after it should be settled. The output from the latch, labelled Off Track Fault (OFTRK-H), is connected directly to the microprocessor. Signal OFTRK-L is cleared by inverted signal OTSET-H from the microprocessor interface after the servo head has settled on track. If the servo head goes off track, the signal is latched high.

1-104. DECELERATION INDICATOR. The deceleration indicator informs the microprocessor when the carriage has started to decelerate. The output is labelled Deceleration Has Started (DEC-L). The Current Command (CC) signal is compared against analog ground by a comparator. The comparator output operates a circuit that provides a narrow pulse output on the rising and falling edge of the input. This pulse is used to clock a flip-flop. The flip-flop is cleared at the beginning of a seek by the First Clock Enable (FCEN-L) signal. Signal FCEN-L remains low long enough for the CC signal to start its acceleration command. When deceleration starts, signal CC changes sign and the flip-flop is clocked. The flip-flop output then goes low indicating that deceleration has begun. Signal DEC-L is used by the microprocessor during a long seek, as an intermediate timeout check point.

1-105. AUTOMATIC HEAD ALIGNMENT OFFSET DAC. This circuit includes an 8-bit digital-to-analog converter (DAC) and an operational amplifier. The DAC provides a current output and the operational amplifier converts the current output to a voltage. The value of the offset voltage is calculated by an automatic head alignment algorithm, which is included in the seek routine. The output of the automatic head alignment DAC is added to the POS signal (to create the Offset Position (OPOS) signal. Signal OPOS is also transmitted to the analog signal multiplexer so that the signal can be verified by the analog-to-digital converter on microprocessor PCA-A4.

1-106. CARRIAGE BACK DETECTOR. The carriage back indicator is located on actuator status PCA-A18 and consists of an infra-red optical sensor that detects when the carriage is fully retracted into the actuator. The output from the sensor, labelled Carriage Back (CRB-L), is transmitted to the microprocessor interface. Signal CRB-L is used during head loading and unloading.

1-107. ANALOG SIGNAL MULTIPLEXER. The analog signal multiplexer is used to select analog signals from servo PCA-A3 for connection to the analog-to-digital converter (ADC) located on microprocessor PCA-A4. The output line from the multiplexer to the ADC is labelled Servo Test (SRVTST). Eight analog test signals are selected by the multiplexer. The signal selected is defined by three Multiplexer Select bits (MXSEL0-H through MXSEL2-H) from the microprocessor interface. The signals input to the multiplexer are Position (POS), Offset (OFST), Velocity Command (VC), Current Command (CC), Reference Voltage (VREF), Current Command For Actuator Driver (CCOM), Temperature (TEMP), and Tachometer (TAC.).

1-108. TACHOMETER BUFFER. The tachometer buffer is a differential amplifier that buffers signals TAC-L and TAC-H from the velocity transducer (tachometer) on the actuator assembly. The output signal, labelled Tachometer (TAC), is input to the current command select logic.

The Connector Verify (CNVF-L) signal is used to check whether cable W1 between servo PCA-A3 and actuator status PCA-A18 is in place. When the velocity transducer connector is plugged into actuator status PCA-A18 and cable W1 is connected between servo PCA-A3 and actuator status PCA-A18, line CNVF-L is connected to ground. The microprocessor checks the state of CNVF-L during self test.

1-109. DRIVE TYPE GAIN SELECT. The drive type gain select circuit sets the gain of the servo system to match the moving mass of the actuator assembly. Microprocessor PCA-A4 reads the motherboard to determine which configuration is being used, and then selects the appropriate feedback resistor. The resistors are selected by activating one of the microprocessor interface output Drive Type (DT0-L through DT2-L) lines.

1-110. POSITION COMPENSATION AND LOW PASS FILTER. The position compensation consists of a single lead-lag network that provides 53 degrees of phase lead at the crossover frequency to stabilize the system. The low-pass filter is also part of the compensation for the system.

1-111. POSITION SIGNAL SELECT AND SELF TEST. This circuitry is used to input the head alignment offset into the position signal circuitry. This is done during self test so that the various circuits on PCA-A3 can be checked. Whenever the Position Self Test signal (PST-L) is active, the alignment offset signal is added in at the point where Slow Position signal (SPOS) and Fast Position signal (FPOS) are input to servo PCA-A3 from track follower PCA-A9. The normal summing point for the offset signal is turned off when Position Self Test (PST-L) is active. This circuit also selects which of the two position signals is required at a particular time. The "slow" signal (SPOS) is used when the disc drive has settled on track. The signal is more immune to servo transients

and cannot be used for track crossings. The "fast" signal (SPOS) is used whenever the drive is not track following. When signal PST-L is active (low), both signals are disabled.

1-112. TEMPERATURE SENSING. Servo PCA-A3 provides control for the temperature measuring circuitry on actuator status PCA-A18. The temperature circuitry measures the actuator coil temperature and the media module air exhaust temperature. The temperature sensors are selected by signal Pack Exhaust Temperature Select (PEXS-H). When signal PEXS-H is inactive (low) the actuator coil temperature sensor is selected and when PEXS-H is active (high) the media module air temperature sensor is selected. The selected sensor output (TEMP) is coupled to the microprocessor interface ADC via the analog signal multiplexer. (Refer to paragraph 1-107.)

1-113. SELF TEST. The self-test procedures for servo PCA-A3 are divided into four sections. The first three sections cover items which can be verified while the heads are not loaded and the fourth section is a self test which requires the heads to be loaded, so the disc drive can perform track-to-track seeks.

The first section tests the Connector Verify (CNVF-L) line, the velocity curve generator, the distance-to-go register, maximum positive and maximum negative velocity commands, signal DLE9-H, and associated digital logic.

The second section tests the automatic head alignment offset DAC, track center detector, signal OFTRK-H, gain from the OFST signal to the CC signal and signal DEC-L. The third section tests other signals that can be verified before the heads are loaded and the fourth section is for self test after the heads are loaded.

1-114. ACTUATOR DRIVER

The actuator driver circuitry is located on actuator driver PCA-A2, emergency retract PCA-A20, and a portion of servo PCA-A3.

The basic function of the actuator driver is to cause a current to flow in the coil of actuator linear motor B1 in response to a command voltage from the servo circuit. Since the amplifier output is a current in response to a voltage input, the amplifier is a transconductance amplifier. A dual-mode amplifier is employed in the actuator driver. When supplying the large currents required for seek and similar operations, the amplifier operates in a switching mode. When the actuator is track following and the required currents are small, the amplifier operates in a linear mode. The switching mode greatly reduces the power dissipated in the amplifier circuits. The amplifier output current is controlled by pulse-width modulation of the output stage switching cycle. The basic switching frequency is 24 kHz. The effective value of the current applied to the linear motor is the average value of the pulse-width modulated waveform.

In the actuator driver, a voltage proportional to linear motor current is generated by a differential amplifier connected across a current sensing resistor. The resulting actuator current is compared to the current command in a pair of error amplifiers, one for each operating mode. Each error amplifier outputs a current error signal which is proportional to the difference between the current command and the actuator current signal. The linear mode error signal is applied directly to the power amplifier, and the switching mode error signal is processed into a pulse-width modulated pulse train before being amplified.

1-115. LINEAR/SWITCHING MODE CONTROL. The actuator driver linear/switching mode control circuitry, located on servo PCA-A3, determines whether the amplifier will operate in the linear mode or the switching mode. The circuit consists of two analog voltage comparators acting as a window detector. If Current Command signal CC is greater than 1 volt of either polarity, corresponding to 2 amperes of linear motor current, the circuit will automatically select the switching mode. If the Current Command magnitude is less than 0.5 volt, corresponding to 1 ampere of motor current, the circuit selects the linear mode. Between 0.5 and 1.0 volt is a region of hysteresis where the circuit remains in the previous mode.

The mode control circuit has two outputs. The first output controls an electronic switch which selects either the Linear Mode Error (LIERR) signal or the Pulse Width Modulated (PWM) signal for application to the power amplifier input. The second output is signal Amplifier Is Linear (LIN-H), used to disable the triangle wave generator when the linear mode is selected.

1-116. LINEAR MODE. The only circuitry used exclusively in the linear mode is the linear mode error amplifier located on PCA-A3. The output of this block is Linear Error (LIERR), a signal proportional to the difference between the Current Command (CC) signal and the Actuator Current (ACUR) signal.

1-117. SWITCHING MODE. The current command processing in the switching mode generates a pulse-width modulated pulse train with an average value proportional to the difference between the Current Command (CC) signal and the Actuator Current (ACUR) signal. The amplitude of the pulse train is carefully controlled so that the power amplifier output from PCA-A2 will switch quickly from cut off to saturation and vice versa, with none of the other stages

saturating. The switching mode circuit includes a switching mode error amplifier, positive and negative voltage level comparators, positive and negative level shifters, a triangle-wave generator and a 40 microsecond delay and offset circuit.

1-118. Switching Mode Error Amplifier. The first block in the pulse width modulator is a switching mode error amplifier located on servo PCA-A3. This is a differential circuit that outputs a Switching Mode Error (SWERR) signal proportional to the difference between the Current Command (CC) signal and the Actuator Current (ACUR) signal.

1-119. Voltage Level Comparators. The actual pulse-width modulation is performed by two analog voltage level comparators. The positive voltage level comparator operates on positive error signals and the negative voltage level comparator operates on negative error signals. The second input to the positive comparator is a Positive Triangle Wave (PTRI) with a negative peak at zero volt and a positive peak at +5 volts. Conversely, the second input to the negative comparator is a Negative Triangle Wave (NTRI) with a negative peak at -5 volts and a positive peak at zero volt.

Both triangle waveforms applied to the voltage level comparators are derived from an oscillator in the triangle-wave generator. The oscillator is gated off by signal LIN-H when the amplifier is in the linear mode. The oscillator frequency is approximately 24 kHz.

1-120. Positive And Negative Voltage Level Shifters. The outputs of the positive and negative voltage level comparators are TTL logic levels (0 to +5 Vdc). This voltage is acceptable for the positive comparator, but the negative comparator output must be converted to a 0 to -5 Vdc swing. Also, a small offset is added to the zero level of each signal and the two signals are combined into one. This level shifting is performed by the positive voltage level shifter and negative voltage level shifter circuit blocks on servo PCA-A3.

1-121. Offset and 40 Microsecond Delay. These stages modify the pulse width modulation signal output to ensure that the output stages in the power amplifier switch correctly.

1-122. BUFFER AMPLIFIER. A buffer amplifier on servo PCA-A3 accepts either the Linear Mode Error (LIERR) signal or the Pulse Width Modulator (PWM) signal, amplifies the selected signal with a gain determined by the operating mode, and provides a low impedance drive to send the signal to the power amplifier on actuator driver PCA-A2. The buffer amplifier output is labelled Current Command for Actuator Driver (CCOM).

1-123. POWER AMPLIFIER. The power amplifier on actuator driver PCA-A2 is a three-stage discrete differential amplifier. The first two stages are true differential stages, and the output stage is a pair of identical power amplifiers driven differentially. The power amplifier input, CCOM, is converted from a single-ended to a differential signal in the first stage.

The power amplifier output is routed through the emergency retract relay to a compensation network and then to the linear motor coil. The emergency retract relay selects either the power amplifier output or the emergency retract output for application to the linear motor. The compensation network ensures the stability of the actuator driver feedback loop and helps keep the power transistors within their safe operating range.

1-124. CURRENT SENSE AMPLIFIER. The current sense amplifier on actuator driver PCA-A2 is a differential amplifier which amplifies the voltage developed across four (functionally two as shown in figure 1-18) current sensing resistors in series with the power amplifier output. A differential amplifier is required because neither side of the power amplifier is grounded and the load (the linear motor) is floating. Current sense amplifiers are used on both sides of the load. The current sense amplifier output, labelled Actuator Current (ACUR), is coupled to the switching mode and linear mode error amplifiers on PCA-A3.

1-125. EMERGENCY RETRACT. The purpose of the emergency retract circuitry is to ensure that the heads will be unloaded off the discs if any event occurs which may potentially prevent normal head unloading. An emergency retract can be triggered by a microprocessor command, a master reset, the spindle speed falling out of phase lock, or any of the +5, +12, +36 or -36 Vdc power supplies falling below acceptable limits. An emergency retract also disables the actuator driver amplifier and disconnects the output of the amplifier from the linear motor. Also, an emergency retract sets a latch which prevents the actuator from being enabled until the latch is cleared by the microprocessor. No additional emergency retracts can occur while the latch is cleared. Since Master Reset (MRST-L) sets the emergency retract latch, no power can be applied to the actuator driver until the microprocessor decides that it is safe to do so.

The components comprising the emergency retract function, with the exception of a few power components, are mounted on emergency retract PCA-A20, which is attached to actuator driver PCA-A2. The circuits on PCA-A20 include emergency retract control logic, relay drivers, a switching regulator, and a power supply fail monitor. In addition, the microprocessor interface for actuator driver PCA-A2 is also located on PCA-A20. The emergency retract circuit has one fault flag output connected directly to the microprocessor.

This signal, Emergency Retract (ER-H), is active (high) while an emergency retract is occurring and remains active until the cause is removed and the emergency retract latch is cleared.

1-126. Microprocessor Interface. The microprocessor interface on emergency retract PCA-A20 is the means of communication other than Emergency Retract (ER-H) between the actuator driver and the microprocessor. Almost all of the required communication involves the emergency retract function.

The signals that the microprocessor writes to PCA-A20 for the purpose of controlling the actions of the PCA include: Processor Emergency Retract (PER-L), Power Amplifier Disable (PADIS-H), Clear Emergency Retract Latch (CLER-H), and Clear Input Latch (CLIP-L).

Signals read by the microprocessor from PCA-A20 regarding status and self test include: Power Supply Fail (PSF-H), Input Latch (INPUT-L), Amplifier Disable (ADIS-L), Latched Emergency Retract (LER-H), and Time Out (TO-H). Refer to table 1-4 for a description of the signals referred to in the above paragraphs.

1-127. Emergency Retract Control Logic. The emergency retract control logic block on emergency retract PCA-A20 consists of three latches and two levels of gating. The first level of gating is essentially an OR function of Spindle Speed Down (SPDDN-H), Master Reset (MRST-L), Microprocessor Emergency Retract (PER-L), and Power Supply Failure (PSF-L). Any one of these four signals will set all of the three latches: the emergency retract latch, the power amplifier latch, and the input latch. The input latch remembers when an input signal capable of causing an emergency retract has been received, and reports this signal to the microprocessor interface as Input Received (INPUT-L). The input latch is cleared by signal Clear Input Latch (CLIP-L) from the microprocessor interface.

The emergency retract latch triggers the emergency retract and also prevents further emergency retracts from occurring until the latch is cleared by signal Clear Emergency Retract (CLER-L) from the microprocessor interface. The status of the emergency retract latch is sent to the microprocessor interface as Latched Emergency Retract (LER-H).

The power amplifier disable latch directly disables the output stage of the actuator driver power amplifier. In addition to being set by the signals which cause an emergency retract, the latch may be clocked to the set state by writing to the actuator driver with Data bus bit D1-H high. This results in a Power Amplifier Disable (PADIS-H) signal being high when the latch is clocked. The microprocessor can therefore disable the power amplifier at any time. The power amplifier disable latch must be cleared by the microprocessor writing to the actuator driver with Data bus bit D1-H low (PADIS-H low). The status of the power amplifier disable is sent to the microprocessor interface as Amplifier Disable (ADIS-H).

The second level of gating is an "OR" function that allows an emergency retract to be triggered by a Latched Emergency Retract (LER-H) or a Power Supply Failure (PSF-H). The third input is a Latching signal (LATC-H) from the switching regulator that prevents the emergency retract from being cleared until it completes the timeout. Note that the Power Supply Fail (PSF-H) signal is included in both levels of gating. This redundancy ensures that an emergency retract will result from any possible combination of power supply failures.

The emergency retract control logic provides drive signals for two relays discussed in the following paragraphs. There are two other outputs: Emergency Retract (ER-H) and Trigger (TRIG). Signal ER-H, sent to the microprocessor as a fault flag, becomes active (high) when an emergency retract occurs and it remains high until cleared by the microprocessor. Signal TRIG is an optically coupled signal to the switching regulator which starts the regulator timing sequence.

1-128. Relay Drivers. Drivers are included in the emergency retract circuitry for two relays located on actuator driver PCA-A2. One relay, a fast-acting reed relay, is used to disable the output stage of the power amplifier upon command from the microprocessor or when an emergency retract is begun. The driver output for this relay is signal Relay 1 Coil (RK1). The other relay is a power relay used to switch the linear motor coil between the power amplifier output and the emergency retract driver output. The driver output for this relay is signal Relay 2 Coil (RK2). The default state of the relays, with no power applied to the relay coils, disables the power amplifier and connects the linear motor to the emergency retract circuit. The control signals for both relay drivers are generated in the emergency retract control logic.

1-129. Switching Regulator. The purpose of the switching regulator is to cause approximately 5 amperes to flow through the linear motor coil for approximately 0.5 second when an emergency retract is received. This guarantees that the heads will unload to the fully retracted position assuming that there is no abnormal restriction of the carriage motion.

1-130. Emergency Retract Driver. The emergency retract driver, located on actuator driver PCA-A2, is a transistor power switching circuit. The input for this circuit is signal Emergency Retract Drive (ERDR), from the switching regulator.

1-131. Emergency Retract Regulator. The emergency retract regulator is located on the heat sink of actuator driver PCA-A2 and produces a voltage approximately 6.8 volts above the -36 Vdc supply. This output voltage, labelled Emergency Retract VCC (ERVCC), is used as a low voltage power supply for the switching regulator circuits.

1-132. SELF TEST. Two self-test outputs are provided in the current command processing circuits. One is analog and the other is digital, and both are derived from the Current Command (CCOM) signal output by the buffer amplifier on PCA-A3.

The analog self-test signal is signal CCOM filtered to a bandwidth of 318 Hz and attenuated to one-half amplitude. This filtering has little effect on the low frequency signals in the linear mode, but in the switching mode the effect is to remove the switching frequency and leave a signal representing the average value of CCOM. After filtering, the analog self-test signal is passed through the analog multiplexer and a buffer amplifier and appears on a line to the microprocessor PCA-A4 labelled Servo Test (SRVTST).

The digital self-test circuit is obtained from CCOM by a self-test window detector circuit on PCA-A3. The self-test window detector thresholds are approximately plus and minus 1.5 volts. If the amplitude of CCOM remains within the +1.5 to -1.5 volt range, the window detector output remains at a constant high level. If CCOM exceeds 1.5 volts in either direction, the window detector output goes low. Thus, the window detector presents a signal to the microprocessor interface which is a constant high level in the linear mode and is a pulse train in the linear mode. The pulse train is low whenever CCOM is commanding the power amplifier to switch on in either direction. The digital self-test signal will enable the processor to determine which operating mode the actuator driver is in, and to measure the switching frequency when in the switching mode. The digital self-test signal is sent to the microprocessor interface circuit on servo PCA-A3.

1-133. SELF-TEST AMPLIFIER. The self-test amplifier, located on PCA-A2, is a simple unity gain inverting amplifier circuit operating on the Actuator Current (ACUR) signal. The amplifier output, labelled Actuator Test (ACTTST), represents the average value of the current in the linear mode. The emergency retract current is also measured as ACTTST.

1-134. POWER SUPPLY FAILURE MONITOR. The power supply failure monitor circuit, located on emergency retract PCA-A20, continually monitors the +5, +12, +36, and -36 volt power supplies to ensure that they remain above minimum acceptable voltages. This is to ensure that power is available to perform emergency retracts, and not to ensure normal operation of the drive.

The outputs of the power supply failure circuits are combined in an "OR" configuration so that a failure of any one or combination of the power supplies will result in the Power Supply Failure (PSF-H) signal going high. This action will trigger an emergency retract.

1-135. HEAD LOADING

The microprocessor interacts with servo PCA-A3, track follower PCA-A9, and actuator driver PCA-A2 to load the heads. A flowchart describing this action is provided in figure 1-8. Head loading occurs after the prehead load portion of the self-test diagnostic has been completed. (The second half of the self-test diagnostic is completed after the heads are loaded.)

Once the motor-spindle assembly reaches its operational speed of 2,700 revolutions per minute, the heads will automatically be loaded. After the microprocessor has concluded that circuit conditions are satisfactory, it starts the initial head loading procedure. First, the necessary conditions are set on servo PCA-A3. This includes setting Seek Off Disc (SKOF-H) low, indicating that the carriage should move toward the center of the media module. Position Control Loop Enable (POSEN-L) is disabled (high) since velocity control will be used. Distance-To-Go Register Clock Enable (DTGEN-H) is disabled (low) so that the desired address can be latched into the DTG register. Long Seek (LNSK-H) is disabled (low) since the drive is not doing a long seek. Velocity Curve Gate Enable (VCGEN-L) is disabled (high) since it is not yet desired to connect the Velocity Command (VC) signal into the servo loop. ROM Address bits 10 and 11 (ROM10-H and ROM11-H) are both low to select a "fast" velocity profile. The DTG register is loaded with a value that selects a zero voltage output from the velocity curve generator.

Next the microprocessor sets track follower PCA-9 for even track selection, opens the carriage back latch, and enables the actuator driver circuitry on PCA-A2.

The microprocessor now starts a timeout count of 50 milliseconds and monitors the Carriage Back (CRB-L) signal and the output of the tachometer on the actuator assembly. At this time, the carriage should still be retracted (CRB-L low) and the tachometer voltage zero. If not, drive error (DERR) 73 is issued.

At the end of the 50-millisecond timeout, the DTG register is loaded with a value that selects a "head load velocity" voltage from the velocity curve generator. Then, after a 10-millisecond interval to allow the carriage to start moving, a timeout count of 90 milliseconds is begun. Again the microprocessor monitors signal CRB-L and the tachometer voltage. If a timeout occurs before CRB-L switches to high (indicating that the carriage has not moved from its retracted position), or the tachometer voltage is not within the proper range, drive errors (DERR's) 74 and 75, respectively, are issued.

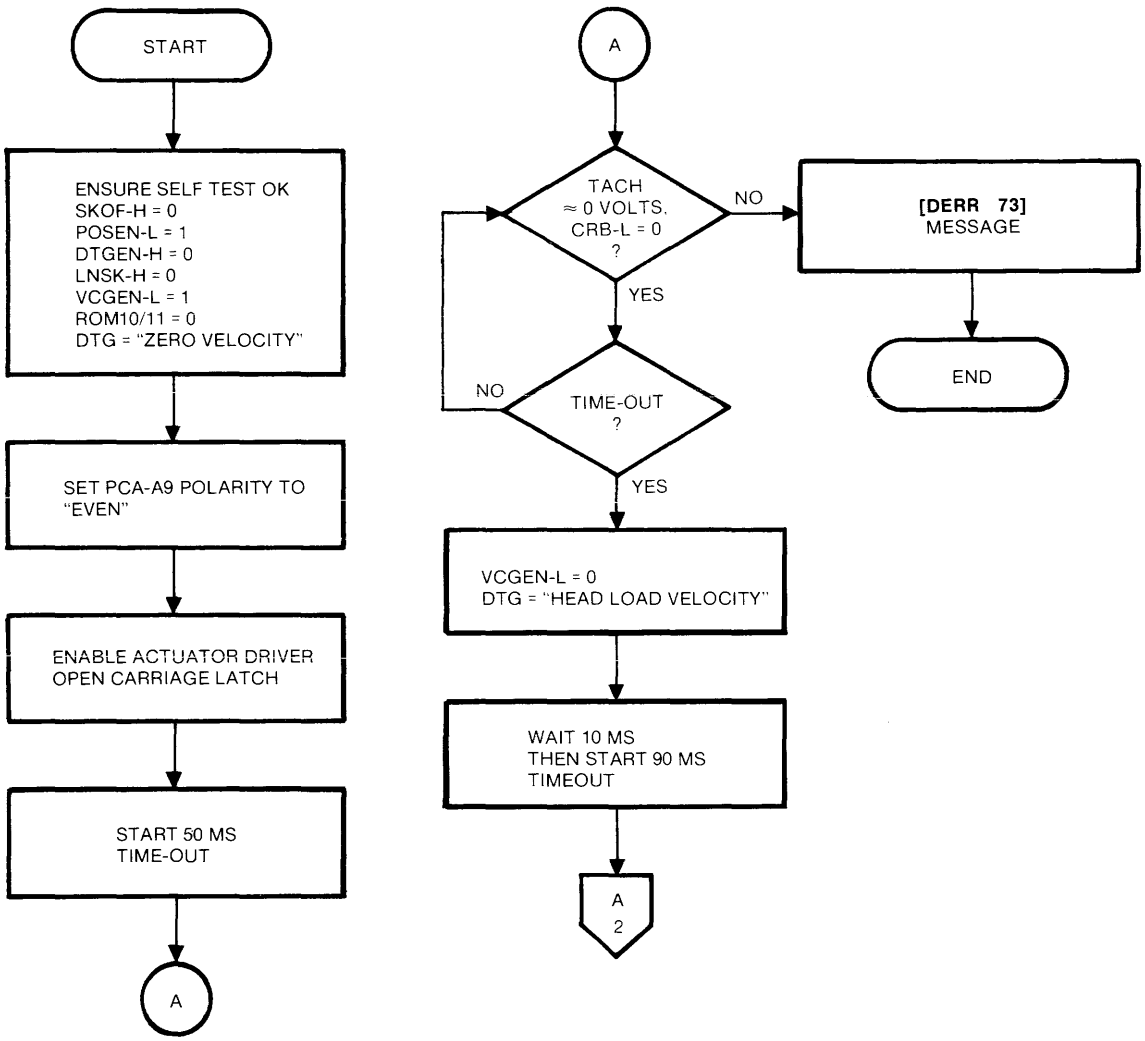


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Figure 1-8. Head Load Flowchart (Sheet 1 of 4)

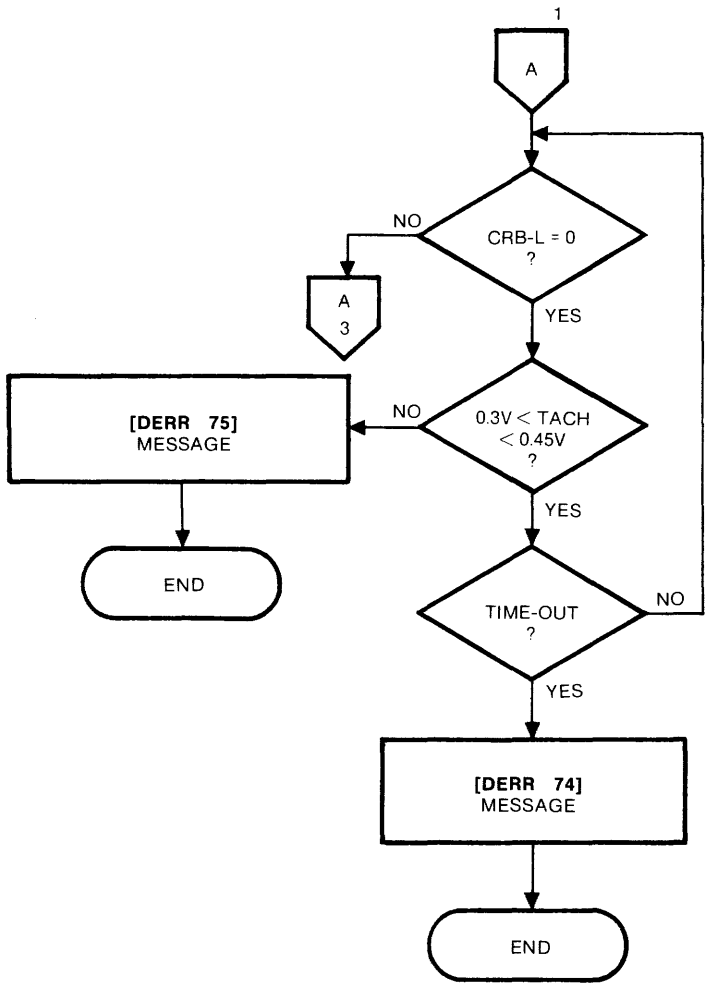

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Figure 1-8. Head Load Flowchart (Sheet 2 of 4)

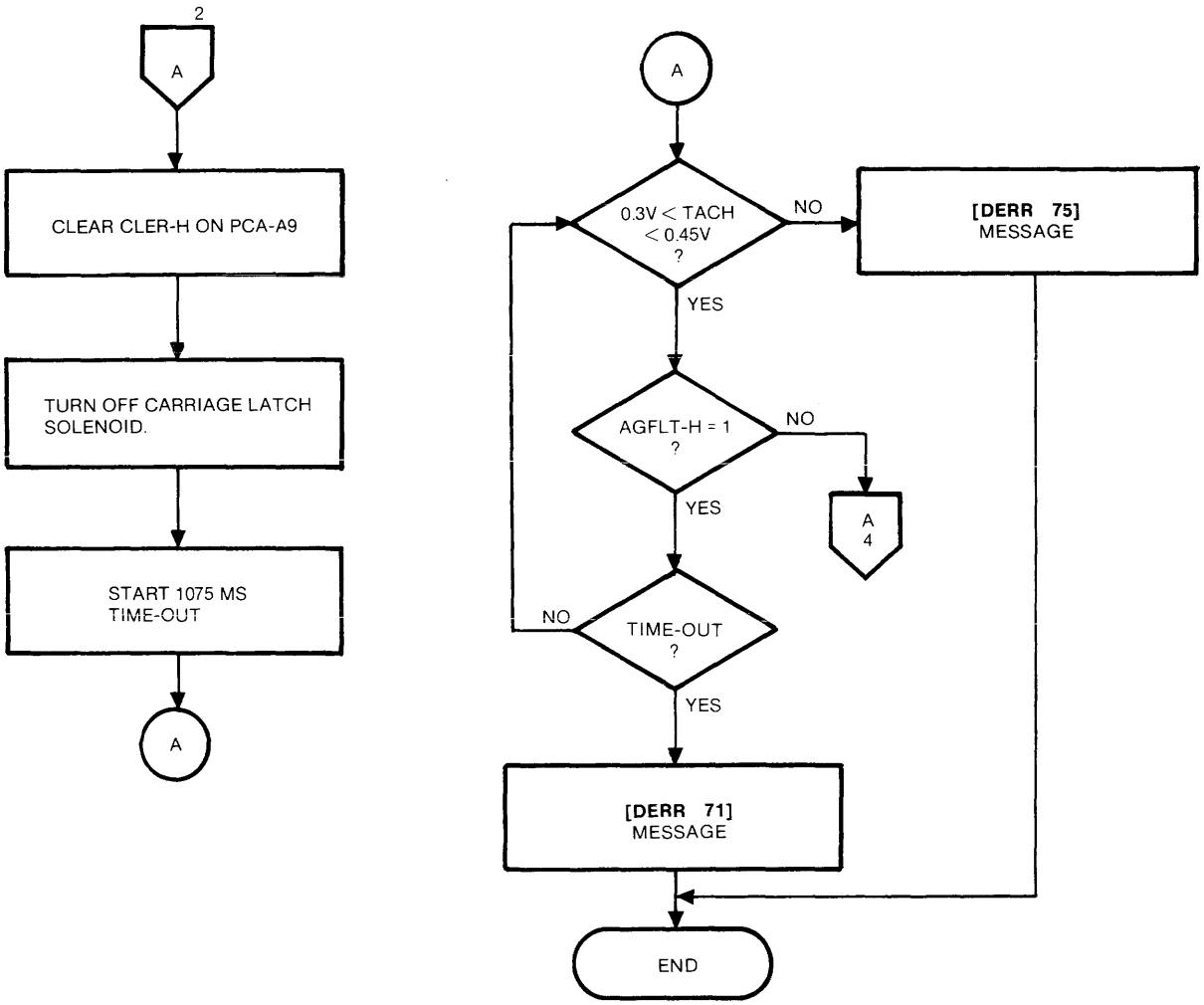

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Figure 1-8. Head Load Flowchart (Sheet 3 of 4)

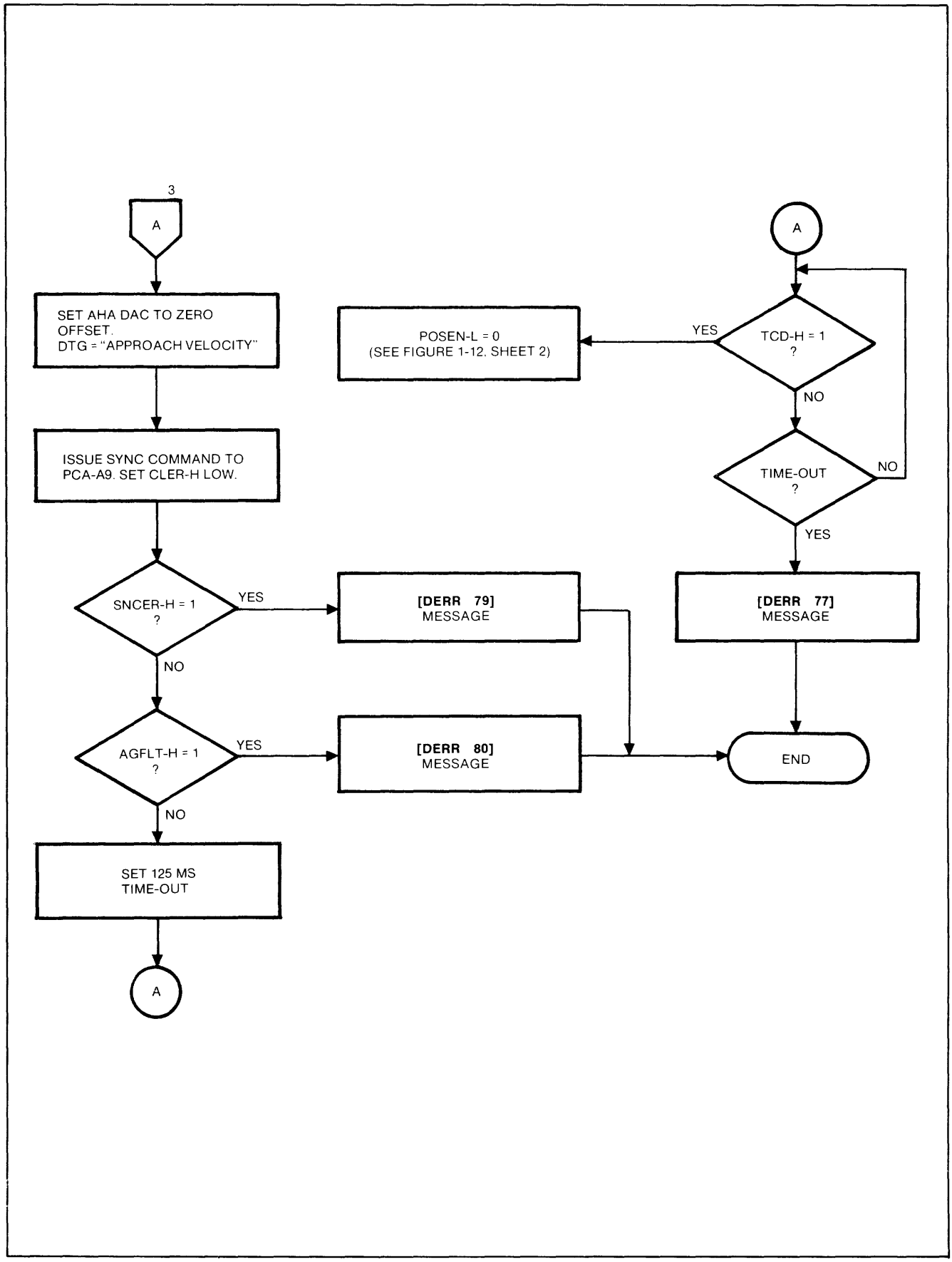

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Figure 1-8. Head Load Flowchart (Sheet 4 of 4)

After verifying that the carriage assembly has moved from its retracted position, the microprocessor holds signal Clear Emergency Retract Latch (CLER-H) on track follower PCA-A9 high and disables the carriage latch solenoid. Next, the microprocessor starts a timeout count of 1,075 milliseconds while monitoring signal AGC Fault (AGFLT-H) and the tachometer voltage. If a timeout occurs before AGFLT-H switches to high, drive error (DERR) 71 is issued. An improper tachometer voltage will trigger a DERR 75 message.

With the heads over the guard band, the auto head alignment DAC is set to zero radial offset and the skew offset is also set to zero. The DTG register is now loaded with a value that selects an "approach velocity" voltage. A sync command (SNCM-L) is now transmitted to track follower PCA-A9 to prepare it for proper dibit decoding. Also, signal CLER-H in track follower PCA-A9 is held low to enable valid AGC fault detection. Proper operation of the track follower is checked by monitoring signals Sync Error (SNCER-H) and AGC Fault (AGFLT-H). Drive errors (DERR's) 79 and 80, respectively, are issued if abnormal conditions are detected.

The microprocessor now starts a 125-millisecond timeout period and monitors signal Track Center Detector (TCD-H) from servo PCA-A3. When TCD-H goes high, signal POSEN-L is set low, switching PCA-A3 to the position loop. The head load operation now performs the automatic head alignment and head settling procedures described for the seek operation (refer to paragraph 1-140). If a timeout occurs before TCD-H goes high, drive error (DERR) 77 is issued.

1-136. HEAD UNLOADING

The microprocessor interacts with servo PCA-A3 and actuator driver PCA-A2 to unload the heads. A flowchart illustrating this interaction is shown in figure 1-9. First, the microprocessor sets Carriage Unlock (CUL-H) low, to ensure that the carriage latch solenoid is de-energized. The microprocessor then sets Seek Off Disc (SKOF-H) high, Long Seek (LNGSK-H) low, Velocity Curve Switch Enable (VCGEN-L) low, Position Control Loop Enable (POSEN-L) high, Distance-To-Go Register Clock Enable (DTGEN-H) low, and Slow Position Signal Enable (SPEN-H) low. This turns on the velocity loop. The DTG register is loaded with a value that selects a "head unload" velocity.

The microprocessor now starts a timeout count of 2 seconds and monitors the Carriage Back (CRB-L) signal. If a timeout occurs before CRB-L goes low, the microprocessor signals drive error (DERR) 87.

When the CRB-L signal goes low, the microprocessor selects a velocity that will move the carriage back to the inner crash pad stops on the actuator. The velocity command chosen causes approximately 6 amperes of current to flow through the actuator, enough to cause the carriage to fully retract. The velocity command is left on for 100 milliseconds.

The microprocessor now sets signal VCGEN-L high, and loads the DTG register with the zero velocity command address. The microprocessor waits for 256 milliseconds to allow the current in the actuator to go to zero and the carriage to stop before turning off the actuator driver.

1-137. RECALIBRATION

Recalibration starts off in the same manner as head unloading. (See figure 1-10.) First the microprocessor sets SKOF-H high, telling the carriage to move toward the edge of the disc. Signals LNGSK-H, VCGEN-L, DTGEN-H, and SPEN-H are set low. Signal POSEN-L is set high. The DTG register is loaded with a "recalibrate" velocity address. If signal ACG Fault (AGFLT-H) is high at this time, drive error (DERR) 81 is issued.

The microprocessor now begins monitoring signals AGFLT-H and TCD-H as the heads move toward the edge of the disc. When it is determined that the heads have reached the edge (no TCD-H signals, AGFLT-H high), signal SKOF-H is set low to reverse the direction of the carriage. If the proper indications are not observed during the timeout intervals shown in figure 1-10, drive error (DERR) 82 is declared. The microprocessor continues to observe signal AGFLT-H and when no fault is indicated, the recalibration operation proceeds to the track zero settling procedure described for the seek operation (refer to paragraph 1-140). Failure to obtain the correct AGFLT-H indication at the end of a 50-millisecond timeout period will result in a drive error (DERR) 71.

1-138. EMERGENCY RETRACT

The microprocessor interacts with actuator driver PCA-A2, servo PCA-A3, and emergency retract PCA-A20 to automatically retract the heads when certain conditions are detected that could cause damage to the heads and/or the media. A flowchart detailing the emergency retract operation is shown in figure 1-11.

An emergency retract is initiated for a master reset, a spindle speed down condition, a power supply failure, or a microprocessor command. Initiation of the emergency retract includes triggering the emergency retract circuitry on PCA's A2 and A20 and activating servo PCA-A3. After a 600-millisecond delay, the microprocessor monitors signal Carriage Back (CRB-L). In the event that the proper indication is not observed, drive error (DERR) 31 is signalled.

1-139. TRACK FOLLOWING

The electronics which are directly involved in track following are track follower PCA-A9, servo PCA-A3, and actuator driver PCA-A2. Track follower PCA-A9 reads the signal from the servo head and converts it into a position error signal. Two signals come from

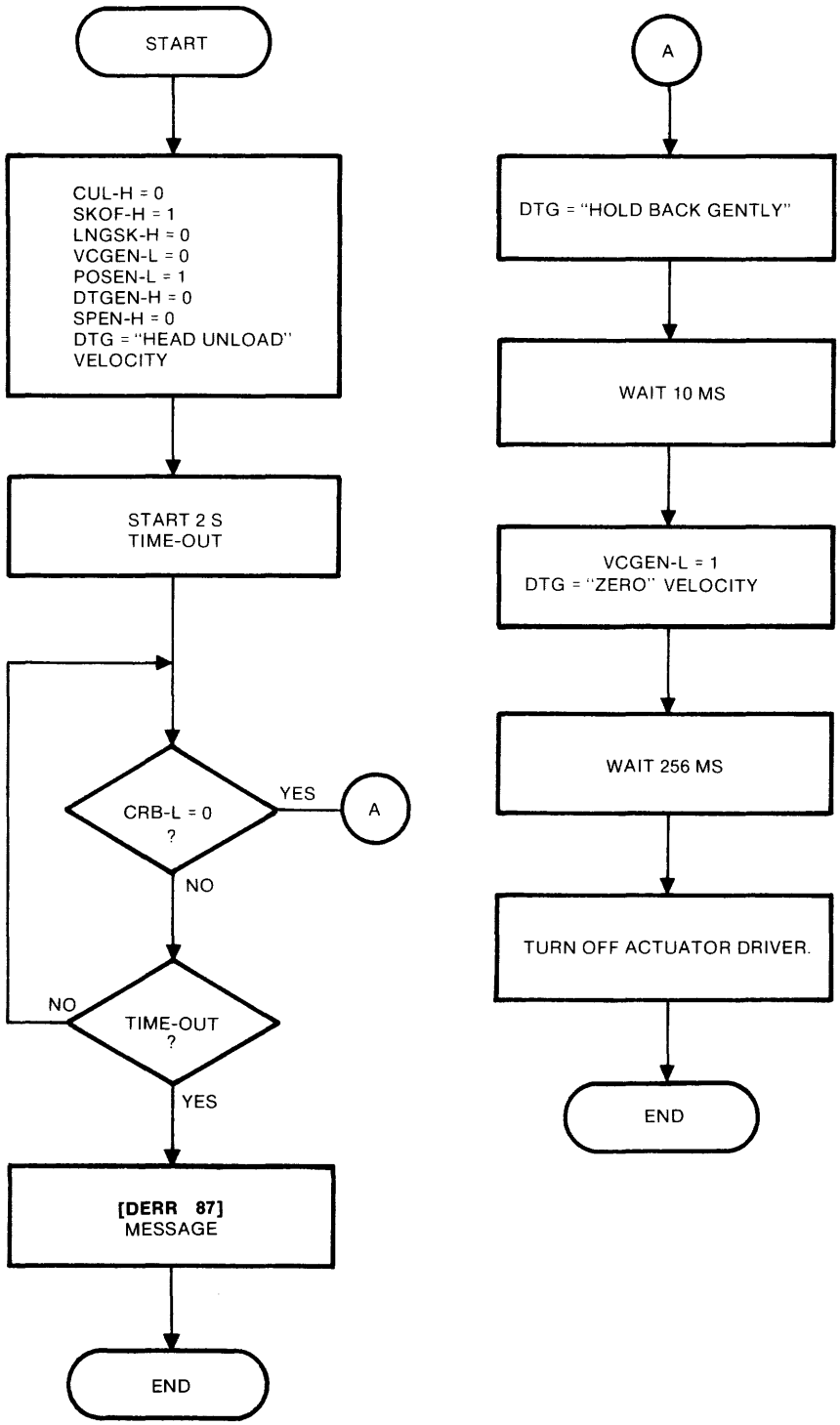

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Figure 1-9. Head Unload Flowchart

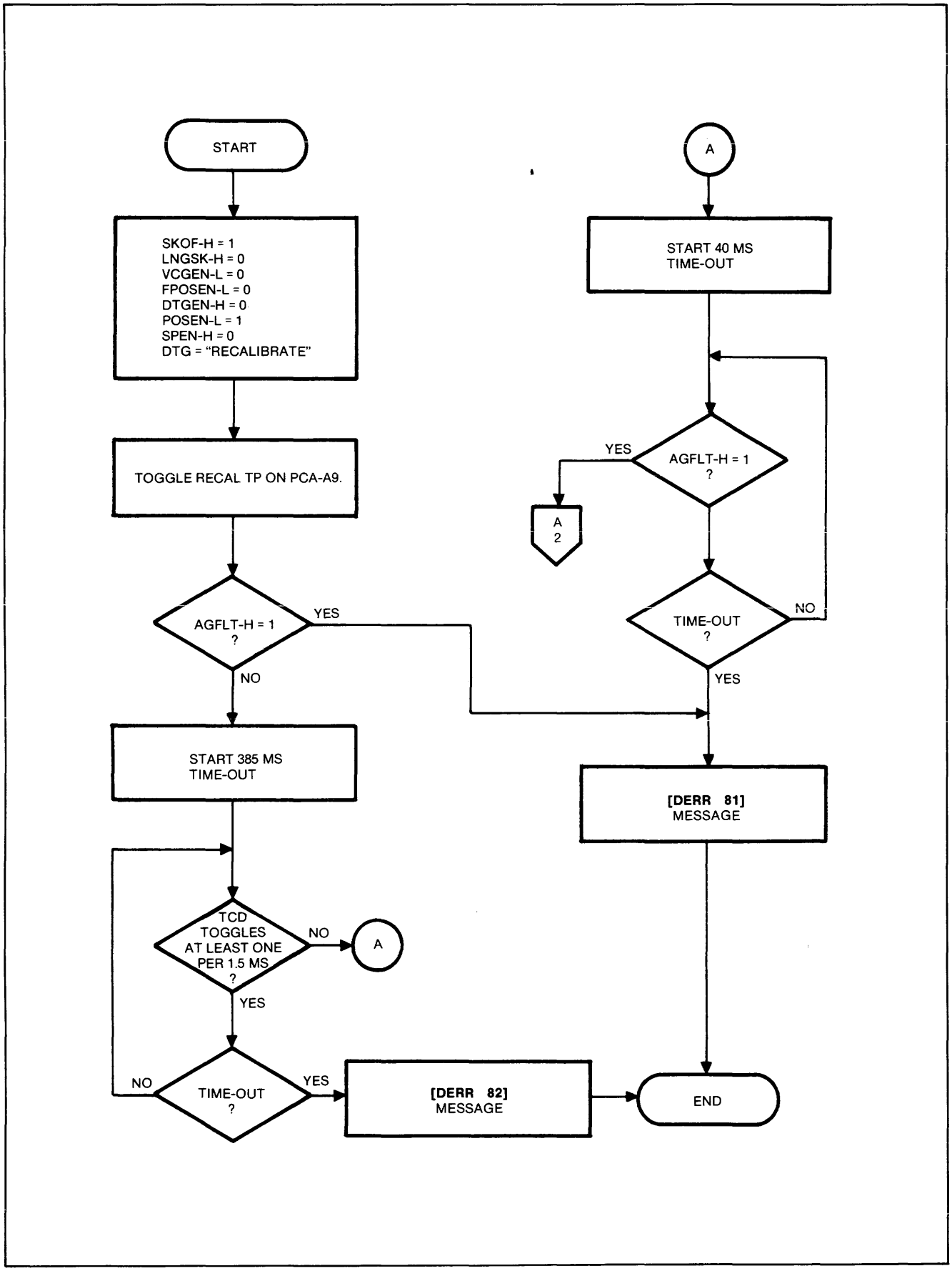

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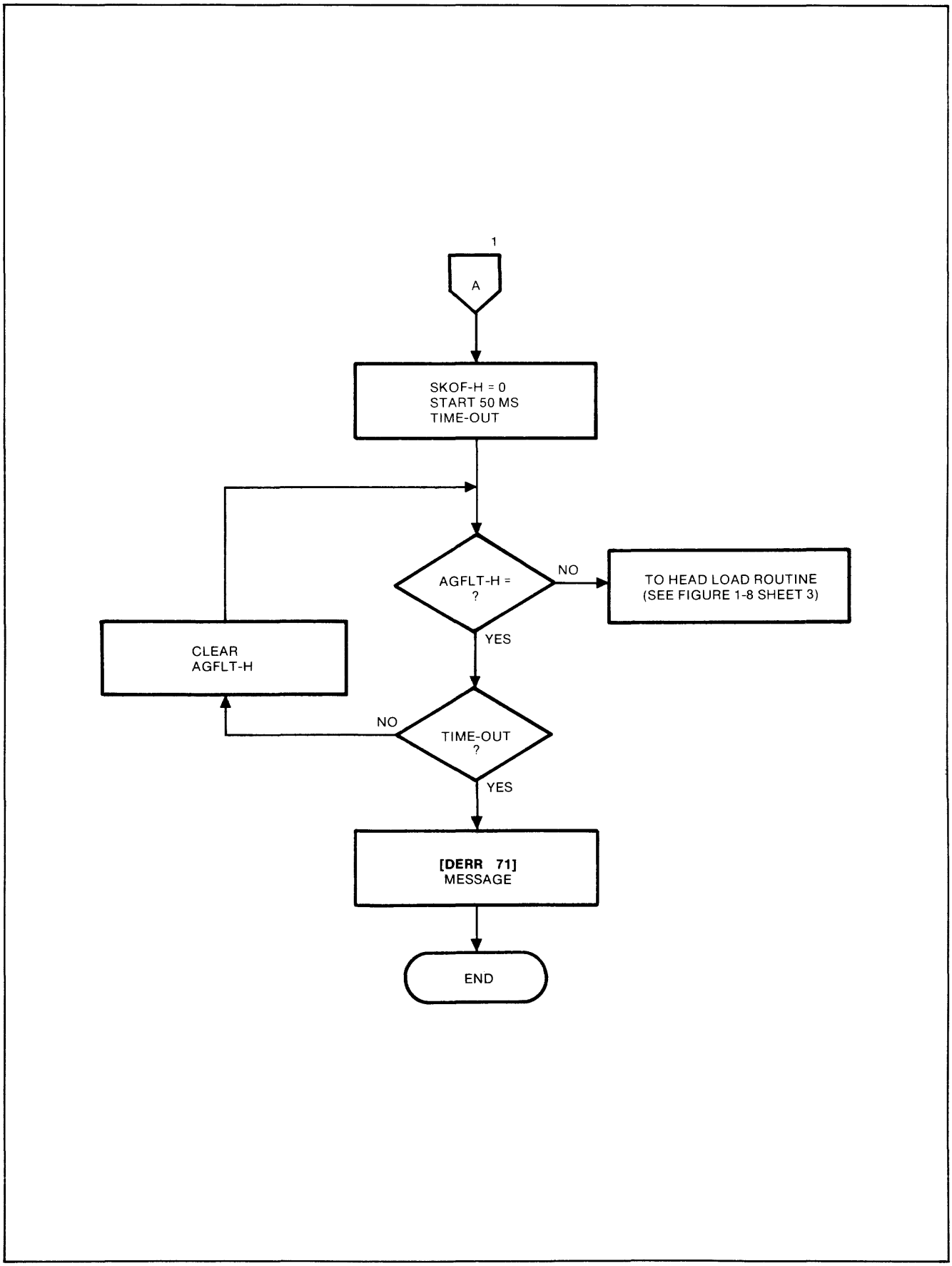
Figure 1-10. Recalibrate Flowchart (Sheet 1 of 2)



7933-355A(2)

Figure 1-10. Recalibrate Flowchart (Sheet 2 of 2)

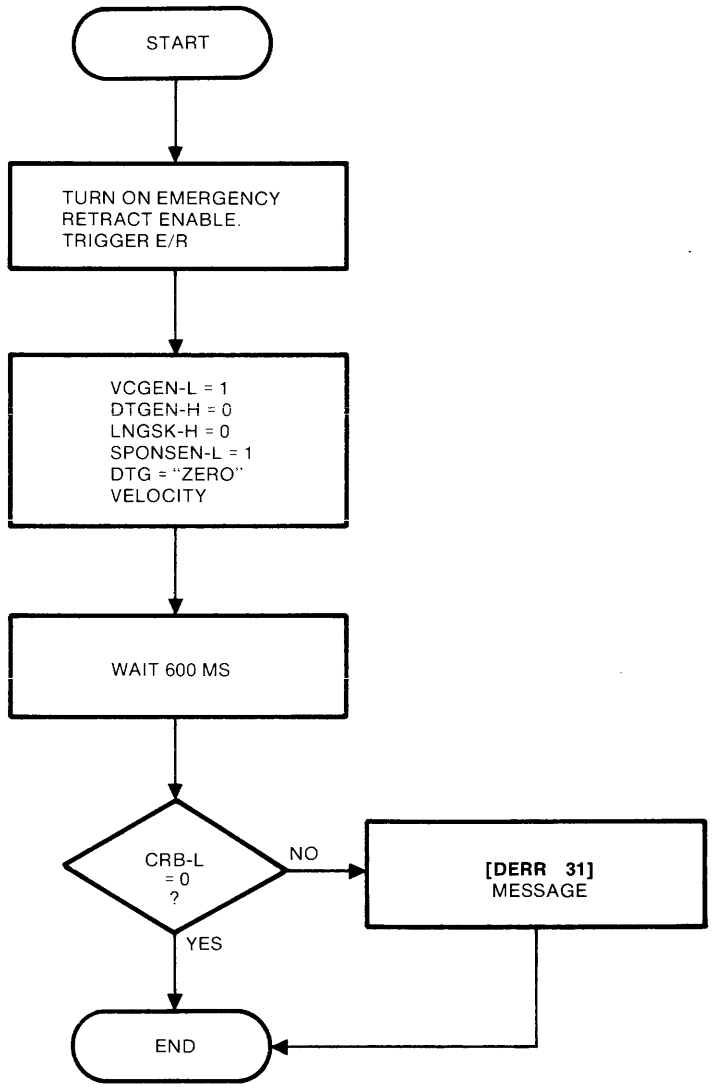


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Figure 1-11. Emergency Retract Flowchart

the track follower PCA. One is the Slow Position (SPOS) signal and the other is the Fast Position (FPOS) signal. The FPOS signal is the normal wide bandwidth position error signal that is used during track-to-track seeks, and while settling on track. The SPOS signal is a slew rate limited version of the error signal and is used during track following.

Actuator driver PCA-A2 converts the low power signal from servo PCA-A3 into a high power signal which drives the actuator. When the drive is following a track, the amplifier is in the linear mode.

Servo PCA-A3 is the point where signals are combined and conditioned to provide the current command signal to actuator driver PCA-A2. The compensation for track following is done by using a single lead/lag network. A low pass filter is also included to minimize the effects of mechanical resonances in the carriage structure.

1-140. TRACK-TO-TRACK SEEKS

The microprocessor interacts with track follower PCA-A9, servo PCA-A3, and actuator driver PCA-A2 to perform seeks. (See figure 1-12.) In general, when the drive is told to do a seek, the microprocessor calculates and stores the length of the seek. If the seek direction is toward the outer edge of the disc, the direction is negative. If the direction is toward the center of the disc, the value is positive. The microprocessor loads the DTG register on PCA-A3 with the correct value and starts the carriage on its way to the desired cylinder. The carriage starts to accelerate toward the target track and continues to accelerate until the carriage velocity intersects the desired velocity curve. While the carriage is accelerating, the microprocessor is calculating the automatic head alignment offset for the target head. Timeouts for acceleration and deceleration are also included. As the carriage moves, the servo head crosses the servo tracks and as each track is crossed, the DTG register is counted down by one. This addresses a new part of the ROM, and the VC output voltage changes accordingly.

The VC output voltage is basically proportional to the square root of the distance to go to the target. When the carriage first starts the seek, the carriage velocity is low, so it accelerates to try and match the command velocity. Once the carriage velocity intersects the commanded velocity, the carriage starts to decelerate. As each track is crossed, the curve is updated and causes the carriage to decelerate at a constant rate.

When the disc drive is doing a seek that is not "long", the plus and minus quarter track crossing detector is used for the entire track. When the disc drive is doing a "long"seek, it uses the track crossings to count down the DTG register for the majority of the seek. When the carriage gets to within five tracks of the target, the DTG value is equal to nine and the plus and minus quarter track crossing is used as the clock. This provides a finer control over the carriage velocity as it approaches the target.

When the DTG gets to the target value for the particular type of seek being performed, it means that the carriage is within three quarter tracks of the center of the target servo track. Since auto head alignment can introduce a plus or minus one-quarter track offset, the final position of the servo head will not necessarily be over the center of the servo track.

Signal TCD-H goes true when the servo head is close enough to its final position for the position servo to be turned on. With signal POSEN-L disabled, signal TCD-H goes high when the servo head is within 240 microinches of the target position. The target position is the center of the servo track, plus the auto head alignment offset.

When the microprocessor sees signal TCD-H go high, it sets signal POSEN-L low. This action enables the position control and disconnects the velocity command curve from the loop. With signal POSEN-L low, the TCD-H window is decreased to 105 microseconds. When the microprocessor enables the position loop, signal TCD-H goes low. The microprocessor now calculates the automatic head alignment values for the rest of the data heads and verifies that the head is on the desired track. Just after the position loop is turned off, the microprocessor reads the least significant bit of the physical track address and properly sets up track follower PCA-A9. The automatic head alignment offset value is looked up for the target head and cylinder, and is output to the servo PCA-A3. The microprocessor then writes to formatter/separator PCA-A8 to select the target head and to select the proper write current.

1-141. READ/WRITE SYSTEM

The read/write system (see figure 1-19) consists of circuits on read/write PCA-A10, formatter/separator PCA-A8, and disc memory access (DMA) PCA-A6. Read/write PCA-A10 also includes an automatic head alignment module which is part of the head positioning system. The purpose of the read/write system is to provide, under microprocessor control, the means to read information from or write information onto the data surfaces of the media module. In addition, the read-write system includes self-test circuitry that permits the microprocessor to monitor operation of the system. Included in the following paragraphs are descriptions of the circuitry on each of the three PCA's followed by a functional description of the read/write system. Refer to table 1-5 for a description of the mnemonics used in figure 1-19. In the "source" column of table 1-5, the numbers in parentheses following the PCA reference designations identify the functional block diagram locations of the PCA's.

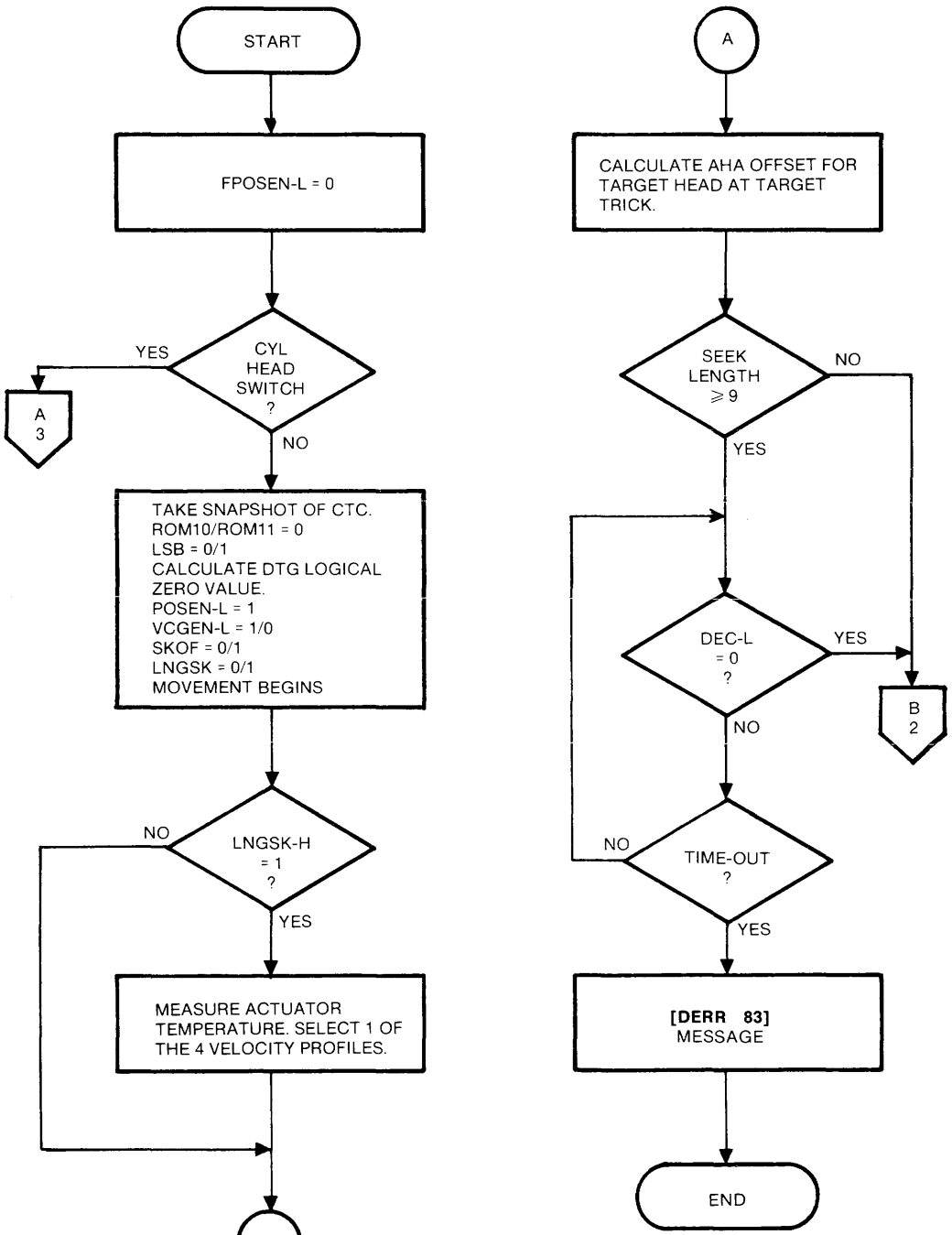

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Figure 1-12. Seek Flowchart (Sheet 1 of 3)

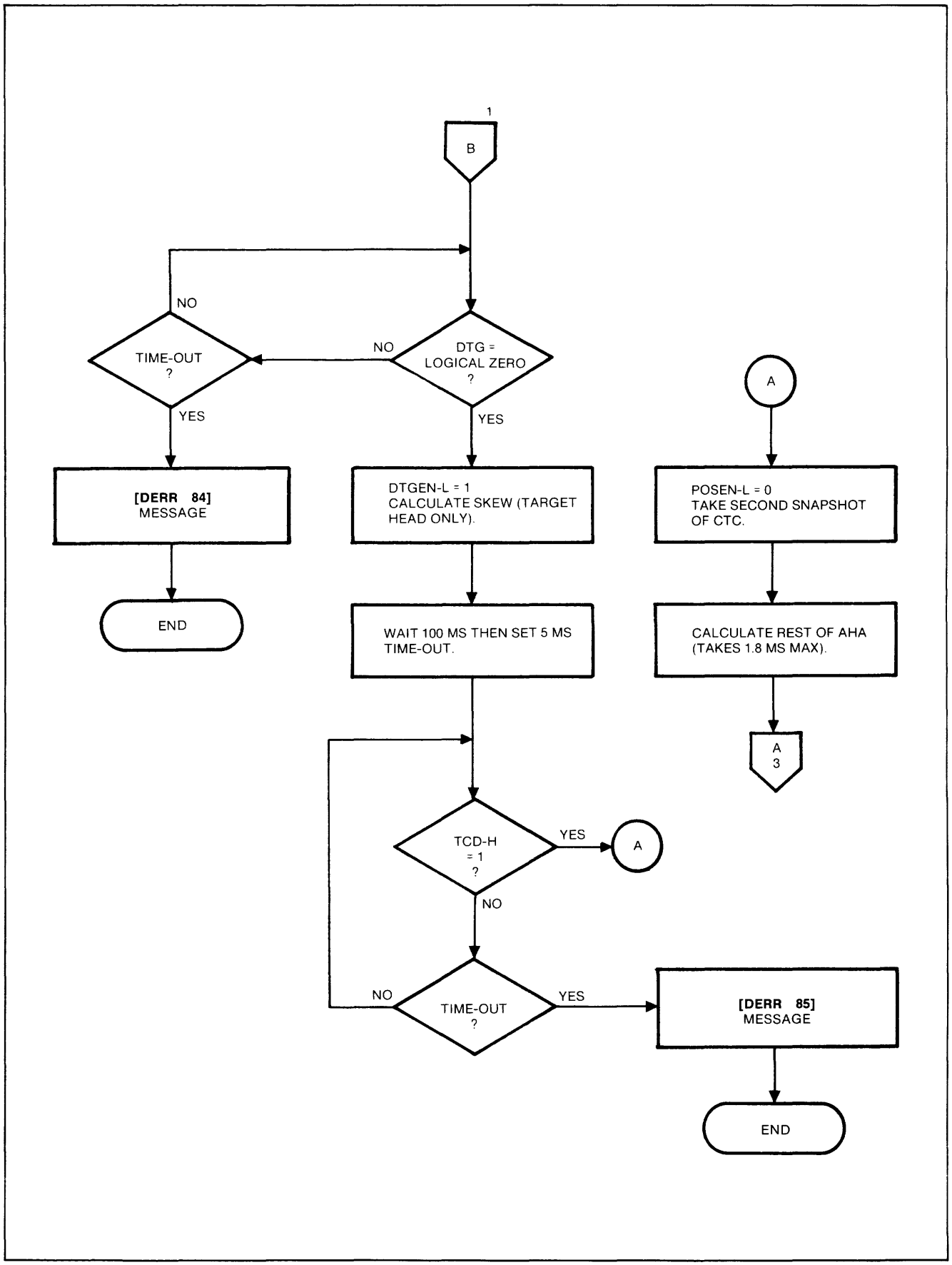

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Figure 1-12. Seek Flowchart (Sheet 2 of 3)

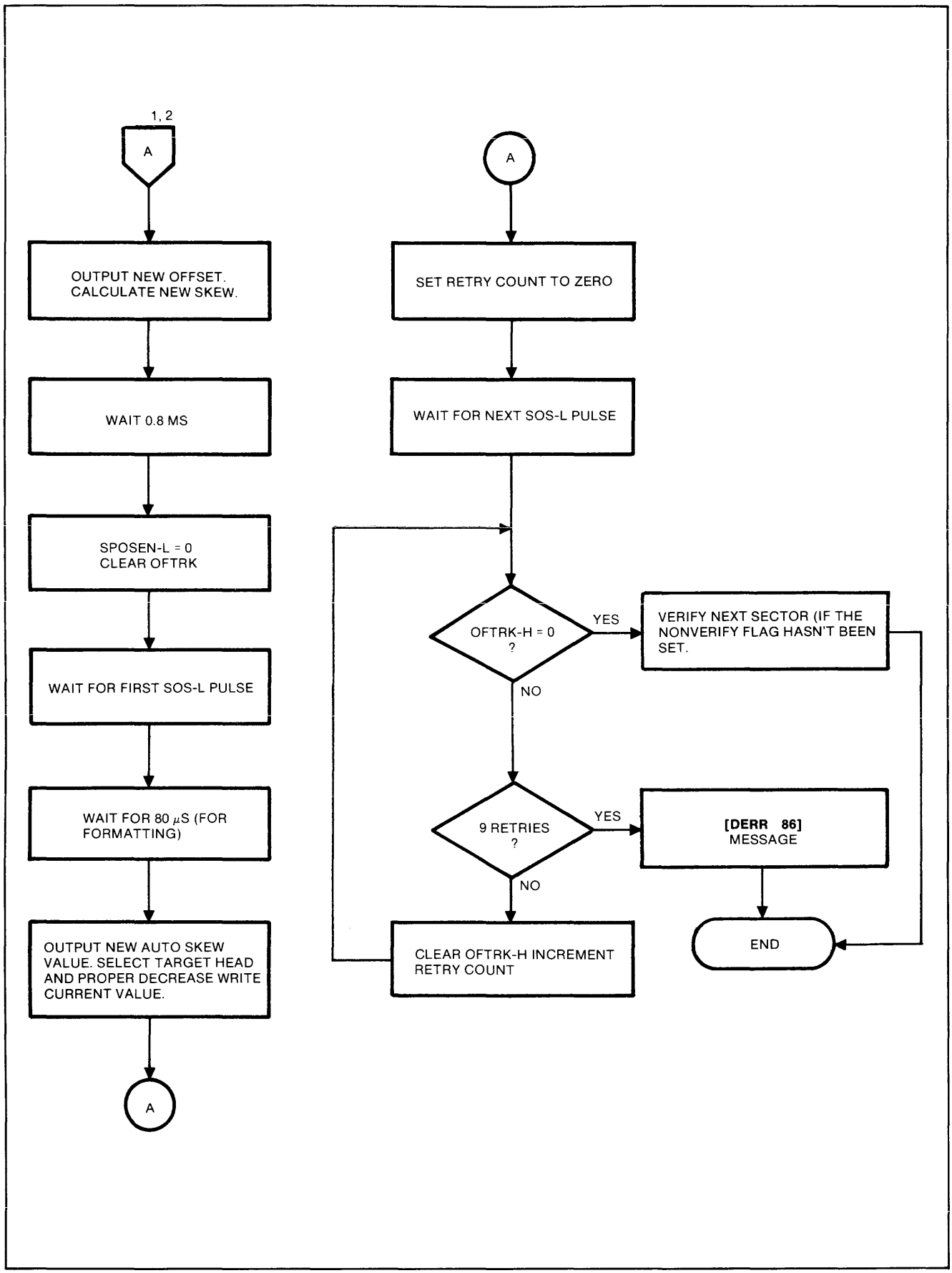

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Figure 1-12. Seek Flowchart (Sheet 3 of 3)

Table 1-5. Read/Write Mnemonics

MNEMONIC	DEFINITION	SOURCE	FUNCTION
A0-H thru A11-H	Address Bus, Bits 0 thru 11	PCA-A4 (1)	Microprocessor Address bus, bits 0 through 11.
ADR0-H thru ADR2-H	Address	PCA-A17 (5)	HP-IB channel address programming lines from HP-IB channel select switch on PCA-A17.
ATN-L	Attention	PCA-A17 (5)	An HP-IB management interface line. ATN-L causes all devices to interpret data on the bus as a controller command and activate this acceptor handshake function (command mode) or data (data mode) between addressed devices.
BF1SL-L	Buffer 1 Select	PCA-A4 (1)	DMA no. 1 buffer select line.
BR0-H thru BR7-H	Board Register, bits 0 thru 7	PCA-A10 (5)	Output lines from board revision register on PCA-A-10 to microprocessor interface on PCA-A8. Signals allow microprocessor to sense state of certain control signals on PCA-A10.
CRB-L	Carriage Back	PCA-A18 (4)	Signal indicating that carriage is fully retracted into the actuator assembly.
CS	Current Source	PCA-A10 (1)(5)	Analog test signal from write path current source. Signal is sent to microprocessor PCA-A4 via analog multiplexer.
D0-H thru D7-H	Data Bus, bits 0 thru 7	PCA-A4 (1)	Microprocessor bidirectional data bus, bits 0 thru 7.

Table 1-5. Read/Write Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
DAV-L	Data Valid	PCA-A17 (5)	Bidirectional HP-IB handshake line. DAV-L indicates that the data on the DIO lines is stable and available to be accepted by the receiving device.
DCP-H	Data Clock Pulse	PCA-A10 (5)	Data clock pulses sent directly to head positioning system for use in the automatic head alignment circuitry.
DCNW-H	DC with no Write	PCA-A10 (5)(4)	Output of read/write fault detect logic indicating that the write current source has stayed on during a write.
DIN-H	Data In	PCA-A6 (5)	Serial read data line.
DIO1-L thru DIO8-L	HP-IB Data Bus, bits 1 thru 8	PCA-A17 (5)	Bidirectional I/O lines used for transfer of data, commands and other messages between the host computer and the disc drive. Transfer is byte serial, bit parallel.
DM1SL-L	DMA no. 1	PCA-A4 (1)	DMA no. 1 register select.
DOUT-H	Data Out	PCA-A6 (5)	Serial data out (that is, enroute to R/W or ECC).
DSOS-L	Delayed Start of Sector	PCA-A8 (5)	Microprocessor interface output to AGC circuitry on PCA-A10. Signal provides the timing for the amplitude sample circuit.
DVSEL-H	Drive Select	PCA-A8 (5)(1)	Microprocessor interface output setting PCA-A8 and PCA-A10 to their operating states.
EC1SL-L	ECC no. 1 Select	PCA-A4 (1)	DMA no. 1 ECC select line.

Table 1-5. Read/Write Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
EOI-L	End or Identify	PCA-A17 (5)	HP-IB control signal used to indicate the end of a multiple byte message on the bus. EOI is also used for parallel polling.
EOS-L	End of Sector	PCA-A8 (5)	Resets the encoder on PCA-A8 at the end of sector.
ER-H	Emergency Retract	PCA-A2 (4)	Signal indicating that an emergency retract has occurred. ER-H is used by fault detect logic on PCA-A10 to deselect heads.
FCLR-L	Fault Clear	PCA-A8 (5)	Clear signal for fault detect logic on PCA-A10.
FIN-H	Formatter/ Separator Input	PCA-A6 (5)	Data output from ECC module on PCA-A6 to input of formatter/ separator PCA-A8.
FLT-H	Fault	PCA-A10 (5)	Drive fault detect output causing head select logic to ignore head selection inputs and deselect all heads if a drive fault occurs.
FLW-L	Follow	PCA-A8 (5)	Microprocessor interface output used to read head alignment offset value from PCA-A10.
FOUT-H	Formatter/ Separator Output	PCA-A8 (5)	Data output from formatter/separator to ECC module on PCA-A6.
FSSEL-L	Formatter/ Separator Select	PCA-A4 (1)	Formatter/Separator PCA-A8 select line.
FUNER-L	Formatter/ Separator Uncorrectable Error	PCA-A8 (5)	Indicates that an error occurred in the R/W PCA after a disc sector has begun transfer.

Table 1-5. Read/Write Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
FWAVE	Full Wave	PCA-A10 (5)	Analog test signal from full-wave rectifier in read path. Signal is sent to PCA-A4 via analog multiplexer on PCA-A10.
HAEN-H	Head Alignment Enable	PCA-A8 (5)	Microprocessor interface output to automatic head alignment circuitry on PCA-A10.
HAGV	Head Alignment Position Voltage	PCA-A10 (5)	An analog signal from automatic head alignment module indicating how far data head is from track center. Signal is sent to PCA-A4 via the analog multiplexer on PCA-A10.
HS0-H thru HS3-H	Head Select, bits 0 thru 3	PCA-A8 (5)	Microprocessor interface output to head select logic on PCA-A10.
IFC-L	Interface Clear	PCA-A17 (5)	HP-IB general management line used by the system controller to halt all current operations on the bus, unaddress all other devices, and disable serial poll.
IO1SL-L	I/O no. 1 Select	PCA-A4 (1)	DMA no. 1 PHI Select line.
LSB-H	Least Significant Bit	PCA-A8 (5)	Microprocessor interface output to automatic head alignment module on PCA-A10.
MA0-H thru MA2-H	Multiplex	PCA-A8 (5)	Microprocessor interface output controlling selection of signals input to analog MUX. Multiplexer output (RWTST) is coupled directly to PCA-A4.

Table 1-5. Read/Write Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
MHF-H	Multiple Head Fault	PCA-A10 (5)	Output of read/write fault detect logic indicating that the head select circuitry has selected more than one head at a time.
MRST-L	Master Reset	PCA-A1 (6)	Master power on reset.
NDAC-L	Not Data Accepted	PCA-A17 (5)	A bidirectional HP-IB handshake line. NDAC-L indicates to the transmitting device that data has been accepted by the receiver.
NMI-L	Non-Maskable Interrupt	PCA-A4 (5)	Interrupt line tied to non-maskable interrupt of the microprocessor.
NRFD-L	Not Ready for Data	PCA-A17 (5)	A bidirectional HP-IB handshake line indicating that a device is ready for data.
OFTRK-H	Off Track	PCA-A9 (4)	Off track fault flag used by PCA-A10 to deselect the heads.
OUTTST	Output Test	PCA-A10 (5)	Analog test signal from 67-nanosecond one-shot representing read path self-test result. Signal is sent to PCA-A4 via analog multiplexer on PCA-A10.
PRE+, PRE-	Preamplifier +, -	PCA-A10 (5)	PCA-A10 read path outputs to automatic head alignment module.
RD-L	Read	PCA-A4 (1)	Microprocessor read command.
RDD-H	Read Data	PCA-A10 (5)	Output of PCA-A10 read path. Signal is input to PCA-A8 for further processing.

Table 1-5. Read/Write Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
REN-L	Remote Enable	PCA-A17 (5)	HP-IB control line used by system controller to enable bus compatable instruments to respond to commands from the controller or another talker.
RWBR-L	Read/Write Board Revision Register	PCA-A8 (5)	Microprocessor interface output enabling board revision register on PCA-A10.
RWC-L	Read/Write Clock	PCA-A8 (5)	Read/write clock used to clock in serial data during disc operations.
RWFLT-H	Read/Write Fault	PCA-A10 (5)	Read/write fault flag from fault detect logic on PCA-A10. Signal is sent directly to microprocessor PCA-A4.
RWTST	Read/Write Test	PCA-A10 (5)	Output of analog multiplexer on PCA-A10. Signal is sent directly to microprocessor PCA-A4.
SHAV	Sampled Head Alignment Voltage	PCA-A10 (5)	Automatic head alignment signal from AHA module on PCA-A10. Signal is sent to PCA-A4 via analog multiplexer on PCA-A10.
SOD-L	Start of Data	PCA-A8 (5)	Output signal from the encoder on PCA-A8 indicating the start of data in a sector.
SOS-L	Start of Sector	PCA-A8 (5)	Indicates that a sector on the disc is about to begin. Comes a little before SOD-L.
SRQ-L	Service Request	PCA-A17 (5)	HP-IB management line. SRQ-L alerts the controller to a need for communication.

Table 1-5. Read/Write Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
ST-H	Self Test	PCA-A8 (5)	Microprocessor interface output to self test signal generator on PCA-A10.
STO-L	Self Test Offset	PCA-A8 (5)	Microprocessor interface output to self test signal generator on PCA-A10.
TDCP-L	Self Test Data Clock Pulse	PCA-A8 (5)	Microprocessor interface output used to self test data clock pulse decoder on PCA-A10.
TFFLT-H	Track Follower Fault	PCA-A9 (4)	Track follower PCA-A9 fault flag. Signal is listed by PCA-A10 to deselect the heads, in the event of a read/write fault.
UNER-L	Uncorrectable Error	PCA-A6 (5)	Indicates that the ECC was unable to correct the data error in the sector just begun.
WC0-H thru WC2-H	Write Current, Bits 0 thru 2	PCA-A8 (5)	Microprocessor interface output to write current reduction circuit on PCA-A10.
WDD-H	Write Data to Disc	PCA-A8 (5)	Write data signal from formatter/separator PCA-A8 input to write path on read/write PCA-A10.
WDIS-L	Write Disable	PCA-A8 (5)	Microprocessor interface output that allows the microprocessor to disable a write operation in cases where PCA-A10 stayed in the write mode when it should have switched back to the read mode.

Table 1-5. Read/Write Mnemonics (continued)

MNEMONIC	DEFINITION	SOURCE	FUNCTION
WEN-L	Write Enable	PCA-A8 (5)	Microprocessor interface output controlling whether the write operation will allow data to pass to PCA-A10. When WEN-L is active (low), read mode is preset at start of sector.
WENC-L	Write Current Enable Current Source	PCA-A8 (5)	Microprocessor interface output to write current source on PCA-A10. Signal enables write current source when active (low).
WNAC-H	Write with no AC	PCA-A10 (5)	Output of read/write fault detect logic indicating that a selected head is not connected or has an open or shorted winding.
WNDC-H	Write with no DC	PCA-A10 (5)	Output of read/write fault detect logic indicating that a write command is issued but no write current results.
WR-L	Write	PCA-A4 (1)	Microprocessor write command.
WRT-L	Read/Write	PCA-A8 (5)	An interval signal on the formatter/separator PCA-A8 which enables the encode mode of operation.
4MHz-H	4-MHz Clock	PCA-A4 (1)	4-MHz self test clock signal used by PCA-A10 for self test purposes.

1-142. READ/WRITE PCA-A10

In the read mode, PCA-A10 changes the readback signals caused by flux transitions on the disc into a series of pulses. These signals are sent to formatter/separator PCA-A8 for decoding and further processing. In the write mode, PCA-A10 changes the write data from formatter/separator PCA-A8 into alternating flux transitions coincident with the incoming data to be written on the disc. Circuit functions on PCA-A10 include head select, a read path, a write path, automatic head alignment, fault detection, self test, and a power supply. Each of these functions is discussed in the following paragraphs.

1-143. HEAD SELECT. The head select circuitry uses a diode array and 14 switching transistors to allow selection of any one of the 13 data heads for connection to the read, write, or automatic head alignment circuits on PCA-A10. The fourteenth head select circuit is used for a self-test signal source. Injection of the output of the self-test signal generator at this point allows all of the read/write chain to be tested as if the signal was generated by a data head. Head selection is performed by microprocessor interface output signal Head Select, bits 0 through 3 (HS0-H through HS3-H) from formatter/separator PCA-A8. Additional head select codes provide for intentional selection of two heads simultaneously (to test the multiple head fault detection circuitry) and deselection of all heads. Signal Fault (FLT-H) from the fault detect logic causes the head select circuit to ignore selection inputs and immediately deselect all heads if a read/write fault occurs, except when PCA-A10 is in a self-test mode.

1-144. READ PATH. The circuits comprising the read path on PCA-A10 are discussed in the following paragraphs.

1-145. Isolation Transistors. The data signal from the heads is coupled through the select diodes to the input of the first data amplifier by two field-effect transistors. These transistors provide isolation during writes so that clipping is prevented and currents in the read amplifier first stage are controlled.

1-146. Data Amplifier. The first data amplifier is a discrete differential cascode amplifier with emitter degeneration to control gain and increase the input impedance of the stage. Two resistors at the amplifier inputs provide controlled loading on the heads.

1-147. Video Amplifier. A video amplifier following the discrete data amplifier acts as a buffer. This amplifier has five parallel resistors that may be clipped for a 16 value binary sequence of gains to compensate for production variations in gain of the other fixed gain stages. This setting assures that the AGC stage is maintained within its dynamic range over the full range of expected head-media conditions. The low impedance outputs of the buffer drive the data filter.

1-148. Data Filter. The data filter provides the proper group delay of frequency to match the read path and to provide proper timing of the read data. The filter also attenuates signals at frequencies higher than signal frequencies from the media.

1-149. Automatic Gain Control Amplifier. The automatic gain control (AGC) amplifier following the data filter is a second video amplifier with a field-effect transistor serving as a gain setting element.

Automatic gain control is accomplished by feeding back the sampled amplitude of the sync field from each sector (unless it is being written). Signal Delay Start of Sector (DSOS-L) from formatter/separator PCA-A8 provides the timing for the amplitude sample. A one-shot provides an 8-microsecond sampling pulse to a field-effect transistor analog switch. This transistor couples the full-wave rectified data signal from the sync field to the input of an operational amplifier integrator. This integrator (read AGC amplifier) provides the signal to control the gain of the AGC video amplifier stage and also provides the analog memory function between samples and during writes.

1-150. Current Buffer. The data signal output of the AGC amplifier is additionally buffered by a monolithic transistor array. A Darlington pair in the array is used to provide the bias voltage for a pair of emitter followers (also in the array). The array buffers the data signal and establishes a dc level of about one diode drop above ground. The emitter followers drive a full-wave rectifier circuit for the read path and a video amplifier buffer for the signals to the head alignment circuit.

1-151. Full-Wave Rectifier. The full-wave rectifier circuit consists of a pair of Schottky diodes with a resistive load to -6.8 volts. The output of the full-wave rectifier drives the AGC circuit, the amplitude qualification circuit, and the differentiator. A test output labelled Full-Wave (FWAVE), is made available to microprocessor PCA-A4 via the analog multiplexer.

1-152. Differentiator. The differentiator stage consists of a passive RC differentiator followed by a video amplifier to restore the amplitude lost in the differentiator. The video amplifier output drives one-half of a dual high-speed sample-and-hold comparator and thus determines the trigger points for the 67-nanosecond output one-shot.

1-153. Amplitude Qualification. The amplitude qualification circuit compares the amplitude of the data signal against a fixed reference voltage and qualifies (allows) outputs from the differentiation sample-and-hold comparator only when the amplitude of the data signal is above the reference. This is accomplished by placing the differentiator's comparator section in the hold mode when the signal amplitude is below the qualification level. Qualification eliminates output pulses which would otherwise result from the low amplitude peaks in the data signal during the shouldering periods and at times between widely spaced data pulses. If the differentiated signal crosses zero in the negative direction while the undifferentiated signal is above the reference level, the dual sample-and-hold comparator output generates a negative transition on the positive output (which should correspond to a positive or negative peak in the data signal from the head). This transition triggers a 67-nanosecond one-shot which produces the Read Data (RDD-H) signal output for the read path. Read Data RDD-H is sent to formatter/separator PCA-A8 for decoding. A test output from the one-shot, labelled Output Test (OUTTST) is made available to microprocessor PCA-A4 via the analog multiplexer.

1-154. WRITE PATH. The circuits making up the write path on PCA-A10 are described in the following paragraphs.

1-155. Write Toggle Flip-Flop. Write Data (WDD-H) signal from formatter/separator PCA-A8 is divided by two (in frequency) by the write toggle flip-flop. This flip-flop alternately switches the write driver transistors on and off. One of these transistors causes a positive transition in the applied magnetic field at the media, and the other transistor causes a negative transition.

1-156. Write Current Source. The write current source determines the amplitude of the current which is applied to the head and thus it sets the magnetic field strength of the media. A test output, labelled Current Source (CS), is made available to microprocessor PCA-A4 via the analog multiplexer.

1-157. Write Current Reduction. The write current reduction circuit allows the nominal current to be reduced under microprocessor control by Write Current, bits 0 through 2 (WC0-H through WC2-H) so that the field strength can be optimized for different radial positions across the disc.

1-158. AUTOMATIC HEAD ALIGNMENT MODULE. Automatic head alignment is accomplished by measuring the constant offset needed to exactly straddle a pair of head alignment bands which are prerecorded on the data surface. Three sets of bands are recorded on each surface, and offsets are determined for each set. The microprocessor uses these three measurements per surface to define a profile of head alignment offsets which are then used for subsequent read/write operations. The circuit that measures the dynamic head misalignment in a radial position (offset) is located on PCA-A10. Simultaneously, an auto skew adjustment is made by comparing timing of circumferential codes in the servo track (on the servo surface) and the head alignment tracks (on the data surface). The circumferential position (skew) measurement is determined by circuitry located on track follower PCA-A9. A table is built in microprocessor memory to allow adjustment for the measured skew across the surface. The head alignment process is invoked to update the tables when any one of the following events occurs: a) a specified number of errors has occurred in reading data, b) the temperature inside the disc drive has changed a specified amount since the last head alignment, c) power up of the disc drive, or d) a predetermined time interval has elapsed. Additional information about automatic head alignment, including a description of the skew measurement circuitry, is provided in paragraph 1-89.

The head alignment module on PCA-A10 consists of four main sections described as follows.

1-159. Phase Locked Loop. The phase locked loop synchronizes with the signals from the auto head alignment bands on the data surfaces.

1-160. Clock Generator. This is a ROM derived clock generator which is driven by the locked voltage-controlled oscillator of the phase locked loop. The generator provides all timing functions for head alignment.

1-161. Head Alignment Offset Detector. The head alignment offset detector consists of a sensitive full-wave integrate-and-dump discriminator which derives an offset error signal for the microprocessor and an AGC signal for the read path AGC amplifier. The microprocessor issues servo offset commands to null the error signal from the head alignment offset detection circuit. Therefore, neither calibration nor linearity of the error signal is critical to the accuracy of the automatic head alignment process.

1-162. Data Clock Pulse Decoder. The data clock pulse decoder determines the presence of index pulses embedded in the head alignment bands. These pulses are compared, on the track follower PCA-A9, to references from the servo surface to determine the amount of timing shift necessary to correct sector skew. This correction compensates for alignment errors between heads in the direction perpendicular to the actuator motion.

1-163. FAULT DETECTION. Four read/write faults are detected by the fault detect logic and the multi-head fault detector on PCA-A10. These are write with no ac, write with no dc, dc and no write, and multihead.

1-164. Write With No AC. The write with no ac fault occurs if the selected head is not connected or has an open or shorted winding. In this case, during a write, the normal feedback from the head is missing. Write with no ac also occurs if the write toggle flip-flop fails, or formatter/separator PCA-A8 fails to send data to read/write PCA-A10 after a write operation has been initiated. Thus, the write with no ac fault checks to ensure that data is actually written during every write operation. This fault should detect dc erasure of data and should immediately switch off the heads to prevent continued erasure of data.

1-165. Write With No DC. The write with no dc fault occurs when a write command is issued, but no write current results. The write with no dc fault may be caused by writing with no head selected, or it may be caused by circuit failures in the write current source on read/write PCA-A10.

1-166. DC And No Write. The dc and no write fault occurs if the write current source stays on during a read operation. Detection of the fault prevents dc erasure of data during reads as the write with no ac fault previously described prevents it during writes.

1-167. Multihead. The multihead fault occurs if a failure in the head select logic causes more than one head to be selected at one time.

1-168. Fault Lines. Each of the above faults is latched when it occurs, and the heads are automatically deselected by signal FLT-H. Thus, no damage will occur to data on the disc surface after the fault has been detected. The latched fault lines Write With No AC (WNAC-H), Write With No DC (WNDC-H), DC And No Write (DCNW-H), and Multihead Fault (MHF-H) are sent to the microprocessor so that it can determine the correct disc drive response to the detected problem.

Signals Off Track (OFTRK-H) and Track Follower Fault (TFLT-H) from track follower PCA-A9 and signal Emergency Retract (ER-H) from emergency retract PCA-A20 are also used to deselect the heads. This prevents writing on the disc when the heads are not on track or when an emergency retract has been initiated. These faults are not latched on PCA-A10 since they are latched at the source. Note that the occurrence of one of these faults during a write will deselect the heads and this will cause read/write faults (write with no ac and write with no dc) to occur. These latter faults will be latched and reported as read/write faults although read/write PCA-A10 is functioning correctly. (In responding correctly to an external problem, read/write PCA-A10 refuses to write; and then reports that a write is not occurring when a write command is being issued.)

1-169. READ/WRITE SELF TEST. The read/write self test may be partitioned into the following four segments: read path verification, write path verification, fault detection verification, and auto head alignment self test. Descriptions of the four segments are provided in the following paragraphs.

1-170. Read Path Verification. A 4-MHz Test Signal (4 MHz-H) generated in microprocessor PCA-A4 is attenuated and filtered by the self-test signal generator on PCA-A10 to provide 4-MHz Gaussian pulses for injection into the read chain. This injection occurs through a self-test transformer which is selected as if it was the fourteenth read/write head. This simulated data signal is processed in the normal read mode, and results in 67-nanosecond pulses at an 8-MHz rate at the read path output. This output is low-pass filtered on read/write PCA-A10 and is directed as signal Output Test (OUTTST) to microprocessor PCA-A4 through the analog multiplexer on PCA-A10. This filtered output is compared to the tolerance range of the 67-nanosecond pulse at the 8-MHz rate. If the measured value is within this range, the path is considered to be functional.

The automatic gain control in the read chain is also tested. This is done by measuring the average value of the full-wave rectified voltage (FWAVE) with the microprocessor to ensure that it is within specification.

1-171. Write Path Verification. Before the heads are loaded over the discs, data is written to each of the heads. If a write with no ac fault does not occur, it can be assumed that all the heads are functioning correctly for write operations.

The write current reduction circuitry is checked by measuring a voltage change within the write current source as the write current is decreased. Signal Current Source (CS) is measured by microprocessor PCA-A4 and if the voltage change is not within specification, a failure must have occurred.

1-172. Fault Detection Verification. All four of the read/write faults previously described can be caused artificially under microprocessor control. The faults can then be cleared by the microprocessor. If the state of one or more of the faults cannot be made to change by the microprocessor, that particular detect circuitry must have failed.

The automatic deselection of heads is disabled during the fault detection verification so that each fault can be simulated long enough to detect its presence with the microprocessor. Signal Self Test (ST-H) turns off the feedback circuit which otherwise would deselect the heads upon fault detection. Since this test mode could allow data to be destroyed (if self test was enabled over a data surface), the Carriage Back Signal (CRB-L) locks out Self Test (ST-H), Master Reset (MRST-L) and Fault Clear (FCLR-H) signals unless the carriage is fully back and the heads are unloaded.

1-173. Auto Head Alignment Self Test. Self test of the automatic head alignment circuitry is accomplished by generating a test dibit waveform and exercising the automatic head module with it. The dibit waveform is developed by counting down the 4-MHz signals from PCA-A4 by 5 or 10. When the 4 MHz is divided by 5, a positive-negative pair is generated at an 800-kHz rate. In the divide-by-10 mode, the rate is 400 kHz. The 800-kHz and 400-kHz signals simulate the dibit rates for on-track and off-track operation, respectively. During self test, these simulated dibits are fed to the phase locked loop, data clock pulse encoder, and head alignment offset detector in a sequence that tests the operation of the automatic head alignment circuits.

1-174. POWER SUPPLIES. The +5 Vdc, +12 Vdc, and -12Vdc supplies are filtered where they enter PCA-A10 and additional on-board filtering is provided for the +12 Vdc and -12 Vdc to the read preamplifier section. Three Zener regulators on PCA-A10 provide +6.8 Vdc and -6.8 Vdc for the first two video amplifiers, the AGC buffer video amplifier, and the remainder of the signal path including a fourth video amplifier. Two additional Zener regulators provide -5.2 Vdc for the write toggle flip-flop, the dual sample-and-hold comparator, and the 67-nanosecond output one-shot.

1-175. ANALOG MULTIPLEXER. The analog multiplexer is used to select analog signals from PCA-A10 for connection to the analog-to-digital converter on PCA-A10. The output line from the multiplexer to the ADC is labelled Read/Write Test (RWTST). Five analog test signals are selected by the multiplexer. The signal selected is defined by three Multiplex Select bits (MA0-H through MA2-H) from the microprocessor interface on formatter/separator PCA-A8. The signals input to the multiplexer are: Output Test (OUTTST), Current Source (CS), Head Alignment Position Voltage (HAGV), Sampled Head Alignment Voltage (SHAV), Full Wave (FWAVE).

1-176. FORMATTER/SEPARATOR PCA-A8

The basic function of formatter/separator PCA-A8 is to encode input data to the read/write channel and decode data from the read/write channel for reliable channel read/write operations. The circuitry on PCA-A8 includes microprocessor interface logic, a time-sequencer and control logic, a decoder, an encoder, a 30-MHz clock generator, and a phase-locked loop (PLL).

1-177. MICROPROCESSOR INTERFACE. The microprocessor interface is an 8-bit wide parallel input/output interface selectable by the four least significant bits of the microprocessor address bus. The microprocessor interface is used to control the operations of formatter/separator PCA-A8 and read/write PCA-A10, as well as supply the microprocessor with fault flags to indicate serious read/write system malfunctions. External inputs to the microprocessor interface include Address Bus, bits 0 through 3 (A0-H through A3-H), Read (RD-L), Write (WR-L), Formatter/Separator Select (FSSEL-L), and Master Reset (MRST-L). Refer to table 1-5 for a description of the microprocessor interface output (control) and input (flag) signals, as shown in figure 1-19.

1-178. TIMER/SEQUENCER. The function of the timer-sequencer circuitry is to provide sequential control signals for all PCA-A8 on-board operations.

1-179. CONTROL LOGIC. The control logic provides for the proper interface between the microprocessor interface and the timer/sequencer for setting up and sequencing a formatter/separator cycle.

1-180. ENCODER. The coding system used in the encoder is called variable length frequency modulation (VLFM). This code is structured using data blocks of two- or four-bit length. There are four possible combinations in the two-bit block, but VLFM uses only three of them (00, 01, 10). If, in a string of data a "11" is encountered, a four-bit block will be encoded (instead of a two-bit block). Only four of the possible 16-bit combinations are encoded (1100, 1101, 1110, and 1111). These three two-bit patterns and four four-bit patterns cover all possible data sequences. All two-bit blocks are mapped into three bits, and all four-bit blocks are mapped into six bits. At first glance, this would appear to be more of a disadvantage than an advantage, but design of the data map ensures that the worst case data pattern generates transitions on the disc surface that are further apart than of other previously employed codes. This means that the data can be packed tighter on the disc.

On a sector write cycle, the Start Of Sector (SOS-L) signal from track follower PCA-A9 starts the encoder writing a 50 percent duty cycle sync field. No input data is required and the sync field has a duration of 16 microseconds from the leading edge of signal SOS-L. Data is fed to Read/Write PCA-A10 via the Write

Data (WDD-H) line. Signal WENC-L switches from high to low when the leading edge of SOS-L is encountered by the encoder. Signal WENC-L enables the write current circuitry on PCA-A10 when active (low).

With the write current enabled, the sync field is written onto the disc. At the end of the 16-microsecond period, the pattern changes to the all-zero pattern. About one byte of 0's are written followed by a 1. Up to and including the synchronization bit (1), all data has been internally generated by the formatter/separator.

When the sync bit is internally generated by the encoder, it is latched and fed out to the ECC module on DMA PCA-A6 via the Start Of Data (SOD-L) line. A clock is being fed to the write path by the same clock line (RWC-L) as for read. However in this case, clock generation is performed by the encoder.

When signal SOD-L goes low, data (FIN-H) is presented to the input of the encoder (FIN-H) on the next clock edge. The first three bits of data are 0's followed by sector data. When the ECC module is finished its output of data, signal End Of Sector (EOS-L) is set low. This operation generates a delayed reset, waiting an appropriate time for the data to propagate through the formatter/separator to the disc, before the write operation is terminated.

Signal EOS-L resets the encoder. The next operation will be a read unless the microprocessor has set up the control logic prior to EOS-L for a write. In this way, the write operation is shut off by default in order to avoid destruction of recorded data.

1-181. DECODER. The decoder generates a data clock and serial data from the code clock and encoded bit sequence. The decoder circuitry includes a 30-MHz clock generator, a phase-locked loop (PLL), and decoder logic.

1-182. 30-MHz Clock. The 30-MHz clock signal is derived from a 30-MHz crystal-controlled reference oscillator on PCA-A8.

1-183. Phase Locked Loop. The function of the PLL is to generate a code clock from the serialized bit sequence recovered from the disc.

1-184. Decoder. On a sector read, the Start Of Sector (SOS-L) signal from track follower PCA-A9 is a 300-nanosecond pulse used to time the start of a sector read. The leading edge of SOS-L generates a delay internally in formatter/separator PCA-A8. The delay is 8 microseconds after which the read operation begins. After this delay, the phase-locked loop on formatter/separator PCA-A8 is switched via the Read/Write Clock (RWC-L) signal to accept the Read Data (RDD-H) pulses from read/write PCA-A10. At this time, signal RDD-H should consist of equally spaced 66-nanosecond pulses with a period of 133 nanoseconds. This periodic sync field allows the PLL to frequency lock to the transitions. At the same time, the Read/Write Clock (RWC-L) signal from the PLL is output to the rest of the read/write system. A certain time later, the incoming pulses on the RDD-H line are spaced further apart (200 nanoseconds). This is the secondary decode sync field. The decoder recognizes this secondary pattern and triggers the decode cycle to begin.

This secondary sync pattern is decoded as a string of zeros. The first pattern that occurs that results in a "1" being output from the decoder is latched and fed to the read/write system as signal Start Of Data (SOD-L). At the same time, the first "1" followed by three 0's is the data synchronization signature (sync word). The bits that follow represent valid data. Data is output to the ECC module on PCA-A6 via the Formatter/Separator Output (FOUT-H) line. The ECC module generates an overflow handshake when it has enough data. When the End Of Sector (EOS-L) line from the ECC module goes low, it stops the formatter/separator and initializes it for the next sector to be read.

Read mode is a default mode for the formatter/separator. As long as handshake lines Start Of Sector (SOS-L), and End Of Sector (EOS-L) are operational, the decoder will continue to automatically synchronize and output disc data via the FOUT-H line.

1-185. DISC MEMORY ACCESS PCA-A6

The purpose of disc memory access (DMA) PCA-A6 is to provide serial/parallel data conversion, supply all HP-IB interface to the disc drive, buffer data between the disc drive and the host computer, implement a cyclic redundancy check (CRC) for data integration on serial data transfers, and provide an error correction code (ECC) module that improves the integrity and recoverability of data written on the disc.

As shown in figure 1-19, DMA PCA-A6 has three separate external interfaces. The disc drive interface module consists of a serial data path with associated control lines. This interface is used to access the disc drive. The HP-IB interface module is used to interface the disc drive to the host computer through the Hewlett-Packard Interface Bus (HP-IB). The DMA buffer module gives the Z-80-based microprocessor system the ability to control data transfers through the DMA. This interface allows the microprocessor access to the HP-IB for command interpretation/execution.

1-186. DMA BUFFER MODULE. The DMA buffer module includes DMA control/status registers, a disc address counter, an I/O address counter, an I/O byte counter, data RAM, and header RAM.

Inputs to the DMA buffer module include 12 Address lines (A0-H through A11-H); eight Data lines (D0-H through D7-H); two control lines: Read (RD-L) and Write (WR-L); four Select lines: Buffer Select (BF1SL-L), I/O Select (IO1SL-L), ECC Select (EC1SL-L), and DMA Select (DM1SL-L); and a Power On Reset (MRST-L) line. The four select lines allow the microprocessor to access the data RAM, the processor to HP-IB interface (PHI) registers, the DMA control/status registers, the error correction logic, and the header RAM.

1-187. DMA Control/Status Registers. The DMA Select (DM1SL-L) line, along with five address bits, are decoded by the DMA to provide 32 memory mapped ports. The first 16 of the 32 memory mapped ports allow access to the 16 bytes of the header RAM and the remaining 16 ports are decoded to provide eight control registers (write registers) and five status registers (read registers).

1-188. Disc Address Counter. The disc address counter is a 13-bit counter used to address the header RAM and the data RAM during data transfers between the disc drive and the DMA. The lower nine bits of the counter are used to address the two RAM's within each sector as detailed in the header RAM description.

1-189. I/O Address Counter. The I/O address counter is a 12-bit counter used to address the data RAM during data transfer between the data RAM and the PHI.

1-190. I/O Byte Counter. The I/O byte counter is a 12-bit down counter which provides a means of stopping the transfer of data over the HP-IB at a predetermined byte count. Before the data transfer is started, the host computer tells the microprocessor how many bytes of data to expect in the transfer. This total byte count will be divided by 4,096 (maximum count with a 12-bit counter) and the remainder loaded into the I/O byte counter. The integer portion of the quotient from the above division is actually the number of times the I/O byte counter will wrap around the remainder number to which it is loaded. The microprocessor keeps track of the number of times this wrap-around occurs and enables the I/O stop circuitry 16 sectors before the end of transfer will occur.

1-191. Data Ram. The data RAM consists of 4 kbytes of static RAM. The RAM receives the address field from three sources: the microprocessor, the disc address counter, or the I/O address counter. Since each disc sector consists of 256 bytes of data, the data RAM is capable of buffering 16 sectors of data enroute to or from the disc. The RAM is effectively converted into a 2-port RAM by multiplexing the disc and I/O address counters during data transfers. All the data enroute to or from the disc drive must pass through the data RAM.

1-192. Header Ram. The header RAM consists of two bipolar 16 by 4 RAM integrated circuits arranged as 16 bytes of very fast read/write memory. The header RAM is used to store the preamble and postamble information during each sector of disc access. The disc drive sector format is shown in figure 1-4. The disc address counter accesses the lower six bytes of header RAM at the beginning of each sector then increments into the data RAM address field (256 bytes) and finally wraps around into the first seven bytes of header RAM near the end of the sector. During a disc write, the six bytes of preamble are taken from the header RAM. If a full sector format is selected, the two cyclic redundancy check (CRC) bytes are also taken from the header RAM. During a disc read operation, the preamble, CRC, and error correction code (ECC) bytes are read into the header RAM.

1-193. HP-IB INTERFACE MODULE. The HP-IB interface circuitry includes a Processor to HP-IB interface (PHI) circuit and a PHI latch. The HP-IB interface inputs include eight data lines (DIO1-L through DIO8-L) and eight control lines. The eight control lines are: Attention (ATN-L), Data Valid (DAV-L), End or Identify (EOI-L), Interface Clear (IFC-L), Not Ready For Data (NRFD-L), Remove Enable (REN-L), Not Data Accepted (NDAC-L), and Service Request (SRQ-L).

1-194. Processor to HP-IB Interface. The processor to HP-IB interface (PHI) is an integrated circuit designed to transfer bytes of data across the HP-IB. The microprocessor will normally set the PHI up to transfer data either into (write) the DMA data RAM or out of (read) the data RAM. Once the proper direction and control bits are set up, the microprocessor enables the start of a PHI/data RAM transfer.

The PHI address and control lines are multiplexed between the microprocessor and the DMA controller. The PHI can be accessed by the DMA machine or the microprocessor through the PHI data bus.

1-195. PHI Latch. The PHI latch is a bidirectional buffer register. The register is used to hold one byte of data enroute to the PHI (disc read) or just extracted from the PHI (disc write). This buffering is necessary due to the PHI's relatively slow access time during data transfers.

1-196. DISC DRIVE INTERFACE MODULE. The disc drive interface module is basically the serial data path between the DMA and formatter/separator

PCA-A8 in the read/write system. Circuitry in the disc drive interface includes a serializier/deserializier (SERDES), SERDES control logic, sector control logic, and a cyclic redundancy check circuit. The disc drive interface lines are End Of Sector (EOS-L), Start Of Data (SOD-L), Read/Write Clock (RWC-L), Read Data (DIN-H), and Write Data (DOUT-H).

The normal sequence of operation of the interface during a disc read or write is as follows: signal EOS-L is activated, informing the DMA to get ready to prepare a sector. Next, SOD-L is activated, informing the DMA that the serial data stream is beginning on the next RWC-L edge. The first active data bit may be delayed several clock edges from SOD-L depending on the direction of the transfer.

Serial data is now clocked into or out of the DMA until the end of the sector is reached. When SOS-L for the next sector is received, it either resets the DMA or continues the transfer depending on microprocessor activity during the previous sector.

1-197. Serializer/Deserialzer. The serializer/deserializer (SERDES) changes serial data from the disc to parallel bytes for buffering and subsequent transfer over the HP-IB. The SERDES also changes parallel data enroute to the disc into a serial data stream.

The serializer consists of an 8-bit holding register and a shift register. During a write, a byte is written (upon request) into the 8-bit holding register sometime prior to the time it will be shifted out by the shift register. The byte is loaded into the shift register at the proper time to provide a continuous data stream.

The deserializer consists of an 8-bit shift register (the same components as the serializing shift register) and an 8-bit holding register. During a read, the serial data is shifted into the deserializing shift register and at the end of the byte, it is loaded into the holding register. Sometime during each byte, the DMA byte controller extracts the byte from the holding register and transfers it to the data RAM.

1-198. SERDES Control Logic. The SERDES control logic controls the start of the disc read and write operations. It also controls the shifting/loading of the registers in the SERDES.

1-199. Sector Control Logic. The sector control logic prevents incoming data from overflowing the data in the data RAM. The data is monitored by the microprocessor in order to control overruns on disc reads and writes. For a disc read, the sector counter is incremented after each sector is read from the disc and decremented after each sector (or partial sector if the last sector does not contain 256 bytes) is transferred over the HP-IB. For a disc write, the sector counter is incremented after the sector is received from the HP-IB and decremented after each sector is written to the disc. During a disc read, HP-IB data transfer is held off by the sector counter when the data RAM becomes empty and transfer does not resume until at least one full sector is read in from the disc. Also, during a disc write, the HP-IB data transfer is held off by the sector counter when the data RAM becomes full and transfer does not resume until at least one sector (256 bytes) of ROM is available.

1-200. Cyclic Redundancy Check. The cyclic redundancy check (CRC) circuit implements the CRC-16 polynomial. During a write, the serial data is fed into the CRC generator until the last bit of the data field has been clocked in. At this time, the output data multiplexer is switched to clock the 16-bit value in the CRC shift register out as two CRC bytes. During a read, the serial data is fed into the CRC checker until the last bit of CRC is clocked in. At this point, the input to the CRC is disabled. If no data error has been detected, all 16 flip-flops in the CRC shift register will contain zeros. If any detectable error has occurred, at least one of the 16 flip-flops will contain a one.

1-201. DMA BYTE CONTROL. The DMA byte control circuit is in charge of all data transfers between the PHI, data RAM and SERDES. The controller consists of two ROM-based state machines, a sector counter, and the necessary logic to accomplish the above function. One ROM-based state machine controls data transfer between the data RAM and the PHI latch. The other ROM-based state machine controls data transfer between the PHI latch and the PHI. Both machines run on an internally generated 12-MHz clock and handshake with each other to synchronize data transfer through the PHI.

1-202. ERROR CORRECTION CODE MODULE. The purpose of the error correction code (ECC) module is to improve the integrity and recoverability of data written on the disc media. To perform this function during a write, the ECC module adds redundant information to the data written on the disc. On a read, the ECC module examines the data and the redundant information and from this can determine if a data error has occurred and correct it if the length of the error is 12 bits or less. Most data errors greater than 12 bits are detected but not corrected.

1-203. Disc Writes. To operate as an error detector and corrector, the ECC module requires additional information along with the data. This redundant information is generated during a write. The process of generating and appending the redundant information is a form of encoding the data. The ECC check polynomial developed by the ECC encoder is 35 bits in length. The data field has 2,112 bits before the ECC information,

thus the addition of the 35 ECC bits makes the sector length written to the disc 2,147 bits.

The ECC module has two write modes. The first is write with encoding. In this mode, the data from the DMA is sent to formatter/separator PCA-A8 until the end of the data field. At this time, the ECC sends the redundant information (ECC postamble) to the formatter/separator. The second mode of operation is write full mode in which the data from the DMA is passed directly to formatter/separator PCA-A8. In this mode, the ECC field is supplied by the DMA. This method of writing is for diagnostic purposes only and is not used for normal operation.

The data to be written to the disc comes into the ECC on the DMA Data Out (DOUT-H) line. The input data is connected to a gate circuit that selects between the DMA data and the encoded ECC postamble. The output of the gating circuit is labelled Formatter/Separator Input (FIN-H). Signal FIN-H goes to formatter/separator PCA-A8 and is the data that is written on the disc. In the normal write mode, data from the DMA is passed to formatter/separator PCA-A8 until the end of the CRC field. At the end of CRC, signified by End Of Sector (EOS-L) going low, the ECC postamble is sent to the formatter/separator. In the write full sector mode, data from the DMA is always passed to the formatter/separator.

The ECC encoder is a linear feedback shift register that generates 35 redundant bits from the data. The ECC field that is generated is appended to the data field immediately following the cyclic redundancy check (CRC). The location of the ECC field in the sector format is shown in figure 1-4.

1-204. Disc Reads. To detect and/or correct the data read from the disc, the ECC module decodes the data and the appended redundant information. This process takes two steps. After the sector has been read and decoded, it is output one bit at a time. Correction is attempted on each bit as it leaves the ECC. The data is delayed one full sector on a read while it passes through the buffer.

There are several options for reading with ECC. The first is read with no correction or detection. This is analogous to the write full sector mode and is used only for diagnostic purposes. A second mode of operation is to read with detection of errors but no correction. The third mode is to read with detection and correction. In this mode, all data errors of 12 bits in length or less will be corrected. A sector with any two or more bits in error separated by more than 12 bits is uncorrectable and must be recovered with a new read, if possible.

There are two ECC read error flags. The first is Uncorrectable Error (UNER-L). This flag is sent as the last bit of the sector transferred to the DMA. Once set, UNER-L requires the microprocessor to clear it or a power-on condition to reset it. A second flag is sent when a correction has occurred. This flag is valid during the sector following the sector of interest.

The ECC is a real-time correction scheme. This requires that as one sector is being decoded, the preceding sector is being corrected, if necessary, as it is being output to the DMA. This requires the use of the two decoders. Each decoder operates independently. While one is decoding the incoming data, the second is correcting the output data. The function of each decoder switches between these two functions at the start of each sector. This allows a given sector to be decoded and corrected by the same decoder.

The decoder is similar to the ECC encoder in that it is a linear feedback shift register. This permits the same hardware to be used for the encoder and decoder with only minor differences. In the decode mode, data from the disc is input to the decoder. To manipulate the data length specified by the polynomial to the actual sector length, the data is preshifted.

At the completion of the ECC field, the linear feedback shift register should be all zeros if no error has occurred. If the register is nonzero, a correctable or uncorrectable error has occurred. The decoder is then shifted each clock cycle. If the decoder traps 12 bits or less, error correction starts. During the time the decoder has been trying to trap an error, the buffer has been outputting one bit of the sector on each clock. When the error burst has been trapped by the decoder, the bits in error are positioned at the output of the buffer. The data is corrected by inverting those data bits that align with the error correction pattern found by the decoder. If any error is corrected, the ECC records that as a correctable error. If no bits are corrected during a sector, and the linear feedback shift register is not all zero's, then the uncorrectable error flag is set. There is a possibility that an uncorrectable error will be incorrectly flagged as a correctable error and correction attempted. The CRC which resides in DMA PCA-A6 provides protection against this occurrence.

1-205. Buffer. The buffer is a 2,147-bit shift register that holds one full sector. As data from one sector shifts in, the data from the previous sector is shifted out. A sector is shifted into the buffer as it is read off the disc. During the next sector it is shifted out to the disc drive interface module.

1-206. Error Detection Logic. There are three errors, that can be detected by the ECC module. These are: Uncorrectable Error (UNER-L), correctable data errors and ECC write errors. Signal UNER-L is set on a disc read when there is an error of greater than 12 bits in length in a given sector. A correctable data error is set when an error of less than 12 bits in length is found in a sector. Signal UNER-L and correctable

data errors are generated during a disc read. ECC write errors are generated during a disc write. An ECC write error is set if there is a hardware failure in the encoders. Signal UNER-L and ECC write errors are classified as hard errors. They are only reset by a Microprocessor Clear (PCLR-L) or Power On Reset (MRST-L). A correctable data error is held for one sector and then reset. An ECC write error is classified as a drive fault as it implies a failing ECC module.

1-207. Control And Timing Logic. The control and timing logic controls the switching of the data streams. The circuitry generates the timing for the end of the data field and the timing for the end of the sector (EOS-L). The synchronization of the ECC data to the data on the formatter/separator and the DMA is also handled by the control and timing logic.

1-208. ECC Data/Control Register. The ECC data/control register permits the microprocessor to control the functions of the ECC module and read the status of the ECC module during self-test.

1-209. ECC Self Test. Self testing the ECC module consists of controlling all the inputs and monitoring the outputs. For the ECC module this requires the control of signals to formatter/separator PCA-A8 and DMA PCA-A6.

A register under microprocessor control drives these interface lines that are normally driven from other PCA's. Through other registers, the microprocessor can read the state of all inputs from the formatter/separator-ECC-DMA interface. In addition, the microprocessor can read the state of all signals generated by the ECC. The signals are read before they are buffered onto the formatter/separator-ECC-DMA bus.

1-210. DISC WRITES

Disc writes, carried out under microprocessor control, can be of two types. One type is when data from the host CPU is sent to the disc drive and then written on the disc. The other type of write is internal to the disc drive. This latter type occurs during functional verify or format. In addition, writes can be either normal with CRC and ECC appended or write full sector with the entire sector being generated by the host CPU.

There are three PCA's directly involved in disc writes. These are read/write PCA-A10, formatter/separator PCA-A8, and DMA PCA-A6. The DMA must contain one sector prior to starting to write a sector on the disc. This prevents an overrun situation where there is no data at some point during the write of a sector. The DMA also contains CRC and ECC generators.

Before the write can begin, the microprocessor checks that the spindle is at speed and the heads are loaded. Following this, the output data stream from DMA PCA-A6 is sent to formatter/separator PCA-A8 where the data is encoded to VLFM. The output from formatter/separator PCA-A8 is then sent to read/write PCA-A10 where the data is changed into current pulses to the selected data head.

The first step in a write operation is to position the heads over the correct track. The correct head is then selected and a sector is verified to ensure that the seek was made to the correct track. The sector that is to be written into is called the target sector. The microprocessor sets up DMA PCA-A6, formatter/separator PCA-A8, and read/write PCA-A10 in the target sector minus one. DMA PCA-A6 is now set to send one sector, starting at the next Start Of Data (SOD-L), with the ECC module set to the write mode, and formatter/separator PCA-A8 also in the write mode. This sets the clock to an internally generated 30-MHz square wave. Finally read/write PCA-A10 is set to the write mode. The write current source is not turned on until after Start Of Sector (SOS-L).

DMA PCA-A6 must be turned on after each sector during the previous sector. The microprocessor checks to ensure that a complete sector is in the DMA before enabling the next sector transfer. Before each sector, the microprocessor writes the header into the header RAM on the DMA. For sectors after the first sector, only the sector number is rewritten. The ECC module on DMA PCA-A6 is set at the beginning of the transfer and remains in the write mode until reset. Formatter/separator PCA-A8 must be set to the write mode by the microprocessor every sector. This prevents a microprocessor failure from causing a write over a good sector. Read/write PCA-A10 remains in the write mode and does not require to be set up at every sector.

To terminate a write, the microprocessor does not enable DMA PCA-A6 and formatter/separator PCA-A8 for the first non-write sector.

The microprocessor will terminate a write upon the receipt of several error conditions. These are:

- An End or Identify (EOI) was received before the correct number of bytes were received by DMA PCA-A6 from the host CPU.
- The number of bytes specified by the byte count has been received, without an EOI being received.
- A channel error has been detected.
- The software thinks that the write is finished, but the hardware thinks that more is required.
- The ECC could not recover from an ECC write error.
- The microprocessor fault detection circuit has detected a fault. This indicates either:

(1) Off-track (OFTRK-H)

(2) Spindle Speed Down (SPDDN-H)

(3) Track Follower Fault (TFFLT-H)

(4) Door Open (DO-H)

(5) Emergency Retract (EMRKT-H)

(6) Power Down (PWDN-H)

(7) R/W Fault (RWFLT-H)

- The firmware indicates that there are additional bytes to write while the DMA indicates that the total transfer has occurred.
- The target sector was not found in one full revolution.
- The ECC has write error.
- A failure of the CTC on microprocessor PCA-A4 to increment from sector to sector.
- The DMA did not contain a full sector prior to when the next sector was to be written.

If there is no error, then a good status is returned. There is no checking at the end of a write to verify any of the written data.

1-211. DISC READS

There are three types of disc reads: an internal read, a normal read, and a full sector read. the internal read is used for testing and verify. The normal read is used to send data to the host CPU. A read full sector does not attempt correction; all data, including the ECC field, is sent to the host. All disc reads require that the heads be positioned over the correct track.

There are several problems that can occur in a read as the result of data errors. The first is a correctable error. This is detected by the ECC module on DMA PCA-A6 and corrected in real time. The only action for the microprocessor is for it to increment the number of correctable sectors detected. A second problem is an uncorrectable sector. This occurs when the error is greater than one 12-bit burst. A signal from the ECC module prevents the sector in question from being sent to the host CPU. A third error is a CRC error. This error occurs when the data out of the ECC module is incorrect. The CRC error can occur if:

- The sector is uncorrectable.
- The ECC incorrectly corrected the error.
- There was a loss of lock while the data was being sent to the DMA.

A fourth type of error is a Formatter/Separator Uncorrectable Error (FUNER-L). The error occurs when the formatter/separator fails to detect the sync bit within its normal window. When the data is not either correct or correctable, then a read retry algorithm is entered.

The read continues until a noncorrectable error occurs, there is a drive error, or the transfer is complete. At the end of the transfer, the DMA and the ECC are cleared. At the same time, formatter/separator PCA-A8 and read/write PCA-A10 are set to lock on the write data clock. This action prevents loss of lock from occurring during nondata sectors.

The drive errors that can occur during a read operation include:

- Offtrack (OFTRK-H)
- Formatter/Separator Error
- Buffer full and I/O not running
- Latency induced
- CTC not counting sectors
- Target sector not found
- Address compare error
- DMA reported error not detected by ECC or formatter/separator
- Uncorrectable error
- FUNER-L error
- Drive fault in non read/write hardware

A read retry routine is initiated by the firmware whenever a retryable data eror occurs during a read operation. The host computer can specify via a CS/80 command, the maximum amount of time allowed for read retries. The host can specify a maximum retry time between 0 and 655.35 seconds in 10-millisecond increments. A retry time of 0 milliseconds will cause no retries to be executed. It should be noted that even when no retries are attempted, one rotational latency will occur as a result of an uncorrectable data error. Also, an additional latency will occur after the data has been recovered before the next sector can be read. Thus, two rotational latencies will occur if the data is recovered on the first try.

The following describes, in order, the operations performed to recover the data.

a. If a read-and-transmit command is being performed, the data that is in the buffer will be sent to the host before any retries are attempted. During a buffered read, there will always be one page in the DMA buffer that is empty and can be used for retry reads. Also, the page that was being used when the data error occurred can be employed. Thus, two pages are available to work with.

b. A logical timer is initialized so that it can be determined how much time elapsed since retries started. Each of the following items will be tried only if enough time is left to complete it.

c. If there is not enough time for step d, return with the data that was available on the first read (since there was no time for retries).

d. Verify and re-read on the next revolution. The data will be read into a different place in the DMA buffer so as not to destroy the data available after the first try. If the data is read with no errors on the retry, it will be returned to the host without reporting any error condition.

e. If the data is returned by any of the following routines, it will be returned with the error marginal data, sparing advised. If the read retry time runs out before the data is recovered, the bad data will be returned along with an indication that the data is not good.

f. If there is not enough time for step g, return the latest data available.

g. Try a second re-read on the next revolution. Return good data if it is read.

h. If no time for step i, then return the latest data available.

i. An automatic head alignment is performed on the head trying to be read from. Then a re-seek to the desired track is performed and an attempt to re-read.

j. If no time is available for step k, return the latest data available.

k. Try re-reads at various radial offsets. The data is read into a different part of the DMA buffer so that the data obtained after step i will not be lost. Up to 10 reads will be done with relative offsets of various values on both sides of track center.

l. If no time for step m, return data available in step i.

m. Try reads at various skew offsets. The sector will be read with skew offsets to microinches in both directions.

n. If a correct read is not yet available, the data read at step i (after automatic head alignment) will be returned.

1-212. POWER DISTRIBUTION SYSTEM

The power distribution system (see figure 1-20) consists of a power module, voltage regulator circuits, fault detection circuits, and associated switches, fuses, indicators, and wiring. The purpose of the power distribution system is to develop the necessary dc operating voltages from the ac supply source and distribute these dc voltages throughout the disc drive. Figure 5-19 is a wiring diagram of the disc drive, and table 5-11 provides a power distribution list for motherboard PCA-A11. Together, the wiring diagram and the distribution list supply power connection information for the disc drive. Refer to table 1-6 for a description of the mnemonics used in figure 1-20. In the "source" column of table 1-6, the numbers in parentheses following the PCA reference designations identify the functional block diagram locations of the PCA's.

1-213. POWER MODULE

The power module is comprised of a metal casting on which a number of the power distribution system components are attached. The module is mounted on slides at the rear of the disc drive enclosure for easy serviceability. The components mounted on the power module include an input power assembly, a blower power assembly, terminal block TB1, power transformer T1, dc power PCA-A13, and spindle driver PCA-A12. Details of these components are provided in the following paragraphs.

1-214. INPUT POWER ASSEMBLY. The input power assembly includes a captive line cord, ~ LINE circuit breaker S1, receptacle J1, and line filter PCA-A21. AC power goes in two directions from ~ LINE circuit breaker S1. One path is to accessory power outlet receptacle J1 located on the bottom of the module and the other path is to line filter PCA-A21. Receptacle J1 provides a source of ac power for future developments of the disc drive. The line filter suppresses the conducted radio frequency interference generated in the disc drive.

1-215. TERMINAL BLOCK AND POWER TRANSFORMER. Terminal block TB1, following line filter PCA-A21, is wired to the primary side of power transformer T1 and permits strapping the transformer primary windings to match the level of the ac supply voltage. Details of the strapping on terminal block TB1 are shown in figure 5-19. The secondary windings of power transformer T1 are connected to dc power PCA-A13 and spindle driver PCA-A12.

1-216. BLOWER POWER ASSEMBLY

The blower power assembly, located at the lower rear of the power module, includes connector J1 and fuse F1. Power for blower motor B3 is derived from the terminal block TB1 connections supplying power to one of the 120-volt primary windings on power transformer T1. This permits operation of a 120 Vac blower motor with primary power inputs of 200, 208, 220, or 240 Vac.

Table 1-6. Power Supply System Mnemonics

MNEMONIC	DEFINITION	SOURCE	FUNCTION
A0-H, A1-H	Address Bus, bits 0 and 1	PCA-A4 (1)	Microprocessor address bus, bits 0 and 1.
AGND	Analog Ground	-	Analog ground system.
D0-H thru D7-H	Data Bus, bits 0 thru 7	PCA-A4 (1)	Microprocessor bidirectional data bus, bits 0 through 7.
DGND	Digital ground	-	Digital ground system.
-EMR SUPP	Emergency Retract Negative Supply	PCA-A12 (6)	Unregulated -36 Vdc supply to emergency retract PCA-A20.
+EMR SUPP	Emergency Retract Positive Supply	PCA-A12 (6)	Unregulated +36 Vdc supply to emergency retract PCA-A20 in head positioning system.
-LMSUPP	Linear Motor -36V Supply	PCA-A12 (6)	Unregulated -36 Vdc supply to actuator driver PCA-A2 in head positioning system.
+LMSUPP	Linear Motor +36V Supply	PCA-A12 (6)	Unregulated +36 Vdc supply to actuator driver PCA-A2 in head positioning system.
MRST-L	Master Reset	PCA-A1 (6)	A master reset signal that initializes the logic PCA's during power on sequencing.
PGND	Power Ground	PCA-A12 (3)	Power supply ground
PWRDN-H	Power Down	PCA-A1 (6)	Signal sent directly to microprocessor signaling a power supply failure on PCA-A1.
RD-L	Read	PCA-A4 (1)	Microprocesor read command.
REGSL-L	Regulator Select	PCA-A4 (1)	Microprocessor select line to PCA-A1.

1-217. DC POWER PCA-A13. DC power PCA-A13 rectifies and filters ac voltages from the secondary windings of power transformer T1 to provide unregulated dc voltages for regulator PCA-A1.

One winding of the power transformer is connected via fuses F110 and F115 to a full-wave rectifier integrated circuit. The output from the rectifier is filtered by capacitor C170 to become approximately +13 Vdc.

A second winding on the power transformer is connected via fuses F210 and F215 to a full-wave bridge rectifer consisting of four diodes. The positive and negative outputs from the rectifier are filtered by capacitors C230 and C270 to become approximately +20 Vdc and -20 Vdc, respectively.

A bleeder resistor is connected across each of the filter capacitors. The values of these resistors are chosen to discharge the capacitors in 2 minutes. This is less time than it should take to disassemble the disc drive to a point where the terminals on the capacitors are exposed.

1-218. SPINDLE DRIVER PCA-A12. Spindle driver PCA-A12 contains circuitry that rectifies and filters ac voltage from a secondary winding on the power transformer to supply +36 Vdc and -36 Vdc operating power for the spindle rotation system and the head positioning system.

One winding on the power transformer is connected via fuses F510 and F520 to a full-wave bridge rectifier. The positive and negative outputs of the rectifier are filtered by capacitors C1 and C2 to become +36 Vdc and -36 Vdc, respectively. A bleeder resistor connected across each of the filter capacitors discharges the capacitors in 2 minutes.

1-219. REGULATOR PCA-A1

Regulator PCA-A1, located in the disc drive card cage, contains +5 Vdc, +12 Vdc, and -12 Vdc regulated supplies that supply operating voltages to the PCA's located in the card cage and mounted on the control panel. Distribution of the voltages to the PCA's in the card cage is via connectors on motherboard PCA-A11, as detailed in table 5-11. Power to the control panel PCA's is via microprocessor PCA-A4 and cable W5. Regulator PCA-A1 also contains fault detection circuitry that monitors certain conditions of the power distribution system and makes available this information to the microprocessor for self test and fault location purposes.

1-220. +5 VDC REGULATED SUPPLY. The +5 Vdc regulated supply is constructed from discrete components and incorporates overcurrent and overvoltage protection. In operation, the unregulated +13 Vdc is delivered through a unity gain power amplifier to the motherboard "load". A comparison amplifier compares the "load" voltage with a stable reference and drives the power amplifier to achieve an error null. This action maintains the "load" voltage essentially equal to the reference level, independent of load current and +13 Vdc supply variations. Potentiometer R185 allows the output to be set to +5 Vdc, ±50 millivolts.

The regulator circuit is protected against load faults by an overcurrent detect circuit that latches the supply output to zero volts for current surges lasting longer than 100 microseconds. When the overload condition is removed, the +5 Vdc output can be restored by turning the ~ LINE circuit breaker off and then on again after a 2-minute delay. Light-emitting diode DS192 is lit when the supply is in a +5 Vdc current shutdown mode.

The +5 Vdc output line is protected against overvoltage conditions which could cause damage to the logic elements. A sensing amplifier compares the output voltage with an independent 6.2 Vdc reference and triggers a crowbar circuit when an overvoltage occurs. For a longer term, fuse F162 in the +13 Vdc line will also open. A further fail-safe action is taken by enabling the normal current shut-down procedure previously described.

The +5 Vdc supply is protected from thermal overload by a thermal switch that opens to disable the power amplifier when the heat sink temperature rises above 70°C (158°F).

1-221. +12 VDC REGULATED SUPPLY. The +12 Vdc regulated supply employs a heat-sink mounted monolithic voltage regulator that incorporates thermal and overcurrent shutdown. Potentiometer R177 allows the output voltage to be set to +12 Vdc, ±0.36 volt. In the event of an overcurrent, overtemperature, or shorted output condition, light-emitting diode DS182 will light to provide a visual indication of a circuit failure.

1-222. -12 VDC REGULATED SUPPLY. The -12 Vdc regulated supply is similar to the +12 Vdc supply and includes a voltage regulator, adjustment potentiometer R117, and LED DS122. The -12 Vdc output is set to -12 Vdc, ±0.36 volt.

1-223. POWER-ON CIRCUIT. The power-on circuit generates Master Reset signal MRST-L which is used for initialization of the disc drive logic circuits during power-on sequencing.

At power turn on, signal MRST-L is active (low) for approximately 500 milliseconds after the +5 Vdc regulated output has stabilized. At very low line voltage (a brownout condition), MRST-L becomes active whenever the +5 Vdc regulated output drops more than 0.25 volt below the reference voltage level.

1-224. FAULT DETECTION COMPARATOR. The fault detection circuits on PCA-A1 inform the microprocessor interface logic when any of the following failure modes or warning conditions occur:

- Loss of -20 Vdc supply (unregulated -12 Vdc).
- Loss of -12 Vdc regulated supply.
- Loss of +20 Vdc (unregulated -12 Vdc) supply.
- Loss of +12 Vdc regulated supply.
- Loss of +13 Vdc (unregulated +5 Vdc).

No tests are made on the regulated +5 Vdc supply. This is because of microprocessor dependence on this voltage.

Fault detection circuits on spindle driver PCA-A12 monitor the +36 and -36 Vdc supplies to the spindle drive and actuator driver PCA-A2. These detectors are discussed in paragraph 1-67.

The fault detection circuitry on PCA-A1 employs voltage comparators that compare the monitored voltages with a 1.1 Vdc reference derived from the regulated +5 Vdc supply. A loss or abnormal condition in any of the monitored voltages causes the associated comparator to latch a signal into the microprocessor interface circuit and to transmit Power Down flag PWRDN-H directly to the microprocessor.

1-225. MICROPROCESSOR INTERFACE. The microprocessor interface to regulator PCA-A1 provides the following four functions:

- Analog outputs for testing voltage levels with the voltage-to-digital converter on microprocessor PCA-A4.
- A flag capability so that the regulator can inform the microprocessor of fault status.
- Labelled outputs of the regulator fault type on an eight-bit output port to the microprocessor.

The analog levels supplied for testing by the analog-to-digital converter on PCA-A4 are taken from the voltage dividers used in the onboard fault detection comparators. These signals are labelled -12TST and +12TST.

When a fault is detected by one of the comparator circuits, the states of all five comparators are clocked into the fault latch register. The state of these latches can then be examined by the microprocessor by enabling the associated line driver.

1-226. AIR CIRCULATION AND FILTRATION SYSTEM

The air circulation and filtration system consists of a centrifugal blower situated at the bottom front of the disc drive cabinet, a prefilter, an absolute filter, and associated ducting.

Cooling air is drawn by the centrifugal blower into the prefilter through vent openings in the front of the cabinet. (See figure 1-13.) Large airborne contaminant particles are trapped as the air is drawn through the prefilter. Approximately one-half of the developed air flow bypasses the absolute filter and is directed toward the power module and the card cage assembly. This flow of cooling air exits through vent openings at the top rear of the cabinet.

The remaining one-half of the air flow developed by the centrifugal blower passes through the filtration element of the absolute filter where 99 percent of all contaminant particles 0.3 micron or larger are removed. After the air is thoroughly filtered, it is ducted into the media module chamber. When the top door of the disc drive is opened to install a media module, all critical areas of the chamber will be purged of any foreign matter. Also, the high positive pressure developed within the media module chamber after a media module has been installed and the top door closed tends to reject any airborne foreign matter. The air flow exiting from the media module chamber is directed over the actuator assembly before being expelled through the vent openings at the top rear of the cabinet.

Figure 1-14 shows the critical elements involved in the read/write process, that is, the read/write gap, the flying height of the head, and the thickness of the oxide coating on the media module disc substrate. The flying height of the head is an average value due to the surface irregularities of both the head and the disc. Figure 1-14 also shows various types of contaminants and their size in relation to the flying height of the head. If a particle is hard enough and of sufficient size, it may scratch either the oxide coating of the disc or the surface of the head. Even if the particle is not hard enough to scratch, it may be large enough to increase the head-to-disc spacing, thereby causing data errors.

To prevent potential damage to the disc drive due to head-to-disc contact and possible data losses, it is extremely important that the cleanliness of the air flow within the disc drive be maintained. To ensure that clean air will be present, the disc drive must be operated in the specified environment and the efficiency of the prefilter and the absolute filter maintained. A pressure-sensitive sensor located in the air flow path monitors air pressure at the output of the absolute filter. The status of the sensor is checked at power turn on by the disc drive self-test routine and on a continuing basis by the host computer. Any indication of an abnormal condition in the air flow must be immediately corrected by service-trained personnel.

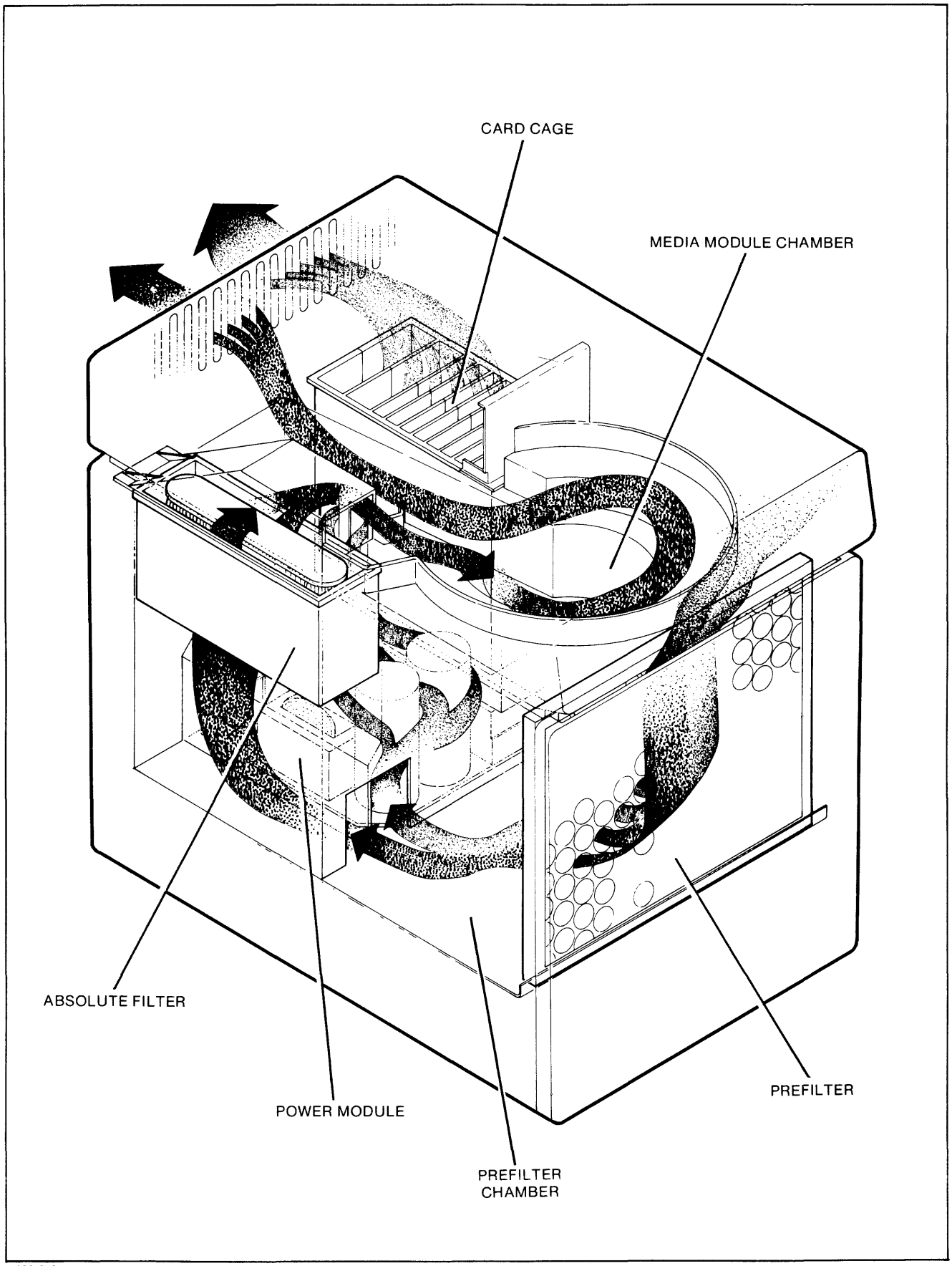


Figure 1-13. Air Circulation and Filtration System

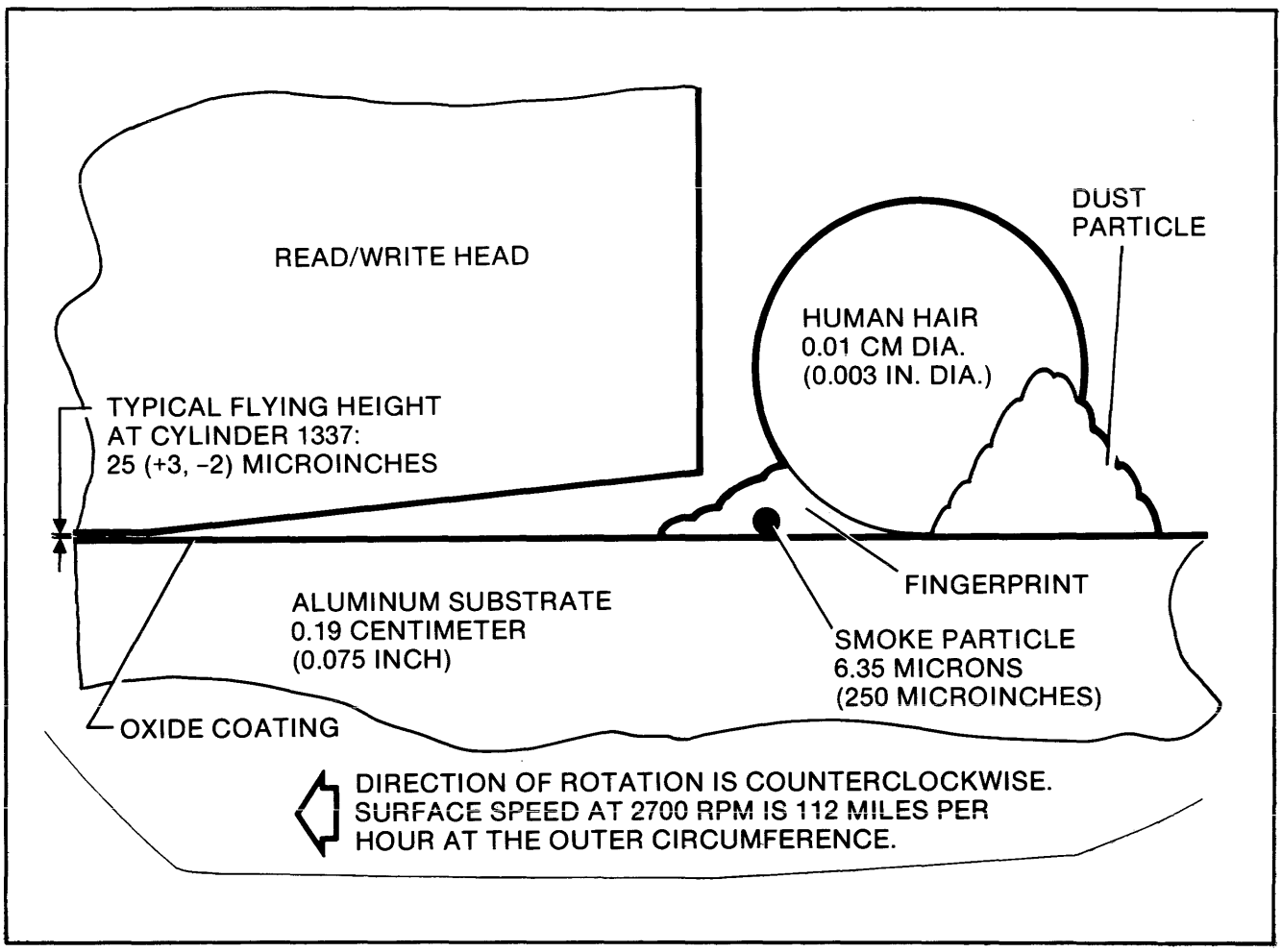
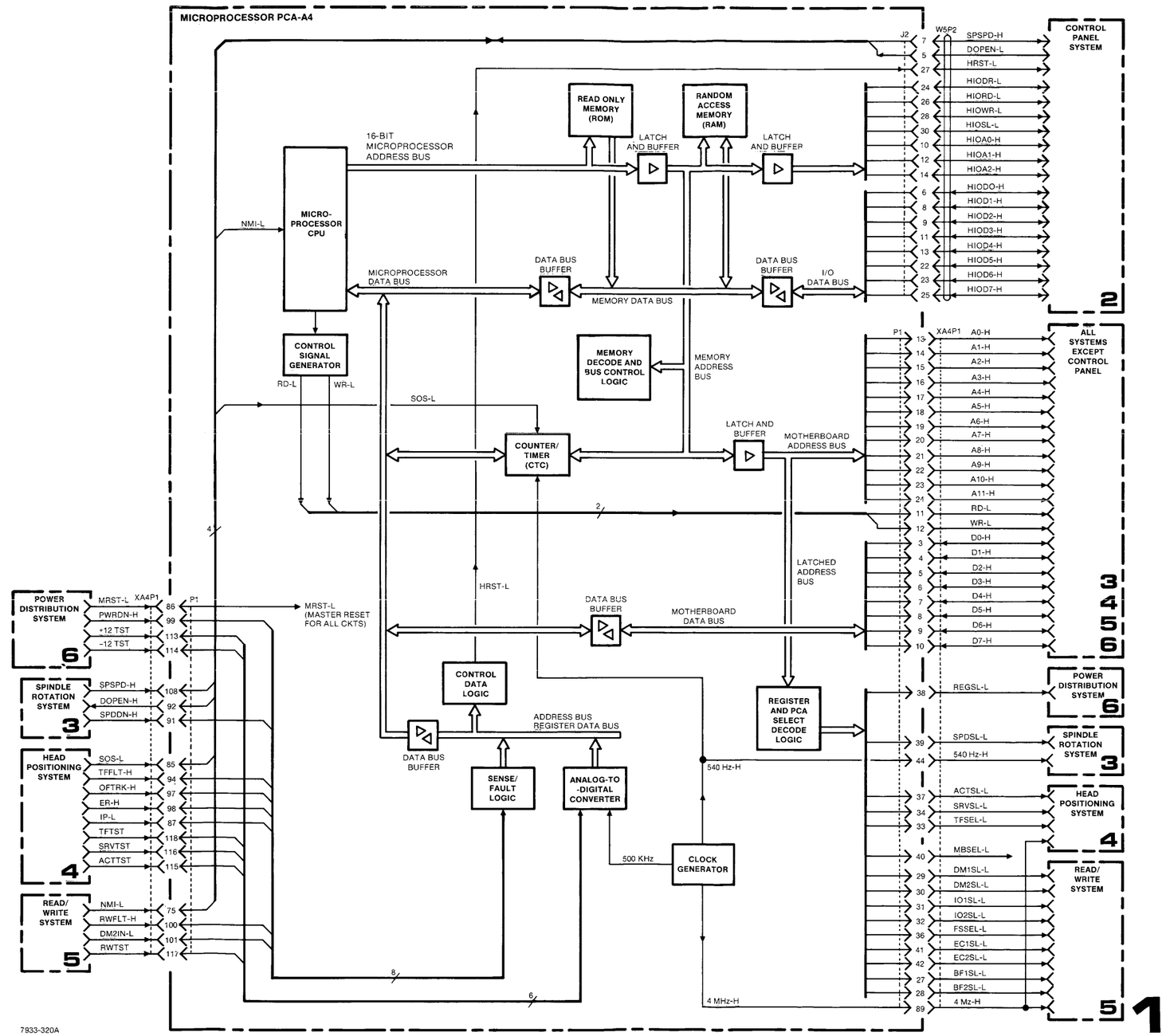


Figure 1-14. Types of Contaminants and Critical Elements


MICROPROCESSOR PCA-A4
J2
W5P2
CONTROL PANEL SYSTEM
SPSPD-H
DOPEN-L
HRST-L
HIODR-L
HIORD-L
HIOWR-L
HIOSL-L
HIOA0-H
HIOA1-H
HIOA2-H
HIOD0-H
HIOD1-H
HIOD2-H
HIOD3-H
HIOD4-H
HIOD5-H
HIOD6-H
HIOD7-H
READ ONLY MEMORY (ROM)
RANDOM ACCESS MEMORY (RAM)
LATCH AND BUFFER
16-BIT MICROPROCESSOR ADDRESS BUS
MICRO-PROCESSOR CPU
NMI-L
DATA BUS BUFFER
I/O DATA BUS
MICROPROCESSOR DATA BUS
MEMORY DATA BUS
CONTROL SIGNAL GENERATOR
RD-L
WR-L
SOS-L
MEMORY DECODE AND BUS CONTROL LOGIC
MEMORY ADDRESS BUS
COUNTER/ TIMER (CTC)
LATCH AND BUFFER
MOTHERBOARD ADDRESS BUS
ALL SYSTEMS EXCEPT CONTROL PANEL
P1
XA4P1
A0-H
A1-H
A2-H
A3-H
A4-H
A5-H
A6-H
A7-H
A8-H
A9-H
A10-H
A11-H
RD-L
WR-L
D0-H
D1-H
D2-H
D3-H
D4-H
D5-H
D6-H
D7-H
LATCHED ADDRESS BUS
HRST-L
DATA BUS BUFFER
MOTHERBOARD DATA BUS
POWER DISTRIBUTION SYSTEM
MRST-L
PWRDN-H
+12 TST
-12 TST
MRST-L (MASTER RESET FOR ALL CKTS)
CONTROL DATA LOGIC
REGISTER AND PCA SELECT DECODE LOGIC
REGSL-L
SPINDLE ROTATION SYSTEM
SPSPD-H
DOPEN-H
SPDDN-H
SPDSL-L
540 Hz-H
ADDRESS BUS REGISTER DATA BUS
DATA BUS BUFFER
SENSE/ FAULT LOGIC
ANALOG-TO -DIGITAL CONVERTER
HEAD POSITIONING SYSTEM
SOS-L
TFFLT-H
OFTRK-H
ER-H
IP-L
TFTST
SRVTST
ACTTST
ACTSL-L
SRVSL-L
TFSEL-L
MBSEL-L
500 KHz
CLOCK GENERATOR
READ/ WRITE SYSTEM
DM1SL-L
DM2SL-L
IO1SL-L
IO2SL-L
FSSEL-L
EC1SL-L
EC2SL-L
BF1SL-L
BF2SL-L
4 Mz-H
4 MHz-H
7933-320A

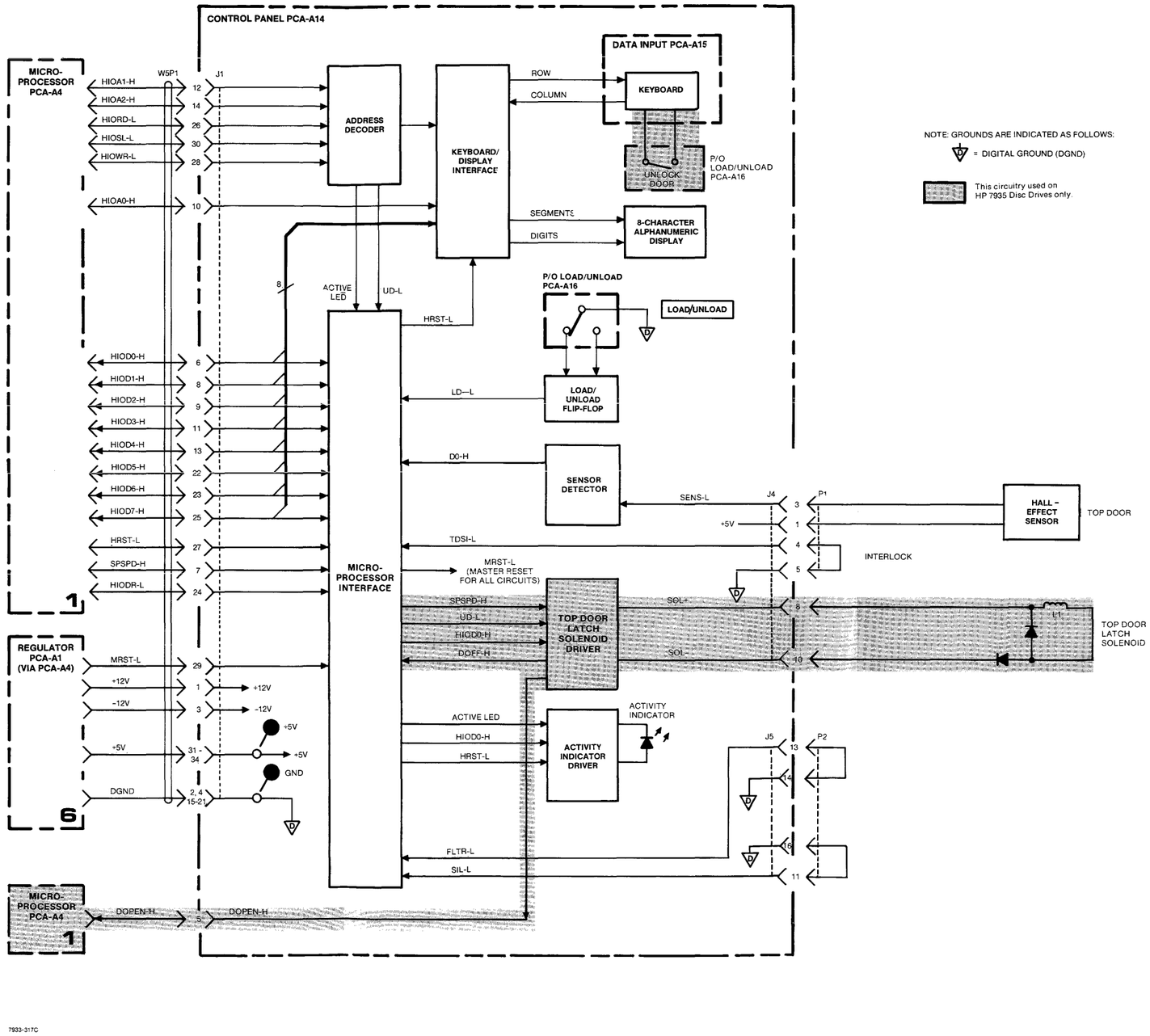


Figure 1-16. Control Panel System, Functional Block Diagram

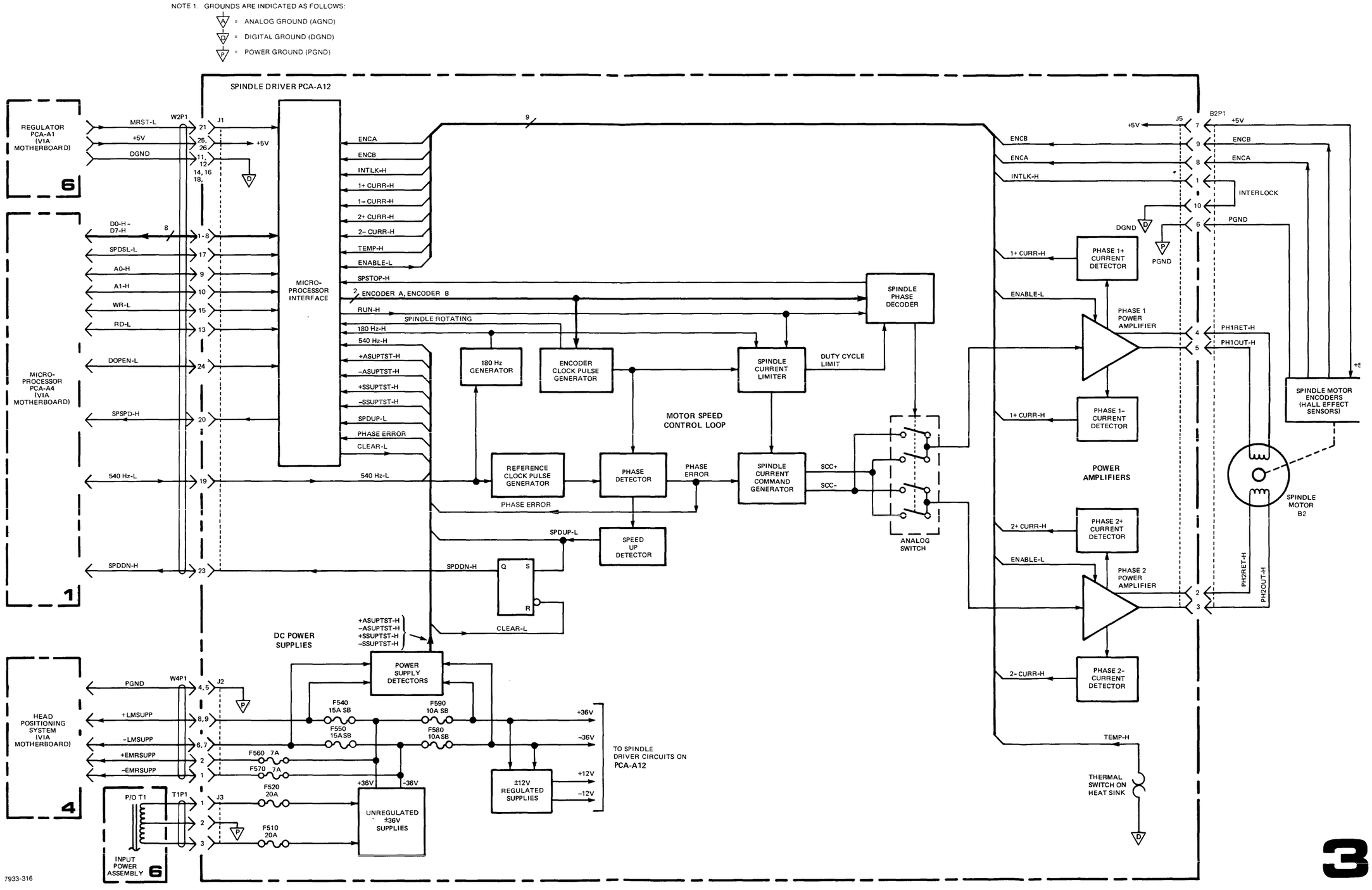
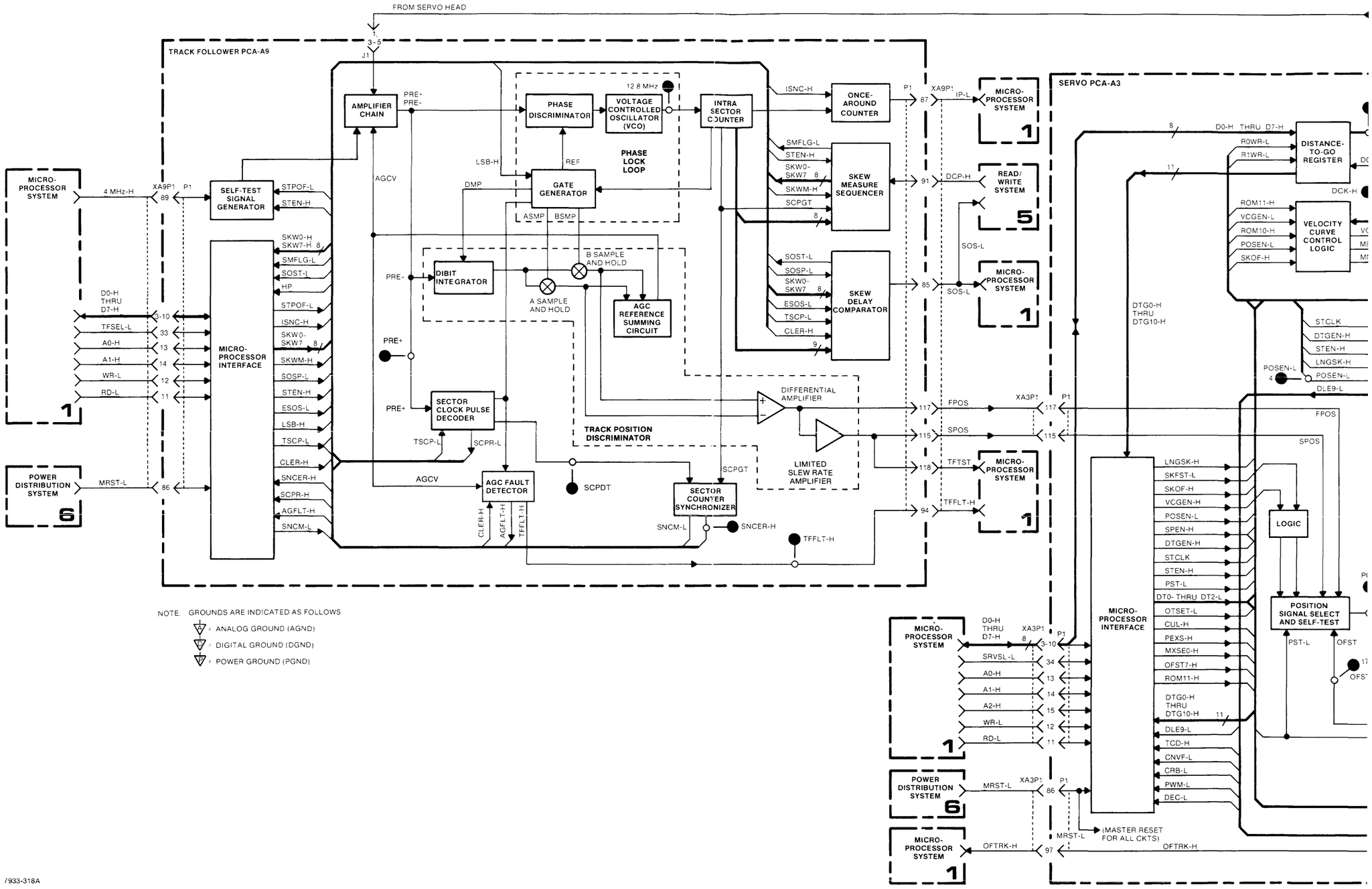


Figure 1-17. Spindle Rotation System, Functional Block Diagram



NOTE: GROUNDS ARE INDICATED AS FOLLOWS

- ⏚ = ANALOG GROUND (AGND)
- ⏚ = DIGITAL GROUND (DGND)
- ⏚ = POWER GROUND (PGND)

7933-318A

ROM SERVO HEAD

PRE-
PRE-

PHASE DISCRIMINATOR

VOLTAGE CONTROLLED OSCILLATOR (VCO)

12.8 MHz

PHASE LOCK LOOP

INTRA SECTOR COUNTER

ISNC-H

ONCE-AROUND COUNTER

P1

XA9P1

IP-L

MICRO-PROCESSOR SYSTEM 1

LSB-H

REF

DMP

GATE GENERATOR

ASMP

BSMP

SMFLG-L
STEN-H
SKW0-SKW7 8
SKWM-H
SCPGT
8

SKEW MEASURE SEQUENCER

91

DCP-H

READ/WRITE SYSTEM 5

SOS-L

SOST-L
SOSP-L
SKW0-SKW7 8
ESOS-L
TSCP-L
CLER-H
9

SKEW DELAY COMPARATOR

85

SOS-L

MICRO-PROCESSOR SYSTEM 1

B SAMPLE AND HOLD

DIBIT INTEGRATOR

A SAMPLE AND HOLD

AGC REFERENCE SUMMING CIRCUIT

DIFFERENTIAL AMPLIFIER

SECTOR CLOCK PULSE DECODER

TRACK POSITION DISCRIMINATOR

LIMITED SLEW RATE AMPLIFIER

117 FPOS

115 SPOS

118 TFTST

94 TFFLT-H

MICRO-PROCESSOR SYSTEM 1

TSCP-L

SCPR-L

SCPGT

AGCV

AGC FAULT DETECTOR

SCPDT

SECTOR COUNTER SYNCHRONIZER

SNCM-L

SNCER-H

TFFLT-H

CLER-H

AGFLT-H

TFFLT-H

SERVO PCA-A3

W1P2

10

9

P O J1

TAC-L

TAC-H

TACHOMETER BUFFER

TAC

VC

LOW PASS FILTER

DRIVE TYPE GAIN SELECT

DT0-L THRU DT2-L

CURRENT COMMAND SELECT LOGIC

POSEN-L

OPOS

POSITION COMPENSATION SELECT

FCEN-L

DECELERATION INDICATOR

DEC-L

DTG0-H THRU DTG10-H

11

VOLTAGE REFERENCE

18

VREF

8

D0-H THRU D7-H

R0WR-L

R1WR-L

DISTANCE-TO-GO REGISTER

DCK-H

VELOCITY CURVE GENERATOR

10

SKOF-H

ROM11-H

VCGEN-L

ROM10-H

POSEN-L

SKOF-H

VELOCITY CURVE CONTROL LOGIC

VCEN-L

MPVEL-L

MNVEL-L

DTG0-H THRU DTG10-H

STCLK

DTGEN-H

STEN-H

LNGSK-H

POSEN-L

DLE9-L

DISTANCE-TO-GO CLOCK CONTROL LOGIC

QTC-H

TCC-H

23

QSEL-L

FPOS

SPOS

LNGSK-H

SKFST-L

SKOF-H

VCGEN-H

POSEN-L

SPEN-H

DTGEN-H

STCLK

STEN-H

PST-L

DT0- THRU DT2-L

OTSET-L

CUL-H

PEXS-H

MXSE0-H

OFST7-H

ROM11-H

DTG0-H THRU DTG10-H

DLE9-L

TCD-H

CNVF-L

CRB-L

PWM-L

DEC-L

MICRO-PROCESSOR INTERFACE

LOGIC

POSITION SIGNAL SELECT AND SELF-TEST

POS

6

CENTER TRACK CROSSING DETECTOR

PST-L

OFST

17

OFST

± QUARTER TRACK CROSSING DETECTOR

POS

AUTO HEAD ALIGNMENT OFFSET DAC

VREF

OPOS

8

OPOS

TRACK CENTER DETECTOR

TCD-H

3

OTSET-L

POSEN-L

OFTRK-H

22

OFTRK-H

OTC-H

OFST0 THRU OFST7

MICRO-PROCESSOR SYSTEM 1

D0-H THRU D7-H

XA3P1

8

3-10

SRVSL-L

34

A0-H

13

A1-H

14

A2-H

15

WR-L

12

RD-L

11

POWER DISTRIBUTION SYSTEM 6

MRST-L

86

MICRO-PROCESSOR SYSTEM 1

OFTRK-H

97

MRST-L

(MASTER RESET FOR ALL CKTS)

CC

12

13

ACUR

LINEAR MODE ERROR AMPLIFIER

LIERR

OFFSET

POS VOLTAGE LEVEL COMPARATOR

STROBE

40 μSEC DELAY

AMPLIFIER MODE ERROR SWITCHING

PTRI

SWERR

TRIANGLE WAVE GENERATOR

NTRI

LIN-H

5

NEG VOLTAGE LEVEL COMPARATOR

LINEAR/SWITCHING MODE CONTROL

PULSE W MODULA

TEST SIGNALS FROM CKTS ON PCA-A3

TAC
TEMP
CCOM
VREF
CC
VC
OFST
POS

ANALOG SIGNAL MULTIPLEXER

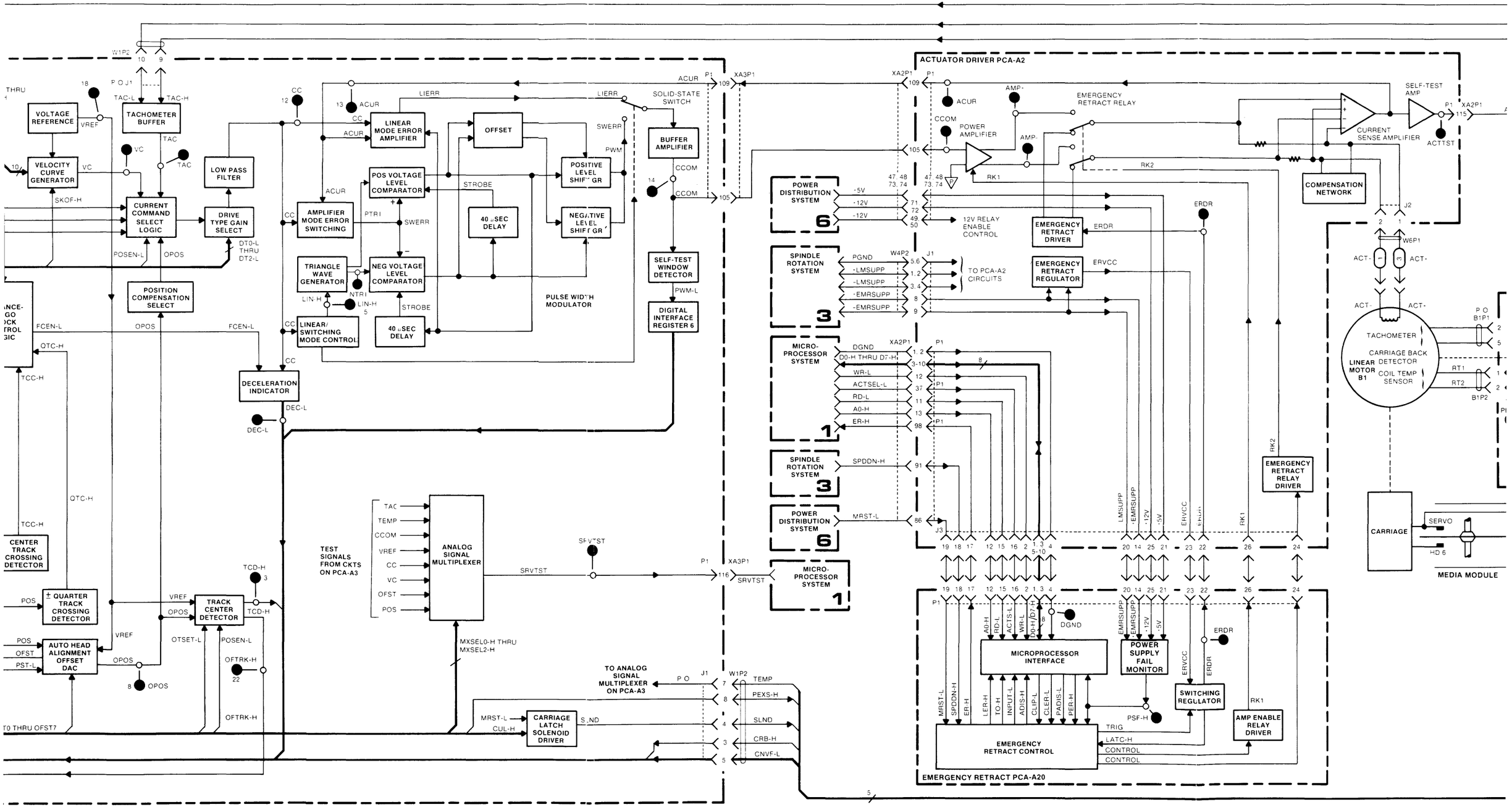
SRVTST

MXSEL0-H THRU MXSEL2-H

MRST-L

CUL-H

CARRIAGE LATCH SOLENOID DRIVER


ACTUATOR DRIVER PCA-A2
VOLTAGE REFERENCE
TACHOMETER BUFFER
VELOCITY CURVE GENERATOR
CURRENT COMMAND SELECT LOGIC
LOW PASS FILTER
DRIVE TYPE GAIN SELECT
POSITION COMPENSATION SELECT
LINEAR MODE ERROR AMPLIFIER
OFFSET
POS VOLTAGE LEVEL COMPARATOR
AMPLIFIER MODE ERROR SWITCHING
TRIANGLE WAVE GENERATOR
NEG VOLTAGE LEVEL COMPARATOR
40 µSEC DELAY
LINEAR/ SWITCHING MODE CONTROL
POSITIVE LEVEL SHIFTER
NEGATIVE LEVEL SHIFTER
PULSE WIDTH MODULATOR
SOLID-STATE SWITCH
BUFFER AMPLIFIER
SELF-TEST WINDOW DETECTOR
DIGITAL INTERFACE REGISTER 6
DECELERATION INDICATOR
CENTER TRACK CROSSING DETECTOR
± QUARTER TRACK CROSSING DETECTOR
TRACK CENTER DETECTOR
AUTO HEAD ALIGNMENT OFFSET DAC
ANALOG SIGNAL MULTIPLEXER
TEST SIGNALS FROM CKTS ON PCA-A3
CARRIAGE LATCH SOLENOID DRIVER
TO ANALOG SIGNAL MULTIPLEXER ON PCA-A3
POWER DISTRIBUTION SYSTEM 6
SPINDLE ROTATION SYSTEM 3
MICRO-PROCESSOR SYSTEM 1
POWER AMPLIFIER
CURRENT SENSE AMPLIFIER
SELF-TEST AMP
EMERGENCY RETRACT RELAY
COMPENSATION NETWORK
12V RELAY ENABLE CONTROL
EMERGENCY RETRACT DRIVER
EMERGENCY RETRACT REGULATOR
TO PCA-A2 CIRCUITS
LINEAR MOTOR B1
TACHOMETER
CARRIAGE BACK DETECTOR
COIL TEMP SENSOR
CARRIAGE
SERVO
HD 6
MEDIA MODULE
EMERGENCY RETRACT RELAY DRIVER
MICROPROCESSOR INTERFACE
POWER SUPPLY FAIL MONITOR
SWITCHING REGULATOR
AMP ENABLE RELAY DRIVER
EMERGENCY RETRACT CONTROL
EMERGENCY RETRACT PCA-A20

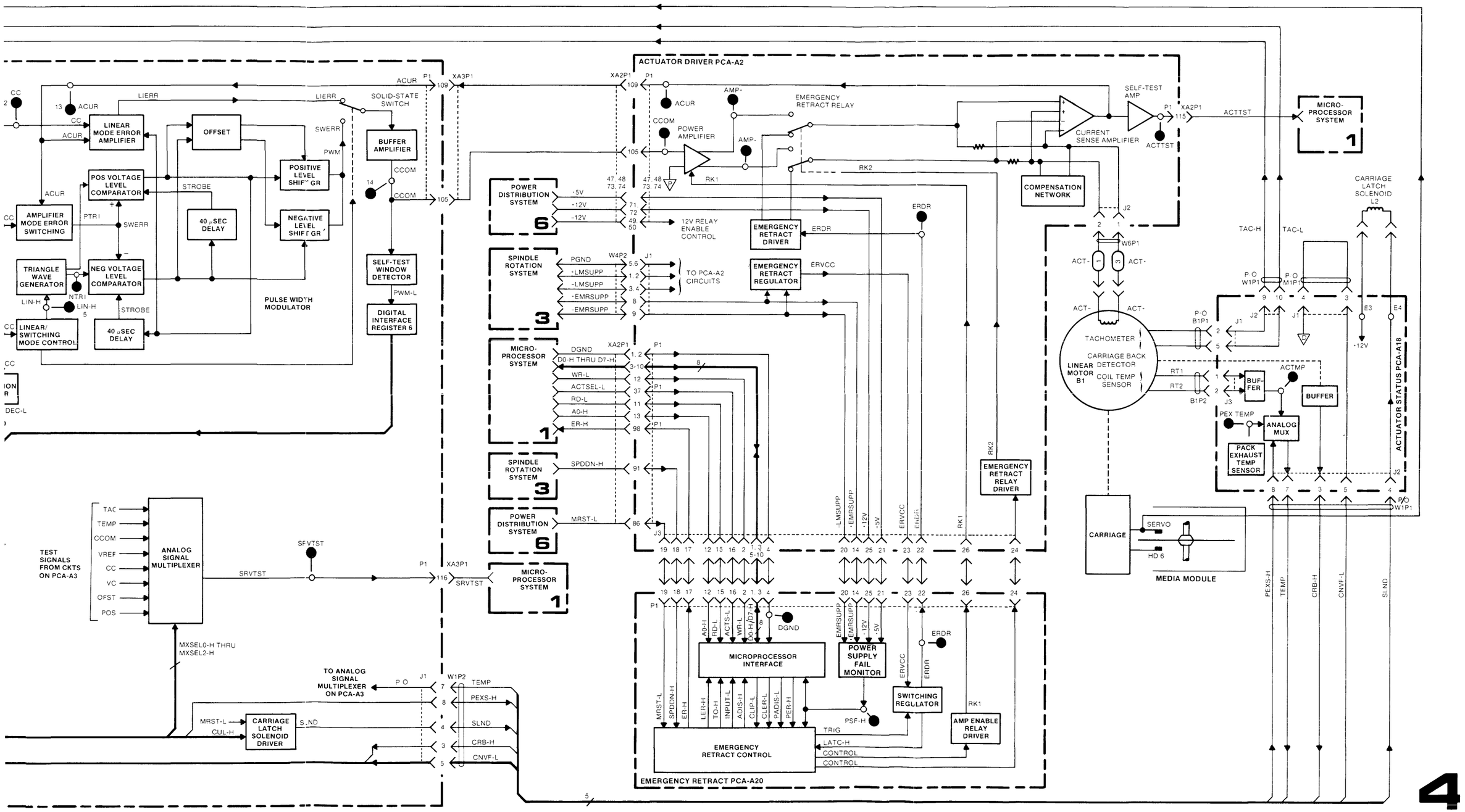


Figure 1-18. Head Positioning System, Functional Block Diagram

NOTE: GROUND IS SHOWN AS FOLLOWS

⏚ - ANALOG GROUND (AGND)

DISC MEMORY ACCESS (DMA) PCA-A6

(See Appendix B for CDMA and Cache PCA functions)

HP-IB PCA-A17

TO/FROM HOST COMPUTER VIA HP-IB

DIO1-L 1, DIO2-L 2, DIO3-L 3, DIO4-L 4, DIO5-L 13, DIO6-L 14, DIO7-L 15, DIO8-L 16, REN-L 17, EOI-L 5, DAV-L 6, NRFD-L 7, NDAC-L 8, IFC-L 9, SRQ-L 10, ATN-L 11

J1 — A17P1 — J1

HP-IB CHANNEL ADDRESS SWITCHES

ADR0-H THRU ADR2-H

HP-IB INTERFACE MODULE

PHI, PHI LATCH, BUFFER, HEADER RAM, BUFFER, BUFFER

ADDRESS BUS

DISC ADDRESS COUNTER

I/O ADDRESS COUNTER

I/O BYTE COUNTER

DATA RAM

DMA BYTE CONTROL

UNER-L, FUNER-L

SOS-L, EOS-L, RWC-L, SOD-L

ECC MODULE

D0-H THRU D7-H, WR-L, RD-L, ECIS-L, A0-H, A1-H

ECC DATA/ CONTROL REGISTER

STATUS, CONTROL

TO/FROM ECC CIRCUITS

CONTROL AND TIMING LOGIC

LINEAR FEEDBACK SHIFT REGISTER

ENCODER/DECODER

LINEAR FEEDBACK SHIFT REGISTER

ERROR DETECTION LOGIC

UNER-L

DIN-H

FIN-H

BUFFER

FOUT-H

DOUT-H, DIN-H, SOD-L, RWC-L, EOS-L

P1: 88, 43, 38, 42, 90, 34

XA6P1

XA8P1: 88, 44, 38, 42, 90, 34, 33

MICRO-PROCESSOR CONTROL SYSTEM

D0-H THRU D7-H — XA6P1 — P1

A0-H THRU A11-H

DMA BUFFER INTERFACE MODULE

ADR0-H THRU ADR2-H

DMA CONTROL/ STATUS REGISTERS

STATUS, CONTROL

TO/FROM DMA CIRCUITS

ECISL-L 41, WR-L 12, RD-L 11, NMI-L 75, IO1SL-L 32, DMISL-L 30, BFISL-L 28

SERDES, SERDES CONTROL, CRC, SECTOR CONTROL

DISC DRIVE INTERFACE LOGIC

DOUT-H, DIN-H, SOD-L, RWC-L, EOS-L

DISC DRIVE INTERFACE MODULE

POWER DISTRIBUTION SYSTEM 6 — MRST-L 86

MRST-L (MASTER RESET FOR ALL CKTS)

HEAD POSITIONING SYSTEM 4 — SOS-L 85

FORMATTER/SEPARATOR PCA-A8

HEAD POSITIONING SYSTEM — SOS-L — XA8P1 85/90 — P1

MICRO-PROCESSOR SYSTEM — D0-H THRU D7-H 3-10, WR-L 12, RD-L 11, A0-H THRU A3-H 13-16, FSSEL-L 36

POWER DISTRIBUTION SYSTEM — MRST-L 86

MICRO-PROCESSOR INTERFACE

TDCP-L, WC0-H – WC2-H, HS0-H THRU HS3-H, DSOS-L, WENC-L, FCLR-L, RWBR-L, MA0-H – MA2-H, STO-L, FLW-L, LSB-H, ST-H, BR0-H THRU BR7-H, HAEN-H, MHF-H, WNDC-H, WNAC-H

STATUS, CONTROL — WEN-L, WRT-L

SOS-L, EOS-L, FUNER-L, FOUT-H, RWC-L, SOD-L, FIN-H, WDD-H

TIMER-SEQUENCER AND CONTROL LOGIC

30-MHz CLOCK GENERATOR

ENCODER

DE-CODER, PPL

RDD-H

P1: 116, 113-115, 109-112, 39, 43, 35, 41, 106-108, 105, 104, 103, 101, 17-24, 32, 30, 29, 28, 27, 37

XA8P1: TDCP-L, WC0-H THRU WC2-H, HS0-H THRU HS3-H, DSOS-H, WENC-L, FCLR-L, RWBR-L, MA0-H THRU MA2-H, STO-L, FLW-L, LSB-H, ST-H, BR0-H THRU BR7-H, HAEN-H, MHF-H, WNDC-H, DCNW-H, WNAC-H

WDD-H — XA10P1

POWER DISTRIBUTION SYSTEM 6

MICRO-PROCESSOR SYSTEM 1

HEAD POSITIONING SYSTEM 4

MICRO-PROCESSOR SYSTEM 1

7933-319B

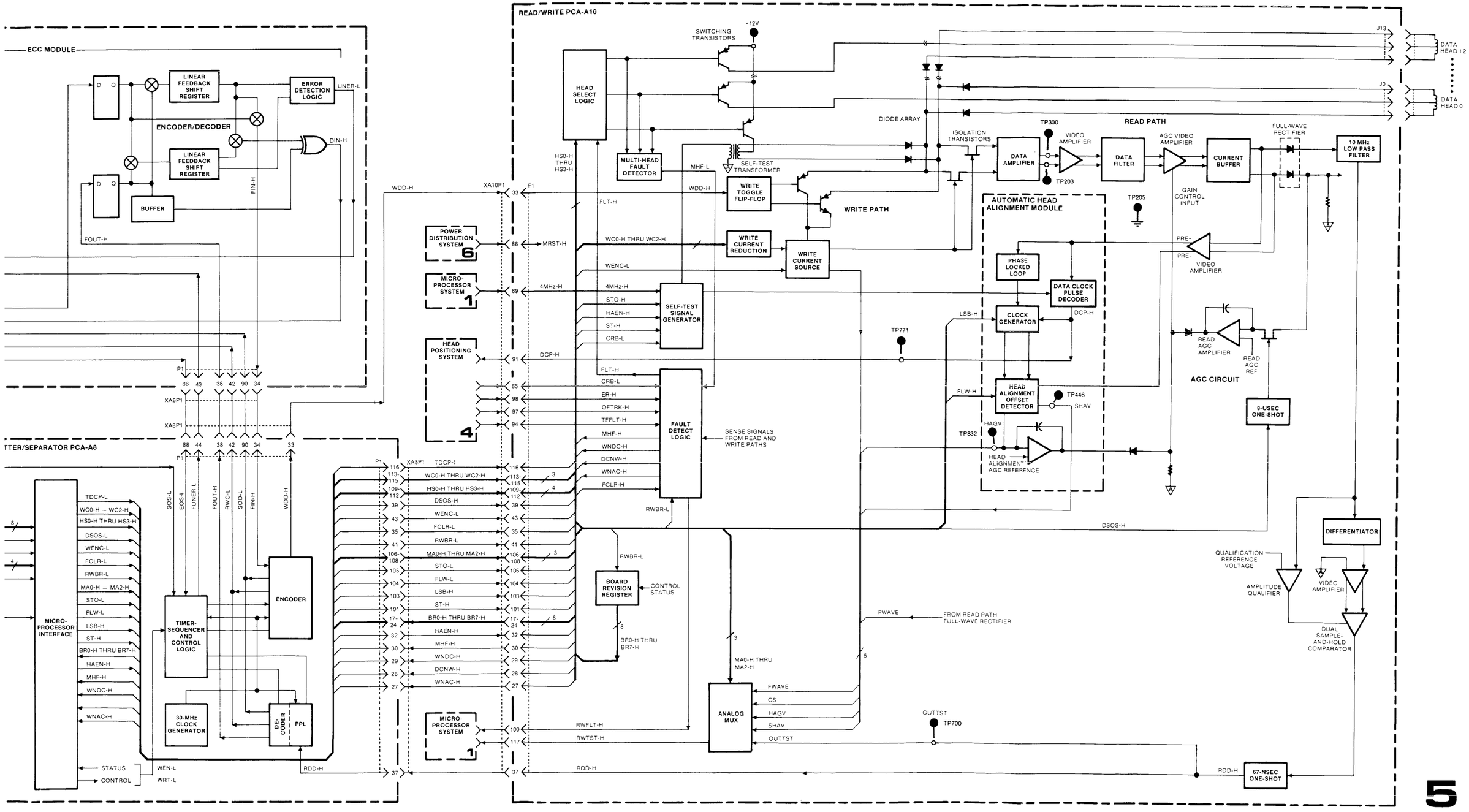
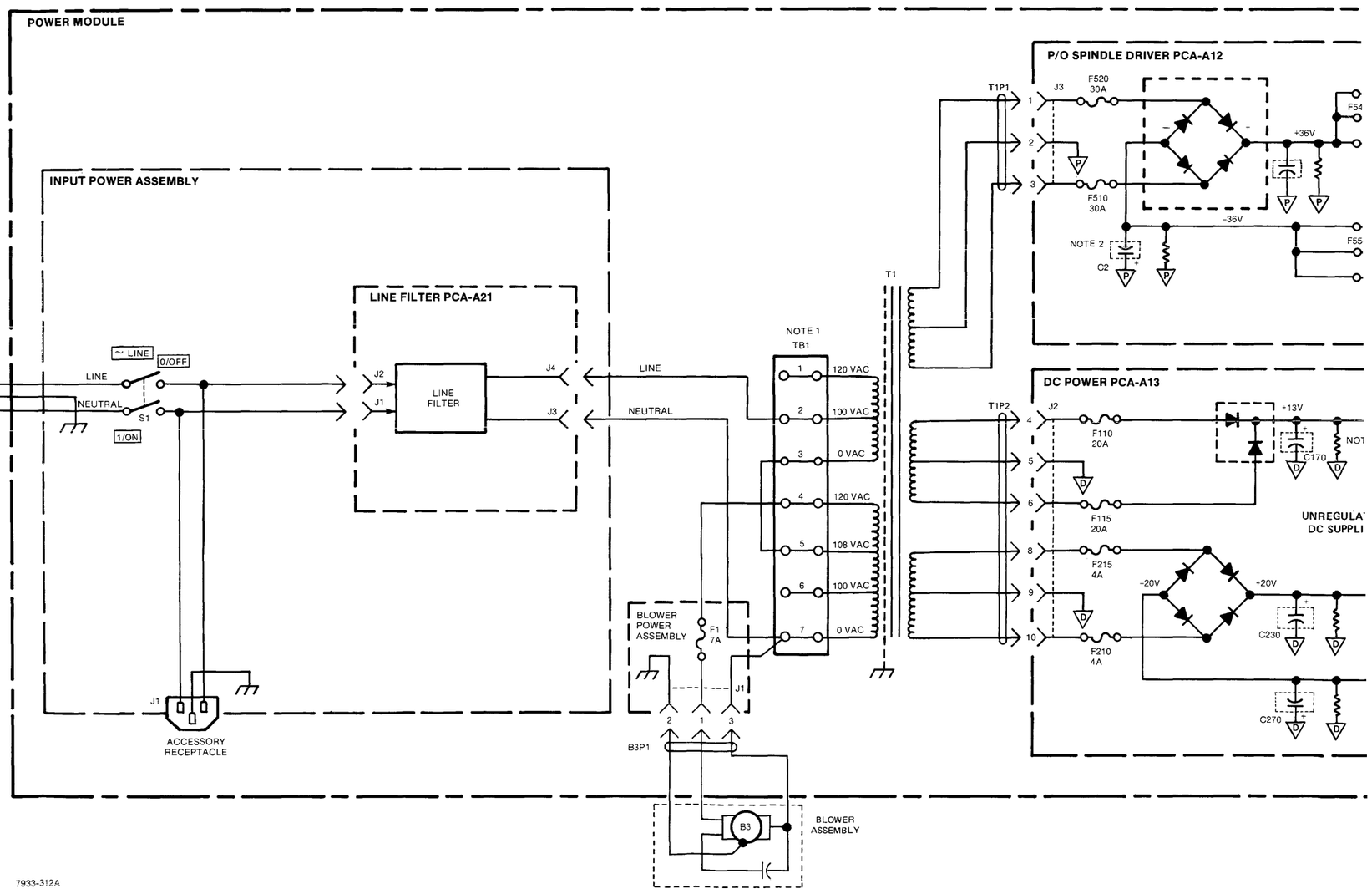


Figure 1-19. Read/Write System, Functional Block Diagram

NOTES:

1. TB1 IS SHOWN JUMPERED FOR 208 VAC (STANDARD) INPUT. JUMPER CONFIGURATIONS FOR OPTIONAL POWER INPUTS (120, 220 AND 240 VAC) ARE SHOWN IN FIGURE 5-20.
2. CAPACITORS C1 AND C2 ARE MOUNTED ON THE POWER MODULE CASTING.
3. CAPACITORS C170, C230 AND C270 ARE MOUNTED ON THE POWER MODULE CASTING.
4. GROUNDS ARE INDICATED AS FOLLOWS:



7933-312A

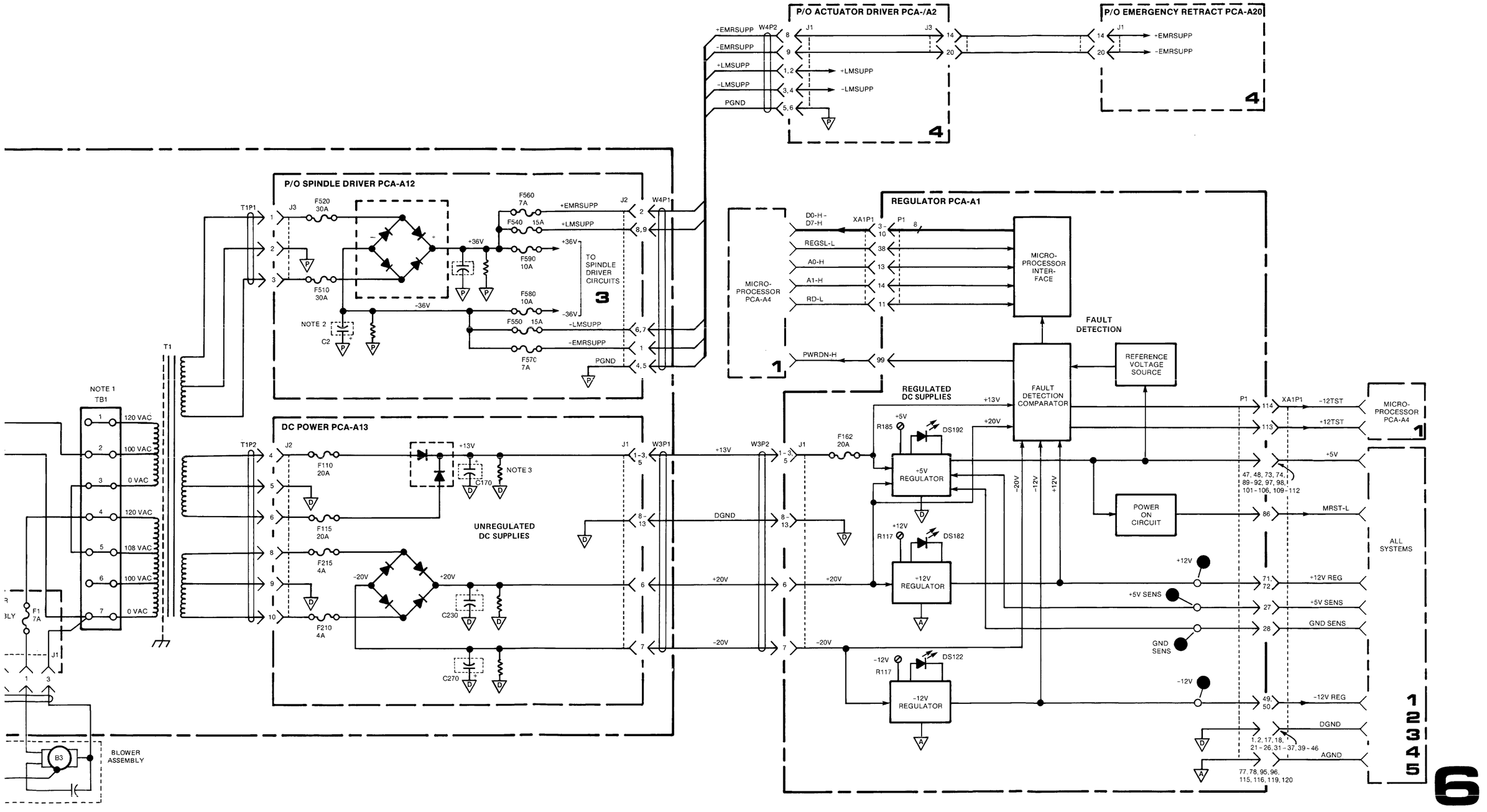


Figure 1-20. Power Distribution System, Functional Block Diagram

CHANNEL INTERFACE

SECTION II

2-1. INTRODUCTION

Interface to the disc drive is accomplished through Hewlett-Packard Interface Bus (HP-IB) hardware and the CS/80 Instruction Set, a set of commands formulated for mass storage devices. The following paragraphs discuss the types of CS/80 commands. Also provided is an overview of HP-IB. For full details of CS/80, refer to the *CS/80 Instruction Set Programming Manual,* part no. 5955-3442.

2-2. CS/80 INSTRUCTION SET

The increase in capabilities of both host computers and mass storage devices has emphasized the need for efficient channel communication. The CS/80 Instruction Set increases the efficiency and speed of channel operations between disc memories and their associated host computers. Table 2-1 is a summary of all CS/80 instructions. The CS/80 Instruction Set allows a host computer to access special utilities within the disc drive. Utilities are routines stored in firmware which allow error rate tests to be performed and the results of such tests to be examined or logged. Utilities are listed in table 2-2. Refer to the *CS/80 External Exerciser Reference Manual,* part no. 5955-3462, for full details.

2-3. TRANSACTION STRUCTURE

A transaction is a logically complete operation between a system host computer and a peripheral device (the disc drive) over a given channel (HP-IB). Three phases may occur during each transaction: command, execute, and report. A transaction begins when a command is received by the disc drive, and ends when a reporting message indicating the status of the transaction is accepted by the host. Figure 2-1 illustrates the transaction structure, and shows the relationship between the disc drive operating states and the channel activity relative to each phase.

A unit is a separately addressable entity within a device (disc drive). A volume is a separately addressable portion of the storage media within a given unit. The controller unit is addressed during diagnostic routines.

2-4. REAL TIME COMMANDS

Real time commands are optimized for execution time. These commands are used most often in host/device transactions. One or more complementary commands may precede a real time command in order to modify the operation of that command. Real time commands include: locate and read, locate and write, and cold load read.

2-5. COMPLEMENTARY COMMANDS

Complementary commands are used to set or update programmable states in the disc drive. The programmable states define characteristics such as: set unit, set address, set block displacement, set return addressing mode, set length, set burst mode, set retry time, set release, set status mask, and set Rotational Position Sensing (RPS) window size. These commands may be included within Real Time, General Purpose, or Diagnostic command messages, or they may stand alone.

When a complementary command (or commands) is embedded within another command, the parameters or conditions established by that complementary command(s) are altered only for the duration of the current command. A stand-alone complementary command, however, sets the parameters or conditions until the same stand-alone complementary command alters the set value or until power-on occurs. Power-on resets all complementary commands to their default values. Therefore, at power-on, length is defaulted to equal the entire volume. A stand-alone Set Length command may give it a "set" value of 1 kbyte to be used for an entire sequence of transactions, although some special case commands could temporarily override this value with an embedded complementary command to set a "current" value of 256 bytes (for 1 sector).

2-6. GENERAL PURPOSE COMMANDS

This command group includes commands which allow the host to determine device type and operating characteristics or to ascertain storage media integrity. These commands are not considered "real time" commands and therefore should not be issued by the host unless it is willing to relinquish control of the drive for a varying period of time. General purpose commands are: locate and verify, spare block, release, release denied, describe, and initialize media.

2-7. DIAGNOSTIC COMMANDS

Diagnostic commands are intended to assist the host in isolating problems in the device to the replaceable assembly level. Some commands allow protected access to variables or data maintained by the device (such as error information), while others cause tests to be performed within the device, or on a specific area of

Table 2-1. Device Command Summary

COMMAND	OPCODE FORMAT					COMMAND FORMAT	FUNCTION
	BINARY	HEX	OCTAL	ASCII	DECIMAL		
LOCATE AND READ (REAL TIME)	<00000000>	00	000	NULL	0	NO VARIABLES OR PARAMETERS	LOCATES DATA INDICATED BY TARGET ADDRESS AND TRANSMITS DATA TO HOST. (PARAGRAPH 2-8)
LOCATE AND WRITE (REAL TIME)	<00000010>	02	002	STX	2	NO VARIABLES OR PARAMETERS	TRANSFERS DATA FROM HOST TO STORAGE AREA BEGINNING AT ADDRESS SPECIFIED BY TARGET ADDRESS. (PARAGRAPH 2-10)
LOCATE AND VERIFY (GENERAL PURPOSE)	<00000100>	04	005	EOT	4	NO VARIABLES OR PARAMETERS	INSTRUCTS DEVICE TO PERFORM AN INTERNAL VERIFICATION OF A SECTION OF DATA TO ENSURE THAT IT CAN BE READ. (PARAGRAPH 2-28)
SPARE BLOCK (GENERAL PURPOSE)	<00000110>	06	006	ACK	6	<00000110> <00000S0T> (P1) P1 = SPARING MODE BYTE S = 0 SKIP SPARE S = 1 JUMP SPARE T = 0 RETAIN DATA T = 1 DO NOT RETAIN DATA T MUST EQUAL 1 FOR TAPE OPERATION S MUST EQUAL 0 FOR DISC OPERATION	ALLOWS HOST TO GIVE DEVICE PERMISSION TO BECOME TEMPORARILY BUSY WHILE SPARING BLOCK INDICATED BY TARGET ADDRESS. (PARAGRAPH 2-27)
COPY DATA (GENERAL PURPOSE)	<00001000>	08	010	BS	8	<00001000> <0VVV0UUU> <0001000T> <P1>------<P6> SET ADDRESS; 6-BYTE PARAMETER ADDRESS OF DATA SOURCE <0XXX0WWW> <0001000T> <P1>------<P6> SET ADDRESS; 6-BYTE PARAMETER ADDRESS OF DATA DESTINATION VVV = VOLUME NUMBER ON UUU FROM WHICH DATA IS COPIED UUU = UNIT NUMBER OF DATA SOURCE T = ADDRESS MODE (0 = SINGLE VECTOR, 1 = 3-VECTOR) XXX = VOLUME NUMBER ON WWW TO WHICH DATA IS COPIED WWW = UNIT NUMBER OF DATA DESTINATION T = ADDRESS MODE (0 = SINGLE VECTOR, 1 = 3-VECTOR)	COPIES AMOUNT OF DATA SPECIFIED BY LENGTH (DEFAULT VALUE, OR COMPLEMENTARY COMMAND VALUE) FROM THE SPECIFIED UNIT AND VOLUME TO A SELECTED UNIT AND VOLUME. (PARAGRAPH 2-29)

Table 2-1. Device Command Summary (continued)

COMMAND	OPCODE FORMAT					COMMAND FORMAT	FUNCTION
	BINARY	HEX	OCTAL	ASCII	DECIMAL		
COLD LOAD READ (REAL TIME)	<00001010>	0A	012	LF	10	NO VARIABLES OR PARAMETERS	USED BY HOST SYSTEM TO BOOTSTRAP ITSELF INTO A HIGHER OPERATING ENVIRONMENT FROM A MORE PRIMITIVE STATE. (PARAGRAPH 2-9)
REQUEST STATUS (DIAGNOSTIC)	<00001101>	0D	015	CR	13	NO VARIABLES OR PARAMETERS	INSTRUCTS DEVICE TO RETURN (IN AN EXECUTION MESSAGE) THE STATUS OF THE LAST TRANSACTION. (PARAGRAPH 2-35)
RELEASE (GENERAL PURPOSE)	<00001110>	0E	016	SO	14	NO VARIABLES OR PARAMETERS	USED TO RELEASE DEVICE FOR A PERIOD OF TIME. (PARAGRAPH 2-30)
RELEASE DENIED (GENERAL PURPOSE)	<00001111>	0F	017	SI	15	NO VARIABLES OR PARAMETERS	PROHIBITS DEVICE FROM RELEASING ITSELF. (PARAGRAPH 2-31)
SET ADDRESS (COMPLEMENTARY)	<00010000> <00010001>	10 11	020 021	DLE DC1	16 17	<0001000T> < P1 > - - - - - - - - - - - - < P6 > 6-BYTE PARAMETER T = ADDRESS MODE (0 = SINGLE VECTOR, 1 = 3-VECTOR) SINGLE VECTOR FORMAT: 6-BYTE BINARY NUMBER 3-VECTOR FORMAT: P1 - P3 = CYLINDER ADDRESS P4 = HEAD ADDRESS P5 - P6 = SECTOR ADDRESS	USED TO SET VALUE OF TARGET ADDRESS. SPECIFIES SINGLE- OR THREE-VECTOR ADDRESS MODE. (PARAGRAPH 2-14)
SET BLOCK DISPLACEMENT (COMPLEMENTARY)	<00010010>	12	022	DC2	18	<00010010> < P1 > - - - - - - - - - - - - < P6 > 6-BYTE PARAMETER PARAMETER FORMAT: 6-BYTE, SIGNED, TWO'S COMPLEMENT, BINARY NUMBER	ADJUSTS TARGET ADDRESS BY NUMBER OF BLOCKS INDICATED BY PARAMETER FIELD. (PARAGRAPH 2-15)
SET LENGTH (COMPLEMENTARY)	<00011000>	18	030	CAN	24	<00011000> < P1 > - - - - - - - - - - - - < P4 > 4-BYTE PARAMETER PARAMETER FORMAT: 4-BYTE, UNSIGNED BINARY NUMBER	DEFINES THE NUMBER OF BYTES IN A DATA TRANSFER. (PARAGRAPH 2-16)

Table 2-1. Device Command Summary (continued)

COMMAND	OPCODE FORMAT					COMMAND FORMAT	FUNCTION
	BINARY	HEX	OCTAL	ASCII	DECIMAL		
SET UNIT (COMPLEMENTARY)	<00100000> <00100001> <00100010> <00100011> <00100100> <00100101> <00100110> <00100111> <00101000> <00101001> <00101010> <00101011> <00101100> <00101101> <00101110> <00101111>	20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F	040 041 042 043 044 045 046 047 050 051 052 053 054 055 056 057	space ! " # $ % & ' (apostrophe) ( ) * (asterisk) + , (comma) - . /	32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47	<0010YYYY> YYYY = UNIT NUMBER (1111 = DEVICE CONTROLLER)	USED TO SPECIFY A SPECIFIC UNIT NUMBER WITHIN A MASS STORAGE DEVICE. (PARAGRAPH 2-12)
INITIATE UTILITY (DIAGNOSTIC)	<00110000> <00110001> <00110010>	30 31 32	060 061 062	0 1 2	48 49 50	<001100XX> < P1 > <P2>----------<P9> UP TO 8-BYTE PARAMETER XX = EXECUTION MESSAGE QUALIFIER 00 = NO EXECUTION MESSAGE 01 = DEVICE WILL RECEIVE EXECUTION MESSAGE TEXT 10 = DEVICE WILL SEND EXECUTION MESSAGE TEXT P1 = UTILITY NUMBER (DEVICE SPECIFIC) PARAMETER QUANTITY AND CONTENT IS FUNCTION OF P1.	DIRECTS DEVICE TO PERFORM ONE UTILITY ROUTINE. (PARAGRAPH 2-33)
INITIATE DIAGNOSTIC (DIAGNOSTIC)	<00110011>	33	063	3	51	<00110011>< P1 > < P2 > < P3 > 3-BYTE PARAMETER P1 - P2 = LOOP PARAMETER P3 = DIAGNOSTIC SECTION NUMBER	DIRECTS DEVICE TO PERFORM ONE INTERNALLY DEFINED DIAGNOSTIC ROUTINE. (PARAGRAPH 2-34)
NO OP (COMPLEMENTARY)	<00110100>	34	064	4	52	NO VARIABLES OR PARAMETERS	CAUSES DEVICE TO DISREGARD MESSAGE BYTE. (PARAGRAPH 2-21)
DESCRIBE (GENERAL PURPOSE)	<00110101>	35	065	5	53	NO VARIABLES OR PARAMETERS	DIRECTS DEVICE TO RETURN INFORMATION ABOUT ITSELF. (PARAGRAPH 2-25)

Table 2-1. Device Command Summary (continued)

COMMAND	OPCODE FORMAT					COMMAND FORMAT	FUNCTION
	BINARY	HEX	OCTAL	ASCII	DECIMAL		
INITIALIZE MEDIA (GENERAL PURPOSE)	<00110111>	37	067	7	55	<00110111><00000CWZ>< P2 > CWZ = INITIALIZE OPTIONS CWZ FOR TAPE UNIT Z = 0 REWRITE SPARING TABLE WITH NO JUMP SPARES Z = 1 RESET SPARING TABLE TO INITIAL SPARES W = 0 INITIAL SPARES ARE EVERY 512TH BLOCK WITH TRACK OFFSET W = 1 INITIAL SPARES ARE NO SPARES C = 0 RUNS CERTIFICATION UTILITY ON TAPE C = 1 INHIBITS CERTIFY TEST (MEDIA REMAINS UNINITIALIZED) CWZ FOR DISC UNIT 000 = RETAIN BOTH FACTORY (PRIMARY) AND FIELD (SECONDARY) SPARES 001 = RETAIN FACTORY SPARES ONLY 010 = RETAIN NO SPARES (CE USE ONLY) P2 = BLOCK INTERLEAVE BYTE (BINARY NUMBER) MUST BE 00 FOR TAPE	USED TO INITIALIZE ALL OF THE DATA FIELDS OF THE DEFINED MEDIA AREA (CURRENT UNIT NUMBER AND VOLUME). (PARAGRAPH 2-26)
SET OPTIONS (COMPLEMENTARY)	<00111000>	38	070	8	56	<00111000><00000VYZ> P1 P1 = OPTION BYTE VYZ FOR TAPE UNIT V = 0 DISABLE AUTO SPARING V = 1 ENABLE AUTO SPARING Y = 0 JUMP SPARE Y = 1 SKIP SPARE Z = 0 DISABLE CHARACTER COUNT Z = 1 ENABLE CHARACTER COUNT	USED TO SET DEVICE SPECIFIC OPTIONS. (PARAGRAPH 2-23)
SET RPS (COMPLEMENTARY)	<00111001>	39	071	9	57	<00111001>< TIME 1 >< TIME 2 > TIME 1 = TIME-TO-TARGET IN HUNDREDS OF MICROSECONDS TIME 2 = WINDOW-SIZE IN HUNDREDS OF MICROSECONDS	SETS TIME-TO-TARGET AND WINDOW-SIZE TIME INTERVALS FOR RPS DATA TRANSFERS. (PARAGRAPH 2-18)
SET RETRY TIME (COMPLEMENTARY)	<00111010>	3A	072	:	58	<00111010>< P1 >< P2 > P1 - P2 = RETRY TIME IN TENS OF MILLISECONDS (16 BIT BINARY NUMBER)	USED TO SET AMOUNT OF TIME AVAILABLE FOR READ AND SEEK RETRIES. (PARAGRAPH 2-19)

Table 2-1. Device Command Summary (continued)

COMMAND	OPCODE FORMAT					COMMAND FORMAT	FUNCTION
	BINARY	HEX	OCTAL	ASCII	DECIMAL		
SET RELEASE (COMPLEMENTARY)	<00111011>	38	073	;	59	<00111011> <TZ000000> T = 1 SUPPRESS RELEASE TIME-OUT Z = 1 RELEASE AUTOMATICALLY DURING IDLE TIME	USED TO SUPPRESS RELEASE TIME-OUT AND TO ENABLE AUTOMATIC RELEASE. (PARAGRAPH 2-22)
SET BURST (COMPLEMENTARY)	<00111100> <00111101>	3C 3D	074 075	< =	60 61	<0011110T>< P1 > T = 0 INDICATES THAT LAST BURST ONLY IS TAGGED WITH A MESSAGE TERMINATOR (EOI ON HP-IB). T = 1 INDICATES THAT ALL BURSTS ARE TAGGED WITH A MESSAGE TERMINATOR. P1 = NUMBER OF 256-BYTE SEGMENTS IN EACH BURST (IF P1 = ALL ZEROES, BURST MODE IS DEACTIVATED).	ACTIVATES AND DEACTIVATES BURST MODE. (PARAGRAPH 2-17)
SET STATUS MASK (COMPLEMENTARY)	<00111110>	3E	076	>	62	<00111110> < P1 > - - - - - - - - - - - - < P8 > 8-BYTE PARAMETER PARAMETER FORMAT: BIT POSITIONS IN PARAMETER BYTES CORRESPOND TO STATUS REPORT ERROR BIT POSITIONS. REFER TO PARAGRAPH 2-35 IN CS/80 REFERENCE MANUAL. 1 = MASKED ERROR	ALLOWS MASKING OF ERROR CONDITIONS REPORTED BY REQUEST STATUS (DIAGNOSTIC) COMMAND. (PARAGRAPH 2-20)
SET VOLUME (COMPLEMENTARY)	<01000000> <01000001> <01000010> <01000011> <01000100> <01000101> <01000110> <01000111>	40 41 42 43 44 45 46 47	100 101 102 103 104 105 106 107	@ A B C D E F G	64 65 66 67 68 69 70 71	<01000YYY> YYY = VOLUME NUMBER	USED TO SPECIFY DESIRED STORAGE VOLUME OF A SPECIFIED STORAGE DEVICE. (PARAGRAPH 2-13)
SET RETURN ADDRESSING MODE (COMPLEMENTARY)	<01001000>	48	110	H	72	<01001000> <00000TTT> TTT = ADDRESSING MODE 000 = SINGLE VECTOR 001 = 3-VECTOR	USED BY HOST TO SPECIFY TYPE OF ADDRESS (SINGLE- OR THREE-VECTOR) TO BE RETURNED IN REQUEST STATUS EXECUTION MESSAGE. (PARAGRAPH 2-24)

Table 2-1. Device Command Summary (continued)

COMMAND	OPCODE FORMAT					COMMAND FORMAT	FUNCTION
	BINARY	HEX	OCTAL	ASCII	DECIMAL		
WRITE FILE MARK (REAL TIME)	<01001001>	49	111	I	73	NO VARIABLES OR PARAMETERS	WRITES A FILE MARK AT THE CURRENT POSITION OF THE TAPE. (PARAGRAPH 2-11)
UNLOAD (GENERAL PURPOSE)	<01001010>	4A	112	J	74	NO VARIABLES OR PARAMETERS	USED TO UNLOAD THE TAPE. (PARAGRAPH 2-32)

Table 2-2. Disc Drive Utilities

UTILITY OPCODE(S) ALLOWED* (HEX)	MICRO OPCODE (HEX)	UTILITY PERFORMED BY THE DISC DRIVE
32	C0	Read Full Sector
32	C2	Read Revision Numbers
32	C4	Read Drive Tables
32	C5	Read Run Time Data Error Log
32	C6	Read Error Rate Test Data Error Log
32	C7	Read Fault Log
30, 32	C8	Initiate Pattern Error Rate Test
30, 32	C9	Initiate Read Only Error Rate Test
30, 32	CA	Initiate Short Error Rate Test
30, 32	CB	Initiate Random Error Rate Test
30, 32	CC	Initiate Random Read Only Error Rate Test
30	CD	Clear Logs
30	CE	Preset Device
31	D1	Receive User Pattern

*Opcode 30 Executes Utility With No Message
Opcode 31 Executes Utility Receive Message
Opcode 32 Executes Utility Send Message

the storage media. Diagnostic commands may be modified by complementary commands. Initialize diagnostic, initialize utility, and request status are all diagnostic commands.

2-8. TRANSPARENT MESSAGES

Transparent commands compensate for different types of channels and differences in operating environments. Transparent commands are intercepted by the device firmware and modify the normal command-execution-reporting transaction sequence. Transparent commands are explained in the *CS/80 Instruction Set Programming Manual,* part no. 5955-3442.

2-9. HEWLETT-PACKARD INTERFACE BUS

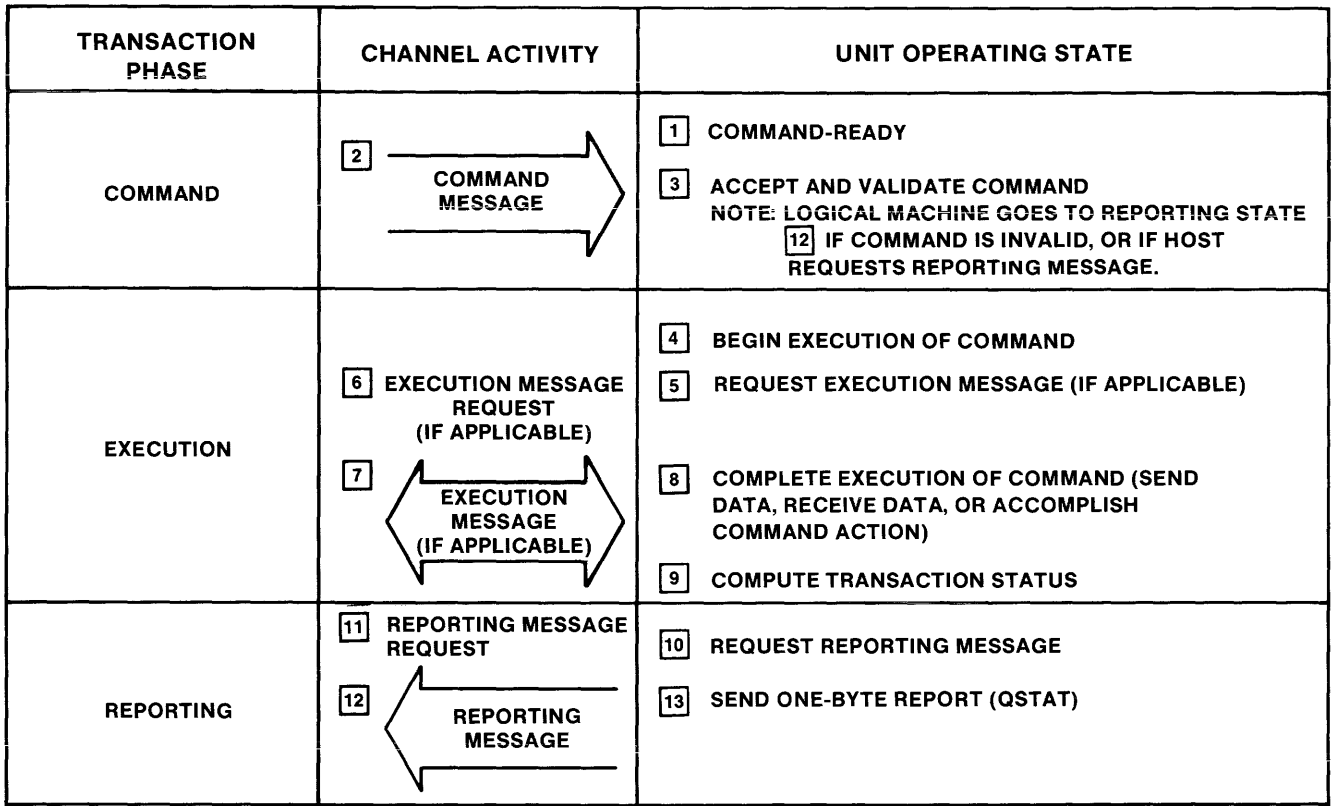
The Hewlett-Packard Interface Bus (HP-IB) provides a standardized method of connecting separate devices (see figure 2-2). The HP-IB permits transfer of commands and data between the components of a system on 16 signal lines. The interface functions for each system component are performed within the component so only passive cabling is needed to connect the system. The cable connects all controllers and other devices of the system in parallel.

The Hewlett-Packard Interface Bus (HP-IB) has certain rules which must be followed for successful installation of the disc drive. Cabling is limited to 1 metre per HP-IB load. Typically the Central Processing Unit (CPU) is 7 equivalent loads and the disc drive is 1 equivalent load.

The CPU adheres to an HP standard which allows 7 metres of HP-IB cable between the CPU and the nearest device connected to it and 1 metre of cable between each additional device. The maximum configuration is eight devices (not including CPU) per HP-IB channel or a maximum of 15 metres or 15 equivalent loads.

The eight Data I/O lines are reserved for the transfer of commands, data, and other messages in a byte-serial, bit-parallel manner. Data and message transfers are asynchronous, coordinated by three handshake lines: Data Valid (DAV-L), Not Ready For Data (NRFD-L), and Not Data Accepted (NDAC-L). The other five lines are for bus management.

Information is transmitted on the data lines under sequential control of the three handshake lines (DAV-L, NRFD-L and NDAC-L). No step in the sequence can be initiated until the previous step has been completed. Information transfer can proceed as fast as devices can respond, but no faster than allowed by the slowest device presently addressed. This permits several devices to receive the same message byte concurrently.



[1] Logical Machine idle in command-ready state.

[2] Host sends command message.

[3] Logical Machine accepts and verifies command. If command is valid, Logical Machine moves to execution state. If not, Logical Machine moves to reporting state.

[4] Unit begins execution of command.

[5] [6] If command involves data transfer, Logical Machine requests an execution message. If not, unit completes execution.

[7] Execution message is established if command involves a data transfer.

[8] Unit completes execution of command. If command involves data transfer, unit sends or receives data through channel module. If not, unit completes action called for in command message.

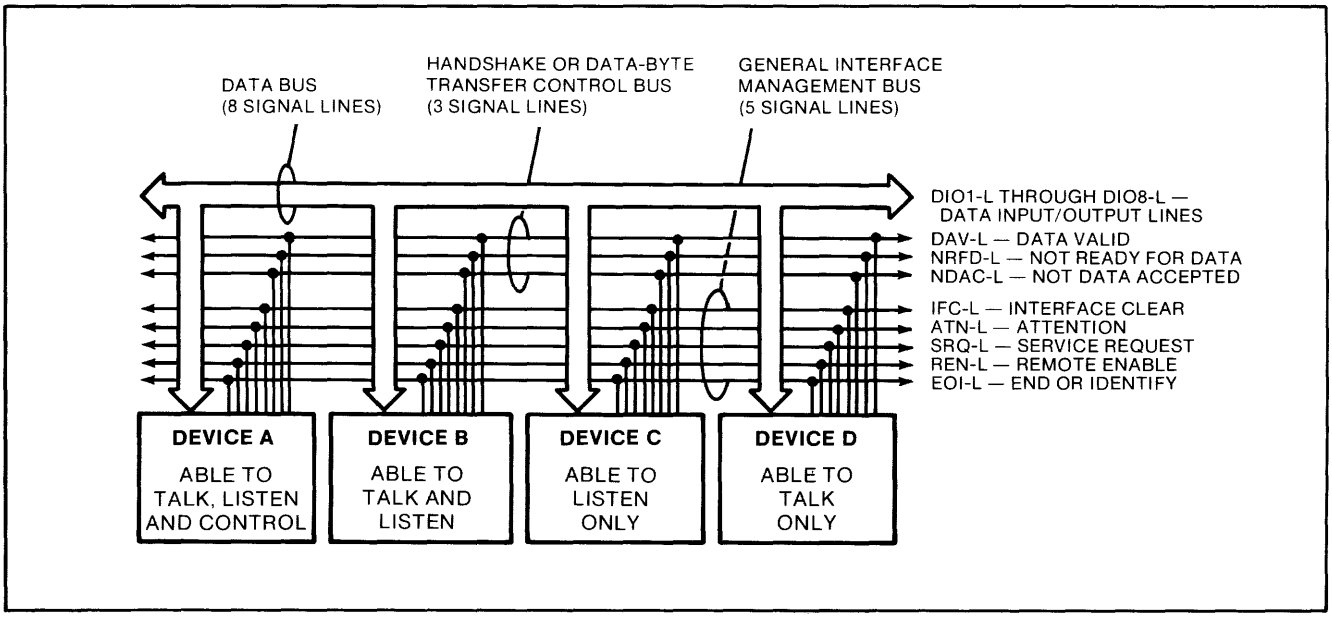
[9] Logical Machine computes completion status of transaction. Pass/Fail status is set into QSTAT, complete status set into request status.

[10] [11] Logical Machine requests reporting message.

[12] Reporting message is established.

[13] Logical Machine sends one-byte reporting message (QSTAT) indicating Pass/Fail status of transaction. Host must send request status command for complete status report (20 bytes).

Figure 2-1. Transaction Structure



5955-3

Figure 2-2. Hewlett-Packard Interface Bus Signal Lines

Devices connected to the bus may be talkers, listeners, or controllers (refer to table 2-3). The Controller-In-Charge (CIC) dictates the role of each of the other devices by setting the Attention (ATN-L) line low and sending talk or listen addresses on the data lines. Addresses are set for each device at the time of system configuration. While the ATN-L line is low, all devices must listen to the data lines. When the ATN-L line is high, devices that have been addressed will send or receive data; all others ignore the data lines. Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN-L is low), all other talkers will be automatically unaddressed.

The Interface Clear (IFC-L) line places the interface system in a known quiescent state. The Remote Enable (REN-L) line is used to select between two alternate sources of device programming data such as the front panel or the HP-IB. The End Or Identify (EOI-L) line is used to indicate the end of a multiple-byte transfer sequence. In addition, when a controller-in-charge sets both the ATN-L and EOI-L lines low, each device capable of a parallel poll responds on the DIO line assigned to it.

2-10. HP-IB COMMUNICATIONS

This section describes the formats and sequences for the HP-IB commands, messages, and transactions that occur between the Controller-In-Charge (CIC) and the disc drive. The following list explains the terms used in this section.

Table 2-3. HP-IB Definitions

HP-IB TERM	DEFINITION	CONSIDERATIONS
TALKER	Any device which sends information over the HP-IB.	There can be only one TALKER sending information over the HP-IB at a time.
LISTENER	Any device which receives information over the HP-IB. Some devices can function as LISTENERS or TALKERS.	In a parallel poll system, there can be up to 8 LISTENERS receiving information over the HP-IB at the same time.
CONTROLLER	Any device that has been programmed to manage data flow between the TALKER and the LISTENER (s) in addition to being a TALKER and a LISTENER.	The CONTROLLER manages data flow by addressing one device as a TALKER and one or more devices as LISTENERS. There can be only one actice CONTROLLER on the HP-IB at any time. The active CONTROLLER is called the CONTROLLER-IN-CHARGE (CIC).
SYSTEM CONTROLLER	Any device that functions as a CONTROLLER and is able to gain absolute control of the HP-IB with the Interface Clear (IFC) signal.	There can be only one SYSTEM CONTROLLER connected to the HP-IB.

COMMAND — A parcel of information transmitted over the channel (HP-IB) relating to a specific operation. Channel commands (usually a single byte) are used to manage operations on the interface channel. Device commands (usually more than one byte) are used to control the operation and are contained within the text of a command message.

UNIVERSAL COMMAND — A channel command that causes all devices on the bus to perform a predetermined interface function. Refer to table 2-4.

Table 2-4. Universal Command Formats

UNIVERSAL COMMAND	UNIVERSAL DEVICE CLEAR
ATN [P001CCCC] P = Parity Bit CCCC = Command Code	ATN [P0010100] P = Parity Bit

PRIMARY COMMAND — The primary I command is a channel command that begins the message sequence. It contains the command to listen or talk and the address of a particular device. The primary II command terminates the message with an unlisten or untalk command.

SECONDARY COMMAND — The secondary command sets up the action required of the disc drive in the text of the message.

TEXT — The text of the message can be 1 to n bytes depending on the required action. The required action can be to receive further qualifying information or instructions (such as a device command), to receive write data, to send read or status data, or to perform a specific operation such as a CLEAR.

MESSAGE — A unique sequence of command and text bytes transmitted over the channel during which the communication link between the devices (for example, CIC and the disc drive) remains unbroken.

COMMAND MESSAGE — A single message containing all the information required to address a device and initiate an operation, set up a programmable parameter, or set up an operation to be executed by an execution message.

EXECUTION MESSAGE — A single message containing all the information required to carry out an operation previously set up by a command message.

TRANSACTION — A complete process or operation carried out over the channel. Some transactions are completed with only a command/report message, and some require a command, execution, and a reporting message.

2-11. CHANNEL MANAGEMENT

The following techniques are used by the CIC to manage the HP-IB: Parallel Poll and Universal Device Clear.

2-12. PARALLEL POLL. The CIC conducts a parallel poll on the HP-IB by asserting ATN-L and EOI-L simultaneously. Each device requiring service can then respond by asserting the DIO line corresponding to its address. The CIC then addresses only the device requiring service. If more than one device requires service, the CIC addresses the device with the highest priority (lowest address) first. Parallel Poll Enable (PPE) and Parallel Poll Disable (PPD) are internal states of the disc drive controller. PPE occurs when the disc drive requires service from the CIC. PPD is the opposite state and occurs whenever the disc drive is active (for example, busy executing a command) or idle. A Parallel Poll Response (PPR) from the disc drive will occur if the CIC asserts both ATN-L and EOI-L and if the disc drive is in the PPE state.

2-13. UNIVERSAL DEVICE CLEAR. A universal command is a channel command that causes all devices on the HP-IB to perform a pre-determined interface function. Universal Device Clear erases information stored in the disc drive controller and places the disc drive in a known reset state. The universal device clear format is shown in table 2-4.

2-14. MESSAGE STRUCTURE

Each message contains the following components (refer to table 2-5).

— Primary I Command
(unidirectional from CIC to device)

— Secondary Command
(unidirectional from CIC to device)

— Text (bidirectional)

— Primary II Command
(unidirectional from CIC to device)

The CIC asserts ATN-L during primary and secondary commands to distinguish them from text information. The disc drive decodes the information contained in both the primary I and secondary commands to prepare for action specified in the text.

Table 2-5. HP-IB Message Structure

HEADER		TEXT	TRAILER
PRIMARY I	**SECONDARY**	**DEVICE COMMAND OR DATA**	**PRIMARY II**
[ATN] **[ONE BYTE]** — UNIDIRECTIONAL • CIC TO DEVICE — BEGINS MESSAGE • ADDRESSES DEVICE TO LISTEN OR TALK • UNIVERSAL	**[ATN]** **[ONE BYTE]** — UNIDIRECTIONAL •CIC TO DEVICE — SET UP DEVICE FOR FURTHER ACTION	**[ONE TO n BYTES]** — BIDIRECTIONAL — QUALIFYING INSTRUCTIONS TO DEVICE — WRITE DATA TO DEVICE — READ DATA TO CIC — STATUS DATA TO CIC	**[ATN]** **[ONE BYTE]** — UNIDIRECTIONAL • CIC TO DEVICE — TERMINATES MESSAGE — UNADDRESSES DEVICE • UNLISTEN • UNTALK

MAINTENANCE

SECTION III

3-1. INTRODUCTION

WARNING

The disc drive does not contain operator-serviceable parts. To prevent electrical shock, refer all installation and maintenance activities to qualified service-trained personnel.

This section contains maintenance precautions, lists of tools and test equipment required, and maintenance instructions. Maintenance of the disc drive must be performed by qualified service-trained personnel.

3-2. MAINTENANCE PRECAUTIONS

To avoid injury to personnel and to prevent damage to equipment, observe the following safety precautions:

WARNING

- **Observe all warnings and cautions provided in this manual and affixed to the equipment.**
- **Use extreme caution when working on the disc drive with the covers removed. Hazardous voltages are present inside the disc drive when the power cable is attached to an active ac power source.**
- **Do not attempt to remove or change printed-circuit assemblies, interconnecting cables, or system cables while ac power is applied to the disc drive.**

CAUTION

- Do not run the disc drive without an absolute filter installed. Severe contamination in the head/disc area may result in damage to the heads and/or disc surfaces.
- Use only the brands of cleaning materials specified in table 3-1. Other brands of cleaning materials may contain contaminating oils and/or lint which could leave a harmful residue.
- Use only the type of alcohol specified in table 3-1. Some other types contain impurities that could cause damage.
- Avoid applying excessive pressure to the gimbal area of a head while cleaning. Excessive pressure may alter or damage the head characteristics which are precision set at the factory.
- Never place an inspection mirror between the heads or allow it to touch the heads. The flying characteristics of the heads may be altered or damaged.
- Do not use oil or other similar lubricants anywhere in the disc drive except where specified.
- Do not turn the disc drive power on or off when the system bus is in an active state (Activity indicator illuminated).
- Do not connect or disconnect the HP-IB cable from the disc drive when the system bus is in an active state (Activity indicator illuminated).
- Do not operate the disc drive with the power module cover removed. This will reduce the efficiency of the disc drive RFI shielding.
- Do not attempt to power up the disc drive with the power module cover removed, or the power module withdrawn from the enclosure. This will interrupt the flow of cooling air in the enclosure and cause overheating and possible damage to the equipment.
- Do not attempt to manually extend the carriage assembly, unless the head spacer tool, part no. 07930-

60154, is installed and there is no media module in the disc drive; otherwise head damage will occur.

- Precautions must be taken during maintenance of the disc drive to avoid accidental erasure of data. Normal writes initiated from the host CPU or the disc drive control panel (diagnostic commands) can overwrite data. Such writes must be restricted to prescripted scratch areas.

- If maintenance of the disc drive requires operation with the card cage cover and/or head contamination shields removed:

  a. Do not unplug or connect any heads while the heads are over the discs.

  b. Do not touch read/write PCA-A10 or the head connectors while the heads are over the discs.

  c. Do not operate the disc drive with the two captive screws at the top of read/write PCA-A10 detached from the adjacent read/write PCA shield.

  d. Do not attempt to remove or install the card cage cover with power applied to the disc drive.

- To avoid accidental erasure of data while performing manual head alignment:

  a. Take precautions to minimize the possibility of electrical discharge. Touch grounded metal on the disc drive before placing the head alignment tool near the carriage assembly.

  b. Do not touch read/write PCA-A10 with the head alignment tool. This could cause a ground path to the head assembly and erase data on the head alignment tracks.

  c. Ensure that the shaft of the head alignment tool has an insulating sheath.

3-3. SERVICE TOOLS AND TEST EQUIPMENT

The following paragraphs list and describe the tools and test equipment required to service the disc drive.

3-4. STANDARD TOOLS

Recommended standard tools and materials required for service are listed in table 3-1. Except where noted, equivalent tools may be substituted.

3-5. STANDARD TEST EQUIPMENT

The following items of standard test equipment are required for maintenance:

- HP 970A Digital Voltmeter, or equivalent battery-operated voltmeter.
- HP 180 Oscilloscope, or equivalent.

3-6. SPECIAL TOOLS

The special tools required for servicing the disc drive are listed in table 3-2.

3-7. PREVENTIVE MAINTENANCE

In a normal operating environment (data processing environment), preventive maintenance should be performed *once per year* on HP 7933 and HP 7935 Disc Drives. The yearly preventive maintenance includes the procedures outlined in paragraphs 3-8 through 3-15.

Preventive maintenance is drastically reduced since many conditions normally checked in a preventive maintenance schedule are self diagnosable by the disc drive. At power on, the disc drive automatically performs a complete series of self-test diagnostics. Also, during idle time, the disc drive cycles through a series of tests to ensure that it is operating at peak performance. These tests include operation of the microprocessor read only memory (ROM) and random access memory (RAM), and the disc memory access (DMA) RAM. Also checked are the disc drive fault log, the need for automatic head alignment, and inputs from the disc drive control panel. The background diagnostics are arranged in such a way that response to a channel request can occur in 140 microseconds or less.

The results of the self-test diagnostics are logged on two tracks called maintenance tracks. These results include a drive fault log, a run time data error log, an error rate test error log, and an address of spared tracks log. Full details of these logs are provided in section V of this manual. This means, for example, that if manual head alignment is required, the internal diagnostic will report the condition to the user who would in turn call a Hewlett-Packard Sales and Support Office for assistance.

Table 3-1. Standard Tools

Tool	HP Part No.
Bit, hex, 3/32-inch, 1/4-inch base	1535-2652
Tape, masking	0460-0030
Wrench, torque, 2 to 12 inch-pounds	1535-2653
Label, universal	7121-0923
Alcohol, isopropyl (filtered)*	8500-0559
Tape head cleaning solution (refill)*	8500-1251
Cotton swabs	8520-0023
Wrench, torque, 10 inch-pounds, preset	8710-1594
Bit, 1/4-inch drive, Pozidriv # 2	8710-0903
Wrench, torque, 30 to 150 inch-pounds	8710-1007
Bit, 1/4-inch drive, hex key	8710-1223
TORX® Driver Kit (includes the following items):	8710-1426
Bit, T6	8710-1424
Bit, T7	8710-1423
Bit, T8	8710-1422
Bit, T9	8710-1421
Bit, T10	8710-1418
Bit, T10, 3.5 in. long	8710-1465
Bit, T15	8710-1415
Bit, T20	8710-1416
Bit, T25	8710-1417
Bit, T27	8710-1420
Bit, T30	8710-1419
Handle, driver	8710-1413
Extension	8710-1425
Pouch	8710-1412
Mirror, inspection	8830-0005
Sleeve, cleaning, with handle*	9310-5074
Wipe, cleaning*	9310-4865
Adapter, 1/4-inch hex to 1/4-inch base	8710-1457
Tool, IC extractor	8710-1213
Kit, ground*	9300-0794
Sealant*	0470-0573
Lubricant, special*	6040-0652

*Do not substitute

WARNING

Isopropyl alcohol is a restricted article (flammable liquid). Transport in accordance with Department of Transportation Regulations, Title 49, parts 171 - 177 (Hazardous materials).

All products which utilize the tape head cleaning solution are shipped with a Material Safety Data Sheet. Follow all applicable safety precautions when using the tape head cleaning solution.

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Table 3-2. Special Tools

Tool	HP Part No.
Gauge, Pressure	0101-0374
Tape, External Exerciser	07908-16001
Extender, PCA	07930-60025
Tool, Head Spacer	07930-60154
Tool, Sensor Defeat	07930-60157
Tool, Control Panel Holder	07930-60161
Tool, Head Alignment Shield	07930-60198
Tool, Head Alignment	13354-20007
Tool, Head Initial Position	13354-20008
Tool, Head Installation	13354-20009

3-8. PRELIMINARY STEPS

WARNING

The disc drive does not contain operator-serviceable parts. To prevent electrical shock, refer all installation and maintenance activities to service-trained personnel.

CAUTION

- Do not turn the disc drive power on or off when the system bus is in an active state (Activity indicator illuminated).
- Do not connect or disconnect the HP-IB cable from the disc drive when the system bus is in an active state (Activity indicator illuminated).

Before performing the procedures described in paragraphs 3-8 through 3-15, perform the following preliminary steps:

CAUTION

Before proceeding with any preventive maintenance, perform a data back-up to protect against accidental data loss.

a. If the disc drive is in an operational state, set the LOAD/UNLOAD switch to the UNLOAD (out) position.

Note: If a BUSY message appears, wait until the system host releases the disc drive and again operate the LOAD/UNLOAD switch. If release is not obtained when the Activity indicator extinguishes, the system must be programmed to release the disc drive.

b. The disc drive will now begin a spin-down operation with the display indicating UNLOAD, SPIN DWN, and finally STOPPED.

c. Remove the shroud (refer to paragraph 6-3).

d. Remove the media module (refer to paragraph 6-8) and store it in a suitable location.

e. Set the ~ LINE switch to the 0/OFF position and disconnect the disc drive power cord from the ac power source.

f. Disconnect the HP-IB cable from the disc drive.

g. Remove the media module chamber (refer to paragraph 6-9).

h. Remove the head contamination shield (refer to paragraph 6-13).

i. Remove and discard the absolute filter (refer to paragraph 6-6).

j. Remove the front panel (refer to paragraph 6-4).

k. Remove and discard the prefilter (refer to paragraph 6-5).

3-9. DATA AND SERVO HEADS

Clean and inspect the heads as follows:

CAUTION

Do not allow the carriage assembly to move forward more than approximately one-half inch from its latched (retracted) position without having the head spacer tool, part no. 07930-60154, installed on the heads. Failure to observe this precaution will result in damage to the heads.

a. Manually release the carriage latch solenoid (8, figure 7-5) and carefully move the carriage assembly forward until the heads project approximately one-half inch beyond the cam towers (25, 25A).

b. Install the head spacer tool, part no. 07930-60154, on the heads.

c. Pull the carriage assembly outward the entire extent of its travel.

CAUTION

Never place an inspection mirror between the heads or allow the mirror to touch the heads. The flying characteristics of the head may be changed or the head damaged.

d. Using an inspection mirror, examine the heads for signs of abrasion (see figure 3-1).

Note: Some heads may have a gray "shaded" area. This is not necessarily a problem, since the flying characteristics of the head are not affected.

e. If any signs of abrasion are apparent, replace the head.

CAUTION

Use only the cleaning sleeves and filtered isopropyl alcohol specified in table 3-1. Use of any other materials may leave a residue that could cause damage to the disc drive.

f. Place a cleaning sleeve on the end of the handle (see figure 3-2).

g. Moisten the cleaning sleeve with filtered isopropyl alcohol.

CAUTION

Avoid applying excessive pressure to the gimbal area of the heads while cleaning. Excessive pressure may alter the factory-preset flying characteristics of the heads.

h. Clean each head by placing the prepared head cleaning tool between the surfaces, then gently wipe the head face. Use only sufficient pressure to thoroughly wet the head and remove the contamination.

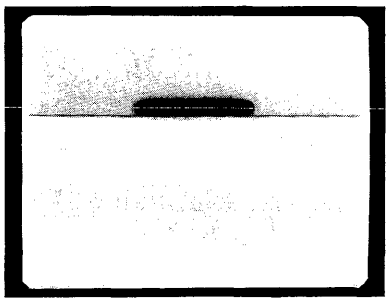
i. Replace the cleaning sleeve on the cleaning tool with a dry cleaning sleeve.

j. Carefully remove the remaining contamination from the head surface.

k. Using an inspection mirror, verify that all evidence of contamination has been removed. If the contamination cannot be removed, replace the head. (Refer to section VI for instructions.)

3-10. CARRIAGE RAILS AND BEARINGS

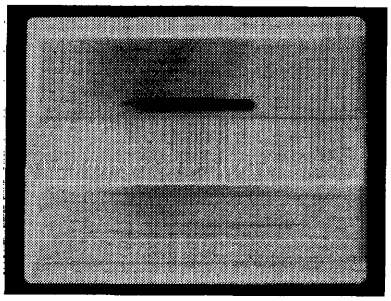
It is important that the carriage rails and bearings are clean in order to maintain the efficiency of the disc drive. To clean the carriage rails and bearings, proceed as follows:



TYPE OF CONTAMINATION:
NONE, IDEAL HEAD CONDITION.

CAUSE:
NEW HEAD OR MINIMAL OPERATION IN A CLEAN ENVIRONMENT.

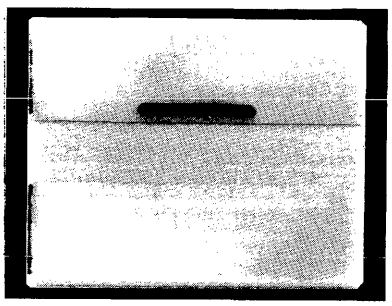
REMEDY:
NONE



TYPE OF CONTAMINATION:
GREY DISCOLORATION OF CERAMIC SLIDER.

CAUSE
FRICTION BETWEEN MEDIA AND HEAD, CAUSED BY CLOSE FLYING HEIGHT.

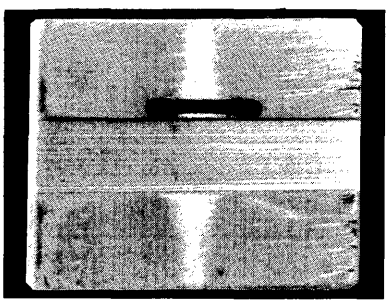
REMEDY:
REPLACEMENT OF HEAD, ONLY AS DETERMINED BY PREVENTIVE MAINTENANCE PROCEDURES.



TYPE OF CONTAMINATION:
OXIDE BUILD-UP ON TRAILING EDGE (DOWN HEAD SHOWN). TYPICAL OPERATING CONDITION.

CAUSE:
NEW MEDIA OR MANY HOURS OF OPERATION.

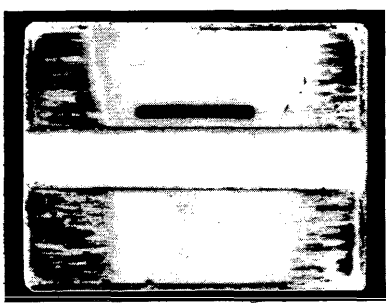
REMEDY:
CLEAN AS OUTLINED IN PARAGRAPH 3-10.



TYPE OF CONTAMINATION:
ABRASION AND PARTICULATE.

CAUSE:
MEDIA IS ABRASIVE OR EXCESSIVE MECHANICAL RUNOUT EXISTS.

REMEDY:
REPLACE DEFECTIVE HEAD. (REFER TO SECTION VI.)



TYPE OF CONTAMINATION:
ABRASION AND PARTICULATE.

CAUSE:
EXCESSIVE OPERATION ON ABRASIVE MEDIA. AIR FLOW RESTRICTED AND/OR CONTAMINANTS PRESENT IN AIR CIRCULATION.

REMEDY:
REPLACE DEFECTIVE HEAD. (REFER TO SECTION VI.)
REPLACE MEDIA.

Figure 3-1. Examples of Head Contamination

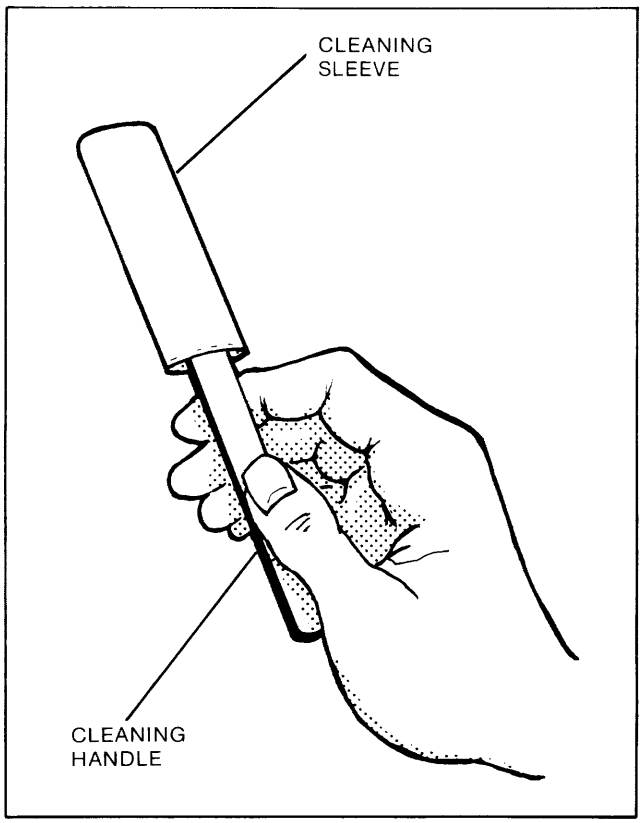


Figure 3-2. Prepared Head Cleaning Tool

CAUTION

When cleaning the carriage assembly bearings, do not allow alcohol to flow on the sides of the bearings. Alcohol will dissolve the lubricant in the bearings and result in premature bearing failure.

a. Moisten a cleaning sleeve with handle (as shown in figure 3-2 in filtered isopropyl alcohol (table 3-1).

b. Clean upper and lower rails.

c. Using a cotton swab (table 3-1), clean bearings and cam towers.

d. Using wipes (table 3-1), clean casting surfaces and rail clamps.

e. Repeat the rail and bearing cleaning procedure until carriage movement is smooth throughout its travel.

f. Proceed with lubrication procedure following.

3-11. BEARING/RAIL LUBRICATION

To lubricate the bearing/rail interface, proceed as follows (cleaning required first, see previous paragraph):

Note: A special lubricant, part no. 6040-0652, has been developed for the actuator linear bearing system to increase its usable life. The lubricant comes in an applicator which dispenses a precise volume. Correct operation of the disc drive requires that the exact volume of lubricant be used and that this procedure be followed exactly.

a. Remove the shipping cap from the lubricant bottle and install the applicator needle cap.

b. Remove the cap from the applicator needle and carefully clean any excess lubricant from the needle and body.

CAUTION

It is imperative that the entire volume of the drop of oil reside in the arch of the bearing where it will be in direct contact with the rail.

c. Locate the carriage near track 200 as shown by the track indicator on the upper rail guide beam. Apply a single, full drop of lubricant to the center arch portion of the lower rear bearing.

d. Move the carriage to its outermost position against the crash stops (track 1337 on the track indicator).

e. Cover the heads with a cleaning wipe. This protects the heads from possible stray oil drops.

f. Apply a single, full drop of lubricant to each of the arch portions of the upper bearing and lower front bearings. (See figure 3-3.)

g. Remove the cleaning wipe from the heads.

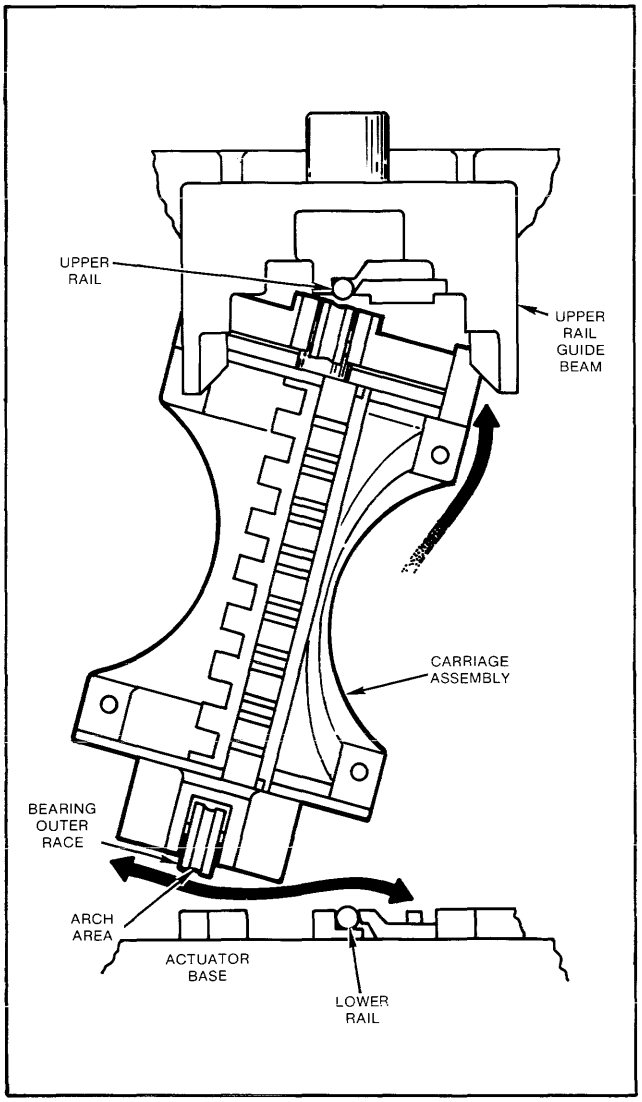
h. Manually move the carriage forward and back at least 10 times to distribute the lubricant on the rail surfaces.

i. Move the carriage assembly to within one-half inch of its latched (retracted) position.

j. Remove the head spacer tool.

k. Return the carriage assembly to its latched position.

l. Run 10 passes of random RO ERT and 50 auto head alignments as follows:



7933-326A

Figure 3-3. Carriage Assembly Lubrication

```
ENTER                    STEP 0=
88                       LOOP
ENTER,10                 NUM=10
ENTER(2x)                STEP 1=
94                       RNRD ERT
ENTER                    STEP 3=
RUN                      RNRD ERT
(wait)                   LOOP

ENTER,CLEAR,50           NUM=50
ENTER(2x),CLEAR          STEP 1=
68                       HD ALIGN
ENTER(2x),0              HD=0
ENTER,RUN                (0 +/- nnn)
Rv (50x)                 LOOP
```

m. Any DERR 70 or 76 will abort the program, in which case the carriage and rails must be replaced.

3-12. SPINDLE GROUND

Inspect the spindle ground contact as follows:

a. Remove the three T15 screws (1, figure 7-3) which secure the bottom cover (2) to the motor-spindle assembly.

b. Examine the graphite button at the bottom of the motor. If the graphite button is worn flat such that the flattened area is more than 5/16-inch (8 mm) in diameter, the ground button assembly *must* be replaced.

c. To install a new or old ground button assembly, place one drop of sealant, part no. 0470-0573, on opposite mating surfaces of the ground button (see figure 6-6A). Do not put any sealant on the ground button threads.

CAUTION

Use extreme care not to touch the top, outermost machined surface of the spindle-motor assembly.

d. Without touching the top, outermost machined surface of the spindle-motor assembly, hold the spindle nose tightly with one hand. With the other hand, hand tighten the ground button into the spindle-motor shaft.

e. While continuing to hold the spindle nose by hand, tighten the ground button with an adjustable wrench until the spindle nose cannot be prevented from turning in your hand.

f. Use a cleaning wipe to clean excess sealant from the ground button.

CAUTION

Ensure that the ground strap (60, figure 7-1) is installed beneath one of the T15 screws which secure the bottom cover. Failure to do this may result in loss of data or damage to the disc drive.

g. Install the ground strap and the bottom cover using the three T15 screws removed in step d. Tighten the screws to 12 inch-pounds.

h. Install the media module chamber. (Refer to paragraph 6-9.)

3-13. MEDIA MODULE CHAMBER AND MOTOR-SPINDLE ASSEMBLY

To clean the media module chamber and the motor-spindle assembly, proceed as follows:

WARNING

All products which utilize the tape head cleaning solution are shipped with a Material Safety Data Sheet. Follow all applicable safety precautions when using the tape head cleaning solution.

CAUTION

Do not touch the spindle hub outermost machined surface with anything except the cleaning wipe moistened with tape head cleaning solution. Fingerprints may cause contamination.

a. Using two hands, pull upward on the inner diameter of the magnetic ring (3, figure 7-3), and remove the ring from the spindle assembly. The ring is held in place by its own magnetism.

b. Using the adhesive side of transparent adhesive tape, remove all magnetic particles from the magnetic ring.

c. Following the removal of all particles, clean the magnetic ring with a cleaning wipe, part no. 9310-4865, moistened with tape head cleaning solution, part no. 8500-1251.

d. Install the magnetic ring by placing one edge of the ring into the magnetic cup on the spindle assembly, then lowering the ring into the cup.

e. Using a cleaning wipe moistened with tape head cleaning solution, carefully wipe clean the interior of the media module chamber, the inside of the top door, and the top of the motor-spindle assembly; especially the spindle nose and the top smooth surfaces of the spindle motor and magnetic ring.

f. Keep the top door closed until a media module is installed in the disc drive.

3-14. MEDIA MODULE

Media modules must be cleaned to remove buildups of contamination which could cause data errors, damage to the media module, or damage to the disc drive. Clean the media modules as follows:

WARNING

All products which utilize the tape head cleaning solution are shipped with a Material Safety Data Sheet. Follow all applicable safety precautions when using the tape head cleaning solution.

a. Use a cleaning wipe, part no. 9310-4865, moistened with tape head cleaning solution, part no. 8500-1251, and wipe clean the outer edge of the flat coupling surface located beneath the removable cover. Be careful not to leave any particles on this surface.

b. Clean the side and bottom surfaces of the media module.

c. Clean the media module being used in the disc drive, and all media modules in storage.

d. Install a new absolute filter (refer to paragraph 6-6).

e. Install a new prefilter (refer to paragraph 6-5).

f. Install the front panel (refer to paragraph 6-4).

3-15. HEAD ALIGNMENT

To check head alignment, proceed as follows:

CAUTION

- Do not turn the disc drive power on or off when the system bus is in an active state (Activity indicator illuminated).

- Do not connect or disconnect the HP-IB cable from the disc drive when the system bus is in an active state (Activity indicator illuminated).

a. Connect the HP-IB cable to the disc drive.

b. Connect the disc drive power cord to the ac power source.

c. Set the ~ LINE switch to the 1/ON position.

Note: Disc drive power must be on at least one-half hour before performing the preventive maintenance procedures.

d. Install the media module, if not previously installed. (Refer to paragraph 6-8.)

e. Set the LOAD/UNLOAD switch to LOAD (in) and allow about five minutes for the disc drive internal diagnostics to complete, as indicated by the DRIVE * display message.

f. Perform the radial head alignment on all heads. To do this, key in the following program:

Keystroke	Display	Remarks
9	LOOP	
8	CLEAR	Clears the diagnostic program.
ENTER	STEP0=	
6	STEP0=6	
8	HD ALIGN	Performs the radial head alignment routine.
ENTER	HEAD=	
RUN	0 YY	YY = head offset count for each head (0 through 12).
Rv	1 YY	
Rv	2 YY	
:		
Rv	12 YY	

g. Record the head offset count for each head (the program will continuously roll through the head/offset counts as the Rv (Roll) key is repeatedly pressed).

h. If the offset count for any head is outside the range ±40 counts, alignment for that head is required (refer to section IV for alignment instructions). If a DERR 60 message is displayed, all heads may require alignment, the servo head may require alignment, or the head may be defective.

i. Following successful completion of the head alignment check, install the head contamination shield (refer to paragraph 6-13) and the shroud (refer to paragraph 6-3).

3-16. ABSOLUTE FILTER

Check air pressure in the absolute filter as follows:

a. Connect the air pressure measuring gauge, part no. 0101-0374, to the pressure tap on top of the absolute filter.

Note: Some early models may not have the pressure tap installed. These models can be upgraded by replacing filter cover, part no. 07930-60179, with filter cover update kit, part no. 07930-60242.

b. The gauge should indicate a pressure of at least 0.4 inch of water. If not, replace the absolute filter. (Refer to section VI for instructions.)

c. Replace the absolute filter and prefilter.

Note: The absolute filter must be replaced at least yearly, regardless of pressure level, since the filter can become contaminated by fungus growths. Also, a dusty environment can require more frequent replacement of either filter. Therefore, measuring the pressure is necessary to determine the extent of "filter plugging" and to develop a PM interval that ensures the pressure never dips below 0.4 inch of water.

ALIGNMENT AND ADJUSTMENT

SECTION IV

4-1. INTRODUCTION

WARNING

The disc drive does not contain operator-serviceable parts. To prevent electrical shock, refer all installation and maintenance activities to service-trained personnel.

CAUTION

- Precautions must be taken during maintenance of the disc drive to avoid accidental erasure of data. Normal writes initiated from the host CPU or the disc drive control panel (diagnostic commands) can overwrite data. Such writes must be restricted to prescripted scratch areas.

- If maintenance of the disc drive requires operation with the card cage cover and/or head contamination shields removed:

  a. Do not unplug or connect any heads while the heads are over the discs.

  b. Do not touch read/write PCA-A10 or the head connectors while the heads are over the discs.

  c. Do not operate the disc drive with the two captive screws at the top of read/write PCA-A10 detached from the adjacent read/write PCA shield.

  d. Do not attempt to remove or install the card cage cover with power applied to the disc drive.

- To avoid accidental erasure of data while performing manual head alignment:

  a. Take precautions to minimize the possibility of electrical discharge. Touch grounded metal on the disc drive before placing the head alignment tool near the carriage assembly.

  b. Do not touch read/write PCA-A10 with the head alignment tool. This could cause a ground path to the head assembly and erase data on the head alignment tracks.

  c. Ensure that the shaft of the head alignment tool has an insulating sheath.

This section contains step-by-step alignment and adjustment procedures for the disc drive. These procedures are to be performed only after a repair has been made or when specified parameters are out of tolerance. Do not make any unnnecessary adjustments to the disc drive.

Note: TORX® hardware is used in the assembly of the disc drive. This hardware requires the use of special drivers (refer to table 3-1). In this manual, any reference to this type of hardware will be accompanied by the appropriate driver size (for example, T15).

4-2. POWER SUPPLY ADJUSTMENTS

Power supply voltages should be checked when the self-test diagnostics indicate a power supply failure or following replacement of regulator PCA-A1, dc power PCA-A13, spindle driver PCA-A12, transformer T1, or capacitors C1, C2, C170, C230, or C270 in the power module.

Power supply voltages are measured at test points on regulator PCA-A1 and at connector W4P2 on actuator driver PCA-A2. Only the +5, +12, and -12 Vdc outputs are adjustable. To check and adjust the power supply voltages, proceed as follows:

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WARNING

The following tests and adjustments are performed with primary power supplied to the disc drive and its protective covers removed. Such maintenance should be performed by service-trained personnel who are aware of the hazards involved (for example, electrical shock and fire).

CAUTION

Do not turn the disc drive power on or off when the system bus is in an active state.

a. Set the disc drive LOAD/UNLOAD switch to the UNLOAD (out) position and the ~ LINE switch to 0/OFF.

b. Disconnect the disc drive power cord from the ac power source.

c. Remove the disc drive shroud (refer to paragraph 6-3) and the card cage cover (refer to paragraph 6-12).

d. Reconnect cables W6, W5, and the cable from HP-IB PCA-A7 to PCA's A2, A4, and A6, respectively, in the card cage.

e. Connect the disc drive power cord to the ac power source.

f. Set the ~ LINE switch to 1/ON and the LOAD/UNLOAD switch to LOAD (in).

g. Connect a digital voltmeter between the +5V and GND test points on regulator PCA-A1 in the card cage. (See figure 4-1.) Check that the voltage is +5 Vdc, ±50 millivolts. If necessary, adjust potentiometer R185 for the correct reading.

h. Similarly check, and, if necessary, adjust the +12 Vdc and -12 Vdc outputs as detailed in figure 4-1.

i. Using a digital voltmeter, check that the level of the +36 Vdc and -36 Vdc supplies connected to actuator driver PCA-A2 via connector W4P2 are within specification. (See figure 4-1.)

Note: Do not disconnect W4P2 from J1 on PCA-A2. Use a probe to measure the voltage at the point where the wires enter the connector. There are no adjustments for the +36 Vdc and -36 Vdc supplies.

j. Set the LOAD/UNLOAD switch to UNLOAD (out) and the ~ LINE switch to 0/OFF.

k. Disconnect the disc drive power cord from the ac power source.

l. Replace the disc drive card cage cover (refer to paragraph 6-12) and the shroud (refer to paragraph 6-3).

4-3. SEEK DECELERATION

The seek deceleration adjustment should be performed following replacement of the velocity transducer, velocity transducer shaft, actuator driver PCA-A2, or servo PCA-A3. To perform this adjustment, proceed as follows:

WARNING

The following adjustment is performed with primary power supplied to the disc drive and its protective covers removed. Such maintenance should be performed by service-trained personnel who are aware of the hazards involved (for example, electrical shock and fire).

CAUTION

Do not turn the disc drive power on or off when the system bus is in an active state.

a. Set the disc drive LOAD/UNLOAD switch to the UNLOAD (out) position and the ~ LINE switch to 0/OFF.

b. Disconnect the disc drive power cord from the ac power source.

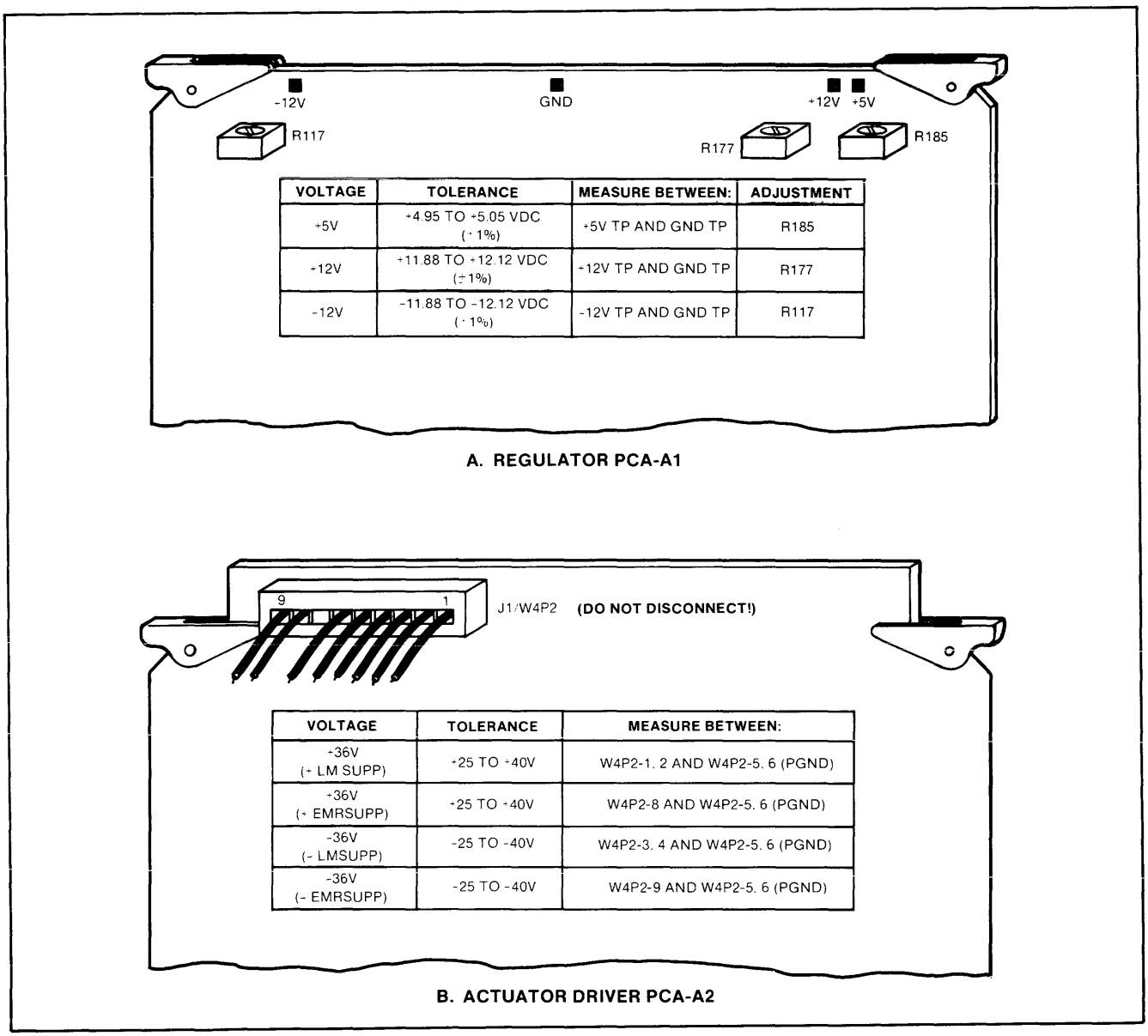
c. Remove the disc drive shroud (refer to paragraph 6-3) and the card cage cover (refer to paragraph 6-12).

d. Reconnect cables W6, W5, and the cable from HP-IB PCA-A17 to PCA's A2, A4, and A6, respectively, in the card cage.

e. Connect the disc drive power cord to the ac power source.

f. Set the ~ LINE switch to 1/ON and the LOAD/UNLOAD switch to LOAD (in).

g. When a DRIVE * message appears, key in the following program to perform the adjust seek deceleration routine:



VOLTAGE	TOLERANCE	MEASURE BETWEEN:	ADJUSTMENT
+5V	+4.95 TO +5.05 VDC (±1%)	+5V TP AND GND TP	R185
+12V	+11.88 TO +12.12 VDC (±1%)	+12V TP AND GND TP	R177
-12V	-11.88 TO -12.12 VDC (±1%)	-12V TP AND GND TP	R117

A. REGULATOR PCA-A1

VOLTAGE	TOLERANCE	MEASURE BETWEEN:
+36V (+ LM SUPP)	+25 TO +40V	W4P2-1, 2 AND W4P2-5, 6 (PGND)
+36V (+ EMRSUPP)	+25 TO +40V	W4P2-8 AND W4P2-5, 6 (PGND)
-36V (- LMSUPP)	-25 TO -40V	W4P2-3, 4 AND W4P2-5, 6 (PGND)
-36V (- EMRSUPP)	-25 TO -40V	W4P2-9 AND W4P2-5, 6 (PGND)

B. ACTUATOR DRIVER PCA-A2

Figure 4-1. Voltage Test Points and Adjustments

Keystroke	Display	Remarks
ENTER	STEP0=	Obtains diagnostic program control.
8	STEP0=8	
8	LOOP	
ENTER	NUM=	
ENTER	STEP1=	
6	STEP1=6	
7	ADJ DECL	Causes the disc drive to enter the adjust deceleration routine.
ENTER	STEP2=	
RUN	FNN YNN	F = forward deceleration value Y = reverse deceleration value

h. The disc drive will now seek alternately from physical cylinder 100 to physical cylinder 1300 with the display indicating deceleration timing.

i. Adjust potentiometer R132 on servo PCA-A3 until the display indicates 38 ±4. (See figure 4-2 for the location of R132.)

j. Clear the diagnostic program and then program it to check seek and verify times between cylinder 0 and the last physical cylinder as follows. Check that the seek time is 39.5 milliseconds or less and the verify time is 3.5 milliseconds or less.

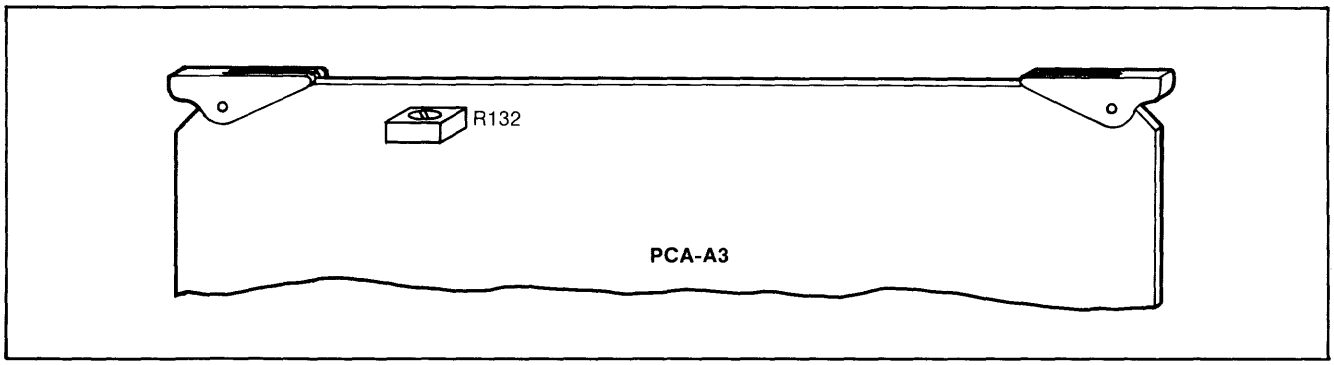


Figure 4-2. Seek Deceleration Adjustment Control

Keystroke	Display	Remarks
CLEAR	LOOP	Clears the diagnostic program.
9	LOOP 9	
8	CLEAR	
ENTER	STEP0=	
6	STEP0=6	
1	SEEK	Causes the disc drive to enter the seek routine.
ENTER	CYL=	
0	CYL=0	
ENTER	HEAD=	
ENTER	SECT=	
ENTER	STEP1=	
8	STEP1=8	
8	LOOP	Loop through the entire program.
ENTER	NUM=	
ENTER	STEP2=	
6	STEP2=6	
6	VFY TIME	Causes the disc drive to seek to the cylinder specified.
ENTER	INC=	
1	INC=1	
3	INC=13	
3	INC=133	
8	INC=1338	
ENTER	DIR=	
ENTER	STEP3=	
9	STEP3=9	
9	SK DELAY	Allows a new seek delay time to be entered.
ENTER	DLY=100	
CLEAR	DLY=	
5	DLY=5	
0	DLY=50	
0	DLY=500	
ENTER	STEP4=	
RUN	:	
	55.5 V.V	s = seek time v = verify time

k. Change command 66 for a cylinder increment of 1. Check that the single cylinder seek time is 2.5 milliseconds or less and the verify time is 3.5 milliseconds or less.

Keystroke	Display	Remarks
CLEAR	SEEK	
EDIT	STEP=	
2	STEP=2	Changes the cylinder seek address.
ENTER	VFY TIME	
ENTER	INC=1338	
CLEAR	INC=	
1	INC=1	Cylinder seek address increment is 1.
ENTER	DIR=	
ENTER	STEP3=	
RUN	5.5 V.V	s = seek time v = verify time

l. Set the LOAD/UNLOAD switch to UNLOAD (out) and the ~ LINE switch to 0/OFF.

m. Disconnect the disc drive power cord from the ac power source.

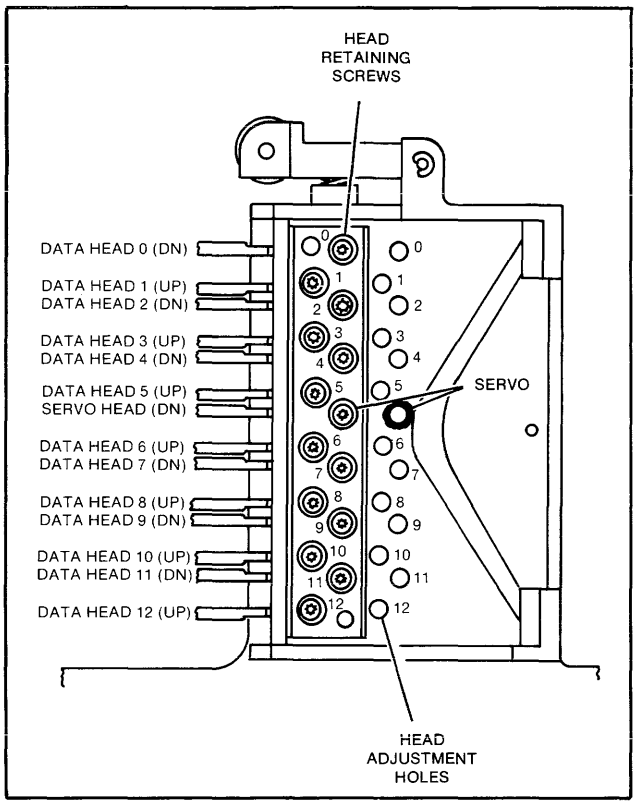
n. Replace the disc drive card cage cover (refer to paragraph 6-12) and the shroud (refer to paragraph 6-3).

4-4. HEAD ALIGNMENT

The following head alignment procedures include instructions for servo head alignment and data head alignment. The locations of the retaining screws and the adjustment holes for the servo head and the data heads are shown in figure 4-3. To prepare the disc drive for head alignment, proceed as follows:

WARNING

The following adjustment is performed with primary power supplied to the disc drive and its protective covers removed. Such maintenance should be performed by service-trained personnel who are aware of the hazards involved (for example, electrical shock and fire).



7933-352A

Figure 4-3. Head Retaining Screw and Adjustment Hole Locations

a. Disconnect the disc drive power cord from the ac power source.

CAUTION

Ensure that the discs have completely stopped spinning before removing the head contamination shield. Damage to the disc drive may result if this precaution is not followed.

b. Remove the disc drive shroud (refer to paragraph 6-3) and the right-hand section of the head contamination shield (refer to paragraph 6-13).

c. Remove the card cage cover (refer to paragraph 6-12).

d. Connect cable W6 (26, figure 7-1) to actuator driver PCA-A2 and cable W5 (10) to microprocessor PCA-A4 in the card cage.

e. Push the remaining slack in cable W5 into card cage slot number 7. This is necessary to avoid short circuits during head alignment.

f. Loosen the two T10 screws (18, figure 7-2) which secure the latch shield (8, figure 7-1) to the media module chamber and remove the latch shield.

Note: Steps f through k need only be performed for convenience in observing the control panel display during manual head alignment.

g. Unplug the three cables from connectors J3, J4, and J5 on the left-hand side of the control panel assembly.

h. Loosen the two captive screws securing ribbon cable W5 to the RF shield assembly.

i. Push on the control panel assembly from behind until it releases from the two spring retainers on the media module chamber.

j. Using the control panel holder, part no. 07930-60161, hang the control panel assembly on the right-hand side of the enclosure.

k. Attach the sensor defeat tool, part no. 07930-60157, to connectors J3, J4, and J5 on the left-hand side of the control panel assembly.

l. Check that a media module is installed in the disc drive.

m. Connect the disc drive power cord to the ac power source and set the ~ LINE switch to 1/ON.

n. Set the LOAD/UNLOAD switch to LOAD (in) and allow about five minutes for the normal power-on sequence.

o. When a DRIVE * message appears, press the following keys on the diagnostic keyboard to obtain diagnostic program control and perform the radial head alignment:

Keystroke	Display	Remarks
ENTER	STEP0=	Obtains diagnostic program control.
6	STEP0=6	
8	HD ALIGN	Performs the radial head alignment routine.
ENTER	HEAD=	
RUN	0 YY	YY = head offset value

CAUTION

When installing the emergency retract (ER) disable jumper between test points ERDIS and ER -36, ensure that no other test points are contacted by the jumper wire. Damage to actuator driver PCA-A2 will result.

If, while this jumper is installed, a RETRACT message appears on the alphanumeric display, a power loss

occurs, or the spindle drive motor begins to slow down, manually pull the heads off the disc IMMEDIATELY. Some resistance will be felt when the carriage contacts the cam towers. The carriage must be firmly latched in its unloaded position. Failure to do this will result in damage to the discs and heads.

p. Install a jumper wire between test points ERDIS and ER -36 (see figure 4-4) on actuator driver PCA-A2. This disables the emergency retract circuitry.

4-5. SERVO HEAD ALIGNMENT

Servo head alignment should be performed when the servo head is replaced or when all of the data heads have been replaced. At installation, initial alignment of the servo head is achieved when it is positioned with head initial position tool, part no. 13354-20008. (Refer to section VI.) Following installation of the servo head, the alignment of the data heads should be checked as described in paragraph 4-6. If the data heads can be aligned, the servo head is correctly positioned. In the event that all of the data heads cannot be aligned, the servo head should be adjusted as follows.

a. Perform the head alignment preparation procedures outlined in paragraph 4-4.

CAUTION

Before tightening any data or servo head retaining screw, the heads must be unloaded, using the Airpurge routine, to prevent damage to the heads or the media.

b. Unload the heads using the Airpurge routine (ENTER, 9, 7, ENTER).

c. Check that the retaining screw for the servo head is tightened to 3 inch-pounds.

d. Load the heads over the discs by re-entering the head alignment routine (ENTER, 6, 8, ENTER), then select any data head which previously displayed a DERR 61 message.

CAUTION

To avoid accidental erasure of data, the following precautions must be observed when performing manual head alignment:

- Take precautions to minimize the likelihood of electrical discharge. Touch grounded metal on the disc drive before placing the head alignment tool near the carriage assembly.
- Do not touch read/write PCA-A10 with the tool. This could cause a ground path to the head assembly and erase data or alignment tracks.
- Do not touch read/write PCA-A10 or the head connectors when the heads are over the discs.
- Ensure that the shaft of the head alignment tool has an insulating sheath.

e. Insert head alignment tool, part no. 13354-20007, in the servo head adjustment hole (marked with indelible marker on some disc drives) and rotate the tool until the DERR 61 message changes to a displacement reading. Remove the head alignment tool.

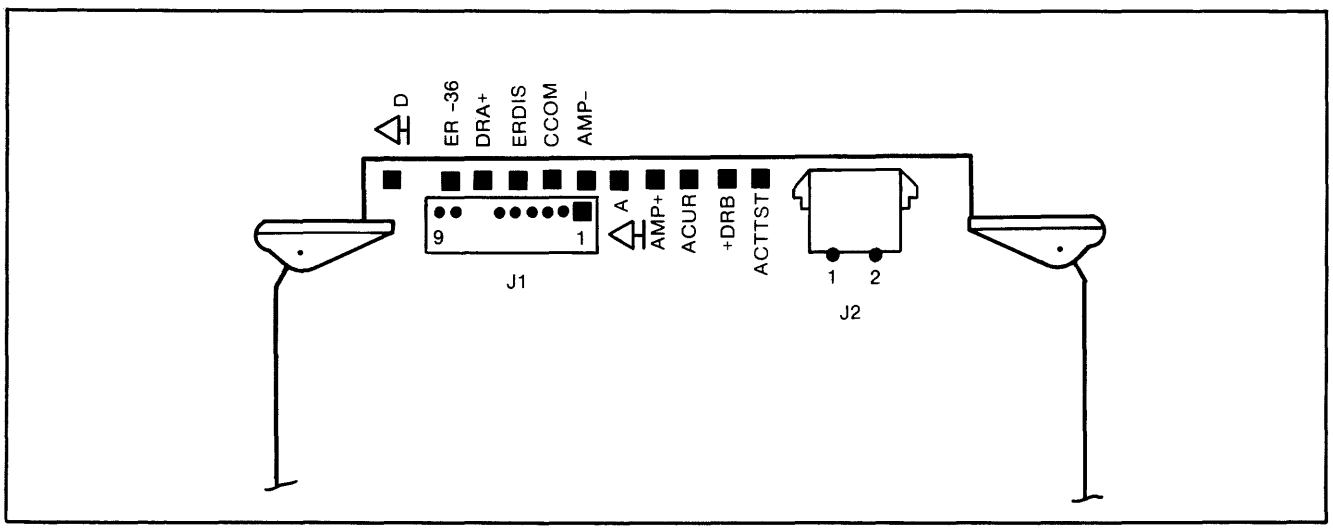


Figure 4-4. Actuator Driver PCA-A2, Test Point Locations

f. Operate the R↓(Roll) key and check that the display indicates a displacement reading for the remainder of the data heads. (This may require some rough adjustment of the data heads.) The reading will appear as a head number (left side) and displacement reading (right side).

CAUTION

Before tightening any data or servo head retaining screw, the heads must be unloaded, using the Airpurge routine, to prevent damage to the heads or the media.

g. Unload the heads using the Airpurge routine (ENTER, 9, 7, ENTER).

h. Tighten the servo head retaining screw to 8 inch-pounds.

i. Align the data heads as described in paragraph 4-6.

4-6. DATA HEAD ALIGNMENT

Data head alignment should be performed: when a data head is replaced, if a head offset value is outside the range ±40 counts, or when the disc drive self-test diagnostic indicates that a data head is out of alignment. A check of data head alignment may also be required when the servo head is replaced. To check data head alignment, proceed as follows:

Note: Installation of the head alignment shield, part no. 07930-60198, is no longer required.

a. Perform the head alignment preparation procedure as outlined in paragraph 4-4.

CAUTION

Before tightening any data or servo head retaining screw, the heads must be unloaded, using the Airpurge routine, to prevent damage to the heads or the media.

b. Unload the heads using the Airpurge routine (ENTER, 9, 7, ENTER).

c. Check that the retaining screw for the head being aligned is tightened to 3 inch-pounds.

d. Load the heads over the discs by re-entering the head alignment routine (ENTER, 6, 8, ENTER), then select the data head to be aligned.

CAUTION

To avoid accidental erasure of data, the following precautions must be observed when performing manual head alignment:

- Take precautions to minimize the likelihood of electrical discharge. Touch grounded metal on the disc drive before placing the head alignment tool near the carriage assembly.
- Do not touch read/write PCA-A10 with the tool. This could cause a ground path to the head assembly and erase data or alignment tracks.
- Do not touch read/write PCA-A10 or the head connectors when the heads are over the discs.
- Ensure that the shaft of the head alignment tool has an insulating sheath.

e. Insert head alignment tool, part no. 13354-20007, in the appropriate head adjustment hole and rotate the tool until the display indicates zero, ±4 counts.

Note: Check that when the tool is rotated around the zero setting, the reading changes from a positive value to a negative value or vice versa. If this does not occur, rotate the tool until a zero setting is found that satisfies this requirement. If the head is defective and cannot be aligned, the display will show a DERR 60 message. However, if all the heads are being aligned, check the alignment of other heads before assuming that one is defective. If one or more of the data heads give a DERR 60 message, it may be necessary to adjust the servo head. Refer to paragraph 4-5 for details.

CAUTION

Before tightening any data or servo head retaining screw, the heads must be unloaded, using the Airpurge routine, to prevent damage to the heads or the media.

f. Unload the heads using the Airpurge routine (ENTER, 9, 7, ENTER).

g. Tighten the data head retaining screw to 8 inch-pounds.

h. Load the heads over the discs by re-entering the head alignment routine (ENTER, 6, 8, ENTER, RUN).

CAUTION

Before aligning any head, ensure that the head retaining screw on the head to be adjusted is tightened to only 5 inch-pounds. Damage to the carriage assembly, the head assembly, or the screw could result.

i. Insert head alignment tool, part no. 13354-20007, sequentially in each head adjustment hole and rotate the tool until the display indicates zero, ±4 counts for each head. Use the R↓ (Roll) key to display each head offset value.

j. Remove the emergency retract disable jumper wire.

WARNING

Be sure to remove the head alignment tool from the disc drive before exiting from the radial head alignment operation. This will cause the disc drive to seek to track 0 and perform an automatic head alignment. Failure to remove the tool may result in injury to the operator and damage to the disc drive.

k. Key in the following program to perform random seeks as indicated.

Keystroke	Display	Remarks
ENTER	HD ALIGN	Exit radial head alignment operation.
8	D ALIGN8	
8	LOOP	
ENTER	NUM=	
1	NUM=1	
0	NUM=10	
0	NUM=100	
0	NUM=1000	Loop 1000 times.
ENTER	END=	
ENTER	STEP1=	
6	STEP1=6	
4	RND SEEK	Random Seek operation.
ENTER	STEP2=	
9	STEP2=9	
9	SK DELAY	Seek delay of 30 ms.
ENTER	DLY=100	
CLEAR	DLY=	
3	DLY=3	
0	DLY=30	
ENTER	STEP2=	
RUN	CYL xx	Wait until finished (about 1 minute).
	LOOP	
9	LOOP 9	
8	CLEAR	
ENTER	STEP0=	
6	STEP0=6	
8	HD ALIGN	Head Alignment routine.
ENTER	HEAD=	
RUN	0 xx	

CAUTION

When installing the emergency retract (ER) disable jumper between test points ERDIS and ER -36, ensure that no other test points are contacted by the jumper wire. Damage to actuator driver PCA-A2 will result.

If, while this jumper is installed, a RETRACT message appears on the alphanumeric display, a power loss occurs, or the spindle drive motor begins to slow down, manually pull the heads off the disc IMMEDIATELY. Some resistance will be felt when the carriage contacts the cam towers. The carriage must be firmly latched in its unloaded position. Failure to do this will result in damage to the discs and heads.

l. Check each head offset value to ensure that the heads are within the range ±12 counts. If not, retighten the head(s) to 5 inch-pounds, reconnect the emergency retract disable jumper wire and repeat steps e, f and g. (Same CAUTIONS apply.)

m. Select the Airpurge command as indicated:

Keystroke	Display	Remarks
CLEAR	HD ALIGN	
CLEAR	STEP0=	
9	STEP0=9	
7	AIRPURGE	(or PURGE)
ENTER	AIRPURGE	(or PURGE)

n. While the airpurge is being performed, install the head contamination shield

o. Cycle the LOAD/UNLOAD switch to UNLOAD (out), then LOAD (in), and allow about one minute for the normal sequence.

p. When a DRIVE * message appears, press the following keys on the diagnostic keyboard to obtain diagnostic program control and perform the radial head alignment:

Keystroke	Display	Remarks
ENTER	STEPO=	Obtains diagnostic program control.
6	STEPO=6	
8	HD ALIGN	Performs the radial head alignment routine.
ENTER	HEAD=	
RUN	0 YY	YY = head offset value

q. Check each head offset value for a range of ±12 counts. If the head offset value for each head is not within this range, remove the head contamination shield, install the emergency retract disable jumper wire, and repeat steps d through n.

CAUTION

After performing the head alignment procedure, the emergency retract disable jumper wire must be removed to enable the emergency retract circuitry. Failure to do this will result in damage to the disc drive.

r. Following successful completion of the head alignment procedure, remove power from the disc drive; then replace the card cage cover and the shroud.

4-7. DATA SURFACE VERIFICATION TEST

The data surface verification test must be performed each time the media module is installed in an HP 7933 Disc Drive, and at initial site installation of an HP 7935 Disc Drive. To perform the test, proceed as follows:

a. Set the LOAD/UNLOAD switch to the LOAD (in) position.

b. The disc drive will now begin an internal diagnostic routine. The normal sequence of display messages will be: TESTING , SPIN UP , AIRPURGE (or PURGE), TESTING , and DRIVE * . If the routine does not complete, the reason will be indicated by any one of the following messages: MOD DOOR , NOMODULE , TEST ERR , MEM FAIL , FAULT , FILTER * , or RESEAT .

Note: The Purge portion of the internal diagnostic routine will require approximately four minutes to complete.

c. If a TEST ERR , MEM FAIL , FAULT , FILTER * , or RESEAT message appears, a message in step b persists or any other message appears, refer to Section V, Service Information, for additional information.

d. Perform the data surface verification test described in table 4-1.

e. To interpret the results of the data surface verification test, add the total number of correctable (COR) errors on all heads. If more than 20 correctable errors or ANY uncorrectable errors are generated, a further diagnostic procedure is necessary before releasing the disc drive for on-line operation. This procedure is described in the next step.

Note: The following procedure requires the use of an external exerciser. Refer to the *External Exerciser Reference Manual,* part no. 5955-3462, for details.

f. Perform the sector sparing procedure described in table 4-2.

Note:

1. The previously described "off-line" data verification test consisted of two read-only error rate test passes which automatically filled the error rate test error log with valid failure information. The first step in the sector sparing procedure described in table 4-2 is to read the error rate test error log (ERT LOG) to verify the sector locations of any errors that occurred during the data verification test. If ANY uncorrectable errors or two or more correctable errors are logged for any sector, that sector should be spared (SPARE). Next, a Write Then Read Error Rate Test (WTR ERT) is executed and two more Read Only Error Rate Test (RO ERT) passes are performed to log any additional sectors that need to be spared. This action should be continued until there are no repeatable errors on any sector in the entire volume.

2. Media module rejection criteria for new media is as follows:

   The total number of spare tracks that are logged in the spare track table should be less than or equal to 28. For media that has been previously installed and checked for data integrity, the media module is

Table 4-1. Data Surface Verification Test

Keystroke	Display	Remarks
ENTER	[STEP0=]	
7	[STEP0=7]	Clears all logs, including the
7	[CLR LOGS]	error rate test error log.
ENTER	[STEP1=]	
RUN	[CLR LOGS]	
CLEAR	[STEP0=]	
6	[STEP0=6]	Causes the disc drive to seek
0	[RECAL]	to logical cylinder, head,
ENTER	[STEP1=]	and sector 0.
8	[STEP1=8]	
8	[LOOP]	
ENTER	[NUM=]	
2	[NUM=2]	
ENTER	[END=]	
2	[END=2]	
ENTER	[STEP2=]	
9	[STEP2=9]	Performs the read only error
0	[READ ERT]	rate test twice. The test area
ENTER	[AREA=]	is volume (all surfaces). The
4	[VOLUME]	test lasts approximately 16
ENTER	[STEP3=]	minutes. The Activity indicator
8	[STEP3=8]	is lit for the duration of the
4	[ERT LOG]	test.
ENTER	[HEAD=]	
ENTER	[STEP4=]	
RUN	[READ ERT]	Displays the information stored
R↓	[HEAD 0]	in the error rate test error
R↓	[2.43E 5]	log. The number "2.43E 5" is
R↓	[COR n]	the number of sectors
R↓	[UCOR n]	transferred, in scientific
R↓	[HEAD 1]	notation (243,000).
R↓	[2.43E 5]	
R↓	[COR n]	Note the number of correctable
R↓	[UCOR n]	(COR) and uncorrectable (UCOR)
.	.	errors recorded for each head.
.	.	
.	.	
R↓	[HEAD 12]	
R↓	[2.43E 5]	
R↓	[COR n]	
R↓	[UCOR n]	
R↓	[RECAL]	
END	[DRIVE *]	Returns the disc drive to CPU control.

to be considered good until there are no more spare tracks available. (This will be indicated by a drive error [DERR] 146 or 231.)

Program command 82, Display Spare Tracks, using the default head parameter (all heads), to verify the above conditions.

3. The number of correctable errors that are not repeatable (those that occur in only 1 or 2 read only passes) should not exceed seven errors on any one head. If this condition is not met, it is an indication that there is a performance problem in the read/write path and/or a head crash.

g. Check the head alignment as indicated in the following program. The display should indicate a head number and a head offset value (YY) of ±40 counts. If the count is outside this range, perform the head alignment procedure outlined in paragraph 4-4.

Keystroke	Display	Remarks
CLEAR	STEP0=	Resets the diagnostic program table.
9	STEP0=9	
8	CLEAR	
ENTER	STEP0=	
6	STEP0=6	
8	HD ALIGN	Perform the radial head alignment routine.
ENTER	HEAD=	
RUN	0 YY	YY = head offset value
R↓	1 YY	
R↓	2 YY	
.	.	
.	.	
.	.	
R↓	12 YY	
CLEAR	HD ALIGN	
END	DRIVE *	Returns control of the disc drive to the CPU.

Table 4-2. Sector Sparing Procedure

COMMAND	PARAMETERS	FUNCTION
1. ERT LOG	All heads.	Determines which sectors must be spared.
2. SPARE	Defective sector(s). Spare retaining data.	Spares any sector with ANY uncorrectable errors or more than one correctable error.
3. WRT ERT	Loop count = 1 Type = PT Area = Volume No offset Pattern Source = PT Output format = ADD	Writes a new pattern on all sectors and records any errors that occur when reading them.
4. RO ERT	Loop count = 2 Not Random Test Area = volume No offset Output Format = ADD	Reads two more volumes of data and logs any errors.
5. SPARE	Any sector that needs sparing. Spare retaining data.	Spare any sector that has developed ANY uncorrectable errors or more than one correctable error.
6. Repeat commands 4 and 5 until there are no repeatable errors on any sector in the entire volume.		

Note: This procedure requires the use of an external exerciser. Refer to the *External Exerciser Reference Manual*, part no. 5955-3462, for details.

SERVICE INFORMATION

SECTION V

WARNING

The disc drive does not contain operator-serviceable parts. To prevent electrical shock, refer all installation and maintenance activities to service-trained personnel.

5-1. INTRODUCTION

This section contains information useful for servicing and troubleshooting the disc drive. Included is a description of the disc drive self-test and internal diagnostic routines, troubleshooting hints, and details of the disc drive signal connections and power distribution. The information provided is for the isolation of malfunctions within the disc drive and not for equipment external to the disc drive.

5-2. SIGNAL CONNECTIONS

Signal connections for the disc drive assemblies are shown in the disc drive wiring diagram (figure 5-19). Motherboard signal connections are also listed in the Motherboard PCA-A11 Signal Distribution List (table 5-10). The numbers in parentheses following the PCA reference designations identify the functional block diagram locations of the PCA's.

5-3. POWER DISTRIBUTION

Power distribution information for the disc drive, with the exception of motherboard PCA-A11, is given in the disc drive wiring diagram (figure 5-19). Motherboard power distribution information is provided in the Motherboard PCA-A11 Power Distribution List (table 5-11).

5-4. SYSTEM FUNCTIONAL DIAGRAMS

Functional block diagrams for the disc drive circuitry are provided in section I of this manual. Included are diagrams for the microprocessor system, control panel system, spindle rotation system, head positioning system, read/write system, and power distribution system (figures 1-15 through 1-20, respectively). Each of the system functional diagrams is accompanied by a circuit description.

5-5. PCA LAYOUT

Figures 5-3 through 5-18 show the layout of fuses, test points, connections, and potentiometers on PCA's A1 through A4, A6, A8 through A14, and A17, A18, A20, and A21.

5-6. INTERNAL DIAGNOSTICS

The following paragraphs provide information on how a user can interact with the disc drive control panel to enter and interpret the disc drive internal diagnostic procedures. In the discussion, all display messages are enclosed in square brackets or outlined, for example [STEP0=] , so that an accurate representation of the display readout can be presented.

The control panel (see figure 5-1) on the disc drive contains a number of switches and indicators that provide an interface to the operations of the disc drive and its internal diagnostics. On the right, the control panel has two switches that permit the operator to load or unload a media module, or unlock the top door (on the HP 7935 only). Next to these controls is an eight-character alphanumeric display that shows the operating status of the drive. Normal messages on the display tell the operator that the disc drive is stopped, ready for normal operations, or that an error has occurred. To the right of the display is an activity indicator that signals when the disc drive is busy executing commands. On the left of the control panel is a keypad for use in accessing the internal diagnostics of the disc drive. The alphanumeric display shows the internal diagnostic program entries and results. The functions of the keys on the keypad are described in figure 5-1.

Under normal conditions, the disc drive receives commands from the system host. At this time the host commands have higher priority than those entered from the control panel keyboard. The disc drive must receive permission from the host to respond to instructions entered on the control panel keyboard. The status requests from the host will automatically update the display so the state of the disc drive can be easily determined at any time.

Release from the host control is requested when the ENTER, EDIT, or CLEAR key is pressed. Once the CPU releases the disc drive to the control panel keyboard, or if a timeout occurs on the release request, the diagnostic mode is entered. The automatic release to the diagnostic mode because of a time out can take up to two seconds. If the control panel display has either [FAULT] or [TEST ERR] when the user

enters a command key to request release, the status causing the fault or error will automatically be displayed.

In the diagnostic mode, the diagnostic keys give the commands to the internal controller. This allows testing the disc drive without the need of the host for all operations not requiring transfers to the host. In addition, the control panel display gives more information relating to drive problems in diagnostic mode than would be otherwise displayed.

The internal diagnostics can initiate any of the commands that the host can, but do not provide for displaying very much data at one time. Up to ten different steps, numbered 0 through 9, can be entered to make a diagnostic program. To indicate how many steps have been used, the step prompt includes a number indicating the current step number. The procedures that can be chosen for execution are listed in table 5-1 and discussed in detail in paragraphs 5-10 through 5-52.

The diagnostic keys normally operate on the contents of the internal program table. Keys are provided for creating and editing user defined programs for the purpose of diagnosing the disc drive. The EDIT key allows the modification of the step pointer to the program table. This means that the user can specify any step desired for modification or examination.

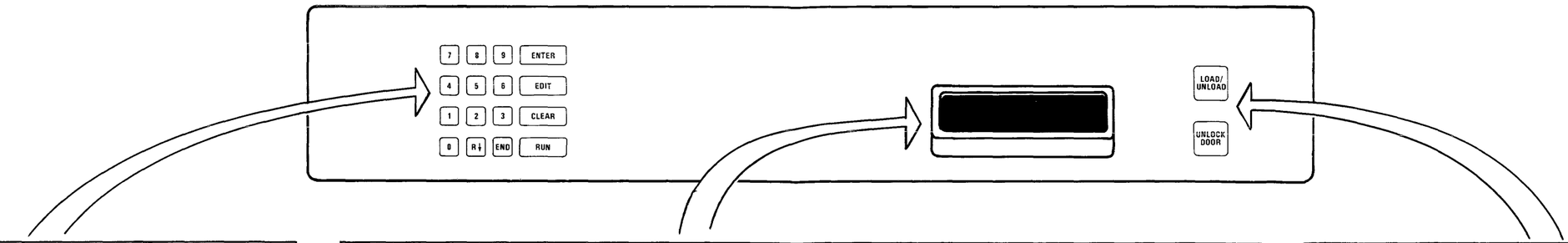
Background diagnostics are running during drive idle time. This includes the time waiting for a key to be pressed. Background diagnostics detect the need for automatic head alignment, update fault logs, and run certain short diagnostics.

There are several procedures that do not increment the step number. Instead, they are executed immediately. An example of this is the Seek Delay procedure. This feature allows the seek delay to be changed without changing the diagnostic program.

After the RUN key is pressed and the diagnostic program is executing, any command key, not numeric keys, will cause the program to abort at the end of the current step. If the procedure is displaying data, the R↓key is required to display the next data or get the next procedure. If another command key is entered instead of the R↓key, that procedure will terminate and process the command key entered. Pressing RUN again will cause the previously entered program to be executed again. If any execute immediate procedures are desired, they can be entered before pressing the RUN key since they do not change the program.

If an undefined procedure number is entered, ILL PROC will be displayed for about one second. If an error is made while entering parameters, ILL PARM will be displayed for about one second. The parameter prompt message will then be redisplayed.

All the error rate tests and diagnostics automatically log the error results in the appropriate drive error logs. The other commands will abort the diagnostic program if an error is encountered and the error number will be displayed. The error messages will remain until any command key is entered. This gives the user time to read the message before proceeding. Numeric keys will be ignored at this time.



DIAGNOSTIC KEY FUNCTIONS

CLEAR	Clears the data value in the destination area, either the program table or the step pointer, and reprompts for the desired data.
EDIT	Sets the destination area to be the step pointer. STEP= will be displayed to prompt for the desired program step value. If the step value is cleared, it will become the current step unless otherwise changed.
END	Returns control of the disc drive back to the system host. Any log entries that have not been written to the disc drive will be cleared. Status will also be cleared so previous operations will not affect the host.
ENTER	Writes the current data to the destination area, either the program table or the step pointer. It sets the destination of following data to be the program table. The parameter pointer will be incremented so that the next data can be displayed.
RUN	Causes a previously entered program to be executed.
R↓(ROLL)	Sets the destination of following data to be the program table. The parameter pointer will be incremented so that the next data will be displayed.
0 thru 9	Digit keys. Only valid if pressed before the ENTER or CLEAR keys. They will be ignored if pressed before the R↓(Roll), EDIT, RUN, or END keys; or the UNLOCK DOOR (7935 only) or LOAD/UNLOAD switches.

Notes:

1. The diagnostic keys operate in RPN format, that is, the numeric keys precede the command keys. There are three exceptions. The first exception is that the first key pressed before gaining control of the internal diagnostics is used to get release from the system host. Either the ENTER, EDIT, or CLEAR key can get release from the host. The second exception is the EDIT key. It is used to interrupt the programming mode temporarily and change the step pointer so that a different step can be examined. The third exception is that any command key pressed while a diagnostic program is executing will interrupt the program and control is passed to the programming mode.
2. The above key definitions simplify the internal diagnostic language because the action of any key is independent from any previous key entry.
3. The program table can only be changed by the ENTER or CLEAR keys. All other keys have no effect on the contents of the program table.
4. If the ENTER key is pressed when an equals (=) sign is displayed with no value following it, default or undefined data will be in the table just as if the CLEAR key was pressed.

DISPLAY MESSAGES

Activity indicator	Signals when the disc drive is busy executing commands.
Alphanumeric display	An eight-character display that provides messages for the operator, indicates that service is necessary, and shows internal diagnostic keyboard entries. Common messages are listed below:
AIRPURGE or PURGE	The disc drive is blowing air through the media module to remove any contamination. This is performed for two reasons: 1) the top door has been opened, or 2) the spindle has stopped after a power failure.
BUSY	The front panel controls are not available because the controller-in-charge is accessing the disc drive.
DERR *** †	The disc drive has an error corresponding to the number nnn listed in Table 5-8, Drive Error (DERR) Numbers.
DOOROPEN	The top door is open. Close the top door. (This message should occur only during servicing on 7933 Disc Drives.)
DRIVE *	The disc drive successfully passed all diagnostics and is ready for operation. (*A single numeral on the right is the primary port channel address. A secondary port channel address numeral will appear to the left of the single numeral if the disc drive is fitted with option 022, dual port.)
FAULT †	The disc drive has a drive fault.
FILTER * †	The disc drive is ready for operation but the prefilter and/or absolute filter requires changing. (*A single numeral on the right is the primary port channel address. A secondary port channel address numeral will appear to the left of the single numeral if the disc drive is fitted with option 022, dual port.)
HFR %*** †	The disc drive has a hardware fault corresponding to the octal number nnn (listed in Table 5-5, Hardware Fault Register (HFR) Numbers.
MEM FAIL	The controller memory failed.
MOD DOOR	The sliding door on the media module is not fully open. Reinstall the media module. (To be done by qualified service-trained personnel on 7933 Disc Drives.)
NOMODULE	A media module is not installed. Install the correct media module. (To be done by qualified service-trained personnel on 7933 Disc Drives.)
PART *** †	The fault isolation program has found a part defective, corresponding to part nnn listed in Table 5-4, Failed Part (PART) Numbers.
RESEAT	The media module did not seat correctly before a head load due to contamination on the coupling mechanism between the spindle and the media module. Remove and reinstall the media module. (To be done only by qualified service-trained personnel on 7933 Disc Drives.) If the message persists, refer to the cleaning procedures in section III of this manual.
SPIN DWN	The spindle is spinning down.
SPIN UP	The spindle is spinning up.
STEP0=	Under certain conditions, this message may occur after the LOAD/UNLOAD switch is pressed. Press the END key to place the disc drive in operation.
STOPPED	The spindle is stopped. The disc drive is waiting for the LOAD/UNLOAD switch or the UNLOCK DOOR switch (on 7935 Disc Drives only) to be pressed.
TERR *** †	The diagnostic program experienced a test error which corresponds to the number nnn listed in Table 5-9, Test Error (TERR) Numbers.
TEST ERR †	The internal diagnostic found an error.
TESTING	The internal diagnostics are running.
UNLOAD	The heads are unloading.
UNLOCK	The UNLOCK DOOR switch on the control panel (7935 only) was pressed, but the top door did not open. Wait for five seconds and press the UNLOCK DOOR switch again.

Note: A media module, part number 97933-60000, is used with the HP 7933 Disc Drive.
A media module, product number 97935A, is used with the HP 7935 Disc Drive.

† *Indicates that service is required by qualified service-trained personnel.*

OPERATOR SWITCH FUNCTIONS

LOAD/UNLOAD switch	Performs the load function when set to the LOAD (in) position and the unload function when set to the UNLOAD (out) position. Before either operation is performed, the disc drive executive will request release from the system host to do the load or unload. The operation will only be done if either the host request times out, or the host grants release. If release is denied, the display will show a BUSY message until release is granted. If UNLOAD is entered by accident, pressing the switch back to the LOAD (in) position will cancel the effect of the switch if the disc drive is not already released. Only the UNLOAD function can abort the LOAD function. If the disc drive is under diagnostic program control, the load and unload functions are executed as soon as the switch is pressed. The contents of the diagnostic program table are unchanged.
Blank switch (7933 only)	Not used in the present configuration of the disc drive. Inadvertent operation of the switch may give an UNLOCK display message when the disc drive is in an unload condition.
UNLOCK DOOR switch (7935 only)	Unlocks the 7935 Disc Drive top door after the unload operation is completed. If the UNLOCK DOOR switch is pressed while the spindle is spinning at speed, the unlock request will be ignored. If the UNLOCK DOOR switch is pressed during a spindown cycle, the unlock request is saved until the spindle is stopped.

Figure 5-1. Disc Drive Control Panel

Table 5-1. Internal Diagnostic Utility Command Assignments

NUMBER	UTILITY COMMAND	EXTERNAL EXERCISER COMMAND*	REFER TO PARAGRAPH
	Head Positioning System Commands		
60	Logical Recalibrate		5-10
61	Seek		5-11
62	Alternate Seek		5-12
63	Incremental/Decremental Seek	INSK	5-13
64	Random Seek		5-14
65	Varying Length Alternate Seek		5-15
66	Check Seek and Verify Times		5-16
67	Adjust Seek Deceleration		5-17
68	Radial Head Alignment		5-18
69	Circumferential Head Skew		5-19
	Read/Write System Commands		
70	Read		5-21
71	Write		5-22
72	Transfer Length		5-23
73	Data Pattern		5-24
74	Spare Sector Retaining Data	SPARE	5-25
75	Spare Sector Without Retaining Data	SPARE	5-26
76	Format	INIT MEDIA	5-27
77	Clear Logs	CLEAR LOGS	5-28
78	No Verify For Seeks		5-29
79	Set Index		5-30
	Display Utilities		
80	Display Status	REQSTAT	5-32
81	Display Fault Log	FAULT LOG	5-33
82	Display Spare Tracks		5-34
83	Display Run Time Error Log	RUN LOG	5-35
84	Display Error Rate Test Log	ERT LOG	5-36
85	Display Board Revision	REV	5-37
86	Display Sensors	SENSE	5-38
87	Display Current Address		5-39
88	Loop	LOOP	5-40
	Error Rate Tests		
90	Read Only Error Rate Test	RO ERT	5-42
91	Pattern Error Rate Test		5-43
92	Short Error Rate Test		5-44
93	Random Error Rate Test		5-45
94	Random Read Only Error Rate Test		5-46
	Execute Immediately Utilities		
95	Velocity Loop Test		5-48
96	Keyboard Test		5-49
97	Air Purge		5-50
98	Clear Diagnostic Program		5-51
99	Seek Delay		5-52

*The MNEMONICS in this column refer to equivalent CS/80 External Exerciser Commands. Refer to the *CS/80 External Exerciser Reference Manual*, part no. 5955-3462 for details.

5-7. INTERNAL DIAGNOSTIC UTILITY COMMAND EXAMPLES

In order to illustrate the use of the internal diagnostic commands, the program entry sequences for a number of typical programs are given below. The first example is a procedure that has no parameters.

Keystrokes	Display	Remarks
	[????????]	Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	This example will cause the
6	[STEP0=6]	heads to recalibrate to
0	[RECAL]	logical 0, 0, 0.
ENTER	[STEP1=]	
RUN	[RUN]	
	[RECAL]	

Some procedures have parameters. This example will seek to the target address of cylinder 1000, head 4, and sector 90.

Keystrokes	Display	Remarks
	[????????]	Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
6	[STEP0=6]	
1	[SEEK]	Get Seek command.
ENTER	[CYL=]	
1	[CYL=1]	
0	[CYL=10]	
0	[CYL=100]	
0	[CYL=1000]	Set cylinder to 1000.
ENTER	[HEAD=]	
4	[HEAD=4]	Set head to 4.
ENTER	[SECT=]	
9	[SECT=9]	
0	[SECT=90]	Set sector to 90.
ENTER	[STEP1=]	
RUN	[RUN]	Run program.
	[CYL 1000] <--	Displayed for the seek delay time.
	[SEEK]	

If the default values for the head and sector could be used, the keystrokes for a seek to cylinder 10 would be as follows:

Keystrokes	Display		Remarks
	[????????]		Unknown display value.
9	[???????9]		
8	[CLEAR]		Clear diagnostic program.
ENTER	[STEP0=]		
6	[STEP0=6]		
1	[SEEK]		Get Seek command
ENTER	[CYL=]		
1	[CYL=1]		
0	[CYL=10		Set cylinder to 10.
ENTER	[HEAD]		Use last head.
ENTER	[SECT=]		Use last sector.
ENTER	[STEP1=]		
RUN	[RUN]		Run program.
	[CYL 10]	<--	Displayed for the seek delay time.
	[SEEK]		

If a seek to the current cylinder and head 4 is desired, the keystrokes would be as follows.

Keystrokes	Display		Remarks
	[????????]		Unknown display value.
9	[???????9]		
8	[CLEAR]		Clear diagnostic program.
ENTER	[STEP0=]		
6	[STEP0=6]		
1	[SEEK]		Get Seek command.
ENTER	[CYL=]		Use last cylinder.
ENTER	[HEAD=]		
4	[HEAD=4]		Set head to 4.
ENTER	[SECT=]		Use last sector.
ENTER	[STEP1=]		
RUN	[RUN]		Run program.
	[CYL 10]	<--	Displayed for the seek delay time.
	[SEEK]		

If it is desired to seek between cylinders 1 and 10 indefinitely, the keystrokes would be as follows:

Keystrokes	Display		Remarks
	[????????]		Unknown display value.
9	[????????9]		
8	[CLEAR]		Clear diagnostic program.
ENTER	[STEP0=]		
8	[STEP0=8]		
8	[LOOP]		Get Loop command.
ENTER	[NUM=]		Set number of loops to infinite.
ENTER	[STEP1=]		
6	[STEP1=6]		
2	[ALT SEEK]		Get Alternate Seek command.
ENTER	[CYL=]		
1	[CYL=1]		
0	[CYL=10]		Set first cylinder to 10.
ENTER	[CYL=]		
1	[CYL=1]		Set second cylinder to 1.
ENTER	[STEP2=]		
RUN	[RUN]		Run program.
	[CYL 10]	<--	The display will change after
	[CYL 1]		each seek. The next seek will
	[CYL 10]		not occur until the seek delay time is finished.
	.		
	.		
	.		
	[CYL 10]		
ENTER (or EDIT or CLEAR)	[LOOP]		

If it is desired to incrementally seek by two cylinders for five seeks starting backwards, the keystrokes would be as follows:

Keystrokes	Display	Remarks
	[????????]	Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
8	[STEP0=8]	
8	[LOOP]	Get Loop command.
ENTER	[NUM=]	
5	[NUM=5]	Set number of loops to 5.
ENTER	[END=]	Set ending step to last.
ENTER	[STEP1=]	
6	[STEP1=6]	

```
3               [INC SEEK]      Get Incremental Seek command.
ENTER           [    INC=]
2               [   INC=2]      Set cylinder increment to 2.
ENTER           [    DIR=]
1               [REVERSE ]      Set starting direction to
                                reverse.
ENTER           [  STEP2=]
RUN             [  RUN   ]      Run program.
                [CYL    8] <--  The display will change after
                [CYL    6]      each seek. The next seek will
                [CYL    4]      not occur until the seek delay
                [CYL    2]      time is finished.
                [CYL    0]
                [  LOOP  ]
```

If it is desired to set up some commands before the loop command, the keystrokes would be as follows. This example sets the transfer length to the number of sectors in one cylinder, then recalibrate to logical 0. The program loops on read and incremental seeks. When the complete volume is read, the disc drive does a recalibrate.

Keystrokes	Display	Remarks
	[????????]	Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
9	[STEP0=9]	
9	[SK DELAY]	Get Seek Delay command.
ENTER	[DLY=nnnn]	
CLEAR	[DLY=]	Clear the old delay.
0	[DLY=0]	Set seek delay to zero.
ENTER	[STEP0=]	
7	[STEP0=7]	
2	[XFER LEN]	Get Transfer Length command.
ENTER	[LEN=]	
1	[LEN=1]	
1	[LEN=11]	Set transfer length to number of
9	[LEN=119]	sectors in one cylinder.
6	[LEN=1196]	
ENTER	[STEP1=]	
6	[STEP1=6]	
0	[RECAL]	Get Recalibrate command.
ENTER	[STEP2=]	
8	[STEP2=8]	
8	[LOOP]	Get Loop command.
ENTER	[NUM=]	
1	[NUM=1]	
3	[NUM=13]	
2	[NUM=132]	
0	[NUM=1320]	Set loop number to 1320.

```
ENTER          [    END=]
4              [   END=4]      Set ending step to 4.
ENTER          [  STEP3=]
7              [ STEP3=7]
0              [  READ  ]      Get Read command.
ENTER          [  STEP4=]
6              [ STEP4=6]
3              [INC SEEK]      Get Incremental Seek command.
ENTER          [    INC=]      Set cylinder increment to 1.
ENTER          [    DIR=]      Set starting direction to
                                forward.
ENTER          [  STEP5=]
6              [ STEP5=6]
0              [ RECAL  ]      Get Recalibrate command.
ENTER          [  STEP6=]
RUN            [  RUN   ]      Run program.
               [CYL    0] <--  The display will change after
               [CYL    1]      each seek. The next seek will
                               not occur until the seek delay
                               time is finished.
                    .
                    .
                    .
               [CYL 1320]
               [XFER LEN]
```

If it is desired to examine a diagnostic program after it has been entered, the keystrokes would be as follows:

Keystrokes	Display	Remarks
	[????????]	Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
8	[STEP0=8]	
8	[LOOP]	Get Loop command.
ENTER	[NUM=]	
4	[NUM=4]	Set loop number to 4.
ENTER	[END=]	
ENTER	[STEP1=]	
6	[STEP1=6]	
2	[ALT SEEK]	Get Alternate Seek command.
ENTER	[CYL=]	
1	[CYL=1]	
0	[CYL=10]	Set first cylinder to 10.
ENTER	[CYL=]	
1	[CYL=1]	Set second cylinder to 1.
ENTER	[STEP2=]	

To examine the program entered above, the keystrokes would be as follows:

Keystrokes	Display	Remarks
EDIT	[STEP=]	
0	[STEP=0]	
ENTER	[LOOP]	Step 0.
Rv	[NUM= 4]	Parm 1.
Rv	[END=]	Parm 2.
Rv	[ALT SEEK]	Step 1.
Rv	[CYL= 10]	Parm 1.
Rv	[CYL= 1]	Parm 2.
Rv	[STEP2=]	Step 2.
Rv	[STEP3=]	Step 3.
Rv	[STEP4=]	Step 4.
Rv	[STEP5=]	Step 5.
Rv	[STEP6=]	Step 6.
Rv	[STEP7=]	Step 7.
Rv	[STEP8=]	Step 8.
Rv	[STEP9=]	Step 9.
Rv	[STEP9=]	Step 9 again.

If the zero was not entered in the above sequence, the step number to be edited would be the current step number. In the preceding two examples, the current step would be step 3.

To change step 1 from an alternate seek to an incremental seek, the keystrokes would be as follows:

Keystrokes	Display	Remarks
EDIT	[STEP=]	
1	[STEP=1]	
ENTER	[ALT SEEK]	Step 1.
CLEAR	[STEP1=]	Prompt for new step 1.
6	[STEP1=6]	
3	[INC SEEK]	Get Incremental Seek command.
ENTER	[INC=]	
2	[INC=2]	Set increment to 2.
ENTER	[DIR=]	Set direction to forward.
ENTER	[STEP2=]	
RUN	[RUN]	Run new program.

5-8. TROUBLESHOOTING

The disc drive incorporates a self-test set of diagnostics that simplify the process of diagnosing and locating hardware malfunctions. The diagnostics are capable of isolating a malfunction in a disc-based system to the disc drive with 99 percent accuracy. Once the disc drive has been identified as the cause of the system failure, the diagnostic routines can identify the particular failing subassembly within the disc drive with 95 percent confidence. The tests performed include internal diagnostics and a set of utilities which can be run off line or with an external exerciser.

The internal diagnostics (see table 5-2) are automatically executed at power on. The sequence of operation for the power on diagnostics is shown in figure 5-2. Also shown in figure 5-2 are the control panel display messages and disc drive operating states that occur during the power on diagnostic sequence. The object of these tests is to evoke all high level operations used during normal drive functions to verify that each is completed successfully. If a subassembly has been identified as faulty, the tests will terminate and the front panel display will indicate the source of the problem.

The microdiagnostic routines listed in table 5-2 test individual subassemblies up to the level where they interface with other subassemblies. The macrodiagnostic routines, also listed in table 5-2, involve multiple PCA testing and are generally used to test the interface between the PCA's. These operational tests deal with the performance of an entire functional system, for example the read/write system and the head positioning (servo) system.

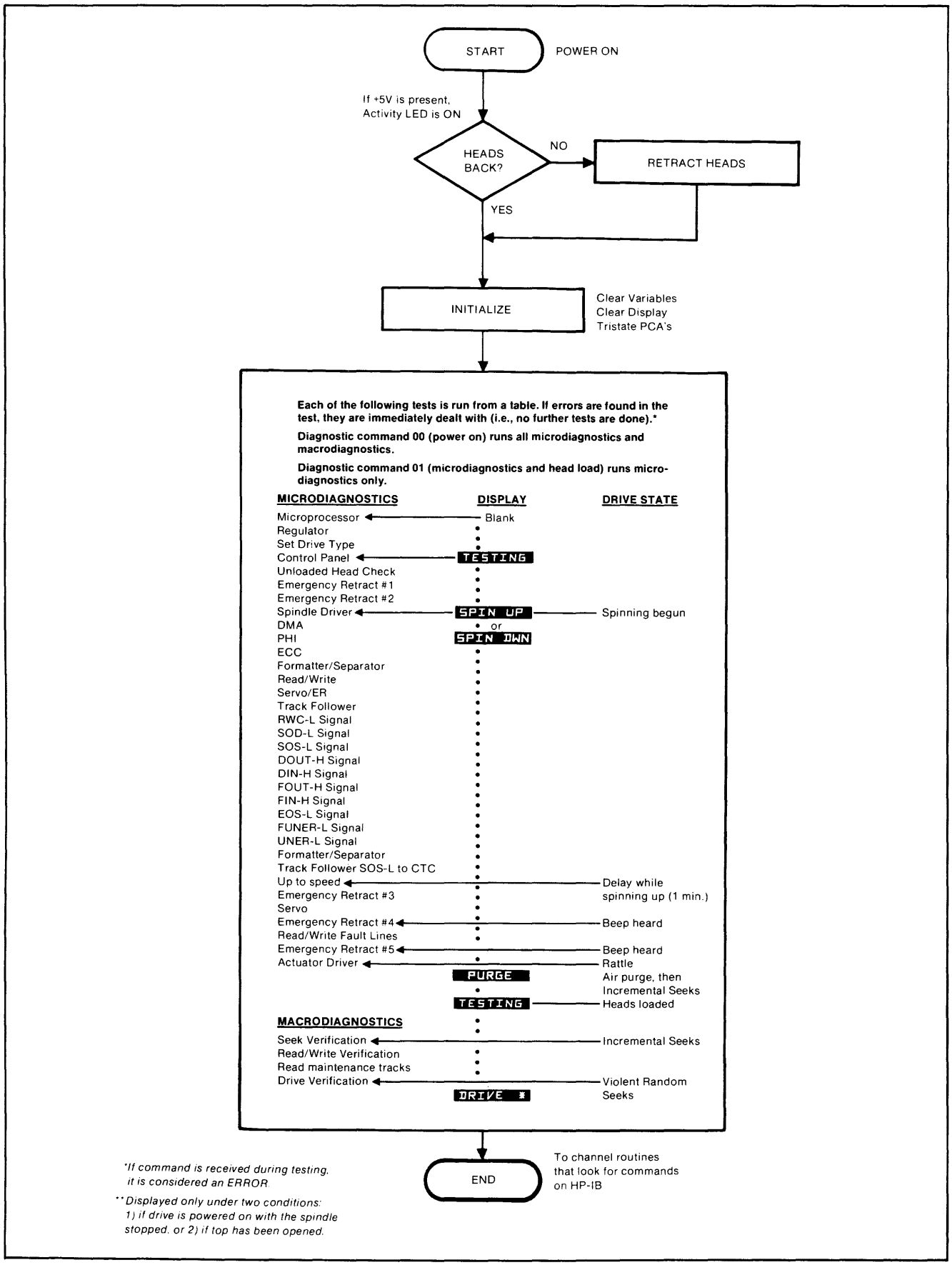
The disc drive has two dedicated maintenance tracks (2 and 1026). The system logs the various results of some of the self-test utilities on these tracks. The logs include a drive fault log, a run time data error log, an error rate test log, and an address of spared tracks log. Full details of these logs are provided in paragraphs 5-33, 5-35, 5-36, and 5-34, respectively.

Once control is given to the control panel keyboard, testing of the disc drive is possible without the need of the host CPU. With this control, the control panel display gives information relating to drive problems. This includes the most probable PCA's or assemblies that are responsible for a test failure.

An additional troubleshooting aid is provided by a CS/80 external exerciser that links the disc drive internal diagnostics and utility programs to service-trained personnel. These tests include a check of the HP-IB channel, as well as a complete interaction of the disc drive with the host CPU. For a detailed description of the external exerciser, refer to the *CS/80 External Exerciser Reference Manual,* part no. 5955-3462.

Table 5-2. Diagnostic Command Assignments

NUMBER	DIAGNOSTIC
	Diagnostic Commands
00	Power On Diagnostic (same as Macrodiagnostics numbers 01 through 05)
	Macrodiagnostics
01	Microdiagnostics and Head Load (same as Microdiagnostics numbers 06 through 40)
02	Seek Verification
03	Read/Write Verification
04	Read Maintenance Tracks
05	Drive Verification
	Microdiagnostics
06	Microprocessor
07	Regulator
08	Set Drive Type
09	Control Panel
10	Unloaded Head
11	Emergency Retract No. 1
12	Emergency Retract No. 2
13	Spindle Driver
14	DMA/CDMA/Cache
15	PHI
16	ECC
17	Formatter/Separator
18	Read/Write
19	Servo/Emergency Retract Interface
20	Track Follower
21	RWC-L signal
22	SOD-L signal
23	SOS-L signal
24	DOUT-H signal
25	DIN-H signal
26	FOUT-H signal
27	FIN-H signal
28	EOS-L signal
29	FUNER-L signal
30	UNER-L signal
31	Formatter/Separator Interface
32	Track Follower SOS-L to CTC
33	Up to Speed
34	Emergency Retract No. 3
35	Servo
36	Emergency Retract Speed Up
37	Emergency Retract No. 4
38	Read/Write Fault Lines
39	Emergency Retract No. 5
40	Actuator Driver
41-59	Undefined



7933-354A

Figure 5-2. Power-On Diagnostic Sequence

5-9. HEAD POSITIONING SYSTEM COMMANDS

5-10. LOGICAL RECALIBRATE

NUMBER : 60

NAME : [RECAL]

PARAMETER : none

DESCRIPTION : Causes the disc drive to recalibrate, then seek to logical cylinder, head, and sector 0. This is because physical cylinder 0 is a head alignment cylinder.

5-11. SEEK

NUMBER : 61

NAME : [SEEK]

PARAMETERS : cylinder number, head number, sector number

ASSIGNED
DEFAULTS : cylinder number = current cylinder
head number = current head
sector number = current sector

OUTPUT
DISPLAY
FORMAT : [CYL cccc]
where:
cccc = logical cylinder address

DESCRIPTION : Sets the target address to the address specified by the cylinder, head, and sector parameters and initiates a seek to the target address. The cylinder number is displayed and the seek delay is initiated. If any of the default addresses are used, that address remains unchanged. However, if any defaults are used on the first seek following release to the control panel, those addresses will be set to zero.

When the ENTER key is pressed, the cylinder will be prompted for by displaying [CYL=]. Up to four digits can be entered for the cylinder number. If an illegal cylinder is specified, [ILL PARM] will be displayed for approximately one second. This is followed by the cylinder prompt.

When the ENTER key is pressed, the head will be prompted for by displaying [HEAD=]. Up to two digits can be entered for the head number. If an

illegal head is specified, [ILL PARM] will be displayed for approximately one second. This is followed by the head prompt.

When the ENTER key is pressed, the sector will be prompted for by displaying [SECT=]. Up to two digits can be entered for the sector number. If an illegal sector is specified, [ILL PARM] will be displayed for approximately one second. This is followed by the sector prompt.

EXAMPLE : Set the target address to cylinder 625, head 3, sector 10.

Keystrokes	Display	Remarks
	[????????]	<-- Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
6	[STEP0=6]	
1	[SEEK]	Get Seek command.
ENTER	[CYL=]	
6	[CYL=6]	
2	[CYL=62]	
5	[CYL=625]	Set cylinder to 625.
ENTER	[HEAD=]	
3	[HEAD=3]	Set head to 3.
ENTER	[SECT=]	
1	[SECT=1]	
0	[SECT=10]	Set sector to 10.
ENTER	[STEP1=]	
RUN	[RUN]	
	[CYL 625]	<-- Display will change after the seek delay.
	[SEEK]	

5-12. ALTERNATE SEEK

NUMBER : 62

NAME : [ALT SEEK]

PARAMETERS : cylinder A, cylinder B

ASSIGNED DEFAULTS :
cylinder A = first logical cylinder (0)
cylinder B = last logical cylinder (1320)

OUTPUT DISPLAY FORMAT :
[CYL cccc]
where:
cccc = logical cylinder address

DESCRIPTION : Causes the disc drive to alternately seek from the first cylinder address to the second. The cylinder address is displayed and the seek delay is initiated. If the LOOP procedure is not entered at the beginning of the program, only the first seek will be done. The target head and sector addresses will remain unchanged.

When the ENTER key is pressed, the first cylinder will be prompted for by displaying [CYL=]. Up to four digits can be entered for the cylinder number. If an illegal cylinder is specified, [ILL PARM] will be displayed for approximately one second. This is followed by the cylinder prompt.

When the ENTER key is pressed, the second cylinder will be prompted for by the display [CYL=]. The cylinder number is displayed following the seek, and the seek delay is initiated. The next time an alternate seek is initiated, the other cylinder address will be the target address.

EXAMPLE : Cause the disc drive to seek between cylinder 10 and cylinder 1, until another command key is pressed.

Keystrokes	Display	Remarks
	[????????]	<-- Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
8	[STEP0=8]	
8	[LOOP]	Get Loop command.
ENTER	[NUM=]	Get infinite looping.
ENTER	[STEP1=]	
6	[STEP1=6]	
2	[ALT SEEK]	Get the Alternate Seek
ENTER	[CYL=]	command
1	[CYL=1]	
0	[CYL=10]	Set first cylinder to
ENTER	[CYL=]	10.
1	[CYL1=1]	Set second cylinder to
ENTER	[STEP2=]	1.
RUN	[RUN]	
	[CYL 10]	<-- Display will change
	[CYL 1]	after each seek. The
	[CYL 10]	next seek will not
	.	occur until the seek
	.	delay time is
		finished.
	[CYL 10]	
ENTER (or EDIT or CLEAR)	[LOOP]	

5-13. INCREMENTAL/DECREMENTAL SEEK

NUMBER : 63

NAME : [INC SEEK]

PARAMETER : cylinder increment
initial seek direction

ASSIGNED
DEFAULT : cylinder increment = 1
initial seek direction = forward

OUTPUT
DISPLAY
FORMAT : [CYL cccc]
where:
cccc = logical cylinder address

DESCRIPTION : Causes the disc drive to seek to the logical cylinder plus the cylinder increment specified. The resulting address is masked to be within the range of the disc drive. If the new address is illegal, the seek changes direction. The cylinder address is displayed and the seek delay is initiated. The target head and sector addresses will remain unchanged. If the loop procedure is not entered at the beginning of the program, only one seek will be done.

NOTE : There are certain combinations of current cylinder and cylinder increment that will cause illegal addresses for both incremental and decremental seeks. For this case the program will run normally, but seeks will not occur. For increments greater than 660, the seeks will not be incremental seeks at the specified increment.

When the ENTER key is pressed, the cylinder increment parameter is prompted for by displaying [INC=]. Up to four digits can be entered for the cylinder increment.

When the ENTER key is pressed, the initial seek direction parameter is prompted for by displaying [DIR=]. Only one digit can be entered for the initial seek direction. The number will cause one of the following messages to be displayed. If an illegal initial seek direction is specified, [ILL PARM] will be displayed for about one second. Then the initial seek direction prompt will be displayed.

The initial directions are: 0 = [FORWARD]
1 = [REVERSE]

EXAMPLE : Cause the disc drive to incrementally seek by one cylinder until another command key is pressed.

Keystrokes	Display	Remarks
	[????????]	<-- Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
8	[STEP0=8]	
8	[LOOP]	Get Loop command.
ENTER	[NUM=]	
ENTER	[STEP1=]	
6	[STEP1=6]	
3	[INC SEEK]	Get Incremental Seek command.
ENTER	[INC=]	Use default increment.
ENTER	[DIR=]	Use default direction.
ENTER	[STEP2=]	
RUN	[RUN]	
	[CYL 1]	<-- Display will change
	[CYL 2]	after each seek. The
	[CYL 3]	next seek will not
	.	occur until the seek
	.	delay time is
		finished.
	[CYL nnnn]	
ENTER	[LOOP]	
(or EDIT or CLEAR)		

5-14. RANDOM SEEK

NUMBER : 64

NAME : [RND SEEK]

PARAMETER : none

OUTPUT DISPLAY FORMAT : [CYL cccc]
where:
cccc = logical cylinder address

DESCRIPTION : Causes the disc drive to seek to a random cylinder. If the Loop procedure is not entered at the beginning of the program, only one random seek will be done. The target head and sector addresses will remain unchanged.

EXAMPLE : Cause the disc drive to random seek until another command key is pressed.

Keystrokes	Display	Remarks
	[????????]	<-- Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
8	[STEP0=8]	
8	[LOOP]	Get Loop command.
ENTER	[NUM=]	Get infinite loops.
ENTER	[STEP1=]	
6	[STEP1=6]	
4	[RND SEEK]	Get Random Seek command.
ENTER	[STEP2=]	
RUN	[RUN]	
	[CYL nnnn]	<-- Display will change
	[CYL nnnn]	after each seek. The
	[CYL nnnn]	next seek will not
	.	occur until the seek
	.	delay time is finished.
	[CYL nnnn]	
ENTER (or EDIT or CLEAR)	[LOOP]	

5-15. VARYING LENGTH ALTERNATE SEEK

NUMBER : 65

NAME : [VLA SEEK]

PARAMETER : none

OUTPUT DISPLAY FORMAT: [VLA SEEK]

DESCRIPTION : Causes the disc drive to do a maximum physical alternate seek. Subsequent seeks will have the target address one cylinder closer to the center of the disc address range than the previous seek. This continues until the seek length reaches zero. At this time, the target addresses will start getting further apart. This continues until an illegal address is generated, at which time the cycle starts over again. This causes all tracks to be accessed and all possible lengths of seeks to be run. If the Loop procedure is not entered at the beginning of the program, only one seek will be done. The target head and sector addresses will remain unchanged.

This command does not use the same target address variables that the other seeks do. This is because two sets of addresses must be saved so that one or the other can be incremented or decremented as needed.

5-16. CHECK SEEK AND VERIFY TIMES

NUMBER : 66

NAME : [VFY TIME]

PARAMETER : cylinder increment
initial seek direction

ASSIGNED
DEFAULT : cylinder increment = 1
initial seek direction = forward

OUTPUT
DISPLAY
FORMAT: [ss.s v.v]
where:
ss.s = seek time in milliseconds
v.v = verify time in milliseconds

DESCRIPTION : Causes the disc drive to seek to the physical cylinder plus the cylinder increment specified. If the new address is illegal, the seek changes direction. The seek and verify times are displayed and the seek delay is initiated. If the loop procedure is not entered at the beginning of the program, only one seek will be done. The target head and sector addresses will remain unchanged.

NOTE : The timing resolution is in 100 microsecond steps.

When the ENTER key is pressed, the cylinder increment parameter is prompted for by displaying [INC=]. Up to four digits can be entered for the cylinder increment.

When the ENTER key is pressed, the initial seek direction parameter is prompted for by displaying [DIR=]. Only one digit can be entered for the initial seek direction. The number will cause one of the following messages to be displayed. If an illegal initial seek direction is specified, [ILL PARM] will be displayed for about one second. Then the initial seek direction prompt will be displayed.

Initial seek directions are: 0 = [FORWARD]
1 = [REVERSE]

EXAMPLE : Cause the disc drive to verify single track seeks until another command key is pressed.

Keystrokes	Display	Remarks
	[????????]	<-- Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
9	[STEP0=9]	
9	[SK DELAY]	Get Seek Delay command.
ENTER	[DLY=nnnn]	
CLEAR	[DLY=]	Clear old delay.
2	[DLY=2]	
0	[DLY=20]	
0	[DLY=200]	Set seek delay to 200.
ENTER	[STEP0=]	
8	[STEP0=8]	
8	[LOOP]	Get Loop command.
ENTER	[NUM=]	Use default loop number.
ENTER	[STEP1=]	
6	[STEP1=6]	
6	[VFY TIME]	Get Verify Seek Times command.
ENTER	[INC=]	Use default increment.
ENTER	[DIR=]	Use default direction.
ENTER	[STEP2=]	
RUN	[RUN]	
	[ss.s v.v]	<-- Display will change
	[ss.s v.v]	after each seek. The
	[ss.s v.v]	next seek will not
	.	occur until the seek
	.	delay time is
		finished.
	[ss.s v.v]	
ENTER (or EDIT or CLEAR)	[LOOP]	

5-17. ADJUST SEEK DECELERATION

NUMBER : 67

NAME : [ADJ DECL]

PARAMETERS : none

OUTPUT DISPLAY FORMAT : [Fff Rrr]
where:
ff = forward seek deceleration value
rr = reverse seek deceleration value

DESCRIPTION : Causes the disc drive to alternately seek from physical cylinder/100 to physical cylinder 1300. The seek deceleration values are displayed and the seek delay is initiated. If the LOOP procedure is not entered at the beginning of the program, only the first seek will be done. The target head and sector addresses will remain unchanged. The seek delay for this command is fixed to prevent overheating the actuator.

5-18. RADIAL HEAD ALIGNMENT

NUMBER : 68

NAME : [HD ALIGN]

PARAMETERs : head number, alignment band number

ASSIGNED DEFAULTs : head number = all heads
alignment band number = 1 (middle alignment band)

OUTPUT DISPLAY FORMAT: [hh snnn]
where:
hh = head number
s = sign of head offset
nnn = head offset value measured in 6.25 microinch steps.

DESCRIPTION : Displays the current head offset for the head specified so that the head can be adjusted. The target cylinder address will be set to the appropriate alignment band address. The target sector address will remain unchanged.

An automatic loop feature is built into the procedure. This updates the display on a periodic basis so that the head offset readout will change as the head is being adjusted. A R↓ (Roll) key entry is required to continue to the next head when the default head number is specified or to move to the next procedure when a specific head is specified.

NOTE : Following this procedure, automatic head alignment will occur.

When the ENTER key is pressed, the head will be prompted for by displaying [HEAD=]. Up to two digits can be entered for the head number. If an illegal head is specified, [ILL PARM] will be displayed for approximately one second. This is followed by the head prompt. If no head is

specified, all heads, in order, will have the alignment displayed. This facilitates a check of all heads.

When the ENTER key is pressed, the alignment band number will be prompted for by displaying [BAND=]. Only 0, 1 or 2 can be entered for the alignment band number. If an illegal alignment band is specified, [ILL PARM] will be displayed for approximately one second. This is followed by the alignment band prompt.

NOTE : During radial head alignment, background diagnostics are not running. This prevents unexpected carriage movement.

5-19. CIRCUMFERENTIAL HEAD SKEW

NUMBER : 69

NAME : [HD SKEW]

PARAMETERS : head number, alignment band number

ASSIGNED DEFAULTS : head number = all heads,
alignment band number = 1

OUTPUT DISPLAY FORMAT: [hh snnn]
where:
hh = head number
s = sign of head skew
nnn = head skew value measured in 0.311 microsecond steps.

DESCRIPTION : Displays the head skew value for the specified head. The target cylinder address will be set to the appropriate alignment band address. The target sector address will remain unchanged. A R↓ (Roll) key entry is required to continue to the next head when the default head number is specified, or to move to the next procedure when a specific head is specified.

NOTE: Following this procedure, automatic head alignment will occur.

When the ENTER key is pressed, the head will be prompted for by displaying [HEAD=]. Up to two digits can be entered for the head number. If an illegal head is specified, [Ill PARM] will be displayed for about one second. This is followed

by the head prompt. If no head is specified, all heads in order will have the timing displayed. This is to facilitate a check of all heads.

When the ENTER key is pressed, the alignment band number will be prompted for by displaying [BAND=]. Only 0, 1 or 2 can be entered for the alignment band number. If an illegal alignment band is specified, [ILL PARM] will be displayed for approximately one second. This is followed by the aligment band prompt.

NOTE : During circumferential head skew, background diagnostics are not running. This prevents unexpected carriage movement.

5-20. READ/WRITE SYSTEM COMMANDS

5-21. READ

NUMBER : 70

NAME : [READ]

PARAMETER : none

DESCRIPTION : Reads data from the disc starting from the current target address, for the length specified by the Transfer Length command, and puts the data into the DMA buffer. If more data is transferred than will fit in the buffer, the data will wrap around. Data is not transferred out of the DMA buffer. The data is not compared with anything. The internal error detection hardware is used to determine whether or not the data is correct.

At the end of the data transfer to the DMA buffer, the target addresses will not be updated. This means that two read commands will read the same data.

NOTE : If the transfer length command is not part of the current program, data transfers will not occur.

EXAMPLE : Cause the disc drive to read cylinder 125 twenty times.

Keystrokes	Display	Remarks
	[????????] <--	Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.

```
ENTER       [  STEP0=]
9           [ STEP0=9]
9           [SK DELAY]     Get Seek Delay command.
ENTER       [DLY=nnnn]
CLEAR       [    DLY=]     Clear the old delay.
0           [   DLY=0]     Set seek delay to zero.
ENTER       [  STEP0=]
7           [ STEP0=7]
2           [XFER LEN]     Get Transfer Length
                           command.
ENTER       [    LEN=]
1           [   LEN=1]
1           [  LEN=11]
9           [ LEN=119]     Set length to
6           [LEN=1196]     a full cylinder.
ENTER       [  STEP1=]
8           [ STEP1=8]
8           [  LOOP  ]     Get Loop command.
ENTER       [    NUM=]
2           [   NUM=2]
0           [  NUM=20]     Set loop number to 20.
ENTER       [    END=]     Set ending step to
                           end.
ENTER       [  STEP2=]
6           [ STEP2=6]
1           [  SEEK  ]     Get Seek command.
ENTER       [    CYL=]
1           [   CYL=1]
2           [  CYL=12]
5           [ CYL=125]     Set cylinder to 100.
ENTER       [   HEAD=]
0           [  HEAD=0]     Set head to 0.
ENTER       [   SECT=]
0           [  SECT=0]     Set sector to 0.
ENTER       [  STEP3=]
7           [ STEP3=7]
0           [  READ  ]     Get Read command.
ENTER       [  STEP4=]
RUN         [  RUN   ]     Run program.
            [CYL  125] <-- Display will remain
            [XFER LEN]     until test is
                           completed.
```

5-22. WRITE

NUMBER : 71

NAME : [WRITE]

PARAMETER : none

DESCRIPTION : Writes to the disc starting from the current target address and for the length specified by the Transfer Length command. The data to be written will start at the beginning of the DMA buffer. If the transfer length is longer than the DMA buffer,

the buffer will wrap around. If the Define Data Pattern command did not precede the write, the previous contents of the DMA buffer will be used for data.

At the end of the data transfer to the DMA buffer, the target addresses will not be updated. This means that two successive write commands will write the same sectors.

NOTE : If the transfer length command is not part of the current program, data transfers will not occur. This will help prevent accidental writes.

EXAMPLE : Cause the disc drive to write surface 5 with a specified pattern.

Keystrokes	Display	Remarks
	[????????]	<-- Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
9	[STEP0=9]	
9	[SK DELAY]	Get seek delay.
ENTER	[DLY=nnnn]	
CLEAR	[DLY=]	Clear old delay.
0	[DLY=0]	Set seek delay to zero.
ENTER	[STEP0=]	
7	[STEP0=7]	
2	[XFER LEN]	Get Transfer Length command.
ENTER	[LEN=]	
9	[LEN=9]	Set length to
2	[LEN=92]	a full track.
ENTER	[STEP1=]	
7	[STEP1=7]	
3	[DATA PAT]	Get data pattern command.
ENTER	[PATT=%]	Set the default pattern.
ENTER	[STEP2=]	
6	[STEP2=6]	
1	[SEEK]	Get Seek command.
ENTER	[CYL=]	
0	[CYL=0]	Set cylinder to 0.
ENTER	[HEAD=]	
5	[HEAD=5]	Set head to 5.
ENTER	[SECT=]	Use last sector.
ENTER	[STEP3=]	
8	[STEP3=8]	
8	[LOOP]	Get Loop command.

```
ENTER          [    NUM=]
1              [   NUM=1]
3              [  NUM=13]
2              [ NUM=132]
0              [NUM=1320]     Set loop number to
                              1320.
ENTER          [    END=]     Set ending step to end.
ENTER          [  STEP4=]
7              [ STEP4=7]
1              [ WRITE  ]     Get Write command.
ENTER          [  STEP5=]
6              [ STEP5=6]
3              [INC SEEK]     Get Incremental Seek
                              command.
ENTER          [    INC=]
ENTER          [    DIR=]
ENTER          [  STEP6=]
RUN            [  RUN   ]     Run program.
                [CYL    1] <-- Display will change
                [CYL    2]     after each seek.
                     .
                     .
                [CYL 1320]
                [XFER LEN]
```

5-23. TRANSFER LENGTH

NUMBER : 72

NAME : [XFER LEN]

PARAMETER : length in sectors

ASSIGNED DEFAULT : length in sectors = 0

DESCRIPTION : Sets the data transfer length to the length parameter, that is, the number of sectors to transfer. The transfer length parameter will be prompted for by displaying [LEN=]. Up to four digits can be entered for the transfer length. If the transfer length procedure is not used in the current program containing the read or write commands, the transfer length will be set to zero so data transfers will not occur.

Note: The transfer length for a track is 92 sectors. The transfer length for a cylinder is 1196 sectors.

5-24. DATA PATTERN

NUMBER : 73

NAME : [DATA PAT]

PARAMETER : 16 - bit octal pattern

ASSIGNED
DEFAULT : 16 bit octal pattern = %177777 (all ones)

DESCRIPTION : Sets the contents of the DMA buffer to the 16-bit octal pattern specified in the pattern parameter. When the ENTER key is pressed, the pattern will be prompted for by displaying [PATT=%]. The percent symbol is a reminder that this number is octal. Up to six octal digits can be entered, although only the last 16 bits will be used for the data pattern. If less than six digits are entered, the leading bits will be zero. The data pattern is checked for octal errors when it is entered from the keyboard.

When release is granted to the HIO, the data pattern is set to all ones for data security.

5-25. SPARE SECTOR RETAINING DATA

NUMBER : 74

NAME : [SPARE]

PARAMETERS : cylinder, head, sector
spare type number

ASSIGNED
DEFAULTS : cyl,head,sect,- no parameter = no operation

DESCRIPTION : Spares the sector pointed to by the target cylinder, head, and sector parameters. The data for the sector to be spared is lost. The data for the remainder of the track is saved. This is the normal spare command. If the sector to be spared can not be verified, this command will not work. The Spare Without Retaining Data command must be used.

If the default parameters are used, [NO DEFLT] will be displayed for approximately one second. This is followed by the procedure prompt. In this manner, the user must explicitly specify where the sector to be spared is located. This helps prevent accidental writes to the disc. After the spare, the status is cleared since sparing changes certain parameters in status.

When the ENTER key is pressed, the cylinder will be prompted for by displaying [CYL=]. Up to four digits can be entered for the cylinder number. If an illegal cylinder is specified [ILL PARM] will be displayed for approximately one second. This is followed by the cylinder prompt.

When the ENTER key is pressed, the head will be prompted by displaying [HEAD=]. Up to two digits can be entered for the head number. If an illegal

head is specified, [ILL PARM] will be displayed for approximately one second. This is followed by the head prompt.

When the ENTER key is pressed, the sector will be prompted for by displaying [SECT=]. Up to two digits can be entered for the sector number. If an illegal sector is specified, [ILL PARM] will be displayed for approximately one second. This is followed by the sector prompt.

5-26. SPARE SECTOR WITHOUT RETAINING DATA

NUMBER : 75

NAME : [SPR NDAT]

PARAMETERS : cylinder, head, sector
spare type number

ASSIGNED DEFAULTS : cyl,head,sect,- no parameter = no operation

DESCRIPTION : Spares the sector pointed to by the target cylinder, head, and sector parameters. The data for the entire track is lost. This command allows sparing of sectors that cannot be verified.

If the default parameters are used, [NO DEFLT] will be displayed for approximately one second. This is followed by the procedure prompt. In this manner, the user must explicitly specify where the sector to be spared is located. This helps prevent accidental writes to the disc. After the spare, the status is cleared since sparing changes certain parameters in status.

When the ENTER key is pressed, the cylinder will be prompted for by displaying [CYL=]. Up to four digits can be entered for the cylinder number. If an illegal cylinder is specified [ILL PARM] will be displayed for approximately one second. This is followed by the cylinder prompt.

When the ENTER key is pressed, the head will be prompted by displaying [HEAD=]. Up to two digits can be entered for the head number. If an illegal head is specified, [ILL PARM] will be displayed for approximately one second. This is followed by the head prompt.

When the ENTER key is pressed, the sector will be prompted for by displaying [SECT=]. Up to two digits can be entered for the sector number. If an

illegal sector is specified, [ILL PARM] will be displayed for approximately one second. This is followed by the sector prompt.

5-27. FORMAT

NUMBER : 76

NAME : [FORMAT]

PARAMETERS : type number
clear number

ASSIGNED DEFAULTS :
format type - no parameter = no operation
clear - no parameter = no operation

OUTPUT DISPLAY FORMAT : [PCYLcccc]
where:
PYCL = physical cylinder addresses
cccc = cylinder number

DESCRIPTION : Uses the clear parameter, telling whether to clear the user defined spare tracks or not in reformatting the disc drive. The interleave cannot be changed from the control panel. The default and clear parameters are not allowed. This requires the user to explicitly specify the use of the current spare tracks to prevent accidental writes.

Logical formats verify that the heads are on the correct track before writing. It is recommended that after a logical format, the Pattern Error Rate test be run for sufficient time to find defects in the media again. Once format is started, it cannot be interrupted from the control panel. On the disc drive, the format command takes about 15 minutes to complete.

Maintenance Track Format (MNT TRK) will reformat only the maintenance tracks without affecting spares or user data.

When the ENTER key is pressed, the type of format will be prompted for by displaying [TYPE=]. Only one digit can be entered for the type. The number will cause one of the following messages to be displayed. If an illegal type is specifed, [ILL PARM] will be displayed for approximately one second. This is followed by the type prompt. If the default parameter is used, [NO DEFLT] will be displayed for about one second. The step prompt will then be displayed.

The types are: 0 = [LOGICAL]
1 = [MNT TRK]

If logical formats were selected when the ENTER key is pressed, the clear parameter will be prompted for by displaying [CLEAR=]. Only one digit can be entered for the clear parameter. The number will cause one of the following messages to be displayed. If an illegal clear parameter is specifed, [ILL PARM] will be displayed for approximately one second. This is followed by the clear parameter prompt. If the default parameter is used, [NO DEFLT] will be displayed for about one second. The step prompt will then be displayed.

The clear values are: 0 = [USE TRKS]
1 = [CLR TRKS]

5-28. CLEAR LOGS

NUMBER : 77

NAME : [CLR LOGS]

PARAMETER : none

DESCRIPTION : Clears the fault log, the run time error log, and the error rate test log for all heads.

5-29. NO VERIFY FOR SEEKS

NUMBER : 78

NAME : [NOVERIFY]

PARAMETER none

DESCRIPTION : Causes the drive firmware to not verify the target cylinder address at the end of the seek. If the no verify procedure is not part of the current program, the target address will be verified at the end of each seek.

The no seek verify command needs to be entered into the program before the seek so that the seek will not automatically verify.

5-30. SET INDEX

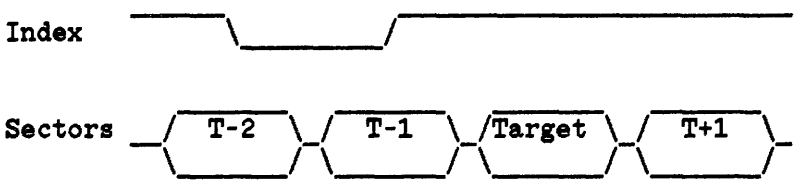
NUMBER : 79

NAME : [SET INDX]

PARAMETER : none

DESCRIPTION : Causes the drive electronics to generate the index pulse preceeding the target logical sector specified by the last seek command. If the set index procedure is not part of the current program, the index pulse will occur at an undefined sector.

The Set Index command needs to be entered into the program before the seek so that at the end of the seek the index pulse can be generated in the correct place. The waveform for the position of the index pulse with respect to the target sector is shown below.



5-31. DISPLAY UTILITIES

5-32. DISPLAY STATUS

NUMBER : 80

NAME : [STATUS]

PARAMETER : none

OUTPUT DISPLAY FORMAT : [STSn%sss]
where:
n = status byte number
sss = octal status value as listed in Table 5-3, Status Buffer Values

[CYL cccc]
where:
cccc = logical cylinder number

[HEAD nn]
where:
nn = head number

[SECT nn]
where:
nn = sector number

[PART nn]
where:
nn = failed part number as listed in Table 5-4, Failed Part (PART) Numbers.

[DERR nnn] or [TERR nnn]
where:
nnn = error number found in Table 5-8, Drive Error (DERR) Numbers or Table 5-9, Test Error (TERR) Numbers.

[HFR %nnn]
where:
nnn = Hardware Fault Register contents in octal as listed in Table 5-5, Hardware Fault Register (HFR) Numbers.

DESCRIPTION : Displays the contents of the status buffer. Up to eight values of status can be displayed (table 5-3). If a particular status byte is zero, it will not be displayed. The status values are displayed in octal so that the different values can be added since more than one bit in a particular status byte can be set. Status is cleared after the last status message is displayed. A Rv (ROLL) key entry is required to continue to the next displayed value or to the next program step if it is the last value.

Following the status bytes, other information may also be displayed, depending upon which status bits are set. If status shows that an address is included, the CYL, HEAD and SECT messages will be displayed. If there are any drive faults, the DERR message (table 5-8) will be displayed for up to 4 faults. If the diagnostic failed, the PART (table 5-4) and TERR (table 5-9) messages will show the failed part number(s) and the error(s) that caused it.

Table 5-3. Status Buffer Values

NUMBER	VALUE[1]
	Reject Status Byte 0
STS1%001	Received illegal address
STS1%002	Received illegal unit or volume address
STS1%004	Received unrecognized opcode
STS1%040	Received command without odd parity
	Reject Status Byte 1
STS1%010	Wrong execution message length
STS1%040	Message sequence violation
STS1%100	Received parameter of wrong value
STS1%200	Parameter exceeded device maximum
	Fault Status Byte 0
STS2%002	Unit hardware fault
STS2%020	Controller Hardware fault
	Fault Status Byte 1
STS3%001	Retransmit command
STS3%002	Recovered from power failure
STS3%010	Release required for internal maintenance
STS3%020	Release requested for diagnostics
STS3%040	Release required for operator
STS3%200	Diagnostic failed[2]
	Access Status Byte 0
STS4%004	The block has not been written
STS4%010	Volume is write protected
STS4%020	Unit is not ready for access
STS4%040	No spare trcks availabie
STS4%100	Uninitialized media
STS4%200	Illegal parallel operation
	Access Status Byte 1
STS5%010	Attempt to transfer past end of volume
STS5%020	Attempt to transfer past end of file
STS5%100	Unrecoverable data[3]
STS5%200	Unrecoverable data overflow
	Information Status Byte 0
STS6%010	Latency induced for slow data transfer
STS6%020	Only one spare track remaining
STS6%040	Request release for internal maintenance
STS6%100	Request release for diagnostics
STS6%200	Request release for operator
	Information Status Byte 1
STS7%004	Error and fault logs are full
STS7%020	Latency induced to correct data[3]
STS7%040	Marginal data[3]
STS7%100	Recoverable data overflow

[1] Messages are bit significant; more than one bit can be set per byte.
[2] Failed part numbers and errors follow.
[3] An address follows.

Table 5-4. Failed Part (PART) Numbers

NUMBER	FAILED PART
1	Regulator PCA-A1
2	Actuator Driver PCA-A2/Emergency Retract PCA-A20
3	Servo PCA-A3
4	Microprocessor PCA-A4
5	DMA No. 2 or Cache PCA-A5
6	DMA No. 1 or CDMA PCA-A6
8	Formatter/Separator PCA-A8
9	Track Follower PCA-A9
10	Read/Write PCA-A10
11	Motherboard PCA-A11
12	Spindle Driver PCA-A12
13	Rectifier PCA-A13
14	Control Panel PCA-A14
17	HP-IB PCA-A17
18	Actuator Status PCA-A18
19	Module Detect PCA-A19
20	Data head 0
21	Data head 1
22	Data head 2
23	Data head 3
24	Data head 4
25	Data head 5
26	Data head 6
27	Data head 7
28	Data head 8
29	Data head 9
30	Data head 10
31	Data head 11
32	Data head 12
33	Servo head
34	not assigned
35	Media module
36	Actuator coil connector
37	Fan
38	Tachometer
39	Spindle motor
40	Actuator +36V fuse, F540
41	Actuator -30V fuse, F550
42	Spindle +36V fuse, F590
43	Spindle -36V fuse, F580
44	Air filters

Table 5-5. Hardware Fault Register (HFR) Numbers

NUMBER	HARDWARE FAULT[1]
HFR%001	Spindle speed is down
HFR%002	Heads are off track
HFR%010	Track follower phase lock loop error
HFR%020	Top door is open
HFR%040	Emergency retract is set
HFR%100	Power failure
HFR%200	Read/write fault

[1] Messages are bit significant; more than one bit can be set per byte.

5-33. DISPLAY FAULT LOG

NUMBER : 81

NAME : [FLT LOG]

PARAMETER : none

OUTPUT
DISPLAY
FORMAT : [DERR nnn] or [TERR nnn]
where:
nnn = error number

[HFR %nnn]
where:
nnn = Hardware Fault Register contents in octal found in Table 5-5, Hardware Fault Register (HFR) Numbers.

DESCRIPTION : Displays the error numbers from the fault log in reverse chronological order. In other words the last error is the first to be displayed. If there are no errors in the log, nothing will be displayed. A Rv (Roll) key entry is required to continue to the next displayed value or to the next program step if it is the last value.

5-34. DISPLAY SPARE TRACKS

NUMBER : 82

NAME : [DSP SPRS]

PARAMETER : head number

ASSIGNED
DEFAULT : head number = all heads

OUTPUT
DISPLAY
FORMAT : [hh cccc] or [hh NONE]
where:
hh = head number
cccc = cylinder number

DESCRIPTION : Reads the spare track table for the specified head. The head and cylinder numbers for the spare tracks will be displayed. If the default head is used, the spare tracks for all heads will be displayed. A Rv (Roll) key entry is required to continue to the next displayed value or to the next program step if it is the last value.

When the ENTER key is pressed, the head number will be prompted for by [HEAD=] being displayed. Up to two digits can be entered for the head number. If an illegal head number is specified, [ILL PARM] will be displayed for about one second. This is followed by the head prompt.

5-35. DISPLAY RUN TIME ERROR RATE LOG

NUMBER : 83

NAME : [ERR LOG]

PARAMETER : head number

ASSIGNED
DEFAULT : head number = all heads

OUTPUT
DISPLAY
FORMAT : [HEAD nn]
where:
nn = head number

[s.ssEee]
where:
s.ssEee = number of sectors transferred expressed in scientific notation

[CORnnnnn]
where:
nnnnn = number of correctable errors

[UCOR nnn]
where:
nnn = number of uncorrectable errors

DESCRIPTION : Reads the run time error log for the head specified. If the default head is specified, the error rate for all the heads will be displayed. Four entries will be displayed for each head. First is the head number, followed by the number of sectors transferred, followed by the number of correctable errors, followed by the number of uncorrectable errors. A Rv (Roll) key entry is required to continue to the next displayed value or to the next program step if it is the last value.

Correctable errors in the RUN LOG are actually a count of the times that a Single Read Retry was induced to correct the data. If more than one retry was required, it is logged in the uncorrectable count. ECC correctable errors are ignored.

When the ENTER key is pressed, the head will be prompted for by displaying [HEAD=]. Up to two digits can be entered for the head number. If an

illegal head is specified, [ILL PARM] will be displayed for about one second. This is followed by the head prompt.

5-36. DISPLAY ERROR RATE TEST ERROR LOG

NUMBER : 84

NAME : [ERT LOG]

PARAMETER : head number

ASSIGNED DEFAULT : head number = all heads

OUTPUT DISPLAY FORMAT :

[HEAD nn]
where:
nn = head number

[s.ssEee]
where:
s.ssEee = number of sectors transferred in scientific notation

[CORnnnnn]
where:
nnnnn = number of correctable errors

[UCOR nnn]
where:
nnn = number of uncorrectable errors

DESCRIPTION : Reads the error rate test log for the head specified. If the default head is specified, the error rate for all the heads will be displayed. Four entries will be displayed for each head. First is the head number, followed by the number of sectors transferred, followed by the number of correctable errors, followed by the number of uncorrectable errors. A Rv (Roll) key entry is required to continue to the next displayed value or to the next program step if it is the last value.

When the ENTER key is pressed, the head will be prompted for by displaying [HEAD=]. Up to two digits can be entered for the head number. If an illegal head is specified, [ILL PARM] will be displayed for about one second. This is followed by the head prompt.

5-37. DISPLAY BOARD REVISION

NUMBER : 85

NAME : [REV CODE]

PARAMETER : part number

ASSIGNED
DEFAULT : part number = all parts

OUTPUT
DISPLAY
FORMAT : [pp aa-r] or [pp NONE]
where:
pp = part number found in table 5-6, Revision Code part numbers
aa = major revision (all ROMs replaced)
r = minor revision (ROMs replaced individually)

DESCRIPTION : Reads the revision register for the part number specified, formats the data, and displays it. If the part is not specified, all parts in order, will have the revision displayed. This is to facilitate a rapid check of all parts. A Rv (Roll) key entry is required to continue to the next displayed value or to the next program step if it is the last value.

When the ENTER key is pressed, the part will be prompted for by displaying [PART=]. Up to two digits can be entered for the part number. If an illegal part is specified, [ILL PARM] will be displayed for about one second. This is followed by the part prompt.

5-38. DISPLAY SENSORS

NUMBER : 86

NAME : [DSP SENS]

PARAMETER : sensor number

ASSIGNED
DEFAULT : sensor number = all sensors

OUTPUT
DISPLAY
FORMAT : [n GOOD] or [n BAD] for the pressure sensors
[n vvvC] for the temperature sensors
where:
n = sensor number
vvv = temperature in celsius
c = celsius

[HFR %nnn] for hardware fault register.
where: nnn=hardware fault register contents in octal as listed in Table 5-5, Hardware Fault Register numbers.

[RWFR %nn] for the read/write fault register contents listed in Table 5-7, Read/Write Fault Register Numbers.

DESCRIPTION : Reads the value of the sensor specified. If the sensor is a temperature sensor, it converts the temperature to Celsius, and displays it. If a pressure sensor is specified, the display will indicate if the pressure is good or bad. If the sensor is not specified, all sensors, in order, will have their values displayed. This is to facilitate a rapid check of all sensors. A Rv (Roll) key entry is required to continue to the next displayed value or to the next program step if it is the last value.

When the ENTER key is pressed, the sensor will be prompted for by displaying [SENSOR=]. Only one digit can be entered for the sensor number. The number will cause one of the following messages to be displayed so that the user can verify that the correct sensor was selected. If an illegal sensor is specified, [ILL PARM] will be displayed for about one second. This is followed by the sensor prompt.

The sensors are: 0 = Not Assigned
1 = [FILTER]
2 = [EXIT AIR]
3 = [ACTUATOR]
4 = [HDWR FLT]
5 = [RWFR FLT]

5-39. DISPLAY CURRENT ADDRESS

NUMBER : 87

NAME : [DSP ADDR]

PARAMETER : none

OUTPUT DISPLAY FORMAT : [CYL cccc] or [PCYLcccc]
where:
CYL = logical cylinder addresses
PCYL = physical cylinder addresses
cccc = cylinder number

[HEAD nn]
where:
nn = head number

[SECT nn]
where:
nn = sector number

DESCRIPTION : Displays the current cylinder, head, and sector addresses. The physical address will be displayed when the current cylinder was specified as a physical target address rather than logical. A Rv (Roll) key entry is required to continue to the next displayed value or to the next program step if it is the last value.

5-40. LOOP

NUMBER: 88

NAME: [Loop]

PARAMETER : loop number
ending step number

ASSIGNED
DEFAULT : loop number = infinite looping
ending step number = 9

DESCRIPTION : Causes the diagnostic program to loop the specified number of times. The loop procedure can only be used once per program. Otherwise [LOOP ERR] will be displayed for about one second and then the step prompt will be redisplayed. If the default loop number is used, the step prompt will not be displayed. There is no way to execute non-loop commands after the infinite loop is completed. The only way to get out of an infinite loop is by getting an error or pressing a command key.

When the ENTER key is pressed, the loop number will be prompted for by displaying [NUM=]. Up to four digits can be entered for the loop number.

If a specific loop number was entered when the ENTER key is pressed, the ending step number will be prompted for by displaying [END=]. Only one digit can be entered for the ending step number. If the ending step number is not specified, it will be set to step 9. This causes the remainder of the program to be part of the loop.

5-41. ERROR RATE TESTS

5-42. READ ONLY ERROR RATE TEST

NUMBER : 90

NAME : [READ ERT]

PARAMETER : test area number

ASSIGNED
DEFAULT : test area number - no parameter = no operation

DESCRIPTION : Runs the Read Only Error Rate Test with the test area specified. The starting address for the test needs to be specified using any of the seek commands. The error information is logged in the Error Rate Test error log.

When the ENTER key is pressed, the area will be prompted for by displaying [AREA=]. Only one digit can be entered for the test area. The number will cause one of the following messages to be displayed. If an illegal test area is specified, [ILL PARM] will be displayed for about one second. Then the test area prompt will be displayed.

The test areas are: 0 = [SECTOR]
1 = [TRACK]
2 = [CYLINDER]
3 = [SURFACE]
4 = [VOLUME]

EXAMPLE : Cause the disc drive to run the read only error rate test 20 times on cylinder 100, head 4, sector 25.

Keystrokes	Display	Remarks
	[????????]	<-- Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
6	[STEP0=6]	
1	[SEEK]	Get Seek command.
ENTER	[CYL=]	
1	[CYL=1]	
0	[CYL=10]	
0	[CYL=100]	Set cylinder to 100.
ENTER	[HEAD]	
4	[HEAD 4]	Set head to 4.
ENTER	[SECT=]	

```
2           [  SECT=2]
5           [ SECT=25]     Set sector to 25.
ENTER       [  STEP1=]
8           [ STEP1=8]
8           [  LOOP  ]     Get Loop command.
ENTER       [    NUM=]
2           [   NUM=2]
0           [  NUM=20]     Set loop number to 20.
ENTER       [    END=]     Set ending step to end.
ENTER       [  STEP2=]
9           [ STEP2=9]     Get Read Only
0           [READ ERT]     Error Rate Test.
ENTER       [   AREA=]     Set test area
0           [ SECTOR ]     to sector.
ENTER       [  STEP3=]
RUN         [  RUN   ]     Run program.
            [READ ERT] <-- Display will remain
            [  SEEK  ]     until test is
                           completed.
```

5-43. PATTERN ERROR RATE TEST

NUMBER : 91

NAME : [PATT ERT]

PARAMETERS : data source number, test area number

ASSIGNED
DEFAULTS : data source number - no parameter = no operation
test area number - no parameter = no operation

DESCRIPTION : Runs the Pattern Error Rate Test with the data source, test area and offset flag parameters specified. The default data source is not allowed. This requires the user to explicitly specify the source of the data to be written to prevent accidental writes. The starting target address for the test needs to be specified using any of the seek commands. The error information is logged in the Error Rate Test error log.

When the ENTER key is pressed, the data source will be prompted for by displaying [DATA=]. Only one digit can be entered for the data source. The number will cause one of the following messages to be displayed. If the user pattern is desired, it must be previously defined with the Data Pattern procedures or else the last data pattern will be used.

The data sources are: 0 = [PATT TBL]
1 = [USER PAT]
2 = [RND PATT]

When the ENTER key is pressed, the area will be prompted for by displaying [AREA=]. Only one digit can be entered for the test area. The number will cause one of the following messages to be displayed. If an illegal test area is specified, [ILL PARM] will be displayed for about one second. Then the test area prompt will be displayed.

The test areas are: 0 = [SECTOR]
1 = [TRACK]
2 = [CYLINDER]
3 = [SURFACE]
4 = [VOLUME]

EXAMPLE 1 : Cause the disc drive to run the Pattern Error Rate Test five times on cylinder 100 using patterns from the pattern table.

Keystrokes	Display	Remarks
	[????????]	<-- Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
6	[STEP0=6]	
1	[SEEK]	Get Seek command.
ENTER	[CYL=]	
1	[CYL=1]	
0	[CYL=10]	
0	[CYL=100]	Set cylinder to 100.
	100	
ENTER	[HEAD=]	
0	[HEAD=0]	Set head to 0.
ENTER	[SECT=]	
0	[SECT=0]	Set sector to 0.
ENTER	[STEP1=]	
8	[STEP1=8]	
8	[LOOP]	Get Loop command.
ENTER	[NUM=]	
5	[NUM=5]	Set loop number to 5.
ENTER	[END=]	Set ending step to end.
ENTER	[STEP2=]	
9	[STEP2=9]	Get Pattern Error
1	[PATT ERT]	Rate test.
ENTER	[DATA=]	Set data source to
0	[PATT TBL]	pattern table.
ENTER	[AREA=]	Set test area
2	[CYLINDER]	to cylinder.
ENTER	[STEP3=]	
RUN	[RUN]	Run program.
	[PATT ERT]	<-- Display will remain
	[SEEK]	until test is completed.

EXAMPLE 2 : Cause the disc drive to run the Pattern Error Rate Test 20 times on cylinder 100, head 4, sector 90 using a user defined pattern.

Keystrokes	Display	Remarks
	[????????]	<-- Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
7	[STEP0=7]	
3	[DATA PAT]	Get Data Pattern command.
ENTER	[PATT=%]	
4	[PATT=%4]	
2	[PATT=%42]	
1	[ATT=%421]	
0	[TT=%4210]	
4	[T=%42104]	Set data pattern.
ENTER	[STEP1=]	
6	[STEP1=6]	
1	[SEEK]	Get Seek command.
ENTER	[CYL=]	
1	[CYL=1]	
0	[CYL=10]	
0	[CYL=100]	Set cylinder to 100.
ENTER	[HEAD=]	
4	[HEAD=4]	Set head to 4.
ENTER	[SECT=]	
9	[SECT=9]	
0	[SECT=90]	Set sector to 90.
ENTER	[STEP2=]	
8	[STEP2=8]	
8	[LOOP]	Get Loop command.
ENTER	[NUM=]	
2	[NUM=2]	
0	[NUM=20]	Set loop number to 20.
ENTER	[END=]	Set ending step to end.
ENTER	[STEP3=]	
9	[STEP3=9]	Get Pattern Error
1	[PATT ERT]	Rate Test.
ENTER	[DATA=]	Set data source to
1	[USER PAT]	user pattern.
ENTER	[AREA=]	Set test area
0	[SECTOR]	to sector.
ENTER	[STEP4=]	
RUN	[RUN]	Run program.
	[PATT ERT]	<-- Display will remain
	[DATA PAT]	until test is completed.

5-44. SHORT ERROR RATE TEST

NUMBER : 92

NAME : [SHRT ERT]

PARAMETER : data source number

ASSIGNED
DEFAULT : data source number - no parameter = no operation

DESCRIPTION : Runs the Short Error Rate Test with the data source parameter specified on the entire volume. The starting target address need not be specified since the cylinders to be tested are random. The default data source is not allowed. This requires the user to explicitly specify the source of the data to be written to prevent accidental writes. The error information is logged in the Error Rate Test error log.

When the ENTER key is pressed, the data source will be prompted for by displaying [DATA=]. Only one digit can be entered for the data source. The number will cause one of the following messages to be displayed. If the user pattern is desired, it must be previously defined with the Data Pattern procedures or else the last data pattern will be used.

The data sources are: 0 = [PATT TBL]
1 = [USER PAT]
2 = [RND PATT]

EXAMPLE : Cause the disc drive to run the Short Error Rate Test three times using random patterns.

Keystrokes	Display	Remarks
	[????????]	<-- Unknown display value.
9	[???????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
8	[STEP0=8]	
8	[LOOP]	Get Loop command.
ENTER	[NUM=]	
3	[NUM=3]	Set loop number to 3.
ENTER	[END=]	Set ending step to end.
ENTER	[STEP1=]	
9	[STEP1=9]	Get Short Error
2	[SHRT ERT]	Rate Test.
ENTER	[DATA=]	Set data source to
2	[RND PATT]	random patterns.

```
ENTER       [  STEP2=]
RUN         [  RUN   ]     Run program.
            [SHRT ERT] <-- Display will remain
            [  LOOP  ]     until test is
                           completed.
```

5-45. RANDOM ERROR RATE TEST

NUMBER : 93

NAME : [RAND ERT]

PARAMETER : data source number

ASSIGNED
DEFAULT : data source number - no parameter = no operation,

DESCRIPTION : Runs the Random Error Rate Test with the data source and offset flag parameters specified on the entire volume. The default data source is not allowed. This requires the user to explicitly specify the source of the data to be written to prevent accidental writes. The starting target address need not be specified since the cylinders to be tested are random. The error information is logged in the Error Rate Test error log.

When the ENTER key is pressed, the data source will be prompted for by displaying [DATA=]. Only one digit can be entered for the data source. The number will cause one of the following messages to be displayed. If the user pattern is desired, it must be previously defined with the Data Pattern procedures or else the last data pattern will be used.

The data sources are: 0 = [PATT TBL]
1 = [USER PAT]
2 = [RND PATT]

EXAMPLE : Cause the disc drive to run the Random Error Rate Test three times using a user defined pattern.

Keystrokes	Display	Remarks
	[????????]	<-- Unknown display value.
9	[????????9]	
8	[CLEAR]	Clear diagnostic program.
ENTER	[STEP0=]	
7	[STEP0=7]	
3	[DATA PAT]	Get Data Pattern command.
ENTER	[PATT=%]	
4	[PATT=%4]	
2	[PATT=%42]	
1	[ATT=%421]	
0	[TT=%4210]	
4	[T=%42104]	Set data pattern.
ENTER	[STEP1=]	
8	[STEP1=8]	
8	[LOOP]	Get Loop command.
ENTER	[NUM=]	
3	[NUM=3]	Set loop number to 3.
ENTER	[END=]	Set ending step to end.
ENTER	[STEP2=]	
9	[STEP2=9]	Get Random Error
3	[RAND ERT]	Rate Test.
ENTER	[DATA=]	Set data source to
1	[USER PAT]	user pattern.
ENTER	[STEP3=]	
RUN	[RUN]	Run program.
	[RAND ERT]	<-- Display will remain
	[DATA PAT]	until test is completed.

5-46. RANDOM READ ONLY ERROR RATE TEST

NUMBER : 94

NAME : [RNRD ERT]

PARAMETER : none

DESCRIPTION : Runs the Random Read Only Error Rate Test on the entire volume. The starting target address need not be specified since the cylinders to be tested are random. The error information is logged in the Error Rate Test error log.

5-47. EXECUTE IMMEDIATELY UTILITIES

5-48. VELOCITY LOOP TEST

NUMBER : 95

NAME : [VEL TEST]

PARAMETER : none

DESCRIPTION : Puts the servo loop in the velocity control mode so that measurements can be made. The firmware then waits for a command key before a recalibrate is done. This exits the test.

This procedure is not programmable, that is, it will not increment the step number. This test is executed after the ENTER key is pressed rather than after the RUN key.

5-49. KEYBOARD TEST

NUMBER : 96

NAME : [KBD TEST]

PARAMETERS : none

DESCRIPTION : Executes the keyboard test. This test displays the name of the last key pressed. If an illegal key is entered because of a hardware problem, [KEY ERR] will be is displayed. The second time the END key is pressed, the procedure will exit.

This procedure is not programmable, that is, it will not increment the step number. This test is executed after the ENTER key is pressed rather than after the RUN key.

5-50. AIR PURGE

NUMBER : 97

NAME : [AIRPURGE] or [PURGE]

PARAMETER : none

DESCRIPTION : Causes the disc drive to execute the spin up sequence if the disc drive is currently unloaded. The heads will not be loaded. If the disc drive has the heads loaded, they will be unloaded. The firmware then waits for any command key. To reload the heads, cycle the LOAD/UNLOAD switch.

This procedure is not programmable, that is, it will not increment the step number. This test is executed after the ENTER key is pressed rather than after the RUN key.

NOTE : This spin up sequence only involves the spindle driver diagnostic. No other foreground diagnostics are executed.

5-51. CLEAR DIAGNOSTIC PROGRAM

NUMBER : 98

NAME : [CLEAR]

PARAMETER : none

DESCRIPTION : Resets the diagnostic program table and associated flags.

Since the diagnostic program variables are cleared, this procedure is not programmable, that is, it will not increment the step number. This test is executed after the ENTER key is pressed rather than after the RUN key.

5-52. SEEK DELAY

NUMBER : 99

NAME : [SK DELAY]

PARAMETER : seek delay time in milliseconds

ASSIGNED DEFAULT : seek delay time = 100 milliseconds

DESCRIPTION : Causes a new seek delay time to be accepted from the keyboard. When the ENTER key is pressed, the seek delay time will be prompted for by displaying [DLY=nnnn] where nnnn is the current delay value. Up to four digits can be entered for the seek delay time. This allows seek delays from 0 to 10 seconds in millisecond steps.

This procedure is not programmable, that is, it will not increment the step number. This test is executed after the ENTER key is pressed rather than after the RUN key. This allows the seek delay to be changed for the existing diagnostic program without disturbing that program.

Table 5-6. Revision Code Part Numbers

NUMBER	PART
0	ROM U-192
1	ROM U-182
2	ROM U-162
3	ROM U-152
4	ROM U-142
5	ROM U-122
6	ROM U-112

Table 5-7. Read/Write Fault Register (RWFR) Numbers

NUMBER	READ/WRITE FAULT[1]
RWFR%01	AC write current missing with write
RWFR%02	DC write current without write
RWFR%04	DC write current missing with write
RWFR%10	Multiple heads are selected

[1]Messages are bit significant; more than one bit can be set per byte.

Table 5-8. Drive Error (DERR) Numbers

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
2	During a read or verify operation, the ECC module reported an uncorrectable error. This error has priority over any CRC errors.	We have encountered a read error that was unable to be corrected by ECC.	This error can be caused by either bad media or a read/write chain fault. A test of the read/write chain should determine if hardware is at fault. If the media is bad, that location should either be avoided in future disc references or that location should be spared.
3	During a read operation, both the uncorrectable read error and a servo system off-track error were encountered.	The off-track condition is the prime suspect. Off-track can induce an uncorrectable read error.	Perform a full servo system test. If that passes successfully, then the read/write system should be tested.
4	During a read operation, the DMA hardware reported a data CRC error. If the drive has ECC, it should have caught the error. If there is no ECC in use, this is the proper reporting error for a read error.	If no ECC is present in the drive, then this error is just a "normal" read error. If ECC is present, the ECC integrated circuit is suspect.	If ECC is installed, it should be fully tested. If no ECC is in the drive, a normal read error has occurred and this error should only prompt concern if it is repeated often.
5	The CRC caught a read data error and the fault register indicates offtrack status. If ECC is present, then it is suspect as it should have caught the error before the CRC.	The off-track condition might easily have caused the read data error. Therefore the head positioning system is more suspect than the read/write system. If ECC is present in the drive, it also is highly suspect as it should have caught the error before the CRC did.	A full test of the head positioning system should be performed. If that is successful, then a read/write test should be done. Again if ECC is present, it should also be checked. 1. Head positioning system. 2. ECC (If installed). 3. DMA PCA-A6. 4. Read/write system.
6	During a drive operation that was receiving data from the host, the drive received an end of transfer before the number of bytes expected to be sent to the drive were received.	In some cases (receiving a command) the early EOI status is expected and is not an error.	The internal diagnostic should be able to find any errors associated with the EOI status. DMA PCA-A6 controls this status message.
7	During a receive or a receive and write operation, the number of bytes expected from the host was received but the last byte was not tagged with EOI.	Under normal conditions, this is a reporting error.	If this error is associated with some possible hardware problem, the DMA PCA-A6 is a good suspect.

NOTE: Some error numbers are acted on internally and may never appear on the display.

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
8	During a receive or receive and write operation, a secondary was received while expecting data or commands.	If this error is associated with a drive problem, DMA PCA-A6 could have problems. This error is a reporting error and does not mean that there are any hardware problems.	If a drive problem seems to exist, DMA PCA-A6 is a likely suspect.
9	An incremental seek was requested that would extend beyond the last track of this drive.	RAM/ROM failure.	Microprocessor PCA-A4.
10	During a verify operation, the ECC module reported an uncorrectable sector.	This is a reporting error and does not mean that the drive is not operational.	If a hardware problem is associated with this error Read/Write PCA-A10 and then ECC electronics (DMA PCA-A6) should be checked out.
11	During a seek position verify operation, the disc drive experienced more offtrack conditions than are allowable.	Head positioning system.	Check out head positioning system electronics. All portions of the system are suspect. 1. Servo PCA-A3. 2. Track Follower PCA-A9. 3. Media. 4. Actuator Driver PCA-A2. 5. Carriage mechanics.
13	During verify after a seek, comparison of logical and physical spare sector numbers did not compare.	DMA header RAM may be bad.	DMA PCA-A6
14	When a check was made of the header read from the disc, the first byte (status) had the most significant bit clear. This bit should always be set.	The read/write system is suspect.	A full self-test should be performed on the read/write system. 1. Read/Write PCA-A10 and Formatter/Separator PCA-A8. 2. DMA PCA-A6.
15	When a check was made of the sector header read from the head, the head number was not the one expected.	The read/write system is suspect.	A full self-test on the read/write system should be performed. 1. Read/Write PCA-A10 and Formatter/Separator PCA-A8 (especially head select). 2. DMA PCA-A6.
16	When a check was made of the sector header read from the disc, the sector number was not legal.	The read/write chain is suspect.	A full self-test on the read/write chain should be performed. 1. Read/Write PCA-A10, Formatter/Separator PCA-A8

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
17	When a check was made of the sector header read from the disc, the cylinder number was not the one expected.	The read/write system and the head position system are suspect.	A full self-test should be performed on both the read/write system and the head positioning system. 1. Read/Write PCA-A10, Formatter/Separator PCA-A8. 2. DMA PCA-A6. 3. Servo PCA-A3, Track Follower PCA-A9. 4. Media.
18	DMA Status indicates that the DMA buffer is full of data. The DMA buffer is held clear during this operation, so the DMA should never report a full buffer.	DMA PCA-A6 may have a hardware failure.	A full self test should be performed on DMA PCA-A6.
19	Formatter/Separator PCA-A8 or ECC electronics (DMA PCA-A6) sent a FUNER-L or UNER-L signal to the DMA electronics. If the ECC has sent the status bit, the error would be an uncorrectable error.	Read/write chain.	Read/write chain.
20	This error is the same as DERR 19 except that the head positioning system electronics also reported an off track error.	The fact that the disc drive went off track could have caused the formatter/separator error.	If a hardware problems seems to be associated with this error, the head positioning system electronics should be checked out.
21	During a DMA buffer write to the disc, a rotational latency was invoked. Since during a buffered write, all the data is already in the DMA RAM so this error would indicate that DMA PCA-A6 is faulty as it is the hardware that indicates such an error.	The circuitry on the DMA that senses the availability of data for a write operation would appear to be bad.	A full self test should be performed on DMA PCA-A6. 1. DMA PCA-A6. 2. Read/Write PCA-A10, Formatter/Separator PCA-A8. 3. Microprocessor PCA-A4.
23	All maintenance copies were searched without finding a valid copy during an access of the system maintenance area. Note that this error, if caused by a read/write problem, will require either a maintenance track format of the current media, or new media. It is possibly recoverable if caused by a head positioning system failure.	The drive has been unable to access a valid copy of a system maintenance file. This could be because seeks to the various copies were unable to be completed or that the read/write chain encountered errors that caused the drive to spare out all its possible copies of the maintenance file. Note that maintenance track sparing is NOT related to the CS/80 Spare command and proceeds without host intervention.	A full self test should be performed on the read/write system and then the head positioning system. 1. Read/Write PCA-A10, Formatter/Separator PCA-A8. 2. DMA PCA-A6. 3. Servo PCA-A3, Track Follower PCA-A9, Actuator Driver PCA-A2. 4. Microprocessor PCA-A4. 5. Media.

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
24	During an access to the spare track table file on the system maintenance area, an invalid check byte was found.	The drive read in a maintenance file that had an invalid checkword. This had to be caused by a read/write failure, an uncorrectable read error, or bad media.	A full self test should be performed on the read/write system. If the read/write system is operating, possibly a write failure occurred, or the media is bad. An Initialize Media (retaining no spares) is suggested. If that does not solve the problem, the media should be replaced. 1. Read/Write PCA-A10, Formatter/Separator PCA-A8. 2. DMA PCA-A6. 3. Media module. 4. Microprocessor PCA-A4.
27	A seek was unable to successfully reach the target track. The actual reason for the failure will be recorded in immediately previous logged DERR's if logging is enabled (other than a internal drive system seek).	Since an inability to successfully read from the target track in order to verify position can also trigger this fault, both the head positioning system and the read/write system are suspect.	A full self-test should be performed on both the head position system and the read/write system. 1. Servo PCA-A3, Track Follower PCA-A9, Actuator Driver PCA-A2. 2. Read/Write PCA-A10, Formatter/Separator PCA-A8. 3. DMA PCA-A6.
28	During an access to the interleave value sector on the system maintenance area, an invalid check byte was found.	The drive read in a maintenance file that had an invalid checkword. This had to be caused by a read/write failure, an uncorrectable read error, or bad media.	A full self test should be performed on the read/write system. If the read/write system is operating, possibly a write failure occurred, or the media is bad. An Initialize Media (retaining no spares) is suggested. If that does not solve the problem, the media should be replaced. 1. Read/Write PCA-A10, Formatter/Separator PCA-A8. 2. DMA PCA-A6. 3. Media module. 4. Microprocessor PCA-A4.
29	A physical head position recalibration operation was unable to successfully attain the normal recal position. This error will prompt a head unload operation. Immediately prior DERR's will elaborate on the cause of the failure if fault logging is enabled (if the recal is not part of a internal drive system operation).	The head positioning system is suspect.	A full self-test should be performed on the head positioning system. 1. Servo PCA-A3. 2. Track Follower PCA-A9. 3. Actuator Driver PCA-A2.

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
30	A head unload operation failed and was forced to perform an emergency retract.	The head positioning system is suspect.	A full head positioning system test should be performed. 1. Servo PCA-A3, Track Follower PCA-A9. 2. Actuator Mechanism. 3. Media.
31	The carriage back indicator did not indicate that the heads were fully unloaded after an emergency retract was attempted.	Either the head positioning system is bad, the drive actuator mechanics are faulty, or the carriage back indicator is bad.	First the drive actuator mechanics should be inspected to check any gross failures such as a stuck carriage. Remember that since this error occurred, that heads could still be over the discs, so caution is advised. Next, if the mechanics appear to be functional, a full head positioning system self-test should be performed. 1. Actuator Driver PCA-A2. 2. Drive actuator mechanics. 3. Carriage back indicator on Actuator Status PCA-A18. 4. Cable W1 from Actuator Status PCA-A18 to Servo PCA-A3. 5. Servo PCA-A3.
32	At the end of a read operation, no data errors were indicated by the hardware, but at some time since the last seek operation, the drive has gone off track. The data read is considered to be valid.	This error is an information error only.	If there are hardware problems associated with this error, the head positioning system electronics should be checked out.
33	During a disc read or write operation, the target sector was passed because there was either no room in the DMA buffer for the sector to be read or there was not a sector worth of information in the DMA buffer to be written to the disc. With RPS enabled on a write operation, the error could mean that the RPS window was missed. Otherwise, during a write operation, DERR 33 means at least one sector was written to the disc and the latency was induced by a subsequent sector write.	None	None

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
34	The ECC electronics reported a correctable error during a read or verify.	This error is an information error only.	If this error is associated with hardware problems, the ECC electronics on DMA PCA-A6 should be checked out.
35	The error log (on disc) is full (it contains 101 entries).	Might be an indication of a severely increasing error rate.	Read/write system, media.
36	The (disc) fault log is full (contains 65 entries).	Might be an indication of more frequent drive faults.	All hardware.
48	During a read operation, the header of each sector is checked for the proper address information. This error signifies that the first byte of that sector's header (status byte) did not have the most significant bit set as required in all sectors.	The read/write system is suspect as that bit should always be set in all sectors.	A full self-test should be performed on the read/write system. 1. Read/Write PCA-A10, Formatter/Separator PCA-A8. 2. DMA PCA-A6. 3. Media
49	During a read operation, the header of each sector is checked for the proper address information. This error signifies that the sector number read from the disc did not correspond to the number that the drive was attempting to read.	A full self-test should be performed on the read/write system. Also the counter integrated circuit that functions as a sector counter on Microprocessor PCA-A4 could be faulty, so a microprocessor self-test should also be performed.	Full self-tests on both the read/write system and the microprocessor should be performed. 1. Read/Write PCA-A10, Formatter/Separator PCA-A8. 2. DMA PCA-A6. 3. Microprocessor PCA-A4. 4. Sector timing generation circuitry Track Follower PCA-A9. 5. Media.
50	During read operation, the header of each sector is checked for the proper address information. This error signifies that the head number read from the disc did not correspond to the number that the drive was attempting to read.	A full self-test should be performed on the read/write system. The head selection circuitry on Read/Write PCA-A10 is especially suspect as no data error was reported for that sector.	A full self-test should be performed on the read/write system. 1. Read/Write PCA-A10, Formatter/Separator PCA-A8. 2. DMA PCA-A6. 3. Media.
51	During a read operation, the header of each sector is checked for the proper address information. This error signifies that the cylinder number read from the disc did not correspond to the number that the drive was attempting to read.	The read/write system and the head positioning system could possibly cause this problem. Since no data error was reported for the sector, we most likely at some point were over the wrong track when we wrote the track or the DMA header RAM was faulty and the wrong cylinder number was passed to the read/write system.	A full self-test should be performed on the read/write system, the DMA PCA-A6, and the head positioning system. 1. Read/Write PCA-A10, Formatter/Separator PCA-A8. 2. DMA PCA-A6. 3. Servo PCA-A3. 4. Track Follower PCA-A9. 5. Actuator Driver PCA-A2. 6. Media.

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
52	During run time, greater than four correctable errors (single read retries to correct data) occurred in 64K sectors transferred.	Faulty data head cable is most frequent cause.	1. Data head cable open. 2. Read/write system, media. 3. Servo runout (media seating). 4. Servo system.
59	During an access of a head alignment band, the phase locked loop of the automatic head alignment circuitry on Read/Write PCA-A10 was unable to phase lock on the servo code.	Either the heads are not currently over the alignment band as thought, the head alignment circuitry on Read/Write PCA-A10 is faulty, or the servo code on the alignment band is bad.	A full self-test should be performed on Read/Write PCA-A10. Next the system should be checked out. After that the signal from the alignment band in question should be analyzed for defects. 1. Read/Write PCA-A10. 2. Head positioning system. 3. Media alignment band.
60	During an access of a head alignment band, the automatic head alignment circuitry on Read/Write PCA-A10 was unable to establish good automatic gain control (AGC) on the alignment band's servo code.	Either the heads are not currently over the alignment band as thought, the head alignment circuitry on Read/Write PCA-A10 is faulty, or the servo code on the alignment band is bad.	A full self-test should be performed on Read/Write PCA-A10. Next the head positioning system should be checked out. After that the signal from the alignment band in question should be analyzed for defects. 1. Read/Write PCA-A10. 2. Head positioning system. 3. Media alignment band.
61	During an access of a head alignment band, the automatic head alignment circuitry on Read/Write PCA-A10 was unable to perform a measurement of the circumferential sector skew.	Either the heads are not currently over the alignment band as thought, the skew measurement circuitry on the track follower is faulty, or the servo code on the alignment band is bad.	A,full self-test should be performed on Track Follower PCA-A9. Next the head positioning system should be checked out. After that the signal from the alignment band in question should be analyzed for defects. 1. Track Follower PCA-A9. 2. Head positioning system. 3. Media alignment band.
63	During an attempt to determine the radial offset for a particular alignment band, we were unable to correct for the observed offset within the required accuracy. Note that we iteratively zero in on the proper offset, so this fault means that the system of alignment is not acting deterministically.	Either the heads are not currently over the alignment band as thought, the position signal from the automatic head alignment circuitry on Read/Write PCA-A10 is bad, the analog-to-digital convertor on Microprocessor PCA-A4 is faulty, or the servo code on the alignment band is bad.	Full self-tests should be performed on the Read/Write PCA-A10, Track Follower PCA-A9, Microprocessor PCA-A4, and the full head positioning system. If all perform well, the servo code on that alignment band should be analyzed for defects. 1. Read/Write PCA-A10. 2. Track Follower PCA-A9. 3. Microprocessor PCA-A4. 4. Head positioning system. 5. Media alignment band.

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
64	During a disc read or write operation the drive detected an unexpected hardware fault register bit set. This means that some hardware was indicating to the microprocessor that a hardware fault had occurred.	After this entry in the fault log, the contents of the fault register that prompted this error is recorded. The contents of that byte should indicate which board is in error. Note that a servo system off-track condition can trigger several read/write faults. Also speed-down will trigger emergency retract and virtually all the other faults.	Suspected hardware is indicated in the contents of the hardware fault register. 1. Indicated PCA due to the hardware fault register. 2. Microprocessor PCA-A4.
70	An excessive amount of disc runout was encountered during radial offset measurement.	Either poor mounting of the media module on the spindle or the automatic head alignment circuitry on Read/Write PCA-A10 is faulty.	1. Media module spindle mounting. 2. Read/Write PCA-A10, automatic head alignment circuitry.
71	During head load, the track follower did not acquire AGC indicating that the guard band had been reached within the proper time.	Either Track Follower PCA-A9 cannot detect the guard band or the head positioning system is much slower than allowable.	1. Track Follower PCA-A9. 2. Servo Head - unable to "read". 3. Head positioning system (Servo PCA-A3, Actuator Driver PCA-A2, or Actuator Status PCA-A18).
73	During a head load, the actuator appeared to move (loss of carriage back) before a velocity command was sent to the servo.	Offsets in the servo-actuator driver, a faulty carriage back indication, or a faulty carriage back latch.	1. Servo PCA-A3. 2. Actuator Driver PCA-A2. 3. Actuator Status PCA-A18. 4. Carriage back latch assembly.
74	During a head load, we did not lose carriage back after a velocity command was sent to the servo.	Faulty carriage back latch, Actuator Driver PCA-A2 not driving the actuator, or a faulty Servo PCA-A3. It would be wise to check all connecting cables.	1. Actuator Status PCA-A18. 2. Actuator Driver PCA-A2. 3. Servo PCA-A3. 4. Carriage assembly. 5. Carriage back latch assembly.
75	During a head load, the output of the velocity tachometer indicates either a too slow or too fast velocity.	The head positioning system may be driven to saturation or the tachometer may not be connected or functional.	1. Actuator Status PCA-A18. 2. Actuator Driver PCA-A2. 3. Servo PCA-A3. 4. Velocity transducer coil. 5. Tachometer rod.
76	During a radial offset measurement, the offset for the current head exceeded the maximum allowable quarter-track offset.	The head alignment circuitry on Read/Write PCA-A3, the A/D convertor on Microprocessor PCA-A4, a poorly manually aligned head, or a carriage mechanical discrepancy. Note: If all data heads exhibit excess offset, the servo head is probably mis-aligned.	1. Read/Write PCA-A10. 2. Microprocessor PCA-A4. 3. Heads (data, servo). 4. Carriage assembly (including cleanliness of rails).

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
77	During a head load or recalibrate, the landing track's track center detect was not found in the allowed time. Note that both track follower, AGC and sync had been successful prior to this.	The track center detect (TCD) circuitry on Servo PCA-A3 or the speed of the entire head positioning system.	Servo PCA-A3.
78	Current operation blocked by existing error condition.	Previous error.	Determined by previous failure(s).
79	During a head load or recall, Track Follower PCA-A9 did not acquire sector sync as expected.	The sync circuitry on Track Follower PCA-A9, media module servo code.	1. Track Follower PCA-A9. 2. Media module.
80	During a head load or a recall, we were unable to gain AGC on the track follower in the time period in which we should have encountered the outer guard band servo code.	The track follower, the pack's servo code or the servo head.	1. Track Follower PCA-A9. 2. Servo head. 3. Media module.
81	During a recalibrate, AGC on Track Follower PCA-A9 was either lost prior to the operation or after slewing off the disc, we were unable to detect the loss of AGC which indicates that we are off the servo code.	The track follower or the media module servo code appear to be non-functional.	1. Track Follower PCA-A9. 2. Servo head. 3. Media module.
82	During a recalibrate, the disc drive slews off the disc while waiting for the absense of track center detects that would signal arrival in the outer guard band, This error indicates that this event did not occur in the allowable time.	The position signal from Track Follower PCA-A9, the TCD circuitry on the servo, or the servo code would be suspect. Also the entire velocity servo system might be very slow.	A test of the entire head positioning system is suggested.
83	During a seek of greater than 32 tracks, Microprocessor PCA-A4 monitors a deceleration bit on Servo PCA-A3. If the acceleratin period lasts past a distance proportional timeout, it is assumed there is an acceleration period error.	The suspect circuitry would be the distance-to-go (DTG) register and the TCD counter on Servo PCA-A3 as well as the media module servo code and Track Follower PCA-A2.	1. Servo PCA-A3. 2. Media module. 3. Track Follower PCA-A9. (NOTE: If the Fast Position (FPOS) signal is too low, this error will occur on all "long" seeks.)

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
84	During a seek, there is a length proportional time-out done until the Distance-To-Go (DTG) register indicates that the heads are within 3/4 track of the destination. If this does not occur within the timeout, this error is generated.	The DTG and track crossing detector circuitry on Servo PCA-A3 is suspect as well as a drop-out of the servo code caused by the media module or Track Follower PCA-A9.	1. Servo PCA-A3. 2. Media module servo code. 3. Track Follower PCA-A9.
85	At the end of a seek the head positioning system switches to approach velocity after reaching within 3/4 track of destination. It then monitors the time until the first track center detect (widened due to position enable off) caused by coming "into" the target track. This error is generated by that period being too long.	The TCD circuitry on Servo PCA-A3 is suspect as well as the media module servo code and Track Follower PCA-A9. Note: A full head positioning system self-test should be run.	1. Servo PCA-A3. 2. Media module code. 3. Track Follower PCA-A9. 4. Linear actuator assembly. 5. Tachometer system 6. Mis-aligned mechanics (carriage, crash stops, etc.).
86	During the final settling on track after enabling position control we were unable to maintain an on-track condition for the required time period.	The head positioning system was unable to maintain track position.	All portions of the head positioning system. 1. Servo PCA-A3. 2. Track Follower PCA-A9. 3. Linear actuator. 4. Carriage assembly.
87	During a head unload, a time-out is performed to wait for the carriage back flag from Actuator Status PCA-A18. This error is generated by the elapsing of the time-out before carriage back is indicated.	The entire head positioning system as well as the carriage back indicator on Actuator Status PCA-A8 is suspect. Also the mechanical state of the carriage assembly could be bad.	1. Actuator Status PCA-A18. 2. Servo PCA-A3. 3. Actuator Driver PCA-A2. 4. Carriage assembly.
88	During a seek velocity calibration, the controller looks for certain numbers in the servo's Distance-To-Go (DTG) register. The time period between two of these numbers is used to calibrate the seek velocity. This error is caused if one of those two numbers was not found within the prescribed time-out.	The probable cause of this error is either the DTG miscounting on the servo, the track follower losing position information, or the microprocessor-servo interface being faulty.	A full servo system internal diagnostic should be performed. 1. Servo PCA-A3. 2. Track Follower PCA-A9. 3. Microprocessor PCA-A4. 4. Media module and/or servo head.

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
89	During seeks greater than 32 tracks, a test of the actuator temperature is made just after the seek movement is initiated. This information is used to determine if the head positioning system should switch to the "slow" seek velocity to prevent overheating of the actuator. This error is when that temperature exceeds the allowable for safe operation.	Poor cooling of actuator due to poor air flow or excessive ambient temperature. Note: Above a certain temperature (120 degrees C) long seeks are slowed to reduce the possibilities of over heating, therefore this error is not to be expected in "normal" operation.	Note: A head positioning system test should be performed. 1. Actuator mechanics thermistor on coil. 2. Actuator Driver PCA-A2. 3. Cable between Servo PCA-A3 and Actuator Status PCA-A18. 4. Cable between Actuator Status PCA-A18 and the actuator assembly.
90	A spare operation retaining data was unable to seek the target track.	It is advised that a full internal diagnostic be performed before any sparing operation to ensure that the disc drive has not lost its ability to seek and read/write. This error may be the reason why sparing was envoked originally.	Tests of the head positioning system and read/write system are suggested.
91	A spare operation retaining data was unable to read all of the data from the target track.	It is advised that a full internal diagnostic be performed before any sparing operation to ensure that the ability to read/write has not been lost. This error may be the reason the sparing operation was envoked originally.	A test of the read/write chain is suggested.
92	A sparing operation was unable to seek to either of the two closest available spare tracks to be used in that operation.	A full internal diagnostic is recommended before any sparing operation. This error would seem to indicate that perhaps a full cylinder of available spare tracks is defective or that the drive can no longer seek.	Tests of the head positioning system and read/write system are suggested.
93	A sparing operation was unable to write the available spare track and successfully verify it.	A full internal diagnostic is recommended before any sparing operation. This error would seem to indicate that either a full cylinder of available spare tracks was defective or that the disc drive can no longer read/write.	A test of the read/write system is suggested.
94	An error was detected in the logical head load routine from the physical head load driver.	Head positioning system.	Head positioning system.

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
96	The CTC did not decrement or reload after the time for one sector.	This problem can originate from anywhere along the sector timing pulse data path.	Any hardware involved with the generation or propagation of the sector timing pulse signal to Microprocessor PCA-A4 including Microprocessor PCA-A4.
97	When the firmware has decided that the disc write operation is complete, it checks the DMA, since in the case of a receive and write operation, the DMA should stop in parallel with the firmware. In the case of a buffer write (write from DMA buffer), the error is not possible since the DMA is NOT currently receiving data from the channel during such a write.	DMA PCA-A6 and channel circuitry.	The DMA microdiagnostic should locate the problem on DMA PCA-A6.
98	A fault bit was detected on the DMA that should never be set for this drive.	The DMA PCA-A6 is highly suspect and the DMA internal diagnostic should be performed on that board.	1. DMA PCA-A6. 2. Microprocessor PCA-A4.
99	The ECC chip experienced a data compare error from the watch-dog linear shift register during a disc write operation.	The ECC chip appears to have an internal fault. Any further disc writes before this fault is investigated is highly suspect.	DMA PCA-A6
100	An attempt was made to reset the ECC chip, but the error status bit associated with that circuitry does not toggle.	Either the ECC circuitry is defective or microprocessor PCA-A4 cannot select the ECC chip.	1. DMA PCA-A6. 2. Microprocessor PCA-A4.
102	The DMA electronics set a bit that indicates the end of a transfer (HWTAF-H) before the expected termination of the tranfer.	Either the DMA PCA-A6 circuitry that monitors for the end of a transfer is faulty, or the microprocessor's ability to sense these bits is faulty.	A full internal diagnostic should be performed. 1. DMA PCA-A6. 2. Microprocessor PCA-A4.
103	During a disc read or write, the target sector for an operation is determined by comparing the controller's target sector number and the sector counter found in the microprocessor PCA's Counter-Timer Chip (CTC). This error indicates that the desired sector number did not appear from the CTC within a full disc rotation.	Either the CTC is not counting (perhaps due to either the CTC circuitry being in fault, or the sector timing circuitry that generates the sector pulses is failing) or there has been a controller fault that caused us to be looking for an illegal sector number.	A full internal diagnostic of the drive should be performed. 1. Microprocessor PCA-A4. 2. Track Follower PCA-A9.

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
104	During a data transfer using the 4K static memory, a double-bit error was detected.	Either the 4K static RAM on the Cache PCA has a double-bit error or the error detection circuitry on the CDMA PCA is faulty.	1. Cache PCA-A5. 2. CDMA PCA-A6.
105	The analog-to-digital converter (ADC) has a bit that should be set at the end of the conversion (EOC). This error is caused by that bit not being set at the end of a conversion.	The circuitry associated with the ADC on Microprocessor PCA-A4 appears to be bad.	A full self-test should be performed on Microprocessor PCA-A4.
106	During a write operation, a CRC error was detected.	DMA failure.	DMA PCA-A6.
107	Inconsistent internal error code(s) encountered by error reporting routine.	ROM failure.	Microprocessor PCA-A4.
108	During a period in which the disc drive is waiting for the sector counter (STP register) to reach an expected value, it was noted that the STP was counting at a faster rate than is possible for the disc drive.	The STP circuitry (it is a channel of the counter-timer (CTC) integrated circuit on Microprocessor PCA-A4 or the circuitry generating sector timing pulses (Track Follower PCA-A9) is bad.	A full self-test should be performed on the head positioning system and Microprocessor PCA-A4. 1. Microprocessor PCA-A4. 2. STP pulse generating circuitry (Track Follower PCA-A9).
109	A hard double-bit error was detected in the 1-Mbyte cache DRAM array. This error disables cache and prompts the operator message "NO CACH".	Either 1-Mbyte DRAM array on Cache PCA-A5 or error detection circuitry on CDMA PCA-A6 is faulty.	1. Cache PCA-A5. 2. CDMA PCA-A6.
110	A double-bit error was detected in the 1-Mbyte cache DRAM array while doing a host transfer-out (3 occurrences = DERR 109).	Either 1-Mbyte DRAM array on Cache PCA-A5 or error detection circuitry on CDMA PCA-A6 is faulty.	1. Cache PCA-A5. 2. CDMA PCA-A6.
111	A microdiagnostic failed that refers to the controller unit as opposed to one of the mass storage units.	As the associated test error (TERR) describes.	As the associated test error (TERR) describes.
113	The device received a channel independent clear directed to unit 0 or 1.	Not a fault - internal error only.	None
114	A channel parity error has been detected by the channel interface, an illegal channel interface state (caused by receiving bus control, DMA handshake error with channel), or channel loopback failure.	The error could be caused by a faulty channel or a fault in the DMA channel interface. This error could also be caused by faulty system configuration or operation.	1. DMA PCA-A6. 2. Host System: a. Channel cabling. b. Channel configuration. c. Host Channel Interface.

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
115	The device received a message type which conflicted with its current state.	Internal error only. The host is out of sync with the state of the drive, or channel experienced a transmission error.	1. HP-IB cables. 2. DMA PCA-A6.
118	Channel activity has placed the device interface in an illegal state.	Host software placed the device in an illegal state, or DMA hardware is improperly communicating with the interface chip.	1. DMA PCA-A6. 2. System configuration problem.
119	The actual length (in bytes) of an HP-IB message conflicted with the expected length.	Internal error only - possible transmission problem.	This error could be the result of a HP-IB configuration problem.
121	An HP-IB message was abnormally terminated.	Internal error only - not a fault.	None
122	The device received a cancel command.	Internal error only - not a fault.	None
128	The CPU sent an illegal opcode to the device.	Internal error only - possible transmission problem.	1. HP-IB cables. 2. DMA PCA-A6.
129	The CPU sent a unit or volume number which was out of bounds for this device.	Internal error only - possible transmission problem.	1. HP-IB cable. 2. DMA PCA-A6.
130	The CPU sent a command which did not have the correct number of parameter bytes for the opcode(s) included.	Internal error only - possible transmission problem.	1. HP-IB cables. 2. DMA PCA-A6.
136	An internal diagnostic failed. Look at test error (TERR) to ascertain which one failed.	Determined by test error (TERR).	Determined by test error (TERR).
137	The current request was aborted due to a lack of valid head alignment information. The aborted operation was most likely a write operation since reads and seeks are allowed without valid head alignment, but not disc writes.	This error was caused by an aborted head alignment operation due to a fault, or if the request for head alignment was triggered by an internally detected pack temperature change, and our request for release was denied by the host system.	A full internal diagnostic should be performed. This will test our ability to perform head alignment. Secondly, ensure that the host system was not ignoring our request for release. 1. Read/Write PCA-A10. 2. Media Module. 3. Microprocessor PCA-A4.
139	PHI parallel poll synchronization problem was experienced by the CPU, or the CPU tried to talk to the drive while it was automatically released.	Internal error only - not a fault.	None
146	No more spares are available for a requested sparing operation.	Internal error only.	Media is getting too old, or has been damaged, or read/write system electronics have degraded.

Table 5-8. Drive Error (DERR) Numbers (continued)

NO.	CAUSE	POSSIBLE FAULT	SUSPECTED HARDWARE
148	Retry attempts have failed to rectify a data error during a read operation.	Internal error only - not a fault.	None
149	An internal event has occurred, which requires a release sequence for servicing.	Internal error only - not a fault.	None
225	A parameter bounds error occurred in a set address command.	Internal error only - possible transmission error.	1. HP-IB cables. 2. DMA PCA-A6.
226	A parameter bounds error occurred in a command other than unit, volume, or address.	Internal error only - possible transmission error.	1. HP-IB cables. 2. DMA PCA-A6.
230	The drive is in a condition such that it is unable to perform the command (such as unloaded or an error condition).	Almost anything in the drive. Perform a full diagnostic. Possible cause is any momentary (lightning, power surge) or hardware fault.	1. Read/write chain. 2. Servo chain.
231	WARNING, the number of available spare tracks is low.	The media module has too many defects or the servo and read/write systems cause too many unrecoverable errors.	1. Media module. 2. Read/write chain. 3. Servo chain.

Table 5-9. Test Error (TERR) Numbers

NO.	CAUSE	SUSPECTED HARDWARE
1	During the microprocessor test (Test 6), a data pattern is written to and read from the control register and an incorrect bit is found.	Microprocessor PCA-A4.
2	During the microprocessor test (Test 6), a data pattern is written to and read from the CTC for each of the 4 channels, and for one of the channels a bit error is found.	Microprocessor PCA-A4.
3	During the microprocessor test (Test 6), different data is written to each of the CTC channels and read back. One of the channels is incorrectly accessed.	Microprocessor PCA-A4.
4	During the microprocessor test (Test 6), each CTC channel is set to timer mode, internally triggered, and allowed to count. An incorrect count value is found in one of the channels.	Microp ocessor PCA-A4.
5	During the microprocessor test (Test 6), the CTC channels 0 to 2 are cascaded and allowed to count. An incorrect count value is found in one of the channels.	Microprocessor PCA-A4.
6	During the microprocessor test (Test 6), the 4 CTC channels are each configured in timer mode with interrupts enabled. Upon interrupt, the wrong channel interrupt vector is received for one of the channels.	Microprocessor PCA-A4.
7	During the microprocessor test (Test 6), the 4 CTC channels are each configured in timer mode with interrupts enabled. Upon interrupt, no interrupt vector is received for one of the channels.	Microprocessor PCA-A4.
8	During the microprocessor test (Test 6), the 4 CTC channels are each configured in timer mode with interrupts enabled. In the allotted time, one of the channels did not request an interrupt.	Microprocessor PCA-A4.
9	During the microprocessor test (Test 6), the frequency divider circuit, which generates the 540 Hz signal, is found to be out of specification.	Microprocessor PCA-A4.
10	During the microprocessor test (Test 6), one of bits 5 to 7 of the microprocessor sense register is in error.	Microprocessor PCA-A4.
11	During the microprocessor test (Test 6), a fault is found in the address selection of the fault register and the sense register.	Microprocessor PCA-A4.
12	During the microprocessor test (Test 6), bits 0 through 2 of the microprocessor sense register has the wrong value. These bits are bits 0 through 2, respectively, of motherboard PCA-A11 address bus.	Any of the PCA's connected to the data bus: Actuator Driver PCA-A2. Servo PCA-A3. Microprocessor PCA-A4. DMA PCA-A6. Formatter/Separator PCA-A8. Track Follower PCA-A9. Motherboard PCA-A11. Spindle Driver PCA-A12.

NOTE: Some error numbers are acted on internally and may never appear on the display.

Table 5-9. Test Error (TERR) Numbers (continued)

NO.	CAUSE	SUSPECTED HARDWARE
13	During the microprocessor test (Test 6), the power supply fault bit is set in the fault register.	1. Regulator PCA-A1. 2. Microprocessor PCA-A4.
14	During the microprocessor test (Test 6), an error is detected in the motherboard data bus when testing a 256-byte block of space.	Any of the PCA's connected to the data bus: Actuator Driver PCA-A2. Servo PCA-A3. Microprocessor PCA-A4. DMA PCA-A6. Formatter/Separator PCA-A8 Track Follower PCA-A9. Motherboard PCA-A11. Spindle Driver PCA-A12.
15	During the microprocessor test (Test 6), one or more of the motherboard data bus bits is stuck low when testing a 256-byte block of address space.	Any of the PCA's connected to the data bus: Actuator Driver PCA-A2. Servo PCA-A3. Microprocessor PCA-A4. DMA PCA-A6. Formatter/Separator PCA-A8. Track Follower PCA-A9. Motherboard PCA-A11. Spindle Driver PCA-A12.
16	During the microprocessor test (Test 6), a data bus contention or failure occurred on the motherboard data bus.	Any of the PCA's connected to the data bus: Actuator Driver PCA-A2. Servo PCA-A3. Microprocessor PCA-A4. DMA PCA-A6. Formatter/Separator PCA-A8. Track Follower PCA-A9. Motherboard PCA-A11. Spindle Driver PCA-A12.
17	During the microprocessor test (Test 6), the end of A/D conversion flag is never received.	Microprocessor PCA-A4.
18	During the microprocessor test (Test 6), either the ground input or reference voltage input of the A/D circuit is found to be out of specification after an A/D conversion.	Microprocessor PCA-A4.
19	During the microprocessor test (Test 6), the +12 Vdc reference voltage input is out of specification.	1. Regulator PCA-A1. 2. Microprocessor PCA-A4.
20	During the microprocessor test (Test 6), the -12 Vdc reference voltage input is out of specification.	1. Regulator PCA-A1. 2. Microprocessor PCA-A4.
21	During the Track Follower interface test (Test 32), the SOS-L line driven from the Track Follower failed to increment the CTC.	Microprocessor PCA-A4.
24	During an access to the spare track table file on the system maintenance area, an invalid check byte is found.	1. Read/Write PCA-A10, Formatter/Separator PCA-A8. 2. DMA PCA-A6. 3. Media Module.
28	During an access to the interleave value sector on the system maintenance area, an invalid check byte is found.	1. Read/Write PCA-A10, Formatter/Separator PCA-A8. 2. DMA PCA-A6. 3. Media Module.

Table 5-9. Test Error (TERR) Numbers (continued)

NO.	CAUSE	SUSPECTED HARDWARE
32	During the Regulator test (Test 7), the Regulator fault register contains a wrong value for -20V and -12V.	1. DC Power PCA-A13. 2. Regulator PCA-A1.
33	During the Regulator Test (Test 7), the Regulator fault register contains wrong values for positive voltages.	Regulator PCA-A1
34	During the Regulator test (Test 7), bits 5, 6, and 7 of the Regulator fault register did not compare to predefined values.	Regulator PCA-A1.
35	During the Spindle Driver test (Test 13), all fuse bits have the wrong value.	1. DC Power PCA-A13. 2. Spindle Driver PCA-A12.
36	During the Spindle Driver test (Test 13), an unexpected combination of fuse bits are missing.	Spindle Driver PCA-A12 and fuses.
37	During the Spindle Driver test (Test 13), all fuse status bits are present except the actuator plus supply fuse bit.	Spindle Driver PCA-A12 and fuse F540.
38	During the Spindle Driver test (Test 13), all fuse status bits are present except the actuator minus supply fuse bit.	Spindle Driver PCA-A12 and fuse F550.
39	During the Spindle Driver test (Test 13), all fuse status bits are present except the spindle plus supply fuse bit.	Spindle Driver PCA-A12 and fuse F590.
40	During the Spindle Driver test (Test 13), all fuse status bits are present except the spindle minus supply fuse bit.	Spindle Driver PCA-A12 and fuse F580.
41	During the Spindle Driver test (Test 13), all fuse status bits are present except both actuator supply fuse bits.	Spindle Driver PCA-A12 and fuses F540/F550.
42	During the Spindle Driver test (Test 13), all fuse status bits are present except both spindle supply fuse bits.	Spindle Driver PCA-A12 and fuses F580/F590.
43	During the Spindle Driver test (Test 13), all fuse status bits are present except both plus supply fuse bits.	Spindle Driver PCA-A12 and fuses F540/F590.
44	During the Spindle Driver test (Test 13), all fuse status bits are present except both minus supply fuse bits.	Spindle Driver PCA-A12 and fuses F550/F580.
48	During the SOS-L signal test (Test 23), the Formatter/Separator read the wrong value from the Track Follower.	Track/Follower PCA-A9
49	During the SOS-L signal test (Test 23), the DMA read the wrong value from the Track Follower.	DMA PCA-A6.
50	During the SOS-L signal test (Test 23), the Track Follower read the wrong value from the Formatter/Separator.	1. Track Follower PCA-A9. 2. Formatter/Separator PCA-A8. 3. DMA PCA-A6.
51	During the RWC-L signal test (Test 21), the ECC chip and DMA read the wrong value from the Formatter/Separator.	DMA PCA-A6.
52	During the RWC-L signal test (Test 21), the ECC chip, DMA and the Formatter/Separator read the wrong value from the Formatter/Separator.	1. DMA PCA-A6. 2. Formatter/Separator PCA-A8.

Table 5-9. Test Error (TERR) Numbers (continued)

NO.	CAUSE	SUSPECTED HARDWARE
53	During the RWC-L signal test (Test 21), the DMA read the wrong value from the Formatter/Separator.	1. DMA PCA-A6. 2. Formatter/Separator PCA-A8.
54	ECC chip read the wrong value (see Test 53).	DMA PCA-A6.
55	During the RWC-L signal test (Test 21), a combination of the ECC chip, DMA and the Formatter/Separator read the wrong value from the Formatter/Separator.	1. Formatter/Separator PCA-A8. 2. DMA PCA-A6.
56	During the UNER-L signal test (Test 30), two uncorrectable sectors were clocked from the Formatter/Separator, but the EROR-L bit is not set on the DMA.	1. DMA PCA-A6. 2. Formatter/Separator PCA-A8.
57	During the UNER-L signal test (Test 30), there is an error in the DMA disc address count.	DMA PCA-A6.
58	During the UNER-L signal test (Test 30), an uncorrectable sector causes the sector counter to change from 0, while EROR-L is set on the DMA.	DMA PCA-A6.
59	During the UNER-L signal test (Test 30), UNER-L did not cause EROR-L to be set. The sector counter also worked incorrectly.	DMA PCA-A6.
60	During the EOS-L signal test (Test 28), the ECC chip read the wrong value from the Formatter/Separator.	1. DMA PCA-A6. 2. Formatter/Separator PCA-A8. 3. Connecting Interface.
61	During the FOUT-H signal test (Test 26), the ECC chip read the wrong value from Formatter/Separator.	1. DMA PCA-A6. 2. Formatter/Separator PCA-A8.
62	During the FOUT-H signal test (Test 26), the Formatter/Separator or the Formatter/Separator and the ECC chip read the wrong value from the Formatter/Separator.	1. DMA PCA-A6. 2. Formatter/Separator PCA-A8.
63	During the FUNER-L signal test (Test 29), the DMA read the wrong value from the Formatter/Separator.	1. DMA PCA-A6. 2. Formatter/Separator PCA-A8.
64	During the FUNER-L signal test (Test 29) the Formatter/Separator or Formatter/Separator and DMA read the wrong value from the Formatter/Separator.	1. Formatter/Separator PCA-A8. 2. DMA PCA-A6.
65	During the SOD-L signal test (Test 22), the DMA read the wrong value from the Formatter/Separator.	1. DMA PCA-A6. 2. Formatter/Separator PCA-A8.
66	During the SOD-L signal test (Test 22), the Formatter/Separator or Formatter/Separator and DMA read the wrong value from the Formatter/Separator.	1. Formatter/Separator PCA-A8. 2 DMA PCA-A6.
67	During the DOUT-H signal test (Test 24), the ECC chip read the wrong value from the DMA.	DMA PCA-A6.
68	During the DOUT-H signal test (Test 24), the DMA or ECC chip and DMA read the wrong value from the DMA.	DMA PCA-A6.
69	During the FIN-H signal test (Test 27), the Formatter/Separator read the wrong value from the ECC chip.	1. DMA PCA-A6. 2. Formatter/Separator PCA-A8. 3. Connecting Interface.

Table 5-9. Test Error (TERR) Numbers (continued)

NO.	CAUSE	SUSPECTED HARDWARE
70	During the DIN-H signal test (Test 25), the DMA read the wrong value from the ECC chip.	DMA PCA-A6.
71	The memory failed a data write/read/compare test. Or an uncorrectable error was found in the cache dynamic RAM array.	1. Cache PCA-A5. 2. CDMA PCA-A6.
72	Failure in cache page addressing, i.e., data written to wrong page.	1. Cache PCA-A5.
73	Error in data transfer from cache memory through CDMA to disc media.	1. CDMA PCA-A6. 2. Cache PCA-A5. 3. Ribbon Cable W7.
74	Data miscompare (single-bit error) found during diagnostics while testing the 4K static RAM buffer.	1. Cache PCA-A5. 2. CDMA PCA-A6.
75	Uncorrectable error found during diagnostics testing of 4K static RAM buffer. Indicates intermittent RAM failure or Hamming error correction failure.	1. Cache PCA-A5 2. CDMA PCA-A6.
80	During the DMA test (Test 14), data written to the DMA registers could not be read.	DMA PCA-A6.
81	During the DMA test (Test 14), the DMA header RAM has a wrong value.	DMA PCA-A6.
82	During the DMA test (Test 14), the DMA data RAM has a wrong value.	DMA PCA-A6.
83	During the DMA test (Test 14), the DMA DATF has a wrong value.	1. DMA PCA-A6. 2 Read/Write Chain.
84	During the DMA test (Test 14), the DMA has a read serial data compare error.	1. DMA PCA-A6. 2. Read/Write Chain.
85	During the DMA test (Test 14), the DMA read a wrong CRC error flag value.	DMA PCA-A6
86	During the DMA test (Test 14), the DMA sector counter is miscounting.	DMA PCA-A6.
87	During the DMA test (Test 14), the DMA has a write serial data compare error.	1. DMA PCA-A6. 2. Read/Write Chain.
88	During the DMA test (Test 14), UNER-L or FUNER-L are being pulled low.	1. DMA PCA-A6. 2. Read/Write Chain.
89	During the DMA test (Test 14), the DMA disc address did not increment.	DMA PCA-A6.
90	During the ECC chip test (Test 16), the ECC interface lines are not what is expected.	DMA PCA-A6.
93	During the ECC chip test (Test 16), there is an ECC chip hardware fault.	DMA PCA-A6
96	During the HP-IB chip test (Test 15), the wrong interrupt bits are set.	DMA PCA-A6.
97	During the HP-IB chip test (Test 15), there is a wraparound data compare error.	DMA PCA-A6.
98	During the HP-IB chip test (Test 15), the identity bits have the wrong value.	DMA PCA-A6.

Table 5-9. Test Error (TERR) Numbers (continued)

NO.	CAUSE	SUSPECTED HARDWARE
99	During the HP-IB chip test (Test 15), the HP-IB interface write missed the end of byte count.	DMA PCA-A6.
100	During the HP-IB chip test (Test 15), the EOI is not received.	DMA PCA-A6.
101	During the HP-IB chip test (Test 15), the secondary command is not detected.	DMA PCA-A6.
102	During the HP-IB chip test (Test 15), there is a write data compare error.	DMA PCA-A6.
103	During the HP-IB chip test (Test 15), there is a read data compare error.	DMA PCA-A6.
104	During the HP-IB chip test (Test 15), the IOSTOP signal came too soon.	DMA PCA-A6.
105	During the HP-IB chip test (Test 15), the sector counter missed incrementing on an I/O write.	DMA PCA-A6.
106	During the HP-IB chip test (Test 15), the sector counter missed decrementing on an I/O read.	DMA PCA-A6.
107	During the HP-IB chip test (Test 15), the automatic buffer fill failed. Buffer fill is for data security.	DMA PCA-A6.
108	During the HP-IB chip test (Test 15), there is a data compare error during an I/O read.	DMA PCA-A6.
112	During the Control Panel Test (Test 9), the top door is open.	Top door sensor and associated circuitry.
113	During the head load sequence following test 40, the media module is not detected as being installed.	1. Media module. 2. Spindle Driver PCA-A12.
114	During the head load sequence following test 40, excessive runout is measured following a head load. Remove the media module and reinstall it.	1 Media Module. 2. Spindle. 3. Servo System.
115	During the head load sequence following test 40, the velocity transducer signal unexpectedly changed.	1 The sliding module door is closed. 2. Velocity Transducer. 3 Carriage Assembly.
116	The user aborted the diagnostic by pressing a button, or the CPU issued a cancel or clear command while the diagnostic is running.	None
117	The user failed to do a Seek command that displays a cylinder address before the command that transfers data.	None
118	The sector counter is not counting properly.	Microprocessor PCA-A4.
119	During the Control Panel test (Test 9), the data written to the display register cannot be read back.	1. Control Panel PCA-A14. 2. Microprocessor PCA-A4.
120	During the Control Panel test (Test 9), the sensor interlock (pressure sensor cable connector) is open.	Control Panel PCA-A14.

Table 5-9. Test Error (TERR) Numbers (continued)

NO.	CAUSE	SUSPECTED HARDWARE
121	During the Control Panel test (Test 9), the keyboard/display scan is too slow.	Control Panel PCA-A14.
124	During the Control Panel test (Test 9), the microprocessor fault register door open bit does not match the control panel door open bit.	1. Microprocessor PCA-A4. 2. Control Panel PCA-A14.
125	The Control Panel read an illegal key value from the keyboard interface.	Control Panel PCA-A14.
126	During the Control Panel test (Test 9), the top door sensor cable is missing.	1. Top door sensor cable is not connected to PCA-A14. 2. Control Panel PCA-A14.
127	Data transfers are illegal following a No Verify For Seeks command. A Seek command without the No Verify option must be performed before data transfers are allowed.	None.
128	During the Spindle Driver test (Test 13), the bits in the spindle status register that should be zero are not.	Spindle Driver PCA-A12.
129	During the Spindle Driver test (Test 13), the spindle enable flip-flop does not read back what is written to it.	Spindle Driver PCA-A12.
130	During the Spindle Driver test (Test 13), the run/stop flip-flop does not read back what is written to it.	Spindle Driver PCA-A12.
131	During the Spindle Driver test (Test 13), the spindle cable is not plugged on the Spindle Driver.	1. Spindle-motor assembly cable. 2. Spindle Driver PCA-A12.
132	During the Spindle Driver test (Test 13), the Spindle Driver heat sink is over-temperature.	Spindle Driver PCA-A12.
133	During the Spindle Driver test (Test 13), the spindle speed up bit is not correct.	Spindle Driver PCA-A12
134	During the Spindle Driver test (Test 13), software timing of the Spindle Driver input clocks indicates that one of them is too slow.	Spindle Driver PCA-A12.
135	During the Spindle Driver test (Test 13), the current sense detectors indicate that no current is flowing in spindle phases.	Spindle Driver PCA-A12.
136	During the Spindle Driver test (Test 13), the encoder bits in the control register did not change. The spindle will not rotate.	Spindle Driver PCA-A12.
137	During the Spindle Driver test (Test 13), the spindle did not lose full speed within the allotted time.	Spindle Driver PCA-A12.
138	During the Spindle Driver test (Test 13), the phase detector bit is in the wrong state.	Spindle Driver PCA-A12.
139	During the Spindle Driver test (Test 13), the microprocessor fault register speed down bit does not match the spindle speed down condition of Spindle Driver PCA-A12.	Spindle Driver PCA-A12.

Table 5-9. Test Error (TERR) Numbers (continued)

NO.	CAUSE	SUSPECTED HARDWARE
140	During the Spindle Driver test (Test 13), one or more card cage PCAs are missing.	Spindle Driver PCA-A12.
141	During the up-to-speed test (Test 33), the software time out for reaching full speed expired.	1. Spindle Driver PCA-A12. 2. Media module. 3. Spindle assembly.
142	A diagnostic is requested which requires that the drive be at full speed while it is not.	None
144	During the Servo interface test (Test 19), the CNVF-L bit is high. A cable is disconnected or missing.	1. Velocity Transducer Cable. 2. Actuator Status PCA-A18. 3. Servo PCA-A3.
145	During the Servo interface test (Test 19), the reference voltage measured out of range.	Servo PCA-A3.
146	During the Servo test (Test 35), the offset voltage measurement did not agree with the value to which the offset DAC is set.	Servo PCA-A3.
147	During the Servo test (Test 35), the DTG register has an unexpected value.	Servo PCA-A3.
148	During the Servo test (Test 35), the velocity command signal measured out of range.	Servo PCA-A3.
149	During the Servo test (Test 35), the current command signal has an unexpected value.	1. Servo PCA-A3. 2. Emergency Retract PCA-A20 (part of PCA-A2).
151	During the Servo test (Test 35), the DTG register has the wrong value indicating that it is clocked by a simulated track crossing voltage less than that specified by first track crossing, or position control mode did not disable the quarter track crossing detector.	Servo PCA-A3.
152	During the Servo test (Test 35), the DTG register has the wrong value indicating that it is not clocked by a track crossing simulated by varying the offset DAC.	Servo PCA-A3.
153	During the Servo test (Test 35), the DTG register has the wrong value indicating that it is not clocked by a quarter track crossing simulated by varying the offset DAC.	Servo PCA-A3.
154	During the Servo test (Test 35), the DTG clock control logic or DTG register failed.	Servo PCA-A3.
155	During the Servo test (Test 35), the off-track circuit did not trigger correctly.	Servo PCA-A3.
156	During the Servo test (Test 35), the deceleration bit has the wrong value.	Servo PCA-A3.
157	During the Servo test (Test 35), the position signal has the wrong value.	Servo PCA-A3.
158	During the Servo interface test (Test 19), the velocity transducer signal is not zero during self test.	1. Velocity transducer. 2. Servo PCA-A3.

Table 5-9. Test Error (TERR) Numbers (continued)

NO.	CAUSE	SUSPECTED HARDWARE
159	During the Servo interface test (Test 19), or the Servo test (Test 35), the carriage is not back or the velocity transducer signal is not zero.	1. Carriage Latch. 2. Actuator Status PCA-A18. 3. Servo PCA-A3. 4. Emergency Retract PCA-A20 (part of PCA-A2).
160	During the Servo interface test (Test 19), the actuator temperature measurement is out of range.	1. Actuator too hot. 2. Actuator temperature sensor. 3. Actuator Status PCA-A18. 4. Servo PCA-A3.
161	During the Servo interface test (Test 19), the media module exhaust temperature measurement is out of range.	1. Actuator Status PCA-A18. 2. Servo PCA-A3.
162	During the Servo interface test (Test 19), the DTG register did not contain what was written to it.	Servo PCA-A3.
163	During the Servo interface test (Test 19), the Servo current command is not disabled by Emergency Retract.	Servo PCA-A3.
165	During the Track Follower test (Test 20), data written cannot be read back.	Track follower PCA-A9.
167	During the Track Follower test (Test 20), the once-around-counter fails.	Track Follower PCA-A9.
168	During the Track Follower test (Test 20), the skew delay comparator fails.	Track Follower PCA-A9.
169	During the Track Follower test (Test 20), the SOS-L signal has the wrong value.	1. Track Follower PCA-A9. 2. Formatter/Separator PCA-A8. 3. DMA PCA-A6.
170	During the Track Follower test (Test 20), the sector-sync circuit fails.	Track follower PCA-A9.
171	During the Track Follower test (Test 20), the track position discriminator and position signal output circuits fail.	Track Follower PCA-A9.
172	During the Track Follower test (Test 20), the skew measure circuit fails.	1. Track Follower PCA-A9. 2. Read/Write PCA-A10.
176	During the head load operation and verification (Test 1), a drive error was generated which aborted the operation. (See note 1.)	As determined by the drive error (DERR) logged in the fault log.
177	During the seek verification test (Test 2), a drive error was generated which aborted the operation. (See note 1.)	As determined by the drive error (DERR) logged in the fault log.
178	During the Read/Write verification test (Test 3), a drive error was generated which aborted the operation. (See note 1.)	As determined by the drive error (DERR) logged in the fault log.
179	During the drive verification test (Test 5), a drive error was generated which aborted the operation. (See note 1.)	As determined by the drive error (DERR) logged in the fault log.
180	During the head load operation and verification (Test 1), the heads were unloaded which aborted the operation. (See note 1.)	As determined by the drive error (DERR) logged in the fault log.

*Note 1. Drive errors may be logged in either the fault log or in status. The user should read the fault log drive errors and not rely only on the status message.

Table 5-9. Test Error (TERR) Numbers (continued)

NO.	CAUSE	SUSPECTED HARDWARE
181	During the seek verification test (Test 2), the heads were unloaded which aborted the operation. (See note 1.)	As determined by the drive error (DERR) logged in the fault log.
182	During the Read/Write verification test (Test 3), the heads were unloaded which aborted the operation. (See note 1.)	As determined by the drive error (DERR) logged in the fault log.
183	During the drive verification test (Test 5), the heads were unloaded which aborted the operation. (See note 1.)	As determined by the drive error (DERR) logged in the fault log.
184	During the head load and verification (Test 1), a Hardware Fault Register bit is set which aborted the operation. (See note 1.)	As determined by the drive error (DERR) logged in the fault log.
185	During the seek verification test (Test 2), a Hardware Fault Register bit is set which aborted the operation. (See note 1.)	As determined by the drive error (DERR) logged in the fault log.
186	During the Read/Write verification test (Test 3), a Hardware Fault Register bit is set which aborted the operation. (See note 1.)	As determined by the drive error (DERR) logged in the fault log.
187	During the drive verification test (Test 5), a Hardware Fault Register bit is set which aborted the operation. (See note 1.)	As determined by the drive error (DERR) logged in the fault log.
188	During the head load and verification (Test 1), the AGC fault is set or off-track occurred more than once which aborted the operation. (See note 1.)	1. Actuator Driver PCA-A2. 2. Servo Head. 3. Actuator. 4. Media.
189	During the seek verification test (Test 2), the AGC fault is set or off-track occurred more than once which aborted the operation. (See note 1.)	1. Track Follower PCA-A9. 2. Servo PCA-A3. 3. Actuator Driver PCA-A2. 4. Servo Head. 5. Media.
190	During the Read/Write verification test (Test 3), the AGC fault is set or off-track occurred more than once which aborted the operation. (See note 1.)	1. Track Follower PCA-A9. 2. Servo PCA-A3. 3. Actuator Driver PCA-A2. 4. Servo Head. 5. Media
191	During the drive verification test (Test 5), the AGC fault is set or off-track occurred more than once which aborted the operation. (See note 1.)	1. Track Follower PCA-A9. 2. Servo PCA-A3. 3. Actuator Driver PCA-A2. 4. Servo Head. 5. Media.
192	In any of the functional verification tests (Tests 1, 2, 3, 5), the proper number of Data Clock Pulses are not received for a head, or, automatic head alignment failed. (See note 1.)	1. Track Follower PCA-A9. 2. Servo PCA-A3. 3. Read/Write PCA-A10. 4. Data Heads. 5. Media.
193	During the head load and verification (Test 1), the Start of Sector timing is wrong.	1. Track Follower PCA-A9. 2. Spindle Driver PCA-A12. 3. Media.
194	During the head load and verification (Test 1), the Sector Clock Pulse timing is wrong.	1. Track Follower PCA-A9. 2. Servo Head. 3. Media.
195	During the head load and verification (Test 1), or the seek Verification test (Test 2), the Data Clock Pulse count is wrong.	1. Read/Write PCA-A10. 2. Servo PCA-A3. 3. Track Follower PCA-A9. 4. Data Heads. 5. Media.

Table 5-9. Test Error (TERR) Numbers (continued)

NO.	CAUSE	SUSPECTED HARDWARE
196	During the seek verification test (Test 2), the seek time is too long.	1. Servo PCA-A3. 2. Actuator Driver PCA-A2. 3. Linear Motor. 4. Carriage. 5. Rails.
197	During the Read/Write verification test (Test 3), the test sector gets data errors.	1. Read/Write PCA-A10. 2. Formatter/Separator PCA-A8. 3. Heads. 4. Media.
198	During the Read/Write verification test (Test 3), all sectors get data errors.	DMA PCA-A6.
199	During the Read/Write verification test (Test 3), a probable head/media problem occurred. The fault log contains the errors.	1. Read/Write PCA-A10. 2. Formatter/Separator PCA-A8. 3. DMA PCA-A6. 4. Heads. 5. Media.
200	During the Read/Write verification test (Test 3), all sectors get uncorrectable errors in the ECC test.	1. DMA PCA-A6. 2. Heads. 3. Media.
201	During the Read/Write verification test (Test 3), a correctable error is expected, but not generated.	1. DMA PCA-A6. 2. Heads. 3. Media.
202	During the Read/Write verification test (Test 3), an uncorrectable error is expected, but not generated.	1. DMA PCA-A6 2. Other PCA's. 3. Heads. 4. Media.
203	During the Read/Write verification test (Test 3), the CRC is not set on reading an uncorrectable error.	1. DMA PCA-A6. 2. Heads. 3. Media.
204	During the Read/Write verification test (Test 3), there are too many off-tracks generated.	1. Servo PCA-A3. 2. Track Follower PCA-A9. 3. Actuator Driver PCA-A2. 4. Actuator Assembly.
205	During the Read/Write verification test (Test 3), there are too many verify faults generated.	1. PCA's. 2. Actuator Assembly.
208	During the Read/Write test (Test 18), there is a Read/Write data path or fault detect error.	1. Formatter/Separator PCA-A8. 2. Read/Write PCA-A10. 3. Motherboard PCA-A11. 4. Head Connectors.
209	During the Read/Write test (Test 18), the automatic head alignment circuits fail.	1. Formatter/Separator PCA-A8. 2. Read/Write PCA-A10. 3. Motherboard PCA-A11.
210	During the Read/Write test (Test 18), a head is open, or disconnected, or connected wrong.	1. Heads. 2. Read/Write PCA-A10.
211	During the Read/Write test (Test 18), Read/Write faults are not read by the microprocessor.	1. Read/Write PCA-A10. 2. Formatter/Separator PCA-A8. 3. Microprocessor PCA-A4. 4. Motherboard PCA-A11.
212	During the Read/Write test (Test 18), an A/D converter error occurred.	Microprocessor PCA-A4.
213	During the Read/Write fault line test (Test 38), the Emergency Retract fault is not detected.	1. Read/Write PCA-A10. 2. Formatter/Separator PCA-A8.

Table 5-9. Test Error (TERR) Numbers (continued)

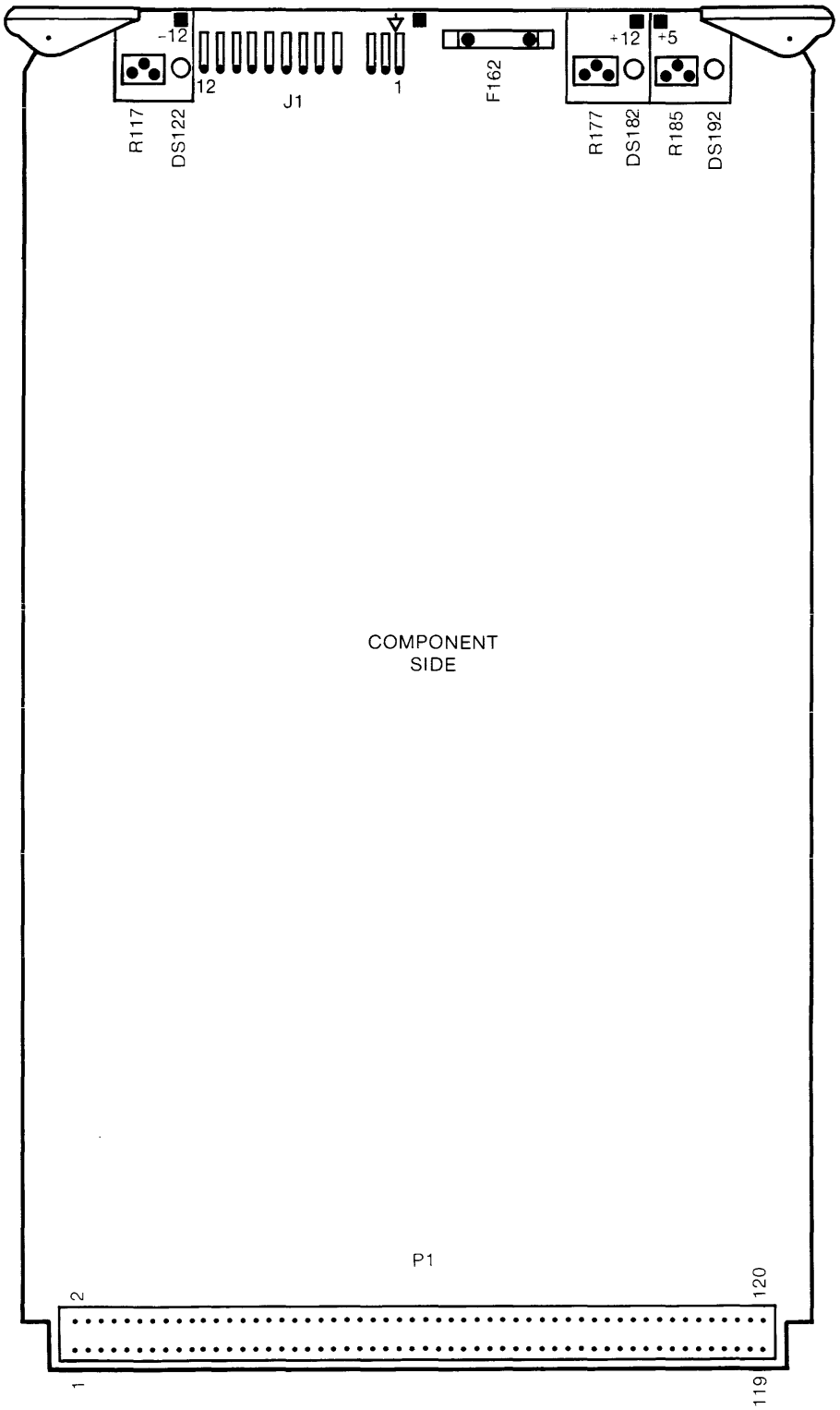
NO.	CAUSE	SUSPECTED HARDWARE
214	During the Read/Write fault line test (Test 38), the Track Follower fault is not detected.	1. Read/Write PCA-A10. 2. Track Follower PCA-A9.
215	During the Read/Write fault line test (Test 38), the Servo off-track fault is not detected.	1. Read/Write PCA-A10. 2. Formatter/Separator PCA-A8.
216	During the Read/Write fault line test (Test 38), fault from either the Emergency Retract, the Track Follower, or the Servo was detected.	1. Read/Write PCA-A10. 2. Emergency Retract PCA-A20 (part of PCA-A2). 3. Track Follower PCA-A9. 4. Servo PCA-A3.
224	During the Actuator Driver test (Test 40), the tachometer indicates either no carriage movement, or movement in the wrong direction.	1. Velocity transducer. 2. Actuator coil. 3. Servo PCA-A3. 4. Actuator Driver PCA-A2.
225	During the Emergency Retract test parts 2, 3, 4, and 5 (Tests 12, 34, 37, and 39), one or more of the bits in the Emergency Retract registers is bad.	1. Emergency Retract PCA-A20 (part of PCA-A2). 2. Spindle Driver PCA-A12.
226	During the Emergency Retract test part 3 (Test 34), or Actuator Driver test (Test 40), the actuator current is out of range.	1. Actuator Driver PCA-A2/Emergency Retract PCA-A20. 2. Servo PCA-A3.
227	During the Emergency Retract Speed Up test (Test 36), the spindle speed down condition fails to set Emergency Retract.	1. Actuator Driver PCA-A2/Emergency Retract PCA-A20. 2. Servo PCA-A12.
228	During the Emergency Retract test parts 1, 2, and 3 (Tests 11, 12, and 34), the Emergency Retract register bits do not match the Emergency Retract latch.	Emergency Retract PCA-A20 (part of PCA-A2).
229	During the Emergency Retract test part 1 (Test 11), the grounded bit has the wrong value.	Emergency Retract PCA-A20 (part of PCA-A2).
230	During the Emergency Retract test part 1 (Test 11), the power supply fail bit has the wrong value.	1. Spindle Driver Fuses (+/- 36V Emergency Retract fuses). 2. Emergency Retract PCA-A20 (part of PCA-A2).
231	During the Emergency Retract test part 2 (Test 12), the power-on bit has the wrong value.	Emergency Retract PCA-A20 (part of PCA-A2).
232	During the Emergency Retract test parts 2 and 3 (Tests 12 and 34), the microprocessor Emergency Retract bit has the wrong value.	1. Microprocessor PCA-A4. 2. Emergency Retract PCA-A20 (part of PCA-A2).
233	During the Emergency Retract test parts 3, 4, and 5 (Tests 34, 37, and 39), or the Actuator Driver test (Test 40), there was an A/D conversion error.	Microprocessor PCA-A4.
234	During the Emergency Retract test parts 3, 4, and 5 (Tests 34, 37, and 39), or the Actuator Driver test (Test 40), the carriage moved when it should not have.	1. Actuator Status PCA-A18. 2. Emergency Retract PCA-A20 (part of PCA-A2). 3. Servo PCA-A3.
235	During the Emergency Retract test parts 3, 4, and 5 (Tests 34, 37, and 39), or the Actuator Driver test (Test 40), the actuator current is out of range.	1. Actuator Driver PCA-A2 2. Servo PCA-A3.

Table 5-9. Test Error (TERR) Numbers (continued)

NO.	CAUSE	SUSPECTED HARDWARE
236	During the Actuator Driver test (Test 40), the Servo current command value is out of range.	Servo PCA-A3.
237	During the Actuator Driver test (Test 40), the actuator current has the wrong value.	1. Servo PCA-A3. 2. Actuator Driver PCA-A2.
238	During the Emergency Retract test parts 2, 3, and 5 (Tests 12, 34, and 39), or the Actuator Driver test (Test 40), the spindle lost speed during an emergency retract test.	1. Spindle Driver PCA-A12. 2. Emergency Retract PCA-A20 (part of PCA-A2).
239	Heads are stuck out on the disc before the diagnostics are run. Head unload has been unsuccessful.	1. Actuator Status PCA-A18 (carriage back detector). 2. Servo PCA-A3.
240	During the Formatter/Separator test (Test 17), the data written could not be read back.	Formatter/Separator PCA-A8.
241	During the Formatter/Separator test (Test 17), the write-clock oscillator, the control state machine, or signals that leave the board cause a failure.	Formatter/Separator PCA-A8.
242	During the Formatter/Separator test (Test 17), full-speed data read back from the Formatter/Separator does not match the data written.	Formatter/Separator PCA-A8.
243	During the Formatter/Separator test (Test 17), the generated RWC-L signal cannot be read correctly.	1. Formatter/Separator PCA-A8. 2. DMA PCA-A6.
244	During the Formatter/Separator test (Test 17), the generated FOUT-H signal cannot be read correctly.	1. Formatter/Separator PCA-A8. 2. DMA PCA-A6.
245	During the Formatter/Separator test (Test 17), the generated SOD-L signal cannot be read correctly.	1. Formatter/Separator PCA-A8. 2. DMA PCA-A6.
246	During the Formatter/Separator test (Test 17), or the Formatter/ Separator interface test (Test 31), the generated FUNER-L signal cannot be read correctly.	1. Formatter/Separator PCA-A8. 2. DMA PCA-A6.
247	During the Formatter/Separator test (Test 17), the wrong FIN-H value is read.	1. Formatter/Separator PCA-A8. 2. DMA PCA-A6.
248	During the Formatter/Separator test (Test 17), the wrong EOS-L value is read.	1. Formatter/Separator PCA-A8. 2. DMA PCA-A6.
249	During the Formatter/Separator test (Test 17), or the Formatter /Separator interface test (Test 31), the wrong SOS-L value is read.	1. Formatter/Separator PCA-A8. 2. Track Follower PCA-A9. 3. DMA PCA-A6.
250	During microdiagnostic isolation routines, more than two PCA's failed.	The failed part is indicated on the display. Refer to table 5-4 for failed part codes.
251	Motherboard drive type bits have the wrong value.	1. Motherboard PCA-A11. 2. Microprocessor PCA-A4.
253	Background diagnostics found an unexpected hardware fault indicated in the hardware fault register. Examine the hardware fault register contents found in the fault log.	1. PCA indicated by the hardware fault register.

Table 5-9. Test Error (TERR) Numbers (continued)

NO.	CAUSE	SUSPECTED HARDWARE
254	Background diagnostics found a data RAM error in the DMA buffer RAM.	1. DMA PCA-A6.

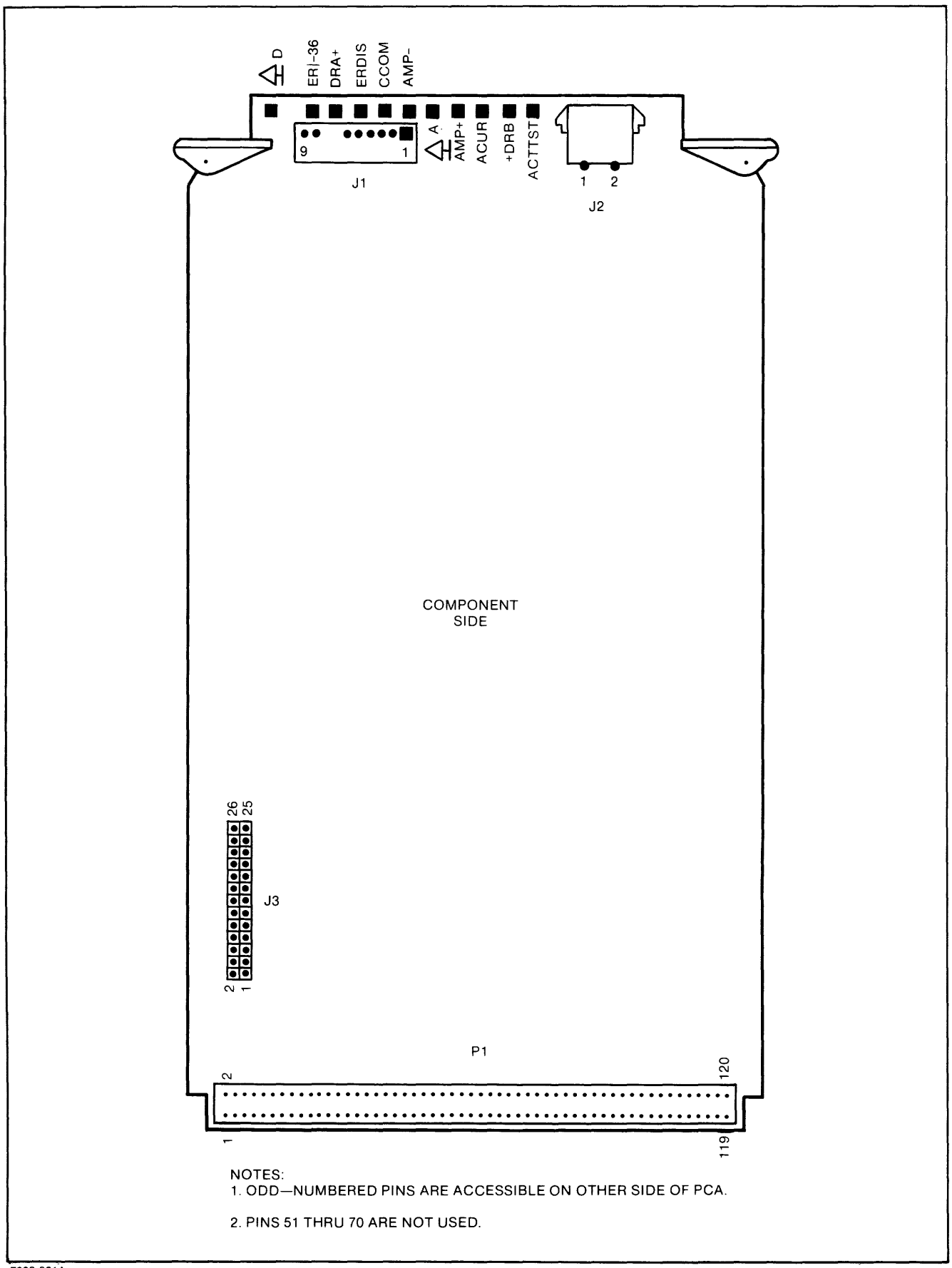


NOTES:
1. ODD—NUMBERED PINS ARE ACCESSIBLE ON OTHER SIDE OF PCA.

2. PINS 51 THRU 70 ARE NOT USED.

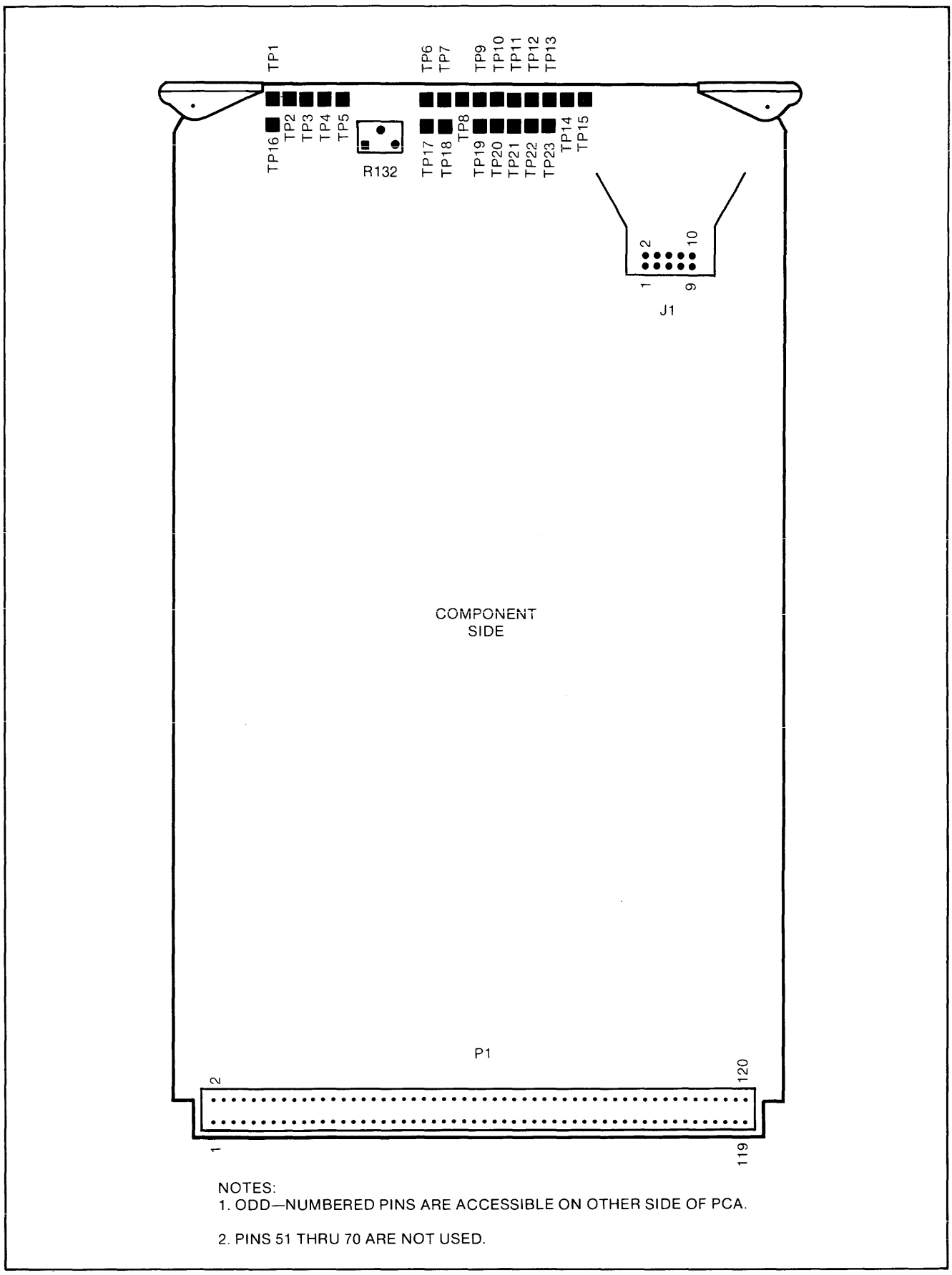
7933-330

Figure 5-3. Regulator PCA-A1 Layout



7933-331A

Figure 5-4. Actuator Driver PCA-A2 Layout

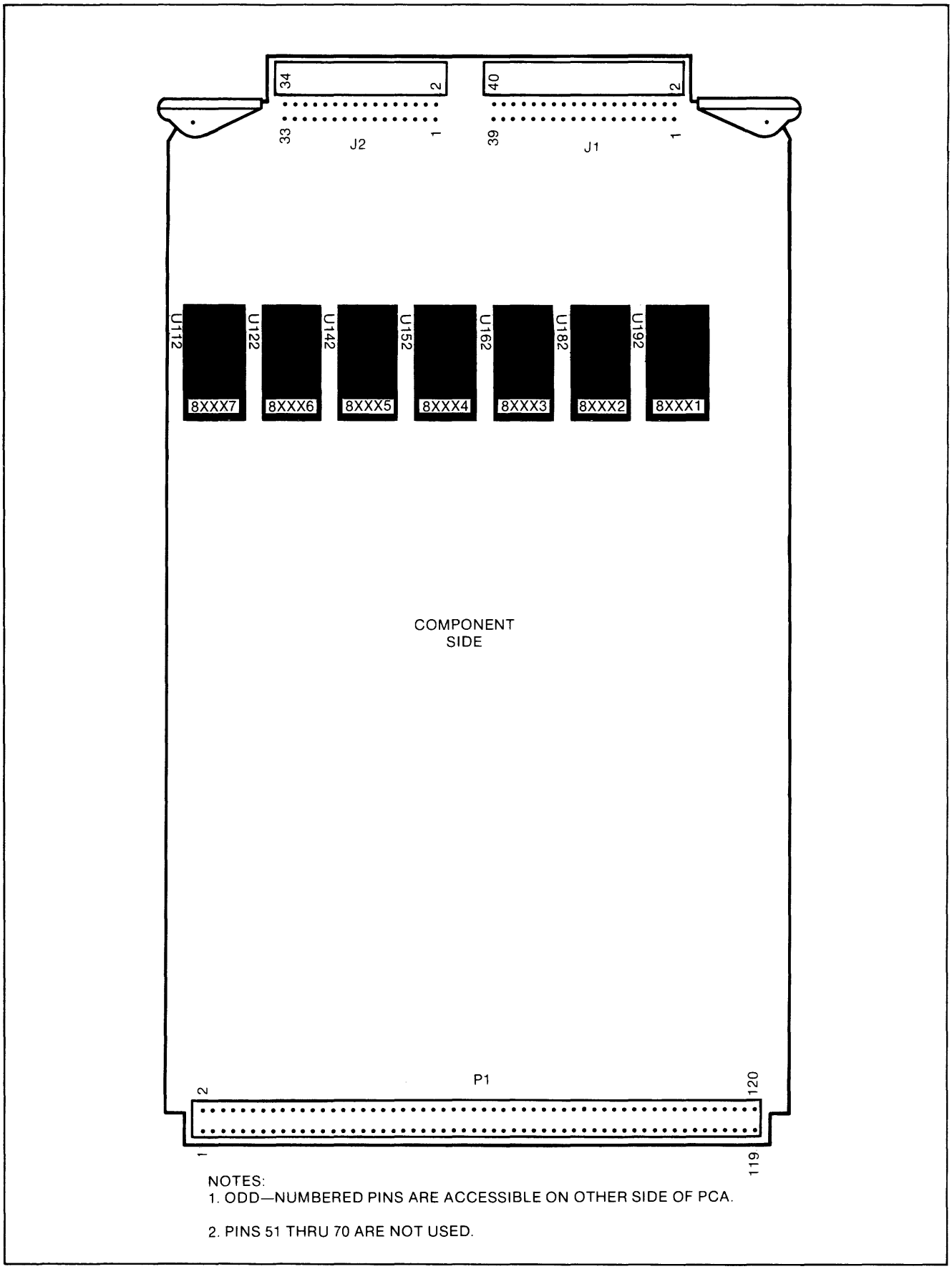


NOTES:
1. ODD—NUMBERED PINS ARE ACCESSIBLE ON OTHER SIDE OF PCA.

2. PINS 51 THRU 70 ARE NOT USED.

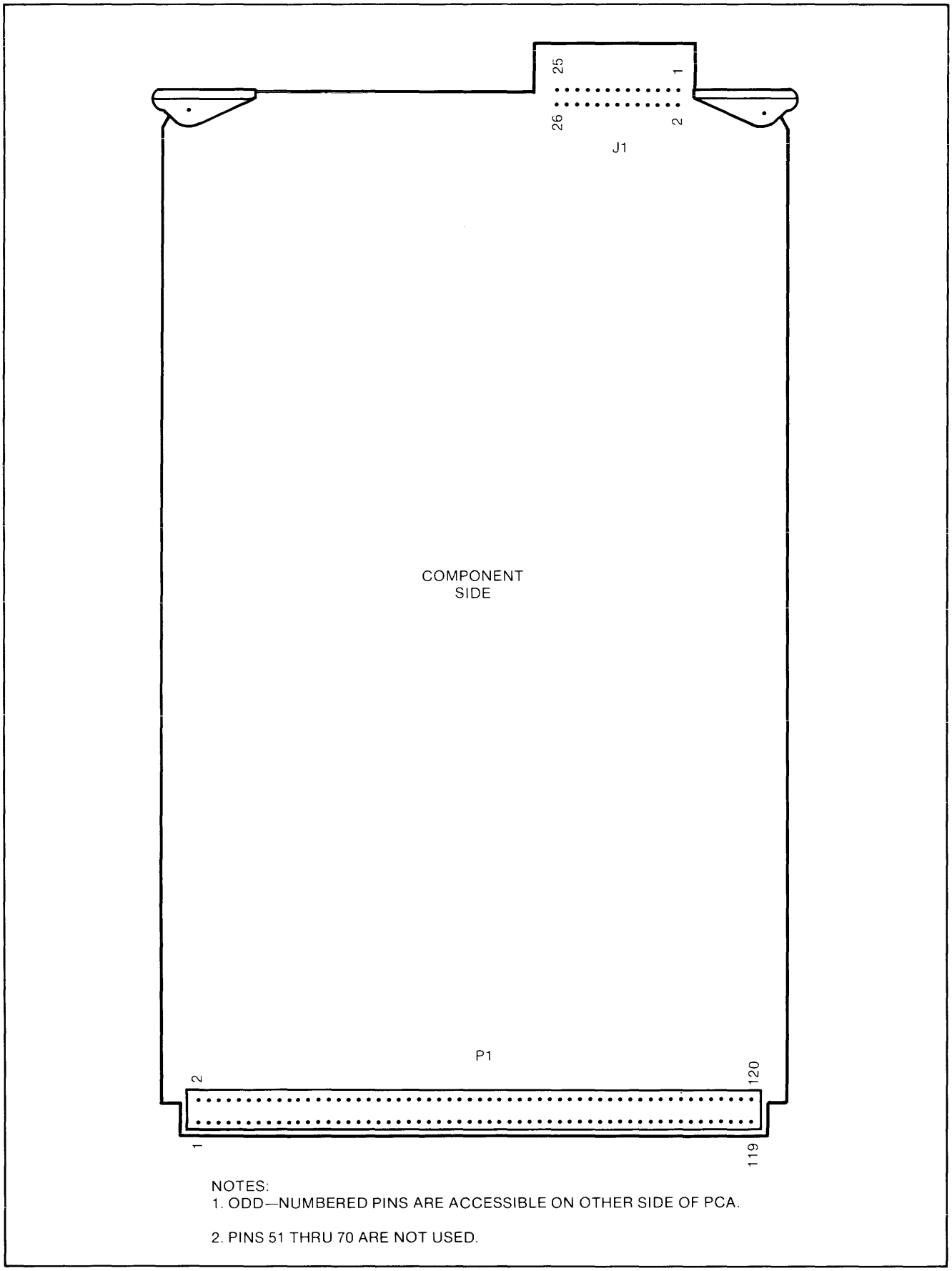
7933-332

Figure 5-5. Servo PCA-A3 Layout



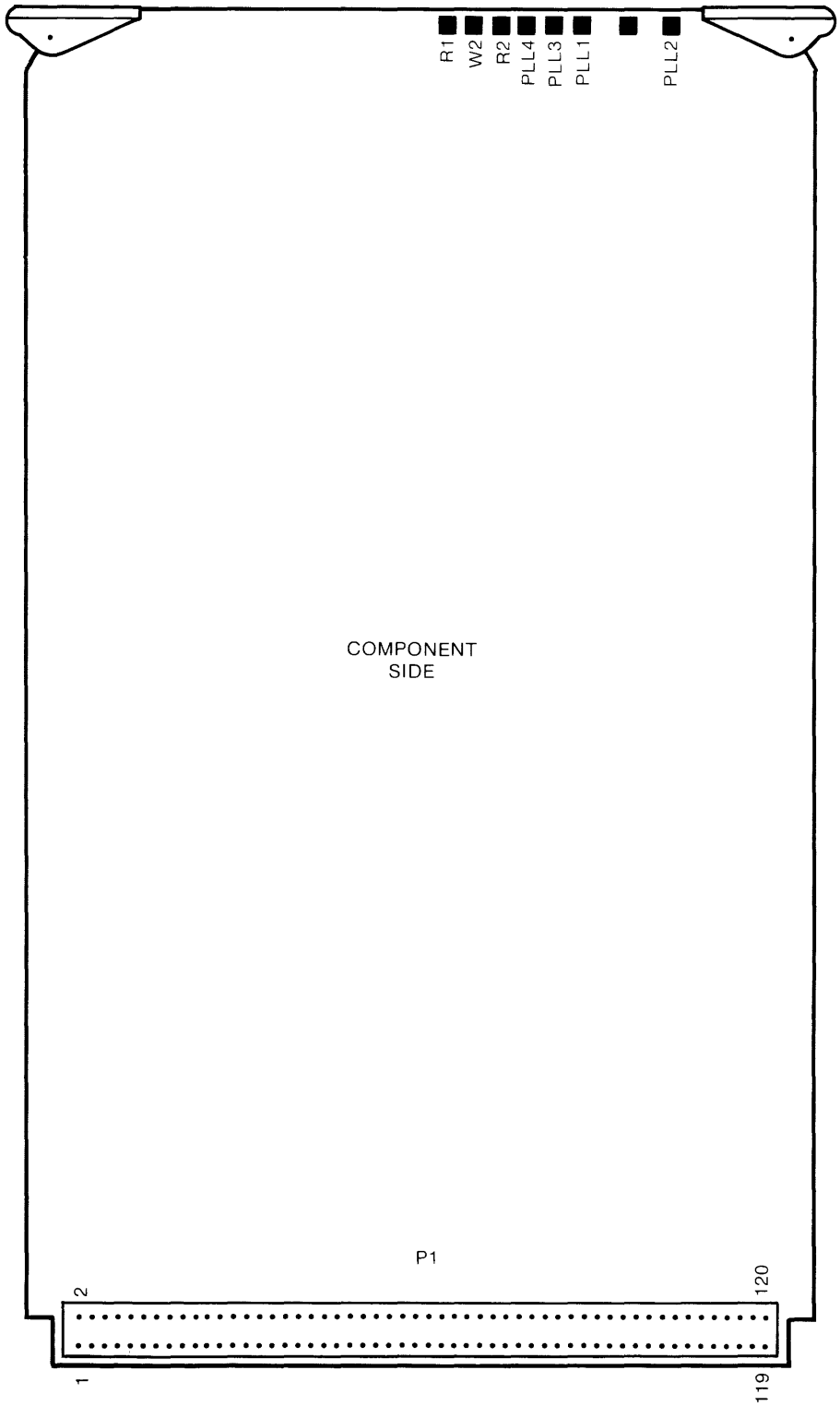
7933-333A

Figure 5-6. Microprocessor PCA-A4 Layout



7933-334

Figure 5-7. Disc Memory Access (DMA) PCA-A6 Layout

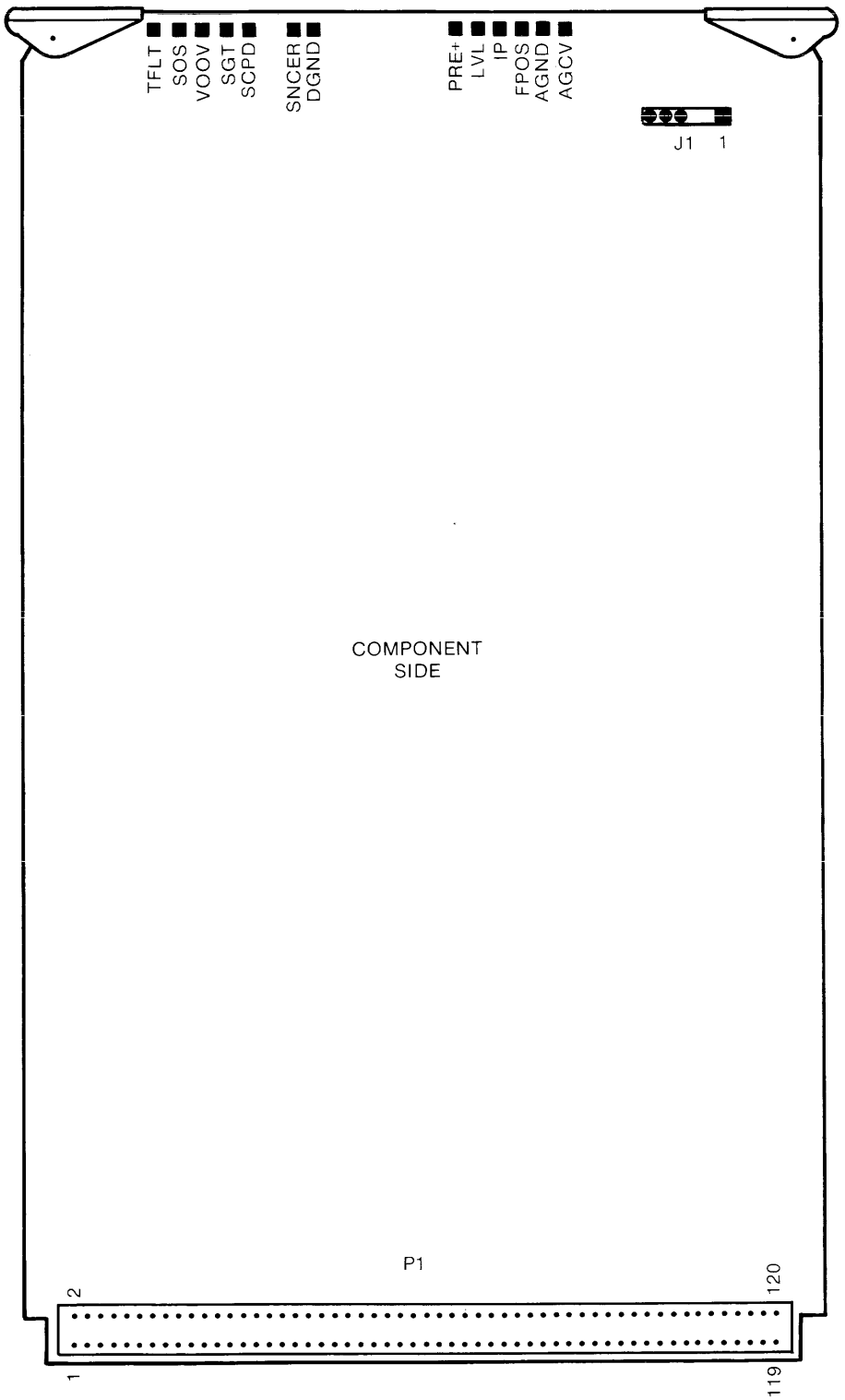


NOTES:
1. ODD—NUMBERED PINS ARE ACCESSIBLE ON OTHER SIDE OF PCA.

2. PINS 51 THRU 70 ARE NOT USED.

7933-336

Figure 5-8. Formatter/Separator PCA-A8 Layout

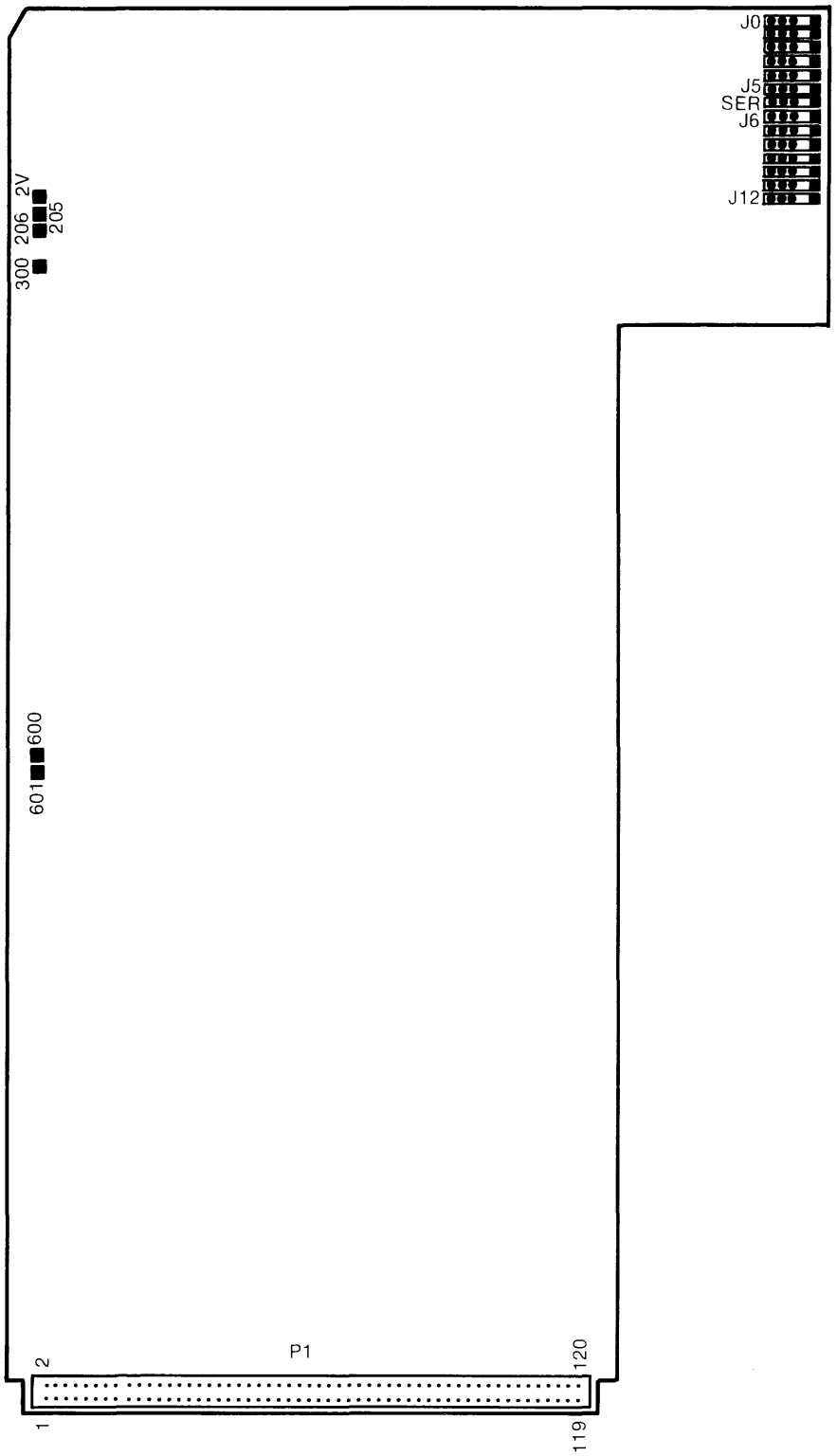


NOTES:
1. ODD—NUMBERED PINS ARE ACCESSIBLE ON OTHER SIDE OF PCA.

2. PINS 51 THRU 70 ARE NOT USED.

7933-337

Figure 5-9. Track Follower PCA-A9 Layout

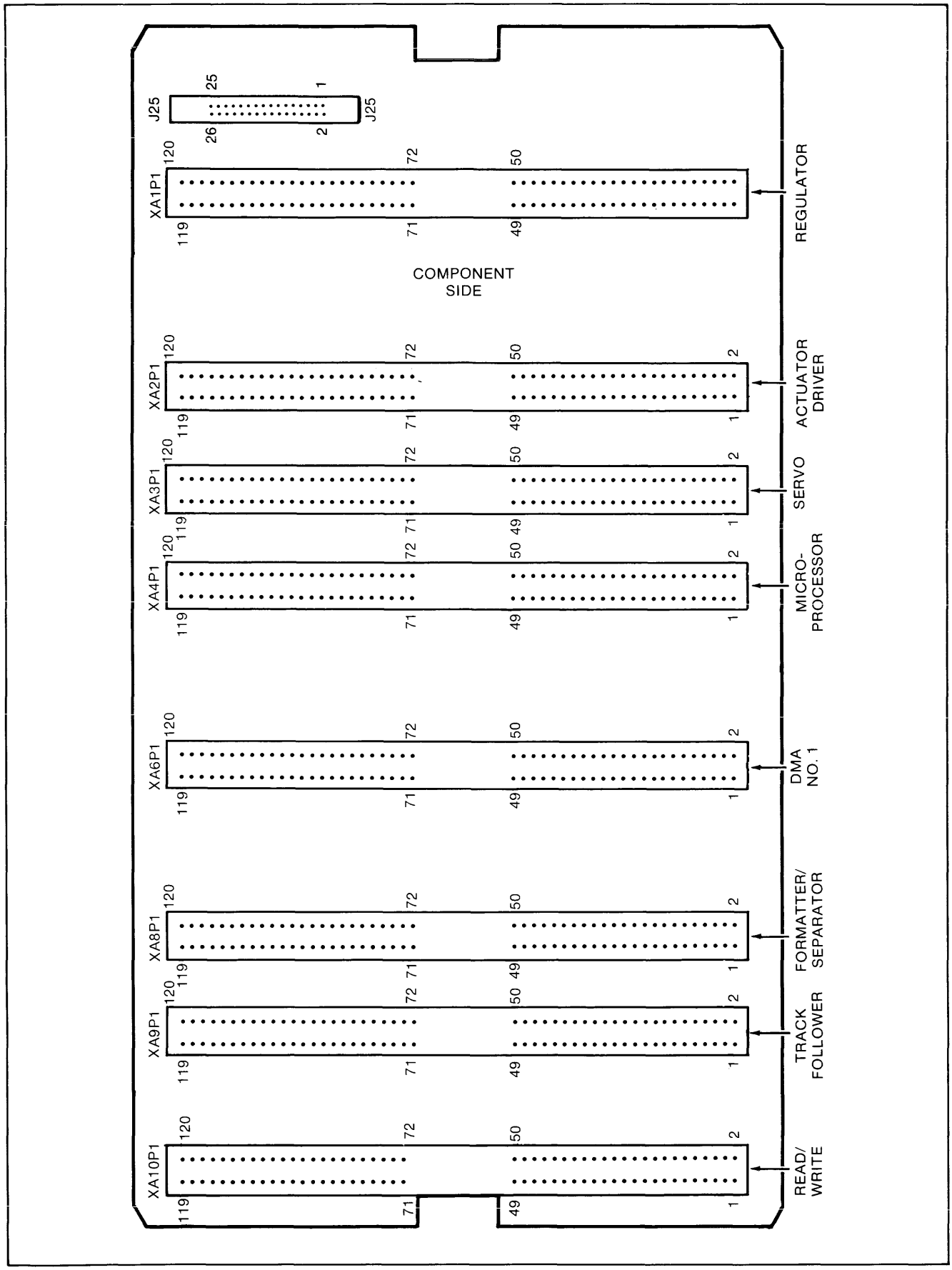


NOTES:
1. ODD—NUMBERED PINS ARE ACCESSIBLE ON OTHER SIDE OF PCA.

2. PINS 51 THRU 70 ARE NOT USED.

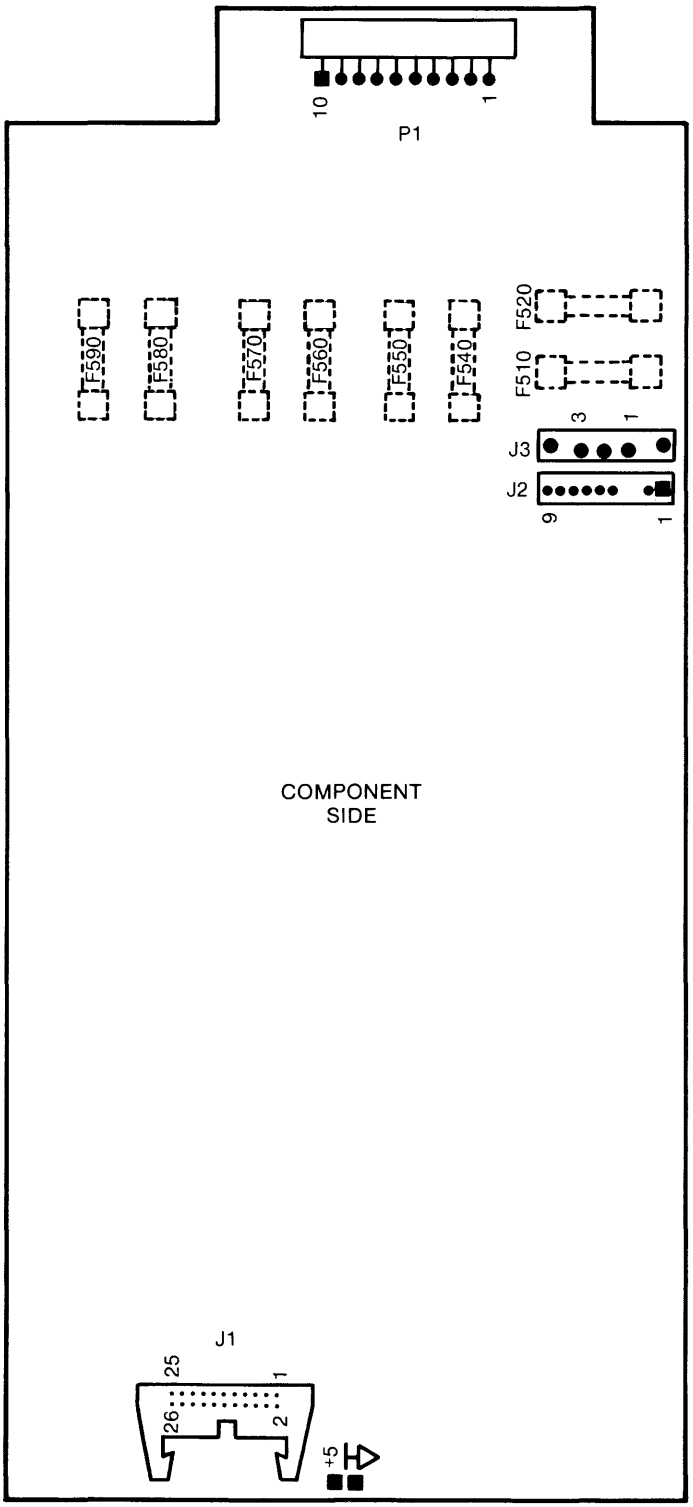
7933-338

Figure 5-10. Read/Write PCA-A10 Layout



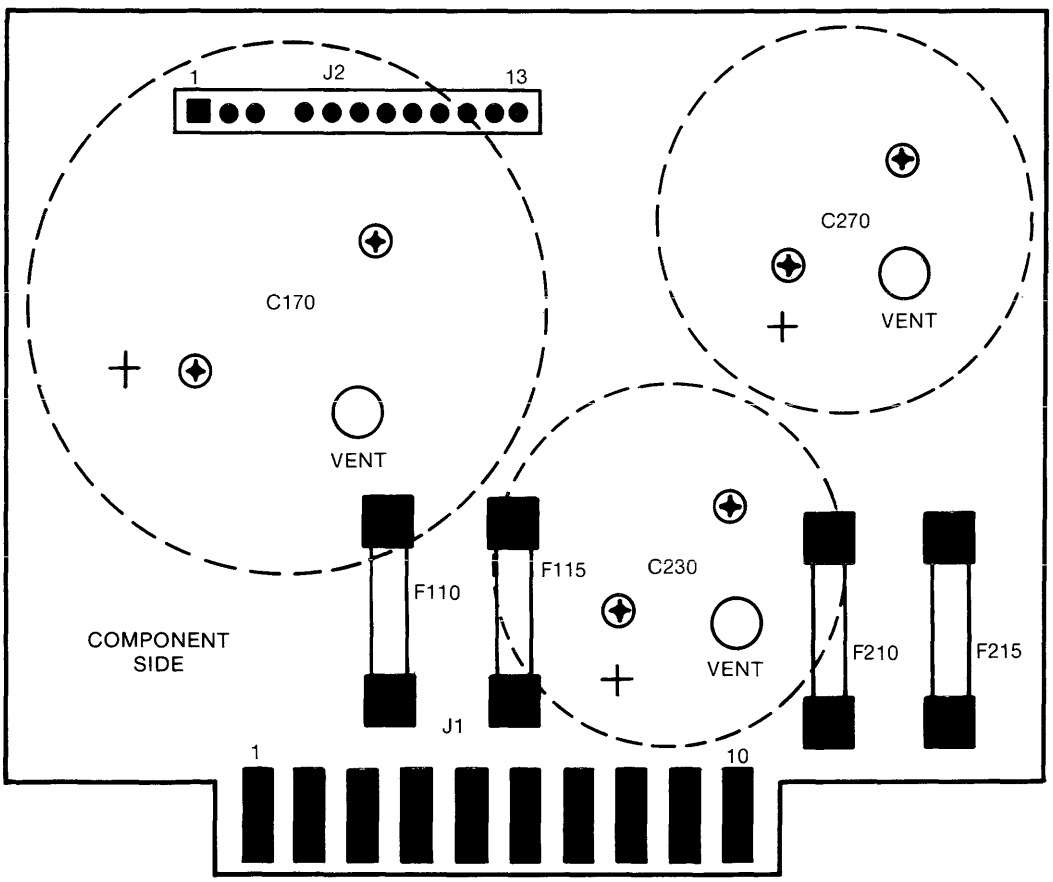
7933-339

Figure 5-11. Motherboard PCA-A11 Layout



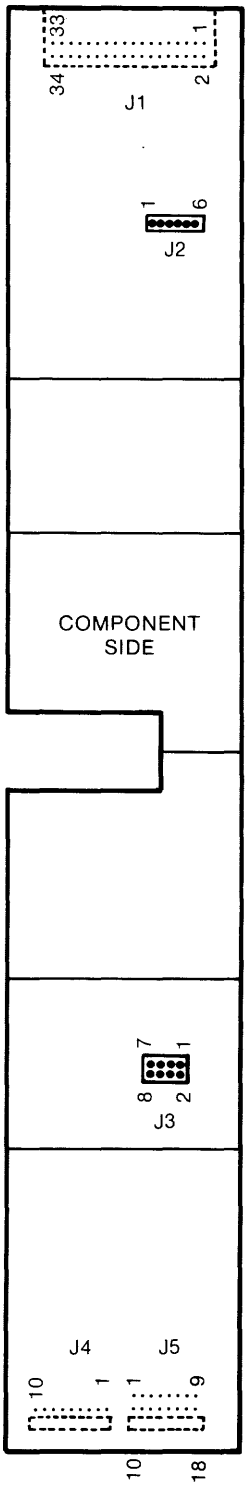
7933-340

Figure 5-12. Spindle Driver PCA-A12 Layout



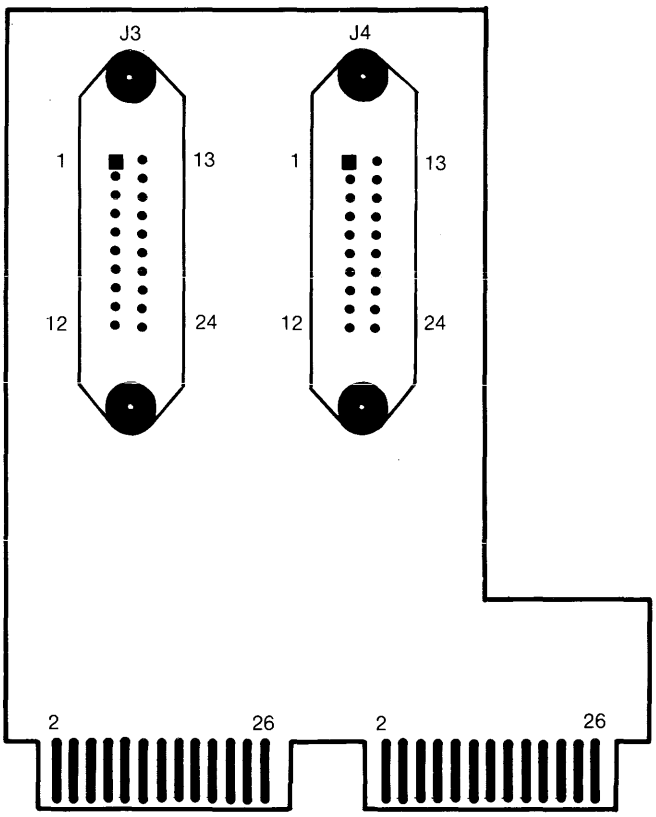
7933-341

Figure 5-13. DC Power PCA-A13 Layout



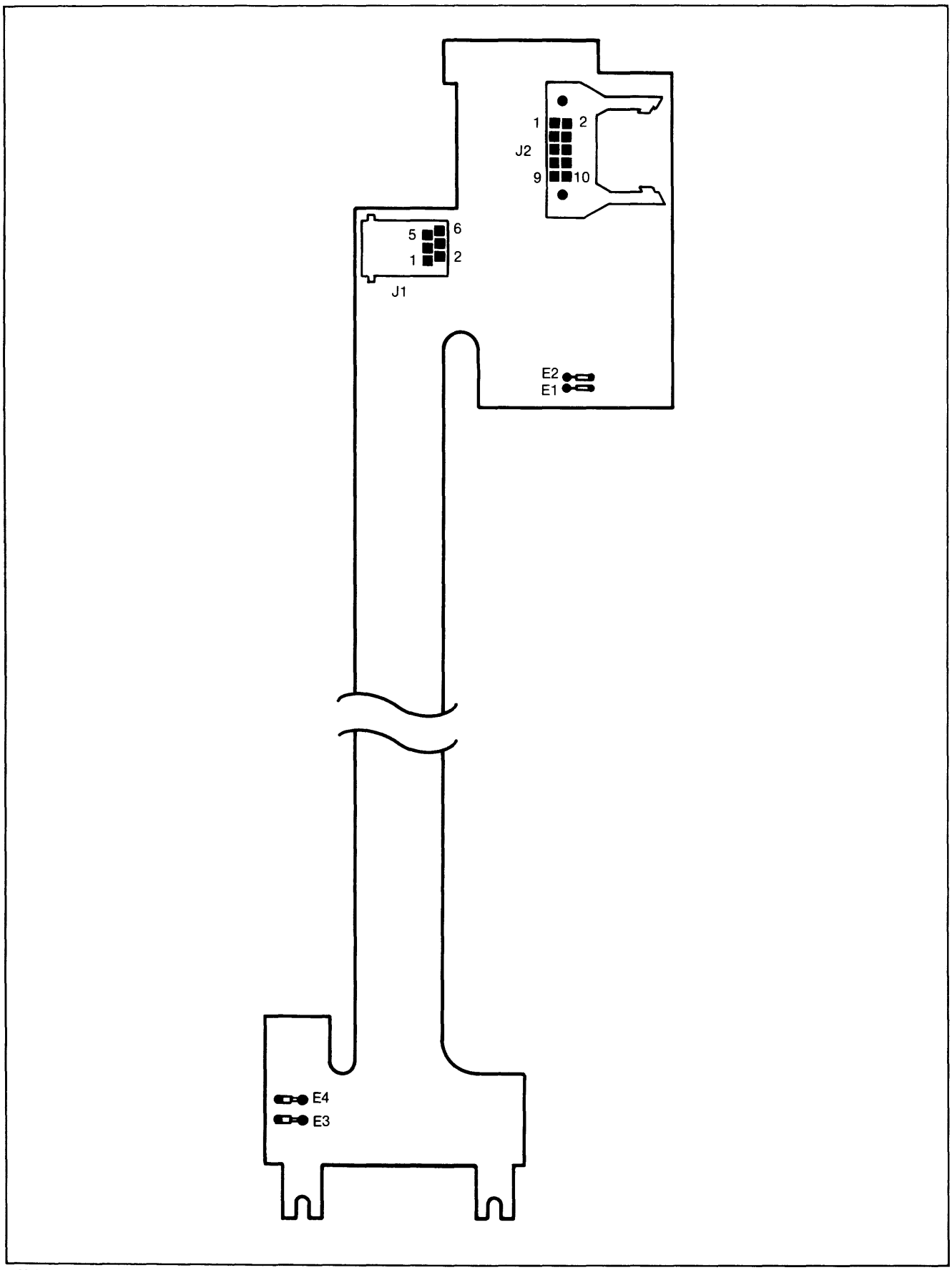
7933-342

Figure 5-14. Control Panel PCA-A14 Layout



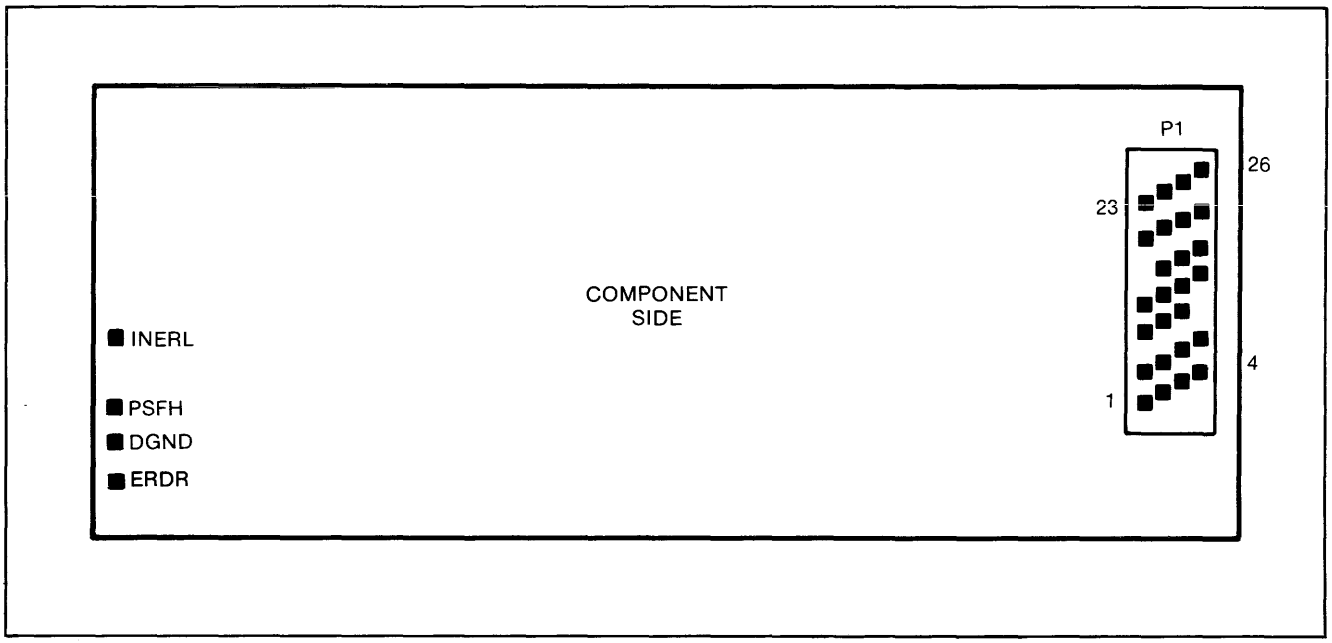
7933-343

Figure 5-15. HP-IB PCA-A17 Layout



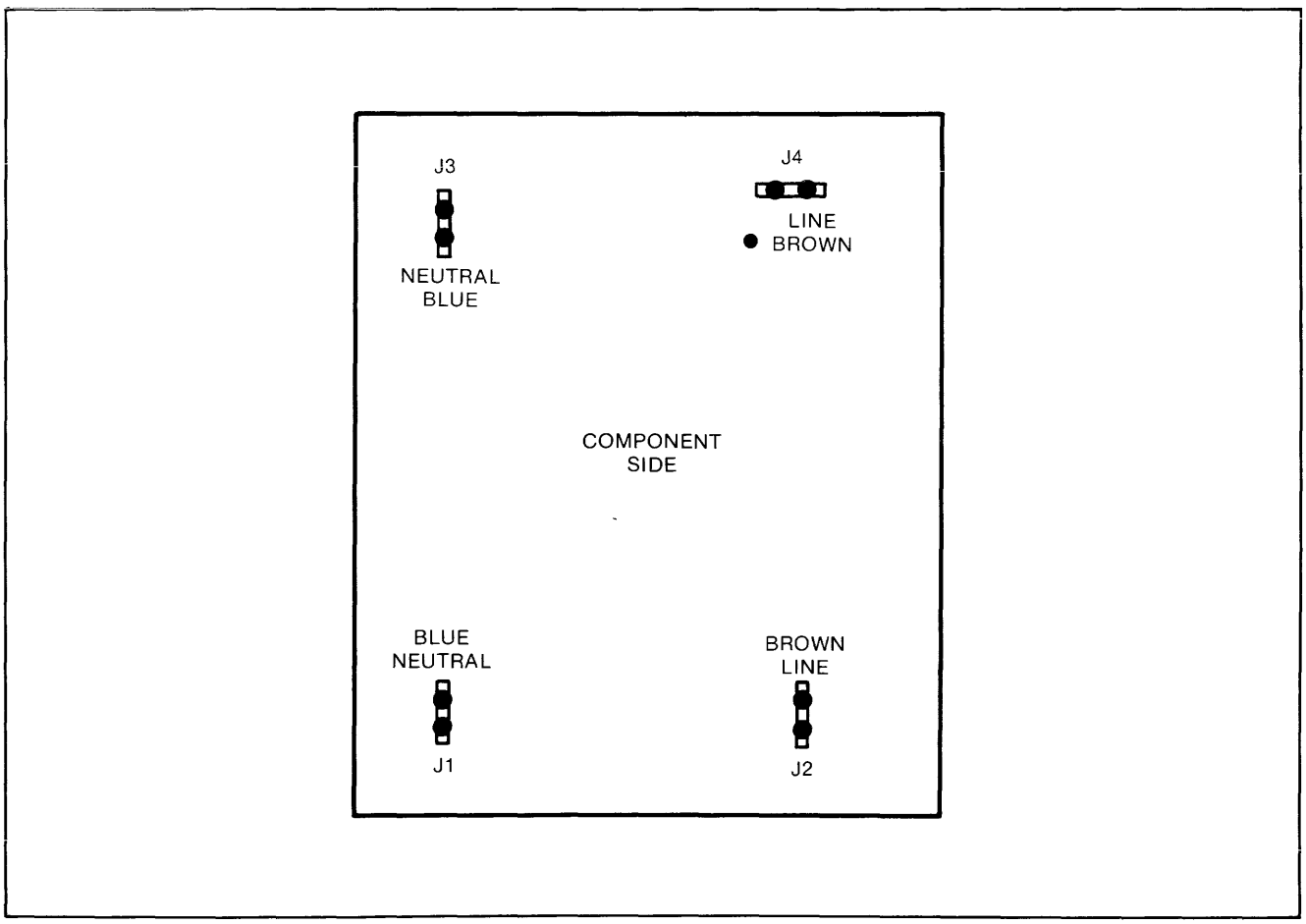
7933-344

Figure 5-16. Actuator Status PCA-A18 Layout



7933-346

Figure 5-17. Emergency Retract PCA-A20 Layout



7933-347

Figure 5-18. Line Filter PCA-A21 Layout

Table 5-10. Motherboard PCA-A11 Signal Distribution List

MNEMONIC	DESCRIPTION	REGULATOR PCA-A1(6)	ACTUATOR DRIVER PCA-A2(4)	SERVO PCA-A3(4)
		XA1P1	XA2P1	XA3P1
A0-H	Address Bus, bit 0	13	13	13
A1-H	Address Bus, bit 1	14	14	14
A2-H	Address Bus, bit 2		15	15
A3-H	Address Bus, bit 3		16	16
A4-H	Address Bus, bit 4			
A5-H	Address Bus, bit 5			
A6-H	Address Bus, bit 6			
A7-H	Address Bus, bit 7			
A8-H	Address Bus, bit 8			
A9-H	Address Bus, bit 9			
A10-H	Address Bus, bit 10			
A11-H	Address Bus, bit 11			
ACTSL-L	Actuator Select		37	
ACTTST	Actuator Test		[115]	
ACUR	Actuator Current		109	109
BF1SL-L	Buffer 1 Select			
BR0-H	Revision Register, bit 0			
BR1-H	Revision Register, bit 1			
BR2-H	Revision Register, bit 2			
BR3-H	Revision Register, bit 3			
BR4-H	Revision Register, bit 4			
BR5-H	Revision Register, bit 5			
BR6-H	Revision Register, bit 6			
BR7-H	Revision Register, bit 7			
CCOM	Current Command		105	105
CRB-L	Carriage Back			85
D0-H	Data Bus, bit 0	[3]	[3]	[3]
D1-H	Data Bus, bit 1	[4]	[4]	[4]
D2-H	Data Bus, bit 2	[5]	[5]	[5]
D3-H	Data Bus, bit 3	[6]	[6]	[6]
D4-H	Data Bus, bit 4	[7]	[7]	[7]
D5-H	Data Bus, bit 5	[8]	[8]	[8]
D6-H	Data Bus, bit 6	[9]	[9]	[9]

NOTES: 1. Number within parenthesis following the PCA reference designation is the service reference number of the functional block diagram where the PCA is documented.

2. Number within brackets indicates signal source.

Table 5-10. Motherboard PCA-A11 Signal Distribution List (continued)

MNEMONIC	MICRO-PROCESSOR PCA-A4(1)	DMA PCA-A6(5)	FORMATTER/ SEPARATOR PCA-A8(5)	TRACK FOLLOWER PCA-A9(4)	READ/ WRITE PCA-A10(5)	J25
	XA4P1	XA6P1	XA8P1	XA9P1	XA10P1	
A0-H	[13]	13	13	13		9
A1-H	[14]	14	14	14		10
A2-H	[15]	15	15	15		
A3-H	[16]	16	16	16		
A4-H	[17]	17				
A5-H	[18]	18				
A6-H	[19]	19				
A7-H	[20]	20				
A8-H	[21]	21				
A9-H	[22]	22				
A10-H	[23]	23				
A11-H	[24]	24				
ACTSL-L	[37]					
ACTTST	115					
ACUR						
BF1SL-L	[27]	28				
BR0-H			17		[17]	
BR1-H			18		[18]	
BR2-H			19		[19]	
BR3-H			20		[20]	
BR4-H			21		[21]	
BR5-H			22		[22]	
BR6-H			23		[23]	
BR7-H			24		[24]	
CCOM						
CRB-L					85	
D0-H	[3]	[3]	[3]	[3]		[1]
D1-H	[4]	[4]	[4]	[4]		[2]
D2-H	[5]	[5]	[5]	[5]		[3]
D3-H	[6]	[6]	[6]	[6]		[4]
D4-H	[7]	[7]	[7]	[7]		[5]
D5-H	[8]	[8]	[8]	[8]		[6]
D6-H	[9]	[9]	[9]	[9]		[7]

Table 5-10. Motherboard PCA-A11 Signal Distribution List (continued)

MNEMONIC	DESCRIPTION	REGULATOR PCA-A1(6)	ACTUATOR DRIVER PCA-A2(4)	SERVO PCA-A3(4)
		XA1P1	XA2P1	XA3P1
D7-H	Data Bus, bit 7	[10]	[10]	[10]
DCNW-H	DC With No Write			
DM2IN-L	DMA 2 Interlock			
DM1SL-L	DMA 1 Select			
DOPEN-H	Door Open			24
DSOS-L	Delayed Start Of Sector			
DCP-L	Delayed Clock Pulse			
EC1SL-L	ECC 1 Select			
EOS-L	End Of Sector			
ER-H	Emergency Retract		[98]	
FCLR-L	Fault Clear			
FIN-H	Formatter/Separator Input			
FLW-L	Follow			
FOUT-H	Formatter/Separator Output			
FPOS	Fast Position			117
FSSEL-L	Formatter/Separator Select			
FUNER-L	Formatter/Separator Uncorrectable Error			
HAEN-H	Head Alignment Enable			
HAENR-H	Head Alignment Enable Reset			
HS0-H	Head Select, bit 0			
HS1-H	Head Select, bit 1			
HS2-H	Head Select, bit 2			
HS3-H	Head Select, bit 3			
IL1-L	Interlock, line 1	84		
IL2-L	Interlock, line 2	82	82	
IL3-L	Interlock, line 3		80	80
IL4-L	Interlock, line 4			84
IL5-L	Interlock, line 5			
IL6-L	Interlock, line 6			
IL7-L	Interlock, line 7			
IL8-L	Interlock, line 8			
IL9-L	Interlock, line 9			
IL10-L	Interlock, line 10			

NOTES: 1. Number within parenthesis following the PCA reference designation is the service reference number of the functional block diagram where the PCA is documented.

2. Number within brackets indicates signal source.

Table 5-10. Motherboard PCA-A11 Signal Distribution List (continued)

MNEMONIC	MICRO-PROCESSOR PCA-A4(1)	DMA PCA-A6(5)	FORMATTER/ SEPARATOR PCA-A8(5)	TRACK FOLLOWER PCA-A9(4)	READ/ WRITE PCA-A10(5)	J25
	XA4P1	XA6P1	XA8P1	XA9P1	XA10P1	
D7-H	[10]	[10]	[10]	[10]		[8]
DCNW-H			28		[28]	
DM2IN-L	101					
DM1SL-L	[29]	30				
DOPEN-H	[92]					
DSOS-L			[39]		39	
DCP-L				91	[91]	
EC1SL-L	[41]	41				
EOS-L		[88]	88			
ER-H	98				98	
FCLR-L			[35]		35	
FIN-H		[34]	34			
FLW-L			104		104	
FOUT-H		38	[38]			
FPOS				117		
FSSEL-L	[36]		36			
FUNER-L		43	[44]			
HAEN-H			[102]		102	
HAENR-H			[32]		32	
HS0-H			[109]		109	
HS1-H			[110]		110	
HS2-H			[111]		111	
HS3-H			[112]		112	
IL1-L						22
IL2-L						
IL3-L						
IL4-L	84					
IL5-L						
IL6-L	83	82				
IL7-L						
IL8-L		79	80			
IL9-L				81		
IL10-L			81	82	82	

Table 5-10. Motherboard PCA-A11 Signal Distribution List (continued)

MNEMONIC	DESCRIPTION	REGULATOR PCA-A1(6)	ACTUATOR DRIVER PCA-A2(4)	SERVO PCA-A3(4)
		XA1P1	XA2P1	XA3P1
IL11-L	Interlock, line 11			
IO1SL-L	I/O 1 Select			
IO2SL-L	I/O 2 Select			
IP-L	Index Pulse			
LIN-H	Amplifier Is Linear		101	101
LSB-H	Least Significant Bit			
MA0-H	Multiplex, bit 0			
MA1-H	Multiplex, bit 1			
MA2-H	Multiplex, bit 2			
MBSEL-L	Motherboard Select			
MHF-H	Multiple Head Fault			
MRST-L	Master Reset	[86]	86	86
NMI-L	Non-Maskable Interrupt			
OFTRK-H	Off Track			[97]
PWRDN-H	Power Down	[99]		
RDD-H	Read Data			
RD-L	Read	11	11	11
REGSL-L	Regulator Select	38		
RWBR-L	Read/Write Register Select			
RWC-L	Read/Write Clock			
RWFLT-H	Read/Write Fault			
RWTST	Read/Write Test			
SOD-L	Start Of Data			
SOS-L	Start Of Sector			
SPDDN-H	Speed Down		91	
SPDSL-L	Spindle Select			
SPDS	Slow Position			115
SPSPD-H	Spindle Speed			
SRVSL-L	Servo Select			34
SRVTST	Servo Test			[116]
ST-H	Self Test			
STO-L	Self Test Offset			
TDCP-L	Self Test Data Clock Pulse			

NOTES: 1. Number within parenthesis following the PCA reference designation is the service reference number of the functional block diagram where the PCA is documented.

2. Number within brackets indicates signal source.

Table 5-10. Motherboard PCA-A11 Signal Distribution List (continued)

MNEMONIC	MICRO-PROCESSOR PCA-A4(1)	DMA PCA-A6(5)	FORMATTER/ SEPARATOR PCA-A8(5)	TRACK FOLLOWER PCA-A9(4)	READ/ WRITE PCA-A10(5)	J25
	XA4P1	XA6P1	XA8P1	XA9P1	XA10P1	
IL11-L						
IO1SL-L	[31]	32				
IO2SL-L	[32]					
IP-L				87		
LIN-H						
LSB-H			[103]		103	
MA0-H			[106]		106	
MA1-H			[107]		107	
MA2-H			[108]		108	
MBSEL-L	[40]					
MHF-H			30		[30]	
MRST-L	86	86	86	86	86	21
NMI-L	[75]	75				
OFTRK-H	97				97	
PWRDN-H	99					
RDD-H			37		[37]	
RD-L	[11]	11	11	11		13
REGSL-L	[38]					
RWBR-L			[41]		41	
RWC-L		42	[42]			
RWFLT-H	100				[100]	
RWTST	117				[117]	
SOD-L		90	[90]			
SOS-L	85	85	85	[85]		
SPDDN-H	91					[23]
SPDSL-L	[39]					17
SPDS				115		
SPSPD-H	108					[20]
SRVSL-L	[34]					
SRVTST	116					
ST-H			[101]		101	
STO-L			[105]		105	
TDCP-L			[116]		116	

Table 5-10. Motherboard PCA-A11 Signal Distribution List (continued)

MNEMONIC	DESCRIPTION	REGULATOR PCA-A1(6)	ACTUATOR DRIVER PCA-A2(4)	SERVO PCA-A3(4)
		XA1P1	XA2P1	XA3P1
TFFLT-H	Track Follower Fault			
TFSEL-L	Track Follower Select			
TFTST	Track Follower Test			
WC0-H	Write Current, bit 0			
WC1-H	Write Current, bit 1			
WC2-H	Write Current, bit 2			
WDD-H	Write Data			
WENC-L	Read/Write Enable			
WNAC-H	Write With No AC			
WNDC-L	Write With No DC			
WR-L	Write	12	12	12
540 Hz-H	540-Hz Clock			
4 MHz-H	4-MHz Clock			
+12TST	+12V Test	[113]		
-12TST	-12V Test	[114]		

NOTES: 1. Number within parenthesis following the PCA reference designation is the service reference number of the functional block diagram where the PCA is documented.
2. Number within brackets indicates signal source.

Table 5-10. Motherboard PCA-A11 Signal Distribution List (continued)

MNEMONIC	MICRO-PROCESSOR PCA-A4(1)	DMA PCA-A6(5)	FORMATTER/ SEPARATOR PCA-A8(5)	TRACK FOLLOWER PCA-A9(4)	READ/ WRITE PCA-A10(5)	J25
	XA4P1	XA6P1	XA8P1	XA9P1	XA10P1	
TFFLT-H	94			[94]	94	
TFSEL-L	[33]			33		
TFTST	118			[118]		
WC0-H			[113]		113	
WC1-H			[114]		114	
WC2-H			[115]		115	
WDD-H			[33]		33	
WENC-L			[43]		43	
WNAC-H			27		[27]	
WNDC-L			29		[29]	
WR-L	[12]	12	12	12		15
540 Hz-H	[44]					19
4 MHz-H	[89]			89	89	
+12TST	113					
-12TST	114					

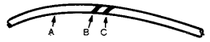
Table 5-11. Motherboard PCA-A11 Power Distribution List

PCA*	+5V	+12V	-12V	GROUND
A1(6) Regulator XA1P1	47, 48, 73, 74, 89 - 92, 97, 98, 100 - 106, 109 - 112	71, 72, 75, 76	49, 50	1, 2, 17, 18, 21 - 26, 31 - 37, 39 - 46, 77, 78, 95, 96, 115, 116, 119, 120
A2(4) Actuator Driver XA2P1	47, 48, 73, 74	71, 72	49, 50	1, 2, 17, 18, 21 - 28, 31 - 36, 38 - 46, 77, 78, 89, 90, 92, 95 - 97, 99, 100, 103, 104, 111 - 113, 116, 119, 120
A3(4) Servo XA3P1	47, 48, 73, 74	71, 72	49, 50	1, 2, 17, 18, 21 - 28, 31 - 33, 35 - 46, 77, 78, 89 - 92, 95, 98 - 100, 103, 104, 111 - 113, 119, 120
A4(1) Microprocessor XA4P1	47, 48, 73, 74	71, 72	49, 50	1, 2, 25, 26, 43, 45, 46, 77, 78, 90, 95, 96, 102 - 106, 109 - 112, 119, 120
A6(5) DMA XA6P1	47, 48, 73, 74	71, 72	49, 50	1, 2, 25, 26, 27, 31, 35, 36, 39, 40, 45, 46, 77, 78, 89, 91, 92, 95 - 106, 109 - 116, 119, 120
A8(5) Formatter/ Separator XA8P1	47, 48, 73, 74	71, 72	49, 50	1, 2, 25, 26, 40, 45, 46, 77, 78, 89, 91, 92, 95 - 100, 119, 120
A9(4) Track Follower XA9P1	47, 48, 73, 74	71, 72	49, 50	1, 2, 17, 18, 21 - 28, 31, 32, 34, 35 - 46, 77, 78, 88, 90, 92, 93, 95 - 106, 109 - 114, 116, 119, 120
A10(5) Read/Write XA10P1	47, 48, 73, 74	71, 72	49, 50	1 - 14, 25, 26, 34, 36, 38, 40, 42, 44, 45, 46, 77, 78, 83, 95, 96, 119, 120
Connector J25	25, 26			11, 12, 14, 16, 18

*Number within parenthesis following the PCA reference designation is the service reference number of the functional block diagram where the PCA is documented.

NOTES:

1. ENCIRCLED NUMBERS (c) INDICATE WIRING COLOR CODE AS FOLLOWS:

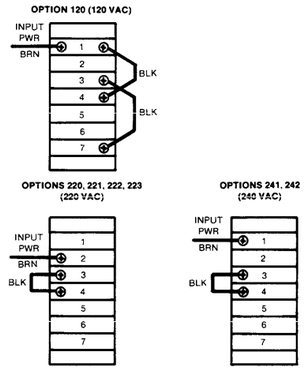


COLOR	A	B	C
BLACK	0	0	0
BROWN	1	1	1
RED	2	2	2
ORANGE	3	3	3
YELLOW	4	4	4
GREEN	5	5	5
BLUE	6	6	6
VIOLET	7	7	7
GRAY	8	8	8
WHITE	9	9	9

2. BLOWER POWER ASSEMBLY FUSE:

FUSE	DESCRIPTION	PART NO.
F1	7A, 250V, SB	2110-0640

3. TERMINAL BLOCK TB1 IS SHOWN STRAPPED FOR AN INPUT VOLTAGE OF 208 VAC (STANDARD) OPTIONAL STRAPPING IS SHOWN BELOW.



4. SPINDLE DRIVER PCA-A12 FUSES:

FUSE	DESCRIPTION	PART NO
F510 F520	30A, 125V 30A, 125V	2110-0661 2110-0661
F540 F550	15A, 250V, SB 15A, 250V, SB	2110-0327 2110-0327
F560 F570	7A, 250V, SB 7A, 250V, SB	2110-0640 2110-0640
F580 F590	10A, 250V 10A, 250V	2110-0051 2110-0051

5. CAPACITORS C1 AND C2 ARE MOUNTED ON THE POWER MODULE CASTING.

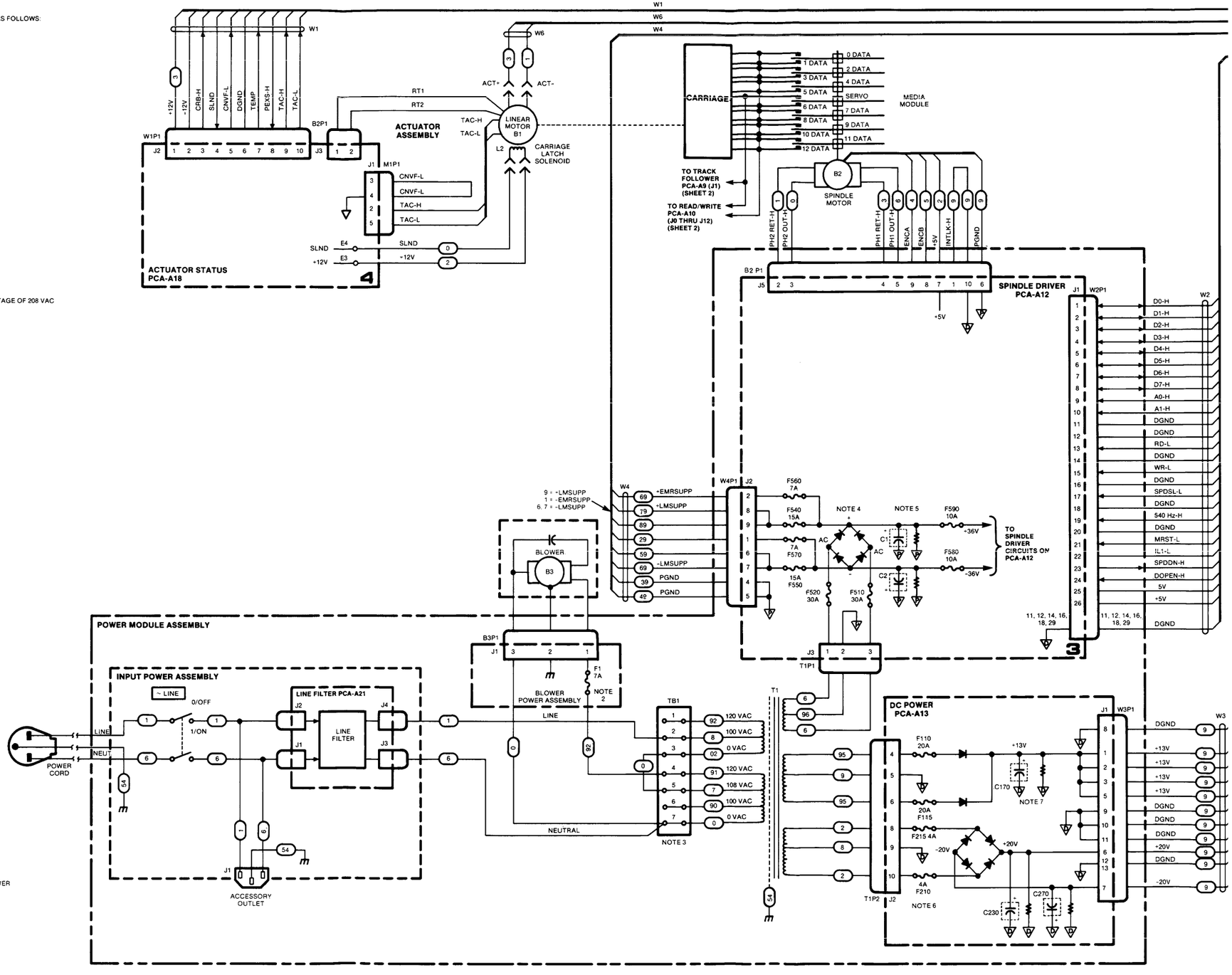
6. DC POWER PCA-A13 FUSES:

FUSE	DESCRIPTION	PART NO.
F110 F115	20A, 32V 20A, 32V	2110-0649 2110-0649
F210 F215	4A, 250V, SB 4A, 250V, SB	2110-0014 2110-0014

7 CAPACITORS C170, C230 AND C270 ARE MOUNTED ON THE POWER MODULE CASTING.

8 GROUNDS ARE INDICATED AS FOLLOWS:

- (A) ANALOG GROUND (AGND)
- (D) DIGITAL GROUND (DGND)
- (P) POWER GROUND (PGND)
- CHASSIS GROUND



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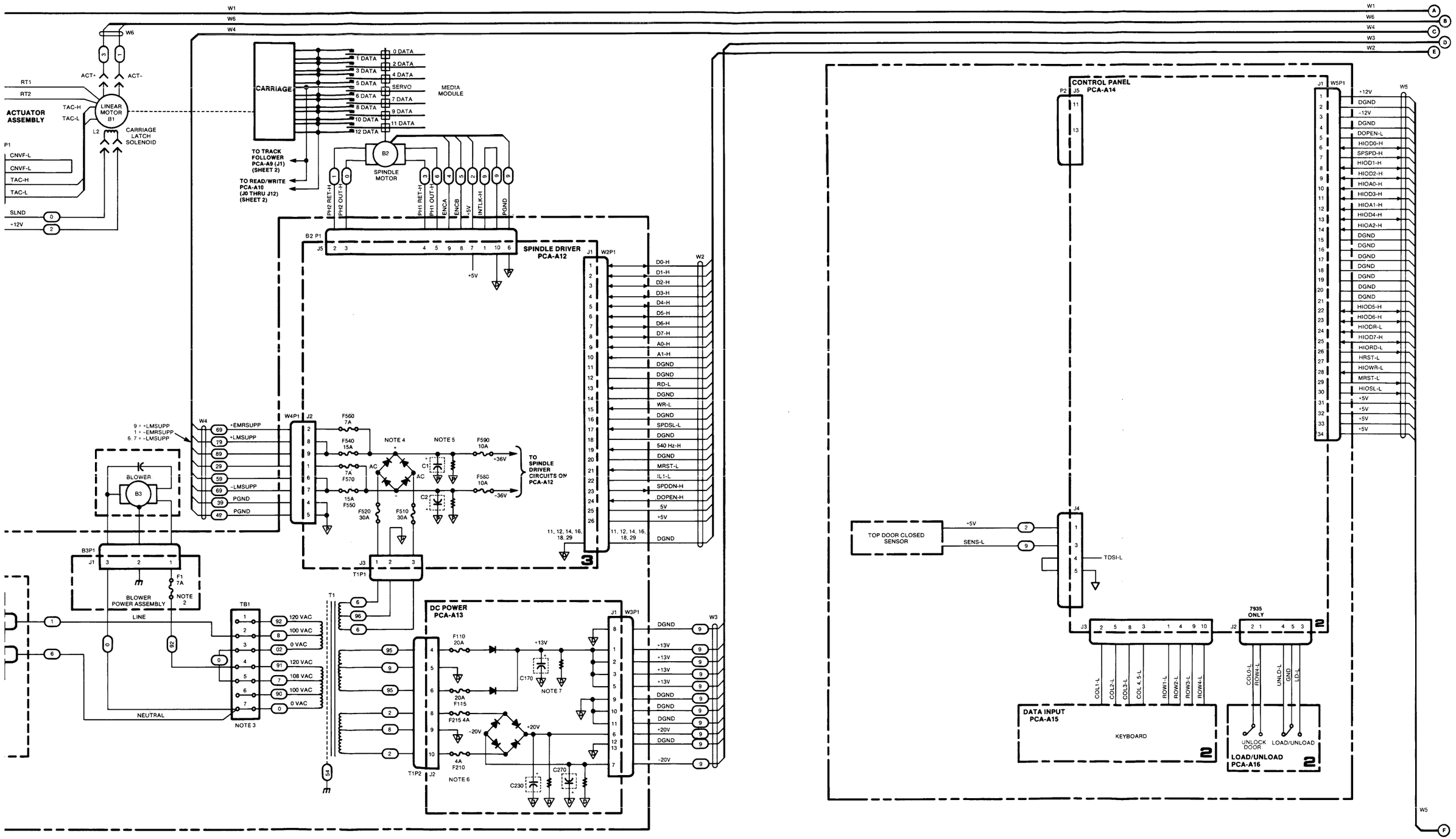
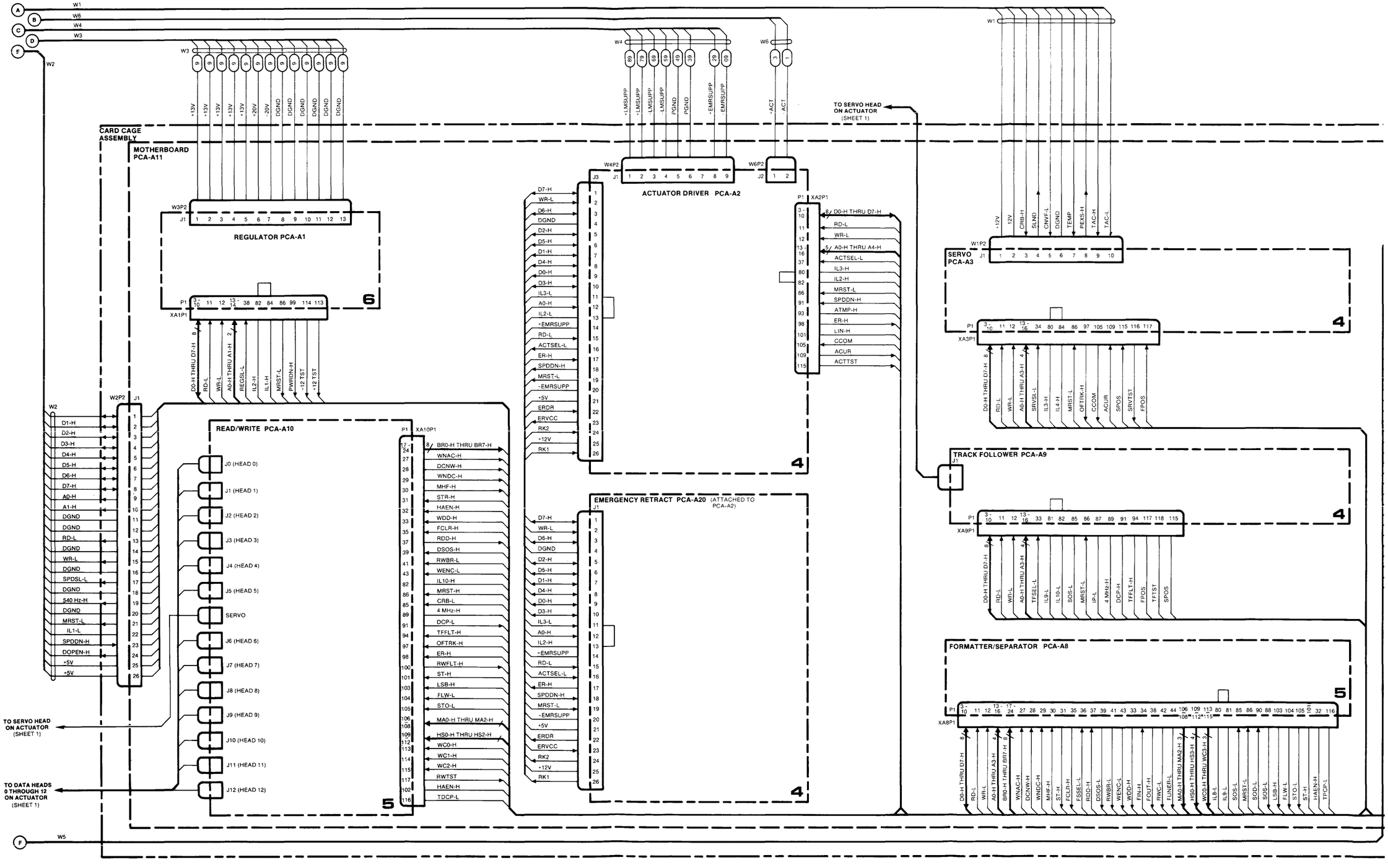


Figure 5-19. Disc Drive Wiring Diagram (Sheet 1 of 2)


W1
W6
W4
W3
W2
W5
CARD CAGE ASSEMBLY
MOTHERBOARD PCA-A11
+13V
-20V
DGND
W3P2
J1
REGULATOR PCA-A1
P1
XA1P1
D0-H THRU D7-H
RD-L
WR-L
A0-H THRU A1-H
REGSL-L
IL2-H
IL1-H
MRST-L
PWRDN-H
-12 TST
+12 TST
W2P2
D1-H
D2-H
D3-H
D4-H
D5-H
D6-H
D7-H
A0-H
A1-H
DGND
RD-L
WR-L
SPDSL-L
540 Hz-H
MRST-L
IL1-L
SPDDN-H
DOPEN-H
+5V
READ/WRITE PCA-A10
XA10P1
BR0-H THRU BR7-H
WNAC-H
DCNW-H
WNDC-H
MHF-H
STR-H
HAEN-H
WDD-H
FCLR-H
RDD-H
DSOS-H
RWBR-L
WENC-L
IL10-H
MRST-H
CRB-L
4 MHz-H
DCP-L
TFFLT-H
OFTRK-H
ER-H
RWFLT-H
ST-H
LSB-H
FLW-L
STO-L
MA0-H THRU MA2-H
HS0-H THRU HS2-H
WC0-H
WC1-H
WC2-H
RWTST
HAEN-H
TDCP-L
J0 (HEAD 0)
J1 (HEAD 1)
J2 (HEAD 2)
J3 (HEAD 3)
J4 (HEAD 4)
J5 (HEAD 5)
SERVO
J6 (HEAD 6)
J7 (HEAD 7)
J8 (HEAD 8)
J9 (HEAD 9)
J10 (HEAD 10)
J11 (HEAD 11)
J12 (HEAD 12)
TO SERVO HEAD ON ACTUATOR (SHEET 1)
TO DATA HEADS 0 THROUGH 12 ON ACTUATOR (SHEET 1)
-LMSUPP
+LMSUPP
PGND
+EMRSUPP
-EMRSUPP
+ACT
-ACT
W4P2
W6P2
J3
J2
ACTUATOR DRIVER PCA-A2
D7-H
WR-L
D6-H
DGND
D2-H
D5-H
D1-H
D4-H
D0-H
D3-H
IL3-L
A0-H
IL2-L
+EMRSUPP
RD-L
ACTSEL-L
ER-H
SPDDN-H
MRST-L
-EMRSUPP
+5V
ERDR
ERVCC
RK2
+12V
RK1
EMERGENCY RETRACT PCA-A20 (ATTACHED TO PCA-A2)
P1
XA2P1
D0-H THRU D7-H
RD-L
WR-L
A0-H THRU A4-H
ACTSEL-L
IL3-H
IL2-H
MRST-L
SPDDN-H
ATMP-H
ER-H
LIN-H
CCOM
ACUR
ACTTST
TO SERVO HEAD ON ACTUATOR (SHEET 1)
+12V
CRB-H
SLND
CNVF-L
DGND
TEMP
PEXS-H
TAC-H
TAC-L
W1P2
SERVO PCA-A3
XA3P1
D0-H THRU D7-H
RD-L
WR-L
A0-H THRU A3-H
SRVSL-L
IL3-H
IL4-H
MRST-L
OPTRK-H
CCOM
ACUR
SPOS
SRVTST
FPOS
TRACK FOLLOWER PCA-A9
J1
XA9P1
D0-H THRU D7-H
RD-L
WR-L
A0-H THRU A3-H
TFSEL-L
IL9-L
IL10-L
SOS-L
MRST-L
IP-L
4 MHz-H
DCP-H
TFFLT-H
FPOS
TFTST
SPOS
FORMATTER/SEPARATOR PCA-A8
XA8P1
D0-H THRU D7-H
RD-L
WR-L
A0-H THRU A3-H
BR0-H THRU BR7-H
WNAC-H
DCNW-H
WNDC-H
MHF-H
ST-H
FCLR-H
FSSEL-L
RDD-H
DSOS-L
RWBR-L
WENC-L
WDD-H
FIN-H
FOUT-H
RWC-L
FUNER-L
MA0-H THRU MA2-H
HS0-H THRU HS2-H
WC0-H THRU WC2-H
IL8-L
IL9-L
SOS-L
MRST-L
SOD-L
SOS-L
LSB-H
FLW-L
STO-L
ST-H
HAEN-H
TPCP-L

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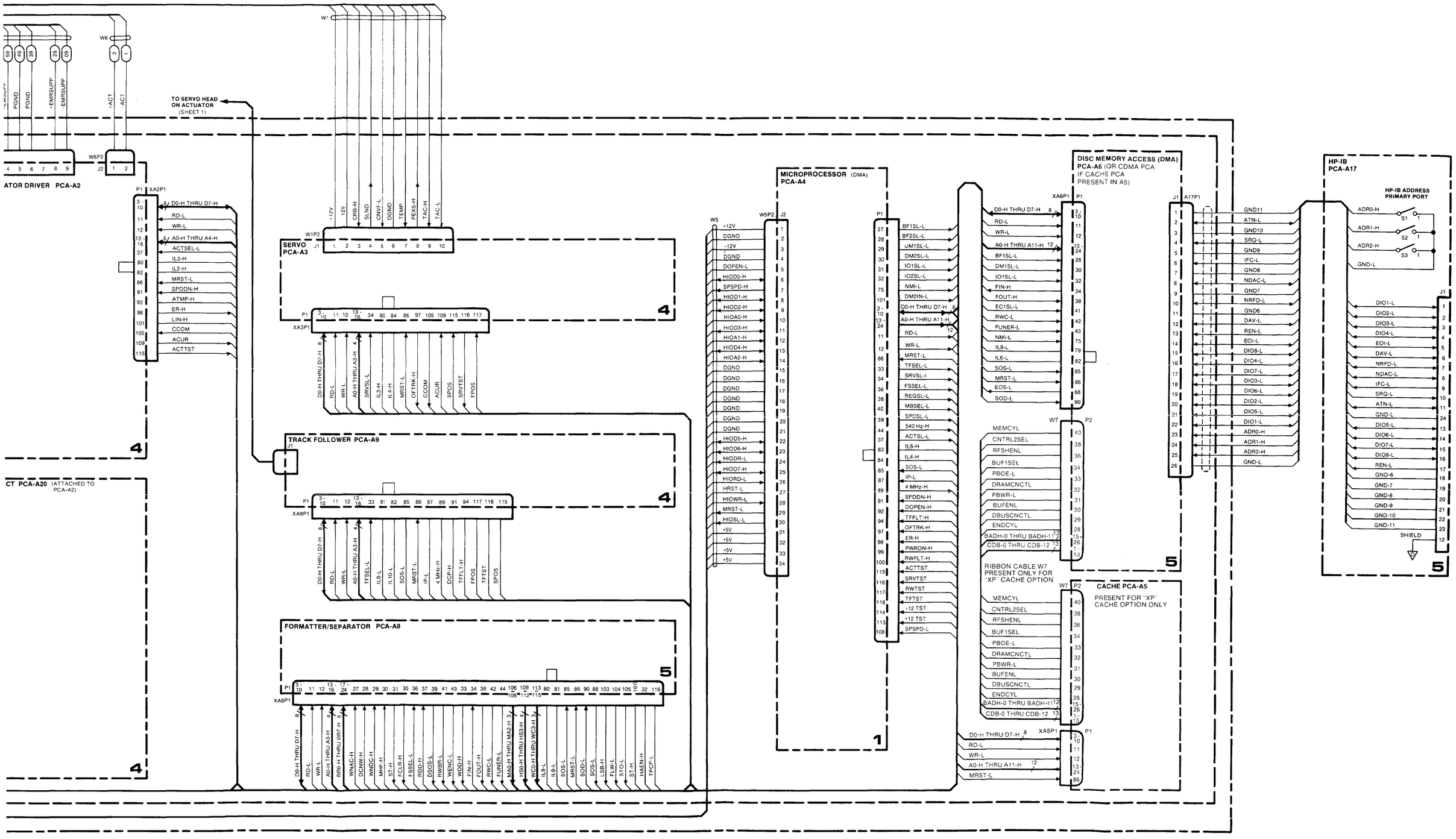

Figure 5-19. Disc Drive Wiring Diagram (Sheet 2 of 2)

Removal and Replacement

SECTION VI

6-1. INTRODUCTION

This section provides removal and replacement procedures for field replaceable assemblies and components in the disc drive. The procedures are given in the order in which disassembly normally occurs. Each assembly or component that must be removed before access can be gained to another assembly is listed first, followed by the next component that can be removed. References are provided to the exploded views in Section VII, Replaceable Parts, to assist in identifying and locating parts.

Note: TORX® hardware is used in the assembly of the disc drive. This hardware requires the use of special drivers (refer to table 3-1). In this manual, any reference to this type of hardware will be accompanied by the appropriate driver size (for example, T15).

6-2. PREPARATION FOR SERVICE

WARNING

The disc drive does not contain operator-serviceable parts. To prevent electrical shock, refer all installation and maintenance activities to qualified service-trained personnel.

CAUTION

- Do not turn the disc drive power on or off when the system bus is in an active state.
- Do not connect or disconnect the HP-IB cable from the disc drive when the system bus is in an active state.
- Observe the torque settings for attaching parts specified in the removal and replacement procedures. Failure to observe these settings may result in damage to the equipment.

Before starting any removal or replacement procedure, perform the following steps:

a. If the disc drive is in an operational state, set the LOAD/UNLOAD switch to the UNLOAD (out) position.

Note: If a BUSY message appears, wait until the system host releases the disc drive and again operate the LOAD/UNLOAD switch. If release is not obtained when the Activity indicator extinguishes, the system must be programmed to release the disc drive.

b. The disc drive will now begin a spin-down operation with the display indicating UNLOAD, SPIN DWN, and finally STOPPED.

c. When a STOPPED message appears, set the ~ LINE switch to the 0/OFF position.

d. Disconnect the disc drive power cord from the ac power source.

e. Disconnect the HP-IB cable from the disc drive.

6-3. SHROUD

To remove the shroud (1, figure 7-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Push in on the shroud latch (2) with a slotted-blade screwdriver or similar tool. When the latch releases, raise the rear of the shroud and then move the shroud forward and away from the disc drive.

To replace the shroud, perform the above steps in reverse order. Ensure that the shroud is latched in place before placing the disc drive in operation.

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6-4. FRONT AND REAR PANELS

To remove the front panel (6, figure 7-1) and the rear panel (5) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Slide the front panel (6) upward until it unlatches from the bottom of the disc drive cabinet and then remove the front panel.

e. Loosen the two 1/4-turn captive screws which secure the rear panel (5) to the disc drive cabinet and remove the rear panel.

To replace the front and rear panels, perform the above steps in reverse order.

6-5. PREFILTER

To remove the prefilter (7, figure 7-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Remove the front panel (6) from the disc drive. (Refer to paragraph 6-4.)

e. Raise the prefilter (7) upward until its lower edge is clear of the disc drive cabinet and then remove the prefilter.

To replace the prefilter, perform the above steps in reverse order. Before installing the prefilter, ensure that the airflow arrow on the edge of the filter is pointing toward the interior of the disc drive cabinet. The cleaning instructions described in Section III, Maintenance, must be performed before the disc drive is returned to service.

6-6. ABSOLUTE FILTER

To remove the absolute filter (24, figure 7-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Release the two fasteners (18, figure 7-1) which secure the absolute filter duct assembly (17) to the disc drive and remove the duct assembly.

e. Remove the absolute filter (24) from the disc drive cabinet. Tilt the absolute filter forward to clear the media module chamber assembly (25).

f. To replace the absolute filter, perform the above steps in reverse order. Before installation, check that the absolute filter is free of defects and that there is sealing tape around its edges. Check also that there is sealing tape (part nos. 0460-1286 [0.25 in. thick] and 0460-1287 [0.125 in. thick]) around the opening on the absolute filter duct assembly that mates with the media module chamber. If the sealing tape has deteriorated, replace it with the appropriate tape. The cleaning instructions described in Section III, Maintenance, must be performed before the disc drive is returned to service.

6-7. CONTROL PANEL ASSEMBLY

To remove the control panel assembly (11, figure 7-1) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Unplug cable W5 (10) from edge connector J1 on the right-hand side of the control panel assembly (11).

e. Loosen the two T10 screws (18, figure 7-2) which secure the door latch shield (8, figure 7-1) to the media module chamber (25) and remove the latch shield.

f. Unplug the three cables from connectors J3, J4, and J5 on the left-hand side of the control panel assembly (11).

g. Push on the control panel assembly (11) from behind until it releases from the two spring retainers (29, figure 7-2) on the media module chamber (25, figure 7-1) and then remove the control panel assembly.

To replace the control panel assembly, perform the above steps in reverse order. Tighten the T10 screws loosened in step e to 15 inch-pounds.

6-8. MEDIA MODULE

To remove a media module from an HP 7935 Disc Drive, refer to the *HP 7935 Disc Drive Operator Instructions,* part no. 07935-90901, or the *HP 7935 Disc Drive Operating and Installation Manual,* part no. 07935-90902. To remove a media module (24A, figure 7-1) from an HP 7933 Disc Drive, proceed as follows:

a. Perform steps a and b of the preparation for service procedure outlined in paragraph 6-2.

b. Remove the shroud. (Refer to paragraph 6-3.)

c. When the STOPPED message appears, release the top door latch, using a slotted blade screwdriver, and open the top door as shown in figure 6-1.

d. Remove the media module following the instructions given in figure 6-2.

e. Place the media module in its protective antistatic plastic bag, part no. 9222-0944.

To replace the media module in the disc drive, proceed as follows:

a. Connect the disc drive power cord to the ac power source.

b. Set the LOAD/UNLOAD switch to the UNLOAD (out) position and ~ LINE switch to 1/ON.

WARNING

All products which utilize the tape head cleaning solution are shipped with a Material Safety Data Sheet. Follow all applicable safety precautions when using the tape head cleaning solution.

c. Using cleaning wipes, part no. 9310-4865, moistened with tape head cleaning solution, part no. 8500-1251, clean the interior of the media module chamber (25, figure 7-1), the inside of the top door (7, figure 7-2), and the motor-spindle seal assembly (65, figure 7-1).

d. Using a cleaning wipe moistened with tape head cleaning solution, wipe clean the side and bottom surfaces of the media module (24A).

e. Carefully install the media module on the disc drive following the instructions given in figure 6-3.

f. Close the top door (7, figure 7-2) and ensure that it is locked.

g. Set the LOAD/UNLOAD switch to the LOAD (in) position.

h. The disc drive will now begin an internal diagnostic routine. The normal sequence of display messages will be: TESTING , SPIN UP , AIRPURGE (or PURGE), TESTING , and DRIVE *. If the routine does not complete, the reason will be indicated by any one of the following messages: DOOROPEN , MOD DOOR , NOMODULE , TEST ERR , MEM FAIL , FAULT , FILTER *, or RESEAT .

Note: The Airpurge (Purge) portion of the internal diagnostic routine will require approximately four minutes to complete.

i. If a TEST ERR , MEM FAIL , FAULT , FILTER * , RESEAT or NOCACH * message appears, a message in step h persists or other message appears, refer to Section V, Service Information, for additional information.

j. Replace the shroud (1, figure 7-1) and check that it is properly latched in place.

k. Perform the data surface verification test described in Section IV, Alignment and Adjustment, before placing the disc drive in service.

6-9. MEDIA MODULE CHAMBER

To remove the media module chamber (25, figure 7-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud (refer to paragraph 6-3) and then unplug cable W5 (10) from edge connector J1 on the right-hand side of the control panel assembly (11).

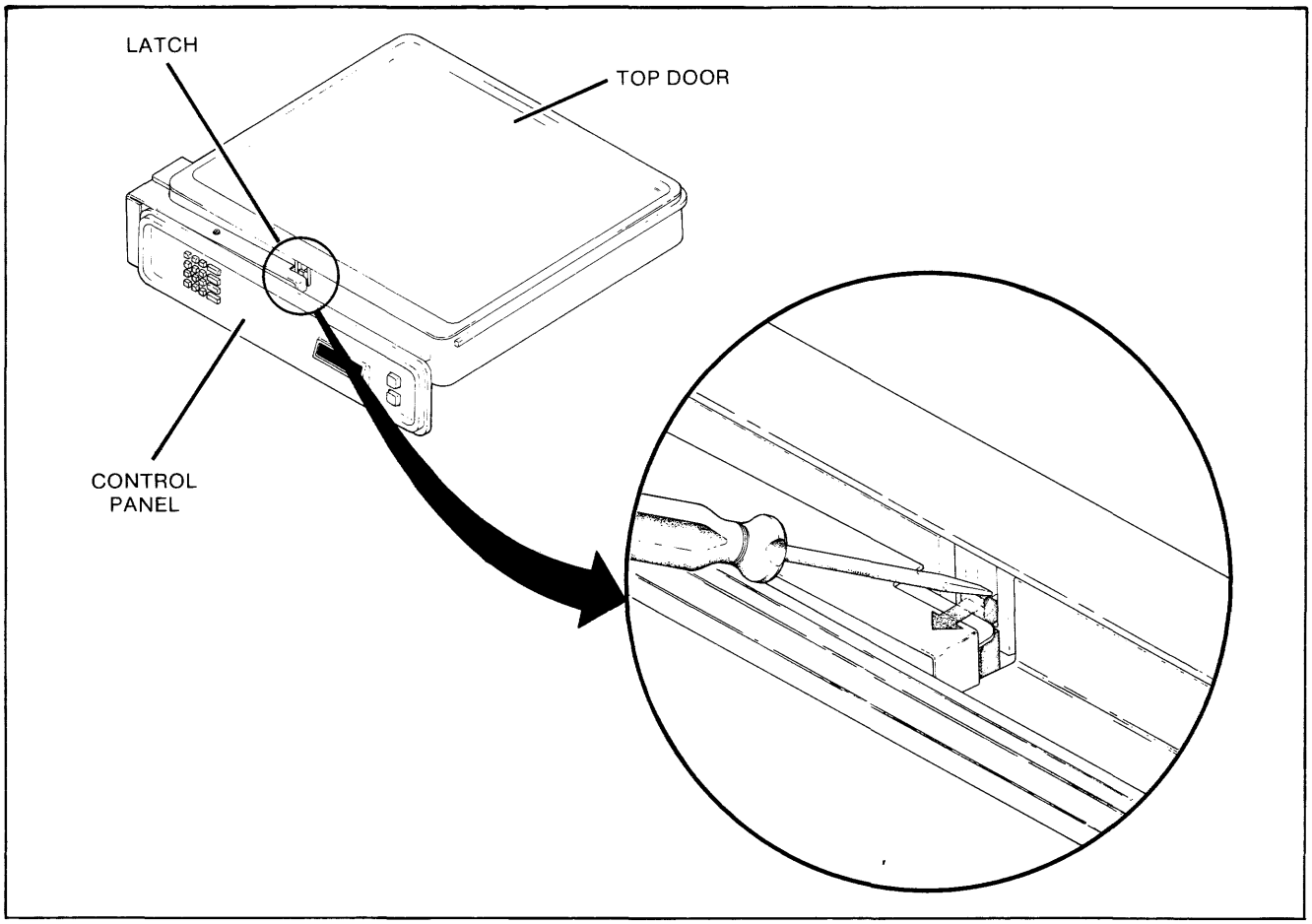
d. Remove the media module. (Refer to paragraph 6-8.)

e. Remove the head contamination shield. (Refer to paragraph 6-13.)

f. Remove the four T10 screws (25A) and two T9 screws (25B) which secure the media module chamber (25) to the cabinet assembly (86).

g. Lift up on the two latches that engage on the latch plates (69) and remove the media module chamber (25) from the disc drive.

Note: When installing a new media module chamber in a disc drive having a serial number prefix of 2319 or higher, remove the foam gasket material from



REF 7933-215

Figure 6-1. HP 7933 Disc Drive Top Door Latch Release

the cabinet on the ledge which surrounds the media module chamber opening (3 places).

To replace the media module chamber, perform the above steps in reverse order. Tighten the screws removed in step f to 10 inch-pounds.

6-10. MEDIA MODULE DOOR-OPENING LATCH

To remove the media module door-opening latch on the 7935 (31, figure 7-2), proceed as follows. (For 7933, door solenoid and shield have been replaced with a spring (23, figure 7-1)).

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud (refer to paragraph 6-3) and the media module chamber (refer to paragraph 6-9).

d. Press down on the media module door-opening latch (31) and remove the latch from the media module chamber.

To replace the media module door-opening latch, perform the above steps in reverse order.

6-11. TOP DOOR HINGES

To remove the top door hinges (9, figure 7-2), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

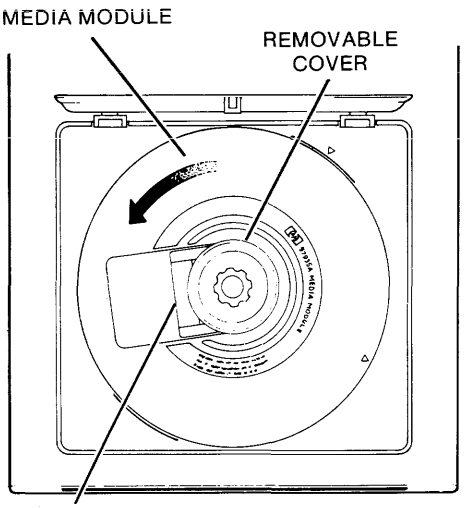
c. Remove the shroud (refer to paragraph 6-3) and the media module chamber (refer to paragraph 6-9).

d. Loosen the two T10 screws (18) which secure the door latch shield (8, figure 7-1) to the media module chamber and remove the door latch shield.

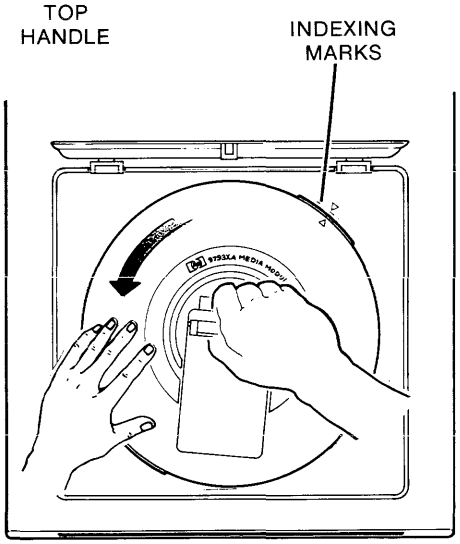
e. Manually operate the top door latch lever (22, figure 7-2) and open the top door (7).

f. Remove the six T25 screws (4), lock washers (5), and flat washers (6) which secure the top door (7) to the top door hinges (9).

1. REMOVE THE REMOVABLE COVER FROM THE MEDIA MODULE AND RAISE THE TOP HANDLE ON THE MEDIA MODULE.



2. USING BOTH HANDS, ROTATE THE MEDIA MODULE COUNTERCLOCKWISE UNTIL THE INDEXING MARKS ARE ALIGNED AS SHOWN OPPOSITE. WHEN PROPERLY ALIGNED, LIFT THE MEDIA MODULE FROM THE MODULE CHAMBER.

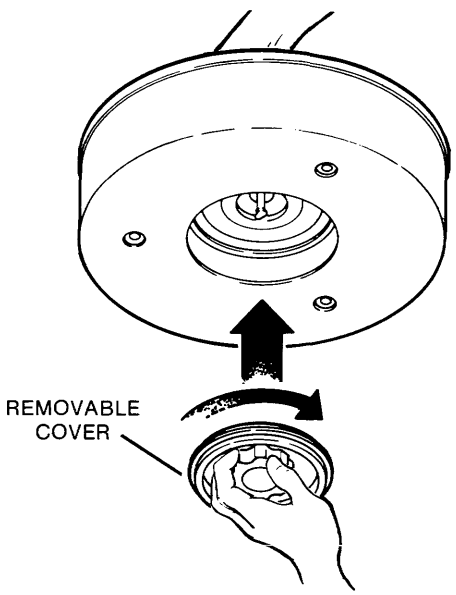


CAUTION

MEDIA MODULES SHOULD BE STORED FLAT IN A CLEAN DUST-FREE AREA. DO NOT STORE MORE THAN TWO HIGH.

3. HOLD THE MEDIA MODULE IN AN UPRIGHT POSITION AND ATTACH THE REMOVABLE COVER TO THE BOTTOM OF THE MODULE. LOCK THE COVER IN PLACE BY ROTATING IT CLOCKWISE.

4. PLACE THE MEDIA MODULE IN ITS PROTECTIVE ANTISTATIC PLASTIC BAG BEFORE STORING IT.



REF 7935

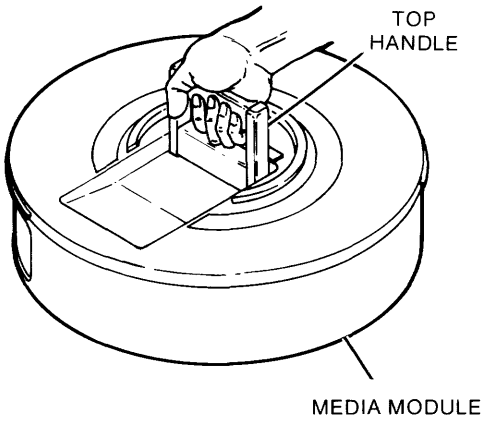
Figure 6-2. Media Module Removal

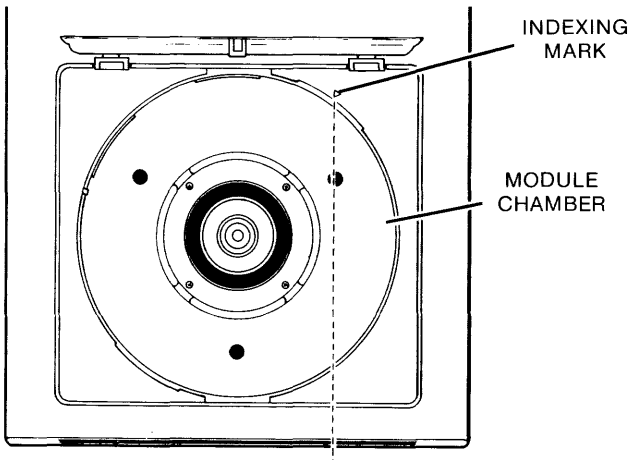
1. ON THE MEDIA MODULE TO BE INSTALLED, RAISE THE TOP HANDLE WITH ONE HAND WHILE HOLDING THE MEDIA MODULE UPRIGHT. THEN WITH THE OTHER HAND, TURN THE REMOVABLE COVER COUNTERCLOCKWISE AND DETACH THE COVER FROM THE MEDIA MODULE.

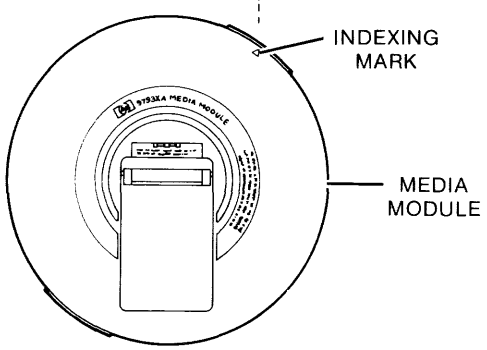
WARNING

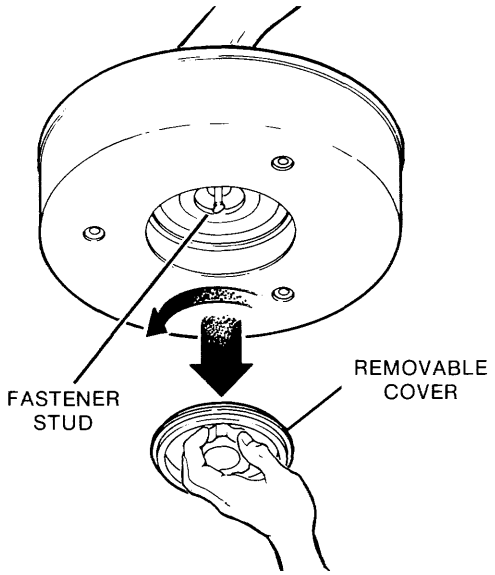
All products which utilize the tape head cleaning solution are shipped with a Material Safety Data Sheet. Follow all applicable safety precautions when using the tape head cleaning solution.

2. FOR THE HP 7933 ONLY, CLEAN THE FASTENER STUD, VISIBLE AT THE BOTTOM OF THE MODULE AFTER THE REMOVABLE COVER IS TAKEN OFF, WITH A CLEANING WIPE MOISTENED WITH TAPE HEAD CLEANING SOLUTION.

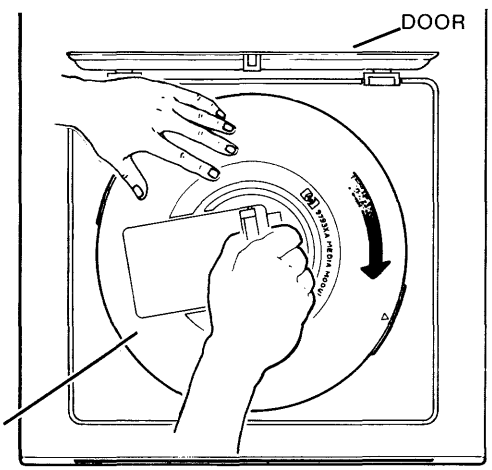








3. HOLDING THE MEDIA MODULE BY THE RAISED HANDLE, ALIGN THE INDEXING MARK ON THE MEDIA MODULE WITH THE INDEXING MARK ON THE MODULE CHAMBER, AS SHOWN OPPOSITE. WHEN PROPERLY ALIGNED, LOWER THE MEDIA MODULE INTO THE MODULE CHAMBER.



4. USING TWO HANDS, ROTATE THE MEDIA MODULE CLOCKWISE UNTIL IT STOPS.

5. LOWER THE TOP HANDLE EVENLY AND FIRMLY.

6. PLACE THE REMOVABLE COVER ON TOP (CENTER) OF THE MEDIA MODULE.

REF 7935

Figure 6-3. Media Module Replacement

g. Remove the eight T10 screws (8) which secure the hinges (9) and the RFI fingers (10, 11) to the media module chamber and remove the hinges and the RFI fingers.

To replace the top door hinges, proceed as follows:

a. Attach the hinges (9) and the RFI fingers (10, 11) to the media module chamber with the eight T10 screws (8) previously removed. Ensure that the RFI fingers are in the correct locations, as shown in figure 7-2. Tighten the screws (9) to 15 inch-pounds.

b. Attach the top door (7) to the hinges (9) with the six T25 screws (4), lock washers (5), and flat washers (6) previously removed. Tighten the screws to 10 inch-pounds.

c. Close the top door and check that it is properly aligned with the frame of the media module chamber. Open and close the top door a number of times to ensure that the door latch is operating correctly. If adjustment is needed, proceed as follows:

(1) Unlock the top door and remove the eight T9 screws (15) which secure the left-hand retainer (14) to the media module chamber.

(2) Remove the eight T9 screws (13) which secure the right-hand retainer (12) to the media module chamber.

(3) Loosen the six T25 screws (4) which secure the top door (7) to the two hinges (9).

(4) Close the top door and align it with the frame of the media module.

(5) When the top door is properly aligned, tighten the four T25 screws (4) accessible through the two slots in the media module chamber to 15 inch-pounds.

(6) Open the top door and tighten the remaining two T25 screws (4) to 15 inch-pounds.

(7) Attach the right- and left-hand retainers with the sixteen T9 screws previously removed. Tighten these screws to 5 inch-pounds.

(8) Open and close the top door a number of times to ensure that the door latch is operating correctly.

d. Replace the latch shield (8, figure 7-1) on the media module chamber. Tighten the two T10 screws (18, figure 7-2) to 15 inch-pounds.

6-12. CARD CAGE COVER

To remove the card cage cover (27, figure 7-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Unplug cable W6 (26) from the actuator assembly and from actuator driver PCA-A2 (33) in the card cage.

e. Loosen the two captive screws on the bracket which secures cable assembly W5 (10) to the card cage cover (27) and unplug W5 from microprocessor PCA-A4 (35) in the card cage.

f. Unplug the HP-IB PCA-A17 cable (46) from DMA PCA-A6 (36) in the card cage.

g. Loosen the four captive screws on the card cage cover (27) and remove the cover.

h. To replace the card cage cover, perform the above steps in reverse order. Tighten the four captive screws loosened in step g to 20 inch-pounds.

6-13. HEAD CONTAMINATION SHIELD

To remove the components of the head contamination shield (30, 31, figure 7-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Loosen the three captive screws which secure the right-hand head contamination shield (30) to the actuator assembly (80) and remove the shield.

e. Loosen the two captive screws which secure the left-hand head contamination shield (31) to the actuator assembly and remove the shield.

To replace the head contamination shield, perform the above steps in reverse order. Tighten the captive screws to 15 inch-pounds.

6-14. CARD CAGE PCA'S

To remove the card cage PCA's (32 through 39, figure 7-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud (refer to paragraph 6-3) and the card cage cover (refer to paragraph 6-12). If read/write PCA-A10 (39) is to be removed, remove the right-hand section of the head contamination shield (refer to paragraph 6-13).

d. On read/write PCA-A10 (39), unplug the data head cables from connectors to J0 through J12. Next, loosen the two captive screws which secure PCA-A10 to the adjacent shield (44), and remove PCA-A10 from the card cage.

e. On track follower PCA-A9 (38), unplug the servo head cable from connector J1.

f. On servo PCA-A3 (34), lift the PCA partially out of the card cage, remove connector clip (29), and unplug cable W1 (28) from connector J1.

g. On actuator driver PCA-A2 (33), unplug cable W4 (48) from connector J1.

h. On regulator PCA-A1 (32), unplug cable W3 (47) from connector J1.

i. Simultaneously lift up on the two PCA extractors and slide the PCA up and out of the card cage chassis.

To replace a PCA in the card cage, proceed as follows:

CAUTION

Ensure that the correct replacement PCA is installed in its corresponding card slot, otherwise damage to the PCA may result.

a. Insert the replacement PCA into the card cage. Press the PCA firmly into the connector on the motherboard until it is firmly seated. On read/write PCA-A10 (39), tighten the two captive screws which secure the PCA to the adjacent shield (44).

b. Reconnect the thirteen data head cables to connectors J0 through J12 on read/write PCA-A10 (39), the servo head cable to connector J1 on track follower PCA-A9 (38), cable W1 (28) to connector J1 on servo PCA-A3 (34), cable W4 (48) to connector J1 on actuator driver PCA-A2 (33) and cable W3 (47) to connector J1 on regulator PCA-A1 (32).

Note: 1. If regulator PCA-A1 (32) is replaced, it will be necessary to perform the power supply adjustment check before returning the disc drive to service. (Refer to Section IV, Alignment and Adjustment, for details.)

2. If actuator driver PCA-A2 (33) or servo PCA-A3 (34) is replaced, it will be necessary to perform the seek deceleration adjustment procedure before returning the disc drive to service. (Refer to Section IV, Alignment and Adjustment, for details.)

c. Replace the card cage cover. Check that the servo head cable connected to track follower PCA-A9 and cable W1 connected to servo PCA-A3 are located in the appropriate slots on the edge of the card cage cover before securing the cover in place.

d. Connect cable W6 (26) to the actuator assembly and actuator driver PCA-A2 (33); cable W5 (10) to microprocessor PCA-A4 (35); and the cable from HP-IB PCA-A17 (46) to DMA PCA-A6 (36).

e. Attach the brackets which secure cable W5 (10) and the cable from HP-IB PCA-A17 (46) to the card cage.

f. Replace the right-hand section of the head contamination shield (30) and install the shroud (1).

6-14A. FIRMWARE UPGRADE KIT

To remove the disc drive firmware from microprocessor PCA-A4 (35, figure 7-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Remove the card cage cover. (Refer to paragraph 6-12.)

e. On microprocessor PCA-A4 (35), simultaneously lift up on the two PCA extractors and slide the PCA up and out of the card cage chassis.

f. Before handling the ROM's in the upgrade kit, securely attach a ground strap to ground on the disc drive and to your wrist. The ground strap is available in the ground kit, part no. 9300-0794.

g. Remove the ROM integrated circuit (IC) chips using one of the two following methods:

(1) On PCA's which have standard IC sockets (identified by being the same length as the ROM chip), use the IC extractor tool, part no. 8710-1213, to remove the ROM chips.

(2) On PCA's which have the zero extraction force sockets (identified by being longer than the ROM chip), insert a small screwdriver in the slot at the end of the IC socket and press downward on the catch (see figure 6-3A). Slowly slide the socket the full extent of its travel. The ROM chip is now released for easy removal.

To install a firmware upgrade kit, proceed as follows:

a. Install the new firmware ROM chips in the appropriate sockets (see figure 5-6); for example, if the ROM chip has the number 82062 (8xxx2, in figure 5-6) stamped on it, install this ROM in the socket labelled U182.

Note: The ROM chips cannot be ordered individually; the complete firmware upgrade kit must be ordered. Refer to table 7-1 for the kit part number.

b. Insert microprocessor PCA-A4 into the card cage.

c. Replace the card cage cover. Check that the servo head cable, connected to track follower PCA-A9, and cable W1, connected to servo PCA-A3, are located in the appropriate slots on the edge of the card cage before securing the cover in place.

d. Connect cable W6 (26) to the actuator assembly and actuator driver PCA-A2 (33); cable W5 (10) to microprocessor PCA-A4 (35); and the cable from HP-IB PCA-A17 (46) to DMA PCA-A6 (36).

e. Attach the brackets which secure cable W5 (10) and the cable from HP-IB PCA-A17 (46) to the card cage.

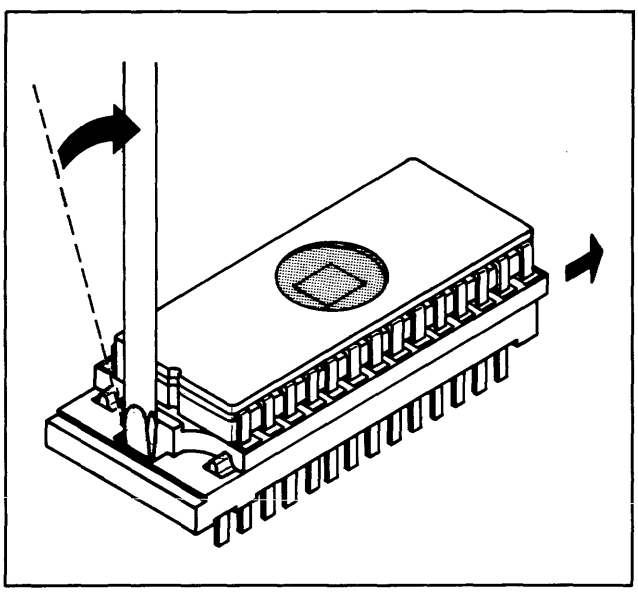


Figure 6-3A. ROM Chip Removal

f. Replace the shroud. Ensure that the shroud is latched in place before placing the disc drive in operation.

6-15. CARD CAGE CHASSIS AND MOTHERBOARD PCA-A11

To remove the card cage chassis (57, figure 7-1) and motherboard PCA-A11 (56), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud (refer to paragraph 6-3), the front and rear panels (refer to paragraph 6-4), and the prefilter (refer to paragraph 6-5).

d. Remove the media module chamber (refer to paragraph 6-9), the card cage cover (refer to paragraph 6-12), and all of the card cage PCA's (refer to paragraph 6-14).

e. Remove the two T15 screws (45) which secure HP-IB PCA-A17 (46) to the disc drive cabinet and remove PCA-A17.

f. Remove the T9 screw (40) which secures the RFI shield (42) to the disc drive.

g. Remove the three T20 screws (41) which secure the RFI shield (42) to the PCA-A10 shield (44) and remove the RFI shield.

h. Remove the two T15 screws (43) which secure the PCA-A10 shield (44) to the disc drive. Move the shield back toward the rear of the disc drive until it unlatches from the card cage (57) and then remove the shield.

i. Remove the twelve T25 screws (51) which secure the power module cover (52) to the disc drive cabinet and remove the cover.

j. Disconnect the blower (61) cable and the motor-spindle (67) cable from the power module connectors at the rear of the prefilter chamber.

k. Unplug cable W2 (53) from connector J25 on motherboard PCA-A11 (56). Close the retainers on the connector.

l. Unplug cable W3 (47) from connector J1 on dc power PCA-A13 (15, figure 7-4) and cable W4 (48, figure 7-1) from connector J1 on spindle driver PCA-A12 (6, figure 7-4). Remove cables W3 and W4 from the card cage and cable W6 from the actuator assembly.

m. Remove the T10 screw (70, figure 7-1) which secures the servo cable retainer (71) to the actuator assembly (80).

n. Remove the card cage chassis (57, figure 7-1) from the disc drive.

o. Remove the fourteen T8 screws (54) which secure the shield (55) and motherboard PCA-A11 (56) to the card cage chassis. Remove the shield and motherboard PCA-A11 from the card cage.

To replace motherboard PCA-A11 and the card cage chassis, perform the above steps in reverse order. Tighten the screws removed in steps e, f, g, h, i, m, and o as follows:

Step	Screw	Index No.	Attached Part	Torque Setting (in.-lb)
e	T15	(45)	HP-IB PCA-A17	25
f	T9	(40)	RFI Shield	10
g	T20	(41)	RFI Shield	25
h	T15	(43)	PCA-A10 Shield	25
i	T25	(51)	Power Module Cover	20
m	T10	(70)	Servo Cable Retainer	10
o	T8	(54)	Motherboard PCA-A11 and Shield	4.5

When attaching PCA-A11 to the card cage chassis, ensure that J25 on PCA-A11 is aligned adjacent to the cable access opening on the card cage chassis. Also, when lowering the card cage chassis into the disc drive cabinet, ensure that the edge of the card cage chassis does not damage the flexible cabling adjacent to the actuator assembly.

6-16. ACTUATOR ASSEMBLY

The actuator assembly is factory installed in the disc drive cabinet and is not field replaceable. However, the majority of the components comprising the actuator assembly are field replaceable. Removal and replacement procedures for these components, in order of disassembly, are provided in the following paragraphs.

6-17. CARRIAGE LATCH SOLENOID

To remove the carriage latch solenoid (8, figure 7-5), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Remove the media module chamber (refer to paragraph 6-9) and the head contamination shield (refer to paragraph 6-13).

CAUTION

Do not allow the carriage assembly to move forward more than approximately one-half inch from its latched (retracted) position without having the head spacer tool, part no. 07930-60154, installed on the heads. Failure to observe this precaution will result in damage to the heads.

e. Manually release the carriage latch solenoid (8) and carefully move the carriage assembly forward until the heads project approximately one-half inch beyond the cam towers (25, 25A).

f. Install head spacer tool, part no. 07930-60154, on the heads.

g. Disconnect the two wires from the carriage latch solenoid (8).

h. Remove the two T15 screws (7) which secure the solenoid bracket (11) to the actuator assembly and remove the solenoid bracket.

i. Remove the two T9 screws (9) and flat washers (10) which secure the carriage latch solenoid (8) to the solenoid bracket (11) and remove the solenoid.

To replace the carriage latch solenoid, follow the above steps in reverse order. Tighten the screws removed in steps h and i as follows:

Step	Screw	Index No.	Attached Part	Torque Setting (in.-lb)
h	T15	(7)	Solenoid Bracket	13
i	T9	(9)	Solenoid	13

Following installation, manually check the locking action of the latch.

6-18. ACTUATOR STATUS PCA-A18

To remove actuator status PCA-A18 (40, figure 7-5) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Remove the media module chamber. (Refer to paragraph 6-9.)

e. Unplug the velocity transducer (1) cable from connector J1 on PCA-A18.

f. Disconnect the two wires from the carriage latch solenoid (8).

g. Remove the two T9 screws (38) and washers (39) which secure the right-hand rigid portion of PCA-A18 (40) to the actuator assembly.

h. Remove the four T10 screws (35) which secure the left-hand rigid portion of PCA-A18 to the actuator assembly.

i. Remove the connector clip (40A) from connector J2 on PCA-A18.

j. Unplug the flexible cable from connector J1 on PCA-A18 and remove PCA-A18.

To replace PCA-A18, perform the above steps in reverse order. Tighten the screws removed in step g to 10 inch-pounds.

6-19. VELOCITY TRANSDUCER AND VELOCITY TRANSDUCER SHAFT

To remove the velocity transducer (1, figure 7-5) and the velocity transducer shaft (5) from the disc drive, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Remove the media module chamber (refer to paragraph 6-9) and the head contamination shield (refer to paragraph 6-13).

e. Unplug the velocity transducer cable from connector J1 on actuator status PCA-A18 (40).

CAUTION

Do not allow the carriage assembly to move forward more than approximately one-half inch from its latched (retracted) position without having the head spacer tool, part no. 07930-60154, installed on the heads. Failure to observe this precaution will result in damage to the heads.

f. Manually release the carriage latch solenoid (8) and carefully move the carriage assembly forward until the heads project approximately one-half inch beyond the cam towers (25, 25A).

g. Install the head spacer tool, part no. 07930-60154, on the heads.

h. Loosen the 1.5 mm hexhead setscrew (6) which secures the velocity transducer shaft (5) to the carriage assembly.

i. Free the velocity transducer shaft (5) from the carriage assembly and push the shaft into the actuator assembly.

j. Remove the two T9 screws (2) which secure the velocity transducer (1) to the actuator assembly.

k. Remove the T9 screw (3) which secures the retainer (4) to the actuator assembly and remove the retainer.

l. Carefully slide the velocity transducer (1), with the velocity transducer shaft (5) inside it, out from the rear of the actuator assembly.

CAUTION

The velocity transducer shaft contains a calibrated magnet. To prevent damage to the velocity transducer shaft, avoid contact by the magnetic end of the shaft with ferrous or magnetic materials.

m. Carefully slide the velocity transducer shaft (5) out from the rear of the velocity transducer (1).

To replace the velocity transducer and velocity transducer shaft (5), proceed as follows.

CAUTION

Exercise extreme care when replacing the velocity transducer. A slight twist on the back section will break the wires inside the assembly.

a. Carefully slide the velocity transducer, with the velocity transducer shaft inside it, into the rear of the actuator assembly. Position the velocity transducer so that the transducer cable is aligned with the slot in the actuator assembly. Secure the velocity transducer in place with the two T9 screws (2) previously removed. Tighten the screws (2) to 10 inch-pounds.

b. Replace the retainer (4) with the T9 screw (3) previously removed. Tighten the screw to 10 inch-pounds.

c. Using a slender rod of nonmagnetic material, push on the magnet end of the velocity transducer shaft (5) until the rod end extends through the hole in the actuator assembly.

d. Insert the rod end of the velocity transducer shaft into the opening on the carriage assembly (16). Tighten the T6 setscrew (6) on the carriage assembly to 5 inch-pounds.

e. Carefully return the carriage assembly to its locked position and remove the head spacer tool.

f. Connect the velocity transducer cable to connector J1 on actuator status PCA-A18 (40).

g. Perform the seek deceleration adjustment described in Section IV, Alignment and Adjustment.

h. Replace the head contamination shield (refer to paragraph 6-13), the media module chamber (refer to paragraph 6-9), and the shroud (refer to paragraph 6-3).

6-20. DATA AND SERVO HEADS

The data heads and the servo head are removed and replaced in the same manner. When any head is replaced, the appropriate head alignment procedure must be performed as part of the replacement. To remove a data head (12, 14, figure 7-5) or the servo head (13), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Remove the media module chamber (refer to paragraph 6-9), card cage cover (refer to paragraph 6-12), and head contamination shield (refer to paragraph 6-13).

e. If the servo head is to be replaced, remove the T10 screw (70, figure 7-1) which secures the servo cable retainer (71) and ground strip (71A) over the servo head cable.

f. Disconnect the appropriate head cable from the connector on read/write PCA-A10. The servo head cable must also be disconnected from connector J1 on track follower PCA-A9.

CAUTION

To avoid damage to the head, be sure to install head installation tool, part no. 13354-20009, on the head as shown in figure 6-4.

g. Install the head installation tool, part no. 13354-20009, on the head to be removed. (See figure 6-4.)

Note: The UP side of the installation tool is used for heads 1, 3, 5, 6, 8, 10, and 12. The DN (down) side of the installation tool is used for heads 0, 2, 4, 7, 9, 11, and the servo head. (See figure 6-5 for head numbering details.)

h. Hold the head in place by applying a slight pressure to the head installation tool, and then loosen the appropriate head retaining screw (19, figure 7-5).

i. Remove the head with the head installation tool attached. Exercise care to avoid damaging critical elements of the head assembly.

j. If it is necessary to replace a head retaining screw (19) and washer (20), proceed as follows:

(1) Loosen all of the head retaining screws (19) on the carriage assembly.

(2) Loosen the two T6 screws (17) which secure the retainer plate (18) to the carriage assembly.

(3) Move the retainer plate (18) back toward the actuator until sufficient clearance is obtained to remove the defective head retaining screw and washer.

(4) Insert the new head retaining screw and washer in place.

(5) Move the retainer plate (18) to its former location and tighten the two screws (17) to 10 inch-pounds.

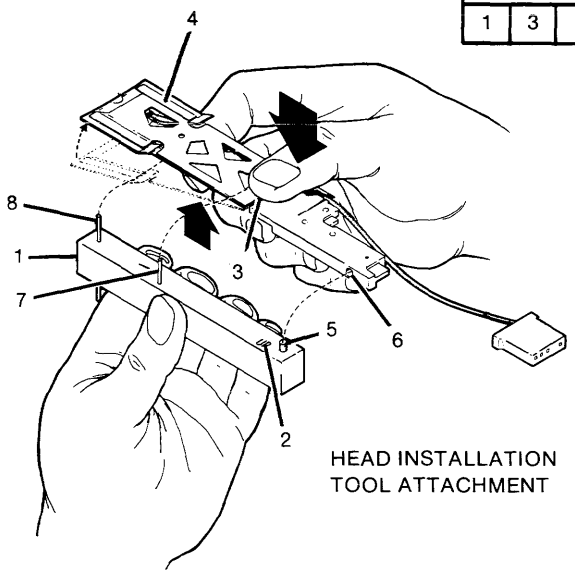
(6) Tighten the head retaining screws (19) to 8 inch-pounds.

To replace a data or servo head, proceed as follows:

CAUTION

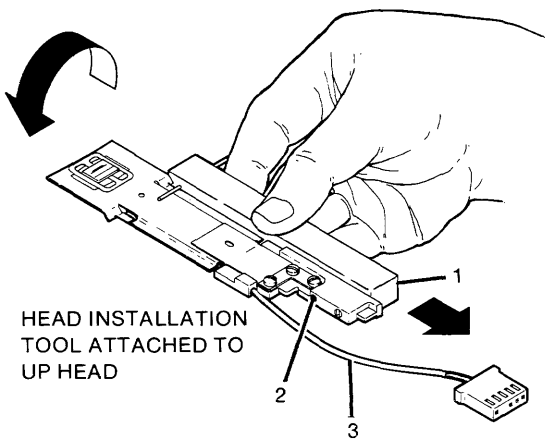
To avoid damage to the head, do not touch or clean the surface of the head that attaches to the actuator.

UP HEADS						
1	3	5	6	8	10	12



HEAD INSTALLATION TOOL ATTACHMENT

1. POSITION TOOL (1) WITH "UP" MARKING (2) AS SHOWN AND THUMB AT SPRING JOINT (3) OF HEAD ASSEMBLY (4).
2. LIFT HEAD ARM UP UNTIL HEAD ASSEMBLY (4) IS STRAIGHT.
3. INSERT POST (5) INTO HOLE (6) WITH CENTER PIN (7) OVER BACK AND FRONT PIN (8) UNDER HEAD ASSEMBLY (4).

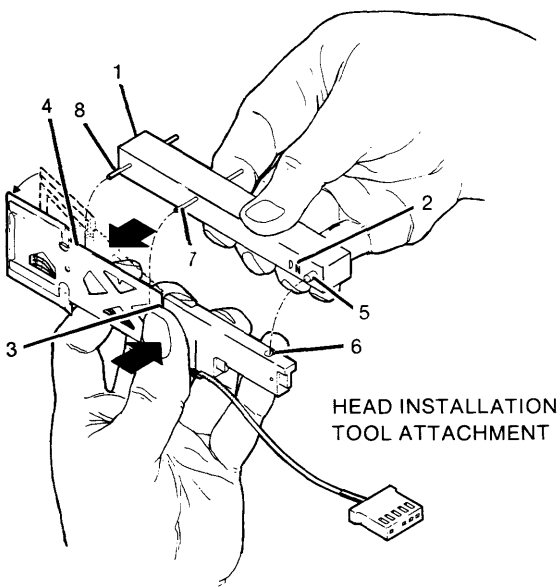


HEAD INSTALLATION TOOL ATTACHED TO UP HEAD

1. HOLDING TOOL (1) AS SHOWN, INSTALL HEAD WITH MOUNTING HOLE (2) AND CABLE (3) FACING CARD CAGE SIDE OF DRIVE.

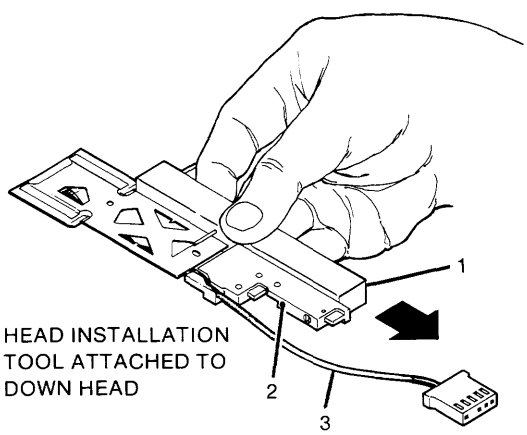
UP HEADS

DOWN HEADS						
0	2	4	7	9	11	SERVO



HEAD INSTALLATION TOOL ATTACHMENT

1. POSITION TOOL (1) WITH "DN" MARKING (2) AS SHOWN AND THUMB AT SPRING JOINT (3) OF HEAD ASSEMBLY (4).
2. LIFT HEAD ARM UP UNTIL HEAD ASSEMBLY (4) IS STRAIGHT.
3. INSERT POST (5) INTO HOLE (6) WITH CENTER PIN (7) OVER BACK AND FRONT PIN (8) UNDER HEAD ASSEMBLY (4).



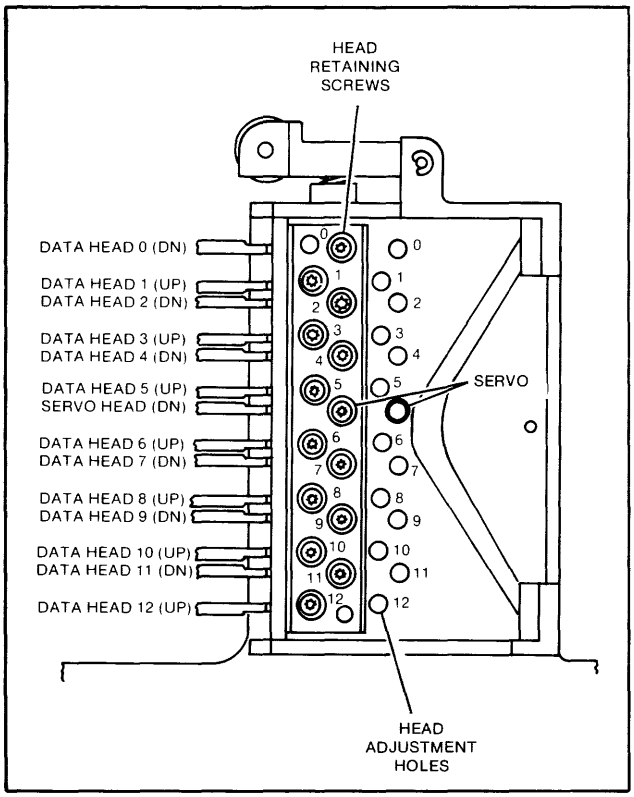
HEAD INSTALLATION TOOL ATTACHED TO DOWN HEAD

1. HOLDING TOOL (1) AS SHOWN, INSTALL HEAD WITH MOUNTING HOLE (2) AND CABLE (3) FACING CARD CAGE SIDE OF DISC DRIVE.

DOWN HEADS

7933-327

Figure 6-4. Using the Head Installation Tool



7933-352A

Figure 6-5. Data and Servo Head Retaining Screw Locations

CAUTION

To avoid damage to the head be sure to use the installation tool on the head as shown in figure 6-4.

a. Install the head installation tool on the replacement head, as shown in figure 6-4. The UP side of the installation tool is used for heads 1, 3, 5, 6, 8, 10, and 12. The DN (down) side of the installation tool is used for heads 0, 2, 4, 7, 9, 11, and the servo head. (See figure 6-5 for head numbering details.)

b. Clean the head as outlined in Section III, Maintenance.

CAUTION

Do not tighten the head retaining screw with the head installation tool attached to the head as the heads will not seat properly in the earrige. Damage to the head and the disc surface is likely to occur if the head retaining screw is tightened with the tool in place.

c. Set the head in place on the carriage assembly and with the head installation tool still attached, move the head until the head initial position tool, part no. 13354-20008, can be inserted into the adjustment hole of the head being installed. (The servo head adjustment hole is marked with an indelible marker on some disc drives; see figure 6-5.) The tip of the initial position tool must fit in the alignment slot on the head.

d. Slide the head assembly back until it is placing pressure on the head initial position tool.

e. Thread the head retaining screw until it is finger tight and the head remains in place.

f. Remove the head installation tool, taking care not to move the head.

g. Remove the head initial position tool and tighten the head retaining screw to 3 inch-pounds.

h. Connect the head cable to its respective connector on read/write PCA-A10 (39, figure 7-1). The connectors are mounted on PCA-A10 in the same order that the heads are mounted on the carriage assembly. Connect the remaining lead from the servo head to connector J1 on track follower PCA-A9 (38). Install the cables in such a manner that they form a smooth semi-circle from the carriage assembly to read/write PCA-A10.

i. If the servo head was removed, secure the servo head cable using the cable retainer (71), ground strip (71A), and T10 screw (70). Tighten the T10 screw to 10 inch-pounds.

j. Replace the card cage cover (refer to paragraph 6-12), media module chamber (refer to paragraph 6-9), and the control panel assembly (refer to paragraph 6-7).

k. Perform the appropriate head alignment procedure, as given in Section IV, Alignment and Adjustment.

l. Replace the head contamination shield (refer to paragraph 6-13) and the shroud (refer to paragraph 6-3).

6-21. CARRIAGE ASSEMBLY

To remove the carriage assembly (16, figure 7-5), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Remove the media module chamber (refer to paragraph 6-9).

e. Remove the head contamination shield. (Refer to paragraph 6-13.)

f. If the carriage assembly is to be reinstalled, perform steps g and h. If a new carriage assembly is to be installed, remove all of the data heads and the servo head (refer to paragraph 6-20), then skip to step i.

CAUTION

Do not allow the carriage assembly to move forward more than approximately one-half inch from its latched position without having head spacer tool, part no. 07930-60154, installed on the heads. Failure to observe this precaution may result in damage to the heads.

g. Manually release the carriage latch solenoid (8) and carefully move the carriage assembly (16) forward until the heads project approximately one-half inch beyond the cam towers (25, 25A).

h. Install head spacer tool, part no. 07930-60154, on the heads.

i. Loosen the 1.5 mm hexhead setscrew (6) which secures the velocity transducer shaft (5) to the carriage assembly and disengage the shaft. Push the shaft into the actuator assembly.

j. Remove the four T15 screws (26) which secure the two cam towers (25, 25A) to the actuator assembly and remove the cam towers.

k. Remove the four T10 screws (15) which secure the carriage assembly to the armature assembly (37).

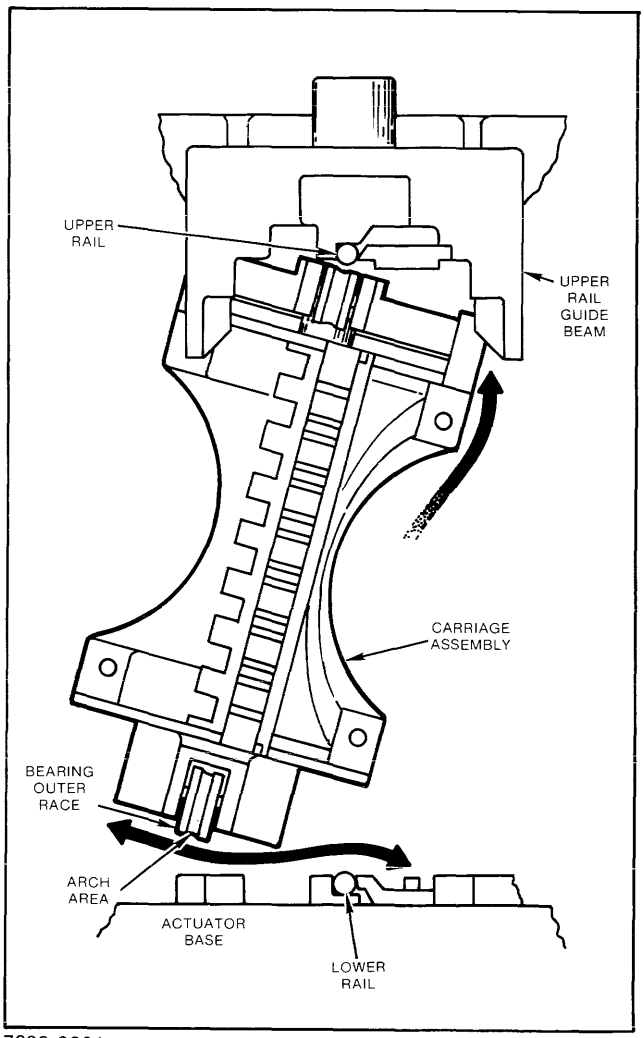
l. Lift up on the carriage assembly and when it is free of the lower rail (43), remove the carriage assembly from the actuator assembly. (See figure 6-6 for removal details.) Place the carriage assembly on a clean, dry work surface.

To replace the carriage assembly, proceed as follows:

a. Clean the lower rail (43, figure 7-5) and the upper rail (46) with a cleaning wipe moistened with filtered isopropyl alcohol.

b. Before installing a new or old carriage, the bearing outer race must be thoroughly cleaned of all particles. This must be done to maximize the future life of the assembly.

c. Saturate a cotton swab with filtered alcohol. Fold a cleaning wipe over the swab and squeeze out excess alcohol. Set the carriage assembly on a clean surface with the bearing readily accessible. Carefully rotate the bearing with one finger while swabbing the arch area and sides of the outer race with the cotton swab (see figure 6-6). Repeat until there is no sign of contaminant particles.



7933-326A

Figure 6-6. Carriage Removal and Replacement Details

CAUTION

Do not allow excess alcohol to wick into the side covers of the bearings. This will dilute the bearing lubricant and result in premature bearing failure.

d. Repeat step c for each of the three carriage bearings.

e. Clean all adjacent surfaces of any contaminant particles.

f. Place the carriage assembly in position adjacent to the rails and engage the carriage on the upper rail (46).

g. Lift up on the carriage assembly and when it is level with the lower rail (43), rotate the carriage assembly into position on the lower rail. (See figure 6-6 for installation details.)

h. Using alcohol, thoroughly clean the four T10 screws (15, figure 7-5) which secure the carriage assembly to the armature assembly (37). Install and tighten each screw equally, beginning with two diagonally opposite screws. Tighten the screws to 10 inch-pounds.

i. Manually unlock the carriage and move it forward.

j. Using a slender rod of nonmagnetic material, push the magnet end of the velocity transducer shaft (5) until the rod end extends through the hole in the actuator assembly.

k. Insert the rod end of the velocity transducer shaft (5) into the opening on the carriage assembly (16). Tighten the 1.5 mm hexhead setscrew (6) on the carriage assembly to 5 inch-pounds.

l. Replace the two cam towers (25, 25A) with the four T15 screws (26) previously removed. Tighten the screws to 15 inch-pounds.

m. Move the carriage assembly forward and check that each side of the carriage is aligned with a crash stop pad (24) on the cam tower and a crash stop pad (47) on the actuator. When alignment is correct the carriage should strike all four crash stop pads with equal force. If necessary, loosen the cam tower securing screws (26) and move the towers forward or back until the desired alignment is achieved. Tighten the screws to 15 inch-pounds.

n. Clean and lubricate the carriage bearing/rail interface as described in section III of this manual.

CAUTION

Failure to lubricate a replaced carriage assembly as prescribed in paragraph 3-11 can result in servo or data errors (plus DERR 70 or 76).

o. Clean the data heads and servo head as described in section III of this manual.

p. Move the carriage assembly to within one-half inch of its latched (retracted) position.

q. Replace the data heads and servo head, if removed (refer to paragraph 6-20), or remove the head spacer tool.

r. Return the carriage assembly to its latched position.

s. Replace the media module chamber. (Refer to paragraph 6-9.)

t. Perform the servo head and data head alignment procedures as detailed in Section IV, Alignment and Adjustment.

u. Replace the head contamination shield (refer to paragraph 6-13) and the shroud (refer to paragraph 6-3).

6-22. ARMATURE ASSEMBLY

To remove the armature assembly (37, figure 7-5), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Remove the media module chamber (refer to paragraph 6-9), the card cage cover (refer to paragraph 6-12), and read/write PCA-A10 (refer to paragraph 6-14).

e. Remove the left-hand section of the head contamination shield (refer to paragraph 6-13).

f. Remove the carriage assembly. (Refer to paragraph 6-21).

g. Remove the four T15 screws (26) which secure the two cam towers (25, 25A) to the actuator assembly and remove the cam towers.

h. Unplug the velocity transducer (1) cable from connector J1 on actuator status PCA-A18 (40).

i. Disconnect the two wires from the carriage latch solenoid (8).

j. Remove the two T9 screws (38) and washers (39) which secure the right-hand rigid portion of actuator status PCA-A18 (40) to the actuator assembly.

k. Remove the four cap screws (35) which secure the coil band cover and the left-hand rigid portion of PCA-A18 (40) to the actuator assembly.

l. Detach the armature assembly (37) from connector J1 on PCA-A18 and carefully withdraw the armature assembly from the actuator.

To replace the armature assembly (37), proceed as follows:

a. Carefully insert the armature assembly into the actuator assembly.

b. Attach the coil band cover (36) and PCA-A18 (40) to the actuator assembly with the two T9 screws (38), two washers (39), and four cap screws (35) previously removed. Tighten the six screws to 10 inch-pounds. Connect the armature assembly to connector J1 on PCA-A18.

c. Replace the crash stop pads (24) on the inner side of the cam towers (25, 25A) with new crash stop pads.

d. Replace the two cam towers (25, 25A) on the actuator assembly with the four T15 screws (26) previously removed. Tighten the four screws to 15 inch-pounds.

e. Replace the two crash stop pads (47) on the actuator with new crash stop pads.

CAUTION

Ensure that the carriage bearing/rail interface cleaning and lubrication is performed when the carriage assembly is installed (refer to section III of this manual). Failure to perform these procedures may result in damage to the disc drive.

f. Replace the carriage assembly as outlined in paragraph 6-21.

g. Extend the carriage forward and check that each side of the carriage is aligned with the crash stop pads on the cam tower and the actuator. When alignment is correct the carriage should strike each crash stop with equal force. If necessary, loosen the screws (26) and move the towers forward or back until the desired alignment is achieved. Tighten the screws to 15 inch-pounds.

h. Attach the two wires to the carriage latch solenoid (8) and move the carriage assembly back until it locks in place.

i. Replace read/write PCA-A10 (refer to paragraph 6-14) and the card cage cover (refer to paragraph 6-12).

j. Replace the media module chamber (refer to paragraph 6-9) and the control panel assembly (refer to paragraph 6-7).

k. Perform the servo head and data head alignment procedures detailed in section IV of this manual.

l. Replace the head contamination shield (refer to paragraph 6-13) and the shroud (refer to paragraph 6-3).

6-23. LOWER AND UPPER RAILS

To remove the lower rail (43, figure 7-5) and the upper rail (46), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Remove the media module chamber (refer to paragraph 6-9).

e. Remove the left-hand section of the head contamination shield (refer to paragraph 6-13).

f. Remove the carriage assembly. (Refer to paragraph 6-21.)

g. Remove the seven T10 screws (41) which secure the lower rail clamp (42) to the actuator assembly; then remove the clamp (42) and the lower rail (43). Use the 10 inch-pound offset torque wrench, part no. 8710-1594, to remove the screws.

h. Loosen the three T10 screws (44) which secure the upper rail clamp (45) to the actuator assembly and remove the upper rail (46).

To replace the upper rail and the lower rail, proceed as follows:

a. Clean the upper and lower rail mount surfaces on the castings with a cleaning wipe moistened with filtered isopropyl alcohol. Remove all particles from the adjacent surfaces.

b. Clean both cam towers in a similar manner to remove all particles from its surfaces.

c. Install new crash stop pads on the cam towers, if necessary.

d. Clean the upper rail (46) and clamp (45) with a cleaning swab and alcohol. Install the rail and clamp on the upper rail guide beam.

e. Locate the end of the upper rail (46) flush with the front of the actuator assembly and tighten the three T10 screws (44) to 5 inch-pounds, starting with the center screw. Use the 10 inch-pound offset torque wrench, part no. 8710-1594. Repeat this procedure a second time, tightening the screws to 10 inch-pounds.

f. Clean the lower rail and clamp with a cleaning swab and alcohol. Install the rail (43) and clamp (42) on the casting surface making sure the rail is captured between the two tabs on the lower rail clamp.

g. Starting with the center screw, tighten the seven T10 screws (41) to 5 inch-pounds, alternating between left and right of the center screw. Use the 10 inch-pound offset torque wrench, part no. 8710-1594. Repeat this sequence, tightening the screws to 10 inch-pounds.

h. Before installing the carriage assembly, clean each rail once again with a cleaning swab and alcohol to remove any particles.

CAUTION

Ensure that the carriage bearing/rail interface cleaning and lubrication is performed when the carriage assembly is installed (refer to section III of this manual). Failure to perform these procedures may result in damage to the disc drive.

i. Install the carriage assembly (refer to paragraph 6-21).

j. Return the carriage assembly to its locked position.

k. Replace the media module chamber. (Refer to paragraph 6-9.)

l. Perform the servo head and data head alignment procedures detailed in section IV of this manual.

m. Replace the head contamination shield (refer to paragraph 6-13) and the shroud (refer to paragraph 6-3).

6-23A. REAR CRASH PAD ASSEMBLY

To remove the rear crash pad prior to installing the new crash pad, part no. 07930-60256, proceed as follows:

a. Remove card cage cover (refer to paragraph 6-12).

b. Remove head contamination shield (refer to paragraph 6-13).

c. Remove the read/write PCA-A10 by first disconnecting all head cables from J0 through J12, and loosening the two captive screws that secure the adjacent RFI shield (44, figure 7-1).

d. Remove the media module, then remove the read/write PCA-A10 support by unscrewing the two screws attached to the actuator/spindle base.

e. Depress the solenoid plunger and install the head spacer tool (table 3-1). Move the carriage assembly forward and unscrew the four T10 screws that attach the carriage assembly to the armature assembly.

f. With a 1.5 mm hexwrench, loosen the setscrew securing the shaft to the velocity transducer and slide the shaft backward into the velocity transducer.

g. Remove the rear crash pad assembly and use a cotton swab with alcohol to clean the mounting surface area.

To install a new rear crash pad, proceed as follows:

a. Place the new rear crash pad, part no. 07930-60256, into position by centering the hole around the velocity transducer and aligning the mounting holes (51, figure 7-5). Insert both T10 mounting screws and hand tighten.

b. Re-attach the velocity transducer shaft.

c. Verify velocity transducer clearance by looking through the hole in the shaft from the rear of the linear motor. While moving the carriage assembly slowly back and forth, an even ring of light should appear all around the velocity transducer shaft magnet. If not, the rear crash pad must be adjusted before tightening the screws to 7 inch-pounds. Recheck clearance once more after tightening.

d. Re-attach the armature to the carriage assembly (previous step e). Tighten the four T10 screws to 10 inch-pounds.

e. Push carriage assembly back into linear motor and remove head spacer tool inserted in previous step e.

f. Re-attach read/write PCA-A10 support to actuator/spindle base. Tighten both screws to 10 inch-pounds.

g. Clean the media module chamber as described in the preventive maintenance procedure (paragraph 3-13). Re-install the media module.

Restore the drive to running condition as follows:

a. Read/write PCA-A10 into card cage, RFI shield tightened to 10 inch-pounds, heads reconnected to PCA-A10.

b. Head contamination shields in place, tighten all 5 screws to 12 inch-pounds.

c. Card cage cover secured with 4 screws, tighten to 12 inch-pounds.

d. All card cage cables reconnected, front panel cable screws (2) tightened to 12 inch-pounds.

6-24. MOTOR-SPINDLE ASSEMBLY

WARNING

When shipping magnetic assemblies (motor-spindles) which have been removed from disc drives, each magnetic assembly must be packaged individually. Transporting more than one removed magnetic assembly in a single container could exceed aircraft limitations, 2.0 milligauss at 2.13 metres (7 feet), which could create a potential hazard during shipping. If the magnetic material is being shipped into or within the United States, all applicable regulations of the U.S. Department of Transportation (DOT) must be followed before release to the initial carrier in the U.S. Refer to DOT Regulations, Title 49, parts 171-177 (Hazardous Materials).

To remove the motor-spindle assembly (67, figure 7-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Remove the prefilter (refer to paragraph 6-5) and the media module chamber (refer to paragraph 6-9).

e. Remove the four T10 screws (64) which secure the seal assembly (65) to the motor-spindle assembly (67) and remove the seal assembly. (Use the T10 bit, part no. 8710-1465.)

f. Remove the T15 screw (3, figure 7-3) which secures the ground cable (60, figure 7-1) to the motor-spindle assembly.

g. Unplug the motor-spindle assembly cable from the connector at the rear of the prefilter chamber.

h. Remove the three T30 screws (66) which secure the motor-spindle assembly to the actuator assembly.

CAUTION

When removing the motor-spindle assembly, do not attempt to lift the assembly by the spindle hub. Damage to the motor-spindle assembly may occur.

CAUTION

The motor-spindle assembly weighs approximately 15.9 kilograms (35 pounds). Exercise care when lifting it from the disc drive.

i. With one hand, push up on the bottom of the assembly until the mounting flange is free of the disc drive and with the other hand grasp the mounting flange. Then, with both hands, lift the assembly out of the disc drive.

To replace the motor-spindle assembly, proceed as follows:

CAUTION

When installing the motor-spindle assembly, do not attempt to lift the assembly by the spindle hub. Damage to the assembly may occur.

a. Grasping the motor-spindle assembly mounting flange with both hands, carefully lower the assembly into the disc drive. When almost in place, support the bottom of the assembly with one hand until the assembly is resting on the actuator casting.

b. Rotate the motor-spindle assembly until the power cable is pointing toward the right-hand side of the disc drive (as viewed from the front).

c. Replace the three T30 screws (66) previously removed. Tighten the screws to 75 inch-pounds.

d. Replace the seal assembly (65) on the motor-spindle assembly with the four T10 (64) screws previously removed. Tighten the screws to 10 inch-pounds.

e. Connect the motor-spindle assembly cable to connector J5 on spindle driver PCA-A12 (6, figure 7-4).

f. Connect the ground cable to the motor-spindle assembly with the T15 screw (3, figure 7-3) previously removed. Tighten the screw to 12 inch-pounds.

g. Replace the media module chamber (refer to paragraph 6-9), the prefilter (refer to paragraph 6-5), and the shroud (refer to paragraph 6-3).

6-25. SPINDLE GROUND KIT

To remove the motor-spindle grounding components and replace with the spindle ground kit, proceed as follows:

Note: Before starting this procedure, a disc back-up should be performed to protect data stored on the media.

a. Remove media module. (Refer to paragraph 6-8.)

b. Perform the preparation for service procedure outlined in paragraph 6-2.

c. Ensure that the disc drive power cord is disconnected from the ac power source.

d. Remove the following items:
- Shroud (refer to paragraph 6-3).
- Front panel (refer to paragraph 6-4).
- Prefilter (refer to paragraph 6-5).

e. Remove motor-spindle assembly. (Refer to previous paragraph.)

f. Remove the three T15 screws (1, figure 7-3) which secure the bottom cover (2) to the motor-spindle assembly.

g. Cover the spindle hub with a cleaning wipe and grasp firmly with one hand. With the other hand, remove the ground button using an adjustable wrench. Discard the ground button.

To install a new spindle ground button, proceed as follows:

a. Place one drop of sealant, part no. 0470-0573, on opposite mating surfaces of the new ground button (see figure 6-6A). Do not put any sealant on the ground button threads.

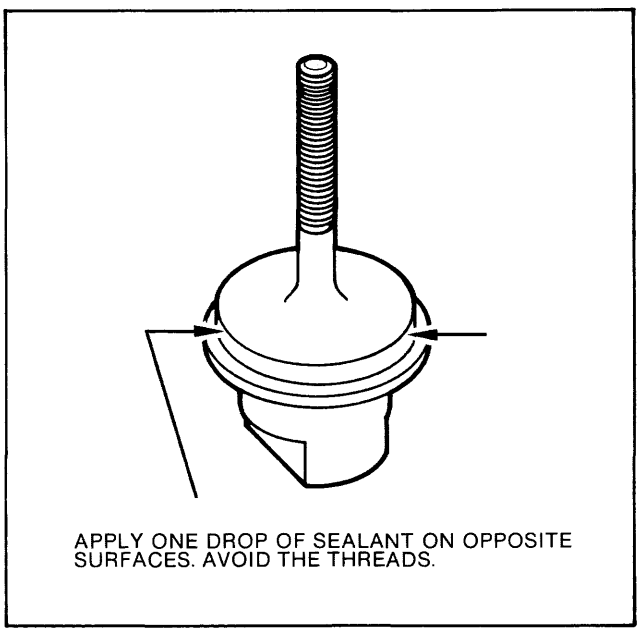


Figure 6-6A. Application of Sealant

CAUTION

Touching the top machined surfaces of the spindle-motor assembly can cause contamination.

b. Without touching the top, outermost machined surface of the spindle-motor assembly, hold the spindle nose tightly with one hand. With the other hand, hand tighten the ground button into the spindle-motor shaft.

c. While continuing to hold the spindle nose by hand, tighten the ground button with an adjustable wrench until the spindle nose cannot be prevented from turning in your hand.

d. Use a cleaning wipe to clean excess sealant from the ground button.

CAUTION

Ensure that the ground strap (60, figure 7-1) is installed beneath one of the T15 screws which secure the bottom cover. Failure to do this may result in loss of data or damage to the disc drive.

e. Install the ground strap and the new bottom cover using the three T15 screws previously removed. Tighten the screws to 12 inch-pounds.

f. Clean the media module chamber and motor-spindle assembly as described in section III of this manual.

g. Reverse steps a through d of the previous (removal) procedure to prepare the drive for operation.

6-26. POWER MODULE

The power module (73, figure 7-1) is located at the lower rear of the disc drive cabinet and is mounted on track slides to facilitate servicing. Field replaceable components in the power module include spindle driver PCA-A12, dc power PCA-A13, an input power assembly, a blower power distribution assembly, transformer T1, and five filter capacitors.

CAUTION

- Do not attempt to operate the disc drive with the power module cover (52) removed. This will reduce the efficiency of the disc drive RF shielding.

- Do not attempt to power up the disc drive with the power module withdrawn from the disc drive enclosure. This will interrupt the flow of cooling air in the enclosure and cause overheating and possible damage to the equipment.

6-27. ACCESS FOR SERVICE

To access the power module (73, figure 7-1) for service, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the shroud. (Refer to paragraph 6-3.)

d. Remove the front panel (6) and rear panel (5) from the disc drive (refer to paragraph 6-4), and the prefilter (refer to paragraph 6-5).

e. Disconnect the blower (61) cable and the motor-spindle (67) cable from the connectors at the rear of the prefilter chamber.

f. Remove the twelve T25 screws (51) which attach the power module cover (52) to the disc drive and remove the cover.

g. Unplug cable W3 (47) from connector J1 on dc power PCA-A13 (15, figure 7-4) and cables W4 (48, figure 7-1) and W2 (53) from connectors J1 and J2 on spindle driver PCA-A12 (6, figure 7-4).

h. Pull the power module assembly (73, figure 7-1) forward until it is fully extended on its slide mounts.

To return the power module to service, perform the above steps in reverse order. Tighten the twelve T25 screws removed in step f to 20 inch-pounds.

6-28. SPINDLE DRIVER PCA-A12

To remove spindle driver PCA-A12 (6, figure 7-4), proceed as follows:

a. Perform the power module access for service procedure outlined in paragraph 6-27.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the cover (1) from PCA-A12 (6).

d. Remove the four T25 screws (4) which secure PCA-A12 to capacitors C1, C2 (11).

e. Remove the two T10 screws (3) which secure PCA-A12 to the two PCA supports (13) attached to PCA-A13 (15).

f. Unplug the power transformer cable from connector J3 on PCA-A12.

g. Loosen the four T15 screws (5) on the PCA-A12 heat sink support (22) and remove PCA-A12 from the power module. Remove the air seal (2) from PCA-A12.

Note: During installation, ensure that the air seal (2) is positioned on PCA-A12 (6) with the foam side facing the front of the disc drive when installed.

To replace spindle driver PCA-A12, perform the above steps in reverse order. Tighten the screws removed in steps d, e, and g, as follows:

Step	Screw	Index No.	Attached Part	Torque Setting (in.-lb)
d	T25	(4)	PCA-A12	15
e	T10	(3)	PCA-A12	5
g	T15	(5)	PCA-A12	15

a. Perform the power supply check described in section IV of this manual.

6-29. DC POWER PCA-A13

To remove dc power PCA-A13 (15, figure 7-4), proceed as follows:

a. Perform the power module access for service procedure detailed in paragraph 6-27.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove spindle driver PCA-A12. (Refer to paragraph 6-28.)

d. Remove the six T25 screws (14) which secure PCA-A13 (15) to capacitors C170 (19) and C230, C270 (20). (Re-install at 20 lbs. torque setting.)

e. Unplug the power transformer (29) cable from connector P1 on PCA-A13 and remove PCA-A13 from the power module.

To replace PCA-A13, perform the above steps in reverse order.

6-30. FILTER CAPACITORS

CAUTION

When replacing the filter capacitors, ensure that the "+" (positive) and "-" (negative) markings on the capacitor terminals match the corresponding + and - markings on PCA's A12 and A13. The vent plugs on the capacitors should also line up with the "VENT" holes in the PCA's.

Filter capacitors C1, C2 (11, figure 7-4) are held in place by a clamp (10) on the power module and the capacitors can be removed following the removal of spindle driver PCA-A12, as outlined in paragraph 6-28. Filter capacitors C170 (19), and C230, C270 (20) are held in place by a clamp (18) and the capacitors can be removed following the removal of dc power PCA-A13, as outlined in paragraph 6-29. Before returning the disc drive to service, perform the power supply check described in Section IV, Alignment and Adjustment.

6-31. INPUT POWER ASSEMBLY

To remove the input power assembly (42 through 57, figure 7-4), proceed as follows:

a. Perform the power module access for service procedure outlined in paragraph 6-27.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Remove the three T10 screws (40, figure 7-4) which secure the input power assembly to the power module.

d. Unplug the brown wire from connector J4 and the blue wire from connector J3 on line filter PCA-A21 (47). Disconnect the green-yellow wire from the ground terminal. Remove the input power assembly from the power module.

Note: On early models which use the receptacle connector (50) and gasket (51), these parts are necessary to maintain cooling airflow within the disc drive. Replace these parts if they become cracked or torn, or replace the entire input power assembly.

To replace the input power assembly, perform the above steps in reverse order. Tighten the three screws (40) removed in step c to 20 inch-pounds.

6-32. BLOWER POWER DISTRIBUTION ASSEMBLY

To remove the blower power distribution assembly (31 through 39, figure 7-4), proceed as follows:

a. Perform the power module access for service procedure detailed in paragraph 6-27.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

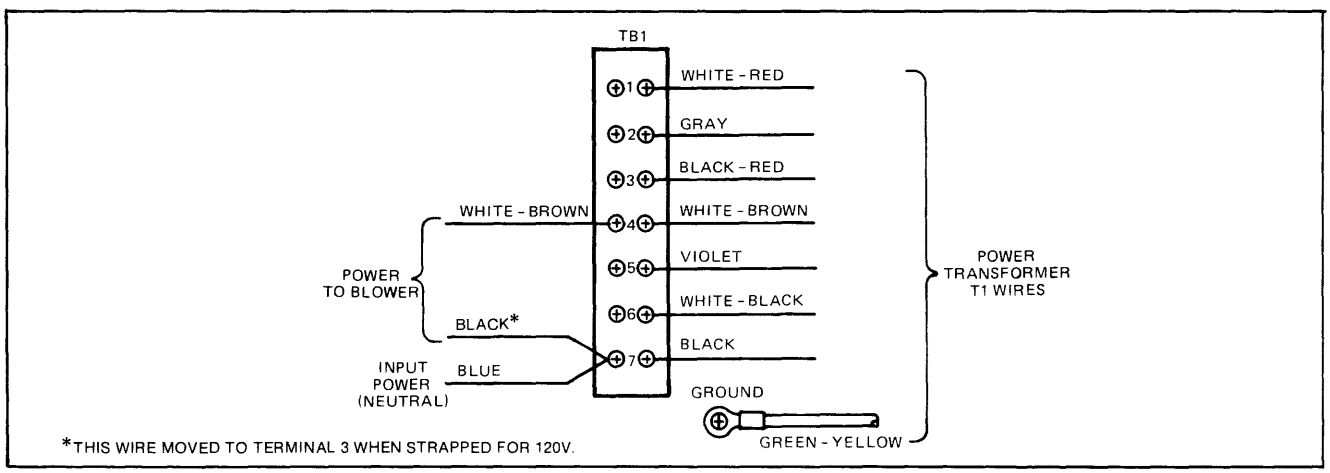
c. Remove the two T10 screws (24, figure 7-4) which secure the strapping chamber cover (23) to the power module and remove the cover.

d. Disconnect the following blower power assembly (31 through 39) wires from terminal block TB1 (27) in the strapping chamber. (See figure 6-7 for details.)

Terminal	Wire
4	white-brown
7	black

e. Remove the four T10 screws (30, figure 7-4) which secure the blower power distribution assembly to the power module casting (61).

f. Thread the two wires removed in step d through the opening in the power module casting and remove the blower power distribution assembly.



7933-34

Figure 6-7. Power Transformer T1 Wiring Details

To replace the blower power distribution assembly, perform the above steps in the reverse order. Tighten the screws removed in steps c and e as follows:

Step	Screw	Index No.	Attached Part	Torque Setting (in.-lb)
c	T10	(24)	Cover	20
e	T10	(30)	Blower Power Distribution Assembly	20

6-33. POWER TRANSFORMER

To remove the power transformer (29, figure 7-4), proceed as follows:

a. Perform the power module access for service procedure outlined in paragraph 6-27.

b. Ensure that the disc drive power cable is disconnected from the ac power source.

c. Remove spindle driver PCA-A12 (refer to paragraph 6-28) and dc power PCA-A13 (refer to paragraph 6-29).

d. Remove the two T10 screws (24) which secure the strapping chamber cover (23) to the power module and remove the cover.

e. Disconnect the following power transformer wires from terminal block TB1 (27). (See figure 6-7.)

Terminal	Wire
1	white-red
2	gray
3	black-red
4	white-brown
5	violet
6	white-black
7	black

f. Remove the T15 screw (58, figure 7-4) which secures the green-yellow ground wire to the power module casting (61).

g. Remove the four T30 cap screws (21) which secure power transformer T1 (29) and the two heat sink supports (22) to the power module.

CAUTION

The power transformer weighs approximately 16 kilograms (36 pounds). Exercise care when lifting the transformer from the power module.

h. Carefully lift the power transformer up and away from the power module.

To replace power transformer T1, perform the above steps in the reverse order. Before placing the transformer in the power module, turn the transformer so that the blue wires on the transformer are facing toward terminal block TB1 (27) in the strapping chamber. Tighten the screws removed in steps d, f, and g as follows:

Step	Screw	Index No.	Attached Part	Torque Setting (in.-lb)
d	T10	(24)	Cover	10
f	T15	(58)	Ground Wire	15
g	T30	(21)	Power Transformer and Heat Sink Supports	60

Following installation, ensure that the transformer wires are reconnected as detailed in steps c and d and illustrated in figure 6-7. Before returning the disc drive to service, perform the power supply check described in Section IV, Alignment and Adjustment.

6-34. BLOWER ASSEMBLY

To remove the blower assembly (61, figure 7-1), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 6-2.

b. Ensure that the disc drive power cord is disconnected from the ac power source.

c. Loosen the two 1/4-turn captive screws on the baffle plate (58) and remove the baffle plate from the disc drive.

d. Disconnect the blower assembly power cable from the connector at the rear of the prefilter chamber.

CAUTION

Do not attempt to pull forward on the blower assembly before it is unlatched from the cabinet. Failure to observe this precaution may result in damage to the cabinet.

e. Disconnect the two 1/4-turn screws which secure the blower assembly to the disc drive cabinet and tilt the blower assembly upward until it unlatches from the cabinet. Remove the blower assembly.

To replace the blower assembly, perform the above steps in reverse order.

REPLACEABLE PARTS

SECTION VII

7-1. INTRODUCTION

This section provides listings of all field-replaceable parts and an illustrated parts breakdown for the disc drive, as well as replaceable parts ordering information.

Replaceable parts for the disc drive are listed in disassembly order in tables 7-1 through 7-6 and illustrated in figures 7-1 through 7-6. In each table, attaching parts are listed immediately after the item they attach. Items in the DESCRIPTION column are indented to indicate relationship to the next higher assembly. In addition, the symbol "— — — x — — —" follows the last attaching part for that item. Indentation of the items in the tables is as follows:

Major Assembly

*Replaceable Assembly

*Attaching Parts for Replaceable Assembly

**Subassembly or Component Part

**Attaching Parts for Subassembly or Component Part

The replaceable parts listings provide the following information for each part:

a. FIG. & INDEX NO. The figure and index number which indicates where the replaceable part is illustrated.

b. HP PART NO. The Hewlett-Packard part number for each replaceable part.

c. DESCRIPTION. A description of each replaceable part. Refer to table 7-7 for an explanation of abbreviations used in the DESCRIPTION column.

d. MFR CODE. The 5-digit code that denotes a typical manufacturer of a part. Refer to table 7-8 for a listing of manufacturers that correspond to the codes.

e. MFR PART NO. The manufacturer's part number of each replaceable part.

f. UNITS PER ASSY. The total quantity of each part used in the major assembly.

The MFR CODE and MFR PART NO. for common hardware items are listed as 00000 and OBD (order by description), respectively, because these items can usually be purchased locally.

TORX® hardware is used in the assembly of the disc drive. This hardware requires the use of special drivers (refer to table 3-1). In this manual, any reference to this type of hardware will be accompanied by the appropriate driver size (for example, T15).

7-2. ORDERING INFORMATION

To order replaceable parts for the disc drive, address the order to your local Hewlett-Packard Sales and Support Office. Headquarter Offices are listed at the back of this manual. Specify the following information for each part ordered:

a. Model and full serial number.

b. Hewlett-Packard part number.

c. Complete description for each part as provided in the replaceable parts listings.

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Table 7-1. Disc Drive, Replaceable Parts

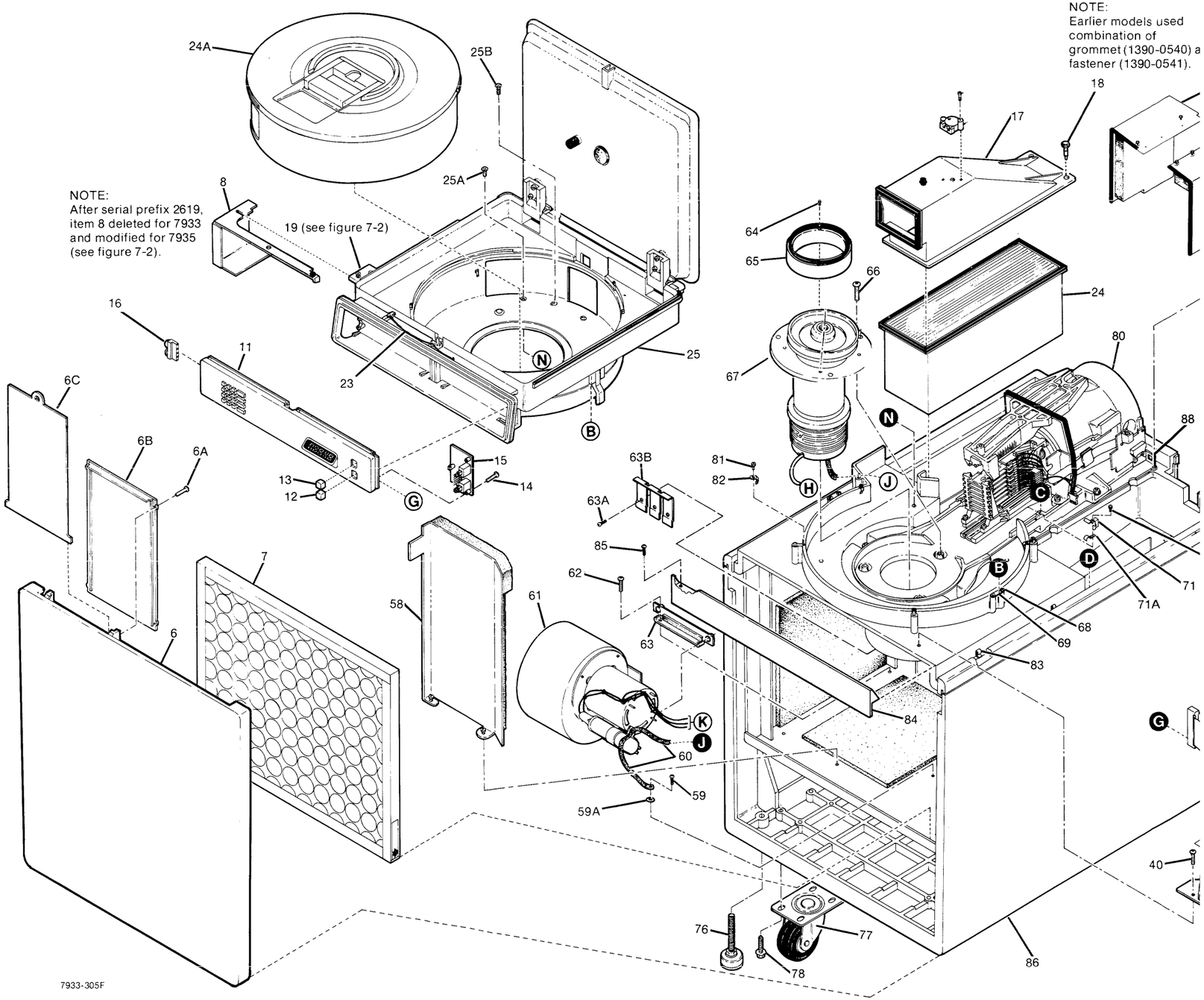
FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
7-1-	7933	DISC DRIVE	28480	7933	
1	07930-60178	*SHROUD ASSEMBLY	28480	07930-60178	1
2	07930-40062	**LATCH, shroud	28480	07930-40062	1
3	07930-40061	**RETAINER, shroud latch	28480	07930-40061	1
4	07930-00075	**SPRING, shroud latch	28480	07930-00075	1
5	07930-60224	*PANEL, rear	28480	07930-60224	1
6	07930-60214	*PANEL, front	28480	07930-60214	1
6A	0624-0528	**SCREW, tapping, fh, 82 degree (7935 only)	00000	OBD	4
6B	07935-40001	**COVER, information card (7935 only)	28480	07935-40001	1
6C	07935-80001	**CARD, information (7935 only)	28480	07935-80001	1
7	3150-0400	*PREFILTER	28480	3150-0400	1
8	07930-00069	*SHIELD, door latch (obsoleted, see figure 7-2)	28480	07930-00069	1
9	2360-0469	*SCREW, machine, pnh, T15, 6-32, 0.75 in. long, w/scw	00000	OBD	2
10	07930-60084	*CABLE ASSEMBLY (W5)	28480	07930-60084	1
11	07933-60049	*CONTROL PANEL ASSEMBLY (7933 only)	28480	07933-60049	1
	07935-60049	*CONTROL PANEL ASSEMBLY (7935 only)	28480	07935-60049	REF
12	5041-0368	**CAP, switch, blank (7933 only)	28480	5041-0368	1
	5041-2090	**CAP, switch, unlock door (7935 only)	28480	5041-2090	REF
13	5041-2007	**CAP, switch, load/unload	28480	5041-2007	1
14	0624-0556	**SCREW, tapping, washer hd, T9, 4-20, 0.625 in. long	00000	OBD	3
15	07930-60016	**LOAD/UNLOAD PCA (A16)	28480	07930-60016	1
16	07930-60241	*CONNECTOR, pressure switch	28480	07930-60241	1
17	07930-60179	*DUCT ASSEMBLY	28480	07930-60179	1
18	0515-0442	**SCREW, T30, M6 by 16 mm	00000	OBD	2
23	07930-80000	**SPRING, door latch (7933 only)	28480	07930-80000	1
24	07930-80238	*FILTER, absolute	28480	07930-80238	1
24A	97935-60000	*MEDIA MODULE ASSEMBLY, 7933 (see figure 7-6)	28480	97935-60000	1
	97935A	*MEDIA MODULE ASSEMBLY, 7935 (see figure 7-6)	28480	97935A	REF
25	07930-60031	*MEDIA MODULE CHAMBER ASSEMBLY (see figure 7-2)	28480	07930-60031	1
25A	0624-0519	**SCREW, tapping, fh, T10, 6-19, 0.375 in. long	00000	OBD	4
25B	0515-0695	**SCREW, machine, fh, T9, 90 degree, M3 by 0.5, 8 mm long)	00000	OBD	2
26	07930-60099	*CABLE ASSEMBLY (W6)	28480	07930-60099	1
27	07930-60126	*COVER, card cage	28480	07930-60126	1
28	07930-60109	*CABLE ASSEMBLY (W1)	28480	07930-60109	1
29	07930-40169	*CLIP, connector (see detail B)	28480	07930-40169	1
30	07930-60206	*HEAD CONTAMINATION SHIELD, right-hand	28480	07930-60206	1
31	07930-60172	*HEAD CONTAMINATION SHIELD, left-hand	28480	07930-60172	1
32	07930-60011	*REGULATOR PCA (A1)	28480	07930-60011	1
33	07930-60012	*ACTUATOR DRIVER PCA (A2)	28480	07930-60012	1
	07930-00067	**INSULATOR SHEET (attached to card cage, not shown)	28480	07930-00067	1
34	07930-60003	*SERVO PCA (A3)	28480	07930-60003	1
35	07930-60302	*MICROPROCESSOR PCA (A4)	28480	07930-60302	1
		**EPROM Kit for PCA-A4 (not shown, see service note for P/Ns)	28480		1
	07930-60258	*CACHE PCA (A5 - for XP drives only)	28480	07930-60258	1
	07930-60262	**RIBBON CABLE W7, A5 tp A6 (not shown - XP drives only)	28480	07930-60262	1
36	07930-60301	*DMA (or CDMA 07930-60357 if XP drive) PCA (A6)	28480	07930-60301	1
37	07930-60007	*FORMATTER/SEPARATOR PCA (A8)	28480	07930-60007	1
38	07930-60004	*TRACK FOLLOWER PCA (A9)	28480	07930-60004	1
39	07930-60006	*READ/WRITE PCA (A10)	28480	07930-60006	1
40	0624-0513	*SCREW, tapping, pnh, T9, 4-20, 0.5 in. long	00000	OBD	1
41	0515-0381	*SCREW, machine, pnh, T20, M4.0 by 0.7, 10 mm long	00000	OBD	3
42	07930-00031	*SHIELD, RFI	28480	07930-00031	1
43	0624-0521	*SCREW, tapping, pnh, T15, 6-19, 0.875 in. long	00000	OBD	2
44	07930-60210	*SHIELD, PCA-A10	28480	07930-60210	1
45	0624-0521	*SCREW, tapping, pnh, T15, 6-19, 0.875 in. long	00000	OBD	2
46	07930-60026	*HP-IB PCA (A17)	28480	07930-60026	1
47	07930-60061	*CABLE ASSEMBLY (W3)	28480	07930-60061	1
48	07930-60098	*CABLE ASSEMBLY (W4)	28480	07930-60098	1
49	0515-0372	*SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	2

Table 7-1. Disc Drive, Replaceable Parts (continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
7-1-					
50	07933-00002	*LABEL, power identification, 120/208V (7933 only)	28480	07933-00002	1
	07933-00003	*LABEL, power identification, 220/240V (7933 only)	28480	07933-00003	REF
	07933-00005	*LABEL, power identification, 208/220V (7933 only)	28480	07933-00005	REF
	07935-00002	*LABEL, power identification, 120/208V (7935 only)	28480	07935-00002	REF
	07935-00003	*LABEL, power identification, 220/240V (7935 only)	28480	07935-00003	REF
	07935-00005	*LABEL, power identification, 208/220V (7935 only)	28480	07935-00005	REF
51	0515-0386	*SCREW, machine, pnh, T25, M5.0 by 0.8, 10 mm long, w/scw	00000	OBD	12
52	07930-60177	*COVER, power module	28480	07930-60177	1
53	07930-60059	*CABLE ASSEMBLY (W2)	28480	07930-60059	1
54	0515-0789	*SCREW, tapping, pnh, T8, M2.5 by 0.45, 10 mm long	00000	OBD	18
55	07930-40021	*SHIELD, motherboard PCA	28480	07930-40021	1
56	07930-60008	*MOTHERBOARD PCA (A11)	28480	07930-60008	1
57	07930-60184	*CARD CAGE CHASSIS	28480	07930-60184	1
58	07930-60176	*BAFFLE PLATE ASSEMBLY	28480	07930-60176	1
59	0515-0433	*SCREW, machine, pnh, T15, M4.0 by 0.70, 8 mm long, w/scw	00000	OBD	1
59A	2190-0010	*WASHER, lock, ext. tooth, no. 8	00000	OBD	1
60	07930-60130	*GROUND CABLE ASSEMBLY	28480	07930-60130	1
61	07930-60249	*BLOWER ASSEMBLY (B3)	28480	07930-60249	1
62	0515-1375	*SCREW, machine, fh, T8, M2.5 by 0.45, 6 mm long	00000	OBD	2
63	07930-60192	*BLOWER SUPPORT ASSEMBLY	28480	07930-60192	1
63A	0624-0512	*SCREW, tapping, pnh, T9, 4-20, 0.375 in. long	00000	OBD	3
63B	07930-00087	*BRACKET, fan	28480	07930-00087	1
64	0515-0655	*SCREW, machine, pnh, T10, M3.0 by 0.50, 8 mm long	00000	OBD	4
65	07930-60197	*SEAL, contamination	28480	07930-60197	1
66	0515-0764	*SCREW, cap, T30, M6.0 by 1.0, 18 mm long	00000	OBD	3
67	07930-60036	*MOTOR-SPINDLE ASSEMBLY (B2) (see figure 7-3)	28480	07930-60036	1
68	0624-0519	*SCREW, tapping, 82-deg fh, T10, 0.375 in. long	00000	OBD	2
69	07930-00023	*PLATE, latch	28480	07930-00023	1
70	0515-0374	*SCREW, machine, pnh, T10, M3.0 by 0.5, 10 mm long, w/scw	00000	OBD	1
71	07930-00065	*RETAINER, servo cable	28480	07930-00065	1
71A	07930-00076	*GROUND STRIP	28480	07930-00076	4
72	0515-0641	*SCREW, tapping, pnh, T15, M4.0 by 0.7, 10 mm long	00000	OBD	8
73	No Number	*POWER MODULE ASSEMBLY (see figure 7-4)	28480	NSR	1
74	07930-60062	*SLIDE ASSEMBLY (Attaching Parts)	28480	07930-60062	2
75	0535-0004	*NUT, hex, M3.0 by 0.5 — — — x — — —	00000	OBD	4
76	0403-0467	*LEVELLER	28480	0403-0467	4
77	1492-0081	*CASTER (Attaching Parts)	06004	2689-1	4
78	0624-0523	*SCREW, tapping, washer hd, T30, 1/4-20, 1 in. long — — — x — — —	00000	OBD	4
79	10833A	*HP-IB CABLE ASSEMBLY, 1 m long	28480	10833A	1
	10833B	*HP-IB CABLE ASSEMBLY, 2 m long	28480	10833B	REF
	10833C	*HP-IB CABLE ASSEMBLY, 4 m long	28480	10833C	REF
79A	0380-1332	*STANDOFF, hex, 6-32, 0.180 in. long	00000	OBD	4
80	No Number	*ACTUATOR ASSEMBLY (see figure 7-5)	28480	NSR	1
81	0624-0520	*SCREW, tapping, pnh, T15, 6-19, 0.50 in. long	00000	OBD	4
82	07930-00074	*GROUND STRIP	28480	07930-00074	4
83	0363-0170	*GROUND STRIP	28480	0363-0170	4
84	07930-40035	*BELT BAND (Attaching Parts)	28480	07930-40035	1
85	0624-0556	*SCREW, tapping, T9, 4-20, 0.625 in. long — — — x — — —	00000	OBD	4
86	No Number	*CABINET ASSEMBLY	28480	NSR	1
87	07930-60246	**SUBPANEL KIT	28480	07930-60246	1
88	07930-00001	**GROUND PLATE (shroud latch catch)	28480	07930-00001	1

·ts (continued)

	MFR CODE	MFR PART NO.	UNITS PER ASSY
	28480	07933-00002	1
	28480	07933-00003	REF
	28480	07933-00005	REF
	28480	07935-00002	REF
	28480	07935-00003	REF
	28480	07935-00005	REF
, w/scw	00000	OBD	12
	28480	07930-60177	1
	28480	07930-60059	1
	00000	OBD	18
	28480	07930-40021	1
	28480	07930-60008	1
	28480	07930-60184	1
	28480	07930-60176	1
g,	00000	OBD	1
	00000	OBD	1
	28480	07930-60130	1
	28480	07930-60249	1
	00000	OBD	2
	28480	07930-60192	1
	00000	OBD	3
	28480	07930-00087	1
g	00000	OBD	4
	28480	07930-60197	1
	00000	OBD	3
	28480	07930-60036	1
	00000	OBD	2
	28480	07930-00023	1
g,	00000	OBD	1
	28480	07930-00065	1
	28480	07930-00076	4
	00000	OBD	8
	28480	NSR	1
	28480	07930-60062	2
	00000	OBD	4
	28480	0403-0467	4
	06004	2689-1	4
	00000	OBD	4
	28480	10833A	1
	28480	10833B	REF
	28480	10833C	REF
	00000	OBD	4
	28480	NSR	1
	00000	OBD	4
	28480	07930-00074	4
	28480	0363-0170	4
	28480	07930-40035	1
	00000	OBD	4
	28480	NSR	1
	28480	07930-60246	1
	28480	07930-00001	1



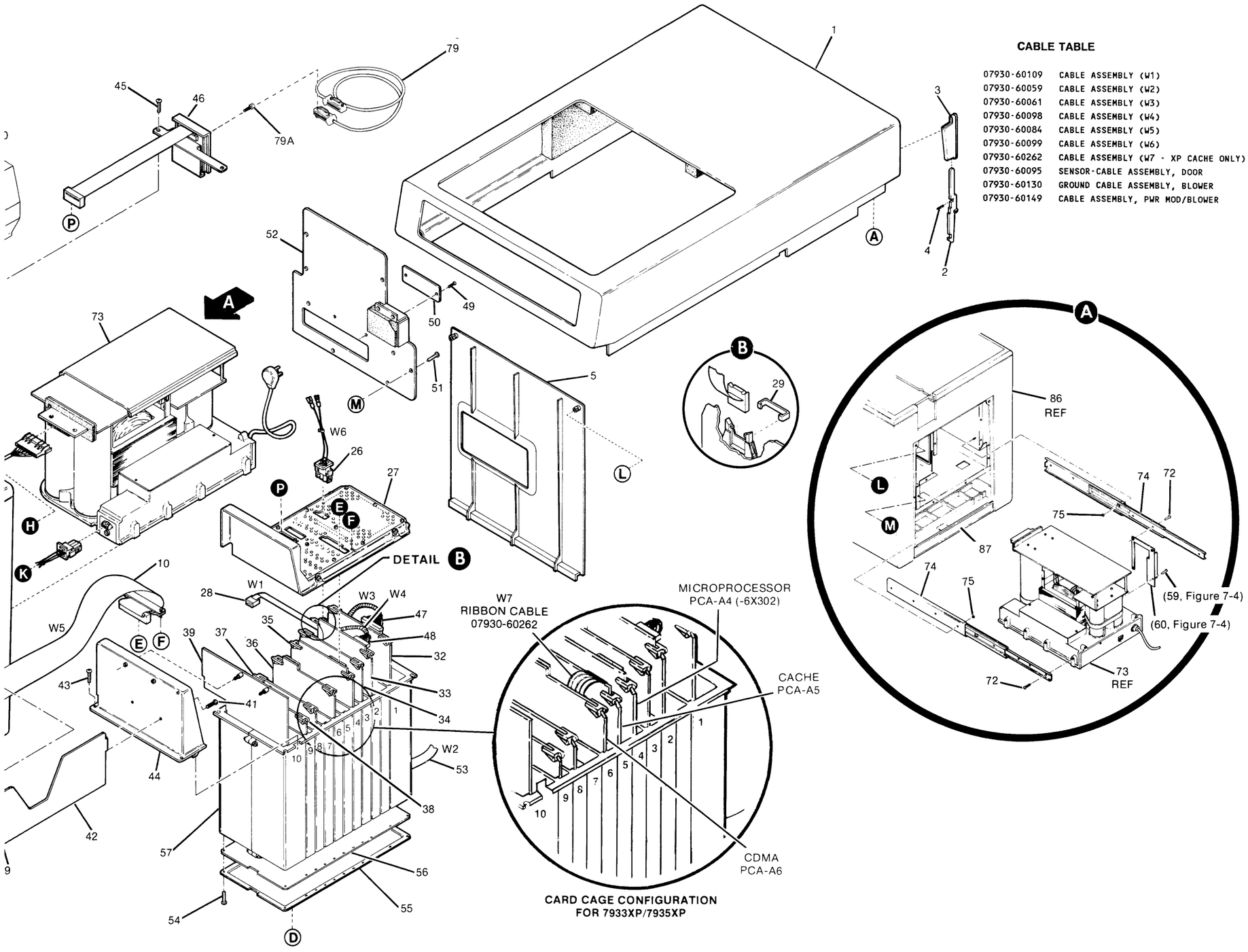
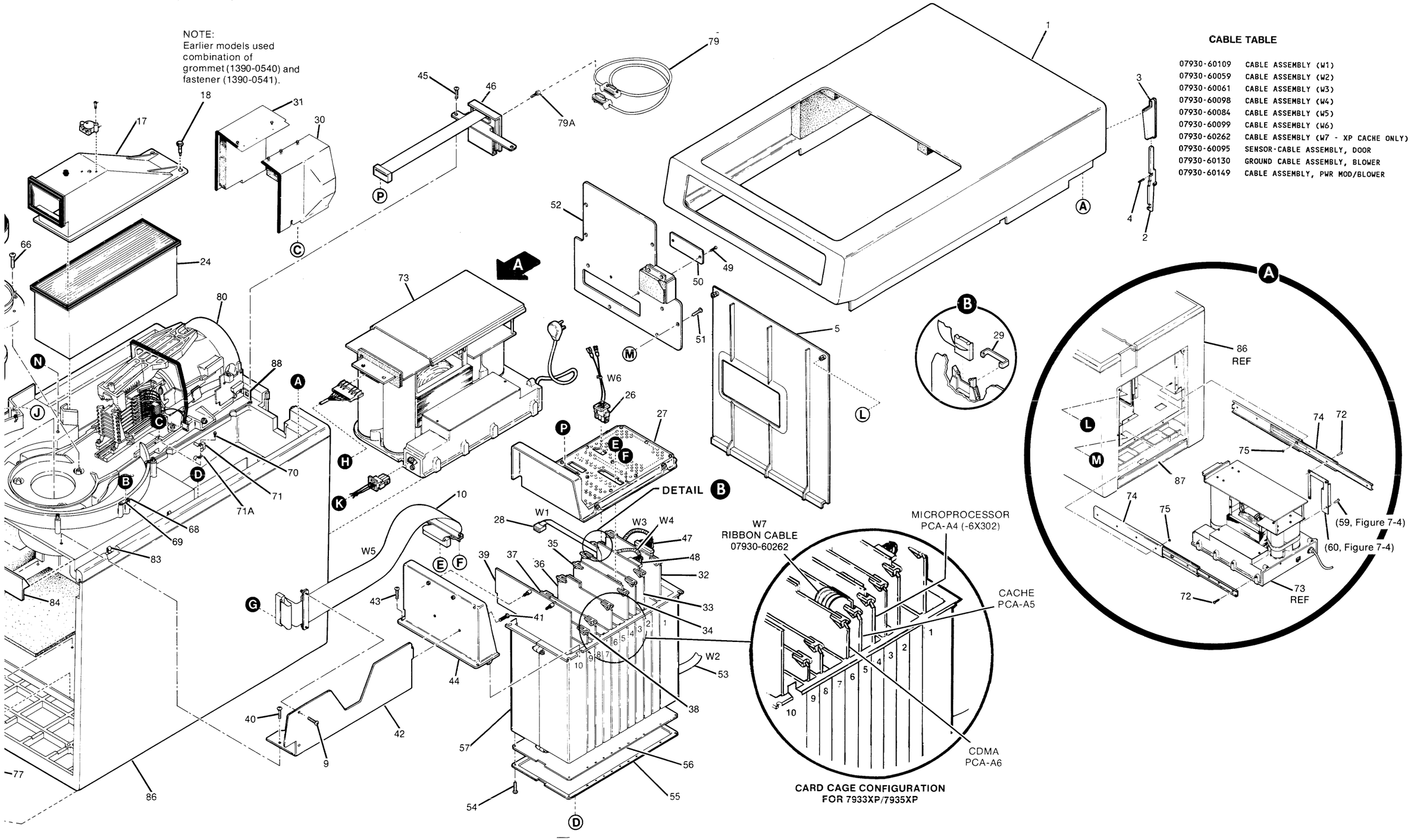


Figure 7-1. Disc Drive, Exploded View

Table 7-2. Medi

FIG. & INDEX NO.	HP PART NO.	D
7-2-	07930-60031	MEDIA MODULE CHAMI
1	0624-0512	*SCREW, tapping, pnh, T
2	07930-40147	*HOLDER, magnet
3	9164-0172	*MAGNET
3A	0515-0638	*SCREW, machine, pnh,
3B	2190-0587	*WASHER, lock, helical,
3C	3050-0894	*WASHER, flat, 5.0 mm
3D	07930-40161	*POST, media module lo
4	0515-0638	*SCREW, machine, pnh,
5	2190-0587	*WASHER, lock, helical,
6	3050-0894	*WASHER, flat, 5.0 mm
7	07930-60205	*TOP DOOR ASSEMBLY
7A	07933-00001	**NAMEPLATE, product,
	07935-00001	**NAMEPLATE, product,
8	0624-0555	*SCREW, tapping, pnh, T
9	07930-60181	*HINGE ASSEMBLY, top
10	07930-00071	*RFI FINGER, left-hand
11	07930-00072	*RFI FINGER, right-hand
12	07930-40042	*RETAINER, right-hand (Attaching Parts)
13	0624-0513	*SCREW, tapping, pnh, T — — — x — — —
14	07930-40065	*RETAINER, left-hand (Attaching Parts)
15	0624-0513	*SCREW, tapping, pnh, T — — — x — — —
16	0520-0133	*SCREW, machine, pnh,
17	0535-0011	*NUT, hex, M2.0 by 0.4, r
18	2360-0461	*SCREW, machine, 82-de
19	07930-60096	*SOLENOID ASSEMBLY
19A	07930-60268	*SHIELD, door latch (793
	07930-80235	**CAUTION LABEL (not
20	0624-0544	*SCREW, tapping, pnh, T
21	2190-0464	*WASHER, flat, no. 6
22	07930-00005	*LEVER, door latch (793
23	07930-60095	*SENSOR CABLE ASSEI
24		Deleted
25		Not Assigned
26		Not Assigned
27		Deleted
28		Deleted
29	1390-0539	*RETAINER, spring (Attaching Parts)
30	0624-0510	*SCREW, tapping, pnh, T — — — x — — —
31	07930-60190	*LATCH, door opening,
32	No Number	*TUB ASSEMBLY
33	07930-20153	*LATCH, media chambe
	1480-0022	**DOWEL, pin



CARD CAGE CONFIGURATION FOR 7933XP/7935XP

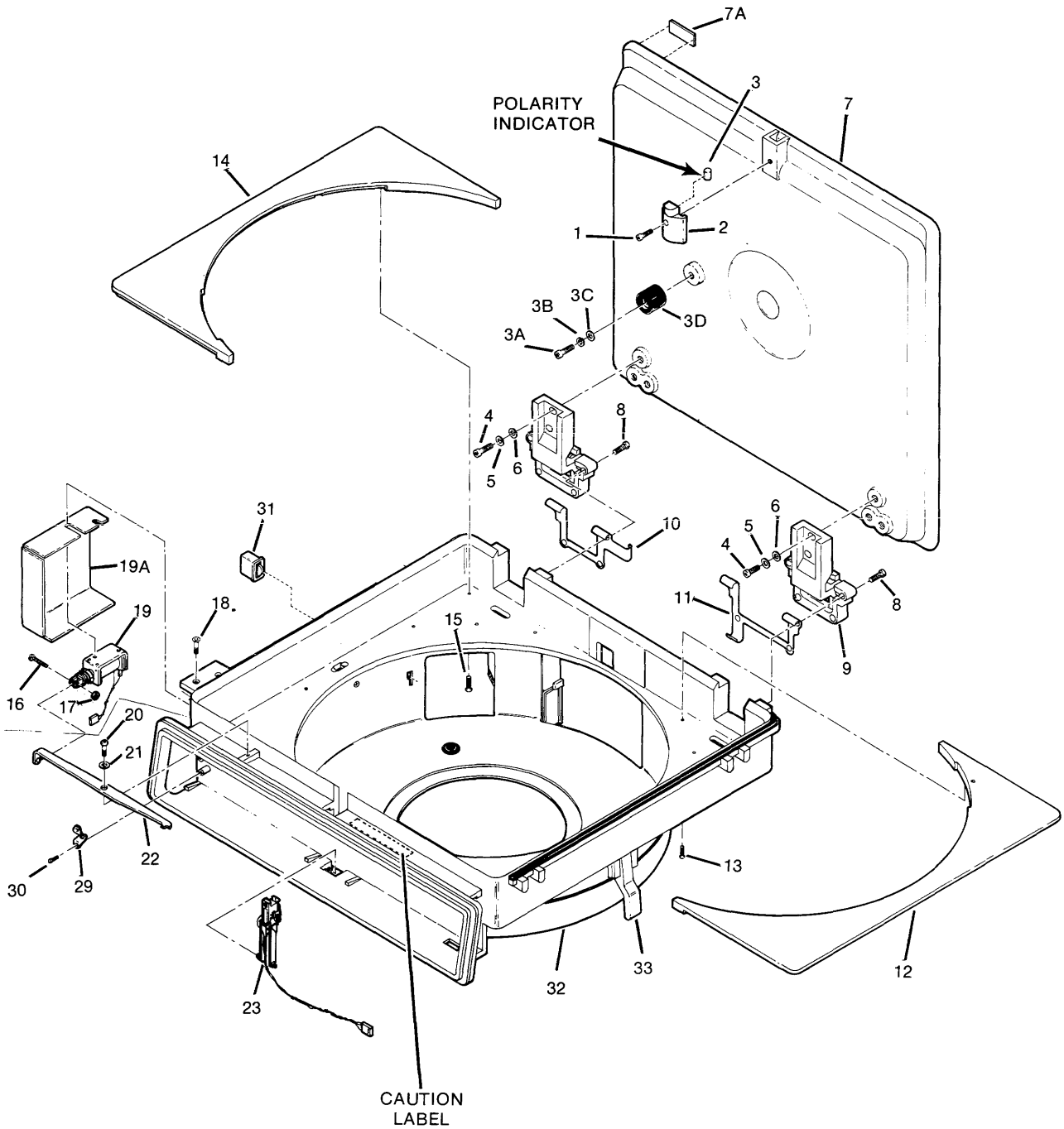
CABLE TABLE

07930-60109	CABLE ASSEMBLY (W1)
07930-60059	CABLE ASSEMBLY (W2)
07930-60061	CABLE ASSEMBLY (W3)
07930-60098	CABLE ASSEMBLY (W4)
07930-60084	CABLE ASSEMBLY (W5)
07930-60099	CABLE ASSEMBLY (W6)
07930-60262	CABLE ASSEMBLY (W7 - XP CACHE ONLY)
07930-60095	SENSOR-CABLE ASSEMBLY, DOOR
07930-60130	GROUND CABLE ASSEMBLY, BLOWER
07930-60149	CABLE ASSEMBLY, PWR MOD/BLOWER

Figure 7-1. Disc Drive, Exploded View

Table 7-2. Media Module Chamber, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
7-2-	07930-60031	MEDIA MODULE CHAMBER ASSEMBLY (25, figure 7-1)	28480	07930-60031	REF
1	0624-0512	*SCREW, tapping, pnh, T9, 4-20, 0.375 in. long	00000	OBD	1
2	07930-40147	*HOLDER, magnet	28480	07930-40147	1
3	9164-0172	*MAGNET	00685	101MG7	1
3A	0515-0638	*SCREW, machine, pnh, T25, M5.0 by 0.8, 14 mm long	00000	OBD	1
3B	2190-0587	*WASHER, lock, helical, 5.0 mm	00000	OBD	1
3C	3050-0894	*WASHER, flat, 5.0 mm	00000	OBD	1
3D	07930-40161	*POST, media module locating	28480	07930-40161	1
4	0515-0638	*SCREW, machine, pnh, T25, M5.0 by 0.8, 14 mm long	00000	OBD	6
5	2190-0587	*WASHER, lock, helical, 5.0 mm	00000	OBD	6
6	3050-0894	*WASHER, flat, 5.0 mm	00000	OBD	6
7	07930-60205	*TOP DOOR ASSEMBLY (order with appropriate nameplate)	28480	07930-60205	1
7A	07933-00001	**NAMEPLATE, product, 7933 (order with top door assembly)	28480	07933-00001	1
	07935-00001	**NAMEPLATE, product, 7935 (order with top door assembly)	28480	07935-00001	REF
8	0624-0555	*SCREW, tapping, pnh, T10, 8-19, 1 in. long	00000	OBD	8
9	07930-60181	*HINGE ASSEMBLY, top door	28480	07930-60181	2
10	07930-00071	*RFI FINGER, left-hand	28480	07930-00071	1
11	07930-00072	*RFI FINGER, right-hand	28480	07930-00072	1
12	07930-40042	*RETAINER, right-hand	28480	07930-40042	1
		(Attaching Parts)			
13	0624-0513	*SCREW, tapping, pnh, T9, 4-20, 0.5 in. long	00000	OBD	8
		— — — x — — —			
14	07930-40065	*RETAINER, left-hand	28480	07930-40065	1
		(Attaching Parts)			
15	0624-0513	*SCREW, tapping, pnh, T9, 4-20, 0.5 in. long	00000	OBD	8
		— — — x — — —			
16	0520-0133	*SCREW, machine, pnh, pozi, 2-56, 0.50 in. long	00000	OBD	1
17	0535-0011	*NUT, hex, M2.0 by 0.4, nylon	00000	OBD	1
18	2360-0461	*SCREW, machine, 82-deg fh, T10, 6-32, 0.375 in. long	00000	OBD	2
19	07930-60096	*SOLENOID ASSEMBLY (7935 only)	28480	07930-60096	1
19A	07930-60268	*SHIELD, door latch (7935 only)	28480	07930-60268	1
	07930-80235	**CAUTION LABEL (not shown)	28480	07930-80235	1
20	0624-0544	*SCREW, tapping, pnh, T10, 6-19, 0.375 in. long	00000	OBD	1
21	2190-0464	*WASHER, flat, no. 6	00000	OBD	1
22	07930-00005	*LEVER, door latch (7935 only)	28480	07930-00005	1
23	07930-60095	*SENSOR CABLE ASSEMBLY	28480	07930-60095	1
24		Deleted			
25		Not Assigned			
26		Not Assigned			
27		Deleted			
28		Deleted			
29	1390-0539	*RETAINER, spring	78553	C4883-022-07	2
		(Attaching Parts)			
30	0624-0510	*SCREW, tapping, pnh, T9, 4-20, 0.250 in. long	00000	OBD	2
		— — — x — — —			
31	07930-60190	*LATCH, door opening, media module	28480	07930-60190	1
32	No Number	*TUB ASSEMBLY	28480	NSR	1
33	07930-20153	*LATCH, media chamber	28480	07930-20153	1
	1480-0022	**DOWEL, pin	28480	1480-0022	1



NOTE:

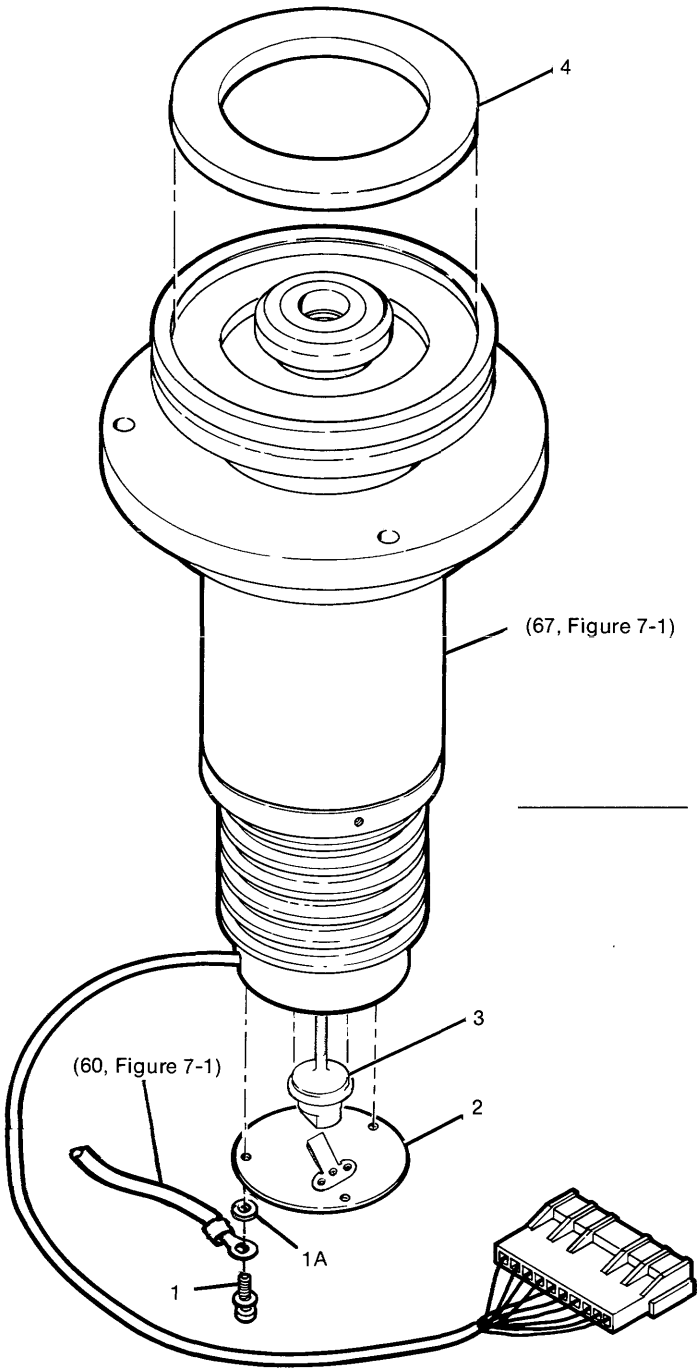
For model 7933, delete solenoid (item 19) and shield (item 19A); substitute spring shown in figure 7-1 (item 23) for lever (item 22).

7933-307C

Figure 7-2. Media Module Chamber, Exploded View

Table 7-3. Motor-Spindle Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
7-3-	07930-60036	MOTOR-SPINDLE ASSEMBLY (67, figure 7-1)	28480	07930-60036	REF
1	0515-0380	*SCREW, machine, pnh, T15, M4.0 by 0.70, 10 mm long, w/scw	00000	OBD	3
1A	2190-0010	*WASHER, lock, ext. tooth, no. 8	00000	OBD	1
	07930-60234	*SPINDLE GROUND KIT (includes items 2 and 3)	28480	07930-60234	REF
2	07930-60233	**COVER ASSEMBLY, bottom	28480	07930-60233	1
3	07930-60232	**GROUND BUTTON ASSEMBLY	28480	07930-60232	1
4	07930-40148	*RING, magnetic, coated	28480	07930-40148	1



7933-306C

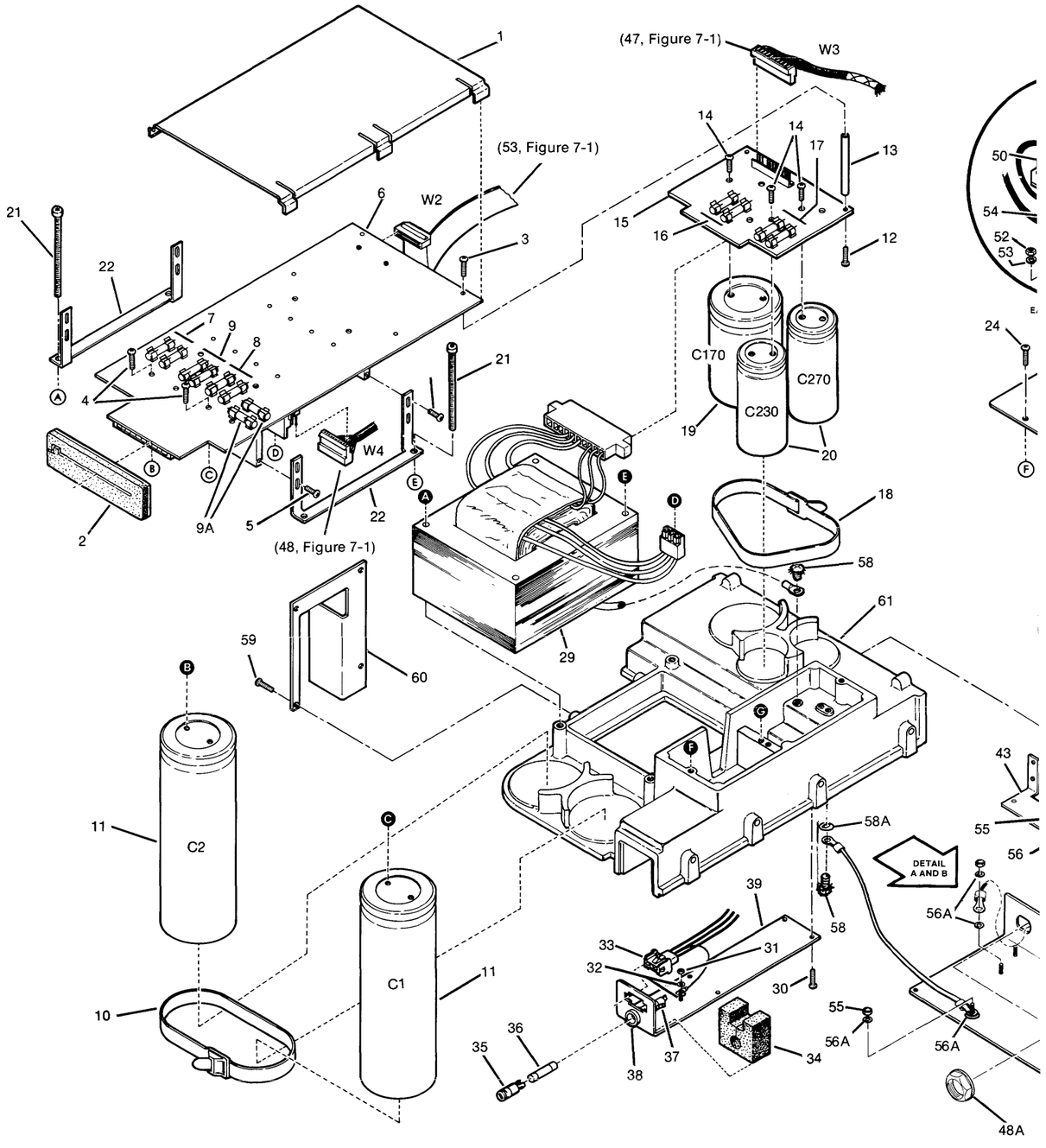
Figure 7-3. Motor-Spindle Assembly, Exploded View

Table 7-4. Power Module Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
7-4-	No Number	POWER MODULE ASSEMBLY (73, figure 7-1)	28480	NSR	REF
1	07930-40123	*COVER, PCA-A12	28480	07930-40123	1
2	07930-60045	*SEAL, air	28480	07930-60045	1
3	0515-0372	*SCREW, machine, pnh, T10, M3.0 by 0.50, 8 mm long, w/scw	00000	OBD	2
4	2680-0278	*SCREW, machine, pnh, T25, 10-32, 0.50 in. long, w/scw	00000	OBD	4
5	0515-0752	*SCREW, tapping, pnh, T15, M4.0 by 0.70, 10 mm long, w/scw	00000	OBD	4
6	07930-60010	*SPINDLE DRIVER PCA (A12)	28480	07930-60010	1
7	2110-0051	**FUSE, 10A 250V (F580, F590)	60016	314010	2
8	2110-0327	**FUSE, 15A 250V SB (F540, F550)	03614	MDA-15	2
9	2110-0640	**FUSE, 7A 250V SB (F560, F570)	60016	313007	2
9A	2110-0661	**FUSE, 30A 125V (F510, F520)	03614	MDA-30	2
10	1400-1149	*CLAMP, capacitor	28480	1400-1149	1
11	0180-3088	*CAPACITOR, 0.067F, +75 -10%, 60 WVDC (C1, C2)	56699	86F-6209	2
12	0515-0372	*SCREW, machine, pnh, T10, M3.0 by 0.50, 8 mm long, w/scw	00000	OBD	2
13	07930-20052	*SUPPORT, PCA	28480	07930-20052	2
14	2680-0278	*SCREW, machine, pnh, T25, 10-32, 0.50 in. long, w/scw	00000	OBD	6
15	07930-60013	*DC POWER PCA (A13)	28480	07930-60013	1
16	2110-0649	**FUSE, 20A 32V (F110, F115)	03614	AGC-20	2
17	2110-0014	**FUSE, 4A 250V SB (F210, F215)	60016	313004	2
18	1400-1149	*CLAMP, capacitor	28480	1400-1149	1
19	0180-3120	*CAPACITOR, 0.082F, +75 -20%, 20 WVDC (C170)	56699	3188GE823U020AGA	1
20	0180-3091	*CAPACITOR, 0.41F, +75 -20%, 30 WVDC (C230, C270)	56699	86F6133H	2
21	0515-0388	*SCREW, cap, T30, M6.0 by 1.0, 100 mm long, w/scw	00000	OBD	4
22	07930-00053	*SUPPORT, heat sink	28480	07930-00053	2
23	07930-00016	*COVER, strapping chamber	28480	07930-00016	1
		(Attaching Parts)			
24	0515-0788	*SCREW, tapping, 90-deg fh, T10, M4.0 by 0.70, 10 mm long — — — x — — —	00000	OBD	2
25	0515-0458	*SCREW, machine, pnh, T10, M3.5 by 0.60, 8 mm long, w/scw	00000	OBD	14
	07930-60105	*STRAPPING WIRE KIT	28480	07930-60105	1
26	0515-0640	*SCREW, tapping, pnh, T15, M4.0 by 0.70, 16 mm long, w/scw	00000	OBD	4
27	0360-2060	*TERMINAL BLOCK (TB1)	28480	0360-2060	1
28	0360-0625	*STRIP MARKER	75382	MS671-7-1A	1
29	9100-4145	*TRANSFORMER, power (T1)	05216	PX-4253	1
30	0515-0788	*SCREW, tapping, 90-deg fh, T10, M4.0 by 0.70, 10 mm long	00000	OBD	4
	07930-60203	*BLOWER POWER DISTRIBUTION ASSEMBLY	28480	07930-60203	1
31	0535-0022	**NUT, hex, M5.0 by 0.8	00000	OBD	1
32	2190-0467	**WASHER, lock, ext. tooth, no. 10	00000	OBD	2
33	07930-60149	**CABLE ASSEMBLY	28480	07930-60149	1
34	07930-80169	**GASKET	28480	07930-80169	1
35	2110-0565	**CAP, fuseholder	28480	2110-0565	1
36	2110-0640	**FUSE, 7A 250V SB (F1)	60016	313007	1
37	2110-0569	**NUT, fuseholder	28480	2110-0569	1
38	2110-0566	**FUSEHOLDER	28480	2110-0566	1
39	07930-00081	**COVER, blower power assembly	28480	07930-00081	1
40	0515-0788	*SCREW, tapping, 90-deg fh, T10, M4.0 by 0.70. 10 mm long	00000	OBD	3
41	8120-3364	*POWER CORD (standard)	16428	CH77340	1
	07930-60211	*POWER CORD (option 120)	28480	07930-60211	REF
	8120-4065	*POWER CORD (option 210, 220)	28480	8120-4065	REF
	8120-3307	*POWER CORD (option 221)	28480	8120-3307	REF
	8120-3306	*POWER CORD (option 222)	28480	8120-3306	REF
	8120-3330	*POWER CORD (option 223)	28480	8120-3330	REF
	8120-3332	*POWER CORD (option 241)	28480	8120-3332	REF
	8120-3752	*POWER CORD (option 242)	28480	8120-3752	REF
	07930-60204	*INPUT POWER ASSEMBLY	28480	07930-60204	1
42	0515-0372	**SCREW, machine, pnh, T10, M3.0 by 0.50, 8 mm long, w/scw	00000	OBD	2
43	07930-00029	**SUPPORT	28480	07930-00029	1
	07930-60108	**PRIMARY POWER WIRING KIT	28480	07930-60108	1
44	0515-0372	**SCREW, machine, pnh, T10, M3.0 by 0.50, 8 mm long, w/scw	00000	OBD	4
45	3105-0155	**CIRCUIT BREAKER (S1)	14280	QOU-220/S369	1
46	0515-0374	**SCREW, machine, pnh, T10, M3.0 by 0.50, 10 mm long, w/scw	00000	OBD	4

Table 7-4. Power Module Assembly, Replaceable Parts (continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
7-4-					
47	07930-60021	**LINE FILTER PCA (A21)	28480	07930-60021	1
48	07930-20178	**CONNECTOR, strain relief (was Grommet)	28480	07930-20178	1
48A	07930-80254	**LOCKNUT, plastic	28480	07930-80254	1
49	0535-0025	**NUT, hex, M3.0 by 0.5, 2.4 mm thick	00000	OBD	REF
50	07930-60180	**CONNECTOR, receptacle	28480	07930-60180	REF
51		Not Assigned			
52	0535-0022	**NUT, hex, M5.0 by 0.8	00000	OBD	1
53	2190-0587	**WASHER, lock, helical, M5.0	00000	OBD	1
54	0362-0776	**GROUND TERMINAL, bronze (Attaching Parts)	74159	PNL-8	2
55	0535-0022	**NUT, hex, M5.0 by 0.8	00000	OBD	4
56	2190-0011	**WASHER, lock, int. tooth, no. 10	00000	OBD	2
56A	2190-0467	**WASHER, lock, ext. tooth, no. 10	00000	OBD	4
		— — — X — — —			
57	07930-00082	**COVER, input power assembly	28480	07930-00082	1
58	0515-0752	*SCREW, tapping, pnh, T15, M4.0 by 0.70, 10 mm long, w/scw	00000	OBD	1
58A	2190-0010	*WASHER, lock, ext. tooth, no. 8	00000	OBD	1
59	0515-0752	*SCREW, tapping, pnh, T15, M4.0 by 0.70, 10 mm long, w/scw	00000	OBD	2
60	07930-00054	*DEFLECTOR, air	28480	07930-00054	1
61	No Number	*CASTING, power module	28480	NSR	1



ntinued)

R DE	MFR PART NO.	UNITS PER ASSY
80	07930-60021	1
80	07930-20178	1
80	07930-80254	1
00	OBD	REF
80	07930-60180	REF
00	OBD	1
00	OBD	1
59	PNL-8	2
00	OBD	4
00	OBD	2
00	OBD	4
80	07930-00082	1
00	OBD	1
00	OBD	1
00	OBD	2
80	07930-00054	1
80	NSR	1

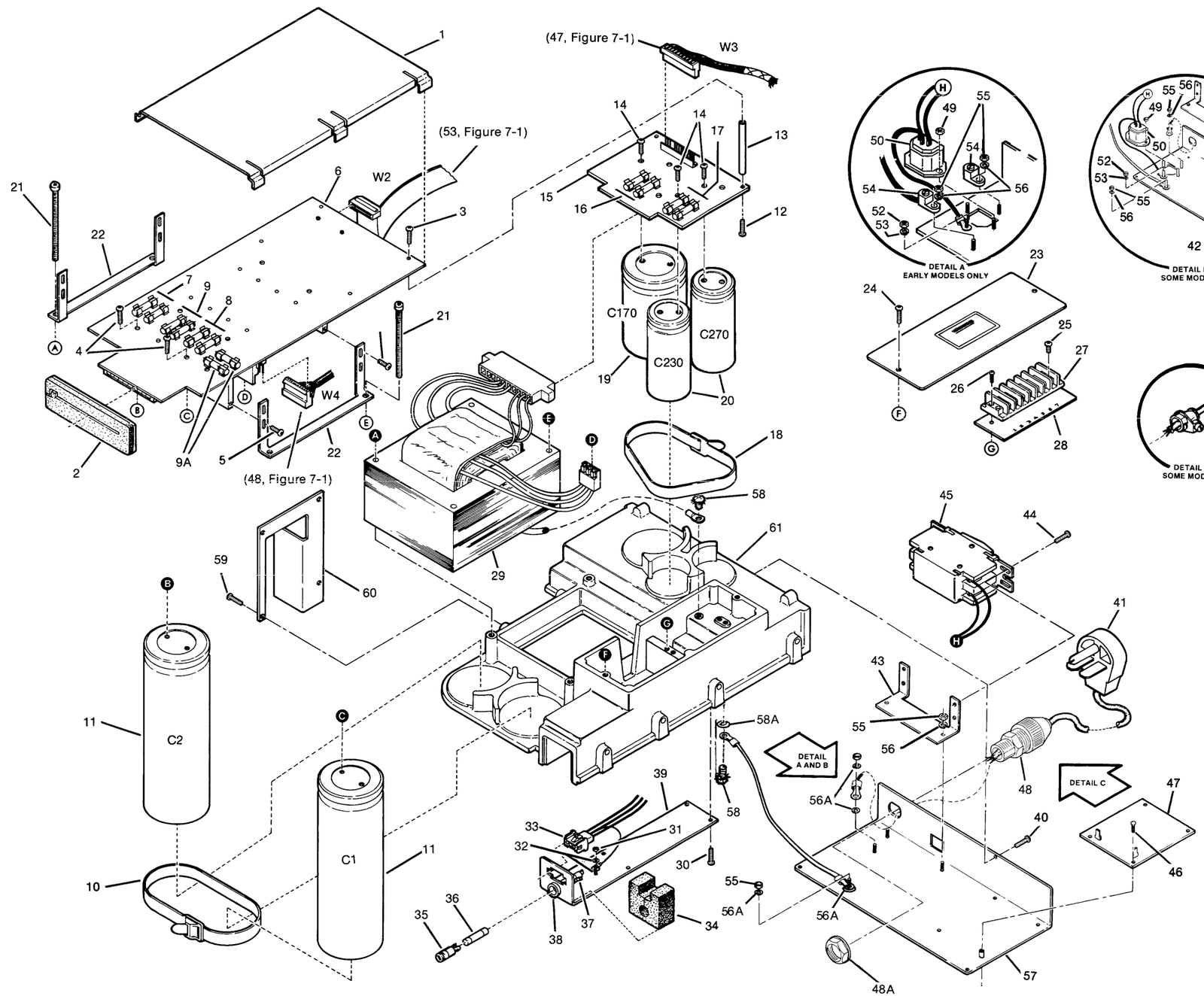


Figure 7-4. Power Module Assembly, Exploded View

Table 7-5. Actuator Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
7-5-	No Number	ACTUATOR ASSEMBLY (80, figure 7-1)	28480	NSR	REF
1	07930-60229	*VELOCITY TRANSDUCER	28480	07930-60229	1
		(Attaching Parts)			
2		Deleted			
3	0515-0794	*SCREW, machine, pnh, T9, M3.0 by 0.50, 8 mm long, with patch lock	00000	OBD	3
4	07930-00080	*RETAINER	28480	07930-00080	1
		— — — x — — —			
5	07930-60227	*SHAFT, velocity transducer	28480	07930-60227	1
		(Attaching Parts)			
6	0515-0763	*SETSCREW, hex, M3.0 by 0.50, 6 mm long	00000	OBD	1
		— — — x — — —			
7	0515-0769	*SCREW, cap, T15, M4.0 by 0.70, 30 mm long, with patch lock	00000	OBD	2
8	0491-0093	*SOLENOID, carriage latch (superseded, order item 11	21790	0491-0093	1
9	2200-0598	*SCREW, machine, pnh, T9, 4-40, 0.250 in. long	00000	OBD	2
10	3050-0229	*WASHER, flat, no. 4	00000	OBD	2
11	07930-60228	*ASSEMBLY, solenoid lock (replaces old solenoid and bracket)	28480	07930-60228	1
12	07930-60254	*HEAD ASSEMBLY, data, down	28480	07930-60254	6
13	07930-60255	*HEAD ASSEMBLY, servo	28480	07930-60255	1
14	07930-60253	*HEAD ASSEMBLY, data, up	28480	07930-60253	7
15	0515-0374	*SCREW, machine, pnh, T10, M3.0 by 0.50, 10 mm long, w/scw	00000	OBD	4
16	07930-60038	*CARRIAGE ASSEMBLY	28480	07930-60038	1
17	0515-0365	**SCREW, machine, pnh, T6, M2.0 by 0.40, 4 mm long, w/scw	00000	OBD	2
18	07930-00021	**PLATE, retainer	28480	07930-00021	1
19	3030-0925	**SCREW, cap, hex, 4-40, 0.5 in. long	00000	OBD	14
20	2190-0376	**WASHER, flat, no. 4	00000	OBD	14
21	1460-1661	**SPRING	28480	1460-1661	1
22	07930-40130	*SUPPORT, PCA	28480	07930-40130	1
		(Attaching Parts)			
23	0515-0374	*SCREW, machine, pnh, T10, M3.0 by 0.50, 10 mm long, w/scw	00000	OBD	2
		— — — x — — —			
24	07930-40059	*PAD, crash stop	28480	07930-40059	2
25	07930-60217	*CAM TOWER ASSEMBLY, left (supplied with crash stop pad)	28480	07930-60217	1
25A	07930-60218	*CAM TOWER ASSEMBLY, right (supplied with crash stop pad)	28480	07930-60218	1
		(Attaching Parts for items 25 and 25A)			
26	0515-0384	*SCREW, cap, T15, M4.0 by 0.70, 16 mm long	00000	OBD	2
		— — — x — — —			
27		Not Assigned			
28		Not Assigned			
29		Not Assigned			
30		Not Assigned			
31		Not Assigned			
32		Not Assigned			
33		Not Assigned			
34		Not Assigned			
35	0515-0373	*SCREW, machine, pnh, T10, M3.0 by 0.50, 10 mm long	00000	OBD	4
36	07930-40102	*COVER, coil band	28480	07930-40102	1
36A	1400-0611	**CABLE CLAMP, stick-on	28480	1400-0611	1
37	07930-60047	*ARMATURE ASSEMBLY	28480	07930-60047	1
38	0515-0373	*SCREW, machine, pnh, T10, M3.0 by 0.50, 10 mm long	00000	OBD	2
39	3050-0805	*WASHER, nylon, flat, no. 6, 0.135 in. thick	00000	OBD	2
40	07930-60018	*ACTUATOR STATUS PCA (A18)	28480	07930-60018	1
40A	07930-40169	*CLIP, connector	28480	07930-40169	1
41	0515-0374	*SCREW, machine, pnh, T10, M3.0 by 0.50, 10 mm long, w/scw	00000	OBD	7

Table 7-5. Actuator Assembly, Replaceable Parts (continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
7-5-					
42	07930-40012	*CLAMP, lower rail	28480	07930-40012	1
43	07930-20060	*RAIL, lower	28480	07930-20060	1
44	0515-0374	*SCREW, machine, pnh, T10, M3.0 by 0.50, 10 mm long, w/scw	00000	OBD	3
45	4040-1103	*CLAMP, upper rail	31846	0559001P	1
46	1530-1924	*RAIL, upper	28480	1530-1924	1
47	07930-40059	*PAD, crash stop	28480	07930-40059	2
48	No Number	*LINEAR MOTOR ASSEMBLY (B1)	28480	NSR	1
49	No Number	*BASE ASSEMBLY	28480	NSR	1
50	0460-1286	*TAPE, gasket, self-adhesive, 0.25 in. wide, 0.25 in. thick	28480	0460-1286	1
51	07930-60256	*REAR CRASH PAD ASSEMBLY	28480	07930-60256	1
	0515-0655	**SCREW, machine, pnh, T10, M3.0 by 0.50, 10 mm long	00000	OBD	2

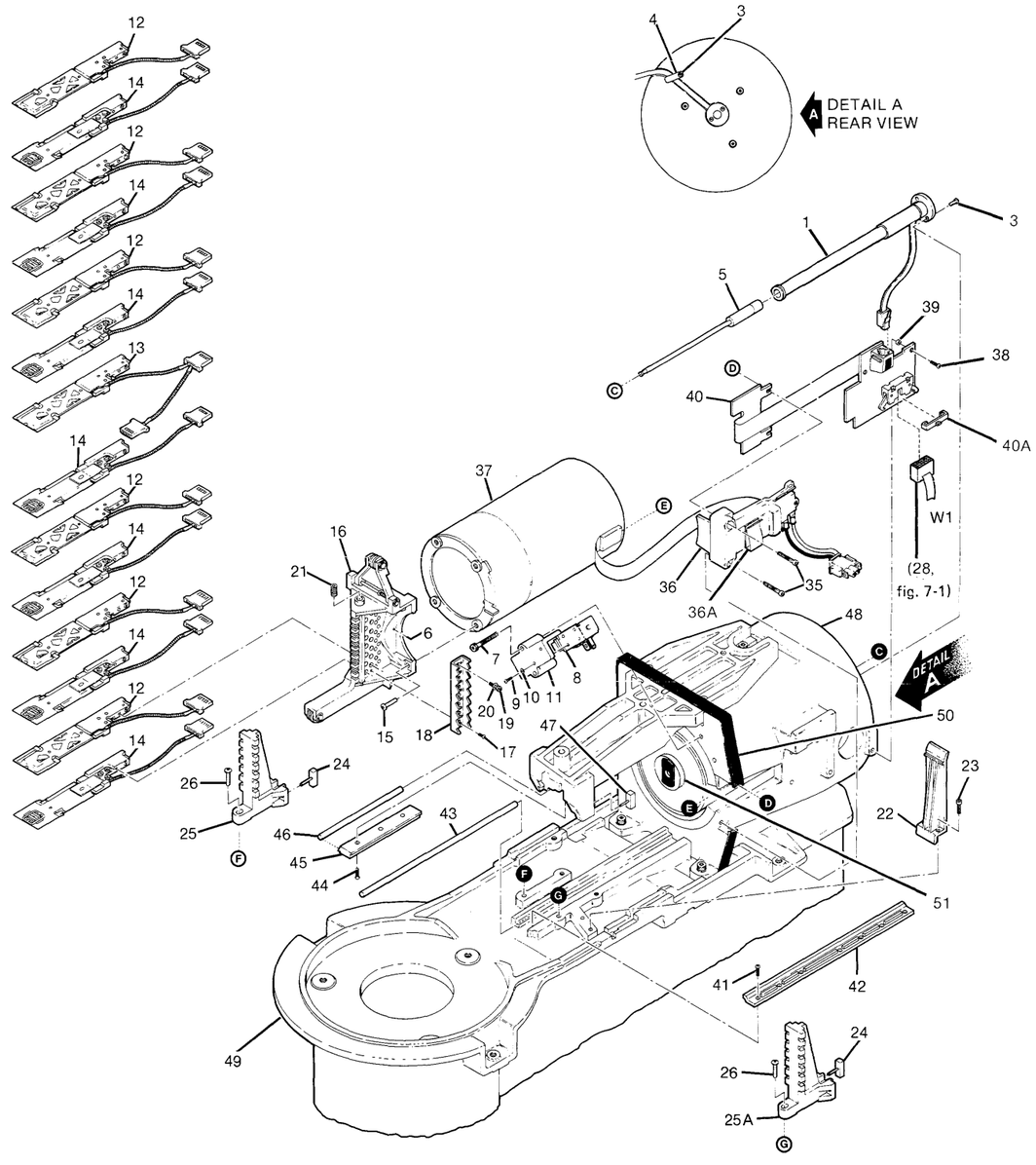
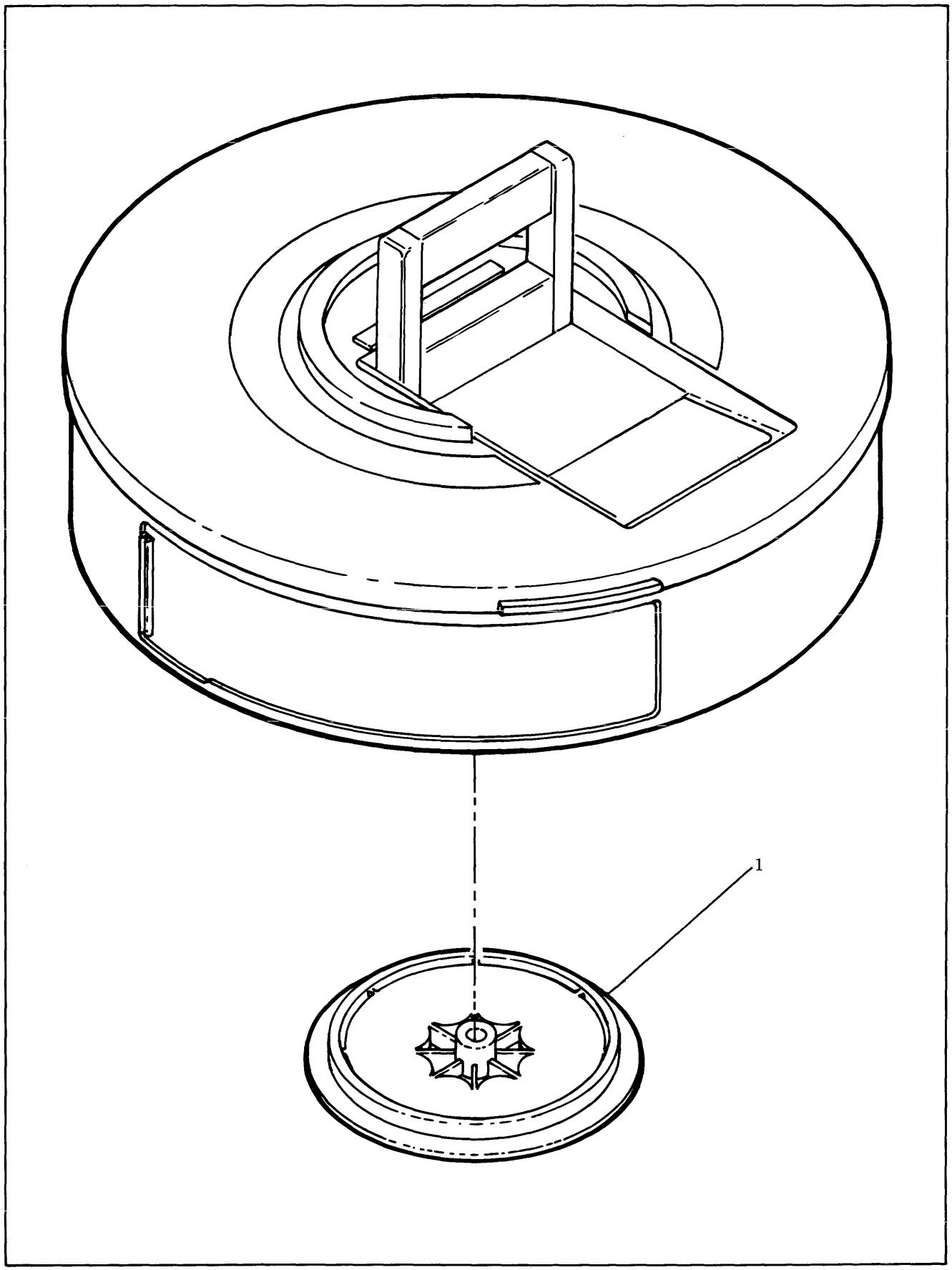


Figure 7-5. Actuator Assembly, Exploded View

Table 7-6. Media Module, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
7-6-	97935-60000	MEDIA MODULE, 7933 (24A, figure 7-1)	28480	97935-60000	REF
	97935A	MEDIA MODULE, 7935 (24A, figure 7-1)	28480	97935A	REF
1	97935-60012	*COVER, removable	28480	97935-60012	1
	9222-0944	*BAG, plastic, protective antistatic	28480	9222-0944	REF



7933-311A

Figure 7-6. Media Module, Exploded View

Table 7-7. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	J	= jack, receptacle connector	T	= transformer
B	= blower, fan, motor, synchro	K	= relay	TB	= terminal board
C	= capacitor	L	= inductor	TP	= test point
CB	= circuit breaker	M	= meter	U	= integrated circuit, non-repairable assembly
CR	= diode	MP	= mechanical part		
DS	= indicator lamp	P	= plug connector	VR	= voltage retulator
E	= contact, miscellaneous electrical part	Q	= semiconductor device other than diode or integrated circuit	W	= cable assembly (with connectors), wire
F	= fuse	R	= resistor	X	= socket
FL	= filter	RT	= thermistor	Y	= crystal unit
H	= hardware	S	= switch	Z	= network, tuned circuit

ABBREVIATIONS

A	= ampere(s)	ID	= inside diameter	qty	= quantity
ac	= alternating current	in.	= inch, inches		
AR	= as required	incand	= incandescent	rdh	= round head
assy	= assembly	incl	= include(s)	rect	= rectifier
		intl	= internal	ref	= reference
brkt	= bracket	I/O	= input/output	rf	= radio frequency
				rfi	= radio frequency interference
c	= centi(10^{-2})	k	= kilo (10^{3}), kilohm	rh	= right hand
C	= Celsius, centigrade	kg	= kilogram	rpm	= revolutions per minute
cer	= ceramic			rwv	= reverse working voltage
cm	= centimetre	lb	= pound		
comp	= composition	LED	= light-emitting diode	sb	= slow blow
conn	= connector	lh	= left hand	SCR	= semiconductor-controlled rectifier
		M	= mega (10^{6}), megohm		
d	= deci(10^{-1})	m	= milli (10^{-3})	scw	= square cone washer
dc	= direct current	mach	= machine	Se	= selenium
deg	= degree(s)	mb	= medium blow	Si	= silicon
dia	= diameter	met oxd	= metal oxide	slftpg	= self-tapping
dpdt	= double-pole, double-throw	mfr	= manufacturer	spdt	= single-pole, double throw
dpst	= double-pole, single-throw	misc	= miscellaneous	spst	= single-pole, single throw
		mm	= millimetre	sst	= stainless steel
elctlt	= electrolytic	mtg	= mounting	stl	= steel
encap	= encapsulated	My	= Mylar	sw	= switch
ext	= external				
		n	= nano (10^{-9})	T	= TORX® screw
F	= Fahrenheit, farad	n.c.	= normally closed	Ta	= tantalum
fb	= fast blow	no.	= number	tgl	= toggle
fh	= flat head	n.o.	= normally open	thd	= thread
fig.	= figure	NSR	= not separately replaceable	Ti	= titanium
filh	= fillister head	ntd	= no time delay	tol	= tolerance
flm	= film				
fw	= full wave	OBD	= order by description	U (μ)	= micro (10^{-6})
fxd	= fixed	OD	= outside diameter		
		ovh	= oval head	V	= volt(s)
G	= giga(10^{9})	oxd	= oxide	var	= variable
Ge	= germanium			Vdcw	= direct current working volts
		p	= pico (10^{-12})		
H	= henry, henries	PCA	= printed-circuit assembly		
hd	= head	phh	= phillips head	W	= watt(s)
hex	= hexagon, hexagonal	pnh	= pan head	w/	= with
hlcl	= helical	P/O	= part of	WIV	= inverse working volts
Hz	= Hertz	pot	= potentiometer	ww	= wire-wound
		pozi	= Pozidriv		

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Table 7-8. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their supplements.

CODE NO.	MANUFACTURER	ADDRESS
00685	Honeywell, Inc., Microswitch Div.	Marlboro, MA
03614	McGraw Edison, Bussman Mfg. Div.	St. Louis, MO
05216	Phoenix Transformer Co.	Phoenix, AZ
06004	Stewart-Warner Corp., Bassick Div.	Bridgeport, CT
11897	Plastiglide Mfg. Corp.	Hawthorne, CA
13150	Vernitron Electronic Component	Laconic, NH
14280	Square-D Co.	Lexington, KY
16428	Belden Corp., Electronic Div.	Richmond, IN
21790	Regdon Corp.	Brookfield, IL
28480	Hewlett-Packard Co.	Palo Alto, CA
31846	Baumback Engineering Co.	Mt. View, CA
56699	Mepco Electra Corp, Inc.	Columbia, SC
58904	Mercotac, Inc.	San Diego, CA
60016	Littelfuse, Inc.	Des Plaines, IL
74159	Teledyne, Inc.	Edinboro, PA
75382	Kulka Electronic Corp.	Mt. Vernon, NY
78553	Eaton Corp., Engineered Fasteners Div.	Cleveland, OH
83014	Hartwell Corp.	Placentia, CA
94959	3-M Co.	St. Paul, MN

APPENDIX A
SERVICE NOTES

CONTENTS

7933-01

SERVICE NOTE

Supersedes: None

Affected Units:
7933H 2204AXXXXX and below

INCOMPATTIBLITY OF LINEAR MOTOR WITH COIL ASSEMBLY ON UNITS WITH SERIAL PREFIX 2204 OR LOWER.

APPLIES TO:	All Units X	Only Units on Agreement ☐
PERFORM:	Immediately ☐	At PM/Normal Call X*
	On Failure ☐	Information Only ☐

WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:	1 hr		
PARTS:			X
TRAVEL:		X*	

SERVICE INVENTORY	Return for update ☐	Use as is ☐
	Return for salvage ☐	See text X

WARRANTY EXTENDED UNTIL: April '83

SYMPTOM: Failure of the coil assembly on units with a serial# prefix equal to 2204 or lower.

CAUSE: The spacing of the linear motor permanent magnets with respect to the coil assembly ribbon cable is such that there may be an interference fit when the coil is replaced with a new coil assembly (see figure on following page).

SOLUTION: Since the linear motor is not a field replaceable item it will be necessary to return defective units to the factory for refurbishment. During the time that the unit is being refurbished, DMD will supply any loaners that are necessary to minimize customer downtime. Before any replacements can occur, however, the factory MUST have a forecast of how many units are actually going to be reworked. This will require an inspection be made on the linear motor to verify spacing between the coil and linear motor (see figure on the next page). Once the inspection has been made and a unit has been verified to have the above problem, DMD Service Engineering should be contacted as soon as possible so that arrangements can be made for a loaner.

It is important to note that in the event of a premature failure of the coil assembly, replacing the coil may provide a temporary fix but that the original problem of incompattablity will still exist.

*note: It is imperative that all units be inspected by no later than three months from the date of installation. However it is recommended that an attempt is made to coordinate all inspections with a normal service call to minimize travel. After the three month mark, this service note moves to "perform immediately" status and DMD will pay travel accordingly.

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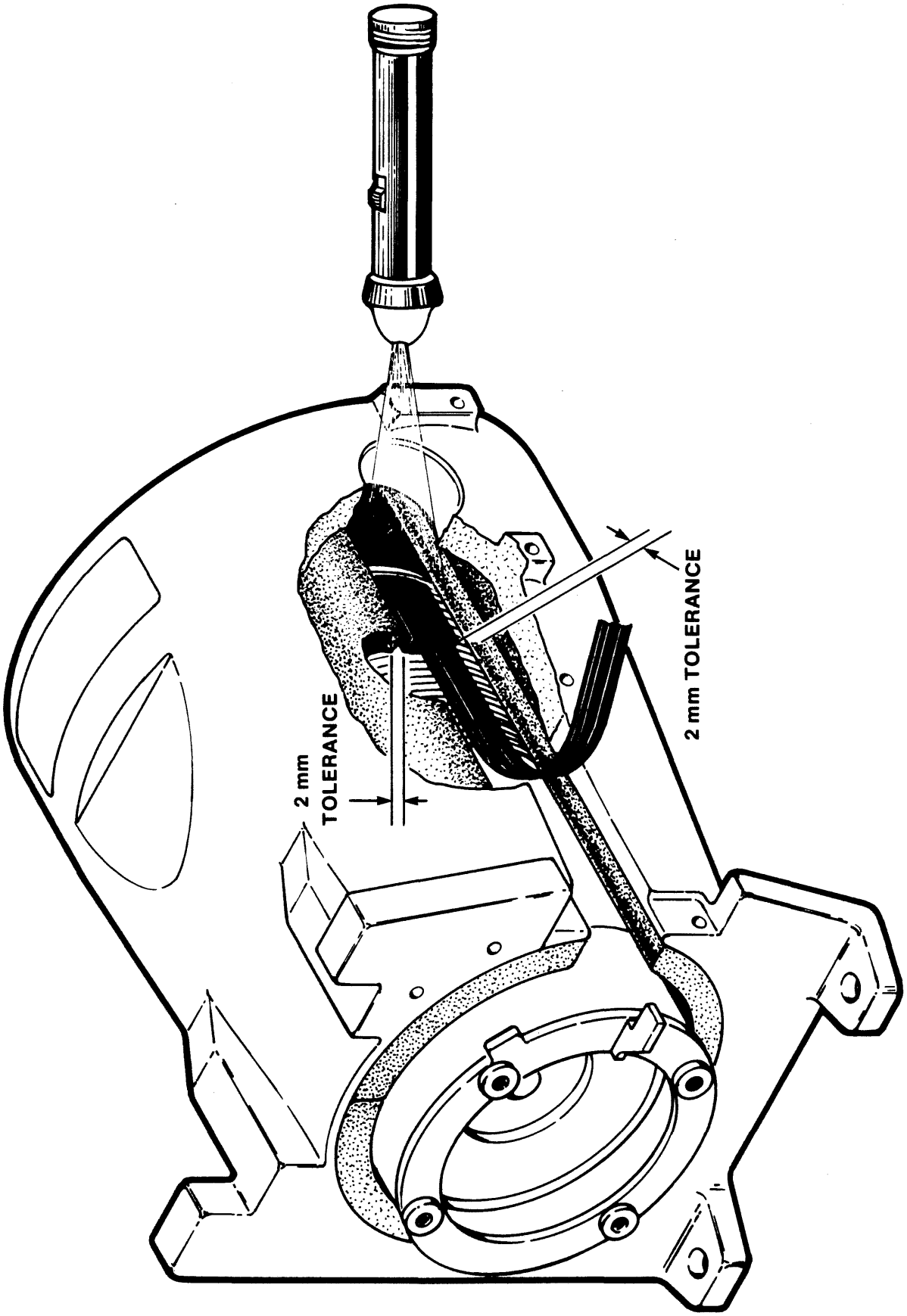

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7933H-02

SERVICE NOTE

Supersedes: None

APPLIES TO:	All Units X	Only Units on Agreement ☐
PERFORM:	Immediately ☐	At PM/Normal Call ☐
	On Failure ☐	Information Only X

WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:			X
TRAVEL:			X

SERVICE	Return for update ☐	Use as is X
INVENTORY	Return for salvage ☐	See text ☐

WARRANTY EXTENDED UNTIL:

PRODUCTS AFFECTED: 7933H
ALL SERIAL NUMBERS

INTERNAL DIAGNOSTIC

SYMPTOM: The 7933 internal diagnostic does not always correctly report the number of the defective part.

CAUSE: All of the PCA's in the 7933 are inter-related, and a failure cannot be located on a certain assembly with 100% accuracy. The diagnostic reports the part number of the first part which did not properly respond in its sequence of testing. The microprocessor PCA is often reported because it controls so many functions of the drive. Before any service call is considered complete, the suspect PCA should be replaced in the disc drive to verify it's failure.

It has been discovered that PCA's can be vibrated loose in shipping. A modification will be made to the card cage cover, but until it is completed we suggest that at installation all PCA's in the card cage be reseated. This should also be done if there are intermittant problems.

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7933H-03

SERVICE NOTE

Supersedes: None

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☐		Information Only ☒
WARRANTY:	**EXTENDED**	**NORMAL**	**NONE**
LABOR:			X
PARTS:			X
TRAVEL:			X
SERVICE INVENTORY	Return for update ☐		Use as is ☒
	Return for salvage ☐		See text ☐
WARRANTY EXTENDED UNTIL:			

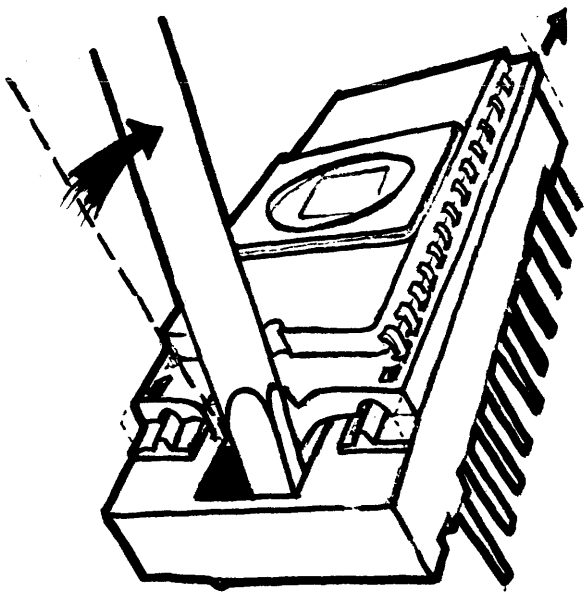
APPLIES TO ALL UNITS
7933H

REMOVING ROMS

SYMPTOM: Roms cannot be removed from the sockets of the 07930-69002 PCA.

CAUSE: Special zero extraction force sockets are used on this PCA.

SOLUTION: Insert a small screwdriver in the socket slot at the top of the IC socket and depress the catch. Slowly slide the top of the socket the full extent of its travel. The chip is now released for easy removal.



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7933-04

SERVICE NOTE

Supersedes:

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☒		Information Only ☐
WARRANTY:	**EXTENDED**	**NORMAL**	**NONE**
LABOR:	.25		
PARTS:			X
TRAVEL:			X
SERVICE INVENTORY	Return for update ☐		Use as is ☐
	Return for salvage ☐		See text ☒
WARRANTY EXTENDED UNTIL:			

7933H R/W PCA FSI UPDATE

07930-69006 Exchange
07930-60006 New

Series 2146 and below

SYMPTOM: If a new R/W or Formatter Separator PCA is installed the disc drive may occasionally fail the power-on self test, usually with TERR 209.

CAUSE: A pull-up resistor was left with one lead unconnected.

SOLUTION: A #30 wire jumper should be added to the trace side of the R/W PCA from U891 pin 2 to U851 pin 12. This jumper should be added to all 07930-69006 PCA's with series 2146 and below in field service inventory. This update will not require return of the PCA's to CSD. The problem has only been noticed when replacement R/W PCA's or Formatter Separators were installed. After jumper wire is added update series number to 2147.

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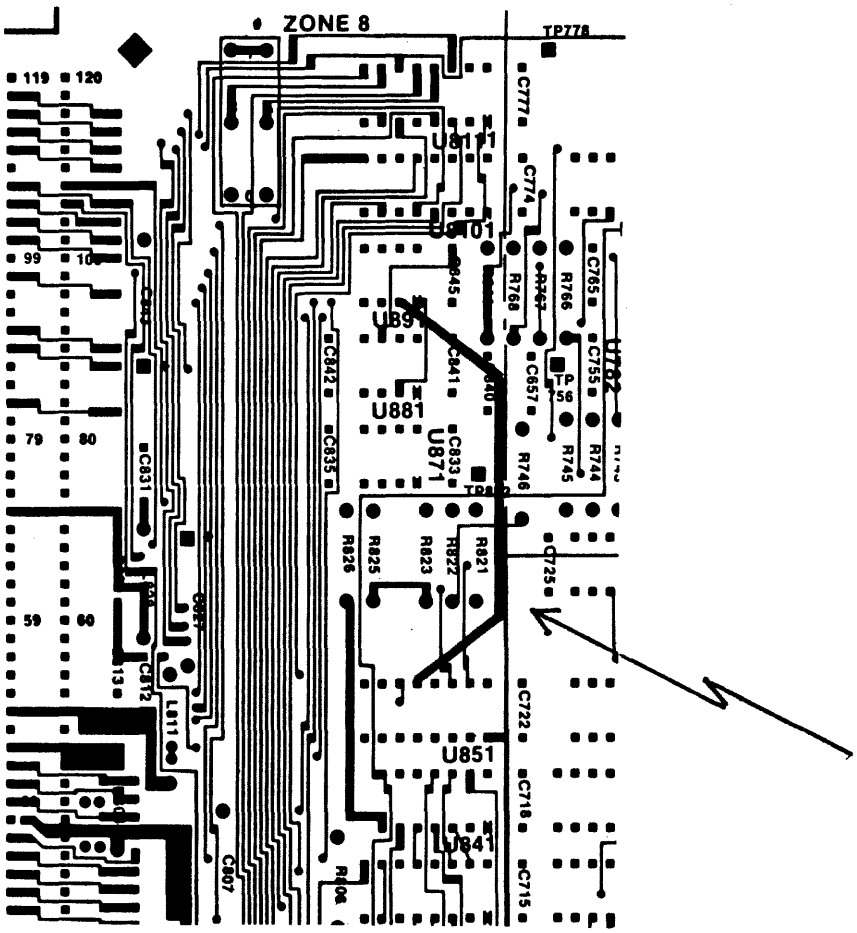

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7933H-05

SERVICE NOTE

Supersedes:

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☒		Information Only ☐
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:	.5hr		
PARTS:	yes		
TRAVEL:	no		
SERVICE INVENTORY	Return for update ☒		Use as is ☐
	Return for salvage ☐		See text ☐
WARRANTY EXTENDED UNTIL:	31 Sept. 1983		

7933H DISC DRIVE

ALL UNITS WITH SERIAL NUMBER PREFIX 2217A AND BELOW

FIRMWARE UPDATE

SYMPTOM: Mandatory upadate on the next failure of the 7933H with serial number prefix 2217A and below.

CAUSE: This firmware revision adds changes that will improve the power-on sequence of the 7933H. These changes will allow for a decrease in the number of steps necessary for media module installation. Specifically, the deleted steps include the 5-minute "PURGE" and the Incremental Seek section of the Data Surface Verification test (see pages 2-14 and 2-18 in the Installation manual/ 07930-90902). In addition, there are several changes that allow for compatability with all revisions of PCA's that may be seen in a 7933H.

SOLUTION: On the next 7933H related failure perform the firmware update by replacing the existing EPROM's with the 7 EPROM's in the new exchange EPROM kit. The part number for the new EPROM kit is 07930-19006. Following is a matrix that matches the part number of the individual EPROM's in the 07930-19006 with their corresponding "U" number on the MICROPROCESSOR PCA (p/n 07930-69002). Note that you cannot order these part numbers individually from CPC and that the full kit must be ordered (07930-19006).

07930-82061	U192
82062	U182
82063	U162
82064	U152
82065	U142
82066	U122
82067	U112

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The 07930-19006 will be supplied through CPC (DIV. 15) Blue Stripe exchange program. Defective EPROM kits should be returned to Division 15(CPC) and not to Division 50 (CSD).

All FSI must be updated as soon as possible because old firmware in the service kits will not work in new 7933H's (serial prefix 2216 and above).

DMD will accept extended warranty (02G) as follows:

Parts-	07930-19006 EPROM exchange kit
Labor-	.5 hours
Travel-	no travel will be accepted

****
* NOTE: When completing the Customer Support Order (CSO) form *
* the service code block should be filled in with: "0005" *
* This code will allow DMD to monitor the implementation *
* of this service note and prevent rejection of warranty *
* billing. *
****

7933H-06

SERVICE NOTE

Supersedes:

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☐		Information Only ☒
WARRANTY:	**EXTENDED**	**NORMAL**	**NONE**
LABOR:			
PARTS:			
TRAVEL:			
SERVICE	Return for update ☐		Use as is ☐
INVENTORY	Return for salvage ☐		See text ☐
WARRANTY EXTENDED UNTIL:			

7933H DISC DRIVE

UNITS WITH SERIAL PREFIX
2216A OR GREATER

CHANGES TO POWER ON SEQUENCE
INTRODUCED BY NEW FIRMWARE(MR2)

SYMPTOM: 7933H's with serial prefix 2216A or greater have a much different power-on sequence than earlier drives.

CAUSE: Several changes have been made to the Firmware in order to improve reliability of the the disc drive and to fix several "bugs" that have been discovered from manufacturing release until now. However, there are just a few changes that the field should be immediately aware of. Following is a brief explanation of these changes.

1. The Firmware will automatically execute a 'PURGE' command after the spindle motor has come completely up to speed. At this time the 'PURGE' message will appear on the front panel. The purge section lasts for 2.5 minutes.

2. After this, the heads will load at a slower speed than with the old Firmware. This decreases the severity of soft crashes when the heads move away from the cam tower (which is a source of contamination).

3. Next, the drive will execute single cylinder seeks accross each of the 1339 physical cylinders and wait approximately 3 revolutions at each cylinder. This will "Lift up" any particles that are on the disc surface and allow these particles to be purged out of the pack. During this 1.5 minute process 'PURGE' will remain displayed on the front panel.

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4. Finally, the familiar violent seeks and other motions will be heard while the front panel displays 'TESTING'. And then you will see 'DRIVE *' indicating that the drive is on-line.

The above procedure will be executed every time the power is turned from "OFF" to "ON" and the spindle is stopped. This requirement allows the drive to experience a power fail without a 4-minute delay if the power comes back up before the spindle stops spinning. This procedure will also be executed if the power is on and the top door is opened. In other words if there is the possibility of a Media Module being removed.

SOLUTION: The changes above will allow the CE to delete a few steps in the installation procedure. Namely, these steps are the five-minute purge and the incremental seek section as shown in the data surface verifiction procedure in the 7933 Installation Manual. It will still be necessary to run two passes of RO ERT and check for any UCOR's or repeatable COR's so that these areas can be spared out.

7933-07

SERVICE NOTE

Supersedes:

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☒		At PM/Normal Call ☐
	On Failure ☐		Information Only ☐
WARRANTY:	**EXTENDED**	**NORMAL**	**NONE**
LABOR:			X
PARTS:			X
TRAVEL:			X
SERVICE INVENTORY	Return for update ☒		Use as is ☐
	Return for salvage ☐		See text ☐
WARRANTY EXTENDED UNTIL:			

7933H DISC DRIVE

7933 SPINDLE DRIVER PCA
07930-69110 EXCHANGE
07930-60010 NEW

SYMPTOM: The Spindle Driver PCA, 07930-60010 ((07930-69010 exchange) has had a higher than expected early failure rate. This is a reliability improvement change and does not imply extended warranty.

CAUSE: Certain transistors on this assembly may be at the minimum specification.

SOLUTION: The Spindle Driver PCA circuitry has been changed to give slightly longer spin-up and spin-down times. This will substantially improve the problem of early failures. Since this problem only occurs during the early life of the drive, no action is required for drives in the installed base. However, we are requesting that all 07930-69010 assemblies in FSI be exchanged for 07930-69110 assemblies, with the improved circuitry. Note that the part number (07930-60010) of the new PCA will remain the same.

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7933-08C

PRODUCT SAFETY SERVICE NOTE

7933H Disc Drive
Serial numbers 2228Axxxxx
and below

APPLIES TO:	All Units X		Only Units on Agreement ☐
PERFORM:	Immediately X		At PM/Normal Call ☐
	On Failure ☐		Information Only ☐
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:	.7hrs.		
PARTS:			
TRAVEL:	X		
SERVICE INVENTORY	Return for update ☐		Use as is ☐
	Return for salvage ☐		See text X

WARRANTY EXTENDED UNTIL: Warranty alway.

Supersedes: All previous 7933-08

SAFETY GROUND INTERRUPT

WARNING

SYMPTOM: The main chassis of some 7933H disc drives may not have a solid ground connection because of improper termination of the earth ground to the main chassis.

CAUSE: This hazard is caused because the type of terminal used to connect the safety ground to the main chassis actually cuts the wire. A new ground terminal has been selected that will make a strong connection without any danger of severing the ground wire.

SOLUTION: Quantities of new ground terminals are being distributed to key people in each SRO according to the number of 7933's installed in that office. Each of these people will be responsible for seeing that these ground terminals are made available to the CE performing the repair. The person receiving the parts in each office will be an ALM if one exists for that office or a person that logically fills that position. In the case of ICON SRO's, distribution will be handled through ICON service headquarters. In the event that there are not enough parts to cover a particular SRO, the ground terminal will be available at CPC/PCE under part number 0362-0776. It is possible to tell if any disc drive has already been updated by the color of the terminal. The correct terminal is bronze colored while the improper terminal is copper. In addition, the CE should use the Maintenance Record sticker mounted on the absolute filter cover to indicate that this service note has been implemented on the drive.

The following is the procedure that must be followed in correcting the problem.

W A R N I N G
****

TO AVOID POSSIBLE ELECTRICAL SHOCK, DISCONNECT THE POWER CORD BEFORE COMPLYING WITH THE FOLLOWING INSTRUCTIONS.

MB/sg
PCO# 48-5227

12/82-48

HEWLETT hp PACKARD

For more information, call your local HP Sales Office or East (301) 948-6370 • Midwest (312) 255-9800 • South (404) 955-1500 • West (213) 877-1282. Or, write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94304. In Europe, Post Office Box CH-1217 Meyrin 2, Geneva, Switzerland. In Japan, Yokogawa-Hewlett-Packard, 1-59-1, Yoyogi, Shibuya-Ku, Tokyo, 151.

9320-3500 (5/77)

Printed in U.S.A.

1) Follow steps 6-31a through 6-31c in the 7933 service manual to expose the Input Power Assembly.

2) Locate the two (2) ground terminals (see figure below) and remove the Green/Yellow ground wire from each of the terminals.

3) Replace these two ground terminals with the new terminals (p/n 0362-0776). Assure that the new terminals are adequately tightened.

4) Cut the exposed wire on the two Green/Yellow wires and strip the insulation to expose new and undamaged wire.

5) Insert the two green/yellow wires back into their original positions and tighten the screws on the new terminals. Note that the power cord bushing may need to be loosened in order to provide enough slack for connection to the ground terminal. There should be no strain on either of the two wires. Retighten the power cord bushing so that strain relief on the power cord is reinstated.

6) Reinstall the Input Power Assembly and Power on Disc. No additional testing is required.

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*   NOTE:   When completing the Customer Support Order (CSO) form the       *
*           service code block must be filled in with "20002". Failure      *
*           to use the service code will result in rejection of the         *
*           warranty billing.                                               *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
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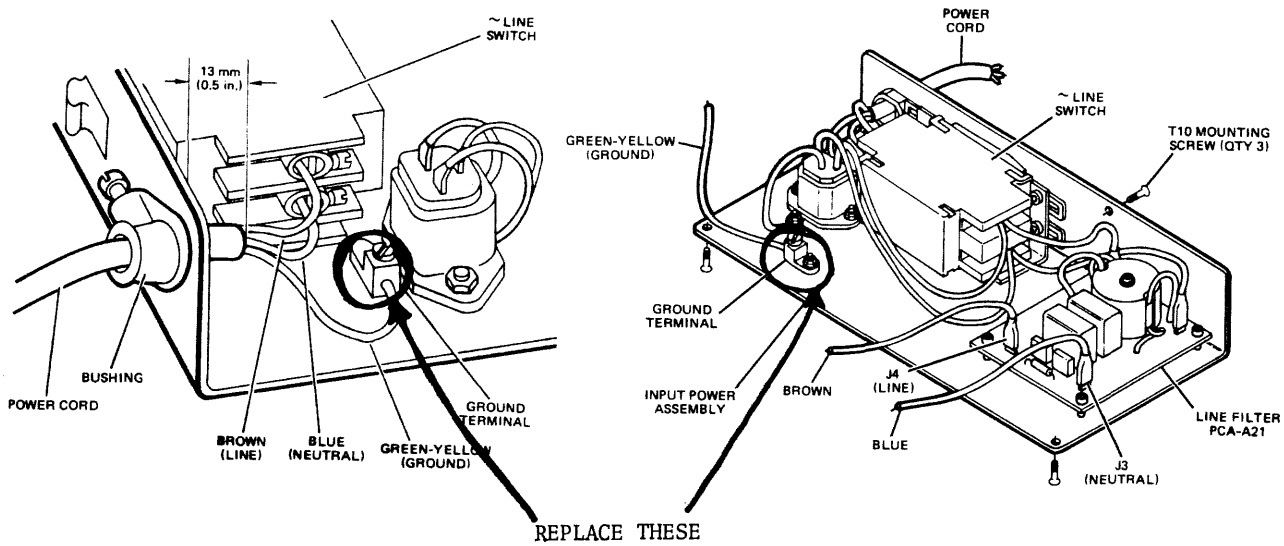

7933H-09

S E R V I C E N O T E

Supersedes: None

APPLIES TO:	All Units ☒	Only Units on Agreement ☐
PERFORM:	Immediately ☐	At PM/Normal Call ☒
	On Failure ☐	Information Only ☐

WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:	X		
TRAVEL:			X

SERVICE INVENTORY	Return for update ☒	Use as is ☐
	Return for salvage ☐	See text ☐

WARRANTY EXTENDED UNTIL: January 1984

7933H 400Mb Disc Drive
Serial Number Prefix less
than 2304Axxxxx

Mandatory Update to MR4
Firmware (p/n 07930-19008)

SYMPTOM: Starting with Serial Number 2304Axxxxx, all 7933H's will contain MR4 firmware. This will be coincident with the Manufacturing release of the 7935H. All 7933H's that were produced prior to the 2304A prefix (May 1983) should be updated to MR4.

CAUSE: MR4 introduces some significant improvements for the 7933 in the areas of performance,reliability and general drive operation. The MR4 firmware is totally backwards compatable and is used in common with the 7935. One of the most noticable features of MR4 is the increased performance which makes the 7933/35 comparable to and in some cases(depending on the system configuration), faster than the 7925. This added performance is achieved by many changes in code structure and more efficient hardware utilization. There are many other changes in the firmware that are not related to performance but are nevertheless significant. The following list addresses some of these changes.

- Front panel message is changed to "AIRPURGE" instead of "PURGE". This keeps customers from misinterpreting and assuming that a data purge is occuring.
- Prevents error information stored in RAM from being cleared by the CPU so it can be later logged permanently on the maintenance tracks.
- Automatically rewrites the spare sector during the read recovery algorithm. This makes the the 7933 nearly immune to a potentially disasterous condition defined as "sector 91" errors.

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9320-4766 (1/83)

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- Improves the velocity transducer/actuator current diagnostic for more reliable diagnosis as well as eliminating any problems caused by "sticky crash stops".
- Eliminates the possibility of not completely finishing a sector transfer if writing when a power fail occurs and resulting in an unrecoverable error on that sector.
- Seeks off of the alignment bands immediately after performing an automatic head alignment. This drastically reduces the probability of destroying the head alignment band in the event of an electronics failure or ESD influence and thereby keeps the media module from being destroyed
- Eliminates the possibility of microprocessor hangs as the result of a recently identified problem associated with the PHI chip. This is expected to reduce some of the common channel timing problems(i.e. channel hardware timeouts) and possibly some system hangs.
- A potential source of erronious DERR 114 has been found and eliminated.

SOLUTION: At next PM or normal call, replace the existing firmware with the MR4 firmware (p/n 07930-19008).
The following is a list of the part numbers of the individual ROMs in the 07930-19008 package versus their "U" number assignment on the Microprocessor PCA. The individual ROMs are not orderable.

07930-82081	U192
82082	U182
82083	U162
82084	U152
82085	U142
82086	U122
82087	U112

The 07930-19008 will be supplied through CPC(div 15) Blue Stripe exchange program. All FSI is to be updated to MR4 as soon as possible.

DMD will accept extended warranty (02G) as follows:

Parts-	07930-19008 EPROM exchange kit
Labor-	No labor will be accepted
Travel-	No travel will be accepted

7933-10

SERVICE NOTE

Supersedes: None

APPLIES TO:	All Units ☐	Only Units on Agreement ☒
PERFORM:	Immediately ☐	At PM/Normal Call ☒
	On Failure ☐	Information Only ☐

WARRANTY:	**EXTENDED**	**NORMAL**	**NONE**
LABOR:	.5 hr		
PARTS:	X		
TRAVEL:			X

SERVICE INVENTORY	Return for update ☐	Use as is ☐
	Return for salvage ☐	See text ☒

WARRANTY EXTENDED UNTIL: June 1984

7933H 400Mb DISC DRIVE
Serial Numbers 2233Axxxxx
and below

Spindle Ground Retrofit
Kit (p/n 07930-60223)

SYMPTOM: Due to a faulty design of the 7933 spindle grounding system, a high failure rate of spindle assemblies has been experienced. Common problems associated with premature failure of this ground are as follows. (This list is not exhaustive)
- High error rate caused by improper ground.
- Excessive run-out indicated by DERR 70 or high error rate due to this excessive run-out (run-out table has a value of above 40). Remember that a "dirty" media/spindle hub causes the same problem.
- Noisy spindle assembly.
- Spin down/Spin up (also caused by numerous other problems.)

CAUSE: The old ground system incorporates a mercury bathed "slip ring" that mechanically fixes the spindle shaft to the bottom cover. This rigid configfuraton allows very little freedom for spindle shaft run-out. Consequently, the two points where the slip ring is fastened to the shaft and bottom cover are subject to excessive stress from the run-out of the shaft. This stress results in the breakdown of the ground contact and ultimately in the total severing of the ground path. In addition the broken parts can easily "fly" into the spindle windings and hall sensors and cause considerable damage to these areas (including the Spindle Driver and Regulator PCA's).

SOLUTION: The ground assembly has been redesigned and consists of a conventional ground button (07930-60221) and a mating bottom cover (07930-60222). Both the bottom cover and the button have been included in a kit, P/N 07930-60223, for ordering convenience.

To remove the old grounding components and replace with the spindle ground kit(07930-60223), proceed as follows:

1. Do a backup. The Media will be taken out.

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HEWLETT PACKARD

2. Remove the three T15 screws and remove the bottom cover.

3. Using needle nose pliars, pull straight down on the mercury slip-ring to expose the retainer screwed into the spindle shaft.

4. Place a 3/8-inch nut driver on the retainer. Start rotating the nut driver in a clockwise direction. This will cause the discs to rotate. With the mass of the discs moving, quickly reverse the rotation (go counterclockwise) to loosen the retainer and remove it from the shaft.

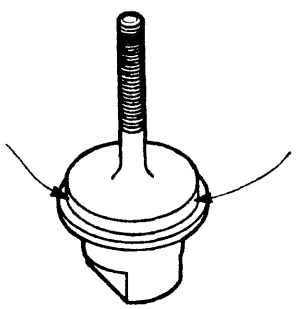
5. Remove the media module.

6. Place one drop of sealant (p/n 0470-0573) on opposite mating surfaces (see figure below). Do not put any sealant on the ground button threads.

7. Without touching the top, outermost machined surface of the spindle hub, hold the spindle nose tightly with one hand. With the other hand, hand tighten the ground button into the shaft. Then, while continuing to hold the spindle nose, tighten the ground button with an adjustable wrench until the spindle nose cannot be prevented from turning in your hand.

8. Install the new bottom cover. Be certain to reinstall the braided ground strap with one of the three T15 screws.

9. Clean the spindle motor and media module chamber very thoroughly using magnetic tape head cleaner (p/n 8500-1251) and reinstall the Media Module.



application of sealant

****
* Note: When completeing the Customer Support Order(CSO) form,the service *
*   code block must be filed in with "20006". Failure to use the   *
*   service code will result in rejection of the warranty billing.   *
****

7933-11

SERVICE NOTE

Supersedes:

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☐		Information Only ☒
WARRANTY:	**EXTENDED**	**NORMAL**	**NONE**
LABOR:			X
PARTS:			X
TRAVEL:			X
SERVICE	Return for update ☐		Use as is ☐
INVENTORY	Return for salvage ☐		See text ☒
WARRANTY EXTENDED UNTIL:			

7933H 400 Mb Disc Drive
Serial Numbers 2233Axxxxx
and below

Addendum to Service Note
#7933-10, Spindle Ground
Retrofit

SYMPTOM: Some of the new bottom covers (07930-60222) don't fit on the spinlde motor due to interference with the stator windings.

CAUSE: There are 3 standoffs that hold the ground spring approximately 1/4 inch from the bottom cover. This allows for an interference fit with the plastic part that the stator winding is wound on (see fig.).

SOLUTION: If the bottom cover does not fit flush on the spindle when the 3 screw holes are properly lined up with the stator housing, it will be necessary to perform the following procedure: (NOTE: There is always only one position out of three possible orientations that will allow the bottom cover to fit flush, so be sure and check all three positions before proceeding). See figure on following page for parts identification.

1. Remove Media Module and Spindle motor.
2. Place Spindle assembly on a Table and lay on its side. DO NOT rest spinle upside down on the hub.
3. Loosen set screw in the middle of the stator housing wall (this is the piece with a ribbed surface) using a T-8 TORX driver.
4. Loosen the cable clamp at the exit notch for the spindle cable.
5. Using the spindle cable for leverage, gently work the stator until it is turning freely in the stator housing. Then rotate the stator counterclockwise as far as possible while still allowing the spindle cable to exit through the notch in the spindle housing.
6. Be sure that stress is taken off of the Stator and encoder wires by pushing the spindle cable inward, making sure that the insulating sheath is also as far inward as possible. Reposition the cable clamp in the notch.
7. When the bottom cover easily fits on the spindle, retighten the set screw to 6 in-lbs, making sure the stator is as deep as possible into the Spindle Assembly.
8. Reinstall Spindle Motor and Media Module.

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9320-4766 (1/83)

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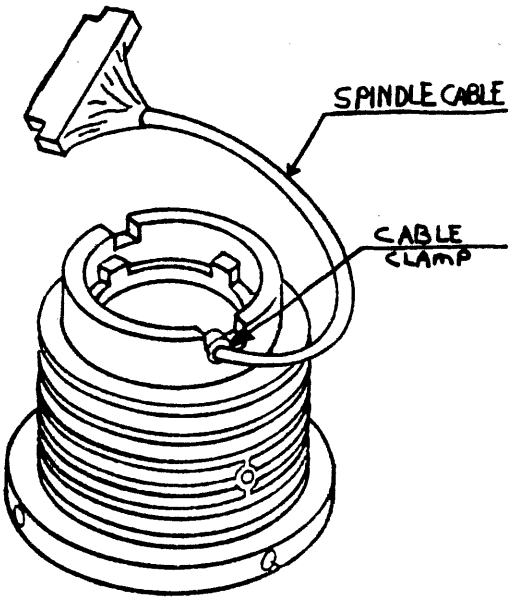
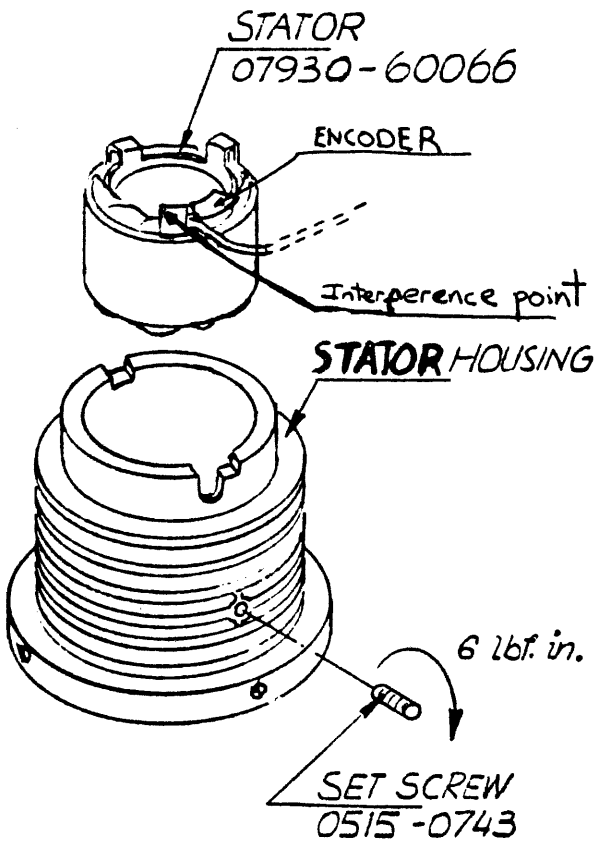

SPINDLE CABLE
CABLE CLAMP


STATOR
07930-60066
ENCODER
Interference point
STATOR HOUSING
6 lbf. in.
SET SCREW
0515-0743

7933H-12
7935H-12

SERVICE NOTE

Supersedes: None

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☐		Information Only ☒
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:			X
TRAVEL:			X
SERVICE INVENTORY	Return for update ☐		Use as is ☒
	Return for salvage ☐		See text ☐
WARRANTY EXTENDED UNTIL:	N/A		

Model Numbers: 7933H Disc Drive
7935H Disc Drive

Parts Affected: 07930-60002 (new)

07930-69002 (exchange)

TITLE: NEW MICROPROCESSOR PCA PART NUMBER

At some time in the future we are planning to introduce a dual port option for the 793X disc drive. The dual port option will require a slight modification to the Microprocessor PCA. In anticipation of this release, we are obsoleting the old Microprocessor, 07930-60002. The new Microprocessor part number is 07930-60302 (07930-69302, exchange).

All old versions will be updated to the new version when returned for repair. These parts are fully backward and forward compatible in single port drives. At this time no parts should be returned simply for updating.

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9320-4766 (1/83)

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7933-13S
7935-13S

PRODUCT SAFETY SERVICE NOTE

Supersedes: NONE

APPLIES TO:	All Units X	Only Units on Agreement ☐
PERFORM:	Immediately X / On Failure ☐	At PM/Normal Call ☐ / Information Only ☐

WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:	0.5 HR.		
PARTS:	YES		
TRAVEL:	YES		

SERVICE INVENTORY	Return for update ☐ / Return for salvage X	Use as is ☐ / See text ☐

WARRANTY EXTENDED UNTIL: ALWAYS

7933 DISC DRIVE

SERIAL NUMBERS
2337A09663 THROUGH 2342A11239

ACTUATOR DRIVER PCA
07930-60012 NEW
07930-69012 EXCHANGE
LOT NUMBER: 1227083

WARNING

HAZARD CATEGORY "A"
HAZARD CLASS "4"

SYMPTOM: THE ACTUATOR DRIVER ASSEMBLY MAY OVERHEAT, PERHAPS TO THE POINT OF COMBUSTION.

CAUSE: FIFTY ONE (51) PRINTED CIRCUIT BOARDS FROM LOT # 1227083 HAD ARTWORK MISREGISTRATION. THIS MAY RESULT IN CATASTROPHIC FAILURE OF THE BOARD.

SOLUTION: WE MUST RECALL THIS ENTIRE LOT OF PCA'S BECAUSE IT IS NOT POSSIBLE TO DETERMINE BY VISUAL INSPECTION WHICH PCA'S HAVE THIS PROBLEM. THE LOT NUMBER IS LOCATED ON THE SOLDER SIDE OF THE PCA, IN THE UPPER RIGHT HAND CORNER, NEAR THE EXTRACTION TAB. YOU SHOULD ONLY BE CONCERNED WITH THE BROWN COLORED LAMINATED FIBERGLASS PCA'S.

ALL DRIVES WITHIN THE SERIAL NUMBER RANGE GIVEN ABOVE SHOULD IMMEDIATELY BE CHECKED FOR THE POTENTIALLY HAZARDOUS ASSEMBLY. ALL ASSEMBLIES FOUND WITH LOT NUMBER 1227083 SHOULD BE REPLACED. DMD WILL ACCEPT WARRANTY BILLINGS FOR PARTS, LABOR, AND TRAVEL.

* *
* NOTE: WHEN COMPLETING THE CUSTOMER SUPPORT ORDER (CSO) FORM THE SERVICE CODE BLOCK MUST BE FILLED IN WITH "20015". USE OF THIS SERVICE CODE IS EXTREMELY IMPORTANT IN TRACKING THE EFFECTIVENESS OF THIS RECALL. *
* *

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9320-5190 (1/83)

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7933H-14
7935H-14

S E R V I C E N O T E

Supersedes:

Model Numbers: 7933H
7935H

Part Affected: 07930-10008

APPLIES TO:	All Units X		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☐		Information Only X
WARRANTY:	**EXTENDED**	**NORMAL**	**NONE**
LABOR:			X
PARTS:			X
TRAVEL:			X
SERVICE INVENTORY	Return for update X		Use as is ☐
	Return for salvage ☐		See text ☐
WARRANTY EXTENDED UNTIL:	N/A		

Disc Memory Division has developed and released new firmware for the 7933 and 7935 disc drives. All disc units shipped from DMD with a product serial number prefix of 2426Axxxxx or later has the new firmware installed. The new firmware is referred to as MR5 and, as with previous firmware, will be supplied through CPC/PCE.

Part number for the new firmware is 07930-10009.

CPC/PCE will be the supplying division for the new firmware.

The following is a list of the major changes incorporated in MR5:

* Simplifies data error diagnosis by not logging corrected data from ECC, while logging in the COR count only those errors which were correctly read after a single retry. The UNC log contains the address and error code byte of errors that required more than one retry during execution of the data recovery algorithm.

* Incorporates a new DERR (DERR 52) which occurs automatically if the soft (single retry) error rate approaches unsafe proportions. This error rate is calculated on a per head basis only. This will be a very good signal to the CE that corrective action should be taken immediately.

- continued -

MB/lr 6/84 - 48

9320-4766 (1/83)

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* Adds a new DERR (DERR 106) which occurs when a CRC error is detected during a WRITE operation. This will fail on such DMA failures as the 12-MHz crystal dropout during the WRITE, which will prevent the system from allowing data to be destroyed. The channel retry, which will follow as a result of this bad transfer status, will insure that the defective sector is rewritten error free.

* Eliminates LDEV NOT READY messages and SPIN DOWN/UP problems except when hardware forces a head unload (power fail, spindle speed down and door open).

* Eliminates known problems that can generate DERR's 1,4,14,15,16,17,29, 48,83,85,89 and 114's).

* Eliminates the possibility of an ECC uncorrectable error not being detected by the CRC. This has, in the past, possibly resulted in bad data being sent to the system with no error indication from the drive.

* Replaces the PHYSICAL FORMAT option with MNT TRK FORMAT. This allows only the maintenance tracks to be formatted in order to recover from a DERR 23 without destroying all of the factory generated spares.

NOTE: This service note does not authorize extended warranty for replacing firmware in pre-2426A serial prefix 7933/35's. Another service note will follow which authorizes this replacement in conjunction with several other items as part of a major update program. Warranty billings submitted prior to the issuing of this follow-on service note will be rejected.

7933H-15
7935H-15

S E R V I C E N O T E

Supersedes: None

7933H Disc Drive
7935H Disc Drive
ALL UNITS

793X RELIABLITY UPGRADE

APPLIES TO:	All Units ☒	Only Units on Agreement ☐
PERFORM:	Immediately ☒	At PM/Normal Call ☐
	On Failure ☐	Information Only ☐

WARRANTY:	**EXTENDED**	**NORMAL**	**NONE**
LABOR:	see "WARRANTY" section		
PARTS:	see "WARRANTY" section		
TRAVEL:	see "WARRANTY" section		

SERVICE	Return for update ☐	Use as is ☐
INVENTORY	Return for salvage ☐	See text ☒

WARRANTY EXTENDED UNTIL: August, 1985

SYMPTOM: Several changes have occurred on the 7933/35 that have made a significant impact on the reliability of these products. Six major contributors to this increased reliability have been selected as the elements in a manadatory field upgrade on all units in the field. However, not all units will require all six procedures to be performed since DMD has started shipping new units with these improvements as soon as their designs were finished and tested. The following is a list of the procedures to be performed and the S/N prefix ranges which are affected.

PROCEDURE	UNITS AFFECTED
- Update to MR5 firmware	2426A and below
- Clean and lubricate rails/bearings	2343A and below
- Install improved spindle ground assy.	2341A and below
- Disable filter pressure sensor	2335A and below
- Install Actuator Status connector clips	2328A and below
- Install improved Absolute Filter	All 50Hz units

CAUSE: Listed below are the major reasons for including the various procedures in this upgrade.

MR5 firmware

* Simplifies data error diagnosis by not logging corrected data from ECC, while logging in the COR count only those errors which were correctly read after a single retry. The UNC log contains the address and error code byte of errors that required more than one retry during execution of the data recovery algorithm.

* Incorporates a new DERR (DERR 52) which occurs automatically if the soft (single retry) error rate approaches unsafe proportions.

MB/sg 8/84

9320-4766 (1/83)

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This error rate is calculated on a per head basis only. This will be a very good signal to the CE that corrective action should be taken immediately.

* Adds a new DERR (DERR 106) which occurs when a CRC error is detected during a WRITE operation. This will fail on such DMA failures as the 12-MHz crystal dropout during the WRITE, which will prevent the system from allowing data to be destroyed. The channel retry, which will follow as a result of this bad transfer status, will insure that the defective sector is rewritten error free.

* Eliminates LDEV NOT READY messages and SPIN DOWN/UP problems except when hardware forces a head unload (power fail, spindle speed down and door open).

* Eliminates known problems that can generate DERR's 1,4,14,15,16,17,29, 48,83,85,89 and 114's).

* Replaces the PHYSICAL FORMAT option with MNT TRK FORMAT. This allows only the maintenance tracks to be formatted in order to recover from a DERR 23 without destroying all of the factory generated spares.

RAIL/BEARING LUBRICATION

* Significantly decreases wearing between the rails and carriage bearings which decreases the amount of "red dust" produced over time. This directly reduces servo related DERR's and the soft data error rate because actuator motion is not hindered by the red dust contamination. In addition, data loss as a result of red dust on the media is eliminated.

SPINDLE GROUND ASSEMBLY

* Provides a ground button/spring combination with wear life predicted at over five years. Bad spindle ground predominantly results in error rate degradation and seek errors.

DISABLE AIR PRESSURE SENSOR and INSTALL NEW ABSOLUTE FILTER

* The pressure sensor has been shown to be unreliable (even when at a proper adjustment level) which has resulted in many unnecessary "FILTER" messages. Since the sensor will be disabled, a new absolute filter (p/n 07930-80238) must be installed at the time of this update to assure a full year filter life in a normal operating environment.

ACTION: The following parts and tools are needed to perform a full update.

PARTS	
Update parts kit *	07930-67902
Absolute filter	07930-80238

* Update kit includes a ground button (07930-60232), ground spring (07930-00093), Pressure sensor (AMP) connector(p/n 07930-60241), 2 Servo connector clips (07930-40169) and MR5 Firmware (07930-19009).

TOOLS

Tape head cleaning solution	8500-1251
Alcohol, 91% isopropyl (filtered)	8500-0559
Q-tips	8520-0023
Cleaning sleeves (with handle)	9310-5074
Cleaning wipes	9310-4865
Bit, hex 3/32-inch 1/4-inch base	1535-2652
Torque wrench (2-12 inch-pounds)	1535-2653
Torque wrench (30-200 inch-pounds)	8710-1007
TORX Driver Kit (will use bits T9,T10,T15 and T30)	8710-1426
Ground Kit	9300-0794
Sealant	0470-0573
Head Spacer tool	07930-60154
Head Alignment tool	13354-20007
Update Tools Kit **	07930-67803

** The Update tools kit includes a Rail lubrication kit (6040-0652), and a 10 inch-pound preset torque wrench (8710-1594). This torque wrench is a new addition to the special tools required for servicing 7933/35's and is required for proper installation of the lower and upper rails. The torque specification for the rail clamp screws has changed from 5 to 10 inch-pounds.

Based on the serial number ranges indicated above, perform one or more of the previously mentioned procedures following these steps carefully. Refer to section VI in the 7933/35 service manual when performing procedures that require removal and replacement of parts.

DRIVE ACCESS:

1. Spin down the disc drive and remove media module.
2. Turn off power.
3. Attach ground strap to chasis ground and your wrist.
4. Remove: Front Cover, Prefilter, Media Chamber, Spindle Motor, Card Cage Cover, L & R Head Contamination shields and Absolute Filter Cover.

MR5 FIRMWARE (2426A and below)

Remove MPU PCA and replace existing firmware with MR5.

ACTUATOR STATUS CONNECTOR CLIPS (2328A and below)

Install two connector clips at each end of the Actuator Status interface cable (on the Servo and Actuator Status PCA's). There are a few drives that have metal clips already installed. These should be replaced with the new plastic clips. A brief procedure is included in the Update Parts Kit explaining how to properly install these clips.

CLEANING

1. Install head spacer tool.

2. Moisten a cleaning sleeve(s) with handle with alcohol for steps 3 and 4.

3. Clean all surfaces adjacent to the rails including casting surfaces, rail clamps, and cam towers.

4. Clean the full length of both upper and lower rails.

********** CAUTION **********

When cleaning the carriage assembly bearings, do not allow alcohol to flow on the sides of the bearings. Alcohol will dissolve the lubricant in the bearings and result in premature bearing failure.

5. Moisten a cotton swab with alcohol and clean the arch portion of all three bearings.

6. Inspect all servo and data heads and, with a new cleaning sleeve, clean any head that shows evidence of contamination.

RAIL LUBRICATION (2343A and below)

Note: A special lubricant (p/n 6040-0652) has been developed for the actuator linear bearing system to increase its useable life. The lubricant comes in an applicator which dispenses a precise volume. Correct operation of the disc drive requires that the exact volume of lubricant be used and this procedure be followed exactly.

1. Remove the shipping cap from the lubricant bottle and install the applicator needle cap and clean any excess lubricant from the neele and body.

********** CAUTION **********

It is imperative that the entire volume of the drop of oil reside in the arch of the bearing where it will be in direct contact with the rail.

2. Locate the carriage near track 200 as shown by the track indicator on the upper rail guide beam. Apply a single, full drop of lubricant to the center arch portion of the lower rear bearing.

3. Move the carriage to its outermost position against the crash stop (cylinder 1339).

4. Cover the heads with a cleaning wipe to protect from possible stray oil drops.

5. Apply a single, full drop of lubricant to each of the arch portions of the upper bearing and lower front bearings.

6. After removing the cleaning wipe covering the heads, manually move the carriage forward and back at least 10 times to distribute the lubricant on the rail surfaces.

NOTE: Any lubricant that was not applied directly to the bearing arches must be thoroughly cleaned off. This will require that steps 2-6 be repeated.

SPINDLE GROUND (2341A and below)

1. Replace ground button and ground spring. These must be replaced as a set. When replacing the ground spring, it is important that the procedure provided with the spring in the Update Parts Kit be followed exactly.

2. Install the Spindle Motor and Media Chamber.

********** CAUTION **********

Only use Magnetic Tape Head Cleaning Solution (p/n 8500-1251) when cleaning the media chamber and spindle hub. Using alcohol will cause the painted surface in the chamber to flake off.

3. Thoroughly clean the Media Chamber and Spindle hub using Tape Head Cleaning Solution.

4. Clean and install Left and Right Head Contamination Shields.

DISABLE AIR PRESSURE SENSOR (2335A and below)

1. Remove Door Latch Shield on Media Chamber.

2. Remove and discard existing pressure sensor cable assembly. Many drives have a ribbon cable which connects to the Module Detect PCA. This ribbon cable may be cut off at the PCA.

3. Install Sensor (AMP) Connector on the Front Panel PCA and re-install Door Latch Shield.

FILTER AND FILTER COVER

1. Remove existing Absolute Filter from the drive and vacuum all around Filter Well and surrounding area.

2. If the drive's power source is 50Hz, replace the old filter with a new Absolute Filter (p/n 07930-80238). If in a 60Hz environment, replace the filter with the new style filter only after all of the old style filters (07930-80053) have been used up.

TESTING

1. Replace all covers and power on Disc Drive.

2. Thoroughly clean and install Media Module and spin up the drive.

3. If carriage cleaning/lubrication procedure was not performed, skip steps 4-7.

4. Run 10 passes of Random RO ERT.

5. Enter the following program into the Front Panel.
   STEP 0=88 (LOOP), NUM=50, END=default
   STEP 1=68 (HD ALIGN), BAND=default, HEAD=0

6. Run the program and begin pressing the ROLL key (down arrow) about once every second. This will force the drive to perform 50 automatic head alignments (takes about 1.5 minutes).

7. DERR's 70 or 76 indicate that the carriage/rails must be replaced.

```
**************************** WARRANTY ************************************
*    When completing the Customer Support Order (CSO) form, use the     *
*    following CE checklist to avoid a rejection of the warranty        *
*    billing and ensure effective implementation of this update.        *
*                                                                       *
*    - Repair type 02G            - STREP = $250.00                     *
*    - Parts used 07930-67902     - Record ACTUAL labor hrs.            *
*    - Zone travel =00            - "20017" in the service code block.  *
*    - The words "793X update" should be in the comments field.         *
*                                                                       *
*    - Write your office number on the card in the firmware return      *
*      box. Enclose the old firmware in the shipping box and assure     *
*      immediate return.                                                *
*                                                                       *
*    - Update the CE log book on the customer site.                     *
*                                                                       *
*    - Note that the Absolute Filter (07930-80238) is not included      *
*      in the above list, and will not be accepted under warranty.      *
*                                                                       *
************************************************************************
```

7933-16A
7935-16A

SERVICE NOTE

Supersedes: 7933-16
7935-16

APPLIES TO:	All Units ☐		Only Units on Agreement ☒ X
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☒		Information Only ☐
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:	X		
TRAVEL:			X
SERVICE INVENTORY	Return for update ☐		Use as is ☐
	Return for salvage ☐		See text ☐
WARRANTY EXTENDED UNTIL: December 31, 1986			

7933H DISC DRIVE
SERIAL NUMBER PREFIX 2446 AND BELOW

7935H DISC DRIVE
SERIAL NUMBER PREFIX 2446 AND BELOW

PART AFFECTED: 07930-64253 UP HEAD
07930-64254 DOWN HEAD
07930-64255 SERVO HEAD

Repair Type: 02G
Repair Class: SN
Service Code: 20020

TITLE: NEW ASSEMBLIES

SYMPTOM: Due to premature failure of the head cable insulation, an excessive failure rate for the head assembly has been experienced in some disc drives. Head cables on the 793X disc drives have a PVC sleeve around the insulated wires. In some environments this sleeve cracks, placing additional strain on the insulation and the wire, resulting in a broken wire. Common symptoms associated with this failure are as follows:

- High data error rate, usually head specific.
- DERR 52 logged in the drive FAULT LOGS.
- Test errors (TERR's) that indicate PART 20 through PART 33 failed.
- UNRECOVERABLE data errors resulting in related system failures.
- Date corruption on the media requiring reformatting of maintenance tracks and/or a system reload.
- Erasure of an alignment band.
- Numerous other drive and system errors that would indicate a data error rate problem exists.

SOLUTION: The primary insulating material used on the three head wires and used as the sleeve around the three wires has been changed from a PVC plastic to a polyeurethane material, resulting in a significant increase in the reliability of the head lead cable. The new head assemblies can be identified by a yellow connector.

PD/sg 12/85-48

9320-4766 (1/83)

HEWLETT PACKARD

DMD recommends the following:

- On first failure replace the defective head.
- On second failure replace the remaining 13 heads.

WARRANTY: Warranty will be extended until 12/31/86 as follows:

TRAVEL: No
PARTS: Yes
LABOR: No

* *
*   *
* NOTE: When completing the Customer Support Order (CSO) the repair type must   *
*   be coded 02G and the repair class must be coded SN (Service Note).   *
*   The servic code block must be filled in with 20020A. For FIREMAN/HCETS*
*   users, the service code (20020A) must be entered in the PRINT field.   *
*   *
* *

7933H-17A
7935H-17A

SERVICE NOTE

Supersedes: 7933H-17, 7935H-17

APPLIES TO:	All Units X		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure X		Information Only ☐
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:	0.5		
PARTS:	X		
TRAVEL:	ON FAILURE ONLY		
SERVICE INVENTORY	Return for update ☐		Use as is ☐
	Return for salvage ☐		See text X
WARRANTY EXTENDED UNTIL:	31 December 1985		

7933H DISC DRIVE
SERIAL NUMBERS
2440A15720 THROUGH 2440A16100

7935H DISC DRIVE
SERIAL NUMBERS
2440A02400 THROUGH 2440A02450

TITLE: MISLOADED CAPACITOR ON SPINDLE DRIVER PCA
(07930-60010-NEW, AND 07930-69110-EXCHANGE)

SYMPTOM: Intermittent spin-down/spin up problems due to a failure on the Spindle Driver PCA. When reviewing the drive fault logs, DERR 230 and/or TERR 253 with the Hardware Fault Register indicating that spindle speed is down (HRF = %001) will most likely be logged. It is possible that servo related errors may also be logged (e.g., DERR 82, 83 and TERR 185, 186 and 187) with the HFR still indicating that spindle speed is down.

SOLUTION: Upon installation or on the next PM, inspect the Spindle Driver PCA for any drives that fail under the specified serial number range. There is a possibility that two polarized capacitors may have been installed reversed in a polarized application in the speed regulation circuitry. The two capacitors are small orange tantalum capacitors C165 and C357. C165 is located just to the right of the motherboard interconnect cable connector when the PCA is viewed from the rear of the drive with the power module cover removed. C357 is located just to the right of the large heat sink in the center of the PCA as viewed from the rear of the drive. Both capacitors must have the "+" (PLUS) lead inserted in the hole with the square pad. If one or both of the capacitors are installed incorrectly, replace the Spindle Driver PCA. Inspect all FSI and return defective parts to CSR for credit.

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9320-4766 (1/83)

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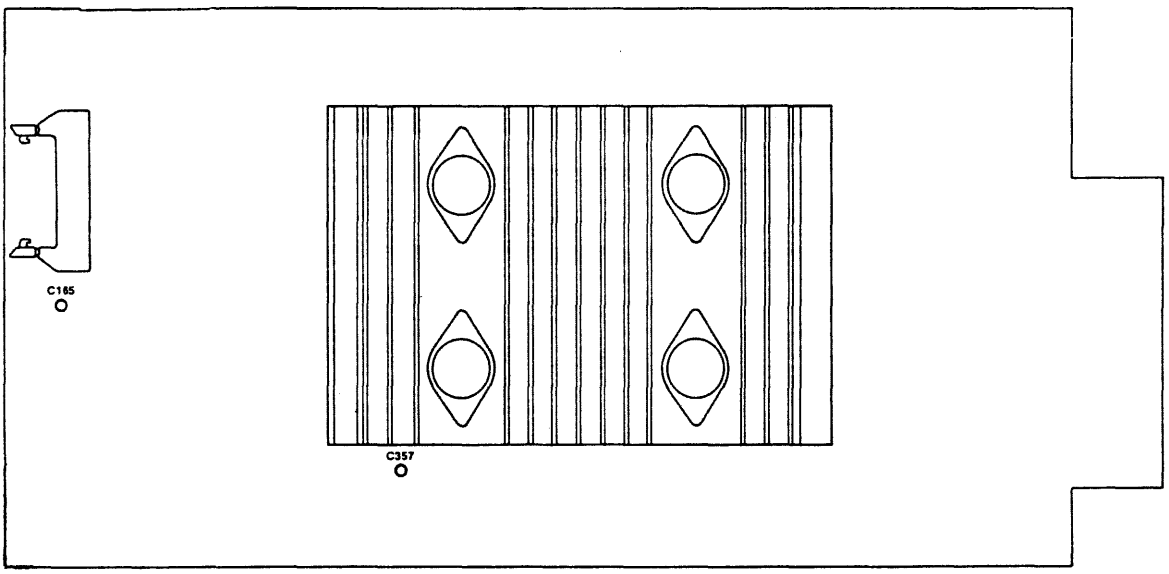
WARRANTY: Warranty will be extended until December 31, 1985 and DMD will pay for one 07930-69010 and 0.5 hours labor for each affected unit. Travel will be covered for failure only.

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*   NOTE:  When completing the Customer Support Order (CSO) Form, the       *
*          SERVICE CODE block must be filled in with "20021". This code     *
*          will allow DMD to monitor the implementation of this service     *
*          note and prevent rejection of warranty billing.                  *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
```



7933H-18
7935H-18

SERVICE NOTE

Supersedes: None

APPLIES TO:	All Units X	Only Units on Agreement ☐
PERFORM:	Immediately ☐	At PM/Normal Call X
	On Failure ☐	Information Only ☐

WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:	ON FAILURE		
TRAVEL:	ON FAILURE		

SERVICE INVENTORY	Return for update ☐ Return for salvage ☐	N/A	Use as is ☐ See text ☐

WARRANTY EXTENDED UNTIL: 1 July, 1986

7933H AND 7935H DISC DRIVES
SERIAL NUMBERS BELOW 2526Axxxxx

TITLE: POTENTIAL SAFETY HAZARD FROM SHORTING BLOWER WIRES

SYMPTOM: Arcing may occur between the blower motor housing and the yellow wires that are connected to the blower motor starting capacitor. This is a result of rubbing between the wires and the housing for a time sufficient to cause the insulation to be worn away.

The only reported symptoms to date have been DERR 52's (high uncorrectable error rate) on random heads and the noise that is generated from the arcing.

SOLUTION: All units should be inspected at next PM or normal service call for signs of wear. If the yellow wires are in contact with any part of the blower housing they should be tied back with a cable tie. If the insulation has worn through or if it is nearly worn through, the blower assembly should be replaced with a new blower assembly (p/n 07930-60249).

WARRANTY: Warranty will be extended until June 31,1986. DMD will pay for one blower assembly (07930-60249) and travel on failure only.

MB/sg 6/85-48

9320-4766 (1/83)

HEWLETT PACKARD

FOR MORE INFORMATION, CALL YOUR LOCAL HP SALES OR SERVICE OFFICE or East (201) 265-5000 ● Midwest (312) 255-9800 ● South (404) 955-1500 ● West (213) 970-7500 or (415) 968-9200 OR WRITE, Hewlett-Packard, 1820 Embarcadero, Palo Alto, California 94303. IN EUROPE, CALL YOUR LOCAL HP SALES or SERVICE OFFICE OR WRITE, Hewlett-Packard S.A., 7, rue du Bois-du-Lan, P.O. Box, CH-1217 Meyrin 2 - Geneva, Switzerland. IN JAPAN, Yokogawa-Hewlett-Packard Ltd., 1-27-15, Yabe Sagamihara City, Kanagawa Prefecture, Japan 229.

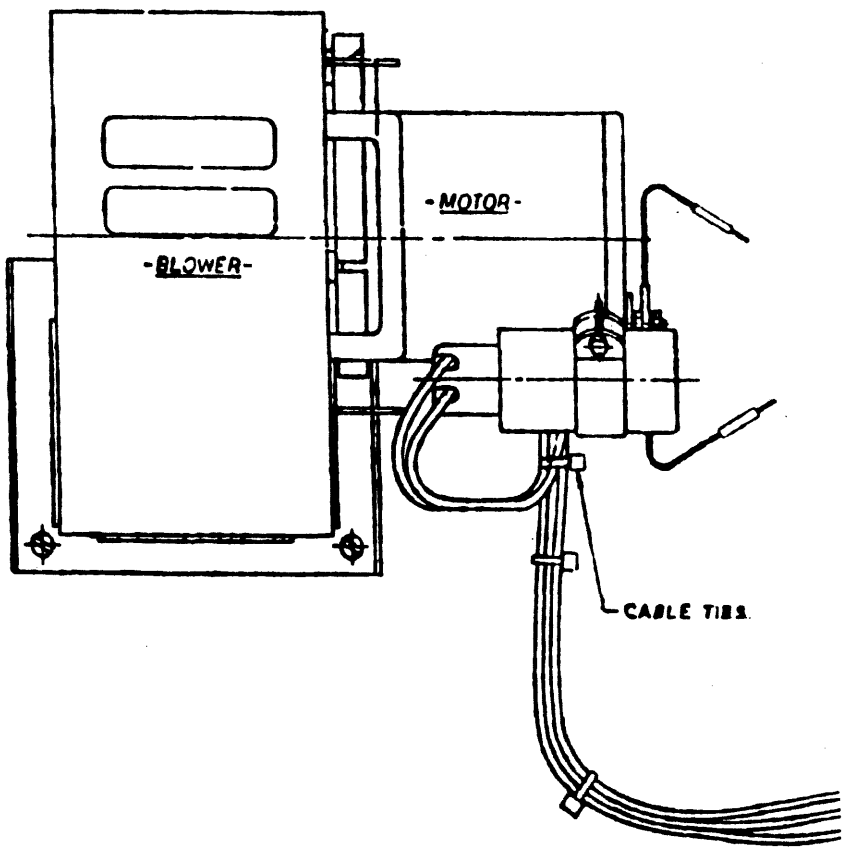
It is believed that the quantity of blowers that will actually require replacement is very low and that most of the installations that exhibit wearing will be fixed simply by tieing the yellow wires back, removing the potential for future wear. In order to verify this assumption, DMD IS REQUIRING THAT ALL BLOWER ASSEMBLIES REPLACED UNDER THIS SERVICE NOTE BE RETURNED TO:

HEWLETT-PACKARD
DISC MEMORY DIVISION
11413 CHINDEN BLVD.
BOISE, IDAHO 83714

ATTN: GENE WILLIAMS/3U

When sending in the defective blower assembly, a copy of the Repair Order must be included in the shipping package. Failure to comply with the above requirements will result in rejection of the extended warranty billing.

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
* NOTE: When completing the Customer Support Order (CSO) Form the SERVICE *
*       CODE block must be filled in with "20033". This code will allow  *
*       DMD to monitor the implementation of this service note and prevent*
*       rejection of warranty billing.                                    *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
```



7933H-19
7935H-19

S E R V I C E N O T E

Supersedes: None

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☒		Information Only ☐
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:	X		
TRAVEL:			X
SERVICE INVENTORY	Return for update ☐ / Return for salvage ☐	N/A	Use as is ☐ / See text ☐
WARRANTY EXTENDED UNTIL:	1 August, 1986		

7933H AND 7935H DISC DRIVES
SERIAL PREFIX 2523 AND BELOW

Part Numbers involved:

07930-19009
07930-67902

TITLE: MR5.1 FIRMWARE FOR 7933/35

SYMPTOM: There are two problems with MR5.0 firmware that are corrected by MR5.1.

The first is seen as a SPIN DWN message on the front panel of the disc drive during a START operation of an HP3000/6X system. The problem was found to be caused by an improper CLEAR sequence which attempted to clear a disc drive that was in the process of executing a CLEAR. In most cases, the system will issue another CLEAR and drive will spin back up and resume normal operation. In some cases the drive will remain in a SPIN DWN state and the START will fail with a BOOTSTRAP CHECKSUM ERROR. A patch to TMIT Delta I, TMIT, and V/E is available to correct the problem of 2 sequential CLEARS during the START(Patch index G039) but there is still the possibility of SPIN DWN on a running system if the drive is sent two sequential clears at any time. MR5.1 WILL NOT eliminate the SPIN DWN symptom in the event of multiple CLEARS but it will guarantee a successful SPIN UP and eventual resumption of normal operation.

The second problem fixed by MR5.1 is exhibited by symptoms resulting from the basic problem of undetected data corruption during a READ operation. The possible system level failures are numerous but some of the more commonly reported failures are:

- Disc space allocation becoming disabled on a drive.
- Part of a file is overlayed with data from the target sector + 1.
- Entries in file extent maps pointing to free space.
- File labels being marked as bad even though they are error free.

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9320-4766 (1/83)

HEWLETT PACKARD

It is not possible for the problem to occur on any 793X disc drive unless the system host enables RPS (rotational position sensing) on that drive. The only hosts that enable RPS on the 793X drives are 3000 systems with MPE V/E or T-MIT and HP9000 series 500 with HPUX. There is a patch available for T-MIT and V/E that automatically disables RPS on any drive that does NOT have MR4.0 or MR5.1 (or later) firmware installed.

SOLUTION: For the first problem, it is recommended that the MPE patch mentioned above be implemented as the complete solution to the SPIN DWN problem. Only the patch will eliminate the SPIN DWN message on the front panel which in most cases is the problem in the customer's eyes (i.e. BOOTSTRAP CHECKSUM ERROR occurs on only a small percentage of the SPIN DWN during START problems).

For the second problem, the MPE patch which disables RPS when the installed firmware revision is earlier than MR5.1 is likewise a viable solution in many cases. This is because RPS provides no performance advantage when there are less than 3 drives on a GIC and eliminating any unneccessary rework on hardware has obvious advantages. Therefore, all 3000 systems running V/E or T-MIT should install the RPS disable patch (patch index G052) but only those systems that suffer appreciable performance degredation when RPS is disabled should consider updating the firmware to MR5.1. There is NO advantage to nor reason for updating firmware in drives that are on systems running other than V/E or T-MIT.

Only 2 EPROMS have to be changed (ROMS 4 and 5) to upgrade MR5.0 to MR5.1, so a two-ROM kit has been set up that is orderable under p/n 07930-19119. All of the MR5.0 in FSI is stocked inside of the 793X Reliability Upgrade Kit (p/n 07930-67902). All of these kits should be paired with the 2-ROM kit when any future reliability upgrades are performed (see service note 7933H-15). For any new reliability upgrade kit orders, order p/n 07930-67903 (identical to 07930-67902 except contains MR5.1 instead of MR5.0). For updating drives that already contain MR5.0, order the 2-ROM kit.

DESCRIPTION	OLD P/N	NEW P/N
MR5.1 F/W SET	07930-19009	07930-19109
MR5.1 UPDATE(2-ROM)	N/A	07930-19119
RELIABITY UPGRADE	07930-67902	07930-67903
ROM4	07930-82094	07930-82194
ROM5	07930-82095	07930-82195

WARRANTY: Labor and Travel will not be covered under warranty for any MR5.1 updates. The cost of updating drives that currently have MR5.0 to MR5.1 ($ 14.00 for the 2-ROM kit) is all that is covered by this service note. Implementation of the reliability upgrade should continue to reference service note 793XH-15 using p/n 07930-67903 if all 07930-67902 stock is depleted.

****
* NOTE: When completing the Customer Support Order (CSO) Form the SERVICE *
*   CODE block must be filled in with "20034". This code will allow *
*   DMD to monitor the implementation of this service note and prevent*
*   rejection of warranty billing. *
****

7933H-20

7935H-20

SERVICE NOTE

Supersedes: NONE

APPLIES TO:	All Units X	Only Units On Agreement	
PERFORM:	Immediately On Failure	At PM/Normal Call X Information Only	
WARRANTY:	**EXTENDED**	**NORMAL**	**NONE**
LABOR:	none		
PARTS:	See text		
TRAVEL:	none		
SERVICE INVENTORY	Return for update Return for salvage	Use as is See text	
WARRANTY EXTENDED UNTIL:	01 Aug., 1986		

7933H AND 7935H DISC DRIVES
SERIAL PREFIX 2544 AND BELOW

TITLE: POTENTIAL SAFETY HAZARD
FROM STRAIN RELIEF

SYMPTOM: The screw on the plastic strain relief can be at line potential if the strain relief is improperly installed or broken.

PROBLEM: The strain relief can break, and if subjected to mechanical stresses, can pierce the insulation on the power cable.
A broken strain relif is usually not visible and must be detected using the following process.

SOLUTION: On your next scheduled site visit, measure the voltage potential between the screw on the plastic strain relief and one of the screws on the power module assembly cover.

```
**************************************************
*    CAUTION!!     Do not touch the screw on     *
*  the plastic strain relief until you have      *
*  verified that no AC potential exists!         *
**************************************************
```

If an AC voltage potential exists, replace the plastic strain relief with a new one, HP P/N 0400-0243. Also inspect and replace power cord if it is damaged. (HP P/N 8120-3364 standard)
The strain relief is NOT a reusable item and must be replaced if removed. The new strain relief is to be torqued to 12 in/lbs.

WARRANTY: Warranty will be extended until 01 Aug.,1986. DMD will pay for a strain relief and power cord on failure only.

```
*****************************************************************
* NOTE:    When completing the Customer Support Order (CSO)     *
* Form the SERVICE CODE block must be filled in with "200035".  *
* This code will allow DMD to monitor the implementation of     *
* this service note and prevent rejection of warranty billing.  *
*****************************************************************
```

GW/sg 7/85-48

9320-4766 (1/83)

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For more information, Call your local HP sales or service office or East 201-265-5000, Midw. 312-255-9800, South 404-955-1500, West 213-970-7500 or 415-968-9200, or Write:
Hewlett-Packard, 1820 Embarcadero, Palo Alto, Ca. 94303.

IN EUROPE, call your local HP sales or service office or write:
Hewlett-Packard S.A., 7 rue du Bois-du-Lan, P.O. Box, CH-1217 Meryin 2 - Geneva, Switzerland.
IN JAPAN, Yokogawa-Hewlett-Packard Ltd., 1-27-15, Yabe Sagamihara City, Kanagawa Prefecture, Japan 229.

7933H-21
7935H-21

SERVICE NOTE

Supersedes: None

APPLIES TO:	All Units X		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☐		Information Only X

WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:			X
TRAVEL:			X

SERVICE INVENTORY	Return for update ☐	Use as is ☐
	Return for salvage ☐	See text X

WARRANTY EXTENDED UNTIL: N/A

MODELS: 7933H
7935H

PART AFFECTED: 0403-0467 Leveler Pad

SERIAL NUMBERS: All drives serial prefix earlier than 2450

TITLE: NEW STYLE LEVELER FEET

SYMPTOM: Under heavy usage some disc drives have a tendancy to migrate or "walk" due to excessive vibration.

SOLUTION: New leveler pads have been found that eliminate walking 793X disc drives. The part number for these pads is 0403-0467 and they are currently used on all drives shipped since serial number prefix 2450. It is essential that the drive rests on all four pads with equal displacement relative to the casters. To accomplish this, lower each pad until it touches the floor and then using a wrench, lower it by one more full turn.

WARRANTY: None. This is a reliability enhancement.

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9320-4766 (1/83)

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7933H-23

7935H-23

SERVICE NOTE

Supersedes: None

MODELS: 7933H
7935H

SERIAL NUMBERS: All units with serial prefix 2607 or greater.

PARTS AFFECTED:

07930-69001	DMA PCA
07930-19109	MR 5.1 FIRMWARE

APPLIES TO:	All Units ☒	Only Units on Agreement ☐
PERFORM:	Immediately ☐	At PM/Normal Call ☐
	On Failure ☒	Information Only ☐

WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:			X
TRAVEL:			X

SERVICE	Return for update ☐	Use as is ☐
INVENTORY	Return for salvage ☐	See text ☒

WARRANTY EXTENDED UNTIL: N/A

TITLE: NEW DMA PCA AND FIRMWARE REVISION

PROBLEM: Part changes to the DMA PCA, P/N 07930-69001, have necessitated a new board part number and a new firmware revision.

SYMPTOMS: Parts changes have been made to the DMA PCA because the vendor for the ECC and the PHI is no longer able to supply these chips. The PHI chip, P/N 1AA6-6104, has been replaced by the Medusa chip, P/N 1TL1-0001. The ECC chip, P/N 1AG5-6001, has been replaced by an ECC chip with P/N 1TL3-0001.

Slight differences between the PHI and the Medusa have resulted in a firmware change from MR5.1 to MR5.3.

SOLUTION: The part number of the DMA PCA has been changed to 07930-69301. This new part number requires a firmware revision of MR5.3 or greater. An MR5.3 firmware kit, P/N 07930-19209, is available to upgrade from firmware revisions prior to MR5.3.

MR5.3 or greater firmware revision is required in a drive that has the 07930-69301 DMA PCA. MR5.3 or greater revision firmware is backward compatible with the 07930-6X001 DMA PCA.

WARRANTY: None. This is an information only service note.

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9320-4766 (1/83)

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7933H-24
7935H-24
7933XP-1
7935XP-1

S E R V I C E N O T E

Supersedes: None

MODELS: 7933H
7935H
7933XP
7935XP

APPLIES TO:	All Units ☒	Only Units on Agreement ☐
PERFORM:	Immediately ☐	At PM/Normal Call ☐
	On Failure ☐	Information Only ☒

WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:			X
TRAVEL:			X

SERVICE INVENTORY	Return for update ☐	Use as is ☐
	Return for salvage ☐	See text ☒

WARRANTY EXTENDED UNTIL: N/A

SERIAL NUMBERS: ALL UNITS

TITLE: NEW FIRMWARE REVISIONS
RELEASED FOR 7933/35
DISC DRIVES

PROBLEM: The introduction of the 7933/35XP disc drives with controller cache and the new DMA PCA (07930-60301) require two new firmware revisions for support. The combination of the new assemblies and firmware has created a compatibility problem between various assemblies and firmware revisions used in the 7933/35 disc drives, and the necessity to support two different revisions of firmware in the field.

SYMPTOM: The new DMA PCA (07930-60301) requires firmware revision MR5.3 or greater due to a compatibility problem that exists between the Medusa HPIB interface chip and MR5.1 or earlier firmware. This incompatibility problem causes a failure in the MPE software memory dump facility when installed as the system disc on HP3000 systems.

MR6.1 firmware is required for the 7933/35XP with controller cache, but due to the expanded microcode required for controller cache it is not compatible with the early version of the microprocessor PCA (07930-6X002). Both MR6.1 and MR5.3 are backward compatible with the old DMA PCA (07930-6X001). MR6.0 was originally intended to support the 7933/35XP drives with controller cache but a firmware design error was discovered as the drives were introduced, resulting with MR6.1. Some number of standard 7933/35H drives were shipped with MR6.0 and there is no problem with using MR6.0 in 7933/35H drives. Currently all 7933/35 "H" and "XP" drives are shipped with MR6.1.

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9320-4766 (1/83)

HEWLETT PACKARD

FOR MORE INFORMATION, CALL YOUR LOCAL HP SALES OR SERVICE OFFICE or East (201) 265-5000 • Midwest (312) 255-9800 • South (404) 955-1500 • West (213) 970-7500 or (415) 968-9200 OR WRITE, Hewlett-Packard, 1820 Embarcadero, Palo Alto, California 94303. IN EUROPE, CALL YOUR LOCAL HP SALES or SERVICE OFFICE OR WRITE, Hewlett-Packard S.A., 7, rue du Bois-du-Lan, P.O. Box, CH-1217 Meyrin 2 - Geneva, Switzerland. IN JAPAN, Yokogawa-Hewlett-Packard Ltd., 1-27-15, Yabe Sagamihara City, Kanagawa Prefecture, Japan 229.

7933/35H disc drives with dual port (option H22) will not be supported on MR6.0 or MR6.1 firmware. There is not enough space in the firmware for both dual port code and controller cache code. Dual port will be supported with MR5.3.

SOLUTION: The following firmware compatibility matrix summarizes the supported firmware configurations. The only firmware revisions required to support all 7933/35 disc drives are MR5.3 and MR6.1.

NOTE: There are no reliability or performance improvements between MR5.1, MR5.3, MR6.0 or MR6.1 on 7933/35H disc drives. This is not a mandatory update service note. Do not update firmware unless it is required due to a related parts replacement.

7933/35 FIRMWARE COMPATIBILITY MATRIX

	MR5.0 07930-19009	MR5.1 07930-19109	MR5.2 NOT USED	MR5.3 07930-19209	MR6.0 07930-19010	MR6.1 07930-19110	7933XP 7935XP CACHE	DUAL PORT
DMA PCA 07930-6X001	OK	OK	NOT USED	OK	OK	OK	NOT OK	OK
DMA PCA 07930-6X301	NOT OK	NOT OK	NOT USED	OK	OK	OK	NOT OK	OK
MPU PCA 07930-6X002	OK	OK	NOT USED	OK	NOT OK	NOT OK	NOT OK	NOT OK
MPU PCA 07930-6X302	OK	OK	NOT USED	OK	OK	OK	OK	OK
7933XP CACHE 7935XP CACHE	NOT OK	NOT OK	NOT USED	NOT OK	NOT OK	OK	****	NOT OK
DUAL PORT	OK	OK	NOT USED	OK	NOT OK	NOT OK	NOT OK	****

WARRANTY: None. This is an information only service note.

7933XP-02
7935XP-02
97930XP-01

SERVICE NOTE

MODELS: 7933XP
7935XP
97930XP

Supersedes: None

APPLIES TO:	All Units ☒	Only Units on Agreement ☐	
PERFORM:	Immediately ☒	At PM/Normal Call ☐	
	On Failure ☐	Information Only ☐	
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:	0.3hrs.		
PARTS:	X		
TRAVEL:	X		
SERVICE INVENTORY	Return for update ☒	Use as is ☐	
	Return for salvage ☐	See text ☐	
WARRANTY EXTENDED UNTIL:	July 1, 1987		

SERIAL NUMBERS:

7933XP AND 7935XP
DISC DRIVES SERIAL
NUMBER PREFIX 2617
AND BELOW

97930XP UPGRADE KITS
SERIAL NUMBER PREFIX
2629 AND BELOW

Repair Type: 02G
Repair Class: CO
Service Code: 20044
Supply Div.: 4800

PARTS AFFECTED:
07930-60257 CDMA PCA

TITLE: NEW CDMA PCA FOR CACHE DRIVES

PROBLEM: An asynchronous input to the controller state machine on the CDMA PCA can violate the minimum set-up time required for the state machine input registers. This can cause the output of the controller state machine to go into an unstable state.

SYMPTOM: The output of the controller state machine controls the addressing of both the dynamic and static memory used in cache. Disruption of these control lines can cause an addressing error in cache or static memory during a data transfer. This misaddressing error can cause the following symptoms:

- DERR 104 Double bit static RAM error
- DERR 110 Double bit dynamic RAM error
- Undetected data corruption

PD/sg

6/86-48

9320-4766 (1/83)

HEWLETT PACKARD

SOLUTION: The CDMA PCA has been redesigned to add a latch to the input of the the controller state machine to eliminate the possiblity of an unstable output. This change has resulted in a new part number for the CDMA PCA (07930-69357).

ACTION: Replace the 07930-60257 CDMA PCA in all 7933/35XP disc drives and 97930XP cache upgrades in the serial number ranges listed above with a 07930-69357 CDMA PCA.

MR6.1 firmware in these units should be upgraded to MR6.2 with the 07930-60269 firmware upgrade kit. Refer to Service Note 7933/35XP-03 or 97930XP-02 for replacement and warranty instructions related to the firmware update.

WARRANTY: DMD will accept warranty as follows except for units purchased internally by HP (TAC units).

```
**************************************************************************
*                                                                        *
*    LABOR:  0.3 hours                                                   *
*                                                                        *
*    PARTS:  CDMA PCA                07930-69357                         *
*                                                                        *
*    TRAVEL: YES                                                         *
*                                                                        *
*    When completing the Customer Support Order (CSO), the repair        *
*    type must be coded 02G and the repair class must be coded CO        *
*    (component).  The service code block must be filled in with         *
*    20044.  For FIREMAN/HECTS users, the service code (20044)           *
*    must be entered in the PRINT field.                                 *
**************************************************************************
```

7933H-25 7935XP-03
7935H-25 97930XP-02
7933XP-03

SERVICE NOTE

Supersedes: None

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☒
	On Failure ☐		Information Only ☐
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:	YES		
TRAVEL:			X
SERVICE	Return for update ☒		Use as is ☐
INVENTORY	Return for salvage ☐		See text ☐
WARRANTY EXTENDED UNTIL:	August 1, 1987		

MODELS: 7933H
7935H
7933XP
7935XP
97930XP

SERIAL NUMBERS:

See Text

PARTS AFFECTED: 07930-19209 MR5.3 Firmware
07930-19110 MR6.1 Firmware

Repair Type: 02G
Repair Class: CO
Service Code: 20045
Supply Division: 4800

TITLE: Firmware Update MR5.4 and MR6.2

PROBLEM: The Medusa chip, used to replace the PHI HP-IB controller chip on the 07930-60301 DMA PCA and the 07930-60357 CDMA PCA, contains an enhancement that allows the HP-IB bus to use a delayed handshake mode. This delay handshake mode is not used by the 793X disc drives. However, under certain conditions the current firmware can inadvertantly set the Medusa chip in the delayed handshake mode. Once set, the delayed handshake mode can only be reset by cycling drive power.

SYMPTOM: Normally the Medusa chip transfers data across the HP-IB at a rate of one megabyte per second. If the delayed handshake mode is set, the data transfer rate for disc read operations is decreased to 625 kilobytes per second. This slower transfer rate can cause up to a 10% decrease in system performance. This problem is a perfomance issue only; it does not affect data integrity.

PD/sg

6/86-48

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SOLUTION: The 793X firmware has been modified to eliminate the possibility of the Medusa chip being set in the delayed handshake mode. This firmware modification requires two new revisions of firmware; MR6.2 and MR5.4. All standard 7933/35H disc drives and 7933/35XP disc drives currently produced are shipped with MR6.2 firmware. MR5.4 firmware is required to support 7933/35H disc drives with the dual port option (OPT H22) or the 07930-6X002 Microprocessor PCA.

Two update kits have been set up to upgrade from MR5.3 to MR5.4, and from MR6.0 or MR6.1 to MR6.2. On the next PM or service call any 7933/35 disc drive with a 07930-6X301 DMA PCA or 07930-6X357 CDMA PCA must be updated to the correct revision of firmware as described below.

UNITS AFFECTED	UPDATE KIT REQUIRED	
7933H and 7935H disc drives with serial number prefix 2607A through 2621A	MR6.2	07930-60269
7933XP and 7935XP disc drives with serial number prefix 2617A or below.	MR6.2	07930-60269
Units with 97930XP Cache Upgrades with serial number prefix 2629A or below.	MR6.2	07930-60269
7933H and 7935H disc drives updated to MR5.3 and the 07930-69301 DMA PCA per Service Note 7933/35H-23	MR5.4	07930-60270
7933/35H drives with OPT H22 (dual port) and serial prefix 2607A through 2621A	MR5.4	07930-60270

TO CONVERT MR5.3 to MR5.4 USE MR5.4 UPDATE P/N 07930-60270

Replace:	FROM	TO
U162 ROM3 on MPU PCA	07930-82293	07930-82393
U122 ROM6 on MPU PCA	07930-82296	07930-82396

TO CONVERT MR6.1 TO MR6.2 USE MR6.2 UPDATE P/N 07930-60269

Replace:	FROM	TO
U182 ROM2 on MPU PCA	07930-82102	07930-82202
U122 ROM6 on MPU PCA	07930-82116*	07930-82216

*07930-82106 used in MR6.0

NOTE: Used PROMs should be discarded. Do not return to DMD.

All 07930-19209 MR5.3 firmware sets and 07930-19110 MR6.1 firmware sets in FSI should be returned for credit. Following are the new part numbers associated with this firmware change.

DESCRIPTION	P/N
MR5.4 F/W FULL SET	07930-19309
MR5.4 UPDATE (2 ROM)	07930-60270
MR6.2 F/W FULL SET	07930-19210
MR6.2 UPDATE (2 ROM)	07930-60269

WARRANTY: DMD will pay warranty for the firmware update kits only. DMD will not pay warranty for units requiring full firmware sets when a 07930-69301 is used to replace a 07930-6X001 DMA PCA (refer to Service Notes 7933H-23 and 7935H-23), or for units purchased internally by HP (TAC units).

****
*
* LABOR: NONE
*
* PARTS: MR5.4 F/W Upgrade Kit 07930-60270
* or MR6.2 F/W Upgrade Kit 07930-60269
*
* TRAVEL: NONE
*
* When completing the Customer Support Order (CSO), the repair
* type must be coded 02G and the repair class must be coded CO
* (component). The service code block must be filled in with
* 20045. For FIREMAN/HECTS users, the service code (20045)
* must be entered in the PRINT field.
****

7933H-22 7933XP-04
7935H-22 7935XP-04

S E R V I C E N O T E

Supersedes: None

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☐		Information Only ☒
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:			X
TRAVEL:			X
SERVICE INVENTORY	Return for update ☐		Use as is ☐
	Return for salvage ☐		See text ☒
WARRANTY EXTENDED UNTIL:	N/A		

MODELS:
7933H 7933XP
7935H 7935XP

SERIAL NUMBERS:
serial prefix 2622 and greater

PARTS AFFECTED:
07930-60256

TITLE: NEW REAR CRASH PAD MATERIAL

SYMPTOM: Head load failures during drive spin up, causing one or more of the following errors:

TERR 180	TERR 236
TERR 224	PART 2
TERR 235	PART 3

CAUSE: The material used in the rear crash pad is slightly sticky and if the carriage has been sitting in contact with the rear crash pad, it may stick and prevent the actuator from loading heads.

SOLUTION: Replace the rear crash pad assembly (part no. 07930-60256). The replacement procedure is described in the 7933/35 Service Manual.

The material used in the 07930-60256 rear crash pad assembly has been changed to a less sticky material. All 7933/35 drives shipped with serial prefix 2622 or later use this new material. Rear crash pad assemblies using the new material can be identified by two small, raised circles on the pad surface.

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CPC/PCE inventory has been purged of all 07930-60256 crash pad assemblies using the old material. All old style crash pads in FSI should be scrapped.

NOTE: Earlier vintage 7933H disc drives (approximately serial number 2216A01700 and earlier) have a thinner rubber pad on the rear crash pad than later drives and thus may not be compatible with the newer assembly. Since the thicker pad moves the actuator closer to the spindle, it is possible for the carriage latch to bind with the carriage unless the latch is moved toward the spindle by the same amount. This can be corrected by using non-magnetic washers (part no. 2190-0402) as 0.40 inch "shims" between the linear motor and the carriage latch housing.

WARRANTY: None. This is an information only service note.

7933/35H-26
7933/35XP-05

S E R V I C E N O T E

Supersedes: None SUPERSEDES:

APPLIES TO:	All Units ☐		Only Units on Agreement ☒
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☒		Information Only ☐
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:	Yes		
TRAVEL:			X
SERVICE	Return for update ☐		Use as is ☐
INVENTORY	Return for salvage ☐		See text ☒
WARRANTY EXTENDED UNTIL:	1 March 1988		

MODELS AFFECTED:
7933H 7935H
7933XP 7935XP

PARTS AFFECTED:
07930-60036
07930-69036

DRIVE SERIAL PREFIX:
7933H 2603A26147 Through 2625A29670
7935H 2603A05312 Through 2625A06336
7933XP 2608A01000 Through 2625A01542
7935XP 2617A01035 Through 2625A01082

Repair Type: 02G.
Repair Class: SN
Service Code: 20049
Supply Division: 4800

TITLE: PREMATURE SPINDLE MOTOR FAILURES

PROBLEM: 7933/35/H/XP disc drives shipped between February and June 1986 have been experiencing premature spindle motor failures. One of DMD's bearing vendors made a manufacturing change that, under certain conditions, can cause the bearing seal to rub in the bearing race, resulting with excessive bearing friction.

SYMPTOM: The symptoms associated with this problem are most apt to appear as a spindle failure while attempting to spin the drive up after it was spun down after an extended period of operation. Failures may also occur during run time operation. Spindle failures related to this problem will always be accompanied with specific TERR and DERR faults indicating either a spindle motor problem and/or a loss of spindle speed (i.e. HFR=%XX1 or %XX3). The specific faults are:

1. TERR 136 - Spindle won't rotate.
2. TERR 141 - Spindle didn't reach speed in time.
3. TERR 187/188 - See note.
4. TERR 225/238 - See note.
5. TERR 253/DERR 64 - See note.

PD/ss 2/87-48

9320-4766 (1/83)

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FOR MORE INFORMATION, CALL YOUR LOCAL HP SALES OR SERVICE OFFICE or East (201) 265-5000 • Midwest (312) 255-9800 • South (404) 955-1500 • West (213) 970-7500 or (415) 968-9200 OR WRITE, Hewlett-Packard, 1820 Embarcadero, Palo Alto, California 94303. IN EUROPE, CALL YOUR LOCAL HP SALES or SERVICE OFFICE OR WRITE, Hewlett-Packard S.A., 7, rue du Bois-du-Lan, P.O. Box, CH-1217 Meyrin 2 - Geneva, Switzerland. IN JAPAN, Yokogawa-Hewlett-Packard Ltd., 1-27-15, Yabe Sagamihara City, Kanagawa Prefecture, Japan 229.

Note: The HFR will always indicate a loss of spindle speed (HFR=%XX1 or %XX3).

SOLUTION: If a 7933/35 disc drive listed in the above serial number ranges fails with one or more of the symptoms described, replace the spindle motor.

FSI spindle motors (part number 07930-69036) should be inspected. If the spindle motor date code is 2609 through 2627, return the spindle motor to SMR. The date code can be found on the white tag located on the top of the mounting flange near the spindle hub.

WARRANTY: DMD will extend warranty through March 1, 1988. Extended warranty will cover parts only (part number 07930-69036) for the replacement of the original spindle motor on failure only. Labor and travel are not covered under extended warranty.

```
**********************************************************************
* NOTE:  To receive proper credit for extended warranty, the         *
*        date code attached to the defective spindle motor           *
*        must be entered in the REPAIR DETAILS field of the          *
*        CSO.  The date code is found on a white tag as shown        *
*        below, where XXXX represents the date code.                 *
*                                                                    *
*                        ------------------                          *
*                        |     48-XXXX     |                         *
*                        |  Made in U.S.A. |                         *
*                        ------------------                          *
*                                                                    *
**********************************************************************

**********************************************************************
* NOTE:  When completing the Customer Support Order (CSO) Form       *
*        the SERVICE CODE block must be filled in with "20049".      *
*        This code will allow DMD to monitor the implementation      *
*        of this service note and prevent rejection of warranty      *
*        billing.                                                    *
**********************************************************************
```

7933H-27 7935H-27
7933XP-06 7935XP-06

SERVICE NOTE

Supersedes:

APPLIES TO:	All Units ☐		Only Units on Agreement/Warranty ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☐		Information Only ☐
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:			X
TRAVEL:			X
SERVICE	Return for update ☐		Use as is ☐
INVENTORY	Return for salvage ☐		See text ☐
WARRANTY EXTENDED UNTIL: N/A			

MODELS AFFECTED:

7933H 7935H
7933XP 7935XP

PARTS AFFECTED:
07930-10310
MR6.3 FIRMWARE

SERIAL NUMBERS: All drives with serial prefix earlier than 2714.

TITLE: NEW FIRMWARE REVISION MR6.3

SYMPTOM: During the head unload sequence a DERR 49 (sector compare error) message will appear on the front panel. The DERR 49 is not logged in the drive's Fault Log, nor reported to the host system. This is a nuisance problem only and does not affect drive reliability or data integrity.

PROBLEM: Under certain conditions the current firmware can cause a flag in the firmware code to have an incorrect value. This causes one sector in one of the four maintenance track copies to be incorrectly written with an illegal sector address. Since there are four redundant copies of the maintenance information this error should not be reported by the front panel.

SOLUTION: The 7933/35 firmware has been changed from MR6.2 to MR6.3 (part number 07930-10310). This new revision of firmware eliminates the possibility that the firmware flag will be incorrectly set. Currently all 7933/35 "H" and "XP" disc drives are shipped with MR6.3.

The MR6.3 firmware change fixes a nuisance problem only and has no effect on drive reliability, performance, or data integrity. Therefore, there is no need to upgrade to MR6.3 firmware unless a drive is experiencing the DERR 49 message during a head unload. The DERR 49 message can

By SS 4/27/87 PCO # 4800

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also be eliminated by re-formatting the maintenance tracks.

Note: This is not a mandatory update service note. An upgrade kit to upgrade from earlier firmware revisions to MR6.3 is not available. The entire MR6.3 firmware set must be purchased, order part number 07930-10310.

FSI inventory of existing MR6.2 firmware (07930-19210) should be returned to CPC/PCE for credit.

WARRANTY: None. This is an information only service note.

7933/35H-28

SERVICE NOTE

Supersedes: None SUPERSEDES:

APPLIES TO:	All Units ☒		Only Units on Agreement ☐
PERFORM:	Immediately ☐		At PM/Normal Call ☐
	On Failure ☐		Information Only ☒
WARRANTY:	EXTENDED	NORMAL	NONE
LABOR:			X
PARTS:			X
TRAVEL:			X
SERVICE	Return for update ☐		Use as is ☒
INVENTORY	Return for salvage ☐		See text ☐
WARRANTY EXTENDED UNTIL:	N/A		

MODELS AFFECTED:

7933H 7935H

Option H22 Only
(Dual Port)

PARTS AFFECTED:
07930-10409
MR5.5 FIRMWARE

SERIAL NUMBERS: All Option H22 drives with serial prefix earlier than 2715

TITLE: NEW FIRMWARE REVISION FOR DUAL PORT DRIVES ONLY

SYMPTOM: The addition of the second DMA PCA in a dual port configuration (Option H22) can cause the data transfer rate to decrease by as much as 30% during data transfers in excess of 23 kbytes (one track).

PROBLEM: When a head switch occurs during a data transfer the firmware unnecessarily interrogates the second DMA HPIB channel. As a result, the target sector immediately after the head switch is missed, which automatically induces a rotational latency.

SOLUTION: The dual port firmware code has been modified to inhibit the interrogation of the second DMA HPIB channel during a head switch. This modification has resulted in new firmware revision MR5.5 for dual port drives. A seven PROM MR5.5 firmware set is available for updating existing dual port drives (part number 07930-10409). 7933/35H disc drives ordered with the dual port option H22 will be shipped with MR5.5 firmware.

PD/ss 5/87-48

9320-4766 (1/83)

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Due to the small number of dual port 7933/35 disc drives in use, MR5.5 firmware has been set up for dual port use only. MR5.4 firmware will remain available for supporting non-dual port drives with the old style microprocessor PCA (07930-6X002). (Refer to Service Note 7935H-23 for details).

WARRANTY: None. This is an information only service note.

APPENDIX B

HP 7933XP
HP 7935XP

CONTROLLER CACHE DESCRIPTION

CONTENTS

ILLUSTRATIONS

Title **Page**

B-1. Introduction

B-2. Product Overview

The HP 7933XP and the HP 7935XP Controller Cache Disc Drives are high performance versions of the HP 7933H and the HP 7935H. The higher performance is achieved by adding one megabyte of memory to the disc drive controller. Existing HP 7933H and HP 7935H Disc Drives can be upgraded to the "XP" configuration by installing the HP 97930XP Upgrade Kit. The one-megabyte controller cache memory is accomplished by changing to a new DMA PCA, adding a CACHE PCA, and changing to a new revision of firmware. HP 7933/35H Disc Drives having serial numbers prefixed 2337 and below contain a Microprocessor PCA (part no. 07930-60002). The 97930XP Upgrade requires a Microprocessor PCA (part no. 07930-6X302). The added one-megabyte random access memory (RAM) keeps the last 255 active areas (16 sector blocks) of the disc so that future accesses to these same areas may be provided to the host without a physical read actually occurring. The objective of this "controller cache" memory is to decrease the overall disc response time and increase system throughput. The amount of system performance improvement will vary depending upon individual system configuration and program application.

The controller cache is implemented as 255 blocks, or pages, of 4096 bytes (16 sectors) each. When the host requests a read, the cache memory will be searched to determine if the entire request can be satisfied from cache. If the request cannot be satisfied from cache, a physical read from the disc will be initiated. When a physical read is 4096 bytes or less, a full 4096 byte read will be initiated beginning at the start address requested by the host and the entire 4096 bytes will be stored in cache. When a new block is needed, the least recently used block is made available for the transfer.

When the host requests a write, controller cache will be searched for all domains which overlap the area to be written. If the entire write request will fit into one cache block, that block will be updated and retained, and all other cache blocks will be flushed from cache memory. If the data to be written is not in a cache block, the data from the write will be written onto the disc, but it will not be retained in cache. The cache will not provide immediate response for writes and the host will have to wait for write operations to complete.

B-3. Objective

The objective of this guide is to familiarize CE's with the new HP 7933/35XP Controller Cache Disc Drives. It is expected that the CE has already had 200 level training on the HP 7933/35H disc products. It is not necessary to have an HP 7933/35XP drive at your disposal to study this guide, but if one is available, it would be useful for familiarization purposes.

After studying this guide, a CE will be qualified to install and service HP 7933/35XP drives and the 97930XP upgrade kit.

The following topics will be discussed:

1. Product Overview
2. Theory of Operation
3. Diagnostic and Utilities
4. Troubleshooting

B-4. Related Manuals

The following manuals provide additional application and technical information about controller cache.

- General Information Manual (part no. 5953-3670)
- Application Engineering Manual (part no. 5953-3672)
- 97930XP Upgrade Kit Installation Manual (part no. 07930-90911)
- HP 7933 and 7935 Service Manual (part no. 07930-90903)
- HP 7933 and 7935 CE Handbook Section (part no. 07930-90905)

B-5. Theory Of Operation

B-6. Hardware

B-7. Standard DMA PCA

As a review, the basic block diagram of the standard DMA is shown in figure B-1. A brief illustrated description follows figure B-1. A thorough discussion on the theory of operation of the DMA PCA can be found in the 7933 and 7935 Disc Drive Service Manual.

B-8. CDMA PCA

The addition of the one-megabyte controller cache memory used in the HP 7933/35XP drives is accomplished by replacing the standard DMA PCA with the CDMA PCA, and adding an additional CACHE PCA. The functional block diagram of the CDMA and the CACHE PCA is shown in figure B-2. The CDMA PCA is functionally the same as the standard DMA PCA, with three major changes. The DATA RAM has been removed and replaced by the CACHE PCA, and a REFRESH TIMER and CACHE ERROR DETECTION has been added.

B-9. Host Reads

When the host requests a read that is less than or equal to 4096 bytes, controller cache will be searched to determine if the entire request can be satisfied from one cache block. If the request cannot be satisfied from one cache block, a physical read will take place beginning at the start address requested by the host and encompassing a full 4096 byte block. This block will then be stored in cache DRAM array.

If the read request is greater than 4096 bytes, cache will not be searched. The request will be handled by the 4096 BYTE STATIC RAM on the CACHE PCA (this is identical to the Data RAM on the standard DMA PCA). The data will not be stored in the DRAM array.

If sections of a read can be satisfied from several blocks, but the entire request cannot be satisfied from one block, a physical read will occur to read in a full 4096 byte block that contains the entire request. The blocks that contain the overlapping data will not be flushed from cache until a write of that data is requested. If a read request can be satisfied from more than one block, the first block found that contains the entire request will be used. When a new block is needed in the cache to satisfy a request, the least recently accessed block will be made available for the transfer.

B-10. Host Writes

When the host requests a write, controller cache will be searched for all blocks which overlap the area to be written. If the write request resides in one cache block, the amount written by the host will be updated in the cache block, physically written to the disc and retained. (The updating of cache, and the physical write actually occur simultaneously. There is a millisecond overhead for the search of controller cache.)

Any write request that resides in controller cache but is greater than 4096 bytes, or is present in more than one cache block (overlapping), will be flushed from cache, and physically written to disc. If the data to be written is not in controller cache at all, the physical write will occur and the data will not be retained in controller cache. The net effect of the write operation is that controller cache will not provide immediate response for writes. The host will have to wait for physical writes to disc to complete.

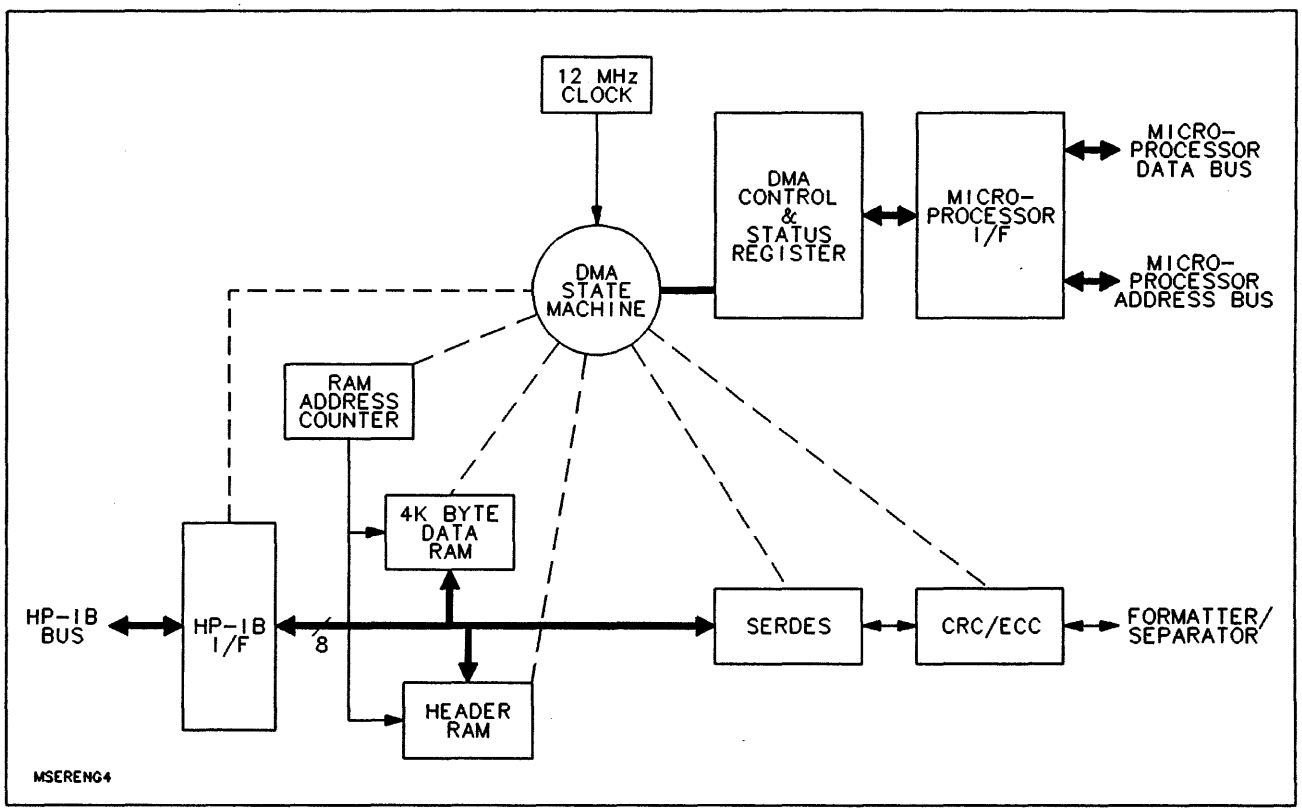

Figure B-1. Standard DMA Block Diagram

B-11. Standard DMA Functional Description

B-12. HP-IB Interface

Controls the interfacing between the host and the disc drive. Drive commands are sent to the microprocessor and data is routed to the DATA RAM.

B-13. Data Ram

The 4096 bytes of static RAM allow for buffering up to 16 sectors of data. All data enroute to or from the disc drive must pass through the DATA RAM.

B-14. Header Ram
The HEADER RAM is used to store the preamble and postamble information during each sector of disc access.

B-15. SERDES
The serializer/deserializer (SERDES) changes serial data from the disc to parallel bytes for buffering and subsequent transfer over the HP-IB. The SERDES also changes parallel data enroute to the disc into a serial data stream.

B-16. CRC/ECC
The CRC/ECC module adds redundant information to the data during a write operation. On a read, the CRC/ECC module examines the data and the redundant information to determine if an error has occurred. It can detect and correct errors 12 bits or less in length, and detect errors greater than 12 bits in length.

B-17. DMA State Machine
The state machine controls the data transfer through all portions of the DMA PCA. The state machine is controlled by the microprocessor through the DMA Control and Status registers.

B-18. Control And Status Registers
The Control and Status Registers are accessed by the microprocessor through the microprocessor interface.

B-19. Microprocessor Interface
Interfaces the DMA PCA with the microprocessor through the microprocessor data and address busses.

B-20. 12 MHz Clock
Supplies the clock required by the Transfer Control State Machine.

B-21. Ram Address Counter
The RAM address counter is used to address the proper RAM addresses during data transfers.

B-22. Controller Cache Functional Description

B-23. Cache Error Detection
The cache error detection circuitry provides double bit error detection and single bit error correction for the CACHE PCA. A 5 bit hamming code is encoded with each byte of read or write data transferred to the CACHE PCA. When the data is transferred back to the CDMA PCA, the hamming code is decoded to ensure the integrity of the data. If a single bit error is detected, it is corrected and the data is passed on to the host (read) or to the disc (write) without generating an error status. If the error detection circuitry detects a double bit error, the microprocessor is flagged, a DERR 110 is entered in the Fault Log, and an UNCORRECTABLE DATA status is sent to the host. It is important to note that the cache error detection circuitry only ensures the data integrity of the data as it is transferred through the CACHE PCA.

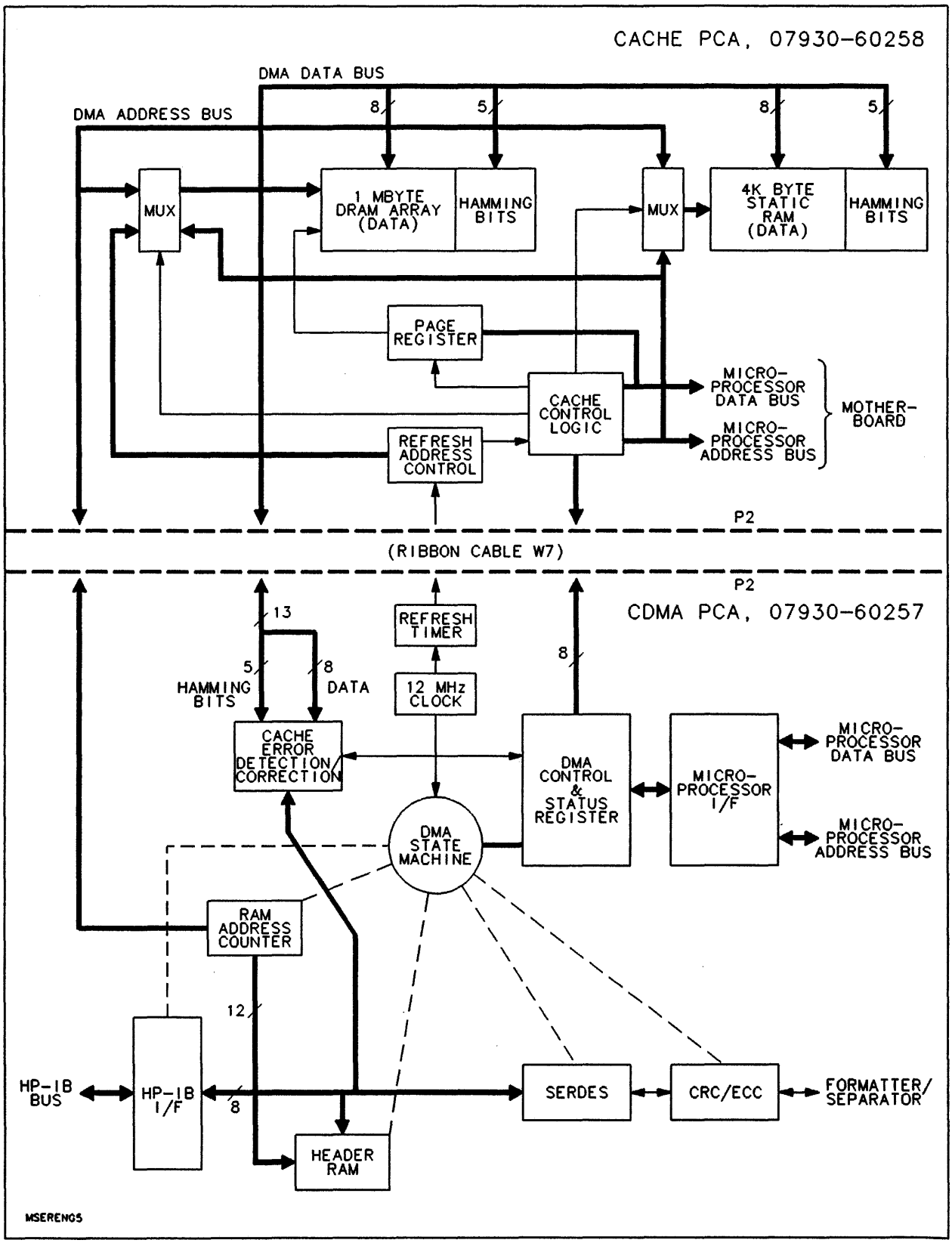

Figure B-2. CACHE/CDMA Block Diagram

B-24. Refresh Timer

The dynamic RAM (DRAM) used on the CACHE PCA requires a refresh cycle every 15 microseconds to re-write the contents of each bit cell in the 1 Mbyte memory array. The refresh timing signal is derived from the 12 MHz oscillator used by the state machine on the CDMA PCA. The actual refresh control circuitry is on the CACHE PCA.

B-25. Cache PCA

The CACHE PCA is located in card cage slot A5 and is interconnected with the CDMA PCA through a ribbon cable. The microprocessor data bus and address bus are connected to the CACHE PCA by way of the Motherboard. Fundamentally, the CACHE PCA replaces and expands the data RAM that was removed from the DMA PCA. It also contains the additional circuitry necessary for controlling the CACHE paging scheme.

B-26. Dram Array

The 1 Mbyte DRAM array is the actual cache memory array use for disc caching. The array is 13 bits wide (8 data bits and 5 hamming bits for error detection) and contains 1,048,576 addresses. The array can be addressed through the multiplexer on the address bus by the CDMA address counter for data transfers; by the refresh address counter for memory refresh cycling; and by the microprocessor via the microprocessor address bus for diagnostic purposes.

B-27. Static Ram

The 4096 byte static RAM is identical to the data RAM on the standard DMA with the exception of the additional 5 hamming bits for error detection. The static RAM is only used when a continuous data transfer exceeds 16 sectors, or if disc caching has been disabled. The static RAM is addressed through a multiplexer by the CDMA address counter for data transfers, or by the microprocessor address bus for diagnostic purposes.

B-28. Control Logic

The function of the control logic is to manage the operations on the CACHE PCA. It uses inputs from the microprocessor and the CDMA control logic to control the addressing of the static and dynamic RAM arrays on the CACHE PCA.

B-29. Page Register

The page register selects the appropriate page from the 255 pages (4096 bytes each) of cache memory as requested by the microprocessor via the microprocessor data bus.

B-30. Refresh Address Control

The refresh address control addresses the appropriate portion of the DRAM array to be re-written during the refresh cycle. It receives its timing from the CDMA.

B-31. Diagnostics And Utilities

The controller cache firmware used in the 7933/35XP products include some new diagnostics and utilities. The major change in the diagnostics is the addition of a memory test on the cache RAM during the power-on diagnostic. This diagnostic will report any errors found during the test and disable cache if the memory diagnostic fails. New utilities in firmware will allow the host to disable cache and access the Cache Error Log and Cache Statistics Table.

B-32. Diagnostic Error Handling

Controller cache diagnostics consist of four separate read/write/compare data tests added to microdiagnostic Test 14. All tests perform the same type of test, but the data written to the memory changes. In the first test, zeros are written to every cache page. After all pages are written, all pages are checked to ensure that zeros are still found. In the second test, the pattern is changed to all ones and the test is repeated. Test three is a repeat with a different pattern in each page going forward. (Page 0 contains 0's, page 1 contains 1's etc.) In test four, the test is repeated with a different pattern going backward. (Page 255 contains 0, 254 contains 1 etc.)

In all four tests, if one or more correctable errors are found in a page, the error log of correctable errors is incremented by 1. If one or more uncorrectable errors are found in a page, the error log of uncorrectable errors is incremented by 1. Note that every byte in the cache could be bad and we will only increment the count once per page per test. All diagnostics, including the controller cache tests of Test 14 are run at Power-On, and if initiated from the HIO. However, if Test 00 is initiated by the system host, or an HP 85, **after** Power-On, Test 14 will be run **without** the controller cache tests.

After Power-On, if Test 14 is initiated by specific request from the HIO, the system host, or the HP 85, the controller cache tests will be included. If the data comparison test fails at any point, the test will create a TERR entry in the Fault Log, and the diagnostic will terminate. The zero and one tests will generate a TERR 71 and the different pattern in each page tests will generate a TERR 72 in this case.

At the end of the diagnostic, if any uncorrectable errors have been found, (uncorrectable count incremented), a TERR 71 will be generated.

The Cache Error Log values are only incremented by the DMA diagnostic. The error log values are initialized to zeros by the Clear Logs command and by drive power-on. The diagnostic never resets the error logs counts to zero.

B-33. Run-Time Error Handling

During run-time processing, all correctable errors will be ignored. The firmware will not count the errors nor notify the host that they have occurred. All correctable error flags will simply be cleared by the firmware at the end of every transfer.

If the uncorrectable error flag is set at the end of a transfer, the following action will be taken:

1. A controller fault is generated to notify the host that bad data has been transferred to the host.

2. A DERR 110 is entered into the Fault Log to indicate that an uncorrectable error occurred.

3. The entire controller cache is flushed and reinitialized so that the cache page which caused the error is the first page to be reused.

If an uncorrectable error is found on three (3) consecutive transfers, the error is considered a hard, repeatable error and the following action is taken:

1. A controller fault is sent to the host to indicate a bad data transfer has taken place.

2. A DERR 109 is entered into the Fault Log instead of the third DERR 110 to indicate a "hard" error.

3. Controller cache is disabled. The cache status is set to the same state it is in when the DMA diagnostic fails. The host may not re-enable the cache. The cache will only be re-enabled if the drive successfully passes the DMA diagnostic.

4. The following message is placed on the front panel to indicate that the cache subsystem has been disabled: **NOCACH** * (where * is the HP-IB device address.)

B-34. New Derr's

The following are new DERR's which may be returned by a 7933/35 with cache installed:

DERR	MEANING
104	A double bit error was detected in static RAM. The drive will allow reads but will block all writes to prevent destroying data on the disc.
109	The cache detected three (3) DERR 110's in three consecutive transfers from the same cache page. Because of this repeatable error, the cache has been disabled. The operator is notified of this event with a message on the front panel. No message is sent to the host computer indicating that the status of the cache has changed. However, the host is notified of the bad data transfer by a controller fault which is returned by the drive. The drive will set the cache status byte in the cache statistics table to indicate that the cache was disabled because of RAM error. (See "Cache Statistic Tables" below)
110	While performing a host transfer out of the cache memory, a double bit error was detected in the cache memory. When this DERR is returned, bad data has been transferred to the host if the operation was a read or bad data has been written to disc if the operation was a write. The host computer is notified of the uncorrectable by a controller fault status return.

B-35. New Terr's

The following are new TERR's which may be returned by a 7933/35 with controller cache installed:

TERR	MEANING
71	The memory failed a data write/read/compare test. The test was either writing zero's or one's to the cache memory and verifying the contents. This requires a double bit error in the cache memory if the Hamming error correction is working properly. This TERR is also returned when an uncorrectable error is found in the cache dynamic RAM array.
72	The cache page addressing failed. Data was written to one page of the cache and it modified a different page. This could also be a pattern sensitivity in the cache memory.
73	The cache failed to transfer data correctly from the cache memory to the disc media through the DMA. This could be either a DMA problem or a cache problem or the cable between them.
74	The diagnostics found a data miscompare while testing the RAM used to store the cache tables. The table RAM is not accessed through the Hamming error correction so this error will be returned for a single-bit error in the table RAM.
75	The diagnostics found an uncorrectable error while testing the 4K static RAM buffer. However, this RAM has already successfully passed a data compare test. Therefore, this could be an intermittent RAM failure or a failure in the Hamming error correction circuitry or the extra parity bits for the Hamming correction.

If any of the above TERR's are returned by the DMA diagnostic, the drive will disable the cache subsystem. In this case, the operator will be notified on the drive's front panel with the following message: **NOCACH** * (where * is the HP-IB device address.)

B-36. Cache Control Utility

A new utility has been added to the firmware to allow the host to enable or disable controller cache under software control. If the disc drive receives a request to disable controller cache and it is already disabled, the request will be ignored. And if the disc drive receives a request to enable controller cache and it is already enabled, the request will be ignored. There is no execution message. If the controller cache was disabled by a diagnostic failure, this command will NOT enable it. The only way to enable controller cache in this case is to successfully pass the DMA diagnostic (TEST 14) or the Power-On selftest.

If a standard 7933/35 disc drive receives a Cache Enable/Disable command and the caching option is not installed, the drive will return an "Illegal Opcode" status.

The following events will cause the disc drive to enable controller cache:

1. Power On
2. Device Clear command from host
3. Cache Enable command from host

The following events will cause the disc drive to disable the cache system:

1. DMA diagnostic failure
2. Power-on selftest failure
3. Cache Disable command from host.

B-37. Cache Error Log

The Cache Error Log keeps count of the correctable (single bit) and uncorrectable (double bit) errors that occurred in the cache memory during the DMA diagnostic only. The purpose of this log is to allow CE's to run a controlled test and have visibility of every error found in the cache memory. The Cache Error Log does NOT contain any run time error information, nor is it in any way connected with the Error Rate Test (ERT) Logs or Run Logs. When a double bit error is found by the DMA diagnostic, A TERR 71 will be generated and the Cache Error Log will be incremented. The error counts in the Cache Error Log will be cleared by the drive under the following conditions:

1. Power-on and power fail.
2. Clear Logs command with clear all parameter.
3. Clear Logs command with clear cache error log parameter.

B-38. Cache Statistics Table

The 7933/35XP disc drives keep statistics that allow the host to calculate the read hit ratio, the write hit ratio and the read/write ratio. The Cache Statistics table is read with the current Read Tables utility. These ratios are used to determine how effectively disc caching is being utilized. Additional information on these ratios and their relationship to system performance can be found in the Application Engineering Manual (P/N 5953-3672). The format of the Cache Statistics Table is as follows:

Cache status	1 byte	0 - Cache enabled 1 - Cache disabled by host request 2 - Cache hardware not installed 3 - Cache disabled because of RAM error May not be enabled by host.
Blockwrite status	1 byte	(Not used on the 7933/35XP)
Page size (bytes)		2 bytes
Number of pages		2 bytes
Number of reads		4 bytes
Number of read hits		4 bytes
Number of writes		4 bytes
Number of write hits		4 bytes

The Cache Statistics Table will be reset to zero in the following cases:

1. Device Clear command from the host.
2. Cache Enable command from the host.
3. Cache enabled automatically by the drive (power on).
4. Clear Cache Statistics command from the host.
5. If any statistic counts overflows the 4 byte integer.

B-39. Troubleshooting

Problems with the 7933/7935 disc drives with controller cache can be divided into two categories; cache related failures and non-cache related failures. The following discussion will explain some of the troubleshooting and diagnostic procedures for cache errors and also some considerations for troubleshooting non-cache problems on a drive with cache memory. The following discussion is not intended to be a complete troubleshooting guide for all types of 7933/7935 disc problems. Refer to the HP 7933 and HP 7935 Disc Drive Service Manual (part no. 07930-90903), and the HP 7933/7935 CE Handbook (part no. 07930-90905) for further details.

B-40. Controller Cache Related Failures

The primary diagnostic available for troubleshooting controller cache problems is the DMA diagnostic (TEST 14) resident in the 7933/7935 firmware. TEST 14 is used in conjunction with the Cache Error Log and the Fault Logs. Refer to paragraph B-31 and following.

TEST 14 logs a count of all correctable (single bit) errors and uncorrectable (double bit) errors that are encountered during the diagnostic in the Cache Error Log. If an uncorrectable error is encountered during the DMA diagnostic, the uncorrectable error count is incremented, the appropriate TERR is logged in the Fault Log, and the diagnostic is terminated. Correctable errors encountered during the DMA diagnostic are only counted in the Cache Error Log. They do not generate a TERR entry in the Fault Log nor cause the diagnostic to terminate.

B-41. Testing Controller Cache

The following procedure is used to test cache memory.

1. Clear Cache Error Log.
2. Run one pass of diagnostic TEST 14.
3. Read Cache Error Log and record contents.
4. Repeat steps 1 through 3 two more times.
5. Evaluate the contents of the Cache Error Log against the diagnostic error rate guidelines below.

The Cache Error Log can not be accessed through the HIO front panel. The HP 85 Service Tool, or a system level utility program, is required to access the Cache Error Log.

B-42. Controller Cache Diagnostic Error Rate

A. If there are 512 or more correctable errors per one pass of TEST 14, there is a hard failure. Replace the following parts in the order listed:

1. CACHE PCA
2. CDMA PCA
3. MICROPROCESSOR PCA

B. If there are less than 512 correctable errors per pass AND the correctable error count is different for each pass of TEST 14, there is a good chance of a cache hardware failure. Replace the parts in the order listed in Step A. If errors continue at a variable rate, additional troubleshooting is required.

C. If there is less than 512 correctable errors per one pass of TEST 14 and the error count is the same value for each pass, NO remedial action is required. This is an acceptable correctable error rate.

D. Any DERR or TERR encountered during TEST 14 should be considered a hardware failure and the appropriate corrective action should be taken.

B-43. Run Time Controller Cache Error Rate

The following are guidelines for the number of cache related DERR's allowed logged in the Fault Log in terms of the total number of sectors read.

DERR	Minimum # of Sectors/DERR
104	10 Million
109	0 (see note)
110	10 Million

Any DERR 109 should be considered a hardware failure and appropriate action should be taken.

B-44. Non-controller Cache Related Failures

Troubleshooting non-cache related failures (i.e. seek errors, spindle rotation, etc) is similar to troubleshooting a standard 7933/7935 drive. But it is important to realize that when controller cach is enabled, there can be a significant reduction in the amount of physical seeks and reads occurring on the drive. This does not affect internal diagnostics such as a read only error rate test (RO ERT), but it can have a significant impact on some on-line tests such as WORKOUT or COLOSSUS. If these types of programs are used to physically exercise the drive, controller cache should be disabled. Otherwise, if the on-line programs are consistently accessing the same disc addresses, most, if not all, of the data transferred will be between the host system and controller cache memory only. While this may be of some value for a system level exercise, it is of little value for exercising all functional areas of the drive. In particular, the entire read/write chain including the head/media interface, and the servo/mechanical portion of the disc drive. Controller cache should be re-enabled after troubleshooting is completed.

B-45. CS 80 External Exerciser

To aid in troubleshooting and supporting 7933/7935 disc drives with cache memory, the following new commands have been added to the HP 85 CS/80 External Exerciser program, revision 2534 or later.

```
CACHEON       - enables disc cache
CACHEOFF      - disables disc cache
CACHE STATUS  - shows status of disc cache (on, off, error, or not installed)
CACHE LOG     - read cache error log
RESET STATS   - resets cache statistics table
```

B-46. CS80UTIL Utility Program

The CS80UTIL program has been enhanced in revisions A.02.01 or later to support the 7933XP/7935XP disc drives on HP3000 computer systems. The new commands are identical to the cache commands added to the External Exerciser program, with one exception. The CACHE STATUS command is replaced with CACHE STATS. With CS80UTIL, the CACHE STATS command not only shows the status of disc cache as described but it also provides the information required to calculate the read, the write and the read/write hit ratio as described in the Cache Statistics Table.

An additional command has also been added to CS80UTIL that is helpful in running controller caching. The DIAG command allows internal diagnostics to be run on-line. With this command the DMA diagnostic (Test 14) can be run on-line. When the DIAG command is issued to a 7933/35 disc drive, it will terminate the command by initiating Test 0. This is necessary because all other internal diagnostic tests cause the drive to spin down. Test 0 will run all power-on diagnostics, reload heads, and return the drive to "drive ready" status.

CS80UTIL is the only on-line utility available to disable or enable disc caching on HP 3000 systems as there is no MPE command for this. In some instances it may be necessary to disable disc caching for troubleshooting or for performance measurement purposes. The following UDC's are suggested if there is a need to provide a method for the System Manager to disable/enable controller cache, or to access or reset the cache statistics table without running CS80UTIL directly.

```
cacheon ldev= "1"
run cs80util.cs80.telesup;info="cacheon !ldev"
**************************
cacheoff ldev="1"
run cs80util.cs80.telesup;info="cacheoff !ldev"
**************************
cachestats ldev="1"
run cs80util.cs80.telesup;info="cache stats !ldev"
**************************
resetstats ldev="1"
run cs80util.cs80/telesup;info="reset stats !ldev"
**************************
```

B-47. HP 1000 Exer Program

The following commands have been added to the EXER utility program for HP 1000 systems running RTE-A Revision 4.0 available from DSD. The command descriptions are the same as those listed for the External Exerciser above.

```
CACHEON
CACHEOFF
CACHE STATS
RESET STATS
CACHE LOG
```

HEADQUARTER OFFICES
If there is no HP Sales Office in your area,
contact one of these headquarter offices.

UNITED STATES:
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Rockville, MD 20850
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Hewlett-Packard Company
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Rolling Meadows, IL 60008
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