HP 13255

TERMINAL DUPLEX REGISTER MODULE

Manual Part No. 13255-91031

REVISED

APR-14-78

NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

The Terminal Duplex Register Module is a general purpose parallel input/output module for use in the HP 264XX DATA TERMINAL family. The interface has TTL levels (+5 volts and ground) for eight input data bits, eight output data bits, and eight input status bits. The module also has two command flip-flops (In and Out) for control of data flow. Jumper options allow the module to be configured in several ways for increased flexibility.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Terminal Duplex Register Module is contained in tables 1.0 through 6.4.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60031	8-Bit Duplex Register PCA	12.9 x 4.0 x 0.5	0.38

Number of Backplane Slots Required: 1

Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B ( ) Other:
Restrictions:	Type tested at product level
Failure Rate:	0.609 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 190 mA	@ mA	@ mA	@ mA
	NOT APPLICABLE	NOT APPLICABLE	NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 4.915 MHz

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
W1 - (U13)		
Jumper A	1K Input termination to GND	No Effect } One in and One out
B	1K Input termination connected to +5V	No Effect }
C	Set Out FF on $\overline{\text{OUTPUT}}$ = Low	No Effect
D	Not Used	Not Used
E	Module ADDR4 = 0	Module ADDR4 = 1
F	Module ADDR9 = 0	Module ADDR9 = 1
G	Module ADDR10 = 0	Module ADDR10 = 1
H	Module ADDR11 = 0	Module ADDR11 = 1

Table 4.0 Jumper Definitions (Cont'd.)

PCA Designation	Function	
	In	Out
W2 - (U15)		
Jumper J	Low on DEVICE IN Resets In FF	High on DEVICE IN Resets In FF
K	Low on DEVICE OUT Resets Out FF	High on DEVICE OUT Resets Out FF
L	COMMAND IN is high when In FF is set	COMMAND IN is low when In FF is set
M	COMMAND OUT is high when Out FF is set	COMMAND OUT is low when Out FF is set
N	OUTPUT ENABLE is high when Out FF is set	OUTPUT ENABLE always high
P	Selects negative 1 microsecond pulse	Selects only one. Others must be out. Signal goes out at P2, Pin S.
Q	Selects positive 1 microsecond pulse	
R	Selects +5 volts on	

5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2		Not used
-3	SYS CLK	4.915 MHz System Clock
-4		Not used
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8		Not used
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10		}
		}
-11		}
		} Not used
-12		}
		}
-13		}
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17		}
		}
-18		}
		} Not used
-19		}
		}
-20		}
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not used
-C		
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R		Not used
-S		
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		Not used
-W		
-X		
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z		Not used

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	COMMAND IN	In Flip-Flop (Polarity selected by Jumper L)
- 2	DEVICE IN	In Flip-Flop Reset (Polarity selected by Jumper J)
- 3	DATA OUT 7	Negative True, Data Out Register Bit 7
- 4	DATA OUT 6	Negative True, Data Out Register Bit 6
- 5	DATA OUT 5	Negative True, Data Out Register Bit 5
- 6	DATA OUT 4	Negative True, Data Out Register Bit 4
- 7	DATA OUT 3	Negative True, Data Out Register Bit 3
- 8	DATA OUT 2	Negative True, Data Out Register Bit 2
- 9	DATA OUT 1	Negative True, Data Out Register Bit 1
-10	DATA OUT 0	Negative True, Data Out Register Bit 0
-11	STATUS 6	Status Bit 6
-12	STATUS 4	Status Bit 4
-13	STATUS 2	Status Bit 2
-14	STATUS 0	Negative True, Status Bit 0
-15	GROUND	Ground

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P2, Pin A	COMMAND OUT	Out Flip-Flop (Polarity selected by Jumper M)
- B	DEVICE OUT	Out Flip-flop Reset (Polarity selected by Jumper K)
- C	$\overline{\text{DATA IN 7}}$	Negative True, Data In Register 7
- D	$\overline{\text{DATA IN 6}}$	Negative True, Data In Register 6
- E	$\overline{\text{DATA IN 5}}$	Negative True, Data In Register 5
- F	$\overline{\text{DATA IN 4}}$	Negative True, Data In Register 4
- H	$\overline{\text{DATA IN 3}}$	Negative True, Data In Register 3
- J	$\overline{\text{DATA IN 2}}$	Negative True, Data In Register 2
- K	$\overline{\text{DATA IN 1}}$	Negative True, Data In Register 1
- L	$\overline{\text{DATA IN 0}}$	Negative True, Data In Register 0
- M	STATUS 7	Status Bit 7
- N	STATUS 5	Status Bit 5
- P	STATUS 3	Status Bit 3
- R	$\overline{\text{STATUS 1}}$	Negative True, $\overline{\text{Status Bit 1}}$
- S	STROBE	Pulse or +5 Volts (Selectable by Jumpers)

Table 6.0 Module Bus Pin Assignments

Function Performed: Output Data	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (HGFE)	X	ADDR 12
Address determined by	H	ADDR 11
Jumpers H, G, F, and E	G	ADDR 10
Jumper Out = 1 Jumoer In = 0	F	ADDR 9
	X	ADDR 8
Function Specifier: Not Applicable	X	ADDR 7
	X	ADDR 6
	X	ADDR 5
Data Bus Bit Interpretation: (Note: These signals	E	ADDR 4
are negative true on the P2 interface.)	X	ADDR 3
	X	ADDR 2
	X	ADDR 1
B7 Output Data Bit 7	X	ADDR 0
	B7	BUS 7
	B6	BUS 6
B6 Output Data Bit 6	B5	BUS 5
	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
B5 Output Data Bit 5	B1	BUS 1
	B0	BUS 0
	1=Logical 1=Bus Low	
B4 Output Data Bit 4	0=Logical 0=Bus High	
	X=Don't Care	
B3 Output Data Bit 3		
B2 Output Data Bit 2		
B1 Output Data Bit 1		
B0 Output Data Bit 0		

Table 6.1 Module Bus Pin Assignments

Function Performed: Input Status

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (HGFE)
Address determined by
Jumpers H, G, F, and E
Jumper Out = 1 Jumper In = 0

Function Specifier: ADDR 0 = 0
ADDR 1 = 0
ADDR 2 = 0

Data Bus Bit Interpretation:

B7 Input Status Bit 7

B6 Input Status Bit 6

B5 Input Status Bit 5

B4 Input Status Bit 4

B3 Input Status Bit 3

B2 Input Status Bit 2

B1 Input Status Bit 1 }
}
}
B0 Input Status Bit 0 }

NOTE: These signals are negative true on the P2 interface.

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
H	ADDR 11
G	ADDR 10
F	ADDR 9
X	ADDR 8
X	ADDR 7
X	ADDR 6
X	ADDR 5
E	ADDR 4
X	ADDR 3
0	ADDR 2
0	ADDR 1
0	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.2 Module Bus Pin Assignments

Function Performed: Input Data	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (HGFE)	X	ADDR 12
Address determined by	H	ADDR 11
Jumpers H, G, F, and E	G	ADDR 10
Jumper Out = 1 Jumper In = 0	F	ADDR 9
	X	ADDR 8
Function Specifier: ADDR 0 = 1	X	ADDR 7
ADDR 1 = 0	X	ADDR 6
ADDR 2 = 0	X	ADDR 5
	E	ADDR 4
	X	ADDR 3
Data Bus Bit Interpretation: (Note: These signals	0	ADDR 2
are negative true on the P2 interface.)	0	ADDR 1
	1	ADDR 0
B7 Input Data Bit 7	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
B6 Input Data Bit 6	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
B5 Input Data Bit 5	B0	BUS 0
	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
B4 Input Data Bit 4	X=Don't Care	
B3 Input Data Bit 3		
B2 Input Data Bit 2		
B1 Input Data Bit 1		
B0 Input Data Bit 0		

Table 6.3 Module Bus Pin Assignments

Function Performed: Read Settings of Command Flip-Flops

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (HGFE)
Address determined by
Jumpers H, G, F, and E
Jumper Out = 1 Jumper In = 0

Function Specifier: ADDR 0 = 1
ADDR 1 = 1
ADDR 2 = 0

Data Bus Bit Interpretation:

B7 In Flip-Flop (0 = Reset, 1 = Set)

B6 Always 0

B5 Always 0

B4 Always 0

B3 Always 0

B2 Always 0

B1 Always 0

B0 Out Flip-Flop (0 = Reset, 1 = Set)

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
H	ADDR 11
G	ADDR 10
F	ADDR 9
X	ADDR 8
X	ADDR 7
X	ADDR 6
X	ADDR 5
E	ADDR 4
X	ADDR 3
0	ADDR 2
1	ADDR 1
1	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.4 Module Bus Pin Assignments

Function Performed: Set/Reset Command Flip-Flops (Input Operation)	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (HGFE)	X	ADDR 12
Address determined by	H	ADDR 11
Jumpers H, G, F, and E	G	ADDR 10
Jumper Out = 1 Jumper In = 0	F	ADDR 9
	X	ADDR 8
Function Specifier:	X	ADDR 7
	X	ADDR 6
	X	ADDR 5
A2 A1 A0	E	ADDR 4
0 1 0 Output Pulse	X	ADDR 3
1 0 0 Reset Out flip-flop	A2	ADDR 2
1 0 1 Reset In flip-flop	A1	ADDR 1
1 1 0 Set Out flip-flop	A0	ADDR 0
1 1 1 Set In flip-flop		
	B7	BUS 7
	B6	BUS 6
Data Bus Bit Interpretation:	B5	BUS 5
	B4	BUS 4
B7 Always 0	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
B6 Always 0	B0	BUS 0
	1=Logical 1=Bus Low	
B5 Always 0	0=Logical 0=Bus High	
	X=Don't Care	
B4 Always 0		
B3 Always 0		
B2 Always 0		
B1 Always 0		
B0 Always 0		

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), component location diagram (figure 3), and parts lists (02640-60031) located in the appendix.

The Terminal Duplex Register Module is very flexible and with jumper selection can provide many functions. The module can perform output only, input only, or input/output. It can be configured for either positive or negative logic (with processor inversion of data). If a minimum amount of status is needed, the status lines can be used for data input if desired. If DATA OUT and DATA IN lines are tied together, a bidirectional bus can be implemented. The Terminal Duplex Register Module consists of bus decoder logic, an address comparator, control logic, an output register, an input register and status, and a strobe generator.

3.1 BUS DECODER LOGIC.

3.1.1 The bus decoder logic receives the bus control inputs and the module address compare input and creates the internal signals which control the functions of the module. This logic decodes one output command ($\overline{\text{OUTPUT}}$) and eight input commands or functions.

3.1.2 The bus decoder logic decodes bus control inputs $\overline{\text{I/O}}$, $\overline{\text{WRITE}}$, $\overline{\text{REQ}}$, bus address information ($\overline{\text{ADDR2}}$, $\overline{\text{ADDR1}}$, and $\overline{\text{ADDR0}}$), and the module address equal (ADDR=) signal from the address comparator block. In addition, it generates internal control signals $\overline{\text{OUTPUT}}$, INPUT STATUS, $\overline{\text{INPUT DATA}}$, and various control functions ($\overline{\text{STROBE TRIGGER}}$, the set and reset commands of the flip-flops, and read Command F-F Status).

3.1.2.1 Two 4-input NAND gates (U35) decode the bus signals, thus determining the direction of data flow. The $\overline{\text{OUTPUT}}$ (U35, Pin 8) signal clocks data from $\overline{\text{BUS0}}$ through $\overline{\text{BUS7}}$ into the output register (U18 and U28) on the positive edge of the pulse. If Jumper C is in, the $\overline{\text{OUTPUT}}$ signal also sets the Out flip-flop at U26, Pin 4. The $\overline{\text{INPUT}}$ signal at U35, Pin 6 enables the 1-of-8 decoder (U34) to determine which input function will be active.

3.1.2.2 If $\overline{\text{INPUT}}$ is low, $\overline{\text{ADDR2}}$, $\overline{\text{ADDR1}}$, and $\overline{\text{ADDR0}}$ determine which command is decoded. $\overline{\text{INPUT DATA}}$ (U34, Pin 9), $\overline{\text{INPUT STATUS}}$ (U34, Pin 7), and $\overline{\text{CMD FF STATUS}}$ (U34, Pin 11) are inverted and control open-collector buffers which gate the information onto the terminal bus. The other input commands $\overline{\text{STROBE TRIGGER}}$ (Pin 10), $\overline{\text{RESET OUT FF}}$ (Pin 12), $\overline{\text{RESET IN FF}}$ (Pin 13), $\overline{\text{SET OUT FF}}$ (Pin 14), and $\overline{\text{SET IN FF}}$ (Pin 15), gate no information to the bus, and therefore, a byte of all "0" 's will be input.

3.2 ADDRESS COMPARATOR.

3.2.1 The address comparator determines if $\overline{\text{ADDR11}}$, $\overline{\text{ADDR10}}$, $\overline{\text{ADDR9}}$, and $\overline{\text{ADDR4}}$ on the data bus match the module address selected by four jumpers on the module. The Address Equal (ADDR=) signal from the address comparator enables the bus decoder logic to select the input/output commands for the Terminal Duplex Register Module.

3.2.2 Four open-collector exclusive OR gates (U14) act as the comparator for $\overline{\text{ADDR11}}$, $\overline{\text{ADDR10}}$, $\overline{\text{ADDR9}}$, and $\overline{\text{ADDR4}}$. If an address compare exists, ADDR= will be true (high) at U14, Pins 3, 6, 8, and 11. ADDR= is combined with $\overline{\text{WRITE}}$, $\overline{\text{I/O}}$, and $\overline{\text{REQ}}$ to enable module commands. Module Jumpers E, F, G, and H control the module address configuration for $\overline{\text{ADDR4}}$, $\overline{\text{ADDR9}}$, $\overline{\text{ADDR10}}$, $\overline{\text{ADDR11}}$ respectively. A jumper in represents a logic 0 for that module address bit. (Refer to the jumper summary in table 4.0.)

3.3 CONTROL LOGIC.

3.3.1 The control logic consists of two command flip-flops (In and Out), gates which control set and resetting of these flip-flops, and gates which select logic polarities for control.

3.3.2 The In flip-flop and Out flip-flop are used to control the flow of data between the Terminal Duplex Register Module and the device it is controlling. Each flip-flop can be set and reset by the bus commands and can also be reset by the controlled device. The two command flip-flops are controlled separately allowing simultaneous input and output operations.

3.3.2.1 The In flip-flop (U26, Pin 9) is associated with the input register. The J-K flip-flop is reset by PWR ON (U24, Pin 6) and can be set/reset by input commands, or reset by DEVICE IN (P2, Pin 2). Jumper J on the module selects whether a high (jumper out) or low (jumper in) at P2, Pin 2 resets the In flip-flop with the K input at U26, Pin 12. Jumper L selects the logic polarity of COMMAND IN (P2, Pin 1). If Jumper L is in, then COMMAND IN will be high when the In flip-flop is set. If Jumper L is out, then COMMAND IN will be low when the In flip-flop is set. The In flip-flop is used to clock data (DATA IN CLK) into the input register (U18 and U28) when it makes a transition from on to off.

3.3.2.2 The Out flip-flop (U26, Pin 5) is associated with the output register. The J-K flip-flop is reset by PWR ON and can be set/reset by input commands, reset by DEVICE OUT (P2, Pin B), or set with an $\overline{\text{OUTPUT}}$ command if Jumper C is in. Jumper K on the module selects whether a high (jumper out) or low (jumper in) at P2, Pin B resets the Out flip-flop with the K input at U26, Pin 2. Jumper M selects the logic polarity of COMMAND OUT (P2, Pin A). If Jumper M is in then COMMAND OUT will be high when the Out flip-flop is set. If Jumper M is out, then COMMAND OUT will be low when the Out flip-flop is set. If Jumper N is in, the Out flip-flop controls the output register buffers allowing a bidirectional open-collector bus.

3.3.2.3 One of the input commands, $\overline{\text{CMD FF STATUS}}$ (U34, Pin 11) enables the In and Out flip-flops to be read as status. Open-collector buffers (U25, Pins 3 and 11) gate the In flip-flop to $\overline{\text{BUS7}}$ and the Out flip-flop to $\overline{\text{BUS0}}$ when a $\overline{\text{CMD FF STATUS}}$ command is decoded by the bus decoder logic.

3.4 OUTPUT REGISTER.

3.4.1 The output register consists of two 4-bit D flip-flops (U18 and U28). The output data comes from the data bus and is clocked into the output register when an output command is decoded.

3.4.2 The output register receives an 8-bit byte from the bus and sends it out on the interface through open-collector buffers (U19 and U29). The Data Out signals are negative true and the buffers can be optionally controlled by the Out flip-flop allowing a bidirectional input/output bus configuration.

3.4.2.1 The two 4-bit D flip-flop registers are clocked on the positive edge of DATA OUT CLOCK at U36, Pin 2. They take the negative true signals from the terminal bus ($\overline{BUS0}$ through $\overline{BUS7}$) and invert them by using the complemented output of the D flip-flops. This preserves positive logic on the PCA. The registers are all reset to "1" at power on.

3.4.2.2 The open-collector buffers each have a pull-up resistor of 1K to +5 volts. Each buffer is capable of sinking 24 milliampers at 0.5 volts (low) or sourcing 2 milliamperes at +3 volts (high). The buffers can be controlled by the Out flip-flop if Jumper N is in.

3.5 INPUT REGISTER AND STATUS.

3.5.1 The input register latches eight data bits ($\overline{DATA\ IN\ 0}$ to $\overline{DATA\ IN\ 7}$ from the P2 connector. Each input bit has a pull-up resistor which can be biased by a jumper to either +5 volts or ground. The status bits are not latched and are available by an input command.

3.5.2 The input register (U39 and U49) and the Status In signals are the two input methods. Data In signals are clocked into the registers by an on-to-off transition of the In flip-flop and may be read thereafter by an Input Data command (see table 6.2). The status is not latched and is read directly to the bus.

3.5.2.1 The input register is made up of two 4-bit D flip-flops. Data is clocked into the input register by a positive edge on the DATA IN CLK, which is the complemented output of the In flip-flop. Inputs from the interface connector (P2) go directly to the D flip-flops. Each input has a 1K pull-up resistor, which can be connected to +5 volts (Jumper B in) or ground (Jumper A in). Jumpers A and B cannot be in simultaneously, otherwise a short from +5 volts to ground will exist. This feature allows a bias of less than +5 volts to be placed on the input lines if a resistor divider or Zener diode is used in Jumper A and B locations. The outputs of the D flip-flop register go to open-collector buffers (U38 and U48) which are enabled by the INPUT DATA command at U36, Pin 4.

3.5.2.2 The eight status input bits go directly to bus driving buffers (U58 and U59) which are enabled by INPUT STATUS at U36, Pin 6. Bits 1 and 0 go through Schmitt gates (U37, Pins 8 and 11) which invert the status polarity. Each status input bit has a 1K pull-up to +5 volts.

3.6 STROBE GENERATOR.

3.6.1 The strobe generator provides a 1-microsecond output pulse when triggered. This signal can be used to clock output or input data as necessary, or can be used as an interface clear function.

3.6.2 The pulse can be selected to be either negative or positive by Jumpers P and Q. If a pulse is not needed, another jumper allows +5 volts to be connected to the pulse output pin (to supply power or indicate power on).

3.6.2.1 The strobe is generated by a one-shot (monostable) function (U23) which is triggered by the negative edge of $\overline{\text{STROBE TRIGGER}}$ at U34, Pin 10. Two output buffers (U17, Pin 3 and 6) are connected to the outputs of the one-shot. Insertion of Jumper P or Jumper Q causes the PCA to provide a negative or a positive pulse, respectively.

3.6.2.2 If a one-shot function is not needed STROBE can be jumpered to +5 volts with Jumper R. Only one of the Jumpers P, Q, or R can be in at one time, otherwise damage to the PCA may occur. The +5 volts can be used for a power on indicator at P2, Pin S.

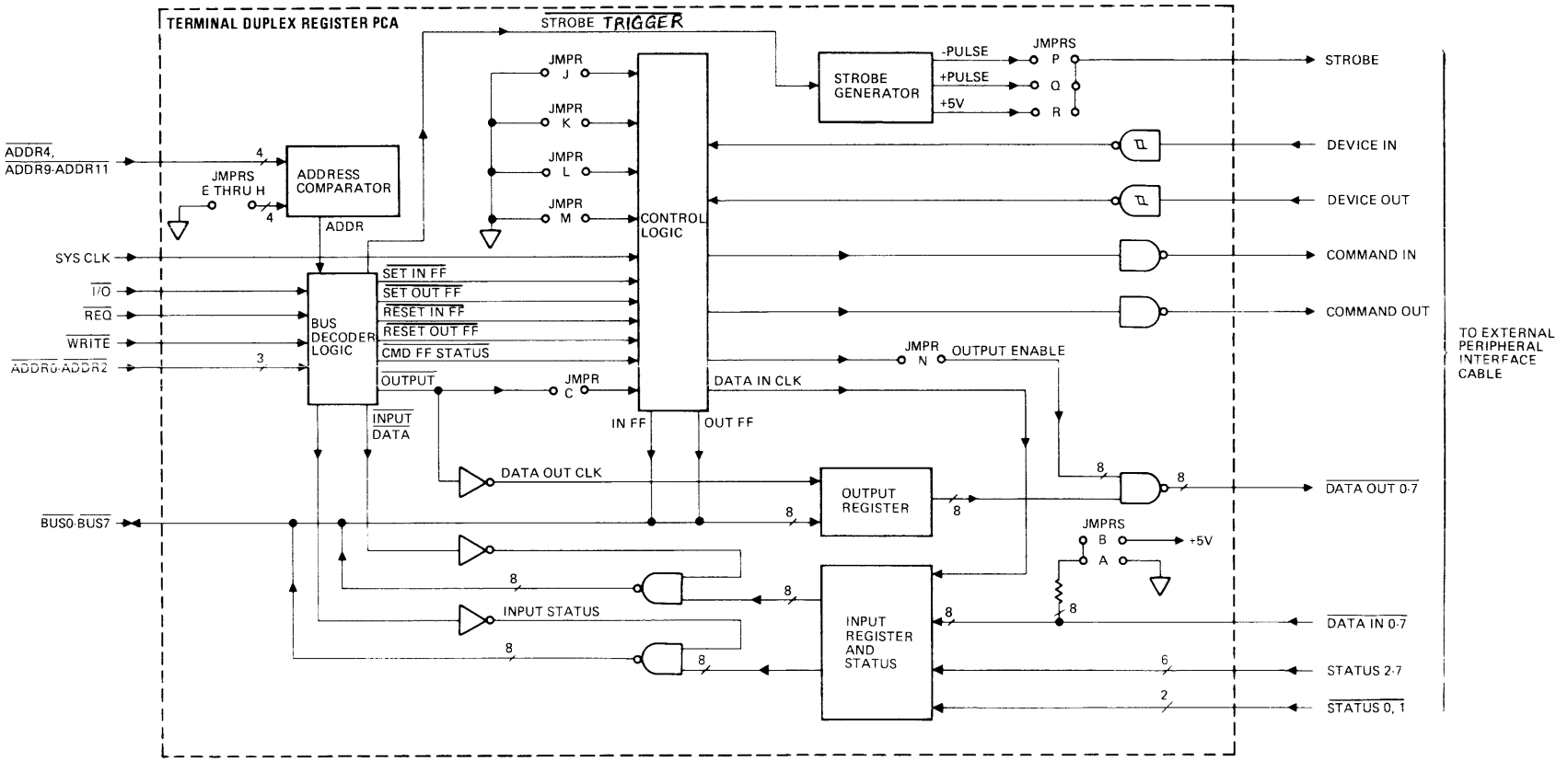
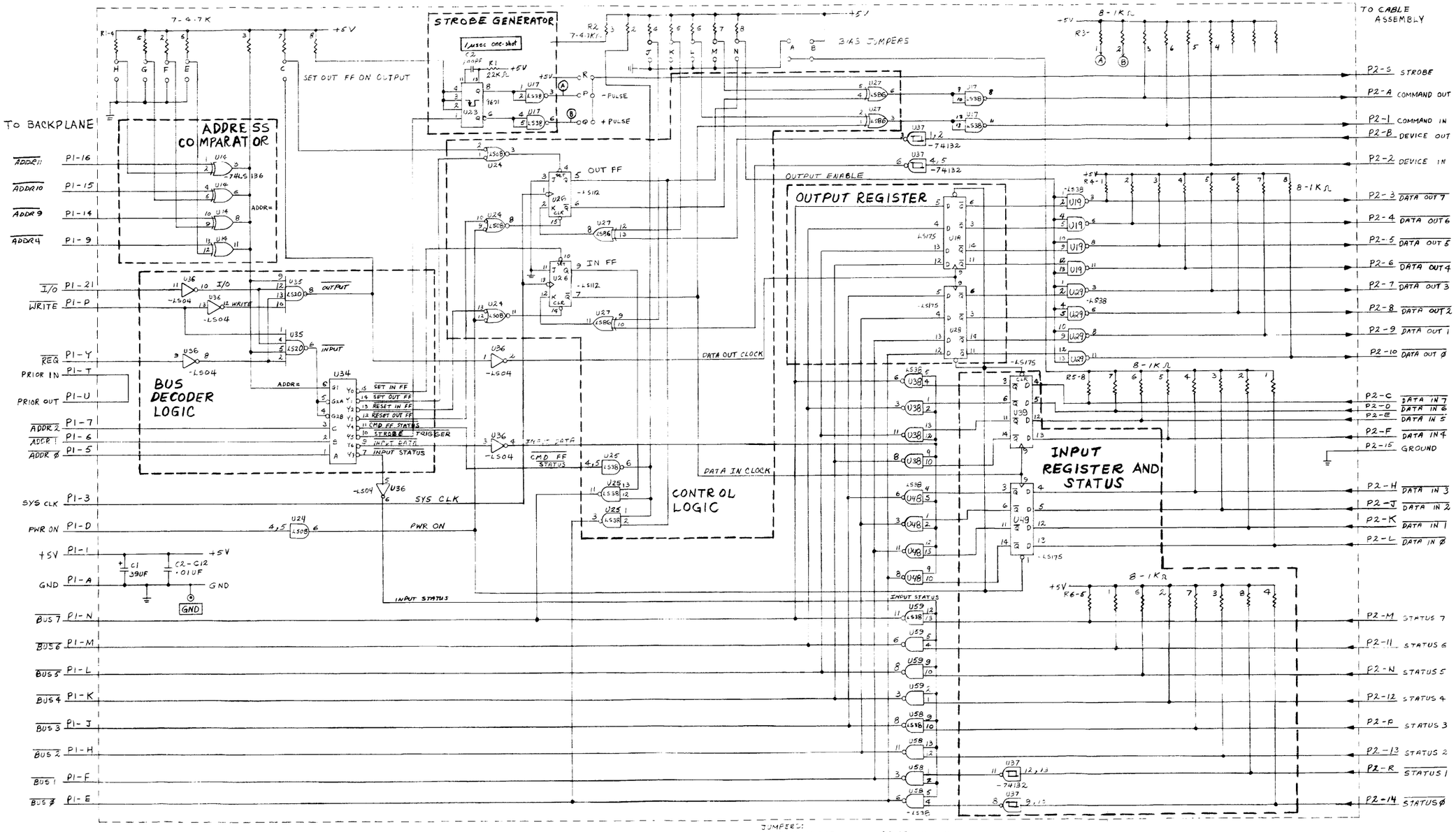


Figure 1
Terminal Duplex Register Block Diagram
APR-14-78 13255-91031

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60031	1	TERMINAL DUPLEX REGISTER ASSEMBLY DATE CODE: A-1448-22 REVISION DATE: 04-15-76	28480	02640-60031
C1	0180-0393	1	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0160-2204	1	CAPACITOR-FXD 100PF +-5% 300WVDC MICA	28480	0160-2204
C3	0160-2055	10	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C4	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C5	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C6	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C7	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C8	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C9	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C10	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C11	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
E1	0360-0124	1	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
R1	1810-0125	2	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R2	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R3	1810-0121	4	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R4	1810-0121		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R5	1810-0121		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R6	1810-0121		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R7	0683-2235	1	RESISTOR 22K 5% .25W FC TC=-400/+800	01121	CB2235
U14	1820-1215	1	IC-DIGITAL SN74LS136N TTL LS QUAD 2	01295	SN74LS136N
U17	1820-1209	8	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U18	1820-1195	4	IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U19	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U23	1820-0207	1	IC-DIGITAL 9601PC TTL MONOSTBL	07263	9601PC
U24	1820-1201	1	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U25	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U26	1820-1212	1	IC-DIGITAL SN74LS112N TTL LS DUAL	01295	SN74LS112N
U27	1820-1211	1	IC-DIGITAL SN74LS86N TTL LS QUAD 2	01295	SN74LS86N
U28	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U29	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U34	1820-1216	1	IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
U35	1820-1204	1	IC-DIGITAL SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
U36	1820-1199	1	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U37	1820-1056	1	IC-DIGITAL SN74132N TTL QUAD 2 NAND	01295	SN74132N
U38	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U39	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U48	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U49	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U58	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U59	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
W1	1200-0482	2	SOCKET-IC 16-CONT DIP-SLDR	91506	516-AG11D
W2	1200-0482		SOCKET-IC 16-CONT DIP-SLDR	91506	516-AG11D



JUMPERS: BUS - I/O ADDRESS

CABLE & JUMPER SPEC. DETERMINE INTERFACE TYPE.

H	MODULE ADDR 11	SELECT	(OUT = 1)
G	MODULE ADDR 10	SELECT	(OUT = 1)
F	MODULE ADDR 9	SELECT	(OUT = 1)
E	MODULE ADDR 4	SELECT	(OUT = 1)

JUMPER: C → IN = SET OUT FF ON DATA OUT COMMAND

JUMPER: *A & B — ALLOW BIAS VOLTAGE SET WITH DISCRETE COMPONENTS - OR -
A IN = R-pack R5 pin 9 = Ground
B IN = R-pack = +5
*A & B cannot both be IN

JUMPERS: P, Q, R (or - OFF IN)
P IN = SELECT - PULSE AT P2-S
Q IN = SELECT + PULSE AT P2-S
R IN = SELECT +5v AT P2-S

N IN = GATE DATA OUT ON OUT FF SET (ELSE ALWAYS GATED)

JUMPERS:
J IN = NEGATIVE TRUE RESET FOR IN-FF
K IN = " " " " FOR OUT-FF
L IN = POSITIVE TRUE COMMAND-IN
M IN = " " " - OUT

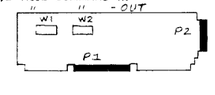


Figure 2
Terminal Duplex Register PCA Schematic Diagram
APR-14-78 13255-91031

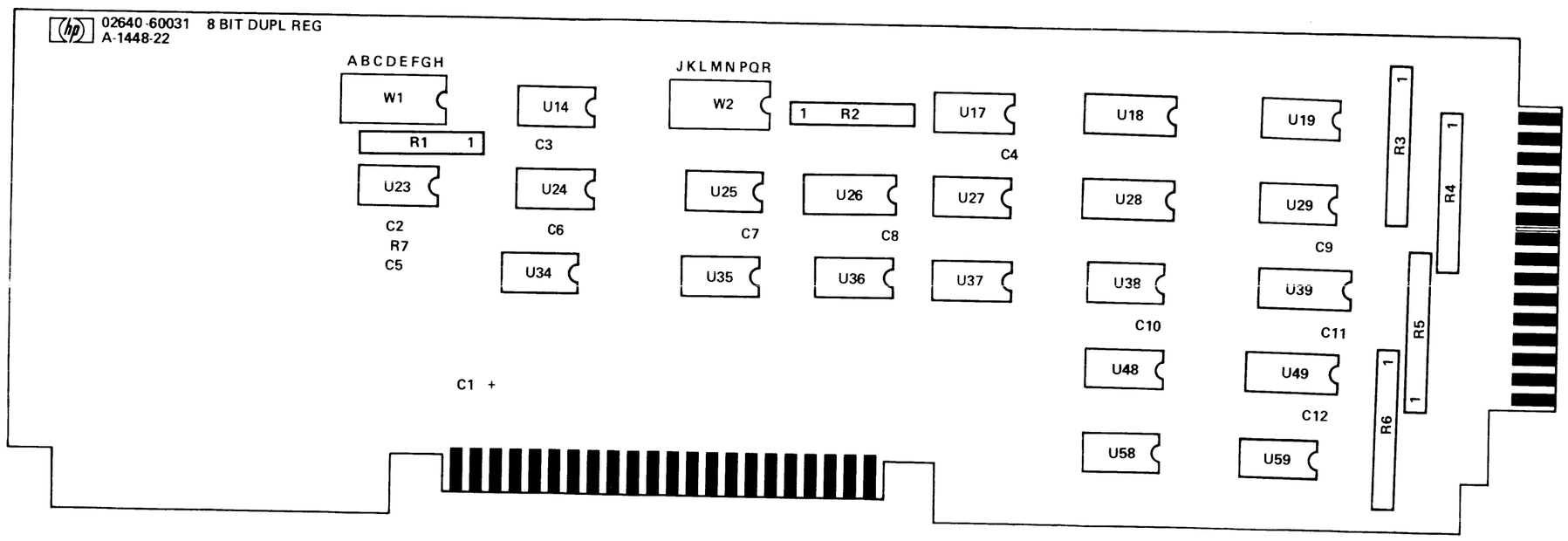


Figure 3
Terminal Duplex Register PCA
Component Location Diagram
APR-14-78 13255-91031