IBM Field Engineering

Theory of Operation

(Manual of Instruction)

Restricted Distribution

Specifications contained herein are subject to change without notice. Revisions and/or supplements to this publication will be issued periodically.

2415 Models 1-3 Tape Control

IBM®

Field Engineering

Theory of Operation

(Manual of Instruction)

Restricted Distribution

This manual is intended for internal use only and may not be used by other than IBM personnel without IBM's written permission.

Specifications contained herein are subject to change without notice. Revisions and/or supplements to this publication will be issued periodically.

2415 Models 1-3 Tape Control

PREFACE

This manual provides detailed descriptions of the functions and operations of the IBM 2415 Models 1-3 Tape Control, in addition to a general introduction to magnetic tape devices and tape control units. A theory of operation manual is intended primarily for instruction and as a classroom aid, not to provide maintenance and troubleshooting information. Complete servicing information is contained in the maintenance manual.

All figures in Chapters 2 and 3 are released as systems reference pages and are in the maintenance diagram volume shipped with each system. I/O operation (IOP) diagrams, referred to in Chapter 3, are contained in the diagram manual. Some figures in Chapter 4 are also released as systems reference pages. Refer to the preface of the diagram manual for a complete explanation of the type of diagrams available and how each group is released for the 2415 tape system.

It is assumed that the reader of this manual is familiar with the following texts, or has had equivalent experience:

Basic Computer System Principles -- Course Code 41077

Oscilloscope Operations -- Course Code 43014

SMS Component Circuits and Logic -- 1440 Preschool Part 3, Form R25-4967

System/360 I/O Interface -- Course Code 43140

Manuals that contain information relating directly to 2415 operations are:

Field Engineering Theory of Operation, IBM 2415 Models 1-6 Magnetic Tape Unit, Form Y22-2915

Field Engineering Maintenance Manual, IBM 2415 Models 1-6 Magnetic Tape Unit and Control, Form Y22-2916

Field Engineering Diagram Manual, IBM 2415 Models 1-6 Magnetic Tape Unit and Control, Form Y22-2917

Recent changes in terminology should be noted. The terms "block" and "interblock gap" (IBG) used in this manual are synonymous with the terms "record" and "inter-record gap" (IRG).

First Edition

This publication, Form Y22-2918-0, obsoletes Form Z22-2918-0. Major technical changes have been made in this publication, and it should be reviewed in its entirety.

Significant changes and additions to the specifications contained in this publication will be reported in subsequent revisions or FE Supplements.

This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. B95, PO Box 390, Poughkeepsie, N.Y. 12602. A form is provided at the back of this publication for the reader's comments. If the form has been removed, comments may be sent to the above address.

CONTENTS

CHAPTER 1. INTRODUCTION 1-1
Input/Output Devices 1-1
Magnetic Tape 1-1
Magnetic Tape Device 1-1
Control Unit 1-2
Channel 1-2
Data Format 1-3
Bit 1-3
Byte 1-3
Character 1-3
Parity Bit 1-3
Block 1-3
Interblock Gaps (IBG) 1-4
File 1-4
Skew 1-4
Check Characters 1-5
Check Character Parity 1-5
I/O Interface 1-7
Control Unit Priority 1-7
2415 Models 1, 2, and 3 Tape Control 1-7
NRZI System of Recording 1-9
Command Operations 1-10
Initial Selection 1-10
Begin Operation or Stack Status 1-11
Test I/O Operation 1-12
Short or Long Busy 1-12
Sense Operation 1-13
Tape Motion Control Commands 1-15
Write Operation 1-16
Read Operation 1-17
Read Backward Operation 1-17
End Status -- Burst Mode 1-17
End Status -- Request In Interrupt 1-18
Status Bits 1-18
Turnaround 1-19
Error Checking 1-19
CE Panel 1-21
Power Supply 1-21
Metering 1-21

CHAPTER 2. FUNCTIONAL UNITS 2-1
Metering and On-Line Gating 2-1
Metering Interface Lines 2-1
On-Line Latch 2-1
Select Signal Switching and Gating 2-1
Select Reed Relay (RR1) 2-2
Select Out Circuits 2-2
Addressing 2-2
Address Decoder 2-2
Address Generator 2-3
Tape Unit Decoding and Unit Free Gating 2-3
TU Address Compare 2-4
Device Register and Device End Scanner 2-4
Device (TU Address) Register 2-5
Device End (Unit Free) Scanner 2-5
Stop Scan 2-5
Unit Free Device End 2-6
Resets (Interface) 2-6
General Reset 2-6
Selective Reset 2-6
Interface Disconnect (Halt I/O and Stop Latch) 2-7
Resets (Tape Control) 2-7
Machine Reset 2-7
Sense Reset 2-8
Status Reset and Reset Arm 2-8
Early Reset 2-9
Idle Reset, and Green and Go 2-9
TAU Reset 2-9
Force Burst Mode (FBM) and Operational In 2-10
Command Register, Decoding, and Gating 2-11
Command Busy Latch 2-11
Command Gate Latch 2-11
Data Register (DR) 2-12
Data Register Parity Circuits 2-12
Data Register Inputs Outbound 2-13
Data Register Inputs Inbound 2-13
Data Register Outputs 2-14
Data Register Resets 2-14
Status Latches 2-14
Status Bytes 2-14
Status Latch Inputs 2-15
Delay Counter, Write Clock, and Sense Counter 2-15
Microsecond Mode 2-15
Millisecond Mode 2-16
Sense Counter 2-16
Counter Oscillators 2-16
Write Triggers and Deskewing 2-16
Writing a Bit on Tape (NRZI) 2-16
Deskewing Delay Counter 2-17
Writing Check Characters 2-17
Cyclic Redundancy Check Register 2-17
CRC Character Generation 2-17
Writing the CRC Character 2-18
Read Clock and Drive 2-18
First Bit Latch 2-19
Read Register 2-19
Register Outputs 2-19
Longitudinal Redundancy Check Register 2-19
Write LRCC 2-19
Read LRCC 2-20
Tape Mark Recognition 2-20
Seven-or Nine-Track Forward 2-20
Nine-Track Backward 2-21
Seven-Track Backward 2-21
Error Detection 2-22
Data or Equipment Check 2-22
Read Parity Check 2-22
Write Parity Check 2-22
Command Reject 2-23
Bus Out Check 2-23
Skew Error 2-23
Word Count 0 2-23
Counter Check 2-23
Interblock Gap Noise 2-24
Ready Drop 2-24
Overrun 2-24
Data Register VRC 2-24
Read Register VRC 2-24
Longitudinal Redundancy Check (LRC) 2-24
C-Compare Error 2-25

CHAPTER 3. PRINCIPLES OF OPERATION. 3-1
Initial Selection Sequence 3-1
Channel Addresses Tape Control 3-1
Address Selection 3-2
Command Set 3-3
Initial Status Byte 3-3
Begin Operation or Stack Status 3-3
Initial Status Bits and TAU Reset 3-4
Sense Operation 3-5
Read Forward Operation 3-5
Start Tape Motion 3-6
Time Read Delay 3-6
Read Data Block 3-6
Stop Read 3-6
Read Tape Mark 3-6
End of Block (EOB) Search 3-6
Read Backward Operation 3-7
Start Tape Motion 3-7
Time Read Delay 3-7
Read Check Characters and/or Tape Mark 3-7
Backward at Load Point 3-7
Read Data Block 3-8
Stop Read 3-8
EOB Search 3-8
Space or Space File Operations. 3-8
Forward Space or Space File 3-9
End Forward Space. 3-9
End Forward Space File 3-9
Backspace or Backspace File 3-10
End Backspace 3-10
End Backspace File 3-10
Write Operation 3-11
Start Tape Motion 3-11
Time Write Delay -- Request First Data. 3-11
Write Data Block 3-11
Stop Write 3-11
End of Block (EOB) Search 3-12
Write Tape Mark or Erase Gap 3-12
Begin Tape Motion and Time LP Delay 3-12
End Erase Gap 3-12
Write the Tape Mark 3-12
EOB Search 3-13
Rewind and Rewind-Unload. 3-13
Begin Operation 3-13
Rewind 3-13
Unit Free Device End. 3-13
Rewind at LP 3-14
Rewind-Unload 3-14
Unit Free after Rewind-Unload 3-14
End Status -- Burst Mode. 3-14
Operation 3-14
End Status -- Request In Interrupt. 3-15
Status Pending 3-15
Request In 3-15
Interrupt Address In 3-16
Interrupt Status In 3-16
Turnaround 3-16
Operation 3-16
Erase before Turnaround 3-16

CHAPTER 4. FEATURES 4-1
Seven-Track Operation 4-1
Data Conversion 4-1
Feature Functional Units 4-2
Mode Register 4-2
Translators 4-2
Byte Counter and Character Counter 4-4
Data Convert Theory of Operation. 4-5
Write Data Convert 4-5
Read Data Convert 4-6
Data Convert Check 4-7

CHAPTER 5. POWER SUPPLIES AND CONTROL 5-1
Power-On Sequence, Remote Operation. 5-1
Overload Control 5-1
Power Controls 5-2

CHAPTER 6. CONSOLE AND MAINTENANCE FEATURES . . 6-1
Section 1. Console 6-1
CE Panel Operation 6-1
Power Controls 6-1
Start, Stop, and Reset 6-1
On-Line and Off-Line. 6-2
Tape Unit Selection 6-2
Commands 6-2
Lamp Test 6-4
Bus Out 6-4
Check Stops. 6-4
Blocks. 6-4
Single Out Tag 6-4
Write Single Character 6-4
Parity Suppress 6-4
Section 2. Maintenance Features (explained in Section 1. Console)

APPENDIX A. UNIT CHARACTERISTICS A-1

APPENDIX B. SPECIAL CIRCUITS B-1
Final Amplifier and Clipping Level Control. B-1
Pulse Generation B-1
Clipping Voltage Levels B-1
Alternate Clipping. B-1

INDEX X-1

CHAPTER 1. INTRODUCTION

Figure	Title	Manual Page
1-1	Control Unit -- System Relationship	1-2
1-2	Blocks and Gaps	1-4
1-3	Write Skew (Exaggerated)	1-5
1-4	Tape Data Format	1-6
1-5	Input/Output Interface Lines, System/360	1-8
1-6	Control Unit Priority Wiring	1-9
1-7	IBM 2415 Tape System	1-10
1-8	NRZI Method of Recording	1-10
1-9	Command Codes	1-11
1-10	Channel Interface Tag Line Sequences	1-12
1-11	Initial Selection Interface Sequence	1-13
1-12	Sense Bytes	1-14
1-13	Status Bits	1-18
1-14	Error Conditions (NRZI Operation)	1-19

CHAPTER 2. FUNCTIONAL UNITS

Figure	Title	Systems* Page
2-1	Metering and On-Line Controls	00.21.01.1
2-2	Select Signal Gating, Delay, and Wiring	00.21.02.1
2-3	Address Decoder and Generator	00.21.03.1
2-4	Tape Unit Address Decode, Selection, and Unit Free Gating	00.21.04.1
2-5	Device Register and Device End Scanner	00.21.05.1
2-6	Resets -- General, Selective, Machine, Sense, and Status	00.21.06.1
2-7	Stop Latch and Halt I/O	00.21.07.1
2-8	Early Reset	00.21.07.1
2-9	Idle Reset (Green and Go)	00.21.07.1
2-10	TAU Reset	00.21.08.1
2-11	Force Burst Mode and Operational In	00.21.09.1
2-12	Command Register, Decoder, and Gating	00.21.10.1
2-13	Bus Out Parity Check and Bus In P-Bit Injection	00.21.09.1
2-14	Data Register Position 7, Input/Output Gating	00.21.11.1
2-15	Data Register Resets	00.21.12.1
2-16	Status Latches	00.21.13.1
2-17	Delay Counter, Write Clock, Sense Counter, and Drive	00.21.14.1
2-18	Write Deskewing and Write Triggers	00.21.15.1
2-19	Cyclic Redundancy Check Register (CRCR)	00.21.16.1
2-20	Read Clock, Drive, and First-Bit Latch	00.21.17.1
2-21	Data Time and Tape Mark Detection	00.21.18.1
2-22	Command Reject	00.31.01.1
2-23	Bus Out Check	00.31.01.1
2-24	Skew Error	00.31.01.1
2-25	Word Count 0	00.31.02.1
2-26	Counter Check	00.31.02.1
2-27	IBG Noise	00.31.02.1
2-28	Ready Drop	00.31.03.1
2-29	Overrun	00.31.03.1
2-30	Data Register VRC	00.31.04.1
2-31	Read Register VRC	00.31.05.1
2-32	LRCR Error	00.31.06.1
2-33	Data Convert Check (DCC)	00.31.06.1
2-34	C-Compare Error	00.31.07.1

CHAPTER 3. PRINCIPLES OF OPERATION

Figure	Title	Systems* Page
3-1	Short Busy or Bypass Select (Flow)	00.40.01.1
3-2	Initial Selection-Address Selection (Flow)	00.40.02.1
3-3	Initial Selection-Command Set, Status In (Flow)	00.40.03.1
3-4	Initial Selection Sequence (Timing)	00.40.04.1
3-5	Sense Operation (Flow)	00.40.10.1
3-6	Read Forward Operation (Flow)	00.41.01.1
3-7	Read Forward Sequence (Timing)	00.41.02.1
3-8	Read Backward Operation (Flow)	00.41.10.1
3-9	Read Backward Sequence (Timing)	00.41.11.1
3-10	Write Operation (Flow)	00.41.20.1
3-11	Write Sequence (Timing)	00.41.21.1
3-12	Forward Space Block/File (Flow)	00.41.30.1
3-13	Backspace Block/File (Flow)	00.41.40.1
3-14	Write Tape Mark or Erase Gap (Flow)	00.41.50.1
3-15	WTM and Erase Gap Sequence (Timing)	00.41.51.1
3-16	Rewind or Rewind-Unload (Flow)	00.40.20.1
3-17	End Status -- Burst Mode (Flow)	00.40.30.1
3-18	End Status -- Burst Mode (Timing)	00.40.31.1
3-19	End Status -- Request In Interrupt (Flow)	00.40.40.1
3-20	End Status -- Request In Interrupt (Timing)	00.40.41.1
3-21	Turnaround (Flow)	00.40.50.1

CHAPTER 4. FEATURES

Figure	Title	Systems* or Manual Page
4-1	Mode Register	00.27.01.1
4-2	Translators	00.27.02.1
4-3	Eight-Bit Code -- BCD Relationship	4-3
4-4	Byte and Character Counter	00.27.04.1
4-5	Data Convert Check (DCC)	4-7

CHAPTER 5. POWER SUPPLIES AND CONTROL

Figure	Title	Manual Page
5-1	Power Distribution and Sequence Control	5-3

CHAPTER 6. CONSOLE AND MAINTENANCE FEATURES

Figure	Title	Manual Page
6-1	IBM 2415 CE Panel	6-1
6-2	Functional Grouping of CE Panel Controls	6-2
6-3	Command Card Wiring	6-3

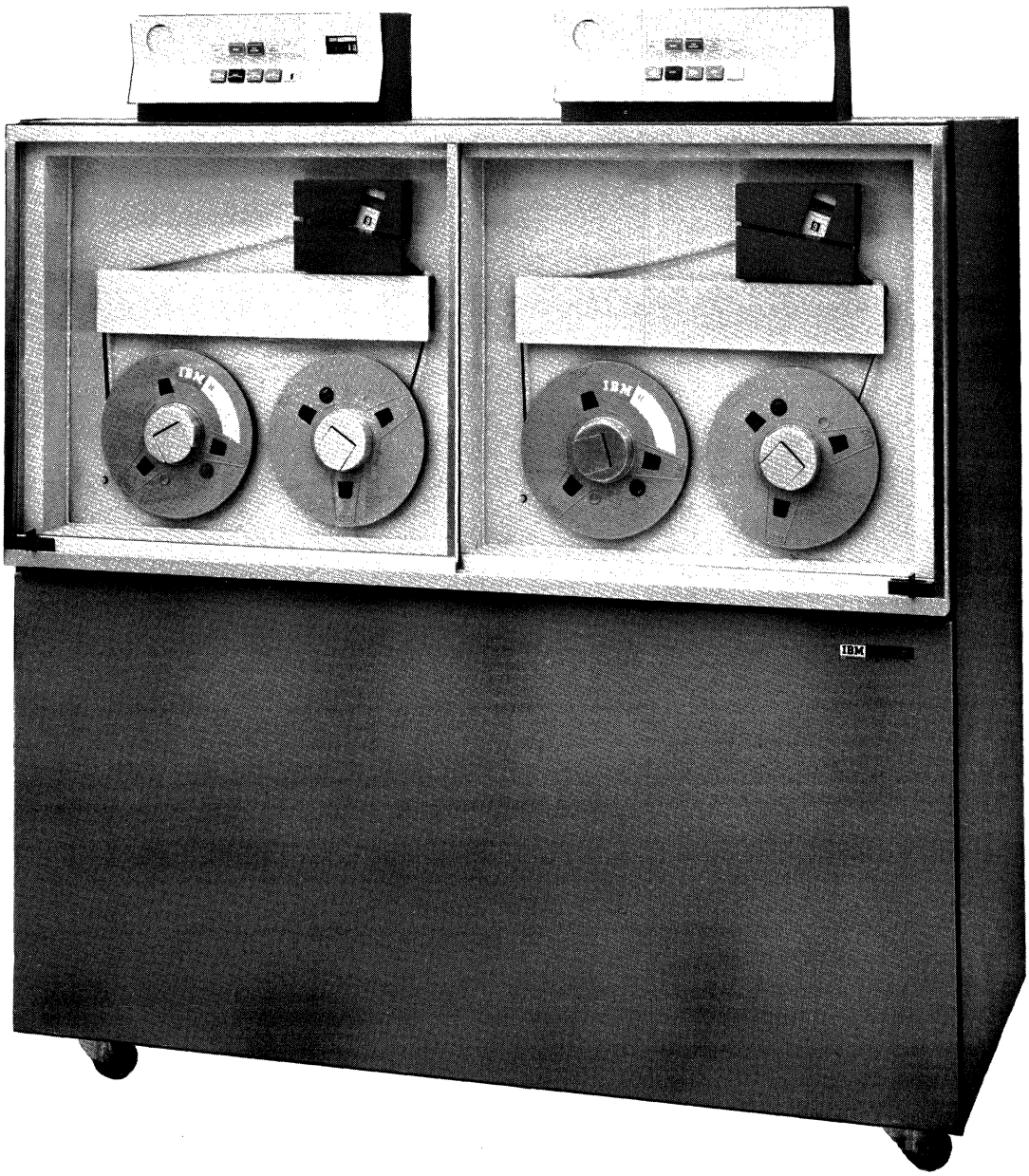
APPENDIX B. SPECIAL CIRCUITS

Figure	Title	Manual Page
B-1	Final Amplifier and Clip Level Control	B-2

* These figures are released as reference pages in the systems maintenance diagram volume that is shipped with each tape system.

ABBREVIATIONS

A	AND Circuit
ALD	Automated Logic Diagram
AND	AND Circuit
AR	Amplifier Circuit
BOB	Beginning of Block
BOT	Beginning of Tape (Load Point)
bpi	Bytes per Inch
CCW	Counterclockwise
CE	Customer Engineer
CRCC	Cyclic Redundancy Check Character
CRCR	Cyclic Redundancy Check Register
CU	Control Unit
CW	Clockwise
DC	Data Converter or Delay Counter
DR	Data Register
EOB	End of Block
EOT	End of Tape (Tape Indicate)
FF	Flip-Flop Circuit
FL	Flip-Latch Circuit
FP	File Protect
I	Inverter
IBG	Interblock Gap
I/O	Input/Output
ips	Inches per Second
LP	Load Point
LRCC	Longitudinal Redundancy Check Character
LRCR	Longitudinal Redundancy Check Register
ma	Milliampere
mill	1/1000 Inch
ms	Millisecond
mv	Millivolt
N	Inverter
NRZI	Non-Return to Zero IBM
O	OR Circuit
OE	Exclusive OR Circuit
OR	OR Circuit
P (bit)	Parity Bit
PE	Phase Encode
RC	Read Clock
RIC	Read In Clock
ROC	Read Out Control
RR	Read Register
R/W	Read/Write
SKB	Skew Buffer
SLD	Simplified Logic Diagram
TAU	Tape Adapter Unit
TB	Binary Trigger
TC	Tape Control
TI	Tape Indicate
TM	Tape Mark
Triac	Triode AC Switch (Semiconductor)
TU	Tape Unit
usec	Microsecond
v	Volt
VRC	Vertical Redundancy Check
WC	Write Clock
WTM	Write Tape Mark



IBM 2415 MODEL 1 OR 4 MAGNETIC TAPE UNIT AND CONTROL

INPUT/OUTPUT DEVICES

IBM Data Processing Systems include input/output devices, control units, channels, storage units, and central processors, although they vary widely in size, complexity, speed, and application. Input/output devices enter information into the system (input) and record information generated by the system (output).

Typical input devices sense or read data information stored on media such as punch cards, magnetic tape, paper tape, printed forms, or printed copy. The same types of media are used in typical output devices to record or write data information. Some devices operate as either an input or output device.

Magnetic tape is used extensively as an input/output medium because it rapidly stores large amounts of data in compact, easily handled form. Data stored (written) on magnetic tape may be retained as permanent recordings that can be reread repeatedly without destroying the recorded information, or as temporary recordings that are erased automatically as new data is written on tape.

Magnetic Tape

- Magnetic tape consists of a long plastic strip coated with a ferromagnetic material.
- Some types of tape are designed to provide superior wear characteristics and greater reliability.
- The width and thickness of tape are generally determined by the type of magnetic tape device on which the tape is used.
- Magnetic tape is supplied on reels for ease of handling.

Magnetic tape consists of a long, flexible, and continuous strip of plastic (the base) coated with a layer of ferromagnetic material dispersed in a suitable binder (the coating). There are two kinds of 1/2-inch wide magnetic tape in general use: IBM DYNEXCEL tape (formerly heavy duty (HD) tape) and Mylar* tape. DYNEXCEL tape provides greater reliability of performance as an input/output medium. Both kinds of tape use a polyethelene plastic base. The composition of the ferromagentic coating determines the color and wear characteristics of the tape. Due to the materials used in the coating, heavy duty tape wears better than Mylar tape and withstands higher temperature during storage.

* Trademark of E.I. DuPont deNemours & Co., Inc.

For ease of handling, magnetic tape is wound on reels similar to those used with conventional home tape recorders. Reel sizes vary according to the type of tape and magnetic tape device on which it is used.

Each reel of magnetic tape contains physical markers to designate the useful or data area portion. The extreme ends of the tape are not usable because some tape must remain on the reels during use. Tape markers that are sensed photoelectrically by the magnetic tape device usually consist of reflective foil stickers. (Refer to Chapter 1 of Field Engineering Theory of Operation, IBM 2415 Models 1-6 Magnetic Tape Unit, Form Y22-2915 for a detailed description of magnetic tape and the method of recording.

Magnetic Tape Device

- A magnetic tape device is the means by which data is actually written on and read from magnetic tape.
- Data is written on tape in separate longitudinal rows called tracks.
- A separate read and write head reads and writes data in each track.
- All read and write heads are packaged in one read/write head assembly.
- Other essential functions of a magnetic tape device, referred to as a tape unit, are tape and reel motion control.
- Most tape unit operations are timed and controlled externally.

A magnetic tape device is the machine that is used as an input device to read data from magnetic tape and as an output device to write data on magnetic tape. A magnetic tape device is most commonly referred to as a tape unit.

Data is recorded on magnetic tape in longitudinal rows called tracks. These tracks are similar to the rows on a punched card. A tape unit has one write head and one read head for each tape track. The read and write heads for all tracks are in a single unit called a read/write head assembly. When reading (input), the tape unit moves tape across the read/write head assembly so that the read heads sense information, previously written on the coated

surface of the tape, as a series of pulses. When writing (output), the tape unit moves tape across the read/write head assembly so that the write heads record new data on the coated surface of the tape by magnetizing the surface coating of each track.

In addition to reading and writing data and moving tape at a fixed speed, a tape unit must also sense tape limits, rewind tape, and control the motion of tape reels. Due to the physical nature of tape movement and control, a magnetic tape unit is, of necessity, an electromechanical device that operates slower than an electronic device. Before data can be written on tape, for example, the tape unit requires a period of delay from the time it is ordered to write, while the tape builds up speed. Tape requires hundreds of microseconds to attain operating speed; whereas, electronic devices, such as a central processor, operate in the nanosecond (thousandths of a microsecond) range.

Control Unit

- Central control of the operation of more than one input/output (I/O) device is more efficient and economical.
- A tape control unit is an all-electronic device that controls several tape units.
- The tape control is entirely responsible for the proper control of all system operations on any attached tape unit.
- The tape control must select a unit, control its movement, time its operations, and monitor conditions such as status and errors.
- A tape control is the only communications link between a tape unit and the external system.
- Control units communicate with the computer system through I/O channels.

A few tape unit functions are controlled automatically by essential circuitry within the device, but most unit functions are controlled externally. One set of timing and control circuits, operating several tape units, is more economical than duplicate control circuitry in each tape unit. A single set of electronic control circuits, used to control multiple I/O devices of the same type, is packaged in a device called a control unit.

A magnetic tape control unit is referred to as a tape control; some of the major functions of a tape control are:

1. Selecting (addressing) a specific tape unit.
2. Initiating the proper status conditions for specific operations.
3. Timing delays before and after writing or reading.
4. Timing of data transfer to and from the computer system input/output control.
5. Controlling the beginning and end of tape motion.
6. Monitoring of tape limit signals, error conditions, tape unit malfunctions, etc.

All system communications with a tape unit, including the flow of data, pass through the tape control (Figure 1-1). However, if the computer system has to communicate directly with all of its control units, system operation is delayed needlessly. A central control, called a channel, usually external to the system central processor, directs all I/O operations.

Channel

- The channel is a separate electronic device that frees the processor from the task of controlling I/O operations.
- The control program in the computer system initiates all I/O operations by issuing instructions to the channel.
- The channel initiates operations by issuing commands to a control unit.

A channel is designed to free the computer system from the time-consuming task of controlling I/O operations; this includes selecting specific control units and I/O devices, initiating operations, and the buffering of data flow to and from the system main storage. (Buffering is the accumulation and temporary storage of groups of data to reduce the number of data transfers required of the system storage.) By relieving the central processor from the task of direct control of I/O, data processing can proceed concurrently with I/O operations.

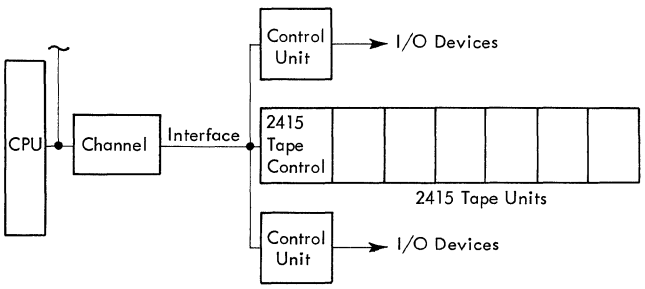


FIGURE 1-1. CONTROL UNIT -- SYSTEM RELATIONSHIP

DATA FORMAT

Bit

- A bit is the smallest unit of information.
- A bit is a binary 1 when it represents an active condition.
- A bit is a binary 0 when it represents an inactive condition.

The smallest unit of information in a data processing system is called a bit. Each bit represents either an active or inactive condition, such as the on or off state of a bistable device (latch). A bit becomes a binary 1 when it represents the on or active condition. A bit becomes a binary 0 when it represents the off or inactive condition.

Byte

- Bits are combined into groups called bytes.
- A byte contains 8 data bits.
- A ninth bit is added for parity checking.

Serial transmission of individual bits between devices, and within devices, is time consuming and inefficient, so groups of eight bits are combined to form bytes. An eight-bit byte can represent a special code, character, letter, or number, whose configuration is determined by the CPU.

Bits or bit positions in a register are designated 0-7.

If a particular character or code is represented by the active state of the four- and seven-bit positions of a byte, the byte would have a 1 bit in positions 4 and 7, and 0 bits in the other six positions. The four- and seven-bit signal lines have active levels; whereas, the remaining lines have inactive levels (on voltage or current signal lines).

A ninth bit is added to a byte for parity checking as the byte is moved from one set of circuits to another. See "Parity Bit."

Character

- A character is a group of six data bits.
- A seventh bit (check bit) is added for parity checking.
- Characters are used for seven-track feature operations only.

Basic 2415 operations utilize the byte on nine-track tape units. When installed as a feature, seven-track tape units can be used to provide compatibility with the tape format of earlier model tape systems. A smaller group of bits for feature operation, called a character, contains six data bits. A seventh bit, called a check (C) bit, is added for parity checking. Refer to Chapter 4 for feature data flow.

Parity Bit

- A parity (P) bit is added to each byte as a means of error checking.
- The total number of binary 1 bits in a byte (data bits and parity bit combined) is always odd for odd parity.
- A character also contains a parity (check) bit.
- The total number of binary 1 bits in a character (data and C bits) is always odd or even, depending on the format designated by the system program.

A parity bit is an additional bit that is added to each byte, or character, as a means of error checking the data. For odd parity, the binary state of the parity bit (1 or 0) is such that there is always an odd number of 1 bits in each byte, or character, including the parity bit.

For example, if a byte contains bits 01101001 (0-7), the parity bit is 1 to give a total of five 1 bits 101101001 (P, 0-7). If a character contains the bits 101100, the check bit is 0 for a total of three 1 bits 0101100. For an even parity character, the binary state of the check bit is such that there is always an even number of 1 bits in each character, including the check bit.

Block

- A group of bytes (or characters) is called a block.
- The amount of data in a tape block (number of bytes or characters) is variable.
- Byte spacing in a block is determined by tape control oscillators and tape speed.
- Tape blocks are separated by gaps of erased tape.

All bits in a byte (or character) are transferred in parallel to the selected tape unit. When data bytes are written on magnetic tape, each byte is written perpendicular to the horizontal edge of tape. Each

bit of a byte is written simultaneously (ideal condition) in separate tracks on tape. A separate group of related bytes, such as all of the information punched in an 80-column card, is called a block. Refer to Field Engineering Theory of Operation, IBM 2415 Models 1-6 Magnetic Tape Unit, Form Y22-2915, for a detailed description of writing on tape. Tape blocks are separated by erased areas of tape (Figure 1-2).

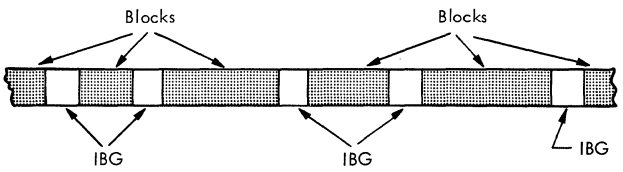


FIGURE 1-2. BLOCKS AND GAPS

Interblock Gaps (IBG)

- An interblock gap is the erased area between two blocks.
- The gap between blocks is generated by tape unit mechanical inertia and tape control and tape unit delay timings.
- A start delay is timed before writing or reading.
- A stop delay is timed after writing or reading.
- Write start and stop delays create the interblock gaps between blocks.
- Groups of related blocks are usually separated by a tape mark.

The gap or blank area of erased tape between blocks is the result of mechanical limitations in the tape unit. Because tape cannot start or stop instantaneously, a period of time (in milliseconds) is required to accelerate tape to full speed or to stop tape after the end of a block.

When end of block is reached, the tape unit "go" signal is dropped to stop movement. However, inertia moves the tape well past the write heads before motion stops. The tape control must make allowance for tape unit limitations by appropriate delay timings, although the tape unit times most of the stop delay.

A command to write another data block starts tape motion again. Bytes are written too close together unless tape is at full speed, so the tape control unit delays transmission of bytes to the tape unit. The start delay time for write operations (while the tape accelerates) is called write delay (or read delay for read type operations).

A gap between blocks on tape represents the total length of tape movement created by the write stop time of one block and the write (start) delay time of the following block. Start-stop times (mechanical), which are adjustable in the tape unit, have a direct bearing on the length of the gap. If tape unit mechanical start and stop times are changed, the length of the resulting gaps are also changed.

Short stop times tend to create shorter gaps. Quick acceleration tends to create longer gaps. When a tape unit gets up to full speed quicker, tape travels a greater distance during write delay time. The normal gap between blocks (Figure 1-2) is 0.6 inch long for nine-track tape units and 0.73 inch long for seven-track tape units. The blocks can be closer in nine-track because nine-track tape unit read/write heads are constructed with a closer spacing between the read and write heads.

File

- A file is a group of blocks.
- Files are separated by tape marks.
- The number of blocks in a file is determined by the CPU program.

A file, as recorded on the tape, is a group of blocks separated by a special block called a tape mark. The number of blocks in a file is variable and is determined by the CPU program. By using tape marks between groups of related blocks, programs can determine when files begin and end.

Skew

- Skew is the misalignment of bits within a byte.
- Bits can be skewed during the writing and/or the reading process.
- Skew is generally mechanical or electrical.
- Mechanical skew is minimized by proper read/write head adjustment.
- Electrical write skew is minimized by adjustable delay taps in the tape control for each tape unit.
- Electrical read skew is minimized by adjustable delay taps in each tape unit.

During a write operation, pulses that comprise a byte are delayed (by preset adjustable delay taps)

to align bits, and these pulses are sent to the tape unit. Ideally, all bits of a byte should be perfectly aligned and should be detected (read) at the same instant as the byte passes over the read heads during a subsequent read operation. Unfortunately, this ideal condition is difficult to achieve due to write and read head manufacturing tolerances, small differences in head assembly adjustments between tape drives, and slight variations in circuit delays between bit tracks. These factors are further aggravated if a tape swerves slightly as it passes over the heads during the write operation or any subsequent read operation.

In the misalignment of bits within a byte, skew can mean a slanting or staggering of bits relative to the horizontal edge of tape. If skew is excessive, bits of adjacent bytes might mix and cause read errors. Figure 1-3 shows an exaggerated example of write skew. The example is called write skew because the bytes are actually written on tape with the bits misaligned. However, bits written on tape in perfect alignment can be skewed during the read operation. Read heads and/or read circuits can cause the bits to be misaligned electrically; that is, some bits are delayed longer than others.

Skew is generally mechanical or electrical. Mechanical skew is usually caused by misadjustment of the write head assembly on the write drive and/or the read head assembly on the read drive. Electrical skew is caused by head manufacturing tolerances and/or circuit delays. Mechanical skew is corrected by adjustment of the head assemblies on the tape unit on which a tape is written and the unit on which the same tape is read. Electrical skew is minimized by adjustable tape control write delay taps or tape unit read delay taps during maintenance.

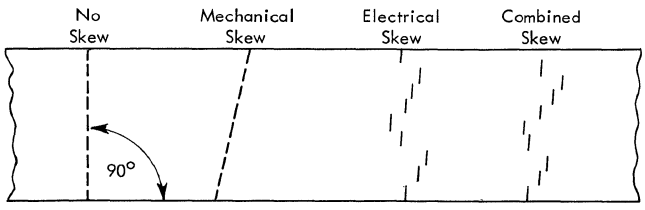


FIGURE 1-3. WRITE SKEW (EXAGGERATED)

Check Characters

- The standard nine-track format contains data followed by two check characters: a CRCC and an LRCC.
- The seven-track format contains data followed by one check character, an LRCC.

The standard nine-track format writes two check characters at the end of each block (Figure 1-4). The first check character is the cyclic redundancy check character (CRCC), and the second check character is a longitudinal redundancy check character (LRCC).

The CRCC is a character developed in the CRC register in the tape control. This character, during each nine-track write operation, represents an accumulation of all the bits in the block. The CRCC is written on tape four byte spaces after the last data byte. (The CRCC is written to create compatible tapes for 2400-series tape systems, which use the CRCC for single bit read error correction.)

The second check character (LRCC) is an odd/even parity count of all the bits in each track of a block. The total number of bits in any track of a block is made an even number by placing a 1 or 0 in the LRCC position. The second check character is written four byte spaces after the CRCC, or a total of eight spaces from the last data byte. The nine-track LRCC represents the same odd/even bit count as the LRCC used in seven-track operations. Since the CRCC is written before the LRCC, the CRCC bits are included in the odd/even LRCC count. Each track must have an even number of bits in each block. For a seven-track operation, only one check character (the LRCC) is written.

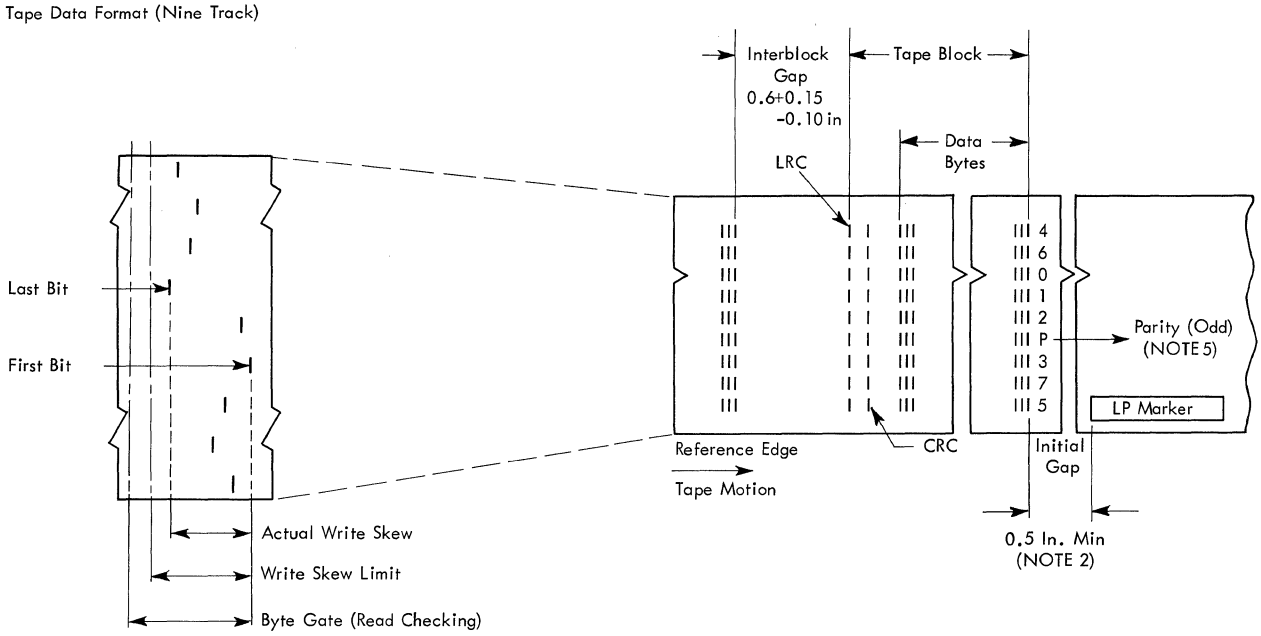
The LRCC in a seven-track operation is written four character spaces after the last data character (Figure 1-4). The seven-track format meets the same specifications as the format used on other IBM tape systems, such as the IBM 729 or 7330 Magnetic Tape Units.

Check Character Parity

- Nine-track LRC character is always odd parity.
- Seven-track LRC character and nine-track CRC character can be odd or even parity.
- CRC character contains an odd number of bits if there is an even number of data characters.
- CRC character contains an even number of bits if there is an odd number of data characters.

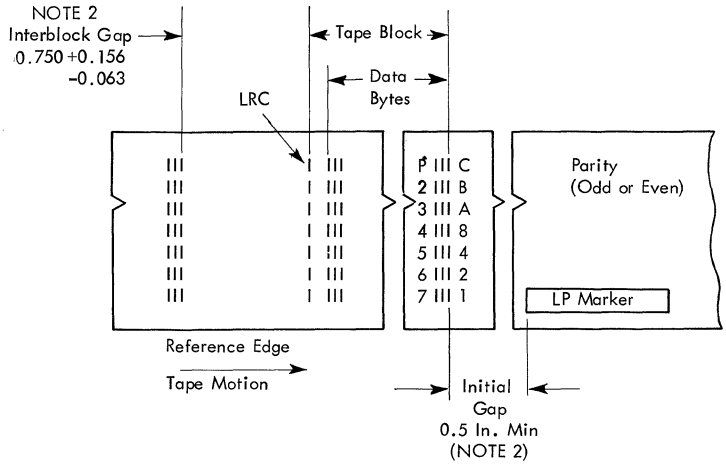
During nine-track operations, the LRCC always contains an odd number of bits. Thus, the vertical redundancy of a nine-track LRCC is always odd. However, the vertical redundancy (number of bits in the character) of the nine-track CRCC can be an odd or even number. As a general rule, the vertical redundancy of the CRCC is an even number if the total number of data bytes in the entire block is an odd number. Likewise, if the total amount of data bytes

Tape Data Format (Nine Track)



NOTES: 1. Tape is shown with oxide side down. NRZI recording. Bit produced by reversal of flux polarity. Tape fully saturated in each direction.
2. Tape to be fully saturated in the erased direction in the initial gap and the inter-record gap. Erasure such that an N seeking end of compass will point to start of tape.
3. CRC - Cyclic redundancy check character. Parity of CRC character is determined by the number of data characters in record. Odd number of data characters-even CRC character, etc. CRC used only in System/360 800 bpi. CRC character spaced four bits from data characters.
4. LRC - Longitudinal redundancy check character - always odd parity. Spaced four bits from CRC.
5. Parity Bit - A vertical parity bit is written for each character containing an even number of bits.

Tape Data Format (Seven Track)



NOTES: 1. Tape is shown with oxide side down. NRZI recording. Bit produced by reversal of flux polarity. Tape fully saturated in each direction.
2. Tape to be fully saturated in the erased direction in the initial gap and the inter-record gap. Erasure such that an N seeking end of compass will point to start of tape.
3. LRC - Longitudinal redundancy check character - odd or even-spaced four bits from data character.
4. Parity Bit - A vertical parity bit is written for each character.

FIGURE 1-4. TAPE DATA FORMAT

in the block is an even number, the vertical redundancy of the CRCC is odd. A nine-track LRCC always contains an odd number of bits; the CRCC may be odd or even, depending on the number of data bytes within the block. The seven-track data format may contain either an odd or even number of bits in the LRC character. This is possible because seven-track operations may employ odd or even redundancy when handling data bytes. The following considerations apply to the redundancy of the seven-track LRCC:

1. Using even redundancy mode always produces an LRCC that contains an even number of bits, regardless of the number of data bytes in the block.
2. When using odd redundancy mode, the number of bits in the LRCC is odd if there is an odd number of data bytes, or the number of bits in the LRCC is even if there is an even number of data bytes in the block.

I/O INTERFACE

- The I/O interface establishes requirements for communication between the channel and control units.
- The I/O interface uses 34 lines.
- The I/O interface specifies the function of the interface lines and the sequence in which the lines are used.

The I/O interface is a set of established requirements for uniform signal transfers between a channel and all control units. The interface uses 34 lines and specifies the signal sequence and information format transferred on the lines. (The reader should be familiar with the contents of Systems Reference Library, IBM System/360 I/O Interface -- Channel to Control Unit, Original Equipment Manufacturers' Information (OEMI), Form A22-6843.) Interface lines are grouped by function (Figure 1-5). The following is a brief review of the functions of each group.

Bus Out Lines transmit information (data, I/O device address, commands, and control orders) from the channel to the control unit.

Bus In Lines transmit information (data, selected I/O device identification, status information, and sense data) from the control unit to the channel.

Tag Lines interlock and control information on the buses and are used for special sequences.

Selection Controls are used for the selection and scanning of I/O control units and attached I/O devices.

Metering Controls condition usage meters in the various attached control units and I/O devices.

CONTROL UNIT PRIORITY

- Control unit priority is determined by internal select signal wiring and physical connections to the interface signal cables.
- Interface priority is the order in which control units are selected if more than one unit requires channel service.
- The select signal leaves the channel as select out, but it may reach some control units as select in.
- When the select signal reaches a control unit for which the signal is not intended, the signal must be propagated to the next lower priority control unit.

The select out and select in lines form a series loop from and to the channel through all attached control units (Figure 1-6). The select out line is jumpered to the select in line in the terminator block located at the tail gate of the control unit which is physically the farthest unit from the channel on the interface cable hookup. Electrical priority is established by wiring within each control unit when the system is installed.

The higher priority control units are wired in series with the select out line from the channel; the lower priority units are wired in series with the select in return line to the channel. The highest priority unit is the first unit which receives the select (out) signal; the lowest priority unit returns the select (in) signal directly to the channel.

The select signal sequence is such that a control unit must propagate the select signal to the next lower priority unit, when selection is not required. That is, when a control unit that does not need service (or is not addressed) receives the select signal, it must regenerate and pass on the select signal to the next control unit physically attached to the select out or select in line.

2415 MODELS 1, 2, AND 3 TAPE CONTROL

The IBM 2415 Tape Control is a control unit that operates as many as six tape units. The difference between Models 1, 2, and 3 is the number of tape units connected to the tape control (Figure 1-7). The

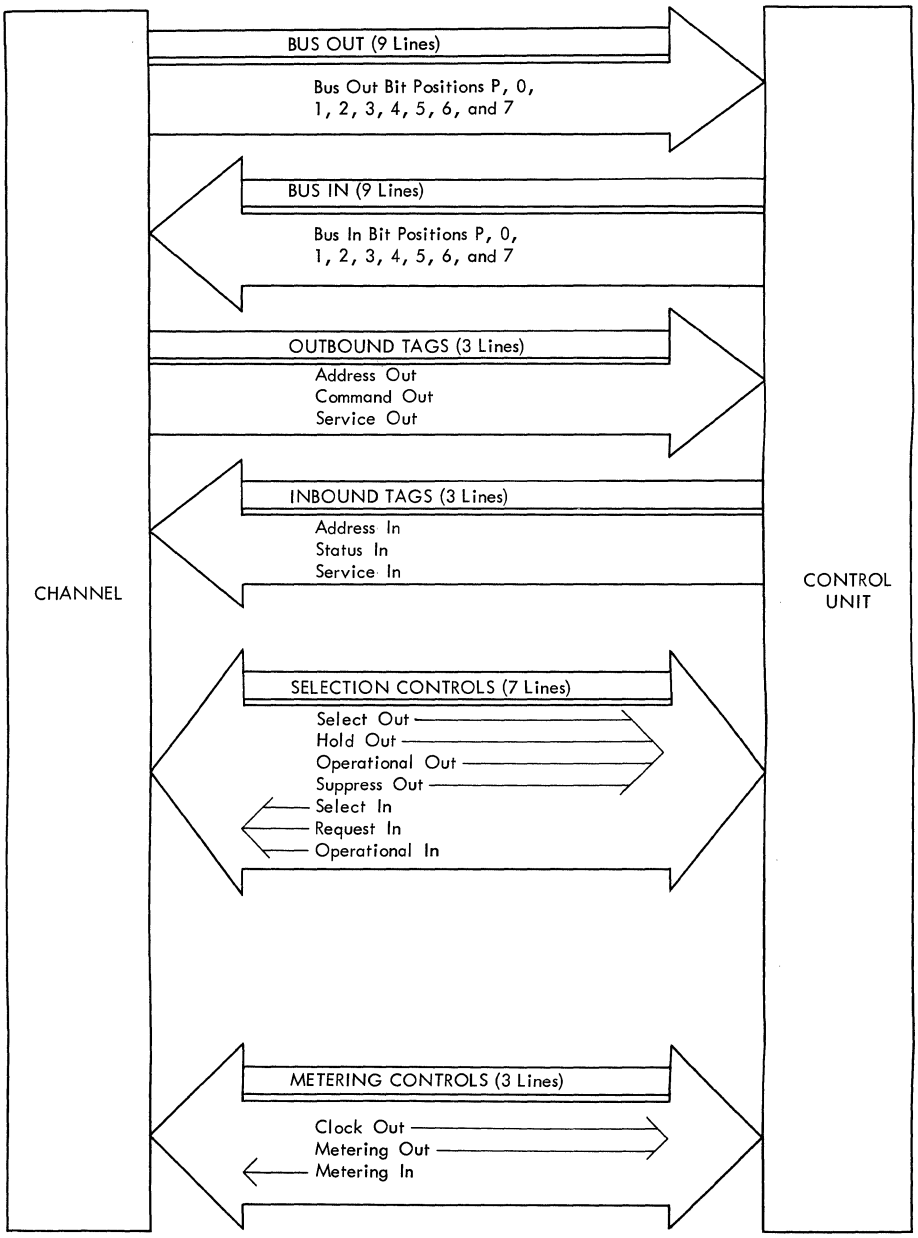


FIGURE 1-5. INPUT/OUTPUT INTERFACE LINES, SYSTEM/360

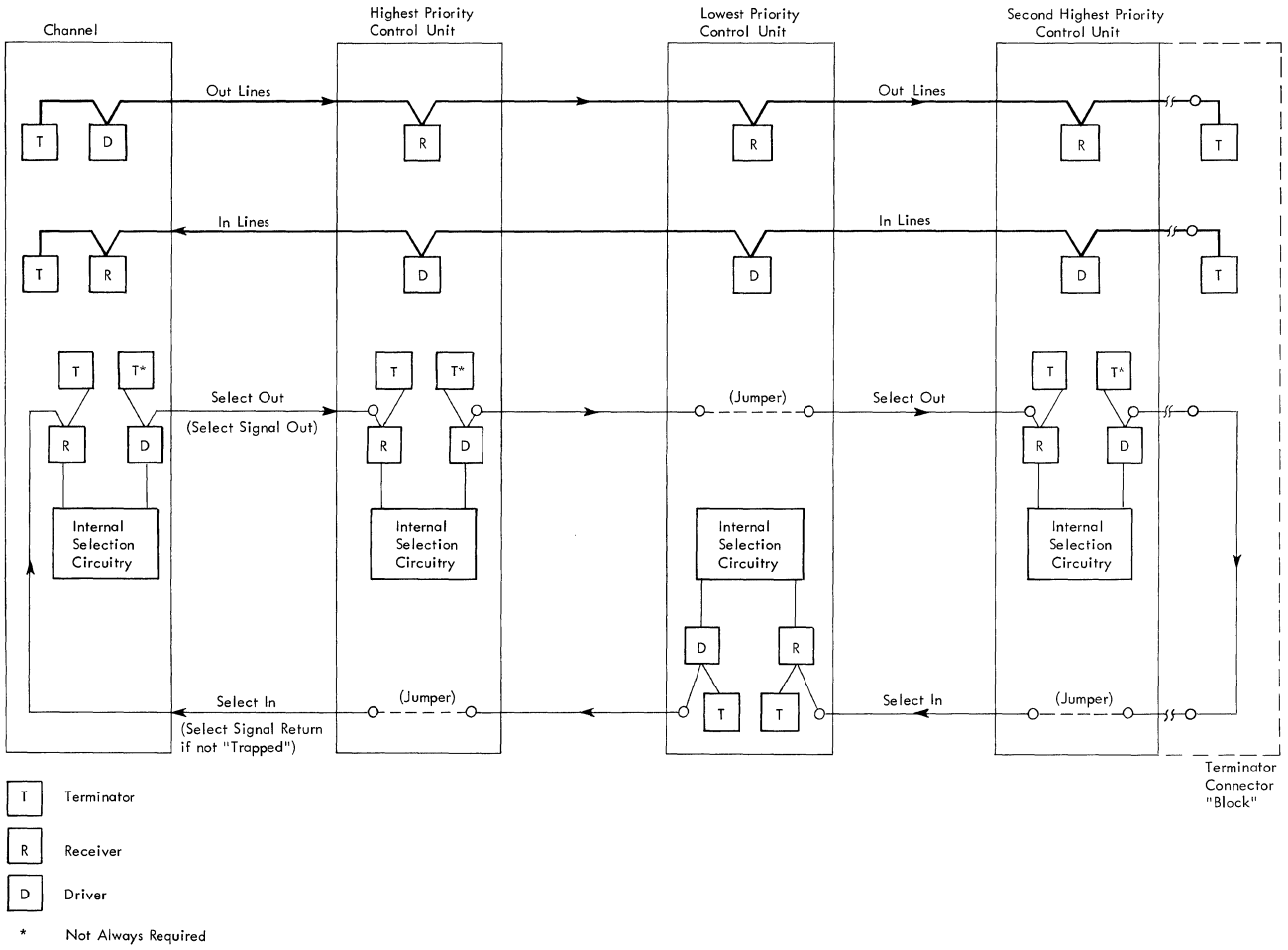


FIGURE 1-6. CONTROL UNIT PRIORITY WIRING

Models 4, 5, and 6 tape control differs from Models 1, 2, and 3 in that it uses a method of coding called phase encode; while Models 1, 2, and 3 use the NRZI system.)

NRZI System of Recording

- Polarity of tape is changed in either direction at a given time to record a 1 bit.
- Polarity of tape is not changed at a given time to record a 0 bit.

The NRZI system of recording information continuously polarizes magnetic tape; a logical 1 is recorded by changing the direction of polarization. A logical 1, then, is indicated by a change in the direction of polarization at a given time, while a logical 0 is indicated by no change in the direction of polarization at a given time. Refer to Chapter 4 of Field Engineering Theory of Operation, IBM 2415 Models 1-6 Magnetic Tape Unit, Form Y22-2915 for a description of how the magnetic pattern is created on tape.

Writing on Tape

The write current waveform, shown in Figure 1-8, is an example of the signal sent to a tape unit write head over the write bus; it represents the information in one recording track. The tape control generates a write current waveform for each track according to the byte information sent by the channel. (The bit pattern in Figure 1-8 represents single track information for nine successive bytes.) Note that a write current polarity change occurs only when a 1 bit is indicated, and the tape is magnetized accordingly.

Reading from Tape

When tape passes over the read heads during read or write operations, the magnetic flux patterns on tape cause read waveforms similar to the single read head signal shown in Figure 1-8. A pulse is generated only when a change in tape magnetic polarity passes the read head. (The write and read waveforms are shown together for a comparison of the results for the same bit pattern.)

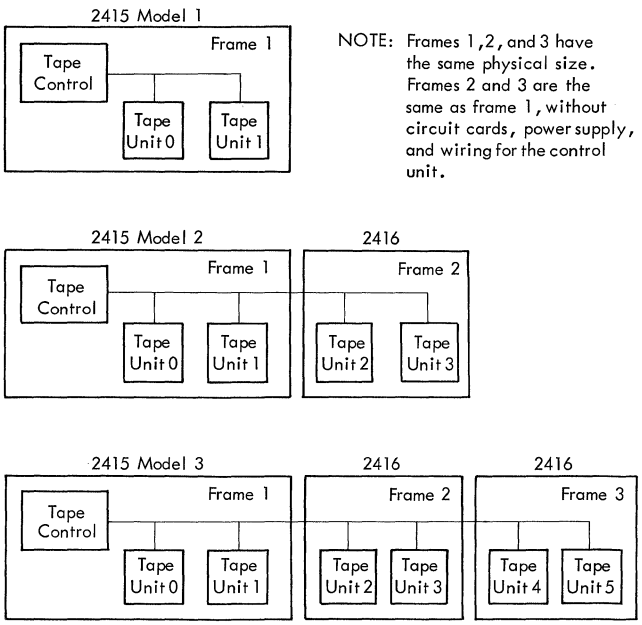
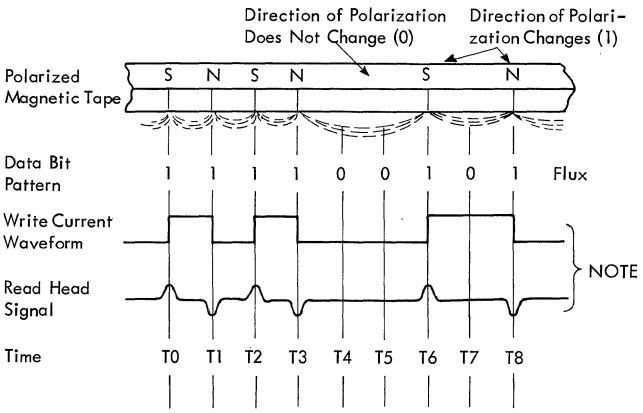


FIGURE 1-7. IBM 2415 TAPE SYSTEM



NOTE: Waveforms shown are for comparison only; these waveforms would be difficult to view together on an oscilloscope.

FIGURE 1-8. NRZI METHOD OF RECORDING

COMMAND OPERATIONS

All command operations are initiated by the channel with an initial selection sequence. During initial selection, a tape control and one tape unit are addressed, and a command is sent to the tape control. The tape control then responds with information about its status, indicating its ability to perform the command. The command (Figure 1-9) specifies which operation is to be performed.

Test I/O and non-motion control command (mode set) operations are completed during initial selection. All other operations are initiated when initial selection is completed. See Figure 1-10. A sense operation transfers information to the channel, but does not use the tape unit. Eight motion control command operations use the tape unit, but there is no data transfer between the tape control and the channel. Read, read backward, and write operations transfer data between the tape unit and the channel.

A detailed block diagram of over-all data flow and controls, Figure UDC-1, is contained in the diagram manual. Refer to Figure UDC-1 in conjunction with the following descriptions.

Initial Selection

- Initial selection is performed in three basic steps: address selection, command set, and status response.
- When the tape control decodes its address, it then decodes the tape unit address and selects one tape unit.
- Tape control traps the select out signal and sends the tape control-tape unit coded address byte back to the channel.
- Channel sends a command to the tape control.
- Tape control decodes the command and sends status information back to the channel to complete the initial selection sequence.

Address Selection

Address selection is initiated by the channel, which sends a coded address byte on bus out and the address out tag (Figure 1-11) to all tape controls in parallel. All attached control units attempt to decode the address. The channel then sends select out to the tape controls in series.

When a tape control decodes its own address, it then sets the tape unit address in the device register and decodes the address to select one of the tape units.

When the tape control address is decoded, the tape control traps the select out signal when it arrives (does not pass it on to the next tape control). The selected tape control now activates the operational in line to interlock itself to the channel. The complete address (tape control and tape unit) is then sent

Command	P	Bits 0	1	2	3	4	5	6	7
Test I/O	1	*	*	*	*	*	0	0	0
Sense		*	*	*	*	0	1	0	0
Read Backward		*	*	*	*	1	1	0	0
Write		*	*	*	*	*	*	0	1
Read		*	*	*	*	*	*	1	0
Control:		*	*	C	C	C	1	1	1
Rewind				0	0	0			
Rewind-Unload				0	0	1			
Erase Gap				0	1	0			
Write Tape Mark				0	1	1			
Backspace Block				1	0	0			
Backspace File				1	0	1			
Forward Space Block				1	1	0			
Forward Space File				1	1	1			
Mode 2 Set: 1,600 bpi (Set Phase Encode)		1	1	0	0	0	0	1	1
800 bpi (Set NRZI)		1	1	0	0	1	0	1	1
Mode 1 Set		D	D	M	M	M	0	1	1

2415 Models 4-6 Only

NOTES: * Can be 1 bit or 0 bit (if odd parity is maintained).
C Control command code.
D Density set.
M Mode modifier.
(1) Reset condition for TC with seven-track and data convert features.
(2) Reset condition for TC with seven-track feature without data convert feature.
(3) Not used. If used, no operation is result.

Density Set

Density	Bits 0	1
200 bpi	0	0
556 bpi	0	1
800 bpi	1	0

Mode Modifiers

	Bits 2	3	4	Set Density	Set Odd Parity	Set Even Parity	Turn On Data Converter	Turn Off Data Converter	Turn On Translator	Turn Off Translator
No Operation	0	0	0							
Diagnostic	0	0	1							
(1)	0	1	0	X	X		X			X
(3)	0	1	1							
	1	0	0	X		X		X		X
	1	0	1	X		X		X	X	
(2)	1	1	0	X	X			X		X
	1	1	1	X	X			X	X	

FIGURE 1-9. COMMAND CODES

back to the channel on the bus in lines for verification, and the complete address activates the address in tag to identify the information on the bus. Address selection is completed at this point.

Command Set

When the channel receives the combined address byte of the tape control and tape unit it has selected, it responds by sending a coded command on bus out and activates the command out tag.

The tape control checks the coded command for correct parity in the data register. If parity is good (odd), the byte is set in the command register and the command is decoded. See Figure UDC-1. The tape control now inspects the decoded command to determine whether or not the designated command can be performed.

Initial Status Response

The tape control completes the initial selection sequence by sending a status byte of information to the channel: tape control and tape unit status information is sent to the channel on bus in, and a status in tag is sent to the channel. The purpose of the initial status byte is to indicate to the channel the operational condition of the tape control and tape unit. If the tape control is not able to perform the command, the status byte indicates why the operation cannot be performed.

The initial status byte is normally empty (except for the P bit) for a read, write, or sense command. The byte contains a channel end status bit for a control command. Because a test I/O command is initiated to relieve the TC of pending status, it is not unusual for any particular status bits to be active during test I/O.

Begin Operation or Stack Status

- Channel response to status in allows the tape control to begin operation or causes the tape control to stack status.
- Service out response signals that the status byte is accepted; proceed with the command.
- Command out response signals that the status byte is rejected; store (stack) status byte and block initiation of any operation that requires channel use.

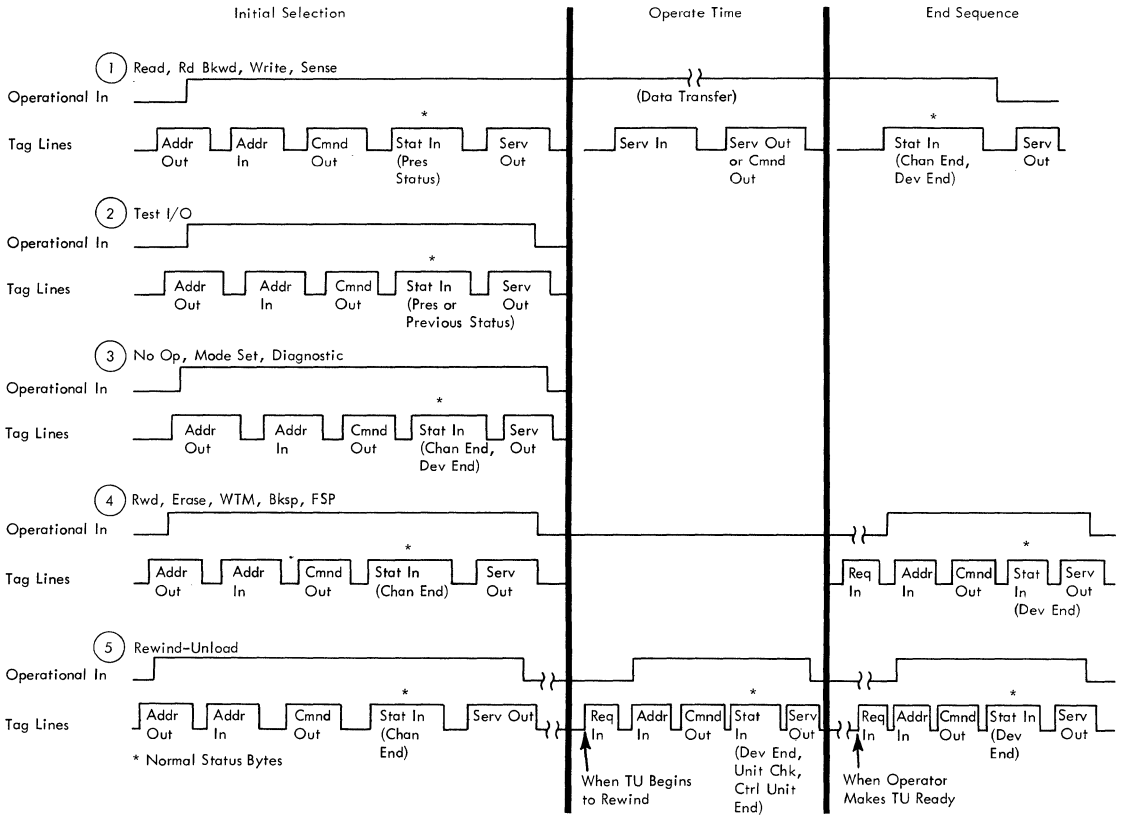


FIGURE 1-10. CHANNEL INTERFACE TAG LINE SEQUENCES

- Prohibitive status conditions in control or tape unit cause tape control to block performance of command at end of initial selection.

At the end of initial selection, the channel response to status in mainly determines tape control procedure. The channel can either accept or reject the status byte. However, in either case, the operation is not executed by the tape control if prohibitive status conditions exist (such as tape unit is busy) as determined by the tape control.

Service Out: This channel response to status in signals the tape control that the status byte was accepted; perform the command if status conditions allow. The tape control continues with read, write, or sense operations, or disconnects from the interface and continues with a control command.

If prohibitive status conditions exist, the tape control disconnects from the interface and blocks performance of the designated command.

Command Out: This channel response to status in signals the tape control to disconnect from the interface and:

1. Block initiation of and store (stack) status for operations that require use of the channel to complete the operation (read, write, or sense commands).
2. Perform the designated control command.

Test I/O Operation

A test I/O operation is performed to interrogate the tape control for status information and, therefore, is completed during initial selection. The test I/O operation is normally initiated by the channel to relieve the tape control of pending status for a previous operation.

The channel responds to the status in tag at the end of initial selection with service out. Gated with the decoded test I/O command, service out generates end test I/O which generates a reset, to reset the tape control.

Short or Long Busy

- Short busy indicates that the tape control is busy and attempted initial selection is terminated before an interface interlock is established.

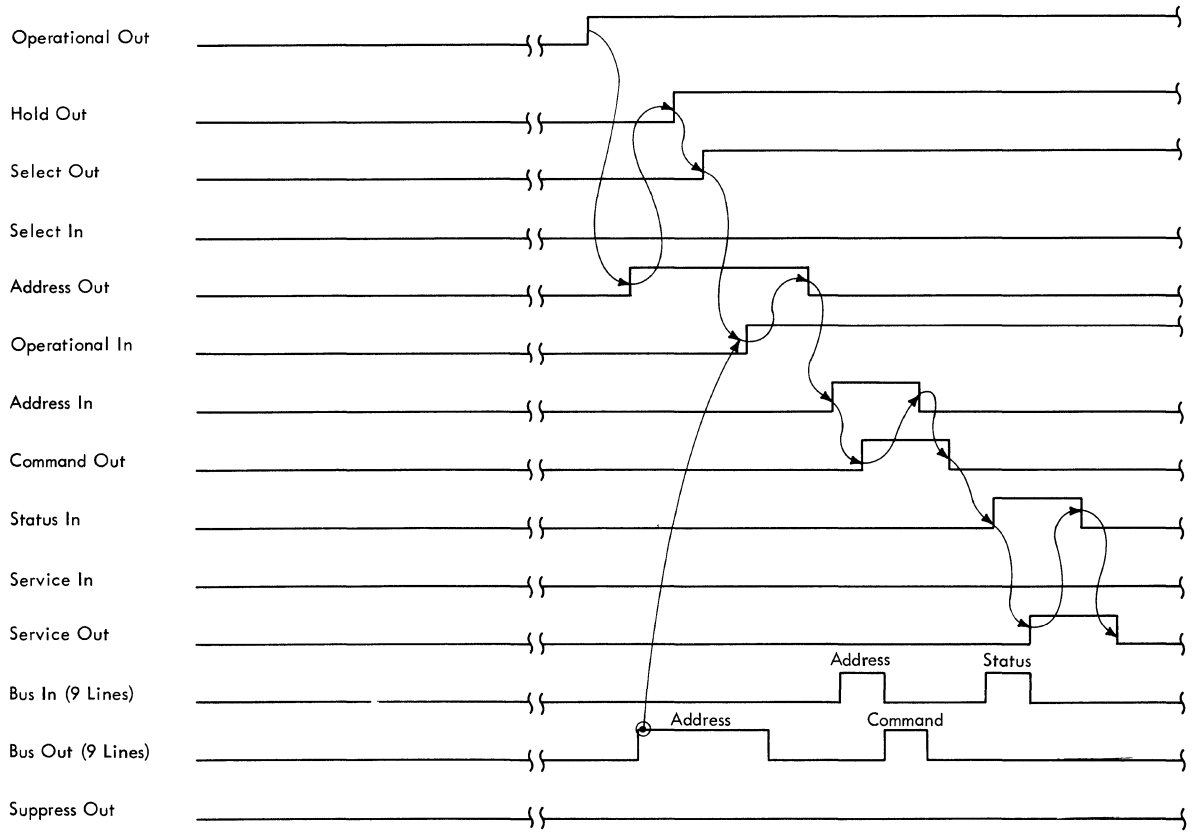


FIGURE 1-11. INITIAL SELECTION INTERFACE SEQUENCE

- Short busy generates a short busy status byte which is sent to the channel.

- Long busy indicates that the tape control has status pending for a previous operation on the selected tape unit.

- Initial selection is completed normally for long busy to send pending status to the channel, but the designated command is not performed.

Short Busy

When address decode is activated at the beginning of an attempted initial selection sequence, short busy is indicated if the tape control is:

1. Already performing a command, or
2. Status is pending for a TU address other than the TU address in the address byte.

In either case, the tape control places a status byte that contains a P, 1 (status modifier), and 3 (busy) bit directly on bus in when select out arrives; the status in tag is also forced. When the channel receives the short busy status byte instead of an address byte, it drops select out to terminate the attempted selection.

Long Busy

If the tape control is holding status for a previous operation for the same tape unit address designated in the address byte, initial selection proceeds but the designated command is not performed. The designated operation is blocked because old status and status associated with the new (intended) operation cannot be mixed; however, a busy bit is added to the existing status byte.

After the initial selection sequence is completed by a channel response to the status byte, the tape control disconnects from the interface. The long busy procedure has relieved the tape control of the pending status.

Sense Operation

- Detailed information about tape control and tape unit conditions is sent to the channel in groups of bits called sense bytes.

- Six sense bytes are sent to the channel during a complete sense operation.

- The last two sense bytes contain no information (all zeros).

- The channel can end the sense operation after receiving any number of sense bytes by initiating an early end.

A sense operation is performed to send sense information to the channel. Sense information is detailed information about the status of the tape control and the addressed tape unit, including error conditions. Sense information, stored in the tape control, is sent to the channel on the bus in lines in an operation similar to a read operation.

Sense Byte Format

Six sense bytes are sent to the channel during a complete sense operation (no early end). Each bit in a sense byte represents a condition of the tape control or the tape unit. Some bits are not used for the 2415 Tape Control, and always contain a 0 bit. Sense bytes 4 and 5 contain all-zero bits. The contents of all sense bits is illustrated in Figure 1-12.

Operation

At the end of initial selection, the channel sends service out to the tape control. The tape control then gates a byte of sense information (sense byte 0) to the data register, which places it on the bus in lines. The tape control then sends a service in tag to the channel to indicate that information is on the bus. When the channel has received a byte of sense information, it sends service out and the tape control sends the next byte.

Ending

When the tape control receives service out following the sending of the sixth sense byte (sense byte 5), it initiates a status in ending operation.

Byte	Bit	Condition
0	0	Command Reject
	1	Intervention Required
	2	Bus Out Check
	3	Equipment Check
	4	Data Check
	5	Overrun
	6	Word Count 0
	7	Data Converter Check
1	0	IBG Noise
	1	TU Status A
	2	TU Status B
	3	Seven Track
	4	Load Point
	5	Write Status
	6	File Protect
	7	
2	0	
	1	
	2	
	3	
	4	
	5	
	6	Forced Unconditionally
	7	
3	0	Data Register Check (VRC)
	1	LRCR Check
	2	Skew Check
	3	Read Register Check (VRC)
	4	Counter Check
	5	Backward at Load Point
	6	C-Compare Check
4		All Zeros
5		All Zeros

Bit 1	Bit 2	TU Status
0	0	Nonexistent
0	1	Not Ready
1	0	Ready and Not Rewinding
1	1	Ready and Rewinding

NOTE:

Sense information is reset by every start I/O except sense, no operation and test I/O.

FIGURE 1-12. SENSE BYTES

Early End

The channel initiates an early end if it does not want all six sense bytes. When the channel receives the last byte it wants, it responds to the next service in tag with command out instead of service out. The tape control then inhibits the remaining sense bytes and initiates a status in ending operation.

Tape Motion Control Commands

- Tape control disconnects from the channel at the beginning of the operation.
- Channel end is sent to the channel in the initial (selection) status byte.
- Operational in line is deactivated when the operation begins.
- Two types of tape motion control commands: rewinding and read/write.
- Tape control disconnects from the tape unit after starting rewind type operations and is free to accept another command from the channel.
- Tape control is interlocked to the tape unit during any read/write type control command.
- Request in interrupt is initiated by the tape control for end status at the completion of the operation.
- Device end bit is sent to the channel in the end status byte.

When the tape control receives a tape motion control command (review Figure 1-9), it sends a channel end bit to the channel in the initial status byte. When the channel accepts the status byte, it initiates the command by sending service out to the tape control. After receiving service out (or command out to reject the status), the tape control drops operational in to disconnect from the channel and activates control lines to the tape unit to start the operation.

Rewinding Commands

If the control command is a rewind type of operation (rewind or rewind-unload), the tape control sends the rewind signal to the tape unit. When the tape unit indicates that it has started rewinding, the tape control disconnects from the selected tape unit. Unless rewind-unload is designated, the tape control is free to accept initial selection for another command from the channel (for any other tape unit).

Immediately after initial selection is complete for a rewind-unload, the tape control initiates a request in interrupt procedure to send a second status byte. This byte includes a device end, unit check, and CU end bit, indicating the rewind-unload has begun (although a second device end is possible after manual intervention). When the interrupt procedure is complete, the tape control is free to accept initial selection.

End Rewind: When a tape unit completes a rewind operation, it must signal the tape control with a unit free-device end. The tape unit that has completed a rewind sends a unit free signal to the tape control. Unit free stops a device end-unit free scanning register at the address of the tape unit.

The tape control begins a request in interrupt procedure and sends an end status byte, containing the device end bit, to the channel to end the interrupt procedure. If the tape control is performing another operation when the tape unit indicates that it has finished rewinding, the other operation in progress must be completed before the request in interrupt is started.

A rewind command causes the tape unit to unload tape, rewind the tape until the load point marker (at the beginning of the reel of tape) passes the head area, load tape back into the vacuum column, and move tape forward to load point.

End Rewind-Unload: A rewind-unload command causes the tape unit to unload tape, rewind the tape to the load point marker, and stop (leaving the tape unloaded). Operator intervention at the tape unit control panel is necessary for any further operation with a tape unit after a rewind-unload is complete. Another device end is generated by unit free when the tape unit is again made ready manually, and another request in interrupt results. (See Figure 1-10 for a review of status byte interface sequences.)

Read/Write Control Commands

If the control command is a read or write type command (erase gap, write tape mark, backspace block or file, or forward space block or file), the tape control must remain interlocked to the tape unit while the operation is being performed. At the completion of the operation, the tape control begins a request in interrupt procedure to send an end status byte (containing a device end bit) to the channel to end the operation).

Erase Gap: An erase gap command causes the tape unit to erase about 4 inches of tape. The tape control sets the tape unit to write status, starts tape motion, and forces a load point (LP) delay. Since

no data is sent to the tape unit during this operation, the tape is erased.

Write Tape Mark: A write tape mark (WTM) command causes the tape unit to erase about 3-3/4 inches of tape and write a special tape mark byte (and an LRCC) at the end of the erased section. The tape control sets the tape unit to write status, starts tape motion, and forces an LP delay. Since no data is sent to the tape unit during this operation, the tape is erased.

After 204 milliseconds of erasing tape, start delay is initiated, with the tape mark byte and LRCC being written at the end of the delay. A nine-track tape mark byte consists of 1 bits in tracks 3, 6, and 7 only. A seven-track tape mark (feature operation) consists of 1 bits in tracks 4, 5, 6, and 7.

Space Block: A forward space block or backspace block operation moves the tape forward or backward one block (to the next interblock gap). This operation is similar to a normal read operation, except that read data is accepted by the tape control but not sent to the channel and read error checks are degated.

If the tape block is a tape mark, a unit exception status bit is added to the end status byte.

Space File: A forward space file or backspace file operation moves the tape forward or backward to the next tape mark (recorded on the tape during a previous write tape mark operation). This operation is similar to a read operation, with the tape control checking for a tape mark at the beginning of each block. (Read data is accepted but not sent to the channel, and read error checks are degated.) The tape does not stop and start again at the end of each data block; it remains in motion until the tape mark is detected.

Write Operation

- Tape control transfers data from the channel to the tape unit during a write operation.
- Tape control requests the first data byte from the channel and stores it in the data register during the write delay. If the first byte is not available from the channel, write operation is stopped and a word count 0 is indicated.
- Each data byte is obtained from the channel by a service in/service out sequence; then written on tape.
- Written data is read back to the tape control for validity checking as tape passes over the read heads.
- End status in procedure is begun when the read circuits detect the end of the block.

During a tape write operation, the channel transfers one byte at a time across the interface lines to the tape control. The tape control initiates all data transfers from the channel, checks each input byte for odd parity, discards the parity bit, and stores other bits of the byte in the data register. In processing bytes from the data register to the write circuits and selected tape unit, the tape control:

1. transfers all bits in eight-bit bytes (nine-track operation),
2. transfers six bits of the eight-bit byte and discards the two high-order positions, 0 and 1 (seven-track translator off mode),
3. converts 3 input eight-bit bytes to 4 six-bit characters (seven-track data converter on mode), or
4. translates each eight-bit byte to equivalent six-bit BCD character (seven-track translator on mode).

(A mode set command previous to the write operation sets the mode register to establish how data is processed during seven-track write operations.) In all cases, however, the tape control transfers one byte to the tape unit during each write clock cycle.

First Data Byte: During the write delay to allow tape to attain operating speed, the tape control requests the first data byte with a service in request to the channel. A channel service out request stores the byte in the data register during the delay. A command out response stops tape motion and begins an end status in procedure.

Write and Read Check Data Block: Each data byte is processed from the channel to the tape control by a service in/service out procedure; then written on tape. When the tape moves across the head, the tape unit reads each byte written previously and returns the data to the tape control which examines it for recording errors that may have occurred. The tape control processes channel data to the tape unit at the same time that it performs a check operation on bytes that were written earlier.

Stop Write: When the channel transfers the last byte in the block, it answers the subsequent request for data from the tape control with command out tag, indicating that the last byte has been transmitted. The tape control causes the tape unit to write the check character(s) at the end of the block.

When the tape unit reads the check character(s) and returns them to the tape control, end of block is detected. The tape control examines the returned check characters, resets the circuits employed in

the write operation, and transmits an end status byte to the channel. See "End Status -- Burst Mode."

The tape unit then begins its stop delay.

Read Operation

- Tape control transfers data from the tape unit to the channel during read operations.
- Each data byte is transferred to the channel by a service in/service out procedure.
- Data is checked for errors as it passes through the tape control.
- End status in procedure is begun when the end of block is detected.

During a read operation, the tape control receives six-bit or eight-bit bytes from the tape unit and transmits odd parity eight-bit bytes to the channel. The tape control initiates all data transfers to the channel. In processing a byte, the tape control strips the parity bit before storing bits in the data register. The tape control assigns the P bit in each byte sent to the channel to ensure that each byte on the bus in lines contains odd parity.

In processing tape data to the channel, the tape control:

1. transfers to the channel all bits in the eight-bit byte received from the tape unit (nine-track operation),
2. changes each input six-bit character to an eight-bit byte by adding two zeros in the high-order position and transfers the eight-bit byte to the channel (seven-track translator off mode),
3. converts 4 input six-bit characters to 3 eight-bit bytes for transmission to the channel (seven-track converter on mode), or
4. translates each six-bit BCD character to an equivalent eight-bit BCD byte (seven-track translator on).

Bits in the mode register (from the previous mode set command) control the manner in which the tape control processes data characters during a seven-track operation.

Stop before EOB: The channel is not required to accept all bytes in the tape block. After accepting the first byte, the channel can terminate data transfers from the tape control at the end of any cycle by responding with command out to a service in request. However, the tape control and the tape unit are committed to the operation until the tape unit reads the complete block. If the tape unit has not transferred the last byte of the block when the channel indicates that it will not accept more data, the tape control blocks service in requests to the channel. The tape control receives, checks, and then discards bytes subsequently received from the tape unit.

End of Block (EOB): When the read circuits detect the check characters at the end of a tape block, the EOB condition causes the tape control to send an end status byte to the channel. See "End Status -- Burst Mode." Tape control read circuits are reset and the tape unit begins its stop delay.

Tape Mark: When the beginning of the tape block is read, the tape control always checks for a tape mark. If a tape mark is indicated, no bytes are transferred to the channel, error circuits are degated, the read operation is ended, and a unit exception status bit is added to the end status byte.

Read Backward Operation

- Tape unit is set to read backward status.
- Major objectives are the same as for a read forward operation.

A read backward operation is similar to a read forward operation, except that the tape moves in the reverse direction and the check characters are read before the data. The data flow path and controls are the same as for read forward.

Feature Operation: Read backward operations are automatically in data converter off mode. The translator operates normally.

A tape mark block is the same when read forward or backward. A tape mark consists of two identical characters: a tape mark and a tape mark check character. Because the configuration is symmetrical, the detection circuits are similar for forward and backward operations.

If the tape unit is at load point, no tape movement occurs and the operation is terminated as soon as initial selection is complete.

End Status -- Burst Mode

- Any operation performed while interlocked to channel on the interface is in burst mode.
- A normal or abnormal set ends signal causes the tape control to begin an immediate status in procedure while in burst mode.
- Status byte usually contains channel end and device end, but can contain other status bits.

- Tape control disconnects from the interface after the channel accepts (or rejects) the status byte.

A set ends signal is generated within the tape control when:

1. A normal or early end is signaled for a read, write, or sense operation.
2. Tape unit drops ready during an operation.
3. Read backward encounters LP.

The set ends signal generates a channel end and device end status bit, and also gates all active status bits to the data register. Tape control activates the status in tag to the channel as it gates a status byte from the data register to bus in.

If the channel responds with service out, the tape control ends the operation by disconnecting from the interface. A command out response from channel causes the tape control to stack status, disconnect from the interface, and attempt a request in interrupt procedure to send the stacked status byte again.

End Status -- Request In Interrupt

- A request in interrupt is necessary anytime end status becomes available when the 2415 is not interlocked to the channel.

- Request in is a control unit initiated selection sequence necessary to recapture the channel.

- Tape control activates request in to the channel which responds with select out.

- Tape control then activates operational in and address in, and places an address byte on bus in.

- Channel responds with command out which signals the tape control to send status.

Whenever outstanding status, usually end status, is held by the tape control and the channel has disconnected earlier (dropped select out), the tape control must re-establish interface communication before end status can be sent. This sequence is begun by an end or stack status condition which causes the tape control to send the request in tag to the channel. When the channel select out response arrives, the tape control raises operational in and address in, and places the tape control and selected tape unit address (locked in device register) on bus in to identify itself.

The channel responds with command out to signal the tape control to send the status byte. From this point, the procedure is the same as for an end status -- burst mode entry.

Status Bits

A single byte of status information (bits) is sent to the channel for the following conditions:

1. Short busy sequence; initial selection is rejected.
2. At the end of every initial selection sequence.
3. When a rewind-unload operation is begun at the tape unit.
4. At the end of any operation that is completed after initial selection is terminated.

Refer to Figure 1-13 for a detailed summary of status bits for the four conditions.

Bit	Designation	When Used
0	Not Used	
1	Status Modifier	See bit 3, busy, description.
2	Control Unit End	1. At completion of an operation during which a TC busy was indicated. 2. At completion of an operation during which a unit check or unit exception is detected.
3	Busy	1. With status modifier bit 1, a TC is addressed and the TC is busy with another command or has status pending for a different TU (short busy). 2. Without status modifier bit 1, a command other than test I/O is recognized and the TC has status pending for the addressed TU (long busy) or (including test I/O) the addressed TU is rewinding.
4	Channel End	1. A read, read backward, write, or sense command has been completed. 2. A control command has been accepted.
5	Device End	1. TU has completed a command: tape reaches LP during rewind; rewind-unload is completed at TC level (TU drops ready); command is completed (occurs with channel end for non-control commands). 2. Occurs with channel end and unit check if TU ready drops while performing a command. 3. TU goes from not ready to ready if TC selected TU while it was not ready, or if TC initiated the rewind-unload that caused the TU to become not ready.
6	Unit Check	1. Any bit except 3 is on in sense byte 0. 2. TU performs read backward, backspace block, or backspace file into or at load point. 3. A rewind-unload is completed at TC level. 4. A ready drop occurs during tape motion operations. 5. A non-existent TU is addressed during initial selection.
7	Unit Exception	1. A write, WTM, or erase gap operation is performed in the end-of-tape area. 2. A tape mark is detected during read, read backward, forward space block, or backspace block.

FIGURE 1-13. STATUS BITS

Turnaround

- Turnaround is necessary when present tape unit directional status is different than the direction indicated by the command.
- Tape control commands the tape unit to change directional status, and provides operational delays until mechanical change is complete.
- Turnaround time is 205 milliseconds

Directional status of the selected tape unit is inspected by the tape control at the beginning of a tape motion operation, and is compared with the direction indicated by the command. If the directions do not match (command is read backward and tape unit status is forward, for example), turnaround is performed.

During turnaround, the tape control commands the tape unit to change status, and delays the command operation long enough for the tape unit to mechanically change the direction of its capstan motor. The tape control sends another signal to the tape unit during turnaround (brake) to hold the reel brakes on while the tape unit is changing its directional status. Total turnaround delay time is 205 milliseconds.

ERROR CHECKING

Error checking circuits recognize error conditions that occur within the tape control or tape unit and error conditions caused by channel operation. A summary of the error conditions is in Figure 1-14. Basic error circuits are shown on Figure UDC-1.

When an error is detected in the tape control (except for gap noise), the next status byte to the channel contains a unit check bit in position 6. Most error conditions activate a separate sense bit and light a separate indicator on the CE panel. In this way, error information is provided for the channel (in a sense operation) and the customer engineer.

Data Check: A group of four data errors are indicated collectively as a data check; these errors (skew, data register, read register, and LRC register) cause a data check sense bit to be sent to the channel in sense byte 0, and the individual sense bit to be sent in sense byte 3.

Equipment Check: An equipment check is a collective indication of two error conditions: C-compare check and counter check.

Parity Check: The command byte (during initial selection) is checked for parity by the bus out check circuit. Bus out check is also signaled for bad parity of the data bytes during write operations. A C-compare check is a parallel parity check of write or read data. Data read back from tape during write operations is parity-checked in the read register (read register VRC).

Data bytes transferred from magnetic tape to the channel during read are checked for correct parity by data register check. A read parity error causes data register VRC and unit check.

Command Reject

A reject error indicates the tape control has received a command it cannot perform: a write, write tape mark, or erase gap is designated and the selected tape unit is file-protected. A mode set-set data converter on command is designated and the data convert feature is not installed in the machine.

Error Indication	Operation	Sense Byte/Bit	Collective Indication	Figure Number	Cause
Command Reject	Write, DC On Mode Set	0/0	U	2-22	FP Error or Set DC On Error
Bus Out Check	Write, Initial Selection	0/2	U	2-23	Parity Error
Overrun	Write, Read, Read Backward	0/5	U	2-29	Late Service Out Response
Word Count 0	Write	0/6	U	2-25	TC Is Refused First Data Byte
Interblock Gap Noise	Write, WTM, ERG	1/0	None	2-27	Noise Signals in Erased Area
Data Register VRC	Read, Read Backward	3/0	D,U	2-30	Read Data Parity Error
LRC Register Check	Write, WTM, Read, Read Backward	3/1	D,U	2-32	Longitudinal Redundancy Error
Skew Error	Write	3/2	D,U	2-24	Excessive Skew (of Data Read)
Read Register VRC	Write	3/4	D,U	2-31	Parity Error (of Data Read)
*C-Compare Error	Write, Read, Read Backward	3/7	E,U	2-34	Parity Compare Error
Counter Check	Operations Using WC-DC	None	E,U	2-26	Delay Counter Steps Too Far
Ready Drop	Tape Motion Operations	None	U	2-28	TU Drops Ready after Start of Operation
Data Convert Check	(See Chapter 4)				

D Data check sense bit (byte 0, bit 4)
E Equipment check sense bit (byte 0, bit 3)
U Unit check status bit (bit 6)

*Inactive for seven-track translate operations

FIGURE 1-14. ERROR CONDITIONS (NRZI OPERATION)

Bus Out Check

Bus out check indicates that either a command byte or a write data byte had incorrect parity. The parity error may have occurred on bus out or in the data register.

A bus out check during initial selection blocks performance of the operation because correct parity of the command byte is a prerequisite for loading the command into the command register.

Overrun

Overrun is a timing check to ensure that each write data byte is received from the channel in time to place it in position on the tape, and that each read byte is accepted by the channel before the next byte is placed on bus in.

If the service out response to service in (indicating that the read byte on bus in was accepted, or that the next write byte is on bus out) does not occur before a specified time, overrun is set.

Word Count 0

A word count 0 error occurs at the beginning of an attempted write operation when the channel responds to the request for the first byte with command out (initiating a stop command). The tape control, which has started to move tape, stops tape motion by beginning the normal end status in procedure, and the write operation is not performed.

Interblock Gap Noise

Interblock gap noise indicates that an erased area has not been erased completely. During a write or write tape mark operation, the read head checks the gap during the start delay for any bits with enough amplitude to be read. In an erase gap operation, the tape is checked from the beginning of tape motion until the beginning of the stop delay.

Data Register Check

A data register check indicates that data in the data register during a read or read backward operation does not have correct vertical parity. If incorrect parity is recognized, data register VRC is indicated.

During nine-track operations, vertical parity is always odd. During seven-track feature operations, either odd or even parity is designated by a previous mode set control command.

Longitudinal Redundancy Check (LRC)

An LRCR check is made during a write, write tape mark, read, or read backward operation to ensure that each track in a tape block, including the CRC and LRC characters, contains an even number of bits. The LRC register must be completely clear of all bits after the LRCC is read at the end of a read or reach check of a write operation; if not, an LRC register check is indicated.

Skew Error

Skew is the time lapse between the receipt of the first bit and the last bit of a byte of data. (Review "Skew.") A skew error occurs if the bytes are written too close together or if bits in a byte are skewed excessively. If a malfunction causes the tape to move too slowly during writing, especially as tape starts, the bytes are too close together.

A skew check is made only during the read check of a write operation, because a skew error signal only, during a read operation, does not necessarily indicate an unreadable block. If the tape block can be read without other errors (VRC, etc.), indicating the block was read successfully, it would be needless to signal an error condition. During write operations, however, it would be unwise to retain a tape block with a marginal skew condition, which might cause subsequent reading trouble, when the block can be recreated easily.

Bytes are checked for skew by providing a time gate for all bits of a byte to be read. A skew error is signaled if any bits are received after the gate is "closed."

Read Register VRC

A read register VRC is a check for vertical parity of data bytes during a write operation only. After bytes have been written, they pass over the read heads, are routed into the read register, and are checked for correct vertical parity. During nine-track operations, parity is always odd. Parity is either odd or even for seven-track operations, depending on the mode register setting.

C-Compare

A C-compare is a check of data transmission between the read register output and data register output during a read operation, and between the bus out P-bit trap and the data register output during a write operation. C-compare is a check to determine that the

parity of a byte is not changed as the byte moves through the tape control. Compare error signals are blocked if a data check or bus out check is also detected.

Counter Check

This error condition occurs when the write clock-delay counter steps to 1536. The delay counter is always stopped before this time during a normal operation. Counter check, therefore, indicates a malfunction in the counter or in one of the circuits that controls counter stepping and resets.

Ready Drop

Ready drop is caused by the loss of ready in the tape unit during any tape motion operation (other than rewind and rewind-unload, when ready is normally dropped). The operation in progress is terminated immediately by the tape control when a ready drop occurs. No ready drop error signal is indicated; only a unit check status bit signals that an error condition has occurred.

Data Convert Check

The data convert check is effective only when the two optional features (seven-track and data convert) are installed. The purpose of a data convert check is described in Chapter 4.

CE PANEL

A CE panel is located on the tape control. By using this panel, the customer engineer can check the operation of the tape control and any attached tape units while the tape control is logically disconnected from the channel.

Any single command from the channel can be simulated by setting the rotary command switch. Three additional commands can be simulated in sequence by inserting three command cards in position on the panel and turning on the multiple command switch. This allows the performance of four consecutive commands. The last command performed is determined by the switch setting and the other three commands are determined by the command cards. If any command cards are used, all three must be used. The desired command can be repeated or the "no-op" command can be used.

A block of any length (controlled by the go-up control) may be written with a fixed bit pattern determined by the bit switch settings.

Indicator lights display the contents of the data register and device register, all error checks, and other information useful in preventive and corrective maintenance.

A receptacle is provided for a remote cable with start and reset switches.

When the command switch is not set at ON LINE, the meter switch is off, or power is off, a select out signal from the channel passes through the tape control to the next control unit on-line and operation of the channel with other I/O devices is not affected.

POWER SUPPLY

Power for the tape control and all attached tape units is provided by a single power supply located in the frame that contains the tape control (frame 1). The power supply provides +12, -12, and -24 vdc; 115 and 12 vac, single-phase; and 208 vac, three-phase. Overload protection is provided by circuit breakers in power supply input and by fuses (with indicating lights) in the power supply output.

METERING

A meter located on the operating panel of tape unit 0 records the time that the 2415 is in use.

The meter operates when three conditions are satisfied:

1. Meter out from the channel is active. This indicates that the channel is operating or is available.
2. The 2415 is on-line.
3. An attached tape unit has tape loaded in the vacuum column and is ready but is not at load point, or is rewinding.

A meter in line enables the CPU meter to run when the 2415 is busy. Turning off the switch on the meter panel or setting the CE command switch away from ON LINE locks the tape control unit in off-line status and the meter cannot run.

A clock out line from the channel makes it impossible to change the on-line/off-line status while the channel is busy.

Figures 2-1 to 2-34 are released in the maintenance volume as reference pages beginning with page numbers 00.21.01.1 and 00.31.01.1.

METERING AND ON-LINE GATING (FIGURE 2-1)

- A 2415 tape system contains one usage meter.

- The usage meter runs only when three conditions are satisfied:
  1. The TC is on-line.
  2. The channel meter-out line is active.
  3. Any of the six tape units is loaded and not at LP.

- TC on-line or off-line status can be changed by either the meter on/off switch or the CE command switch if two conditions are satisfied:
  1. The clock-out line is inactive.
  2. The TC is not busy (idle).

Usage meters record the time a system, unit, or group of units is busy. The customer records the meter readings monthly for billing purposes.

A 2415 TC with as many as six attached tape units contains only one usage meter (unlike many other tape systems which have a meter on the TC and one on each attached tape unit). The 2415 usage meter and meter on/off switch are mounted on the operating panel of tape unit 0, frame 1. This meter records time whenever the central processing unit (CPU) is recording time, and the TC is not off-line and any of the six tape units is loaded and not at load point.

Metering Interface Lines

Meter signaling between the TC and the system uses three interface lines: meter out, clock out, and meter in.

Meter Out

When the CPU is recording time, the meter-out line from the channel is active (providing that the channel is in on-line status). Meter out is gated into the TC by the on state of the on-line latch.

If any tape unit is loaded and away from load point, the TU "meter-on" line gates "run meter" to pick a reed relay which activates the usage meter. A loaded tape unit is considered as being used as long as it is off load point, even though it is not moving tape.

Clock Out

The state of the on-line latch, which determines whether the usage meter can run, can be changed by the meter on/off switch (or the CE command switch) only when the channel clock-out line is inactive. An active clock-out line indicates that the CPU is either not stopped or not waiting; thus, the CPU must be in an inactive state before the TC can be set from on-line to off-line or from off-line to on-line status.

Meter In

An active meter-in line to the channel indicates that the TC is on-line and busy. The TC is busy if the command busy latch is on, indicating that an operation is in progress, or that the TC is still interlocked to the channel (held on-line).

On-Line Latch

When the on-line latch is on, the TC is enabled (on-line); when the latch is off, the TC is disabled (in an off-line condition) and cannot perform on-line operations. Meter out from the channel and meter in to the channel are degated by the off state of the on-line latch. Also, the usage meter cannot run when the TC is off-line.

The on-line latch can be turned off by the meter on/off switch or the CE panel command rotary switch. Generally, the meter switch is used by system operators to control operation of the usage meter. The CE panel rotary switch automatically resets the on-line latch when the command switch is rotated away from the on-line position. To turn on the on-line latch, the meter switch must be on and the command switch set to the on-line position.

However, neither switch is effective unless:

1. Clock out from the channel is inactive, and
2. The TC is not busy (performing a command or operation).

NOTE: When the on-line latch is off, latch outputs degate all channel interface input and output lines. Consequently, the TC cannot respond to an attempted initial selection by the channel; the select signal is bypassed.

SELECT SIGNAL SWITCHING AND GATING (FIGURE 2-2)

- The select signal may arrive as either select out or select in, depending on TC priority.

- Select signal priority is established by panel jumpers when the system is installed.

- A reed relay card routes the select signal.

- If 2415 TC power is on and the TC is in an on-line condition, the reed relay is picked to allow entry of the select signal.

- A power-off or off-line condition drops the reed relay, so that the select signal is bypassed (provided the TC does not supply interface terminator voltage).

- The select signal, whether it is select out or select in, is referred to as select out on Systems pages.

Control unit priority, as explained in Chapter 1, is determined by the:

1. physical location of the CU among the interface cables
2. select out/select in priority jumpers.

Details of panel jumper connections are shown at the bottom of Figure 2-2. The heavy lines (note 2) indicate jumpers for high-priority operation. Note that select out is jumpered from pin B to pin C, and then to the reed relay card. Note also that select in passes through two jumpers as it enters and leaves the tape control.

Select Reed Relay (RR1)

When the 2415 TC is in an on-line condition and power is on, the select signal reed relay is picked. The signal from pin C or pin D (3Y02) passes through RR1-1 N/O (via relay card pins B and D) to condition the minus AND (3B) input to the select circuit. If the relay is down, the select signal passes through RR1-2 N/C and RR1-3 N/C, through a panel jumper, and to the next CU.

Select Out Circuits

After the select signal passes through RR1, it is gated by "-S on-line," then hold out from the TC (AND C4). The on-line gate is necessary if select arrives as off-line status is set; the gate at AND 3B operates faster than the relay (RR1) can drop. The hold-out line is necessary to decondition the select signal rapidly. Hold out is sent in parallel to all control units; the select signal (select out/ select in) is sent in series and, not gated by hold out, would take too long to drop at the TC.

The select signal is referred to as select out on Systems pages. Although select out is routed to several 2415 circuits, it is ineffective unless an address decode condition exists. Address decode is active only if bus out contains the correct 2415 TC address. See "Addressing." If address decode is inactive, the select signal is bypassed by the AND at 5F-5G (Systems 01.01.68.1) and through RR1-4 N/O to the next CU.

If address decode is active, select out or select out delayed conditions other 2415 circuits. The delayed select signal, select out 1, is used to delay the rise of some lines (such as bypass select) or to delay the fall of other lines. Note that the force burst line maintains the select out lines (OR 3C); force burst forces up select out to degate reset of the operational in latch and allow completion of an interface operation if the channel drops the select signal too early.

ADDRESSING

- An interface I/O address byte consists of a five-bit control unit address and the three-bit address of an attached I/O device (tape unit).

- To become selected, the control unit must recognize its address on bus out during an initial selection sequence.

- A control unit generates its address and sends it with a TU address to the channel on bus in during an initial selection or request in interrupt sequence.

- A tape unit (TU) address is set into the device register during an initial selection sequence.

- A unit free condition (scanner stop) causes generation of a TU address within the device register.

- A TU is unconditionally addressed (selected) when its address is in the device register.

- TU address compare circuits are important only if a status pending condition exists at the beginning of an initial selection sequence.

Address Decoder (Figure 2-3)

- A control unit address is in bit positions 0-4 of an I/O address; bit position 0 is the high-order position.

- Address decode circuits are set (wired) by address card pluggable jumpers to establish a specific I/O address.

- The 2415 TC address decode line is activated when the correct TC address is decoded.

- Initial selection proceeds only if address decode is active.

To initiate an I/O operation, the channel begins an initial selection sequence by placing a combined tape control-tape unit address on the interface bus out. Each control unit on the interface compares the control unit address portion of the address byte with its preset address as soon as address out (and select out in the 2415) rises. Because each control unit has a different I/O address, only one control recognizes the address (providing the address is valid and all control units are functioning normally).

An I/O address byte consists of:

1. Bits 0-4 -- control unit address
2. Bits 5-7 -- I/O device (tape unit) address
3. P bit for odd parity of the address byte

The 2415 TC address decode (compare) circuit is a set of pluggable jumpers on an EHR standard jumper card at card location 3H05. These jumpers represent a preset address that is compared with channel bus out lines to decode the address. When the system is installed, the TC address, selected by the customer, is fixed by installing jumpers that allow all decoder outputs to become active when the proper TC address is on bus out. See Figure 2-3.

Each jumper allows a plus level output if the address is correct; all five outputs must be active (+) to indicate recognition. A +bus out line is plus if a 1 bit is indicated and, the -bus out line is minus for a 1 bit. The converse is true for a 0 bit; therefore, +bus out is plus for a 1 bit and -bus out is plus for a 0 bit.

For example, if the TC address is 00110 (binary), the card jumpers are installed as follows:

Address bit 0	Pins P and Q (+ level indicates 0 bit)
Address bit 1	Pins L and M (+ level indicates 0 bit)
Address bit 2	Pins K and H (+ level indicates 1 bit)
Address bit 3	Pins F and E (+ level indicates 1 bit)
Address bit 4	Pins A and B (+ level indicates 0 bit)

Address Decode Latch

During initial selection, address out and select out are activated by the channel. Assuming that the sample address (00110) is in the 2415, the address decode latch is set to allow an initial selection sequence to take place. Note the latch output functions on Figure 2-3; these functions are described under "Initial Selection Sequence" in Chapter 3.

Address Decode Latch Reset

An address decode latch reset occurs if the following conditions exist:

1. Status in and command out: if the channel rejects the status byte at the end of initial selection.
2. Service out: if the channel accepts the status byte at the end of initial selection.
3. Operational in and select out are inactive (the TC is not communicating with the channel).
4. Halt I/O (channel has issued an interface disconnect to stop the initial selection sequence).
5. Machine reset. See "Machine Reset."

Address Generator (Figure 2-3)

- A combined TC-TU address is sent to the channel for address verification during an initial selection or request in sequence.
- Address generator circuits encode the correct TC address for transmission to the channel.
- The binary address code is generated by pluggable jumpers connected to fixed voltage levels.
- The TU address is not encoded by the address generator.

During either a request in interrupt or initial selection sequence, the 2415 TC verifies its identification by sending an address byte to the channel. The byte contains the TC address and the address of the designated TU. The combined address is gated directly to the channel bus in.

The TC portion of the address is wired with jumpers on the same type of EHR card (at 3H06) as the address recognition jumpers (Figure 2-3). (The TU address is gated from the device register.) If the address of the TC is 00110, the jumpers are installed as follows:

Address bit 0	Pins P and Q (- level indicates 0 bit)
Address bit 1	Pins L and M (- level indicates 0 bit)
Address bit 2	Pins K and H (+ level indicates 1 bit)
Address bit 3	Pins F and E (+ level indicates 1 bit)
Address bit 4	Pins A and B (- level indicates 0 bit)

Note that + and - levels are generated because the pluggable jumpers connect to fixed S level inputs.

Tape Unit Decoding and Unit Free Gating (Figure 2-4)

- The binary address of the selected TU is held in the device register.
- The three-bit binary address is decoded to activate one of six select lines.
- A TU is addressed (selected) when its select line is active.

- The logical address of select and unit free lines can be changed by panel jumpers.

A binary coded TU address can be set in the device registers in two ways:

1. From bus-out bit lines 5, 6, and 7 during an initial selection sequence.
2. As a result of the scanning function of the register being stopped by a unit free condition. See "Device Register and Device End Scanner."

Any time the device register is not scanning, the binary TU address is unconditionally decoded to select (address) one of the six tape units.

TU Address Decode

The active and inactive outputs of the device register are decoded by AND circuits to activate one of the six tape unit select lines. Except for unit free signaling, only a selected TU can communicate with the TC.

Selection Jumpers: Normally, the six select lines to the tape units are connected by panel wire jumpers to the decoder outputs as indicated on Figure 2-4. The jumper connections provide the ability to change the logical address of any or all tape units.

For example, suppose addresses for tape units 2 and 3 are to be exchanged:

Remove jumpers:	from 4F02 pin C to pin L
	from 4F02 pin D to pin P
Add jumpers:	from 4F02 pin C to pin P
	from 4F02 pin D to pin L

TU addresses may also be changed by switching select line jumpers within each TU. Remember, however, that write deskewing is gated by select lines; skew re-adjustment may be necessary any time select lines are exchanged.

Unit Free Gating

Any or all tape units can signal a unit free (end rewind) condition; however, the scanning sequence and the order in which the signals arrive determine which TU becomes selected when the scanner is stopped. See "Device Register and Device End Scanner."

In addition to the stop scan line, only ungated unit free lines stop the scanner. The address in the device register (which is the stopped scanner) is decoded, and the appropriate select line selects the TU and gates out the corresponding unit free line. Unit free is gated by select to ensure that device end is generated for the designated TU address only. If the channel rejects the unit free (device end) status byte, the internal stack latch is set to "remember" that a unit free is still waiting.

Because each TU has its own unit free line, each line corresponds to a particular select line. Therefore, panel jumpers are provided to allow the exchange of unit free lines at the same time select lines may be exchanged. The unit free and select lines for a particular device must correspond exactly; otherwise, unit free signals will be generated for the wrong TU addresses.

TU Address Compare

- A TU address compare condition indicates a match between the TU bus out address and TU device register address during initial selection.

- Address compare blocks a short busy response to initial selection if status pending is active.

- Pending status causes a short busy response to initial selection without an address compare, or causes a long busy response with an address compare.

A true AND-OR logic compare circuit is used for TU address comparison. Bus out bit 5, 6, and 7 lines are compared with TU device register outputs to determine if an exact match exists during an initial selection sequence. A TU address match is significant only if status pending is active. Status pending indicates that the TC is holding status information for a previous operation associated with a particular TU address.

If an address compare is indicated, the initial selection sequence is allowed to continue because the initial status byte to the channel relieves the TC of the outstanding (pending) status for the addressed TU, although the intended operation will be blocked by long busy. If an address compare is not indicated, the status pending condition causes a short busy (force status in) sequence which blocks normal completion of the initial selection sequence. However, the status pending (outstanding status) condition is not cleared and the CU end (status) latch is set. See "Initial Selection Sequence" in Chapter 3 for additional information.

DEVICE REGISTER AND DEVICE END SCANNER (FIGURE 2-5)

- Device register and device end scanner consists of three latches and set/reset controls.

- A three-bit binary TU address is stored in the device register.

- Device register outputs are unconditionally decoded to activate one of six TU decimal addresses.
- A TU remains selected (addressed) as long as its address is held in the device register.
- The device register is stepped, like a counter, when selection of a TU is unnecessary.
- When stepping, the register is scanning for a unit free (device end) condition at any TU.

The device register and device end scanner are combined into a single circuit that functions as either a register or counter (scanner); the basic circuit consists of three latches. When functioning as a register, this circuit stores the address of the TU to be selected. When functioning as a scanner, the latches are stepped like a counter to scan for tape units that may be signaling a unit free (ready) condition.

Device (TU Address) Register

Device register latch positions are designated device register A, B, and C, which represent the binary numbers 4, 2, and 1. Six tape units are available to a 2415 TC, and these units are represented by addresses 0-5. Any time an address is held in the register, the three-bit binary address is unconditionally decoded to activate one of the six decimal addresses. See Figure 2-3. A TU remains selected as long as its binary address is held in the register.

A TU address is set into the device register by one of two conditions:

1. During an initial selection sequence when the address decode line is active if the TU select latch is off. The register is reset before the rise of select out 1, and set to bus out lines 5, 6, and 7 after the rise of select out 1 (bottom of Figure 2-5).
2. When the register stops scanning to indicate the address of a TU with a unit free condition; the scanning function is controlled by AND sets A, B, and C and resets A, B, and C.

Regardless of the method by which the TU address is set into the register, the basic functions are the same:

1. The output is decoded to activate the proper select line.
2. The register originates the binary TU address destined for the channel during an initial selection or request in sequence.

Device End (Unit Free) Scanner

When no TU remains selected, the stop scan line becomes inactive and the device register latches begin to step as a free-running counter; this is called scanning. The register scans (counts) in the TU decimal address sequence 0, 4, 5, 1, 3, 2, 0, ... at approximately a 5-megacycle rate. Note the latch set/reset timing diagram at the lower right of Figure 2-5.

Provided no TU signals a unit free and the stop scan line remains inactive, the register scans continuously when power is on. Device register latch outputs are routed back to the input set A, B, and C AI's and the reset A, B, and C AI's, to control the scanning function. During a complete scanning cycle, each TU address is activated once for a short period (not long enough to select a TU).

As an example of scanner operation, note the set A AND at the moment when all latches are off (address 0 is active). Stop scan and all unit free lines are plus; device register latches B and C are off; therefore these lines are also plus. Set A becomes active to turn on device register latch A. With latch A on, set C becomes active to turn on device register C. With latch C on, reset A becomes active to turn off latch A, and so on. Scanning continues until the common stop scan line becomes minus (active) to decondition all scanner set and reset circuits, or a unit free line becomes minus to decondition only the set and reset circuits that stop the scanner at the TU address that signals unit free.

Stop Scan

Stop scan is a TC control for stopping the scanner to ensure that a particular TU address is retained in the device register. Conditions that activate stop scan are:

1. Command busy latch on: during the execution of most commands, a specific TU must remain selected.
2. Address decode latch on: during the initiation of any command, the TC is addressing a specific TU that must remain selected.
3. Status pending: outstanding status exists for the TU address in the register and scanning cannot begin again until the status is sent to and accepted by the channel.
4. Operational in latch on: the TC is interlocked to the channel and is performing a sequence that is associated with a particular TU that must remain selected.
5. Chain latch on: command chaining is indicated during a status in procedure (usually at the end of initial selection). The selected TU must remain selected until the chain is "broken." A chained TU has device end (unit free) signal priority.

Unit Free Device End

When a rewind or rewind-unload operation is begun at a selected TU or a TU is selected when it is in a not ready status, the TC generates "set arm" to turn on the TU arm latch (upper left, Figure 2-5). When a TU becomes ready with its arm latch on, its unit free line is raised and sent to the TC. Unit free at the TC indicates one of three conditions; the TU has:

1. reached LP after a rewind.
2. been made ready manually after a rewind-unload is complete.
3. become ready after it was selected while not ready (during manual rewind, for example).

Any active unit free line stops the scanner which "locks up" with the address of the TU that sent the unit free signal. If two or more unit free signals arrive at the TC simultaneously, the scanning sequence (0, 4, 5, etc.) determines which TU becomes selected when the scanner stops.

Device End

A device end status bit is sent to the channel when any command operation other than test I/O is completed, and when a rewind-unload is begun. However, the device end latch is not used for unit free device end generation; the selected unit free line generates status bit 5 for transmission to the channel.

The scanner can begin scanning again as soon as the stop scan line drops after the status in sequence.

RESETS (INTERFACE)

- Resets restore groups of latches and triggers to a beginning status.
- Three types of resets can be transmitted over the interface: general reset, selective reset, and interface disconnect.
- The interface does not include reset lines; combinations of existing interface lines are used to activate interface resets.
- General reset is a system-generated, beginning reset that is issued to the channel which transmits it to all attached control units.
- Selective reset is a channel-generated, malfunction reset that is issued to a particular control unit.
- Interface disconnect is a channel-generated, halt I/O signal that is issued to a particular control unit.
- Interface resets cause the following at the 2415 Tape Control: general or selective reset stops any tape control and selected tape unit operation, and restores all tape control latches. Interface disconnect causes the tape control to reset only the latches necessary to disconnect from the interface, but any operation in progress continues to a normal stopping point.
- General and selective resets activate most 2415 tape control resets.

General Reset (Figure 2-6)

- Generated to create a beginning status throughout a System/360.
- Accepted by all attached channels and control units.
- Activates 2415 resets to end all operations and restore all triggers and latches.

A System/360 general reset is generated when the system reset key is pressed, when initial program loading is performed, or when power is brought up in the system. This reset clears all status and interrupt conditions, and establishes a beginning status throughout the system when the reset is terminated.

The channel propagates a system reset over the I/O interface. A system (general) reset condition is active in all attached control units when both the suppress out and operational out interface signals are inactive. All resets within the 2415 Tape Control (except reset arm) are held active, including machine reset to all tape units, while general reset is active, unless the tape control is in an off-line status. As a result, any operation in progress is stopped, all data transfer is terminated, the channel disconnects from the interface, and tape is stopped, regardless of the type of operation. Density is automatically set to 800 bpi.

Selective Reset (Figure 2-6)

- Generated as a result of a time-out condition or a malfunction detected by the channel.
- Signaled on the I/O interface from the channel by deactivating operational out while suppress out is active.
- Accepted only when the control unit is interlocked on the interface (operational in active).
- Activates the same resets as general reset at the 2415, except for machine reset to the tape units.

If the channel detects a malfunction in the tape control and/or tape unit operation or senses a time-out condition during interface operations, a selective reset is generated. The channel activates the suppress out line; then deactivates the operational out line. Only the control unit with its operational in line active can accept the reset (note the selective reset AND, Figure 2-6).

All resets activated by general reset within the 2415, except machine reset to all tape units, are also activated by selective reset if the tape control is not off-line. As a result, any operation in progress that is directly controlled by the tape control is stopped, all tape control latches are restored, density is set at 800 bpi, and the channel disconnects from the interface.

However, none of the attached tape units are reset; if one or more tape unit is performing a rewind type operation, a unit free causes a device end, request in interrupt after the rewind is complete.

Interface Disconnect (Halt I/O and Stop Latch, Figure 2-7)

- Generated at the channel usually as the result of a halt I/O instruction issued to the channel by the CPU.
- Causes the interlocked tape control to disconnect from the interface.
- Activates 2415 halt I/O to turn on the stop latch and reset any 2415 latch that can activate an interface line to the channel.
- Halt I/O creates a stop condition that stops data transfer and allows normal termination of any operation in progress.

An interface disconnect is generated by a channel (for reasons that vary with the type of system and channel) or as the result of a halt I/O instruction issued to a channel from the system. This disconnect signal causes the interlocked control unit to decondition its operational in line and allows the channel to disconnect from the interface. The operational control unit detects the disconnect when it senses an inactive select out and an active address out condition.

In the 2415 Tape Control, the disconnect signal activates halt I/O which resets the status in and force burst mode latches (among others) to cause the reset of the operational in latch. The set of the stop latch (Figure 2-7) begins termination of a burst mode type operation (write, read, or sense) by holding the service in latch reset and:

1. generating end write (and write disconnect) for a write operation.
2. generating early sense end for a sense operation.
3. allowing tape motion to continue until the next IBG is sensed for a read type operation.

A control operation is not affected because the tape control is not interlocked on the interface during execution of the command.

If an interface disconnect is detected during an initial selection sequence, the stop latch generates a TAU reset (Figure 2-10) which clears the command register to prevent execution of the designated command. In this case, status is not stacked.

RESETS (TAPE CONTROL)

- Basic resets generated within the 2415 Tape Control are:

Machine Reset	Idle Reset
Sense Reset	Reset Arm
Status Reset	Early Reset
TAU Reset	

- Machine reset is a complete reset that restores all tape control latches and registers and all tape arm latches.
- Sense reset is an initial selection, beginning reset of all tape control error (sense bit) latches.
- Status reset and reset arm are generated when the channel answers status in with service out, indicating the status byte was accepted.
- TAU reset is an end operation reset generated by a normal or abnormal end condition.
- Idle reset is active when the tape control is not busy and is available for operation.
- Early reset is a between-tape-block read gating reset during space file operations.

Machine Reset (Figure 2-6)

- Stops any operation in progress and restores all latches and registers in the tape control.
- Activated by a general or selective interface reset, or a power-on or manual tape control reset.
- Power-on reset pulse is generated by a tape control power-on sequence.

- Tape unit machine reset is generated by a tape control power-on reset.

- Manual reset is generated by depression of the CE panel reset key or by depression of the reset key on the remote start/reset box.

A machine reset establishes a beginning status throughout the 2415 Tape Control; all latches, including status and sense, are reset and the contents of all registers are cleared. Because forward or backward go is dropped unconditionally, tape is stopped without regard to mode or type of operation. Consequently, tape may be stopped within a block (before an IBG) during a read type operation.

A tape control machine reset is sent to all tape unit arm latches only if general reset is activated. A selective reset does not reset the tape unit arm latches (note AND E2) to allow generation of a unit free (device end) at the completion of a rewind type operation. A true machine reset is generated within all tape units by a tape control power-on condition.

Power-On Reset: As tape control dc power becomes active, a resistor-capacitor network generates a power-on reset pulse (Systems 07.01.02 and 07.07.01). Power-on reset OR'ed with manual reset generates tape control machine reset; power-on reset only is sent to all tape units to generate tape unit machine reset.

Manual Reset: Depression of the CE test panel reset key or the remote start/reset control box reset key activates manual reset. (Do not confuse this reset key with the operating panel reset key over each tape unit frame.) Manual reset, like the power-on reset, activates the tape control machine reset.

Sense Reset (Figure 2-6)

- Turns off all sense bit error latches.

- Primarily a beginning reset generated during initial selection for all commands, except those that require retention of sense data.

- Also generated by machine reset, CE circuit check reset, or on recognition of a tape mark after a read operation.

- Check reset is generated by depression of the CE panel check reset key.

A sense reset is generated to clear all sense bit indications in preparation for a new command operation. After the command register is set and the designated command is decoded during an initial selection sequence, the rise of command out 3 (see timing pulses on Figure 2-12) activates sense reset for most commands. The fall of command out 1 deactivates the reset.

Logically, sense reset is blocked if a sense command is decoded; the existing sense data must be sent to the channel during execution of the command. A test I/O or mode set no-operation command also blocks sense reset. A test I/O may precede a sense command; therefore, sense data should not be cleared. A no operation is a programming tool that performs no logical function in the tape system; therefore, sense data is not affected.

Read Tape Mark: During a read command operation, if the block that is read is a tape mark, sense reset is generated to turn off any error latch that may have been set. Recognition of the tape mark is, in itself, indication of a successful operation; none of the possible error indications are important. The channel is advised that a tape mark has been sensed by a unit exception status bit (7) in the end status byte (Systems 02.46).

Check Reset: Most sense bit latches are error (check) indicators. During off-line test operations, a customer engineer can clear these error latches by pressing the check reset key on the tape control CE test panel to activate sense reset.

Status Reset and Reset Arm (Figure 2-6)

- Status reset restores all status latches (except unit check) and turns off force burst mode after an end status in sequence.

- Generated by machine reset or when the channel accepts a status byte by responding to status in with service out.

- A channel service out response to status in also generates reset arm.

After the channel accepts a status byte, whose bits are composed of the on or off condition of the status latches, the status latches are restored. Status reset, therefore, turns off the status latches at the end of an initial selection sequence or after an end status in sequence if the channel accepts the status byte.

A command out response to status in does not generate a status reset unless control command is designated, because the control command is executed regardless of the type of response.

If test I/O is designated, status reset generates end test I/O at the end of initial selection. End test

I/O resets the force burst mode latch and generates a TAU reset. The off state of force burst mode and TAU reset ends the test I/O (initial selection) sequence.

Reset Arm: This is also a status accepted reset that turns off the arm latch of the selected tape unit. If the arm latch was on, it has caused a unit free-device end condition on completion of a rewind type operation and resulted in a request in, end status interrupt. Reset arm is gated by status bit 5 to bus in to ensure that device end has been sent to the channel.

Early Reset (Figure 2-8)

- Early reset latch is turned on by stop delay only for space file operations after spacing over all but tape mark blocks.
- Early reset deconditions the end read operation gating circuits, such as EOB timing.
- Early reset latch is turned off before reading each tape data block.

Idle Reset, and Green and Go (Figure 2-9)

- Indicates the tape control is idle and can accept initial selection.
- Idle reset holds the stop latch off.

When the command register is clear and the command busy latch is off, the tape control is not performing a command. If both the read and write clocks are also clear, a condition called green and go is active which resets and holds off the TAU reset latch.

Green and go activates idle reset if the device end scanner is not stopped by a chained command or status pending condition. Idle reset indicates that the tape control is not busy with an operation or not busy holding or anticipating end status.

TAU Reset (Figure 2-10)

- Clears the command register and turns off certain end operation latches.
- Usually generated by the on state of the TAU reset latch.
- Also generated by machine reset (including manual reset) or if selected tape unit is rewinding at the beginning of initial selection.
- TAU reset latch is set by a normal or abnormal end operation condition.

A command code is retained in the command register until the command is executed. After the command operation is completed at the TC level or a condition occurs that prohibits execution or normal completion of an operation, a TAU reset is generated to clear the command register of the command code. (TAU--tape adapter unit--is an obsolete term that is a carry over from earlier systems; consider TAU reset an end operation reset.)

In addition to the TAU reset latch, the TAU reset line is activated by a machine reset or a rewind busy condition.

Rewind Busy: Whenever a selected tape unit signals it is rewinding at the beginning of an initial selection sequence, the intended command operation must be blocked. To clear the command register, the rewind busy latch is set to activate TAU reset (rewind busy also generates a busy bit for the status byte). Rewind busy and command busy (Figure 2-12) are set at the same time (rise of command out 3, about 5.4 microseconds after the rise of command out after the address in sequence). However, the command busy latch is reset immediately because the command register is cleared by the TAU reset.

The initial selection sequence proceeds to a normal end, at which time "not operational in" turns off the rewind busy latch.

TAU Reset Latch

Most TAU resets are generated by the on state of the TAU reset latch. The turn-on conditions (Figure 2-10) are:

1. End test I/O: generated by a status reset if test I/O is designated. See Figure 2-6.
2. TU status set UK (unit check): this circuit, which also sets the unit check status latch, indicates a nonexistent tape unit when neither ready nor rewinding is active.
3. Stop during status in: an interface disconnect signal (halt I/O) is the only normal turn-on circuit to the stop latch (Figure 2-7) during a status in sequence.
4. Stack status at the end of initial selection: the stack latch is turned on if the channel responds to the initial status byte with command out instead of service out (except when control command is designated).
5. Command reject: either a service out or command out response to status in activates forced busy sample to cause a reset if:
   a. Selected TU is file-protected and a write type operation is designated.

b. Data converter on mode set is designated and the data convert feature is not installed.

6. Forced busy: either a short or long busy causes a reset because the tape control is unavailable for operation in either case (for a short busy sequence, even initial selection is terminated early).

Reset conditions described in items 2-6 and the rewind busy condition cause premature terminations to attempted command operations. In each case, the designated command cannot be executed and the TAU reset is generated to end the operation at the end of initial selection. (A halt I/O, item 3, may cause an early end to initial selection.)

Rewind or Ready End Control: Except for a ready drop condition, this turn-on of the TAU reset latch is the normal termination for most operations. The end tape operation line (Figure 2-16) generates set ends for read, write, or sense operations, and control end for control operations. Either end condition sets the channel end and/or the device end latch which activates the rewind or ready end control line (if tape unit ready is active throughout the operation).

The rewind at LP line causes a TAU reset during initial selection when rewind is designated because the rewind is unnecessary. The rewind hold latch causes a TAU reset when the selected tape unit deconditions ready, indicating the rewind has begun. The rewind command code is no longer needed in the command register.

Ready drop is an abnormal condition. If a selected tape unit drops ready, due to a malfunction or manual error, while performing a read, write, or control tape motion operation, the ready drop latch is set. Once ready drops, even for a short period, normal completion of the operation in progress is unlikely. Therefore, unit check, channel end, and device end are set to begin an end status in sequence, and the TAU reset latch is set to clear the command register and end the operation.

Force Burst Mode (FBM) and Operational In (Figure 2-11)

- Operational in is the tape control interlock line to the channel.

- FBM is turned on to force the channel to remain interlocked on the interface by controlling the operational in latch reset.

- The on state of the force burst mode latch turns on the operational in latch and prevents its reset, unless machine reset is active.

- The FBM latch is turned off when:
  1. a joint operation (performed by channel and tape control) is complete.
  2. the tape control and/or tape unit can complete an operation without the channel.
  3. an attempted operation cannot be executed.
  4. an interface reset is activated.

When the channel and a control unit must communicate, the interface selection control lines must be activated. A channel-initiated communication sequence is called initial selection; a tape control-initiated sequence is called a request in interrupt. During either sequence, the channel select out line and the tape control operational in line are activated to interlock both units on the interface.

Once communication is established, either unit can retain the interlock condition by maintaining the appropriate selection control line, select out by the channel or operational in by the control unit. (The channel can, however, override the interlock by generating an interface reset. See "Resets (Interface)."

Set FBM and Operational In

The tape control address in latch, turned on early in either interface selection sequence, turns on the FBM latch which turns on the operational in latch. Operational in to the channel is generated by the operational in latch.

The status gate turn-on to the FBM latch covers the remote possibility that the FBM latch may not be on if command chaining is indicated and a rewind command was issued when tape was already at load point. This turn-on circuit is required if the channel drops select out too early. Original circuit design assumed that operational in must be held active on the interface between chained commands; on some systems, the status gate turn-on to FBM prevents the loss of "operational in" if select out is lost.

Operational In Latch Reset Control

Whenever the 2415 Tape Control is involved in a selection sequence or data transfer operation, the FBM latch degates the operational in latch reset to retain the interface interlock until all communications are complete. Note that the reset AND circuit to the operational in latch is gated by not select out (Figure 2-11). Note also that force burst, from the FBM latch output, is OR'ed with select out from the channel.

Select out timing and the significance of the force burst line is shown more clearly on Figure 2-2; the select out OR is shown again (OI, 3C). When the

FBM latch is on, select out is forced; therefore, the operational in latch is not reset until after the FBM latch is reset.

FBM Latch Resets

Conditions for activating FBM latch resets (Figure 2-11) are:

1. Stop command: a command out response to any service in request indicates data transfer is stopped by the channel. With FBM off, the channel can end interface communication if it drops select out.
2. Reset force burst: the normal end operation reset to FBM. Green and go (TC idle state) is active after the TAU reset of the command register; service out 1 (service out delayed 1.8 microseconds) is the channel response to status in, usually for end status.
3. End test I/O: generated at the end of initial selection during which the test I/O is performed.
4. Reject status: a channel command out response to either initial or end status that indicates the channel cannot continue interface communication (stack status).
5. Halt I/O: an interface disconnect signal; the tape control must drop its interface interlock within 6 microseconds.
6. Control command started: a service out response to initial status when control command is designated; this occurs at the end of initial selection because the channel is not needed to complete the operation.
7. Machine reset: see "Machine Reset."

COMMAND REGISTER, DECODING, AND GATING (FIGURE 2-12)

- A command byte is stored in the nine-latch position command register.
- Command register entry is blocked if command byte parity is even.
- The on state of the command busy latch indicates a command is in the command register.
- A command operation cannot begin after initial selection, unless the command gate latch is turned on.

The command register is a storage device that consists of nine latches. These latches, P and 0-7, receive an odd parity command byte directly from bus out during initial selection. Command register outputs are routed to a series of AND gates that decode the command byte. Decoder outputs then condition circuits that execute the command if the decoded lines are gated.

Command Byte Parity: Before a command byte is set into the command register, it is set into the data register for a parity check. The odd byte line from the parity circuit must be active to allow the command byte to enter the command register. See the AI at the upper right of Figure 2-12. The command byte is set into the data register at the rise of command out; set command register rises at command out 1.

If command byte parity is bad (even), the set command register line is blocked. No operation can be performed at the end of initial selection because the command register will be empty.

Command Register P Bit: The P bit is useful in coding only the test I/O command. Since all other bit positions are blank for this command, the P bit distinguishes the test I/O command from an empty command register (command register off). The P bit is not used in decoding any other command and is not used for parity checking in the command register.

Command Busy Latch

Command busy is turned on at command out 3 time and remains on until the command register is reset. However, before the command busy is turned on, the latch off state (and odd byte) gates the command register set to allow entry to the command register. The on state blocks entry to the command register when the channel sends command out at any time other than initial selection command set. For example, a command out response to service in stops a write operation.

Another "not command busy" output gates idle reset (green and go) between command operations (Figure 2-9).

After a command is set into the command register and a valid command is decoded, command out 3 turns on command busy to condition the operating circuits.

Command Gate Latch

Execution of a command cannot begin until initial selection is complete and the command gate latch is turned on. Completion of initial selection is indicated when the status in latch is turned off and the command busy latch is on. The status in latch is turned off when the channel responds to initial status in. A service out response to status in is the channel signal for the TC to perform the command, unless it was completed during initial selection (such as test I/O).

A command out response signals the TC to stack the initial status byte and disconnect from the interface. As a result, only operations that do not require channel assistance can be completed (motion type control operations). A read, write, or sense command is terminated because the TC generates a TAU reset to clear the command register. In any case, the status in latch is turned off after the channel response to status in.

Counting: Because the tape unit is timing the 17-millisecond stop delay at the end of an operation, its counting line to the TC is active. This line is gated out by the TU only if it is selected. Therefore, if counting is active, the turn-on of command gate is delayed until the TU, selected for a new operation, completes the stop delay count.

Command Gating: Decoder outputs that begin an operation are gated only if the command gate latch is on. Ungated command decoder outputs are used during initial selection to determine whether a certain type of command can be performed, or are used only after the operation has begun.

Command Register Reset: Only a TAU reset can clear the command register. After the register is clear, the "command register off" line resets command busy which resets command gate. See "TAU Reset" for details.

CE Panel

Commands can be set into the command register from the CE panel during off-line operations; on-line operations can be duplicated.

DATA REGISTER (DR)

- DR contains 12 latch positions; only eight positions (5-12) are used for nonfeature operations.
- All 12 DR positions are used for data convert feature operations.
- DR inputs from the channel are gated by "set DR outbound."
- DR inputs for transmission to the channel are gated by "set DR inbound."
- Command bytes from channel bus out are set into the DR for parity checking only.
- Status, sense, and read data bytes from the 2415 TC pass through the DR for transmission to the channel over bus in.
- Address bytes bypass the DR.
- Write data bytes from channel bus out pass through the DR to the write circuits.
- Tape mark bits are forced into certain DR positions by TC circuits during write tape mark operations.
- The cyclic redundancy check character (CRCC) passes through the DR from the CRC register when the CRCC is to be written.
- Parity (P) bits do not enter the DR: bus out P bits set a P-bit trap latch (Systems 04.16) and condition the bus out parity circuit. Bus in P bits (generated by bus out parity circuit) are gated to bus in from the parity generator to bypass the DR.
- Special DR input/output gating for features is bypassed by panel jumpers if features are not installed.
- Basic DR resets are divided into two groups, 1-6 and 7-12, to accommodate the data convert feature.

All information bytes transferred between the channel and 2415 TC, except address bytes, pass through the data register. The command byte is set into the data register for parity checking only because the command register has no parity check circuit.

Data Register Parity Circuits

- Two parity circuits are conditioned by the DR.
- One parity circuit (Figure 2-13) parity-checks all bytes set into the DR from the channel, or generates P bits (when necessary) for bytes destined for the channel.
- Another parity circuit (Systems 01.04.28.1) parity-checks all bytes read from tape during read operations (data register VRC), or generates P bits (when necessary) for all bytes written on tape.
- Nonfeature DR operation was designed to use two parity circuits to simplify gating, and because feature operation requires the use of two circuits.

Figure 2-13 shows the parity circuit that checks all data bytes sent to the 2415 from the channel. A byte parity bit from the channel sets a P-bit trap latch whose output is compared with the data bits in the DR by the parity circuit. An even total bit count turns on the bus out check latch.

This circuit generates P bits (for odd parity only) for bytes set into the DR for transmission to the channel; this includes all status, sense, and read bytes. Parity bits read from tape are "trapped" by another trap latch and used by a second parity circuit for a data register vertical redundancy check only (read VRC).

For nonfeature operations, DR parity checking and generation can be performed by a single parity circuit, although gating circuits would be more complex. However, the prime purpose for using a second parity circuit concerns feature operations. When either data convert or seven-track translate is operative, a byte bit configuration entering the DR from the channel for a write operation, for example, will not be the same as the configuration gated to the write circuits. See Chapter 4 for feature data flow. Therefore, the same parity circuit cannot be used for both parity checking and P-bit generation simultaneously. The same type of condition exists (in reverse) for data read from tape during feature operations.

Data Register Inputs Outbound (Figure 2-14)

- Outbound gating is active for DR inputs that are outbound from the channel, or WTM or CRCC bytes to be written on tape.

- Bus out data inputs are jumpered directly when the data convert feature is not installed.

- The set DR outbound gate to DR positions 5-12 is active for:
  Write operations
  Write tape mark operations
  Initial selection command sets
  CRCC write time

Positions 5-12 of the DR are similar; Figure 2-14 shows DR position 7 as a typical example (to show all positions would be impractical). All input and output gates are shown in detail to present an overall view of DR controls.

The set outbound AND input to the DR7 latch is activated by the bus out data input gated by the common DR gate line "set data register outbound." The write TM input is used to degate the data AND only to DR positions that do not provide a 1 bit to write a tape mark.

Data inputs to each AND are modified according to the latch position function for each operation. For example, DR position 1 receives bus out 0 or 4 during data convert (DC) operations only; this DR position is not used for any other operation. DR position 7 data input shows DC inputs, the CRCC input, and the nonfeature bus out 2 input. Note that this input passes through a jumper wire that is removed if the DC feature is installed; the bus out 2 input is alternated with the bus out 6 input for DC feature operations only. Refer to Chapter 4.

Set Data Register Outbound is a common gating line to all outbound DR input gates; it is activated during:

1. Write operations: the data gate latch is set at the beginning of the operation (by first service in) and is gated by +S write. Each time the channel responds with a service out to a TC service in, the write in gate line is activated to set the new data byte into the DR.
2. WTM operations: every write clock 2, 3 pulse activates the outbound gate, but each data AND input is degated where necessary. See Figure IOP-15N, sheet 2.
3. Initial selection command set: a command out response to address in indicates a command byte is on bus out from the channel. This gate sets the command byte in the DR for parity checking before the byte is gated to the command register from bus out. (The command busy latch is not turned on until the byte is in the command register.)
4. Write CRC character time: active once at the end of a write operation to gate the CRCC into the DR from the CRCR (DR gates CRCC to the write circuits).

Data Register Inputs Inbound

- Inbound gating is active for DR inputs that are inbound to the channel from the 2415 TC.

- Read data from tape is jumpered directly to inbound gating when the seven-track (translate) feature is not installed.

- The set DR inbound gate to DR positions 5-12 is active for:
  Read operations
  Status byte during status in sequences
  Sense operations

Positions 5-12 of the DR are similar; see "Data Register Inputs Outbound." DR position 7 (typical example) is shown in Figure 2-14. The set DR7 inbound AND is conditioned by one of three common gating lines and the information byte inputs.

Set Data Register Inbound: Command gate lines to all inbound DR input gates are active during:

1. Read operations: a read clock (RC) 8 pulse is gated for read forward or backward operations only Data bits are gated directly from the read register for nonseven-track operation or from the read register through the translator first. (+S character

count 2-4 is always active without the feature.)

2. Status in sequences for an initial selection (initial) status byte: an end status burst mode sequence or an end status request in interrupt sequence that is gated by the gate status to data register line (bottom of Figure 2-14). DR position 7 receives the control unit (CU) end status bit from the CU end latch.

3. Sense operations: sense byte bit 2 information differs for each sense byte; the byte 1 AND is important because the three jumper inputs vary with the number of attached tape units. The jumpers are connected during system installation; they prevent false not ready indications for nonexistent tape units (note 6, Figure 2-14).

Data Register Outputs

- The DR latch OR output sends data to the write circuits directly or through the translator.
- The DR latch AND output sends data to channel bus in directly or the data is gated by data convert circuits.
- Both DR outputs also condition parity check and/or parity generator circuits.

Without any feature installed, both DR latch outputs are jumpered to route data into or out of the 2415 TC. See Figure 2-14, notes 3 and 4. Data entering the TC is routed from the OR half of the latch to the write circuits through the translator circuit with the seven-track feature installed. (A byte is altered with translate "on" or passed unchanged with translate "off.") If the DC feature is not installed, the latch output first passes through a jumper.

Data leaving the TC is routed from the AND half of the latch via a jumper directly to the bus in gating circuit or is first gated out by special circuits with the data convert feature installed. (The byte count 3 line is active if the data converter is off.)

DR Parity Checking: Both DR latch outputs condition parity circuits; see "DR Parity Circuits."

Data Register Resets (Figure 2-15)

- Basic DR resets, except the end operation (disconnect) reset, for all latch positions turn on the data register reset latch.
- Due to the data convert feature, basic resets are divided into two groups: latch positions 1-6 and latch positions 7-12.
- Each group of resets is OR'ed with the data convert reset controls that are gated for read or write operations.

The two upper inputs to the DR reset latch are feature inputs and are described in Chapter 4. Basic resets that set the latch are activated:

1. by read or write gates from the -S data register reset 1-6 line; two gates are generated for nonfeature operations (note the AND blocks without the DC notation).

2. by a stop command: a command out response to a TC service in request during a sense, write, or read operation.

3. for a stack status condition: a command out response to status in.

4. by a status reset: channel accepts status by responding with service out to status in.

5. by a write clock 15 pulse: this is generated after write disconnect.

A basic end read or write operation reset is gated by the on state of the stop delay latch and OR'ed with the DR reset latch output.

STATUS LATCHES (FIGURE 2-16)

- A byte of status information is sent to the channel during initial selection and during an end status in sequence.
- The initial or end status byte is assembled in the status latches.
- There are five basic status latches and two latches for busy status.
- Most status latches are turned off by status reset.

A byte of status information, indicating the basic status conditions of the TC and the selected tape unit, is sent to the channel when the TC is signaled to start a command, and after a command operation has been completed. These status bytes, referred to in this manual as "initial status byte" and "end status byte," are assembled in the status latches. (A short busy status in sequence bypasses the status latches with busy status; refer to "Initial Selection Sequence" in Chapter 3 for details.)

Status Bytes

An initial status byte normally contains only a P bit for a read, write, or sense operation; or only a channel end bit for control commands if an operation is to be performed. If an initial status byte contains any

other status bits, the command is not executed due to prohibitive conditions, such as a unit check (unless the operation was completed during initial selection). Therefore, the initial status byte provides the channel (and system control program) with no detailed information, unless the operation will not proceed. If pending (stacked) status for a previous operation is contained in the status latches, the performance of a new command is automatically precluded.

An end status byte, sent to the channel during an end status in sequence, indicates to the channel that an operation has been completed, and whether any unusual conditions occurred.

When other than normal end status bits are sent to the channel in a status byte, system programming sequences must initiate a sense command operation if the specific nature of an unusual condition, such as unit check, is required. Status bit information is general; sense bit information is specific.

Status Bits

A status byte from the 2415 Tape Control normally contains as many as six status (1) bits in byte positions 2-7. Positions 0 and 1 contain 0 bits. The only exception is the one-bit status modifier position during a short busy sequence if initial selection is rejected. Refer to "Initial Selection Sequence" in Chapter 3 for details. Status latch input conditions shown in Figure 2-16 are summarized in Figure 1-13, Chapter 1.

Status Latch Inputs

Status latches are not turned on by a common set line. Some inputs are gated during initial selection; others are gated while an operation is in progress; still others are gated at the end of an operation. A study of each command operation in Chapter 3 is necessary to understand the circumstances that signal specific status conditions. All status latch outputs are gated simultaneously into the data register during initial or end status byte sequences.

Status Reset

Status conditions, pertaining to a particular operation and tape unit, must be retained by the TC until the channel accepts the status byte, or until the channel activates a reset in the TC. The status reset line (Figure 2-6) is activated by the following:

1. A status in and service out sequence. The TC gates status to bus in, and the channel accepts with service out during an initial selection or end status cycle.

2. Machine reset activated by CE circuit resets, a general reset, or a selective reset.

DELAY COUNTER, WRITE CLOCK, AND SENSE COUNTER (FIGURE 2-18)

- Basic counter consists of 11 binary triggers.
- Write clock operation uses only the first four triggers (1, 2, 4, and 8) and runs in microsecond mode.
- When the counter functions as a delay counter, it runs in either millisecond or microsecond mode.
- When the counter functions as a sense counter, only the first three triggers are used and the counter is stepped by read clock RC7 pulses.
- Write microsecond mode generates write pulses and measures proper byte spacing on tape.
- Delay counter microsecond mode measures write check character and EOB delays.
- Delay counter millisecond mode measures time delays for starting and stopping tape.
- Sense counter outputs gate sense bytes.
- A counter check is indicated if the counter steps through 1536.

The write clock-delay counter consists of 11 binary triggers with appropriate control and drive circuits. This basic counter provides timed pulses for write operations, sense operations, end of block searching, and time delays. Millisecond time delays allow a tape unit to perform a mechanical operation such as starting and stopping tape motion. The counter runs in either the slow millisecond mode or the fast microsecond mode, depending on the delay required and the operation being performed.

Each binary trigger is complemented (changes state) by a positive input. Oscillators generate several frequencies; the proper frequency for the operation being performed is gated to the first binary trigger. Each positive shift in the oscillator drive complements the 1 trigger. When any trigger is turned off, a positive shift complements the following trigger.

Microsecond Mode

Microsecond mode oscillators are gated to the counter by either write condition or an end of block

search (reading function). Write condition also blocks the input to the fifth (16) trigger, so that only the first four triggers will run when the counter is used as a write clock. The write clock always runs in microsecond mode; it counts to 15 then repeats. A data byte (or character) is written for each write clock cycle.

Write disconnect overrides write condition (note, Figure 2-17) to gate turn-on of the fifth (16) trigger and to allow the counter to time the writing of the check character. End of block search causes the counter to run in microsecond mode, but the fifth trigger is not blocked because write condition is off; therefore, all positions of the counter are operating.

Millisecond Mode

Only a 5-kc oscillator is gated to the counter in millisecond mode when a delay is necessary to allow time for the tape unit to complete a mechanical action. Whenever a long delay period is needed, only millisecond mode and all counter positions are used.

Counter Check: The delay counter steps as far as 1536 only if there is a malfunction. Therefore, a count of 1536 causes a counter check (which sets unit check). See "Counter Check."

Sense Counter

During a sense operation, the counter is stepped each time the read clock, used for timing the delay between bytes, reaches 7. Counter outputs, decoded to activate counts 1-6 consecutively, gate the proper sense bytes to the channel.

Counter Oscillators

Three oscillators are used to generate the counter drive pulses. Outputs of the oscillators drive binary triggers; each trigger halves the frequency. For each operation, the proper frequency is gated to the drive by either mode. Millisecond mode always runs at 5 kc. During nine-track operations, tape density is always 800 bpi; the microsecond mode frequency is 240 kc. During seven-track operations, density can be 200, 556, or 800 bpi; the corresponding microsecond frequencies are 60, 167, and 240 kc.

Reset: When all oscillator drive gates are inactive, the 11 clock positions are held reset. With all binary triggers off, a basic gating line, WC DC off, is generated. This line is used extensively to signal that certain delays can begin, that certain delays are complete, or that the counter is idle. The counter-off line gates the green and go condition which generates idle reset.

WRITE TRIGGERS AND DESKEWING (FIGURE 2-18)

- There are nine write triggers, one for each tape track.
- Deskewing circuits correct skew by delaying the write pulse in each track the amount of time required to compensate for track circuit differences.
- A binary 1 is written when a write trigger is flipped.
- Deskewing delay pulses are generated by a three-stage counter.
- The LRC character is written at the end of tape block by resetting any write triggers that are on.

Write triggers are binary triggers that generate the write current shifts that cause bits to be written (magnetic flux reversals) on tape. Figure 2-18 shows one track circuit as a typical example; however, the tape control contains nine deskewing and write trigger circuits, one for each tape track. The deskewing circuits make it possible to delay the write pulses to each trigger separately, so that all bits in a byte are written with a minimum of skew. The nine write circuits in the control unit control the writing of all nine tracks in the selected tape unit. By adjusting the delay lines associated with the tape unit select lines (during maintenance), the proper write pulse delay is selected for each trigger according to the tape unit selected. Delay line taps must be adjusted for as many as six tape units in all nine-track circuits.

Writing a Bit on Tape (NRZI)

Each write trigger output is routed through a line driver and amplifier to the corresponding coil in a tape unit write head. Current flows in the write head coil whenever write status is active. Each time the state of a write trigger is changed, the coil current is reversed and a 1 bit is written on tape. A coil current change causes a magnetic flux reversal on tape. For a binary 0, the write trigger is not "flipped" and the binary 0 is represented on tape by the absence of a flux reversal. (This method of coding 0 and 1 bits is called the NRZI method of recording.)

For any operation other than a write, WTM, or erase gap, the write triggers are held reset. To write data, a tape mark, or the CRC character, write pulse is AND'ed with a bit from the data register to flip the trigger. Write pulse is always later than the bit from the data register, and therefore, controls the time when the write trigger is flipped and

the bit is written. By delaying the write pulse, the time the 1 bit is written is controlled and excessive skew write is eliminated.

Deskewing Delay Counter

To write data, the write pulse latch is set at WC3. The output of the latch controls a three-stage counter which generates a series of write pulses (waveforms, Figure 2-18). The particular pulse which provides the proper length delay in each track for each TU address is sent through a jumper to the write trigger input circuit. (The counter and write pulse latch are common to all nine trigger circuits.)

The counter is held reset when the write pulse latch is off; when the latch is set at WC3, the counter is allowed to step. The output of the write pulse latch is AND'ed with deskew drive which sets and resets the counter drive latch in microsecond mode. Deskew drive is generated by the same oscillator that drives the write clock, so that the counter steps in synchronism with the write clock. The output of the counter is decoded to provide seven different delays in increments of 2 microseconds. The decoded outputs of the counter are fed back to latches A, B, and C, and the latches step under control of the even and odd outputs of the counter drive latch. The decoded count 8 output resets the write pulse latch.

Writing Check Characters

The CRC character, generated in the CRC register and gated into the data register, is written at 267 microseconds of the write disconnect delay. A CRC character bit in the data register is AND'ed with a counter delay line to generate a write pulse just as is done to write data, except the write pulse latch is set during the write disconnect delay.

The LRC character is written in an entirely different way. The LRC requires that the total number of bits in any track (including the CRC and LRC characters) be an even number. If a write trigger has been flipped an odd number of times when the data and CRC characters have been written, the trigger is turned on. Therefore, the LRC character can be written simply by resetting any trigger that is on at write LRC time (write disconnect delay 543 microseconds). This is performed by AND'ing the output of the write trigger with the write check character and write pulse, and feeding it back to the write trigger input.

CYCLIC REDUNDANCY CHECK REGISTER (FIGURE 2-19)

- Consists of nine latches and input gating.
- Characters are shifted each WC3 time and set into the CRC register at WC4, 5 time.
- All bytes of a data block are combined in the CRC register to form one CRC character.
- The CRC register is given an extra shift just before writing the CRC character.
- All CRC register positions, except 2 and 4, are inverted before writing.
- CRC is written at 267 microseconds of write disconnect delay.

The cyclic redundancy check (CRC) register consists of nine flip latches (-TO and +TA) and their input gating. The register positions are P and 0-7. The CRC characters are generated by combining the outputs of the data register with the outputs fed back from the CRC register in exclusive OR circuits. The exclusive OR's create conditions to shift the characters into the input latches at WC3 time of each write clock cycle. At WC4, 5 time, the characters are set into the CRC register. After a block of data is written, the character remaining in the CRC register is gated into the data register at CRC time and written on tape.

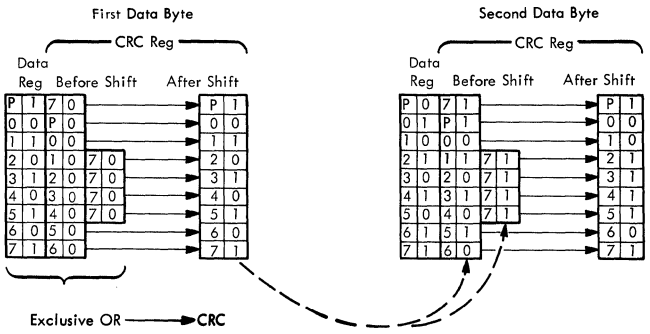
CRC Character Generation

In the chart at the lower left of Figure 2-19, inputs on the left are exclusive OR'ed with the present status of the CRC register positions in the center to determine which CRC register positions will be changed at shift CRC time (WC3). In the cases of CRC register positions P, 0, 1, 6, and 7, any one and only one of two conditions active (output of data register and output of one CRC register position) sets the corresponding CRC register latch. (Active means a 1 bit is present.) In the case of positions 2, 3, 4, and 5, any one or all three conditions active (output of data register and output of two CRC register positions) sets the corresponding CRC register latch. This is accomplished by exclusive OR'ing two of the three conditions and then exclusive OR'ing the result with the third condition. Any CRC register latch that is not set at set CRC time (WC4, 5) is reset.

As each data byte passes through the data register to the write triggers, it also enters the CRC register. Between the data register and the CRC register is a group of exclusive OR (OE) circuits. The data register outputs are one set of inputs to the OE circuits, and CRC register feedback forms the other inputs. The outputs of the OE circuits are gated into the input latches by a shift CRC pulse at WC3 time. At WC4, 5 time, the character in the latches is set in the CRC register. The new character in the CRC register is a combination of the character received from the data register and the last previous character in the CRC register. The first character of each block passes unchanged through the OE circuits and into the CRC register. When there is a character in the CRC register, the incoming character from the data register is changed.

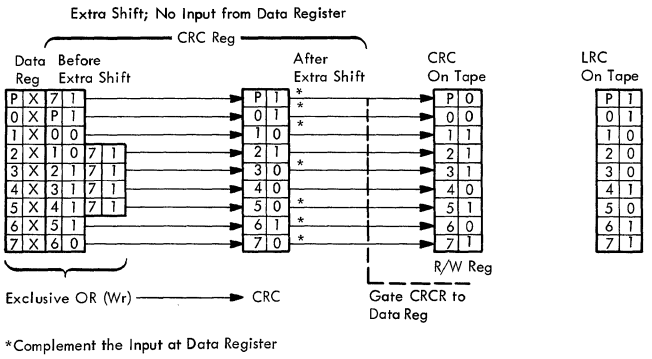
Positions 2, 3, 4, and 5 have three-way OE circuits. The outputs from these OE circuits are active when any one or all three inputs are active; that is, an odd number of inputs causes an output. Positions P, 0, 1, 6, and 7 have two-way circuits. One and only one input causes an output.

The following is an example of CRC register operation during write. In this example, two data bytes are shifted into the register and written on tape. Data bytes used in the example are 101 010 101 and 010 101 011. The CRC character written on tape is 001 110 101:



Writing the CRC Character

At the end of a write operation, the CRC character is given an extra shift with no inputs from the data register at 63 microseconds of the write disconnect delay. The CRC character is set into the CRC register at 96 microseconds of the delay. This extra shift is necessary so that the tape written by a 2415 can be used on machines that read the CRC for error checking and correction. A read operation normally has one more shift than a write operation because reading the CRC causes a shift. To use the CRC for checking, the character count must be the same for reading and writing. Therefore, the 2415, which does not use the CRC for checking, causes an extra shift for compatibility with other machines. As a result of the extra shift, the following occurs:



*Complement the Input at Data Register

To write the CRC character, the CRC register is gated into the data register at CRC time (130 microseconds of the write disconnect delay). Positions 2 and 4 are entered directly into the data register but all other positions are inverted. If all positions are entered directly, the LRC character is blank. In a read backward operation, reading will not begin correctly unless an LRC character is read. Inverting part of the CRC character assures that there will always be 1 bits in the LRC character. The CRC character is sent to the write triggers and written on tape at 267 microseconds of the write disconnect delay. The CRC character is written four character spaces after the last data byte and four character spaces before the LRC character.

READ CLOCK AND DRIVE (FIGURE 2-20)

- Read clock is a four-stage binary counter.
- Read clock is started when the first bit in a byte is read.
- The clock counts to 10 during a read operation and to 12 during a read check of a write operation.
- During a sense operation, the read clock times the spacing between sense bytes.

The read clock is a four-stage binary counter that generates timed pulses used in processing data through the tape control unit. It also generates the pulses necessary to time sense bytes sent to the channel.

The read clock runs in microsecond mode; it starts when the first bit of each byte is sensed. The read clock is run during a write operation to allow a read check of written data.

First Bit Latch

Because skew occurs, all the bits in a byte are not read simultaneously; the first bit of each byte read from tape sets the first bit latch, which starts the read clock. The first bit latch, reset at either RC10 or RC12, resets all four positions of the counter (normally, before bits of the next byte arrive).

Outputs from the final amplifiers for all nine tracks are routed to the first bit OR gate. The bit in the byte that is read first conditions the turn-on AND gate (via the OR) to set the first bit latch. Each first bit is gated by RC off and the data gate latch to set the first bit latch. RC off ensures that all four stages of the counter are reset and "settled down" before the clock is started by the next first bit. Data gate is turned on after 4 milliseconds of the start delay and remains on throughout the data block until stop delay time.

READ REGISTER (SYSTEMS 01.03.52.1)

- RR consists of nine latches.
- Bits of each byte read from tape passes through final amplifiers and are gathered in read register.
- RR routes each byte to data register and LRCR register during read operations.
- RR routes each byte only to LRCR during write operations.
- RR VRC is signaled during write operations only.

As each bit is read from tape, it is amplified and shaped (see "Final Amplifier and Clipping Level," Appendix B), and set into its corresponding read register position. The read register, which contains nine latch positions (Systems 03.52, 03.54, and 03.56), acts as a buffer where 1 bits are assembled as a byte is read from tape. Because each byte contains a small amount of skew, a delay is needed to allow enough time to assemble the entire byte in the register. Each first bit of a byte is routed directly from the final amplifiers to start the read clock. A byte is not moved out of the register until RC8 time (about 29 microseconds after first bit) during read command operations.

Register Outputs

During read command operations, read register outputs are routed:

1. Directly to the data register, or through the translate circuits then to the data register, from which data bytes are transferred to the channel; the RC8 data register set pulse is blocked for write or spacing operations.
2. To the LRC register for an LRCR check at the end of the tape block. (No set pulse used; RR latch outputs set LRCR latches directly.)

Vertical redundancy checking (VRC) of read bytes is performed at the output of the data register, not the read register.

During a read check of a write operation, read register outputs are routed to the:

1. Read register VRC circuit to allow a parity check of each byte written earlier in the operation.
2. LRC register for an LRCR check at the end of the block.

Data is not sent to the data register for parity checking because the DR is used to process write data to the tape unit.

RR Reset: The RR is reset every RC9 pulse after each byte is assembled. The RR is held reset whenever the data gate latch is off.

LONGITUDINAL REDUNDANCY CHECK REGISTER (SYSTEMS 01.03.64)

- Longitudinal redundancy is a check of the longitudinal parity of each track in an entire tape block.
- The longitudinal redundancy check register (LRCR) contains one binary trigger for each of the nine tracks.
- The triggers are complemented each time a bit is read in the corresponding track.
- At the end of a block all triggers should be off.

Longitudinal redundancy checking is a method of error detection that checks the longitudinal (lengthwise to the tape) parity of each track in a block. The total number of bits in any track of a block should be even. During read or read check operations, LRCR triggers turn on or off for each 1 bit in the corresponding track. At the end of the block, all the triggers should be off. If any LRCR trigger is on after the LRCC is read, an error is indicated.

Write LRCC

The LRCR has nothing to do with the creation of the LRC character during a write operation. An LRC character is generated by resetting the tape control write triggers left on after the last byte is written. If the total number of bits written in a track (including the CRCC) is odd, the write trigger will be on at write LRCC time. The write trigger is reset to write a bit in the LRCC. If the bits in the track are even, the write trigger is off at LRCC time and no bit is written in the LRCC for that track.

Read LRCC (Read or Read Check of Write Operations)

When the tape block passes the read heads, each bit complements a trigger in the LRCR. Since the triggers started from a reset condition, they should be off after an even number of bits. If each complete track including both check characters has an even number of bits, the LRCR will be blank at the end of the block.

A checking circuit samples the LRCR during read disconnect time. If no register latches are on, the LRCR error latch is not turned on; one or more latches left on in the LRCR signals an error. The LRCR error latch on also turns on the data check and unit check latches.

TAPE MARK RECOGNITION (FIGURE 2-21)

- A tape mark (TM) is a block of two identical characters, the TM and its LRCC. In nine-track format, each character contains bits 3, 6, and 7; in seven-track format, each character contains bits 9, 10, 11, and 12 (BCD 8, 4, 2, and 1).
- Tape mark recognition is active during all read type operations, both forward and backward.
- A byte of data may have the same bit configuration as a tape mark.
- A data byte with the configuration of a tape mark is identified as a true tape mark only if it has the spacing of a tape mark block.
- Unit exception is set if a tape mark is recognized during a read or a space block operation, either forward or backward.
- A tape mark (when recognized) is never transmitted to the channel.

A tape mark is written on tape whenever the system program issues a WTM control command, usually to indicate the beginning and end of a group of related data blocks. During subsequent read operations, the tape mark must be recognized. A true tape mark consists of a block of two identical characters; these characters are the tape mark character and its LRC character, separated by four character spaces. It is possible for the LRC or the CRC character following a block of data, or for a data byte, to have the same configuration as a tape mark character.

Tape mark recognition circuits must recognize true tape marks but must allow the tape unit to pass over check characters or data bytes that have the same configuration as a true tape mark. Characters on tape which have the configuration of a tape mark are recognized as true tape marks only if they have the proper spacing for a tape mark block.

During a read, read backward, forward space block, or backspace block operation, recognition of a tape mark block signals a unit exception status condition. An important function of the tape mark recognition circuit is to recognize a tape mark and terminate a forward or backward space file operation. Unit exception is not set for file operations. Because a data byte can appear to be a tape mark, the circuit measures the space between bytes to identify true tape marks. A tape mark consists of two characters that read the same forward or backward, with seven character (byte) spaces between them for nine-track and three spaces between them for seven-track operations. If the first byte of a block with the configuration of a tape mark is read and a second byte is read one character space later, the block must be data and not a true tape mark.

The tape mark recognition circuit controls the transmission of the first data byte to the channel during a read or read backward operation. When the first bytes of each block are read, the tape mark recognition circuit must determine whether the block is a tape mark or data. If it is a tape mark, service in is blocked. If it is a block of data and the first byte read has the configuration of a tape mark, data transmission to the channel is blocked until the block is identified as data.

For a read forward operation, the block is identified as data if the first two bytes read are one character space apart; and as a tape mark if the bytes are separated by at least three blank spaces. For a read backward operation, the identification is more complicated because there are four possible nontape mark combinations of check characters and data:

1. Nine-track format with LRCC and CRCC.
2. Nine-track format with LRCC but a blank CRCC.
3. Seven-track format with LRCC.
4. Seven-track format with a blank LRCC.

The following steps are used to identify a tape mark. See Figure 2-21.

Seven-or Nine-Track Forward

1. Start delay sets the first character latch.
2. First bit starts the read clock.
3. Tape mark sample checks the first data byte at RC9-1 (via the seven- and nine-track forward and seven-track backward block).
4. If the byte has the configuration of a tape mark, the tape mark latch is set.
5. At RC9-2, the first character latch is reset via the seven- or nine-forward block.

6. If the byte was data, another byte follows one character space later; and the tape mark latch is reset at RC2, 3 of the second byte read clock cycle (by the TM data AND gate).

7. If the byte was a true tape mark, the next byte is either four or eight character spaces later; and the read disconnect latch is set at EOB 2.3 characters.

8. Read disconnect prevents resetting the tape mark latch at RC2, 3 of the cycle when the LRCC is read. The on state of the tape mark latch blocks generation of service in.

Nine-Track Backward

Nine-Track Backward with Blank CRCC

1. With a blank CRCC, there are seven character spaces between the LRCC and the closest data byte; there will always be an LRCC.

2. Start delay sets the first character latch.

3. First bit starts the read clock when the first bit of the LRCC is read; the tape mark sample is not generated because the data time latch is off.

4. Data time is set after six character spaces.

5. The read clock is started when the first bit of the first byte after the LRCC is read.

6. At RC9-1, the nine-track backward block conditions tape mark sample and sets the seven- and nine-track backward latch.

7. If the byte has a tape mark configuration, the tape mark latch is set.

8. At RC9-2, the first character latch is reset.

9. If the byte was data, another byte follows one character space later; and the tape mark latch is reset at RC2, 3 of the second byte by the TM data AND.

10. If the byte was a true tape mark, no byte follows and the read disconnect latch is set at EOB 10 characters.

Nine-Track Backward with CRCC

1. There will always be an LRCC for nine-track backward operations. There are three character spaces between the LRCC and the CRCC, and three character spaces between the CRCC and the closest data byte.

2. Start delay sets the first character latch.

3. First bit starts the read clock and turns on the character counter when the first bit of the LRCC is read.

4. When the CRCC is read, first bit of the CRCC turns off the character counter and starts the read clock. Data time is set at RC10 time through the nine-track backward block too late to take a tape mark sample at RC9-1 time. When the next byte (first data byte) is read, a tape mark sample is taken at RC9-1 (via the nine-track backward block). The seven- and nine-track backward latch is also set at this time.

5. If the byte has a tape mark configuration, the tape mark latch is set.

6. At RC9-2, the first character latch is reset.

7. If the byte was data, another byte follows one character space later; and the tape mark latch is reset at RC2, 3 of the second data byte by the TM data block.

8. If the byte was a true tape mark, no byte follows and the read disconnect latch is set at EOB 10 characters.

Seven-Track Backward

Seven-Track Backward with LRCC

1. There are three character spaces between the LRCC and the nearest data byte. A CRCC is not used in seven-track operations.

2. Start delay sets the first character latch.

3. When the first bit of the LRCC is read, first bit starts the read clock.

4. At RC9-1 time, a tape mark sample is generated.

5. If the LRCC has the configuration of a tape mark, the tape mark latch is set.

6. At EOB 2-3 character time, the data time and seven- and nine-track backward latches are set.

7. When the next byte (first data byte) is read, first bit starts the read clock.

8. A tape mark sample is again taken at RC9-1.

9. The first character latch is reset at RC9-2.

10. If the byte was data, another byte follows one character space later; and the tape mark latch is reset at RC2, 3 of the second data byte by the TM data block.

11. If the byte was a true tape mark, no byte follows and the read disconnect latch is set at EOB 6 characters.

Seven-Track Backward with Blank LRCC

1. Start delay sets the first character latch.

2. When the first byte (data) is read, first bit starts the read clock and flips the character counter.

3. At RC9-1, a tape mark sample is taken.

4. If the byte has the configuration of a tape mark, the tape mark latch is set.

5. When the second byte is read, the first bit starts the read clock and flips the character counter. At RC2, 3, the data block is conditioned. (The seven- and nine-track backward line is not minus until the data time and seven- and nine-track backward latches are set.) The data block resets the TM latch and

first character latch. The force data time seven-track line sets the data time latch which, in turn, sets the seven- and nine-track backward latch. The seven- and nine-track backward line deconditions the data block.

ERROR DETECTION

- A unit check status bit is usually indicated when an error has occurred.
- Specific error conditions are indicated by sense bits.
- Errors are indicated by red lights on the CE panel.
- Data and equipment checks indicate more than one type of error condition.
- Twelve error conditions are recognized in the 2415 Models 1-3.
- Data convert check is not an error condition. See Chapter 4.

The error conditions and operations involved are listed in Figure 1-12. Error latch diagrams, Figures 2-22 to 2-34, are located on reference pages in the maintenance diagram volume.

Data or Equipment Check

A group of four data errors are indicated collectively as a data check. These four errors (skew, data register, read register, and LRC register) cause a data check sense bit to be sent to the channel in sense byte 0, and cause the individual sense bit to be sent in sense byte 3.

An equipment check is a collective indication of two error conditions: C-compare check and counter check.

Read Parity Check

The sequence for a single byte during a read operation is:

1. Complete byte, including parity, is loaded into the read register.
2. Gate data bits from the read register to the data register (and LRCR).
3. Gate parity bit from the read register to the read P-bit trap latch.
4. Check even-odd count of data register contents (Systems 04.17) and inject parity bit on bus in.
5. Check even-odd count of data register contents (Systems 04.28) and compare with contents of read P-bit trap to determine whether parity is correct.

A service out 1 (not service out) pulse clears the previous byte from the data register and read P-bit trap. At RC8 time, the eight data bits are loaded into the data register and the parity bit is loaded into the binary trigger (read P-bit trap).

Inject Parity: The data register contents are checked for even or odd number of logical 1 bits in the bus in parity inject circuit (Systems 04.17). An even number of 1 bits in the data register generates +S even count, and the bus in P bit is active; a logical 1 parity bit is injected into the byte on bus in. An odd number of 1 bits in the data register fails to generate +S even count, and the bus in P bit is inactive; a logical 0 parity bit is injected into the byte on bus in.

Check Parity: The data register contents are also checked for even or odd number of logical 1 bits in the read parity check circuit (Systems 04.28). An even number of 1 bits in the data register generates an active inject P signal output. Inject P (+ and -) is compared with the + and - outputs from the read P-bit trap. If inject P is active (indicating the byte should have one P bit) and the read P-bit trap indicates the received byte did not have one parity bit, -S set data register VRC is gated. At RC10, the data VRC latch is set to indicate an error condition.

A C-compare check is not a parity check during read operations. Refer to "C-Compare Error."

Write Parity Check

Inject Parity

The P bit from each data byte on bus out from the channel is stored in the bus out P-bit trap at the same time the eight data bits are stored in the data register. The write parity inject circuit (Systems 04.28) inspects the data register contents for even or odd number of logical 1 bits in the byte, and generates an active inject P signal if the byte contains an even number of ones.

The +S inject P line is sent to the write trigger along with the eight data bits from the data register. Write clock timing sets (writes) the parity and data information into the write triggers at WC3 time.

Check Parity

Each byte is checked for correct parity in two separate circuits using two different methods. A separate error condition is set if either circuit detects a parity error.

Bus Out Check

The bus out check circuit compares the data register contents with the bus out parity bit stored in the bus out P-bit trap. The bus out parity check circuit (Systems 04.17) compares the nine input bits with exclusive OR circuits (review Figure 2-13). Since the byte has an odd number of 1 bits when parity is correct, +S even count indicates an error. The bus out check latch is set by even count at service out 2 not 1 time to indicate the error condition.

C-Compare Check

The C-compare check circuit is also a parity check during write operations; it compares the inject P signal with the parity bit stored in the bus out P-bit trap. However, a bus out check takes precedence over C-compare. Refer to "C-Compare Error."

Command Reject (Figure 2-22)

Command reject indicates that the control unit has received a write type command it cannot perform because tape is file-protected; this includes a write, write tape mark, or erase gap. Also, a data convert "on" mode set command is received when the tape control does not have the data convert feature installed. A reject is not signaled for a command it cannot perform because of an invalid command code.

Command reject, which occurs during initial selection, is indicated by sense byte 0, bit 0, and a unit check status bit in the initial status byte.

Bus Out Check (Figure 2-23)

Bus out check indicates that either a command byte or a write data byte had incorrect parity. The parity error may have occurred on bus out or in the data register.

A bus out check during initial selection blocks performance of the designated operation. Correct parity of the command byte is a prerequisite for loading the command into the command register. Bus out check, for bad command byte parity, is indicated by a unit check status bit in the initial status byte.

A bus out check for bad parity data bytes during a write operation is indicated by a unit check bit in the end status byte after a write operation. The on state of the but out check latch is indicated by sense byte 0, bit 2.

Skew Error (Figure 2-24)

During a write or write tape mark operation, each byte is checked for excessive skew as it passes over the read head. A limit is placed on the time that can elapse between the reading of the first and last bits in a byte. If any bits are sufficiently out of line to exceed this "byte gate" limit, a skew error condition is set.

When the first bit of a byte sets the first bit latch to start the read clock, the skew gate latch reset line is deconditioned. All bits of a byte should be read by RC5 time, when the skew gate latch is turned on. If a bit is read after RC5 and before RC10 when the first bit and skew gate latches are reset, the skew check latch is turned on. Any bits read between RC5 and RC10 represent:

1. Lagging bits of the byte which started the read clock, indicating excessive skew, or
2. First bits of the following byte, indicating that bytes were written too close together and/or excessive skew.

A skew check is indicated by sense byte 3, bit 2, and a data check which is sense byte 0, bit 4. A unit check status bit is included in the write operation end status byte.

Word Count 0 (Figure 2-25)

Word count 0 indicates that a write operation has been terminated before any data was written on tape. After initial selection, when the tape control sends its first service in, the channel should respond with service out and a byte of data. If the tape control sends command out, the write operation must be terminated immediately. The word count 0 latch is set when the stop on write first character line begins the end status in sequence.

Word count 0 is indicated by sense byte 0, bit 6, and a unit check bit in the end status byte.

Counter Check (Figure 2-26)

When the write clock-delay counter steps to 1536, a counter check error occurs. The delay counter is always stopped before count 1536 during a normal operation. Counter check, then, indicates a malfunction in the counter or in one of the circuits that controls counter stepping and resets.

A counter check is indicated by an equipment check, sense byte 0, bit 3, and a unit check status bit. No individual sense bit is provided for a counter check error.

Interblock Gap Noise (Figure 2-27)

Interblock gap (IBG) noise indicates that the gap or an erased area has not been erased completely. During a write or write tape mark operation, the read head checks the IBG during the start delay for any bits with enough amplitude to be read. During an erase gap operation, the tape is checked from the beginning of tape motion until the beginning of stop delay time.

If noise bits are detected, the interblock gap noise latch is set and a noise check is indicated on the CE panel; but the status byte will not contain a unit check bit. The channel is notified of noise only when a 0 bit is in sense byte 1.

Ready Drop (Figure 2-28)

The AND gate used to control the setting of the ready drop latch blocks ready drop during sense, rewind, and rewind-unload operations. Ready drop checking is used only during write, write tape mark, erase, and read type operations: read, read backward, forward space file and block, and backspace file and block.

During these operations, the inactive -S ready line indicates that the selected tape unit became not ready during the operation. This condition occurs because of broken tape, or loss of power or malfunction of the tape unit, or operator intervention.

Setting the ready drop latch activates set ends. This signal generates channel end and device end. Device end and unit check (also activated by ready drop) generates a "rewind or ready end control." The operation is terminated (refer to "End Status -- Burst Mode" in Chapter 3), and the channel end, device end, and unit check status bits are set. No sense bit is indicated.

Rewind hold is set during rewind and rewind-unload operations. Loss of ready during one of these operations will not set ready drop, but rewind or ready end control is activated to end the operation.

Overrun (Figure 2-29)

During write operations, overrun indicates the channel did not repond to a service request within the allotted time. During read operations, overrun indicates the channel did not accept the byte on bus in within the allotted time. The time is critical because the bytes are recorded on the tape at consistent intervals, and the tape moves at a constant speed.

Write Operations: The tape control requests a data byte from the channel by sending service in tag (at WC8 time). This line complements (sets) the overrun binary trigger. The channel must respond with a byte of data and service out soon enough so that delayed service out 1 occurs prior to WC2, 3 time. If service out 1 is not active, WC2, 3 is gated to set the overrun latch. If service out 1 is active, the overrun binary trigger is reset and WC2, 3 is blocked.

Read Operations: The tape control places a data byte on bus in and signals the channel by sending service in tag (at RC10 time). Service in tag sets the overrun binary trigger, which must be reset by service out 1 prior to RC7 time to block the setting of the overrun latch.

An overrun error is indicated by sense byte 0, bit 5, and a unit check status bit in the end status byte.

Data Register VRC (Figure 2-30)

A data register VRC check indicates that data in the data register during a read or read backward operation is not in correct vertical parity. During a nine-track operation, vertical parity must always be odd. Parity can be either odd or even during a seven-track operation, depending on the mode register setting.

The data (register) VRC latch is indicated by sense byte 3, bit 0, and data check, which is indicated by sense byte 0, bit 4. A unit check bit is included in the read operation end status byte.

Read Register VRC (Figure 2-31)

A read register VRC is a check for vertical parity of data bytes during a write operation only. When the bytes that have just been written pass over the read heads, they are read into the read register and checked for correct vertical parity. During nine-track operations, parity must always be odd. Parity can be either odd or even for seven-track operations, depending on the mode register setting.

The read register check latch is indicated by sense byte 3, bit 4, and a data check which is sense byte 0, bit 4. A unit check bit is included in the write operation end status byte.

Longitudinal Redundancy Check (LRC) (Figure 2-32)

An LRC check is made during a write, write tape mark, read, or read backward operation to ensure that each track in a tape block, including the CRC and LRC characters, contains an even number of bits. The LRC register contains a binary trigger for each of the nine tracks. Each bit, read in a track during read or write type operations, changes the state of the trigger; the trigger should be off after a block is read if the track contains an even number of bits.

Any trigger that is on at the end of the operation gates the setting of the LRCR check latch during read disconnect time. An LRCR check is indicated by sense byte 3, bit 1, and a data check which is sense byte 0, bit 4.

C-Compare Error (Figure 2-34)

A C-compare is a check of data transmission between the read register output and data register output during a read operation, and a parity check of the data register output and bus out P-bit trap latch during a write operation. Its purpose is to check operation of the equipment; it is not a primary parity check. A bus out check or data check (VRC, LRC, or skew error) takes precedence over C-compare by holding the C-compare check latch reset.

Read C-Compare

During a read operation, each byte must have the same parity in the data register that it had in the read register. If the one-bit count of a byte in read register positions 0-7 is odd, the C-compare TB is turned on. The odd byte line from the data register parity circuit for the same byte must turn off the TB, or the C-compare check latch is set at RC2, 3 of the next read clock cycle. If only the data register or only the read register signals an odd byte, the TB is turned on and signals a C-compare at the next RC2, 3.

A read C-compare is actually an exclusive OR comparison of the outputs of two parity circuits. If the outputs differ, C-compare is set; if the outputs are the same (both signal odd or even), C-compare is not set.

Write C-Compare

When data passes through the TC during write operations, only one parity check point (data register output) is available as bytes move to the TU. Therefore, C-compare is used as a parity type check, instead of a compare check, using the bus out P-bit trap latch and the write parity inject parity circuit.

A data byte is loaded into the data register and the bus out P-bit trap latch by the service out tag. The eight data bits in the data register are checked for even or odd parity by the write parity inject circuit (Systems 04.28). At service out 1 not service out time, the C-compare binary trigger is complemented (set) by +S adjust P bit if the data register contains an odd number of 1 bits (no parity bit needed; -S inject P signal is inactive). At WC3 time, the C-compare binary trigger is complemented again if the bus out P-bit trap is empty (+S character step C-compare write). Strobe is on during WC7 time. If the C-compare binary trigger is complemented twice (odd number of bits in DR and no P bit) or not at all (even number of bits in DR and a P bit in the trap), strobe is degated and C-compare check is not set.

DR 1 Bits	Binary Trigger (Service Out)	P Trap	Binary Trigger (WC3)	Strobe (WC7)
Odd	Complement	Empty	Complement	-----
Odd	Complement	Set	----------	Error
Even	----------	Set	----------	-----
Even	----------	Empty	Complement	Error

Seven-Track Write C-Compare

During seven-track nontranslate write operations, bus out 0 and 1 are not transmitted to the TC. The channel, however, can place bits on bus out lines 0 and 1. For this reason, bus out P, 0, and 1 must be checked instead of only the P bit to determine whether lines 2-7 are odd or even. If lines 0 and 1 remain off, the P bit indicates 2-7 parity. If line 0 or 1 contains a bit, the circuit is adjusted to represent the parity of 2-7 only, the portion transmitted to the TU.

During nine-track or seven-track convert, only the P bit is needed for the C-compare circuit because all positions of the bus out lines are used. A P bit indicates that lines 0-7 are even. No P bit indicates that lines 0-7 are odd.

During seven-track data convert feature operations, the parity compare is made once for every four characters (24 bits) processed. Refer to "Data Convert Theory of Operation" in Chapter 4.

A C-compare error is indicated by sense byte 3, bit 7, and an equipment check which is sense byte 0, bit 3. A unit check bit is included in the end status byte.

This chapter of the manual provides a description of the sequence of machine functions necessary to perform a complete operation. All commands are described as complete operations, except for the beginning and ending sequences. Each command operation is begun by the same sequence called initial selection and is terminated by one of two ending sequences: end status burst mode or request in interrupt.

The reader should be familiar with the contents of Chapter 2 before studying this chapter which is mainly concerned with over-all data flow and control of specific operations; Chapter 2 provides detailed descriptions of specific circuits and how they are used for all operations.

INITIAL SELECTION SEQUENCE (FIGURES IOP-1, IOP-2, AND IOP-3)

- All command operations are begun by an initial selection sequence.
- Initial selection is begun when the channel sends the combined I/O address of a control unit and I/O device on the bus out lines and activates address out.
- The channel activates select out to select the addressed TC and TU.
- TC must bypass (regenerate) the select signal if it cannot accept the signal or if the channel is addressing another control unit.
- TC must reply with an immediate short busy sequence, if it is addressed while busy with an operation or holding "old" status for another TU address.
- If neither a bypass nor busy sequence occurs, an address in sequence is begun and TC activates operational in to interlock the channel.
- TC returns the same address byte to the channel on bus in and signals address in.
- Channel responds with a command byte and signals command out.
- TC decodes the command and determines whether the operation can be performed.
- TC advises the channel of status conditions by sending a status byte on bus in and activating status in.
- TC begins the operation if status conditions permit and if the channel accepts the status byte; otherwise, some operations are blocked when TC disconnects from the interface.

Initial selection is the interface signal sequence by which the channel begins an I/O operation with the tape unit (TU) through the tape control (TC), or just a control unit. Regardless of the command operation designated, the basic initial selection signal sequence is standard (only the resulting control unit action varies with the intended operation).

General Reset: Before the channel begins any I/O operation, it must raise the operational out selection control line to decondition general reset in all control units on the interface. When active, operational out releases machine reset in the 2415 TC.

Channel Addresses Tape Control (Figures IOP-1, 3-1, and 3-4)

- To address TC, the channel places a combined TC and TU address byte on bus out to all attached control units.
- Channel activates address out tag to indicate an I/O address is on bus out.
- To select designated TC, the channel activates select out and hold out.
- If addressed TC cannot accept selection, select signal must be propagated (bypassed).
- If addressed TC is busy, it must accept the select signal and perform an immediate short busy status in sequence and disconnect from the interface.
- If addressed TC can continue the initial selection sequence, the select signal is trapped and TC address selection begins.

A TC address is assigned at the time of installation; each control unit on the interface must have a different address, so that only one control unit at a time can respond to channel selection. The device portion of the address designates one of the six tape units available to the 2415 TC.

2415 TC Address Decode

Address bits 0-4 condition the TC address decoder (Figure IOP-1, coordinate C2) to decode its address. Address out tag followed by select out from the channel signals address decode (C3) and sets the address decode latch (C4) to begin address selection, unless bypass select or a short busy sequence has occurred to block selection.

Bypass Select Signal

Actually, the channel can only attempt selection, because the addressed TC might not be able to accept the selection. Selection begins when the channel raises select out (the select signal) to the highest priority control unit (CU) first. If the first control is not the addressed unit, the CU must propagate the select signal to the next lower priority control. Each CU must propagate the signal, in turn, until select out reaches the addressed TC.

If the addressed TC has low priority, the select signal may arrive as select in, indicating the TC is in series with the select signal return to the channel. Select signal line jumpers (Figure IOP-1, B1-2) are installed during system installation. (Hold out (A1) is raised to all control units in parallel before select out is raised to the first control; this line reduces the time necessary to drop the select signal at the selected control at the end of an operation.)

When the select signal reaches the 2415 TC during attempted selection by the channel, the signal is bypassed if the:

1. TC is not enabled (in off-line mode) or TC power is off. The select signal read relay (RR1) is down to allow the select signal, regardless of decoding, to pass on to the next CU through the read relay N/C points (B2).
2. TC cannot decode the CU address. Bypass select signal regenerates and sends a select signal to the next CU when select out rises (A4).

NOTE: If the TC is the last CU on the interface and has power off, a "hangup" occurs because the lines do not have a terminating voltage.

Short Busy Sequence

If neither of the bypass conditions exist, an address decode condition must first determine whether the TC is busy before selection can be accepted. The 2415 TC is busy if either of two conditions exists:

1. TC is performing a nonburst mode operation (refer to "Burst Mode" in Chapter 1) indicated by the on state of the command busy latch.
2. TC has status stored for a previous operation using a different TU address. Bus out bits 5, 6, and 7 (TU address for intended operation) are compared with the TU address locked in the device register. If these bits do not compare, selection must be blocked.

Either busy condition causes a short busy sequence that terminates the channel attempt at selection. Short busy (D4) causes the following:

1. Turns on the force busy latch (C5) to hold the address decode latch off and prevent address selection.
2. Forces a P, 1, and 3 bit status byte to the bus in lines (E4). Bit 3 is a busy status bit, bit 1 is a modifier that indicates the TC (as opposed to TU) is busy, and the P bit indicates odd parity.
3. Forces status in tag to the channel.

The channel accepts the status byte and usually responds by dropping the select signal to end the sequence.

Address Selection (Figures IOP-2, 3-1, and 3-4)

- TC decodes binary TU address and selects the designated tape unit.
- TC verifies the complete I/O address by regenerating and returning, on bus in, the same address byte received from channel bus out.
- Channel and 2415 TC become interlocked on the interface during address selection.

Select Tape Unit

Address decode latch on (Figure IOP-1) sets the status in latch (Figure IOP-2, B2) and begins the selection sequence by stopping the device end (register) scanner if it is operating. If the TU select latch is off, select out timing resets the device register and sets the register to the binary tape unit address on bus out (A, Figure 3-4). If the TU select latch is on, the designated address is already in the register and the set/reset procedure is unnecessary. Device register outputs, ungated, are decoded and one of six TU select lines is routed to the designated TU.

Operational In Tag

Three key latches are set after the rise of select out 1: address in (B4), force burst mode, and operational in (C4-5). (Resets to force burst mode, not shown, control when TC will drop operational in during ending sequences.) Operational in is gated to the channel (C1) to interlock the TC and channel on the interface.

Address In

When operational in is active, the combined TC-TU address byte is gated to bus in from the TC address (jumper card) generator and the TU device register (D1-5). A P bit is added for odd parity.

After the channel drops its address out tag, the address in latch output, delayed about 1.0 microsecond by a capacitor circuit, gates the address in tag to the channel, indicating an address is on bus in. The TC now waits for a channel command out response and a command byte; address selection is complete.

NOTE: If the channel determined that the address byte was invalid, it drops select out (perhaps issue a halt I/O) to terminate the sequence.

Command Set (Figures IOP-3, 3-1, and 3-4)

- Command out response to address in signals the TC to accept the bus out command byte.
- TC accepts the command byte only if parity is odd.
- If the command is accepted, TC determines whether the designated operation can be performed.

To complete the initial selection sequence, the 2415 TC must perform many tasks in a predetermined sequence. When the channel accepts the address byte and signals command out, indicating the command byte is on bus out, the TC routes the command out signal through three time delays (A1-3), combinations of which produce a sequence of timed pulses. As a result, four gating lines are available: command out (not delayed) and command out 1, 2, and 3. These lines are used to complete most of the remainder of the initial selection sequence.

Command Parity Check

Command out (not delayed) gates the command byte, except the P bit, into the data register (A4) for a parity check (because the command register has no parity circuit). The P bit is set into a separate P-bit trap latch. The P-bit trap latch and the data register condition a parity circuit (A5) to activate "odd byte" if total parity is odd. Odd byte gates the entire byte into the command register after a 2.8-microsecond delay (command out 1). If byte parity is even, the byte is not set in the register, the unit check status latch is set (F3), and the bus out check (sense bit) latch is set; however, initial selection will be completed.

Command Decoding

Command register outputs are decoded immediately (B4-5) to determine what operation is designated. Figure 1-9 shows the command codes. Many decoder outputs condition circuits for testing whether the command can be performed. Initiation of the operation is determined by status conditions and the channel response to initial status.

Command Busy Latch: Most basic command decoder outputs also set the command busy latch (C3), which remains on as long as a command is in the command register. Command busy has several gating functions.

Sense Reset: This reset (C5) is generated to clear all sense bit and error latches, including the unit check status latch, in preparation for the new command.

Initial Status Byte (Figures IOP-3, 3-1, and 3-4)

- Command out timing gates the setting of status latches for certain conditions.
- Status pending indicates that the status latches contain previous operation status.
- Contents of status latches form initial status byte which is sent to the channel.

Existing status conditions set the appropriate status latches as shown at the bottom of Figure IOP-3. Latch outputs are gated (D4) into the data register near the end of command out timing. Command out 3 resets the address in latch (C1) to gate the status byte from the data register to bus in (E1-5); a P bit is added (E5) to provide odd parity.

After the channel drops command out and all out tag timings are complete, the status in tag latch is set (D4). The status in tag latch output, delayed about 1.0 microsecond to allow input/output lines to settle, gates the status in tag to the channel (D1).

Begin Operation or Stack Status (Figure IOP-3)

- Channel response to status in ends initial selection sequence.
- Service out response to status in signals "status byte accepted; proceed with command."
- TC disconnects from the interface for nonburst mode operations.

- Command out response to status in signals "status byte rejected; stack status byte and block burst mode type operations" or "begin nonburst mode operations after disconnecting from interface."

- TC blocks beginning of an operation and disconnects from the interface when it determines that the command cannot be executed, regardless of the channel response.

- Some commands are completed during initial selection sequence.

Status Accepted -- Proceed

A service out response to status, delayed 1.8 microseconds (service out 1), resets the status in latch (E2-3) to set the command gate latch (E5) if the selected tape unit is not counting (timing out a 17-millisecond stop delay at the end of a previous operation). Command gate latch on gates the decoded command lines from the command decoder to begin the designated command. Refer to the appropriate IOP diagram for the specific operation.

Burst Mode Operations: The TC remains interlocked on the interface to execute a data transfer (read, write, or sense) command, unless the command register was reset by a prohibitive status condition to block the operation. The TC blocks performance of a command by setting the status latches and clearing the command register with a TAU reset before sending the initial status byte to the channel. See "Initial Status Bits and TAU Reset."

Tape Motion Control Operations: After a service out response to initial status for tape motion control operations, command gate is set by the fall of the status in latch and the operation is begun if the TU is not counting. Control command and service out 1 turns off the burst mode latch (Figure 2-11) and operational in, and the TC is disconnected from the interface. However, a TAU reset is not generated to clear the command register until the end of the operation; or, as in the case of rewind or rewind-unload, until the selected TU indicates it is rewinding. See the appropriate IOP diagram.

Status Reset: Because the channel has accepted initial status, service out generates a reset to clear all status latches except unit check. A sense reset clears unit check at the beginning of the next operation; if unit check was on, the intended command would not be performed.

Status Rejected

A command out response to status in sets the stack latch (B3) for any designated operation that would be executed in burst mode (read, write, or sense) because the channel cannot continue. Stack is not set for any control command code that must be retained in the command register (tape motion control commands). With the stack latch on, the TC:

1. Blocks operation by generating a TAU reset.
2. Blocks generation of status reset to retain status information.
3. Gates status pending to generate a request in interrupt and again attempts to send the status byte after the TC disconnects from the interface.

A command out response to initial status for any command causes the TC to reset the force burst and operational in latches and to disconnect from the interface.

Tape Motion Control Operations: Because service out was not received, a tape motion control operation is not begun until "not force burst mode and not select out" from the channel turns off operational in. Not operational in turns off the status in latch (E3) to set command gate and begin the operation.

Initial Status Bits and TAU Reset (Figure 2-10)

TAU Reset: A TAU reset is generated to clear the command register during or at the end of initial selection because:

1. Designated command was completed during initial selection (test I/O or feature operation mode set). The reset lines used here are "end test I/O at end of initial selection" and "rewind or ready end control" gated by the "normal" +AI through the "ready" +AI.
2. Stack latch was set by a command out response to status in (rejection of initial selection status byte input).
3. Stop latch is on because the channel sent an interface disconnect during selection (Figure 2-7).
4. Initial status byte contained any status bit combination except channel end only.

Specific initial selection TAU resets for prohibitive status conditions are listed in the following section.

Status Bits: An initial status byte can contain almost any combination of bits, depending on status conditions and the designated command. The command is not executed if the byte contains any bit other than a P bit (for odd parity for a "clean" byte), unless a control command is designated. The status byte for

a control command contains a channel end bit (or channel end and device end bits if the operation is completed during initial selection).

Refer to the bottom of Figure IOP-3; the status latches set during initial selection to block operation, excluding short busy, are unit check and/or busy.

Unit check is set if any of the following conditions exist:

1. Command reject:
   a. Write, write tape mark, or erase gap is designated and the selected TU is file-protected.
   b. A data converter on mode set is designated and the TC does not have the feature installed.

Either condition also sets the command reject sense latch.

2. Bus out check; the command byte has even parity. This condition also sets the bus out check sense latch.

3. Prohibitive tape unit status; the selected tape unit is not ready or is already rewinding. This condition, TU status set UK, is degated if a sense command is designated, because the selected tape unit is not needed to perform the command.

Conditions 1 and 3 also set the TAU reset latch to clear the command register and block the operation. An even parity command byte (bus out check) cannot enter the command register, thereby precluding any operation; therefore, TAU reset is unnecessary.

A busy condition is indicated by the on state of either the rewinding busy or force busy latch (Figure 2-16). Rewinding busy is set if the selected tape unit is rewinding when initial selection begins, not if rewind is designated by the command byte. A rewinding condition also sets unit check and generates a TAU reset to block the new operation.

Force busy is set by long busy which is a status pending condition for a previous operation on the same (selected) tape unit. The intended operation is not performed because of the outstanding status; therefore, a TAU reset is generated.

SENSE OPERATION (FIGURE IOP-4)

Command code 0100, in bit positions 4, 5, 6, and 7, is decoded as a sense command (B1) during initial selection. Service out is received from the channel at the end of initial selection, if the channel accepts the status byte. Service out 1, gated by sense, sets the first bit latch. First bit gates read clock oscillator pulses to the read clock to initiate a read clock cycle.

During the first read clock cycle, RC7 steps the write clock delay counter to count 1, and sense byte 0 is gated to the data register input. RC8 gates the byte into the register, which places it on bus in to the channel. An RC9 pulse generates a service in tag which is sent to the channel to indicate that data is on the bus. An RC10 pulse resets first bit to end the cycle (RC12 ends the cycle for PE machines due to different timing requirements necessary during a read operation).

The channel now responds with service out. Service out 1 resets the data register and sets the first bit latch to begin the second read clock cycle. This time RC7 steps the delay counter to count 2, and sense byte 1 is gated to the data register input. This cycle is completed exactly like the first cycle. The third read clock cycle steps the delay counter to count 3 to gate sense byte 2. The fourth cycle steps the counter to count 4 to gate byte 3. The fifth and sixth cycles step through count 5 and 6, but the data register is empty for sense bytes 4 and 5; two all zero-bit bytes are sent to the channel.

Normal End Sense: A normal end to the sense operation occurs only after all six sense bytes have been sent to the channel. The channel responds to sense byte 5 with service out, and a seventh read clock cycle is begun. RC7 steps the delay counter to count 7. Count 7 is AND'ed with the not service in latch (part of service in/service out timing) to generate end sense. End sense activates set ends, and the ending operation begins. Refer to "End Status -- Burst Mode." No TC error conditions can occur during execution of a sense operation (after initial selection is complete).

Early End Sense: An early end to the sense operation can occur after the transfer of any sense byte (including the last one). If the channel responds to service in and a sense byte with command out (instead of service out), the stop latch is set. The stop latch output is AND'ed with the not service in latch to generate early end sense. Early end sense activates set ends, and the ending operation begins. Refer to "End Status -- Burst Mode."

READ FORWARD OPERATION

Refer to Figures 3-6 and 3-7 in the maintenance diagram volume for flow and timing charts and Figure IOP-11N in the diagram manual, which is contained in the maintenance diagram volume. On Figure IOP-11N, data flow is shown for nine-track operation, although seven-track motion controls are also shown. Seven-track feature data flow, including translate and data convert, is described in Chapter 4 and depicted on Figures IOP-12N and IOP-13N.

Start Tape Motion

After the channel accepts the initial (selection) status byte by signaling service out, the command gate latch is set. Refer to "Initial Selection Sequence" for details. To begin a read forward operation, command gate and read activate forward go (Figure IOP-11N, coordinate A3) if the TU is in forward status; if not, a turnaround sequence is necessary (Figure IOP-8) to activate "set forward" (C5). When the TU is in forward status, forward go gates "go" (A5) to the TU.

Time Read Delay

The standard read delay is preceded by an LP delay if tape on the selected TU is at load point.

LP and/or Standard Read Delay

During initial selection, the LP erase latch is set (B2) by command busy if the selected TU is signaling LP. Forward go sets the LP delay latch (B2) to run the delay counter in millisecond mode (B5). After the 153-millisecond read LP delay is complete, both LP latches are reset and the standard read delay begins immediately; not LP delay resets the delay counter and turns on start delay (A4) to restart the delay counter for the standard (start) delay. Both read and write operations use the start delay latch, although the standard read delay is 4.2 milliseconds and the standard write delay is 7.0 milliseconds.

After 4.0 milliseconds of start delay timing is complete, the data gate latch and first character latch are set (C3) to prepare for the reading of data. When the standard read delay of 4.0 milliseconds is complete, start delay is reset to stop and reset the delay counter.

Read Data Block

As the data block begins to pass over the read heads, the first (most leading) bit of the first data byte sets the first bit latch (C4) to run the read clock for one cycle; RC10 of the cycle resets the read clock and the first bit latch.

During the first read clock cycle, all remaining bits of the first data byte are gathered in the read register (E4) and routed to the LRC register (E4). At RC8 time, the first byte is set into the data register from the read register (LRCR is for LRC error checking). The first half of an RC9 pulse (RC9-2) turns off the first character latch (C3); the last half of RC9 generates a strobe pulse to set the service in latch. After the strobe pulse falls, the service in tag latch is set (D4) and service in is sent to the channel; the first data byte, already in the data register, is gated to bus in. The channel accepts the byte and responds with the service out tag to reset the service in latch. This procedure is the same for a seven-track read forward operation, although the entire RC9 pulse is used to strobe.

When the first bit of the second byte is sensed, the first bit latch is set again (the latch should have been reset almost 30 microseconds earlier). The procedure for moving the byte to the channel is the same as the first byte, except that the strobe is a full RC9 pulse. All remaining bytes of the block are processed to the channel in the same manner.

Stop Read

The channel may have been conditioned to accept only part of the tape block being read, in which case a service in request may be answered by a command out tag instead of service out when the channel has enough data. The TC will block further service in attempts, but the TC must continue moving tape to the next IBG. During the remaining portion of the block, error checks are degated.

Note that command out (F1) sets the stop latch (F2) which holds the service in latch off. EOB sensing and end operation are identical. See "EOB Search."

Read Tape Mark

If the first byte of the tape block is a tape mark configuration, the tape mark latch is set during the first half of RC9 (RC9-1) during the first read clock cycle. This latch blocks the turn-on of the service in tag latch, so that the TM is not sent to the channel. Refer to "Data Time and Tape Mark Recognition" in Chapter 2 for details. The TM read operation is terminated the same as for a data read operation.

End of Block (EOB) Search

During every read clock cycle, RC6, 7 sets the EOB search latch (F3) to start the delay counter in microsecond mode (B5). EOB search is normally reset by RC2, 3 of the following cycle to reset the delay counter. After the last data byte is read, EOB search remains on and the delay counter continues stepping to time the four character spaces to the first check character, usually the CRCC (a TM has no CRCC). At delay counter count 32, the EOB 2.3 characters line sets the read disconnect latch (F3).

EOB search remains on to continue driving the delay counter in microsecond mode as tape is spaced over the check characters. For a seven-track operation (or if a TM is the tape block) with only the LRCC, the delay counter times about eight character spaces

and causes the reset of the EOB search latch (F1). For a nine-track operation, EOB is not reset until 12 character spaces are timed to ensure that both the CRCC and LRCC are past the heads.

The fall of EOB search stops and resets the delay counter, and sets the stop delay latch (F4) when all delay counter latches are off. Stop delay on then steps the delay counter in millisecond mode to time the first part of the stop delay period. After 2.0 milliseconds for a nine-track operation or 8.0 milliseconds for a seven-track operation, stop delay gates "set count" (F5) to the tape unit. An 800-microsecond drive is also sent to the tape unit, which begins counting the final 17 milliseconds of stop delay.

When the tape unit signals it has begun the count (counting), end tape operation is generated to set the device end and channel end status latches, which begin the end status in sequence. Refer to "End Status -- Burst Mode." Refer also to "Error Detection" in Chapter 2 for a description of the error conditions possible during a read operation.

Status Bits

Normally, the end status byte contains only channel end and device end bits; however, unit exception and/or unit check may also be included. Unit exception is set if the tape block read was a tape mark. Unit check is set if one or more read error conditions was encountered during the operation. See Figure 2-16.

READ BACKWARD OPERATION

Refer to Figures 3-8, 3-9, and IOP-11N in the maintenance diagram volume. On Figure IOP-11N, data flow is shown for a nine-track operation, although seven tape motion controls are also shown. Seven-track data flow is described in Chapter 4 and depicted on Figure IOP-12N.

Start Tape Motion

Channel acceptance of the initial (selection) status byte is signaled by service out, which causes the command gate latch to be set. See "Initial Selection Sequence" for details.

To begin a read backward operation, command gate and read backward activate backward go (Figure IOP-11N, coordinate A3) if the tape unit is already in backward read status; if not, a turnaround sequence is necessary before set backward and set read status (C5) can be signaled to the tape unit. When the selected tape unit is in backward read status, backward go gates "go" to the tape unit.

Time Read Delay

Backward go also turns on the start delay latch (B4) to start the standard 4.2-millisecond read delay. Start delay runs the delay counter (B5) in millisecond mode. After 4.0 milliseconds of start delay, the data gate latch and first character latch are set (C3) to prepare for the reading of the tape block. When the read delay is complete, start delay is reset to stop and reset the delay counter.

Read Check Characters and/or Tape Mark

A check character is the first byte sensed at the beginning of a read backward operation; the block may be a tape mark. Configurations that can be encountered are:

1. Nine-track operation:
   a. LRCC and no CRCC then data bytes
   b. LRCC and a CRCC then data bytes
   c. LRCC and single TM byte then IBG
2. Seven-track operation:
   a. LRCC then data bytes
   b. Data bytes only; LRCC blank
   c. LRCC and single TM byte then IBG

In all the preceding cases, the first bit of the first byte read turns on the first bit latch (C4) and runs the read clock for one cycle. During this cycle, the EOB search latch (F2) is set by RC6, 7 to run the delay counter in microsecond mode for character space timing. Details of how each of the preceding configurations is detected are provided in Chapter 2 under "Data Time and Tape Mark Recognition."

Tape Mark: If a true tape mark is detected, the delay counter continues to step, gated by the EOB search latch, until six EOB character spaces are timed for a seven-track operation or until ten character spaces are timed for a nine-track operation. Either condition sets the read disconnect latch (F3). From this point, end operation is the same as for reading a data block.

Backward at Load Point

The backward end latch (B1) and LP erase latch (B2) are set if:

1. Tape on the selected tape unit is already at LP during initial selection, or
2. Tape is moved to LP before any data is sensed (read heads were ahead of the first tape block).

In either case, the tape control end operation procedure is the same, although the latter condition is not detected until after the standard read delay is timed. The LP erase latch performs no usable function for read backward; the LP delay latch is set for read forward operations only.

If tape is already at LP, backward end is not set until the channel accepts the initial status byte and signals service out, which turns on command gate to gate the backward command line. When all service out tag delays (and service out) are inactive, initial selection is complete. Backward end and load point generate read backward at LP (B2).

If tape is not at LP but the read heads are located between LP and the first tape block, the backward operation begins normally by moving tape backward and completing the read delay. Also, the data gate and first character latches are set. Instead of reading the first bit, the LP is encountered and backward end is set.

In either case, the read backward at LP line sets the channel end, device end, and unit check status latches (Figure 2-16). Channel and device end cause an immediate end status in procedure. See "End Status -- Burst Mode."

Read Data Block

If the first byte configuration read from tape is not a tape mark, RC9 of the read clock cycle, started by the first data byte, generates a strobe pulse to set the service in latch. At the fall of the strobe pulse, a service in tag is generated and sent to the channel. (The exception is seven-track backward: the first turn-on of the service in tag latch was blocked by "not data time seven-track backward.")

An RC8 pulse of the same read clock cycle that set service in sets the entire first byte into the data register from the read register (E4). (The read register also gates the byte into the LRCR for error checking.) The data register output is immediately gated to channel bus in, so that when the service in tag to the channel rises at RC9 time the byte is already on bus in. The channel accepts the byte and signals service out, which resets the service in latch.

Each data byte is processed in the same manner: the first bit of each byte causes a read clock cycle, RC2, 3 resets EOB search, RC6, 7 sets EOB search, RC8 moves a byte to the data register and bus in from the read register, RC9 causes a service in request, and service out resets the service in latch.

Stop Read

The channel may have been conditioned to accept only part of the tape block being read, in which case a service in request may be answered by a command out tag instead of service out when the channel has enough data. The TC will block further service in attempts, but the TC must continue moving tape to the next IBG. During the remaining portion of the block, error checks are degated.

Note that command out (F1) sets the stop latch (F2) which holds the service in latch off. EOB sensing and end operation are identical. See "EOB Search."

EOB Search

An EOB search is active throughout the operation, the same as for read forward. As the read clock cycle for the last data byte proceeds, the EOB latch is again reset at RC2, 3 then set at RC6, 7. The EOB latch remains on to run the delay counter for proper spacing before the stop delay begins. Read disconnect is set (E3) after six character spaces for seven-track operations or nine character spaces for nine-track operations. This extra spacing is not needed for tape positioning at the true end of block, but is necessary to prevent the erroneous turn-on of read disconnect at the beginning of read backward (due to check characters).

After eight character spaces for seven track or 12 character spaces for nine track, EOB search is reset to stop and reset the delay counter. Stop delay, set when EOB search falls, now gates the delay counter to run in millisecond mode for the first part of tape stopping delay. At either 2.0 or 8.0 milliseconds, stop delay gates set count (F5) to the tape unit. An 800-microsecond drive is also sent to the tape unit, which begins counting the additional 17-millisecond stop delay. When the tape unit begins the count and sends back the counting signal, end tape operation is generated to set the channel and device end status latches. Both end conditions begin the end status in sequence immediately. Refer to "End Status -- Burst Mode" for ending details, including the deconditioning of go.

Refer also to "Error Detection" in Chapter 2 for a description of the error conditions possible during a read backward operation.

Status Bits

Normally, the end status byte contains only channel end and device end bits (Figure 2-16); however, unit exception and/or unit check may also be included. Unit exception is set if the tape block read was a tape mark. Unit check is set if one or more read error conditions was encountered during the operation; it is also set if load point was indicated as the operation began, or if load point was encountered instead of sensing a tape block.

SPACE OR SPACE FILE OPERATIONS

Forward space and space file operations are similar to read forward operations, and backspace and backspace file operations are similar to read backward

operations. The major difference in both cases is that no data read from tape is sent to the channel. Refer to Figures IOP-11N, 3-12, and 3-13 in the maintenance diagram volume.

A control command operation begins when the command gate latch is set by a service out or command out response to initial status at the end of initial selection. Command gate is not set until operational in falls if a command out was active. The tape control disconnects from the interface after either out tag drops at the end of initial selection.

Forward Space or Space File

A forward space operation causes the tape to move forward one tape block to the next IBG; a forward space file operation causes the tape to move forward to the IBG after the first tape mark block is encountered. These control command operations begin in the same manner.

Begin Tape Motion and Time Read Delay

Both operations begin exactly like a read forward command; the following is a summary of the sequence:

1. Command gate activates forward go (A3), unless the selected tape unit is in backward status, in which case a turnaround sequence is performed first.
2. When turnaround is inactive, forward go gates the go signal to the selected tape unit (A5).
3. Time 153-millisecond read LP delay if tape is at LP at the beginning of the operation; LP erase sets LP delay (B1) to run the delay counter in millisecond mode; reset both latches and the delay counter after the delay is complete and begin the standard read delay.
4. Forward go (and not LP erase) sets start delay (B4) to run the delay counter in millisecond mode (B5), which times the standard 4.2-millisecond read delay.
5. Set the data gate and first character latches (C3) after 4.0 milliseconds of start delay; then reset the start delay latch to stop and reset the delay counter after the 4.2-millisecond read delay is complete.

Space over Data or TM Block

When the tape block begins passing over the read heads, the first bit latch (C4) is set by the first bit of the first byte. First bit runs the read clock (C5) for one cycle. The first byte (and all other bytes) passes through the read register into the LRC register only because the RC8 data register set pulse and service in are blocked. A strobe pulse is generated by RC9 for read, read backward, or sense command operations only (D2).

First bit signals and read clock pulses detect a tape mark and/or the EOB. Detection of a tape mark is described under "Data Time and Tape Mark Recognition" in Chapter 2. If a tape mark is detected, the tape mark latch is set; but the EOB procedure is the same as for a data block.

EOB Search

Each first bit causes a read clock cycle, during which the EOB search latch is set (F2) at RC6, 7 time and reset by RC2, 3 time of the next cycle. When EOB search is on, the delay counter runs in microsecond mode; when EOB search is off, the counter is stopped and reset. After the last byte of data or a TM is read, EOB remains on to allow the counter to time 2.3 character spaces (about midway between the last byte and the first check character).

The EOB 2.3 characters line sets the read disconnect latch (E3). The EOB search latch remains on, driving the delay counter until either 8 or 12 character spaces are timed, depending on seven-or nine-track operation. When EOB search is reset, the stop delay latch is set at the same time the counter is reset.

End Forward Space

The stop delay latch runs the delay counter in millisecond mode (and holds the EOB search latch reset). After either a 2.0 or 8.0 millisecond delay (nine-or seven-track operation), set count is sent to the selected tape unit, which sends back "counting" when it begins the 17-millisecond stop delay. End tape operation is generated to set the device end status latch (gated by control command). Device end starts an end status procedure. See "End Status -- Request In Interrupt." See "Status Bits" for an explanation of the bits included in the status byte.

End Forward Space File

After the stop delay latch is set, the delay counter runs, but will step for a short period because stop delay will be blocked. (A space file operation is stopped only after a tape mark is detected.)

When the delay counter 4 trigger is on, the early reset latch is set. The on state of the early reset latch turns off read disconnect and stop delay to block stop delay timing and allow tape motion to continue.

As the next tape block is read, the entire reading procedure is repeated. The early reset latch, turned off by the fall of disconnect and stop delay, is reset to block stop delay timing unless the tape block read is a tape mark. With the tape mark latch on, the turn-on of early reset is blocked and the operation ends exactly like a space forward operation.

Status Bits

Normally, device end is the only bit included in the end status byte for control command; channel end was sent to the channel in the initial (selection) status byte. During a space operation, if the block that is spaced is a tape mark, a unit exception bit is added. The unit exception bit is not added for a space file operation. A unit check bit is added only if the tape unit ready line drops during either operation. A CU end bit is also added if unit exception (bit) is indicated.

Backspace or Backspace File

A backspace operation causes the tape to move backward one tape block to the next IBG; a backspace file operation causes tape to move backward to the next IBG after spacing over a tape mark. Both control command operations begin in the same manner.

Begin Tape Motion and Time Read Delay

Both operations begin exactly like a read backward command; the following is a summary of the sequence:

1. Command gate activates backward go (A3), unless the selected tape unit is not in backward status, in which case a turnaround sequence is performed first.
2. When turnaround is inactive, backward go gates the go signal to the selected tape unit (A5).
3. If tape is already at LP, the backward end latch is set to generate read backward at LP (B2) and an end status in sequence begins immediately.
4. Backward go also sets start delay (B4) to run the delay counter in millisecond mode (B5), which times the standard 4.2-millisecond read delay.
5. Set the data gate and first character latches (C3) after 4.0 milliseconds of start delay; then reset the start delay latch to stop and reset the delay counter after the 4.2-millisecond read delay is complete.

Space over Data or TM Block

When the tape block begins passing over the read heads, the first bit of the first byte read sets the first bit latch (C4) to run the read clock for one cycle. At this point, the data time and tape mark detection circuits are activated to check the configuration of the first bytes read. Review "Data Time and Tape Mark Recognition" in Chapter 2. If a tape mark is detected, either a backspace or backspace file operation is terminated. If the check characters are followed by data, the operation continues.

First bits of data bytes run the read clock. Bytes move through the read register to the LRC register only; service in is not generated. An RC9 strobe pulse is generated for read, read backward, or sense command operations only (D2).

First bit signals and some read clock pulses are used to detect a tape mark and/or the EOB. If a tape mark is detected, the tape mark latch is set; but the EOB procedure is the same as for a data block.

Move Tape to LP: If no data is read and tape is moved to LP, either type of operation is terminated because backward end is on (B1). Read backward at LP begins an immediate end status in procedure.

EOB Search

Each first bit causes a read clock cycle, during which the EOB search latch is set (F2) at RC6, 7 time and reset by RC2, 3 time of the next cycle. When EOB search is on, the delay counter runs in microsecond mode. When EOB search is off, the counter is stopped and reset. After the last byte of data is read, EOB remains on to allow the counter to time six or ten character spaces (nine-or seven-track operation) and set read disconnect (F3).

The EOB search latch remains on, driving the delay counter until either 8 or 12 character spaces are timed, depending on seven-or nine-track operation. When EOB search is reset, the stop delay latch is set at the same time the counter is reset.

End Backspace

See "End Forward Space;" operation from this point is the same.

End Backspace File

See "End Forward Space File;" operation from this point is the same.

Status Bits

Normally, device end is the only bit included in the end status byte at the end of a control command; channel end was sent to the channel in the initial (selection) status byte. During a backspace operation, if the block that is spaced over is a tape mark, a unit exception bit is added. The unit exception bit is not added for a backspace file operation.

A unit check bit is added to the status byte if:

1. Load point was on or is encountered as either type of operation begins.
2. Tape unit ready drops when the operation is in progress.

A control unit (CU) end bit is also added if LP was indicated (item 1) or unit exception is on. See Figure 2-16.

WRITE OPERATION

Refer to Figures 3-10, 3-11, and IOP-15N in the maintenance diagram volume for flow and timing information. On Figure IOP-15N, data flow is shown for nine-track operation, although seven-track tape motion controls are also shown. Seven-track data flow is shown on Figures IOP-16N and IOP-17N, and is described in Chapter 4.

Start Tape Motion

After the channel accepts the initial (selection) status byte by signaling service out, the command gate latch is set (Figure IOP-3). To begin a write operation, command gate and write (WTM and erase) activates forward go (Figure IOP-15N, coordinate A3). Go and set write is routed to the selected tape unit (TU) to begin tape motion (A5).

Time Write Delay -- Request First Data

The standard write delay is preceded by an LP delay if the selected TU is at load point.

LP and/or Standard Write Delay

During initial selection, the LP erase latch (A1) is set by command busy if the selected tape unit signals tape is at load point. Forward go sets the LP delay latch (B1) to run the delay counter in millisecond mode (A5). After approximately 3-3/4 inches of tape is erased forward (204 milliseconds), both LP latches are reset and the standard write delay begins immediately. The not LP delay line resets the delay counter and turns on start delay to start the delay counter again.

After a 4.0-millisecond start delay, a service in request for the first byte is generated (B1-4). The data gate latch (B2) and the first character latch (E1) are set at the same time. If the channel responds with command out (E1), indicating that it cannot supply the first byte, the stop latch is set (E2) to allow end write, which activates write disconnect and blocks the write operation. Tape is moved but no data is written. Stop and first character set the word count 0 sense latch and begin the end status in sequence. Device end is set to degate go to the tape unit (A3).

Normally, the channel responds to a request for data with service out (C1) after it sets the byte on bus out. Service out 1 sets the byte into the data register (C3). Start delay is reset by count 36, 7 milliseconds after it was set, to complete the standard write delay and reset the delay counter.

Write Data Block

The fall of start delay sets write condition (D2) after the delay counter is reset (WC DC off). Write condition routes the 240-kc oscillator (seven-track oscillators are determined by the density designated; see Figure 2-18) to the write clock, which is the first four trigger positions of the delay counter. Write condition also blocks the turn-on of the 16 trigger. The write clock runs continuously.

The first data byte, stored in the data register (DR), is written on tape by a WC3 pulse (D5), possibly delayed for deskewing. At WC4, 5 the same byte is gated into the CRCR input latches (C-D4). (The CRC shift into the CRCR triggers occurs at the next WC3 pulse.) A WC7 pulse strobes the service in latch (B3) to generate another service in request for the next byte. The channel must respond by the next WC2, 3 pulse; if the channel does not respond, an overrun error is signaled.

Service out 1 sets the bus out byte in the DR; service out 2 resets service in (B3). The service in/service out procedure is repeated for each byte of data to be included in the data block.

Stop Write

A command out response to any service in is a channel signal that the last byte of data has already been sent; stop the operation. Command out sets the stop latch to allow the turn-on of the end write latch; the output, permit write disconnect (E3), activates write disconnect and disables the block turn-on of the delay counter 16 trigger. The counter continues to step (in microsecond mode) past write clock 15 of the last write clock cycle to time the spacing of the check characters.

Write Check Characters

After a 130-microsecond time lapse, the:

1. CRC character configuration is gated from the CRCR to the DR (D4), for nine-track operation only.
2. write check character latch is set (D4).

After 267 microseconds, the CRCC is written; and at 543 microseconds, the LRCC is written. The LRCC is generated by resetting any write trigger that is still on. The 543-microsecond signal also resets write condition (D2) to stop and reset the delay counter.

For a seven-track operation, no CRCC is generated and the LRCC is written at 267 microseconds. Write condition is reset at the same time.

End of Block (EOB) Search

When a data block is written, the same data is read back into the read circuits (F1) for read register VRC and skew error checking. Therefore, after writing is complete, end operation must await a read circuit indication that the check characters have been detected at the read heads.

The fall of write condition allows the turn-on of the EOB search latch (E3, like it is turned on for each byte during a normal read operation). EOB search on drives the delay counter in microsecond mode; if EOB is reset, it resets the counter. When the counter steps to 32 (2.3 character spaces) after the last byte is read, check character spacing is indicated and the read disconnect latch is set (E4). The counter is allowed to run longer in order to space over the check characters. EOB search is then reset to turn on stop delay (F4). EOB search also stops and resets the delay counter.

Stop delay activates set count immediately (E5) which is sent to the tape unit, along with 800-microsecond pulses, to allow the tape unit to begin counting the 17-millisecond stop delay for proper IBG spacing. When the tape unit signals it has begun the count, end tape operation is generated to set the device end and channel end status latches, which begin the end status in sequence. Refer to "End Status -- Burst Mode." Refer also to "Error Detection" in Chapter 2 for a description of the error conditions possible during a write operation, and to Figure 2-16 for status condition bits that can be included in the end status byte.

Status Bits

Normally, the end status byte contains only channel and device end bits; however, unit exception and/or unit check may also be included. Unit exception is set if tape indicate (TI) is encountered during the operation. Unit check is set if one or more write error conditions is encountered during the operation.

WRITE TAPE MARK OR ERASE GAP

A write tape mark (WTM) operation is similar to a write command operation, except that no data is sent from the channel. An erase gap (ERG) operation is the same as the beginning of a WTM operation. Refer to Figures IOP-15N, 3-14, and 3-15 in the maintenance diagram volume for flow and timing information.

Begin Tape Motion and Time LP Delay

A control command operation begins when the command gate latch is set by a service or command out response to initial status at the end of initial selection. Command gate is not set until operational in falls, if command out was the response. The TC disconnects from the interface after either out tag drops at the end of initial selection.

Both operations begin in the same manner. Command gate activates forward go (Figure IOP-15N, coordinate A3) if backward status is inactive; if not, a turnaround sequence is necessary to set forward status and write status in the selected tape unit. See "Turnaround."

When "not turnaround" is active, forward go gates "go" to the tape unit to begin tape motion. Forward go also sets the LP delay latch (A1) because the LP erase latch is already on (set when the command byte was loaded into the command register). LP delay gates millisecond drive to the delay counter to time a write LP delay. When tape moves forward, approximately 3-3/4 inches of tape is erased.

End Erase Gap

Erasure of almost 4 inches of tape is the function of an erase gap operation. When the delay counter steps to 1088, a delay of 217 milliseconds is complete and end tape operation is generated (F5) to begin an end status in procedure. See "End Status -- Request In Interrupt." During the end status procedure, a TAU reset turns off the LP latches and resets the command register, which drops go to the tape unit. The status latches that are set are described at the end of the following section.

Write the Tape Mark

After 204 milliseconds of the LP delay has elapsed, the LP latches are reset (gated by not erase gap, A1). With LP erase off, the start delay latch is set (A3) and the delay counter is reset. Start delay starts the delay counter in millisecond mode again to time the 7.0-millisecond standard write delay.

When count 36 is reached (7.0 milliseconds), the start delay latch is turned off to stop and reset the delay counter. (The service in latch is not set at 4.0 milliseconds of start delay because the strobe is gated by "write" only.) The fall of start delay sets write condition (D2), which starts the write clock and deconditions the write clock-delay counter turn-on to the 16 trigger (B5).

Tape Mark Configuration

A tape mark (TM) consists of two bytes (characters): a single TM byte followed four character spaces later by its LRC character which has the same bit configuration as the TM; no CRCC is written. Seven-and nine-track tape marks differ; a nine-track TM consists

of a 1 bit in tape tracks 3, 6, and 7; all other tracks are 0 (no bits). A seven-track TM consists of a 1 bit in tracks 4, 5, 6, and 7 and no bits in all other tracks; these tracks correspond to the 8, 4, 2, and 1 bit positions of a binary coded decimal (BCD) character.

Command register outputs, ungated or AND'ed with the seven track line, are shown at the bottom of Figure IOP-15N, sheet 2. These TM gating lines "force" bits into the proper positions of the data register at WC2, 3 of the first write clock cycle. The TM is written and deskewed at WC3 when the write pulse latch is set (Figure IOP-15N, coordinates C-D5).

Also, at WC2, 3 of the first cycle, the stop latch is set (E2) to allow the setting of the end write latch; this latch generates permit write disconnect, which allows the next (second) write clock cycle to extend past the 16 trigger. When the delay counter reaches 32 (130 microseconds), the write check character latch is set (D4) to write the TM LRC character. (The CRC time latch is held reset by "not write.")

At write disconnect 267 or 543 microseconds (seven or nine track, respectively), the write pulse latch is set to reset write condition which stops and resets the delay counter.

EOB Search

A delay follows the fall of write condition while the written TM moves from the write to the read heads. With write condition off, the EOB search latch is set by an RC6, 7 pulse of the read clock cycle that is started when the TM is read.

EOB search also runs the delay counter in microsecond mode. After 2.3 character spaces (about midway between the two bytes), read disconnect is set (E4). When either 8 or 12 more spaces are timed, EOB search is reset, which resets the delay counter and sets stop delay (E4). For a nine-track operation, set count is sent to the TU immediately to start the 17-millisecond stop delay; for a seven-track operation, set count is delayed 6.6 milliseconds to create a longer IBG. When the TU signals it is counting, end tape operation is generated to begin the end status sequence. See "End Status -- Request In Interrupt."

Status Bits

Normally, only a device end bit is included in the end status byte for a control command; channel end was sent to the channel in the initial (selection) status byte. A unit exception bit is added, if either the WTM or erase gap operation moved tape beyond tape indicate (TI). A unit check bit is set if the selected tape unit drops ready or if the WTM operation signaled an LRCR check or skew error.

REWIND AND REWIND-UNLOAD

Because rewind and rewind-unload operations are similar, they are depicted on the same logic diagram. Refer to Figures IOP-5 and 3-16 in the maintenance diagram volume.

Begin Operation

During initial selection for either a rewind or rewind-unload operation, the following occurs:

1. Tape unit address is set in the device register (scanner stopped, D2 on Figure IOP-5) to select the designated tape unit.
2. The rewind hold latch is set (B1) after command out drops and the command byte has been accepted.
3. Set arm (C2) is sent to the selected tape unit to set the arm latch (D4) and "prime" for a unit free device end.

The arm latch is set because:

1. Rewind or rewind-unload was designated, or
2. The selected tape unit was not ready (busy) when initial selection began, regardless of the designated operation.

When the command gate latch is set at the end of initial selection, either rewind or rewind-unload is gated immediately to the selected tape unit as the TC disconnects from the interface. When either the rewind latch (B4) or the rewind-unload latch (C4) is set in the TU, ready (E4) to the TC is deconditioned to indicate the operation has begun. The inactive ready condition generates a TAU reset (B3) to clear the command register of the command code.

Rewind

If the chain latch is off, indicating the channel does not want to "hold" the TU, the TC is now free of the unit. With the command register clear, the command busy latch is reset to allow the device register to scan (D2); the select line becomes inactive.

Unit Free Device End

When the tape unit has completed the rewind operation (tape is at LP), ready is again activated and, gated by the arm latch, unit free (D4) is sent to the TC. The ungated unit free signal stops the scanner at the address of the tape unit involved. Device register outputs are decoded (D2) to reselect the tape unit and gate the unit free signal (C1). After a 1.0-microsecond delay, the unit free signal, gated by

select, sets the status in latch which begins an end status sequence by generating a service request. Refer to "End Status -- Request In Interrupt."

After the channel has accepted the device end status byte, the bit 5 to bus in line activates reset arm which is sent to the tape unit (not shown on Figure IOP-5).

Rewind at LP

If the selected tape unit is already at LP (tape is rewound) when initial selection began, a TAU reset is generated as soon as the channel end latch (B1) is set. Channel end is always set for a control command during selection because a channel end bit must be included in the initial status byte. A device end bit is not included due to program compatibility with other tape systems. The device end bit is generated and sent in a separate status byte after initial selection is complete and the TC has disconnected from the interface.

Operation

With the tape already at LP and the arm latch on, ready remains active (E4). Unit free also remains active and sets the status in latch 1.0 microsecond after the command busy latch is reset at the end of the selection sequence. The status in latch generates a service request to cause a request in interrupt for the device end status byte. (Unit free from the tape unit prevents the scanner from starting again; the tape unit remains selected.) The arm latch is reset after the status in procedure.

Rewind-Unload

Once the tape unit has begun the rewind-unload, the TC must perform an immediate end status in sequence. Because there is no guarantee that the TU will be made ready again after it is unloaded, system programming requires a device end status byte to indicate that the tape unit has begun the rewind-unload.

When the TU signals not ready, the set device end and CU end line (B2) sets the device end and CU end status latches. The not ready condition, gated by rewind-unload, also sets the unit check status latch.

Device end on activates status pending (E2) to maintain "stop scanner," so that the TU remains selected after command busy falls at the end of initial selection. The device end latch also begins the status sequence. Refer to "End Status -- Request In Interrupt."

Unit Free after Rewind-Unload

At the end of the end status -- request in interrupt sequence, status reset resets device end and CU end, and sets a latch that blocks the sending of another unit check status bit to the channel until a sense reset is generated. Resetting device end and CU end drops stop scanner (D2), which allows the scanner to start. The select line to the tape unit drops, and the TC is freed of the TU.

After the tape unit is unloaded, a unit free is generated if the unit is manually reloaded and made ready again, because the arm latch is still on. Unit free causes another status in sequence during which a a status byte, with device end only, is sent to the channel. The sequence is the same as described under "Unit Free Device End."

END STATUS -- BURST MODE (FIGURES IOP-6, 3-17, AND 3-18)

This is the normal ending sequence performed at the completion of sense, write, and read operations. The sequence is initiated by any of the lines that activate set ends (Figure IOP-6), usually the end tape operation line.

Initiating Conditions: End sense or early end sense is used at the completion of a sense operation. The "not control" AND gate (end tape operation, not control command, and not TAU reset) is used at the end of write, read forward, and read backward operations. If a word count 0 condition is set at the beginning of a write operation, the "stop on write and first character" input to set ends is used. Read backward LP is an abnormal ending condition: when LP is sensed at the beginning of a read backward operation, the ending sequence is initiated and a unit check is set. Ready drop is an abnormal ending condition that occurs when ready condition is lost in the selected tape unit during an operation (such as tape breaking or an operator pressing the reset pushbutton).

Operation

Set ends sets the device end, channel end, and status gate latches. Device end and channel end are the normal end status conditions that will be sent to the channel in the end status byte (bits 4 and 5); however, other status bits may also be included. The status gate latch, set by the set ends line, gates the status byte to the data register by activating gate status to DR and set DR inbound. (Details of the status bits and status circuits are described in Chapter 2, and at the end of each operation description.) The contents

of the data register is inspected for an odd or even number of 1 bits, and a parity bit is added to the output. (The injected parity bit is a 1 if the DR contains an even number of 1 bits.) The contents of the DR, and the parity bit, are connected to bus in by gate in data. A bit in data register position 10 (device end) resets the status gate latch.

Device end and channel end set the TAU reset latch. The actual gating of TAU reset is through a number of AND and OR gates, conditioned by not force busy, not ready drop, not command out, and not address out. TAU reset causes the sequential resetting of the command register, command busy latch, and command gate latch.

Resetting the command register and the command busy latch activates green and go which is AND'ed with device end (status pending) and not status gate (reset by DR10) to activate the set status in line. Set status in is gated by select out and operational in latch (which are active during burst mode operations) to set the status in latch. The status in tag latch is then set, and status in tag is sent to the channel to indicate that the data on bus in is a status byte.

Tape motion is stopped when the device end latch is set, which degates the go line to the tape unit.

Status Accepted: Service out tag is received from the channel in response to status in, if the end status byte is accepted. Service out timing (service out and not service out 1) is gated by the status in latch, to activate the status reset line. This line clears the TC of stored status conditions.

Status Not Accepted: Command out is received from the channel in response to status in, if the end status byte is rejected. The stack latch is set, and status is retained by the TC (stacked) rather than being reset.

The TC is relieved of the stacked status by initiating a request in interrupt, or if the channel begins an initial selection sequence.

END STATUS -- REQUEST IN INTERRUPT (FIGURES IOP-7, 3-19, AND 3-20)

A request in interrupt sequence is begun any time end status is available and the TC is not interlocked on the interface. To perform the sequence, the TC requests service, identifies itself, interlocks the channel, and sends the end status byte.

Suppress Out

The channel can suppress all but the first attempt to interrupt by holding the suppress out tag active to all control units; stack latch off degates suppress out. However, if the TC is not chained (chain latch off), all attempts are blocked for a unit free condition.

Chain Latch: The chain latch is set in a control unit if the channel raises suppress out during any status in sequence. Once the chain latch is set, the TC has unit free request in-interrupt priority on the interface because the stack latch is not set if a unit free device end is rejected. The chain latch is reset during the next status in sequence, unless the channel again raises suppress out.

Status Pending

An interrupt sequence is begun by status pending (Figure IOP-7, coordinate A3) if any one of four conditions exists:

1. Selected unit free is activated on completion of a rewind type operation, or when a TU becomes ready after it was selected while it was not ready.
2. Device end status latch on; this is a key latch for beginning nonburst mode interrupts. It is set by:
   a. End tape operation (control end) at the end of a tape control supervised control operation (not rewind type of operation).
   b. Set device end and CU end as soon as initial selection is complete to begin the special device end, CU end, unit check status sequence after a rewind-unload has begun.
3. CU end status latch on (earlier machine design used this latch for status pending; the condition no longer exists).
4. Stack latch on which is set when the channel rejects a status byte, unless it is the initial status byte when a control command is initiated. If the channel rejects a control command end status byte, the stack latch is set because the command register is off.

A TAU reset is generated (A4) as soon as device end is set if the command gate latch is on. The command register contains a command byte at the end of a tape motion type control command (WTM, backspace, etc). TAU reset clears the register when this sequence begins because the command code is no longer needed. With the command register off, the go line to the selected tape unit is dropped (forward or backward command is dropped), although the tape unit is timing its stop delay.

Request In

Status pending or a selected unit free condition stops the scanner (if it is running) to select the appropriate TU. If the scanner is stopped, the proper TU address

is in the register. Status pending or unit free also sets the status in latch (A-B4) to activate service request which sends request in to the channel, unless suppress out is active. See "Suppress Out." The TC waits for the channel select signal before it can continue. If a higher priority control unit is also requesting service, TC might have to wait for sometime.

When the select signal arrives, the address in latch is set, after a 1.8-microsecond delay, by select out 1 (C3). The address in latch turns off the stack latch (if it is on) and turns on the force burst mode latch (C4), which sets the operational in latch (C5). Operational in (C1) is sent to the channel immediately, to interlock the TC to the interface.

Interrupt Address In

When operational in is set, the combined address of the TC and the selected TU (C3-4) is placed on channel bus in. The address byte P bit is generated by a circuit which is wired at system installation; wiring is determined by the designated tape control address (Systems 01.01.28.1). After a 1.0-microsecond delay, the address in tag (D2) is also sent to the channel, which responds with command out to signal the control unit to proceed.

Interrupt Status In

When command out rises (D1), the gate status to the data register line gates the on state of any status latch to the data register; the status bits shown are the only bits possible for this type of sequence, although not all will necessarily be on. A selected unit free bypasses the device end latch and is gated directly to the data register (circle 10, D4).

The status byte, with a P bit for odd parity (D5), is placed immediately on bus in. After a 3.6-microsecond delay, the address in latch is reset to drop the address in tag to the channel.

With the fall of address in, the channel drops command out. After all command out fall timing is complete, the status in tag latch is set (D2-3) to gate the status in tag to the channel after a 1.0-microsecond delay.

Status Accepted

A service out response to status in (E2) generates a status reset to turn off the status latches (except unit check), and reset the selected tape unit arm latch if it is on. Service out 1 turns off the status in, status in tag, and force burst mode latches. Operational in is reset after the channel drops select out, although select out may be down already.

Status Rejected

A command out response to status in sets the stack latch (B2), unless only unit free caused the interrupt; for a unit free, the internal stack latch is set (F3). With the (interface) stack latch on, status pending is active to prevent initiation of a new operation in the TC. The internal stack latch does not activate status pending; its only function is to prevent loss of the unit free if another unit free (another TU address) is signaled.

With the (interface) stack latch on, another request in sequence is begun, unless suppress out is active. Command out turns off force burst mode to reset operational in and the status latches.

TURNAROUND (FIGURES IOP-8 AND 3-21)

The purpose of turnaround is to cause the TU to change directional status and delay tape motion (for 205 milliseconds) to allow time for TU status to be mechanically changed.

Operation

If the TU is in backward status when a forward command is decoded, forward command (Figure IOP-8) is gated by backward status to set the turnaround latch (D2). If the TU is in forward status and the command is a backward command, backward command is gated by forward status and read status to set the turnaround latch.

Turnaround drives the write clock-delay counter (A3) in millisecond mode to begin turnaround timing. The turnaround signal is gated by not brake latch to send brake to the TU (E3). The brake signal is used in the TU to hold the tape reel brakes on, and protect circuits while its status is changing.

With the brake signal on, the TC sends the signals to change status. Delay counter trigger 128 is AND'ed with forward command (or backward command) (D3) and turnaround to send set forward (or set backward) to the TU 25.6 milliseconds after turnaround starts.

The brake signal is turned off 32 milliseconds after being turned on: delay counter trigger 256 is gated by turnaround to set the brake latch. Turning on the brake latch inhibits brake to the TU.

The TC delays for another 173 milliseconds to allow the capstan motor in the TU to change direction and come up to speed again. At DC 1024 (205 milliseconds), the turnaround latch is reset and forward go (or backward go) is enabled to start tape motion.

Erase before Turnaround

A short (19-millisecond) erase is perfo med prior to turnaround if the TU is in write status when a

read backward command (read backward, backspace block or file) is decoded.

When a backward command is received, setting the turnaround latch is inhibited by read status from the TU. Backward command is gated by not read status to generate the erase forward signal. Erase forward starts the write clock-delay counter and sends go to the TU to move tape.

Count 96 from the delay counter, active 19 milliseconds after starting the delay counter, sends set read to the TU. The TU changes from write status to read status (still moving tape). When read status is received from the TU, erase forward to the delay counter drive and to the go line is inhibited. Read status now enables setting the turnaround latch, and turnaround begins.

An IBM 2415 Model 1, 2, or 3 tape system utilizes nine-track tape units and the NRZI method of coding data. To provide flexibility, and compatibility with earlier tape systems, one or two features can be added:

1. Seven-track feature tape units with seven-track read/write heads can be interchanged with nine-track units. Also, seven-track tape motion control circuits are added to the tape control. Only NRZI coding is used.
2. Data convert feature; for conversion of eight-bit data bytes to six-bit characters or vice versa, if the seven-track feature is also installed. Only NRZI coding is used.

NOTE: Figures 4-1, 4-2, 4-4, IOP-12, IOP-13, IOP-16, and IOP-17 are in the maintenance diagram volume 1.

Seven-Track Operation

Operation of seven-track tape units is similar to operation of nine-track tape units; the differences are in tape stopping delays and data flow.

Stop Delay: A 0.75-inch interblock gap (IBG) is created for seven-track tape write operations; a 0.60-inch IBG is created for nine-track operations. To obtain the additional gap length for seven-track operations, the tape control stop delay time is increased by 6.6 milliseconds before the tape unit is signaled to begin the count run out. Modified tape motion operation in the tape control is controlled by the seven track line from a seven-track tape unit.

Data Flow: Nine-track data flow is modified for seven-track operations to provide compatibility with earlier tape systems. Seven-track operation provides:

1. Densities of 200, 556, or 800 bytes per inch.
2. Either odd or even redundancy parity checking.
3. Translation of eight-bit (hexadecimal) bytes to or from six-bit binary coded decimal (BCD) characters.
4. Processing of the BCD tape mark (bits 8, 4, 2, and 1).

Items 1-3 are controlled by special mode set (control) commands that set the mode register, a functional unit feature, to the desired mode of operation; all four items require the seven track line from a seven-track tape unit for proper control.

NOTE: Because of the similarity between seven- and nine-track tape motion and data flow (nontranslate) controls, differences in functions and operations are explained in the appropriate text throughout Chapters 1, 2, and 3. Functional units that are used primarily for feature operations are explained in this chapter.

Data Conversion

- Data conversion (DC) is an optional feature that allows processing binary seven-track information with maximum packing efficiency.
- Data conversion always uses odd parity mode.
- During a write operation, 3 eight-bit bytes are converted to 4 six-bit characters to be written on tape.
- During a read operation, 4 six-bit characters from the tape unit are converted to 3 eight-bit bytes to be sent to the channel.
- Data conversion cannot be used for read backward operations.
- Position 2 of the mode register controls data conversion. Mode register 2 on represents data convert off.
- Data conversion and translate modes cannot be used at the same time.

Data conversion is an optional feature for a tape control that has the seven-track feature installed. When seven-track data is processed, six bits of each character are useful data. If these six-bit characters are placed in System/360 (eight-bit) storage, two bit positions are unused. Data conversion stores data in all (eight) bit positions to increase storage packing efficiency. Three 8-bit bytes have the same number of information bits (24) as 4 six-bit characters.

Tape controls equipped with this feature can operate with the data converter on or off. When the data converter (DC) is off during a seven-track operation, each six-bit character occupies an eight-bit byte location. The six-bit characters occupy positions 2-7 on the interface bus lines and positions 7-12 in the data register.

Data conversion is automatically turned off during read backward. If the characters are read in reverse order, the bits cannot be placed in the proper byte sequence on the bus in lines.

FUNCTIONAL UNITS FEATURE

Mode Register (Figure 4-1)

- Mode register consists of five latches that are set by command byte bits 0-4.
- Density, parity, translate, and data convert modes are set for a seven-track operation only.
- Nine-track operation forces 800 bpi, odd parity, and translate and data convert off.

The mode register consists of five latch positions; it receives bits 0-4 from the command register when a mode set (control) command is issued during initial selection. Bits in the mode register set the modes or operating conditions for a seven-track operation. These modes are: 200, 556, or 800 bpi density, even or odd parity, data convert on or off, and translator on or off. No operation and diagnostic are the only modes that can be set for a nine-track NRZI operation.

A mode set command is identified by no bit 5 and bits 6 and 7 in the command byte. The command is decoded at the command register and AND'ed with either bit 3 but not 4, or with bit 2. This prevents no operation and diagnostic modes from setting the mode register. Diagnostic mode (for CE diagnostic use) is set by a separate circuit by bit 4 but not bit 2. Diagnostic mode prevents writing a P bit, so that error detection circuits may be checked.

When it is desired to set modes (such as density or translate) to be effective at the same time as diagnostic mode, two mode set commands must be used and the diagnostic mode set command issued last. This is necessary because diagnostic mode does not reset the mode register, but other mode sets do reset the mode register.

The mode register is reset during a mode set command at command out 2 not command out 3 time. Mode set is effective at this time, also, but it remains effective, after the reset line drops, to set bits from the command register into the mode register. The mode register setting remains active for all succeeding command operations, unless another mode set command is received or machine reset is activated. Note that machine reset causes the mode register 0 latch to be turned on. This sets density at 800 bpi (the reset condition). A no operation or diagnostic mode set does not reset the mode register.

Nine-track operation forces 800 bpi, translate and data convert off, and odd redundancy mode. Also, data convert is forced off for a read backward command.

Translators (Figures 4-2, 4-3, IOP-12N, and IOP-16N)

- Translate can be used when writing or reading seven-track tape.
- Write translate circuits are separate from read translate circuits.
- Mode register 4 turns on the translators.
- The write translator changes eight-bit code to six-bit code.
- The read translator changes six-bit code to eight-bit code.
- A substitute blank character is used when six-bit code is in even parity.

A translator is a group of AND and OR circuits that changes back and forth between the eight-bit hexadecimal code and the six-bit (BCD) code used on seven-track tape systems (Figure 4-3). Data translation is not a separate feature; it is an option included with the seven-track feature.

Translate On

Translate is turned on by the on state of the mode register 4 latch. During a nine-track operation, the register 4 output is deconditioned. During a seven-track operation, bit 4 in a mode set command sets mode register 4 to turn on translate; it remains on until the mode register is reset by another mode set command or by a machine reset.

Write translate circuits are connected between data register outputs and the write triggers, and these circuits automatically change the eight-bit code to the six-bit code as data passes through the translator. Read translate circuits are connected between the read register outputs and data register inputs, and these circuits change the six-bit code to the eight-bit code as data passes through the translator. See Figures IOP-12N and 13N for seven-track data flow.

When translate is on, two of the bit positions do not pass through the translator. For any character, bit positions 5 and 7 of the eight-bit code are always the same as bit positions 4 and 1 of the six-bit code; therefore, translation is unnecessary.

Translate Off

When a tape control unit with the seven-track feature installed operates with a nine-track tape unit, the eight-bit code bits pass unchanged through both the

Collating Sequence	Graphics 8 Bit	Graphics BCD	8 Bit Code 0	1	2	3	4	5	6	7	BCD B	A	8	4	2	1
00	blank	blank	0	1	0	0	0	0	0	0	0	0	0	0	0	0
01	.	.	0	1	0	0	1	0	1	1	1	1	1	0	1	1
02	←	¤)	0	1	0	0	1	1	0	0	1	1	1	1	0	0
03	(	[	0	1	0	0	1	1	0	1	1	1	1	1	0	1
04	+	<	0	1	0	0	1	1	1	0	1	1	1	1	1	0
05	GM	GM	0	1	0	0	1	1	1	1	1	1	1	1	1	1
06	&	& +	0	1	0	1	0	0	0	0	1	1	0	0	0	0
07	$	$	0	1	0	1	1	0	1	1	1	0	1	0	1	1
08	*	*	0	1	0	1	1	1	0	0	1	0	1	1	0	0
09	)	]	0	1	0	1	1	1	0	1	1	0	1	1	0	1
10	;	;	0	1	0	1	1	1	1	0	1	0	1	1	1	0
11	MC	MC	0	1	0	1	1	1	1	1	1	0	1	1	1	1
12	-	-	0	1	1	0	0	0	0	0	1	0	0	0	0	0
13	/	/	0	1	1	0	0	0	0	1	0	1	0	0	0	1
14	,	,	0	1	1	0	1	0	1	1	0	1	1	0	1	1
15	%	% (	0	1	1	0	1	1	0	0	0	1	1	1	0	0
16	WS	WS	0	1	1	0	1	1	0	1	0	1	1	1	0	1
17	↑	\	0	1	1	0	1	1	1	0	0	1	1	1	1	0
18	SM	SM	0	1	1	0	1	1	1	1	0	1	1	1	1	1
19	♭	♭	0	1	1	1	1	0	1	0	0	1	0	0	0	0
20	#	# =	0	1	1	1	1	0	1	1	0	0	1	0	1	1
21	@	@ '	0	1	1	1	1	1	0	0	0	0	1	1	0	0
22	▽	:	0	1	1	1	1	1	0	1	0	0	1	1	0	1
23	=	>	0	1	1	1	1	1	1	0	0	0	1	1	1	0
24	TM	TM	0	1	1	1	1	1	1	1	0	0	1	1	1	1
25	♁	♁	1	1	0	0	0	0	0	0	1	1	1	0	1	0
26	A	A	1	1	0	0	0	0	0	1	1	1	0	0	0	1
27	B	B	1	1	0	0	0	0	1	0	1	1	0	0	1	0
28	C	C	1	1	0	0	0	0	1	1	1	1	0	0	1	1
29	D	D	1	1	0	0	0	1	0	0	1	1	0	1	0	0
30	E	E	1	1	0	0	0	1	0	1	1	1	0	1	0	1
31	F	F	1	1	0	0	0	1	1	0	1	1	0	1	1	0
32	G	G	1	1	0	0	0	1	1	1	1	1	0	1	1	1
33	H	H	1	1	0	0	1	0	0	0	1	1	1	0	0	0
34	I	I	1	1	0	0	1	0	0	1	1	1	1	0	0	1
35	♁	♁	1	1	0	1	0	0	0	0	1	0	1	0	1	0
36	J	J	1	1	0	1	0	0	0	1	1	0	0	0	0	1
37	K	K	1	1	0	1	0	0	1	0	1	0	0	0	1	0
38	L	L	1	1	0	1	0	0	1	1	1	0	0	0	1	1
39	M	M	1	1	0	1	0	1	0	0	1	0	0	1	0	0
40	N	N	1	1	0	1	0	1	0	1	1	0	0	1	0	1
41	O	O	1	1	0	1	0	1	1	0	1	0	0	1	1	0
42	P	P	1	1	0	1	0	1	1	1	1	0	0	1	1	1
43	Q	Q	1	1	0	1	1	0	0	0	1	0	1	0	0	0
44	R	R	1	1	0	1	1	0	0	1	1	0	1	0	0	1
45	RM	RM	1	1	1	0	0	0	0	0	0	1	1	0	1	0
46	S	S	1	1	1	0	0	0	1	0	0	1	0	0	1	0
47	T	T	1	1	1	0	0	0	1	1	0	1	0	0	1	1
48	U	U	1	1	1	0	0	1	0	0	0	1	0	1	0	0
49	V	V	1	1	1	0	0	1	0	1	0	1	0	1	0	1
50	W	W	1	1	1	0	0	1	1	0	0	1	0	1	1	0
51	X	X	1	1	1	0	0	1	1	1	0	1	0	1	1	1
52	Y	Y	1	1	1	0	1	0	0	0	0	1	1	0	0	0
53	Z	Z	1	1	1	0	1	0	0	1	0	1	1	0	0	1
54	0	0	1	1	1	1	0	0	0	0	0	0	1	0	1	0
55	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	1
56	2	2	1	1	1	1	0	0	1	0	0	0	0	0	1	0
57	3	3	1	1	1	1	0	0	1	1	0	0	0	0	1	1
58	4	4	1	1	1	1	0	1	0	0	0	0	0	1	0	0
59	5	5	1	1	1	1	0	1	0	1	0	0	0	1	0	1
60	6	6	1	1	1	1	0	1	1	0	0	0	0	1	1	0
61	7	7	1	1	1	1	0	1	1	1	0	0	0	1	1	1
62	8	8	1	1	1	1	1	0	0	0	0	0	1	0	0	0
63	9	9	1	1	1	1	1	0	0	1	0	0	1	0	0	1

FIGURE 4-3. EIGHT-BIT CODE -- BCD RELATIONSHIP

read and write translators. When the tape control writes with a seven-track tape unit with the translator off, bits 2-7 pass through the write translator unchanged. (The blank character is a special case which will be discussed later.) Bits in positions 0 and 1 are dropped. When seven-track tape is read, bits 2-7 pass through the read translator unchanged, and zeros are entered in bit positions 0 and 1.

Parity Bit

A parity bit is never translated. In all cases, the original parity bit is dropped and a new one is generated for the new character being written on tape or for the byte sent to the channel on bus in. The eight-bit code is always in odd parity; the six-bit code has either even or odd parity as specified by the mode register setting.

Substitute Blank

Translating a blank is a special case. In the six-bit code, a blank is represented by the absence of bits in all seven positions; in odd parity mode, the parity bit (C bit) is present. In even parity mode, the parity bit is absent and no bits are written on tape. To prevent this condition, a substitute blank, consisting of an A bit, is provided. Since the translator is in even parity mode, the C bit is also present and the character is written on seven-track tape as bits in the C and A positions. During a read translate operation, the substitute blank is translated to the standard eight-bit blank consisting of a bit in position 1.

When writing on seven-track tape in even parity with translate off, a substitute blank is used to avoid writing a character with no bits. For this condition, the eight-bit blank is translated to the six-bit substitute blank even though the translator is off.

Writing a six-bit substitute blank for an eight-bit blank normally causes a C-compare error, but this special case is not an error condition. During a write operation, the -S blank even line prevents setting a C-compare error (circle 1, Figure 4-2).

Byte Counter and Character Counter (Figure 4-4)

- Counters control data flow gating through the TC during write or read data convert operations.
- Byte counter gates eight-bit bytes into the data register during write and out of the data register during read.
- Byte counter also gates eight-bit bytes to bus out parity check from the data register during write and P-bit injector during read.
- Character counter gates six-bit bytes out of the data register during write and into the data register during read.
- Character counter also gates data register resets for both read and write operations.
- Both counters control C-compare checking and service in blocking during read and write operations.
- Both counters are reset at end of either type of operation.

Data conversion data flow through the data register is controlled completely by the byte and character counters. Data flow is grouped in segments of 24 bits; 3 eight-bit bytes make up 4 six-bit characters. The byte counter gates the eight-bit bytes to and from the bus lines and to and from the particular data register positions. The character counter gates divided eight-bit bytes as six-bit characters to and from the tape unit and to and from the particular data register positions. Channel service for a byte is suspended for one clock cycle by the byte counter for each group of four characters processed.

Both counters are reset when the data convert line from the mode register is deconditioned by read disconnect at the end of either a read or write operation.

Byte Counter

A simple two-stage binary counter (which counts to four: 0, 1, 2 and 3) is used as a byte counter. Byte counts 1, 2, and 3 gate bytes to and from the appropriate data register positions; count 0 does not gate data bytes. For every 3 eight-bit bytes (24 bits) processed during data convert operations, one service in request is suspended by:

1. Count 0 during the third of four character cycles during write operations.
2. Count 1 (and character count 2-4) during the first of four character cycles during read operations.

Byte count 0 is active when the counter is held reset by not data convert; however, not data convert degates the count 0 output and forces up the count 3 output for nondata conversion operations. See the bottom of Figure 4-4.

Byte Counter Stepping: During data convert write operations, the first counter step pulse (to step from 0 to 1) is generated by status reset at the end of initial selection. When the first eight-bit byte arrives from the channel (after 4.0 milliseconds of write delay), count 1 gates the byte into the appropriate data register positions. From this point, the counter is stepped by a WC4, 5 pulse during each write clock cycle for the remainder of the operation.

During data convert read operations, the first step pulse is generated by the service out response to initial status in; the counter steps from 0 to 1 and remains at 1 until the second character is read from tape. Service out responses to service in requests step the counter through 2 and 3, then back to 0. Because service in is blocked during the next character cycle (again, the first of a group of four) and no service out is available, an RC2, 3 clock pulse steps the byte counter from 0 to 1. This same procedure is repeated continually for the read operation.

Character Counter

A single binary trigger (TB) is used as a character counter (Figure 4-4). When the TB is on, it gates either the first or third character of a group of four; when it is off, it gates either the second or fourth character of a group of four. When the mode register output line data convert is deconditioned (minus), the TB is held reset and character count 2 or 4 remains active for nondata convert gating.

Character Counter Stepping: During write operations, the TB is turned on by the status reset pulse at the end of initial selection. For the remainder of the write operation, the TB is turned off with one WC7 pulse; and the TB is turned on with the next WC7 pulse to gate odd numbered characters then even numbered characters from the data register to the tape unit.

During read operations, the TB is turned on and off with an RC2, 3 pulse during every read clock (character) cycle. The read clock is started by the first bit latch when the first bit of each character is read from tape.

DATA CONVERT THEORY OF OPERATION

Tape motion control for data convert operations is identical to all other seven-track operations; the only difference in operation is data flow through the tape control. The reader should study write and read theory of operation in Chapter 3 before attempting to understand data conversion data flow. Figures IOP-13N and IOP-17N depict data flow for data convert write and read operations.

Write Data Convert (Figure IOP-17N)

When data convert is active from the mode register during a write operation, tape control converts 3 eight-bit data bytes from the channel to 4 six-bit characters, and transmits 1 six-bit character to the tape unit during each write clock cycle. The byte and character counters generate input and output gates for the data register.

Byte counter outputs gate bytes into the data register: count 1 sets positions 1-8; count 2 sets positions 1-4, and 9-12; count 3 sets positions 5-12. Character counter outputs gate characters from the data register to the tape unit: the first and third output characters from the data register are taken from positions 1-6; the second and fourth output characters from the data register are unloaded from positions 7-12. Each six-bit character is gated by the write pulse and deskewing circuits to the tape unit.

Tape control does not request a data byte from the channel after transferring the third character from the data register to the tape unit. The byte and character counters step once during each write clock cycle. The following is the sequence of a write convert operation. See Figures IOP-17N and 4-4:

1. Service out response to initial selection status in begins write delay, and steps byte counter to 1 and steps character counter to 1-3.
2. Send service in to the channel for first byte after 4.0 milliseconds of write delay.
3. Service out (delayed) response from the channel sets byte into data register positions 1-8 gated by byte count 1.
4. After the 7.0-millisecond write delay is complete, start write clock.
5. Character count 1-3 gates first character from data register positions 1-6; write character at WC3 time.
6. WC4, 5 steps byte counter to 2.
7. WC7 steps character counter to 2-4, and sets service in latch for next byte.
8. Service out (not service out 1) response resets data register positions 1-6.
9. Service out 1 sets next byte into data register positions 1-4 and 9-12, gated by byte count 2.
10. Character count 2-4 gates data register positions 7-12 to write character at next WC3.
11. Next WC4, 5 steps byte counter to 3.
12. Next WC7 steps character counter to 1-3, and sets service in latch for next byte.
13. Service out (not service out 1) resets data register positions 7-12.
14. Service out 1 sets next byte into data register positions 5-12, gated by byte count 3. (Data register now contains two complete characters.)
15. Character count 1-3 gates data register positions 1-6 to write character at next WC3.
16. Next WC4, 5 steps byte counter to 0.
17. Next WC7 steps character counter to 2-4; service in is blocked for this write clock cycle.
18. Next WC9 and byte count 0 reset data register positions 1-6 (service out is not forthcoming).
19. Character count 2-4 gates data register positions 7-12 to write character at next WC3.
20. Next WC4, 5 steps byte counter to 1.
21. Next WC7 steps character counter to 1-3, and sets service in for another byte.

The first four characters (24 bits or 3 bytes) have been written on tape and the counters are at the same count settings as they were when the operation began; repeat steps 3-21 (except step 4) for the remainder of the tape block.

Stop Write: If the channel responds with command out instead of service out, the operation is terminated. Service in and command out can turn on the stop trigger, regardless of the counter settings.

If the stop trigger is on when the byte counter is at count 1, data transfer stops and write condition is reset. When the byte counter is at any other setting when the stop trigger is set, write disconnect and the reset of write condition are blocked for one more character (write clock) cycle to process the bits remaining in the data register (some register positions are blank).

An extra cycle is provided by the require one more cycle latch which is turned on every WC5 during the entire operation, except when byte count 1 is active. Write disconnect is blocked by this latch to allow one more write clock cycle before write condition is reset and the write clock-delay counter 16 trigger is allowed to turn on. The one more cycle latch is shown at the bottom of Figure 2-18.

Error Checks: A bus out check is made for each byte from the channel. Because the parity check is performed at the data register outputs, byte counts rather than character counts gate each byte to the parity circuit. Byte count 1, for example, gates a byte into data register positions 1-8 and also gates positions 1-8 to the parity circuit so that the parity of all eight bits is checked.

C-compare circuits cannot make a byte-for-character check due to the difference in bit count. However, a compare check is made of each group of 24 bits, representing three bytes or four characters. Parity for 24 bits must be the same regardless of how the bits are grouped, although a P-bit adjustment is made if characters are written using even redundancy parity checking. A C-compare error sample is generated after each group of 24 bits is processed.

Read Data Convert (Figure IOP-13N)

When data convert is active from the mode register during a read operation, the tape control converts groups of 4 six-bit characters from tape to groups of 3 eight-bit bytes. The byte and character counters generate input and output gates for the data register.

Character counter outputs gate characters into the data register: count 1-3 gates the first or third character into positions 1-6; count 2-4 gates the second or fourth character into positions 7-12. Byte counter outputs gate bytes out of the data register to the channel bus in: count 1 gates the first byte from positions 1-8; count 2 gates the second byte from positions 1-4 and 9-12; count 3 gates the third byte from positions 5-12.

A service in request is generated only when at least eight bits (one byte) are available in the data register. For every four input six-bit characters to the data register, only three service in requests are generated (after the second, third, and fourth characters are read). The following is the sequence of a read convert operation. See Figures IOP-13N and 4-4:

1. Service out response to initial selection status in steps the byte counter from 0 to 1; read delay begins.
2. Service out and not service out 1(status reset) resets the entire data register.
3. When the first bit of the first character is read (after read delay is complete), the first bit latch is set to run the read clock for one cycle.
4. RC2, 3 steps the character counter to 1-3.
5. First character latch then character count 1-3 are AND'ed with byte count 1 to activate inhibit first service in; a complete eight-bit data byte is not available.
6. RC8 sets the first of four characters in data register positions 1-6, gated by character count 1-3.
7. The second of four characters is read to restart the read clock.
8. RC2, 3 steps the character counter to 2-4 which drops inhibit first service in.
9. RC8 and count 2-4 set the second of four characters into data register positions 7-12; data register is full.
10. Byte count 1 gates first byte (of group of three) from data register positions 1-8 to the channel (bus in).
11. Fall of RC9 (strobe pulse) generates service in to the channel.
12. Service out (not service out 1) response steps byte counter to 2.
13. Fall of service out resets data register positions 1-6.
14. Third character of the first bit is read and restarts the read clock.
15. RC2, 3 steps character counter to 1-3.
16. RC8 and count 1-3 sets third character into data register positions 1-6.
17. Byte count 2 gates second byte from data register positions 1-4 and 9-12 to bus in.
18. Fall of RC9 generates service in to the channel.
19. Service out response steps byte counter to 3.
20. Fall of service out resets data register positions 7-12.

21. Fourth character of the first bit is read and restarts the read clock.

22. RC2, 3 steps character counter to 2-4.

23. RC8 and count 2-4 set the fourth character into data register positions 7-12.

24. Byte count 3 gates the last of three bytes from data register positions 5-12.

25. Fall of RC9 generates service in to the channel.

26. Service out steps byte counter to 0.

27. Fall of service out and count 0 resets entire data register.

28. Four characters have been read and sent to the channels as three bytes; the next character (first of another group of four) restarts the read clock.

29. RC2, 3 steps the byte counter to 1 and steps the character counter to 1-3; byte count 1 and not character count 2-4 activate inhibit first service read byte 1 to block service in.

Repeat steps 6-29 for the remainder of the tape block.

Stop Read: Read operations can be terminated either by the tape control sensing the end of data or the channel refusing to accept more data. If the channel responds to service in with command out, the stop trigger turns on and blocks service in. No more data is transmitted to the channel; however, the tape control continues reading until the end of block is sensed.

When the tape control ends the operation, the status of information in process is determined if an additional service in is needed. Some bits remain in the data register after the last character is read because there is not an even multiple of four characters on tape. See "Data Convert Check." Another service in is necessary to send the "leftover" bits, plus blanks to complete a byte, to the channel.

Data Convert Check

When a block read from tape does not contain a multiple of four characters, there may be one, two, or three characters processed during the last byte counter cycle. (For a complete cycle, the byte counter must step through all four counts.) Data convert checking circuits (Figure 4-5) detect the need for an additional service in request in addition to signaling a data convert check.

During EOB timing, the set data convert check line, activated by EOB 1.5 characters, sets the service in latch and data convert check (DCC) latch if a group of less than four characters was read as the last data on tape. However, set data convert (and service in) is not necessary if certain positions of the data register are blank; these conditions are explained in the following text.

One Character Left at EOB: Byte count 1 causes EOB 1.5 characters to set service in and DCC. The last character in data register positions 1-6 and blanks from positions 7 and 8 are sent to the channel as the last byte. The DCC signal is an indication to the system program that the last byte sent has been "padded" with blanks.

Two Characters Left at EOB: Of the 12 bits in the data register, the first byte (positions 1-8) is sent to the channel in a normal manner before EOB 1.5 time. The last four bits of the second (last) character are in data register positions 9-12. At EOB 1.5 characters, set data convert check is generated by byte count 2 only if any of positions 9-12 contains a bit. If no bits are present, the set of service in and DCC is blocked and the operation ends normally. If at least one bit is present, data register positions 9-12 (as received from tape) and blank positions 1-4 are sent to the channel as the last byte. DCC is set to signal the byte is padded.

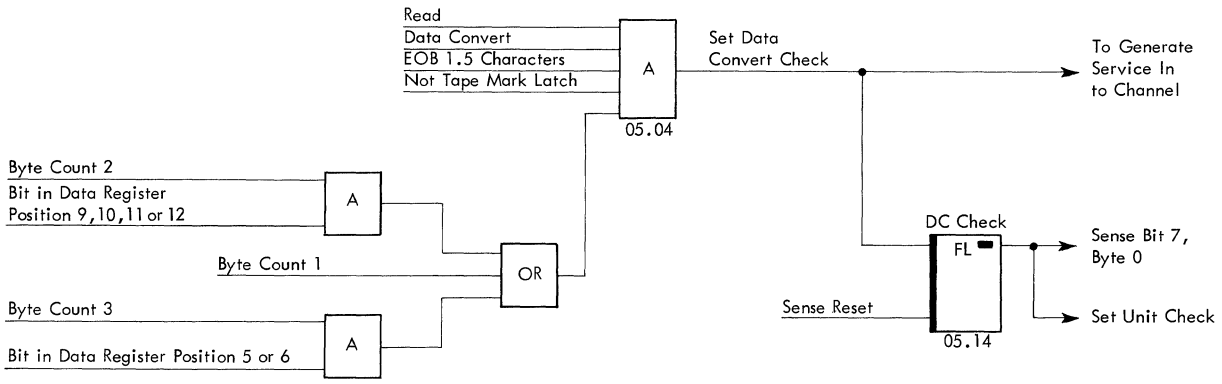


FIGURE 4-5. DATA CONVERT CHECK (DCC)

Three Characters Left at EOB: Two complete eight-bit bytes are sent to the channel in the normal manner before EOB timing reaches 1.5 character spaces. The two remaining bits of the third (last) character are in data register positions 5 and 6. If neither register position contains a bit, the operation is terminated normally without signaling a DCC. If either position contains a bit, service in and DCC are set by byte count 3, and the last byte is padded with blanks from data register positions 7-12.

- The TC power supply provides all ac and dc power for the TC and all attached tape units.
- In remote operation, the channel provides sequential power-on control and parallel power-off control of all attached control units.
- In local operation, the power supply is controlled by the power on/off switch, providing the channel is not indicating emergency power off (EPO).
- The power supply is turned on in a sequence that ensures that an overload condition in one area of the TC or any tape unit removes dc power to all preamplifier, amplifier, and logic cards, and ac power to the capstan, reel drive, and vacuum pump motors.

Power for the 2415 TC and all attached tape units is provided by a power supply (Figure 5-1) located in the frame that contains the TC (frame 1). The power supply receives input power from a single three-phase power source (such as wall power) and provides ac and dc power for the TC logic, all tape unit logic and amplifiers, all tape unit motors, all fans, and the channel power-control relay contacts. The three-phase input power passes through a feedthrough capacitor, to filter out line noise, to circuit breaker CB1.

Two output lines from CB1 provide a single-phase, 208-vac input for power supply PS5. The -24 volt output from PS5 is available within the power supply whenever wall power is on and CB1 is closed. The power-supply control switches and the channel power-control relay contacts do not affect PS5.

POWER-ON SEQUENCE, REMOTE OPERATION

With the remote/local switch set to REMOTE and the power switch set to ON, the power supply is controlled by three relay contacts in the channel. The -24 volt output from PS5 provides power for all three contacts. The system EPO contacts are held closed as long as channel power is on and no emergency condition occurs to open the contacts. The system EPO output from the channel is connected to all control units in parallel.

To turn on all connected control units sequentially, the channel closes a system-on relay contact to all connected control units. A channel-step (rotary) switch closes a set of contacts for only one control unit at a time. That control unit brings up its power and sends a power-up signal to the channel. The channel then steps the channel-step switch one position and a set of contacts closes for the next control unit.

The -24 volt output from PS5 provides power through de-energized relay contact K1-2, circuit breakers CB3 and CB4, and the circuit breaker in each of the 12 volt power supplies to the coil of relay K2. Relay contacts K2-1 and K2-2 are picked.

When the channel-step switch to the 2415 TC closes, -24 volts through the system EPO and system-on contacts in the channel is sent through the closed power on/off switch to energize relay K1. Contact K1-3 closes and -24 volts is applied, through contact K2-2, to the coil of relay K5. The three-phase source power is now gated through the contacts of K5 and circuit breaker CB2 to supply ac power to the fans and motors in all frames.

The phase 1 and 3 lines from the K5 contacts supply input power for the four 12 volt power supplies. Circuit breaker CB2 is not necessary in the input to these supplies due to the circuit breaker in each supply.

Overload Control

Circuit breaker CB1, located in the input power lines, provides overload protection for the over-all power supply circuit. Opening CB1, due to a power supply malfunction or by operating the CB manually, removes all ac and dc power from the power supply and the 2415.

Circuit breaker CB2, located in the output power lines to the fans and motors, provides overload protection for the vacuum and capstan motors in all tape units, the meter circuit in tape unit 0, and the fans that cool all tape unit and TC circuits.

Circuit breakers CB3 and CB4 and the circuit breaker in each of the four 12 volt power supplies control relay K5 to remove all ac and dc output power in case of failure of a single circuit breaker. CB3 is in the 115-vac line to the reel motors in all tape units. CB4 is in the 12-vac line to the control gates of the reel motors. An open CB3 or CB4 indicates a malfunction in a reel motor circuit in one of the tape units. A malfunction in one of the 12 volt power supplies or an overload in the output of one of the supplies results in an open circuit breaker for that supply.

Opening one of the six circuit breakers removes power from the K2 coil. With contact K2-1 open, restoration of the circuit breaker will not re-energize K2. The normally closed contact of K2-1 gates -24 volts to the power check light. Contact K2-2 opens and removes power from the K5 coil. The four contacts of K5 open and block all ac power outputs, the

-24 volt output, and, by removing input power to the 12 volt power supplies, all 12 volt outputs.

Restoring Power after Overload

Relay K2 is normally energized through the normally closed contact K1-2. Relay K1 remains energized when a circuit breaker opens (except for CB1), so that K2 cannot be energized in the normal manner. With the reset pushbutton depressed, contact K1-2 is bypassed to energize K2 and restore power to K5 coil, providing the circuit breaker that opened has been reclosed and the malfunction that caused it to open has been corrected.

POWER CONTROLS

The power supply controls consist of a check light, an on/off and a remote/local switch, and a reset pushbutton. Either of two conditions can turn on the check light:

1. Opening one of the six circuit breakers in the K2 coil circuit. Power through normally closed contact K2-1 turns on the check indicator. The malfunction that opened the circuit breaker must be corrected, the circuit breaker closed, and the reset pushbutton pressed.

2. Closing CB1 with the remote/local switch set to LOCAL and the on/off switch set to ON. Relay K1 can energize prior to K2, and the K2 turn-on circuit path through normally closed contact K1-2 is opened, preventing turn-on of K2. Pressing the reset pushbutton energizes K2 and turns off the check indicator.

The on/off switch controls power supply operation only when the remote/local switch is set to LOCAL. In remote operation, setting the on/off switch to OFF de-energizes K1 which removes power from the K5 coil. Opening the K5 contacts turns off all output power from the power supply. To restore power with the on/off switch, the remote/local switch must first be set to LOCAL. In local operation, the channel system-on and channel-step switch contacts are bypassed. The on/off switch, then, controls power supply operation, providing that the system EPO switch in the channel is closed.

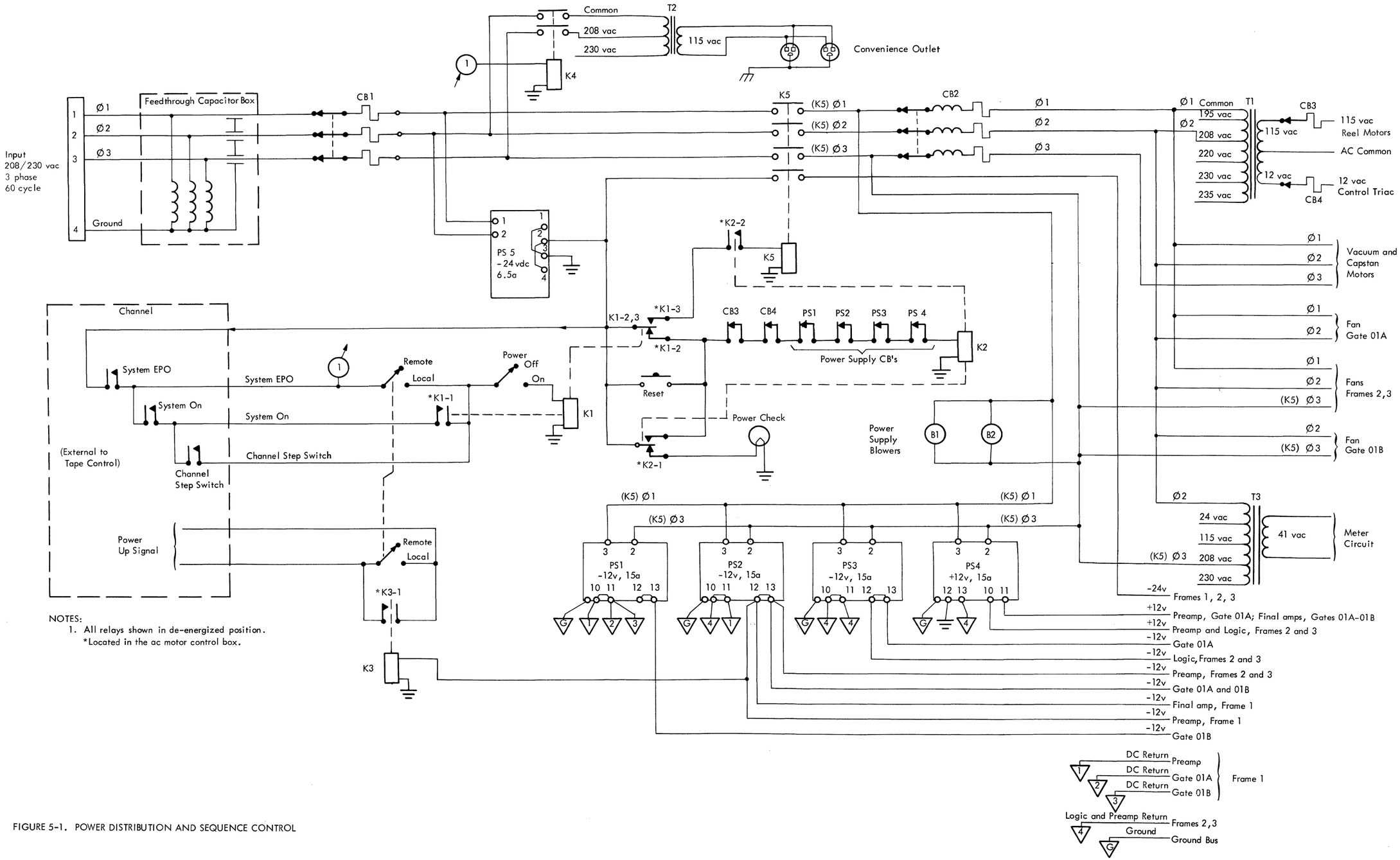


FIGURE 5-1. POWER DISTRIBUTION AND SEQUENCE CONTROL

SECTION 1. CONSOLE

The IBM 2415 Magnetic Tape Unit and Control is provided with a customer engineering (CE) panel. The CE panel (Figure 6-1) is at the rear of the frame that contains the TC. Since this panel operates the tape units through the TC circuitry, the TC is disconnected from the channel when the CE panel is used.

CE PANEL OPERATION

The CE panel controls are divided into functional groups for discussion here. These groups, and the text heading for each, are shown in Figure 6-2.

Power Controls

Refer to Chapter 5 for a description of the power check light, on/off switch, remote/local switch, and reset pushbutton.

Start, Stop, and Reset

The start, stop, and reset pushbuttons on the left side of the CE panel control all CE panel operations. The start switch initiates an operation, providing that the TC was in a reset status prior to pressing the switch. Pressing the stop switch terminates an operation; the TC remains in the condition it is in at the moment the switch is pressed (some latches on). Pressing the reset pushbutton stops an operation and resets the TC.

A remote start/reset switch (P/N 454304) plugs into the socket just above the start switch on the CE panel. The start and the reset pushbuttons on this switch box perform the same function as the pushbuttons on the CE panel.

On-Line and Off-Line

The TC is on-line (controlled by the channel) when the command switch is set to ON LINE, and is off-line when the command switch is set to any other position.

When on-line, all controls on the CE panel are disabled except the power control switches and the two check stop switches. When off-line, all controls on the CE panel are enabled, and the TC must be operated from the CE panel.

In off-line mode, all tags and bus lines between the channel and the TC are disabled, except select out. Select out is bypassed through a relay to either the next control unit or to the channel, depending on priority of the 2415 TC.

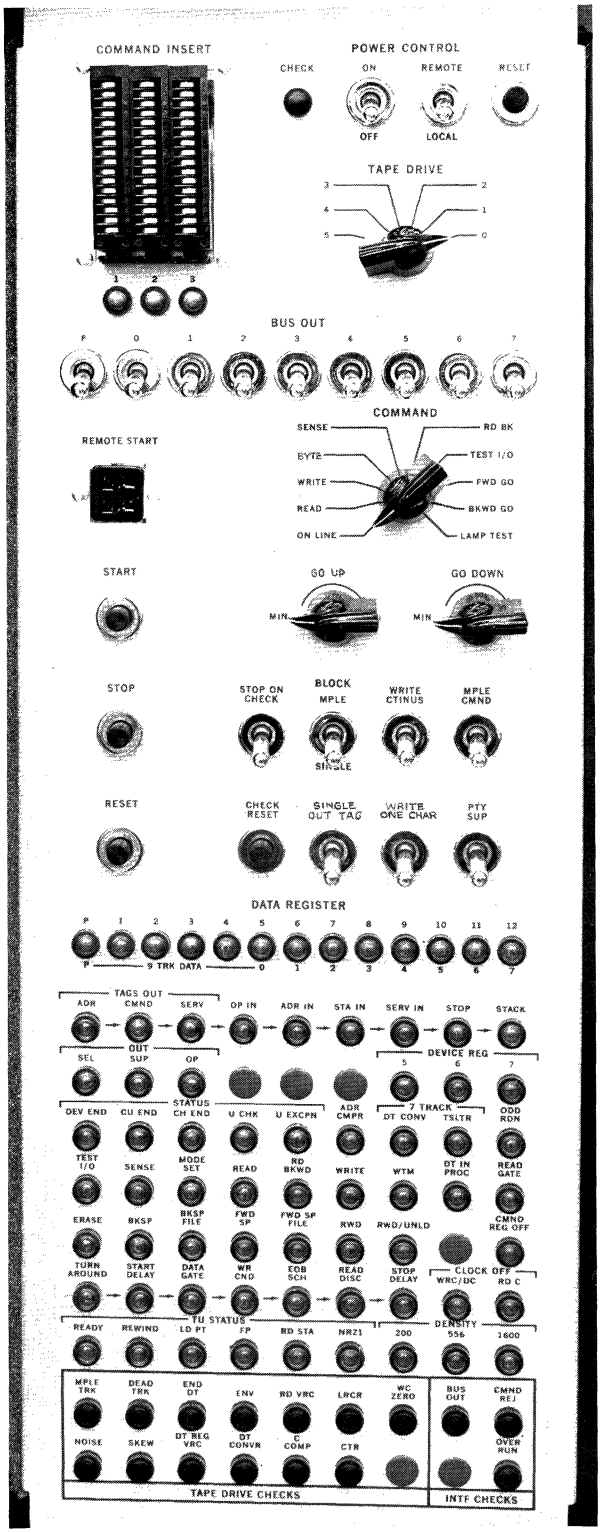


FIGURE 6-1. IBM 2415 CE PANEL

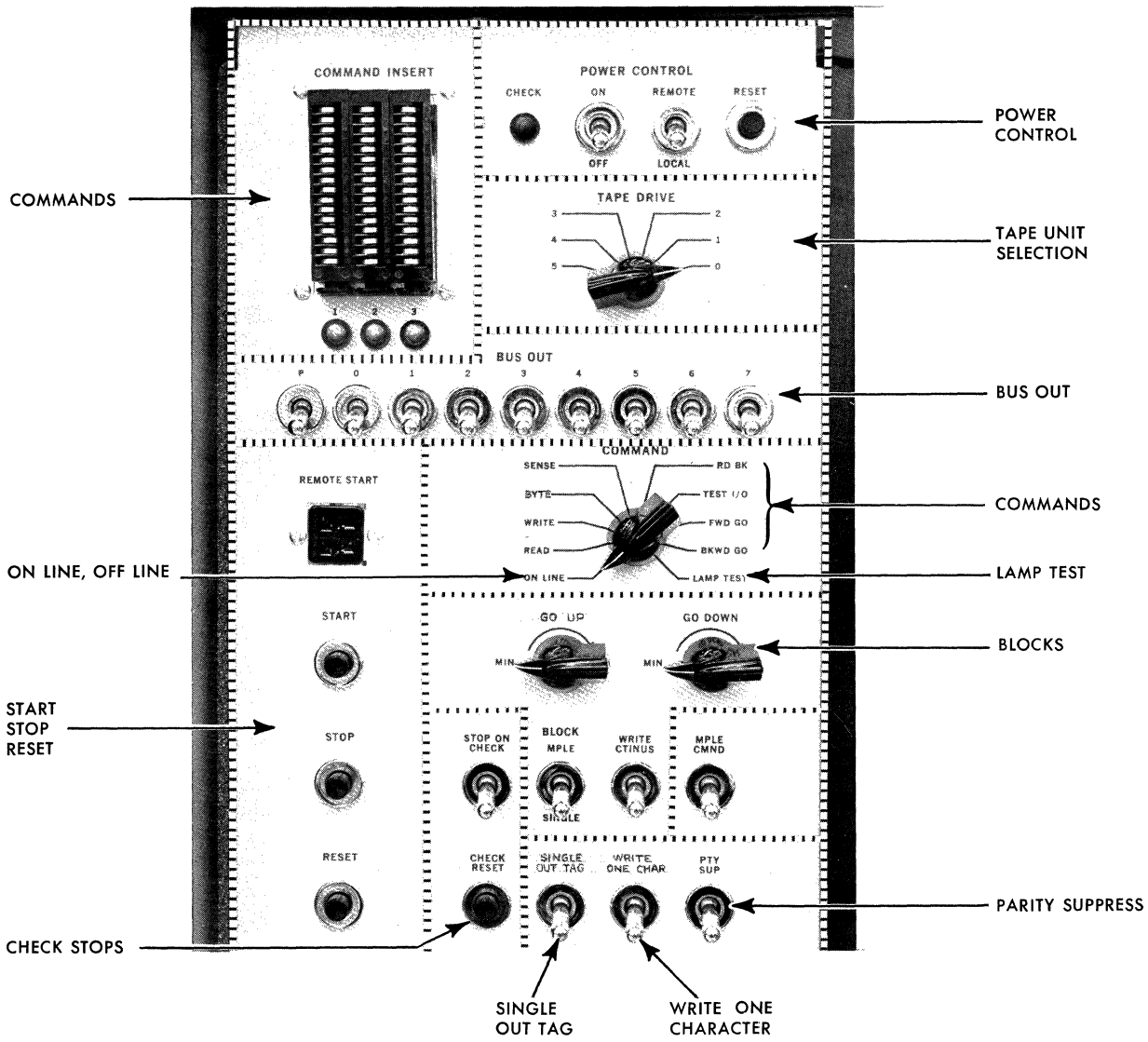


FIGURE 6-2. FUNCTIONAL GROUPING OF CE PANEL CONTROLS

CAUTION

Tape motion should be halted prior to changing the position of the command switch to lessen the possibility of component damage.

Tape Unit Selection

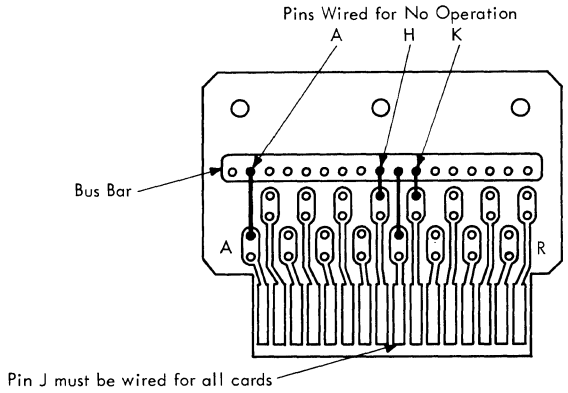
When off-line, a tape unit is selected from the CE panel by setting the tape drive switch to the address number of the desired tape unit.

Commands

Single commands are initiated from the CE panel by setting the command switch to any position other than ON LINE. The TC and selected tape unit then perform the designated command. This designated command is either the command selected by the setting of the command switch, or a command selected by the setting of the bus out switches with the command switch set to BYTE (control command). The bus out switches are set according to the chart shown in Figure 6-3.

Multiple commands are performed by setting the multiple command switch to the up position and inserting command cards in all three of the command insert card positions (in the upper left corner of the CE panel). The TC and selected tape unit then perform four commands in sequence (three commands selected by command cards, followed by the command selected by the command switch).

Command cards are wired to perform any of the tape unit commands (one command per card). See Figure 6-3 for wiring instructions for the command cards.



NOTES:
1. Card illustrated is wired for no operation (A, H, and K).
2. Connect pin J to bus bar, and connect pins specified in code table to bus bar.
3. Card Part Numbers:

Blank	491349
Read	5414365
Read Backward	5414364
Write	5414363

4. Set P bit to obtain odd parity.
5. Use mode set 1 density set for card pins B and C.

	P	0	1	2	3	4	5	6	Gnd	7	
Command	A	B	C	D	E	F	G	H	J	K	← Pin Name
Test I/O	X								X		
Read								X	X		
Read Backward	X					X	X		X		
Sense							X		X		
Write									X	X	
No Operation	X							X	X	X	
Control:				C	C	C	X	X	X	X	
Rewind							X	X	X	X	
Rewind-Unload	X					X	X	X	X	X	
Erase Gap	X				X		X	X	X	X	
Write Tape Mark					X	X	X	X	X	X	
Backspace Block	X			X			X	X	X	X	
Backspace File				X		X	X	X	X	X	
Forward Space Block				X	X		X	X	X	X	
Forward Space File	X			X	X	X	X	X	X	X	
Mode 1 Set: (NOTE 5)		D	D	M	M	M		X	X	X	
Diagnostic Use →		D	D			X		X	X	X	
(NOTE 4)		D	D		X			X	X	X	
		D	D	X				X	X	X	
		D	D	X		X		X	X	X	
		D	D	X	X			X	X	X	
		D	D	X	X	X		X	X	X	

Model 1 Density Set

Density (bpi)	B	C
200		
556		X
800	X	

Mode Modifiers

Set Density	Set Odd Parity	Set Even Parity	Turn On Data Converter	Turn Off Data Converter	Turn On Translator	Turn Off Translator
X	X		X			X
X		X		X		X
X		X		X	X	
X	X			X		X
X	X			X	X	

FIGURE 6-3. COMMAND CARD WIRING

When multiple commands are performed, all three command insert positions must contain cards. If just two or three commands are desired, cards wired for no operation (Figure 6-3) may be inserted in one or two of the card positions.

Lamp Test

All indicator lamps on the CE panel can be tested by setting the command switch to LAMP TEST. This causes all indicators to light, except for indicators used with features not installed.

Bus Out

The bus out switches have two functions: (1) During a control command, these switches determine the command to be performed; (2) During any write operation, these switches determine the bit configuration of the byte written on tape.

If a control command and a write operation are performed in sequence, the bus out switches determine both the command and the bit configuration.

Check Stops

Setting the stop on check switch to the up position causes an operation to stop the moment an error condition occurs. The error that causes the stop can then be determined by inspection of the red checks indicators at the bottom of the CE panel.

The check reset pushbutton must be pressed to reset the error conditions and enable subsequent operations. The stop on check and check reset switches are operable off-line and on-line.

Blocks

Operations are performed one block at a time by setting the block switch to SINGLE. In this condition, the TC stops when a single block has been written or read. When writing, the length of the block is determined by the setting of the "go up" (formerly block length) control.

Operations are performed repeatedly by setting the block switch to MPLE. In this condition, the TC performs an operation for the length of a single block, stops for a certain length of time (determined by the setting of "go down" control), and repeats the operation for the length of another block. This sequence continues until either the stop or the reset pushbutton is pressed.

A continuous block is written by setting the write continuous switch to the up position and performing a write operation. In this condition, the go up and go down controls have no effect.

Single Out Tag

When performing single-block operations (block switch set to SINGLE), the initial selection portion of the operation can be performed one step at a time. This is done by setting the out tags/single switch to the up position and initiating each step of initial selection by pressing the start pushbutton.

Each time start is pressed, an out tag is generated and the initial selection is performed to the point where another out tag should be generated. The operation stops at that point and start must be pressed again to obtain the next out tag.

Write Single Character

Troubleshooting the CRCC, LRCC, and error circuits can be simplified in some instances by writing single data byte blocks. When the write single character switch is on during off-line write operations, blocks that contain one byte followed by a CRC and LRC character are created.

Parity Suppress

The parity suppress switch enables diagnostic mode. A diagnostic mode-mode set control command turns on the diagnostic mode latch. If the parity suppress switch is on when the diagnostic mode latch is on, no P bits are written during write operations. The suppress parity feature allows the creation of bad (even) parity bytes, or all-zero bit bytes which are of value in troubleshooting error detection, CRCC, and LRCC circuits. Diagnostic mode can be set by diagnostic programs or when operating the CE panel off-line.

Characteristic	Description
Reading and writing speed	18.75 inches/second
Rewind time (full reel)	4.0 minutes
Tape reel capacity	2,400 feet (max)
Tape speed (inches/second)	18.75
Byte density (bytes/inch)	800 556 200
Data rate (bytes/second)	15,000 10,425 3,750
Inter-record gap (nine-track)	0.6 inch
Inter-record gap (seven-track)	0.73 inch
Gap time (nine-track)	32 milliseconds
Gap time (seven-track)	38.6 milliseconds
Tape reversal delay (turnaround)	205 milliseconds
Magnetic tape:	
Width	1/2 inch
Thickness of base	0.0015 inch
Length	2,400 feet (max)
Tape format (standard)	nine tracks (8 data, 1 parity)
Tape format (optional)	seven tracks (6 data, 1 parity)
Power requirements	208 vac, 3 phase; 208 vac, single phase; 12 vac; 115 vac, single phase; +12v, -12v, -24 vdc. All supplied from tape control power supply.
Dimensions (each frame):	
Height	60 inches
Width	60 inches
Depth	29 inches
Weight:	
With tape control	1,400 pounds (2415)
Without tape control	600 pounds (2416)

Environmental conditions:	Operating	Nonoperating	Storage	Shipping
Room temperature (°F)	60-90	50-110	35-150	40-150
Relative humidity (percent)	20-80	8-80	0-80	0-100
Maximum wet bulb temperature (°F)	78	80	85	85

FINAL AMPLIFIER AND CLIPPING LEVEL CONTROL (FIGURE B-1)

- Final amplifiers shape and amplify pulses from the tape unit.
- The clipping level control ensures that pulses are of proper voltage.
- A data one-bit output of the amplifier circuit is a 2-microsecond negative pulse.
- Write clipping level voltage is 1.1 volts; normal read clipping level is 0.75 volts.
- After a read error, attempted rereads are automatically performed at three different voltage levels.

Final amplifiers shape and amplify one-bit pulses from the tape unit read bus. The final amplifiers route the pulses to the read register. The clipping level control ensures that only signal pulses of higher amplitude than a predetermined minimum (clip level) are permitted to pass through the amplifier to the read register; low-amplitude signals, usually noise pulses, are blocked.

Pulse Generation

Pulses from the tape unit enter the tape control on the read bus (Figure B-1). When the scanner is stopped, indicating the tape control is operational, the pulses are amplified by the amplifier block and sent to the limiter. On any one read bus line, normal one-bit pulses always alternate in polarity (NRZI). The amplifier has two output lines: one for positive pulses and one for negative pulses; these pulses are similar to the pulses on the read bus lines but are of greater amplitude and of the same polarity. The limiter passes only those pulses that meet the minimum voltage requirements as determined by the clipping level control block. The square wave output of the limiter is routed to a pulse generator which generates a 2-microsecond negative pulse for each 1 bit; this bit enters the read register position that corresponds to the same tape track. Figure B-1 shows one of nine final amplifier circuits (dashed line area) and clip level controls common to all track circuits.

Clipping Voltage Levels

The voltage on pin C of the clipping level block determines the minimum voltage level of the pulses that are permitted to pass through the limiter. Pulses with a voltage higher than the clipping voltage pass through the limiter, but pulses with a voltage lower than the clipping voltage will not pass through the limiter.

During a write operation, the bytes are read for error checking as they pass the read head. To ensure that the bits written are of sufficient amplitude to be read on subsequent read operations, higher standards are required on write than on read and the clipping level on pin G is 1.1 volts. If a read error occurs during write, a data check is signaled (to advise the control program to rewrite the block). Failure to read a bit at 1.1 volts during write is detected in the read register as a VRC error.

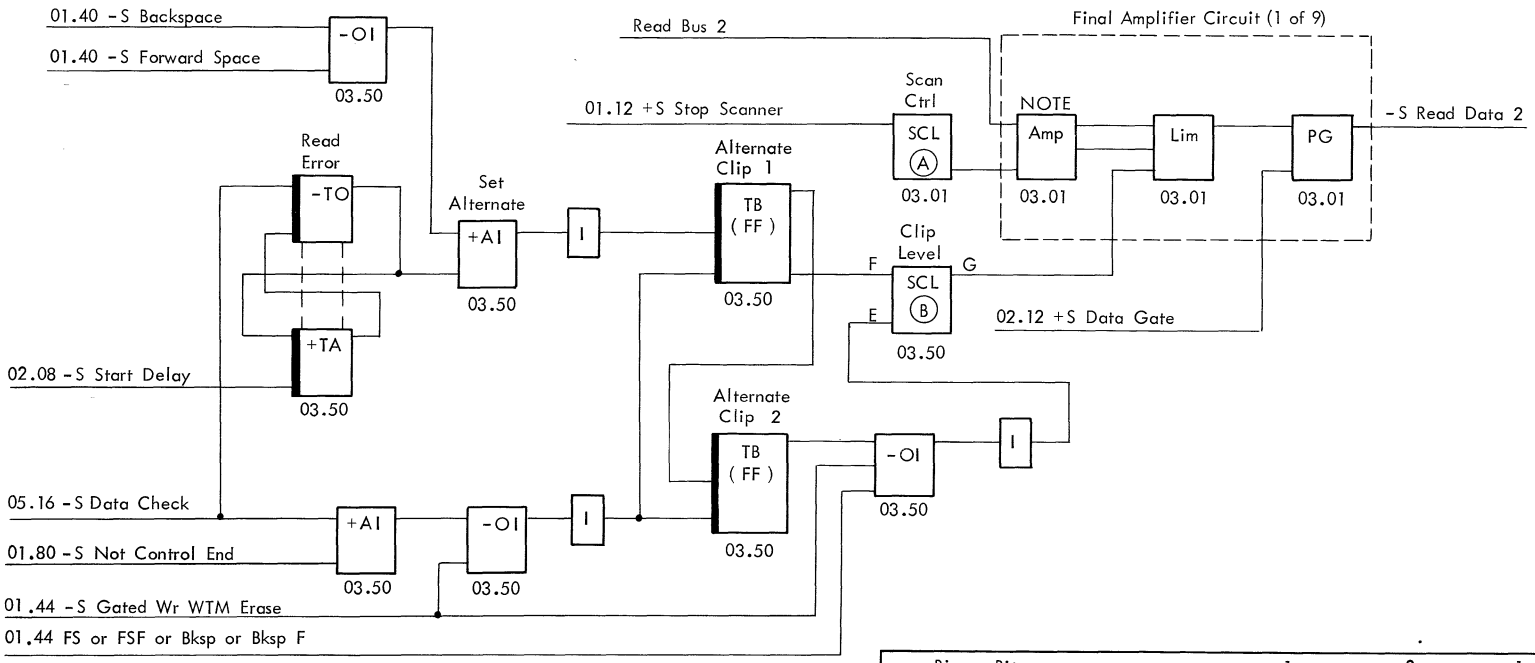
For a normal read operation, the clipping level is 0.8 volts. Any byte that is read correctly during the read check of write with the level at 1.1 volts may be read correctly at the read operation level of 0.8 volts, unless the tape is damaged or contaminated in the interim.

During a read operation, if a bit is too weak to pass through the limiter at this level a data register VRC is indicated. At the option of the system control program, the read operation can be repeated any number of times in attempting to read the block correctly. Three additional read clipping levels are automatically gated for successive attempts to reread after an error has been recognized.

Alternate Clipping

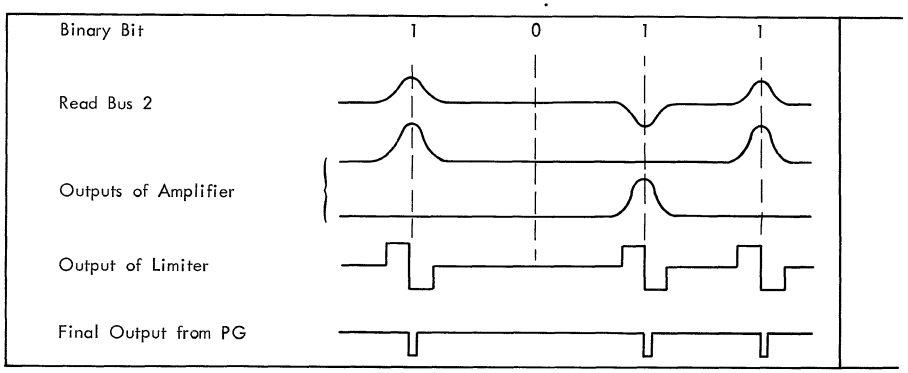
When a read error is detected, the data (register) VRC latch is set. The VRC latch activates data check which sets the read error latch. In order to reread the block, the tape unit must either forward space or backspace over the block. Either of these operations, along with the on condition of the read error latch, conditions the set alternate AND gate and the alternate clip 1 binary trigger is flipped. This causes pin F of the clipping level block to become positive, lowering the clipping level to 0.4 volts, for the first error reread in an attempt to read low amplitude bit signals which were missed at normal level.

If the error occurs again and another reread is attempted, the alternate clip trigger is again flipped



Clipping Voltage Levels (SCL Block (B))	PIN E	PIN F	PIN G
Write	-	-	1.1v
Normal Read	+	-	0.8v
* First Error Reread	+	+	0.4v
* Second Error Reread	-	-	1.1v
* Third Error Reread	-	+	0.6v

* This condition exists when read error is followed by forward space or backspace.



NOTE : Final amplifier 2 is shown as a typical example. The other eight final amplifiers are similar.

FIGURE B-1. FINAL AMPLIFIER AND CLIP LEVEL CONTROL

automatically and the clipping level is set at 1.1 volts; this is an attempt to screen out unusually high "noise" bits that may have caused the VRC error. If the error still occurs and another reread is attempted, the clipping voltage is set at 0.6 volts.

A byte that was read incorrectly because a bit was weak may be read correctly if the clipping voltage is lowered. If the error was caused by noise, raising the clipping voltage could result in a correct reading. However, it is possible that lowering the clipping voltage to read a weak bit will result in an error because of noise, and raising the voltage to eliminate noise will result in an error because a bit is now too weak. Therefore, the third attempt is made at an intermediate voltage of 0.6 volts.

If any attempt to re-read is successful (no data check), the binary triggers are reset when the not control end line (not forward or backspace attempt) goes positive at the end of the successful read. The clipping voltage will return to the normal 0.8 volts for the next read operation.

If an error persists, the clipping level is changed repeatedly for as many times as the system control program attempts to reread. Unless the block can be read without a data check, the block is said to contain a permanent error.

Address
  compare (TU) 2-4
  decode 2-3, 3-2
  decode latch 2-3, 3-2
  encode 2-3
  generator 2-3
  in tag 3-3, 3-16
  out tag 3-3
  panel jumpers 2-3
  select out circuits 2-2
  selection 1-10, 3-2
Addressing
  address decode latch 2-3
  address generator 2-3
  tape control 3-1
  TC address decoder 2-2
  TU address decoder 2-4
  TU selection 2-4
  unit free gating 2-4
Amplifiers
  final B-1
  first bit latch 2-19
Arm
  reset arm 2-8
  set arm 2-6, 3-13

Backspace or backspace file
  description 1-16
  end operation 3-10
  EOB search 3-10
  operation 3-10
  over data or TM 3-10
Backward go (see go)
Binary 1 or 0
  bit 1-3
Binary triggers (see triggers)
Bit
  alignment (skew) 1-4
  binary 1 or 0 1-3
  byte 1-3
  density 4-1
  write triggers 2-16
Block
  data 1-3
  gap 1-3
  spacing 1-3
Blocks and gaps 1-4
Brake signal
  turnaround 3-16
Buffering data
  channel 1-2
Burst mode
  force burst mode latch 2-10
  operational in tag 3-2
  operations 3-4
Busy
  force busy 3-2, 3-5
  long 1-12
  rewind 2-9, 3-5
  short 1-12, 3-2
  status bits 3-4

Bypass select
  attempt initial selection 3-2
Byte
  bit group 1-3
  block 1-3
  counts 4-4

C-compare
  circuit 2-25
  data convert 4-6
  description 1-19, 2-25
CE panel
  console 6-1
  description 1-21
  switches 6-1
Channel 1-2
Character
  bit group 1-3
  block 1-3
  check 1-5
  counts 4-5
  data conversion 4-1
Characteristics (2415) A-1
Check character
  CRCC 1-5
  LRCC 1-5
  parity 1-5
  reading 2-20, 2-21, 3-7
  writing 2-17, 3-11
Clipping level
  alternate clipping B-1
  data check B-1
  voltages B-1
Clocks
  read 2-18, 3-6
  write 2-15
Command byte
  cards 6-2
  codes 6-2
  command set 3-3
  decoding 3-3
  parity 2-11, 3-3
Command out tag (see initial selection)
  fall timing 3-16
  status rejected 2-12, 3-4
  stop latch 2-7, 3-6, 3-8, 3-11
Command register
  decoder 2-11
  description 2-11
  output gating 2-11, 2-12
  reset 2-12
  set 2-11
Command reject
  circuit 2-22
  description 1-19, 2-22, 3-5
  TAU reset 2-9
Command set (see initial selection)
Control unit
  priority 1-6, 1-7, 3-2
  tape control (2415) 1-7

Counters
byte and character 4-4
counter check 2-22
delay, write clock, sense 2-15
deskewing 2-17
Counting
command gate latch 2-11
read backward 3-8
read forward 3-7
write 3-12
CRCC (see check character)
CRC register 2-17
format 1-5
generation 2-17
purpose 1-5
read 2-20, 2-21
register shifting 2-18
write 2-17, 3-11
Data convert feature
c-compare 4-6
check (DCC) 4-7
description 4-1
error checks 4-6
operation 4-5
read 4-6
write 4-5
Data register
description 2-12
outputs 2-14
parity circuits 2-12
resets 2-14
set inbound 2-13
set outbound 2-13
Delay
erase gap 3-12
LP 3-6, 3-7, 3-11, 3-12
read 3-6
start 3-6, 3-7
stop 3-5, 3-7, 4-1
write 3-11
Delay counter (see EOB search)
binary triggers 2-15
drive modes 2-15, 2-16
microsecond mode 2-15
millisecond mode 2-16
oscillators 2-16
reset 2-16
sense counter 2-16
turnaround 3-16
write clock 2-15, 3-11, 3-12
Density
characteristics A-1
feature 4-1
Deskewing (see write triggers)
delay counter 2-17
skew 1-4
Device end
end status burst mode 3-14
end status interrupt 3-16
unit free 2-6, 3-13
Device end scanner (see scanner)
Diagnostic mode
mode set 4-2
End status (see status bits)
burst mode 1-17, 3-14
request in interrupt 1-18, 3-15
EOB search
backspace or backspace file 3-10
data convert operation 4-7
delay counter 2-15
forward space or space file 3-9
read backward 3-8
read forward 3-6
write 3-11
WTM 3-13
Erase before turnaround 3-16
Erase gap
description 1-15
end operation 3-12
operation 3-12
Error checking (see errors)
Error detection (see errors)
Errors (see parity checking)
bus out check 1-20, 2-23
c-compare 1-20, 2-25
command reject 1-19, 2-23
counter check 1-21, 2-15, 2-23
data check 1-19, 2-22, B-2
data register VRC 1-20, 2-24
equipment check 1-19, 2-22
error checking 1-19
error detection 2-22
IBG noise 1-20
LRCR check 1-20, 2-24
overrun 1-20, 2-24
read B-1
read parity checks 2-22
read register VRC 1-20, 2-24
ready drop 1-21, 2-24
skew error 1-20, 2-23
word count 0 1-20, 2-23
write parity checks 2-22

Feature
data flow 4-1
descriptions 4-1
functional units 4-2
operations 4-1
File
description 1-4
space file operations 3-8
Final amplifiers (see amplifiers)
First bit
latch 2-19
read clock 2-18
read data 3-6, 3-7
Force burst mode (FBM) latch
end status burst mode 3-15
operational in tag 3-2
resets 2-11
set 2-10
Format
bit 1-3
byte 1-3
character 1-3
data 1-3

sense byte 1-14
tape block 1-3
tape mark 2-20
Forward space or space file
description 1-16
end operation 3-9
EOB search 3-9
operation 3-9
over data or TM 3-9
Forward go (see go)

Go
backward 3-7, 3-10
forward 3-6, 3-9, 3-11, 3-12
turnaround 3-16, 3-17
Green and go
command busy reset 3-15
idle reset 2-9, 3-15

Halt I/O
interface reset 2-7
stop latch 2-7

IBG
blocks and gaps 1-4
gap 1-3
noise 1-20, 2-24
size 4-1
Indicators
CE panel 1-21, 2-12, 6-1
error checking 1-19
Initial selection
begin operation 1-11, 3-3
command set 1-11, 3-3
description 1-10
operation 3-1
stack status 2-12, 3-3
status byte 3-3
Inject parity
c-compare 2-25
write parity check 2-22
Interface lines 1-7
I/O
control 1-2
devices 1-1

Latches
address decode 2-3
address in 2-10, 3-3, 3-16
backward end 3-7, 3-41
brake 3-16
chain (stop scan) 2-5, 3-13, 3-15
channel end (see status bits)
command busy 2-11, 3-3, 3-15
command gate 2-11
command register 2-11
CRC time 3-13
CU end (see status bits) 2-4
data gate 2-21, 3-6, 3-10, 3-11
data register 2-13
data register reset 2-14
data time 2-20
deskewing counter 2-17
device register 2-4
end write (stop write) 3-11
EOB search 3-6, 3-9, 3-10, 3-12
error latches (see errors)
first bit 2-19
first character 2-21, 3-6, 3-7, 3-10, 3-11
force busy 3-2, 3-5
force burst mode 2-10, 3-15, 3-16
internal stack 3-16
LP delay -- LP erase 3-6, 3-7, 3-10, 3-11, 3-12
mode register 4-2
on-line 2-1
operational in 2-10, 3-15, 3-16
P-bit trap (bus out) 2-12, 2-25, 3-3
read disconnect 3-6, 3-9, 3-12
read error B-1
read register 2-19
rewind hold 3-13
rewind busy 2-9, 3-5
service in 3-5, 3-6, 3-8, 3-11
service in tag 3-5, 3-6, 3-8, 3-11
skew gate 2-22
stack 2-12, 3-4, 3-15, 3-16
start delay 2-21, 3-6, 3-7, 3-10, 3-11
status 2-14
status in 2-11, 3-14, 3-15, 3-16
status in tag 3-6
stop 2-7, 3-6, 3-8, 3-11
stop delay 3-6, 3-9, 3-12
tape mark 2-20, 3-9, 3-10
TAU reset 2-9, 3-4, 3-5
TU select 2-5, 3-2
turnaround 3-16
unit check (see status bits)
unit exception (see status bits)
write check character 3-12, 3-13
write condition 3-11, 3-12, 3-13
write pulse 2-17, 3-13
Load point
backward at 3-7
read LP delay 3-6
rewind at 3-14
tape markers 1-1
write LP delay 3-11
Long busy 1-13
LRCC (see check character)
checking 2-19
format 1-5
LRCR VRC 1-20, 2-24
purpose 1-5
LRC register 2-19
read 2-20, 2-21
write 2-19, 3-11

Magnetic tape 1-1
Magnetic tape device 1-1
Metering
controls 1-7, 1-21
interface lines 2-1
on-line latch 2-1
usage meter 2-1
Microsecond mode
delay counter 2-15
Millisecond mode
delay counter 2-16
Mode set commands 4-2

NRZI method of recording
description 1-9
write triggers 2-16
On/off line control
CE panel 2-12, 6-1
Operational in latch
in tag 3-2
reset 2-10
set 2-10
Overload control
power supply 5-1

Parity checking
byte 1-3
character 1-3
check (C) bit 1-3
command byte 2-11
data register 2-12
error checking 1-19
error detection 2-22
parity bit 1-3, 4-4
Parity inject
write parity check 2-22
Power supply
CB's 5-1
contactors 5-1
controls 5-2
description 1-21
sequence 5-1
voltages 5-1
Priority
bypass select 3-2
control unit 1-7, 3-16

Read
backward operation 1-17, 3-9
clock 2-18, 3-6
data block 3-6, 3-8
delay 3-6, 3-7, 3-9, 3-10
first bit latch 2-19
forward operation 1-17, 3-5
method 1-9
register 2-19
register VRC 1-20, 2-24
stop 1-17, 3-6, 3-8
Read error
clipping levels B-2
latch B-2
permanent B-2
Read/write control command 1-15
Read/write heads
magnetic tape device 1-1
skew adjustment 1-4
Ready drop
description 1-21, 2-24
ready end control 2-10
Recording (see NRZI)
Registers
command 2-11
CRC 2-17
data 2-12
device (TU address) 2-4
LRC 2-19
mode 4-2
read 2-19
Request in 3-15
Resets
arm 2-9
check 2-8
data register 2-14
early 2-9
end operation (TAU) 2-9
general 2-6, 3-1
idle 2-9, 3-15
interface 2-6
interface disconneot 2-7
machine 2-7
malfunction 2-6
manual 2-8
power on 2-8
selective 2-6
sense 2-8, 3-3
status 2-8, 2-15, 3-4
system 2-6
TAU 2-9, 3-4, 3-5, 3-15
2415 TC 2-7
Rewind or ready end control 2-10
Rewind or rewind-unload
description 1-15
end operation 3-14
operation 3-13

Scanner
device end 2-4, 2-6
device register 2-5
rewind or rewind-unload 3-13
sequence 2-5
stop scan 2-5, 3-14
Select signal
bypass 3-2
lines 1-7
priority jumpers 2-2
reed relay card 2-2
select out circuits 2-2
switching and gating 2-1
Selection (see addressing)
address 1-10, 3-2
bypass select 3-2
controls 1-7
initial 1-11, 3-3
tape unit 3-2, 6-2
Sense (see errors)
bytes 1-14, 3-5
cycles 3-5
description 1-13
end 3-5
operation 3-5
Sense counter (see delay counter)
operation 3-5
read clock 2-18
Set count (see counting)
Seven-track features 4-1
Short busy 1-13, 3-2
Skew
adjustment 1-4
check 1-22, 2-23
deskewing 2-16
electrical 1-4
error 1-20, 2-22
mechanical 1-4

Space operations 1-16, 3-8
Stack
  status rejected 2-12, 3-4
Status
  accepted 2-12, 3-4, 3-15, 3-16
  bits 1-18, 2-15, 3-4, 3-7, 3-8, 3-10, 3-12, 3-13, 3-14
  bytes 2-14
  end operation 3-14, 3-16
  initial 1-11, 3-3, 3-4
  latches 2-14
  reject (stack) 2-12, 3-4, 3-15, 3-16
  response 1-11
Status pending
  request in 3-15
  short busy 1-13, 3-2
  TU address compare 2-4
Substitute blank 4-4
Suppress out 3-15
Switches
  CE panel 6-1
  channel rotary step 5-1
  meter 2-1, 5-2
  power on/off 5-2

Tape
  block format 1-3
  magnetic tape 1-1
  markers 1-1
Tape control
  control unit 1-2
  functions 1-2
  system relationship 1-2
  2415 TC 1-7
Tape mark
  configuration 3-12
  feature operation 1-17
  file 1-4
  format 2-20
  read 3-6, 3-7
  recognition 2-20
  write 3-12
Tape motion
  control commands 1-15, 3-4, 3-12
  read backward 3-7
  read forward 3-6
  space or space file 3-8
  write 3-11
Tape motion control commands
  description 1-16
  operations 3-4
Tape tracks
  magnetic tape device 1-1
Tape unit
  magnetic tape device 1-1
  select latch 2-5, 3-2
Test I/O
  decoding and P bit 2-11
  operation 1-12
Translators 4-2
Triggers
  alternate clipping B-1
  character counting 4-5
  delay counter 2-15
  LRC register 2-19
  read clock 2-18
  write 2-16
Turnaround
  description 1-19
  erase before 3-16
  operation 3-16

Unit free
  after rewind-unload 3-14
  device end 2-6, 3-13
  gating 2-4
  scanner 2-5, 3-13
  selected 3-15
  signaling 2-5, 3-13
Usage meter
  metering controls 1-7

Write
  data block 3-11
  description 1-16
  first byte 1-16, 3-11
  operation 3-11
  stop 1-16, 3-12
  tape mark 3-12
Write clock (see delay counter)
  operation 2-15, 3-11, 3-12
Write condition
  delay counter-write clock 2-15
  write data 3-11
Write delay (see delay)
  magnetic tape device 1-1
Write disconnect
  delay counter-write clock 2-15
  end write latch 3-11
  stop write 3-11
Writing on tape
  bits on tape 2-16
  CRC character 2-18
  data block 3-11
  deskewing 2-16
  LRC character 2-19
  method of 1-9
  tape block format 1-3
Write pulse
  latch 2-17
  write triggers 2-16, 3-11
Write tape mark (WTM)
  description 1-16
  operation 3-12
Write triggers
  deskewing 2-16
  resets (write LRCC) 2-19, 3-11, 3-13

CUT ALONG LINE

COMMENT SHEET

IBM 2415 MODELS I–3 TAPE CONTROL

FIELD ENGINEERING THEORY OF OPERATION, FORM Y22-2918-0

FROM

NAME _____ OFFICE/DEPT NO. _____

CITY/STATE _____ DATE _____

To make this manual more useful to you, we want your comments: what additional information should be included in the manual; what description or figure could be clarified; what subject requires more explanation; what presentation is particularly helpful to you; and so forth.

How do you rate this manual: Excellent ____ Good ____ Fair ____ Poor ____

Suggestions from IBM Employees giving specific solutions intended for award considerations should be submitted through the IBM Suggestion Plan.

NO POSTAGE NECESSARY IF MAILED IN U.S.A.

FOLD ON TWO LINES (LOCATED ON REVERSE SIDE), STAPLE AND MAIL

fold fold

FIRST CLASS
PERMIT NO. 81
POUGHKEEPSIE, N.Y.

BUSINESS REPLY MAIL

NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

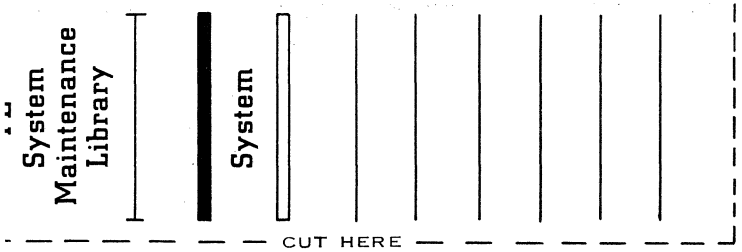
POSTAGE WILL BE PAID BY . . .

IBM CORPORATION

P.O. BOX 390
POUGHKEEPSIE, N.Y. 12602

ATTENTION: FE MANUALS, DEPT. B95

fold fold



Y22-2918-0

Printed in U.S.A. Y22-2918-0

IBM

International Business Machines Corporation
Field Engineering Division
112 East Post Road, White Plains, N.Y. 10601